DESIGNERS' GUIDE TO POWER PRODUCTS

APPLICATION MANUAL

SGS-THOMSON MICROELECTRONICS

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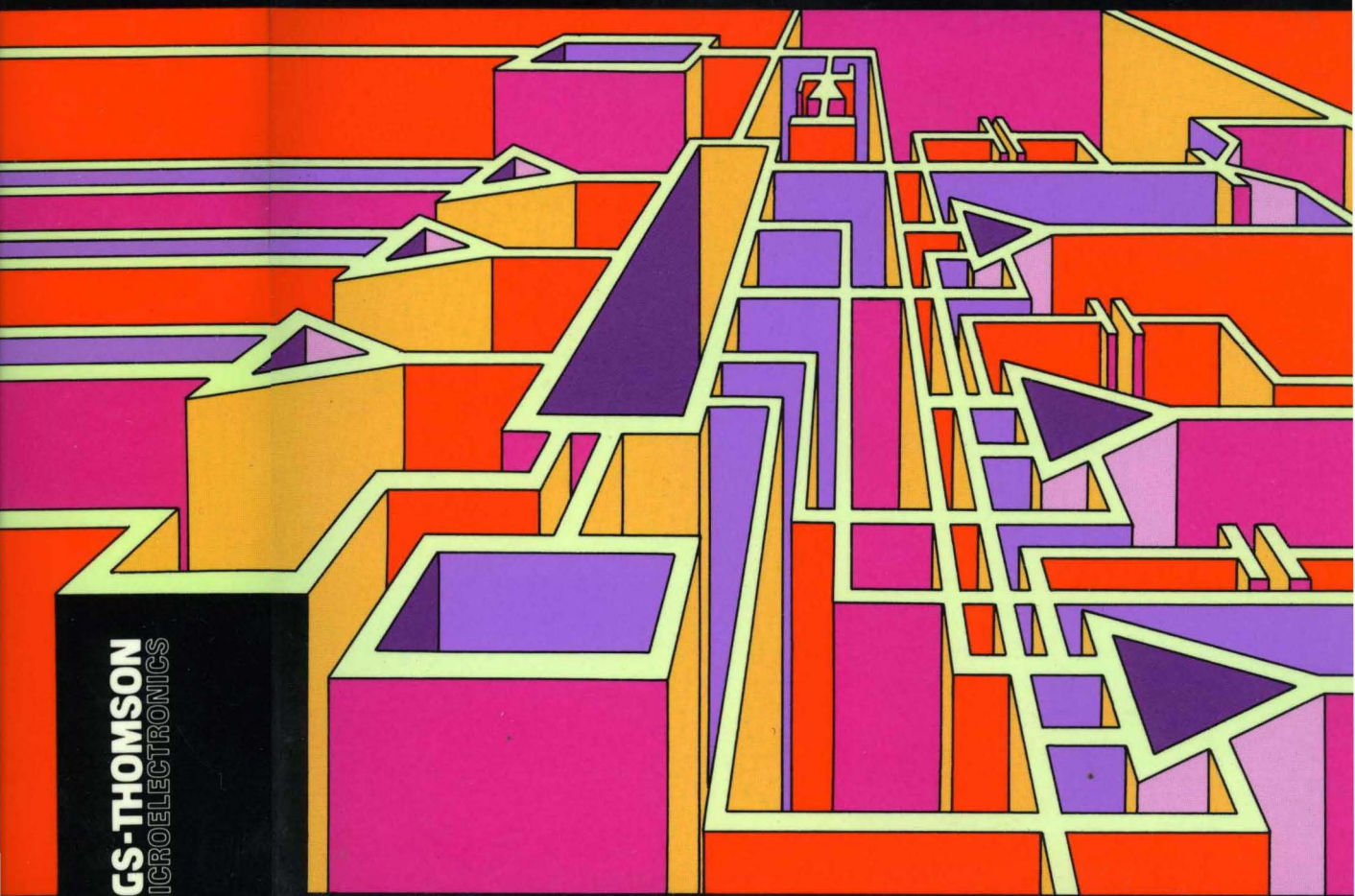
APPLICATION MANUAL

2nd EDITION



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USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

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1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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THE BRIGHTER POWER

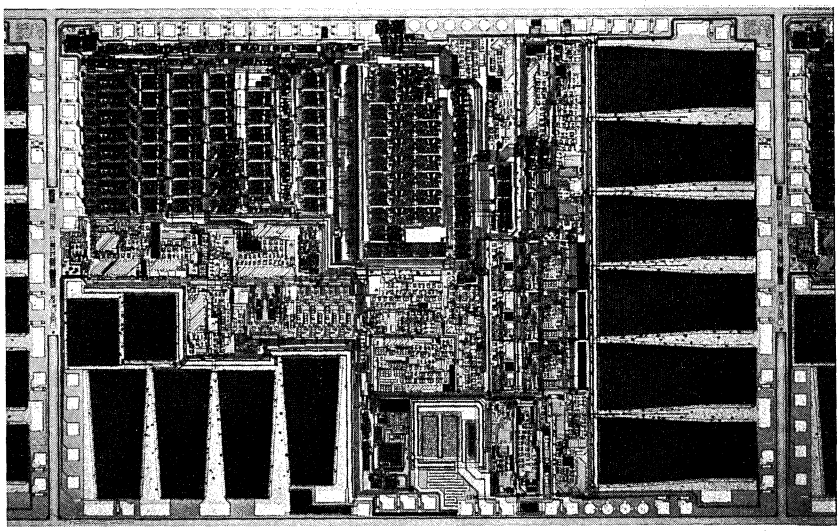
This book has been written for those interested in taking advantage of the most recent advances in power integrated circuits. Smart power integrated circuits together with power discrete devices form the heart of modern power electronics.

SGS-THOMSON is well established in the field of power electronics, both for power discretes and power integrated circuits. In particular, the company is a world leader in power integrated circuits. Ever since rankings were published for the fast-growing power IC and smart power IC markets SGS-THOMSON has been number one. Moreover, the company has a share almost twice that of the nearest competitor in both power IC markets.

Our long term experience in bipolar discretes has led to reliable rugged devices using state-of-the-art bipolar structures and both single and double implanted planar edge termination techniques that meet today's demand for very high switching speeds and high breakdown voltages.

These techniques are not confined to bipolar transistor fabrication. High voltage Power MOS using high efficiency edge structures and platinum ion implanted IGBTs use flexible processes that produce a range of rugged high voltage devices ideal for switchmode applications.

SGS-THOMSON's leadership in power IC technology has its roots in its pioneering work at the end of the '60s, when the first ICs combining power circuits and control circuits were first created. Initially this technology was used in applications such as audio amplifiers, voltage regulators and TV deflection circuits. Later it was extended to applications such as motor and solenoid driving.



Thanks to an advanced 2nd generation BCD smart power process, SGS-THOMSON integrates highly complex power subsystems on a single chip. This IC, designed for a hard disk drive, controls and drives both the spindle motor and the head positioner. It includes more than 10,000 transistors.

INTRODUCTION

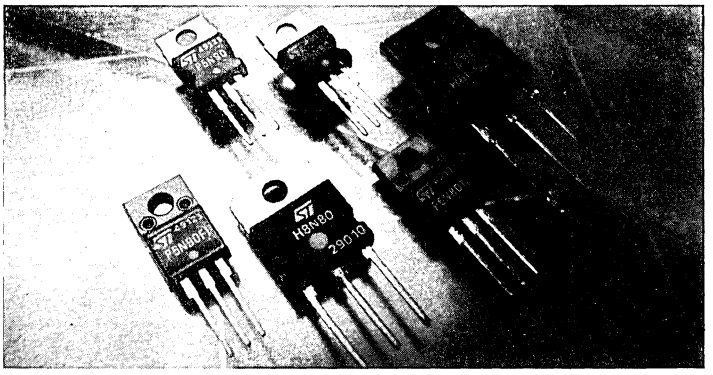
In the early eighties another major step forward was taken when SGS-THOMSON introduced a new power IC technology that combined bipolar CMOS and DMOS power transistors on the same chip.
Unlike other "smart power" technologies, this allowed the integration of isolated DMOS transistors so any number could be placed on one chip and interconnected in any way. Recently a shrink version of this technology has been introduced. Thanks to 2.5µm geometries this version makes it possible to integrate very complex LSI power circuits on one chip.

One example of the new generation is a single chip that controls and drives three motors in a fax machine. Another circuit drives the head positioning and spindle motor actuators of a 2.5" hard disk drive. This power IC, made with the 2nd generation BCD process, integrates highly complex power subsystems on a single chip. It includes more than 10,000 transistors.

In addition to the BCD technology, VIPower ICs have been developed. These unique monolithic power ICs are based on discrete transistors with current flowing vertically through the silicon and have integrated control circuits constructed on-chip. Three sub-families of power ICs have been derived from this technology. Included in these sub-families are bipolar output ignition drivers rated at 450V, 8.5A and Power MOSFET output high-side drivers with an $R_{DS(on)}$ as low as 30mΩ and $V_{(BR)DSS}$ of 60V and low-side drivers rated at 450V, 0.75Ω.

Because most SGS-THOMSON power ICs are innovative the company places great emphasis on application support. For many products there are sophisticated application development tools - hardware and software - for use with the lab PC. The company also regularly publishes application documentation. This volume is a follow-on from the Smart Power Application Manual, reflecting the broader scope of power electronics. It includes application notes and other useful material about SGS-THOMSON power ICs, power technologies and power discretes.

SGS-THOMSON's innovative smart power processes are made to fit the needs of today. By providing complex functions in small, rugged and easy to use packages the task of system design is made easier and the system reliability is improved.



A variety of high voltage Power MOS in power packages to suit today's environments.

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APPLICATION NOTE

SMART POWER PROCESSES FOR LSI CIRCUITS

by Carlo Cini

Over the years smart power technology has advanced to ever-increasing power and voltage levels. At the same time, almost unnoticed there has been a remarkable increase in the smartness of circuits -- the amount of complexity that can be integrated practically on one chip.

Today, for example, it is possible to integrate circuits like the one shown in figure 1, which contains two 1A motor drives, a 3A solenoid driver, a 1A switchmode power supply and a micro interface (this chip will be described in more detail later). Clearly the possibility of integrating so much of a system has a dramatic effect on the way system engineers approach partitioning; complexity is no longer limited by technology, but by economic factors.

The technologies that allow such circuits to be made are generally known as "BCD" technologies because they combine bipolar, CMOS and DMOS process structures. First introduced by SGS in 1986, they allow IC designers to use bipolar components when high precision is needed (in references etc), CMOS for high density digital and analog, and power DMOS for low dissipation output stages.

Low dissipation is, in fact, one of the key advantages of BCD technology. A DMOS power transistor in switchmode operation dissipates very little power so it is possible to deliver high power to the load without expensive power packaging and cooling systems (the power that can be dissipated inside an IC is determined by the package). Equally important is the fact that low dissipation power stages make it feasible to place several power stages on the same chip. This, together with the high density CMOS, makes high complexity circuits feasible.

BCD TECHNOLOGY

The first commercial process to combine bipolar, CMOS and power DMOS was the Multipower-BCD process introduced by SGS-THOMSON in 1986. A 60V technology, this was created by merging vertical DMOS technology with a conventional junction-isolated bipolar IC process (figure 2).

Figure 1: A High Complexity Smart Power IC Containing Multiple Drivers.

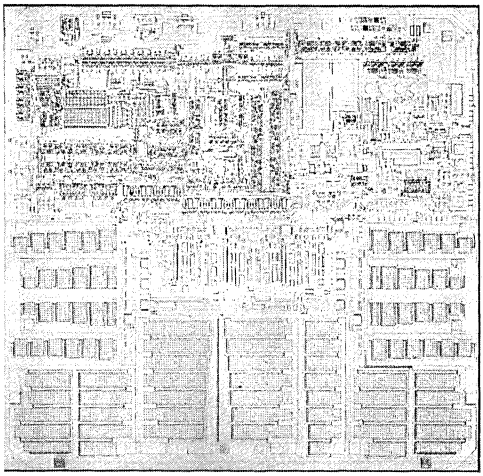
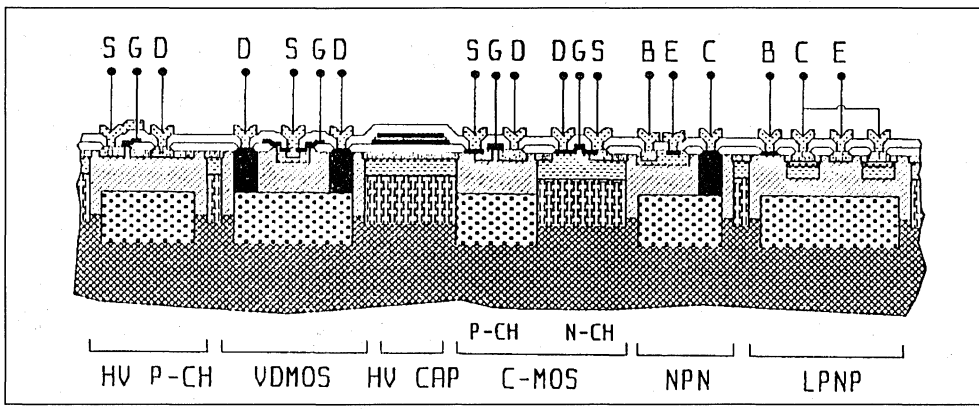


Figure 2: Cross Section of the Multipower-BCD Process.



An important characteristic of this technology is that it provided all of the contacts on the top surface of the die and completely isolated the power DMOS transistors. This was important because it allowed the integration of any kind of power stage: high side, low side, half bridge or bridge. Moreover, multiple power stages could be integrated on one chip.

Having bipolar, CMOS and DMOS structures available gives the designer freedom to choose the most appropriate for each part of the circuit. Bipolar structures are used primarily in linear functions where high precision is needed: low offsets, low drift and so on; it can also be useful in predriving stages. CMOS is useful both for high density logic and high density analog circuits where high precision is not needed.

DMOS power stages have several important advantages over their bipolar equivalents. Most important is the low dissipation, which is because DMOS devices need no driving current in DC conditions and operate very efficiently in high-speed switching applications. Other advantages include the freedom from second breakdown and the presence of an intrinsic freewheeling diode, which is useful with inductive loads.

Since the original 60V process was introduced several other process variations have been introduced: a 100V version, a 250V version and a new family of shrink processes called BCD-II, which use a 2.5u geometry. The evolution of these can be continuous and to give an idea of the improvement made and forecasted there are two values (Ron x area and number of transistors per square millimieter, which express clearly the strength of a technology. For the power components there is the Ron x Area parameter which indicates for a given area the reduction in ON resistance, and hence the improvement in the electrical efficiency, or rather, the reduction of the power dissipated. This parameter appears to improve by a factor of two every four years. In the signal section the most common parameter is the number of transistors per square millimeter. Here progress is more marked than in the power section because it is possible to exploit the knowhow existing in VLSI technology where the microlithography is the dominating factor and not the current.

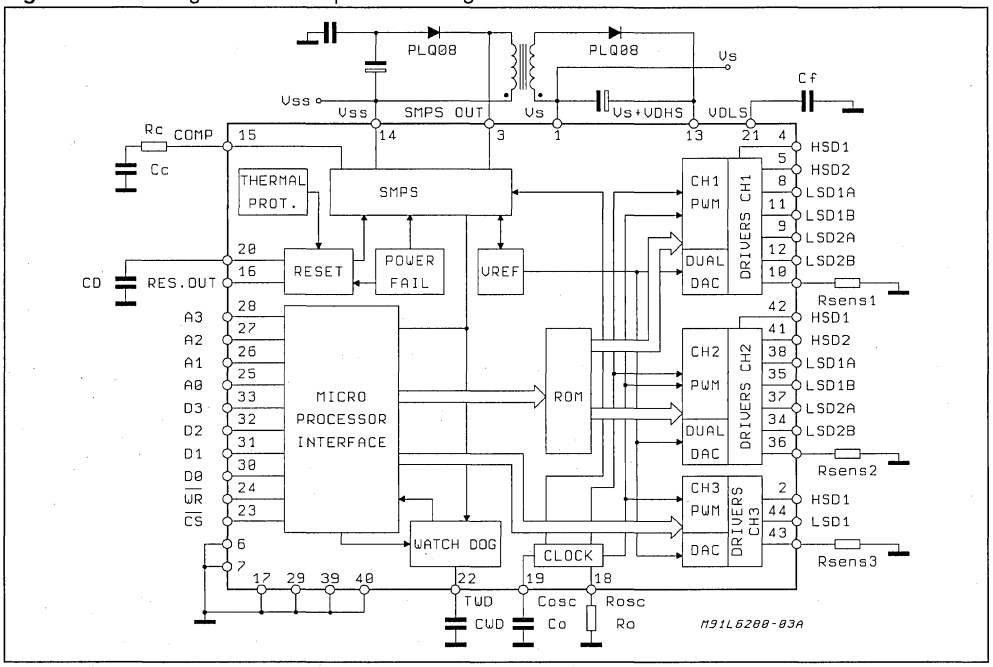
A high voltage (>600V) version is also close to introduction. The 60V and 100V versions cover the majority of applications today, in industrial, computer peripheral, automotive and consumer products. At present the main applications for 250V technology are in lamp ballasts and power supplies, though it is expected that when new high pressure gas discharge lamps are adopted by the automotive industry circuits in this technology will be appropriate. The expected uses of 500V technology are mainly in offline power supplies and home automation.

EXAMPLE PRODUCTS

We will now examine some typical BCD IC exemplify the remarkable versatility of the technology. Figure 3 shows the block diagram of a chip introduced in 1988 for a portable typewriter application -- the chip shown in figure 1.

This circuit integrates 15 power DMOS transistors and about 4000 other transistors. On this chip are all of the power subsystems needed in the typewriter: a 1A motor drive for the carriage positioner, a 1A motor drive for paper feed, a 1A motor drive for the daisy wheel, a 3A solenoid driver for the hammer and a 1A/5V switchmode supply that power the micro. In addition the chip includes all of the interface circuits, control logic and protection circuits. One interesting characteristic of this circuit is that most of the functions are programmed by loading internal registers. It is even possible to program output stage configurations,

Figure 3: Block Diagram of the Chip Shown in Figure 1.



an interesting concept that makes the device more flexible than one would expect from such a complex and highly-specific solution.

With the introduction of the shrink version, BCD-II, circuits of this complexity have become smaller and less expensive. Figure 4 shows a recent example of a custom circuit in BCD-II technology for a computer peripheral application that includes a servo positioning system, motor controller and various other functions that were not integrated on other ICs on the board.

Figure 4: Complex Smart Power Chip Realized with Shrunk BCD-II Process.

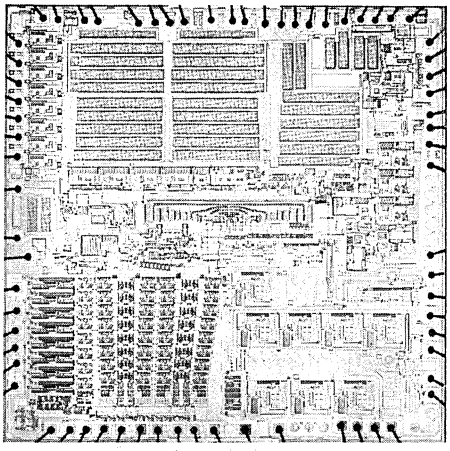
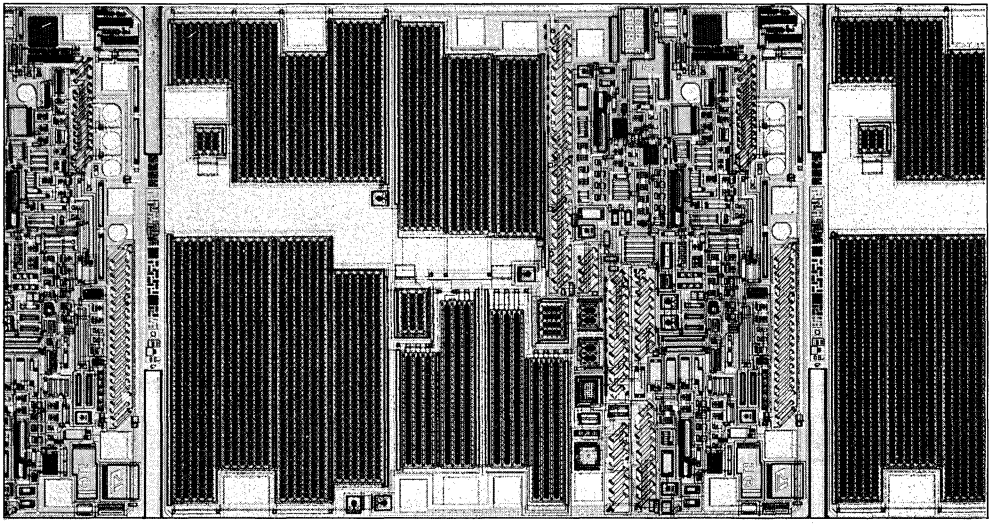


Figure 5: A Multiple Linear Regulator Chip in BCD Technology.



Though most BCD circuits use switchmode DMOS power stages it is also possible to use the technology in linear applications, as illustrated in figure 5, which shows a quad linear regulator chip. Designed for a car radio, this circuit contains four regulators (10V/60mA, 8V/50mA, 5V/300mA, 5V/600mA) with bipolar PNP pass transistors. BCD technology was chosen in this case for several reasons: low current drain, compact die size and the possibility of having an uninterrupted positive output even in the presence of a negative dump transient.

The circuit shown in figure 6 is an example of a multiple power chip for the automotive market. This chip is used in rearview mirror units and drives the three motors (mirror adjust up/down, adjust left/right and fold) plus the defroster heating element. Mixed bonding is employed in this circuit.

Figure 7 shows a practical high voltage IC fabricated in BCD250 technology for a compact fluorescent lamp ballast application. A DMOS bridge output stage is clearly visible.

Figure 6: Multiple Smart Power Chip for Car Mirror Control.

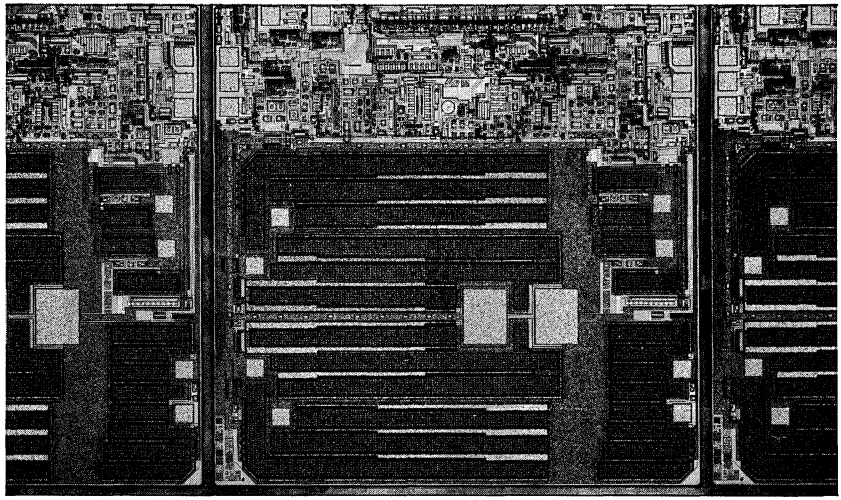
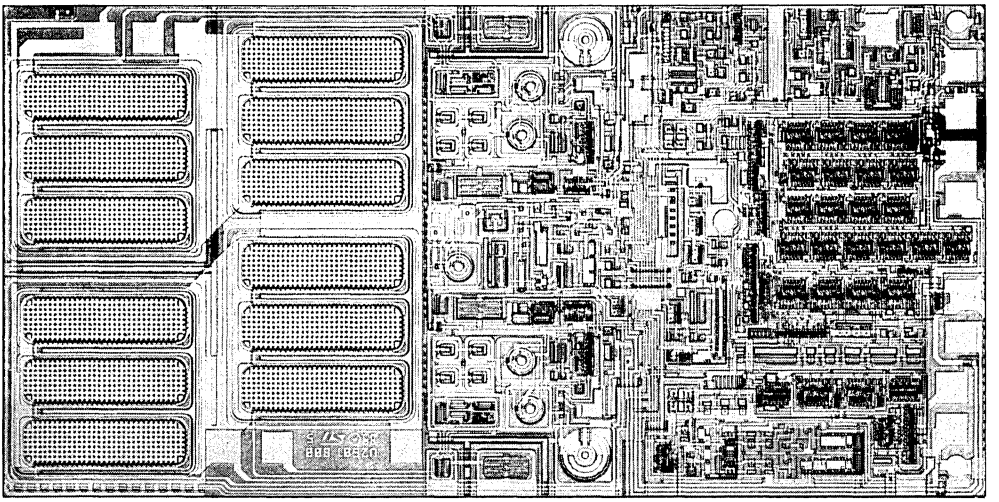


Figure 7: High Voltage IC for Electronic Lamp Ballast.

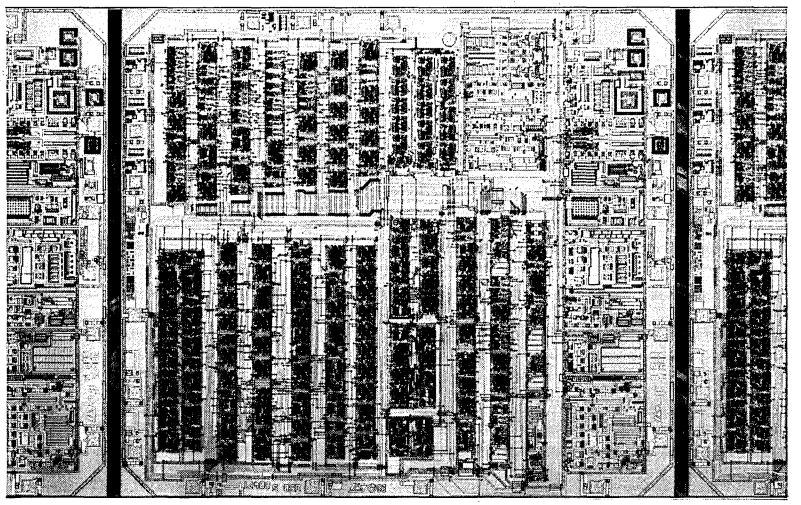


FAST DEVELOPMENT

The design of a BCD smart power IC, even a complex one, is surprisingly short. From the original idea to having a part working perfectly in the application takes typically six to ten months. These parts may not meet the original spec 100%, or SGS-THOMSON's yield standards, but they are good enough to use in production. Very complex ICs can be developed in roughly the same time because it is possible to divide the work between several designers. Unlike digital chips, in fact, a smart power IC is often designed by a single design engineer. This fast development is possible because such circuits almost always use just well known and predictable elements -- mainly library cells -- which are simply interconnected. And unlike linear power ICs, the DMOS power stages usually operate in switch-mode, which makes their behavior more predictable. The low power dissipation of power DMOS also helps because it minimizes unwanted thermal interactions.

In some cases the designer may also opt to use automatic layout techniques. This method is fast,

Figure 8: Example of Layout Generated Using Automatic Software Tools.



though it is not used where die size has to be reduced using manual layout. The circuit shown in figure 8 is an example of a BCD circuit laid out using automatic design tools.

Further time is saved by the application of 100% layout verification using CAD. This practically eliminates the risk of the first silicon not working because of a layout error.

PACKAGES

In power ICs, where dissipation is a fundamental limit, packaging very often determines both the performance and the cost of ICs. Fortunately for users of automatic assembly equipment in this area radically new packaging concepts are not expected in the near future. All of the ICs described here are, in fact, housed either in DIP, chip carrier or power packages like the Multiwatt 15-lead power tab package.

For high complexity types, where the pin count is generally high, plastic-leaded chip carrier PLCC packages are very popular. By modifying the lead frame, replacing all of the leads on one side by a triangular head spreader, it is possible to dissipate as much as 2.5W in a 44-lead PLCC. This is the package used for the chip in figure 1.

Where the highest output power is needed packages like the Multiwatt are used. To cope with the high currents involved in some circuits a mixed bonding technique has been developed for this package, using thick aluminum wires for the high current connections and thin gold wires for the others. An example of this is shown in figure 9, a 10A switching regulator IC. Thick aluminum could not be used for all connections because the large bonding pads required would waste too much silicon area; the use of multiple gold wires for power connections would compromise reliability.

BCD technology is often described as "mixed", primarily because it mixes bipolar, CMOS and digital. But it can also be described as mixed because it mixes analog and digital, because it mixes signal and power, because it mixes thick and thin metallization, and because of the mixed bonding technique.

Figure 9: An example of a power IC using mixed wire bonding.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SMART POWER TECHNOLOGY EVOLVES TO HIGHER LEVELS OF COMPLEXITY

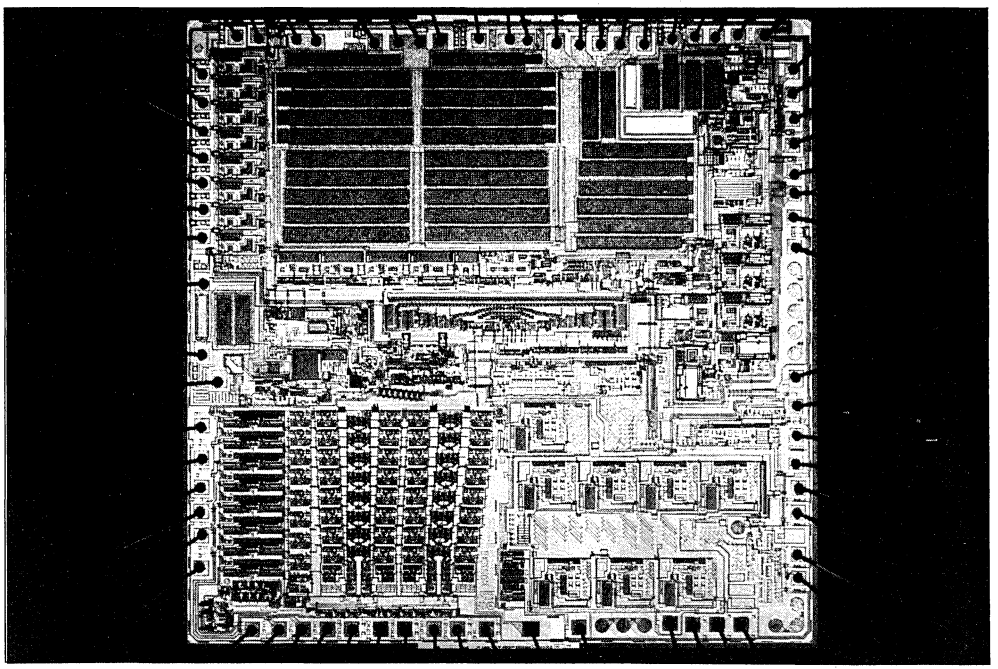
by Bruno Murari

Smart power devices are the shooting stars in power semiconductors, because it's possible to integrate digital and analog functions together with multiple power stages on the same silicon chip. The trend towards higher density will continue.

Since it was first introduced in 1986, mixed bipolar/CMOS/DMOS smart power technology has evolved rapidly, extending voltage capability and integrating highly complex subsystems on single chips containing thousands of transistors.

Integrated circuit fabrication technologies that combine bipolar, CMOS and power DMOS structures on the same chip have had a significant impact on "smart power" integrated circuit design. Since the dissipation of power DMOS stages in switchmode operation is very low it is possible to produce ICs capable of delivering substantial power to the load without the usual heatsinks, cooling fans and so on. Moreover, because it permits the integration of high-density CMOS and multiple DMOS power stages the traditional constraints on complexity are removed and circuits containing complete subsystems have been produced. An example of this is shown in figure 1 — a custom IC that integrates a motor control system, servo positioning system, a step up converter, microprocessor interface and other circuits.

Figure 1: An example of the complexity now possible in smart power ICs. This custom LSI device developed by SGS-THOMSON for a computer peripheral application that integrates a servo positioning system, DC motor controller/driver and various other "glue" functions" not integrated in the other ICs on the board.



BCD TECHNOLOGY

A power IC technology combining bipolar, CMOS and power DMOS was first introduced by SGS-THOMSON in 1986. Called Multipower-BCD, this was a 60V process created by merging a conventional junction-isolated bipolar IC process with vertical DMOS technology. The result is a process requiring 12 masks in the standard version — no more complex than modern bipolar technologies.

Where this process departed significantly from previous smart power processes is that it employs isolated DMOS power devices. The significance of this is that designers are not limited to a single power DMOS transistor per chip, but can have any number (hence "Multipower") and connect them in any way. Thus it is possible to integrate any power stage configuration (low side, high side, half bridge or bridge), or even to have several complete power stages on the same chip.

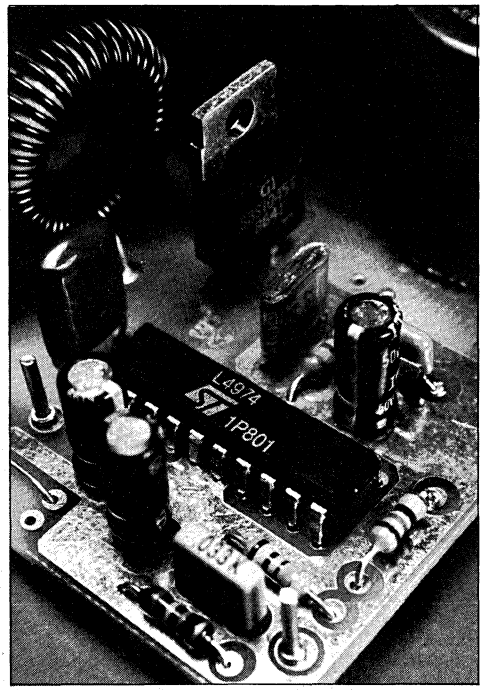
Clearly the combined BCD process gives circuit designers the possibility of choosing the optimal technology for each circuit function: bipolar is the first choice for linear functions where high precision and low offsets are required; CMOS is best for complex analog and digital signal functions because of its high density; and power DMOS is ideal for power stages.

It is the possibility of integrating power DMOS stages that gives BCD technology its greatest advantage: low dissipation. Unlike bipolar power transistors, power DMOS devices need no driving current in DC conditions and operate very efficiently in fast switching operations.

This low dissipation can be exploited to increase the amount of useful power that can be achieved with a given package. For example, both SGS-THOMSON's L296 bipolar power switching regulator and the functionally similar L4970 BCD type are assembled in the Multiwatt package, but the bipolar version delivers up to 160W while its BCD counterpart delivers up to 400W.

An alternative way to profit from low dissipation is to use less costly low power packages in place of high power packages. Very often a bipolar power IC in a power package can be replaced by a BCD part in a DIP, or even PLCC or SO, package. This can bring substantial savings not only because power packages are more costly, but also because they are more costly to mount on the board and are not well suited to automatic assembly. For example, a 4A bipolar switching regulator IC in the Multiwatt package can be replaced by a BCD switching regulator in a DIP package (figure 2) which delivers almost the same current.

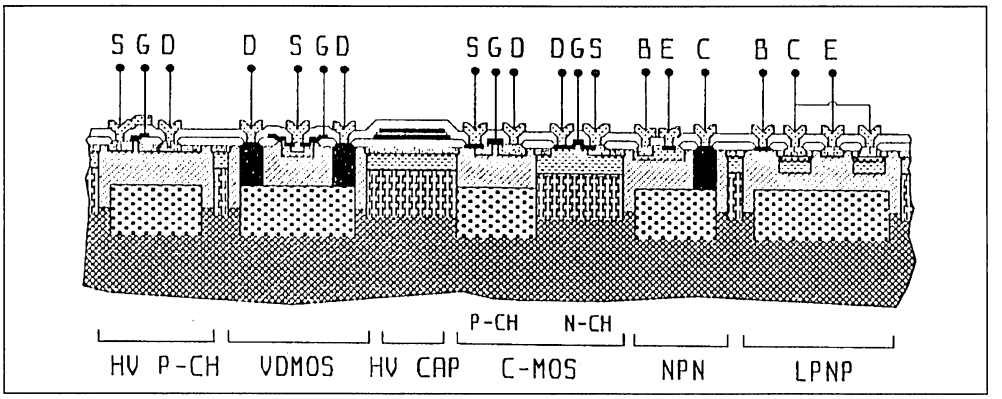
Figure 2: The low dissipation of power DMOS can be exploited to make power ICs in low power packages, which are less expensive and easier to mount. This DIP-packaged switching regulator delivers 3.5A, replacing a Multiwatt packaged bipolar IC.



Recently SGS-THOMSON has introduced a "shrink" version of the original BCD process — called BCD-II — which greatly increases the circuit and current density that can be achieved (figure 3).

The original Multipower-BCD process family used 4 micron lithography.
In the BCD-II versions this is reduced to 2.5 microns.
Consequently the current density and component density are approximately doubled. In the case of the 60V version, the shrink increases signal component density from 650 transistors/mm^2 to 1500 tr/mm^2; at the same time the R_{ON}.Area is reduced from 0.9 ohms/mm^2 to 0.5 ohms/mm^2.

Figure 3: A shrink version of the Multipower-BCD technology has now been introduced. Called BCD-II, this version doubles the component density, making high complexity devices much less expensive.



STANDARD BCD PRODUCTS

The first BCD chips to be marketed were the L6202 and L6203 DMOS bridge driver ICs — actually the same die assembled in DIP (L6202) and Multiwatt (L6203) packages. Both of these devices have an ON resistance of 0.3 ohms, which gives a maximum continuous current of about 1.5A (DIP version) and 3A (Multiwatt version).

These were followed by a variety of power ICs for computer peripheral, industrial and automotive applications. Typical examples include switching regulator ICs, lamp drivers for automotive applications and motor drivers of various types.

All of the early chips and many introduced more recently are standard devices in the sense that they are normally used in various end products, like standard linears or standard logic. In the late eighties, however, designers began to apply BCD technology to make power ICs with a complexity that can truly be called LSI.

LSI COMPLEXITY IN POWER ICs

We have seen that BCD technology allows an arbitrary number of complete power stages on one chip and the dissipation of each is low enough to ensure that the cumulative dissipation of these power stages is within the limit of practical packages. Moreover, high density CMOS allows signal level circuits of LSI complexity to be added on the same chip.

An interesting consequence of these factors is that BCD technology allows the IC designer to build complex systems on a single chip. Moreover, the technological limit on complexity is beyond the complexity of a wide range of end products.

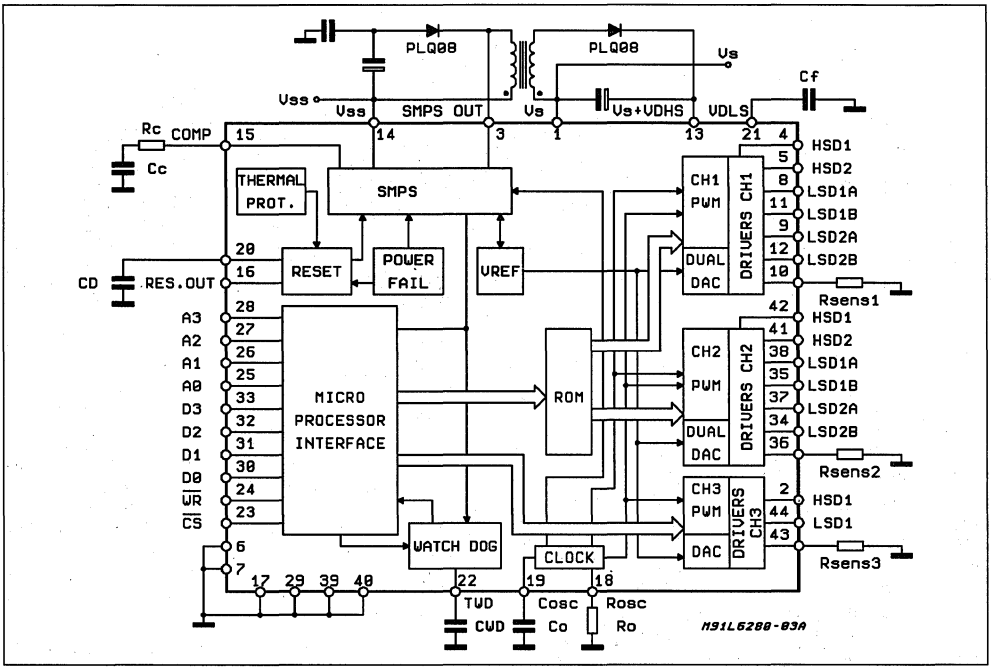
The first example of a circuit that exploits the possibilities of LSI smart power is the L6280, a device introduced in 1989 for a portable typewriter application (figure 4). This IC integrates two 1A motor drivers, a 3A solenoid driver, a 5V/1A SMPS and microprocessor interfacing circuitry — all of the power subsystems of the typewriter. The L6280 behaves like a microprocessor peripheral, latching commands from the bus. All of the functions can be controlled by software — even the output stage configurations.

Surprisingly, perhaps, the overall dissipation of this complex IC is so low — less than 1.5W — a power package was not needed. In fact the L6280 is assembled in a PLCC 44 chip carrier, though the 11 pins on one side are all connected together and used to conduct heat to the PCB tracks.

Since then the same approach has been applied to other applications of comparable or greater complexity. One example is a custom chip designed for a computer peripheral application (figure 1) that integrates a motor control circuit, a servo positioning system, a step up converter, a microprocessor interface and various other glue circuits needed on the board. There are 12 power transistors and roughly 4000 other transistors in this IC. Such a solution is extremely effective because of the increasing trend towards very compact solutions.

BCD technology can also be applied in areas where the emphasis is more on "smart" than on power. An example of this is the telephone set. Using Multipower-BCD technology it has been possible to realize a single-chip telephone that includes a pulse/tone dialler, voice circuit, ringer and monitor amplifier. Modest power capability is needed for the ringing transducer and the monitor loudspeaker, but half of the chip is occupied by the complex CMOS logic. A total of 16,000 transistors are integrated in this circuit.

Figure 4: Designed for a portable typewriter application, the L6280 integrates two motor drivers, a solenoid driver, a power supply and complex control logic.



The introduction of the shrunk BCD-II technology both increases the amount of logic that can be integrated at a reasonable cost. This improvement in microlithography also allows an improvement in current density of the power DMOS transistors — an interesting advantage over bipolar technology where current density depends on emitter area and cannot be improved in this way.

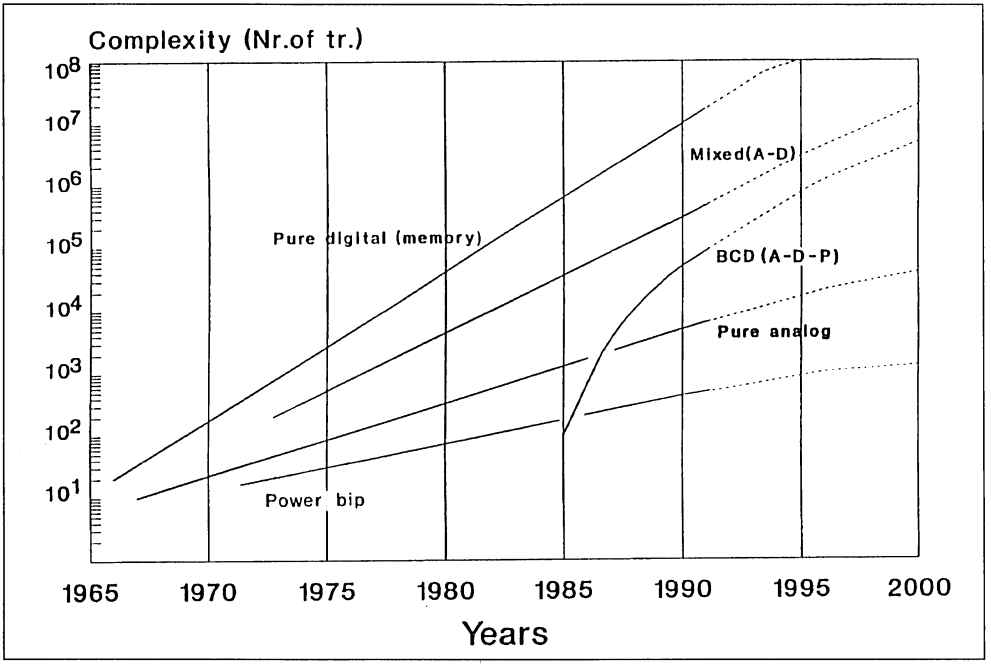
It is also interesting to compare the potential complexity increases for various technologies (figure 5). Clearly there has been a much greater increase in the complexity of pure digital circuits (about eight decades) than in analog circuits (four decades). In fact pure analog ICs containing thousands of components are extremely rare. A consequence of these curves is that there is a tendency to use digital techniques whenever possible because it allows a greater reduction in area. The possibility of having dense digital circuits on a BCD chip allows designers power IC designers to take advantage of this trend.

At present the capabilities of the technology in terms of complexity generally exceed the demands of system designers, few of which have learned to exploit fully the level of integration now possible. Another important consideration is that LSI smart power devices will invariably be full custom and developed for a specific end use with IC designers and system designers working together; at this level of complexity standard products are unlikely.

To create a complex smart power IC the system designer has to understand the capabilities and limits of IC technology and consider a highly-integrated solution from the outset. With today's level of certainty in power IC design this is not a risky choice.

Given the need to embody system knowhow in silicon it is evident that some system designers would prefer to do their own design, using a cell library approach. SGS-THOMSON uses such a design technique in house but we believe that it is too early to offer this on the market because the design of power ICs is not as mechanical as low power ICs and the silicon design experience of a skilled designer is very important. The main difficulty lies in avoiding unwanted interaction between power sections and signal sections — where a power IC designer really earns his salary. Another non-trivial complication is that there is a difference between designing a circuit which works and designing one that can be produced and tested in large volumes. Often, in fact, the development of testing hardware and software can be more troublesome than the design of the IC itself.

Figure 5: BCD technology allows power IC designers to take advantage of the much greater level of integration achieved in digital technology. Analog functions are replaced by digital equivalents in complex circuits.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

NEW LEVELS OF INTEGRATION IN AUTOMOTIVE ELECTRONICS

by Riccardo Ferrari , Marco Morelli

One of the fastest growth areas today in electronics is in the automotive field. In this note the authors describe the particular needs of this field and some typical dedicated ICs developed by SGS-THOMSON.

INTRODUCTION

Since the early seventies, more and more functions have been added to our cars not only with the purpose of guaranteeing a better comfort to drivers and passengers, but also to reduce operating costs and finally to ensure compliance with new regulations concerning noise and pollution are concerned. Because of all these needs, cars have to house more and more modules designed to perform more or less complex operations (Fig. 1).

This growth makes more and more evident the need to reduce the room taken by each module, with the double target of minimizing the cost of the particular function and increasing the number of functions in a specific car; in parallel, by increasing the number of modules, it becomes mandatory to increase the reliability of each of them, otherwise the reliability of the total car would be badly affected.

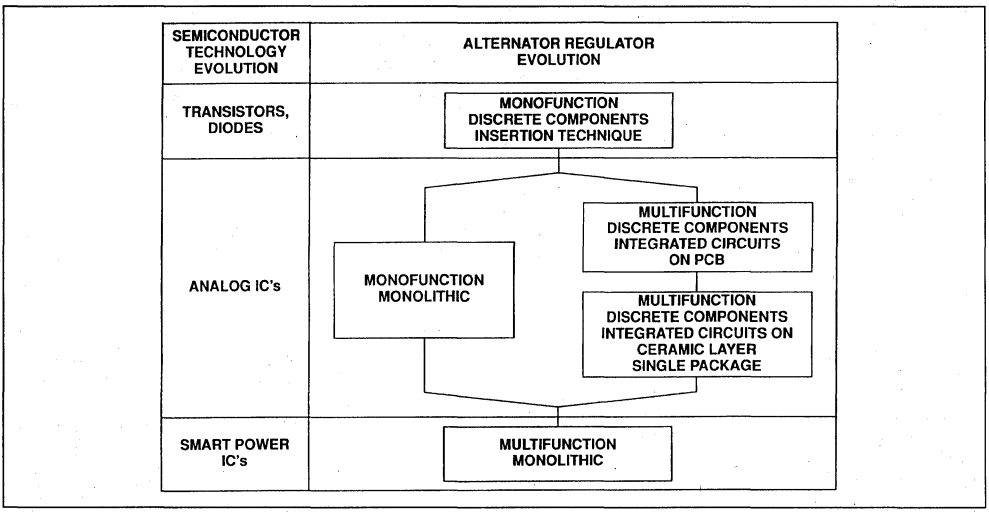
All these issues recently pushed the manufacturers of automotive systems to refer very often to producers of integrated circuits asking for the development of monolithic devices capable of replacing effectively a number of discrete components, passive parts included; anyway the trend to a total integration is not over by just designing onto a simple piece of silicon a complete function, but it carries on implementing in the same device a number of auxiliary services, that would add a substantial cost if achieved by discrete components, that can easily find place on a few extra square millimeters of silicon.

To that purpose the example given by the alternator regulator, subject of a specific description in the following pages, is particularly enlightening. Figure 2 shows briefly the evolution of the alternator regulator paralleled with the evolution of the silicon technology; it is evident that the key issue to pursue the monolithic design of very complex functions in the automotive environment is the availability of process capable to host on the same chip high density signal circuitry, together with power stages managing currents of several amperes; a process with these characteristics is usually called "smart power" process.

Figure 1: Electronics in present and future automobiles.

SAFETY & CONVENIENCE	BODY CONTROL	POWER TRAIN	DRIVER INFORMATION
Rear Window Defogger	Cruise Control	Ignition	Digital Gauges
Climate Control	Intermittent Wipar	Spark Timing	Digital Clock
Keyless Entry	Antitheft Devices	Voltage Regulator	Multitons Alarms
Automatic Door Lock	Electr. Suspension	Alternator	Engine Diagn. Results
Light Drimmer	Electr. Steering	Idle Speed control	Service Reminders
Traction Control	Multiplex Wiring	Turbo Control	Miles to Empty
Antiskid Braking	Module to Module	Emission System	Shift Indicator
Window Control	Communications	Transmiss. Control	Head-up Display
Memory Seat	Load Sensit. Braking	Diagnostics	CRT Display
Heasted Windshield	Hard/Soft Ride Control		Audio Annunciator
Voice Controlled Trunk			
Airbag Restraints			

Figure 2: Alternator regulator evolution.

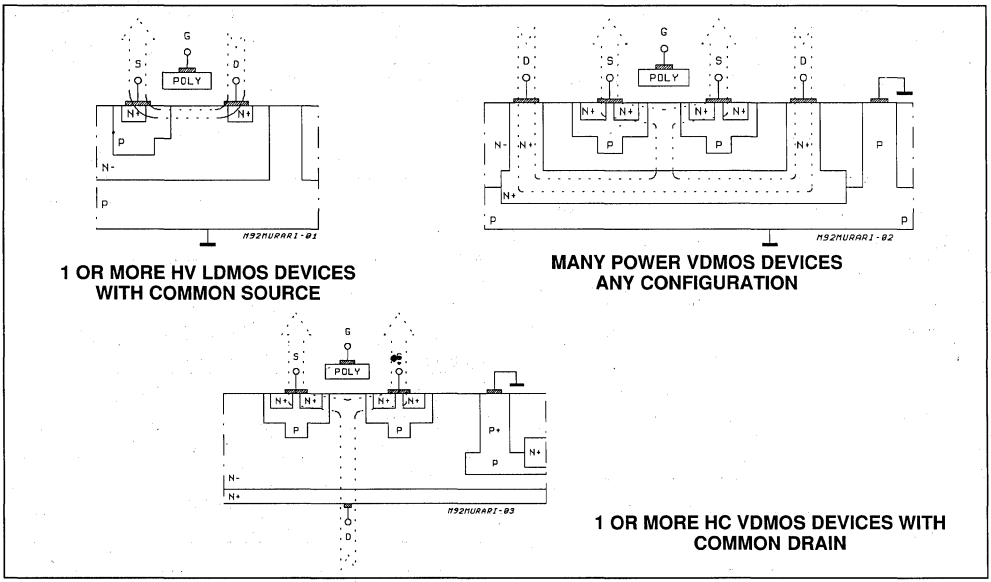


TECHNOLOGY OVERVIEW

Over the years SGS-THOMSON has developed various technologies that allow the realization of smart power circuits. The simplest way to classify these technologies is to refer to the process type, which can be purely bipolar or mixed, that is, including on a single piece of silicon both MOS structures (of control and power) and bipolar structures.

Another method (figure 3) is to examine the way in which the current flows through the power section; horizontal, with the current entering and leaving through the upper surface, or vertical, where the current enters through the upper surface and leaves through the lower surface; for this lower connection, instead of wire, the tie bar

Figure 3: Integrated DMOS structures.



MULTIPOWER BCD/60 vs. BCD60II

	BCD20/60	BCD60II
Junction isolation	down	up and down
Field oxide	Tapered oxide	Locos + field implant
VDMOS R on* Area (Ω*mm^2)	0.9	0.5
LDMOS R on* Area (Ω*mm^2)	0.6	0.25
CMOS tr. density (mm^{-2})	650	1500
CMOS thres. voltage (V)	1.3	1
min. NPN area (mil^2)	11	4
min. PNP area (mil^2)	15	5
Number of masks	12/14	13/15

of the package is used.

The choice of one technology rather than another depends on various elements. By simplifying as far as possible the criteria, we can say that vertical technologies can guarantee, for a given area, lower resistances but they have the limitation of being able to include just one power device per circuit (or more than one, but always with the collectors or drains short-circuited). Horizontal technologies instead make it possible to have power structures that are completely independent. It is therefore evident that a vertical technology will give excellent results in the design of a light switch, while a horizontal technology will be equally well suited to the design of a multiple actuator.

Finally we have to underline that the continuous evolution of the silicon technologies has already made available, for the design activity, second generation processes, offering to the user both higher component density in the signal section and higher current density in the power area, so that in some cases the limit to achieve very low values of resistance does not come from the silicon, but from the bonding wires. An example of comparison between a first generation smart power technology - today in full industrial production - and a second generation one - today available for new designs - is given in Table 1: the way is open to processes that will allow the design - on the same chip-actuators - of several amperes together with microcontroller of not negligible power.

It is important at this point to underline that a smart power circuit does not consist of just silicon technology, but relies heavily on package technology. In fact it is well known that a signal device is bonded using gold wires with a diameter of 25 microns; however, gold wires can be used effectively up to diameters of 50 microns, which allows

Figure 4: Mixed bonding technology.

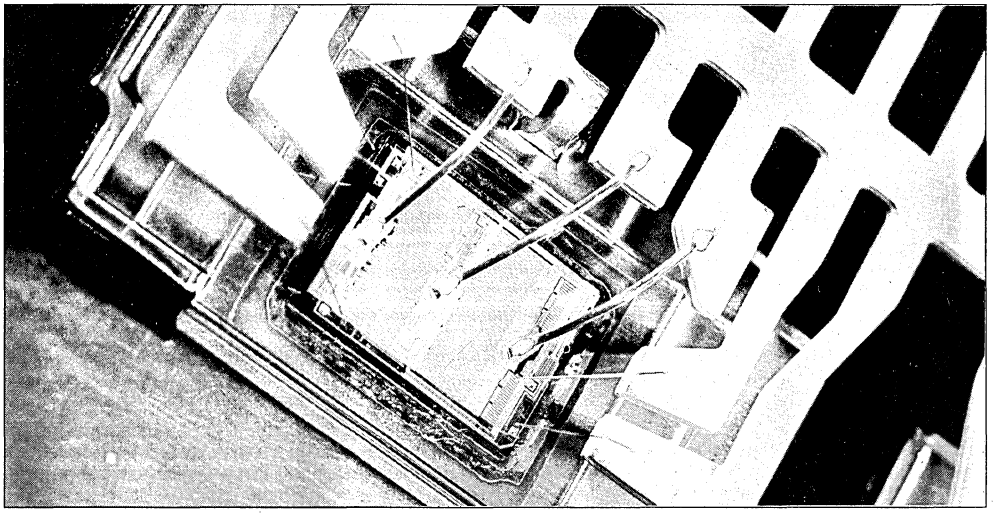
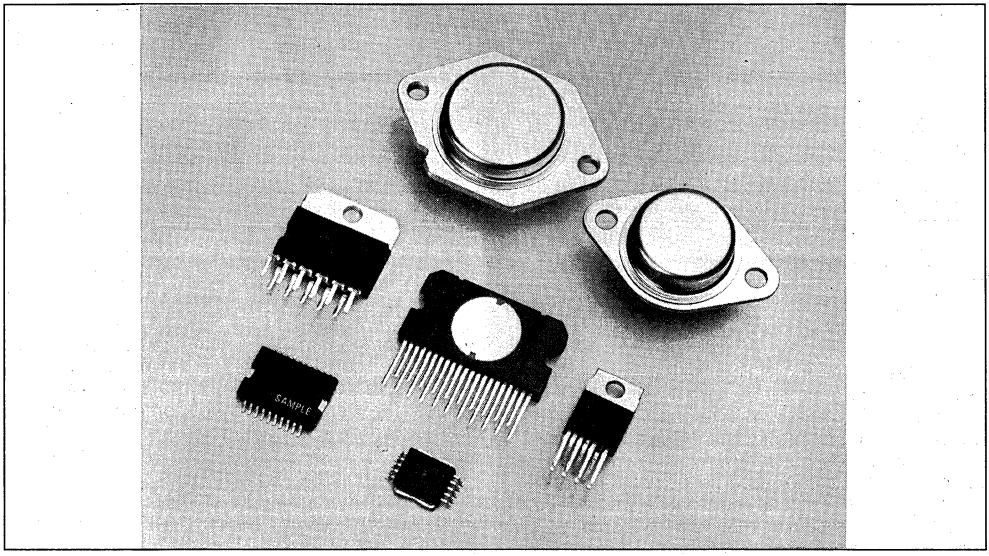


Figure 5: Power packages.



reliable operations with currents up to 2A, provided that the wire is surrounded by resin (the current capacity drops by 50% for wires in free air - that is, in the case of hermetic packages).

When, however, one has to deal with very high currents (more than 5A in single-point injection actuators, and more than 10A for window lift motors) gold wires are no longer suitable for obvious cost reasons so it is necessary to turn to aluminum wires with a diameter from 180 microns to 375 microns; clearly in this case it will be necessary to have adequately dimensioned bonding pads on the die, with a significant waste of silicon area.

Optimization is obtained with a mixed bonding technology where signal pads are bonded with thin gold wires and power pads with thick aluminum wires (figure 4). A further optimization is obtained by orienting the pads in the pad-to-bond-post direction.

Finally, another key area for a real industrial implementation of a smart power device is packaging; SGS-Thomson has a reputation of unparalleled excellence in the development and in the production of packaging techniques to meet power dissipation even in the presence of high pin count, and several innovative SGS-Thomson packages have been adopted as worldwide industry standards; in Figure 5 several types are displayed, including hermetic metal can, particularly suitable for components, such as the alternator regulators, that have to operate at a rather high temperature, with junction temperature that may exceed 150°C, in an extremely severe environment, since the regulator is usually exposed to any kind of dangerous element, such as grease, sand, dust, salt water and so on. A quite original power package for surface mounting, combining a low $R_{th\ j\text{-}case}$ (less than 3°C) with a small geometry, is under development in our laboratory.

THREE EXAMPLES

THE ALTERNATOR REGULATOR.

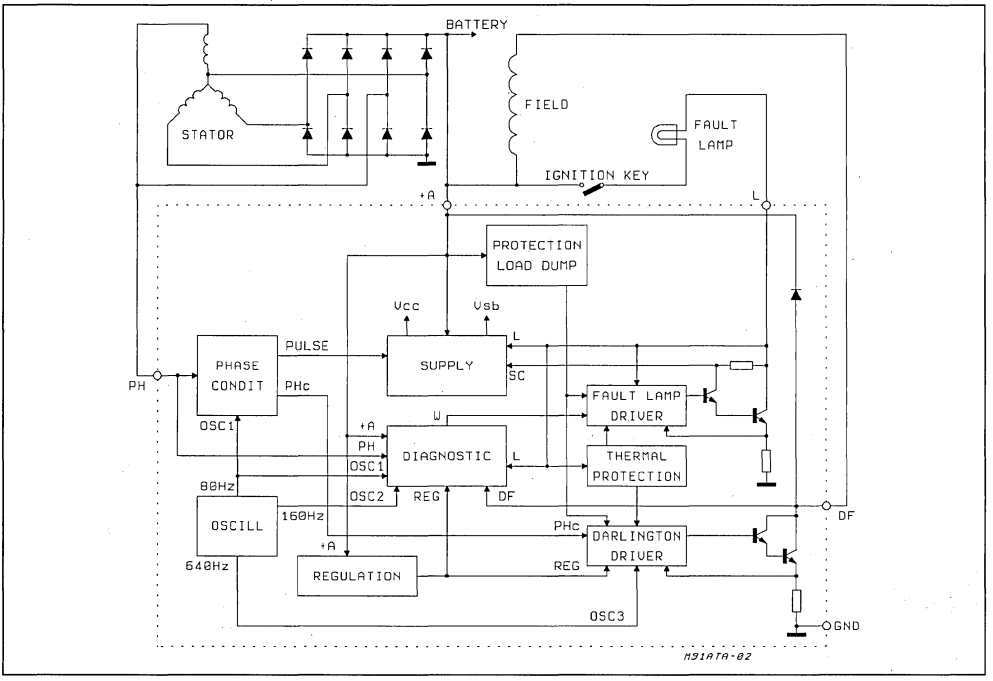
We have already briefly mentioned the evolution of the alternator regulator, but it is worth covering with some more details the history of this function.

Since the simple realization of so-called monofunction regulators by means of discrete components - diodes, transistors and resistors - the progress of the technology allowed the design of a monolithic component, still monofunction: in parallel, to provide the driver with more information about the status of the charging function, multifunction regulators were designed, but the power remained external, on a separate component.

A further improvement came with the assembly technology on a ceramic substrate, housed in a single package, but still several chips of silicon were needed.

Now SGS-Thomson has reached the maximum level of integration by designing a monolithic multifunction regulator and offering to the customer a device that minimizes the assembly operations and maximizes the reliability because of the single piece of silicon and the minimum number of connections between the silicon itself and

Figure 6: Block diagram of alternator regulator.



the rest of the system: nevertheless the accuracy of the regulation and the number of possible malfunctions monitored by the circuit are well above what offered so far by the market.

The main characteristics of the device are summarized in Table 2 and the block diagram of the circuit is displayed in Figure 6.

The choice of the technology required a particular care and was driven by the following factors:

1)A circuit for the regulation of the alternator voltage, even if equipped with a complex diagnostic, is however a circuit where the power section, including the field drive in low side configuration and the free wheeling diode plus a big active zener diode, takes a significant share - about one third of the total, (see Figure7); therefore a bipolar process has been selected.

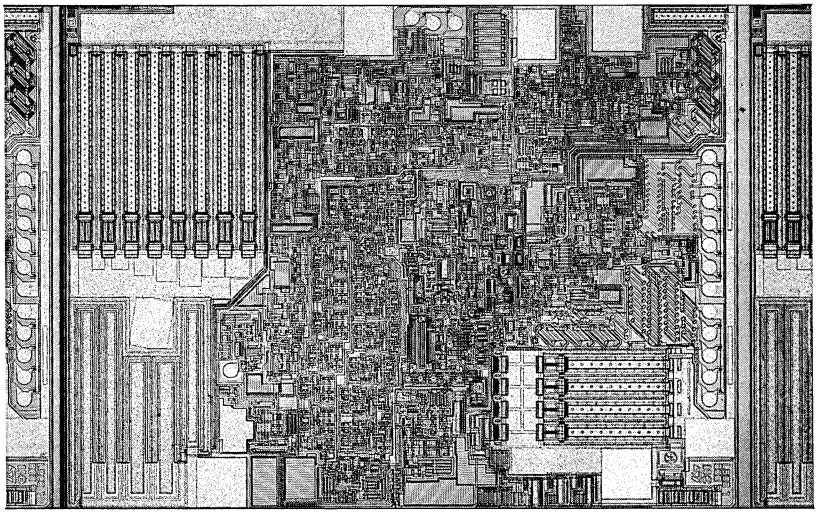
2)On the other side, about 600 small signal devices had to be integrated, and because of that a technology with a good intensity was mandatory, otherwise the total economy of the program would have been affected.

3)Finally an alternator regulator must be able to withstand very severe voltage transients, as fixed by ISO 7637/1, with voltages up to 270V and energy up to 50 joule, that arise on the car electrical network, for instance, if a sudden misconnection of the alternator occurs.

Table 2: MONOLITHIC ALTERNATOR REGULATOR

- Low side configuration
- No external component
- Accuracy on regulated voltage better than 1%
- Precise temperature coefficient
- Self-oscillating analog regulation loop
- Minimized field current at alternator stopped (500 mA max)
- Maximum field current trimmed at 5A, with 1.5V saturation voltage
- Full Diagnostic: alternator stopped
  Broken belt
  Extravoltage
  Broken wire alternator-battery
- Protected against short circuit (current limitation and thermal shutdown)
- Protected against short circuit of fault lamp driver
- Protected against extravoltages according to ISO 7637/1

Figure 7



Considering all of the above, SGS-Thomson has selected a high voltage process, internally named BSOII, fully bipolar, horizontal, with lithography of 3μm, and more than 100V of breakdown voltage in the VCBO condition.

The device is encapsulated in an hermetic package, TO-3 multileads, with bonding wires of 5 mils, able to carry continuous current up to 7 amperes (see again Figure 6).

THE PEAK & HOLD INJECTOR DRIVER

Let us now consider the U140, another component designed by SGS-Thomson to make available to the user a complex function on a simple chip; it is an actuator to drive in low side configuration the fuel injector in "single point" injection system.

As it is well known, quite essential for a good efficiency of the injection system is the capability to fix in the best way the time while the injector is opened, since that time is directly proportional to

Figure 8: Injector driver.

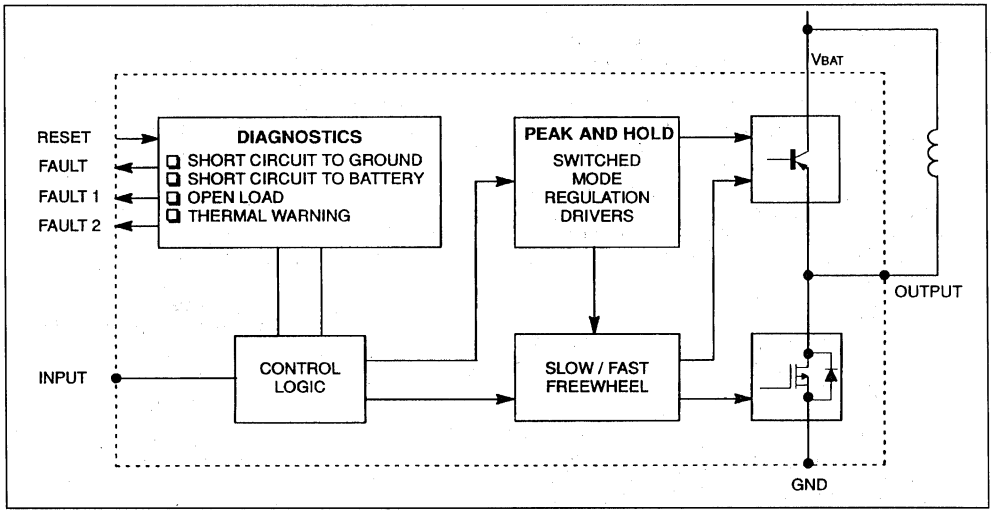
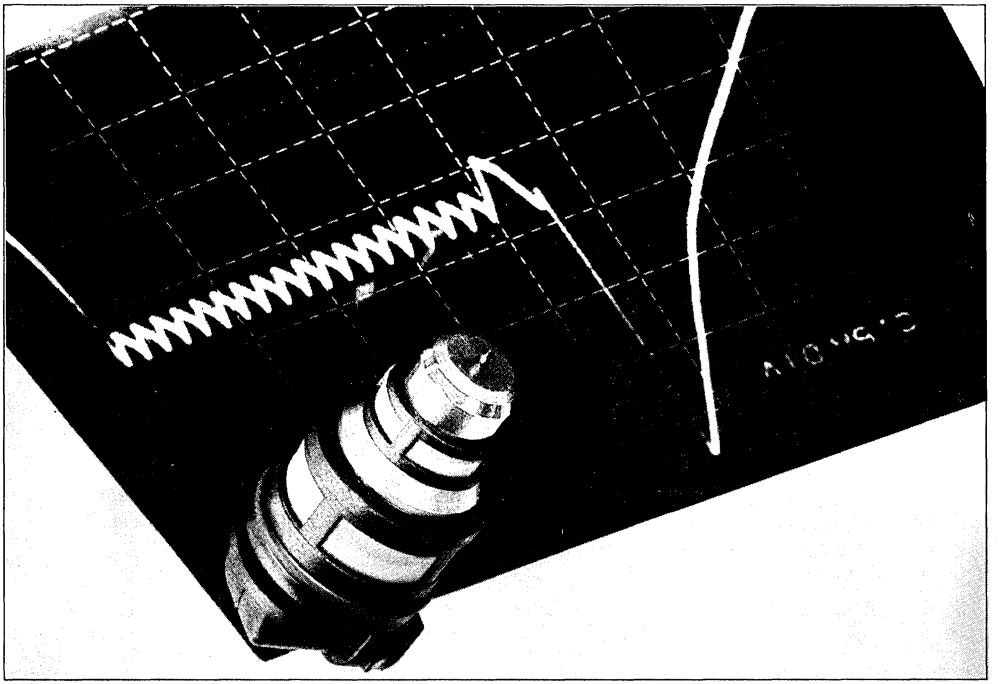


Figure 9



the quantity of fuel transferred to the intake manifold.

Particularly important to fix the fuel volume are the opening and the closing time of the nozzle, since both must be extremely fast; now, a single point injector needs a consistent current in the opening phase - up to 5A at the "PEAK" - but once opened, less current is enough to maintain the status - "HOLD" -. At the end of the cycle, finally the driving current must be switched off in a time as short as possible. The U140 meets all the above mentioned requirements: in addition, in the "HOLD" phase a further reduction of the current is achieved by switching on and off the driver stage (Figure 8), so reducing the power consumption and, as a consequence, the junction temperature.

A special mention shall be paid to the transition from "HOLD" to the "OFF" condition; as already said, it is quite important to reduce as much as possible this time; in the U140 that is achieved by discharging the inductor through an active zener set at a quite high voltage (about 70V), and that guarantees the closing of the injector in less than 50 sec. The same diode is set at 3V in the HOLD time. No external component is required by this circuit, that interfaces directly the microcontroller of the engine management system; by the way, the microntroller has just to fix the start and the end of the injection time, since the U140 is totally autonomous in fixing the current levels in the different phases, as well as the sampling of the holding current. (Figure 9).

The device incorporates a very sophisticated diagnostic (see again Figure 8), and transfers to the microcontroller all the relevant information on the status of the load.

The advantages of this monolithic devices are quite evident, if compared with existing solutions which need not less than 15 components including at least one IC and two discrete transistors, but are not limited to cost and room reduction, and to a consistent increase of the reliability: as a matter of fact the monolithic design allows to get, practically at zero cost, a very accurate value of the voltage of the recirculation diode, improving the accuracy on the ON time of the injector, and, last but not least, a diagnostic covering all the possible failure modes of the load.

The circuit is realized with SGS-Thomson's BCD technology, a mixed process including Bipolar, CMOS, and DMOS structures on the same chip; the input section is therefore able to interface directly a microcontroller, and the low side driver is designed with a DMOS having an R_{DSON} of less than 0.5 ohm. As already explained the recirculation diode is set at 70 volt in the transition from HOLD to OFF; because of that we selected the

Table 3: MONOLITHIC PEAK AND HOLD INJECTOR DRIVER

- Low side configuration
- Peak current function of battery voltage to provide a constant charging time
- Fast recirculation voltage independent from battery voltage
- Slow recirculation at max 3V
- Off time and peak current in hold condition internally fixed
- Full diagnostic: - open load
  - short circuit to ground and battery
  - thermal warning

BCD100, an option with a minimum breakdown Drain-Source voltage of 100V.

All the main features of this innovative device are listed in Table 3.

REARVIEW MIRROR DRIVING

While we are on the subject of higher levels of integration it is useful to mention the development of circuits for the multiplex wiring system, which replaces conventional cabling with a common bus and "intelligent" switches.

The intelligent switch circuits are key components for the multiplex system, and one of these is a multiple driver IC,the L9946, developed by SGS-THOMSON for rearview mirror driving applications.

This IC integrates all of the control functions and power circuits needed in the electronic external rear-view mirror unit now being adopted for high end cars and is the first chip to integrate these functions. (see Figure 10).

An important feature is that the IC is controlled directly by a microprocessor -- all of the possible drive conditions are controlled by loading 4-bit commands and the L9946 generates the appropriate motor control signals.

No external power circuits are needed because the L9946 drives directly the two motors used for mirror orientation (µp/down and left/right), the motor that "folds" the mirror for maneuvering and the demister heating element. In a typical application the chip is used in multiplex door wiring system where the door is connected to the body by three wires and all door functions controlled remotely using smart chips.

Inside the chip are four DMOS half bridge power stages which drive the three bidirectional DC motors, plus a DMOS high side driver that drives the demister element. Control logic integrated on the chip decides how these transistors are to be

Figure 10

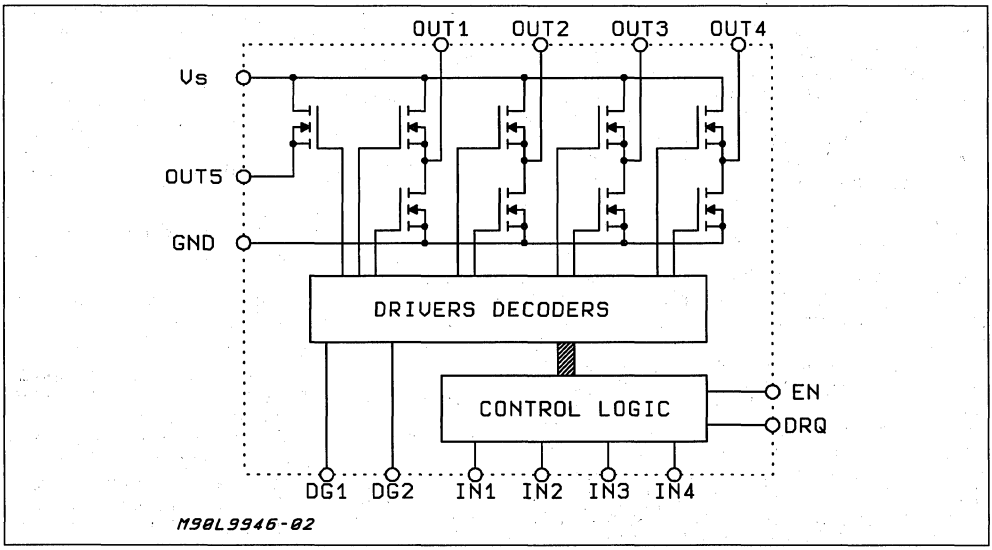


Table 4: MULTIPLE HALF-BRIDGE DRIVER

- 4.75A TOTAL OUTPUT CURRENT
- VERY LOW CONSUMPTION IN OFF STATE
- OVERLOAD DIAGNOSTIC
- OPEN LOAD DIAGNOSTIC
- GROUNDED CASE

switched to achieve the desired motion -- including rapid braking. Two of the half bridges are rated at 1A output current; the other two half bridges and the high side driver are capable of delivering up to 4.75A.

In common with many other dedicated automotive ICs the L9946 incorporates diagnostic functions. Conditions such as overload and open load are signalled to the control micro so that appropriate action can be taken. In addition there is a standby pin that allows the micro to put the L9946 into a dormant state when it is not needed.

CONCLUSIONS

We think we have demonstrated that the industrial availability of processes capable to match, on the same silicon, high power and complex control functions is the key element to the integration of completed functions on a single chip of silicon. The examples described demonstrate that SGS-Thomson has developed a technology portfolio that can offer different answers for different applications, always optimizing the trade-off among the various needs.

On the other side, all the above considerations would have a merely academic interest if they were not associated with a convenient cost. It is clear that the monolithic integration of complex functions implies the use of not negligible areas of silicon, and that even in presence of high density processes.

It is therefore important to devote adequate resources to the diffusion technique, to increase the yield of each process.

Today's chips, up to 30mm^2 (and all the thee examples are below that limit) can be produced at prices competitive with an equivalent discrete solution, and in the second half of the 90's the target will be expanded up to areas of 40mm^2, giving a green light to the monolithic design of complete modules.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SMART POWER TECHNOLOGIES FOR POWERTRAIN & BODY ELECTRONICS

by R. Ferrari

Smart power ICs are becoming increasing by common in automotive powertrain and body electronics. This note provides a general introduction to the subject.

As is well known, electronics is slowly but progressively invading every part of the automotive environment (figure 1); entering first in the car radio, it has extended progressively and is now present in all of the subsystems of an automobile. For those people who prefer a "historical" approach, the evolution of auto electronics has been divided into three main sections, each subdivided into various phases, correlated with the state of the art in general electronics at that time. Today, at the beginning of the 90's we are in the SMART POWER phase, and it is precisely that which we intend to discuss briefly here (see fig. 2).

We will look at, first of all, some definitions: smart power or intelligent power indicates those families of integrated circuits which include both logic control circuits and components capable of delivering a significant amount of power to a generic load. In numbers, a circuit can be considered smart power if it is able to deliver more than 0.5A to the load, or of withstanding more than 50V, or able to supply a power of at least 1W to the load.

Over the years SGS-THOMSON has developed various technologies that allow the realization of smart power circuits (figure 3). The simplest way to classify these technologies is to refer to the process type, which can be purely bipolar or mixed, that is, including on a single piece of silicon both MOS structures (of control and power) and bipolar structures. Another method (figure 4) is to examine the way in which the current flows through the power section; horizontal, with the current entering and leaving through the upper surface, or vertical, where the current enters through the upper surface and leaves through the lower surface; for this lower connection instead of wire the tie bar of the package is used.

The choice of one technology rather than another depends on various elements (figure 5) but simplifying as far as possible the criteria, we can say that vertical technologies can guarantee, for a given area, lower resistances but they have the limitation of being able to include just one power device per circuit (or more than one, but always with the collectors or drains short-circuited); while

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Memory Seat	Load Sensit. Braking	Diagnostics	CRT Display
Heasted Windshield	Hard/Soft Ride Control		Audio Annunciator
Voice Controlled Trunk			
Airbag Restraints			

Figure 2.

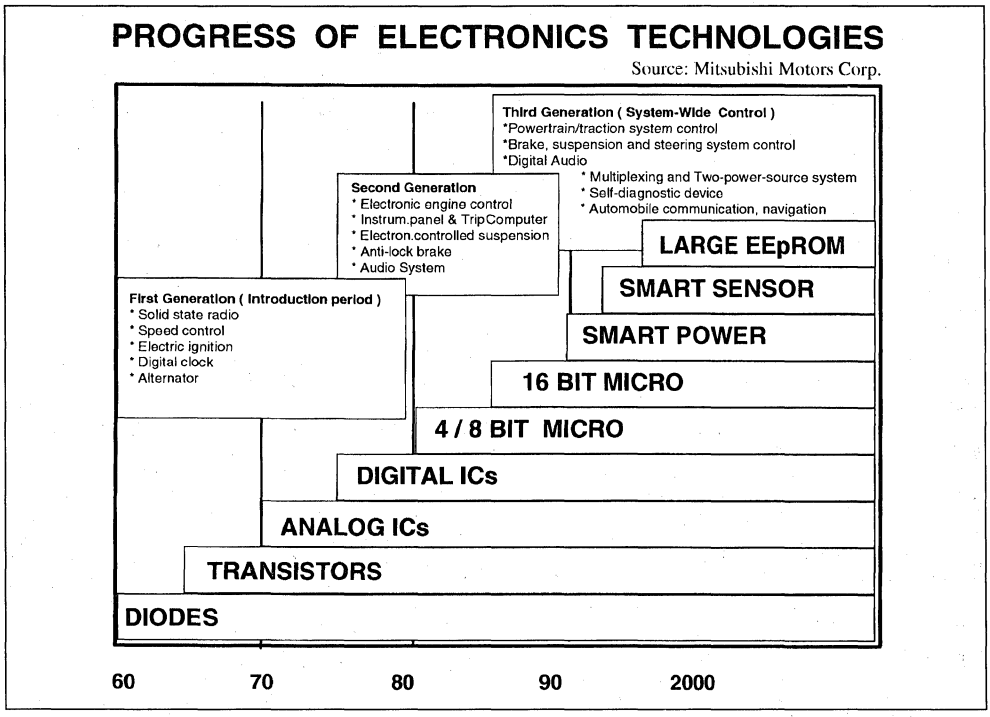


Figure 3: Smart Power Technologies Matrix.

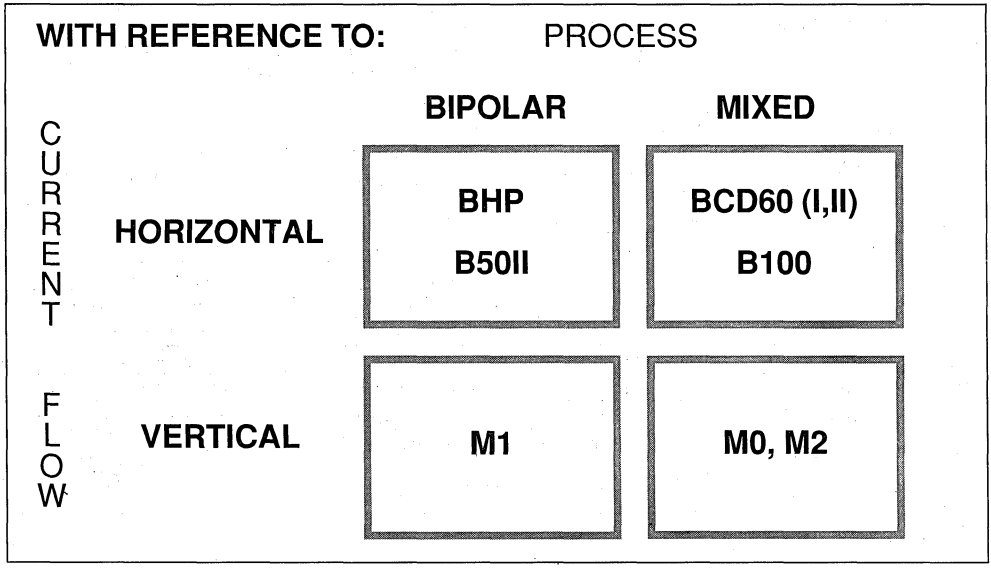
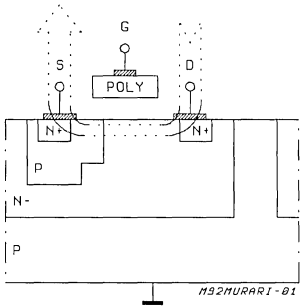
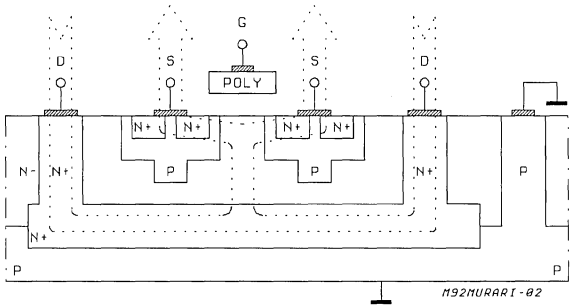


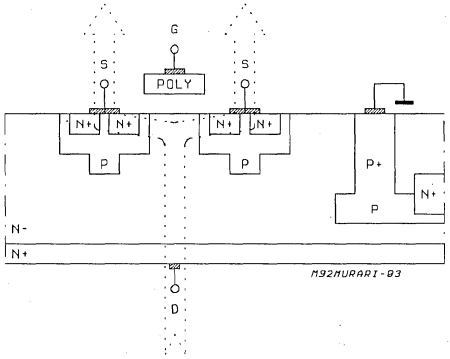
Figure 4: Integrated DMOS structures.



1OR MORE HV LDMOS DEVICES WITH COMMON SOURCE



MANY POWER VDMOS DEVICES ANY CONFIGURATION



1 OR MORE HC VDMOS DEVICES WITH COMMON DRAIN

Figure 5: Smart Power Technology Matrix selection criteria.

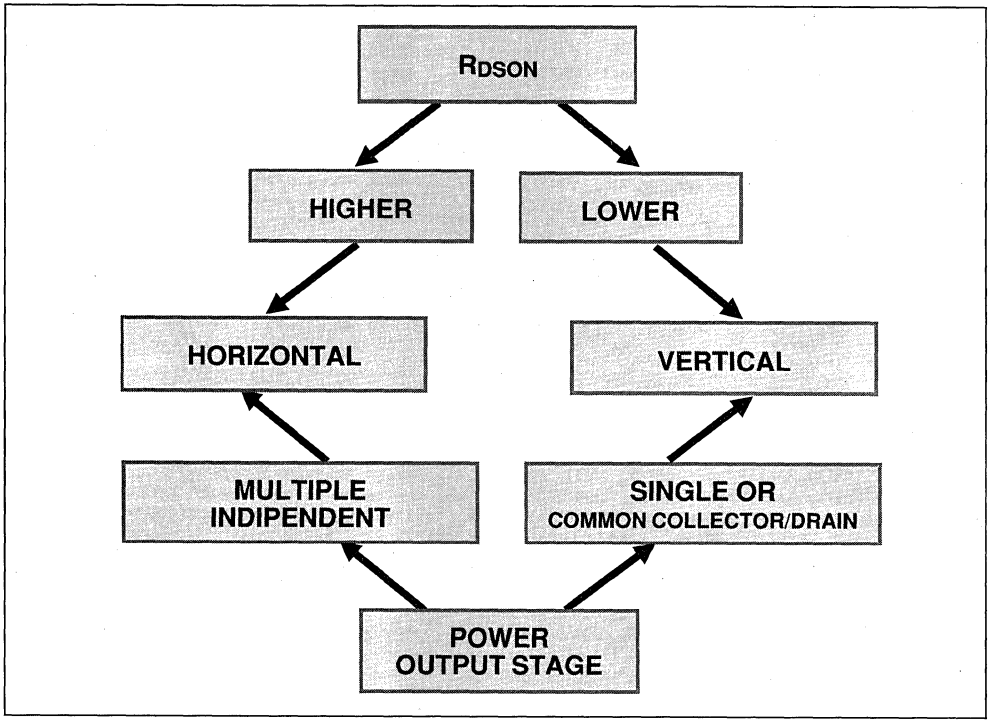


Figure 6.

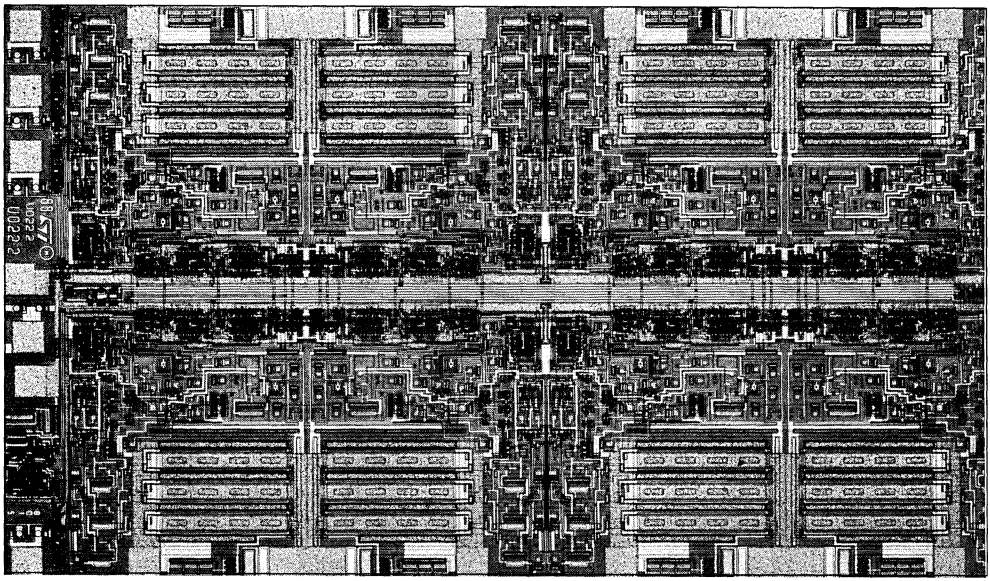


Figure 7: Bonding wire features.

WIRE	DIAMETER (micron)	RESISTANCE (mOhm/mm)	D.C. CAPABILITY (Ampere) in plastic package
GOLD	25	45	1.25
GOLD	51	11	2.50
ALUMINIUM	178	1	15
ALUMINIUM	254	0.5	28
ALUMINIUM	381	0.2	43

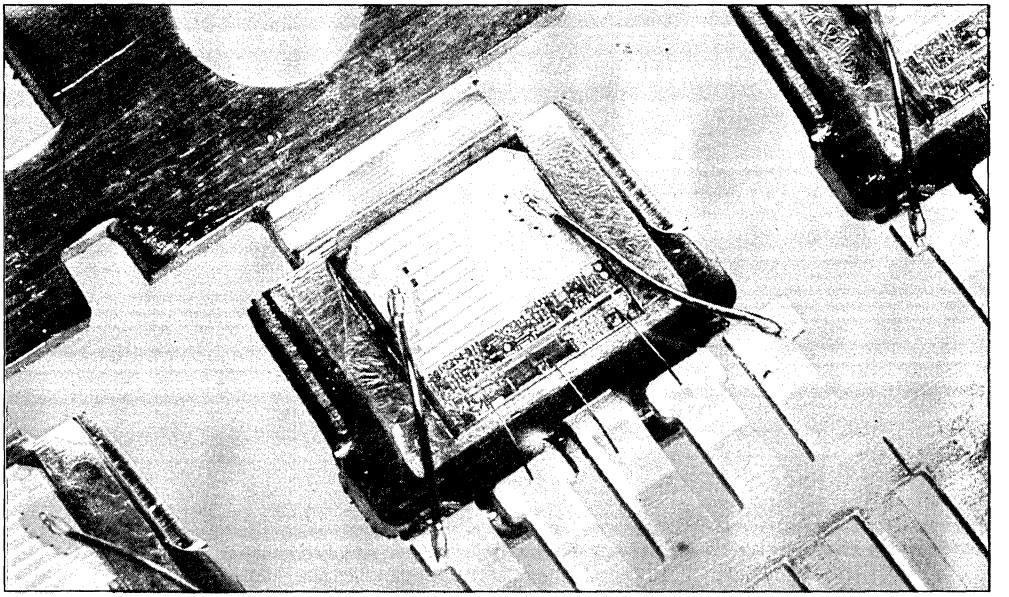
horizontal technologies make it possible to have power structures that are completely independent (figure 6). It is therefore evident that a vertical technology will give excellent results in the design of a light switch, while a horizontal technology will be equally well suited to the design of a multiple actuator.

It is important at this point to underline that a smart power circuit does not consist of just silicon technology, but relies heavily on package technology. In fact it is well known that a signal device is bonded using gold wires with a diameter of 25 microns; however, gold wire can be used effectively up to diameters of 50 microns, which allows reliable operation with currents up to 2A, provided that the wire is surrounded by resin (the current capacity drops by 50% for wires in free air — that is, in the case of hermetic packages,

When, however, one has to deal with very high currents (more than 5A in single-point injection actuators, and more than 10A for windowlift motors) gold wires are no longer usable for obvious cost reasons so it is necessary to turn to aluminum wires (figure 7) with a diameter from 180 microns to 375 microns; clearly in this case it will be necessary to have adequately dimensioned bonding pads on the die, with a significant waste of silicon area.

Optimization is obtained with a mixed bonding technology where signal pads are bonded with thin gold wires and power pads with thick aluminum wires (figure 8). A further optimization is obtained by orienting the pads in the pad-to-bond-post direction. But while we are speaking of power it is also important to speak of packages (figure 9). These packages are part of a long tradition of TO-220 type packages (with 3, 5 and 7 pins) but recently new needs in assembly are bringing important evolutions of the classic tab

Figure 8.



packages. Devices completely encapsulated in completely isolated packages — called Isowatt — are already in production; in these devices isolation up to 1000V is obtained with a minimum reduction in the junction-to-case thermal resistance.

On the other hand, the practice of using clips, rather than screws, for mounting packages is becoming always more common, both to save space and to obtain better long-term reliability in thermal conduction. This has led to the TABLESS isolated package which accumulates the previous two needs, while for surface mounting a non-isolated package with a junction-case thermal resistance less than 3'C/W is in development in our laboratories and will be available in industrial quantities in 1991.

Now that we have examined the means that technology places at our disposition, both in diffusion and in assembly, we can now examine what typical structures smart power processes will allow us to make, and which kind of circuit will normally be driven by each structure (figure 10).

Figure 9: Power package Matrix.

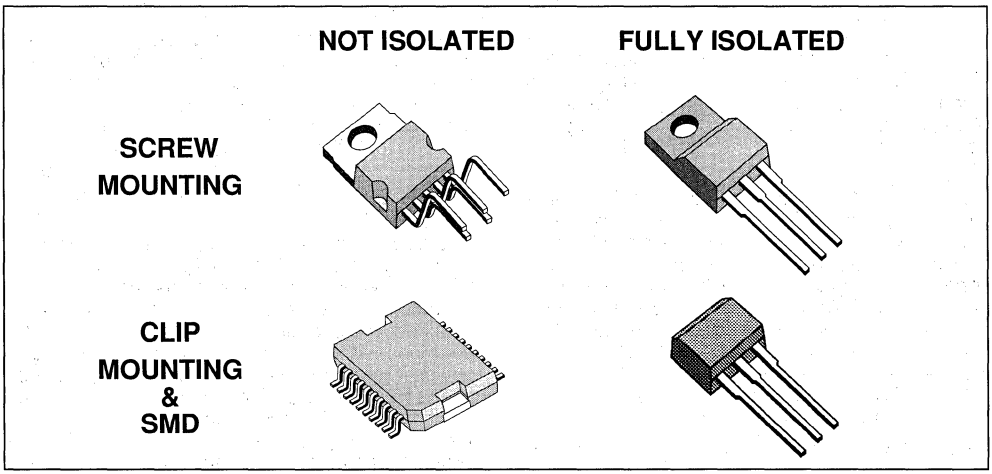


Figure 10: Intelligent power actuators basic configuration.

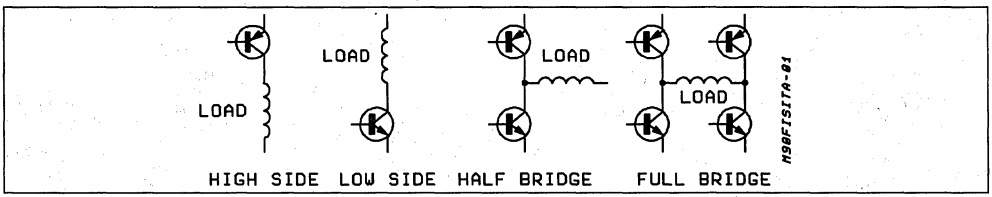
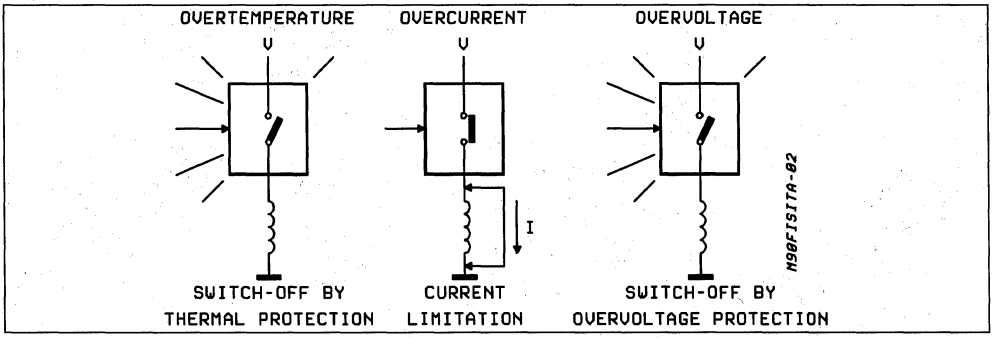


Figure 11: Intelligent power actuators basic protection.



1. The typical, so-called High Side configuration, in which the actuator is located between the supply and the load, is traditionally used in the supply of resistive loads, typically lamps, but is also suitable for mono-directional motors.

2. When the actuator is between the load and the ground of the supply system we have a "low side" configuration, very common for driving inductive loads such as, for example, the solenoids that control the opening of valves (injectors, ABS system, automatic transmission), but also ignition coils.

3. Finally, when we have to drive a motor that rotates in both directions it will be necessary to use a bridge structure; the choice between integrating the whole bridge or just half of it clearly depends on the current involved. Today's technology allows us to realize efficiently a complete bridge to drive a door lock motor, while it is necessary to use two half bridges if the load is a windowlift.

In all of these structures there will always be integrated a certain number of protection circuits, to guarantee survival of the device in the presence of possible failures in the surrounding ambient (figure 11).

These include, to name a few, the automatic shutdown when the silicon reaches a critical temperature (which can be caused not only by a short circuit in the load or its connections, but also by the degradation of thermal contact between the device and its heatsink). Today, in certain applications such as fuel injection this automatic shutdown tends to be replaced with a warning signal, which informs the control unit when a critical situation has been reached, leaving the unit itself to decide what to do (for example, reduce performance to guarantee functionality).

Another very common structure is output current limiting, even in the case of a load short circuit. Usually the intervention of the limitation circuit is accompanied by a diagnostic signal that is made available for the control system. Finally, in some devices a circuit is included that is able to detect overvoltages in the supply system, disabling the output stage and placing it in the best conditions to support the overvoltage.

Given the above, we will now describe a practical case with the aim of identifying how the design time can be optimized through a suitable interaction between the system designer and the silicon manufacturer.

The circuit shown in figure 12 is a dual low-side actuator designed to drive two independent loads with currents up to 3A each (typically injectors). The technology employed is mixed (bipo-

Figure 12.

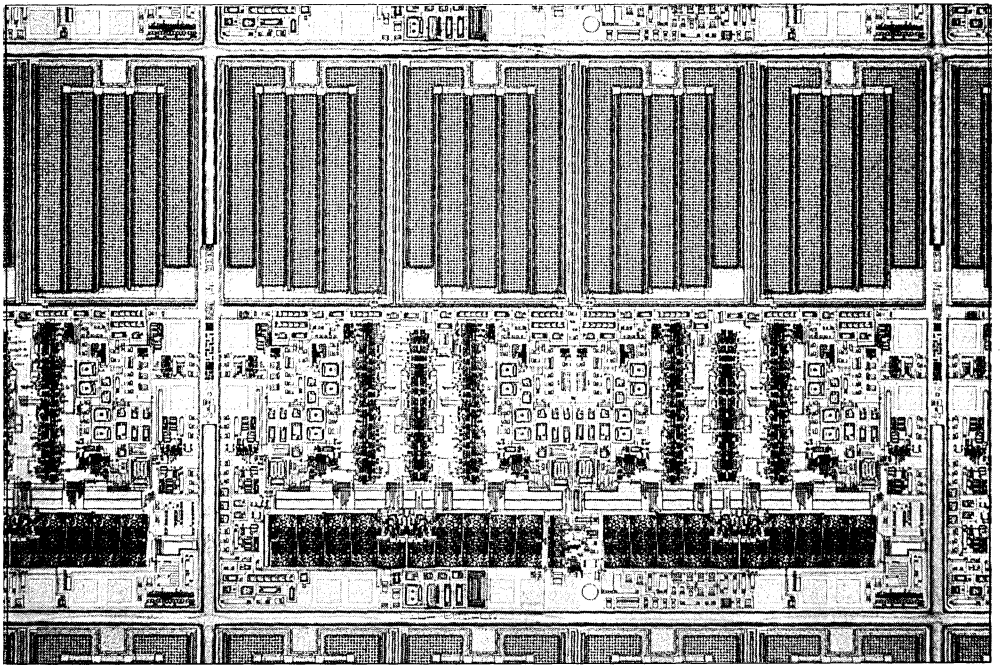
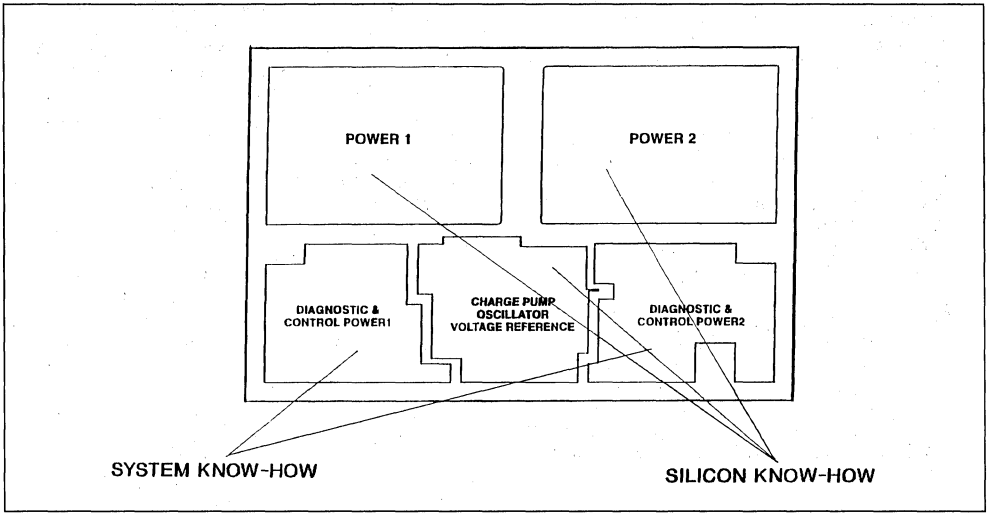


Figure 13: Expertise partitioning when designing a smart power actuator.



lar/CMOS/DMOS) with a horizontal current flow (BCD60); if we pass from the photograph to a topographical diagram of the silicon (figure 13) it becomes immediately evident that the chip is divided into a limited number of macroblocks, for each of which it is easy to attribute project leadership. In fact it will be an essential task of the system designers to define the criteria for the driving of the actuator as it is to define the malfunctions for which the activation of a diagnostic signal is necessary. On the other hand it is indisputable that only the silicon designer can optimize the design of the power section and take advantage of structures already available in his library to realize those functions which are necessary and also repeated frequently in different devices.

The system designer, too, can take considerable advantage from the use of cell libraries so the total design time can be reduced to a minimum (7-9 months from the start of the design to working silicon), reducing significantly the gap traditionally existing between a dedicated circuit (full custom) and a semicustom circuit obtained from gate arrays or standard cells.

A brief glance at another two circuits, each representative of a technology described above.

In the first we see a highly-innovative circuit for use in ignition systems. This is the VB020 (figure 14), a circuit realized in mixed vertical technology (M2) able to drive directly the primary of the ignition coil, combining a darlington with a vertical current flow with a driver circuit and TTL/CMOS compatible control circuit (figure 15). In the device are integrated circuits to limit the collector voltage (fixed at 450V max).

We conclude this series of examples with the L9937 (figure 15), a bridge circuit designed to drive a door lock motor and therefore capable of delivering continuous currents of 6A with starting peaks up to 12A. The device is realized in horizontal bipolar technology and, as appears in the photograph, is almost entirely occupied by four large power transistors that constitute the output stages of the circuit. In this case, too, you can see the mixed bonding (gold for the signal wires, aluminum for power wires) and the pads oriented to optimize silicon area. In the block diagram (figure 16) you can see a chain of diodes which has the function of monitoring the temperature of the chip.

This brief introduction to smart power technologies would not be complete if it did not dedicate a few words to the price that the customer must pay to buy circuits of this type. In fact a typical question that semiconductor companies frequently hear is "How much does a square millimeter of smart power silicon cost?". Since the price of a square millimeter of silicon depends on the total area of the chip I believe that it can be a pleasant surprise to discover that even for fairly sizable chips — that is, up to 25/6mm2 — the price of each mm2 increases very little (about 25%). The curve of figure 17 gives the trend for areas between 5 and 50mm2 and, though based on a theoretical calculation, follows closely the present commercial reality. Obviously the graph reflects the current state of the art; if only three years ago the elbow of the of the curve had been moved violently to the left without arriving at saying that the evolution will continue indefinitely with the same speed, it is however reasonable to expect in the next few years a further extension of the linear zone at least towards the 40mm2 region. As for the meaning of "1mm2 of silicon", several

Figure 14: Fully integrated high voltage darlington for electronic ignition.

- PRIMARY COIL VOLTAGE UP TO 450V
- COIL CURRENT LIMIT INTERNALLY SET TTL/CMOS COMPATIBLE INPUT
- BUILT-IN COLLECTOR-EMITTER VOLTAGE CLAMPING
- OVERVOLTAGE PROTECTION OF THE DRIVING CIRCUIT
- FULLY INSULATED FIVE LEAD POWER PACKAGE

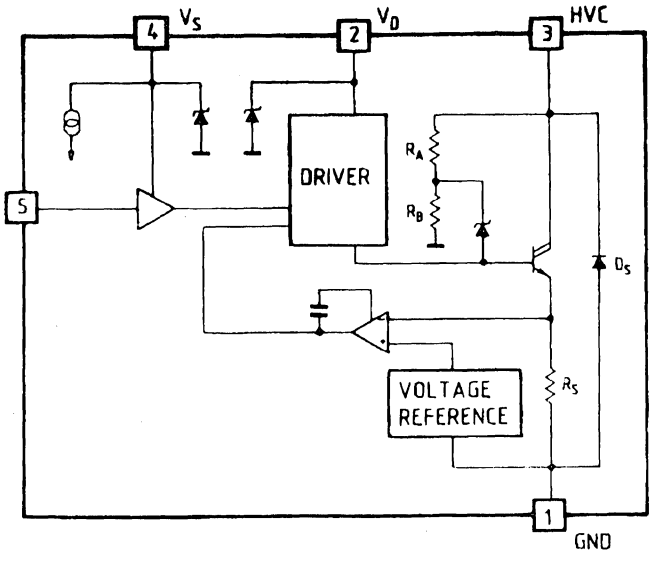


Figure 15.

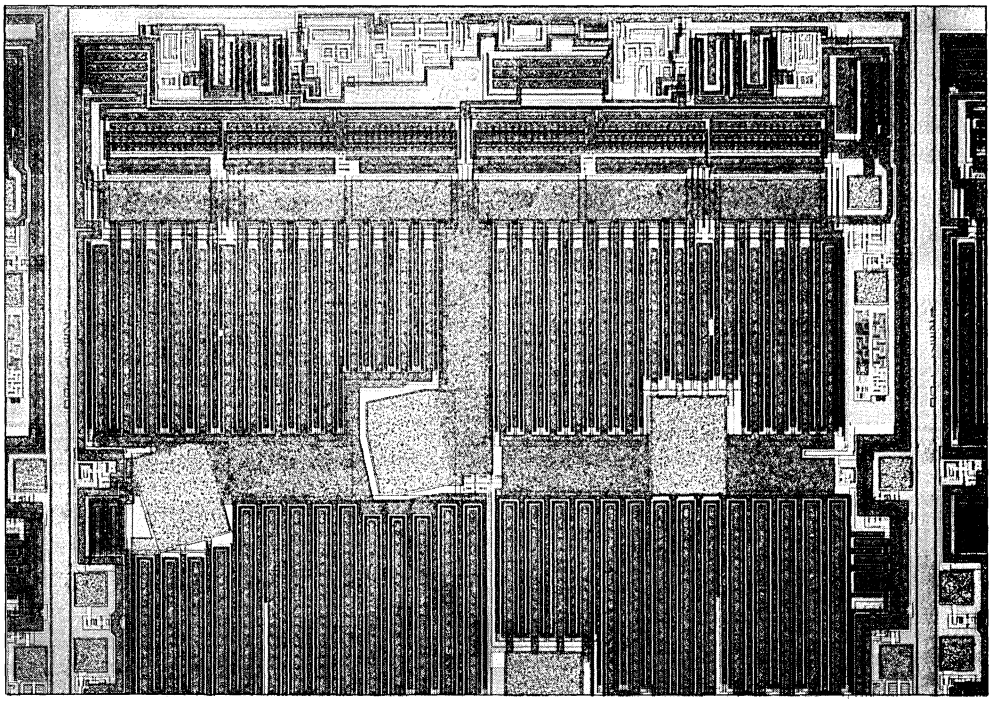


Figure 16: Full bridge motor driver.

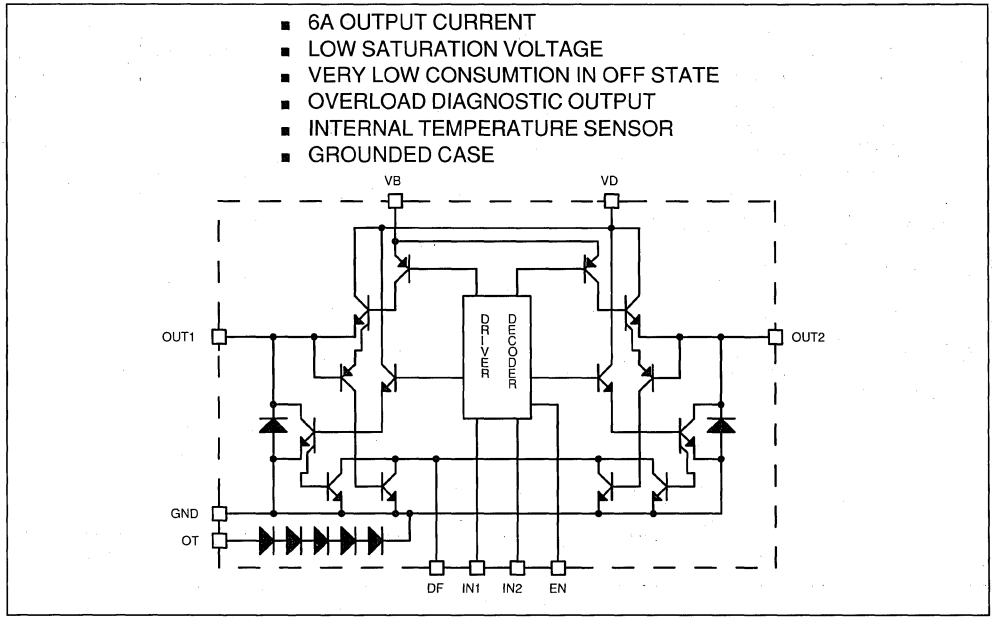


Figure 17: Smart power silicon.

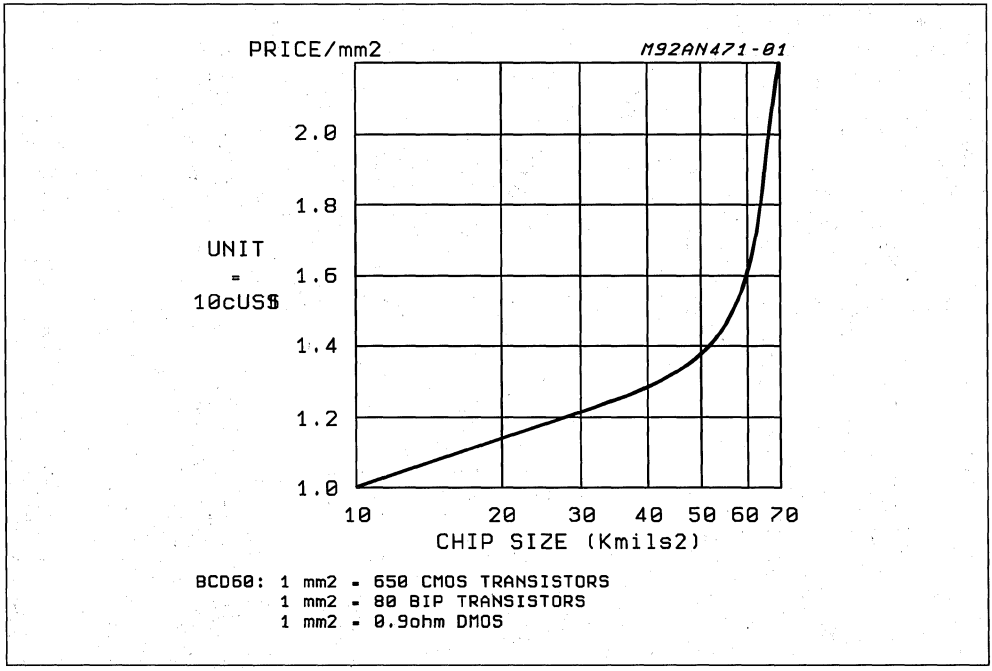
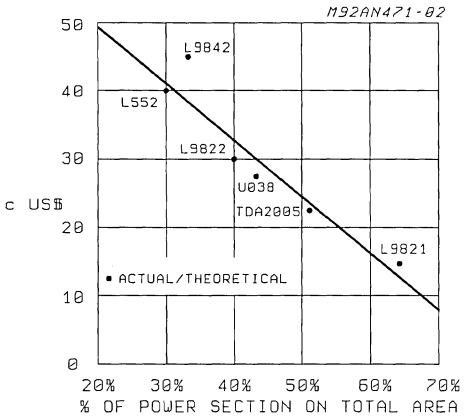


Figure 18: Smart power devices.



possibilities are given at the foot of the table.

There is another way to evaluate the price of a smart power circuit, and this is to estimate the price for each ampere delivered to the load. This method of calculation is less rigorous and can be plotted as a graph assuming as size reference the percentage of silicon dedicated to power compared to the total area of the chip. The line shown in the figure 18 graph indicates that one ampere costs approximately 30 cents but can rise to 45 cents for circuits containing particularly complex control and diagnostic logic, and it can fall to 15 cents for devices consisting essentially of only power stages. It must be underlined that two consumer devices (L552 and TDA2005 — both audio power amplifiers) for which we can assume stable specifications, mature technologies and ample markets, lie exactly on the curve. This should be indicative of the final trend for automotive devices which are as yet young devices in a young market.

HIGH CURRENT MOTOR DRIVER ICs BRING AUTOMOTIVE MULTIPLEX CLOSER

by Riccardo Ferrari & Sandro Storti

Smart power ICs delivering up to 25A complete the family of power components needed in automotive multiplex systems, making it possible to drive even a windowlift motor directly. With these ICs the large-scale adoption of partial multiplex schemes moves much closer.

One of the essential prerequisites for the large-scale introduction of multiplex wiring systems for vehicles is the availability of high power ICs capable of driving lamps, motors, solenoids and relays. These ICs must be able to survive in an exceptionally hostile environment, they must be highly reliable and — since so many are needed in each vehicle — they must be inexpensive.

Many power ICs suitable for this emerging market have already been introduced, but a gap was left at the high current end of the range, where ICs delivering 20A or more are needed to drive loads like windowlift motors.

Today SGS-THOMSON has filled this gap with new power ICs that exploit technologies that make it possible to build very high current ICs that are both reliable and economical. Two such ICs are the L9936 half-bridge motor driver and the L9937 full bridge motor driver.

The L9936 (figure 1a) contains a half-bridge circuit capable of delivering 20A dc current, which is sufficient to drive directly a windowlift motor. Since the motor is bidirectional two of these devices are used to make a complete drive stage. Designed for lighter loads, the L9937 (figure 1b) contains a full bridge delivering up to 6A continuous (12A peak for starting). A single L9937 device drives a bidirectional dc motor.

Figure 1a: Capable of delivering 25A, the L9936 half bridge driver is a smart power IC suitable for driving windowlift motors in automotive multiplex wiring systems.

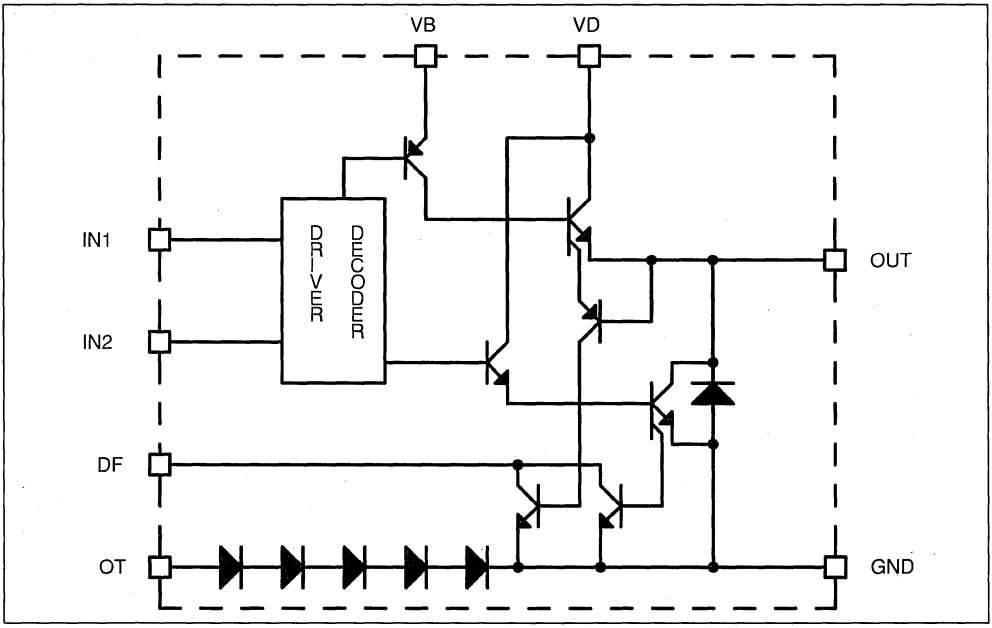
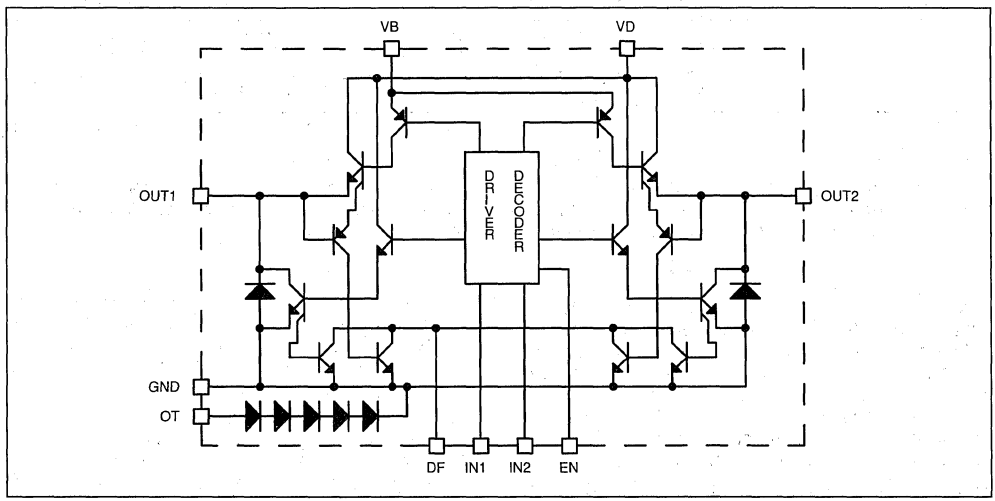


Figure 1b: A full bridge driver, the L9937 delivers 6A (10A peak) and is used in motor driving applications such as doorlock driving.



Both of these ICs are fabricated using an enhanced bipolar power process and a new mixed bonding technology. Bipolar technology has been adopted for these circuits — rather than the "BCD" mixed bipolar/CMOS/DMOS technology used for other multiplex switches — for several reasons. First of all, when very high currents are involved the resistance of the silicon is no longer dominant — half of the series resistance is caused by the metallization tracks on the surface of the chip and the bonding wires. Consequently there is nothing to be gained by using DMOS technology to further reduce the output transistor resistance. Figure 2 shows the contributions to the saturation resistance of a power NPN transistor in the BHP20 process used for these ICs. The use of thick metal (6 microns) significantly reduces voltage drop with high load currents in this technology.

Another reason for using bipolar technology is that the substrate currents generated in the substrate when 20A load current recirculates would affect low-level CMOS logic. In the L9936 and L9937 high-level bipolar logic is used in the control stages to avoid this danger, giving excellent noise immunity. Interfacing to this high-level logic

AUTOMOTIVE MULTIPLEX WIRING SYSTEMS

Multiplex wiring is the system where a conventional wiring harness is replaced partly or completely by a single, common bus which carries power and control signals throughout the vehicle. Each load is equipped with an electronic switch that recognizes commands on the control bus and returns status information.

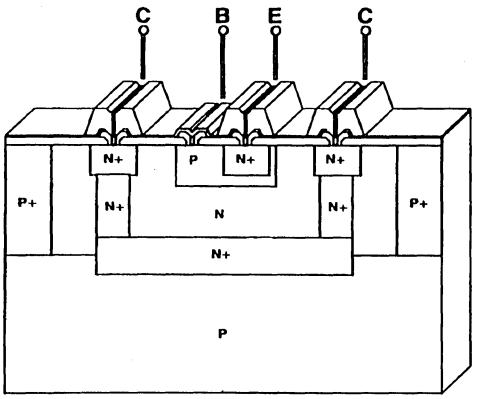
There are many different standards for the multiplex bus, of which the simplest is a three-wire scheme having one wire for the battery, one for control data and a common ground. Extra wires are sometimes added for more reliable transmission.

In a typical operation sequence, such as turning on a lamp, the control switch will cause a suitable command to be transmitted on the bus. The smart switch controlling the lamp will recognize the command and attempt to turn on the lamp. A signal indicating successful or unsuccessful completion is then returned on the bus.

Advantages of multiplex wiring are weight reduction, easier assembly, greater reliability and simpler fault diagnosis & repair. The simplicity of multiplex wiring is particularly important in critical points such as the connection between the driver's door and the rest of the body; in one case 27 wires were reduced to just three by the adoption of a multiplex subsystem.

Crucial to the success of multiplex wiring is the availability of electronic switches that can guarantee the necessary reliability and performance. Multiplex wiring is already used in small scale trials and will be adopted on volume produced vehicles in 1991.

Figure 2: In very high current ICs the voltage drop of the metallization and the bonding wires becomes significant. This example, a power transistor realized with the BHP20 process (used for the L9936 and L9937) indicates typical values. Because of this problem it is more important to optimize the metal resistances than that of the silicon.



POWER NPN
ISOLATED AREA = 5.7 mm²

MAXIMUM CURRENT = 20A
R_{SAT} = 30 mΩ

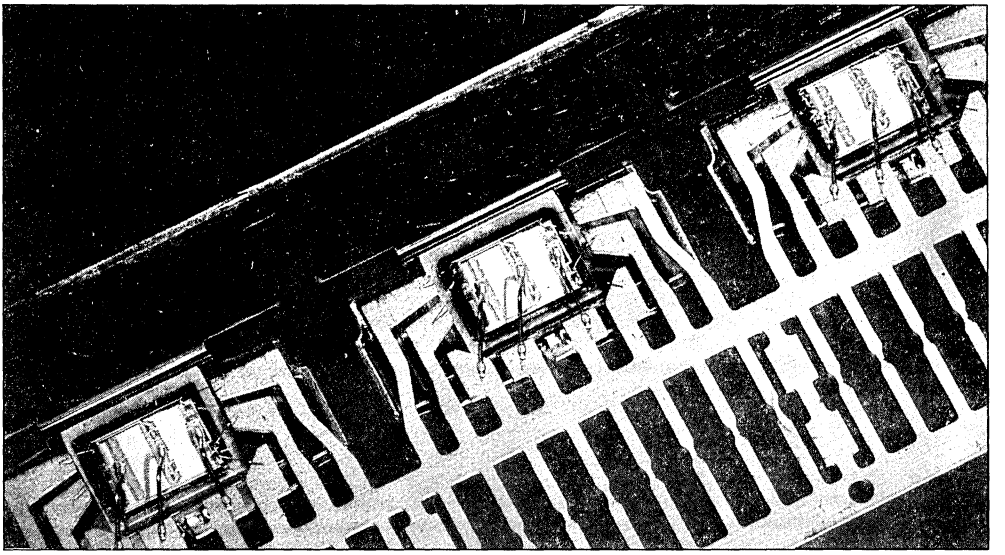
CONTRIBUTION TO R_{SAT}:
- **WIRES 6 mΩ**
- **METAL 10 mΩ**
- **SILICON 14 mΩ**

THIS IS OBTAINED BY:
- **USING DOUBLE METAL THICKNESS (0.7 + 5 μm)**

is performed in the bus interface chip which will be placed between the L9936/7 and the multiplex bus. Since these interface chips are system dependent they are always developed for a specific application, rather than being standard parts like the power ICs.

The mixed wire bonding technology used in the new ICs is clearly visible in the photo, figure 3. Because of the high current it is not possible to use the standard thin gold wires employed in

Figure 3: The mixed bonding technology used in the L9936 — shown here after bonding but before encapsulation — reconciles the conflicting requirements of current and silicon area. Thick aluminum wires are used for the power connections; thin gold wires for the signal connections.



standard ICs. Thick gold wires are out of the question, partly because of cost, but also because they are too rigid to bond to the chip without damaging it.

One alternative, widely used in simple power ICs, is to use thick aluminum wires. However, a thick aluminum bonding wire needs a large bonding pad on the die. In a simple device like a 3-terminal regulator this is not a problem because there are few such pads, but for more complex ICs with eight or more connections the wasted silicon area would be excessive.

Another alternative, still used by some companies, is to use two or more thin gold wires in parallel for each power connection. This solution, however, is costly because more gold wire is needed and it is prone to reliability problems because it is extremely difficult to verify each bond. Moreover, for the currents used in multiplex applications so many parallel wires would be needed this method would be totally impractical.

SGS-THOMSON has developed and industrialized a different solution: a mixed bonding technology where thin gold wires (50um) are used for signal connections and thick aluminum wires (250um) are used for power connections. The two bonding wire types can be clearly seen in figure 3. Note also that the bonding pads for the aluminum wires are oriented in the direction of the wire to avoid needless waste of silicon area.

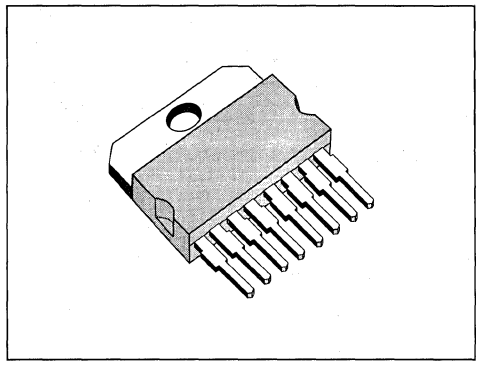
Because gold and aluminum are bonded using different techniques this has necessitated a two-step bonding operation. Moreover, because of the combination of different bonding metals the leadframe has to be plated with a special gold alloy. This plating is selective, being applied only to the bond area, partly for economy and partly to avoid gold on the external leads, which could contaminate soldering baths, causing reliability problems on PC boards.

Different bonding techniques are used to weld the two types of wire to the surface of the chip. For the thin gold wires the thermosonic method is used where an electric discharge first creates a small ball on the free end of the wire; this ball is then pressed onto the bonding pad and vibrated rapidly (in the ultrasonic range), causing the gold ball and silicon surface to weld together.

The thicker aluminum wires are bonded using the simpler ultrasonic method, where the wire is simply pressed onto the surface of the chip then vibrated rapidly to weld the wires to the pad. Because more vigorous vibrations are used in this technique the aluminum wires are bonded first, followed by the gold wires.

To guarantee automotive-level reliability the bonds are pull tested on a sample of parts. In this test the wires are pulled to determine their breaking strength. Gold wires must resist a force of at least 15g; aluminum wires must resist a pull of

Figure 4: After molding and cropping the finished part looks like this. This eight-lead version of the Multiwatt package — first developed by SGS-THOMSON in 1979 — has wider lead spacing to suit the large high current PCB tracks.



130g. Moreover, the wire must break leaving the bonds intact — if a bond detaches before the wire breaks the part fails the test.

The L9936 is housed in a new eight-lead version of the successful Multiwatt package, originally developed by SGS-THOMSON in 1979 (figure 4). This version has eight leads in line at 0.1" centers, rather than the usual two rows of leads. This makes the Multiwatt-8 package suitable for very high current devices where wide PCB tracks are needed. An 11-lead Multiwatt package is used for the L9937.

The new package also has a larger die flag — to accommodate today's large chip sizes — which has necessitated the addition of new antistress features in the frame design. These features ensure a dependable adhesion between frame and resin — essential for humidity resistance — and isolate the die flag mechanically from the external tab to ensure that the die is not damaged if the tab is deformed during mounting.

In a typical application both the L9936 and L9937 are used with a customer specific interface chip which handles bus interface and protocol handling functions. Two different approaches at the system level are used today (figure 5). In the first case each load has its own interface, connected directly to the multiplex bus. An alternative is to combines several load units into a single module; this approach is very attractive in situations like door multiplex where there is a high concentration of loads in a distinct and fairly compact assembly.

Figure 6 shows a generic door multiplex solution of the second type, illustrating the role of the new high current bipolar driver ICs. In this example an L9937 drives the door lock motor, two L9936's drive the windowlift motor, a VN02 high side

driver IC drives a hazard warning light (the light on the edge of the door that turns on whenever the door is opened) and an L9946 multiple half-bridge IC drives the three rear-view mirror motors (two for mirror adjustment and one for "folding" of the whole mirror unit for car washes and so on) and the mirror de-icing heater. All of these integrated circuits are available today.

Pure bipolar technology is used only for the very high current ICs. For all of the other parts a mixed bipolar+CMOS+DMOS technology has been chosen because of the higher efficiency of DMOS power stages and because it allows the integration of complex parts. The L9946 multiple half bridge, for example, has a four high power half bridges plus a microprocessor interface all on the

Figure 5: Two approaches are being used for multiplex systems. In the first each load has its own bus interface; in the second loads are grouped together and share a common electronics module. This approach is used in door multiplex systems, where the loads are all close together and multiplex wiring used primarily to reduce the number of wires passing from the body to the door.

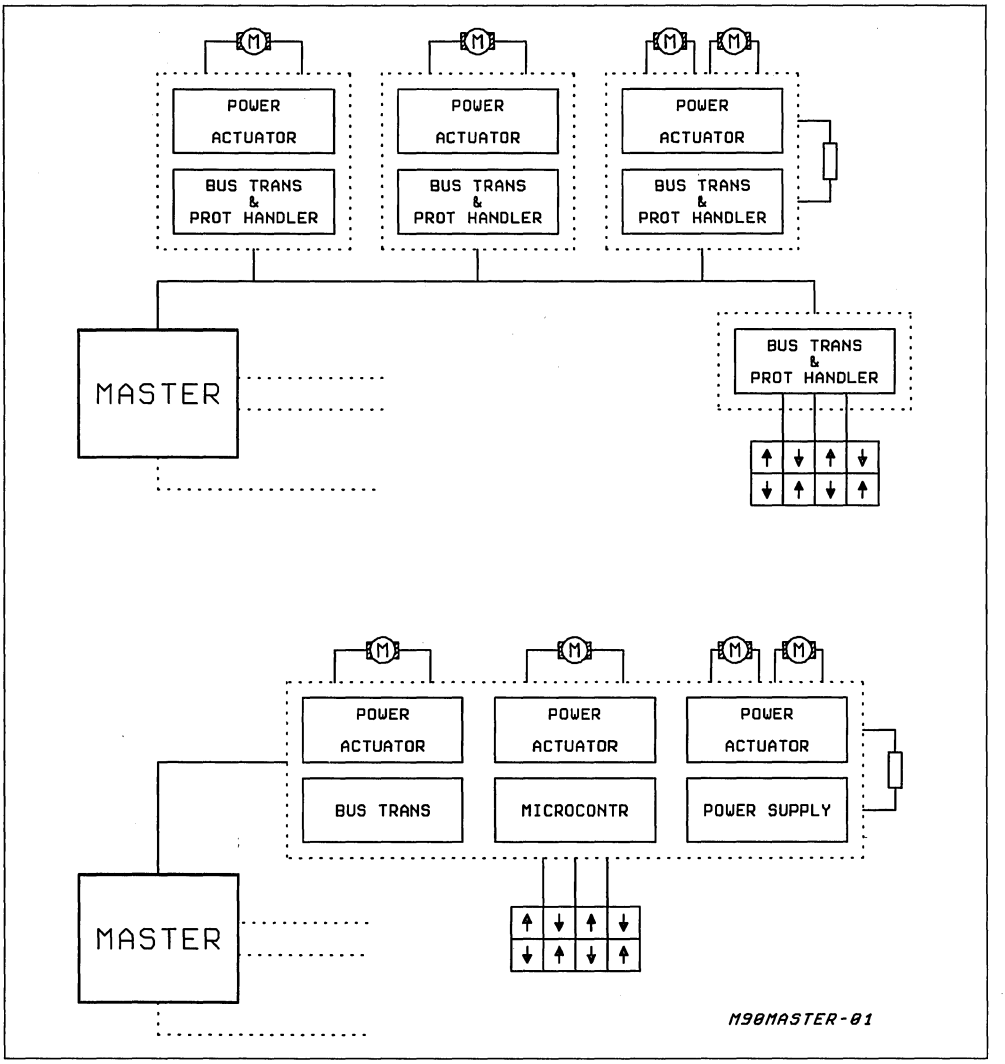
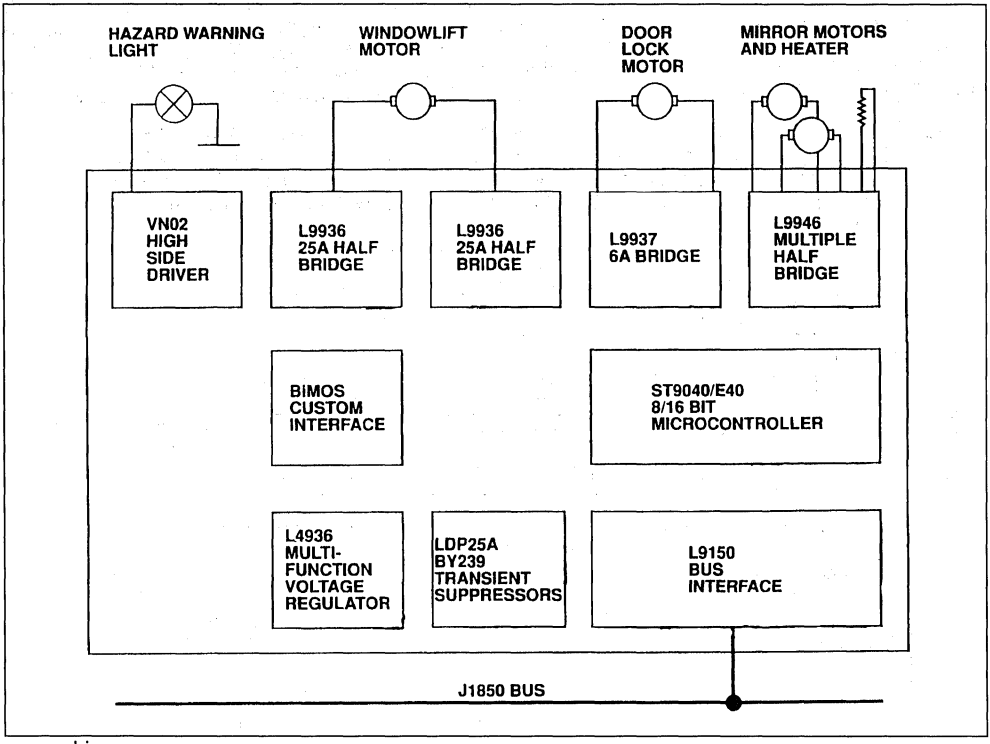


Figure 6: A typical door multiplex solution will use a mixture of high current bipolar power ICs and BCD power ICs. Solutions of this type will be on production models in 1991.



same chip.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

MIXED WIRE BONDING TECHNOLOGY FOR AUTOMOTIVE SMART POWER ICs

by R. Ferrari and A. Massironi

By using a mixture of gold and aluminum bonding wires in the same IC, SGS-THOMSON has found a reliable way to correct very high current ICs that avoids wasting die area.

One of the essential prerequisites for the large-scale introduction of multiplex wiring systems for vehicles is the availability of high power integrated circuits (ICs) capable of replacing relays, driving directly lamps, motors and solenoids. These ICs must be rugged and highly reliable yet inexpensive. Many power ICs suitable for this market are already available but a gap was left at the high current — roughly 4A+ — end of the range; ICs delivering 20A or more are needed for loads like windowlift motors.

One of the main problems in high current IC design lies in the thin wires that connect the silicon chip itself to the external connections of the IC package. These bonding wires are typically fine gold wires (up to 50um thick) which cannot carry more than a few amperes of current.

Increasing the thickness of the gold wires is ruled out partly because of cost, and also because they are too rigid to weld to the surface of the chip without damaging it. It is possible in theory to use two or more gold wires in parallel for each connection but this solution is generally impractical because the large number of bonding pads waste space on the chip (the cost of a silicon chip is proportional to its area), the cost of the wire is excessive and because testing each bond is difficult.

Figure 1: Part of an almost completed strip of integrated circuits utilizing the new mixed bonding technology. The gold and aluminum wires connecting the silicon chip — the small gray rectangle — with the gold-plated external connections can be clearly seen.

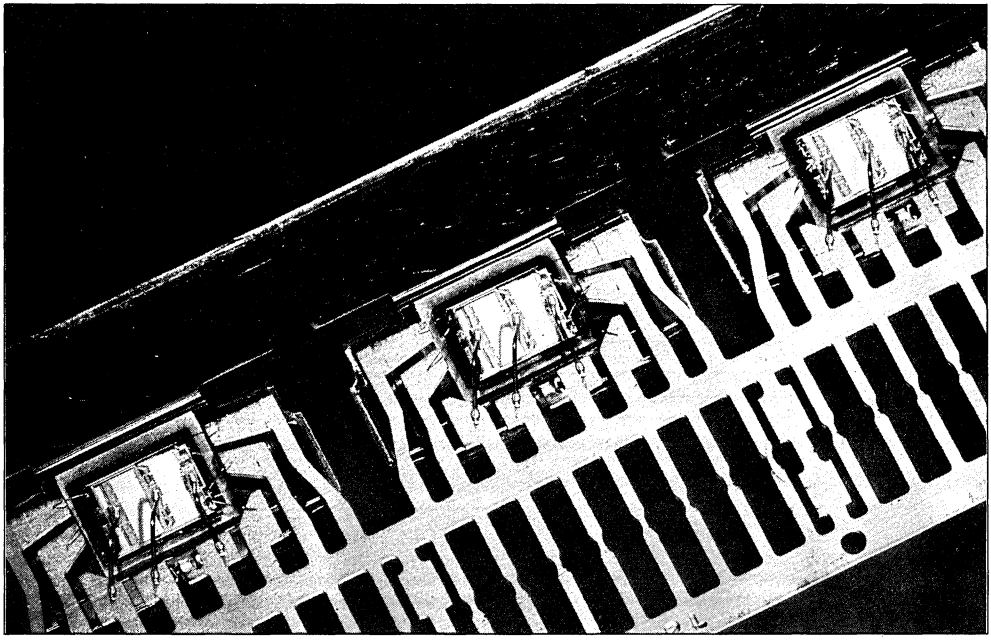
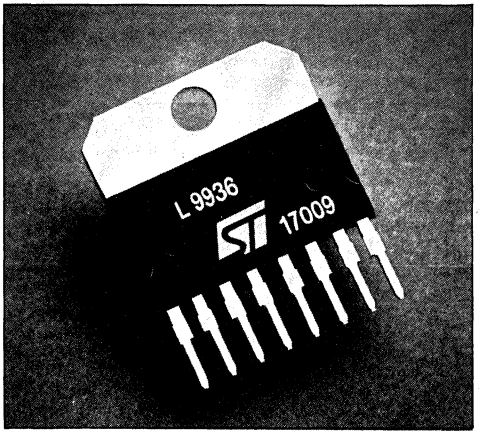


Figure 2: After the wire bonding operation the completed frame assembly is encapsulated in black plastic resin and the parts of the metal frame that served as a mechanical support are removed. The finished parts are then tested and marked with the type number and lot tracing information.



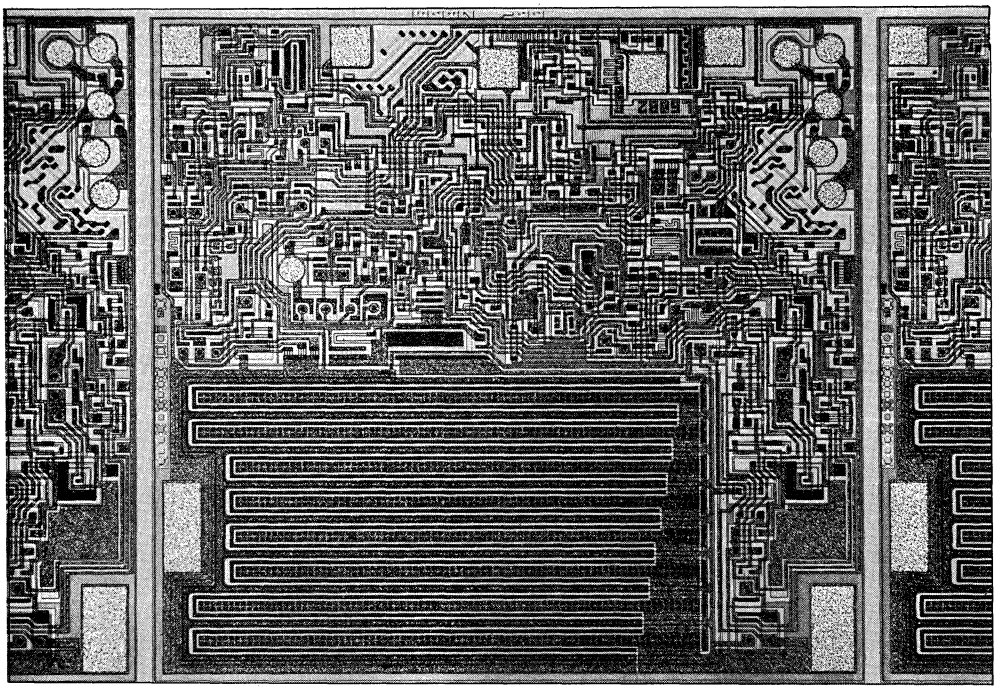
One alternative, widely used in simple power ICs, is to use thick (250um) aluminum wires. However, a thick aluminum bonding wire needs a large bonding pad on the die. In a simple device like a 3-terminal voltage regulator this is not a problem because there are few such pads, but for more complex ICs with eight or more connections the wasted silicon area would be excessive.

SGS-THOMSON has developed and industrialized an effective and efficient solution to this problem: a mixed bonding technology where thin gold wires are used for low current connections and thick aluminum wires used for power connections. Figure 1 shows a bonded frame of a 20A windowlift motor driver that uses this method; the two types of bonding wire can be clearly seen. Figure 2 shows the same IC after encapsulation with black molding resin and removal of the support elements of the frame.

Because of the use of aluminum bonding wires a selective gold alloy plating of the leadframe is necessary; gold is one of the few metals that will weld reliably to aluminum. Apart from reasons of cost, gold plating is used selectively — rather than the simpler overall plating — because of gold were used on the external lead part of the frame it would contaminate the circuit board soldering bath, leading to possible reliability problems.

Different bonding techniques are used to weld the

Figure 3.



two types of wire to the surface of the silicon chip. For the thin gold wires the thermosonic method is used where an electric discharge first creates a small ball on the free end of the wire, this ball is then pressed on to the bonding pad and vibrated rapidly (in the ultrasonic range), causing the gold ball and silicon surface to weld together.

The thicker aluminum wires are bonded using the simpler ultrasonic method, where the wire is simply pressed onto the surface of the chip then vibrated rapidly to weld the wire to the pad. Because more vigorous vibrations are used in this technique the aluminum wires are bonded first, followed by the gold wires. On the production lines two separate machines are used in tandem.

Reliability is an important consideration in automotive ICs therefore it is essential that wire bonds be secure throughout the lifetime of the circuit. To ensure that bonds are correctly executed some parts are subjected to a pull test, where the wires are pulled to determine their breaking strength. Gold wires must resist a force of at least 15g; the thicker aluminum wires must resist a pull of 130g. In both cases the wire must break; the bonds must not detach.

These pull tests are also repeated on statistical samples after accelerated life testing where parts are subjected to humidity, thermal cycling, and other stresses.

Mixed bonding technology can be used in various different power IC packages, though the photos here show the Multiwatt-8 package. This type has eight leads in line at 0.1" centers — wider than is usual — to suit high current circuits where wide circuit board tracks are used. The metal frame design of such packages reflects the care taken to ensure reliability in line with the needs of the auto market. For example, the die-mounting zone of the frame is isolated mechanically by notches and groove from the external mounting tab area. This ensures that deformation caused by overtightening the mounting screw will not subject to stress that could adversely affect reliability.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

HOW DESIGN RULES INFLUENCE THE HIGH FREQUENCY SWITCHING BEHAVIOUR OF POWER MOSFETs

by A. Galluzzo, M. Melito, M. Paparo

ABSTRACT

Starting from the basic structure of a Power MOSFET this paper describes the electrical equivalent circuit, it analyses in detail the relationship between the physical structure and the switching behaviour of the device, mainly in the high frequency range, introducing $R_{DS(on)}$, C_I and C_{OSS} gate charge concepts.

A comparison of power losses of devices rated at different BV_{DSS} of die size is carried out.

The influence of the state-of-the-art Power MOSFET structure on the ruggedness of the devices (dV/dt induced from the application circuit and unclamped inductive switching) is also briefly analysed.

Some future structural modifications improving both switching behaviour and resulting ruggedness are described.

Lastly a brief overview of IGBT technology is discussed underlining their advantages and drawbacks compared with Power MOSFET devices.

INTRODUCTION

In spite of their relatively recent introduction on the market Power MOSFET devices are becoming certainly the most successful "high runners" in the Power actuators and industrial application field because of the inherent advantages introduced in terms of switching times and simplicity of the drive.

This paper aims to outline some of the factors that are under the control of the Power device designer that enable him to improve the performance of Power MOSFETs for the benefit of system designers while leaving the basic Power MOSFET structure unchanged.

POWER MOSFET EQUIVALENT CIRCUIT

Fig 1 shows the cross section of an N-channel enhancement mode Power MOSFET structure while fig. 2 shows the equivalent electrical schematic of the device including the most important parasitic components playing a crucial role for the switching and ruggedness performance of the device.

A Power MOSFET is realized by fabricating thousands of elementary square cells where source regions are connected together by means of a common surface metallization[1].

A polysilicon layer interconnects the gates of all cells. The source region of a cell is inside a P-layer which forms the channel region necessary to control the vertical current flow of the device.

The following list is a key to the drawing of the simplified model shown in figure 2:

R_G = Polysilicon gate resistance

C_1 = Capacitance between gate and source

C_2 = Capacitance between gate and P region

C_3 = Capacitance between gate and N epytaxial layer

C_4 = Capacitance of the channel depletion zone

C_5 = Capacitance of the depletion zone in the superficial epitaxial layer

C_6 = Capacitance of the body-drain junction

In the text, reference is also made to the following capacitances:

C_{GD}: total equivalent capacitance between gate and drain

C_{GS}: total equivalent capacitance between gate and source

C_{DS}: total equivalent capacitance between drain and source

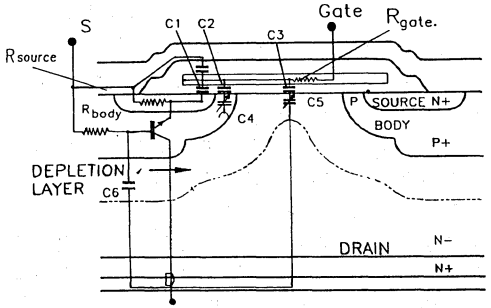


Fig. 1 - Power MOSFET structure.

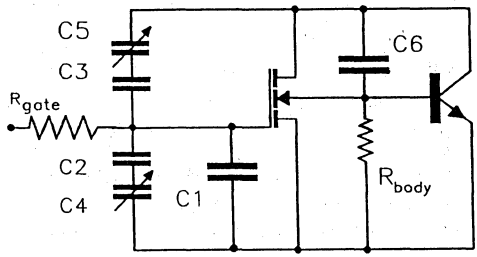


Fig. 2 - Power MOSFET equivalent circuit.

The parasitic bipolar transistor shown in fig.2 is formed by the body region between the N area of the source and the N epi layer of the drain.

The body-source resistor is due to the P-body bulk resistance and the P-body/metal contact resistance.

For most of the applications it is sufficient to substitute, on the schematic diagram, a "body-drain diode" in place of this parasitic bipolar transistor.

Device behaviour is straightforward in fact with positive drain-source biasing, as soon as the gate source voltage reaches the threshold voltage (V_{th}), necessary to invert the P-well region below the gate oxide, the current begins to flow from drain to source regions. The relationship between V_{DS}, V_{GS} and I_D is the typical input-output characteristic.

In switching applications, once the circuit topology has been established (type of converter, frequency, magnetics etc.), the optimization of the design requires the minimum of power losses possible.

During the device's on-state, $R_{DS(on)}$ is the parameter to be taken as low as possible to reduce losses; this parameter is normally defined as follows:

$$R_{DS(on)} = R_{CH} + R_{ACC} + R_{JFET} + R_{EPI}$$

Where:

- R_{CH} is the channel total equivalent resistance, depending on the horizontal layout of the device channel length and channel perimeter,
- R_{ACC} is due to excess charges within the drain region below the gate oxide,
- R_{CH} and R_{ACC} are the most dominant contribution for low voltage devices,
- R_{JFET} is the resistance of the drain region between the P body regions of two adjacent cells,
- R_{EPI} is due to the intrinsic epy bulk resistance therefore strongly dependent on BV_{DSS}.

SWITCHING BEHAVIOUR

The switching behaviour of a Power MOSFET is affected by the unavoidable parasitic capacitances of the structure. Therefore switching losses can be predicted taking into account the gate charge curve and the output capacitance, C_{DS}. Second order effects due to packaging and assembly will be neglected in the following discussion as they can be taken into account by means of suitable macromodels for computer simulation [2.3]

The gate charge curve (fig.3), obtained by injecting a constant gate input current is split into several areas.

At the beginning, starting from

$$V_{GS} = 0,\ Ci \approx C1 + C2 + C5,$$

I_D remains equal to I_{DSS} until V_{GS} reaches V_{TH} (region 1); C4 decreases further when V_{GS} increases so that when

$$V_{GS} = V_{TH},\ Ci \approx C1 + C4 + C5.$$

Therefore I_D builds-up while V_{GS} increases from V_{TH} up to $V_{TH} + I_D/gm$ (region 2). Due to the linear behaviour of the Miller body drain capacitance, V_{GS} remains constant while V_D decreases until the device becomes fully ON (region 3 and 4)

$$Ci \approx C1 + C4 + C3$$

In the saturation region (5) a further increase of V_{GS} yields a V_{DS} decrease down to $R_{DS(on)} * I_D$.

The gate charge curve is obtained at constant gate current hence the horizontal axis is proportional to the stored charge and to the time necessary to switch on and off under defined driving conditions.

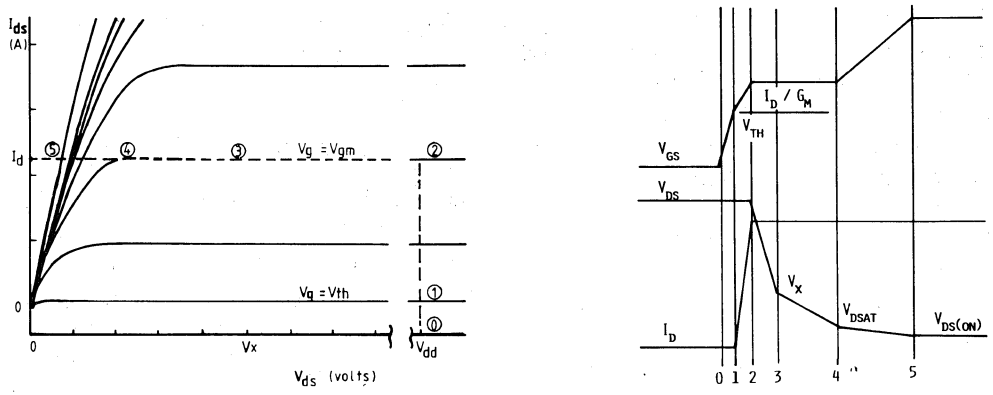


Fig. 3 - Load line and dynamic characteristics versus gate charge.

Therefore it follows that a first comparison between two devices rated at the same voltage and $R_{DS(on)}$ can be made by simply looking at their gate charge characteristics.

C_{DS} capacitance does not influence the evolution of the gate voltage but is responsible for the power losses during switching.

C_{DS} does not generally limit the dV/dt experienced by the drain region. In fact, for a high voltage device (IRF830) with the following bias conditions:

drain voltage V_{DD} = 400V

gate voltage max VG = 15V

gate external resistor R_G = 10 ohm

d_Q = charge variation inside zone 3 of the gate charge curve the dV/dt imposed by the drain voltage is:

$$dV/dt = V_{DD} * (V_G - V_{TH})/(d_Q * R_G) = \frac{400 * (15-3.5)}{20 * 10^{-9} * 10} = 23 \text{ kV/msec}$$

As : $I_D = C_{DS} * dV/dt$ and C_{DS} = 44 nF (typical)
I_D is about 1A

$$I_D = 44 * 10^{-12} * 23 * 10^9 = 1A.$$

A current of roughly 1 Amp is then required to charge C_{DS} at the dV/dt set by the gate circuit: because the device has a nominal current of 5 Amps, C_{DS} has little influence when an IRF830 is used in standard applications.

This means that in most of the cases it is possible to take into account the effects of C_{DS} when calculating the power dissipation during both turn-on and turn-off.

The situation in resonant converters is quite different, where the current or voltage is negligible during switching and the previous approach is no longer valid. C_{DS} effects now influence the stored energy.

Fig. 4 shows how $R_{DS(on)}$ and C_{DS} limit the device working frequency in resonant converters.

The power dissipation versus working frequency for devices rated at different breakdown voltage, die size and $R_{DS(on)}$ has been analysed.

It can be observed that a high voltage Power MOSFET dissipation at low frequency is greater than the power dissipation of a medium voltage one with the same die size.

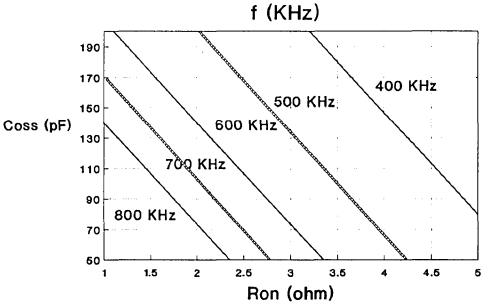


Fig. 4 -How $R_{DS(on)}$ and C_{DS} limit the device working frequency.

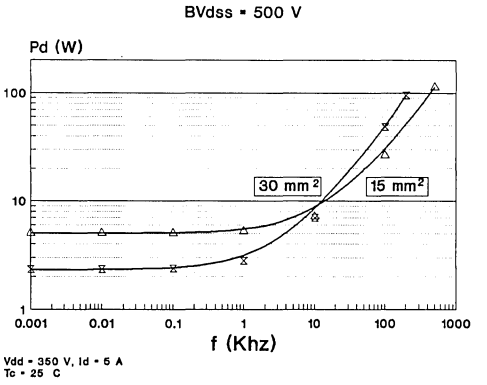


Fig. 5 - Power Dissipation versus frequency.

A simple explanation can be based on the higher value of R_{epi} of high voltage devices in comparison to medium voltage ones.

Increasing the cell packing density, especially for low voltage devices allows reduction of the die size while maintaining the same $R_{DS(on)}$ and gives an improvement in capacitance values and of the power dissipation at high frequency (where the power losses are more significant during switching).

Fig. 5 shows that a well defined application requires the right Power MOSFET device. A device with a large $R_{DS(on)}$ will be preferable for the same BV_{DSS} if the target is optimised efficiency at high frequency.

PERFORMANCE vs LAYOUT RULES

For low voltage devices it is possible to improve the $R_{DS(on)}$ and the gate charge curve by optimizing the horizontal layout and dopant profile. Fig. 6 shows the improvement obtained in gate charge characteristics for 3 devices rated at 60V, 20 milliohm, each with different cell packing density and bonding on the cells.

Cell dimension and the distance between adjacent cells are respectively 19μm and 15μm for standard devices, 14μm and 8 μm for very high density device, 10μm and 6μm for ultra high density devices.

The different behaviour is obtained because of better exploitation of the silicon area with reduced cell dimensions and distances which produce a reduced total device area for a given $R_{DS(on)}$

For high voltage devices the most significant term that contributes to $R_{DS(on)}$ is R_{epi}. Nevertheless, optimization of horizontal layout strongly influences the capacitance values (C_1 to C_5).

Starting from the standard 500V process of 0.35 Mcell/inch^2 performance can be improved by both increasing cell density up to 0.76 Mcell/inch^2 and the oxide thickness of critical cell areas (reducing C_{DS} capacitance) (see fig.7).

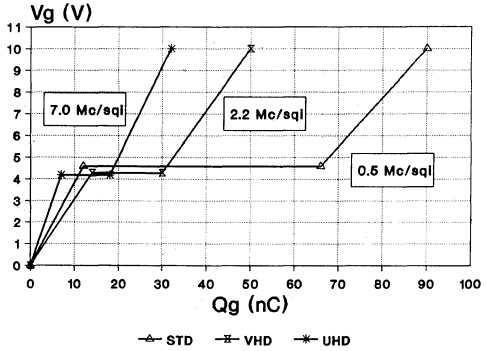


Fig. 6 - Influence of cell packing density on gate charge.

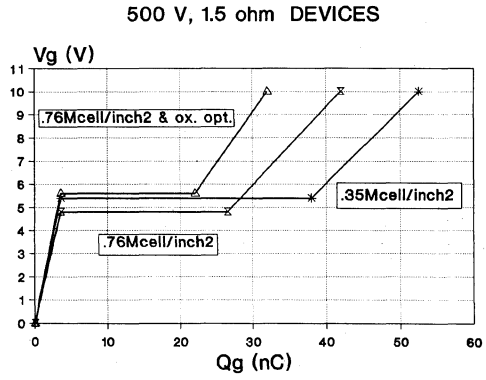
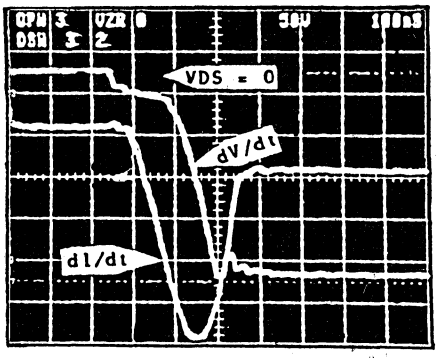
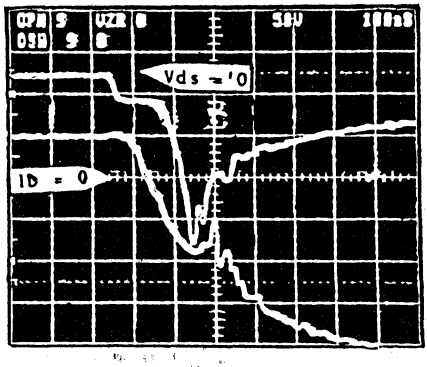


Fig. 7 - Oxide and layout influence on gate charge.



Diode recovery
V = 50V/div I = 5A/div
DI/dt = 200A/µS, dV/dt = 2V/ns



Parasitic turn-on during
Diode recovery I = 10A/div
dI/dt = 250A/µS, dV/dt = 4V/nS

Fig. 8 - Typical waveforms when failure occurs.

RUGGEDNESS

A very important characteristic of power devices is ruggedness.

A Power MOSFET must withstand a static and dynamic dV/dt U.I.S. (unclamped inductive switching) caused by the application and environment.

A failure due to static dV/dt occurs when a sudden voltage variation is experienced between the source and drain of a power MOSFET in the off state; this causes a current flow through both the body-drain capacitance and the body resistance: if the current is big enough the voltage drop across R_B causes the parasitic transistor to switch on and the device fails because of the simultaneous

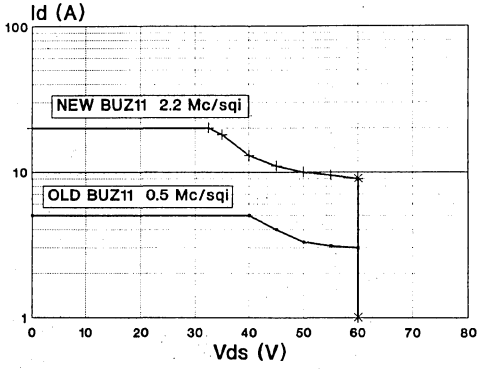


Fig. 9 - Ruggedness improvement.

presence of high voltage and high current with a subsequent hot spot generation.

The dynamic dV/dt occurs when fast voltage variation finds the body-drain diode in recovery conduction (after freewheeling behaviour). Now the current flowing through R_B is the sum of the recovery current and the current due to the body-drain capacitance.

Clearly a lower dV/dt than the previous case can now produce device degradation.

Fig. 8 shows a typical waveform during this kind of failure.

When the device switches an inductive load and the drain-source voltage overcomes the nominal defined breakdown value, then unclamped inductive switching occurs.

When this happens the energy stored in the load inductor discharges rapidly through the device at breakdown voltage, forcing I_D current, to flow in the device and increase junction temperature. Under effect of the temperature change the V_{BE} of the parasitic BJT decreases and can cause switch-on of the transistor itself, the current flowing in R_b (body bulk).

When even a small portion of the parasitic BJT switches on the whole Power MOS fails because of the current focusing effect.

The failure mechanism is almost the same for all described stress. A way to improve the ruggedness of the device is to optimise its vertical and lateral structure reducing R_B and the low current gain of the parasitic transistor as much as possible.

Fig. 9 shows the improved ruggedness obtained by the optimization of body doping in comparison with the first generation Power MOS.

IGBT VERSUS POWER MOS

From the results of measurements referring to switching speed and ruggedness the Power MOS is an almost ideal device due to unipolar conduction, but in some very high voltage applications, the device's $R_{DS(on)}$ becomes a real limitation.

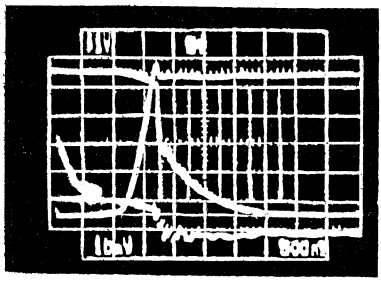
For applications at high voltage where $R_{DS(on)}$ losses are of primary importance, IGBTs find a suitable environment.

An IGBT has the same structure as the Power MOS and additionally has a P-layer under the standard N doped drain. When the device is on the P-N junction so realized injects minority carriers into the drain region modulating its total epi resistivity.

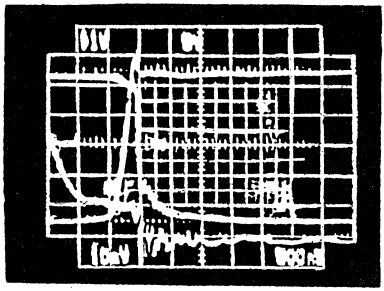
This means that the IGBT is a high voltage device with an insulated gate having a low voltage drop during the conduction phase.

In the structure of the IGBT it is easy to recognize a PNPN (degenerative) structure driven by a power MOS.

This implies that a device designer must realize a device with a degenerative current value (I_{LATCH}) greater than the nominal current in all working conditions, to ensure that the PNPN structure never turns-on. This is



Vds - 80 V/div
Id - 2 A/div
Vg - 5 V/div
Rg - 100 ohm
L - 180 µh
T - 100 °C



WITHOUT IRRADIATION

WITH IRRADIATION

Fig. 10 - IGBT switching characteristics.

well demonstrated in practice because $I_{LATCH} > 5\ I_D$ nominal in all conditions. An additional way to design latch free devices is to control transfer characteristic g_m so that for a given driving condition drain current never exceeds the permitted I_{Dmax}(I_D latch).

Currently the state-of-the-art fall time of an IGBT's drain current is longer than that of equivalent power MOSFET of same area. In fact when the power MOSFET in the IGBT structure is switched off, the charge stored in the base of the PNP parasitic transistor can be removed only by intrinsic carrier recombination.

Referring to fig.10 the first portion of t_{fall} is related to power MOSFET switch-off while the tail is due to the longer recombination time of the carriers.

A well known method to speed-up the switching off behaviour of the device is the lifetime killing technique using gold and platinum doping, ion implantation and ß irradiation. Fig.10 shows the improvement of

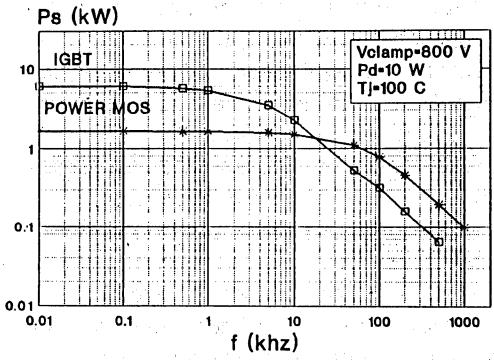


Fig. 11 - Power MOSFET versus IGBT.

IGBT's fall time obtained with ß irradiation of the device.

A comparison of the power handling capability of a 1000V IGBT and a 1000V Power MOS of both $25mm^2$ is shown in fig.11 where P_D is kept constant (10W).

It is undoubtedly advantageous to use IGBT's at a frequency below 20kHz to reduce losses and cut silicon costs.

The 3rd generation of IGBTs showing a fall time lower than 200nsec will allow the crossover point of fig.11 to move up to 50kHz.

CONCLUSION

State-of-the-art power MOSFETs and IGBTs have been shown to be rugged and reliable as a result of many years of production and technological know-how. Nevertheless, the uninterrupted progress of the technology and the constant relationship with final users and system designers is a challenge for the device designers. They must take into account second order effects and new demands to provide continuous improvement of field controlled devices both in terms of performance and lower cost.

With the aim of reaching better performance the main targets for improving the devices have been defined. These concepts will also be applied to the production of new devices. Detailed design rule variation will produce significant improvements in low voltage devices; increasing cell density and tuning dopant profiles. For medium-high voltage devices switching losses will be greatly reduced by varying the differentiating oxide thickness in conjunction with the covered active regions of the device layout.

These new design rules will therefore lead to better power conversion efficiency and greater ruggedness.

The predicted, reduced switch-off time as low as 0.2msec,obtained by new life-time control techniques (tested on 500V laboratory devices) will allow IGBTs to be cost effective competitors to power MOSFETs in the high voltage, medium frequency range (30 to 50kHz).

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SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

GATE CHARGE CHARACTERISTICS LEAD TO EASY DRIVE DESIGN FOR POWER MOSFET CIRCUITS

by M. Melito, F. Portuese

ABSTRACT

The traditional method of specifying input impedance for power MOSFETs is not incorrect, but it is incomplete and often leads to confusion when it is used as a design tool. An alternative method is to use the gate charge curve, which is directly related to the total input impedance and allows a simple evaluation of the drive energy and the switching performance to be made.This paper deals firstly with an analysis of the gate-charge waveform which is related to the device physics and develops an analytical expression, which gives a very good approximation of the total gate-charge. Secondly, the influence of the electrical parameters, both external to the device (e.g. I_D, V_{DD}) and the internal ones (V_{th}, g_{fs}, C_{iss}, C_{oss}, C_{rss}, cell density) are analysed.The paper also highlights how it is possible to extrapolate the actual dynamic behaviour of the device easily from this curve. Finally, an evaluation criterion is suggested that allows a comparison to be made between the actual performances, both static and dynamic, of devices with similar nominal characteristics.

GATE CHARGE MEASUREMENT

During the switching of a POWER MOSFET, the gate current has the typical behaviour of current in an RC circuit, see figure 1. The transient lasts for some tens of nanoseconds or more, due essentially to the RC time constant and the maximum current available in the driving circuit. If the current in the gate, I_g, is constant and small enough, the switching time can be increased to a level where the voltage and the current waveforms are free from the parasitic effects caused by the stray inductances that are usually associated with high frequency power switching. In this way it is possible to isolate the influence of the external factors and analyse only the internal parameters. The test circuit and the related waveforms are shown in figure 2.

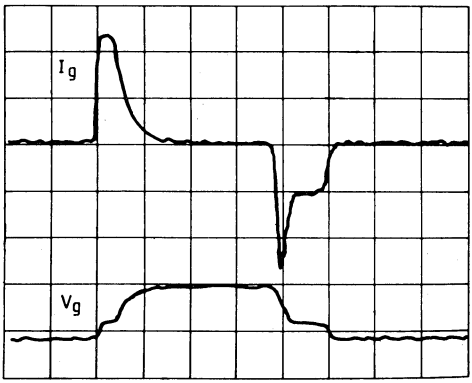


Fig. 1 - I_g, V_{gs} waveforms

GATE-CHARGE CURVE ANALYSIS

To get a better understanding of the phenomena which occur during switching it is useful to refer to the model of the POWER MOSFET shown in figure 3b. The figure 3a shows the cross section of a single cell illustrating the parasitic capacitances. The gate-charge waveform is strictly related to the modulation of the gate-source equivalent capacitances during switching. This is due to the variation of the intrinsic capacitance of the device with gate and/or drain voltage. Figure 4 shows the load line and C_{gs}, C_{gd} variation during each phase of switching. Figure 5 shows a typical gate-charge curve: the capacitances influencing the shape and the length of each zone are marked.

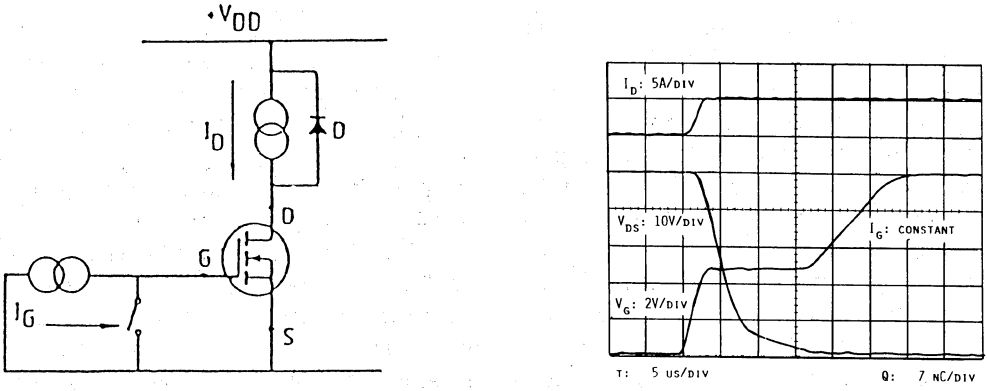
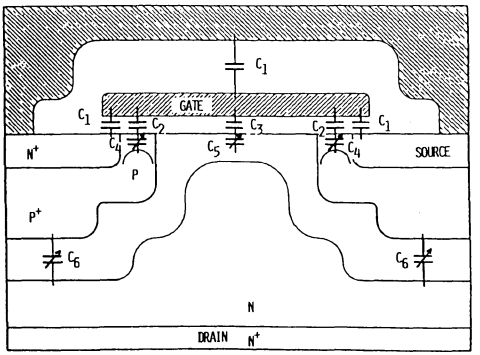
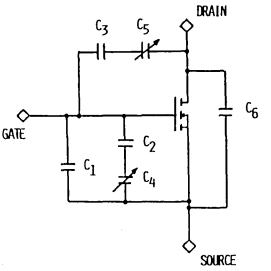


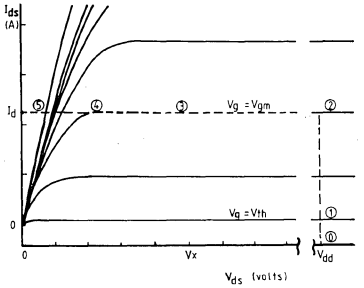
Fig. 2 - Test circuit and related waveforms.





C_1: Capacitance between gate and source (both N° and metal)
C_2: Capacitance between gate and P zone.
C_3: Capacitance between gate and epi N.
C_4: Capacitance of the depiction zone in the superficial epi.
C_5: Capacitance of the depietion zone in the superficial epi.
C_6: Capacitance of the body-drain junction.

Fig. 3 - Cross section of a Power MOSFET cell and its electrical equivalent.



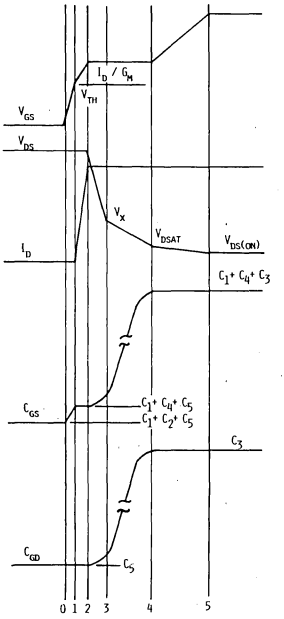


Fig. 4 - Load line and capacitances modulation.

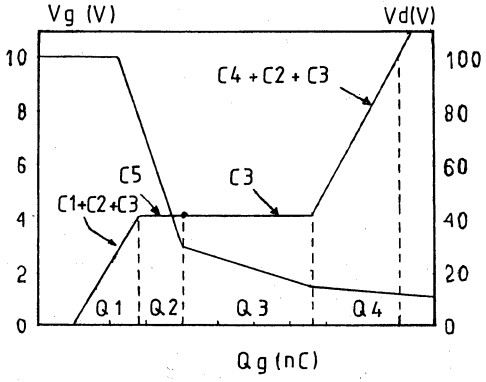


Fig. 5 - Gate charge curve

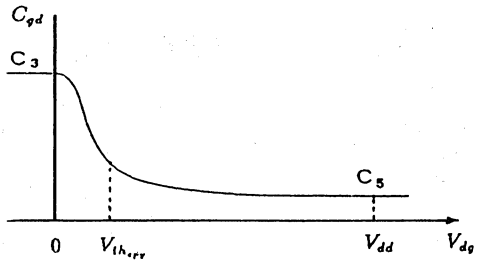


Fig. 6 - C_{gd} modulation

In the first zone the equivalent capacitance is nearly equal to C_{iss} because V_d is constant and the variation of V_g has no influence. The charge supplied to the gate can be approximated by the expression :

$$Q_1 = (C_1 + C_2 + C_5) \cdot V_{gm} = C_{iss} \cdot V_{gm}$$

where V_{gm} is the gate to source voltage required to just carry the desired I_d and it can be easily deduced using the output characteristic. In the horizontal zone the equivalent capacitance seems to be infinite, in fact V_{gs} remains constant though charge is supplied to the gate. This phenomenon, known as the Miller effect, is due to the modulation of the capacitance C_{gd} by V_{ds}. The waveform of this capacitance variation is typical of a MOS structure switching from being strongly inverted to the accumulation status, see figure 6.

The only difference is due to the fact that modulation of the depletion zone is caused not only by the voltage but also by lateral injection of the charge coming from the channel.

Looking at the drain voltage, figure 4 and figure 5, a slope variation can be observed occurring at a voltage, V_x, physically corresponding to the transition from a highly charged P zone to simple depletion of the MOSFET capacitor that exists between the deep body cells. The first slope is related to $C_5 \approx C_{rss}$, the second to C_3, the polarity of V_{gd} being so that $C_5 >> C_3$. So the charge supplied to the gate during the Miller effect can be split into two parts:

$$Q_2 = C_5 \cdot (V_{dd} - V_x) \approx C_{rss} \cdot (V_{dd} - V_x)$$

$$Q_3 = C_3 \cdot (V_x - V_{d(sat)})$$

being $V_x = V_{gm} + V_{th\text{-}epy} + R_{epy} \cdot I_d$ and $V_{d(sat)}$ the voltage drain corresponding to the "knee" of the output characteristic with $V_{gs} = V_{gm}$. The slope of the final part is associated with the oxide capacitances. ($V_{th\text{-}epy}$ is the threshold voltage of the MOSFET capacitor existing between the P zone; R_{epy} is the resistance of the drain due to the epi). The charge supplied during this phase is:

$$Q_4 = (C_1 + C_2 + C_3) \cdot (V_{g(max)} - V_{gm})$$

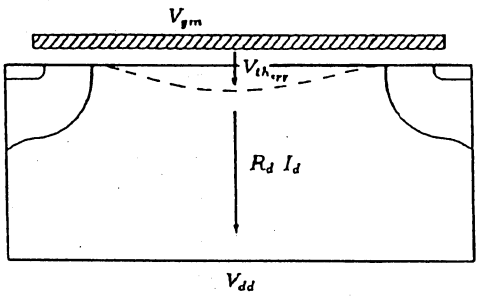


Fig. 7 - V_x evaluation.

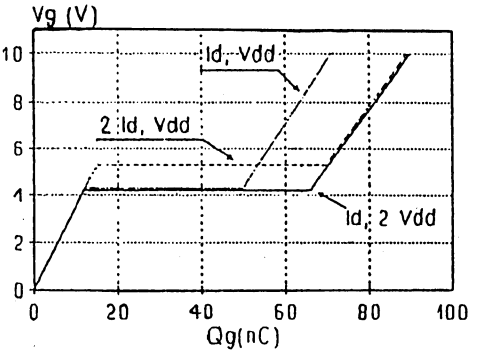


Fig. 8 - Gate charge curves as a function of I_d and V_{dd}.

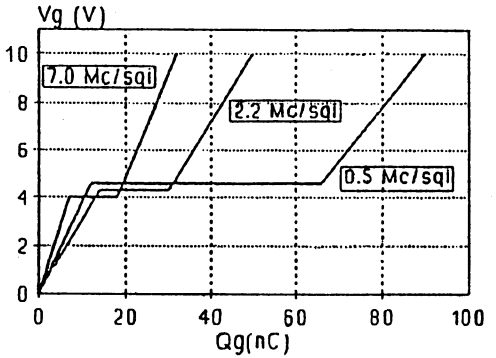


Fig. 9 - Influence of cell density on gate charge.

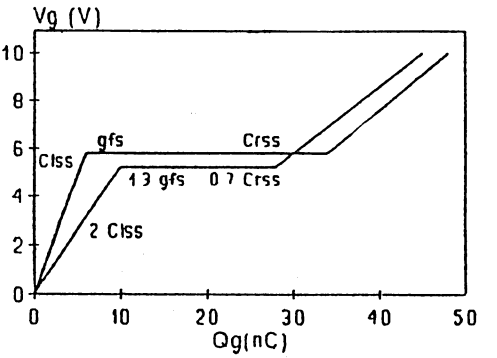


Fig 10 - Comparison of gate charge curves of two devices with different values of C_{iss}, g_{fs} and C_{rss}.

EFFECTS OF THE PHYSICAL AND ELECTRICAL PARAMETERS ON THE GATE-CHARGE CURVE

The previous discussion has shown that the total charge supplied to the gate is influenced by several parameters, which are essentially:

a) electrical parameters (V_{dd}, I_d)

b) structural parameters (cell density, capacitances, V_{th}, g_{fs})

The electrical parameters are imposed by the external circuit and depend on the application; the structural parameters are typical of the device and can be adjusted during the device design stage in order to optimise its performance. Figure 8 shows the influence of I_d and V_{dd} on the shape of the gate-charge curve.

Figure 9 summarizes the effects of the structural parameters: the gate-charge curves of devices having the same static characteristics ($R_{ds(on)}$, BV_{dss}, I_d) and different

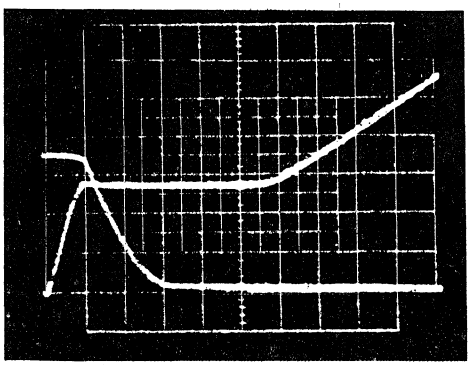


Fig. 11 - Gate charge curve of IRF832. V_{gs} = 2V/div, V_d = 100V/div, Q_g = 5nC/div.

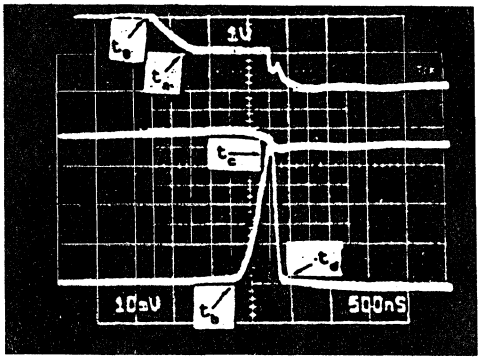


Fig. 12 - IRF832 turn-off. V_{gs} = 5V/div, V_d = 100V/div, I_d = 1A/div, t = 500ns/div, R_g = 180 Ohms.

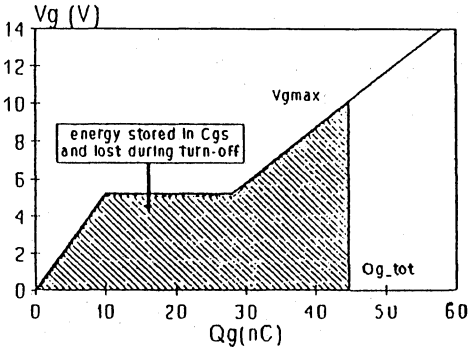


Fig. 13 - Driving energy and gate charge.

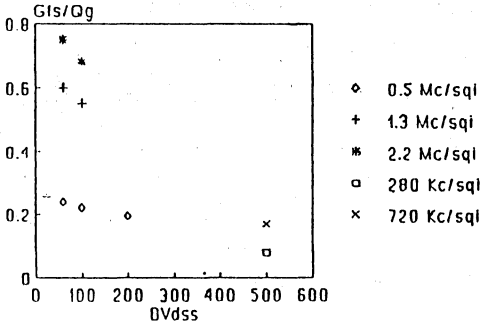


Fig. 14 - Comparison of technologies.

cell densities, are shown. Figure 10 shows the influence of the capacitances and of the transconductance on the same curve.

Use of the gate-charge curve

The gate-charge curve analysis is useful for obtaining important information about device switching characteristics. The following example evaluates the switching time of the SGS-THOMSON IRF832 as an example.

Figure 11 and figure 12 show, respectively, the gate charge curve and the turn-off of the IRF832 measured under similar conditions of I_d and V_{dd}. Note that the horizontal axes of the gate-charge graph are in nanocoulombs ($Q = I_g * t$, I_g=const.) while the vertical axes are in volts. Referring to figure 5 and figure 11, the values of the single contribution to gate charge are:

Q_1 = 5 nC

Q_2 = 11 nC

Q_3 = 13 nC

Q_4 = 18 nC

During t_a, C_{gs} is constant so this time is easy to evaluate using the usual calculation for RC circuits:

$$t_a = R_g * C_{gs} * \ln(V_{gs}(t_0)/V_{gs}(t_a))$$

substituting:

$$R_{gs} = 180,$$

$$C_{gs} = dQ/dV = 18nC / 4.7V = 3829pF,$$

$$V_{gs}(t_0) = 10V,\ V_{gs}(t_a) = 5.3V$$

$$t_a = 438ns.$$

From t_a to t_c, I_g is constant and its value is $I_g = V_{gm}/R_{gs}$ = 29.4mA hence:

$$t_b = Q_3/I_g = 442\ ns$$

$$t_c = Q_2/I_g = 374\ ns$$

During t_d C_{gd} is constant and using the previous expression :

$$t_d = R_g * C_{gs} * \ln (V_{gs}(t_c)/V_{gs(th)}) = 96ns$$

Note $C_{gs} = C_{iss}$

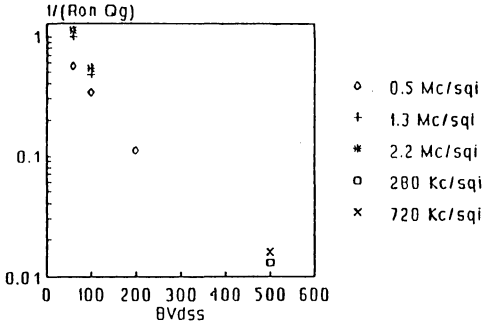


Fig. 15 - Comparison of technologies.

Looking at figure 12 it is possible to see that the calculated times are very close to the measured ones.

The gate charge curve is also helpful because it allows the driving energy to be calculated. The area under the gate-charge curve represents, in fact, the total amount of energy needed to turn-on the device while $V_{gmax} * Q_{g\text{-}tot}$ is the total energy that the driving circuit has to supply, see figure 13.

In order to obtain fast switching with low driving energy and low energy dissipation during the cross-over, the optimum device should have low Q_g and high g_{fs}. To obtain low power dissipation during the on state, the optimum device should have low R_{dson}.

It is useful to define two merit coefficients to give a measure of device performance:

$$K_1 = g_{fs}/Q_g \qquad K_2 = (R_{ds(on)} * Q_g)^{-1}$$

Devices having analogous nominal characteristics (BV_{dss}, I_d) but manufactured using different technologies can be quickly compared, see figure 14 and figure 15. Note that the two coefficients are not dependent on device die size because of their definition. They both depend on switching features (Q_g) but K_1 is related to the saturation zone (g_{fs}) of the Power MOSFET out characteristics whilst K_2 is related to the linear characteristic (R_{on}).

CONCLUSION

The gate charge curve supplies useful information about the actual behaviour when the device switches. From the user's point of view, these curves allow the correct design of the drive circuit and correct choice of the device which best satisfies the design criteria. The use of two merit coefficients allows a quick comparison of devices having similar

nominal characteristics but manufactured using different technologies.

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2. M.MELITO, F.PORTUESE, A.SINERI. "COSMOS: A Tool for Optimisation of Layout and Process Parameters in Power Design", The Electrochemical Society 175th meeting, Los Angeles, May 1989.
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4. A.GALLUZZO, M.MELITO, M.PAPARO "How Design Rules Influence the High Frequency Switching Behaviour of Power MOSFETs", PEC, Long Beach, February '90.

ANALYSIS AND OPTIMISATION OF HIGH FREQUENCY POWER RECTIFICATION

By J.M. PETER

How can the performance of power electronics be improved ? Today, in many cases, it is the job of the designer. The fast rectifier switching behaviour depends on the operating conditions. The analysis and the optimisation of these conditions can be an important source of improvement in performance.

1. SWITCH-OFF OF FAST RECOVERY RECTIFIERS

It is possible to define theoretically two types of switch-off[1].

1.1. FREE-WHEEL MODE (figures 1 & 2)

When the rectifier switches-off it is always in parallel with a voltage source. In this case the assumption is that the parasitic inductances are negligible. This type of behaviour can be met in the majority or rectifier applications such as free-wheel rectifiers in step-down and step-up converters, full wave rectifiers, etc... (figure 2). Generally, a rectifier in free-wheel mode is always in parallel with a voltage source when it turns-off.

1.2. RECTIFIER MODE (figures 1 & 3)

An inductance defines the dI_F/dt (decreasing slope of the rectifier current) and when the rectifier switches-off it is always in series with this inductance. This type of behaviour can be met in some applications such as rectifiers in flyback converters and many functions in thyristor circuits, (figure 3). Generally speaking a rectifier in the rectifier mode is always in series with an inductance L and this inductance L defines the dI_F/dt. The fundamental difference between these two modes is that in the rectifier mode there is a stored energy $1/2LI_{RM}^2$ due to the series inductance. After the turn-off this energy is dissipated in the rectifier and/or in the associated circuits.

1.3. TURN-OFF LOSSES

Free-wheel mode

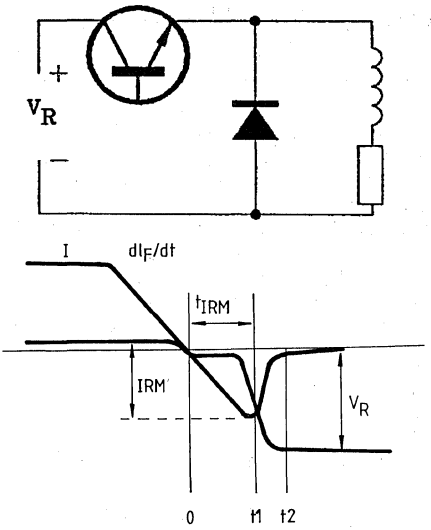
W_{OFF} is the energy dissipated in the rectifier during turn-off.

$$WFR = \int_{t_1}^{t_2} V dt \text{ (refer to figure 1)}$$

Low voltage (< 200V) fast rectifiers have a high internal capacity and the minority carriers have a very short life time. High voltage fast rectifier have a thicker N silicon layer and the minority carriers have longer life time and consequently different behaviour during the turn-off condition blocking state. (Higher I_{RM} and t_{IRM} - more damping).

Figure 1 : Fast Rectifier : the two turn-off modes.

a) Free-wheel Mode.



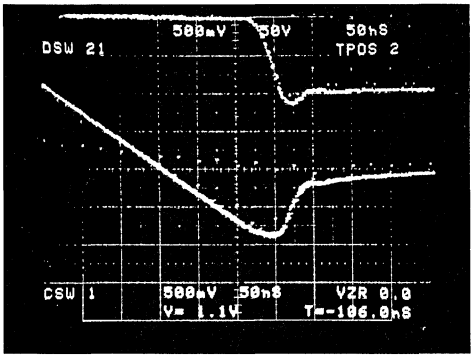
dI_F/dt FIXED BY THE TRANSISTOR (or by the external circuit)

LOW LOSSES IN THE RECTIFIER

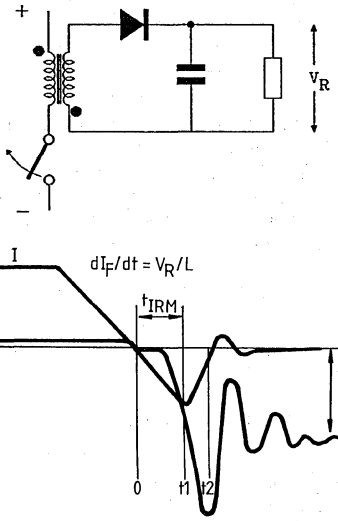
$W_{OFF} = K \cdot V_R \cdot I_{RM} \cdot T_{IRM}$

$(0.15 < K < 0.35)$

NO OSCILLATIONS AND OVERVOLTAGE



b) Rectifier Mode.



dI_F/dt FIXED BY THE INDUCTANCE

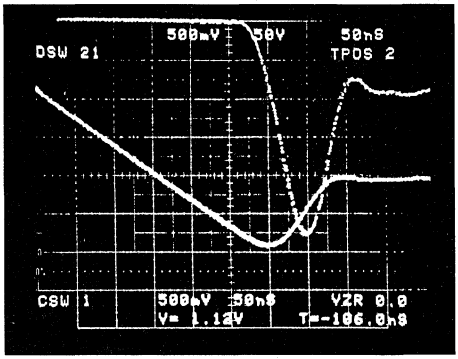
$dI_F/dt = V_R/L$

HIGH LOSSES IN THE RECTIFIER

$W_{OFF} = K \cdot V_R \cdot I_{RM} \cdot T_{IRM} + 1/2\ L_J{}^2{}_{RM}$

When a snubber is used some of the energy is dissipated in the snubber.

ALWAYS OVERVOLTAGE AND OSCILLATIONS IN SOME CONDITIONS



5A/div. 50V/div. 0.05µs/div.

BYT30 – 1000 – I_F = 3A – dI_F/dt = – 75A/µs – V_R = 100V – T_{CASE} = 25°C

According to the experimental results the turn-off energy loss $(W)_{FR}$ in the free-wheel mode can be written :

$$(W)_{FR} = K \times V_R \times I_{RM} \times t_{IRM} \quad (1)$$

$K^{(1)}$ is a constant that depends on the thickness of the N type silicon layer.

Max Voltage Rating (V)	200	400	800	1000	1200
K	0.12	0.14	0.22	0.28	0.35

Rectifier mode

Losses in this mode, $(W)_{REC}$, are the sum of the stored energy 1/2 L I_{RM}^2 and the recovery energy $(W)_{FR}$:

$$(W)_{REC} = (W)_{FR} + 1/2\ L\ I_{RM}^2 \quad (2)$$

In some cases, oscillations can occur. This depends on the damping due to the current tail effect after switch-off. When oscillations occur energy is dissipated during the oscillations partly in the rectifier and partly in the circuit. When snubbers are used a significant part of the energy is dissipated in the snubber.

2. PRACTICAL SWITCH-OFF BEHAVIOUR

The two cases, free-wheel mode and rectifier mode are simplified cases that are easy to simulate in a laboratory characterisation. In practical equipment there is always a possible overlap between the two theoretical modes, because :

1. No circuit is without parasitic inductances.
2. The rise time (or the fall time) of the switch is not infinitely fast when compared with the rate of change of current, dI_F/dt.

Experimental results show that in all cases the following formula can be used :

$$(W)_{OFF} = (W)_{FR} + 1/2\ L_S\ I_{RM}^2 \quad (3)$$

Where L_S = series inductance

This important relationship is a useful tool for the designer, giving him the main parameters that influence the turn-off energy.

N.B. : The following relationship (4) is only true for the pure rectifier mode.

$$(W)_{OFF} = Q_R \times V_R \quad (4)$$

Where Q_R = recovered charge

(1) K is experimental - Defined for SGS-THOMSON Microelectronics fast rectifiers.

Figure 2 : Rectifiers in Free Wheel Mode.

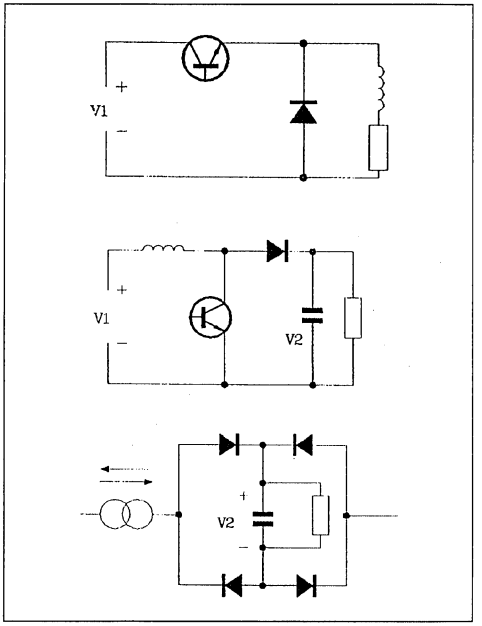


Figure 3 : Rectifiers in Rectifier Mode.

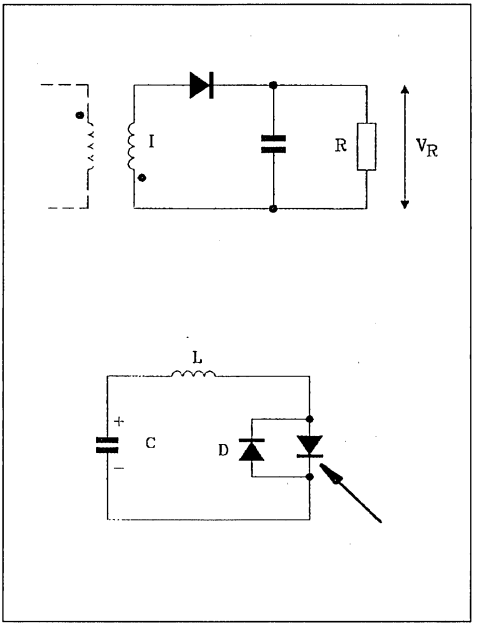
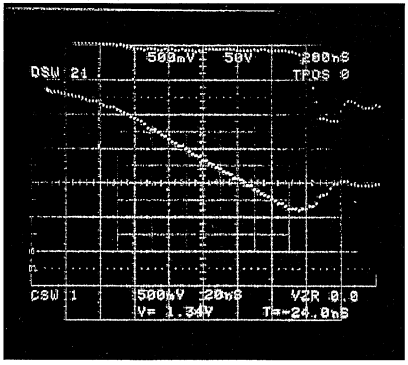
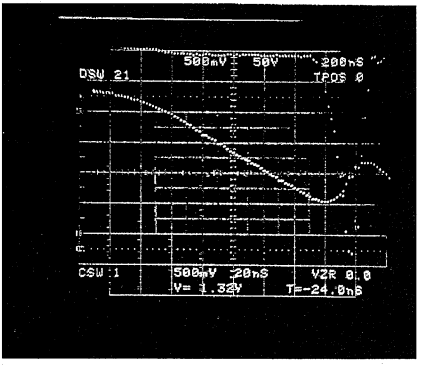


Figure 4 : Switch-off Behaviour of the Ultrafast BYT12-400V Rectifier (current rating 12A - voltage rating 400V).
Conditions : I_F = 13A dI_F/dt = – 150A/µs V_R = 100V T_{case} = 25°C.
In the case of rectifier mode : L = 0,6µH.
The turn-off lost energy calculated by the current and voltage is :
$(W)_{FR}$ = 3µJ free-wheel mode.
$(W)_{REC}$ = 10µJ rectifier mode.
The storage energy in the inductance is : 1/2 L I_{RM}^2 = 7.5µJ.

a) Free wheel mode.



b) Rectifier mode.



The use of this equation for a lot of practical circuits can be considered as a first approximation. It leads to over estimated losses, if the rectifier does not operate in pure "rectifier mode".

3. CHARACTERISTICS OF FAST RECTIFIERS

The characteristics of fast rectifiers are the result of a trade off between :

- Speed (I_{RM})
- Max voltage rating (V_{RRM})
- Forward voltage drop (V_F).

Example : 12A fast rectifiers.

V_{RRM}		200	400	800	1000
Type		BYW81	BYT12-400	BYT12-800	BYT12-1000
T_j = 100°C	I_{RM}(A)	1.8	3.7	6	7.8
dI_F/dt = – 50A/µs					
	t_{IRM}(µs)	0.05	0.075	0.160	0.200
V_F	(V)	0.66 + 0.0071	11 + 0.021	1.3 + 0.031	1.3 + 0.031

Operating conditions

I_{RM} increases with dI_F/dt (figure 5).

I_{RM} increases with T_j (figure 6).

The important points that emerge are :

1. High voltage fast rectifiers are not so fast as low voltage fast rectifiers, (comparing devices of equal current rating).
2. T_j and dI_F/dt have a strong influence on the reverse recovery current.

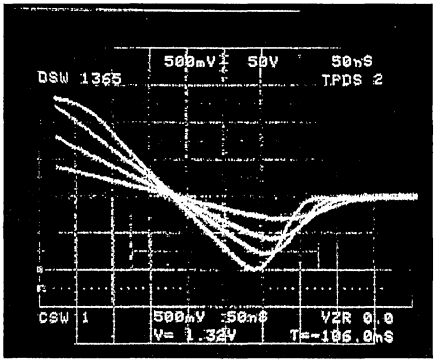
4. EXAMPLES

4.1. FLYBACK CONVERTER (figure 7)

The behaviour is as a pure rectifier ; the rectifier is driven by a current source, the inductor, L.

For a frequency less than 100kHz the switching losses are small in comparison to the conduction losses, because dI_F/dt defined by V_o/L is always small, (see table figure 7).

Figure 5 : Switch-off Behaviour of the Fast Rectifier BYT12P 1000 (current rating 12A voltage rating 1000V). Influence of the dI_F/dt.



5A/div, 50ns/div, Tj = 25°C

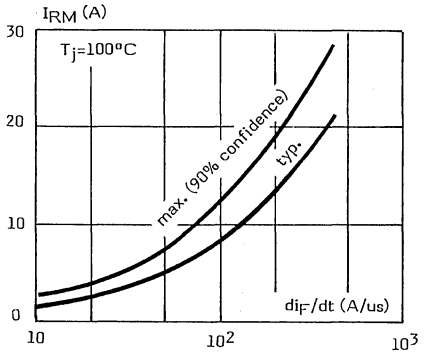
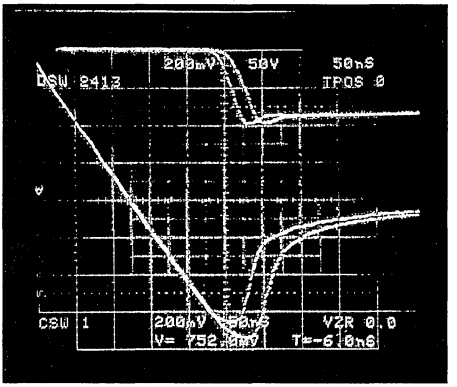
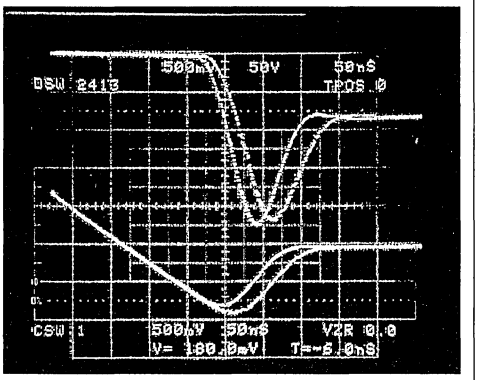


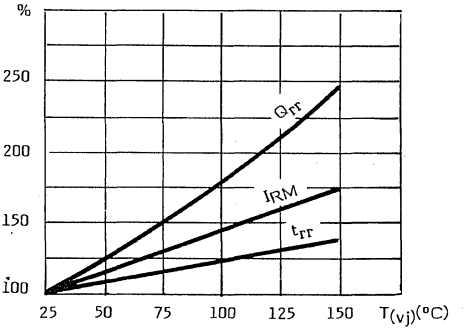
Figure 6 : Switch-off Behaviour of the Fast Rectifier BYT12 1000 Influence of T_j. One Curve $T_j = 25°$, one curve $T_j = 60°$.



100V/C, 2A/div, 50ns/div
Free-wheel mode



100V/C, 2A/div, 50ns/div
Rectifier mode



How can the designer reduce the losses ?

1. The ratio I peak/I_{AVG}, is very unfavourable in this type of circuit. It is essential when the peak voltage is less than 200V that the "high efficiency ultra fast" family which have very low conduction losses are used. When the peak voltage is greater than 200V one solution is to use a rectifier with higher current rating.

Example :

In the same circuit at 12A with :

- BYT12-800 : conduction losses = 7.6W, a 12A rectifier.
- BYT30-800 : conduction losses = 6W, a 30A rectifier

2. Reduce the junction temperature. If Tj is decreased from 100 to 75°C the switching losses are reduced by 20%.

4.2. SMALL CURRENT RECTIFIER (figure 8)

A transformer with a leakage inductance measured on the secondary side L_S = 1µH supplies a fast diode D. The average output current is 0.8A and the output voltage is 48V.

The designer wants to use the popular diode BA157. This is not possible because the total power dissipation is 1.15W at 40kHz. At this frequency he can only use a popular 2A current rated diode (for 0.8A rectified current) and at 200kHz there is no solution with popular diodes (see table in figure 8).

How can the designer reduce the losses ?

1. Choose a diode in the "high efficiency family". For example he can use the BYW100 for 40kHz to 200kHz, (see table figure 8).
2. Reduce the leakage inductance : with a leakage inductance L_S = 0.1µH, BY218 at 200kHz (1.24W, ΔT_j = 93°C).

4.3. FULL WAVE OUTPUT RECTIFIER

There are two different full wave rectifying circuits.

4.3.1. VOLTAGE SOURCE - CURRENT OUTPUT

Current and voltage behaviour are indicated in figure 9. The inductance L_S is the leakage inductance of the insulation transformer.

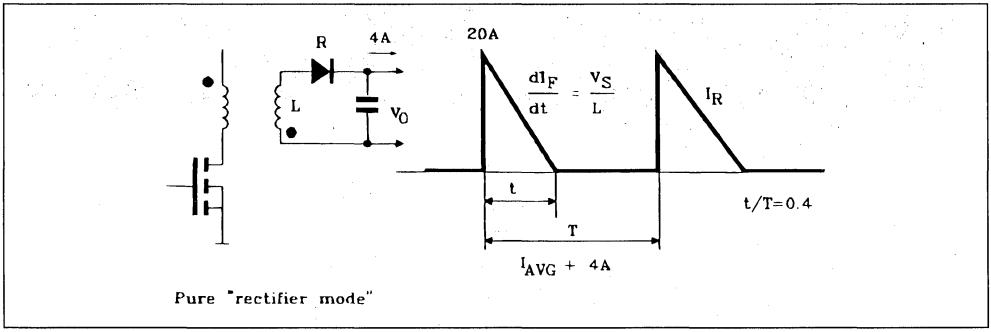
The 4 rectifiers operate in an intermediate mode between "free wheel" and "rectifier", because there are some 1/2 L_S I_{RM}^2 losses.

4.3.2. CURRENT SOURCE - VOLTAGE OUTPUT (figure 10).

In this circuit, each rectifier operates in "free wheel" mode. The series inductance does not introduce additional losses. (This assummes there is no parasitic inductance between the rectifiers and the capacitor C).

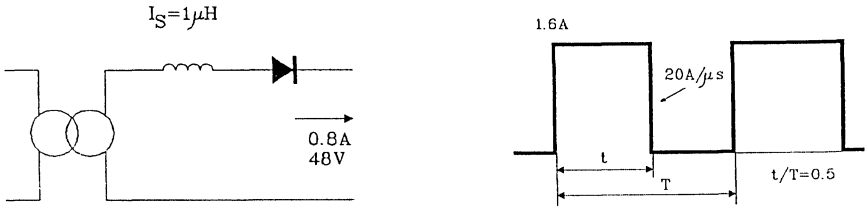
How can the designer reduce the losses ?

Figure 7 : Flyback Rectifier Output Average Current 4A.
Below 100kHz the switching losses are negligible, in comparison with the conduction losses. The reason is limited dI_F/dt, consequently limited I_{RM}.



V_O (V)	12	48	100
Rectifier	BYW81-100 "High Efficiency"	BYT12-400	BYT12-800
Conduction Losses (W)	3.2	6	7.6
Switching Losses a 50kHz (W)	0.006	0.05	0.81
Switching Losses a 200kHz (W)	0.05	0.5	5.5

Figure 8 : The Popular Diodes BA157 – BY218 are not Fast Enough for High Frequency Rectifying. The BYW100 is well adapted.



DIODE	BA157 Popular	BY218 Popular	BYW100-200 High Efficiency
I_{RM} a 100°C dI/dt = – 20A/μs (A)	2.8	2.8	0.75
t_{IRM} a 100°C dI/dt = – 20A/μs (A)	0.14	0.14	0.05
$(W)_{FR}$ (μJ)	2.08	2.08	0.01
1/2 L_S I^2_{RM} (μJ)	3.9	3.9	0.28
Conduction Losses (W)	0.944	0.744	0.592
Switching Losses a 40kHz (W)	0.2	0.2	0.012
Switching Losses a 200kHz (W)	1.3	1.3	0.06
Total Diode Losses a 40kHz (W)	1.15	0.44	0.6
Δ Tj a 40kHz (°C)	115°	71°	60°
Total Diode Losses a 200kHz (W)	1.97	1.77	0.65
Δ Tj a 200kHz (°C)	197°	132°	65°

a) Voltage source - current output
Reduce the transformer leakage inductance. Table of figure 11 shows that in the case of the 400V 10A 200kHz bridge circuit the suppression of the inductance L_S can save 4 x 16.5W = 66W. Replace in the same circuit the high voltage fast rectifier BYT12-600 by 3 "high efficiency" BYW81-200 in series (see figure 12 - table). The total losses decrease from 186W to 58W. This result is very important as it shows it is more efficient to use several "high efficiency" ultra fast rectifiers instead of a single high voltage one for high frequency operation.

b) Both
Use of sinusoidal current (resonant converter) instead of rectangular waveforms. Figure 11 shows that for the same conditions (400V - 10A - 200kHz) the switching losses with a sinusoidal current are only 4 x 7.5 = 30W (4 x 22 = 88W with rectangular wave forms).

4.4. STEP UP CONVERTER

The rectifier operates in free wheel mode. The main losses in this case occur in the transistor during the turn-on (similar to the step down converter). Figure 13 shows that with 600V output at 40kHz, if the rectifier switching losses are reasonable, the transistor turn-on losses are too high.

How can the designer reduce these turn-on losses ? (fig. 13).

a) Decrease the rectifier junction temperature by more efficient cooling.
If the BYT12-800 junction temperature decreases from 100 to 70°C, the transistor turn-on losses decrease from 39.5W to 33W.

b) To replace one BYT12-800 by 4 high efficiency BYW81-200 in series. The total balance is a reduction in losses from 39.5 to 16.6W in the transistor with same losses in the rectifier.

IN SUMMARY

Two major actions reduce switching losses caused by fast recovery rectifiers :

1. APPROPRIATE CHOICE OF COMPONENT
   - The fastest rectifier compatible with the peak voltage in the application.

- If the peak voltage V_R exceeds 400V the designer must analyse carefully the switching losses :
  - These losses are proportional to $I^2_{RM} \times V_R$.

A 800V fast rectifier has an I_{RM} approximately two times higher than a 400V fast rectifier (same current rating).

Figure 9 : Voltage Source, Output Current Full Bridge Circuit.

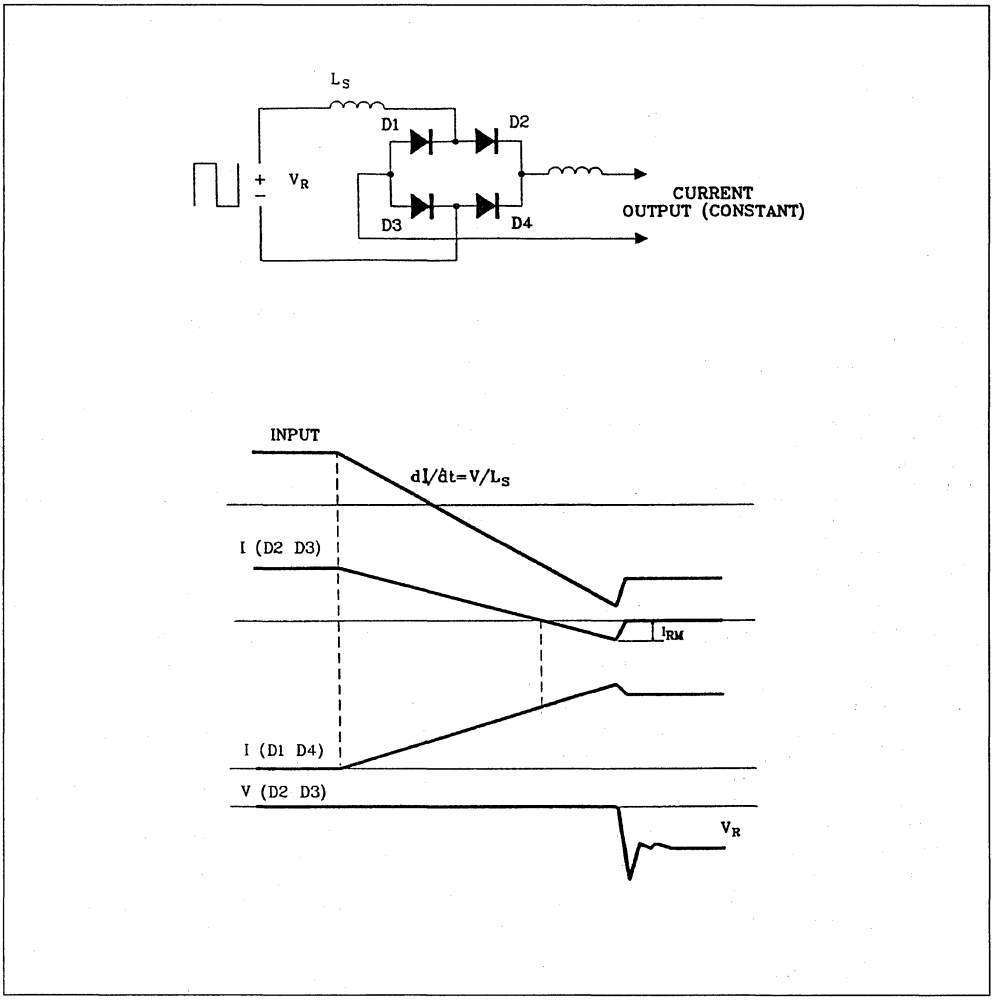
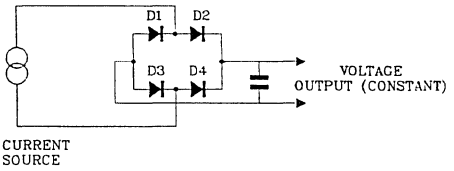
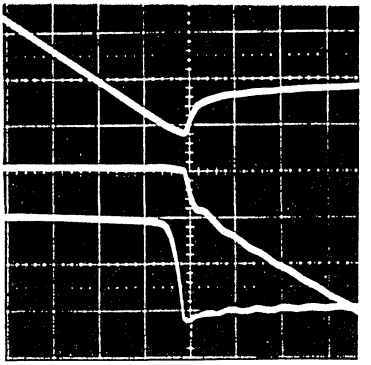


Figure 10 : Current Source, Output Voltage Full Bridge Circuit.





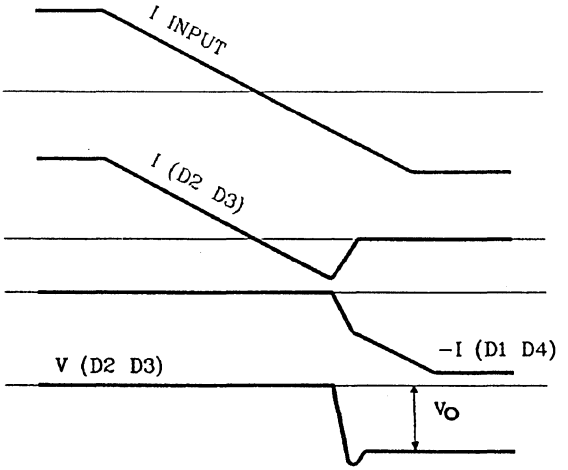
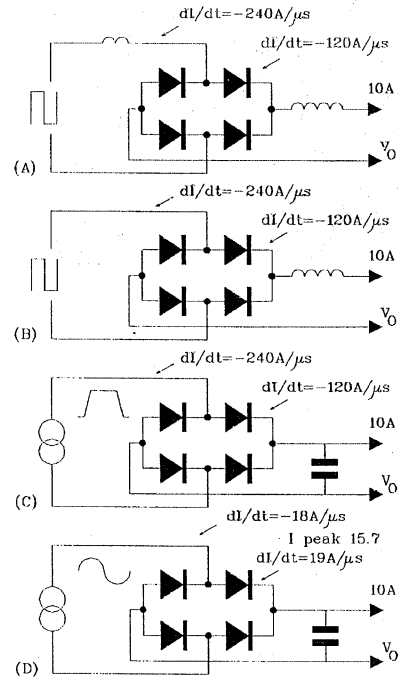


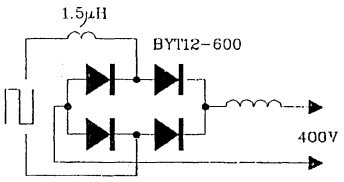
Figure 11 : Switching Losses (per leg) in a full Wave 200kHz Bridge Circuit. Output 10A.
In case of voltage source, current output, the (leakage) inductance L_S introduces LsI^2_{RM} losses.
In case D, the losses are smaller (6 x 4 = 24W instead of 22 x 4 = 88W) because dI/dt is smaller, consequently I_{RM} is smaller.

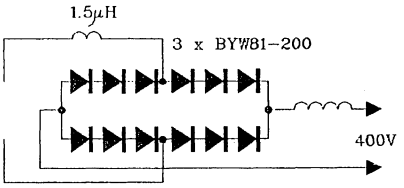
L_S = 0.5µH (48V)
1µH (200V)
1.5µH (400V)



V_0	48	200	400
Rectifier	BYW81-100	BYT12-300	BYT12-600
200kHz			
	0.76W	5.6W	38.5W
	0.16W	2W	22W
	0.16W	2W	22W
	0.04W	0.6W	6W

Figure 12 : Switching Losses (per leg) in the Full Wave 400V 200kHz Bridge Circuit with two Different "rectifiers".
Replacing the high voltage BYT12 – 600 rectifier by 3 "high efficiency" ultra fast BYW81 – 200 in series reduces the total losses dramatically. This is why the I_{RM} from BYW81 is very low and the voltage drop of this high efficiency rectifier is very low.

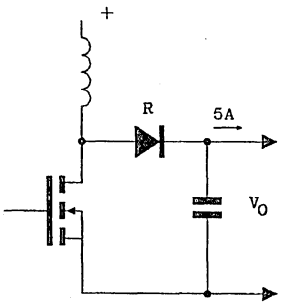


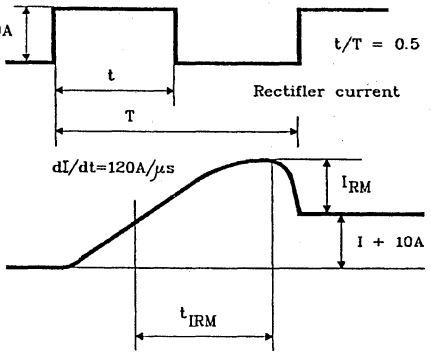


Rectifier	BYT12-600	3xBYW81-200
Conduction Losses (W)	8	11
Switching Losses (W)	38.5	3.5
Total Losses per Leg (W)	46.5	14.5

F = 200kHz
V_0 = 400V
I_{AVG} = 10A
dI_F/dt = – 120A/µs
t/T = 0.5

Figure 13 : In the Step-up (or step down) Converter the Majority of Losses Occur in the Transistor, Specially when a High Voltage Rectifier is used.
In some case replacing a high voltage rectifier by several faster rectifiers in series (and consequently with a lower voltage rating) can minimize the total losses despite the increase of the rectifier conduction losses.





Transistor turn-on current

$$(W)_{ON} = \frac{V_R}{2}\left[\frac{I}{dI/dt} + (I + I_{RM})\, t_{IRM}\right]$$

Figure 13 (continued).

V_0	48	300	600	600
Rectifier	BYW81-100	BYT12-400	BYT12-800	4 x BYT81-200
(dI_f/dt = 120A/µs) I_{RM} (A) (T_j = 100°) t_{IRM} (µs)	3.8 0.04	6 0.06	10.5 0.12	3.8
Rectifier Conduction Losses (W)	3.65	6.5	8	14.6
Rectifier Switching Losses a 40kHz (W)	0.04	0.6	6.7	0.5
Total Rectifier Losses a 40kHz (W)	3.7	7.1	14.7	15.1
Transistor Turn-on Losses a 40kHz (W)	1.32	1	0.7	39.5

The rectifier voltage drop increases with the rating voltage.

Example : BYW81 "high efficiency" 200V rating V_F = 0.85V (max).

BYT12-600 600V rating V_F = 1.8 (max).

IMPORTANT CONSEQUENCES :

If the switching frequency is greater than 40kHz in many cases it will be more efficient to replace one high voltage (600 - 800 - 1000V) rectifier by a series of ultrafast rectifiers (200V or 400V). Despite the increase of conduction losses, a dramatic reduction of switching losses results in a decrease in the total losses.

2. OPTIMAL OPERATING CONDITIONS

2.1. In many cases parasitic inductance gives additional losses. A reduction of those parasitic inductances L_S decreases not only the voltage spikes but also the switching losses.

2.2. Junction temperature plays an important rôle. The switching losses are approximately proportional to Tj. Improving the rectifier cooling is very important for all high frequency rectifiers.

2.3. For full wave rectifying circuits, with an isolation transformer the switching losses are always lower in case of :

Current source → rectifying → voltage source

than :

Voltage source → rectifying → current source

because the impedance due to the transformer leakage inductance is integrated in the current source, and does not play any part in the additional losses.

2.4. The use of the resonant circuit with sinusoidal current waveforms results in a significant reduction in the switching losses due to the limited dI_F/dt or to the smaller V_R re-applied voltage.

CONCLUSION

Reducing the switching losses in high frequency converters is team work.

The manufacturer has improved the fast recovery rectifier characteristics. The designer has now some tools to analyse, with a greater accuracy, the rectifier behaviour and choose the optimal solution in order to minimize the losses.

REFERENCE

[1] "Switching behaviour of fast diodes in the converter circuits" - p.63 to 78 in the hand book SGS-THOMSON Microelectronics "Transistors & Diodes in Power Processing".

SMART POWER DEVELOPMENT SYSTEM

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

PC-BASED DEVELOPMENT SYSTEM CUTS DESIGN TIME OF SMART POWER IC APPLICATIONS

by Thomas L. Hopkins

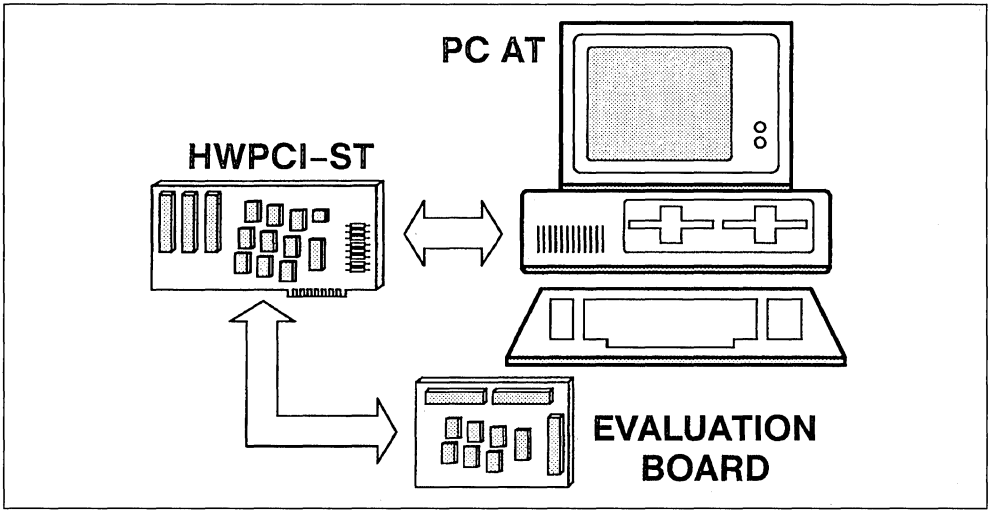
A Smart Power Development System allows the designer to evaluate a smart power device in the final application, such as emulator systems allows designers to evaluate and debug microprocessors.

As smart power integrated circuits become more complex they are approaching the realm where they can be considered power peripheral chips. These new devices can no longer be evaluated with a simple bench set up using a few switches and a function generator. Before the device will operate in an application, one or more registers must be programmed to set the operating conditions of the device. To speed development of applications using these devices a PC based system, the Smart Power Development System, has been developed. The SPDS allows the user to quickly develop and evaluate the device performance in a real application. This paper discusses the SPDS and shows a typical application for a stepper motor drive circuit, the L6223A.

The current generation of smart power integrated circuits contain more logic than their predecessors and many, like the L6280 and L6223A, contain one or more registers that must be programmed for the device to operate. This adds a new dimension to the users task who must now develop software to drive the devices before he can start to evaluate the device operation. In addition such tasks as calculating the power dissipation and required heat sink for a power integrated circuit is a more complicated task than for discrete devices.

To assist the user in evaluating such devices the Smart Power Development System (SPDS) was developed. This PC based system consists of three parts: 1) a general purpose interface card that interfaces to the PC bus, 2) a dedicated printed circuit board for each device supported, and 3) a dedicated software package for each device supported. The block diagram of the SPDS is shown in figure 1.

Figure 1: PC-Based SPDS



PC INTERFACE

To allow the PC to easily drive a variety of applications, a general purpose interface card was needed. The interface card chosen, similar to the Burr-Brown PCI 2000 Series, provides 32 I/O lines, 4 counter/timer channels, and a rate generator, as shown in figure 2.

The 32 I/O lines are general purpose parallel lines that may be programmed, in groups of 8, as either output or input lines. The 32 I/O lines plus their associated control registers are mapped, as eight bit registers, into the user address space of the PC and are easily addressed by the application program. In the SPDS system these 32 lines are used as parallel outputs to drive the dedicated application board.

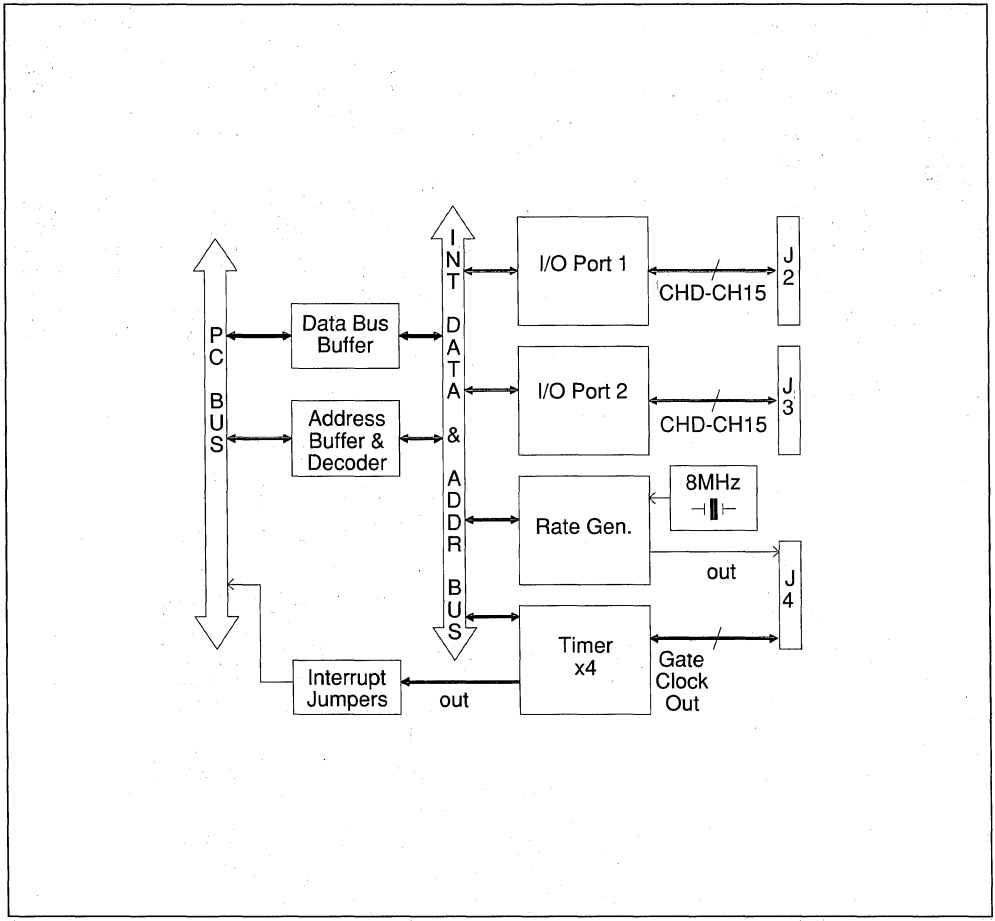
The rate generator provides a stable timebase for operation of the system. The frequency of the rate generator output is given by the equation:

$$F_{out} = \frac{8MHz}{(N_1 \cdot N_2)}$$

where N_1 and N_2 are integers between 2 and 65535. In this configuration, the output frequency can then range from 2 MHz to approximately .002 Hz. This clock signal is used by the four counter timer channels that provide the variable step rate timing used in stepper motor applications or the period of output patterns in pattern generator type applications.

This flexible configuration allows the PC interface to be independent of the device being evaluated and provides a general purpose interface that can drive many types of applications.

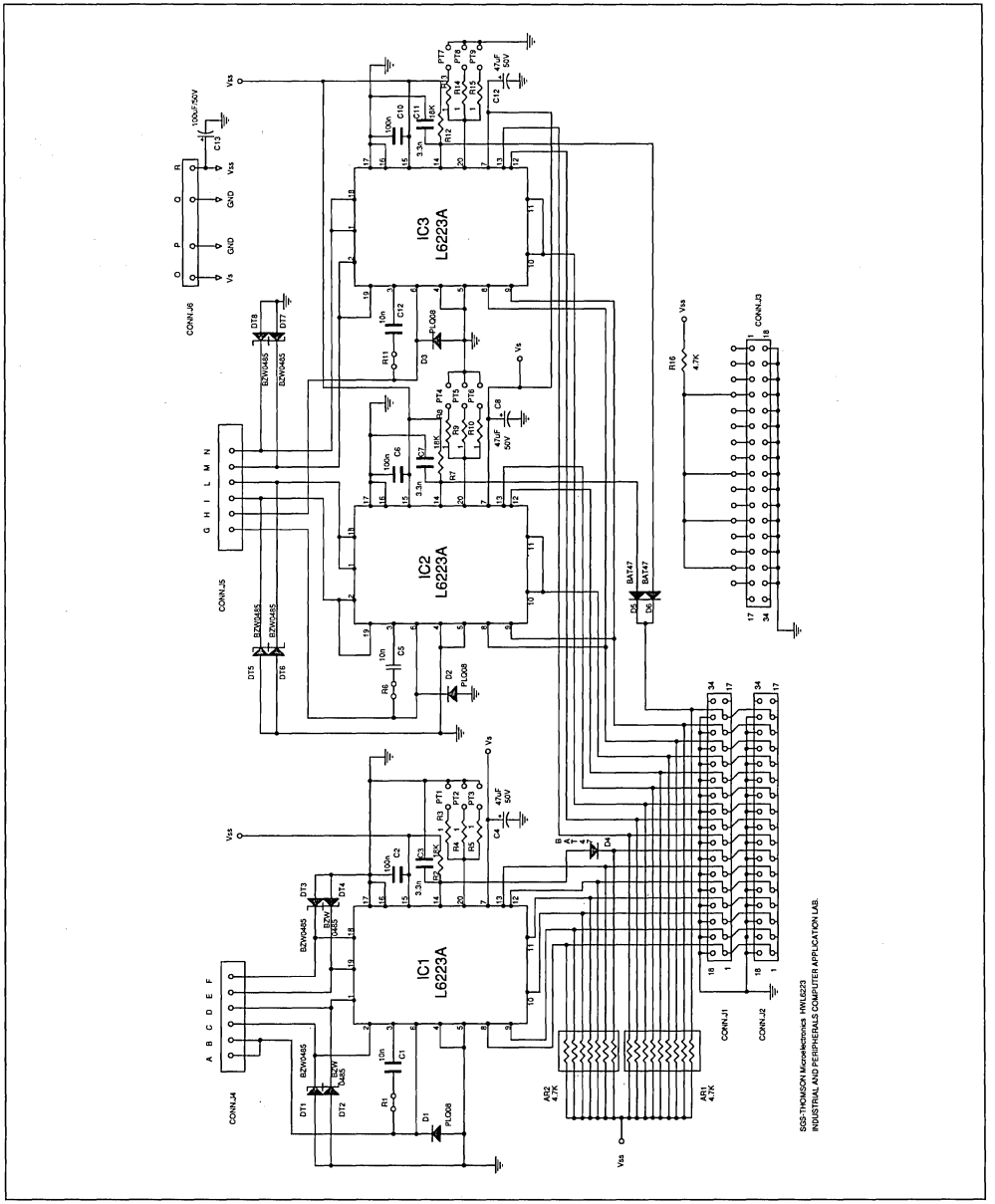
Figure 2: SPDS Interface Card



DEDICATED HARDWARE

Each device, or family of devices, supported by the SPDS has a dedicated application board that connects to the PC interface card and includes the dedicated circuitry around the evaluation device. In the case of the L6223A the dedicated board includes two configurations for the L6223A driving a unipolar stepper motor, a single device application and a dual device application. The schematic diagram for the L6223A Dedicated Board is shown in Figure 3.

Figure 3: Dedicated Board for L6223A



This allows the user to choose the configuration that best suits his application depending on the current level required by the motor.[2] The software then allows the user to select which of the two implementations will be driven for evaluation.

Other dedicated boards support devices in bipolar stepper motor driver applications, DC motor driver applications, and solenoid driver applications.

SOFTWARE

Each of the SPDS systems includes a software package dedicated specifically to the devices. Although the features vary depending on the application and the specific devices, the L6223A package is typical. The L6223A package includes: 1) calculation of the acceleration and deceleration ramps for a stepper motor, 2) a driver routine for real time operation and 3) a simulation package that simulates the thermal behavior of the device or devices.

ACCELERATION AND DECELERATION RAMPS

The acceleration/deceleration ramp section the program is unique to step motor applications. This routine calculates the step timing required to raise the step motor from zero up to the final speed. The calculation is made from the mechanical characteristics of the application.

The required inputs include the characteristics of the motor, specifically the static Torque (T_{stat}), the slope of the Torque vs Speed curve (T_{slope}) and the number of steps per revolution. The torque characteristics for a typical stepper motor are shown in Figure 4. In the simple model for a stepper motor the torque decreases approximately linearly as the speed increases from zero up to the maximum motor speed where the Torque falls to zero.[1] This curve can be approximated by a straight line having a static Torque (T_{stat}) and a slope (T_{slope}) as shown in Figure 4. Here the approximation for the torque curve allows for a Torque utilization factor of less then unity.[1] In addition to the motor characteristics the program needs the mechanical characteristics of the system, as referred to the motor shaft. The two required values are the frictional Torque (T_{fric}) and the total Inertia (J_{tot}). From these values the program calculates the period of each step during the acceleration ramp. These values are then saved and used by the real time program to drive the motor.

Figure 4: Typical stepper motor torque characteristics

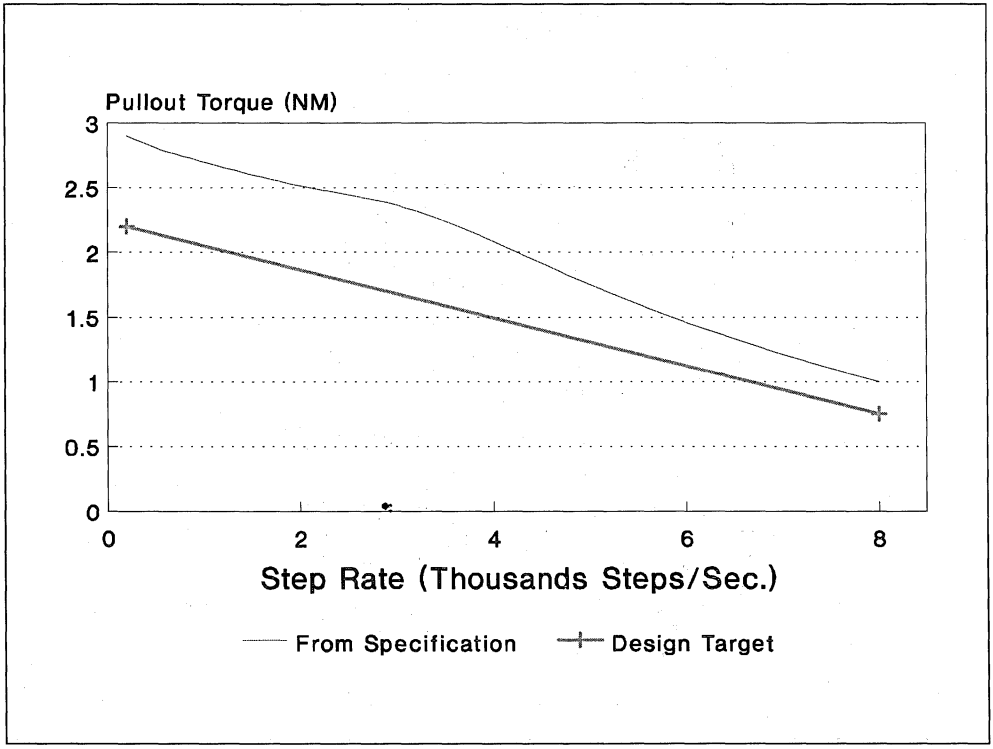


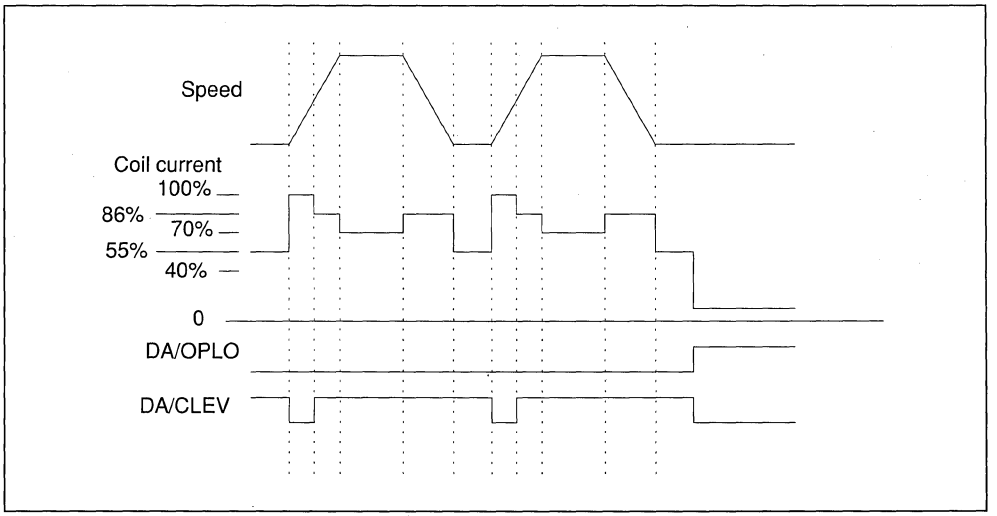
Figure 5: SPDS entry screen

```
TEXT MOVEMENT    Number 1  of 2    Filename: DEFTEST.DIM

Rotation sense  ( FW / BW )                                  FW
Acceleration current    (100% 85% 70% 55% 40%)               100
Frequency     ( 10 or 20 Khz )                               20
Number of steps before the intermedia current                10
Intermedia current      (100% 85% 70% 55% 40%)               85
Frequency     ( 10 or 20 Khz )                               20
Number of steps of constant speed                            199
Costant speed current   (100% 85% 70% 55% 40%)               55
Frequency     ( 10 or 20 Khz )                               20
Deceleration current    (100% 85% 70% 55% 40%)               70
Frequency     ( 10 or 20 Khz )                               20
Stand by current ( OPen or CLose loop )                      CL
Stand by current          100% 85% 70% 55% 40%               40
Frequency     ( 10 or 20 Khz )                               20
Half or Full   ( H / F )                                     F
Time of stand by          (m.sec)                            200

        F1 to next movement          ESC to go back
```

REAL TIME OPERATION

One major advantage of the SPDS is the ability to operate the devices in a real time application without having to first write a driver routine. In the real time operation section of the program the user defines a sequence of movements and the motion profile and operating parameters for each movement. This is done using a simple text entry screen, as shown in Figure 5. Each movement is divided into five segments, as shown in Figure 6. Using the motion text entry screen, the user may define the operating conditions of the driver chip for each segment of the movement. The entry screen allows the user to select one of five current levels and the chopping frequency, both of which are selected by programming the internal shift register in the L6223A [3], for each segment of the movement.

Figure 6: Stepper movements



The entry screen also allows the user to define the number of steps in the first segment and the third segment of the movement. The number of steps in the second and fourth segment of the movement are defined by the acceleration ramp and deceleration ramps being used.

The final segment of the movement is the standby period, which is really the period where there is no movement between two movements. The user is allowed to select the period and operating conditions during standby. Utilizing the programmability of the L6223A, the user may select either open loop or closed loop operation during this time as well as the current level and the chopping frequency.

The user may define any number of movements in a sequence and then set the parameters of each movement. Once this definition is completed, the SPDS will continually execute the sequence programmed in real time. In the execute mode the SPDS displays some of the operating parameters of the system, as shown in Figure 7 and 11. During the execution the user may modify the step timing of either the acceleration or deceleration ramps and observe the affect on the mechanical behavior of the system.

Once the user is satisfied with the system operation all of the values of the acceleration ramp, deceleration ramp and motion profile can be saved on the disk for future use.

SAFE (and SAVE) DESIGN BY SIMULATION

The final section of the SPDS system allows the user to evaluate the thermal behavior of the device in the application. In this section the movement is simulated based on the average velocity, as shown in Figure 8. Using the input electrical parameters of the application and motor, the program calculates the chopping duty cycle and the effect on power dissipation due to the step rate. To these values are added the quiescent losses, which are assumed to be constant, to get find the power dissipation in the device. The program also accounts for variation in the R_{DSon} with die temperature.

The simulation outputs two representations of the information. The first, shown in Figure 9, shows the power dissipation and required thermal impedance from the junction to ambient ($R_{thj\text{-}a}$) to limit the maximum junction temperature to a specified value versus the peak coil current (I_p). For

Figure 7: Operating parameter display

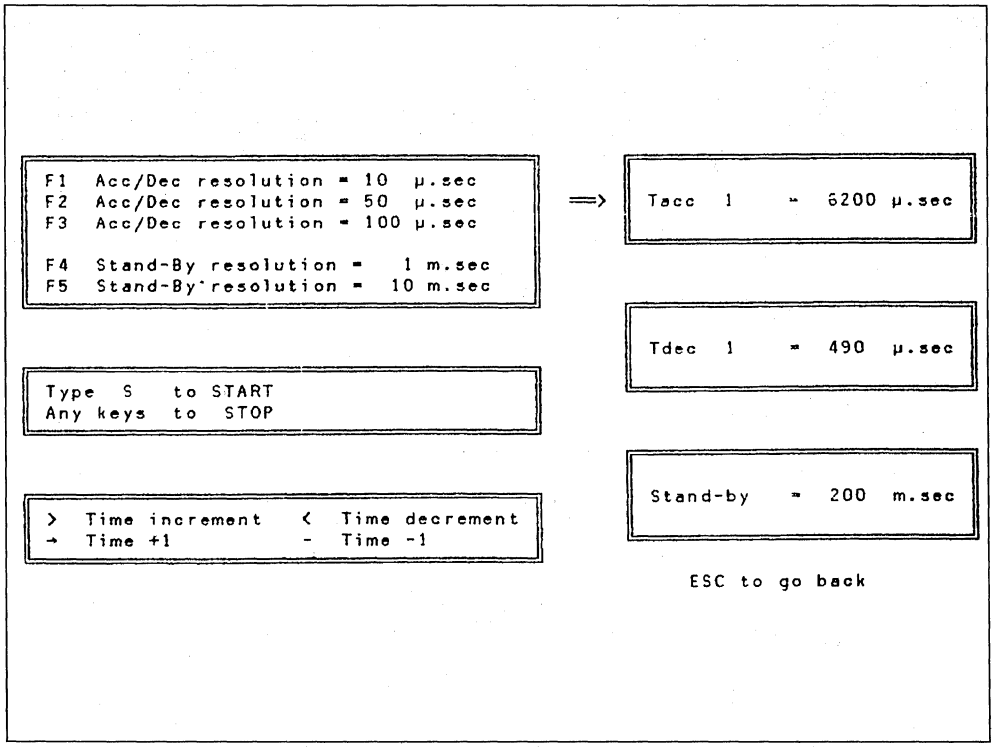


Figure 8: Stepper motor movement simulation

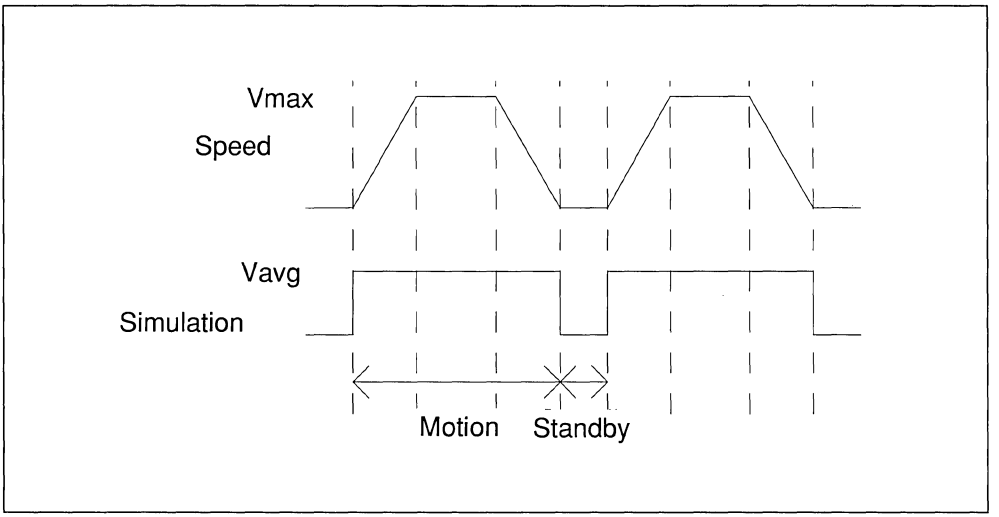
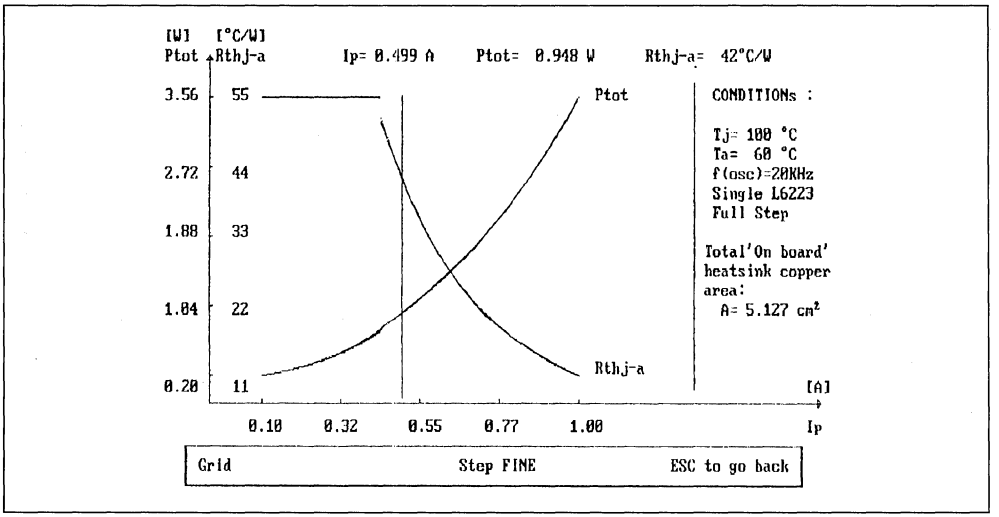


Figure 9: Power dissipation and required thermal impedance



required values of thermal impedance less than 55°C/W (the thermal impedance of the package in free air) the power dissipation is calculated assuming a constant thermal impedance of 55°C/W. For any given value of current, selected by moving the cursor, the calculated value for P_d and $R_{thj\text{-}a}$ are shown on the top of the graph. The program also calculates the number of square inches of copper required on the printed circuit board to achieve the required thermal impedance, for values that are achievable in this manner. When the power dissipation exceeds the level that may be dissipated in this configuration, a message that an external heat sink is required is displayed.

The second output (see fig. 10) of the simulation program calculates the power dissipation and die temperature assuming constant values of $R_{thj\text{-}a}$. For this simulation, three values of thermal impedance are chosen; the thermal impedance of

Figure 10: Power dissipation and die temperature

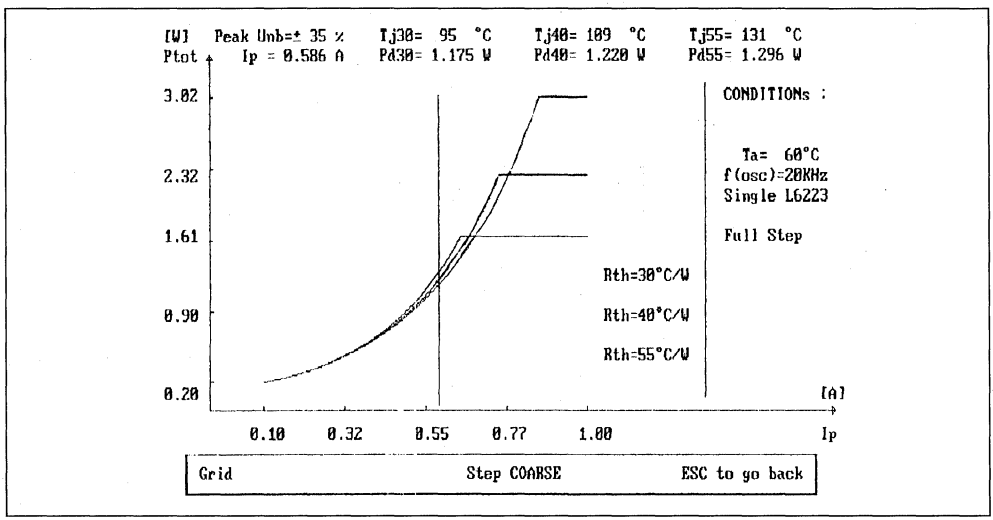
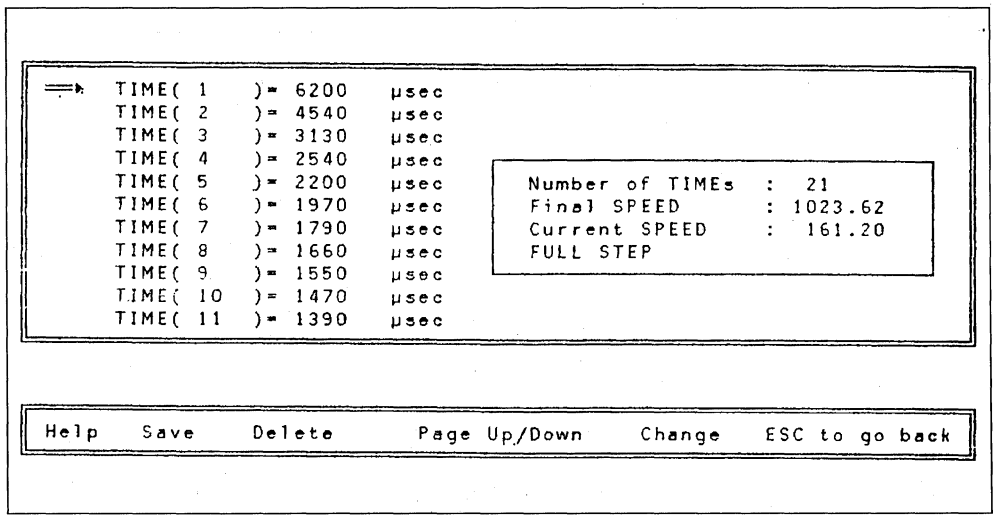


Figure 11: Acceleration ramp timing



the package in free air (55°C/W), the minimum practical value of thermal impedance using only copper on the PCB (40°C/W) and the minimum practical value using an external clip on heat sink (30°C/W).[4] Each of the graphs are interrupted when the die temperature exceeds 150°C, the maximum rating of the device. When the current level selected by the cursor would cause the device to exceed the maximum rating, a message is displayed that the device will go into thermal shut down at that level.

CONCLUSION

The Smart Power Development System allows the user to quickly evaluate a smart power device in the final application, much as emulator systems allow user to evaluate and debug microprocessors. The system contains two key components that allow the user to 1) quickly define the operation of the device and evaluate it in a real time application and 2) verify that the device will operate within the its safe operating limits. For compli-

cated devices that require the user to program one or more internal registers before the device will operate, the system can greatly reduce the time required to evaluate the system, without requiring the user to write any specific software.

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1)A. Leenouts, The Art and Practice of Step Motor Control, Intertec Communications Inc., Ventura Ca., 1987

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3)"L6223A Data Sheet", Industrial and Computer Peripheral ICs databook 2nd Edition, 1992, pp 449 to 479.

4)T. Hopkins, "Designing with Thermal Impedance" Proceedings of the Fourth Annual IEEE Semiconductor Thermal and Temperature Measurement Symposium, San Diego, Ca., Feb. 1988.

STEPPER MOTORS

STEPPER MOTOR DRIVER CONSIDERATIONS COMMON PROBLEMS & SOLUTIONS

by Thomas L. Hopkins

This note explains how to avoid same of the more common pitfalls in motor drive design. It is based on the author's experience in responding to enquiries from the field.

INTRODUCTION

Over the years while working with stepper motor users, many of the same questions keep occurring from novice as well as experienced users of stepper motors. This application note is intended as a collection of answers to commonly asked questions about stepper motors and driver design. In addition the reference list contains a number of other application notes, books and articles that a designer may find useful in applying stepper motors.

Throughout the course of this discussion the reader will find references to the L6201, L6202 and L6203. Since these devices are the same die and differ only in package, any reference to one of the devices should be considered to mean any of the three devices.

Motor Selection (Unipolar vs Bipolar)

Stepper motors in common use can be divided into general classes, Unipolar driven motors and Bipolar driven motors. In the past unipolar motors were common and preferred for their simple drive configurations. However, with the advent of cost effective integrated drivers, bipolar motors are now more common. These bipolar motors typically produce a higher torque in a given form factor [1].

Drive Topology Selection

Depending on the torque and speed required from a stepper motor there are several motor drive topologies available [5, chapter3]. At low speeds a simple direct voltage drive, giving the motor just sufficient voltage so that the internal resistance of the motor limits the current to the allowed value as shown in Figure 1A, may be sufficient. However at higher rotational speeds there is a significant fall off of torque since the winding inductance limits the rate of change of the current and the current can no longer reach it's full value in each step, as shown in Figure 2.

Figure 1: Simple direct voltage unipolar motors drive.

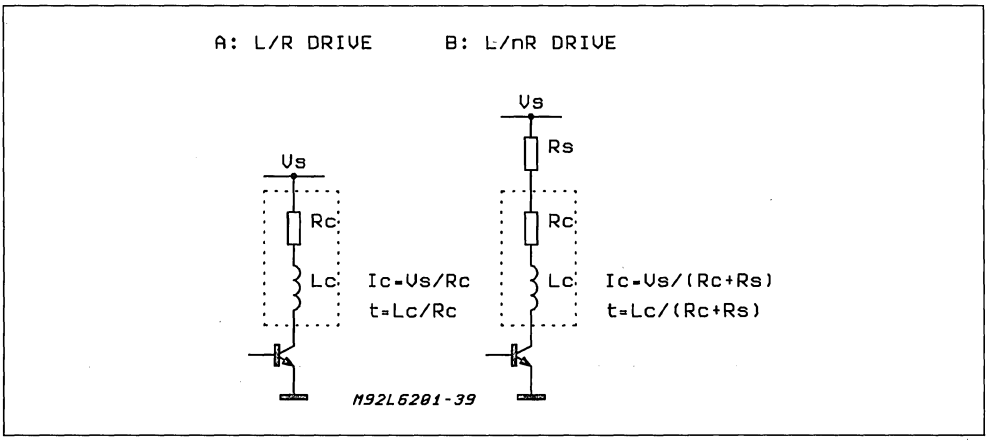
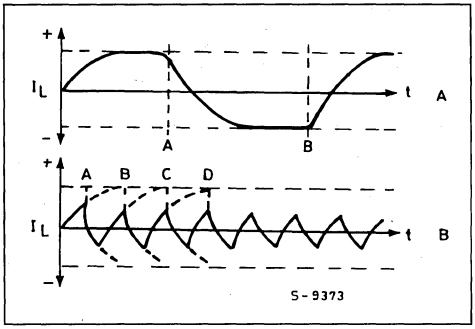


Figure 2: Direct voltage drive.
A - low speed;
B - too high speed generates fall of torque.



One solution is to use what is commonly referred to as an L/nR drive (Fig. 1B). In this topology a higher voltage is used and the current limit is set by an external resistor in series with the motor winding such that the sum of the external resistance and the internal winding resistance limits the current to the allowed value. This drive technique increases the current slew rate and typically provides better torque at high rotational speed. However there is a significant penalty paid in additional dissipation in the external resistances.

To avoid the additional dissipation a chopping controlled current drive may be employed, as shown in Figure 3. In this technique the current through the motor is sensed and controlled by a chopping control circuit so that it is maintained within the rated level. Devices like the L297, L6506 and PBL3717A implement this type of control. This technique improves the current rise time in the motor and improves the torque at high speeds while maintaining a high efficiency in the drive [2]. Figure 4 shows a comparison between the winding current wave forms for the same motor driven in these three techniques.

Figure 3: Chopper drive provides better performance.

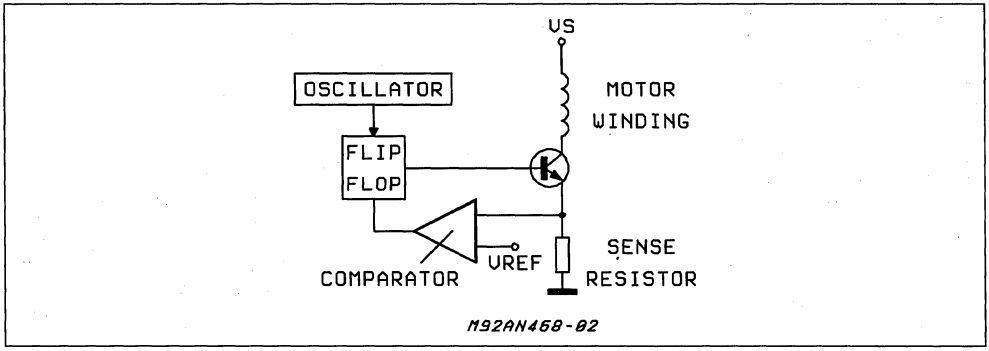
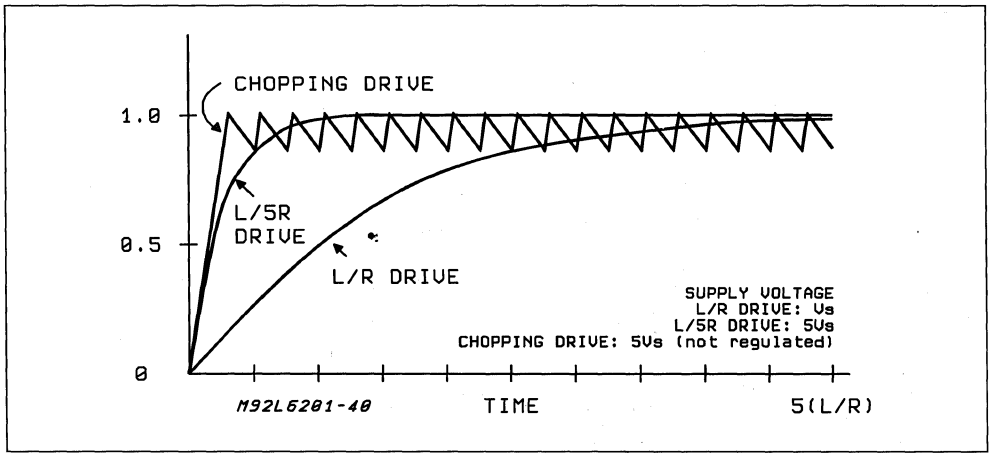


Figure 4: Motor current using L/R, L/5R and chopper constant current drive.



In general the best performance, in terms of torque, is achieved using the chopping current control technique [2]. This technique also allows easy implementation of multiple current level drive techniques to improve the motor performance. [1]

Driving a Unipolar Motor with the L298N or L6202

Although it is not the optimal solution, design constraints sometimes limit the motor selection. In the case where the designer is looking for a highly integrated drive stage with improved performance over previous designs but is constrained to drive a unipolar wound (6 leaded) motor it is possible to drive the motor with H-Bridge drivers like the L298N or L6202. To drive such a motor the center tap of the motor should be left unconnected and the two ends of the common windings are connected to the bridge outputs, as shown in Figure 5. In this configuration the user should notice a marked improvement in torque for the same coil current, or put another way, the same torque output will be achieved with a lower coil current.

A solution where the L298N or L6202 is used to drive a unipolar motor while keeping the center connection of each coil connected to the supply will not work. First, the protection diodes needed from collector to emitter (drain to source) of the bridge transistors will be forward biased by the transformer action of the motor windings, providing an effective short circuit across the supply. Secondly the L298N, even though it has split supply voltages, may not be used without a high voltage supply on the chip since a portion of the drive current for the output bridge is derived from this supply.

Selecting Enable or Phase chopping

When implementing chopping control of the current in a stepper motor, there are several ways in which the current control can be implemented. A bridge output, like the L6202 or L298N, may be driven in enable chopping, one phase chopping or two phase chopping, as shown in Figure 6. The L297 implements enable chopping or one phase chopping, selected by the control input. The L6506 implements one phase chopping, with the recirculation path around the lower half of the bridge, if the four outputs are connected to the 4 inputs of the bridge or enable chopping if the odd numbered outputs are connected to the enable inputs of the bridge. Selecting the correct chopping mode is an important consideration that affects the stability of the system as well as the dissipation. Table 1 shows a relative comparison of the different chopping modes, for a fixed chopping frequency, motor current and motor inductance.

Figure 5: Driving a unipolar wound motor with a bipolar drive

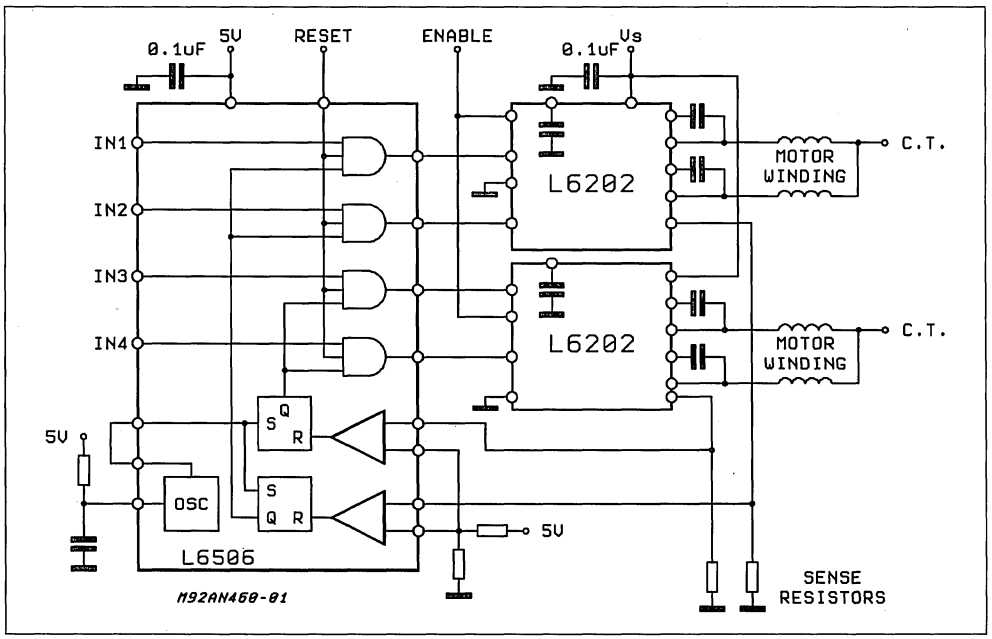


Table 1: Comparative advantages of chopping modes

Chopping Mode	Ripple Current	Motor Dissipation	Bridge Dissipation *	Minimum Current
ENABLE	HIGH	HIGH	HIGH	LOWER
ONE PHASE	LOW	LOW	LOWEST	LOW
TWO PHASE	HIGH	LOW	LOW	Ipp/2

(*) As related to L298N, L6203 or L6202.

Figure 6a: Two Phase Chopping.

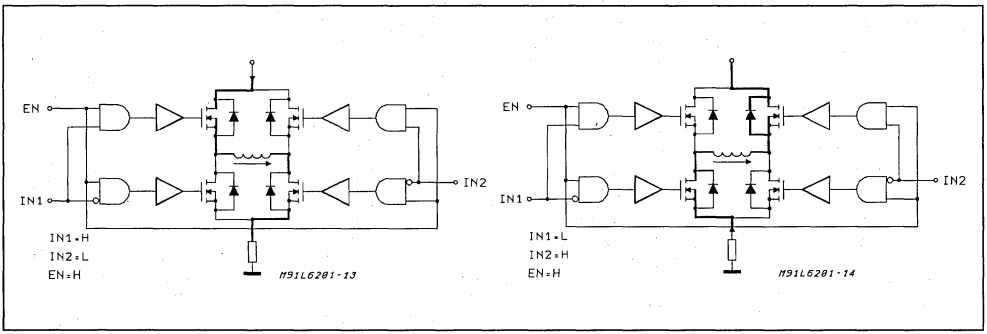


Figure 6b: One Phase Chopping.

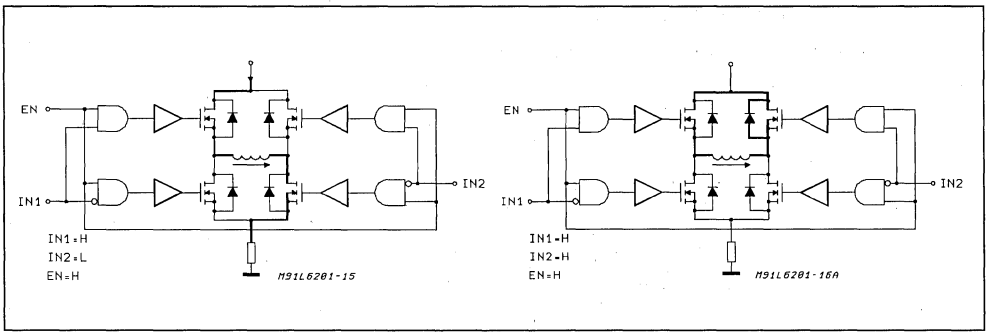
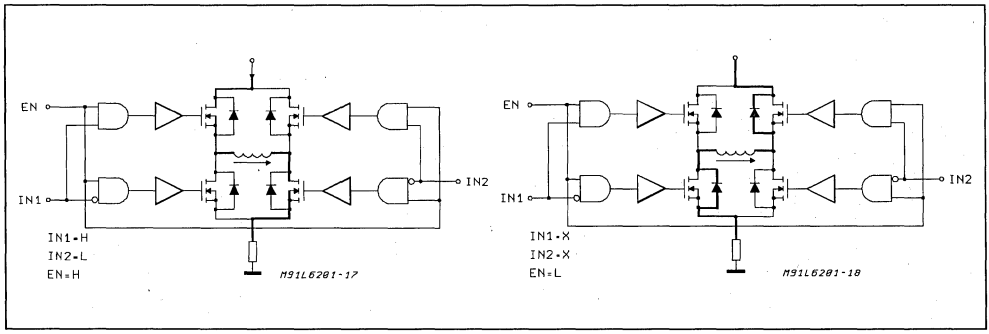


Figure 6c: Enable Chopping.



RIPPLE CURRENT

Since the rate of current change is related directly to the voltage applied across the coil by the equation:

$$V = L \frac{di}{dt}$$

the ripple current will be determined primarily by the chopping frequency and the voltage across the coil. When the coil is driven on, the voltage across the coil is fixed by the power supply minus the saturation voltages of the driver. On the other hand the voltage across the coil during the recirculation time depends on the chopping mode chosen.

When enable chopping or two phase chopping is selected, the voltage across the coil during recirculation is the supply voltage plus either the V_F of the diodes or the RI voltage of the DMOS devices (when using the L6202 in two phase chopping). In this case the slope of the current rise and decay are nearly the same and the ripple current can be large.

When one phase chopping is used, the voltage across the coil during recirculation is V_{on} (V_{sat} for Bipolar devices or $I \cdot R_{DSon}$ for DMOS) of the transistor that remains on plus V_F of one diode plus the voltage drop across the sense resistor, if it is in the recirculation path. In this case the current decays much slower than it rises and the ripple current is much smaller than in the previous case. The effect will be much more noticeable at higher supply voltages.

MOTOR LOSSES

The losses in the motor include the resistive losses (I^2R) in the motor winding and parasitic losses like eddie current losses. The latter group of parasitic losses generally increases with increased ripple currents and frequency. Chopping techniques that have a high ripple current will have higher losses in the motor. Enable or two phase chopping will cause higher losses in the motor with the effect of raising motor temperature. Generally lower motor losses are achieved using phase chopping.

POWER DISSIPATION IN THE BRIDGE IC.

In the L298N, the internal drive circuitry provides active turn off for the output devices when the outputs are switched in response to the 4 phase inputs. However when the outputs are switched off in response to the enable inputs all base drive is removed from output devices but no active element is present to remove the stored charge in the base. When enable chopping is used the fall time of the current in the power devices will be longer and the device will have higher switching losses than if phase chopping is used.

In the L6202 and L6203, the internal gate drive circuit works the same in response to either the input or the enable so the switching losses are the same using enable or two phase chopping, but would be lower using one phase chopping. However, the losses due to the voltage drops across the device are not the same. During enable chopping all four of the output DMOS devices are turned off and the current recirculates through the body to drain diodes of the DMOS output transistors. When phase chopping the DMOS devices in the recirculation path are driven on and conduct current in the reverse direction. Since the voltage drop across the DMOS device is less than the forward voltage drop of the diode for currents less than 2A, the DMOS take a significant amount of the current and the power dissipation is much lower using phase chopping than enable chopping, as can be seen in the power dissipation graphs in the data sheet.
With these two devices, phase chopping will always provide lower dissipation in the device. For discrete bridges the switching loss and saturation losses should be evaluated to determine which is lower.

MINIMUM CURRENT

The minimum current that can be regulated is important when implementing microstepping, when implementing multilevel current controls, or anytime when attempting to regulate a current that is very small compared to the peak current that would flow if the motor were connected directly to the supply voltage used.

With enable chopping or one phase chopping the only problem is loss of regulation for currents below a minimum value. Figure 7 shows a typical response curve for output current as a function of the set reference. This minimum value is set by the motor characteristics, primarily the motor resistance, the supply voltage and the minimum duty cycle achievable by the control circuit. The minimum current that can be supplied is the current that flows through the winding when driven by the minimum duty cycle. Below this value current regulation is not possible. With enable chopping the current through the coil in response to the minimum duty cycle can return completely to zero during each cycle, as shown in figure 8. When using one phase chopping the current may or may not return completely to zero and there may be some residual DC component.

When using a constant frequency control like the L297 or L6506, the minimum duty cycle is basically the duty cycle of the oscillator (sync) since the set dominance of the flip-flop maintains the output on during the time the sync is active. In constant off time regulators, like the PBL3717A, the minimum output time is set by the propagation delay through the circuit and it's ratio to the selected off time.

Figure 7: The transfer function of peak detect current control is nonlinear for low current values.

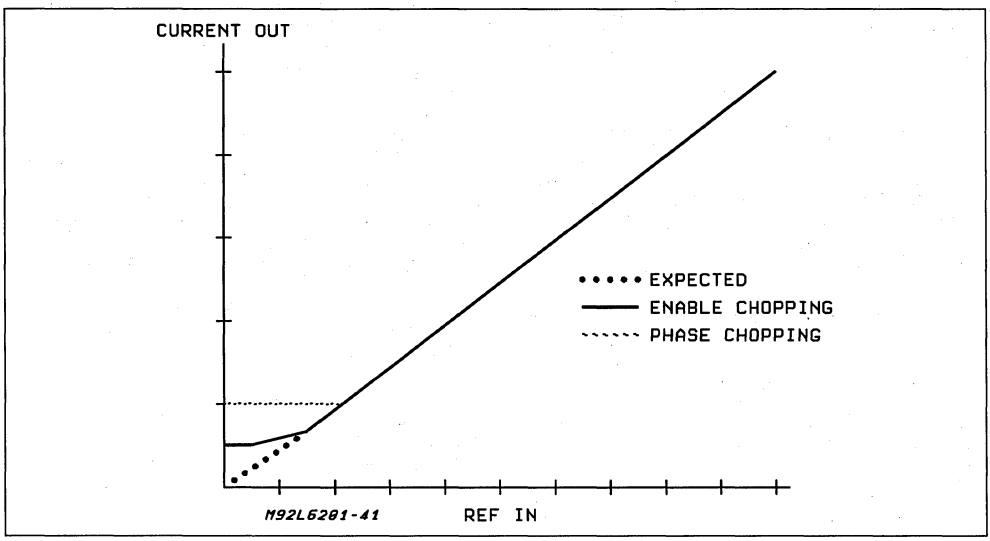
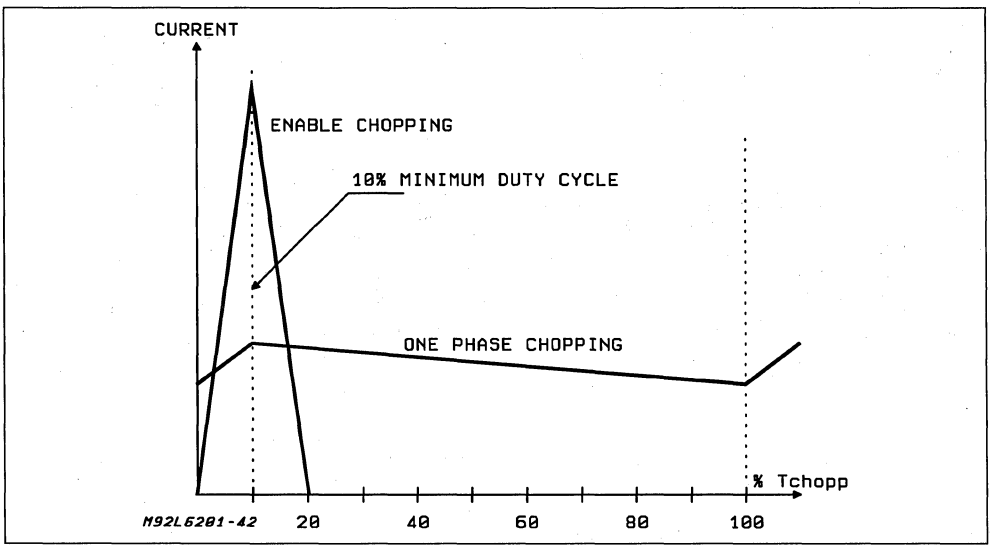
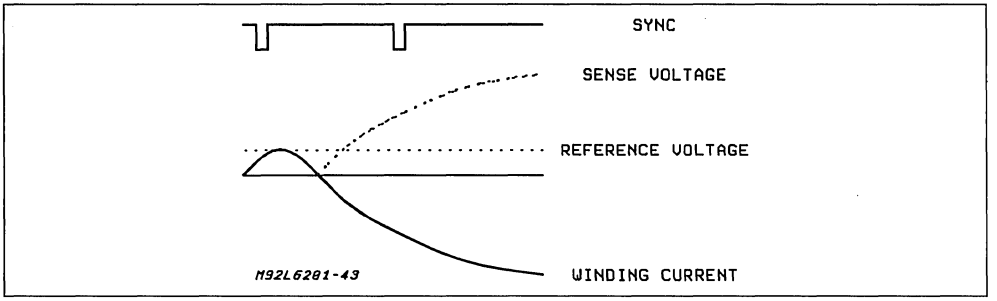


Figure 8: A Minimum current flows through the motor when the driver outputs the minimum duty cycle that is achievable.



For two phase chopping the situation is quite different. Although none of the available control chips implement this mode it is discussed here since it is easy to generate currents that can be catastrophic if two phase chopping is used with peak detecting control techniques. When the peak current is less than 1/2 of the ripple (I_{pp}) current two phase chopping can be especially dangerous. In this case the reverse drive ability of the two phase chopping technique can cause the current in the motor winding to reverse and the control circuit to lose control. Figure 9 shows the current wave form in this case. When the current reaches the peak set by the reference both sides of the bridge are switched and the current decays until it reaches zero. Since the power transistors

Figure 9: Two phase chopping can loose control of the winding current..



are now on, the current will begin to increase in a negative direction. When the oscillator again sets the flip-flop the inputs will then switch again and the current will begin to become more positive. However, the effect of a single sense resistor used with a bridge is to rectify current and the comparator sees only the magnitude and not the sign of the current. If the absolute value of the current in the negative direction is above the set value the comparator will be fooled and reset the flip-flop. The current will continue to become more negative and will not be controlled by the regulation circuit.

For this reason two phase chopping is not recommended with bridge circuits like the L298N or L6203 and is not implemented in any of the currently available driver IC's. The problem can be avoided by more complex current sense techniques that do not rectify the current feedback.

Chopper Stability and Audio Noise.

One problem commonly encountered when using chopping current control is audio noise from the motor which is typically a high pitch squeal. In constant frequency PWM circuits this occurrence is usually traced to a stability problem in the current control circuit where the effective chopping frequency has shifted to a sub-harmonic of the desired frequency set by the oscillator. In constant off time circuits the off time is shifted to a multiple of the off time set by the monostable. There are two common causes for this occurrence.

The first cause is related to the electrical noise and current spikes in the application that can fool the current control circuit. In peak detect PWM circuits, like the L297 and L6506, the motor current is sensed by monitoring the voltage across the sense resistor connected to ground. When the oscillator sets the internal flip flop causing the bridge output to turn on, there is typically a voltage spike developed across this resistor. This spike is caused by noise in the system plus the reverse recovery current of the recirculating diode that flows through the sense resistor, as shown in Figure 10. If the magnitude of this spike is high enough to exceed the reference voltage, the comparator can be fooled into resetting the flip-flop prematurely as shown in Figure 11. When this occurs the output is turned off and the current continues to decay. The result is that the fundamental frequency of the current wave form delivered to the motor is reduced to a sub-harmonic of the oscillator frequency, which is usually in the audio range. In practice it is not uncommon to encounter instances where the period of the current wave form is two, three or even four times the period of the oscillator. This problem is more pronounced in breadboard implementations where the ground is not well laid out and ground noise contributes makes the spike larger.

When using the L6506 and L298N, the magnitude of the spike should be, in theory, smaller since the diode reverse recovery current flows to ground and not through the sense resistor. However, in applications using monolithic bridge

Figure 10: Reverse recovery current of the recirculation diode flows through the sense resistor causing a spike on the sense resistor.

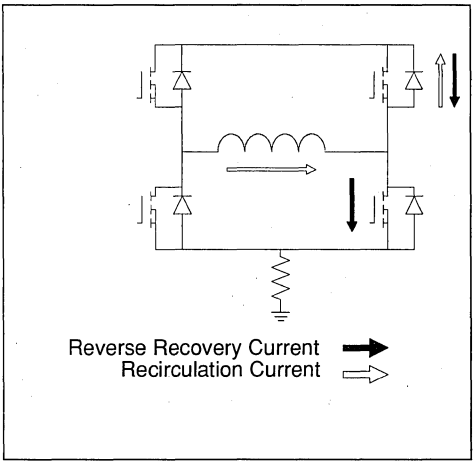
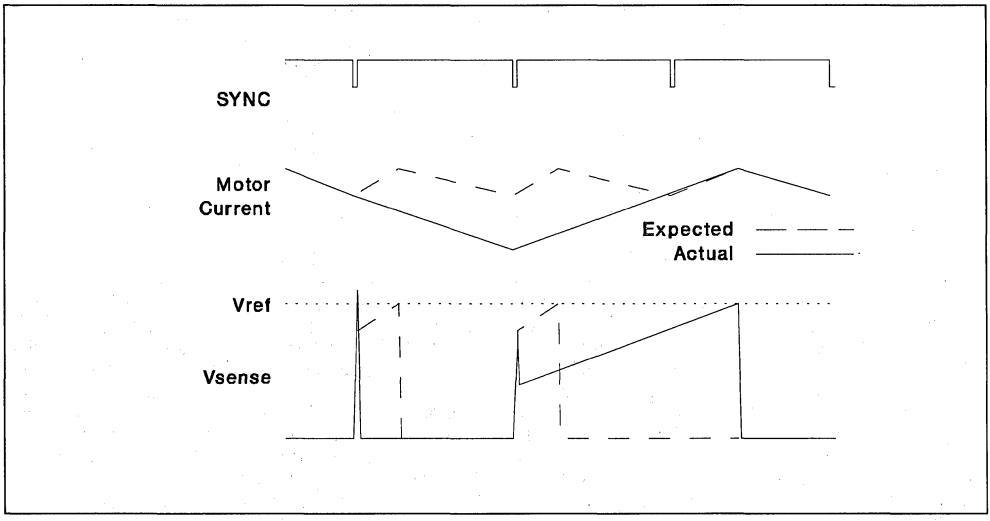


Figure 11: Spikes on the sense resistor caused by reverse recovery currents and noise can trick the current sensing comparator.



drivers, like the L298N, internal parasitic structures often produce recovery current spikes similar in nature to the diode reverse recovery current and these may flow through the emitter lead of the device and hence the sense resistor. When using DMOS drivers, like the L6202, the reverse recovery current always flows through the sense resistor since the internal diode in parallel with the lower transistor is connected to the source of the DMOS device and not to ground.

In constant off time FM control circuits, like the PBL3717A, the noise spike fools the comparator

CALCULATING POWER DISSIPATION IN BRIDGE DRIVER IC'S

The power dissipated in a monolithic driver IC like the L298N or L6202 is the sum of three elements: 1) the quiescent dissipation, 2) the saturation losses and 3) the switching losses.

The quiescent dissipation is basically the dissipation of the bias circuitry in the device and can be calculated as Vs · Is where Vs is the power supply voltage and Is is the bias current or quiscent current from the supply. When a device has two supply voltages, like the L298N, the dissipation for each must be calcualted then added to get the total quiescent dissipation. Generally the quiescent current for most monolithic IC's is constant over a vide range of input voltages and the maximum value given on the data sheet can be used for most supply voltages within the allowable range.

The saturation loss is basically the sum of the voltage drops times the current in each of the output transistors. For Bipolar devices, L298N, this is Vsat · I. For DMOS power devices this is $I^2 \cdot R_{DSon}$.

The third main component of dissipation is the switching loss associated with the output devices. In general the switching loss can be calculated as:

$$Vsupply \cdot Iload \cdot tcross \cdot fswitch$$

To calculate the total power dissipation these three compnents are each calculated, multipled by their respective duty cycle then added togther. Obviously the duty cycle for the quiescent current is equal to 100%.

and retriggers the monostable effectively multiplying the set off time by some integer value.

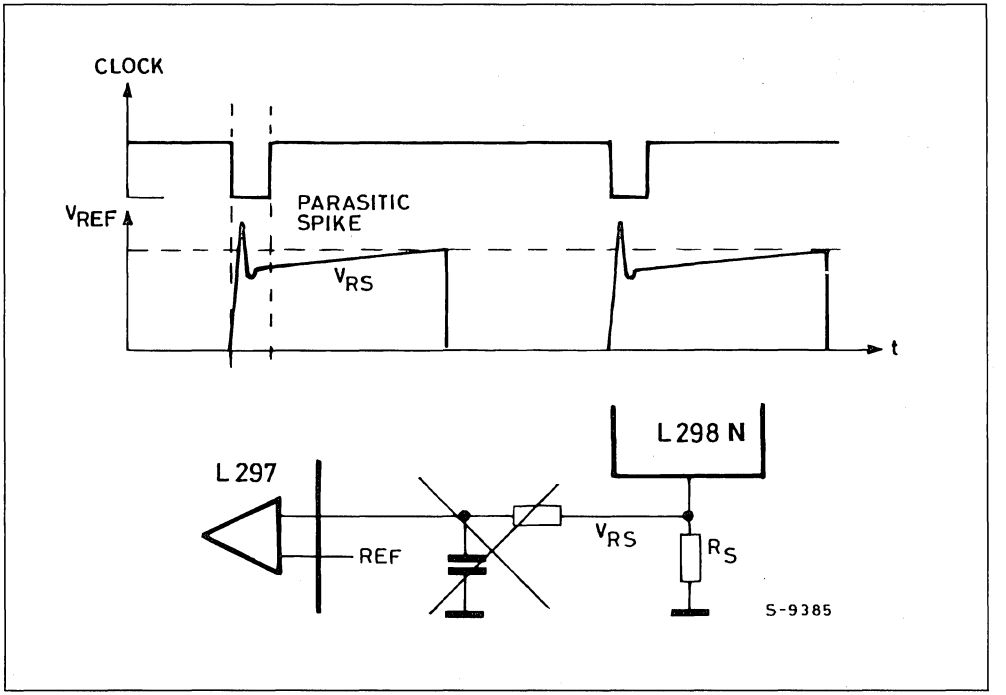
Two easy solutions to this problem are possible. The first is to put a simple RC low pass filter between the sense resistor and the sense input of the comparator. The filter attenuates the spike so it is not detected by the comparator. This obviously requires the addition of 4 additional components for a typical stepper motor. The second solution is to use the inherent set dominance of the internal flip-flop in the L297 or L6506 [1][3] to mask out the spike. To do this the width of the oscillator sync pulse is set to be longer than the sum of the propagation delay (typically 2 to 3µs for the L298N) plus the duration of the spike (usually in the range of 100ns for acceptable fast recovery diodes), as shown in figure 12. When this pulse is applied to the flip-flop set input, any signal applied to the reset input by the comparator is ignored. After the set input has been removed the comparator can properly reset the flip-flop at the correct point.

The corresponding solution in frequency modulated circuits, is to fix a blanking time during which the monostable may not be retriggered.

The best way to evaluate the stability of the chopping circuit is to stop the motor movement (hold the clock of the L297 low or hold the four inputs constant with the L6506) and look at the current wave forms without any effects of the phase changes. This evaluation should be done for each level of current that will be regulated. A DC current probe, like the Tektronix AM503 system, provides the most accurate representation of the motor current. If the circuit is operating stability, the current wave form will be synchronized to the sync signal of the control circuit. Since the spikes discussed previously are extremely short, in the range of 50 to 150 ns, a high frequency scope with a bandwidth of at least 200 MHz is required to evaluate the circuit. The sync signal to the L297 or L6506 provides the best trigger for the scope.

The other issue that affects the stability of the constant frequency PWM circuits is the chopping mode selected. With the L297 the chopping signal may be applied to either the enable inputs or the four phase inputs. When chopping is done using the enable inputs the recirculation path for the current is from ground through the lower recirculation diode, the load, the upper recirculation diode and back to the supply, as shown in Figure 6c. This same recirculation path is achieved using two phase chopping, although this may not be implemented directly using the L297 or L6506. In

Figure 12: The set-dominanct latch in the L297 may be used to mask spikes on the sense resistor that occur at switching.



this mode, ignoring back EMF, the voltage across the coil during the on time (t_1) when current is increasing and the recirculation time (t_2), are:

$$V_1 = V_s - 2\,V_{sat} - V_{Rsense}$$

and

$$V_2 = V_{ss} + 2\,V_F$$

The rate of current change is given by (ignoring the series resistance):

$$V = L\frac{di}{dt}$$

Since the voltage across the coil (V_2) during the recirculation time is more than the voltage (V_1) across the coil during the on time the duty cycle will, by definition, be greater than 50% because t_1 must be greater than t_2. When the back EMF of the motor is considered the duty cycle becomes even greater since the back EMF opposes the increase of current during the on time and aides the decay of current.

In this condition the control circuit may be content to operate stability at one half of the oscillator frequency, as shown in Figure 13. As in normal operation, the output is turned off when the current reaches the desired peak value and decays until the oscillator sets the flip-flop and the current again starts to increase. However since t_1 is longer than t_2 the current has not yet reached the peak value before the second oscillator pulse occurs. The second oscillator pulse then has no effect and current continues to increase until the set peak value is reached and the flip-flop is reset by the comparator. The current control circuit is completely content to keep operating in this condition. In fact the circuit may operate on one of two stable conditions depending on the random time when the peak current is first reached relative to the oscillator period.

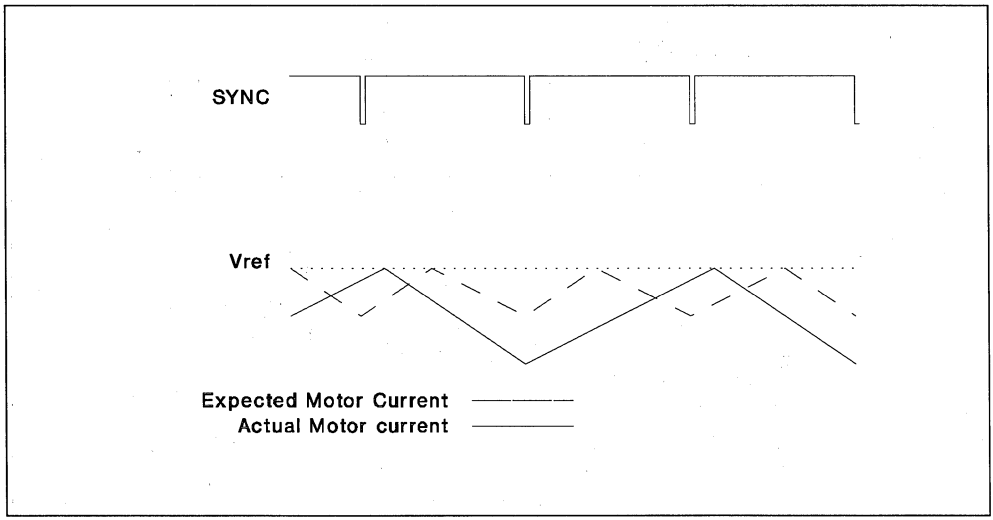
The easiest, and recommended, solution is to apply the chopping signal to only one of the phase inputs, as implemented with the L297, in the phase chopping mode, or the L6506.

Another solution that works, in some cases, is to fix a large minimum duty cycle, in the range of 30%, by applying an external clock signal to the sync input of the L297 or L6506. In this configuration the circuit must output at least the minimum duty cycle during each clock period. This forces the point where the peak current is detected to be later in each cycle and the chopping frequency to lock on the fundamental. The main disadvantage of this approach is that it sets a higher minimum current that can be controlled. The current in the motor also tends to overshoot during the first few chopping cycles since the actual peak current is not be sensed during the minimum duty cycle.

EFFECTS OF BACK EMF

As mentioned earlier, the back EMF in a stepper motor tends to increase the duty cycle of the chopping drive circuits since it opposes current increased and aids current decay. In extreme, cases where the power supply voltage is low compared to the peak back EMF of the motor, the duty cycle required when using the phase chopping may exceed 50% and the problem with the stability of the operating frequency discussed

Figure 13: When the output duty cycle exceeds 50% the chopping circuit may sinchronize of a sub-harmonic of the oscillator frequency.



above can occur. At this point the constant frequency chopping technique becomes impractical to implement and a chopping technique that uses constant off time frequency modulation like implemented in the PBL3717A, TEA3717, TEA3718, and L6219 is more useful.

Why Won't the motor move

Many first time users of chopping control drives first find that the motor does not move when the circuit is enabled. Simply put the motor is not generating sufficient torque to turn. Provided that the motor is capable of producing the required torque at the set speed, the problem usually lies in the current control circuit. As discussed in the previous section the current sensing circuit can be fooled. In extreme cases the noise is so large that the actual current through the motor is essentially zero and the motor is producing no torque. Another symptom of this is that the current being drawn from the power supply is very low.

Avoid Destroying the Driver

Many users have first ask why the device failed in the application. In almost every case the failure was caused by electrical overstress to the device, specifically voltages or currents that are outside of the device ratings. Whenever a driver fails, a careful evaluation of the operating conditions in the application is in order.

The most common failure encountered is the result of voltage transients generated by the inductance in the motor. A correctly designed application will keep the peak voltage on the power supply, across the collector to emitter of the output devices and, for monolithic drivers, from one output to the other within the maximum rating of the device. A proper design includes power supply filtering and clamp diodes and/or snubber networks on the output [6].

Selecting the correct clamp diodes for the application is essential. The proper diode is matched to the speed of the switching device and maintains a V_F that limits the peak voltage within the allowable limits. When the diodes are not integrated they must be provided externally. The diodes should have switching characteristics that are the same or better than the switching time of the output transistors. Usually diodes that have a reverse recovery time of less than 150 ns are sufficient when used with bipolar output devices like the L298N. The 1N4001 series of devices, for example, **is not** a good selection because it is a slow diode.

Although it occurs less frequently, excess current can also destroy the device. In most applications the excess current is the result of short circuits in the load. If the application is pron to have shorted loads the designer may consider implementing some external short circuit protection [7].

Shoot through current, the current that flows from supply to ground due to the simultaneous conduction of upper and lower transistors in the bridge output, is another concern. The design of the L298N, L293 and L6202 all include circuitry specifically to prevent this phenomena. The user should not mistake the reverse recovery current of the diodes or the parasitic structures in the output stage as shoot through current.

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[2]"Constant Current Chopper Drive Ups Stepper-Motor Performance" (AN468)

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[5]Leenouts, Albert. The Art and Practice of Step Motor Control. Ventura CA: Intertec Communications Inc. (805) 658-0933. 1987

[6]Hopkins, Thomas. "Controlling Voltage Transisnts in Full Bridge Drivers" (AN280)

[7]Scrocchi G. and Fusaroli G. "Short Circuit Protection on L6203". (AN279)

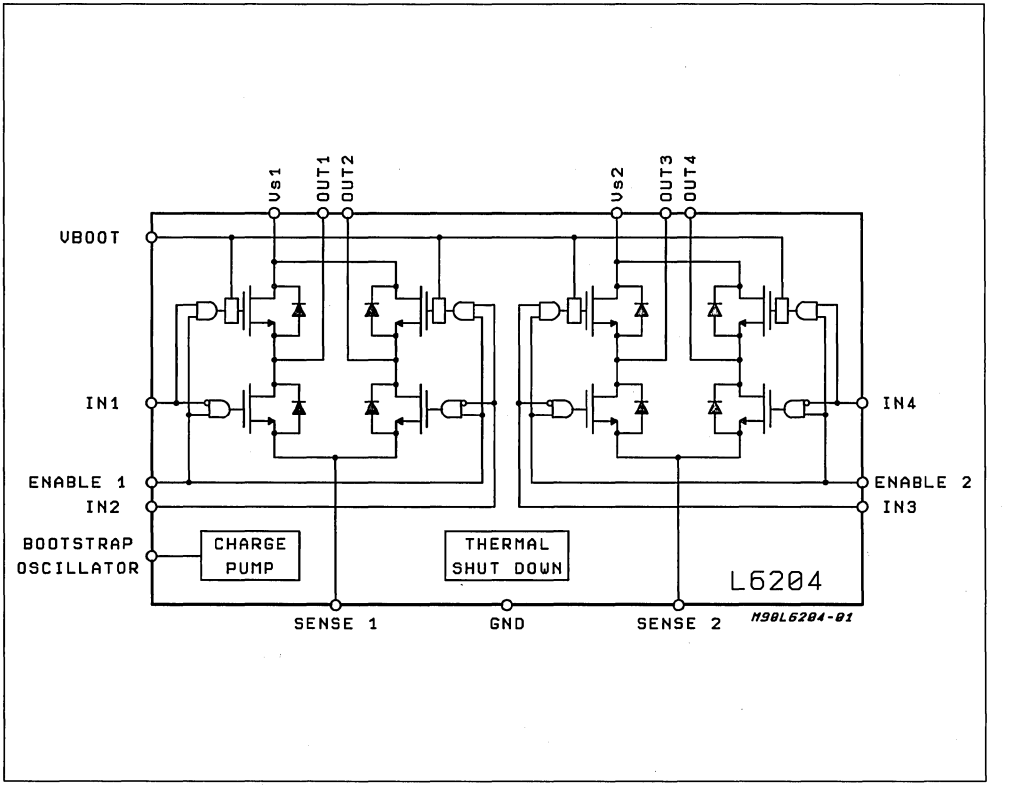
USING THE L6204, A BIPOLAR STEPPER AND DC MOTOR DRIVER IN BCD TECHNOLOGY

by E Balboni

Containing two H-bridge drivers, the L6204 is a compact and simple solution for driving two-phase bipolar stepper motors and in applications where two DC motors must be driven.

The L6204 is a DMOS dual full bridge driver mainly designed to drive bipolar stepper motors. All the inputs are TTL/CMOS compatible and each bridge can be enabled by its own dedicated input. The windings current can be regulated by sensing the voltage drop across two low value resistors at the low end of both the bridge: this is the feedback for the current controller. To feed the gates of the upper DMOS, a peak to peak rectifier charges a capacitor in series with the Power Supply voltage at the optimum DC level defined by an on-board square wave oscillator. The L6204 , with 0.5 A drive capability without external heatsink up to 70°C, is packaged in a 20 leads PowerDip with four heat transfer pins. The Block diagram of the device is shown in fig.1.

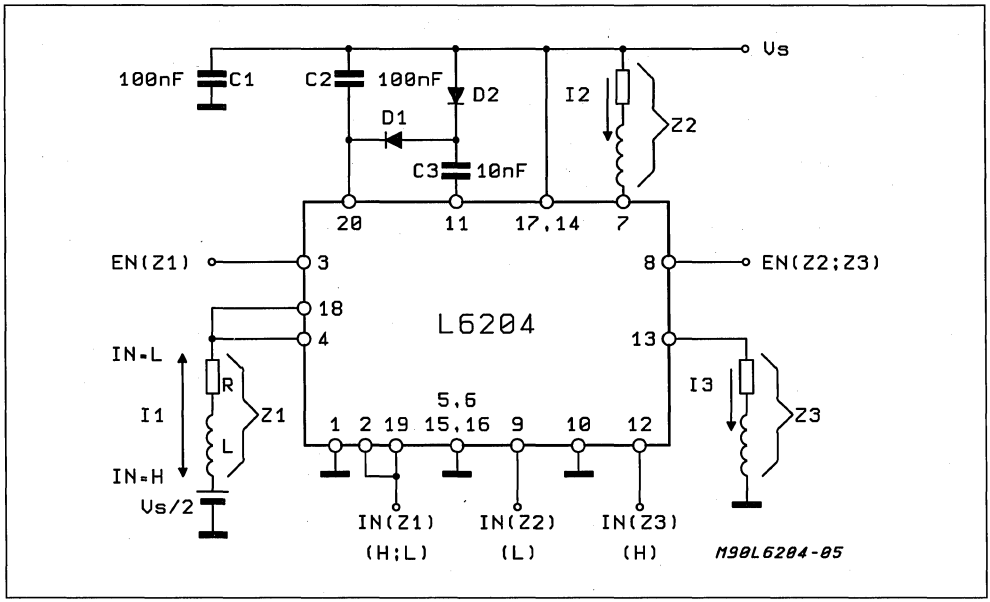
Figure 1: Block diagram of the L6204 single chip dual full bridge driver.



GENERAL APPLICATIONS HINTS

The L6204 can be used in a very wide range of applications such as the drive of lamps, solenoids, DC motors or any other inductive loads. The drive of different loads in single-ended configuration is shown in fig.2. The current in the Load Z1, that may be a DC motor, can flow in both the directions but its peak amplitude cannot be controlled. By means of a change of the Duty Cycle of the input signal it is possible to vary in Open Loop Mode the steady state speed of the DC motor: this is possible because the average current in the winding is dependent from the Duty Cycle. The L/R ratio must be a few times shorter than the minimum DC. In a similar way it can be dimmed a lamp connected to the supply (Z2) or to ground (Z3). Very often, when a DC motor is driven, peak current and speed must be booth controlled in a Closed Loop Mode.

Figure 2: The L6204 is not intended only for Bipolar Stepper applications: here above three different driver configurations are shown. Z1 is a DC motor to be driven in both CW and CCW direction. Z2 can be solenoid like a relay or hammer. Z3 can be an alogen lamp which light intensity is controlled by variable Duty Cycle.



This is achieved by the configuration shown in fig.3A. The two independent motors (A and B) can be controlled by only one controller (L6506). The sensing resistor (RsA, RsB) generates a voltage proportional to the motor current, that is the feedback for the current control loop. A second loop, not shown in figure, can control the speed stability while the direction is defined by the Input state of the L6506. The Enable Input (ENA, ENB) can inhibit one motor or the other while the Power Enable acts on both at the same time. D1 and D2 (BAT41 or equivalent), C3 and C4, generates the bootstrap voltage by rectifiing the wave available at pin. 11 of the L6204. When more than one driver is used at the same Supply Voltage on a common Printed Circuit Board, the bootstrap voltage can be generated only by one of them (master) and used to supply all the other L6204 (slaves) saving diodes and capacitors. R1 C1 (R2 C2) is a snubber network that must be closely connected to the output pins and its use is recommended in all the application circuits using the L6204. The values can be calculated as it follows: R = Vs/Ip and C = Ip/(dV/dt), where Vs is the maximum Supply Voltage of the Application, Ip is the peak of the load current and dV/dt is the Slew Rate accepted as the optimum compromise between speed and transient generation/radiation (SR of 200 V/µS are commonly chosen). The network R5C5 sets the operating frequency according to f = 1/(0.69 R5C5) for R5 ≥ 10Kohm. R3 and R4 are used to protect the comparator input inside the L6506 against possible negative transitions across the sensing resistor RsA or RsB. The L6204 can be used with paralleled inputs and outputs to double the current capability of the single bridge; for an optimized solution, however, 1.6 times the nominal current is recommended in-

stead of two. This configuration is shown in fig.2 to drive the load Z1. A more complex circuit, in wich one paralleled L6204 drives a DC motor, is shown in fig.3B; in this example the two chopper of the L6506 are used to implement two functions: 1) Current Control during speed variation at Ip max = 0.8A and 2) Current Control during brake and/or direction change at higher current level that depends from the brake repetition (it must be in the Max Ratings limit). The divider R6R7 defines the brake current intensity as V17/Rs while the product (Ip max.) x (Rs) is the limit of the reference voltage V16 for speed control. The Enable function is driven via the L6506 . Since during the brake time the Enable of the L6506 is chopped, the motor current ricirculates via the Supply; because of this a suitable large capacitor must be connected in parallel to C2.

Figure 3A: Bidirectional DC motor drive. The L6204 can drive two motors.

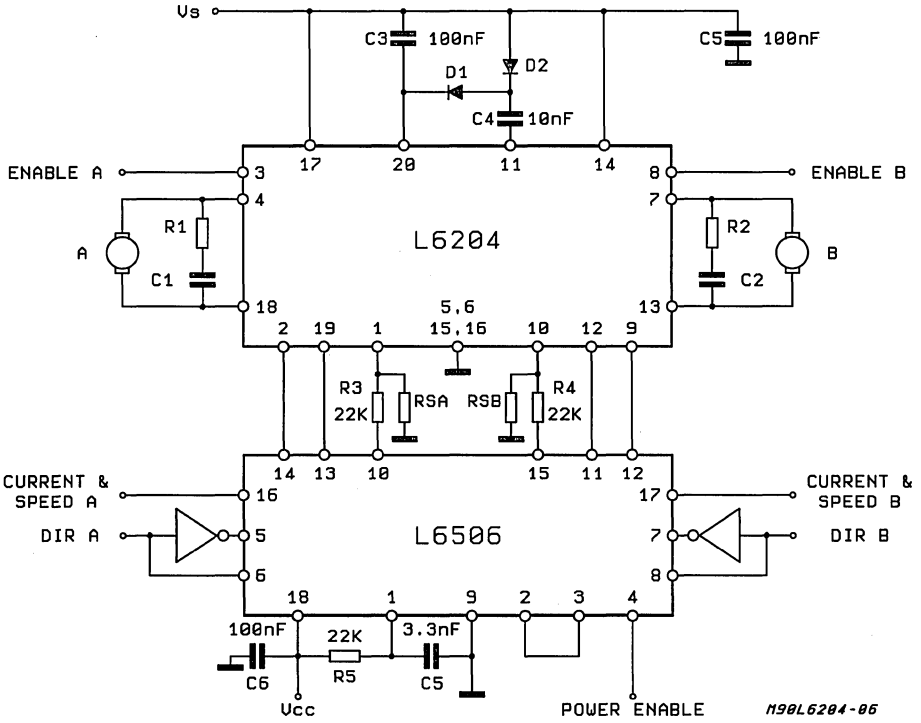
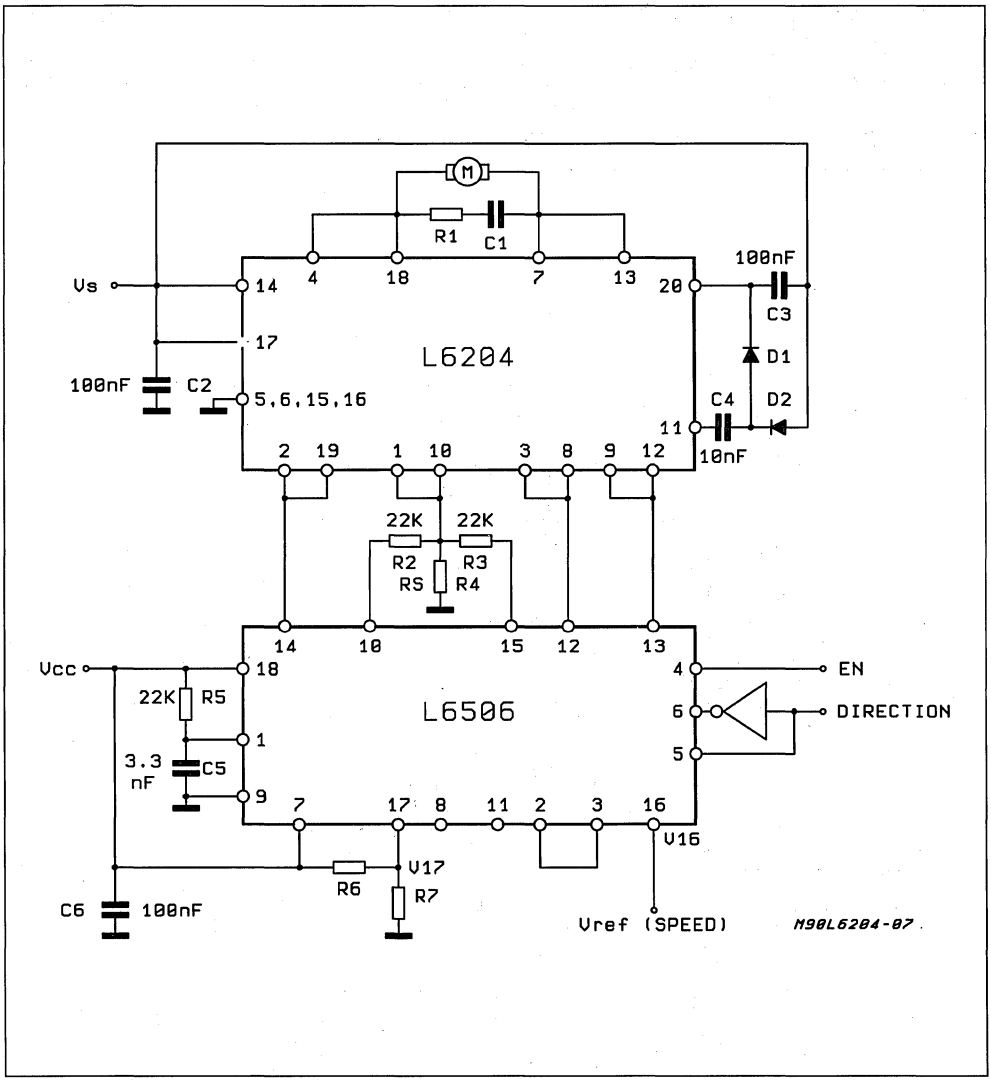


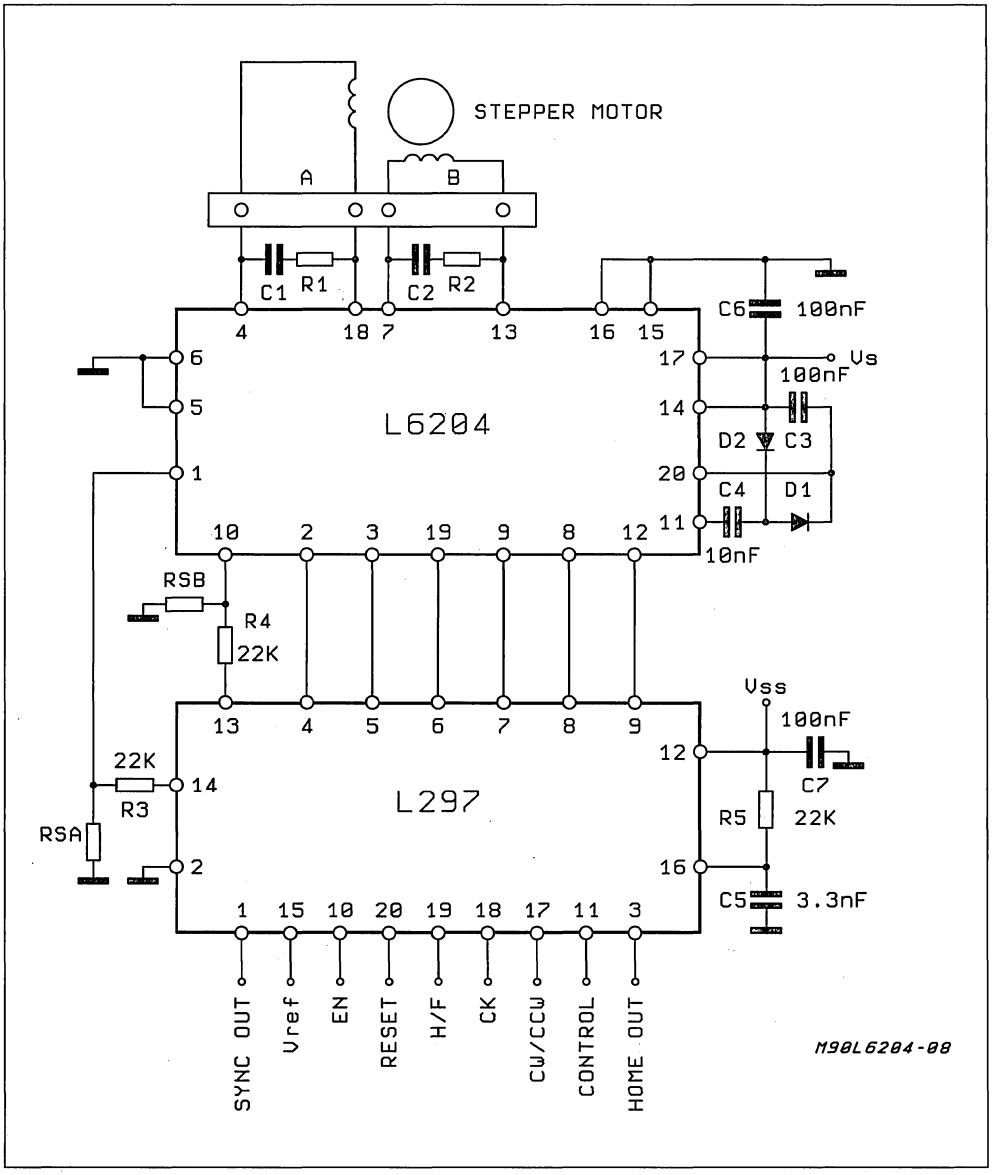
Figure 3B: Bidirectional DC motor drive. The L6204 can drive the motor in a paralleled configuration while the L6506 provides the peak current control both during normal rotation and during braking time.



Stepping Motor Driving

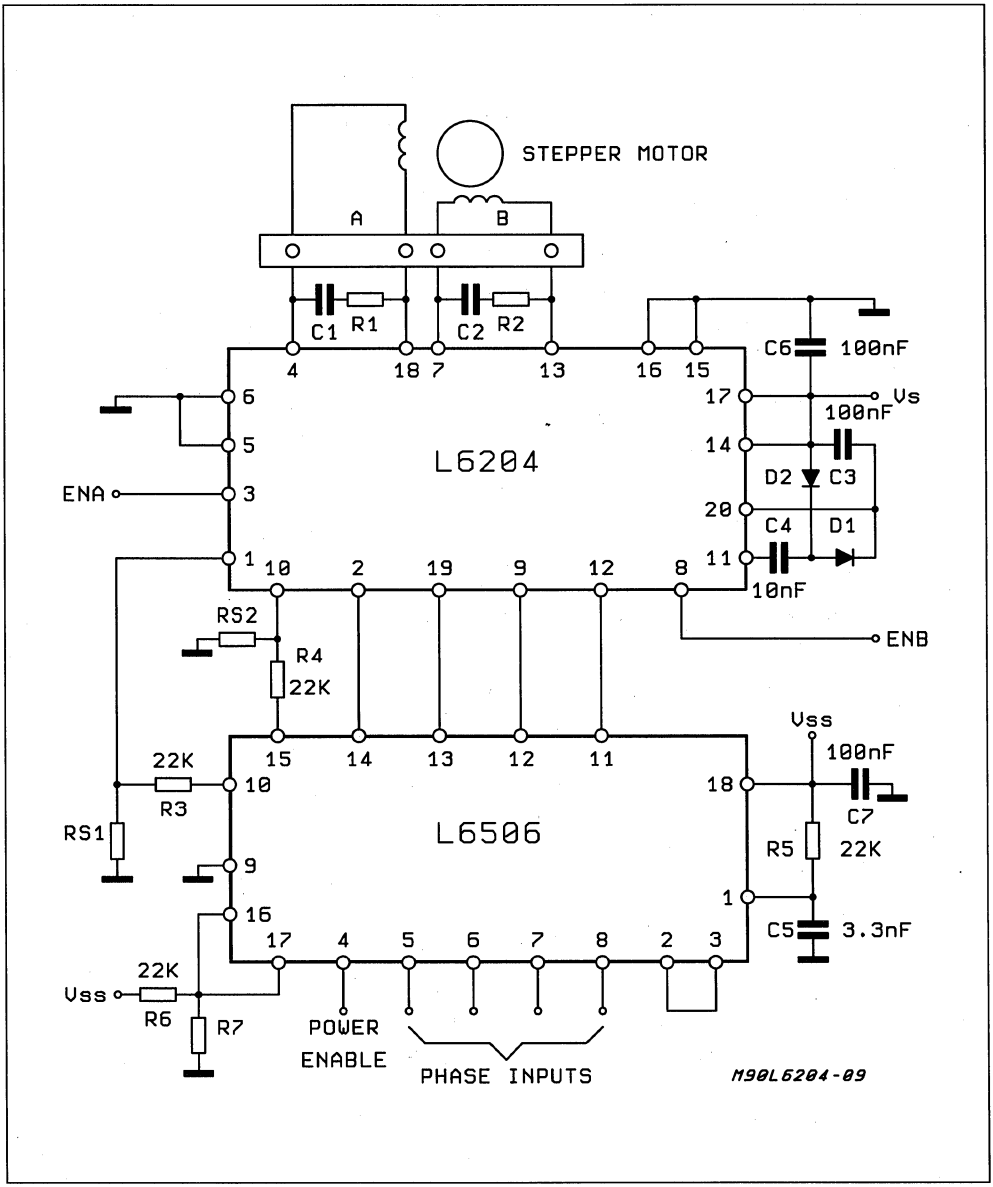
The drive of one stepping motor is shown in fig.4, where the controller L297 generates the requested signals to drive the motor in Half-Step Mode or in Full Step Mode.
The rotation speed or step change is controlled by a clock signal or a single clock pulse at pin.18 (CK). The Mode depends from the logical state of the H / F input while the state of the CW/CCW input defines the direction of the rotation. Depending on the numbered state, odd or even, of an internal clock pulse at the moment at wich the Full-Step Mode is selected, the motor is driven with two-phases-on or with one-phase-on respectively. An open collector output (home) indicates the translator state 0101 that occurs only during an odd numbered state of the internal clock.

Figure 4: Bipolar stepping motor drive: phase sequence generation and current peak control are achieved by means of the controller L297.



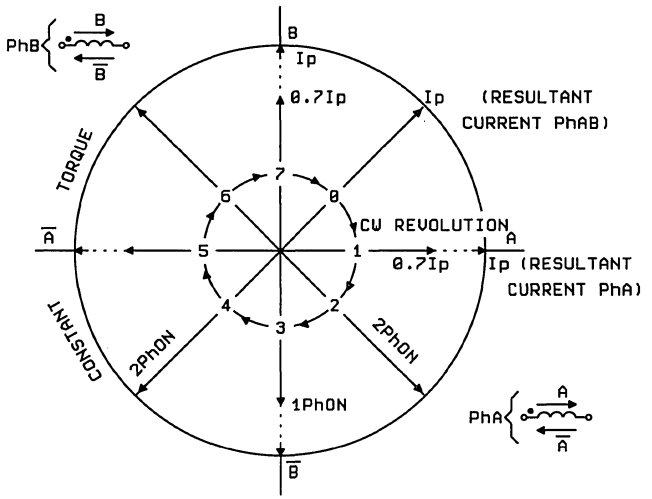
This last is obtained from the oscillator the frequency of which is fixed by the ratio 1/0.69 R5C5 about (R5 ≥ 10Kohm). The peak of the chopped current is given by the ratio of the reference voltage at pin.15 and the value of the sensing resistors Rs. When the four phase signals needed at the inputs of the L6204 are generated in any other way than by the L297 (for example, via µProcessor), the motor driver needs one interface to control the peak current. One possible solution is shown in fig.5.

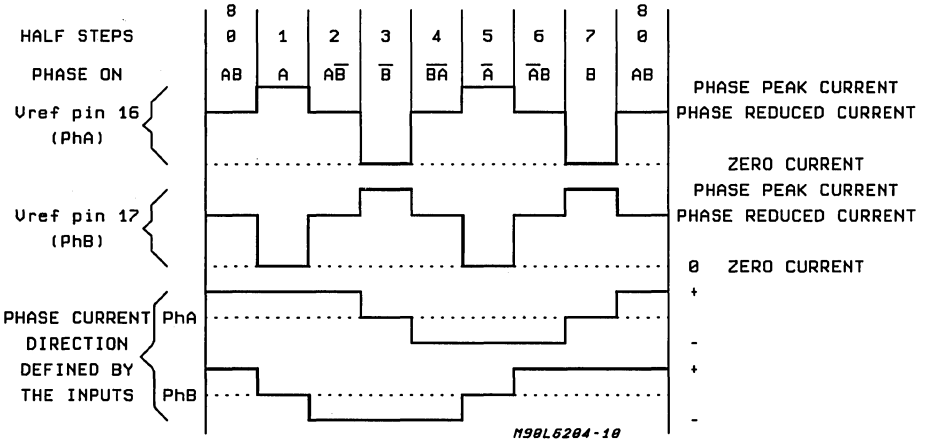
Figure 5: The L6506 can be used to control the peak current in the windings of a bipolar stepper motor. The power is supplied by the L6204.



The motor can be driven in the Full-Step or in Half-Step Mode. The chopped current Ip is controlled at the value Vref/Rs where Vref is the output voltage of the divider R6 R7. The pins 16 and 17 (reference input voltage of the controller) can be driven with two different signals. This arrangement allows to keep constant the motor current and the torque during the Half-Step Mode revolution of the stepper. This behavior is well explained by the fig. 6.

Figure 6: Characteristics of the Half - Step Mode drive with constant torque control. It should be noted that the resultant current is constant while the current in the windings alternates between one-phase-on and two-phase-on with a ratio of $\sqrt{2}$.





BIPOLAR STEPPER MOTOR CONTROL

By Pierre PAYET BURIN

This application note is intended to provide design details for the implementation of a stepper motor control, built around the TEA3717.

This integrated circuit has been developed to offer control and current regulation of up to 1A, in one winding of a bipolar motor.

Two TEA3717s and a minimum of external components are sufficient to implement the full control function of a two-phase bipolar stepper motor.

The system can be commanded, according to the desired mode of operation, by either fixed or programmable logic.

FUNCTIONAL DESCRIPTION

The circuit is organized around a H-bridge configurated by four transistors and their integrated free wheel diodes.

The "Phase" input controls the switching of the bridge transistors and also determines the direction of the current flow in the winding. The signal applied to this input is first gated through a Schmidt trigger and then through a delay element so as to avoid a simultaneous conduction of transistors when direction of current in the bridge is reversed.

Regulation of winding current is performed by chopping action on the power supply for a duration t_{off} determined by a monostable.

This monostable is triggered by the output level swing of a comparator, to the input of which a voltage proportional to delivered output current is applied.

The current spikes corresponding to the diodes reverse recovery time are filtered by a low pass filter R_C C_C to not trigger the comparator.

Three comparators are available for this purpose : their thresholds are internally fixed ratios of V_R input voltage. Each of them can be selected individually by using I_1 and I_0 inputs.

Figure 1 : TEA3717 Block Diagram.

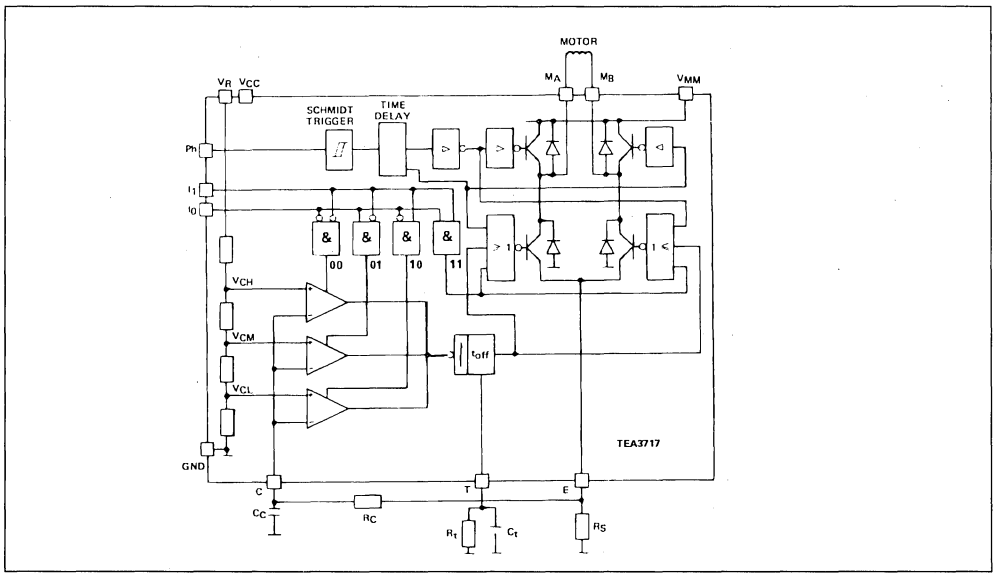
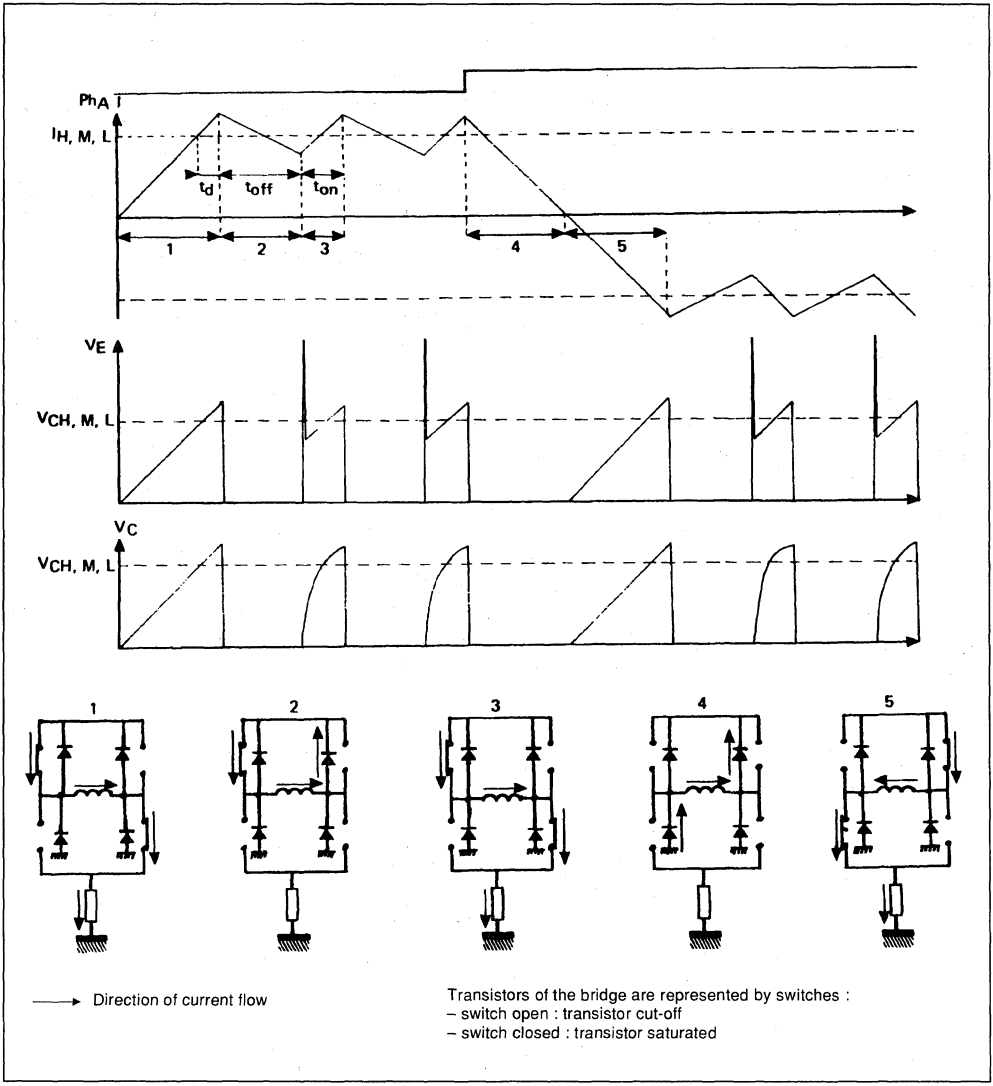


Figure 2 : Typical Operating Sequences.



CONTROL OF BIPOLAR TWO-PHASE MOTOR

The proposed diagram features two TEA3717s each controlling one winding. Full-step and fraction-of-a-step operation is performed by combined use of phase and current level selection control inputs.

Figure 3 : Control of a Bipolar Two-phase Motor.

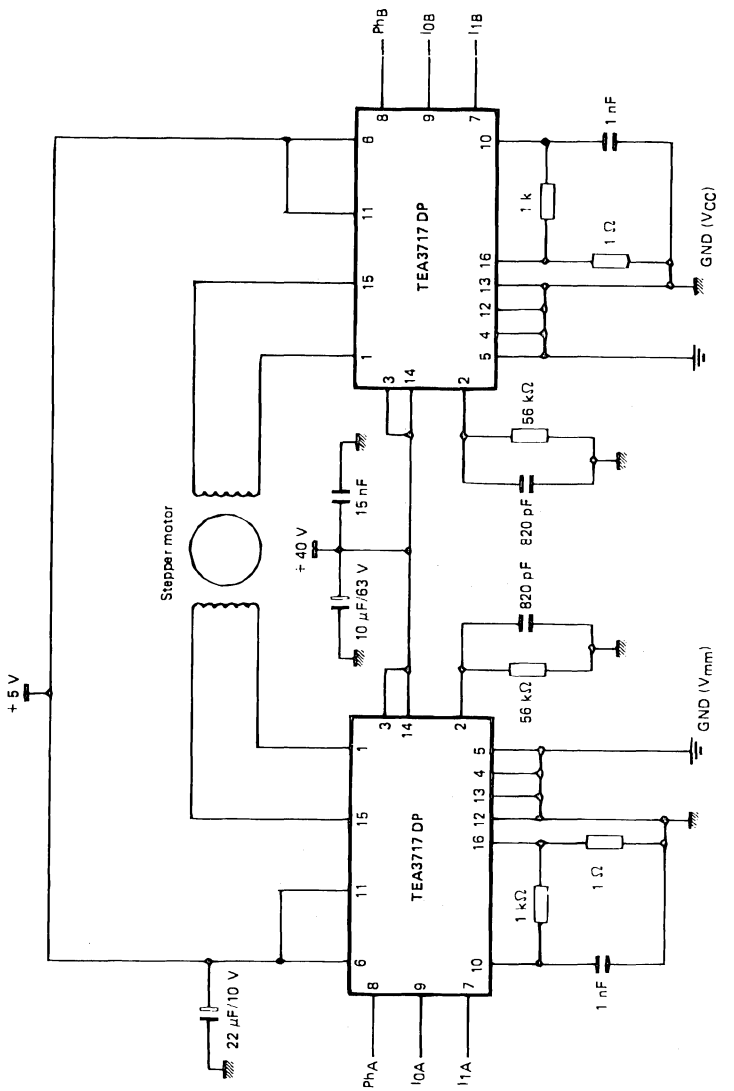
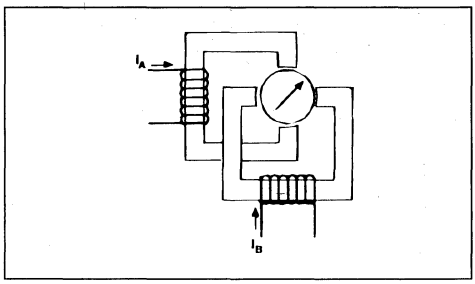


Figure 4 : Winding Currents for Rotation in Full-and Micro-steps.



I_A, I_B : Currents flowing through motor windings.
I_H, I_M, I_L : Current thresholds selected by I_0, I_1.
I : any of I_H, I_M or I_L values.

I_0	I_1	I
1	1	0
0	1	I_L
1	0	I_M
0	0	I_H

N° of steps	I_A	I_B
1	I	I
2	I	− I
3	− I	− I
4	− I	I

Full step.

N° of steps	I_A	I_B
1	I	I
	I	0
2	I	- I
	0	- I
3	- I	- I
	- I	0
4	- I	I
	0	I

1/2 step.

N° of steps	I_A	I_B
1	I	I
	I_M	I_L
2	I_M	- I_L
	I	- I

1/3 step.

N° of steps	I_A	I_B
1	I	I
	I_M	I_L
	I	0
2	I_M	- I_L
	I	- I

1/4 step.

N° of steps	I_A	I_B
1	I	I
	I_H	I_M
	I_H	I_L
	I_H	- I_L
2	I_H	- I_M
	I	- I

1/5 step.

N° of steps	I_A	I_B
1	I	I
	I_H	I_M
	I_M	I_L
	I	0
	I_M	- I_L
	I_H	- I_M
2	I	- I

1/6 step.

N° of steps	I_A	I_B
1	I	I
	I_H	I_M
	I_M	I_L
	I_H	I_L
	I_H	- I_L
	I_M	- I_L
	I_H	I_M
2	I	- I

1/7 step.

N° of steps	I_A	I_B
1	I	I
	I_H	I_M
	I_M	I_L
	I_H	I_L
	I	0
	I_H	- I_L
	I_M	- I_L
	I_H	- I_M
2	I	- I

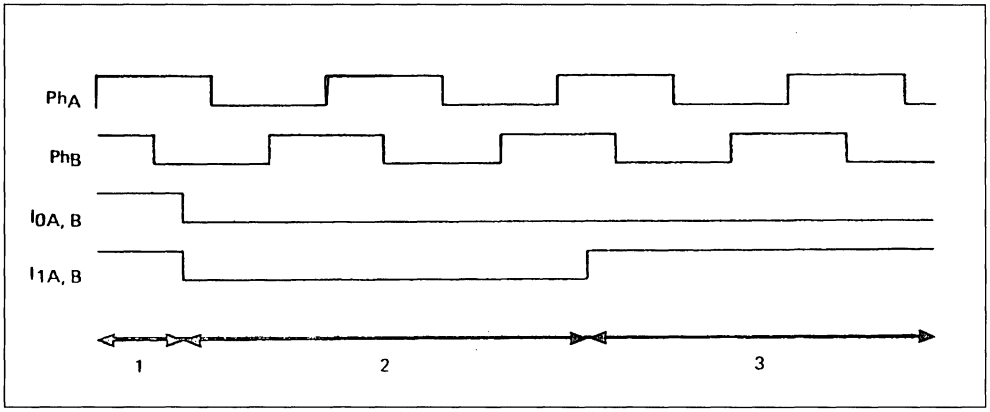
1/8 step.

FULL-STEP OPERATION :

This is moto's typical mode of operation. Simultaneous power supply to both windings guarantees availability of maximum torque.

"Phase" inputs determine the direction of current flow in the windings, while inputs I_0 and I_1 at a constant level, select the level of this current. This is the simplest type of control implementation.

Figure 5 : Signals to Provide to Controller for Full-step Rotation.



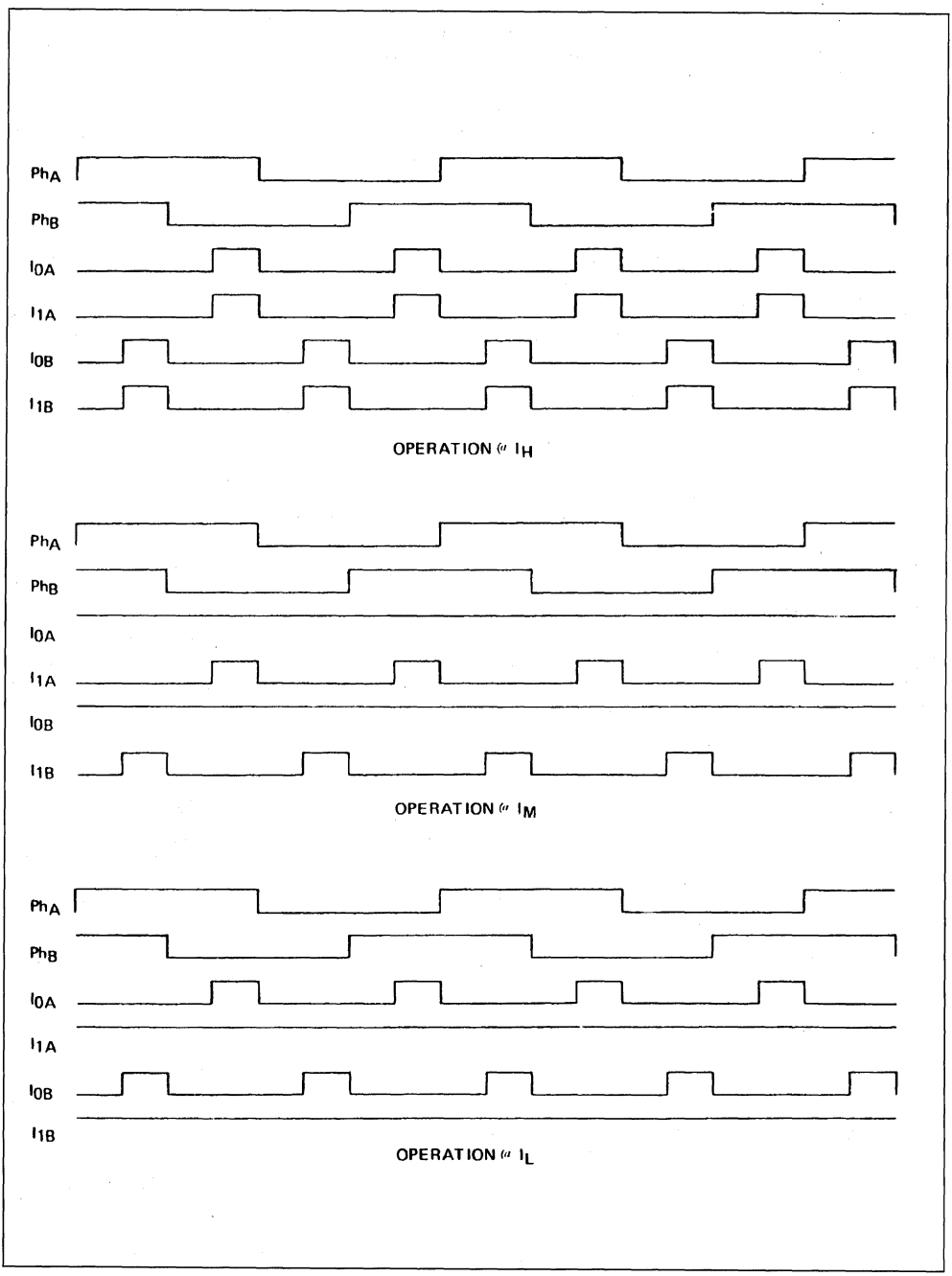
1 - Motor not controlled.
2 - Rotation of 7 steps @ I_H max. current.
3 - Rotation of 6 steps @ I_L low current.

HALF-STEP OPERATION :

This mode allows to double the motor resolution and also to eliminate certain vibrations. Power is applied alternately to one winding and then to both. In half-step position, where only one winding is powered, torque available on motor spindle is at its lowest value.

Same control signals as those used for full-step operation are applied to "phase" inputs, and I_0, I_1 inputs are used to annul the current in one winding.

Figure 6 : Signals to Provide to Controller for Full-step Rotation.



MICRO-STEP OPERATION:

Micro-steps of up to 1/8 are obtained by implementing the flow of different supply current levels through both windings.

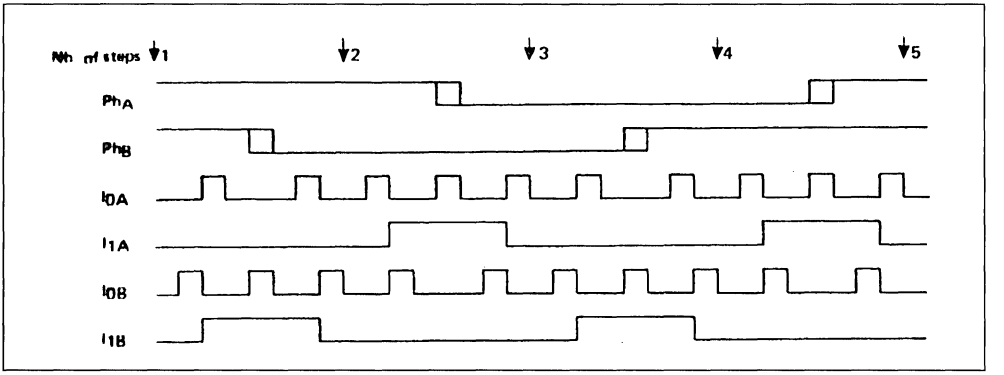
This type of operation may be envisaged if a good rotational regularity is required.

Some factors reduce the positioning precision of micro-steps :

- difference between theoretical value and available value for winding current,
- comparator threshold levels dispersion,
- motor winding characteristics dispersion.

These factors don't affect full-step position

Figure 7 : Signals to Provide to Controller for Rotation in 1/8th of a Step.



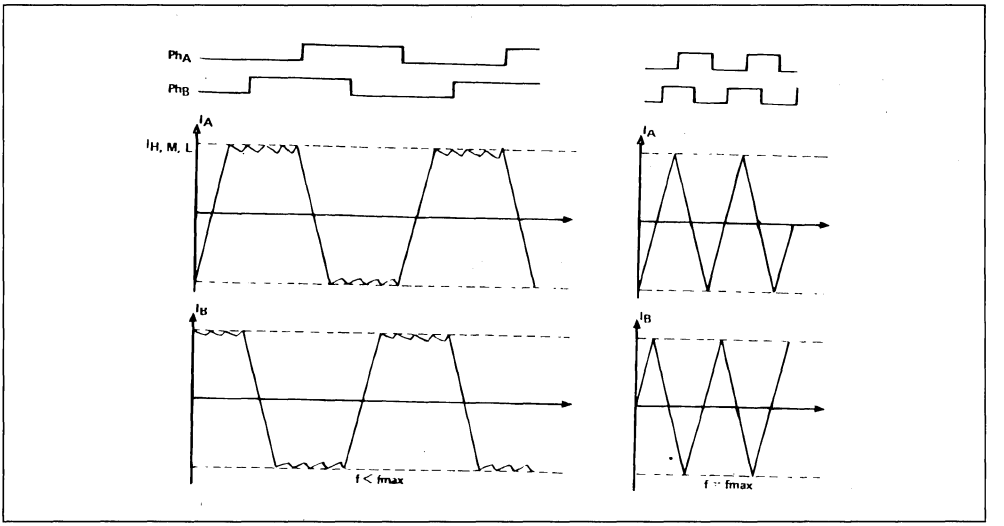
CHOICE OF OPERATING FREQUENCY

Motor's rotational speed is determinated by the frequency of Ph_A and Ph_B signals.

This speed is limited by the mechanical characteristics and the time constant of L, r circuit formed by the winding.

The rate of current increase in the winding depends on V_{mm}. Thus, if operation at maximum speed is desired, it would be a good practice to work with high supply voltages.

Figure 8 : Phase Currents for two Differents Speeds.



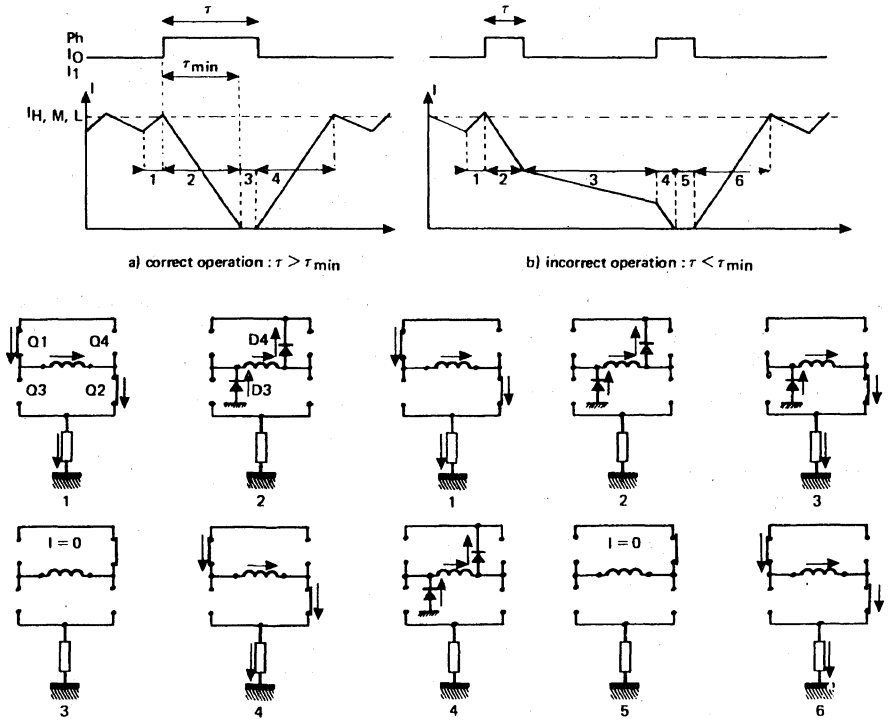
$I_1 = I_0 = Ph$ COMMAND

Simultaneous application of control signals to three inputs Ph, I_1 and I_0 (or to Ph and one of I inputs while the other is it at high level), is used for half-step operation or unipolar mode.

It must be ensured that the time t during which $Ph = I_1 = I_0 = 1$ is higher than the time t min required to annul the winding current.

If while the current is still positive, control signals $Ph : I_0 = I_1 = 1$ are applied to corresponding inputs, diode D2 or D3 will conduct and cause Q1 and Q4 to be turned-off, which prevents the current rise in the winding and disturbs the proper motor operation. Blocking of Q1 and Q4 is performed by a built-in protection unit and prevents the parasitics generated by the conduction of D2 and D3 to cause any short-circuit within the bridge.

Figure 9 : Operation with $Ph = I_1 = I_0$.



Normal circuit operation
——→ Direction of current flow.

1b, 2b Identical to 1a, 2a
3b : Q1 cut-off due of conduction of D3.
Slow decrease of current since.
$V_{MB} - V_{MA} = 0$ instead of being $- V_{mm}$.

4b ←→ 2b
5b ←→ 3a
6b ←→ 1b.

CHOICE OF T_{OFF} : SWITCHING TIME FOR CURRENT REGULATION

The value of t_{off} determines the quality of the current regulation in one phase.

The larger the t_{off}, the more important is the current ripple.

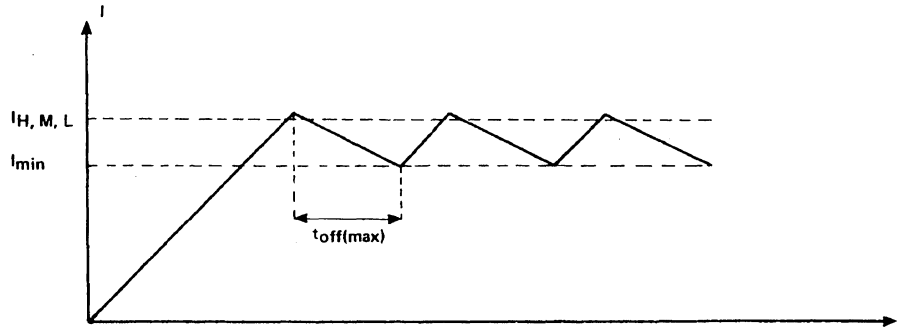
Value of t_{off} is found from the expression $t_{off} = 0.69 R_t.C_t$ where $1k\Omega \leq R_t \leq 100k\Omega$

A suitable value of t_{off} for the majority of applications is 30µs.

*$t_{off(max)}$

This is the t_{off} value over which the ripple value becomes excessive
Let's k be the desired ripple value and t = L/r.the time constant of motor winding, then :
$t_{off(max)}$ is given approximately by : $t_{off(max)} \approx kt$

Figure 10 : Winding Current @ off (max).



$$k = \frac{I_{H,M,L} - I_{min}}{I_{H,M,L}} \qquad t = \frac{L}{r}$$

$t_{off\,(max)} = kt$

*$t_{off(min)}$

This is the limit under which the current regulation is not guaranteed.

Even if the current continually exceeds the threshold levels I_H, I_M or I_L, the device will ensure a minimum conduction time $t_{on(min)}$ which is combination of two periods :

- t_d : comparator trigger time and transistor desaturation time implosed by TEA3717

- t'_d : this is the time required by V_C to reach the comparator threshold level and is determined by low pass filter R_C, C_C.

Therefore, t_{off} must be selected to be long enough to allow the current to fall to a level below I_H, I_M or I_L.

Supply voltage V_{mm} and winding characteristics both determine the value of $t_{off(min)}$.

Figure 11 : Winding Current @ $T_{OFF(MIN)}$.

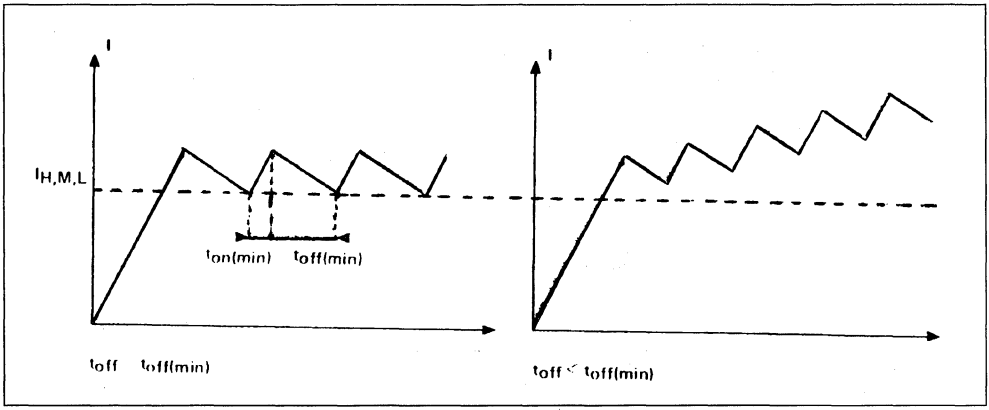
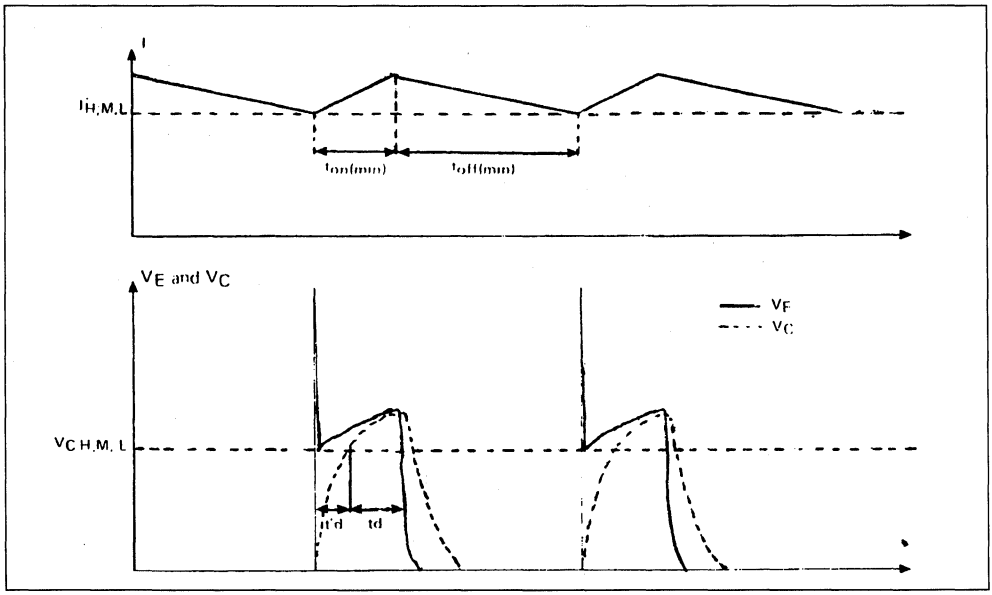


Figure 11 Bis : Winding Current, V_E and V_C Voltages @ $T_{OFF(MIN)}$.



SELECTION OF R_S VALUES

Three values of motor current I_H, I_M and I_L are determinated by the choice of R_S and V_R values.

The value of R_S is calculated such that $V_{CH} = R_S.I_H$

where $V_{CH} = \frac{0.42}{5}$

V_R and I_H is the maximum motor supply current.

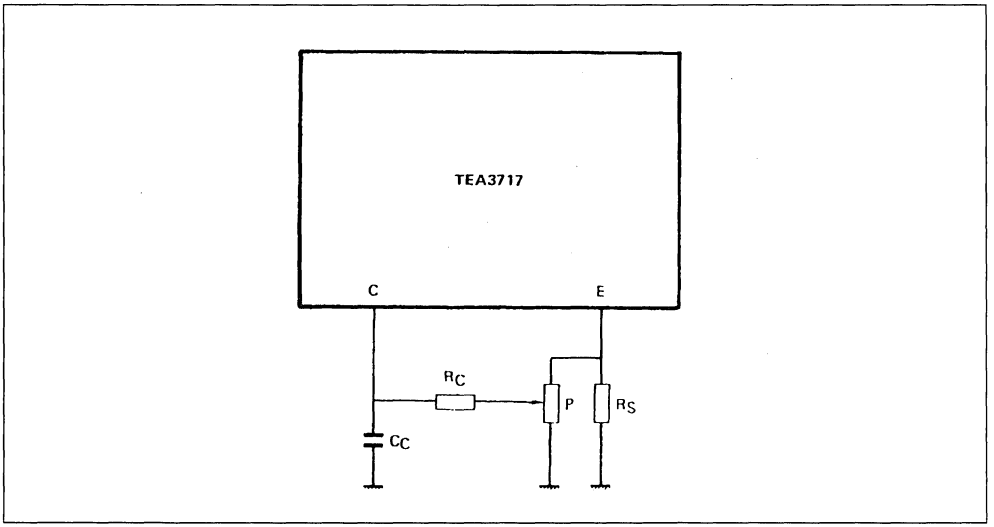
A choice of R_S value around 1Ω will guarantee a fast increase of the winding current and offers the possibility of operation with a voltage around 5 V for V_R, and thus is suitable for most applications.

It is also possible to vary the motor current in a continuous mode :

- by V_R adjustment
- by feeding back a portion of the voltage drop across R_S through a potentiometer whose wiper is connected to the comparator input.

In order to minimize the differential voltage V_E - V_C due to comparator's input current, care must be taken to avoid the appearance of a large impedance between E and C terminals. Appropriates values of P and R_C would be : P = 1 kΩ and R_C = 470Ω .

Figure 12 : Continuous Variation of Current Level.



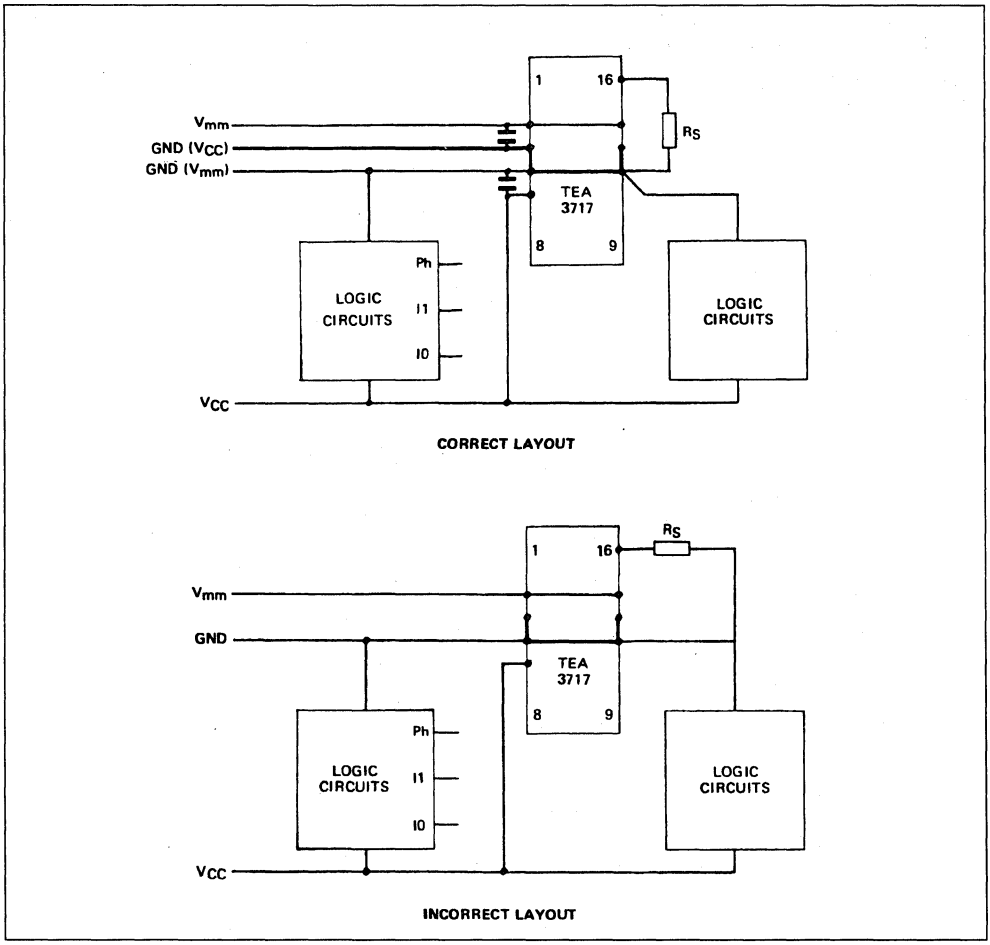
CABLING

Since the TEA3717 operates in switch mode, it is essential to take particular cabling precautions so as to avoid the generation of interferences susceptible to disturb the correct operation of the control electronics.

Recommended precautions are :

- Separated ground connection for V_{mm} supply
- Connection link between RS and the TEA3717 must be kept as short as possible
- Decoupling of V_{mm} by a ceramic capacitor (15 to 150nF) directly connected to the TEA3717 and also by an electrolytic of higher value : 10 to 22µF.
- Decoupling of V_{CC}.

Figure 13 : TEA3717 PC Board Layout.



SHORT CIRCUIT PROTECTION ON L6203

By G. SCROCCHI and G. FUSAROLI

With devices like L6203 used as driver often interfacing the external world by means of wires, can be easy to have short circuits.

A short circuit can occur for many reasons : a short on the load, a mistake during the connection of the wires between the device and the load (i.e. L6203 driving a motor), an accidental short between the wires and so on.

The outputs of L6203 are not protected against the short circuit and if a short occurs, the big amount of current flowing through the outputs can destroy the device.

To avoid this risk can be useful to add a circuitry to protect the device : in this case, to have a total protection, we must consider three types of short circuit :

1 - output to output short circuit
2 - output to supply voltage short circuit
3 - output to ground short circuit

The first step is to sense the short circuit current. In output to output (fig 1) or output to supply (fig 2) short circuit can be used the sensing resistor (Rsl) already used to set the current flowing in the load during the normal operation.

Figure 1.

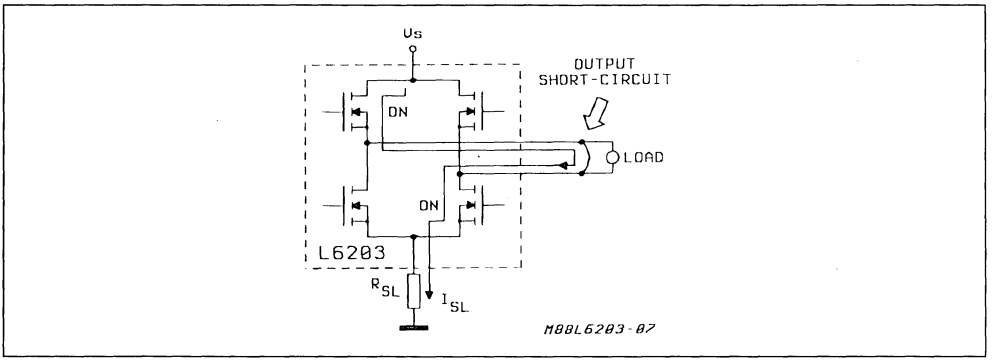
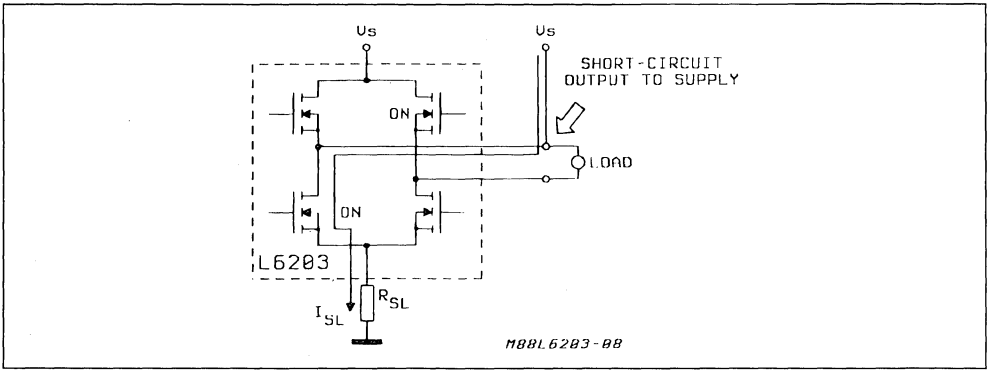
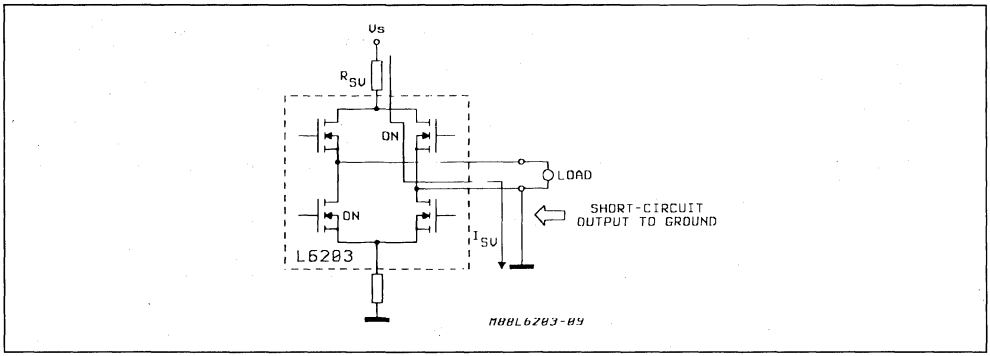


Figure 2.



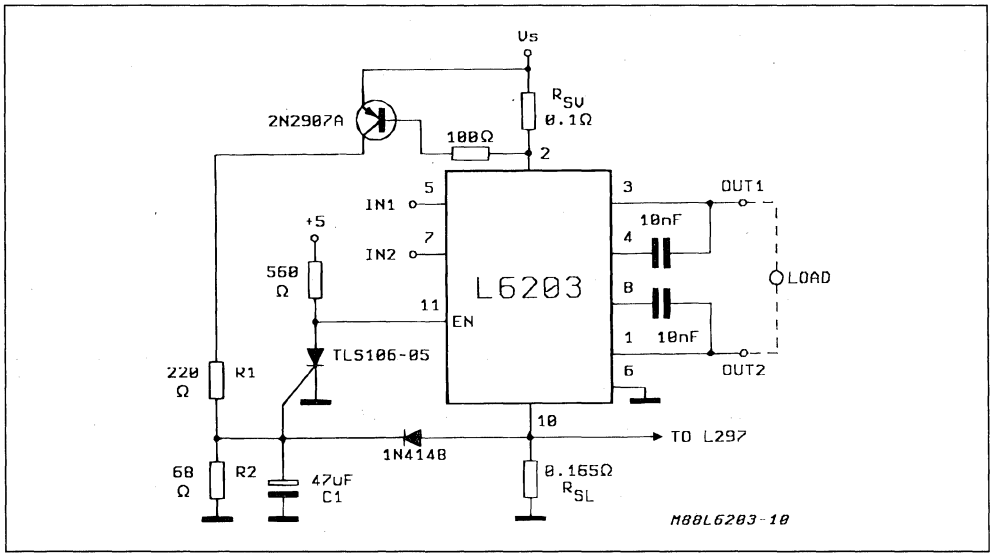
To sense the output to ground short circuit (fig 3) another sensing resistor (Rsu) must be added between the supply pin and the supply voltage.

Figure 3.



The second step is to create a threshold over which the value of the current must be considered as short circuit : for this way a transistor or a diode could be used.
The complete protection will be given by the ' or ' of the signal coming from the upper and the lower sensing circuitry ; this signal can be used to act on the ENABLE pin of the L6203 disabling the output stages.
A complete protection schematic diagram is shown in fig. 4.

Figure 4.



In normal operation the circuit works up to 3A/40V. When a short circuit occurs the SCR is triggered and L6203 disabled : due to the SCR memory L6203 is kept disabled until the power is switched off and then on, if the cause of short was removed.

The short circuit is detected when :

$$I_{SU} > \frac{V_{BE(T1)}}{R_{SU}} = \frac{0.6}{0.1} = 6A$$

$$I_{SL} > \frac{V_D + V_{THSCMT}}{R_{SC}} = \frac{0.6 + 0.7}{0.165} = 7.8A$$

The effective short circuit peak current is greater than Isu and Isl : this is due to the high dI/dT during the short and to the delay between the short circuit detection and the ENABLE intervention :

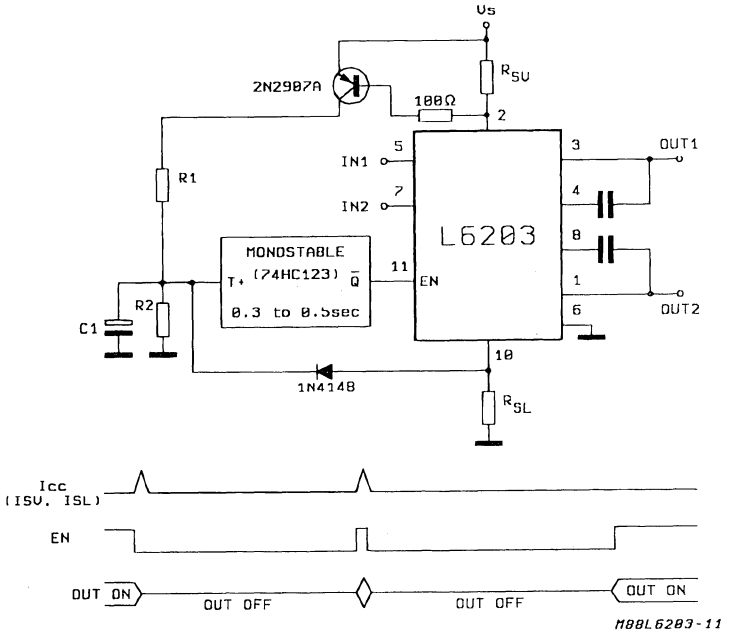
Rsu and Rsl must be non inductive resistors.

R1 and R2 are used to scale the signal when the transistor goes on and in conjunction with C1 to filter the short circuit signals in order to avoid false trig ger of the SCR : this filtering should not be too much heavy to avoid to introduce an excessive delay in the short circuit loop.

Isu and Isl must be calculated at the effective operating temperature being the Vbe and Vd temperature dependent.

Instead of the SCR, a monostable with a long time constant (0.3 ÷ 0.5 sec) can be used : in the case, every time a short circuit occurs, L6203 is disabled for the monostable time constant and then enabled, if the short is still present L6203 is disabled again, if the short was removed L6203 returns in normal operation (fig 5).

Figure 5.



R_1, R_1, C_1, R_{SU}, R_{SL} are choosen depending on the application.
The intervention of the protection circuit is determined by

$$I_{SU} > \frac{V_{BE}}{R_{SU}}$$

$$I_{SL} > \frac{V_{IH} + V_D}{R_{SL}}$$

$V_D = V_{DIODE}$

V_{IH} = min VInput High T+ Monostab

CONTROLLING VOLTAGE TRANSIENTS IN FULL BRIDGE DRIVER APPLICATIONS

by Thomas L. Hopkins

In applications that involve fast switching of inductive loads, designers must consider the voltage transients that are generated in such applications. To insure a reliable design, the voltage transients must be limited to a level that is within the safe operating conditions of the switching device. This application note discusses the sources of voltage tran-sients in full bridge applications and techniques that can be used to limit these over-voltage conditions to safe levels. Special attention will be given to applications using monolithic implementations of full bridge circuits like the SGS-THOMSON L6202 and L6203.

MAXIMUM RATINGS

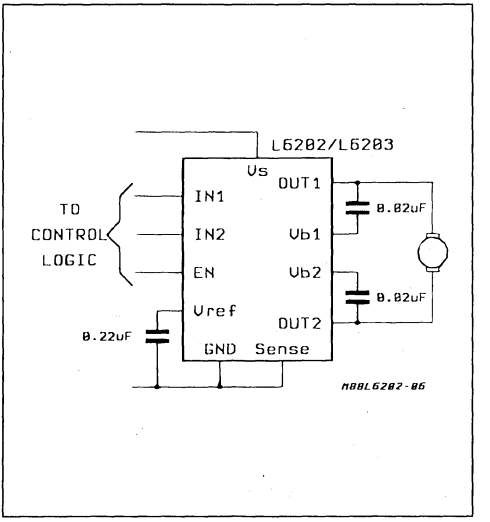
The maximum voltage rating for the bridge driver can be derived from the maximum ratings of the devices used in the output stage and are generally the BV_{ceo} or BV_{dss} of the power devices. In addition to the maximum allowable voltage across the output device, additional limits may be needed on the maximum output voltage above supply or below ground, depending on the implementation of the output stage.

As an example of a full bridge circuit, consider the SGS-THOMSON L6202 and L6203. These devices are full bridge drivers implemented with DMOS transistors on a monolithic structure. Using these devices full bridge drive circuits, like shown in figure 1, are easily implemented. The device has a maximum rating for the supply voltage of 60V, which implies a maximum BV_{dss} for the output devices of 60V. In addition, due to the monolithic implementation, the voltage between the two output terminals must not exceed 60V. Therefore, the maximum ratings that must be considered for the application are :

V_{supply}	60V
V_{ds} any output	60V
V_{01} - V_{02} :	60V

Similar maximum ratings will exist for any full bridge application, with the exception of the differential output voltage limit, which will not exist for discrete implementations.

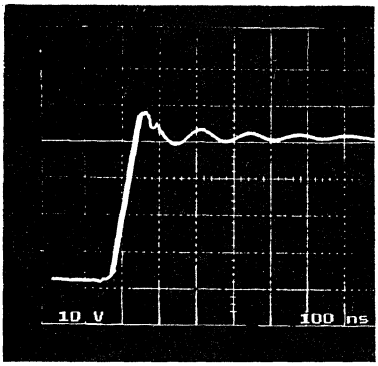
Figure 1 : DC Motor Drive Circuit using L6203.



SOURCES OF VOLTAGE TRANSIENTS

To protect against the over-voltage that may occur as a result of the inductive property of the load, voltage clamps are normally employed to limit the voltage across the output devices. In bridge applications these clamps are normally a diode bridge that clamps the voltage to one diode drop above supply and one diode drop below ground. However, if the diode switches slower than the transistor, there is a short time where neither the transistor nor the diode is conducting and the voltage rise is limited only by the capacitance on the node. The result is that a vol-tage overshoot occurs during the time before the diode turns on. When the bridge is build with DMOS power transistors, the intrinsic body diode is often used as the clamp. This is true for the L6202 and L6203. As can be seen in the figure 2, the turn-off time of the DMOS device in the L6203 is in the range of 25 to 50nS while the turn-on time of the intrinsic drain to source diode is in the range of 150nS. This difference in switching time is characteristic of many DMOS devices.

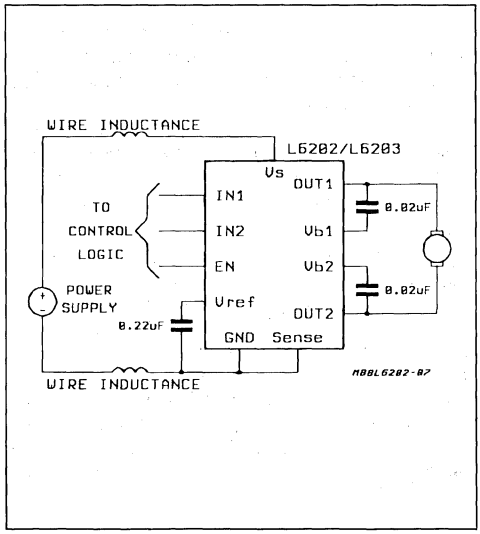
Figure 2 : Output Switching Waveform for L6203.



The second main factor contributing to the transients is the parasitic inductance in the wiring or printed circuit board layout. Figure 3 shows the parasitic inductances in the DC motor application. When the current flowing in these parasitic inductances is rapidly switched, the inductive property of the wire causes a voltage transient. When large currents are rapidly switched, as with DMOS transistors, large voltage transients can be induced across even small parasitic inductances. For an inductive load driven by an H-Bridge the change of current in the power supply lead is equal to twice the load current when the bridge is switched off or the bridge is switched from one diagonal pair of transistors being on the other pair. Here switching the bridge results in a change of direction of current flow in the power leads. The time that it takes to switch the current is essentially the turn off time of the output device. In this case the resulting voltage across the inductance is given by the equation :

$$v = L\,di/dt = \frac{L_2 \times I1}{Toff} \qquad (1)$$

Figure 3 : Parasitic wiring Inductances in DC Motor Drive Circuit.

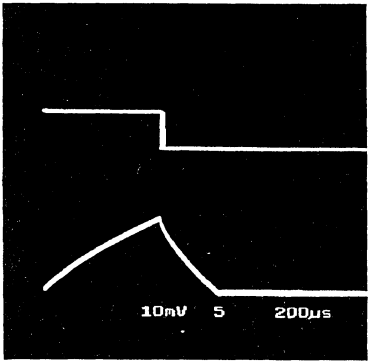


In fast switching applications, like the L6202, where the switching time is as short as 25nS, the induced voltage spike can become quite large. For example if the DC motor in figure 3 was driven with 4A and the bridge was switched off, a parasitic inductance of only 15nH would produce a 5V spike. Since the current is reversed in both the supply and ground leads the device would see a 10V spike between the power supply pin and chip ground, if the inductance of both wires were the same.

As a design example, consider a DC motor driver shown in figure 1 with the following system characteristics :

Supply Voltage	Max 46V Min 38V
Peak Motor Current	5A
Chopping Frequency	50kHz

Figure 4 : Enable Input and Motor Current for Examples.



For evaluation, the motor will be driven with a peak current of 4A. Figure 4 shows the input signals for the L6202 and the motor current used in the evaluation.

Here the bridge is energized and the load current is allowed to build up to 4A. When the 4A peak is reached, the bridge is disabled and the current decays through the intrinsic diodes in the DMOS power stage. All figures in the remainder of this note are taken under these operating conditions.

POWER SUPPLY FILTERING

To reduce the effect of the wiring inductance a good high frequency capacitor can be placed on the board near the bridge circuit to absorb the small amount of inductive energy in the leads. It should be noted that this capacitor is usually required in addition to an electrolytic capacitor, which has poor performance at high frequencies.

Operating Voltages.

Figure 5a : Supply Voltage.

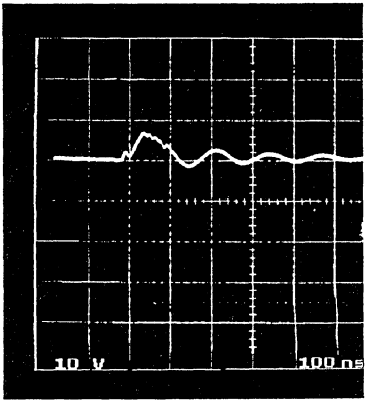
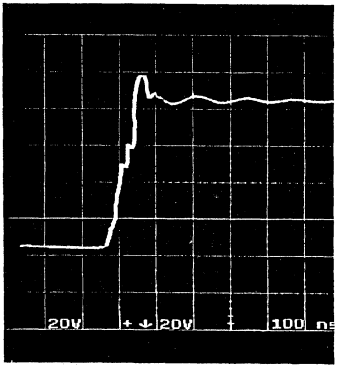


Figure 5a shows the spike on the power supply pin of the L6203 and the output pins when the bridge was disabled. These waveforms were present when the device was mounted on a printed circuit board where reasonable care was taken in the layout. When a 0.2µF polyester capacitor was connected between the supply and ground pin of the L6203 the voltage spike on the power supply was significantly reduced, as shown in figure 6a.

Figure 5b : V01 - V02.



Looking at the voltage waveform at the output terminals of the L6202, shown in figure 6b, a large spike is still present. The worst case spike is measured between the output terminals of the device (V_{out1} - V_{out2}) since the spikes above the supply and below ground are both present. After the voltage spike on the power supply was eliminated, the tran-sients on the output must be related to the mismatch of switching times between the diodes and power transistors. To control these spikes two possible alternatives are present ; 1) use faster diodes, or 2) use an external circuit to slow the voltage rise time across the output when the transistors are turned off. Schottky diodes connected external to the L6203 would more closely match the switching time of the DMOS power transistors, but are expensive and require additional board space.

Operating Voltages with 0.2µF Bypass Capacitor on Supply Pin.

Figure 6a : Supply Voltage.

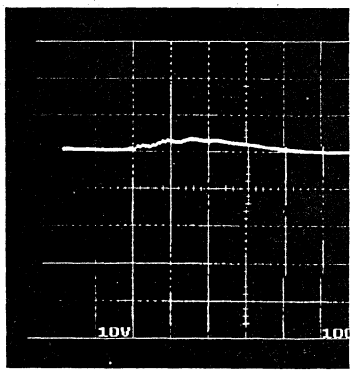
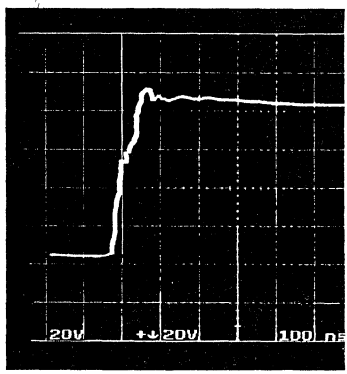


Figure 6b : V01 - V02.

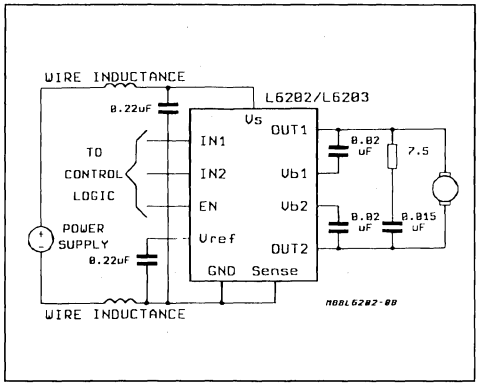


Slowing down the output voltage rise time can be accomplished by connecting a snubber network across the output ter minals of the device. Figure 7 shows the connection for a RC snubbing circuit used with the L6203. With properly selected values the slope of the voltage waveform can be limited to where the diodes have sufficient time to turn on and clamp the remaining inductive energy.

SNUBBER DESIGN CONSIDERATIONS

The function of the snubber network is to limit the rate of change of the voltage across the motor (output terminals of the L6203) when one of the DMOS devices is turned off. Using the RC snubbing circuit shown in figure 7, the rate of change of the voltage on the output is dominated by the capacitor while the resistor is used primarily to limit the peak current flowing through the power transistor when it turns on.

Figure 7 : DC Motor Drive Applications with Snubber Network and Bypass Capacitor.



The time constant of the motor current is much longer than the switching time, due to the inductance of the motor. At the time of switching the DC motor can be assumed to be a constant current generator equal to the peak current at switching. If this current is switched into the snubber, the voltage across the snubber network will jump to a value equal to the snubber resistance times the motor current. After the initial step, the rate of change is limited by the motor current charging the snubber capacitor.

To properly size the snubber network the resistor is selected such that the maximum motor current will produce a voltage less than the minimum power supply voltage. If the resistor is larger than this value, the snubber will be ineffective since the capacitor will not limit the voltage rise until the voltage has become greater than the power supply. For the de-sign example, the maximum resistance for the snubber is given by the equation :

$$R_{max} = V_{smin}/I_{peak} = 38V/5A = 7.6\ Ohm \quad (2)$$

The snubber capacitor is calculated from the peak current and the target rise time. The capacitance is given by the equation :

$$C = I_{peak}\ dt/dv = 5A\ 150nS/50V = 0.015\mu F \quad (3)$$

When the snubber network is installed in the application the voltage transients on the terminals of the L6203 are greatly reduced, as shown in figure 8.

The drawback of a snubber network of this type is that a current spike will flow into the transistor when it is switched on as the capacitor is discharged. The theoretical peak value of this spike is given by the equation :

$$I = V_{smax}/R = 42V/7.5Ohm = 5.6A \quad (4)$$

Operating Voltages with Snubber Network and By-pass Capacitor.

Figure 8a : Sypply Voltage.

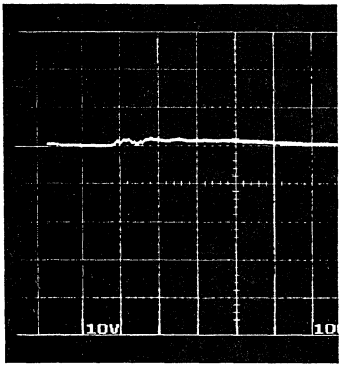
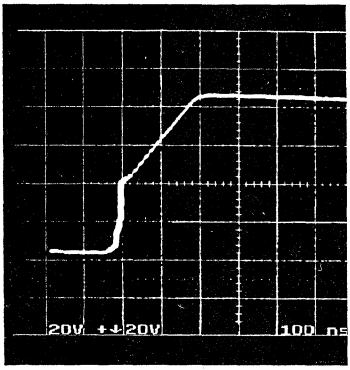
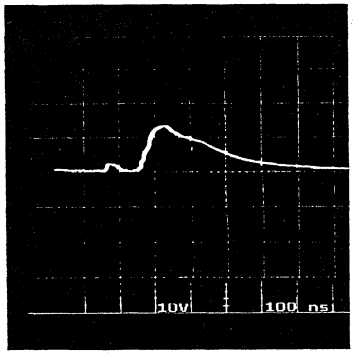


Figure 8b : V01 - V02.



This peak current flowing in the snubber is added to the load current when the device is turned on and the total peak current in the transistor is the sum of the snubber circuit current plus the load current. In practice the peak current measured is usually much less than the calculated peak, due to the capacitors internal resistance and inductance and the resistor inductance. Figure 9 shows the peak current in the snubber network in the design example.

Current in the Snubber Circuit.
Figure 9a : Turn on 2.0A/div.



The power dissipated in the snubber resistor is the sum of the dissipation during the turn-on and turn-off of the bridge. The resistor dissipation is :

$Pd = (I1^2 \cdot R \cdot DC) + (I2^2 \cdot R \cdot DC)$ (5)

where

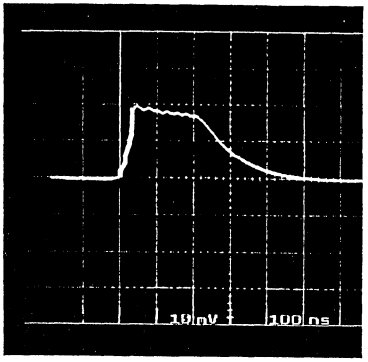
I_1 = Current at turn-on
I_2 = Current at turn-off
R = Snubber resistor
DC = Duty Cycle of current flow

For the design example the power dissipation, not considering the duty cycle is :

$Pd = ((2.5)^2 \cdot 7.5 \cdot .01) + ((5)^2 \cdot 7.5 \cdot 0.01)$
$= 0.469 + 1.875$
$= 2.344$ W (6)

If the device is chopping for only a portion of the time the dissipation in the resistor will be reduced.

Figure 9b : Turn off 2.0A/div.



CONCLUSION

With the 0.2µF bypass capacitor and the snubber circuit in place the voltage transients measured in the application have been limited to within safe values for the L6202. As shown in figure 8, the power supply voltage, the voltage across each of the DMOS transistors and the voltage across the output of the bridge (Vout1 - Vout2) are all within the maximum rating of the device with some margin.

SUMMARY

To insure reliable performance of a H-bridge drive circuit, the designer must insure that the device operates within the maximum ratings of the device(s) used in the circuit. One of the critical parameters to consider is the maximum voltage capability of the devices. To maintain the reliability, the voltage transients due to switching inductive loads must be maintained within the ratings of the device.

Two techniques used to control the voltage transients in fast switching applications are proper bypass filtering of the power supply and snubbing the outputs to control voltage rise times. Using these two techniques the voltage transients in a DMOS bridge application can be controlled to within safe levels.

A HIGH EFFICIENCY, MIXED-TECHNOLOGY MOTOR DRIVER

By C. CINI

A new mixed technology called Multipower-BCD allows the integration of bipolar linear circuits, CMOS logic and DMOS power transistors on the same chip. This note describes a H-bridge motor driver IC realized with this technology.

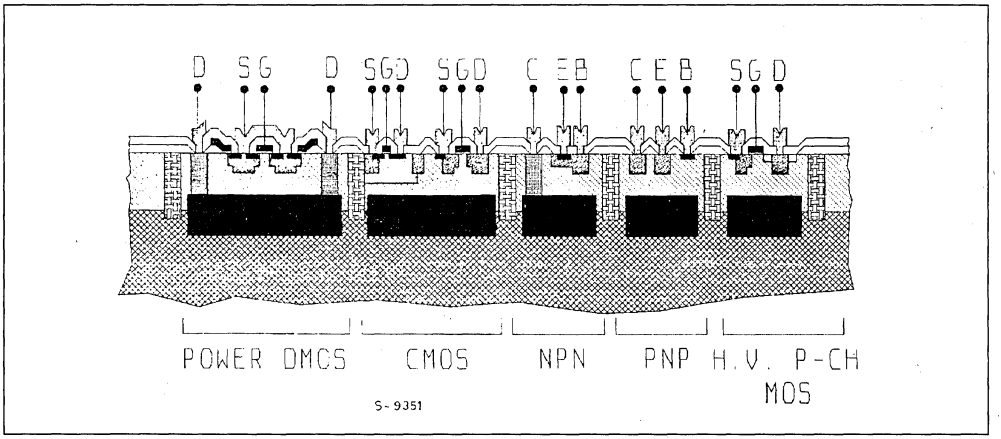
The miniaturization and integration of complex systems and subsystems has led in recent years to the implementation of monolithic circuits integrating logic functions and power sections.

For these applications SGS–THOMSON Microelectronics has developed a new technology called Multipower BCD which allows the integration on the same chip of isolated Power DMOS elements, bipolar transistors and C-MOS logic.

Thanks to high efficiency, fast switching speed and the absence of secondary breakdown, this technology is particularly suitable for fast, high current solenoid drivers and high frequency switching motor control. The free-wheeling diode intrinsic to the DMOS structure (necessary if the device drives an inductive load) and the great flexibility available in the choice of the logic and driving section components allow the complete integration of power actuators without further expense in silicon area-and a compact implementation of complex signal functions.

This technology has been applied to produce a switching power driver - the L6202/3 - capable of delivering 4A per phase, which is suitable for speed and position control in D.C. motor applications.

Figure 1 : A Schematic Cross Section of Bipolar, C-MOS, DMOS Structures (BCD).



MULTIPOWER BCD TECHNOLOGY

Multipower BCD technology combines the well known vertical DMOS silicon gate process, used for discrete POWER MOS devices, and the standard junction isolation, sinker and buried layer process. The architecture of the process is centred around the vertical DMOS silicon gate, a self aligned structure, which guarantees short channel length (1.5 µm) with consequent low $R_{DS(ON)}$ for the device.

In standard IC technologies the voltage capability is determined essentially by the thickness of the epitaxial layer and it is the same for signal and power components. But if the epi thickness is increased to allow the inclusion of high voltage transistors even the linear dimension of small signal transistors must be increased proportionally. In contrast MULTIPOWER BCD permits the realization of high voltage lateral DMOS structures in an epi-layer dimensioned for low voltage bipolar linear elements. Thus

it is possible to mix on the same die very dense CMOS logic, high precision bipolar linear circuits, very efficient DMOS power devices and high voltage lateral DMOS structures.

In this way the constraints which limit the complexity of signal processing circuits that can be integrated economically on a high chip are greatly reduced.

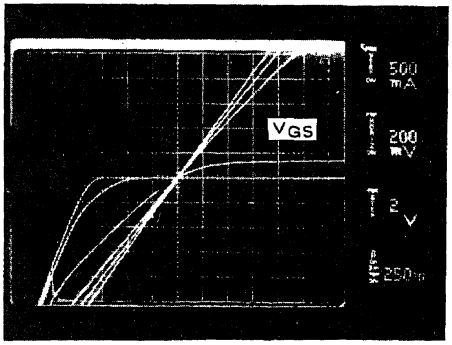
The active structures available in Multipower BCD technology are represented in fig. 1.

Within the vertical DMOS is indicated an intrinsic diode that can operate as a fast free-wheeling diode in switch mode applications. In fact DMOS, as a result of the way by which it is realized, is almost a symmetrical bidirectional device. That is, it can operate with the electrical I-V characteristic shown in the 3rd quadrant of fig. 2 ; that is, as a controlled resistor of value decreasing inversely with the gate source voltage applied to the power to which it is associated, up to a minimum equal to the $R_{DS(ON)}$ of the device itself, shunted by the body-drain diode intrinsic to the structure that limits the negative excursion of V_{DS}. Of the devices represented in fig. 1 the table 1 lists the electrical characteristics.

Table 1 : Devices in Multipower BCD Technology.

• Vertical DMOS	BV_{DSS} > 60 V	$V_{TH} \cong 3$ V	f_T > 1 GHz
• Lateral DMOS	BV_{DSS} > 100 V	$V_{TH} \cong 3$ V	f_T > 800 MHz
• P-channel with Drain Extension	BV_{DSS} > 85 V	$V_{TH} \cong 3$ V	f_T > 200 MHz
• Bipolar NPN	LV_{CEO} > 20 V	ß = 35	f_T > 300 MHz
• Bipolar PNP	LV_{CEO} > 20 V	ß = 20	f_T > 7 MHz
• C-MOS N and P-channel	BV_{DSS} > 20 V	$V_{TH} \cong 3$ V	

Figure 2 : I-V Characteristic of DMOS N-channel Power Device.



THE L6202 & L6203 H-BRIDGE DRIVERS

Using this technology a H-bridge IC has been realized which accepts TTL or C-MOS compatible signals and is suitable for high efficiency, high frequency switching control of DC and stepping motor. The power stage consists of four DMOS N-channel transistors with $R_{DS(ON)} \cong 0.3\ \Omega$.

When this device is supplied with the maximum voltage of 60V it can deliver a DC current of 1.5A in a standard DIP.16 (L6202) and up to 5A in a MULTIWATT package (L6203).

The device can also operate with a peak current of 8A for a time interval essentially determined by the time constant of heat propagation (< 200ms).

The system diagram representing the internal function blocks and external components (outside the dashed line) is shown in fig. 3.

The integrated circuit has 3 Inputs : Enable, Input 1, Input 2. When Enable is "low" all power devices are off ; when it is "high" their conduction state is controlled by the logic signals Input 1 and Input 2 that drive independently a single branch of the full bridge. When Input 1 (Input 2) is "high" DMOS 1 (DMOS 1') is "on" and DMOS 2 (DMOS 2') is "off", when is "low" DMOS 1 (DMOS 1') is "off" and DMOS 2 (DMOS 2') is "on".

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150 °C. When the thermal protection is removed the device restarts under the control of the Input and Enable signals.

ON-OFF SYNCHRONIZATION CIRCUIT

ON-OFF synchronization of the power devices located on the same leg of the bridge must prevent simultaneous conduction, with obvious advantages in terms of power dissipation and of spurious signals on the ground and on sensing resistors.

Because of the very short turn-on, turn-off times characteristic of POWER MOS devices a dead time (time in which all power transistors are "off") of 40 ns is sufficient to prevent rail-to-rail shorts. The circuit that provides this time interval is shown in fig. 4 with the voltage waveforms that explain how it works. Let us suppose Enable = "high". Because of the delay times introduced by INV1 and INV2, V2 and V3 are two waveforms contained one in the

Figure 3 : L6202-6203 Block Diagram.

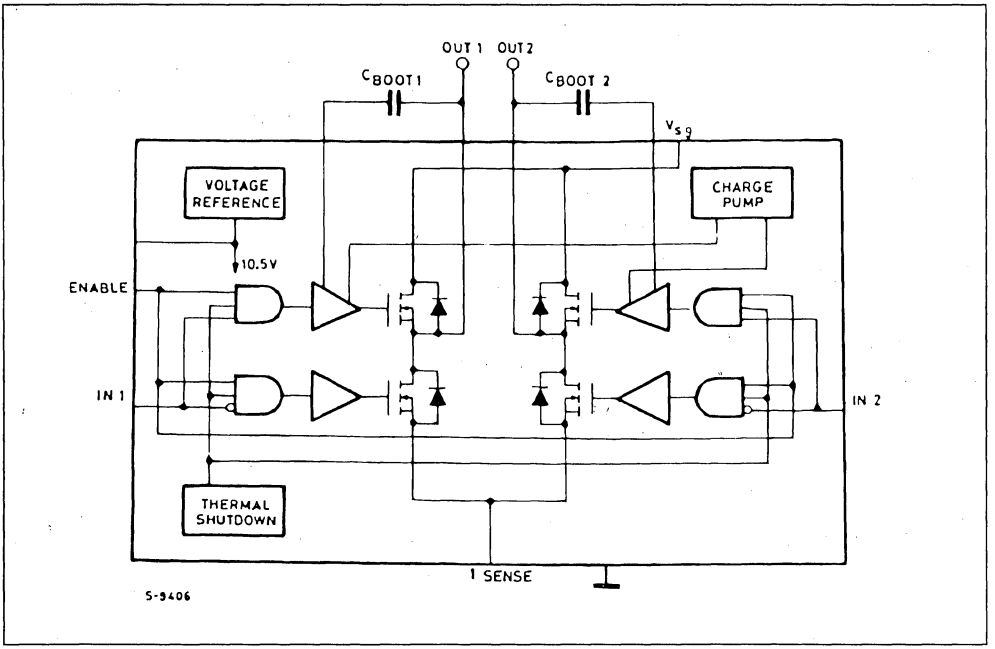
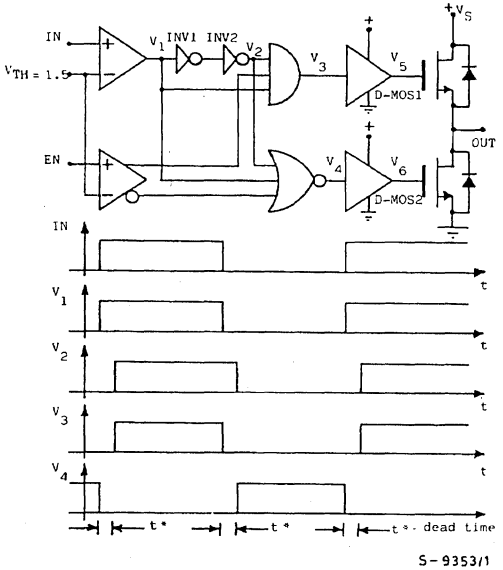


Figure 4 : A Schematic Representation of ON-OFF Synchronism Circuit.

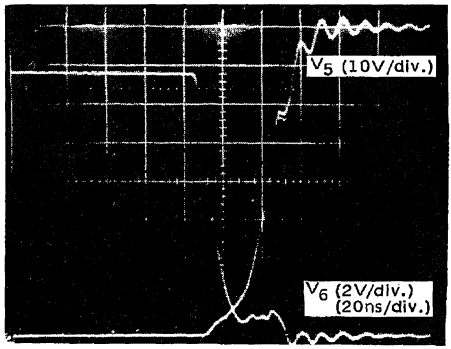


other and of polarity suitable to assure that the turn-on of a power transistor happens only after the turn-off of the other. The gate voltages V5 and V6 of DM1 and DM2 are represented in fig. 5. In fig. 3 we can see also the modality of operation of the Enable signal, charge pump and bootstrap circuits.

Concerning POWER MOS driving, it must be noted that it is necessary to assure to all DMOS N-channel a gate-source voltage of about 10V to guarantee full conduction of the POWER MOS itself. While there are no particular problems for driving the lower POWER MOS device (its terminals is referred to ground) for the upper one it is necessary to provide a gate voltage higher than the positive supply because it has the drain connected to the positive supply itself.

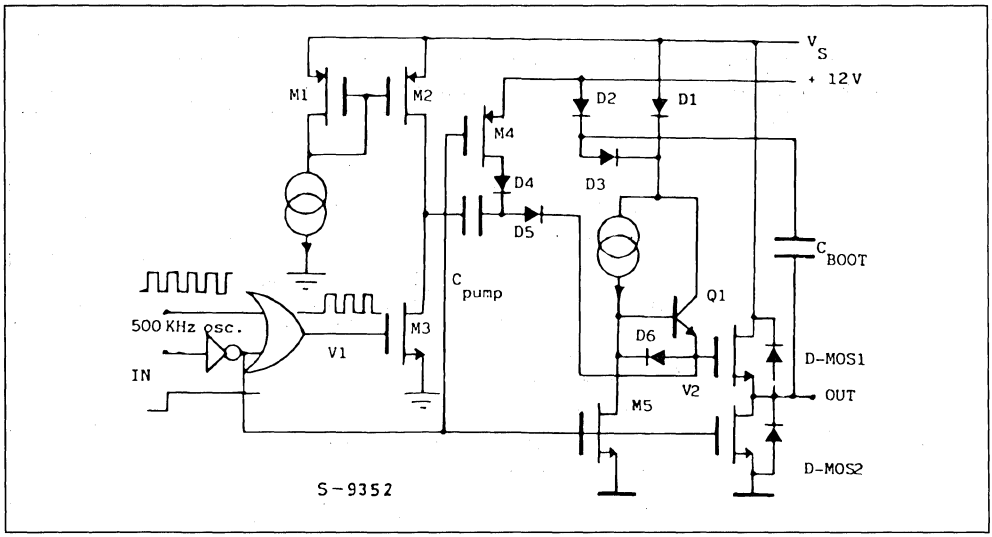
This is obtained using a system that combines a charge pump circuit, that assures DC operation, with a bootstrapping technique suitable to provide high switching frequencies. The circuit that satisfies to all these requirements is represented in the schematic diagram of fig. 6.

Figure 5 : POWER MOS Gate Voltage Waveforms.



In the description of this circuit we can assume that C_{BOOT} is absent and IN commutes from the "low" to the "high" level.

Figure 6 : Schematic Representation of Charge PUMP and BOOSTRAP Circuit used to Drive the Gate of the Upper DMOS Device.



In this condition, by means of D1, the circuit charges immediately the DMOS1 gate capacitance to V_S while the charge pump, activated by the signals IN = "low", as it can be seen in fig. 7, must supply only a voltage of about 10V.

In the switching operation it will be C_{BOOT} that guarantees a faster turn-on of the upper POWER MOS and consequently high commutation frequencies.

In fact during the period in which DMOS2 is "on" C_{BOOT} is charged to a voltage of about 12V.

When V_{out} raises because DMOS2 is disactivated D2 and D1 became "off" while D3, that remains "on"

connects the gate circuit to C_{BOOT} that raises higher than V_S and makes DMOS1 full "on" in a very short time interval (20 ns).

It must be noted that the switch M4 in the fig. 6 circuit, driven by a complementary phase respect to M3 disconnects D4, D5 and D6 from 12 V when M5 goes "on" to assure the "turn-off" of DMOS1.

Figure 7 : Charge PUMP Abilitation Signal and Gate Voltage of DMOS Upper Device.

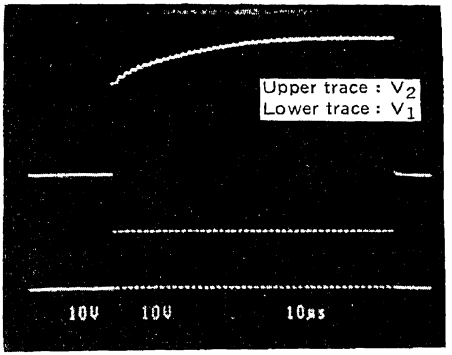
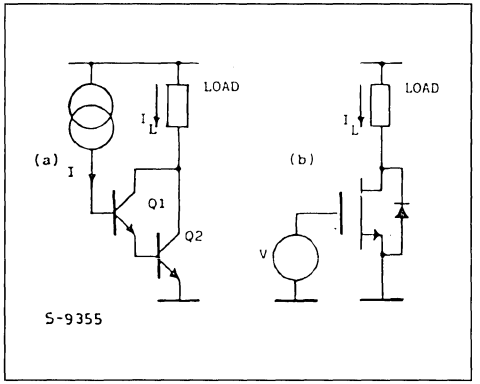


Figure 8 : Darlington Bipolar and DMOS Power Stages.



PERFORMANCE

One of the most important features is the very high efficiency achieved.

To appreciate the benefits of low power dissipation, and consequently of high efficiency, of a circuit realized in DMOS technology we must refer to the equivalent bipolar solution and also consider separate DC and AC operation.

Consider the typical Darlington power stage frequently used in integrated circuit and a DMOS power stages both represented in fig. 8.Neglecting the power dissipation in the driving section, in static conditions, the total dissipation of the two stages when they are "on" is in the case (a) :

$$P_{d(a)} = (V_{CESAT1} + V_{BE2}) \times I_L$$

and in the case (b) :

$$P_{d(b)} = R_{DS(ON)} \times I_L^2$$

where I_L is the load current.

Because the saturation loss of a power DMOS transistor can be reduced by increasing the silicon area it is possible to satisfy the condition

$$R_{DS\text{-}ON} \times I_L < (V_{CESAT1} + V_{BE2})$$

and then to obtain lower dissipation.

Concerning to the driving section, an other essential difference must be emphaisised.

While in case (a) during the time in which the power is "ON" it is necessary to supply a current for maintaining Q1 saturated, in the case (b) power is dissipated only during the commutation of the gate voltage.

About AC operation, it must be noted that the greatest advantage, always in terms of power dissipation, is due to the inherently fast turn-on, turn-off times of power MOS devices. In fact, if we suppose that the load is of inductive type and that the current waveform is triangular on the voltage commutation of the output, the total power dissipation is :

$$P_d = V_S \, I_L \, T_{COM.} \, f_{SWITCH}$$

where : V_S = Supply voltage, I_L = Peak load current,
$T_{COM.} = T_{TURN\text{-}ON} = T_{TURN\text{-}OFF}$,
f_{SWITCH} = Chopper frequency.

Because $T_{COM.}$ in DMOS case is ≤ than in bipolar case at a fixed frequency we have a lower dissipation or at fixed dissipation we can tolerate higher switching frequency.

Considering all these aspects, with a power device consisting of about 2200 cells we have realized DMOS power devices characterized by $R_{DS(ON)}$ 0.3 Ω and by switching times t_r, t_f of 50 ns. Other characteristics of the device when is configured as shown in fig. 9 are listed in table 2.

Fig. 10 shows the supply current with no load, vs. switching frequency.

Figure 9.

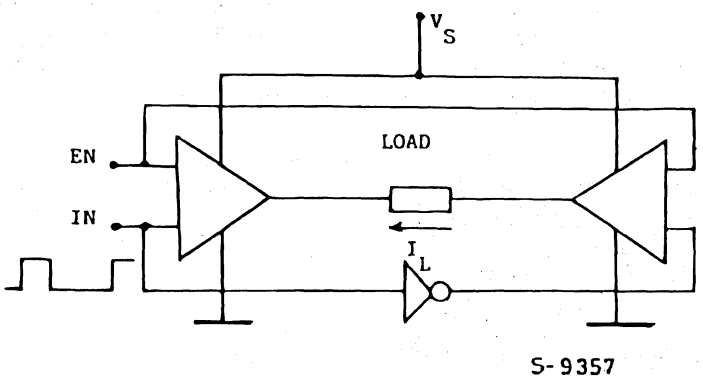
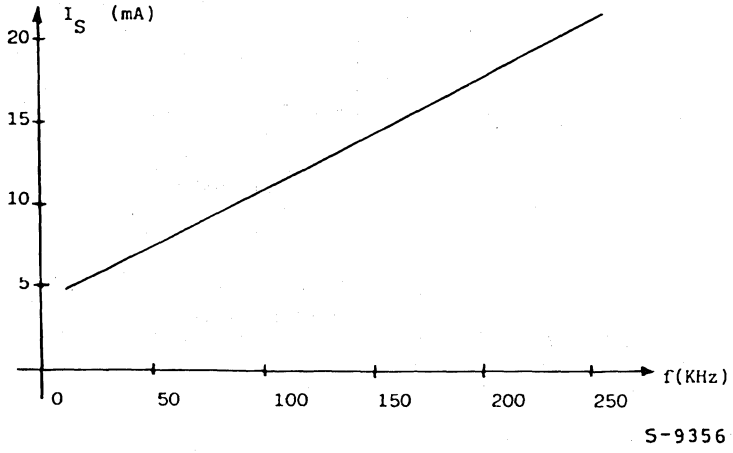


Table 2 : Main Features of L6202/6203.

• V_S (maximum supply voltage)		=	60 V
• I_L (maximum output current)		=	1.5 A DIP.16
		=	5 A MULTIWATT Package
• Efficiency	η	=	90 % (I_L = 1.5 A, $f_{chopper}$ = 50 KHz, V_S = 54 V)
• Power Dissipation	P_d	=	1.5 W
• t_d (turn-on, turn-off propagation delay)		=	100 ns

Figure 10.



STEPPER MOTOR DRIVING

By H. SAX

Dedicated integrated circuits have dramatically simplified stepper motor driving. To apply these ICs designers need little specific knowledge of motor driving techniques, but an under-standing of the basics will help in finding the best solution. This note explains the basics of stepper motor driving and describes the drive techniques used today.

From a circuit designer's point of view stepper motors can be divided into two basic types : unipolar and bipolar.

A stepper motor moves one step when the direction of current flow in the field coil(s) changes, reversing the magnetic field of the stator poles. The difference between unipolar and bipolar motors lies in the may that this reversal is achieved (figure 1) :

Figure 1a : BIPOLAR - with One Field Coil and Two Chargeover Switches That are Switched in the Opposite Direction.

Figure 1b : UNIPOLAR - with Two Separate Field Coils and are Chargeover Switch.

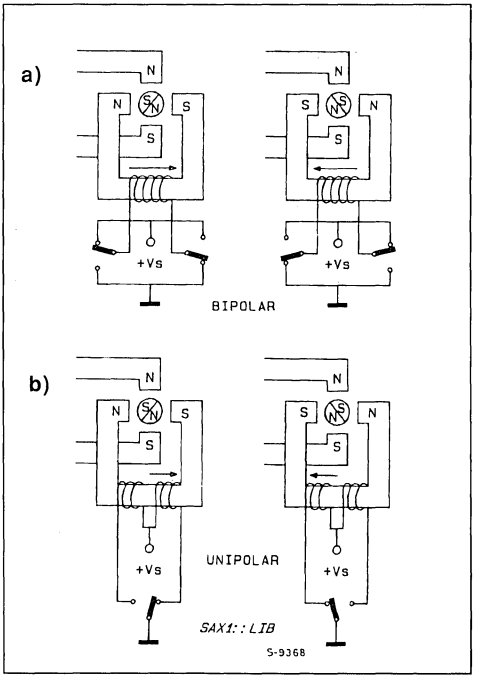
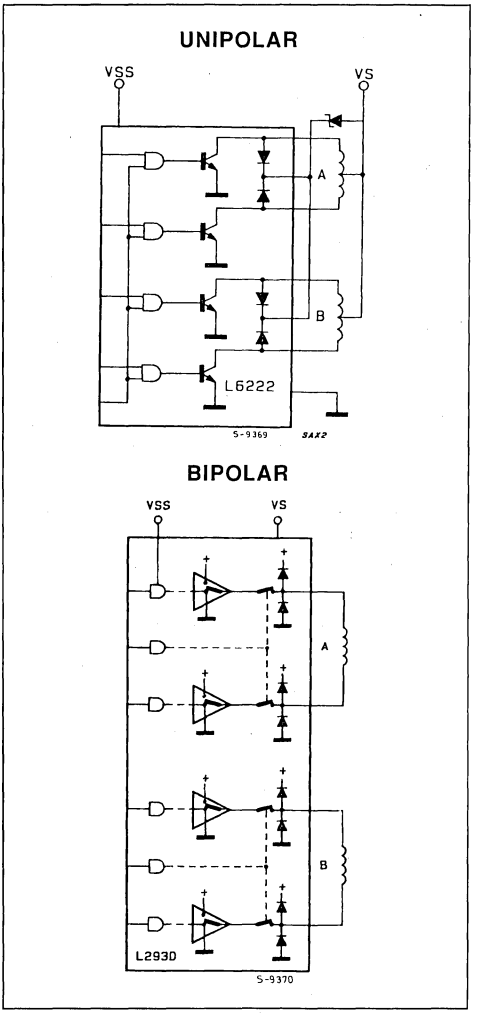


Figure 2 : ICs for Unipolar and Bipolar Driving.



The advantage of the bipolar circuit is that there is only one winding, with a good bulk factor (low winding resistance). The main disapuantages are the two changeover switches because in this case more semiconductors are needed.

The unipolar circuit needs only one changeover switch. Its enormous disadvantage is, however, that a double bifilar winding is required. This means that at a specific bulk factor the wire is thinner and the resistance is much higher. We will discuss later the problems involved.

Unipolar motors are still popular today because the drive circuit appears to be simpler when implemented with discrete devices. However with the integrated circuits available today bipolar motors can be driver with no more components than the unipolar motors. Figure 2 compares integrated unipolar and bipolar devices.

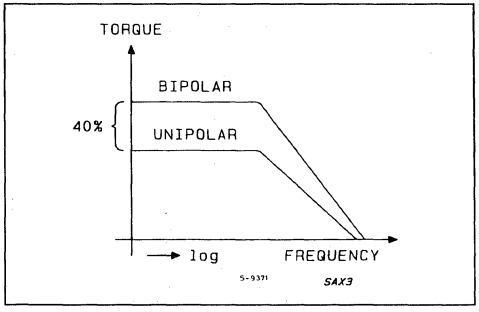
BIPOLAR PRODUCES MORE TORQUE

The torque of the stepper motor is proportional to the magnetic field intensity of the stator windings. It may be increased only by adding more windings or by increasing the current.

A natural limit against any current increase is the danger of saturating the iron core. Though this is of minimal importance. Much more important is the maximum temperature rise of the motor, due to the power loss in the stator windings. This shows one advantage of the bipolar circuit, which, compared to unipolar systems, has only half of the copper resistance because of the double cross section of the wire. The winding current may be increased by the factor $\sqrt{2}$ and this produces a direct proportional affect on the torque. At their power loss limit bipolar motors thus deliver about 40 % more torque (fig. 3) than unipolar motors built on the same frame.

If a higher torque is not required, one may either reduce the motor size or the power loss.

Figure 3 : Bipolar Motors Driver Deliver More Torque than Unipolars.



CONSTANT CURRENT DRIVING

In order to keep the motor's power loss within a reasonable limit, the current in the windings must be controlled.

A simple and popular solution is to give only as much voltage as needed, utilizing the resistance (R_L) of the winding to limit the current (fig. 4a). A more complicated but also more efficient and precise solution is the inclusion of a current generator (fig. 4b), to achieve independence from the winding resistance. The supply voltage in Fig. 4b has to be higher than the one in Fig. 4a. A comparison between both circuits in the dynamic load/working order shows visible differences.

Figure 4 : Resistance Current Limiter (a) and Current Generator Limiting.

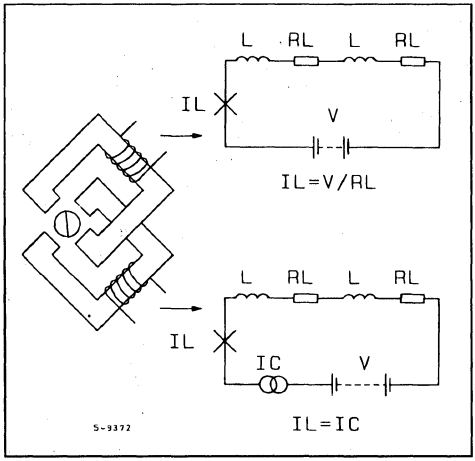
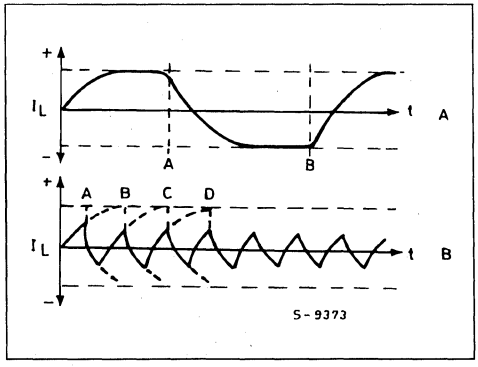


Figure 5 : At High Step Frequencies the Winding Current cannot Reach its Setting Value because of the Continuous Direction Change.



It has already been mentioned that this power of the motor is, among others, proportional to the winding current.

In the dynamic working order a stepper motor changes poles of the winding current in the same stator winding after two steps. The speed with which the current changes its direction in the form of an exponential function depends on the specified inductance, the coil resistance and on the voltage. Fig. 5a shows that at a low step rate the winding current I_L reaches its nominal value V_L/R_L before the direction is changed. However, if the poles of the stator windings are changed more often, which corresponds to a high step frequency, the current no longer reaches its saturating value because of the limited change time ; the power and also the torque diminish clearly at increasing number of revolutions (fig. 5).

MORE TORQUE AT A HIGHER NUMBER OF REVOLUTIONS

Higher torque at faster speeds are possible if a current generator as shown in Fig. 4b is used. In this application the supply voltage is chosen as high possible to increase the current's rate of change. The current generator itself limits only the phase current and becomes active only the moment in which the coil current has reached its set nominal value. Up to this value the current generator is in saturation and the supply voltage is applied directly to the winding.

Fig. 6, shows that the rate of the current increase is now much higher than in Figure 5. Consequently at higher step rates the desired current can be maintained in the winding for a longer time. The torque decrease starts only at much higher speeds.

Fig. 7 shows the relation between torque and speed in the normal graphic scheme, typical for the stepper motor. It is obvious that the power increases in the upper torque range where it is normally needed, as the load to be driven draws most energy from the motor in this range.

EFFICIENCY - THE DECISIVE FACTOR

The current generator combined with the high supply voltage guarantees that the rate of change of the current in the coil is sufficiently high.

At the static condition or at low numbers of revolutions, however, this means that the power loss in the current generator dramatically increases, although the motor does not deliver any more energy in this range ; the efficiency factor is extremely bad.

Help comes from a switched current regulation using the switch-transformer principle, as shown in fig. 8. The phase winding is switched to the supply voltage until the current, detected across R_S, reaches the desired nominal value. At that moment the switch, formerly connected to + V_S, changes position and shorts out the winding. In this way the current is stored, but it decays slowly because of inner winding losses. The discharge time of the current is determined during this phase by a monostable or pulse oscillator. After this time one of the pole changing switches changes back to + V_S, starting an induction recharge and the clock-regulation-cycle starts again.

Figure 6 : With a Step Current Slew, it is not a Problem to Obtain, even at High Step frequencies Sufficient Current in Windings.

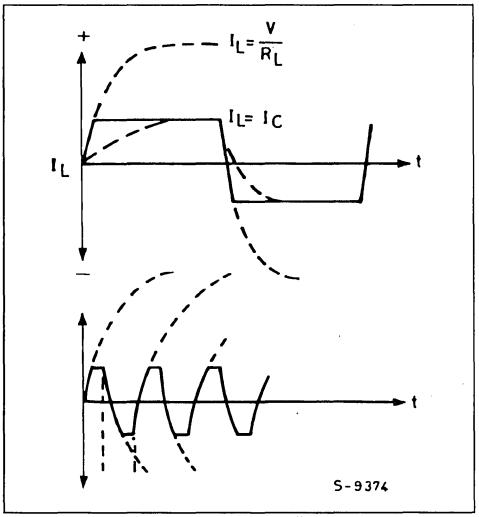
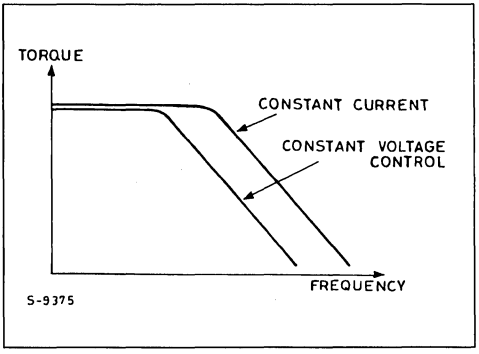


Figure 7 : Constant Current Control of the Stepper Motor Means more Torque at High Frequency.



Since the only losses in this technique are the saturation loss of the switch and that of the coil resistance, the total efficiency is very high.

The average current that flows from the power supply line is less than the winding current due to the concept of circuit inversion. In this way also the power unit is discharged. This king of phase current control that has to be done separately for each motor phase leads to the best ratio between the supplied electrical and delivered mechanical energy.

POSSIBLE IMPROVEMENTS OF THE UNIPOLAR CIRCUIT

It would make no sense to apply the same principle to a stabilized current controlled unipolar circuit, as two more switches per phase would be necessary for the shortening out of the windings during the free phase and thus the number of components would be the same as for the bipolar circuit ; and moreover, there would be the well known torque disadvantage.

From the economic point of view a reasonable and justifiable improvement is the "Bi-Level-Drive" (fig. 9). This circuit concept works with two supply voltages ; with every new step of the motor both windings are connected for a short time to a high supply voltage. This considerably increases the current rate of change and its behaviour corresponds more or less to the stabilized power principle. After a predetermined the switch opens, a no a lower supply voltage is connected to the winding thru a diode.

This kind of circuit by no means reaches the performance of the clocked stabilized power control as per fig. 8, as the factors : distribution voltage oscillation, B.e.m.f., thermal winding resistance, as well as the separate coil current regulation are not considered, but it is this circuit that makes the simple unipolar R/L-control suitable for many fields of application.

Figure 8 : With Switch Mode Current Regulation Efficiency is Increased.

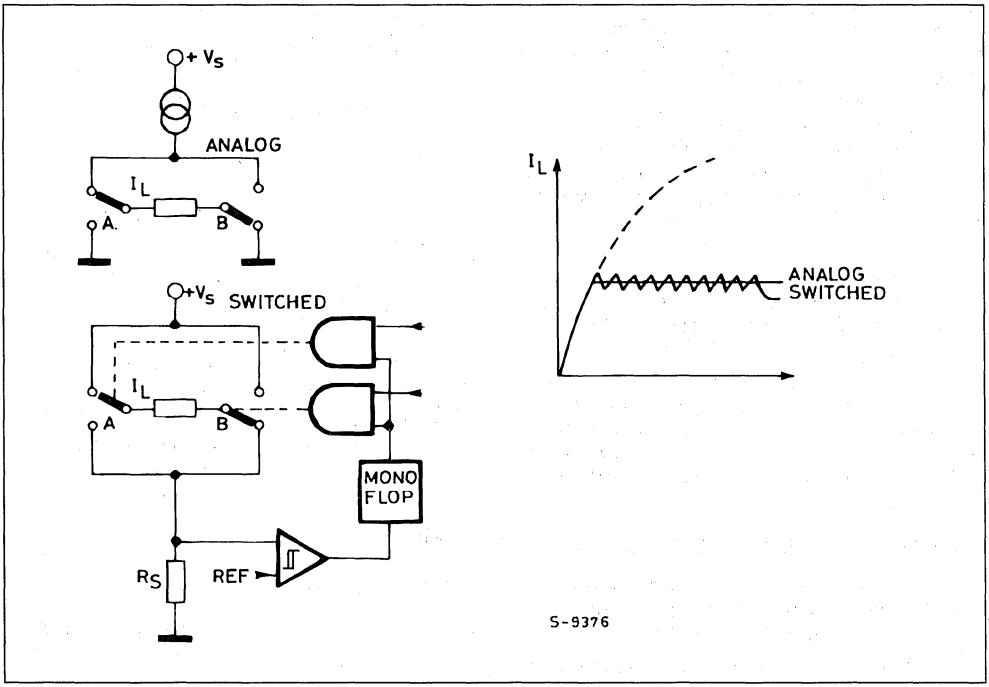
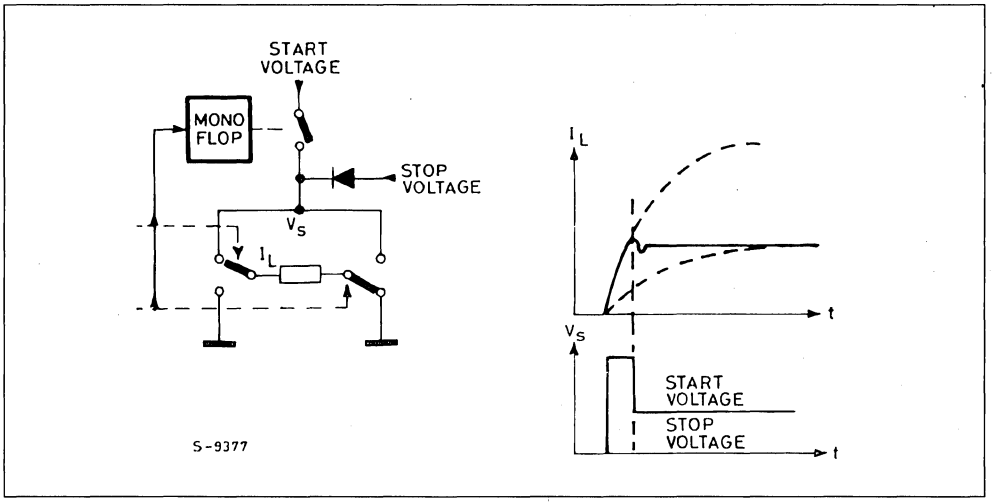


Figure 9 : At Every New Step of the Motor, it is Possible to Increase the Current Rate with a Bilevel Circuit.



ADVANTAGES AND DISADVANTAGES OF THE HALF-STEP

An essential advantage of a stepper motor operating at half-step conditions is its position resolution increased by the factor 2. From a 3.6 degree motor you achieve 1.8 degrees, which means 200 steps per revolution.

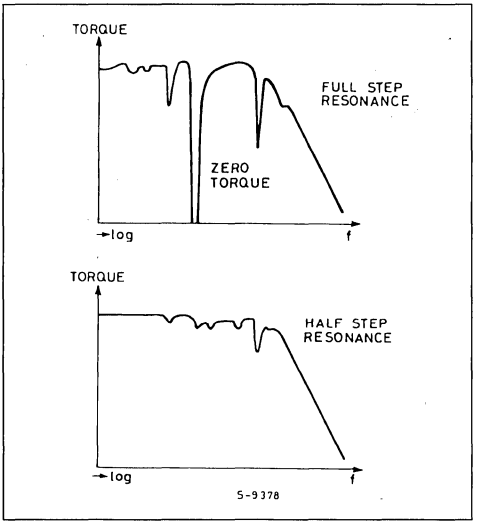
This is not always the only reason. Often you are forced to operate at half-step conditions in order to avoid that operations are disturbed by the motor resonance. These may be so strong that the motor has no more torque in certain step frequency ranges and looses completely its position (fig. 10). This is due to the fact that the rotor of the motor, and the changing magnetic field of the stator forms a spring-mass-system that may be stimulated to vibrate. In practice, the load might deaden this system, but only if there is sufficient frictional force.

In most cases half-step operation helps, as the course covered by the rotor is only half as long and the system is less stimulated.

The fact that the half-step operation is not the dominating or general solution, depends on certain disadvantages :

- the half-step system needs twice as many clock-pulses as the full-step system ; the clock-frequency is twice as high as with the full-step.
- in the half-step position the motor has only about half of the torque of the full-step.

Figure 10 : The Motor has no More Torque in Certain Step Frequency Ranges with Full Step Driving.



For this reason many systems use the half-step operation only if the clock-frequency of the motor is within the resonance risk area.

The dynamic loss is higher the nearer the load moment comes to the limit torque of the motor. This effect decreases at higher numbers of revolutions.

TORQUE LOSS COMPENSATION IN THE HALF-STEP OPERATION

It's clear that, especially in limit situations, the torque loss in half-step is a disadvantage. If one has to choose the next larger motor or one with a double resolution operating in full-step because of some insufficient torque percentages, it will greatly influence the costs of the whole system.

In this case, there is an alternative solution that does not increase the coats for the bipolar chopping stabilized current drive circuit.

The torque loss in the half-step position may be compensated for by increasing the winding current by the factor $\sqrt{2}$ in the phase winding that remains active. This is also permissible if, according to the motor data sheet, the current limit has been reached, because this limit refers always to the contemporary supply with current in both windings in the full-step position. The factor $\sqrt{2}$ increase in current doubles the stray power of the active phase. The toal dissipated power is like that of the full-step because the non-active phase does not dissipate power.

The resulting torque in the half-step position amounts to about 90 % of that of the full-step, that means dynamically more than 95 % torque compared to the pure full-step ; a neglectable factor.

The only thing to avoid is stopping the motor at limit current conditions in a half-step position because it would be like a winding thermal phase overload concentrated in one.

The best switch-technique for the half-step phase current increase will be explained in detail later on Fig. 11 shows the phase current of a stepping motor in half-step control with an without phase current increase and the pertinent curves of stap frequency and torque.

Figure 11 : Half Step Driving with Shaping Allows to Increase the Motor's Torque to about 95 % of that of the Full Step.

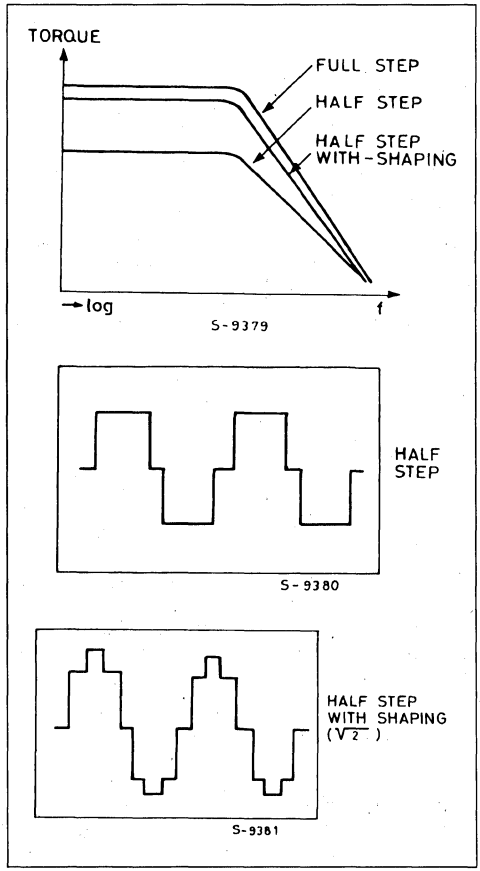
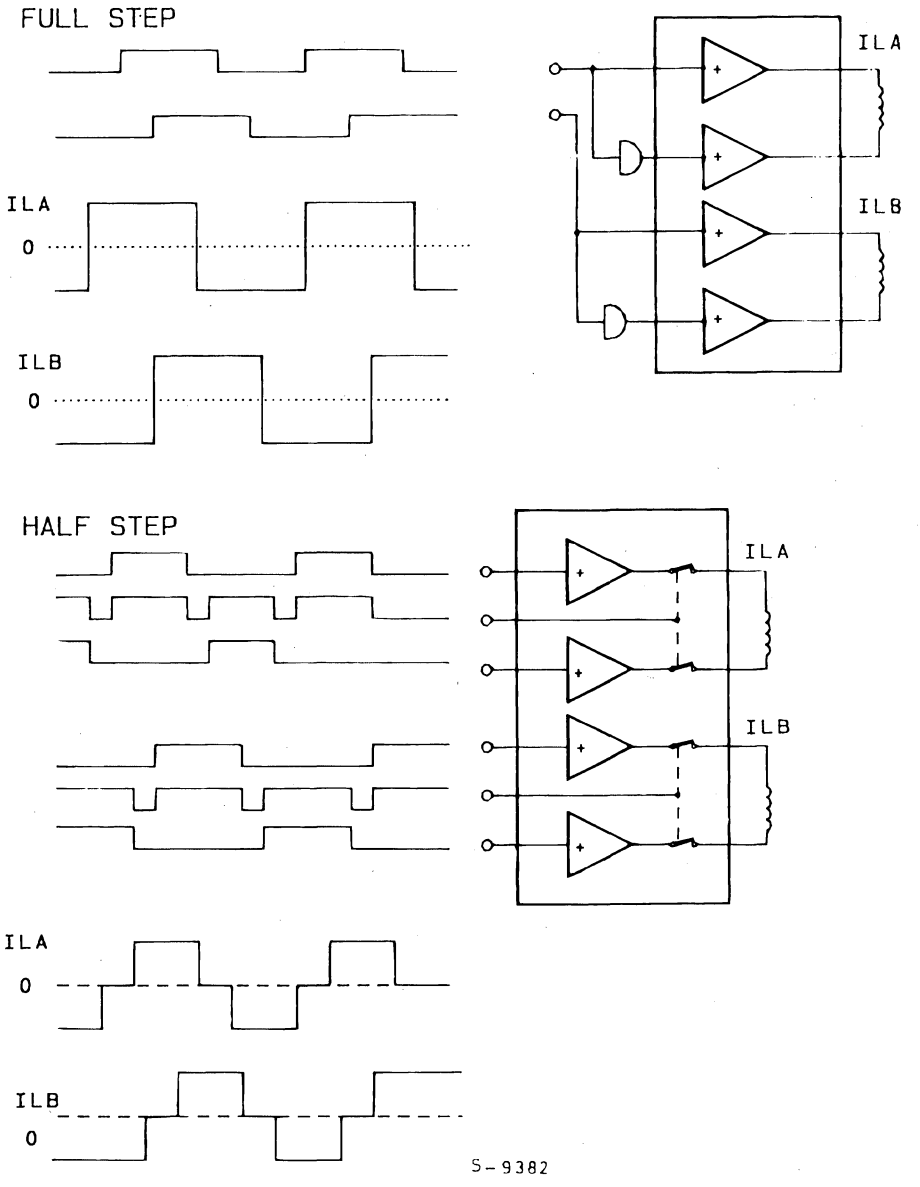


Figure 12 : Only Two Signals for Full Step Driving are Necessary while Four (six if three-state is needed on the output stages) for half Step.



DRIVE SIGNALS FOR THE MICRO ELECTRONIC

A direct current motor runs by itself if you supply if with voltage, whereas the stepping motor needs the commutation signal in for of several separated but linkable commands. In 95 % of the applications today, the origin of these digital commands is a microprocessor system.

In its simplest form, a full-step control needs only two rectangular signals in quadrature. According to which phase is leading, the motor axis rotates clockwise or counter-clockwise, whereby the rotation speed is proportional to the clock frequency.

In the half-step system the situation becomes more complicated. The minimal two control signals become four control signals. In some conditions as many as six signals are needed. If the Tri-state-command for the phase ranges without current, necessary for high motor speeds, may not be obtained from the 4 control signals. Fig. 12 shows the relationship between the phase current diagram and the control signal for full and half-step.

Since all signals in each mode are in defined relations with each other, it is possible to generate them using standard logic. However, if the possibility to choose full and half-step is desired, a good logic implementation becomes quite expensive and an application specific integrated circuit would be better. Such an application specific integrated circuit could reduce the number of outputs required from a microprocessor from the 6 required to 3 static and dynamic control line.

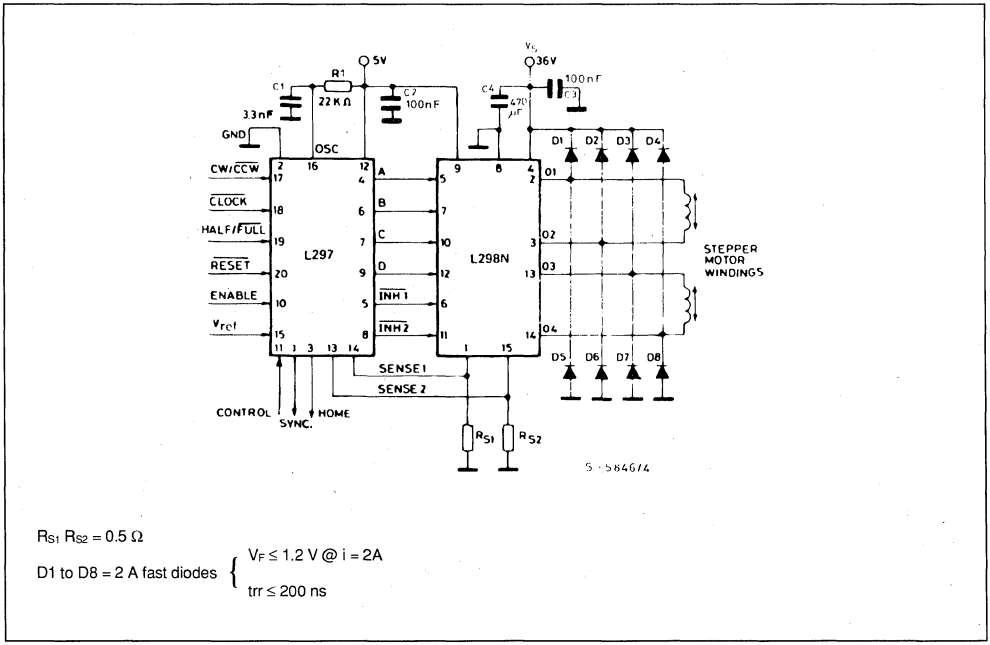
A typical control circuit that meets all these requirements is the L297 unit (fig. 13).

Four signals control the motor in all operations :

1. CLOCK : The clock signal, giving the stepping command
2. RESET : Puts the final level signals in a defined start position
3. DIRECTION : Determines the sense of rotation of the motor axis.
4. HALF/FULL : Desides whether to operate in full or in half-step.

Another inhibit input allows the device to switch the motor output into the Tri-state-mode in order to prevent undesired movements during undefined operating conditions, such as those that could occur during.

Figure 13 : The L297 avoids the Use of Complicated Standard Logic to Generate Both Full and Half-step Driving Signals Together with Chopper Current Control.



R_{S1} R_{S2} = 0.5 Ω

D1 to D8 = 2 A fast diodes { $V_F \leq 1.2$ V @ i = 2A ; trr ≤ 200 ns

SWITCH-MODE CURRENT REGULATION

The primary function of the current regulation circuit is to supply enough current to the phase windings of the motor, even at high step rates.

The functional blocks required for a switchmode current control are the same blocks required in switching power supplies ; flip-flops, comparators ; and an oscillator are required. These blocks can easily be included in the same IC that generates the phase control signals. Let us consider the implementation of chopper current control in the L297.

The oscillator on pin 16 of the L297 resets the two flip-flops at the start of each oscillator period. The flip-flop outputs are then combined with the outputs of the translator circuit to form the 6 control signals supplied to the power bridge (L298).

When activated, by the oscillator, the current in the winding will raise, following the L/R time constant curve, until the voltage across the sense resistor (pin 1, 15 of L298) is equal to the reference voltage input (pin 15, L297) the comparator then sets the flip-flop, causing the output of the L297 to change to an equiphase condition, thus effectively putting a short circuit across the phase winding. The bridge is activated into a diagonally conductive state when the oscillator resets the flip-flop at the start of the next cycle.

Using a common oscillator to control both current regulators maintains the same chopping frequency for both, thus avoiding interference between the two.

The functional block diagram of the L297 and the power stage (L298) are shown in Figure 14 alone with the operating wave forms.

An important characteristics of this circuit implementation is that, during the reset time, the flip-flops are kept reset. The reset time can be selected by selecting the impedance of the R/C network or pin 16. In this way, the current spike and noise across the sense resistors that may occur during switching will not cause a premature setting of the flip-flop. Thus the recovery current spike of the protection diodes can be ignored and a filter in the sense line is avoided.

THE RIGHT PHASE CURRENT FOR EVERY OPERATING CONDITION

The Chopper principle of the controller unit reveals that the phase current in the motor windings is controlled by two data : the reference voltage at pin 15 of the controller and the value of the sense resistance at pins 1 and 15 of the L298, that is $I_L = V_{REF}/R_S$. By changing V_{REF} it is very easy to vary the current within large limits. The only question is for which purpose and at which conditions.

More phase current means more motor torque, but also higher energy consumption.

An analysis of the torque consumption for different periods and load position changes shows that there is no need for different energies.

There is a high energy need during the acceleration or break phases, whereas during continuous operation or neutral or stop position less energy has to be supplied. A motor with its phase current continuously oriented at the load moment limit, even with the load moment lacking, consumes needlessly energy, that is completely transformed into heat.

Therefore it is useful to resolve the phase current in at least two levels controllable from the processor. Fig. 18 shows a minimal configuration with two resistance and one small signal transistor as changeover switch for the reference input. With another resistance and transistor it is possible to resolve 2 Bits and consequently 4 levels. That is sufficient for all imaginable causes.

Fig. 16 shows a optimal phase current diagram during a positioning operation.

Figure 14 : Two ICs and very Few External Components Provide Complete Microprocessor to Bipolar Stepper Motor Interface.

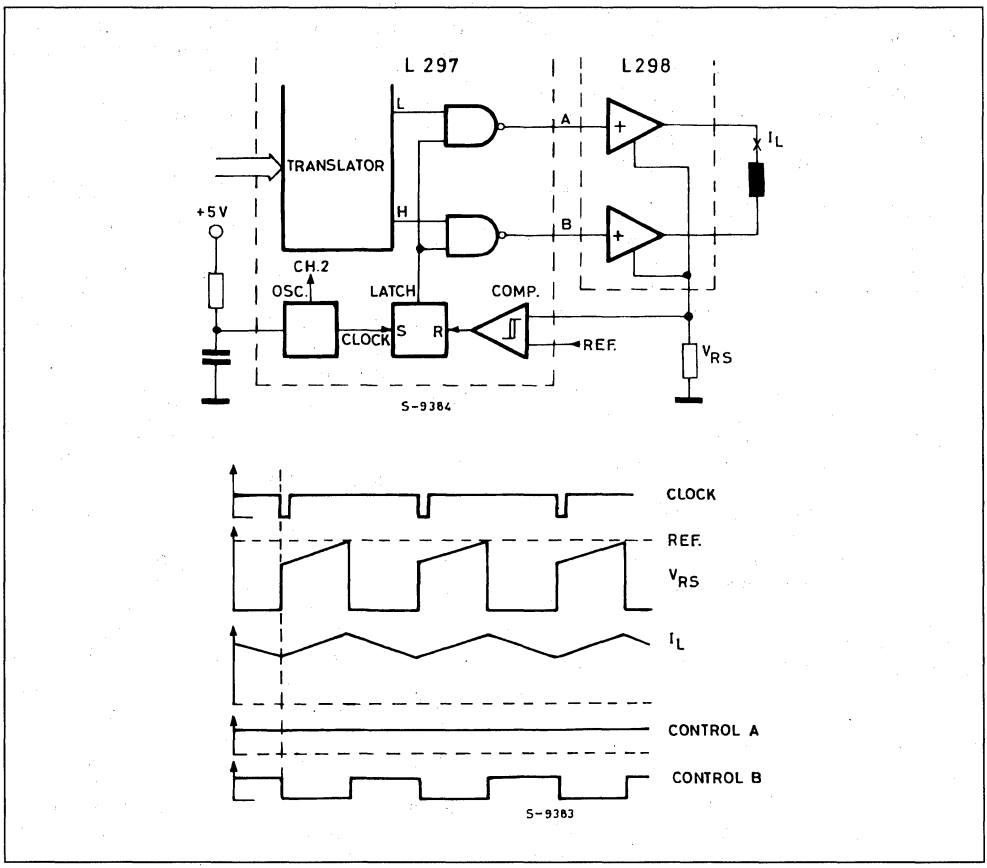


Figure 15 : Because of the Set-dominant Latch Inside the L297 it is Possible to Hide Current Spikes and Noise Across the Sense Resistors thus Avoiding External Filters.

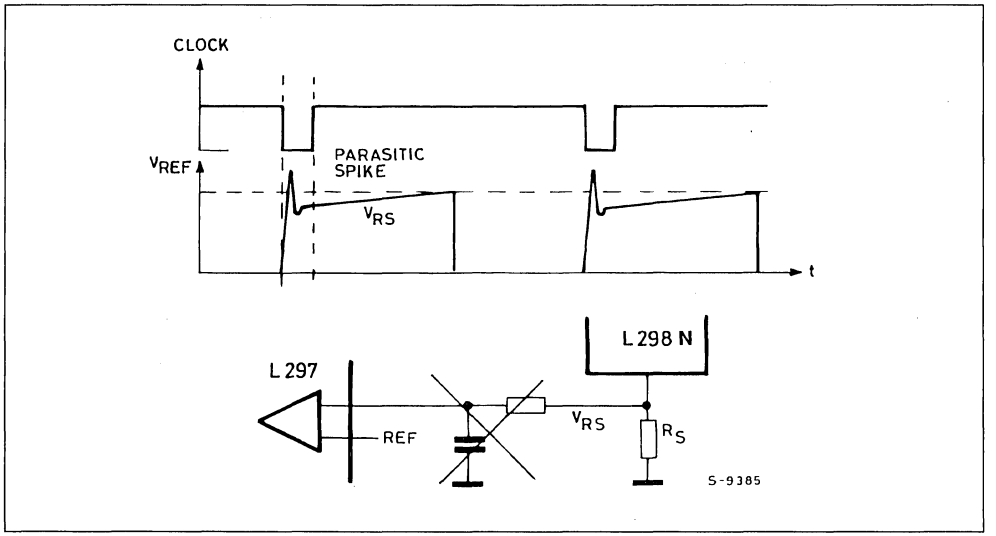
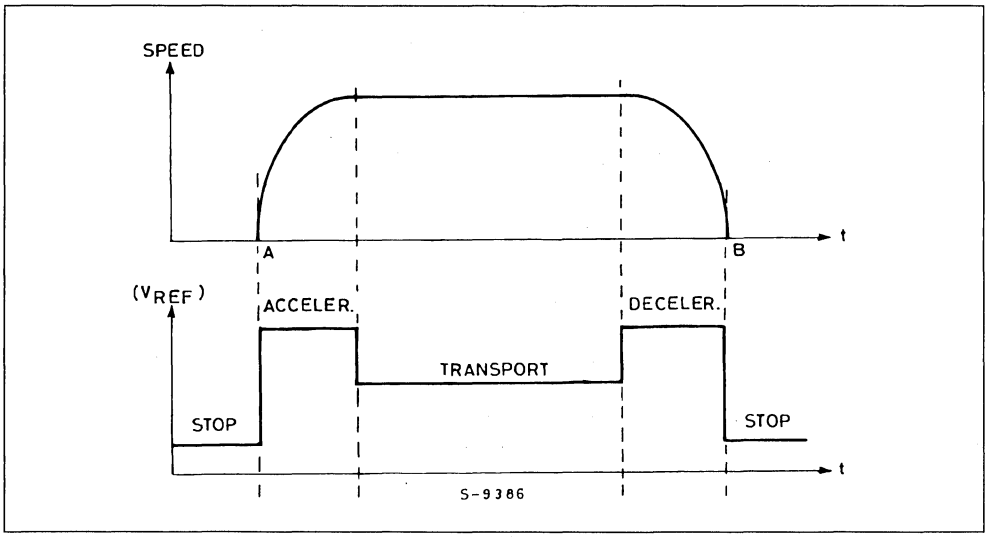


Figure 16 : More Energy is needed During The Acceleration and break Phases Compared the Continuous Operation, Neutral or Stop Position.



HIGH MOTOR CLOCK RESETS IN THE HALF-STEP SYSTEM

In the half-step position one of the motor phases has to be without current. If the motor moves from a full-step position into a half-step position, this means that one motor winding has to be completely discharged. From the logic diagram this means for the high level bridge an equivalent status of the input signals A/B, for example in the HIGH-status. For the coil this means short circuit (fig. 17 up) and consequently a low reduction of the current. In case of high half-step speeds the short circuit discharge time constant of the phase winding is not sufficient to discharge the current during the short half-step phases. The current diagram is not neat, the half step is not carried out correctly (fig. 17 center).

For this reason the L297 controller-unit generates an inhibit-command for each phase bridge, that switches the specific bridge output in the half-step position into Tri-state. In this way the coil can start swinging freely over the external recovery diodes and discharge quickly. The current decrease rate of change corresponds more or less to the increase rate of change (fig. 17 below).

In case of full-step operation both inhibit-outputs of the controller (pin 5 and 8) remain in the HIGH-status.

Figure 17 : The Inhibit Signal Turns Off Immediately the Output Stages Allowing thus a Faster Current Decay (mandatory with half-step operation).

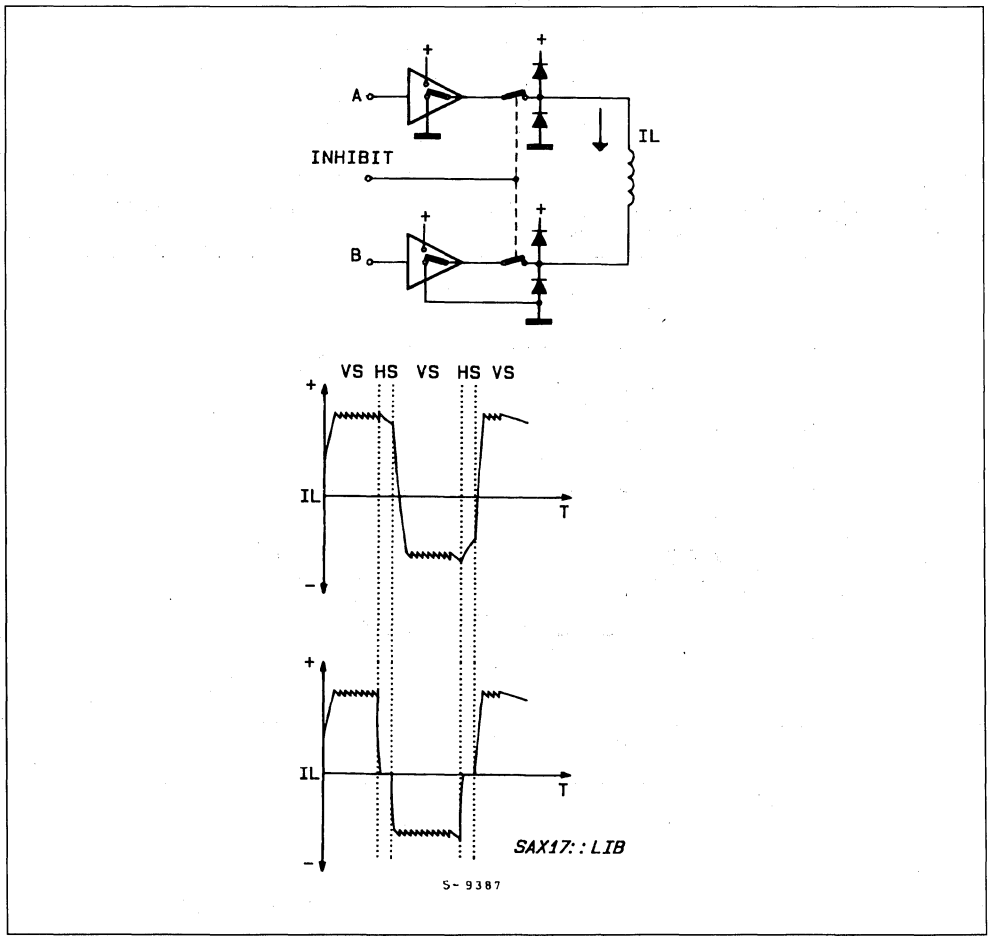
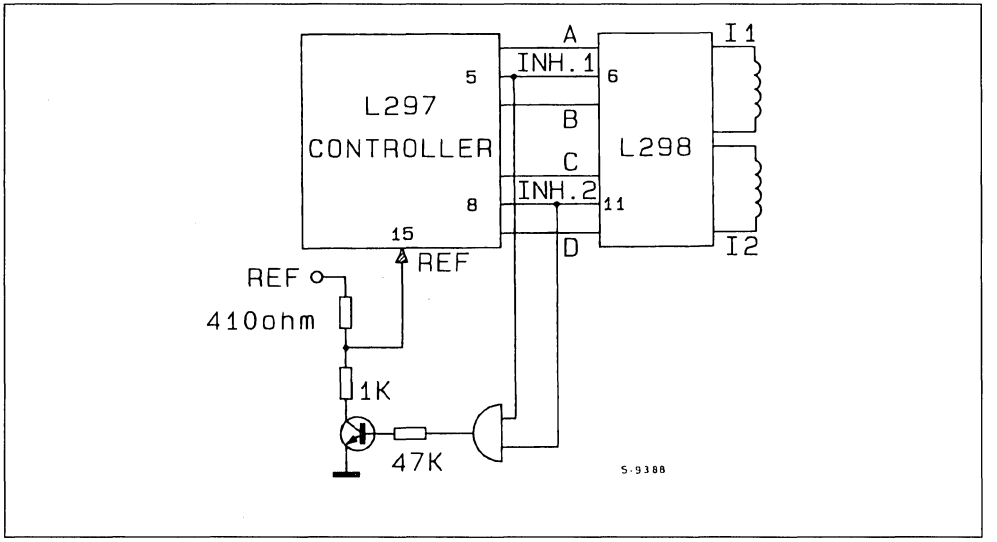


Figure 18 : With This Configuration it is Possible to Obtain Half-step with Shaping Operation and Therefore More Torque.



MORE TORQUE IN THE HALF-STEP POSITION

A topic that has already been discussed in detail. So we will limit our considerations on how it is carried out, in fact quite simply because of the reference voltage controlled phase current regulation.

With the help of the inhibit-signals at outputs 5 and 8 of the controller, which are alternatively active only when the half-step control is programmed, the reference voltage is increased by the factor 1.41 with a very simple additional wiring (fig. 18), as soon as one of the two inhibit-signals switches LOW. This increases the current in the active motorphase proportionally to the reference voltage and compensates the torque loss in this position. Fig. 19 shows clearly that the diagram of the phase current is almost sinusoidal, in principle the ideal form of the current graph.

To sum up we may say that this half-step version offers most advantages. The motor works with poor resonance and a double position resolution at a torque, that is almost the same as that of the full-step.

BETTER GLIDING THAN STEPPING

If a stepper motor is supposed to work almost gliding and not step by step, the form of the phase current diagram has to be sinusoidal.

The advantages are very important :

- no more phenomena of resonance
- drastic noise reduction
- connected gearings and loads are treated with care
- the position resolution may be increased further.

However, the use of the L297 controller-unit described until now is no longer possible of the more semplicated form of the phase current diagram the Controller may become simpler in its functions.

Fig. 20 shows us an example with the L6505 unit. This IC contains nothing more than the clocked phase current regulation which works according to the same principle as L297. The four control signals emitting continuously a full-step program are now generated directly by the microprocessor. In order to obtain a sinusoidal phase current course the reference voltage inputs of the Controller are modulated with sinusoidal half-waves.

The microprocessor that controls the direction of the current phase with the control signals also generates the two analog signals.

For many applications a microprocessor with dedicated digital to analog converters can be chosen. Eliminating the need for separate D/A circuits.

About 5 bit have proved to be the most suitable suddivision of the current within one full-step. A higher

resolution brings no measurable advantages. On the contrary, the converter clock frequency is already very high in case of low motor revolutions and very difficult to process by the processor-software. It is recommended to reduce the D/A resolution at high step frequencies.

In case of higher motor revolutions it is more convenient to operate only in full-step, since harmonic control is no longer an advantage as the current has only a triangular waveform in the motor winding.

PRECISION OF THE MICRO STEP

Any desired increase of the position resolution between the full step position has its physical limits. Those who think it is possible to resolve a 7.2° - stepper motor to 1.8° with the same precision as a 1.8° - motor in full-step will be received, as there are several limits :

The rise rate of the torque diagram corresponding to the twisting angle of the rotor for the 7.2° - motor is flatter by a factor of 4 then for the original 1.8° - motor. Consequently with friction or load moment, the position error is larger (fig. 21).

For most of the commercial motors there isn't a sufficiently precise, linear relationship between a sinusoidal-current-diagram and an exact micro step angle. The reason is a dishomogeneous magnetic field between the rotor and the two stator fields.

Above all, problems have to be expected with motors with high pole feeling. However, there are special stepper motors in which an optimized micro step operation has already been considered during the construction phase.

Figure 19 : The Half-step with Shaping Positioning is Achieved by Simply Changing Reference Voltages.

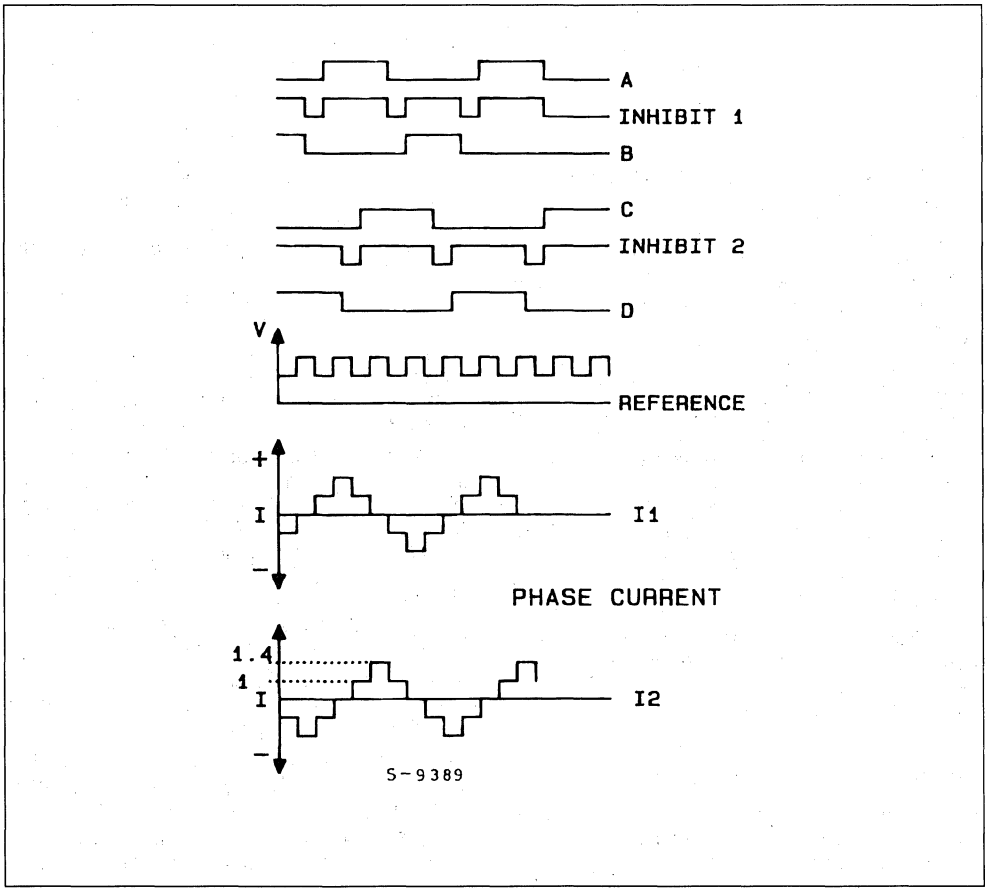
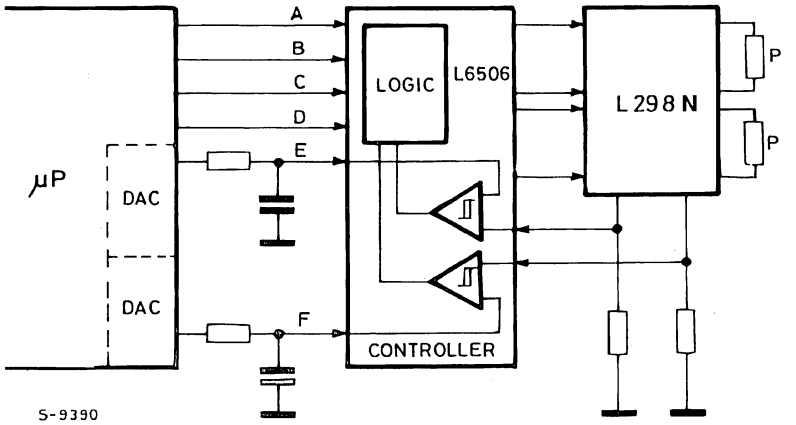


Figure 20 : L6506 Unit Gives The Possibility to Modulate Separately the Two Reference Voltage Inputs in Order to obtain a Sinusoidal Phase Current.



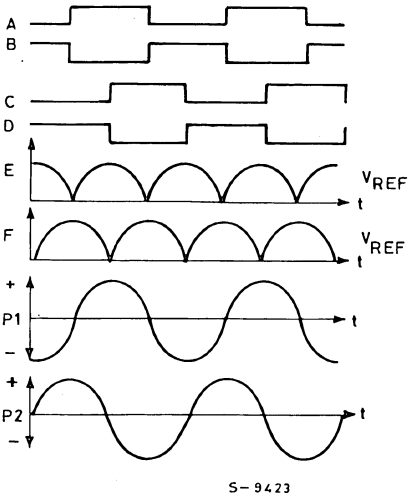
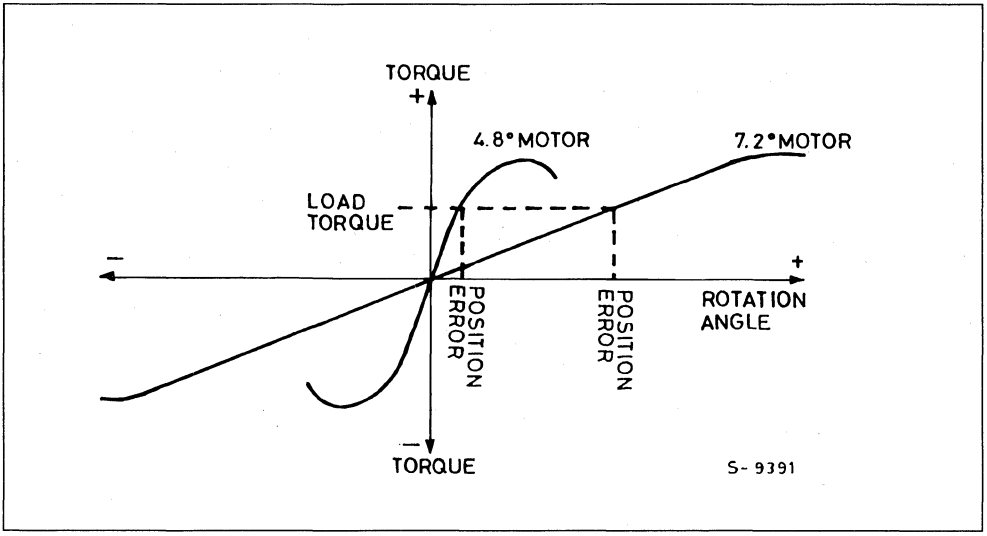


Figure 21 : Better Resolution is achieved with Low Degree Motor but More torque is delivered with high Degree Motor.



CONCLUSIONS

The above described application examples of modern integrated circuits show that output and efficiency of stepper motors may be remarkably increased without any excessive expense increase like before.

Working in limit areas, where improved electronics with optimized drive sequences allow the use of less expensive motors, it is even possible to obtain a cost reduction.

CONSTANT-CURRENT CHOPPER DRIVE UPS STEPPER-MOTOR PERFORMANCE

The most efficient and performant way to drive a stepper motor is to use a "chopper" drive circuit. This note explains some basic theory then presents practical circuits based on power ICs.

PULSE WIDTH-MODULATED DRIVE IMPROVES MOTOR TORQUE AND SPEED YET ADDS NO COMPLEXITY TO CIRCUIT

Designers opting to use a fractional-horsepower stepper motor in applications such as computer printers can improve the motor's efficiency and its torque and speed characteristics by using a constant-current pulse-width-modulated (PWM) chopper-drive circuit. What's more, for high-power drives, dedicated control chips and a constant-current chopper drive can be as simple to use as direct drive.

A basic problem for a directly driven stepper is that the motor winding's time constant (L/R) causes the current to increase slowly in the winding during each pulsed input. It may, therefore, never reach full-rated value, especially at high speed, or high pulsing rates, unless the voltage (V_S) across the terminals is high. In the simplest stepper drive (see fig. 1a), transistor or Darlington switches sequentially activate the windings to drive the motor (see box, "Stepper motor basics").

This type of drive performs poorly because the supply voltage must be low so that the steady-state current is not excessive. As a result, the average winding current – and hence the torque – is very low at high drive motor speed.

Often, this problem is overcome by introducing a series resistance, thereby increasing the overall value by a factor of four - giving an L/4R ratio - and also by increasing the supply voltage (see fig. 1b). This arrangement reduces the motor's time constant, which improves torque at high step rates. However such an approach is inefficient, because the series resistor constitutes a substantial waste of power.

Figure 1 : Common unipolar stepping drives (a) produce insufficient torque output becuase their supply voltage must be kept low to limit current. Adding series resistance to an L/4R ratio (b) and raising the supply voltage proportionately improves torque output, especially at high step rates.

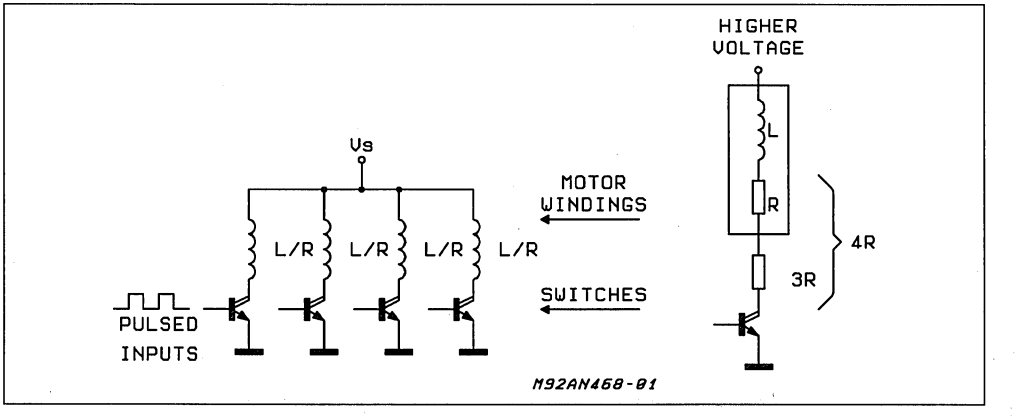
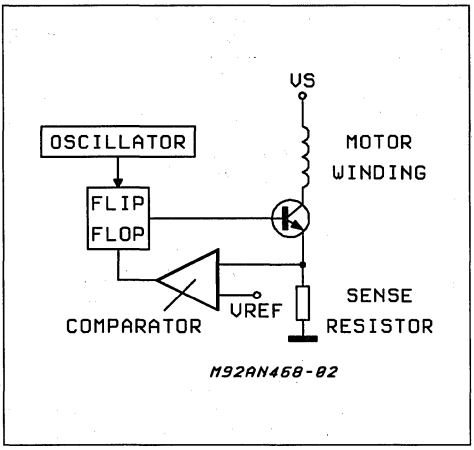


Figure 2 : A Pulse-width-modulated, or chopper, drive overcomes most of the problems of the simpler direct drive or even linear constant-current drives.



CONSTANT CURRENT IS BEST

Introducing a feedback loop to control the winding current is a better solution. Linear constant-current control is possible but is rarely used because of high power losses in the power stage. However, a pulse-width-modulation scheme – a chopper circuit – not only solves the L/R time-constant problem but cuts power dissipation too (see fig. 2).

A four-phase bifilar/hybrid unipolar stepper motor could use a quad Darlington like the ULN2075B as a chopper driver and a chip like the L6506 as a current controller (see fig. 3).

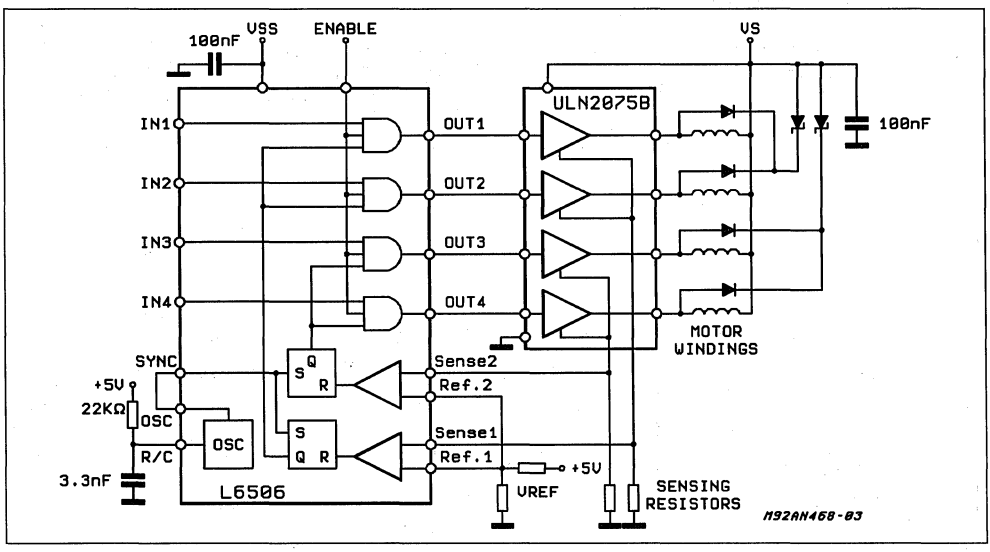
The L6506, which contains all the chopper circuitry, is simple to use. An external RC network sets the oscillator frequency, and a voltage divider (or trimmer) sets the reference voltages, and hence the phase currents. Normally an oscillator frequency of over 20 KHz is chosen to avoid motor noise. The maximum usable frequency depends on the L/R time constant of the motor.

Control signals for the four-phase inputs can be provided by a micro-computer chip or a simple repetitive sequence from a logic circuit. Note that the L6506 contains just two independent chopper-control loops - sufficient for a four-phase unipolar stepping motor because opposing windings never energize together.

DRIVING BIPOLAR MOTORS

Bipolar stepper motors, preferred for their better torque/weight ratio, however, are normally driven by H-bridge output stages. They enable a single-polarity supply to drive each motor winding end sequentially to achieve a polarity-reversal effect on the windings.

Figure 3 : A simple chopper drive for a unipolar stepping motor, can be assembled with just two chips : a Quad Darlington output driver IC and constant-current feedback controller IC.



STEPPER-MOTOR BASICS

In computer-peripheral office-equipment applications, the most popular stepper motors are permanent-magnet types with two-phase bipolar windings or bifilar-wound unipolar windings. Stripped to the essentials, both types consist of a permanent-magnet rotor surrounded by stator poles carrying the windings.

A two-pole motor would have a step angle of 90 °. However, most motors have multiple poles to reduce the step angle to a few degrees.

A bipolar permanent-magnet stepper motor has a single winding for each phase – and the current must be reversed to reverse the stator field. Bifilar/hybrid unipolar motors, however, have two windings wound in opposite directions for each phase, so that the field can be reversed with a single-polarity drive. Unipolar motors were once popular because the drive was simpler. But with today's dual bridge (H-bridge) ICs, it is just as easy to drive a bipolar motor.

In the most popular drive technique - two-phase-on - both phases are always energized. In another method – called the wave drive – one phase is energized at a time.

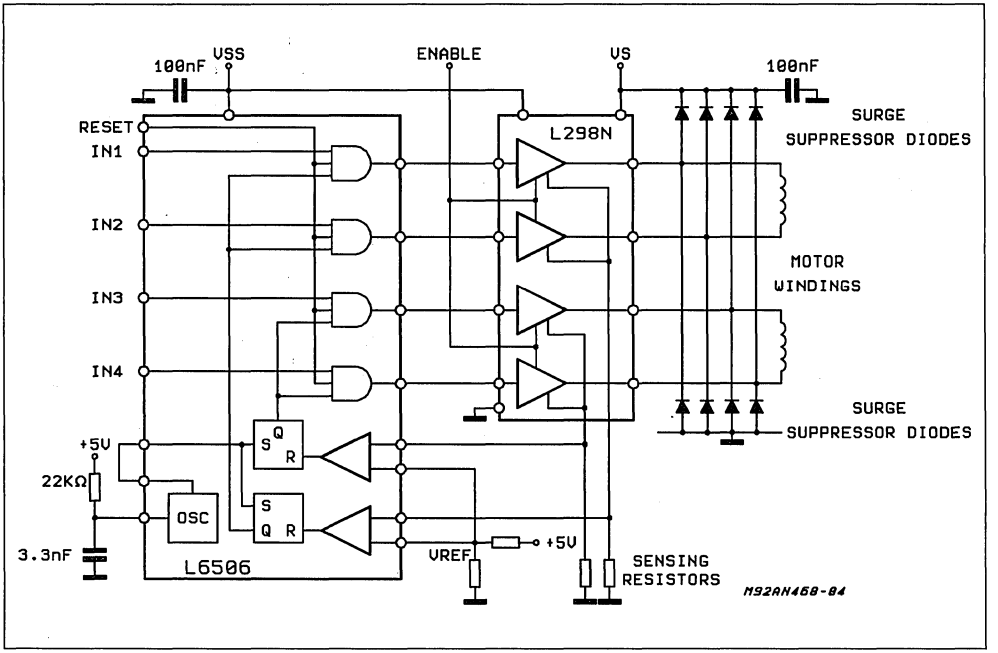
A third technique combines the two sequences and drives the motor one half-step at a time. Half-stepping is very useful because motor mechanically designed for very small step angles are much more complex – and costly – to built. It is more economical to use a 100-step motor in half steps rather than a 200-step motor in full step.

Recently designers have started microstepping, or driving the motor at one-quarter stepping rather or less. This type of operation can obtain fine step control without using mechanically complex motors with small step angles.

A two-phase bipolar motor needing up to 2A/phase can be driven by a single IC - the L298N dual bridge (see fig. 4). It contains two H-bridges with all the necessary level shifters and gates to directly interface low-level input logic signals.

As before, a complete chopper drive can be built by adding a current-controller chip and the necessary protective diodes, an RC network to define the oscillator frequency and a reference-voltage divider to set the current level. Four-phase signals to the controller are provided by a controlling microcomputer or by another dedicated controller chip - the L297 stepper-motor controller.

Figure 4 : A Dual-bridge IC provides a simple power-stage design solution for a bipolar stepper motor.



Containing an internal translator circuit controlled by step-and-direction inputs, the L297 motor controller (see fig. 5) allows operation in three modes : two-phase-on, half-step and wave-drive.

The normal two-phase-on mode is selected by a low level on the half/full input when the device has been reset to start.

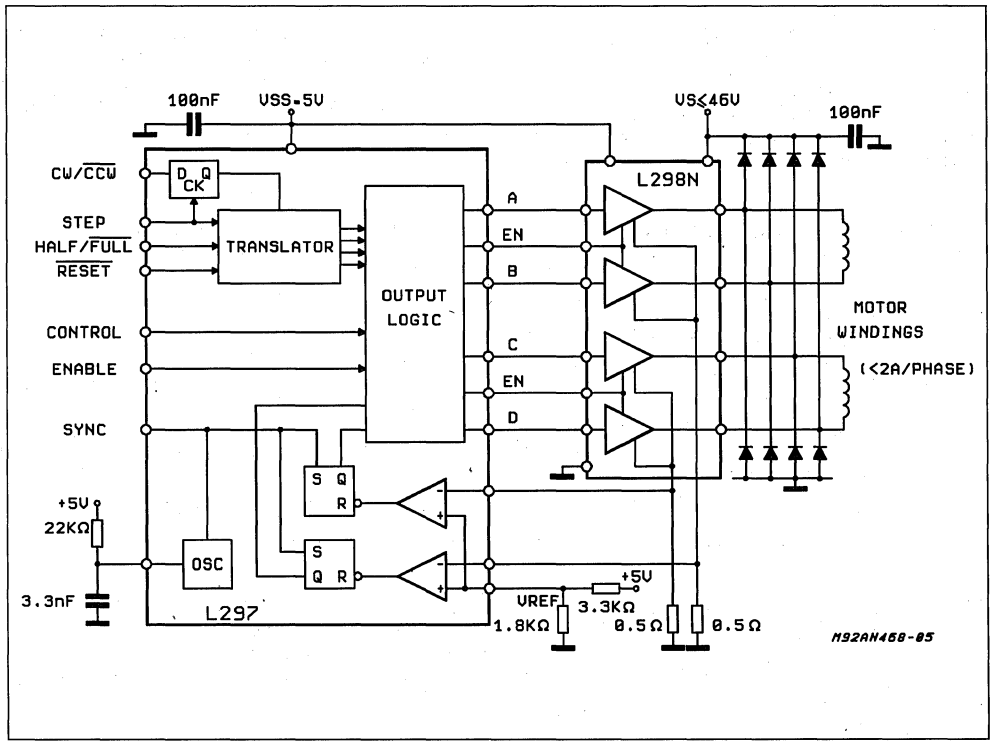
Half-step drive is selected by a high level on the half/full step input. To initialize the wave-drive mode, the user disables the output stage (brings enable low), resets the device, steps the translator one step, brings half/full low, and then reenables the outputs.

The L297 also lets the designer select either phase or inhibit chopping. Phase chopping provides lower ripple and is suitable four unipolar motor, whereas inhibit chopping returns energy to the supply and is better for bipolar motors.

In applications such as printer-paper feed, the motor is often at rest. Since the full torque is not usually necessary to hold the motor in position, designers can save power by switching the current to a lower level between runs. With an L297 or L6506 control chip, this task can be done by simply switching the reference input between two levels.

Where several chopper drives are used in the same system, they should be synchronized prevent intermodulation effects. This is done by connecting the sync pins to one another and omitting the oscillator RC network on all but one device.

Figure 5 : controlled by step, direction, and mode inputs, the L297 stepper-motor controller chip performs some of the functions of a controlling microcomputer.



HANDLING HIGH CURRENT

For current drives greater than 2A/phase, the two bridges in an L298N IC can be paralleled by connecting inputs to the corresponding outputs. However, for a more equal distribution of the load and chip heating, driver 1 should be paralleled with driver 4, and driver 2 with driver 3. Additionally, total current should be derated by 0.5 A to allow for the maximum possible imbalance between the current in each bridge. Thus two L298s can drive motors rated at 3.5 A/phase.

A different configuration for microstepping stepper motors is employed in the PBL3717A control circuit. It contains all of the control and power circuitry for one phase of a motor. An H-bridge output stage can drive motors rated at up to 1A/phase. Two of these devices are needed to drive a two-phase bipolar motor.

The output current level from the PBL3717A is set both by an analog-reference input and two logic inputs (I_1 and I_0), which select one of three preset current levels (the fourth combination disables the outputs stage). This feature implements the microstepping, in which several current levels are used to obtain very small step angles for even more precise control (but at the expense of a less regular torque). Unlike the L297 and L6506, the PBL3717A has a constant off-time chopper driver which is ideal for microstepping.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

USING THE L6506 FOR CURRENT CONTROL OF STEPPING MOTORS

by Thomas Hopkins

Chopper-type current control circuits improve the performance of motor drives. This note shows how this can be done simply using the L6506 current controller IC.

The L6506 is a linear integrated circuit designed to sense and control the current in stepping motors and other similar devices. When used in conjunction with power stages like the L293, L298N, or L7180 the chip set forms a constant current drive for inductive loads and performs all the interface functions from the control logic through the power stage.

The L6506 may be used with either two phase bipolar or four phase unipolar motor configurations. The circuit in figure 1 shows the L6506 used in conjunction with the L298N in a 2 phase bipolar stepper motor application. The circuit in figure 2 implements a similar 4 phase unipolar application.

CURRENT CONTROL LOGIC

In these two circuits, the L6506 is used to sense and control the current in each of the load windings. The current is sensed by monitoring the voltage across a sense resistor (R_{sense}) and using a Pulse Width Modulated control to maintain the current at the desired value.

An on-chip oscillator drives the dual chopper and sets the operating frequency. An RC network on pin 1 sets the operating frequency, which is given by the equation :

$$f \approx \frac{1}{0.69\ R1\ C1} \qquad (1)$$

for R1 > 10 KΩ

The oscillator provides pulses to set the two flip-flops, which in turn cause the outputs to activate the power actuator. Once the outputs have been activated the current in the load starts to increase, limited by the inductive characteristic of the load.

Figure 1 : Application Circuit for Bipolar 2 Phase Stepper Motor.

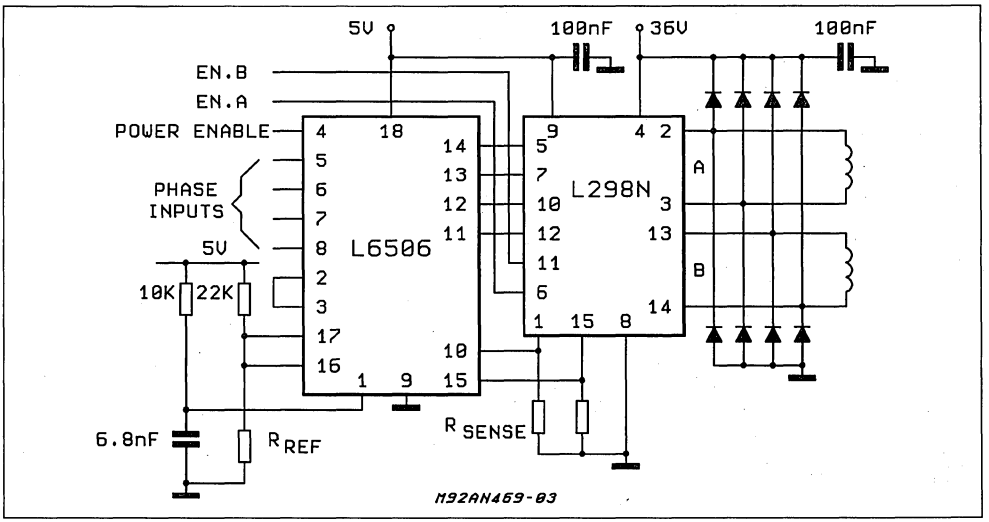
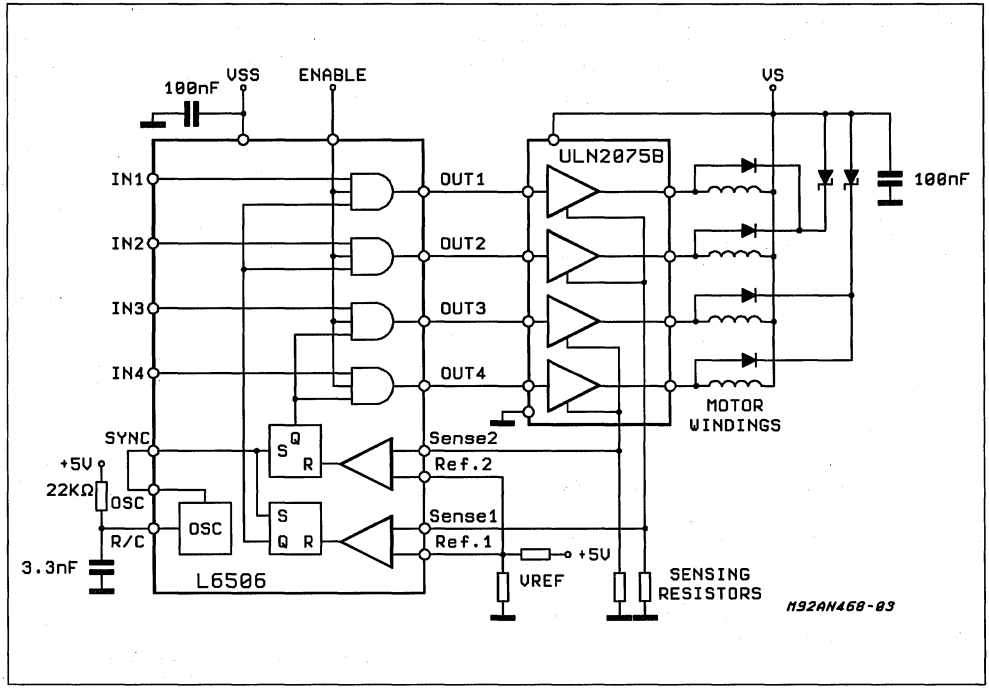


Figure 2 : Application Circuit for Unipolar 4 Phase Stepper Motor.



When the current in the load winding reaches the programmed peak value, the voltage across the sense resistor (R_{sense}) is equal to reference voltage input (V_{ref}) and the corresponding comparator resets its flip-flop. This interrupts the drive and allows the current to decay through a recirculating path until the next oscillator pulse occurs. The peak current in each winding is programmed by selecting the value of the sense resistor and V_{ref} and is given by the equation :

$$I_{peak} = \frac{V_{ref}}{R_{sense}} \qquad (2)$$

The minimum output pulse width is determined by the pulse width of the oscillator, or other signal applied to the sync input. The internal oscillator is designed to provide narrow pulses to the sync input but the pulse width should be considered carefully. In some applications it is desirable to set the pulse width of this sync pulse to be just longer than the turn on delay time of the actuator stage. This may be useful in systems where the switching noise or recovery current of the catch diodes, which passes through the sense resistor, causes the comparator to sense a current above the peak current. By making the sync pulse wide enough to hold the flip-flop set at the time the switching transient occurs will cause the device to ignore this false data.

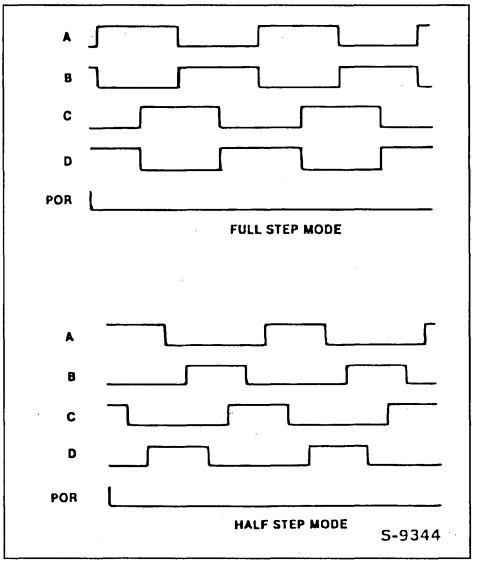
When the internal oscillator is used the pulse width can be modified by changing the value of the capacitor on pin 1.

Increasing the capacitance will widen the pulse width.

The L6506 may be used with either a bridge driver, as shown in figure 1, for bipolar motors or a quad darlington array, as shown in figure 2, for 4 phase unipolar motors. For eigher configuration, half step may be implemented using the 4 phase inputs with the input waveforms shown in figure 3.

The recirculation path for the motor current is through a catch diode for unipolar motors, or a catch diode and one of the lower transistors of the bridge for bipolar motors. Both of these implementations produce a low ripple current since the voltage across the motor during the recirculation time is much less than the power supply voltage. Figure 4 shows the ripple current for bipolar motor applications using the L6506 and the L298N.

Figure 3 : Input Signal for Stepper Motor Drive.

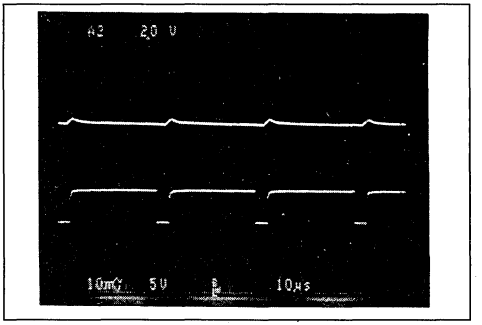


When implementing a half step drive, both outputs of the L6506 will be low during the half step of one phase. This means a very long time is required for the current in the "off" winding to decay when driving bipolar motors.

Alternately, the power stage (L298N) may be inhibited to put the output in the state and achieve a faster current decay.

Since separate V_{ref} inputs are provided for each channel, each of the loads may be programmed independently allowing the device to be used to implement microstepping or applications with different peak and hold currents. In this type of application, changing the reference voltage (V_{ref}) will change the load current, effectively implementing a transconductance amplifier.

Figure 4 : Ripple Current in Bipolar Motors.



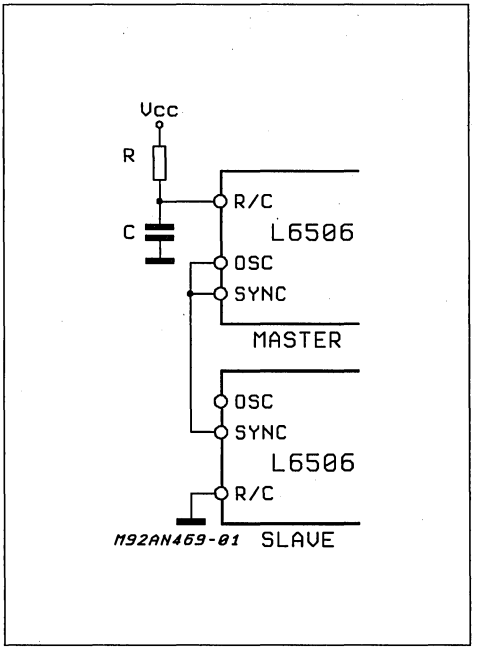
SYNCHRONIZING MULTIPLE DEVICES

Ground noise problems in multiple configurations can be avoided by synchronizing the oscillators. This may be done by connecting the sync pins of each of the devices with the oscillator output of the master device and connecting the R/C pin of the unused oscillators to ground as shown in figure 5. The devices may be synchronized to external circuits by applying synchronizing pulses to the sync pins. It should be noted, however, that the input pulse sets the minimum on time of the outputs and will therefore set a minimum output average current.

SELECTING THE OSCILLATOR COMPONENTS

When selecting the values for the external components for the oscillator one of the primary considerations is the operating frequency. In addition there is another important consideration for these components.

Figure 5 : Synchronizing Multiple Devices.

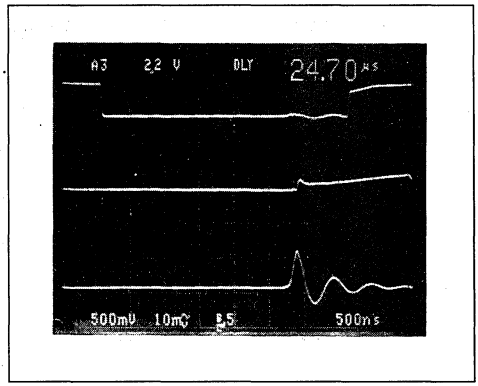


In many applications the reverse recovery current of the free wheeling diodes and of parasitic elements in the power stage will flow through the sensing resistor in addition to the load current. Also there is sometimes noise generated in the system when the power stage is swiched on.

These two sources of error can fool the current limiting stage and make it appear to operate at a subharmonic of the desired frequency. With the proper selection of the oscillator components this behavior can be avoided.

The design of the L6506 is such that the flip-flops used in the device are set dominant so that whenever the sync input is low the Q output of the flip-flop will be high even if the reset is applied by the comparator at the same time. This characteristic of the flip-flops can be used to make the current sensing immune to the recovery currents and noise spikes that occur when the power devices switch. If the sync pulse is longer than the turn on delay time of the power stage, as shown in figure 6, these two sources of errors will be ignored.

Figure 6 : Load Current and Sync Pulse.



To select the proper values for the oscillator components a more detailed equation for the operating frequency and duty cycle of the oscillator is required. The required equations can be derived from the equivalent circuit for the oscillator section shown in figure 7.

As can be seen from figure 7, the full equation for the operating frequency includes not only the external resistance and capacitance but the internal discharge resistor as well. The full equation for the operating frequency is :

$$f = \frac{1}{0.69C1\left[R1 + \left(\frac{R1 \cdot Ri}{R1 + Ri}\right)\right]} \qquad (3)$$

The equations for the active time of the sync pulse (T2), the inactive time of the sync signal (T1) and the duty cycle can also be found by looking at the figure 7 and are :

$$T2 = 0.69C1\,\frac{R1\,Ri}{R1 + Ri} \qquad (4)$$

$$T1 = 0.69\,R1\,C1 \qquad (5)$$

$$DC = \frac{T2}{T1 + T2} \qquad (6)$$

By substituting equations 4 and 5 into equation 6 and solving for the value of R1 the following equations for the external components can be derived:

$$R1 = \left(\frac{1}{DC} - 2\right)Ri \qquad (7)$$

$$C1 = \frac{T1}{0.69\,R1} \qquad (8)$$

Looking at equation 4 it can easily be seen that the minimum pulse width of T2 will occur when the value of Ri is at its minimum and the value of R1 at its maximum. Therefore, when evaluating equation 7 the minimum value for Ri of 700Ω (1 KΩ –30 %) should be used to guarantee the required pulse width.

For a typical application using the L298, which has a maximum turn on delay of 2.5 µs, with the L6506 consider the following operating points:

$$f = 20\ KHz$$

$$T1 + T2 = 50\ \mu s$$

$$T2\ min = 3\ \mu s$$

From equation 6:

$$DC = \frac{3\mu s}{50\mu s} = 0.06$$

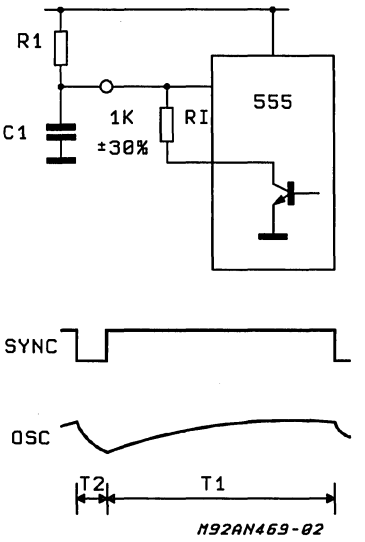
From equation 7:

$$R1 = \left(\frac{1}{0.06} 2\right) 700 = 10.3K\Omega$$

From equation 8:

$$C1 = \frac{47\mu s}{(0.69)\,(10.3K)} = 6.6nF$$

Figure 7 : Oscillator Circuit and Waveforms.

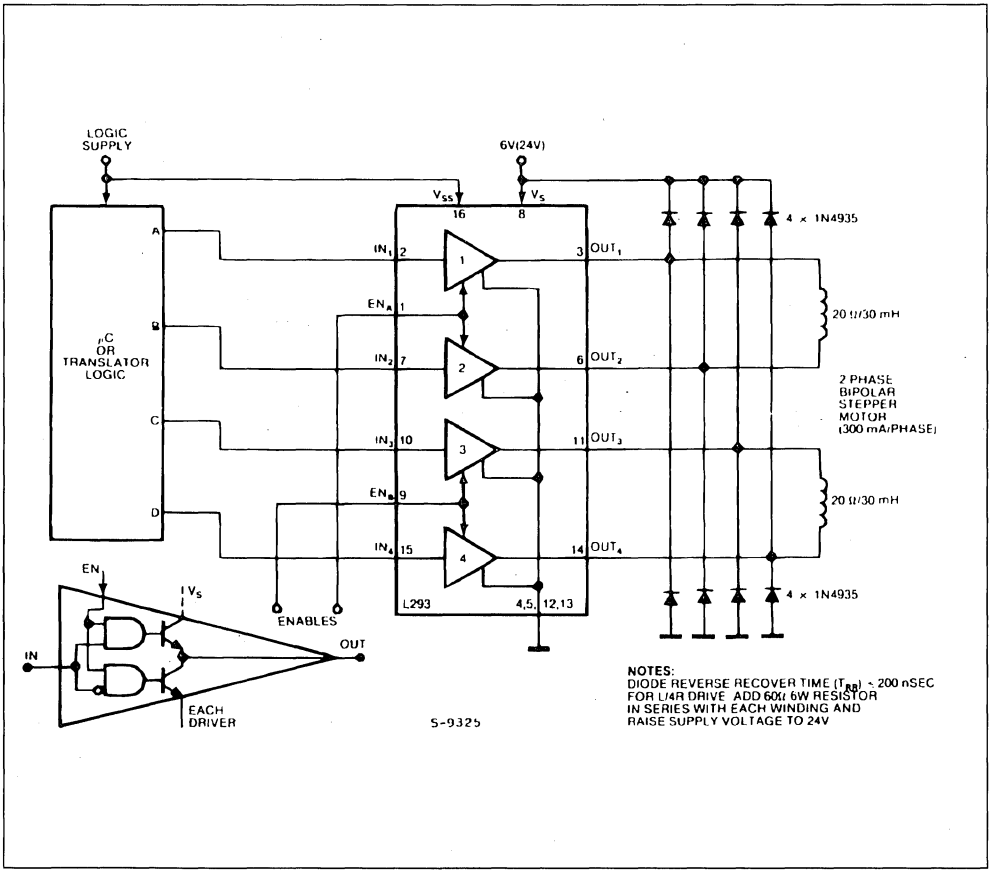


HIGH-POWER, DUAL-BRIDGE ICs EASE STEPPER-MOTOR-DRIVE DESIGN

In addition to simplifying design problems, a family of dedicated chips improves stepper-motor drive-circuit reliability by significantly reducing the component count.

The L293, L293E and L298N dual-bridge ICs (see **box**, "inside the dual-bridge ICs") significantly reduce the problems encountered in the design of stepper-motor drive circuitry. They can, for example, simplify the design and increase the efficiency of constant-current choppers. And with a single chip replacing the transistors and predriver stages, circuit performance improves. Best of all, the devices have applications in complex as well as basic driver networks.

Figure 1 : The Simplest Stepper-motor Drive Technique is the Basic L/R Configuration. Adding Series Resistors and Raising the Supply to Make an L/4R Drive Improves Torque at High Steps rates but Reduces Efficiency.



SIMPLEST DESIGN IS AN L/R DRIVE

The simplest motor-drive configuration (fig. 1) consists of a µC that performs the translator function in software (see **box**, "Generating switching sequences") and drives the motor through a L293 dual bridge. Only eight external components are required ; these are diodes that protect the device's output transistors against inductive spikes generated when a winding de-energizes.

The L293 handles 1A continuous (for higher current use and L298N). However, if you plan to run the motor continuously with two phases on, dissipation will be the limiting factor.

You can improve the performance of this basic L/R drive by increasing the series resistance and raising the supply voltage to restore the original phase current. At high speeds, torque improves, but efficiency decreases. Normally, you increase each winding's resistance by a factor of four through the addition of a 3R series resistance, resulting in the L/4R drive.

INSIDE THE DUAL-BRIDGE ICs

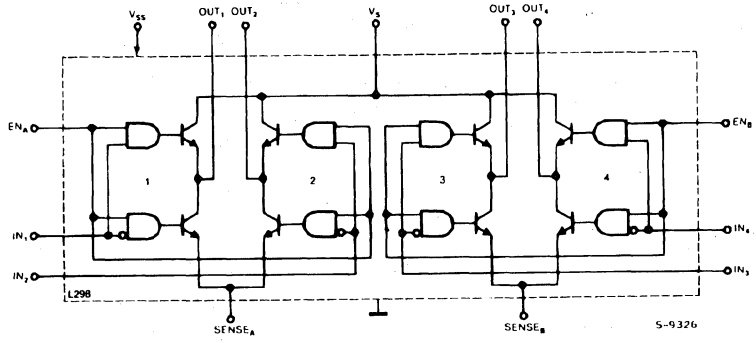
The L293, L293E and L298N (figure) contain two power-transistor bridges, predriver stages, control logic and protection circuitry. There's a control input for each bridge and an enable input for each half bridge ; inputs connect directly to µCs, CMOS or TTL. The ICs integrate level shifters with a separate logic-supply pin. For current sensing, the L293E and L298N have external emitter connections.

A single package drives a 2-phase bipolar stepper motor, challenging the assumption held by many that unipolar motors are easier to drive.

You can use a bipolar motor - simpler and less expensive than a unipolar motor - without building complex power stages. Furthermore, you don't have to worry about simultaneous conduction of a half bridge's source and sink transistors - a basic problem with discrete-component bridge circuits. Chip design makes it impossible for both transistors to be on at the same time.

Designers should also discard the mistaken idea that constant-current chopper drivers are complicated and expensive. You can build one with two bridge ICs and a few passive components.

Dual-bridge driver ICs reduce the parts count of bipolar stepper motors and simplify design. The schematic of the L298N is functionally similar to those of the L293 and L293E.



Type	I_O	$I_{O(PEAK)}$	V_S	Package	Sensing Connections
L293	1 A	1.5 A	36 V	16 DIP	
L293E	1 A	1.5 A	36 V	20 DIP	One Per Half Bridge
L298N	2 A	2.5 A	46 V	Multiwatt 15	One Per Bridge

MULTIPLE SUPPLIES BOOST PERFORMANCE

A dual-level supply also improves the performance of a basic L/R circuit. A high supply voltage yields good torque characteristics when the motor is running. A lower-than-rated voltage provides some holding torque when the motor is at rest, thereby saving power when the motor is idle.

Fig. 2 shows a suitable voltage-switch circuit. R_X sets the holding current, which can be low because a permanent magnet or hybrid stepper motor provides some holding torque at zero current. However, make certain the L293's motor-supply input never goes below the logic-supply voltage. While there's no danger of damaging the device, it's impossible to drive the output transistors correctly under such conditions.

The dual bridge's enable inputs offer a means of extending the chip's flexibility. For example, you can connect them directly to the logic supply - no resistors are needed - to enable the chip permanently. As an alternative, use the enable inputs to disable the motor during the power-on reset sequence.

In wave-drive and half-step modes, use the enable inputs to increase torque at high speeds. When a winding de-energizes, flux collapse is a function of the current-decay rate. During this decay, the de-energized winding opposes the efforts of the next winding in sequence, partially cancelling the torque.

You can minimize this effect by disabling a bridge only when the winding it drives is turned off ; because the $\Delta i/\Delta t$ of an inductor equals E/L, disabling the bridge accelerates the current decay. This action discharges the winding's stored energy through its supply and maintains the terminal voltage E at V_S plus two diode drops. If you were to leave the bridge enabled, the current would flow to ground through one diode and one transistor, and it would lower the terminal voltage. This scheme doesn't apply with drives with two phases on because no winding ever de-energizes.

Figure 2 : Switching the Supply to a Lower Voltage when the Motor is Idle Saves Current without Compromising Driving Power.

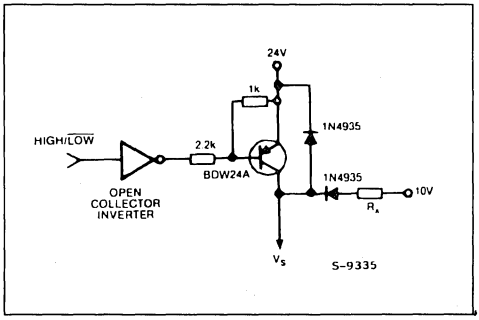
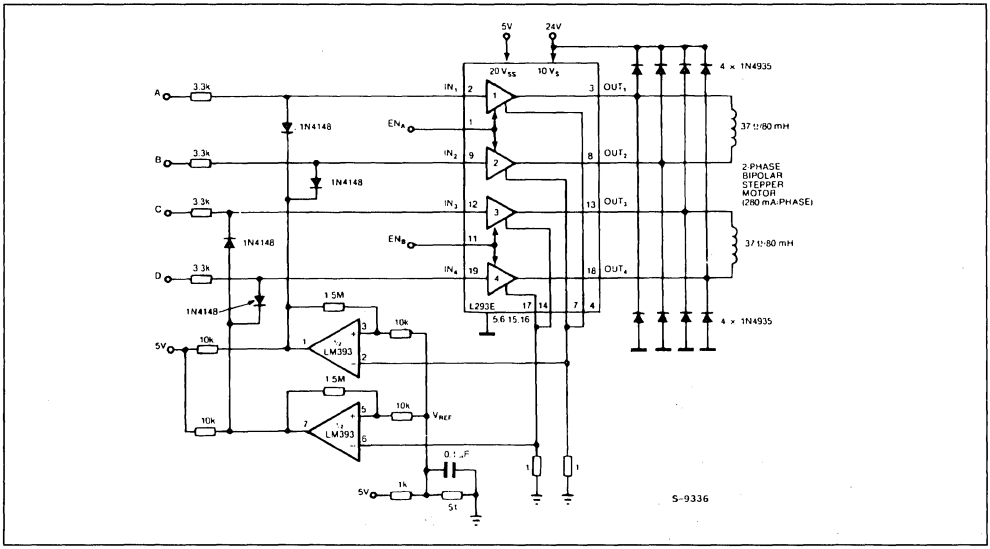


Figure 3 : Maintaining a Constant-average Phase Current this Fixed-ripple Chopper Provides Improved Performance and Efficiency V_{REF} Controls the Phase Current.



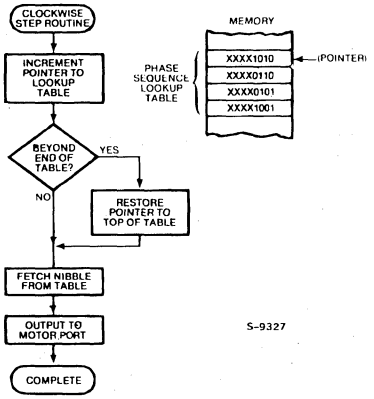
GENERATING SWITCHING SEQUENCES

In addition to selecting a motor and determining power-stage design, you must also decide how to generate the switching sequences that step the motor. Programming a µC or using a special piece of hardware called a transistor accomplishes this task.

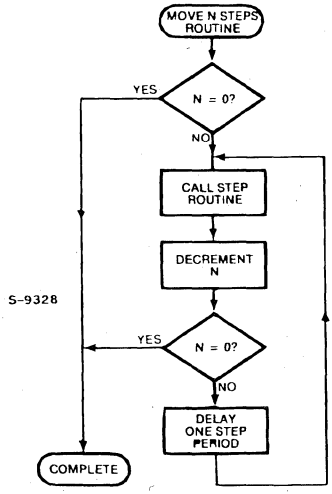
Software translation is more economical, and it is the first choice for large-volume products. Fig. A shows a basic step procedure (a) that you can integrate into a routine (b) ; the routine executes a clockwise rotation of N steps at a fixed rate. The step rate is defined by a software loop, but you can also use programmed timer interrupts.

Fig. A : A µC can generate the phase sequence (a) for a stepper motor. A routine (b) expands a single-step routine into are that executes a move of N steps.

a)



b)

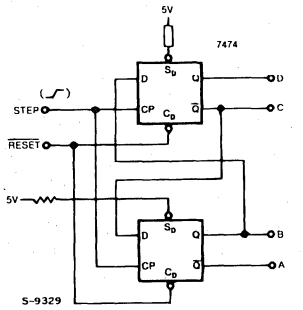


A simpler approach uses the software equivalent of a shift register. For example, you can load a 99 (hex) into a register and take the phases from bits 0 to 3. A Rotate Left instruction yields a clockwise step ; a Rotate Right instruction causes a counterclockwise move.

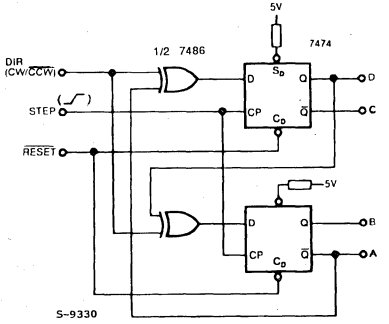
When software translation ties up your µC, lighten the load by adding a hardware translator. In applications involving unidirectional motors, this logic circuit (fig. B) requires only one pulse for each step ; you'll also need a direction signal (b) if your motor rotates in both directions. By adding a 7408 to a 2-phase translator, you can satisfy a wave-drive application (c), while the addition of two OR gates provides fast turn-off in wave-drive mode.

Fig. B : Built a simple 2-phase hardware translator using a dual flip-flop, for single (a) or bidirectional (b) rotation. Add some extra ICs for wave-drive signals (c) and to provide fast turn-off (d).

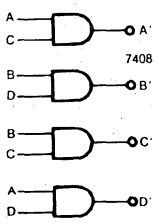
a)



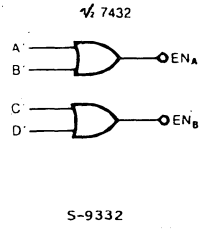
b)



c)



d)



Often a µC controls the translator, setting the direction line and providing a pulse for each step. Software is thus simplified, and if you use a programmed interrupt scheme, the µC is free to handle other tasks. Fig. C describes an absolute-positioning routine for a step with a direction-control translator ; Fig. D outlines how programmed timer interrupts are used to relieve the burden on the C.

Two special cases call for hardware translation. The first is in a system for which you have already designed in control circuitry to provide step and direction signals. The second case involves single-quantity and small-run applications, in which the cost of a few ICs is a small price to pay for simplified software.

Figure C : For use with a Hardware Translator this a Absolute-positioning Routine Sets the Direction Line and Sends the Appropriate Number of Step Pulses.

Notes : Enter with **desired** position **current** position in register or memory location.

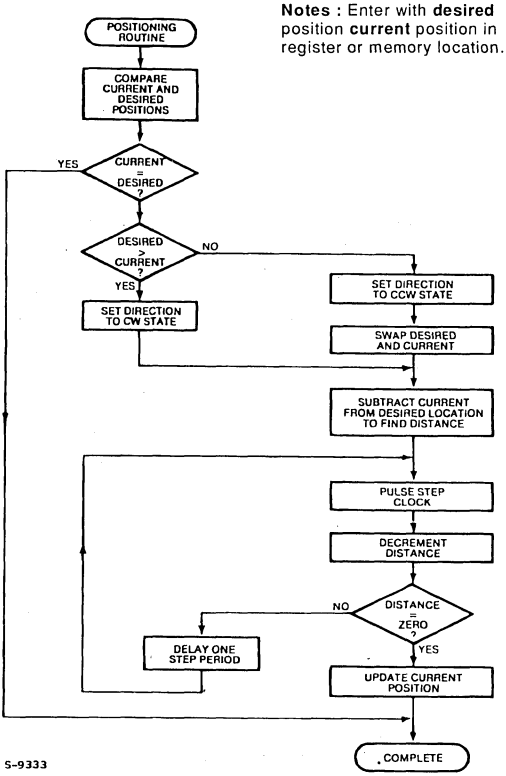
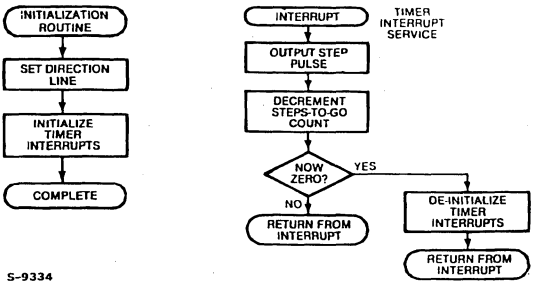


Figure D : To Set a motor Step Rate, used Programmed Timer Interrupts in Place of Software Timing Loops.



CHOPPER CIRCUIT OFFERS MORE ENHANCEMENTS

Adding a chopper circuit to maintain a constant-average phase current improves performance and efficiency. Fig. 3 shown a simple constant-current drive that employs a dual bridge, dual comparator and a few passive components. This circuit requires an L293E, because this dual-bridge IC offers access to the lower emitter connections, thus letting you insert current-sensing resistors.

Operation of this fixed-ripple chopper drive is straightforward. When the µC or translator activates a bridge, the increasing load current raises the voltage across the sensing resistor until it equals the comparator's reference voltage. The comparator then switches, clamping the translator signals through the diodes to deactivate the bridge. As the current decays, the voltage across the sensing resistor decreases until it equals the comparator's lower threshold. The comparator switches again, allowing the µC or translator to activate a bridge and restart the cycle. As long as the translator drives the bridge, this sequence repeats to provide a constant-average phase current with fixed ripple.

V_{ref} adjusts the lower current limit, while the comparator's hysteresis sets the ripple, and hence the peak current. Although a divider establishes the value of V_{ref} in this case, you can employ the dual-supply design approach and switch V_{ref} to a lower value when the motor is idle. In addition, use of a D/A converter establishes V_{ref} for micro-stepping applications. This drive circuit, with its fixed-ripple current characteristics, is well suited for such service.

FIXED-FREQUENCY CHOPPER IS MOTOR INDEPENDENT

Fig. 3's drive has some disadvantages. First, the chopper frequency depends on motor characteristics, and these parameters vary from unit to unit. In addition, it's impossible to synchronize the choppers, and this shortcoming can cause trouble on the ground plane.

Using a flip flop/comparator arrangement (fig. 4) to develop a fixed-frequency chopper overcomes these problems. In this circuit, the NE555 timer generates negative pulses that reset the flip flops to enable the phase-control signals from the transla-

Figure 4 : This Fixed-frequency Constant-current Chopper Driver Enables the Synchronization of Several Drives, thus Minimizing Potential Ground-plane Problems.

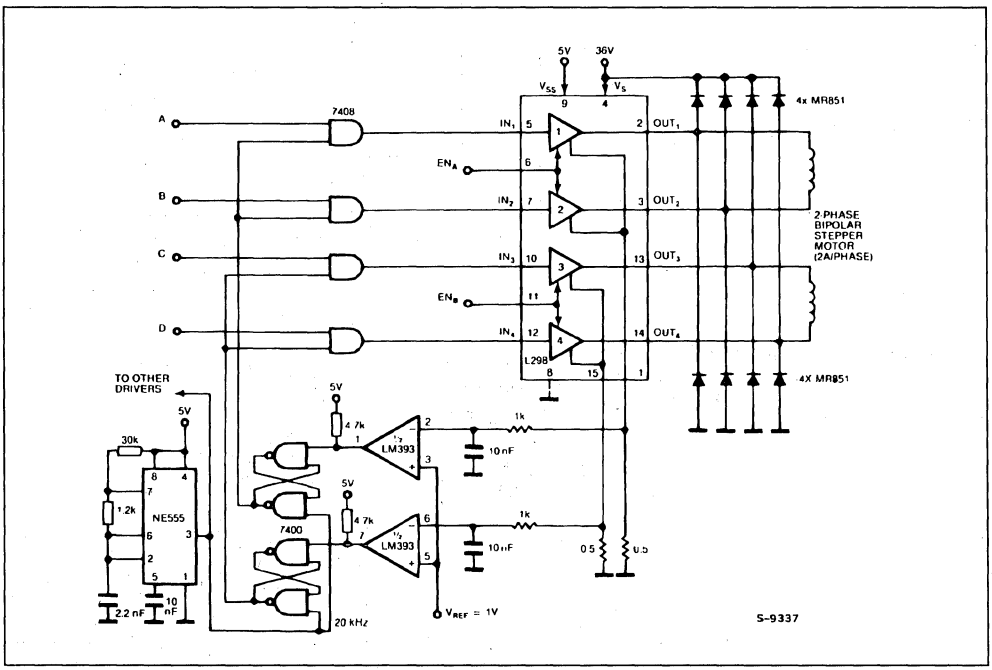
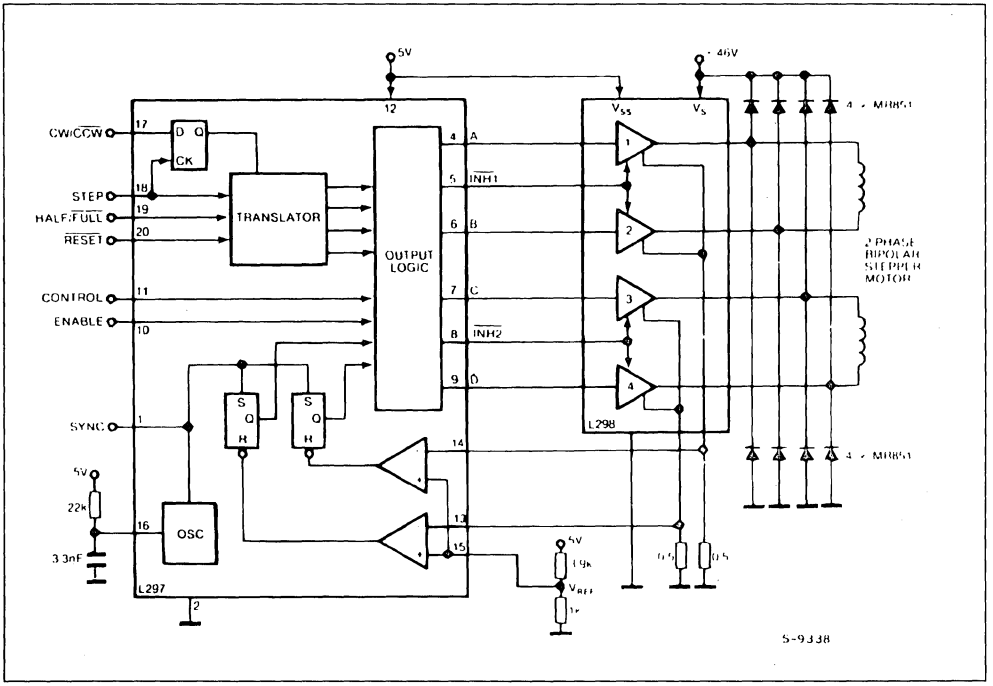


Figure 5 : A Special Translator-chopper Control Circuit cuts the Drivers Components Count to the Minimum.



tor. If these signals are set to energize a winding, the current in that winding rises until the voltage across the sensing resistor switches the comparator, thus setting the flip flop. This disables the phase signals and deactivates the bridge. Current in the winding falls until the next clock pulse resets the flip flop, and the sequence repeats to maintain a constant current.

CONTROLLER IC REDUCES COMPONENT COUNT

If you're using a hardware translation and constant-current choppers, you can further reduce the component count by using a controller chip such as the L297 – a 20-pin DIP that houses a translator and a dual fixed-frequency chopper circuit. Under the control of step and direction inputs, the L297 generates normal, wave-drive and half-step sequences.

As shown in fig. 5, the controller connects directly to a dual bridge. External component requirements are minimal : and RC network to set the chopper frequency and a resistive divider to establish the comparator reference voltage (V_{ref}).

To accommodate motors with a phase current as great as 3.5 A, replace the single dual-bridge IC with two devices configured in parallel (input to input, enable to enable, etc) to form a single bridge. It's extremely important that you pair the half bridges – 1 with 4 and 2 with 3 – to ensure optimum current sharing.

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THE L297 STEPPER MOTOR CONTROLLER

The L297 integrates all the control circuitry required to control bipolar and unipolar stepper motors. Used with a dual bridge driver such as the L298N forms a complete microprocessor-to-bipolar stepper motor interface. Unipolar stepper motor can be driven with an L297 plus a quad darlington array. This note describes the operation of the circuit and shows how it is used.

The L297 Stepper Motor Controller is primarily intended for use with an L298N or L293E bridge driver in stepper motor driving applications.

It receives control signals from the system's controller, usually a microcomputer chip, and provides all the necessary drive signals for the power stage. Additionally, it includes two PWM chopper circuits to regulate the current in the motor windings.

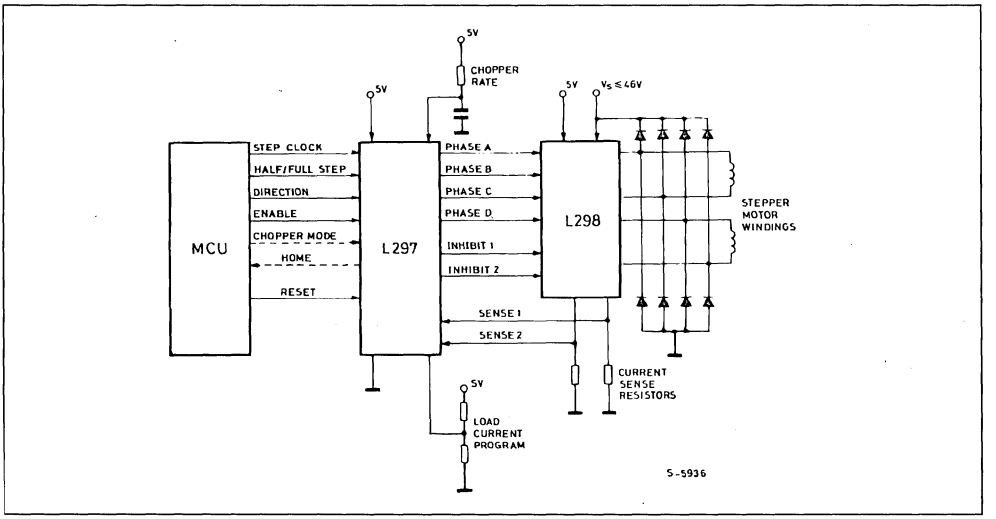
With a suitable power actuator the L297 drives two phase bipolar permanent magnet motors, four phase unipolar permanent magnet motors and four phase variable reluctance motors. Moreover, it handles normal, wave drive and half step drive modes. (This is all explained in the section "Stepper Motor Basics").

Two versions of the device are available : the regular L297 and a special version called L297A. The L297A incorporates a step pulse doubler and is designed specifically for floppy-disk head positioning applications.

ADVANTAGES

The L297 + driver combination has many advantages : very few components are required (so assembly costs are low, reliability high and little space required), software development is simplified and the burden on the micro is reduced. Further, the choice of a two-chip approach gives a high degree of flexibility-the L298N can be used on its own for DC motors and the L297 can be used with any power stage, including discrete power devices (it provides 20mA drive for this purpose).

Figure 1 : In this typical configuration an L297 stepper motor controller and L298 dual bridge driver combine to form a complete microprocessor to bipolar stepper motor interface.



For bipolar motors with winding currents up to 2A the L297 should be used with the L298N ; for winding currents up to 1A the L293E is recommended (the L293 will also be useful if the chopper isn't needed). Higher currents are obtained with power transistors or darlingtons and for unipolar motors a darlington array such as the ULN2075B is suggested. The block diagram, figure 1, shows a typical system.

Applications of the L297 can be found almost everywhere ... printers (carriage position, daisy position, paper feed, ribbon feed), typewriters, plotters, numerically controlled machines, robots, floppy disk drives, electronic sewing machines, cash registers, photocopiers, telex machines, electronic carburetos, telecopiers, photographic equipment, paper tape readers, optical character recognisers, electric valves and so on.

The L297 is made with SGS' analog/digital compatible I^2L technology (like Zodiac) and is assembled in a 20-pin plastic DIP. A 5V supply is used and all signal lines are TTL/CMOS compatible or open collector transistors. High density is one of the key features of the technology so the L297 die is very compact.

THE L298N AND L293E

Since the L297 is normally used with an L298N or L293E bridge driver a brief review of these devices will make the rest of this note easier to follow.

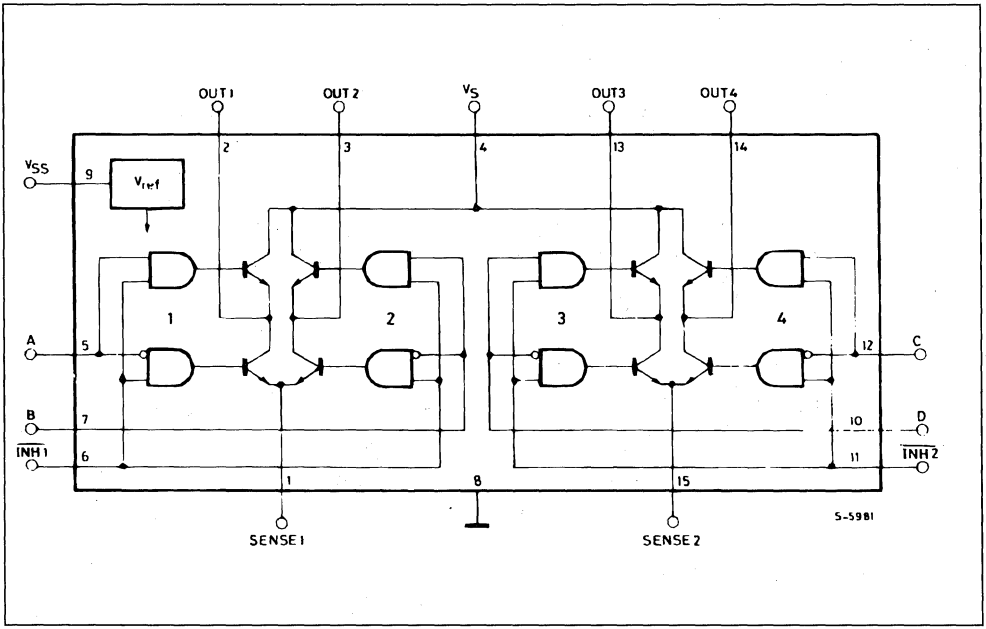
The L298N and L293E contain two bridge driver stages, each controlled by two TTL-level logic inputs and a TTL-level enable input. In addition, the emitter connections of the lower transistors are brought out to external terminals to allow the connection of current sensing resistors (figure 2).

For the L298N SGS' innovative ion-implanted high voltage/high current technology is used, allowing it to handle effective powers up to 160W (46V supply, 2A per bridge). A separate 5V logic supply input is provided to reduce dissipation and to allow direct connection to the L297 or other control logic.

In this note the pins of the L298N are labelled with the pin names of the corresponding L297 terminals to avoid unnecessary confusion.

The L298N is supplied in a 15-lead Multiwatt plastic power package. It's smaller brother, the functionally identical L293E, is packaged in a Powerdip – a copper frame DIP that uses the four center pins to conduct heat to the circuit board copper.

Figure 2 : The L298N contains two bridge drivers (four push pull stages) each controlled by two logic inputs and an enable input. External emitter connections are provided for current sense resistors. The L293E has external connections for all four emitters.



STEPPER MOTOR BASICS

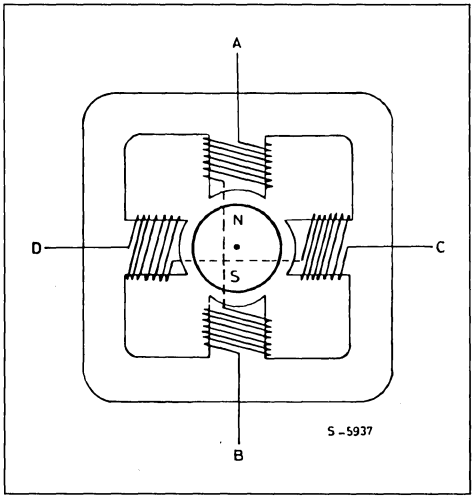
There are two basic types of stepper motor in common use : permanent magnet and variable reluctance. Permanent magnet motors are divided into bipolar and unipolar types.

BIPOLAR MOTORS

Simplified to the bare essentials, a bipolar permanent magnet motor consists of a rotating permanent magnet surrounded by stator poles carrying the windings (figure 3). Bidirectional drive current is used and the motor is stepped by switching the windings in sequence.

For a motor of this type there are three possible drive sequences.

Figure 3 : Greatly simplified, a bipolar permanent magnet stepper motor consist of a rotaring magnet surrounded by stator poles as shown.



The first is to energize the windings in the sequence AB/CD/BA/DC (BA means that the winding AB is energized but in the opposite sense). This sequence is known as "one phase on" full step or wave drive mode. Only one phase is energized at any given moment (figure 4a).

The second possibility is to energize both phases together, so that the rotor always aligns itself between two pole positions. Called "two-phase-on" full step, this mode is the normal drive sequence for a bipolar motor and gives the highest torque (figure 4b).

The third option is to energize one phase, then two, then one, etc., so that the motor moves in half step increments. This sequence, known as half step mode, halves the effective step angle of the motor but gives a less regular torque (figure 4c).

For rotation in the opposite direction (counter-clockwise) the same three sequences are used, except of course that the order is reserved.

As shown in these diagrams the motor would have a step angle of 90°. Real motors have multiple poles to reduce the step angle to a few degrees but the number of windings and the drive sequences are unchanged. A typical bipolar stepper motor is shown in figure 5.

UNIPOLAR MOTORS

A unipolar permanent magnet motor is identical to the bipolar machine described above except that bifilar windings are used to reverse the stator flux, rather than bidirectional drive (figure 6).

This motor is driven in exactly the same way as a bipolar motor except that the bridge drivers are replaced by simple unipolar stages - four darlingtons or a quad darlington array. Clearly, unipolar motors are more expensive because thay have twice as many windings. Moreover, unipolar motors give less torque for a given motor size because the windings are made with thinner wire. In the past unipolar motors were attractive to designers because they simplify the driver stage. Now that monolithic push pull drivers like the L298N are available bipolar motors are becoming more popular.

All permanent magnet motors suffer from the counter EMF generated by the rotor, which limits the rotation speed. When very high slewing speeds are necessary a variable reluctance motor is used.

Figure 4 : The three drive sequences for a two phase bipolar stepper motor. Clockwise rotation is shown.

Figure 4a : Wave drive (one phase on).

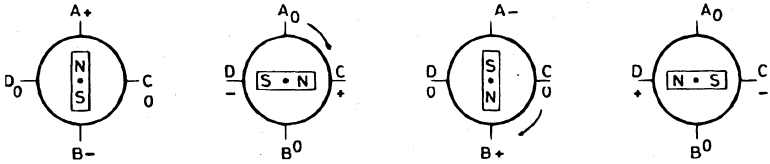


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Figure 4b : Two phase on drive.

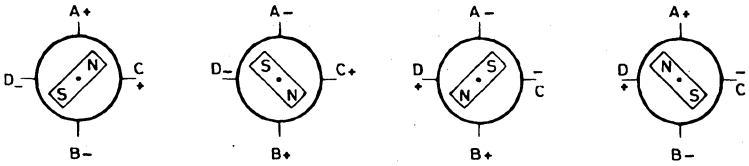

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Figure 4c : Half step drive.

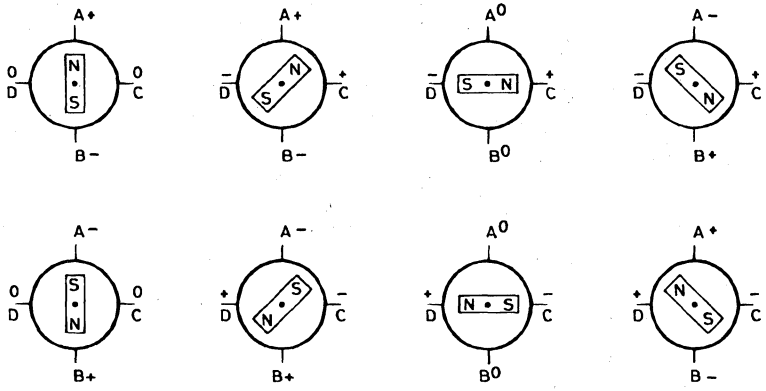


Figure 5 : A real motor. Multiple poles are normally employed to reduce the step angle to a practical value. The principle of operation and drive sequences remain the same.

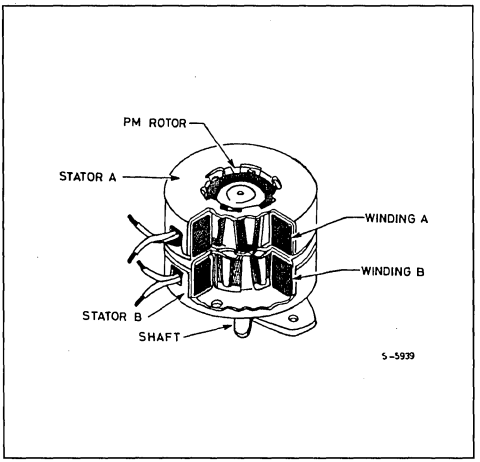
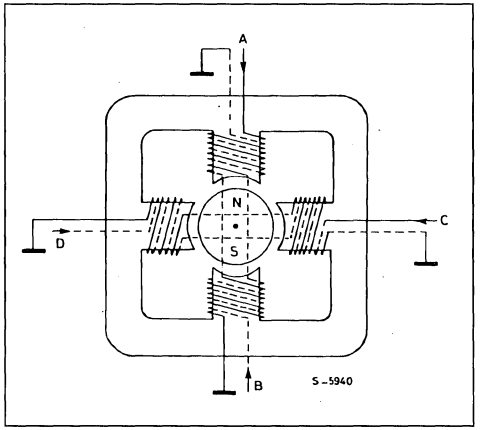


Figure 6 : A unipolar PM motor uses bifilar windings to reverse the flux in each phase.



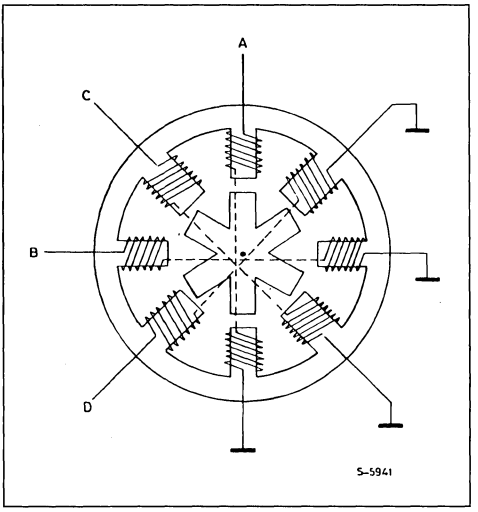
VARIABLE RELUCTANCE MOTORS

A variable reluctance motor has a non-magnetized soft iron rotor with fewer poles than the stator (figure 7). Unipolar drive is used and the motor is stepped by energizing stator pole pairs to align the rotor with the pole pieces of the energized winding.

Once again three different phase sequences can be used. The wave drive sequence is A/C/B/D ; two-phase-on is AC/CB/BD/DA and the half step sequence is A/AC/C/BC/B/BD/D/DA. Note that the step angle for the motor shown above is 15 °, not 45 °.

As before, pratical motors normally employ multiple poles to give a much smaller step angle. This does not, however, affect the principle of operation of the drive sequences.

Figure 7 : A variable reluctance motor has a soft iron rotor with fewer poles than the stator. The step angle is 15 ° for this motor.



GENERATING THE PHASE SEQUENCES

The heart of the L297 block diagram, figure 8, is a block called the translator which generates suitable phase sequences for half step, one-phase-on full step and two-phase-on full step operation. This block is controlled by two mode inputs – direction (CW/ CCW) and HALF/ FULL – and a step clock which advances the translator from one step to the next.

Four outputs are provided by the translator for subsequent processing by the output logic block which implements the inhibit and chopper functions.

Internally the translator consists of a 3-bit counter plus some combinational logic which generates a basic eight-step gray code sequence as shown in figure 9. All three drive sequences can be generated easily from this master sequence. This state sequence corresponds directly to half step mode, selected by a high level on the HALF/ FULL input.

The output waveforms for this sequence are shown in figure 10.

Note that two other signals, $\overline{INH1}$ and $\overline{INH2}$ are generated in this sequence. The purpose of these signals is explained a little further on.

The full step modes are both obtained by skipping alternate states in the eight-step sequence. What happens is that the step clock bypasses the first stage of the 3-bit counter in the translator. The least significant bit ot this counter is not affected therefore the sequence generated depends on the state of the translator when full step mode is selected (the HALF/ FULL input brought low).

If full step mode is selected when the translator is at any odd-numbered state we get the two-phase-on full step sequence shown in figure 11.

By contrast, one-phase-on full step mode is obtained by selecting full step mode when the translator is at an even-numbered state (figure 12).

Figure 8 : The L297 contains translator (phase sequence generator), a dual PWM chopper and output control logic.

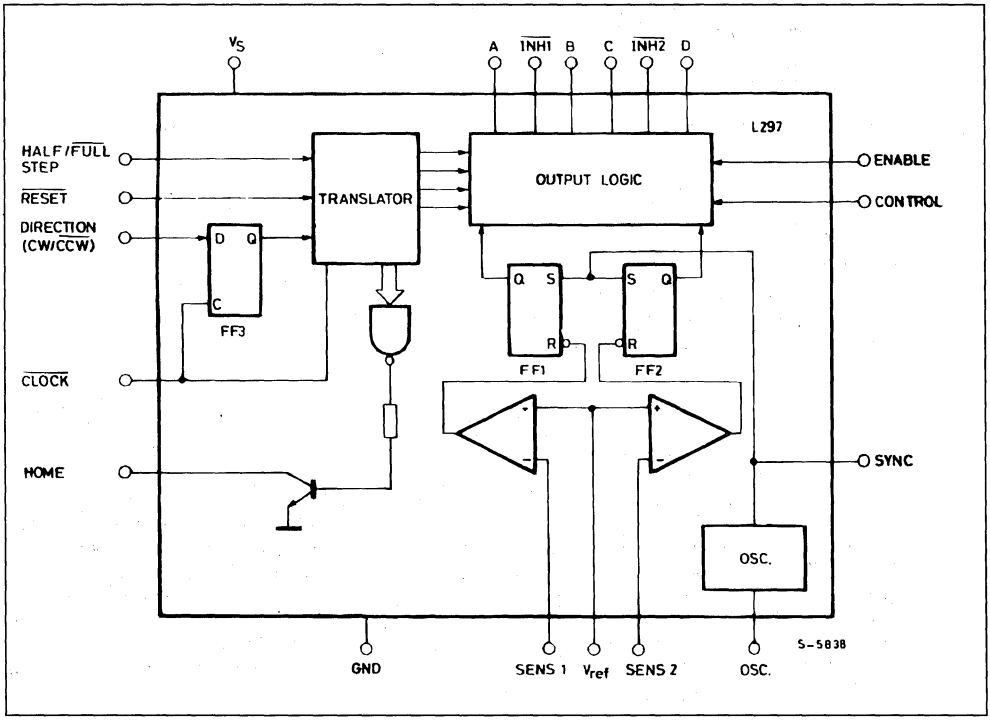


Figure 9 : The eight step master sequence of the translator. This corresponds to half step mode. Clockwise rotation is indicated.

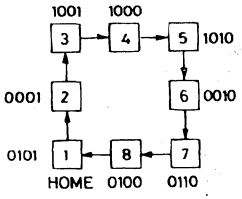


Figure 10 : The output waveforms corresponding to the half step sequence. The chopper action in not shown.

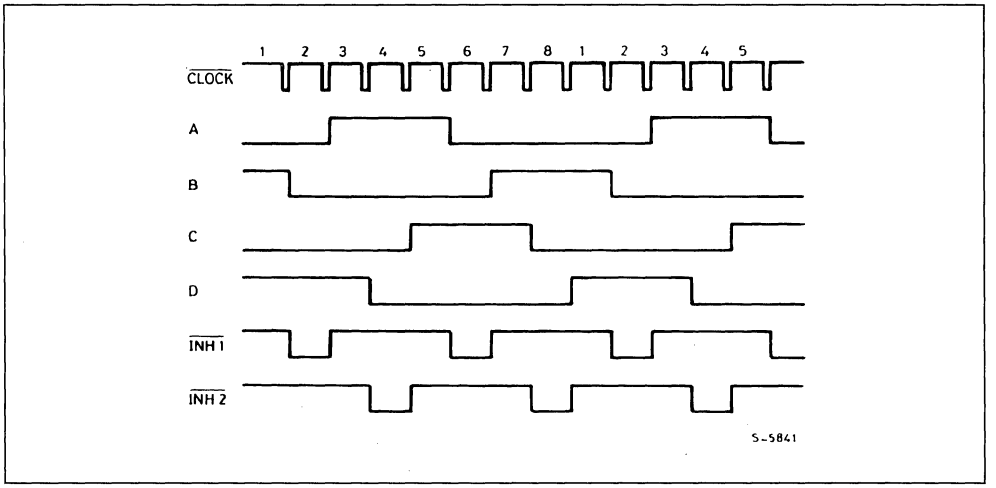


Figure 11 : State sequence and output waveforms for the two phase on sequence. $\overline{INH1}$ and $\overline{INH2}$ remain high throughout.

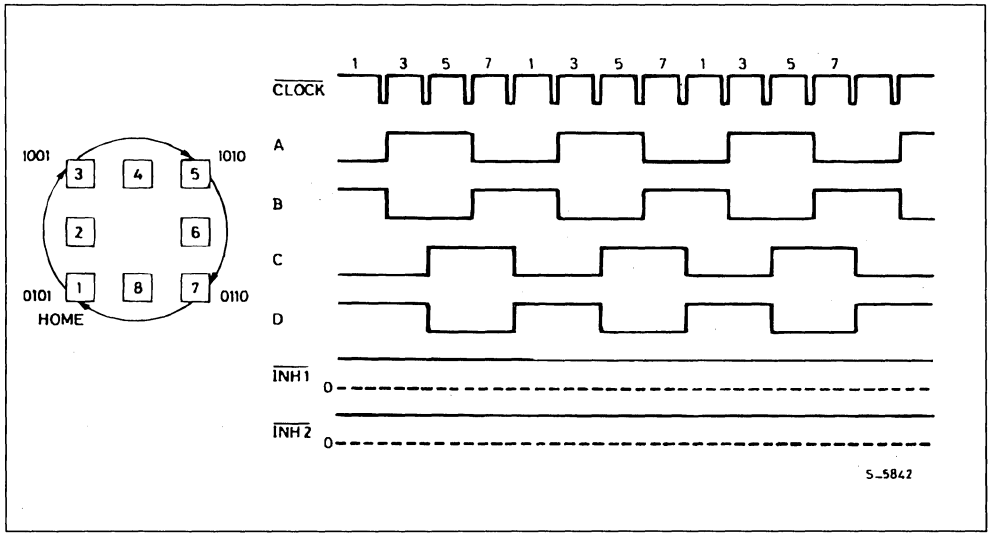
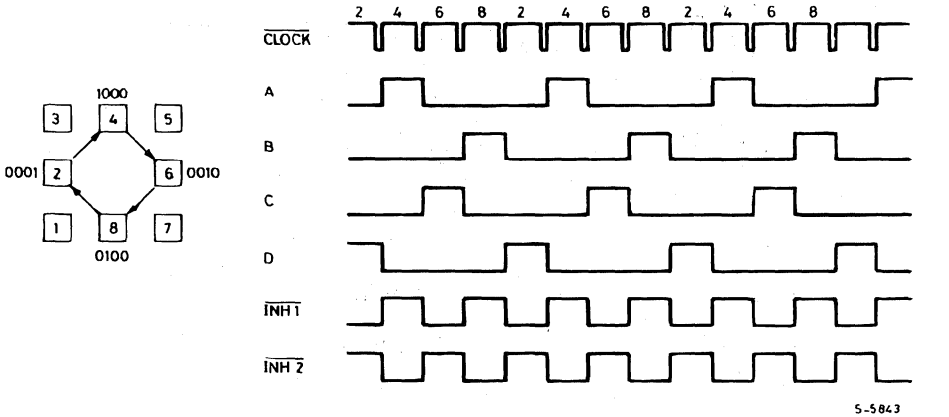


Figure 12 : State Sequence and Output Waveforms for Wave Drive (one phase on).



INH1 AND INH2

In half step and one-phase-on full step modes two other signals are generated : INH1 and INH2. These are inhibit signals which are coupled to the L298N's enable inputs and serve to speed the current decay, when a winding is switched off.

Since both windings are energized continuously in two-phase-on full step mode no winding is ever switched off and these signals are not generated.

To see what these signals do let's look at one half of the L298N connected to the first phase of a two-phase bipolar motor (figure 13). Remember that the L298N's A and B inputs determine which transistor in each push pull pair will be on. INH1, on the other hand, turns off all four transistors.

Assume that A is high, B low and current flowing through Q1, Q4 and the motor winding. If A is now brought low the current would recirculate through D2, Q4 and R_S, giving a slow decay and increased dissipation in R_S. If, on a other hand, A is brought low and INH1 is activated, all four transistors are turned off. The current recirculates in this case from ground to V_S via D2 and D3, giving a faster decay thus allowing faster operation of the motor. Also, since the recirculation current does not flow through R_S, a less expensive resistor can be used.

Exactly the same thing happens with the second winding, the other half of the L298 and the signals C, D and INH2.

The INH1 and INH2 signals are generated by OR functions :

$$A + B = \overline{INH1} \qquad C + D = \overline{INH2}$$

However, the output logic is more complex because inhibit lines are also used by the chopper, as we will see further on.

OTHER SIGNALS

Two other signals are connected to the translator block : the RESET input and the HOME output

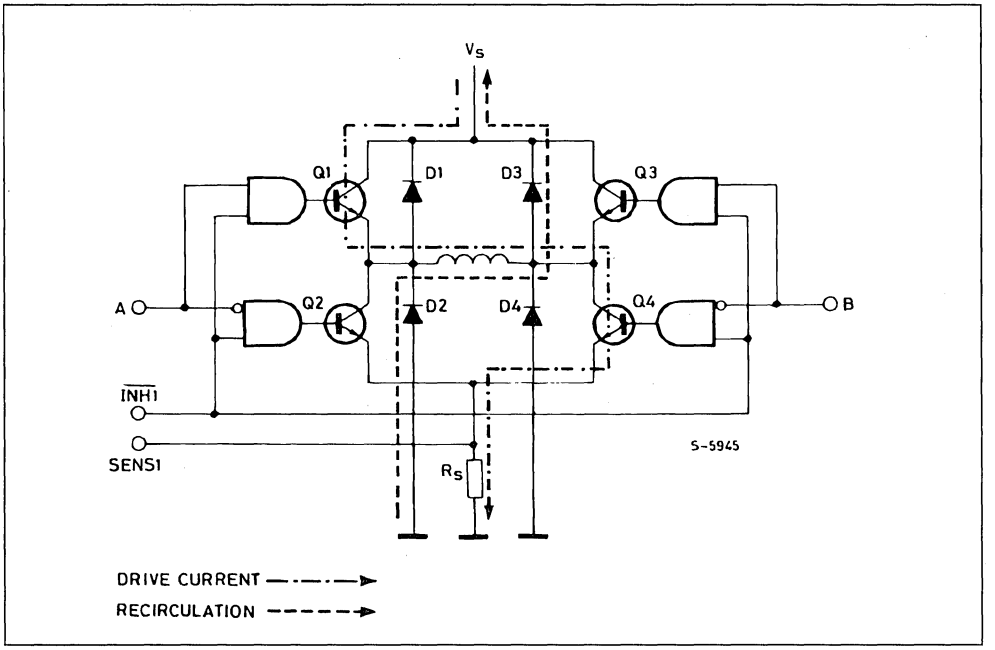
RESET is an asynchronous reset input which restores the translator block to the home position (state 1, ABCD = 0101). The HOME output (open collector) signals this condition and is intended to the ANDed with the output of a mechanical home position sensor.

Finally, there is an ENABLE input connected to the output logic. A low level on this input brings INH1, INH2, A, B, C and D low. This input is useful to disable the motor driver when the system is initialized.

LOAD CURRENT REGULATION

Some form of load current control is essential to obtain good speed and torque characteristics. There are several ways in which this can be done – switching the supply between two voltages, pulse rate modulation chopping or pulse width modulation chopping.

Figure 13 : When a winding is switched off the inhibit input is activated to speed current decay. If this were not done the current would recirculate through D2 and Q4 in this example. Dissipation in R_S is also reduced.

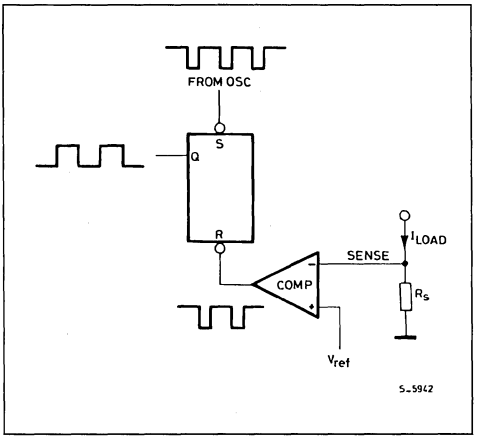


The L297 provides load current control in the form of two PWM choppers, one for each phase of a bipolar motor or one for each pair of windings for a unipolar motor. (In a unipolar motor the A and B windings are never energized together so thay can share a chopper ; the same applies to C and D).

Each chopper consists of a comparator, a flip flop and an external sensing resistor. A common on chip oscillator supplies pulses at the chopper rate to both choppers.

In each chopper (figure 14) the flip flop is set by each pulse from the oscillator, enabling the output and allowing the load current to increase. As it increases the voltage across the sensing resistor increases, and when this voltage reaches V_{ref} the flip flop is reset, disabling the output until the next oscillator pulse arrives. The output of this circuit (the flip flop's Q output) is therefore a constant rate PWM signal. Note that V_{ref} determines the peak load current.

Figure 14 : Each chopper circuit consists of a comparator, flip flop and external sense resistor. A common oscillator clocks both circuits.



PHASE CHOPPING AND INHIBIT CHOPPING

The chopper can act on either the phase lines (ABCD) or on the inhibit lines INH1 and INH2. An input named CONTROL decides which. Inhibit chopping is used for unipolar motors but you can choose between phase chopping and inhibit chopping for bipolar motors. The reasons for this choice are best explained with another example.

First let's examine the situation when the phase lines are chopped.

As before, we are driving a two phase bipolar motor and A is high, B low (figure 15). Current therefore flows through Q1, winding, Q4 and R_S. When the voltage across R_S reaches V_{ref} the chopper brings B high to switch off the winding.

The energy stored in the winding is dissipated by current recirculating through Q1 and D3. Current decay through this path is rather slow because the voltage on the winding is low ($V_{CEsat\,Q1} + V_{D3}$) (figure 16).

Why is B pulled high, why push A low ? The reason is to avoid the current decaying through R_S. Since the current recirculates in the upper half of the bridge, current only flows in the sensing resistor when the winding is driven. Less power is therefore dissipated in R_S and we can get away with a cheaper resistor.

This explain why phase chopping is not suitable for unipolar motors : when the A winding is driven the chopper acts on the B winding. Clearly, this is no use at all for a variable reluctance motor and would be slow and inefficient for a bifilar wound permanent magnet motor.

The alternative is to tie the CONTROL input to ground so that the chopper acts on INH1 and INH2. Looking at the same example, A is high and B low. Q1 and Q4 are therefore conducting and current flows through Q1, the winding, Q4 and R_S, (figure 17).

Figure 15 : Phase Chopping. In this example the current X is interrupted by activating B, giving the recirculation path Y. The alternative, de-activating A, would give the recirculation path Z, increasing dissipation in R_S.

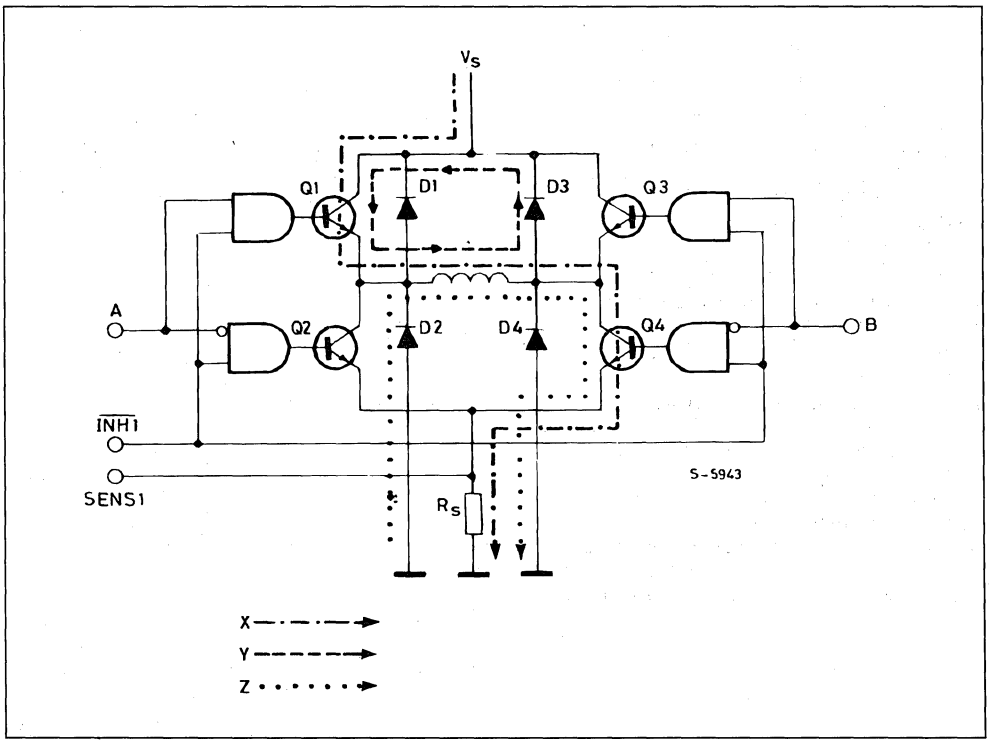


Figure 16 : Phase Chopping Waveforms. The example shows AB winding energized with A positive with respect to B. Control is high.

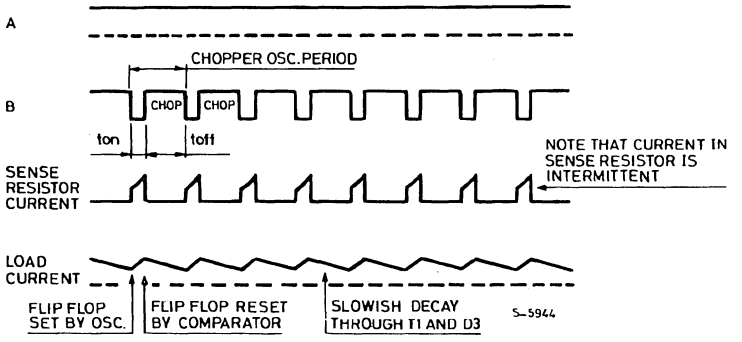
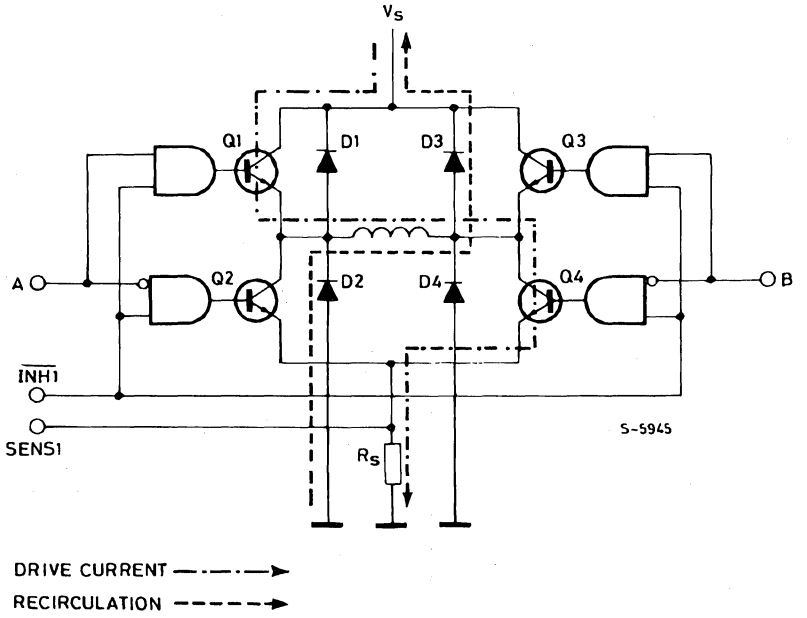


Figure 17 : Inhibit Chopping. The drive current (Q1, winding, Q4) in this case is interrupted by activating $\overline{INH1}$. The decay path through D2 and D3 is faster than the path Y of Figure 15.



In this case when the voltage accross R_S reaches V_{REF} the chopper flip flop is reset and INH1 activated (brought low). INH1, remember, turns off all four transistors therefore the current recirculates from ground, through D2, the winding and D3 to V_S. Discharged across the supply, which can be up to 46V, the current decays very rapidly (figure 18).

The usefulness of this second faster decay option is fairly obvious ; it allows fast operation with bipolar motors and it is the only choice for unipolar motors. But why do we offer the slower alternative, phase chopping ?

The answer is that we might be obliged to use a low chopper rate with a motor that does not store much energy in the windings. If the decay is very fast the average motor current may be too low to give an useful torque. Low chopper rates may, for example, be imposed if there is a larger motor in the same system. To avoid switching noise on the ground plane all drivers should be synchronized and the chopper rate is therefore determined by the largest motor in the system.

Multiple L297s are synchronized easily using the SYNC pin. This pin is the squarewave output of the on-chip oscillator and the clock input for the choppers. The first L297 is fitted with the oscillator components and outputs a sqarewave signal on this pin (figure 19). Subsequent L297s do not need the oscillator components and use SYNC as a clock input. An external clock may also be injected at this terminal if an L297 must be synchronized to other system components.

Figure 18 : Inhibit Chopper Waveforms. Winding AB is energized and CONTROL is low.

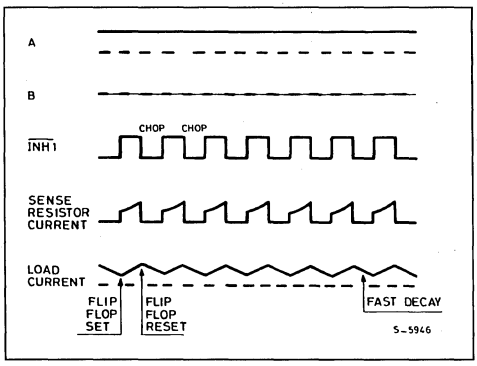
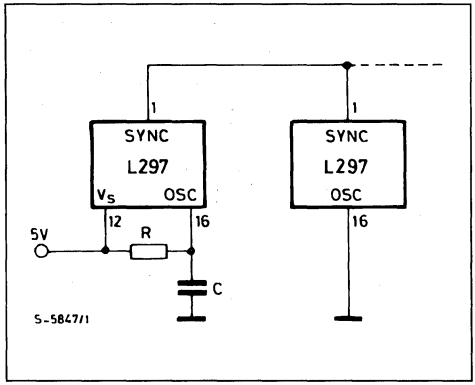


Figure 19 : The Chopper oscillator of multiple L297s are synchronized by connecting the SYNC Inputs together.



THE L297A

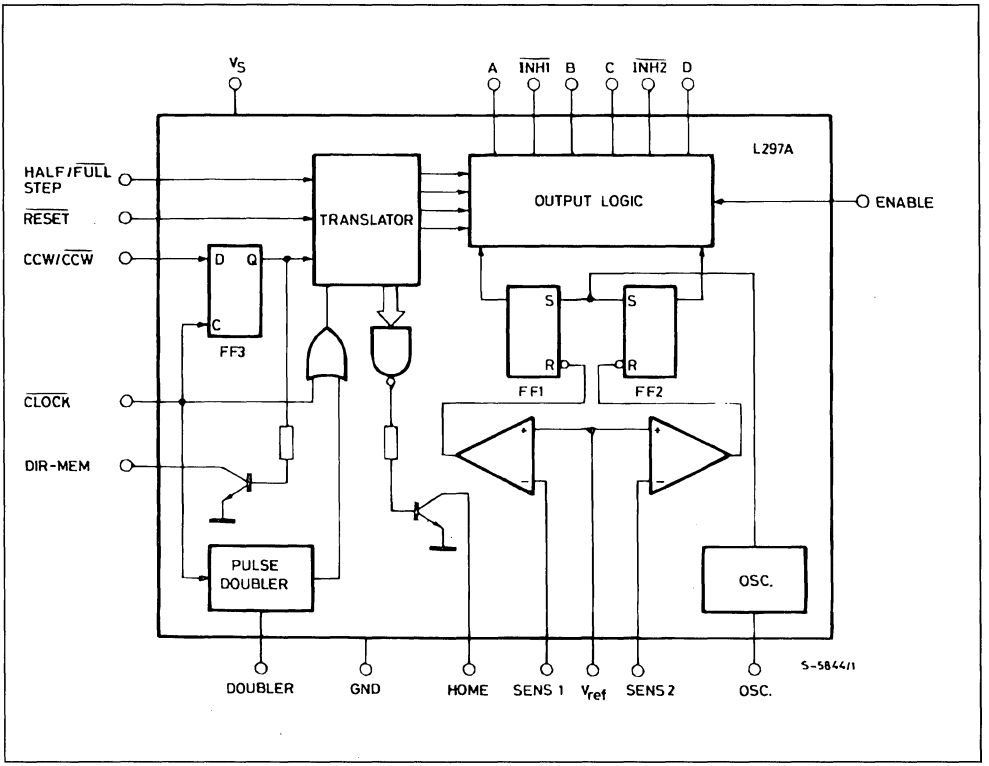
The L297A is a special version of the L297 developed originally for head positioning in floppy disk drives. It can, however, be used in other applications.

Compared to the standard L297 the difference are the addition of a pulse doubler on the step clock input and the availability of the output of the direction flip flop (block diagram, figure 20). To add these functions while keeping the low-cost 20-pin package the CONTROL and SYNC pins are not available on this version (they are note needed anyway). The chopper acts on the ABCD phase lines.

The pulse doubler generates a ghost pulse internally for each input clock pulse. Consequently the translator moves two steps for each input pulse. An external RC network sets the delay time between the input pulse and ghost pulse and should be chosen so that the ghost pulses fall roughly halfway between input pulses, allowing time for the motor to step.

This feature is used to improve positioning accuracy. Since the angular position error of a stepper motor is noncumulative (it cancels out to zero every four steps in a four step sequence motor) accuracy is improved by stepping two of four steps at a time.

Figure 20 : The L297A, includes a clock pulse doubler and provides an output from the direction flip flop (DIR – MEM).



APPLICATION HINTS

Bipolar motors can be driven with an L297, an L298N or L293E bridge driver and very few external components (figure 21). Together these two chips form a complete microprocessor-to-stepper motor interface. With an L298N this configuration drives motors with winding currents up to 2A ; for motors up to 1A per winding and L293E is used. If the PWM choppers are not required an L293 could also be used (it doesn't have the external emitter connections for sensing resistors) but the L297 is underutilized. If very high powers are required the bridge driver is replaced by an equivalent circuit made with discrete transistors. For currents to 3.5A two L298N's with paralleled outputs may be used.

For unipolar motors the best choice is a quad darlington array. The L702B can be used if the choppers are not required but an ULN2075B is preferred.

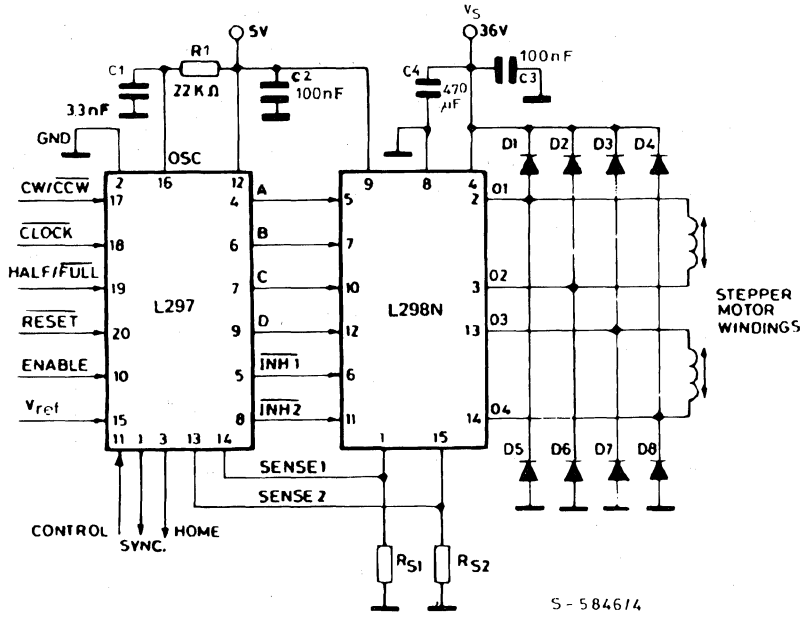
This quad darlington has external emitter connections which are connected to sensing resistors (figure 22). Since the chopper acts on the inhibit lines, four AND gates must be added in this application.

Also shown in the schematic are the protection diodes.

In all applications where the choppers are not used it is important to remember that the sense inputs must be grounded and V_{REF} connected either to V_S or any potential between V_S and ground.

The chopper oscillator frequency is determined by the RC network on pin 16. The frequency is roughly 1/0.7 RC and R must be more than 10 KΩ. When the L297A's pulse doubler is used, the delay time is determined by the network R_d C_d and is approximately 0.75 R_d C_d .R_d should be in the range 3 kΩ to 100 kΩ (figure 23).

Figure 21 : This typical application shows an L297 and L298N driving a Bipolar Stepper Motor with phase currents up to 2A.



R_{S1} R_{S2} = 0.5 Ω
D1 to D8 = 2 Fast Diodes

VF ≤ 1.2 @ I = 2 A
trr ≤ 200 ns

Figure 22 : For Unipolar Motors a Quad Darlington Array is coupled to the L297. Inhibit chopping is used so the four AND gates must be added.

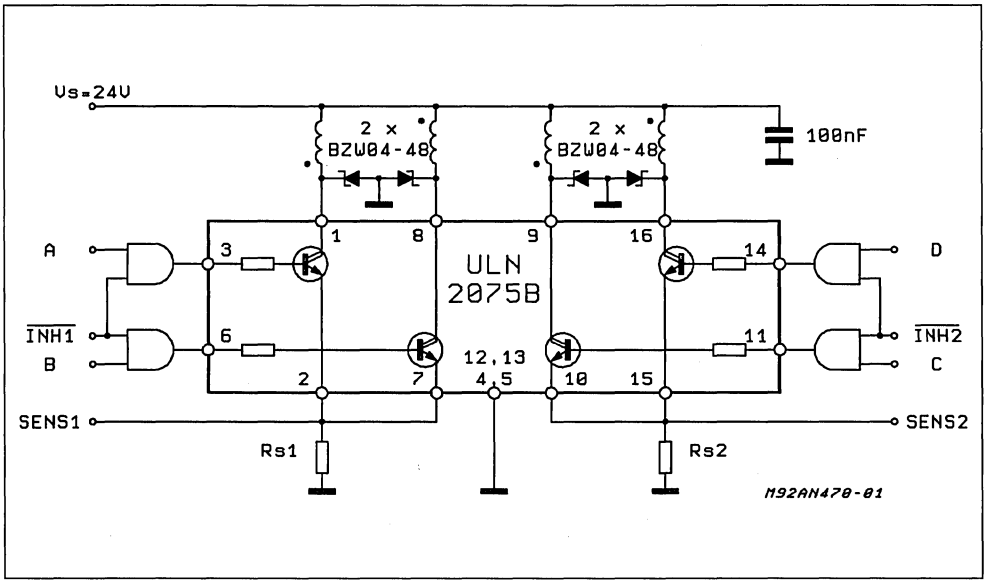
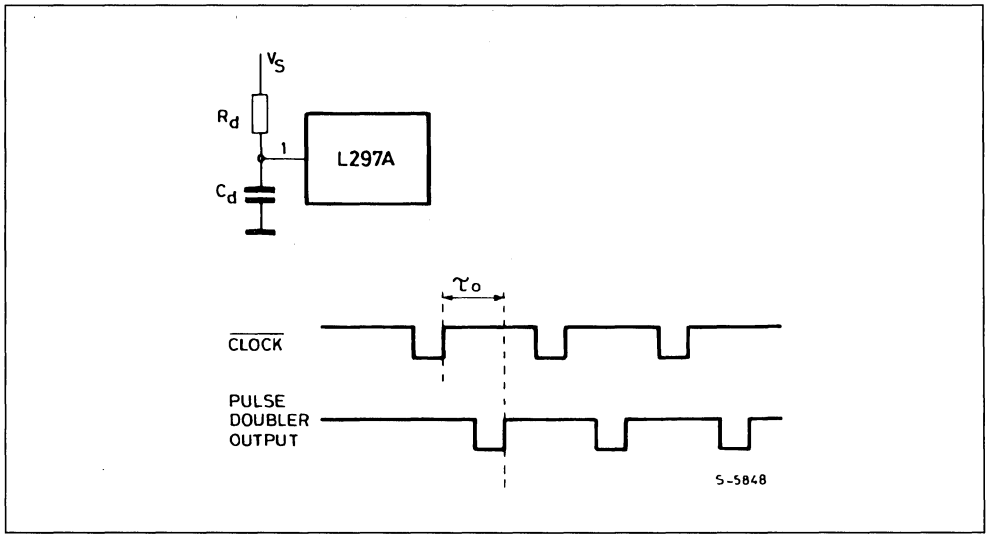


Figure 23 : The Clock pulse doubler inserts a ghost pulse τ_o seconds after the Input clock pulse. $R_d C_d$ is closen to give a delay of approximately half the Input clock period.



PIN FUNCTIONS – L297

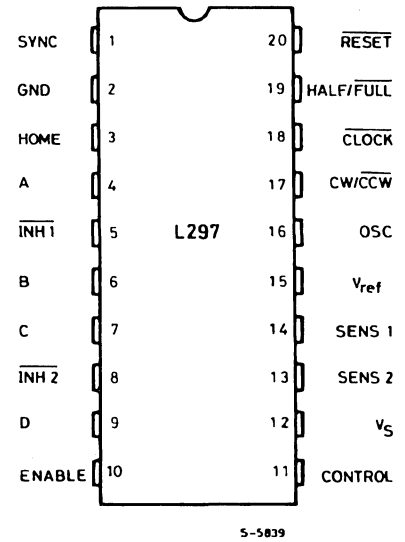
N°	Name	Function
1	SYNC	Output of the On-chip Chopper Oscillator. The SYNC connections of all L297s to be synchronized are connected together and the oscillator components are omitted on all but one. If an external clock source is used it is injected at this terminal.
2	GND	Ground Connection.
3	HOME	Open collector output that indicates when the L297 is in its initial state (ABCD = 0101). The transistor is open when this signal is active.
4	A	Motor phase A drive signal for power stage.
5	$\overline{INH1}$	Active low inhibit control for driver stages of A and B phases. When a bipolar bridge is used this signal can be used to ensure fast decay of load current when a winding is de-energized. Also used by chopper to regulate loadcurrent if CONTROL input is low.
6	B	Motor phase B drive signal for power stage.
7	C	Motor phase C drive signal for power stage.
8	$\overline{INH2}$	Active low inhibit control for drive stages of C and D phases. Same functions as $\overline{INH1}$.
9	D	Motor phase D drive signal for power stage.
10	ENABLE	Chip enable input. When low (inactive) $\overline{INH1}$, $\overline{INH2}$, A, B, C and D are brought low.
11	CONTROL	Control input that defines action of chopper. When low chopper acts on INH1 and INH2 ; when high chopper acts on phase lines ABCD.
12	V_s	5 V Supply Input.
13	$SENS_2$	Input for load current sense voltage from power stages of phases C and D.
14	$SENS_1$	Input for load current sense voltage from power stages of phases A and B.
15	V_{ref}	Reference voltage for chopper circuit. A voltage applied to this pin determines the peak load current.
16	OSC	An RC network (R to V_{CC}, C to ground) connected to this terminal determines the chopper rate. This terminal is connected to ground on all but one device in synchronized multi - L297 configurations. $f \cong 1/0.69\ RC$, $R > 10\ k\Omega$.
17	CW/$\overline{CCW}$	Clockwise/counter clockwise direction control input. Physical direction of motor rotation also depends on connection of windings. Synchronized internally therefore direction can be changed at any time.
18	$\overline{CLOCK}$	Step Clock. An active low pulse on this input advances the motor one increment. The step occurs on the rising edge of this signal.
19	HALF/$\overline{FULL}$	Half/full Step Select Input. When high selects half step operation ; when low selects full step operation. One-phase-on full step mode is obtained by selecting FULL when the L297's translator is at an even-numbered state. Two-phase-on full step mode is set by selecting FULL when the translator is at an odd numbered position. (the home position is designated state 1).
20	RESET	Reset Input. An active low pulse on this input restores the translator to the home position (state 1, ABCD = 0101).

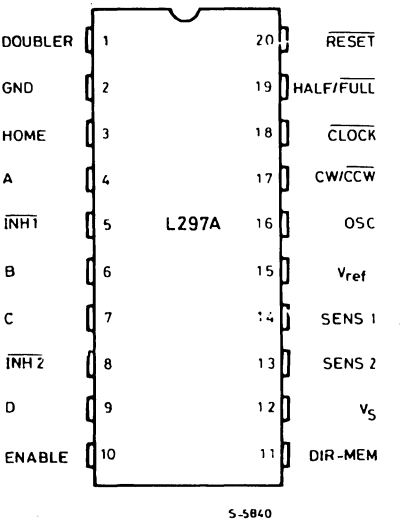
PIN FUNCTIONS – L297A

Pin function of the L297A are identical to those of the L297 except for pins 1 and 11.

N°	Name	Functions
1	DOUBLER	An RC network connected to this pin determines the delay between an input clock pulse and the corresponding ghost pulse.
11	DIR-MEM	Direction Memory. Inverted output of the direction flip-flop. Open collector output.

Figure 24 : Pin connections.





DC AND BRUSHLESS MOTORS

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TWIN-LOOP CONTROL CHIP CUTS COST OF DC MOTOR POSITIONING

by H. Sax, A. Salina

Using a novel control IC that works with a simple photoelectric sensor, DC motors can now compare with stepper motors in positioning applications where cost is critical. The chip contains two complete control circuits, so that two motors can be controlled with one IC.

Since the introduction of integrated power drive stages, stepper motors have been the most popular choice for positioning drives in cost-critical applications like printer carriage control. Though DC motors are cheaper, require less power and provide more holding torque, they were rejected because they needed a costly shaft angle encoder to achieve comparable performance.

Today, however, it is possible to build a cheap, fast and efficient DC motor positioning drive that uses a simple optical encoder. What makes this possible is an integrated circuit — the SGS-THOMSON type L6515 — that embodies a twin-loop control system and uses a novel tacho conversion scheme which works effectively without high precision sensors.

The new IC is designed to work in a system shown schematically in figure 1. Actually the device contains two complete control circuits because most applications involve two motors. For simplicity only one half is shown. The system is controlled by a micro and uses a high-power bridge IC as the output stage to drive the motor. On the motor shaft is an optical encoder that provides two sinusoidal or triangular outputs 90° out of phase.

Two closed-loop operating modes are used: speed control and position control. At the beginning of a positioning action the system operates in speed control mode. The microcontroller applies a speed demand word to the L6515's DAC, normally calling for maximum speed. The motor current rises rapidly, accelerating the motor to the desired speed, which is maintained by a tacho feedback voltage derived from the sensor signals.

A counter in the micro monitors the squared sensor outputs, counting pulses to determine the distance travelled. As the target position is reached the micro reduces the speed demand word step-by-step, thus decelerating the motor. Eventually, when the speed demand word is zero and the final position very close, the micro closes the po-

Figure 1: A highly integrated control circuit using novel circuit techniques makes it possible to design a dc motor positioning system that competes with stepper motors. This device is used with a bridge power stage and optical encoder.

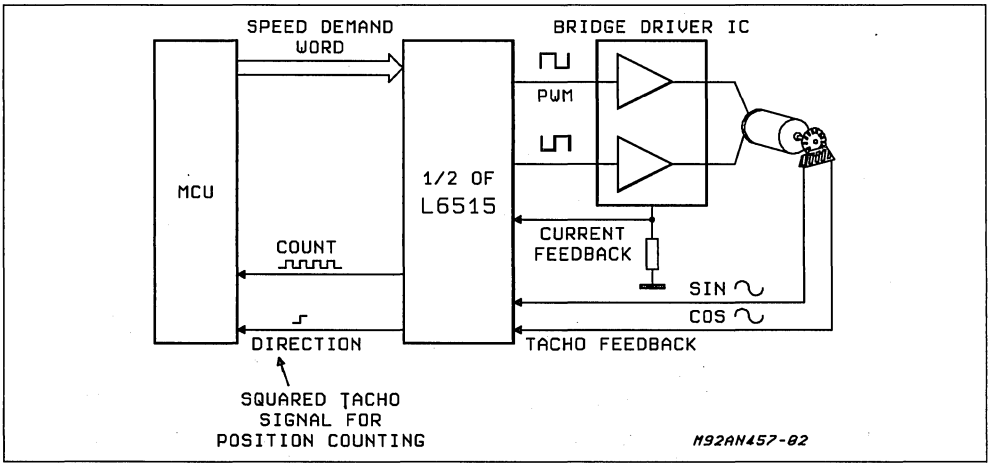
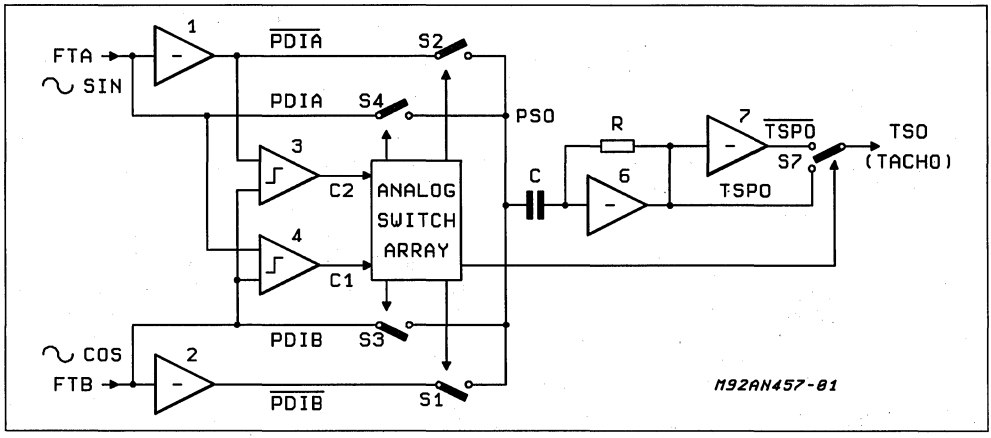


Figure 2: Unlike conventional tacho converters the L6515 uses this circuit which does not depend on a high-precision mechanism because it exploits the crossover points between the sine and cosine signals from the encoder.



sition loop — where one of the sensor outputs is connected directly to the error amplifier — forcing the motor to stop and hold in a position corresponding to a zero crossing of the sensor signal.

This combination of closed loop speed control, pulse counting and closed loop position control gives very fast and precise positioning.

GENERATING THE TACHO SIGNAL

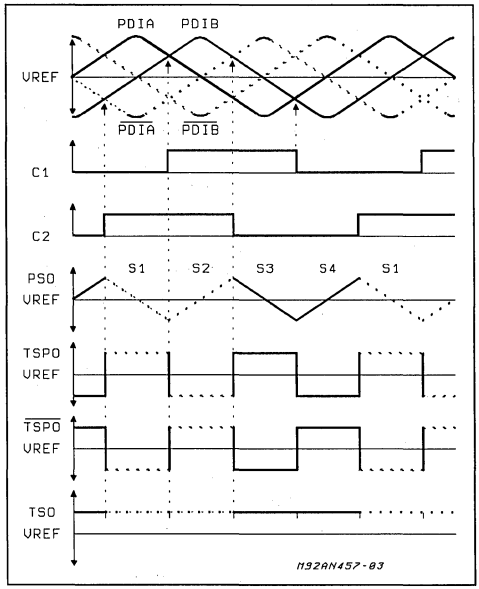
Systems working on this basic principle have been used before, but they used a conventional tacho conversion scheme where the encoder outputs are converted to a voltage proportional to speed by differentiation and synchronous rectification. To make this scheme work the encoder signals must be exactly sinusoidal or the tacho output will not be sufficiently precise. This in turn calls for great mechanical precision in the encoder construction and electronic brightness control for the light source. Such encoders are intrinsically expensive.

One alternative is to design a purely digital system, where the controller simply processes pulses from a simple encoder. However, this would require an encoder with a large number of steps/rotation to keep the loop stable at low speeds and guarantee the necessary precision. Also, at high speeds the pulse rate would overload low cost microcontrollers.

A completely new approach has been chosen for the L6515 which solves this problem. Rather than depend on the magnitude of the signals, this method relies on sensing the $\Delta V/\Delta t$ between crossovers in the encoder signals (figure 2).

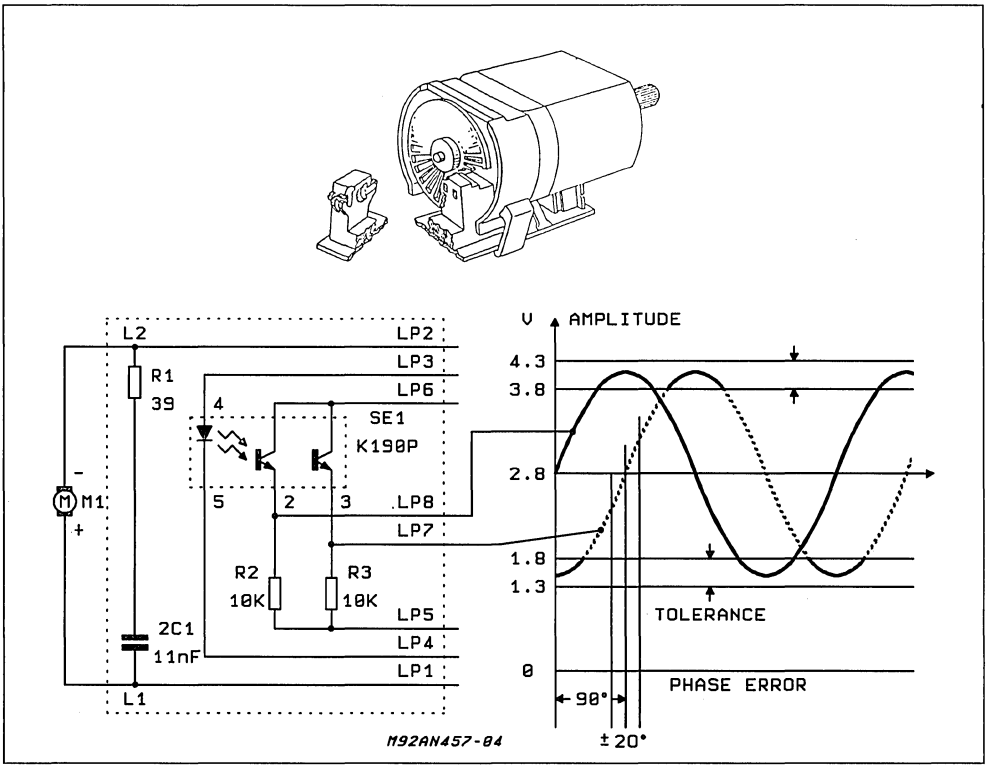
How this works can be seen in the waveforms of figure 3. First the two encoder signals are in-

Figure 3: Waveforms and truth table for the tacho conversion circuit in figure 2.



TRUTH TABLE, S1 - S7			
C1	**C2**	**CLOSED**	**S7 IN POSITION**
L	H	S1	TSPO
H	H	S2	$\overline{\text{TSPO}}$
H	L	S3	TSPO
L	L	S4	$\overline{\text{TSPO}}$

Figure 4: The system operates with a simple, inexpensive optical encoder which has only one adjustment, which ensures that the maxima of the sine and cosine waveforms are within a certain tolerance. All other tolerances are guaranteed by the construction of the encoder.



verted, giving a total of four signals. One of these is selected by the switches S1 to S4 depending on the outputs of the two comparators which cross-compare the sine and cosine signals. The selected encoder signal is then differentiated and the output inverted or not depending on the two comparator outputs.

The beauty of this approach is that it is independent of the encoder waveforms — they can even be triangular. The only requirement for precision is that the maxima of the sine and cosine waveforms must be within a certain tolerance, ensuring sufficient precision in the crossover points. This can be achieved in practice with a simple mechanical adjustment.

Figure 4 shows an encoder used in this system and how it is attached to the motor. For an encoder of this type and a resolution of less than 100 steps/revolution no other adjustments are necessary because the mechanical construction guarantees all of the other tolerances.

CLOSING THE POSITION LOOP

As we have seen above, the tacho loop is augmented by a position loop for the final precise positioning and holding. How the two loops are connected in shown in figure 6.

The eight bits from the microcontroller consist of five bits for the magnitude of the speed demanded, one bit for its sign (and hence the motor direction) and two bits which select which half of the IC is addressed. If a speed demand word of 00000 is loaded one of the two switches S5 or S6 is closed, depending on the direction selected. Thus one of the encoder signals is connected directly to the summing point of the error amplifier input and the motor will be brought to a halt at the zero crossover of the encoder signal. It will remain in this position until a new position operation is initiated.

At the output of the error amplifier is the pulse-width-modulation circuit which drives an external power stage (figure 8).

In basic outline this circuit is very simple: the error

Figure 5: Application Circuit

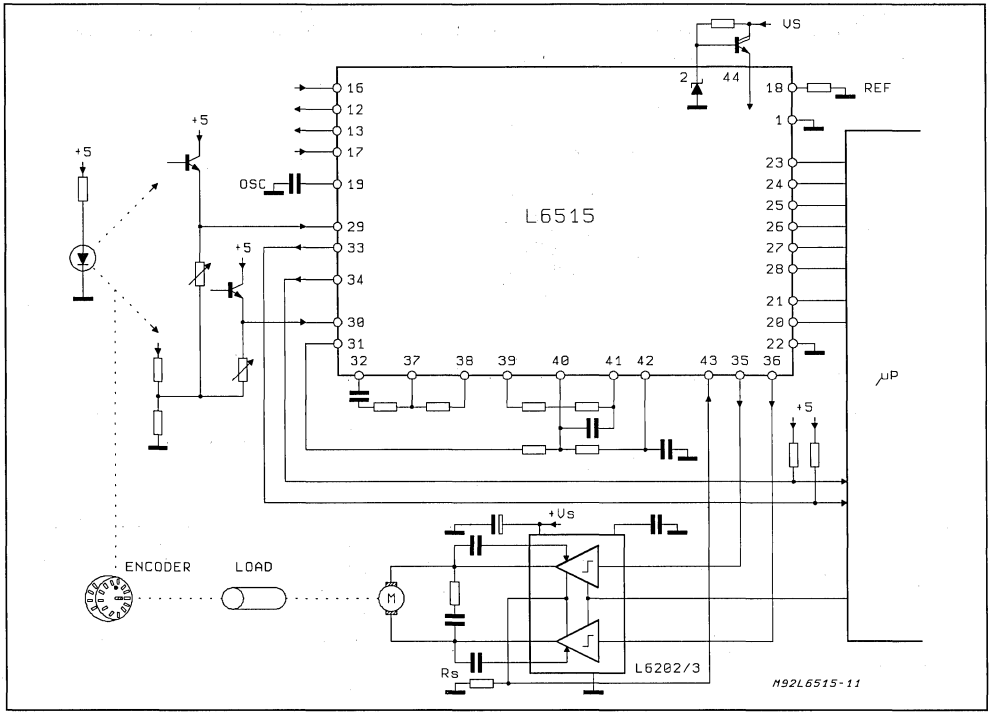


Figure 6: Shown schematically, the complete system has a main, velocity loop where the tacho signal and the output of a DAC are compared in an error amplifier which drives a PWM output stage. For final positioning S5 or S6 is closed, forming a position loop.

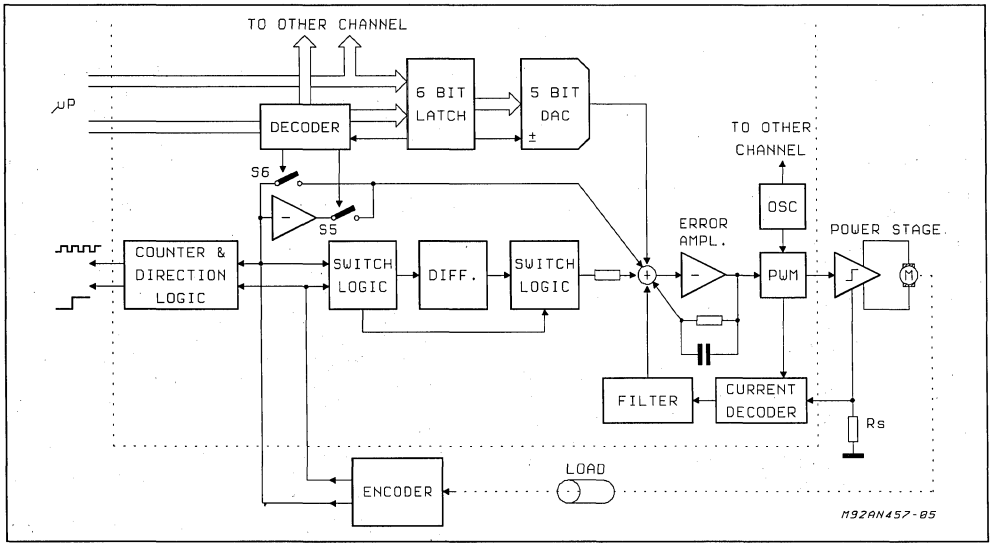


Figure 7: Because there is a single sense resistor connected to the lower legs of the bridge the current feedback voltage does not reflect the polarity of the motor current. Before the feedback signal can be added to the error signal its polarity must be restored.

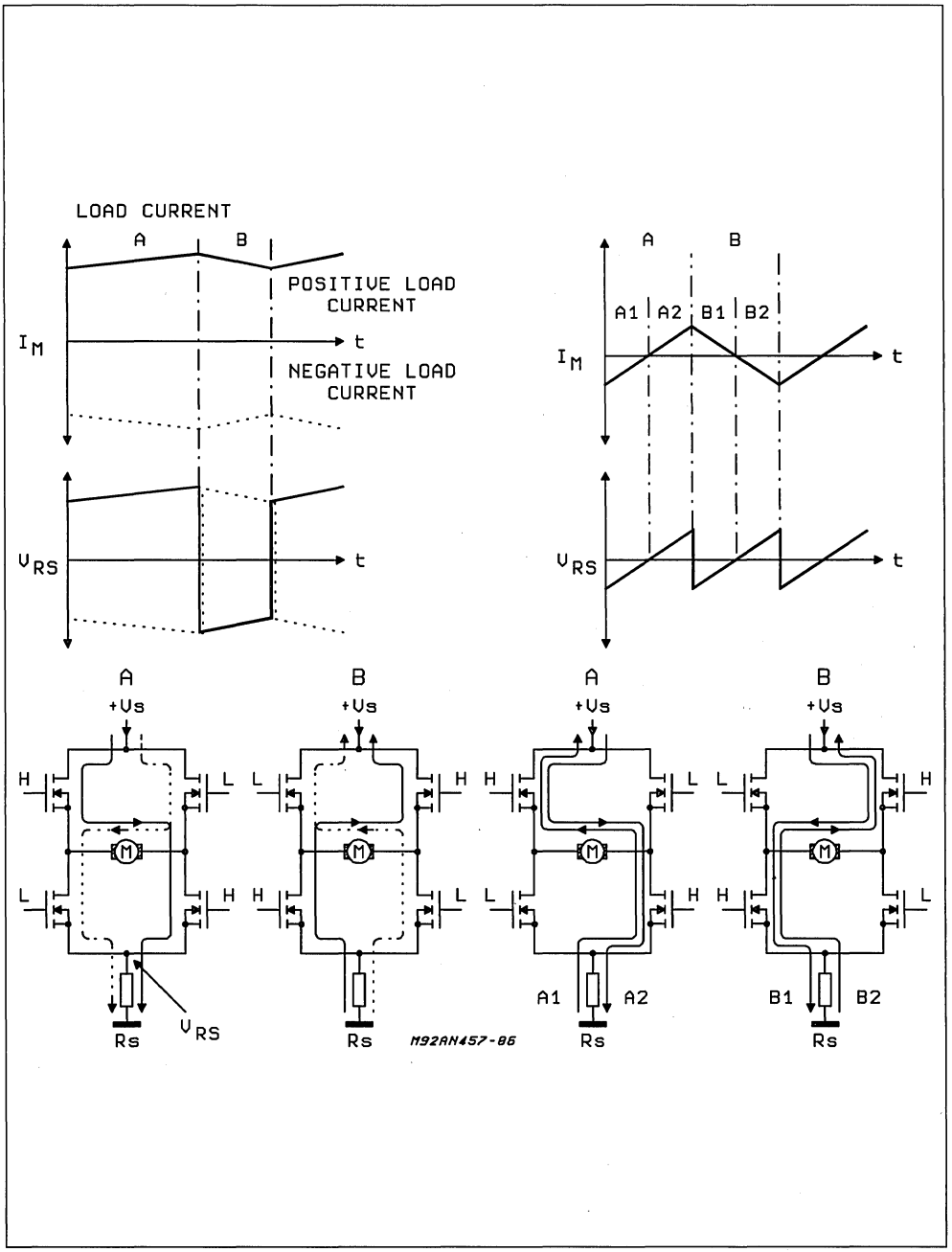
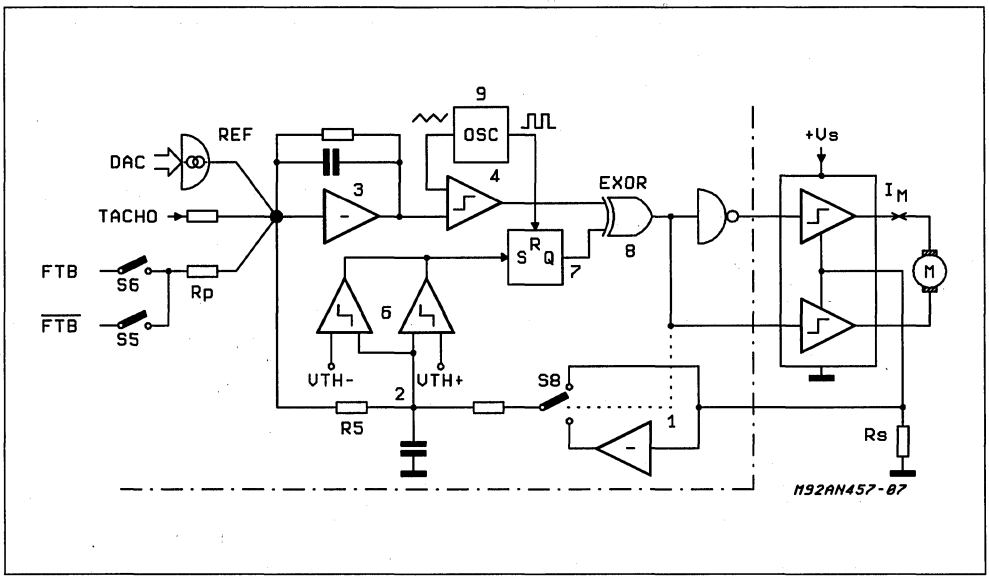


Figure 8: The pulse width modulator is formed by an oscillator (9) and a comparator (4). Switch S8 and (1) restore the correct polarity to the voltage from the current sense resistor.



amplifier output sets the threshold of the comparator 4, thus transforming the triangular wave from the oscillator into a rectangular signal whose duty cycle depends on the error amplifier output amplitude.

Feedback is provided by the sensing resistor Rs, which provides a voltage proportional to I_M.

The whole loop works in current mode which controls the torque of the motor.

Figure 9: The gain of the current loop is set by R5, while the maximum current can be set independently by the sense resistor, Rs.

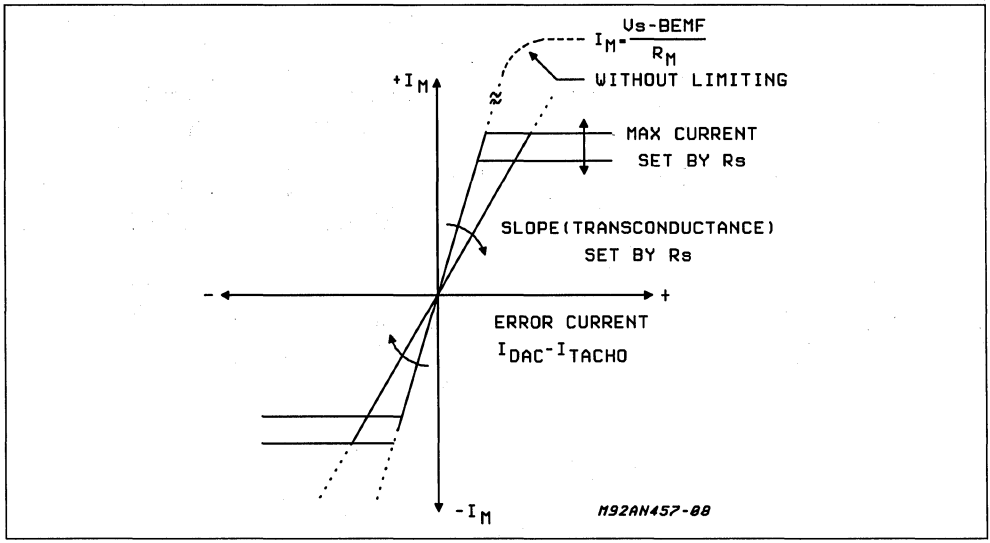
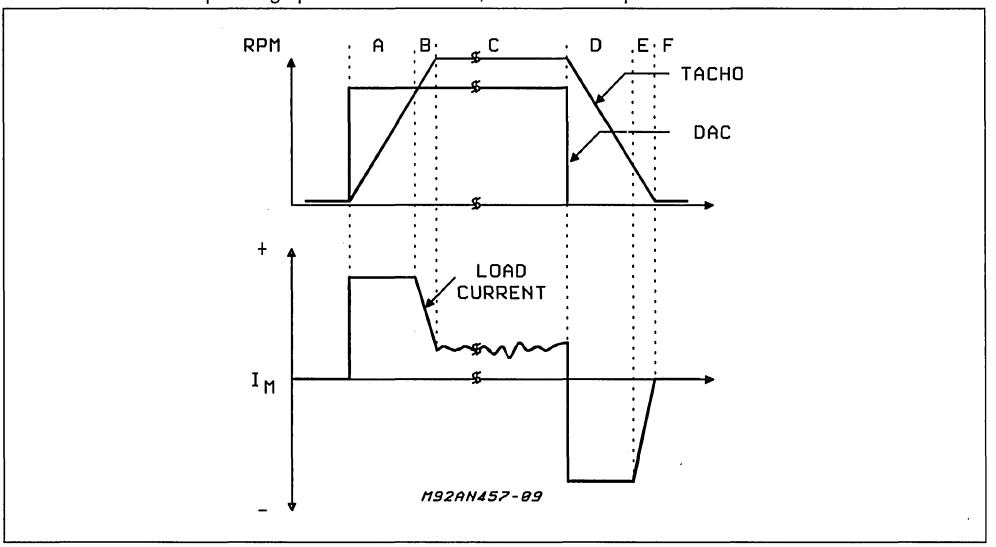


Figure 10: There are six distinct phases in an elementary positioning operation. These waveforms show the corresponding speed demand word, actual motor speed and motor current.



However, in practice it is necessary to reconstruct the polarity of the feedback voltage because the voltage across R_S is always of the same polarity, regardless of the direction of the drive current. This is performed by the inverter in the feedback path which is switched by S8 depending on the direction of the drive signal, which controls the current direction.

When the motor is accelerating rapidly to the set speed the current control loop saturates so the load current could increase to the point where the power stage or motor may be damaged.

To prevent this a limiting circuit formed by stages 6, 7 and 8 has been included. Normally the flip flop is reset periodically by the R_S oscillator and remains in the reset state; consequently the EXOR gate is "transparent", having no effect on the PWM output. When, however, the current exceeds a positive or negative threshold the flip flop will be set, thus the EXOR gate will invert the PWM output thus reversing the bridge drive, causing the current to drop rapidly.

Figure 8 shows the loop characteristics of the system and how they are controlled.

The loop gain is set by the resistor R5, while the maximum current is set independently by the sensing resistor R_S. These components can be set to accommodate a wide variety of motors and conditions.

Now that the circuit functions have been explained it is possible to follow in detail the functioning of the device. A basic positioning operation would consist of six steps (figure 10):

A.Acceleration, where the current is at a maximum limited by stages 6/7/8 (indicated in figure 8)

B.End-of-acceleration, where the current is reduced under control of stages 3/4

C.Constant speed, where tacho feedback controls the current at a low value

D.Deceleration, where the current is limited by stages 6/7/8

E.End-of-deceleration, where the current is controlled by 3/4

F.Positioning, where either S5 or S6 is closed.

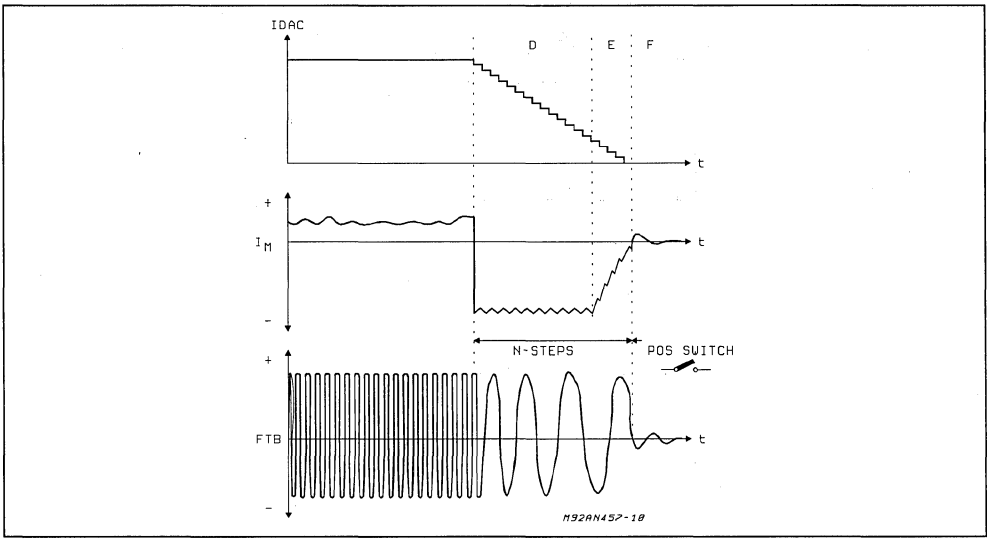
In practice phase D will be replaced by a series of decelerations to bring the motor speed down smoothly to zero at the destination point. Figure 10 shows the corresponding waveforms.

HIGH POWER BRIDGE ICs

The L6515 control IC is designed to be used with monolithic high power bridge driver ICs which are widely used today for DC and stepper motor driving. These devices are very simple to use because they are controlled by logic level inputs and include basic protection circuits to prevent damage in case of a fault in the controller or software.

Suitable types for output currents from 500mA to 4A are listed in Table 1. Note that bridge drivers

Figure 11: In a real positioning operation the deceleration of the motor is controlled smoothly by a progressive reduction of the speed demand word.



using DMOS power stages make it possible to obtain 1.5A output current using a DIP package, which is very compact and convenient for assembly. Also, single power ICs containing two bridges are available, so it is possible to make a positioning system for two motors with just two ICs.

The same BCD technology used to make smart power bridges like the L6202 and L6204 is also employed in the L6515, even though there are no power stages in the device. This technology is, in fact, highly suitable for this IC because it combines high density logic with the precision of bipolar circuits. Moreover, it also allows the inclusion of very low resistance MOS transistors which are needed in the tacho conversion switching circuits.

SOFTWARE

Software to control the L6515 must initialize the system at each reset then manage each positioning operation.The initialization routine is very simple; bringing the two latch control inputs R & S high together resets both of the latches at the DAC inputs. (see Figure 5).

At the same time the position counters in the micro will be zeroed. If the mechanical subsystem is in an unknown position the motor will have to be driven at a moderate speed to a known position during this phase. In a printer, for example, it can be driven towards an endstop.

For each positioning operation the micro will have to determine a suitable profile — in particular when to begin deceleration. Then, once the first speed demand word has been latched into a DAC it will have to count the squared encoder pulses, usually with an interrupt routine. At specific distances from the end point reduced speed demand words will be loaded and then when the final position has been reached a zero speed demand word will be loaded; this automatically activates the position loop.

Table 1: High Power Bridge Driver ICs

HIGH-POWER BRIDGE DRIVER ICs				
TYPE	**FUNCTION**	**TECHNOLOGY**	**DC CURRENT**	**PACKAGE**
L6204	DUAL BRIDGE	DMOS	0.5 A	20 - PIN POWERDIP
L6201	BRIDGE	DMOS	1 A	20 - PIN SO
L6202	BRIDGE	DMOS	1.5 A	20 - PIN POWERDIP
L298N	DUAL BRIDGE	BIPOLAR	2 A	15 - PIN MULTIWATT
L6203	BRIDGE	DMOS	4 A	11 - PIN MULTIWATT

HOW TO DRIVE DC MOTORS WITH SMART POWER ICs

by Herbert Sax

There are many ways to control DC motors. Open-loop current control acts directly on torque and thus protects the electronics, the motor and the load. Open-loop variable voltage control makes sense if the motor and electronics are not overloaded when the motor stalls. Open-loop variable voltage control with a current limiting circuit constitutes the simplest way of varying speed. However, a closed-loop system is needed if precision is called for in selecting speeds.

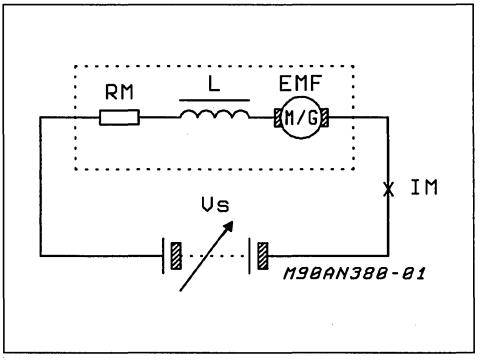
No other motor combines as many positive characteristics as the direct current design: high efficiency, ease of control & driving, compactness without sacrificing performance and much more. And DC motors can be controlled in many ways — open loop current control, variable voltage control or closed-loop speed control — providing great flexibility in operational characteristics.

Before we turn to a detailed discussion of the various methods of control, it is worthwhile recalling a few basics.

DC MOTOR BASICS

Generally speaking, the electric equivalent circuit of a motor (figure 1) consists of three components: EMF, L and R_M.

Figure 1: Electrical equivalent circuit of a DC motor, consisiting of EMF, the winding inductance L and the winding resistance R_M.



The EMF is the motor terminal voltage, though the motor is always a generator, too. It is of no significance whether the unit operates as a motor or a generator as far as the terminal voltage is concerned. The EMF is strictly proportional to the speed and has an internal resistance of zero. Its polarity represents the direction of motion, independent of the motor voltage applied.

The winding inductance, L, is the inevitable result of the mechanical design of the armature. Since it hinders the reversal of current flow in the armature, to the detriment of torque as speed increases, the winding inductance is an interference factor for the motor. It also obstructs rapid access to the generator voltage (EMF).

Motors of coreless, bell armature or pancake design are considerably less susceptible to winding inductance. The smaller mass of these motors improves their dynamic performance to a significant extent. On the positive side, the winding inductance can be used to store current in pulse-width modulation (PWM) drive systems.

The winding resistance, R_M, is purely an interference variable because losses that reduce the degree of efficiency increase as the load torque on the motor shaft increases, the latter being proportional to the current I_M. It is also due to the winding resistance that the speed of the motor drops as load increases while the terminal voltage Vs remains constant.

Some of the mathematical relationships are shown below in simplified form:

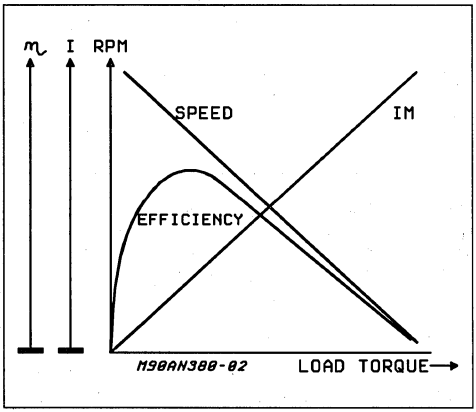
$$EMF = V_S - (I_M . R_M)$$

$$\text{Motor current } I_M = (Vs - EMF)/R_M$$

$$\text{Efficiency} = \frac{EMF \cdot I_M}{V_S \cdot I_M} = \frac{P_{OUT}}{P_{IN}}$$

The drive torque at the motor shaft is proportional to the motor current I_M. Figure 2 shows the relationships graphed in a form commonly used for DC motors. It is because of bearing and brush friction that the efficiency tends towards zero at low load torques.

Figure 2: Relationship between speed, efficiency and motor current of a DC motor.



These basics show that essentially there are only two parameters governing how an electrical change can be made to act on the motor shaft:

a) with the current to vary the torque

b)with the mapping of the EMF on the speed

On account of the winding resistance R_M, open loop variable voltage control exercises no more than an indirect effect on torque and speed and can therefore be used only for simple functions (speed variation).

A number of sample applications using smart power ICs and illustrating open-loop variable voltage or current control and closed loop speed control are discussed here. All of these circuits permit the motor to run in both directions. The modifications needed for unidirectional operation are slight and generally involve a simplification of the design.

OPEN-LOOP VARIABLE VOLTAGE CONTROL

In technical terms variable voltage control is the simplest to implement. Its main scope of application is in simple transport or drive functions where exact speed control is not essential. Applications of this kind are found, for example, in the automobile industry for driving pumps, fans, wipers and power window lifts.

The circuit shown in figure 3 is an example of a variable speed motor with digital direction control. The motor voltage can be controlled via an analog input. If the polarity of the control signal is the variable that determines the motor's direction of rotation — as is usually the case in servo systems, for example — the design shown in figure 4 can be used.

One of the operational amplifiers is responsible for the V_M/V_{IN} voltage and the other has an gain of 1, so that the voltage losses Vs - V_M are divided evenly between the two parts of the bridge.

Equivalents to the circuits in figures 3 and 4 are shown in figure 5 and figure 6; these latter circuits, however, are switchmode and their efficiency is thus improved to a considerable extent.

Figure 3: Circuit for driving a variable-speed motor. Where the enable function is needed, the type L6242 can be used.

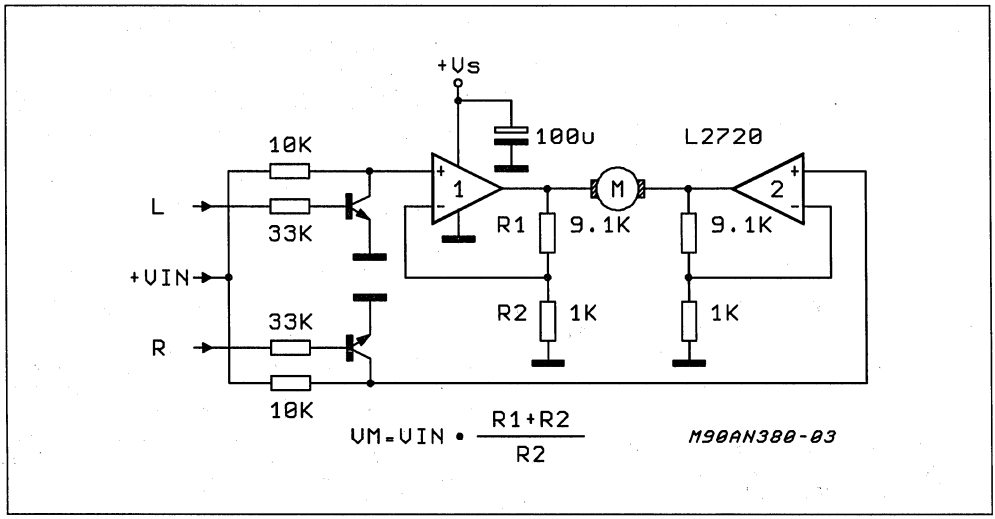


Figure 4: A typical circuit for driving servo system.

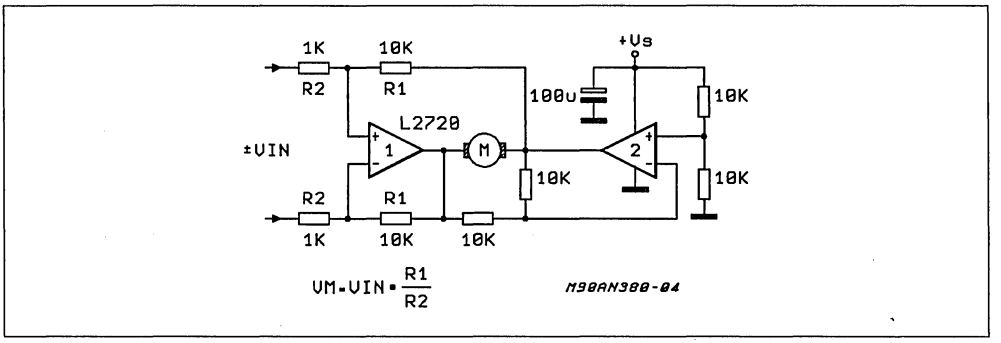


Figure 5: Equivalent circuit to that in Figure 3, but using PWM.

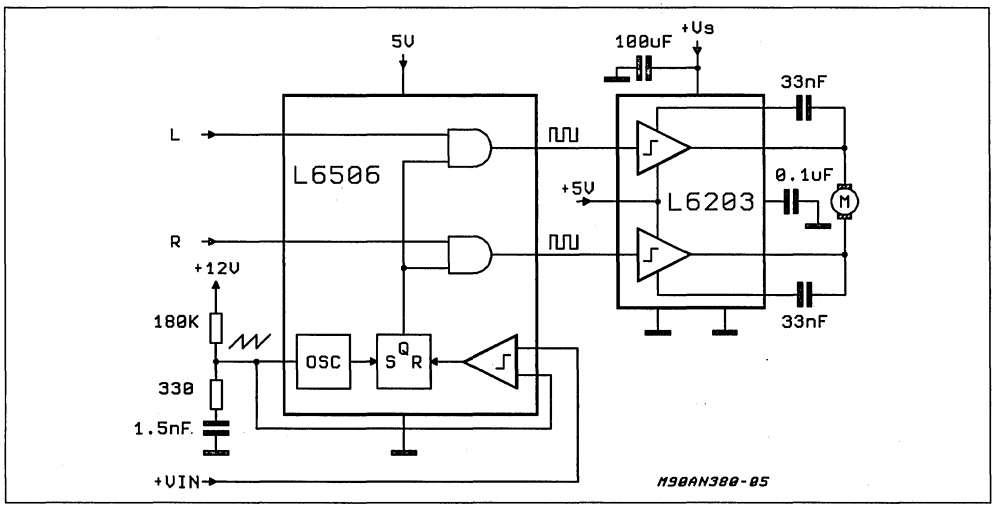
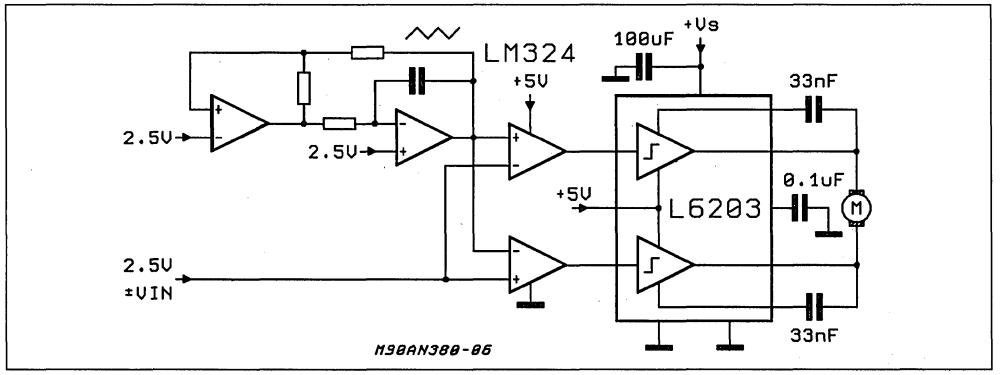


Figure 6: Equivalent circuit to that in Figure 4, but using PWM.



OPEN-LOOP CURRENT CONTROL

Open-loop control is called for whenever a motor has to supply a constant or variable torque. Applications include the head motors in tape recorders or the motors used to tension threads when textile fibers are wound onto spools. The speed of the motor at any given time is of no significance. In applications of this nature the motor shaft will often rotate in the direction opposite to that determined by the current.

Two conditions are particularly important in a current controlled application. The circuit will not operate unless $V_{Mmax} \geq EMF + (I_M R_M)$, if the motor shaft is running in the same direction as the drive. The equation applicable to a counter rotating motor shaft is:

$$-V_{Mmax} - EMF \leq I_M R_M$$

Open-loop current control is often used in conjunction with open-loop variable voltage control or closed loop speed control. Such an arrangement would be designed to:

- limit torque to protect the load and the motor
- protect the power ICs against overload
- obtain acceleration and deceleration characteristics independent of speed.

Figure 7 shows the simplest form of open-loop current control with a positive & negative supply. Transferring the circuit to a bridge eliminates the ground at one end of the shunt R_S and a way of differentially sampling the sense resistor voltage must be found. One solution is shown in figure 8. As in figure 4, the second half of the bridge operates as a voltage inverter.

Figure 7: Current control circuit with bipolar voltage supply in its simplest form.

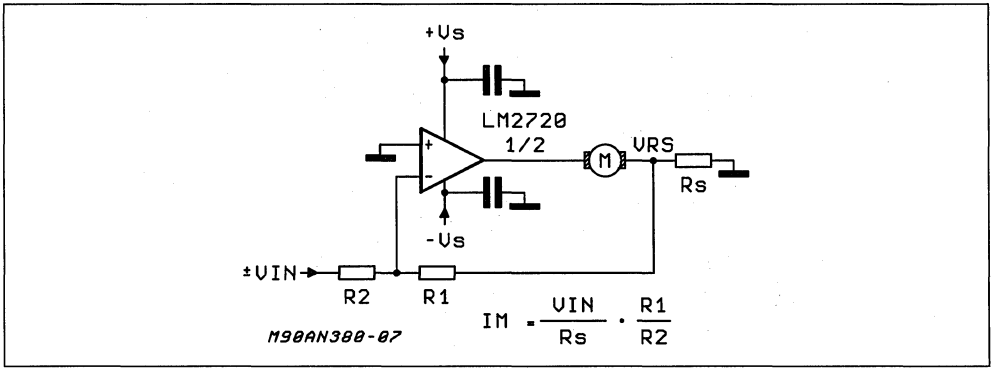
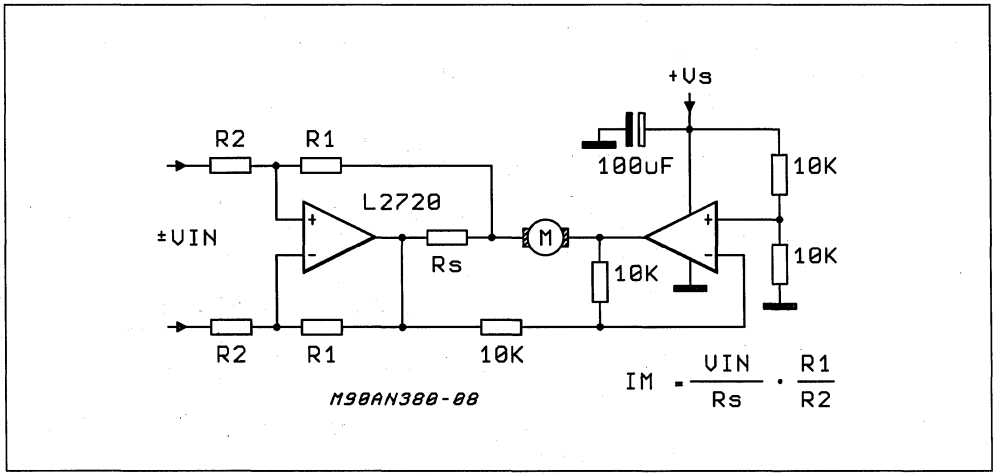


Figure 8: This circuit permits differentiated sampling of the voltage at the sense resistor.



When the principle behind the circuit shown in figure 8 is transferred to a switchmode circuit (figure 9), a considerable degree of complexity is called for to reduce power loss. For this reason the circuit is shown in slightly simplified form.

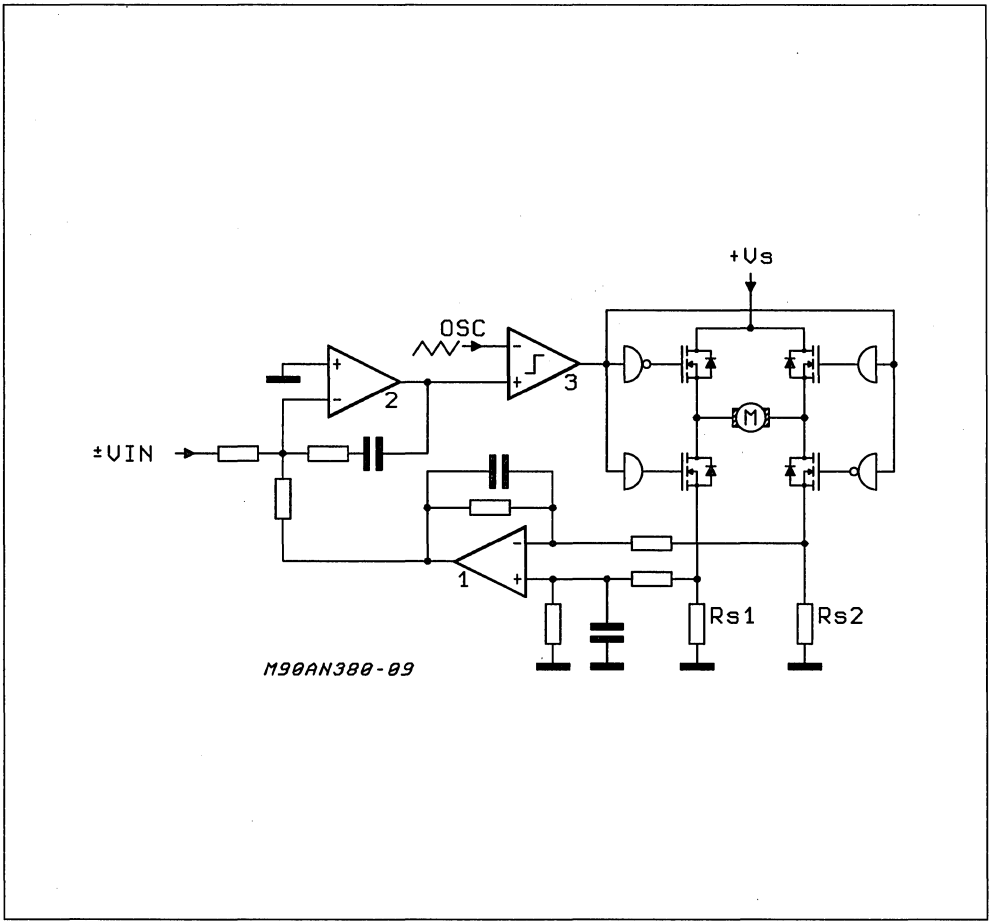
Operational amplifier 1 reconstructs the current proportional voltage V_{RS} to ground as shown in figure 7. Two sense resistors are needed, as otherwise it would not be possible to detect the direction of the current in the bridge.

Operating as a PI controller and converting the error signal in a PWM via comparator 3, OP2 compares the reference and feedback values. One major advantage of a circuit such as that shown in figure 9 is its high transfer linearity maintained even in the vicinity of the zero current crossing. Open-loop current control also functions with a generator, the motor returning its own kinetic energy and that of the load to the supply voltage in a controlled manner. Braking is a case in point, and for this reason circuits of this design are usually found in servo positioning drives that demand precise current control over a wide operating range.

CLOSED-LOOP SPEED CONTROL

Many circuits, often of completely different design, have been developed for closed-loop speed control. The most suitable system has to be chosen on the basis of the requirements that a drive concept has to meet. These requirements also determine how the speed will be sensed and processed.

Figure 9: Operating principle of the circuit of figure 8 transferred to a PWM arrangement.



The table provides an overview of the most common principles of sensing and processing and their influence on control characteristics and system costs.

CHARACTERISTICS		PRINCIPLE OF SPEED SENSING					SIGNAL PROCESSING			AC REFERENCE	
		DC Tacho	V-I Control	EMF Sense	AC Tacho	Commutation Sense	P Control	PI Control	PID Control	PLL Control	Digital Sensor
CONTROL ACCURACY	HIGH				•	•				•	•
	MEDIUM	•		•				•	•		
	LOW		•				•				
EXTENDED CONTROL RANGE POSSIBLE		•		•			•				
CONTROL REACTION	FAST	•	•	•			•		•		•
	SLOW				•	•		•			
GOOD CONTROL CHARACTERISTICS AT LOW SPEEDS		•		•			•		•		
SUITABLE FOR SERVO DRIVES		•					•	•	•		•
SYSTEM COST	HIGH	•								•	•
	MEDIUM			•	•				•		
	LOW		•			•	•	•			

CLOSED-LOOP CONTROL PROCESSES

DC Tachogenerator

Since a control circuit with a DC tacho-generator yields a direct voltage that is proportional to speed, the circuit itself is less complex than all other designs. Nonetheless, high precision — a constant voltage with low ripple — signifies high cost. On the other hand, the actual electronic control circuit is simplicity itself, as figure 10 shows. The bridge extension for a simple supply voltage is identical to that shown in figure 8.

A closed loop current control system providing braking and acceleration independent of the supply voltage and the internal motor resistance is easy to superimpose on the circuit (figure 11).

Similarly little difficulty is involved in modifying the circuit in figure 10 to yield a switched bridge, because the process entails no more than converting the control error signal into a PWM output (figure 12).

Figure 10: Control with DC tachogenerator: a direct speed proportional DC voltage is generated.

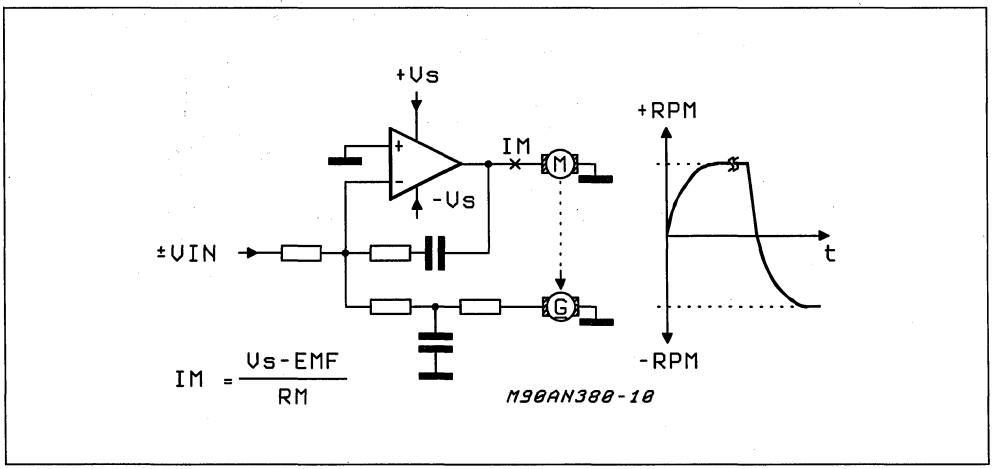


Figure 11: In this circuit, acceleration and braking behavior is independent of the supply voltage and the motor's internal resistance.

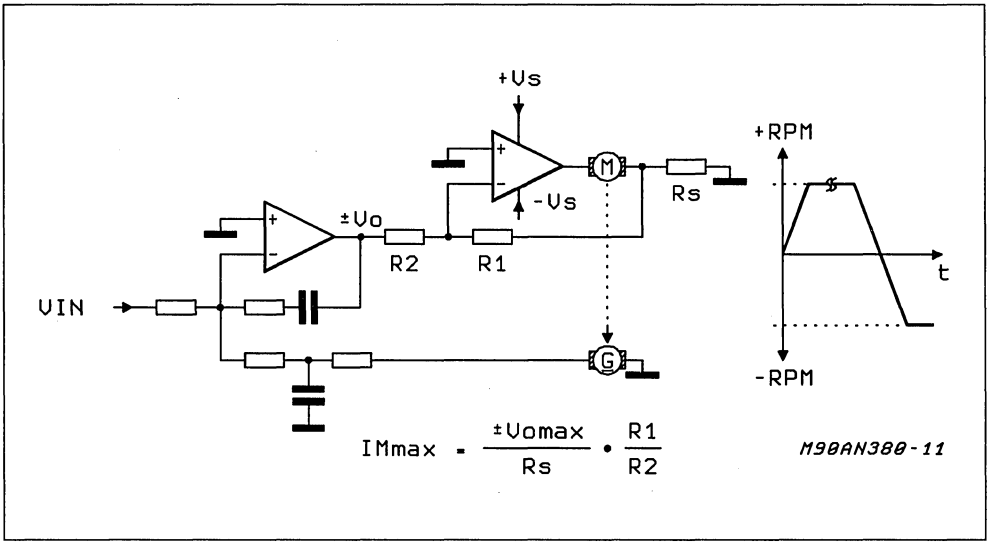
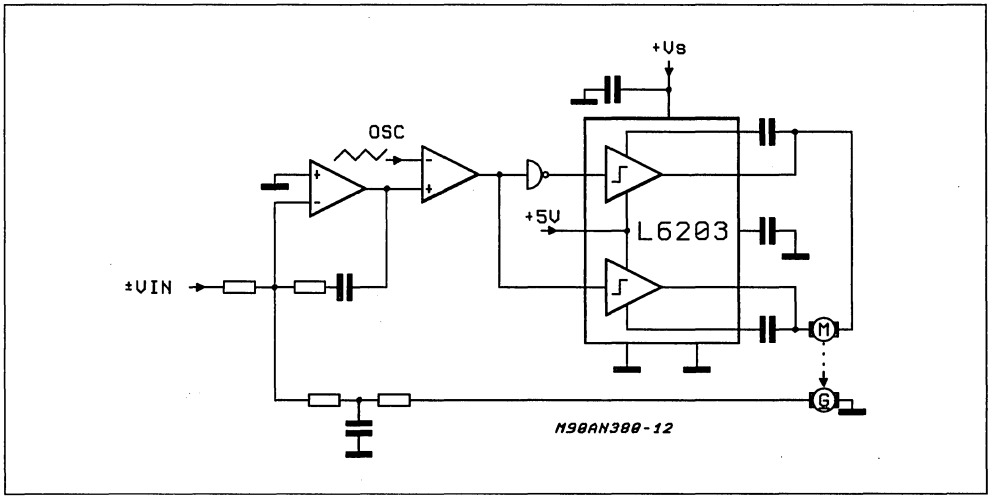


Figure 12: PWM conversion of the control error signal.



V-I Control (Internal Resistance Compensation)

V-I control is based in the principle that the voltage drop at the motor internal resistance I_M, that increases with load torque can be compensated by increasing the motor voltage V_M (figure 13). However, compensation is less than complete because the winding resistance R_M is heavily dependent on the temperature, and brush resistance modulation makes itself felt as an additional interference variable.

In practice this means that the voltage drop is slightly under compensated and positive feedback is reduced even further as frequencies get higher. The control action result improves with the ratio of EMF to $I_M.R_M$. A sample circuit in which the effect of the positive feedback loop can clearly be seen is shown in figure 14.

The desired speed is set with the aid of R1 and R2. The relationship is expressed as:

$$EMF = V_{IN} . R1/R2$$

The value selected for R_S is one tenth of R_M and V_{RS} is amplified by a factor of 10 in OP2 (R5 = R4/10).

The output voltage of OP2 is then identical with the voltage drop at R_M. When R1 = R3, the internal resistance is compensated by 90%. Residual control instabilities can be cancelled out by C1.

The circuit can also be extended to a bridge, although this entails relocating resistor R_S (figure 15). It is surprising that the V-I controller circuitry is again simplified to a considerable extent if amplification is not needed. The V-I control concept can be adapted for a PWM motor control system; the functional layout is rather complex, however, as figure 16 shows. Even so, it is worthwhile in many instances because DC tacho-generators are expensive.

Figure 13: The principle of V-I control.

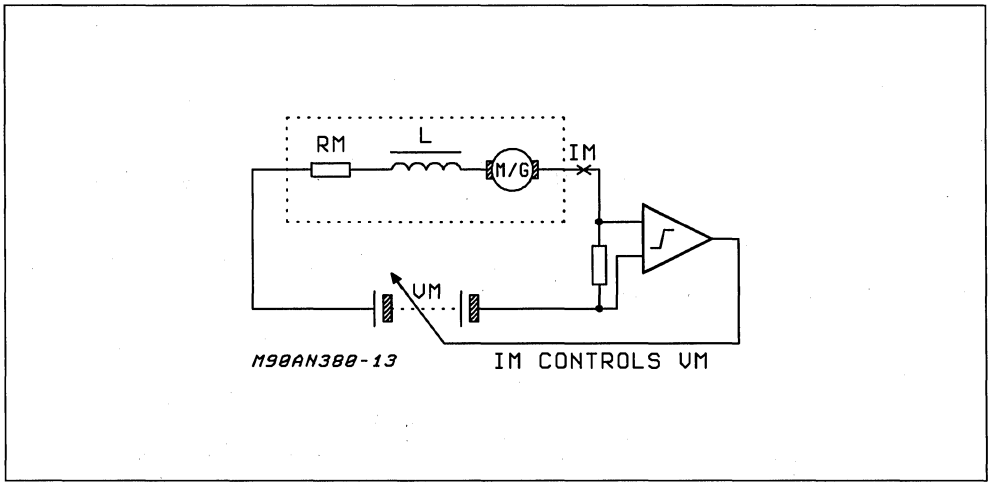


Figure 14: Example circuit in which the positive feedback loop can clearly be seen.

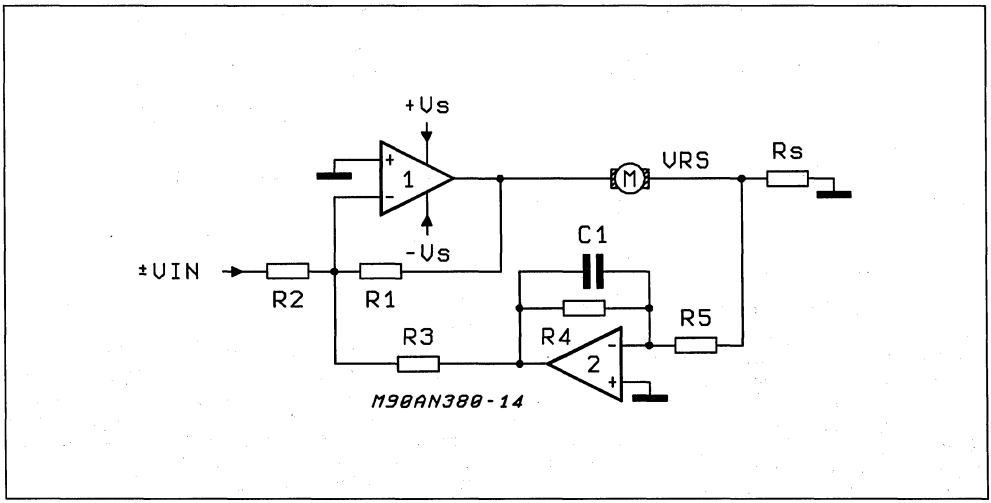


Figure 15: Circuit as in figure 14, expanded to include a bridge.

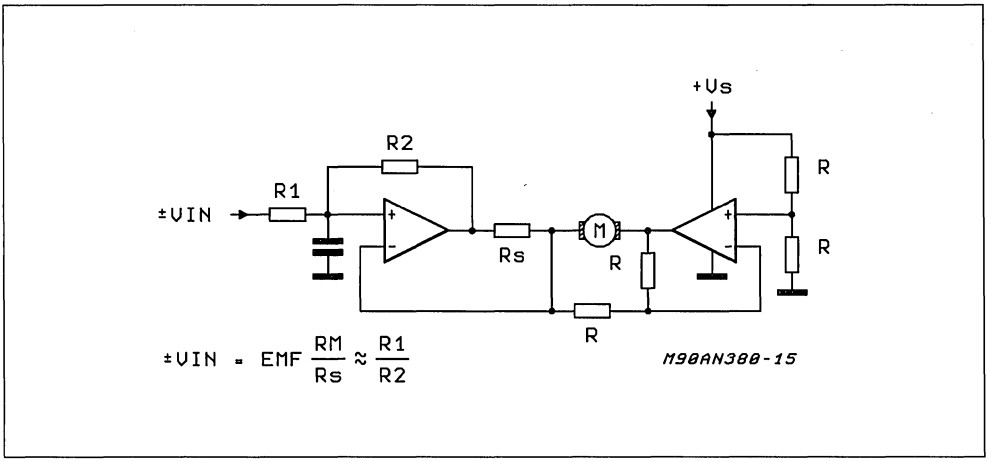
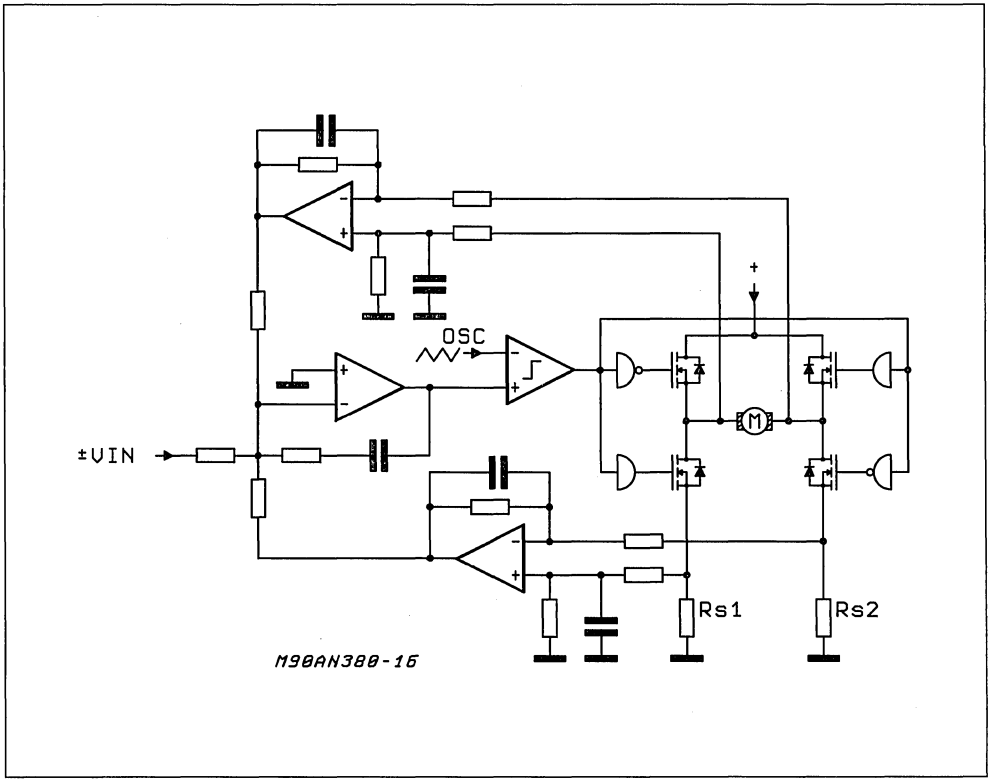


Figure 16: The principle of V-I control transferred to a PWM motor circuit: complexity is increased significantly.



EMF Sensing

The EMF can also be sensed directly, rather than be simulated as in the V-I control setup, when the current I_M is zero (EMF = V_M-I_M.R_M). To achieve this the motor current must be switched off as quickly as possible. Motor inductance represents an obstacle since the energy it stores must first be dissipated before an EMF measurement can be made at the motor terminals. This is the reason why only coreless motors of bell armature or pancake design are suitable. Figure 17 is a block diagram showing how the EMF can be sensed.

In the major partial time t1 the motor carries current. This is followed by a time window t2 in which the motor is de-energized and the motor inductance discharges. There then follows a short sampling phase t3 in which the EMF is sensed and stored in a capacitor until the next sampling phase. The number of cycling cycles per second depends on the dynamic behavior of the load torque. The interval between any two EMF measurements should be of a duration such that the kinetic energy of the drive system bridges a load change without a significant speed drop. Figure 18 illustrates a layout using a current-controlled output stage that has a high impedance output when the input is open.

The circuit for sensing EMF is particularly well suited to switchmode motor control schemes. The monolithic switching output stages available today already have an enable input for releasing the motor, but the concept will usually accommodate this option even if discrete output stages are used. An example circuit is shown in simplified form in figure 19.

Figure 17: Principle by which the EMF can be sensed.

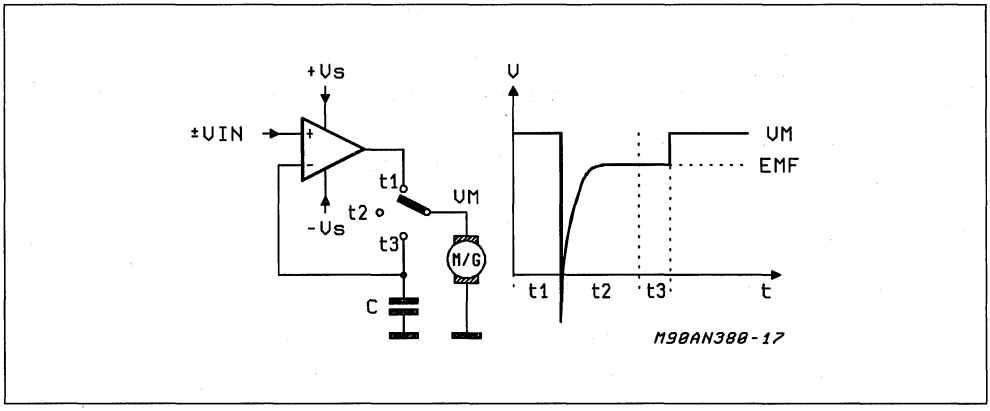


Figure 18: Driver circuit with current controlled output stage with high impedance output when input is open.

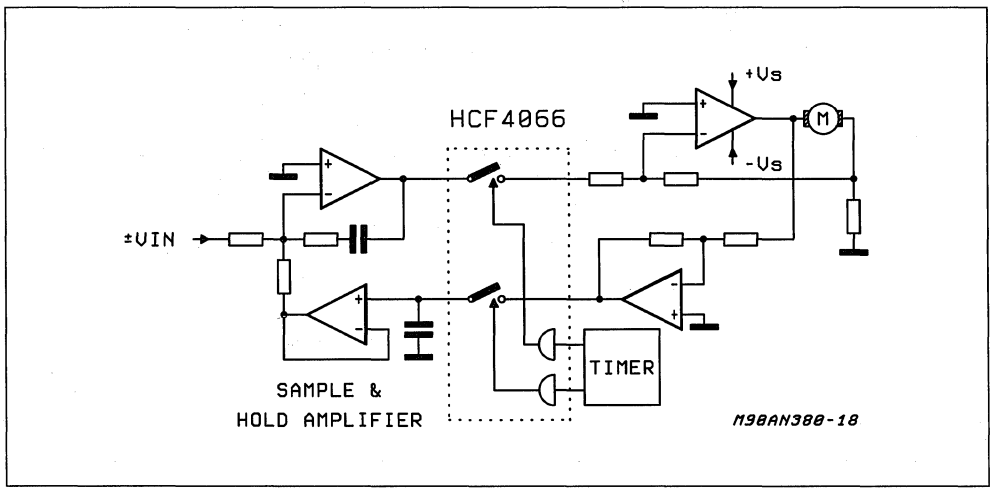
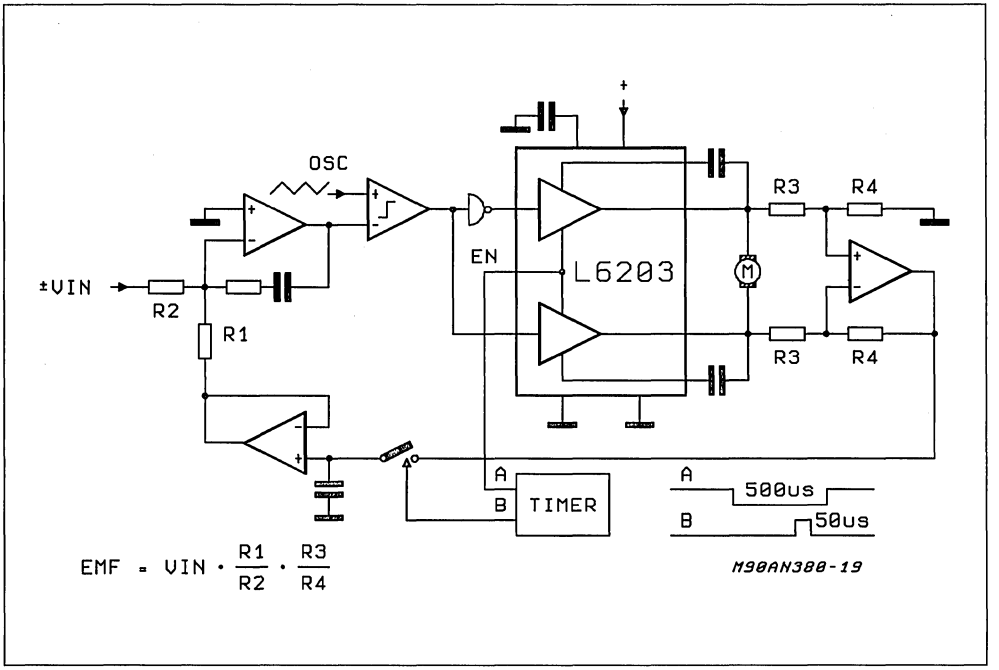


Figure 19: Circuit as in figure 18, but with PWM output stage.



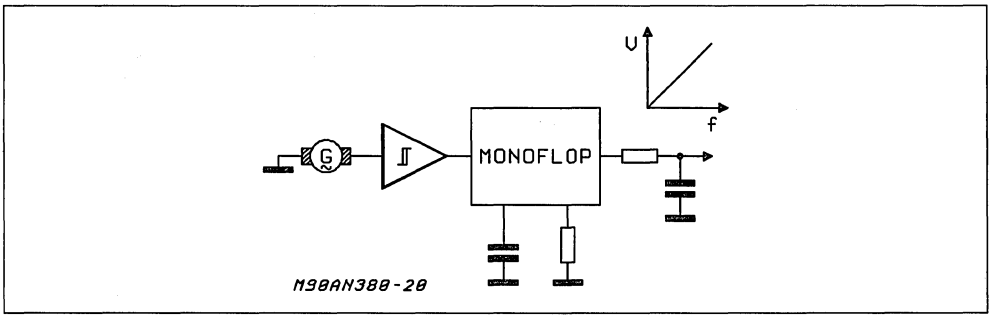
AC Tachogenerator

Economic and with a signal that is easy to process, the AC tachogenerator is the most frequently used means of sensing the speed of a DC motor. Problems arise, however, when the tachogenerator frequency is low, due either to a low speed or a lack of poles on the generator. However, multiple pole tachogenerators are expensive regardless of whether they are magnetic or optical. Most circuits convert the speed proportional tacho frequency back into a DC signal in an f/V converter (Fig. 20).

However, some circuits make use of the proportional relationship between speed and AC voltage amplitude when the tachogenerator is inductive (figure 21). Accuracy is wanting to a certain extent in this arrangement.

Since the output signal of an AC tachogenerator contains no information concerning the direction of rotation, the control loop functions in only one quadrant. For the same reason it is common practice to control the reference in a single quadrant. A separate digital signal determines the direction of rotation. Figure 22 shows a typical

Figure 20: The tachogenerator frequency can be converted back into a DC signal in an f/V converter.



PWM circuit.

Comparator 1 converts the sinusoidal tachogenerator signal into a squarewave voltage that triggers the monostable. The ON time is constant, which means that the DC average increases proportionally as the tachogenerator frequency increases. The error amplifier OP1 also functions as an integrator (C1) and compares the DC reference with the DC average of the monostable output. A DC signal superimposed by a triangular wave AC voltage component can be detected at the output of OP1.

An analog power operational amplifier can also be used instead of the switchmode output stage. In an arrangement like this, the output of the error amplifier OP1 drives the V_{IN} input of the output stage as shown in figure 3.

Figure 21: Alternatively, the proportionality between speed and AC amplitude can be used if the tachnogenerator is inductive.

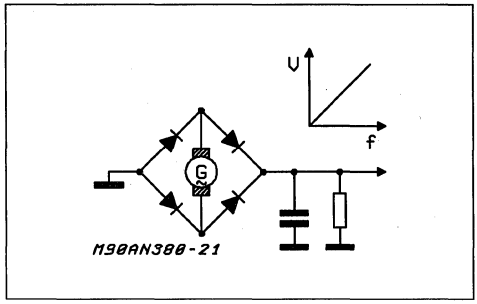
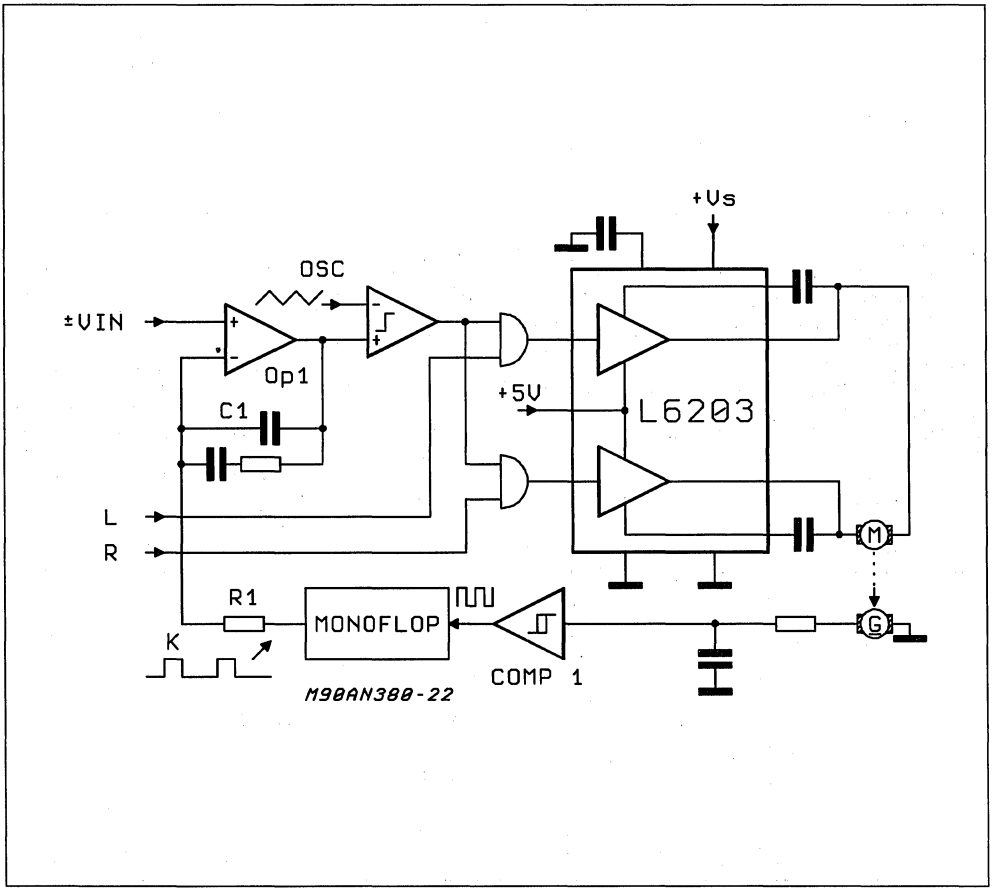


Figure 22: In this PWM circuit the comparator 1 converts the sinusoidal tachogenerator signal into a squarewave.



COMMUTATION Sensing

Commutation sensing is a process that exploits the inherent ripple of the EMF of the motor current as an AC tachogenerator. However, only motors with few poles yield an adequate signal-to-noise margin. Three-pole motors with an AC component equal to approx 30% of the DC value are most suitable (figure 23).

The rapid current reversal is differentiated and used as an equivalent tachogenerator signal (figure 24). The rest of the circuit follows the pattern shown in figure 22, although only one output stage of the type shown in figure 3 is used. A switchmode output stage would interfere with the ripple sensing so is not recommended. One drawback of commutation sensing is the exceptionally low tachometer frequency. A three pole motor, for example, produces a frequency of 200Hz at a speed of 2000 rpm.

Since the AC component of the OP1 error amplifier output signal (figure 22) should not be more than 10% of the DC component at rated speed and nominal load torque, the integrator time constant C1R1 is very large. Control response is sluggish and no longer suitable for rapid load changes.

Assistance can be obtained by superimposing V-I control which has high-speed response to relieve the tachogenerator control loop and accelerate transient response by a considerable margin. Figure 25 shows a sample circuit for a bridge.

Superimposed V-I control can also be used with a real AC tachogenerator to improve the transient load response.

Figure 23: Principle of commutation sensing.

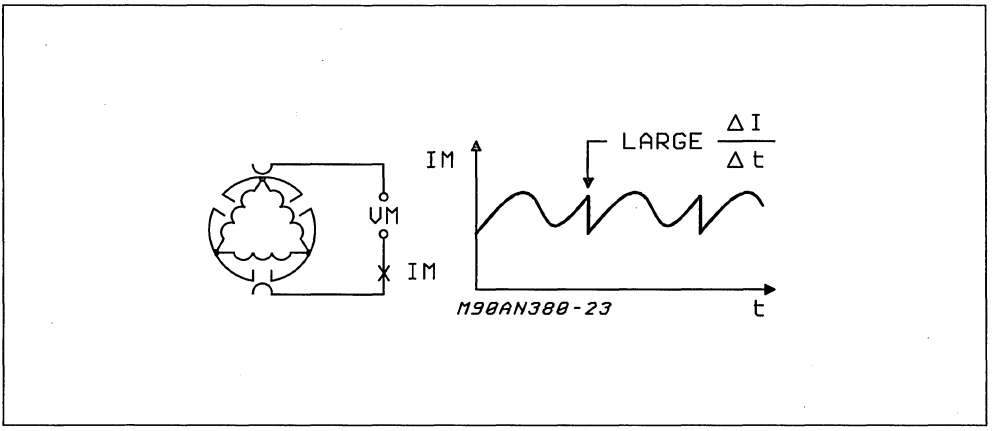


Figure 24: The fastest current reversal is commutated and used as a substitute tachogenerator signal.

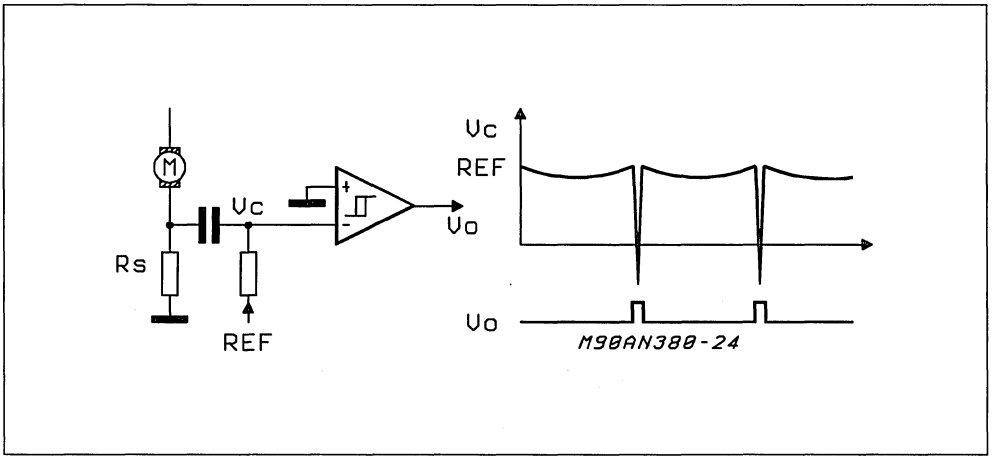
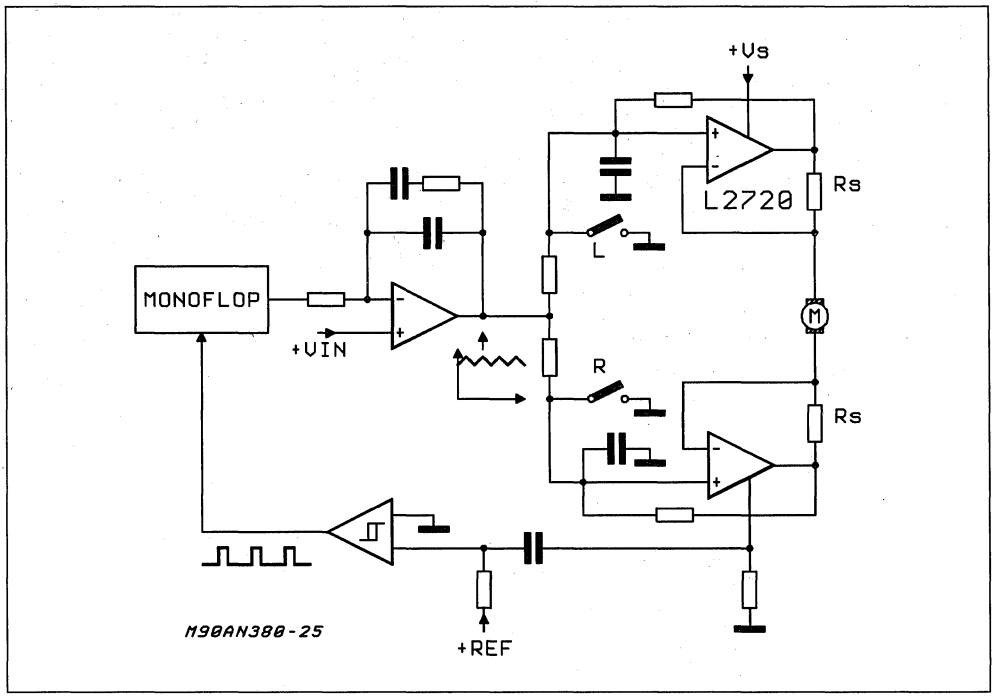


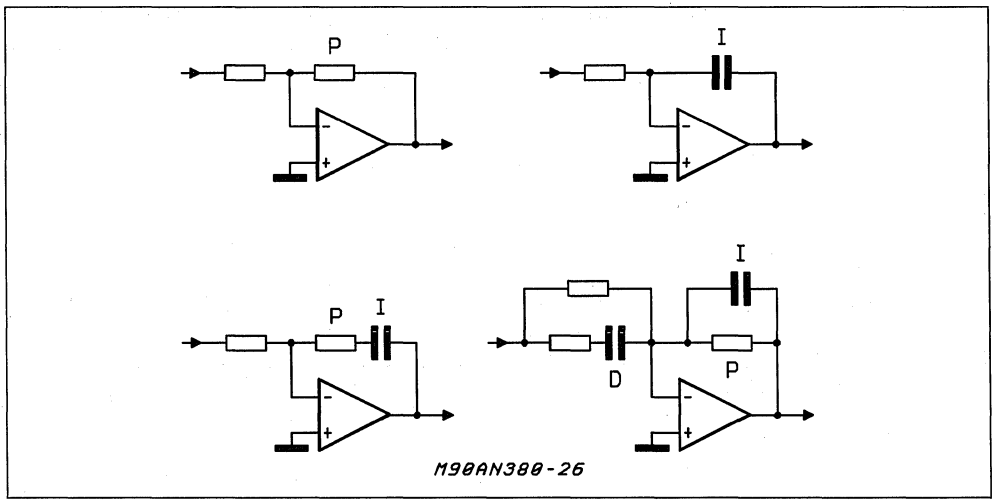
Figure 25: Example circuit for a bridge.



Processing the Tachogenerator Signal

The control principle (figure 26) applied in processing the speed feedback and reference signals in a controlled system depends on a number of factors (table page 6).

Figure 26: P, I, PI and PID controllers.

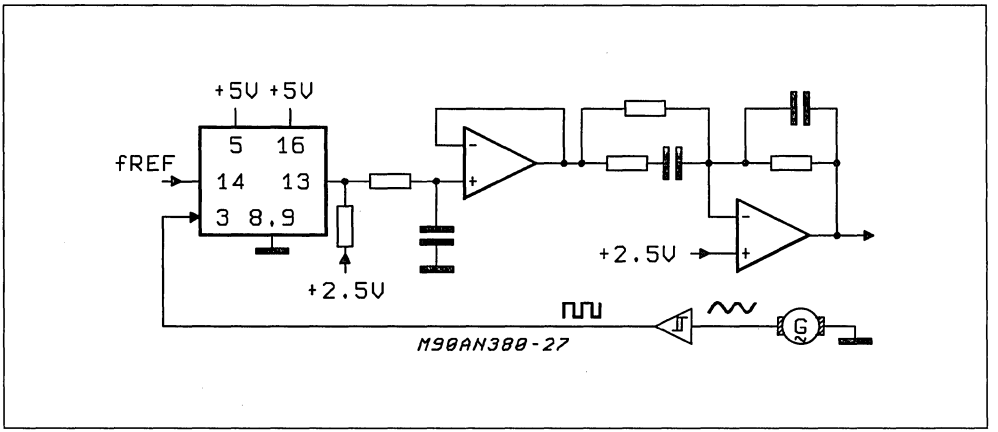


The criteria governing the selection of a P controller, an I controller, a PI controller or a PID controller are as follows: stability of the control loop, reaction time, transient response, load behavior, speed range and control factor. For example, if the reference signal is a frequency it would make sense to use an AC tachogenerator as the feedback value sensor and process both signals on a purely digital level. Powerful microcontrollers or digital signal processors are used.

In special cases that demand a control error of zero — for example, when two drive shafts have to be phase synchronized as well as running at the same speed — PLL control is the only option. A system of this nature compares reference and feedback value for phase as well as frequency. In turn, of course, the AC tachogenerator must meet extreme requirements regarding phase stability since any jitter would be interpreted as a control error, producing a spurious response in the system.

PLL speed control systems are used in video recorders, floppy and hard disk drives and in a number of industrial drive systems. Figure 27 shows a typical PLL speed control circuit. The frequency comparator is phase comparator 2 of the HCF4046 CMOS PLL circuit.

Figure 27: Typical PLL circuit for controlling speed.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

LOAD CURRENT SENSING IN SWITCHMODE BRIDGE MOTOR DRIVING CIRCUITS

by Herbert Sax

Switchmode drive circuits with pulse-width modulation control of the current are widely used in motor driving because they give the best performance.
In such circuits it is important to sense the load current precisely. This note provides practical solutions to this problem.

When it comes to controlling or driving electromagnetic actuators precise sensing of the load current is one of the key functions of any system. A switchmode bridge, however, does not lend itself to direct measurement of the load current in series with the actuator because the high common-mode levels that result from pulse-width modulation are far from conducive to low-cost measuring circuits.Even so, however, these problems can be overcome without resorting to costly isolating amplifiers. Most of the functions needed can be integrated in smart power circuits; some have already been implemented.

CURRENT CONTROL OF A DC MOTOR

In the final analysis, the voltage reference determines the complexity of a circuit for sensing the load current of a DC motor bridge. The simplest arrangement calls for a measuring shunt at the common source pin of the lower branch of a power MOSFET bridge (Fig.1A).

On virtually all the smart power bridges in widespread use this pin is accessible and is adequate for straightforward current limitation functions.

During the load inductor's charge phase, the current that also drives the motor has no alternative but to flow diagonally to the shunt through the two transistors T1 and T2 and can therefore be sensed. Once the load current reaches its nominal value, it should be stored by the most efficient possible means.

The best way of achieving this aim is to short circuit the terminals, in other words to turn on transistors T2 and T3.

Figure 1A: Switch Mode Current Control Circuit for Load Current Limitation.(DMOS Bridge Configuration)

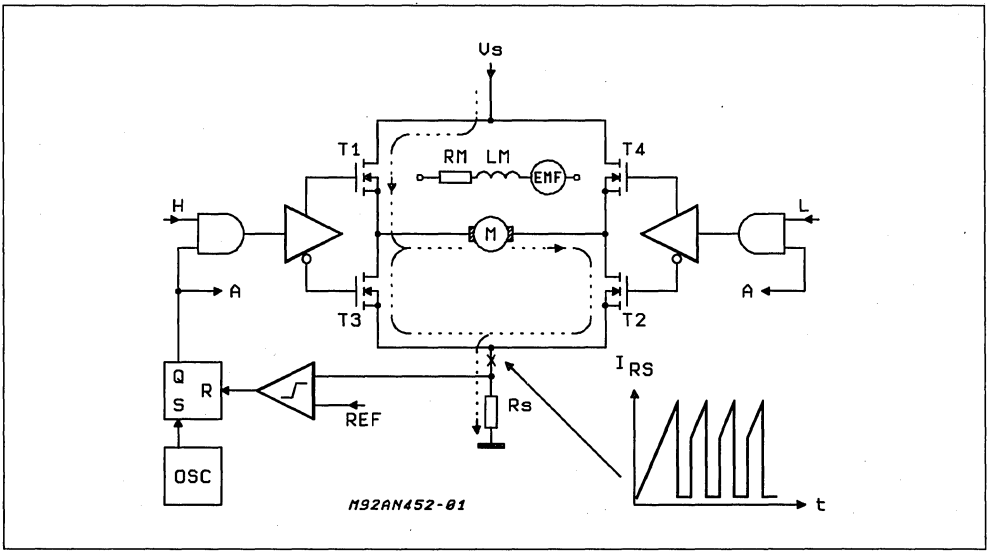
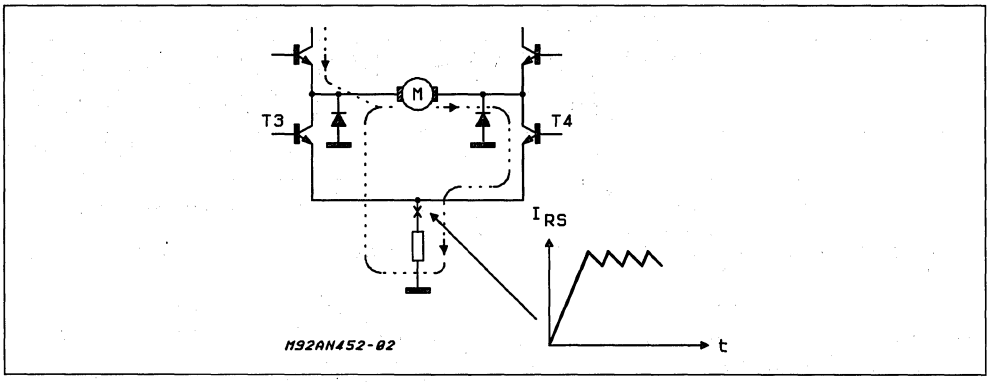


Figure 1B: Switch Mode Current Control Circuit for Load Current Limitation.(Bipolar Bridge Configuration)



A significant difference now becomes apparent between the new DMOS smart power bridges (Fig.1A) and the conventional bipolar configurations (Fig.1B). Since active MOSFET transistors and their body diode are reverse conductive, the load current circulates in the lower circuit and is no longer accessible at Rs. Neither the bridge nor the controller circuit is at risk — always supposing that the current in the short-circuited free-wheeling circuit drops — and the circuit illustrated in Fig. 1A represents the classic solution for simple clocked current limitation functions.

BRAKING

When a DC motor brakes, the counter EMF it generates feeds the motor inductor. When the two lower bridge transistors T2 and T3 are ON and forming what amounts to a terminal short circuit the current increases rapidly to a value equal to EMF/R_M.

Dangers arise if the short circuit current is allowed to exceed the maximum current rating of the bridge. Transistors having a large surface area can help avert damage, but they are costly irrespective of whether the board carries discrete components or smart power chips. It must also be borne in mind that merely short circuiting the terminals leads to a situation in which the motor's kinetic energy is largely converted into heat by the winding resistance, the time the motor needs to come to rest is uncontrolled.

SENSING THE BRAKING CURRENT

Consequently the aim must be to render the current measurable during braking. There are two approaches to this problem, both using current measuring shunts connected to ground on one side for the sake of simplcity.

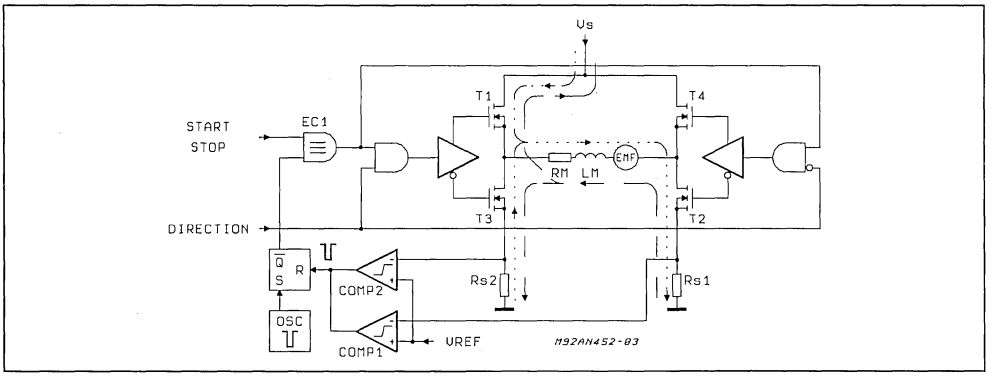
The first arrangement is based on a bridge having interconnected source pins and will be described below. The alternative is a circuit with two separate shunts in the source pins of the lower bridge transistors, as shown in Fig 2.

During the charge phase of the load inductor, the current that causes the motor to turn in a given direction flows diagonally through T1, T2 and RS1. In the free-wheeling phase T2 and T3 are conductive and the situation is as shown in Fig 1A. Despite the fact that during this free-wheeling phase the current is sensed as a positive voltage at R_{S1} and a negative voltage at R_{S2}, the information is ignored because the current is dropping. This no longer applies in the braking phase, when the start-stop input goes low.

At this point a higher current in the free-wheeling circuit activates comparator comp 2. Through the equivalence circuit EC1, the comparator disables T3 and makes T1 go conductive, thus inverting the left side of the bridge for a maximum of one oscillator period. The kinetically generated energy of the counter-EMF stored in the motor inductor is returned to the power input (Vs). This process is repeated periodically until the EMF divided by the motor resistance R_M yields a braking current that is less than VREF/RS1. This controlled return of energy has one major advantage in that the braking current and thus the braking time can be influenced, while on the other hand, a large proportion of the motive energy is recovered and the winding resistance has to dissipate much less heat.

Sadly, however, the configuration shown in Fig. 2 is not feasible with all smart power bridges with DMOS power transistors. Not infrequently the source pins of the lower half of the bridge are interconnected on the chip, either because a limited number of pins are available or because the metal resistance would be too high. In cases of this nature the only resort is to connect two ICs in parallel and form a bridge from two half bridges. Of course this entails an additional advantage in that since conductive losses are lower, too.

Figure 2: Same As Figure 1a but Including Braking Energy Recovery.



SOLUTIONS FOR SERVO SYSTEMS

Circuits such as those shown in figs 1 and 2 are used primarily to protect the motor and semiconductor bridge from overload. Torque limitation is often another major concern in stepper motor drive systems and with DC motors. Although the current can be varied within adequate limits by varying the reference voltage, the tolerance factor becomes larger as the values become smaller because only one-sided peaks can be measured, instead of mean values. If the current fluctuates close to or across zero, another strategy affording greater precision is needed.

Servo systems, being closed-loop control systems with position and speed sensors, are heavily reliant on accurate current sensing in a form that is perfectly reliable in the current reversal range close to zero. This further entails adopting a different drive strategy.

Since a short-circuited free-wheeling circuit in which both lower transistors are conductive would produce severe non-linearities in the current reversal range close to zero, it is to be avoided at all costs. Free-wheeling in this case means selectively inverting the bridge, thus causing the current to drop along a largely linear path, but no more than five to ten percent before the original status is readopted. In a configuration of this nature, a zero motor current means that the bridge remains active, but the sampling ratio is cut to 50%.

Since there are only two conductive states (either T1 and T2 or T3 and T4), the current always flows through R_S, irrespective of whether the circuit incorporates two separate shunts or one common shunt.

Fig. 3 illustrates the current curves and their effect on the sense resistors R_S. Reconstructing the load current requires only an operational amplifier that operates as a subtractor. Via resistor R_1, the capacitors suppress the peaks that occur during changeover. Since the common-mode interference level is high, fast operational amplifiers are the obvious first choice if high signal precision is required.

Figure 3: Current Sensing by Reconstructor.

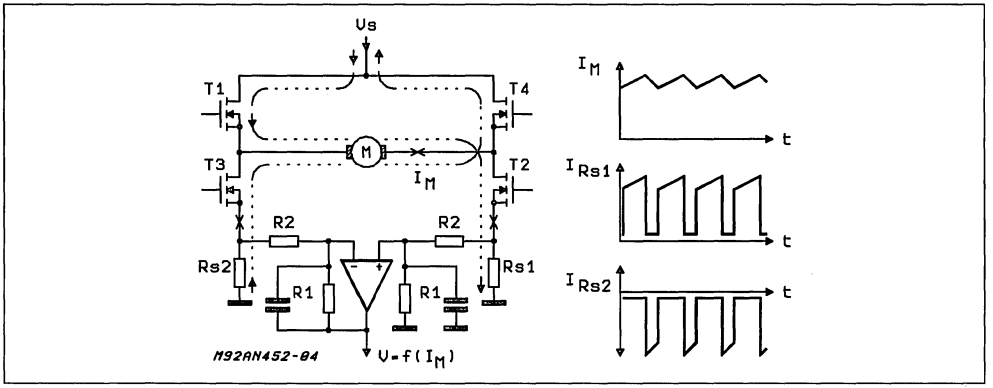


Figure 4: Current Sensing in the Load Circuit.

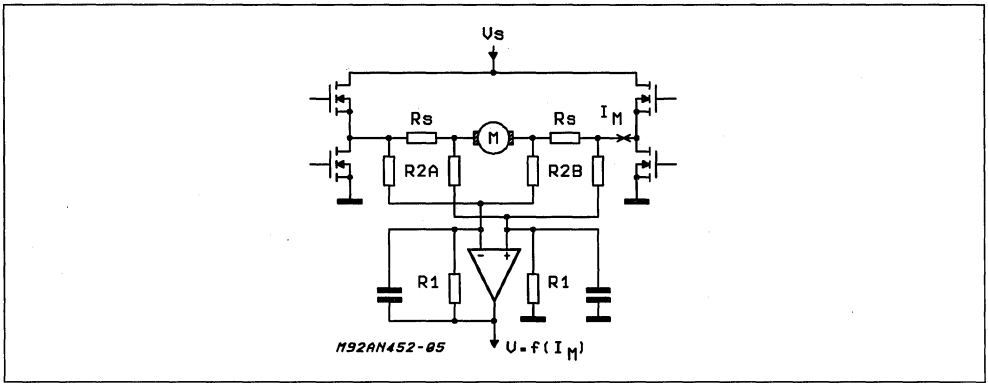


Fig. 4 shows another circuit that is feasible for all situations in which, since they cannot be inserted in the source circuit, the shunts have to be connected directly in series with the load, with all the disadvantages that this entails.

Although a single resistor suffices in theory, an operational amplifier provides the speed and common-mode suppression characteristics that make it virtually the ideal choice. Nonetheless, the results can be improved considerably by sensing the current on both sides of the load. Since measurement is symmetrical, the useful signals and the sense resistors are added together, while the counter-phase edges are subtracted, thus significantly reducing the common-mode load on the operational amplifier. This is true in so far as the matrix resistors are capable of satisfying the very high requirements.

CURRENT RECONSTRUCTION

Bridges with a common source output show an interesting current pattern. The load current is a positive signal during the charge phase of the coil, while it is negative in the inverted state, in other words during the free-wheeling phase. The only way to reconstruct this current is to periodically invert the sense voltage V_{RS}.

Two of the many solutions to this problem are shown in Fig. 5. The V_{RS} signal is applied to the output alternately as a direct or inverted signal (Fig. 5A), or the operational amplifier can work in the inverting or non-inverting mode, depending on the position of the switch. In both cases lateral MOS transistors or even simple small-signal bipolar transistors are perfectly adequate as switches. The RC filter at the output smooths switching peaks without distorting the time constant of the current control loop.

Figure 5A: Recovery of the Load Current Map.(Direct/Inverted Solution)

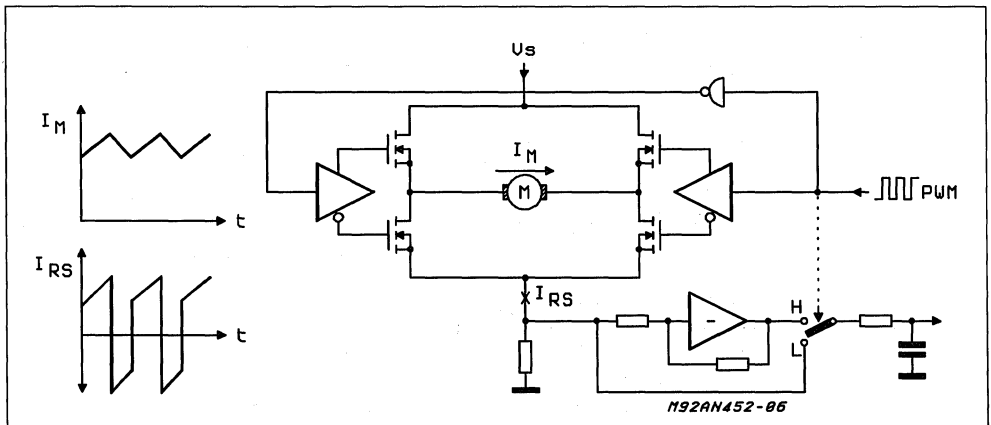
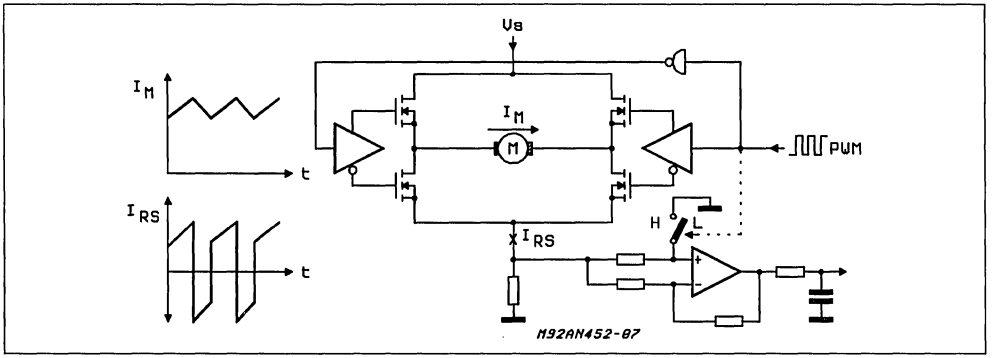


Figure 5B: Accovery of the Load Current Map. (Inverting/non Inverting Solution)



PRACTICAL EXAMPLE

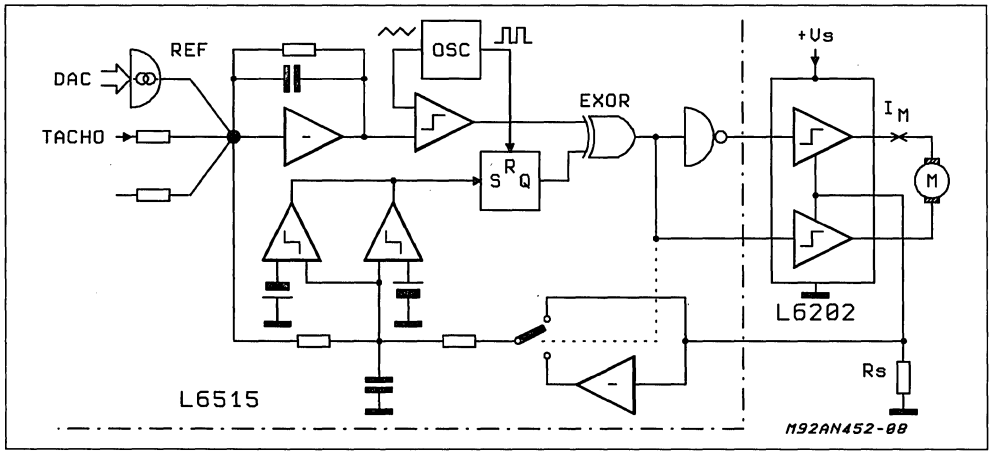
Fig. 6 shows part of the circuit for a DC motor positioning system as use in a typewriter to control four movements. It consists of a controller circuit driving a smart power DMOS bridge with a single current sensing output.

Motor current can reach a maximum of 1A and is influenced by two control loops. The inner loop limits the current by positive or negative peak sampling of the reconstructed current information. An exclusive OR gate inverts the bridge phase for a maximum of one oscillator period, thus causing the current to change its direction. This loop is not delayed and therefore reacts very quickly. The second loop operates in a conventional circuit as a transconductance amplifier and converts an input error signal into a proportional current. If the difference between the measured value and the set point is large enough to force the error amplifier into saturation, the inner circuit limits the acceleration of braking current to the permissible maximum.

POTENTIAL APPLICATIONS

The example circuits for sensing current and processing the signals shown in Figs. 1 to 6 are easily adaptable to other electromagnetic actuators that receive a bidirectional feed. Microstepping motors are a case in point, one in which inexpensive but nonetheless precise current control is very much desired by every user. As power MOSFETS in the guise of discrete components or smart power ICs become more popular, the techniques of sensing current in the source circuit either directly by means of shunts or in directly as sense FETs become correspondingly more important. The unavoidable errors caused by the base current of the bipolar transistors used to date thus become a thing of the past. Although the gate source capacitance remains a potential source of interference, its effect can be suppressed by analog or digital filters.

Figure 6:Part of a DC Motor Positioning Control Circuit.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

A SOLID STATE BLINKER FOR AUTOMOTIVE APPLICATIONS

by Sergio Ciscato

Using dedicated power ICs today it is possible to make a car blinker circuit without relays. The benefits are simpler cablinng and better reliability.

Present car direction indicator system generally use a dedicated integrated circuit as the SGS-THOMSON L9686 in conjunction with a relay to control the flashing of the lamps. A high current electromechanical switch is necessary to turn on the right or the left direction indicator lamps; to provide the emergency blinker feature a 3-pole power switch is needed too (see Fig. 1).
The first disadvantage of this system is the high number of power connections between the master module and the switches; in addition, the high currents flowing through the switches and across the relay contacts decrease their lifetime and consequently the reliability of the system.
Thanks to smart power devices is is possible to implement a solid state car direction indicator system (see Fig. 2), that solves these problems.

Figure 1: Traditional System

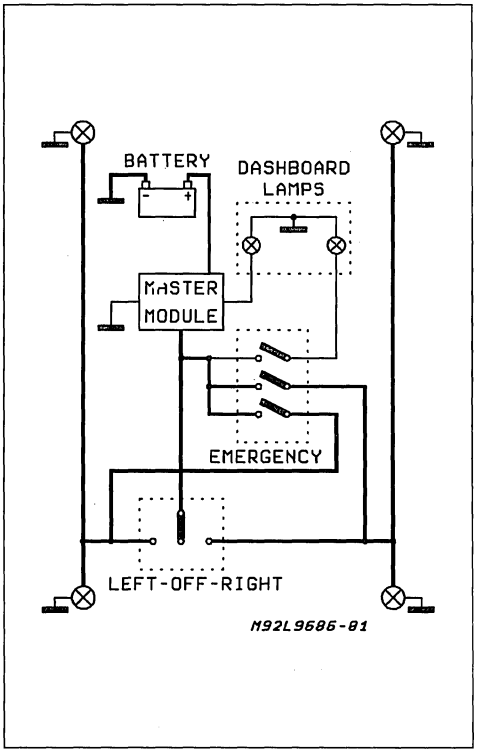
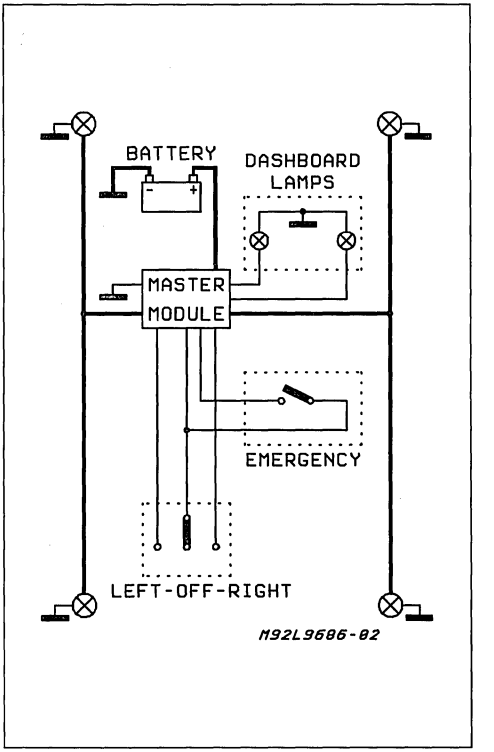


Figure 2: New Solid State System



CIRCUIT DESCRIPTION

The control device in the system described here is the L9686, but the relay is replaced by two L9821 High Side Drivers; this device delivers up to 25A peak output current with R_{ON} = 100mΩ, short circuits and thermal protection.

When a power devices is turned on, the local supply voltage can drop several volt below its nominal value because of the line inductance. This voltage drop could cause disturbances to the control logic that in some cases could produce undamped oscillations on the suplly line itself.

To avoid these oscillations and to prevent EMI disturbances, the L9821 was chosen as the power device in this applications because of a feature that limits the output current slew rate (di/dt) during the switching edges.

Fig. 3 and Fig. 4 show the rising and the falling edges of the output current of an L9821 device loaded with two 21W lamps; the current level in the first case is higher than in the second one because of the inrush current of the bulbs (see Fig. 5).

Figure 3: Rising Edge of the Output Current

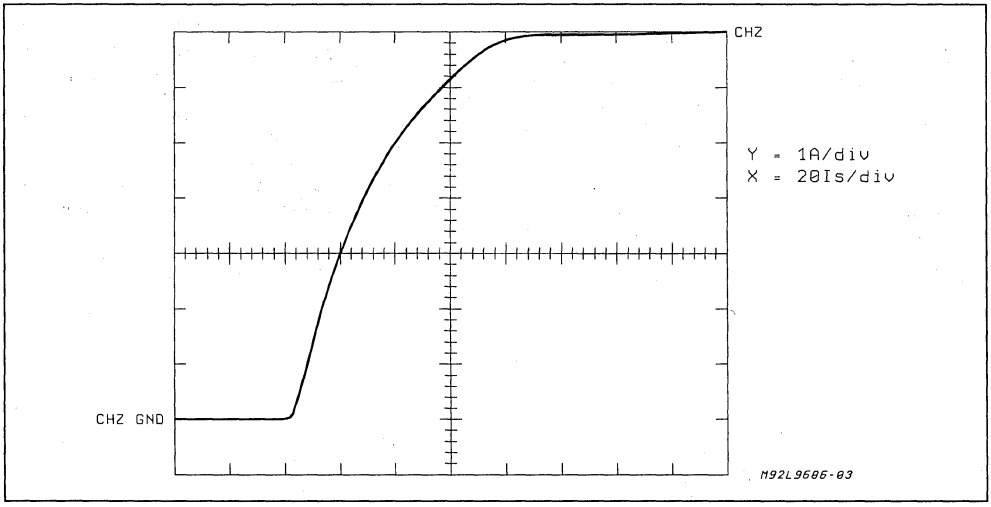


Figure 4: Falling Edge of the Output Current

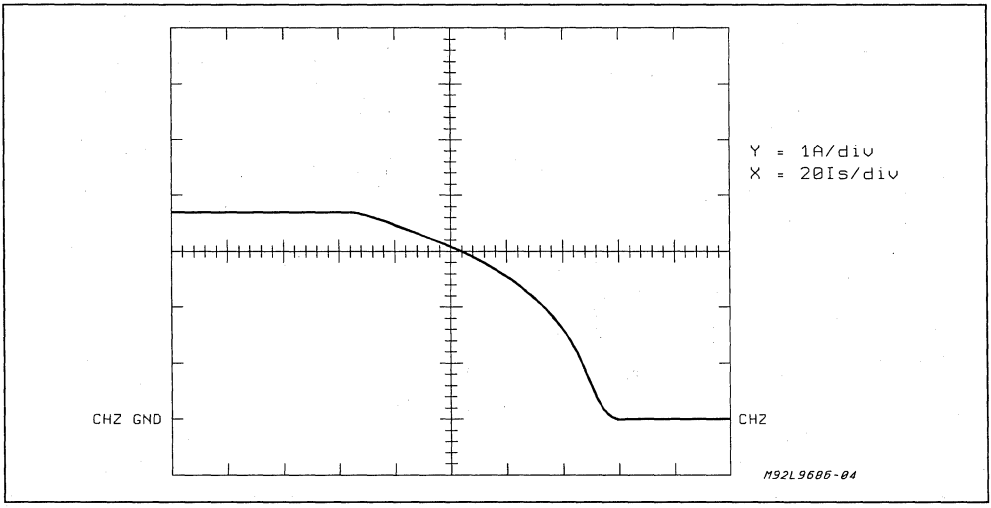


Figure 5: Output Current Waveform

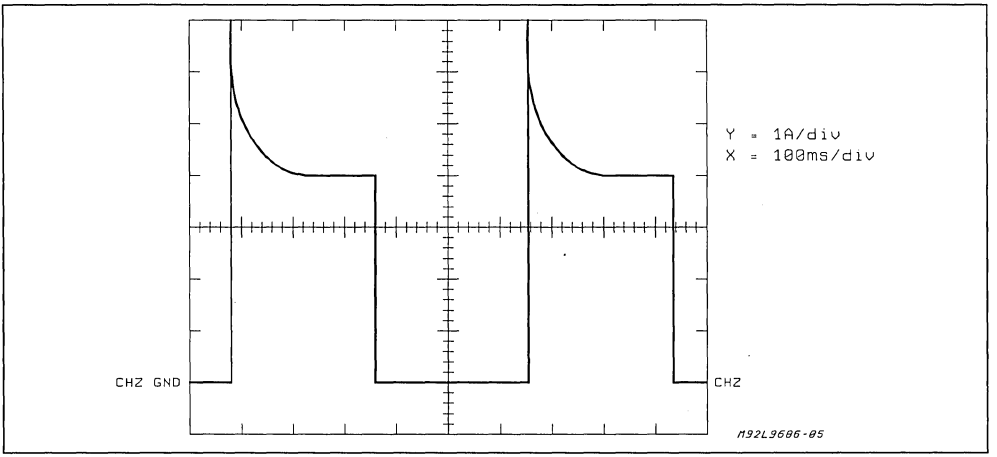


Fig. 6 shows the complete schematic diagram of the master module: when S1 is closed (left or right) the L9686's internal oscillator starts and pin 3 goes high; then the input voltage of one of the two L9821 devices goes high too, resulting in the lamps switching on. After a time equal to half of the oscillation period pin 3 of the L9686 returns low and the lamps are threfore switched off. The flashing cycle stops and the circuit is reset to the initial conditions when S1 is open.
The flashing frequency depends on the external RC networkR1 and C1 according to the following formula:

$$Fn = 1/ (1.5 \times R1 \times C1 \text{ (typ.)}$$

R3 and C2 provide hysteresis to avoid spurious switching of the oscillator comparator at every lamp turn on; this hysteresis is not necessary if the L9686 is used in conjunction with a relay, because of the relatively long delay time of this last one. Rshunt senses the current flowing in the right or the left lamps (depending on the S1 position): when one of the lamps is defective the voltage drop across R_{shunt} is reduced to a half and the failure is indicated by doubling the flashing frequency. S2 allows the emergency blinker function: when it is closed the L9686 device drives, through the diodes D1 and D2, both the L9821 smart switches and hen both the right and the left lamps.

The emrgency blinker operation is monitored by he flashing of both the dashboard lamps L1 and L2 while in normal operation only L2 flashes.

OVERVOLTAGE PROTECTION

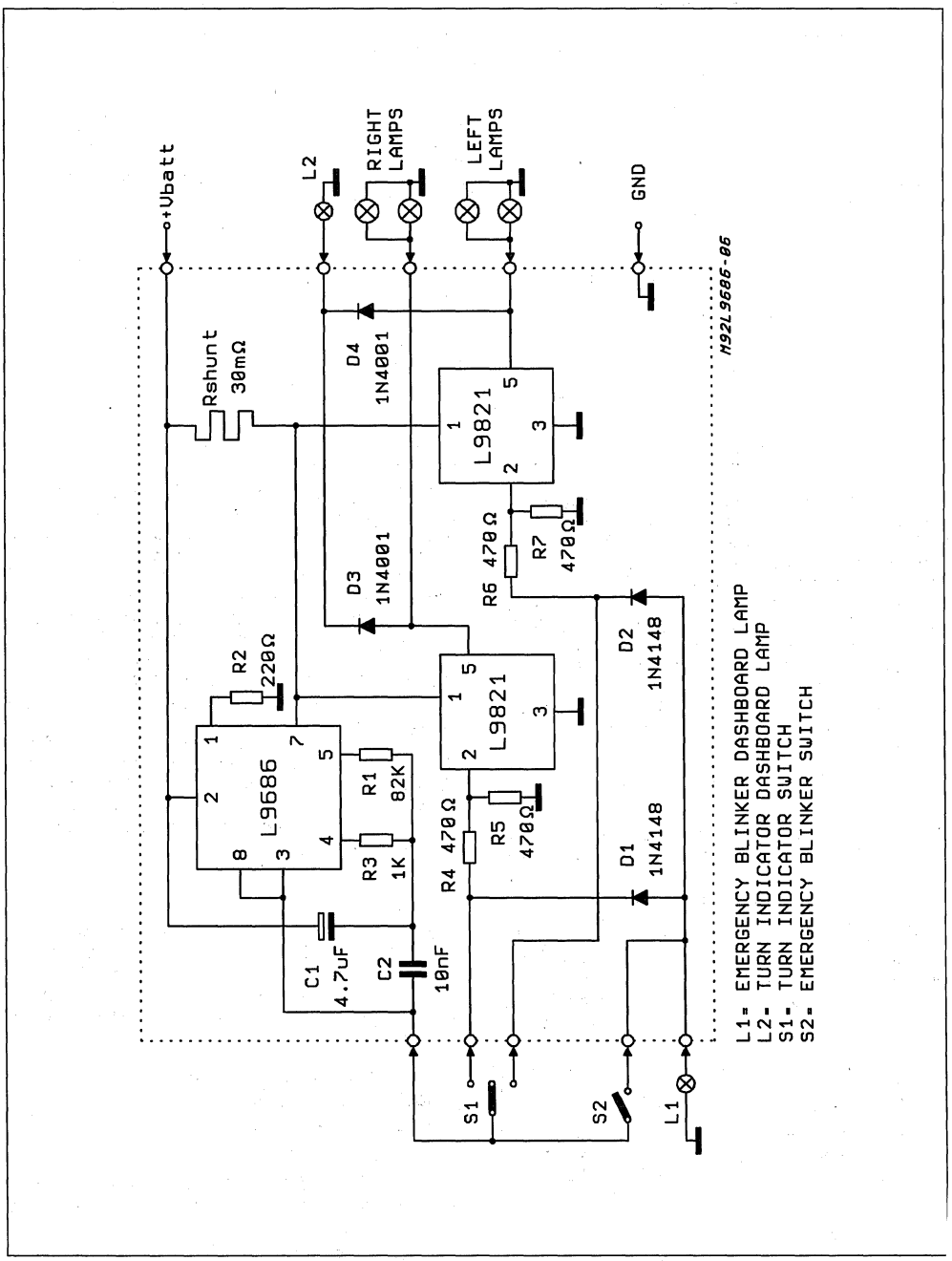
An L9821 device can withstand up to 60V load dump transient. If a centralized overvoltage protection is not provided on the alternator it is possible to increase the load dump capability of this application by placing a dedicated protection device, such as a Transil, between the supply voltage and the ground terminals. This transil must withstand the double battery, a condition often requested for the automotive equipment, so a good choice is a device with at least 26V breakdown voltage. The same protection device allows the described application to withstand all the other voltage transients. If a centralized load dump protection device is already present on the alternator a small protection zener diode is sufficient to clamp the low energy overvoltage transients due to the disconnection of the several loads in the car. In this case the breakdown voltage of the local protection device must be higher than the clamping voltage of the centralized diode.

ADVANTAGES

Fig. 2 shows a possible wiring diagram of the described system in a car; the master module has 10 connections, compared to the four of the conventional system showed in Fig. 1, but from the comparison between the two possibilities we can see some advantages:

- centralized wiring at the master module
- less power connections
- less power wire length
- no power switches
- no multipolar switch for the emergency blinker
- short circuit protection between the lamps and ground
- inrush current limiting of the smart switches increases the lamps lifetime

Figure 6: Schematic Diagram



REAR MIRRORS MULTIPLEXING USING L9946

by L. Valsecchi & S. Vergani

The application of the L9946 device in a real-world automotive multiplex system is described. After a brief introduction to the multiplex concept, the hardware and software key points are discussed. It turns out that L9946 is very well suited for this kind of relatively complex applications.

THE MULTIPLEX CONCEPT

In this section a brief introduction to the basic multiplex (MUX) concepts is given. Generally speaking, a MUX is composed by a number of units connected through a serial bus. There is a set of meaningful serial messages and each unit can recognise a subset of messages relevant to it. Once a relevant message is received, the unit performs an action according to the information contained in the message. Usually an acknowledge technique is used, so that a bidirectional information flow between units can be established. It is possible to draw a rough distinction between MUX systems based on the communication strategy. In increasing complexity order, a MUX can be classified as follows.

1) MASTER-SLAVE:

One unit is qualified as master unit, and it is the only one that can autonomously start a transmission. The other units (slaves) can transmit only after the reception of a message out of a defined set.

2) QUASI MULTI-MASTER:

As before, one unit acts like a master, but some slave units can start an autonomous transmission to the master. This happens usually when a significant event has occurred (e.g. a key has been pressed).However, the slave units cannot communicate each other directly. The messages flow is under the total control of the master unit.

3) MULTI-MASTER:

Every units can commuicate each other, and there is no more a well defined master unit.In fact, the control, at a given time, is owned by the unit currently autonomously transmitting.

The format of the serial messages, as well as the characteristics of the physical interface of the bus line are defined by a series of rules called the PROTOCOL SPECIFICATION. These rules also define in details the behaviour of the transmitting and receiving units when a situation of bus contention (i.e. when two units try to access the bus simultaneously) occurs.

The ISO (International Organization for Standardization) has standarized, at various levels, three protocols called CAN, VAN, J1850. This means that documents exist as a reference to achieve the compatibility between two systems using the same protocol.

In fact, especially for slow speed data bus, custom protocols have been developed.

There are definite advantages in using a MUX system in the automotive field. First, the number of wires required to perform the same functions is dramatically reduced. For example,with the MUX approach, to connect a keyboard unit to other units such as window lift motor control, rear mirror control etc., only three (or four if a differential bus is used) wires are required, independently of the number of keys or motors used. This leads to a reduction of costs of the harness of the vehicle.

Flexibility is another feature common to well designed multiplex systems.

The multiplex architecture allows a high degree of freedom in the choice of the physical location of the units inside the vehicle. For example, as long as the serial bus line is provided, a control keyboard can be placed indifferently in the door or on the dashboard without changing the vehicle wiring.

Furthermore, if a certain computational power (i.e. a microcontroller) is located in the peripheral units, the functional behaviour of the whole system can be defined by software so that upgrading and modification can be accomplished without changing the hardware.

Also, a sophisticated diagnostic strategy can be implemented. Usually one or more units collect diagnostic information that can be read by a tester connected to the system when a car technical assistance is required. Such a tester generally includes a menu driven diagnosis procedure, lead-

ing to easier fault detection and thus to shorter repair time.

REAR MIRRORS MULTIPLEX SYSTEM

INTRODUCTION

The application described here is an example of how the L9946 can be used as a mirror controller in a MUX system.

To explain in all the details a MUX system design is beyond the scope of this application note. However, the key points in hardware and software design will be discussed in depth.

GENERAL DESCRIPTION

This MUX is composed by a keyboard unit, a left mirror unit and a right mirror unit.

The electronics is intended to be placed inside the external rear mirror case, and inside the physical keyboard. To achieve this, when possible, devices available in small SO package have been chosen. In this way, using surface mounting technique, very compact PCB layout can be obtained.

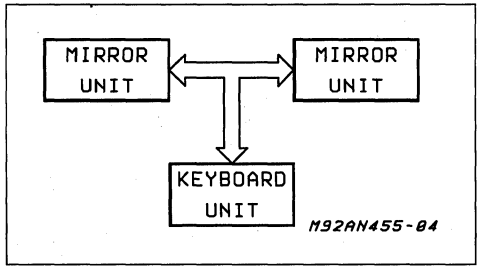
The three units are connected through a differential bus.

Including power supply line and ground return, only four connection wires are required, obtaining a substantial saving compared to the traditional solution, that requires eight wires.

The system block diagram is shown in fig. 1.

The functions implemented are:

Figure 1: System Block Diagram



- mirror plate movements
- open / fold
- wiper

The commands available are activated by 6 push buttons located in the keyboard unit.

An additional three-way selector allows to switch between the left or the right mirror. When this selector is in its central position, the only function available is a simultaneusly mirror open/fold movement.

MIRROR UNIT DESCRIPTION

The block diagram of the mirror unit is shown in fig. 2.
The schematic diagram of the mirror unit is shown in fig. 3.
The only difference between the left and right mirror unit is the position of a jumper that configures the address of the unit.

Figure 2: Mirror Unit Block Diagram

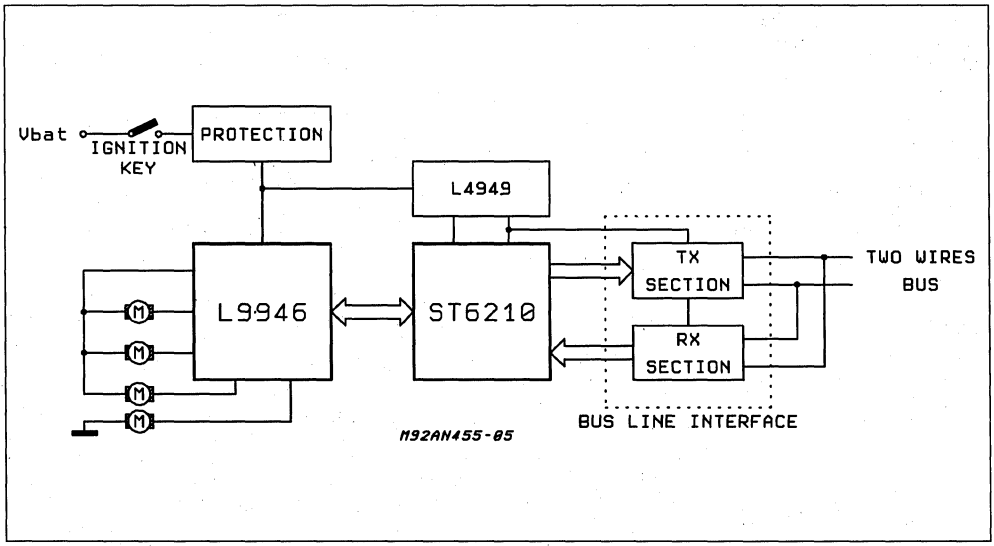
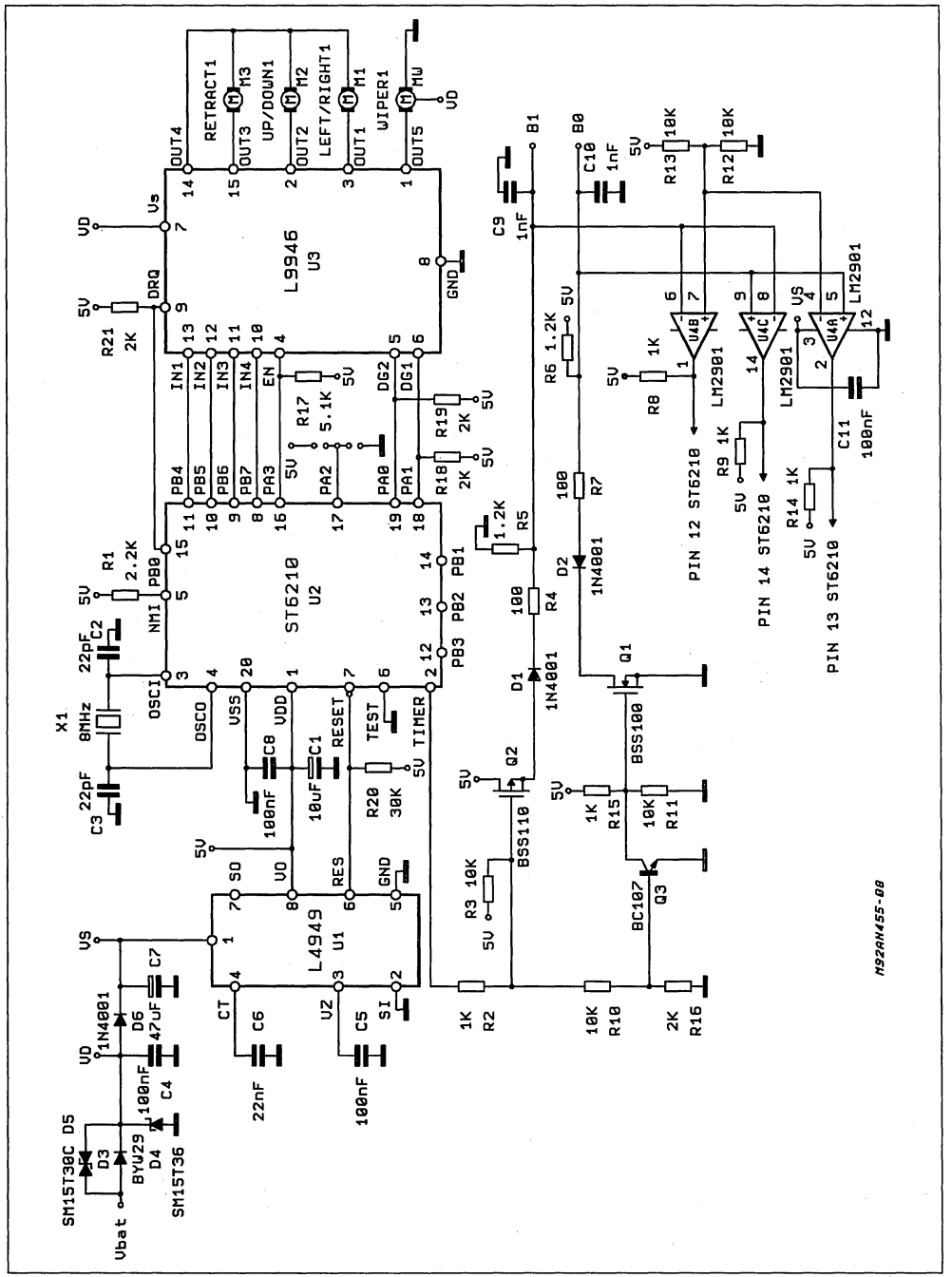


Figure 3: Mirror Unit Schematic Diagram.



In the following sections the main functional blocks are described.

Protections

The units must be protected against a number of possible anomalous voltages on the power supply line coming from the battery.

This anomalous conditions are:

1) Reverse battery

2) Load dump

3) Short negative spikes

Voltage Regulator (L4949)

This device provides the five volts necessary for the microcontroller and to the bus line interface. It also provides to the microcontroller the correct power on reset signal.

Microcontroller (ST6210)

The microcontroller (uC) choosen for this application is the ST6210 (1K8 EPRPOM, 64 bytes RAM).This is a 20 pin device, available in SO20 package. The ST6 family is intended for low-medium complexity applications.

The heaviest task for the uC in this, or similar, application is the protocol handling, i.e. the reception and the transmission of the serial messages on the bus.

Due to the low computational power and speed of this uC, the protocol was chosen to be relatively slow (3.3 kbits/sec) and the bit encoding was chosen in such a way that the decoding algorithm is tailored to optimize the hardware uC resource usage.

In this case the uC also drives the L9946 and protects it against overcurrent and/or overtemperature reading back the dignostic signals DG1 and DG2.

Mirror Actuator (L9946)

The L9946 in this application is used to drive the four mirror motors: two for the plate movements, one for the open/fold movement and one for the wiper motor. In this particular application the wiper can be driven by the high-side driver thanks to a mechanical solution built into the mirror that performs automatically the wiper alternative movement.

Bus Line Interface

This is the circuitry that realize the physical interface between the unit and the bus line. Since the functioning of the whole system relies on the correctness of the exchanged messages, the bus line interface must be designed very carefully. A complete discussion of the needed design criteria is far beyond the scope of this application note.

A list of desirable features is:

a) High noise rejection

b) Line faults (short to GND or VCC, wire cut) detection and real time recover.

c) High RF noise immunity

d) Low RF emission

The solution implemented here is a differential bus line driven by two complementary MOS devices.

The passive components around the MOS polarize and protect the devices against shorts, spikes and negative voltages applied to the bus lines.

Capacitances placed on the bus lines filter out RF noise, also reducing the bandwidth of the bus channel in order to avoid too sharp edges during bus transitions, i.e. RF emission and subsequently possible interferencies with other equipment (dashboard instrumentation, car radios etc.)

The three comparators in the RX section allow a full fault detection and recovery. This means that transmission and reception can continue also if one line is shorted to GND or V_{CC} or cut.

Figure 4: Keyboard Unit Block Diagram

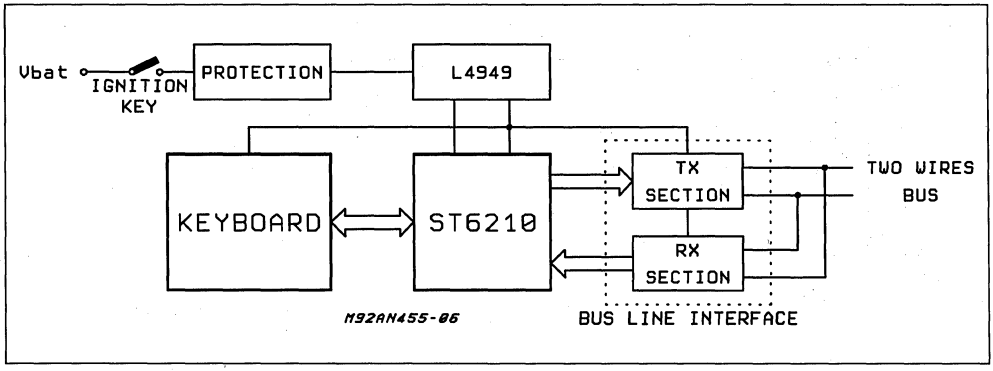
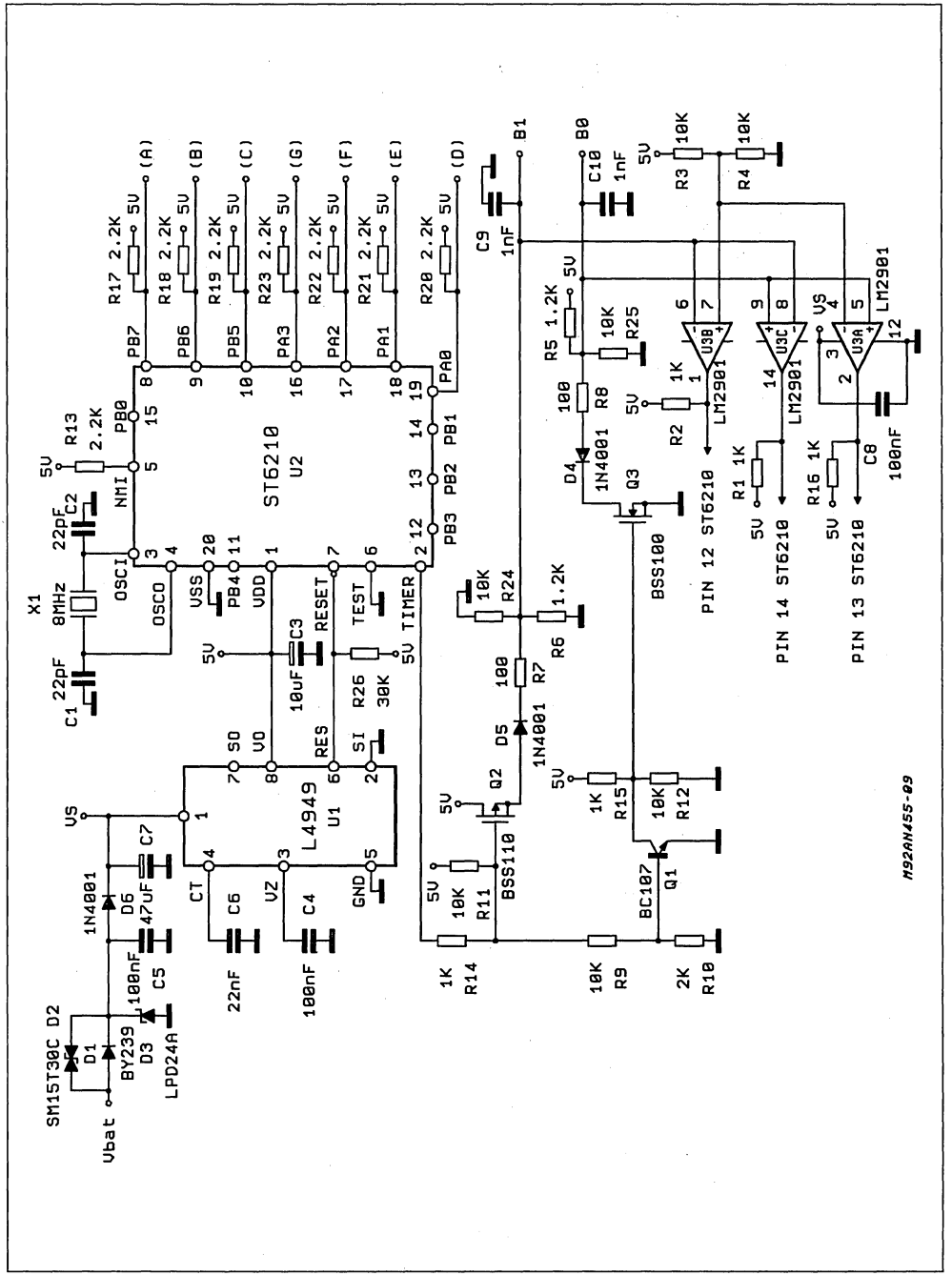


Figure 5: Keyboard Unit Schematic Diagram.



KEYBOARD UNIT DESCRIPTION

The block diagram and the schematic diagram of the keyboard unit are shown respectively in fig. 4 and fig. 5.

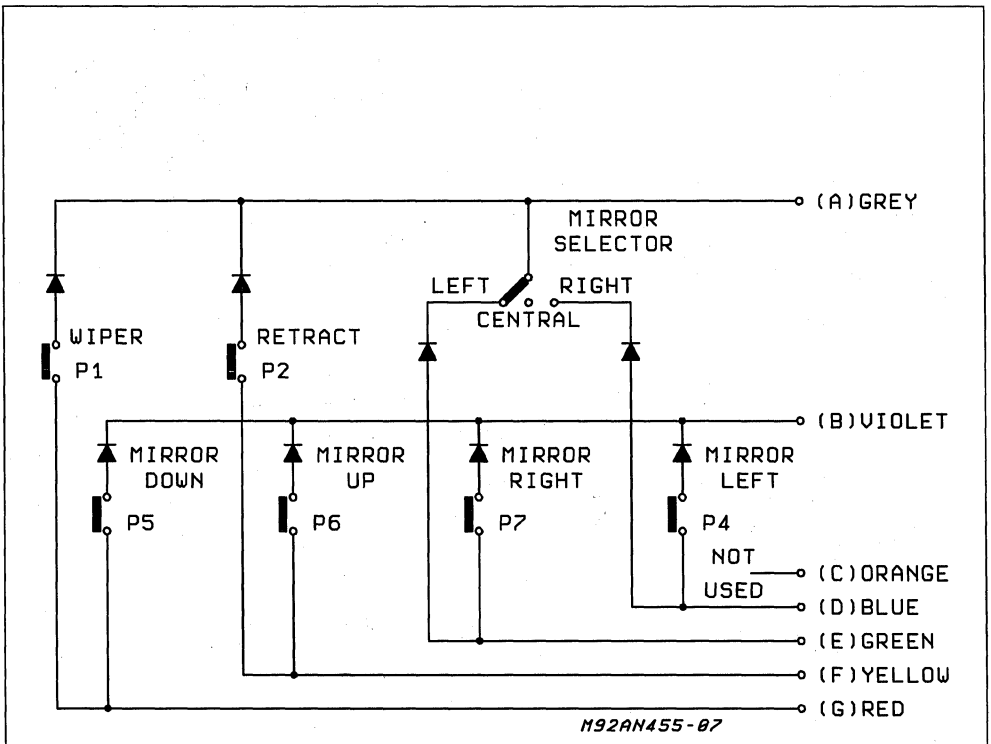
Many blocks in the architecture of this unit are very similar or identical to those used in the mirror unit.

This blocks are protections, voltage regulator and the bus line interface. The uC used is the same adopted in the mirror units.

A 4 X 2 matrix-organized keypad is connected to the unit. The schematic diagram of the physical keyboard is shown in fig. 6.

Since the physical keyboard rows and columns are directly connected to the uC pins, it must be placed very close to the electronics to avoid induced noise. A software debouncing strategy has been implemented so that a key transition is validated only if the new state has been stable for at least fifty milliseconds.

Figure 6: Keyboard Schematic Diagram.



SOFTWARE DESCRIPTION

Introduction

Two different programs have been written, one for the mirror units and one for the keyboard unit. The software was developed using the ST6 hardware emulator, and the ST6 macroassembler and linker. The mirror unit and keyboard unit programs are respectively about 1340 and 1280 bytes long. The main difficult in this software development was to overcome the uC limitations (using some software tricks) without affecting the overall program's readability.

Mirror Unit's Software Description

The software developed for this unit can be divided, at the functional level, into 3 main sections.

1) PROTOCOL HANDLER SECTION

This routines perform the serial bus message reception and transmission.

The reception procedure starts when a valid SOM (see BUS PROTOCOL DESCRIPTION paragraph) is detected. The reception ends successfully when the following conditions are obeyed:

a) Ten correct bits (i.e. with the right timing between two edges) are decoded.

b) The received checksum field matches the checksum calculated upon the preceding eight received bits.

If an error occurs, the reception is aborted and the unit starts to wait for a new valid SOM.

The transmission routine starts when the unit must send a message on the bus line. The ST6 timer is used to obtain the desired time between the edges.

2) MESSAGES DECODING AND ACTUATIONS

This section performs the message decoding and the actual driving of the L9946.

Once a correct message is received, the mirror unit compares the received address field with its own address. If they are equal, the data field of the message is decoded and the corresponding action or series of actions are undertaken.

The data fields recognized by the mirror units and their meaning are:

01110 : wiper on

10000 : wiper off

01010 : fold/open

00010 : up movement

00100 : down movement

00110 : left movement

01000 : right movement

10010 : stop motors

Immediately after the action has started, the mirror unit transmits an acknowledge message to the master unit (i.e. the keyboard unit). This message is the echo of the acknowledged reception.

3) L9946 PROTECTION

The L9946 DG1 and DG2 pins are connected to uC interrupts lines so that a fast switch off is executed when an overcurrent or an overtemperature occurs in the device.

Keyboard Unit Software Description

In the sotfware for this unit the protocol handler section is the same code used in the mirror units.

The keyboard units acts like the master of the system.

The matrix keyboard is scanned every five milliseconds. If no key status variation is detected, every fifty milliseconds a stop message is sent to the slave units as a polling. The slave units should answer to this messages. If this is not the case, the master unit knows that one or both slaves are disconnected or broken.

When a key is pressed, a debouncing procedure is started. If the pressure remains at least for fifty millisecond the corresponding command message is sent to the unit selected by the position of the three-way selector.

If this selector is in its central position, only the fold/open command is enabled, and the subsequent command is sent to both slave units.

The keyboard unit keep sending the command until the key is released. Then, the normal no-operation polling is executed.

BUS PROTOCOL DESCRIPTION

1. GENERAL

The information between the units is passed in messages transmitted serially on the bus connected to all the units.

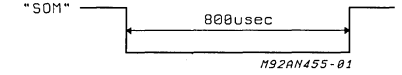
When the bus is in the idle state, i.e. no message is transmitted, its state is called "passive state". It is driven in the "active state" by a transmitting unit at the start of a message for the "start of message" time.The state is passive for the first (most significant bit) information time, active for the next bit time and so on until the message is finished (terminated) in the passive state. The value of the bit is determined by the time elapsed between two consecutive transition of the bus state. This bit encoding is called VPWM (variable pulse width modulation).

2. MESSAGE SYMBOL WAVEFORMS

The following sections show the nominal timing requirements of the VPWM message simbols generated by the software protocol handler as they appear on one wire of the bus. On the other bus wire the signal is inverted.

2.1. START OF MESSAGE

This symbol appears at the start of every message when a transmitter drives the bus in the active state to start the message.

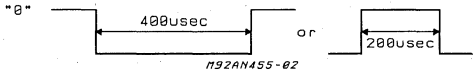


2.2. DATA BIT

Each data bit is represented by the time between two consecutive transitions. These are both passive and active bit states that are used alternately.

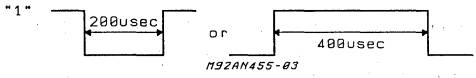
2.2. "0" BIT

The two "0" bit waveforms are:



2.3. "1" BIT

The two "1" bit waveforms are:



3. MESSAGE FORMAT

A message consists of a start of message (SOM) field, an address (ADR) field (3 bits), a data (DATA) field (5 bits) and a checksum (CHK) field (2 bits), for a total of 10 bits transmitted.

With the timing given in the above sections, the average transmission bit rate is 3.3 Kbps.

The SOM is the signal on wich every receiving unit starts the reception procedure.

Once a successful reception has been completed, the DATA field is decoded and the related action undertaken only if the ADR field matches with the wired address assigned to the receiving unit.

The CHK field is a way to detect some type of errors occurred during the DATA field bits transmission. During the reception procedure, a checksum value is calculated, and the reception is valid only if this value is equal to the contents of the received CHK field.

The algorithm used to calculate the checksum is the following.

a) Count the number of "1" bits in the DATA and ADR fields.

b) Take the two less significant bits of this number.

c) Complement these bits.

SGS-THOMSON MICROELECTRONICS

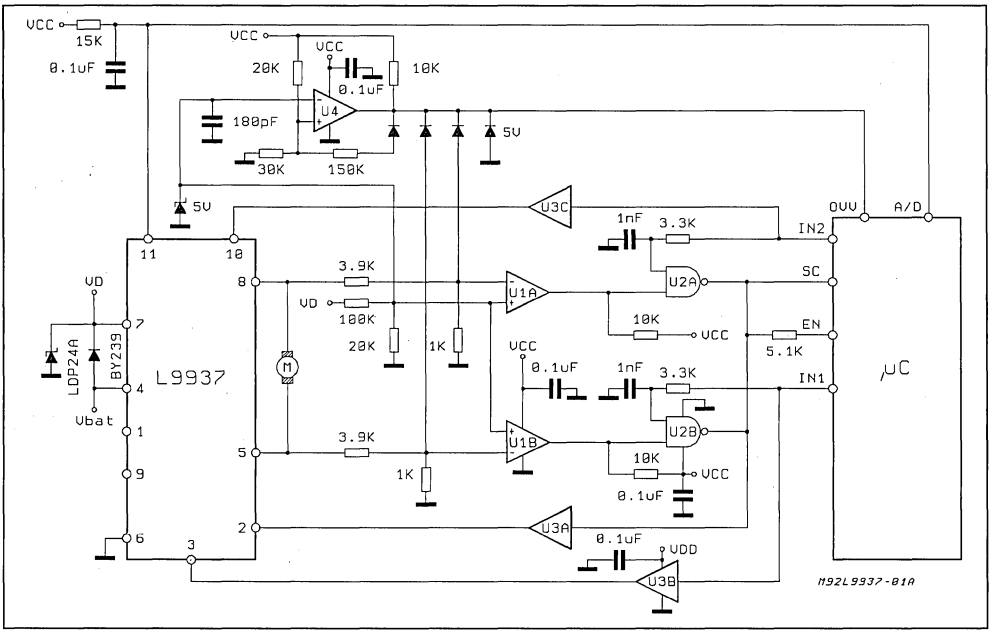
APPLICATION NOTE

6A DOOR LOCK MOTOR DRIVER FOR AUTOMOTIVE

by Stefano Vergani

An application of the L9937 device (Full Bridge Motor Drive) is described. The interface between the L9937 and a µC is discussed. A complete protections circuitry description is also given.

Figure 1.



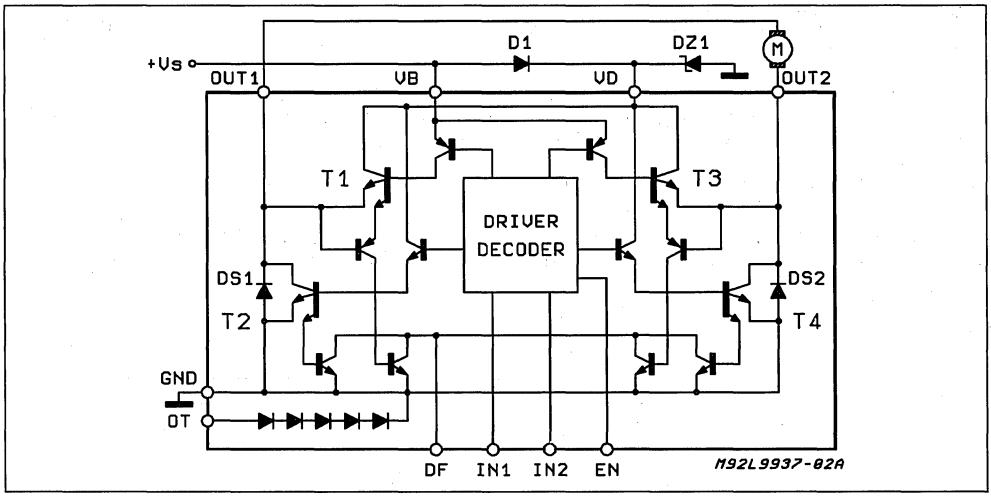
The L9937 device is a full bridge for bidirectional motor driver applications realized in bipolar technology; it can deliver up to 6A output current with low saturation voltage.
Two diagnostic informations are provided to monitor overload conditions and the internal temperature, and the device is assembled in the MULTIWATT-11 package with the case connected to the ground terminal.
The L9937 is particularly suitable to drive bidirectional DC motors in µC based systems.
Fig. 1 shows a possible application circuit, with an analog interface between the power devices and the µC.

In the following, the functions of each block of the analog interface are described.

1 - Overvoltage And Reverse Battery Protection

L9937 is particularly suitable to drive the door lock motors in automotive applications. Fig. 2 shows the circuit schematics; due to the hostile automotive environment, it is necessary a transil (suggested type LDP24A) between V_D and GND, to protect the L9937 against overvoltages higher than 50V. The diode D1 suggested type BY239-200A) supplies the voltage VD necessary for the correct device's operation at the same time it protects the device against the reverse battery.

Figure 2



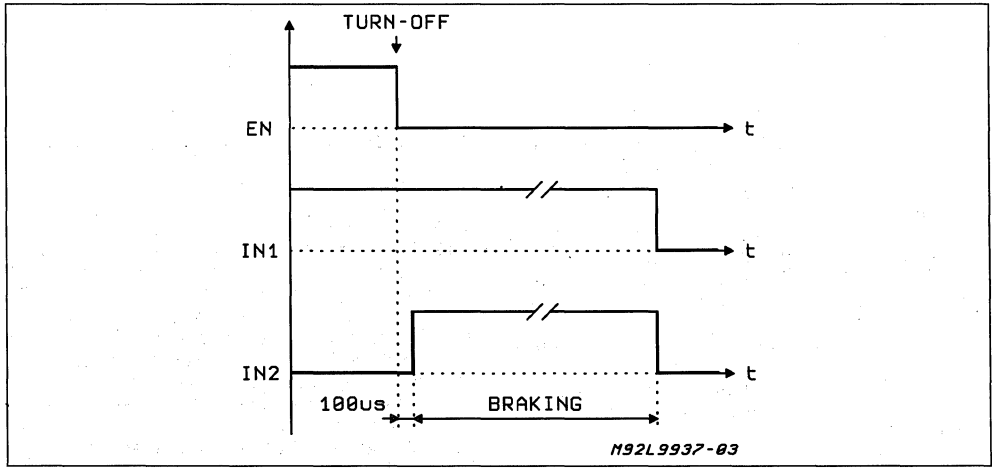
2 - Switch-off Sequence

Referring to Fig. 2 and supposing i.e. T1 and T4 ON, T2 and T3 OFF (this means EN=H IN1=H IN2=L), the following steps have to be observed to allow a correct recirculation of the current in the motor at the switch off (Ref. Fig. 3):

a)switch off T1 and wait for 100µs about in this condition (EN = L IN1 = H IN2 = L)
b)after the a.m. delay switch ON T2 (EN = L IN1 = H IN2 = H)
c)switch off both T2 and T4 after the motor stop (EN = L IN1= L IN2 = L)

Step a) allows the recirculation of the motor current due to the inductive component of the motor itself between DS1 and T4; the 100µsec delay time is needed to avoid the cross-conduction in the left half bridge.
In step b) the motor is short circuited to GND (T2 and T4 ON) and this allows the dynamic braking. In step c) T1, T2, T3 and T4 are OFF to allow a very low current consumption of the bridge. If the dynamic braking is not requested, step b) can be omitted. In any case the lower power transistor of an half bridge must be kept ON, after the switch off of the upper transistor of the other half bridge, for a time longer than $T = 5 \cdot R_L/L_L$, where Rl and Ll are the resistance and the inductance of the load.

Figure 3: Switch-off Sequence



3 - Input Driving Voltage

To allow a correct operation of L9937 over the full temperature range, the driving voltage at the input pins must be higher than 5.5V, with 4mA current capability.

4 - Short Circuit Protection

It is possible to protect L9937 against short circuit to ground and across the motor in the full bridge application.
The circuit schematics shown in Fig. 4 uses two voltage comparators (U1A, U1B) to detect the Vce of the upper power transistors. U2A and U2B are open drain NAND gates (i.e. part no. HCC40107) and U3A/B/C/D are non inverting buffer to drive the L9937 (i.e. part no. 74HC4050).
U1A and U1B sense the differential voltage VD-OUT2 and VD-OUT1 respectively. Referring to Fig. 4, chosen R1=100K and R2=20K, the values of R3 and R4 may be calculated according to the following formula:

$$R3 = \frac{(V_D - V_{CETH}) - 0.166\ V_D)}{0.166\ V_D} * R4$$

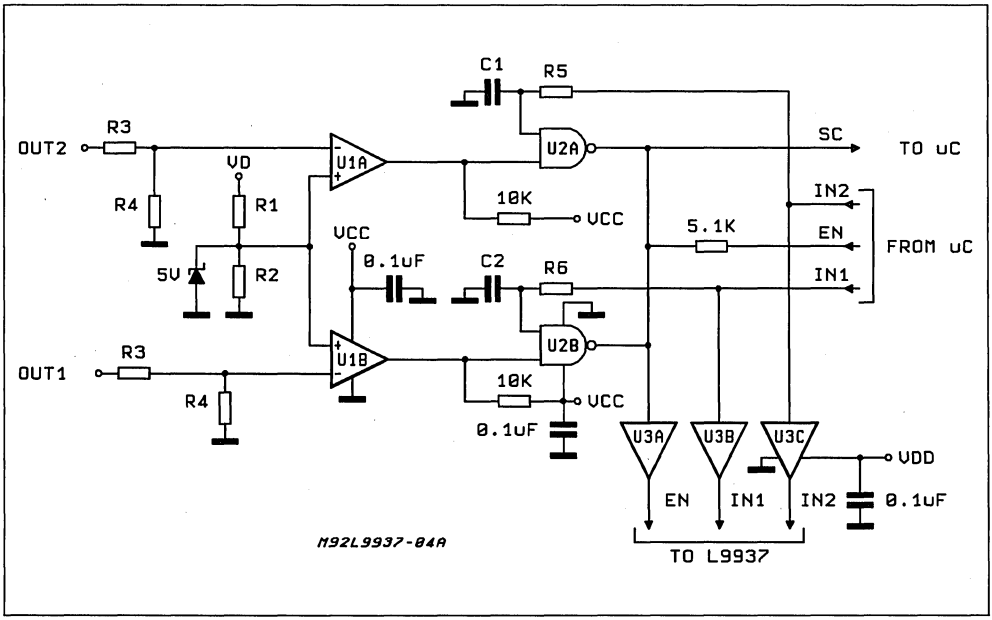
where :

V_D = bridge power supply
V_{CETH} = collector to emitter detection threshold.

Choosing:
V_{CETH} = 2V @ V_D = 12V and R4 = 1K, the above formula gives R3 = 4K.

When all signals from µC are at low level (motor off), the inputs to the bridge are low too; in these conditions the output voltage of the two comparators is high and therefore the outputs of U2A/U2B are free. When the µC sends, for example, IN2 and EN high, OUT2 of the bridge goes high and OUT1 goes low.
At this point the output of U1A pulls down the input of U2A before that the delay capacitor C1 is charged (through R5) up to the U2A threshold; in this way the U2A output remains free and the bridge drives the motor.
If a short circuit occurs, the Vce of the upper power transistor increases above the threshold and then the U2A output pulls down the enable input of L9937. At the SDME time the SC signal to µC, high in normal conditions, goes low; at this point the µC executes the switch-off sequence.
We have just explained what happens when a short circuit occurs during the motor running phase. Another faulting condition occurs switching on the bridge when a short circuit is present; in this case the bridge is driven for a time depending on the time constant R5 • C1 = R6 • C2.
Choosing R5 = R6 = 3.3K and C1 = C2 = 1nF, then the time constant will be T = 3.3µsec, that is 5µsec about delay time. Longer delay time might allow the short circuit current to reach values beyond the absolute maximum ratings.

Figure 4



5 - Thermal Protection

The L9937 has 5 built-in diodes series-connected that can be used to implement a thermal protection for the device.
Fig. 5 shows the relationship between the voltage across the diodes and the temperature at 100µA diode current.

Figure 5

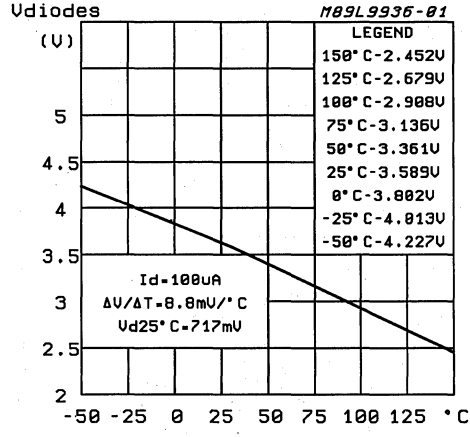
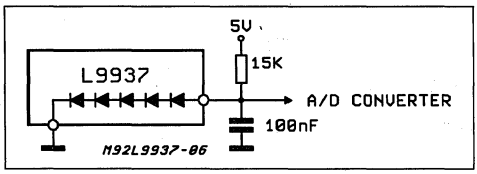


Fig. 6 shows the simplest solution to do a thermal protection; an A/D converter of the µC is used to detect the voltage drop across the 5 diodes. The 15K resistor sets the current in the diodes and the 100nF capacitor acts as a filter against the noise. When the µC detects a voltage lower than the low threshold chosen according to the diagram in Fig. 5, it executes the switch-off sequence and rejects any command to the bridge until the diodes voltage increases beyond the high threshold. The recommended hysteresis value is 30°C.

Figure 6

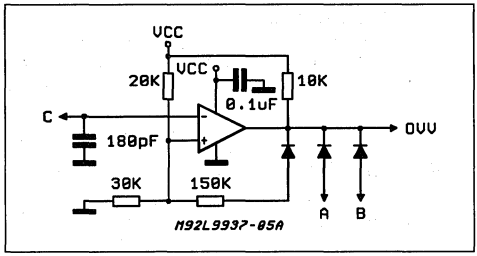


6 - Overvoltage Protection

At point 1 we suggest a way to protect the L9937 against the voltage transients. This protection allows the device to withstand overvoltages only if the bridge is not operating. To protect the device against the overvoltages in all the operating conditions it is possible to implement the circuit shown in Fig. 7.

(Note: A-B are connected to the nodes between

Figure 7



R3 and R4 (left side and right side) in Fig. 4; C is connected to the node between R1 and R2 in Fig. 4). When V_D reaches 18V the comparator output pulls down A and B, causing the intervention of the hardware protection showed in Fig. 4; at the same time the OVV signal is sent to µC, which executes the switch off sequence. The µC must reject any command to the bridge during the overvoltage conditions.
With the values shown in Fig. 7, a 1V hysteresis is provided.
It is possible to enhance the performances of the system just described avoiding the braking of the motor also for short duration voltage transients; to do this the µC, once received the overvoltage diagnostic signal (OVV), put at low level the enable of the L9937, confirming the hardware switch-off of the motor; in this condition an output of the half bridge is in high impedance state and the other one is low, allowing the recirculation of the current and the free running of the motor.
The system holds this condition until OVV is active; when the OVV signal is released the µC resets the hardware protection, sending EN = IN1 = IN2 = L and then restore the previous command to the bridge.
It is mandatory, however, to wait for the complete current recirculation of the motor before to reset the hardware protection; in facts, when EN = IN1 = IN2 = L both the L9937 outputs are in high impedance conditions.

7 - Diagnostic Feedback Output

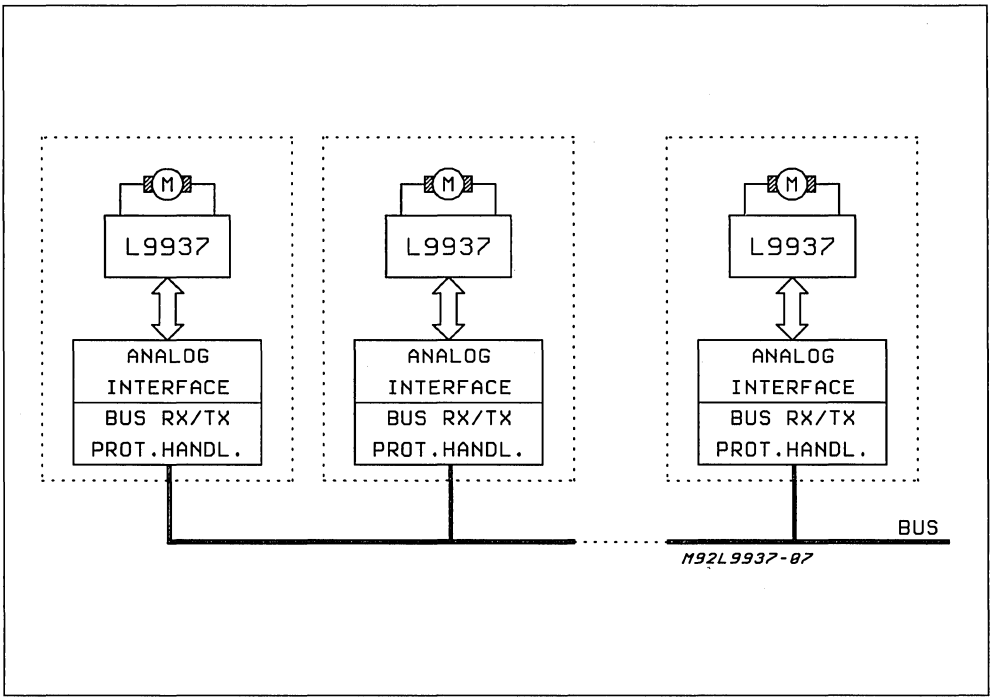
DF pin is an open drain output to monitor overcurrent and overtemperature conditions.
The overcurrent detection threshold is inversely dependent from the temperature of the chip.
Typical application of this function is to send the DF signal, with an external pull-up to Vcc, to a digital input of the µC; when the DF signal goes at low level, the µC executes the switch-off sequence.

L9937 IN A BODY MULTIPLEX ENVIRONMENT

All the functions described above can be implemented in a custom integrated circuit together with a bus transceiver and a protocol handler.

It is then possible to obtain a very small size module that can be integrated directly in the actuator. Fig. 8 shows a typical application of these modules as peripheral units in a "Class A" wired Multiplex System.

Figure 8: "Class A" Wired Peripheral Application



DRIVING DC MOTORS

By G. Maiocchi

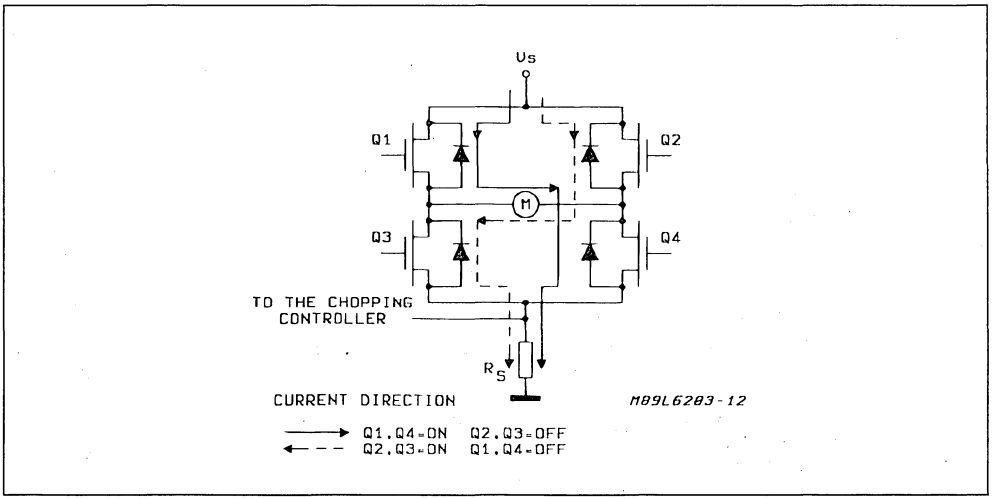
INTRODUCTION

Driving DC motors with integrated circuits seems at first to be rather simple. Yet by analyzing the actual application it is possible to see if there exist conditions causing stresses to the IC during operation which in the end can cause failure. With proper design and analysis in critical applications it is possible to avoid conditions which lead to IC damage.

GENERAL CONSIDERATIONS

Figure 1 illustrates driving a DC motor using a power MOS bridge.

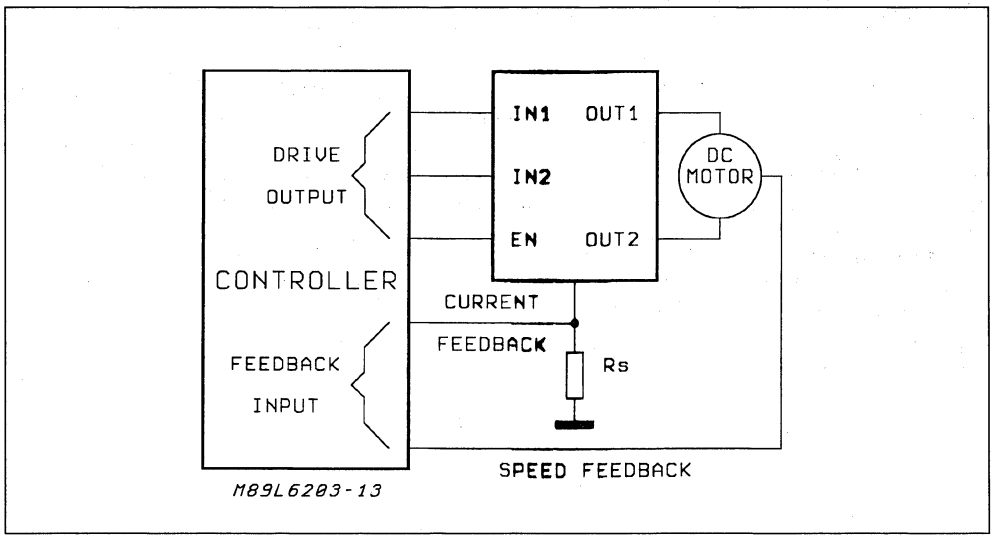
Figure 1.



By driving the four MOS in the correct sequence the direction of current flow through the motor is reversed, consequently reversing the direction of the motor's rotation. The motor torque is a function of the current amplitude, the motor's internal parameters, and the external load. The resistive torque is dependent on the motor's internal friction. The current level can be controlled with current chopping. The controller checks the current level by monitoring the sense resistor voltage and then drives the appropriate power MOS. On the other hand this means that when current does not flow in the sense resistor (which we will examine during recirculation) it is not possible to measure the current level and thus limit it.

Figure 2 shows a more general application circuit which includes an external control loop. Data relating to the actual motor speed is transmitted to the controller by the system which stabilizes the current in the bridge as a function of the requested rotation velocity. In this case also the current is limited through chopping.

Figure 2.



Electrically a DC motor can be viewed as a series RL network with a voltage generator V(ω). The generator represents the back electromotive force (BEMF) generated by the motor's rotation and which opposes the electromotive force of the supply.

The value of the BEMF is a function of the motor's angular velocity. If the motor has no external load and its velocity is not limited, it will accelerate up to the velocity w such that V(w) equals the supply voltage Vs. In this situation the two EMF's cancel each other and thus the motor torque responsible for acceleration will go away. In reality V(ω) is always slightly less than Vs in which case a small motor torque is necessary to compensate resistive torque due to internal friction.

Thus it can be seen that the motor's BEMF can reach elevated values which in some cases can create application problems due to a certain type of stress.

RECIRCULATION CURRENT

Part of the energy delivered to the circuit by the supply is stored in the motor's inductance. When an inductive load is driven, during chopping and during inversion of the diagonal of the bridge, there is always some recirculation current which allows this energy to discharge.

The following figures show the resulting current paths based on the type of chopping method used. In the first two cases, "two-phase" and "enable" chopping, the current decays quickly and, is thus, fast recirculation. When "one-phase" chopping is implemented the current requires a longer time period to decay and, is thus, slow recirculation.

Figure 3a : Two Phase Chopping.

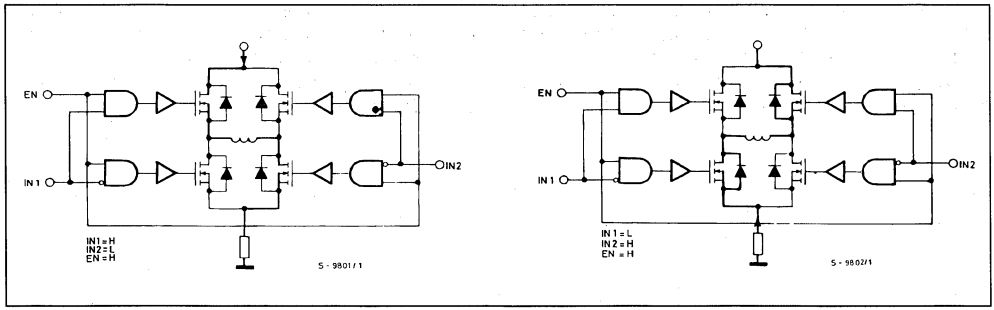


Figure 3b : Enable Chopping.

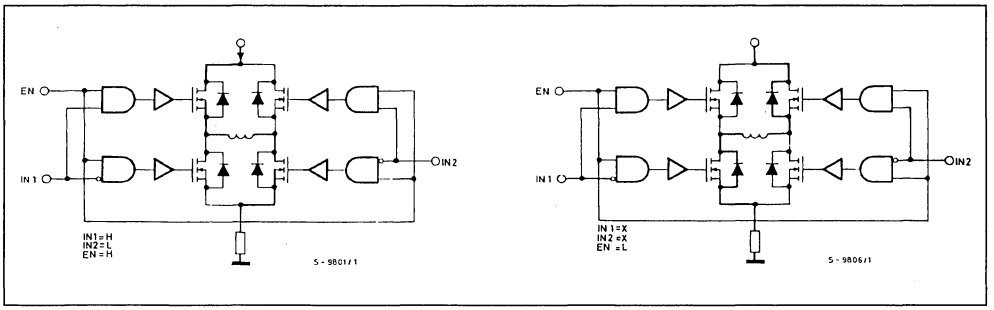
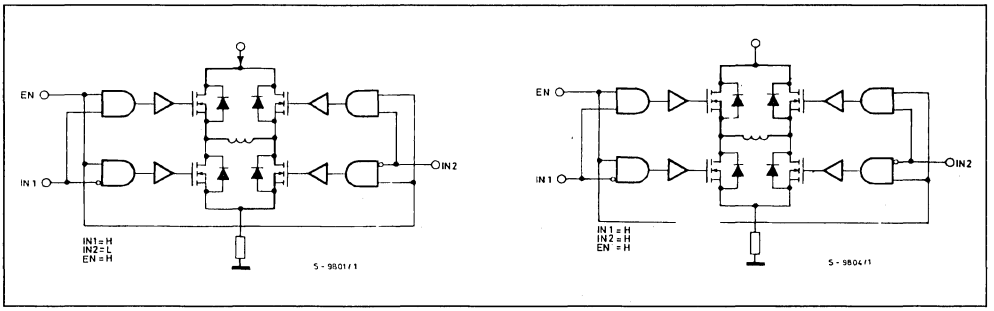


Figure 3c : One Phase Chopping.



DYNAMIC BEHAVIOUR

The driving of a DC motor will be analyzed dynamically during different motion phases. Fundamental to the working conditions of the IC is the type of load which the motor is driving. In fact if the load is frictional, the deceleration phase is not particularly serious for the IC since the load itself is supplying a braking torque. However, when the load is inertial it will appear to the IC to be a motor torque generator.

This could take the IC into critical operating conditions which can incur failure.

- Acceleration Phase : The current rises, delivering a torque which allows the motor to accelerate, up to the maximum velocity or till it is stabilized by the control loop. The type of load essentially determines the required current.

-Constant Velocity : In this case the required velocity is less than the maximum. The current is limited by chopping. This can be done by turning ON and OFF a MOS of the diagonal which is in conduction.

- Deceleration : When a DC motor must be decelerated, the type of load being driven becomes important. As previously stated, in the case of a frictional load, the load is essentially braking the motor. Thus, in general, it could be sufficient to cancel the motor torque by opening the bridge (i.e. disable the driver). In the case of an inertial load, however, the braking torque is provided by the driver. It is this situation that is of most concern. Since every change of direction involves a braking phase, a detailed analysis of this situation will be done.

ROTATION INVERSION

Initially the current flows in one direction as shown in figure 4. Figure 5 illustrates the situation when the diagonal is switched. The motor's inductance discharges the stored energy by fast recirculation through diodes D2 and D3.

Figure 4.

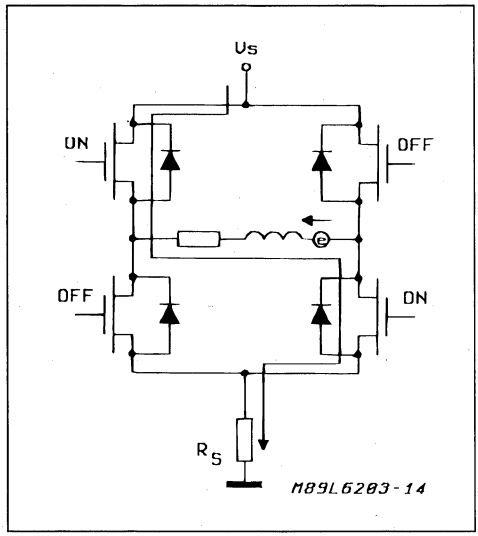
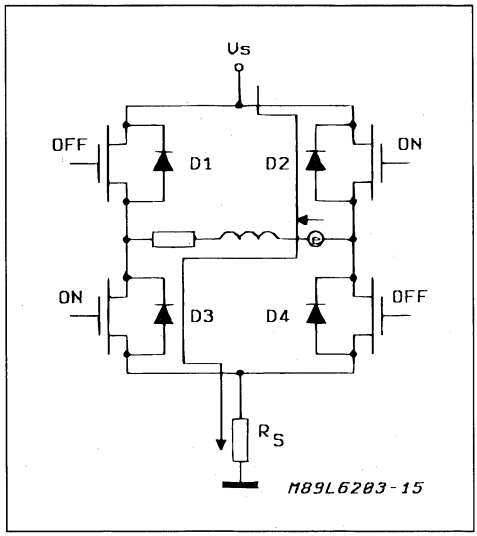


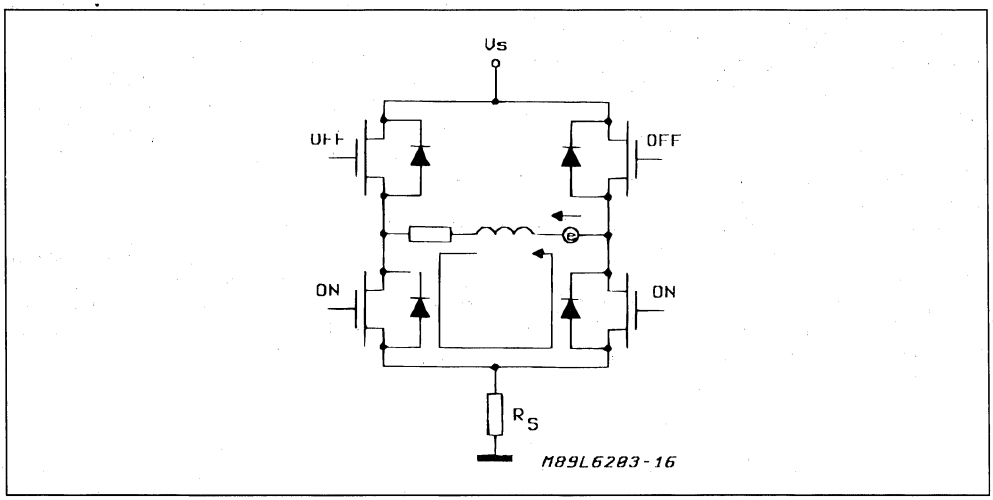
Figure 5.



The inertial load of the motor, which can be viewed as a flywheel, has stored energy during the phase prior to inverting the diagonal. This energy is returned to the motor providing a motor torque which keeps the motor rotating. Greater still is the flywheel's moment of inertia, greater than the motor torque that it provides to the motor. The discharge time is longer because the flywheel must discharge its energy. Also associated with the motor's rotation is the BEMF. Thus, in order to stop the motor a braking torque must be applied. This is generated when, following completion of slow recirculation, the current begins to flow in the opposite direction from the previous state.

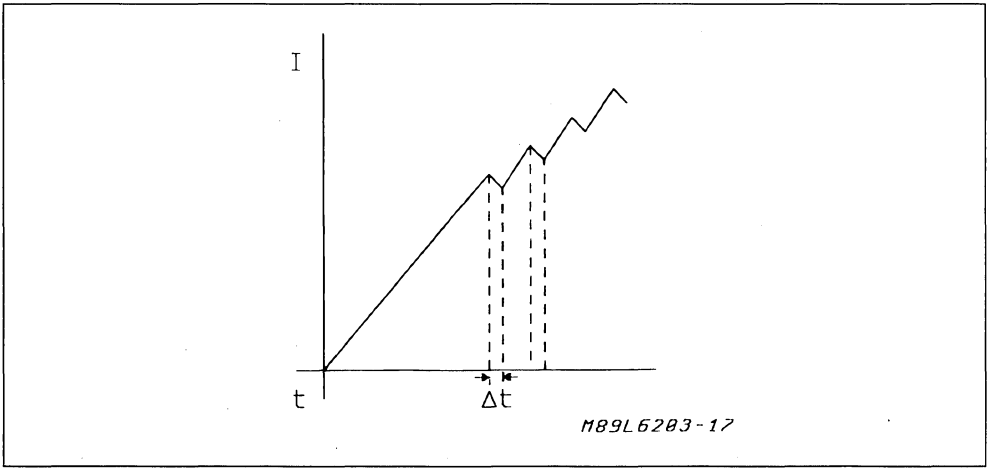
It is precisely at this point which effectively the braking phase begins. When the sense voltage rises to the preset level chopping is triggered. In figure 6 chopping results in slow recirculation (in practice the motor is short-circuited).

Figure 6.



As it can be seen, the BEMF is dropped across the relatively low resistances of the motor, the diode in line and the MOS that is ON. The sense resistor does not enter into this. If the motor's rotational velocity remains high the recirculation current could be very large, enough to damage the IC. Actually the current does not rise instantaneously to the steady state value of : I = V(ω)/(Rm + Rd + Rdson). Rather, the current follows the graph shown in figure 7. In fact, when chopping begins the sense current goes to zero, thus turning MOS M2 ON again. The motor current flows through the sense resistor, re-enabling the chopping. The cycle repeats in an iterative manner with a recirculation current that continues to rise.
Due to the inertial load and the BEMF it generates and the recirculation current as described above, the current in the sense resistor will be greater than the desired value set by Im = Vref/Rsense. When the current reaches the maximum level (see previous paragraph) the current will fall to the preset level controlled by the chopping, the inertial load having discharged its energy from the previous phase. This elevated current level is temporary, but can be damaging to the IC.

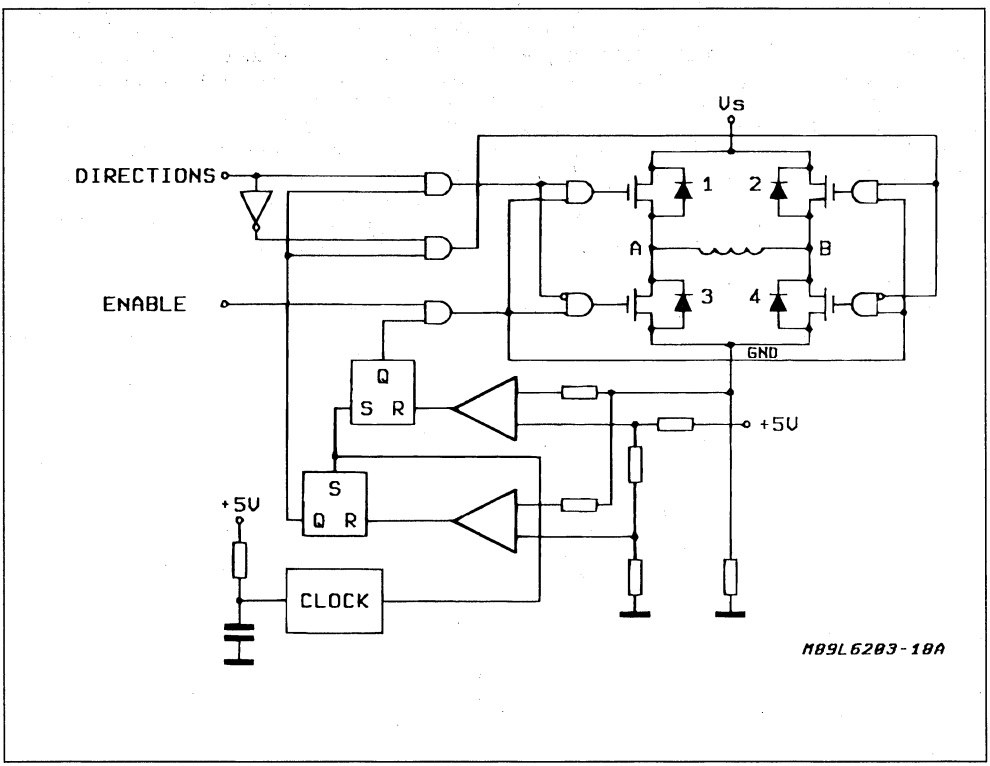
Figure 7.



[caption for figure 7]
I = recirculation current
delta t = time interval during which current flows through Rsense.

Braking the motor by short-circuiting it involves an accurate study of the mechanical system during the design phase. Knowing the value of the BEMF generated by the motor during braking, the motor resistance, and the equivalent resistance of the MOS and diode involved during recirculation it is possible to determine the recirculation current and if it is less than or greater than the maximum value that the IC can tolerate.

Figure 8.



If the recirculation current is too high it will be necessary to brake the motor with an alternative method. Using fast recirculation in combination with slow recirculation it is possible to brake the motor. Even if this is less than an efficient manner it avoids causing damage to the IC due to overcurrent. The basic circuit is shown in figure 8. Figure 9 is the application circuit which the Application Lab of Agrate, experimented with. This circuit uses an L6203 as the power driver. As seen in figure 8, as long as the recirculation current does not reach too high a value slow recirculation is used (one-phase chopping). Above a critical threshold slow recirculation is replaced with fast recirculation achieved by enable chopping. The slow and fast recirculations are triggered by two different reference voltages which determine the two current level thresholds. The higher current level for triggering fast recirculation is set little below the max current level available by the IC.

Figure 10 is the current waveform observed on the oscilloscope during few diagonal inversions. In this figure we can see the general trend of the motor current during three inversions of the rotation. A more detailed view of what really happens to the motor current is showed in fig. 11. Before the rotation inversion the motor is sinking its steady state current (about ±250mA in this application, the sign depending from the current flow direction). At the rotation inversion, first the current rises, as previous described, to the current level defined by Iref2. At this moment ENABLE chopping is activated starting the fast recirculation and the current level is clamped at this reference current level. When the motor has dissipated a sufficient rate of its inertial energy, the current falls down, first to the level defined by Iref1 (slow recirculation) for all that interval time that is required to dissipate the remaining inertial energy and then to its steady state working level.

Figure 9.

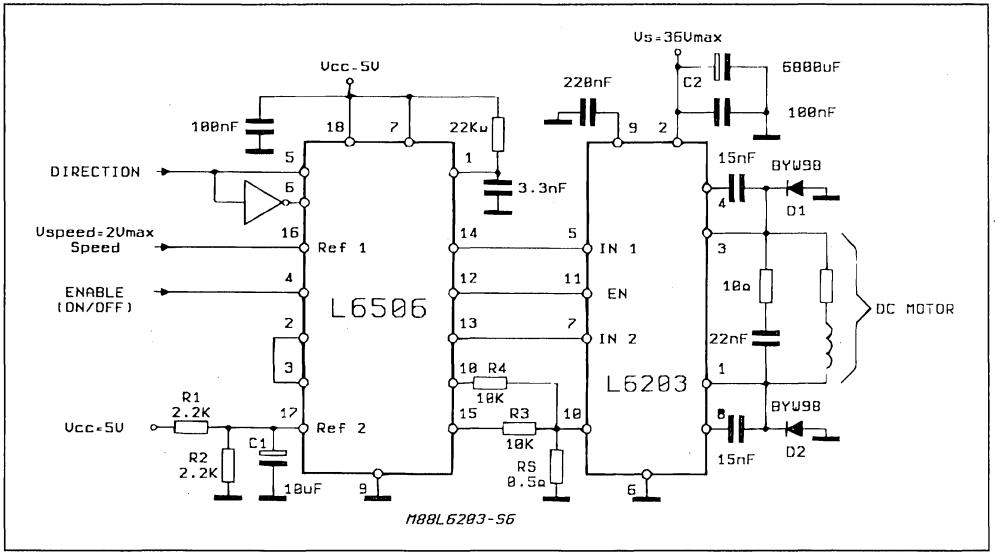
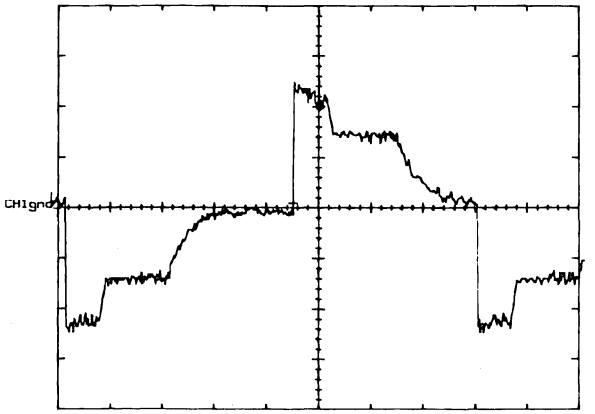


Figure 10.

VERT. 2A/DIV HOR.100ms/DIV

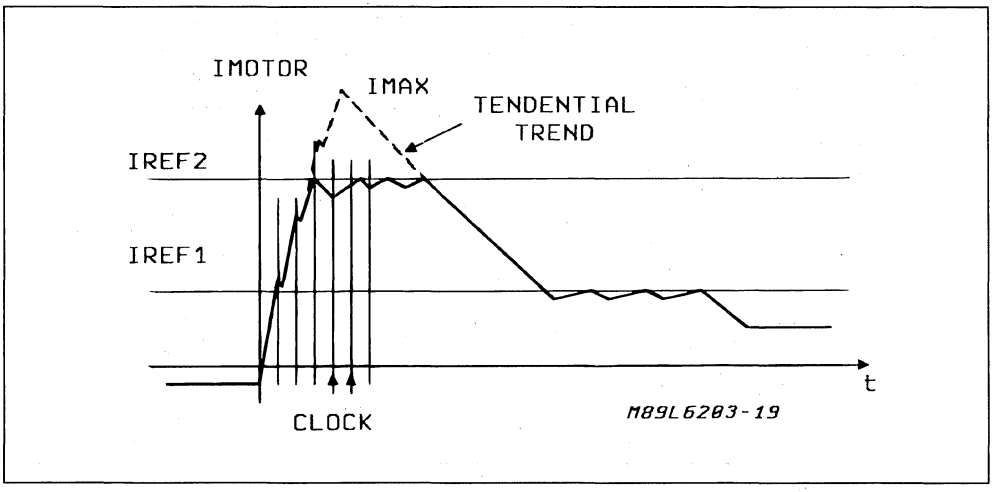


Three diagonal inversion of a unloaded DC motor

This scheme prevents damage to the IC due to overcurrent. However, failure due to overvoltage is still possible. An inertial load will return energy to the supply. If the power supply is the type which cannot sink current but can only source current, then the energy from the motor will load the power supply capacitor to a voltage above Vs. If the capacitor value is not large enough, during recirculation the capacitor voltage will rise rapidly. Meanwhile, the lower active diode is below ground during recirculation. There is a differential voltage between the overvoltage and the point below ground. If this exceeds the absolute maximum voltage of the IC, damage can occur. Overvoltage can be limited with an appropriate value of power supply capacitor. For the below ground condition of the lower diodes, the sources of the upper MOS can be clamped to ground with schotky diodes.

When Vs is relatively low it may be sufficient to control the differential voltage drop by just limiting the overvoltage with the power supply capacitor and not having to use the schottky diodes. The feasibility of this solution should nevertheless be verified experimentally in the specific application.

Figure 11.



APPLICATIONS OF MONOLITHIC BRIDGE DRIVERS

High power monolithic bridge drivers are an attractive replacement for discrete transistors and half bridges in applications such as DC motor and stepper motor driving. This application guide describes three such devices - the L293, L293E and L298 - and presents practical examples of their application.

The L293, L293E and L298 each contain four push-pull power drivers which can be used independently or, more commonly, as two full bridges. Each driver is controlled by a TTL-level logic input and each pair of drivers is equipped with an enable input which controls a whole bridge. All three devices feature a separate logic supply input so that the logic can be run on a lower supply voltage, reducing dissipation. This logic supply is internally regulated.

Additionally, the L293E and L298 are provided with external connections to the lower emitters of each bridge to allow the connection of current sense resistors. The L293E has separate emitter connections for each channel ; the L298 has two, one for each bridge.

Figure 1 shows the internal structure of the L293, L293E and L298. The L293 and L293E are represented as four push pull drivers while the internal schematic is given for the L298. Though they are drawn differently the L293E and L298 are identical in structure ; the L293 differs in that it does not have external emitter connections.

Figure 1 : The L293, L293E and L298 contain four push pull drivers. Each driver is controlled by a logic input and each pair (a bridge) is controlled by an enable input. Additionally, the L293E has external emitter connections for each driver and the L298 has emitter connections for each bridge.

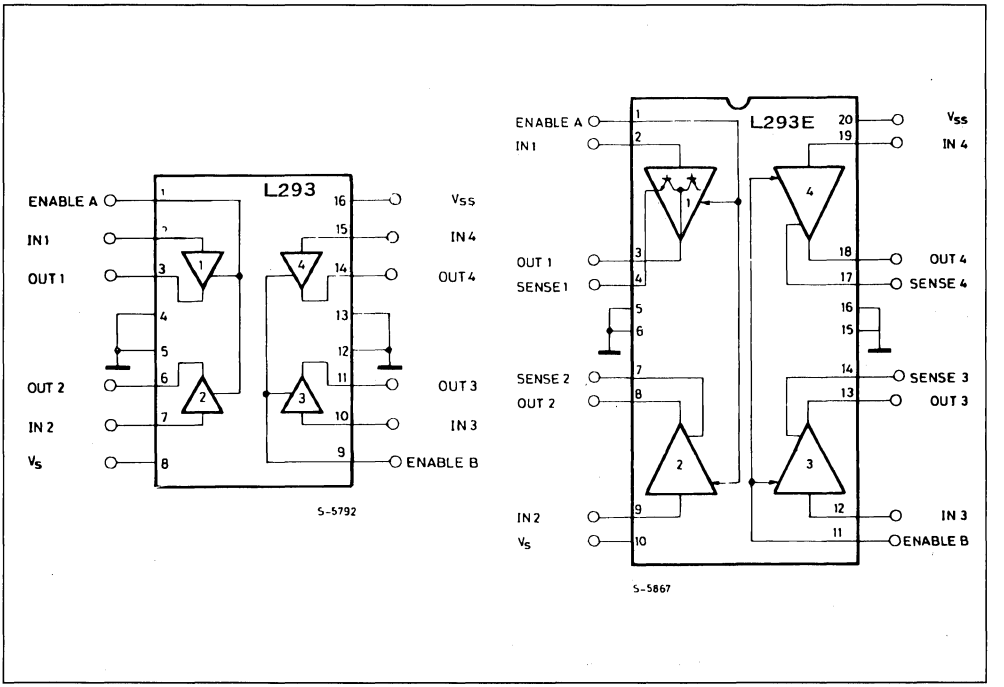
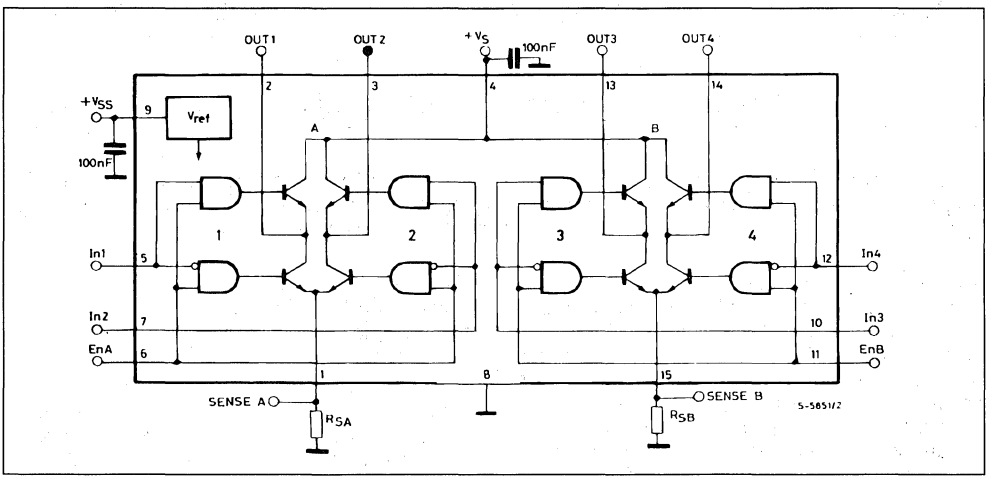


Figure 1 (continued).



The L293 is packaged in a 12 + 4 lead POWERDIP package (a 16-pin DIP with the four center leads used to conduct heat to the PC board copper) and handles 1A per channel (1.5 peak) at voltages up to 36 V.

The L293E, also rated at 1 A/36 V, is mounted in a 16 + 4 lead POWERDIP package. A 15-lead MULTIWATT plastic power package is used for the L298N which handles up to 2A per channel at voltages to 46 V.

All three devices includes on-chip thermal protection and feature high noise immunity. The high switching speed makes them particularly suitable for switch mode control.

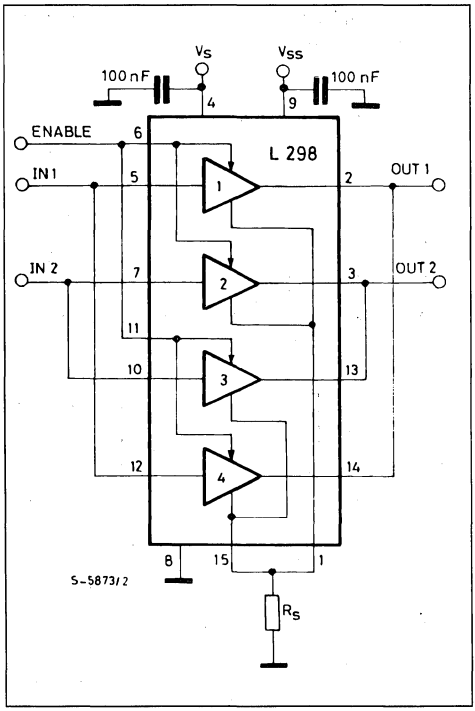
PARALLELING OUTPUTS

Higher output currents can be obtained by paralleling the outputs of both bridges. For example, the outputs of an L298N can be connected in parallel to make a single 3.5 A bridge. To ensure that the current is fairly divided between the bridges they must be connected as shown in figure 2. In other words, channel one should be paralleled with channel four and channel two paralleled with channel three. Apart from this rule the connection is very straightforward - the inputs, enables, outputs and emitters are simply connected together.

The outputs of an L293 or L293E can also be paralleled - in this case too channel 1 must be paralleled with channel 4 and channel 2 with channel 3.

But if two bridges are needed this is not a good idea because an L298N may be used. However, if only

Figure 2 : For higher currents outputs can be paralleled. Take care to parallel channel 1 with channel 4 and channel 2 with channel 3.



one bridge is required an L293 connected as a single bridge may be cheaper than an underutilized L298N.

SHORT CIRCUIT PROTECTION

L293 and L298N drivers can be damaged by short circuits from the output to ground or to the supply. Short circuits to ground are by far the most common and can be protected against by the circuit shown in figure 3.

When the output is short circuited the input is pulled low after a delay of roughly 10 µs, a period determined by the RC time constant. The upper transistor of the output stage is thus turned off, interrupting the short circuit current. When the short is removed the circuit recovers automatically. This is shown by the waveforms of figure 4.

Note that if the short circuit is removed while V1 is high the output stays low because the capacitor C is charged to V_{IH}. The system is reset by the falling edge of V1, which discharges C.

Figure 3 : This circuit protects a driver from output short circuits to ground.

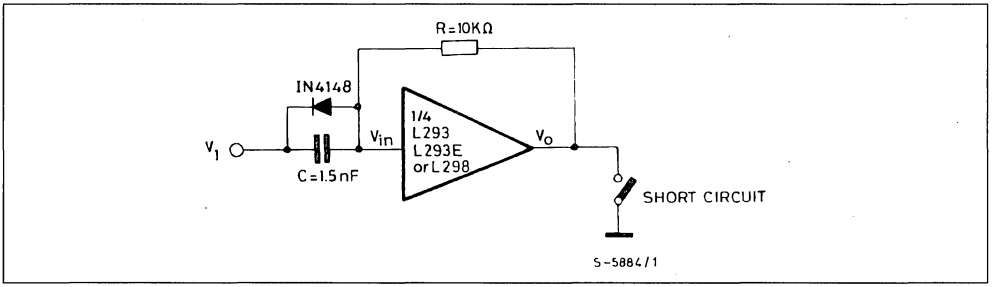
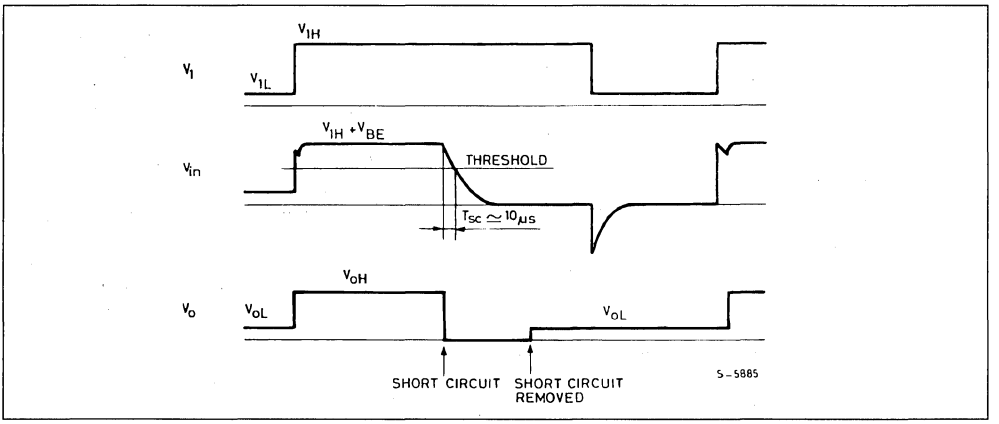


Figure 4 : Waveforms illustrating the short circuit protection provided by the circuit of fig. 3.



DC MOTOR DRIVING

In application where rotation is always in the same sense a single driver (half bridge) can be used to drive a small DC motor. The motor may be connected either to supply or to ground as shown in figure 5.

The only difference between these two alternatives is that the control logic is inverted - a useful fact to remember when minimising control logic.

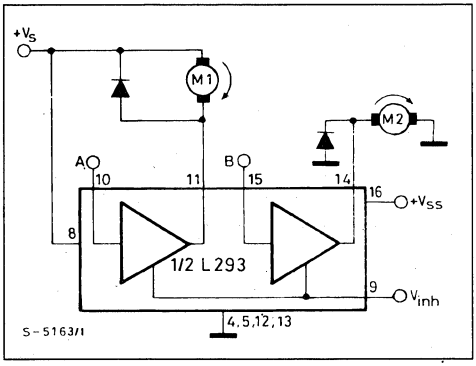
Each device can drive four motors connected in this way. The maximum motor current is 1A for the L293 and 2A for the L298N. However if several motors are driven continuously care should be taken to avoid exceeding the maximum power dissipation of the package.

Each motor in this configuration is controlled by its own logic input which gives two alternatives : run and fast stop (the motor shorted by one of the transistors).

The enable/inhibit inputs also allow a free running motor stop by turning off both transistors of the driver. Since these inputs are common to two channels (one bridge) this feature can only be used when both channels are disabled together.

A full bridge configuration is used to drive DC motors in both directions (figure 6). Using the logic inputs of the two channels the motor can be made to run clockwise, run anticlockwise or stop rapidly.

Figure 5 : For rotation in one direction DC motors are driven by one channel and can be connected to supply or ground.



V_{inh}	A	M1	B	M2
H	H	Fast Motor Stop	H	Run
H	L	Run	L	Fast Motor Stop
L	X	Free Running Motor Stop	X	Free Running Motor Stop

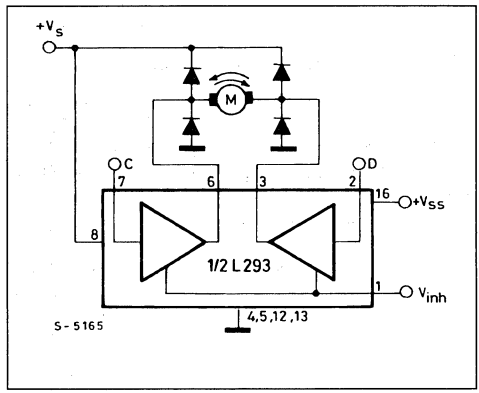
L = Low H = High X = Don't Care

Again, the enable/inhibit input is used for a free running stop - it turns off all four transistors of the bridge when low. A very rapid stop may be achieved by reversing the current, though this requires more careful design to stop the motor dead. In practice a tachometer dynamo and closed loop control are usually necessary. Like the previous circuit, this configuration is suitable for motors with currents up to 1A (L293/L293E) or 2A (L298N).

The motor speed in these examples can be controlled by switching the drivers with pulse width modulated squarewaves. This approach is particularly suitable for microcomputer control.

For undirectional drive with a single channel the

Figure 6 : A bridge is used for bidirectional drive of DC motors.



Inputs		Function
V_{inh} = H	C = H ; D = L	Turn Right
	C = L ; D = H	Turn Left
	C = D	Fast Motor Stop
V_{inh} = L	C = X ; D = X	Free Running Motor Stop

L = Low H = High X = Don't Care

PWM control signal can be applied to either the channel input or the appropriate enable input. In both cases the recirculation path is through the suppression diode and motor, giving a fairly slow decay. From a practical point of view it is preferable to control the channel input because the circuit response is faster. This is very convenient because each channel has an independent input.

The situation is different for bidirectional motors driven by a bridge. In this case the two alternatives have different effects. If the channel inputs are driven by the PWM signal, with suitable logic, the recirculation path is through a diode, the motor and a transistor (figure 7a), givind a slow decay. On the other hand, if the enable input is controlled the recirculation path is from ground to supply through two diodes and the winding. This path gives a faster decay (figure 7b).

Figure 8 shows a practical example of PWM motor speed control. This circuit includes the oscillator and modulator and allows independent regulation of the speeds of the two motors. The channel inputs are used to control the direction.

An interesting feature of this circuit is that it takes advantage of the threshold of the enable/inhibit input to economise on comparators. The TBA820M audio amplifier generates triangle waves, the DC

level of which is varied from 0 to 5 V by means of P1 and P2.

Since the switching threshold of the L293's enable/inhibit inputs is roughly 2 V the duty cycle of the output current (and hence the motor speed) is controlled by the setting of the potentiometer.

In this circuit the switching frequency is set by R1/C1 and the amplitude of the oscillator signal is set by the divider R2/R3.

Figure 7a : If the current shown by the solid line is interrupted by bringing A low the current recirculates round the dotted path. Decay is slow.

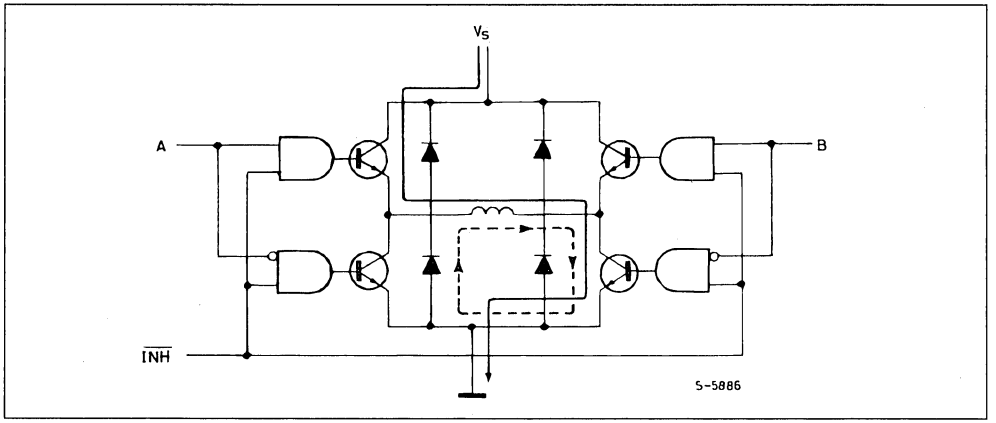


Figure 7b : If the enable input is brought low to interrupt the current indicated by the solid line the current recirculates from ground to V_S and the decay is faster.

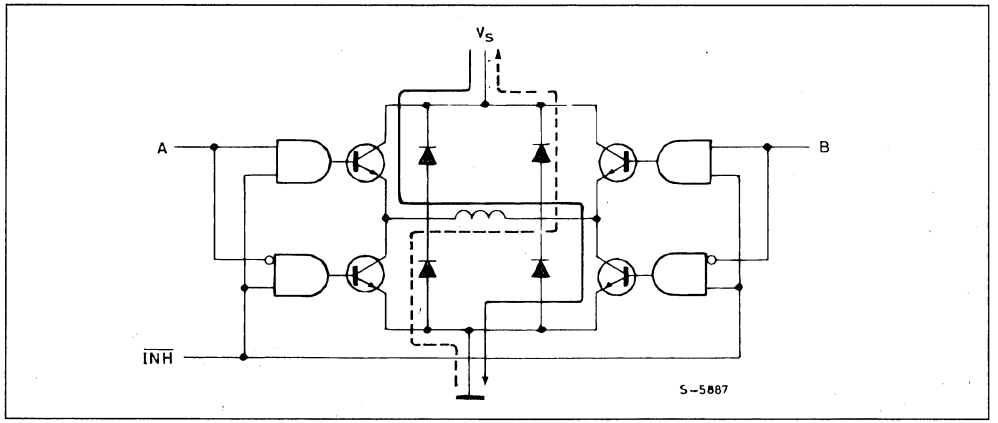
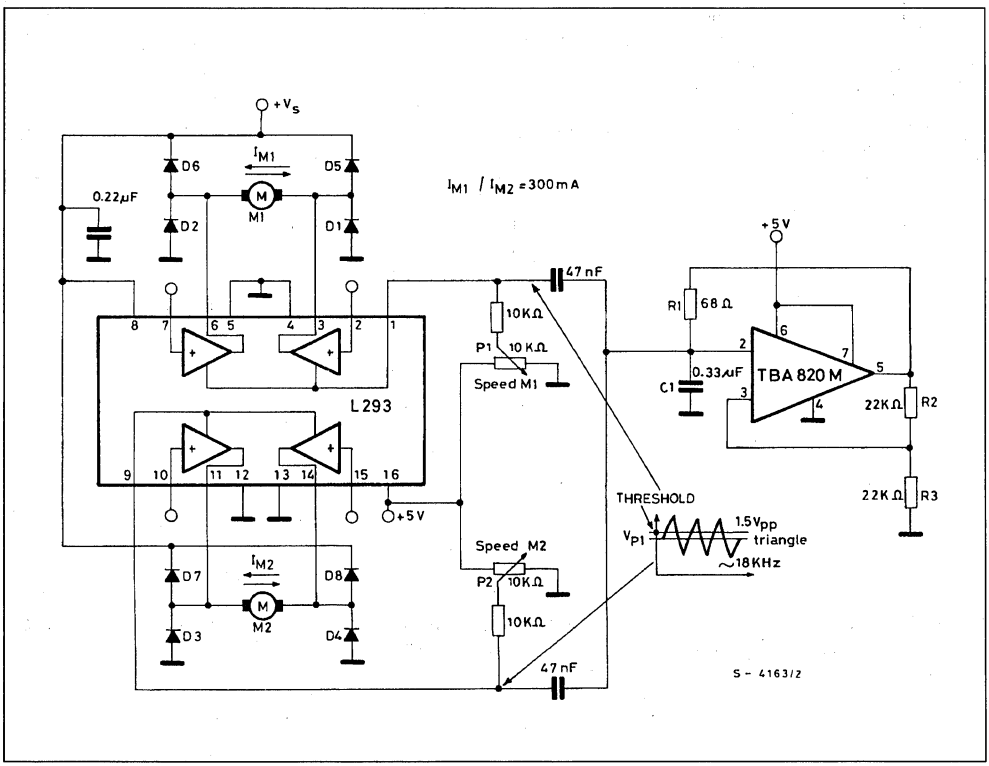


Figure 8 : This circuit illustrates PWM control of the motor speed. The speed of each motor is controlled independently.



STEPPER MOTOR DRIVING

Monolithic bridge drivers are extremely useful for stepper motor driving because they simplify the use of bipolar motors. This is an important point since a bipolar stepper motor costs less than an equivalent unipolar motor (it has fewer windings) and gives more torque per unit volume, other things being equal.

The basic configuration for bipolar stepper motor driving is shown in figure 9. In this example it is assumed that a suitable translator (phase sequence generator) is connected to the four channel inputs.

Either an L293 or an L298N can be used in this circuit ; an L293E would be wasted compared to an L293 because load current regulation, and hence the sense resistor connection, is not used.

But load current requlation is highly desirable to exploit the performance characteristics of the motor. Using an L293E or L298N this can be implemented by adding an LM339 quad comparator as shown in figure 10.

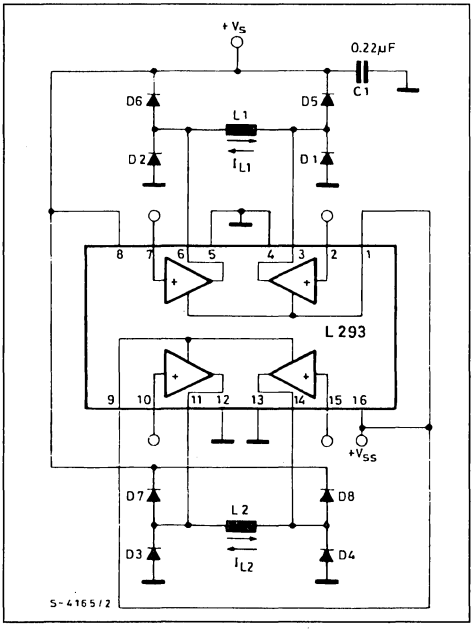
This is another circuit that requires an external translator but it provides independent PWM chopper regulation of the current in each winding.

Looking at motor phase one, the comparator output is initially high, enabling the bridge through pin 1.

The current in the motor winding rises until the voltage across the sensing resistor R2 produces a voltage at the inverting input of the comparator equal to the voltage on the non-inverting input (370 mV). This value is produced by the divider R10/R11 and by the hysteresis determined by R6 and R8.

At this point the comparator switches, disabling the bridge. The current in the winding recirculates through D5 and D6 until the voltage across R2 falls below the lower threshold of the comparator. The comparator then switches again and the cycle repeats.

Figure 9 : A single device can be used to drive a two phase bipolar stepper motor.



The peak current in each winding is determined by V_{ref} (in this case it is 0.5 A) and the switching rate - and hence the average current - depends on the hysteresis of the comparator and R4C4. With the component values shown the switching frequency is roughly 20 kHz.

The figure 10 circuit uses only half of the LM339 quad comparator. With the adition of a few extra passive components we can take advantage of the spare comparators to implement short circuit protection. Figure 11 shows how this is done.

As before, comparators 1 and 2 regulate the current in the windings but in this case the connection is different because the inhibit/enable inputs are used for the short circuit protection. The PWM choppers act on the channel inputs through the four clamp diodes D9, D10, D11 and D12. This is a simple trick which allows us to use the channel inputs both for the step sequencing and the choppers.

Comparators 3 and 4 realize the short circuit protection function. Again looking at phase one, comparator 3 operates as a flip flop. Its output is connected to the bridge enable inputs (pins 1 and 11) and is normally high, enabling the drivers. If the output current (sensed by RS1) reaches double the nominal value the comparator CP3 switches, inhibiting the two bridges.

The comparator remains in this state until the V_{SS} supply (5 V) is interrupted. The outputs of comparators 3 and 4 are ORed together so that a short circuit on one phase disables both bridges.

For this circuit V_A should be less than 300 mV (V_A is the voltage on the + input of CP1). From the value chosen for V_A and the desired phase current the sense resistor RS1 (and RS2) is chosen. The current ripple should be at least 30 mA to avoid spurious triggering of CP1 and CP2.

The component values indicated are for a motor with a resistance of 37 Ω/phase, inductance of 80 mH/phase and a current of 280 mA/phase. V_{ref} is 243 mV giving V_A = 274 mV when the output is high and 243 mV when the output is low. Since RS1 = 1 Ω the current is the winding reaches 274 mA peak and has a ripple of roughly 30 mA. The switching frequency depends on the hysteresis of the comparators and the motor characteristics. For this example the frequency is about 15 kHz.

Stepper motor drive circuits can be simplified using the L297 stepper motor controller which contains a translator to generate the phase sequences plus a dual PWM chopper to regulate the phase currents.

The L297 connects directly to the L293E or L298N as shown in figure 12. This example drives a bipolar stepper motor with winding currents up to 2.5 A. For lower currents an L293E is used and more powerful motors can be driven by two L298N's with paralleled bridges, giving up to 3.5 A.

In this configuration the motor is controlled through the L297. A step clock moves the motor one increment, the CW/CCW input controls the direction and the HALF/FULL input selects half step or normal operation. The input V_{ref} is connected to a suitable voltage reference and sets the peak winding current in the motor. The choppers in the L297 can operate on the phase lines or the inhibit lines, depending on the state of the logic input called CONTROL.

For a more detailed description of the L297 see "Introducing the L297 Stepper Motor Controller".

Figure 10 : Two comparators provide chopper current regulation in this bipolar stepper motor drive circuit.

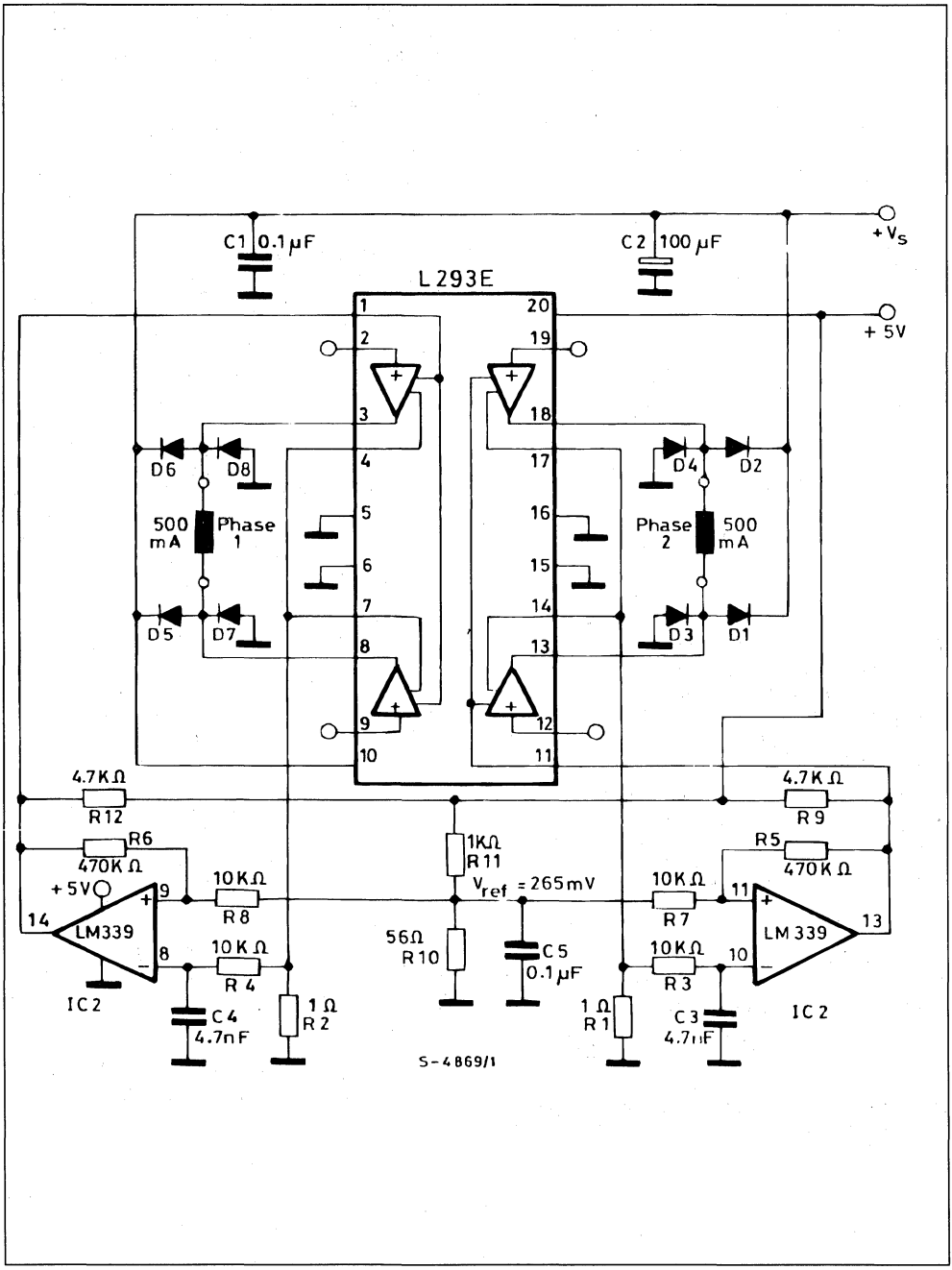


Figure 11 : With a quad comparator both current regulation and short circuit protection can be obtained.

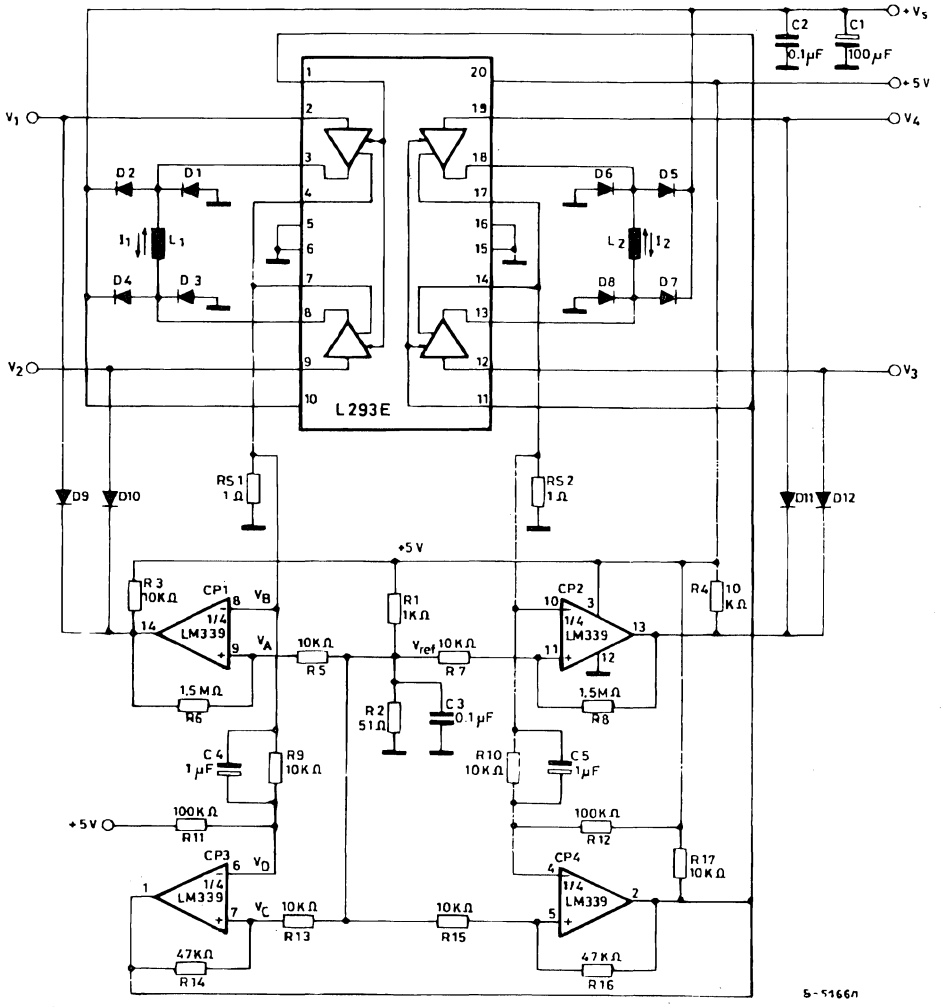
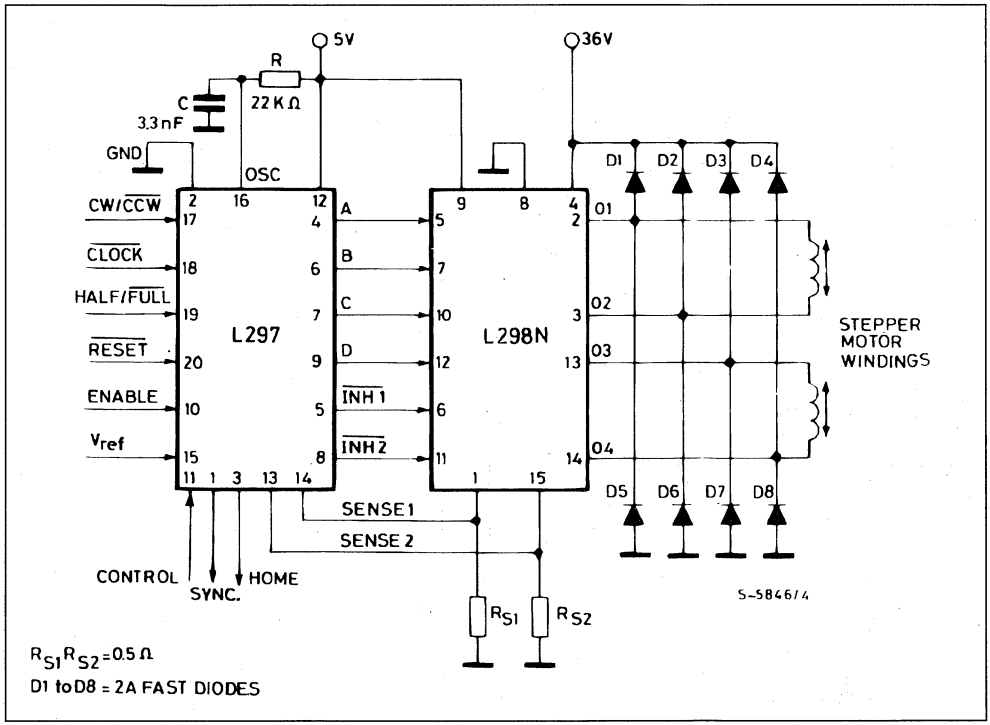


Figure 12 : An L297 stepper motor controller and a L298N driver together from a complete microprocessor-to-stepper motor interface. This circuit drives bipolar stepper motors with winding currents up to 2 A.



SPEED CONTROL OF DC MOTORS WITH THE L292 SWITCH–MODE DRIVER

Power dissipation in DC motor drive systems can be reduced considerably with an L292 switchmode driver. This application guide describes two speed control systems based on this device ; one voltage controlled and one controlled by a 6-bit binary word. Both examples are designed for 60 W motors equipped with tacho dynamos.

The L292 is a monolithic power IC which functions effectively as a power transconductance amplifier. It delivers a load current proportional to an input voltage, handling up to 2 A at 18-36 V with a bridge output stage. Completely self-contained, it incorporates internal switchmode circuitry and all the active components to form a current feedback loop.

The L292 is designed primarily for use with an L290 and L291 in DC motor servopositioning applications. However, the L292 can be useful in a wide range of applications as the two examples here show. The first is a simple tachometer feedback circuit, the speed of which is controlled by a DC voltage ; direction is controlled by the polarity of this voltage. The second circuit is controlled digitally and includes an L291 D/A converter.

SYSTEM WITH DC CONTROL

In this system the control quantity is a dc voltage variable between

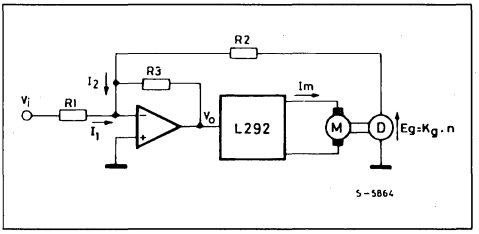
$$+ V_{iM} \text{ and } - V_{iM}$$

Since the quantity under control is the speed of the motor, it is required that it varies linearly in function of the control voltage.

A simplified circuit diagram of the system is shown in fig. 1.

The current I_1, proportional to the set voltage V_i, and the current I_2, proportional to the speed of the motor, are fed to the sum point of the error amplifier. Assuming that the motor does not drain current, the system is in a steady-state condition whenever $I_1 = -I_2$; as a matter of fact, in this case the output from the error amplifier V_o is 0V. During transients, the voltage V_o will assume a value $V_o = -R3\,(I_1 + I_2)$ and consequently, since the L292 integrated circuit operates as a transconductance (G_m), a mean current $I_m = G_m \cdot V_o$ will flow in the motor determining an acceleration proportional to it.

Figure 1 : Simplified Circuit Diagram of DC control System.



CALCULATION OF R1, R2, R3

Let us call:

V_{iM} the maximum control voltage value

n_M the maximum speed allowed for the motor

K_g voltage constant of the dynamo

By imposing that the balance condition be met in correspondance to the maximum rotation speed the following equation is obtained :

$$I_1 = -I_2 \; ; \quad \frac{V_{iM}}{R1} = -\frac{K_g \cdot n_M}{R2}$$

Since R2 is the impedance which the tachometer dynamo is loaded on to and its value is recommended by the manufacturer, it is possible from the previous relationship to determine the value of R1.

Resistor R3 determines the system gain. It's best to keep the gain as high as possible (and consequently R3 as high as possible) to obtain a high response speed of the system, even of for small variations in the control voltage. On the other hand, an excessive gain would cause excessive overshoot around the balance conditions at the end of transients. Consequently, a trade-off must be made between the two opposing requirements in selecting the final gain.

The value for R3 should be theoretically determined by studying the transfer function, by knowing the electrical and mechanical constants of the motor as well as the load applied to it.

A complete diagram of the circuit actually realized is shown in fig. 2, while fig. 3, shows the characteristic n = f (V_i) obtained.

Resistor R2 drawn in the simplified circuit diagram has been split here in two parts and, in addition, a capacitor has been interposed to ground to filter the signal coming from the tachometer dynamo.

The curve n. 1 in fig. 3 refers to the operation of the motor in no-load condition, with a current drain of 200 mA ; the curve n. 2 refers to a motor loaded so as to drain a current of 1A. By disregarding the discontinuity around the origin, it can be noted that the characteristics are linear over the whole control voltage range.

By analyzing the curves around the origin, it can be noted that the motor stands still as long as the input signal does not exceed a certain threshold level, which is as much higher as the current drained by the motor is higher.

Let us call G_m the transconductance of L292, and I the starting current of the motor ; the voltage which must be available at the input of L292 in order that the motor starts turning is :

$$V_o = \frac{I}{G_m} \text{ with } G_m = 220 \ \frac{mA}{V} \text{ (typical value)}$$

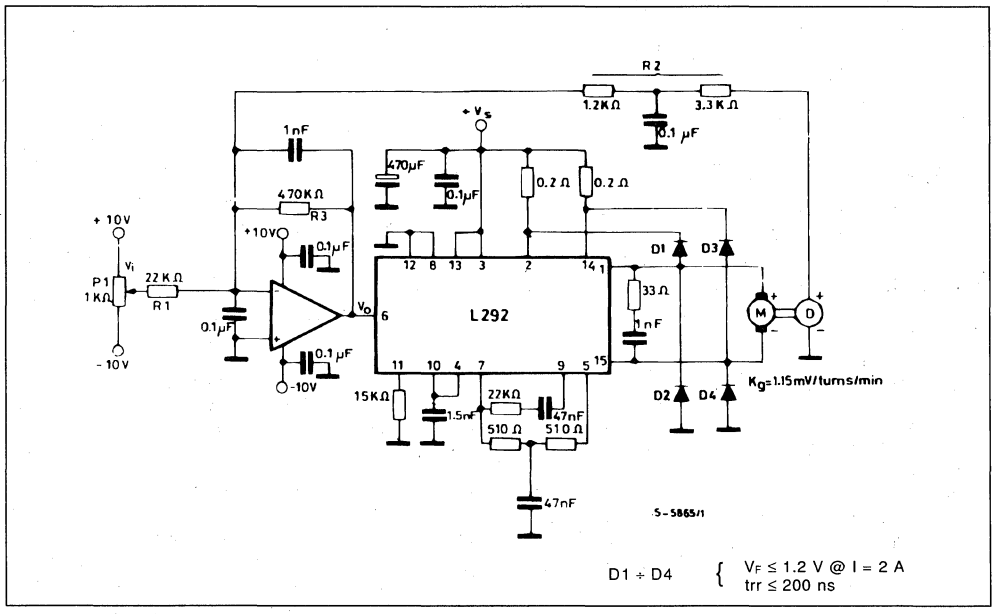
The corresponding control voltage will be :

$$V_i = V_o \cdot \frac{R1}{R3} = \frac{I}{G_m} \cdot \frac{R1}{R3}$$

and it is as much lower as the gain of the error amplifier is higher.

The presence of a control voltage interval in which the motor stands still, can be useful when it is required that, for a certain position of potentiometer P1 (see fig. 2), the motor speed be zero. An other method to hold the motor still is to use the inhibits of L292, for instance by grounding pin 13.

Figure 2 : Complete Circuit Diagram.



It can be noted from fig. 3 that, by keeping the control voltage V_i constant, the speed varies according to the motor current drain.

Let us call ΔI the current variation ; the voltage variation required at the input of L292 is

$$\Delta V_o = \frac{\Delta I}{G_m}$$

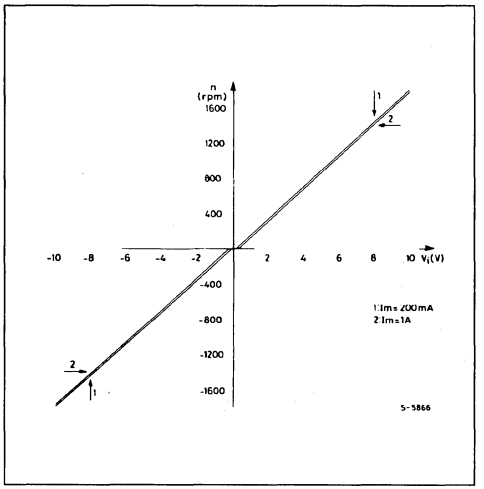
since the control voltage is constant, to generate this ΔV_o it is necessary that the rotation speed be varied by a quantity Δn such as to have :

$$K_g \cdot \Delta n \cdot \frac{R3}{R2} = \Delta V_o = \frac{\Delta I}{G_m}$$

$$\Delta n = \frac{\Delta I}{G_m K_g} \cdot \frac{R2}{R3}$$

(ΔI shall be taken with its sign)

Figure 3 : Output Characteristics of the Circuit in fig. 2.



In this case too, the variation Δn is as much lower as the error amplifier gain is higher. With the circuit shown in fig. 2 Δn is approximately 30 turns/min. with ΔI = 800 mA, Δn = 0.037 turns/mA.min approx.

It is possible to adopt a circuit which prevents the variation in the number of turns in function of motor current. The problem is to "sense" the current flowing through the motor and to send a current proportional to it to the sum point of the error amplifier. The complete circuit which includes, beside the voltage feed-back loop, also a current feed-back loop, is illustrated in fig. 4.

In the integrated circuit L292, a current proportional to the mean current drained by the motor flows between pin 5 and pin 7.

An operational amplifier amplifies the voltage drop provoked by this current across a 510 Ω resistor and sends a current to the sum point which is consequently proportional to the mean current in the motor, the value of which can be made vary by acting on potentiometer P2. By properly adjusting P2, a condition can be achieved in which the speed does not change when the current drained by the motor varies.

The discontinuity around the origin, which was present in the previous circuit (fig. 2), is practically negligible in the circuit shown in fig. 4.

The characteristic n = f (V_i) relevant to the circuit of fig. 4 is shown in fig. 5, and this characteristic does not substantially change over the whole range of currents allowed by the L292 (up to 2A).

In the circuit described above if the motor stall condition is requested. It is preferable to act on the inhibits of the integrated circuit L292, for instance by grounding pin 13, instead of adjusting potentiometer P1 : as a matter of fact, the exact position of this potentiometer is difficult to obtain, since the characteristic crosses the axis V_i in one only point (this mean that n is only 0 for a very narrow interval of V_i).

Figure 4 : Complete Circuit with Current Feedback.

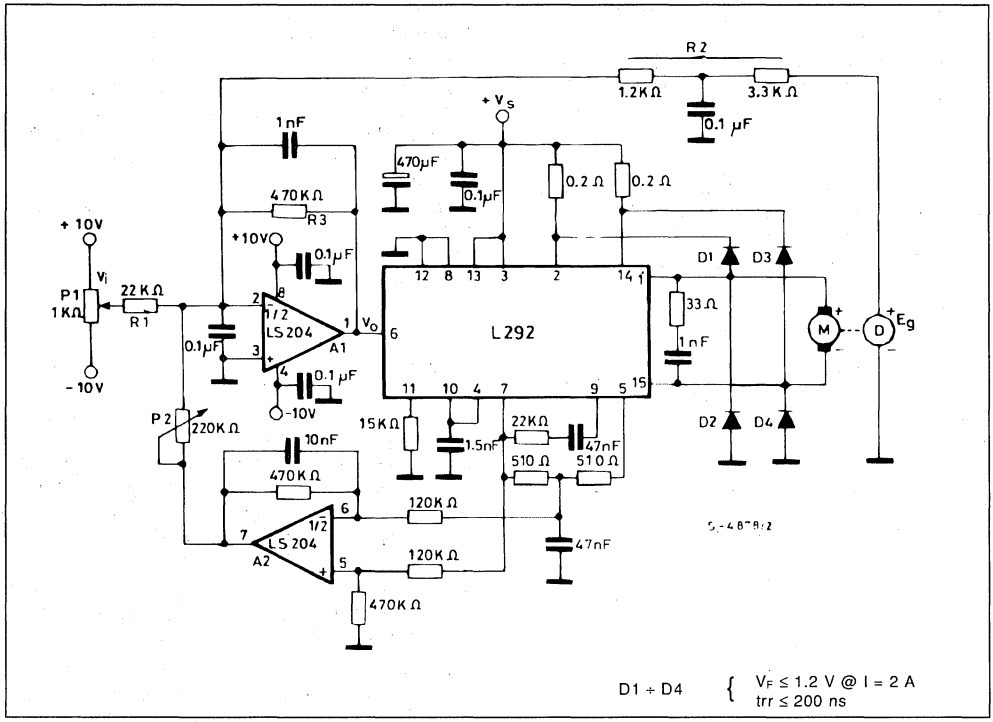
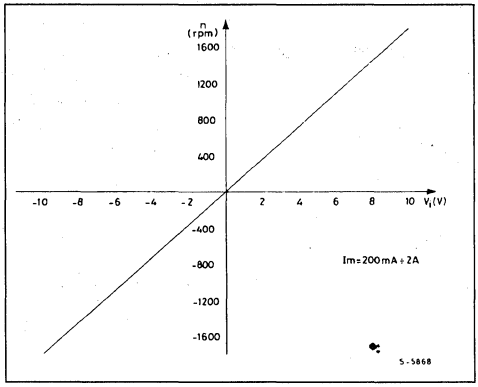


Figure 5 : Output Characteristics of the Circuit in fig. 4.

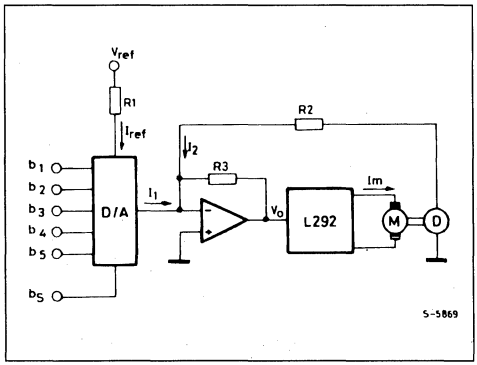


SYSTEM WITH DIGITAL CONTROL

In this system the speed information is given to the circuit by a binary code made up of 5 information bits plus one sign bit, which determines whether the movement shall the clockwise or counter-clockwise. For the circuit implementation, the integrated circuits L291 (which includes a D/A converter and two operational amplifiers) and L292 are used.

A simplified circuit diagram is shown in fig. 6.

Figure 6 : Simplified Circuit Diagram (digital control).



The current value I_1 depends on the value of I_{ref} and on the value of inputs b_1 through b_5, where its sign depends on the b_S input.

The maximum value for I_1, which is obtained whenever inputs b_1 through b_5 are low, is :

$$I_{1\,max} = I_{ref}\,\frac{31}{16} = \frac{V_{ref}}{R1}\cdot\frac{31}{16}$$

In order to have the system in a steady state condition (no current drained by the motor), it must be :

$$I_1 = -\,I_2$$

By imposing the balance condition at the maximum speed, one obtains : $I_{1\,max} = -\,I_{2\,max}$

$$\frac{V_{ref}}{R1}\cdot\frac{31}{16} = \frac{K_g\,n_M}{R2}$$

where

K_g = dynamo's voltage constant

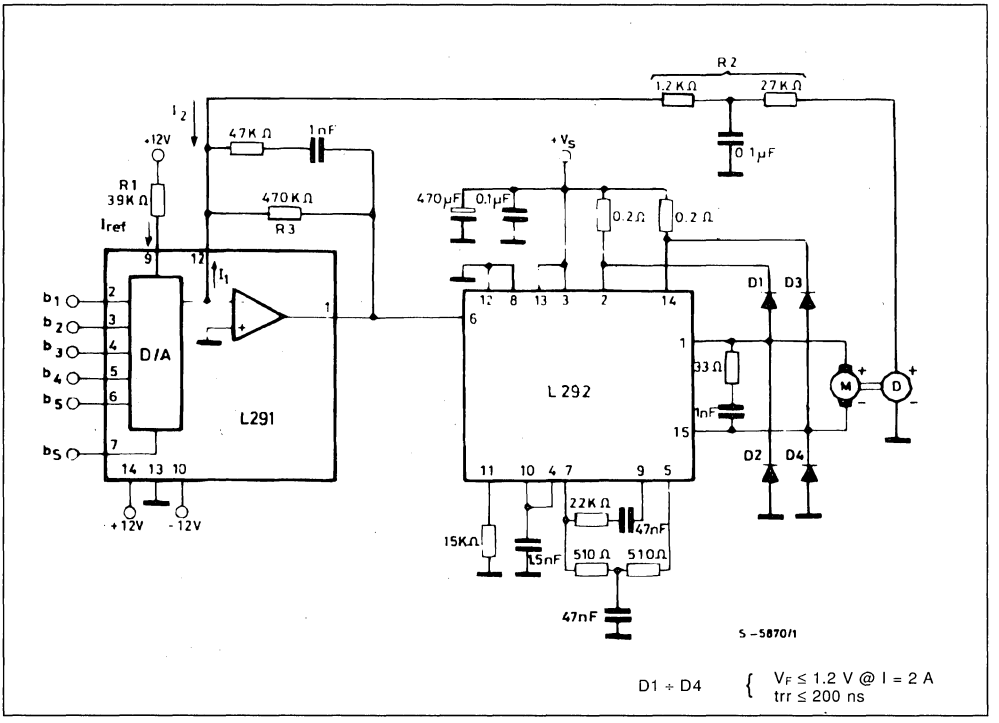
n_M = maximum speed preset for the motor.

The current I_{ref}, and consequently the ratio $V_{ref}/R1$, must lie within a certain range imposed by the D/A converter actually used.

In our case, this range is 0.3 to 1 mA. The values of R1 and R2 can be determined from the previous relationship. The same considerations made in the description of the DC control system apply for the selection of R3.

A complete diagram of the circuit implemented is indicated in fig. 7, while the input versus output characteristics is shown in fig. 8.

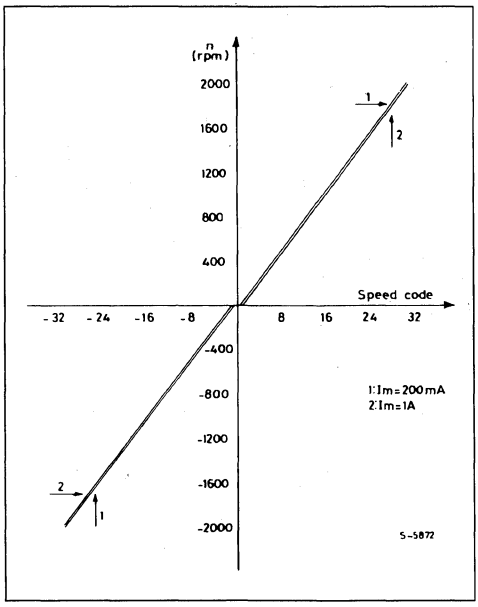
Figure 7 : Complete Circuit Diagram.



In the graph of fig. 8 the rotation speed of the motor is represented on ordinates, while the decimal speed code, corresponding to the binary code applied to inputs b_1 through b_5, is represented on abscissae.

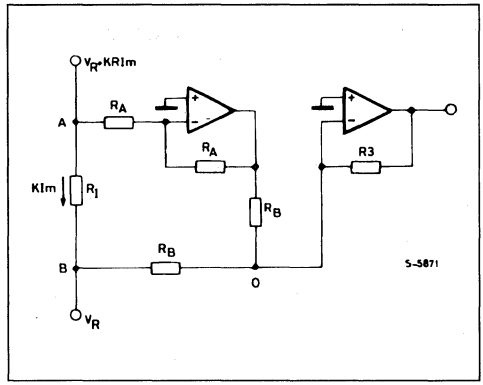
The abscissa 1 corresponds to the minimum speed code, i.e. input b_1 low and remaining inputs high, since the least significant input is b_1 and the active status of inputs is low. The abscissa 31 corresponds to the maximum speed code, i.e. all inputs b_1 through b_5 low. The negative abscissae have been obtained by changing the status of the b_5 input. The graph in fig. 8 should have been made up of a number of dots ; these dots have been joined together with an ininterrupted line for convenience. This graph has the same features as the graph in fig. 3, i.e. the curve features a discontinuity around the origin, and it lowers as long as the motor current drain increases. In this case too, the circuit in fig. 7 can be modified in order to prevent that the speed vary in function of the motor load, by adding a current loop in the control circuit, by using the remaining operational amplifier available in the integrated circuit L291.

Figure 8 : Output Characteristic of the Circuit in fig. 7.



Since this amplifier has only the inverting input available, while the non-inverting input is grounded, a circuit arrangement as schematically shown in fig. 9 has been adopted in order to have an output signal referred to ground, given an input signal referred to a reference voltage (in L292) of approximately 8 V.

Figure 9 : Translator Circuit.



Resistors R_A and R_B must be high-precision resistors in order to have output 0 with no I_m current present. In the practical implementation, resitors with an accuracy of 5 % are used and the ends of a potentiometer are interposed between resitors R_B and the output to the sum point of the error amplifier is made through the cursor. The gain of this current loop is propotional to the ratio $R3/R_B$. A complete circuit diagram is shown in fig. 10.

Since, for reasons of gain, resistor R_B must be 27 kΩ and, if connected to pin 7 of L292, should have subtracted too much current by thus affecting the correct operation of L292, it has been connected to pin 11, having the same potential as pin 7. Consequently, the resistance value between pin 11 and ground has been modified, in order to maintain the switching frequency of L292 unchanged. In order to have a correct adjustment of potentiometer P1, it is enough to set the 0 speed code (b_1 through b_5 high) and turn the cursor until the motor stops.

The input versus output characteristic obtained with the circuit of fig. 10 is indicated in fig. 11.

Figure 10 : Complete Circuit with Current Feedback.

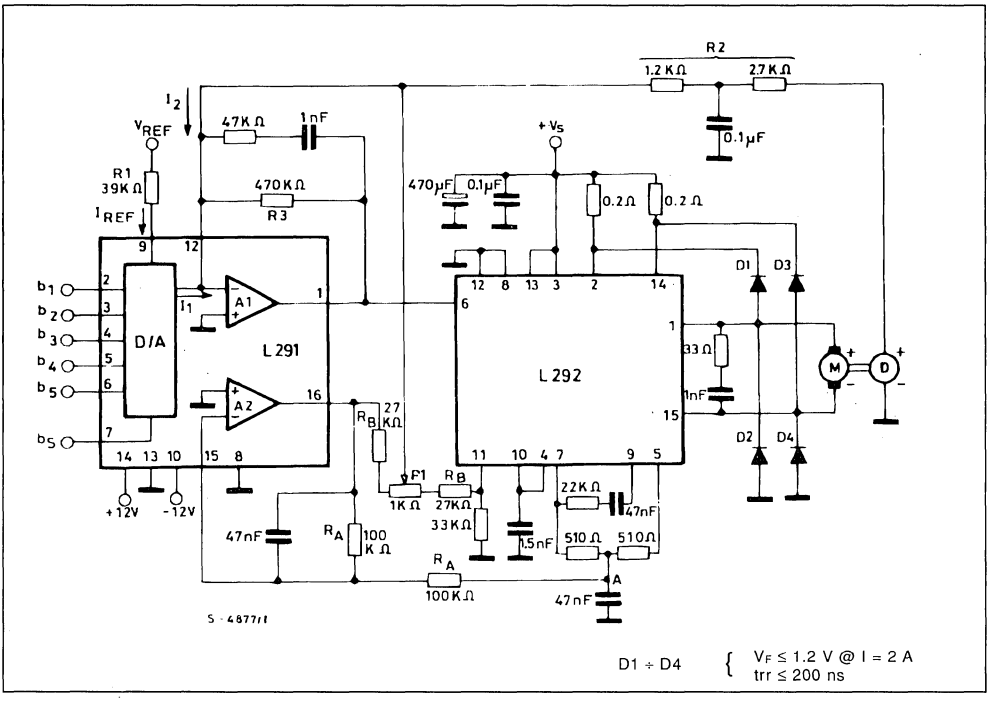
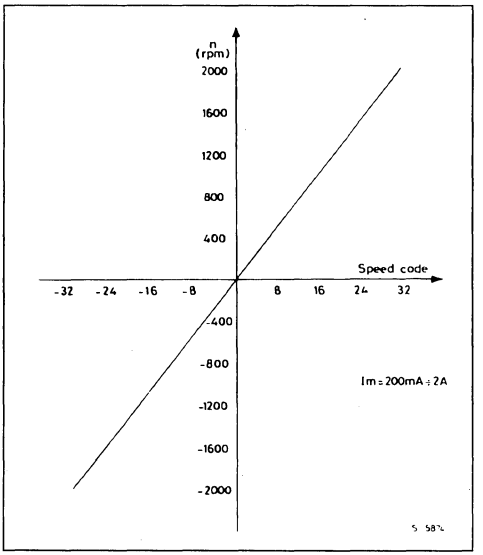


Figure 11 : Output Characteristic of the Circuit in fig. 10.



RESPONSE TO INPUT STEP

Measurements have been taken on the circuits described in the previous paragraphs, in order to analyze how the motor speed varies when a step variation is imposed to the input.

For the system DC control, the control voltage has been changed from 0 to the maximum value V_{iM} and down to 0 again. For the digital system the speed code has been changed from 0 (b_1 through b_5 high) to the maximum value (b_1 through b_5 low) and down to 0 again. When the control quantity changes from 0 to the maximum value, the output voltage of the error amplifier (V_o, fig. 1 and fig. 6) assumes its maximum value, since the feed-back signal coming from the tachometer dynamo initially 0. In these conditions, L292 supplies the motor with the maximum current (2A) and maintains it until the motor speed is sufficiently close to the maximum value.

Since the motor is powered from a constant current, it moves with a constant current, it moves with a constant acceleration and consequently its speed grows linearly from 0 up to the maximum value over the time interval t_a. The time needed for the motor to reach the maximum speed also depends, besides

the current, on the electrical and mechanical characteristics of the motor and on the moment of inertial of the load applied to the motor. When the control quantity changes from the maximum value to 0, the output of the error amplifier V_o assumes the maximum value, but with an opposite sign with respect to the previous case, and the current flowing in the motor is also reversed and tends to brake it, by making the speed linearly decrease from the maximum value down to 0 over the time period t_f. The no-load characteristics, relevant to the motor used for the previous tests, are shown in fig. 12. The times t_a and t_f are not equal to each other, which circumstance is basically due to the frictions which, during the acceleration phase, oppose increase of speed, while during the deceleration phase they contribute to make the speed decrease. As a matter of fact, from the movement equation :

$$J\ddot{\Theta} + D\dot{\Theta} + T_f = K_T I_M$$

where :

J = System moment of inertia

D = Coefficient of viscous friction

T_f = Braking couple

K_t = Motor constant

$\dot{\Theta}$ = Angular speed

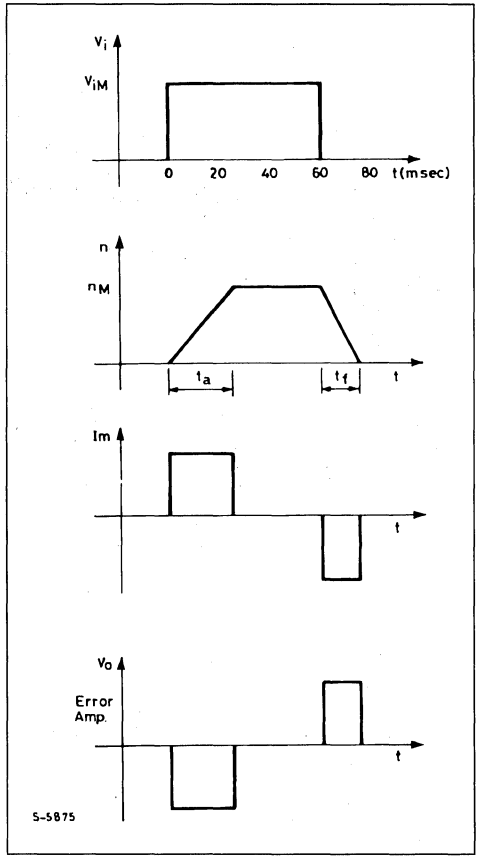
$\ddot{\Theta}$ = Angular acceleration

and by disregarding the term $D\dot{\Theta}$, one obtains :

$$\ddot{\Theta} = \frac{KT \cdot I_M - T_f}{J}$$

where from it can be seen that $|\ddot{\Theta}|$ is greater if I_M is negative.

Figure 12 : Pulse Response.

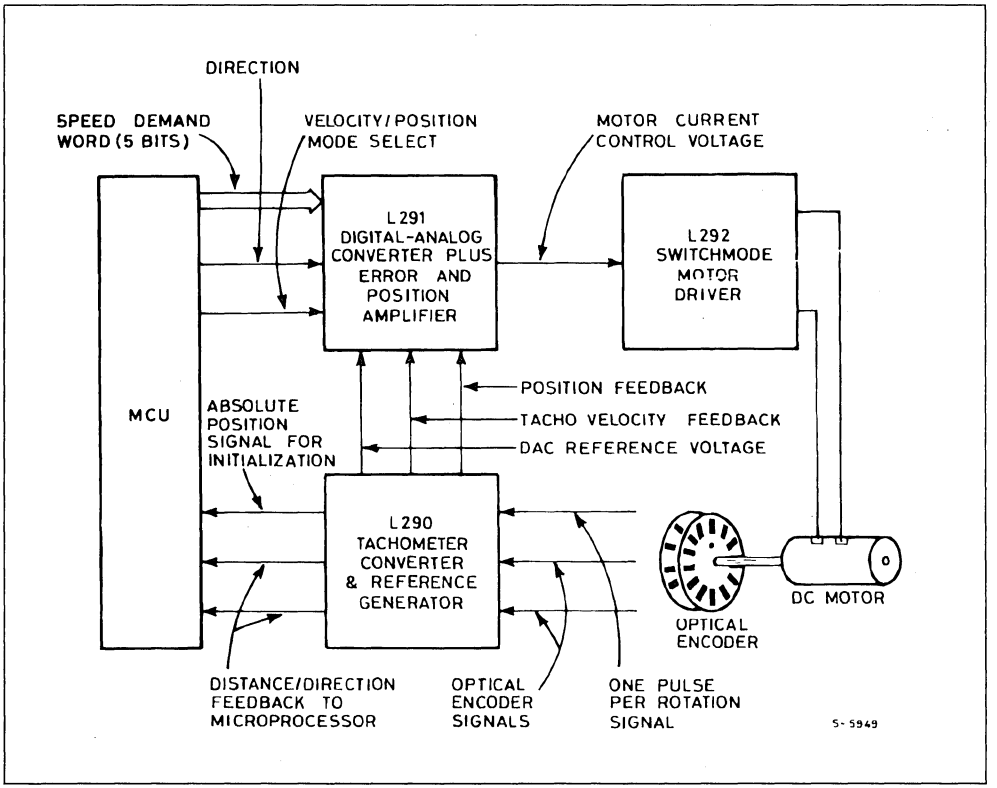


THE L290/L291/L292 DC MOTOR SPEED/POSITION CONTROL SYSTEM

The L290, L291 and L292 together form a complete microprocessor-controlled DC motor servopositioning system that is both fast and accurate. This design guide presents a description of the system, detailed function descriptions of each device and application information.

The L290, L291 and L292 are primarily intended for use with a DC motor and optical encoder in the configuration shown schematically in figure 1. This system is controlled by a microprocessor, or microcomputer, which determines the optimum speed profile for each movement and passes appropriate commands to the L291, which contains the system's D/A converter and error amplifiers. the L291 generates a voltage control signal to drive the L292 switchmode driver which powers the motor. An optical encoder on the motor shaft provides signals which are processed by the L290 tachometer converter to produce tacho voltage feedback and position feedback signals for the L291 plus distance/direction feedback signals for the control micro.

Figure 1 : The L290, L291 and L292 form a complete DC Motor servopositioning System that connects directly to Microcomputer Chips.



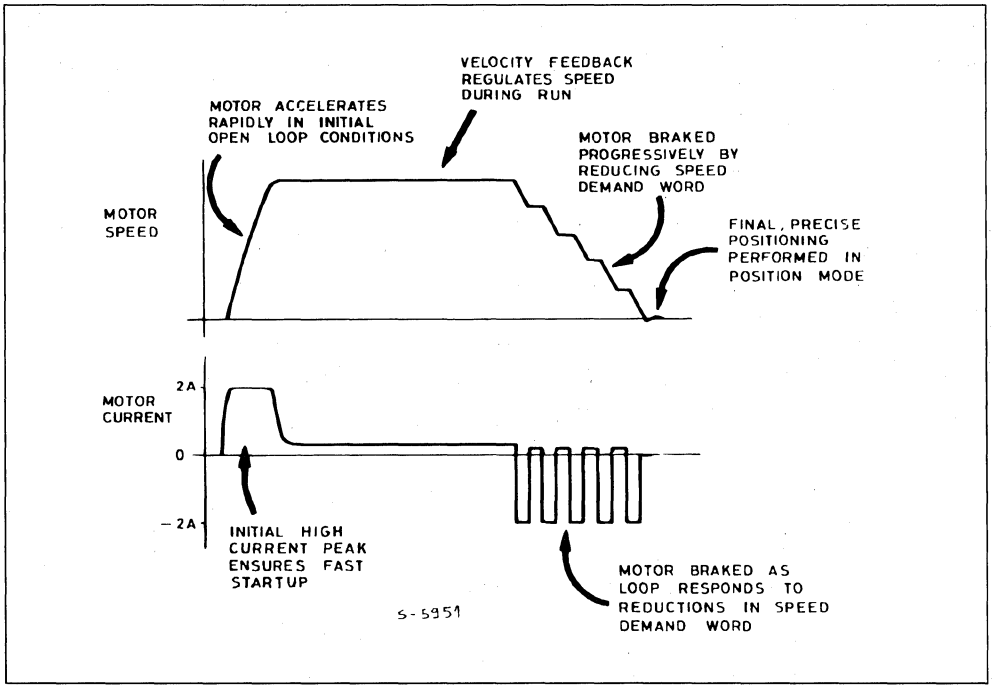
The system operates in two modes to achieve high speed and accuracy : closed loop speed control and closed loop position control. The combination of these two modes allows the system to travel rapidly towards the target position then stop precisely without ringing.

Initially the system operates in speed control mode. A movement begins when the microcomputer applies a speed demand word to the L291, typically calling for maximum speed. At this instant the motor speed is zero so there is no tacho feedback and the system operates effectively in open loop mode (see figure 2). In this condition a high current peak - up to 2A – accelerates the motor rapidly to ensure a fast start.

As the motor accelerates the tacho voltage rises and the system operates in closed loop speed mode, moving rapidly forwards the target position. The microcomputer, which is monitoring the optical encoder signals (squared by the L290), reduces the speed demand word gradually when the target position is close. Each time the speed demand word is reduced the motor is braked by the speed control loop.

Finally, when the speed code is zero and the target position extremely close, the micro commands the system to switch to position mode. The motor then stops rapidly at the desired position and is held in an electronic detent.

Figure 2 : The System operates in two Modes to achieve High Speed and Accurary. Tachometer Feedback regulates the Speed during a Run and brakes the Motor towards the End. Position Feedback allows a Precise Final Positioning.



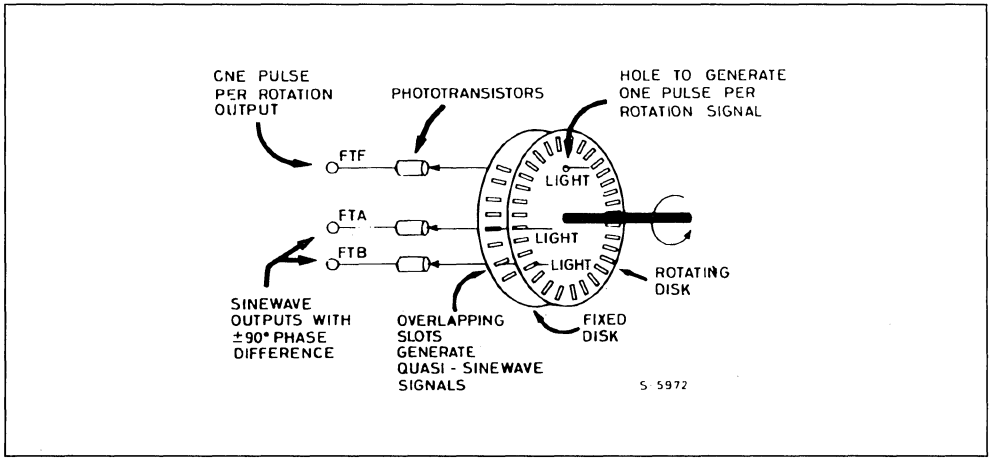
OPTICAL ENCODER

The optical encoder used in this system is shown schematically in figure 3. It consist of a rotating slotted disk and a fixed partial disk, also slotted.

Light sources and sensors are mounted so that the encoder generates two quasi-sinusoidal signals with a phase difference of ± 90° . These signals are referred to as FTA and FTB. The frequency of these signals indicates the speed of rotation and the relative phase difference indicates the direction of rotation. An example of this type is the Sensor Technology STRE 1601, which has 200 tracks. Similar types are available from a number of manufactures including Sharp and Eleprint.

This encoder generates a third signal, FTF, which consists of one pulse per rotation. FTF is used to find the absolute position at initialization.

Figure 3 : The System operates with an Optical Encoder of the Type shown schematically here. It generates two Signals 90 ° out of Phase plus a one Pulse–per–rotation Signal.



THE L290 TACHOMETER CONVERTER

The L290 tachometer converter processes the three optical encoder signals FTA, FTB, FTF to generate a tachometer voltage, a position signal and feedback signals for the microprocessor. It also generates a reference voltage for the system's D/A converter.

Analytically, the tacho generation function can be expressed as :

$$TACHO = \frac{dV_{AB}}{dt} \cdot \frac{FTA}{|FTA|} - \frac{dV_{AA}}{dt} \cdot \frac{FTB}{|FTB|}$$

In the L290 (block diagram, figure 4) this function is implemented by amplifying FTA and FTB in A1 and A2 to produce V_{AA} and V_{AB}. V_{AA} and V_{AB} are differentiated by external RC networks to give the signals V_{MA} and V_{MB} which are phase shifted and proportional in amplitude to the speed of rotation. V_{MA} and V_{MB} are passed to multipliers, the second inputs of which are the sign of the other signal before differentiation.

The sign $\left(\frac{FTA}{|FTA|} \text{ or } \frac{FTB}{|FTB|}\right)$ is provided by the comparators CS1 and CS2. Finally, the multiplier outputs are summed by A3 to give the tacho signal. Figure 5 shows the waveforms for this process.

This seemingly complex approach has three important advantages. First, since the peaks and nulls of CSA and CSB tend to cancel out, the ripple is very small. Secondly, the ripple frequency is the fourth harmonic of the fundamental so it can be filtered easily without limiting the bandwidth of the speed loop. Finally, it is possible to acquire tacho information much more rapidly, giving a good response time and transient response.

Feedback signals for the microprocessor, STA, STB and STF, are generated by squaring FTA, FTB and FTF. STA and STB are used by the micro to keep track of position and STF is used at initialization to find the absolute position.

Position feedback for the L291 is obtained simply from the output of A1.

The L290 also generates a reference voltage for the L291's D/A converter. This reference is derived from V_{AA} and V_{AB} with the function :

$$V_{ref} \equiv |V_{AA}| + |V_{AB}|$$

Since the tacho voltage is also derived from V_{AA} and V_{AB} it follows that the system is self compensating and can tolerate variations in input levels, temperature changes and component ageing wifh no deterioration of performance.

Figure 4 : The L290 processes the Encoder Signals, generating a Tacho Voltage and Position Signal for the L291 plus Feedback Signals for the Microprocessor. Additionally, it generates a Reference Voltage for the L291's D/A Converter.

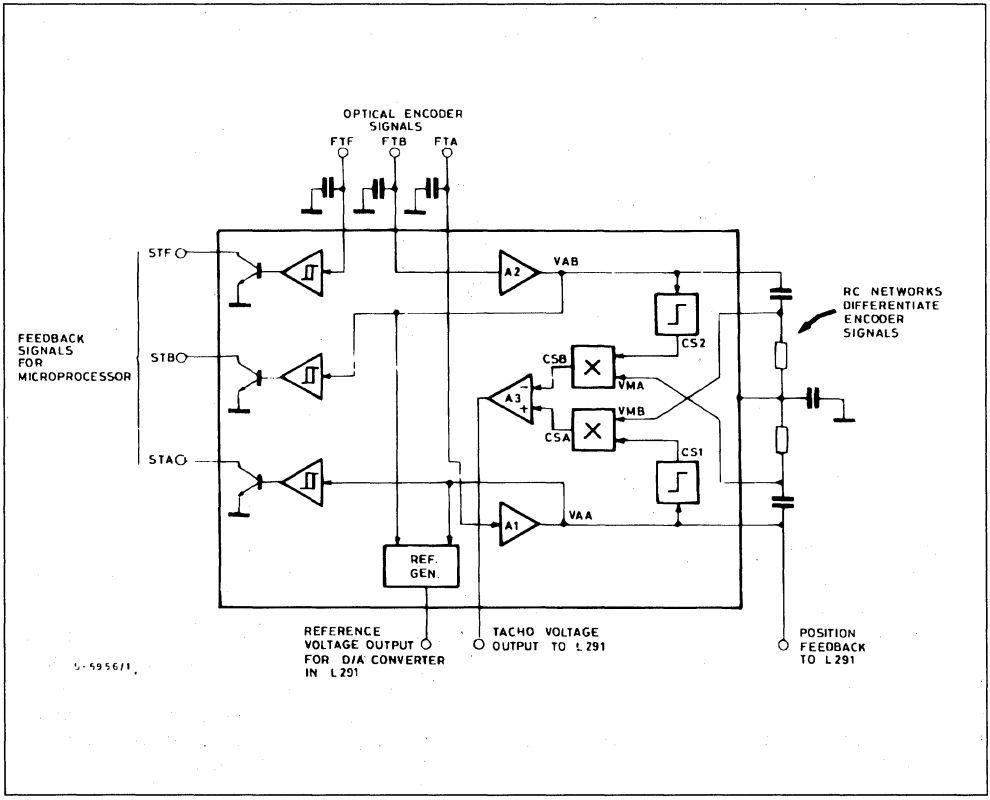


Figure 5 : These Waveforms illustrate the Generation of the Tacho Voltage in the L290. Note that the Ripple is fourth Harmonic. The Amplitude of TACHO is proportional to the Speed of Rotation.

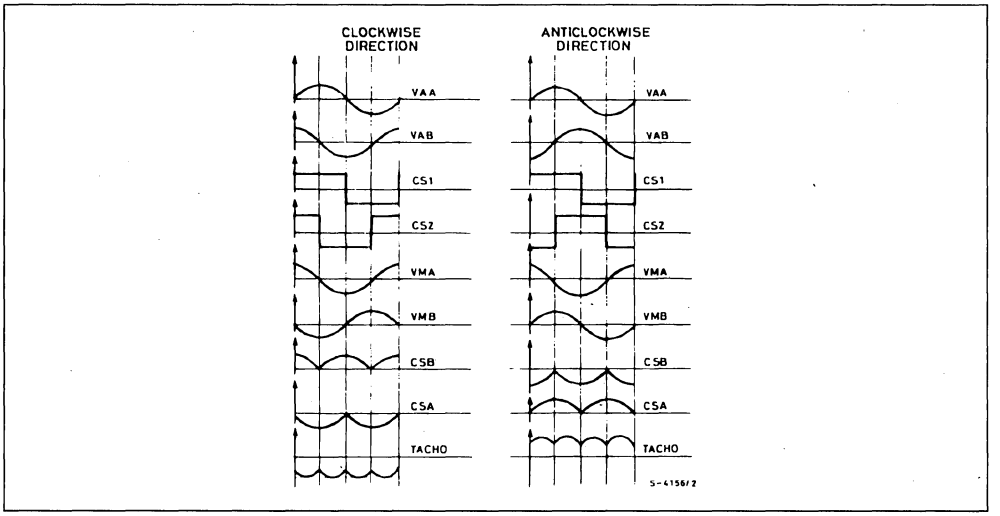
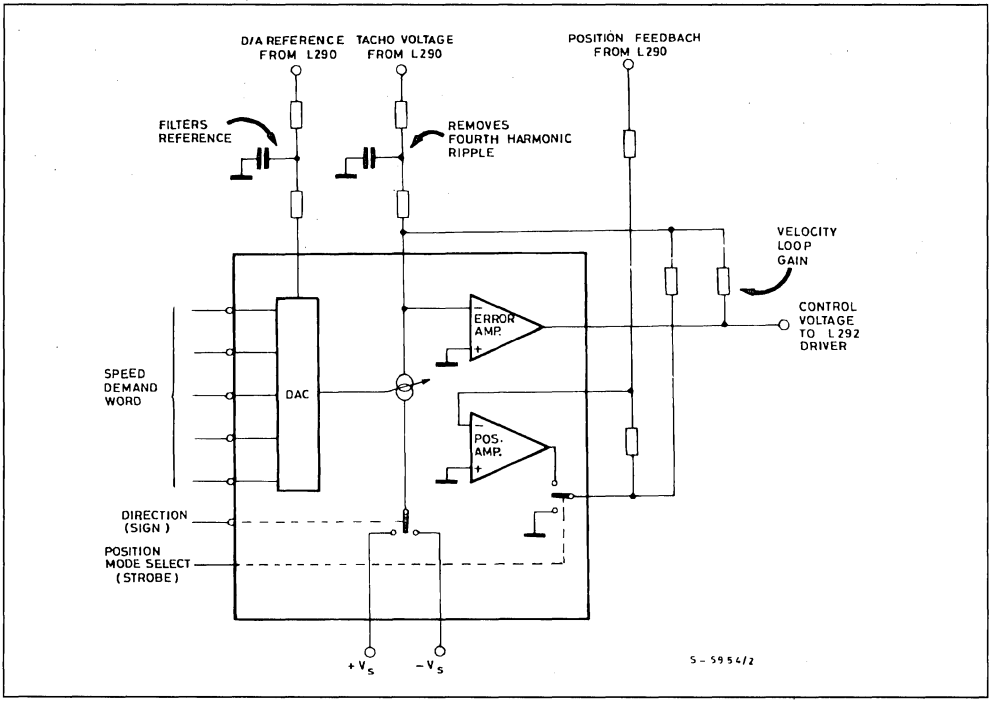


Figure 6 : The L291 Links the System to the Microprocessor. It contains the system DA converter, main error amplifier and position amplifier.



THE L291 D/A CONVERTER AND AMPLIFIERS

The L291, shown in figure 6, links the system to the micro and contains the system's main error amplifier plus a position amplifier which allows independent adjustment of the characteristics of the position loop.

It contains a five bit D/A converter with switchable polarity that takes its reference from the L290. The polarity, which controls the motor direction, is controlled by the micro using the SIGN input.

The main error amplifier sums the D/A converter output and the tacho signal to produce the motor drive signal ERRV. The position amplifier is provided to allow independent adjustment of the position loop gain characteristics and is switched in/out of circuit to select the mode. The final position mode is actually 'speed plus position' but since the tacho voltage is almost zero when position mode is selected the effect of the speed loop is negligible.

THE L292 SWITCHMODE MOTOR DRIVER

The L292 can be considered as a power transconductance amplifier - it delivers a motor current proportional to the control voltage (ERRV) from the L291. It drives the motor efficiently in switchmode and incorporates an internal current feedback loop to ensure that the motor current is always proportional to the input control signal.

The input control signal (see block diagram, figure 7) is first shifted to produce a unipolar signal (the L292 has a single supply) and passed to the error amplifier where it is summed with the current feed-back signal. The resulting error signal is used to modulate the switching pulses that drive the output stage.

External sense resistors monitor the load current, feeding back motor current information to the error amplifier via the current sensing amplifier.

The L292 incorporates its own voltage reference and all the functions required for closed loop current control of the motor. Further, it features two enable inputs, one of which is useful to implement a power on inhibit function.

The L292's output stage is a bridge configuration capable of handling up to 2A at 36V. A full bridge stage was chosen because it allows a supply voltage to the motor effectively twice the voltage allowed if a half bridge is used. A single supply was chosen to avoid problems associated with pump-back energy.

In a double supply configuration, such as the example in figure 8 a, current flows for most of the time through D1 and Q1. A certain amount of power is thus taken from one supply and pumped back into the other. Capacitor C1 is charged and its voltage

can rise excessively, risking damage to the associated electronics.

By contrast, in a single supply configuration like figure 8b the single supply capacitor participates in both the conduction and recirculation phases. The average current is such that power is always taken from the supply and the problem of an uncontrolled increase in capacitor voltage does not arise.

A problem associated with the system used in the L292 is the danger of simultaneous conduction in both legs of the output bridge which could destroy the device. To overcome this problem the comparator which drives the final stage consists of two separate comparators (figure 9). Both receive the same V_t, the triangular wave from the oscillator, signal but on opposite inputs.

Figure 7 : The L292 Switchmode Driver receives a Control Voltage from the L291 and delivers a switchmode regulated Current to the Motor.

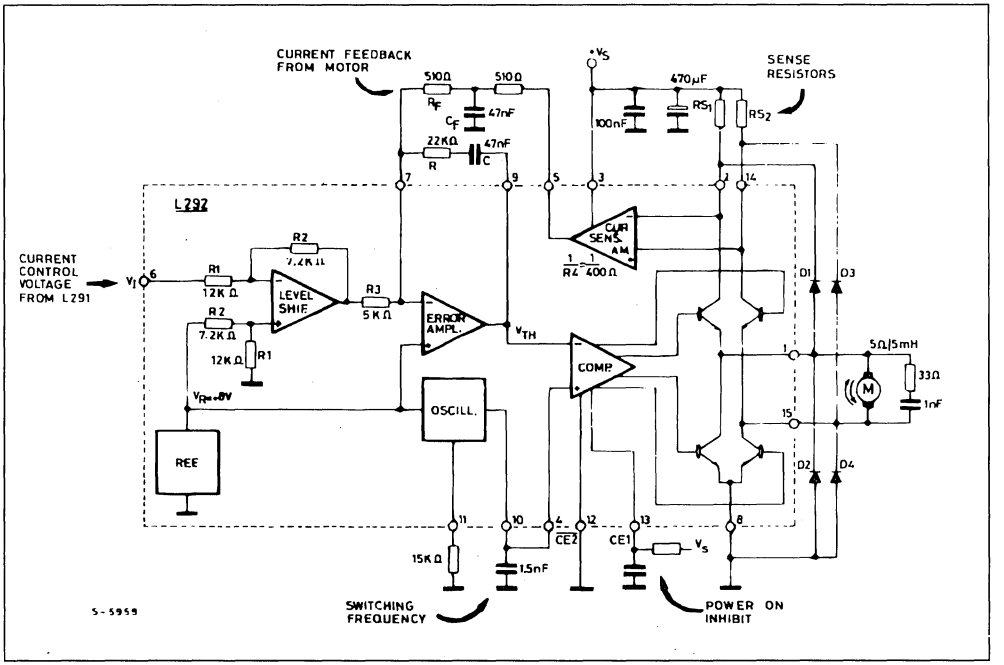
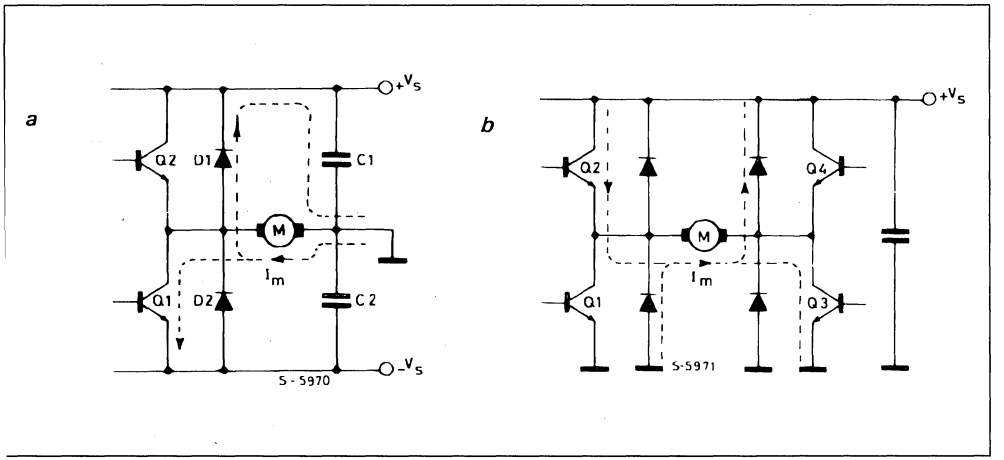
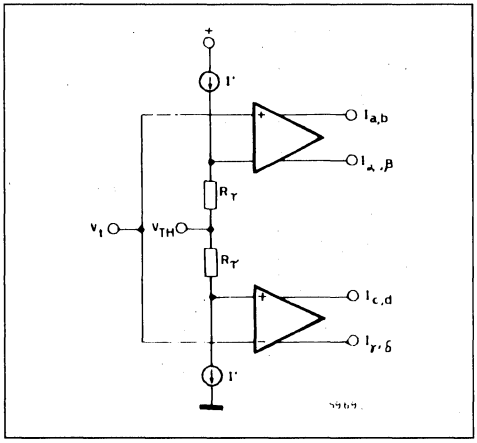


Figure 8 : A Simple Push Pull Output (a) needs a Split Supply and the Device can be damaged by the Voltage Built up on C1. The L292 has a Bridge Output to avoid these Problems. Only one Supply is needed and the Voltage across the Single Capacitor never rises excessively. Moreover, the Motor can be supplied with a Voltage up to twice the Voltage allowed with a Half Bridge.



The other two inputs are driven by V_{TH}, the error amplifier output, shifted by plus or minus $R\tau I'$. This voltage shift, when compared with V_t, results in a delay in switching from one comparator to the other.

Figure 9 : The L292's final Comparator actually consists of two Comparators. This Configuration introduces a Delay to prevent simultaneous Conduction of two Legs.

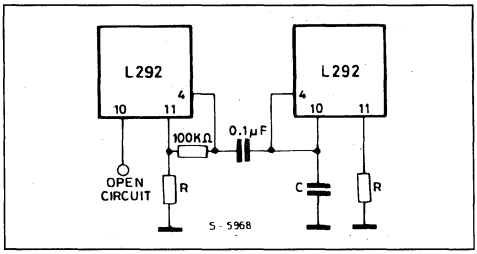


Consequently there will always be a delay between switching off one leg of the bridge and switching on the other. The delay τ is a function of the integrated resistor $R\tau$ (1.5kΩ) and an external capacitor C17 connected to pin 10 which also fixes the oscillator frequency. The delay is given by :

$$\tau = R\tau \ C17$$

In multiple L292 configurations (in a typewriter, for example, there may be two systems) it is desirable to synchronise the switching frequencies to avoid intermodulation. This can be done using the configuration shown in figure 10.

Figure 10 : Ground Plane switching Noise and Modulation Phenomena are avoided in Multi–L292 Systems by synchronizing the Chopper Rate with this RC Network.

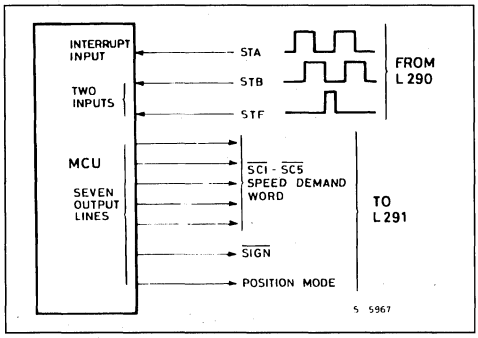


SOFTWARE AND INTERFACING TO THE MICRO

In a typical system the L290/1/2 system is connected to the control microcomputer through ten I/O lines : seven outputs and three inputs.

The outputs are all connected to the L291 D/A converter and consist of the five bit speed demand word, SIGN (which sets the direction) and the speed/position mode select line. Position feedback for the micro comes from the L290 tacho converter and consists of the signals STA, STB (the squared encoder outputs) plus the one-pulse-per rotation signal, STF (figure 11).

Figure 11 : In a typical system the L290/L291/ L292 combination is linked to the micro through seven output lines, two inputs and an interrupt input.



To follow the motor position the micro counts the STA pulses to measure the distance travelled and compares the phase of STA and STB to sense the direction. The most convenient way to do this is to connect the STA line to an interrupt input. An interrupt service routine will then sample STB and increment or decrement the position count depending on the relative phase difference : + 90° if STB is high ; -90° if STB is low.

It could be argued that the micro doesn't need to sense the direction of the rotation because it controls the direction. In practice, however, it is better to sense the direction to allow for the possibility that the motor may be moved by externally applied forces.

For each movement the micro calculates the distance to be travelled and determines the correct direction. It then sets the L291 to velocity feedback mode, sets the director appropriately and sets the speed demand word for maximum speed (possibly less if the move is very short).

By means of the STA interrupt service routine it follows the changing position, reducing the speed de-

mand word to brake the motor when the target position is very close. Finally, the micro orders the L291 to switch to position loop control for the final precise positioning.

When the system is powered up the mechanical subsystem may be in any position so the first step is to initialize it. In applications where the optical encoder never rotates more than one revolution – the daisy wheel of a typewriter, for example – this is simply done by rotating the motor slowly until the STF signal (one-pulse-per-rotation) is detected.

Where the optical encoder rotates more than once the 'one-pulse-per-rotation' signal is not sufficient. An example of this is the carriage positioning servo of a computer printer. In this case the simplest solution is to fit a microswitch on one of the endstops. First the motor is run backwards slowly until the carriage hits the endstop. Then it moves forward until the STF signal is detected. The beauty of this solution is that the endstop microswitch does not need to be positioned accurately.

Figure 12 : Complete Application Circuit of the System.

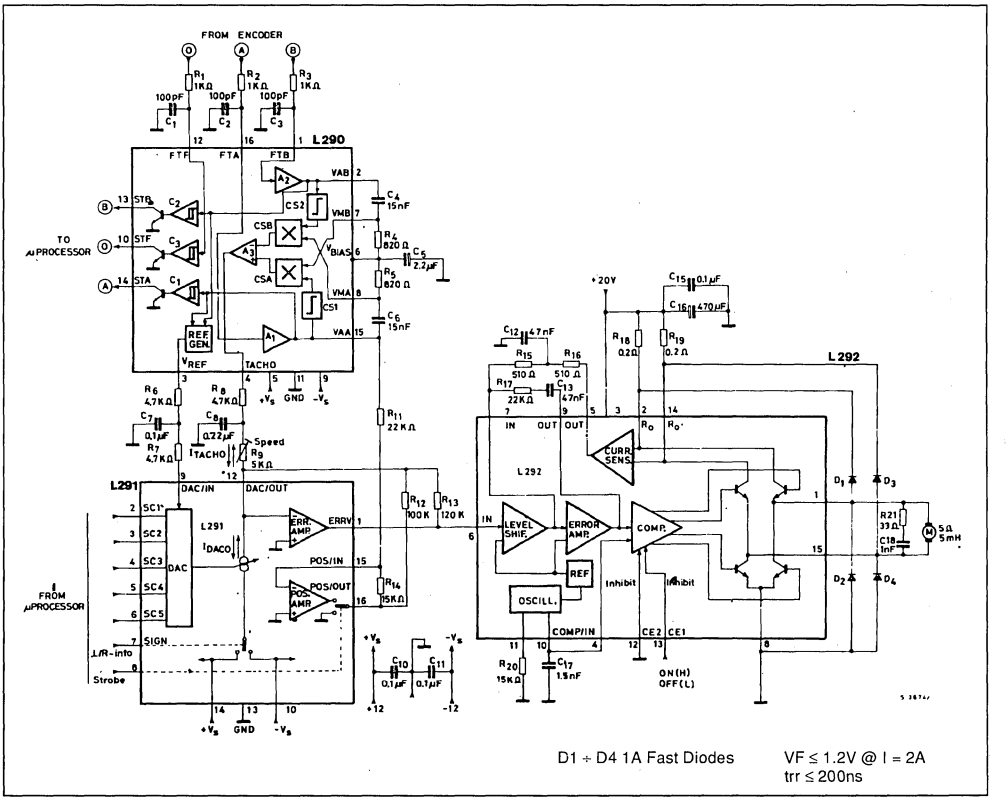


Figure 13 : P.C. Board and Component layout (1 : 1 scale).

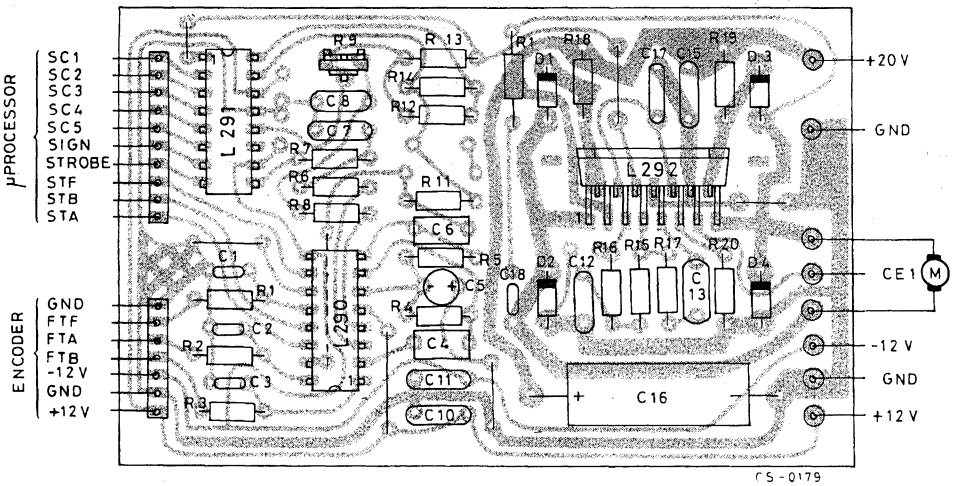


Figure 14.

Component	Recommended Value	Purpose	Larger than Recommended Value	Smaller than Recommended Value
R1, R2, R3	1 kΩ	To filter the noise on the encoder signals.	Offset voltage increase (V_{AA}, V_{AB}).	
R4, R5	820 Ω	Differentiator Network	Tacho offset and tacho signal increase.	Tacho offset increase. Tacho signal decrease.
R6, R7	4.7 kΩ	To set the D/A input current.	D/A input current decrease.	D/A input current increase.
R8	4.7 kΩ	To set the motor speed.	Motor speed increase.	Motor speed decrease.
R9	5 kΩ	To adjust the motor speed.	Danger of Oscillation R9 ≤ R13/10	
R11	22 kΩ	To set the position loop gain.	– Position loop gain decrease.	– Position loop gain increase. – Danger of oscillation of the motor shaft.
R12	100 kΩ	To set the position loop gain.	– Position loop gain decrease.	– Position loop gain increase. – Danger of oscillation of the motor shaft.
R13	120 kΩ	To set the speed loop gain.	– Speed loop gain increase.	– Speed loop gain decrease.
R14	15 kΩ	To set the position loop gain.	– Position loop gain increase. – Danger of oscillation of the motor	– Position loop gain decrease.
R15, R16	510 Ω	To filter the feedback current.	Danger of output saturation of the current sensing amplifier R15 + R16 ≤ 3.3 kΩ.	

Figure 14 : (continued).

Component	Recommended Value	Purpose	Larger than Recommended Value	Smaller than Recommended Value
R17	22 kΩ	To set the gain of the err. amplifier.	Increase of the gain at high frequencies.	Danger of Oscillations R17 > 5.6 kΩ
R18, R19	0.2 Ω	To set the transconductance value of the L292.	Transconductance decrease (R18 , R15). $I_m \leq 0.44$ V.	Transconductance increase.
R20	15 kΩ	To set the oscillator frequency.	Oscillator frequency decrease.	Oscillator frequency increase. R20 ≥ 8.2 kΩ
R 21	33 Ω	Compensation Network		Increase of the peak current in the output transistors during the communications.
C1, C2, C3	100 pF	To filter the noise on the encoder signals.	Bandwidth reduction of the low pass filter.	Bandwidth increment of the low pass filter.
C4, C6	15 nF	Differentiator Network	Tacho signal increase.	Tacho signal Decrease.
C5	2.2 µF	By-pass Capacitor	Larger set-up time after power on.	Reduced by-pass effect at low frequencies.
C7	0.1 µF	Low-pass filter for the D/A input current.		Increase of the current ripple at low speed.
C8	0.22 µ	– Low pass filter for the tacho signal. – To determine the dominant pole of the speed loop.	Bandwidth reduction of the speed loop.	Low filtering at low speed, causing noise on the motor.
C10, C11	0.1 µF	Supply By-pass Capacitor		Danger of Oscillations.
C12	47 nF	To filter the feedback current	– Lower value of the damping factor. – Danger of Oscillations	– Higher value of dumping factor.
C13	47 nF	To set the gain of the error amplifier C13 - R17 = L_M/R_M		
C15	0.1 µF	Supply By-pass Capacitor		Danger of Oscillations
C16	470 µF	Supply By-pass Capacitor		Ripple increment on the supply voltage.
C17	1.5 nF	To set the oscillator frequency and the dead time of the output transistors.	– Oscillation Frequency Reduction – Dead time increment.	– Oscillation Frequency Increment – Dead time reduction.
C18	1 nF	Compensation Network		Danger of Oscillations
D1, D2, D3, D4	1 A Fast Diodes	Recirculation Diodes		

APPLICATION CIRCUITS

The complete circuit is shown in figure 12 ; a suitable layout for evaluation is given in figure 13. Component values indicated are for a typical system using a Sensor Techonology STRE1601 encoder and a motor with a winding resistance of 5Ω and an inductance of 5mH (this motor is described fully in figure 17). How to calculate values for other motors is explained further on.

Figure 14 explains what each component does and what happens if is varied. Maximum and minimum values are also indicated where appropriate.

ADDING DISCRETE TRANSISTORS FOR HIGHER POWER

In the basic application, the L292 driver delivers 2 A to the motor at 36V. This is fairly impressive for an integrated circuit but not enough for some applications - robots, machine tools etc. The basic system can be expanded to accomodate these applications by adding external power transistors to the L292.

This is a preferable to simply adding a discrete driver stage in place of the L292 because the L292's current control loop is very useful.

Figure 15 shows how four transistors are added to increase the current to 4, 6 or 8A, depending on the choice of transistor. When coupled to the L290 and L291 this configuration appears to the system as an L292.

The average motor current, I_m, is found from :

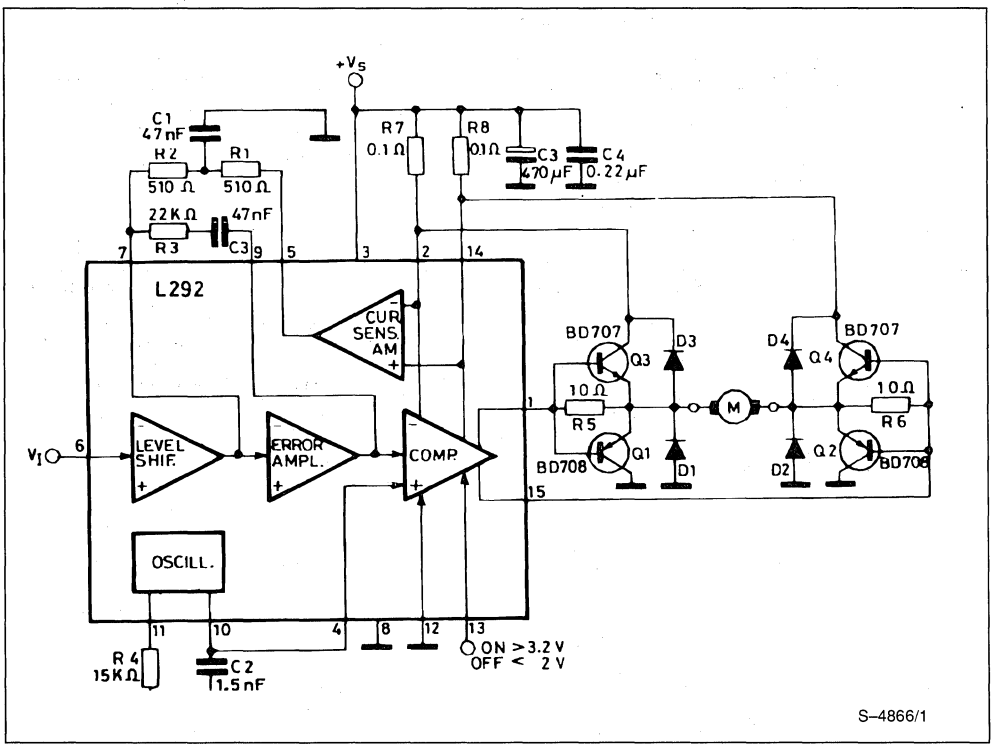
$$I_m = \frac{V_i\ 0.044}{R_x}$$

Where V_i is the input voltage and R_x is the value of the sense and resistors R7 and R8.

Suitable transistors for this configuration are indicated below :

I(A)	V_i(V)	R_x(mΩ)	Q1, Q2	Q3, Q4	D1 - D4
4	9.1	100	BD708	BD707	2A Fast Diodes
6	9.1	65	BD908	BD907	3A Fast Diodes
8	9.1	50	BDW52A	BDW51A	4A Fast Diodes

Figure 15 : For higher power external transistors are added to the L292. This circuit delivers up to 4A, if 2 BDW51A and 2 BDW52A are used it can deliver 8A.



The circuit shown in figure 16 is suitable for motor currents up to 50A at voltages to 150V. Two suplies are used ; 24V for the L292 and LS141 and 150V for the external transistors and motor. This circuit too behaves just like an L292, except for the higher power, and connects to the L290 and L291 as usual.

The motor current is given by :

$$I_m = \frac{V_{in} \times 120 \times 10^{-6} R}{R_S}$$

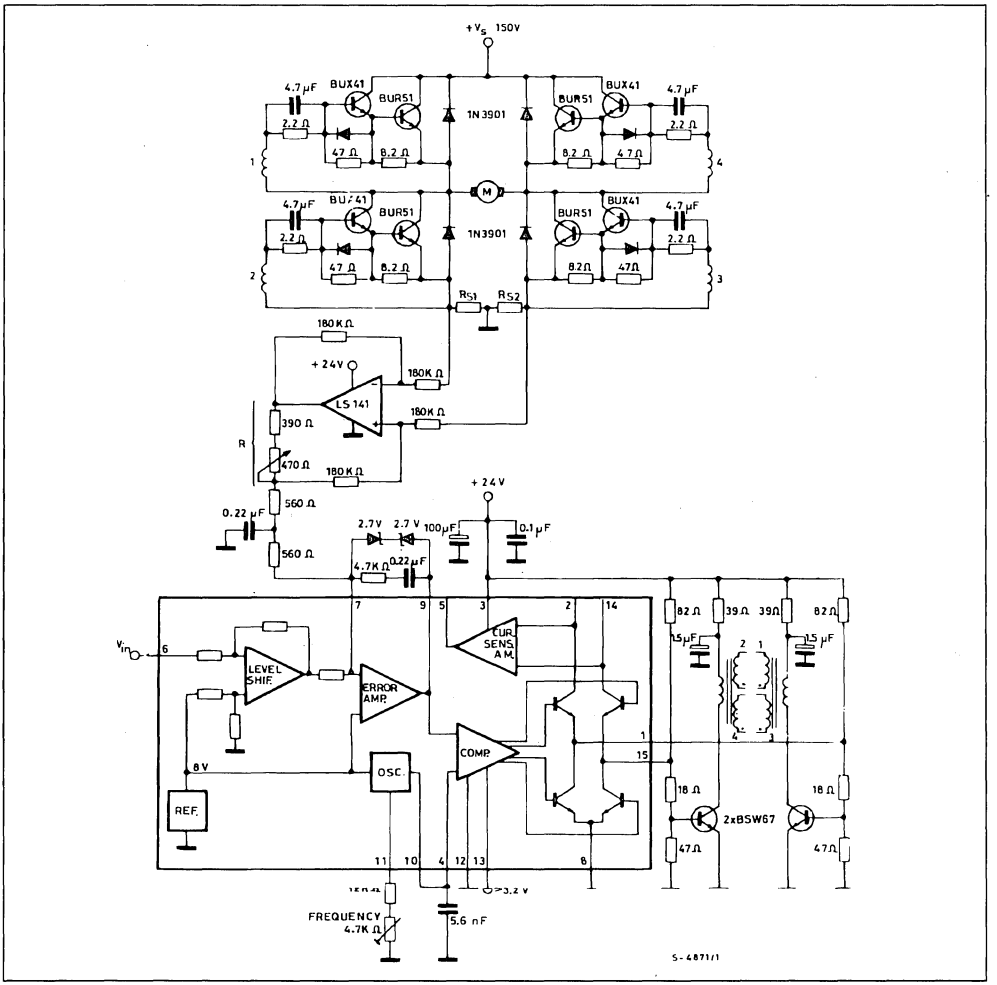
where $R_S = R_{S1} = R_{S2} = 12 \times 10^{-3}\ \Omega$

and $390\ \Omega < R < 860\Omega$

This gives a range of transconductance values (I_m/V_{in}) from 3.0A/V (R = 390 Ω) to 8.6A/V (R = 860Ω).

In this circuit the L292 drives two transformers whose secondaries drive the power transistors. The coil ratio of the transformers is 1 : 20. To limit the duty cycle at which the transformers operate from 15% to 85%, two zener diodes are inserted between pin 7 and pin 9 of the L292. The LS141 op amp supplies current feedback from the transistor bridge to the L292.

Figure 16 : For higher voltages and currents–up to 150V at 50A, this circuit can be used. It connects to the L290 and L291, behaving just like and L292.



DESIGN CONSIDERATIONS

The application circuit of figure 12 will have to be adapted in most cases to suit the desired performance, motor characteristics, mechanical system characteristics and encoder characteristics. Essentially this adaptation consists of choosing appropriate values for the ten or so components that determine the characteristics of the L290, L291 and L292.

The calculations include :

- Calculation of maximum speed and acceleration ; useful both for defining the control algorithm and setting the maximum speed.
- Calculation of R8 and R9 to set maximum speed.
- Laplace analysis of system to set C8, R11, R12, R13 and R14.
- Laplace analysis of L292 loop to set the sensing resistors and C12, C13, R15, R16, R17.
- Calculation of values for C4 and C6 to set max level of tacho signal.
- Calculation of values for R6 and R7 to set D/A reference current.
- Calculation of R20 to set desired switching frequency.

MAXIMUM ACCELERATION

For a permanent magnet DC motor the acceleration torque is related to the motor current by the expression :

$$T_a + T_f = K_T I_m$$

where :

I_m is the motor current

K_T is the motor torque constant

T_a is the acceleration torque

T_f is the total system friction torque

The acceleration torque is related to angular acceleration and system inertia by :

$$T_a = (J_m + J_{oe} + J_L)\, a$$

where :

J_m is the moment of inertia of the motor

J_{oe} is the moment of inertia of the encoder

J_L is the moment of inertia of the load

a is the angular acceleration

In a system of this type the friction torque T_f is normally very small and can be neglected. Therefore, combing these two expressions we can find the angular acceleration from :

$$a = \frac{K_T}{J_m + J_{oe} + J_L} \cdot I_m$$

It follows that for a given motor type and control loop the acceleration can only be increased by increasing the motor current, I_m.

The characteristics of a typical motor are given in figure 17. From this table we can see that :

$K_T = 4.3$N cm/A (6.07 oz. in/A)

$J_m = 65$g . cm^2 (0.92×10^{-3} oz. in s^2)

We also know that the maximum current supplied by the L292 is 2 A and that the moment of inertia of the STRE 1601 optical encoder, J_{oe}, is 0.3×10^{-4} oz. in. s^2.

The moment of inertia of the load J_L, is unknown but assume, for example, that $J_{oe} + J_L \cong 2\, J_m$. Therefore the maximum angular acceleration is :

$$a = \frac{6.07 \times 2}{2 \times 0.92 \times 10^{-3}} = 6597.8 \text{rad/s}^2$$

Fig. 17 - The Characteristics of a Typical DC Motor.

Motor - Parameter	Value
U_{BB} (V_s)	18 V
C. emf. K_E	4.5 mV/min^{-1}
N_o (without load)	3800 rpm
I_{om} (without load)	190 mA
T_f (friction torque)	0.7 N cm
K_T (motor constant)	4.3 N cm/A
Amature Moment of Inertia	65 g. cm.^{2}
R_M of the Motor	5.4 Ω
L_M of the Motor	5.5 mH

MAXIMUM SPEED

The maximum speed can be found from :

$V_{S\,min} = 2\, V_{CEsat} + R_S\, I_m + K_e\, \Omega + R_m\, I_m$

where :

$E =$ $K_e\, \Omega$ is the internally generated voltage (EMF)

K_e is the motor voltage constant

Ω is the rotation speed of the motor.

For example, if $V_{s\,min} = 20$V

$2\, V_{CEsat} + R_s\, I_m = 5$V (from L292 datasheet)

$R_m\, I_m = 10.8$V ($R_m = 5.4\ \Omega$)

we obtain :

$$K_e\, \Omega\, (E) = 4.2\text{V}$$

and

$$\Omega = \frac{4.2\text{ V}}{4.5\text{ mV/min}^{-1}} = 933.3\text{rpm} = 97.74\text{rad/s}$$

The STRE1601 encoder has 200 tracks so this speed corresponds to :

$$V = \Omega \frac{200}{60} = 3111.1 \text{ tracks/s.}$$

The time taken to reach maximum speed from a standing start can be found from

$$\Delta t = \frac{\Omega}{a} = \frac{97.74 \text{ rad/s}}{6597.8 \text{ rad/s}^2} = 14.8\text{ms}$$

We can also express the acceleration in terms of tracks/s^2 :

$$K = \frac{V}{\Delta t} = \frac{3111.1 \text{ tracks/s}^2}{14.8 \text{ ms}} =$$

$$= 210209.5 \text{ tracks/s}^2$$

Therefore the number of tracks necessary to reach the maximum system speed for our example is :

$$p = \frac{V^2}{2K} = 23 \text{ tracks}$$

This information is particularly useful for the programmer who writes the control software.

SETTING THE MAXIMUM SPEED

The chosen maximum speed is obtained by setting the values of R6, R7, R8, R9, C4 and C6 (all shown on the application circuit, figure 12). This is how it's done :

The first step is to calculate R6 and R7, which define the DAC current reference. From the L291 datasheet we know that I_{ref}, the DA converter current reference, must be in the range 0.3mA to 1.2mA.

Choosing an I_{ref} of roughly 0.5mA, and knowing that V_{ref} (the L290s reference output) is typically 5V, it follows that :

$$R6 + R7 = \frac{V_{ref}}{I_{ref}} = 10\text{k}\Omega$$

Therefore we can choose R6 = R7 = 4.7kΩ (5% tolerance).

Substituting the minimum and maximum values of V_{ref} (from the L290 datasheet) and the resistance variations we can now check that the variation of I_{ref} in the worst case is acceptable.

$$I_{ref\ min} = \frac{V_{ref\ min}}{(R6 + R7)\ max} = 0.46\text{mA}$$

$$I_{ref\ typ} = \frac{V_{ref\ (typ)}}{4.7\text{k} + 4.7\text{k}} = 0.53\text{mA}$$

$$I_{ref\ max} = \frac{V_{ref\ max}}{(R6 + R7)\ min} = 0.62\text{mA}$$

These values are within the 0.3mA to 1.2mA limits.

Now that the reference current is defined we can calculate values for R8 and R9 which define the tacho current at the summing point.

The full scale output current of pin 12 of the L291 (the D/A converter output) is :

$$I_o = 1.937\ I_{ref}$$

which is typically 1.02mA.

The worst case output current is when I_{ref} is at a maximum (0.62mA) and the I_{out} error is maximum (+ 2 %) :

$$I_o = 0.62 \times 1.937 \times 1.02 = 1.22\text{mA}$$

This less than the 1.4 mA maximum value for I_{out} specified in the L291 datasheet.

Assuming that the maximum DC voltage at the TACHO output of the L290 (pin 4) is 7V (this is the tacho voltage generated at the maximum system speed), we can find the sum of R8 and R9 ;

$$R8 + R9 = \frac{V_{tacho\ DC}}{I_{o\ typ}} = \frac{7}{1.02} = 6.85\text{k}\Omega$$

Therefore we choose R8 = 4.7kΩ and a 5kΩ trimmer for R9. R9 is used to adjust the maximum speed.

We can now calculate the ripple voltage and maximum tacho voltage :

$$V_{ripple\ pp} = \frac{\pi}{4} (\sqrt{2} - 1)\ V_{tacho\ DC} \cong 2.3\ V_{pp}$$

$$V_{tacho\ max} = \frac{\pi}{4} \sqrt{2}\ V_{tacho\ DC} \cong 7.8\ V_p$$

This value is within the voltage swing of the tacho amplifier (± 9V) ; that means the choice of $V_{tacho\ DC}$ = 7V is correct.

At this point we know the values of R6, R7, R8 and R9. The maximum speed can now be set by choosing values for C4 and C6 which form the differentiation networks on the L290. These values depend on the number of tracks of the optical encoder. For the STRE1601 encoder the capacitor values can be found from figure 18. These curves show how the capacitor values is related to frequency (encoder rotation speed) for different tacho voltages and maximum speed. The example values are $V_{tacho\ DC}$ = 7V and maximum speed = 3111 tracks/sec therefore the value for C4 and C6 is 15nF.

The values of R4 and R5 must be 820Ω to minimize the offsets.

Figure 18 : C4 and C6 value versus rotation speed for various maximum tacho voltage values.

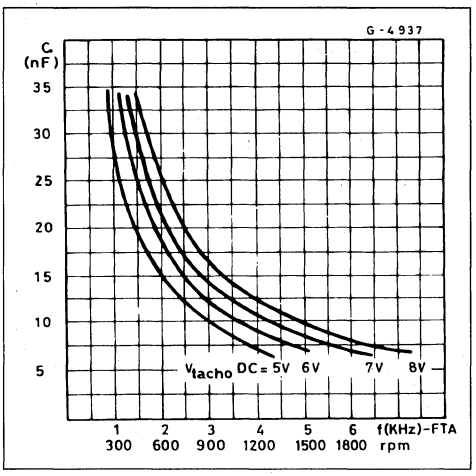
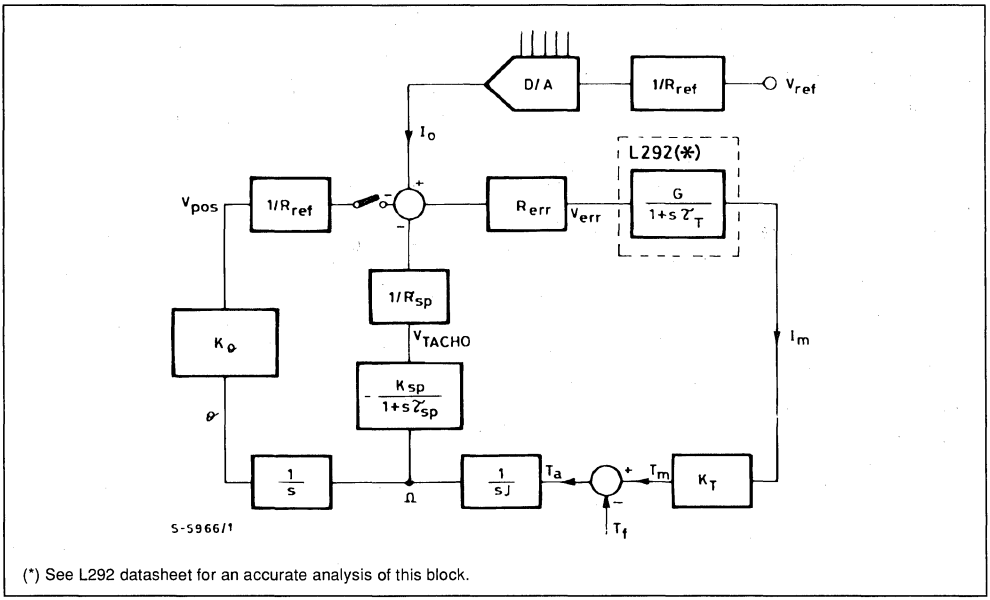


Figure 19.



(*) See L292 datasheet for an accurate analysis of this block.

List of terms

s : Laplace variable
K_T : Motor torque constant
T_a : Acceleration torque
T_f : Total system friction torque
J : Total moment of inertia ($J = J_{oe} + J_m + J_L$).
Ω : Speed
θ : Angular position
K_{sp} : Conversion factor that links the motor rotation speed and the TACHO signal.
K_T : Conversion factor that links the motor position and the Vpos signal.

LAPLACE ANALYSIS OF THE SYSTEM

Stable values for the components R11, R12, R13, R14 and C8 can be found from a Laplace analysis of the system. Figure 19 shows a simplified block diagram of the system which will be useful for the analysis.

The analysis is based on the angular speed Ω and on the motor position θ. The motor is represented, to a first approximation, by the current Im and by the acceleration torque, Ta, which drives an inertial load J.

There are two conversion factors, Ksp and Kθ. They link the mechanical parameters (position and speed) with the equivalent feedback signals for the two loops. The values of Ksp and Kθ are determined by the encoder characteristics and the gain parameters of the integrated circuits. The openloop and closed-loop gains are fixed by four external resistors :

- R_{ref} – fixes the reference current (R6 + R7)
- R_{speed} – fixes the speed loop gain (R8 + R9)
- R_{pos} – controls the position loop gain (R12)
- R_{err} – controls the system loop gain (R13).

The stability both of the speed loop and of the speed-position loop are defined by external components.

The fundamental characteristics of the speed control system can thus be determined by the designer.

τ_{sp} is the time constant that determines the dominant pole of the speed loop and is determined by C8, R8 and R9

$$\tau_{sp} = C8 \quad \frac{R8\ R9}{R8 + R9.}$$

SETTING THE L292 COMPONENTS

The sensing resistor and feedback loop component values for the L292 can be calculated easily using the following formulae. A detailed Laplace analysis of this block is given on the L292 datasheet.

a) Sense resistors. $R_S = R18 = R19$

$$\frac{I_m}{V_i} = \frac{R2\ R4}{R1\ R3} \cdot \frac{I}{R_S}$$

$$\Rightarrow \quad R_S = \frac{R2\ R4\ V_i}{I_m\ R1\ R3}$$

(These resistors are all inside the L292).

where :

I_m is the motor current

V_i is the input voltage corresponding to I_m.

For example, Im = 2 A, Vi = 9.1 V, resistor values as in figure 7 (L292 internal block diagram)

$$R_s = \frac{0.044}{I_m} \qquad V_i = 0.2\ \Omega$$

b) R17, R15, R16, C12, C13

$$G_{mo} = \frac{2\ V_s}{R_m\ V_R}$$

V_s = L292 supply voltage

R_m = motor resistance

V_R = L292 reference voltage

and

$$\xi = \sqrt{\frac{R4C13}{4R15\ C12\ G_{mo}\ R_s}}$$

R4 = L292 internal resistor (400Ω)

Rs = R18 = R19

A good choice for ξ is $1/\sqrt{2}$. Substituting this value, Gmo and the values of R4 and R_S :

$$\xi^2 = \frac{1}{2} = \frac{400\ C13}{4R15\ C12 \times 0.2}$$

$$\Rightarrow \frac{1000\ C13}{R15\ C12} = 1$$

Also $$f_T = \frac{0.9}{2\pi\ R15\ C12}$$

Assuming that f_T is 3kHz, another recommended value :

$$R15\ C12 \cong 47 \times 10^{-6}s$$

Therefore we can find C13 :

$$1000\ C13 \cong 47 \times 10^{-6}$$

$$\Rightarrow C13 = 47nF$$

Since

$$\frac{L_m}{R_m} = R17\ C13$$

$$R17 = \frac{L_m}{C13\ R_m}$$

For the example motor Lm = 5mH, R_m = 5.4Ω therefore :

$$R17 = \frac{L_m}{C13\ R_m} = 22k\Omega$$

From R15 C12 ≅ 47 x 10^{-6} s, choosing a value of R15 ; 510Ω , we have :

$$C12 = 82nF$$

Also, R16 = R15 = 510Ω.

DEAD TIME

C17 sets the switching delay of the L292 which protects against simultaneous conduction. The delay is :

$$\tau = R_\tau \, C17$$

and R_τ is an internal 1.5k resistor. The suggested 1.5nF value gives a switching delay of about 2.25µs. This is more than adequate because the transistors have a switch off delay of only 0.5µs.

SWITCHING FREQUENCY

The switching frequency is set by C17 and R20 :

$$f_{osc} = \frac{1}{2\,R20\,C17}$$

R20 must be at least 8.2kΩ and is varied to set the frequency : the value of C17 is imposed by dead time requirements. Typically the frequency will be 15-20kHz.

It should be outside the audio band to reduce noise but not to high or efficiency will be impaired. The maximum recommended value is 30kHz.

CURRENT RIPPLE

To reduce dissipation in the motor and the peak output current the ripple, Δ Im,should be less than 10% of the maximum current.

Since

$$\Delta I_m = \frac{V_s}{L_m} \cdot \frac{T}{2}$$

($\frac{T}{2}$ = half period oscillator)

and

$$\Delta I_m = 0.1\ I_{m\,max}$$

$$0.1\ I_{m\,max} = \frac{V_S}{2\,f\,L_{M\,min}}$$

$$L_{M\,min} = \frac{5\,V_S}{f\,I_{m\,max}}$$

Therefore there is a minimum inductance for the motor which may not always be satisfied. If this is the case, a series inductor should be added and the value is found from :

$$L_{series} = \frac{5\,V_s}{f\,I_{m\,max}} - L_M$$

EFFICIENCY AND POWER DISSIPATION

Neglecting the losses due to switching times and the dissipation due to the motor current, the efficiency of the L292's bridge can be found from :

$$\eta = 1 - \frac{\Delta t1}{\Delta t1 - \Delta t2} \cdot \frac{V_{sat}}{V_s} - \frac{\Delta t1}{\Delta t - \Delta t2} \cdot \frac{V_{over}}{V_s}$$

where :

$V_{over} \cong 2V\ (2V_{BE} + R_s\, I_m)$

$V_{sat} \cong 4V\ (2V_{CEsat} + 3\ V_{BE}\ )$

Δ t1 = transistor conduction period

Δ t2 = diode conduction period.

If $\Delta t1 \geq \Delta t2$ and $V_s = 20V$ we obtain :

$$\eta = 1 - \frac{4}{20} = 80\%$$

In practice the efficiency will be slightly lower as a results of dissipation in the signal processing circuit (about 1W at 20V) and the finite switching times (about 1W).

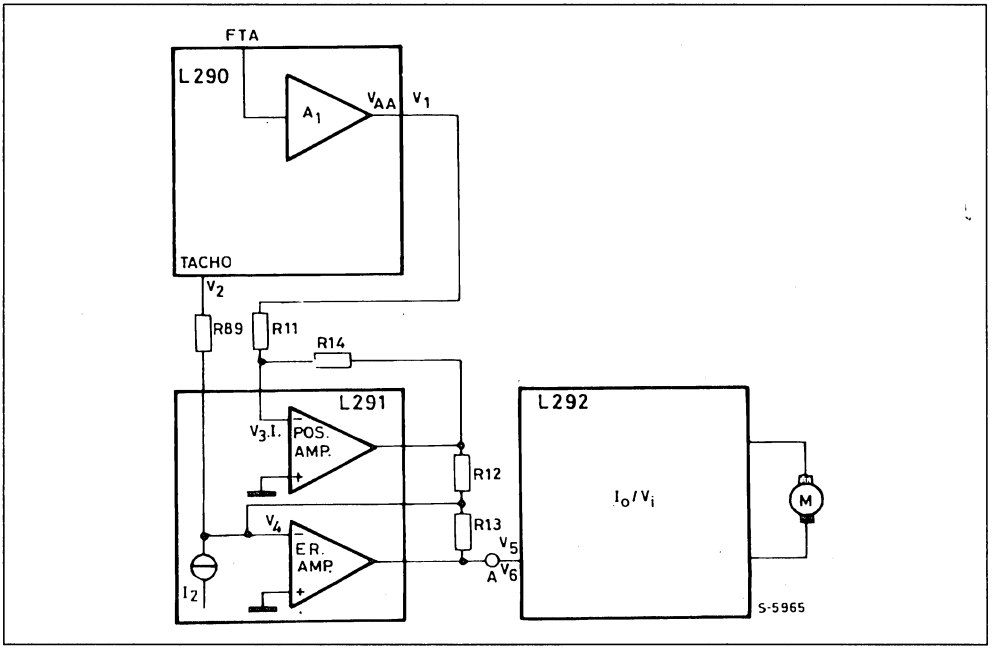
If the power transferred to the motor is 40W, the 80% efficiency implies 10W dissipated in the bridge and a total dissipation of 12W. This gives an actual efficiency of 77%. Since the L292's Multiwatt package can dissipate up to 20W it is possible to handle continuous powers in excess of 60W.

POSITION ACCURACY

The main feature of the system L290, L291, L292 is the accurate positioning of the motor. In this section we will analyse the influence of the offsets of the three ICs on the positioning precision.

When the system is working in position mode, the signal FTA coming from the optical encoder, after suitable amplification, is sent to the summing point of the error amplifier (L291). If there were no offset and no friction, the motor would stop in a position corresponding to the zero crossing of the signal FTA, and then at the exact position required. With a real system the motor stops in a position where FTA has such a value to compensate the offsets and the friction ; as a consequence there is a certain imprecision in the positionning. The block diagram, fig. 20, shows the parts of the 3 ICs involved in the offsets. First we will calculate the amount of the offsets at the input of the IC L292 (point A of fig. 20).

Figure 20.



L290

The offset of the TACHO signal, V2, is the main cause of the imprecision of the positioning. Another offset in L290 is V1, the output offset voltage of A1. The contribution at point A is :

$$V_{1A} = V1 \cdot \frac{R14}{R11} \cdot \frac{R13}{R12}$$

$$V_{2A} = V2 \cdot \frac{R13}{R89}$$

L291

In this IC there are the following offsets :

V3 = input offset voltage of the position amplifier

I1 = input bias current of the postion amplifier

I2 = output offset current of the D/A converter plus ER. AMP bias current

V4 = input offset voltage of the error amplifier.

Their contribution at point A is :

$$V_{3A} = V3 \cdot \left(1 + \frac{R14}{R11}\right) \cdot \frac{R13}{R12}$$

$$VI_{1A} = I1 \cdot R14 \frac{R13}{R12}$$

$$VI2A = I2 \,.\, R13$$

$$V_{4A} = V4 \left(1 + \frac{R13}{R12//R89}\right)$$

L292

Referring to this IC we must consider the input offset voltage V5. Moreover, we call V6 the input voltage that must be applied to the L292 to keep the motor in rotation, i.e. to compensate the dynamic friction. V6 is not an offset voltage, but has the same effects, and for this reason we have to put it together with the offsets.

$V_{5A} = V5 \quad \frac{I_o}{V_i}$ = Transconductance of L292

$$V_{6A} = V6 = \frac{I6}{\left[\frac{Io}{V_i}\right]}$$

I_6 = Motor current necessary to compensate the dynamic friction

The total offset voltage referred to point A is given by the sum of all the precedent terms :

$V_A = V_{1A} + V_{2A} + V_{3A} + VI_{1A} + VI_{2A}\ V_{4A} + V_{5A} + V_{6A}$.

The amplitude of the signal FTA necessary to compensate the offset VA is :

$$V_{FTA} = V_A \cdot \frac{R12}{R13} \cdot \frac{R11}{R14} \cdot \frac{1}{A1}$$

Calling V_M the maximum value of the signal FTA, the phase error of the system is :

$$\alpha = \sin^{-1} \frac{V_{FTA}}{V_M}$$

If α_c is the phase between two consecutive characters, (it may be equal 360° or multiple of it) the percentage error in the character positioning is :

$$\varepsilon = \frac{\alpha}{\alpha c} \cdot 100$$

In these calculations we have not considered how the precision of the signal FTA, coming from the optical encoder, influences the positioning error. The percentage value of the pitch accuracy must be added to ε to have the total percentage error in the character positioning. Any DC offset of the mean value of the signal FTA must be multiplied by A1 and added to V1 to obtain its effect on the error.

NUMERICAL EXAMPLE

In this numerical example we will calculated the precision of the positioning in the worst case, i.e. with all the offsets at the max value. The values of the external components are taken from the application circuit. (fig. 12).

R11 = 22K R12 = 100K R13 = 120K R14 = 15K R89 = R8 + R9 = 6K

From the data sheets of the three ICs we can find :

V1 = 55mV V2 = 80mV V3 = 4.5mV

V4 = 2mV V5 = 350mV

I1 = 0.3µA I2 = 0.4µA

A1 min = 22dB = 12.6

$$\frac{Io}{Vi}\ \text{min} = 205\ \frac{mA}{V}$$

$$V_{Mmin} = 0.4\ V$$

For I_6 we will consider the value I6 = 50mA

$$V_{1A} = 55.10^{-3} \cdot \frac{15}{22} \cdot \frac{120}{100} = 45mV$$

$$V_{2A} = 80 \cdot 10^{-3} \cdot \frac{120}{6} = 1.6V$$

$$V_{3A} = 4.5 \cdot 10^{-3} \left(1 + \frac{15}{22}\right) \cdot \frac{120}{100} = 9.1mV$$

$$VI_{1A} = 0.3 \cdot 10^{-6} \cdot 15 \cdot 10^{3} \frac{120}{100} = 5.4mV$$

$$VI_{2A} = 0.4 \cdot 10^{-6} \cdot 120 \cdot 10^{3} = 48mV$$

$$V_{4A} = 2 \cdot 10^{-3} \cdot \left(1 + \frac{120}{5.6}\right) = 44.9mV$$

$$V_{5A} = 350mV$$

$$V_{6A} = \frac{50}{205} = 244mV$$

$$V_A = 2.346V$$

$$V_{FTA} = 2.329 \cdot \frac{100}{120} \cdot \frac{22}{15} \cdot \frac{1}{12.6} = 0.228V$$

$$\alpha = \sin^{-1} \frac{0.226}{0.4} \cong 35°$$

If we consider an optical encoder with 200 tracks/turn and a daisy wheel with 100 characters, the phase between two consecutive characters is ac = 720°, and then the maximum percentage error we can have is.

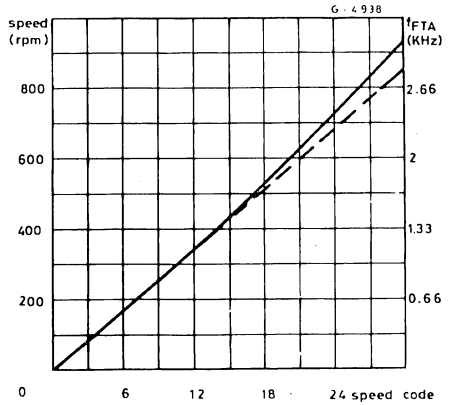
$$\varepsilon = \frac{35}{720} \cdot 100 \cong 4.8\%$$

From this numerical example we can see that the main contribution to the positioning error is given by the offset of the TACHO signal (V_{2A}) , other big contributions are given by the input offset voltage of L292 (V_{5A}) and by the voltage necessary to compensate the dynamic friction of the moto (V_{6A}). This last term is only determined by the motor and can also have greater values.

The error we have calculated is the maximum possible and it happens when all the offsets have the max value with the same sign, i.e. with a probability given by the product of the single probabilities. Considering as an example every offset has a probability of 1% to assume the max value, the probability the error assumes the max value is :

$$P = (10^{-2})^{7} = 10^{-14}$$

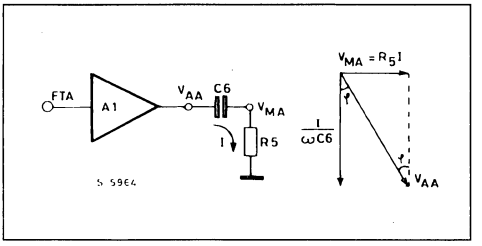
Figure 21.



SPEED ACCURACY

If we consider the complete system with L290-L291-L292 driving a DC MOTOR with optical encoder, we can note the speed of the motor is not a linear function of the speed digital code appied to L291. The diagram of fig. 21 shows this function and it is evident that the speed increases more than a linear function, i.e. if the speed code doubles, the speed of the motor becomes more than the double. The cause of this non linearity is the differentiator network R4 C4 and R5 C6 (see fig. 22) that has not an ideal behaviour at every frequency.

Figure 22.



1) $V_{MA} = V_{AA} \sin \varphi$

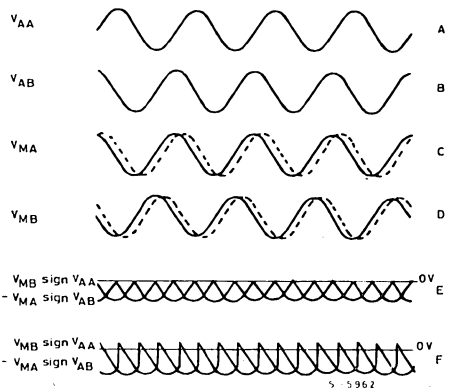
$\varphi = tg^{-1}$ ω R5 C6 $\omega = 2 \pi f$

2) $V_{MA} = V_{AA} \sin tg^{-1} \omega$ R5 C6

f = frequency of the signal FTA

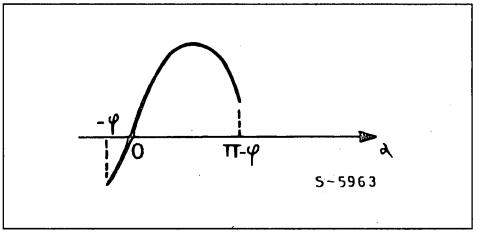
This last relation gives the amplitude of the signal V_{MA} ; it is evident there is not a linear function between VMA and ω, like $V_{MA} = K\omega$ and the difference is greater if the product ω R5 C6 doesn't respect the disequation ω R5 C6 $\ll$ 1., i.e. at high frequencies.

Figure 23.



The phase angle between V_{MA} and V_{AA} should be 90° and then $\varphi = 0$, in our case φ increases with the frequency according to the equation $\varphi = tg^{-1}$ w R5C6, and inflences the amplitude of the output signal TACHO. In fig. 23 are shown the waveforms that contribute to generate the TACHO signal. A and B are the signals V_{AA} and V_{AB} in phase with the input signals FTA and FTB. C and D are the signals V_{MA} and V_{MB} : the continue line indicate the ideal case, in fact the phase between V_{MA} and V_{AA} is 90° ; the dotted line is referred to the real case in which the phase is lower than 90°. By adding the two signals shown in E we obtain the TACHO signal, whose expression is :

Figure 24.



$V_{TACHO} = V_{MB}$. sign $V_{AA} - V_{MA}$. sign V_{AB}.

The signals in E are reffered to the ideal case, the ones in F to the real case. It is possible to demonstrate the mean value of the TACHO signal in the real case is lower than the one we could have with an ideal differentiator network and this explains why in fig. 21 the speed of the motor increases more than a linear funciton. The mean value of the waveforms F is (fig. 24).

$$3)\ V_m = \int_{-\varphi}^{\pi-\varphi} K1 \sin\alpha\, d\alpha = \frac{2K1}{\pi}\cos\varphi$$

Since the waveforms E are half sinewaves, the mean value is

$$4)\ V'm = \frac{2\,K1}{\pi}$$

We can conclude that two causes contribute to give a TACHO signal lower than the theoretical one, both due to differentiator network :

a) the amplitude of the signal V_{MA} is lower than V_{MA} = Kω and we can call ε1 the relative percentage error.

$$\varepsilon 1 = \frac{\sin tg^{-1}\,\omega\,R5\,C6 - \omega\,R5\,C6}{\omega\,R5\,C6} \cdot 100$$

b) the mean value of the signals V_{MA} . sign V_{AB} and V_{MB} . sign V_{AA} is lower than the theoretical one because there is a shift in the phase of the signals V_{MA} and V_{MB}. The relative percentage error only due to the shift of the phase is

$\varepsilon 2 = (\cos\varphi - 1)\,.\,100 \quad \varphi = tg^{-1}\,\omega\,R5\,C6$

The total percentage decrease of the TACHO signal is given with a good approximation by the sum of ε1 and ε2.

Example :

Consider :

f = 3000Hz corresponding to

$n = \frac{3000}{200} \cdot 60 =$ 900rpm of the motor if 200 are the tracks/turn of the encoder

$\varepsilon 1 \cong -2.6\%$ with R5 = 820Ω

C6 = 15nF

$\varepsilon 2 \cong -2.6\%$

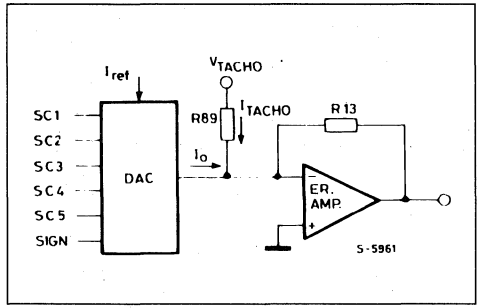
$\varepsilon 3 \cong \varepsilon 1 + \varepsilon 2 \cong -5.2\%$

From the diagram of fig. 21 we note that at a speed of 900 rpm corresponds a theoretical speed of 855rpm with a percentage difference of about 5.2%.

SPEED ACCURACY DUE TO THE D/A CONVERTER

To analyse the influence of the DAC precision on the speed accuracy we will refer to the following (fig. 25).

Figure 25.



The value of the output current of the DAC I_o depends on Iref and on the digital code defined by the inputs SC1-SC5, while its direction depends on the value of the SIGN input, the max theoretical value of I_o, obtained with SC1-SC5 low is :

$$I_{OM} = \pm \frac{31}{16} I_{ref}$$

The motor will run at a speed corresponding to the following value of the TACHO signal :

$$V_{TACHO} = -\,I_{OM}\,.\,R89 = \pm\frac{31}{16} I_{ref}\,.\,R89$$

This last relation is true if we don't consider the motor friction and the offsets. Consider now the possible friction and the offsets. Consider now the possible spreads we can have in the motor speed due to the DAC. If we call I_{OM1} the value of the max output current I_o corresponding to the SIGN LOW and I_{OM2} the one corresponding to the SIGN HIGH, the percentage error we have in the max speed from the positive to the negative value is :

$$\varepsilon 4 = \frac{I_{OM1} + I_{OM2}}{I_{OM}} \cdot 100$$

Note that we have consider the sum of I_{OM1} and I_{OM2} because they have opposite signs. This kind of error is principally due to a different gain of the DAC between the two conditions of the SIGN LOW and HIGH. An equal difference of I_{OM1} and I_{OM2}, from I_{OM} ($|I_{OM1}| - |I_{OM}| = |I_{OM2}| - |I_{OM}|$) doesn't constitute a speed error because this shift from the theoretical value can be compensated by adjusting the resistor R89 that is formed by a fixed resistor in series with a potentiometer.

With the guaranteed values on the L291 data sheet we can calculate for $\varepsilon 4$ the max value :

$$\varepsilon 4 = \frac{21\ \mu A}{1.4\ mA} \cdot 100 = 1.5\ \%$$

Another characteristic of a D/AC is the linearity, that in our case is better than ± 1/2 LSB. This value is sufficient to guarantee the monotonicity of I_o, and then of the speed of the motor, as a function of the input digital code. The precision of ± 1/2 LSB implies a spread of the speed at every configuration of the input code of ± 1.61% referred to the maximum speed. The max percentage error we can have is then greater at low level speed (±50% at min speed) and has its minimum value at the maximum speed (1.61%).

ACCURACY DUE TO THE ENCODER

The amplitude of the signals FTA and FTB determines the value of the TACHO signal. This amplitude must be constant on the whole range of the frequency, otherwise it is not possible to have a linear function between the TACHO signal and the frequency. The spread of the amplitudes of the two signals FTA and FTB between several encoder can be compensated by adjusting the potentiometer R9 (see fig. 12). The phase between the two signals should be 90°. If there is a constant difference from this value, a constant factor reduction of the TACHO signal results that can be compensated with the potentiometer R9. If the difference from 90° is random, also the reduction of the TACHO signal is random in the same way, and by means of R9 it is possible to compensate only the mean value of that reduction.

AN ECONOMIC MOTOR DRIVE WITH VERY FEW COMPONENTS

INTRODUCTION

The main objectives of this design are the economy and circuit simplicity which enable costs to be reduced to a minimum. For this reason the design is particulary suitable for domestic appliances powered by the 220 V AC mains. In this area, characteristics such as low cost, simplicity (and consequently greater reliability) have priority.

With these objectives the choice of the power switch is very important because the complexity of the drive circuit, the number and the power of the auxiliary supplies and the protection networks, depend on its characteristics. These factors lead to the decision to use a HIMOS device (an IGBT) as a power switch. The main characteristics of a HIMOS device are that:

- It switches high current with very low ON resistance, similar to a BJT (bipolar junction transistor).
- It is very rugged and has very large safe operating areas similar to Power MOSFETs.
- It has high overload current capability.
- It is easy to drive (like Power MOSFETs) consequently it is possible to drive it directly by means of popular linear IC.

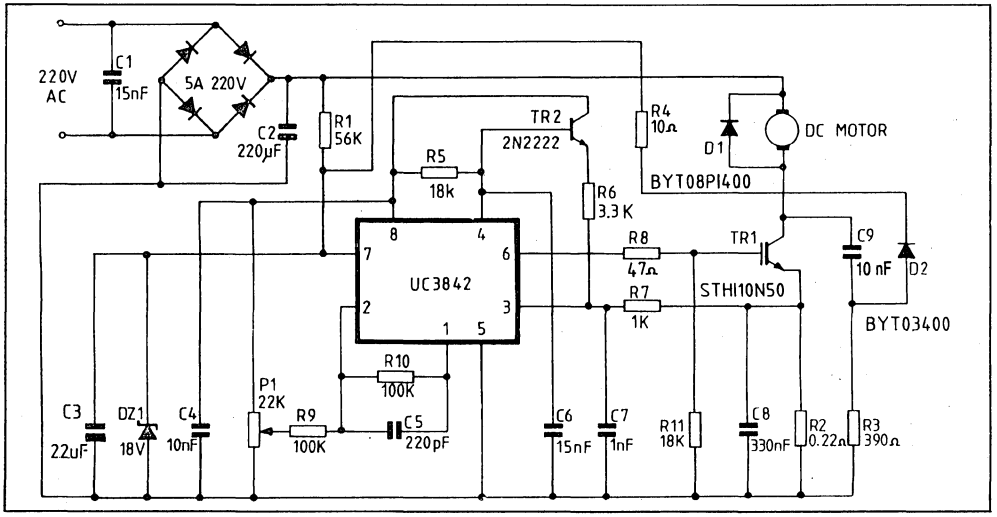
These characteristics are very suitable for motor drive applications in general and make HIMOS the new way of power switching in this area. An additional factor is that a HIMOS device has a smaller chip area than Power MOSFETs, or bipolar transistors with the same ratings ($V_{(BR)\,DSS}$ and $I_{DS\,max}$).

CIRCUIT DESCRIPTION

This DC motor drive circuit has a single switch topology and works in current mode; an STHI10N50 HIMOS is used as the power switch. The complete circuit schematic is shown in figure 1. Its main features are as follows:

- 300V, 4A DC permanent magnet step down motor drive
- Current mode PWM control
- Output current adjustable pulse by pulse from 0 to 4A
- 220 AC ± 10% supply voltage
- 6KHz switching frequency
- From 6% to 95% operating duty cycle

Figure 1: Circuit diagram of the HIMOS motor drive



The PWM controller IC used is STUC3842. It is a popular, economic eight pin IC widely used for off-line and DC to DC converters. STUC3842 provides the features necessary to implement fixed frequency current mode control scheme with a minimal external parts count.

Internally implemented circuits include under voltage lockout featuring start-up current less than 1mA, a precision reference, logic to insure latched operation, a PWM comparator which provides current limit control and a totem pole output stage. It can directly drive the gate of the 500V 10A HIMOS switch STHI10N50. The choice of this IC and its current mode working matches the requirements of economy and simplicity of this application.

Fig. 2 - STHI10N50 output characteristics (I step = 6V)

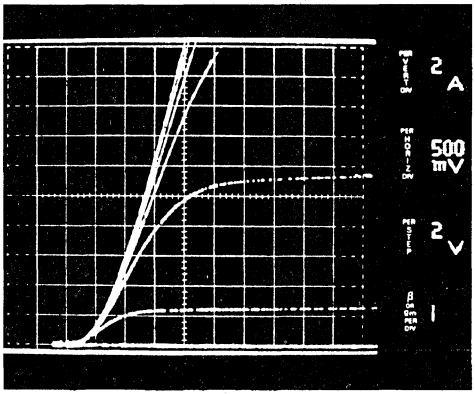
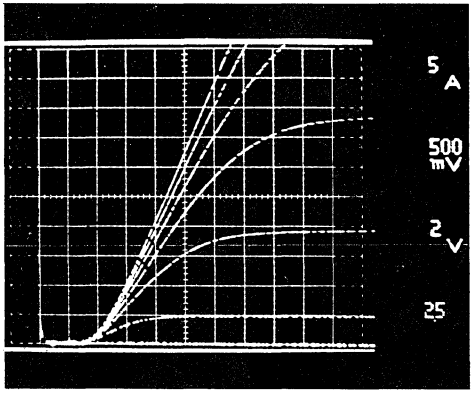


Fig. 3 - STHI20N50 output characteristics (I step = 6V)



The motor speed is controlled by the error voltage which is variable from OV to +5V, and is applied to pin 2 of the IC by means of R9. This voltage sets a constant current level at which the IC interrupts, pulse by pulse, the current in the power switch: the PWM control is therefore a "current mode" type. The HIMOS switch used is STHI10N50, for higher power motors STHI20N50 can be used simply by changing resistors R2 and R6 and free-wheeling diode D1. Figures 2 and 3 show respectively the output characteristics of STHI10N50 and STHI20N50 devices.

An important part of the circuit is the snubber consisting of R3, C9, D2. This accomplishes two functions:

a) it provides power for the UC3842 using the charge current of C9 during the STHI10N50 turn-off; infact the IC requires about 20 mA DC as supply current and cannot be biased simply through resistor R1 which should be 10Kohm 10W. Instead, using this active snubber, R1 can be set to a value of 56Kohm 2W in order to apply the start up power to the UC3842.

b) it reduces the energy dissipated in the power switch during turn-off; consequently a smaller heatsink can be used for STHI10N50 giving additional cost reduction.

To insure a continuous power supply to the IC, using the active snubber C9, R3, D2, it is necessary that the capacitor C9 must be completely discharged before turn-off. Because C9 is discharged by means of R3 during the ON phase of the power switch, there is a limit to the minimum ON time which cannot be less than 8 μs, consequently the minimum duty-cycle is 6%.

Considering a peak current I_p = 4A, a fall time t_f = 1.5 μs and the minimum ON time of 8 μs, the values of the snubber components are calculated as follows:

$C9 = (I_p \cdot t_f)/2V_{cc} = 10$ nF

$R3 = T_{on\ (min)}/2 \cdot C9 = 400$ohm

The power dissipated across R3 is:

$P = 1/2 \cdot C9 \cdot V^2 \cdot f = 3W$

The adoption of this snubber does not affect the efficiency of the circuit during normal operation because its power dissipation is very low and it has the additional benefit of using this energy to supply the IC so reducing the dissipation in the power switch. The extra cost is negligible with respect to the cost of a transformer for supplying the low voltage power to the IC.

The network of Tr2 and R6 adds a fraction of the ramp oscillator voltage to the "current sense" si-

gnal at pin 3 of the IC (via transistor Tr2 2N2222) to allow slope compensation. Consequently duty-cycles as high as 50% can be obtained.

Diodes D1 (BYT08PI400) and D2 (BYT03400) are fast recovery types and have been used in order to minimize stresses on the power switch.

MEASUREMENTS ON THE CIRCUIT

The DC motor drive was tested in several operating conditions. These were maximum and rated output current and in blocked rotor conditions.

The waveforms of the drain voltage, V_{DS}, drain current, I_D, and gate voltage, V_G, both with and without the snubber can be seen in figures 5 and 6 respectively.

Fig. 4 - STHI10N50 turn-off with snubber I_d= 1A/div, V_{ds}= V50/div, V_g=5V/div

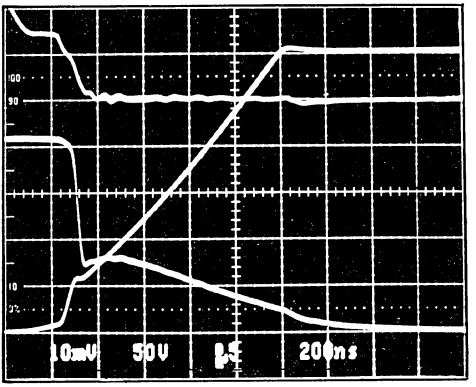
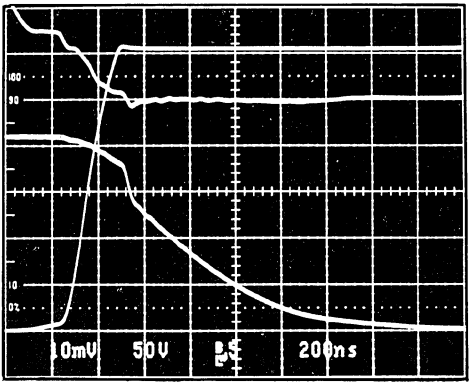


Fig. 5 - STHI10N50 turn-off without snubber I_d= 1A/div, V_{ds}= 50V/div, V_g= 5V/div



Here you can see the typical behaviour of a HIMOS device at the turn-off when typical features of both Power MOSFET and BJT are involved. The storage phase of the turn-off is dependent on the MOS behaviour as the base collector junction of the PNP transistor is reversed biased: the gate voltage decreases to a point where the Miller effect begins to control the current in the drain and V_{DS} start to rise. The fall time phase can be divided into two parts: the first part is the MOS turn-off and is very fast, the second is slow and starts when the MOS channel is closed and the PNP transistor has an open base turn-off and is dominated by recombination of excess carriers. Therefore the first part of the time is controlled by the gate drive circuit, the second part is dependent on the PNP transistor life-time and gain.

Since the PNP gain increases as V_{DS} increase, the fall time consequently varies with V_{DS}. Therefore, when the snubber is used and the V_{DS} slope is dominated by the capacitance, the fall time region due to the MOS is more evident (figure 6).

Figure 6 shows the turn-on behaviour of the HIMOS: it very fast (t-rise 30ns) and, as with Power MOS devices, is a function of the impedance of the driver circuit and the applied gate voltage.

Fig. 6 - STHI10N50 turn-on I_d= 1A/div, V_{ds}=50V/div

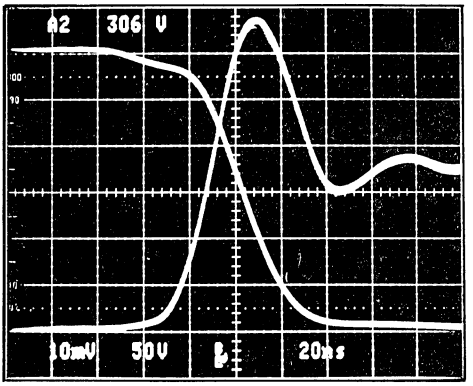
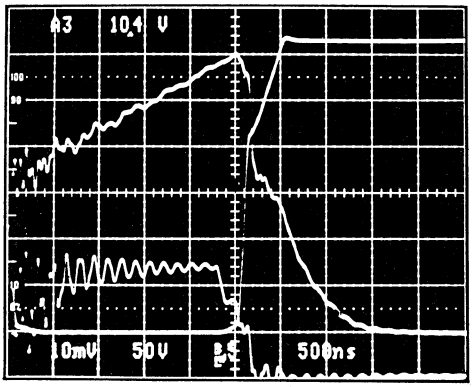


Figure 7 shows the behaviour in the case of a blocked rotor and with the current control set at the maximum 4A. This condition was simulated, as worst case, with and inductance of 300uH and a resistance of 1 Ω: the current does not exceed 6A. The overcurrent of 2A, with respect the control current of 4A, is due to the delay introduced by the network

of R7, C7 of about 2 μs. This filter network is necessary to suppress the leading edge spikes on the IC current sense comparator input.

Fig. 7 - Blocked rotor' beheaviour I_d= 1A/div, V_{ds}= 50V/div, V_g= 5V/div



The losses in the circuit, for the maximum rating of each component are approximately as follows: P(R1) = 2W, P(R3) = 3W, P(R2) = 3W, P(D1) = 4W, P(Tr1) = 7W.

CONCLUSION

A 300V 4A DC permanent magnet single quadrant motor drive was developed with objectives of maximum circuit simplicity and economy. Consequently a current mode PWM control with a popular IC was adopted and an STHI10N50 HIMOS (an IGBT) was used.

The low drive energy requirement due to the high input impedance of the HIMOS allows substantial cost reduction in the control circuit. Conductivity modulation of the drain produces a low ON resistance, an essential feature to work with high peak currents in the switching element. The ruggedness, due to the excellent safe operating areas, is especially relevant for motor control applications.

The easy drive, high current handling and excellent ruggedness make HIMOS the new way of power switching in the motor control field.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

VERSATILE AND COST EFFECTIVE INDUCTION MOTOR DRIVE WITH DIGITAL THREE PHASE GENERATION

B. Maurice/JM. Bourgeois/B. Saby

INTRODUCTION

The three phase induction motor is a simple design, rugged, maintenance-free which appears in home appliances requiring cost effective solutions. For speed control of these motors, a frequency variation of the inverter output voltage is required. The voltage/frequency ratio must be maintained constant, so control of these motors normally require complex control circuitry for the generation of the balanced three phase sine wave outputs.

Usually the generation of the three phase PWM signals may be controlled by a dedicated circuit, such as the SGS-THOMSON L6234, which is driven by a separate microcontroller. This solution is optimum while performance prevails over cost.

The solution demonstrated in this application note is a simplified solution using a standard ST9 microcontroller which includes large on-chip ROM memory and an internal Direct Memory Access (DMA) controller. This combination reduces the need of dedicated ICs (hardware being replaced by software), and allows over 50% of the CPU time to perform control, environmental and supervision tasks.

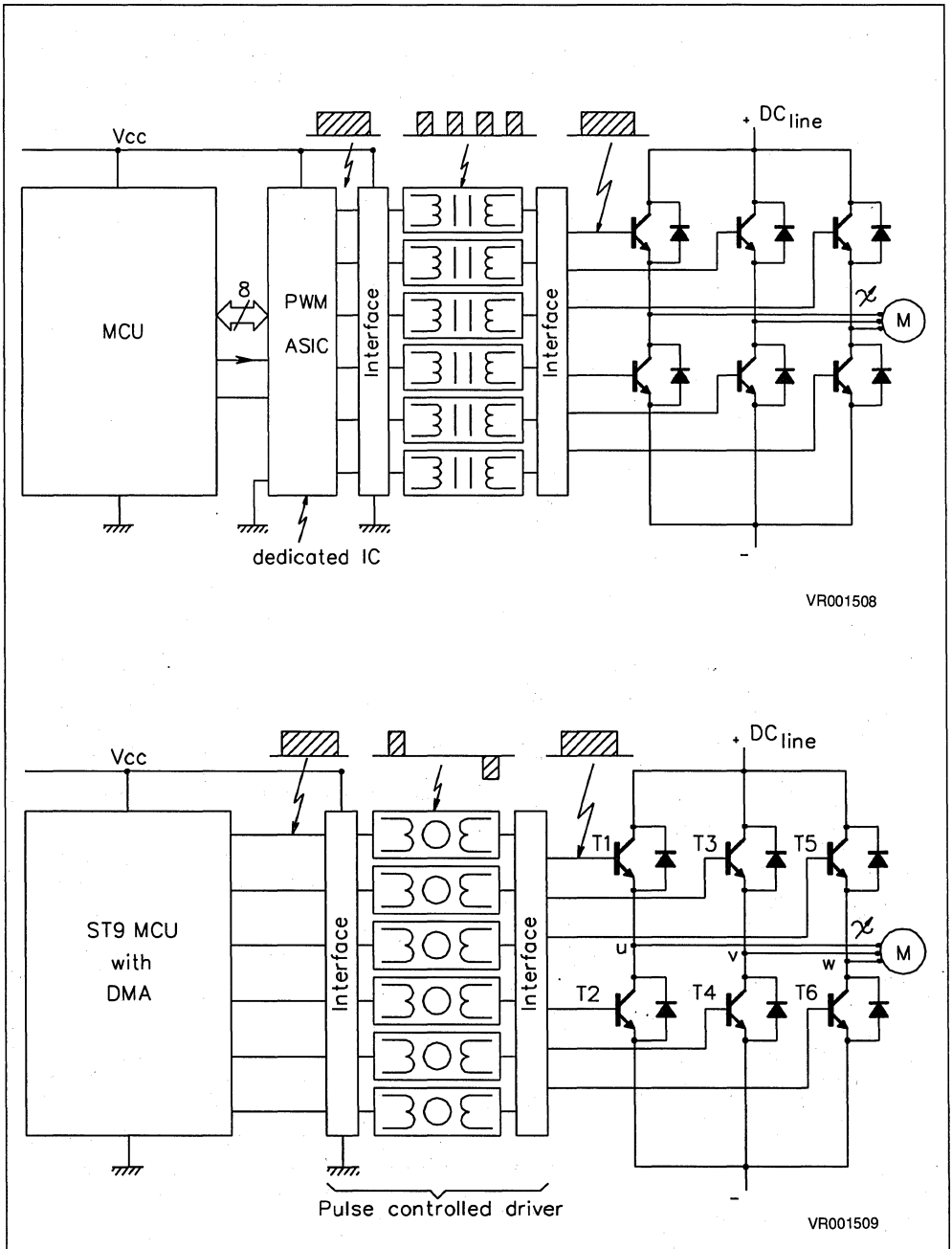
A practical solution to quantize three phase sine-waves, and to create the corresponding DMA table is shown allowing motor voltage and motor frequency to be chosen independently. A dead time avoiding cross conduction through the bridge is also created by software. Very low acoustic noise operation can be achieved despite a switching frequency below 10kHz, due to a shifting of the switching instants leading to a virtual doubling of switching frequency.

Each of the six digital outputs of the ST9 sets directly the state of the six power MOSFETs (or IGBTs) of the bridge via an insulated interface. This interface is described in the second part of this note. The fully isolated pulse controlled gate driver requires no floating auxiliary supply, meets safety standards and achieves a large dV/dt immunity.

Figure 1 shows how to generate a three phase sine wave by modulation of pulse width. This modulation is often obtained with a special dedicated IC controlled by a MCU (above).

Using a MCU having large memory integrated on the chip combined with DMA, spares the use of dedicated IC (below). Hardware is replaced by software. The sine waves are directly synthesized by the MCU.

Figure 1. Three Phase PWM Generation Techniques



DIGITAL CONTROL OF POWER SWITCHES

In this proposed solution, the ST9 microcontroller controls simultaneously the ON- and OFF- states of the six power switches of the inverter bridge. All these instantaneous ON-OFF states are stored in internal memory (ROM) and are sequentially transferred (every 5s for example) to six bits of a parallel output port by DMA (see Figure 2). The voltage level 0-5V of each output bit drives directly the gate interfaces of the six power switches .

All data corresponding to the switching duty cycle values is permanently stored in ROM and generates the quantized three phase sine waves. A dead time between adjacent Power switches is also stored, avoiding cross-conduction through the power bridge. The motor frequency and motor voltage are also stored independently.

The major part of the ROM is occupied by this permanent data, used to generate, step by step, the three phase sine-waves. This data is grouped in several tables (patterns), constituting series of bytes that have to be sequentially output on the parallel output port. A full scrolling of each pattern corresponds to a complete switching basic cycle of the six power switches. This is repeated the necessary number of times to complete the step duration of sine wave. The following pattern will then be scrolled to realize the following step.

This direct sequential transfer from memory to output port is performed by DMA [2], and is self operating. The central unit only works when the last byte of one pattern appears, the program then determines whether the same pattern must be scrolled again, or if another new pattern has to be scrolled.

All patterns needed for an application, as well as the program managing their scrolling order and their number of repetitions, are to be created and stored in ROM.

MOTOR DRIVE CONFIGURATION

Microcontroller

The ST9036 microcontroller from the ST9 family with 16k-byte of ROM or EPROM memory [1], of which only one output port and one multifunction timer are used for PWM generation. Six bits of its output port are gathered in pairs, one pair for every bridge leg (phases: u,v,w). The two bits remaining free can be used, for example, either to control two other power switches (i.e for heat control in a washer), or to generate a synchronized signal to perform measurement of V/I phase.

The ST9 microcontroller is able to manage two further functions:

a) Slow operations for motor and environment controls, such as timing of sequential operations, speed control, safety supervision tasks, etc. (These are not detailed in this application note).

b) Faster operations for real time management of the states of the power switches for PWM generation.

All others functionalities of the ST9036 remain available, such as other I/O ports, Timers, Analog/Digital converters and all interrupt functions.

Figure 2. DMA Transfer to control power switches

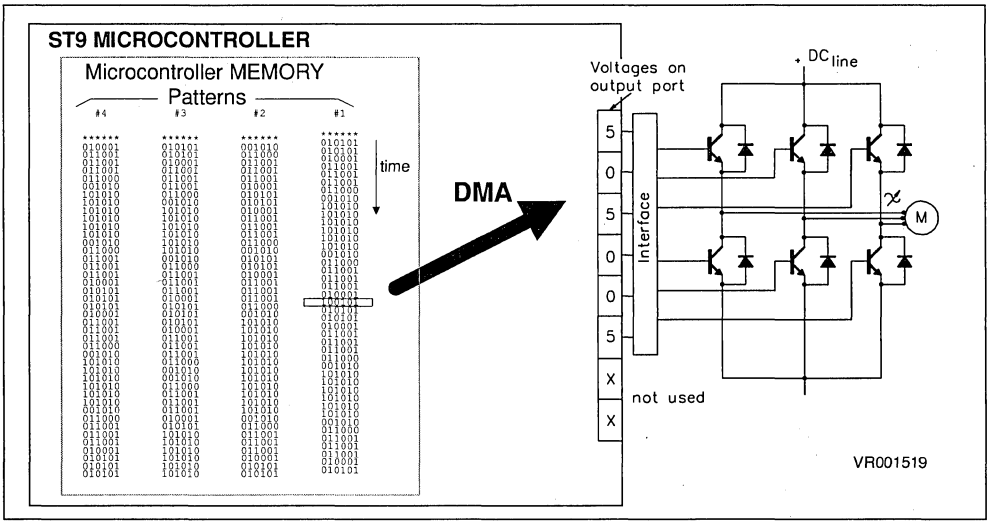
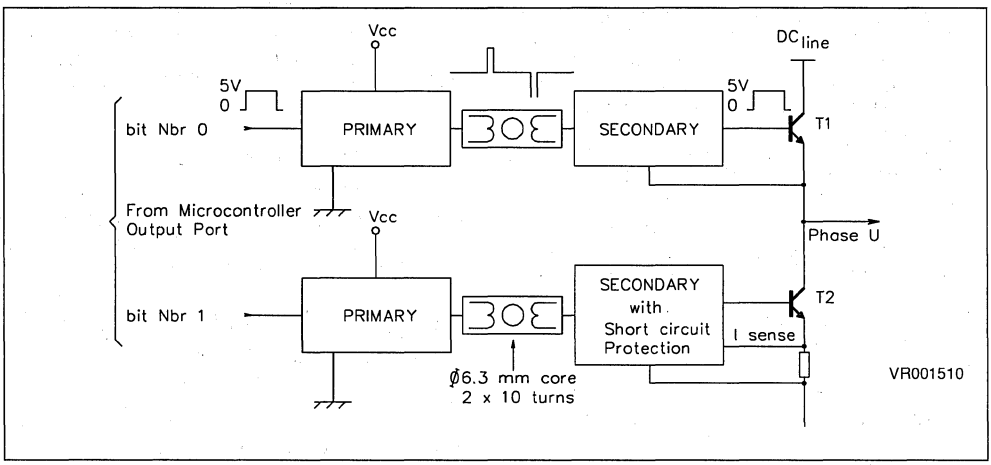


Figure 3. Driver for one Bridge Leg



In the practical example described in the following sections, ST9 is not heavily occupied by these real time operations:

- Using DMA is similar to slowing down the ST9 and engages only 35-40% of the CPU time.
- Speed control (frequency variation) needs only few instruction lines but no memory space. The memory space is mainly used to store necessary data to generate six various three phase voltages supplying the motor (1k-byte for each voltage).

Drivers For Power Switches

The driver interfaces the ST9 output port to the gate of the power switches.

- it converts the output level (5V) to the required gate-source voltage level (15V) of IGBT or Power-MOSFET.
- it provides a galvanic isolation.
- it protects against current surges and short circuits.

It is constituted by six independent circuits for the six power switches. Each is a pulse controlled driver [4] including: (see Figure 3)

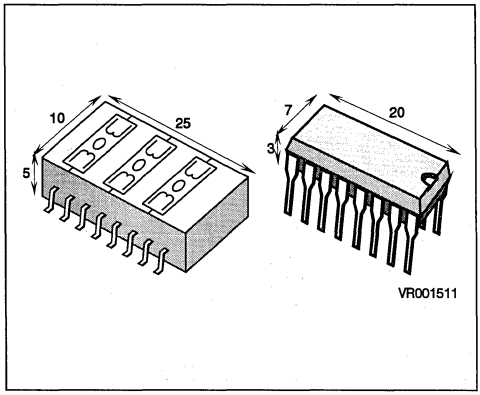
- a primary circuit to create a calibrated Pulse with short duration.
- a small pulse transformer. (DIL molded package)
- a floating secondary circuit operating without any auxiliary supply and including the autonomous short circuit protection.

The primary circuit differentiates the logic level input signal. The positive and negative calibrated output pulses (±15V/0.5µs) correspond to the switch-on/switch-off command. The primary circuit output stage is a full bridge having a low output impedance in order to obtain short rise times and high amplitude current pulses.

The pulse transformer can be small. A ferrite core of 6.3mm diameter with 10 turns is sufficient as it has to sustain 15V for 0.5µs. In this application, three core transformers are housed in the same standard or SMD package [3].

The secondary circuit needs no supply and uses the input gate capacitor of the Power-MOSFET or IGBT like an R/S memory.latch. The required energy is limited to charge and discharge the input gate capacitor. During the OFF-state, a low impedance is maintained across the gate-source of the Power switch, avoiding any reconduction due to externally applied dV/dt.

Figure 4. Transformer Core Size vs 16 pin DIL



In several applications, when isolation between the power and control sections is not mandatory, the low side driver can be a simple non-insulated driver. Nevertheless, the fully isolated solution performs high dV/dt immunity and meets insulation standards.

DC/AC Inverter

For this function, a three-phase bridge with six switches (Power-MOSFETs or IGBTs) is used. (Figure 1). The two switches of each bridge leg are opposite phase controlled. A dead time, avoiding simultaneous conduction, is generated directly by the ST9036 microcontroller.

Sine wave generation: (Figure 5)

The voltage on middle point of "u-phase" bridge leg is given by:

$V_u = V_{DC}.\delta_u$ $\quad \delta_u$ = u-phase duty cycle

$t_{on\ hi}$ = "ON state" duration of high side switch

$\delta = t_{on\ hl}/T_s$ $\quad T_s$ = switching period

$V_{uw} = V_u - V_W$ $\quad V_{uW}$ = phase to phase motor voltage

If δ_u is sinusoidal modulated, the average voltage on half bridge middle point describes sinusoidal wave form centered to $V_{DC}/2$. To avoid DC components in the motor, each phase voltage has to be symmetrical compared to $V_{DC}/2$.

Motor voltage value

Motor voltage is maximal when the duty cycle modulation varies from 0% to 100% (modulation depth: K=100%)

Motor voltage is minimal (nil) when modulation depth K=0; δ does not vary and is equal to 50% (Figure 5b)

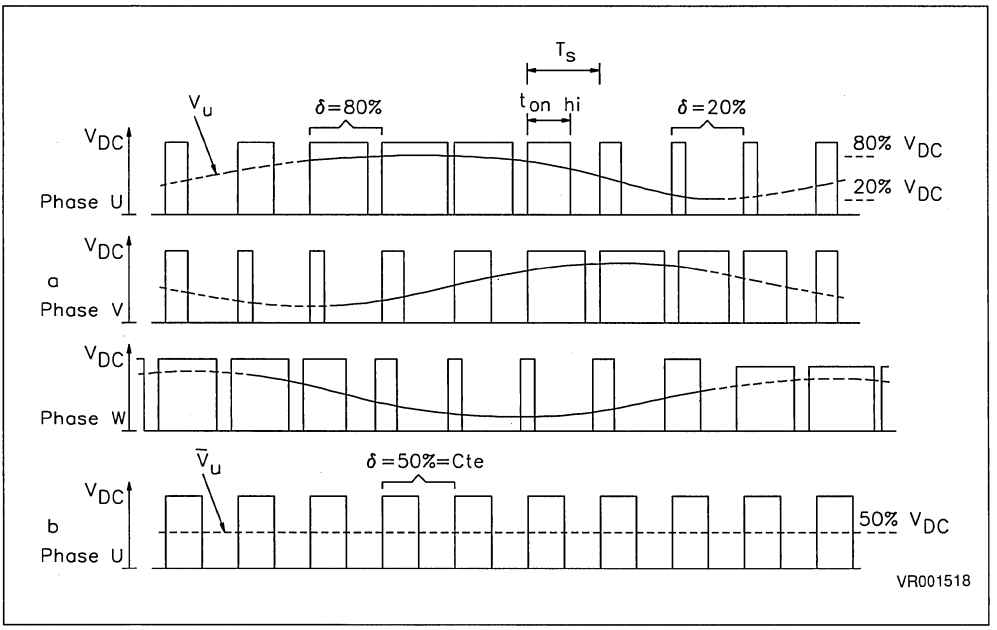
Sine wave frequency variation

This is obtained by varying the frequency of the duty cycle modulation.

CREATING TABLES OF DATA

The variable speed drive of induction motors requires generating three voltage sine waves and control of their amplitude, phase and frequency. The first step is to digitize the three phase system in order to create all the necessary data to be stored into the ROM of the ST9 microcontroller.

Figure 5. Sine Wave Generation at the output of one bridge leg
a. Modulation depth 60%, duty cycle 20 to 80% **b. Constant duty cycle**



Fundamental period quantification

The fundamental period of motor voltage is divided into 24 "segments"; (each segment equals 15° of arc). This gives a good sine wave accuracy in many applications. During each "segment" the voltage is a percentage of the DC line voltage, given by duty cycle (δ). For example, the duty cycle must be 55% during the segment from 165° to 180° for phase U (Figure 6).

Creating the duty cycle table

The second step is to establish a table giving, for each segment, the duty cycle value (δ) for each of the three phases. In fact δ1, δ3, δ5 are duty cycle values for each high-side switch (T1, T3, T5). The low side switches are in the opposite states and their duty cycle value is complementary to 100%. This entire table defines exactly the three-phase sine wave system during one period (T_O) and for one motor voltage. (Figure 7) These table values respect phase balance and avoid neutral currents. To achieve these conditions it must be ensured that:

a) on each line, the sum of the three duty cycle values is constant (equal to 150%).

b) The duty cycle has a symmetrical value either side of 50%. In practice the quantized values have to be chosen close to the mathematical value of sinus for only a quarter of the period, then symmetrically repeated respecting the condition (a).

This duty cycle table is not stored in ROM. It only defines the necessary data to create the patterns. One line of this table defines one pattern (see following section).

Figure 6. The fundamental period divided into "segments"

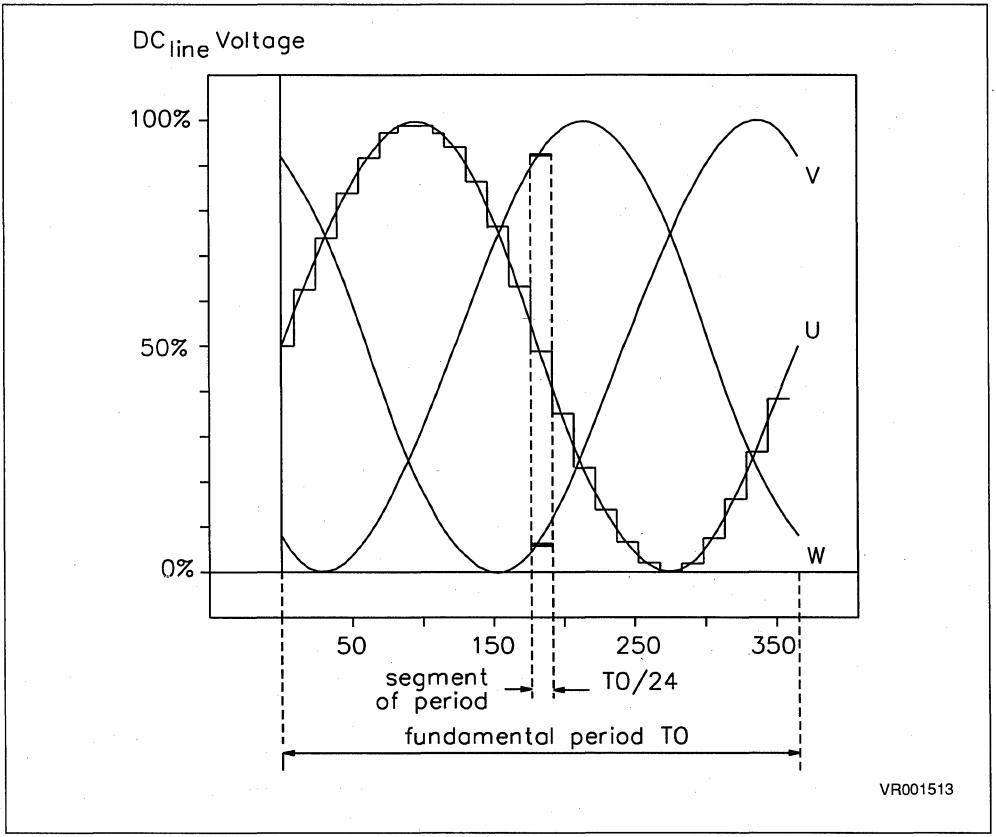


Figure 7 . Duty cycle table defining data to create patterns $V_{PHASE} = 0.6xV_{LINE}$

Pattern #	U δ1%	V δ3%	W δ5%
1	80	40	30
2	80	45	25
3	75	55	20
4	70	60	20
5	60	70	20
6	55	75	20
7	45	80	25
8	40	80	30
9	30	80	40
10	25	80	45
11	20	75	55
12	20	70	60
13	20	60	70
14	20	55	75
15	25	45	80
16	30	40	80
17	40	30	80
18	45	25	80
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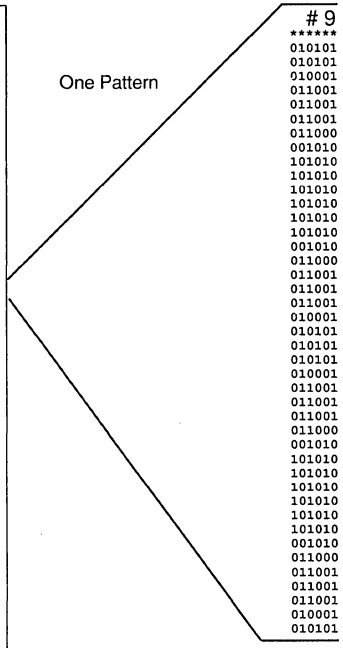
20	60	20	70
21	70	20	60
22	75	20	55
23	80	25	45
24	80	30	40



Pattern definition

A pattern is a succession of bytes stored in memory. Each bit (1;0) of these bytes gives the instantaneous state (ON;OFF) of each of the 6 six power switches (Figures 7&9). Pattern contains number of bytes necessary to define one entire basic switching cycle.

A particular pattern has to be created for each segment of the sine wave period. All these patterns are stored in the ST9036 ROM.

For example (Figure 8), a pattern contains sequence of 42 bytes defining one basic switching cycle. The switching period T_s, shared into 42 units of times, gives a good sensibility of duty cycle adjustment of about 2.5% (1/42th). This time unit corresponds to the rhythm of the DMA timer and its duration is chosen as a multiple of the ST9 microcontroller clock period (0.25µs).

In this example, one unit of time equals 4.75µs in order to have a pattern scrolling time or switching period T_s = 200µs. This corresponds to 5kHz of switching frequency.

Two dead times (one time unit each) at every state change of adjacent switches avoid cross conduction of the bridge leg.

Figure 8. Example of switching cycle for transistor T1

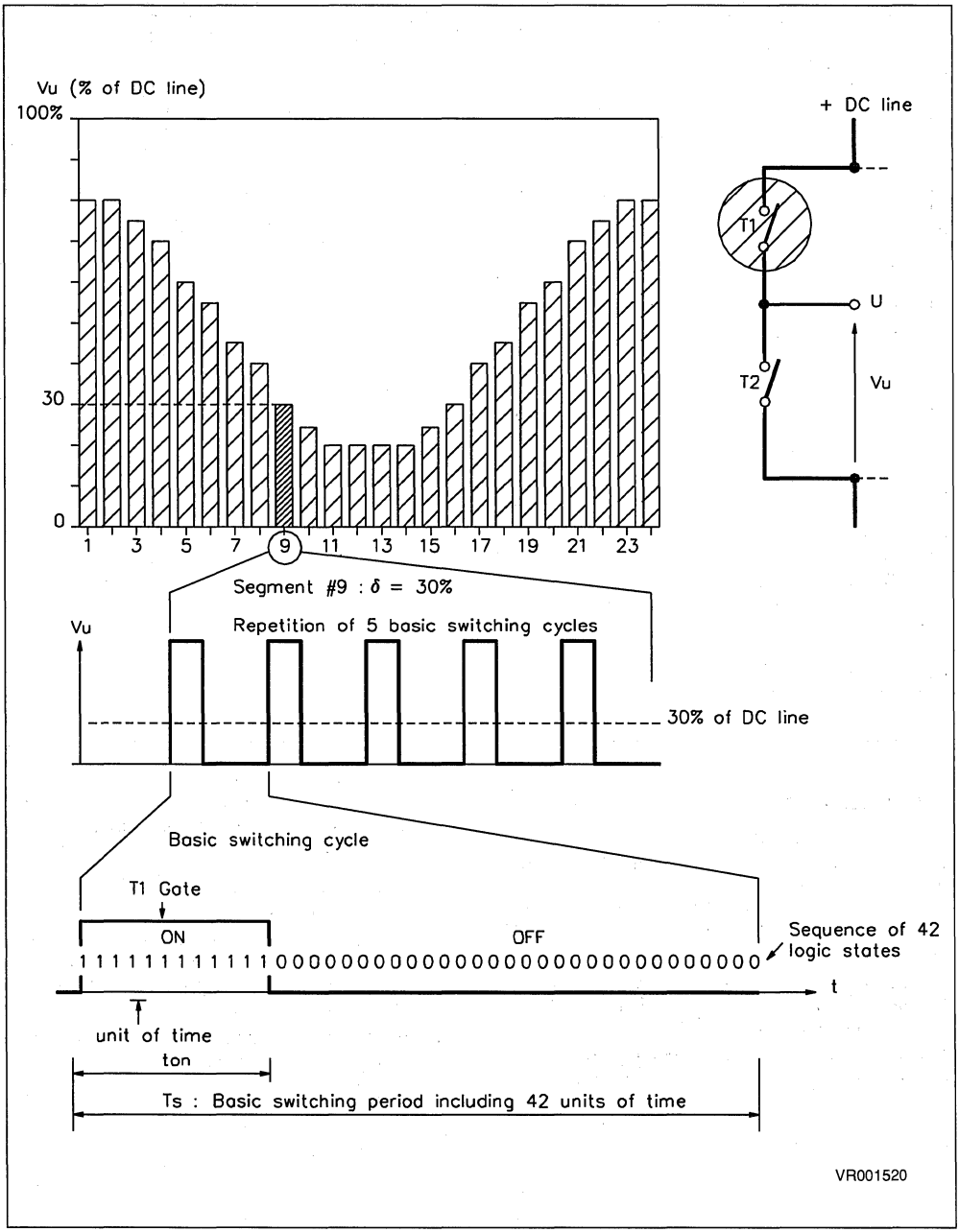


Figure 9. Pattern table

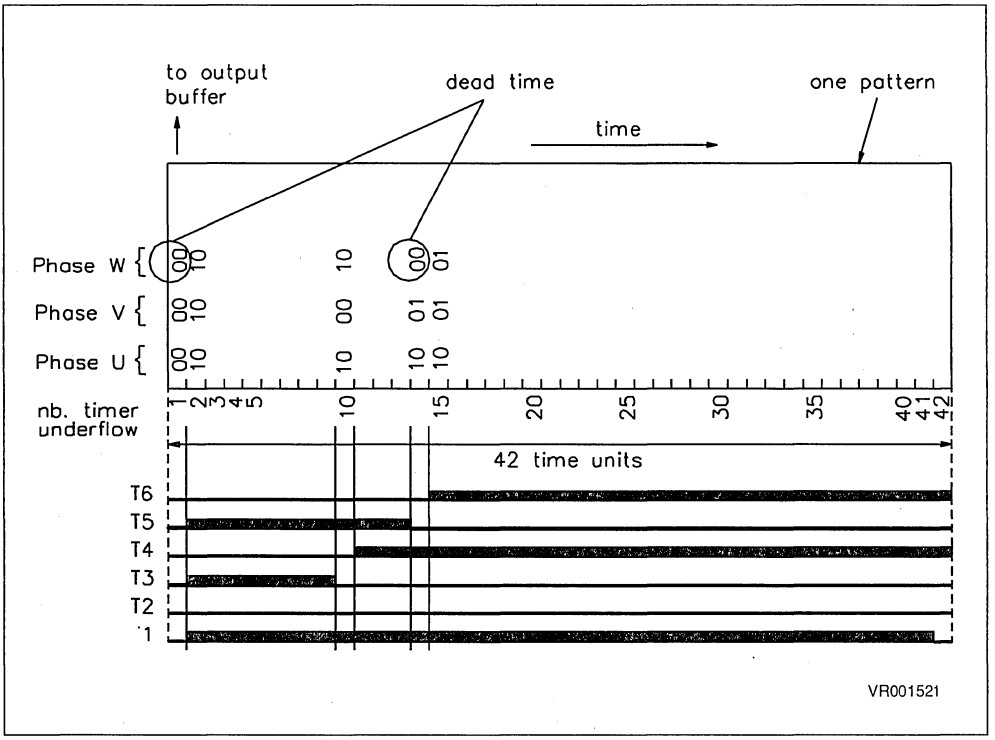


Figure 9: One pattern is an elementary table grouping all necessary bits to define the basic switching cycle of every six inverter switches. Bytes are sequentially read by DMA, and transferred to the output buffer. The resulting switching cycles shown on the bottom of the figure gives the following duty cycles:

-phase U: $\delta 1$ (T1) = 100% ; $\delta 2$ (T2) = 100% - $\delta 1$

-phase V: $\delta 3$ (T3) = 20% ; $\delta 4$ (T4) = 100% - $\delta 3$

-phase W: $\delta 5$ (T5) = 30% ; $\delta 6$ (T6) = 100% - $\delta 5$

MOTOR VOLTAGE CONTROL

One table of duty cycle defines the 24 stored patterns (set of patterns) containing information to one AC motor voltage. As an example, the peak value of phase voltage generated by the table given on Figure 7 is equal to 60% of V_{DC} line. It is necessary to create a set of patterns for each of the needed motor voltage.

The motor voltage can be controlled independently of the frequency. This voltage depends on the set of pattern which the DMA is reading. By storing within ROM and reading different set of patterns, the voltage across the motor can be changed and shaped. In this example, a set of patterns includes 24 patterns of 42 bytes each = 1008 bytes.

Figure 10 shows $\delta 1$ duty cycle of the T1 switch for various values of motor voltage. On the right side the chart gives the corresponding values of $\delta 3$ and $\delta 5$. Each line of these charts defines a pattern. These values respect the phase balance and avoid current in neutral line. The useful RMS voltage across motor phases is given by:

$$V_{RMS} = \frac{1}{2}.K.\sqrt{\frac{3}{2}}.V_{DCline}$$

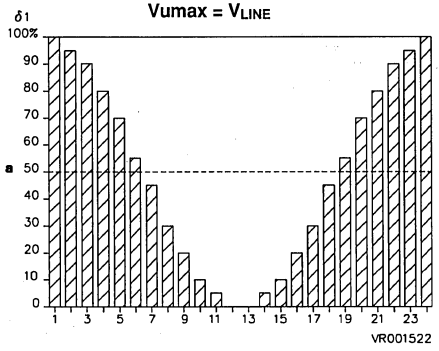
The K factor corresponds to modulation depth of the duty cycle (δ) as shown on examples (a,b,c).

a: K= 1.0 when duty cycle varies from 0% to 100%

b: K= 0.6 when duty cycle varies from 20% to 80%

c: K= 0.2 when duty cycle varies from 40% to 60%

Figure 10. δ1 Duty Cycle of T1 Switch



Set of Patterns

Pattern	δ1	δ3	δ5
1	100	30	20
2	95	45	10
3	90	55	5
4	80	70	0
5	70	80	0
6	55	90	5
7	45	95	10
8	30	100	20
9	20	100	30
10	10	95	45
11	5	90	55
12	0	80	70
13	0	70	80
14	5	55	90
15	10	45	95
16	20	30	100
17	30	20	100
18	45	10	95
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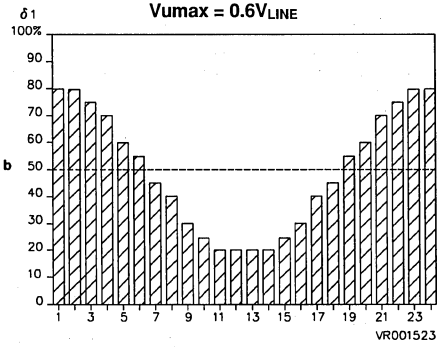
20	70	0	80
21	80	0	70
22	90	5	55
23	95	10	45
24	100	20	30



One Pattern

1	80	40	30
2	80	45	25
3	75	55	20
4	70	60	20
5	60	70	20
6	55	75	20
7	45	80	25
8	40	80	30
9	30	80	40
10	25	80	45
11	20	75	55
12	20	70	60
13	20	60	70
14	20	55	75
15	25	45	80
16	30	40	80
17	40	30	80
18	45	25	80
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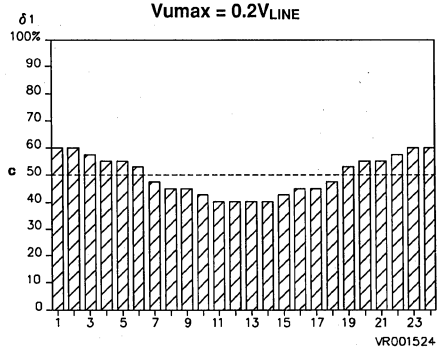
22	75	20	55
23	80	25	45
24	80	30	40



Set of Patterns

1	60	45	45
2	60	48	42
3	58	52	40
4	55	55	40
5	55	55	40
6	52	58	40
7	48	60	42
8	45	60	45
9	45	60	45
10	42	60	48
11	40	58	52
12	40	55	55
13	40	55	55
14	40	52	58
15	42	48	60
16	45	45	60
17	45	45	60
18	48	42	60
19	52	40	58
20	55	40	55
21	55	40	55
22	58	40	52
23	60	42	48
24	60	45	45

MOTOR FREQUENCY CONTROL

Motor frequency is controlled via duration of the fundamental period T_O.

The shortest duration of the period (the highest frequency) is reached when each segment of this period corresponds to only one reading of the corresponding pattern. In our example (Figure 11) the pattern reading duration equals 200µs, and with 24 segments.

When each segment corresponds to two readings of pattern, the fundamental period is twice as long. Thus the frequency (motor speed) can be controlled step by step whether the pattern is read once or several times. Consequently when starting from the highest frequency, it is possible to have discrete submultiples of frequency.

F = Fo/N N = number of times of patterns being read

The speed resolution is low for high motor speed, but high for low motor speed. So, to perform the speed control by software, it is sufficient to give the number of times the pattern is to be read. For example, when repeating 20 times the same pattern the following results are obtained:

4.75µs = time unit

42 = number of time units per pattern

20 = number of patterns (or switching cycle) reading per segment

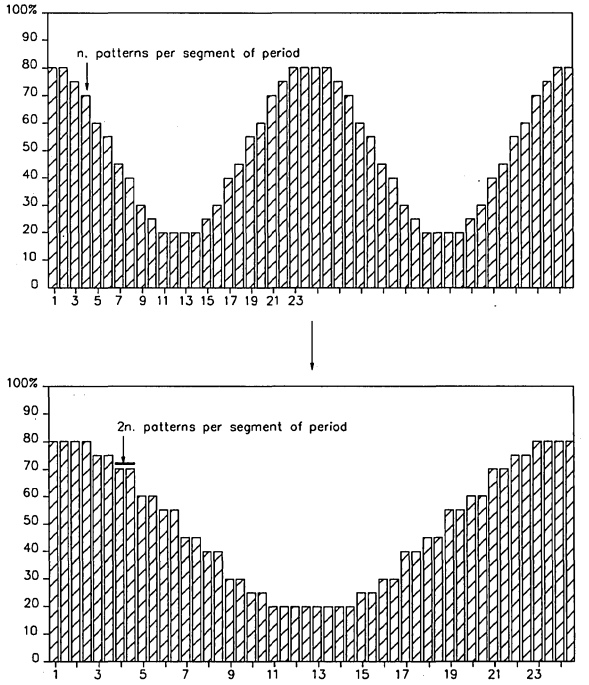
24 = number of segments per fundamental period

This gives a fundamental frequency of 10.4Hz

Another way to adjust motor speed by software is to change the DMA timer period. That is equivalent to modifying the "time unit" duration. The reduction of time unit duration is limited by the highest consumption of CPU time to be accepted and the shortest permissible dead time is according to power switches used.

By combining these two methods, pattern repetition and timer variation, it is possible to perform quasi-continuous variation of motor speed.

Figure 11. Fundamental Frequency variation
a. To = 200x24=4800 ms Fo=208Hz
b. To = 200x2x24=9600ms Fo=104Hz



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DEPHASING SWITCHING INSTANTS

When creating the pattern, the instant of switching can be chosen specifically for each bridge leg. For example it is possible to simultaneously turn-on all the high side switches (T_1, T_3, T_5) and stop them when respectively each duty cycle is reached (Figure 12a).

Through other ways for the same duty cycle the ON-state is centered at the middle of pattern (Figure 12b).

Various other possibilities can be chosen to create the pattern. The acoustic noise of the motor will depend on this choice. For example the pattern shown in Figure 12c gives a large current ripple and very noisy motor,while, on the contrary, Figure 12b gives a noiseless motor according to small current ripple (shown at 20ms/div; 2A/div).

When the three high side switches or the three low side switches are simultaneously ON or simultaneously OFF, no energy is transmitted into the motor, which is freewheeling. Another possibility is to choose simultaneously the OFF-state rather than the ON state simultaneously as shown Figure 12e to compare with Figure 12b. In this case two switches of one bridge-leg are not switched and switching losses are reduced.

Figure 12 shows how various possibilities can be chosen for pattern creation .
Current ripple and acoustic noise of motor will depend on this choice.

On the right side, motor current with:

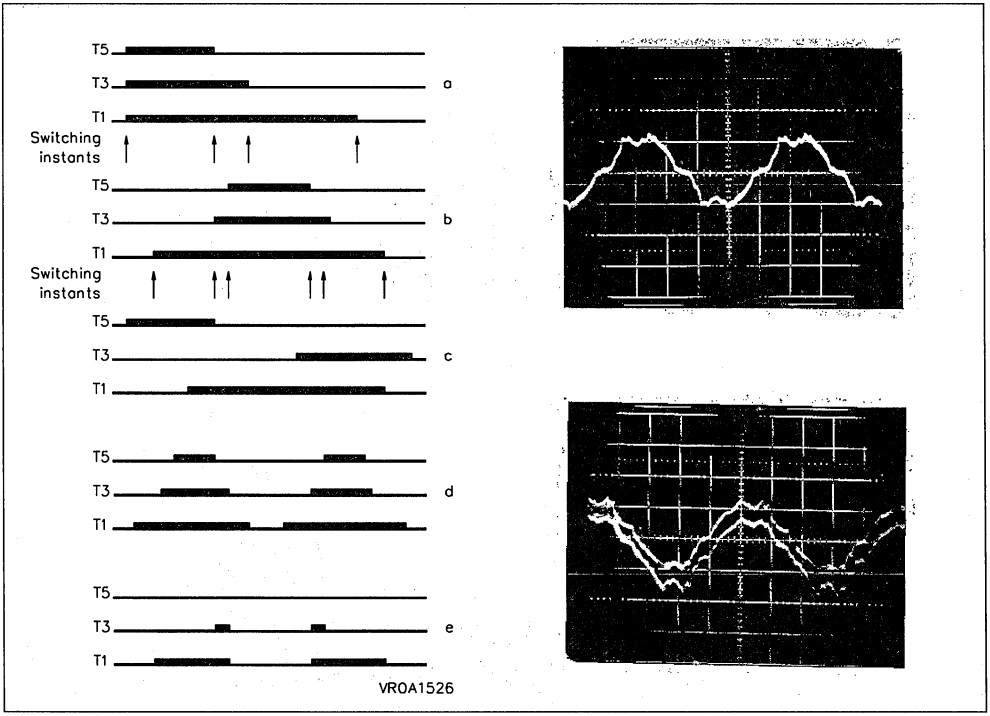
- noiseless motor according to small current ripple.
- noisy motor according to large current ripple.

As the energy is transmitted when switches are not in the same state, the rule to create a pattern is to maximize the instants where the switches are in the same state and simultaneously shift the switching instants.

All these methods can be used to obtain very low acoustic noise operation in spite of a switching frequency below 10kHz.

Without reducing the time unit, it is possible to increase the acoustic frequency by sharing in two equal parts each duty cycle time (δ=60% $\Rightarrow$ δ=30%+30%) . The switching frequency is doubled and acoustic noise is close to the inaudible region and becomes very low (Figure 12d)

Figure 12. Pattern options affecting ripple and acoustic noise



EXPERIMENTAL EXAMPLES

Figure 13 shows an example of generated three phase PWM signals on microcontroller outputs. It represents three control signals for T1, T3, T5. The set of pattern corresponds to a modulation depth of 100% as shown on table Figure 10a. The phase angle between each phase is 120%.

Figure 14 shows current measured in motor phase (20ms/div, 2A/div).
a) obtained with set of pattern shown on Figure 10b, and repeated twenty time, f=10Hz
b) patterns are repeated twice, f=100Hz.

The used set of pattern (at 60%) of Figure 10b, combined with doubly of switching instants (Figure 12d), gives a well defined sine wave.

Very little ripple of current and doubling switching frequency give a noiseless motor operation.

The motor is speeded up by repeating patterns only twice (Figure 14b). Simultaneously the motor voltage is increased by using set of pattern (Figure 10a) having modulation depth of 100%.

Figure 13. Three microcontroller outputs: 5ms/div, 5V/div

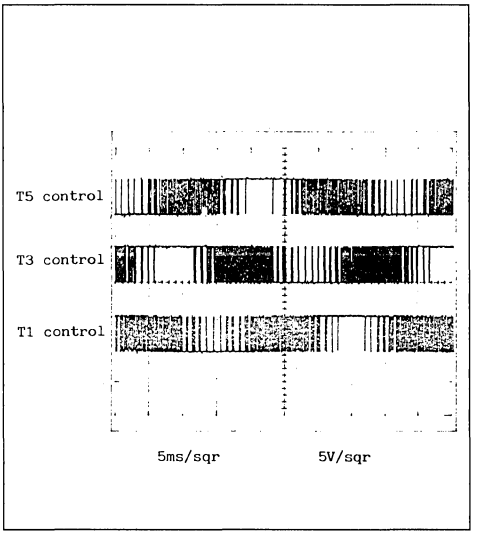
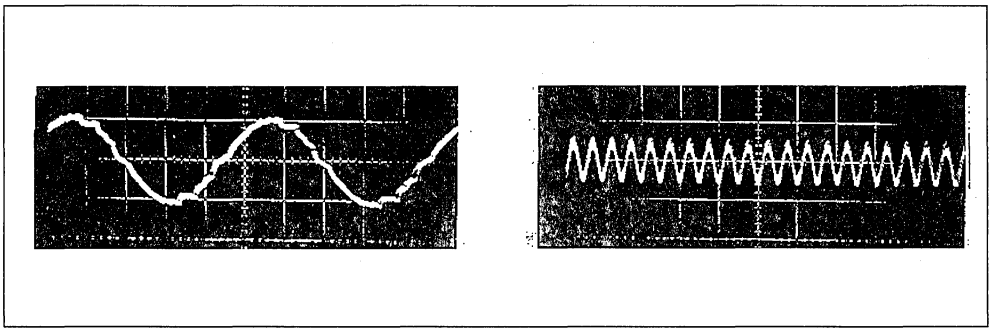


Figure 14. Current measured in motor phase



SUMMARY

For large volume applications such as washing machines, air conditioning or cooling pump motor drives, cost optimization is a key issue. The solution to drive induction motor presented in this paper simplifies conventional digital solution. Using a ST9 microcontroller with Direct Memory Access and fast data transfer, replaces dedicated ICs by software or more precisely by data stored in microcontroller memory.

The proposed solution is very versatile because a standard microcontroller, the ST9036, can be programmed for various applications, only the software will has to be adapted.

This note presents methods to generate data in order to shift the switching instants of inverter switches. This allows to reduce motor acoustic noise in spite of switching frequency being below 10 kHz, and to minimize motor and converter losses.

The described pulse controlled gate driver uses standard components and small enough core transformers that can be fitted into a Surface Mounting Package. This way offers a cheap fully galvanic insulation when required.

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APPENDIX MICROCONTROLLER WITH DMA

The feature of microcontroller with DMA (direct Memory Access) consists in having a possibility of direct access between microcontroller memory and its on-chip peripherals. Moreover, one of the parallel I/O ports can be coupled with the timer's DMA channel, allowing fast data transfers between memory and this I/O port with minimum CPU overhead. Data transfers are scheduled by the timer.

The only task of the Microcontroller software is to specify which pattern is to be read by the DMA channel at a given time in order to reproduce the three-phase sinewaves, as described in the previous sections. After a complete pattern transfer, the Micro-controller CPU is interrupted (DMA End of block interrupt) and the DMA should start to read the next pattern.

In order to achieve high speed continuous transfers without stringent response time requirements for this End of block interrupt, a "swap mode" is used: while a pattern is read by the DMA channel, the subsequent pattern can be prepared in advance; so, once the last byte of the pattern is read, the DMA automatically switches to the new pattern while the old one can be updated during the DMA End of block interrupt routine.

First tests show that the DMA operation in swap mode, as described hereabove, accounts for 35-40% of the total available CPU time of the Microcontroller. Therefore, thanks to its processing power, the Microcontroller can easily perform any control and supervision task in addition to this DMA-driven PWM generation.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

MOTOR CONTROL DESIGN USING VERTICAL SMART POWER ICs

by R. Letor, M. Melito, A. Galluzzo

ABSTRACT

Readily available smart power devices can greatly simplify a power designer's design task by releasing him from the problems of designing high current control circuits.

Whilst making this aspect of the design transparent to the user, smart power ICs only require a standard logic compatible input signal.

These features are illustrated by practical examples of motor control using two different circuit configurations, a single switch and a full bridge circuit, working in continuous and in switched current modes.

The paper demonstrates that the problems of motor control (stalled motor, overload, etc..) are simply and successfully resolved by using smart power devices.

The devices contain an integrated vertical current flow power MOSFET, high side gate drive, maximum current control, protection circuits and a diagnostic status output.

The input and output control functions directly interface to a microprocessor allowing comprehensive control and fault diagnosis of the condition of the load, i.e. short circuit, open load and overload.

Designs safe-guarding the circuit against extreme working conditions are considered, such as a power supply disconnection with an inductive load.

Finally, future developments in smart power IC design for motor control are reviewed.

1.0 INTRODUCTION

In many application areas such as robotics, process control, automotive actuators, etc, the DC motor control board is, in effect, a power peripheral device of a micro-processor or micro-controller system.

Attaining high current, low power dissipation and effective diagnostic feedback with these peripheral boards can be a problem.

Using smart power ICs helps to overcome these difficulties and, additionally, provides a bonus: compact designs due to the reduced circuit size as a result of the integration.

The technology, one of three Vertical Intelligent Power (VIPower^{TM}) technologies, that includes, on a single silicon chip, a vertical current flow power MOSFET and analog and logic circuits, has allowed different families of devices to be produced that satisfy a wide range of applications.

Integrating a sense-FET on to the smart power ICs allows very high current, equal to that of discrete power MOSFET devices, to be controlled, resolving the problems of high current sensing even at high switching frequencies.

This leads to the possibility of making a wide range of interesting devices in a variety of packages with high power dissipation, some of which can be surface mounted.

The integration of analog and logic circuits that perform the various protection, diagnostic and current control functions, permit the design of a system where the peripheral circuit protects itself and the motor.

The micro-processor is able to handle the motor being aware of its working conditions.

2.0 MAXIMUM CURRENT LIMITATION AND CONTROL.

Current sense together with current limiting circuits are necessary in motor driving circuits, both for protection problems in overload conditions and in motor torque control.

The delay, the accuracy and the working mode of these circuits can be varied according to the application requirements and with the working mode (switching or continuous).

2.1 CURRENT SENSING.

The following disadvantages of the standard current sense circuits using a sense resistor or a current transformer highlight the advantages of using an integrated current sense circuit with a sense-FET:

- there is power dissipation ($P_d=R_{sens}I^2$)
- a high peak voltage is generated across the stray inductance due to the high switching speed ($V_{peak} = L_{stray}$ di/dt).
- the noise tolerance of the control circuit is adversely affected due to capacitive coupling.

Figure 1 shows that the sense-FET works as a current mirror so only a part of the current flows through the sense resistor, hence the power dissipation in the sense resistor is very low. In addition to this the integrated device requires less wiring. As a result there is less stray inductance. This, in turn, means it is possible to design a current sense circuit for very high switching speeds. If linear and accurate current control is not necessary, other methods of current sensing, such as detecting the saturation voltage or monitoring the junction temperature of the power sensing element, can be successfully employed.

Figure 2 shows the generic block diagram of the SGS-THOMSON Microelectronics high side intelligent switch.
Figure 3 shows that when a smart power IC temperature sense circuitry protects the device to prevent its destruction in over-current conditions, the over-temperature circuit turns the integrated power switch off at a safe operating temperature (140°C). This type of protection depends on the ability of the device to dissipate heat.

2.2 CURRENT LIMITING WITH VIPower

The current limiting can be achieved using linear or chopper techniques. Both solutions allow the current control to be relative to an external command and/or to internal parameters (internal references, junction temperature, voltage drop across the power transistor during the on state, etc.) as shown in figure 4 and 5.

3.0 DRIVING HIGH SIDE N-CHANNEL POWER MOSFETs

A Power MOSFET used in high side configuration requires a voltage greater than the power rail, high enough to turn on the device in full saturation.
This supply can have different configurations depending on the working conditions.
There are different methods of generating this gate drive voltage.
The charge pump technique can be used which is suitable for the continuous working mode or there is the bootstrap circuit which is suitable for switching applications.
These techniques or a combination of them can be integrated into the control circuit of the VIPower ICs, but some integration problems must be considered.

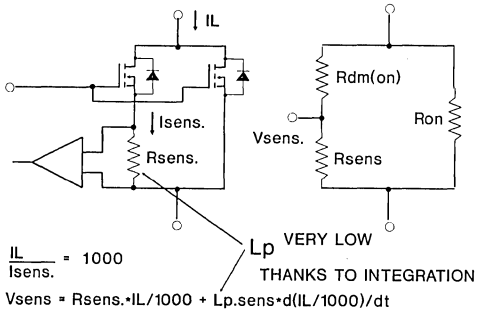

Figure 1 - Integrated current sense using a sense-FET and ON state equivalent circuit.

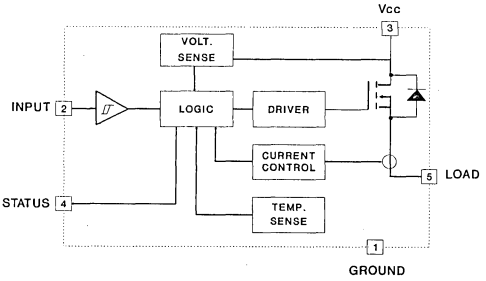

Figure 2 - Block diagram of a VIPower IC showing the main sense circuits.

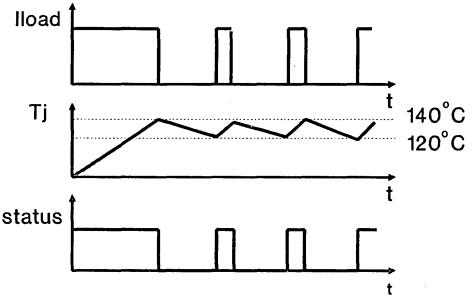

Figure 3 - Overload working mode of the VIPower intelligent switch, VN05

They are:

- the silicon area is proportional to capacitance value.
- number of pins must be limited to reduce the cost of the package.This means that the design of the drive circuit must be the best compromise between silicon area, number of pins and in the application under consideration that can have the following requirements:
- continuous working mode, switching working mode, or both.
- low switching losses (fast turn-on).
- low voltage applications typically 6 to 36V.
- complete turn-on of the power transistor in all working conditions.

Figure 6 shows the schematic of an integrated charge pump circuit that ensures sufficient gate-source voltage even if power supply is 5V or less.

This circuit multiplies the power supply voltage by three.

The integrated charge pump can only supply a few milliamperes and is therefore limited to use in continuous mode applications (i.e. solid state relays) because it needs a few hundred microseconds to generate enough charge to turn-on a Power MOSFET.

For switching applications, an external bootstrap capacitor can be connected to an internal control circuit, and, to ensure 100% duty cycle, both the charge pump and the bootstrap methods can be used (figure 7).

Figure 8 shows the turn-on switching behaviour of a VIPower IC with a Power MOSFET output using a bootstrap circuit to generate the gate drive voltage.

The switching time can be optimized in order to match low switching dissipation and electromagnetic compatibility.

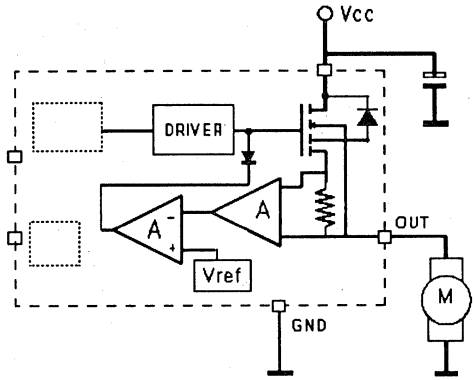

Figure 4 - Continuous current control in a VIPower IC

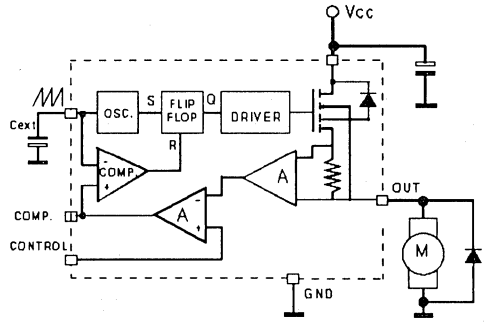

Figure 5 - Switched current control in a VIPower IC

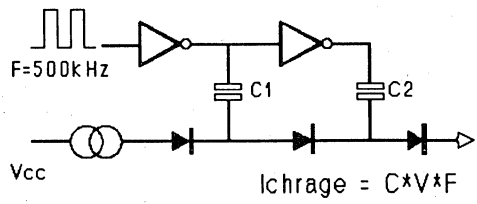

Figure 6 - Integrated charge pump that multiplies V_{cc} by 3.

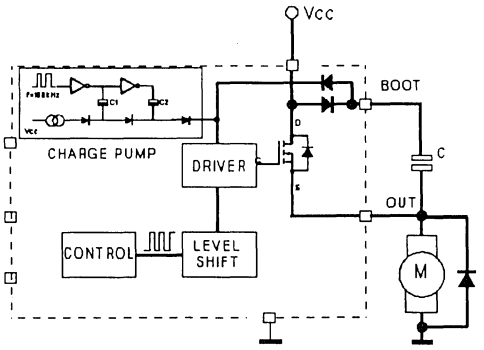

Figure 7 - Bootstrap and charge pump in a VIPower IC, allowing switching and continuous mode.

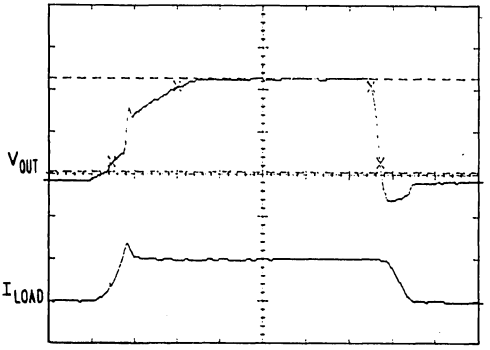

Figure 8 - Switching waveforms of output voltage and current in a VIPower IC V = 5V/div, I = 5A/div, t = 1 us/div

4.0 FAULT DIAGNOSTIC.

The ability to process the diagnostic information is very important in the design of fault tolerant systems.

In a motor drive circuit, this process can be complicated due to the changing working conditions of the motor and to the large variety of fault conditions, stalled motor, overload, open circuit due to the brush deterioration, etc.

The control circuit of a VIPower IC must be able to recognize these fault conditions and others, such as power supply failure, and differentiate between various fault conditions using a minimum of output pins and to be able to filter out false alarm signals.

This feature is achieved by the integration of a digital delay network and logic circuit that can, for example, operate as follows:

If a short circuit exists, when the device is turned on the VIPower IC internally limits the current and, after 33ms, it turns-off and the diagnostic output goes low.

If an open load exists (I_{out} < 50ma), when the device is turned on, then the diagnostic output goes low after 2ms.

If a fault condition appears during normal operation, the diagnostic output goes low immediately and the device turns-off.

If the device turns-off due to a fault condition, the control circuit must be reset by taking the input low.

These functions make it possible to discriminate between a false alarm signal given when the motor starts up and there is an in rush current or due to the inductive behaviour of the motor which can cause a low current for few µs.

By exploiting these features, it is possible to create a program able to interact with the VIPower IC and to identify the nature of the fault condition; this is illustrated in figure 9. A tri-state output can be used if only two fault conditions are to be identified.

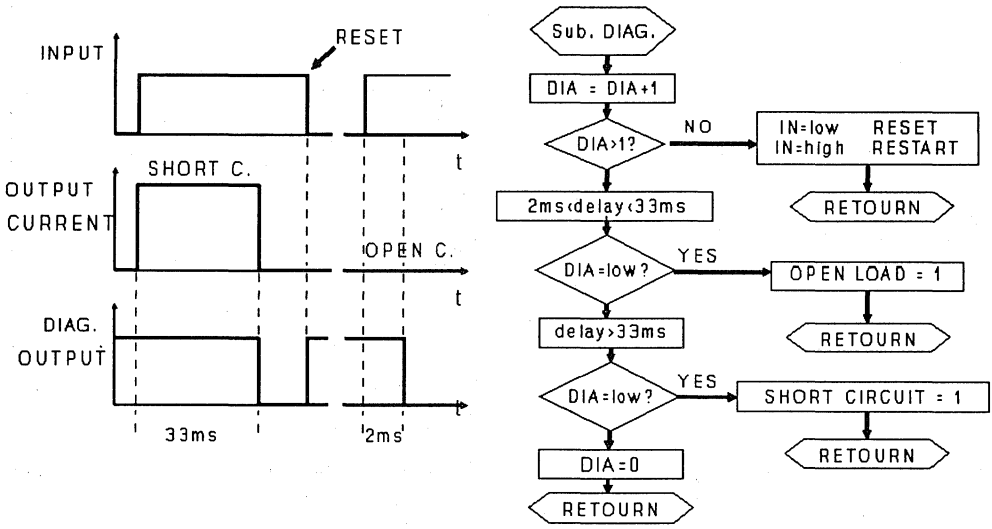

Figure 9 - Timing diagram of the diagnostic system in the VM201 intelligent switch and flow chart of a subroutine able to differentiate fault conditions.

5.0 MOTOR DRIVE USING TWO VERTICAL SMART POWER ICs IN A FULL BRIDGE CIRCUIT.

5.1 CIRCUIT DESCRIPTION.

The circuit in figure 10 shows how a very simple motor drive for an automotive electric window lift can be made using two high side smart power solid state relays and two discrete power MOSFETs in a full bridge configuration.

The SGS-THOMSON VIPower ICs used, VN05, have a very low $R_{DS(on)}$ (150 mΩ), maximum current limiting at 15A, under-voltage detection at 6.5V, thermal shut down (150°C), over-temperature and open circuit diagnostic output and a digital filter that makes the device able to distinguish between real and false fault conditions. The VM201, a power MOSFET plus the control circuitry integrated on to one silicon chip, provides all these features in a 5 pin HEPTAWATT package. Each half of the bridge is comprised of one VM201 and one standard power MOSFET.

The motor control board is CMOS and TTL compatible. This is possible because of the CMOS/TTL compatibility of the VIPower IC input and output and to the use of a low side CMOS buffer driver.

The free-wheel diodes are the intrinsic diodes of the discrete and integrated power MOSFETs. No power sense components are needed as the VIPower IC has an internal sense-FET.

In this application, the purpose of the diagnostic output (open collector), is to detect the stalled motor condition to protect the window at its extremes of travel and any accidental obstruction, eg an arm or dog!

This condition is characterised by an overload current caused by the stalled motor.
The ability of self decision of the VIPower IC and of interfacing software as shown in the previous section , 4, enables the circuit to filter a false stalled motor condition and to safeguard the power devices from over temperature stress.
Open load fault diagnosis can be used to recognize deterioration of the motor brushes.

5.2 BEHAVIOUR OF THE VIPower DEVICES.

The low $R_{DS(on)}$ (100mΩ), allows the devices to work at a high ambient temperature.
The worst case blockage of the window creates a current in the motor of up to 7A - 8A causing on-state power dissipation in the VIPower IC of 10W - 13W at a junction temperature, Tj = 100°C. This condition allows the devices to operate under the worst case conditions with a $R_{th\ junction\text{-}ambient}$ < 8°C/W, and with $T_{ambient}$ = 50°C. This avoids over-temperature detection during normal operation.
The figure 11 shows the behaviour of the current in the motor and of the diagnostic output during turn-on and turn-off. This behaviour is due to the overload current in the motor when the window reaches its limits of movement or is physically obstructed.

6.1 POWER SUPPLY DISCONNECTION DURING OPERATION.

In some applications, such as process controls, the main power supply protection system can, under certain conditions, disconnect the power supply during operation.
If the loads are motors or inductive loads, the collapsing magnetic field of the inductance can drive the output pin negative. The control circuit of the IC is isolated from the power MOSFET output section by an isolating junction which forms a well in the silicon surface; the control circuitry is constructed in this well. If the MOSFET cannot provide the current flow and the junction of the control circuit insulation is forward biased, this condition can prove critical due to the activation of parasitic components, and cause a current to flow though the control pins of the VIPower IC that can damage or disturb the micro-processor circuits.
The simple solution shown in figure 12, shows a clamping diode that enables the output power-MOSFET to conduct the energy stored in the inductance. Figure 13 shows the VIPower IC behaviour during a power supply disconnection; however the negative voltage spike on the diagnostic output can cause an incorrect feedback signal which can be avoided by using an R/C filter.

7.0 FUTURE DEVELOPMENT OF MOTOR DRIVE ICs.

The future trends of the VIPower technology, using a vertical current flow power MOSFET, are influenced by the needs in specific applications to drastically reduce the dimension of the high current motor control boards.
Surface mounting packages are being developed to satisfy this requirement. They will allow mounting in hybrid circuits without the need for sophisticated die attach technology.
These packages will have outlines that conform to those of existing packages, together with thermal resistance characteristics suitable for power devices.

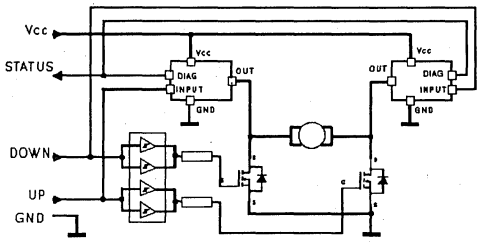

Figure 10 - Motor drive for a window lift with two VM201 intelligent switches

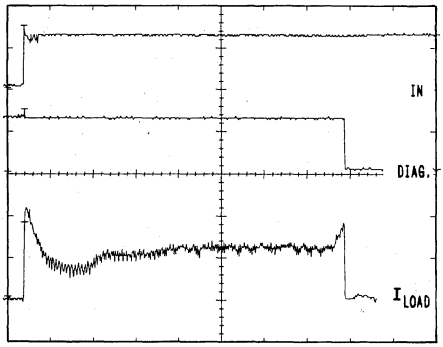

Figure 11 - The VM201 during the in rush current at turn-on of the left window and at turn-off due to a stalled condition. INPUT=5V/div, DIAG=5V/div, OUTPUT CURRENT=5A/div, t=100ms/div

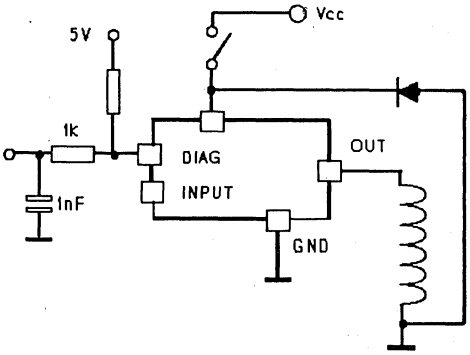

Figure 12 - Protection from accidental power supply disconnection

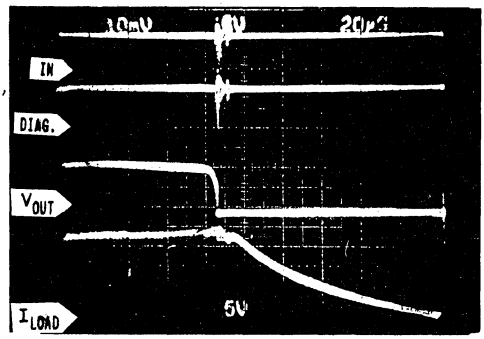

Figure 13 - Waveforms during power supply disconnection.
IN=5V/div, DIAG=5V/div, OUT=10V/div, Iout=2A/div

7.1 CONFIGURATIONS OF NEW LOW VOLTAGE MOTOR DRIVE ICs.

To give some concrete example of future ICs, typically power tool applications with a single switch are considered.
For full bridge applications, where bi-directional rotation is required, a double high side driver with two external low side discrete power MOSFETs can be employed, figure 14. A full bridge cannot be integrated in one chip using only VIPower technology because the substrate of the IC forms a common drain to all the integrated power MOSFETs.
However this can be resolved by using both

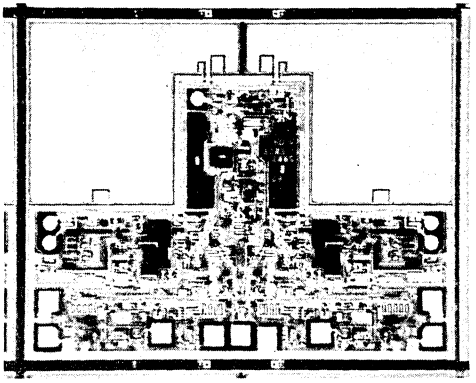

Figure 14 - Chip of a double side driver

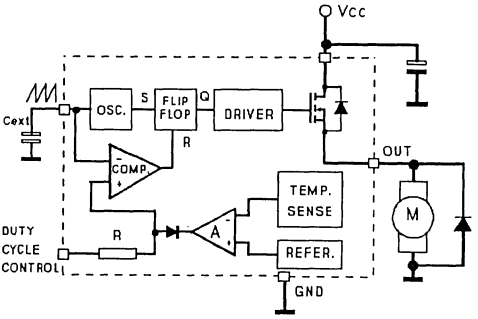

Figure 15 - Limitation of the maximum CHIP temperature using a temperature feedback.

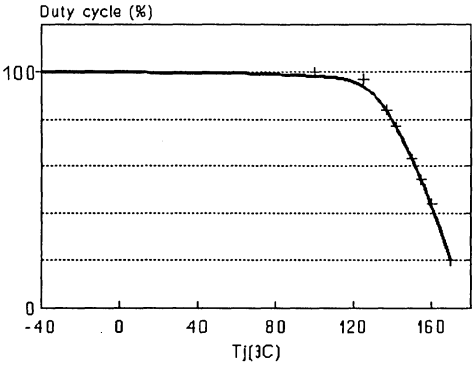

Figure 16 - Duty cycle reduction vs Tj in the circuit of Fig. 15.

the VIPower and the BCD (Bipolar CMOS DMOS) technologies. Figures 15 and 17 show examples of possible single switch mode motor control configurations integrated in VIPower technology:

Figure 15: The micro-processor sets the maximum duty cycle and the VIPower IC internally limits the operating junction temperature; when the temperature reaches the maximum value, the temperature sense circuit operates in a feed-back loop and reduces the duty cycle (figure 16) in order to maintain the junction temperature at a safe value; This feature allows the motor to work in overload conditions safeguarding the power ICs from the stress of over-temperature.

Figure 17: Speed and maximum torque control of the motor can be achieved using a feed-back control circuit for the current and the motor speed, the latter employing a frequency to voltage converter; this gives the possibility of precise control including motor acceleration control.

All these applications see the VIPower IC as a peripheral device of a micro-processor with the ability to make decisions; The VIPower IC, however, is self protected from over-current, over-temperature, etc, and is able to exercise rapid control over the process.

8.0 CONCLUSION.

Several problems are solved by the integration of a power MOSFET with appropriate control circuitry on one silicon chip. It achieves:

high current capability in a compact package

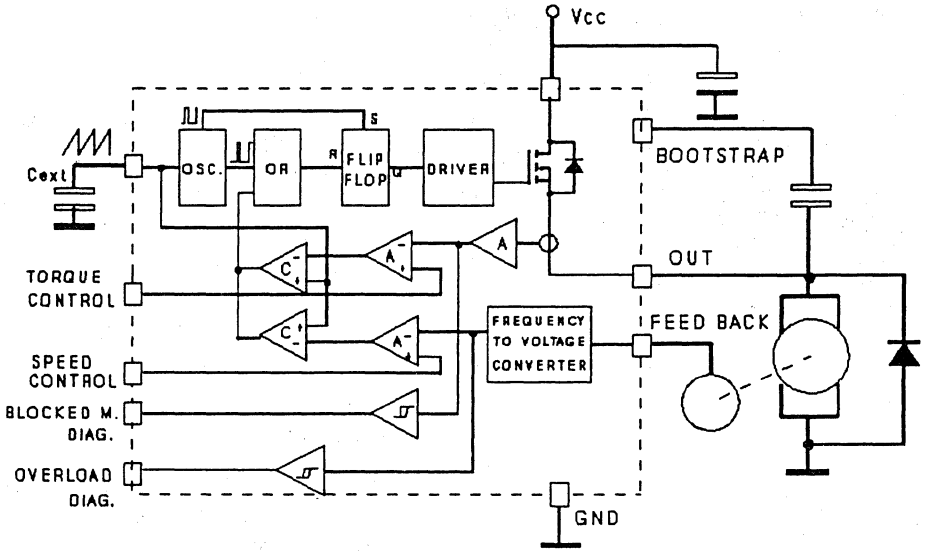

Figure 17 -Torque and/or speed motor control implementation

- no power dissipation in the sensing element using a sense-FET.
- no interference of the control circuit by stray induction in the external wiring.
- the ability to drive a power device from a logic circuit.
- diagnostic control and information.

The internal protection, the ruggedness and the wide range of working frequency make the VIPower IC able to drive motors and inductive loads under all working conditions without external protection.

The CMOS/TTL compatibility of the input and the output signals directly interface with a micro-processor and allow it to be used in many applications such as automotive actuators, process control, and robotics.

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DRIVERS AND IPS

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

HOW THE TDE1897/8 BEHAVE IN EXTREME OVERLOAD CONDITIONS

by U. Moriconi

The circuit designer may be interested and get some insight on how the TDE1897/8 behave, if extreme overload conditions are forced on to them. Although the conditions may range outside the limits of the datasheet guarantieed performances, erroneous connections during an installation phase may occur and momentarily create such conditions. The performed tests confirm the extreme ruggedness of these devices and their ability to survive the accidental overload.

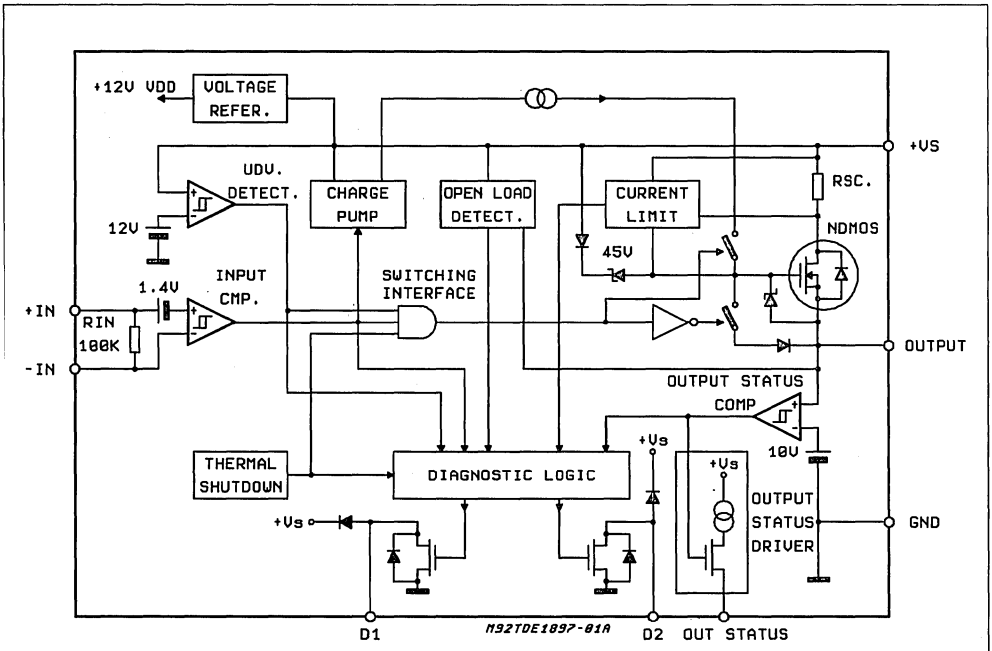
The TDE1897/8 is a monolithic Intelligent Power Switch (IPS) in High Side Configuration and BCD tecnology (see fig.1),dedicated to drive resistive and inductive load such as lamps, Relays, electro-valves, etc. An internal voltage clamping diode to +Vs creates, in inductive load, a fast demagnetization path without external components.

Suitable for industrial application, it operates in the 18 to 35V supply range delivering output current up to 500mA . In typical application it can drive up to 1 - 1.5H load coil (48 to 60Ω typical associated resistance).

OVERLOAD CONDITIONS

To investigate the behaviour of TDE1897/8 in extreme inductive overload conditions, that may occur when too big a load is connected to the device output, tests were performed, in bias conditions that lead the device to function out of the datasheet operatives and rated limits.

Figure 1: Block Diagram

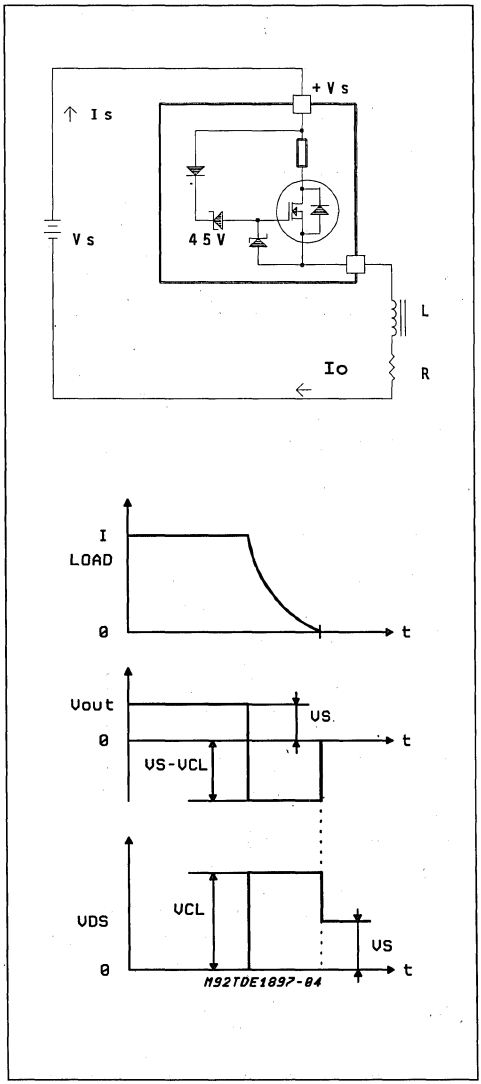


Test Conditions (referred to the circuit of fig. 2) Vs = +24V; Io = Internal Limited; T_{amb} = 25°C; L = 1.4H (non saturating); R_l = 12Ω; Vi = 2V (Vih)(#); T_j = from øLim-Hy to øLim and above (*)

(#) The input signal asks for a permanent "on" state.

(*) øLim & Hy = thresholds of intervention and histeresis of the internal thermal protection circuit.

Figure 2: Inductive Load Equivalent Circuit and Demagnetization Cycle Waveforms



OVERLOAD OPERATION

Due to the internal limitation (I_{SC}), the output current (I_O) is not limited by the load (V_S/R_l = 2A; I_{SC} ≤ 1.5A) but by the device itself. As soon as the current reaches I_{SC}, the I.P.S. goes out of the minimum resistance state and increases its voltage drop so that $I_O = I_{CS}$. The silicon temperature of the D.U.T. increases rapidly up to the thermal protection threshold value (øLim) and such protection tries to cut-off the output DMOS. The turn-off of the output forces the demagnetization cycle, that discharges the energy of the inductive load (to Vs) through the device.

The higher clamped current value (I_{SC}) will produce, during the demagnetization, more stress conditions because of both:

- The higher energy in the magnetic load
- The higher peak power (1)

During the "on" state the power (P_{don}) on the D.U.T (see the 225msec. interval in fig.3) is defined by the I_O (I_{SC}) and R_l values. The chip temperature rapidly increases and reaches the upper thermal protection threshold value (øLim); at that moment the protection is triggered on, inducing the attempt of switch-off, the associated demagnetization phase (some 50msec. after the 225msec. interval), and finally the switch-off.

The D.U.T. starts then to cool down staying in the off-state, until the chip temperature goes down to lower thermal threshold value (øLim-Hy). When lower limit (øLim-Hy) value is underpassed, the thermal protection circuit withdraws itself, the chip resumes its normal functions and restarts another cycle. In facts its input has been connected permanently to a voltage level of more than 2V, meaning a continuos request for conduction. A new overload cycle is so started, and a periodic repetition of:

- load charging
- current limitation
- overtemperature and demagnetization
- cooling down in the off state .

It can be noted that, for given thermal parameters (Z_{th}, Thermal protection levels and hysteresis), differences in P_{don} affect only the "T_{ON}" and "T_{OFF}" duration and ratio of such periodic repetition.

The Minidip device (TDE1897BDP) suffers heavier stress conditions than the SIP9 option (TDE1898ASP) because of the package differences (Minidip vs. SIP9 involves higher thermal gradients).

Note(1)
During the demagnetization phase , the power dissipated inside the I.P.S. Chip is: $I_O(t) * V_{CL}$
-$I_O(t)$ decays to zero from I_{SC}.
-V_{CL} is set by the I.P.S. itself to about 50V

SOME MEASUREMENTS AND CALCULATIONS

For a typical TDE1897BDP sample, thats is in Minidip package, (see Fig. 3) in "thermal" periodic repetition, the current (self-limited region) is limited to 1.1A and the voltage across the D.U.T. is = 10.8V for 225msec. "on" time. The energy dissipated on the D.U.T. in the demagnetization cycle is = 1.28 J (**) The repetition cycle rate is = 0.27Hz(t = 3.7sec.).

P_{don} (average) = 1.1A · 10.8V · 0.225sec/3.7s = 0.72W

$P_{dem.}$ (average) = 1.28J · 0.27cycles/s = 0.346W

Adding the small power dissipated for operating quiescent current and for $I_O(t)^2*R_{ON}$ in load-charging region, the total power $P_{(tot)}$= 1.1W is a realistic value.

Minidip (on the test-socket) $R_{thj\text{-}amb}$ is about 85 °C/W that leads the average temperature in the hot region of the chip) to 115-120°C (the chip isn't homogeneous in temperature. Higher temperatures are reached, during dissipation, in the area of the output DMOS).

Figure 3: TDE1897BDP Output Voltage (CH2) and Output Current (CH1) vs. Time in Thermal Periodic Repetition.

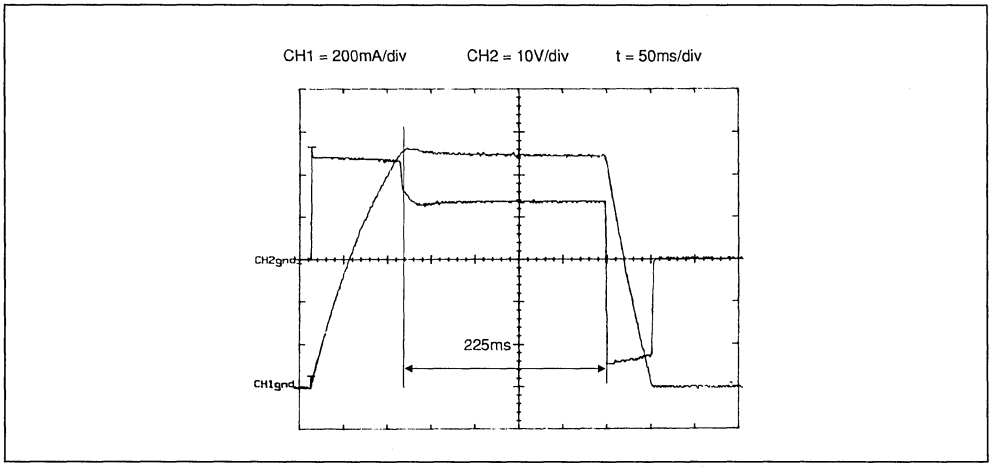
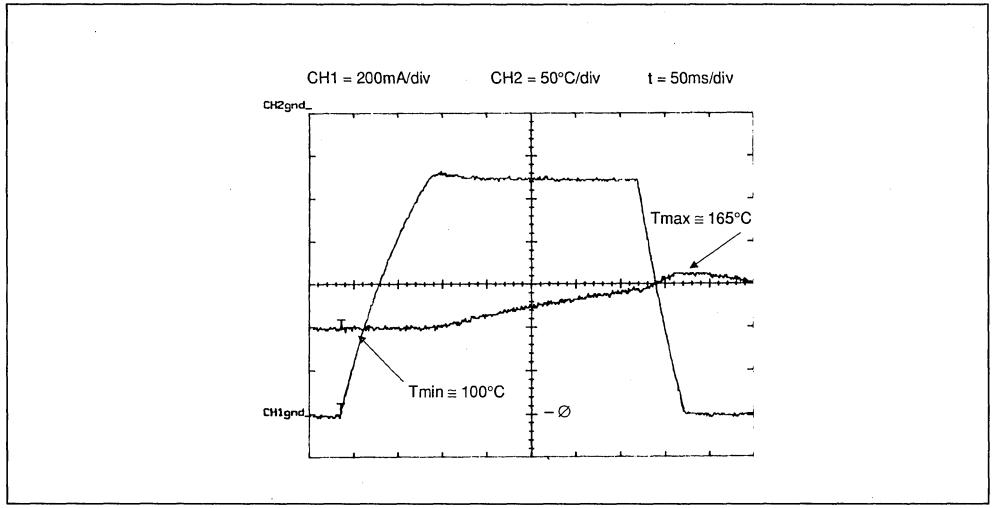


Figure 4: TDE1897BDP Output Current and Temperature in the Test Point, vs. Time.



For a typical TDE1898ASP sample, that is in SIP9 package, (see Fig. 5) in "thermal" periodic repetition, the current (self limited region) is limited to 1.15A and the voltage across the D.U.T. is = 10.2V for 300msec. "on" time. The energy dissipated on the D.U.T. in the demagnetization cycle is = 1.38J (**). The repetition cycle rate = 0.52Hz (t = 1.92sec.).

P_{don} (average) = 1.15A · 10.2V · 0.3s/1.92s = 1.83W

P_{dem} (average) = 1.38J · 0.522 cycles/s = 0.72W

The total power = 2.6W

The $R_{th\ j\text{-}amb}$ for SIP9 "on socket" is about 50 °C/W that leads the average temperature on the hot region of the chip to 150°C.

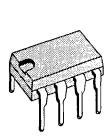
Note(**) The formula to use is :

$W = V_{CL} \cdot L/R_I * \{I_O - [(V_{CL} - V_S)/R_I] \cdot \log[1 + (I_O \cdot R_I)/(V_{CL} - V_S)]\}$

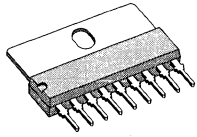
It is also interesting to see (Fig. 4 and 6) the temperature versus time (mesaured monitoring the forward voltage drop of an internal diode placed 1.5mm from the center of the power DMOS) in a region of the chip at lower average temperature.

On the "hot" region, the estimated temperature is quite higher (up to + 60°C. on the peak temperature, during the demagnetization phase)

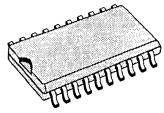
However no failure could be observed on the cheked devices also reducing the R_I value down to 8Ω, on some Minidip samples.



Minidip



SIP9



SO20

ORDERING NUMBERS:

TDE1898DP
TDE1897BDP

TDE1898ASP

TDE1898FP

Figure 5: TDE1898ASP Output Voltage (CH2) and Output Current (CH1) vs Time in Thermal Periodic Repetition

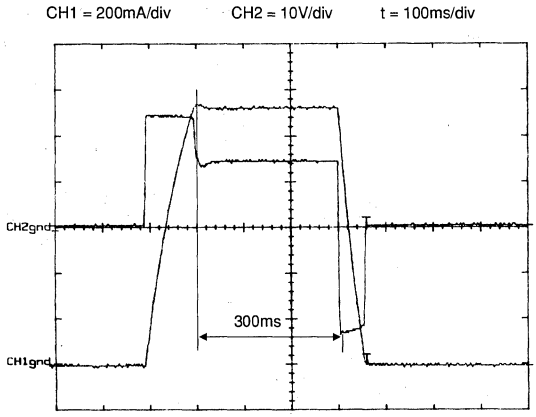
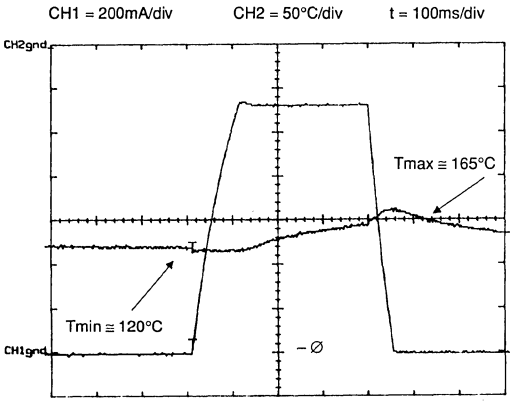


Figure 6: TDE1898ASP Output Current and Test Point Temperature vs. Time



CONCLUSION

The complex protection sistem of TDE1897/8 proves effective also in extreme overload conditions. Althougth the behaviour of such devices in those conditions cannot be guaranteed due to the high temperatures that accelerate the intrinsic ageing mechanism, the test performed show that there is a lot of margin beyond the guaranteed limits of the device datasheet. These test also show that it is very likely that such devices will survive to non permanent overloads like the ones possible in practice during the installation or modification of an industrial control system.

SWITCH–MODE DRIVERS FOR SOLENOID DRIVING

This design guide describes the operation and applications of the L294 and L295 switch-mode solenoid drivers. Integrating control circuitry and power stage on the same chip, these devices replace complex discrete circuits, bringing space and cost savings.

Many applications, particularly in computer peripherals, require a high power, fast solenoid driver circuit. In the past these circuits have been realised with discrete components because the high powers required precluded the use of monolithic technology.

SGS-THOMSON Microelectronics has overcome this problem with a new high power bipolar technology that uses an innovative implanted isolation technique. This technology is used to fabricate two switchmode solenoid driver chips, the L294 and L295, which both incorporate high power output stages and control circuitry. Both circuits are designed for efficient switmode operation and are mounted in Multiwatt ® plastic package.

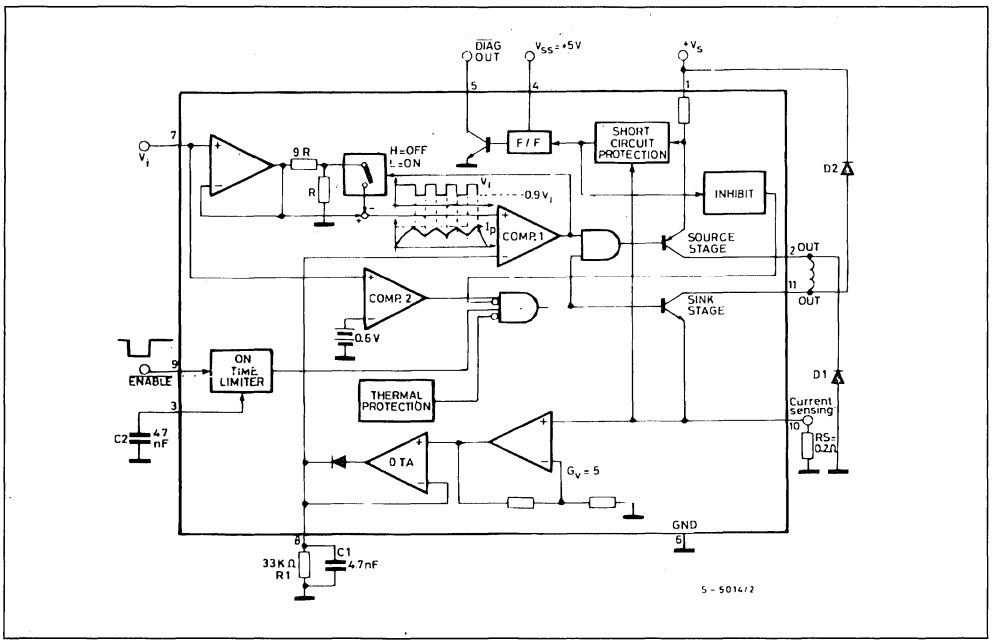
THE L294 SOLENOID DRIVER

The L294 is designed for solenoid driving applications where both very high speed and high current are essential ; needle and hammer driving in printer mechanisms, for example. It delivers 4 A with supply voltages up to 46 V, handling effective powers up to 180 W.

Shown in figure 1, the L294 is controlled by a TTL - level logic input and the peak load current is programmed by a reference voltage applied to the pin labelled V_i.

Internal switchmode control circuitry regulates the solenoid current by turning the output stage on and off repeatedly to keep the load current between the

Figure 1 : Internal Block Diagram of the L294 Switchmode Solenoid Driver.



programmed peak value, I_p, and a lower limit of 0.9 I_p.

Other features of the L294 include thermal shutdown, output short circuit protection, overdriving protection and a latched diagnostic output. This output indicates fault conditions such as a short circuit solenoid.

CIRCUIT OPERATION

In most applications the L294 is used with a fixed reference voltage (V_i) and the solenoid is controlled by negative-going pulses on the ENABLE input. When the ENABLE input is active (low level), the output stage is enabled and the load current rises as shown in figure 2.

The load current is sensed by an external resistor (R_S) in the emitter of the sink stage. Through the op amp and transconductance amplifier (OTA), the sensed voltage charges an external RC network (R1C1) which determines the switching characteristics of the device.

Figure 2 : Output Current Waveforms of the L294. The Output Current in regulated by Switching between a Peak Value, Ip, and a lower Limit of 0.9 Ip.

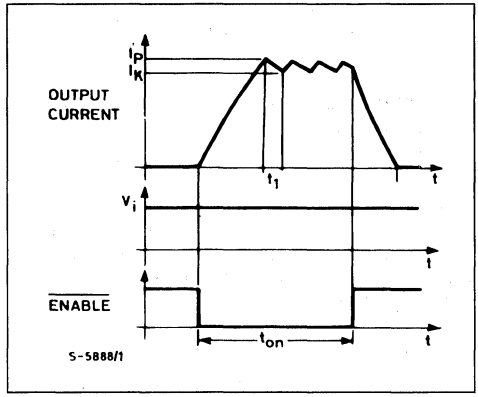
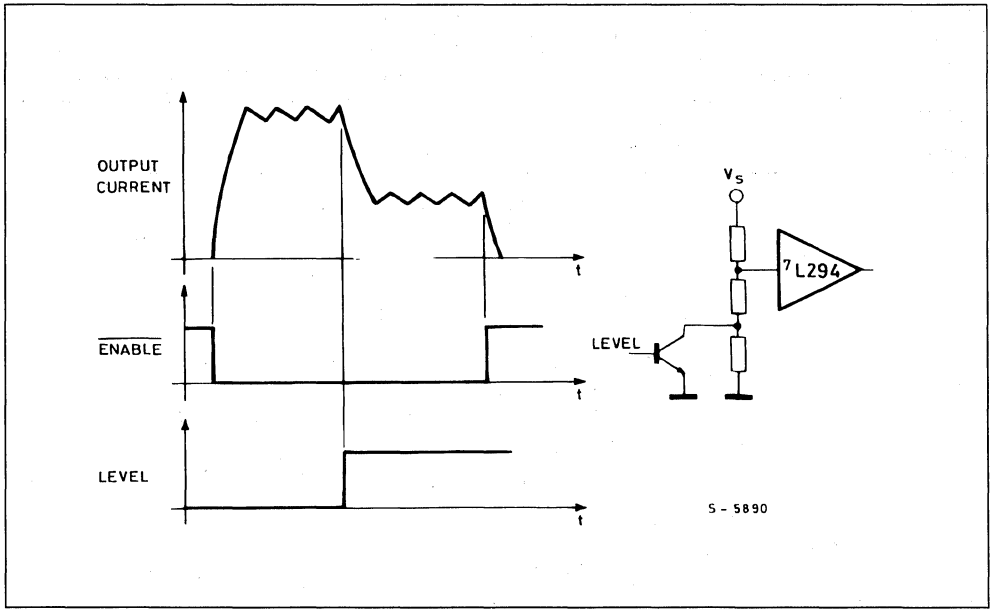


Figure 3 : Two Level Current Control can be implemented by switching Vi between two Values.



The voltage across this RC network is compared with the voltage V_i, which fixes the output peak current. When the current has reached the programmed peak value this comparator switches, turning off the output source stage and closing a switch which reduces the voltage on the non-inverting input to 0.9 V_i. The load current now recirculates in D1. The voltage on pin 8 falls with a time constant determined by R1C1 or the load characteristics, whichever is the longest. In other word. R1C1 sets the minimum recirculation time constant.

When the voltage across R1C1 has fallen to the 0.9 V_i threshold the comparator switches on, turning the output stage back on and restoring the V_i comparison threshold.

The output source stage is switched in this way, regulating the load current, until the ENABLE input goes high again. At this point the output stage is disabled - both source and sink - and the load current recirculates through D1 and D2 to ensure a fast decay. By varying the voltage V_i the peak load current can be programmed to any value in the range 0.6 A to 4 A. This feature can be exploited to implement two-level current control if the fixed reference is replaced by a switched reference as shown in figure 3.

PROTECTION

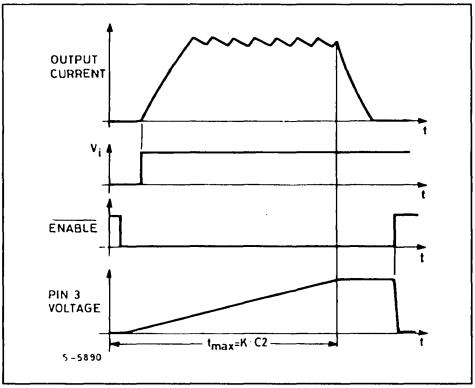
To protect the load and the L294 from overdriving an on-time limiter inhibits the output stage independently of the ENABLE input if the duration of the input pulse exceeds a period set by the external capacitor C2 (figure 4). This circuit is reset by taking the ENABLE input high. The on-time limiter can be disabled by grounding pin 3.

Protection against overheating is incorporated in the form of a thermal shutdown circuit which disables the output stage when the junction temperature exceeds 150°C. The circuit restarts when the temperature has fallen about 20°C.

The L294 is also protected against short circuits to ground, to supply and across the load. Triggered when the source stage current exceed 5 A or the sink stage current exceed 1 V/R_S, the short circuit protection block inhibits the output stage and sets a flip flop which is supplied by a separate supply voltage V_{SS}. This flip flop is connected to the diagnostic output and signals that all is not well - a shorted solenoid, for example. The diagnostic flip flop is reset by removing the supply V_S.

A LED can be connected to the diagnostic output as shown in figure 5. If the diagnostic function is not required the V_{SS} supply can be omitted. The short circuit protection, however, still functions, even without V_{SS}.

Figure 4 : On–time Limiter Waveforms. After a Period defined by C2 the Output is disabled regardless of the State of ENABLE, protecting against overdriving.



USING THE L294

The basic application circuit for the L294 is shown in figure 5 ; a suggested layout is given in figure 6. The circuit is complete except for the source of V_i. In most cases this will be provided by a simple resistive divider dimensioned to set the desired peak current. With a 0.2Ω sense resistor as shown, the L294 has a transconductance of 1A/V for V_i above 600 mV. The device will not work with V_i less than 450 mV and operation is not guaranteed for V_i between 450 mV and 600 mV.

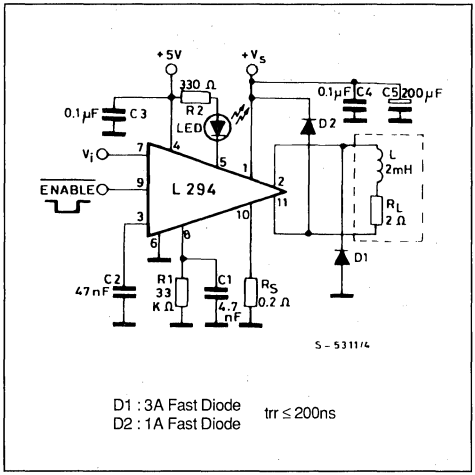
The on-time limiter delay - set by C2- is approximately 120 000 x C2. Pin 3 must be grounded if the on-time limiter isn't used.

Switching frequency depends partly on the timing network R1C1 and partly on the load characteristics.

R1C1 determines the minimum value of t_1 (see figure 2), which is given by $t1 \geq 0.1 \times R1C1$. C1 must be in the range 2.7 - 10 nF to ensure stability of the amplifier OTA. R1 must be at least 10 kΩ to give sufficient gain for OTA. The standard application circuit of figure 5 has a switching frequency of about 10 kHz.

The recirculation diodes should be fast types and rated at 3A (D1) and 1A (D2). If the full 4A capability of the L294 is not used these can be reduced.

Figure 5 : Standard Solenoid driving Application of the L294. Pin 7 must be connected to a Suitable Reference Voltage to set the Peak Current.



A high initial peak and low holding current can be obtained with the circuit shown in figure 7a. This example supplies a current peak for about 10 ms.

The peak current, I_{OEX}, (see figure 7a) is found from :

$$I_{OEX} = \frac{V_z}{5} \cdot \frac{R2}{R_S} \cdot \frac{1}{R1 + R2}$$

V_z is the zener voltage. The zener and R5 can be omitted if a regulated 5 V supply is available for point A.

The holding current, I_{hold}, is found from :

$$I_{hold} = \frac{V_z}{5} \cdot \frac{(R2 \,//\, R4)}{R_S} \cdot \frac{1}{R1 + (R2 \,//\, R4)}$$

The duration of the peak is determined by R3C1 and is increased by raising R3 or C1.

Typical component values are listed in the table below :

	I_{OEX} = 4 A I_{HOLD} = 1 A	I_{OEX} = 2.5 A I_{HOLD} = 0.5 A
R1	10 kΩ	10 kΩ
R2	47 kΩ	27 kΩ
R3	150 kΩ	150 kΩ
R4	2.7 kΩ	1.5 kΩ
R5	0.2 Ω (1 W)	0.27 Ω (0.5 W)
D1	3 A	1.5 A
D2	0.5 A	0.5 A
C1	0.2 µF	0.2 µF

Figure 6 : Suggested printed Circuit Board layout for the Application Circuit of figure 5.

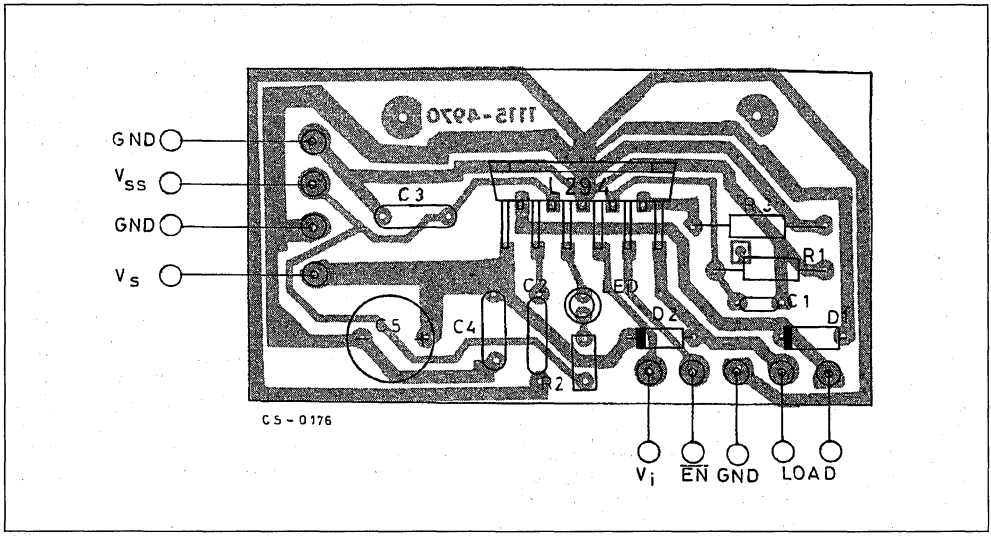


Figure 7a : Application Circuit for two Level Current Control. This Circuit generates a high Peak Current for a Period determined by R3C1 then a lower holding Current.

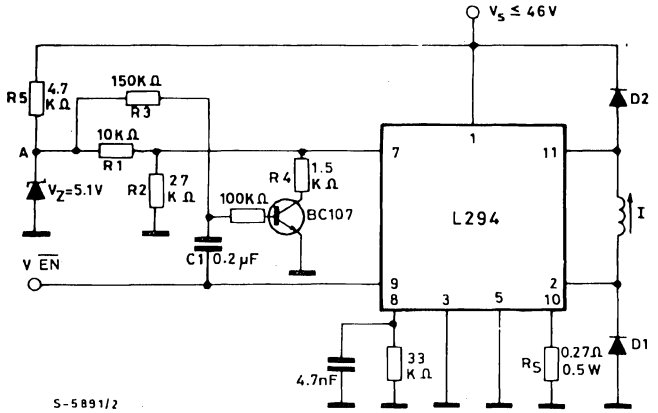


Figure 7b : Output Current Waveform obtained with the Circuit of fig. 7a.

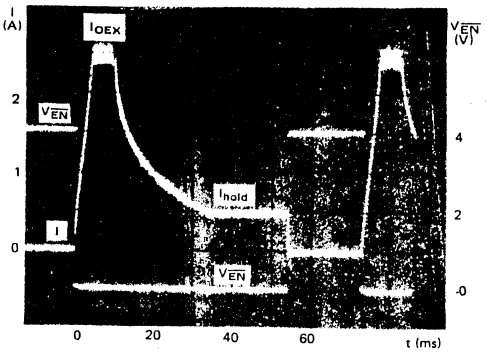


Figure 8 : Pin Functions of the L294.

N°	Function
1	Solenoid Supply Voltage V_S (12-46 V)
2	Output, Source Stage
3	On-time Limiter Time Constant. A capacitor to ground sets delay period (120 000 x C2 seconds). On-time limiter is disabled by grounding this pin.
4	Supply Input (5 V) for Diagnostic Flip Flop.
5	Diagnostic Output, Open Collector. Signals intervention of latched short circuit protection. Reset by removing pin 1 supply.
6	Ground.
7	V_i Reference Input. Peak output current is proportional to V_i. Transconductance is 1 A/V for R_S = 0.2 Ω and $V_i \geq 600$ mV.
8	Timing. A parallel RC network from this pin to ground sets the minimum recirculation time constant. The capacitor must be 2.7-10 nF to ensure stability. The resistor must be greater than 10 kΩ.
9	$\overline{\text{ENABLE}}$. TTL-compatible logic input that controls the solenoid current. The solenoid is driven when this input is at a low level. The on-time limiter overrides enable.
10	Connection for Load Current Sense Resistor.
11	Output, Sink Stage

THE L295 DUAL SWITCHMODE DRIVER

The L295 is a dual switchmode solenoid driver which handles up to 2.5 A per channel at voltages up to 46 V - a total effective power handling of 220 W. Compared to the L294 it offers a more economical solution when 2.5 A is sufficient because there are two drivers per chip. Like the L294 it features switchmode regulation of the output current and thermal shutdown. Additionally it has a separate logic supply input so that the logic can be run at a lower voltage, reducing dissipation.

Intended for inductive load driving, the L295 is particularly suitable for solenoids and stepper motors. One L295 drives two solenoids and two L295s can drive the four phases at a unipolar stepper motor or the two phases of a bipolar stepper motor in bridge configuration.

Each channel of the L295 is controlled by a TTL-level digital input and the peak load current is programmed, independently for each channel, by a voltage reference input. A chip enable input is also provided to disable both channels together.

INSIDE THE L295

Internally the L295 (figure 9) bears little resemblance to the L294. Looking at channel one, when the V_{IN1} input goes high the output transistors Q1 and Q2 are switched on (the enable input EN is assumed to be active, i.e. low). The current in the load then rises exponentially, as shown in figure 10, until the voltage across the external sense resistor R_{S1} reaches the current program reference voltage V_{ref1}.

The comparator COMP1 switches and sets the flip flop FF1 which turns off the source transistor Q1. The load current now recirculates through D2-Q2-R_{S1} and decays.

What happens next is determined by the oscillator components R and C on pin 9. If these components are present the flip flop is reset by the next clock pulse before the current decays very far. The output stage is therefore turned on again and the load current rises.

When it reaches the peak value COMP1 switches again, setting the flip flop and disabling the output stage. This process is repeated, regulating the load current until V_{in1} goes low. The output stage is then disabled and the current falls off rapidly, recirculating through D1 and D2 (figure 10).

If the oscillator components are omitted and pin 9 grounded the current simply decays slowly until V_{in1} goes low. The output stage is then disabled and the load current recirculates through D1 and D2. This case is illustrated by the waveforms of figure 11. Note that in this case the peak current level is controlled.

Unlike the L294, the switching frequency of the current regulation loop is determined by the oscillator components R and C (the L294 is also affected by the load). Typically, the switching frequency will be

10-30 kHz. Another difference between the two devices is that the L294 gives a constant ripple, the L295 does not.

TWO LEVEL CONTROL

Since the peak load current is programmed by the reference voltage (for each channel), two level current control can be obtained by switching between two reference voltages. A high V_{ref} is selected initially to give a high initial current peak. Then, after a suitable interval, V_{ref} is reduced to give the lower holding current (figure 12). Two level current control is very useful for solenoids which require a high initial current peak for fast actuation.

Figure 9 : Internal Block Diagram of the L295 Dual Switchmode Driver.

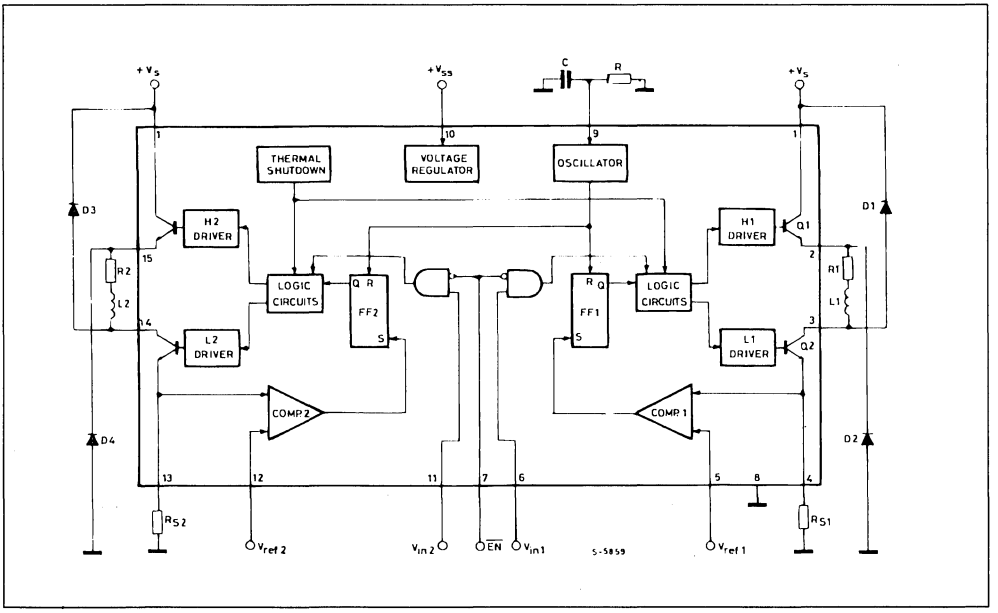


Figure 10 : Waveforms illustrating Normal Operation of the L295.

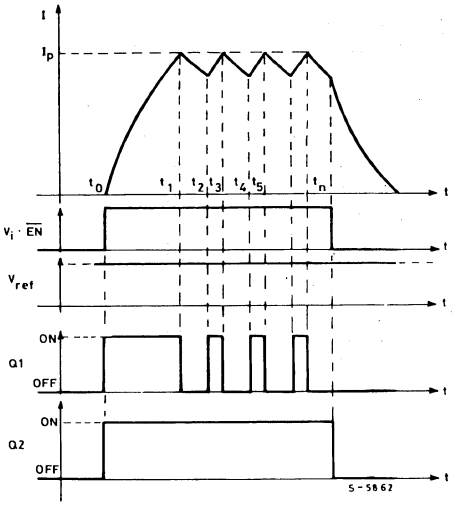


Figure 11 : When the Oscillator Components are omitted and Pin 9 grounded the L295 delivers a simple Current Peak to the Load.

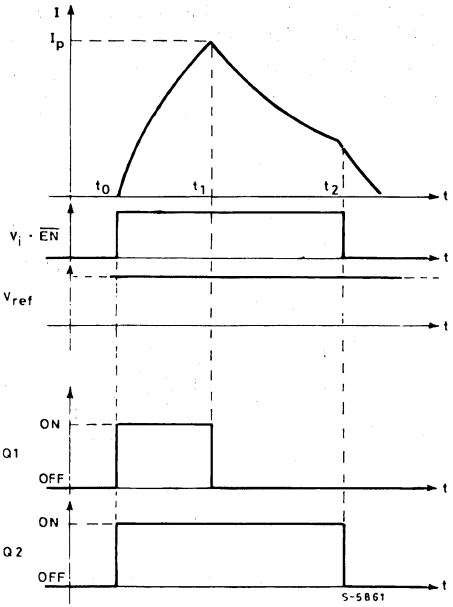
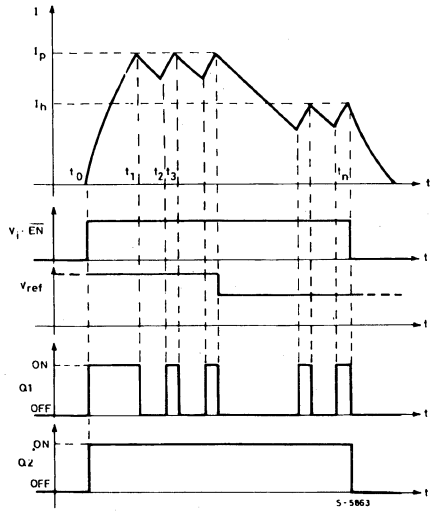


Figure 12 : Two Level Current Control is obtained by switching V_{ref} between two Values.



L295 APPLICATION HINTS

The basic application circuit of the L295 is shown in figure 14. A suitable layout is given in figure 15.

Suitable values for the oscillator components, R and C, can be found from the nomogram, figure 16. The value for the reference voltages depends on the desired peak current and is equal to I_pR_s ; it must be in the range 0.2 V to 2 V.

If the V_{ref} inputs are left open circuit the L295 assumes an internal default value of 2.5 V giving a peak current of 2.5/R_S amperes.

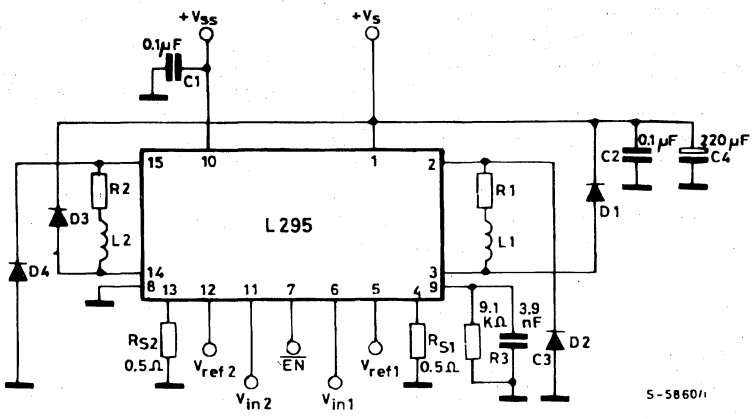
The L295 can also be used to drive unipolar stepper motors. For a four phase motor two devices are used, connected as shown in figure 17. This circuit provides switchmode regulation of the load current with a chopper rate of about 25 kHz. The enable inputs (EN, connected together) enable/disable the whole circuit and the channel inputs V_{in1} . . . V_{in4} are driven by a suitable translator circuit. Phases 1 and 2 must not be energised together because they share the same sense resistor. The same applies to channels 3 and 4. However, ' two phase on' drive is still possible for bifilar motors where phases one and two represent one winding and 3 & 4 the other, and also for variable reluctance motors with phase 1 adjacent to phase 3 etc.

Two L295s could also be used to drive a bipolar stepper motor in systems where a translator already exists.

Figure 13 : Pin Functions of the L295.

N°	Function
1	Solenoid Supply Voltage, V_s (12-46 V).
2	Channel one Output, Source Stage.
3	Channel one Output, Sink Stage.
4	R_{S1}. Sense Resistor Connection, Channel one.
5	V_{ref1}. A voltage on this pin sets peak current of channel one. If this pin is left open or connected to V_{ss} a default V_{ref} of 2.5 V is assumed. An externally applied V_{ref} must be in the range 0.2 to 2 V.
6	Vin1. Logic Input for Channel one. Driver is active when Vin1 is high and $\overline{EN}$ low.
7	$\overline{EN}$. Chip Enable (active low). When high both channels are disabled.
8	Ground.
9	Oscillator Timing Network. This pin is grounded to produce a single peak.
10	V_{ss}. Logic supply voltage, internally regulated. (4.75-10 V).
11	V_{in2}. Logic Input for Channel two. Driver is active when V_{in2} is high and EN low.
12	V_{ref2}. Voltage input, controls peak current of channel two. If left open or connected V_s an internal 2.5 V reference is assumed. An externally applied V_{ref} must be in the range 0.2 to 2 V.
13	R_{S2}. Sense Resistor Connection, Channel two.
14	Channel two Output, Sink Stage.
15	Channel two Output, Source Stage.

Figure 14 : Typical pplication Circuit of the L295. R1 L1 and R2 L2 are solenoids.



D1 : 3A Fast Diode
D2 : 1A Fast Diode trr ≤ 200ns

Figure 15 : Suggested printed Circuit Board layout for the Circuit of figure 14.

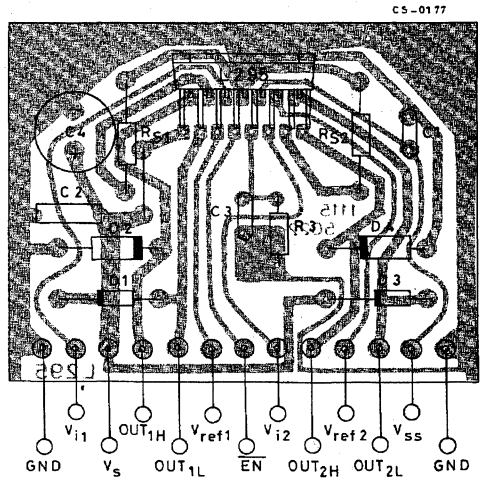


Figure 16 : Nomogram for the Selection of Values for the Oscillator components. RC.

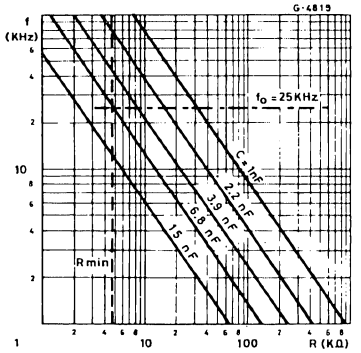
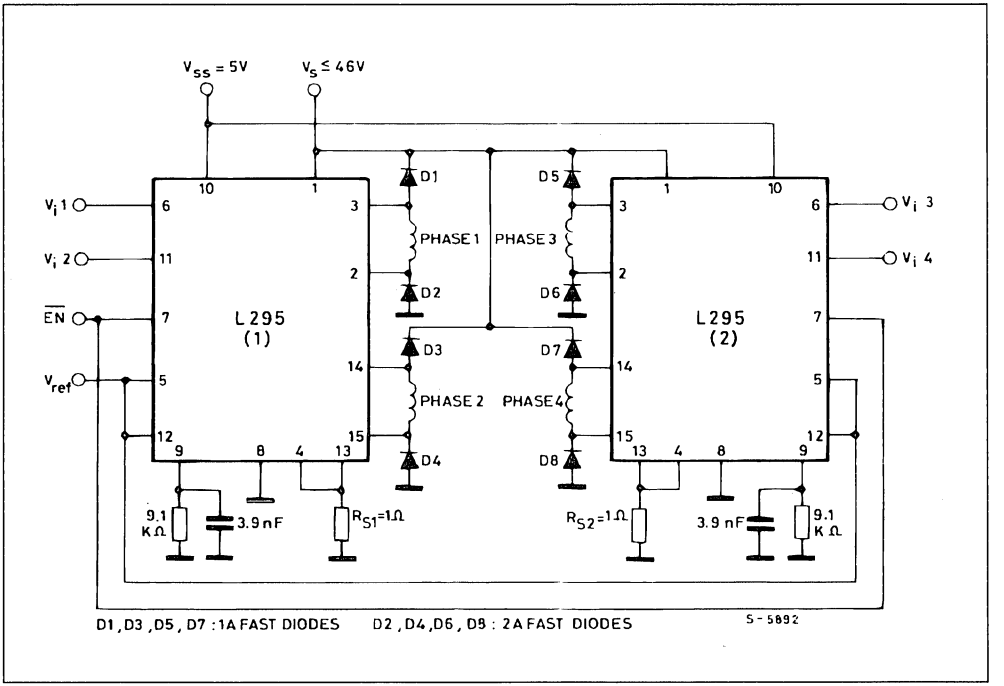


Figure 17 : Two L295s, connected as shown, can be used to drive a four Phase Unipolar Stepper Motor.



FULLY PROTECTED HIGH VOLTAGE INTERFACE FOR ELECTRONIC IGNITION

By S. PALARA ; M. PAPARO ; R. PELLICANO

INTRODUCTION

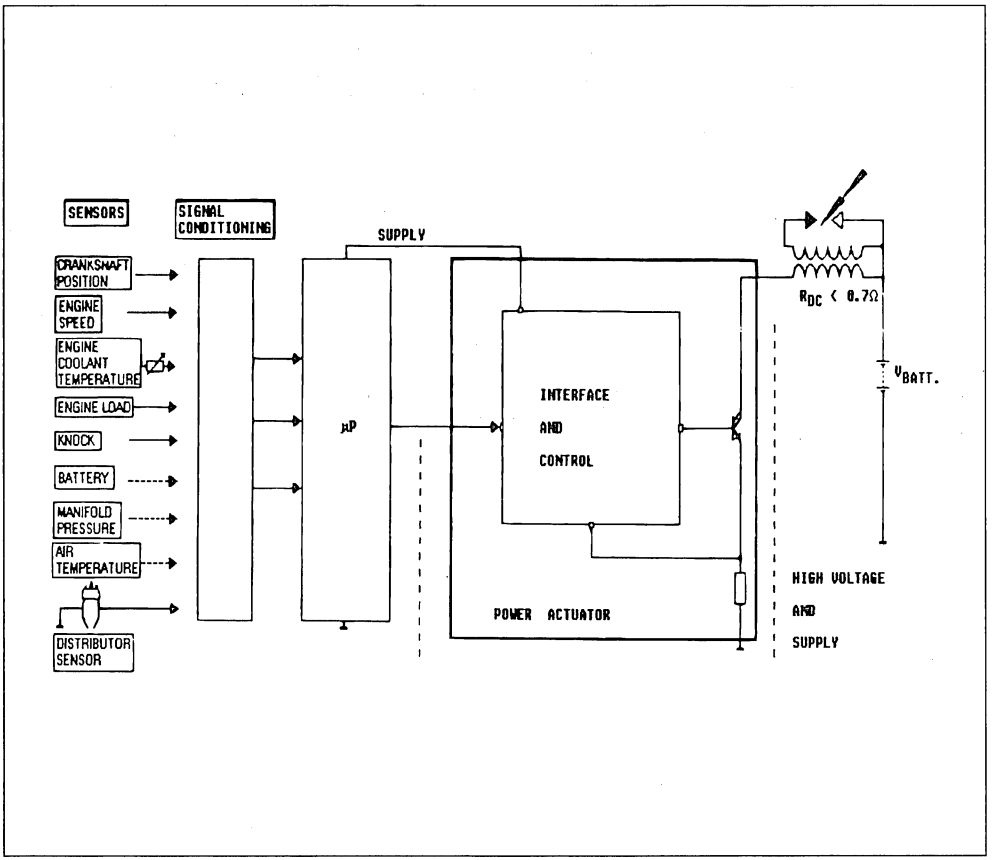
It is well known that an electronic car ignition system must be able to generate and supply the high energy discharge to the spark plugs, firing the petrol/air mixture at a precise point in each piston cycle.This job is performed by means of an high energy coil, its driver stage and the most suitable controller ; an example is shown in fig. 1.

In the most recent car ignition systems the coil current loading signal is controlled by a microprocessor that can also optimize the ignition timing. This ensures the correct spark at every speed for all environmental conditions.

The engine efficiency is so optimized ensuring the minimum toxic exhaust gas emission.

The high voltage necessary to generate the spark is obtained by charging the primary winding of the ignition coil with a controlled energy, i.e. a controlled current.

Figure 1 : Car Ignition System.



At the firing point this current is suddenly interrupted transferring the stored energy to the secondary winding and produces output voltage in excess of 20KV and therefore the spark.

The fig. 1 power actuator must also limit the current to a max of 10A and the voltage on the primary to a maximum of about 400V.

The voltage clamp avoids any damage to the power actuator : if the spark plug, for example, is disconnected, the energy stored in the coil is transferred back to the power actuator.

The device described in this paper realizes these power actuator functions with a very innovative integrated single chip solution.

THE VIPOWER M1 TECHNOLOGY

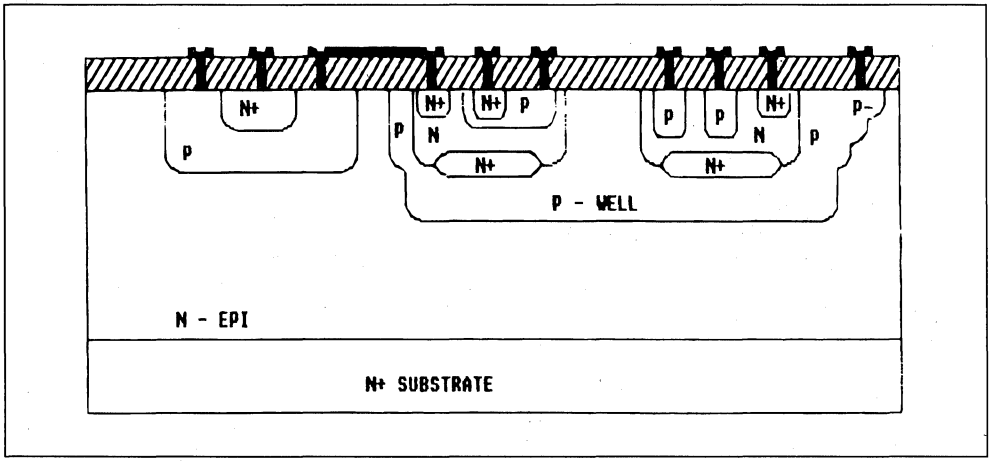
The VIPower M1 structure shown in fig. 2 combines a vertical current flow NPN power transistor and a low voltage junction isolated I.C. on the same silicon substrate.

This is realized inside a diffused p-type well that takes the place of a reverse-biased p-substrate of conventional ICs and must be connected to the most negative supply.

As in a standard discrete BJT, the first epitaxial layer thickness and resistivity set the Vceo and the ruggedness of the high voltage device, the second epi growth fixes the features of the low voltage components (up to 100V V_{CBO}).

The maximum voltage the power device can withstand is neverthless also dependent on the maximum field strentgh at the silicon surface and on the n^+/p–well parasitic diode breakdown voltage.

Figure 2 : VIPower Technology Vertical Structure.



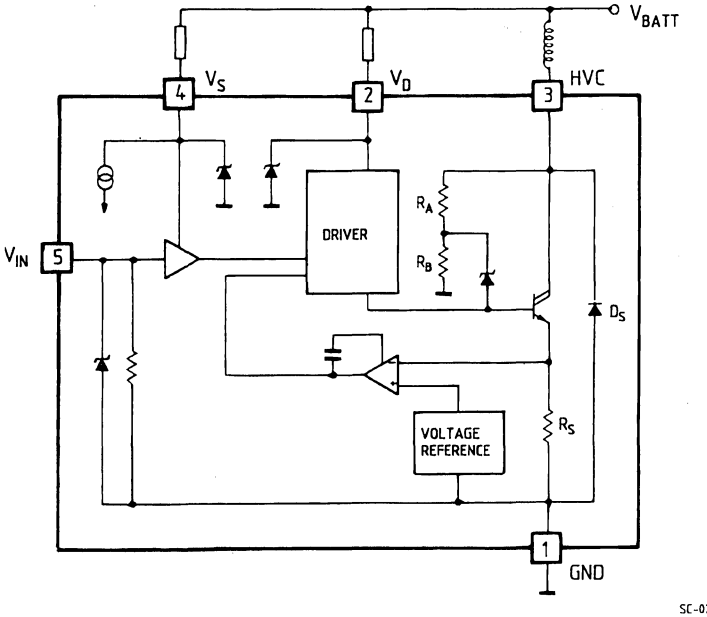
The high voltage termination of the integrated circuit is achieved by a p-diffused resistor in spiral from connected between the substrate (power darlington collector) and ground.

DEVICE CHARACTERISTICS

The device realizes the ignition, power actuator subsystem of fig. 1.

In the block diagram of fig. 3 the power Darlington with its driver and input stage, the current limit, voltage clamp circuitry and the overvoltage protection are shown.

Figure 3 : Device Block Diagram.



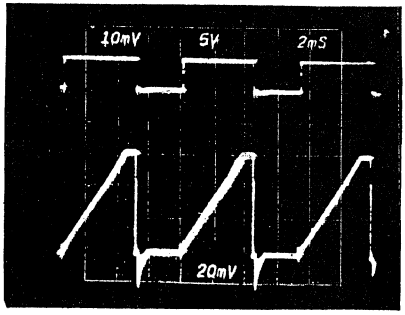
A TTL/CMOS compatible input signal coming from a logic interface, like a microprocessor, determines the turn on of the power darlington integrated in the chip.

The darlington collector current charges the coil linearly as long as a set level is reached, typically 6A ± 3%, sensed by an internal aluminium emitter resistance.

The voltage drop on this resistor is compared with an internally generated threshold (~ 200mV) and limits the current, thus controlling the Darlington base current until the input signal causes the output Darlington to switch off.

Photo 1 shows the coil current behaviour together with the corresponding input signal.

Photo 1 : Collector Current and Corresponding Input Signal.



Input signal (5V/div)

Coll. current (2A/div)

The current loop is made by compensated operational amplifier ensuring enough precision of the set value and hence of the stored energy without requiring external components.

The regulation stability is infact mandatory in the car ignition system to avoid spurious sparks on the secondary coil winding.

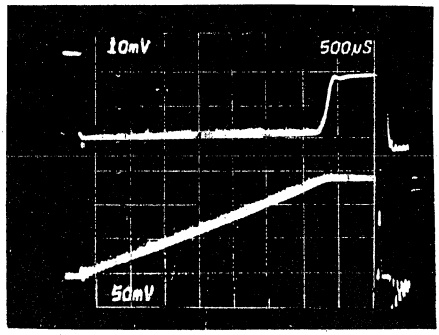
During the current limiting phase, the Darlington collector voltage reaches the battery voltage minus the voltage drop on the coil (due to the primary resistance). It causes high power dissipation in the power actuator which the microprocessor minimizes by delaying the output Darlington switch on.

The overvoltage on the power Darlington collector during the transition from the coil charging to the current limiting phase is low enough to avoid undesiderable sparks.

At the input signal switch-off the power Darlington is immediately turned off and the energy stored in the coil is transferred from the primary to the secondary winding causing the spark.

The collector voltage of the power Darlington then rises very rapidly and is detected by the spiral resistor used as the high voltage termination for the chip.

Photo 2 : Collector Voltage During Coil Charging.



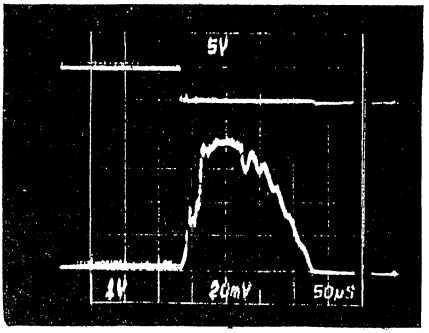
Coll. volt. (5V/div)

Coll. current (2A/div)

This resistor, used as a divider, is connected to a low voltage zener circuit that turns on the power Darlington, holding the collector voltage at a value determined in the chip (~ 400V ± 10%) which is less than the Darlington V_{CEO}.

Photo 3 shows the collector voltage during the clamp in absence of the spark plug i.e. the worst case for stress on the integrated circuit.

Photo 3 : Voltage Clamp.

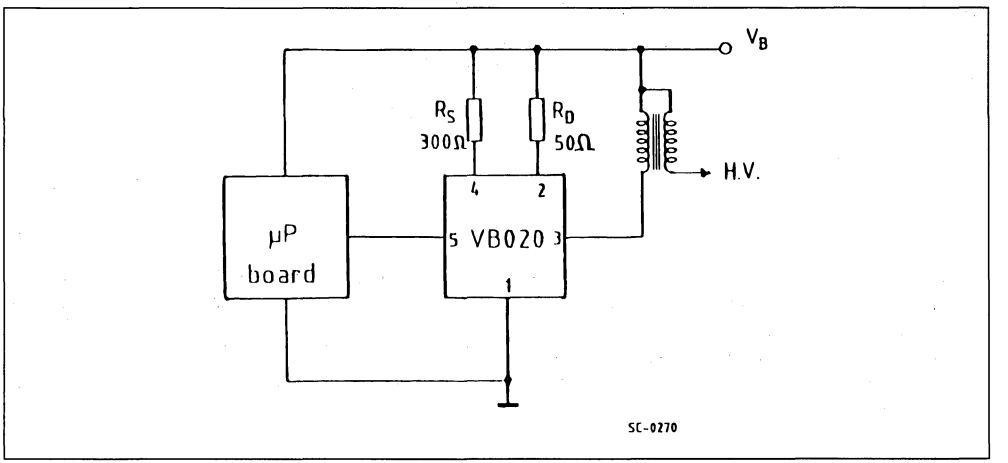


Input signal (5V/div)

Coll. volt. (100V/div)

Fig. 4 shows the application circuit for this device.

Figure 4 : Application Circuit .



Two separate pins for the supply : pin 4 and pin 2, are connected to the battery by means of two different resistors.

Pin 2 represents the supply of the driver with a current of up to 200mA.

Pin 4 is the supply for the rest of the circuit ($I_{4.1}$ ~ 3mA).

A picture of the die is shown in photograph 4.

The device is assembled in a new fully insulated five-lead plastic power package, ISOWATT 5 and shown in figure 5.

Photo 4 : The Die.

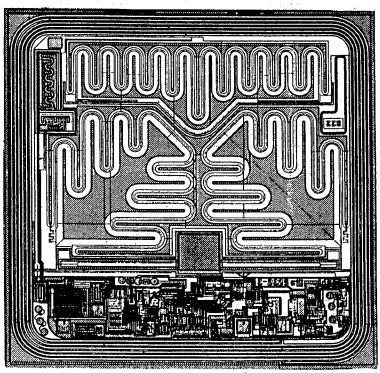
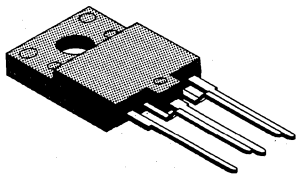


Figure 5.

ISOWATT 5



CONCLUSION

The ignition controller described in this paper completely substitutes the existing hybrid solution which requires additional components and manufacturing processes (i.e. insulating substrates, ink layers, active and special passive devices, laser trimming, encapsulation etc..). This single chip solution leads to an intrinsic increased compactness. The subsequent higher reliability is further enhanced by the known advantages of integration.

Additionally to that a cost reduction benefit through this approach is also achievable.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TRANSISTORIZED POWER SWITCHES WITH IMPROVED EFFICENCY

By M. Bildgen *, K. Rischmuller *

ABSTRACT.

An important objective for power electronic design is the reduction of power losses. This paper analyses the output characteristics of bipolar and MOS power stages and indicates limits for further on state loss reduction. A fast high voltage driver/switch combination with very low on state and switching losses is described. The switch is designed with cellular bipolar junction transistors driven by a smart power switch mode regulator. The driver handles duty cycles from 0...100 % and requires only one unregulated auxiliary supply. The static and dynamic behaviour of the switch and its new driver stage are shown and discussed. The switch exhibits low losses and is able to operate at inaudible switching frequencies on the rectified mains.

Keywords. Mains supplied operation, on state loss reduction, simplified base drive, smart power, high switching frequencies, Darlington, POWER MOSFET, cellular bipolar transistor.

INTRODUCTION

Loss reduction is a major objective in all power electronic equipment. The switching losses of all kinds of switching power semiconductors have been significantly reduced by means of structures with increased interdigitation, cellular structures and improved carrier lifetime control. Today performances are often close to those that physical laws allow. The switching losses have been reduced to such an extent, that lowering on state losses has become the key for further loss reduction. Further loss reduction can only be achieved through the reduction of on state losses which is the major topic discussed in this paper.

HOW TO REDUCE LOSSES?

Lowering on-state losses is of particular importance in inverter circuits operating with switching frequencies below 20kHz and in resonant converters where switching losses are already negligible.

For evaluation of on state losses, power semiconductor devices can be classified as:

a) devices with dominating resistive output behaviour

b) devices with dominating p-n junction behaviour of output characteristics (Fig.1).

The Power MOSFET (MOS), the Bipolar Modulated FET (BMFET)[5] and the Bipolar Junction Transistor (BJT) exhibit a resistive output behaviour (Fig.1a). Their on state voltage drop can be reduced through increasing die size, a question of technology and cost.

The Bipolar Darlington (DLT), the MOS Gated Bipolar Transistor (MOSBIP), the Insulated Gate Bipolar Transistor (IGBT) and Thyristors (GTO, FCTh...) exhibit a dominating p-n junction output behaviour (Fig 1b). The on state voltage drop of these devices is the sum of the threshold voltage of the p-n junction and the voltage drop across a resistance. The threshold voltage is determined by physical laws, only the resistive part of the on state voltage depends on the die size. The influence of die size on on-state losses is relatively limited and is not a feature that can be used to give significant loss reduction.

MOSFET AND BIPOLAR TRANSISTOR

The MOSFET, the BMFET and the BJT can have an on state voltage drop of less than 600mV and fast switching: A high power MOSFET e.g. a TSD4M450 ($R_{DS(on)}$ = 0.1Ω, V_{DS} =500V, I_D MAX = 45A) handles a current of 5 Amps with an on state voltage drop of only 500mV. The die area of such a device is about 170 mm^2. The MOSFET requires only short gate current pulses for its drive.

A very fast cellular BJT e. g. a BUF410 (450V/1000V, 15A) switches 5 Amps with about 500mV on state voltage drop. The die area of this device is about 36mm^2 and has therefore a very low silicon cost. The BJT requires base current:

— in excess of a fifth of the collector current

— and negative bias for fast turn off switching, immunity against reverse current and dv/dt.

Nevertheless, the power gain is very high, e.g. when switching 400V x 5A = 2kW, a drive power

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Fig.1: Symbols, equivalent circuits and output characteristics of power semiconductor devices; a) devices with resistive output behavi0ur; b) devices with p-n junction behaviour

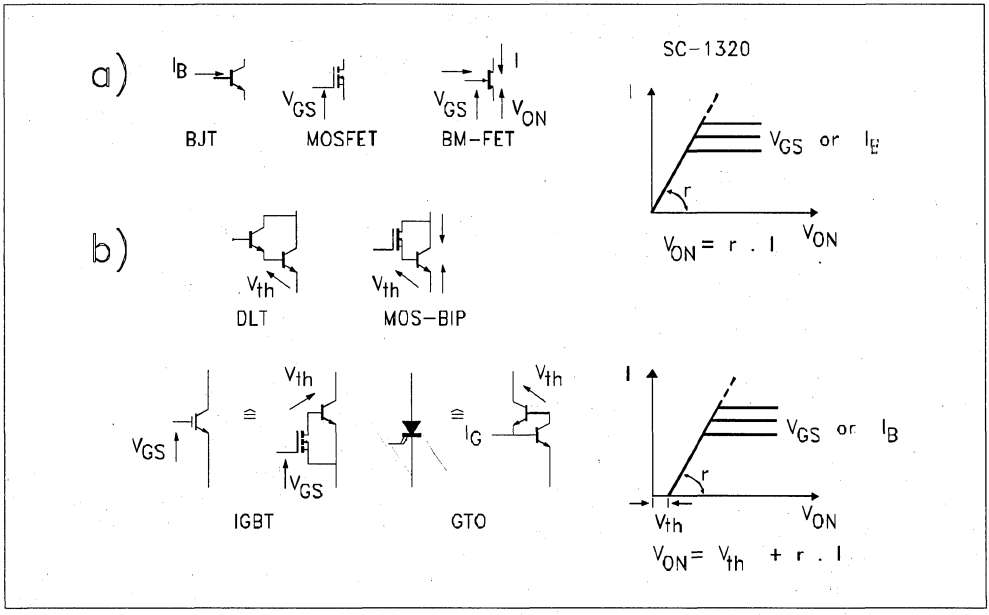


TABLE 1: On-state and driver losses of different device/driver configurations

Device + Driver	On-losses $V_{CE} + I_C$	Driver Consuptios $V_S + I_B$	Total Conductive Losses
BJT + (1)	0.5V x 20A = 10W	4A x 12V = 48W	58 W
DLT + (1)	1.5V x 20A = 30W	0.6A x 12V = 7W	37 W
BJT + (2)	0.5V x 20A = 10W	10W	20 W
DLT + (2)	1.4V x 20A = 28W	4W	32 W

of only 1A x 1V =1 W (base current multiplied by base emitter voltage) is needed.

The gap in die size between the POWER MOS-FET and the cellular BJT, increasing with voltage and current, is so important, that it is worth thinking about low loss base drive for bipolar transistors.[1, 2, 3]

TRANSISTORS AND DARLINGTONS

The Darlington is the most popular switch in mains supplied, medium power applications. The major reason for this choice is its moderate base current consumption.

A typical fast switching 20A,450V Darlington requires a 0.6A base current. With a conventional driver circuit operating from an 8V to 12V auxilary supply, the worst case driver consumption would be 12V x 0.6A = 7W (Table 1).

The collector-emitter on state losses of the Darlington can be typically calculated to be about 30W. The total conduction losses amount to about 37W.

The bipolar junction transistor exhibits collector emitter on state losses of only 10W but requires a positive base current of 4A.

The total driver loss in the transistors is 4A x 1V = 4W (base current multiplied by base emitter voltage). With a conventional driver circuit operating

Fig. 2: Example of a switch-mode driver circuit for fast switching applications

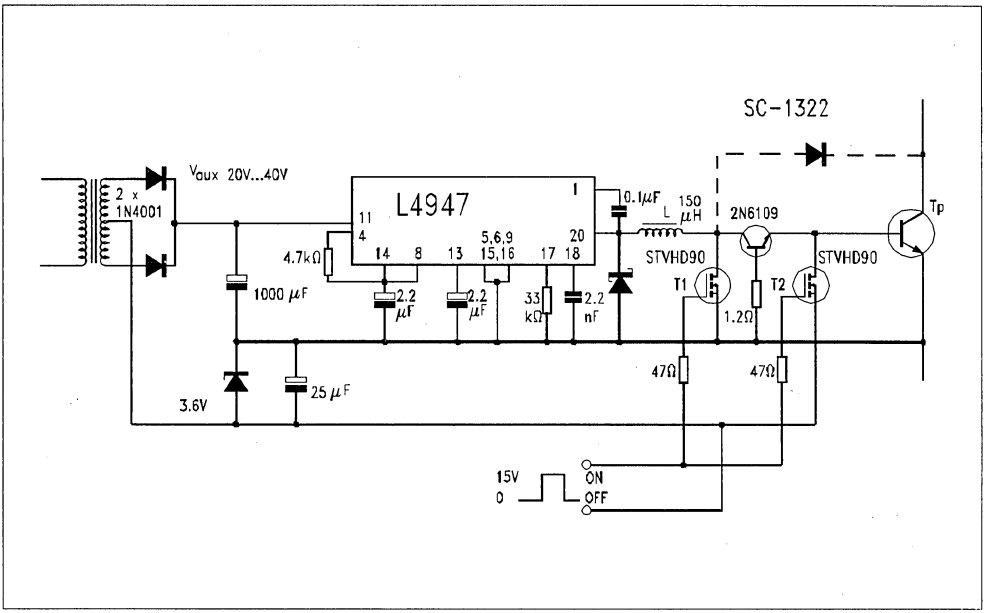
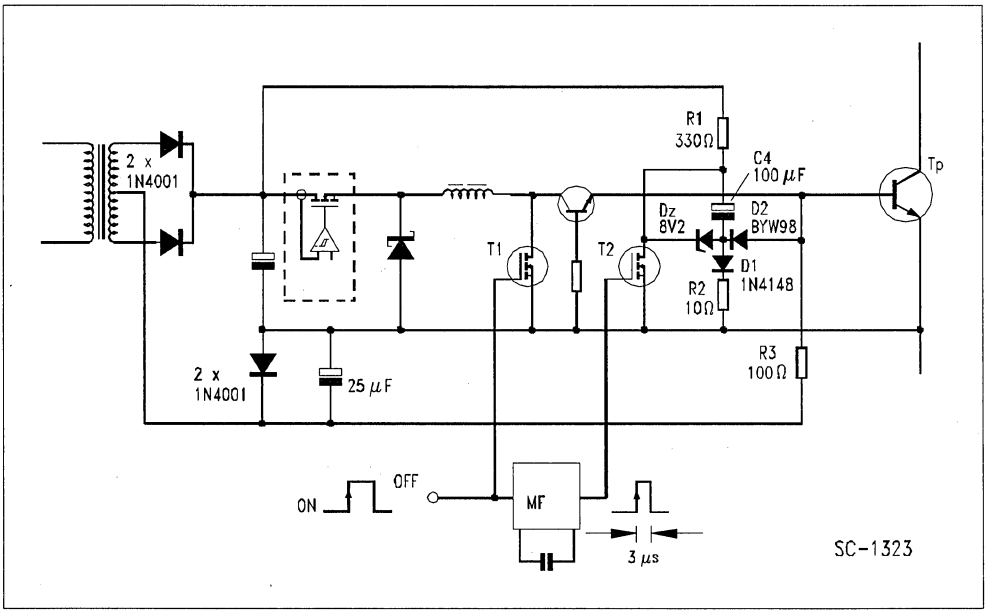


Fig.3: Self generation of negative bias from a positive supply voltage



from an 8V to 12V auxilary supply, the worst case driver consumption would be 48W - total conduction loss would be 58W. The poor efficiency of conventional driver stages is the reason that the transistor power switch exhibits higher conduction losses than the Darlington. Using driver stages with high efficiency allows BJT power stages to be used instead of Darlingtons which results in significant loss reduction.

DESCRIPTION OF THE SWITCH MODE BASE DRIVER

An L4974 smart power IC with a MOSFET output stage operates as a buck regulator in current mode. The IC is contained in a DIL package but is able to supply a 4 Amp base current. (Fig.2). The efficiency is so high that thermal conduction to the PCB provides sufficient cooling. During the off state of the power transistor, TP, a MOSFET T1 applies a short circuit to the output of the buck regulator. The IC operates with low duty cycle and maintains constant current in the choke L. For turn on of the power transistor TP, the MOSFET, T1, is turned off and the constant choke current flows into the power transistor's base. The rate of rise of base current is limited only by the MOSFET turn off speed. In order to obtain very fast switching, a high density MOSFET (STVHD90) which has a very reduced input and output capacitance, has been used.

If the power transistor base current is 4 Amps and the auxilary supply voltage 20V, the driver input current will be about 0.47 Amps. Increasing the auxilary supply voltage further reduces the input current.

NEGATIVE BIAS FOR FAST TURN OFF SWITCHING

The first version of the circuit generates negative bias with a Zener diode between auxilary supply and driver stage (Fig.2). The current return path to the auxiliary supply is through this diode. Losses in the Zener diode are small, due to the fact that input current of the driver circuit is small. For turn off, T1 and T2 are turned on, T2 applies the negative bias to the power transistor base, thus obtaining fast switching and immunity against reverse current and dv/dt.[4]

The second version of the circuit generates its negative bias directly from a positive auxilary supply:

a capacitor C1 (Fig.3) is permanently charged via a resistor R1 and a diode D1. At turn off switching, T2 is turned on for a time t1, slightly longer than the power transistor's storage

Fig. 4: Test circuits for switching losses

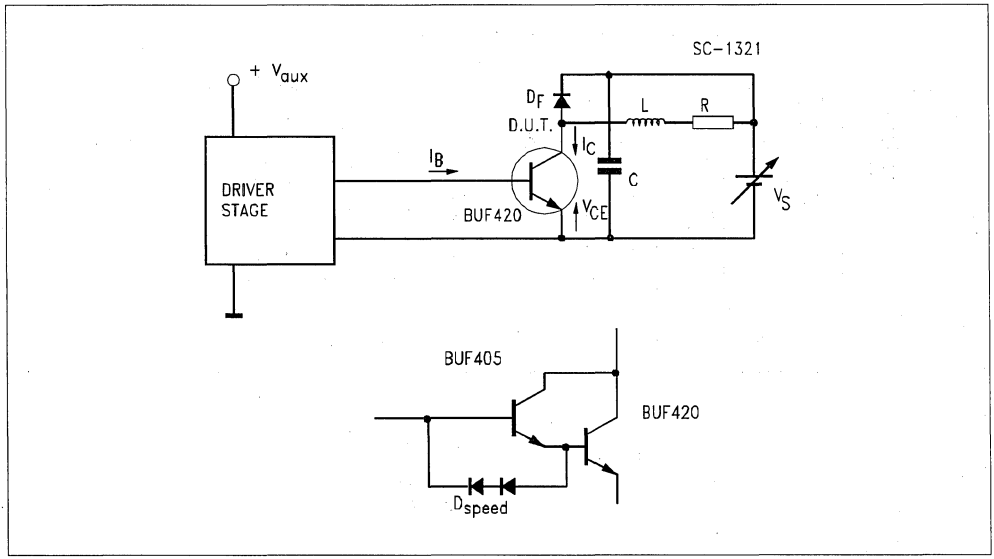


Fig. 5: Turn-on and off switching waveforms with transistors and Darlingtons

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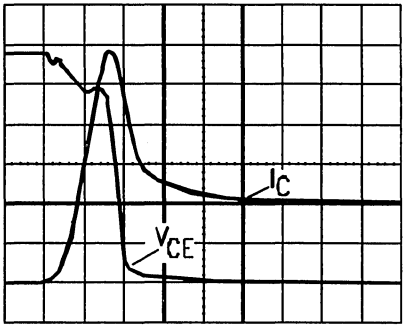
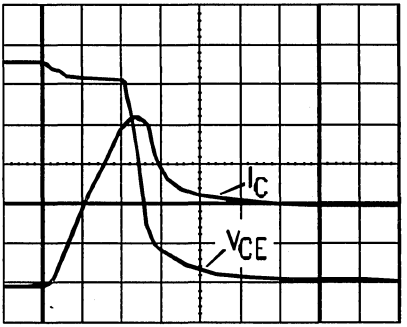


Darlington:
BUF405 + BUF420/BYT30-600
Turn-on: V_{CE} = 50V/div
I_C = 10A/div
t = 100ns/div
di_c/dt = 450A/μs

SC-1326



Bipolar Junction Transistor:
BUF420/BYT30-600
Turn-on: V_{CE} = 50V/div
I_C = 10A/div
t = 100ns/div
di_c/dt = 450A/μs

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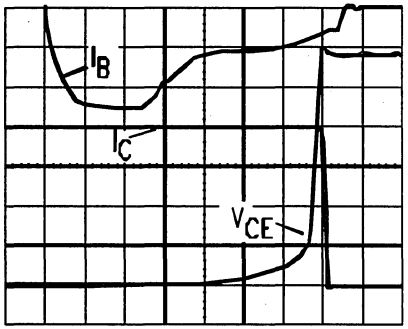
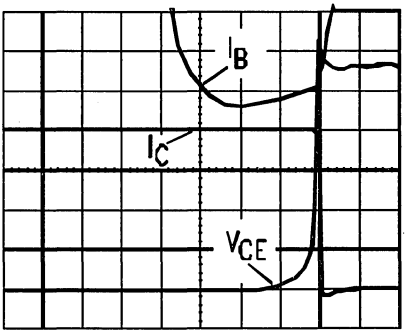


Darlington:
BUF405 + BUF420/BYT30-600
Turn-off: V_{CE} = 50V/div
I_C = 5A/div I_B = 2A/div
t = 500ns/div

SC-1327



Bipolar Junction Transistor:
BUF420/BYT30-600
Turn-off: V_{CE} = 50V/div
I_C = 5A/div I_B = 2A/div
t = 500ns/div

TABLE2: Switching energy losses of transistor and Darlington with BUF420 and BYT30-600

DEVICE UNDER TEST (DUT)	TURN-ON ENERGY	TURN-OFF ENERGY	TOTAL SWITCHING ENERGY
CELL. - BJT	1 mJ	0.5 mJ	1.5 mJ
CELL. - DLT	0.9 mJ	0.8 mJ	1.7 mJ

time, ts. T2 connects the positive electrode of C1 to ground, thus a negative voltage appears at the base of TP. T2 turns off after the turn off switching of TP and C1 continues charging. The state of charge of C1 is independant of duty cycle - sufficient negative bias is available with any duty cycle.

TEST RESULTS

Fast transistors and Darlingtons made using cellular technology (e.g.BUF420) have been tested in a buck converter with 280V supply voltage and 20A output current (Fig.4) Both types of switches have been driven from the same switch mode driver circuit. The turn on and turn off waveforms are shown in Fig. 5a and 5b. The devices were operated at Tj =85°C.

As expected, the turn on speed di_C/dt of the Darlington is twice as fast as that of the transistor switch. The reverse recovery current of the free wheel diode increases with di/dt. This makes the difference in turn-on loss between the fast switching transistor stage and the faster switching Darlington stage insignificant (Table 2). The storage time of a transistor stage is less than that of a Darlington stage. The test results confirm this well known fact.

With a given driver stage, the negative base current of a Darlington is reduced, due to the voltage drop of the speed up diodes. (Fig. 4) This explains the observed increased turn off losses with the Darlington.

CONDUCTION LOSSES

The conduction losses, including driver losses have been calculated and confirmed by measurement. With a duty cycle of 100% the total conduction losses of a 20A Darlington with conventional driver are O.6A x 12V + 1.5V x 20A = 37W. The same Darlington driven from the switch mode driver exhibits conduction losses of 32W. The conduction losses of the transistor with switch mode driver are 0.5A x 20V + 0,5V x 20A =20W.

This is about 60% of the switch mode driven Darlington.

CONCLUSION

Low loss driver circuits suffered from duty cycle limitations, or from excessive circuit complexity. New smart power devices reduce this complexity to an acceptable level, allowing the introduction of switch mode driver techniques in to transistorized power electronic equipment. The new configuration can be used to simplify and improve existing converter/inverter circuits (fewer auxiliary supplies, smaller heatsinks, higher efficiency).

The use of switch mode driver stages is not limited to BJTs, but offers improved efficiency in circuits with Darlingtons, BMFETs and GTOs.

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APPLICATION NOTE

ELECTRONIC IGNITION WITH VB020 AND L497

by M. Melito

INTRODUCTION

The VB020 is a monolithic high voltage integrated circuit which combines a vertical power darlington with built-in protection circuits for coil current limiting and collector voltage clamping. The device interfaces directly with a microprocessor which controls the dwell angle.

This application note shows how it is possible to use the VB020 in an electronic ignition system not employing a microprocessor.

The IC used, the L497, is a more conventional electronic ignition controller for breakerless ignition systems using a Hall effect sensor.

OPERATING PRINCIPLE

The schematic of fig.1 shows how the two ICs are connected to control both the coil current, providing the required stored energy and the dwell angle, for low power dissipation.

The L497 was designed to drive an external Darlington and in a standard application circuit the current control is performed monitoring the coil current through a sensing resistor on the emitter of the Darlington. When the voltage drop across the sensing resistor reaches the internal comparator threshold value the dwell angle control circuit is enabled. Meanwhile the coil current is kept constant forcing the

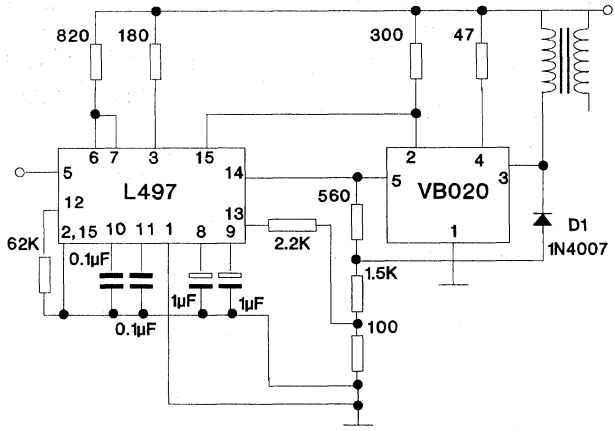


Fig. 1 - Schematic of electronic ignition with VB020 and L497.

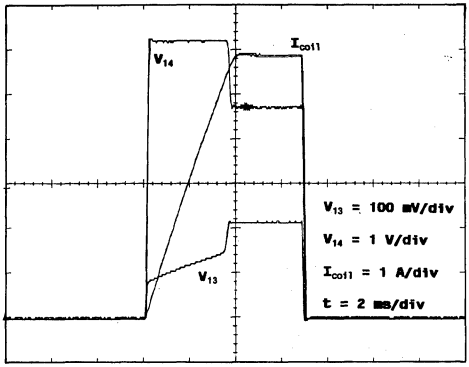


Fig. 2 - V_{13}, V_{14} and I_{coil} waveforms.

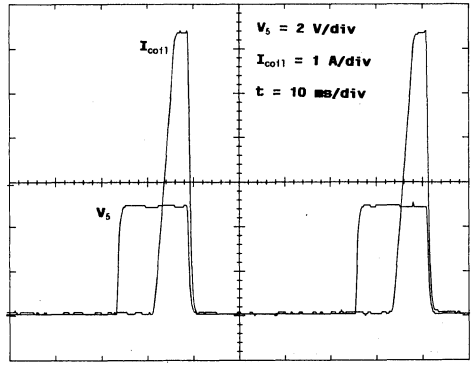


Fig. 3 - Duty-cycle = 30%; frequency = 20 Hz.

Darlington into the active region until the high-low transition of the input signal causes the spark to occur. The collector voltage is clamped to a value that is externally fixed by a resistive network. The internal dwell angle control circuit calculates the conduction time for the output Darlington in relation to the speed of rotation, to the supply voltage and to the characteristics of the coil, thus avoiding excessive power dissipation in the Darlington itself.

By linking together the L497 and the VB020 it is possible to avoid both the coil current sensing and the collector voltage clamping networks because the VB020 has internal built-in protection circuits which perform these functions. The dwell angle control is performed by supplying the L497 with the feedback signal shown in fig.2. The diode, D1, keeps the voltage at pin 13 of the L497 under the internal comparator threshold voltage until the VB020 begins to regulate the coil current. At this point

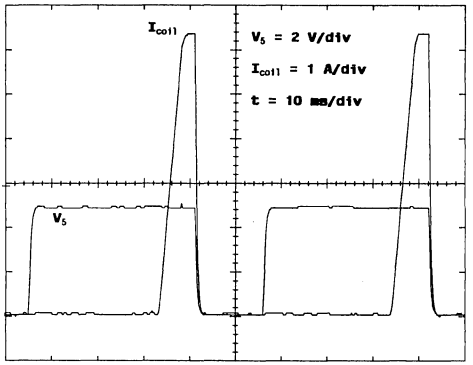


Fig. 4 - Duty-cycle = 70%; frequency = 20 Hz.

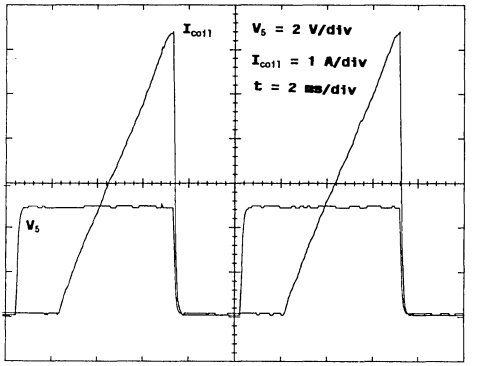


Fig. 5 - Duty-cycle = 70%; frequency = 100 Hz.

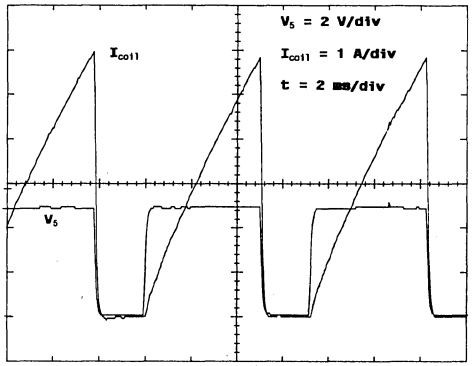


Fig. 6 - Duty-cycle = 70%; frequency = 140 Hz.

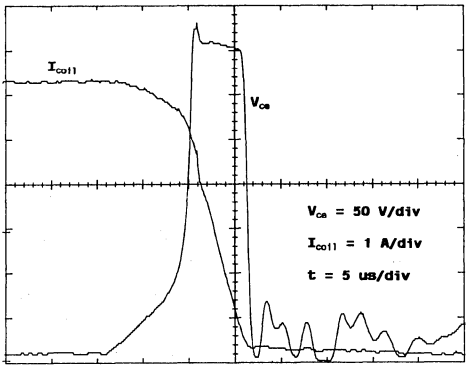


Fig. 7 - Turn-off in normal operating mode.

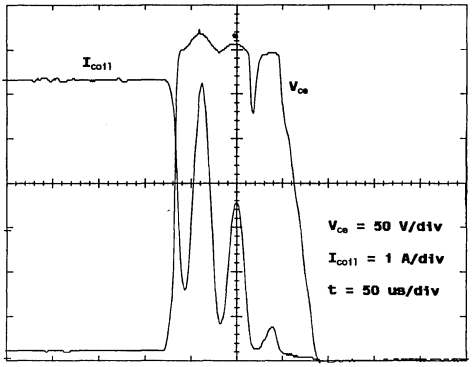


Fig. 8 - Turn-off with open gap.

D1 is turned-off and the voltage on pin 13 can reach the threshold voltage of the internal comparator enabling the dwell control circuit. Figures 3 to 8 show the system performance (V_{in}, I_{coil}) under various conditions and fig. 9 shows the conduction angle versus r.p.m. for a four cylinder engine.

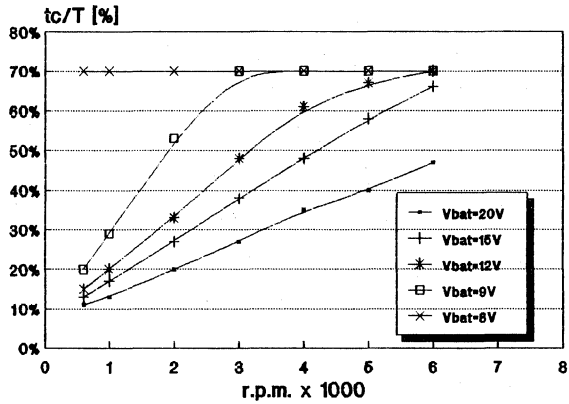


Fig. 9 - Conduction angle versus r.p.m.

CONCLUSION

The VB020 can be used in electronic ignition systems without using a microprocessor.
The overall cost of the system can be competitive with the solution using a Darlington because the current limiting and voltage clamping function performed by the VB020 are trimmed on silicon avoiding the need for additional adjustment.

REFERENCES

[1] F. Pellegrini, "L482 Development Report", SGS-THOMSON internal report, August 1982.

[2] M. Paparo, "L497 Development Report", SGS-THOMSON internal report, July 1985.

[3] "Automotive Products" Data-book, SGS-THOMSON microelectronics

INTELLIGENT AUTOPROTECTED DRIVERS

by I.M.PETER and I.RATES

INTRODUCTION

In industrial applications, where digital control signals are provided by automation equipment, suitable **Drivers** are required to control various loads such as Relays, Lamps, Electrovalves, etc.

What are the essential main characteristics of these Drivers ?

- Primarily, they must be autoprotected, that is, they must be self-resistant to industry-originated disturbances, short-circuits, over-currents, accidental load and ground disconnection, and so on.
- Then, in case of fault occurrence, they must be capable of providing interactive dialogue with the central processor unit.
- And finally, they must meet the requirements of the standards currently in force and those of the forthcoming projects, imposing that one terminal of the load should be directly connected to ground (see figure 1).

The objective of this note is to discuss and illustrate how a family of autoprotected control has been developed from basic concepts and also to outline the likely future trends.

FUNDAMENTALS

The control signal is applied to a comparator, the output of which drives a current source. This current source in turn drives the power transistor T1. A transistor T2 driven by the voltage drop across shunt R_{SC} is configured to provide feed-back to power transistor T1. As soon as the voltage drop across this shunt exceeds 0.7V, T1 T2 configuration will act as a current limiting-unit so that $I_{limit} = 0.8/R_{SC}$. This is how the device is protected against short-circuits.

Another internal unit monitors the junction temperature which varies as a function of dissipated power (i.e. $V_{CC} \times I_{CC}$) and cooling conditions. As soon as this temperature exceeds + 175°C (upper threshold), the protection until is activated and will sink the generator current I_B thereby turning the device off. In the off condition, the device will cool down, and when the junction temperature falls below + 140°C (lower threshold), the thermal protection unit is deactivated and the device is restored to its normal operating mode. However, if the overload conditions persist, the system will operate in low frequency relaxation mode with a frequency ranging from 1Hz to a few Hz according to the nature of the overload. Whatever the operating conditions :

- The current is limited at a programmable level.
- The junction temperature limit is never exceeded.

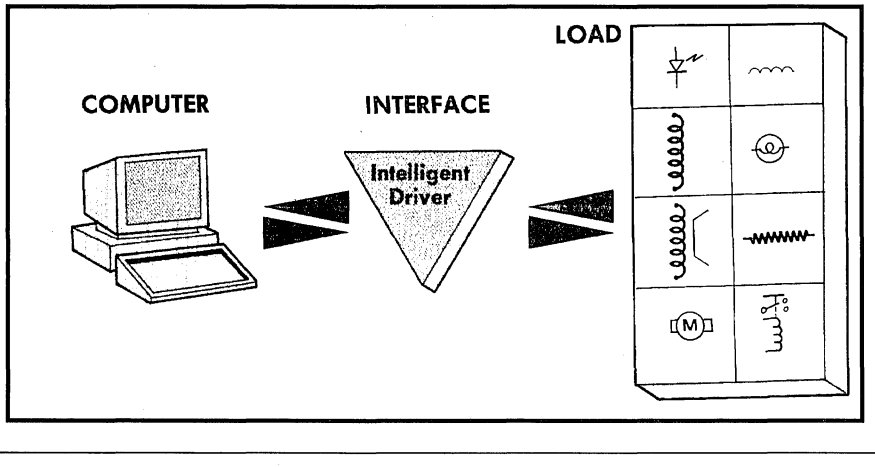


Figure 1 : There are two possible configurations of load/controller combination. Some standards and forthcoming projects will require one end of the load to be directly connected to ground.

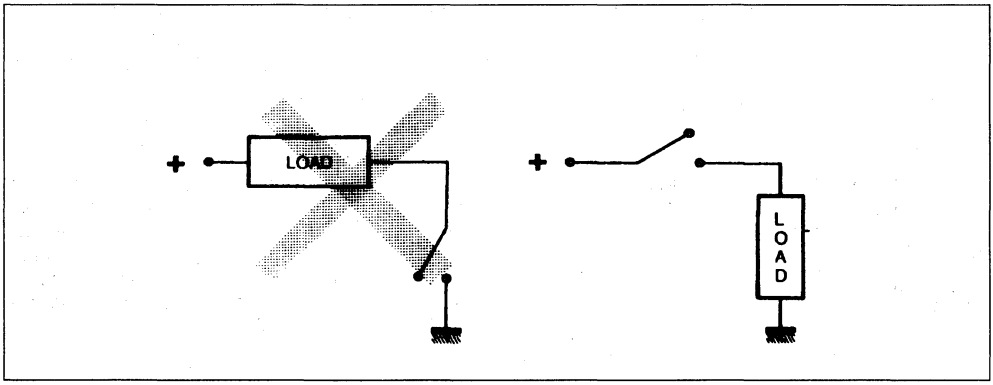
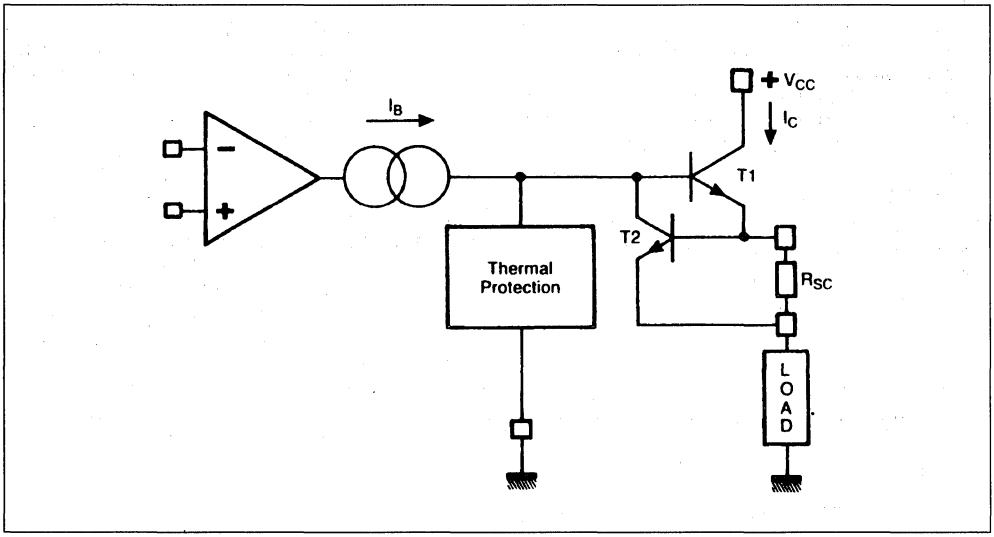


Figure 2 : Basic Functional Diagram of TDE 1647.



These features make the TDE 1647 which is the basic circuit of the family, a switch well-suited to applications implementing drives for lamps, inductive loads, blinkers and relays, etc.

It is worth mentioning that the current limit feature when used to limit the starting current, will in the case of incandescent bulbs, result in a considerable extension of their life duration.

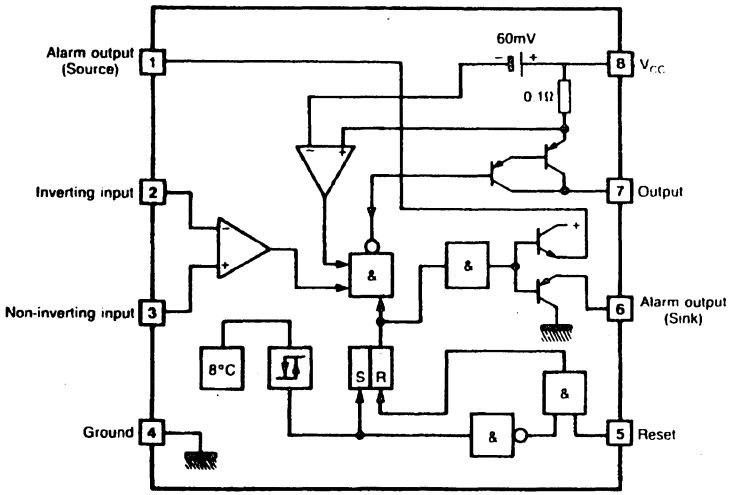
INTERACTIVITY – A SECOND FAMILY OF CIRCUITS

In many applications, the control system must receive the acknowledgement of the execution of an issued command, or receive information reflecting possible failures and disturbances. The TDE1798 has been designed to meet these requirements (see figure 3).

This autoprotected driver contains memory logic circuitry required to latch the device status and return the stored information to the processor.

This device is protected against thermal overloads exactly in exactly the same way as TDE1647 and in addition, if Reset input is held low, the driver output remains blocked after a thermal overload and this condition is indicated by a signal sent through the Alarm output pin. The Reset input is used to return the circuit to its normal mode of operation. In fact, if this input is maintained high, the device will operate in exactly the same way as TDE1647 that is, in case of continuous overloads, it will function in a low-frequency relaxation mode.

Figure 3 : TDE 1798 Autoprotected Control.



SHORT-CIRCUIT PROTECTION.

This device is protected against short-circuits by a current-limit feature operating exactly the same as the preceding device. Under overload conditions, the current is limited but the memory logic function is inactive.

POWER SUPPLY VOLTAGE LIMITS.

All of the devices of the entire family operate in a wide range of supply voltages : from + 6V to maximum voltage (between + 3V and + 6V, the protection logic is operational but the temperature detection circuit becomes inactive).

INDUCTIVE LOADS.

If a free wheel diode is connected across an inductive load, the voltage drop remains null while current decays slowly (figure 4). Two distinct solutions are possible to provide a rapid fall of this current :

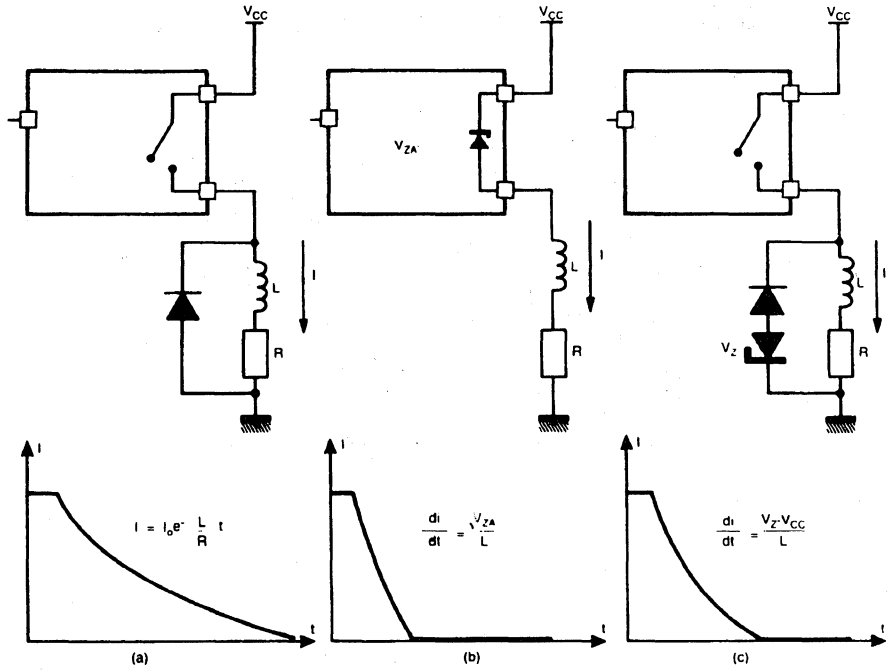
a)- Do not connect any additional device across the load. The output transistor of TDE1767/TDE1798 has been particularly designed to operate in avalanche mode and to clamp at voltage V_{ZA}. This outstanding feature eliminates the need of additional components in the case of inductive loads and automatically provides a rapid fall of load current.

As far as the users are concerned, this is an interesting feature. However, care must be taken not to exceed the operating limit of this transistor ; that is, energy dissipated in the transistor ($\frac{1}{2}LI^2$) should be less than 100mJ.

b)- In the case where energy stored in the load is very large, a Zener diode may be used to absorb this energy.

In case (b), the device and its internal logic circuits are protected against negative voltage peaks appearing between output and ground (figure 4).

Figure 4 : Current Decay in an Inductive Load.

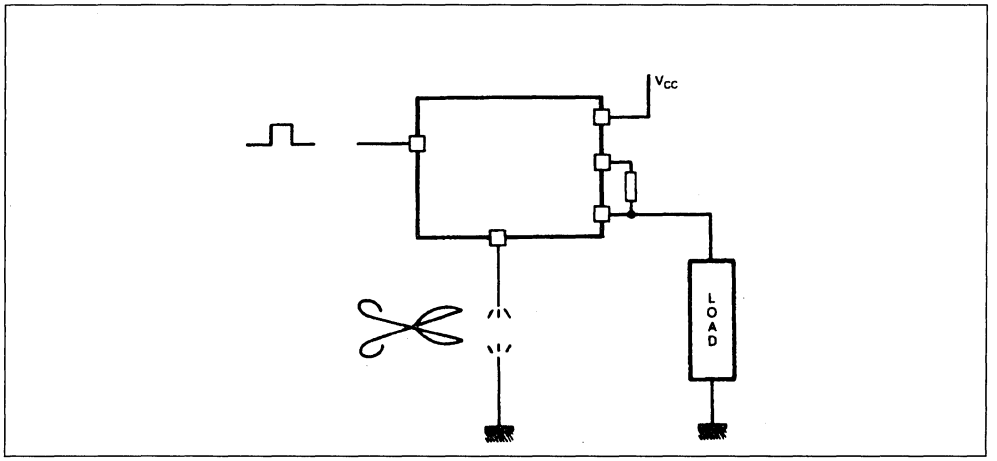


a) – With free wheel diode.
b) – Without free wheel diode – the internal transistor operates in avalanche (@ voltage V_{ZA}).This condition offers the most rapid current fall.
c) – Addition of an auxiliary avalanche diode, $V_Z \leq$ V max.peak voltage accepted by the circuit. Note that these devices have been designed to withstand peak negative voltages of as high as $V_{CC} - V_{ZA}$ between output and ground teminal.

GROUND DISCONNECTION.

Besides the protection against disconnection of the power circuitry, these devices are also protected against accidental disconnection of ground return path. This is an outstanding security feature and the TDE1798 was particularly developed to meet VDE422, the European standard which requires an instantaneous disabling of the output circuitry in case of accidental disconnection of ground (figure 5).

Figure 5 : The autoprotected control meet European security standard requirements. Output is automatically disabled in case of accidental disconnection of ground path.



ANOTHER PROGRAMMABLE CIRCUIT.

TDE1767 is another version of this circuit which in combination with an external resistor, implements a programmable short-circuit detection feature.

HIGHER POWER – OPTIMUM SECURITY

The control discussed so far are specified for output currents of 0.3A to 0.5A. TDF1778 & TDF1779 are dual autoprotected control capable of handling up to 2 x 2A. These monolithic devices contain 2 individual drivers which share a common monitoring logic circuitry (figure 6).

Protection features offered by these circuits are :

A thermal protection feature similar to circuits mentioned earlier.

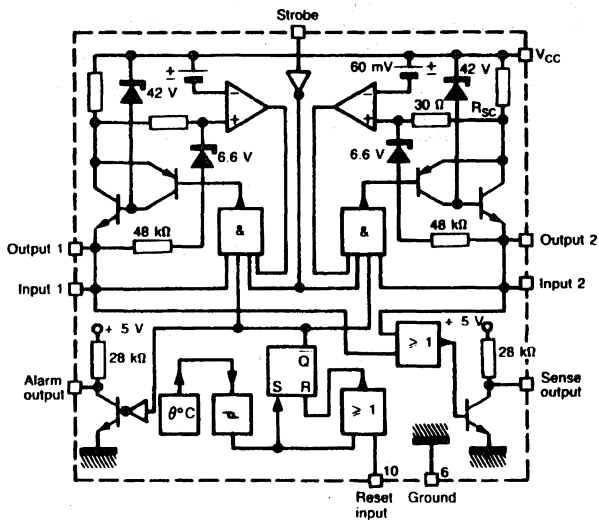
Signalling Logic, Fault Memory and the availability of a Reset input (similar to preceding circuit).

Short-circuit protection. If the device is operated with current of the order of 2A, safe operating area of the transistor must be taken into account. Figure 7 illustrates the characteristics of the integrated protection unit. The fault memory feature is inactive when device is in current limit mode.

The output transistor of these circuits is not protected in avalanche. However, in the case of TDF1778, a 42V Zener diode inserted between the positive supply and the base of the output transistor, will transform it to an avalanche protected transistor.

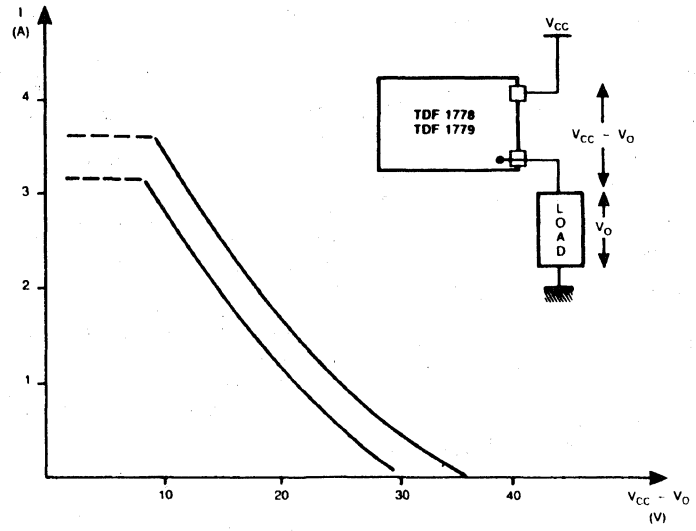
An additional feature, detection of load disconnection, is also offered by these circuits. A high-value resistor (not shown in the figure 6) is connected between the power supply terminal and the outputs. As long as the load remains connected to the output and the input is blocked, the output potential is practically null. If the load is disconnected, this potential will rise and correspondingly, a signal is sent to the central unit through the Sense Output terminal.

Figure 6 : TDF1778 Autoprotected Control.



Dual output : 2 x 2A. Fault memory. Thermal and short–circuit protection.
Detection of and protection against ground and load disconnection.

Figure 7.



Current protection limit. For TDF1778 and TDF1779 devices, this varies as a function of $V_{CC} - V_O$ voltage appearing across the controller. This limit corresponds to the safe operating area.

APPLICATIONS

Main characteristics of this family of AUTOPROTECTED CONTROL are :

- Particularly suited to 24V to 48V - 0.3A to 4A systems.
  - Operation from + 6V to maximum voltage.
  - Can be used in parallel configuration.
- Protection against :
  - Over-currents.
  - Excessive heating.
  - Accidental ground disconnection.
  - Interactive dialogue with central processor unit (ALARM & RESET) terminals available on certain series.
  - Detection of load disconnection (TDF1778 & TDF1779).
  - Protection of output transistor by avalanche (some families).
  - µP and TTL compatible inputs.

Figure 8 illustrates some conventional industrial automation applications built around these devices.

Power handling capability of these devices can be readily enhanced by the addition of an external power transistor as shown in figure 9. Further to these conventional applications, autoprotected control are also well suited for the implementation of choppers (figure 10) and more complex circuits (Bridge, Half bridge...).

FUTURE EVOLUTION

Two trends for these circuits :

- Enhancement of power handling capability.
- Reduction of losses - A new circuit offering considerable reduction of voltage drop and thus the losses, is forcast to be available in 1986. One of the consequences will be improving the circuit density in the equipment, thus achieving size reduction.

CONCLUSION

This new family of devices opens a new era of controllers which are :

- On one hand stand-alone, i.e. self-protected against external disturbances. If operated in this mode, in case of fault occurence, the device itself will make the appropriate decision without the intervention of the central processor unit.
- On the other hand, capable of interactive dialogue, which means they are readily associated to processors and monitored by digital systems.

Figure 8 : Some Typical Applications of Autoprotected Controllers.

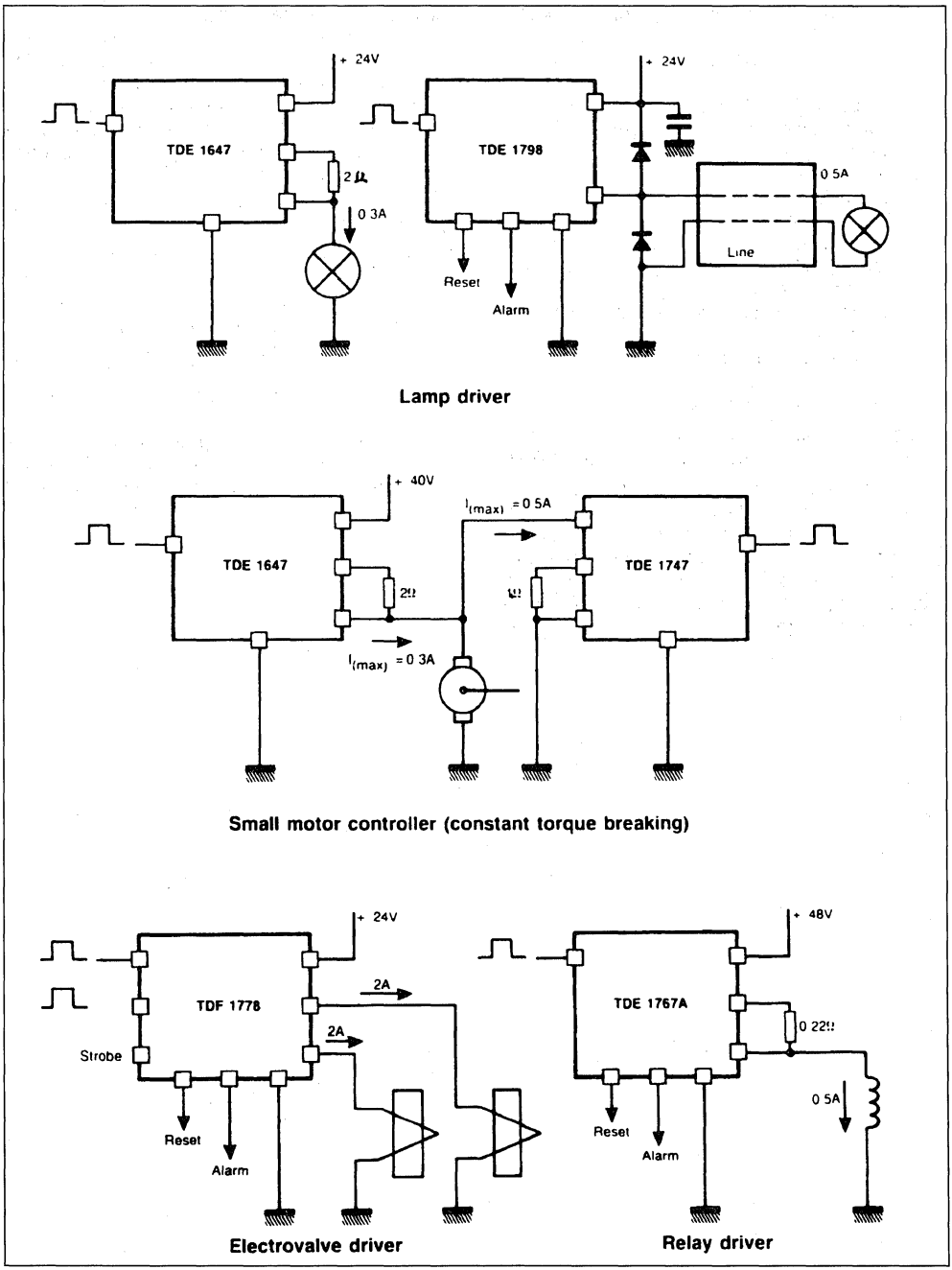
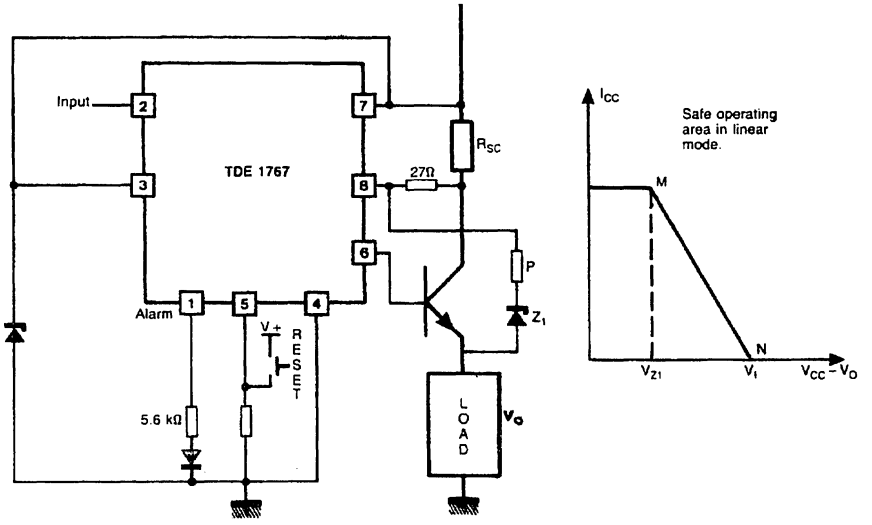


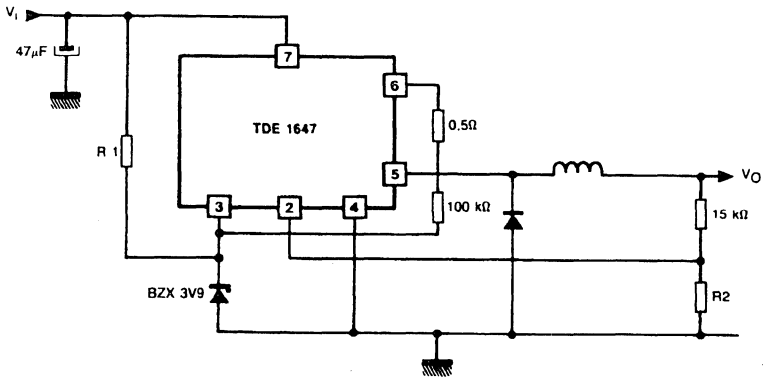
Figure 9 : TDE1767 Power Boosting.



RSC resistor determines the short–circuit current.
Voltage V_{Z1} determines the abscissa of point M.
Resistor P determines the abscissa of point N.

VI (V)	R1 (KΩ)	R2 (KΩ)	VO (V)
+ 12	62	1.5	+ 5
+ 18	91	3.5	+ 12

Figure 10 : Voltage Step–Down Chopper.



INTERFACES DEDICATED TO PROCESSES CONTROL

By J.M. BOURGEOIS & L. PERIER

Controlling tasks are very common in many areas, for example the control functions associated with buildings, the factory automation control, the production and control of energy, the chemical industries...

These tasks are genrally managed by process controlers or industrial micro computers linked to a supervisor and sometimes a dedicated computer.

At the control level, sensors and actuators are the means of controlling the physical processes, and are monitored and driven by the process controller interfaces.

- 90% of system failures are due to the wiring or the sensors/actuors. Wiring may be reduced by the use of a field BUS and the distributed interfaces.
- Considering the remaining 10% of failures, 90% of them are due to the input/output interfaces.

Thus, if the reliability of the interfaces and the diagnostic functions are improved, the availability of the system increases (working time/wirking time + stopping time). A good means to achieve that is to use integrated self protected interfaces allowing a telediagnostic from the controller. The devices have integrated on the same silicon chip the safety and diagnostic functions and the power switch.

A better availability is achieved by mixing integrated interface with field BUS, decreasing the first 80% of errors, and the installation cost of the system.

A FAMILY OF INTEGRATED INTERFACES

The family of new circuits are dedicated to drive any type of inductive and resistive loads.

Their main characteristics are :

* No indeterminate states up on power on.
* Short circuit protection with the positive supply and ground by current limitation.
* Over heating protection.
* Protected against overloads.
* Alarm output with delay.
* Open ground protection.
* Output voltage can be lower than ground for fast inductive load demagnetisation.
* Differential input for universal logic compatibility.
* Output paralleling capability.

Generally, hybrid or discrete circuits are used for these interface functions in process controller. Using integrated devices is cost effective and provides a better thermal protection because of the integration of the temperature sensor. As consequence, overload protection is totally reliable. Integrated interfaces are available in high side and low side configuration, for a range of current from 0.5A to 2A. They operate with a supply voltage range of + 8V to + 32V, a typical block diagram of one of these devices, the UAB/UAF 1780, is shown in Figure 1.

APPLICATION CIRCUIT OF THE UAB/UAF 1780

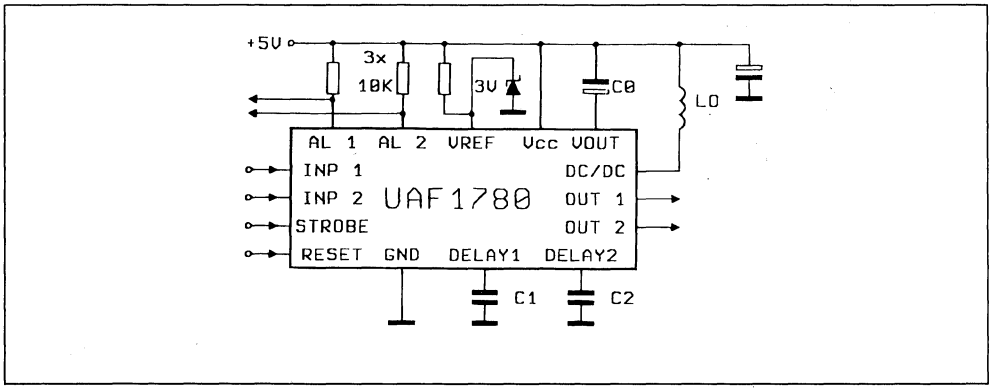
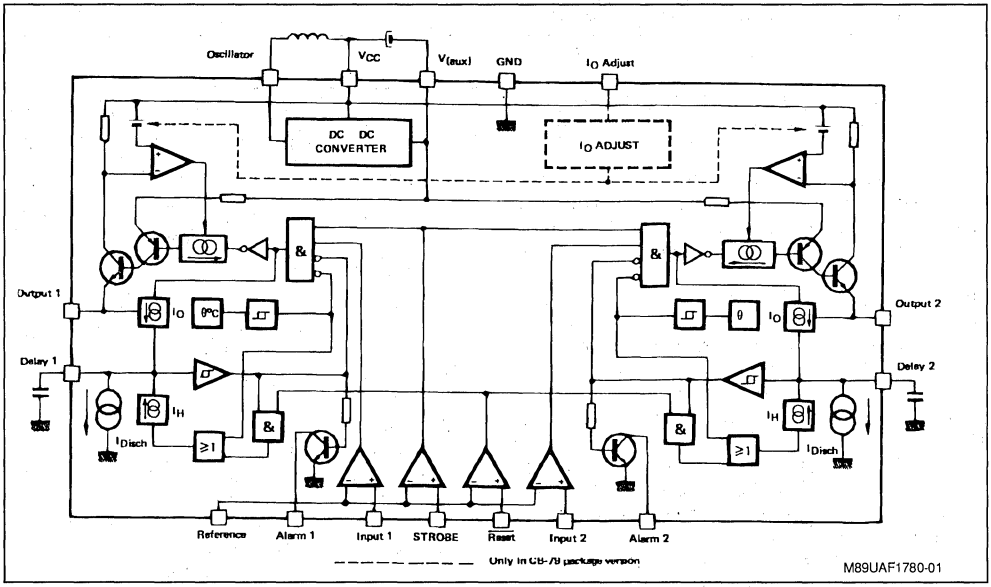


Figure 1 : UAF 1780 Structure.



APPLICATIONS

A local peripheral was designed for use by a micro computer or process controllers. The circuit uses four UAB/UAF 1780 which are dual integrated interfaces delivering up to 1A without heatsink and more than 2A with. The interfaces are driven and monitored by a Z86E11 micro controller whose UART allows the communication link with a serial field BUS.

Figure 2 shows the block diagram of the system.

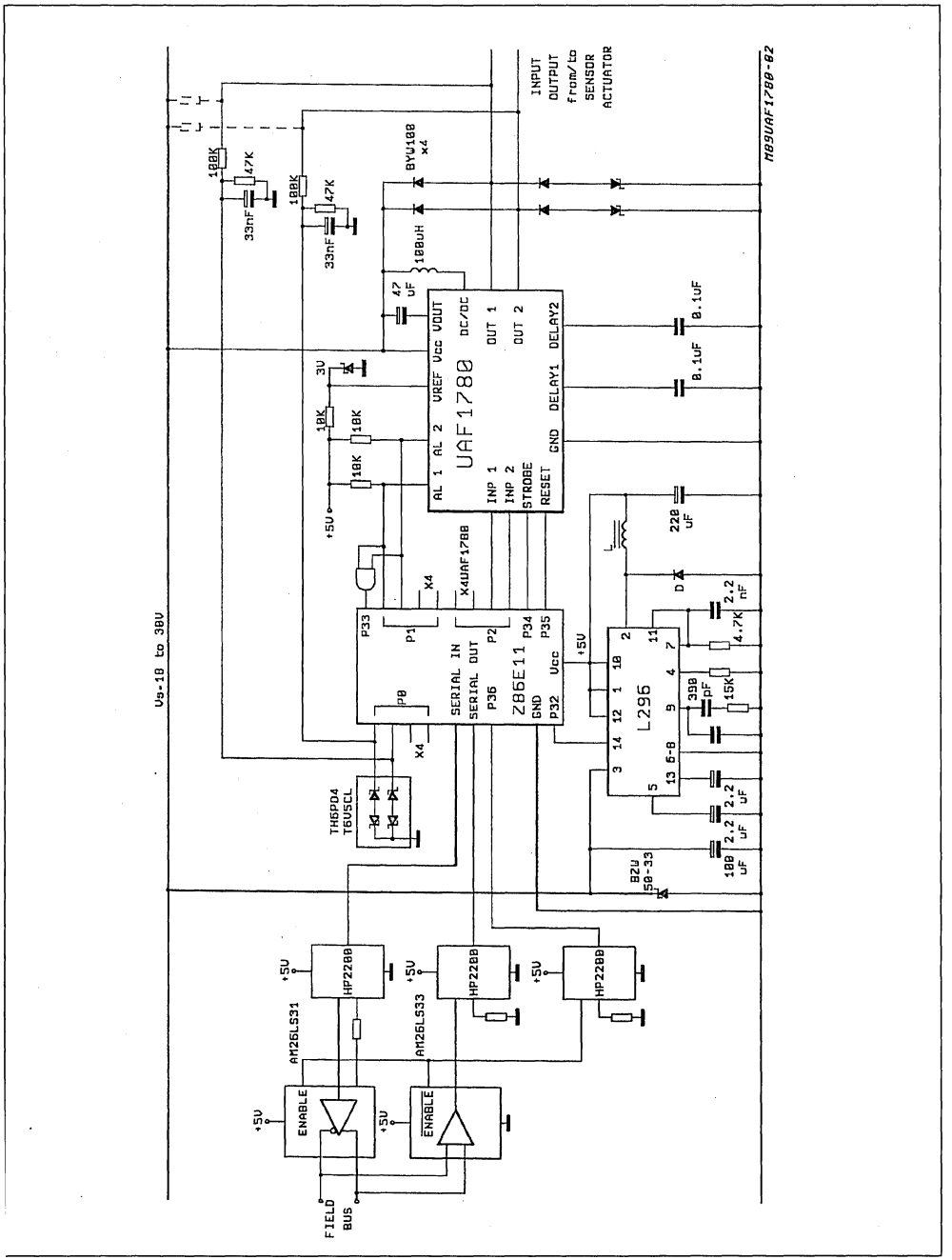
The configuration of the output of the integrated interface allows each output to be used as on input (via P_0) if desired. Only one of the four UAF 1780 is showed on the figure.

- In output configuration, the interface controls and minotors the load. The feedback signal to the port P_0 means that the state of the output can be monitored increasing the diagnostic capability
- In input configuration, the interface is off and the signals are read via the P_0 port.

List of items :

* UAB/UAF 1780 : Intelligent full protected power switch
* Z86E11 : 8 bits microcontroler
* TRANSIL TH6P04T6V5CL : Octal protection zener in DIL package
* L296 : High current switching regulator with reset output
* AM26LS31 : High speed differential line driver
* AM26LS33 : Differential line receiver
* TRANSIL BZW5033 : Transcient voltage suppressors 5Kw/1msec
* BYW100/100 : High efficiency ultra fast diodes V_{RRM} = 100V trr = 25/60nsec Vf = 0.85V

Figure 2 : Block Diagram of the Peripheral.



MAIN CHARACTERISTICS OF THIS PERIPHERAL

a) Inductive load demagnetisation :

The ability of the integrated interfaces output to sustain negative voltage up to 30V, provide a very fast demagnetization of inductive loads.
The size of the Zener diode depends on its voltage, the load current and the commutation frequency.

b) Noise and spike immunity.

The interfaces are supplied directly from the local 24V line. Because they withstand voltage spikes of up to 60V for 10ms, a transil is an effective protection for supply disturbances.

The outputs are protected by diodes connected to the ground and to supply to ensure the interface outputs are not subjected to parasitic voltage spikes.

c) Interrupt priority register.

–The first priority is given to the switching regulator L296 which warns the micro controller when there is an interruption in the supply voltage. This regulator provides simultaneously two auxiliary supplies one of which is isolated and used for the field BUS interface AM26LS31.

–The second priority is used for the communication with the host computer via the UART.

–The third priority is used to monitor the default signal of the UAF1780 interfaces.

d) Field BUS interface :

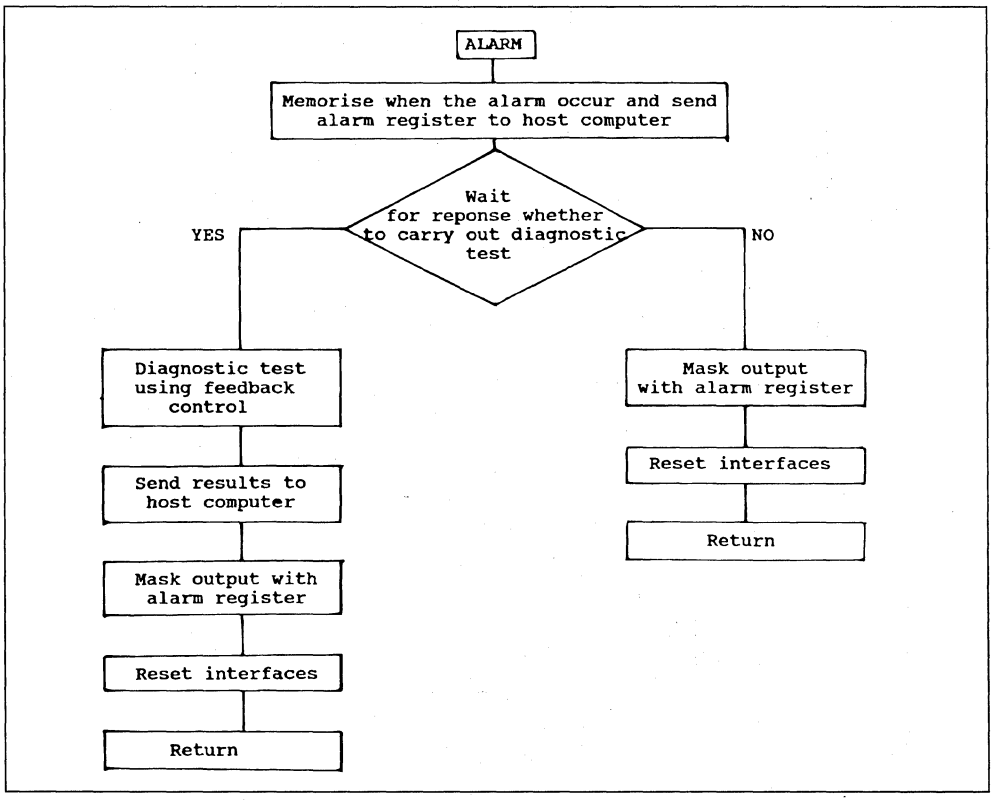
The galvanic isolation of this peripheral requires only three opto couplers because of the multiplexing of the INPUT/OUTPUT and alarm signal.

e) Efficiency :

The high efficiency of these integrated interfaces is due to an integrated DC/DC converter which reduces the on state voltage of the output Darlington stage.

DIAGNOSTIC CONTROL

When alarm output is enabled, the following processus is started.

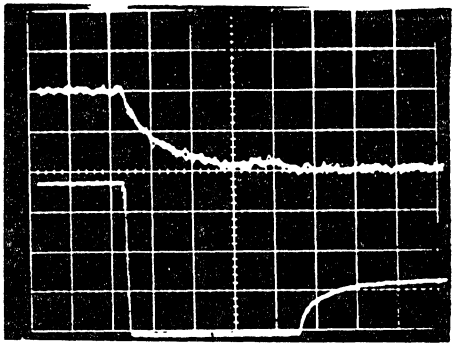


INTERFACE BEHAVIOUR

a) Inductive load.

Figure 3 shows the turn-off commutation with an inductive load, the demagnetisation zener diode used was 10V. This diode provides a current path for the load demagnetisation and a protection against negative spikes induced from in the wiring.

Figure 3 : I load : 0.4 A/div
V out : 10 V/div.

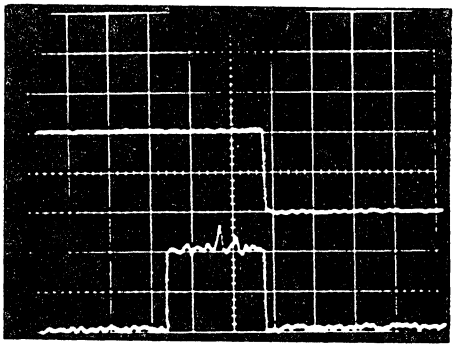


t : 20 msec/div.

b) Short circuit behavior :

Figure 4 shows the output current and the alarm signal in case of short circuit. The current is internally limited for a preset delay, after which a low level is applied on the alarm output and the current switched off. This device can be reactived by the reset input.

Figure 4 : V alarm : 2 V/div
I load : 2 A/div.



t : 1 msec/div.

c) Over heating detection :

Figure 5 shows the output current and alarm signal in case of over heating detection. When the silicon chip reaches 150°C, the current is switched off and the alarm output actived. If the reset input is low, the switch restarts after the thermal hysteresis cycle and a preset delay. If the reset is high, the switch will remain off and the alarm low.

CONCLUSIONS

This family of integrated full protected interfaces provides more reliability in process control. Due to the alarm output, the real time diagnostic function can easily be multiplexed with a low cost micro controller.

The set of devices used for this application is optimized and provides a high immunity against all disturbances from the line voltage, the wiring and the loads.

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HIGH SIDE MONOLITHIC SWITCH IN MULTIPOWER-BCD TECHNOLOGY

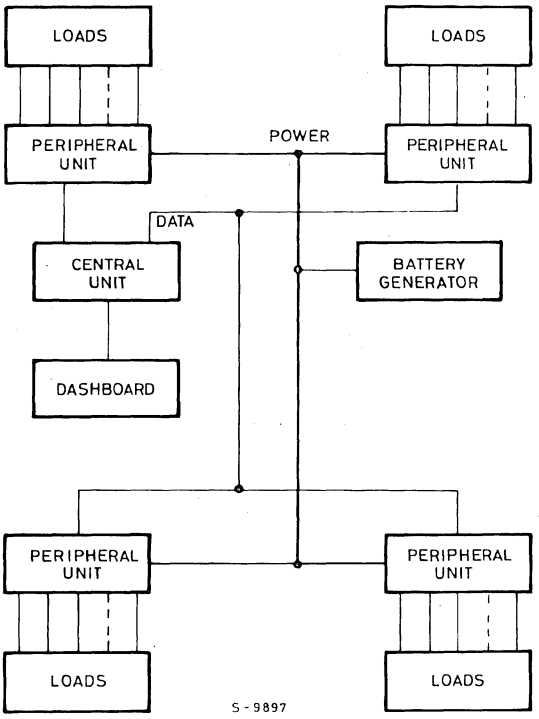
by C.Cini, C. Diazzi, D. Rossi, S. Storti

Recent advances in integrated circuit technology have allowed the realization of a new mixed process integrating isolated DMOS power transistors in combination with bipolar and CMOS signal structures on the same chip. Called Multipower-BCD, this technology has been used to realize a monolithic self-protected high-side switch mainly intended for automotive applications. Driven by TTL, CMOS input logic it can supply resistive or inductive loads up to 6A DC allowing a current peak of 25A with an $R_{DS(on)} = 0.1\Omega$. Fault conditions are signaled on a diagnostic output pin.

ELECTRONIC POWER SWITCHES IN THE CAR

The increase of the number of the electrical components in the car (today more than 50) and the increase in assembly costs shall soon make economical multiplexed power supply and control systems. These systems consist of a single line for power supply and a multiplexed signal network for control ; in this way it is not necessary to have a wire for every load, but only a common power line and a common signal line for all the loads (fig. 1).

Figure 1 : Example of a Multiplexed System.



The control system is made, for example, with a central unit near the dashboard, for the user interface, a serial data transmission line and some peripheral units near the loads (fig. 2).

The multiplexed system not only makes it possible to reduce weight and overall dimensions of the cable harness, now critical in some places (e.g. the junction between the vehicle body and the doors), but, also makes it possible to have a bidirectional signal between peripheral units and the central unit without any extra line, this is useful for fault detection and, in a future, for data transmission to make a more complex informatic system.

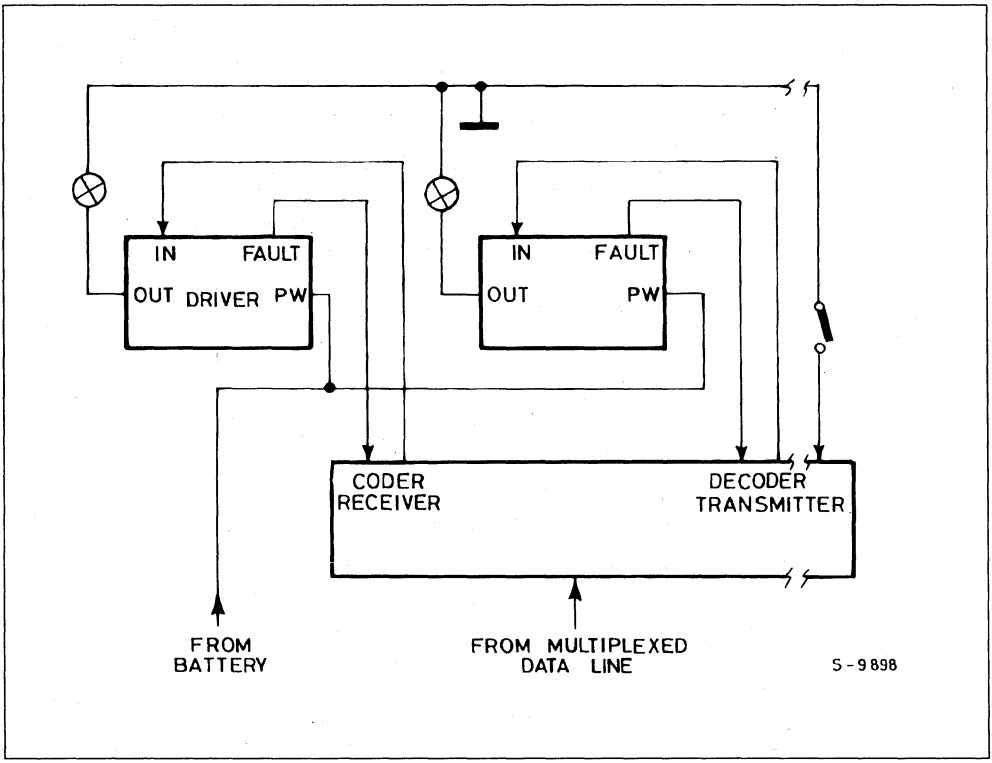
Today the key problem, from the system engineering point of view, is data transmission whereas for semiconductor technology the key problem is the electronic power switches.

The electronic switch, in addition to its main function, must be able :

1) to withstand a very high peak current (20A) with total battery voltage (≡ 14V) applied.
2) to protect itself, the power network and the load against overvoltages (load dump ≡ 60V) and overload (protection with fuses is impractical),
3) to make some fault detections e.g. detect short circuit or open load condition.

For this reasons a simple electromechanic or electronic switch standing alone is not sufficient, a more complex circuit is necessary and for this the monolithic solution is the most effective.

Figure 2 : Block Diagram of a Peripheral Unit.



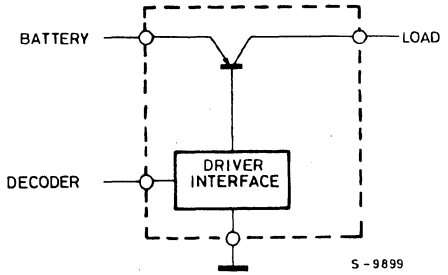
HIGH SIDE DRIVER

The problem of electrochemical corrosion is of primary importance in automotive systems because the electrical components are in an adverse environment (temperature, humidity, salt), for this reason the series switch is connected between the load and the positive power source. Therefore when the electrical component is not powered (that is for the greatest part of the lifetime of the car) it is at the lowest potential and electrochemical corrosion does not take place.

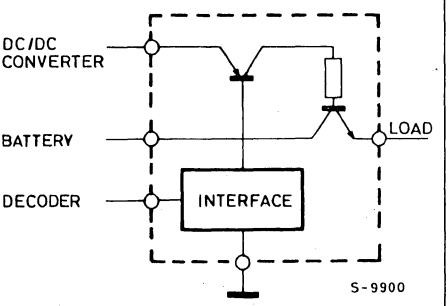
For this connection, components such as power PNP bipolar transistor or Power P-channel MOS would be integrated with low level signal circuitry (fig. 3a), but this kind of element is less efficient and more difficult to realize than their complementary one. NPN bipolar transistors or N-channel MOS, if directly driven by the supply voltage, are not a good solution because the minimum voltage drop on the switch is V_{BE} or V_T (threshold voltage) ; the best solution is to have a driving voltage for the power transistor, higher than the positive supply. Nevertheless a power junction NPN transistor (fig. 3b) needs a certain amount of base current (β = 10-60 to have deep saturation) that could be obtained with a DC-DC converter ; if centralized it complicates the power supply distribution network, if decentralized it complicates the peripheral unit always critical for size, reliability and cost.

Figure 3 : Possible High Side Drivers.

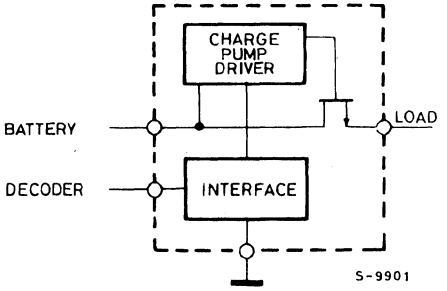
A) with PNP pass transistor



B) with NPN pass transistor (needs external DC-DC converter)



C) with N CHANNEL DMOS



On the other side a POWER MOS N-channel (fig. 3c), being a voltage driven device, requires for the driving only a capacitive charge pump which can be fully integrated on the switch chip.

Bipolar transistors moreover need driving power and principally, are limited in maximum peak power by second breakdown.

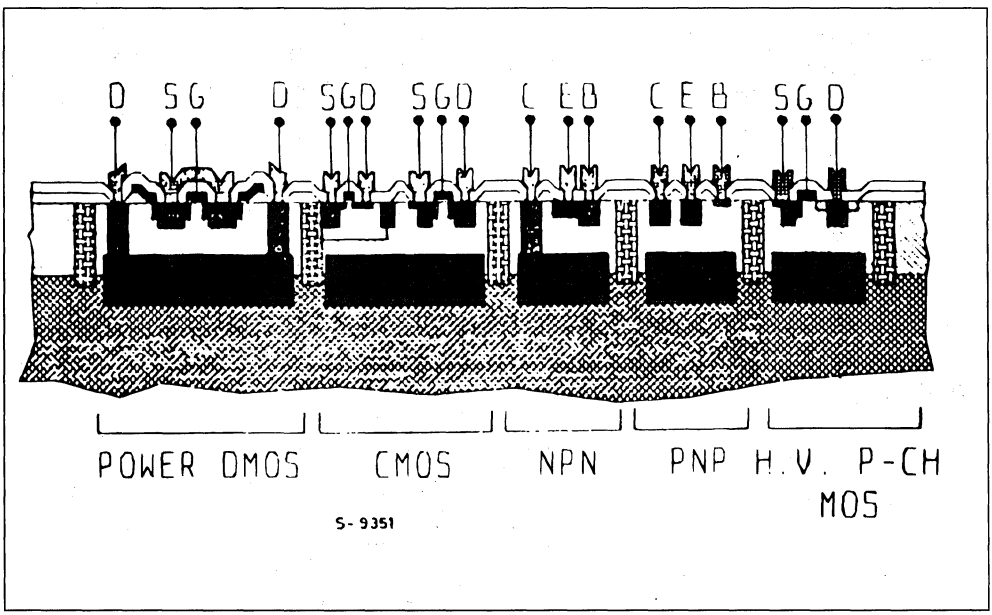
THE PROCESS TECHNOLOGY

For the realization of the device a mixed Bipolar-CMOS-DMOS process has been utilized. This process integrates the following components (tab.1) (Fig. 4) :

Table 1 : Devices in Multipower-BCD Technology.

VERTICAL D-MOS	BV_{DSS} > 60V	V_{TH} = 3V	f_T = 1GHz
P-CHANNEL DRAIN EXTENSION	BV_{DSS} > 75V	V_{TH} = 1.9V	f_T = 200MHz
C-MOS N-CHANNEL	BV_{DSS} > 15V	V_{TH} = 0.9V	
C-MOS P-CHANNEL	BV_{DSS} > 15V	V_{TH} = 1.9V	
BIPOLAR PNP	V_{CEO} > 20V	β = 30	f_T = 10MHz
BIPOLAR NPN1	V_{CEO} > 20V	β = 30	f_T = 300MHz
BIPOLAR NPN2	V_{CEO} > 20V	β = 250	f_T = 1GHz
BIPOLAR NPN3	V_{CEO} > 20V	β = 250	f_T = 140MHz

Figure 4 : A Schematic Cross Section of Bipolar, CMOS and DMOS Structures.

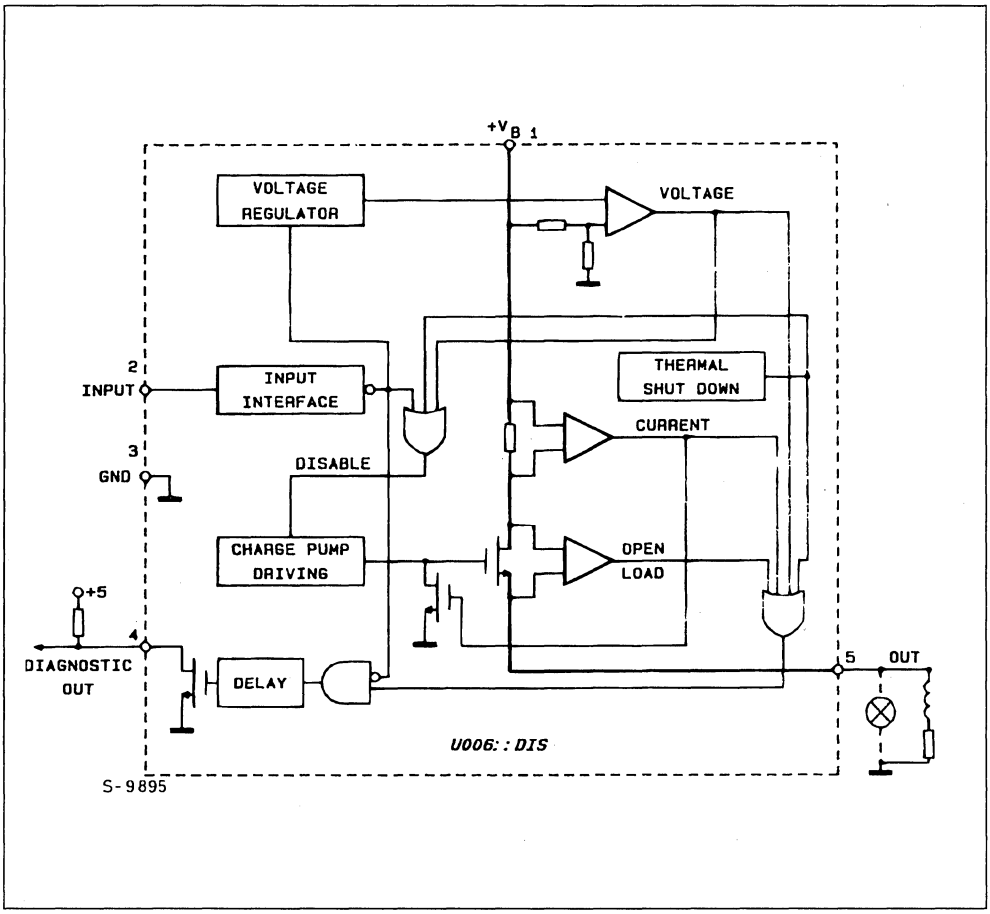


- N-CHANNEL POWER DMOS able to withstand V_{DS} = 60V for the series element.
- BIPOLAR NPN AND PNP TRANSISTORS mainly employed in analog circuitry where low offset and high gain are needed e.g. voltage comparators and references, operational amplifiers.
- CMOS TRANSISTORS to realize a dense logic network with stand by currents practically negligable.
- PASSIVE COMPONENTS as resistors with a great variety of sheet resistivity (30+8500Ω/□) to optimize both very high and very low resistive circuitry and gate oxide capacitors (e.g. to realize charge pump capacitors).

THE CIRCUIT

The circuit (fig. 5) is made by a power DMOS series element, a driving circuit with a charge pump, an input logic interface and some protection and fault detection circuits.

Figure 5 : Block Diagram of High Side Switch L9801.



THE POWER DMOS

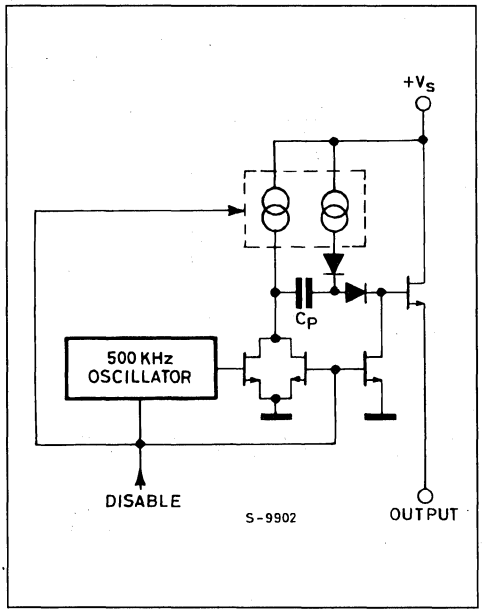
The power DMOS transistor is an array to 10,000 elementary DMOS cells that occupies an area of about 19,000 mils^2 and has a $R_{DS(on)}$ = 80mΩ with V_{GS} = 10V. The low value of $R_{DS(on)}$ is required both to increase the power transferred to the load and to minimize the power dissipated in the device. In fact the switch must be operative also at very high ambient temperature (125°C) as required in automotive applications. For example to drive a 5A (60W) load, the drop on the switch is 400 mV and the dissipated power is 2W ($R_{th\ j\text{-}case}$ 1.25°C/W).

THE CHARGE PUMP

The charge pump is a capacitive voltage doubler (fig. 6) starting from power supply (car. battery), driven by a 500 KHz oscillator.

The pump capacitor is an integrated 80 pF capacitor, the storage capacitor is the gate capacitance of the power itself (~ 500 pF).

Figure 6 : Charge Pump.



INPUT INTERFACE

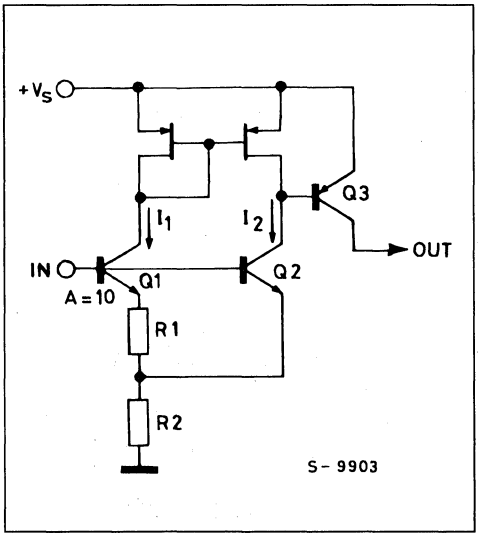
Considering the very wide operating temperature range (Tj = 40 to + 150°C) it is not possible to obtain the logic threshold from the conduction threshold of any elementary device, because of its temperature coefficient, respecting TTL input levels.

Nevertheless a solution with a voltage reference and comparator is not suitable because it needs a bias current flowing also when the device is in the OFF state.

This point is of great importance because the switches are directly connected to the car battery without the interposition of the ignition switch, thus also a little current (> 50μA) multiplied for the number of the switches (e.g. 50), causes an appreciable discharge current always flowing.

For this reason a threshold circuit has been designed derived from a well known voltage reference (fig. 7).

Figure 7 : Input Interface.



Fixed a threshold value $V_{IN} = V_{IN}^*$ for this value must be, by design $I_1 = I_2 = I_0^*$.

if α = area ratio $\quad \alpha = \dfrac{A_{Q1}}{A_{Q2}}$

must be $\quad I_1 = \dfrac{\Delta V_{BE}}{R1}$

$$(I_1 + I_2)\, R2 + V_{BE}\,(Q2) = V_{IN}$$

that is $V_{IN}^* = 2\,\dfrac{R2}{R1}\,\dfrac{KT}{q}\,1n\,\alpha + V_{BE}\ Q2$

Reasoning around the threshold point it can be noted that the transconductance of Q2 is greater than the transconductance in Q1 branch (Q1series R1).

For this

if $V_{IN} > V_{IN}^*$	$I_2 > I_1$	Q3 ON
if $V_{IN} < V_{IN}^*$	$I_2 < I_1$	Q3 OFF

The choice of the values is made imposing :

1) $V_{IN}^* \equiv V_{BG} \equiv 1.250V$ band-gap voltage of silicon.

   In this case V_{IN}^* is practically stable in temperature and centered respect TTL input levels ($V_{LMAX} = 0.8V$. $V_{HMIN} = 2V$).

   The idle current I_{ABS} in the worst case, that is when $V_{IN} = V_{L\,MAX} = 0.8V$. $Tj = 150°C$, it must be $I_{ABS} = I_1 + I_2 < 50\mu A$.

The proposed circuit has also a third working region :

when $V_{IN} < V_{BE}$ $I_{ABS} = 0$ Q3 OFF

Observed that the TTL OUTPUT low level is $V_{L\,MAX}$ 0.4V with practical driving circuits the idle current of this interface is zero : only at very high junction temperature ($V_{BE} < 400mV$) or with noise margin = V_{BE} 0.4V) this performance cannot be warranted.

The output of this circuit is useful to switch off not only the power DMOS, but also all the other circuits so that the idle current only the one of the input interface.

PROTECTION AGAINST OVERVOLTAGES

When the supply reaches the maximum operative voltage (18V) the device is turned OFF, protecting itself and the load ; moreover local zener clamps are provided in some critical points to avoid that V_{GS} of any MOS transistor could reach dangerous values even during 60V load-dump transistor.

PROTECTION AGAINST OVERLOAD

If the design of this device the peculiar inrush current of incandescent lamps must be considered, in fact.

1) When the tungsten wire is cold its resistence is about one tenth of the nominal steady state value (e.g. about 300mΩ for a 12V/50V lamp).
2) The decay time constant for the turn on extracurrent of an incandescent lamp supplied with an ideal voltage source is on the order of some milliseconds.
3) A lamp powered with a constant current slightly higher than its steady state value has a turn on time on the order of 100msec. This time comparable with human reaction time is too much long for all flash-signalling devices.

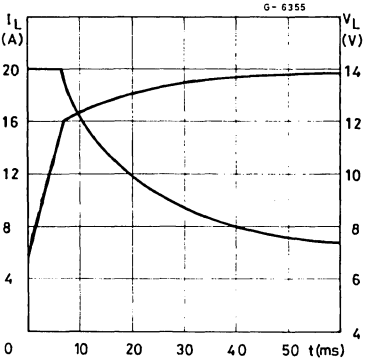
The design choice has been to put a 20A current limit (that is $I_{max} = 5\ I_{nom}$ for a 50W/12V rated lamp). This is a compromise between lamp turn on time (40msec) and electric and thermal dimensioning of the device (fig. 8).

If the high current condition persists (e.g. load short circuit) and the junction temperature rises above 155°C a thermal protection circuit turns off the device preventing any damage.

It must be noted that the power DMOS has no second breakdown, for this reason current limiting and thermal shutdown are sufficient to protect the device against any overload.

Some thermal hysteresis is provided to avoid a potentially critical condition (both current and voltage present during thermal shut down) for the POWER MOS.

Figure 8 : Lamp Current (I_L) and Voltage (V_L) vs. Time with 20A Current Limitation and 12V/50W Lamp.



FAULT DETECTION

When the device is driven and one of the protections (over temperature, overvoltage, overload) is present a fault detection open drain output turns-on. This output is active also when the drop on the POWER MOS is less than 80mV (that is $I_{load} < 1A$) detecting the open load (disconnected or burned-out).

When the device is off the fault detection circuits are not active and output transistor is turned off to allow a minimum quiescent current.

MOTOR AND INDUCTIVE DRIVING

This device can drive unipolar DC motors and solenoids as well, in fact is can recirculate an inductive current when the output voltage goes more than a threshold lower than ground. The possibility to have a high start-up current is useful also for DC motors.

CONCLUSION - FUTURE DEVELOPMENTS

A process allowing the integration of power DMOS, CMOS and BIPOLAR transistor makes possible the construction of a monolithic switch comprehending also protection and fault detection functions.

The power DMOS approach allows also the possibility to make a large range of power switches with different ON resistance and current capability only scaling proportionally the power area.

Moreover the CMOS structures can be utilized to make also the coder/decoder circuit to interface directly the transmission line.

Those features and the possibility to integrate more than one power element on the same chip makes possible, in a near future, the integration of the whole peripheral unit.

POWER SUPPLY

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

DESIGNING WITH THE L4963 MONOLITHIC DISCONTINUOUS MODE POWER SWITCHING REGULATOR

by M Roncoroni

The L4963 is a new switching regulator designed to operate in discontinuous mode, reducing the number of the external components, giving a very cost effective solution. This application note explains how the device operates and how it can be used. Typical application circuits are also described.

The L4963 is a new monolithic stepdown switching regulator IC operating in discontinuous mode. This device, able to deliver 1.5A to the load at a voltage of 5.1V and up to 36V with derated current, is designed to satisfy very low cost applications due to the fact that the number of the external components are dramatically reduced.
Moreover the inductor value is reduced by a factor of three or four in comparison with a corresponding continuous mode solution. Also the plastic package (Powerdip 12+3+3), that needs no heatsink, contributes to decreasing the cost of the overall application.

Although the L4963 is intended for very low cost applications, it integrates features like remote inhibit, reset and power-fail outputs for microprocessor.

In the following we will explain in detail its principle of operation and the criteria that regulate the choice of the external components.

CIRCUIT OPERATION

The L4963 operates in discontinuous mode. In principle in this kind of operation the energy stored in the inductor is fully discharged to the load before to start a new cycle.
To operate in this way, the device contains, in its regulation loop, additional blocks compared to the usual Error/Amplifier, Oscillator and Pulse Width Modulator used in the continuous mode devices.

Figure 1: L4963 Block Diagram

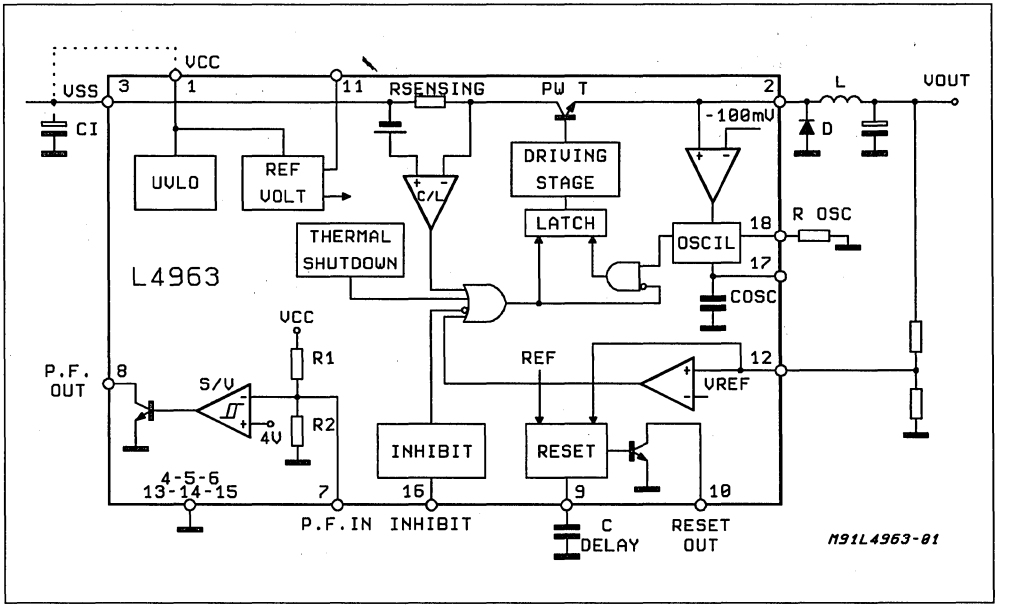
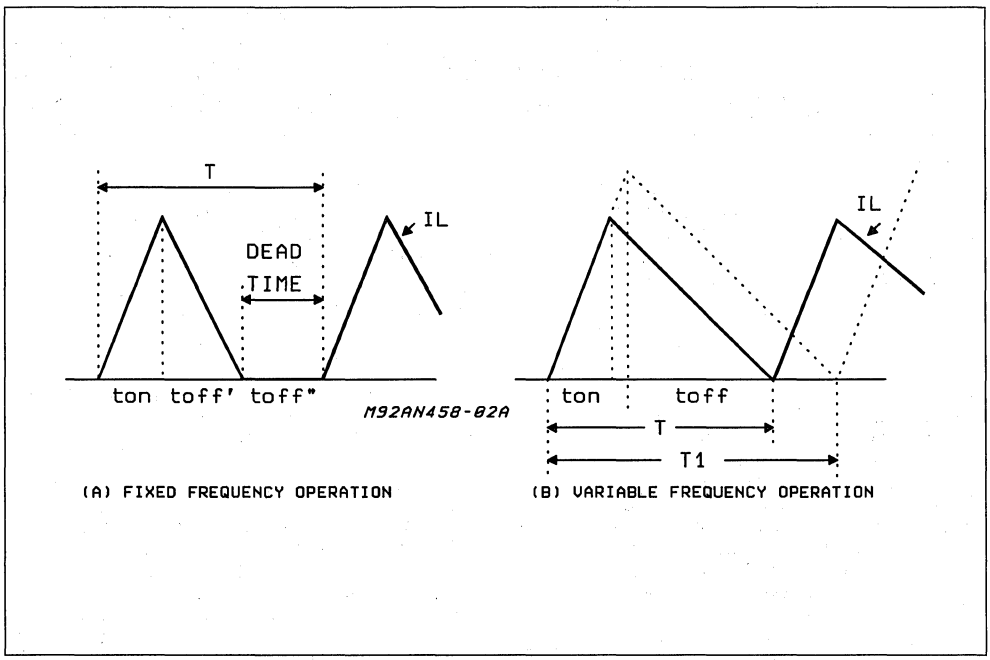


Figure 2: Waveforms



The L4963 control loop is shown in the block diagram of fig.1 and the blocks that take part to the regulation loop, are determined by the system operating conditions.

For a given value of the inductor L (that will be further calculated), if we examine the current across the inductor (I_L), we can have two different situations that modify the device operation. This two different conditions depend on the load current value that device has to deliver: changing the load current (I_O), the current through the inductor can have one of the shapes shown in fig. 2.

In both the waveforms, the current in the coil goes to zero during the T_{off} period of the power stage, but in the case shown in fig. 2A there is a "Dead Time" during which, both the Power stage and the Free-Wheeling diode are not conducting. The dead-time period ("T_{off}") increases lowering the load current. The system will start with a new cycle at the next set pulse coming from the clock. In this way the system operates in fixed frequency mode, set by the External resistor RT connected between pin. 17 and ground.

In fixed frequency mode, the current in the inductor reaches the peak value, determined by the load current, following the law:

$$I_{L+} = \frac{V_{in} - V_{cesat} - V_{out}}{L} \cdot t_{on} \quad (1)$$

When the output voltage reaches its nominal value, the E/A output resets the power stage and the discharge period starts.

When the power transistor turns off, the inductor will try to mantain the forward current constant, and the voltage at pin.2 will fly negative until the diode D is brought into conduction. The current in the inductor L will now continue to circulate in the same direction as before, decreasing linearly from the peak value to zero following the law:

$$I_{L-} = I_{peak} - \frac{V_{out} + V_F}{L} \cdot t_{off} \quad (2)$$

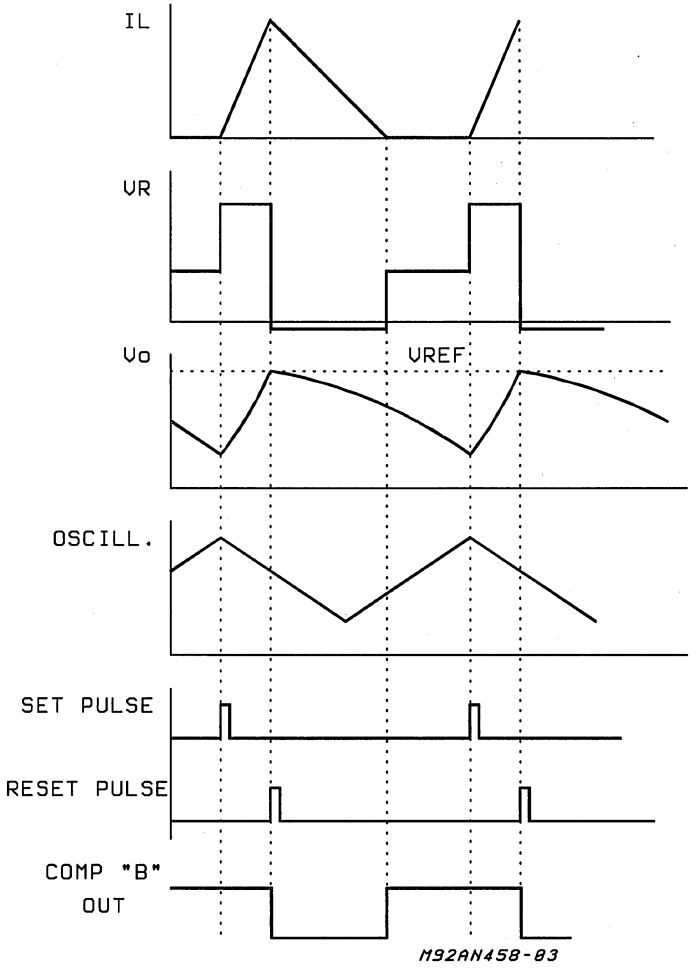
It follows, then, a third period $t_{off"}$ (dead time) during which there is no current neither across the power transistor, nor in the diode D, nor in the inductor L (the inductor runs 'DRY'). This period ceases when the next set pulse from the clock circuit enables again the power stage repeating the cycle.

The operation frequency is equal to the clock frequency, that is determined by the resistor R_t, connected between pin. 17 and ground:

$$f_{osc}\,(KHz) = \frac{0.033}{R_t\,(K\Omega)}$$

In fig.3 are shown the voltage and current waveforms associated to this mode of operation.

Figure 3: Fixed Frequency Operation



Referring again to the block diagram in fig. 1, and with a given inductor L, we suppose to have a load current that reduces the Dead Time toff" to zero. At this point we suppose that the clock send a set pulse to the latch and the power stage turns on. The current in the inductor grows from zero up to its peak value ($I_{peak}=2I_{out}$) following the law stated in Eq. 1.
If the peak current is below the Current Limitation threshold, it is again the Error Amplifier that turns off the power stage and the inductor will discharge following the eq. 2.
If the system is not able to discharge completely the inductor during the maximum toff time allowed by the fixed frequency operating mode an internal comparator, (which compares the voltage on the free-wheeling diode cathode with a precise internal reference Vr = -100mV) will mantain the power stage off until the inductor will be completely discharged.
This comparator prevents the discharge of the internal timing capacitor C_t, until the Energy in the inductor is completely discharged and the diode D ceases to conduct (see fig.4).

The system is working in a variable frequency mode, with a switching frequency that is depending on the current delivered to the load.
Bigger is the load current higher is the stored energy and longer is the time during which the comparator will block the discharge of the timing capacitor C_t, decreasing the system operating frequency. In fig.4 are shown the waveforms associated with this mode of operation.

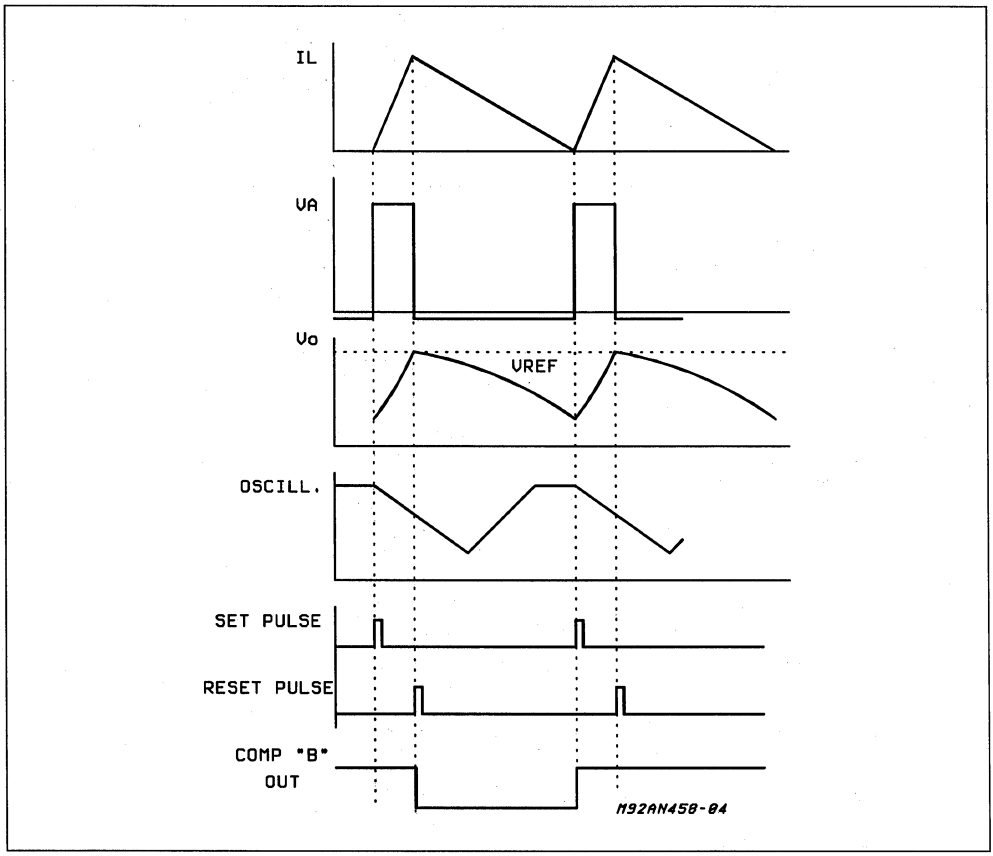
CALCULATION OF THE INDUCTANCE VALUE, L

To calculate the inductance, that is a critical element in the circuit, we have to consider that:

- The switching frequency increases reducing the load current I_{out} and increasing V_{in}.
- The switching frequency decreases increasing the load Current I_{out} and decreasing V_{in}.

So to calculate the inductor value we have to

Figure 4: Self-oscillating Operation



specify the minimum operation frequency (higher than 20KHz to avoid audible noise), for the minimum input voltage V_{in} at full load.
The equation to calculate the maximum inductor value is:

$$L \leq \frac{(V_{in(min)}) - V_{cesat} - V_o) \cdot D}{2 \cdot I_{out(max)} \cdot f_{min}}$$

$$\text{where: } D = \frac{V_o + V_F}{V_{in(min)} - V_{cesat} + V_F}$$

In overload or in short circuit conditions, the switching frequency decreases below the minimum limit fixed in standard operative conditions (f_{min}). For this reason is important to select a f_{min} with margin to avoid values inside the audible range in worst case.
Too low inductance values are not suitable because the increased ripple current in the core may generate too high ripple voltage in the output.

Example:

We want to use the L4963 in an application in the following conditions:
V_i = 15V to 35V
V_o = 5V
I_o = 1.5A (max)
f_{min} > 25KHz
V_{cesat}= 1.5V
V_F = 1V

The right inductance for this application is calculated as follows:

$$D_{max} = \frac{5 + 1}{15 - 1.5 + 1} = 0.41$$

$$L \leq \frac{(15 - 1.5 - 5) \cdot (0.41)}{2 \cdot 1.5 \cdot 25 \cdot 10^3} = 46\mu H$$

Suggested value for L is in this case 40µH that corresponds to about a 15% less the max. allowed inductance.

OUTPUT CAPACITOR SELECTION

All the considerations for the choice of the filter capacitor in a system working in continuous mode are still valid in a discontinuous mode operation (Ref. L296 Appl.note). Let summarize the results with some useful suggestion for this specific system.

The Ripple Voltage imposed on the D.C. output voltage is given by the sum of two terms. The first term (V_c), depends from I_{Lpeak}, Switch. Frequency and C_{out} values and the second (V_{ESR}) is due to Equivalent Series Resistance (ESR) of the capacitor multiplied by the I_{Lpeak} current.

$$V_o = V_c + V_{ESR} \quad (6)$$

Where:

$$V_c = \frac{I_{Lpeak}}{8 \cdot C_{out} \cdot f} = \frac{2I_{out}}{8 \cdot C_{out} \cdot f} = \frac{I_{out}}{4 \cdot C_{out} \cdot f} \quad (7)$$

$$V_{ESR} = I_{Lpeak} \cdot ESR = 2 \cdot I_{out} \cdot ESR \quad (8)$$

Once fixed the amount of ripple voltage desired for the application, with the first term we determine the minimum suitable capacitor value and with the second one we determine the maximum ESR acceptable.
Normally, for frequencies above 20KHz, the maximum ESR defines the choice of the filter capacitor value. In general, lower capacitor values have higher ESR ratings, so higher output capacitors than is calculated in eq. (7) should be used.

To guarantee a proper operation of the internal Error Amplifier, the minimum ripple voltage in the output must exceeds 15mV, to ensure a minimum voltage difference across its input terminals.

POWER DISSIPATION

It can be considered as the addition of three values:

Ptot = Psat + Pq + Psw where:

Psat: Saturation losses of the power transistor plus the sensing resistor power dissipation.

$$Psat = V32 \cdot I_o \cdot \frac{ton}{T} = V32 \cdot I_o \cdot \frac{V_o}{V_i}$$

V32 = dropout voltage between input (pin 3) and output (pin 2).

For worst case (for I2 = 3A switch current) the V32 = 2V

Pq: Losses due to the stand-by current and to the power driving current.

$$Pq = Vi \cdot I'3q + Vi \cdot I''3q = \frac{t_{on}}{T} = Vi \cdot I'3q + Vo \cdot I'' 3q$$

In fig. 6 and fig. 7 are showed these two typical values of quiescent current.

For the we worst case we can considered:

I'3q (0% d.c.) =13mA

I''3q (100% d.c.) = 17mA

Psw: Power transistor switching losses:

$$Psw = V_i \cdot I_O \cdot \frac{tr + tf}{2T}$$

Figure 5: V32 Voltage vs. Output Current

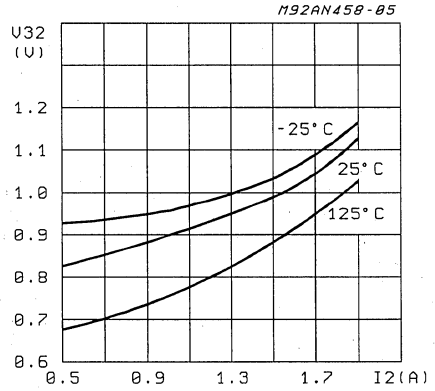


Figure 6: Quiescent Drain Current vs. Supply Voltage (0% Duty Cycle)

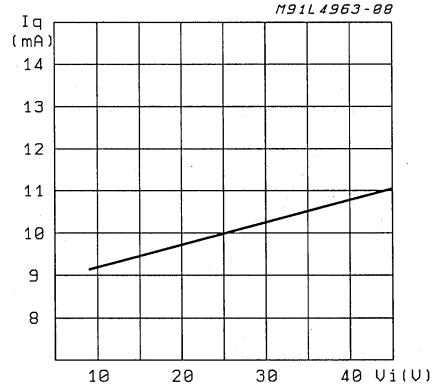
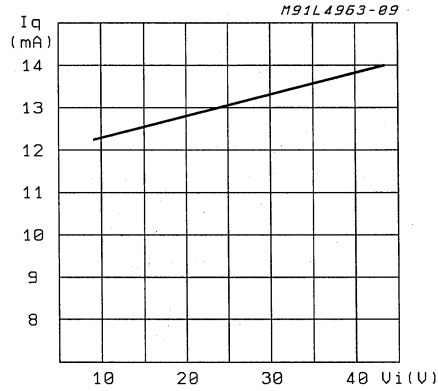


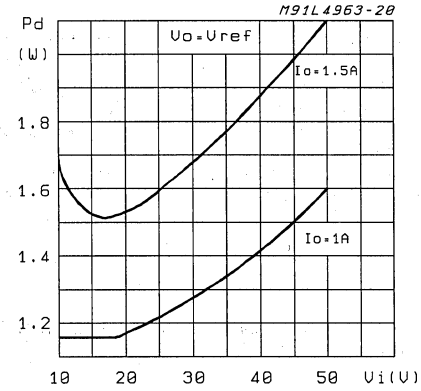
Figure 7: Quiescent Drain Current vs. Supply Voltage (100% Duty Cycle)



The fig. 8 shows the total power dissipation of the device.

For V_{out} > 5V the output current can be less then 1.5A. In fact we have to consider that the maximum power dissipation for this device is 2W at T_{amb} of 70° and is this value that limits the output current value.

Figure 8: Power Dissipation vs. Input Voltage.



EFFICIENCY

The system efficiency is expressed by the following formula.

$$\eta\% = \frac{P_O}{P_i} \; 100$$

where $P_O = V_O \, I_O$ (with $I_O = I_{load}$)

is the output power to the load and P_i is the input power absorbed by the system. P_i is given by P_O plus all the other system losses. The expression of the efficiency becomes threfore the following.

$$\eta = \frac{P_O}{P_O + P_{sat} + P_q + P_{sw} + P_D + P_L}$$

The three terms concerning the device power losses have already been discussed in the previous paragraph.
We examine now the last two terms concerning the external components losses.

PD – Losses due to the recirculation diode

These losses increase as V_i increase, as in this case the ON time of the diode is greater.

$$PD = VF \cdot I_O \cdot \frac{V_i - V_O}{V_i} = VF \cdot I_O \cdot \left(1 - \frac{V_O}{V_i}\right)$$

where VF is the forward voltage of the recirculation diode at current I_O.

Figure 9: Efficiency vs. Output Voltage

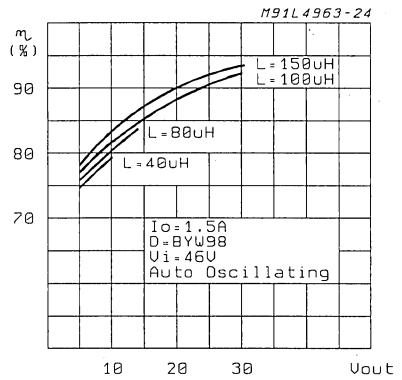
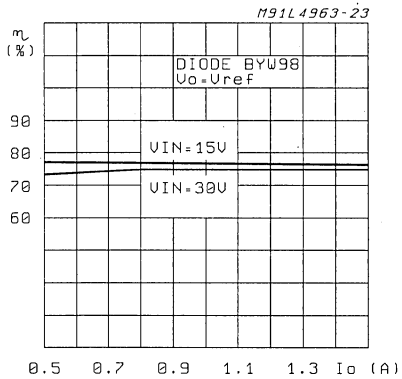


Figure 10: Efficiency vs. Output Current



PL – Losses due to the coil

Wecan divide these losses in two parts: core losses and copper losses.

The core losses for molypermalloy powder cores are given by the following formula.

$$W = 0.568 \cdot f^{1.23} \cdot B^{2.56}$$

where W = watt/lb

f = KHz

$$B = KGauss = \frac{(V_i - V_O) \cdot V_O \cdot 10^8}{N \cdot Ae \cdot f \cdot V_i}$$

N = number of turns

Ae = core cross section (cm^2)

copper losses:

$$P - \rho I^2_o \, MLT.N$$

N = number of turns

MLT = lenght/turn for 20% of winding factor

ρ = copper resistivity (1.72 10E-6Wcm)

Refer to table 1 for some ρ/Aw suggest values.

Table 1

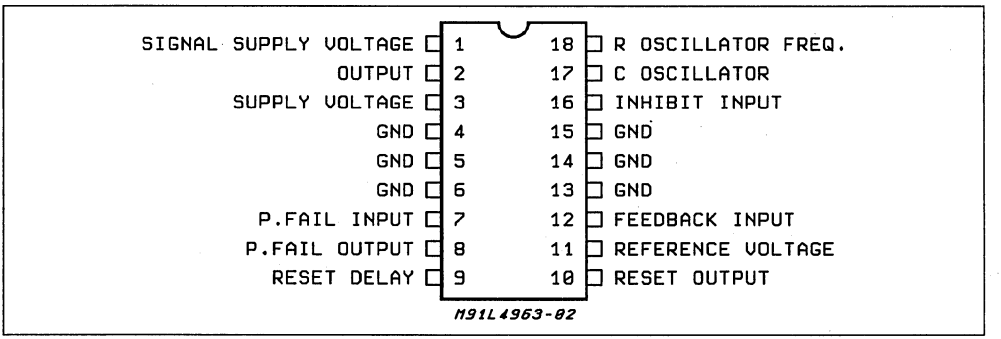
AWG	Diameter Copper (cm)	OHMS/CM 20C	OHMS/CM 100C
18	.102	.000209	.000280
19	.091	.000264	.000353
20	.081	.000333	.000445
21	.072	.000420	.000561
22	.064	.000530	.000708

Typical efficiencies obtained with the test and application circuit of fig. 20 are shown below.

DEVICE DESCRIPTION

Fig.11 shows the pin connection of the Powerdip 12+3+3 plastic package. The internal block diagram of the device is shown in fig.1. Each block will now be examined in detail.

Figure 11: Powerdip 12+3+3 Pin Connection



POWER SUPPLY

The device has two separate pins dedicated for the supply source. Pin.1 is for the Signal (Vcc) and Pin.3 for the Power (Vss) source; normally these two pins are connected together (see the typical application circuit Fig. 18). The L4963 is provided with an internal stabilized power supply that feeds the precise internal voltage reference 5.1V (±2%) and the internal analog blocks.

UNDER VOLTAGE LOCK OUT (UVLO)

The UVLO circuit ensures that Vcc is adequate to make the L4963 fully operational before enabling the output power stage. The UVLO turn-on and turn-off thresholds are internally fixed at 8.4V and 7.9V respectively.

This function acts also on the Power Fail and Reset Circuits; their output voltages pin.8 and pin.10 respectively, remain low state until the turn-on threshold is reached.

OSCILLATOR

The oscillator circuit behaves in a completely different way compared to the usual Step-Down regulator operating at fixed frequency and variable duty cycle. In fact, usually, the oscillator generates a fixed frequency sawtooth waveform that is compared with the Error Amplifier output voltage, generating the PWM signal to be sent to the power output stage.

In the L4963, the oscillator function is quite different. In the following we will describe briefly its operation referring to the simplified internal schematic shown in fig.12.

It is composed of a comparator (with inputs compatible to ground) with an hysteresis whose thresholds are 1V and 4.1V respectively.

The oscillator uses an external resistor RT on pin.18 to establish the charging and discharging current of the internal timing capacitor CT = 50pF, fixing in this way the maximum switching frequency:

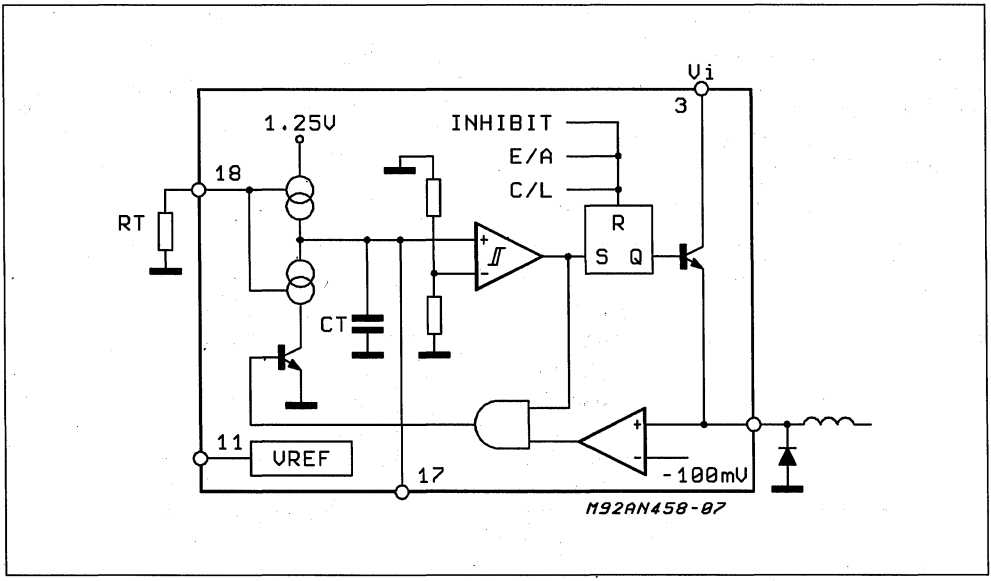
$$f_{osc}(KHz) = \frac{0.033}{Rt\ (K\Omega)}$$

It is also possible to increase the internal timing capacitor value, connecting an external capacitor between pin.17 and ground. The oscillator circuit, as we have seen in the "CIRCUIT OPERATION" paragraph, sends a set pulse to the latch that enables the power stage.

This set pulses train is at fixed frequency imposed by the external resistor when the device operates for low output currents (Dead time present in the inductor current I_L).

When we are operating in self-oscillating mode, the comparator that senses the free-wheeling status disables the oscillator pulses output until the inductor is fully discharged, varying in this way the switching frequency. It is also possible to disable the oscillator forcing the system to operate always in self-oscillating mode, connecting together the internal oscillator capacitor (pin.17) with the voltage reference pin.11.

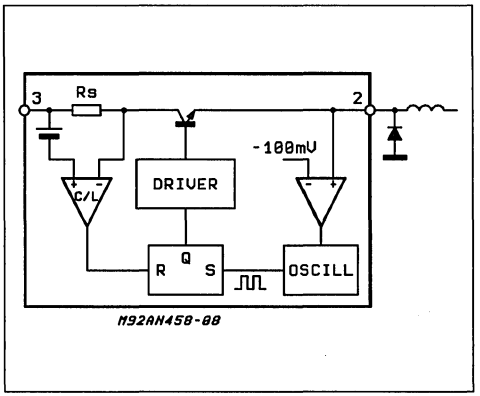
Figure 12: Oscillator Circuit



CURRENT LIMITATION

Output overload protection is provided by a current limiter circuit. The load current is sensed by an internal metal resistor (Rs) in series to the power transistor. When the voltage drop on the sense resistor, reaches the current comparator offset voltage, the current comparator generates a reset pulse for the latch, disabling the power stage.
Typical current limiting threshold is around 4.5A.
The power stage will be enabled again only when the energy stored in the inductor will be completely discharged, this due to the free-wheeling sense comparator (see Circuit operation paragraph for details).
The current limiting circuit operates also as soft-start during the device turn-on preventing over-currents on the load.
In fig.13 is shown the simplified internal schematic circuit of the current limiter.

Figure 13: Current Limiter



RESET

The reset circuit accomplishes a very important function when the L4963 is used in applications where it feeds microprocessors and logic devices. The function block diagram is shown in Fig.14. The Reset circuit monitors the output voltage and generates a logic signal when the output voltage is within the limits required to supply correctly the microprocessor.
This function is realized through three pins:

- Feedback input (pin.12)
- Reset delay (pin.9)
- Reset output (pin.10)

When the monitored voltage on pin.12 is lower than 5V, the comparator (A) output is high and the reset delay capacitor is not charged because the transistor Q1 is saturated, also the transistor Q2 is saturated, mantaining the voltage on pin.10 at low level.
When the voltage on pin 12 exceeds 5V, the transistor Q1 switches off and the delay capacitor (Cd) starts to charge through an internal current generator of about 110µA. When the voltage on pin 9 reaches 4.5V, the output of the comparator (B) switches low and pin 10 goes high.
As the output is an open collector transistor (Q2), a pull-up external resistor is required.

On the contrary, when the Reset input voltage goes below 5V, with an hysteresis of 100mV, the comparator (A) triggers again and sets istantaneously the voltage on pin 10 low, therefore forcing to saturation the Q1 transistor, that starts the fast discharge of the delay capacitor.
As shown in the block diagram, the Reset output is low when the UVLO or The INHIBIT signals are present.
Inside the chip there is a digital filter that prevents the Reset circuit activation if V_{out} drops below the reset threshold for less than 2s.
In this way the Reset circuit neglects very fast drops in the output voltage.
In fig.15 and Fig.16 are shown respectively the Reset circuit Waveforms and a typical application.

Figure 14

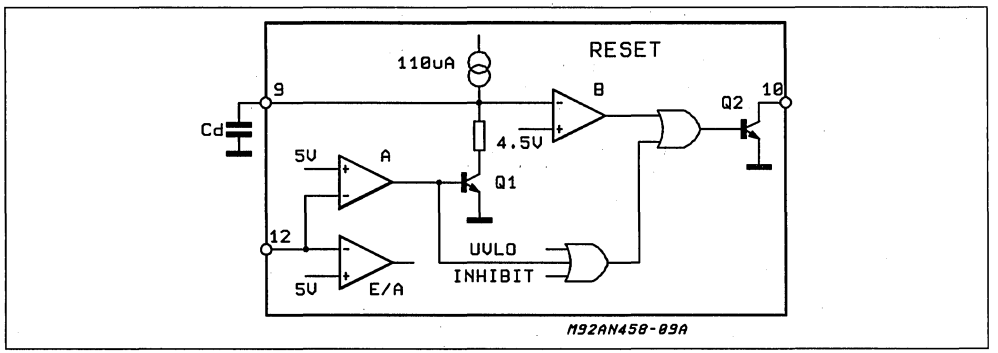


Figure 15

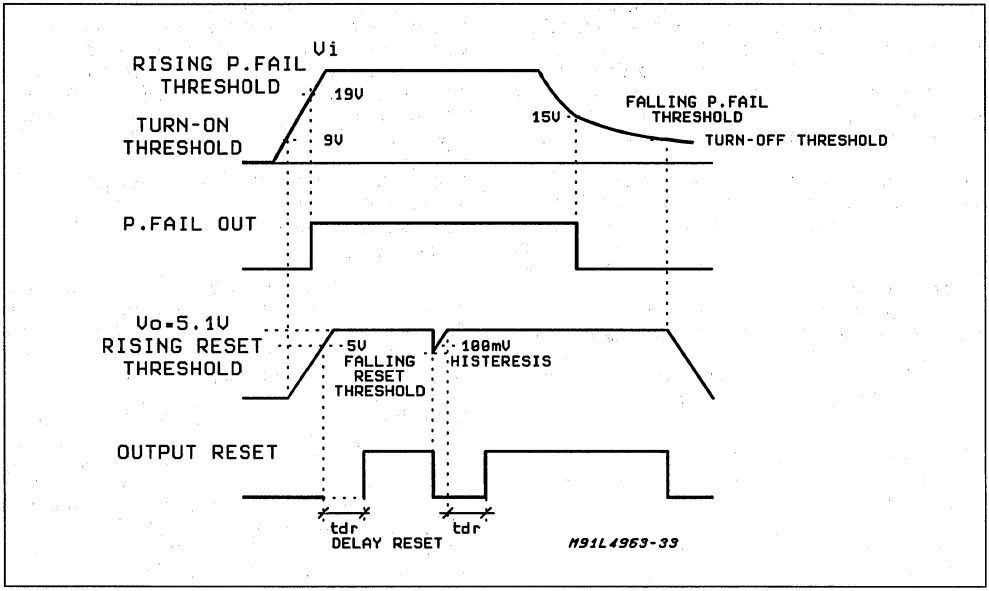
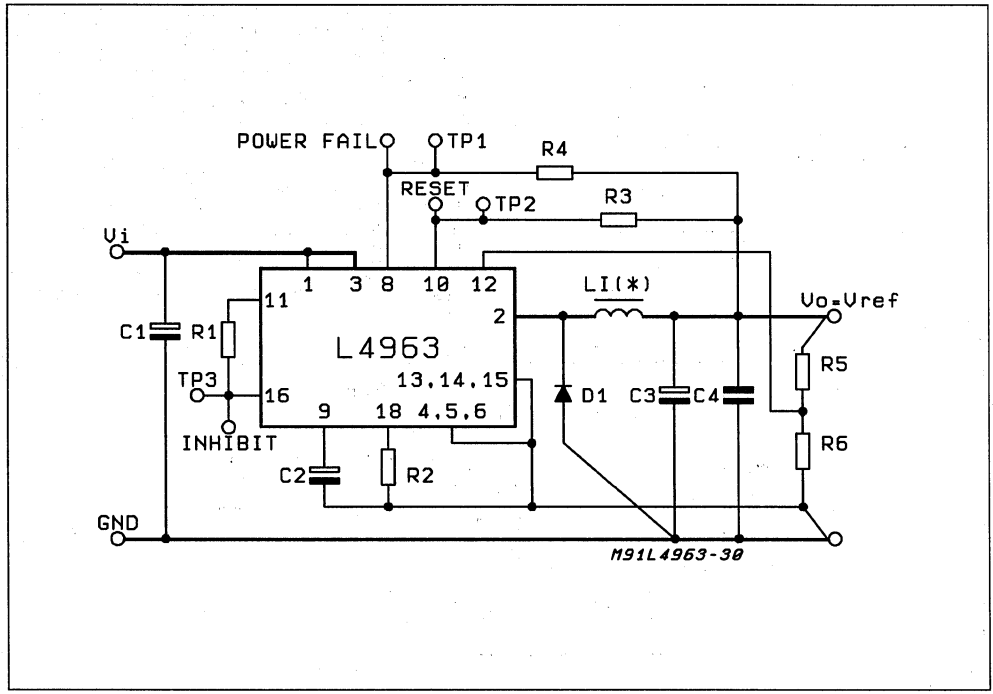


Figure 16



POWER FAIL

The Power-Fail circuit monitors the supply voltage (V_{SS}) via an internal voltage divider (R1=115KΩ, R2=35KΩ) as shown in Fig.17. When the supply voltage reaches the typical rising threshold voltage of 22V, set by the internal voltage divider, the Power Fail comparator output voltage goes low, turning off the output transistor Q1. This gives an high level on pin.8. As the power Fail output is an open collector transistor (Q1), an external pull-up resistor is required.

The Power Fail output goes low, giving an alarm signal, when the input voltage decreases reaching the internal typical Falling threshold voltage level of 18V. It is possible to change the rising and the falling threshold voltages, connecting a proper external voltage divider on pin.7.
In fig. 15 are shown the power fail waveforms.

INHIBIT

The INHIBIT function, available on pin.16, disables the regulator with a TTL logic signal. An high level at this pin (above 2.2V) switches off the power stage and forces low the output reset.
This useful feature, is normally used for supply sequencing and remote control ON-OFF.

THERMAL PROTECTION

The thermal protection function, operates when the junction temperature reaches 150°C; it acts directly on the power stage, turning it immediately off.
The thermal protection is provided with hysteresis and therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease of about 30°C below the intervention threshold.

APPLICATIONS

The L4963, thanks to the reduced external component count represents a very low cost effective solution in many applications.

In Fig.18 the complete typical application circuit is shown, where all the functions available on the device are being used.
In fig.19 is shown the same application circuit for reduced filter capacitor count and its PCB. As evident the PCB dimensions are reduced.
Below we will describe the design procedure to follow and some suggestion regarding the external components to use.

Figure 17

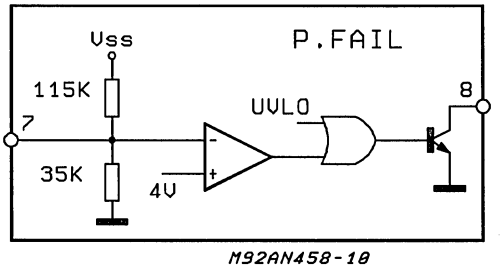
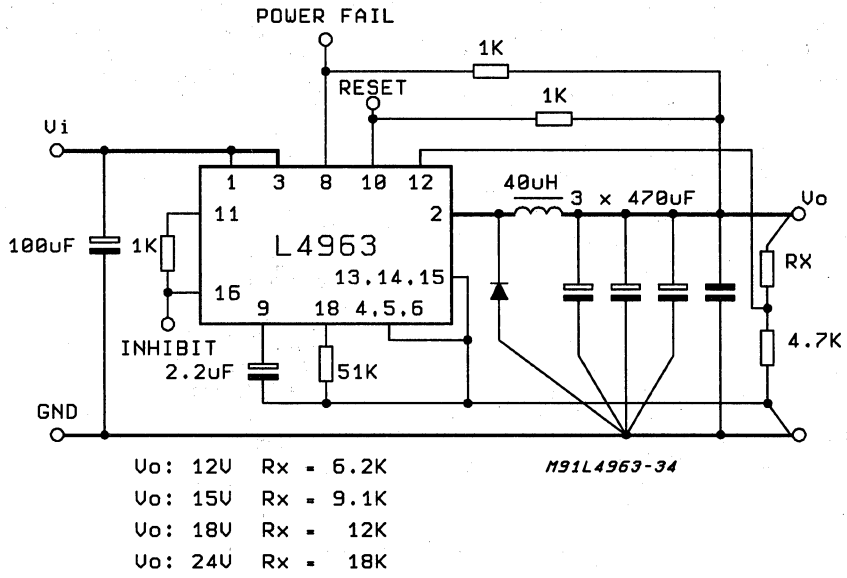


Figure 18: Test and Application Circuit



PART LIST

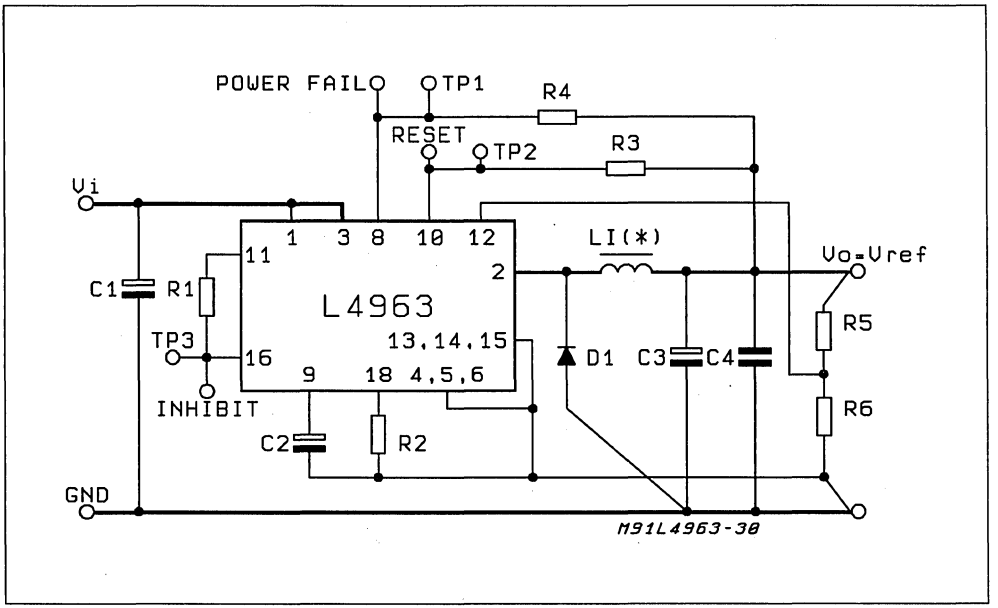
CAPACITOR	
C1	1000µF 50V EKR (*)
C2	2.2µF 16V
C3, C4, C5	4700µF 40V EKR
C4	1µF 50V film
RESISTOR	
R1	1KΩ
R2	51KΩ
R3	1KΩ
R4	1KΩ
R5, R6	see table

Resistor Values for Standard Output Voltages		
Vo	**R6**	**R5**
12	4.7KΩ	6.2KΩ
15	4.7KΩ	9.1KW
18	4.7KΩ	12KW
24	4.7KΩ	18KW

Diode: BYW98
Core: L = 40µH Magnetics 58121-A2MPP
34 Turns 0.9mm (20AWG)

(*) Minimum 100µF if V_i is a preregulated offline SMPS output or 1000µF if a 50Hz transformer plus rectifiers is used.

Figure 29: Typical Application Circuit



PART LIST

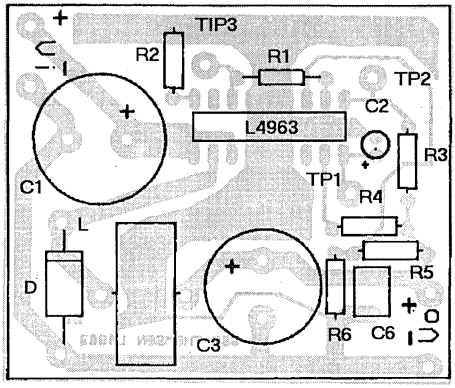
CAPACITOR	
C1	1000µF 50V EKR (*)
C2	2.2µF 16V
C3	4700µF 40V EKR
C4	1µF 50V film
RESISTOR	
R1	1KΩ
R2	51KΩ
R3	1KΩ
R4	1KΩ
R5, R6	see table

Resistor Values for Standard Output Voltages		
V_O	R6	R5
12	4.7KΩ	6.2KΩ
15	4.7KΩ	9.1KW
18	4.7KΩ	12KW
24	4.7KΩ	18KW

Diode: BYW98
Core: L = 40µH Magnetics 58121-A2MPP
34 Turns 0.9mm (20AWG)

(*) Minimum 100µF if V_i is a preregulated offline SMPS output or 1000µF if a 50Hz transformer plus rectifiers is used.

Figure 20: P.C. Board and Component Layout of the Circuit of fig. 21 (1:1 scale).



L4963 Step-Down Regulator Design Example

Referring to the complete typical application circuit shown in fig.19, and defined the following conditions:

- V_{out} = Regulated output voltage
- $V_{in(min)}$= Minimum input voltage
- $V_{in(max)}$ = Maximum input voltage
- $I_{out(max)}$ = Maximum load current
- f_{min} = Minimum switch freq. in self-oscillating mode.

We calculate the value of the external components.

1. OUTPUT VOLTAGE SETTING:

The output voltage is established by the voltage divider constituted by R5 and R6. To select the right R5 value use the following formula:

$$R5 = \frac{(V_{out} - V_{ref})}{V_{ref}} \cdot (R6)$$

where: V_{ref} = 5.1V
R6 = Is normally set at 4K7Ω

For a Quick calculation of some standard output voltages, the following table is useful:

Resistor Values for Standard Output Voltages		
Vo	**R6**	**R5**
12	4.7KΩ	6.2KW
15	4.7KΩ	9.1KΩ
18	4.7KΩ	12KΩ
24	4.7KΩ	18KΩ

To obtain V_{out} = V_{ref}, the pin.12 is directly connected to the output, therefore eliminating both R5 and R6.

2. INDUCTOR SELECTION:

The max. duty cycle is determined by the following formula:

$$D_{max} = \frac{V_{out} + V_F}{V_{in(min)} - V_{ce(sat)} + V_F}$$

Where: $V_{ce(sat)}$ = 1.5 V
V_F = Catch diode forward drop

The maximum inductor value is then calculated:

$$L\ max = \frac{(V_{in(min)} - V_{ce(sat)} - V_{out})}{2 \cdot I_{out(max)} \cdot f(min)} \cdot D\ max$$

where:
f(min) 20KHz to be out of the audible range.

In discontinuous mode operation, the inductor current may reach very high peaks ($I_{Peak} = 2I_{out}$), so it is important to verify that the coil will not saturate in overload or short circuit conditions damaging the output power stage due to the high dI/dt ratio.
Therefore, a correct dimensioning requires a saturation current above the maximum current limit threshold ($I_{2max\ -\ peak}$ = 6A).

3. Output Capacitor Selection:

The output voltage ripple depends on the current ripple in the inductor and on the performance of the output capacitor at the switching frequency .The minimum value of the output filter capacitor is obtained from:

$$C_{out(min)} = \frac{I_{out(max)}}{4 \cdot V_{ripple(p-p)} \cdot fmin}$$

where $V_{ripple(p-p)}$ is the amount of ripple voltage desired.

Clearly this formula doesn't take care of the capacitor Equivalent Series Resistance (ESR) value, that is the dominant factor to define the output ripple voltage at switching frequencies greater than 20KHz.

So we suggest to use also the following formula:

$$ESR(max) = \frac{V_{ripple(p-p)}}{2 \cdot I_{out(max)}}$$

Where the ESR(max) requirement is not satisfied by the capacitor value given by the first formula, use an higher value or, better, put in parallel several capacitors in order to reduce the total ESR.

The capacitors' voltage rating should be at least 1.25 times greater than the given output voltage.

The big advantage of this system is to greatly reduce number of external components compared to the continuous mode solution.

The only drawback is a higher ripple voltage on the output that can be up three times larger than in continuous mode.

A proper choice of low ESR filtering capacitors can solve this problem greatly reducing the output ripple.

4. CATCH DIODE SELECTION:

The catch diode must comply with several requirements and its choice requires special care.

The current rating must be at least 1.2 times greater respect the maximum load current, but this is not enough because in short circuit conditions, the maximum current limiter threshold is 6A to which correspond an average output current of I_{out} = Ipeak/2 = 3A. This is the current requirement to useto choose the right diode.

The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.

The diode recovery speed is not so important because the power stage is turned-on only when the inductor is fully discharged and the diode is definitely off. So there is not simultaneous conduction between them.

This allows a reduction of the disturbances with respect to the continuous mode, because they are mainly radiated during the transistor switch on, for the steep slopes during the simultaneous conduction of transistor and reverse conduction-diode.

LOW COST APPLICATION

If the remote inhibit, the reset and the power fail functions are not used we can reduce further the external component count.

It is possible in this case, to have a very efficient-switch mode power supply for very low cost applications.

Two examples of minimal component count regulators are shown in fig.21 and fig.22.

Figure 21: A Minimal 5.1 Fixed Regulator – Very Few Components are Required

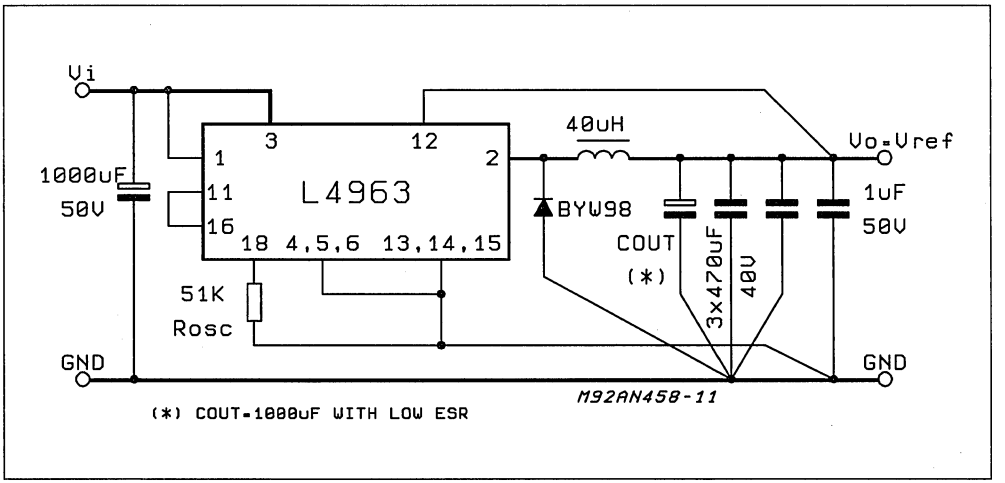
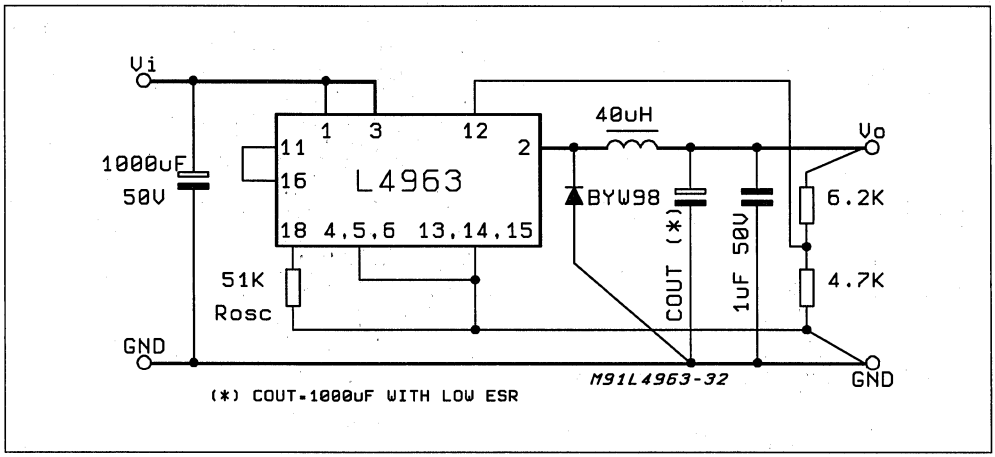


Figure 22: A Minimal Components count for V_O = 12V



DUAL OUTPUT POWER SUPPLY

The application shown in fig.23 is interesting because it provides two output voltages. The main voltage, is directly controlled by the feedback loop, the second voltage is obtained through an auxiliary winding. As the auxiliary voltage is obtained through a completely separated winding, it is possible to obtain either a positive or a negative voltage. Where isolation is not required between the two outputs, we can reduce the number of the auxiliary turns improving also the tolerance of the secondary output using the configuration illustrated in fig.24.

For both this configurations, the discontinuous mode is ideal because we have a good energy transfer between primary and secondary windinngs, due to the high energy stored in the coil that is function of the ripple current in the inductor.

Figure 23: Multioutput isolated.

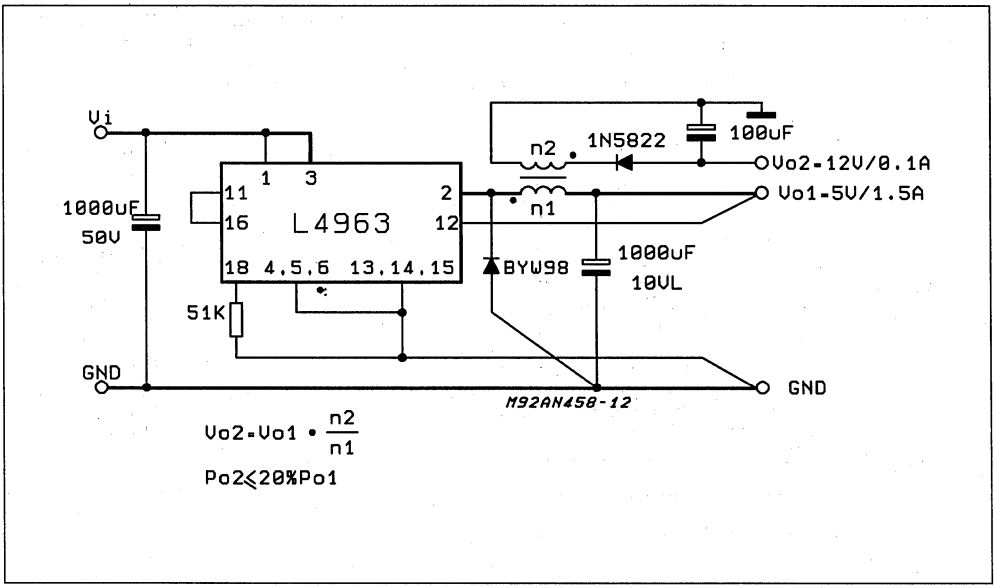
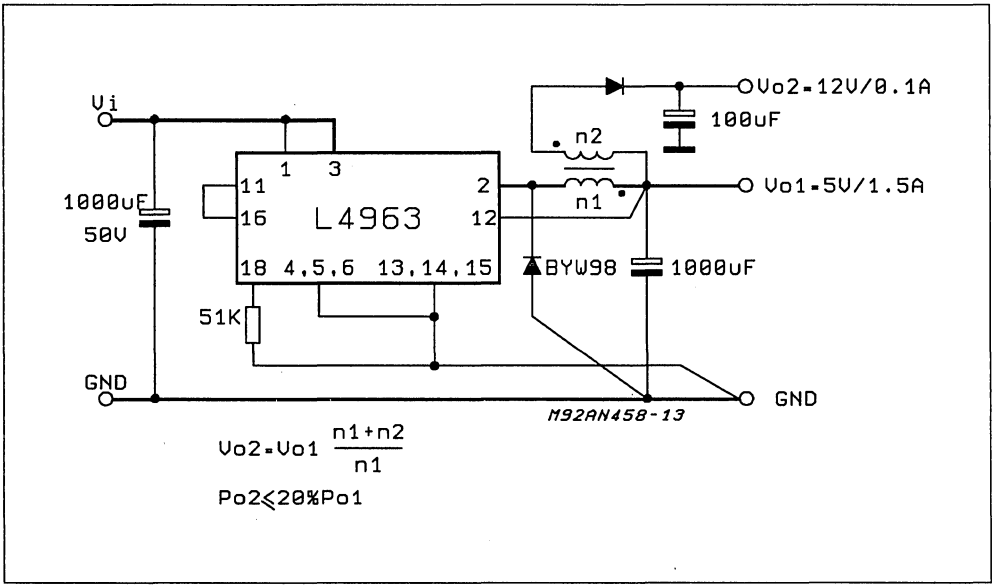


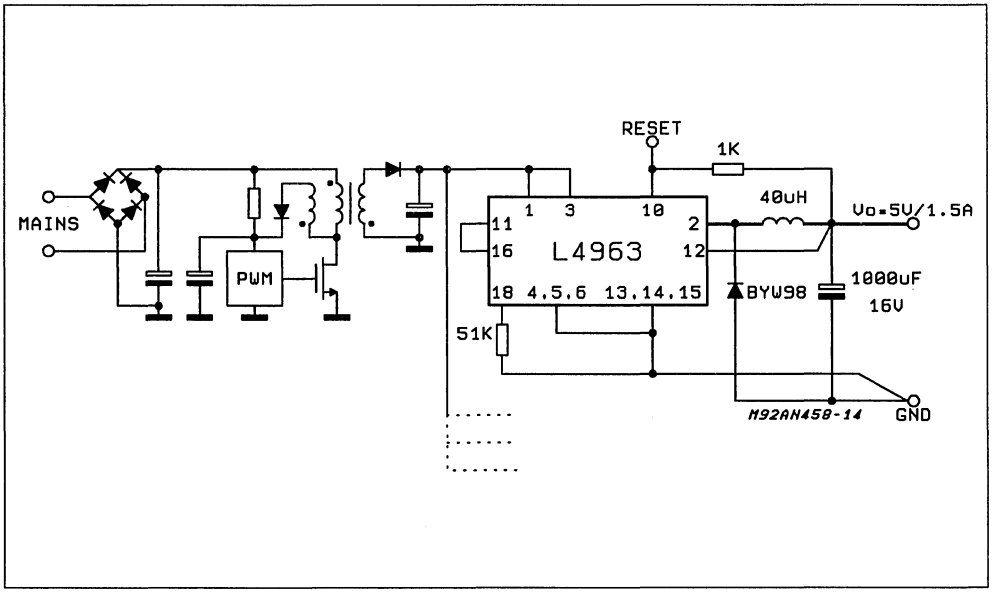
Figure 24: Multioutput not isolated.



L4963 IN OFF-LINE POWER SUPPLY

The L4963 can be useful as post regulator in off-line power supplies, where it can sobstitute the usual linear post regulation increasing the efficiency and reducing the complexity of the transformer, if the distributed power supply approach is used (see fig.25).

Figure 25: Typical off-line solution using L4963 as post regulator.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

INTRODUCTION TO A 10A MONOLITHIC SWITCHING REGULATOR IN MULTIPOWER-BCD TECHNOLOGY

by C.Diazzi

The L497X series of high current switching regulator ICs exploit Multipower-BCD technology to achieve very high output currents with low power dissipation – up to 10A in the Multiwatt power package and 3.5A in a DIP package .

Switched mode techniques led to the development of high efficiency circuits offering space saving and a reduction in costs, mainly of the heatsink and output LC filter. For these applications a new technology, called MULTIPOWER-BCD, has been developed which allows the integration on the same chip of isolated power DMOS elements, Bipolar transistors and CMOS logic.

The technology is particularly suitable for the problems rising in the switch mode field, due to the characteristics of high efficiency, fast switching speed, no secondary breakdown of the power DMOS element.

The great flexibility that we have at our disposal for the choice of the signal and driving sections components allows optimization and compactness of the system. With MULTIPOWER-BCD it has been possible to implement the family L497X, a new series of fully integrated switching regulators suitable for DC-DC converters working in Buck configuration. The complete family consists of five devices which differ each other only by the output current value (2A, 3.5A, 5A, 7A, 10A) they can deliver to the load. The devices rated at 2A and 3.5A are assembled in Power Dip (16+2+2), while the others are assembled in the Multiwatt15 package. Each device integrates a DMOS output power stage, a control section, limiting current and supervisor functions like Reset and Power Fail signal for microprocessors applications.

Output voltage can be adjusted starting from the internal reference voltage (5.1V) up to 40V, allowing a maximum output power of 80W for the 2A version and of 400W for the 10A version. Maximum operating supply voltage is 55V.

THE TECHNOLOGY

The technology architecture is based on the vertical DMOS silicon gate process that allows a channel length of 1.5 micron ; using a junction isolation technique it has been possible to mix on the same chip Bipolar and CMOS transistors along with the DMOS power components (Fig. 2). Figure 1 shows how this process brings a rapid increase in power IC complexity compared to conventional bipolar technology.

Figure 1: BCD process and increase in power ICs complexity.

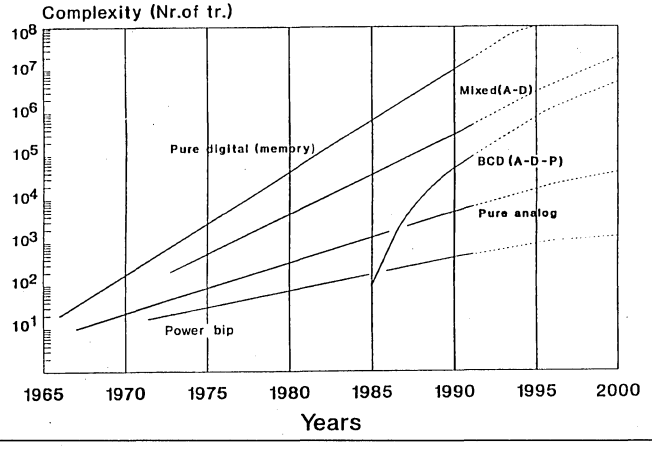
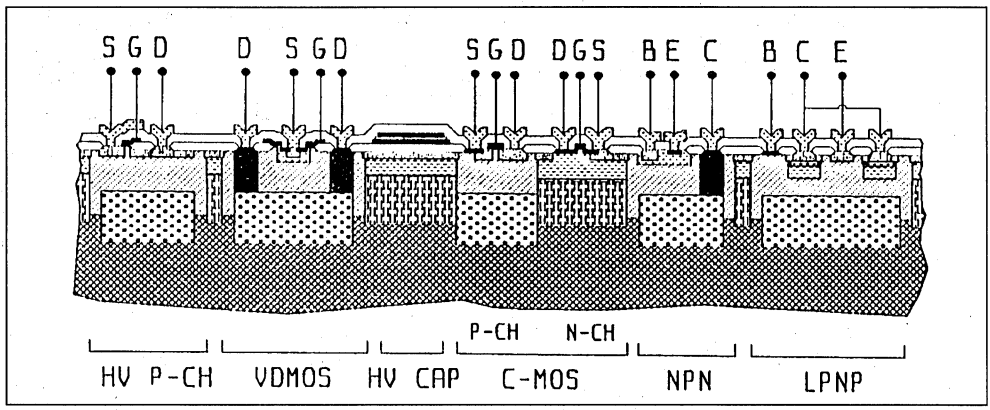


Figure 2: Cross section of the BCD mixed technology.



In the 70's class B circuits and DC circuits allowed output power in the range of 70W. By 1980 ,with the introduction of switching techniques in power ICs, output powers up to 200W were reached ; with BCD technology the output power increased up to 400W.

FUNCTIONS AND BLOCK DIAGRAM

The complete block diagram of the high power L4970A is shown in fig.3. Each block is analysed in the following.

POWER SUPPLY

The device is provided with an internal stabilized power supply (Vstart =12V), that provides the supply voltage to the analog and digital control blocks and also the supply voltage to the bootstrap section. The Vstart voltage supplies also the internal Reference Voltage section that provides accurate 5.1V voltage to the control loop. Through trimming techniques the 5.1V reference is within +- 2% limits.

OSCILLATOR and FEDFORWARD

The oscillator block (fig.4) generates the sawtooth

Figure 3: Block diagram of the 10A monolithic regulator L4970A.

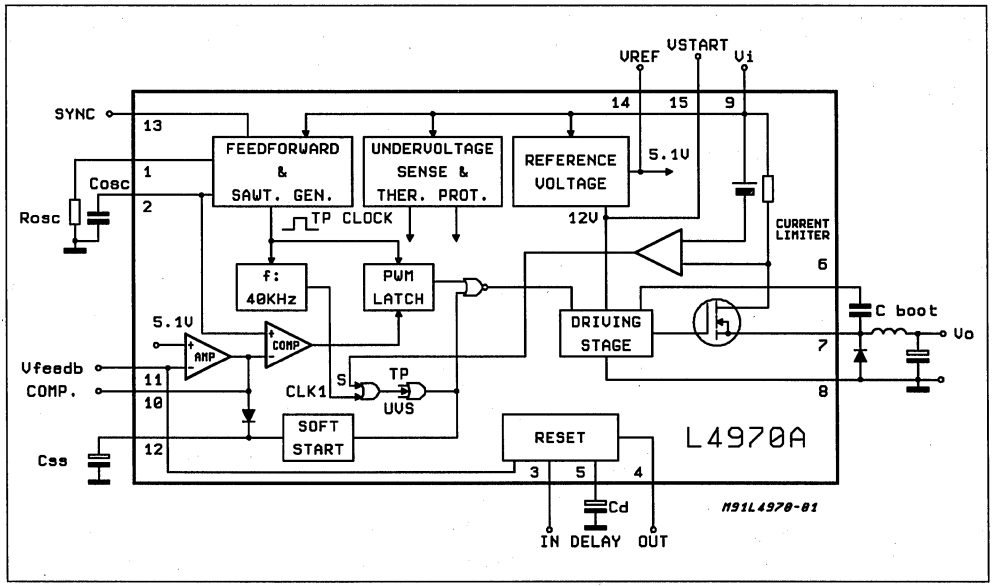


Figure 4: Oscillator circuit.

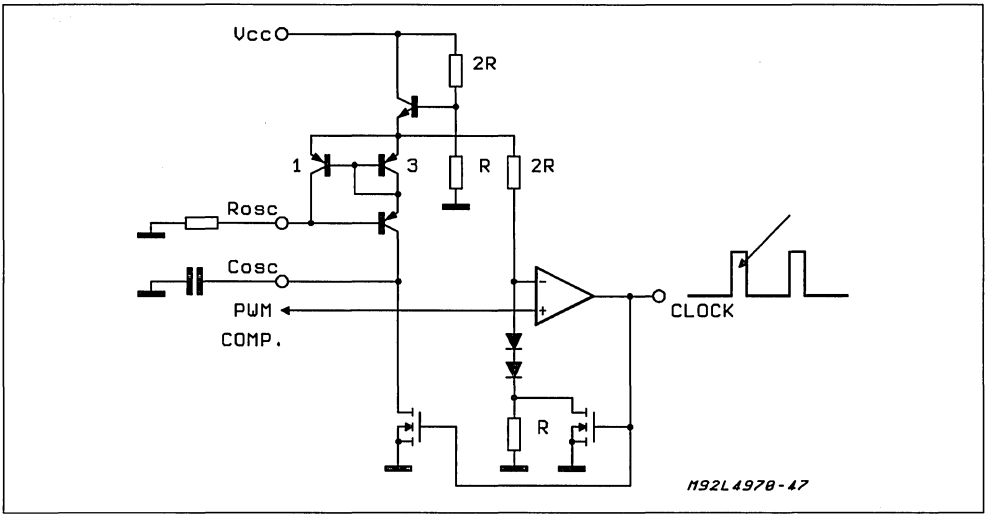
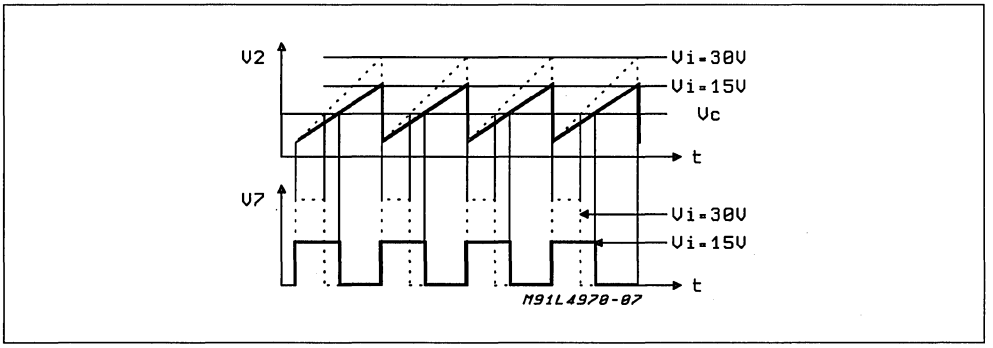


Figure 5: Voltage Feeforward waveform.



waveform that sets the switching frequency of the system. The signal, compared with the output voltage of the error amplifier, generates the PWM signal to be sent to the power output stage. The oscillator features a voltage feed-forward technique which is completely integrated and doesn't require any external component. Feed-forward function works in the supply voltage range 15-45V. The rate of increase of the sawtooth wavw-form is directly proportional to the input voltage Vcc. As Vcc increases, the output pulse-width (transistor on-time) decreases in such a manner as to provide a constant "volt-second' product to the inductance(fig.5).

From fig.5 it is shown that the duty cycle changes due to the ramp increase when Vcc increases. The error amplifier output doesn't have to change to keep the loop in regulation. This feature increases significantly the line regulation performance.

A resistor, between Rosc and GND , defines a current that is mirrored internally to charge the oscillator capacitor on the Cosc pin. The voltage at pin.Rosc is a function of Vcc value for the implementation of the feed-forward function (oscillator slope proportional to Vcc). A comparator is sensing the voltage across Cosc capacitor and discarge it when the ramp exceedes an upper threshold proportional to Vcc for the implementation of the feed-forward function. The Cosc discharge current is internally controlled at a value of about 20 mA. The lower threshold of the comparator is about 1.3V (2VBE). Here are reported basic equations for the oscillator:

$$I_{CHARGE} = \frac{V_{CC} - 9V_{BE}}{R_{osc.}} \text{ for } 15V \leq V_{CC} \leq 45V \quad (1)$$

$$I_{DISCH} \cong 20mA \quad (2)$$

$$V_{TH.HIGH} = \frac{V_{CC} - 9V_{BE}}{9} + 2V_{BE} \text{ for } 15V \leq \leq V_{CC} \leq 45V \quad (3)$$

$$V_{TH.\,LOW} = 2V_{BE} \quad (4)$$

$$F_{SWITCH} \cong \frac{9}{R_{OSC.}\, C_{OSC.}} \quad (5)$$

Note that formula (5) does not take in account the discharge time of C_{osc}, that is not negletable working at high F_{SWITCH} (200 KHz), and that is dependent on C_{osc} value.

$$T_{DISCH.} = \frac{(V_{TH.HIGH} - V_{TH.LOW}) \cdot C_{osc.}}{20mA} \quad (6)$$

By which :

$$F_{SWITCH} = \frac{1}{\frac{R_{osc}\, C_{osc}}{9} + T_{DISCH}} \quad (7)$$

During the discharge time of Cosc a clock pulse is generated that is available on pin.SYNC and that can be used to synchronize max 3 devices of the same family. See also fig. 6 and fig. 7 for the switching frequency versus value of R4 (R_{osc}).

PWM

The comparison between oscillator sawtooth and error amplifier output generates the PWM signal that feeds the driving stages. A PWM latch structure is implemented to avoid multiple pulses that could be dangerous for the power stage. A maximum duty cycle limitation is implemented in the PWM stage. Such limitation is obtained by the synchronization pulse generated in the oscillator section during the Cosc discharge time. When the pulse is present the driver is inhibited. In this way even if the error amplifier output completely overcomes the oscillator sawtooth, the power stage can not work in DC conditions, but is switched off during the clock pulse allowing a maximum duty cycle tipically in the range 90 - 95 %

SOFT START

Soft start (see fig.8) is an essential function for correct start-up and to obtain a monotonically increasing output voltage, without overstressing the output power stage. Soft start operates at the start-up of the system and after the intervention of thermal protection. The function is realized through a capacitor connected to soft start pin, which is charged at constant current(about 100uA) up to a value of about 7V.

During the charging time , through PNP transistor Q1 the voltage at the output of the transconductance amplifier is forced to increase with the same rising speed of Css capacitor. As the capacitor is charged, the PWM signal begins to be generated as soon as the error amplifier output voltage crosses the ramp; the power stage starts to switch with steadily increasing duty cycle (fig.9).

The charge of the soft-start capacitor is started every time the system begins to work after an anomalous condition occurred (undervoltage and thermal protection). The Css discharge current is in the range of about 20mA.

Figure 6: Switching frequency vs. R_{osc} (L4970A/77A/75A).

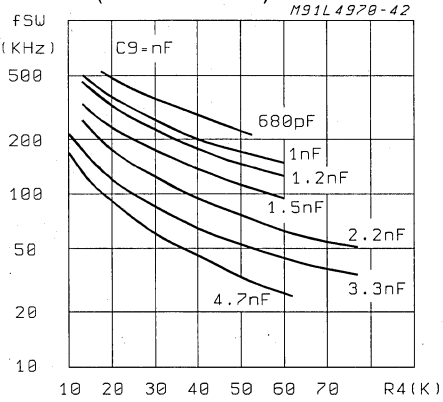


Figure 7: Switching frequency vs. R_{osc} (L4972A/74A).

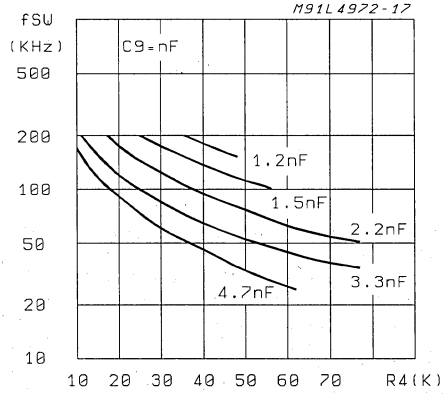


Figure 8: Soft start circuit.

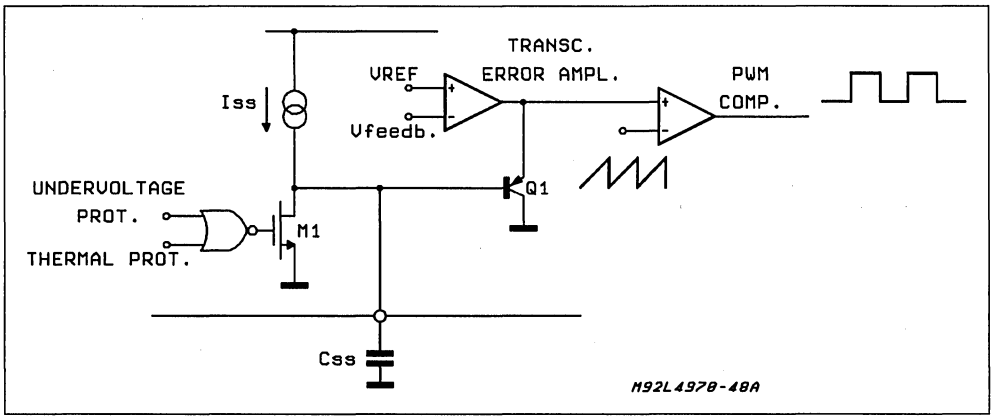


Figure 9: Soft start waveforms.

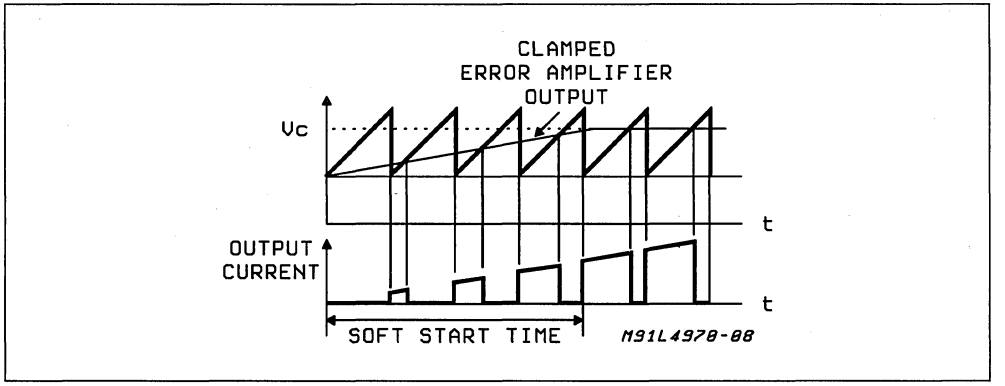
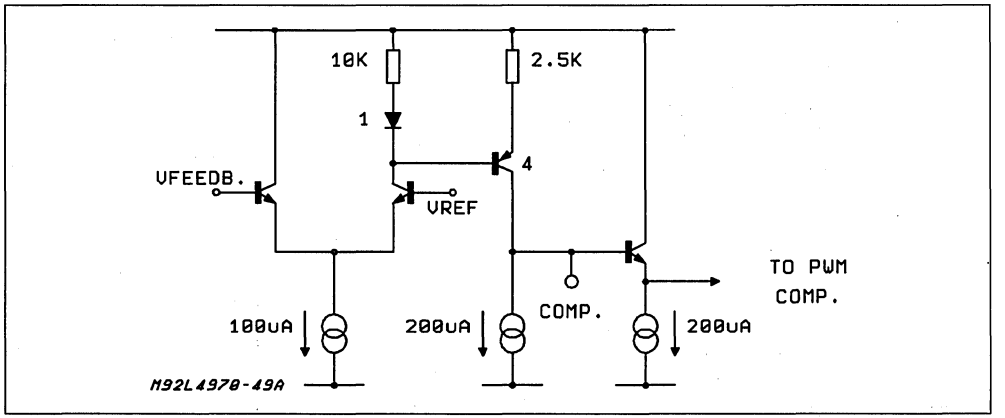


Figure 10: Error amplifier circuit.



UNDERVOLTAGE LOCKOUT

The chip features a complete built-in under voltage lock out protection, keeps the power output stage off up to the moment Vcc reaches 11v, with an hysteresis of 1V. After reaching the 11V value the system starts with the soft start feature.

ERROR AMPLIFIER

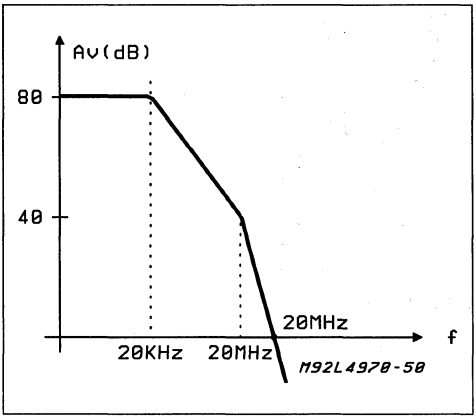
The error amplifier is a transconductance Operational Amplifier featuring a current output. The simplified schematic is represented in fig.10.

The basic characteristics of the uncompensated operational amplifier are the following:

- G_M = 4mA/V,
- R_o = 2.5Mohm,
- A_{Vo} =80dB,
- $I_{source/sink}$ = 200µA
- I_{Input} Bias Current = 0.3µA

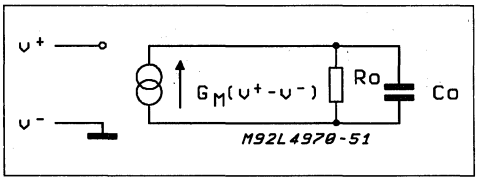
The frequency behavior of the uncompensated amplifier is reported in fig.11.

Figure 11: Open loop gain (error amplifier only).



Neglecting the high frequency behavior (in the hypotesis that in the overall frequency compensation of the loop the second pole of the operational amplifier is far below the 0 dB axis), we can make a first order approx. by which the error amplifier can be schematized by the equivalent circuit of fig.12.

Figure 12: Error amplifier equivalent circuit.



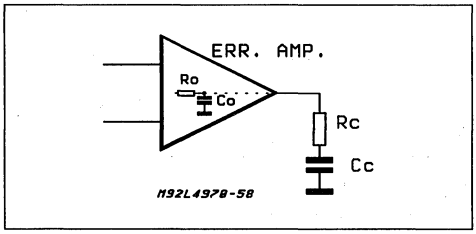
by which

$$A_v(s) = G_M \cdot \frac{R_o}{1 + SR_o C_o}$$

where C_o = 3pF.

The error amplifier is inserted in the regulation loop and can be easily compensated, thanks to its high output impedance, with a network between its output and ground. The typical compensated network is shown in fig.13.

Figure 13: Compensation network of the error amplifier.

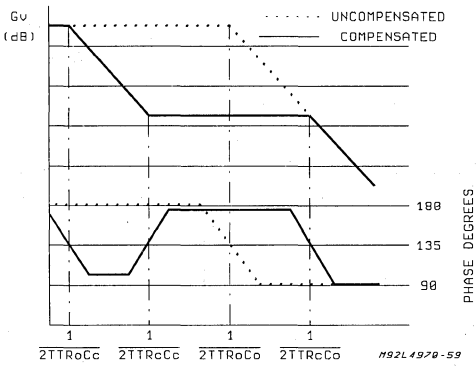


The transfer function is:

$$A_V(s) = G_M \cdot \frac{R_o (1 + S R_c C_c)}{S^2 R_o C_o R_c C_c + S (R_o C_c + R_o C_o + R_c C_c) + 1}$$

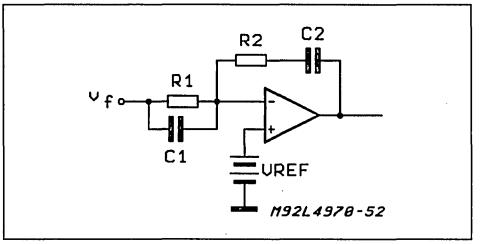
In the hypotesis that Rc<Ro and Cc>Co, the Bode diagram of the compensated amplifier is reported (see fig.14).

Figure 14: Bode plot showing gain and phase of compensated error amplifier.



The compensation network introduces a low frequency pole and a zero that usually is put at the frequency of the resonant pole of the output LC filter. The second high frequency pole is usually at a frequency of no interest. If needed , more sophisticated compensation circuits can be used by feedback with the opamp. An example is shown in fig.15.

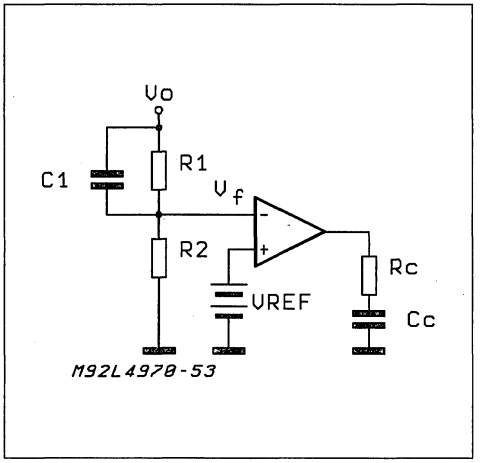
Figure 15: One pole, two zero compensation network.



Such a configuration introduces a low frequency pole and two zeros Z1 = 1/2ΠR1C1 and Z2 = 1/2ΠR2C2. Note that due to the high output impedance it is present also a second pole p2 = gm/2ΠC1. Usually it is better to use the highest possible value for R1, to have a low value for C1 in such a way to put p2 at the highest frequency. Limitations to R1 value are put by offset voltage due to opamp. input bias currents.

If a resistive divider is used at the output of the power supply, for voltages higher than 5.1V, it is possible to introduce a second zero with the network of fig.16.

Figure 16: Compensation network for output voltages higher than 51V.



Such a configuration introduce 2 zeros at:

$$Z_1 = \frac{1}{2\Pi\, R_c\, C_c}\ ;\quad Z_2 = \frac{1}{2\Pi\, R_1\, C_1}$$

and 2 poles at:

$$P_1 = \frac{1}{2\Pi\, R_o C_c}\ ;\quad P_2 = \frac{1}{2\Pi\, R_x\, C_1}\ ;\quad R_X = \frac{R_1\ R_2}{R_1 + R_2}$$

APPLICATION EXAMPLE

Consider the block diagram of fig.17, representing the internal control loop section, with the application values:
Fswitch = 200KHz, L = 100µH, C =1000µF, Po=50W, Vo =5.1V, Io =10A and Fo = 500Hz.

G_{loop} = PWM · Filter

Figure 17: Block diagram used in stability calculation.

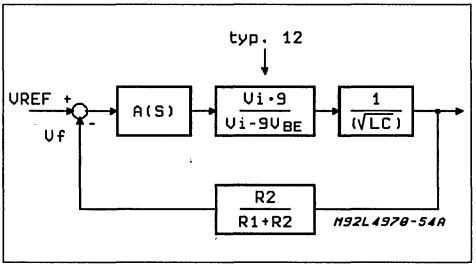
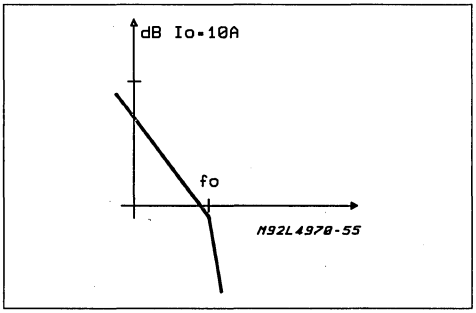


Figure 18: Frequency behavior of the circuit of fig 17.



The system requires that DC gain is maximum to achieve good accuracy and line rejection. Beyond this a bandwidth of some KHz is usually required for a good load transient response. The error amplifier transfer function must guarantee the above constraints. A compensation network that could be used is shown in fig.19.

$$A(s) = \frac{(1 + sR_1C_1)\ (1 + sR_2C_2)}{sR_1C_1\left(1 + s\frac{C_1}{G_M}\right)}$$

Figure 19: Compensation network.

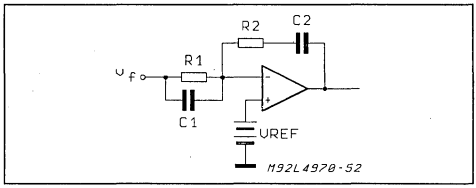
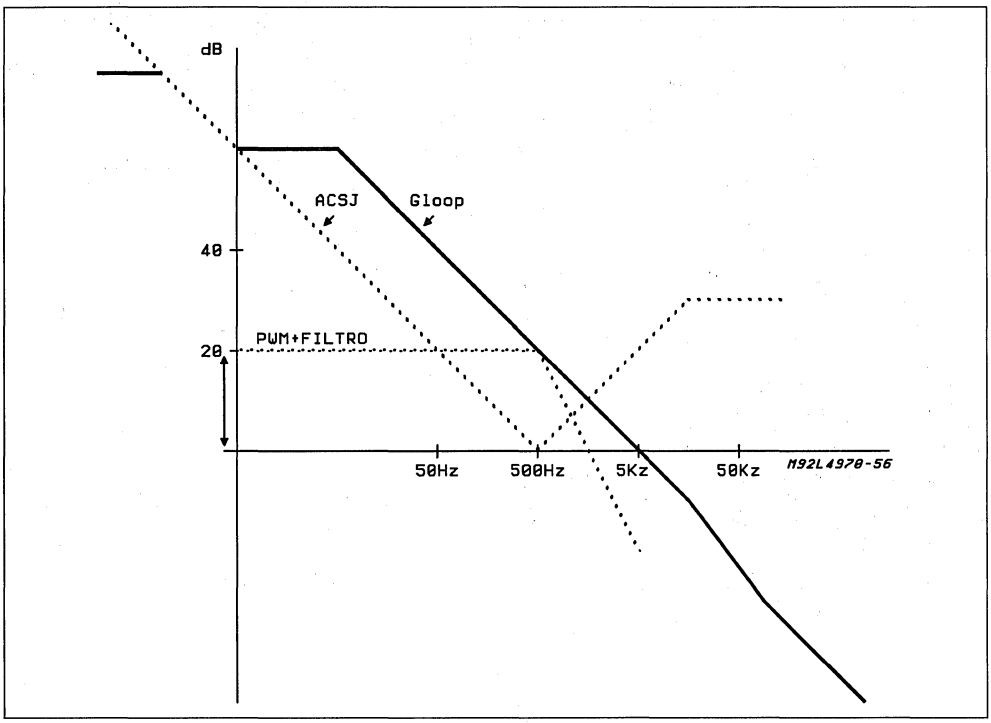


Figure 20: Bode plot of the regulation loop with the compensation network of fig. 19.



The criterium is to define Z1, Z2 close to the resonant pole of the output LC filter. The $Gm/2\Pi C_1$ pole must be placed at a frequency at which open loop gain is below 0 dB axis (Fig. 20).

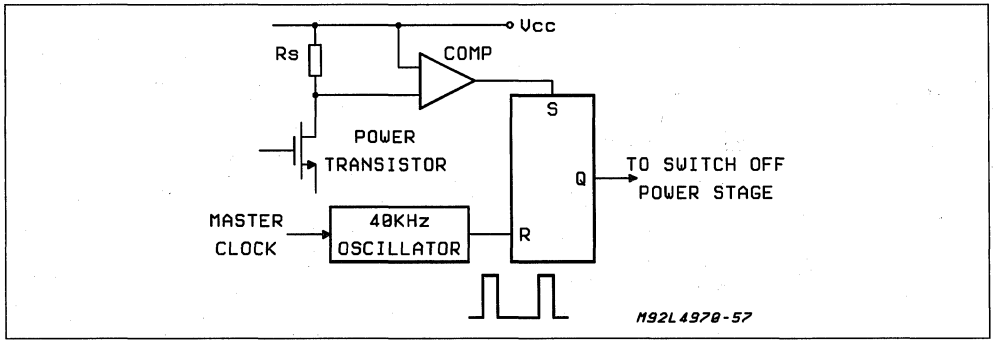
CURRENT LIMITATION

Current limitation is implemented intrnally to the chip and doesn't need any external component.

The output current is sensed by an internal resistor in series with the drain of the power transistor. On chip trimming guarantees ±10% accuracy on the value of peak current limitation.

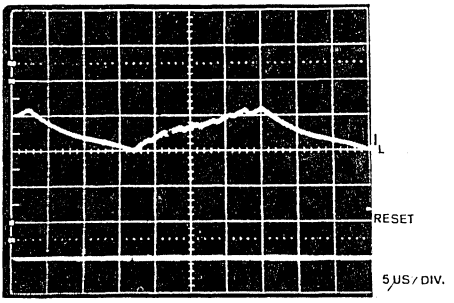
Current limit protection works pulse by pulse with lowering of tnhe switching frequency. Fig.21 shows circuital implementation of current protection.

Figure 21: Current protection circuit.



When the comparator senses an overcurrent, the flip-flop is set and an internal inhibit signal is generated. The flip-flop remains set until next reset clock pulse coming from the internal 40 KHz oscillator. After the reset pulse the regulation loop takes the control of the system and the output current begins to increase to the load value at the switching frequency of the master clock. If the overload condition is still present the protection cycle repeats. This mixed, pulse by pulse, lowering frequency current protection method, assures a constant current output when the system is in overload or short circuit and allows to implement a reliable current limitation even at high switching frequency (500 KHz) reducing the problems of signal delay through the protection stage. Fig.22 shows behavior of the inductance current when the system is in overload.

Figure 22: Overload inductance current.



The internal 40 KHz oscillator is synchronized with the master clock. When the system works with the master clock at a lower frequency of the internal clock, than the internal clock tracks the master frequency. This assures that the frequency does not increas during overload.

POWER FAIL-RESET CIRCUIT

The L4970A include a voltage sensing circuit that may be used to generate a power on power off reset signal for a microprocessor system. The circuit senses the input supply voltage and the output generated voltage and will generate the required reset signal only when both the sensed voltages have reached the required value for correct system operation. The Reset signal is generated after a delay time programmable by an external capacitor on the delay pin. Fig. 23 shows the circuit implementation of Reset circuit. The supply voltage is sensed on an external pin, for programmability of the threshold, by a first comparator. The second comparator has the reference threshold set at slightly less the ref. voltage for the regulation circuit and the other input connected internally at the feedback point on the error amplifier. This allows to sense the output regulated voltage. When both the supply voltage and the regulated voltage are in the correct range, transistor Q1 turns off and allows the current generator to charge the delay capacitor. When the capacitor voltage reaches 5V the output Reset signal is generated. A latch assures that if a spike is present on the sensed voltage the delay capacitor discharges completely before initialization of a new Reset cycle. The output gate assures immediate take of reset signal with-

Figure 23: Power fail and reset circuit.

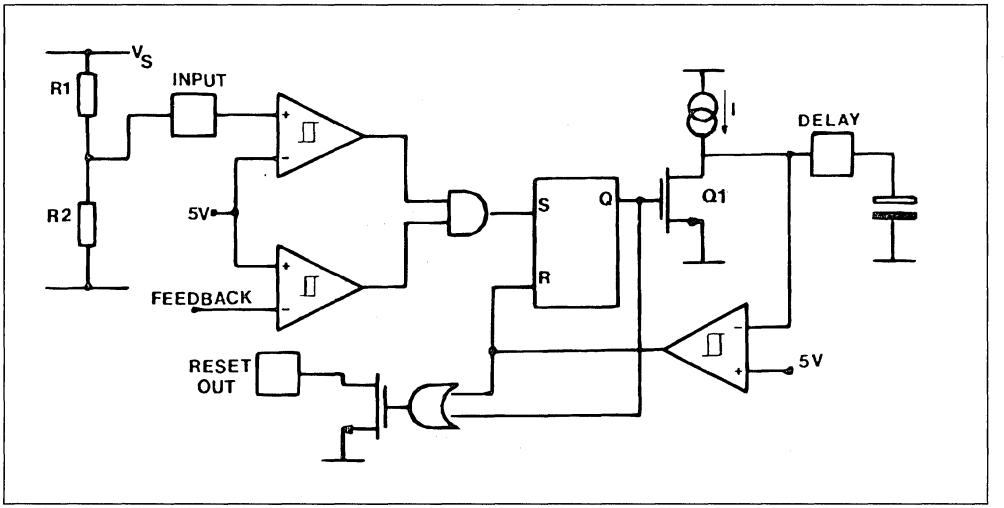
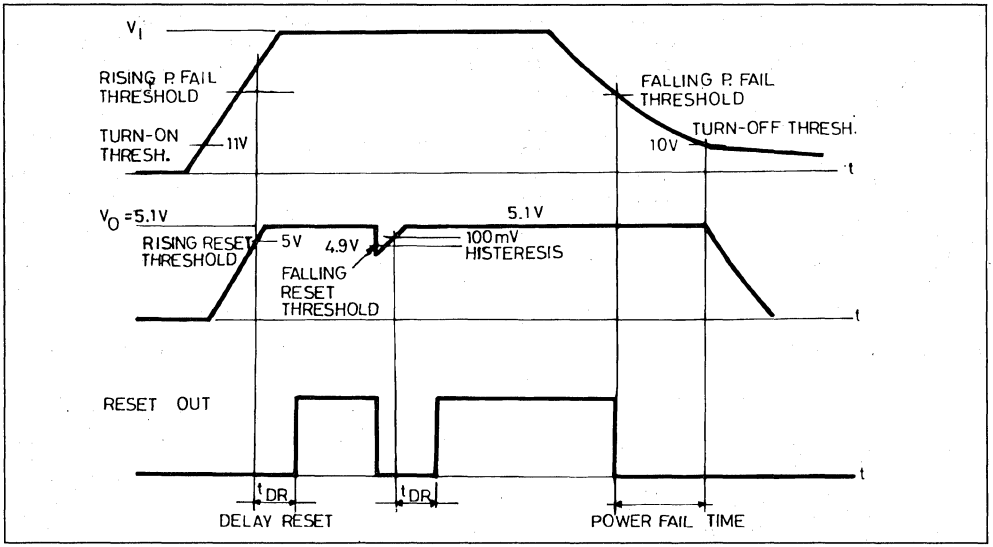


Figure 24: Reset and power fail waveforms.



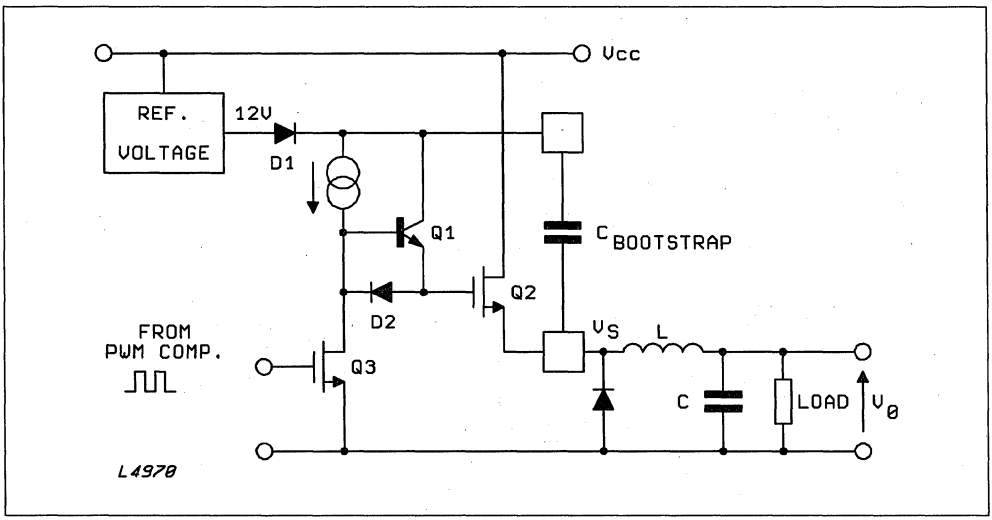
out waiting for complete discharge of delay capacitor. Reset output is an open collector transistor capable of sinking 20mA at 200mV voltage.Fig. 24 shows reset waveforms.

THE POWER STAGE

A simplified schematic of the output stage along with the external filter components is shown in fig.25.

Figure 25: Power stage circuit.

Power stage and associated driving circuits are among the most critical components to achieve good performances at high switching frequency. An external bootstrap capacitance, charged via diode D1 at 12V, is needed to provide the correct gate drive to the power DMOS N-channel transistor. The driving circuit is able to deliver a current peak of 0.5A, during turn on and turn off phases, to the gate of power DMOS transistor. The circuit-described shows commutation times of 50ns.



The five devices of L497X family differentiate each other only for the level of current protection, while the control part is the same and power device area is the same to guarantee low power dissipation also for low current versions in DIP package.

Table 1 and fig.26 shows electrical characteristics of the power DMOS implemented in the chip.

THERMAL PROTECTION

The thermal protection function operates when the junction temperature reaches 150°C; it acts directly on the power soft start capacitor, discharging it. The thermal protection is provided with hysteresis and therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease of about 30 degree C below the intervention threshold.

Figure 26: Gate-charge curve for the power DMOS.

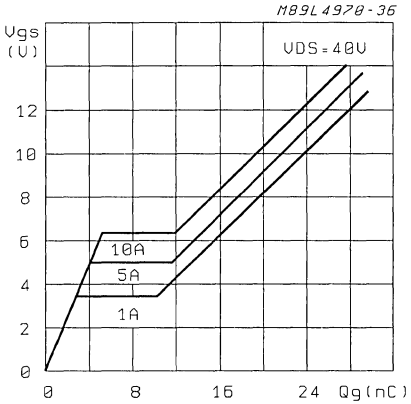


Table 1.

B_{VDSS} > 60V	at I_D = 1mA		V_{GS} = 0V
$R_{DS(ON)}$ = 100mΩ	at I_D = 10A	T_j = 25°C	V_{GS} = 10V
$R_{DS(ON)}$ = 150mΩ	at I_D = 10A	T_j = 150°C	V_{GS} = 10V
V_{TH} = 3V	at I_D = 1mA		

SIMPLIFIED SWITCH-MODE BASE DRIVE CIRCUIT WITH THE L4974 SMARTPOWER-IC

By Klaus RISCHMULLER

INTRODUCTION

Conventional driver circuits for bipolar-junction-transistors and Darlingtons have a high power dissipation. In order to reduce this dissipation, switch-mode driver stages have been proposed[1]. A new, very simplified driver stage, taking advantage of the switch-mode principle is presented here. It has been designed around smartpower-IC L4974. The efficiency of the IC is so high, that even with a 4 Amp base-current, the smartpower device is housed in a DIL-package ... !

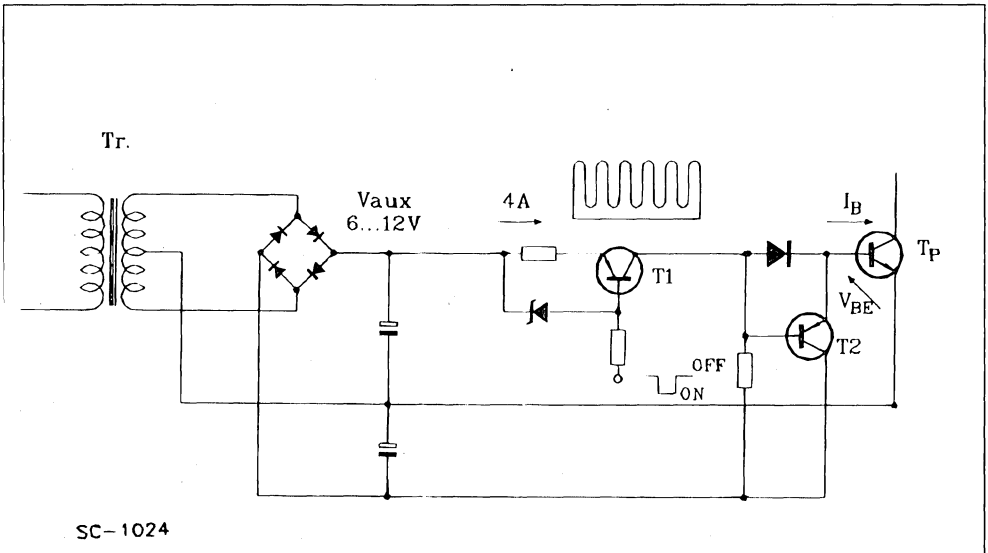
Bipolar-junction-transistors need negative bias in order to obtain fast turn-off switching and a good immunity against reverse conduction followed by dv/dt. This driver circuit generates the negative bias internally - it can be supplied from a single, unregulated source.

The new configuration can be used to simplify and improve existing converter/inverter circuits (less auxiliary supplies, less heatsinks and higher efficiency).

CONVENTIONAL BASE DRIVE V/S SWITCH-MODE BASE DRIVE

Conventional base driver circuits draw base current from an auxiliary supply voltage between 6 to 12 Volts. The base-current amplitude is limited by means of resistors or dissipative current sources. (figure 1) Such a base driver has a very low efficiency. The power transistors base-emitter voltage is about 1V, but 5V to

Figure 1 : Dissipative Driver Circuit.



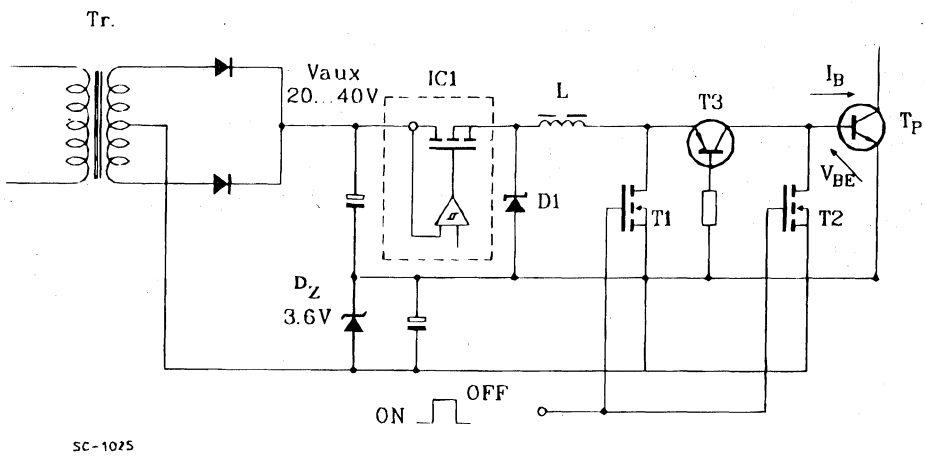
During permanent conduction with a 4A-base-current, the transformer Trs has to supply a power of 56W. About 90% of this power is dissipated in the driver circuit.

11V are dropped inside the driver circuit. Applying the switch-mode principle to base driver circuits, substantial energy savings can be made. Auxiliary power supply and heatsinking costs can be greatly reduced.

HOW IT WORKS

Figure 2 shows the principle of such a switch mode driver circuit. A smartpower-IC with a MOSFET output-stage operates as a buck regulator in current-mode. During the off-state of the power transistor, TP - figures 1-4., a MOSFET, T1, applies a short-circuit to the output of the buck regulator. Thus, the smartpower IC operates with reduced duty cycle and maintains a constant current in the choke L. In order to turn-on power transistor TP, the MOSFET T1 is turned off and the constant choke-current flows into the power transistors base. The rate of rise of base current is only limited by the MOSFET turn-off speed. In order to obtain very fast switching, high density MOSFETs (STVHD 90) with very low input capacitances have been used in the circuit[2].

Figure 2 : Simplified Switch Mode Driver Circuit.



With an input voltage of 20V and a base current of 4A, the transformer supplies about 10W to the driver circuit. No device in the driver circuit has to be cooled with a heatsink.

During the on-state, the driver circuit input current can be estimated using the term 2 * I_B * V_{BE}/V_{aux}, where I_B is the base current, V_{BE} the base-emitter voltage and V_{aux} the voltage of the auxiliary supply.

If the power transistor base current is 0.5A. and the auxiliary supply voltage 20 Volts, the driver input current will be about 0.5 Amps. If the auxiliary supply voltage is increased, the input current will be further reduced.

NEGATIVE BIAS OUT OF POSITIVE SUPPLY

The negative bias for fast turn-off switching can be generated by various means.

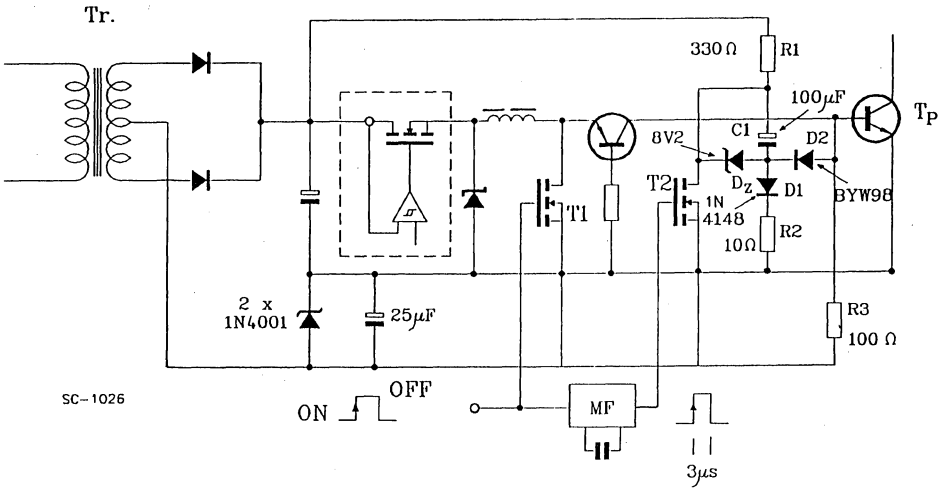
A zener diode can be connected in series between auxiliary supply and driver stage, D_Z (figure 2). The potential at the zener diode anode is negative compared to the emitter potential of the power transistor. The losses in the zener diode are low, due to the reduced input current of the switch-mode base drive.

For turn-off switching, T1 and T2 are turned on. T1 applies a short circuit to the buck regulator output, T2 applies the negative bias to the power-transistor base.

It is also possible to generate a negative bias directly from positive auxiliary supply :

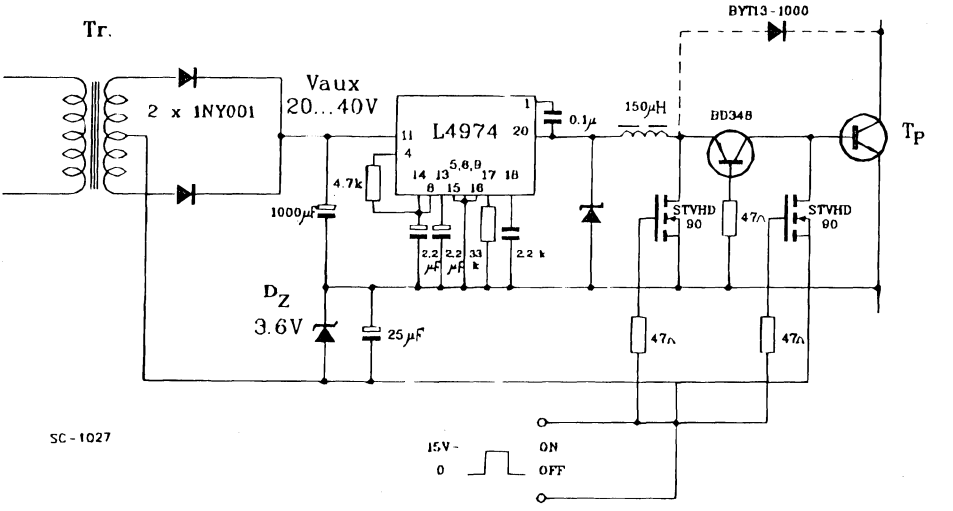
A capacitor C1 (figure 3) is permanently charged via a resistor R1 and a diode D1. At turn-off switching, T2 is turned on for a short time t1. This time has to be chosen to have a value slightly higher than power transistor's storage-times. T2 connects the positive electrode of C1 to ground during t1. Thus a negative voltage is applied to the base during turn-off switching off TP. T2 remains 'off' after turn-off and C1 continues to be charged. The advantage of this configuration is that the state of charge of C1 is independant of duty cycle - sufficient negative bias is always available[3].

Figure 3 : Modified Circuit with Dynamic Self-generation of the Negative Bias.



The capacitor C1 is charged during the conduction and the non-conduction time of TP. Its state of charge is independant of the duty-cycle !

Figure 4 : Complete Circuit Diagram for 4 Amp Base Current Supply.



The L4974 is housed in a Dual-in-line package – the PCB is sufficient for cooling. For higher base current, L4974 can be replaced by L4970.

RESULTS

With a BUF 420 (a cellular ETD-transistor) in the power stage, storage-times less than 1µs and fall-times lower than 25ns have been obtained when switching 20A, from a 400V supply.

The overshoot of the base-emitter voltage and the influence of parasitic inductances in series with the base are negligible due to the fact that the driver acts, at turn-on, as a nearly ideal current source. A turn-on speed dI_C/dt for the power transistor as high as 200A/µs has been obtained without any special design effort.

CONCLUSION

The application of the switch-mode principle to driver stages gives significant loss reduction and a very much reduced cost for auxiliary supply and heatsinking. In the past switch-mode driver circuits were considered as too complex. New smartpower-IC's allow a reduction in complexity and take advantage of the high efficiency achievable using a switch mode circuit. The 4A-version of the driver uses a Dual-in-line IC and no heatsinks. The combination of switch-mode principle with self generation of negative bias further reduces cost of the driver and its auxiliary supply. The concept shown appears to be valid for base currents up to 20 Amps ; its use for gate drive for SCR and GTO could also be investigated.

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2. Databook : POWER MOS DEVICES page 621 to 625 (STVHD 90), SGS-THOMSON Microelectronics

3. K. Rischmüller : Fast switching with power transistors and Darlingtons - state of the art, Application note, SGS-THOMSON Microelectronics

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ULTRA FAST NiCd BATTERY CHARGING USING ST6210 MICROCONTROLLER

L. Wuidart, P. Richter

INTRODUCTION

Today many cordless and portable equipments are supplied by a Nickel-Cadmium (NiCd) battery. The ultra fast charging of these batteries in less than half an hour is a very attractive service for users. Such a short charging time requires an "Ultra Fast" battery, a supply with a relatively high output power, and a charge control circuit more complex than for standard chargers. Moreover, automatic battery voltage identification is an appreciable feature.

The power converter proposed in this note is able to fully charge a common NiCd battery pack of 1.2Ah/7.2V within 15 minutes. The power converter has thus a corresponding output power capability of roughly 80W. The converter operates as a current source providing a constant 7A current to the battery while charging.

The battery charge is controlled by an economical microcontroller, the ST6210, a member of the ST6 microcontroller family. The programmed control provided by the ST6210 allows the charging of NiCd battery packs from 2 to 6 cells (2.4V to 7.2V). The supply to the microcontroller is simply generated from an auxiliary winding of the power transformer.

THE POWER CONVERTER

The asymmetrical half-bridge is today considered as one of the most attractive topologies for the primary side of a 220Vac off-line Switch Mode Power Supply (SMPS, see Figure 1). Adding the SGS-THOMSON AVS10 kit allows the automatic sensing and adaption to input voltages in the range of 90 to 240Vac.

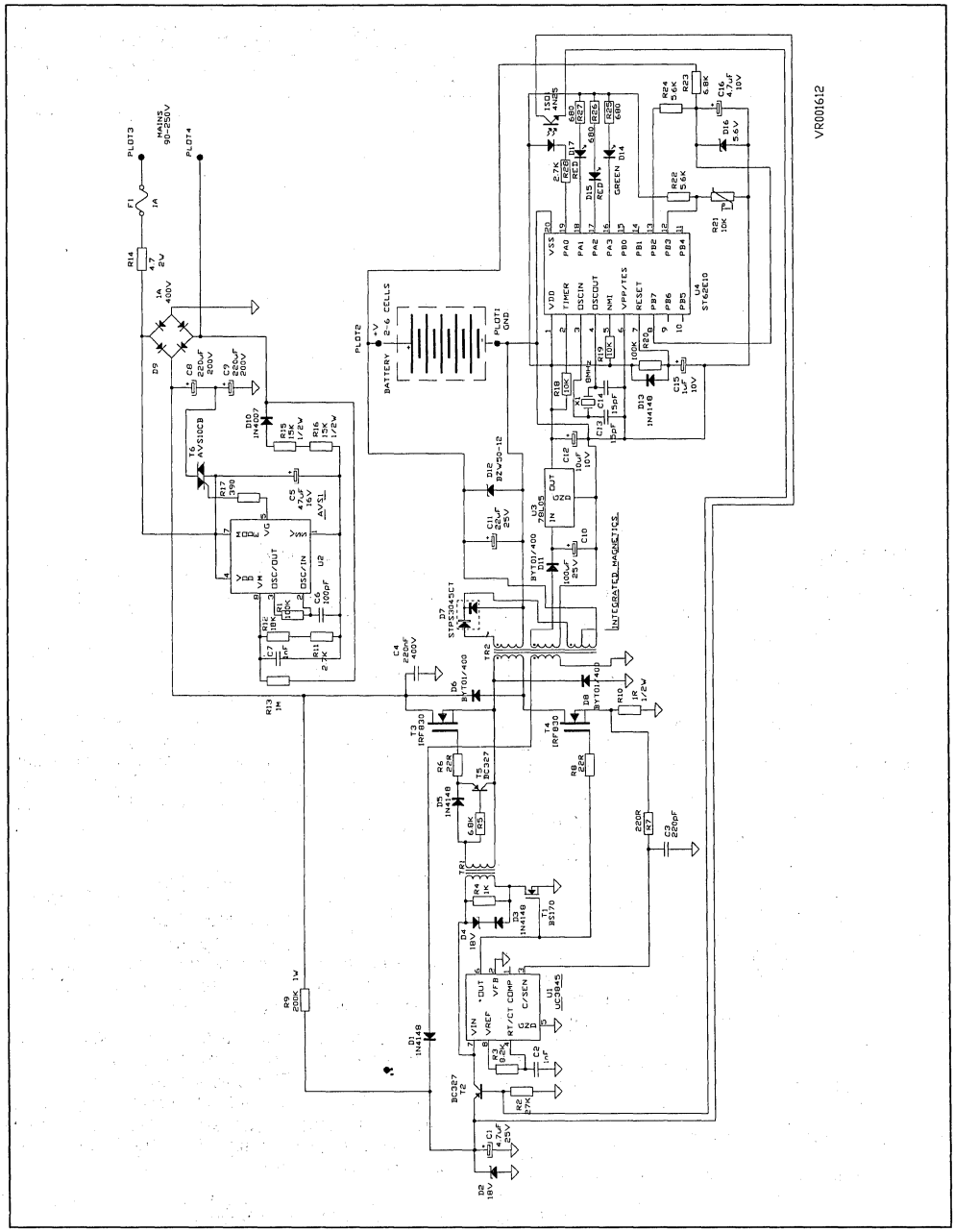
Contrary to single switch structures, the leakage inductance of the power transformer is much less critical. The two demagnetization diodes (BYT01/400) provide a simple non-dissipative way to systematically clamp the voltage across the switches to the input DC voltage Vin. This allows the use of standard 500V power MOSFET devices, such as the IRF830FI (in isolated ISOWATT 220 package), simply driven by a small pulse transformer.

The power converter is totally controlled from the primary side with a standard Pulse Width Modulation (PWM) control IC, the UC3845 regulating in current mode. A single optocoupler makes this SMPS operate as a battery charger. The SMPS is turned on or off from the secondary by the ST6210 microcontroller via this optocoupler.

The switching frequency is fixed at 100kHz in order to keep the magnetic part to a reasonable manufacturing cost level. The power transformer and the output inductor can be integrated on a single ferrite core [4]. This integrated magnetic technique can be optimised to allow a significant shrinking of the power converter size.

For more information on the power converter, refer to reference [4] of the bibliography.

Figure 1. Ultra Fast NiCd battery charger schematic



BATTERY CHARGE CONTROL

Ultra Fast Charge Control Method

For Ultra fast charge systems - under half an hour - the majority of battery manufacturers recommend the negative delta voltage method (-ΔV) otherwise called the negative slope cut-off circuit [2] [3].

When a NiCd battery reaches full charge, its voltage decreases slightly (Figure 2). The negative delta voltage method (-ΔV) consists of stopping the charge as soon as the voltage characteristic slope becomes negative. This technique allows the very rapid charge of a NiCd battery, near to its full capacity. Moreover, no compensation for the age of the battery is required because only relative voltages are measured.

In this application, the battery voltage is sensed by a ST6210 microcontroller housed in 20 pin dual in line package. The integrated Analog to Digital converter (ADC) of this micro-controller is able to detect a typical voltage drop of -10mV/cell.

MONITORING FUNCTIONS

The battery charge is totally monitored by the HCMOS ST6210 in PDIP or PSO 20 pin package, the ST6210. By using this micro-controller, additional monitoring functions can be easily added to the Ultra fast charge control program.

Stand-by current charge: Burst mode

Once the negative voltage drop has been detected by the ST6210, the ultra-fast charging is stopped and the power converter supplies the battery with a stand-by current around 170mA. This stand-by charge is provided by burst mode current control. The converter is successively turned on and off at 25Hz with a small duty cycle of 0.025. The ST6210 manages this burst mode from the secondary side via an optocoupler to the auxiliary supply of the PWM control IC (UC3845).

A small 100µF reservoir capacitor is sufficient to keep the ST6210 correctly supplied during the off periods (39ms) of the burst mode. This is possible due to the low current consumption in run mode of the ST6210 HCMOS micro-controller (typically 3mA with an 8MHz oscillator, reducing to typically 1mA for a 2MHz oscillator).

Battery temperature protection

Temperature protection is simply realized by using an NTC resistor placed on the battery pack. This NTC resistor is directly connected to another input of the ADC of the ST6210. When the battery temperature reaches 40°C during an Ultra Fast charge phase, the converter is switched into burst mode to protect the battery.

Battery presence

The ST6210 program detects whether the battery pack is connected or not. When the battery is not connected, the converter is turned into burst mode. The resulting stand-by current (170mA) flows into the output Transil diode (BZW 50-12).

CHARGE CONTROL PROGRAM DESCRIPTION

Figure 3 shows the main flow chart of the program for the complete charge control. The overall system is reset after each new mains connection.

Battery voltage measurement:

The battery voltage is directly measured by the ST6210 Analog to Digital Converter through a resistor divider chain. The technique used allows the ST6210 to automatically adapt to the battery type and voltage (from 2 to 6 cells, 2.4V to 7.2V).

Figure 2. One NiCd Cell Charge Characteristic

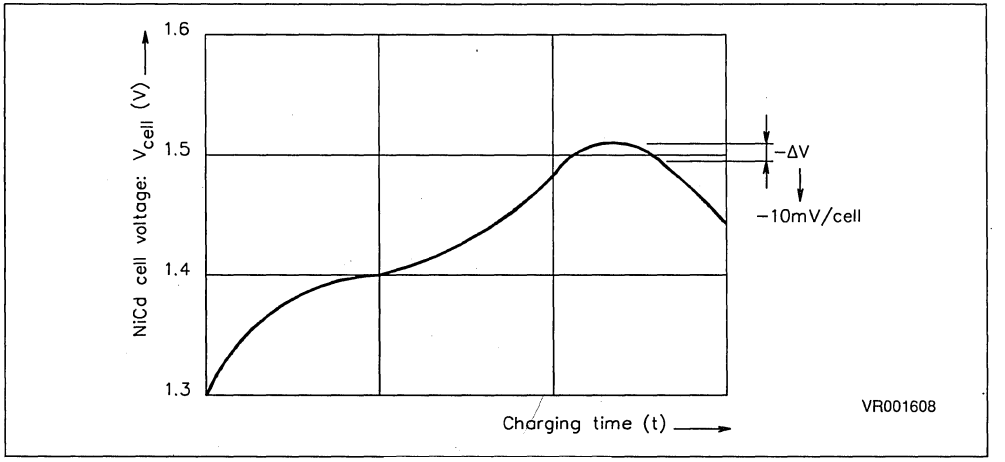
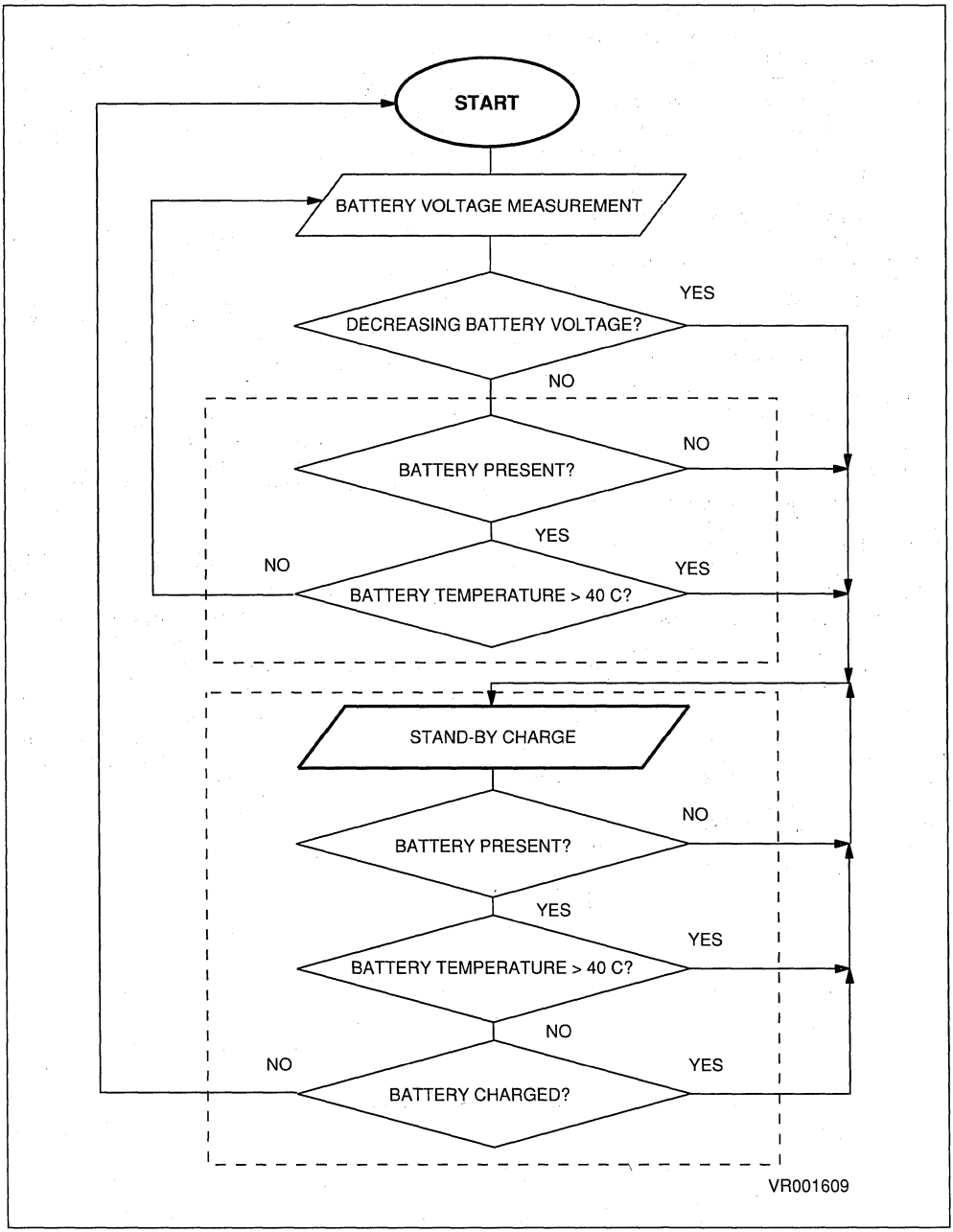


Figure 3. Main flow chart of the Ultra Fast Charge control program



Monitoring principle

The ST6210 averages a series of 256 battery voltage measurements (Σ Mn). The 256 conversions are made in a time frame of around 19 ms, with an inter-frame delay time of 0.5s (in this example). An average AVr of the last 8 averaged values is made according to the formula:

$$AVr = \sum \frac{\sum Mn \ldots \sum Mn-8}{8}$$

This AVr value is compared to the previous average AVr-1 and the highest value is stored. This rolling average value follows the battery voltage curve. Once the AVr value begins to decrease, indicating the battery is fully charged, the ST6210 stops the Ultra Fast charging.

The response time to detect the battery voltage drop ranges from 0.5 to 4 seconds, depending on the slope of the battery voltage curve at the charge completion. A longer delay time is able to increase the noise immunity, but at the cost of an extended response time.

PRACTICAL RESULTS

Tests made with different battery packs confirm that the battery charge is efficiently controlled by the ST6210 using its internal A/D converter. Results on the battery voltage and temperature pack versus charging time are shown in Fig. 5.

These recordings have been made with a common 1.2Ah/7.2V NiCd battery pack for cordless drills. The temperature of the battery pack does not exceed 33°C for an ambient temperature of 26°C.

Figure 4: Sequencing principle of the Battery Voltage measurement

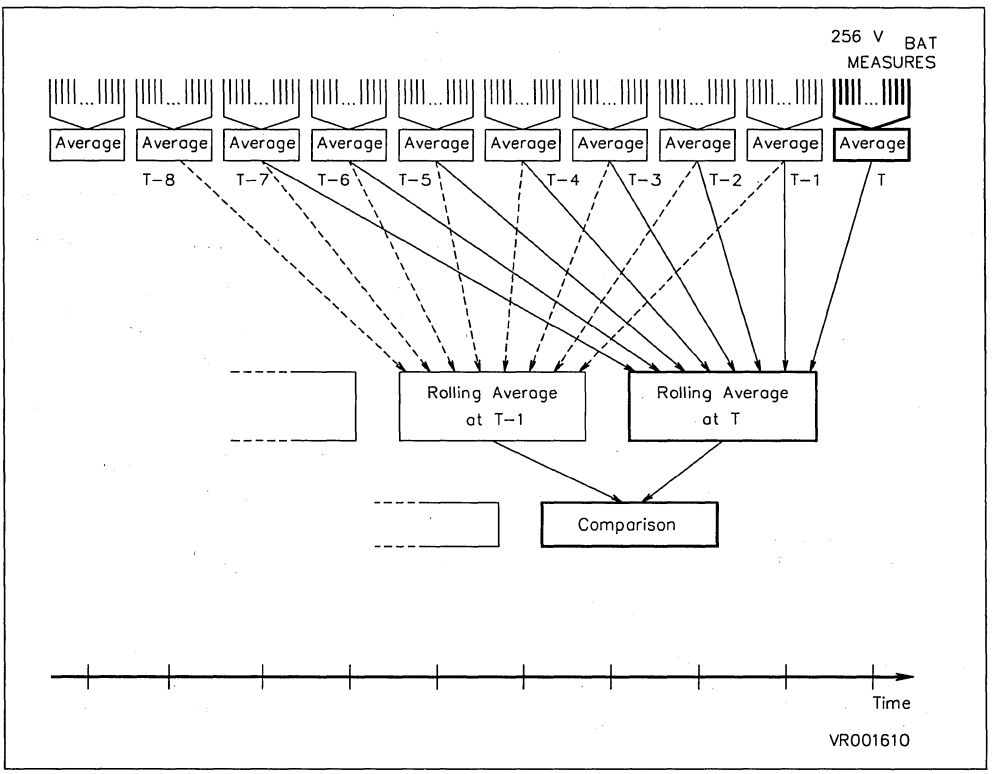
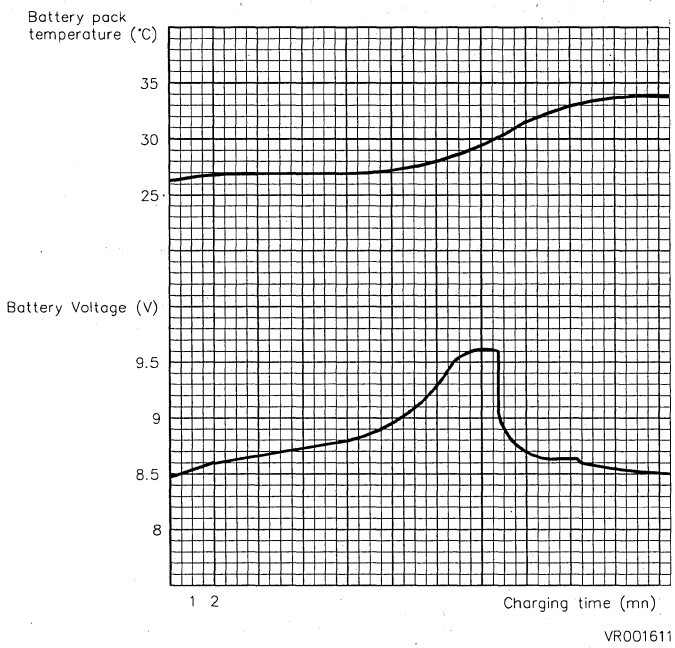


Figure 5 . VBAT and Pack. Temp Vs time



SUMMARY

Charging a NiCd battery in less than half an hour saves battery packs and time. It can enlarge the use of battery powered equipments, especially in professional applications.

Such ultra fast charging has to be carefully monitored to maximize the life time of the battery and the charge safety. Moreover, this improvement needs to be achieved with a compact equipment including a minimum of components.

The proposed power charger is realized with a conventional SMPS topology. The size and number of the magnetic components are minimized by using an integrated magnetic technique.

This note shows that an ultra fast charge can be totally monitored by a single 20 pin HCMOS microcontroller, the ST6210.

The program used in the validation of this Battery Charger is available from SGS-THOMSON. This software routine has the basic ultra fast charger and many additional features including stand-by charge, temperature protection, battery presence detection and automatic battery voltage sensing. Given the flexibility offered by the programmability of the ST6210, other specific requirements can be implemented. Consult your local SGS-THOMSON sales office or franchised distributor.

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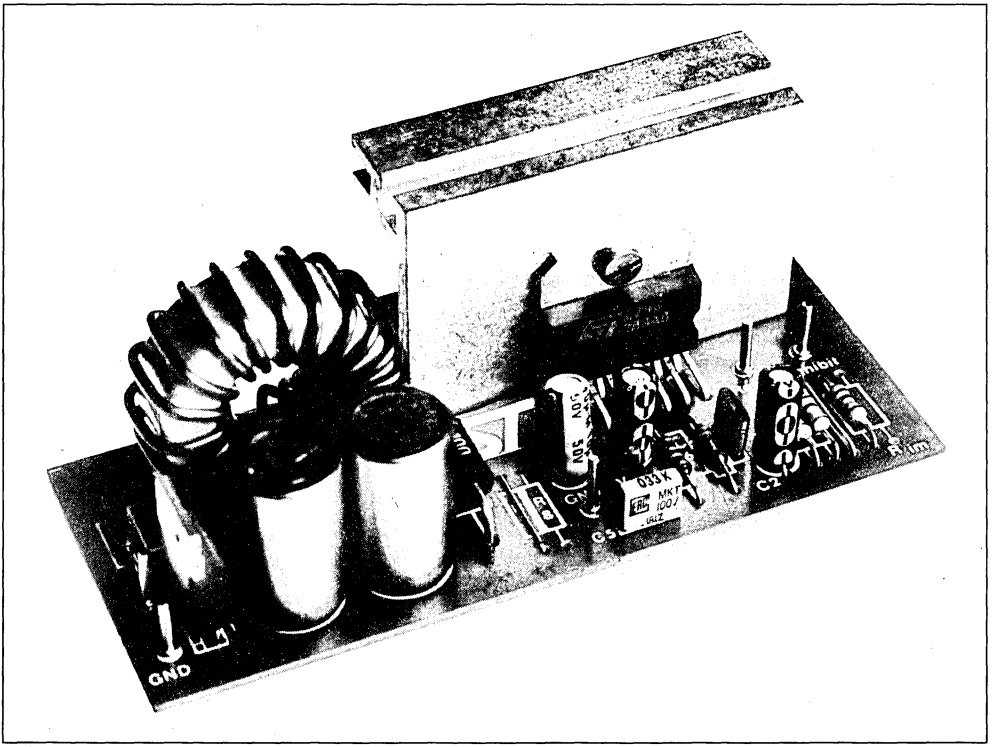
SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

DESIGNING WITH THE L296 MONOLITHIC POWER SWITCHING REGULATOR

A cost-effective replacement for costly hybrids, the L296 Power Switching Regulator delivers 4A at an output voltage of 5.1V to 40V and includes many popular supply features. This comprehensive application guide explains how the device operates and how it is used. Typical application circuits are also presented.



The SGS THOMSON L296 is the first monolithic switching regulator in plastic package which includes the power section. Moreover, the circuit includes all the functions which make it specially suited for microprocessor supply.

Before the introduction of L296, which realizes the step down configuration, this function was implemented with discrete power components driven be integrated PWM regulator circuits (giving a maximum output current of 300 to 400mA) or with hybrid circuits. Both of these solutions are characterized by a low efficiency of the power transistor. For this reason it is generally necessary to operate at frequencies in the 20kHz to 40kHz range. Of the two alternatives discrete solutions are usually less expensive because they do not include as many functions as the L296.

With the new L296 regulator the driving problem of the power control stage has been eliminated. Besides a higher overall efficiency, it is therefore also possible to operate directly at frequencies as high as 100kHz. At 200kHz the device still operates (further reducing the cost of the L and C external components) when a reduction of a few percent in efficiency is acceptable.

The device delivers a maximum current of 4 A to the load, at an output voltage adjustable from 5.1 to 40V ; the maximum operating input voltage is 46V. The high voltage and the high current capabilities of the device are a result of the special technology used and the special care taken in designing the power transistor. Essential requirements for a good power transistor are high gain and high current levels, low saturation voltage and good second breakdown robustness. To achieve high gain at high current levels, the power transistor has to be designed to maximize the emitter's perimeter/area ratio.

In the L296 power transistor, realized with a high voltage (50V) process, current densities in the magnitude order of 10mA/Mil^2 are achieved.

In its most complete configuration, in which all the available functions are being used, a significant reduction of the external component count is achieved compared with discrete component solution.

The L296 is mounted in a MULTIWATT® plastic package with 15 pins, minimizing the cost per watt and allowing a low thermal resistance of 3°C/W between junction and package and of 35°C/W between junction and ambient. This thermal resistance (inclucing the contact resistance) is comparable to that of the more costly metal TO-3 packages.

THE STEP-DOWN CONFIGURATION

Fig. 1 shows the simplified block diagram of the circuit realizing the step-down configuration. This circuit operates as follows : Q1 acts as a switch at the frequency f and the ON and OFF times are suitably controlled by the pulse width modulator circuit. When Q1 is saturated, energy is absorbed from the input which is transferred to the output through L. The emitter voltage of Q1, V_E, is Vi-Vsat when Q is ON and $-V_F$ (with V_F the forward voltage across the D diode as indicated) when Q1 is OFF. During this second phase the current circulates again through L and D. Consequently a rectangular shaped voltage appears on the emitter of Q1 and this is then filtered by the L-C-D network and converted into a continuous mean value across the capacitor C and therefore across the load. The current through L consists of a continuous component, I_{LOAD}, and a triangular-shaped component super-imposed on it, ΔI_L, due to the voltage across L.

Figure 1 : The Basic Step-down Switching Regulator Configuration.

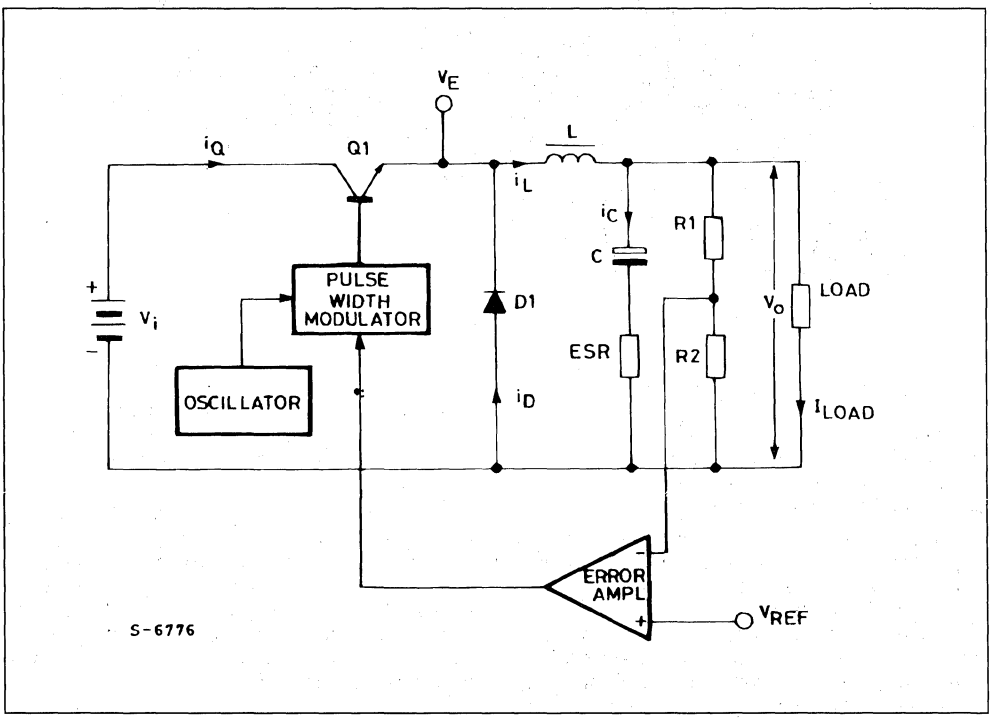


Figure 2 : Principal Circuit Waveforms of the figure 1 Circuit.

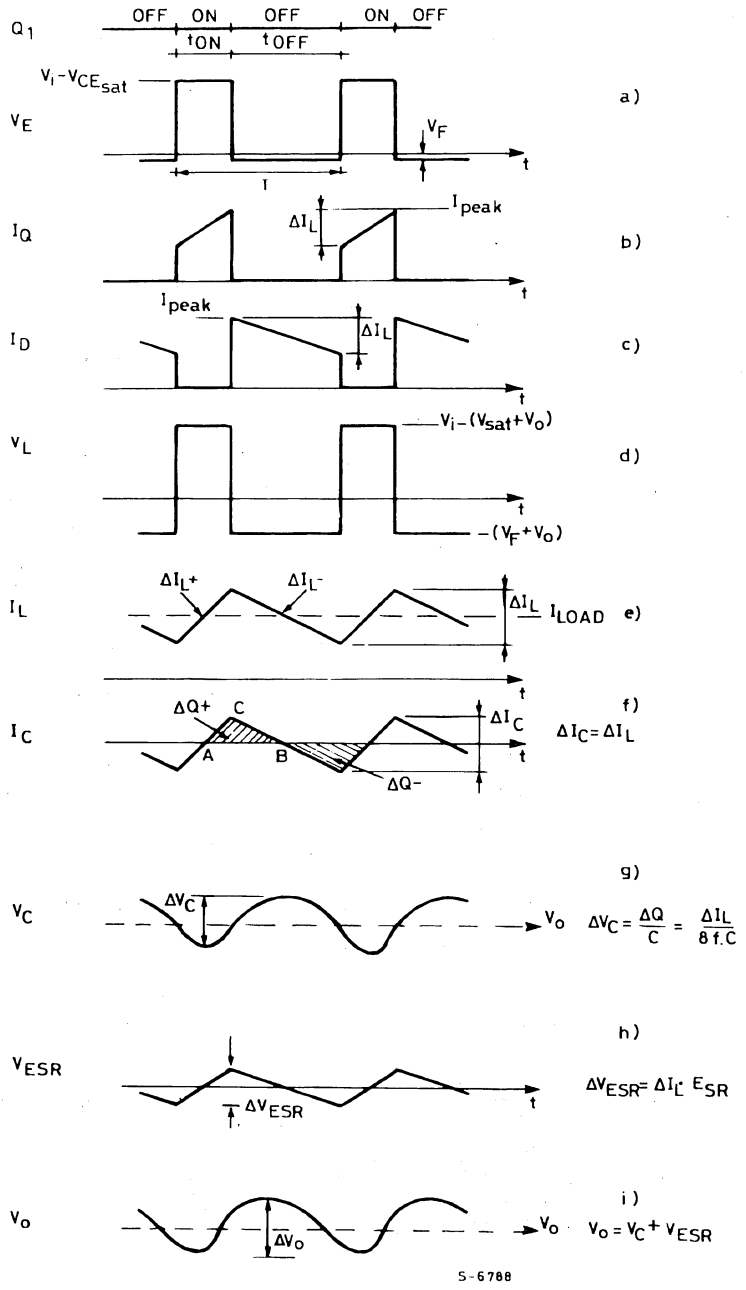


Fig. 2 shows the behaviour of the most significant waveforms, in different points of the circuit, which help to understand better the operation of the power section of the switching regulator. For the sake of simplicity, the series resistance of the coil has been neglected. Fig. 2a shows the behaviour of the emitter voltage (which is practically the voltage across the recirculation diode), where the power saturation and the forward V_F drop across the diode era taken into account.

The ON and OFF times are established by the following expression :

$$V_o = (V_i - V_{sat}) \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

Fig. 2b shows the current across the switching transistor. The current shape is trapezoidal and the operation is in continuous mode. At this stage, the phenomena due to the catch diode, that we consider as dynamically ideal, are neglected. Fig. 2c shows the current circulating in the recirculation diode. The sum of the currents circulating in the power and in the diode is the current circulating in the coil as shown in fig. 2e. In balanced conditions the ΔI_L^+ current increase occuring during T_{ON} has to be equal to the ΔI_L^- decrease occurring during T_{OFF}. The mean value of I_L corresponds to the charge current.

The current ripple is given by the following formula :

$$\Delta I_L^+ = \Delta I_L^- = \frac{(V_i - V_{sat}) - V}{L} T_{ON} = \frac{V_o + V_F}{L} T_{OFF}$$

It is a good rule to respect to $I_{OMIN} \geq I_L/2$ relationship, that implies good operation in continuous mode. When this is not done, the regulator starts operating in discontinuous mode. This operation is still safe but variations of the switching frequency may occur and the output regulation decreases.

Fig. 2d shows the behaviour of the voltage across coil L. In balanced conditions, the mean value of the voltage across the coil is zero. Fig. 2f shows the current flowing through the capacitor, which is the difference between I_L and I_{LOAD}.

In balanced conditions, the mean current is equal to zero, and $\Delta I_C = \Delta I_L$. The current I_C through the capacitor gives rise to the voltage ripple.
This ripple consists of two components : a capacitive component, ΔV_C, and a resistive component, ΔV_{ESR}, due to the ESR equivalent series resistance of the capacitor. Fig. 2g shows the capacitive component ΔV_C of the voltage ripple, which is the integral of a triangular-shaped current as a function of time. Moreover, it should be observed that v_C (t) is in quadrature with i_C(t) and therefore with the voltage V_{ESR}. The quantity of charge ΔQ^+ supplied to the capacitor is given by the area enclosed by the ABC triangle in fig. 2f :

$$\Delta Q = \frac{1}{2} \cdot \frac{T}{2} \cdot \frac{\Delta I_L}{2}$$

which therefore gives :

$$\Delta V_C = \frac{Q}{C} = \frac{\Delta I_L}{8fc}$$

Fig. 2h shows the voltage ripple V_{ESR} due to the resistive component of the capacitor. This component is V_{ESR} (t) = i_C (t) · ESR. Fig. 2i shows the overall ripple V_o, which is the sum of the two previous components. As the frequency increases (> 20kHz), which is required to reduce both the cost and the sizes of L and C, the V_{ESR} component becomes dominant. Often it is necessary to use capacitors with greater capacitance (or more capacitors connected in parallel to limit the value of ESR within the required level.

We will now examine the stepdown configuration in more detail, referring to fig. 1 and taking the behaviour shown in fig. 2 into account.

Starting from the initial conditions, where Q = ON, $v_C = V_o$ and $i_L = i_D = 0$, using Kirckoff second principle we may write the following expression :

$V_i = v_L + v_C$ (V_{sat} is neglected against V_i).

$$V_i = L \frac{di_L}{dt} + v_C = L \frac{di_L}{dt} + V_o \quad (1)$$

which gives :

$$\frac{di_L}{dt} = \frac{(V_i - V_o)}{L} \quad (2)$$

The current through the inductance is given by :

$$I_L = \frac{(V_i - V_o)}{L} t \quad (3)$$

When V_i, V_o, and L are constant, I_L varies linearly with t. Therefore, it follows that :

$$\Delta I_L^+ = \frac{(V_i - V_o) T_{ON}}{L} \quad (4)$$

When Q is OFF the current through the coil has reached its maximum value, I_{peak} and because it cannot very instantaneously, the voltage across the coil is inverted and the diode D becomes forward biased to allow the recirculation of the current through the load.

When Q switches OFF, the following situation is present :

$v_C(t) = V_o$, $i_L(t) = i_D(t) = I_{peak}$

And the equation associated to the following loop may be written :

$$V_F + L\frac{di_L}{dt} + v_C = 0 \qquad (5)$$

where :

$$v_C = V_o$$

$$\frac{di_L}{dt} = -(V_F + V_o)/L \qquad (6)$$

It follows therefore that :

$$i_L(t) = -\frac{V_F + V_o}{L}\, t \qquad (7)$$

The negative sign may be interpretated with the fact that the current is now decreasing. Assuming that V_F may be neglected against V_o, during the OFF time the following behaviour occurs :

$$I_L = \frac{V_o}{L}\, t \qquad (8)$$

therefore :

$$\Delta I_L^- = \frac{V_o}{L}\, T_{OFF} \qquad (9)$$

But, because

$\Delta I_L^+ = \Delta I_L^-$ if follows that :

$$\frac{(V_i - V_o)\, T_{ON}}{L} = \frac{V_o\, T_{OFF}}{L}$$

which allows us to calculate V_o :

$$V_o = V_i \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_i \frac{T_{ON}}{T} \qquad (10)$$

where T is the switching period.

Expression (10) links the output voltage V_o to the input voltage V_i and to the duty cycle. The relationship between the currents is the following :

$$I_{iDC} = Io_{DC} \cdot \frac{T_{ON}}{T}$$

EFFICIENCY

The system efficiency is expressed by the following formula :

$$\eta\,\% = \frac{P_o}{P_i}\ 100$$

where $P_o = V_o I_o$ (with $I_o = I_{LOAD}$)

is the output power to the load and P_i is the input power absorbed by the system. P_i is given by P_o, plus all the other system losses. The expression of the efficiency becomes therefore the following :

$$\eta = \frac{P_o}{P_o + P_{sat} + P_D + P_L + P_q + p_{sw}} \qquad (12)$$

DC LOSSES

P_{sat} : saturation losses of the power transistor Q. These losses increase as V_i decreases.

$$P_{sat} = V_{sat} \cdot I_o \frac{T_{ON}}{T} = V_{sat}\, I_o \frac{V_o}{V_i} \qquad (13)$$

where $\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ and V_{sat} is the power transistor saturation at current Io.

P_D : losses due to the recirculation diode. These losses increase as V_i increases, as in this case the ON time of the diode is greater.

$$P_D = V_F I_o \frac{V_i - V_o}{V_i} = V_F I_o \left(1 - \frac{V_o}{V_i}\right) \qquad (14)$$

where V_F is the forward voltage of the recirculation diode at current I_o.

P_L : losses due to the series resistance R_S of the coil

$$P_L = R_S I_o^2 \qquad (15)$$

P_q : losses due to the stand-by current and to the power driving current :

$$P_q = V_i I'_{3q} + V_i I''_{3q} \frac{T_{ON}}{T} \qquad (16)$$

where being :

$\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ it follows that :

$P_q = V_i I'_{3q} + V_o I''_{3q}$ in which :

$I'_{3q} = I_{3q}$ at 0 % duty cycle

$I''_{3q} = I_{3q(100\,\%\ d.c.)} - I_{3q\ (0\,\%\ d.c.)}$

SWITCHING LOSSES

P_{sw} : switching losses of the power transistor :

$$P_{sw} = V_i I_o \frac{t_r + t_f}{2T}$$

The switching losses of the recirculation diode are neglected (which are anyway negligible) as it is assumed that diode is used with recovery time much smaller than the rise time of the power transistor.

We can neglect losses in the coil (it is assumed that ΔI_L is very small compared to I_o) and in the output capacitor, which is assumed to show a low ESR.

Calculation of the inductance value, L

Calculation T_{ON} and T_{OFF} through (4) and (9) respectively it follows that :

$$T_{ON} = \frac{\Delta I_L^+ \cdot L}{V_i - V_o} \qquad T_{OFF} \quad \frac{\Delta I_L^- \cdot L}{V_o}$$

But because :

$T_{ON} + T_{OFF} = T$ and $\Delta I_L^+ = \Delta I_L^- = \Delta I_L$,

it follows that :

$$\frac{\Delta I_L \cdot L}{V_i - V_o} + \frac{\Delta I_L \cdot L}{V_o} = T$$

Calculating L, the previous relation becomes :

$$L = \frac{(V_i - V_o)\, V_o}{V_i\, \Delta I_L}\, T \qquad (18)$$

Fixing the current ripple in the coil required by the design (for instance 30% of I_o), and introducing the frequency instead of the period, it follows that :

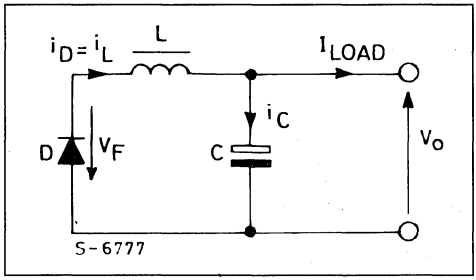
$$L = \frac{(V_i - V_o)\, V_o}{V_i \cdot 0.3 \cdot I_o \cdot f}$$ where L is in Henry and f in Hz

Calculation of the output capacitor C

From the output node in fig. 3 it may be seen that the current through the output capacitor is given by :

$i_C(t) = i_L(t) - I_o$

Figure 3 : Equivalent Circuit Showing Recirculation when Q1 is Turned Off.



From the behaviour shown in fig. 2 it may be calculated that the charge current of the output capacitor, within a period, is $\Delta I_L/4$, which is supplied for a time T/2. It follows therefore that :

$$\Delta V_C = \frac{\Delta I_L}{4C}\,\frac{T}{2} = \frac{\Delta I_L\, T}{8C} = \frac{\Delta I_L}{8fC} \qquad (19)$$

but, remembering expression (4) :

$$\Delta I_L^+ = \frac{(V_i - V_o)\, T_{ON}}{L} \quad \text{and} \quad T_{ON} = \frac{V_o}{V_i}\, T$$

therefore equation (19) becomes :

$$\Delta V_C = \frac{(V_i - V_o)\, V_o}{8\, V_i f^2\, L\, C}$$

Finally, calculating C it follows that :

$$C = \frac{(V_i - V_o)\, V_o}{8\, V_i\, \Delta V_C\, f^2\, L} \qquad (20)$$

where : L is in Henrys
C is in Farads
f is in Hz

Finally, the following expression should be true :

$$ESR_{max} = \frac{\Delta V_{Cmax}}{\Delta I_L} \qquad (21)$$

It may happen that to satisfy relation (21) a capacitance value much greater than the value calculated through (20) must be used.

TRANSIENT RESPONSE

Sudden variations of the load current give rise to overvoltages and undervoltages on the output voltage. Since $i_C = C\,(dv_C/dt)$ (22), where $dv_C = \Delta V_o$, the instantaneous variation of the load current ΔI_o is supplied during the transient by the output capacitor. During the transient, also current through the coil tends to change its value.
Moreover, the following is true :

$$v_L = L\,\frac{di_L}{dt} \qquad (23) \qquad \text{where } di_L = \Delta I_o.$$

$v_L = V_i - V_o$ for a load increase

$v_L = V_o$ for a load decrease

Calculating dt from (22) and (23) and equalizing, it follows that :

$$L\,\frac{di_L}{v_L} = C\,\frac{dv_C}{i_C}$$

Calculating dv_C and equalizing it to ΔV_o, it follows that :

$$\Delta V_o = \frac{L \Delta I_o^2}{C(V_i - V_o)} \qquad (24) \qquad \text{for } + \Delta I_o$$

$$\Delta V_o = \frac{L \Delta I_o^2}{C V_o} \qquad (25) \qquad \text{for } - \Delta I_o$$

From these two expressions the dependence of overshoots and undershoots on the L and C values may be observed. To minimize ΔV_o it is therefore necessary to reduce the inductance value L and to increase the capacitance value C. Should other auxiliary functions be required in the circuit like reset or crowbar protections and very variable loads may be present, it is worthwhile to take special care for minimizing these overshoots, which could cause spurious operation of the crowbar, and the undershoot, which could trigger the reset function.

DEVICE DESCRIPTION

Fig. 4 shows the package in which the device is mounted and the pin function assignments.

The internal structure of the device is shown in fig. 5. Each block will now be examined.

Power supply

The device is provided with an internal stabilized power supply that, besides supplying the reference voltage of 5.1V for the whole system, also supplied the internal analog blocks.

Special features of the voltage reference are its accuracy, temperature stability and high line rejection. Through zenze-zap trimming, the voltage is within ± 2% limits.

Figure 4 : Pin Assignments of the L296.

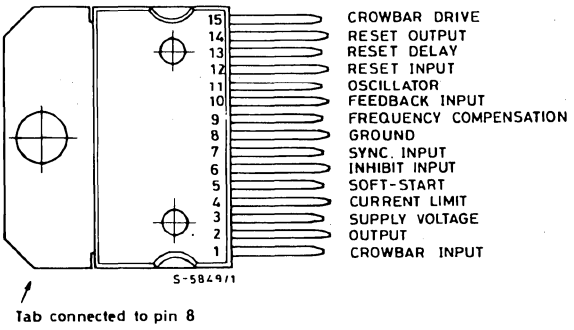
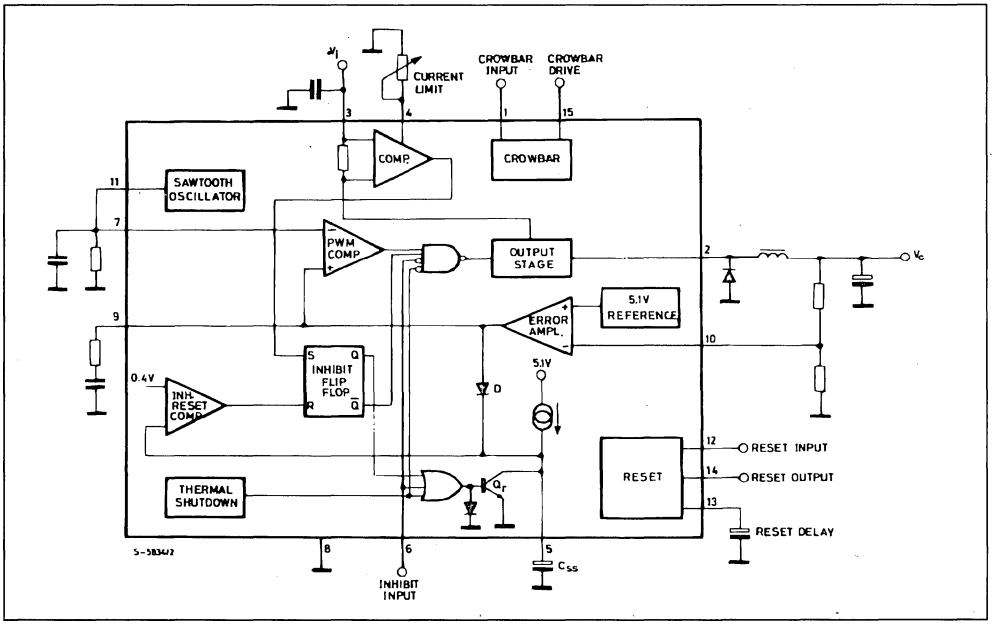


Figure 5 : Block Diagram of the L296. In Addition to the Basic Regulation Loop the Device includes Functions such as Reset, Crowbar and Current Limiting.



OSCILLATOR

The oscillator block generates the saw-tooth waveform that sets the switching frequency of the system. This signal, compared with the output voltage of the error amplifier, generates the PWM signal to be sent to the power output stage. The saw-tooth, whose amplitude is between 1.2V and 3.2V, is generated by charging rapidly the C_{osc} capacitor which then discharges across the R_{osc} resistance. As shown in fig. 6, the oscillator is realized by a comparator (with grounded compatible input) with hysteresis whose thresholds are 1.2V and 3.2V respectively. The C_{osc} capacitor and the R_{osc} resistance are connected to the non-inverting input of the comparator which set the oscillating frequency is fixed. When the voltage on pin 11 is less than 3.2V, the switch S_1 is closed and the current generator charges the C_{osc} capacitor rapidly ; in this phase S_2 is also closed. As soon as 3.2V is reached the comparator output drives S_2 open (therefore opening S_1, too) ; the inverting input voltage is reduced to about 1.2V and the capacitor starts to discharge itself across the R_{osc} resistor (the I_{bias} effect is neglected). When the voltage reaches 1.2V, S_2 and S_1 close again and a new cycle starts. The generated waveform is shown in fig. 7.

To achieve a good accuracy of the switching frequency it is essential to have a charging time of the capacitor which is much smaller than the discharging time. In this way, the oscillation frequency only depends on the external components C_{osc} and R_{osc}. For this reason the capacitor charging current (when S_1 is ON) is typically around 10mA. For example, with a 2.2nF capacitor to switch from 1.2V to 3.2V about 400ns is required, which is negligible compared to the 10µs period that occurs when the operation is performed at 100kHz. The diagrams shown in fig. 8 allow the calculation of the R_{osc} value (R_1 in fig. 8) with C_{osc} as a parameter (C_3 in fig. 8) when the oscillation frequency required for operation has been previously fixed.

Figure 6 : Internal Schematic of the Oscillator.

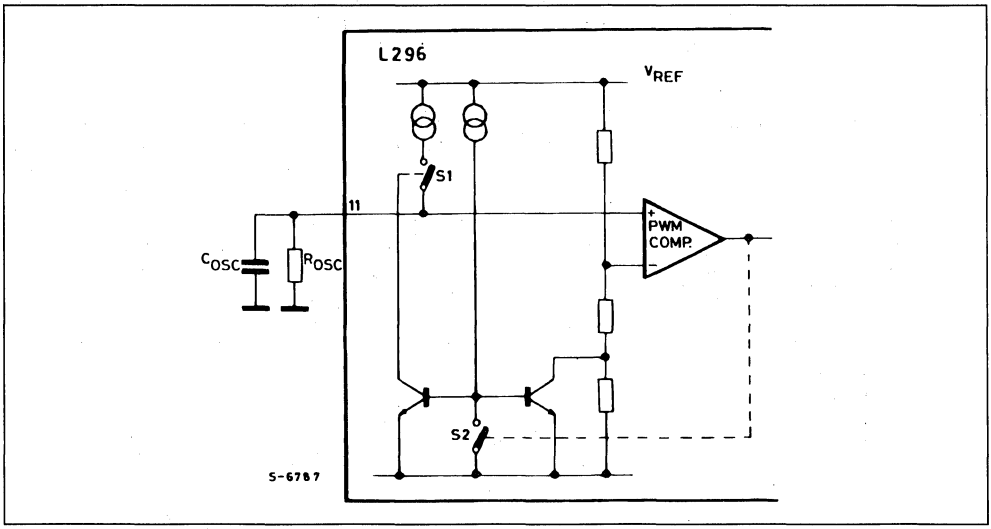


Figure 7a : Oscillator Waveform at Pin 11 with f = 100Khz (R_{osc} = 4.3KΩ, C_{osc} = 2.2nF).

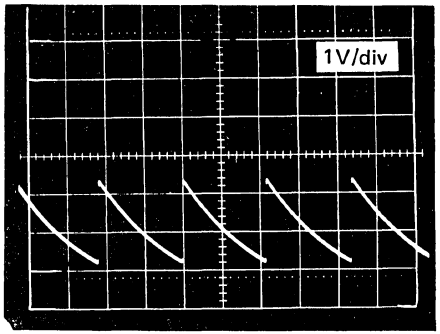


Figure 7b : Oscillator Waveform at Pin 11 with f = 50Khz (R_{osc} = 9.1KΩ, C_{osc} = 2.2nF).

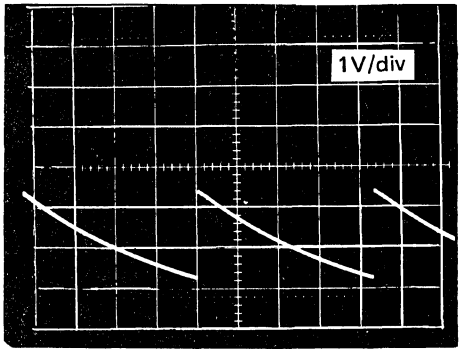


Figure 8 : Nomogram for the Choice of Oscillator Components.

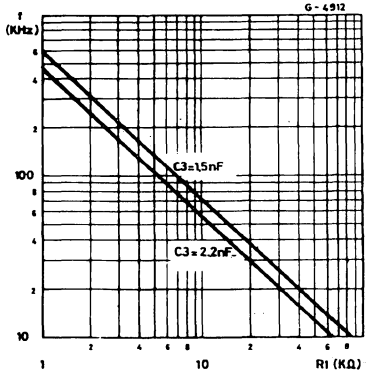


Fig. 8 shows two suggested values for the C_{osc} capacitance. Excessively low capacitance value may give rise to an inaccuracy of the upper threshold due to the switching delays of the comparator. This inaccuracy in caused by an excessively short rise time of the voltage. A capacitance value too high gives rise to a charging time which is too compared to the discharging time. An additional inaccuracy cause would be therefore present for the switching frequency, now due to spread of the charge current.

The oscillation frequency is given by the following formula :

$$f_{osc} = \frac{1}{R_{osc}\, C_{osc}} \qquad (26)$$

PWM (see fig. 9)

The PWM signal is generated on the comparator output ; the triangular-shaped waveform and the continuous signal coming from the output of the transconductance error amplifier are sent to its inputs. The PWM signal is then transferred to the driving stage of the output power transistor.

SOFT START (see fig. 9)

Soft start is an essential function for correct start-up, to prevent stresses and possible breakdown from occurring in the power transistor and to obtain a monotonically increasing output voltage.
In particular, the L296, as it does not have any duty cycle limitation and due to the type of current limitation does not allow the output to be forced to a steady state without the aid of the soft-start facility. Soft-start operates at the start-up of the system, after the inhibit has been activated, after an intervention of the current limitation and after the intervention of the thermal protection.

The soft-start function is realized through a capacitor connected to pin 5 which is charged at constant current (≅ 100μA) up to a value of about V_{REF}. During the charging time, through PNP transistor Q58, the voltage on pin 9 is forced to increase with the same rising speed as on pin 5. Starting from the discharged capacitor condition (pin 5 voltage = 0V) the power transistor is in the OFF condition, as the voltage on pin 9 is smaller than the minimum level of the ramp voltage. As the capacitor is charged, the PWM signal begins to be generated as soon as the error amplifier output voltage crosses the ramp ; the power stage starts to switch with steadily increasing duty cycle. This behaviour is shown in fig. 10. As soon as the steady condition is reached the duty cycle sets itself to the right value due to the effect of the feedback network while the soft-start capacitor completes its charging to a value very close to V_{REF}.

The soft-start effect is determined, apart from the switch-on time, when the current limitation operates, due to either an overload or a short circuit, to keep the mean value of the current absorbed by the power supply low.

Moreover from fig. 11 it may be observed that since the voltage on pin 9 can decrease under the minimum ramp level and increase over the maximum level no limitations have been provided on the duty cycle, which therefore may vary between 0 and 100%.

Figure 9 : Partial Internal Schematic Showing PWM and Soft Start Blocks.

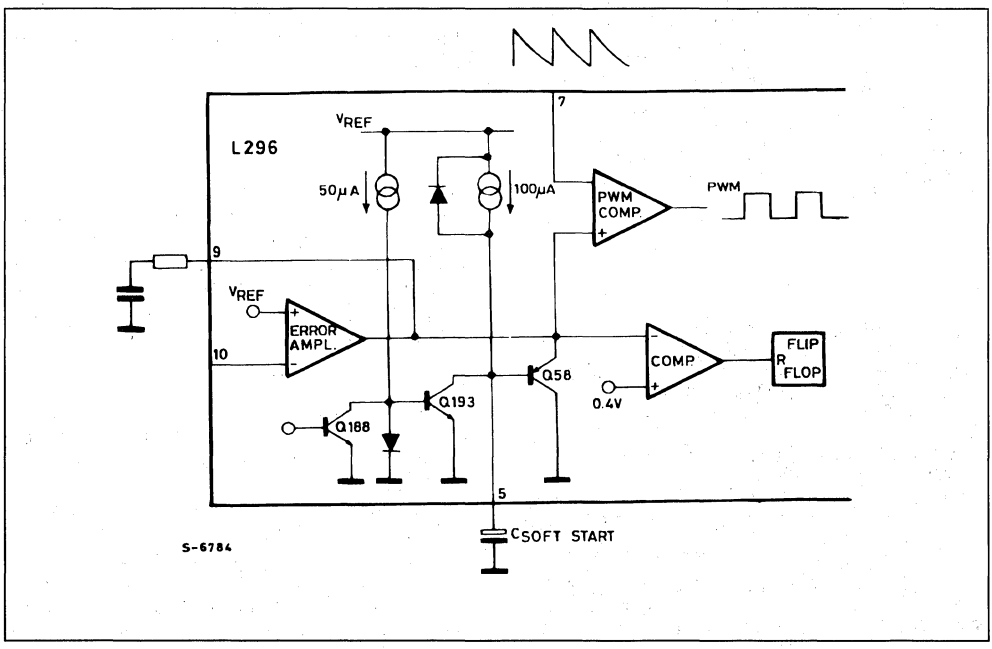


Figure 10 : Soft Start Waveforms. When power is applied, or after an inhibit, the L296's output current rises slowly under control of the soft start circuit.

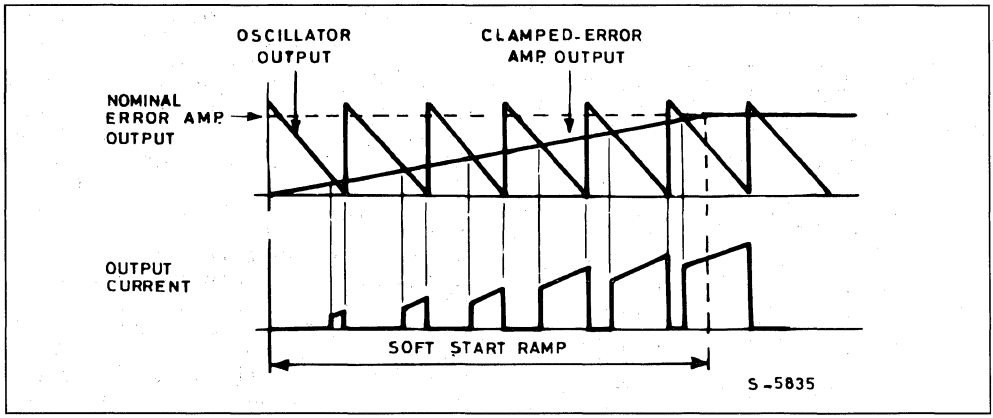
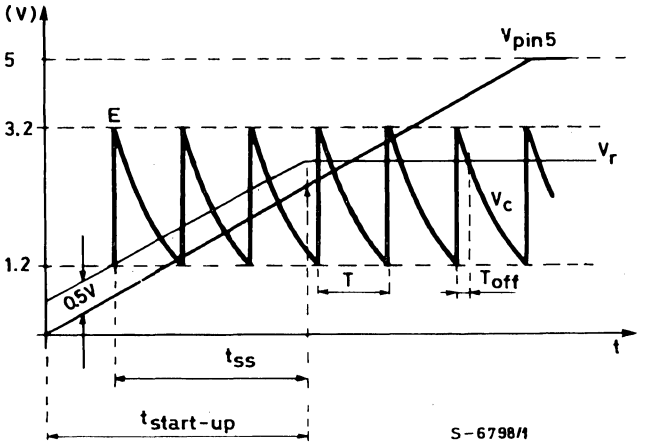


Figure 11 : Waveform for Calculation of Duty Cycle and Soft Start Time.



CALCULATING THE DUTY CYCLE AND SOFT-START TIME

Assume, for simplicity, that the rising edge of the ramp is instantaneous ; V_r is the output voltage of the error amplifier and V_c the ramp voltage (see fig. 11). The PWM comparator block switches when $V_r = V_c$; therefore :

$$V_r = V_c = E\, e^{-\frac{t}{R_{osc}\, C_{osc}}}$$

Consequently :

$$t = R_{osc}\, C_{osc}\, \ln\frac{E}{V_r}$$

The time obtained from this expression is the T_{OFF} time of the power transistor. The duty cycle d is given by :

$$d = \frac{T_{ON}}{T} = \frac{T - R_{osc}\, C_{osc}\, \ln\frac{E}{V_r}}{T} = \quad (27)$$

$$= 1 - \ln\frac{E}{V_r} = \frac{Vo}{Vi}$$

Consequently, starting with the capacitor discharged, the output of the regulator will be at the nominal level when the voltage at the terminal of the capacitor (which is charged by a constant current) has reached $V_r - 0.5V$.

$$t_{start\text{-}up} = \frac{C_{ss}\,(V_r - 0.5V)}{I_{5so}}$$

where C_{ss} is the soft-start capacitor and I_{5so} is the charging current.

Considering as the soft-start time the time required for the soft-start capacitor to charge from (1.2 V – 0.5V) to V_r – 0.5V, gives :

$$t_{ss} = \frac{C_{ss}\,(V_r - 1.2)}{I_{sso}}$$

substituting V_r from (27) gives :

$$V_r = E\, e^{-\left(1 - \frac{Vo}{Vi}\right)}$$

substituting into (28) gives :

$$t_{ss} = \frac{C_{ss}}{I_{sso}}\,(E\, e^{\left(\frac{Vo}{Vi} - 1\right)} - 1.2)$$

SYNCHRONIZATION

The synchronization function is available on pin 7, this function allows the device to be switched at an externally generated frequency (leaving pin 11 open), or to mutually synchronize several devices, using one of them as master and the others as slave (fig. 12).

This allows several devices to be operated at the same frequency, avoiding undesirable intermodulation phenomena. The number if mutually synchronizable devices is obviously much greater than the three devices shown in the figure. It is anyway diffi-

cult to establish an exact maximum number of devices, as it depends on different conditions.

The first consideration concerns the accuracy which must be achieved and maintained on the oscillation frequency. Since the bias current on pin 7 is an output current, the sum of all the bias currents must be much smaller than the capacitor discharge current in close proximity to the lower discharge threshold. Therefore, assuming $C_{osc} = 2.2nF$ and $R_{osc} = 4.3K\Omega$, it follows that :

$$\frac{1.2V}{4.3K\Omega} = 280\mu A$$

Assuming that a 10% variation may be accepted, it follows therefore that the number of synchronizable devices is given by :

$$N = \frac{28\mu A}{I_{bias\ max}}$$

This means that if the overall I_{bias} is too high it may modify the discharging time of the capacitor.

The second consideration concerns the layout design.

In the presence of a great number of devices to be synchronized, the lenght of the paths may become significant and therefore the distributed inductance introduced along the paths may begin to modify the triangular shaped waveform, particularly the rising edge which is very steep. This effect would affect the devices that are physically located more distant from the master device.

The amplitude of the saw-tooth to be externally connected must be with in 0.5V and 3.5V, values also representing the maximum swing of the error amplifier output.

CURRENT LIMITATION

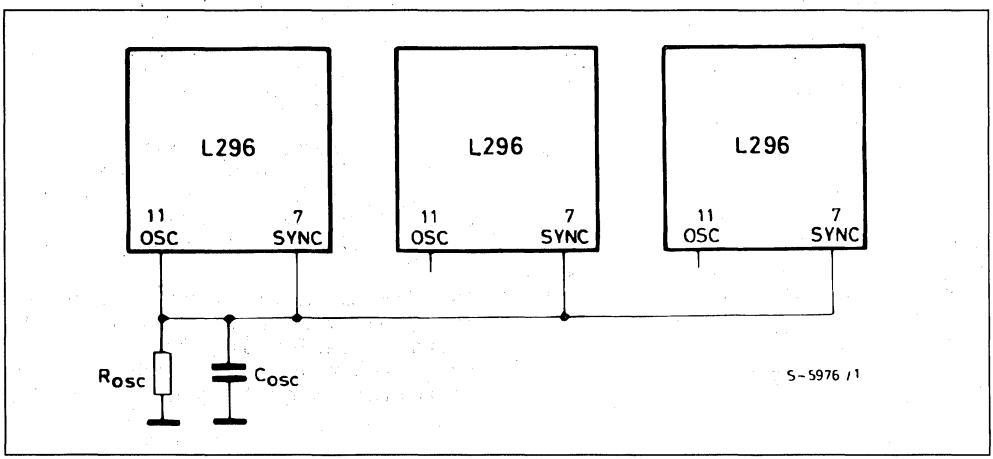
The current limitation function has been realized in a rather innovative way to avoid overload condition during the short circuit operation. In fact, while for all the other devices a constant current limitation is implemented by acting on the duty cycle (therefore, in short circuit conditions an output current is equal to the maximum limitation current), the new control approach allows operation in short circuit conditions with a mean current much smaller than the allowed 4A value. Operation of the current limiter will now be described.

Refer to the block diagram, fig. 13.

The current which is delivered from the output transistor to the load flows through the current sensing resistor R_S. When the voltage drop on R_S is equal to the offset voltage of the current comparator, the comparator generates a set pulse for the flip-flop, with a delay of about 1µsec. The purpose of this delay is to avoid triggering of the protection circuit on the current peak that occurs during the recirculation phase. Therefore, the output Q goes low and the power stage is immediately switched off, while the output $\overline{Q}$ goes high and acts directly on the soft-start capacitor dischargng the soft-start capacitor at a constant current (about 50µA).

When the voltage on pin 5 reaches 0.4V the comparator triggers, supplying a reset pulse to the flip-flop ; from now on, the power stage is enable and the soft-start phase starts again. When the limitation cause, either overload or short circuit, is still present the cycle repeats again. The waveform of the output current on pin 2 is shown in fig. 14.

Figure 12 : In multiple supplies several l296's can be synchronized as shown here.



From fig. 14 it may be observed how this current limitation technique allows the short circuit operation with a very low output current value.

It is possible to reduce the maximum current value by acting on pin 4. On this pin a voltage of about 3.3V is present ; by connecting a resistance a constant current, given by 3.3/R, is sent to ground. This current reduces the offset voltage of the current comparator, therefore anticipating its triggering threshold.

Figure 13 : Partial Schematic Showing the Current Limiter Circuit.

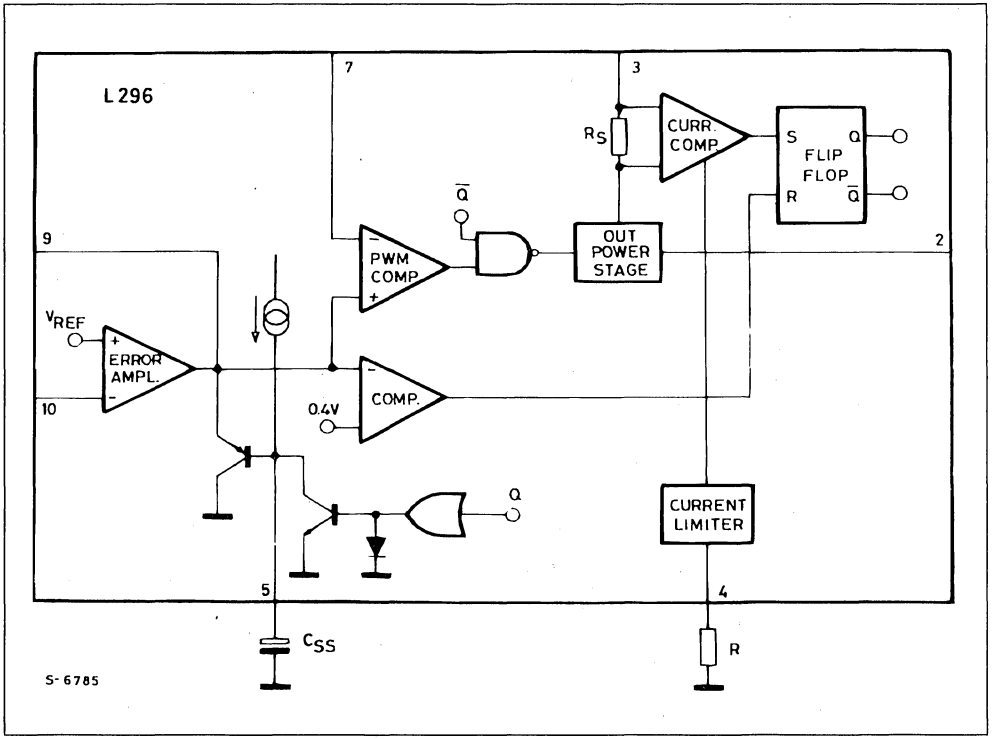


Figure 14a : Current Limiter Waveforms.

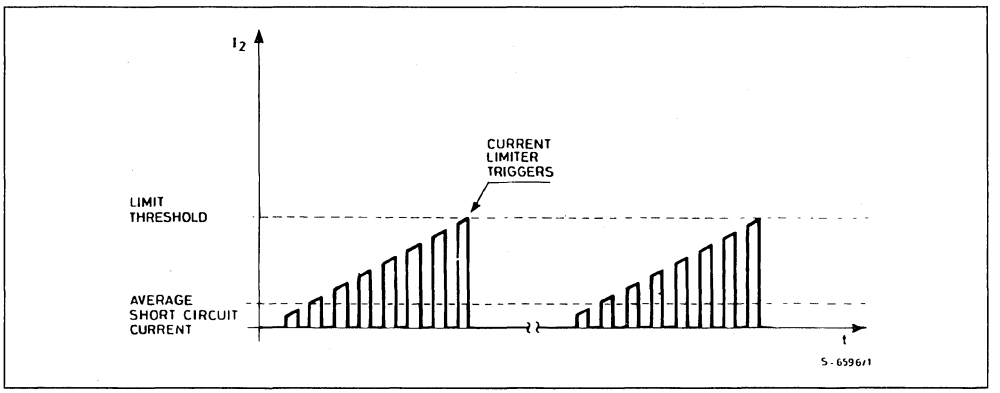


Figure 14b : Load Current in Short Circuit Conditions (V_i = 40V, L = 300µH, f = 100KΩ).

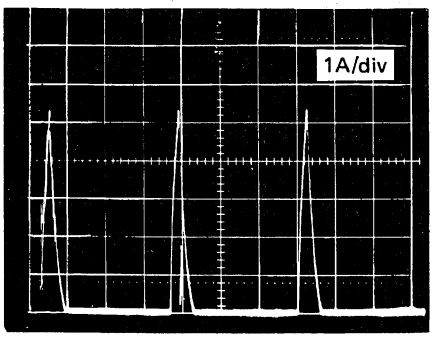
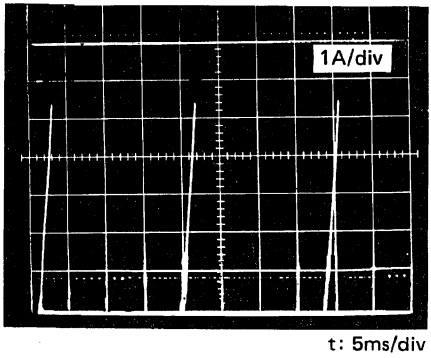


Figure 14c : Current at Pin 2 when the Output is Short Circuited.



RESET

The reset function is of great importance when the device is used to supply microprocessors, logic devices, and so on. This function differentiates the L296 device from all previous devices. The block diagram of the function is shown in fig. 15. A reset signal is generated when the output voltage is within the limits required to supply the microprocessor correctly.

The reset function is realized through the use of 3 pins : the reset input pin 12, the reset delay pin 13 and the reset output pin 14. When the voltage on pin 12 is smaller than 5V the comparator output is high and the reset capacitor is not charged because the transistor Q is saturated and the voltage on pin 14 is at low level, since Q2 is saturated, too. When the voltage on pin 12 goes above 5V, the transistor Q switches OFF and the capacitor can start to charge through a current generator of about 100µA. When the voltage on pin 13 goes above 4.5V the output of the related comparator switches low and the pin 14 goes high. As the output consists of an open collector transistor, a pull-up external resistance is required. In contrast, when the reset input voltage goes below 5V, less a hysteresis voltage of about 100mV, the comparator triggers again and instantaneously sets the voltage on pin 14 low, therefore forcing to saturation the Q1 transistor, that starts the rapid discharge of the capacitor. Obviously, the reset delay is again present when the voltage on pin 13 is allowed to go under 4.5V.

To achieve switching operations without uncertainties the two comparators have been provided with an hysteresis of about 100mV. In every operating condition the reset switching is guaranteed with a minimum reset input of 4.75V, the value required for correct operation of the microprocessor even in the presence of the minimum V_{REF} value.

Normally pin 12 is used connected to pin 10. When it is connected to the output, the function may be more properly called "reset" ; on the other hand, when it is connected through resistive divider, to the input voltage, the function is called "power fail". Fig. 16 and fig. 17 show the two possible usages.

The "power-fail" function is used to predict, with a given advance, the drop of the regulator output voltage, due to main failures, which is enough to save the data being processed into protected memory areas. Fig. 18 summarizes the reset function operation.

Figure 15 : Partial Schematic Showing Reset Circuit.

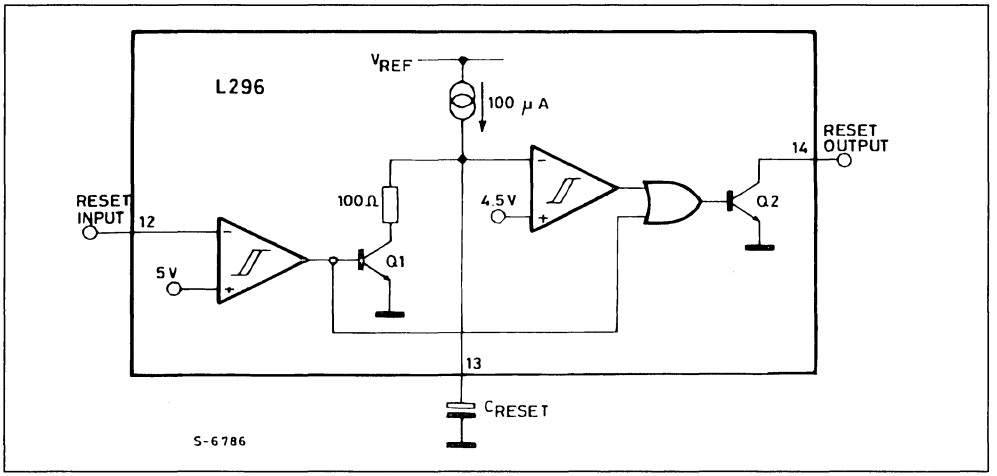


Figure 16 : For Power - On reset the reset block is connected as shown here.

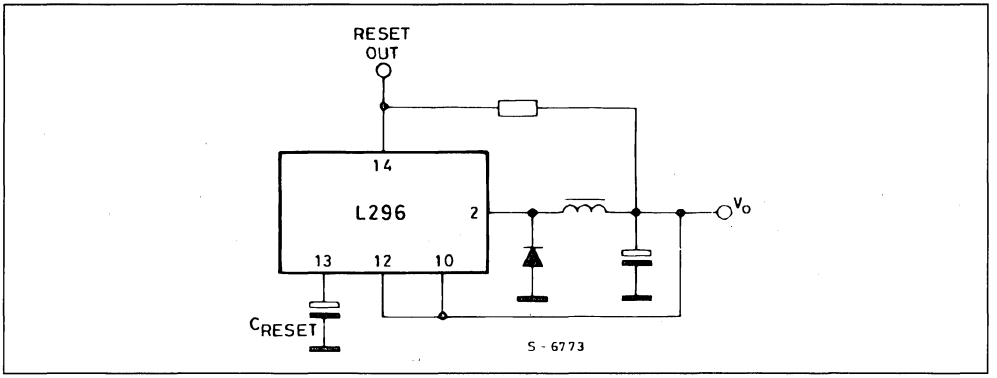


Figure 17 : To obtain a power fail signal, the reset block is connected like this.

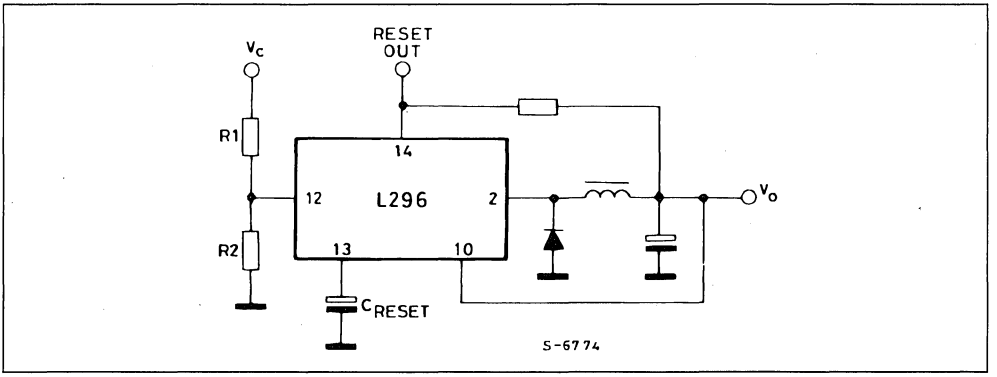
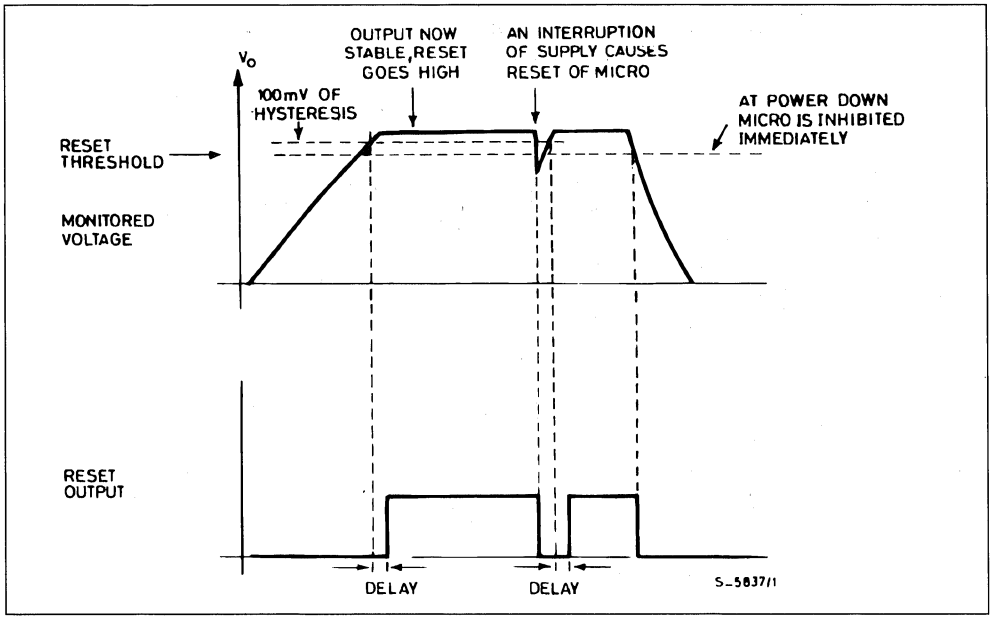


Figure 18 : Waveform of the Reset Circuit.



CROWBAR

This protection function is realized by a completely independent block, using pin 1 as input and pin 15 as output. It is used to prevent dangerous overvoltages from occurring when the output exceeds 20% of rated value. Pin 15 is able to output a 100mA current to be sent to the gate of a SCR which, triggering, short circuits either output or the input. When connected to the input, as the SCR is triggered a fuse in series connected to power supply is blown and to bring the system back to operation manual intervention is requested. Figs. 19, 20 and 21 show the different configurations.

When the voltage on pin 1 exceeds by about 20% the V_{REF} value the output stage is activated, which sends a current to the SCR gate, after a delay of about 5µsec to make the system insensitive to low-duration spikes. When activated, the output stage delivers about 100mA ; when not activated, it drains about 5mA and shows a low impedance to the SCR gate to avoid uncorrect triggering due to random noise. If the crowbar function is not used connect pin 1 to ground.

Figure 19 : Connection of Crowbar Circuit at Output for 5.1V Output Applications.

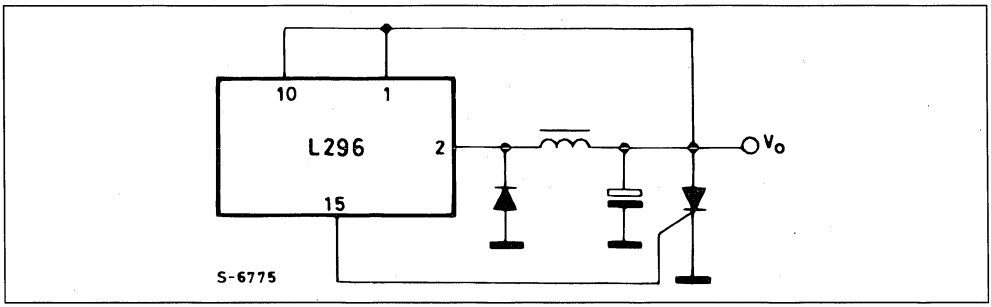


Figure 20 : Connection of Crowbar Circuit at Output for Output Voltages above 5.1V.

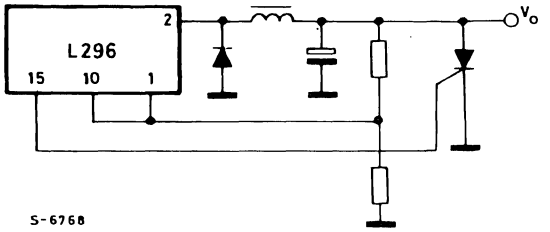
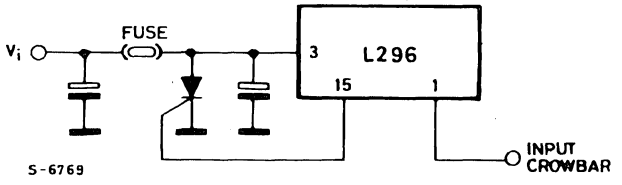


Figure 21 : Connection of Crowbar Circuit to Protect Input. When triggered, the scr blows the fuse.



INHIBIT

The inhibit input (pin 6) is TTL compatible and is activated when the voltage exceeds 2V and deactivated when the voltage goes under 0.8V. As may be seen in the block diagram, the inhibit acts on the power transistor, instantaneously switching it off and also acts on the soft-start, discharging its capacitor. When the function is unused, pin 6 must be grounded.

THERMAL PROTECTION

The thermal protection function operates when the junction temperature reaches 150°C ; it acts directly on the power stage, immediately switching it off, and on the soft-start capacitor, discharging it. The thermal protection is provided with hysteresis and, therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease of about 30°C below the intervention threshold.

APPLICATIONS

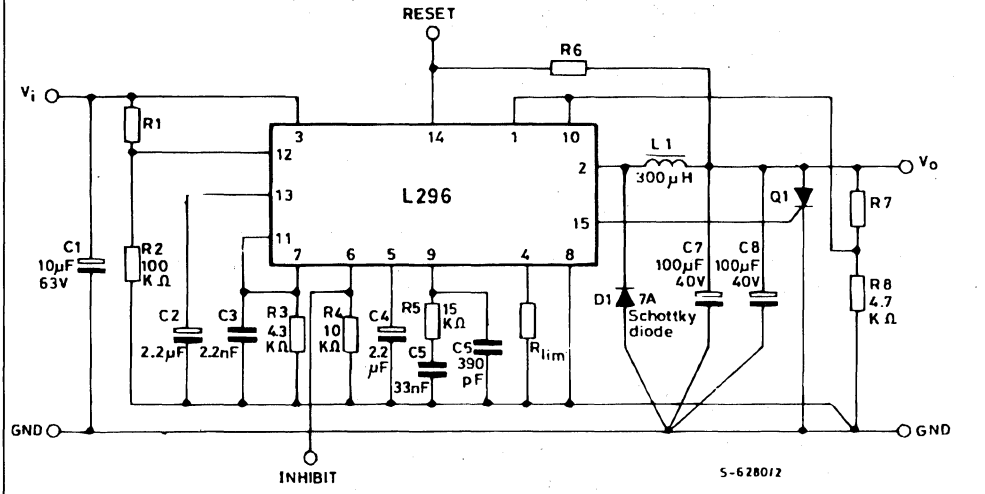
Though the L296 is designed for step-down regulator configurations it may be used in a variety of other applications. We will now examine these possibilities and show how the capabilities of the device may be extended.

In fig. 22 the complete typical application is shown, where all the functions available on the device are being used. This circuit delivers to the load a maximum current of 4A and a voltage which is established by the voltage divider constituted by R_7 and R_8 resistances. The following table is helpful for a quick calculation of some standard output voltages :

Resistor Value for Standard Output Voltages		
V_o	R_8	R_7
12 V	4.7 kΩ	6.2 kΩ
15 V	4.7 kΩ	9.1 kΩ
18 V	4.7 kΩ	12 kΩ
24 V	4.7 kΩ	18 kΩ

To obtain $V_o = V_{REF}$ the pin 10 is directly connected to the output, therefore eliminating both R_7 and R_8. The switching frequency is 100kHz.

Figure 22 : Schematic, PCB Layout and Suggested Component Values for the Evaluation Circuit used to characterize the L296. This is a typical stepdown application which exercises all the device's functions.



C7, C8 : EKR (ROE)

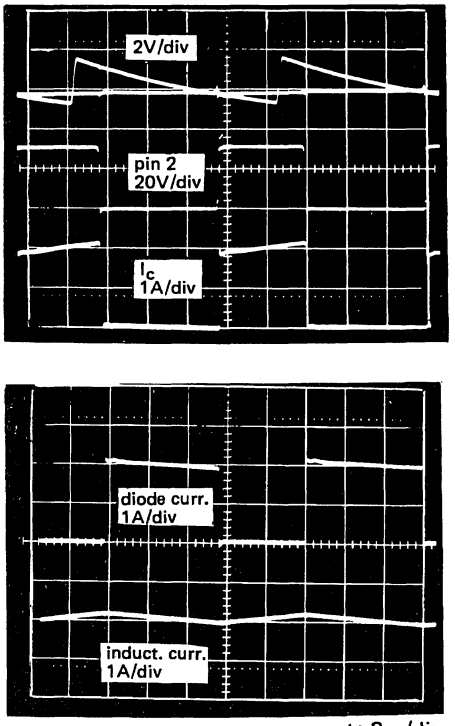
SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	
Thomson GUP 20 x 16 x 7	65	0.8 mm.	1 mm.

SUGGESTED INDUCTOR (L1) (continued)

Core Type	No Turns	Wire Gauge	Air Gap
Siemens EC 35/17/10 (B6633 & - G0500 - x 127)	40	2 x 0.8 mm.	
VOGT 250 µH Toroidal Coil, Part Number 5730501800			

Figure 23 : Oscilloscope Photographs Showing Main Waveform of the Figure 22 Circuit.



The oscilloscope photographs of the main waveforms are shown in fig. 23. The output voltage ripple ΔV_o depends on the current ripple in the coil and on the performance of the output capacitor at the switching frequency (100kHz). A capacitor suitable for this kind of application must have a low ESR and be able to accept a high current ripple, at the working frequency. For this application the Roederstein EKR series capacitors have been selected, designed for high frequency applications (> 200kHz) and manufactured to show low ESR value and to accept high current ripples. To minimize the effects of ESR, two 100μF/40V capacitors have been connected in parallel. The behaviour of the impedance as a function of frequency is shown in fig. 24.

Also the selection of the catch diode requires special care. The best choice is a Schottky diode which minimizes the losses because of its smaller forward voltage drop and greater switching frequency rate. A possible limitation comes from the backward voltage, that generally reaches 40V max.

When the full input voltage range of the device is required in this application it is possible to use super fast siodes with 35 to 50ns rated recovery time, where no more problems on the backward voltage occur (on the other hand, they show a greater forward voltage). The use of slower diodes, with trr = 100ns or more is not recommended ; The photographs in fig. 25 show the effects on the power current and on the voltage on pin 2, due to the diodes showing different speeds. Diodes showing trr greater than 35-50ns will reduce the overall efficiency of the system, increasing the power dissipated by the device.

The third component requiring care is the inductor. Fig. 22a shows the part numbers of some types used for testing. Besides having the required inductance value, the coil has to show a very high saturation current.

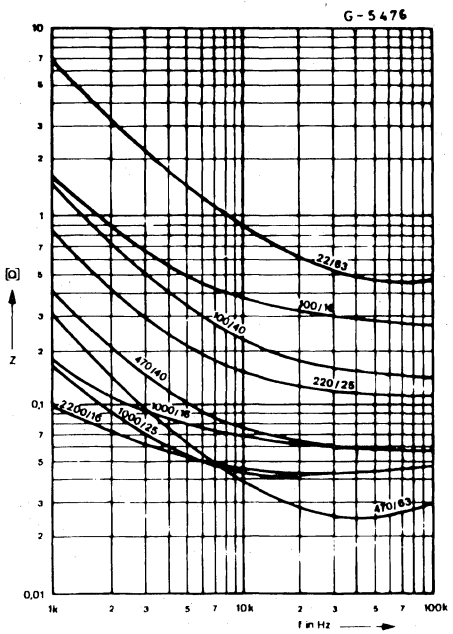
Therefore, a correct dimensioning requires a saturation current above the maximum value of I_{2L}, the current limit threshold.

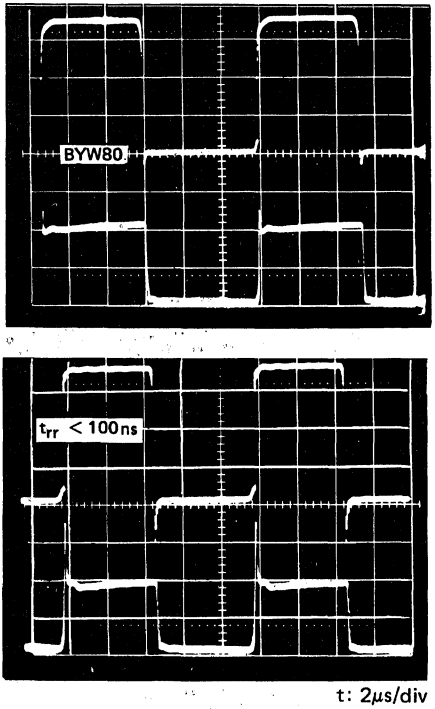
To achieve high saturation with ferrite cores an air gap between the two core halves must be provided ; the air gap causes a leakage flux which is radiated in the surrounding space. To better limit this phenomenon "pot cores" may be used, whose geometry is such to better limit the flux radiated to the outside.

Using toroidal cores, for instance of Magnetic 58930-A2 moly-permalloy kind, both the requirements of high saturation and low leakage flux are satisfied. The saturation is softer that the saturation shown by the ferrite materials. The air gap is not concentrated in one area, but is finely distributed along the whole core ; this gives the low leakage flux value.

Careful selection of the external components therefore allows the realization of a power supply system whose benefits are significant when compared to a system with the same performance but realized with the linear technique.

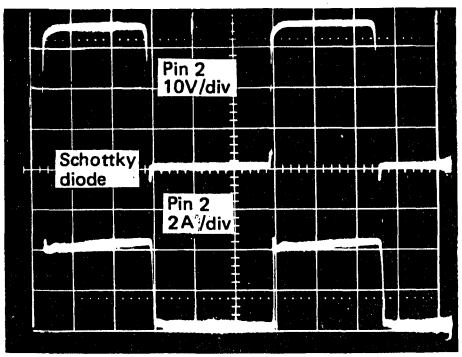
Figure 24 : Typical Impedance/Frequency curves for EKR Capacitors.





t: 2μs/div

Figure 25 : Oscilloscope Photographs Showing the Waveform obtained with Diodes having Different t_{rr} Values.



t : 2μs/div

LOW COST APPLICATION AND PREREGULATOR

Fig. 26 shows the low cost application of a 4A and V_o = 5.1V power supply. A minimum amount of essential external components is required, which are necessary for correct operation. It is impossible to save other components, specially the soft-start capacitor. Without soft-start, the system cannot reach the steady state and there is also a serious risk of damaging the device.

This application is very well suited not only as a low-cost power supply, but also as pre-regulator for post-regulators distributed in different circuit points, or even on different boards (fig. 27). The post-regulators may be selected among the low-drop types, like L4805 and L387 for example, still obtaining a high efficiency, combined with an excellent regulation. The use of L387 device allows us to use also the reset function, useful to power a microprocessor.

SWITCHING vs LINEAR

Switching regulators are more efficient than linear types so the transformer and heatsink can be smaller and cheaper. But how much can you gain ?

We can estimate the savings by comparing equivalent linear and switching regulators. For example, suppose that we want a 4 A/5 V supply.

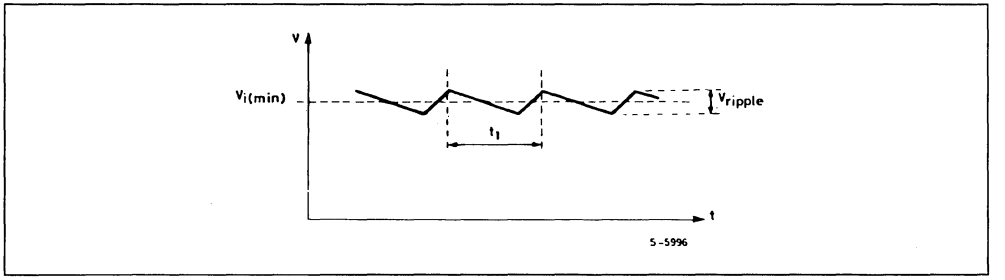
Linear

For a good linear regulator the minimum dropout will be at least 5V at 4A. The minimum input voltage is given by :

$$V_{i\,min} = V_o + V_{drop} + \frac{1}{2} V_{ripple}$$

where :

$$V_{ripple} \cong \frac{I_o\, t_1}{C} = \frac{4 \times 8 \times 10^{-3}}{10 \times 10^{-3}} = 3.2\ V$$



(a good approximation is 8ms for t_1 at mains frequency of 50Hz and 10.000µF for C, the filter capacitor after the bridge). Therefore $V_{imin} \cong 1.6V$. Since operation must be guaranteed even when the mains voltage falls 20%, the nominal voltage on load at the terminals of the regulator must be :

$$V_{nom} = \frac{V_{i\,min}}{0.8} = \frac{10.6}{0.8} = 13.25V$$

To allow even a small margin we have to choose :

$V_{nom} = 14V$

The power that the series element must dissipate is therefore :

$P_d = (V_{nom}\ V_o)\ I_o = 36W$

and a heatsink will be necessary with a thermal resistance of :

$R_{th\ heats.} = 0.8°C/W$

and the transformer must supply a power of :

$P_{diss} = 14 \times 4 = 56W$

It must therefore be dimensioned for :

$$PD = \frac{56}{0.9} = 62VA$$

Switching (L296)

Assuming the same nominal voltage (14V), the L296 data sheet indicates that the power dissipated in this case is only 7W. And this power is dissipated in two elements ; the L296 itself and the recirculation diode.

It follows that the transformer must be roughly 30VA and the heatsink thermal resistance about 11°C/W.

	Linear	Switching
Transformer	62 VA	30 VA
Heatsink	0.8 °C/W	11 °C/W

This comparison shows that the L296 switching regulator allows a saving of roughly 50% on the cost of the transformer and an impressive 80-90% on the cost of the heatsink. Considering also the extra functions integrated by the L296 the total cost of active and passive components is roughly the same for both types.

Finally, it is important to note that a lower power dissipation means that the ambient temperature in the regulator enclosure can be lower - particularly when the circuit is enclosed in a box - with all the advantages cooler operation brings.

If for some reason it is necessary to use higher supply voltages the switching technique, and hence the L296, becomes even more advantageous.

Figure 26 : A Minimal Component Count 5.1V / 4A Supply.

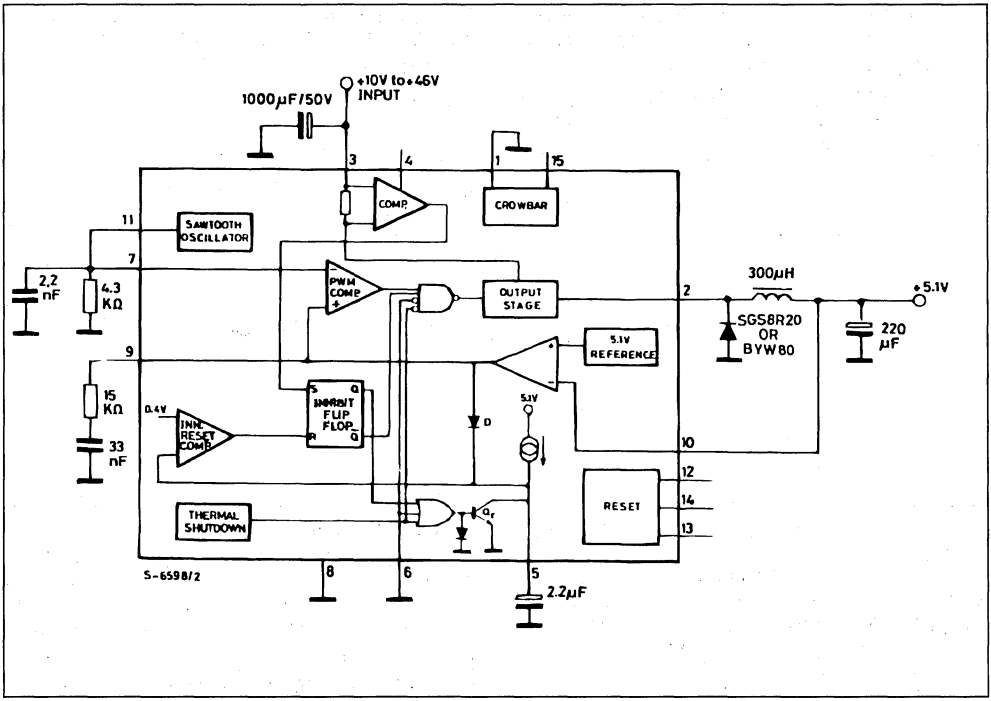
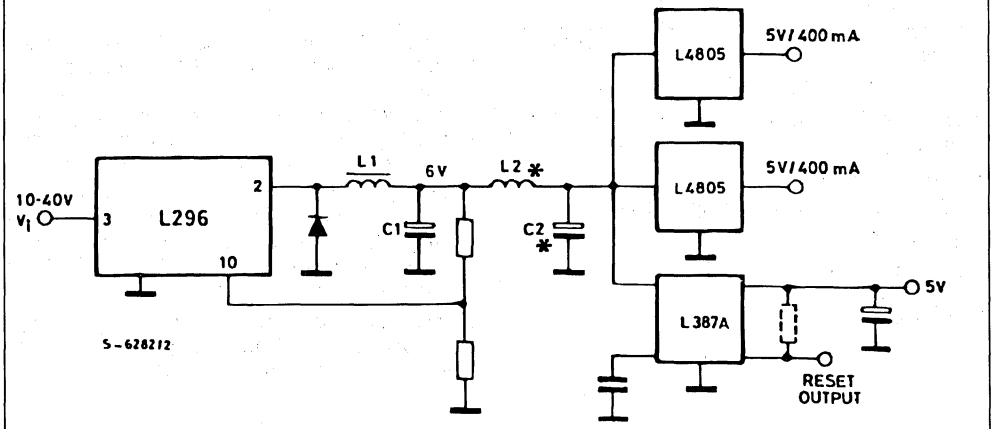


Figure 27 : The L296 may also be used as a preregulator in distributed supply systems.



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

POWER SUPPLY COMPLETE WITH TRANSFORMER

Fig. 28 shows a power supply complete of transformer, bridge and filter, with regulation on the output voltage from 5.1V to 15V.

As already stated above, the output capacitors have to show some speciale features, like low ESR and high current ripple, to obtain low voltage ripple values and high reliability. The input filter capacitors must not be neglected because they have to show excellent features, too, having to supply a pulsed current, required by the device at the switching frequency. The current ripple is rather high, greater than the load current. For this application, two parallel connected 3300µF/50V EYF (ROE) capacitors have been used.

POWER SUPPLY WITH MAINS SWITCHING PREREGULATOR

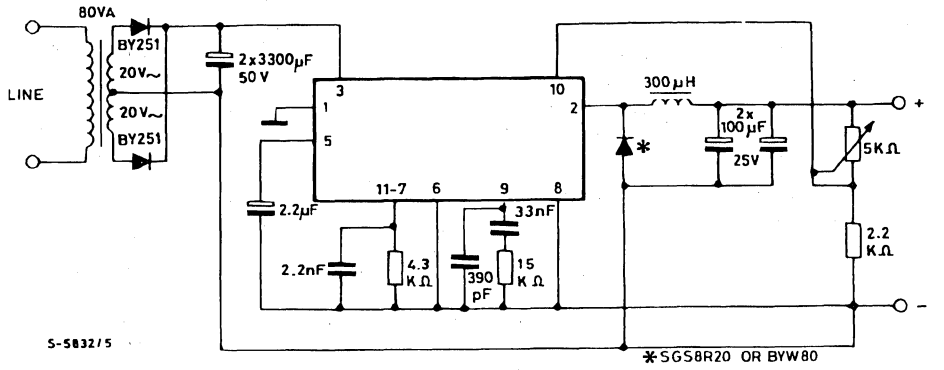
When it is desirable to eliminate the 50/60Hz transformer - in portable or volume-limited equipment-a mains preregulator can be added to reduce the input voltage to a level acceptable for the L296.

In this case the pre-regulator circuit is connected to the primary of the transformer which now operates at the switching frequency and is therefore smaller and lighter.

Using a UC3840 which includes the feed-forward function it is possible to compensate mains variation within wide limits. The secondary voltage is therefore only affected by load variations. Using one or more L296s as postregulators, feedback to the primary is no longer necessary, reduces the complexity and cost of the transformer which needs only a single secondary winding.

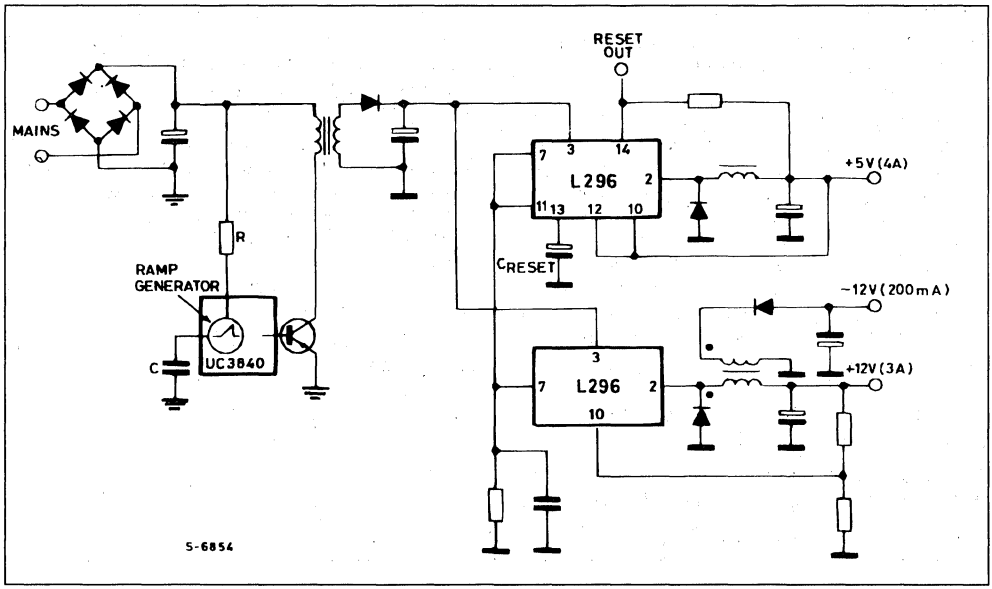
Fig. 28A shows a multi-output supply with a mains preregulator.

Figure 28 : A Typical Variable Supply showing the Mains Transformer.



V_o = 5.1 to 15V
I_o = 4A max. (min. load current = 100mA)
ripple ≤ 20mV
load regulation (1A to 4A) = 10mV (V_o = 5.1V)
line regulation (200V ± 15% and to I_o = 3A) = 15mV (V_o = 5.1V)

Figure 28A : A Multiple Output Supply using a Switching Preregulator rather than a Mains Transformer.



POWER SUPPLY WITH 0 - 30V ADJUSTABLE VOLTAGE

When output voltages lower than 5V are required, the circuit shown in fig. 29 may be used.

Calibration is performed by grounding the P1 slider. Acting on P2, the current which flows through the 10kΩ resistor is fixed at approximately 2.5mA to obtain an output voltage of 30V. The equivalent circuit is shown in fig. 30.

Acting now on the slider of P1, the current flowing through the divider may be varied. The new equivalent circuit is shown in fig. 31.

Reducing the current flowing, also the voltage drop across the 10kΩ resistance is reduced, together with V_o. When the current reaches zero, it follows that $V_o = V_{REF}$. When the voltage on the slider of P1 exceeds V_{REF}, the current start to flow in opposite direction and V_o begins to decrease below 5V.

When $I_1 \times 10k\Omega = V_{REF}$ it follows that $V_o = 0$.

DUAL OUTPUT REGULATOR

The application shown in fig. 32 is specially interesting because it provides two output voltages. The first voltage, the main one, is directly controlled by the feedback circuit. The second voltage is obtained through an auxiliary winding.

It often happens, when microprocessors, logic devices etc., have to be power supplied, that a main 5V output and an auxiliary + 12V or – 12V output are required, the latter with lower current requirements (100 ÷ 200mA) and a stabilization level not excessively high. As the auxiliary power supply is obtained through a completely separated winding, it is possible to obtain either a positive or negative voltage (compared to the main voltage or also a completely isolated voltage. With V_i variable between 20V and 40V, V_o = 5.1V and I_o = 2.5A, the auxiliary - 12V/0.2A voltage is within a ± 2% tolerance.

Figure 29 : Variable 0–30V supply illustrating how output voltages below 5.1V are obtained.

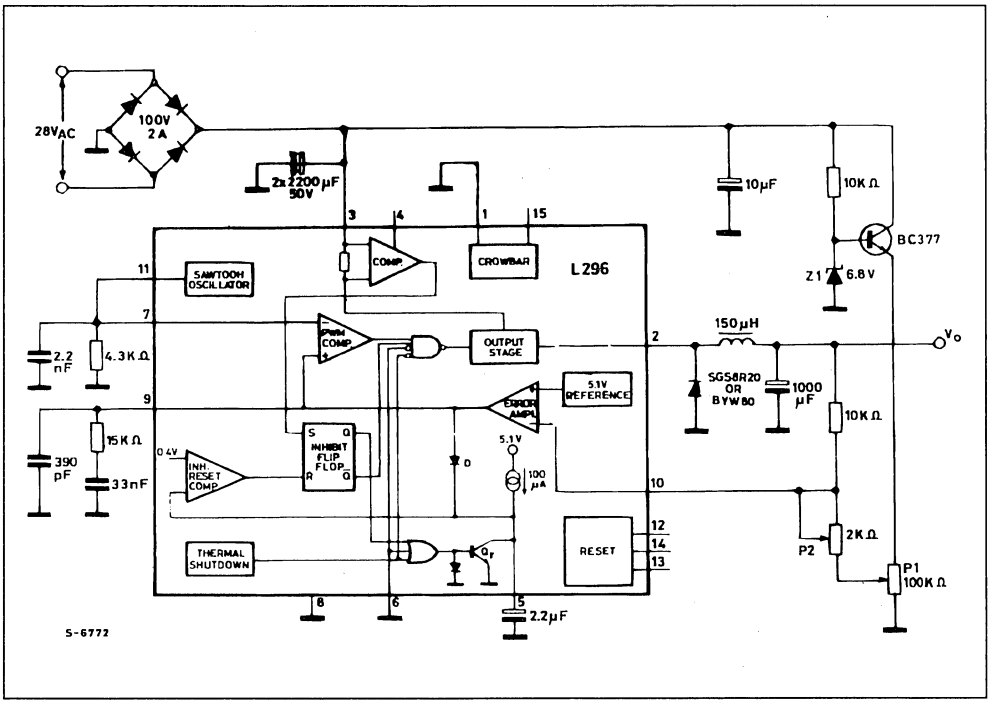


Figure 30 : When setting up the figure 29 circuit the slider of P1 is grounded, giving the equivalent circuit shown here, and P2 adjusted to give an output voltage of 30V.

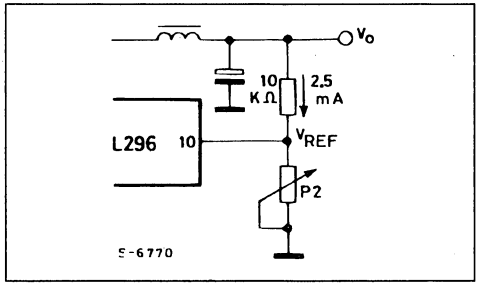


Figure 31 : Partial Schematic showing Output Voltage Adjustment of Figure 29.

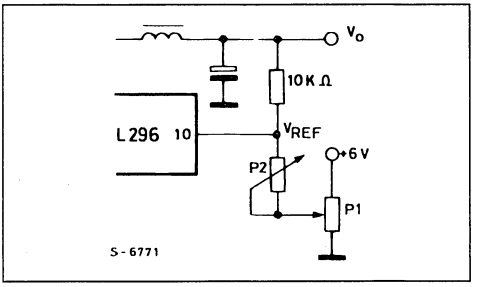
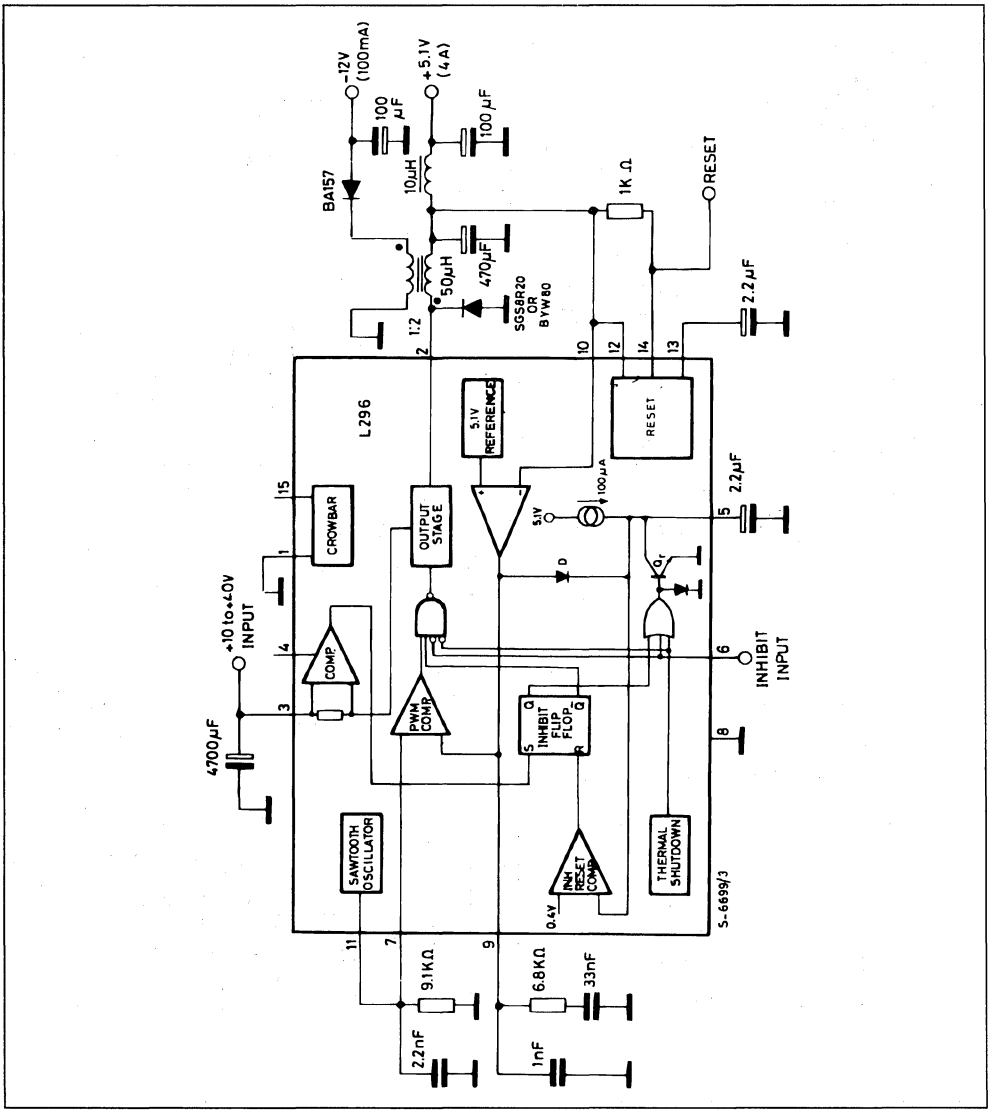


Figure 32 : Dual output regulator showing how an additional winding can be added to the inductor to generate a secondary output.



PERSONAL COMPUTER POWER SUPPLY

Using two mutually synchronized devices it is possible to obtain a four output power supply suitable for power a microprocessor system.

V_{01} = 5.1V/4A

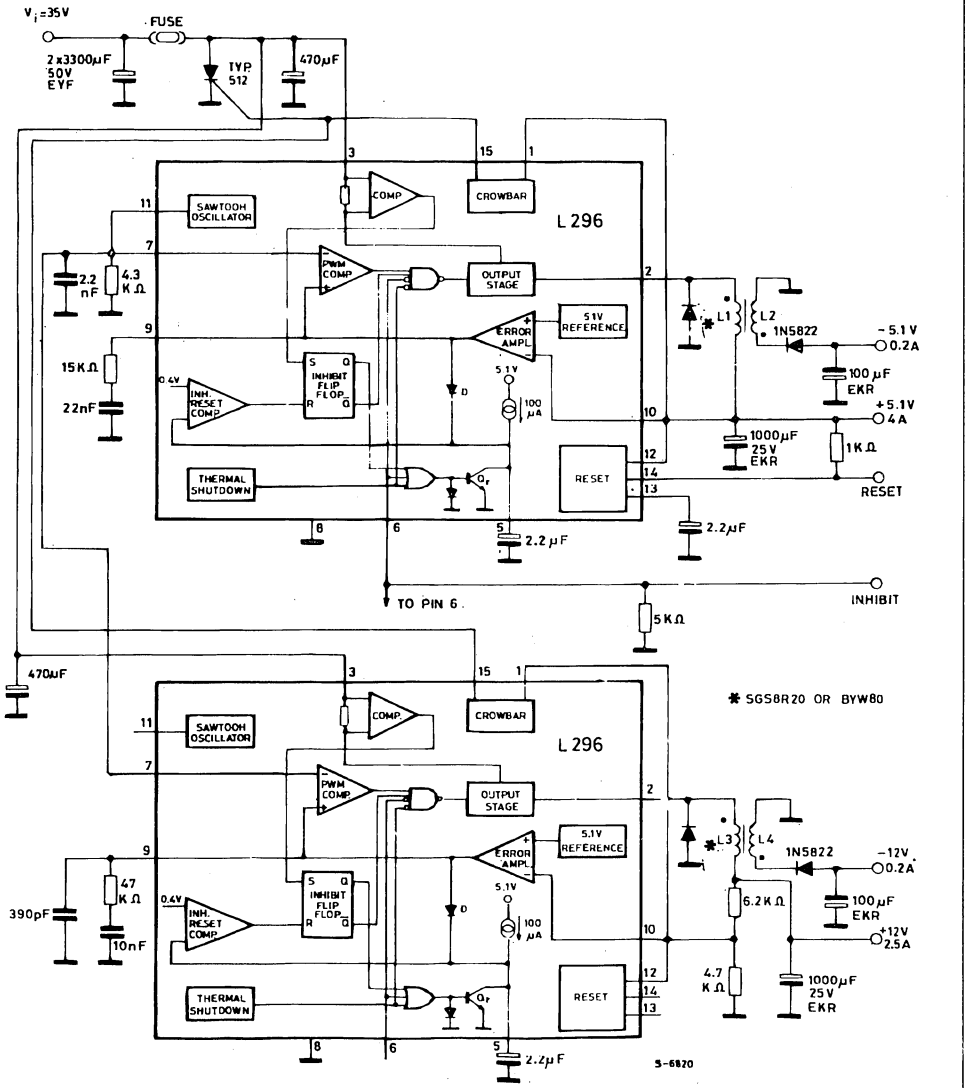
V_{02} = 12V/2.5A (up o 4A)

V_{03} = – 5V/0.2A

V_{04} = – 12V/0.2A

The schematic diagram is shown in fig. 33. The 5V output is also provided with the reset function, that is available also for the 12V output.

Figure 33 : Microcomputer Supply with 5V, – 5V, 12V and – 12V Outputs.



The feedback is direct, no other external component is used and no calibration is therefore required. An output is obtained with the accuracy of the reference voltage (± 2%). For the 12 V output, by using a resistive divider with 1 % resistance an output is obtained whose spread is within ± 4%.

The two devices are mutually synchronized not to give rise to intermodulation which could generate unpleasant noise and, at the same time, a further component saving is achieved.

The crowbar function is implemented on both 5V and 12V outputs, using a single SCR connected to the input. The latter, by discharging to ground the electrolytic filter capacitors, blows the fuse connected in series with the devices power supply. In this way, should a faulty be present on either of the main outputs, the supply is switched off for whole system.

To inhibit both the devices with a single input signal, it is possible to connect the two inhibit inputs (pin 6) together ; the 5KΩ resistance is used when the inhibit input is left open. If this input is not used it must be grounded.

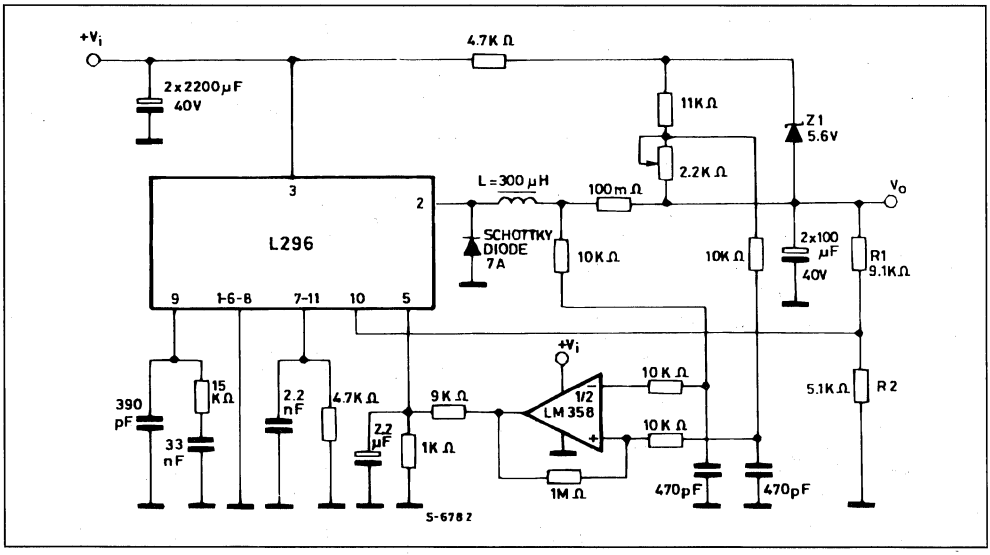
As may be noted in the diagram, to obtain the two auxiliary voltages is very simple and cost-effective.

It is suggested that the diodes are fast types (trr < 50nsec) ; should slower diodes be required some more turns have to be added to the auxiliary winding.

BATTERY CHARGER

When the device has to be used as current generator it is necessary to avoid the internal current limiter is operated fig. 34 shows the circuit realizing constant current limitation. In this way it is possible to obtain a 6V, 12V and 24V battery charger. For each of these voltages a max. current of 4A is available, which is large enough for batteries up to 40-45Ah (for 12V type). With reference to the electric diagram through the 2KΩ potentiometer the max output current is set, while through the R_1 – R_2 output divider the voltage is set. (R_1 may be replaced by either a potentiometer or a 3 position switch, to directly obtain the three 6V, 12V and 24V voltages).

Figure 34 : Battery charger circuit illustrating how the device is used to regulate the output current.



HIGHER INPUT VOLTAGE

Since a maximum input voltage of 46V (operating value) may be applied to the device the diagram shown in fig. 35 may be used when it is necessary to exceed this limit.

This system is particularly useful when operating at low output voltages. In this case a mean current I_{IDC} which has a low value when compared to I_o is obtained. In fact, since $V_o = V_i (T_{ON}/T)$ and $V_o I_o = V_i I_{IDC}$ (assuming the device has an ideal efficiency), it follows that $I_{IDC} = I_o (T_{ON}/T)$.

Assuming to be :

V_o = 5V I_o = 4A and $V_3 \approx$ 37V

it follows that :

$$T_{ON} / T = V_o / V_i = \frac{5}{37} = 0.135$$

I_{IDC} = 4 x 0.135 = 0.54A.

With input voltage 50V and I_o = 4A, the external transistor dissipates about 7W. High good efficiency is still achieved, around 74% ; in the real case, considering also the device losses, an efficiency around 62% is achieved.

During output short circuits the external transistor is not overloaded because in this condition I_{IDC} reduces to values lower than 100mA. It is not possible to realize this application with series post-regulator because the efficiency would be unacceptably low.

MOTOR CONTROL

The L296 is also suitable for use in motor controls applications. Fig. 36 shows how to use the device to drive a motor with a maximum power of about 100W and provided with a tachometer generator for a good speed control.

Figure 35 : The maximum input voltage can be raised above 46V by adding a transistor as shown here.

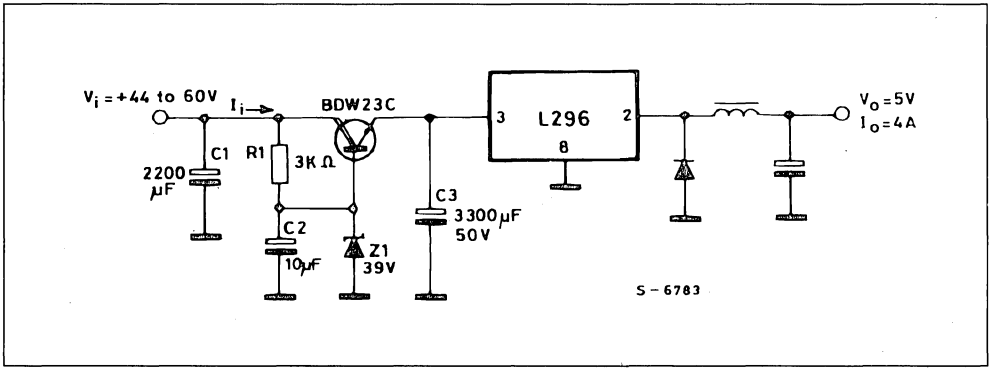
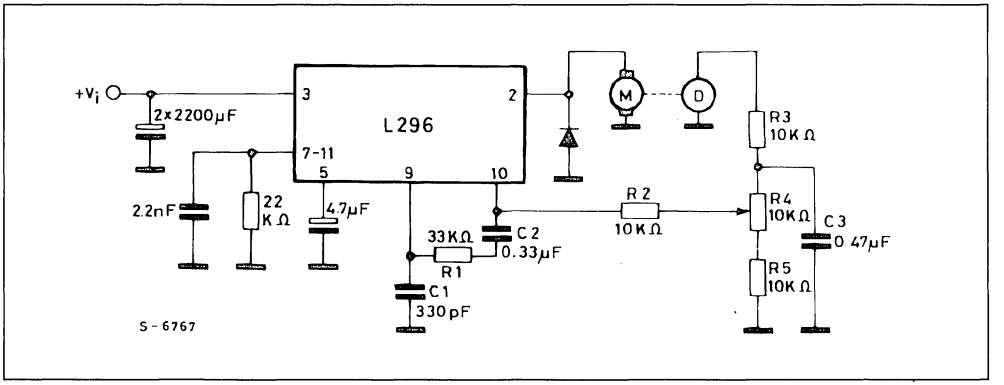


Figure 36 : With a tacho dynamo supplying feedback the L296 can be used as a motor speed controller.



HIGHER CURRENT REGULATORS

It is possible to increase the output current to the load above 4A through the use of an external power transistor. Fig. 37 shows a suitable circuit. The frequency is around 40kHz to prevent the device from loosing excessive power due to switching on the external power.

The circuits shown in fig. 38 and fig. 39 show how current limitation may be realized in two different ways : through a sensing resistor connected in series with the collector of the external power transistor or through a current transformer.

In the first case, the sensing resistor is a low value resistor able to withstand the maximum load current required. The V_{CE} of the power transistor is higher than its V_{CEsat} ; when the resistor is connected in series to the collector V_{CE} is reduced ; consequently since the overall dissipated power is constant, the power dissipated by the sensing resistor is subtracted from that dissipated by the power transistor. The values indicated in figs. 38 and 39 realize adjustable current limitation for load currents around 10A.

Figure 37 : The output current may be increased by adding a power transistor as shown in this circuit.

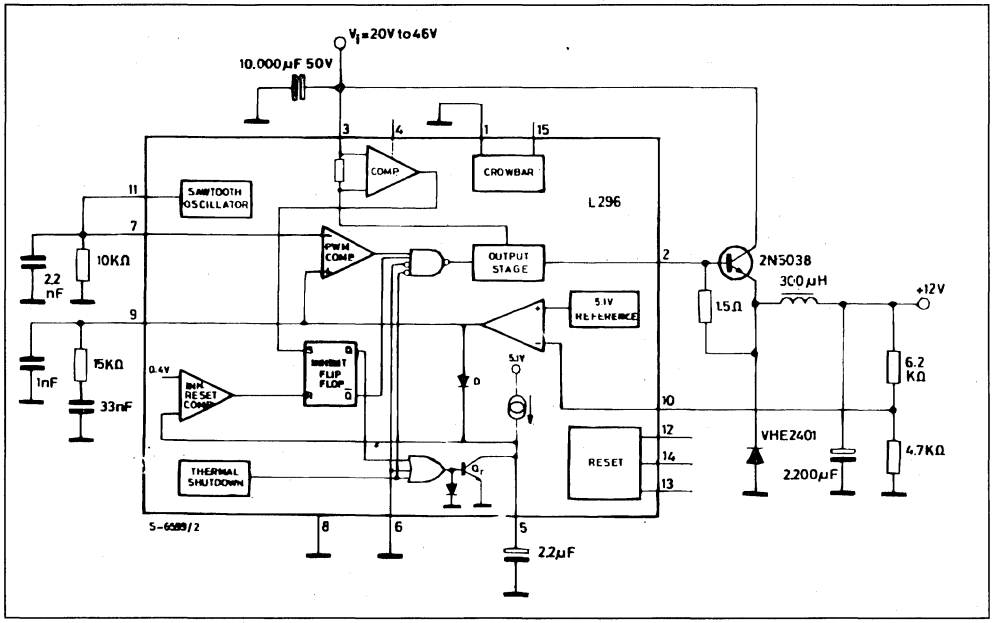


Figure 38 : This circuit shows how current limiting for the external transistor is obtained with a sensing resistor.

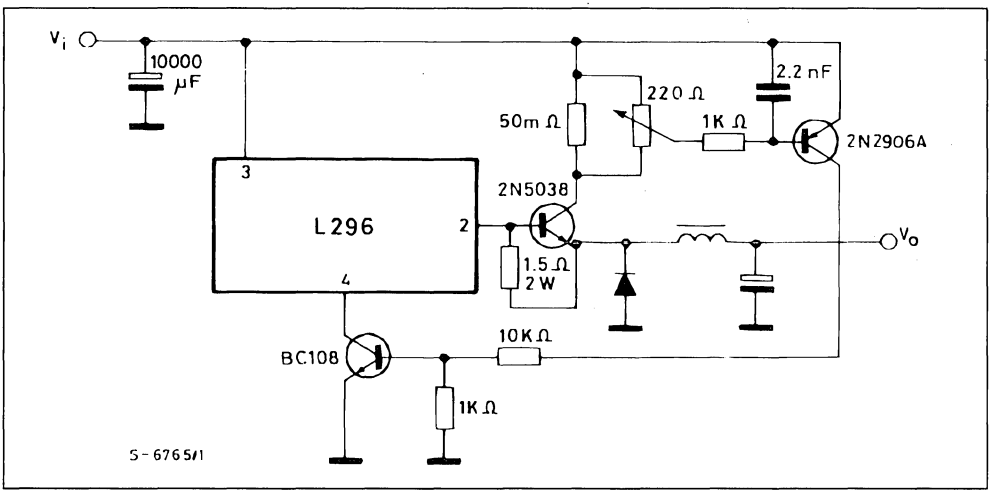
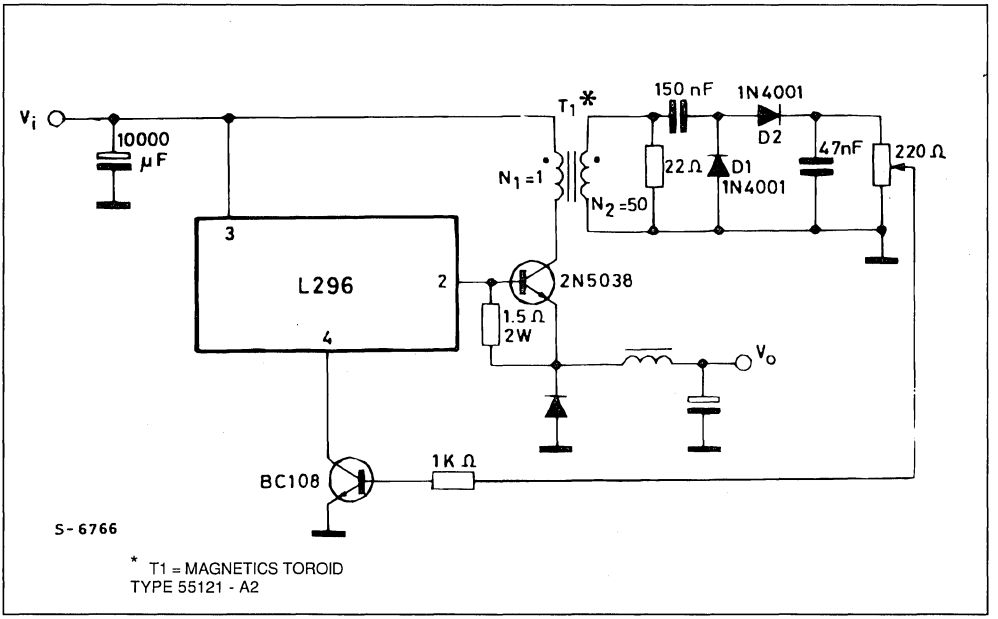


Figure 39 : A small transformer is used in this example for current limiting.



STEP-UP CONVERTER

With the L296 it is also easy to realize a step-up converter, by using a MOS power transistor. Fig. 40 shows the electric diagram of the step-up converter. The frequency is 100kHz, operation is in discontinuous mode and the device internal current limiter is used. Therefore no other external protection is required.

The input voltage could be a 12V car battery, from which an output voltage of 35V may be obtained. Lower output voltage of 35V may be obtained. Lower output voltage values may be obtained by reducing the value of R_7.

DESCRIPTION OF OPERATION

Fig. 41 shows the diagram of the circuit realizing the step-up configuration.

When the transistor Q1 is ON, the inductance L charges itself with a current given by :

$$i_L = \frac{V_i}{L} t$$

The peak current in the coil is :

$$I_{peak} = \frac{V_i}{L} T_{ON}$$

Figure 40 : A Step-up Converter using a Power MOS Transistor.

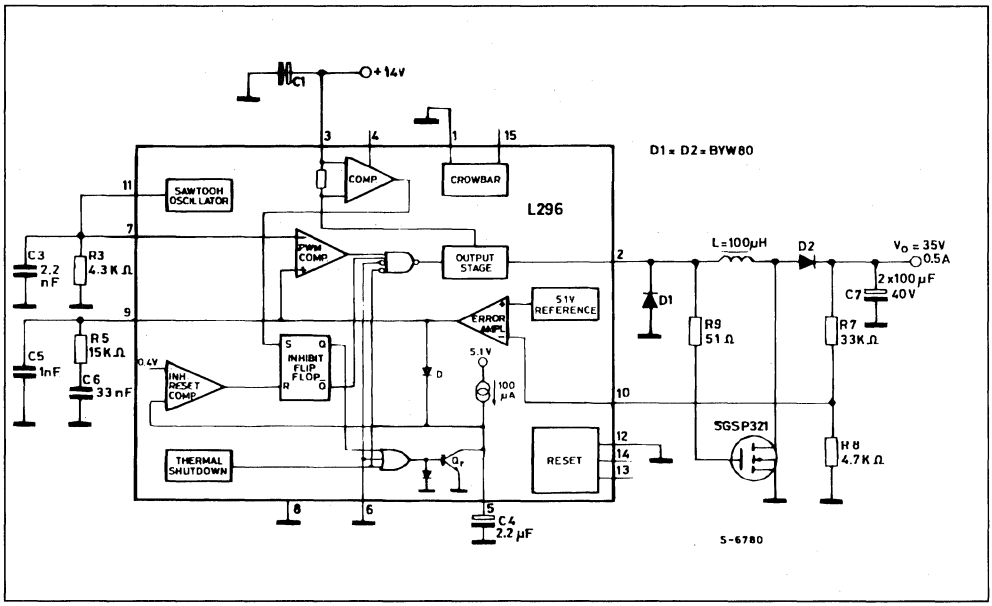
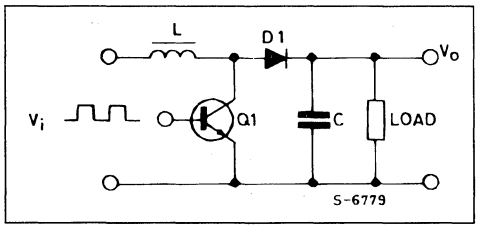


Figure 41 : Basic Schematic for Step-up Configurations.



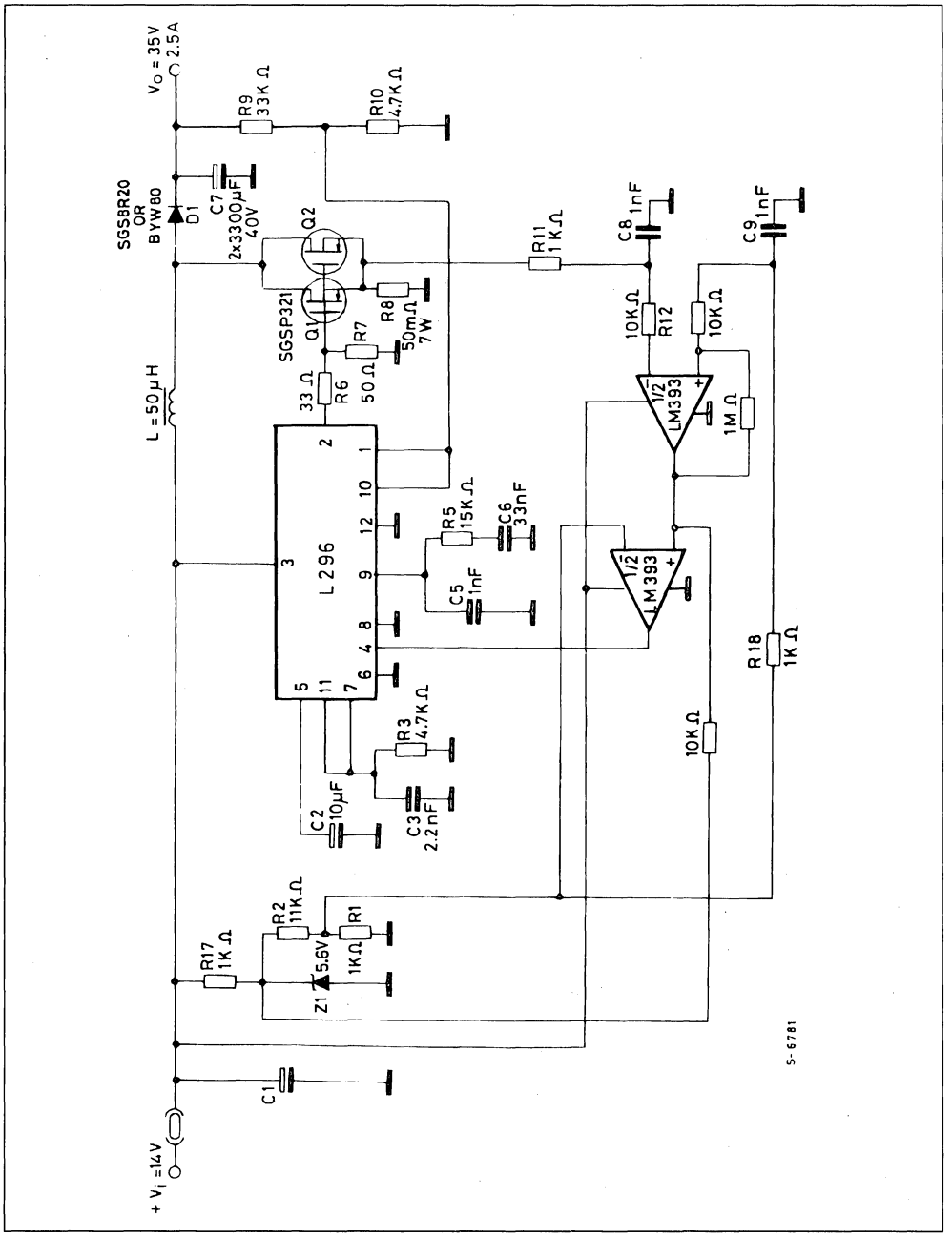
In this configuration, unlike the step-down configuration, the peak current is not strictly related to the load current. The energy stored in the coil is successively discharged across the load when the transistor switches OFF. To calculate the I_o load current, the following procedure may be used :

$$\frac{1}{2} L I^2_{peak} = V_o I_o T$$

$$I_o = \frac{L I2_{peak}}{2 V_o T} = \frac{V_i^2 T_{ON}^2}{2 L V_o T}$$

For a greater output power to be available, the internal limitation must be replaced by an external circuit to protect the external power devices and to limit the current peak to a convenient value. A dual comparator (LM393) with hysteresis is used to avoid uncertainties when the current limitation operates. The electric diagram is shown in fig. 42.

Figure 42 : High power step-up converter showing how the current limiting function is realized externally.



LAYOUT CONSIDERATIONS

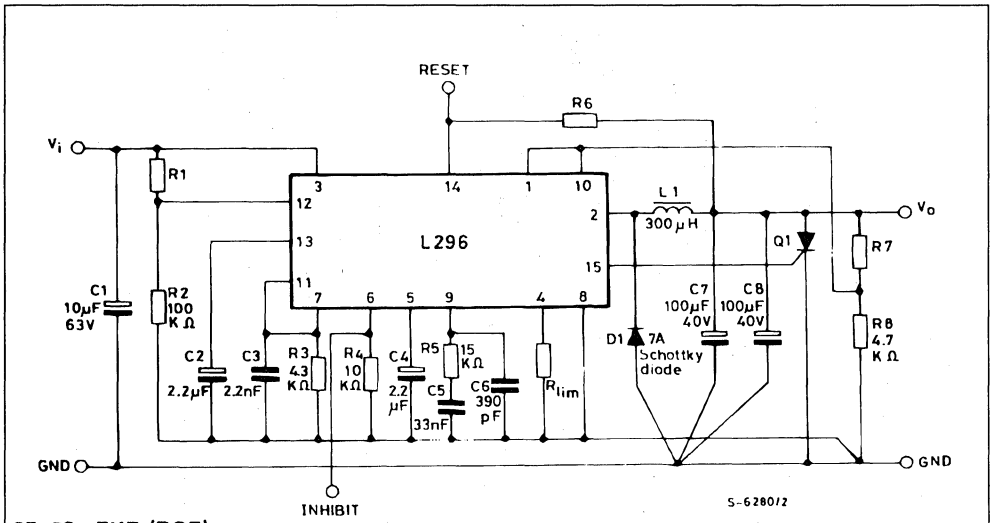
Both for linear and switching power supplies when the current exceeds 1A a careful layout becomes important to achieve a good regulation. The problem becomes more evident when designing switching regulators in which pulsed currents are over imposed on dc currents. In drawing the layout, therefore, special care has to be taken to separate ground paths for signal currents and ground paths for load currents, which generally show a much higher value.

When operating at high frequencies the path length becomes extremely important. The paths introduce distributed inductances, producing ringing phenomena and radiating noise into the surrounding space.

The recirculation diode must be connected close to pin 2, to avoid giving rise to dangerous extra negative voltages, due to the distributed inductance.

Fig. 43 and fig. 44 respectively show the electric diagram and the associated layout which has been realized taking these problems into account. Greater care must be taken to follow these rules when two or more mutually synchronized devices are used.

Figure 43 : Typical application circuit showing how the signal and power grounds are connected.



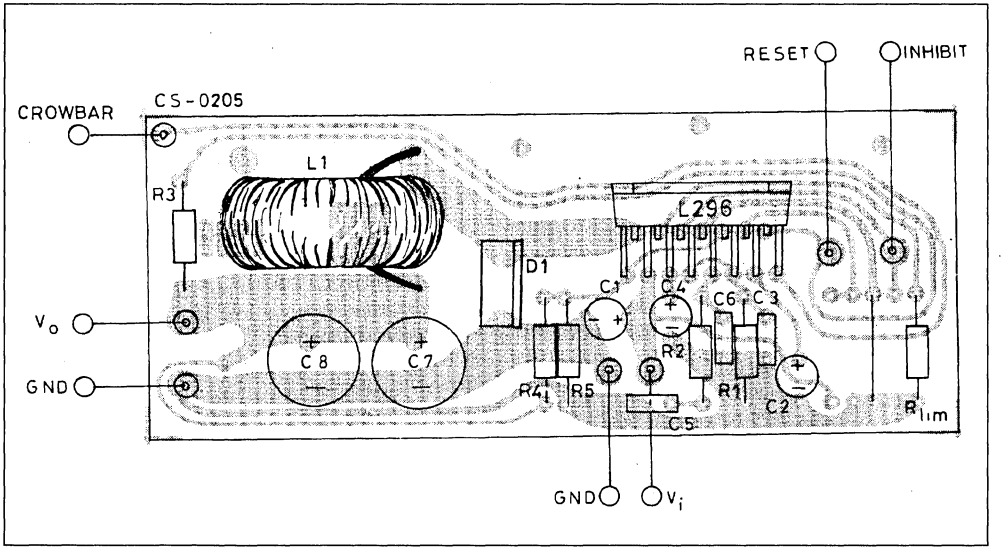
C7, C8 : EKR (ROE)

SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	
Thomson GUP 20 x 16 x 7	65	0.8 mm.	1 mm.
Siemens EC 35/17/10 (B6633 & - G0500 - x 127)	40	2 x 0.8 mm.	
VOGT 250 µH Toroidal Coil, Part Number 5730501800			

Resistor Value for Standard Output Voltages		
V_O	R_8	R_7
12 V	4.7 kΩ	6.2 kΩ
15 V	4.7 kΩ	9.1 kΩ
18 V	4.7 kΩ	12 kΩ
24 V	4.7 kΩ	18 kΩ

Figure 44 : A Suitable PCB Layout for the Figure 43 Circuit realized in Accordance with the Suggestions in the Text (1 : 1 scale).



HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reacing values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150°C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150°C for long periods or of more than 170°C for short periods. In any case the temperature accelerates the ageing process and therefore influences the device life ; an increase of 10°C can halve the device life. A well designed heatsink should keep the junction temperature between 90°C and 110°C. Fig. 45 shows the structure of a power device. As demonstrated in thermo-dynamics, a thermal circuit can be considered to be an electrical circuit where R_1, R_2 represent the thermal resistance of the elements (expressed in °C/W) (see fig. 46).

C1, C2 are the thermal capacitance (expressed in °C/W)
I is the dissipated power
V is the temperature difference with respect to the reference (ground)

This circuit can be simplified as shown in fig. 47, where :

C_c is the thermal capacitance of the die plus that of the tab.
C_h is the thermal capacitance of the heatsink
R_{jc} is the junction case thermal resistance
R_h is the heatsink thermal resistance

Figure 45.

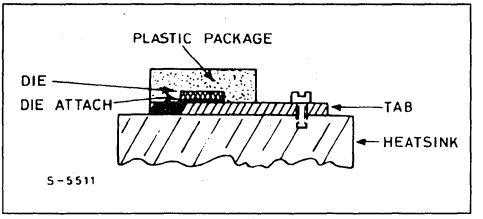


Figure 46.

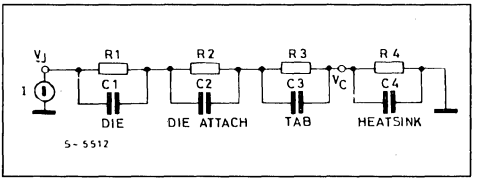
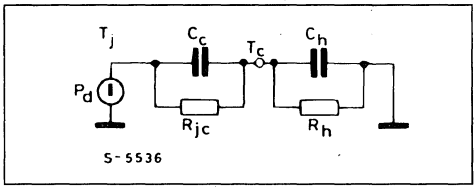
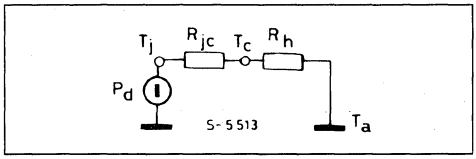


Figure 47.



But since the aim of this section is not that of studing the transistors, the circuit can be further reduced as shown in figure 48.

Figure 48.



If we now consider the ground potential as ambient temperature, we have :

$$T_j = T_a + (R_{jc} + R_h)\, P_d \qquad a)$$

$$R_h = \frac{T_j - T_a - R_{jc}\, P_d}{Pd} \qquad b)$$

$$T_c = T_a + R_h\, Pd \qquad c)$$

Thermal contact resistance depends on various factors such as the mounting, contact area and planarity of the heatsink. With no material between the device and heatsink the thermal resistance is around 0.5°C/W ; with silicone grease roughly 0.3°C/W and with silicone grease plus a mica insulator about 0.4°C/W. See fig. 49. In application where one external transistor is used together, the dissipated power must be calculated for each component. The various junction temperature can be calculated by solving the circuit shown in fig. 50. This applies if the dissipating elements are fairly close with respect to the dissipator dimensions, otherwise the dissipator can no longer be considered as a concentrated constant and the calculation becomes difficult. This concept is better explained by the graph in fig. 51 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of heatsink and the same dissipated power. The graph in fig. 51 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides. The temperature jump will depend on the total dissipated power and on the devices geometrical positions. We want to show that there exists an optimal position between the two devices :

$$d = \frac{1}{2} \cdot \text{side of the plate}$$

Figure 49.

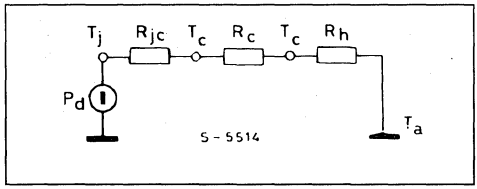


Figure 50.

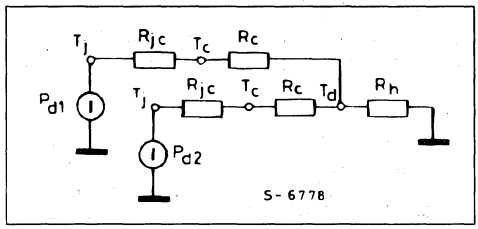


Fig. 52 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4). This graph may be useful in application with two L296 synchronized.

Figure 51.

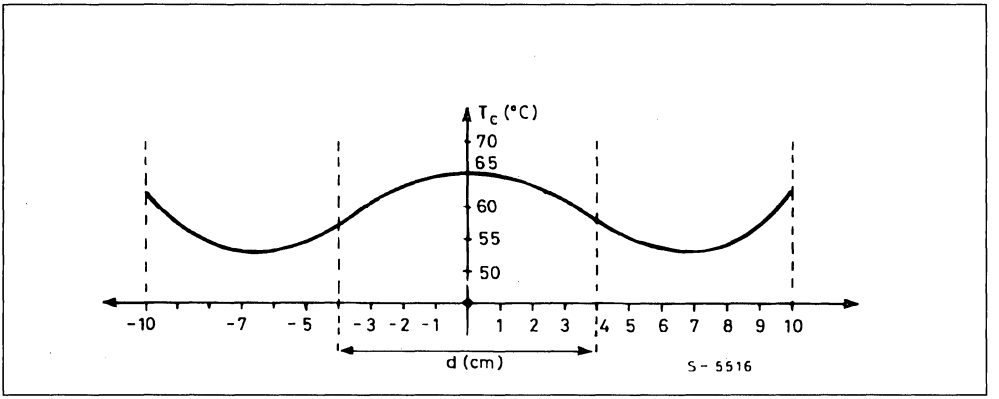
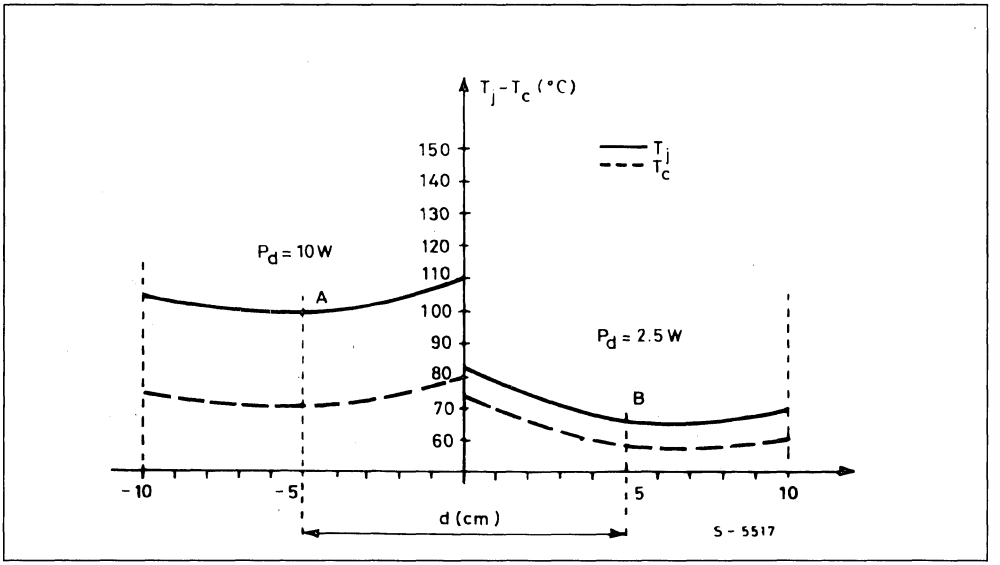


Figure 52.



APPENDIX A

CALCULATING SYSTEM STABILITY

This section is intended to help the designer in the calculation of the stability of the whole system.

Figure A1 shows the entire control system of the switching regulator.

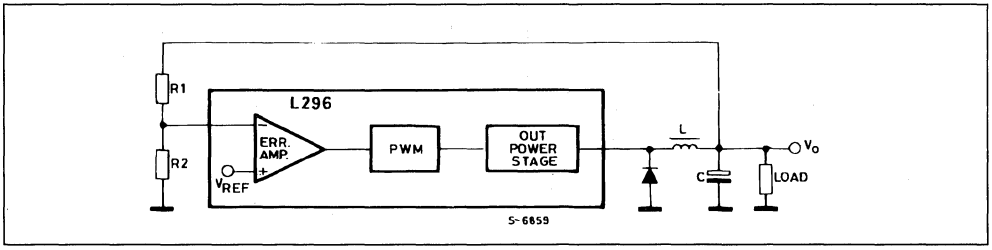
The problem which arises immediately is the transfer function of the PWM block and output stage, which is non-linear. If this function can be considered linear the analysis is greatly simplified.

Since the circuit operates at a constant frequency and the internal logic is fairly fast, the error introduced by assuming that this function is linear is minimized. Factors which could contribute to the non-linearity are an excessive delay in the output power transistor, ringing and parasitic oscillations generated in the power stage and non-linearity introduced by magnetic part.

In the case of the L296, in which the power transistor is internal and driven by well-controlled and efficient logic, the contribution to non-linearity is further reduced.

For the assumption of linearity to be valid the cut-off frequency of the LC filter must be much lower than the switching frequency. In fact, switching operation introduces singularities (poles) at roughly half the switching frequency. Consequently, as long as the LC filter is still dominant, its cut-off frequency must be at least an order of magnitude lower than the switching frequency. This condition is not, however, difficult to respect. The characteristics of LC filter affect the output voltage waveforms ; is generally much less than an order of magnitude below the switching frequency.

Figure A1 : The Control Loop of the Switching Regulator.



GAIN OF THE PWM BLOCK AND OUTPUT STAGE

The equation which links V_o to V_i is :

$$V_o = V_i \frac{T_{ON}}{T}$$

A variation ΔT_{ON} in the conduction time of the switching transistor causes a corresponding variation in the output voltage , ΔV_O, giving :

$$\frac{\Delta V_o}{\Delta T_{ON}} = \frac{V_i}{T}$$

Indicating with V_r the output voltage of the error amplifier, and with V_{ct} the amplitude of the ramp (the difference between the maximum and minimum values), T_{ON} is zero when V_r is at the minimum value and equal to T when V_r is at a maximum. Consequently :

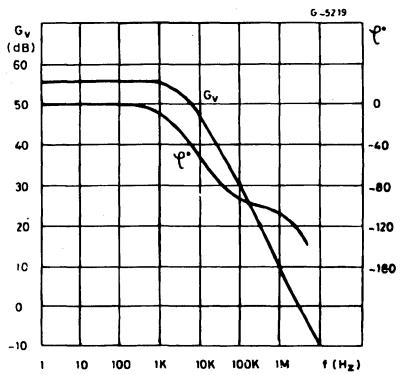
$$\frac{\Delta T_{ON}}{\Delta V_r} = \frac{T}{V_{ct}}$$

The gain is given by :

$$\frac{\Delta V_o}{\Delta V_r} = \frac{V_i}{V_{ct}}$$

Since V_{ct} is absolutely constant the gain of the PWM block is directly proportional to the supply voltage V_i.

Figure A2 : Open Loop Frequency and Phase Response of Error Amplifier.



The error amplifier is a transconductance amplifier (it transforms a voltage variation at the input into a current variation at the output). It is used in open loop configuration inside the main control loop and its gain and frequency response are determined by a compensation network connected between its output and ground.

In the application a series RC network is recommended which gives high system gain at low frequency - to ensure good precision and mains ripple rejection and a lower gain at high frequencies to ensure stability of the system. Figure A2 shows the gain and phase curves of the uncompensated error amplifier.

The amplifier has one pole at about 7kHz and a phase shift which reaches about – 90° at frequencies around 1MHz.

The introduction of a series network R_C C_C between the output and ground modifies the circuit as shown in figure A3.

Figure A4 shows the gain and phase curves of the compensated error amplifier.

Figure A3 : Compensation Network of the Error Amplifier.

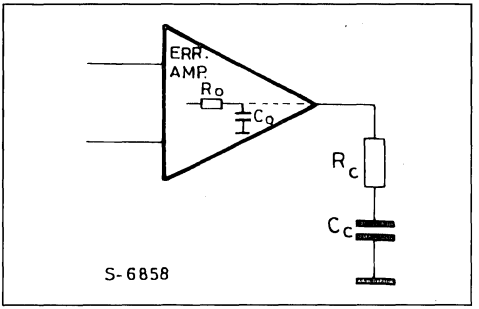
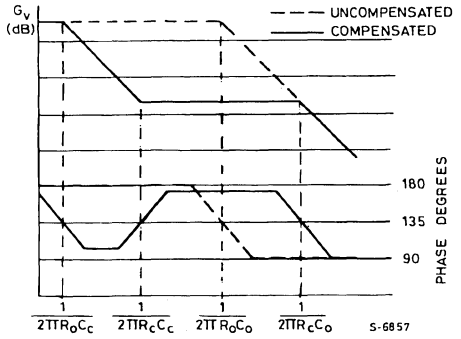


Figure A4 : Bode Plot Showing Gain and Phase of Compensated Error Amplifier.



CALCULATING THE STABILITY

For the stability calculation refer to the block diagram shown in figure A5.

The transfer functions of the various blocks are rewritten as follows.

The simplified transfer function of the compensated error amplifier is :

$$G_{EA} = g_m Z_c = \frac{1 + s R_C C_C}{s C_C} \quad (gm = \frac{1}{2500})$$

The DC gain must be considered equal to :

$A_o = g_m R_o$

PWM block and output stage :

$$G_{PWM} = \frac{V_i}{V_{ct}}$$

LC FILTER :

$$G_{LC} = \frac{1 + s C \cdot ESR}{s^2 LC + s C ESR + 1}$$

where ESR is the equivalent series resistance of the output capacitor which introduces a zero at high frequencies, indispensable for system stability. Such a filter introduces two poles at the angular frequency.

$$\omega_o = \frac{1}{\sqrt{LC}}$$

Refer to the literature for a more detailed analysis.

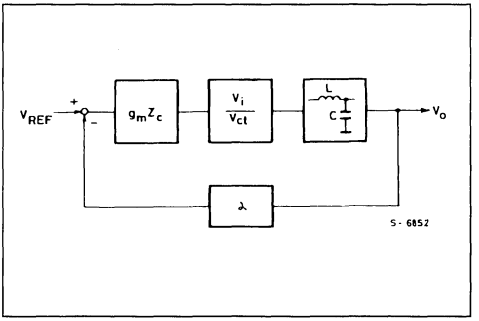
Feedback : consists of the block labelled α

$\alpha = 1$ when $V_o = V_{REF}$ (and therefore $V_o = 5.1V$)

and

$$\alpha = \frac{R_2}{R_1 + R_2} \quad \text{when } V_o > V_{REF}$$

Figure A5 : Block Diagram Used in Stability Calculation.



To analyse the stability we will use a Bode diagram. The values of L and C necessary to obtain the required regulator output performancen, once the frequency is fixed, are calculated with the following formulae :

$$L = \frac{(V_i - V_o)\, V_o}{V_i\, f\, \Delta I_L}$$

$$C = \frac{(V_i - V_o)\, V_o}{8L\, f^2\, \Delta V_o}$$

Since this filter introduces two poles at the angular frequency

$$\omega_o = \frac{1}{\sqrt{LC}}$$

we place the zero of the $R_c\, C_c$ network in the same place :

$$\omega_z = \frac{1}{R_C\, C_C}$$

Taking into account also the gain of the PWM block, the Bode plot of figure A6 is obtained.

The slope where the curve crosses the axis at 0dB is about 40dB/decade therefore the circuit is unstable.

Taking into account now the zero introduced by the equivalent series resistance (ESR) of the output capacitor, we have further condition for dimensioning the $R_c\, C_c$ network. Knowing the ESR (which is supplied by the manufacturer for the quality components) we can determine the value of R_c so that the axis is crossed at 0dB with a single slope. The zero introduced by the ESR is at the angular frequency :

$$w_{zESR} = \frac{1}{ESR \cdot C}$$

The overall Bode diagram is therefore as shown in figure A7.

Figure A6 : Bode Plot of System Taking Filter and Compensation Network into Account.

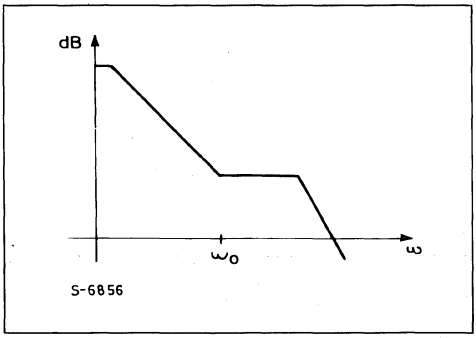
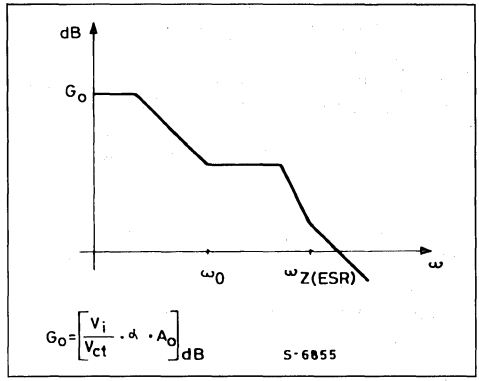


Figure A7 : Bode Plot of Complete System Taking into Consideration the Equivalent Series Resistance of the Output Capacitor.



DC GAIN AND LINE REGULATION

Indicating the open-loop gain of the error amplifier with A_o, the overall open-loop gain of the system is :

$$A_t = A_o \cdot \frac{V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}$$

When $V_o = V_{REF}$, the gain becomes :

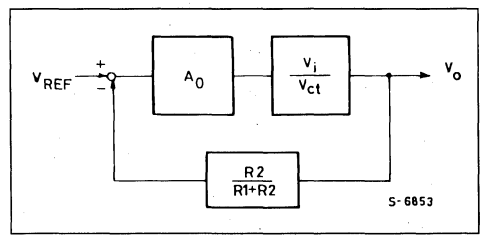
$$A_t = A_o \cdot \frac{V_i}{V_{ct}}$$

Considering the block diagram of figure A8 and calculating the output variation ΔV_o caused by a variation of V_i, from the literature we obtain :

$$\frac{\frac{\Delta V_o}{V_o}}{\frac{\Delta V_i}{V_i}} = \frac{A_o \cdot \frac{V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}}{1 + A_o \cdot \frac{V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}}$$

This espression is of general validity. In our case the percentage variation of the reference must be added by vector addition.

Figure A8 : Block Diagram for Calculation of Line Regulation.



APPENDIX B

REDUCING INTERFERENCE

The main disadvantage of the switching technique is the generation of interference which can reach levels which cause malfunctions and interfere with other equipment.

For each application it is therefore necessary to study specific means to reduce this interference within the limits allowed by the appropriate standards.

Among the main sources of noise are the parasitic inductances and capacitances within the system which are charged and discharged fastly. Parasitic capacitances originate mainly between the device case and the heatsink, the windings of the inductor and the connection wires. Parasitic inductances are generally found distributed along the strips of the printed circuit board.

Fast switching of the power transistors tends to cause ringing and oscillations as a result of the parasitic elements. The use of a diode with a fast reverse recovery time (trr) contributes to a reduction in the noise flowing by the current peak generated when the diode is reverse biased.

Radiated interference is usually reduced by enclosing the regulator in a metal box.

To reduce conducted electromagnetic interference (or radio frequency interferences - RFI) to the levels permitted a suitably dimensioned filter is added on the supply line. The best method, generally, to reduce conducted noise is to filter each output terminal of the regulator. The use of a fixed switching frequency allows the use of a filter with a relatively narrow bandwidth. For off-line switching regulators this filter is usually costly and bulky. In contrast, if the device is supplied from a 50/60 Hz transformer the RFI filter problem is greatly reduced.

Tests have been carried out at the laboratories of Roederstein to determine the dimensions of a mains supply filter which satisfies the VDE 0871/6.78, class B standard. The measurements (see figs. B1 and B2) refer to the application with the L296 supplied with a filtered secondary voltage of about 30V, with $V_o = 5.1V$ and $I_o = 4A$. The switching frequency is 100kHz.

Figure B1 shows the results obtained by introducing on the transformer primary a 0.01µF/250V ~ class X capacitor (type ERO F1772-310-2030). To reduce interference further below the limit set by the standards an additional inductive filter must be added on the primary of the transformer.

Figure B2 shows the curves obtained by introducing this inductive filter (type ERO F1753-210-124). Measurements have also been performed beyond 30MHz ; the maximum value measured is still well below the limit curve.

Figure B1 : EMI Measurements with a Capacitor Connected across the Primary Transformer with Screen Grounded (A)

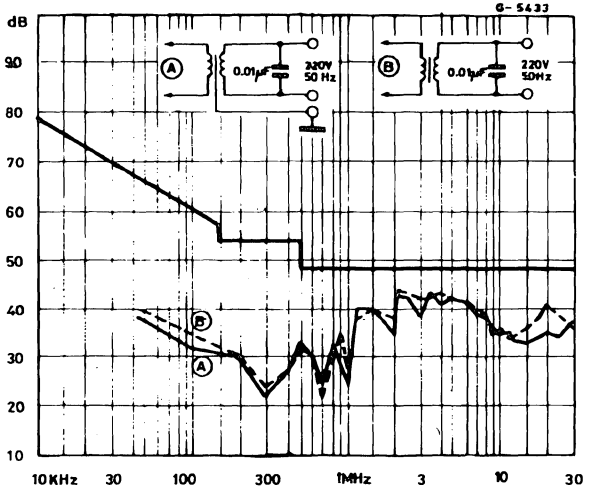
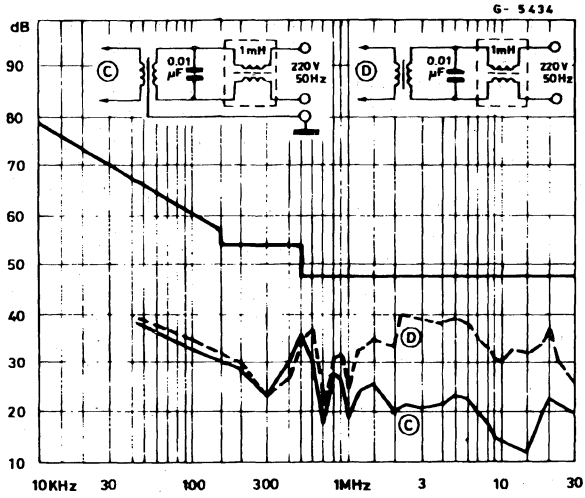


Figure B2 : EMI results with the addition of an inductive filter on the mains input.

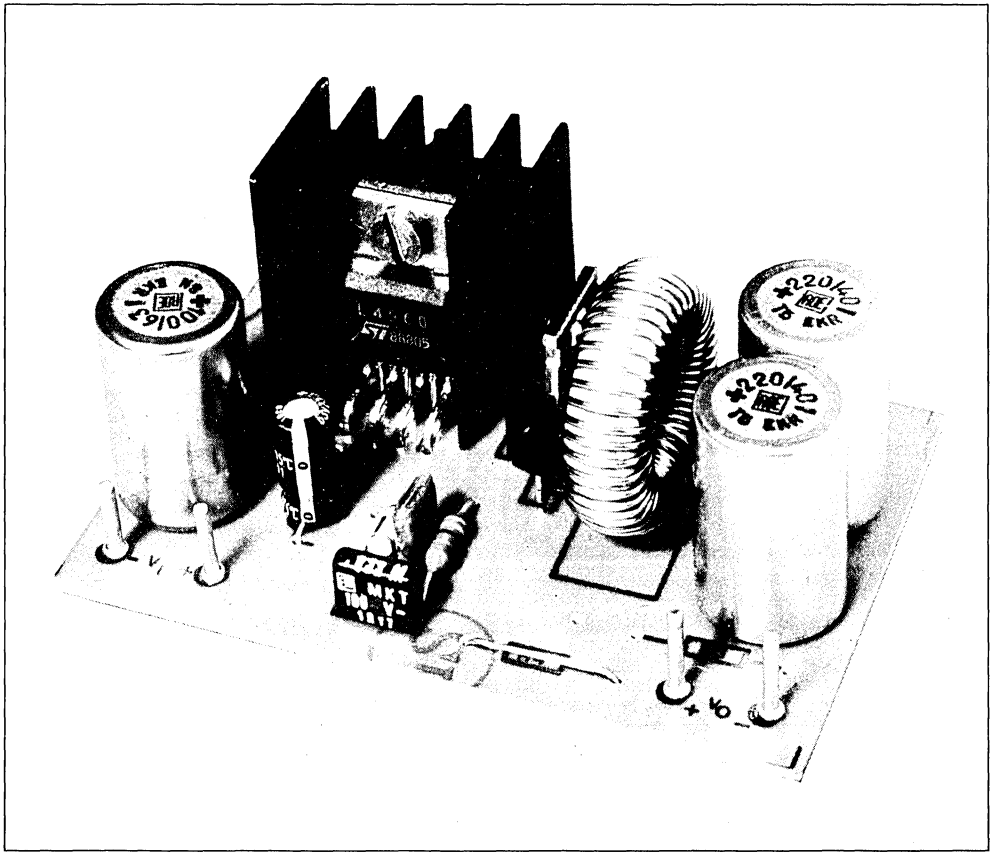


SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

DESIGNING MULTIPLE-OUTPUT POWER SUPPLIES WITH THE L296 AND L4960

Multiple output supplies can be realized simply and economically using the SGS THOMSON Microelectronics L296 and L4960 high power switching regulators. This note describes several practical circuits of this type.



Most of the switching regulators produced today have multiple outputs. The output voltages most frequently used - at least for powers up to 50W - are + 5V – 5V, + 12V and – 12V. In these supplies the 5 V output is normally the output which delivers the highest current and requires the highest precision. For the other voltages - particularly the negative outputs - less precision (± 5 % ± 7 %) is usually sufficient. Often, however, for high current 12V outputs better stabilization and greater precision (typically ± 4 % - the output tolerance of an L7800 series linear regulator) are required.

Multiple output supplies which satisfy these requirements can be realized using the SGS THOMSON L296 and L4960 high power switching regulator ICs, Several practical supply designs are described below to illustrate how these components are used to build compact and inexpensive multi-output supplies.

DUAL OUTPUT 15W SUPPLY

V_{o1} = 5V/3A, V_{o2} = 12V/150mA

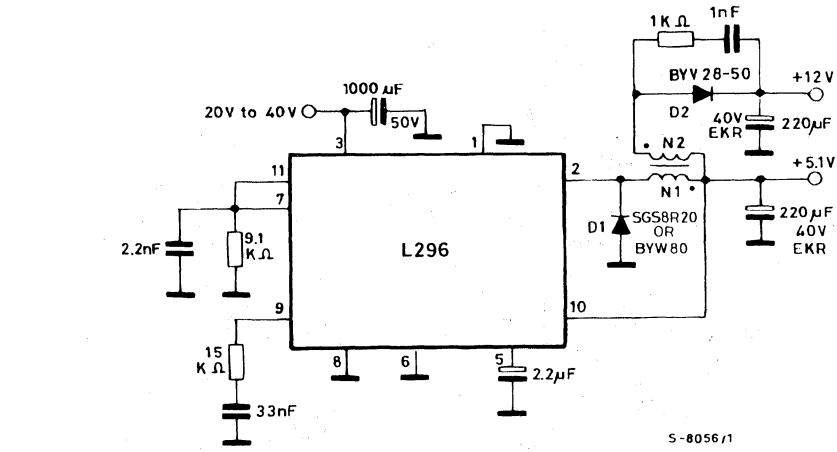
A single L296 is used in this application to produce two outputs. The application circuit, figure 1, illustrates how the second output (12V) is obtained by adding a second winding to the output inductor. Energy is transferred to the secondary during the recirculation period when the internal power device of the L296 is OFF.

Since the 12V output is not separated from the 5V output fewer turns are necessary for the second winding, therefore less copper is needed and load regulation is improved.

In applications of this type it is a good rule to ensure that the power drain on the auxiliary output is no more than 20-25% of the power delivered by the main output.

Table 1 shows the performance obtained with this dual output supply. This circuit operates at a switching frequency of 50KHz.

Figure 1 : Dual Output DC-DC Converter (5V/3A, 12V/150mA).



Transformer : magnetics 58930, N1 = 30 turns, N2 = 40 turns.

Table 1.

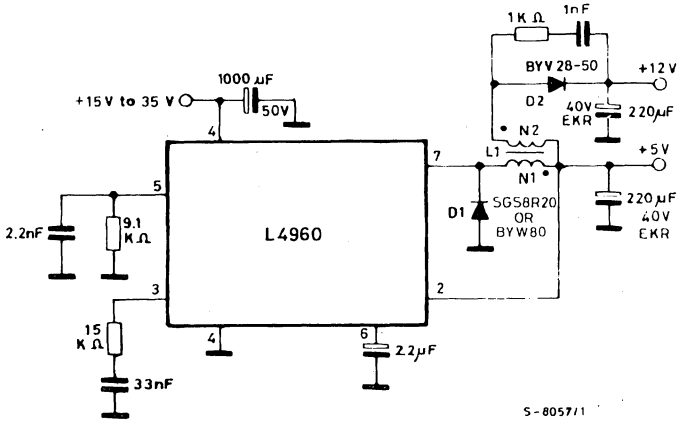
Parameter		V_{O1}	V_{O2}	Unit
Output Voltage I_{O1} = 3A	V_i = 30V I_{O2} = 150mA	5.120	12.089	V
Output Ripple		70	40	mV
Line Regulation I_{O1} = 3A	20V ≤ V_i ≤ 40V I_{O2} = 150mA	15	30	mV
Line Regulation I_{O1} = 700mA	20V ≤ V_i ≤ 40V I_{O2} = 100mA	15	10	mV
Load Regulation I_{O1} = 700mA → 3A	V_i = 30V I_{O2} = 150mA	10	130	mV
Load Regulation I_{O1} = 700mA	V_i = 30V I_{O2} = 100 → 150mA	0	40	mV
Load Regulation I_{O1} = 3A	V_i = 30V I_{O2} = 100 → 150mA	0	40	mV
Efficiency	V_i = 30V V_{O1} = 5.120V I_{O1} = 3A V_{O2} = 12.089V I_{O2} = 150mA	75		%

DUAL OUTPUT 7.5W SUPPLY

V_{o1} = 5V/1.5A, V_{o2} = 12V/100mA

The same technique - adding a secondary winding - can also be used to produce an economical and simple dual output supply with the L4960, a device containing the same control loop blocks as the L296 and a 2A output stage (fig. 2). Though this circuit costs very little the performance obtained (see table 2) is more than satisfactory. The switching frequency is 50kHz.

Figure 2 : Dual Output DC-DC Converter (5V/1.5A, 12V/100mA).



Transformer : magnetics 58206, N1 = 30 turns, N2 = 40 turns.

Table 2.

Parameter		V_{O1}	V_{O2}	Unit
Output Voltage I_{O1} = 1.5A	V_i = 25V I_{O2} = 100mA	5.050	12.010	V
Output Ripple		50	30	mV
Line Regulation I_{O1} = 1.5A	15V ≤ V_i ≤ 35V I_{O2} = 100mA	7	75	mV
Line Regulation I_{O1} = 500mA	15V ≤ V_i ≤ 35V I_{O2} = 50mA	7	60	mV
Load Regulation I_{O1} = 0.5A → 1.5A	V_i = 25V I_{O2} = 100mA	3	100	mV
Load Regulation I_{O1} = 500mA	V_i = 25V I_{O2} = 50mA → 100mA	0	55	mV
Load Regulation I_{O1} = 1.5A	V_i = 25V I_{O2} = 50mA → 100mA	0	50	mV
Efficiency	V_i = 25V V_{O1} = 1.5V V_{O2} = 100mA	78		%

TRIPLE OUTPUT 15W SUPPLY

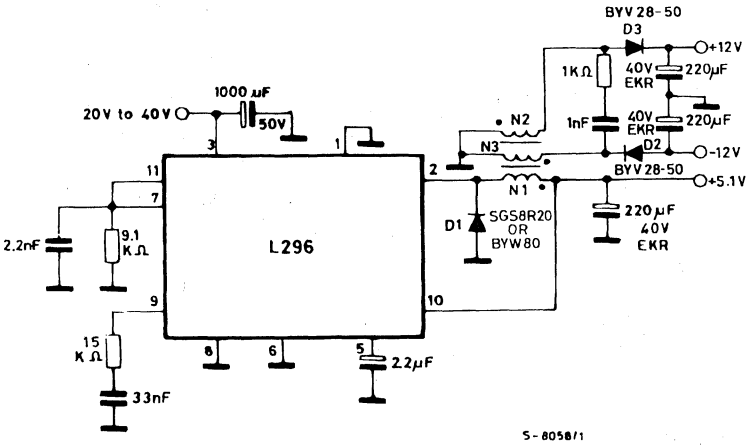
V_{o1} = 5V/3A, V_{o2} = 12V/100mA, V_{o3} = -12V/100mA

Figure 3 shows how to obtain two auxiliary outputs (± 12V) which are isolated from the 5V output. For this output power range an L296 is used.

To ensure good tracking of the 12V and - 12V outputs the secondary outputs in this application should be bifilar wound.

This circuit operates at 50KHz and gives the performance indicated in table 3.

Figure 3 : Triple Output DC-DC Converter (5V/3A, 12V/100mA).



Transformer : magnetics 58206, N1 = 30 turns, N2 = 40 turns.

Table 3.

Parameter		V_{O1}	V_{O2}	V_{O3}	Unit
Output Voltage I_{O1} = 3A	V_i = 30V $I_{O2} = I_{O3}$ = 100mA	5.057	12.300	– 12.300	V
Output Ripple		80	30	30	mV
Line Regulation I_{O1} = 700 mA	20V ≤ V_i ≤ 40V $I_{O2} = I_{O3}$ = 100mA	15	60	60	mV
Line Regulation I_{O1} = 3A	20V ≤ V_i ≤ 40V $I_{O2} = I_{O3}$ = 100mA	18	100	100	mV
Load Regulation I_{O1} = 0.7A → 3A	V_i = 30V $I_{O2} = I_{O3}$ =100mA	4	150	150	mV
Load Regulation I_{O1} = 3A	V_i = 30V I_{O2} = 100mA I_{O3} = 50 → 100mA	0	125	52	mV
Load Regulation I_{O1} = 3A I_{O2} = 50 → 100mA	V_i = 30V I_{O3} = 100mA	0	50	120	mV
Efficiency		76			%

TRIPLE OUTPUT 7.5W SUPPLY

V_{o1} = 5V/1.5A, V_{o2} = 12V/50mA, V_{o3} = – 12/50mA

For lower output powers, the L296 in the previous application may be replaced by an L4960 as shown in figure 4. The performance of this circuit is indicated in table 4.

Figure 4 : Triple Output DC-DC Converter (5V/1.5A, 12V/50mA, – 12V/50mA).

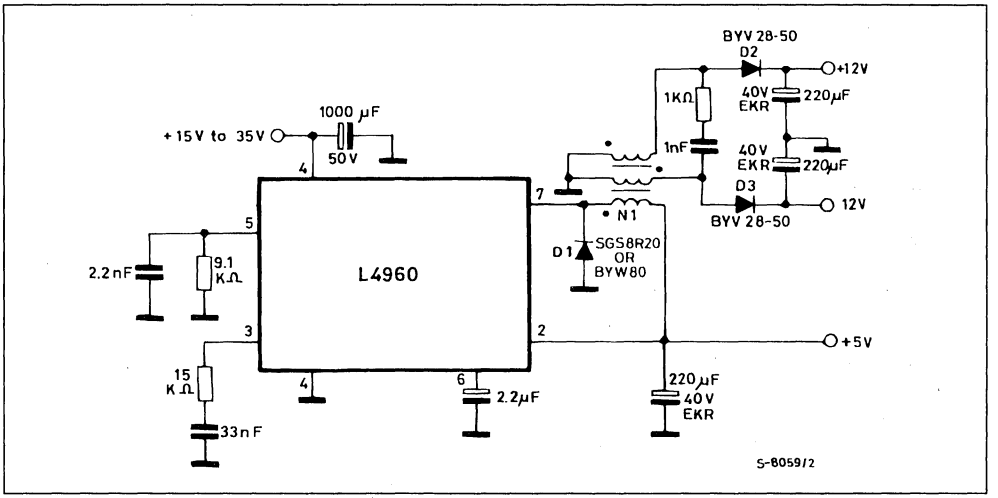


Table 4.

Parameter		V_{O1}	V_{O2}	V_{O3}	Unit
Output Voltage I_{O1} = 1.5A	V_i = 25V $I_{O2} = I_{O3}$ = 50mA	5.040	12.020	– 12.020	V
Output Ripple		60	30	30	mV
Line Regulation I_{O1} = 500mA	15V ≤ V_i ≤ 35V $I_{O2} = I_{O3}$ = 50mA	5	80	80	mV
Line Regulation I_{O1} = 1.5A	15V ≤ V_i ≤ 35V $I_{O2} = I_{O3}$ = 50mA	4	60	60	mV
Load Regulation I_{O1} = 0.5A → 1.5A	V_i = 25V $I_{O2} = I_{O3}$ = 50mA	5	120	120	mV
Load Regulation I_{O1} = 1.5A I_{O3} = 20 → 50mA	V_i = 25V I_{O2} = 50mA	0	15	50	mV
Load Regulation I_{O1} = 1.5A I_{O2} = 20 → 50mA	V_i = 25V I_{O3} = 100mA	0	50	15	mV
Efficiency			70		%

THE L296 AND L4960 HIGH POWER SWITCHING REGULATORS

The SGS THOMSON L296 is a monolithic stepdown switching regulator assembled in the 15-pin Multiwatt package. Operating with supply input voltages up to 46V it provides a regulated 4A output variable from 5.1V to 40V.

Internally the device is equipped with current limiter, soft start and reset (or power fail) functions, making it particularly suitable for supplying microprocessors and logic.

The precision of the L296's internal reference (± 2%) eliminates the need for external dividers or trinning to obtain a 5V output.

The synchronization pin allows synchronous operation of several devices at the same frequency to avoid generating undesirable beat frequencies.

The L4960 is a similar device assembled in the 7-lead Heptawatt package. Like the L296 it has a maximum input voltage of 46V and it provides a regulated output voltage variable from 5V to 40V with a maximum load current of 2.5A. Current limiting, soft start and thermal protection functions are included.

The thermal protection circuit in both the L296 and L4960 has a hysteresis of 30°C to allow soft restarting after a fault condition.

THE STEP DOWN CONFIGURATION

Figure 5 shows the basic structure of a step down switching regulator. The transistor Q is used as a switch and the ON and OFF times are determined by the control circuit.

When Q is saturated current flows from the supply, Vi, to the load through the inductor L. Neglecting the saturation voltage of Q, Ve ≅ Vi.

When Q is OFF, current continues to flow in the inductor L, in the same direction, forcing the diode into conduction immediately therefore Ve is negative. In these conditions the load current flows through L and D.

The average value of the current in the inductor is equal to the load current. In the inductor a triangular current ripple equal to . ΔI_L is added to this average current.

During the time when Q is ON this ripple is :

$$\Delta I_L = \frac{(V_i - V_o)\, T_{ON}}{L}$$

and when Q is off it is :

$$\Delta I_L = \frac{V_o \cdot T_{OFF}}{L}$$

Equating these expression and assuming that the transistor and diode are ideal we obtain :

$$V_o = V_i \cdot \frac{T_{ON}}{T}$$

T_{ON} is the conduction time of the transistor

T is the oscillator period

The absolute average current in the supply is therefore :

$$I_{ioc} = I_o \cdot \frac{T_{ON}}{T}$$

Once the working frequency and desired ripple current have been fixed the value of the inductor L is given by :

$$L = \frac{(V_i - V_o)\, V_o}{V_i\, f\, \Delta I_L}$$

and the value of the capacitor C required to give the desired output voltage ripple (Δ V) is :

$$C = \frac{(V_i - V_o)\, V_o}{8\, L\, f^2\, \Delta f_o}$$

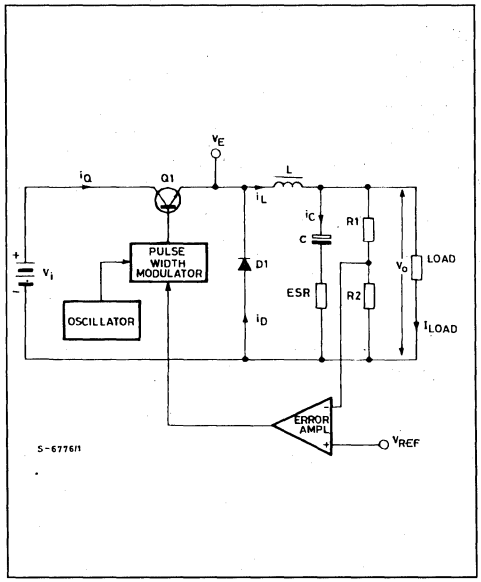
This capacitor must have a maximum ESR given by :

$$ESR_{MAX} = \frac{\Delta V_o}{\Delta I_L}$$

And, finally, the minimum load current, I_{OMIN}, must be :

$$I_{OMIN} = \frac{\Delta I_L}{2} = \frac{(V_i - V_o)\, V_o}{2\, V_i\, f_L}$$

Figure 5 : Basic STEP-DOWN Configuration.



30W DC-DC CONVERTER

Designing power supplies in the 30-40W range is becoming increasingly difficult because it is here that there is the greatest need to maintain performance levels and reduce costs. The application proposed here is very competitive because it exploits new ICs to reduce size, number of components and assembly costs.

This solution, the DC-DC converter, compares very favourable with off-line switching supplies in terms of cost. DC-DC converters can, in fact, be realized even by designers with little experience and allows the convenience of working with low voltages, Off-line switching supplies are only preferable when the weight and size of the mains transformer in a DC-DC converter would be excessive.

In this circuit, figure 6 two devices are used, an L296 and an L4960. The L296 is used, to supply a 5V output with a current of 3A and the auxiliary – 5V/100mA output and the L4960 is used to provide the 12V/1.5A output and the auxiliary – 12V/100mA output.

Figure 6 : Multioutput DC-DC Converter with L296 and L4960 (5V / 3A, 12V / 1.5A, –12V/100mA, –5V/100mA).

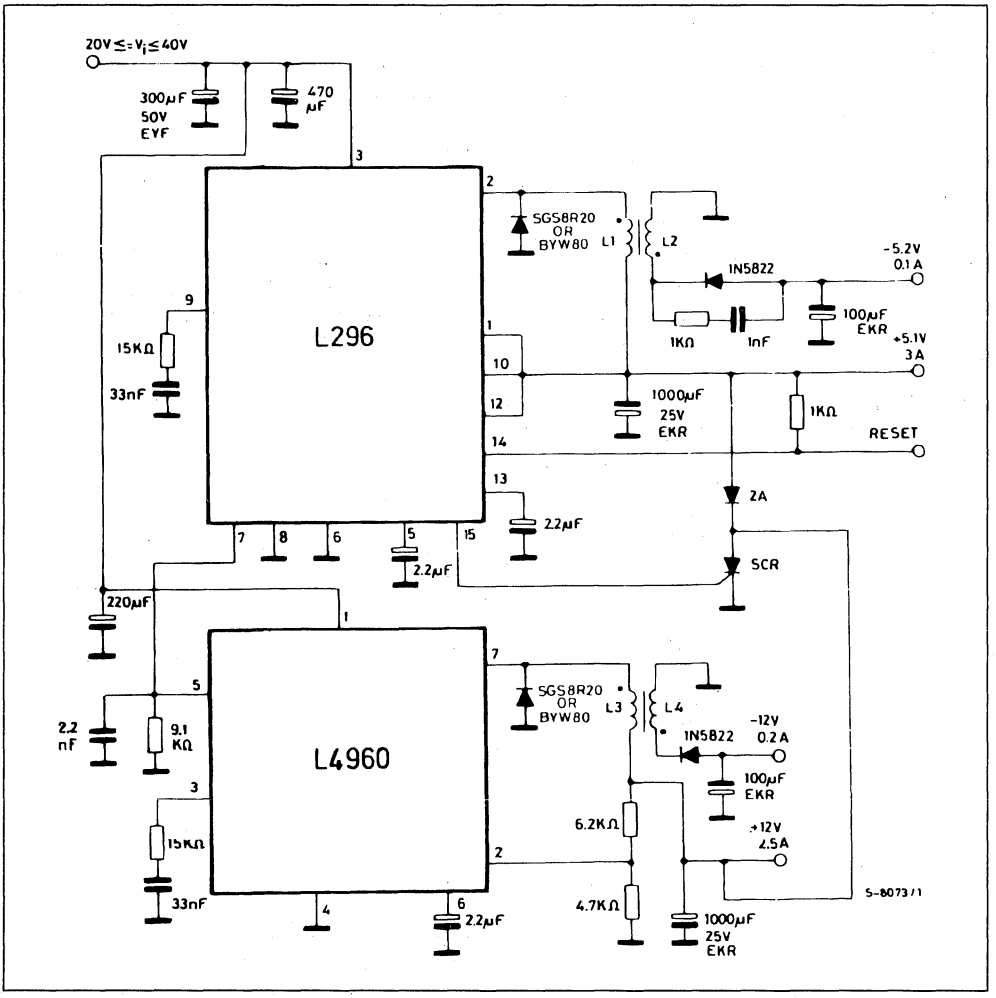


Table 5 shows the performance obtained with this power supply.

Table 5.

Parameter		V_{O1}	V_{O2}	V_{O3}	V_{O4}	Unit
Output Voltage I_{O1} = 3A I_{O2} = 100mA	V_i = 30V I_{O3} = 1.5A I_{O4} = 100mA	5.080	– 5010	11.96	12.00	V
Output Ripple		50	30	50	40	mV
Line Regulation I_{O1} = 1A I_{O3} = 0.5A	20V ≤ V_i ≤ 40V I_{O2} = 100mA I_{O4} = 100mA	13	15	10	20	mV
Load Regulation I_{O1} = 1A to 3A	V_i = 30V I_{O2} = 100mA	8	90			mV
I_{O3} = 0.5 to 1.5A	I_{O4} = 100mA			3	80	mV
Load Regulation I_{O1} = 3A	V_i = 30V I_{O2} = 50 → 100mA	0	100			mV
I_{O3} = 1.5A	I_{O4} = 50 → 100mA			0	100	mV
Load Regulation I_{O1} = 1A	V_i = 30V I_{O2} = 50 → 100mA	0	35			mV
I_{O3} = 0.5A	I_{O4} = 50 → 100mA			0	90	mV
Line Regulation I_{O1} = 3A	20 ≤ V_i ≤ 40V I_{O2} = 100mA	15	45			mV
I_{O3} = 1.5A	I_{O4} = 100mA			15	40	mV

This application illustrates how two devices may be synchronized. Note also that the reset circuit is used in this case to monitor the output voltage (see figure 7).

If a power fail function is required in place of the reset function the figure 6 circuit should be modified as shown in figure 8.

Figure 7 : Reset Output Waveforms.

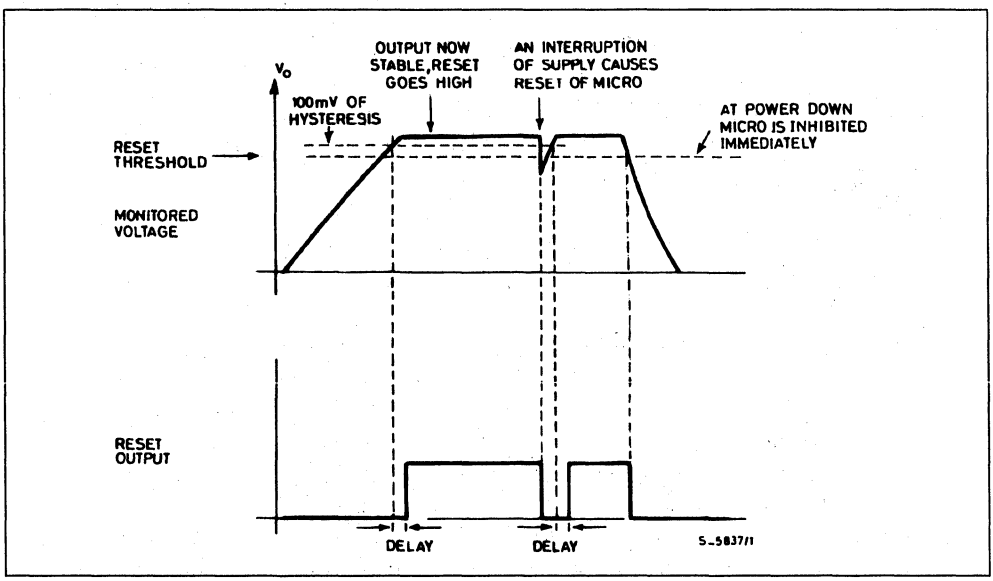
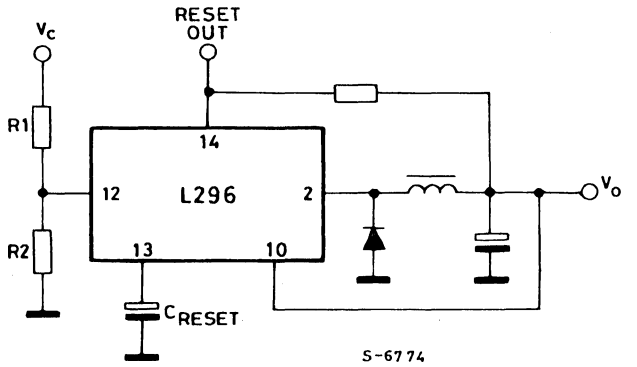


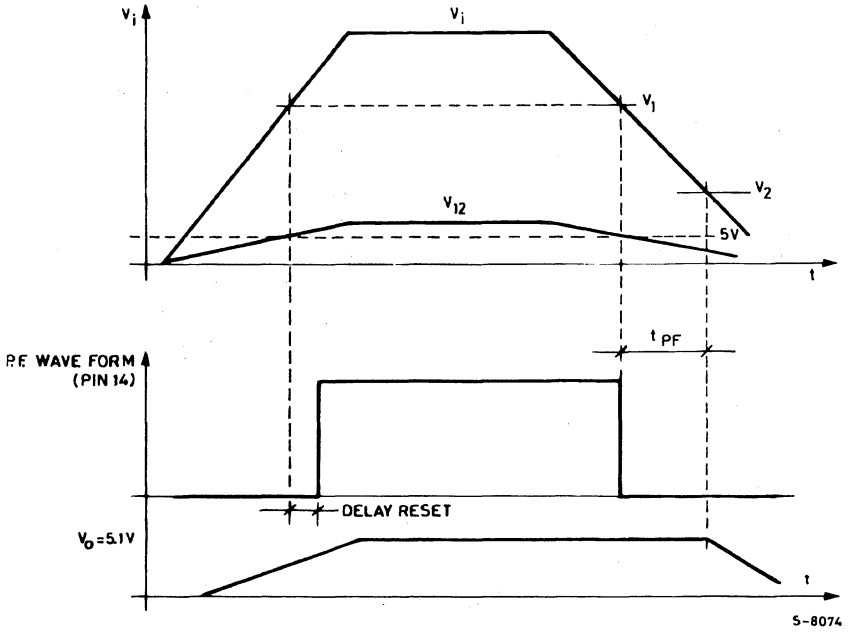
Figure 8.



CALCULATING THE POWER FAIL TIME

The 'power fail time' is defined as the time from when the power fail output (pin 14) goes low to the time when the input voltage falls to the minimum level required to maintain the regulated output (see figure 9). From this definition we can evaluate the energy balance.

Figure 9.



The energy which the filter capacitor C supplies to the operating device while it discharges is :

$$E = 1/2\ C\ (V_1^2 - V_2^2) \quad (1)$$

The load drains a power of $P_o = V_o\ I_o$. Taking into consideration the average efficiency η (derived with the input between V_1 and V_2), the power to be supplied at the input of the device is :

$$P_{o2} = \frac{P_o}{\eta} \quad (2)$$

Equating the expressions (1) and (2) gives :

$$1/2\ C\ (V_1^2 - V_2^2) = \frac{P_o}{\eta} \cdot t_{PF}$$

where V_i is the input voltage at which the voltage on pin 12 reaches 5V (through the divider R_1/R_2) ; V_2 is the maximum input voltage below which the device no longer regulates.

Rearranging this expression to obtain C :

$$C = \frac{2\ P_o\ t_{PF}}{\eta\ (V_1^2 - V_2^2)}$$

EXAMPLE - Suppose that V_o = 5V, I_o = 3A, T_{pf} = 10ms and V_i = 35V. Fixing V_1 = 25V and V_2 = 10V we obtain :

$$C = \frac{2\ P_o\ t_{PF}}{\eta\ (V_1^2 - V_2^2)} = \frac{2 \times 15 \times 10\ .\ 10^{-3}}{0.75\ (25^2 - 10^2)} = 760\mu F$$

We obtain choose a capacitor of 1000µF.

CROWBAR

The L296 includes an internal crowbar function ; the only external component needed is an SCR. The intervention threshold of this block is fixed internally at 20% of the nominal value of the internal reference.

In the figure 6 circuit the SCR is triggered by an overvoltage on the 5V output (usually the most important output to monitor) and shortcircuits to ground the 5V output and, through the diode which connects the two outputs, the 12V output.

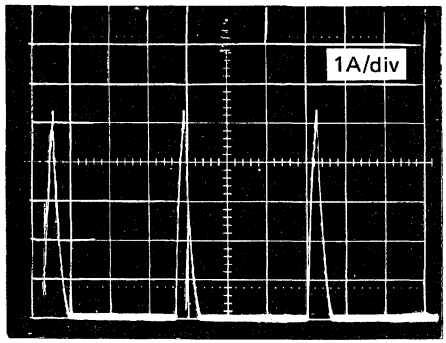
Since the internal current limiter in the device is designed to function as shown in figure 10 (that is, with pulsed output current) the SCR turns off in the gap between pulses and is re-activated gain if, when the device restarts softly, the fault condition has not been eliminated. But if the fault no longer exists the SCR remains OFF and the output voltage returns to the normal value.

If the designer prefers the supply to remain off after the SCR has been activated the circuit can be modified as shown in figure 11. In this modification, when the SCR is triggered a very high current flows in the fuse, blowing it.

Since the filter capacitor can have a high value and be charged to high voltages the choice of SCR is important. The type used in this circuit - the TYP512 - is a plastic packaged SCR able to handle 12 Arms and 300A for 10ms. The maximum forward and reverse voltages are about 50V.

If the crowbar circuit is not used it is advisable to connect pin 1 to ground or pin 10.

Figure 10 : Load Current in Short Circuit Conditions (V_i = 40V, L = 300µH, f = 100KHz).



Current at Pin 2 when the Output is Short Circuited.

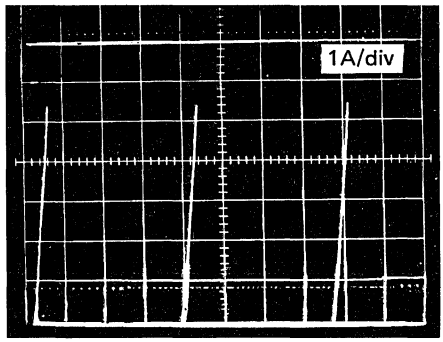
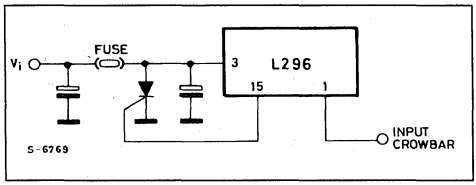


Figure 11.



UC3842 PROVIDES LOW-COST CURRENT-MODE CONTROL

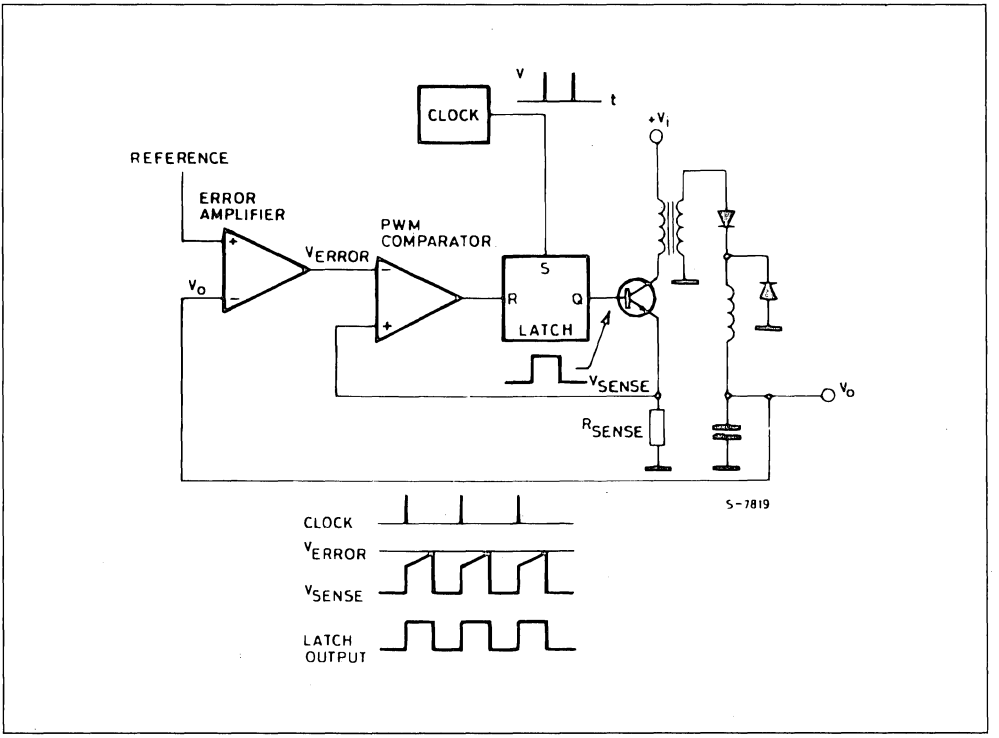
The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives : good electrical performance and low cost. The UC3842 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current-mode operation. In addition, the UC3842 is optimized for efficient power sequencing of off-line converters and for driving increasingly popular POWERMOS.

This application note gives a functional description of the UC3842 and suggests how to incorporate the IC into practical power supplies. A review of current-mode control and its benefits is included and methods of avoiding common pitfalls discussed. The final section presents designs of two power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Figure 1 : Two-loop Current-mode Control System.



Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved ; i.e., the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an error-voltage-controlled-current-source for the purposes of small-signal analysis. This is illustrated by figure 2. The two-pole control-to-output frequency response of these converters is reduced to a single pole (filter capacitor in parallel with load) response.

One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gain-bandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler and better behaved, as illustrated in figure 3. Capacitor C_i and resistor R_{iz} in figure 3a add a low frequency zero which cancels one of the two control-to-output poles of non-current-mode converters. For large-signal load changes, in which converter response is limited by inductor slew rate, the error amplifier will saturate while the inductor is catching up with the load. During this time, C_i will charge to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output vol-tage. The recovery time is R_{iz} C_i, which may be milleseconds. However, the compensation network of figure 3b can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i.

Figure 2 : Inductor Looks Like a Current Source to Small Signals.

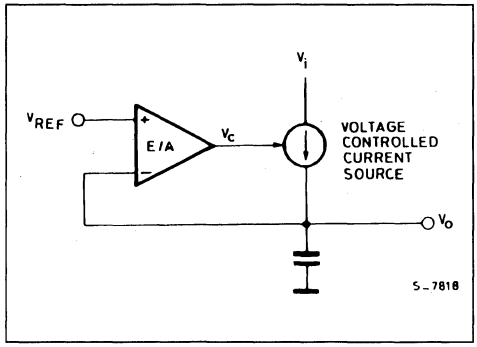


Figure 3 : Required Error Amplifier Compensation for Continuous Inductor Current Designs using (a) Duty-cycle Control and (b) Current-mode Control.

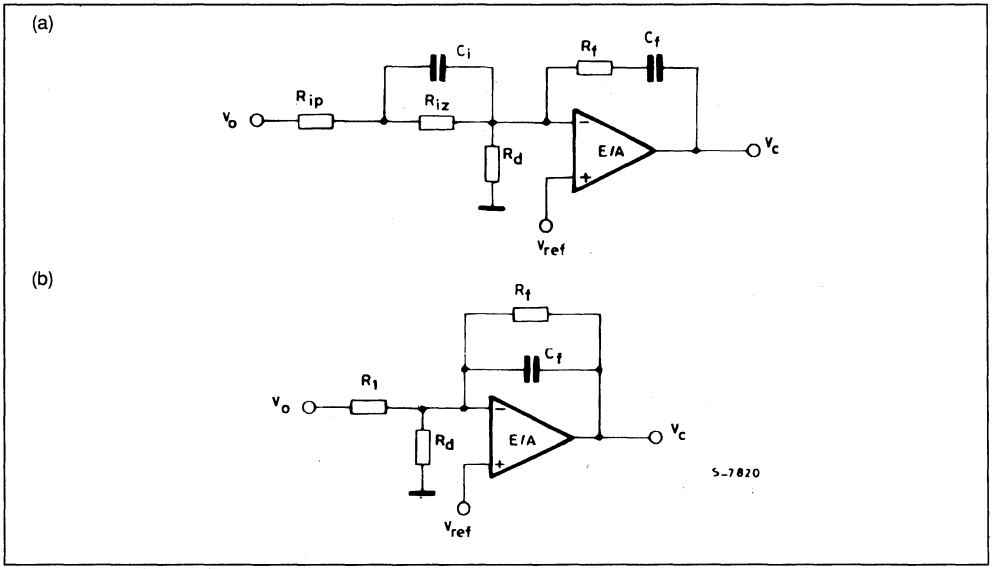
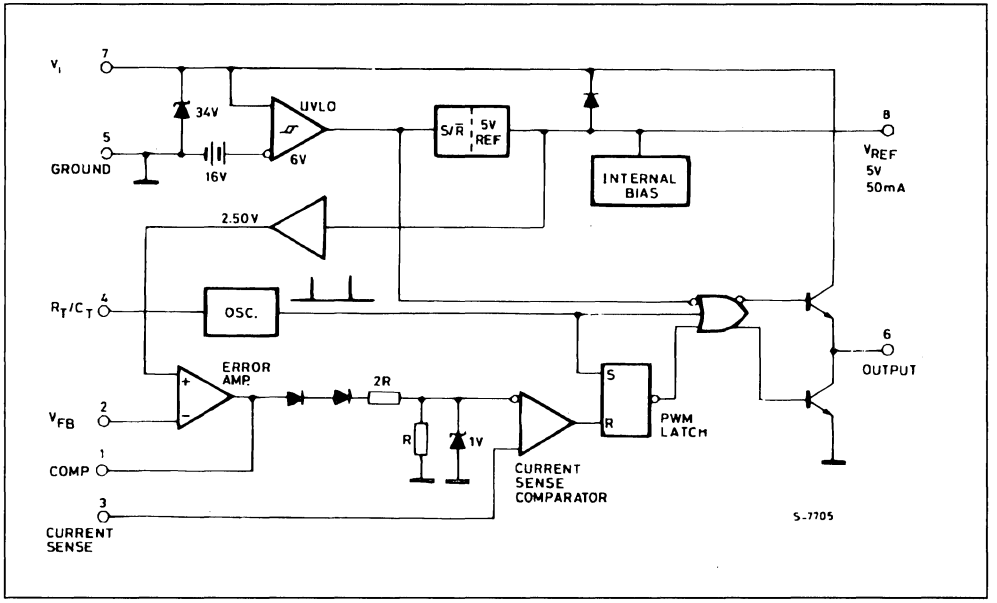


Figure 4 : UC3842 Block Diagram.



Current limiting is simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

FUNCTIONAL DESCRIPTION

A block diagram of the UC3842 appears in figure 4. This IC will operate from a low impedance DC source of 10 V to 30 V. Operation between 10 V and 16 V requires a start-up bootstrap to a voltage greater than 16 V in order to overcome the under-voltage lockout. V_{CC} is internally clamped to 34 V for operation from higher voltage current-limited sources ($I_{CC} \leq 30$ mA).

UNDER-VOLTAGE LOCKOUT (UVLO)

This circuit insures that V_{CC} is adequate to make the UC3842 fully operational before enabling the output stage. Figure 5a shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16 V and 10 V respectively. The 6 V hysteresis prevents V_{CC} oscillations during power sequencing. Figure 5b shows supply current requirements. Start-up current is less than 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by figure 6. During normal circuit operation, V_{CC} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN}. At start-up, however, C_{IN} must be charged to 16 V through R_{IN}. With a start-up current of 1 mA, R_{IN} can be as large as 100 kΩ and still charge C_{IN} when V_{AC} = 90 V RMS (low line). Power dissipation in R_{IN} would then be less than 350 mW even under high line (V_{AC} = 130 V RMS) conditions.

During UVLO, the UC3842 output driver is biased to a high impedance state. However, leakage currents (up to 10 μA), if not shunted to ground, could pull high the gate of a POWERMOS. A 100 kΩ shunt, as showing in figure 6, will hold the gate voltage below 1 V

Figure 5 : (a) Under-voltage Lockout and (b) Supply Current Requirements.

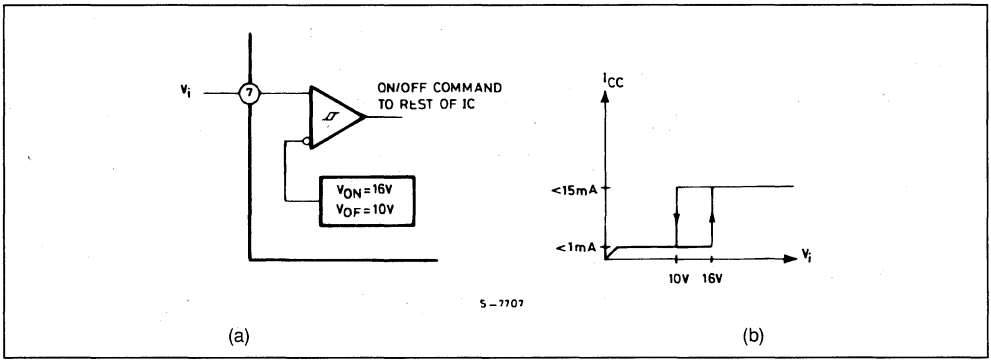
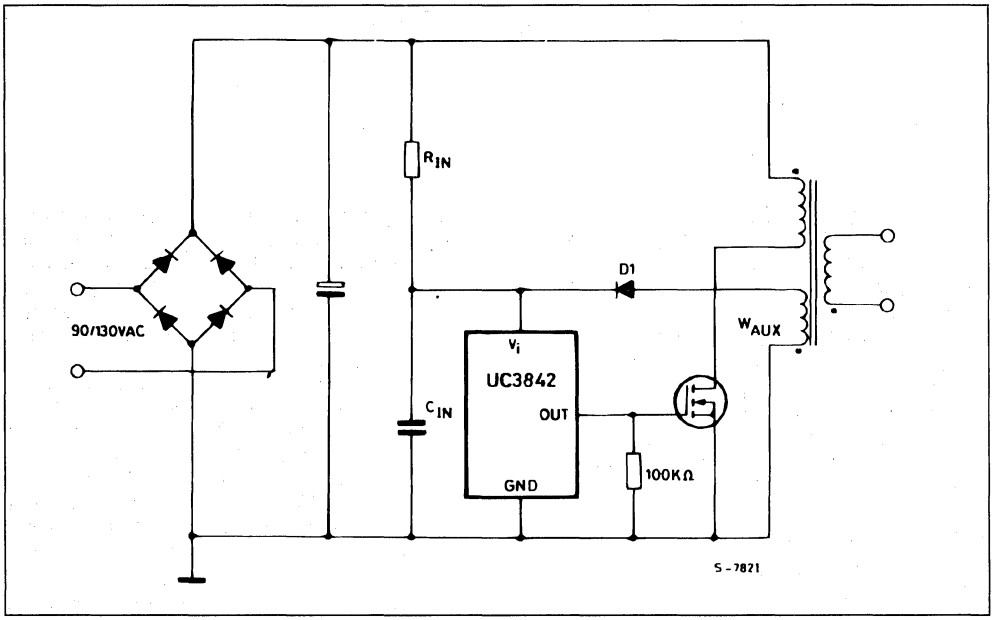


Figure 6 : Providing Power to the UC3842.



OSCILLATOR

The UC3842 oscillator is programmed as shown in figure 7a. Oscillator timing capacitor C_T is charged from V_{REF} (5 V) through R_T, and discharged by an internal current source. Charge and discharge times are given by :

$$t_c \approx 0.55\ R_T\ C_T$$

$$t_d \approx R_T\ C_T\ \ln\left(\frac{0.0063\ R_T - 2.7}{0.0063\ R_T - 4.0}\right)$$

frequency, then, is : $$f = \frac{1}{t_c + t_d}$$

For $R_T > 5\ k\Omega$, t_d is small compared to t_c, and :

$$f \approx \frac{1}{0.55\ R_T\ C_T} \approx \frac{1.8}{R_T\ C_T}$$

During the discharge time, the internal clock signal blanks the output to the low state. Therefore, t_d limits maximum duty cycle (D_{MAX}) to :

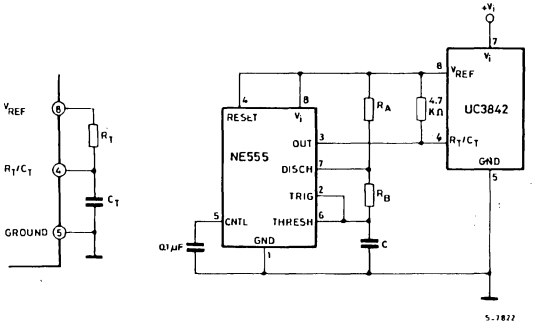
$$D_{MAX} = \frac{t_c}{t_c + t_d} = 1 - \frac{t_d}{\tau}$$

where $\tau = 1/f$ = switching period.

The timing capacitor discharge current is not tightly controlled, so t_d may vary somewhat over temperature and from unit to unit. Therefore, when very precise duty cycle limiting is required, the circuit of figure 7b is recommended.

One or more UC3842 oscillators can be synchronized to an external clock as shown in figure 8. Noise immunity is enhanced if the free-running oscillator frequency ($f = 1/(t_c + t_d)$) is programmed to be ~ 20 % less than the clock frequency.

Figure 7 : (a) Oscillator Timing Connections and (b) Circuit for Limiting Duty Cycle.



(a)

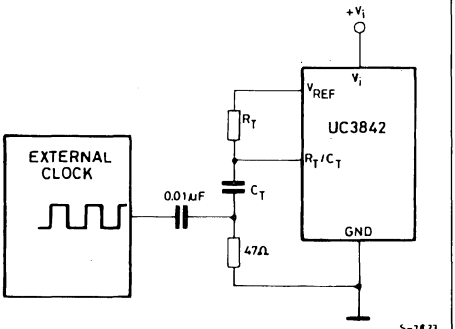
(b)

$$D_{MAX} = \frac{t_c}{(t_H + t_L)}$$

$$t_H = 0.693\ (R_A + R_B)\ C$$

$$t_L = 0.693\ R_B\ C$$

Figure 8 : Synchronization to an External Clock.



ERROR AMPLIFIER

The error amplifier (E/A) configuration is shown in figure 9. The non-inverting input is not brought out to a pin, but is internally biased to 2.5 V ± 2 %. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 10a shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with continuous inductor current. The feedback components add a pole to the loop transfer function at $f_p = 1/2\ \pi R_f\ C_f$. R_f and C_f are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_i and R_f fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0dB) at $f \approx f_{switching}/4$. This technique insures converter stability while providing good dynamic response.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_p and C_p in the circuit of figure 10b provide this pole.

The E/A output will source 0.5 mA and sink 2 mA. A lower limit for R_f is given by :

$$R_{f\,(MIN)} \approx \frac{V_{E/A\ OUT(max)} - 2.5\ V}{0.5\ mA} = \frac{6\ V - 2.5\ V}{0.5\ mA} = 7\ k\Omega$$

E/A input bias current (2 µA max) flows through R_i, resulting in a DC error in output voltage (V_o) given by :

$$\Delta\ V_{o(max)} = (2\ \mu A)\ R_i$$

It is therefore desirable to keep the value of R_i as low as possible.

Figure 11 shows the open-loop frequency response of the UC3842 E/A. The gain represent an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1 MHz due to second-order poles at ~ 10 MHz and above.

Figure 9 : UC3842 Error Amplifier.

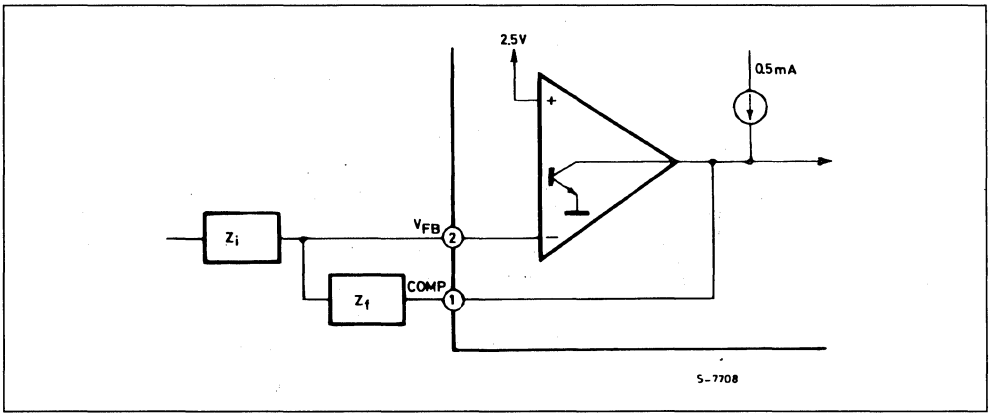


Figure 10 : (a) Error Amplifier Compensation Addition Pole and (b) Needed for Continu ous Inductor-current Boost ad Flyback.

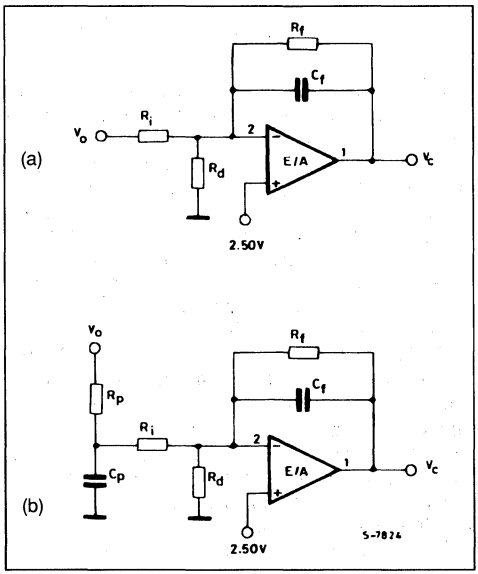
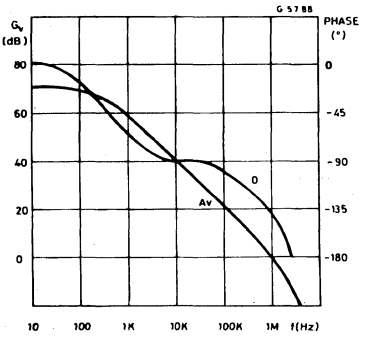


Figure 11 : Error Amplifier Open-loop Frequency Response.



CURRENT SENSING AND LIMITING

The UC3842 current sense input is configured as shown in figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_S. Under normal operation the peak voltage across R_S is controlled by the E/A according to the following relation :

$$V_{RS}\,(pk) = \frac{V_C - 1.4\ V}{3}$$

where : V_C = control voltage = E/A output voltage.

R_S can be connected to the power circuit directly or through a current transformer, as figure 13 illustrates. While a direct connection is simpler, a transformer can reduce power dissipation in R_S, reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-reference sensing. The relation between V_C and peak current in the power stage is given by :

$$i_{(pk)} = N\left(\frac{V_{RS(pk)}}{R_S}\right) = \frac{N}{3\,R_S}\,(V_C - 1.4)$$

where : N = current sense transformer turns ratio.
= 1 when transformer not used.

For purposes of small-signal analysis, the control-to-sensed-current gain is :

$$\frac{i_{(pk)}}{V_C} = \frac{N}{3\,R_S}$$

When sensing current in series with the power transistor, as shown in figure 13, current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and/or interwinding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC3842 current-sense comparator is internally clamped to 1 V (figure 12). Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e. the current limit is defined by :

$$i_{MAX} = \frac{N \cdot 1\ V}{R_S}$$

Figure 12 : Current Sensing.

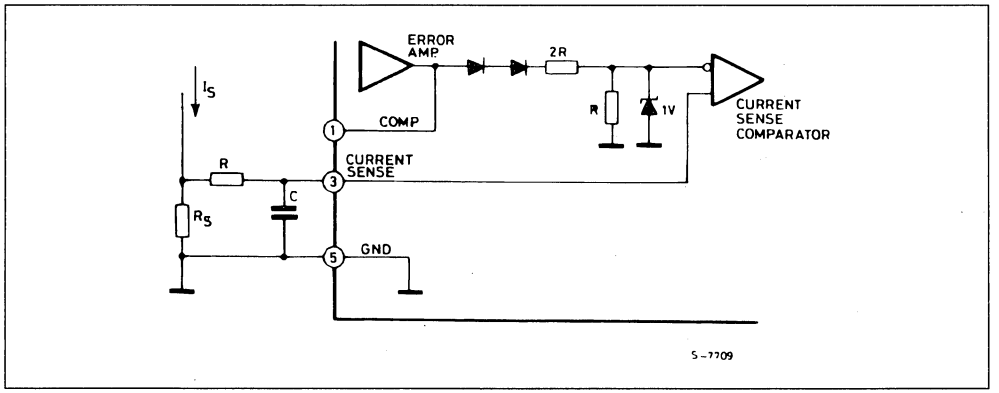
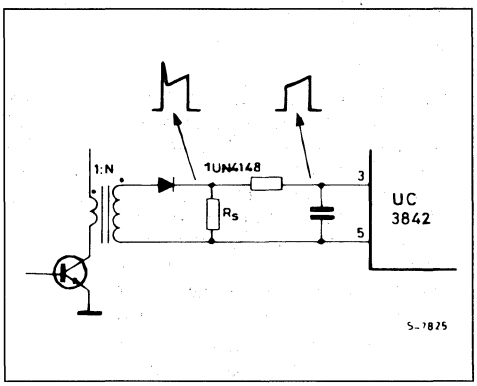


Figure 13 : Transformer-coupled Current Sensing.



TOTEM-POLE OUTPUT

The UC3842 has a single totem-pole output. The output transistors can be operated to ± 1 A peak current and ± 200 mA average current. The peak current is self-limiting, so no series current-limiting resistor is needed when driving a power MOS gate.

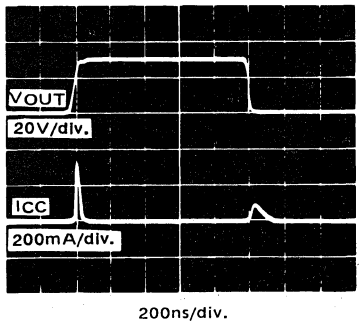
Cross-conduction between the output transistors is minimal, as figure 14 shows. The average added power due to cross-conduction with V_i = 30 V is only 80 mW at 200 kHz.

Figures 15-17 show suggested circuits for driving POWERMOS and bipolar transistors with the UC3842 output. The simple circuit of figure 15 can be used when the control IC is not electrically isolated from the power MOS. Series resistor R_1 provides damping for a parasitic tank circuit formed by the power MOS input capacitance and any series wiring inductance. Resistor R_2 shunts output leakage currents (10 µA maximum) to ground when the under-voltage lockout is active. Figure 16 shows an isolated power MOS drive circuit which is appropriate when the drive signal must be levelshifted or transmitted across an isolation boundary. Bipolar transistors can be driven effectively with the circuit of figure 17. Resistors R_1 and R_2 fix the on-state base current. Capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

PWM LATCH

This flip-flop, shown in figure 4, ensures that only a single pulse appears at the UC3842 output in any one oscillator period. Excessive power transistor dissipation and potential saturation of magnetic elements are thereby averted.

Figure 14 : Output Cross-conduction.



SHUTDOWN TECHNIQUES

Shutdown of the UC3842 can be accomplished by two methods ; either raise pin 3 above 1 V or pull pin 1 below 1 V. Either method causes the output of the PWM comparator to be high (refer to block diagram, figure 4). The PWM latch is reset dominant so that the output will remain low until the first clock pulse following removal of the shutdown signal at pin 1 or pin 3. As shown in figure 18, an externally latched shutdown can be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower under-voltage lockout threshold (10 V). At this point all internal bias is removed, allowing the SCR to reset.

Figure 15 : Direct POWERMOS Drive.

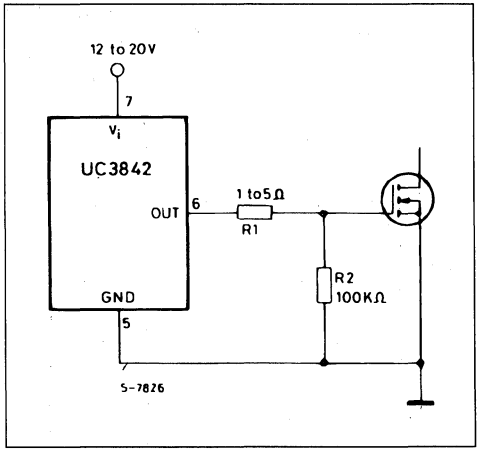


Figure 16 : Isolated POWERMOS Drive.

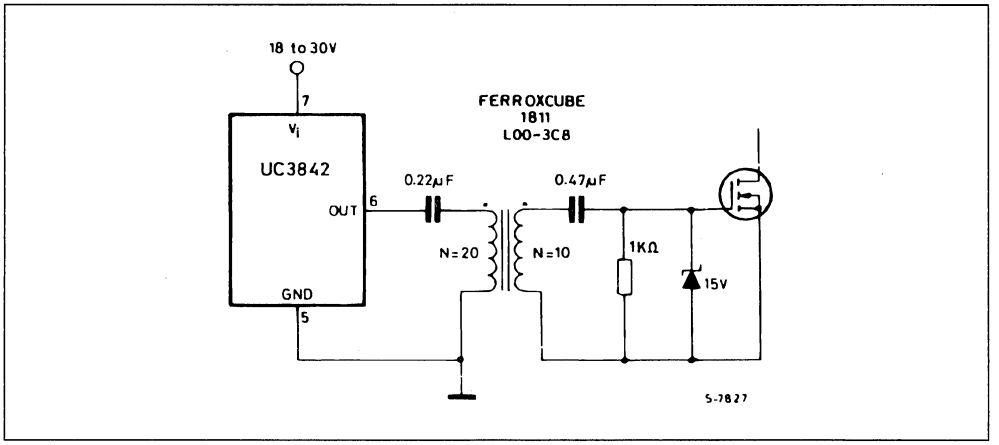
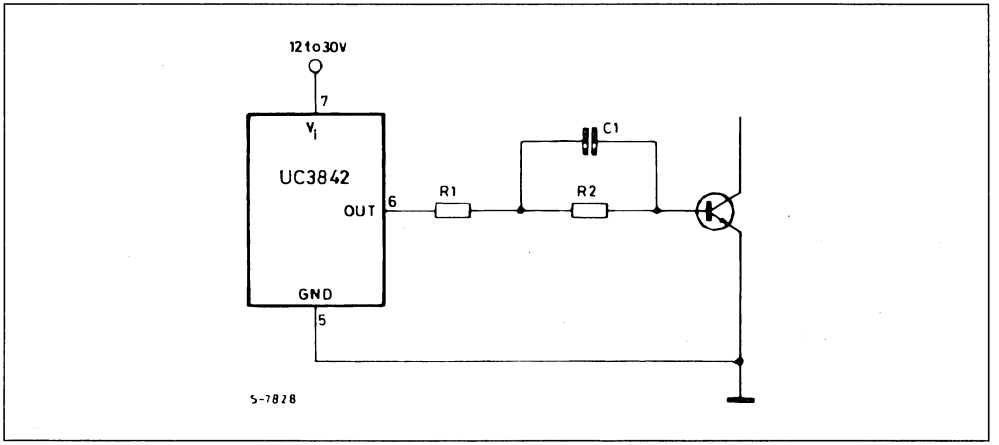


Figure 17 : Bipolar Drive with Negative Turn-off Bias.



AVOIDING COMMON PITFALLS

Current-mode controlled converters can exhibit performance peculiarities under certain operating conditions. This section explains these situations and how to correct them when using the UC3842.

SLOPE COMPENSATION PREVENTS INSTABILITIES

It is well documented that current-mode controlled converters can exhibit subharmonic oscillations when operated at duty cycles greater than 50 %.

Fortunately, a simple technique (usually requiring only a single resistor to implement) exists which corrects this problem and at the same time improves converter performance in other respects. This "slope compensation" technique is described in detail in Reference 6. It should be noted that "duty cycle" here refers to output pulse width divided by oscillator period, even in push-pull designs where the transformer period is twice that of the oscillator. Therefore, push-pull circuits will almost always require slope compensation to prevent subharmonic oscillation.

Figure 18 : Shutdown Achieved by
(a) Pulling Pin 3 High
(b) Pulling Pin 1 Low.

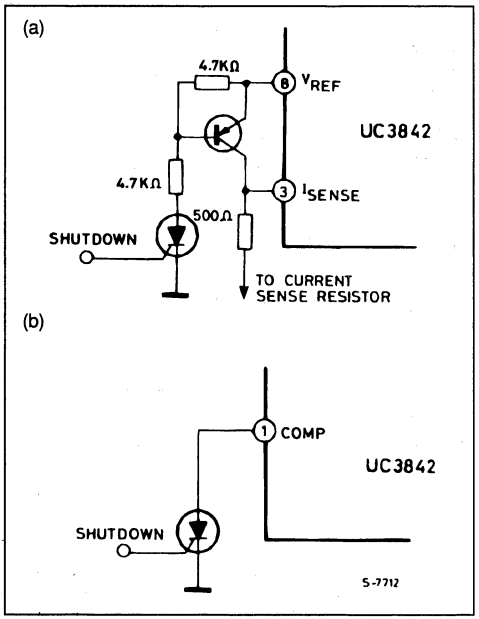


Figure 19 illustrates the slope compensation technique. In figure 19a the uncompensated control voltage and current sense waveforms are shown as a reference. Current is often sensed in series with the switching transistor for buck-derived topologies. In this case, the current sense signal does not track the decaying inductor current when the transistor is off, so dashed lines indicate this inductor current. The negative inductor current slope is fixed by the values of output voltage (V_o) and inductance (L) :

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{-V_F - V_o}{L} = \frac{-(V_F + V_o)}{L}$$

where : V_F = forward voltage drop across the freewheeling diode. The actual slope (m_2) of the dashed lines in figure 19a is given by :

$$m_2 = \frac{R_S}{N} \cdot \frac{di_L}{dt} = \frac{-R_S (V_F + V_o)}{NL}$$

where : R_S and N are defined as the "Current Sensing" section of this paper.

In figure 19b, a sawtooth voltage with slope m has been added to the control signal. The sawtooth is synchronized with the PWM clock, and practice is most easily derived from the control chip oscillator as shown in figure 20a. The sawtooth slope in figure 19b is $m = m_2/2$. This particular slope value is significant in that it yields "perfect" current-mode control ; i.e. with $m_2/2$ the average inductor current follows the control signal so that, in the small-signal analysis, the inductor acts as a controlled current source. All current-mode controlled converters having continuous inductor current therefore benefit from this amount of slope compensation, whether or not they operate above 50 % duty.

More slope is needed to prevent subharmonic oscillations at high duty cycles. With slope $m = m_2$, such oscillations will not occur if the error amplifier gain ($A_{V(E/A)}$) at half the switching frequency ($f_s/2$) is kept below a threshold value (reference 6) :

$$A_{V\,(E/A)} \;\Big|\; \substack{m = m2 \\ f = f_s/2} \;< \frac{\pi\, 2\, C_O}{4\,\tau}$$

where : C_o = sum of filter and load capacitance
$\tau = 1/f_s$

Slope compensation can also improve the noise immunity of a current-mode controlled supply. When the inductor ripple current is small compared to the average current (as in figure 19a), a small amount of noise on the current sense or control signals can cause a large pulse-width jitter. The magnitude of this jitter varies inversely with the difference in slope of the two signals. By adding slope as in figure 19b, the jitter is reduced. In noisy environments it is sometimes necessary to add slope $m > m_2$ in order to correct this problem. However, as m increases beyond $m = m_2/2$, the circuit becomes less perfectly current controlled. A complex trade-off is then required ; for very noisy circuits the optimum amount of slope compensation is best found empirically.

Once the required slope is determined, the value of R_{SLOPE} in figure 20a can be calculated :

$$3\,m = \frac{\Delta V_{RAMP}}{\Delta\, t_{RAMP}} \cdot A_{V(E/A)} = \frac{0.7\ V}{\tau/2}\left(\frac{R_{SLOPE}}{Z_F \mid f_s}\right) = \frac{1.4}{\tau}\left(\frac{R_{SLOPE}}{Z_F \mid f_s}\right)$$

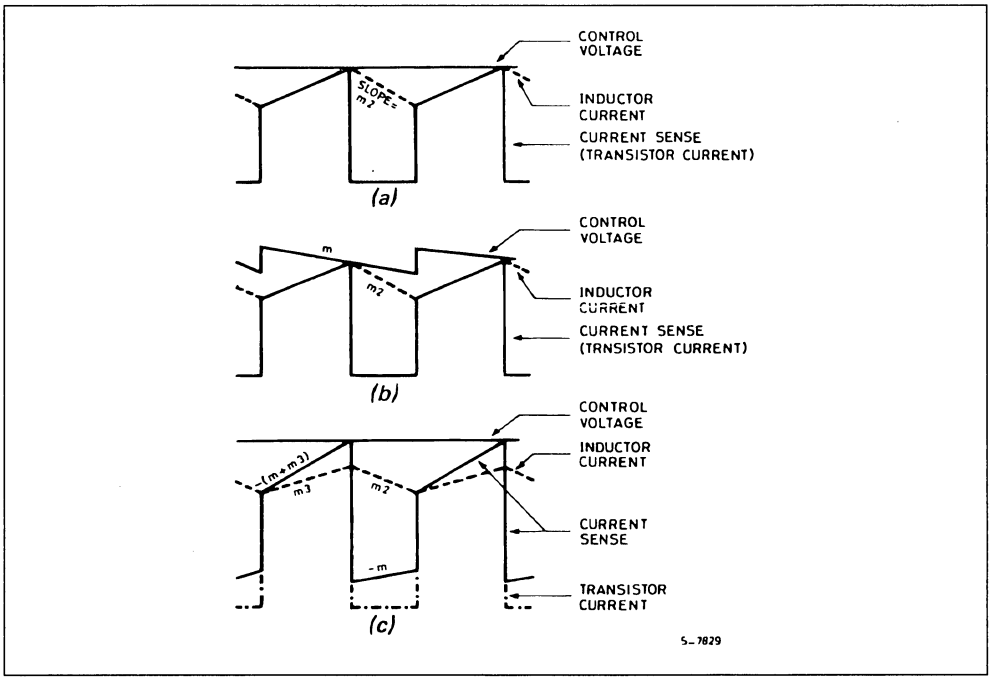
$$R_{SLOPE} = \frac{3\,m\,\tau}{1.4}\,(Z_F \mid f_s) = 2.1 \cdot m \cdot \tau \cdot Z_F \mid f_s$$

where : $Z_F \mid f_s$ is the E/A feedback impedance at the switching frequency.

For $m = m_L$: $\Delta\tau_{RAMP}$

$$R_{SLOPE} = 1.7\,\tau\left(\frac{R_s\,(V_F + V_O)}{NL}\right) Z_F \mid f_s$$

Figure 19 : Slope Compensation Waveforms :
(a) No Comp.
(b) Comp. Added to Control Voltage.
(c) Comp. Added to Current Sense.



Note that in order for the error amplifier to accurately replicate the ramp, Z_F must be constant over the frequency range f_s to at least 3 f_s.

In order to eliminate this last constraint, an alternative method of slope compensation is shown in figures 19c and 20b. Here the artificial slope is added to the current sense waveform rather than subtracted from the control signal. The magnitude of the added slope still relates to the downslope of inductor current as described above. The requirement for R_{SLOPE} is now :

$$m = \frac{\Delta V_{RAMP}}{\Delta t_{RAMP}} \left(\frac{R_f}{R_f + R_{SLOPE}} \right) = \frac{0.7}{\tau/2} \left(\frac{R_f}{R_f + R_{SLOPE}} \right)$$

$$R_{SLOPE} = \frac{1.4\ R_f}{m\tau} - R_f = R_f \left(\frac{1.4}{m\tau} - 1 \right)$$

For $m = m_2$:

$$R_{SLOPE} = R_f \left(\frac{1.4\ NL}{R_S\ (V_F + V_O)\ \tau} - 1 \right)$$

R_{SLOPE} loads the UC3842 R_T/C_T terminal so as to cause a decrease in oscillator frequency. If $R_{SLOPE} >> R_T$ then the frequency can be corrected by decreasing R_T slightly. However, with $R_{SLOPE} \leq 5\ R_T$ the linearity of the ramp degrades noticeably, causing over-compensation of the supply at low duty cycles. This can be avoided by driving R_{SLOPE} with an emitter-follower as shown in figure 21.

Figure 20 : Slope Compensation Added (a) to Control Signal or (b) to Current Sense Waveform.

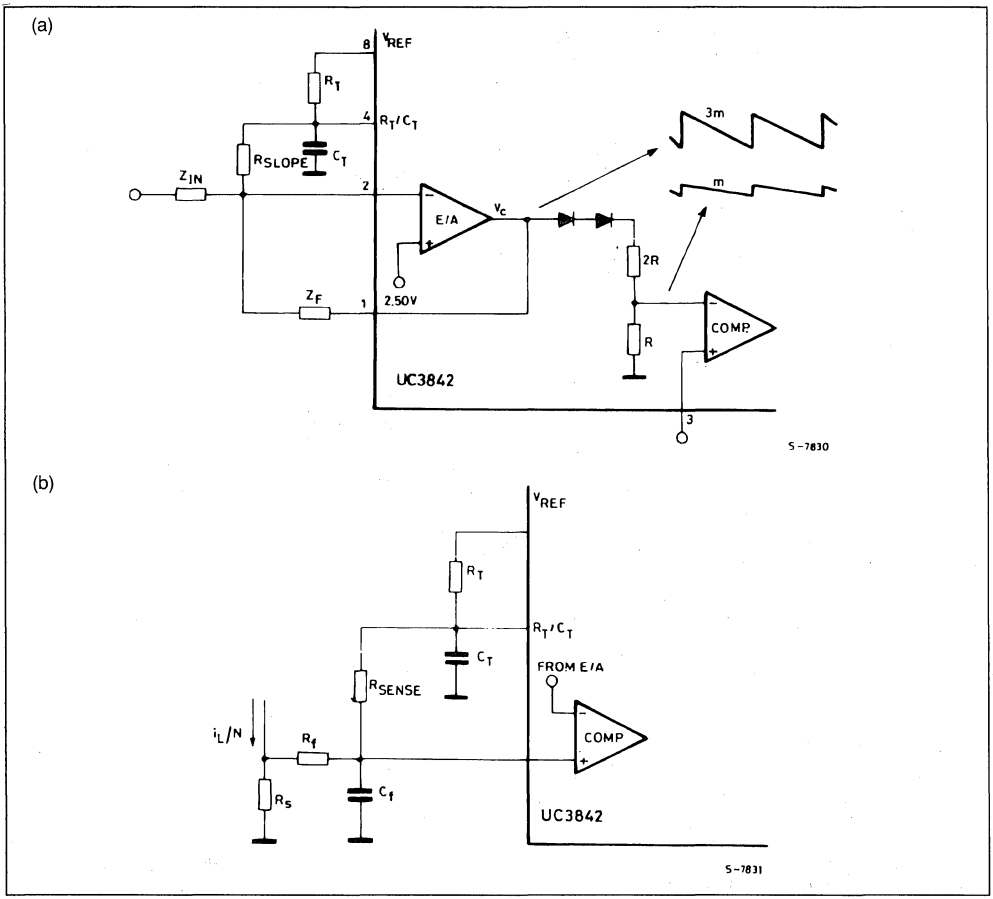
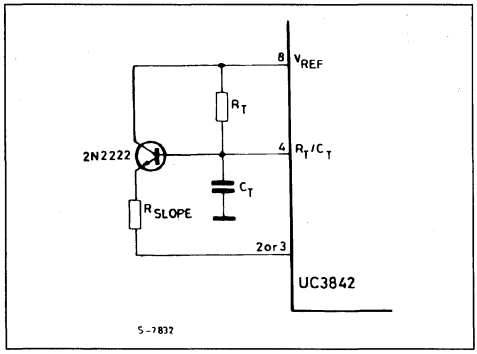


Figure 21 : Emitter-follower Minimizes Load at R_T/C_T Terminal.



NOISE

As mentioned earlier, noise on the current sense or control signals can cause significant pulse-width jitter, particularly with continuous-inductor-current designs. While slope compensation helps alleviate this problem, a better solution is to minimize the amount of noise. In general, noise immunity improves as impedance decrease at critical points in a circuit.

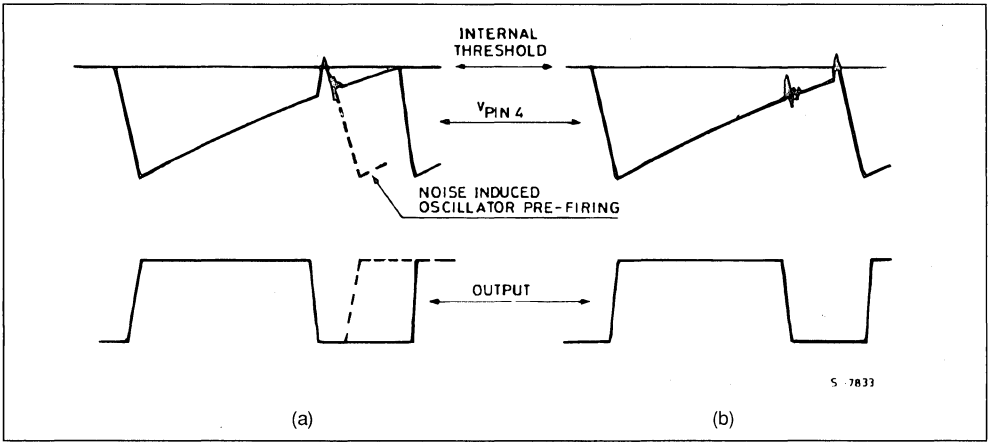
One such point for a switching supply is the ground line. Small wiring inductances between various ground points on a PC board can support common-mode noise with sufficient amplitude to interfere with correct operation of the modulating IC. A copper ground plane and separate return lines for high-current paths greatly reduce common-mode noise.

Note that the UC3842 has a single ground pin. High sink currents in the output therefore cannot be returned separately.

Ceramic bypass capacitors (0.1 µF) from V_I and V_{REF} to ground will provide low-impedance paths for high frequency transients at those points. The input to the error amplifier, however, is a high-impedance point which cannot be bypassed without affecting the dynamic response of the power supply. Therefore, care should be taken to lay out the board in such a way that the feedback path is far removed from noise generating components such as the power transistor(s).

Figure 22a illustrates another common noise-induced problem. When the power transistor turns off, a noise spike is coupled to the oscillator R_T/C_T terminal. At high duty cycles the voltage at R_T/C_T is approaching its threshold level (~ 2.7 V, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude will prematurely trip the oscillator as shown by the dashed lines. In order to minimize the noise spike, choose C_T as large as possible, remembering that deadtime increases with C_T. It is recommended that C_T never be less than ~ 1000 pF. Often the noise which causes this problem is caused by the output (pin 6) being pulled below ground at turn-off by external parasitics. This is particularly true when driving POWERMOS. A diode clamp from ground to pin 6 will prevent such output noise from feeding to the oscillator. If these measures fail to correct the problem, the oscillator frequency can always be stabilized with an external clock. Using the circuit of figure 8 results in an R_T/C_T waveform like that of figure 22b. Here the oscillator is much more immune to noise because the ramp voltage never closely approaches the internal threshold.

Figure 22 : (a) Noise on Pin 4 Can Cause Oscillator to Pre-trigger.
(b) With External Sync. Noise Does not Approach threshold Level.

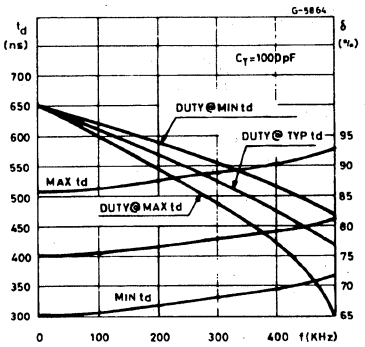


MAXIMUM OPERATING FREQUENCY

Since output deadtime varies directly with C_T, the restraint on minimum C_T (1000 pF) mentioned above results in a minimum deadtime varies for the UC3842. This minimum deadtime varies with R_T and therefore with frequency, as shown in figure 23. Above 100 kHz, the deadtime significantly reduces the maximum duty cycle obtainable at the UC3842 output (also show in figure 23). Circuits not requiring large duty cycles, such as the forward converter and flyback topologies, could operate as high as 500 kHz. Operation at higher frequencies is not recommended because the deadtime become less predictable.

The speed of the UC3842 current sense section poses an additional constraint on maximum operating frequency. A maximum current sense delay of 400 ns represents 10 % of the switching period at 250 kHz and 20 % at 500 kHz. Magnetic components must not saturate as the current continues to rise during this delay period, and power semiconductors must be chosen to handle the resulting peak currents. In short, above ~ 250 kHz, may of the advantages of higher-frequency operation are lost.

Figure 23 : Deadtime and Maximum Obtainable Duty-cycle vs. Frequency with Minimum Recommended C_T.



CIRCUIT EXAMPLES

1. OFF-LINE FLYBACK

Figure 24 shows a 25 W multiple-output off-line flyback regulator controlled with the UC3842. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below.

SPECIFICATIONS :

Line Isolation : 3750 V

Switching Frequency : 40 kHz

Efficiency @ full load : 70 %

Input Voltage 95 VAC to 130 VAC (50Hz/60Hz)

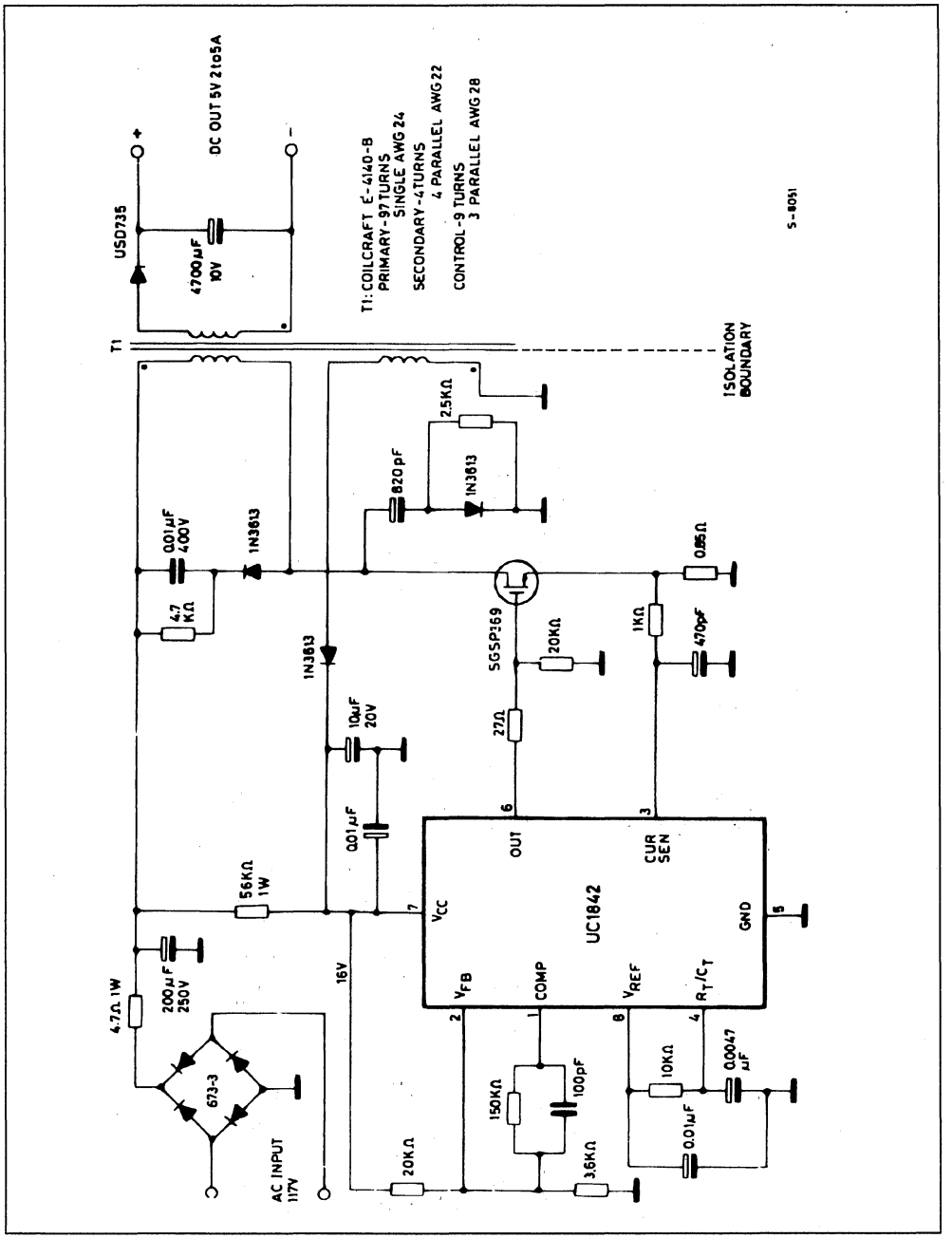
Output Voltage :

A. + 5 V, 5 % : 1 A to 4 A load
Ripple voltage : 50 mV
P-P Max.

B. + 12 V, 3 % : 0.1 A to 0.3 A load
Ripple voltage : 100 mV
P-P Max

C. – 12 V, 3 % 0.1 A to 0.3 A load
Ripple voltage : 100 mV
P-P Max

Figure 24 : 25W off-line Flyback Regulator.



A 25W OFF-LINE FLYBACK SWITCHING REGULATOR

INTRODUCTION

This note describes a low cost switching power supply for applications requiring multiple output voltages, e.g. personal computers, instruments, etc... The discontinuous mode flyback regulator used in this application provides good voltage tracking between outputs, which allows the use of primary side voltage sensing. This sensing technique reduces costs by eliminating the need for an isolated secondary feedback loop.

The low cost, (8 pin) UC1842 current mode control chip employed in this power supply provides performance advantages such as :

1) Fast transient response
2) Pulse by pulse current limiting
3) Stable operation

To simplify drive circuit requirements, a TO-220 power MOS SGSP369 is utilized for the power switch. This switch is driven directly from the output of the control chip.

POWER SUPPLY SPECIFICATIONS

1. Input voltage : 95VAC to 130VAC (50 Hz/60 Hz)
2. Output voltage :
   A. + 5 V, ± 5 % : 1 A to 4 A load
   Ripple voltage : 50 mV P-P Max
   B. + 12 V, ± 3 % : 0.1 A to 0.3 A load
   Ripple voltage : 100 mV P-P Max
   C. – 12 V, ± 3 % : 0.1 A to 0.3 A load
   Ripple voltage : 100 mV P-P Max
3. Line Isolation : 3750 V
4. Switching Frequency : 40 KHz
5. Efficiency @ Full Load : 70 %

BASIC CIRCUIT OPERATION

The 117VAC input line voltage is rectified and smoothed to provide DC operating voltage for the circuit. When power is initially applied to the circuit, capacitor C2 charges through R2. When the voltage across C2 reaches a level of 16 V the output of IC1 is enabled, turning on power MOS Q1.

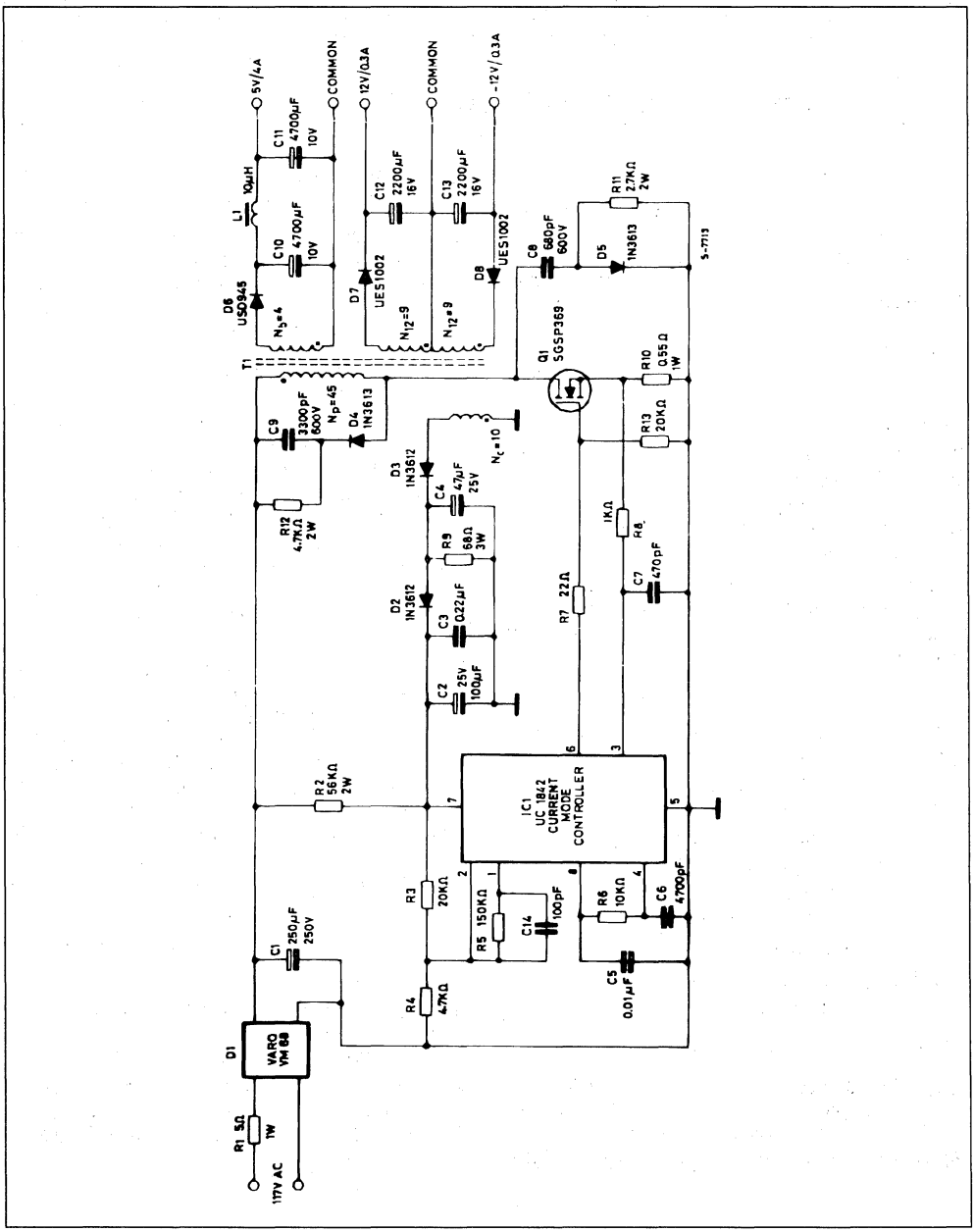
During the on time of Q1, energy is stored in the air gap of transformer (inductor) T1. At this time the polarity of the output windings is such that all output rectifiers are reverse biased and no energy is transferred. Primary current is sensed by a resistor, R10, and compared to a fixed 1 V reference inside IC1. When this level is reached, Q1 is turned off and the polarity of all transformer windings reverses, forward biasing the output rectifiers. All the energy stored is now transferred to the output capacitors. Many cycles of this store/release action are needed to charge the outputs to their respective voltages. Note that C2 must have enough energy stored initially to keep the control circuitry operating until C4 is charged to a level of approximately 13 V. The voltage across C4 is fed through a voltage divider to the error amplifier (pin 2) and compared to an internal 2.5 V reference.

Energy stored in the leakage inductance of T1 causes a voltage spike which be added to the normal reset voltage across T1 when Q1 turns off. The clamp consisting of D4, C9 and R12 limits this voltage excursion from exceeding the BVDSS rating of Q1. In addition, a turn-off snubber made up of D5, C8 and R11 keeps power dissipation in Q1 low by delaying the voltage rise until drain current has decreased from its peak value. This snubber also damps out any ringing which may occur due to parasitics.

Less than 3.5 % line and load regulation is achieved by loading the output of the control winding Nc, with R9. This resistor dissipates the leakage energy associated with this winding. Note that R9 must be isolated from R2 with diode D2, otherwise C2 could not charge to the 16 V necessary for initial start-up.

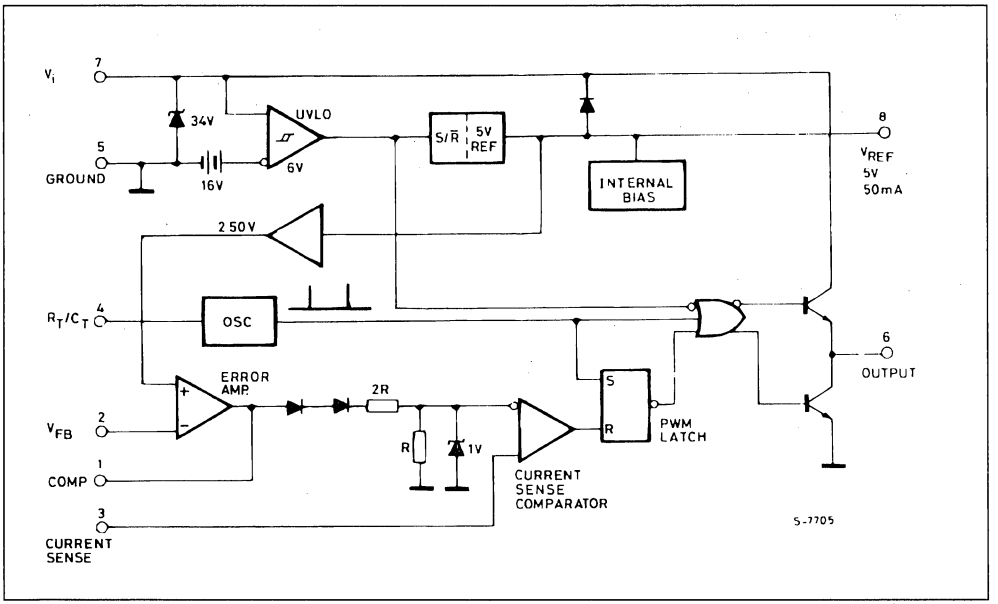
A small filter inductor in the 5 V secondary is added to reduce output ripple voltage to less than 50 mV. This inductor also attenuates any high frequency noise.

Figure 1 : 25W Off-line Flyback Regulator.

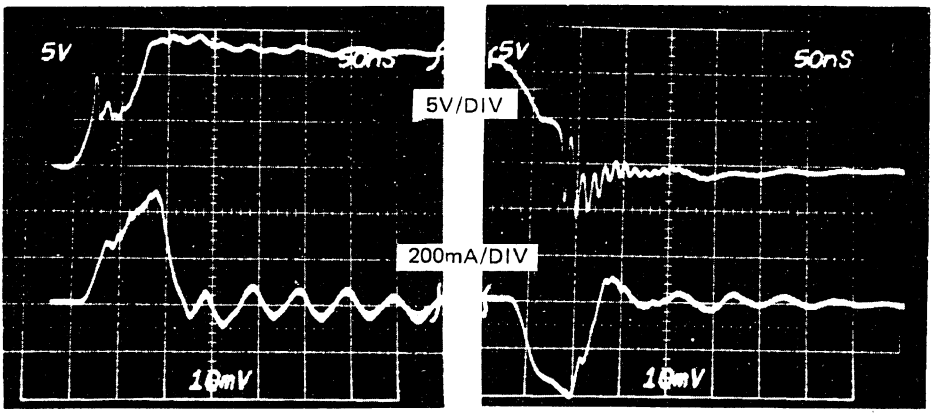


Notes : 1. All resistors are 1/4 W unless noted.
2. See appendix for construction details.
3. L1 = Ferroxcube 204T50-3C8 (Toroid), N° turns : 4, Wire Gauge : 1 mm. (18 AWG).

Figure 2 : Block Diagram : UC1842 Current Mode Controller.

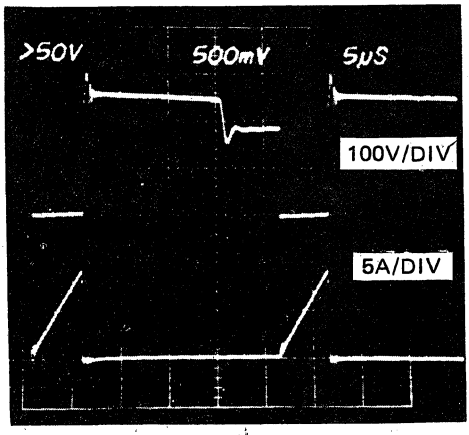


TYPICAL SWITCHING WAVEFORMS

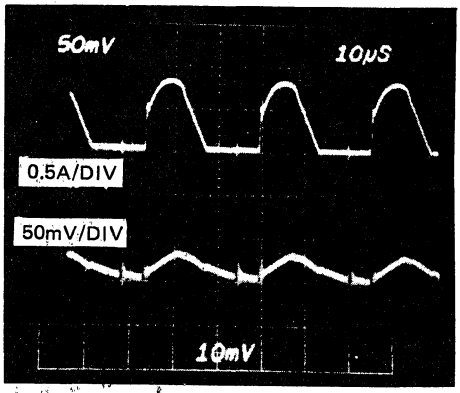


Upper trace : Q1 - Gate to source voltage
Lower trace : Q1 - Gate Current

TYPICAL SWITCHING WAVEFORMS



Upper trace : Q1 - Drain to source voltage
Lower trace : Primary current - I_D



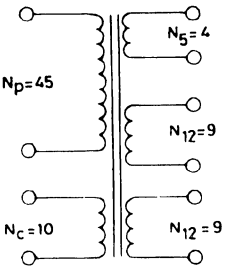
Upper trace : + 5V charging current
Lower trace : + 5V output ripple voltage

PERFORMANCE DATA

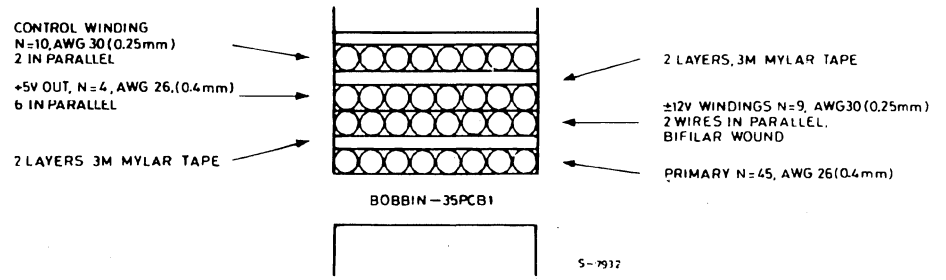
Conditions		5 V out	12 V out	– 12 V out
Low Line (95 VAC)				
± 12 @ 100 mA	+ 5 V @ 1.0 A	5.211	12.05	– 12.01
	4.0 A	4.854	12.19	– 12.14
± 12 @ 300 mA				
	+ 5 V @ 1.0 A	5.199	11.73	– 11.69
	4.0 A	4.950	11.68	– 11.63
Nominal Line (120 VAC)				
± 12 @ 100 mA	+ 5 V @ 1.0 A	5.220	12.07	– 12.03
	4.0 A	4.875	12.23	– 12.18
± 12 @ 300 mA	+ 5 V @ 1.0 A	5.208	11.73	– 11.68
	4.0 A	4.906	11.67	– 11.62
High Line (130 VAC)				
± 12 @ 100 mA	+ 5 V @ 1.0 A	5.207	12.06	– 12.02
	4.0 A	4.855	12.21	– 12.15
± 12 V @ 300 mA	+ 5 V @ 1.0 A	5.200	11.71	– 11.67
	4.0 A	4.902	11.66	11.61
Overall Line and Load Regulation		± 3.5 %	± 2.3 %	± 2.4 %

APPENDIX POWER TRANSFORMER - T1

Core : Ferroxcube EC-35/3C8
Gap : 0.25mm. in each outer leg
Note : For reduced EMI put gap in center leg only.
Use 0.5mm.



TRANSFORMER CONSTRUCTION



FLEXIBLE LOW COST HIGH EFFICIENCY 130W SMPS USING SGSD00055 AND TEA2018A

By R. LETOR - S. FLERES

ABSTRACT

A low cost, high efficiency, flexible and reliable 130W flyback power supply has been designed using the new Fastswitch high voltage Darlington SGSD00055 and the TEA2018A PWM controller.

The advantages of the new Darlington are low cost together with low switching and driving losses, a large safe operating area and simple drive requirements.

The TEA2018A provides the SMPS with comprehensive protection whilst using very few components.

The low cost of this design makes it a viable option for use in personal computers, telecommunication equipment, battery chargers and TVs.

The example evaluated in this paper is intended for CTV applications.

INTRODUCTION

The SGSD00055 is a new 1000V Darlington designed in high voltage planar technology.

The main features of this device are fast switching capability, large reverse safe operating area and very low cost.

This high efficiency 130W flyback SMPS capitalises on the features of this transistor to produce a highly reliable power supply.

By adding to this the facilities offered by the TEA2018A, significant component reduction can be made whilst retaining all the desirable features.

The high voltage that the Darlington can withstand plus the large safe operating area allows the use of a low cost transformer with high leakage inductance.

The leakage inductance of a low cost transformer is likely to produce voltage spikes in excess of 850V at turn-off, a voltage that standard Darlingtons are unlikely to be able to handle.

An added advantage of this high voltage capability is that smaller snubber networks can be used giving reduced dissipation in these networks.

The switch mode power supply characteristics are summarised in the following table :

Operating mode :	non continuous flyback	
A.C. input voltage :	110/220V	± 15%
Maximum frequency :	25kHz	
Maximum output power :	130W	
Outputs :	+ 200V	50mA
	+ 150V	500mA
	+ 25V	1.5mA
	+ 16V	500mA
Line regulation :	.016%/V	
Load regulation :	.035%/W	
110W efficiency :	82%	

CIRCUIT DESCRIPTION

Figure 1 shows the complete circuit and component list.

The rectified mains voltage applied to the primary of the flyback transformer is switched at 20KHz by the Darlington Q1 with a duty cycle of about 30%.

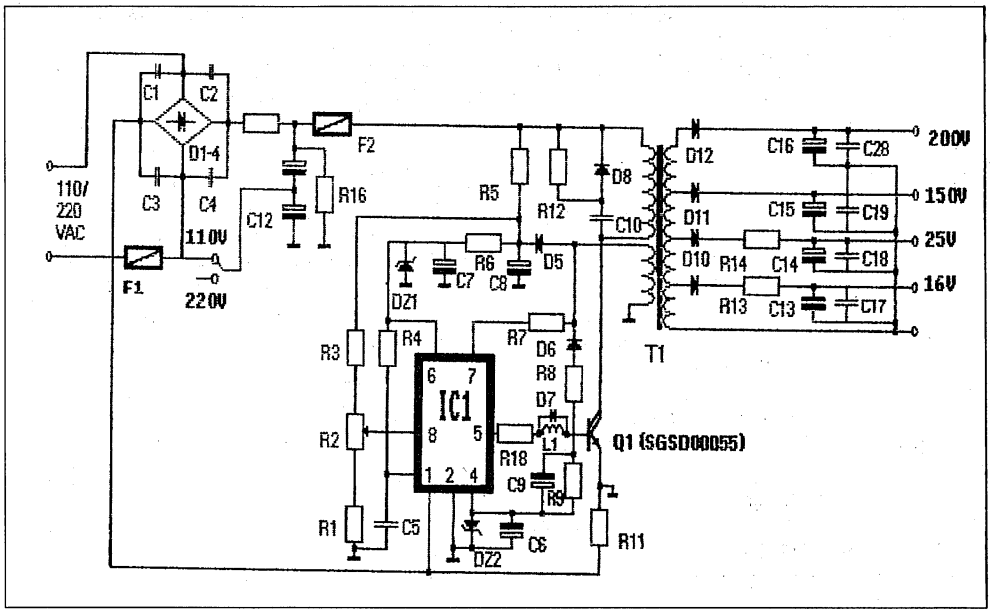
During the on-state the base current value depends upon the collector current, the TEA2018A performing the proportional base drive.

The negative voltage necessary for the turn-off is provided by the D6, R8, R9, C9 network, which charges the C6 capacitor during the on-state.

At turn-off, the inductor L1 limits the reverse base current and prevents the turn-off from being too fast hence reducing any "tail turn-off" problem.

The snubber network R12, C10, D8 ensures safe switch off inside the safe operating area and very low switching losses at turn-off.

Figure 1 : 130W SMPS Using SGSD00055.



COMPONENT LIST

R1	1K	1/4W
R2 trimmer	22K	
R3	1K	1/4W
R4	56K	1/4W
R5	100K	1W
R6	220K	2W
R7	10K	1/4W
R8	10	1W
R9	470	2W
R10	2.7	1/2W
R11	0.33	2W
R12	2.2K	7W
R13	1	2W
R14	0.75	4W
R15	4	4W
R16	100K	1/2W
L1	4.7µH	
C1 - C4	1nF	1kV
C5	680pF	1kV
C6	4.7µF	6.3V
C7	100µF	16V

C8	100µF	25V
C9	4.7µF	6.3V
C10	1.8nF	1kV
C11 - C12	220µF	250V
C13 - C14	220µF	63V EKA
C15	10µF	250V
C16	10µF	300V
DZ1	10V	1W
DZ2	4.7V	1/2W
D1 - D4	2A 250V	Rectifier Bridge
D5	1N4001	
D6	BA157	
D7	1N4148	
D8	BYT13-800	
D9 - D10	BYW98	
D11- - D12	BY299	
Q1	SGSD00055	
IC1	TEA2018A	
T1	SAREA 29.6024	
F1	0.5 A FUSE	
F2	0.5 A FUSE	

Figure 2 shows the power losses in the Darlington and in R12 as C10 is varied.

The minimum power losses occur when C10 has a value of 1.0nF.

In fact a value of 1.8nF was used in order to give a sufficient safety margin at turn-off.

In this way a 1W reduction of the power losses in the Darlington was obtained (see figure 3).

This in turn reduced the working temperature with a consequent improvement in reliability. To obtain the same safety margin with a 850V Darlington a 2.2nF capacitor would have to be used for C10.

Figure 2 : Power Losses vs $C_{Snubber}$.

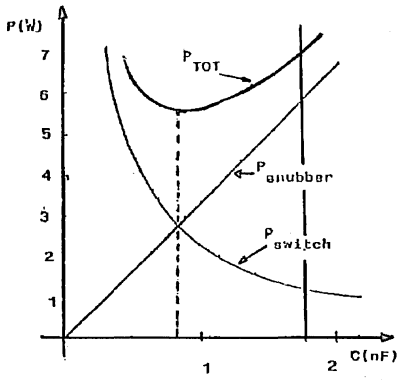


Figure 4 shows the short circuit conditions both with and without the demagnetisation control. During normal operation the maximum current is limited by the current mode control.

When a short circuit occurs without the demagnetisation circuit, the collector current increases until the transformer core is saturated.

This happens because collector current continues increasing even after the current limiter intervenes due to the storage current, at a rate 0.25A/µS.

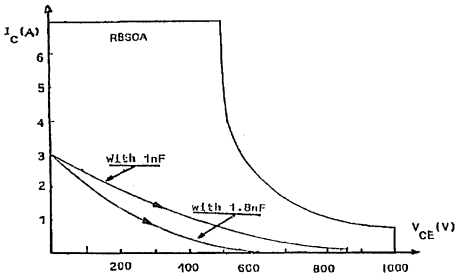
Hence the energy stored in the transformer core during $t_{storage}$ eaches a value of about 50µJ, while during the discharge cycle the energy reduces to about 3µJ.

This would result in higher losses. Using the 1000V Darlington permits the use of a cheaper "lossy" transformer as the Darlington itself will withstand the higher voltage peaks caused by a leakage inductance 4 times greater than the peak that a 850V Darlington can withstand.

The TEA2018A demagnetisation circuit allows the following features to be designed into the circuit :

- non-continuous flyback mode for all load conditions
- soft start
- short circuit protection

Figure 3 : Load Line Shape at Turn-off.



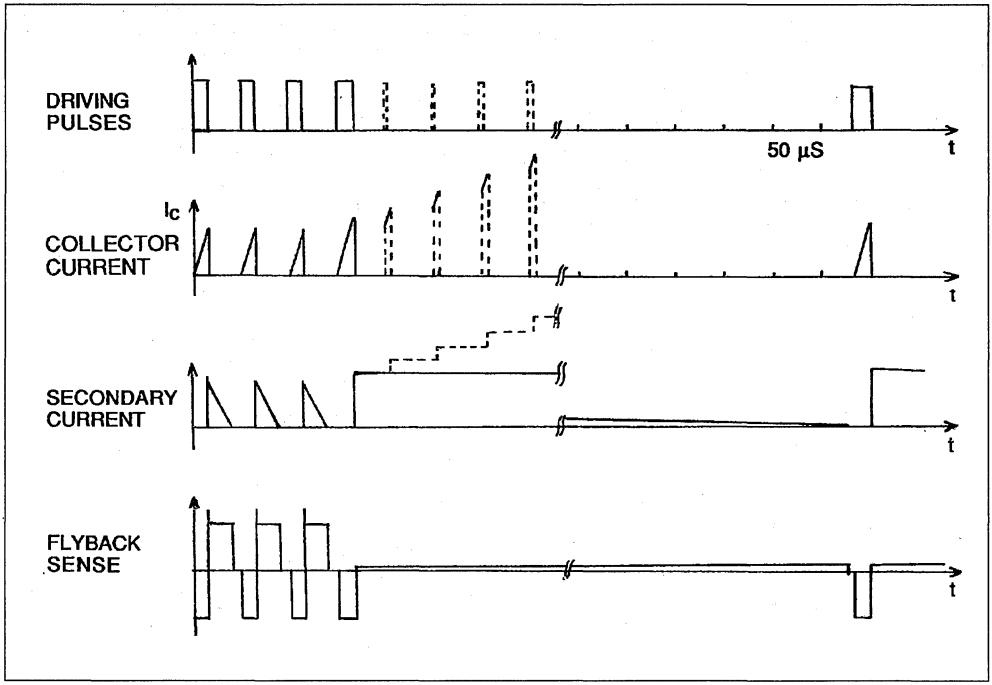
In this application the demagnetisation circuit inhibits the base drive until all the stored energy in the core of the transformer has been discharged through the diode, the secondary winding and the short circuit resistances.

The demagnetisation current behaves in the same way during start-up avoiding extra currents.

It also ensures non-continuous mode operation under every load condition.

The following figures and photographs illustrate the performance of this power supply.

Figure 4 : Short Circuit Operation.



---------	without demagnetisation circuit
———	with demagnetisation circuit

Figure 5a : Efficiency versus Output Power.

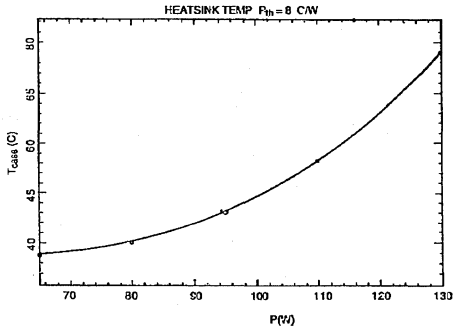
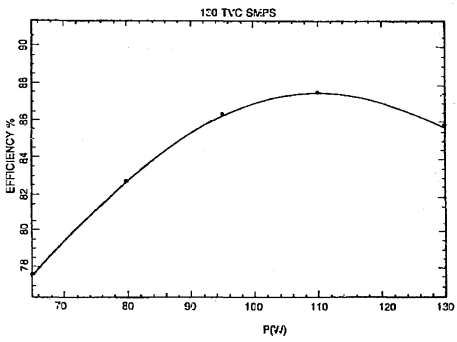
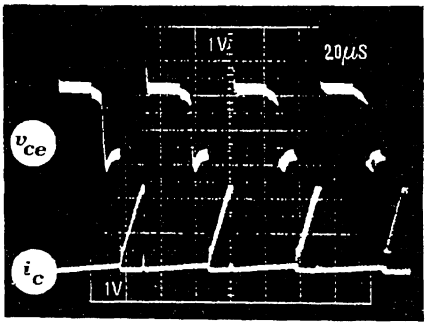


Figure 5b : Heatsink Temperature versus Output Power for R_{th} (heatsink) 8°C/W.

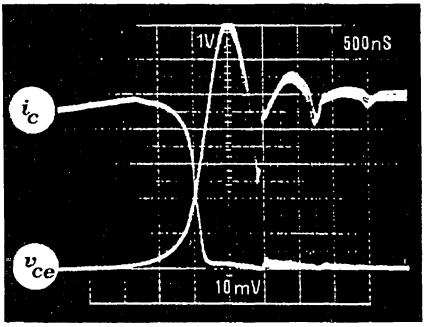


Photograph 1 : Collector Voltage and Current Waveforms.



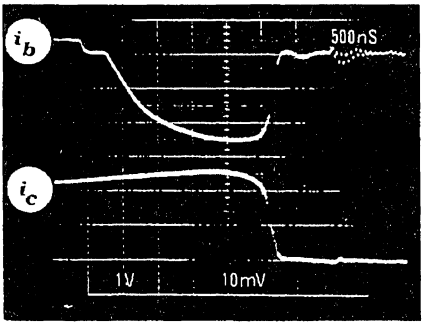
I_C = 1A/div V_{CE} = 100V/div V_{CC} = 250V

Photograph 2 : Turn-off Waveforms.



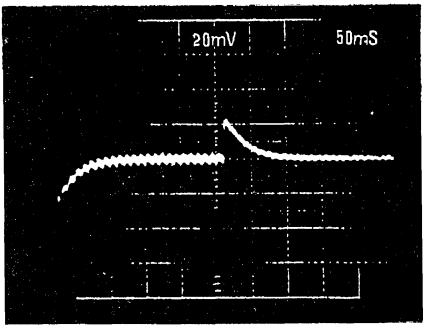
I_C = 0.5A/div V_{CE} = 100V/div

Photograph 3 : Collector and Base Current at Turn-off.



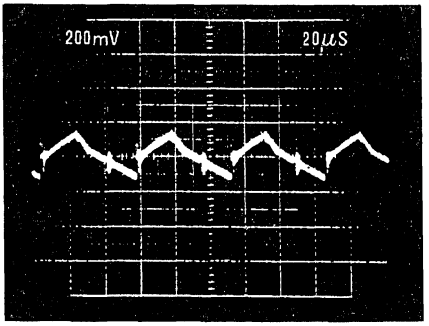
I_C = 1A/div I_B = 0.2A/div

Photograph 4 : Transient Response to a step Load



V = 2V/div

Photograph 5 : Output Ripple on the 25V Output.



V= 200mV/div I = 1.5A

CONCLUSIONS

The new 1000V Darlington allows the construction of a flexible, reliable and low cost switching power supply.

It has a high efficiency even at low loads due to the very low driving energy required, the low switching losses and the reduced snubber losses.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

A SECOND-GENERATION IC SWITCH MODE CONTROLLER OPTIMIZED FOR HIGH FREQUENCY POWER MOS DRIVE

INTRODUCTION

Since the introduction of the SG1524 in 1976, integrated circuit controllers have played an important role in the rapid development and exploitation of high-efficiency switching power supply technology. The 1524 soon became an industry standard and was widely second-sourced.

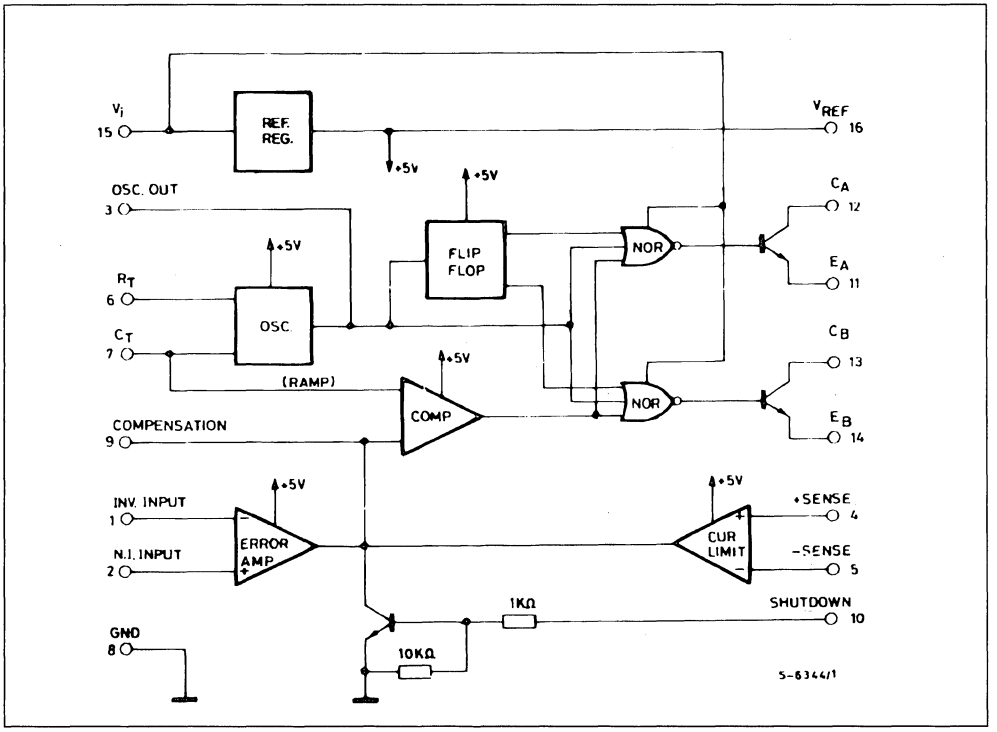
Although this device contained all the basic control elements required for switching regulator design, practical power supplies still required other functions which had to be implemented with additional external discrete circuitry.

An additional development within the semiconductor industry was the introduction of practical Power Mos which offered the potential of higher efficiencies at higher speeds with resultant lower overall system costs.

In order to be able to take full advantage of the speed capabilities of power MOS, it was necessary to provide high peak currents to the gate during turn-on and turn-off to quickly charge and discharge the gate capacitances of 800 to 2000 pF present in higher current units.

The development of a second-generation regulating PWM IC, the SG1525A, and its complimentary output version, the SG1527A, was a direct result of the desire to add more power supply elements to the control IC,

Figure 1 : The SG1524 relating PWM block diagram.
This design was the first complete I.C. control chip for switch mode power supplies.



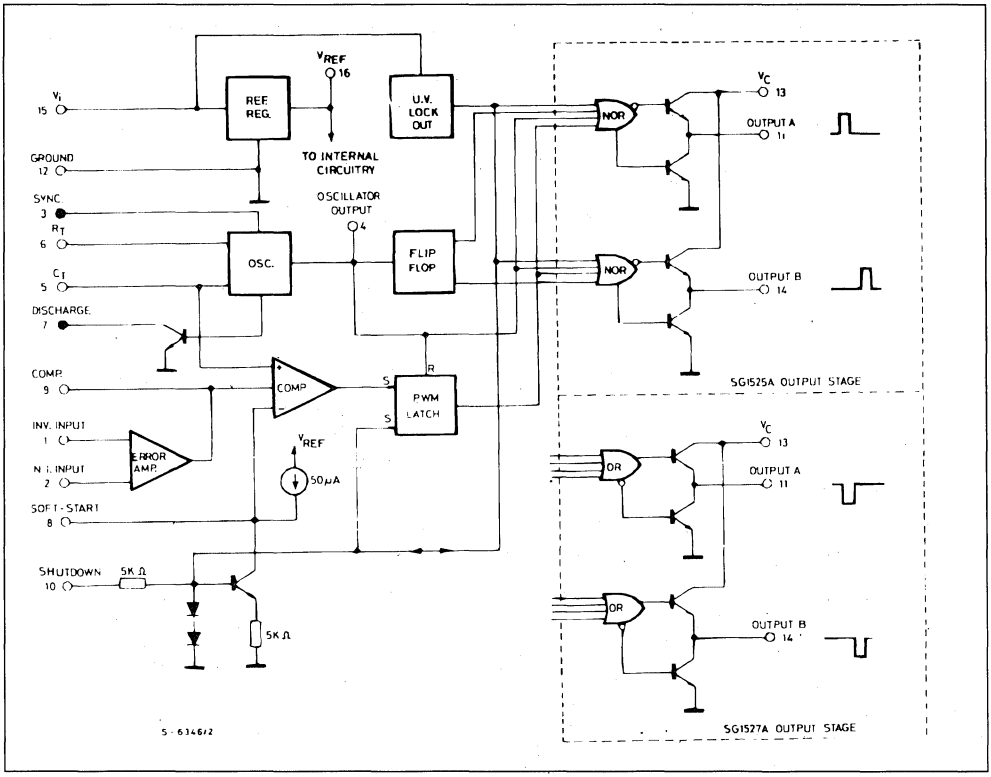
as well as to optimize the interfacing of high current power devices.

INTEGRATING MORE POWER SUPPLY FUNCTIONS

Having achieved the greatest level of acceptance among users of first generation control chips, the 1524 became the starting point for expanding IC controller capabilities. This early device, shown in figure 1, contains a fixed-voltage reference source, an oscillator which generates both a clock signal and a linear ramp waveform, a PWM comparator, and a toggle flip-flop with output gating to switch the PWM signal alternately between the two outputs.

With this circuitry already defined, a two pronged development effort was initiated : 1) to add additional features required by most power supply designs and 2) to improve the utility of features already included within the 1524. The resultant block diagram for the SG1525A is shown in figure 2. Two general comments should be made relative to the overall block diagram. First, in optimizing the output stage for bi-directional, low impedance switching, commitments had to be made as to whether the output should be high or low during the active, or ON state. Since this is application defined there are needs for both output states, so both were developed with the SG1525A device defined by an output configuration which is high during the ON pulse, and the SG1527A configured to remain high during the OFF state. This difference is implemented by a mask option which eliminates inverter Q_4 (see figure 3) for the SG1527A. In all other respects, the 1525A and 1527A are identical and any description of the 1525A characteristics apply equally to the 1527A. Second, a major difference between this new controller and the earlier 1524 is the deletion of the current limit amplifier. There are so many system considerations in providing current control that it is preferable to leave this as a user-defined external option and allocate the package pins to other, more universally requested functions. Current limiting possibilities are discussed further under shutdown options.

Figure 2 : The SG1525A family represents a "second generation" of IC controllers.

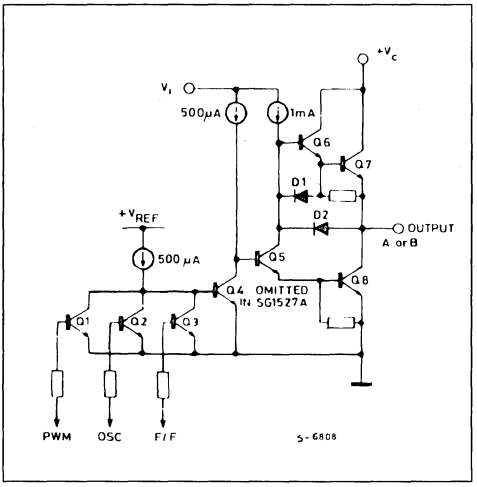


"TOTEM-POLE" OUTPUT STAGE

One of the most significant benefits in using the SG1525A is its output configuration. For the first time it has been recognized in an IC controller that it is more difficult to turn a power switch off than turn it on. With the SG1525A, a high-current, fast transition, low impedance drive is provided for both turn-on and turn-off of an external power transistor or Power MOS. The circuit schematic of one of the two output stages contained within the device is shown in figure 3. This is a two-state output, either Q_8 is on, forming a low saturation voltage pull-down, or Q_7 is on, pulling the output up to V_C. Note that V_C is a separate terminal from the V_i supply to the rest of the device.

This offers the benefits of potentially operating the output drive from a lower supply than the rest of the circuit for power efficiencies, decoupling of drive transients from more sensitive circuits, and a third terminal for extracting a drive signal. Note that even though V_C can be set either higher or lower than V_i, the output cannot rise higher than approximately 1 1/2 volts below V_i.

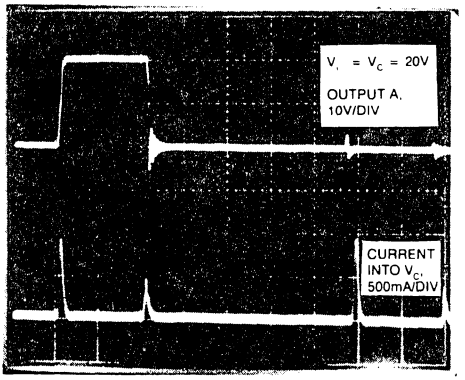
Figure 3 : One of Two Power Output Stages Contained within the SG1525A which Conduct Alternately due to the Internal Flip-flop.



During the transition between states, there is a slight conduction overlap between source and sink which results in a pulse of current flowing from V_C to ground. However, due to the high-speed design configuration of this stage, this current spike lasts for only about 100ns. A typical current waveform at V_C is shown in figure 4. This transient will normally be decoupled from the rest of the control power by a 0.1 µF capacitor from V_C to ground but it should not, otherwise, cause a problem unless very high frequency operation is contemplated where it will contribute to overall device power dissipation, by becoming a significant portion of the total duty cycle.

The output saturation characteristics of this stage are shown in figure 5. The source transistor, Q_7 is a straight forward Darlington and its saturation voltage remains between 1 and 2 V out to 400 mA under the assumption that $V_i \geq V_{CC}$. The sink transistor, Q_8, however, has a non-uniform characteristic which needs explanation. At low sink currents, the 1 mA current source through Q_5 insures a very low saturation voltage at the output. As load current increases past 50 mA, Q_8 begins to come out of saturation for lack of base drive but only up to about 2 V. Here diode D_2 becomes forward biased shunting a portion of the load current through Q_5 to boost the base current into Q_8. With this circuit, the sink transistor can both support high peak discharge currents from a capacitive load, as well as insure the low static hold-off voltage required for bipolar transistors.

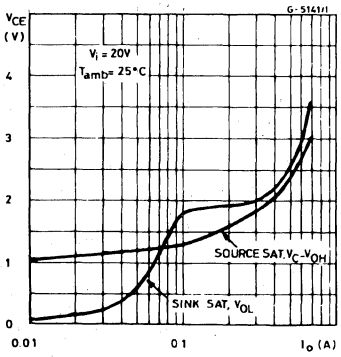
Figure 4 : Current "spiking" on the V_C terminal caused by conduction overlap between source and sink is minimized by high-speed design techniques.



HORIZONTAL = 500ns/DIV

A typical output configuration for a push-pull bipolar transistor power stage is shown in fig. 6. With a steady state base drive current from the SG1525A of 100 mA, this stage should be able to switch 1 to 5 A of transformer primary current, depending upon the choice of transistors. The sum of R_1 and R_2

Figure 5 : The output saturation characteristics of the SG1525A provide both high drive current an low hold-off voltage.



determine the maximum steady state output current of the SG1525A while their ratio defines the voltage across C_2 which, at turn off, becomes the reverse V_{BE} for Q_1. With the values given, the output current and voltage waveforms are shown in figure 7 for a one microsecond pulse. If power MOS are used for the output switches as shown in figure 8, the interfacing circuitry can become even simpler with only a small series gate resistor potentially required to damp spurious oscillations within the power device.

Figure 6 : A Typical Push-pull Converter Power Stage Using External Bipolar Power Transistor Switches

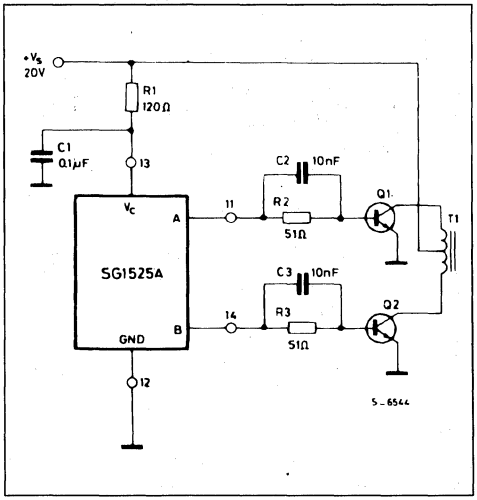
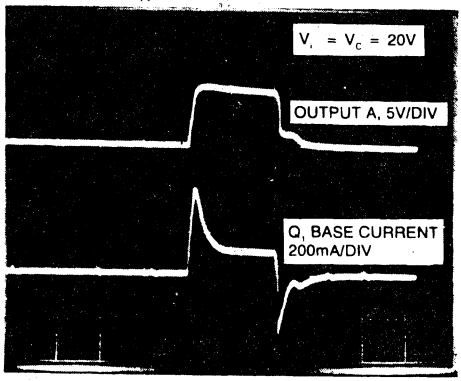


Figure 7 : Base current waveforms (figure 6 circuit) show the enhanced turn-on and turn-off current possible with the SG1525A.



HORIZONTAL = 500ns/DIV

Push-pull direct transformer drive is also particularly advantageous with SG1525A as shown in figure 9. A version of this configuration is required for isolation when the control circuit is referenced to the secondary side of an off-line power system, and to provide level shifting of drive signals for bridge and full bridge switching. The configuration of figure 9 has a couple of important advantages. First, by connecting the drive transformer primary directly between the outputs of the SG1525A, no center-tap is needed and the full primary is driven with opposite polarities. Secondly, between each output pulse, both outputs are pulled to ground which effectively shorts the two ends of the primary winding together coupling a low-impedance turn-off signal to the switching transistors.

A useful single-ended configuration, typical of buck regulators, is shown in figure 10. Here the SG1525A outputs are grounded and the PWM signal is taken from the V_C terminal which switches close to ground during each clock period as the internal source transistors are alternately sequenced.

Figure 8 : Replacing bipolar transistors with power MOS provides even greater simplicity due to the low driving impedances of the SG1525A in each transition.

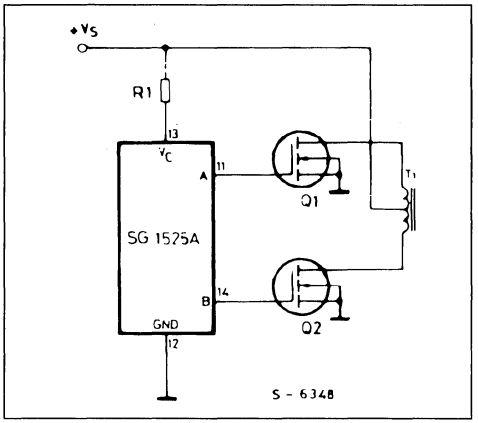


Figure 9 : The SG1525A is ideally suited for driving a low-power base drive transformer and eliminates the need for a primary center-tap.

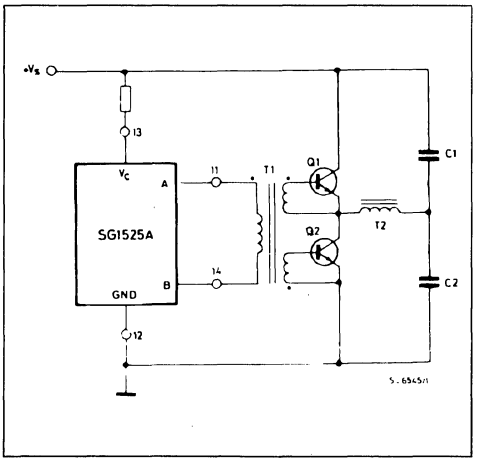
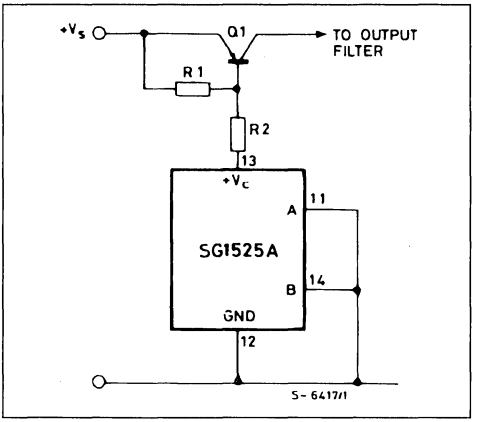


Figure 10 : A single-ended Ground-referenced Power Stage for a Flyback or Boost Regulator.



CONTROLLING POWER SUPPLY START-UP

Although the advantages of the SG1525A's output stage will often be reason enough for its selection, there are several other important and useful features incorporated within this product. One problem previously overlooked in PWM circuits is keeping the output under control as the supply voltage is turned on and off. Undefined states, particularly the possibility of turning on an output before the oscillator is running, can be quite awkward, if not catastrophic. To prevent this, the SG1525A has incorporated an under-voltage lockout circuit which effectively clamps the outputs to the off state with as little as 2 1/2 V of supply voltage which is less than the vol-tage required to turn the outputs on. This clamp is maintained until the supply reaches approximately 8 V insuring that all the remaining SG1525A circuitry is fully operational prior to enabling the outputs. The clamp reactivates when the supply is lowered to approximately 7.5 V. There is about 500 mV of hysteresis built in to eliminate clamp oscillation at threshold.

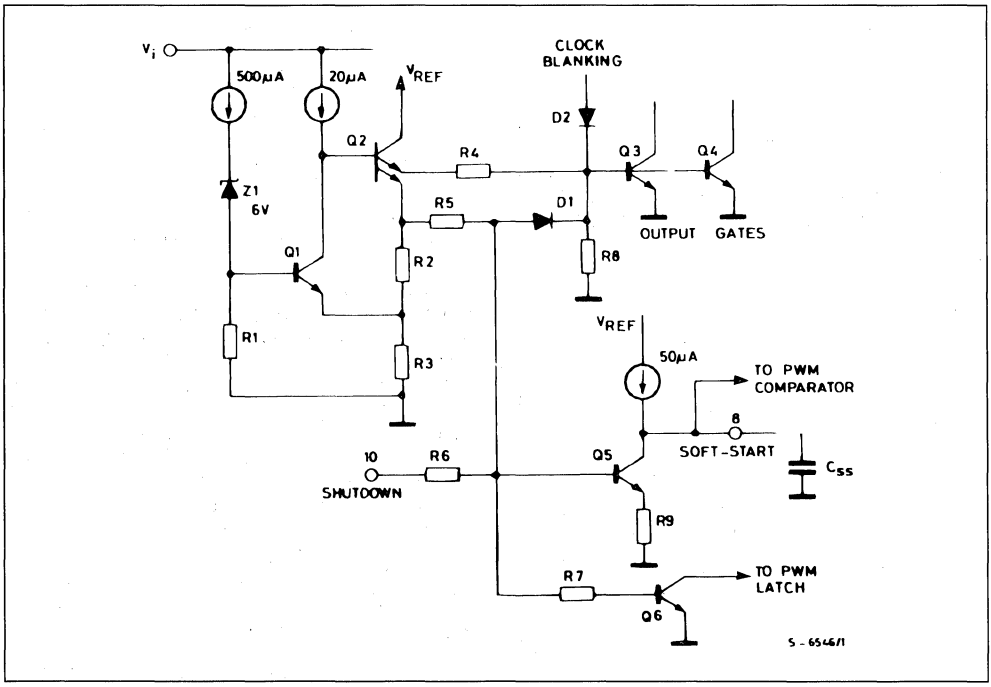
Another important aspect of power sequencing is restraining the outputs from immediately commanding a 100 % duty cycle when they are activated. This is accomplished by a slow turn on (soft-start) which is defined by an internal 50 µA current source in conjunction with an externally applied capacitor. The details of this power sequencing system are shown in figure 11.

Q_3 and Q_4 are the output gates normally driven by the oscillator through D_2 to provide output blanking between pulses. (One of these transistors is shown as Q_2 in figure 3). At low supply voltages, Q_2 conducts with base drive from the 20 µA current source. Q_2 provides three functions. First, current through R_4 activates the output gates with minimum voltage drop. Second, current through R_5 activates the shutdown transistor Q_5 holding the soft-start capacitor, C_{SS}, discharged. Third, R_2 provides a small bucking voltage across R_3 for hysteresis at the switch point.

When the input voltage becomes high enough to provide a little more than one volt at the base of Q_1, that transistor turns on. This turns off Q_2, activating the outputs and allowing C_{SS} to begin to charge from the internal 50 µA current source. The time to reach approximately 50 % duty cycle will be

$$t = \left(\frac{2 \text{ volts}}{50\ \mu A}\right) C_{SS}$$

Figure 11 : The Internal Power Turn-on, Soft-start, and Shutdown Circuitry of the SG1525A.



POWER SUPPLY SHUTDOWN

An important part of any PWM controller is the ability to shut it down at any time for a variety of reasons, including system sequencing requirements or fault protection. Several options are available to the user of the SG1525A, which require an understanding of the capability of the shutdown terminal, pin 10. Referring to figure 11, the base of Q_5 is turned on by a signal which is clamped to approximately 1.4 V by the action of D_1 and the V_{BE} of gates Q_3 and Q_4. This holds the outputs off and keeps C_{SS} discharged by Q_5 which, with R_9, becomes a 100 µA net current sink.

If, during normal operation, pin 10 is pulled high, three things happen. First, the outputs are turned off within 200 ns through D_1. Second, the PWM latch is set by Q_6 so that even if the signal at pin 10 were to disappear, the outputs would stay off for the duration of that period, being reset by the next clock pulse. Third, Q_5 is activated commencing a 100 µA

discharge of C_{SS}. However, if the activation pulse on pin 10 has a duration shorter than 1/3 of the clock period, the voltage on C_{SS} will remain high and soft-start will not be reactivated. Naturally, a fixed signal on pin 10 will eventually discharge C_{SS}, recycling soft-start.

Thus, the shutdown pin provides both sequencing capability as well as a convenient port for protective functions, including pulse-by-pulse current limiting.

REGULATING PWM PERFORMANCE IMPROVEMENTS

The SG1525A also offers significant performance and application improvements in almost all of the additional basic functions of a PWM over those obtainable with earlier devices. A general description of these features is outlined below :

REFERENCE REGULATOR

The output voltage of this regulator is internally trimmed to 5.1 V ± 1 % during manufacture, eliminating the need for adjusting potentiometers in most applications.

ERROR AMPLIFIER

SG1525A uses the same basic transconductance amplifier as the SG1524 with an important difference : it is powered by V_i rather than V_{REF}. Now the input common-mode range includes V_{REF} eliminating the need for a voltage divider with its attendant tolerances. An additional feature relative to the error amplifier is that the shutdown circuitry feeds into a separate input to the PWM comparator allowing pulse termination without affecting the output of the error amplifier which might have a slow recovery, depending upon the external compensation network selected. An important benefit of a transconductance amplifier is the ease with which its current mode output can be over-ridden by other external controlling signals.

PWM COMPARATOR

The significant benefit of the SG1525A's PWM comparator is in its following latch. A common problem with earlier devices was that any noise or ringing on the output of the error amplifier would affect multiple crossings of the oscillator ramp signal resulting in multiple pulsing at the comparator's output. The SG1525A's latch terminates the output pulse with the first signal from the comparator, insuring that there can be only a single pulse per period, removing all jitter or threshold oscillation from the system. Another important advantage of this latch is the ability to easily implement digital or pulse-by-pulse current limiting by merely momenetarily activating the shutdown circuitry within the SG1525A. This could be as simple as connecting pin 10 to a ground-referenced current sensing resistor. For greater accuracy, some added gain may be advantageous. Once a current signal causes shutdown, the output will remain terminated for the duration of the period, even though the current signal is now gone. An oscillator clock signal resets the latch to start each period anew.

OSCILLATOR

The functions of the oscillator within the SG1525A have been broadened in two important aspects. One is the addition of a synchronization terminal, pin 3, allowing much easier interfacing to an external clock signal or to synchronize multiple SG1525A's together. The other is the separation of the oscillator's discharge network from its charging current source for deadtime control. Reference should be made to the schematic of figure 12 for an understanding of the operation of this circuit. The heart of this oscillator is a double-threshold comparator, Q_7 and Q_8, which allows the timing capacitor to charge to an upper threshold by means of the current source defined by R_T and mirrored by Q_1 and Q_2. The comparator then switches to a lower threshold by turning on Q_{10} and discharges C_T through Q_3 and Q_4 with a rate defined by R_D. As long as C_T is discharging, the clock output is high, blanking the outputs.

Since the overall oscillator frequency is defined by the sum of the charge and discharge times, there are three elements now in the frequency equation which is approximately :

$$f \approx \frac{1}{C_T\,(.07\,R_T + 3\,R_D)}$$

External synchronization can easily be accomplished with a 2.8 V positive pulse at pin 3. This will turn on Q_9, lowering the comparator threshold below wherever the voltage on C_T may happen to be. Two factors should be considered : First, the voltage on C_T determines the amplitude of the PWM ramp, and if the sync occurs too early, the loop gain will be higher and the resolution may be worse. Second, the sync circuit is regenerative within 200 ns ; and, while a wider pulse can be used, C_T will not begin to recharge as long as the sync pin is high. For synchronizing multiple SG1525A devices together, one need only to define a master with the correct R_TC_T time constant, connect its output pin to the slave sync pins, and set each slave R_TC_T for a time constant 10-20 % longer than the master.

Figure 12 : A Simplified Schematic of the SG1525A's Oscillator Circuitry.

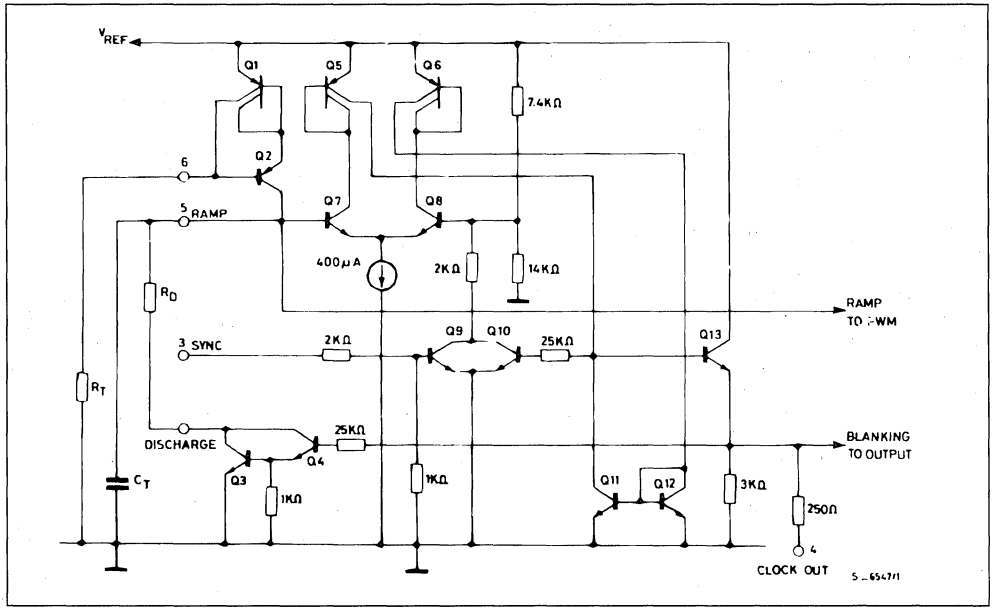
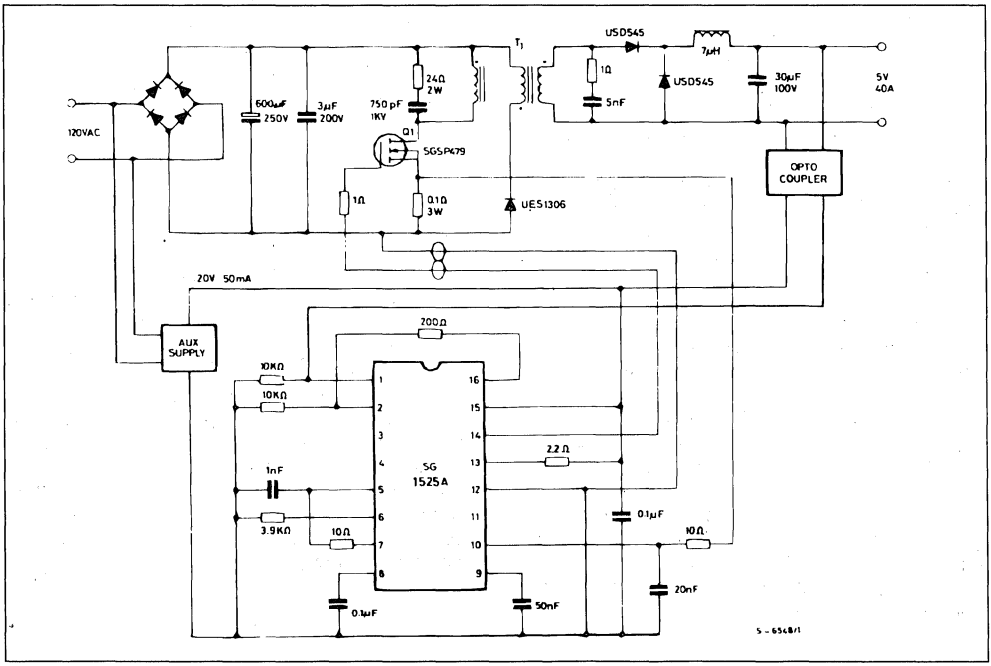


Figure 13 : 200 W, Off-line Forward Converter.

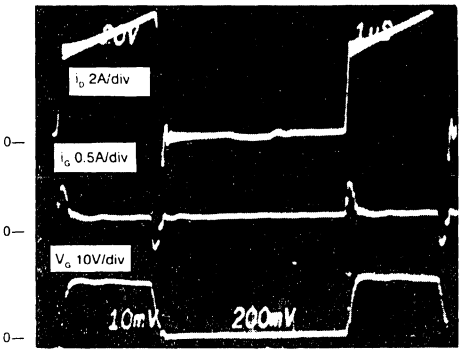


A 200 WATT, OFF-LINE, FORWARD CONVERTER

The ease of interfacing the SG1525A into a practical power supply system can be illustrated by the off-line, power converter shown in figure 13. This 200 W supply places the control circuitry on the primary side of the power transformer where direct coupling can be used to drive the power switch. While simplifying the drive electronics, this configuration usually requires an isolated voltage feedback signal which is most easily accomplished by an optocoupler driven by some type of voltage regulator IC such as a L123 or LM723. One other undefined block in figure 13 is the auxiliary power supply which supplies the low voltage, low current bias supply for the SG1525A and the drive for Q_1 the power switch. The choice of the SGSP479 power MOS for this switch keeps the total power requirements from the auxiliary supply at less than 1 W ; readily implemented with a small, line-driven transformer.

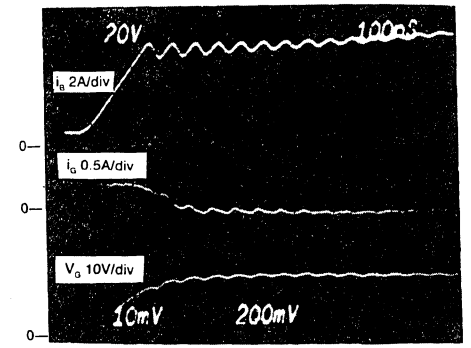
This converter is designed to operate at 150 kHz which is accomplished by running the SG1525A at 300 kHz and using only one of the outputs. This also automatically insures that the duty cycle can never be greater than 50 %, a requirement of the power transformer in this configuration. The high operating frequency allows the output filter's roll-off to be set at 12 kHz, greatly simplifying the overall loop stability considerations as adequate response can be achieved with only the single-pole compensation of the error amplifier provided by the 0.05 µF capacitor on pin 9. The totem-pole output of the SG1525A is used to advantage to drive Q_1 by providing a 400 mA peak current to charge and discharge the power MOS gate capacitance while keeping overall power dissipation low. Waveform photographs of this operation are shown in figure 14.

Figure 14 : Current and Voltage Waveforms for the 200 W Off-line Forward Converter with a SG1525A Direct Driven Power MOS Switch (operating frequency is 150 KHz with output current equal to 40 A).

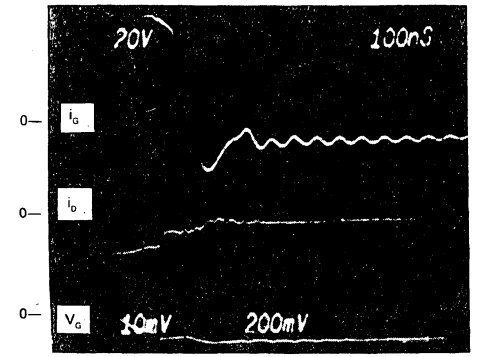


1 µs/div

a) Waveforms of I_D, I_G, V_G



b) Risetime
≈ 90 ns



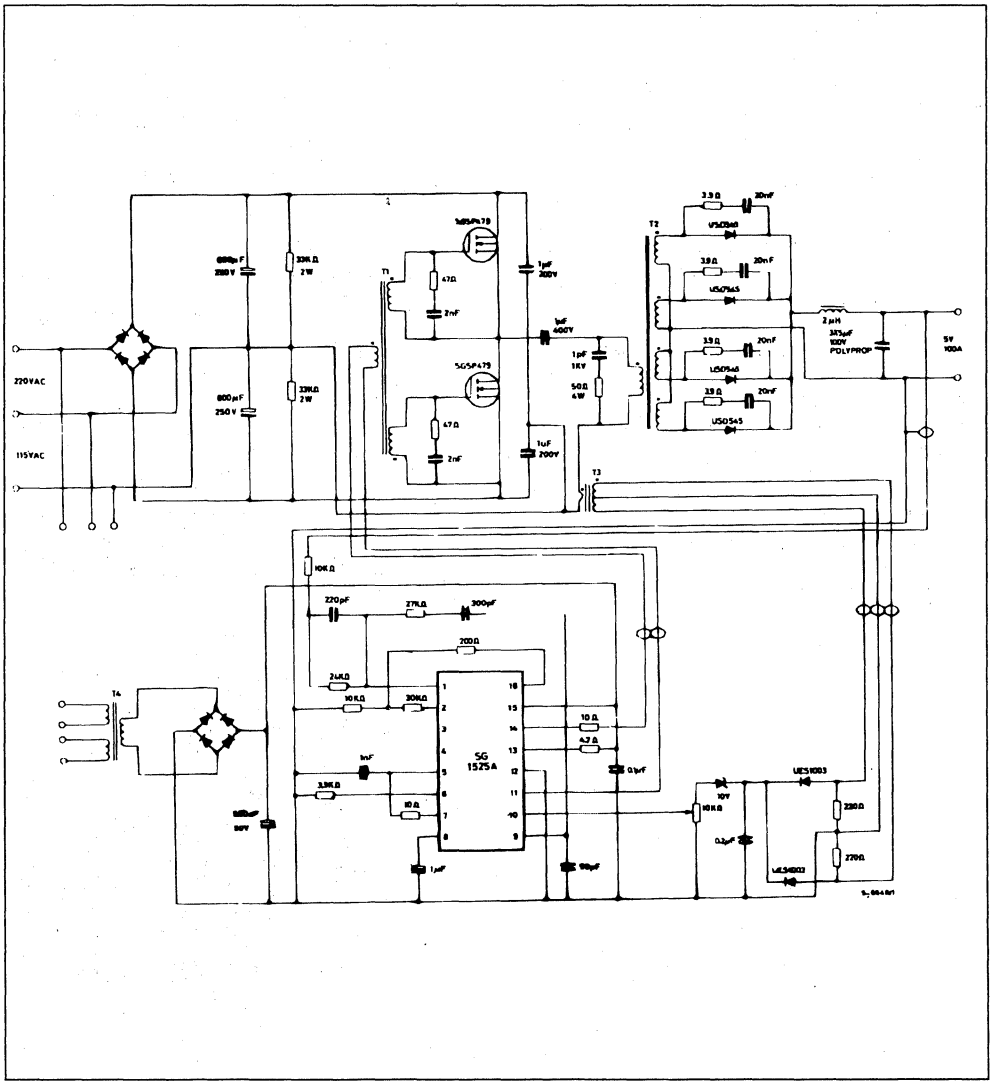
c) Falltime
≈ 30 ns

When operating at full load, the efficiency of this converter is 73 % with by far the greatest power losses occurring in the output rectifiers-even though Schottky devices have been selected.

Switching losses have been minimized by the fast current transitions, primarily defined by the leakage inductance of the transformer. Although this switching time could probably be even further reduced, there could be problems with current spikes during rise time due to Schottky rectifier capacitance.

Current limiting for this converter is provided by measuring the current in SGSP479 with the 0.1 Ω resistor in series with the source and using this voltage to activate the shutdown circuitry within the SG1525A. While this will provide a fast-acting short circuit protection on a pulse-by-pulse basis, a comparator may need to be added for a more accurate current limit threshold.

Figure 15 : 500 W, 100 kHz Half-bridge Schematic.



Transformer winding data

500 W, 100 kHz, Off-Line, Half-Bridge Converter :

T1 Core : Ferrox 486T250-3C8
Pri : 14 T #22AWG
Sec (2) : 7 T #22AWG

T2 Core : Ferrox EC52-3C8 (EE)
Pri : 14 T, 2 layers, 2 #16AWG in parallel
Sec (2) : each 2 T, C.T., copper strap 0.01" x 0.8"

T3 Core : Ferrox 486T250-3C8
Pri : 1 T
Sec : 20 T, C.T. #22AWG

T4 117 V/220 V, 25 V, 0.15 A, 50-60 Hz

L1 Core : Ferrox IF30-3C8
4 turns, 5 #12AWG in parallel

500 WATT, OFF-LINE, HALF-BRIDGE CONVERTER

The circuit shown in figure 15 uses a pair of SGSP479 power MOS in a half-bridge configuration with the SG1525A chip referenced to the secondary side of the power transformer.

The power MOS gates are driven directly from the control chip output through step down and isolation transformer T1. The SG1525A output terminals (pins 11 and 14) provide active pull-up and pull-down (dual source/sink for the primary of T1. This provides the fast, high current turn-on and turn-off pulses needed for the power MOS gates. In addition, the two ends of the primary windings are shorted to ground during deadtime, which prevents accidental turn-on by transients. Note that the current supplied by the SG1525A outputs drops to a small value when the gate capacitance has been charged or discharged to the desired gate voltage. Damping resistors with series blocking capacitors across the two secondaries of T1 minimize ringing due to the power MOS gate capacitance and the inductance of T1 and lead inductance, particularly during deadtime.

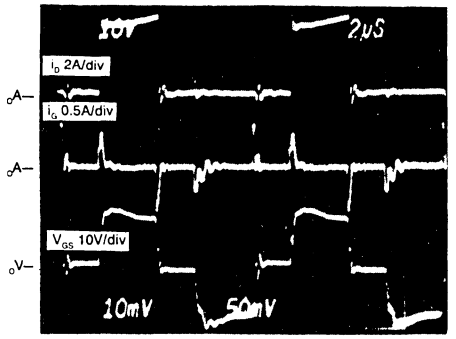
Deadtime for the SG1525A is set very simply by a single resistor between pins 5 and 7. Only a small amount of deadtime is needed since the power MOS have no storage time and a very short delay time.

Slow turn-on is accomplished by a single capacitor at pin 8.

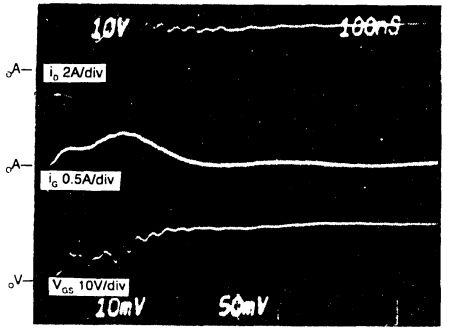
Current limiting is provided by current transformer T3 in series with the primary of the power transformer T2. The signal is rectified, threshold adjusted and sent to the shutdown terminal, pin 10, of the SG1525A.

Waveforms of the converter are shown in the scope photos of figure 16. Current rise and fall times are 20 ns and 10 ns.

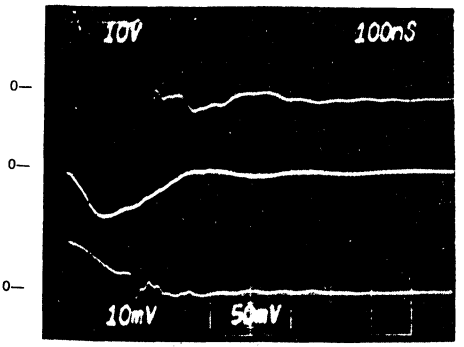
Figure 16 : Performance Waveforms for the Half-bridge, 500 W, 100 kHz Converter with Output Current of 80 A.



2 µs/div
a) Waveforms of I_D, I_G, V_G



100 ns/div
b) Risetime



100 ns/div
c) Falltime

IMPROVED PERFORMANCE ; LESS COMPLEXITY

Although power supply designers for some time now have had an ever widening inventory of IC components available to ease their design tasks, the final measure of improvement has to be in terms of system performance versus cost. With fewer interface components to the power stages, freedom from potentiometer adjustments, protected start-up and shut-down, a built in soft-start network and several additional system-level features, the SG1525A provides a significant contribution to both performance and costs while simultaneously making the designer's task easier. With these accomplishments, it is clear that this device truly does represent a step-function improvement, introducing a second-generation of power control components.

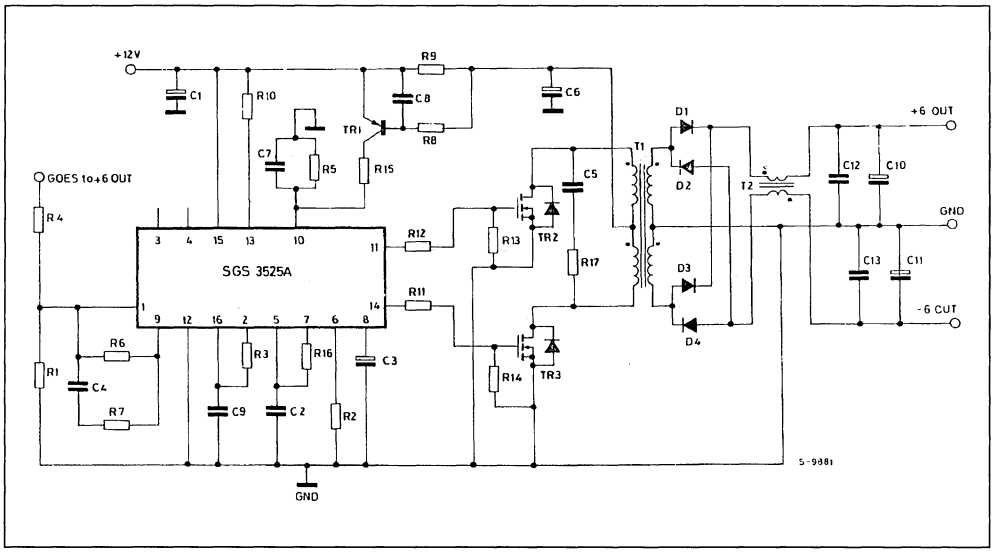
200kHz 15W PUSH PULL DC-DC CONVERTER

BY M. SUTERA

INTRODUCTION

The 15 W DC-DC converter, shown in fig. 1 has a push-pull topology and works in continuous mode with two outputs (+ 6 V, – 6 V) and features primary side control with full protection against fault conditions. There is no insulation between the primary and secondary side.

Due to the high working frequency, the power switches used are the new SGS-THOMSON advanced POWER MOS type : IRFZ20 with high density and bonding on the active area.



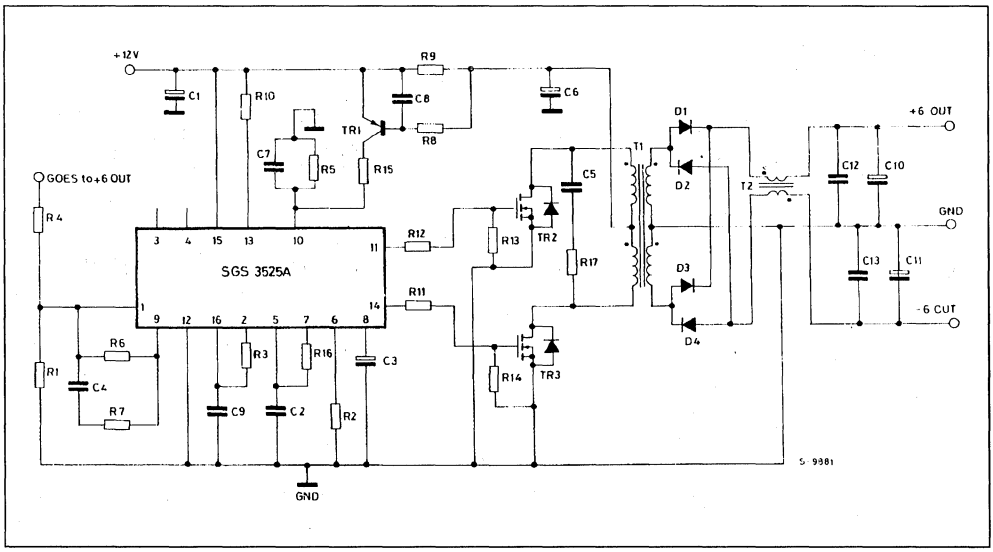
The PWM controller is the linear integrated circuit SGS3525A, with dual source/sink output drivers, internal soft-start, pulse by pulse shut-down and adjustable dead-time control.

Table 1 shows the power supply specifications.

Table 1.

Operating mode	:	Push Pull
DC Input Voltage	:	10V DC to 18V DC
Switching Frequency	:	200kHz ± 10%
Total Power Output	:	15W
Outputs	:	+ 6V ± 5% 0.1 to 1.3A
		– 6V ± 5% 0.1 to 1.3A
Line Regulation (+ 6V output)	:	0.05%/V
Load Regulation (+ 6V output)	:	0.2%/A
Efficiency (@ 1/2 load)	:	76%
Output Ripple @ Max Load + 6V, – 6V Outputs 50mV Peak to Peak		

Figure 1.



CIRCUIT DESCRIPTION

The DC input is chopped at a high frequency (200kHz). This high switching frequency allows the use of a very small transformer.

Due to the push-pull configuration of the converter the POWER MOS devices, the transformer and the diodes work at the frequency of 100kHz (photo 1, 2) ; the output filters and the oscillator of PWM controller work at a frequency of 200kHz (photo 3).

When Tr2 is on and Tr3 is off, diodes D2, D3 conduct and diodes D1, D4 are off. When Tr3 is on and Tr2 is off diodes D1, D4 conduct and diodes D2, D3 are off.

The snubber formed by C5, R17 is used to clamp the voltage spikes on Tr2 and Tr3 drains. With a leakage inductance L_d = 0.5µH, a primary current I_p = 2.8 A at $V_{IN\,MIN}$ and maximum load and an allowable voltage spike V_p = 30V we can calculate C5 as follows :

$$C5 = \frac{L_d \cdot I_p^2}{(2\,V_{MIN} + V_p)^2 - (2\,V_{IN})^2} = 1.8\ nF \qquad \text{Eq. 1}$$

The PWM controller SGS352A has the two drive outputs in totem-pole configuration in order to drive the POWER MOS. The feedback signal for the PWM is directly connected to the inverted input of

the error amplifier from the + 6 V output by the resistive divider R4-R1. The maximum current protection is sensed by Tr1, R9, R8 and is connected to pin 10 (shut-down).

The magnetic coupling of the series inductance in the output filter is very important for good regulation of the voltages. In this way when the load is very different in the two outputs (+ 6V max load ; – 6V min load or viceversa) the indirectly regulated output (– 6V) has a very stable output voltage (see fig. 2).

The efficiency is excellent : 70 % over a wide range (fig. 3).

The transient response is very fast : about 50ms. Photo 4 shows the transient response of load regulation due to a load variation from 100mA to 1.3A and from 1.3A to 1.3A to 100mA (+ 6V output).

Fig. 4 shows the P.C. board (track layout) and the component positions.

Figure 2.

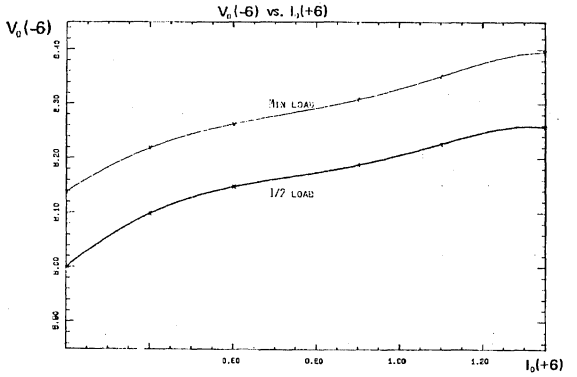


Figure 3.

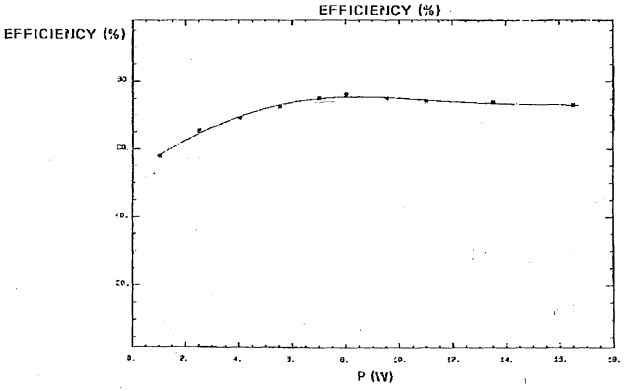
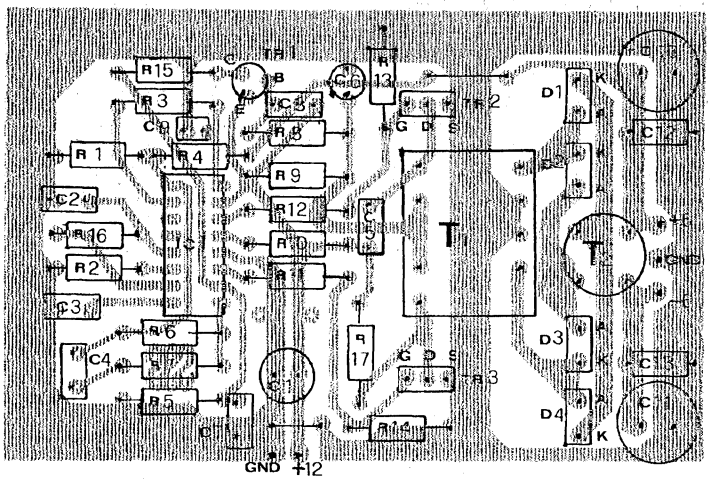


Figure 4 : P.C. Board and Components Layout (1 : 1 scale).



TRANSFORMER

For this design a Tomita E core of 2E 6 ferrite material was chosen. To calculate the core size we used the following equations :

$$A_e \cdot A_n > \frac{10^5 \cdot P_{OUT}}{1.16 \cdot \Delta B \cdot f \cdot d} = 0.143cm^4$$

Eq. 2

where :

P_{OUT} = output 15 (W)

ΔB = flux density swing (T) we chose $\Delta B = 200mT$

d = current density we chose = $450A/cm^2$

f = working frequency of transformer

A_e = effective area of magnetic path [cm^2]

A_n = useful winding cross section [cm^2]

The core size is then EE 25 x 6.5 with $A_e = 0.42cm^2$, $A_n = 0.45cm^2$ and $A_e \cdot A_n = 0.189cm^4 > 0.143cm^4$.

The maximum value of primary current at V_{MIN} is :

$$I_P = \frac{P_{OUT}}{\eta \cdot \delta_{MAX} \cdot (V_{MIN} - \Delta V)}$$

$$= \frac{15}{0.75 \cdot 0.8 \cdot 9} = 2.8A$$

Eq. 3

where ΔV is the voltage drop on the R9 resistor and on the POWER MOS, δ_{MAX} = maximum duty cycle, η = efficiency.

The turns ratio is given by the following equations :

$$n = \frac{V_{prim.}}{V_{sec}} \cdot \delta_{MAX}$$

$$n = \frac{V_{MIN} - \Delta V}{V_{OUT} + V_f} \cdot \delta_{MAX} = 1.03$$

Eq. 4

The number of turns N_p is calculated as follows :

$$N_{pMIN} = \frac{V_{MIN}[V] \cdot \delta_{MAX}}{\Delta B[T] \cdot A_e[cm^2] \cdot f[Hz]} \cdot 10^4 = 9.5turn$$

Eq. 5

The number of turns used was $N_p = 10$ and $N_s = 10$.

The primary inductance is then the same as the secondary inductance.

$L_p = L_s = N_p^2 \cdot A_L = 100 \cdot 2400nH = 240\mu H$

The value of L_d (leakage inductance) was measured on the transformer :

$L_d = 0.5\mu H$

OUTPUT FILTER

The most interesting part of the output filter is the transformer T2 which, coupling the output series inductance of the two outputs, gives good regulation of the – 6V output (magnetic regulator).

T2 construction is very simple because the two inductance are directly wound on the same cylindrical ferrite core. Each winding is made up of 200 turns and is : L (+ 6V) = L (– 6V) = 17µH.

The four fast recovery diodes used are BYW29 -100 type.

Capacitors C10, C11 are 220µF Roederstein EKR low ESR type for application in switching power supplies.

The ripple value obtained is very low = 50mV peak to peak (photo 3).

Photo 1 : Tr2, Tr3, V_{ds} (V_{ds} = 20V/div.).

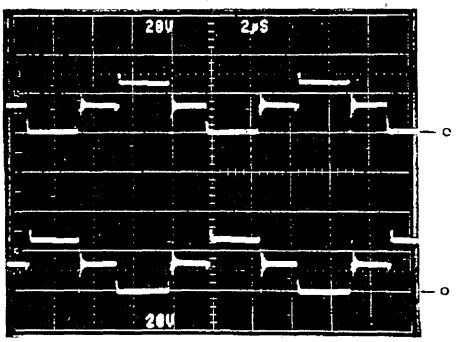
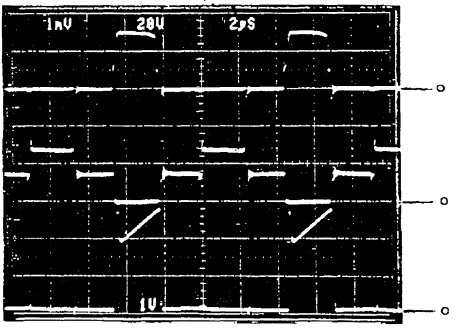


Photo 2 : Tr3 Waveforms (V_G = 10V/div, V_{ds} = 20V/div, I_d = 1A/div.).



COMPONENT LIST

Resistors

R1	=	8.2K	1/4W
R2	=	5.6K	1/4W
R3	=	1.2K	1/4W
R4	=	1.5K	1/4W
R5	=	1.2K	1/4W
R6	=	470K	1/4W
R7	=	3.3K	1/4W
R8	=	390Ω	1/4W
R9	=	0.22Ω	1W
R10	=	10Ω	1/4W
R11	=	22Ω	1/4W
R12	=	22Ω	1/4W
R13	=	5.6K	1/4W
R14	=	5.6K	1/4W
R15	=	18Ω	1/4W
R16	=	47Ω	1/4W
R17	=	33Ω	1/2W

Capacitors

C1	=	100µF
C2	=	1nF
C3	=	1µF
C4	=	10nF
C5	=	1.8nF
C6	=	2.2µF
C7	=	10nF
C8	=	2.7nF
C9	=	10nF
C10	=	220µF
C11	=	220µF
C12	=	330nF
C13	=	330nF

Transistors

TR1	=	2N2907
TR2, TR3	=	IRFZ20

Diodes

D1, D2, D3, D4	=	BYW2929-100

IC_S

I1	=	SGS3525A

Transformers

T1 core	=	TOMITA EE 25 x 6.5 2E6 Material
T2 core	=	cylindrical 30 x 20mm

Photo 2a : Turn On.

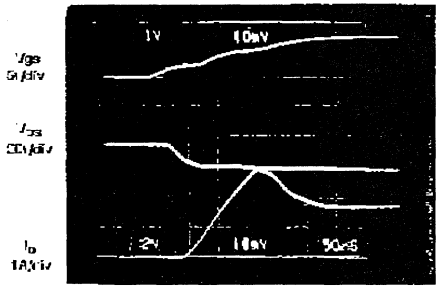


Photo 2b : Turn Off.

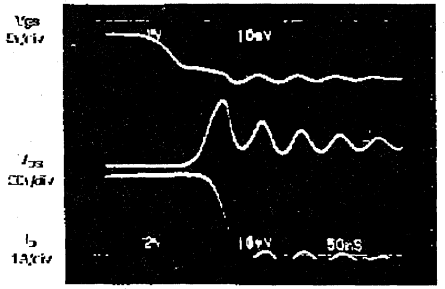


Photo 3 : Ripple on + 6V and – 6V Outputs (20mV/div.).

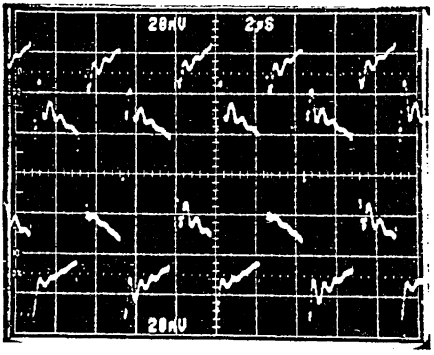
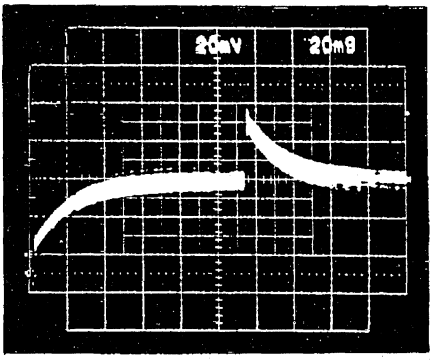


Photo 4 : Transient Response (20mV/div.).



HIGH VOLTAGE TRANSISTORS WITH POWER MOS EMITTER SWITCHING

BY M. SUTERA

INTRODUCTION

This paper summarizes the results of an investigation carried out on power devices with both MOS and BIPOLAR parts working together in the same circuit. The "emitter drive" configuration was considered, with switching power supply applications in mind.

The devices used are :

Power MOS	: SGSP321, IRFZ20
Bipolar transistors	: BUV48, BU508A
Ultrafast bipolar transistors	: SGS463
(Hollow Emitter)	: SGS443
Fast darlingtons	: SGSD00055, BU810

In the case of flyback switching power supplies a practical example is also described.

CIRCUIT DESCRIPTION

The term "emitter switching" describes a circuit configuration where a low voltage transistor (MOS or Bipolar) switches off the emitter current of a high voltage transistor, and consequently the transistor itself.

This configuration combines the fast switching of a low voltage device with the high power switching of a high voltage device, since :

high current x high voltage = high power switching.

The combination of a high voltage bipolar and a low voltage Power MOS is preferable due to the high switching speed and the low driving energy of the combined power switch.

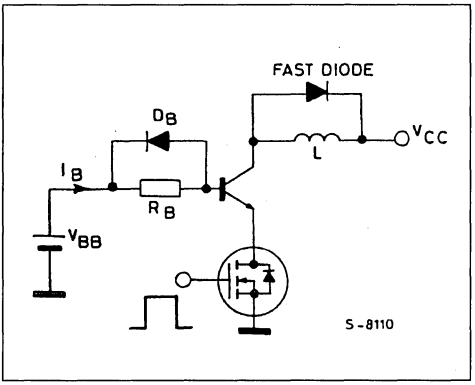
The base of the high voltage bipolar device is driven by a constant voltage source. The energy dissipated to drive the high voltage bipolar device depends on the losses that the forward bias current I_{B1} generates in the resistance in series with R_B, $I_{B1}^2 \cdot R_B \cdot t$. This power dissipation can only be reduced by using high gain transistors or Darlingtons.

(see fig. 1).

The diode in series with the base serves to clamp the base over voltage at turn-off.

The two transistor stage is driven by the gate of the low voltage Power MOS. Very low driving energies, about 180nJ per cycle, are involved in the charging of the input capacitances.

Figure 1 : The Basic Circuit used for the Evaluation of the Emitter Switching System. The Base Drive Circuit used is shown for Comparison.



Consequently the stage can be directly driven by the output of suitable linear integrated circuits.

The possibily of direct driving by an IC output together with the excellent switching speed make this configuration extremely suitable for switching power supplies at frequencies of 50kHz or higher.

CIRCUIT OPERATION

As we have seen, the forward base current I_{B1} is fixed by the external circuitry :

$$I_{B1} = \frac{V_{BB} - V_{BEsat} - V_{DSon}}{R_B}$$

The collector current instead depends on the load, and in general, varies with the time.

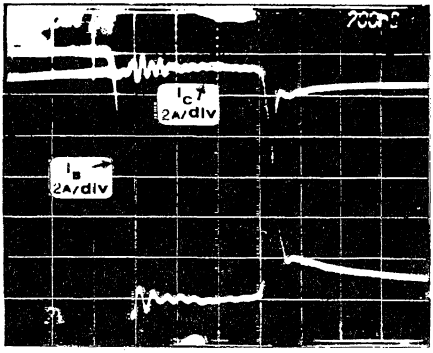
The turn-on and turn-off phases can be analysed separately.

TURN-OFF

When the driving signal to the Power MOS is low the drain current is interrupted and the emitter current of the high voltage bipolar falls to zero. The emitter reaches the base voltage and will not carry any more current. As a result the collector current can only flow through the base, becoming a reverse base current that depletes the base to collector junc-

tion. This reverse base current I_{B2}, from the moment when the emitter current disappears, coincides with the collector current. See photo 1. The stored charge is removed in a typically very violent, and consequently rapid manner.

Photo 1 : Base and Collector Current at Turn-off.



As a result the storage time is substantially reduced.

The fall time, which is related to the recombination under the emitter, is also generally reduced.

Typical values for the fall and storage time of the SGS-Thomson devices used in the test are shown in table 1, for both emitter and the base drive circuits.

Table 1 : Typical tf and ts on Inductive Load.

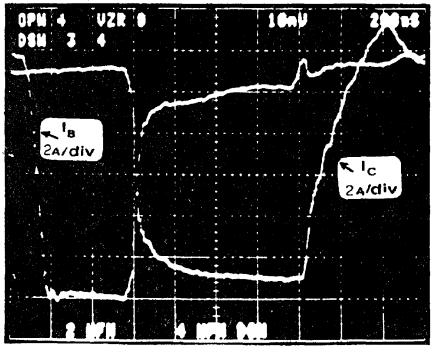
Device	$I_{C(A)}$	Emitter switching		Base Switching	
		tstorage	tfall	tstorage	tfall
BUX48	10	500ns	100ns	2µs	200ns
BU508A	5	800ns	300ns	6µs	400ns
SGSD00055	10	400ns	100ns	1.2µs	100ns
BU810	5	300ns	150ns	800ns	150ns
SGSD00035	10	300ns	50ns	800ns	50ns
SGSD00039	5	300ns	40ns	700ns	50ns

TURN-ON

When the Power MOS is the on state, the bipolar device also starts conducting. The dynamic behaviour (see photo 2) does not differ in any substantial way from the usual case of the base drive.

The dynamic saturation transient $V_{CEsat\ dyn}$ is also practically the same with a base drive as with an emitter drive. The collector current, when the collector load is the primary winding of a switching transformer, can vary according to two possibilities, (see fig. 2).

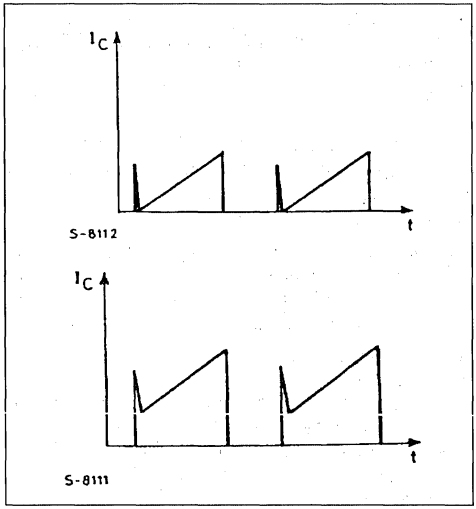
Photo 2 : Base and Collector Current at Turn-on.



a) After the initial peak due to the recovery of the diode present on the secondary winding, the collector current increases linearly starting from zero

b) After the same initial peak, the collector current increases linearly starting from the value memorized in the magnetic circuit at the end of the previous cycle.

Figure 2 : Collector Current Waveforms with Varying Load.



REVERSE BIAS SAFE OPERATING AREA

A problem that occurs in bipolar transistors is damage caused by "current crowding".

Fig. 3a illustrates current flowing in a typical bipolar device. Fig. 3b shows how, when the device is

turned off and the current begings to die away, the current focuses with a high concentration under the emitter. This high current density can damage or destroy the transistor.

Figure 3a.

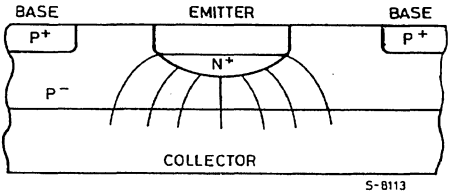
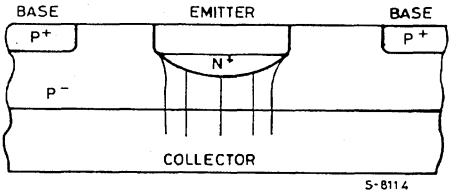


Figure 3b.



The energy dissipated within a bipolar power transistor at turn-off can be found graphically from a plot of I_C versus V_{CE} at turn-off. Three cases are shown in fig. 4a, b and c. The shaded area is proportional to the energy that is dissipated in the device during turn-off.

Consequently turn-off times affect the SOA of the device, (fig. 5b). These problems can be overcome using emitter switching.

Figure 4a : Slow Turn-off. No Crowding but High Average Heating.

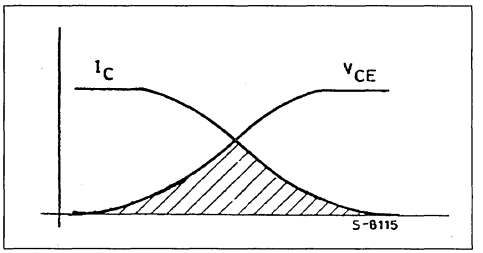


Figure 4b : Fast Turn-off. Crowding with Low Average Heating but Possible High Peak Power.

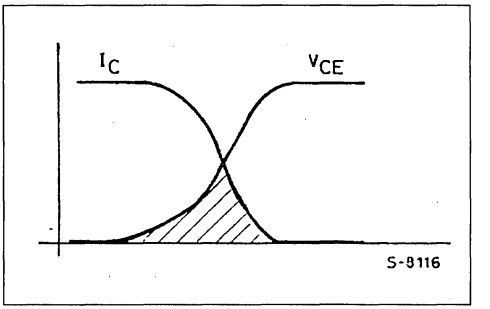
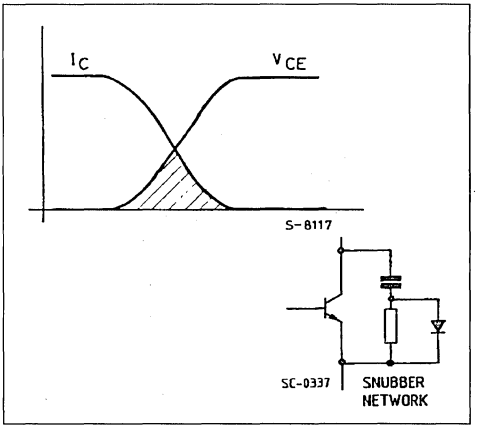


Figure 4c : Fast Turn-off (with V_{CE} delayed by snubber network).



The way the stored charge is swept away in the high voltage bipolar device when it is driven by the emitter, produces some interesting consequences.

The stored charges are evacuated through the base contact when the emitter current is zeroed and not later than a few tens of nanoseconds after the beginning of the storage interval. Consequently, during the turn-off, no charge is injected from the emitter into the base. Although the reverse base current is quite relevant, no focusing of the current in the centre of the emitter fingers takes place.

The bipolar device therefore exhibits an energy absorbing ability at the turn-off RBSOA that is substantially higher than if a normal base drive were used. With a base drive the emitter would inject charges and the voltage drop across the distributed base resistance would induce the "emitter crowding" phenomenon.

The practical evidence for all the transistors investigated (BUV48, BU508A, SGSF463) shows that the reverse bias operating area (RBSOA) extends right up to the BV_{CES} ! (see fig. 5).

This extreme effect is unfortunately much less pronunced when using fast Darlingtons. The higher complexity of the charge extraction mechanism and the charge injection from the emitter into the base in the driver transistor imply that the RBSOA extension is almost irrelevant.

Figure 5a : Reverse Bias Safe Operating Area.

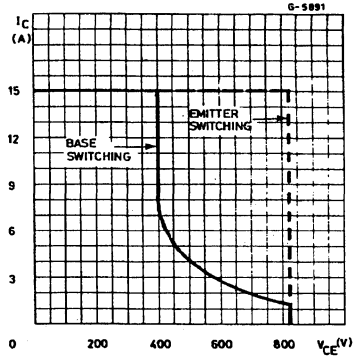
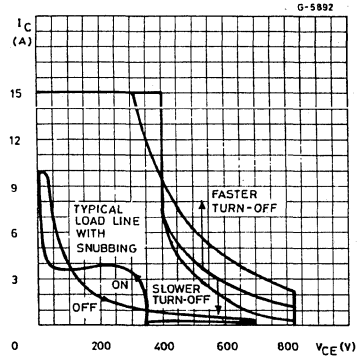


Figure 5b : How Reverse Bias Safe Operating Area Changes for :
i) slow turn-off.
ii) fast turn-off.



A POSSIBLE APPLICATION

A possible application of the "emitter switching" configuration is shown in figure 6, where a switching power supply operating in a "flyback" mode has been implemented.

The basic criteria used in choosing the value of the circuit elements are given below. The purpose of the study was to demonstrate the feasibility and to evaluate the advantages. Exact circuit element values can be further optimized, especially in the case of the transformer.

The power source in the mains singlephase, 220V a.c., and the switching frequency can be set to 50kHz or more.

The devices used were :

Q1 : fast Darlingtons with BV_{CES} 1000V for 110V line
- SGSBU810 for current up to 5A
- SGSD0055 for current above 5A

Fast transistor with $BV_{CES} \geq 800V$ for 220V line
- SGSF443 for currents up to 5A
- SGSF463 for current up to 10A

Q2 : Low voltage POWER MOS ($BV_{DSS} = 50V$)
- SGSP321/IRFZ20 for currents up to 10A

Q3 : High voltage, low current POWER MOS $V_{(BR)\,DSS} \leq 450V$)

Control IC : UC3842

DZ2 : Zener diode 2W/20V

D1 : 25V diode, with I_C peak rating as high as 10A for 500ns

C6 : Electrolytic capacitor, 100µF, 25V. It absorbs possible variations of V_{BB}.

R3 : Resistor setting the forward bias base current of the Darlington :

$$R3 = \frac{V_{CE} - V_{BEsat} - V_{DSon} - R_7 I_D}{I_{B1}}$$

Its power rating must exceed $R3 . I_B^2 . t$ (in practice 3W)

R7 : Shunt resistor to sense the switch current. The over current $I_{S\,max}$ protection is set according to

$$R7 = \frac{1V}{I_{Smax}}$$

C4, R6 : RC network, filtering the disturbances induced by the switching transients on the I_{Smax} protection input.

C3, R5 : RC network, setting the switching frequency and the maximum duty cycle, according to the UC3842 data sheet.

$t_{charge} = 0.55\ R_5\ C_3$

$t_{discharge} =$

$R_5 \times C_3 \ln [(6.3\ R_5 - 2.7)/(6.3\ R_5 - 4)]$

$f = 1/(t_c + t_d)$

R8, R9 : Resistive divider of the feedback voltage from a secondary sense winding, rectified by D5 and C5. The divided voltage is compared by the control IC to an internal reference of 2.5V.

C2, R4 : Compensating network in the error amplifier of the feed-back voltage.

R1 : Resistor biasing the Q3 gate (1.2M, 1/4W)

R2 : Resistor that limits the inrush current through the POWER MOS, Q3, at the turn-off (1.2, 2W)

D4 : Fast recovery diode
Its voltage/current ratings depend on the particular secondary winding it rectifies.

D5 : Low current/low voltage diode

D3, R10, C8 : Snubber network (fig. 6 shows just one of the possible configurations).

$$C8 = \frac{L_d\ I_c^2}{V_{DS}^2}$$

$R10 = 1/4fC8$

$P\ (R_{10}) = 1/2\ L_d\ I_D^2 \cdot f$

where :

f = switching frequency

L_d = stray inductance of the transformer

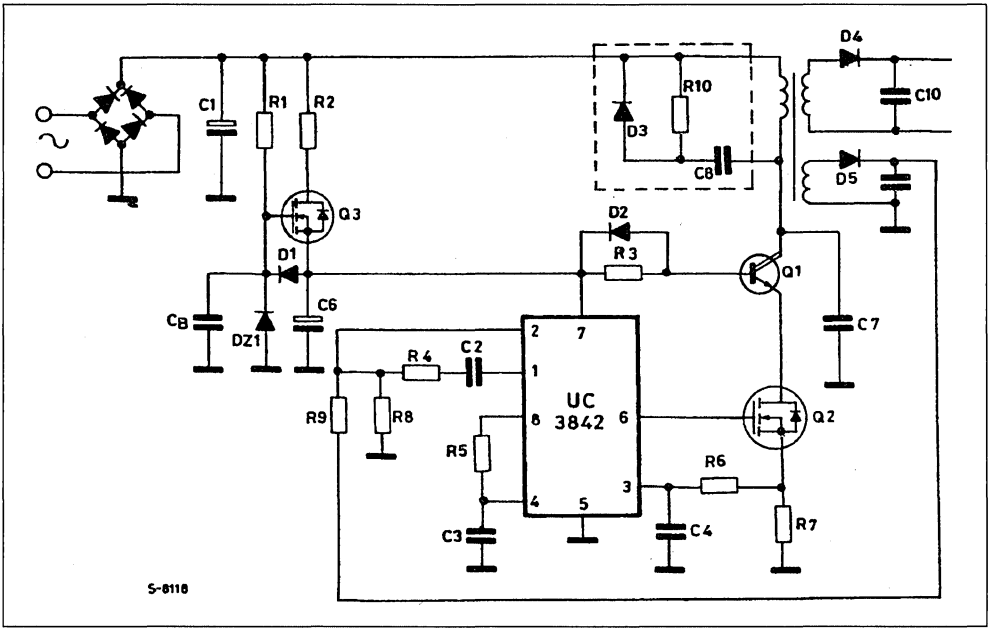
V_{OS} = maximum voltage overshoot allowed

D3 : A 400V fast recovery diode

C7 : The use of a capacitor reduces the crossover of the Darlington (3 to 6nF)

It is important to note that, the power transistor Q3 acts only at the turn-on of the power supply and when the capacitor C6 supplies more energy to the base of the Darlington and to the supply input of the IC than is returned to C6 during the turn-off of the Darlington, Q1.

Figure 6 : "Emitter Switching" Circuit.



CONCLUSION

The "emitter drive" configuration exhibts some clear differences with respect to the usual "base drive" configuration, and they can be particularly useful in switching power supply applications :

- Substantial reduction of the storage time and improvement of the fall time.

Switching frequencies of 50kHz and higher are possible

- The dynamic drive circuitry is simplified. The negative voltage supply is not required to remove the stored charge from the base. The energy needed to drive the gate of the POWER MOS is very low (180nJ per cycle).
- Extremely high ruggedness at the turn-off of the inductive load (i.e. very large RBSOA) if the high voltage bipolar part is a transistor.
- Higher power dissipation in the on-stage, due to the additional losses in the POWER MOS ($I_D^2 \cdot R_{DS\,(on)} \cdot t_{on}$).

This last point is the only disadvantage, but it is more than compensated for if switching at high frequencies. The lower switching losses (a saving each cycle) can justify the higher on-state losses (a fixed expenditure) as soon as the switching frequency is high enough, which is often the case in switching power supplies.

A TRANSISTOR FOR 100 kHz CONVERTERS : ETD

BY Luc WUIDART

INTRODUCTION

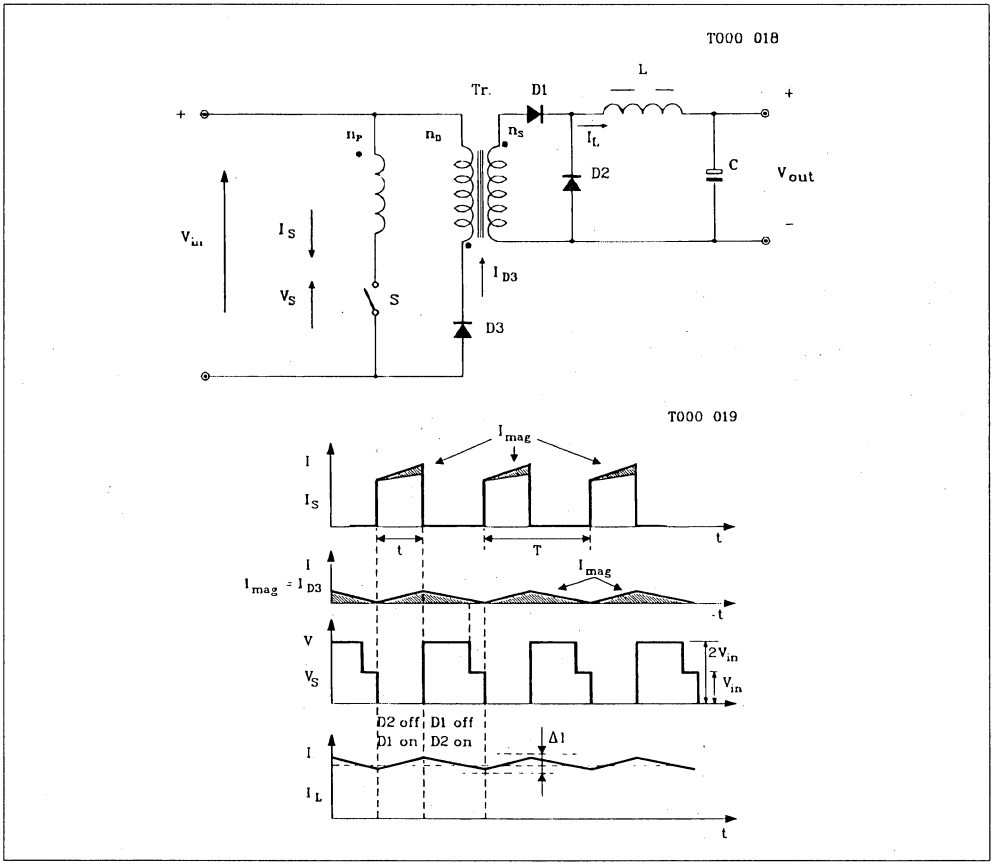
Power converter designers aim to reduce the size and the weight of their equipment. Hence, there is a trend towards higher operating frequencies. Consequently for the semiconductor manufacturers, there is a growing demand for fast switches. The POWER MOSFET transistor is now well known as a fast device.

However, the development of ultra fast "ETD" bipolar transistors is now challenging this way of thinking in certain applications. As an illustration, we have selected an example of a "300W - 100kHz forward" switch mode power supply (SMPS).

VOLTAGE CONSTRAINTS

This "forward" converter contains a single power switch and operates directly from the 220V AC mains. The principle wave forms are illustrated in figure 1.

Figure 1 : Basic Theoretical Wave Forms of the Forward SMPS.



The switch must be capable of withstanding a static collector-emitter voltage which, to a first approximation, is given by :

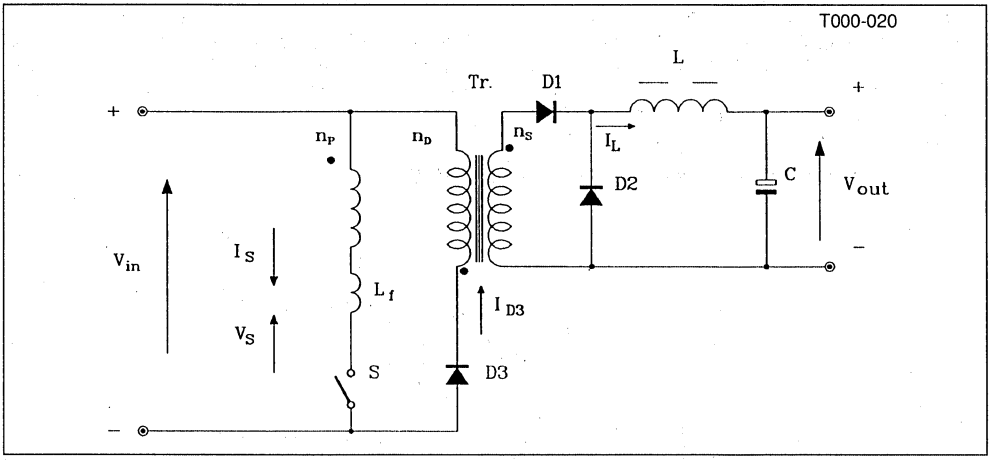
$(1 + n_P/n_D) \times V_{in}$, where,

- n_P = number of turns in the primary winding
- n_D = number of turns in the demagnetization winding
- V_{in} = rectified mains voltage

When operating on the 220V AC mains and when n_P equals n_D, the voltage across the switch terminals should only reach 750V in the worst case (corresponding to a maximum rectified mains value of 375V AC).

In reality, the voltage across the switch terminals reaches a peak value (V_{peak}) which is much higher. The peak value depends upon the switching time, the circuit capacitance and the leakage inductance L_f between primary winding n_P and the demagnetization winding n_D (see figure 2).

Figure 2 : Leakage Inductance L_f between Primary Winding n_P and Demagnetization Winding n_D.



DESIGN OF SNUBBER CIRCUIT

At turn-off, energy stored in the transformer leakage inductance generates a voltage spike (figure 3). In order to limit this voltage spike, the energy must be transferred to the capacitor C_{min} in the snubber circuit. The energy depends on the switching current. In a 300W SMPS, the peak value of the current I_{max} is 5A. It is this value of current which is used to calculate the value of the capacitance C_{min} required.

With a maximum voltage V_{peak}, the value of C_{min} can be calculated using the following formula :

$$C_{min} = \frac{L_f \times I_{max}^2}{V_{peak}^2 - V_{in\,max}^2 (1 + N_P/N_D)^2}$$

Figure 3a : Wave Forms of Switching Current and Voltage Across the Switch Terminals at Turn-off.

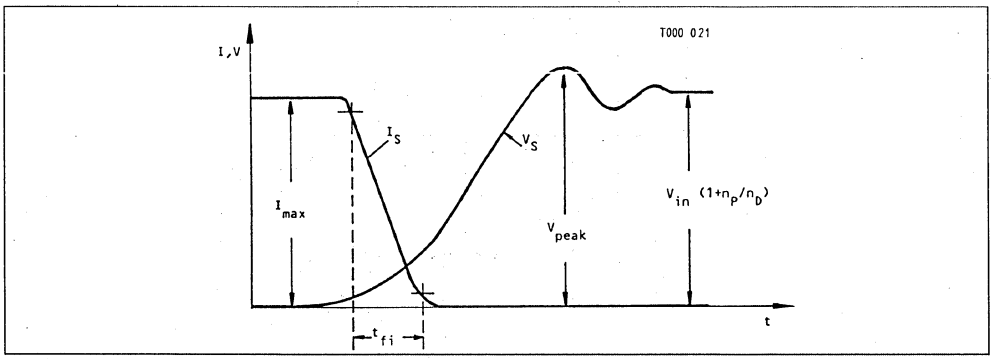
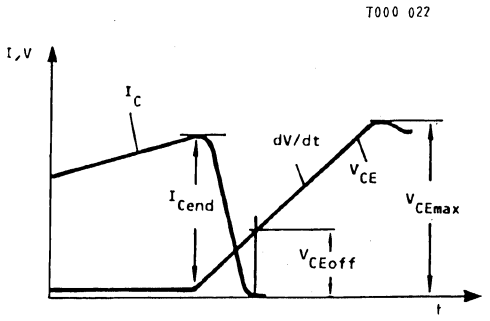


Figure 3b : Definition of the Voltage V_{CEoff}. V_{CEoff} is measured when the Collector Current Reaches 2 % of the Collector I_{Cend}.



We call V_{CEoff} the voltage which appears during the turn-off at the moment when the collector current I_C reaches 2% of its value I_{Cend}. If the value V_{CEoff} measured in the circuit is low compared to the rating V_{CEW} of the transistor, the safety margin between the SOAR and the stress on the transistor is large. V_{CEW} is the maximum V_{CE} voltage at turn-off with current.

In practice, V_{peak} can be set between 800 and 900V. To provide a safety margin, a switch with a blocking voltage capability of 1000V must be used. This voltage corresponds to parameter V_{CEV} for bipolar transistors and to V_{DSS} for POWER MOSFET components.

For bipolar transistors, an additional parameter must be considered : the Reverse Biased Safe Operating Area : (RBSOA). The turn-off cycle must remain within the RBSOA, otherwise, the value of capacitance must be increased from C_{min} to a higher value C_r.

Thermal dissipation in the snubber resistor, R_s (figure 6), will be increased in the same ratio :

$$C_r = \frac{t_{fi} \times I_{max}}{2 \times V_{CEoff}}$$

For the selected transistor, V_{CEoff} must be less than the specified V_{CEW} (see figures 3a and 3b).

SWITCH TYPE

In this application, three different types of switch using different technologies are considered. These are :

- conventional bipolar transistor,
- POWER MOSFET,
- ultrafast bipolar "ETD" transistor (see appendix).

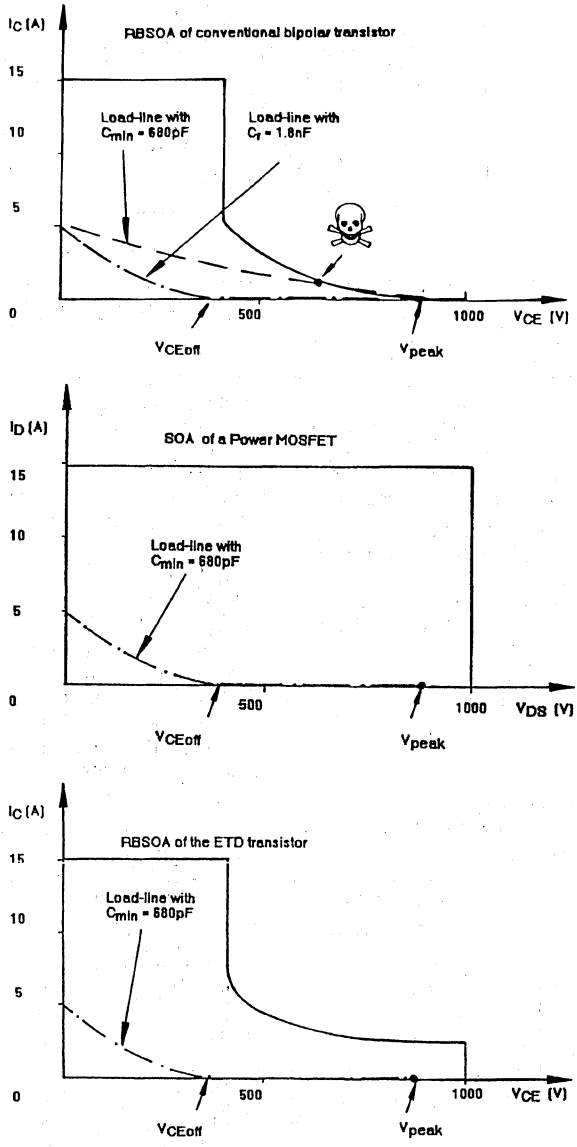
Table 1 summarizes the performances of these types of switches under operating conditions, i.e., for a junction temperature of 100°C and with a well adapted gate/base drive (optimized totem-pole drive for POWER MOSFETs and negative bias drive for bipolar transistors).

Table 1 : Transistor Characteristics.
Characteristics at Tj = 100°C "Totempole" gate drive. Base drive with negative bias. Same silicon area for each switch.

	Blocking Voltage Capability	Switching Time (Tj = 100°C)		Conduction (T_j = 100°C)
		t_r	t_{fi}	R_{DSon}, V_{CEsat}
STHV 102 VDMOS	1000V	100ns	100ns	5.4Ω
BUV 48 Conventional Transistor	1000V	85ns (60A/µs)	250ns	2.8V (5A)
BUF 410A ETD Transistor	1000V	50ns (100A/µs)	100ns	2.8V (5A)

The first point to notice is that at turn-off, an ETD transistor is as fast as a POWER MOSFET.
More surprisingly, the ETD transistor is twice as fast as a POWER MOSFET at turn-on.
Let us now consider the effects of the characteristics upon the size of the snubber. With a leakage inductance of 6.5µH and a current of 5A, a capacitor C_{min} of value 680pF is sufficient to limit the voltage V_{peak} to 900V (fig. 4) :

Figure 4 : Comparison of Turn-off Cycle Within the Safe Operating Areas for the Three Different Switches.



- However, a capacitor C_r of 1.8nF is required to limit the V_{CEoff} voltage to a value that is within the RBSOA of the bipolar conventional transistor.
- In comparison, the POWER MOSFET and ETD transistors can be kept within their safe operating areas with a capacitor of only 680pF.

LOSS EVALUATION

For the 300W forward SMPS operating at 100kHz, the following assumptions have been made.

The losses have been evaluated assuming a current I_{nom} of 4A, corresponding to the nominal output power. A current of 2.8A rms is obtained with a duty cycle of 48.5%. For a realistic comparison, conduction losses were reduced by paralleling two POWER MOSFETs (the conduction losses of a single POWER MOSFETs would be approximately 43W). The results of this evaluation are as shown in Table 2.

Table 2 : Results of Loss Evaluation for the Conventional Bipolar Transistor, the two paralleled Power MOSFET and the ETD BUF 410A Transistor.

	BUV48A	2 x STHV102	BUF410A
Silicon Area	30mm^2	40mm^2	30mm^2
Snubber (RCD) C_r	1.8nF	680pF	680pF
P_R*	51W	19W	19W
Losses in the Switch	30W	34W	17.5W
Conduction	5.4W	21.3W	5.4W
Switching	20.7W	12.3W	9.2W
Drive	3.9W	0.4W	2.9W
TOTAL LOSSES (RCD + COM)	81W	53W	36.5W

* P_R is the power dissipated in the resistor of the snubber circuit.

- for this application, the ETD transistor requires no more silicon area than a conventional bipolar transistor.
- the ETD transistor uses the same value of snubber capacitance as a POWER MOSFET.
- conduction losses in the ETD and the conventional bipolar transistor are the same.
- the ETD transistor has the lowest switching losses of the three devices considered.

In our example, at 100kHz, the superior performance of an ETD transistor results in about a 50% reduction in losses as compared to the BUV48A and 30% compared with POWER MOSFETs.

CONCLUSION

The example described in this paper (300W - 100kHz SMPS), figure 6 shows that of the three devices considered, the ETD transistor is the optimum cost/performance solution.

In addition, as a result of its fast switching capability ($t_r < 50ns$; $t_{fi} < 100ns$) and its extended RBSOA, the ETD transistor can be successfully used in other applications such as resonant converters, motor drives or uninterruptible power supplies.

ETD transistors with blocking voltage capability higher than 1000V are under development. These transistors will enable higher switching frequencies to be used in equipment supplied directly from the 380/440V mains supply.

APPENDIX I

WHAT MAKES ETD TRANSISTORS SO ATTRACTIVE ?

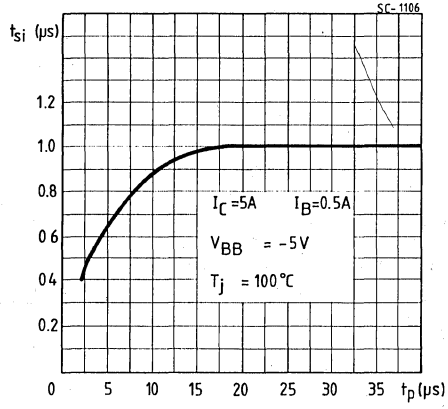
The new generation of ETD transistors adapted for high voltage applications is designed with an inovative technology utilizing a high degree of interdigitation.

The most innovative feature of this technology consists of the replacement of the traditional bipolar structure with emitter fingers (size : 250µm) by a cellular structure with much smaller dimensions (80µm cells). This cell design considerably eases the extraction of charge stored in the transistor during each switching cycle, since access to the intrinsic base is easier. This makes it possible to reduce switching times to values as low as 100ns.

The "Planar" technology has been selected for two reasons :

It permits extension of safe operating area at turn-off. Moreover, it requires a reduced number of masking levels with respect to conventional high voltage "mesa" power technologies.

Figure 5 : Curve Illustrating the Variation of Storage Time t_{si} versus Conduction Time t_p. (ETD transistor BUF410A).

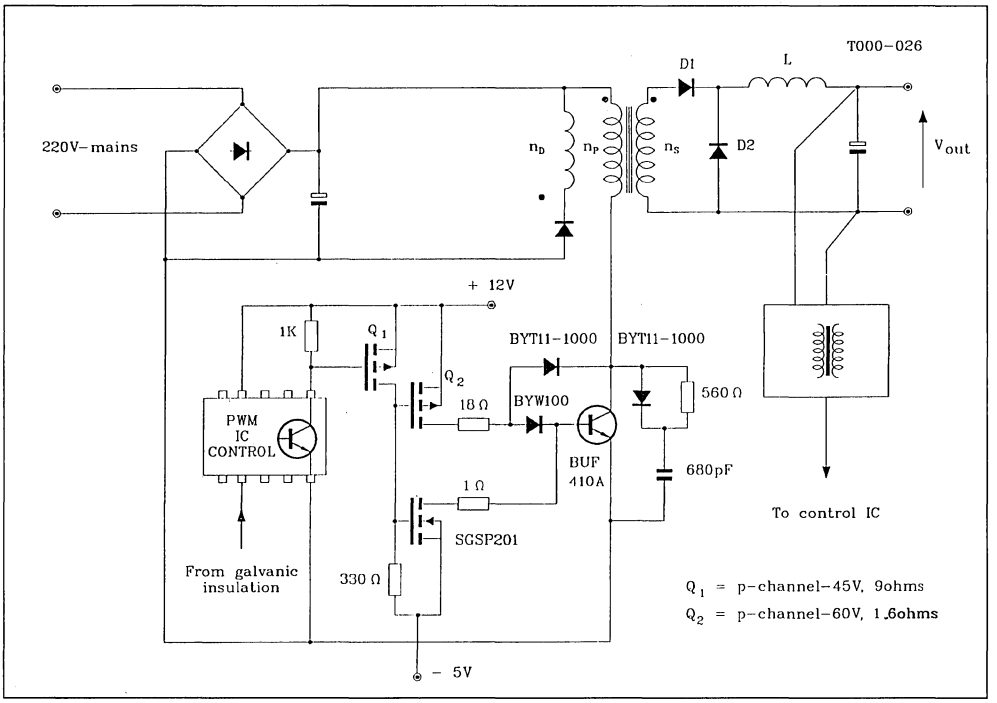


REGULATION DYNAMICS

In SMPS or motor drive applications, the minimum conduction time is a fundamental parameter when considering the dynamic regulation. The delay time at turn-off of the POWER MOSFETs specified in the data sheet is sufficiently low.

In the case of bipolar transistors, storage time depends on conduction time. In our application at 100kHz, conduction time must vary from less than one microsecond to five microseconds. In the BUF410A data sheet, the curve showing the variation of storage time, t_s, versus conduction time, t_p, shows that storage time varies from zero to 750ns maximum (see Figure 5). Consequently, the regulation dynamics are not limited.

Figure 6 : Schematic Diagram of an ETD BUF410A Transistor Implemented in a 300W – 100kHz Forward SMPS Application.



AN INNOVATIVE HIGH FREQUENCY HIGH CURRENT TRANSISTOR CHOPPER

By L. PERIER & J. BARRET

INTRODUCTION

Recent developments in power semiconductors and associated technologies have made possible the realization of medium power converters (5-50kVA) operating at switching frequencies higher than 20kHz.

This paper presents the design of a high current (500A), high frequency (20kHz) chopper using fast Darlington switches operating from a low voltage supply (60V). New optimised design techniques for paralleling power semiconductor devices are described. The association of these methods allows the switching of 500A in less than 200ns.

These new techniques are also suitable for high voltage medium power converters operating at high switching frequency, such as UPS, welding converters, motor drives and battery chargers.

A 500A - 20kHz CHOPPER WITH DARLINGTON IN PARALLEL

High frequency bandwidth and regulation is achieved for the 500A output current by switching at an ultrasonic frequency of 20kHz with a turn-off time of less than 200ns. Consequently, high rates of change of current (in excess of 2000A/µs) are experienced. Six Darlington transistors (ESM2012 D) in parallel and four ultra fast rectifiers (BYV54-200) in parallel are used to achieve the current rating.

Figure 1 : Switches used in the Chopper.

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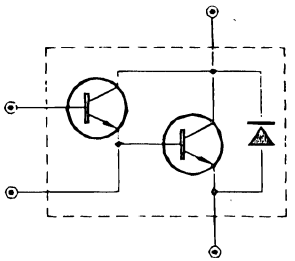

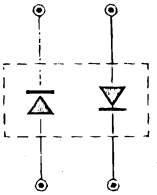

ESM 2012 D

V_{CEW} = 125V
V_{CEV} = 150V
V_{CEsat} (100°C) < 1,5V
for I_C = 70A
I_B = 0,25A
t_{fi}(100°C) < 0,4ms
R_{th} = 0,7K/W

BYV 54-200

V_{RRM} = 200V
V_F(100°C) < 0,85V for I_F = 50A
R_{th} = 1,2K/W

Figure 2 : New Base Drive Concept which Automatically Generates the Negative Bias. The negative bias generated is independent of the duty cycle.

1/ Power stage

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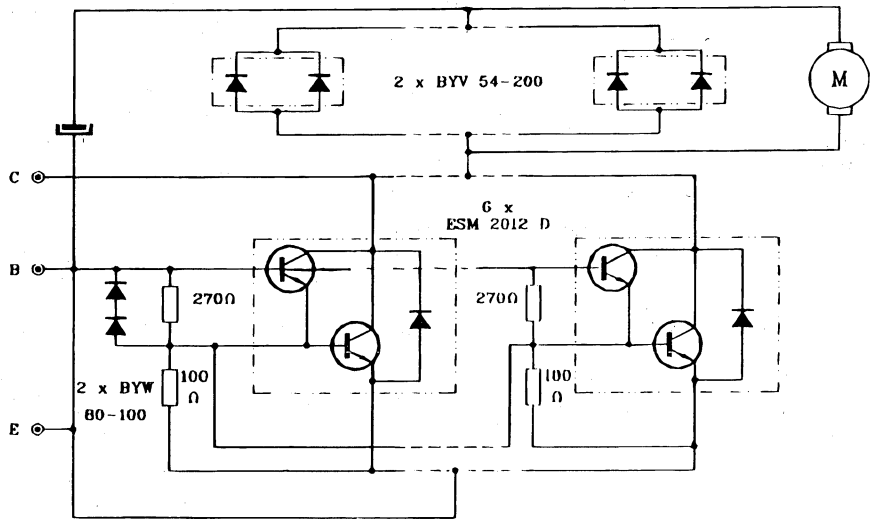

2/ Base Drive

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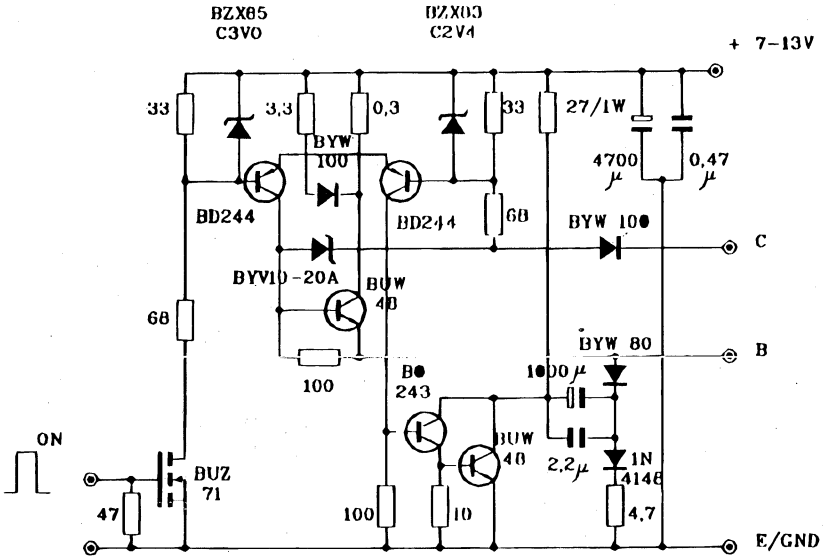


The 500A/60V/20kHz chopper

A power Darlington and diodes are shown in figure 1 together with their important characteristics. Figure 2 shows the power stage and the base drive circuit.

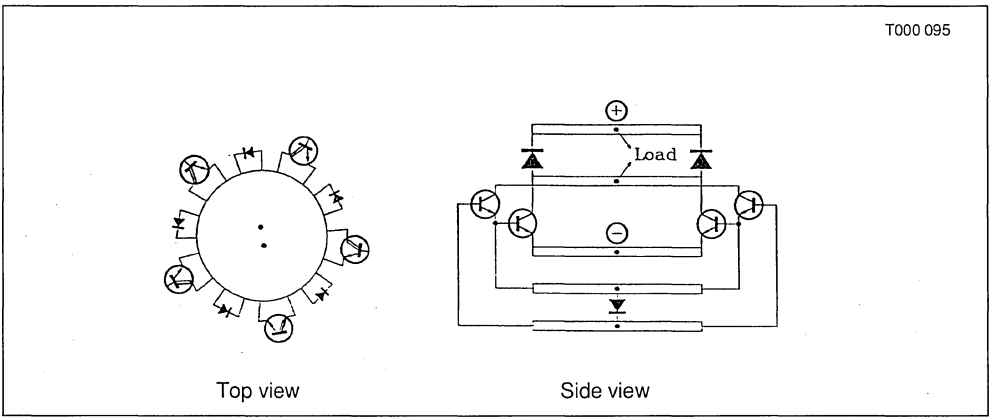
A base current of 5A is sufficient to control a collector current of 500A. The static and dynamic sharing of the collector and base current between the paralleled devices is better than 90% provided :

a) The devices are mounted in a circular layout on a common heatsink as shown in figure 3. Good utilization of the heatsink is achieved using this physical layout.

b) The bases of the output stages of the Darlingtons must be linked together. The access to the bases of the output stage of the ESM2012 D Darlingtons enables this.

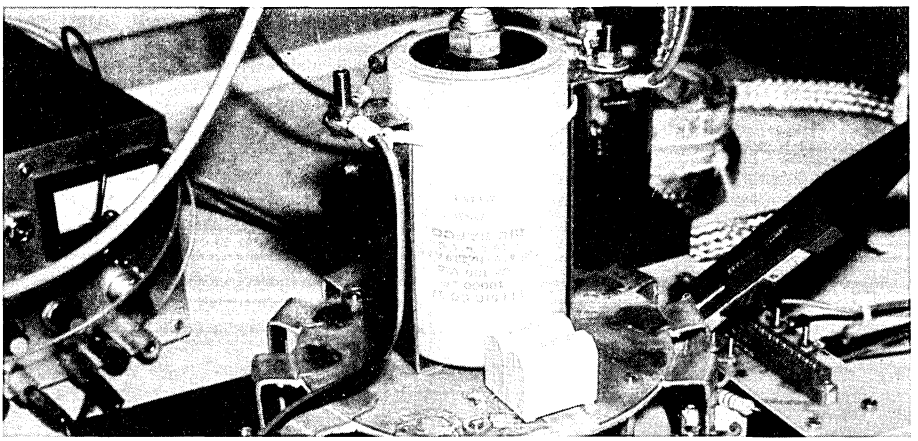
Due to excellent current sharing, the Darlingtons can be used close to their nominal collector current rating.

Figure 3 : Circular Geometry for the Physical Layout of Power Devices.



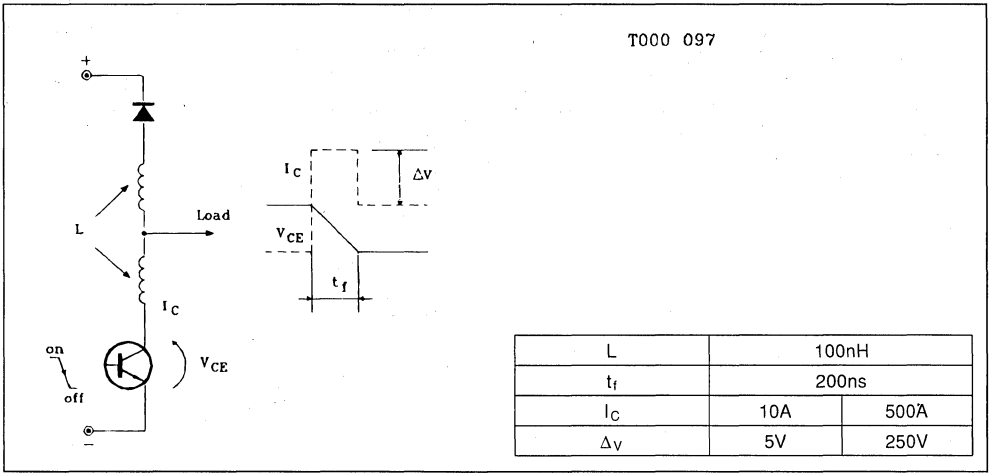
The BYV54-200 ultra fast rectifiers in parallel are not derated as these fast recovery epitaxial diodes have negligible voltage drop (V_F) spread.

Figure 4 : Power Stage.



Low wiring inductances are required for high performance switching as parasitic inductances cause overvoltage spikes at turn-off.

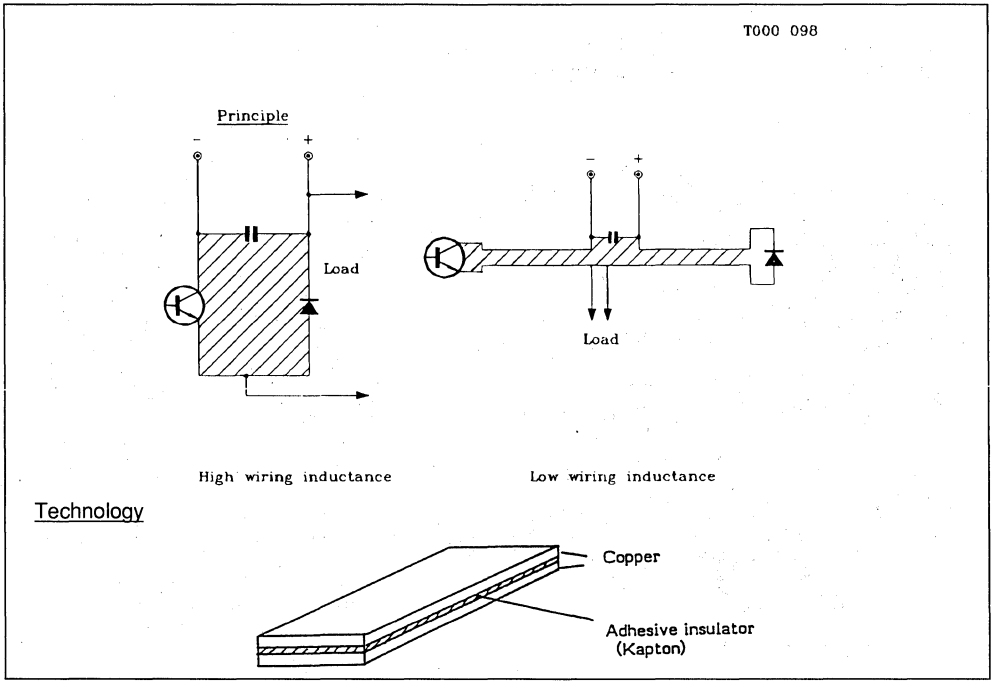
Figure 5 : A Low Wiring Inductance is Necessary in Order to Avoid High Over Voltages at Switch off.



L	100nH	
t_f	200ns	
I_C	10A	500A
ΔV	5V	250V

The 500A chopper has been designed with a low inductance plate wiring method. The plate wiring consists of 2 parallel copper plates separated by a thin adhesive insulator (see figure 6).

Figure 6 : Low Inductance Wiring.

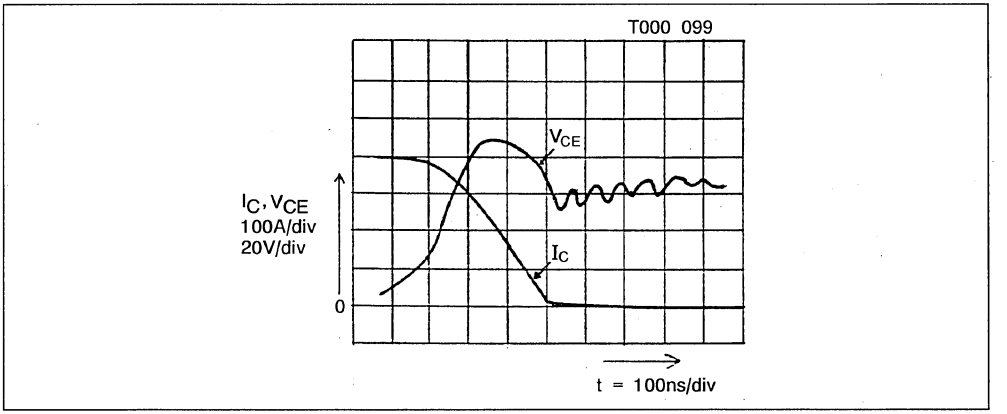


Wiring inductances as low as 5nH/m can be achieved in a 500A_{RMS} circuit using plate wiring.

The parasitic inductance of the power stage of the 500A chopper (capacitor + Darlington + free-wheeling diode) has been estimated at 20nH. Such a reduction of wiring inductance in the power stage and the base drive allows :

* Very high switching speed of the Darlingtons at turn-on and turn-off : 2000A/µs.
* At turn-off an overvoltage of only 50V is experienced by the Darlingtons for a dI/dt of 2000A/µs.

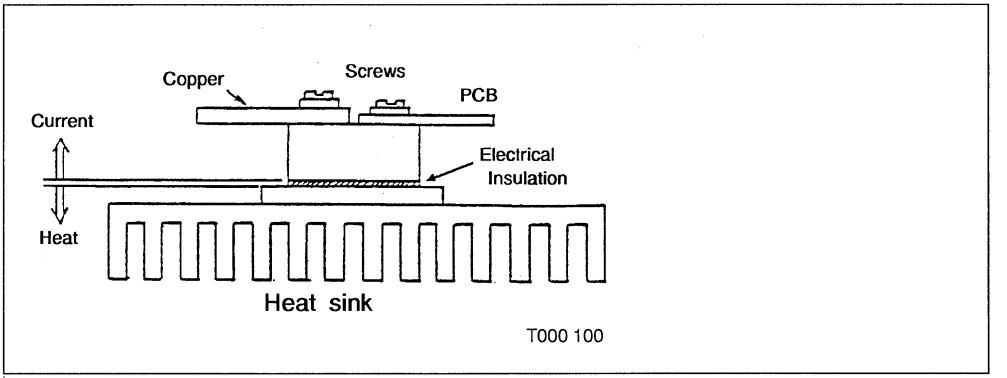
Figure 7 : Turn-off Switching of the Fast Darlington Switch.



The ISOTOP package is used for all the power semiconductor components in order to optimize cooling and wiring.

The package has screw terminals on the top of the case suitable for plate wiring, low parasitic inductance due to its low profile and internal insulation with low thermal resistance.

Figure 8 : A High Current Package : ISOTOP.



CONCLUSION

The design of a 500A - 20kHz chopper using fast switching Darlingtons and diodes has been presented.

The power semiconductor components have been packaged in the ISOTOP package, allowing screw connections and plate wiring techniques to be used. The techniques developed also can be applied in the design of medium and high voltage converters.

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APPENDIX I

LOW INDUCTANCE WIRING

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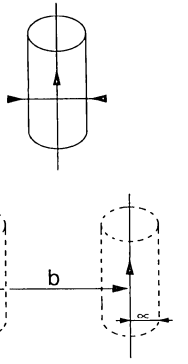

1. Modelling and inductance
   The inductance of wiring made circular cross section wire, can be modelled as the sum of two terms :
   a) Self inductance of one wire :

$$L_1 = \frac{\mu O}{8\pi} \text{ (H/m)} \qquad \text{Eqn.1}$$

   b) Mutual inductance of the loop :

$$L_2 = \frac{\mu O}{\pi} L_n \frac{b-a}{a} \text{ (H/m)} \qquad \text{Eqn.2}$$

   The total inductance of the wiring os thus :

$$L_T = \frac{\mu O}{\pi} \left(\frac{1}{4} + \ln \frac{b-a}{a} \right) \text{ (H/m)} \qquad \text{Eqn.3}$$

LT depends strongly on the geometry of the circuit. The best way to decrease LT is to decrease the area of the loop :

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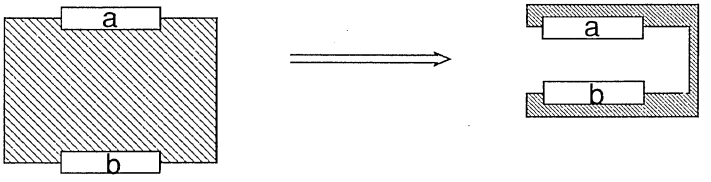

2. TECHNOLOGY FOR LOW INDUCTANCE WIRING

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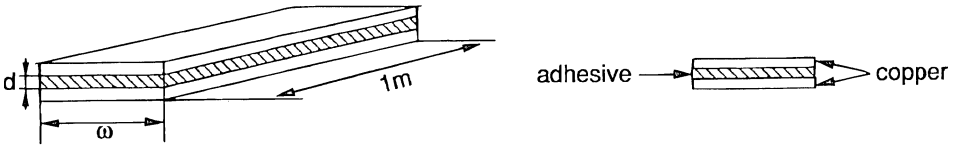


$$L = \mu O. \frac{d}{W} \qquad \text{Eqn.4}$$

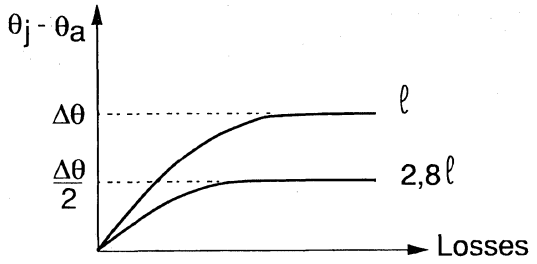
$I = 500A$, $\delta = 20A/mm^2$, $W = 50mm$, $d = 1mm$

$\Rightarrow L = 20nH/m$

APPENDIX II

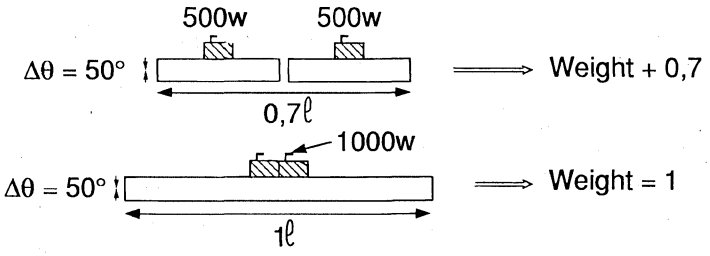
The cooling ability of a heatsink is not linearily dependent on its length

T000 104



Separation of heat sources is thus necessary to optimize the cooling

T000 105



Length, volume and weight can be reduced in some case by a factor of $\sqrt{2}$ if heating sources are spread over the heatsink

A POWER STAGE FOR A 20kHz 10kW SWITCHED MODE POWER SUPPLY FOR THE INDUSTRIAL 380/440V MAINS

By Jean BARRET

INTRODUCTION

The theory of transistor converters operating from the single phase 220V mains is not the same as that for switched mode power supplies operating directly from the 380V and 440V mains and delivering an output power of more than 10kW. For the latter the increased technological constraints must be taken into account when designing such a converter. This paper explains the design of a 10kW - SMPS operating on the three-phase 380V - 440V mains and the solutions which have been found to resolve the technological problems.

CHOICE OF THE CONVERTER STRUCTURE

The converter has been designed for a supply from the 380V and 440V mains. It must provide an output voltage of 80V and an output power of 10kW. The operating frequency has been chosen to be 20kHz. There are several possible solutions for the topology of the converter. The choice of topology has been strongly influenced by technological considerations.

CONVERTER TOPOLOGIES FOR THE 10kW - POWER RANGE

Considering the high supply voltage and the switching frequency of 20kHz, converter topologies applying a voltage in excess of the supply voltage to the transistors, or necessitating a power transformer with a low leakage inductance have been eliminated. Transformers with a low leakage inductance that respect the insulation standards are difficult to manufacture. The one transistor "forward" converter and "push pull" converter are thus eliminated.

The choice of the converter topology is reduced to two converter types :

- The full-bridge (figure 1) which is a symmetrical structure with alternating magnetic polarisation.
- The asymmetrical half-bridge (figure 2) in which the magnetic polarisation is uni-directional.

Figure 1 : Full Bridge Converter.

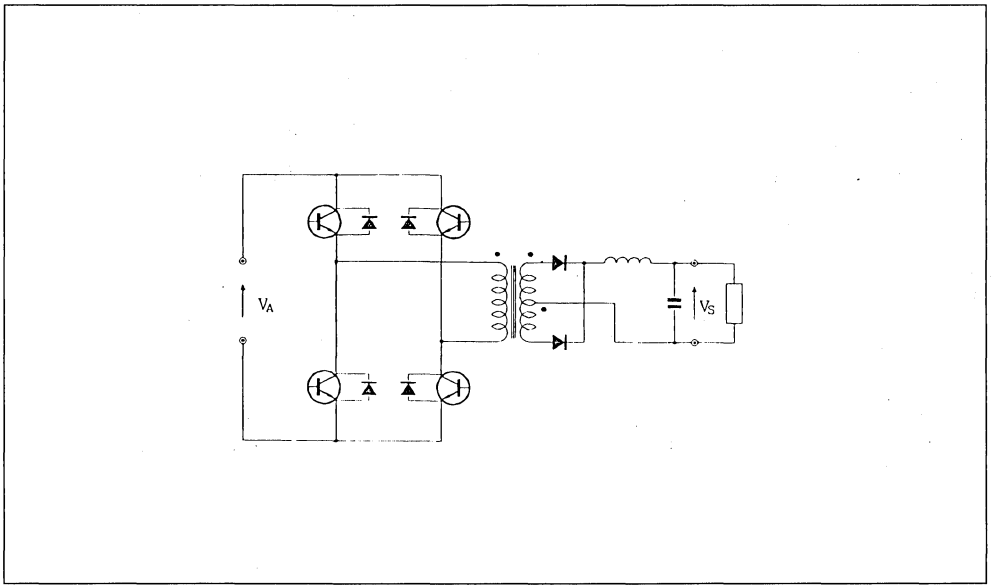
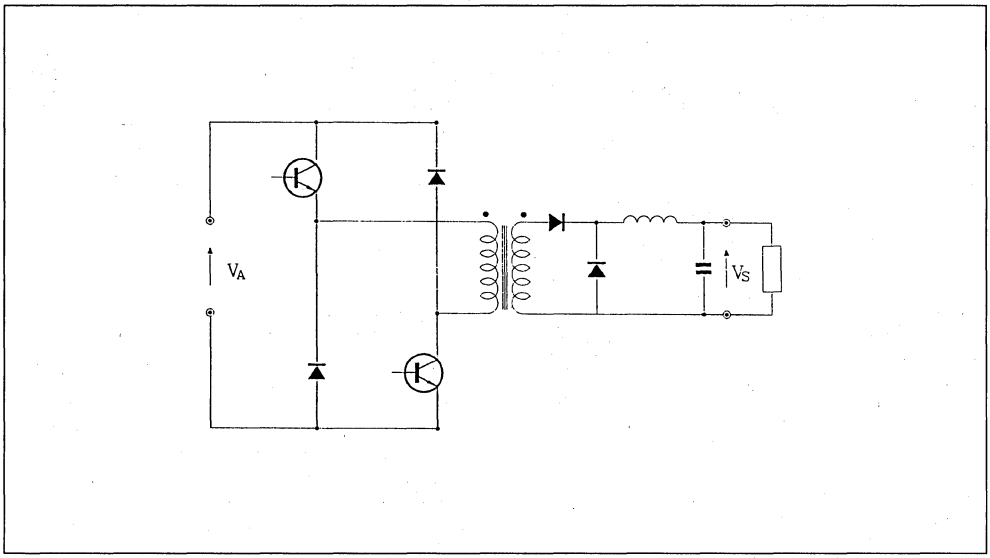


Figure 2 : Asymmetrical Half Bridge FORWARD Converter.



CHOICE CRITERIA

Theoretically the complete bridge is the solution for high output power : at equal output power the transformer is half as big as that of an asymmetrical half bridge.

In practice, there exist a certain number of secondary parasitic phenomena which reduce the advantages of a symmetric structure in comparison to the half bridge. One of these phenomena is that a full bridge is never perfectly balanced. A circuit to correct the symmetry must therefore be designed in and the transformer must be slightly larger to avoid saturation due to dissymmetry.

The full bridge necessitates the use of 4 bidirectional switches and therefore of 4 galvanically isolated drive circuits, whilst the half bridge only requires 2. Simple switching aid networks cannot be directly applied to a full bridge, due to the direct coupling between the upper and lower switches. Supplementary chokes therefore have to be added which would complicate the circuit considerably.

The asymmetrical half bridge does not have these problems. The input current of the asymmetrical half bridge has a bad form factor. Consequently and contrary to a full-bridge, the input filter capacitors of a half-bridge are subject to a high RMS-current.

These different considerations led us to choose an asymmetrical half bridge. The experiment has shown that our choice was reasonable and we think today that for an output power in the 10kW area, the asymmetrical half bridge presents the best technical and economical compromise.

For a substantially higher output power the full bridge seems to be preferable. Alternatively, 2 asymmetric half-bridge circuits can be used, operating in antiphase.

THE ASYMMETRICAL HALF BRIDGE

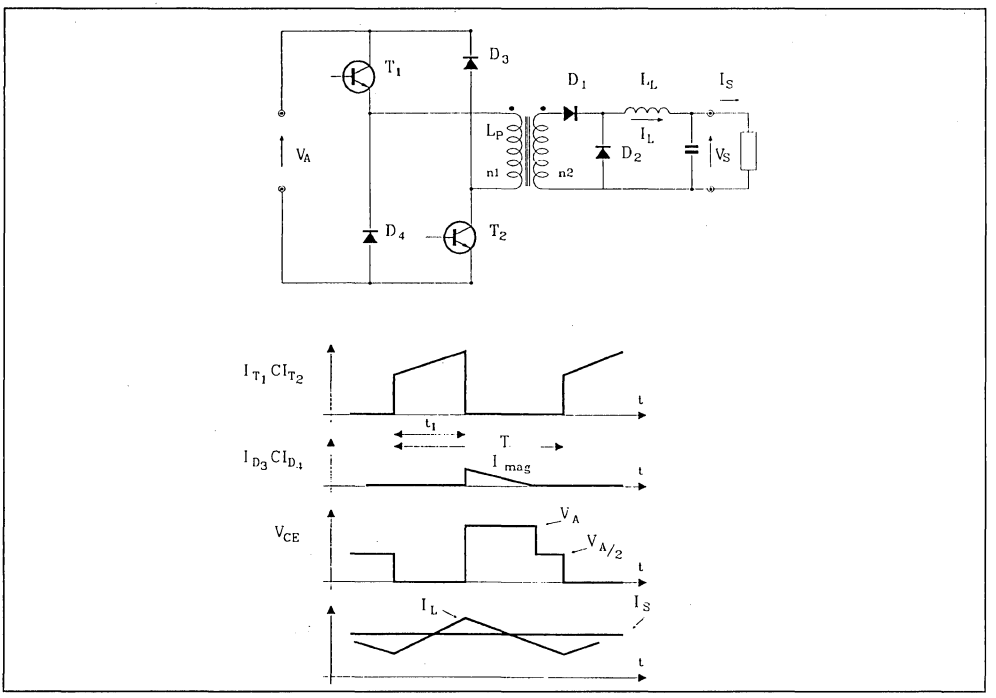
GENERAL CIRCUIT DIAGRAM

The figure 3 shows the basic circuit and the principal voltage and current waveforms of an asymmetrical half bridge.

In this converter, the transistors T1 and T2 are driven simultaneously. They conduct for a time τ and are off for the rest of the period, $T - \tau$.

The diode D1 on the secondary conducts while the transistors are conducting (time τ). The secondary current (during time τ) goes through the inductance L. The diode D2 operates as a free-wheel diode (time $T - \tau$).

Figure 3 : Forward Asymmetrical Half Bridge Converter.



THE MAIN FEATURES OF AN ASYMMETRICAL HALF BRIDGE

The main features of an asymmetrical half bridge are :

- The power transformer and ferrite core. Litz wire is used for the primary because of its reduced skin effect. The low leakage inductance is obtained by winding a half-primary and a half-secondary onto each leg of the transformer. A reduction of the duty cycle with increasing input voltage limits the magnetisation of the core. This reduces the transformer's volume to a minimum.
- The Power Switches. The simultaneously driven power switches must be fast. Their drive must not be disturbed by parasitic signals. To obtain a good voltage safety margin, turn-off snubbing networks are necessary.
- Rectifiers and filter components. The choke inductance is the principal component of the output circuit. As far as possible, the inductance must be high, so that the maximum current in the power switches and the recifier diodes is as low as possible. Fast recovery diodes are used to reduce the switching oscillations. The use of an RC network in parallel to each diode reduces the voltage ripple on the output.
- Safety. In power equipment, safety is a fundamental element which must be considered from the very first stages of design. The principal active safety elements we introduced are :
  a. current limitation for the power switches,
  b. a soft start,
  c. protection against overload on the output,
  d. control of auxiliary voltages,
  e. control of the transformer core magnetisation,
  f. minimum conduction time for complete discharging of the snubbers.
- Control. The control circuit was developed with an integrated circuit, the UAA4006. Amongst other things, this circuit contains several protection functions. The output voltage is detected by means of an extra winding on the filter choke. The free wheel diode is conducting during the demagnetisation phase of the filter choke. During that time interval the voltage across the filter choke is equal to the output voltage. This voltage is fed to the control IC. The control IC also provides the features a-f listed above for safe operation.

THE POWER SWITCHES

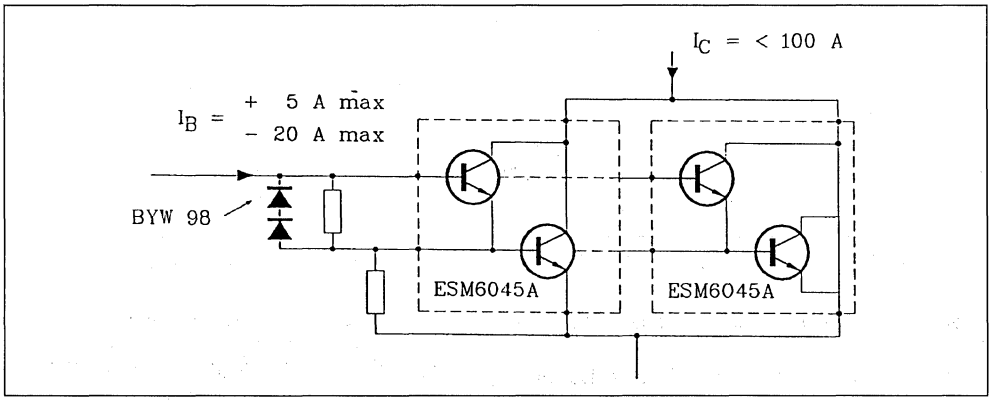
For the 10kW switched mode power supply operating from the 380V - 440V mains two fast power switches able to switch 100A with a maximum supply voltage of 700V are required.

There are two possible solutions when choosing the power transistors.

1. To choose transistors with V_{CEW} higher than the maximum voltage the switch has to sustain. Theoretically, this would allow a design without turn-off switching aid networks.
2. To choose transistors with V_{CEW} higher than half the maximum supply voltage and with a V_{CEV} rating higher than the maximum voltage the switch has to support.

The second solution has the advantage of better switching performance than the first one.

Figure 4 : Power Switch.



Note that this type of transistor is mounted in an ISOTOP package. The insulation voltage between the die and the bottom of the case is 2.5kV r.m.s. This avoids not only external insulation but also considerably reduces the capacitance between the transistor and the heat sink, hence gives a reduction in RFI.

A certain number of precautions are required when using transistors with V_{CEW} lower than the maximum voltage, to which the switch is subjected :

- A base-emitter resistance must be connected to each transistor (value stated on the data sheet), which insures a static blocking voltage of 700V and therefore protects the switch against any problem arising from the negative bias. Nevertheless the auxiliary voltage should be monitored.
- A turn-off switching aid network must be connected to each switch to insure that the load line stays in the RBSOA at switch off. In our case, the network has to be calculated so that the collector-current reaches zero before the collector-emitter voltage reaches 450V.
- The driver circuit must be capable of providing sufficient base current with an optimized waveform.
- The conduction time of each transistor will always have to remain higher or equal to the time necessary to discharge the snubber capacitor even in the case of an overload.

If these precautions are respected, the voltage safety margin is the same as if very high voltage transistors were being used.

The switching times must be as short as possible since the minimum conduction time is of the order of 7µs and during a short circuit at the output about 2 to 3µs.

Our choice is a Darlington combination using ESM6045A (fig. 4).

PRINCIPAL CHARACTERISTICS OF THE TRANSISTORS USED

ESM6045A

- V_{CEW} > 450V
- V_{CEV} > 1000V (V_{BE} = − 5V)
- V_{CEsat} > 2.0V
- t_{fi} < 0.6µs
- t_{si} < 6.0µs
- t_c < 2.0µs

} I_C = 60A and I_B = 2.4A, T_j = 100°C

BASE DRIVE CIRCUIT

The base drive turns the transistor switches on and off as determined by the electronic control and safety circuit.

The positive base drive is regulated in order to maintain the power transistors in quasi-saturation. This reduces the effect of parameter spread of the power transistors and simplifies the paralleling. The storage and fall times are also reduced by this means.

The base drive must have a high immunity to electrical disturbances (dV/dt for example). The input interface uses a driver transformer with a bobbin with two segments. The base drive circuit for one switch is shown in figure 5.

Figure 5 : Base Drive Circuit.

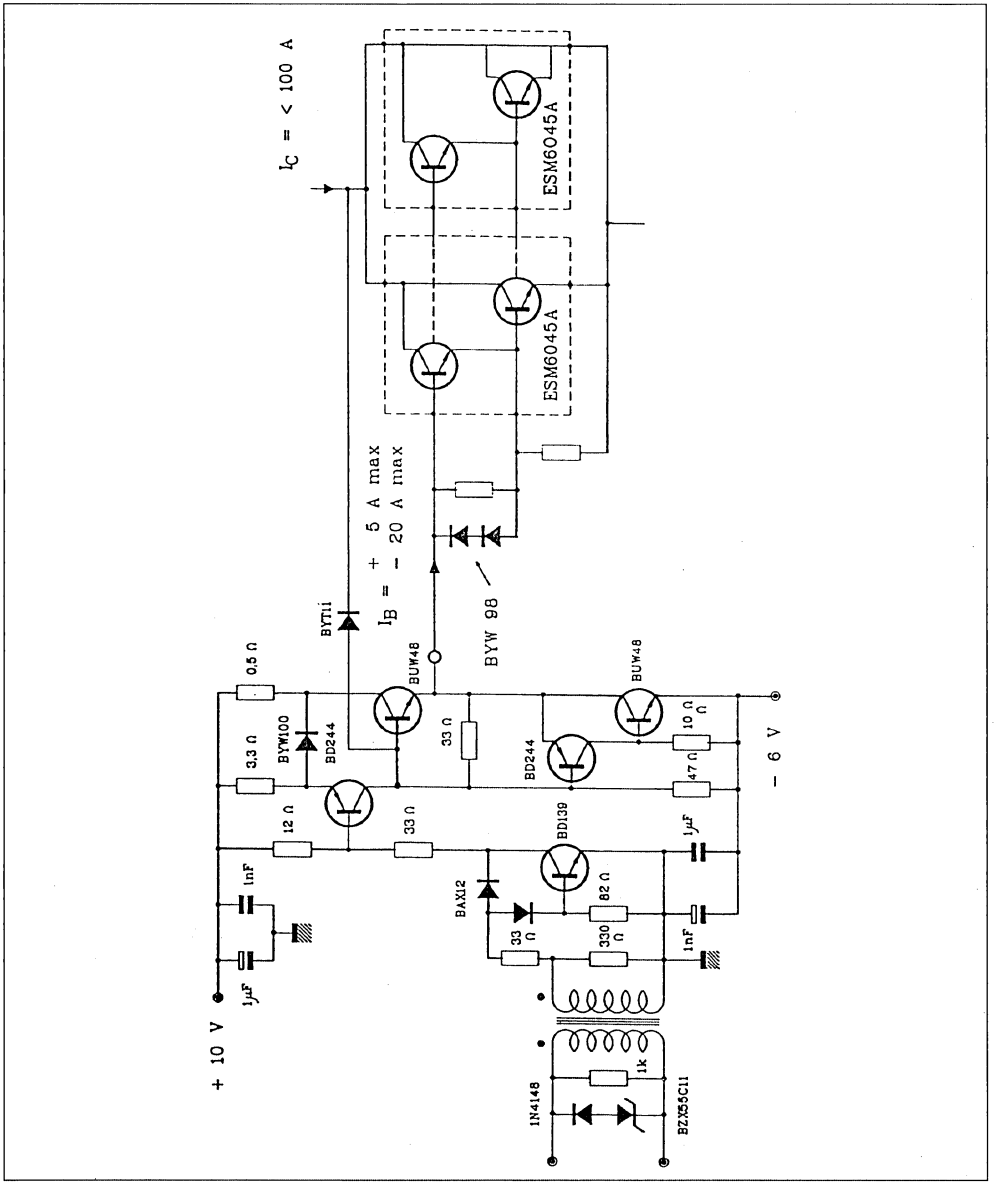
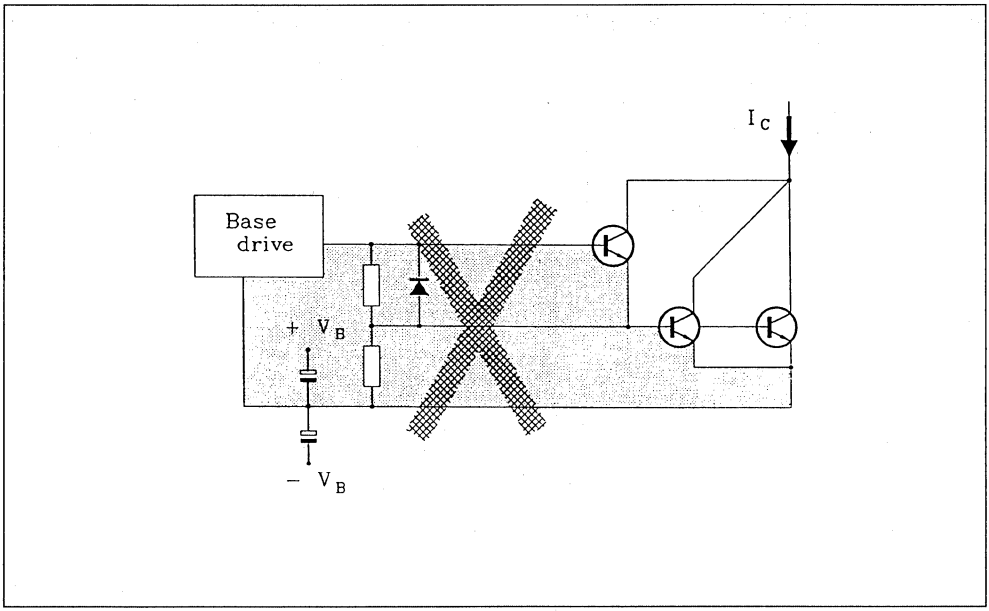
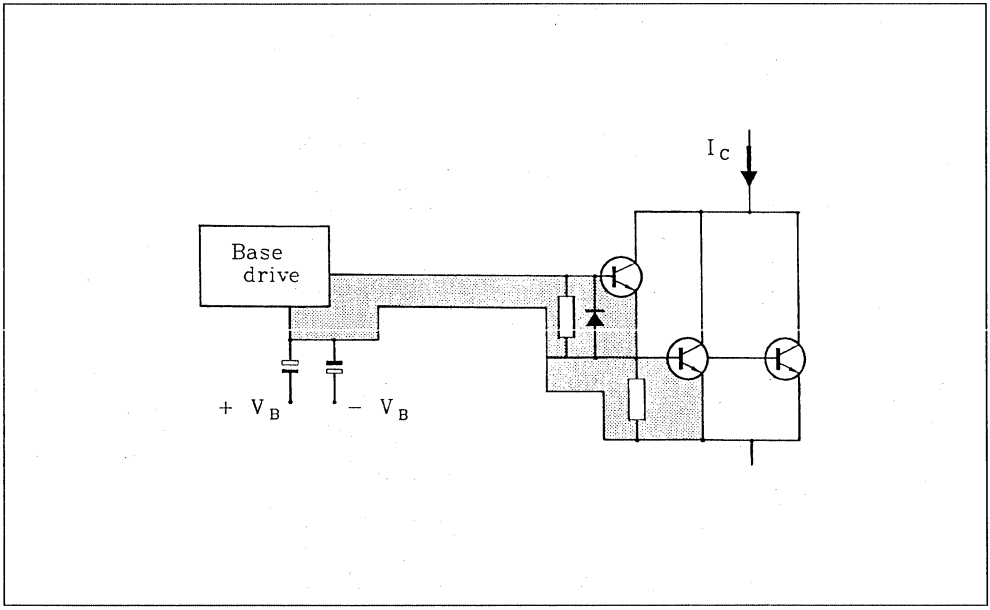


Figure 6 : Wiring for High Power Switching.

a) Base Drive with Poor Wiring.



b) Base Drive with Recommended Wiring.



WIRING PRECAUTIONS

Special care must be taken concerning the wiring of the fast high power switches. The switching speeds being in the order of 200A/µs (much more if they are not limited), current/voltage oscillations are induced in the leads.

It is therefore necessary to pay particular attention to the wiring to reduce the parasitic inductance :

- The connections between transistors, and to the drive must be as short as possible (figure 6) and form very small wiring loop areas.
- Try to obtain the highest symmetry possible between the paralleled transistors. The spread of the transistor -characteristics is only of second order, (for components of the same type and from the same manufacturer) the spread in switching times is essentially a result of the wiring dissymmetry.
- The reference point for the driver must be the emitter connection of the power transistor. Figure 6a shows an example where the zero point of the driver circuit is disturbed by voltages created by the fast rise and fall (dI/dt = 50A/µs) of the output current of the driver stage.
- The decoupling capacitors must be connected as close as possible to the switches.
- The decoupling capacitors must have low equivalent series inductances and resistances. To further reduce the impedance of the decoupling capacitor, multilayer film capacitors with low parasitic impedance have been connected in parallel to the electrolytic capacitors.

THE SNUBBERS

A turn-off switching aid network is needed due to the V_{CEW} rating of the switching transistors which is lower than the supply voltage. To obtain high efficiency from the power supply, switching aid networks with energy recovery have been choosen [2].

Due to the reverse recovery behaviour of the diodes these snubbers do not operate in an ideal way. The reverse recovery current of the diode D_{AC3} (fig. 7) causes some problems.

The reverse recovery time, t_{rr}, is dependant on the diode technology and the switching conditions.

The reverse recovery current of this diode has several consequences.

- With a low load on the output of the power supply it produces a reverse collector-emitter current in the transistor. The transistor can be protected against this current by means of an antiparallel diode between collector and emitter.
- The reverse recovery current of D_{AC3} partially recharges the capacitor C1 (and discharges C2), figure 7.
- It also flows through the choke L. If the stored energy is not discharged it will generate overvoltages. The diode D_{AC4} clamps and limits this overvoltage to the supply-voltage. Unfortunately, the current through this "clamp" recharges C1 still more (fig. 8).

Diode D_{AC3} must be chosen with care. To reduce the parasitic phenomena it must have a very fast recovery characteristic. The type BYT30-1000 was used.

The resistor (R) parallel to the diode D_{AC1} allows the complete discharge of the capacitor C1 during the conduction time of the transistor (figure 8). This increases the snubber losses, but they are still significantly reduced (~ 30%) when compared to those of a conventional RCD-snubber.

These modifications to the snubber with energy recovery are justified with high switching frequencies (e.g. : 20kHz) and when the minimum conduction time is short. In this case the snubber must reset very rapidly and the parasitic phenomena of the components can no longer be neglected.

The other components of the snubber are chosen in the same way as those for the conventional RCD-snubber.

Figure 7 : Non Dissipative Snubber.

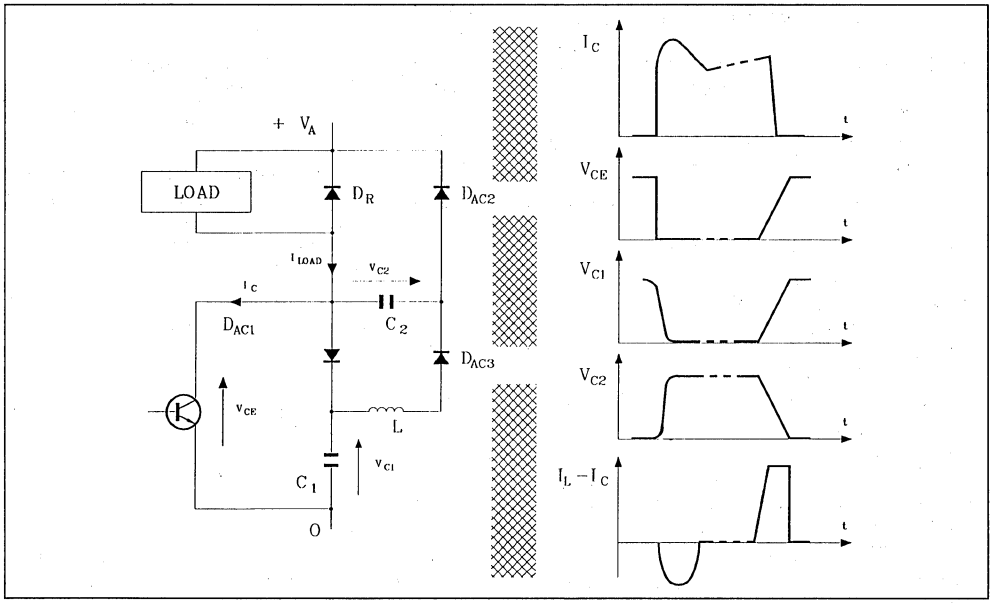
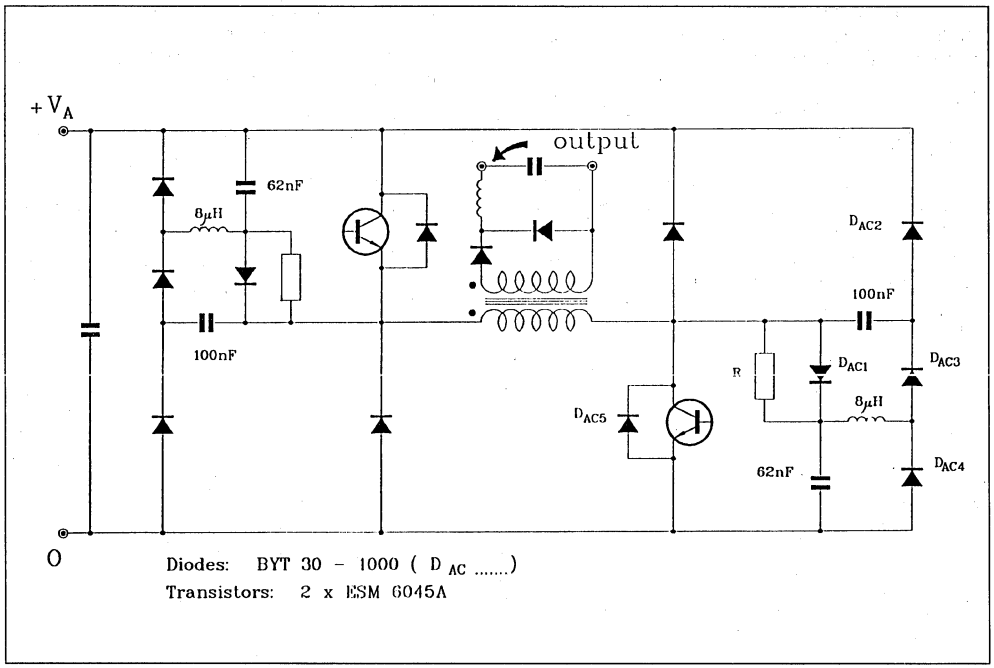


Figure 8 : Complete Diagram of a Power Converter Output Stage.



CONCLUSION

The technological constraints are very important in the design of converters supplied from the 380V - 440V mains.

The use of high voltage transistors with a V_{CEW} rating lower than the supply voltage requires certain precautions, but enables a fast switching speed to be achieved.

The magnetic components (transformer, filter-choke), technological choices are also important since they affect the overall performance of the equipment as well as their influence on the size of the active components.

Adding the snubber with energy recovery increases the efficiency of the power supply and the overall reliability.

This circuit constitutes a basis for the development of switched mode power supplies in the power range of 1 to 10kW for power supply, welding induction heating, battery charger and other high power applications.

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POWER SEMICONDUCTORS FOR HIGH FREQUENCY AC/DC CONVERTERS SUPPLIED ON THE 380/440V MAINS

By L. PERIER & J.M. CHARRETON

INTRODUCTION

This paper is the result of the development in our laboratory of different switches and converters able to operate at ultrasonic frequency, supplied directly from the rectified 380/440V mains.

This paper presents, in the first part, a typical specification for the converter and power switches.

The second part describes several switches and driving circuits optimized for those requirements.

1. SPECIFICATION :

Our objective was to develop switches and drivers optimized for AC/DC converters supplied on the industrial 380/440V mains, switching at ultrasonic frequency as used in Switch Mode Power Supply, battery charger or welding converter applications.

We based our development on the design of a 5KW asymetrical half bridge (2 transistor forward) converter. An equipment of 10kW could be design with the same switches mounted in full bridge or in the assembly of two asymetrical half bridge operating in antiphase.

Because of the high voltage supply, the blocking voltage capability of the switches is 1000V. In order to minimize the transformer and filters size and the acoustic noises a switching frequency over 20kHz is required.

In a 5kW asymetrical half bridge supplied on the 380V mains, the maximum duty cycle of conduction of the power switches is 50% of the total period. The current in the switch is 15A. Consequently the RMS current in the switch is 11A.

In order to use a very small heatsink the conduction losses in each switch are minimized (30W).

Auxiliary supplies for the power switches are also excluded in order to minimize the volume and the cost of the auxiliary circuitry.

2. A 1000V MOSFET SWITCH :

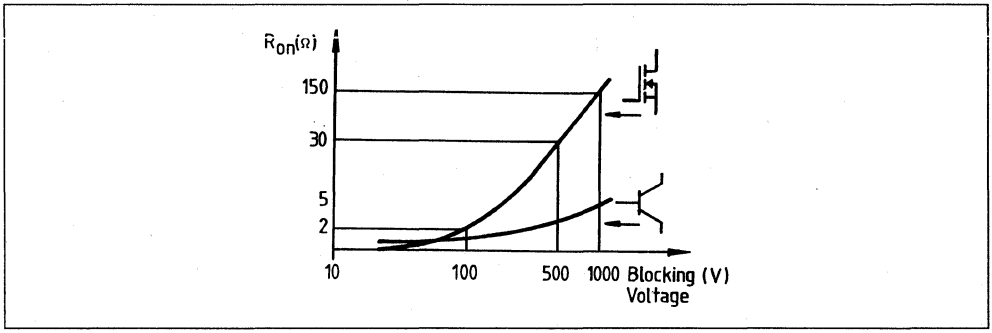
Power MOSFET technology is well adapted for the design of switches able to operate at high frequency. 1000V MOSFETs exist and they present the classical advantages of the MOSFET technology : low drive consumption, good turn-off safe operating area, high over current capability, ...

But the resistance of the epitaxial layer required to widthstand the blocking voltage V_{DS} (if 250V) is approximately proportionnal to $V_{DS}^{2.5}$. Consequently, the on resistance R(on) of the Power MOSFET increases rapidly with the blocking voltage capability V_{DSS}.

The only way to reduce the conduction losses with a 1000V MOSFET is to operate at very low current density and to use very large die areas.

In our design, one switch requires a Ron of 0.15 ohm (Tj = 25°C). That means the paralleling of 25xSTHV102 (3.5 ohms in SOT93 package) or more reasonably 5xST5MG40 (0.7 ohm in ISOTOP package).

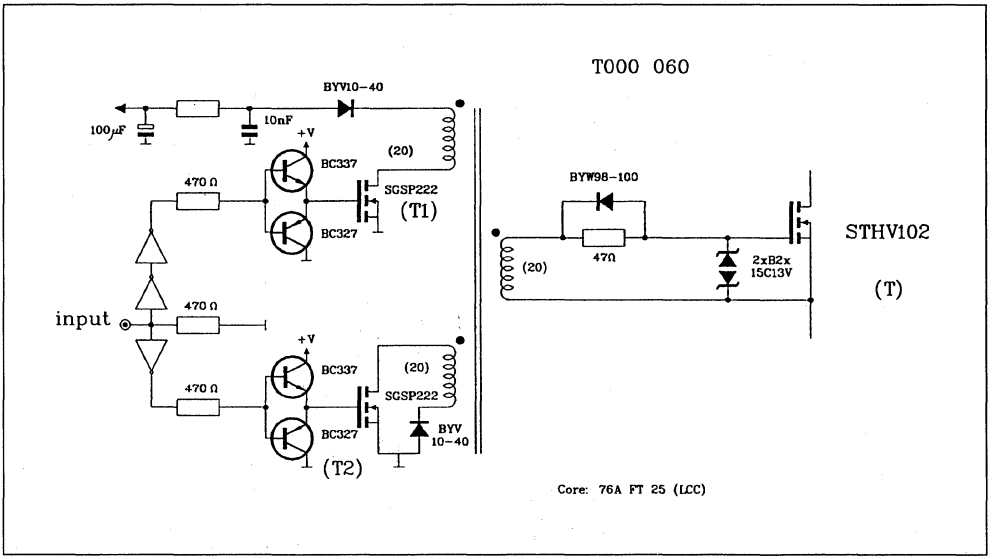
Figure 1 : ON Resistance $R_{(on)}$ versus Blocking Voltage V_{off}.
(die area = 1mm2 - junction temperature = 100°C).



The gate drive presented in figure 2 provides the galvanic isolation of the drive signal and avoids auxiliary supplies.

When the signal MOSFET T1 is on, the power MOSFET T is on. When the signal MOSFET T2 is on, the driving transformer is short circuited and discharges the gate source capacitance of T, turning Power MOSFET T 'off'.

Figure 2 : Schematic of the Power Switch and Driver.



3. A CASCODE/EMITTER SWITCHING SWITCH :

50V high density Power MOSFET can operate at a current density 100 times the current density of 1000V MOSFET for the same conduction losses (typically 2A/mm2 instead of 0,02A/mm2).

The current density of a 1000V bipolar transistor is in the region of 0.4A/mm^2. For applications requiring the same current capability and the same dissipation, the 1000V MOSFET requires about 30 times more silicon than the equivalent bipolar solution resulting in a substantially higher power switch cost.

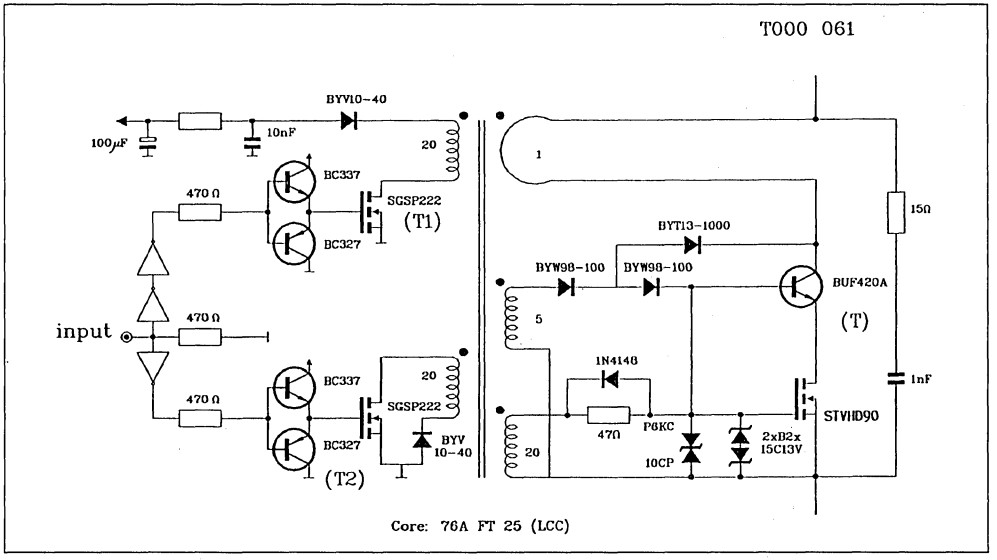
Bipolar transistors developed with highly interdigitated technologies such as the Easy-To-Drive technology (ETD) have a very fast fall time compatible with operation at high frequency.

Consequently a solution using a high density 50V Power MOSFET (STVHD90) and a 1000V bipolar in ETD technology (BUF420A) in cascode configuration has been developed.

The driving circuit presented in figure 3 requires only one transformer to provide the voltage control of the MOSFET and the base current of the bipolar.

When the signal MOSFET T1 is on, the power switch T is on. The turn-on of the signal MOSFET T2 turns-off T.

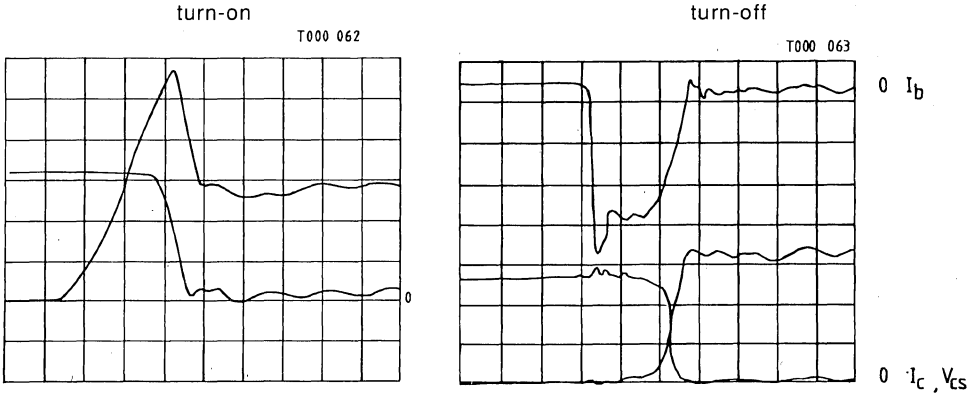
Figure 3 : Schematic of the Cascode Switch and Driver.



As presented in figure 4, the cascode switch is very fast at turn-off. A Storage time less than 500ns and fall time less than 20ns have been obtained. The rate of fall of the collector current is very high (2000A/µs). The use of low inductance wiring methods and packages is a condition for the design of this circuit. A turn-off snubber (R, C) limits oscillations and maintains the bipolar switch inside its specified Reverse Bias Safe Operating Area.

The rate of rise of the collector current (dI/dt)on at turn-on is limited in the converter by the leakage inductance of the power transformer. Therefore turn-on speed of the switch is not very critical. A (dI/dt)on of 50A/s has been obtained.

Figure 4 : Cascode Switching Waveforms.



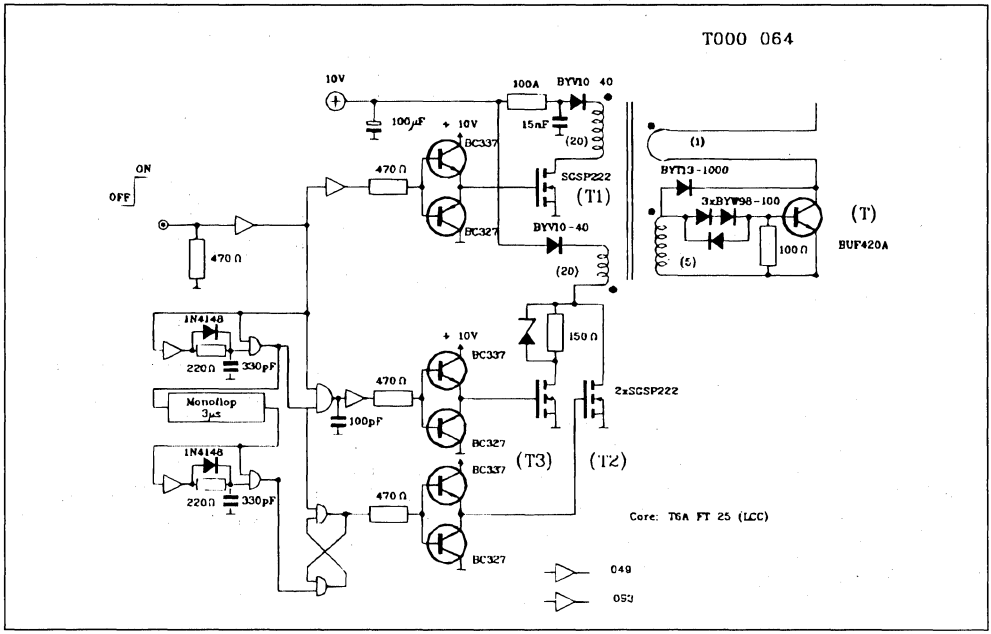
Ic, Ib : 5A/div. Vcs : 200V/div. t : 0,2µs/div.

4. BIPOLAR SWITCH :

The elimination of the 50V high density MOSFET is the last step to reduce the conduction losses and the number of power packages. But the remaining bipolar transistor must be driven with a negative bias on the base/emitter junction in order to obtain fast turn-off and a blocking voltage capability extended up to V_{CEV}.

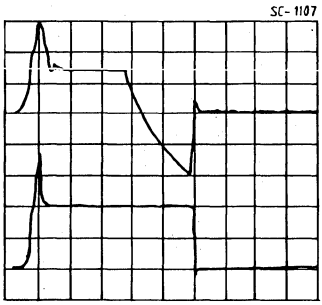
In the circuit presented in figure 5, when T1 is on the power switch T is on. T is turned-off when T2 and T3 are on. T2 drives the negative base current of T and is turned-off after 3µs. T3 resets the magnetic flux in the driver transformer before the next turn-on of T.

Figure 5 : Bipolar Switch and Driver.



With this circuit, a BUF420A switches 20A with a storage time of 2µs and a fall time of 50ns at Tj = 100°C, see figure 6.

Figure 6 : The Bipolar Switching Waveforms.



I_b : 2 A /div

I_c : 10A/div.

5. CONCLUSION :

This paper proposes different switches and drivers able to operate in AC/DC converters switching at ultrasonic frequency and directly supplied from the rectified 380/440V mains.

The availability of 1000V MOSFET makes possible the design of switches with high frequency capability, large turn-off safe operating area, large overcurrent capability and easily controlled gate drive. A limitation of this solution is in the trade-off between the conduction losses and the current density. A medium current 1000V MOSFET switch needs several packages in parallel or a big heatsink.

A switch developed with 1000V bipolar transistor has low conduction losses and few parallel packages. Thanks to the use of highly interdigitated very fast technology (ETD) the switching speed is comparable to the MOSFET solution. But the turn-off delay time is longer and the driving circuitry is more complex than a MOSFET circuit.

A Cascode circuit has the advantages of both bipolar and MOSFET technologies. It allows low dissipation with short turn-off delay time and simple driving circuitry. High density low voltage MOSFETs minimises the increase of the forward drop. Because of the very fast turn-off speed, special care must be taken with the wiring.

Driving circuits using only one transformer to provide the galvanic isolation power/logic and the energy to drive the power switches are also presented and adapted to each configuration of power switch.

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OPTIMISED POWER STAGES FOR HIGH FREQUENCY 380/440VAC MEDIUM POWER SWITCH MODE SUPPLIES

By C.K. PATNI & L. PERIER

ABSTRACT

This paper presents the elements necessary to make the optimum choice of power semiconductors (for the transistors and secondary diodes) and the power stage configurations for medium power SMPS (from 1kVA to 15kVA).

The power stage practically realized comprises of an asymmetrical bridge forward converter. An optimised power switch combining bipolar and MOSFET technologies is developed. It is capable of switching in excess of 50A at 25kHz on the 380/440VAC rectified three phase mains.

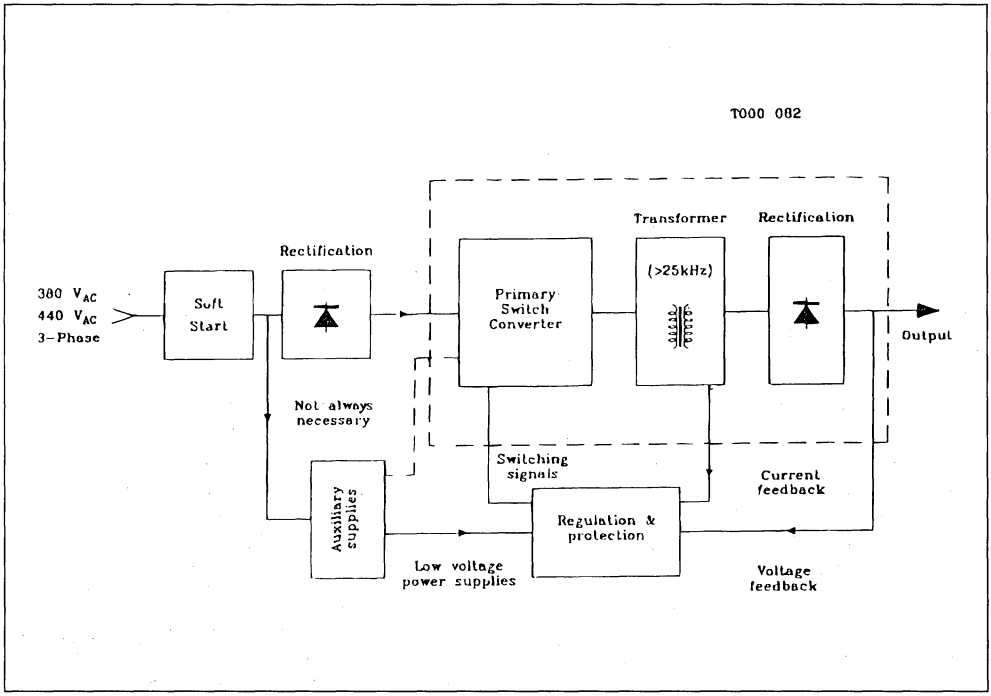
Secondary diode choice depends largely on the transformer ratio and the desired output D.C. voltage. Conduction losses at 25kHz govern the choice of secondary diodes.

INTRODUCTION

System designers of switch-mode solutions for electric welders, battery chargers and computer power supplies need to choose the power-stage configuration, power semiconductors and regulation best suited for their application. This paper provides data necessary to make this choice.

Figure 1 illustrates a system block diagram of a typical medium power SMPS with the primary operating directly on the 380/440VAC rectified mains. The paper limits the discussion to the power-stage of the SMPS. Power stage configurations such as asymmetrical bridge, full-bridge and half-bridge converters are compared. Bipolar and MOSFET technologies are compared. Schottky and fast recovery epitaxial diodes are considered for the secondary rectification.

Figure 1 : Block Diagram of a Medium Power SMPS.

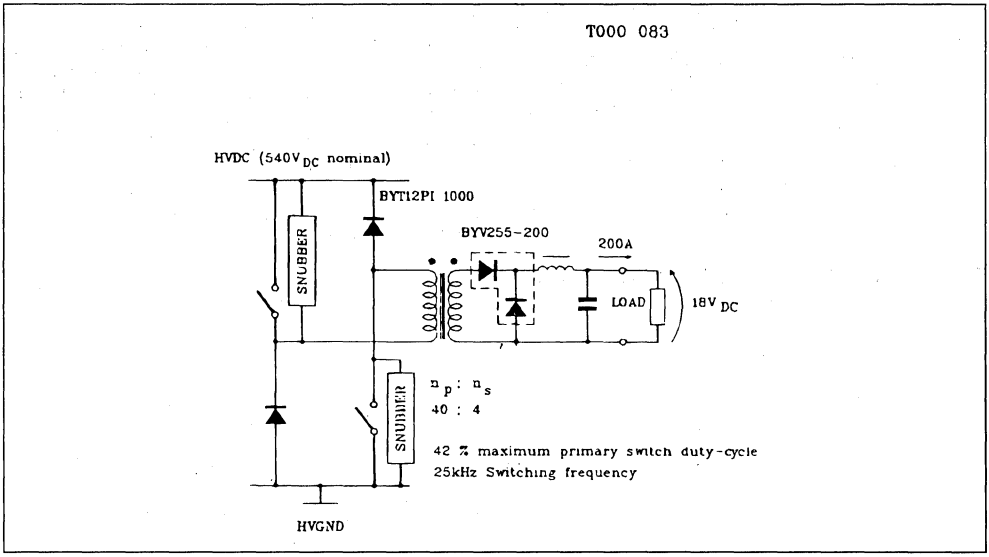


POWER STAGE CONFIGURATIONS

For medium power applications (1kVA to 15kVA), the choice of the converter on the 3-phase industrial mains is between the asymmetrical bridge, capacitor-split half-bridge and full-bridge converters [1]. The half-bridge and full-bridge converters are symmetrical converters and thus require smaller input filtering than asymmetrical bridge converters. However, it is possible to combine two asymmetrical bridge converters operating in antiphase in order to obtain a power stage, which viewed from its input and output current waveforms, appears to be a symmetrical full-bridge converter.

The asymmetrical bridge converter (figure 2) comprises of two power switches in series with the load connected between the two switches. Simultaneous conduction of these power switches when a fault condition exists on the secondary of the transformer is not catastrophic as there is at least the leakage inductance of the transformer limiting the rate of rise of primary switch currents. The controlled rate of rise of primary current enables low-cost feedback protection circuits to react to the fault condition and turn-off the primary switches.

Figure 2 : Asymmetrical Bridge Converter - The Developed Power Stage.



The use of turn-off switching-aid-networks (snubbers) does not pose a problem in asymmetrical bridges. In half-bridge and full-bridge converters, the use of turn-off snubbers generally necessitates the use of turn-on snubbers required to limit the rate of rise of primary switch currents [2].

The developed power stage utilizes the asymmetrical bridge converter because of these reasons.

For very high output power capability (in excess of 10kVA), the full-bridge converter can be the optimum choice provided the circuitry necessary to maintain volts-seconds symmetry can be easily implemented. The full-bridge operates the transformer in two magnetic quadrants. Consequently the size of the transformer can be reduced. Figure 3 illustrates a full-bridge converter which incorporates the advantages of the asymmetrical bridge structure (no catastrophic simultaneous conduction of transistors and easy snubber networks) with the advantages of the symmetrical converter of reduced transformer size.

TECHNOLOGY CHOICE

Bipolar and MOSFET technologies are best adapted for high frequency (greater than 20kHz) medium power SMPS. Figure 4 illustrates the on-state resistance for 1mm^2 of silicon surface versus blocking voltage for high voltage power MOSFETs. The resistance of the epitaxial layer required to withstand blocking voltage V_{DS} (in excess of 250V) is approximately proportional to $V_{DS}^{2.5}$. Consequently, even if this theoretical limit is approached, the on-state resistance increases rapidly as blocking voltage V_{DS} increases for high voltage power MOSFETs.

Figure 3 : A Quasi-asymmetrical Full-bridge Converter.
– Transformer provides inductance between two switches in series.

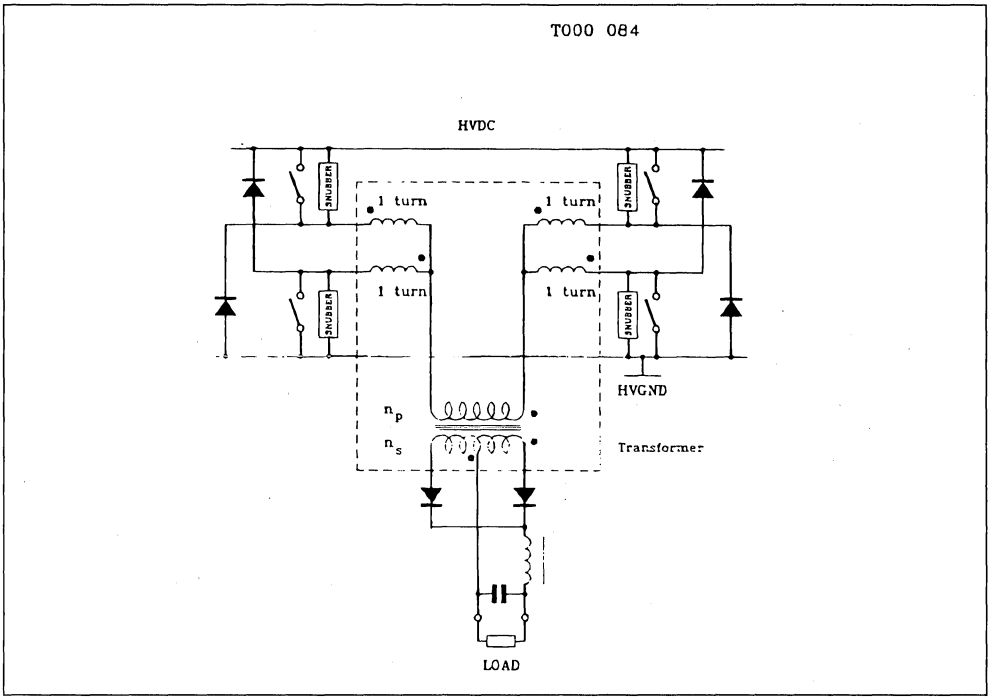
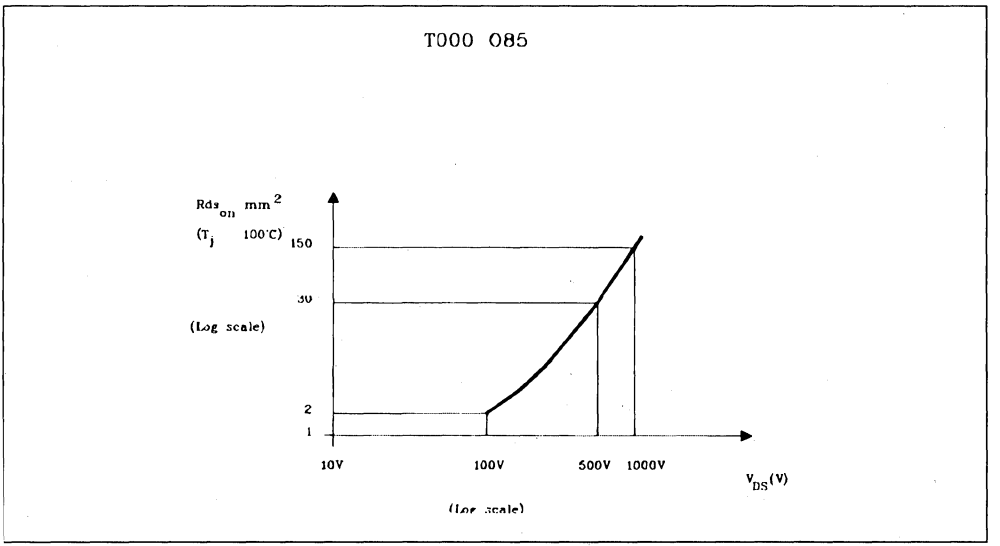


Figure 4 : MOSFET Blocking Voltage versus on-state Resistance/mm^2.



The current density for a 1000V bipolar transistor, such as a BUF410A is in the region of 0.4A/mm^2 when conducting a nominal current of 10A with an on-state collector-emitter voltage of 2V maximum at 100°C junction temperature. The equivalent on-state resistance for a 1000V bipolar is thus approximately 5 Ohm/mm^2 whereas for a 1000V Power MOSFET is 100 Ohm/mm^2. For an application specifying only nominal switching current capability, the Power MOSFET solution requires 30 times more silicon than the equivalent bipolar solution (not considering the drive requirements) resulting in substantially higher power transistor cost.

Even though higher current density is achieved with bipolar transistors, the Power MOSFET has the clear advantage of a larger safe operating area at turn-off, larger peak current capability and easy voltage controlled gate drive. The 1000V bipolar transistor has the disadvantage of longer turn-off delay time (due to its storage time) and high drive current requirements. A cost comparison of a Power MOSFET based solution with a bipolar based solution should thus be based on cost of the switch together with its drive, protection and auxiliary power supply circuits.

Quantitative comparison is complicated by the very different operational characteristics of Power MOSFETs and bipolar transistors. However, qualitative comparison leads the authors to conclude the following :

1) In medium power SMPS, where bipolar and Power MOSFET technologies can be used, the technology comparison must be based on cost evaluation of solutions meeting the specification both for PEAK transistor switching current as well as AVERAGE/RMS transistor switching current.
2) Generally the Power MOSFET is sized for the RMS transistor switching current, whilst verifying that the peak current capability of the device meets the specification.
3) The bipolar solution is sized on the peak transistor switching current specified in the application.

THE DEVELOPED POWER STAGE

The developed power-stage has the characteristic listed in table 1. The asymmetrical bridge forward converter was used with the maximum duty cycle limited to approximately 40%. The continuous rated primary current was 20A (for 40% duty cycle). The peak primary switch current capability was 50A. The transformer design (provided in appendix I) had a primary to secondary turns ratio of 10 to 1. Consequently the continuous rated secondary output current was 200A at a secondary output voltage of approximately 18V. The secondary output peak current was 500A when primary switch current was 50A.

Table 1 : Developed Power Stage Characteristic.

Comments	Value
Input Supply Voltage	380/415/440V$_{AC}$
Continuous Primary Current	20A
Peak Primary Current	50A
Maximum Duty Cycle	40%
Switching Frequency	25kHz
Continuous Secondary Current	200A
Peak Secondary Current	500A
Secondary Voltage (nominal)	18V

THE ASYMMETRICAL BRIDGE CONVERTER

A solution for the converter, based on bipolar and Power MOSFET technologies, encompassing the advantages of high switching current density and voltage controlled drive, was developed : this converter for the power stage was based on the CASCODE switch [3]. Due to the relatively large nominal primary switch current (20A), a bipolar based solution was necessary. The CASCODE switch required a simple voltage controlled drive signal. No floating auxiliary supplies were required as the base current for the bipolar transistor was provided by a proportional current transformer. Figure 5 illustrates the primary CASCODE switch (based on bipolar and MOSFET technologies) which is used in the asymmetrical bridge converter.

The switch comprises of a BUV298A bipolar transistor (B1) in ISOTOP package and a high density 50V (23 mOhm at 25°C) Power MOSFET STHVD90 (F1) connected in CASCODE. A 1000V Power MOSFET STHV102 (F2) provides the initial base current. A 50V Power MOSFET BUZ11 (F3) turns-on when the STHVD90 CASCODE MOSFET (F1) is turned-off. Consequently the collector current is extracted via the base through Power MOSFET F3. A turn-off snubber (comprising of R1, D1 and C1) maintains the turn-off within the reverse bias safe operating area (RBSOA) of the bipolar BUV298A.

The primary switch conduction losses (at nominal 20A current for 40% duty cycle) are approximately 30W at a 100°C junction temperature for the CASCODE switch. The primary switch could be based purely on 1000 volts Power MOSFETs (STHV102, 3.5 ohm at 25°C) in parallel. However, for 10 of these Power MOSFETs in parallel, under the same operating condition, the conduction losses would be approximately 90W.

Figure 6 illustrates a pulse transformer gate drive used with the primary switches. This gate drive provides positive and negative bias of the Power MOSFETs in the CASCODE switch. The pulse

transformer also provides the isolation between the primary switches and the control logic. With this gate drive, the asymmetrical bridge converter requires no auxiliary power supplies.

Figure 5 : The Developed CASCODE Asymmetrical Bridge Converter.

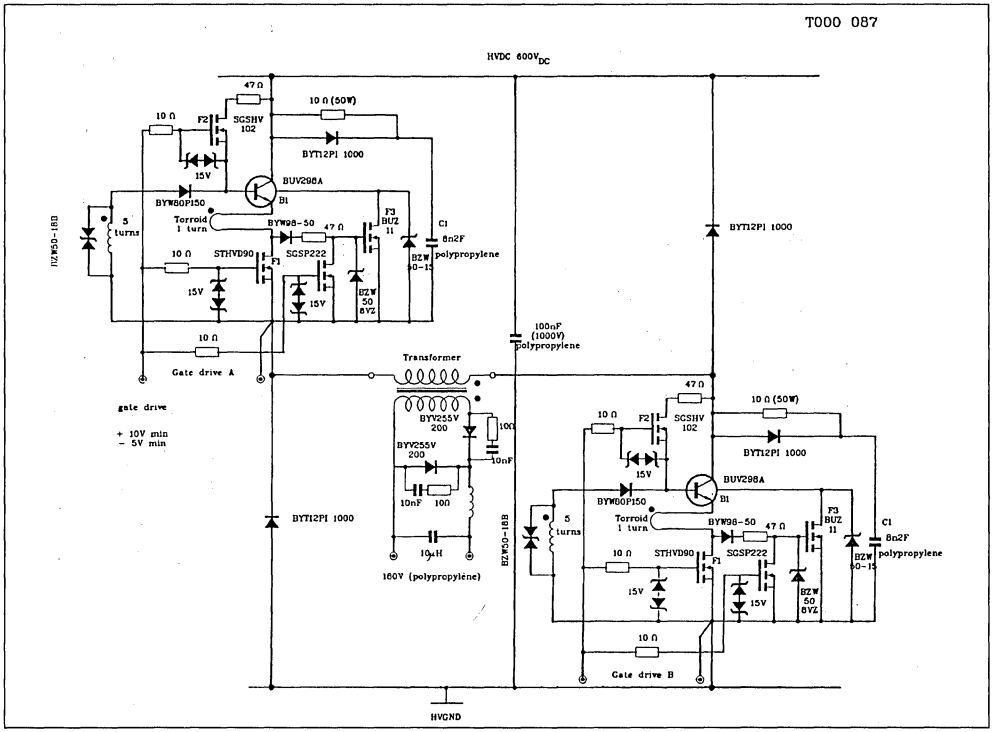
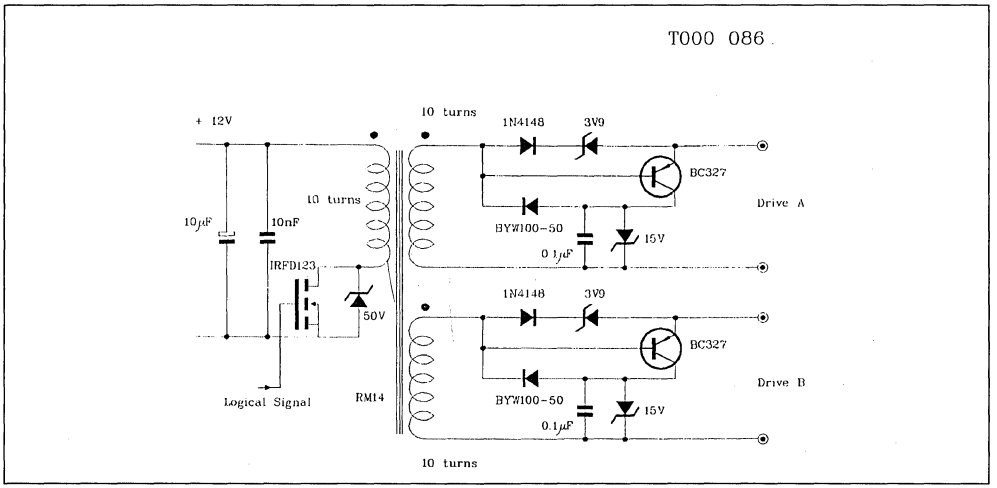


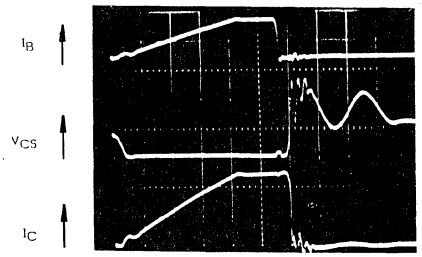
Figure 6 : Isolated Pulse Transformer based Gate Drives for Power Stage.



ASYMMETRICAL BRIDGE OPERATION

Figure 7 illustrates the extremely fast switching and short (less than 500ns) storage time at turn-off obtained using this CASCODE switch. The primary switch was tested with a bridge high voltage DC rail of 600V_{DC}, primary current of 50A at 25kHz switching frequency.

Figure 7 : CASCODE Primary Switch Commutation – (I_{PEAK} = 50A).



t = 1µs/div
I_B = 10A/div
V_{CS} = 200V/div
I_C = 20A/div

SECONDARY RECTIFYING DIODES

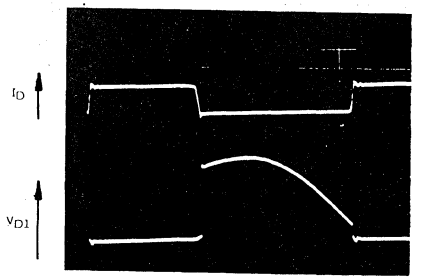
The transformer had a primary to secondary turns ratio of 10 to 1. Consequently the voltage experienced by the secondary diodes at 600V_{DC} HVDC was 60V in addition to any overvoltage due to parasitic inductances.

Schottky diodes which have extremely low conduction voltage (approximately 0.4V) can not be used for this application as they are limited in blocking voltage to approximately 50V. If the secondary output voltage was 5V (for example, computer applications), the transformer ratio would have been higher thus permitting the use of Schottky diodes.

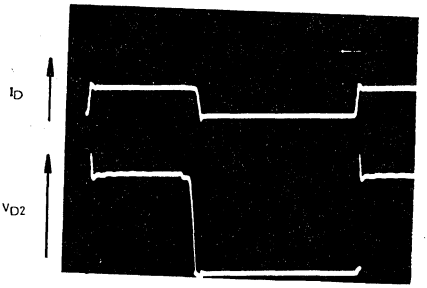
The diodes best suited for the specified secondary output are fast recovery epitaxial diodes ('FRED'). FRED diodes BYV255V200 were used in the circuit having conduction voltages of approximately 0.85V at rated current and at 125°C junction temperature. Figure 8 illustrates the blocking voltage experienced by the secondary diodes with resistor/capacitor snubber networks.

At continuous rated output power, each secondary diode conducts for approximately 50% of the time an average current of 100A. Assuming a junction temperature of 125°C, the instantaneous forward voltage drop is 0.85V at approximately 100A. Hence diode conduction losses are approximately 85W ; (0.85Vx100A = 85W).

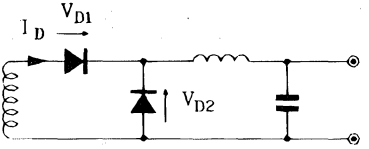
Figure 8 : Secondary Diode Switching Waveforms.



5µs/div
V_{D1} = 20V/div
I_D = 50A/div



5µs/div
V_{D1} = 20V/div
I_D = 50A/div



The leakage inductance between primary and secondary of the transformer is generally large such that the rate of decay of current in these diodes is controlled. Hence the reverse recovery is not critical. Thus at 25kHz switching frequency conduction losses are the prime criteria for the choice of the secondary diodes.

CONCLUSION

Bridge converters for medium power SMPS (1kVA to 15kVA) have been discussed. Turn-off snubbers and low-cost protection circuitry can be used with asymmetrical converters. A quasi-asymmetrical full-bridge converter has been proposed for high power SMPS which operate the transformer in two magnetic quadrants.

The 1000V Power MOSFET is a well adapted choice for low continuous power SMPS especially when high pulse current capability is specified for the primary switch. Bipolar transistors have high current density and are better adapted for medium power SMPS.

The choice of secondary diodes at 25kHz switching frequency is based primarily on conduction losses.

The developed power stage utilized the CASCODE configuration for the primary switch. This solution had the advantages of both the bipolar and Power MOSFET technologies. Fast epitaxial rectifying diodes (FRED) have been used in this power stage.

REFERENCES

1. SGS-THOMSON Microelectronics, 1984, "Transistor and Diodes in Power Processing", 187-198.
2. SGS-THOMSON Microelectronics, 1978, "The Power Transistor in its Environment", Chapter 8, 181-206.
3. Robinson F. and Williams B.W., 1987, "Emitter Switching High-Power Transistors", EPE Conference, 55-59.

ANNEX I

TRANSFORMER DESIGN

The transformer design parameters for the developed asymmetrical bridge forward converter are :

$V_{MIN} = 500V_{DC}$ $V_{MAX} = 600V_{DC}$

$V_{OUTPUT} = 18V$ $I_{OUTPUT} = 200A$

Duty cycle = 0.4 (MAX) Freq. (f) = 25kHz

For forward converter operation equation [1] provides an approximate practical method of calculating the ferrite cross-sectional area.

$$S = K\sqrt{V_{OUTPUT}.I_{OUTPUT}} = 900mm^2 \quad [1]$$

S = cross-sectional area in mm^2

V_{OUTPUT} = Output secondary voltage

I_{OUTPUT} = Output secondary current

K = 15 (for B50 ferrite material).

Two GER65/33/27 (LCC) E shape B50 ferrites were sandwiched together to form a ferrite core cross-sectional area (S) of $1064mm^2$.

Minimum number of primary turns (N_p) can be calculated using equation [2].

$$N_P > \frac{V_{MAX}.\text{Duty cycle}}{B_{MAX}.S.f} > 36 \quad [2]$$

N_P was made equal to 40.

The number of secondary turns can be calculated using equation [3].

$$N_S = \frac{V_{OUTPUT}.N_P}{V_{MIN}.\text{Duty cycle}} > 3.6 \quad [3]$$

N_S was made equal to 4. Hence the primary to secondary turns ratio was 10 to 1. Consequently peak primary current (20A) was one tenth of 200A secondary current.

The primary RMS current can be calculated using equation [4].

$$I_{RMS} = I_{PEAK}.\sqrt{\text{Duty cycle}} = 20\sqrt{0.4} = 12.5A \quad [4]$$

Using a current density of $5A/mm^2$, the primary was wound using two wires in parallel of 1.25mm diameter.

The secondary wire cross-sectional area was $20mm^2$ calculated in a similar manner as for the primary wire.

MEASURED PARAMETERS

Leakage inductance = 90µH

(secondary short-circuited)

Primary inductance = 17.5mH

Insulation material used between primary and secondary was capable of supporting $1500V_{AC}$ at 50Hz. Three pieces of 0.65mm plastic film were used for this isolation.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2260 / TEA2261
HIGH PERFORMANCE DRIVER CIRCUITS FOR S.M.P.S.

SUMMARY

SUMMARY (continued)

I. INTRODUCTION

The TEA2260/61 is an integrated circuit able to drive a bipolar transistor directly with an output base current up to 1.2A.

So the TEA 2260/61 covers a wide range of application from 80W to more than 200W with all safety requirements respected.

The high performances of the regulation loop provide a very low output power due to an automatic burst mode.

The TEA 2260/61 can be used in a MASTER SLAVE STRUCTURE, in a PRIMARY REGULATION or a SECONDARY REGULATION.

The TEA 2260/61 is very flexible and high performance device with a very large applications field.

The only difference between TEA2260 and TEA2261 concerns security functions (see paragraph II.8)

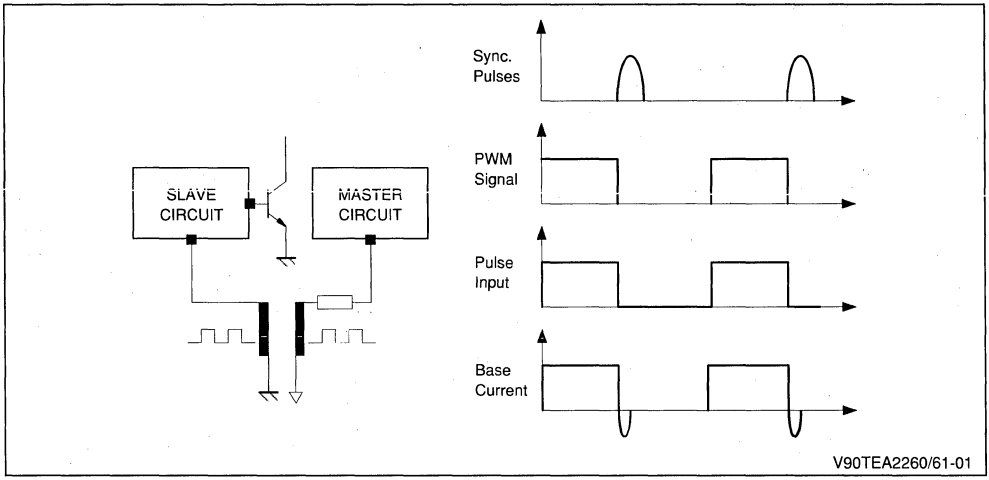
I.1. MASTER SLAVE MODE (fig.1)

In this configuration the master circuit located on the secondary side, generates PWM pulses used for output voltage regulation. These pulses are sent via a feedback transformer to the slave circuit (Fig.1).

In this mode of operation, the falling edge of the PWM Signal may be synchronized with an external signal. By this way the switching off time of the power transistor, which generates lot of parasites, can be synchronized on the line flyback signal in TV applications.

An other advantage of the MASTER SLAVE STRUCTURE is to have a very good regulation not depending of the coupling between transformer primary and secondary windings, which allows the use of low cost switch mode transformers.

Figure 1.



I.2 BURST MODE (fig.2)

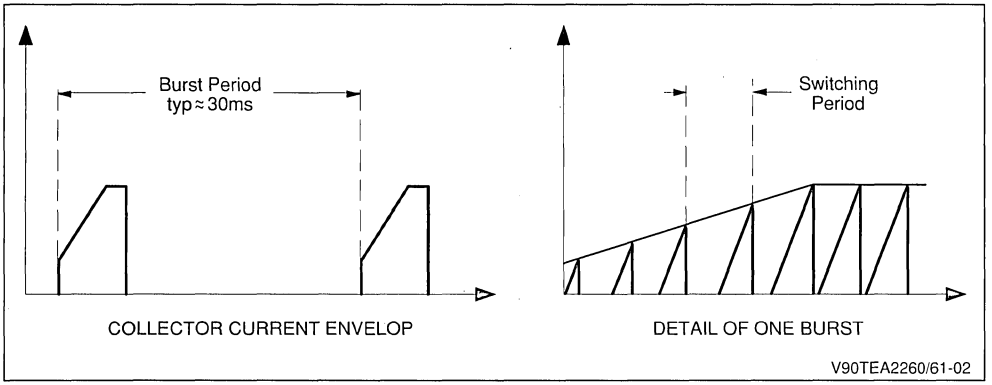
During start-up and stand-by phases, no regulation pulses are provided by the master circuit to the slave circuit.

The slave circuit operates in primary regulation mode. When the output power is very low the burst mode is automatically used.

This operating mode of the SMPS effectively provides a very low output power with a high efficiency. The TEA2260/61 generates bursts with a period varying as a function of the output power.

Thus the output power in burst mode can varied in a wide range from 1W to more than 30W.

Figure 2 : Burst Mode Operation.



I.3. OPERATION OF MASTER SLAVE POWER SUPPLY IN TV APPLICATION

The system architecture generally employed is depicted in Fig.3. On the secondary side a micro controller is connected to the remote control receiver which generates control signal for the stand-by and normal modes of operation (Fig.4).

- In stand-by mode, the device power consumption is very low (few watts). The master circuit does not send pulses and hence the slave circuit works in primary regulation and burst mode.
- In the normal mode, the master circuit provides the PWM signal required for regulation purposes. This is called MASTER SLAVE MODE. The master circuit can be simultaneously synchronized with the line flyback signal.
- Power supply start-up. As soon as the V_{CC}(start) threshold is reached, the slave circuit starts in continuous mode and primary regulation as long as the nominal output voltages are not reached. After this start-up phase the microcontroller holds the TV Set in stand-by mode or either in normal mode.

Figure 3 : TV Application System Diagram.

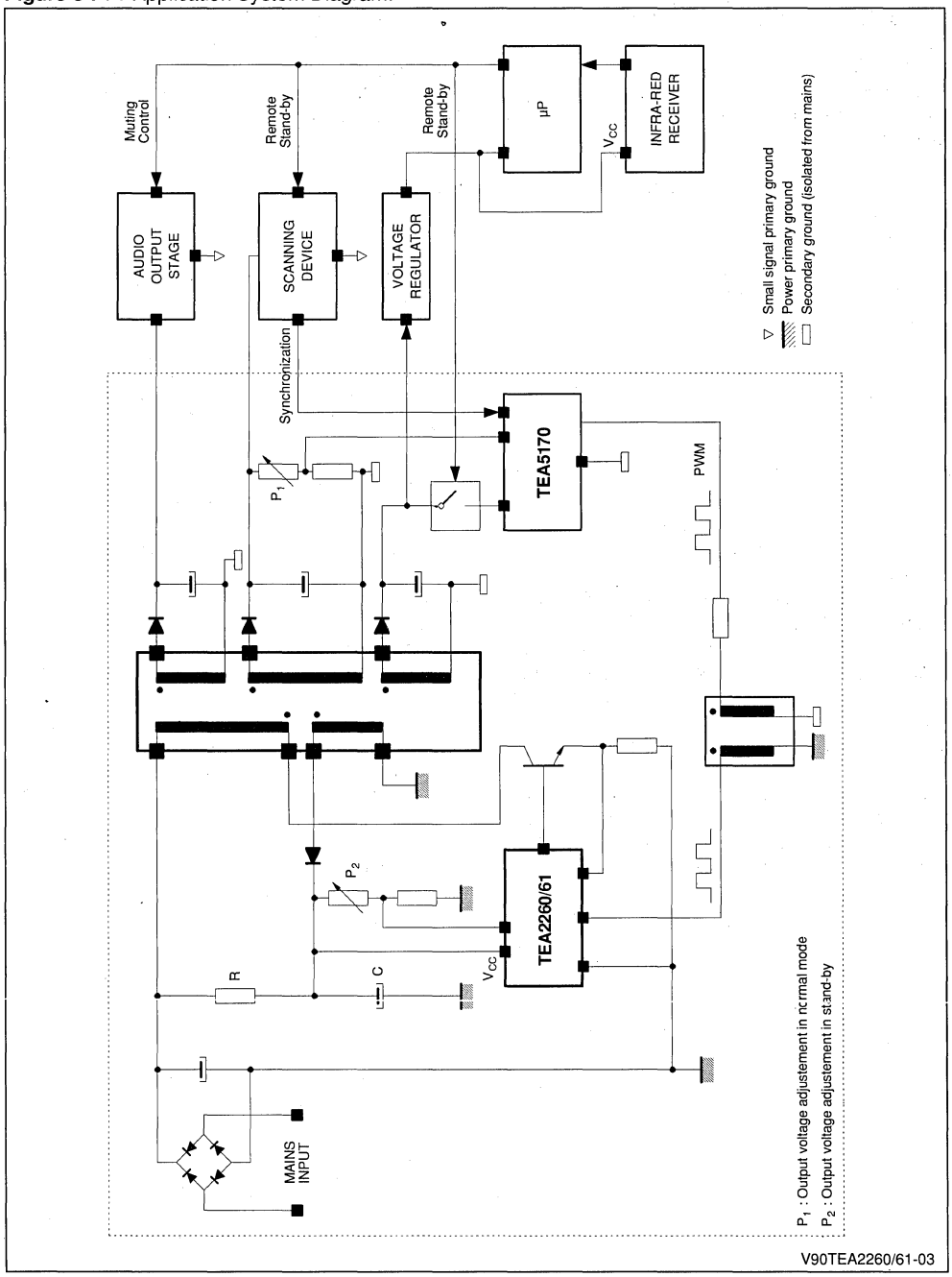
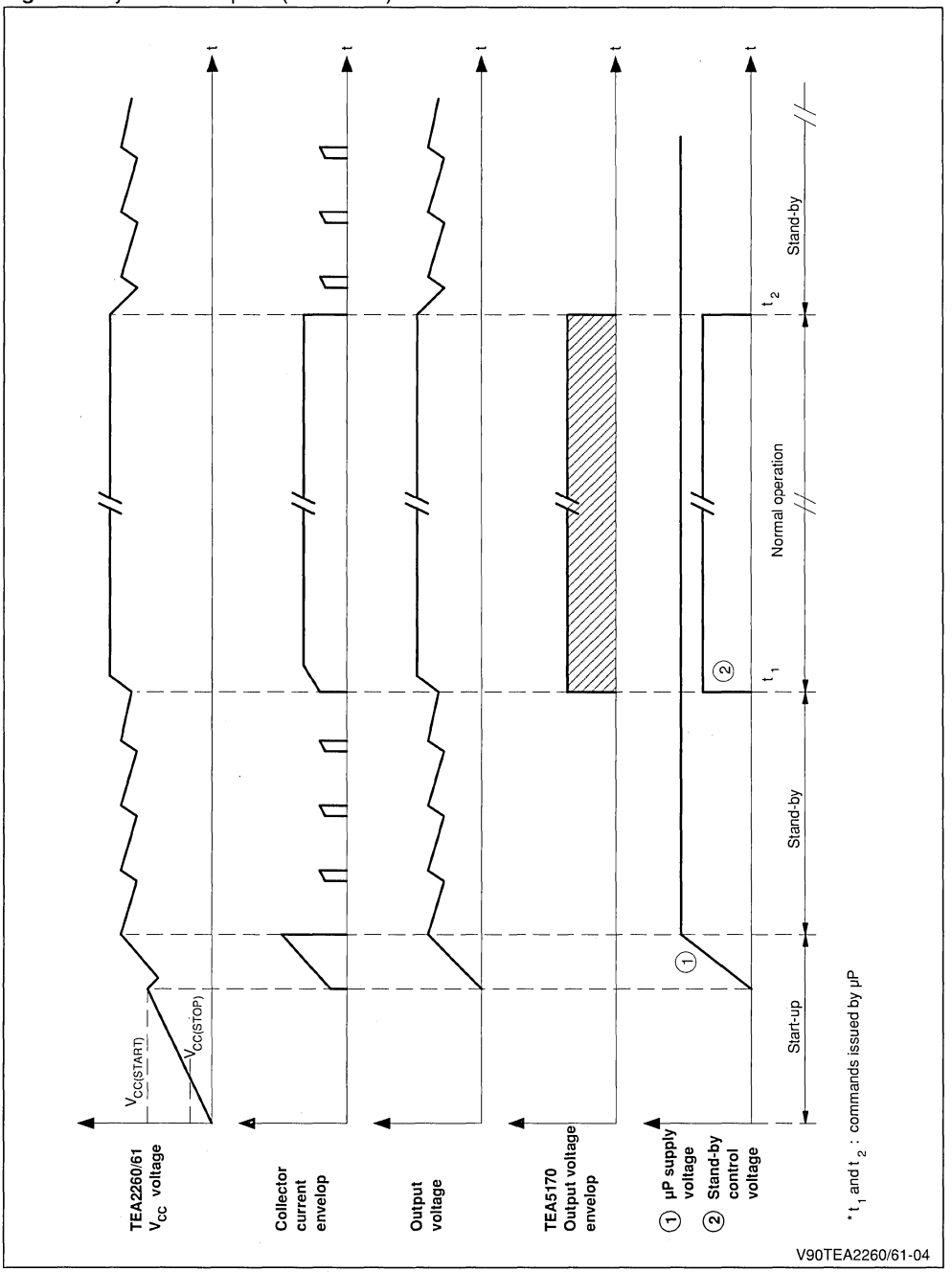


Figure 4 : System Description (waveforms).



I.4. SECONDARY REGULATION (fig.5, 6)

In this configuration the TEA2260/61 provides the regulation through an optocoupler to ensure good accuracy.

The advantage of this configuration is the avaibility of a large range of output power variation (e.g 1W to 110W).

This feature is due to the automatic burst mode (see paragraph II.6).

The structure in a TV Set is simpler than the MASTER SLAVE STRUCTURE because the power supply switches from normal mode to burst mode automatically as a function of the output power.

Figure 5 : TV Application System Diagram.

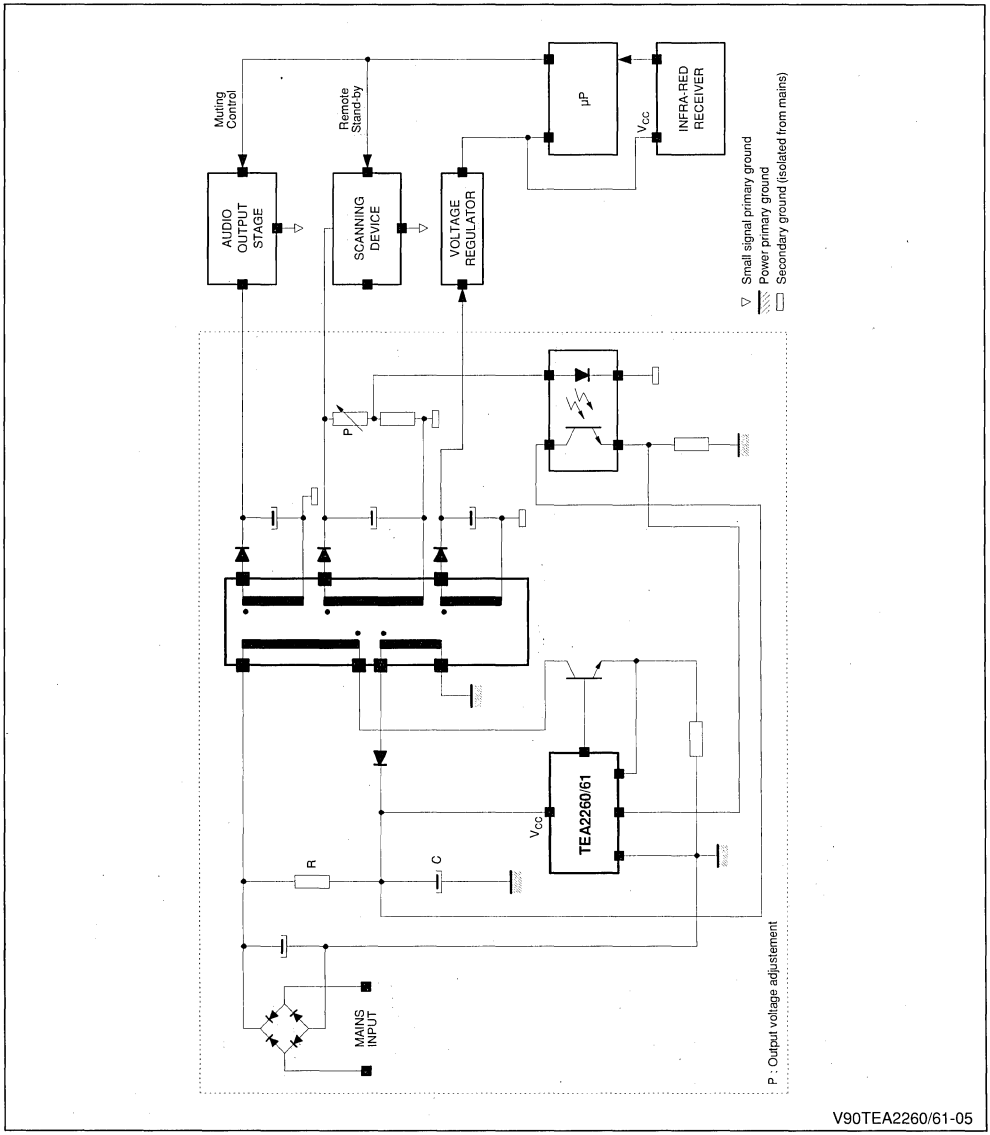
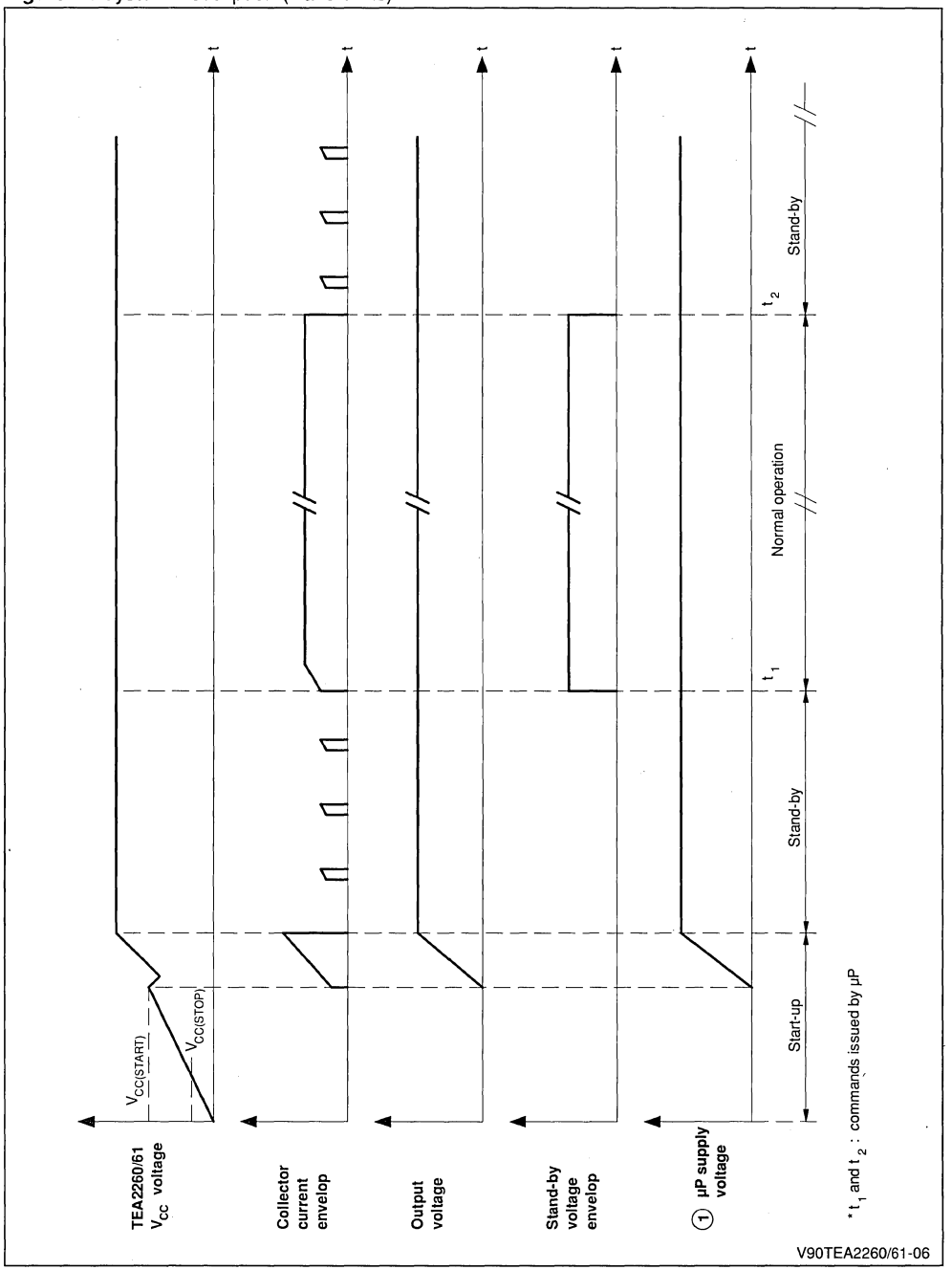


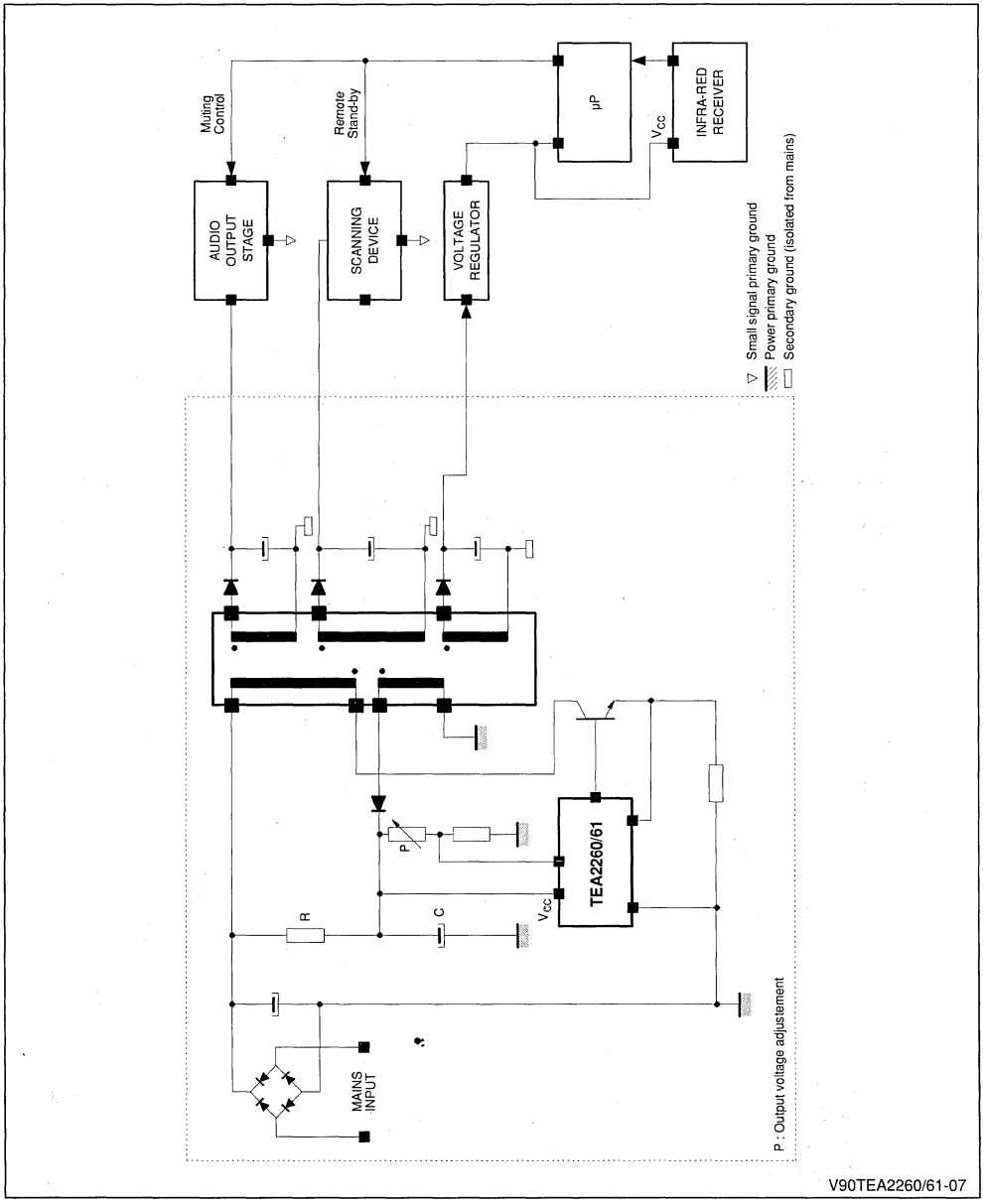
Figure 6 : System Description (waveforms).



I.5. PRIMARY REGULATION (fig.7)

In this configuration the TEA2260/61 provides the regulation through an auxilliary winding.
This structure is very simple but the accuracy depends on the coupling between the transformer primary and secondary winding.
Due to the automatic burst mode the output power can vary in a large range.

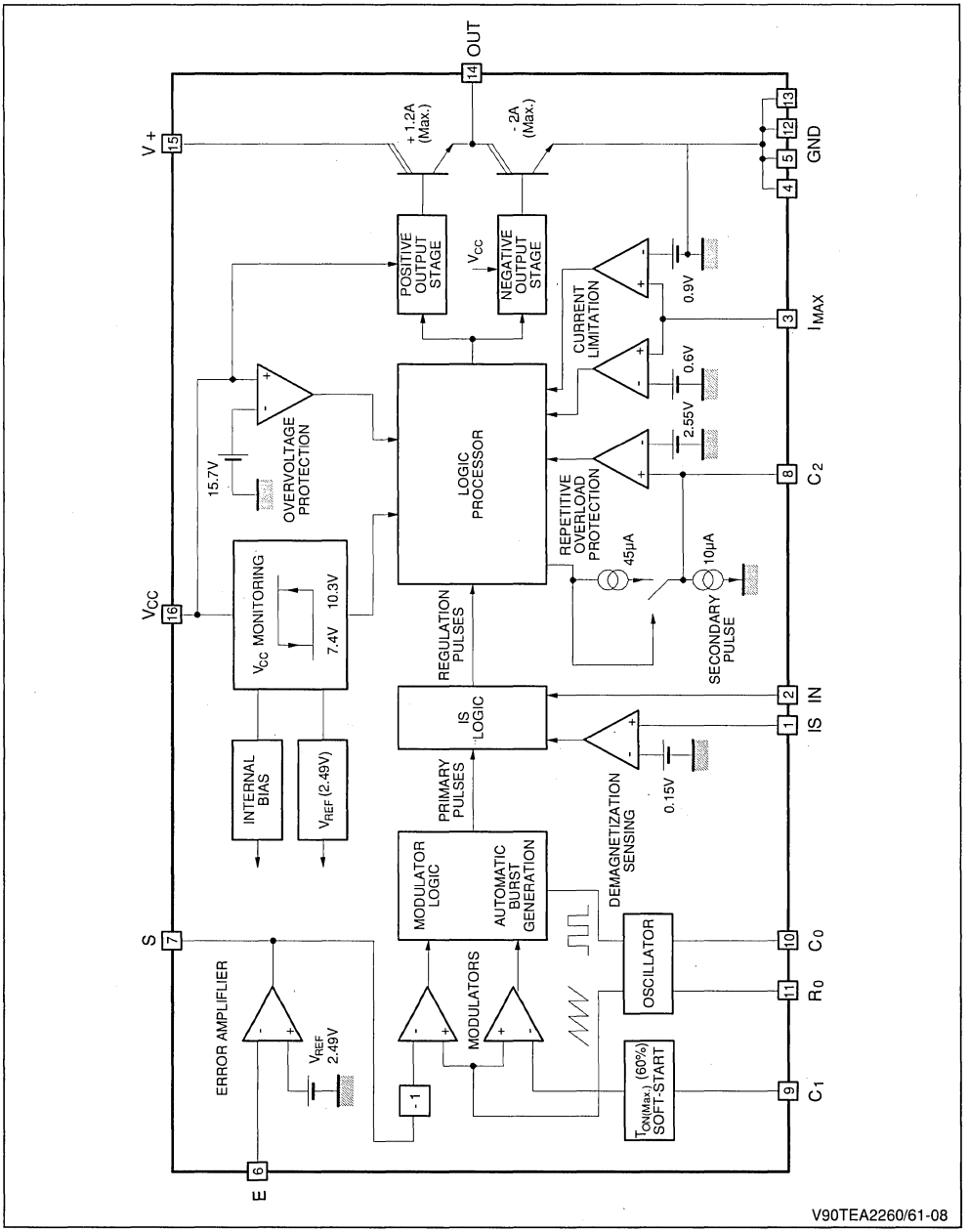
Figure 7 : TV Application System Diagram.



II. CIRCUIT DESCRIPTION

Figure 8 shows the integrated functions.

Figure 8.



The circuit contains 8 blocks :

- Voltage reference and internal V_{CC} generation.
- RC oscillator
- Error amplifier
- Pulse width modulator (PWM)
- "Is logic" for transformer demagnetization checking.
- Current limitation sub-unit (IMAX)
- Logical block.
- Output stage.

II.1. VOLTAGE REFERENCE AND INTERNAL V_{CC} GENERATION (fig.9)

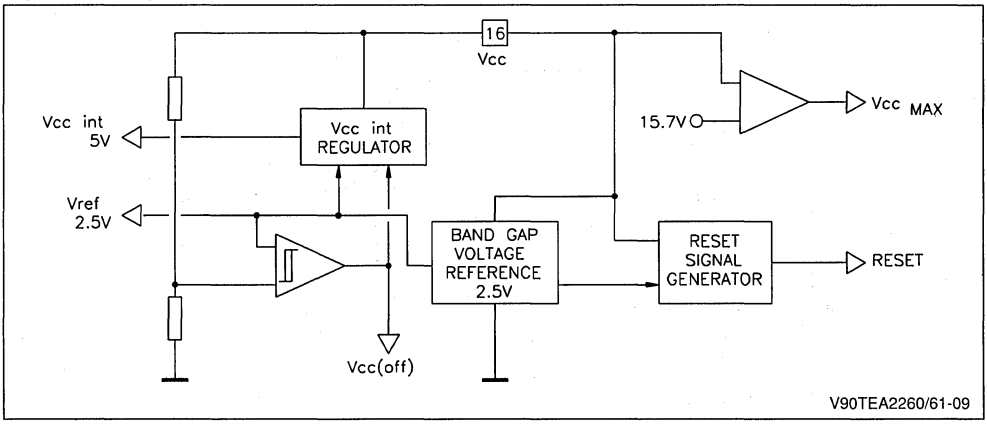
This block generates a 2.5 V typ. voltage reference valid as soon as V_{CC} exceeds 4V. It is not directly accessible externally but is transmitted to other blocks of the circuit.

This block also generates an internal regulated V_{CC}, $V_{CC(int)}$, the nominal value of which is 5V. $V_{CC(int)}$ supplies the circuit when Vcc is higher than $V_{CC(start)}$ (10.3V typ.).

This allows the circuit to achieve a good external V_{CC} rejection, and to provide high performance even with large V_{CC} supply voltage variations.

This block also generates initialization and control signals for the logical block. It also contains the $V_{CC(Max.)}$ comparator (typ threshold 15.7V).

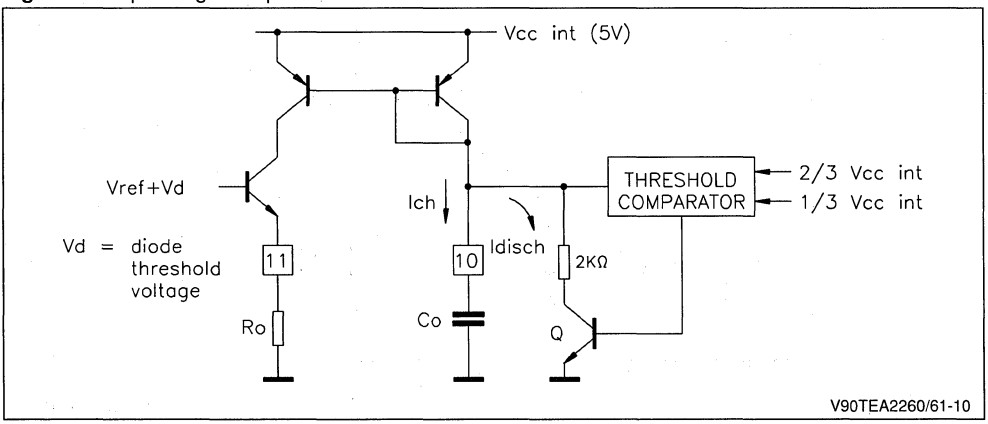
Figure 9 :Voltage Reference Block Principle.



II.2. OSCILLATOR (fig 10,11)

The oscillator determines the switching frequency in primary regulation mode. Two external components are required : a resistor R_O and a capacitor C_O. The oscillator generates a sawtooth signal, which is available on pin 10.

Figure 10 Operating Principle.

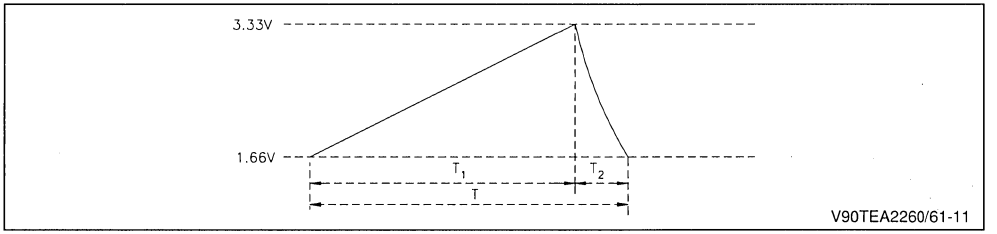


C_O capacitor is charged with a constant current. The current is fixed by R_O which is supplied by voltage Vref.

$$I_{ch} = \frac{2.5}{R_O}$$

When the voltage across C_O reaches $\frac{2}{3}$ x V_{CCint} (typ 3.33V), Q Transistor conducts and C_O is quickly discharged into an 2kΩ (typ) internal resistor. When the voltage reaches 1/3 x V_{CC-int} (typ 1.66V), the discharge is stopped, and the linear charge starts again.

Figure 11 : Sawtooth available accross C_O.



Theoretical values of T, T_1 and T_2 as function of R_O and C_O :

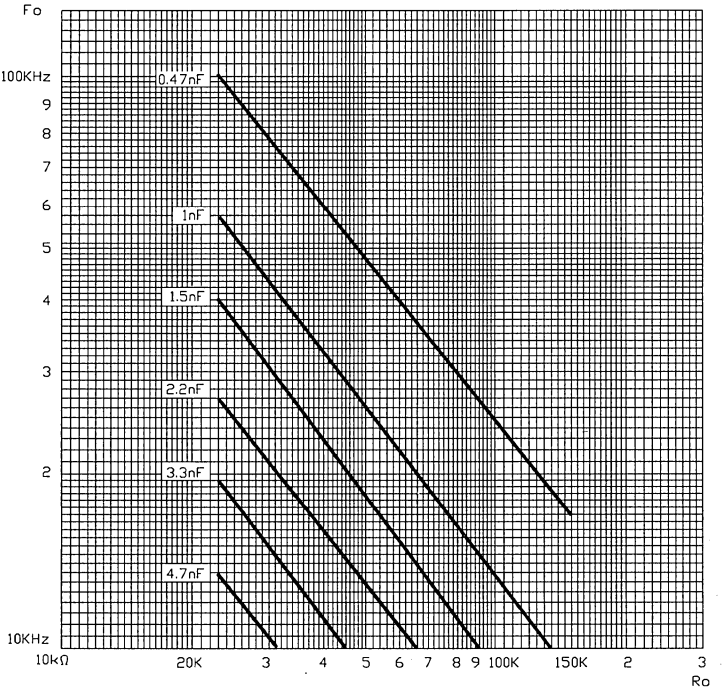
$T = C_O (0.69 \times R_O + 1380)$

$T_1 = R_O \times C_O \times 0.69$

$T_2 = C_O \times 2000 \times 0.69 = C_O \times 1380$

Due to the time response of comparators and normal spread on thresholds values, the real values of T_1 and T_2 may be slightly different, compared with these theoretical values. (see following curves).

Figure 12 : Frequency as a Function of R_O and C_O.



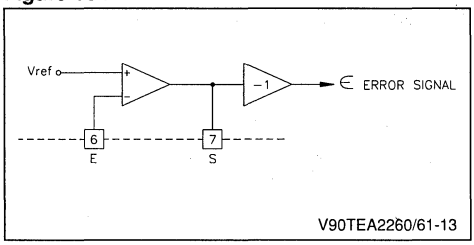
II.3. ERROR AMPLIFIER (fig.13)

It is made of an operational amplifier. The open loop gain is typically 75dB. The unity gain frequency is 550kHz (typ). An internal protection limits the output current (pin 7) at 2mA in case of shorted to ground.

Output and inverting input are accessible thus giving high flexibility in use. The non-inverting input is not accessible and is internally connected to V_{REF} (or 0.9 V_{REF} in burst mode - see paragraph II.6)

Before driving the pulse width modulator (PWM) and in order to get the appropriate phase, the error amplifier is followed by an inverter.

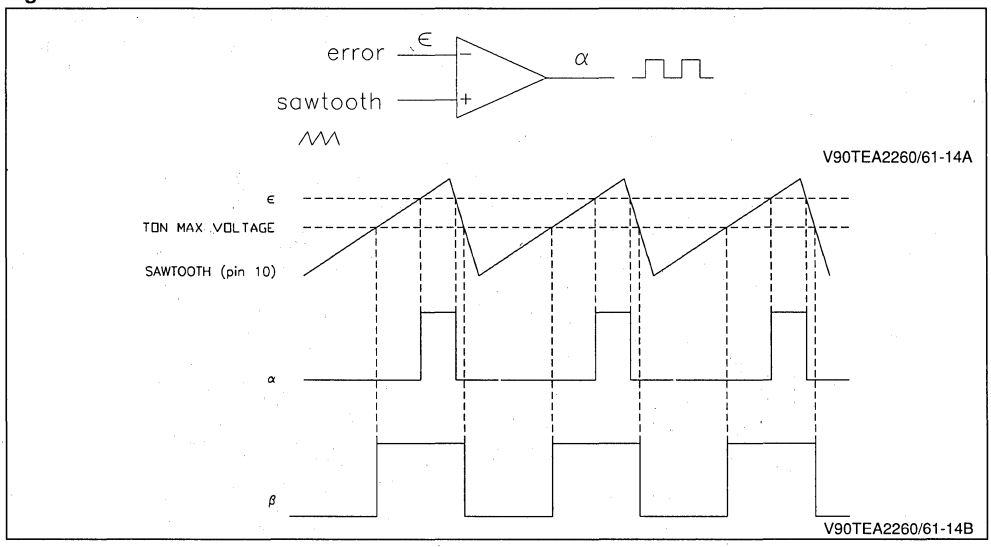
Figure 13 .



II.4. PULSE WIDTH MODULATOR(PWM)(fig.14)

The pulse width modulator consists of a comparator fed by the output signal of the error amplifier and the oscillator output. Its output is used to generate conduction signal.

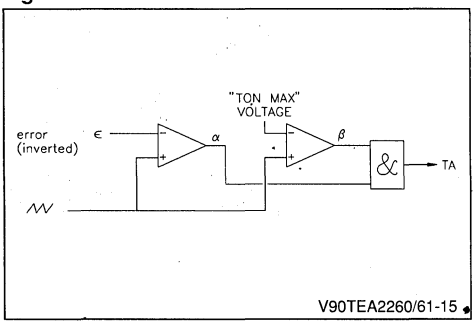
Figure 14 .



The TEA2260/61 actually integrates two PWM :

- A main PWM generates a regulation signal (∝) by comparing the error signal (inverted) and the sawtooth.
- An auxiliary PWM generates a maximum duty cycle conduction signal (β), by comparing the sawtooth with an internal fixed voltage. Furthermore, during the starting phase of the SMPS, in association with an external capacitor, this PWM generates increasing duty cycle, thus allowing a "soft" start-up.
- A logic "AND" between signals (∝) and (β) provides the primary regulator output signal T_A.

Figure 15.

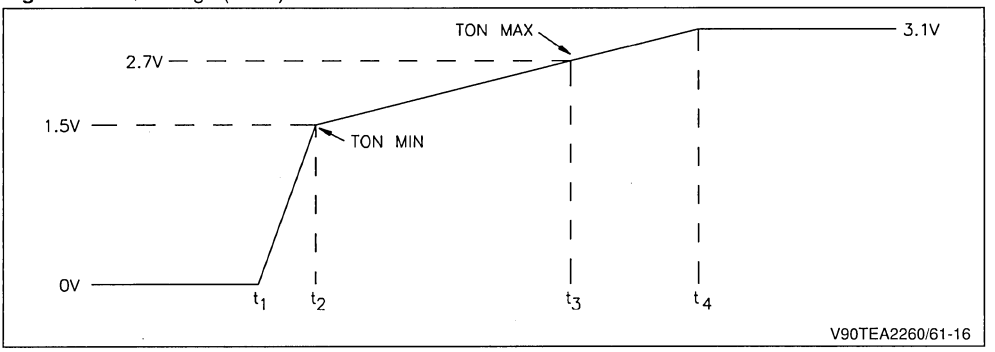


II.5. SOFT START OPERATION (fig.16)

From t_1 to t_2, there is no output pulse (pin 14) and C_1 is charged by a 180µA current (typically). When C_1 voltage reaches 1.5V (typically), output pulses appear and the charge current of C_1 is divided by 20 (9µA typically), then the duty cycle increases progressively. When C_1 voltage reaches 2.7V (typically), the soft-starting device ceases to limit the duty cycle, which may reach 60%

Under established conditions C_1 voltage is charged to 3.1V (typically)

Figure 16 : C_1 Voltage (Pin 9).



II.6. BURST GENERATION IN STAND BY (primary regulation mode)

When the SMPS output power becomes very low, the duty cycle of the switching transistor conduction becomes also very low. In order to transmit a low average power, while ensuring correct switching conditions to the power transistor, a "burst" system is used for energy transmission in stand by mode.

Principle :

For a medium output power (e.g. more than 10W), the voltage reference is applied to the non- inverting input of the error amplifier. When output power decreases as the minimum conducting time of the power transistor is reached, the output voltage tends to increase. Consequently the error signal applied to the PWM becomes higher than the sawtooth. This is detected by a special logic and the voltage applied to the non inverting input becomes Vref = 0.9 x 2.5 = 2.25V typically.

Consequently the regulation loop is in an overvoltage equivalent state and the output pulses disappear. The output voltage decreases and when it reaches a value near 0.9 times the normal regulation value , the voltage applied to the non inverting input is switched again to the normal value V_{REF} = 2.5V. Pulses applied to the power transistor reappear, the output voltage increases again, and so on... A relaxation operation is obtained, generating the burst.

Futhermore, to avoid a current peak at the beginning of each burst, the soft-start is used at this instant.

Advantages of this method :

- improved power supply efficiency compared with traditional systems, for low power transmission.
- automatic burst-mode continuous mode transition, as a function of the output power.
- high stand-by power range.
- burst frequency and duty cycle adjustable with external components to the circuit.

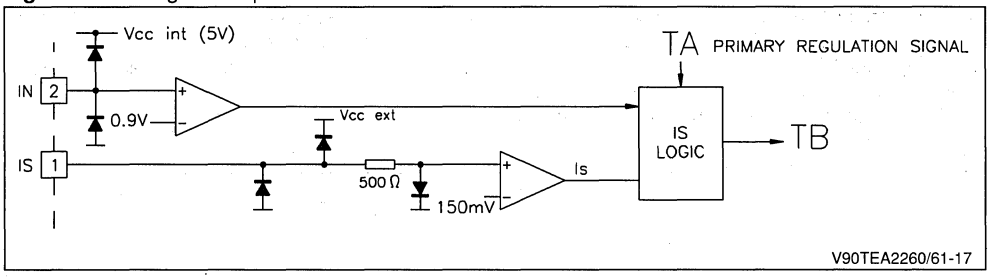
II.7. IS LOGIC (fig.17)

During the transition from the "stand-by" mode to the "normal operating" mode, conduction pulses generated by the secondary regulator occur concurrently with those from the primary regulator.

These pulses are non-synchronous and this may be dangerous for the switching transistor. For example if the transistor is switched-on again during the overvoltage phase, just after switching-off, the FBSOA may not be respected and the transistor damaged.

To solve this problem a special arrangement checking the magnetization state of the power transformer is used.

Figure 17 : IS Logic Principle Schematic.

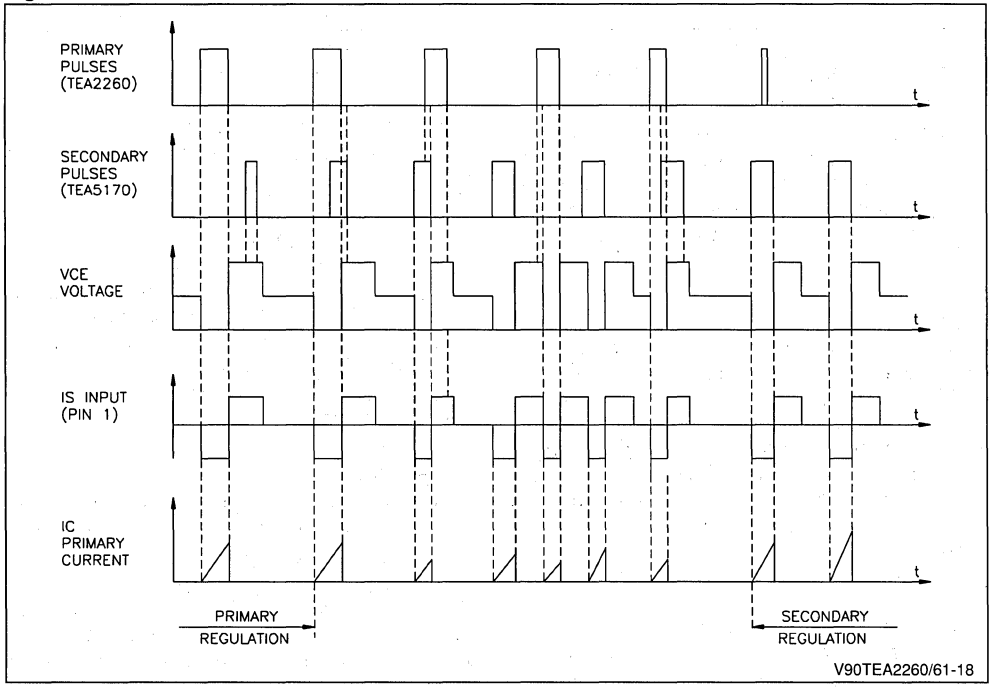


The aim of the IS Logic is therefore to monitor the primary regulation pulses (TA) and the secondary regulation pulses (pin 2), and to deliver a signal TB compatible with the power transistor safety requirements.

The IS Logic block comprises mainly two D flip-flops.

When a conduction signal arrives, the corresponding flip-flop is set in order to inhibit a conduction signal coming from the other regulation loop. Both flip-flops are reset by the negative edge of the signal applied to the demagnetization sensing input (Is Pin 1).

Figure 18.



Note : The demagnetization checking device just described is only active when there are concurrently primary and secondary pulses, which in practice only occurs during the transient phase from Stand-by mode to normal mode.

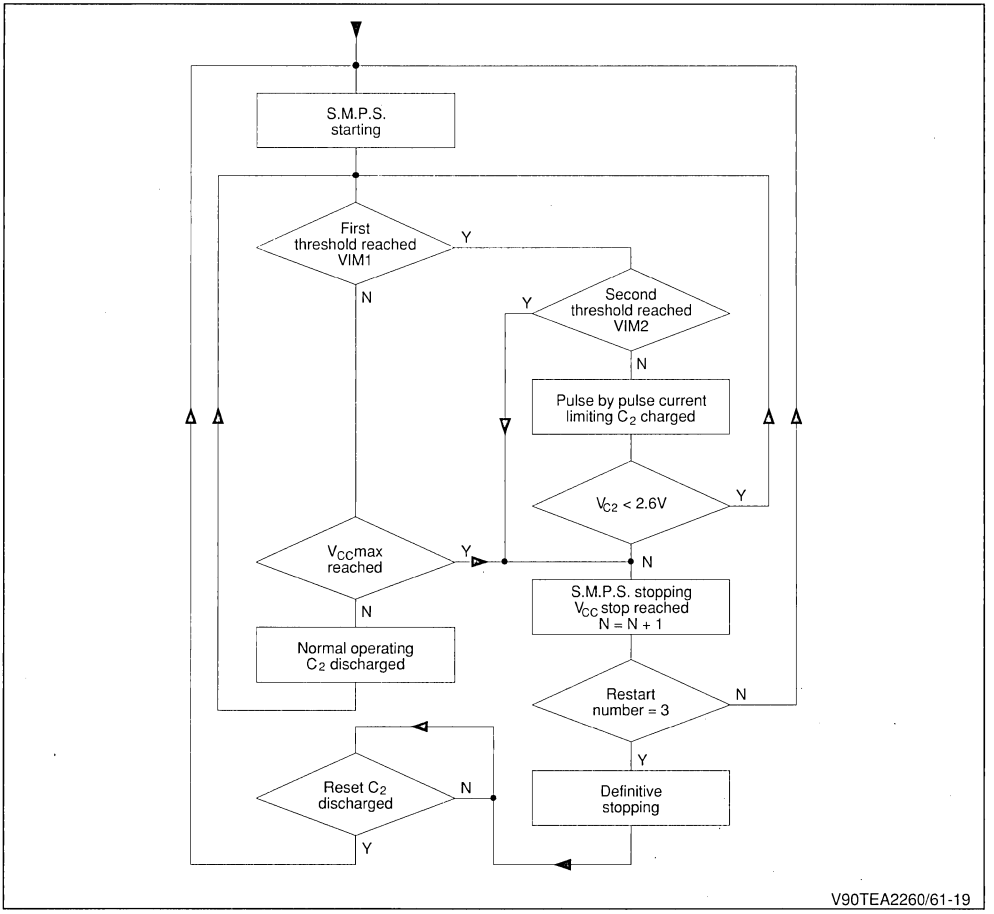
When the power supply is in primary regulation mode **or** in secondary regulation mode, the demagnetization checking function is not activated.

II.8. SAFETY FUNCTIONS : Differences between TEA2260 and TEA2261

TEA2260 :

Concerning the safety functions, V_{CC}(max) (overvoltage detection) VIM1, VIM2 (overcurrent detection) the TEA2260 uses an internal counter which is incremented each time V_{CC}stop is reached (after fault detection) and try to restart. After 3 restarts with fault detection the power supply stops. But in certain cases where the TV set is supplied for a long time, without swich off, the power supply could stop (cases of tube flashes). In this case it is necessary to switch off the TV set and swich on again to reset the internal counter.

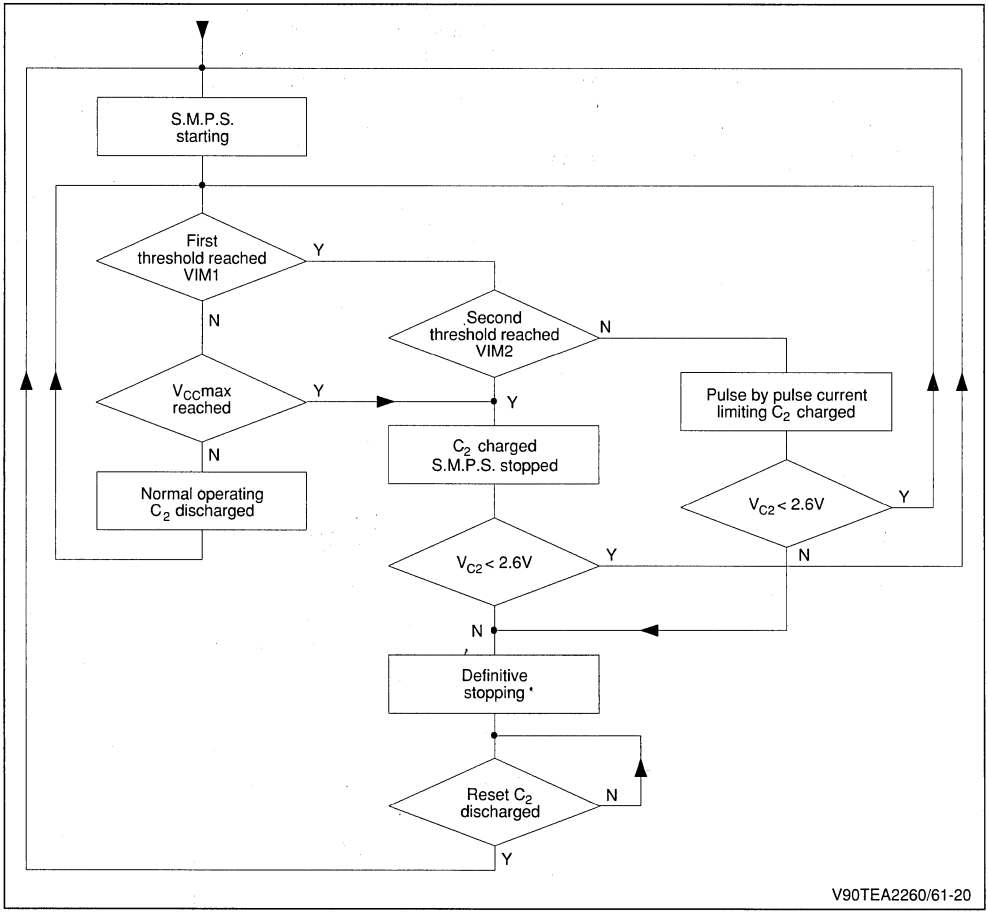
Figure 19 : TEA2260 Safety Functions Flowchart.



TEA2261:

The safety detections are similar to TEA2260 for V_{CC}(max) (overvoltage detection) VIM1, VIM2 (overcurrent detection), but each time a fault detection is operating the C_2 capacitor is loaded step by step up to 2.6V, (case of long duration fault detection) and the power supply stpos. To discharge C_2 capacitor it is necessary to switch off the TV set and to switch on again and the power supply starts up.

Figure 20 : TEA2261 Safety Functions Flowchart.

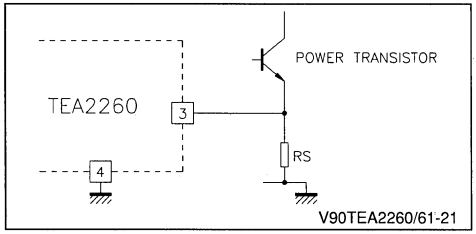


II.8.1. I MAX (power transistor current limitation)

The current is measured by means of a resistor inserted in the emitter of the power transistor. The voltage obtained is applied on pin 3 of the TEA2260/61.

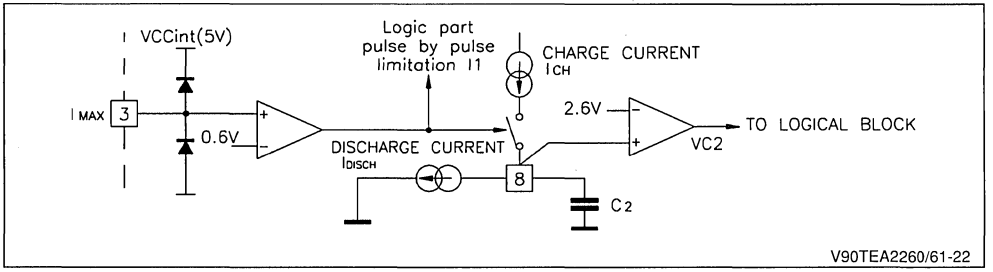
The current limitation device of the TEA2260/61 is a double threshold device. For the first threshold, there is no difference between the two devices, only for the second threshold.

Figure 21.



II.8.1.1. First threshold : VIM1 (typical value)

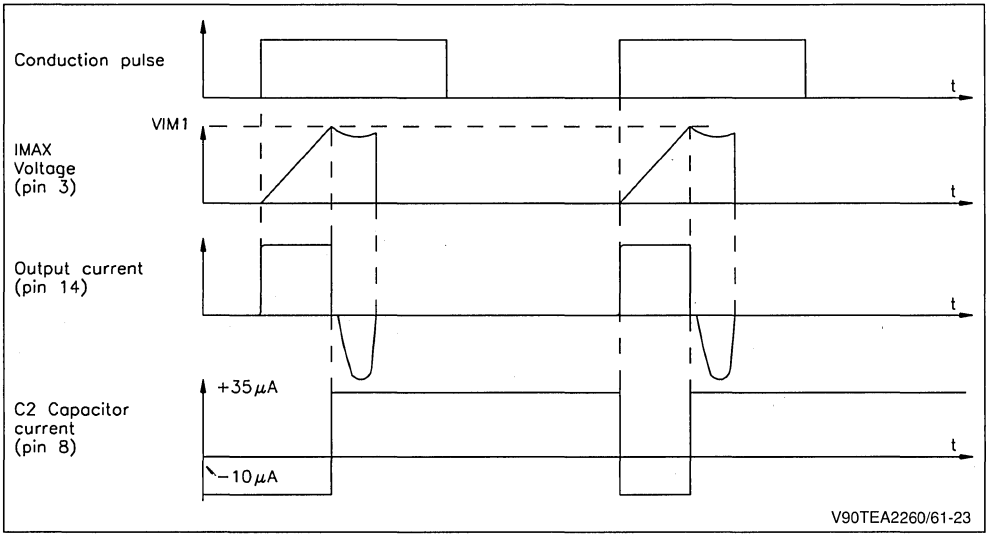
Figure 22 : Current Limitation Schematic Principle. First Threshold Part.



Two actions are carried out when the first threshold is reached

- The power transistor is switched-off (pulse by pulse limitation). A new conduction pulse is necessary to switch-on again.
- The C_2 capacitor, which is continuously discharged by Idisch current (10µA typically), is charged by the current Ich - I disch (45µA - 10µA = 35µA typically), until the next conduction pulse.

Figure 23 : Example of First Current Limitation Threshold Triggering.



The capacitor C_2 is charged as long as an output overload is triggering the first current limitation threshold. When the voltage across C_2 reaches the threshold V_{C2} (typically 2.55V), output pulses (pin 14) are inhibited and the SMPS is stopped. A restart may be obtained by decreasing Vcc under the $V_{CC(stop)}$ threshold to reset the IC.

If the output overload disappears before the voltage across C_2 reaches V_{C2}, the capacitor is discharged and the power supply is not turned off. Due to this feature, a transient output overload is tolerated, depending on the value of C_2 (see III.2.5).

II.8.1.2. Second current limitation threshold (VIM2) for TEA2260

In case of hard overload or short circuit, despite the pulse by pulse current limitation operation, the current in the power transistor continues to increase. If the second threshold VIM2 is reached, the power supply is immediately turned off and the internal counter is incremented. After 3 restarts, the power supply is definitively stopped.Restart is obtained by decreasing V_{CC} below $V_{CC(stop)}$, as in the case of stopping due to the repetitive overload protection triggering.

II.8.1.3. Second current limitation threshold (VIM2) for TEA2261

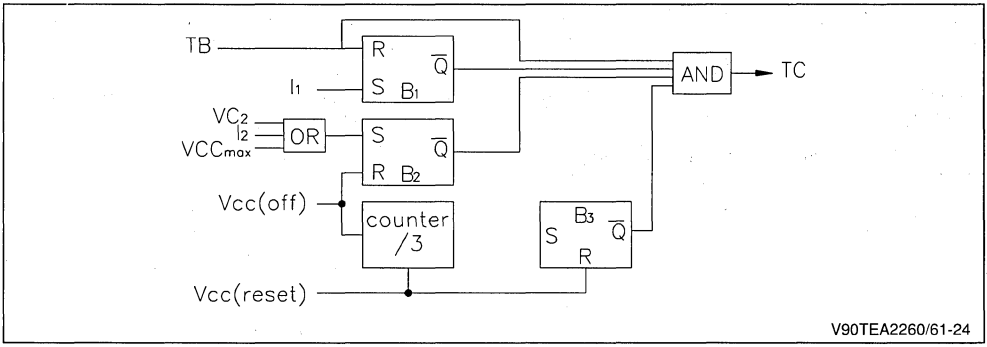
For this device, if the second threshold is reached, the power supply is turned off, C_2 is charged and a new start-up is authorized only if $V_{C2} < 2.6V$.

II.8.2. LOGICAL BLOCK :

This block receives the safety signals coming from different blocks and inhibits the conduction signals when necessary.

II.8.2.1. Logical block for TEA2260

Figure 24 : TEA2260 Simplified Logical Block Diagram.



TB is the conduction signal (primary or secondary)coming from the Is logical block.

TC is the conduction signal transmitted to the output stage.

I_1 is the output signal of the first current limitation threshold comparator. It is memorized by the flip-flop B_1.

I_2 is the output signal of the second current limitation threshold comparator

V_{C2} is the output signal of the comparator checking the voltage across C_2.

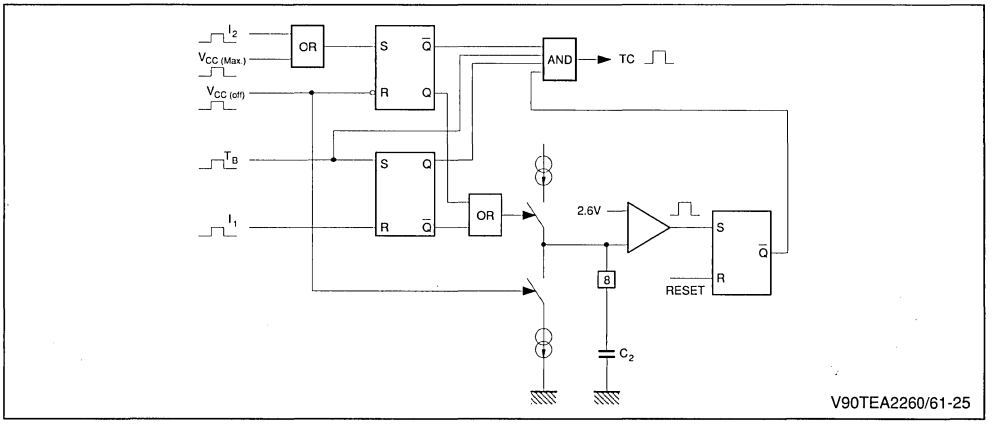
$V_{CC(Max.)}$ is the signal coming from V_{CC} checking comparator.

These three signals V_{C2}, I_2, $V_{CC(Max.)}$ are memorized by B_2.
In case of B_2 flip-flop setting (I_2 or V_{C2} or $V_{CC(Max.)}$ defect) the current consumption on V_{CC} increases. This function allows to decrease the V_{CC} voltage until $V_{CC(stop)}$. After this the current consumption on Vcc decreases to $I_{CC(start)}$ and a new start up is enabled.

The $V_{CC(Off)}$ signal comes from the comparator checking V_{CC}. A counter counts the number of $V_{CC(off)}$ establishment. After four attempted starts of the power supply the output of the circuit is inhibited. To reset the circuit it is necessary to decrease V_{CC} below 5.5V typically. In practice this means that the power supply has to be disconnected from the mains.

II.8.2.2.Logical block for TEA2261

Figure 25.

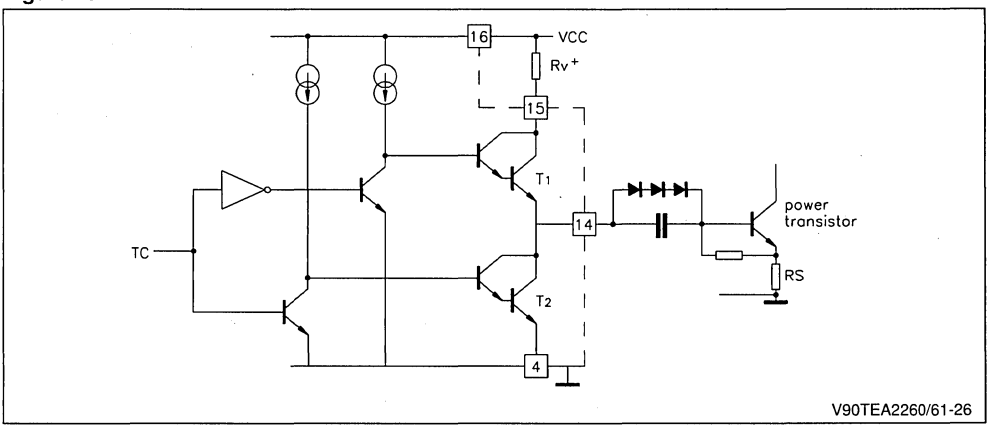


V_{CC}(off) is a signal coming from a comparator checking V_{CC}. When V_{CC} > V_{CC}(stop),V_{CE}(off) is high.
V_{CC}(max) is a signal coming from a comparator checking V_{CC}. When V_{CC} > V_{CC}(max),V_{CC}(max) is high.
I_1 is a signal coming from the first current limitation threshold comparator.
When I_{max} x R_{SHUNT} > VIM1, I_1 is high.
I_2 is a signal coming from the second current limitation threshold comparator.
When I_{max} x R_{SHUNT} > VIM2,I_2 is high.
TB is the conduction signal coming from the error ampliflier system.
TC is the output signal transmitted to the output stage.

II.9. OUTPUT STAGE

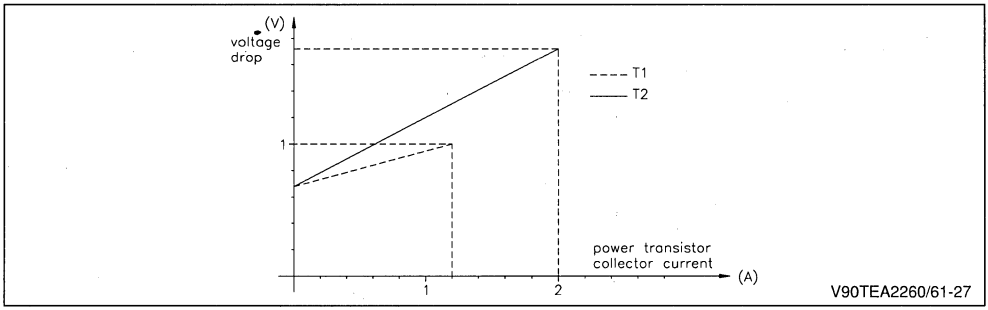
The output stage is made of a push-pull configuration : the upper transistor is used for power transistor conduction and the lower transistor for power transistor switch-off.

Figure 26.



A capacitive coupling is recommanded in order to provide a sufficient negative base current through the power transistor .

Figure 27 : Typical Voltage Drops of Output Transistor versus Current.



Important remark : Due to the internal output stage structure, the output voltage (Pin 14) must never exceed 5V. This condition is respected when a bipolar transistor is driven.
Note that Power-MOS transistor drive is not possible with the TEA2260/61.

III. TV APPLICATION 120W - 220 VAC - 16 kHZ SYNCHRONIZED ON HORIZONTAL DEFLECTION FREQUENCY

General structure and operational features of this power supply were outlined in section I.
The details covered below apply to a power supply application using the master circuit TEA5170.
(refer to TEA5170 data sheet and TEA5170 application note "AN088" for further details).

III.1. CHARACTERISTICS OF APPLICATION

- Discontinuous mode Flyback SMPS
- Standby function using the burst mode of TEA2260/61
- Switching Frequency
  - Normal mode : 15.625 kHz (synchronized on
  - horizontal deflection frequency)
  - Standby mode : about 16 kHz
- Nominal mains voltage : 220 VAC
- Mains voltage range : 170 VAC to 270 VAC
- Nominal output power : 120W
- Output power range in normal mode $14W < P_O < 120W$
- Output power range in standby mode $1W < P_O < 25W$
- Efficiency
  - Normal mode : 85% (under nominal conditions)
  - Stand by mode : 45%
- Regulation performance on high voltage output : 140 VDC
  - ± 0.3% versus mains variations of 170 VAC to 270 VAC (P_{OUT} : 120W)
  - ± 0.5% versus load variations of 14W to 120W (V_{in} = 220 VAC)
- Overload protection and complete shut down after a predetermined time interval.
- Short circuit protection.
- Open load protection by output overvoltage detection
- Complete power supply shut-down after 3 restarts resulting in the detection of a fault condition for TEA2260.
- Complete power supply shut-down when V_{C2} reaches 2.6V for TEA2261.

III.2. CALCULATION OF EXTERNAL COMPONENTS

Also refer to TEA5170 application note "AN408/0591" for calculation methods applicable to other power supply components.

The external components to TEA2260/61 determine the following parameters :

- Operating Frequency in primary regulation
- Minimum conduction time in primary regulation
- Soft start duration
- overload duration
- Error amplifier gain and stand-by output voltage
- Base drive of the switching transistor
- Primary current limitation

Ideal values :

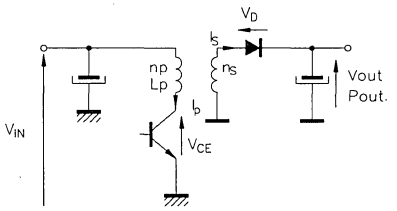
- Free running Frequency in stand-by mode : 16kHz
- $Ton_{(min)}$ duration : 1µs
- Soft start duration : 30ms
- Maximum overload duration : 40ms
- Error amplifier Gain : 15
- Maximum primary current depends on the transformer specifications

III.2.1. Transformer calculation

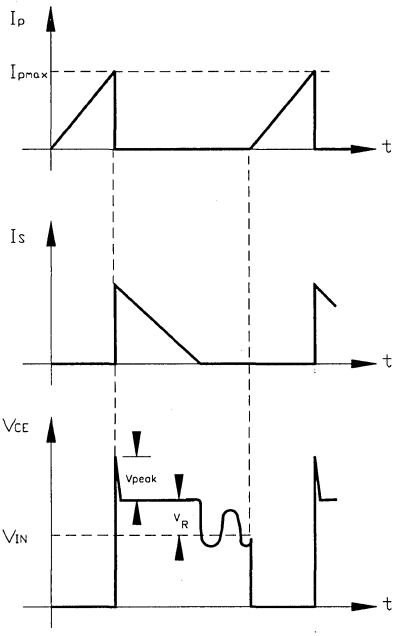
The following important features must be considered to calculate the specifications of the transformer :

- Maximum output power : 120W
- Minimum input voltage :
- 220 VAC - 20% → Vin(min) = 210 VDC with 40V ripple on the high voltage filtering capacitor
- Switching Frequency : 15.625kHz
- Maximum duty cycle : 0.45
- Output voltages :
  + 140V - 0.6A
  + 14V - 0.5A
  + 25V - 1A
  + 7.5V - 0.6A
  + 13V - 0.3A

Figure 28.



V90TEA2260/61-28A



V90TEA2260/61-28B

Maximum primary current

$$I_{P(max)} = 2 \times \frac{P_{OUT}}{\eta \times V_{IN(min)} \times \frac{T_{ON(max)}}{T}}$$

η : efficiency of the power supply $0.80 < \eta < 0.85$

Primary inductance of the transformer

$$L_P = \frac{V_{IN(min)}}{I_{P(max)}} \times T_{ON(max)}$$

Transformer ratio

$$\frac{ns}{np} = \frac{(V_{OUT} + V_D) \times T_{DM}}{V_{IN(min)} \times T_{ON(max)}}$$

Reflected voltage

$$V_R = \frac{1}{\frac{T}{T_{ON(max)}} - 1} \times V_{IN(min)}$$

Overvoltage due to the leakage inductance

$$V_{PEAK} = \frac{I_{P(max)}}{2} \times \sqrt{\frac{L_f}{C}}$$

with : Lf = leakage inductance of the transformer
$0.04 \times Lp < Lf < 0.10 \times Lp$
C = capacitor of the snubber network (see III.2.2.2)

Numerical application

To determine the specifications of the transformer, it is necessary to make a compromise between a maximum primary current and a maximum voltage on the transistor :

- To minimize the maximum primary current

with $0.4 < \frac{T_{ON(max)}}{T} < 0.5$

- To minimize the maximum voltage on the transistor during the demagnetization phase.

$0.3 < \frac{T_{ON(max)}}{T} < 0.4$

When the output power of the power supply is greater than 100W it is better to minimize the maximum primary current because the current gain $B_f = I_C / I_B$ of bipolar transistor is $1.5 < B_f < 6$

Choice : $\frac{T_{ON(max)}}{T} < 0.45$

$$I_{P(MAX)} = \frac{2 \times P_{OUT}}{\eta \times V_{IN(MIN)} \times \frac{T_{ON(MAX)}}{T}} = \frac{2 \times 120}{0.85 \times 210 \times 0.45} = 3A$$

$$L_P = \frac{V_{IN(MIN)}}{I_{P(MAX)}} \times T_{ON(MAX)} = \frac{210}{3} \times 0.45 \times 64\ 10^{-6} = 1.95mH$$

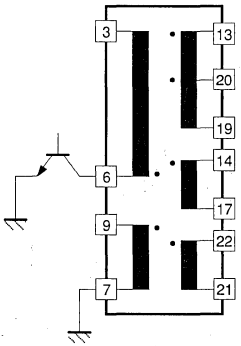
$$V_R = \frac{1}{\frac{T}{T_{ON(MAX)}} - 1} \times V_{IN(MIN)} = \frac{1}{\frac{1}{0.45} - 1} \times 210 = 172V$$

V_{PEAK} will be calculated with the snubber network determination (see II.2.2.2.1)

III.2.1.1 Transformer specification

- Reference : OREGA - SMT5 - G4467-03
- Mechanical Data :
  - Ferrite : B50
  - 2 cores : 53 x 18 x 18 (mm) THOMSON-LCC
  - Airgap : 1.7 mm
- Electrical Data :

Figure 29.



Winding	Pin	Inductance
n_P	3-6	1.95µH
n_{AUX}	7-9	8.1µH
n2	19-13	770µH
n3	19-20	8.2µH
n4	14-17	4.2µH
n5	22-21	31.7µH

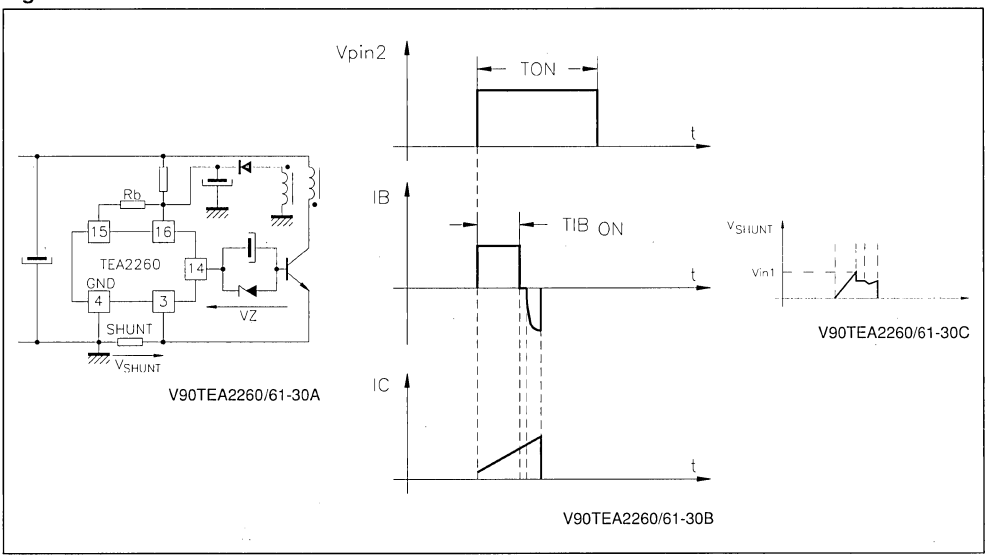
V90TEA2260/61-29

III.2.2. Switching transistor and its base drive

III.2.2.1. First current limitation

Note : in current limitation TIBon < T_{ON}

Figure 30 : Current Limitation.



The current measurement is $I_E = I_B + I_C$
The maximum collector current calculated in III.2.1 is $I_{C(Max.)}$ = 3A (a switching transistor SGSF344 may be chosen)

The current gain is: $B_f = \frac{I_C}{I_{B+}} = 3.5$

The current limitation is :

$$I_{E(max)} = I_{P(max)} - (T_S \times \frac{V_{IN(min)}}{L_P}) + I_{B+}$$

with : T_S = storage time of the switching transistor (typ 3µs) and VIM1 = first threshold of current measurement (typ 0.6 v)

$$R_{SHUNT} = \frac{V_{IM1}}{I_{E(max)}}$$

Numerical application

$$I_{E(max)} = I_{P(max)} - (T_S \times \frac{V_{IN(min)}}{L_P}) + I_{B+}$$

$$I_{E(max)} = 3 - (3\ \ 10^{-6} \times \frac{210}{1.95\ \ 10^{-3}}) + 0.85 = 3.52A$$

$$R_{SHUNT} = \frac{V_{IM1}}{I_{E(max)}} = \frac{0.6}{3.52} = 0.169\Omega$$

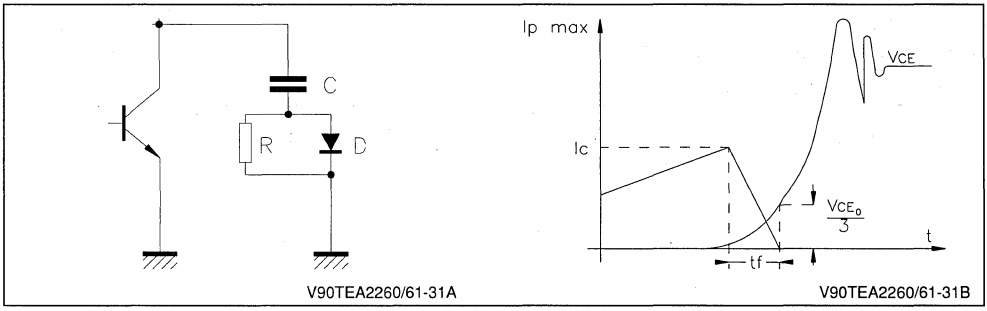
III.2.2.2 Snubber network

A R.D.C network is used to limit the overvoltage on the transistor during the switching off time.
When the transistor is switched off, the capacitor is charged directly through the diode.
When the transistor is switched on, the capacitor is discharged through a resistor.

- $C = \frac{I_{P(max)} \times t_f}{2 \times \frac{VCE_O}{3}}$
- $3 \times R \times C = T_{on(min)}$ (to discharge the the capacitor C by the correct amount)
- Maximum power dissipated in R :

$$P = \frac{1}{2} \times C \times (V_{IN(max)} + V_R)^2 \times F$$

Figure 31.



Numerical application (with SGSF 344 transistor) with :

$I_{P(Max.)} = 3A$ - $V_{IN(Max.)} = 370$ VDC

$t_f = 0.3\mu s$ - $V_R = 172V$

$V_{CEO} = 600V$ - $F = 16kHz$

$T_{ON(Min.)} = 4\mu s$

$$C = \frac{I_{P(max)} \times t_f}{2 \times \frac{VCE_O}{3}} = \frac{3 \times 0.3\ 10^{-6}}{2 \times \frac{600}{3}} = 2.25nF$$

$$R = \frac{T_{ON(min)}}{3 \times C} = \frac{4\ 10^{-6}}{3 \times 2.25\ 10^{-9}} = 560\Omega$$

$$P = \frac{1}{2} \times C \times V_{IN(max)} + V_{R)}{}^2 \times F$$

$$P = \frac{1}{2} \times 2.25 \cdot 10^{9} \times (370 + 172)^2 \times 16 \cdot 10^{3} = 5.29W$$

In the final application a value of 2.7nF is chosen to decrease the overvoltage on the transistor in short circuit condition.

III.2.2.2.1 Overvoltage due to the leakage inductance

(See. III.2.1)

The capacitor C of the snubber network influences the overvoltage due to the leakage inductance.

$$V_{peak} = \frac{I_{C(max)}}{2} \sqrt{\frac{L_f}{C}}$$

Numerical application

with : $L_f = 0.08 \times L_p = 0.08 \times 1.9\ 10^{-3} = 152\mu H$

$$V_{peak} \frac{3}{2} \times \sqrt{\frac{152\ 10^{6}}{2.25\ 10^{9}}} = 390V$$

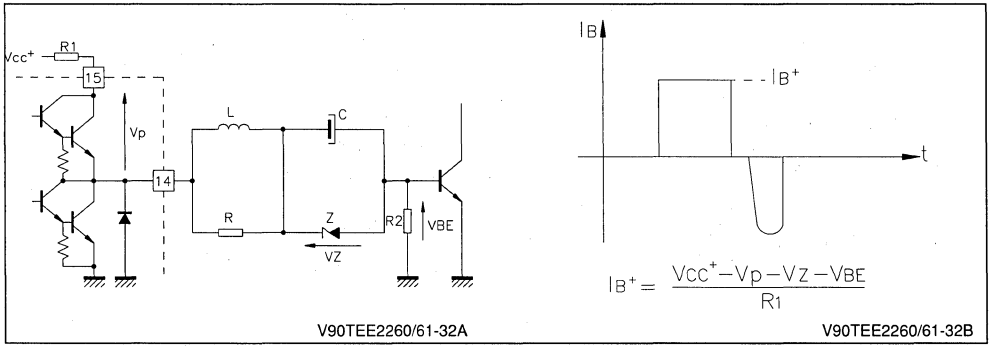
so $V_{CE(Max.)} = V_{IN(Max.)} + V_R + V_{peak} =$

$V_{CE(Max.)} = 370 + 172 + 390 \cong 930V$

III.2.2.3. Base drive

The output stage of the TEA2260/61 works in saturation mode and hence the internal power dissipation is very low.

Figure 32.



$$R_1 = \frac{V_{CC+} - V_P - V_Z - V_{BE}}{I_{B+}}$$

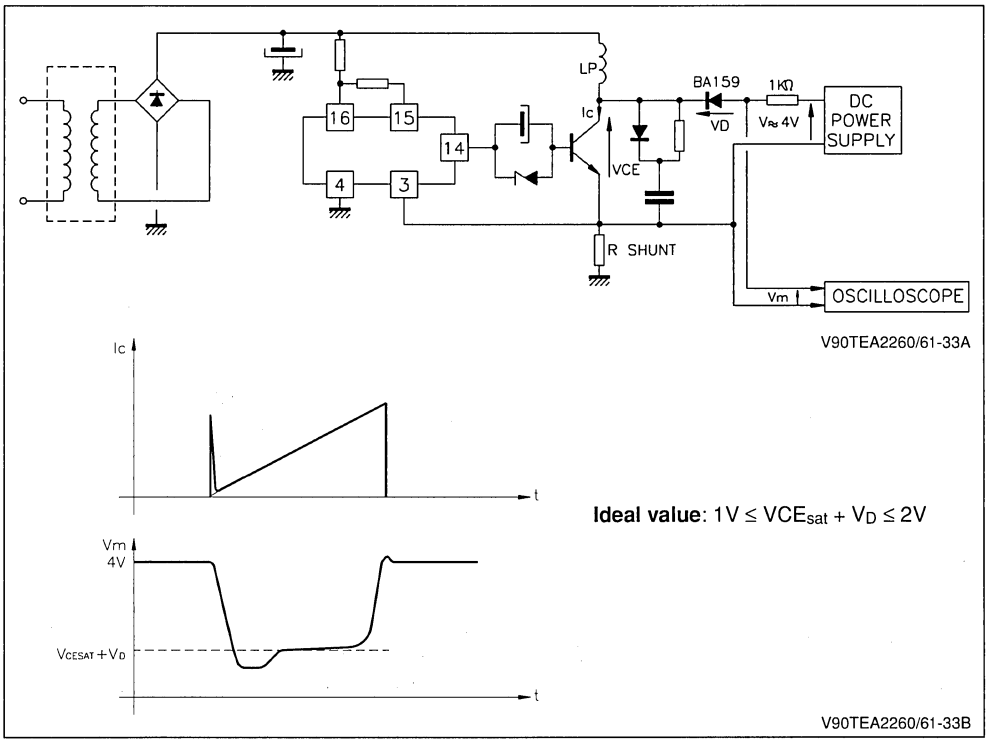
Numerical application

$$R_1 = \frac{13 - 0.9 - 3 - 0.6}{0.85} \cong 10\Omega$$

in this case the current gain,

$B_F = \frac{I_C}{I_B} = \frac{3}{0.85} = 3.5$ but it is recommanded to verify the V_{CE} sat dynamic behaviour on the transistor as follows:

Figure 33.



Remark :The mains of the TEA2260/61 must be provided through an isolation transformer for this measurement

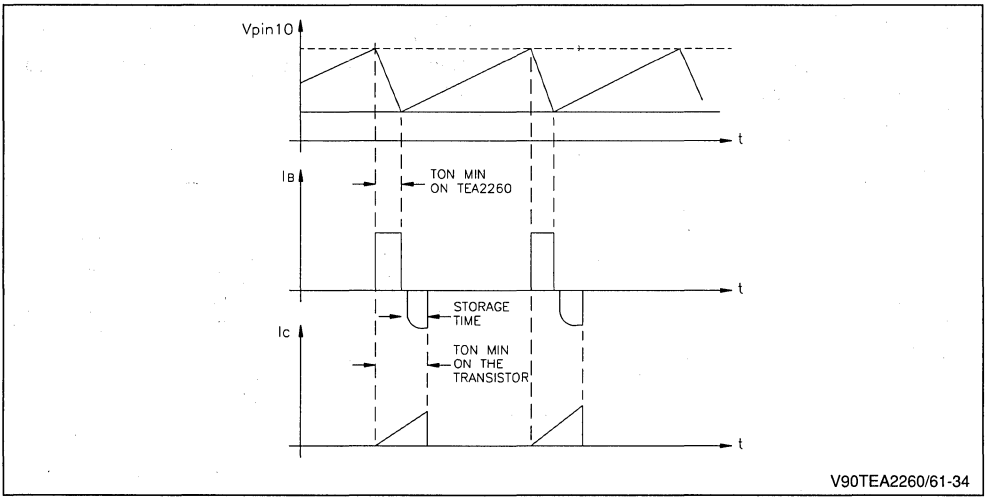
III.2.3. Oscillator frequency

The free running frequency is given on II.2.

The typical value of minimum conduction time $T_{ON(Min.)}$ on the output of the TEA2260/61 is given by: $T_{ON(Min.)} = 1040 \times C_O$

Note : the minimum conduction time $T_{ON(Min.)}$ on the transistor is longer due to the storage time.

Figure 34.



Numerical application

F_O = 16kHz

C_O is chosen at 1nF

so T_{ON} min on the TEA2260/61 = 1µs

$$R_O = \frac{1}{F_O \times C_O \times 0.66} - 1.57 \cdot 10^3$$

$$R_O = \frac{1}{16\ 10^3 \times 1\ 10^{-9} \times 0.66} - 1.57 \cdot 10^3$$

R_O = 93kΩ

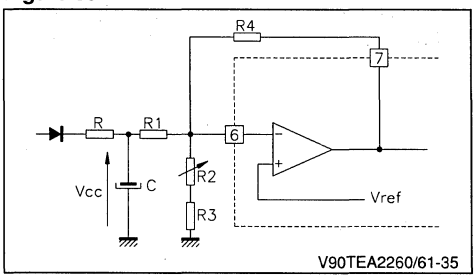
R_O = 100kΩ is chosen.

Note : F_O is chosen relatively low to avoid magnetization of the transformer during the start-up phase.

III.2.4. Regulation loop

In stand by mode the error amplifier of the TEA2260/61 carries out the regulation.

Figure 35.



- The R.C. filter is necessary to avoid the peak voltage due to the leakage inductance. The time constant τ = RC is about 30µs < R.C. < 150µs as a function of the transformer technology.
- To achieve a stable behaviour of the regulation loop and to decrease the ripple on the output voltage in stand by mode the time constant should be approximately :

$$(R_1 + R_2 + R_{3)} \times C \cong \frac{R_{OUT} \times C_{OUT}}{15}$$

with : C_{OUT} (filtering output capacitor) and R_{OUT} (load resistor on the output in stand by mode)

- To ensure a stable behaviour in stand-by mode the amplifier gain is choosen to :

$$G = \frac{R_4}{R_2 + R_3} \cong 15$$

Calculation of R, R_1, R_2, R_3, R_4

a) The resistor R is given by

$$R = \frac{\tau}{C}$$

C choosen between 1µF < C < 10µF

τ = 80µs is chosen

C = 2.2µF is chosen

Numerical application

$$S_O\ R = \frac{\tau}{C} = \frac{80\ 10^{-6}}{2.2\ 10^{-6}} = 36\Omega$$

b) The resistors R_1, R_2, R_3 are given by

$$R_1 + R_2 + R_3 \cong \frac{C_{OUT} \times R_{OUT}}{15 \times C}$$

with :

V_{REF} : reference voltage of the error amplifier

$V_{REF} = 2.5V$

$V_{CC(stand\text{-}by)}$: Vcc voltage in stand by mode.

$V_{CC(stand\text{-}by)} = 0.9 \times V_{CC}$ (in normal mode)

Numerical application

with :

$V_{CC} = 13V$

$V_{REF} = 2.5V$

$R_{OUT} = 2k\Omega$ on output 135V

$C_{OUT} = 100\mu F$ on output 135V

$C = 2.2\mu F$

$$R_1 + R_2 + R_3 \cong \frac{C_{OUT} \times R_{OUT}}{15 \times C}$$

$$= \frac{100\ 10^{-6} \times 2\ 10^{3}}{15 \times 2.2\ 10^{-6}} = 6k\Omega$$

$$R_2 + R_3 = (R_1 + R_2 + R_3) \times \frac{V_{REF}}{V_{CC(stand\ by)}}$$

$$R_2 + R_3 = 6 \cdot 10^{3} \times \frac{2.5}{0.9 \times 13} = 1.28k\Omega$$

values choosen :

R_2 potentiometer resistor of $1k\Omega$

R_3 fixed resistor $1k\Omega$

$R_1 = (R_1 + R_2 + R_3) - (R_2 + R_3)$

$R_1 = 6k - 1.28k = 4.7k\Omega$

c) The resistor R_4 is given by $R_4 \cong 15 \times (R_2 + R_3)$

Numerical application

$R_4 \cong 15 \times (R_2 + R_3) \cong 15 \times (1.28\ 10^{3}) \cong 18k\Omega$

III.2.5. Overload capacitor

When an overload is detected with the first threshold VIM1 the capacitor C_2 (pin 8) is charged until the end of the period as shown in figure 36.

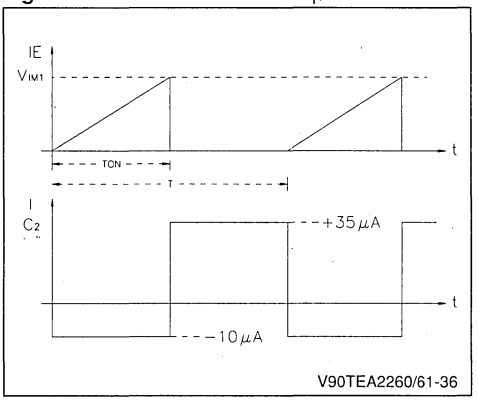
So the average load current is given by :

$$I_{C2} = \frac{T - T_{ON}}{T} \times I_{CH} - I_{DISCH}$$

the threshold to cut off the TEA2260/61 power supply is 2.5V typically and hence the delay time before overload detection is given by :

$$T_{overload} = \frac{2.5 \times C_2}{(\frac{T - T_{ON}}{T} \times I_{CH}) - I_{DISCH}}$$

Figure 36 : Load of Overload Capacitor.



Numerical application

with : maximum overload time = 40ms

the longer delay time is obtained when

$T_{ON} = T_{ON(Max.)}$

$$C_2 = ((\frac{T - T_{ON(Max.)}}{T} \times I_{CH}) - I_{DISCH}) \times \frac{T_{overload}}{2.5}$$

$$C_2 = (0.55 \times 45 \times 10^{-6} - 10 \times 10^{-6} \frac{40 \cdot 10^{-3}}{2.5} \cong 220nF$$

Note : in practice, the overload capacitor value must be greater than the soft start capacitor ($C_2 \geq C_1$) to ensure a correct start up phase of the power supply.

III.2.6 Soft start capacitor

Refer to paragraph II.5 for the soft start function explanation.

The soft start duration is given by :

$$T_{SOFTSTART} = \frac{(2.7 - 1.5) \times C_1}{9 \cdot 10^{-6}}$$

$$C_1 = 7.5 \cdot 10^{-6} \times T_{SOFT\ START}$$

Numerical application

with : Tsoft start = 30ms

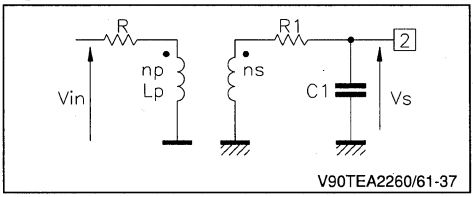
$C_1 = 7.5\ 10^{-6} \times 30\ 10^{-3} = 220nF$

III.2.7. Feed back voltage transformer

A feedback voltage transformer is used to send information from the secondary circuit (master circuit) to the primary circuit (slave circuit).

This transformer is needed to provide an electric insulation between primary and secondary side.

Figure 37.



The feedback input of TEA2260/61 is fed with logic level (threshold 0.9V)
It is necessary to have the same waveform on the primary side as on the secondary side.
For this reason the time constant must be higher than the maximum conduction time in normal mode.
Hence the primary inductance Lp must be calculated as follows :

$L_P > 3.R.T_{ON(Max.)}$

Numerical application

with :

$T_{ON(Max.)} = 28\mu s$

$R = 270\Omega$

$L_P > 3 \times 270 \times 28\ 10^{-6} = 22mH$

a) When the TEA5170 is used VIN = 7V

$$\frac{ns}{np} = \frac{V_{S(min)}}{V_{IN} \times (1 - \frac{T_{ON(max)}}{T})}$$

$$\frac{ns}{np} = \frac{1.5}{7 \times (1 - 0.45)} = 0.389$$

b) When the TEA 2028 is used VIN = 12V

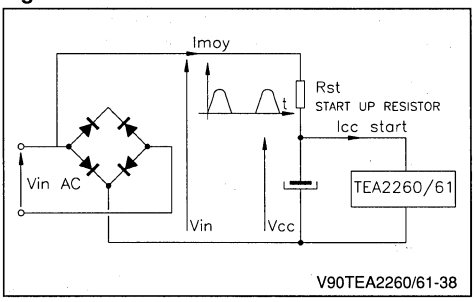
$$\frac{ns}{np} = \frac{1.5}{12 \times (1 - 0.45)} = 0.227$$

Note : The $R_1.C_1$ filter is used to damp oscillation on the secondary side of the feedback transformer. The time constant $R_1 \times C_1 \cong 0.1\mu s$.

III.2.8. Start up resistor

After switching on the power supply the filtering capacitor on V_{CC} of TEA2260/61 is charged through a resistor connected to the mains input voltage. Do not connect this resistor to the high voltage filtering capacitor because there is enough energy in this capacitor to cause three attempted restarts and to cut off the TEA2260/61 on fault detection when the power supply is switched off. Hence it is recommended to connect the start-up resistor as follows:

Figure 38.



Start-up delay time

$$I_{MOY} = \frac{\sqrt{2} \times V_{IN\ AC(min)}}{\pi \times R_{ST}}$$

$$\text{Start-up delay time} = Tst = \frac{V_{CC\ START}}{I_{MOY} - I_{CC\ START}} \times C$$

$$R_{ST} = \frac{\sqrt{2} \times V_{IN\ AC(min)}}{\pi \times \left((C \times \frac{V_{CC\ START}}{T_{ST}}) + I_{CC\ START} \right)}$$

Power dissipated in start-up resistor

$$P = \frac{V_{IN\ AC(max)}^2}{2\ .\ R_{ST}}$$

Numerical application

with :

start-up delay time = 1s

$V_{IN(max)} = 370V$ DC ($V_{IN\ AC(max)} = 265V$)

$V_{IN\ AC(min)} = 175V$

$V_{CCstart} = 10.3V$

$I_{CCstart} = 0.7mA$

$C = 220\mu F$

$$R_{ST} = \frac{2 \times 175}{\pi \times (220\ 10^{-6} \times 10.3 + 0.7\ 10^{-3})} = 26k\Omega$$

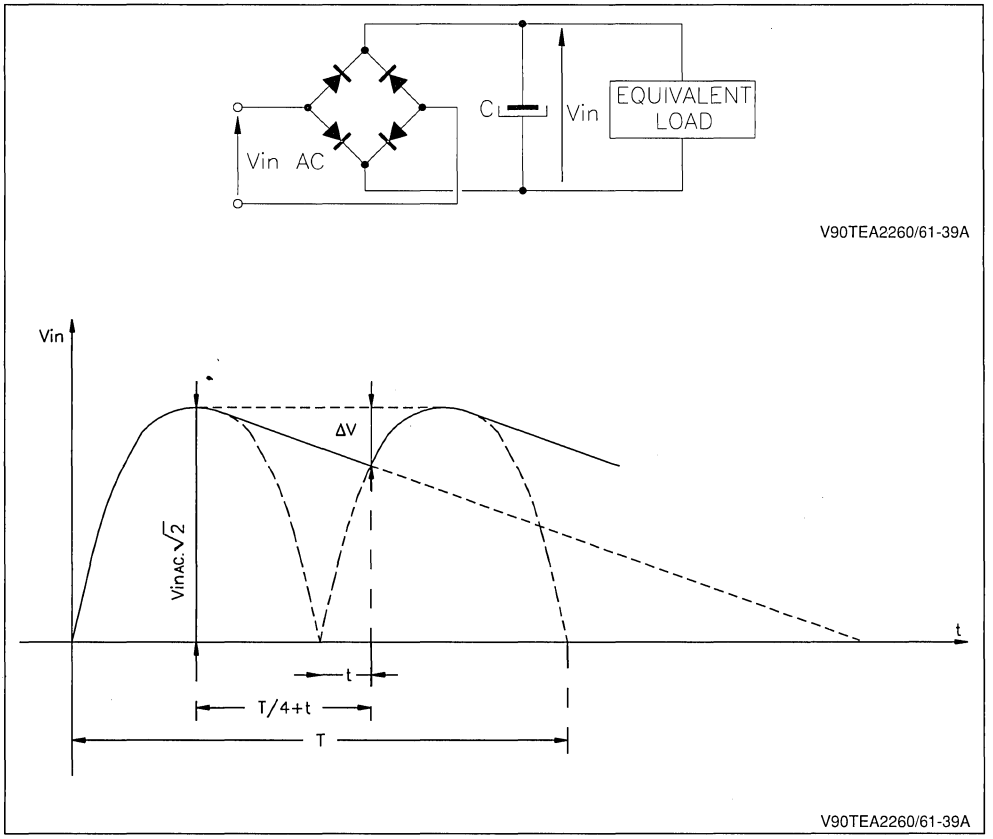
Value choosen = $22k\Omega$

Power dissipated

$$P = \frac{(265)^2}{2 \times 22\ 10^3} = 1.6W$$

III.2.9. Determination of high voltage filtering capacitor

Figure 39.



Hypothesis :

ΔV : ripple on the filtering voltage
$V_{IN.AC(min)}$: minimal value of A.C. input voltage
T : period of the mains voltage
P_{OUT} : output power of the power supply
η : efficiency of the power supply

$$C = \frac{T}{2\pi} \times \frac{\frac{\pi}{2} + \text{ArcSin}\left(1 - \frac{\Delta V}{V_{IN\ AC(min)} \times \sqrt{2}}\right)}{\Delta V \times V_{IN\ AC(min)} \times \sqrt{2}} \times \frac{P_{OUT}}{\eta}$$

Numerical application

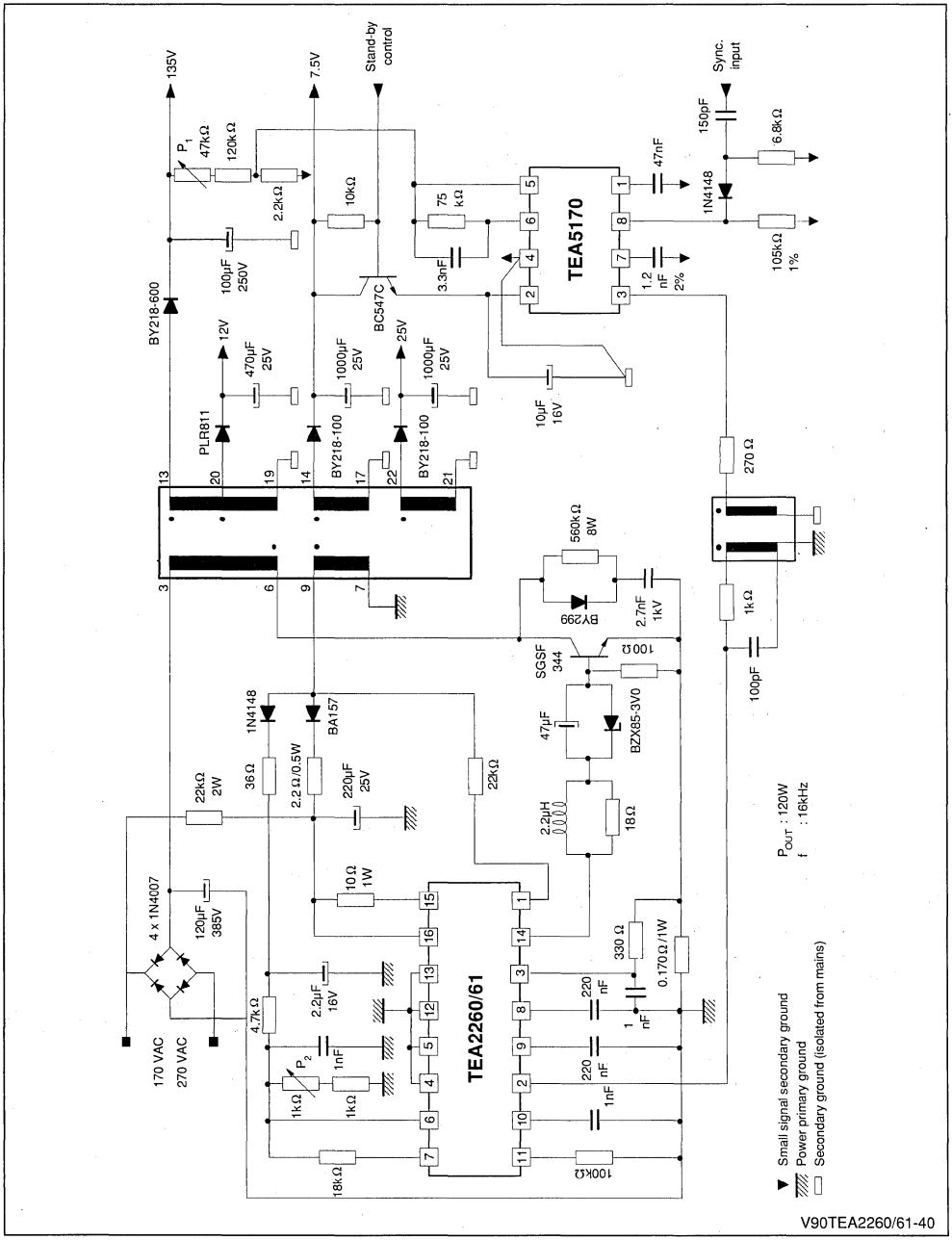
ΔV = 40V
$V_{IN\ AC(min)}$ = 170 VAC
T = 20ms
P_{OUT} = 120W
η = 0.85

$$C = \frac{20\ 10^{-3}}{2\pi} \times \frac{\frac{\pi}{2} + \text{ArcSin}\left(1 - \frac{40}{250}\right)}{40 \times 250} \times \frac{120}{0.85} = 115\mu F$$

value choosen : C = 120µF

III.3. ELECTRICAL DIAGRAM

Figure 40.



IV. TV APPLICATION 140W - 220 VAC - 32kHZ SYNCHRONIZABLE

All details concerning the determination of external components are described in section III.

IV.1. APPLICATION CHARACTERISTICS.

- Discontinuous mode flyback SMPS
- Stand-by function using the burst mode of TEA2260.
- Switching frequency in burst mode : 16kHz
- Switching frequency in normal mode : 32kHz
- Nominal mains voltage : 220 VAC
- Mains voltage range : 170 VAC to 270 VAC
- Output power range in normal mode $25W < P_O < 140W$
- Output power range in stand-by mode $2W < P_O < 45W$
- Efficiency at full load > 80%
- Efficiency in stand-by mode (Po = 7W) > 50%
- Short circuit protection
- Long duration overload protection
- Complete shut down after 3 restarts with fault detection for TEA2260
- Complete shut down when V_{C2} reaches 2.6V for TEA2261

***Load regulation* (VDC = 310V)**

Output 135V (± 0.18%) → (I_{135} : 0.01A to 0.8A; I_{25} = 1A)

Output 25V (± 2%) → (I_{135} : 0.8A; I_{25} = 0.5A to 1A)

***Line regulation* (I_{135} : 0.8A; I_{25} : 1A)**

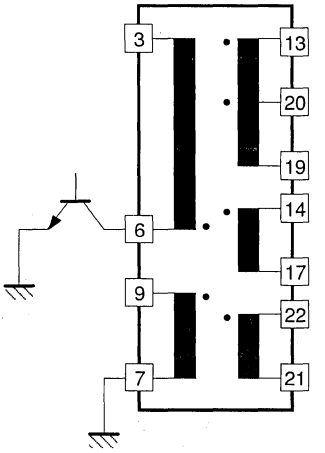
Output 135V (± 0.13%)→ (210V < VDC < 370V)

Output 25V (± 0.17%)

IV.2. TRANSFORMER CHARACTERISTICS

- Reference : OREGA.SMT5. G4576-03
- Electrical Data :

Figure 41.

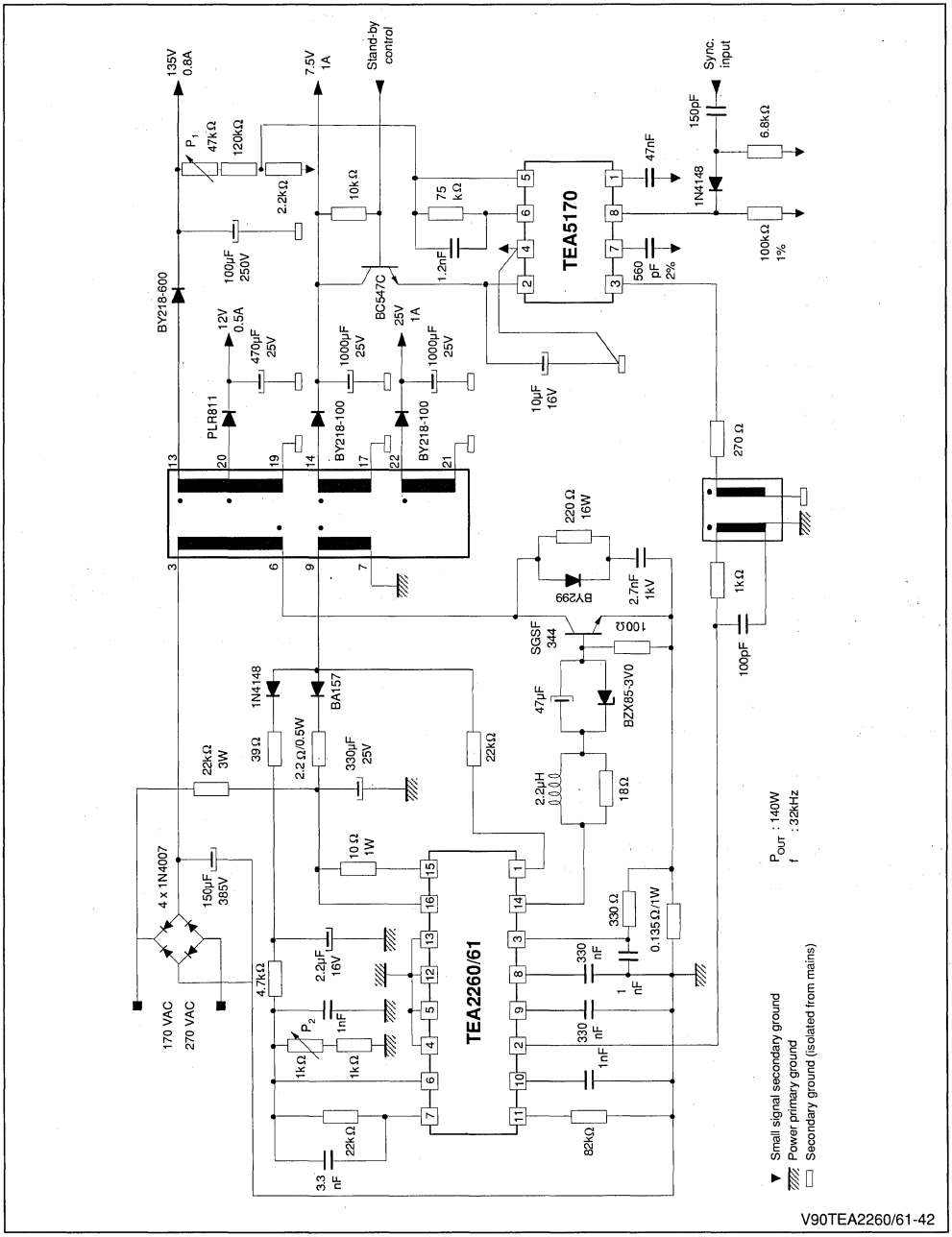


V90TEA2260/61-41

Winding	Pin	Inductance
n_p	3-6	790µH
n_{aux}	7-9	5.4µH
n2	19-13	338µH
n3	19-20	4.8µH
n4	14-17	3.4µH
n5	22-21	13µH

IV.3. ELECTRICAL DIAGRAM

Figure 42.



V. TV APPLICATION 110W -220 VAC - 40kHz REGULATED WITH OPTOCOUPLER

This application works in asynchronous mode. The regulation characteristics are very attractive (output power variation range from 1W to 110W due to automatic burst mode (see II.6). In this configuration higher is the regulation loop gain, lower is the output voltage ripple in burst mode (e.g. ouput voltage ripple 0.8% with a loop gain of 15).

V.1. FREQUENCY SOFT START

The nominal switching frequency is 40kHz but during the start-up phase the switching frequency is shifted to 10kHz in order to avoid the magnetization of the transformer.
Otherwise the second current limitation will be reached at high input voltage and hence the power supply will not start.

V.2. APPLICATION CHARACTERISTICS

- Discontinous mode Flyback SMPS
- Switching frequency : 40kHz
- Nominal mains voltage : 220 VAC
- Mains voltage range : 170 VAC to 220 VAC
- Output power in normal mode : 30W < P_O < 110 W
- Output power in burst mode : 1W < P_O < 30W. The transient phase between normal mode and burst mode is determinated automatically as a function of the output power. Hence the regulation of the output voltage is effective for an output power variation of 1W < P_O < 110W
- Efficiency as full load > 80%
- Efficiency in burst mode (P_O = 8W) > 50%
- Short circuit protection
- Open load protection
- Long duration overload protection
- Complete shutdown after 3 restarts with fault detection for TEA2260
- Complete shut down when V_{C2} reaches 2.6V for TEA2261

Load regulation *(VDC = 310V)*
Output 135V (± 0.15%) → (I_{135} : 0.05A to 0.6A; I_{25} = 1A)
Output 25V (± 2.5%) →(I_{135} = 0.6A; I_{25} : 0.25 to 1A)

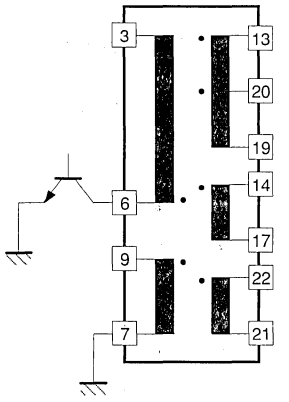
Line regulation *(I_{135} : 0.6A; I_{25} : 1A)*
Output 135V (± 0.30%) → (210V < VDC <, 370V)
Output 25V (± 0.30%)

Influence of the audio output on the video output
Output 135V (± 0.1%) →(I_{135} = 0.6A; I_{25} : 0 →1A)
Output 135V (± 0.05%) →(I_{135} = 0.3A; I_{25} : 0 →1A)

V.3. TRANSFORMER SPECIFICATION

- Reference : OREGA.SMT5. G4576-02
- Mechanical Data :
  - Ferrite : B50
  - 2 cores : 53 x 18 x 18 (mm) THOMSON LCC
- Electrical Data :

Figure 43.

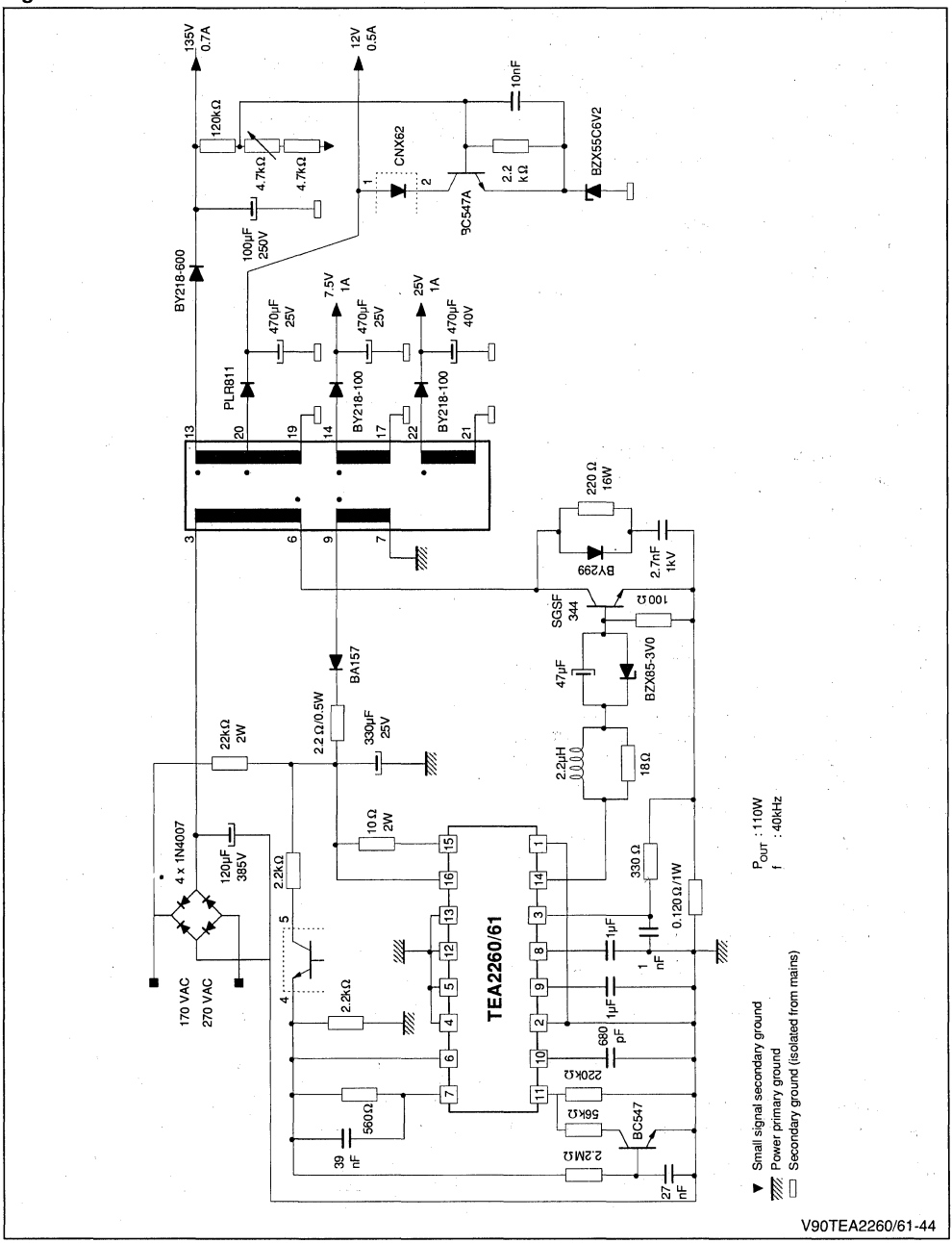


V90TEA2260/61-43

Winding	Pin	Inductance
n_p	3-6	790µH
n_{aux}	7-9	5.4µH
n2	19-13	338µH
n3	19-20	4.8µH
n4	14-17	3.4µH
n5	22-21	13µH

V.4. ELECTRICAL DIAGRAM

Figure 44.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2018A-TEA2019
FLYBACK SWITCH MODE POWER SUPPLY IMPLEMENTATION

By : J-Y.COUET & T.PIERRE

SUMMARY

SUMMARY *(CONTINUED)*

I - INTRODUCTION

The aim of this application note is to provide the designer with information on how to design and implement a simple and low-cost switching power supply around the TEA2018A SMPS Controller.

This publication has been sub-divided into 3 distinct sections, namely :

- An overview of the current mode regulation
- Detailed description of TEA2018A characteristics
- Application example of a 30W discontinuous mode flyback converter operating directly on $220V_{RMS}$ mains voltage.

This document also covers a description of **TEA2019** which replaces the **TEA2018A** in applications requiring power transistor turn off synchronization with an external signal.

This function is particularly useful in video applications where the switching transistor turn off is synchronized with the line flyback signal.

SPECIFICATION OF A TYPICAL APPLICATION

- Discontinuous Mode Flyback
- Switching Frequency : up to 40kHz
- Power : the power handling capability is determined by the amount of available base current. Assuming a forced gain of 6 for the power transistor: • $P_{MAX} \approx 60W$ (TEA2018A)
  • $P_{MAX} \approx 90W$ (TEA2019)

II - TABLE OF UNITS AND SYMBOLS

Symbol	Function	Unit
f	Switching Frequency	Hz
f_{OSC}	Oscillator free-running Frequency	Hz
f_{REF}	Reference Frequency (TEA 2019)	Hz
I_{OUT}	Output Current	A
I_P	Primary Current	A
I_S	Secondary Current	A
L_P	Primary Inductance	H
P_{OUT}	Output Power	W
T	Switching Period	s
T_{REF}	Reference Period (TEA2019)	s
t_{ON}	Transistor ON time	s
$t_{ON(L)}$	Conduction time fixed by current regulation	s
t_S	Power transistor storage time	s
V_{AC}	Mains RMS Voltage	V_{RMS}
V_{BE}	Power Transistor base-emitter voltage	V
V_{IN}	Input DC voltage	V
V_{CC}	Positive supply voltage	V
V_{CE}	Power transistor collector-emitter voltage	V
V_{OUT}	Output Voltage	V
ΔI_{CHARGE}	Average current delivered by the PLL of TEA2019	A
η	Power supply efficiency	%

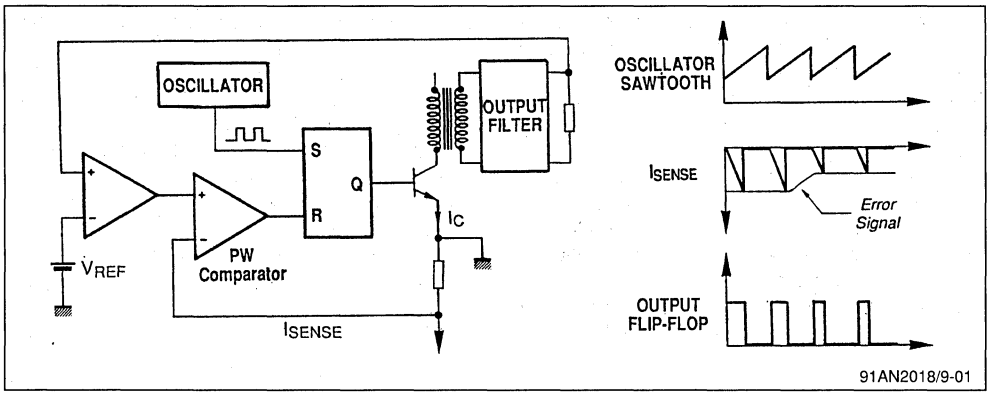
III - CURRENT MODE REGULATION

III.1 - Description

In current mode operation, the regulation is performed by monitoring the peak current through the power switch (switching transistor).

- At every period, the conduction of the power transistor is initialized by a clock signal issued from the oscillator.
- The power transistor is turned-off when its collector current reaches the threshold level fixed by error amplifier.

Figure 1 : Current Mode Control



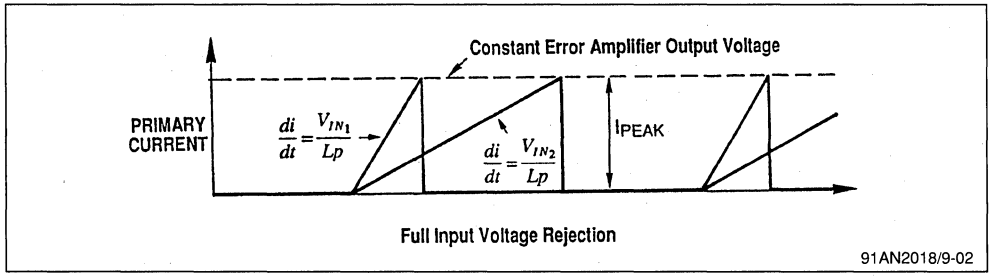
The main advantage of *Current Mode Regulation* in *Discontinuous Mode Flyback Configuration* is that it offers an efficient rejection of all input voltage variations.

The peak current value through the power switch, at constant output power, is independent of the input voltage value.

$$P_{OUT} = \frac{1}{2} \cdot L_P \cdot (I_{PEAK})^2 \cdot f \cdot \eta$$

Variations of the input voltage have no effect on the error amplifier output voltage.

Figure 2

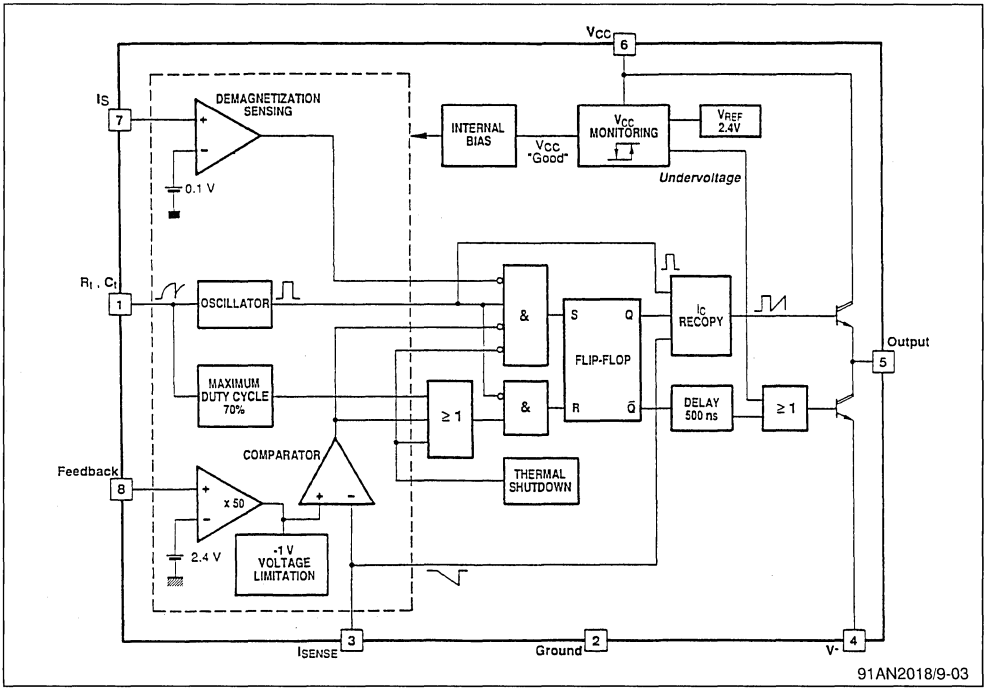


IV - FUNCTIONAL DESCRIPTION OF TEA 2018A

IV.1 - Block diagram

(all values given in the following block diagram are typical values).

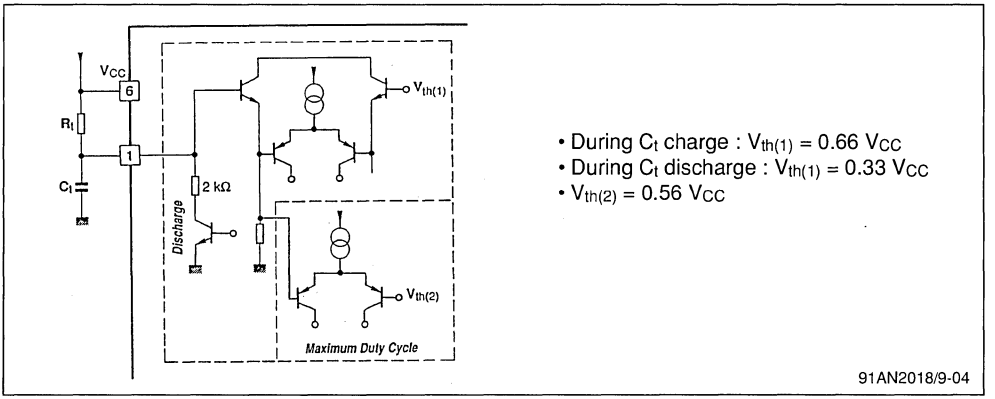
Figure 3



IV.2 - Oscillator and maximum duty cycle

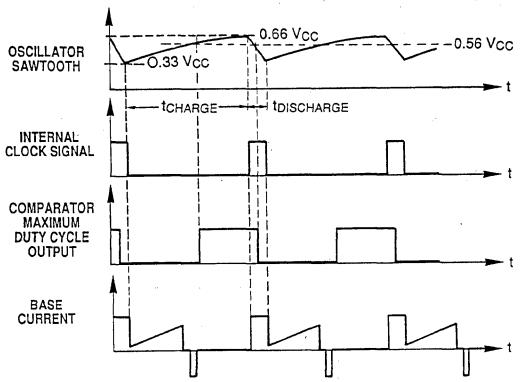
IV.2.1 - Simplified diagram

Figure 4



IV.2.2 - Waveforms

Figure 5



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PERIOD : $T \approx t_{CHARGE} + t_{DISCHARGE}$

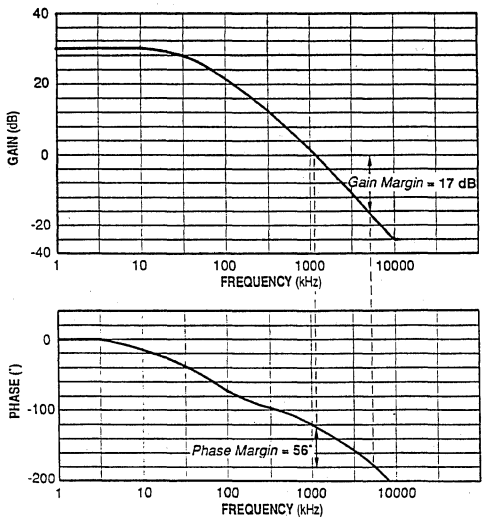
- $t_{CHARGE} \approx 0.66\ R_t\ .\ C_t$
- $t_{DISCHARGE} \approx 0.66\ R_{DISCHARGE}\ .\ C_t$

$$T \approx 0.66\ C_t\ (R_t + 2000)$$

IV.3 - Error amplifier

- The error amplifier gain is internally fixed at 30dB typical value.
  Internally implemented compensation networks set the frequency response characteristics.
- Voltage Reference : The value of the reference voltage applied to the inverting terminal is 2.4 V.

Figure 6 : Error Amplifier Frequency Response Characteristics



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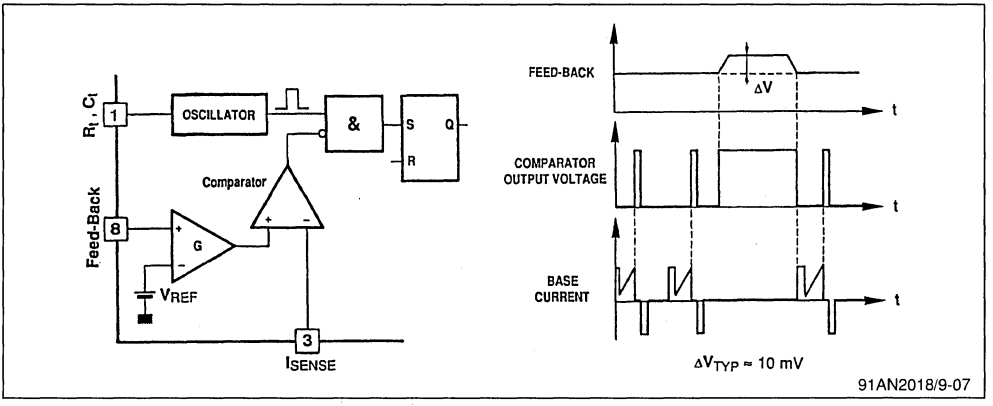
IV.3.1 - Functional behaviour on low-load

When the feed-back voltage exceeds the regulation range, the comparator output remains in high state thereby avoiding the initiation of any new conduction cycle.

Figure 7



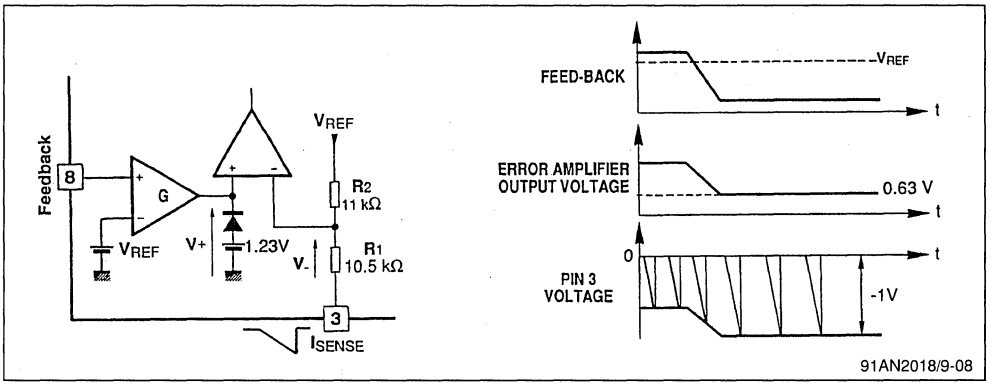
Consequence : On low loads, the conduction frequency becomes lower than the oscillator frequency.

IV.4 - Current measurement & limitation

Peak current through the power switch is set by the error amplifier output voltage.

Clamping the amplifier output voltage at 0.63V will result in limiting the I_{SENSE} pin voltage at 1V level.

Figure 8



In current limitation :

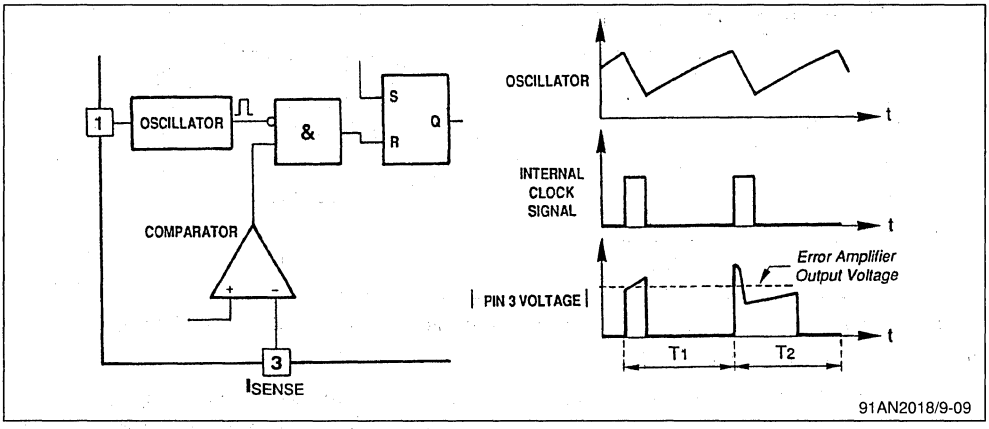
$$\left.\begin{aligned} V^+ &= 1.23\ V - V_{BE} = 0.63V \\ V^- &= V_{(PIN3)} + \left(V_{REF} - V_{(PIN3)}\right)\frac{R1}{R1 + R2} \end{aligned}\right\} \Rightarrow V_{(PIN3)} = -1V$$

IV.4.1 - Disabling the current monitoring function

During oscillator saw-tooth flyback, the output of the PWM comparator is disabled and consequently :

- The minimum conduction time $t_{ON(min)}$ required to discharge the snubber network is fulfilled whatever the status of I_{SENSE} input at the beginning of conduction cycle (T1 period on waveforms of Figure 9).
- All parasitics such as those generated by the recovery of secondary-connected diodes (without RC filter) are eliminated (period T2 on Figure 9).

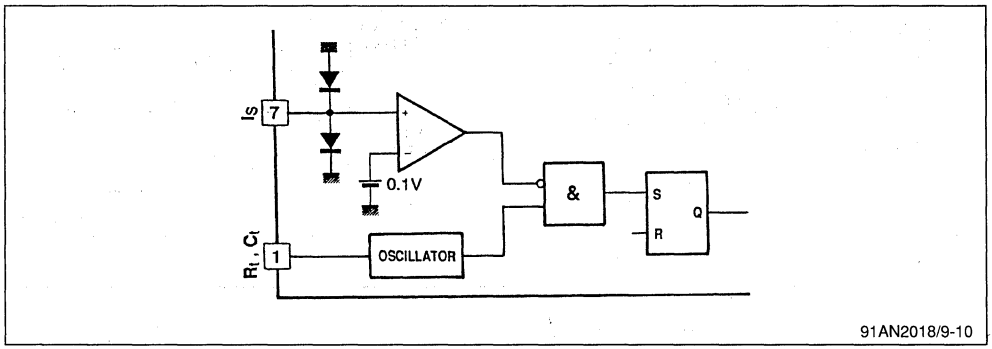
Figure 9



IV.5 - Demagnetization monitoring

No new conduction cycle is allowed as long as the pin 7 voltage remains higher than 0.1V .
When used in *Discontinuous Mode Flyback* configuration, this function will inhibit any new conduction as long as the transformer is not fully demagnetized.
It is obvious that this function offers efficient security in case of overload and short-circuits.

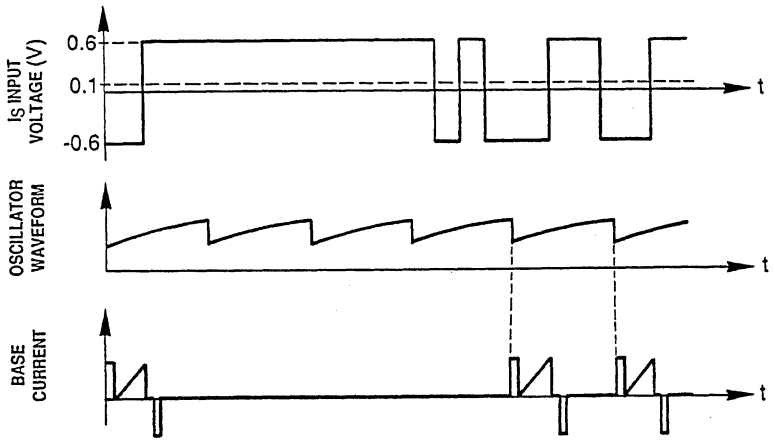
Figure 10 : Demagnetization Sensing



Comments :

- Demagnetization monitoring feature can be used to implement an on-off function.
- This function is disabled by grounding the pin7.

Figure 11 : Waveforms



IV.6 - Thermal protection

When the junction temperature exceeds +150°C, an on-chip protection device will inhibit any new conduction.

IV.7 - TEA2018A behaviour as a function of V_{CC}

Figure 12 : V_{CC} Monitoring Circuit

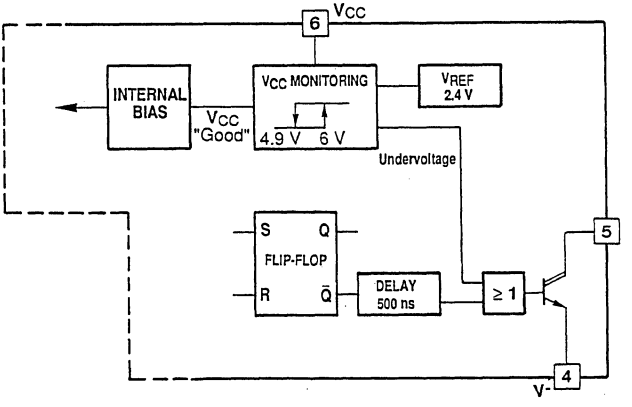
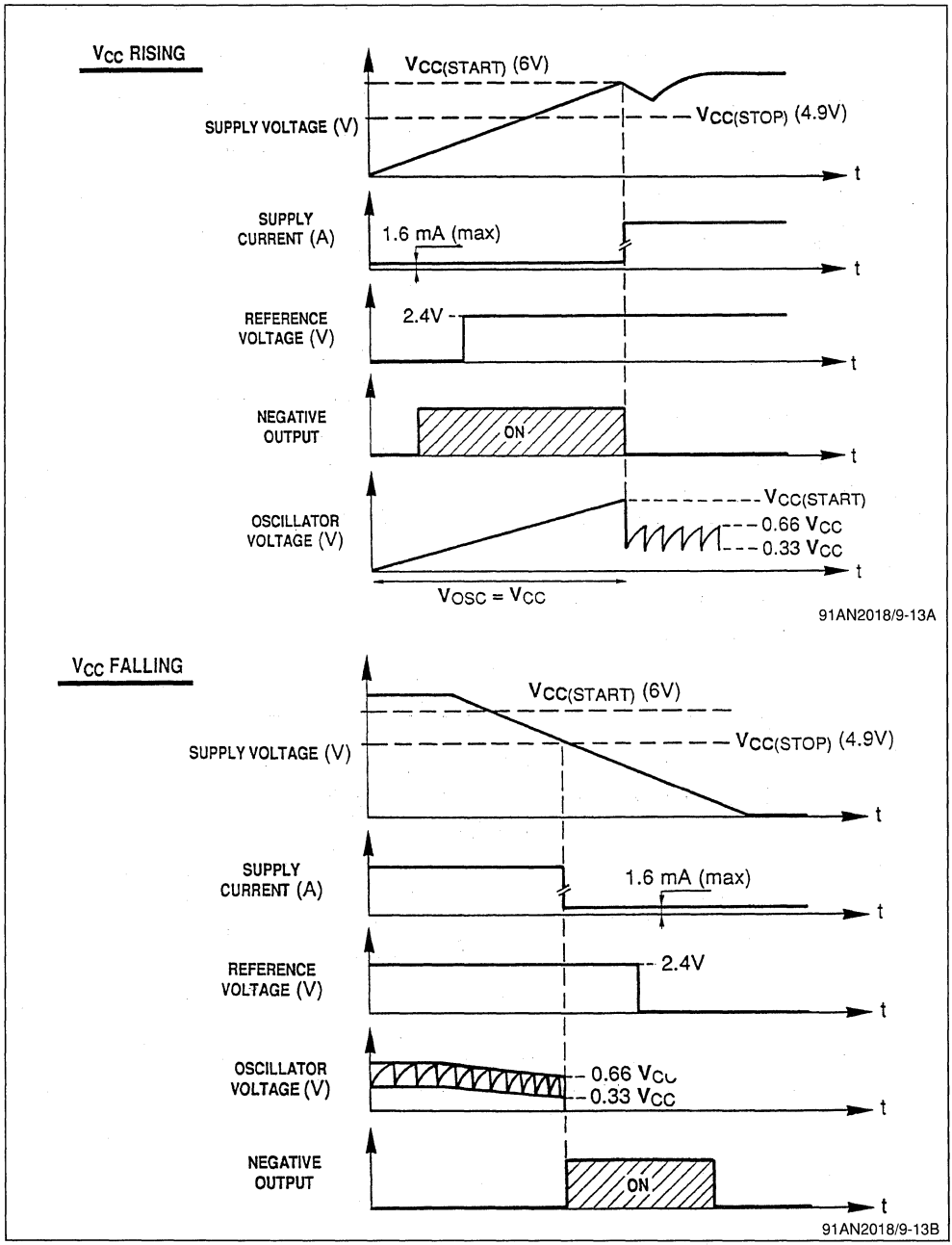


Figure 13 : Waveforms



IV.8 - Output stage (Power transistor base drive)

The TEA2018A has been designed to provide direct drive to bipolar power transistors.

Figure 14 : Simplified Diagram of the Output Stage

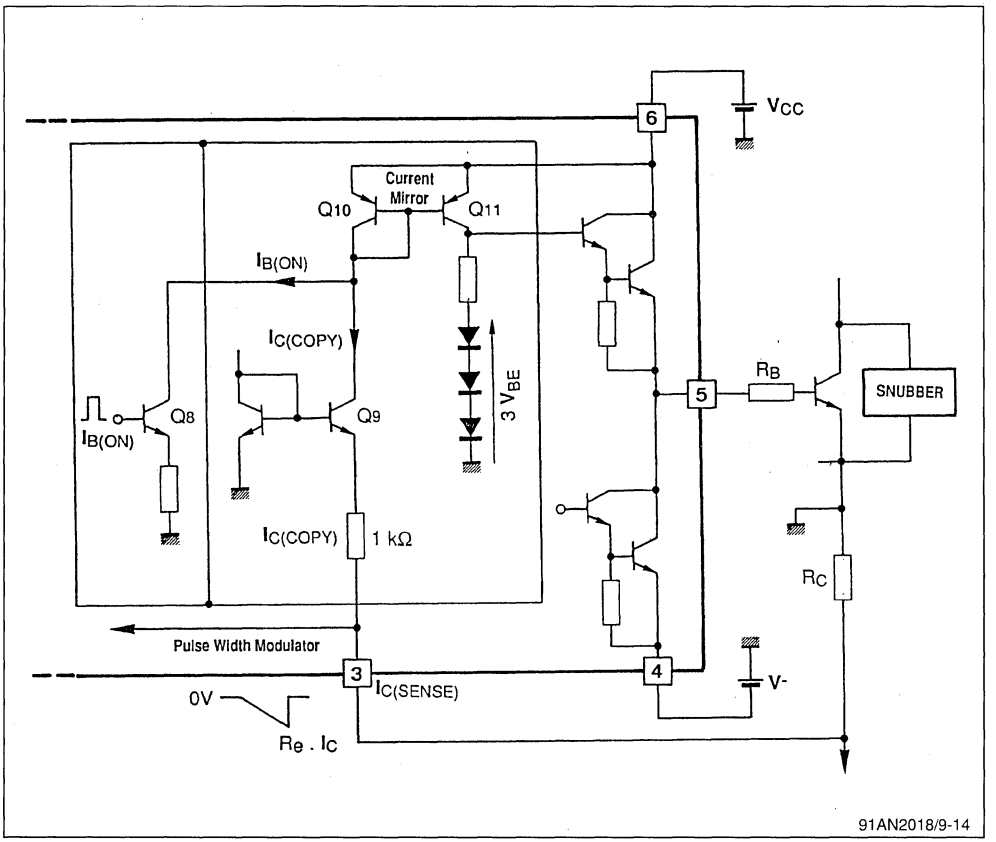
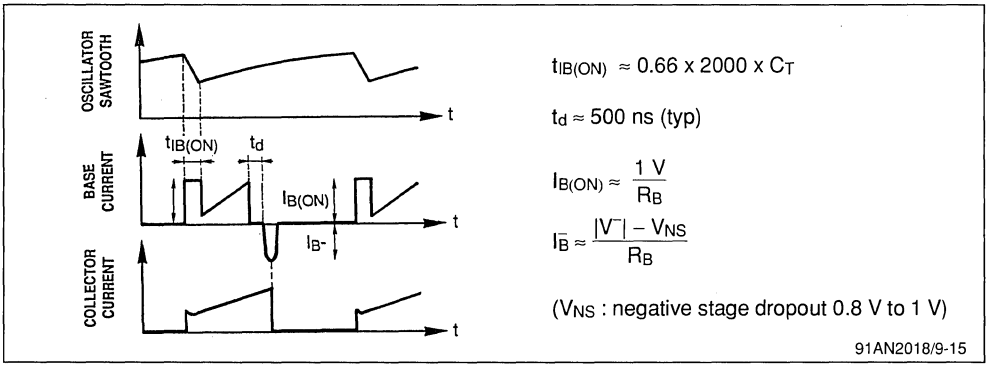


Figure 15 : Waveforms



IV.8.1 - Transistor turn-on

A pulse current "$I_{B(ON)}$" provides for rapid transistor turn-on. The duration of this pulse is equal to the oscillator saw-tooth fall time.

The value of this current is : $I_{B(ON)} \approx 1V/R_B$

IV.8.2 - Proportional base drive

Once the turn-on current pulse $I_{B(ON)}$ has been issued, the internal current recopy device of TEA2018A will output a voltage V_{OUT} such that :

$$\left.\begin{array}{l} V_{out} = V_{(PIN3)} + V_{BE} \\ V_{OUT} = V_{BE} + R_B \cdot I_B \\ V_{(PIN3)} = R_E \cdot I_C \end{array}\right\} \Rightarrow \text{Forced gain} = \frac{I_C}{I_B} = \frac{R_B}{R_E}$$

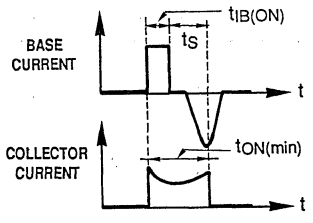
IV.8.3 - Transistor turn-off

The power transistor is turned-off by the application of a negative base current. A 500ns typical interval duration between the positive stage turn-off and the negative stage turn-on, will prevent simultaneous conduction of complementary output stages and also abrupt transistor turn-off.

IV.8.4 - Minimum conduction time

In order to allow the discharge of snubber network, each conduction cycle has a minimum duration equal to $t_{ON(min)}$.

Figure 16



- $t_{ON(min)} = t_{IB(ON)} + t_S$
- t_S : Power Transistor storage time

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V - APPLICATION EXAMPLE

V.1 - Customized application design

V.1.1 - Specifications

Output Power	$3.3W \leq P_{OUT} \leq 30W$
Effective Input Voltage	$176\ V_{RMS} \leq V_{AC} \leq 245\ V_{RMS}$
Input Voltage for Start-up and Regulation	$200\ V_{DC} \leq V_{IN} \leq 350\ V_{DC}$
Regulation Input Voltage after Start-up	$130\ V_{DC} \leq V_{IN} \leq 350\ V_{DC}$
Transistor Reflected Voltage	$V_R = 210V$
Switching Frequency	$f = 27kHz$
Expected Efficiency	$\eta = 70\%$
Output Short-circuit Protection	Yes
Open-load Protection	Yes
2 Outputs	(5V, 2A), (12V, 1.5A)

V.1.2 - Calculation of power elements (see also section 7.1)

- $V_{IN(MIN)} = 200V$
- $\frac{t_{ON(L)}}{T} = 0.426$

(where $t_{ON(L)}$ = conduction time fixed in current limitation mode)

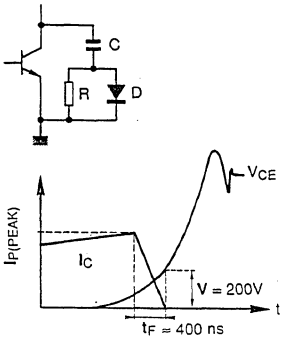
- $I_{P(AV)} = 0.214$
- $I_{P(PEAK)} = 1A$
- $L_p = 3mH$
- $P_{OUT(MIN)} = 2.65W$

- 5V Output : $\frac{ns}{np} \leq 0.029$ $I_{S(PEAK)} = 9.4A \Rightarrow$ Diode : BYW98 - 50
- 12V Output : $\frac{ns}{np} \leq 0.061$ $I_{S(PEAK)} = 7.05A \Rightarrow$ Diode : BYW98 - 50
- Transistor selection

$\left\{ \begin{array}{l} \bullet\ I_{C(MAX)} = 1A \\ \bullet\ V_{C(MAX)} = V_{IN(MAX)} + V_R + V_{SPIKES} \approx 800V \end{array} \right\} \Rightarrow$ BUV 46A

V.1.3 - Transistor switching aid network

Figure 17



- $C = \frac{I_{(PEAK)} \cdot t_F}{2 \cdot V} \approx 1nF$
- $3RC \approx t_{ON(MIN)}$
  $R \approx 1k\Omega$ [for $t_{ON(MIN)} \approx 3\mu s$]
- Diode : BA159
- Maximum Power dissipated in R :

$P = \frac{1}{2} C [V_{IN(MAX)}]^2 . f \approx 1.8W$

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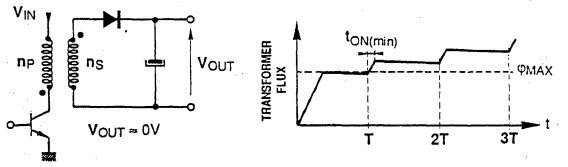
V.1.4 - Demagnetization sensing

a. *Risk of flux runaway without demagnetization sensing*

In the absence of demagnetization sensing, the converter will operate in continuous mode flyback at power supply start-up and also in the case of overloads.

Due to the minimum conduction time imposed by TEA2018A, there will be risk of flux runaway within the transformer and the current through the transistor.

Figure 18



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Flux runaway at start-up or in case of short-circuit : $V_{IN} \cdot t_{ON(MIN)} > V_{LOSS} \cdot \left(\frac{np}{ns}\right) \cdot [T - t_{ON(MIN)}]$

(Where $V_{LOSS} \approx 1.5$ V is the voltage drop accross the rectifier diode and the resistive component of secondary winding).

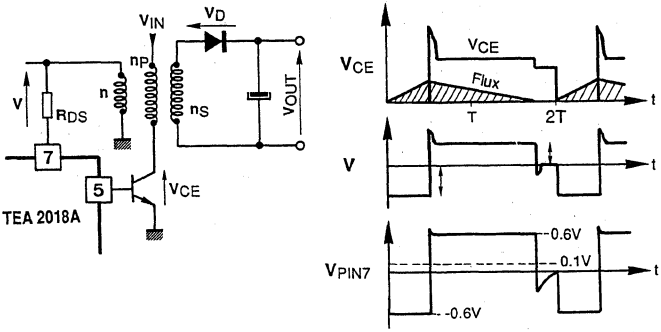
Combining $t_{ON(min)}$ and *demagnetization sensing* functions, will yield highly secure operation ensuring the following functions :

- magnetic flux monitoring
- efficient discharge of snubber networks

b. *Implementing the demagnetization sensing*

The winding used for circuit power supply will also reflect an image of the induced flux. The value of the resistor "R_{DS}" used for this function is not critical and can fall within : $10k\Omega < R_{DS} < 47k\Omega$ range.

Figure 19 : Configuration Arrangement and Short-circuit Waveforms



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No new conduction cycle may be initiated as long as the transformer is not fully demagnetized. On start-up, and in the case of overloads, the demagnetization sensing function will modify the frequency of the conduction cycles accordingly.

c - *Damping network*

Once the transformer has been demagnetized, positive voltage oscillations produced by the discharge of resonant "L_P.C" network may result in unwanted activation of the demagnetization monitoring function.

To prevent this problem, all that required is to damp the voltage oscillations, as shown in Figure 21, through "R_D - D_D" network where diode D_D "shunts" the resistor "R_D".

Figure 20

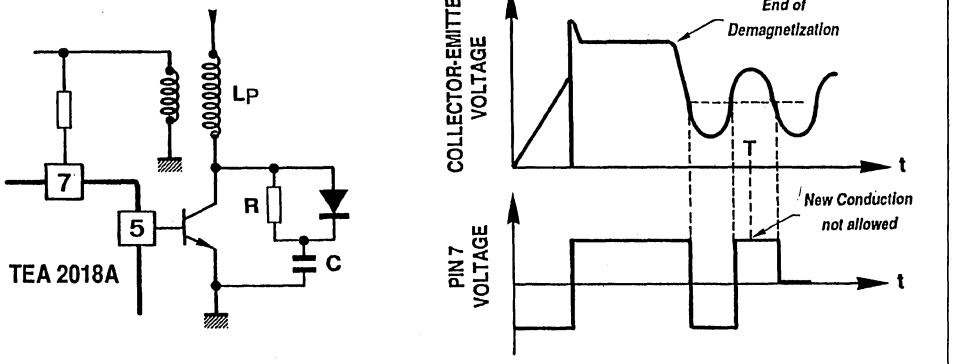
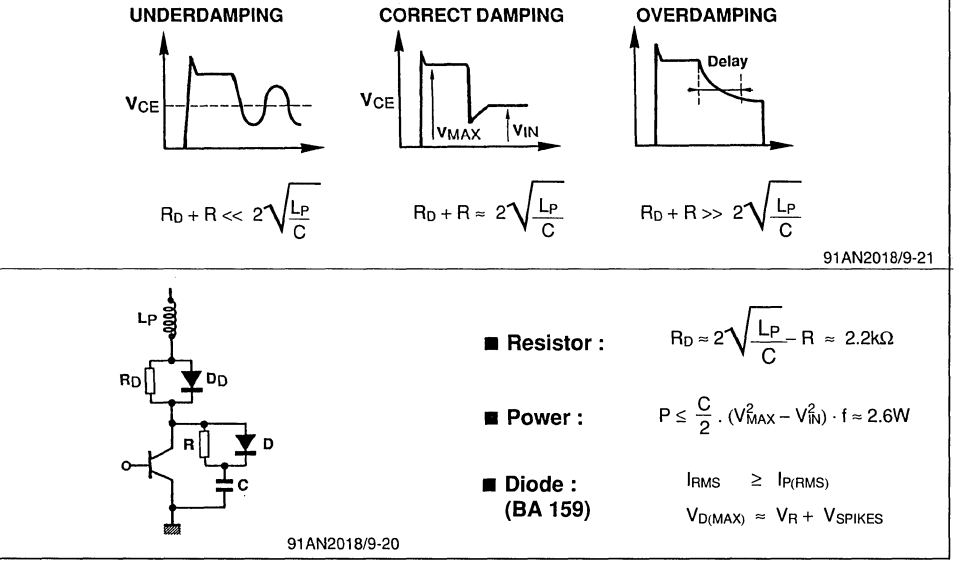


Figure 21

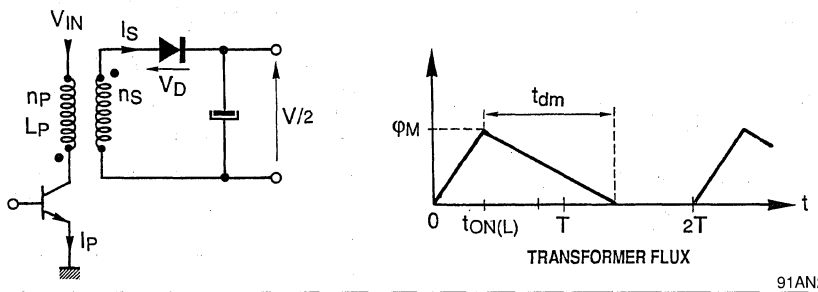


d - *Transformation ratio considerations*

On initial start-up, due to demagnetization monitoring function, the value of conduction frequency will rise in multiples of the normal operating frequency "f" as illustrated below :

Employing a conventionally calculated transformer, the converter will stop operating at "f/2" frequency.

Figure 22



At frequency "f/2" :

$$P_{1/2} = \frac{1}{2} \cdot L(I_p)^2 \cdot \frac{f}{2} = \frac{P_{MAX}}{2}$$

$$V_{1/2} = \frac{V_{out}}{\sqrt{2}}$$

The converter operating frequency will switch from "f/2" to "f" if the following condition is satisfied :

$$t_{on} + t_{DM} < T \qquad (1)$$

(@ f/2 frequency)

$$\varphi_M = L_P \cdot I_P = V_{IN(MIN)} \cdot t_{ON(L)} \qquad (2)$$

(where $t_{ON(L)}$ = conduction time fixed in current limitation mode)

$$\varphi_M = L_S \cdot I_S = \frac{ns}{np}(L_p\, I_P) = \frac{V_{OUT}}{\sqrt{2}} \cdot t_{DM} \qquad (3)$$

Combining (1), (2) and (3) :

$$\frac{ns}{np} \leq \frac{[V_{OUT} + V_D]\,[T - t_{ON(L)}]}{[V_{IN(MIN)} \cdot t_{ON(L)}]\,\sqrt{2}}$$

V.1.5 - Oscillator

The value of capacitor "C_t" is calculated as a function of :

- $t_{ON(min)} : \approx 3\mu s$
- $t_{ON(min)} = t_{IB(ON)} + t_{STORAGE}$ } $C_t = 1.2nF$
- $t_{STORAGE} \approx 1.5\mu s$ } $C_t \geq 470pF$
- $t_{IB(ON)} \approx 0.66\ Ct\ .\ 2000$

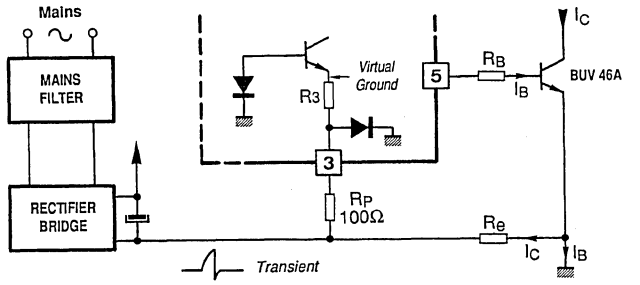
The value of resistor R_t is calculated as a function of period T as follows :

$T = 0.66\ C_t\ (R_t + 2000) = 37\mu s \rightarrow Rt \approx 47k\Omega$

V.1.6 - Power transistor base drive

The "R_e" resistor is calculated as a function of "current limitation" and the resistor "R_B" as a function of "forced gain". Resistor "R_P" can be connected to pin 3 "I_{SENSE}" to protect the device against mains-generated transitional overvoltages.

Figure 23



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Current limitation

$$V_{(PIN3)} \approx 0.88V \text{ (current limitation threshold value)}$$

$$V_{(PIN3)} \approx \frac{R3}{R_P + R3} \cdot R_E \cdot I_C \Rightarrow R_E = 1\Omega \begin{cases} \bullet\ R_p = 100\Omega \\ \bullet\ R3 = 1\Omega \\ \bullet\ I_{C(MAX)} \approx 1A \end{cases}$$

Gain calculation

$$I_{C(MAX)} = 1A \Rightarrow \text{Transistor : BUV46A} \Rightarrow \text{Forced Gain} \approx \frac{I_C}{I_B} = 9$$

$$V_{(PIN3)} = R_B \cdot I_B \,, V_{(PIN3)} = \frac{R3}{R_P + R3} \cdot R_C \cdot I_C \Rightarrow R_B = 8.2\Omega$$

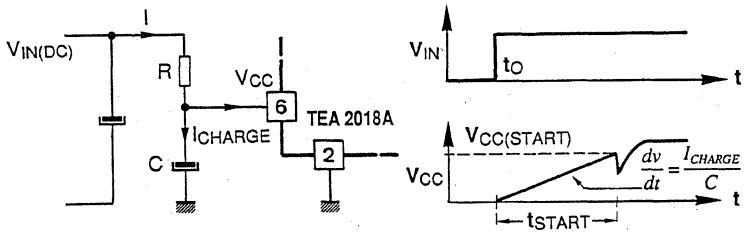
V.1.7 - Self-supply

Power supply start-up

A high value resistor inserted between the "high voltage source" and "V_{CC}" capacitor will charge up this capacitor upon the initial supply start-up.

The TEA2018A starts operating at $V_{CC} \approx 6V$ (typ). On-chip implemented hysteresis of 1.1V (typ) will trigger the self-supply function.

Figure 24



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The value of R is calculated to yield maximum start-up time.

- C = 220µF
- $V_{CC(START)MAX}$ = 6.6V
- $I_{CC(MAX)}$ = 1.6mA
- t_{START} = 3s

- $I_{CHARGE} = \frac{V_{CC(START)MAX} \cdot C}{t_{START}}$
- $R = \frac{V_{AC(MIN)} \cdot \sqrt{2}}{I_{CC(MAX)} + I_{CHARGE}}$
- R = 120 kΩ

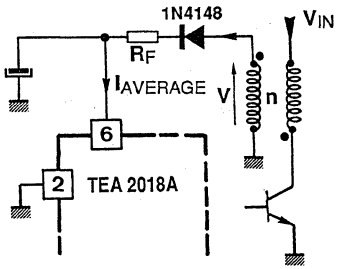
a - *Positive self-supply : V_{CC}*

The V_{CC} supply is provided by a flyback-type winding. The number of turns "n" is selected to yield a voltage "V" of approximately 10V.

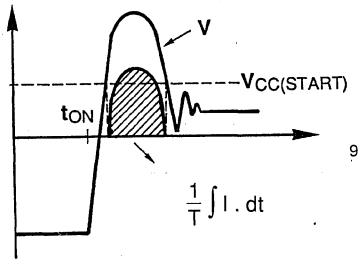
Within the self-supply arrangement, the resistor "R_F = 15Ω" in combination with the capacitor of V_{CC}, form a filter network which attenuates mains-generated voltage spikes.

Note that in the absence of this filter, the energy generated by voltage spikes can often satisfy the power supply requirements of the TEA2018A in case of any short-circuit on low-voltage windings.

Figure 25



$$\frac{n}{n_s} \approx \frac{9 + V_D}{V_{OUT} + V_D}$$



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is sufficiently high to meet the power supply requirements without R_F

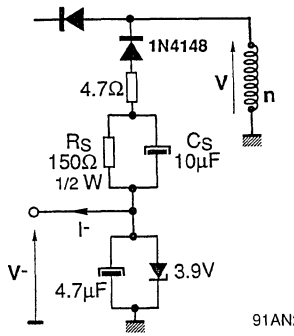
b. *Negative Self-supply : V*
A negative supply voltage "V⁻" is required for efficient transistor turn-off.

This voltage is generated by an auxiliary winding connected in forward arrangement.

The "zener diode" will clamp this negative voltage and make it independent from the input voltage (V_{IN} > 200V).

The "C_S" capacitor will accelerate V- settling process upon the initial power supply start-up. Resistor "R_S" is used to limit the current upon the negative power supply setup.

Figure 26



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- $I_{\overline{AV}} \approx I_{\overline{B}} \times \frac{t_s}{T} \approx 15$ mA

- $R_{S(MAX)} \approx \dfrac{\left(V_{IN} \cdot \frac{n}{n_p}\right) - (1V - |V^-|)}{I_{(\overline{AV})}}$

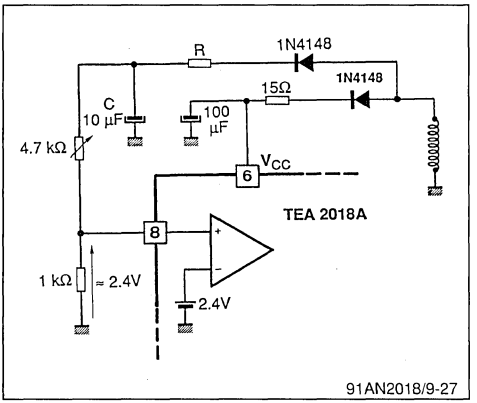
$\approx 230\Omega$ (@ V_{IN} = 200V)

Prefered value : $R_S = 150\Omega$

V.1.8 - Regulation
As illustrated in Figure 28, the self-supply winding is also used for voltage regulation.

To avoid the power drawn by TEA2018A to influence the regulation, the supply for regulation is generated by a source independent from "V_{CC}".

Figure 27



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The RC filter attenuates the parasitics due to voltage spikes generated by switching. However, the cut-off frequency of this filter must be sufficiently high so as to avoid excessive slow-down of the regulation loop response.

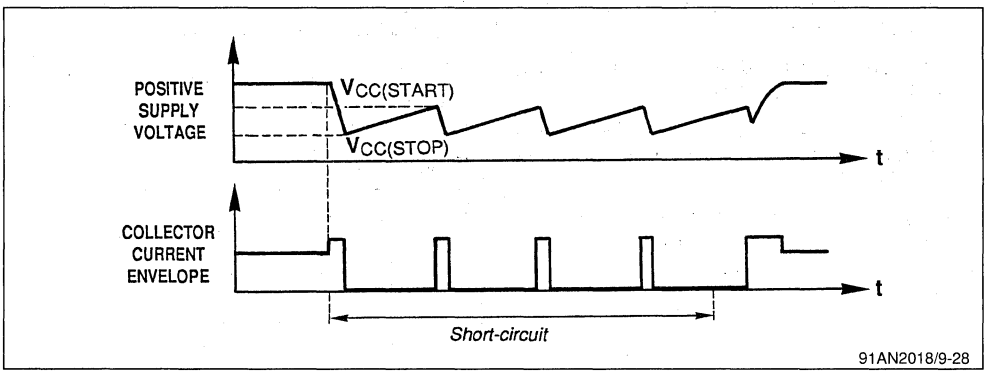
V.1.9 - Operation under overload & short-circuit conditions

In case of any overload, the secondary voltage will fall, circuit power supply will drop below $V_{CC(STOP)}$, consequently TEA2018A stops operating and its power consumption will fall under the current supplied by the start-up resistor.

The capacitor of "V_{CC}" begins charging up and a new conduction cycle will be initiated as soon as "V_{CC}" reaches "$V_{CC(START)}$" level.

The system will function in relaxation mode as long as the overload persists.

Figure 28

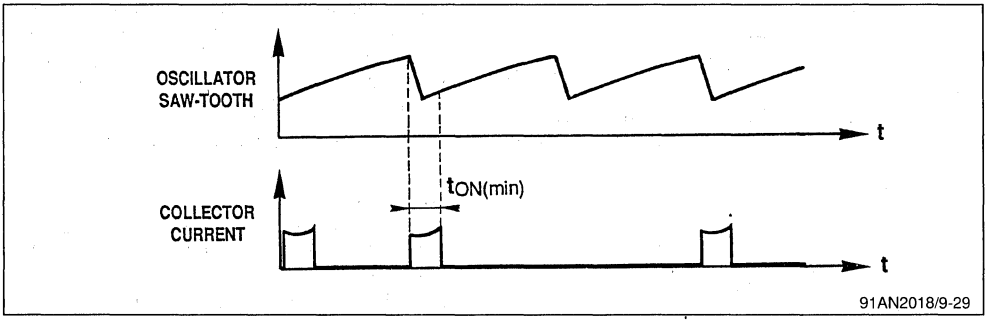


V.1.10 - Operation on Low-loads
When the output power falls below :

$$P_{OUT(MIN)} = \frac{(V_{IN} \cdot t_{(ON(MIN))})^2}{2 \cdot L_P} \cdot f \cdot \eta$$

the regulation becomes incompatible with the operating frequency "f", conduction cycles occur in a random fashion and at a frequency lower than "f".

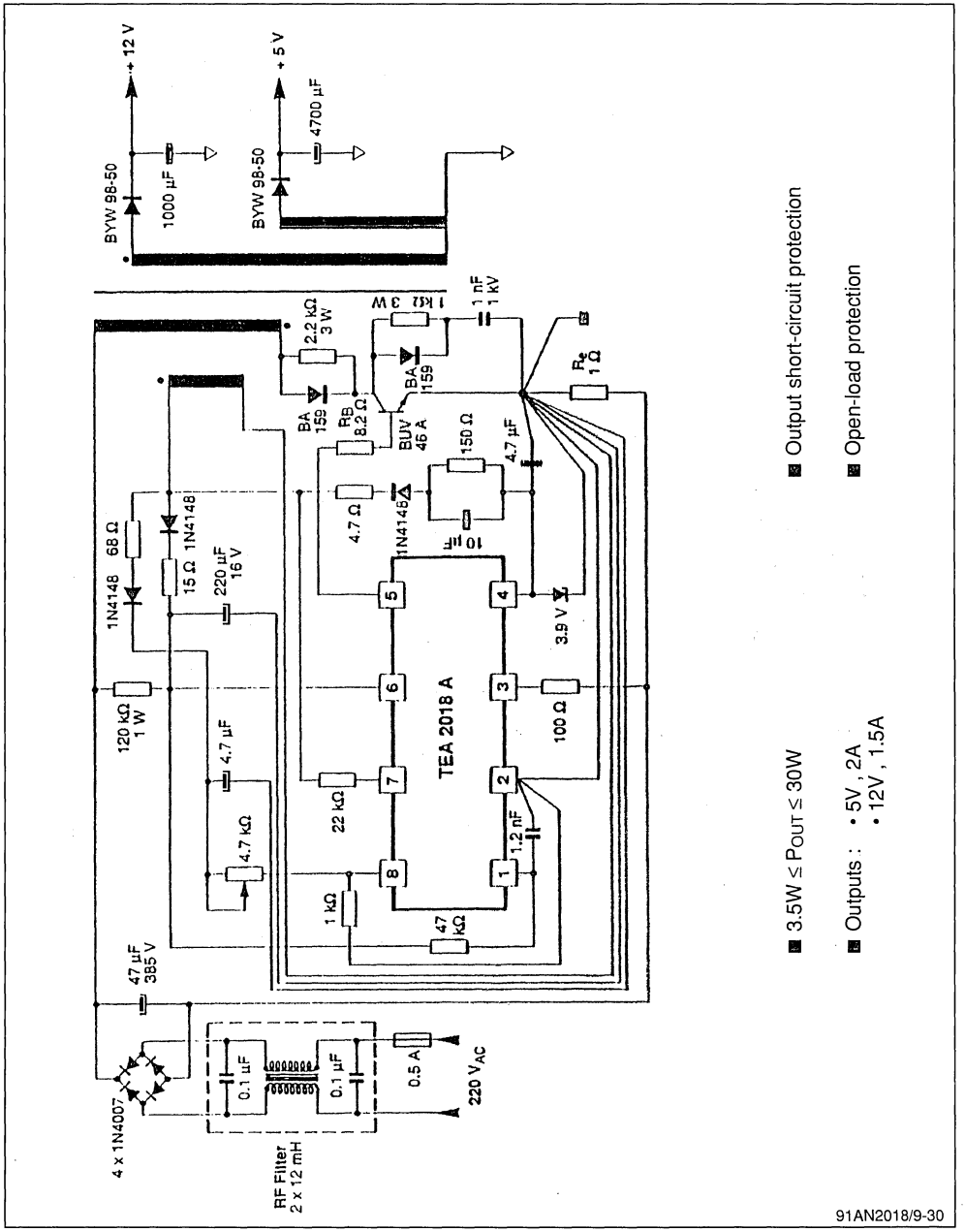
Figure 29



Note : This event has no impact on the power supply reliability.

V.1.11 - Complete Application Diagram

Figure 30



VI - FUNCTIONAL DESCRIPTION OF TEA2019

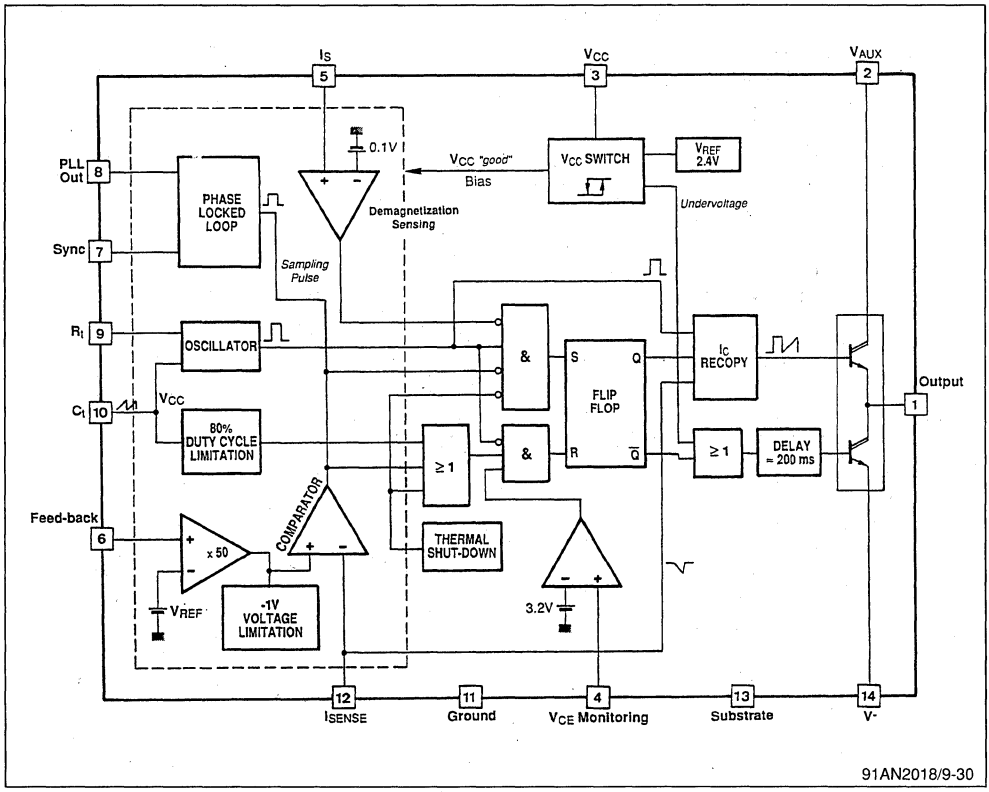
VI.1 - Introduction

The TEA2019 has an internal architecture similar to TEA2018A and offers the following additional features :

- a true positive current source providing linear charge-up of the timing capacitor "Ct".
- an internal PLL which allows synchronization of the power transistor turn-off with an external clock signal
- power transistor desaturation monitoring
- possibility to dissipate externally the power required for transistor base drive

VI.2 - Block Diagram

Figure 31

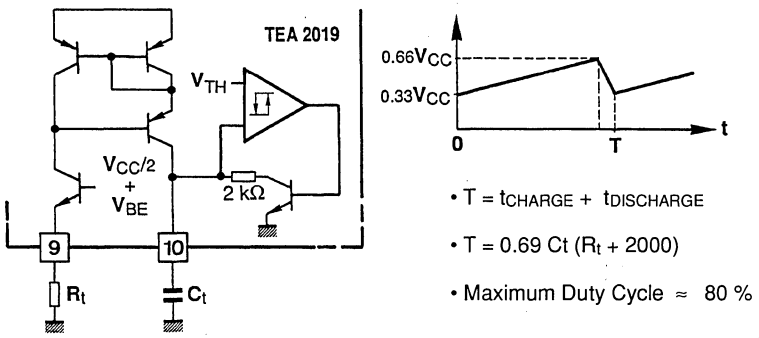


VI.3 - Differences between TEA2018A & TEA2019

VI.3.1 - Oscillator

The oscillator saw-tooth waveform is linear. The capacitor "C_t" charging current is constant and is determined by the value of resistor "R_t".

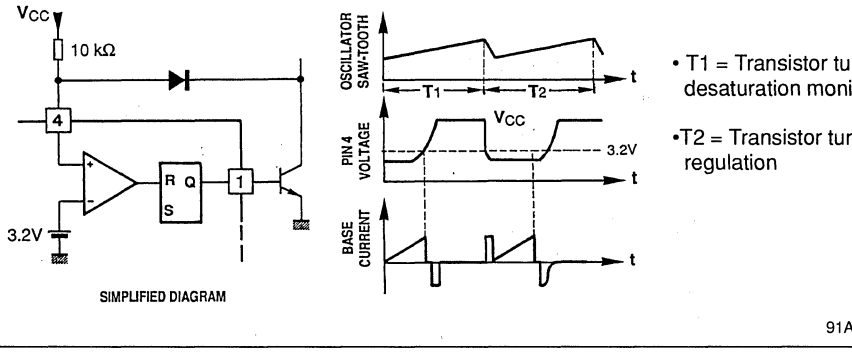
Figure 32



VI.3.2 - V_{CE} Monitoring

If during the power transistor conduction period the pin 4 voltage exceeds 3.2V, the transistor would be turned-off until the next conduction cycle. To disable this function, pin 4 must be grounded.

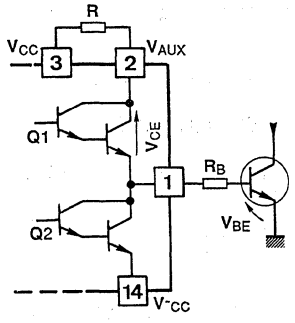
Figure 33



VI.3.3 - Output stage

An external resistor connected between V_{CC} and V_{AUX} will dissipate a portion of the power required by the base drive. The value of this resistor is calculated to be as large as possible but appropriately dimentioned to avoid the saturation of the output stage Q1.

Figure 34



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$$R = \frac{V_{CC} - V_{BE} - V_{CE(MIN)}}{I_{B(MAX)}} - R_B \quad \text{(where } V_{CE(MIN)} \approx 1.5\ V\text{)}$$

- Power dissipated in Q_1 (Flyback) :

$$P = \frac{t_{ON}}{T}\left[(V_{CC} - V_{BE}) \cdot \frac{I_{B(MAX)}}{2} - (R_B + R) \cdot \frac{I^2_{B(MAX)}}{3} \right]$$

- Power improvement compared to TEA2018A :

$$\frac{\Delta P}{P} = \frac{2 \cdot R \cdot I_{B(MAX)}}{3\,(V_{CC} - V_{BE}) - 2 \cdot R_B \cdot I_{B(MAX)}} \approx \frac{2\,(V_{CC} - 3.5\ V)}{V_{CC} - 5V}$$

$$\left\{ \text{at : } V_{CC} = +9\ V \Rightarrow \frac{\Delta P}{P} = 0.5 \quad \text{i.e.} \quad 50\% \right\}$$

VI.3.4 - PLL

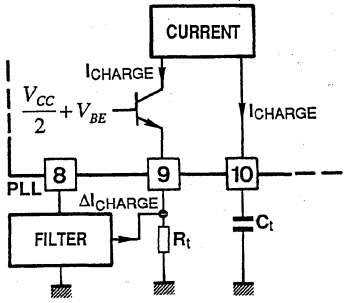
In a discontinuous mode flyback configuration, the power transistor turn-off produces significant amount of noise. It is therefore interesting to synchronize this event with an external signal.

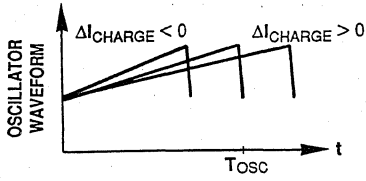
Since the transistor turn-off instant in current mode operation is generally unknown, consequently, only phase and frequency locking of the oscillator will enable to synchronize the transistor turn-off time without disturbing the voltage regulation loop.

a. - *Operating principles*

Oscillator phase and frequency can be accurately controlled by adjusting the charge current of "C_t" capacitor. The PLL behaves as a current generator, the direction and the magnitude of which are function of the phase difference between transistor turn-off and the synchronization signal.

Figure 35





$$I_{CHARGE} = \frac{V_{CC}}{2R_T} - \Delta I_{CHARGE}$$

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b - *Internal structure*

The major building block of the PLL is an analog multiplier whose two inputs are the synchronization signal and power transistor turn-off monitoring signal. Multiplier output signal has a complex spectrum; a low-pass filter is employed to extract the DC and low-frequency components.

Figure 36

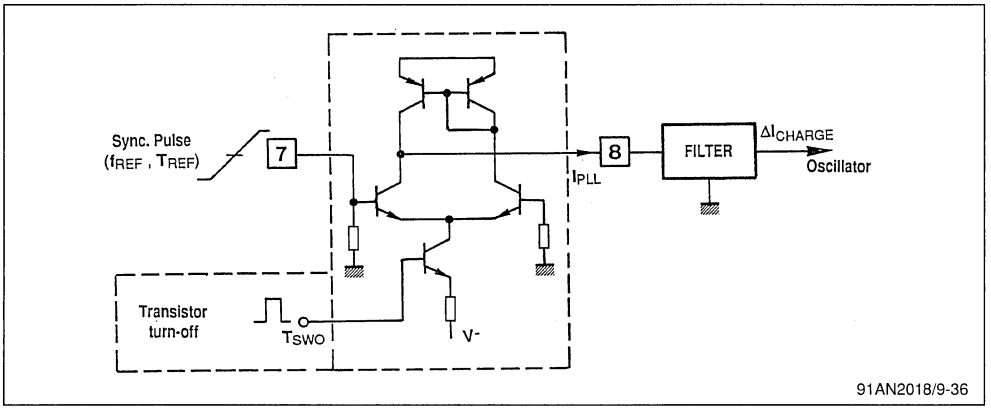
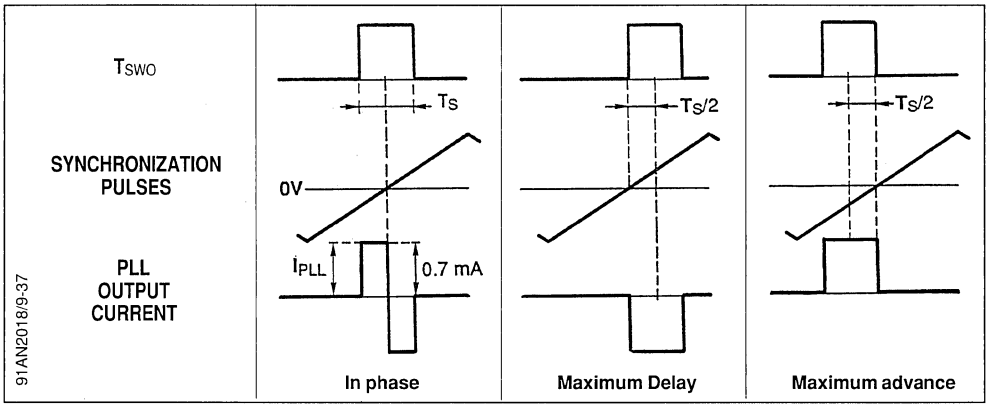


Figure 37 : Synchronization configuration waveforms

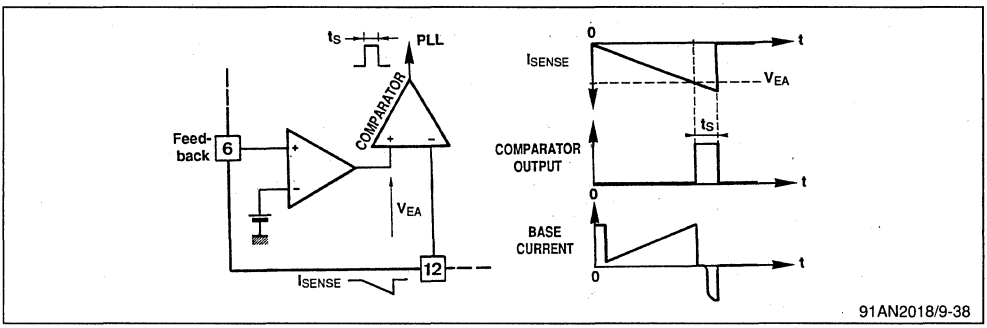


The PLL will source or sink the maximal current when the shift interval between synchronization signal and the transistor turn-off equals $t_s/2$.

c - *PLL input signal*

c1 - Transistor turn-off Signal : T_{SWO}
Due to transistor storage time, the PWM comparator will generate a pulse which will be used as T_{SWO} signal.

Figure 38

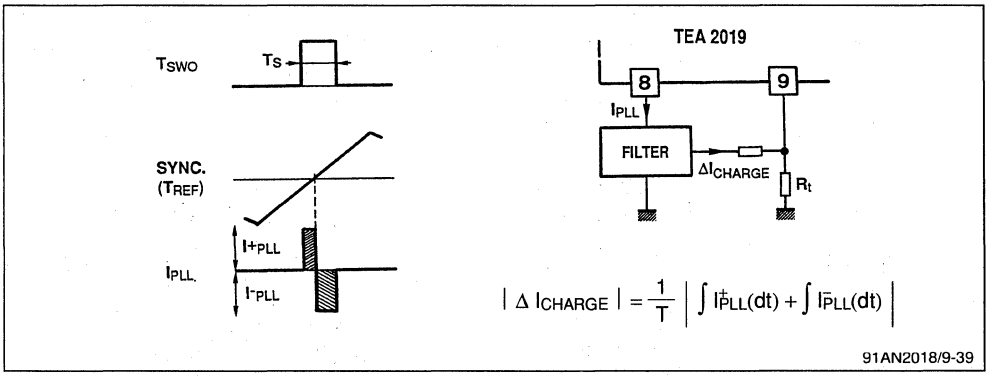


c2 - Synchronization Signal
The characteristics of synchronization signal are outlined in section 6.3.5.

d. - *Characteristics of the PLL*

d1 - Synchronization
When synchronization occurs, the average current delivered by PLL is equal to ΔI_{CHARGE} required for frequency compensation.

Figure 39

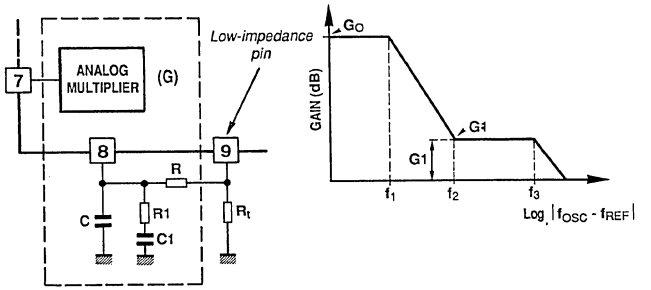


d2. - Capture Range : | f_O - f_{REF} | $_{MAX}$

The signal delivered by PLL prior to synchronization has | f_O - f_{REF} | component. G_{dB} is the overall gain of multiplier and filter stages. Phase locking is possible if the frequency difference | f_O - f_{REF} | satisfies the following relationship :

$$G_{dB\ |\ f_O - f_{REF}\ |} \geq 0\ db$$

Figure 40



$$f_1 = \frac{1}{2\pi (R + R1)\, C1} \qquad f_2 = \frac{1}{2\pi\, R1C1} \qquad f_3 = \frac{R + R1}{2\pi\, .\, C\, .\, R\, .\, R1}$$

e - *Output filter calculation*

For stability reasons, the output filter is calculated at gain G1 ≈ 0 dB.

- "f2" frequency determines the capture range.
- "f3" frequency is equal to the free-running frequency "f_O".
- The "G_O" gain is rather complex to evaluate. By approximation, it is proportional to the switching transistor storage time "t_S".
  At t_S = 2µs , the gain G_O ≈ 24dB

f - *Numerical application*

The following calculations yield the optimum value of capture range :

- f_O = 15.6kHz (switching frequency)
- f_2 = 2.2kHz (this is the selected capture range ± 8µs with respect to 64µs period)

G1 = 0dB , V_{CC} = 8V , t_S = 2µs , C_t = 1.5nF ,

R_t = 56kW , G_O = 24dB

R = R_t yields excellent noise immunity.

$$G_0 - G_1 = -20 \log \frac{R1}{R + R1} \quad \Rightarrow R1 \approx 3.9k\Omega$$

$$f_2 = \frac{1}{2\pi\, R1C1} \quad \Rightarrow C_1 \approx 22nF$$

$$f_3 = \frac{R + R1}{2\pi\, .\, C\, .\, R\, .\, R1} \quad \Rightarrow C \approx 3.3nF$$

g - *Holding range*

Once the capture occurs, the free-running frequency "f_{OSC}" can rise within the holding range without causing loss of synchronization.

When synchronization is achieved, the filter no longer introduces any attenuation and thus the holding range becomes larger than the capture range.The holding range is given by :

$$\Delta T = T_{REF}\, .\, \frac{1}{1 + \dfrac{0.33\, .\, V_{CC}\, .\, C_T}{I_{PLL}\, .\, t_S}}$$

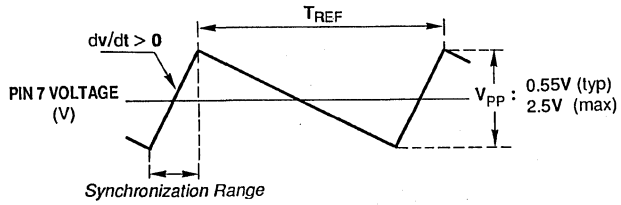
Where :

- T_{REF} : the period of synchronization signal
- I_{PLL} : the maximum current the PLL can source or sink (0.7mA typ)

VI.3.5 - Synchronization signal and the input filter

The synchronization signal applied to PLL input (pin7) must respect the following conditions :

Figure 41



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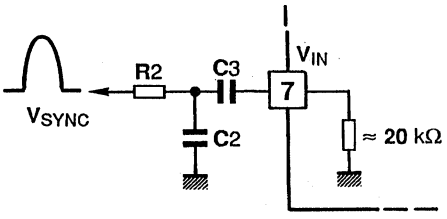
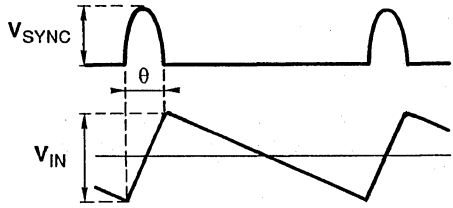
The TEA2019 has been particularly designed for video applications where the synchronization signal is obtained from the flyback signal generated during the line flyback.

Figure below illustrates the configuration arrangement used in such applications.

Figure 42





- In typical application : C3 = 47nF, C2 = 33nF
- R2 is calculated as a function of :

$$R2 \approx \frac{\theta}{C2 \log\left(\frac{V_{SYNC}}{V_{SYNC} - V_{IN}}\right)}$$

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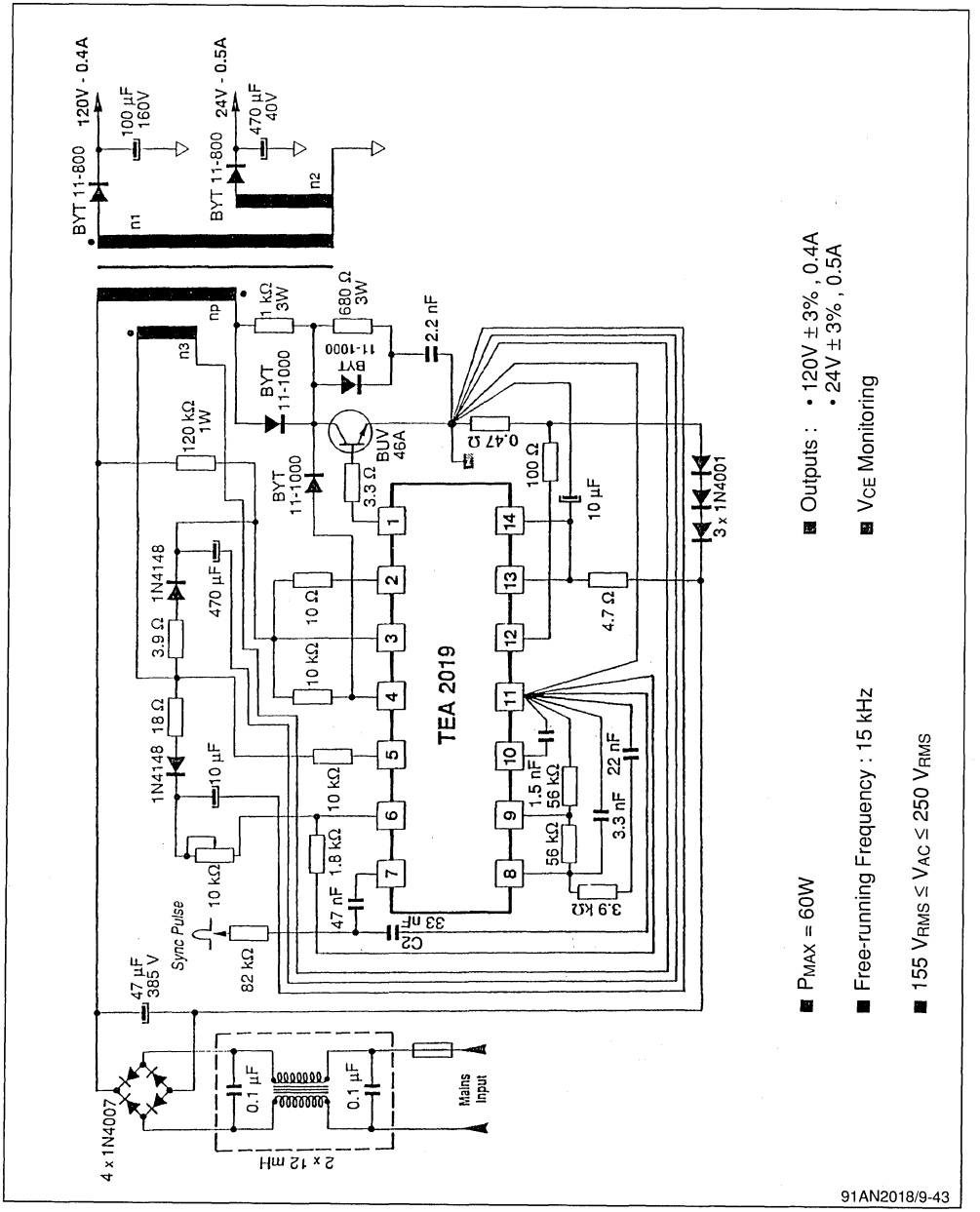
VI.4 - Applications

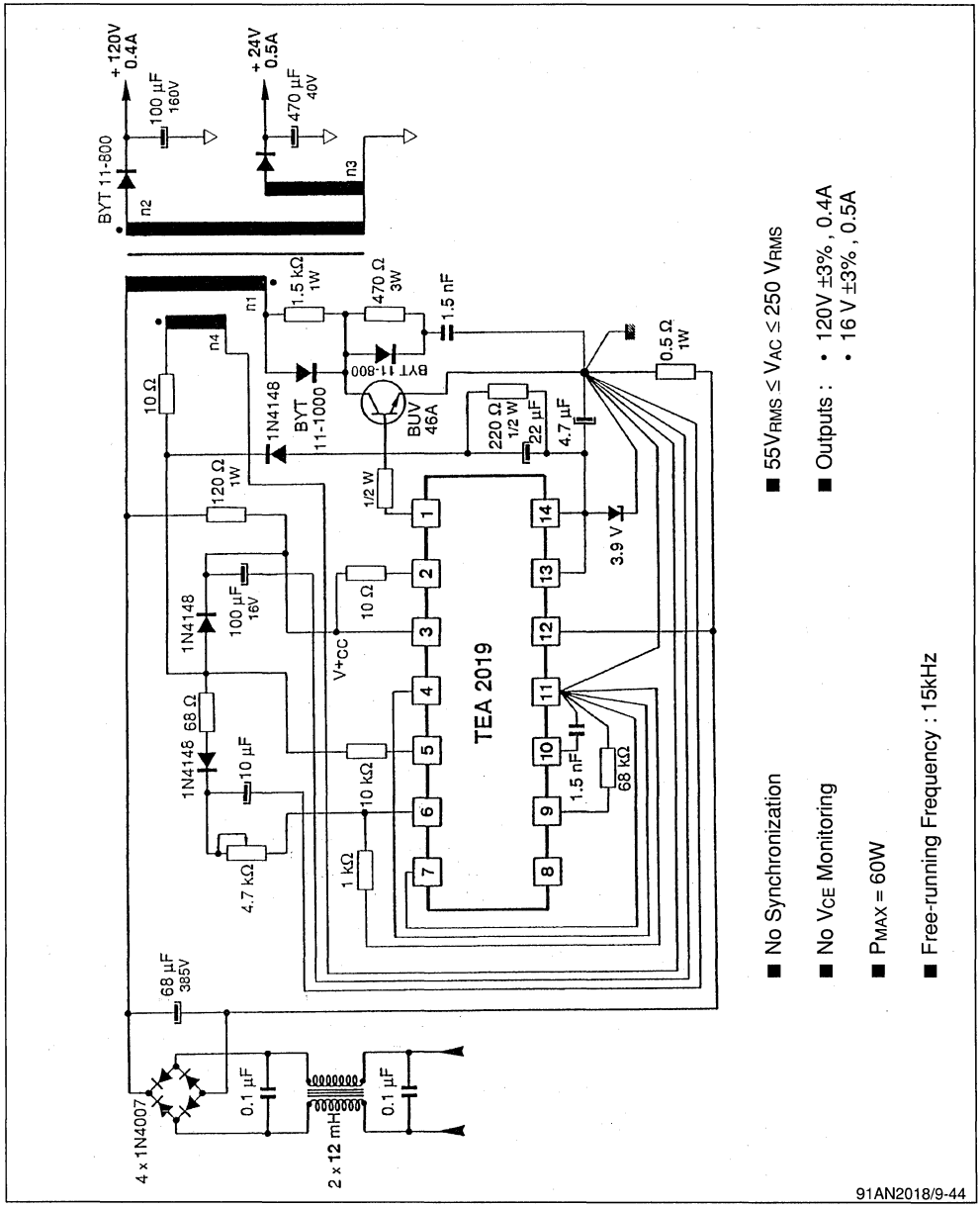
VI.4.1 - Typical application with synchronization

Figure 43



VI.4.2 - TEA2019 Configuration for power boosting

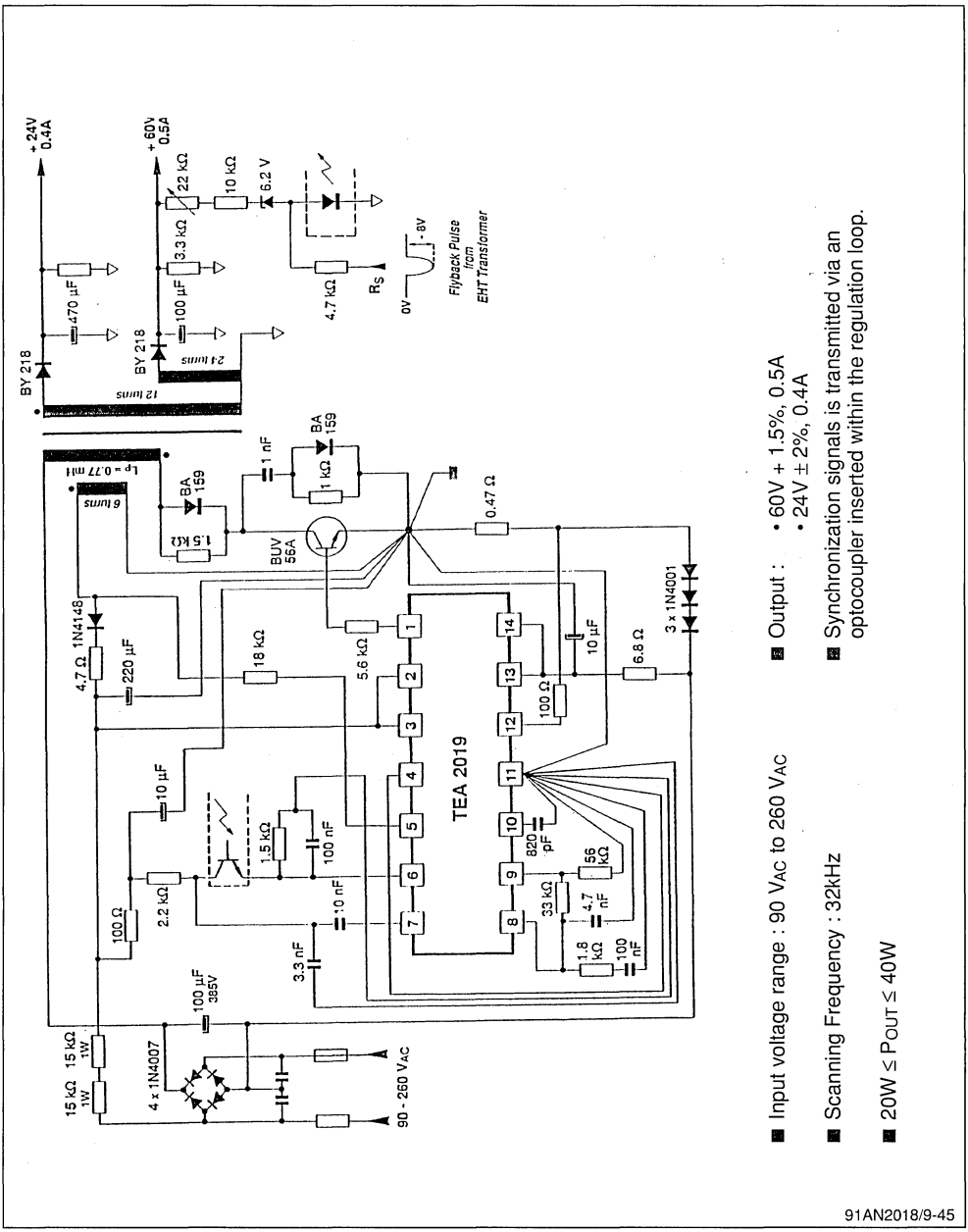
Figure 44



Comment : V- voltage is generated by the auxiliary winding.

VI.4.3 - Monitor application

Figure 45



VI.5 - Synchronization signal transmission

This signal is often generated from the secondary of the power supply, and therefore requires galvanic isolation.
Two solutions outlined below are both appropriate :

Figure 46 : Transmission through EHT transformer winding

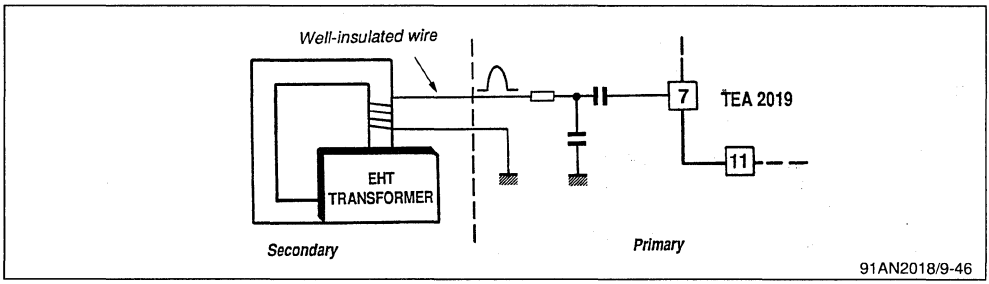
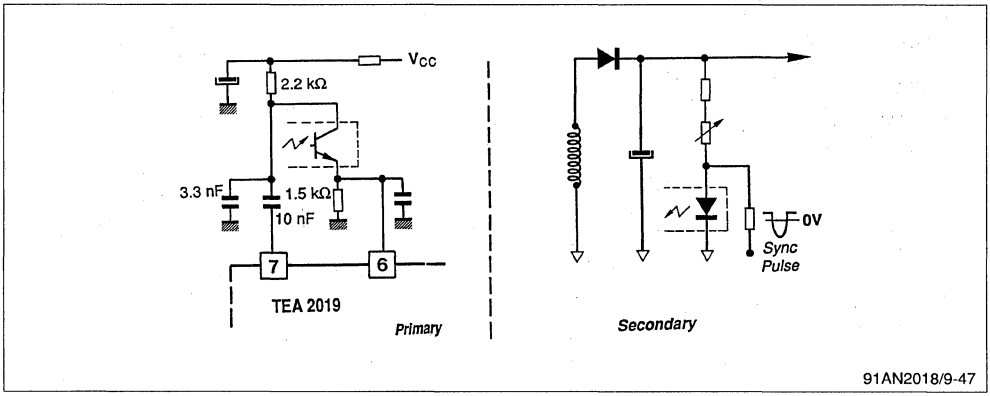


Figure 47 : Transmission via the Optocoupler of Regulation Loop

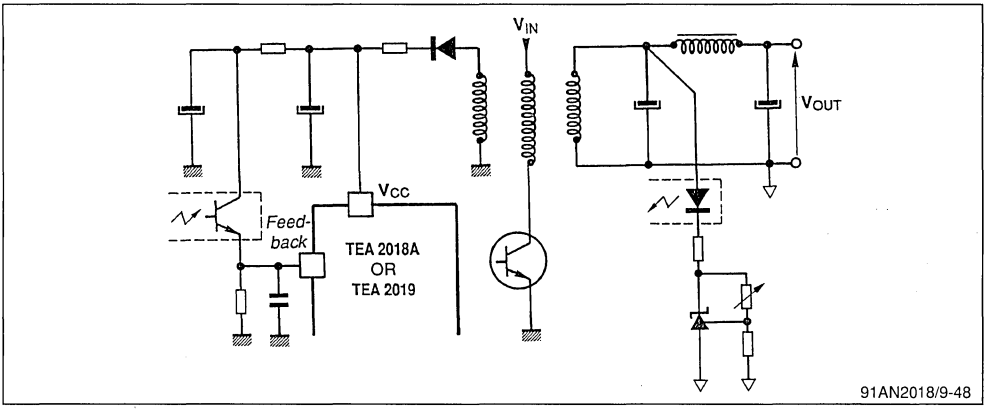


In this configuration, the optocoupler is used for the transmission of both, feed-back voltage and the synchronization signal.

VI.6 - APPLICATION VARIANTS

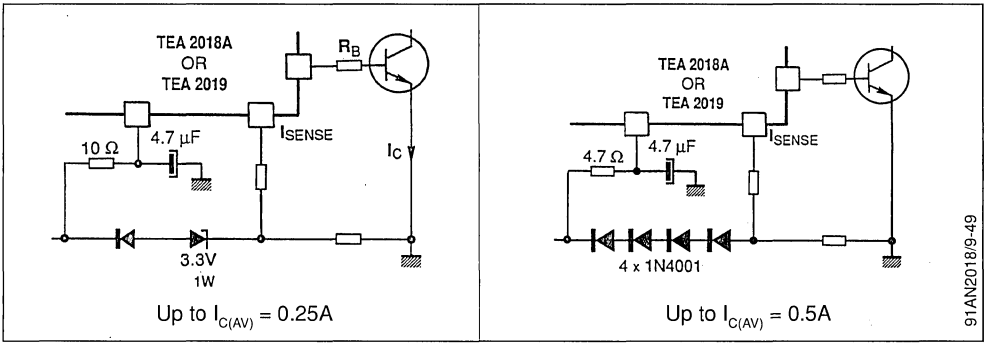
VI.6.1 - Regulation by optocoupler

Figure 48



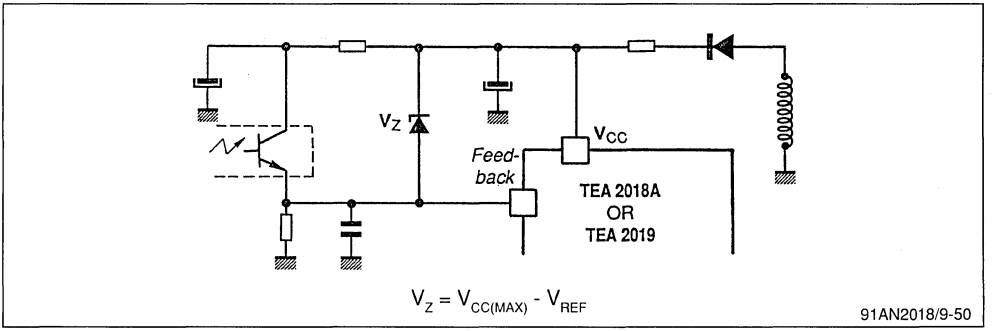
VI.6.2 - V⁻ Generator

Figure 49



VI.6.3 - Overvoltage protection

Figure 50



VI.6.4 - Application without demagnetization sensing

If the condition given below is satisfied, the demagnetization sensing function can be omitted without any risk of flux runaway in case of short-circuits or at start-up.

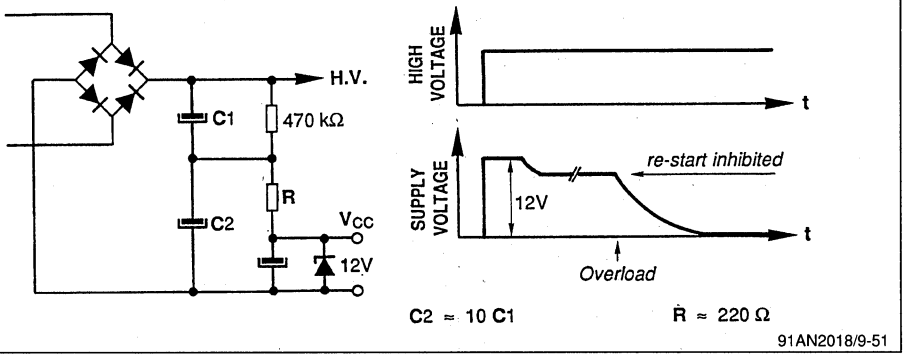
$$(V_{OUT} + V_{LOSS}) \leq V_{LOSS} \frac{V_{IN(MIN)}}{V_{IN(MAX)}} \cdot \frac{T - t_{ON(MIN)}}{t_{ON(MIN)}} \cdot \frac{T - t_{ON(L)}}{t_{ON(MAX)}}$$

Consequently, the damping network is no longer required and the "demagnetization sensing input" can be grounded.

VI.6.5 - Full shut-down at overload

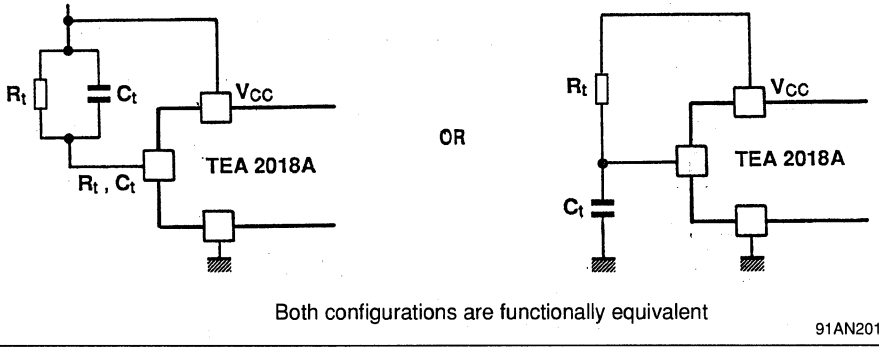
In case of overload, the arrangement depicted below will completely shut-down the power supply. To re-start the system, capacitor "C1" must be discharged.

Figure 51



VI.6.6 - Oscillator (TEA2018A only)

Figure 52



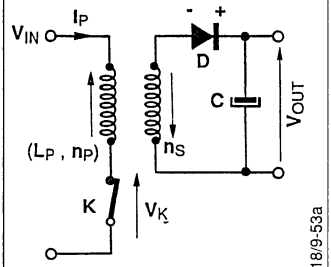
VII - FIXED FREQUENCY DISCONTINUOUS MODE FLYBACK

VII.1 - Fundamentals

An operating phase includes 3 phases :

- $0 \le t \le t_{ON}$: energy is stored within the primary inductance
- $t_{ON} \le t \le t_{dm}$: energy transfer toward the secondary winding
- $t_{dm} \le t \le T$: dead time, the transformer is fully demagnetized.

Figure 53

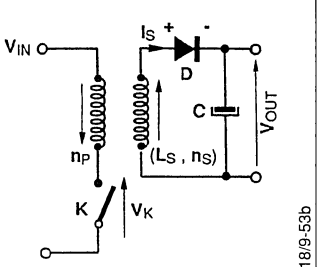


91AN2018/9-53a

$0 < t < t_{ON}$

- K : closed
- $V_K = 0$
- $\frac{dI_p}{dt} = \frac{V_{IN}}{L_p}$
- $V_D = V_{OUT} + \frac{ns}{np} V_{IN}$
- Energy stored during t_{ON}

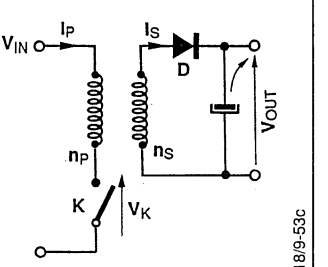
$W_{LP} = \frac{(V_{IN}\, t_{on})^2}{2L_p}$



91AN2018/9-53b

$t_{ON} < t < t_{dm}$

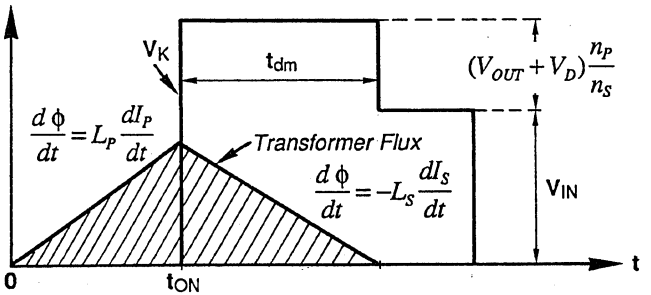
- K : open
- D : conducts
- $V_K = V_{IN} + (V_{out} + V_D)\frac{np}{ns}$
- $\frac{dI_s}{dt} = -\frac{(V_{OUT} + V_D)}{L_s}$
- $t_{dm} - t_{ON} = \frac{ns}{np} \cdot \frac{V_{IN} \cdot t_{ON}}{V_{OUT} + V_D}$



91AN2018/9-53c

$t_{dm} < t < T$

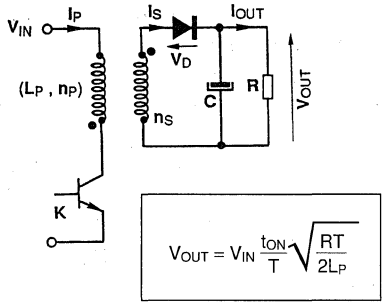
- $I_P = 0$, $I_S = 0$
- K : open
- D: blocked
- $V_K = V_{IN}$



91AN2018/9-53d

VII.2 - Transformer calculation and power semiconductors selection

Figure 54



91AN2018/9-53d

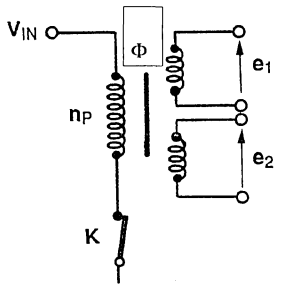
• Maximum operation duty cycle :	
(1) $\frac{t_{ON(L)}}{T} = \frac{V_R}{V_R + V_{IN(MIN)}}$	(2) $\frac{t_{ON(L)}}{T} = \frac{V_R}{V_R + \sqrt{2} \cdot V_{IN(MIN)}}$
• Maximum average primary current :	$I_{P(AV)MAX} = \frac{P_{OUT(MAX)}}{\eta} \cdot \frac{1}{V_{IN(MIN)}}$
• Maximum peak primary current :	$I_{P(PEAK)} = 2\, I_{P(AV)MAX} \cdot \frac{T}{t_{ON(L)}}$
• Primary inductance :	$L_P = V_{IN(MIN)} \cdot \frac{t_{ON(L)}}{I_{P(PEAK)}}$
• Maximum transformation ratio :	
(1) $\left(\frac{ns}{np}\right)_{(MAX)} = \frac{[V_{OUT} + V_D]\,[T - t_{ON(L)}]}{V_{IN(MIN)} \cdot t_{ON(L)}}$	(2) $\left(\frac{ns}{np}\right)_{(MAX)} = \frac{[V_{OUT} + V_D]\,[T - t_{ON(L)}]}{V_{IN(MIN)} \cdot t_{ON(L)} \cdot \sqrt{2}}$
• Peak rectifier current :	$I_{S(PEAK)} = 2\, I_{OUT} \frac{T}{(t_{dm} - t_{ON})}$
• Minimum power transfer at frequency "f" :	$P_{OUT(MIN)} = \eta \cdot \frac{[V_{IN(MAX)} \cdot t_{ON(MIN)}]^2}{2 \cdot L_P} \cdot f$

Where :
- (1) : without demagnetization monitoring
- (2) : with demagnetization monitoring
- $t_{ON(L)}$: Conduction time before current limitation

VII.3 - Multi-output flyback

All transformer windings undergo the same flux change of dϕ/dt. Regulation of any output causes regulation of all other windings.

Figure 55



$$\bullet \frac{e_1}{n_1} = \frac{d\Phi}{dt}$$

$$\bullet \frac{e_2}{n_2} = \frac{d\Phi}{dt}$$

$$\Rightarrow \quad \frac{e_1}{e_2} = \frac{n_1}{n_2}$$

91AN2018/9-55

AN AUTOMATIC LINE VOLTAGE SWITCHING CIRCUIT

VAJAPEYAM SUKUMAR
THIERRY CASTAGNET

ABSTRACT

The voltages found in line sockets around the world vary widely. Power supply designers have, most often, overcome this problem by the use of a doubler/bridge switch that can double the 120V nominal line and simply rectify the 240V nominal voltage.

A two device solution (comprising an integrated circuit and a customized triac) that will adapt the power supply to various line voltages around the world is described in the following paper. This circuit replaces a manual switch and could also open special markets. Other advantages of this integrated circuit solution are ease of circuit design, lower power dissipation, a smaller component count and additional safety features.

INTRODUCTION - THE DOUBLER/BRIDGE CIRCUIT.

AC line voltages the world over can be divided into two main categories :

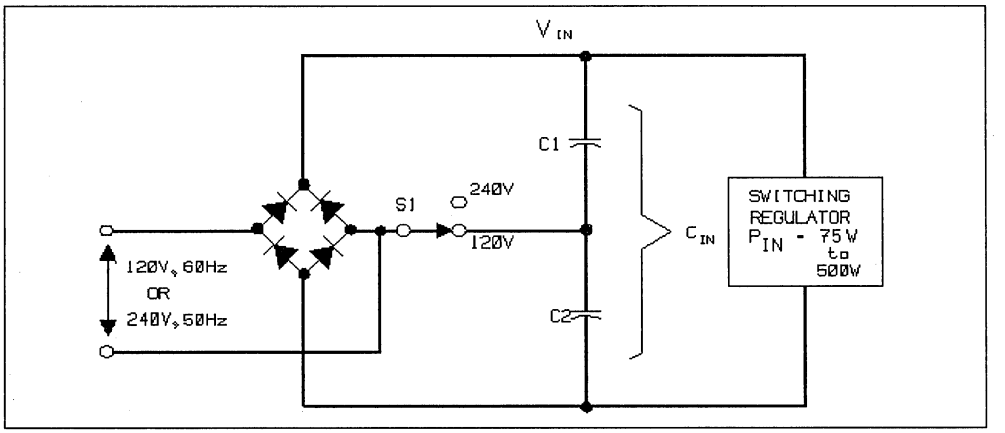
a)120V nominal, 60Hz systems. Electronic equipment is usually designed to run in the 90V - 132V range.

b) 240V nominal, 50Hz systems. Equipment has to be designed to run in the 187V-264V range.

A good reference for the various line voltages around the world is found in [1].

Power supplies built to run off these voltages have to be either wide range input or must use a doubler/bridge circuit. The disadvantage of the wide range input scheme - that all components have to meet worst case current and voltage requirements - makes such a solution popular only at less than 75W power levels. The popular doubler/bridge circuit is shown in Fig. 1. When the AC input voltage is 120V nom. (doubler mode) the switch S1 is closed. During the positive half cycle of the input voltage capacitor C1 is charged. During the negative half cycle of the input voltage, capacitor C2 is charged to the peak line voltage. When the line voltage is 240V nom. (bridge mode), the switch S1 is open and the circuit works like a conventional bridge rectifier.

Figure 1. Schematic Diagram of a Doubler/Bridge Circuit.

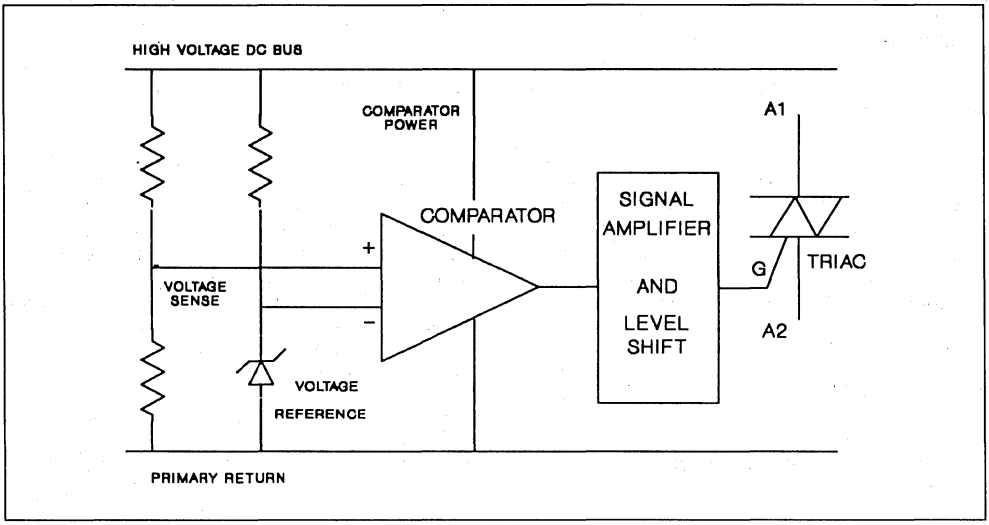


At power levels of over 500W, power factor correction circuits and three phase line input voltage circuits dominate. So, the automatic line voltage switching (AVS) circuit is used mostly in the 75W-500W power range.

The recent push to replace the mechanical switch S1 in Fig.1 with an automatic line voltage switching (AVS) circuit came from computer manufacturers. They found that the small additional cost of the AVS circuit is less than the costs of power supply failures incurred by inadvertently positioning the switch in the wrong position.

While many of the early AVS designs used relays, the triacs, with their superior reliability, small size and low cost are now more popular.

Figure 2. Discrete AVS Circuit Block Diagram



DISCRETE AUTOMATIC VOLTAGE SWITCHING CIRCUIT

Figure 2 shows a diagram of the various blocks comprising a discrete implementation of the AVS circuit. The line voltage selection circuit can be divided into three main functions:

1. Detection of peak line input voltage. Various schemes use resistive or capacitive dividers to measure the voltage across C1 and C2.

2. Comparison with a reference voltage that is generated with the help of a zener diode. A simple comparator can be implemented with two small signal transistors.

3. Drive for the triac. If the circuit is to be in the doubler mode, then the output signal of the comparator is boosted to provide the drive to turn the triac on. This interface circuitry can consist of a high voltage transistor and bias resistors.

DISCRETE VS INTEGRATED CIRCUIT AVS.

An IC based AVS circuit should be designed to overcome the disadvantages of the discrete solution that are listed below.

1. Power Dissipation.

This is critical because the entire supply current necessary for the operation of the AVS circuit comes from the high voltage bus. Every milliampere of current saved in the sensing, comparison and drive circuitry increases the efficiency of the entire system.

$$P_D(AVS)=k^*(V_{AC})^2. \quad (1)$$

About 80% of the power lost in the AVS scheme

is in the gate drive to the triac. This means that a sensitive gate triac is the best candidate for the switch S1 in Figure 1.

Discrete AVS solutions usually use between 5W and 12W.

2. Immunity to Input Line Voltage Transients.

Most power supplies today are designed to meet IEEE 587 or similar line transient specifications. We must choose a triac that withstands these transient voltages without any triggering. So we have to make a compromise between low gate drive requirements (I_{GT}) and good static dv/dt immunity. The gate drive circuit of the triac must also be designed to reduce any parasitic voltages at the gate. The gate non- trigger voltage (V_{GD}) of most triacs is about 0.2V.

3. Effect of Line Sags and Surges.

Line voltages are generally considered to vary about +/- 10% from their nominal values. The 120V nominal can be as high as 132V and the 208V nom. can fall to 187V. Between 132Vac and 187Vac, there exists a window, in which we have to design the threshold voltage of the comparator in Fig. 2. Additional ('strife', etc.) test requirements can reduce this window to a smaller 140V to 170V. An analysis of worst case component tolerances is critical in AVS design.

Ultimately, however, there will always be line voltage waveforms that will fool an automatic voltage selection scheme. One can think of situations where, say, a large motor will pull the line voltage down below the threshold voltage during startup. A good AVS system will monitor the line voltage and protect the power supply . In some applications, the bridge mode (240V mode) is considered the fail safe mode and if the unit starts off in the bridge mode, it should not be able to change modes till the power is recycled.

SGS-THOMSON AVS10 SOLUTION.

We at SGS-THOMSON studied the possibility of an integrated circuit solution for this application. The cost constraints ruled out any exotic single chip solutions and forced us to opt for an 8 pin DIP IC for sensing and a TO-220 triac as the power switch. This IC+triac solution, called AVS10, also offers optimal protection against noise.

In order to maximize the design flexibility and reduce turn around time, we chose a semi-custom solution called ANACA. A 12V CMOS ANACA process used offers mixed analog/digital standard cell capability.

OPERATION OF THE AVS10 CIRCUIT

A typical application diagram for the AVS10 in a power supply is shown in Fig. 3.

Figure 3. AVS10 Application Schematic Diagram

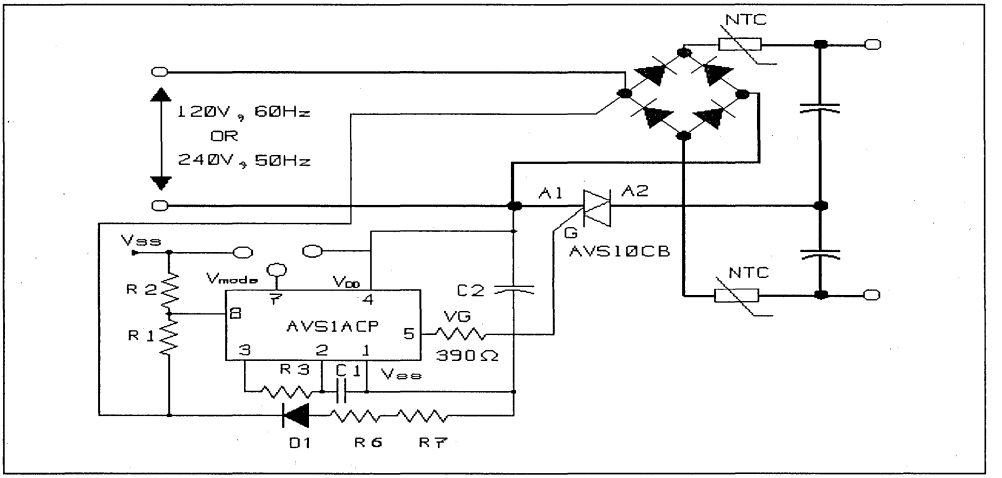
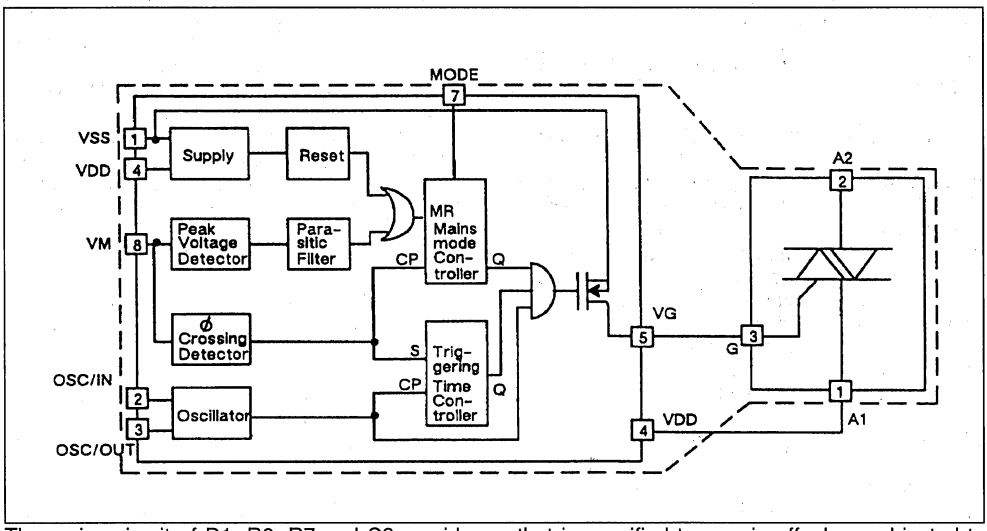


Figure 4. AVS10 Block Diagram



The series circuit of D1, R6, R7 and C2 provide power for the chip. Pin 1, Vss, is a shunt regulator that provides a -9V (nom.) output. R1 and R2 are resistive divider precision resistors that are a measure of the input line. The voltage at Pin 8 varies with the input line. Thus the voltage at Pin 8 is not only a measure of the peak input voltage, but it can also sense line voltage zero crossing. Pins 2 and 3 are inputs to an oscillator. The resistor R3 and C1 set the oscillator frequency. Pin 5 drives the gate of the triac through a 390Ω resistor. Pin 7 offers the user a choice of two different modes of operation. The block diagram of the IC is given in Fig. 4.

1. Decreased Power Dissipation.

Decreased power dissipation is an important advantage of the AVS10. While most discrete AVS schemes need 5W to 12W of power, the AVS10 uses about 2W. This performance is thanks to an innovative gate triggering scheme (Patent Pending). The gate current is made up of a pulse train that has a typical duration of around 23µs (45kHz+/-5%). The duty cycle of the pulses is typically 10%. The values of R2 and C3 in Fig. 3 are chosen to give us the pulse frequency.

2. Immunity To Voltage Transients.

The triac of the AVS10 is a sensitive gate triac that is specified to remain off when subjected to dv/dt of 50V/µs. Circuit layout is critical in preventing false dv/dt turn on of the triac [2]. The IC of the AVS10 circuit has a built in digital filter that suppresses the effect of all spikes of less than 200µs duration.

3. Operating In The Failsafe Mode. $V_{mode} = V_{SS}$.

The mode pin on the AVS10 IC, Pin 7 determines the behavior of the circuit if it is turned on into a line surge/sag situation. If Pin 7 is tied to V_{SS} (Pin 1), the AVS10 circuit is in a failsafe mode. This means that if the device is turned into a bridge mode, it will remain in the bridge mode, even if the voltage were to suddenly dip into the 110V range.

4. Operation In Reactive Mode. $V_{mode} = V_{DD}$.

If Pin 7, the mode pin, is tied to V_{DD}, then the device will switch between bridge and doubler modes if the input voltage changes. If the 110V input changes to 220V, then the AVS10 turns the triac off by the next mains cycle. If the 220V input falls to 110V, the AVS10 circuit has a validation period of 8 mains cycles (when it verifies that the voltage is still at 110V) after which the triac turns on. Thus, safety features are built into the AVS10 circuit. Typical timing diagrams for the two modes are given in Figs. 5 and 6.

Figure 6. Timing diagram - $V_{mode} = V_{SS}$

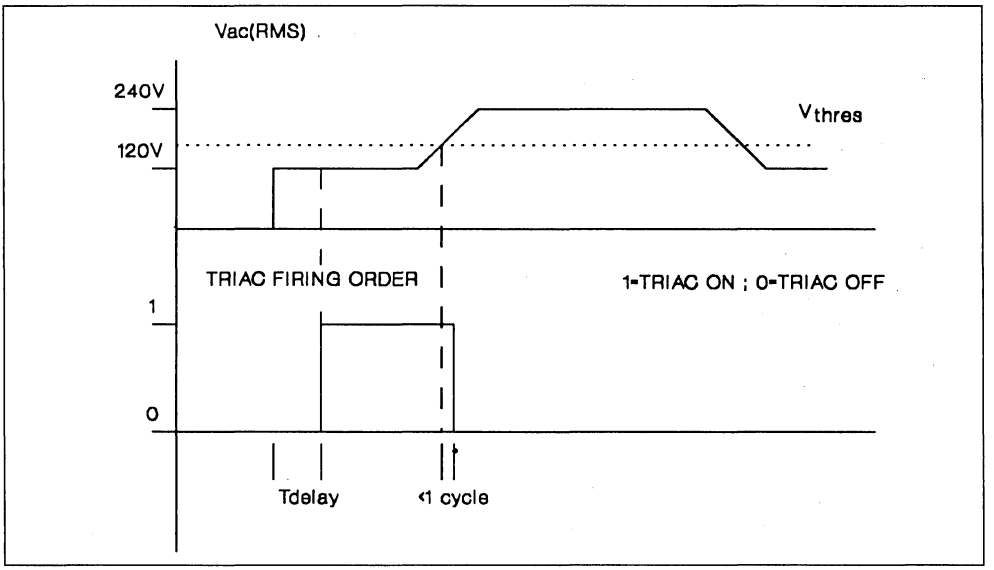
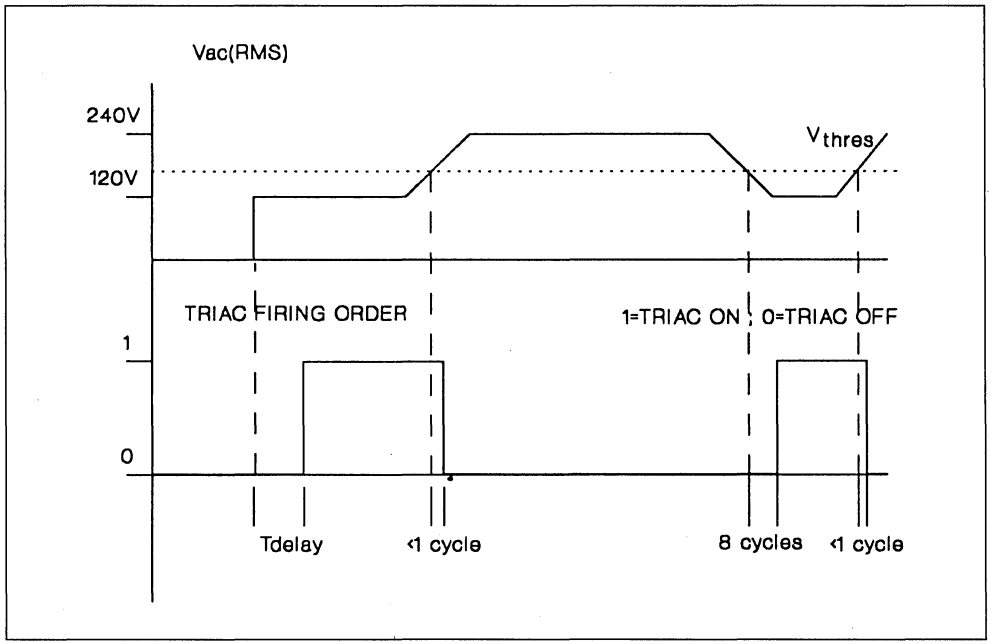


Figure 5. Timing Diagram - $V_{mode} = V_{dd}$



A detailed account of how to set the input voltage threshold is found in [2].

5. Additional Safety Features.

Additional steps are taken to enhance the safety of design include starting up always into the bridge mode. There is a delay of around 250 ms at start up before the AVS10 goes into the doubler mode.

Hysteresis is also built into the comparator to prevent small line voltage variations from causing toggling between bridge and doubler modes. Only a voltage variation of over 10% of the line voltage can cause the AVS10 to change modes.

CONCLUSION

This paper describes an efficient way of implementing an automatic doubler/bridge circuit. The primary use of this circuit is in 75W to 500W SMPS. Other innovative uses are possible. One example would be industrial motor drives which can be designed to accept either 120V line-to-neutral or 208V line-to-line input.

The main advantages of the AVS10 solution are:

1. High Efficiency. Losses are just 2W vs. 5W-10W for discrete schemes.

2. Safety. Uses digital spike suppression, hysteresis, validation of range, a failsafe mode and good control over the triac triggering.

3. Space Optimization., small supply resistor. Good reliability.

4. Ease of Use. Eliminates manual line selection errors.

5. Suitable solution for various power range:
   AVS10 up to 300W
   AVS12 up to 500W.

REFERENCES.

[1] PSMA Handbook of Standardized Terminology for the Power Sources Industry.
Appendix C.

[2] SGS-THOMSON technical note 'How To Use The AVS Kit'.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

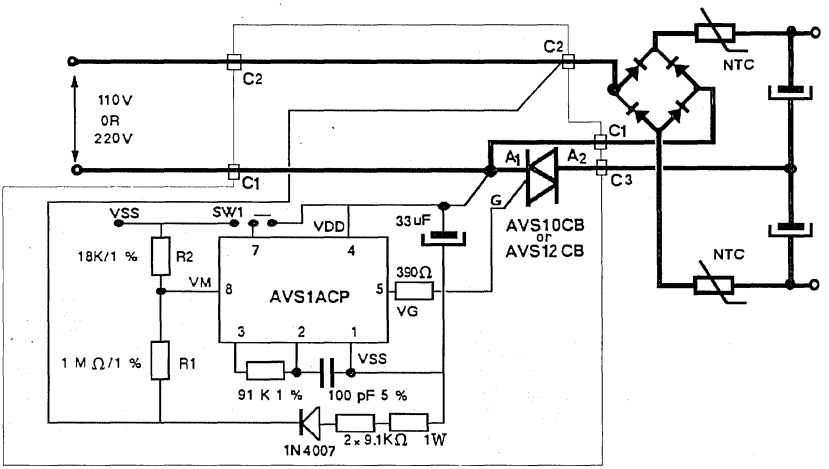
HOW TO USE THE AVS KIT

PRELIMINARY NOTE

I DESCRIPTION OF THE AVS KIT :

The AVS10, or AVS12, is an automatic mains selector to be used in on line SMP supply with Power up to 500W. It is made of two devices.

This switch modifies automatically the structure of the input diodes bridge in order to keep a same DC voltage range.



The AVS is compatible with 50 and 60 Hz mains frequency and operates on two mains voltage ranges :

- On range I (110 V_{RMS}) the AC voltage varies from 88 to 132 V and the triac is ON : the bridge operates as voltage doubling circuit.

- On range II (220 V_{RMS}) the AC voltage varies from 176 V to 276 V and the triac is OFF : the circuit operates as full wave bridge.

II PERFORMANCE OF THE AVS :

The control of the switch is made by the comparison of the mains voltage (VM on pin 8) with internal threshold voltages (VTH and VH on pin 8).

When mains voltage increases from range I to range II the triac conduction is completly stopped before one mains period because VM > VTH.

When mains voltage drops from range II to range I VM becomes lower than VTH - VH. There are two options (V mode on pin 7) :

- V mode = VDD ; the triac triggering is valided 8 mains periods after power on reset.

- V mode = VSS ; the triac control remains locked to range II until circuit reset.

III USE OF THE AVS :

Calculation of the oscillator :

The oscillator frequency is determined by the mains frequency (50 and 60 Hz) and the gate control : its required value must be 45 KHz ± 5%; so the value of components is :

C = 100 pF/5%
R = 91 KOhms/1%

The frequency control is made on pin 3.

Adjustement of the mains mode change :

The measure of the mains voltage is made by a detection of the peak value.
The change of mains range is made by adjustement of resistor bridge and we advice :

800 kOhms < R1 + R2 < 2 mOhms

Calculation of the change from range I to range II (on pin 8) :

$[VTH . (R1 + R2)]/(R2 . \sqrt{2}) + Vreg / \sqrt{2}$ = max.RMS voltage on Range I

Vreg typ = - 9 V and VTH typ = 4.25 V

Calculation of the change from Range II to range I :

$[(VTH - VH) . (R1 + R2)/R2 . \sqrt{2}] + Vreg / \sqrt{2}$ = min . RMS voltage on range II

Vreg typ = - 9 V and VH typ = 0.4 V

Performance of the power on reset :

The power on reset permits the charge of the bulk capacitors of the SMP supply through soft start circuit.
The triac triggering is valided (on range I) after the validation of power on reset (charge of supply capacitor C) and a temporization of 8 mains periods.

T delay = delay time between power on and triac triggering

$Td = 0,89 . Vreg . R . C/[(V_{RMS} . \sqrt{2}/\pi) - R . Iss] + 8/f$

f = mains frequency

R = supply resistor = 18 kOhms

C = supply capacitor = 33 µF

V_{RMS} = mains voltage

Iss = quiescent supply current of AVS

Supply of the controller :

The structure of the supply regulator is a shunt regulator and its current must be lower than Iss max = 30 mA.

In order to have a good behavior of the circuit against mains voltage spikes the pin 4 (VDD) of the integrated circuit has to be connected straightly with the A1 of the triac. In same way the supply diode rectifier and R1 have to be connected to the diode bridge (see typical application diagram).

Triac control :

Between pin 5 and triac gate there is a resistor in order to limit the gate current; its value is given by the controller supply and triac ; the required value is 390 Ohms (5%).

Thermal rating of triac :

The knowlegde of the maximum triac current I_{TM} and the current pulse width tp in worst case conditions allows to calculate the losses, PT dissipated by the triac :

I_{TRM} = R_{MS} triac current
$= I_{TM} \times \sqrt{tp} \times \sqrt{f}$

$PT = 4 . tp . f . I_{TM} . V_{TO}/\pi + rt . tp . f . (I_{TM}^2)$

for AVS10CB :

V_{TO} = threshold voltage of triac = 1.1 V
rt = on state triac resistance = 49 mohms

for AVS12CB:

VTO = 1V
rt = 45 mOhms

The figure 1 of DC general characteristics of triac gives these losses PT versus I_{TRMS} for this application. The figure 2 allows to calculate the external heatsink R_{TH} versus PT and Tamb when Tj = 110C

$Tj - Tc = R_{TH}$ j-c AC . PT
$Tc - Tamb = R_{TH} . PT$

Example on AVS10 :

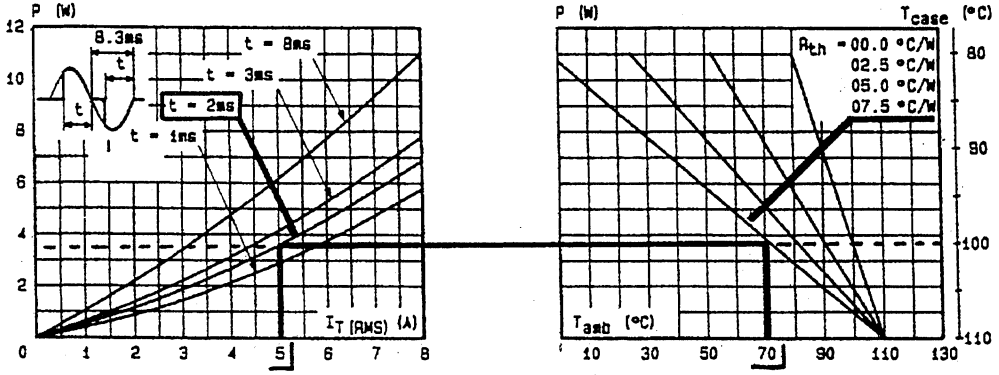


Figure 1 and Figure 2 of AVS10 Datasheet

if tp = 2ms and I_{TRMS} = 5A

- PT = 3.8W

- Tc = 100°C if Tj = 110°C

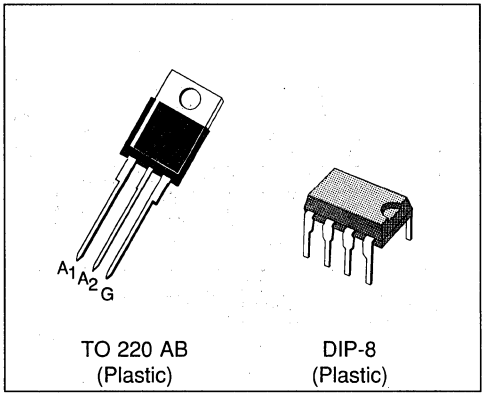
- R_{TH} = 7.5 °C/W if Tj = 110°C and Tamb < 70°C

Annex : AVS demo board

COMPONENT LIST FOR AVS10.

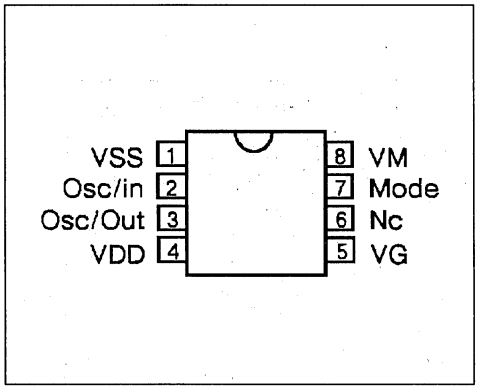
DESIGNATION	QTE	REFERENCE	OBSERVATIONS	MARQUE
PRINTED CIRCUIT	1	4751		
RESISTANCE	1	R1	1 MOhms 1%	
RESISTANCE	1	R2	18 KOhms 1%	
RESISTANCE	1	R3	91 KOhms 1%	
RESISTANCE	2	R4	9.1 KOhms 1W	
RESISTANCE	1	R6	390 Ohms 5%	
DIODE	1	D1	1N4007	
CONDENSATOR	1	C1	100 pF 5%	
CONDENSATOR	1	C2	33µF 16V RADIAL	
TRIAC	1	IC2	AVS10CB / AVS12CB	SGS-THOMSON
INTEGRATED CIRCUIT	1	IC1	AVS1ACP08	SGS-THOMSON
SUPPORT	1		CI 8 PINS	
INVERTER	1	SW1	MINIDIP	
SOCKET	1	SL 3W	3 PINS	WEIDMULLER
PLUG	1	BL3	3 PINS	WEIDMULLER

Products PIN out

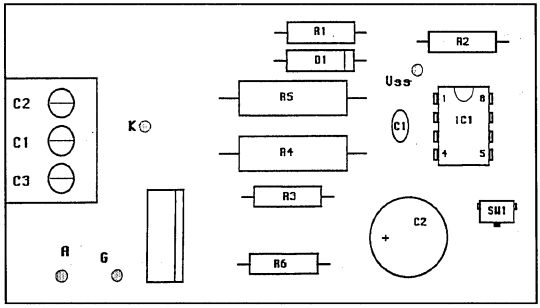


TO 220 AB
(Plastic)

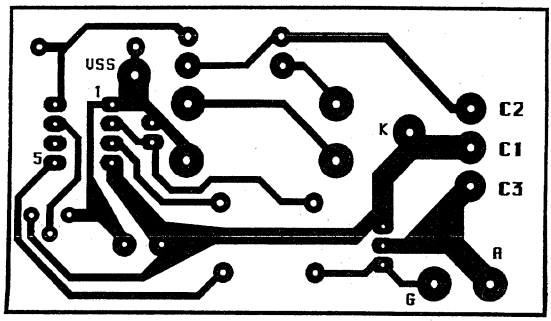
DIP-8
(Plastic)



Components layout



Printed circuit layout (Copper side) : 1/1 scale



POWER SUPPLY DESIGN BASICS

by P. ANTONIAZZI

Aimed at system designers whose interest focusses on other fields, this note reviews the basic power supply design knowhow assumed in the rest of the book.

In mains-supplied electronic systems the AC input voltage must be converted into a DC voltage with the right value and degree of stabilization.

Figures 1 and 2 show the simplest rectifier circuits. In these basic configurations the peak voltage across the load is equal to the peak value of the AC voltage supplied by the transformer's secondary winding. For most applications the output ripple produced by these circuits is too high. However, for some applications - driving small motors or lamps, for example - they are satisfactory.

If a filter capacitor is added after the rectifier diodes the output voltage waveform is improved considerably. Figures 3 and 4 show two classic circuits commonly used to obtain continuous voltages starting from an alternating voltage. The Figure 3 circuit uses a center-tapped transformer with two rectifier diodes while the Figure 4 circuit uses a simple transformer and four rectifier diodes.

Figure 1 : Basic Half Wave Rectifier Circuit.

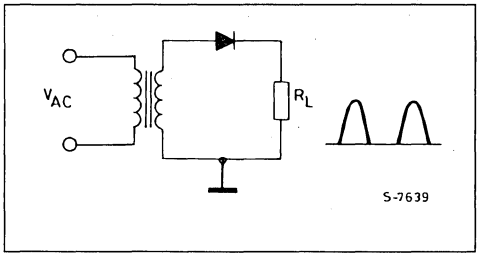


Figure 2 : Full Wave Rectifier Wich uses a Center-tapped Transformer.

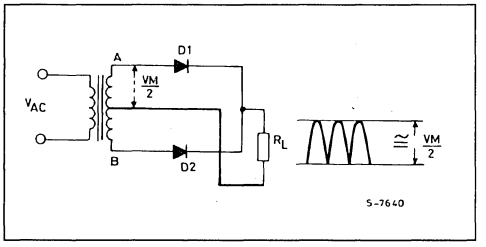


Figure 3 : Full Wave Rectified Output From the Transformer/rectifier Combination is filtered by C1.

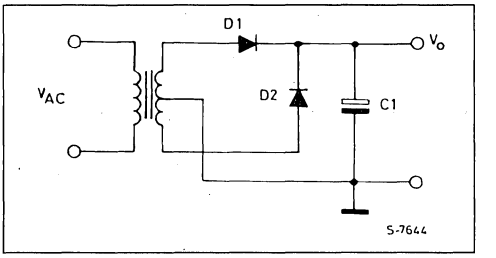


Figure 4 : This Circuit Performs Identically to that Shown in Figure 3.

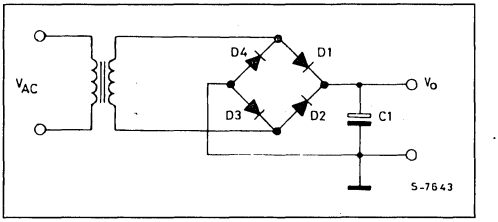


Figure 5 shows the continuous voltage curve obtained by adding a filter capacitor to the Figure 1 circuit. The section b-c is a straight line. During this time it is the filter capacitor that supplies the load current. The slope of this line increases as the current increases, bringing point c lower. Consequently the diode conduction time (c-d) increases, increasing ripple. With zero load current the DC output voltage is equal to the peak value of the rectified AC voltage.

Figure 6 shows how to obtain positive and negative outputs referred to a common ground. Useful design data for this circuit is given in figures 7, 8 and 9. In particular, the curves shown in Figure 7 are helpful in determining the voltage ripple for a given load current and filter capacitor value. The value of the voltage ripple obtained is directly proportional to the load current and inversely proportional to the filter capacitor value.

Figure 5 : Output Waveforms from the Half-wave Rectifier Filter.

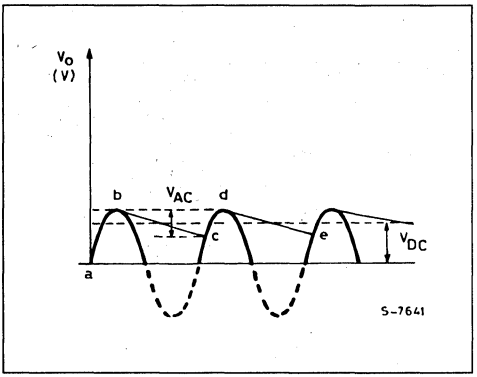


Figure 6 : Full-wave Split Supply Rectifier.

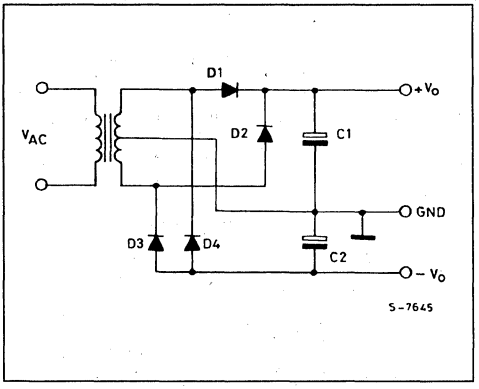


Figure 7 : Ripple Voltage vs. Filter Capacitor Value (full-wave Rectifier).

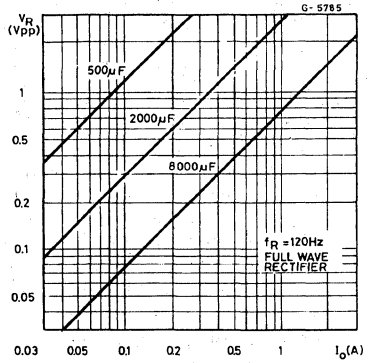


Figure 8 : DC to Peak Ratio for Half Wave rectifiers.

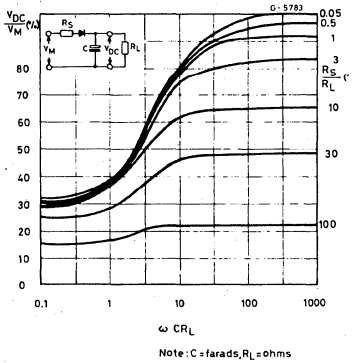


Figure 9 : DC to Peak Ratio for Full-wave Rectifiers.

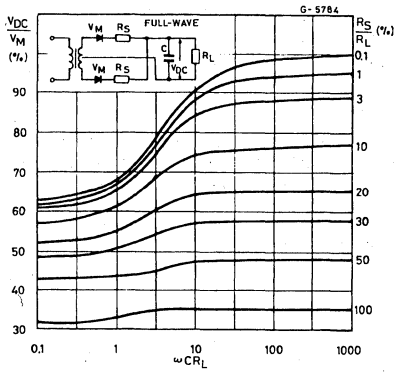


Figure 10 : DC Characteristics of a 50 VA Non-regulated Supply.

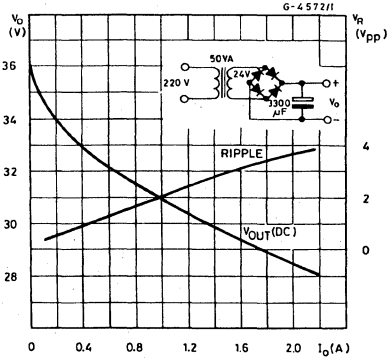


Table 1.

Mains (220V)	Secondary Voltage	DC Output Voltage (V_O)		
		I_O = 0	I_O = 0.1A	I_O = 1A
+ 20%	28.8V	43.2V	42V	37.5V
+ 15%	27.6V	41.4V	40.3V	35.8V
+ 10%	26.4V	39.6V	38.5V	34.2V
	24V	36.2V	35V	31V
− 10%	21.6V	32.4V	31.5V	27.8V
− 15%	20.4V	30.6V	29.8V	26V
− 20%	19.2V	28.8V	28V	24.3V

The performance of a supply commonly used in consumer applications - in audio amplifiers, for example - is described in figure 10 and table 1.

When a low ripple voltage is required an LC filter network may be used. The effect on the output voltage of this addition is shown in figure 11. As figure 11 shows, the residual ripple can be reduced by 40 dB. But often the inductor is costly and bulky.

Often the degree of stability provided by the circuits described above is insufficient and a stabilizer circuit is needed. Figure 12 shows the simplest solution and is satisfactory for loads of up to about 50mA. This circuit is often used as a reference voltage to apply to the base of a transistor of to the input of an op amp to obtain higher output current.

The simplest example of a series regulator is shown in Figure 13. In this circuit the transistor is connected as a voltage follower and the output voltage is about 600 - 700mV lower than the zener voltage. The resistor R must be dimensioned so that the zener is correctly biased and that sufficient base current is supplied to the base of Q1.

For high load currents the base current of Q1 is no longer negligible. To avoid that the current in the zener drops to the point where effective regulation is not possible a darlington may be used in place of the transistor.

When better performance is required the op amp circuit shown in Figure 14 is recommended. In this circuit the output voltage is equal to the reference voltage applied to the input of the op amp. With a suitable output buffer higher currents can be obtained.

The output voltage of the Figure 14 circuit can be varied by adding a variable divider in parallel with the zener diode and with its wiper connected to the op amp's input.

The design of stabilized supplies has been simplified dramatically by the introduction of voltage regulator ICs such as the L78xx and L79xx - three-terminal series regulators which provide a very stable output and include current limiter and thermal protection functions. Figures 16, 17 and 18 show how these circuits are used. Refer to the datasheets for more information.

Figure 11 : Ripple Reduction Produced by a Single Section Inductance-capacitance Filter.

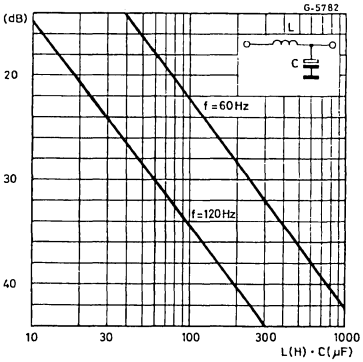


Figure 12 : Basic Zener Regulator Circuit.

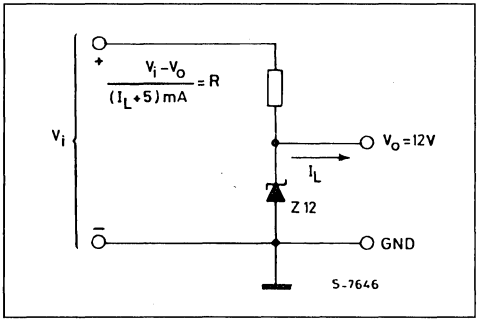


Figure 13 : The Series Pass Zener-based Regulator Circuit can Supply Load Currents up to about 100mA.

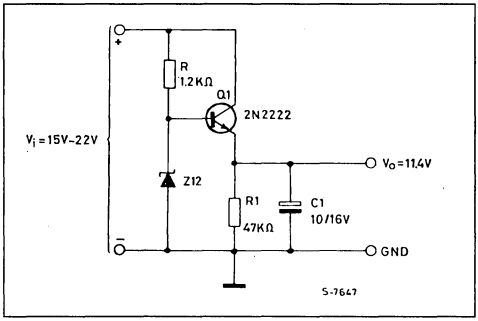


Figure 14 : The Op-amp-based Regulator can Supply 100mA with Excellent Regulation.

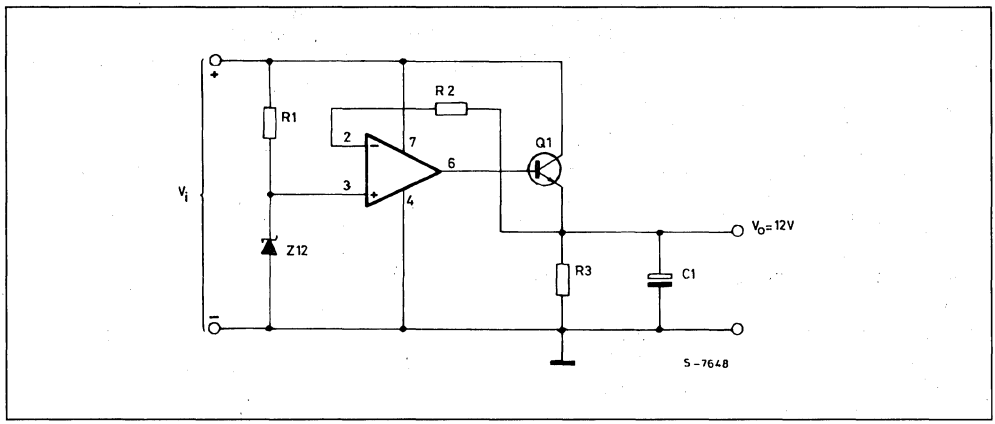


Figure 15 : Zener Regulator Circuit Modified for Low-noise Output.

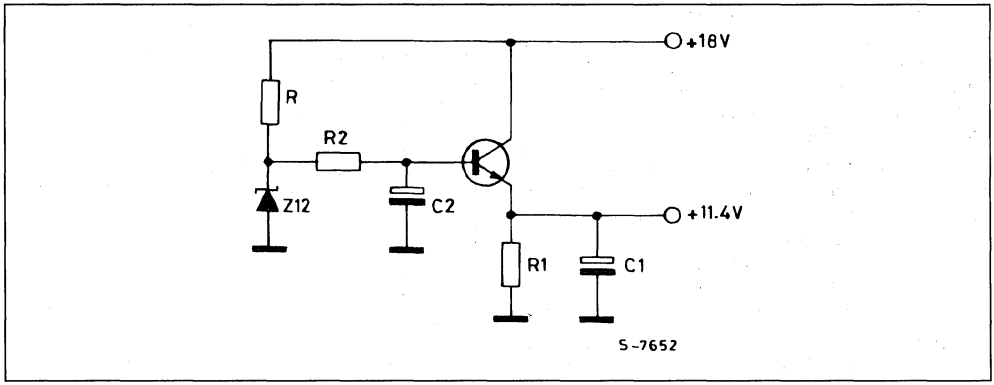


Figure 16 : A Three Terminal 1A Positive Regulator Circuit is very Simple and Performs very Well.

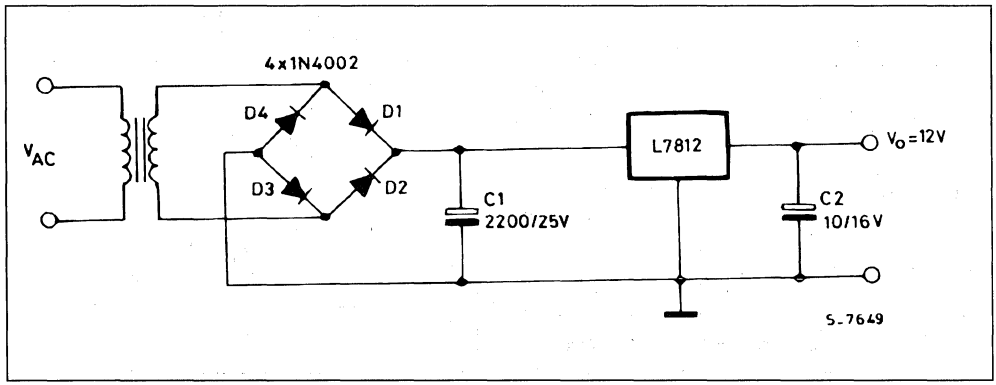


Figure 17 : A Three Terminal 1A Negative Voltage Regulator.

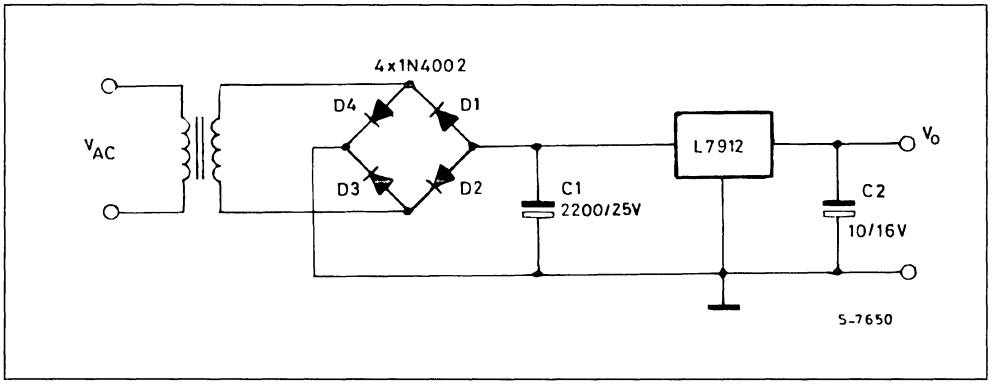
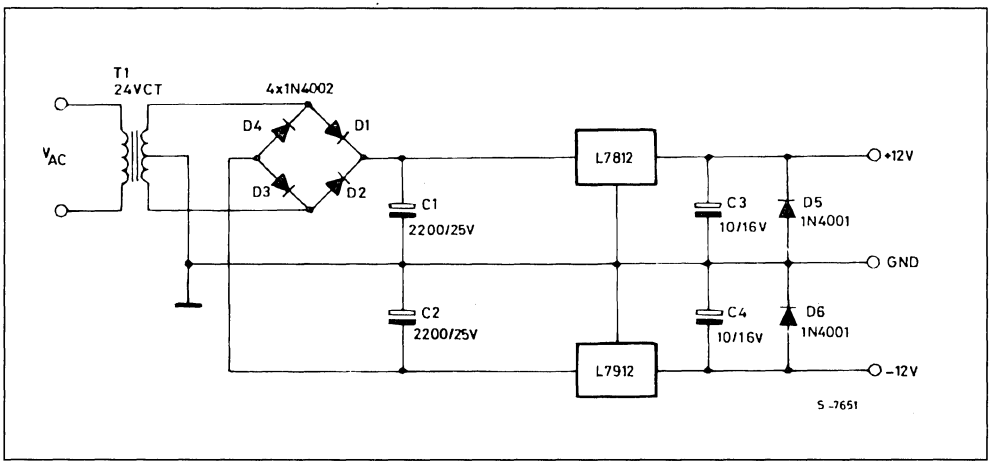


Figure 18 : Complete ± 12V – 1A Split Supply Regulator Circuit.



VERY LOW DROP REGULATORS ENHANCE SUPPLY PERFORMANCE

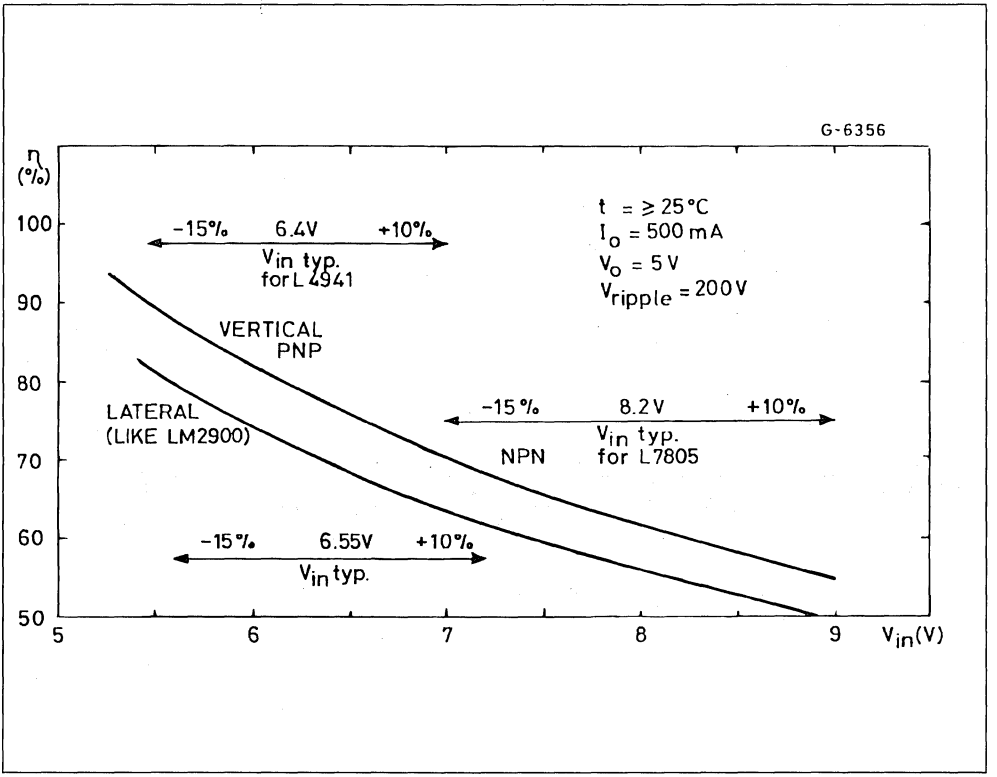
By Paolo ANTONIAZZI and Arturo WOLFSGRUBER

Standard three-terminal voltage regulator ICs use an NPN transistor as the series pass element, so the input-output voltage drop is 1.5V-2V. Low dropout regulators using lateral PNP pass transistors have been available for several years, but a lateral PNP transistor has low gain, so the base current is necessarily high, and a low f_T, so the settling time is poor. Moreover, for stability a large output capacitor is needed.

Applying a new bipolar technology (see APPENDIX : Technology Is The Key) SGS-THOMSON has developed two 5V low drop voltage regulators that use a new vertical PNP transistor structure to obtain low dropout and low quiescent current.

Type L4940 delivers up to 1.5A and offers an input-output voltage drop of 700mV at the full 1.5A output current. A 1A version, type L4941, has an input-output drop of 450mV at 1A (100mV at 0.1A). Both types have a quiescent current of 15mA at 1A (4mA with no load). Consequently these devices dissipates less power, improving the efficiency of any supply system (figure 1).

Figure 1 : A voltage regulator using vertical isolated PNP transistor is more efficient than regulators with NPN pass transistors because the drop out is lower. And it is more efficient than a regulator having a lateral PNP pass transistor because the quiescent current is lower.



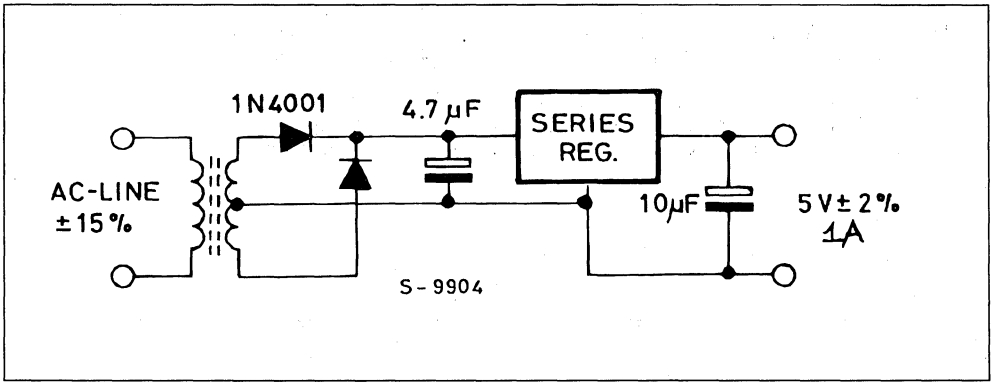
Compared to other "low drop" regulator the L4940 and L4941 have other advantages : regulation performance is guaranteed right down to the minimum input voltage and the device is stable even without an output capacitor. Additionally, a special circuit limits the quiescent current for input voltages from 3V to 5V, typically high for low drop regulators because of the saturation of the series regulator.

The two application areas which benefit the most from second generation low drop regulators like the L4940 and L4941 are post regulation and battery supplies. However, the device brings cost savings in any three-terminal regulator application.

LOW DISSIPATION REDUCES SIZE, WEIGHT & COST

In simple series regulator applications the low dissipation of the L4940/1 reduces the size and weight of the mains transformer, heatsink and printed circuit board. A comparison between equivalent 5V/1A circuits using the L4941 and a standard L7805 regulator (figure 2) shows that the L4941 solution is not only more compact and lighter, it also costs less since the difference in costs between an L4941 and an L7805 is less than the cost saving.

Figure 2 : In simple series regulator applications the L4941 can replace standard three-terminal regulators like the L7805, reducing size, weight and cost. Heat dissipation is reduced, too.



COMPARISON BETWEEN L7805 AND L4941

L4941			L7805	
Component	**Value**	**Cost***	**Value**	**Cost***
Transformer	220V/7.5V 9.4VA	$4.8	220V/8.6V 11VA	$5.4
Diodes	2x1N4001	$0.1	2x1N4001	$0.1
Capacitors	4.7µF 10V 10µF	$0.5 $0.1	4.7µF 16V 100n	$0.75 $0.08
Heatsink	20°C/W	$0.2	10°C/W	$0.3
PC Area	20cm^2	$0.27	26cm^2	$0.35
		$5.97		$6.98

The L4941 solution, excluding the cost of the IC, is thus $1 cheaper. Moreover it is lighter, more compact and dissipates 1.6W less.

* guide price for 1000 pieces.

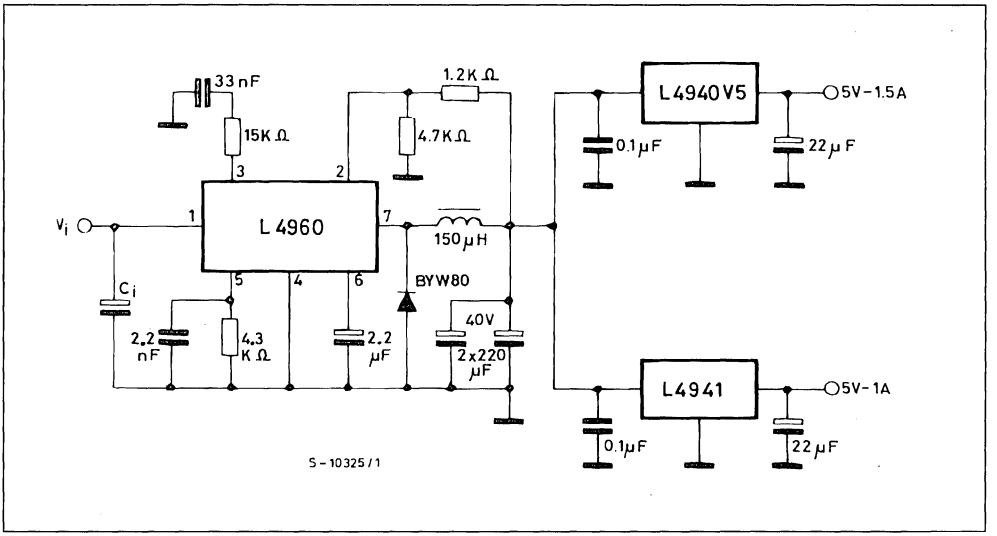
These low drop regulators also bring important benefits in supplies using post regulation, the technique where one or more linear regulators follow another regulator (often switching), to improve precision, reduce ripple and improve transient response. Though lightweight and cheap, an offline switching regulator suffers from poor load and line regulation and needs additional chokes and capacitors to reduce ripple.

Using standard regulators the efficiency of post regulation systems is low because the intermediate voltage must be high enough to allow for the post regulator's voltage drop. Moreover, a lateral PNP low drop regulator has a poor transient response so it cannot reject switching ripple effectively.

If L4940s or L4941s are used for post regulation the intermediate voltage need only be 1V above the final output voltage and 40dB SVR can be obtained at 30kHz. Consequently less power is dissipated both in the post regulators and in the pre-regulator, making post regulation much more attractive -- designers can now have the precision, low ripple and fast response without sacrificing efficiency.

Figure 3 shows a typical post-regulation power supply using a switching regulator, based on the L4960, followed by L4941 low drop regulators.

Figure 3 : Low drop regulators like the L4941 improve the efficiency of post regulation supplies because less power is dissipated and because the intermediate voltage can be lower. In this typical supply design an L4960 offline switching regulator is followed by L4941 post regulators, giving an high overall efficiency.



IMPROVING BATTERY SUPPLIES

The second application area where the L4940 and L4941 are particularly useful is in battery-powered equipment. Because of their lower dropout these devices need fewer battery cells -- five, compared to the six needed for an NPN regulator. In addition, with five NiCd cells the efficiency is 77-96% and the cells can be completely discharged.

The low quiescent current of the L4940 and L4941 reduces power consumption, prolonging battery life. Moreover, since they will continue to provide a stable 5V output with input voltages as low as 5.45V they also extend the effective battery life by allowing continued operation when the battery would previously have been discarded (figure 4).

Figure 4 : The vertical PNP pass transistor permits a minimum dropout without the penalty of higher quiescent current, giving a 30-50% longer battery life in equipment drawing a constant current two hours a day.

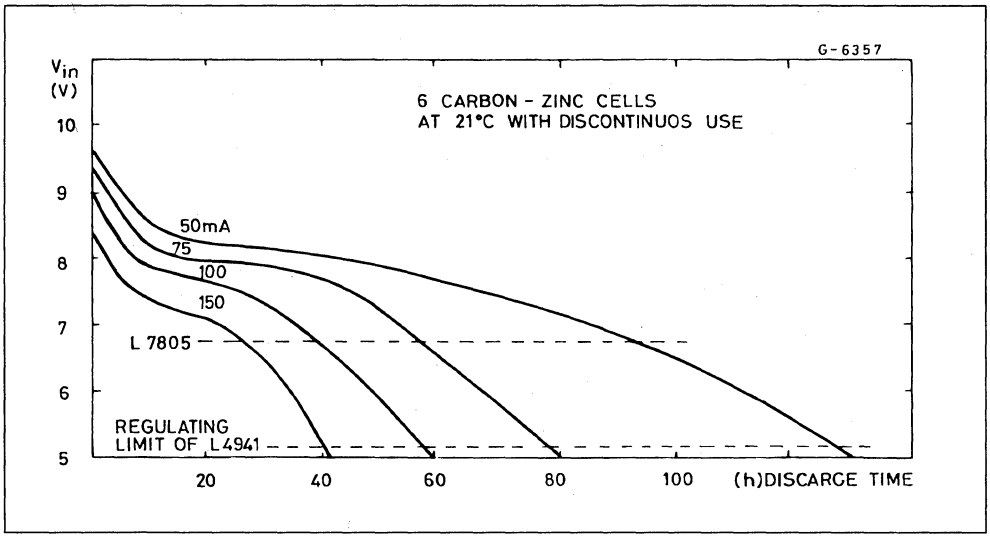
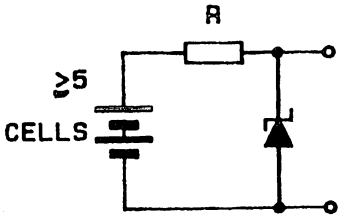
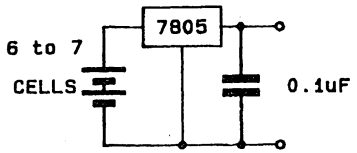


Figure 5 shows how an L4941 solution compares with five alternative 5V battery supplies.

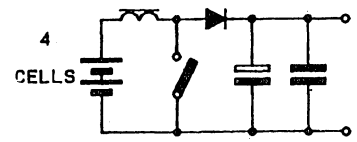
Figure 5 : The L4941 is also useful in battery-powered equipment, prolonging battery life by reducing current drain and supplying a regulated 5V output until the battery voltage has fallen to 5.45V. Here the L4941 solution is compared with five alternatives.



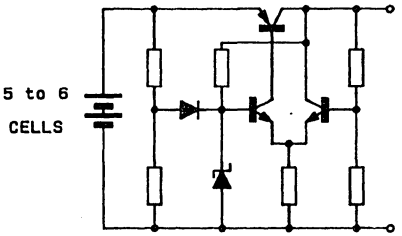
1. ZENER REGULATOR -- High current consumption when battery fully charged and high losses in Rser.



2. NPN SERIES REGULATOR -- Needs at least 7Znn/C, 6NiCd or 4Pd cells..

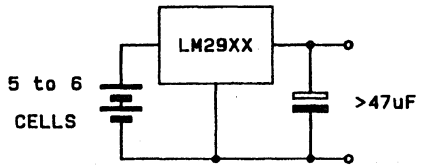


3. DC-DC CONVERTERS -- Complicated and costly. Generates EMI and average efficiency ⇐ 75%.

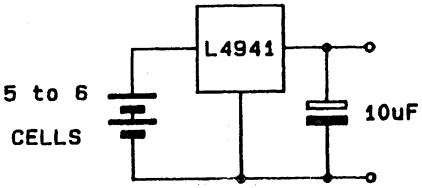


4. DISCRETE LOW DROP REGULATOR -- Bulky and performs poorly in comparison with integrated solutions.

Figure 5 (continued).



5. LATERAL PNP LOW DROP REGULATORS -- High quiescent current, limited output current and stability problems.



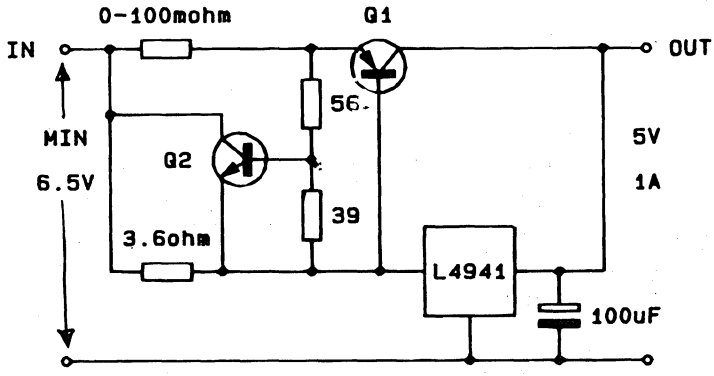
6. L494x VERTICAL PNP LOW DROP REGULATORS -- Need only 6Zn/C cells or 5NiCd cells (which are completely discharged). Quiescent current is low and average efficiency 80%.

HIGHER CURRENT

To obtain more than 1.5A output current a discrete PNP transistor can be added to the L4940 as shown in figure 6. In this circuit Q2 is a current limiter to protect the external pass transistor when the output is short circuited. An on-chip protection circuit prevents damage to the L4940.

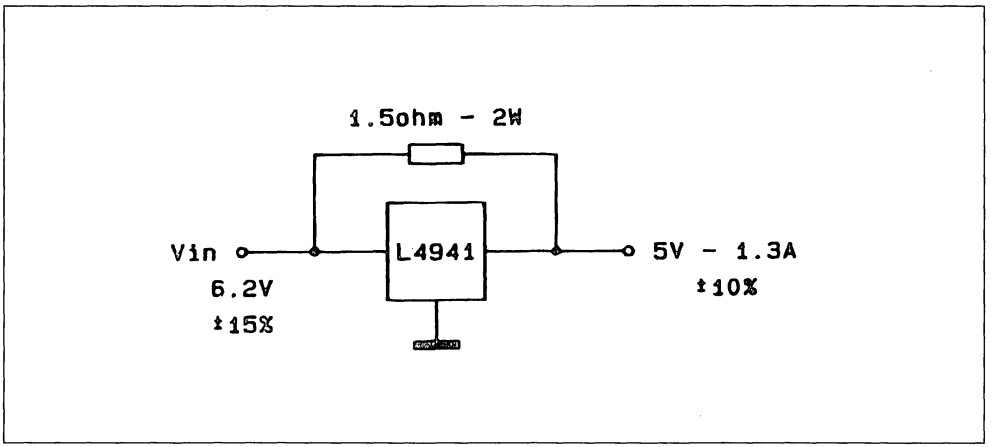
When the load current does not vary greatly higher

Figure 6 : An external PNP transistor can be added to the L4941 to obtain higher output current. Q2 is a current limiter to protect the external transistor.



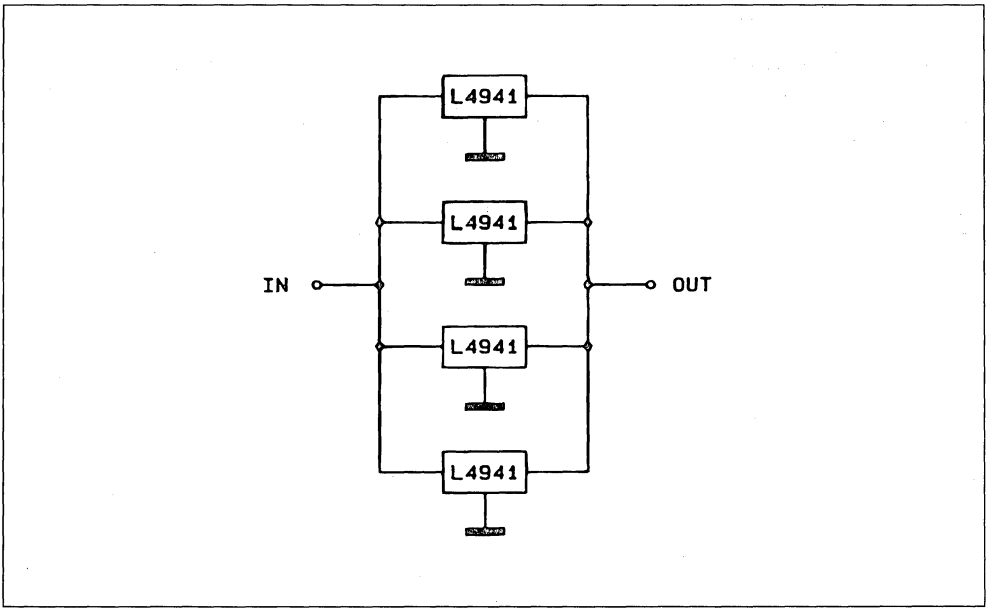
output current can also be obtained by using a shunt resistor as shown in figure 7.

Figure 7 : If the load current does not vary much a simple way to obtain higher current is to add a shunt resistor.



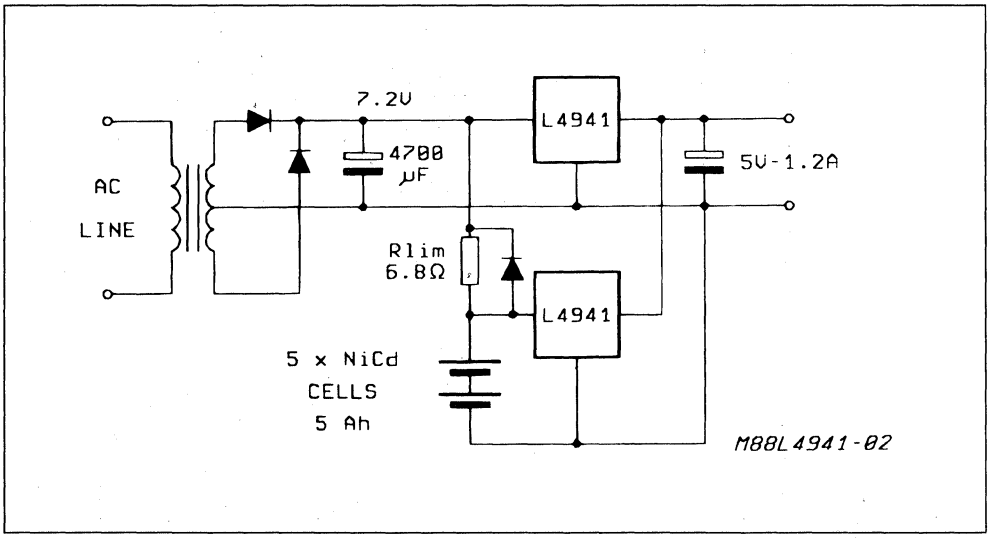
Another way to obtain higher current is simply to connect several devices in parallel as shown in figure 8. This solution also increases the overall reliability of the system and is useful also when reliability is of prime importance.

Figure 8 : Multiple L4941s can be paralleled to increase both output current and reliability.



Finally, higher current can be obtained with two devices in parallel connected to parallel sources (figure 9). This circuit provides an uninterruptable 1.2A/5V output by paralleling the normal line input with a backup battery, which is charged through Rlim when the AC input is present.

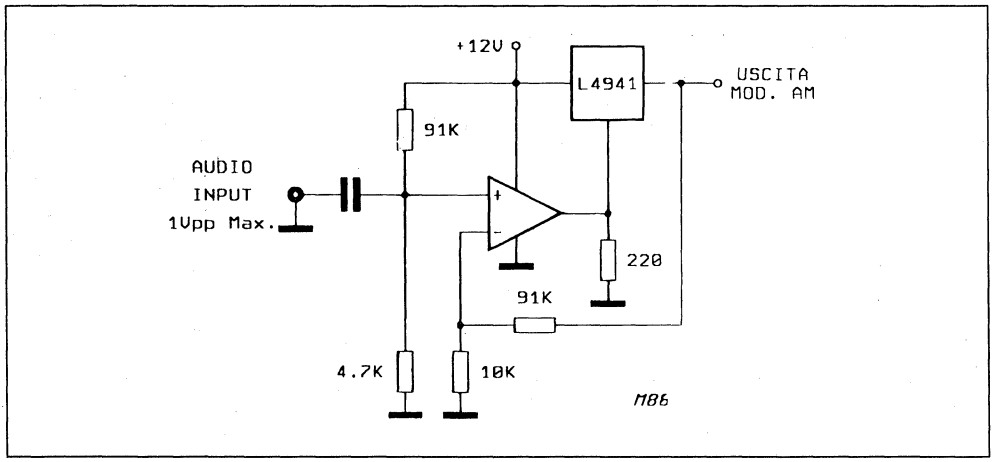
Figure 9 : Connecting two L4941s in parallel with an AC input and a battery yields an efficient 1.2A/5V uninterrutable supply.



USING THE L4941 AS A MODULATOR

Apart from power supply applications, the L4941 can be used as a modulator (figure 10). The modulator part of this circuit is also useful in the lab as a supply for SVR measurements or generally as a basic circuit for an amplifier or generator driving resistive loads. The average output voltage can be varied by adjusting the divider on the non-inverting input of the op amp.

Figure 10 : The L4941 can be used as a modulator as illustrated in this circuit.

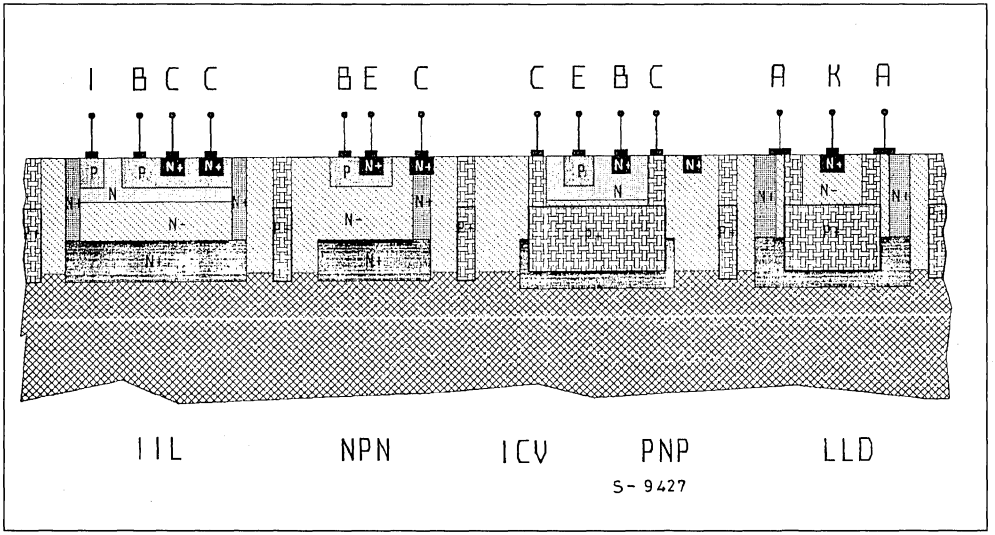


APPENDIX : TECHNOLOGY IS THE KEY

In parallel with the emergence of mixed bipolar/DMOS processes, pure bipolar technology has made significant advances, too. One of the most important of these advances ? the development of a new power PNP transistor structure -- the isolated collector vertical PNP (ICV PNP) -- which is similar in performance to NPN power transistors.

The ICV PNP is a key element in the SGS-THOMSON MICROELECTRONICS Multipower-HDS^2 P^2 (HDS^2 P^2 = High Density Super Signal/Power Process) used to design the L4940 & L4941 low drop regulators, a 20V "Multipower" process which offers NPN & ICV PNP power transistors, small signal NPN & PNP transistors, IIL logic, ECL logic and a new low leakage diode structure (see fig. 11).

Figure 11 : Multipower bipolar process with new ICV-PNP (isolated collector vertical PNP), similar in performance to NPN power transistors.



This process is characterized by an exceptionally high current density -- 6A/mm^2 for NPN transistors ; 2A/mm^2 for PNP transistors (at V_{SAT} = 1V, H_{FE} = 10) -- and very high density in the signal processing section.

Thanks to the ICV PNP power transistor structure, designers can choose any output configuration -- low side, high side, half bridge, bridge. In addition, the low voltage drop of the ICV PNP is very useful in applications where the dropout voltage is critical - in voltage regulators and automotive solenoid drivers, for example.

Another new structure offered by Multipower-HDS^2 P^2, the Low Leakage Diode (LLD) is very useful in power ICs driving inductive loads. With a parasitic PNP gain about four orders of magnitude lower than conventional diodes, the LLDs reduce dissipation in the chip -- always an important consideration in power IC design.

Multipower-HDS^2 P^2 can be applied in simple products where an ICV PNP output stage is needed such as the L4941. Moreover, because it allows the integration of very complex control circuits it is also used for power ICs which integrate a complete power subsystem such as the L6217, a single chip microstepping drive for stepper motors.

A similar process rated at 60V -- Multipower-S^2 P^2 -- has also been developed. While Multipower-HDS^2 P^2 is aimed at low voltage, high complexity applications, Multipower-S^2 P^2 is intended for higher voltage applications with medium complexity control circuits.

A DESIGNER'S GUIDE TO THE L200 VOLTAGE REGULATOR

Delivering 2 A at a voltage variable from 2.85 V to 36 V, the L200 voltage regulator is a versatile device that simplifies the design of linear supplies. This design guide describes the operation of the device and its applications.

The introduction of integrated regulator circuits has greatly simplified the work involved in designing supplies. Regulation and protection circuits required for the supply, previously realized using discrete components, are now integrated in a single chip. This had led to significant cost and space saving as well as increased reliability. Today the designer has a wide range of fixed and adjustable, positive and negative series regulators to choose from as well as an increasing number of switching regulators.

The L200 is a positive variable voltage regulator which includes a current limiter and supplies up to 2 A at 2.85 to 36 V.

The output voltage is fixed with two resistors or, if a continuously variable output voltage is required, with one fixed and one variable resistor.

The maximum output current is fixed with a low value resistor. The device has all the characteristics common to normal fixed regulators and these are described in the datasheet. The L200 is particularly suitable for applications requiring output voltage variation or when a voltage not provided by the standard regulators is required or when a special limit must be placed on the output current.

The L200 is available in two packages :

Pentawatt - Offers easy assembly and good reliability. The guaranteed thermal resistance ($R_{th\ j\text{-}case}$) is 3 °C/W (typically 2 °C/W) while if the device is used without heatsink we can consider a guaranteed junction-ambient thermal resistance of 50 °C/W.

TO-3 - For professional and military use or where good hermeticity is required.

The guaranteed junction-case thermal resistance is 4 °C/W, while the junction-ambient thermal resistance is 35 °C/W.

The junction-case thermal resistance of this package, which is greater than that of the Pentawatt, is partly compensated by the lower contact resistance with the heatsink, especially when an electrical insulator is used.

CIRCUIT OPERATION

As can be seen from the block diagram (fig. 1) the voltage regulation loop is almost identical to that of fixed regulators. The only difference is that the negative feedback network is external, so it can be varied (fig. 3). The output is linked to the reference by :

$$V_{out} = V_{ref} \left(1 + \frac{R2}{R1} \right) \qquad (1)$$

Considering V_{out} as the output of an operational amplifier with gain equal to $G_v = 1 + R2/R1$ and input signal equal to V_{ref}, variability of the output voltage can be obtained by varying R1 or R2 (or both). It's best to vary R1 because in this way the current in resistors R1 and R2 remains constant (this current is in fact given by $V_{ref}/R1$).

Equation (1) can also be found in another way which is more useful in order to understand the descriptions of the applications discussed.

$$V_{out} = R1\ i_1 + R2\ i_2$$

and since in practice $i_1 \gg i_4$ (i_4 has a typical value of 10 μA) we can say that

$$V_{out} + R1\ i_1 + R2\ i_1 \text{ with } i_1 = \frac{V_{ref}}{R1}$$

Therefore

$$V_{out} = \frac{R2}{R1} V_{ref} + V_{ref} = V_{ref} \left(1 + \frac{R2}{R1} \right)$$

In other words R1 fixes the value of the current circulating in R2 so R2 is determined.

Figure 1 : Block Diagram.

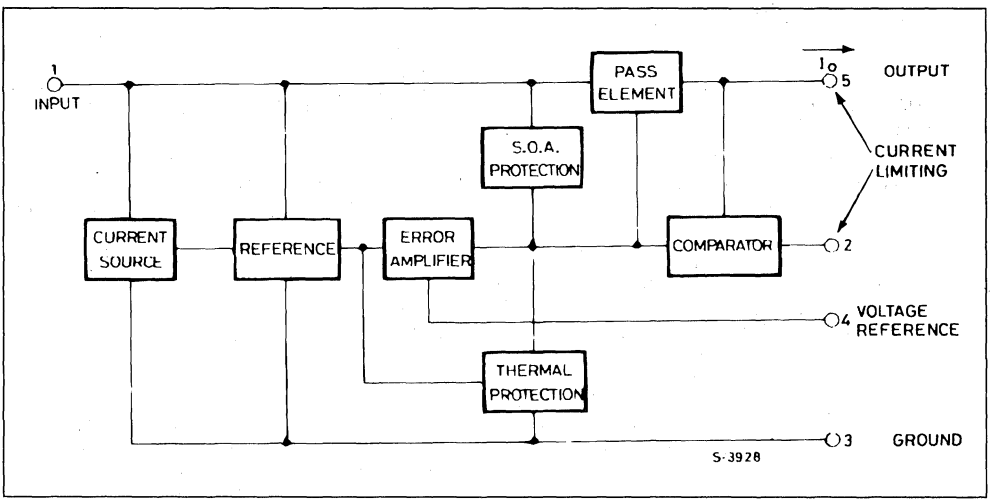


Figure 2 : Schematic Diagram.

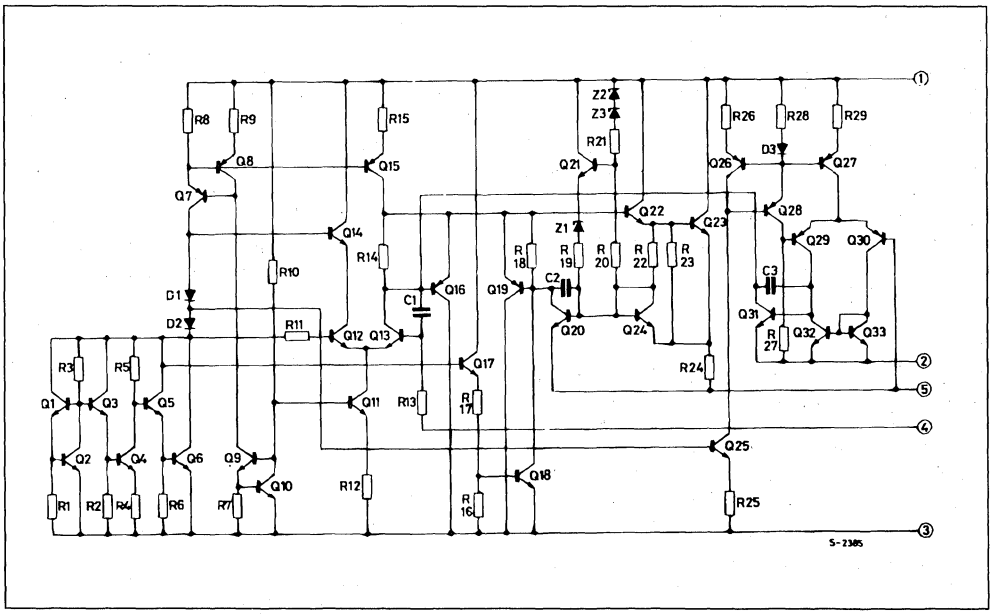
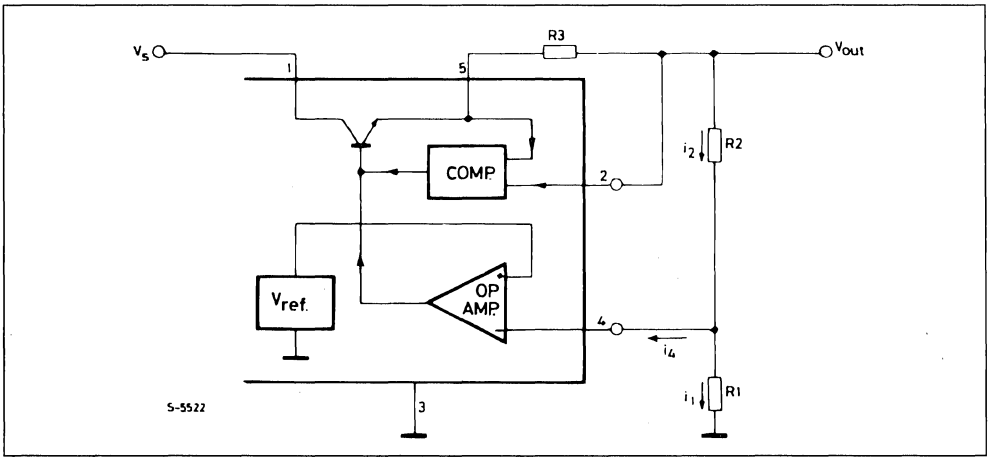


Figure 3.

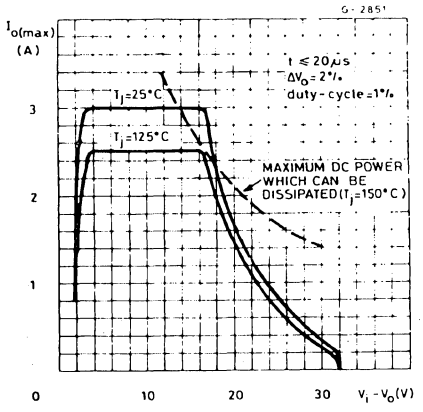


OVERLOAD PROTECTION

The device has an overload protection circuit which limits the current available.

Referring to fig. 2, R24 operates as a current sensor. When at the terminals of R24 there is a voltage drop sufficient to make Q20 conduct, Q19 begins to draw current from the base of the power transistor (darlington formed by Q22 and Q23) and the output current is limited. The limit depends on the current which Q21 injects into the base of Q20. This current depends on the drop-out and the temperature which explains the trend of the curves in fig. 4.

Figure 4.



THERMAL PROTECTION

The junction temperature of the device may reach destructive levels during a short circuit at the output or due to an abnormal increase in the ambient temperature. To avoid having to use heatsinks which are costly and bulky, a thermal protection circuit has been introduced to limit the output current so that the dissipated power does not bring the junction temperature above the values allowed. The operation of this circuit can be summarized as follows.

In Q17 there is a constant current equal to :

$$\frac{V_{ref} - V_{BE17}}{R17 + R16} \quad (V_{ref} = 2.75\ V\ typ)$$

The base of Q18 is therefore biased at :

$$V_{BE18} = \frac{V_{ref} - V_{BE17}}{R16 + R17} \cdot R16 \cong 350\ mV$$

Therefore at $T_j = 25\ °C$ Q18 is off (since 600 mV is needed for it to start conducting). Since the V_{BE} of a silicon transistor decreases by about 2 mV/°C, Q18 starts conducting at the junction temperature :

$$T_j = \frac{600 - 350}{2} + 25 = 150\ °C$$

CURRENT LIMITATION

The innovative feature of this device is the possibility of acting on the current regulation loop, i.e. of limiting the maximum current that can be supplied to the desired value by using a simple resistor (R3 in fig. 2). Obviously if R3 = 0 the maximum output cur-

rent is also the maximum current that the device can supply because of its internal limitation.

The current loop consists of a comparator circuit with fixed threshold whose value is V_{sc}. This comparator intervenes when $I_o \cdot R3 = V_{sc}$, hence

$$I_O = \frac{V_{SC}}{R3}$$ (V_{SC} is the voltage between pin 5 and 2 with typical value of 0.45 V).

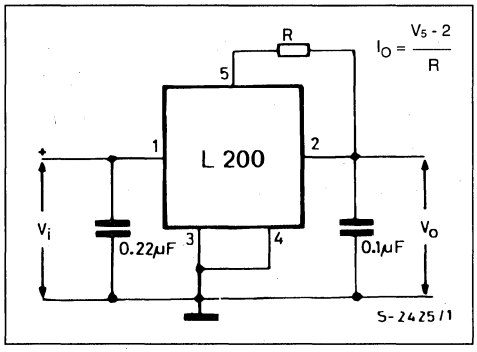
Special attention has been given to the comparator circuit in order to ensure that the device behaves as a current generator with high output impedance.

TYPICAL APPLICATIONS

PROGRAMMABLE CURRENT REGULATOR

Fig. 5 shows the device used as current generator. In this case the error amplifier is disabled by short-circuiting pin 4 to ground.

Figure 5.



The output current I_o is fixed by means of R :

$$I_O = \frac{V_{5-2}}{R}$$

The output voltage can reach a maximum value $V_i - V_{drop} \cong V_i$ 2 V (V_{drop} depends on I_o).

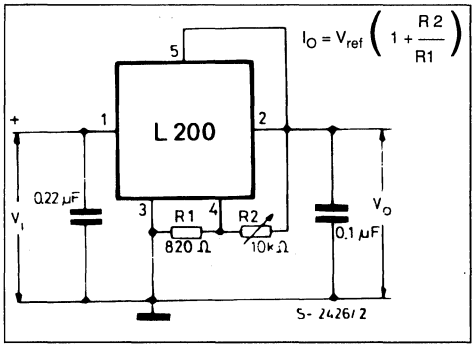
PROGRAMMABLE VOLTAGE REGULATOR

Fig. 6 shows the device connected as a voltage regulator and the maximum output current is the maximum current that the device can supply. The output voltage V_o is fixed using potentiometer R2. The equation which gives the output voltage is as follows :

$$V_O = V_{ref} \left(1 + \frac{R2}{R1}\right)$$

By substituting the potentiometer with a fixed resistor and choosing suitable values for R1 and R2, it is possible to obtain a wide range of fixed output voltages.

Figure 6.



The following formulas and tables can be used to calculate some of the most common output voltages.

Having fixed a certain V_o, using the previous formula, the maximum value is :

$$V_{O\,max} = V_{ref\,max} \left(1 + \frac{R2_{max}}{R1_{min}}\right)$$ and the minimum value is :

$$V_{O\,min} = V_{ref\,min} \left(1 + \frac{R2_{min}}{R1_{max}}\right)$$

The table below indicates resistor values for typical output voltages :

V_o ± 4 %	R1 ± 1 %	R2 ± 1 %
5 V	1.5 kΩ	1.2 kΩ
12 V	1 kΩ	3.3 kΩ
15 V	750 Ω	3.3 kΩ
18 V	330 Ω	1.8 kΩ
24 V	510 Ω	3.9 kΩ

PROGRAMMABLE CURRENT AND VOLTAGE REGULATOR

The typical configuration used by the device as a voltage regulator with external current limitation is shown in fig. 7. The fixed voltage of 2.77 V at the terminals of R1 makes it possible to force a constant current across variable resistor R2. If R2 is varied, the voltage at pin 2 is varied and so is the output voltage.

The output voltage is given by :

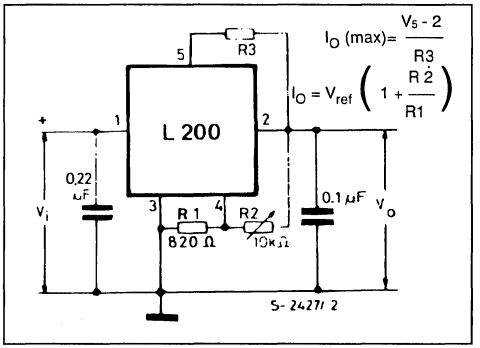
$$V_O = V_{ref} \cdot (1 + \frac{R2}{R1}), \quad \text{with } V_{ref} = 2.77 \text{ V typ}$$

and the maximum output current is given by :

$$I_{O\,max} = \frac{V_{5-2}}{R3} \quad \text{with } V_{5-2} = 0.45 \text{ V typ.}$$

To maintain a sufficient current for good regulation the value of R1 should be kept low. When there is no load, the output current is $V_{ref}/R1$. Suitable values of R1 are between 500 Ω and 1.5 kΩ. If the load is always present the maximum value for R1 is limited by the current value (10 µA) at the input of the error amplifier (pin 4).

Figure 7.



DIGITALLY SELECTED REGULATOR WITH INHIBIT

The output voltage of the device can be regulated digitally as shown in fig. 8. The output voltage depends on the divider formed by R5 and a combination of R1, R2, R3 and P2. The device can be switched off with a transistor.

When the inhibit transistor is saturated, pin 2 is brought to ground potential and the output voltage does not exceed 0.45 V.

REDUCING POWER DISSIPATION WITH DROPPING RESISTOR

If may sometimes be advisable to reduce the power dissipated by the device. A simple and economic method of doing this is to use a resistor connected in series to the input as shown in fig. 9. The input-output differential voltage on the device is thus reduced.

The formula for calculating R is as follows :

$$R = \frac{V_{i\,min} - (V_O + V_{drop})}{I_O}$$

Figure 8.

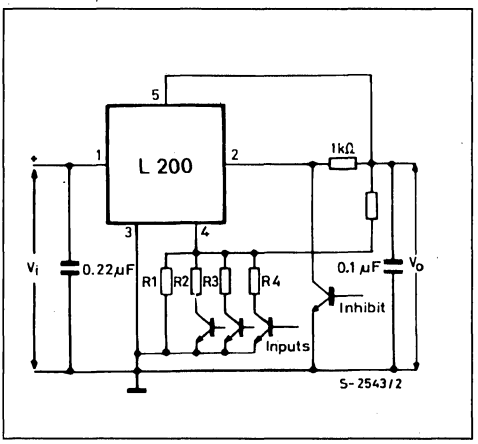
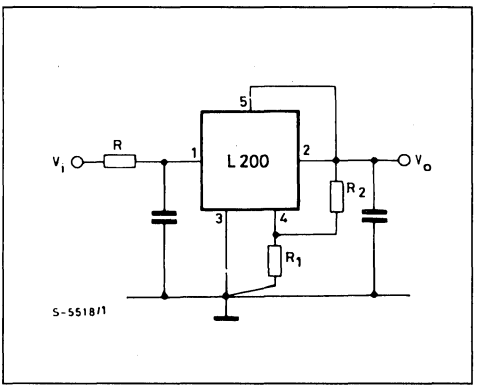


Figure 9.

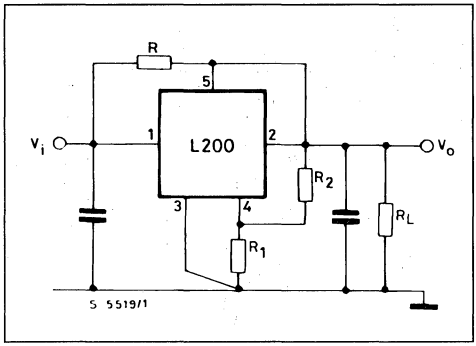


Where V_{drop} is the minimum differential voltage between the input and the output of the device at current I_o. $V_{in\,min}$ is the minimum voltage. V_o is the output voltage and I_o the output current.

With constant load, resistor R can be connected between pins 1 and 2 of the IC instead of in series with the input (fig. 10). In this way, part of the load current flows through the device and part through the resistor. This configuration can be used when the minimum current by the load is :

$$I_{O\,min} = \frac{V_{drop}}{R} \quad \text{(instant by instant)}$$

Figure 10.



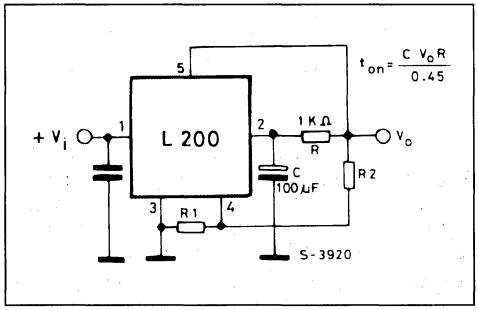
SOFT START

When a slow rise time of the output voltage is required, the configuration in fig. 11 can be used. The rise time can be found using the following formula :

$$t_{on} = \frac{CV_o R}{0.45}$$

At switch on capacitor C is discharged and it keeps the voltage at pin 2 low ; or rather, since a voltage of more than 0.45 V cannot be generated between pins 5 and 2, the V_o follows the voltage at pin 2 at less than 0.45 V.

Figure 11.



Capacitor C is charged by the constant current i_c.

$$i_c = \frac{V_{sc}}{R}$$

Therefore the output reaches its nominal value after the time t_{on} :

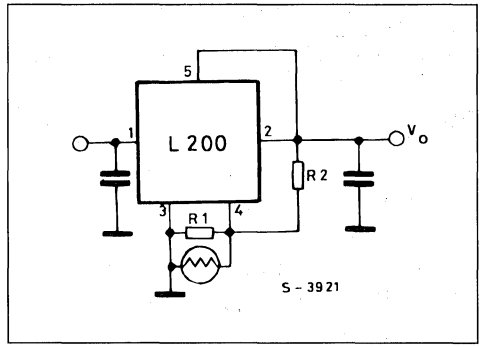
$$V_O - V_{sc} = \frac{I_C \cdot t_{on}}{C}$$

$$t_{on} = C \cdot \frac{V_O - 0.45}{0.45} \cdot R \cong \frac{CV_OR}{0.45}$$

LIGHT CONTROLLER

Fig. 12 shows a circuit in which the output voltage is controlled by the brightness of the surrounding environment. Regulation is by means of a photo resistor in parallel with R1. In this case, the output vol-tage increases as the brightness increases. The opposite effect, i.e. dimming the light as the ambient light increases, can be obtained by connecting the photoresistor in parallel with R2.

Figure 12.



LIGHT DIMMER FOR CAR DISPLAY

Although digital displays in cars are often more aesthetically pleasing and frequently more easily read they do have a problem. Under varying ambient light conditions they are either lost in the background or alternatively appear so bright as to distract the driver. With the system proposed here, this problem is overcome by automatically adjusting the display brightness during daylight conditions and by giving the driver control over the brightness during dusk and darkness conditions.

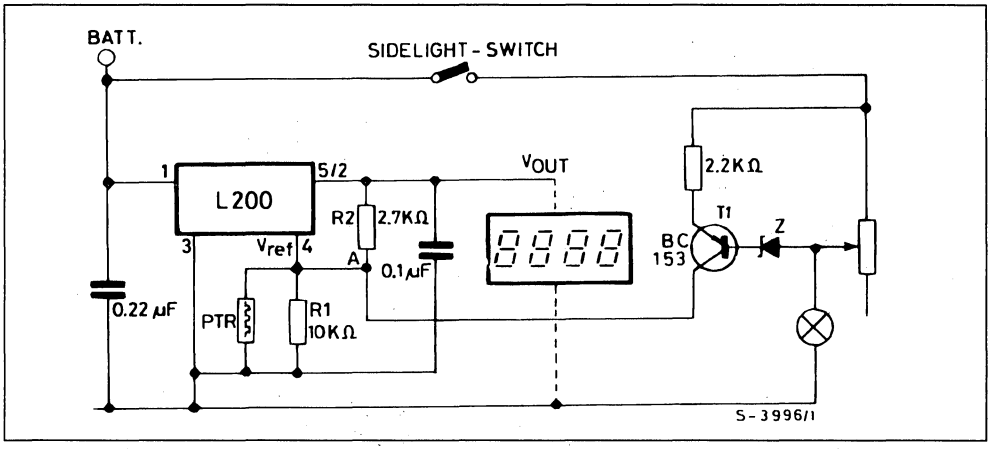
The circuit is shown in fig. 13. The primary supply is shown taken straight from the car battery however it is worth noting that in a car there is always the risk of dump voltages up to 120 V and it is recommended that some form of protection is included against this.

Under daylight conditions i.e. with sidelights off and T1 not conducting the output of the device is determined by the values of R1, R2 and the photoresistor (PTR). The output voltage is given by

$$V_{out} = V_{ref} \quad (1 + \frac{R2}{PTR//R1})$$

If the ambient light intensity is high, the resistance of the photoresistor will be low and therefore V_{out} will be high. As the light decreases, so V_{out} decreases dimming the display to a suitable level.

Figure 13.



In dusk conditions, when the sidelights are switched on, T1 starts to conduct with its conduction set by the potentiometer wiper at its uppermost position the sidelights are at their brightest and current through T1 would be a minimum. With the wiper at its lowest position obviously the opposite conditions apply.

The current through T1 is felt at the summing node A along with the currents through R2 and the parallel network R1, PTR. Since V_{ref} is constant the current flowing through R1, PTR must also be constant. Therefore any change in the current through T1 causes an equal and opposite change in the current through R2. Therefore as I_{T1} increases, V_{out} decreases i.e. as the brightness of the side-lights is increased or decreased so is the brightness of the display.

The values of R2 and PTR should be selected to give the desired minimum and maximum brightness levels desired under both automatic and manual conditions although the minimum brightness under manual conditions can also be set by the maximum current flowing through T1 and, in any case, this should not exceed the maximum current through R2 under automatic operation.

The circuit shown with a small modification can also be used for dimmers other than in a car. Fig. 15 shows the modification needed. The zener diode should have a $V_F \geq 2.5$ V at I = 10 µA.

HIGHER INPUT OR OUTPUT VOLTAGES

Certain applications may require higher input or output voltages than the device can produce. The problem can be solved by bringing the regulator back

Figure 14.

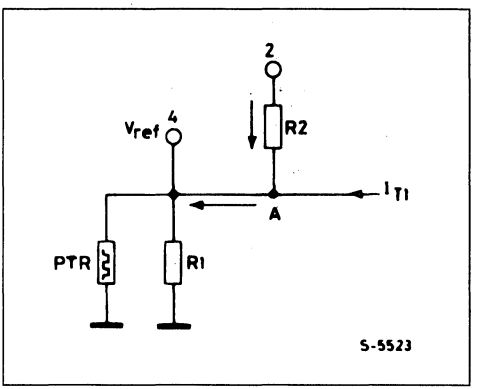
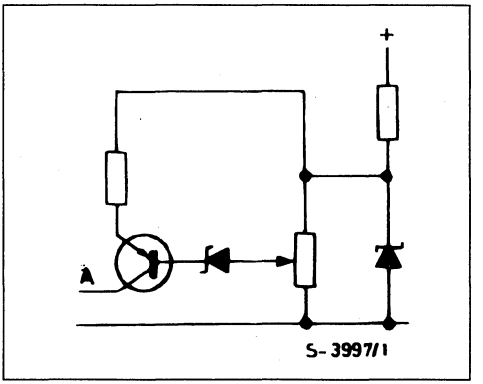


Figure 15.



into the normal operating units with the help of external components.

When there are high input voltages, the excess voltage must be absorbed with a transistor. Figs. 16 and 17 show the two circuits :

Figure 16.

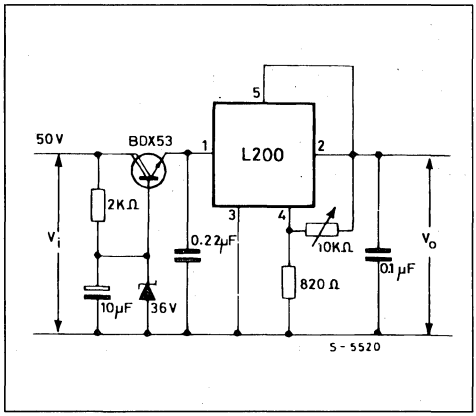
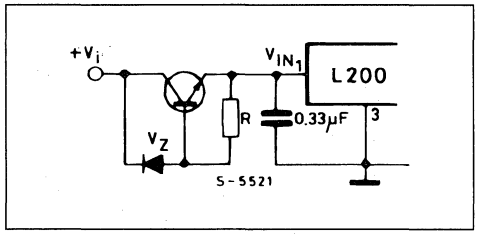


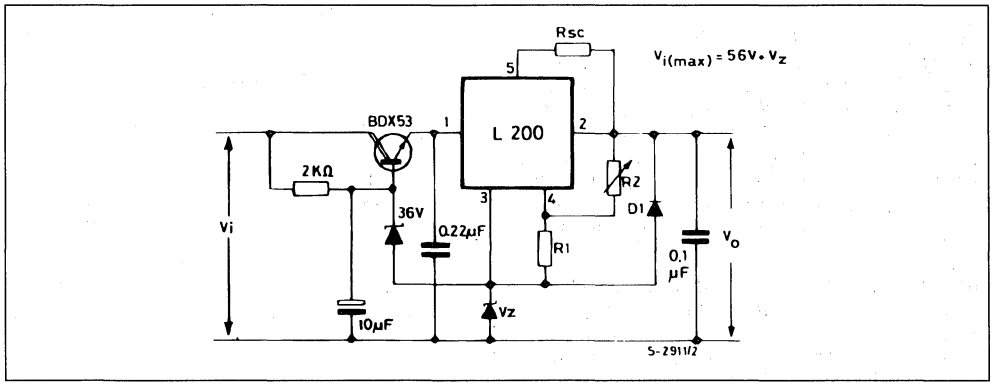
Figure 17.



The designer must take into account the dissipated power and the SOA of the preregulation transistor. For example, using the BDX53, the maximum input voltage can reach 56 V (fig. 16). In these conditions we have 20 V of V_{CE} on the transistor and with a load current of 2 A the operation point remains inside the SOA. The preregulation used in fig. 16 reduces the ripple at the input of the device, making it possible to obtain an output voltage with negligible ripple.

If high output voltages are also required, a second zener, V_Z, is used to refer the ground pin of an IC to a potential other than zero ; diode D1 provides output shortcircuit protection (fig. 18).

Figure 18.



POSITIVE AND NEGATIVE VOLTAGE REGULATORS

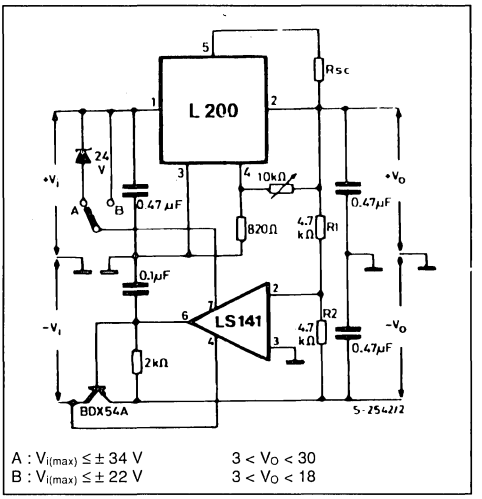
The circuit in fig. 19 provides positive and negative balanced, stabilized voltages simultaneously. The L200 regulator supplies the positive voltage while the negative is obtained using an operational amplifier connected as follower with output current booster.

Tracking of the positive voltage is achieved by putting the non-inverting input to ground and using the inverting input to measure the feedback voltage coming from divider R1-R2.

The system is balanced when the inputs of the operational amplifier are at the same voltage, or, since one input is at fixed ground potential, when the voltage of the intermediate point of the divider foes to 0 Volts. This is only possible if the negative voltage, on command of the op-amp, goes to a value which will make a current equal to that in R1 flows in R2. The ratio which expresses the negative output voltage is :

$$V^- = V^+ \cdot \frac{R2}{R1}$$ (If R2 = R1, we'll get $V^- = V^+$)

Figure 19.



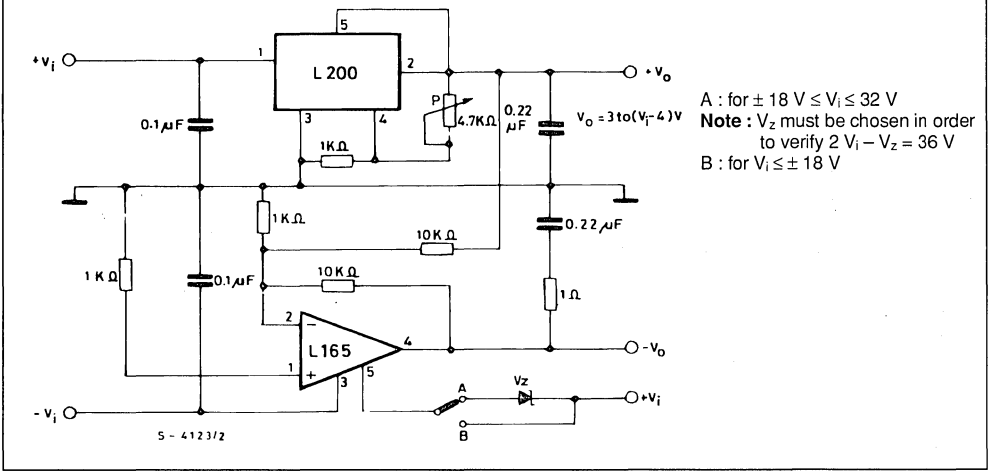
A : $V_{i(max)} \leq \pm 34$ V $3 < V_O < 30$
B : $V_{i(max)} \leq \pm 22$ V $3 < V_O < 18$

Since the maximum supply voltage of the op amp used is ± 22 V, when pin 7 is connected to point B output voltages up to about 18 V can be obtained. If on the other hand pin 7 is connected to point A, much higher output voltages, up to about 30 V, be obtained since in this case the input voltage can rise to 34 V.

Fig. 20 shows a diagram is which the L165 power op amp is used to produce the negative voltage. In this case (as in fig. 19) the output voltage is limited by the absolute maximum rating of the supply voltage of the L165 which is ± 18 V. Therefore to get a higher Vout we must use a zener to keep the device supply within the safety limits.

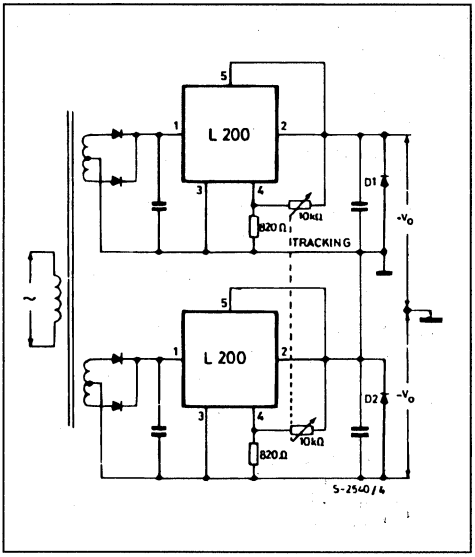
If we have a transformer with two separate secondaries, the diagram of fig. 21 can be used to obtain independent positive and negative voltages. The two output diodes, D1 and D2, protect the devices from shortcircuits between the positive and negative outputs.

Figure 20.



A : for ± 18 V ≤ V_i ≤ 32 V
Note : V_z must be chosen in order to verify 2 $V_i - V_z = 36$ V
B : for $V_i \leq \pm 18$ V

Figure 21.



COMPENSATION OF VOLTAGE DROP ALONG THE WIRES

The diagram in fig. 22 is particularly suitable when a load situated far from the output of the regulator has to be supplied and when we want to avoid the use of two sensing wires. In fact, it is possible to compensate the voltage drop on the line caused by the load current (see the two curves in fig. 23 and 24). R_K transforms the load current I_L into a proportional voltage in series to the reference of the L200. R_K I_L is then amplified by the factor

$$\frac{R2 + R1}{R1}$$

With the values of R_Z, R2 and R1 known, we get :

$$R_K = R_Z \frac{R1}{R1 + R2}$$

R_Z, R1 and R2 are assumed to be constant.

If R_K is higher than 10 Ω , the output voltage should be calculated as follows :

$$V_O = I_d R_K + V_{ref} \frac{R2 + R1}{R1}$$

Figure 22.

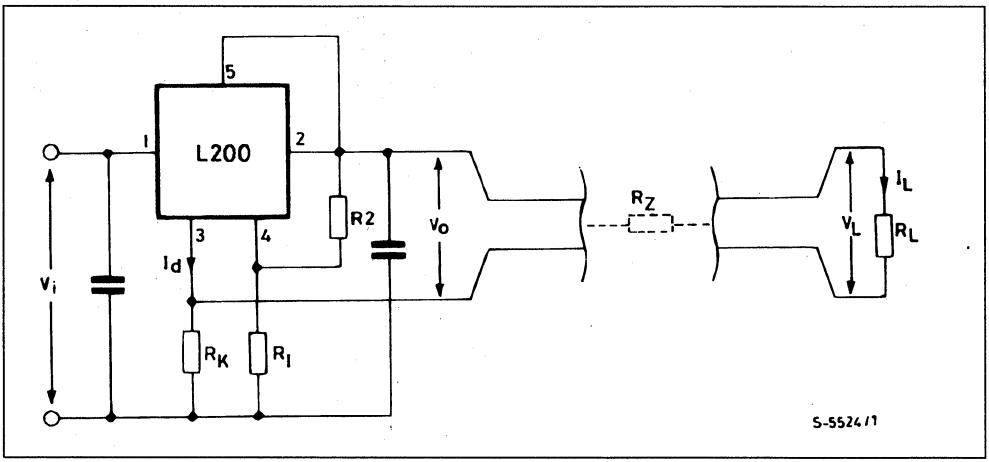


Figure 23.

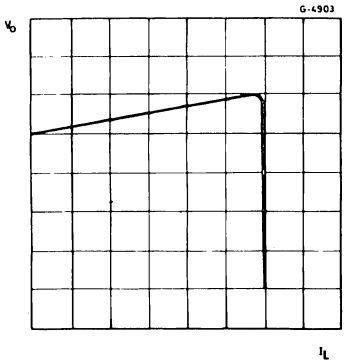
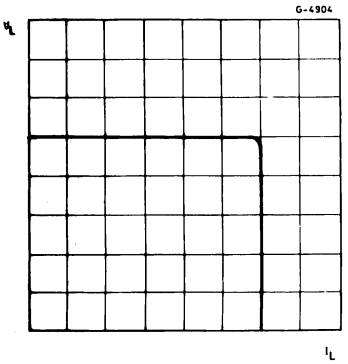


Figure 24.



MOTOR SPEED CONTROL

Fig. 25 shows how to use the device for the speed control of permanent magnet motors. The desired speed, proportional to the voltage at the terminal of the motor, is obtained by means of R1 and R2.

$$V_M = V_{ref} \left(1 + \frac{R2}{R1}\right)$$

To obtain better compensation of the internal motor resistance, which is essential for good regulation, the following equation is used :

$$R3 \leq \frac{R1}{R2} \cdot RM$$

This equation works with infinite R4. If R4 is finite, the motor speed can be increased without altering the ratio R2/R1 and R3. Since R4 has a constant voltage (V_{ref}) at its terminals, which does not vary as R4 varies, this voltage acts on R2 as a constant current source variable with R4. The voltage drop on R2 thus increases, and the increase is felt by the voltage at the terminals of the motor. The voltage increase at the motor terminals is :

$$V_M = \frac{V_{ref}}{R4 + R3} \cdot R2$$

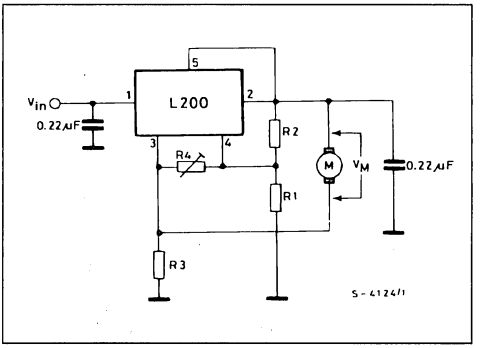
A circuit for a 30 W motor with $R_M = 4\,\Omega$, $R1 = 1\,k\Omega$, $R2 = 4.3\,k\Omega$, $R4 = 22\,k\Omega$ and $R3 = 0.82\,\Omega$ has been realized.

POWER AMPLITUDE MODULATOR

In the configuration of fig. 26 the L200 is used to send a signal onto a supply line. Since the input signal V_i is DC decoupled, the V_o is defined by :

$$V_O = V_{ref} \left(1 + \frac{R2}{R1}\right)$$

Figure 25.



The amplified signal V_i whose value is :

$$G_V = -\frac{R2}{R3}$$

is added to this component. By ignoring the current entering pin 4, we must impose $i_1 = i_2 + i_3$ (1) and since the voltage between pin 4 and ground remains fixed (V_{ref}) as long as the device is not in saturation, $i_1 = 0$ and equation (1) becomes :

$i_2 = -i_3$ with $i_3 = \frac{V_i}{R3}$ (for $X_c \ll R3$) Therefore

$$V_o = R2\ i_2 = -\frac{V_i}{R3} \cdot R2$$

An application is shown in fig. 27. If the DC level is to be varied but not the AC gain, R1 should be replaced by a potentiometer.

Figure 26.

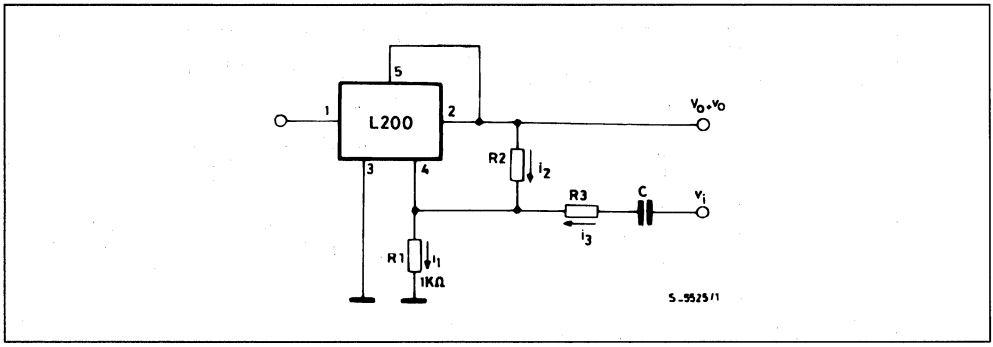
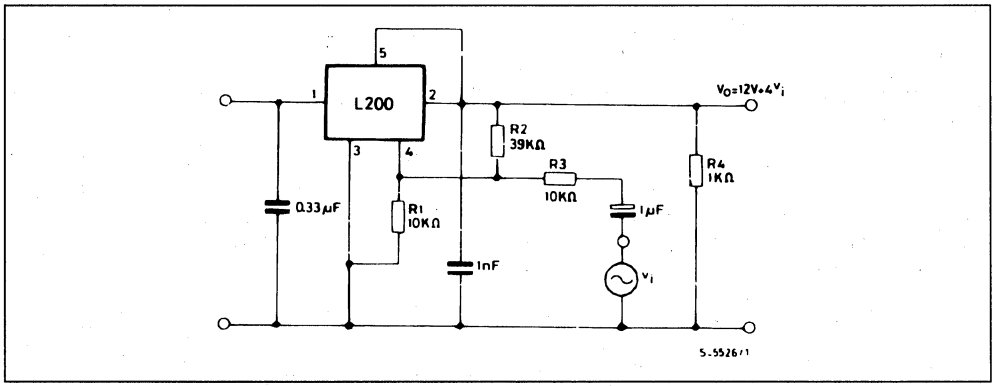


Figure 27.



HIGH CURRENT REGULATORS

To get a higher current than can be supplied by a single device one or more external power transistors must be introduced. The problem is then to extend all the device's protection circuits (short-circuit protection, limitation of T_j of external power devices and overload protection) to the external transistors. Constant current or foldback current limitation therefore becomes necessary.

When the regulator is expected to withstand a permanent shortcircuit, constant current limitation becomes more and more difficult to guarantee as the nominal V_o increases. This is because of the increase in V_{CE} at the terminals of the transistor, which leads to an increase in the dissipated power. The heatsink has to be calculated in the heaviest working conditions, and therefore in shortcircuit. This increases weight, volume and cost of the heatsink and increase of the ambient temperature (because of high power dissipation). Besides heatsink, power transistors must be dimensioned for the short-circuit.

This type, of limitation is suited, for example, with highly capacitive loads. Efficiency is increased if preregulation is used on the input voltage to maintain a constant drop-out on the power element for all V_{out}, even in shortcircuit. Foldback limitation, on the other hand, allows lighter shortcircuit operating conditions than the previous case. The type of load is important.

If the load is highly capacitive, it is not possible to have a high ratio between I_{max} and I_{sc} because at switch-on, with load inserted, the output may not reach its nominal value.

Other protection against input shortcircuit, mains failure, overvoltages and output reverse bias can be realized using two diodes, D1 and D2, inserted as indicated in fig. 28.

Figure 28.

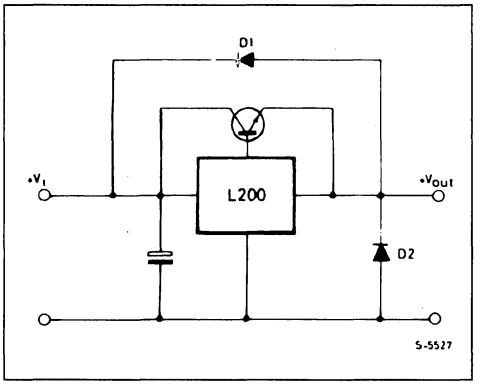
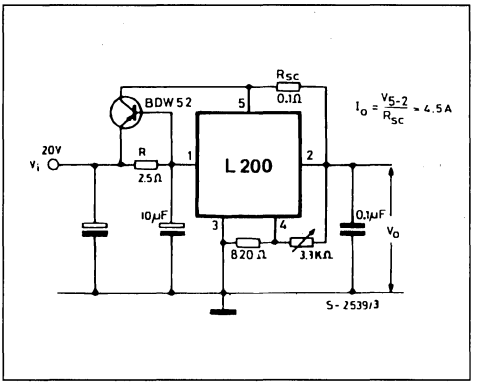


Figure 29.



USE OF A PNP TRANSISTOR

Fig. 29 shows the diagram of a high current supply using the current limitation of the L200. The output current is calculated using the following formula :

$$I_o = \frac{VSC}{RSC} \cong \frac{0.45\ V}{0.1\ \Omega} = 4.5\ A$$

Constant current limitation is used ; so, in output shortcircuit conditions, the transistor dissipates a power equal to :

$$P_D = V_i \cdot I_o = V_i \cdot \frac{V_{SC}}{R_{SC}}$$

The operating point of the transistor should be kept well within the SOA ; with $R_{SC} = 0.1\ \Omega$, V_i must not exceed 20 V. Part of the I_o crosses the transistor and part crosses the regulator.

The latter is given by : $I_{REG} = I_B + \frac{V_{BE}}{R}$

where I_B is the base current of the transistor (–100 mA at I_C = 4 A) and V_{BE} is the base-emitter voltage (– 1 V at I_C = 4 A) ; with R = 2.5 Ω, $I_{REG} \cong$ 500 mA.

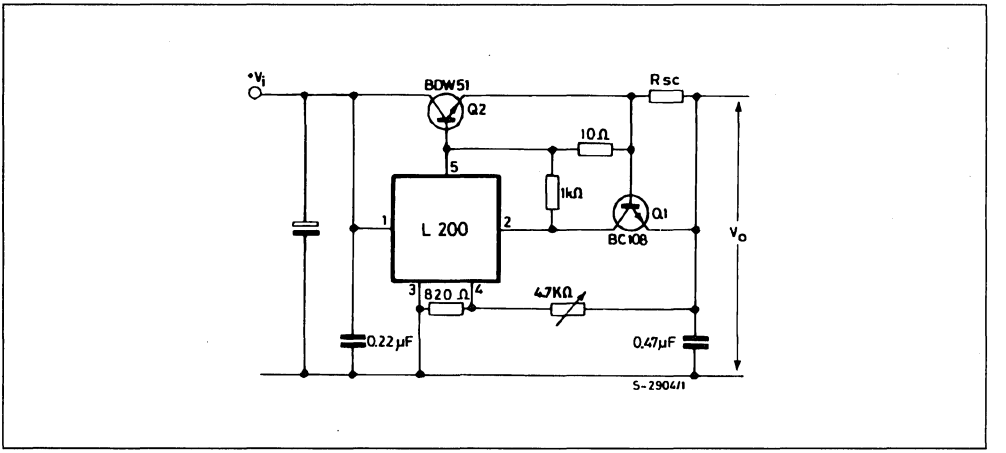
USE OF AN NPN POWER TRANSISTOR

Fig. 30 shows the same application as described in figure 29, using an NPN power transistor instead of a PNP. In this case an external signal transistor must be used to limit the current. Therefore :

$$I_o = \frac{V_{BE\ Q1}}{R_{SC}}$$

As regards the output shortcircuit, see par. 1.5.

Figure 30.



12 V 4 A POWER SUPPLY

The diagram in fig. 31 shows a supply using the L200 and the BD705. The 1 kΩ potentiometer, PT1, together with the 3.3 k resistor are used for fine regulation of the output voltage.

Current limitation is of the type shown in fig. 32. Trimmer PT2 acts on strech AB of characteristic. With the values indicated (PT2 = 1 kΩ, PT3 = 470 Ω, R = 3 kΩ), currents from 3 to 4 A can be limited. The field of variation can be increased by increasing the value of R_{SC} or by connecting one terminal of PT to the base of the power transistor, which, however, provides less stable limitation. If section AB is moved, section BC will also be moved.

The slope of BC can be varied using PT3. The voltage level at point B is fixed by the voltage of the zener diode. The capacitor in parallel to the zener ensures correct switch-on with full load. The BD705 should always be used well within its safe operating area. If this is not possible two or more BD705s should be used, connected in parallel (fig. 33).

Further protection for the external power transistor can be provided as shown in fig. 34. The PTC resistor, whose temperature intervention point must prevent the T_j of the power transistor from reaching its maximum value, should be fixed to the dissipator near the power transistor. Dimensioning of R_A and R_B depends on the PTC used.

Figure 31.

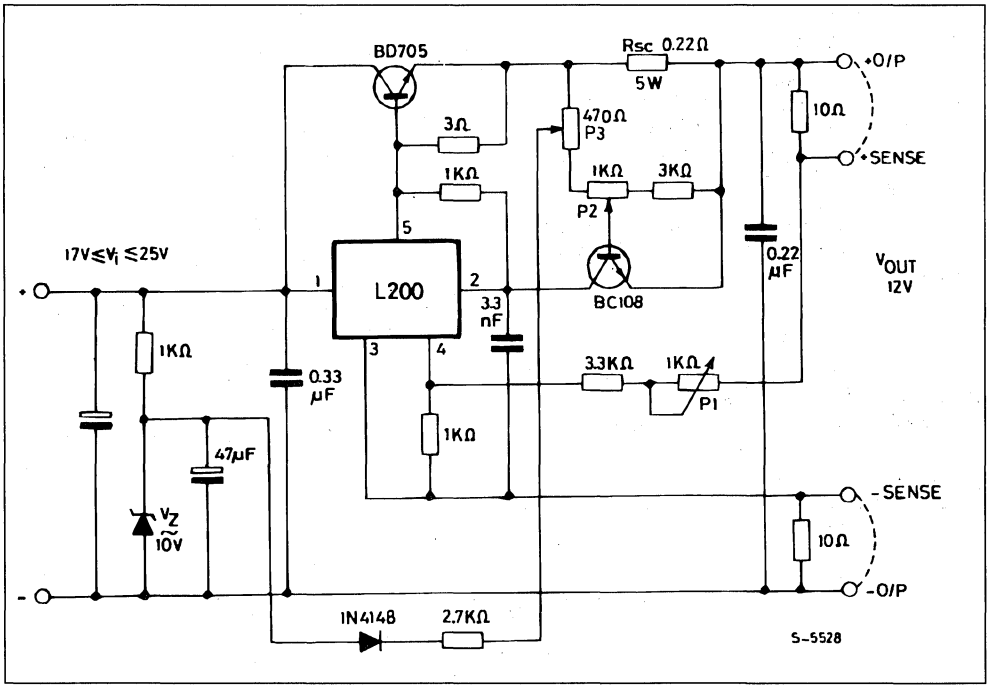


Figure 32.

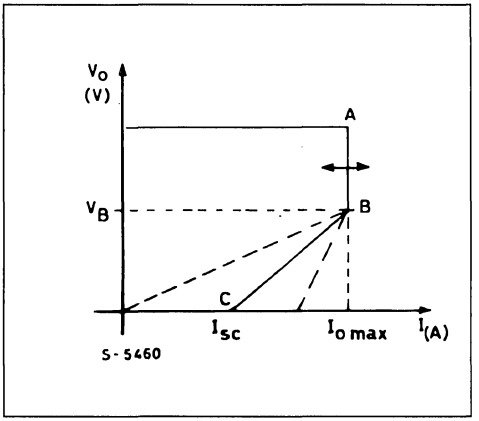


Figure 33.

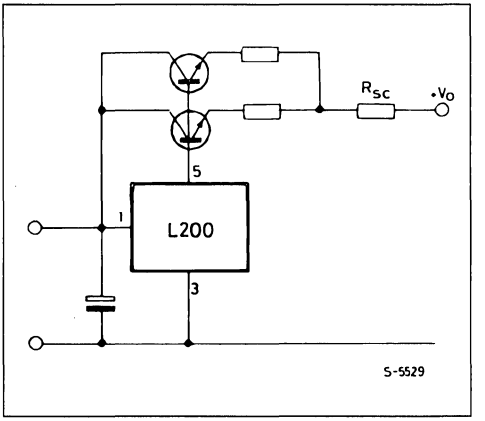
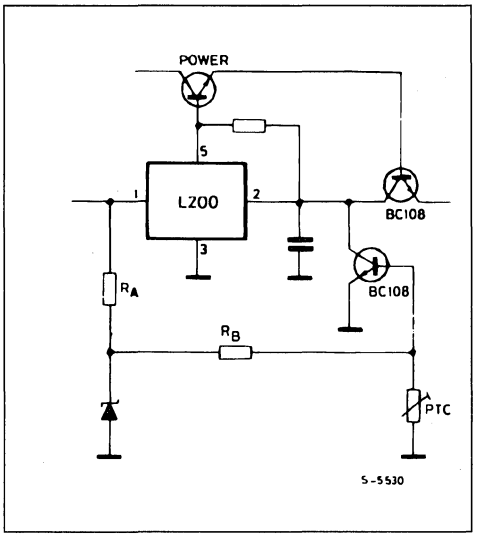


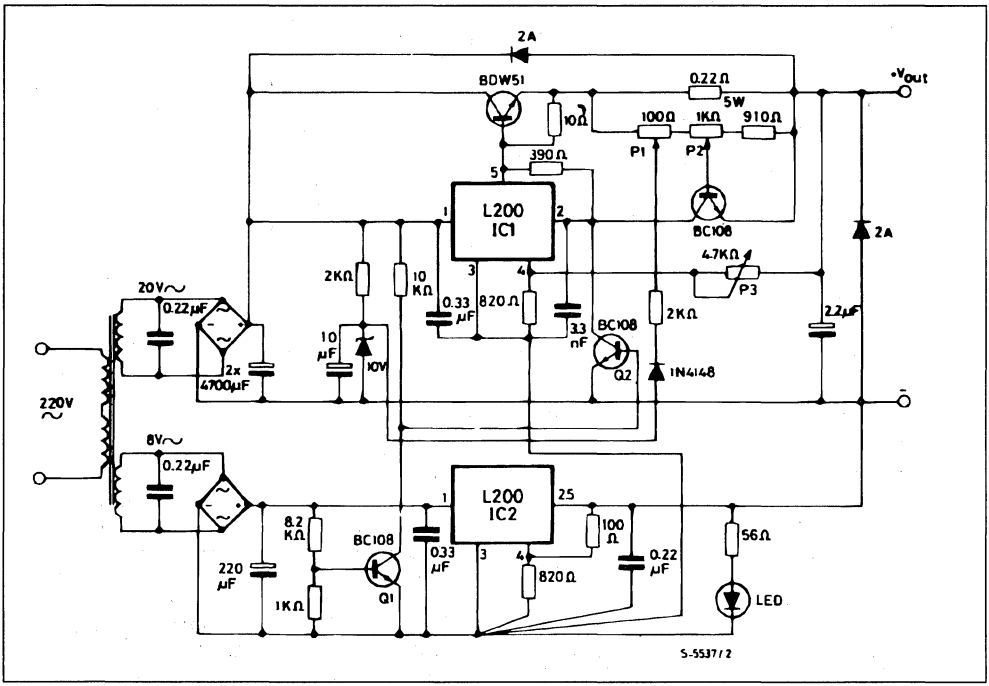
Figure 34.



VOLTAGE REGULATOR FROM 0 V TO 16 V - 4.5 A

Fig. 35 shows an application for a high current supply with output voltage adjustable from 0 V to 16 V, realized with two L200 regulators and an external power transistor. With the values indicated, the current can be regulated from 2 A to 4.5 A by potentiometer PT2. PT1, on the other hand, is used for constant current or foldback current limitation. The integrated circuit IC2, which does not require a heatsink and has excellent temperature stability, is used to obtain the 0 V output. It is connected so as to lower pin 3 of IC1 until pin 4 reaches 0 V. Q1 and Q2 ensure correct operation of the supply at switch-on and switch-off.

Figure 35.



POWER SUPPLY WITH V_o = 2.8 TO 18 V, I_o = 0 TO 2.5 A

The diagram in fig. 36 shows a supply with output voltage variable from 2.8 V to 18 V and constant current limitation from 0 A to 2.5 A. The output current can be regulated over a wide range by means of the op. amp. and signal transistor TR_2. The op. amp. and the transistor are connected in the voltage-current converter configuration. The voltage is taken at the terminals of R3 and converted into current by PT_2.

I_o is fixed as follows :

$$\frac{R4\ I_o}{PT2} = I_1\ (*) \qquad (**)\ I_{sc} = \frac{V_{SC}}{R2}$$

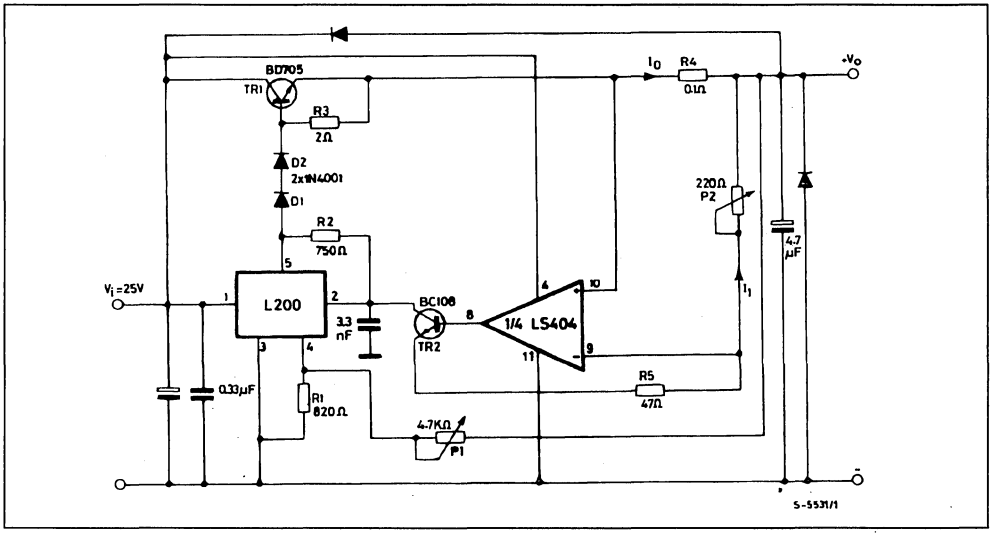
When $I_1 = I_{sc}$, the regulator starts to operate as a current generator. By making (*) equal to (**) we get :

$$\frac{R4\ I_o}{PT_2} = \frac{V_{SC}}{R2} \quad \text{Therefore} \quad I_o = \frac{VSC}{R2 \cdot R4} \cdot PT_2$$

Diodes D1 and D2 keep transistor TR_2 in linear condition in the case of small output currents. If it is not necessary to limit the current to zero, one of the diodes can be eliminated : the second diode could also be eliminated if TR_1 were a darlington instead of a transistor.

The op. amp. must have inputs compatible with ground in order to guarantee current limitation even in shortcircuit. With a negative voltage available, even of only &a few volts, current limitation is simplified.

Figure 36.



LAYOUT CONSIDERATIONS

The performance of a regulator depends to a great extent on the case with which the printed circuit is produced. There must be no impulsive currents (like the one in the electrolytic filter capacitor at the input of the regulator) between the ground pin of the device (pin 3) and the negative output terminal because these would increase the output ripple. Care must also be taken when inserting the resistor connected between pin 4 and pin 3 of the device.

The track connecting pin 3 to a terminal of this resistor should be very short and must not be crossed by the load current (which, since it is generally variable, would give rise to a voltage drop on this stretch of track, altering the value of V_{ref} and therefore of V_o.

When the load is not in the immediate proximity of the regulator output "+ sense" and "– sense" terminals should be used (see fig. 37). By connecting the "+ sense" and "– sense" terminals directly at the charge terminals the voltage drop on the connection cable between supply and load are compensated. Fig. 37 shows how to connect supply and load using the sensing clamps terminals.

Figure 37.

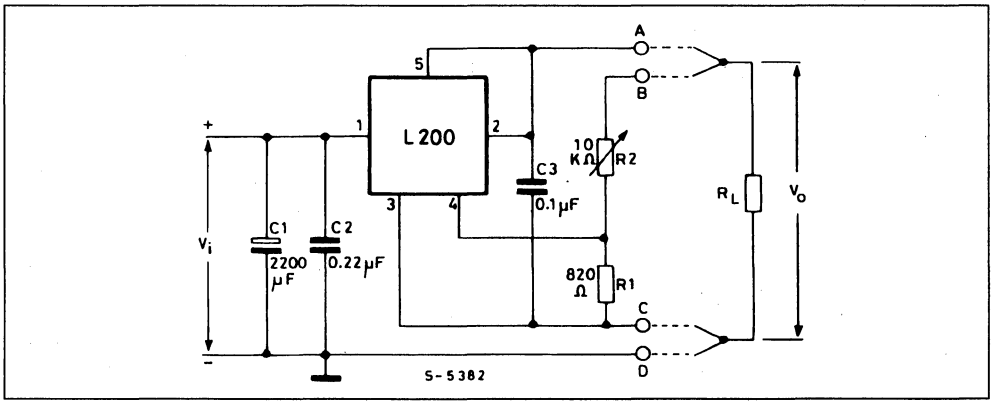
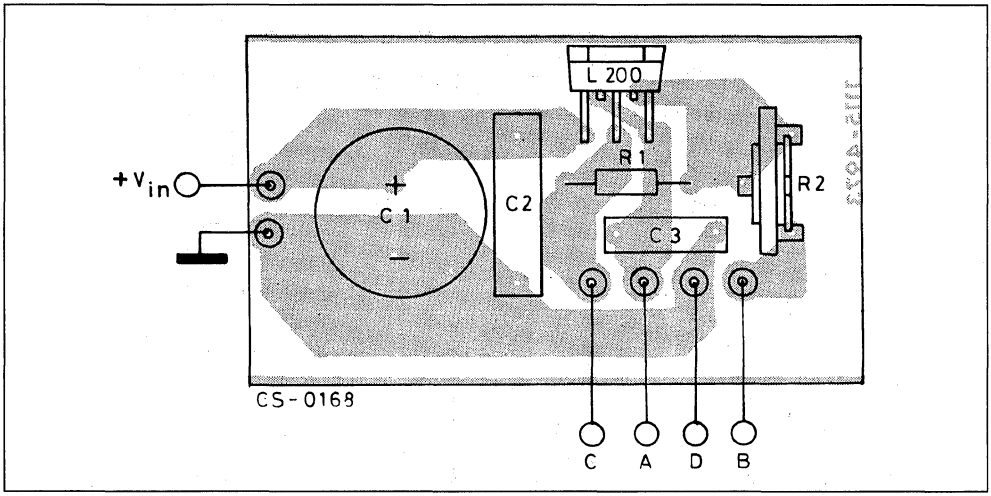


Figure 38.



HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching value which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150 °C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150 °C for long periods or of more than 170 °C for short periods (24 h). In any case the temperature accelerates the ageing process and therefore influences the device life ; an increase of 10 °C can halve the device life. A well designed heatsink should keep the junction temperature between 90 °C and 110 °C. Fig. 39 shows the structure of a power device. As demonstrated in thermodynamics, a thermal circuit can be considered to be an electrical circuit where R1, 2 represent the thermal resistance of the single elements (expressed in C/W) ;

Figure 39.

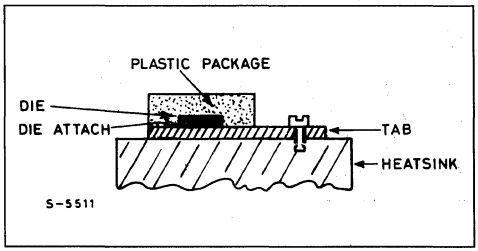
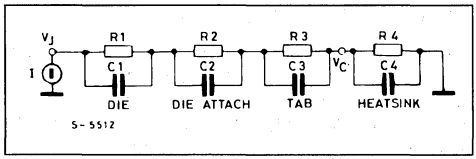


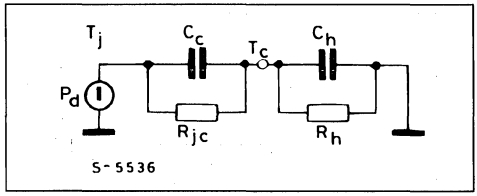
Figure 40.



C1, 2 the thermal capacitance (expressed in °C/W)
I the dissipated power
V the temperature difference with respect to the reference (ground)

This circuit can be simplified as follows :

Figure 41.

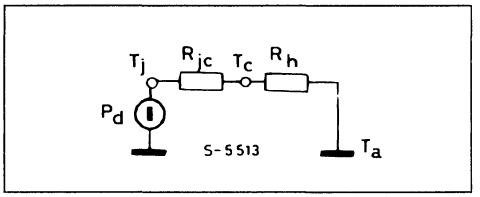


Where C_e is the thermal capacitance of the die plus that of the tab.

C_h is the thermal capacitance of the heatsink
R_{jc} is the junction case thermal resistance
R_h is the heatsink thermal resistance

But since the aim of this section is not that of studing the transistors, the circuit can be further reduced.

Figure 42.



If we now consider the ground potential as ambient temperature, we have :

$$T_i = T_a + (R_{jc} + R_h)\, P_D \qquad (1)$$

$$Rth = \frac{T_i - T_a - R_{IC} \cdot P_d}{Pd} \qquad (1a)$$

$$T_c = T_a + R_h \cdot P_d \qquad (2)$$

For example, consider an application of the L200 with the following characteristics :

$V_{in\ typ} = 20$ V
$V_o = 14$ V
Io typ = 1 A
$T_a = 40$ °C
— typical conditions

$V_{in\ max} = 22$ V
$V_o = 14$ V
$I_{o\ max} = 1.2$ A
$T_a = 60$ °C
— overload conditions

$P_{d\ typ} = (V_{in} - V_o) \cdot I_o = (2014) \cdot 1 = 6$ W

$P_{d\ max} = (2214) \cdot 1.2 = 9.6$ W

Imposing $T_j = 90$ °C of (1a) we get (from L200 characteristics we get $R_{jc} = 3$ °C/W).

$$R_h = \frac{90 - 40 - 3 \cdot 6}{6} = 5.3\ °C/W$$

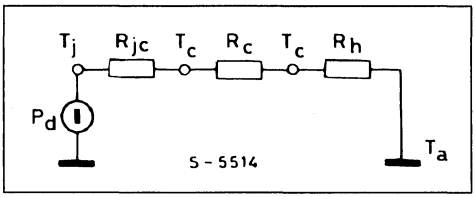
Using the value thus obtained in (1), we get that the junction temperature during the overload goes to the following value :

$$T_j = 60 + (3 + 5.3)\ .\ 9.6 = 140\ °C$$

If the overload occurs only rarely and for short periods, dimensioning can be considered to be correct. Obviously during the shortcircuit, the dissipated power reaches must higher values (about 40 W for the case considered) but in this case the thermal protection intervenes to maintain the temperature below the maximum values allowed.

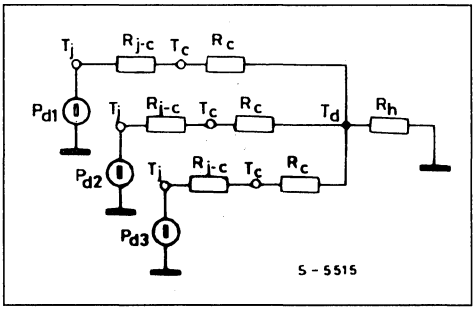
Note 1 : If insulating materials are used between device and heatsink, the thermal contact resistance must be taken into account (0.5 to 1 °C/W, depending on the type of insulant used) and the circuit in fig. 43 becomes :

Figure 43.



Note 2 : In applications where one or more external transistors are used together with the L200, the dissipated power must be calculated for each component. The various junction temperatures can be calculated by solving the following circuit :

Figure 44.



This applies if the various dissipating elements are fairly near to one another with respect to the heatsink dimensions, otherwise the heatsink can no longer be considered as a concentrated constant and the calculation becomes difficult.

This concept is better explained by the graph in fig. 45 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of dissipator and the same dissipated power. The graph in fig. 45 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides. The temperature jump will depend on the dissipated power and one the device geometry but we want to show that there exists an optimal position between the two devices :

$$d = \frac{1}{2} \cdot \text{side of the plate}$$

Fig. 46 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4).

This graph may be useful in applications with the L200 + external transistor (in which the transistor generally dissipates more than the L200) where the temperature of the L200 has to be kept as low as possible and especially where the thermal protection of the L200 is to be used to limit the transistor temperature in the case of an overload or abnormal increase in the ambient temperature. In other words the distance between the two elements can be selected so that the power transistor reaches the $T_{j\,max}$ (200 °C for a TO-3 transistor) when the L200 reaches the thermal protection intervention temperature.

Figure 45.

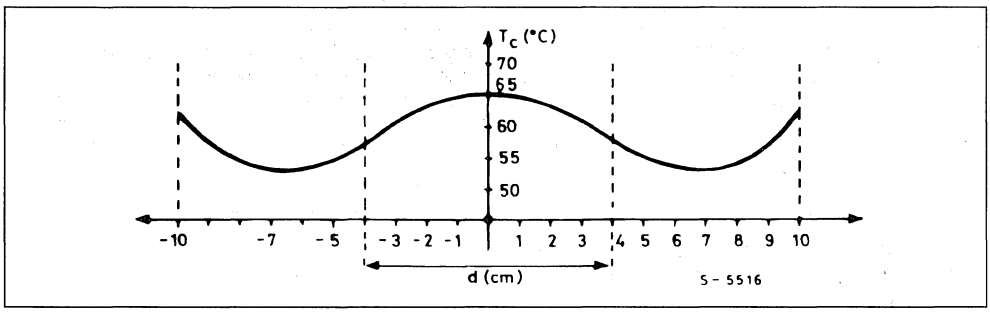
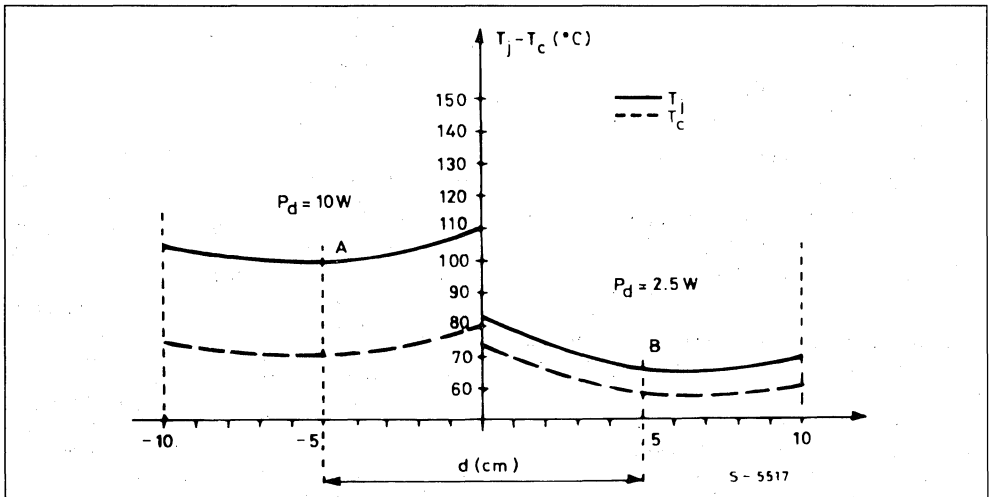


Figure 46.



A : Position of the device with high power dissipation (10 W)
B : Position of the device with low power dissipation (2.5 W)

DUAL REGULATORS SIMPLIFY MICRO SYSTEM SUPPLY DESIGN

Combining two 5 V regulators and a reset circuit on a single chip, special purpose regulator chips simplify the design of power supplies for microprocessor systems incorporating battery backup RAMs or shadow-type NV RAMs.

Power supplies for microprocessor systems are often complicated by the need to take care of the special requirements of non-volatile read/write memory. Where battery backup CMOS RAMs are used, for example, it is important to ensure that the RAMs are disabled when the primary supply is removed. And when shadow-type NV memory is included the backup transfer must be initiated and completed when the supply is interrupted. Designed specifically for such applications, the SGS-THOMSON Microelectronics L4901, and L4902 dual voltage regulators combine two 5 V regulators plus a reset circuit on a single chip, simplifying the designer's task.

Assembled in the SGS-THOMSON Heptawatt [TM] 7-lead package, the L4901 and L4902 contain separate voltage regulators rated at 5 V/300 mA (the "V1" output) and 5 V/400 mA (the "V2" output).

Both the V1 and V2 regulators have an output voltage precision of ± 2 % and include protection against output short circuits and 60 V input transients. Also included on the chip is a reset circuit with externally programmable timing which depends on the input voltage and the output of the V1 regulator.

Functionally, the two devices are identical except that the L4901 has separate inputs to the two regulators and the L4902 has a common input plus a disable input which controls the V2 output (fig. 1).

Generally the V1 regulator is used to supply circuits which must be powered continuously - volatile memory, a time-of-day clock and so on - while the V2 output supplies other 5 V circuits which may be powered down when the equipment is inactive.

The V1 output features a very low leakage current at the output - less than 1 µA - to allow the use a backup battery. The V1 regulator also features a low quiescent current at the input (0.6 mA typical) to minimize battery drain in applications where the V1 regulator is permanently connected to a battery supply.

Figure 1a : TWO 5V OUTPUTS - The L4901 Dual Regulator Provides 300 mA and 400 mA 5 V Outputs and Includes a Microprocessor Reset Function. This Device is Ideal for Microprocessor Systems with Battery Backup or Shadow RAM.

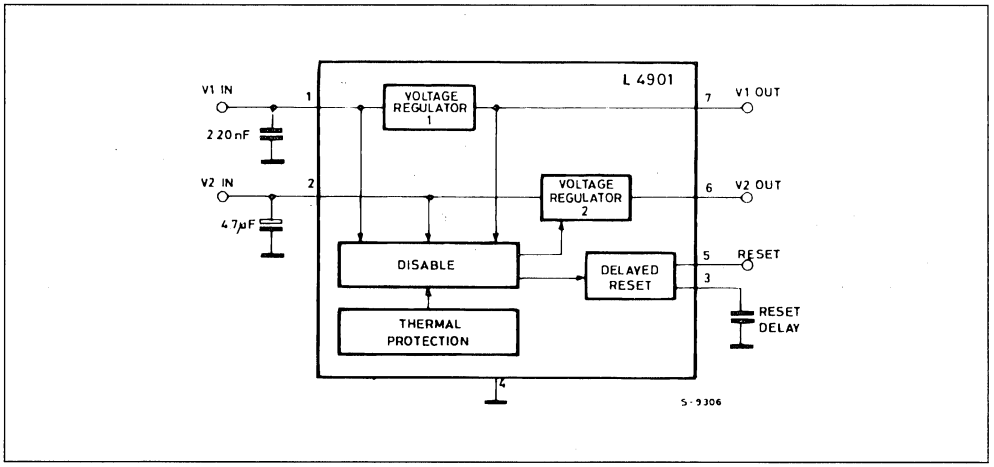


Figure 1b : DISABLE INPUT - The L4902 is Similar to the L4901 but also Features a Disable Input for the V2 Regulator.

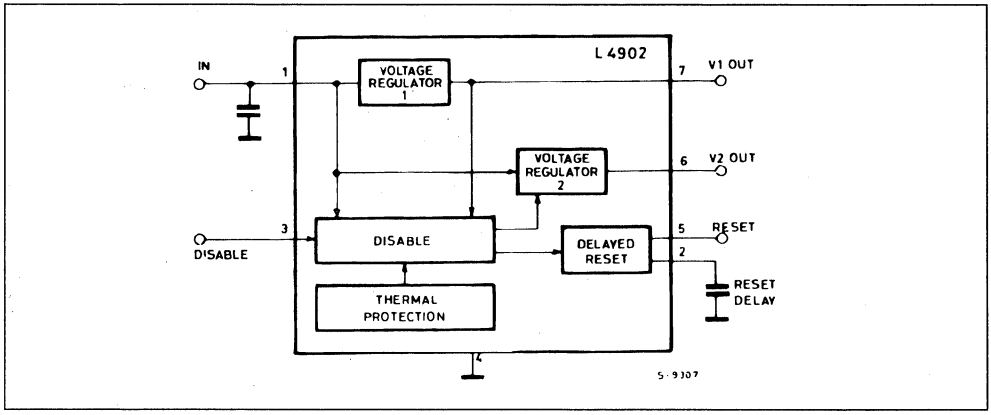
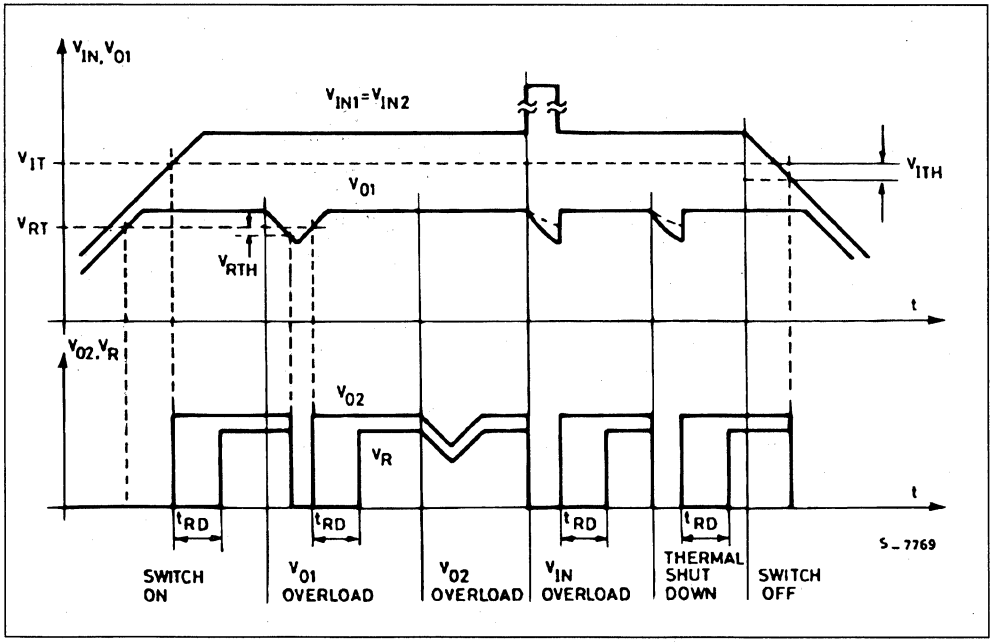


Figure 2 : WAVEFORMS - An Important Feature of the L4901 Series Regulators is that the Reset Circuit Monitors the Input Voltage.



VERSATILE DEVICES

The L4901 and L4902 are versatile devices which simplify the supply circuitry of many systems and can be used in a number of different ways.

One possibility, outlined in figure 3, is to connect the V1 regulator permanently to a battery to supply a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory. In this example the V2 output supplies non-essential 5 V circuits. A typical use of this scheme is in trip computers or car radios with programmable tuning.

An alternative, shown in figure 4, is to use the L4901 with a backup battery on the V1 output to maintain a CMOS clock and a standby-type NMOS microcomputer chip. In this case the main on/off switch disconnects both the V1 and V2 regulators from the battery.

Figure 5 illustrates how the L4902's disable input may be used in a CMOS microcomputer application. In this example the V2 output, supplying non-essential circuits, is turned off under control of the microprocessor circuit. Configurations of this type are used in products where the "OFF" switch is part of a keypad scanned by a micro which operates continuously, even in the "OFF" state.

The L4901 is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shows in figure 6 the V1 output supplies the CMOS RAMs and the V2 output supplies the microprocessor plus other 5 V circuits. The L4901's reset output is used both to reset the Z80 and, through the M74HC138 address decoder, to ensure that the RAMs are disabled as soon as the main supply voltage starts to fall. Note that the M74HC138 is supplied from the backup battery.

It is important to make sure that the RAMs are disabled because the lithium cells used as backup batteries have a high internal resistance. If the RAMs were not forced into the low consumption standby state the battery voltage could drop so low that memory contents are corrupted. Moreover, to prevent latch up, no input of a CMOS RAM should ever be higher than the supply voltage.

Figure 3 : LOW QUIESCENT CURRENT at the V1 Input makes the L4901 Useful in Applications like this where the V1 Regulator is always connected to the Battery.

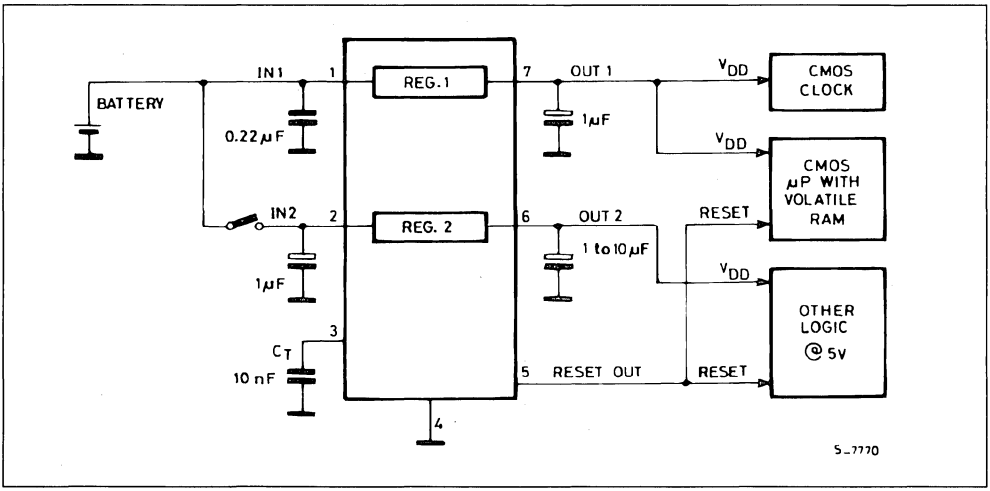


Figure 4 : LOW LEAKAGE at the V1 Output makes the L4901 Ideal for Battery Backup Operation.

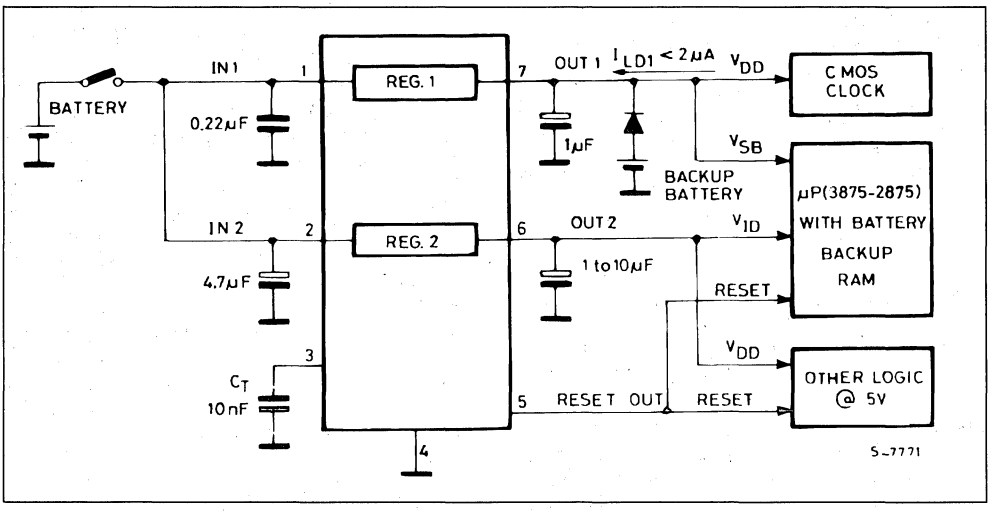
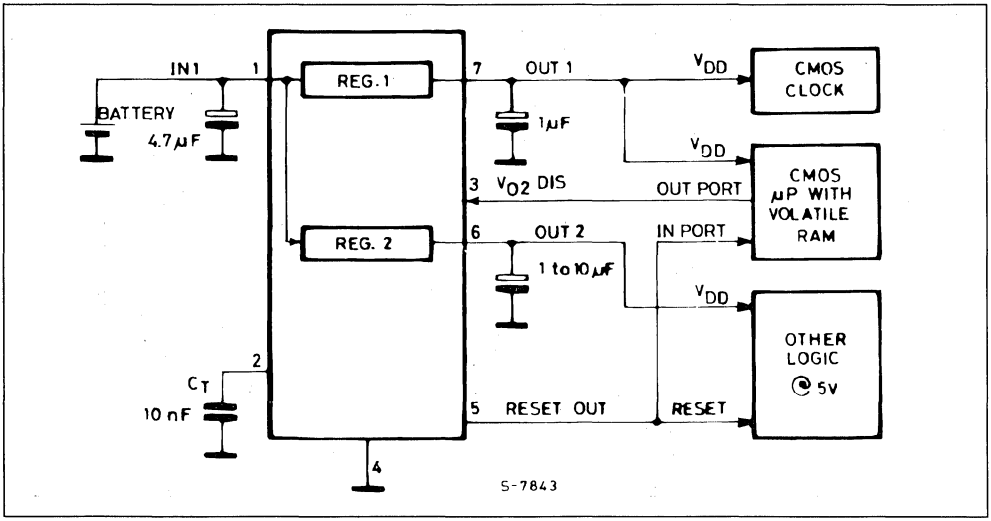


Figure 5 : STANDBY - The L4902 can be used in Applications where the Supply is connected Permanently and the Disable Function Used to Turn Off on-essential Circuits in the Standby State.



IDEAL FOR SHADOW MEMORIES

Another interesting application for the L4902 is supplying a shadow-ram microcomputer chip like the SGS-THOMSON M38SH72 where a fast non-volatile memory is backed up on-chip by a slow EEPROM (figure 7). For these chips it is important to ensure that the backup command is generated when the supply is removed, a function which the L4902's reset output can perform. Since the L4902's reset function depends on the INPUT voltage the power fail condition is sensed early enough to guarantee that the backup transfer will be successful.

In figure 7 the reset output is forced low when the input voltage falls below 6.3 V or when the V1 output goes below 4.8 V. This allows 10 µs for the backup transfer (with 10 µF capacitors) which is more than sufficient.

Similarly, the L4902 can be used with shadow-type RAMs such as the Xicor X2201. In the figure 8 circuit a capacitor on the V1 input ensures that the X2201 is powered during the transfer operation. When the input voltage is removed or goes below 6.3 V the L4902's reset output, connected to the 8085's TRAP input, forces the execution for a service routine which saves the state of the machine in the RAM then issues a backup command. The V2 output drops immediately while the 680 µF capacitor on the V1 input provides enough energy to keep the X2201 running for the 10 ms needed to complete the backup transfer. The low consumption of the V1 regulator allows the use of a relatively small capacitor for this function.

ADING A WATCHDOG

By adding a few components and two Schmitt trigger gates a watchdog function can be added tothe L4902 (figure 9). Normally an output port of the micro will supply a software-generated pulse at least every 10 ms. If something has gone wrong in the software or hardware and these pulses are missing the disable input will be activated after a period set by R1.C1, disabling all the circuitry connected to the V2 output of the L4902. The disable period could be useful to prevent spurious operation of motors and solenoids while the control processor is malfuntioning.

Figure 6 : CMOS RAMs - The L4901 is Useful in Systems with Battery Backup CMOS RAMs Because the Reset Output can be used to Ensure that the RAM Chips are disabled to Reduce Battery Drain when the Main Supply is removed.

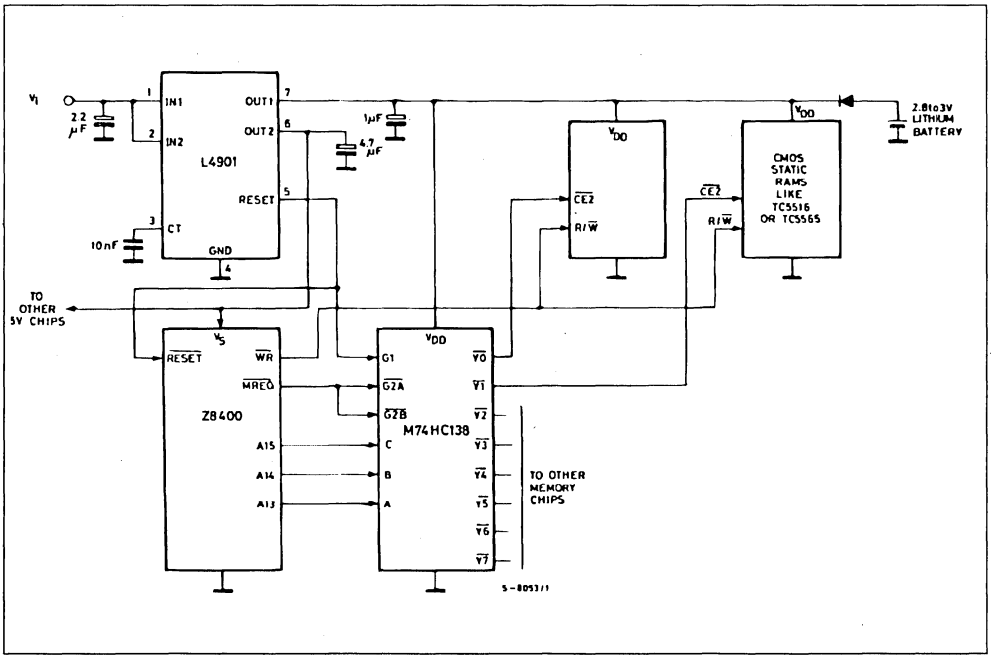


Figure 7 : NV MEMORY µCs - The L4902 is also Useful for Supplying Chips like the SGS-THOMSON M38SH72 Single-chip Micro with NV Memory. In this Application the Reset Circuit initiates the RAM-to-shadow Transfer.

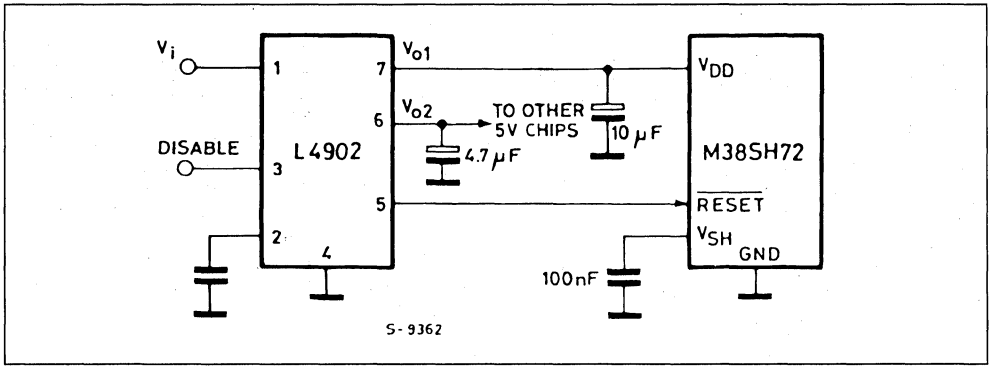


Figure 8 : SHADOW RAMs - The L4901's Reset Function also serves in Systems using Shadow Type NV RAMs like the X2201 to ensure that the Backup Transfer is executed Correctly.

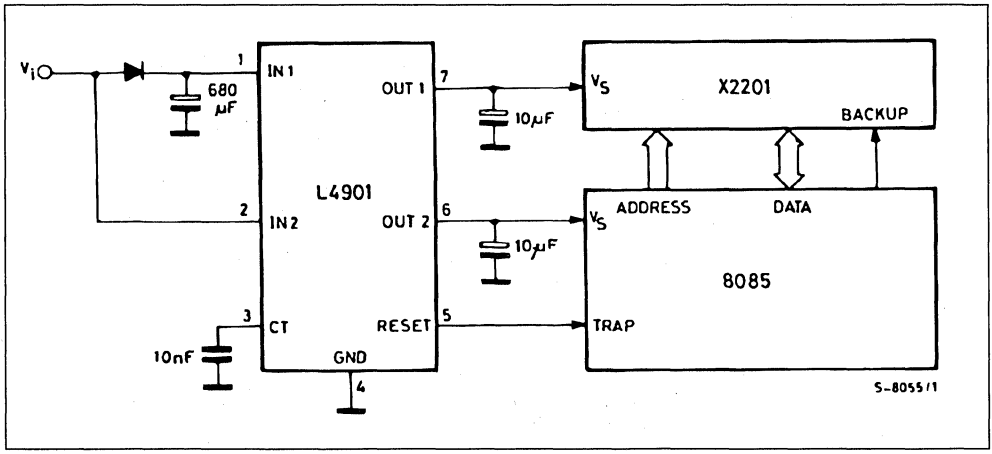
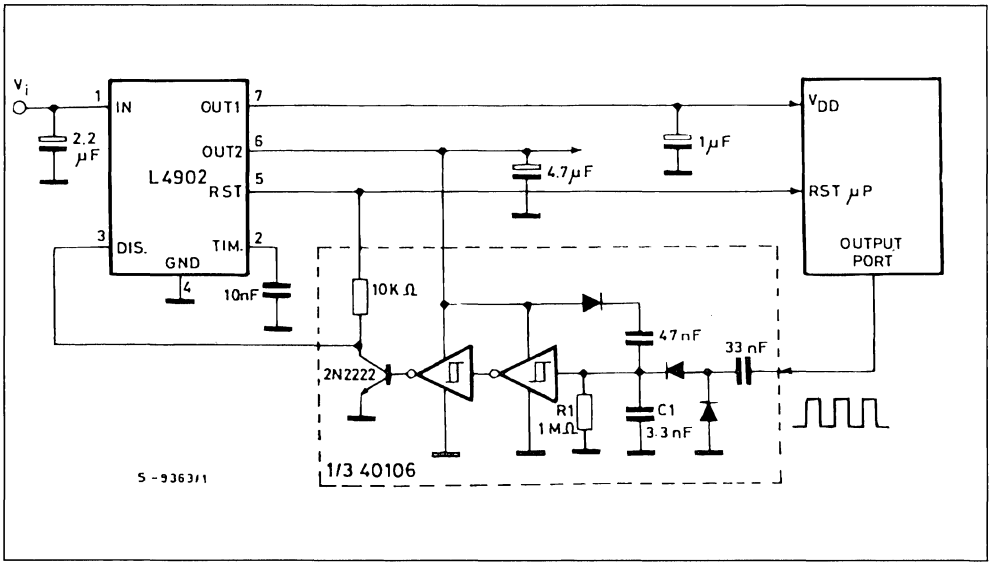


Figure 9 : With a CMOS Schmitt Trigger and a few Components a Watchdog Function can be added for Critical Application.



LOW DROP VOLTAGE REGULATORS FOR AUTOMOTIVE ELECTRONICS

By S. CISCATO

Linear voltage regulators with an input-output voltage drop of less than 2V are used to ensure continuity of the stabilized output in applications where a battery supply is used. This note describes the characteristics and operation of these devices.

Low drop linear voltage regulators are low voltage (5 to 12V) regulators which are able to provide effective stabilization of the output voltage even when the difference between input voltage and output voltage is less than 2V.

This situation can arise accidentally for a brief period when the main supply source is overloaded. It may also result from a deliberate design decision aimed at reducing the power dissipated in the supply - for example, when the device is used as a post regulator in portable instruments.

Low drop regulators are used widely in automotive applications, a field where integrated circuits have to be particularly rugged. For this reason most low drop devices include protection functions not found in standard regulators. Before describing the SGS THOMSON family of low drop regulators we will therefore begin with a brief description of the automotive electrical environment.

AUTOMOTIVE ENVIRONMENT

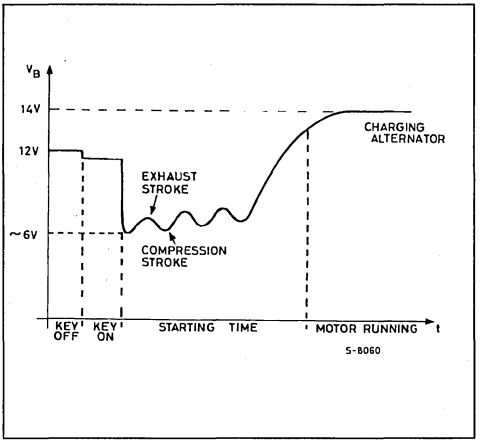
In addition to the battery voltage drop during starting, the automotive field presents a number of other serious problems concerning the regulator input voltage : positive and negative high energy / high voltage transients (load dump and field decay), positive and negative low energy/very-high-voltage spikes (switching spikes), battery reversal and battery voltage doubling.

All of these hazards must be withstood by the regulator without damage over an ambient temperature range very close to military standards (– 40 to + 125°C for underhood devices ; – 40 to + 85°C for other devices). Moreover, an output voltage precision of ± 4% to ± 2% is required over the whole temperature range and in all conditions of input voltage and load current.

BATTERY VOLTAGE DROP

During motor starting the battery is overloaded by a peak current of up to 100A drawn by the starter motor. In this condition, which persists for 20-30ms, the battery voltage drops to about 6V in very cold weather (figure 1).

Figure 1 : Cold Starting Supply Voltage Drop.



Using standard regulators with a dropout of 1.7V to 2.1V the minimum 4.75V supply necessary for essential functions such as ignition, injection and electronic engine control cannot be guaranteed. Another unfortunate consequence is the loss of RAM memory contents in car radios and trip computers.

A voltage regulator with a voltage drop of less than 1.2V is therefore necessary.

BATTERY VOLTAGE DOUBLING

To aid cold weather starting with a partially flat battery, sometimes two batteries are used in series, doubling the voltage. Regulators must therefore withstand input voltages of 24-26V without disturbing operation.

BATTERY REVERSAL

Voltage regulators must be protected internally against negative input voltages to guard against accidental battery reversal.

LOAD DUMP TRANSIENTS

Load dump transients are high voltage, high energy positive transients.

The response time of the output voltage of an alternator to load variations is very long because of the long time constant of the excitation winding and mechanical inertia.

When the load is reduced instantaneously (by turning off lights, cooling fans and so on) the output voltage of the alternator tends to present a positive peak, the amplitude of which depends on the speed of rotation and the excitation current.

During normal operation this does not cause problems because of the high capacity of the battery which, connected in parallel with the alternator output, is able to absorb the transient energy without a significant increase in voltage.

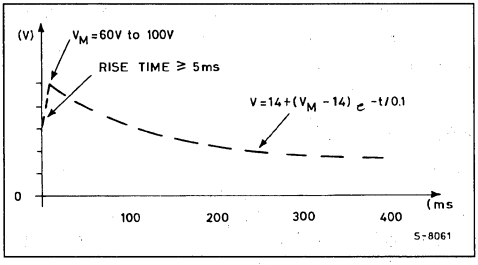
However, motor manufactures impose the standard that electronic devices must be protected against load dump transients because it is possible for the connection between battery and alternator to break.

The worst case voltage peak occurs when the battery-alternator cable is disconnected with the battery discharged and the motor running at its fastest rotation speed. In this case, the load variation is at a maximum and the voltage peak reaches a value comparable with the no-load output of the alternator running at maximum speed with the maximum excitation current.

Figure 2 shows a typical load dump waveform.

Motor manufacturers require that voltage regulators are able to protect themselves and the load against peak voltages of 60 - 100V with an equivalent series resistance of 0.1 to 1Ω , depending on the type of alternator and external protection device used.

Figure 2 : Load Drump Transient.



FIELD DECAY TRANSIENTS

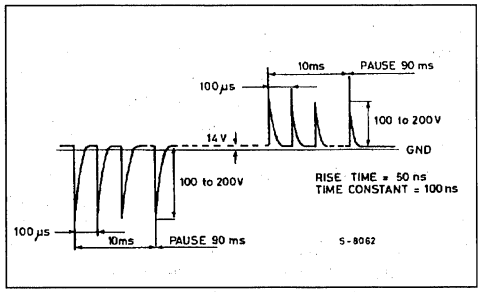
Field decay transients are high energy, high voltage negative transients.

If the ignition switch is turned off while current is flowing in inductive loads (electric motors, alternator field coil and so on) a negative voltage transient appears on the supply rail. The peak value in modulo of this transient is of the same order of magnitude as a load dump transient. In this case, too, the regulator must protect itself and the load.

SWITCHING SPIKES

Windscreen wiper motors, lamp flashers and ignition sparks behave as high frequency noise generators with an equivalent series resistance of 50 to 500 Ω. The energy associated with these transients is much lower than load dump or field decay transients but the negative and positive peaks can reach 200V. Figure 3 shows the voltage waveform which the regulators must withstand.

Figure 3 : Switching Spikes.



REGULATOR DESIGN

DROPOUT

The dropout voltage of a linear voltage regulator can be defined for a given output current, I_o, as the minimum difference between input and output voltage below which the output voltage is 100mV lower than the voltage measured at I_o with the nominal input voltage. The current I_o must be specified since the dropout voltage increases as the load current increases.

To obtain a dropout voltage of 0.05 to 1V with an output current of 10 to 50mA, the regulator types L387A, L487, L47XX, L48XX, L4920, L4921, LM2930A and LM2931A are configured with a PNP series-pass transistor as shown in figure 4. The PNP transistor is connected in the common emitter configuration and can therefore operate in saturation, yielding the low dropout voltage desired.

For higher dropout values an NPN series-pass element in emitter follower configuration may be used. This approach, shown in Figure 5, is used in the L2600 series regulators which have a maximum dropout voltage of 1.9V at 500mA.

Figure 4 : PNP Series Pass Transistor in Common Emitter Configuration for very Low Drop Out Voltage Regulators.

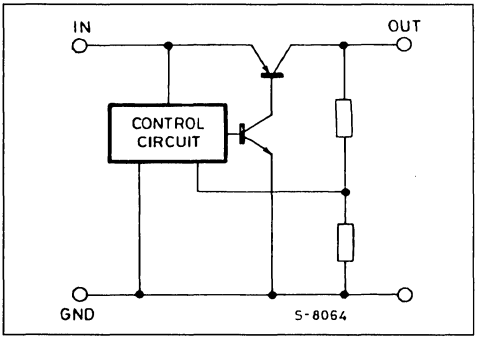
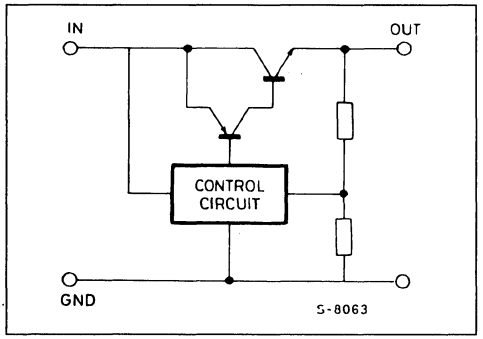


Figure 5 : NPN Series Pass Transistor in Emitter Follower Configuration.



CURRENT CONSUMPTION/QUIESCENT CURRENT

The circuit configurations shown in figures 4 and 5 behave differently as far as concerns the current consumed by the device but not delivered to the load. In the case of figure 5, this current is that necessary for the functioning of the auxiliary circuitry of the regulator (voltage reference, op amp and so on). The base current of the output transistor flows into the load.

In the Figure 4 circuit, in contrast, the base current of the output transistor does not flow through the load and, particularly in saturation, depends heavily on the load current.

Normally lateral PNP transistors are chosen for ICs because they can withstand high positive and negative overvoltages. When negative overvoltages at the input do not occur, or are eliminated by external protection devices, vertical PNP transistors can be used in place of lateral types.

Since vertical PNP transistors have higher gain the current consumed in the regulator is significantly reduced. Vertical PNP transistors will be used in future designs.

VOLTAGE REFERENCE

The wide operating range of input voltage (6 to 26V) and ambient temperature (40 to 125 °C) over which high output voltage precision is required means that a well stabilized voltage reference must be used.

All low drop regulators use bandgap type voltage references (see figure 6). In this structure the two transistors Q_2 and Q_1 have an emitter area ratio of 10 and carry equal collector currents imposed by the current mirror Q_3, Q_4, Q_5. In these conditions the base-emitter voltages of Q_1 and Q_2 differ (at 25 °C) by :

$$V_{BE} = \frac{KT}{q} \ln \frac{A(Q_2)}{A(Q_1)} = 60 \text{ mV}$$

where $\frac{A(Q_2)}{A(Q_1)} = 10$ (emitter area ratio)

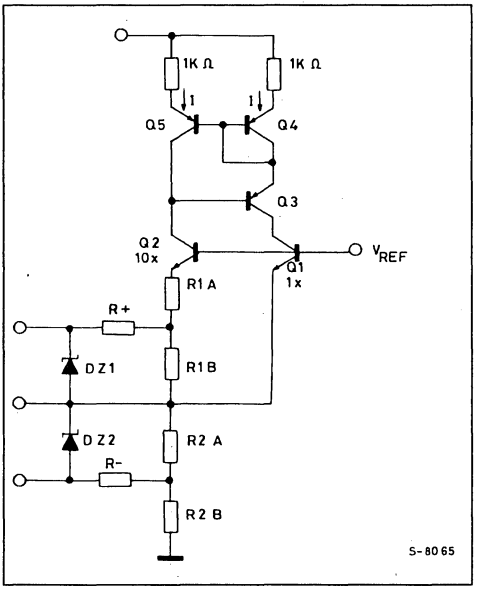
$\frac{KT}{q} = 26$ mV

K = Boltzmann's constant

T = Temperature in Kelvin

q = Charge on an electron

Figure 6 : Bandgap Voltage Reference Circuit in Low Drop Voltage Regulators.



The rejection of V_{ref} to variations in the supply voltage is improved by supplying the reference circuit from a stabilized voltage. This is achieved in the L26XX, L48XX, L4920, L4921, LM2930A and LM2931A regulators by means of a preregulator. In the L487, analysing the Figure 6 circuit gives :

$$V_{ref} = V_{BE}(Q_1) + 2\frac{R1}{R2}\Delta V_{BE}(Q_2, Q_1)$$

To maintain V_{ref} constant as temperature varies it is necessary that $\frac{d V_{ref}}{dT} = 0$ which implies choosing $\frac{R2}{R1}$ so that $\frac{2R2}{R1} \cdot \frac{60}{T(25\,^{\circ})} + \frac{dV_{BE}(Q_1)}{dT} = 0$

where $T(25\,^{\circ}) = 298$ K

$\frac{d V_{BE}(Q1)}{dT}$ = negative temperature coefficient of the base-emitter voltage.

In L387A and L47XX regulators, in contrast, the supply to the bandgap is switched from the input to the output as soon as the nominal output voltage is reached (figures 7, 8, 9). The variation in output voltage with temperature is shown in figure 10.

Figure 7: Block Diagram of L2600 Series Regulators.

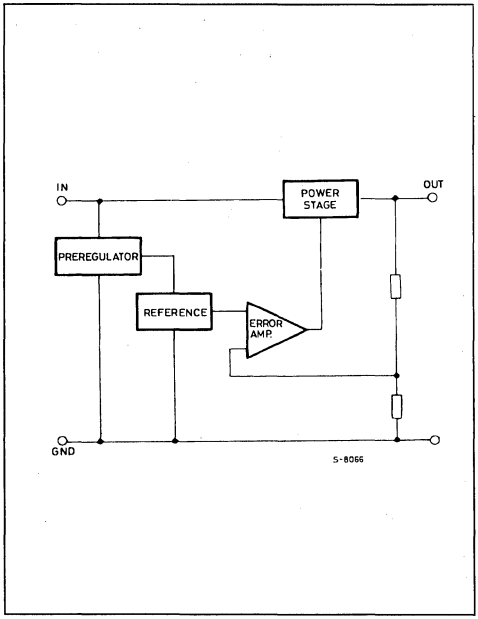


Figure 8 : Block Diagram of L387A and L487 Series Regulators.

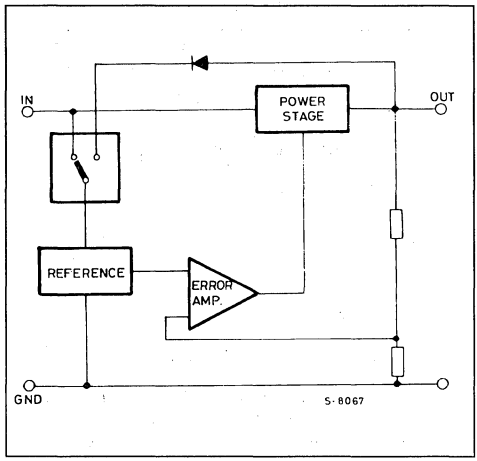


Figure 9 : Block Diagram of LM2930A, LM2931A and L4800 Series Regulators.

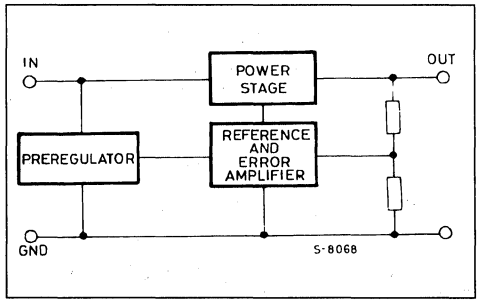
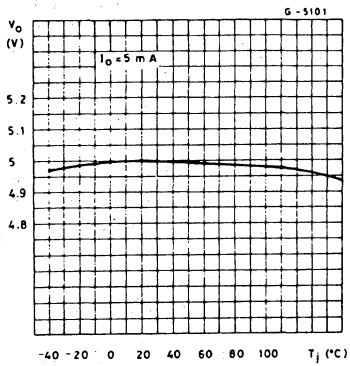


Figure 10 : Outputs Voltage vs. Temperature.



PROTECTION AGAINST HIGH ENERGY TRANSIENTS

To protect the LM2930A, LM2931A, L4920, L4921 and L48XX regulators against high-voltage, high-energy positive transients the basic circuit shown in Figure 11 is used. The zeners in this circuit limit the supply voltage to the maximum operating value and turn off the output stage. The output transistor can thus withstand voltages up to the BV_{CES} , breakdown voltage.

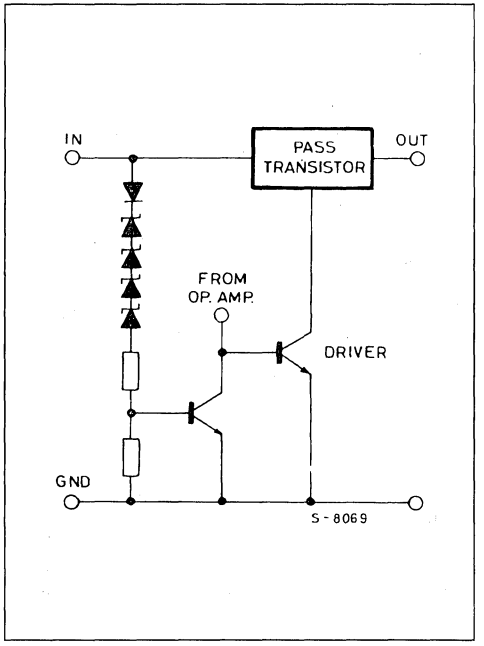
In the other regulators (L487, L387A, L47XX and L26XX) the supply to the internal circuits is also turned off.

The speed of intervention of these protection schemes is fast enough to ensure that the regulator can withstand high energy transients with a rising slope of 10V/µs without problems, interrupting normal operation only momentarily.

Protection against negative transients is provided by the high series impedance of the possible current paths and the reverse BV_{BEO} breakdown voltage of the lateral PNP transistors (BV_{CBO}).

The breakdown voltages BV_{CES} and BV_{CBO} depend on the technology therefore the transient capability is ± 60V, ± 80V or ± 100V for the various types.

Figure 11 : Overvoltage Protection Circuit.

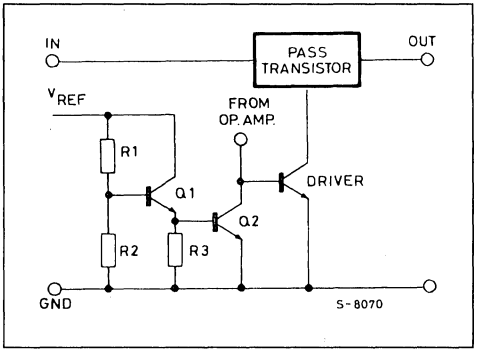


PROTECTION AGAINST LOW ENERGY OVERVOLTAGES

As shown in figure 3, the low energy overvoltages which the devices must resist have very brief rise time and can exceed the breakdown voltages. The protection schemes described above are therefore insufficient. However, since the energy associated with these transients is very low, the regulators can withstand them without problems. Nevertheless it is advisable to place a capacitor of around 100nF at the input.

All of the low drop regulators except the L26XX types need a compensation capacitor at the output. This capacitor also provides extra filtering for low energy transients because it has a low impedance at high frequencies.

Figure 12 : Thermal Protection Circuit.



THERMAL PROTECTION

When the junction temperature exceeds the safe maximum for the device a thermal protection circuit (figure 12) holds the output transistor off until the overtemperature condition has passed.

In the figure 12 circuit the resistors R1, R2 and R3 are calculated so that the base voltage of Q_1 is 600mV, thus preventing the conduction of Q_1 and Q_2.

As the junction temperature increases the minimum V_{BE} for conduction of the two transistors fall until, at about 15 °C, 2 V_{BE} = 600mV, the two transistors conduct and Q_2 turns off the output transistor driver.

CURRENT PROTECTION

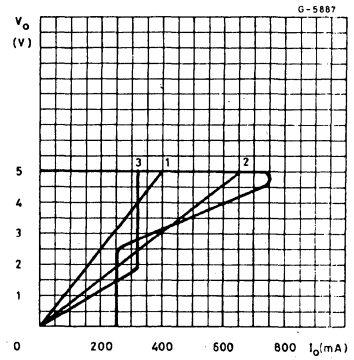
In the L487, L387A and L26XX regulators the output current is limited to its maximum value in the event of a short circuit. A special circuit acts on the base of the output transistor, preventing the output current from exceeding the limit set for the duration of the overload.

In the L4920, L4921, LM2930A, LM2931A and L48XX regulators a foldback circuit (figure 13) is used to limit the power dissipated in both the devices and the load in short circuit conditions. The current is limited to a low value (I_{sc}) of about 200 mA as soon as it exceeds the maximum value. The output voltage in this condition reaches a value corresponding to the current I_{sc} flowing through the load.

When the overload condition is removed the output voltage only returns to the nominal load value if the new static load line does not intersect the negative slope region of the curve in figure 13. If it does, the new operating point will be at the intersection.

It is important to note that when power is applied, if the load line intersects the curve in the negative slope region, the regulator will operate with a lower-than-nominal voltage. This can happen with a passive load greater than the normal load (even if it is less than the maximum load I_M) or with active loads such as a current sinker which draw more than I_{sc} even at low voltages (figure 13, curve 3).

Figure 13 : 1) Acceptable Load Line for Turn-on
2) Unacceptable Load Line for Turn-on.



EXTERNAL COMPENSATION

Since the purpose of a voltage regulator is to supply a fixed output voltage in spite of supply and load variations, the open loop gain of the regulator must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shifts due to other poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be the capacitor used to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequency too low to be compensated by a capacitor which can be integrated. For the L487, L47XX, L48XX, L387A, LM2930A and LM2931A external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The parassitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is 47 F (100 µF for L4800 series).

In the L2600, which uses an NPN power transistor, the stabilization capacitor is small enough to be integrated so no output capacitor is needed. Indeed, if an output capacitor is used it may cause oscillation unless it is greater than 100 µF, in which case it would itself be the dominant pole. If an electrolytic capacitor of more than 100 µF is used, a small capacitor must not be added in parallel or with the ESR of the electrolytic it would from another pole, worsening the stability of the system.

TURN-ON WITH CAPACITIVE LOADS

A load which presents a significant capacity between the output and ground (including the external compensation capacitor) will be seen by the regulator as a short circuit when power is applied. The regulator therefore delivers the short circuit current until the load capacitor has been charged to the nominal value.

This factor is extremely important for the dimensioning of the power source. Even a very small DC load can in such cases behave like a maximum load and the power drained from the supply is the sum of the short circuit current delivered to the load and the maximum current consumed in the regulator.

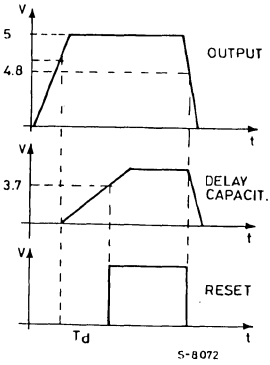
Moreover, as explained above, in regulators with foldback protection the static load line must not cross the negative slope region of figure 13 or the output voltage will not reach the nominal value when power is applied.

SPECIAL FUNCTIONS

RESET

The L387A and L487 include a power on/off reset function which inhibits the operation of circuits supplied by the regulator when the output voltage is too low (4.75V) to guarantee correct operation of logic (figure 14). To avoid malfunctions a delay is also introduced so that the enable signal is only issued some time after the safe output voltage has been reached.

Figure 14 : Reset Timing Waveforms.



The reset circuitry (figure 15) consists of :

- a comparator connected between the voltage reference and a tap of the output divider, the voltage of which is higher than the feedback voltage ;
- an SCR to memorize any brief glitches in the output voltage that can cause some trouble with the logic.
- a delay circuit with an external capacitor charged by an internal current source

This function has been integrated into the voltage regulator to exploit the basic advantage of taking information at the source. The use of double calibrations can thus be avoided.

For the correct operation of the reset function, two basic relations must be satisfied in all cases

$V_{res\ max} < V_{out\ min}$ (1)
$V_{res\ min} > 4.75\ V$ (2)

where $V_{res\ max}/V_{res\ min}$ are maximum/minimum value for the reset signal going high-low.

(1) means that the RESET signal must be high when the device is regulating

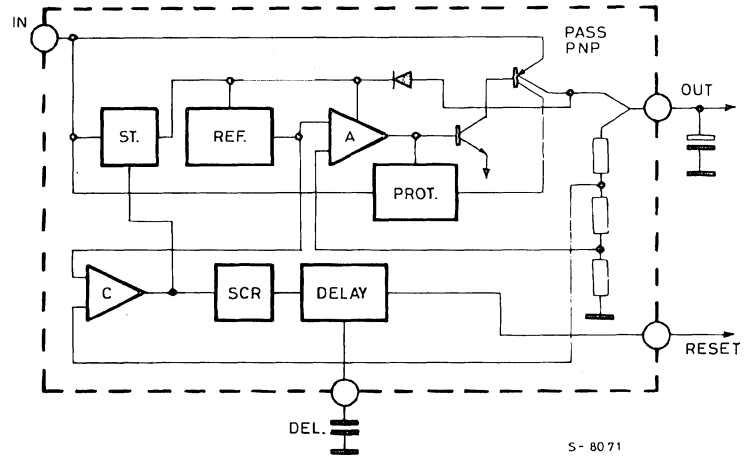
(2) means that the RESET signal must be low when the output voltage goes under 95 % of the nominal (5V). Expressions (1) and (2) can be rewritten as :

$(V_{res\ max} - V_{res\ min}) + (V_{nom} - V_{out\ min}) < V_{nom} - 4.75V$ (3)

This means that the sum of all the errors in the worst case must be less than 5 % (250mV).

- absolute spread of the reference
- error due to the load regulation (1 % max)
- error due to the offset of the reset comparator and error amplifier (0.5 %)
- errors due to the output divider (0.5 %)
- hysteresis of the comparator to speed up the transitions (50mV that is 1 % referred to 5V output)

Figure 15 : Schematic Block Diagram of a Voltage Regulator with Reset Function.

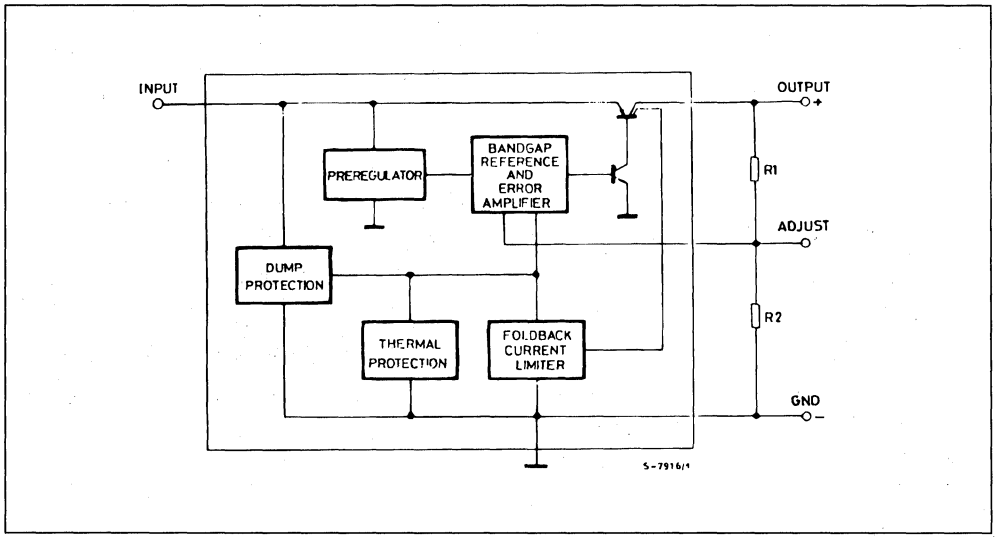


VARIABLE OUTPUT VOLTAGE

The L4920 and L4921 are structurally identical to L48XX series regulators except that the voltage divider in the feedback loop is available externally (figure 16). The output voltage can therefore be varied from 1.25V (the reference voltage) to 20V. It should be noted, however, that the minimum input voltage is 5.1V for operation with output voltages below 4.5V (otherwise the internal circuits will not work). For output voltages above 4.5V the input voltage must be at least equal to the output voltage plus the dropout voltage. The L4920 and L4921 are therefore low dropout regulators only for voltages above 4.5V.

A value of 6 KΩ is recommended for R2 to match the internal circuitry.

Figure 16 : The L4920 and L4921 are Structurally Identical to L48XX Series Regulators Except that the Voltage Divider in the Feedback Loop is Available Externally.



POWER MOS & IGBTS

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SAFE BEHAVIOUR OF IGBTs SUBJECTED TO dV/dt

by R. Letor, M. Melito

ABSTRACT

When an IGBT in the off state is subjected to a high dV/dt, parasitic turn-on can occur leading to additional losses.

This paper describes the phenomenon and indicates the main parameters influencing this behaviour.

Several methods of suppressing this parasitic phenomenon are described.

Using a suitable design of gate drive, it is possible to increase the circuit reliability in all conditions.

Practical examples and measurements are given.

INTRODUCTION

The behaviour of IGBTs subjected to a dV/dt differs according to the working conditions. We can consider two distinct cases:

- **static dV/dt**

  The static condition occurs when the dV/dt applied to an IGBT in the off state, acting through the reverse capacitance $C_g \approx C_{res}$, causes the gate voltage to rise turning the device on. This behaviour is typical of a circuit in bridge configuration, where the dV/dt is generated during complementary switch turn-on. This undesired effect generates

additional losses, mostly in devices in the off-state, due to the presence of both high voltage and high current on the collector. Parasitic turn-on must be avoided and this can be prevented by modifying the design of the drive circuit.

dynamic dV/dt

In this condition the dV/dt is applied to an IGBT during the recombination of minority carriers in the substrate and a peak current appears during the collector voltage rise time even if the gate and the emitter are in short circuit. The dynamic condition can occur when the IGBT works in thyristor mode, typically in a quasi resonant converter with a zero curent switch (QRC-ZCS). In this case the power losses depend on the device structure and on the converter resonant frequency. Thus, this phenomenon sets a limit to the operating frequency.

1. SPURIOUS TURN-ON IN STATIC dV/dT CONDITION.

1.1 Description of the Phenomenon.

The equivalent diagram of fig.1 shows current flow across the structure of an IGBT in the off-state when a rising collector-emitter voltage is applied.

The current through the reverse capacitance C_{gc} ($C_{gc} << C_{ge} \approx C_{res} \Rightarrow i = C_{res} \cdot dV/dt$), charges the gate capacitance; in this way, the gate voltage can reach the IGBT threshold voltage and a conduction current appears.

Photo 1 shows the waveforms during a spurious dV/dt turn-on giving prominence to the simultaneous presence of high voltage and high current.

If the output impedance of the drive source is high this phenomenon occurs more easily because of the higher ratio between the reflected V_{ge} and the applied dV/dt.

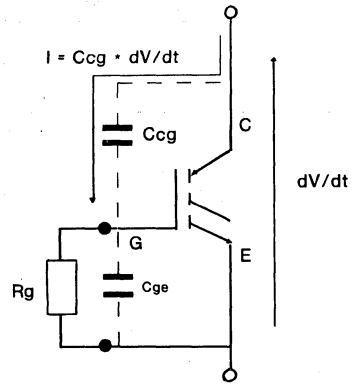


Fig.1 - Current flow through IGBT capacitances due to dV/dt

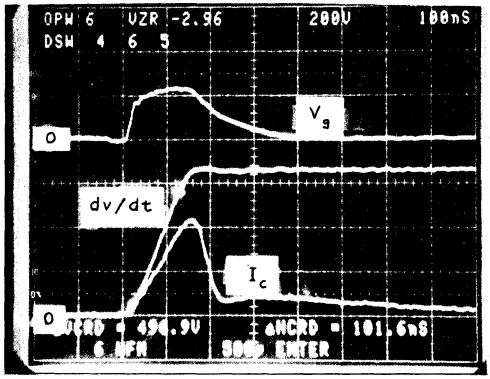


Photo 1 - Waveforms during a spurious turn-on due to static dv/dt condition.
Gate voltage = 2V/div,
Drain Voltage = 200V/div,
Drain current = 2A/div.

Thus the main parameters influencing an IGBT's behaviour in static dV/dt condition are:

- device characteristics (C_{res}, C_{ge}, V_{th}, g_{fs})
- temperature
- R_{ge}, dV/dt value
- gate bias

1.2 The influence of temperature.

When the temperature increases, IGBT parameters vary as follows:
- transconductance at low current increases
- threshold voltage decreases
- turn-off time increases

As a consequence, when the temperature increases the power losses due to dV/dt turn-on increase and the phenomenon occurs at a lower dV/dt value.
Photo 2 shows a comparison of the peak current at T_j = 25°C and T_j = 100°C with the same static dV/dt conditions.

1.3 The influence of dV/dt and R_{ge}.

The effect of R_{ge} and dV/dt can be evaluated with the simplified circuit in fig.2 but the mathematical resolution is not easy because of the influence of the voltage on C_{gc} and C_{ge}. The behaviour of SGS-THOMSON's IGBTs were characterized by the test circuit in fig.3, taking care to measure the energy dissipated in the devices at Tc = 100°C $E = \int v(t) \cdot i(t)dt$.

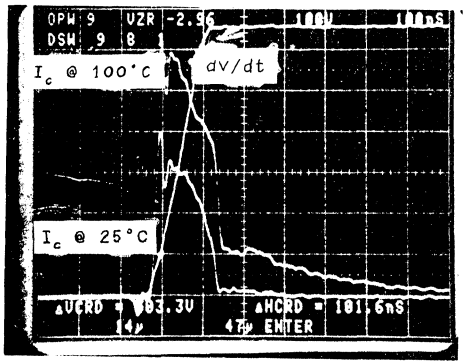


Photo 2 - Comparison between the peak current due to static dv/dt with Tc = 25°C and Tc = 100°C, ID = 2A/div, V_D = 100V/div, Rg = 100 W, E@25°C = 226 mJ, E@100°C = 1. 2m6 mJ

The curves in fig.4 show this measured energy versus both R_{ge} and a typical dV/dt.
Considering a single curve, dV/dt = constant, it can be observed that it has a minimum constant value for R_{ge} lower than the "knee" value.
In this region IGBT parasitic turn-on does not occur and the absorbed energy only charges the IGBT output capacitance.

1.4 The influence of gate bias.

Gate bias voltage influence was analyzed for negative voltage (V_{EE}) using the test circuit in fig. 3.
Figs.5 and 6 show that, when V_{EE} = -5V spurious turn-on does not occur even if the value of the resistance connected to the gate is high (180Ω). Looking at the waveforms in fig. 7 we can note two different effects on the gate voltage due to the negative bias. The first is obviously that the gate voltage is offset from V_{EE} and the second is that there is a different gate voltage peak even if the applied dV/dt is the same. This happens because of the influence of gate voltage on C_{ge}.
Photo 3 shows the gate charge curve and clearly demonstrates the variation of the slope

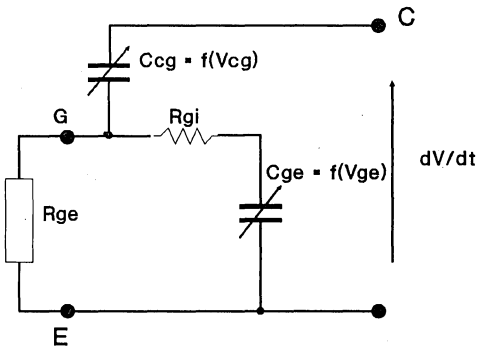
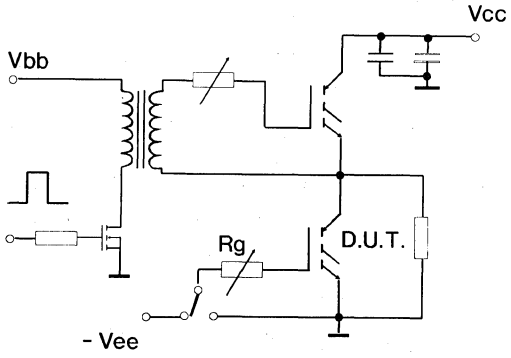


Fig. 2 - Simplified input circuit.



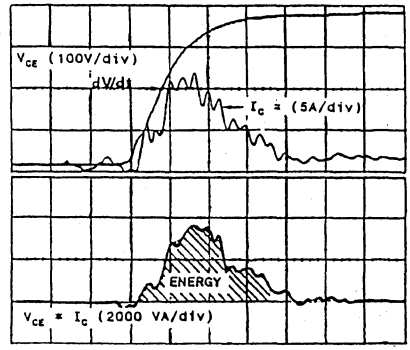


Fig. 3 - Test circuit and related waveforms

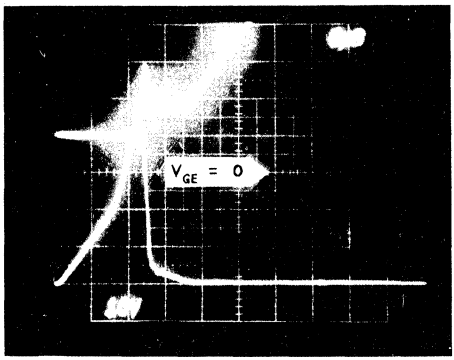


Photo 3 - Gate charge. Curve Vge = 2V/div. Vce = 100V/div

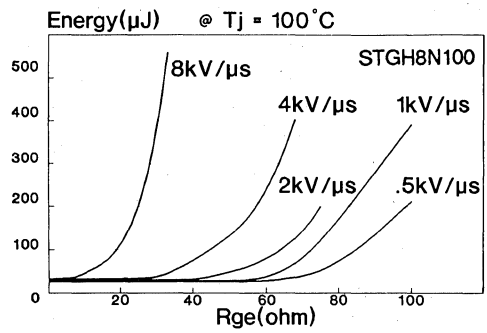


Fig. 4 - Energy dissipated versus R_{ge} and dV/dt

of the voltage occuring at V_{ge}=-2V. If V_{ge} is greater than this value then $C_{ge} = C_{ies}$ (input capacitance, output short circuited) if V_{ge} is lower than this then C_{ge} is about four times C_{ies} and reduces the gate voltage peak.

2. HOW TO AVOID PARASITIC dV/dt TURN-ON.

The previous paragraph shows that it is possible to avoid undesired turn-on during dV/dt by:

a) connecting gate and emitter by a low turn-off resistance

b) reducing dV/dt

c) biasing the gate, during the off state, with a negative voltage

2.1 LOW R_{ge} VALUE DURING THE OFF PHASE.

Depending on the required performance, this solution can be applied as follows:

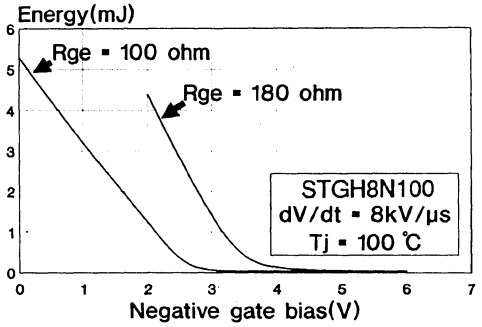


Fig. 5 - Dissipated energy versus negative gate bias and R_{ge}

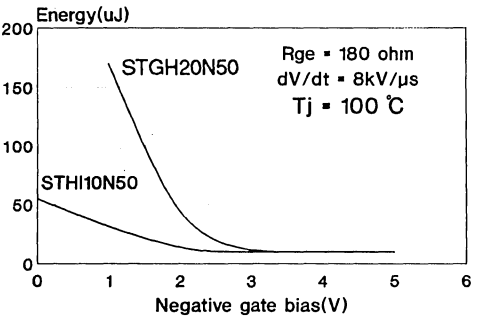


Fig. 6 - Dissipated energy versus negative gate bias

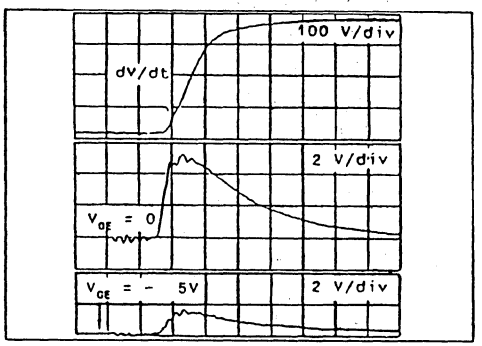


Fig. 7 - Comparison of gate voltage behaviour with and without negative bias

1) R_{ge} is the gate turn-off resistance as shown in fig.8a.

2) R_{ge} is connected just after turn-off as shown in fig.8b.

The disadvantage of the driving circuit shown in fig.8a is that this circuit does not guarantee the full safe operating area (RBSOA) when Rgs is less than 100Ω, for the following reasons:

- the latching current depends on dV/dt during turn-off
- R_{ge} strongly influences dV/dt at turn-off
- the RBSOA is guaranteed for R_g = 100Ω

Fig.9 shows this behaviour and the diagram in fig.10 shows that the maximum R_{ge} necessary to avoid dV/dt problem is less than 100Ω
Thus, the driving circuit of fig.9 is suitable for applications where the full safe operating area @ Rg = 100Ω is not required.
The driving circuit of fig.8b turns-off the IGBT with Rg = 100Ω obtaining the full RBSOA but the delay "d= $t_{storage}$ + t_{fall}" for each must be optimised for each application.

2.2 Reduction of dV/dt.

The spurious turn-on problem due to dV/dt is typical of the circuit shown in fig.11; in this circuit, the free-wheeling diode in the parallel with the lower IGBT, which is in the off state, is turned off during the upper IGBT turn-on and a high dV/dt is generated.
Thus, dV/dt value depends on :

- complementary IGBT turn-on speed (dI/dt)
- free-wheeling diode "softness"
- wiring inductances

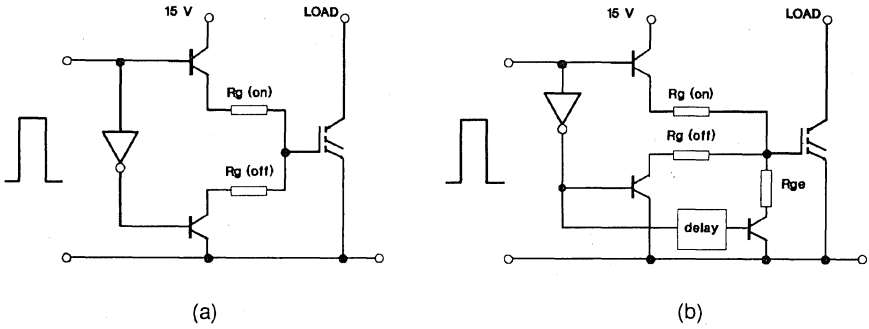


Fig. 8 - IGBT driving circuits

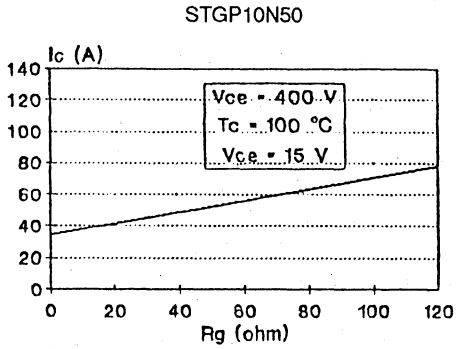


Fig. 9 - I_{latch} versus R_{goff}

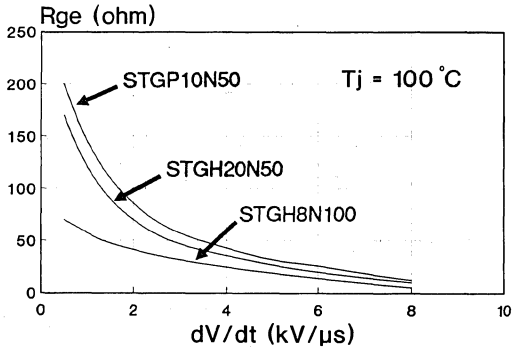


Fig. 10 -Max R_{ge} values that avoid static dV/dt turn-on versus dV/dt

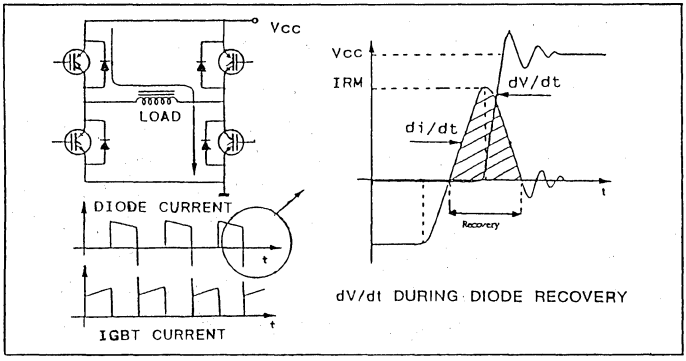


Fig. 11 - Typical circuit where static dV/dt conduction can occur.

Diode current recovery
during turn-off = 10A/div

Drain voltage and dv/dt
due to the diode turn off 200V/div.

Current due to spurious
turn-on with Rgs = 100 Ω2A/div

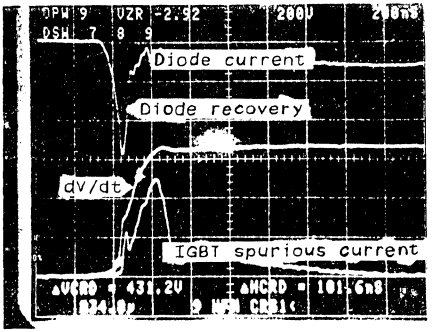


Photo 4 - Waveforms in the circuit of fig. 11 when: R_{gon} = 100 Ω

Diode recovery = 5A/div.

Dv/dt due to diode turn-off 200V/div.

Current in the IGBT in off state 2A/div.

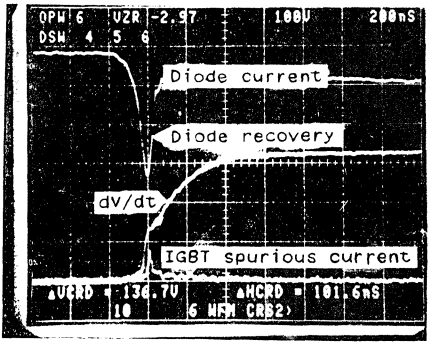


Photo 5 - Waveforms in the circuit of fig. 11 when R_{gon} = 200Ω. In this condition turn-on due the dv/dt does not occur.

and it can be minimized:

- using fast soft recovery diodes.
- reducing wiring length.
- turning on IGBTs slowly, with a high value of turn-on gate resistance.

Photo 4 and 5 show that the dV/dt is reduced to a safe value in the circuit of fig.11. Photo 4 uses a low value of turn-on gate resistance whereas photo 5 uses a high value gate resistance. In the case of photo 5 spurious turn-on due to the dV/dt does not occur.

2.3 driving the IGBT with a negative voltage.

Biasing the gate negatively, as shown in photo 6, causes a higher dV/dt during turn off because of the availability of a large gate current. It is possible to avoid this drawback, which reduces the effective RBSOA, simply by increasing the value of $R_{g(off)}$.

3. DYNAMIC dV/dt.

This condition may occur in a zero current quasi resonant converter where the IGBT works as a thyristor.
In this application, see fig. 12 and photo 6 the IGBT is turned-off when the collector current is zero and the collector voltage starts to rise after a delay time $t_d \approx (2 * f_{resonance})^{-1}$, corresponding to the end of the reverse recovery phase of the antiparallel diode.
This increasing voltage causes a current spike, leading to power losses because of the minority carriers in the IGBT substrate. The amplitude of the spike depends on several factors which involve both IGBT and circuit characteristics. One of the factors is the amount of the stored charge when the dV/dt is applied. The stored charge depends on the type of IGBT (slow or fast), junction temperature and resonant frequency.
Increasing temperature and/or frequency leads

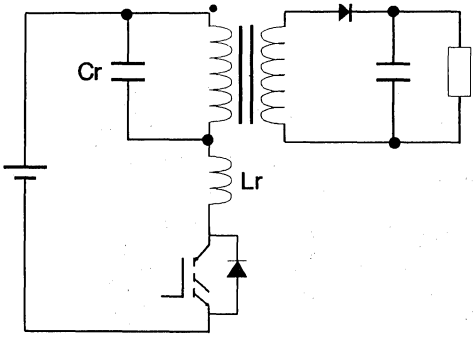


Fig. 12

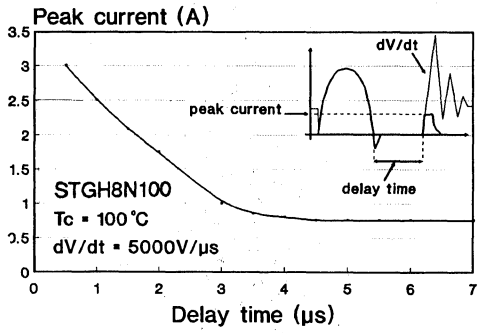


Fig. 13 - Peak current versus t_{delay}

Gate voltage = 10V/div

Drain current = 2A/div

Drain voltage = 200V/div

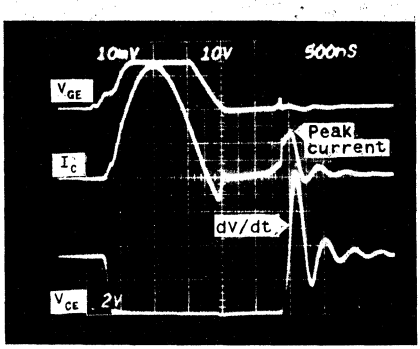


Photo. 6 - Waveforms in a resonant converter where dynamic dv/dt occurs. Device = STGH8N100, Tc = 100°C

to a higher current peak. The diagram in fig.13 shows how increasing resonant frequency affects the current peak.

For frequencies lower than about 120 kHz the current peak is constant, because there is no more stored charge and due solely to capacitive effects that are similar to those in Power MOSFETs.

The other factor is related to the rate of voltage rise which depends strongly on the softness of the diode. Using a slower IGBT emphasizes the effects discussed above. In low frequency working conditions the power losses are no longer negligible and must be considered during the circuit design in order to avoid thermal runaway and consequent device failure.

4. CONCLUSION.

The dV/dt phenomenon causes power dissipation in IGBT devices and this may lead to the failure due to thermal runaway. The way to avoid this phenomenon depends on the operating conditions.

When an IGBT works in a static dV/dt condition, as for example in a bridge circuit, it is possible to prevent the dV/dt phenomenon by modifying the design of the IGBT drive circuit:

- reducing dV/dt.
- connecting a low gate-emitter resistance.
- driving the IGBT with a negative voltage at turn-off.

If a high current is to be controlled with a switched mode technique, it is necessary to design the drive circuit to obtain the full guaranteed RBSOA.

When the IGBT works in dynamic dV/dt condition, as in a QRC-ZCS, it is not possible to avoid power dissipation in the device by optimization of the drive circuit. These kind of losses can only be limited by selecting a suitable converter resonant frequency and antiparallel diode.

STATIC AND DYNAMIC BEHAVIOUR OF PARALLELED IGBTs

by R. Letor

ABSTRACT

Problems associated with power device characteristics when power devices are connected in parallel, such as thermal stability and balanced switching behaviour can be solved by using insulated gate bipolar transistors (IGBT).

This note deals with parallel IGBT behaviour analyzing both static and dynamic characteristics.

The influence of heatsink mounting, lay-out, and drive circuit are described in order to demonstrate the best way to parallel IGBTs for optimum performance.

In addition the major advantages of the ISOTOP package are shown.

I. INTRODUCTION

When switching devices are paralleled, the following points must be carefully considered:

1) On-state losses balance.
2) Switching losses balance.
3) Thermal stability.

The loss unbalance, depending mainly on the spread of the device parameters (V_{CEsat}, switching time), can cause excessive power dissipation in one or more devices.

The thermal instability, correlated to the behaviour of the devices when the temperature increases, can cause thermal runaway and lead to the failure of the device. This note explains the theory, describes practical examples and suggests possible solutions.
The behaviour of the IGBTs considered is not dependent on type, hence, the results can be extended to all SGS-Thomson IGBTs.

II. BEHAVIOUR OF PARALLELED IGBTS IN THE ON STATE.

The IGBT is a voltage driven device, hence when the devices are in parallel the drive conditions are the same for all devices (i.e. they all have the same V_{GE}).
Thus the influence of output characteristics and of the transfer characteristics can be studied separately.

A. Current balance in the on state.

Current balance can be studied with the simplified circuit of fig.1 where the following conditions are respected:

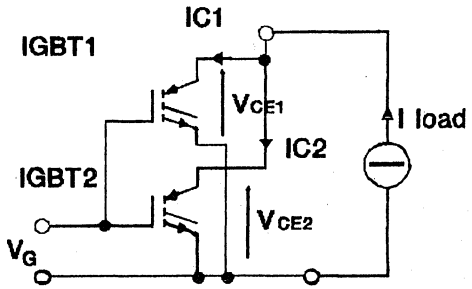


Fig. 1. Circuit where current balance depends only on IGBT characteristics.

$$V_{CEsat1} = V_{CEsat2}$$
$$I_{C1} + I_{C2} = I_{LOAD}$$
$$V_{CEsat1} = f(I_{C1}, T_{j1}, V_{GE1})$$
$$V_{CEsat2} = f(I_{C1}, T_{j2}, V_{GE2}) \quad (1)$$

This system of equations (1) has a graphical solution which is shown in fig.2 for the extrapolation of current balance in two paralleled IGBTs with the same junction temperature ($T_{j1} = T_{j2}$).
Figure 3 shows the influence of the spread of V_{CEsat} on the current balance.

B. The influence of the temperature on current balance.

The fig.4 shows the basic equivalent structure of the IGBT.
The device functions as a bipolar transistor which is supplied base current by a Power-MOSFET.
The IGBTs output characteristic combines both the bipolar and the Power-MOSFET characteristics.

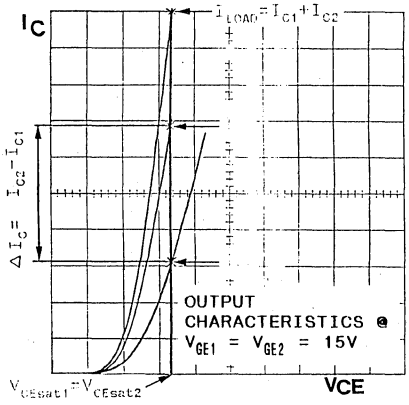


Fig. 2. Graphical extrapolation of current balance in the on state for two STGP10N50 @ I_{LOAD} = 10A; $T_{j1} = T_{j2}$ = 25°C; I_C = 1A/div.: V_{CE} = 0.5V/div.

The curves in fig.5 show these effects and highlight the following points:

1 - The temperature coefficient of V_{CEsat} is negative at low current density ($I < I_{NOM}$) (bipolar effect).

2 - The temperature coefficient of V_{CEsat} is positive at high current density ($I > I_{NOM}$) (Power-MOSFET effect).

3 - The temperature coefficient of the dynamic resistance (di/dv) is positive (Power-MOSFET effect).

The effect of this behaviour is that the influence of the temperature on current balance is small and that the current balance improves when the temperature increases, if $T_{j1} = T_{j2}$ ($\Delta T_j = 0$), (fig.6).

Figure 7 shows the effect on current balance when the junction temperature of paralleled devices are different ($\Delta T_j = 0$) and the medium temperature is constant $(T_{j1} + T_{j2})/2=K$:

- At low current, current balance is worst when the temperature difference increases, but the temperature coefficient is low.

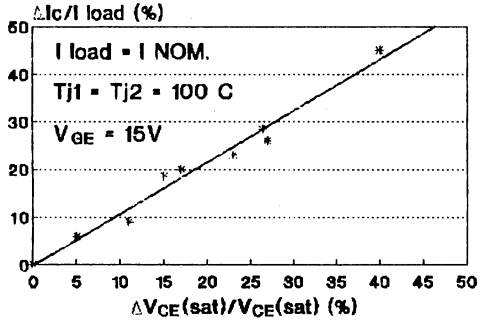


Fig. 3. Current balance versus the $V_{CE}(sat)$ difference in two paralleled IGBTs.

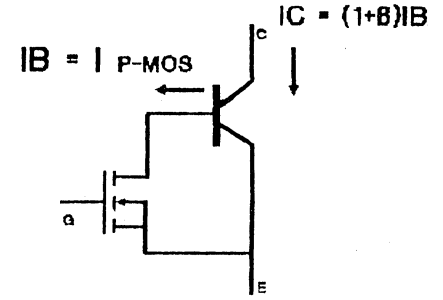


Fig. 4. Simplified equivalent circuit of an IGBT.

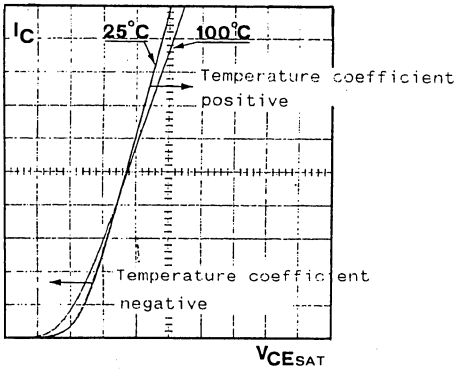


Fig. 5. Output characteristics versus the temperature for STGP10N50. I = 2A/div.; V = 0.5V/div.

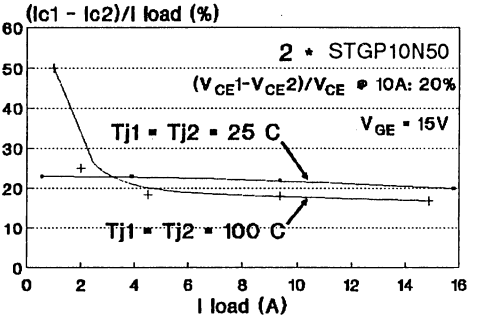


Fig. 6. Current balance versus I_{LOAD} and temperature in two paralleled IGBTs.

- At high current the behaviour is similar to the power- MOSFET behaviour; in fact, current balance improves when the temperature difference increases.

C.INFLUENCE OF THE TRANSFER CHARACTERISTICS.

When IGBTs are strongly saturated, the influence of the transfer characteristics on paralleled devices behaviour is small.
The figure 8 shows that the gate voltage scarcely influences the V_{CEsat} value; hence it is not possible to improve the current balance in the on-state by connecting an emitter-ground resistance.

III. PARAMETERS INFLUENCING SWITCHING BEHAVIOUR.

The IGBT's switching behaviour depends on:

- Device parameters (V_{th}, g_{fs}, C_i, C_{rss},C_o).
- Drive circuit.
- Lay-out (Parasitic inductances).

The switching behaviour is studied in the circuit of figure 9 where the stray inductance "L_{s1}+L_{s2}+L_{s3}" is small and the IGBTs are turned on, while the free wheeling diode is still conducting; with this working condition di/dt is not limited by the stray inductances and depends on the IGBTs switching speed

$$(dI/dt \gg Vcc/(L_{s1} + L_{s2} + L_{s3}).$$

A. Turn-on.

During turn-on, the switching losses depend mainly on the di/dt that influences the peak current due to the diode recovery (Eco ≈ Ipeak * tcross * Vcc/2).
In the circuit of figure 9, the voltage drop caused by the inductance of the emitter-ground connection (L_{s1}), reduce the drive current ($I_G = (Vd - V_G - L_{s1} * di/dt) / R_G$), and acts as a negative feedback during current rise time. Taking into account the effect of L_{s1}, the value of di/dt is:

$$di/dt \approx (Vd-V_{th}) / (R_G C_i / g_{fs} + Ls1)$$

For 1000V devices and with RG = 100Ω:

$$15 * 10^{-9} < R_G C_i / g_{fs} < 25 * 10^{-9}$$

The inductance of 1cm of wiring is:

$$L_{s1} \approx 10 * 10^{-9} \text{ H/cm}$$

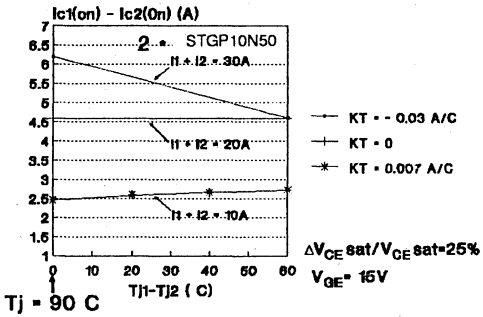


Fig. 7. Influence of ΔT_j on current balance during the ON-state. KT is a temperature coefficient.

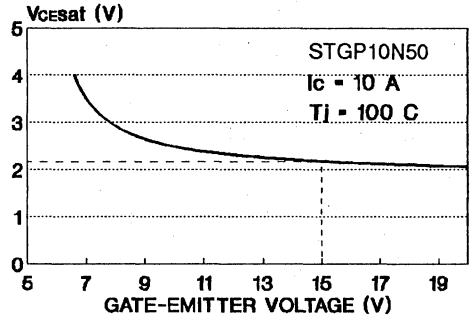


Fig. 8. Typical V_{CEsat} versus gate bias.

From this it can be seen that the spread of device parameters has less influence on the di/dt value than the parasitic inductance of the emitter-ground connection.

B. Fall.

During current fall two distinct phases can be seen (figure 10).
Phase 1 is similar to the current fall of power-MOSFET and the parameters influencing the di/dt are the same parameters that influence di/dt during turn-on.
The tail during phase 2 which is due to the minority carriers stored in the substrate mainly affects the switching losses.
The tail amplitude depends on Tj and on the turn-off current; hence, the turn-off current and the working temperature mainly influence the losses during the fall time (Fig. 11,12).

C. Storage.

During the storage time "$I_C = g_{fs}\ (V_{GE}-V_{th})$", "di/dt ≈ 0", and the current waveform depends only on the IGBTs parameters (g_{fs}, V_{th}) and on the drive circuit.

IV. PARALLELED IGBT'S SWITCHING BEHAVIOUR.

The influence of the drive circuit, of the lay-out and of the device parameters was verified using the following conditions:

- 1 Gate drive with separate gate resistances (fig.13).
- 2 Gate drive with one gate resistance (fig.14).
- 3 Unbalanced emitter-ground wiring connection (fig.15).
- 4 Paralleling devices with the maximum spread of the parameters.

The voltage and collector current waveforms are stable in all conditions, even in the worst case condition where the gates are driven with a common resistance and the wiring inductances are strongly unbalanced

A. Turn-on.

Photo 1,2 show that the drive circuit influence on peak current balance is small and photo 3 shows that the peak current unbalance is significant in condition 3, where $\Delta L_{s1} = 0.15\mu H$.

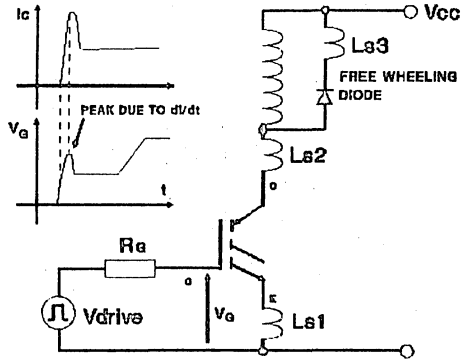


Fig. 9. Circuit showing the parasitic inductances influencing the switching behaviour.

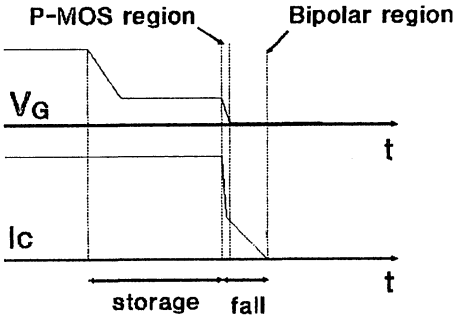


Fig. 10. Gate voltage and current waveforms during turn-off time.

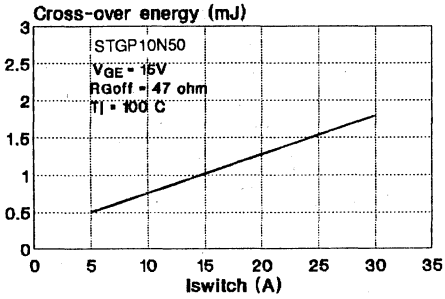


Fig. 11. Switching losses at turn-off V_s turn-off current.

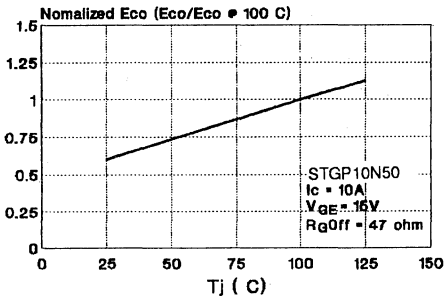


Fig. 12. Influence of temperature on turn-off losses.

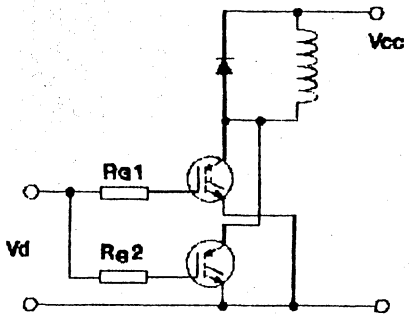


Fig. 13. Driving with separate gate resistance.

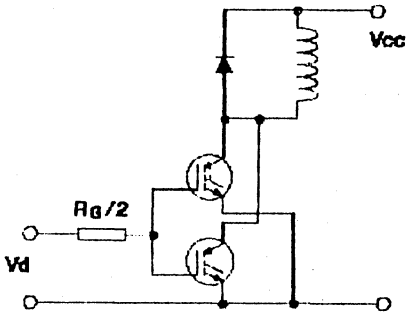


Fig. 14. Driving with one gate resistance.

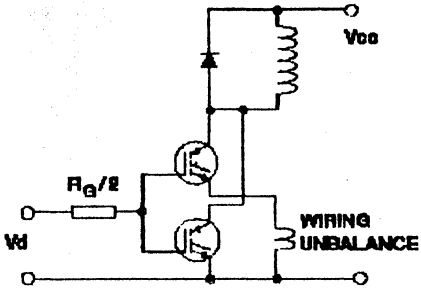


Fig. 15. Emitter ground wiring unbalance.

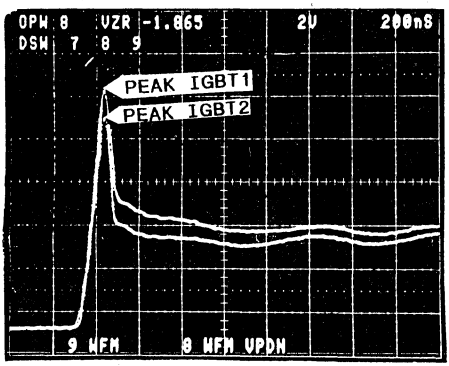


Photo 1. Turn-on with separate gate drive (fig. 13) of an STGH8N100; I = 2A/div., t = 200ns/div.

IGBTs with the maximum difference in parameter values were paralleled; the comparison of current waveforms in photo 1 and 2 demonstrates that the influence of parameter spread is low ($L_{s1} \approx 30$ nH).

B. Fall.

Photo 4 and 5 show that the wiring inductance unbalance affects only the power-MOSFET phase; but this behaviour creates negligible switching loss unbalance in comparison to the total turn- off switching losses.
The current unbalance just before current fall that affects the tail amplitude can create significant switching loss unbalance (see fig 17).

C. Storage.

During the storage time, the spread of the IGBTs parameters (g_{fs}, v_{th}) and the difference

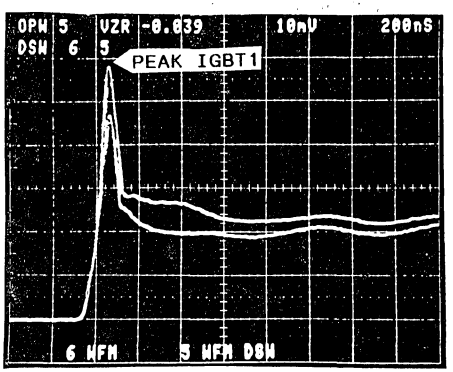


Photo 2. Turn-on with one gate resistance (fig. 14) of an STGH8N100; I = 2A/div., t = 200ns/div.

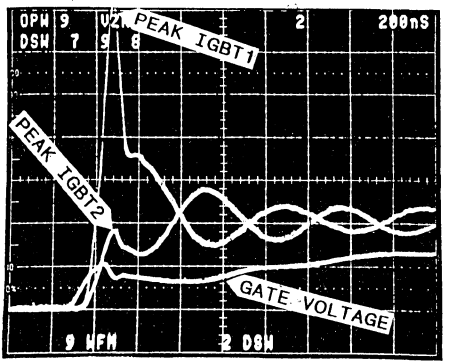


Photo 3. Turn-on with unbalanced emitter-ground wiring (fig. 15) of a STGH8N100; I = 2A/div., t = 200ns/div.

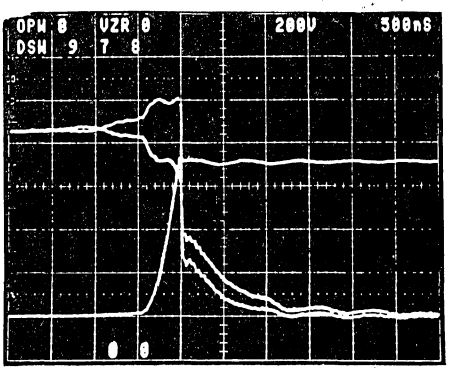


Photo 4. Turn-off with balanced gate-emitter wiring (fig. 14) of a STGH8N100; I = 2A/div., V = 200V/div., t = 500ns/div.

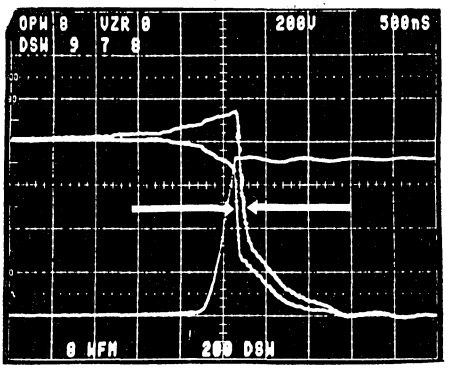


Photo 5. Turn-off with unbalanced emitter-ground wiring (fig. 15) of a STGH8N100; I = 2A/div., V = 200V/div., t = 500ns/div.

between storage times causes current unbalance thus creating switching loss unbalance.

Photo 6 shows the effect of the storage time differences when the gates are driven with separate gate resistances.

The collector current begins to fall in the device with the smaller storage time, consequently the current increases in the other IGBT so increasing storage current unbalance.

Driving the gates with only one gate resistance minimize this effect (photo 7); the device with the higher storage time hold the gate voltage to "$V_{th}+g_{fs}I_C$" until the fall time phase, so equalizing the storage times.

Current unbalance due to the IGBTs parameter spread can be calculated with the equations (2) and (3).

The curves of fig.16,17 show, respectively , storage current unbalance and the consequent switching loss unbalance between two devices where the V_{th} and g_{fs} values are the limits of the parameter spread.

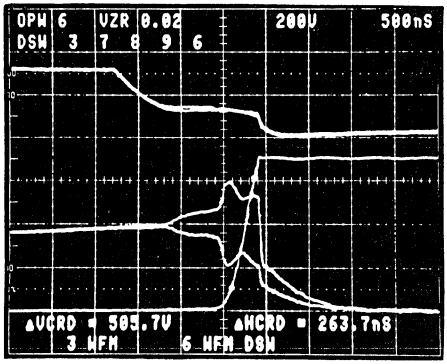


Photo 6. Effect of separate gate drive on storage current waveform. I_C=2A/div., V_{CE}=200V/div., V_{GE}=10V/div., t=500ns/div.

$$I_{load} = I_{1st} + I_{2st} = V_{GE}\,(g_{fs1} + g_{fs2}) - (g_{fs1}V_{th1} + g_{fs2}V_{th2}) \quad (2)$$

$$I_{storage} = I_{1st} - I_{2st} = V_{GE}\,(g_{fs1} - g_{fs2}) - (g_{fs1}V_{th1} - g_{fs2}V_{th2}) \quad (3)$$

V. THERMAL STABILITY.

When IGBTs are connected in parallel the on-state current is greater in the device with the smaller V_{CEsat} (fig.2); thus, the power dissipation and the junction temperature is higher in this device.

This phenomenon can cause a thermal instability because of the following reasons:

- Current unbalance increases when junction temperature difference increases (fig.7).
- Switching loss unbalance increases when junction temperature difference increases (fig.12).

The thermal stability can be achieved by mounting the paralleled IGBTs on the same heatsink; in this way the heatsink works as a negative feedback, because it transmits the heat from the device with the higher T_j to the device with the lower T_j so reducing the junction temperature difference.

In the ideal case where the thermal resistances ($R_{thj\,h}$,$R_{th\,x}$) are null, the thermal stability is assured because the devices work at the same temperature and the current balance improves when the temperature increases as shown in fig.6.

In real conditions the thermal resistances "R_{thjh}" are not negligible and the thermal stability can be studied with the equivalent thermal circuit of fig.18 which can be simulated with the system shown in fig.19.

The behaviour of the system near the final working point, is simulated using two paralleled IGBTs driving a constant inductive load; the devices are only active when the

heatsink temperature is uniform and at the final temperature which is independent of the current balance as the equations (4),(5),(6), (7),(8) show.

$$(T_{heatsink}=T_{amb.}+R_{th\ h\text{-}amb.}(V_{CE(sat)}(I_{C1}+I_{C2})+ \text{Switching losses}) \approx \text{const.} \quad (4)$$

$$I_{C1} + I_{C2} = I_{LOAD} = \text{const.} \quad (5)$$

$$V_{CEsat} \approx \text{const.} \quad (6)$$

$$\text{Switching losses} \approx \text{const.} \quad (7)$$

$$T_{amb.} = \text{const.} \quad (8)$$

The stability was evaluated with the following conditions:

- heatsink temperature constant (load constant).
- Initial junction temperature equal to the heatsink temperature (100°C).
- Turn-off current unbalance constant and equal to the maximum value (worst case).
- Thermal capacitances disregarded.

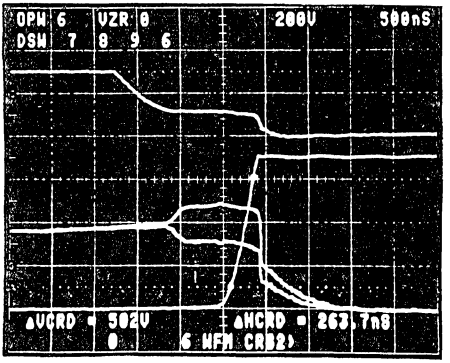


Photo 7. Turn-off with one gate drive resistance; I_C=2A/div., V_{CE}=200V/div., V_{GE} = 10V/div., t = 500ns/div.

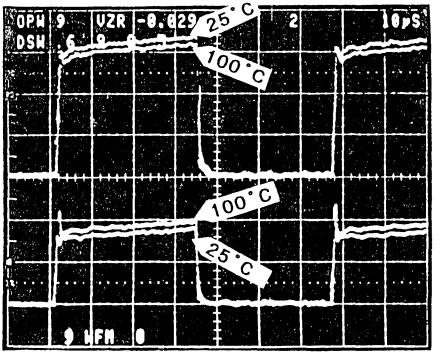


Photo 8. Comparison of current balance at T_j=25°C and 100°C; I_C=2A/div., t=10µs/div.

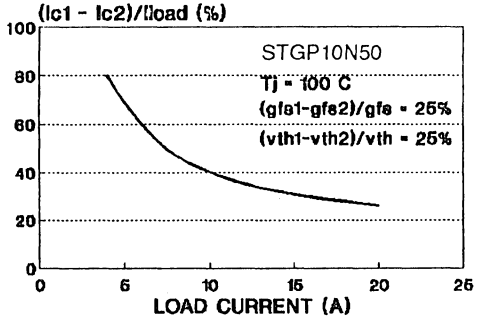


Fig. 16. Storage current unbalance versus load current.

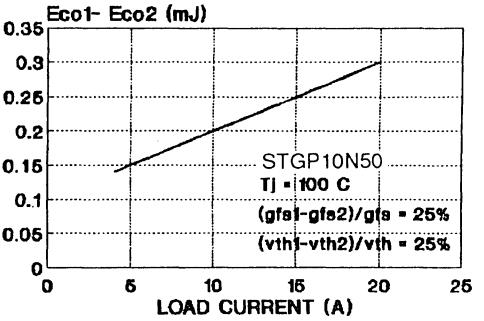


Fig. 17. Switching losses unbalance due to storage current unbalance.

The blocks in fig.19 signify the following computations:

1 - calculates initial current unbalance ($\Delta T_j = 0$) depending on the output characteristics of paralleled IGBTs.

2 - Calculates junction temperature difference depending on the on-state current unbalance (ΔI_{on}) and on switching current unbalance (ΔI_s).

$$\Delta T_j = R_{thjh} * (\Delta \text{ Power dissipation}).$$

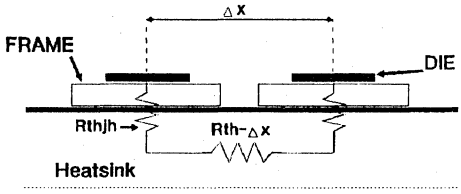


Fig. 18. Equivalent thermal circuit.

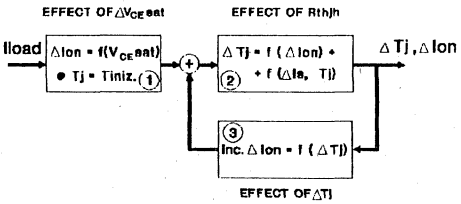


Fig. 19. Simulation of the temperature changes for two paralleled IGBTs.

3 - Calculates the growth of current unbalance (incr.ΔI) due to junction temperature difference (fig.16).

If $R_{th\,x}$ is negligible ($R_{th\,x} << R_{th\,jh}$):

$$f(\Delta I_{on}) = R_{th\,jh} * \Delta Pd_{on} =$$

$$R_{th\,jh} * V_{CEsat} * (t_{on}/T) * \Delta I_{on} = K_R * \Delta I_{on} \quad (9)$$

$$f(\Delta I_S, \Delta T_j) = R_{th\,jh} * Pd_{switching} =$$

$$R_{th\,jh} * f * \Delta E_{co}(\Delta I_S, \Delta T_j) \quad (10)$$

$$\Delta E_{co}(\Delta I_S, \Delta T_j) = \Delta E_{co}(\Delta I_S, 100°C) *$$

$$* (1+\Delta T_j * K_S) \text{ (see fig.12,17)} \quad (11)$$

$$\text{incr } \Delta I_{on} = K_T * \Delta T_j \text{ (see fig.7)} \quad (12)$$

The equation (13) is the transfer function of the system.

$$\Delta T_j = K_R * \Delta I_{on} + R_{th\,jh} * f * \Delta E_{co} /$$

$$(1-(K_R * K_T + K_S * R_{th\,jh} * \Delta E_{co} * f)) \quad (13)$$

Thermal stability is guaranteed if the equation (14) is true.

$$(K_R K_T + K_S R_{th\,jh} * \Delta E_{co} * f) < 1. \quad (14)$$

A. Example of two paralleled STGP10N50FI (Fully insulated package).

Conditions: $f = 15KHz$

$I_{LOAD} = 10A$

$\Delta V_{CEsat}/V_{CEsat} = 20\%$

$R_{th\,jh} = 3.5°C/W$

$t_{on}/T = 0.5$

Parameters	Reference
$\Delta E_{co} = 0.2$ mJ	See fig.17
$K_S = 0.005/°C$	See fig.12
$K_T = 0.007$ A/°C	See fig.7

$K_R = 3.5$ $K_R = 2\ R_{th\ jh} * t_{on}/T$

$\Delta I_{on}\ (\Delta T_j=0) = 2A$ See fig.3

$V_{CEsat} = 2V$

Solution of the equations (13) and (14):

$$K_R K_T + K_S * R_{th\,jh} * \Delta E_{co} * f) = 0.08 << 1 \quad (15)$$

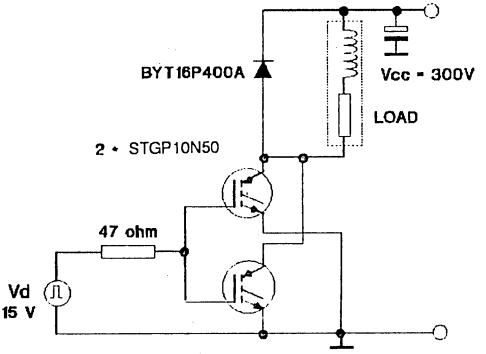


Fig. 20. Chopper circuit where paralleled IGBT behaviour was checked.

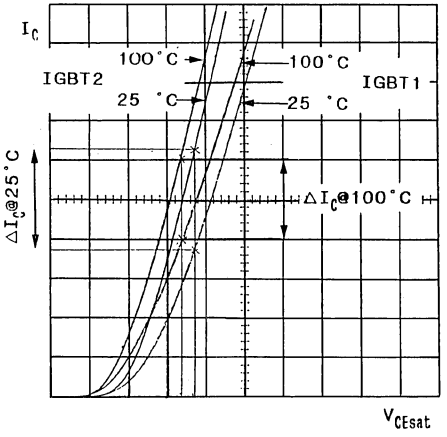


Fig.21. Output characteristics of the devices in fig. 20 and estimation of current balance at $T_{j1} = T_{j2} = 25°C$ and 100°C.

$\Delta T_j = 19°C$ (16)

$\Delta Ion\ (\Delta T_j = 19°C) = 2.13\ A$ (17)

The equations (15) (16) (17) show that the thermal stability is very high even when the devices are insulated and switching loss unbalance is high (worst case).

The conditions studied in this paper were carried out by mounting the paralleled devices in the chopper circuit shown in fig.20.

Photo 8 shows the current balance improvement when the heatsink temperature increases (25°C - 100°C) and the devices are working in the chopper circuit.

The fig.21 shows the output characteristics of the paralleled devices and the estimated on-state current.

VI. IGBTS IN THE ISOTOP PACKAGE.

To reduce parameter spread, the IGBTs dice are mounted in the ISOTOP package with the "die sister" technique; the thermal resistance between the device junctions is reduced to a minimum and the gates are connected in parallel.

When the ISOTOP packages are paralleled, they give the following advantages:

- The small and compact size of the package (fig.22) and the low R_{thjc} value (0.5°C/W) give a minimal thermal resistance between the paralleled devices.
- This package was designed in order to minimize emitter ground wiring effects; In fact Isotop packages provide an auxiliary emitter pin which makes it simple to separate the driving circuit from the power circuit (fig.22,23).

Photo 9 & 10 show that unbalanced wiring connections have very little effect on the

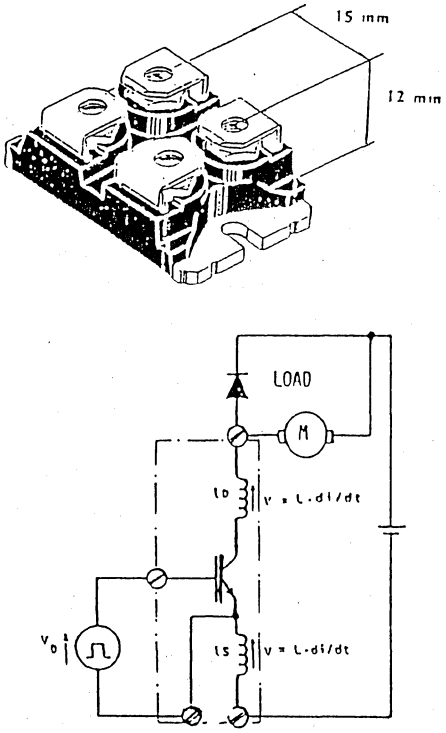


Fig. 22. Dimensions of the ISOTOP package and schematic diagram showing an auxiliary emitter pin.

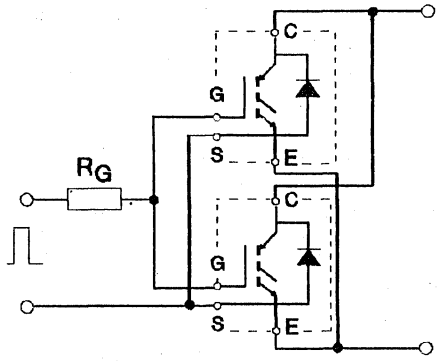


Fig. 23. Paralleling ISOTOP.

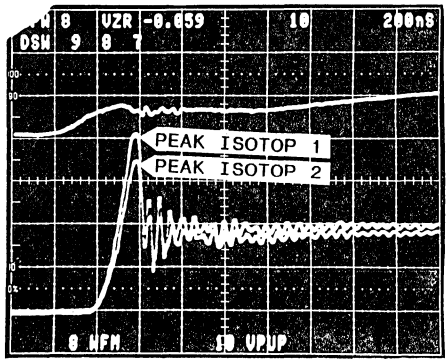


Photo 9. Turn-on of two TSG50N50DV with unbalanced emitter ground wiring. I_C=25A/div. V_{GE}=10V/div. t=200ns/div.

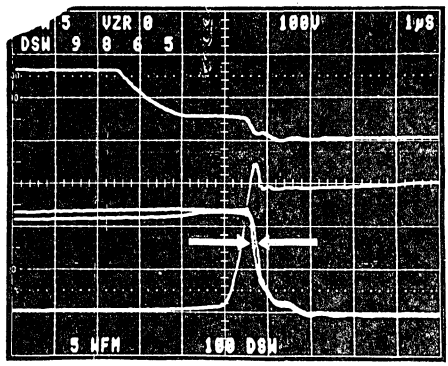


Photo 10. Turn-off of two paralleled TSG50N50DV. I_C = 25A/div. V_{CE} = 100V/div. V_{GE} = 10div. t = 1µs/div.

switching behaviour: the difference in length of emitter ground connections is 15 cm.
It can be seen in photo 10 that there is no peak voltage due to di/dt (V = L di/dt) on the gate-emitter auxiliary pin during current rise.

VII. CONCLUSIONS.

The performances in terms of current balance, thermal stability and switching behaviour when SGS-THOMSON IGBT devices are paralleled, are very satisfactory.
The transfer characteristics has no real influence on current balance in the on-state.
The on state current and the switching current balance are ensured respectively by the low spread of the V_{CEsat} values and by the low spread of device parameters.
High thermal stability is obtained by mounting the paralleled devices on the same heatsink even when the devices are insulated (mica, insulated package).
For an optimum switching behaviour of paralleled devices, it is necessary:

- to drive the gates with only one gate resistance.
- to balance the emitter-ground wiring.

When IGBTs are in the ISOTOP package, the wiring unbalance tolerance is high and the thermal resistance (R_{thjh}) is low; thus,the advantages of the ISOTOP package are:

- easy to design the lay-out when paralleling IGBTs in ISOTOP.
- small thermal resistance between the junctions of paralleled devices; thus, temperature difference between the junction of the devices in parallel is reduced to a minimal value.

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SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

HOW SHORT CIRCUIT CAPABILITIES GOVERN THE DESIRED CHARACTERISTICS OF IGBTs

by C.G. Aniceto, R. Letor

ABSTRACT.

Short circuit tolerance of IGBTs can be obtained by the optimization of both the protection circuit and the intrinsic ruggedness of devices.

This note discusses application design criteria and IGBT characteristics compared to the intrinsic short circuit ruggedness.

1.0 INTRODUCTION.

The continuous growth of IGBT applications requires more differentiation of device electrical characteristics. In fact, the structure of IGBTs makes them flexible to use and their switching performance can be specifically matched to many different applications.

For the best match between application requirements and IGBT characteristics, some compromise between the saturation voltage, switching speed and ruggedness is necessary.

To define the suitable IGBT short circuit ruggedness specification, this note analyzes the parameters influencing their behaviour during short circuit operation, and verifies the performance of the more usual short circuit protection compared to IGBT short

circuit ruggedness.
It is also shown that modification of the IGBT structure improves the short circuit performance without compromising the saturation voltage and switching speed.

2.0 SHORT CIRCUIT OPERATION OF IGBTs.

Static and dynamic characteristics are not sufficient to predict the short circuit behaviour of IGBTs. Also, dynamic phenomena correlated to stray parameters and to the short circuits circumstances must be carefully considered.

2.1 SHORT CIRCUIT MODES AND WAVEFORMS.

Real short circuit mode can be simulated using the test circuits "A" and "B" illustrated respectively in figure 1 and figure 5.

TEST CIRCUIT "A": The device is turned on when the collector is directly connected to the supply voltage and the short circuit inductance can be changed.This circuit simulates either a short circuit in one leg of a bridge circuit, or a permanent short circuit of the load [4].

The waveforms of figure 2 show the behaviour in the test circuit "A" when all the stray parameters are reduced to a minimal value. The effect of a significant short circuit inductance is shown in figure 4. The inductance, the reverse capacitance "C_{RS}", the gate capacitance "C_G", R_G, together with the IGBT amplification, constitute a resonant R,L,C circuit as shown in figure 3. Hence di/dt at turn-on generates a very high peak current due to a gate voltage overshoot.

TEST CIRCUIT "B": The short circuit is actived during the on-state. In this case a dV/dt is applied to the collector when the gate voltage is high and the device is in full conduction. This condition simulates accidental short circuit of the load during normal operation [4].

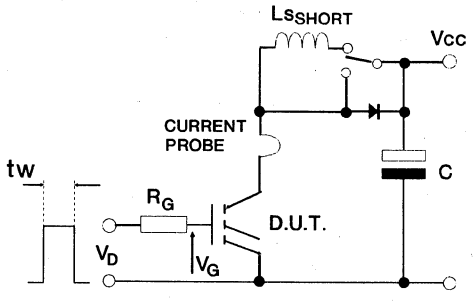

Fig. 1. Testcircuit"A" $L_{SHORT} \approx 4\mu H$, $L_{STRAY} \approx 150nH$.

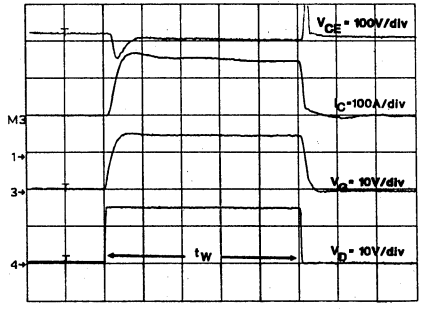

Fig. 2. Short circuit test with short circuit inductance = L_{STRAY}. Time scale: 2µs/div.

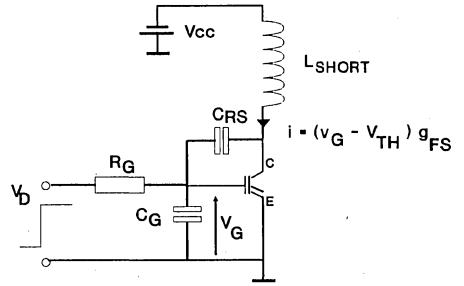

Fig. 3. Simplified equivalent circuit of the short circuit condition.

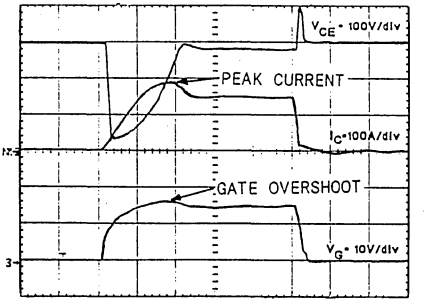

Fig. 4. Short circuit test with short circuit inductance = L_{SHORT}. Time scale = 2µs/div.

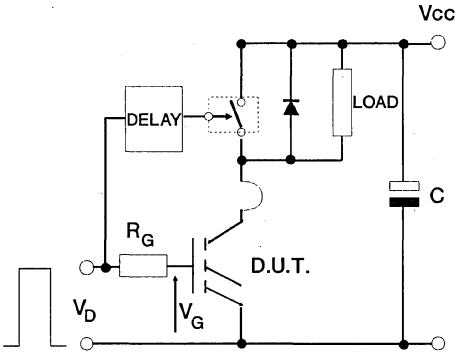

Fig. 5. Test circuit "B". Short during saturation.

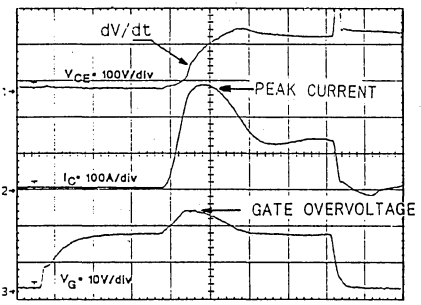

Fig. 6. Effect of the dV/dt when the short circuit occurs during IGBT full conduction. t = 2µs/div.

The waveforms of figure 6 show the effect of the dV/dt in the test circuit "B". The dV/dt acting trough reverse capacitance causes the gate voltage to rise over the driving voltage [6]. A peak current much higher than short circuit current is generated.

2.2 SHORT CIRCUIT STRESSES.

The failure of IGBTs during short circuit condition occurs either with static latch or with dynamic latch of the parasitic SCR of the structure (figure 14) [2]:

- Static latch is due to the high current density.
- Dynamic latching is due to the high dV/dt at turn-off.

The influence of the temperature is critical because the latching current decreases when temperature increases. Moreover, during short circuit there is a very fast temperature rise due to the very high energy increase dissipated in the device.

For this, gate voltage overshoot must be avoided and the short circuit current must be reduced as much possible. In fact:

During overshoot, the collector current ($i_C = g_{FS}\ (v_g - V_{TH})$) can reach the static latching current, especially if the transconductance of the device is high.
At turn-off the junction temperature is higher than at turn-on, so the dV/dt due to the stray inductance "Ls_C" can cause a dynamic latch-up.
Moreover, the stray inductance "Ls_C" creates an overvoltage at turn-off (see figures 2,4,6) due to the di/dt. If the di/dt at turn-off is not controlled by a suitable gate resistance the overvoltage can reach breakdown causing device failure.

2.3 PARAMETERS INFLUENCING SHORT CIRCUIT BEHAVIOUR (figure 7).

The main parameters influencing static and dynamic short circuit behaviour are:

- Transconductance g_{FS}, C_G, C_{RS} (Device parameters)
- Driving voltage V_D, R_G (Driving circuit)
- Ls_C, Ls_E (Stray inductance of lay-out and of capacitance)
- Ls_{SHORT}, dV_{CE}/dt, V_{CE} (Short circuit conditions)

The stray inductances Ls_E (emitter-ground) and Ls_G (gate-drive) mainly influence di/dt at turn-on, but they are not critical for usual circuit lay-out and must be carefully considered, only when devices are paralleled [8].
Transconductance g_{FS} is the most critical parameter. In fact, a high value of g_{FS} can generate very high continuous short circuit current and very high peak current during transient.

2.4 SHORT CIRCUIT CAPABILITY CHARACTERIZATION.

In order to make test conditions as reproducible as possible, the short circuit capability characterization was implemented using test circuit "A" with stray inductances reduced to minimum value.

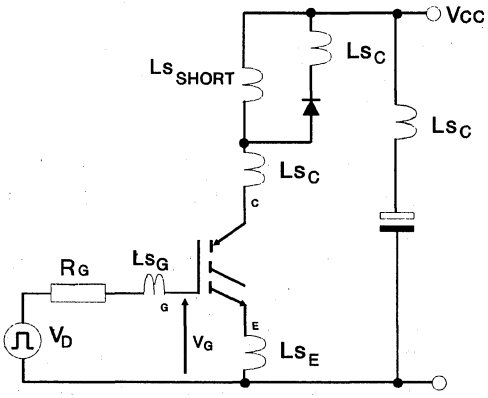

Fig. 7. Circuit parameters influencing short circuit current of the IGBTs.

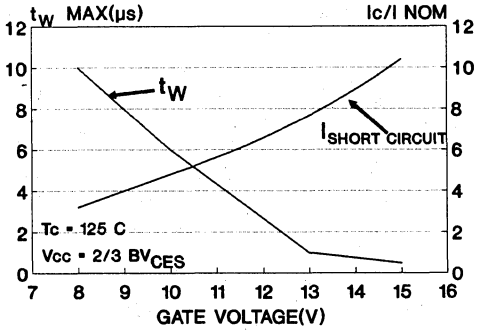

Fig. 8. Short circuit performance versus gate bias of IGBTs having a high transconductance. Maximum current overshoot ≤ 20% $I_{SHORT\ CIRCUIT}$.

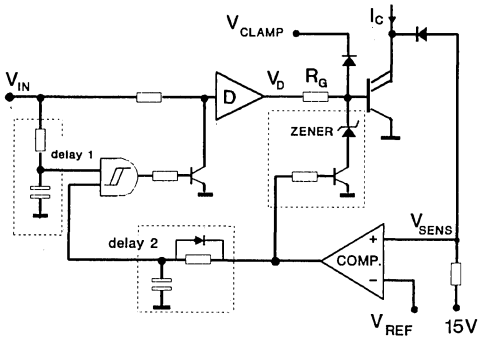

Fig. 9. Short circuit protection with high false alarm immunity.

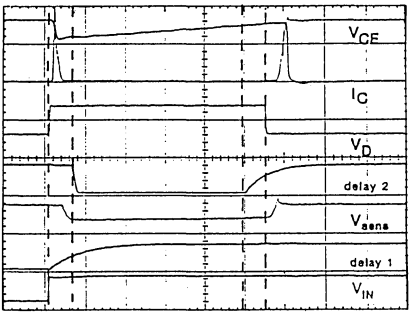

Fig. 10. Timing diagram of the protection circuit at turn-on and during overcurrent condition.

Short circuit capability is expressed in terms of:

- MAX SHORT CIRCUIT TIME (t_W as defined in figure 2)
- SHORT CIRCUIT CURRENT & PEAK CURRENT (I_{SHORT}, I_{PEAK})
  Versus: - V_G, R_G, T_C, V_{cc}.

Figure 8 shows a characterization example of a IGBT having a high value of the transconductance. For $V_G \geq 13V$ the device fails at turn-on due to static latch-up.

3.0 SHORT CIRCUIT PROTECTION.

To ensure short circuit tolerance of a power control system and of its output power switches, the following problems must be carefully considered:

1 - Limitation of the short circuit current.

2 - Limitation of short circuit protection delay.

3 - Nuisance tripping creating false alarm.

3.1 DESCRIPTION OF THE PROTECTION CIRCUIT.

The figure 9 shows the schematic diagram of a protection circuit using the IGBT saturation voltage for sensing. Sensing resistors or current transformers can also be employed without significant changes.

The zener diode limits the gate voltage during a short circuit condition so limiting short circuit current.

Delay 1 and delay 2 realized with a R, C filter and Schmitt trigger avoid activation of the protection circuit in case of false short circuit conditions. Delay 1 must filter transitory phenomena at IGBT turn-on, delay 2 gives noise immunity to the circuit.

The diode "**D2**" clamps gate voltage overshoots due to dV/dt.When a short circuit is detected the IGBT is turned off by its gate resistor in order to limit dV/dt and collector overvoltages.

The timing diagram in figure 10 shows the working mode of the circuit at turn-on and with an overcurrent condition during operation:

- At turn-on, the input 1 of the "AND" becomes high (IN_{HIGH} = 8V) after delay 1; If IGBT saturation was not detected (IN_{LOW} = 2V) during delay 1 the driving circuit input taken low.

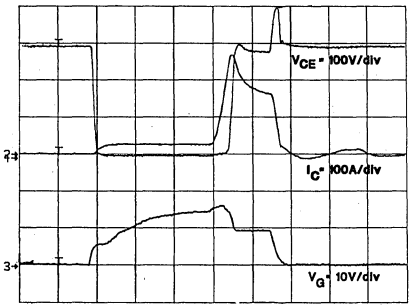

Fig. 11. Short circuit protection waveforms in the test condition "B". IGBT is TSG50N50DV. Time scale: 2µs/div.

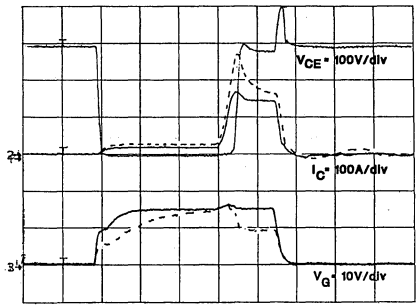

Fig. 12. Short circuit waveforms without voltage reduction of a IGBT having low transconductance compared to waveforms of figure 11 in dotted lines. t = 2µs/div.

- When, during normal operation, there is a overcurrent condition, the IGBT saturation voltage reaches reference voltage "V_{REF}" and the comparator activate the zener and the delay 2. If the overcurrent condition continues after delay 2, then the driver input is pulled down and the IGBT is turned-off.

This circuit works as a monostable multivibrator with positive edge triggering, but the IGBT is "ON" only if V_{IN} is high, so the noise immunity is assured. If a overcurrent or a short circuit condition were detected, it is necessary to take V_{IN} to the low.

3.2 PERFORMANCE OF THE PROTECTION CIRCUIT.

When the short circuit exists at turn-on (test circuit "A"), test conditions of the characterization are respected.

The performances of the circuit can be critical when the short circuit occurs during normal working conditions and the device is in full saturation. Figure 11 shows that a significant current overshoot stresses the IGBT (STGP50N50) under this short circuit condition even if the protection works correctly.

In fact the protection circuit needs a delay to pull the gate voltage to a safe value. This delay depends on the saturation voltage detection time and on the discharge time of the IGBT input capacitance. The discharge time can be significant due to the Miller effect during collector voltage rise. Moreover a high value of g_{FS} can induce a very sharp rise of the current during delay.

To avoid this phenomenon, IGBTs with a lower value of saturation current and transconductance should be employed. In fact, if the short circuit current is limited by the device itself, then it is not necessary to reduce the gate voltage during short circuit time. Figure 12 shows collector current and gate voltage waveforms of an IGBT having low saturation current (I_{Csat} = 3 * I_{NOM} @ V_G = 15V) subjected to the same short circuit condition shown in figure 11 and without any gate voltage reduction, compared to the STGP50N50 with high transconductance and gate voltage reduction during short circuit (same waveforms of figure 11 in dotted lines).

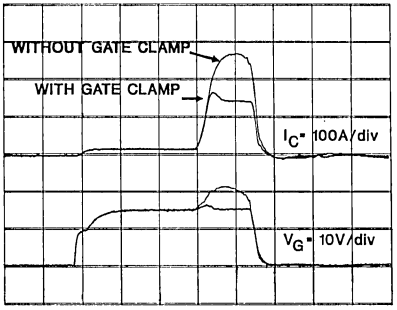

Fig. 13. Gate voltage and collector current with and without gate voltage clamping. t = 2µs/div.

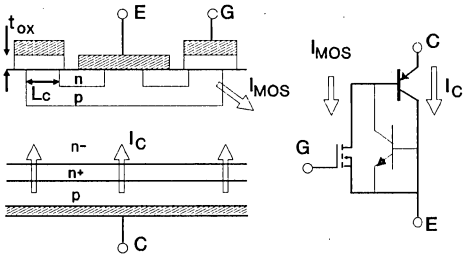

Fig. 14. Cross section of IGBT structure and simplified equivalent circuit.

If the gate voltage reduction is eliminated a fast clamping circuit is necessary. Figure 13 shows a comparison of the gate voltage and collector current waveforms with and without gate clamping voltage. This diode also limits gate voltage overshoots in the short circuit condition.

3.3 SHORT CIRCUIT SPECIFICATION OF IGBTs.

The criteria for providing short circuit protection to match the reliability of the more usual protection circuits are:

- $t_W > 5\mu s$ (delay to avoid false allarm)
- $I_{Csat} < 3 \cdot I_{NOM}$ (to ensure safe turn-off)
- $T_c = 125°C$ (working temperature)

5µs is the time necessary to ensure full saturation of IGBTs.

To give sufficient margin for safe operation $t_W \approx 10\mu s$.

4.0 DESIGN OF AN IGBT UNDER SHORT CIRCUIT CONDITIONS

The intrinsic short circuit ruggedness of IGBTs was improved by a optimization of the device structure aimed at obtaining a suitable value of the saturation current ("I_{Csat}" @ V_G=15V, Tj=150°C).

Parameters influencing transconductance and I_{Csat} ($I_{Csat} = g_{FS} \cdot (V_G - V_{TH})$ saturation current also affect saturation voltage "V_{CEsat}" [2] as shown by (1) and (2).

$$I_{Csat} = \frac{1}{(1-\alpha_{PNP})} \frac{\mu_{ns} C_{ox}}{2} \frac{Z}{L_C} (V_G - V_{TH}) \qquad (1)$$

$$V_{CE} = \frac{KT}{q} \ln \left[\frac{(1-\alpha_{PNP}) dI_C}{2qW_R Z D_a n_i F(d/L_a)} \right] + \frac{(1-\alpha_{PNP}) L_C I_C}{\mu_{ns} C_{ox} Z (V_G - V_{TH})} \qquad (2)$$

Where "L_C" is the channel lengh, "Z" is the channel perimeter, "C_{ox}" is the oxide capacitance ($C_{ox} = \varepsilon S/t_{ox}$).

I_{Csat} can be limited both by reducing the gain of the PNP transistor (α_{PNP}) and by acting on the MOSFET characteristics (L_c, Z, C_{ox}).

"α_{PNP}" influence both the PN junction threshold (first term of equation (2)) and the second term. For this reason only the MOSFET characteristics were optimized, so gaining advantages both in dynamic performances (C_G reduction) and in thermal stability [8].

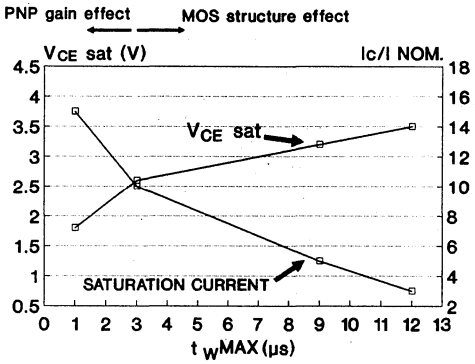

Fig. 15. Trade-off between saturation voltage and the short circuit ruggedness expressed as MAX t_w and saturation current @ V_G = 15V.

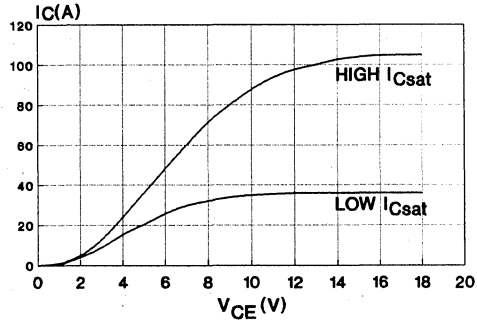

Fig. 16. Comparison of two IGBT output characteristics, with low I_{Csat} (ICsat ≈ INOM) and HIGH I_{Csat} (10 * I_{NOM}) @ V_G = 15V.

To reduce the saturation current by 70%, channel lengh (L_c) and oxide thickness "t_{ox}" were increased by 40%. This gives the best compromise between short circuit performances and saturation voltage as figure 15 and 16 show.

The lefthand side of figure 15 shows the effect of the PNP gain reduction due to life time reduction processes.

5.0 CONCLUSION.

The analysis of parameters influencing short circuit operation of IGBTs has led to the design of a suitable protection circuit, even for devices having modest short circuit performance.

This solution allows the use of IGBTs with very low saturation voltage.

However, an additional very fast circuit that reduces gate voltage during short circuit is necessary. During the delay of this circuit the dV/dt due to the IGBT desaturation can cuase a dangerous peak current. IGBTs having low transconductance can solve this problem.

Deacreasing transconductance of a IGBT causes saturation voltage to increase. The optimization of the IGBT structure allowed the realization of an IGBT with sufficient short circuit capability (t_W MAX = 10 µs), and with a value of V_{CEsat} that is 20% higher than the V_{CE}sat of a IGBT having t_W MAX = 1µs. This IGBT requires a simplified short circuit protection network and it does not compromise the efficiency or the short circuit ruggedness of the system.

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SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SWITCHING WITH IGBTS: HOW TO OBTAIN A BETTER PERFORMANCE

by A. Galluzzo, R. Letor, M. Melito

ABSTRACT

IGBTs are now being used in a variety of switching applications due to their attractive characteristics, particularly their current density, ruggedness and gate driving circuit. To exploit the best aspects of IGBTs it is necessary to understand how their switching performance can be controlled by the designer and how much the voltage and current waveforms can be shaped to obtain an acceptable compromise in terms of switching speed, ruggedness, power dissipation and EMI.

This paper, starting with voltage and current waveform analysis, highlights both the device and driving circuit characteristics which govern the switching. It suggests, by using a simple driving circuit, how to control both voltage and current slopes, independently.

The influence of negative gate bias and driving impedance versus dV/dt ruggedness are analyzed.

Finally the IGBTs switching behaviour, when connected in parallel, is examined.

1 - ANALYSIS OF PARAMETERS WHICH INFLUENCE SWITCHING WAVEFORMS

The switching behaviour of IGBTs is affected by the unavoidable parasitic capacitance of the structure. Moreover the turn-off losses are strongly dependent on the characteristic of the tailing effect on the collector current during turn-off. Nevertheless switching losses can be predicted and then limited to an acceptable value, that is compatible with the need for safe and noiseless switching. The main parameters governing switching behaviour: gate bias, driving impedance, stray inductances, gate charge must also be taken into account.

Fig. 1 shows a schematic circuit where the parasitic inductances which influence switching behaviour are highlighted.

In the following discussion it has been assumed that the stray inductances are small enough so that dI/dt >> Vcc/(Ls+Lc+Ld).

1.1 TURN-ON

When the freewheeling diode is conducting during turn-on switching (fig. 2) , increased losses occur in the diode if the dI/dt in the IGBT collector is increased. However the losses in the IGBT decrease with increasing dI/dt in the IGBT collector (fig. 3).

Reducing dI/dt leads to higher losses in the power switch but it makes the reverse recovery behaviour of the freewheeling diode softer, thus reducing EMI problems. Fig. 4 shows dI/dt versus Rg with Ls as a parameter. Ls includes both stray inductances due to package and external inductances due to source grounding layout. These inductances strongly influence dI/dt at turn-on because they act as negative feedback to the gate thus reducing the effective voltage applied to the device. This effect is emphasized in fig. 5 where the collector and gate current are shown.

The gate voltage was set at 15 V to give a low Vcesat and also because this value is applied as a standard gate voltage when various device characteristics are defined in data sheets.

1.2 TURN-OFF

The IGBTs turn-off (fig. 6) can be divided into three consecutive phases:

a) the gate voltage begins to decrease until it reaches the value when the Miller effect occurs;during this phase the collector voltage increases slightly changing the output characteristics with Ic=constant.

b) this phase is the Miller effect and the gate voltage remains constant because of modulation of the collector-gate capacitance.
This is due to collector voltage rapidly increasing to its maximum value.

c) the collector current begins to fall quickly (it is related to the turn-off of the MOS part of the IGBT structure) then it continues with a "tail" which is due to recombination of minority carriers in the substrate.

This tail, which causes the major losses, is strongly related to technology and its effect can not be mitigated by driving circuit.

After the collector current, collector voltage and junction temperature has been determined, turn-off losses can be controlled only during phase b) varying dv/dt through Rg while losses occurring during phase c) are slightly influenced by the driving circuit.

Increasing dV/dt decreases losses but it is necessary to take care not to exceed the RBSOA boundaries which also depend on junction temperature, collector current and collector voltage.

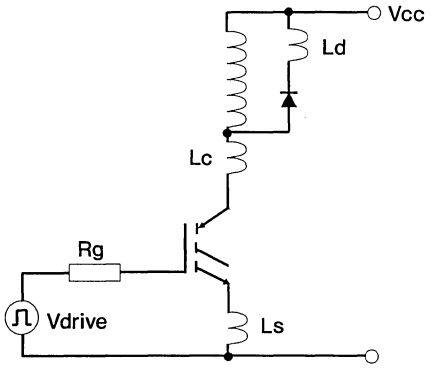

Fig. 1: Parasitic inductances influencing the switching behaviour

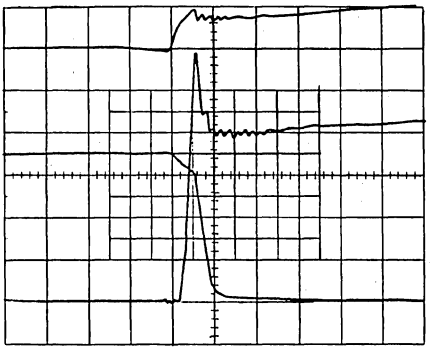

Fig. 2: Turn-on switching during freewheeling diode conduction

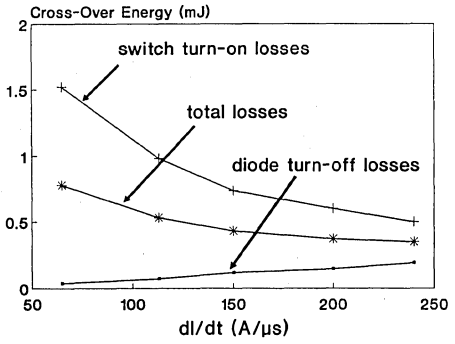

Fig. 3: Switching losses comparison

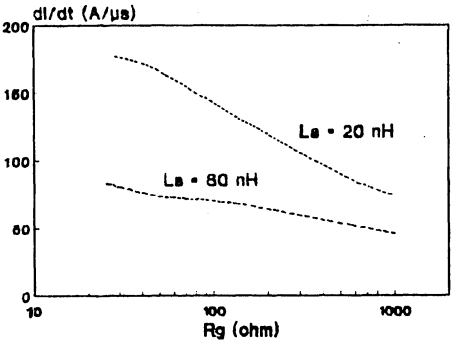

Fig. 4: Rg and Ls influence on dI/dt during turn-on

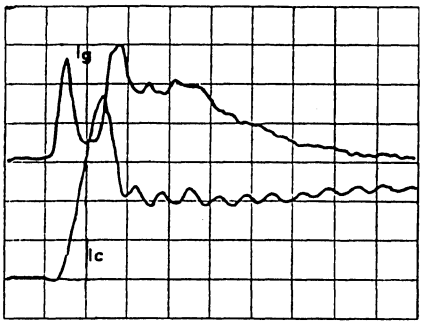

Fig. 5: Ic and Ig during turn-on

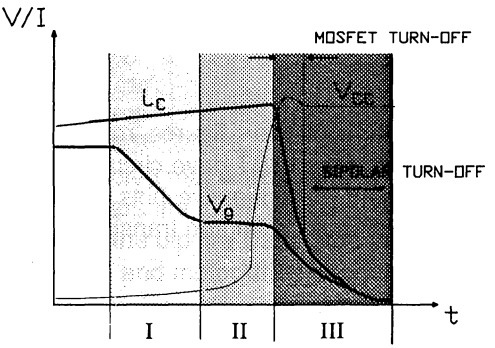

Fig. 6: IGBTs turn-off

2 - HOW TO MANAGE DI/DT AND DV/DT

Useful information about switching behaviour of IGBTs can be obtained from the gate charge curve. Even if the measuring conditions are quite different from the operating ones the total charge supplied to gate during switching is the same. The switching speed of a voltage driven device is strictly related to the rate of supplying charge to the gate input. This is true for IGBTs too, except during the falling edge of the collector current.

If we are able to control the rate of supplying this charge, i.e. if we can manage the amplitude of the gate current during switching we can independently vary both the voltage and the current slope.

2.2 TURN-ON

The driving circuit shown in fig. 7 allows dI/dt to be varied through R1 but at the same time this resistance fixes the collector voltage slope. Increasing R1 leads to a lower dI/dt and also to a lower dV/dt which increases turn-on losses.

It would be useful to have a di/dt low enough to reduce EMI problems and a dV/dt fast enough to keep power losses to a minimum. It is possible to achieve that using a driving circuit which operates according to the schematic shown in fig. 8.

The current slope is fixed by R1 and voltage slope by R2 by turning Q2 on after Q1 with a suitable delay. The waveforms in figures 9a and 9b show the difference between the standard circuit and the improved version.

2.3 TURN-OFF

The driving circuit can only control the slope of the collector voltage (fig. 10) and only slightly influences the fall of the collector current which is responsible of the major losses due to the tailed turn-off.

Figures 11, 12 and 13 show the effect of Vc, Ic and Tj on the amplitude of the tail of the collector current.

To minimize turn-off losses it is best to choose a device whose characteristics matches better the required operating conditions in terms of Vc, Ic and Tj.

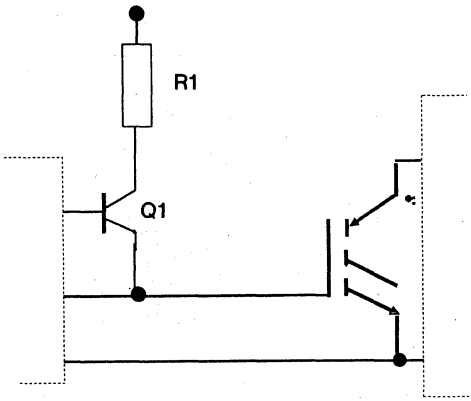

Fig. 7: Standard driving circuit

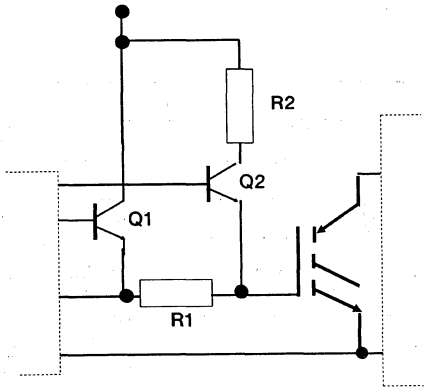

Fig. 8: Improved driving circuit

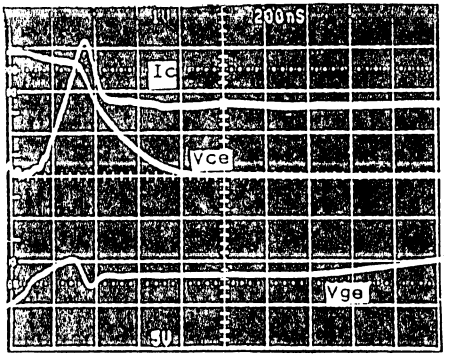

Fig. 9 a: Switching waveforms with standard driving circuit

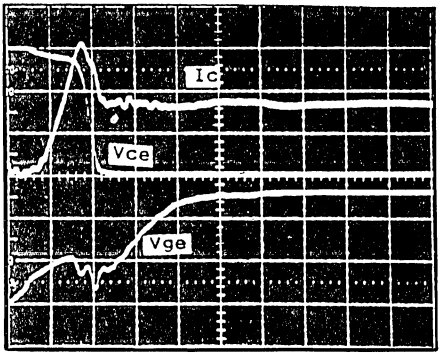

Fig. 9 b: Switching waveforms with improved driving circuit

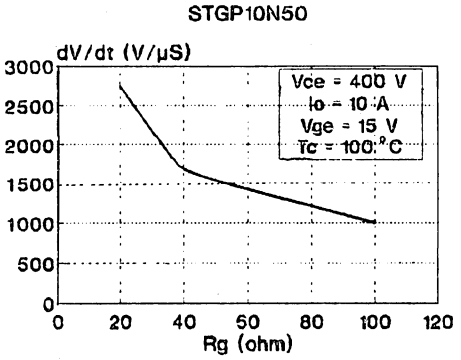

Fig. 10: Rg influence on dV/dt during turn-off

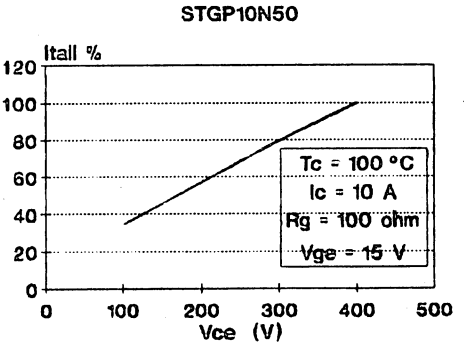

Fig. 11: I_{tail} versus collector voltage

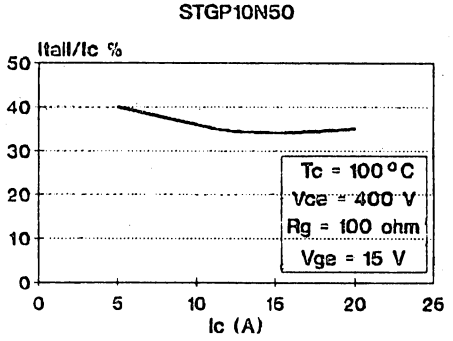

Fig. 12: I_{tail} versus collector current

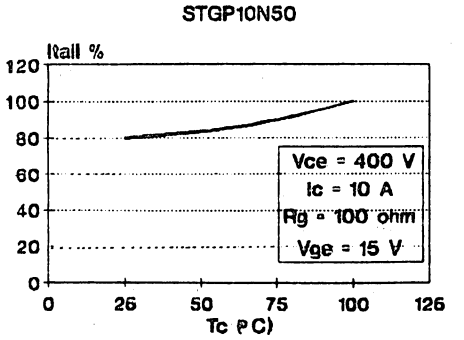

Fig. 13: I_{tail} versus Tj

3 - HOW TO AVOID DV/DT PROBLEMS

The spurious turn-on problem due to dV/dt is typical of the circuit shown in fig. 14.
The free-wheeling diodes in parallel with each IGBT are turned off during the opposite IGBT turn-on generating a dV/dt whose value depends on :

- opposite IGBT turn-on speed (dI/dt)
- free-wheeling diode "softness"
- wiring inductances
- gate bias and driving impedance

This applied dv/dt, acting through the collector-gate capacitance (fig.15) causes the gate voltage to rise turning the device on and leading to additional losses. This undesired effect is emphasized when temperature increases because of temperature dependence of Vth and gfs.
It is possible to avoid this effect either minimizing the dv/dt value or making the device less sensitive to dV/dt by a driving circuit specifically designed for this purpose or combining the two techniques above mentioned.
The first item requires using fast soft recovery diodes, reducing wiring length and turning the IGBTs on slowly. The second one requires the driving impedance to be fixed at such low value that the gate voltage can not exceed the threshold voltage during dV/dt. The value of this driving impedance depends on die-size of the device: fig. 16 shows the Rge needed to avoid spurious turn-on due to dv/dt.
Another way of avoiding spurious turn-on is to bias the gate negatively. Fig. 17 shows the different behaviour of gate voltage with and without negative bias.
The lower peak of the gate voltage is due to the different equivalent input capacitance when the gate is negatively biased.

4 - PARALLELED IGBTS SWITCHING BEHAVIOUR

The influence of the spread of parameters, of drive circuit and lay-out unbalance was investigated splitting the analysis as follows:

a) driving IGBTs with one gate resistance for each device (fig. 18);
b) driving IGBTs with a common gate resistance for all the devices (fig.19);
c) unbalancing emitter wire connection (fig. 20);
d) paralleling devices with the maximum spread of the parameters.

The performed analysis pointed out that voltage and collector current waveforms are stable even in the worst case conditions which occur when the gates are driven with a common resistance and the wiring inductances are strongly unbalanced.
In detail :
- IGBTs behaviour during turn-on is not very different in a) or b) conditions (fig. 21 and fig. 22).

If the paralleled devices have different storage times, driving the gates with one resistance for each device has the drawback shown in fig. 23: the collector current of the device having the smaller storage time begins to fall before the other one do.
Consequently, because of the inductive load, the 2nd IGBT has to switch-off a collector current greater than the other device thus increasing storage current unbalance. Driving the gates with only one gate resistance minimizes this effect (fig. 24): the device with the higher storage time holds the gate voltage to "V_{th} + I_c/gfs" until the fall time phase, so equalizing the storage times.
- The effect of a poorly balanced emitter connection is highlighted during the rising and the falling edge of the collector current.

Fig. 25 shows the peak current unbalance, during turn-on, when the condition c) occurs. In the case shown $\Delta Ls = 0.15\mu H$.

Fig. 26 and fig. 27 show the corresponding effect during turn-off: wiring inductance imbalance affects only the power-MOSFET phase.

This behaviour creates negligible switching losses imbalance compared with the total turn-off ones.The current unbalance just before current fall affects the tail amplitude and it can create significant imbalance in the switching losses.

- IGBTs with the maximum spread in parameter values were paralleled; the comparison of current waveforms in fig. 21 and fig. 22 demonstrates that, during turn-on, the influence of parameter spread is low (Ls $\approx$ 30 nH).

The spread of IGBTs parameters (gfs, Vth, gate-charge) leads to different storage times and causes current imbalance thus creating switching losses imbalance.

Current imbalance due to the IGBTs parameter spread can be calculated with the equations (2) and (3).

The curve of fig. 28 shows the imbalance in switching losses between two devices where the Vth and gfs values are the limits of the parameter spread.

$$I_{load} = I_{1st} + I_{2st} = V_{GE}\,(g_{fs1} + g_{fs2}) - (g_{fs1}V_{th1} + g_{fs2}V_{th2}) \qquad (2)$$

$$I_{storage} = I_{1st} - I_{2st} = V_{GE}\,(g_{fs1} - g_{fs2}) - (g_{fs1}V_{th1} - g_{fs2}V_{th2}) \qquad (3)$$

CONCLUSION

A careful analysis of circuit and device parameters, influencing switching waveforms, was carried out taking into account negative gate bias, dV/dt influence and effects of device paralleling.

The following statements were explained:

- it is possible to manage separately both the current and the voltage slope except the collector current tail;

- negative gate bias reduces spurious turn on caused by dV/dt in bridge configurations;

- negative gate bias without Rg adjustment reduces the RBSOA because of increased dV/dt;

- common resistor on the gate of paralleled devices improves switching losses balance;

- stray inductance on emitter connection reduces switching speed and can causes losses unbalance in paralleled devices;

Performance improvements obtained by optimization of gate driving circuit involve cost increases. It is task of the system designer to define a good trade off between cost and performances.

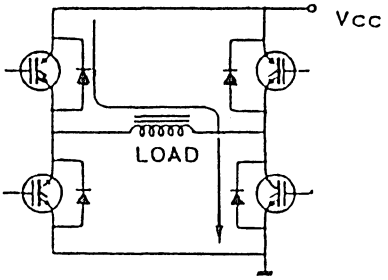

Fig. 14: Typical circuit where dV/dt conduction can occur

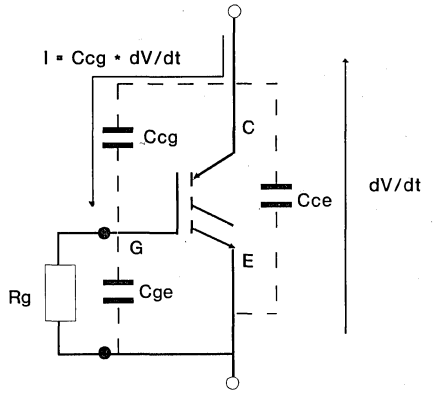

Fig. 15: Current flow through IGBT capacitance due to dV/dt

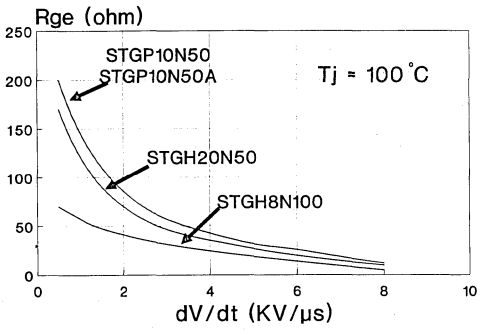

Fig. 16: Rge values that avoid dV/dt conduction versus dV/dt

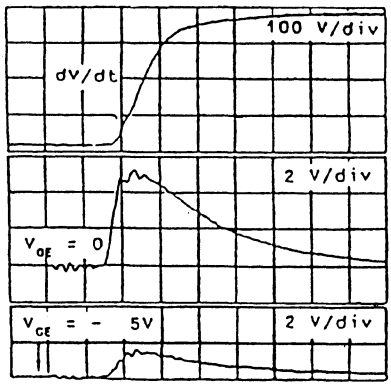

Fig. 17: Comparison of gate voltage behaviour with and without negative bias

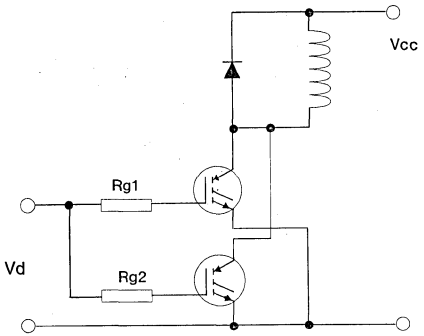

Fig. 18: Driving with separate gate resistance

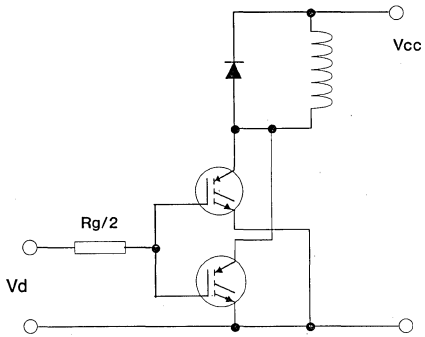

Fig. 19: Driving with one gate resistance

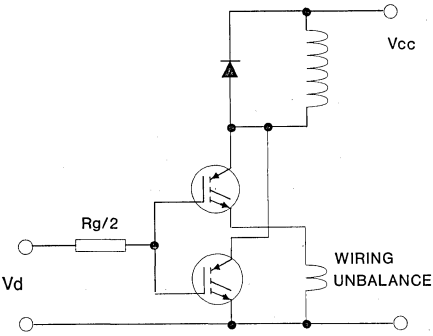

Fig. 20: Emitter grounding unbalance

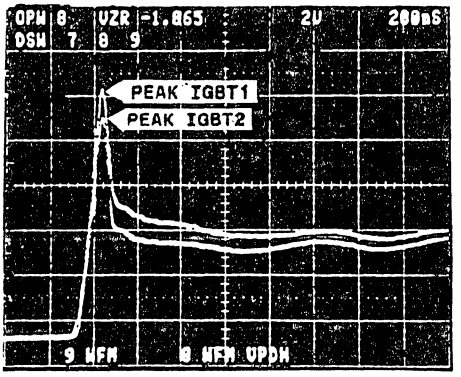

Fig. 21: Turn-on with separate gate drive (fig. 18) of an STGH8N100. I_c = 2A/div

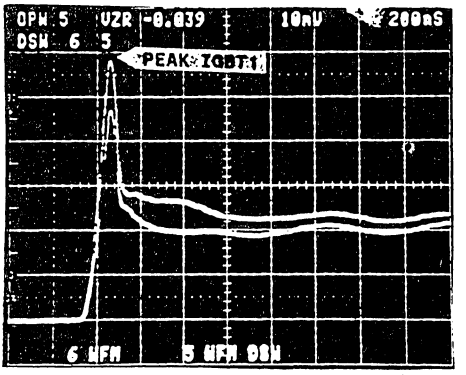

Fig. 22: Turn-on with one gate resistance (fig. 19) of an STGH8N100. I_c = 2A/div

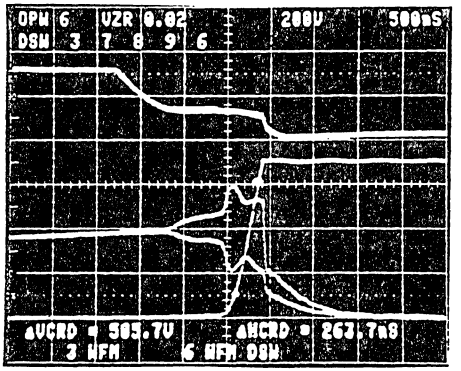

Fig. 23: Effect of separate gate drive on storage current waveforms. I_c = 2A/div, V_{ce} = 200/div, V_{ge} = 10/div

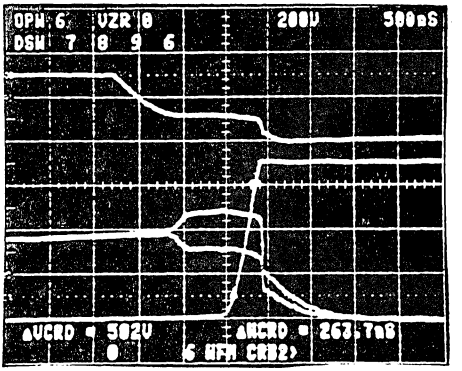

Fig. 24: Turn-off with one gate resistance. I_c = 2A/div, V_{ce} = 200/div, V_{ge} = 10/div

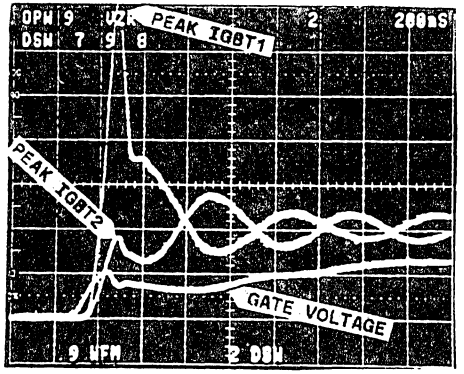

Fig. 25: Turn-on with unbalanced emitter-ground connection (fig. 20). I_c = 2A/div

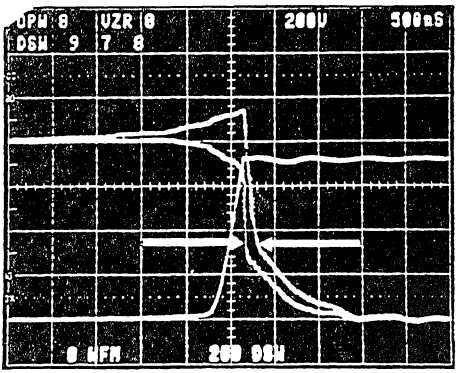

Fig. 26: Turn-off with unbalanced emitter-ground connection (fig. 20). I_c = 2A/div

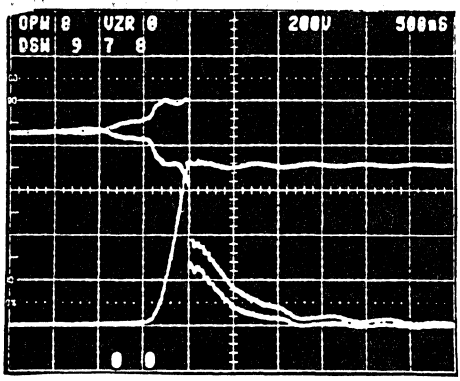

Fig. 27: Turn-off current waveforms with balanced gate-emetter wiring (fig. 19). I_c = 2A/div

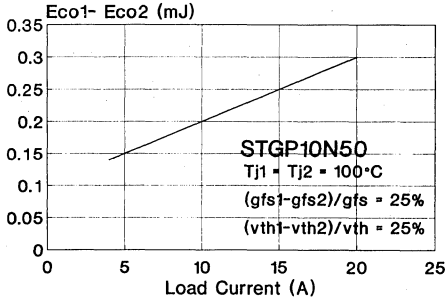

Fig. 28: Switching losses unbalance

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SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SERIES CONNECTION OF MOSFET, BIPOLAR AND IGBT DEVICES

by R. Letor

ABSTRACT.

Fast power switches with voltage ratings much higher than those of single fast switching devices can be made by connecting Bipolar Transistors, Power MOSFET and IGBTs in series.

Problems associated with device characteristics such as balanced switching, steady state and thermal behaviour must be carefully considered when designing with such switches.

This note deals with the series connection behaviour analyzing both static and dynamic characteristics of the devices.

Two philosopies for driving circuits are described and design criteria are given for obtaining optimum performance.

1.0 INTRODUCTI0N.

Advantages of BIPOLAR TRANSISTORS, Power MOSFETs and IGBTs reside in the simplicity of the driving circuit and on their high switching speed. But, applications of these devices are limited to maximum reverse voltage, generally up to 1000V - 1500V. Higher voltage ratings would make these devices unattractive due to problems related to their structure.

For example, theoretical $R_{DS(on)}$ of a Power MOSFET increases with the square of the voltage breakdown ($R_{DS(on)}$ = 5.93 E-9 * (VDSMAX)$^{2.5}$). Figure 1 showing the real behaviour of SGS-THOMSON Power MOSFETs versus breakdown voltage, demonstrates that the current rating of three 800V Power MOSFETs in series will be higher than a single 2000V Power MOSFET.

Moreover, the design of IGBTs and BIPOLAR transistors with higher voltage ratings can be difficult due to the rise time of the switching waveform shown in figure 2.

Therefore, in some applications like battery chargers, inverters for medium voltage lines such as railway traction using frequencies up to 20kHz or high resolution TV deflection with operating frequencies of up to 64kHz, the series connection of fast switching power devices can be an interesting solution.

When connecting switching devices in series, voltage sharing during the off-state, and during transient must be carefully considered.

In fact the spread of leakage current creates unequal reverse voltage sharing. Delay between commutation due to switching time differences causes transient overvoltage.

If the parameters are temperature dependent, junction temperature difference must also be considered.

2.0 STEADY STATE VOLTAGE SHARING.

2.1 HOW TO BALANCE STEADY STATE VOLTAGE SHARING.

Figure 4 illustrates how the difference in blocking voltage characteristics results in unequal state voltage and how a resistor connected in parallel to each device (figure 3) equalizes the voltage sharing.

Equations 1 and 2 can be derived from the graphical information in figure 4 and to evaluate the value of R that reduces the difference of blocking voltage to a fixed value ΔV_R with a fixed V_M.

$$\Delta V_{R12} = V_{R1} - V_{R2} = R_1 * \Delta I R_{12} \qquad (1)$$

$$V_M = V_{R1} + V_{R2} + \ldots + V_{Rn} \qquad (2)$$

Equation (1) assumes that the leakage current is constant, this approximation is errs on the side of caution and introduces a safety margin.

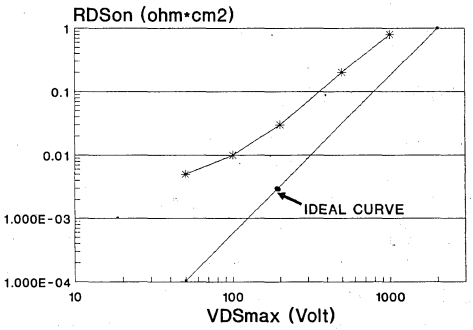


Fig. 1. Ideal and real behaviour of $R_{DS(on)}$ vs breakdown voltage.

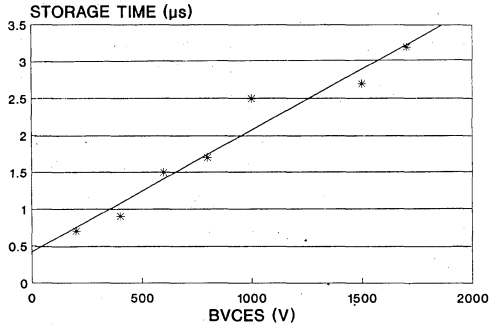


Fig. 2. Storage time behaviour versus rated BV_{CES} for bipolar transistors.

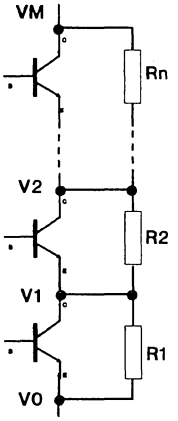


Fig. 3. Connection of sharing capacitors.

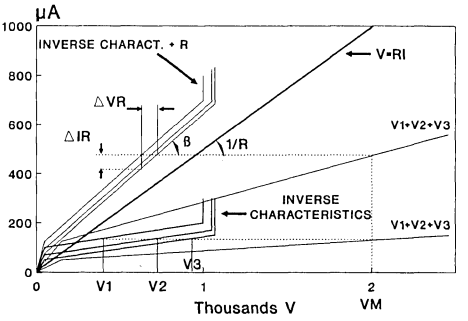


Fig. 4. Graphical calculation of sharing resistors when V_M and ΔV_R are fixed.

If we suppose that device 1 has the lower I_{RM}, V_{R1} will be the maximum reverse voltage ($V_{R1} = V_{RM}$) and developing the equation (2):

$$V_M = V_{RM} + V_{RM} - \Delta V_{R12} + \ldots$$
$$\ldots + V_{RM} - \Delta V_{R1n} = n \cdot V_{RM} - \sum_2^n \Delta V_{R1n} \quad (3)$$

The worst case condition, when n devices are connected in series, occurs when (n-1) devices have maximum leakage current and one device has the lowest possible leackage current: $\Delta IR_{1n} = \Delta IR_{max}$.
In this case, setting $R_1 = R_2 = \ldots = R_n$, the solution of the equations 1 and 2 gives:

$$R = (n \cdot V_{RRM} - V_M) / (n-1) \cdot \Delta IR_{max} \quad (4)$$

2.2 EVALUATION OF ΔIR_{max}.

ΔIR_{max} is the sum of $\Delta IR_D + \Delta IR_T$, where:

- ΔIR_D is the maximum leakage current dispersion at a fixed V_R and Tj.
- ΔIR_T is due to the difference between the junction temperatures of each device (ΔTj).

For devices today available $\Delta IR_D \approx 0.6IRM$ @ $V_R = V_{RRM}$ and Tj = 100°C.

The difference in junction temperature depends on both differences of power dissipation and on the thermal resistance between devices.

$$\Delta Tj = \Delta (R_{th} \cdot P_{DISSIPATION})$$

Experience shows that ΔTj = 10°C is the maximum value for insulated devices mounted on the same heatsink.
Using the derating shown in figure 5, for ΔTj = 10°C:

$$\Delta IR_T = 0.2\ IRM.$$

Taking a safety margin we can use:

$$\Delta IR = 0.85\ IRM.$$

2.3 EXAMPLE 1: series connection of three STHV82 Power MOSFETs:

Ratings:

V_{DSS} = 800V

I_{DSS} max = 1000µA @ Tj=125°C

$R_{DS(on)}$ max = 2Ω @ Tj=25°C

$R_{thj\text{-}case}$ = 1°C/W

Conditions:
Maximum blocking voltage: V_M = 2000V
Maximum Current and duty cycle:
I_M = 3A, t_{on}/T = 0.5
Case temperature:
T_{CASE} = 80°C
Switching frequency : 50KHz.

Calculation of sharing resistor values.

T_j can be estimated using:

$R_{DS(on)}$ @ T_j = 100°C ≈ $R_{DS(on)}$(25°C) * 1.7

$T_j \approx T_{case} + R_{thj\text{-}case}$ *
$R_{DS(on)}$ * ID^2 * $t_{on}/T \approx$ 100°C.

For T_j = 100°C using the derating of figure 5:

I_{RM} = (1 - 0.6)mA = 0.4mA

For safety operation and reliability

V_{RM} = 0.9 V_{DSS} = 720V.

Using equation (4):

R = (3 * 720 - 2000)/(2 * 0.4 E-3) = 200 kΩ.

Maximum power dissipation of each resistor when t_{on}=0: V^2/R = 2.6 W.

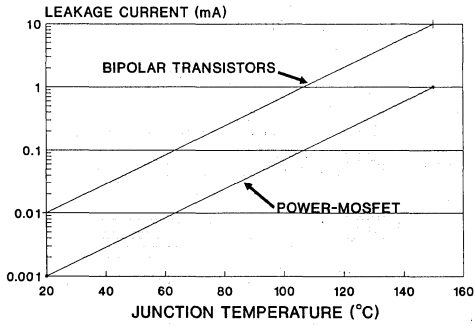


Fig. 5. Leakage current versus junction temperature.

2.4 IS IT POSSIBLE TO ELIMINATE THE SHARING RESISTORS?

For high frequency operation, it is necessary to consider the impedance of the output capacitance of the device which is in parallel with the sharing resistors.
In the previous example the impedance of the STHV82 output capacitance (150pF) is much lower than the calculated value of the sharing resistors:

$$Z_{Coss} = 1/2\pi fCoss \approx 21\ K\Omega << 200K\Omega$$

Therefore, if only high switching frequency conditions are expected, then the sharing resistors can be omitted.

3.0 DRIVING CIRCUIT FOR FAST SWITCHING DEVICES IN SERIES.

Two philosophies for driving switching power devices in series and for optimizing transient voltage sharing can be developed:

1) Driving each device in series with syncronized pulses and masking the difference of switching time.
2) Equalizing switching times with an optimized driving circuit.

Syncronized driving pulses can be generated by a transformer and delay turn-off time difference can be masked by snubber capacitors.
When continuous mode and wide range of duty cycle are required, it is difficult to design a method for driving the transformer. In this case auxiliary supplies and optocouplers can be used.
Equalization of switching times and continuous mode can be achieved using capacitive coupling between output circuit and driving circuit and diode network can be used for continuous bias.

3.1 DRIVING CIRCUIT GENERATING SYNCRONIZED PULSES AND TRANSFORMER COUPLING.

It is possible to achieve excellent synchronization of the driving pulses together with good control of the driving voltage and current.

Figure 6 shows a driving circuit for both voltage and current controlled devices.

The coupling inductances between the primary winding and every secondary must be as balanced as possible in order to equalize all the transfer impedances.

In both circuits the device driving current is limited on the primary side of the transformer; this feature reduces the difference in delay turn-off time of devices in series.

In fact during delay turn-off time or storage:

$$(I_{D1} + I_{D2}) = I_D \cdot n_2/n_1$$

Input impedances of devices ≈ 0

$$(-I_{B1} \approx -I_{B2} = I_D/2).$$

At the end of storage for bipolar transistors or at the end of Miller effect for voltage controlled devices (Power MOSFET, IGBT) the input impedance becomes very high and the driving current fall, when the faster device turns-off, the device with the higher turn-off delay time increases its switching speed because it is driven by all the available current $(-I_{B(G)} = I_D \cdot n_2/n_1)$.

3.2 EQUALIZATION OF TURN-OFF DELAY TIMES USING CAPACITANCES.

In the circuit of figure 7, the capacitors transmit driving voltage to the high side devices and the diodes supply continuous gate voltage during the on state. The circuit works as follows.

During transition: We suppose that initially all Power MOSFETs are in the off state and capacitor voltages are balanced. When the positive edge is applied to drive circuit, P_1 turns-on and pulls down the source of P_2. The capacitor network charges the gate of P_2. P_2 starts turn-on phase and pulls down source of P_3 etc...

The turn-off phase is similar to the turn-on phase. When P_1 turns-off, the source of P_2 is pulled up. A negative voltage discharges the gate of P_2 into the capacitor network turning

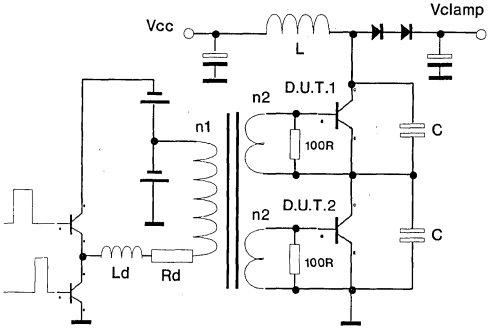


Fig. 6. Syncronized Drive of fast switching power devices in series using a transformer.

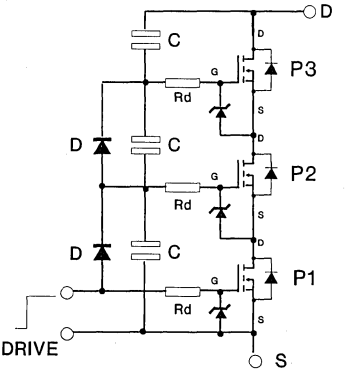


Fig. 7. Capacitors and diode network driving Power MOSFETs connected in series.

P_2 off, etc.
For a better voltage balance during switching, the capacitor must be charged to the same voltage (V_{C1}=V_{C2}=...=V_{C3}); imbalance is due to Power MOSFET gate charge and discharge of the capacitors network. For this

$$\Delta V_{max} = (n-1) \cdot Q_{GATE\ CHARGE} / n \cdot C$$

During on state:

$$V_{GATE}(n) = V_{DRIVE} - (n-1) \cdot (V_{DS(on)}+V_{F\ diode})$$

Therefore, for full saturation of every device connected in series a driving voltage greater than 15V is necessary.

Possible configurations. This circuit configuration can be used for series connection of IGBTs and BIPOLAR TRANSISTORS.
When connecting IGBTs, sharing capacitors are necessary because the turn-off current tail of IGBTs does not depend on the driving circuit.

ADVANTAGES: Using POWER MOSFETs this circuit allows optimum dynamic voltage balance with low values of capacitors so minimizing energy dissipation.

DISADVANTAGES: The circuit is critical when driving bipolar transistors due to high drive energy.
It is difficult to optimize switching waveforms. You can see in Photo 1 that current fall waveforms are not correct.
The driving voltage necessary for full saturation can be greater than the rated gate voltage.
For better on-state and switching performances, a regulator for each POWER MOSFET gate must be introduced (Figure 8) and optimization of the driving circuit will be necessary.

EXAMPLE 2.

Photo 2 shows POWER MOSFET drain voltage balance and drain current behaviour in the circuit of figure 7, where STHV102 devices are connected in series and in parallel.

C = 1500pF.

$Q_{GATE\ CHARGE}$ of 2 · STHV102 @ (V_G = 15V) = 2 · 85nc = 170nc

ΔV = 170 E-9 / 2 · 1500 E-12 = 56.5V

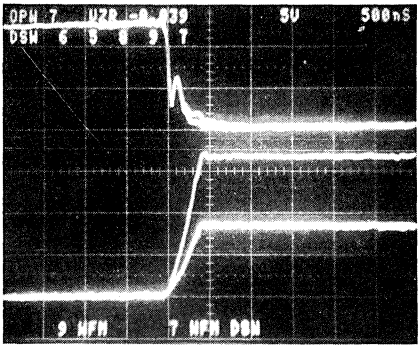


Photo 1. Voltage sharing and drain current of two Power MOSFETs in series as described in the example 1.
I = 2A/div, V = 500V/div.

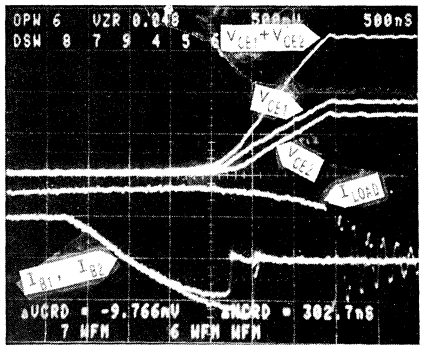


Photo 2. Load current and voltage sharing behaviour of two BUV46 in series as shown in figure 5. C_S = 4.7nF,
I_B = 0.5A/div, I_{LOAD} = 2A/div, V = 500V/div.

4.0 TRANSIENT VOLTAGE SHARING WITH SYNCRONIZED DRIVING CIRCUIT.

The transition overvoltages due to the difference between turn-off times can be controlled using sharing capacitors as shown in figure 9.

During switching operation, discharge of the sharing capacitors generates power losses so reducing efficiency of the converter.

In this note we define the losses of efficiency due to the capacitors discharge as follows:

Balancing losses/handled power = $n \cdot 0.5 \cdot C \cdot V^2 \cdot f/(V_M \cdot I_C \cdot \text{duty cycle})$.

4.1 HOW TO CALCULATE SHARING CAPACITORS.

Worst case condition occurs at turn-off with a inductive load. When the faster device in series turns-off, all the current load charges the capacitance in parallel to the slower device output', and generates a fast voltage rise.

Using suitable capacitances it is possible to retard the voltage rise and to fix ΔV_R as shown in figure 9.

$$C = \Delta Q/\Delta V_R = \int_{t_2}^{t_1}(I_1(t) - I_2(t))\,dt / \Delta V_R \quad (5)$$

For n devices connected in series and setting $C_1 = C_2 = ... = C_n$, Δt and ΔI are fixed to the maximum value.

4.2 SERIES OF BIPOLAR TRANSISTORS.

At turn-off the difference in storage time must be considered. In fact, denaturation at the end of the storage will cause collector voltage rise. For bipolar transistors the spread of this parameter, about 50%, is much higher than the fall time. For this $\Delta Q \approx I_{OFF} \cdot \Delta t_{storage}$ and the equation (5) becomes:

$$C_{MIN} = I_{OFF} \cdot \Delta t_{storage} / \Delta V_{R\,max}. \quad (6)$$

EXAMPLE 3:

Series connection of two BUV46AFI.

Ratings:

$V_{CES} = 1000V$

$1.5\mu s < t_{storage} < 2.5\ \mu s$ @ $I_c = 2.5A$;

$I_{B1} = -I_{B2} = 0.5A$, $T_c = 25°C$.

$I_{C\,nom.} = 5A$

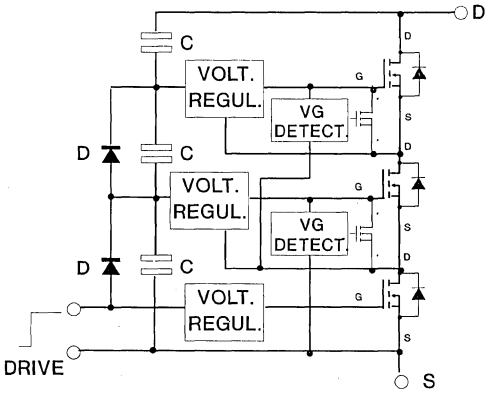


Fig. 8. Driving circuit of figure 7 for optimized driving voltage and switch-off.

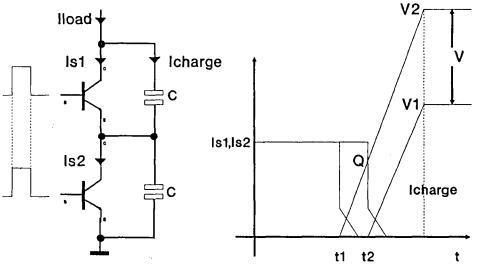


Fig. 9. Evaluation of sharing capacitors reducing the effect of delay turn-off time spread.

Conditions:

Maximum turn-off clamping voltage:

V_M = 1600V.

I_{OFF} max. = 3A.

Switching frequency:

15 KHz, duty cycle = 0.5

$I_{B1} = -I_{B2}$ = 0.5A

Solution:

For safety margin:

$V_{CEmax} = 0.9 \cdot V_{CES}$ = 900V

$\Delta V_{R\ max} = 2 \cdot V_{CEmax} - V_M$ = 200V

Using equation (6):

$C2_{MIN}$ = (3 • 1E-6)/200 = 15nF.

The power dissipation due to discharge of sharing capacitors is:
Balancing losses = $P_D = C \cdot V^2 \cdot F$ = 144 W.

(Balancing losses/handled power %) =

$P_D / I \cdot V_{max} \cdot 0.5 \cdot \%$ = 6 %

For better efficiency this energy must be reduced. For this, it is necessary to limit the maximum spread by a selection of devices. If $\Delta t_{storage}$ = 300ns, then a 4.7 nF sharing capacitor can be used as shown in photo 2.

4.3 SERIES OF POWER MOSFETs.

The current fall in POWER MOSFETs is very fast; equation (5) becomes:

$$\Delta V_R = I_{OFF} \cdot \Delta t_{OFF} / C$$

t_{OFFmax} can be calculated using gate charge, as shown in figure 7:

$$- t_{OFF} = (Q_1 + Q_2)/I_{GATE}$$

If I_{GATE} is balanced for all devices in series , then Δt_{OFF} max can be calculated using the distribution of figure 11; moreover, due to temperature independance of gate charge, temperature difference between junction devices can be disregarded:

$$- \Delta t_{OFF} = 5/100 \cdot \text{(typical value of } t_{OFF})$$

If each POWER MOSFET has its own driving resistor, then tollerance of resistors must be considered and delay turn-off time can be calculated as follows:

$$- t_{OFF} = t_a + t_b = R_G C_{GS} \ln 3 + Q_2 R_G / (V_{Drive} - G_m I_D)$$

EXAMPLE 4: Series of two STHV102.

Ratings:

V_{DS} = 1000V

Gate charge: $Q_1 + Q_2$ = 62 nc ± 5%

Conditions:

I_G = 100 mA.

Maximum clamping voltage:

V_M = 1600V

I_{OFF} = 3A

F = 15 KHz, duty cycle = 0.5

Solution:

For safety margin:

$V_{DSmax} = 0.9 \cdot V_{DS}$ = 900V

$\Delta V_{R\ max} = 2 \cdot V_{DSmax} - V_{max}$ = 200V

$\Delta t_{OFF} = \Delta (Q_1 + Q_2)/I_G$ =

6.2 E - 9/ 100 E - 3 = 62ns.

C_{MIN} = (3 • 62 E-9) / 200 = 930pF.(1000pF)

P_D @ F=15 KHz = C $V^2 \cdot f$ = 9.6 W

(Balancing Losses/handled power) = 0.4 %
Photo 3 shows devices behaviour with the conditions of the example and C = 1500pF.

4.4 SERIES OF IGBTs.

Photo 4 shows the behaviour of two 1000 V IGBTs in series at turn-off using an inductive load with sharing capacitors (1500pF). Due to the high fall time value (figure 9), the total voltage (V_{CE1} + V_{CE2}) can reach the clamping voltage before the end of current fall.

Therefore, the equation (6) can not be simplified and ΔV_R must be split as follows:

$$\Delta V_R = \Delta V_{R1} + \Delta V_{R2}$$

where:

$\Delta V_{R1} = V_1 - V_2$ @ $t = t_a$ (photo 4) is due both, to the delay turn-off time difference, and to the difference of current tail during voltage rise.

ΔV_{R2} is due to the difference of sharing capacitor charge when $V_1 + V_2 = V_{CLAMP}$ = constant due to the difference of current tail and Δt_{FALL}: $\Delta V_2 = \Delta Q_2/2C$

The minimum value of sharing capacitor can not be calculated easily due to the influence of dV/dt on the current tail behaviour.

For easy evaluation, the charge time of the sharing capacitor ($t_a - t_0$) must be equal to the maximum t_{FALL}. In this case:

$$C = 2 \cdot (I_{OFF} - I_{TAIL}/2) \cdot t_{FALLmax}$$

$$\Delta V_R = \Delta V_{R1} = (\Delta t_{OFF} \cdot (I_{OFF} - I_{TAIL}/2))/C + \Delta I_{TAIL} \cdot t_{FALLmax}/2C$$

Δt_{OFF} depending on gate charge spread is temperature independent.

I_{TAIL}, ΔI_{TAIL}, t_{FALL} are temperature dependent as shown in figure 13.

EXAMPLE 5:

Series of two IGBTs STGH8N100.

Ratings:

V_{CESmax} = 1000 V

I_{Cmax} = 8A @ Tc=125°C

t_{FALL} = 800ns ± 20% @ Tc =125°C

(see figure 9)

Gate charge ≈ 60 nc ± 5%

(similar to STHV102)

Conditions:

V_{CLAMP} = 1600 V

ΔV_{Rmax} = 200V

I_{Cmax} = 8 A

Tj_{max} = 125°C

I_{GATE} = 100mA

f = 15Khz, duty cycle = 0.5

Solution:

$C = 2 \cdot (I_{OFF} - I_{TAIL}/2) \cdot t_{FALLmax} / V_{CLAMP} = 7.8$ nF

$\Delta t_{OFF} = \Delta (Q_1 + Q_2)/I_G =$
6.2 E - 9/ 100 E - 3 = 62ns.

$\Delta V_R = \Delta V_{R1} = (\Delta t_{OFF} \cdot (I_{OFF} - I_{TAIL}/2))/C + \Delta I_{TAIL} \cdot t_{FALLmax}/2C = 113$ V

Resulting $\Delta V_R << 200$ V, a 6.8 nF capacitor can be used and ΔV_R=130V.

Balancing losses =

$$P_D\ (15KHz) = C \cdot V^2 \cdot f = 65W$$

(Balancing Losses/handled power) =

$$P_D / V_{max} \cdot I \cdot 0.5 = 1\ \%.$$

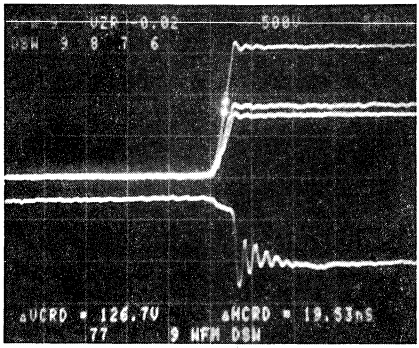


Photo 3. Load current and voltage sharing of two Power MOSFET STHV102 in series as shown in figure 5. C_S = 1.5nf, Δt_{off} = 60ns, I = 2A/div, V = 500V/div.

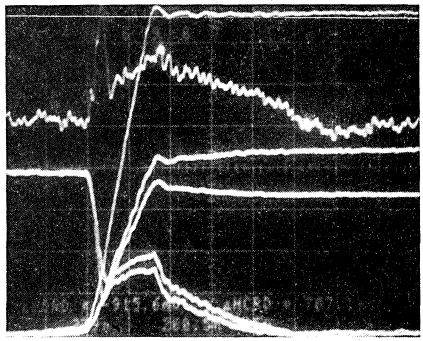


Photo 4. Turn-off behaviour of two IGBTs STGH8N100 in series with syncronized driving pulses. C = 1.5nF, T_j = 100°C. I=2a/div, I_{CHARGE}=0.5A/div, V=200V/div.

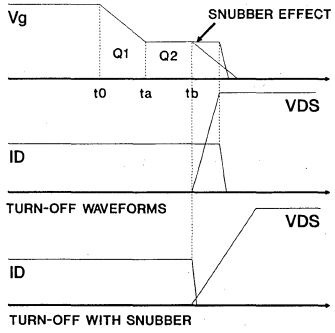


Fig. 10. Turn-off behaviour of Power MOSFET when connecting snubber capacitors.

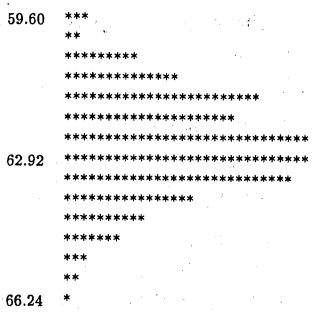


Fig. 11. Spread of the Power MOSFET gate charge.

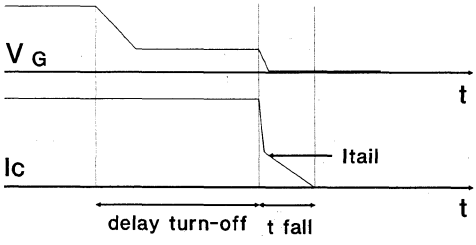
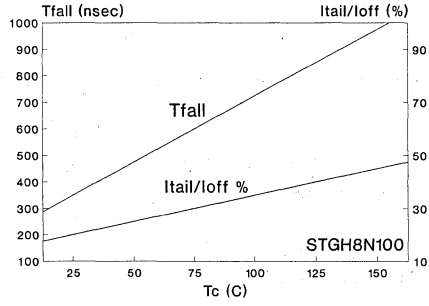


Fig. 12. Current fall behaviour of IGBT devices.



Vce= 800V , Ic=8A , Vg=15V , Rg= 100ohm

Fig. 13. t_{FALL} and current tail of IGBTs vs junction temperature.

5.0 CONCLUSIONS.

Every switching power device can be connected in series successfully in order to make a power switch for fast switching applications working at a voltage greater than 1500 V.

For optimum voltage sharing during steady state and switching, it is necessary:

- to make a compromise with the additional power losses introduced by sharing capacitors and by sharing resistors.
- that the junction temperature difference between devices in series must be as low as possible; especially for bipolar transistors and IGBTs.

Bipolar transistors require a selection by storage time.

Power MOSFETs are temperature independent and have very low parameter spread, making them easy to connect in series.

IGBTs need considerable sharing capacitors, but these devices are attractive thanks to their very low saturation voltage and low driving energy.

The driving circuit can be made either by using a trahformer for syncronized driving pulses, or with a diode and capacitor network.

When using a transformer, driving voltage or current can be controlled easily, but, continuous mode and a wide range of duty cycle can be a problem .

The diode and capacitor network allows equalisation of devices turn-off time, so reducing sharing capacitors value when gate voltage controlled devices are used. This method requires hard optimization of the circuit for very fast switching applications.

NOVEL PROTECTION AND GATE DRIVES FOR MOSFETs USED IN DRIDGE-LEG CONFIGURATIONS

BY C. PATNI

INTRODUCTION

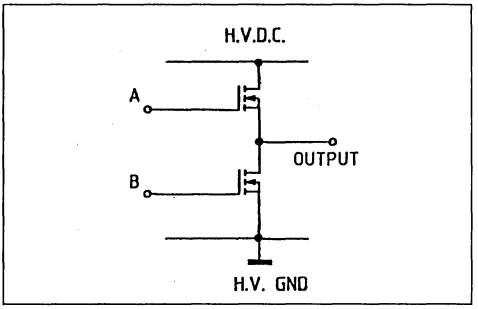
The bridge-leg is an important building block for many applications such as drives and switch-mode power supplies. Simple gate drives with protection for POWER MOSFETs need to be designed for the "low-side" and the "high-side" switches in the bridge-leg. The POWER MOSFET can conduct a peak drain current, I_D, which is more than three times its continuous current rating. The POWER MOSFET peak current capability and its linear operating mode are used to good effect in designing device protection circuitry.

Bridge-leg configurations have a direct bearing on the degree of protection that can be incorporated. Consequently, bridge-leg configurations, protection concepts and gate drives are created simultaneously to design optimised and reliable power electronic circuits.

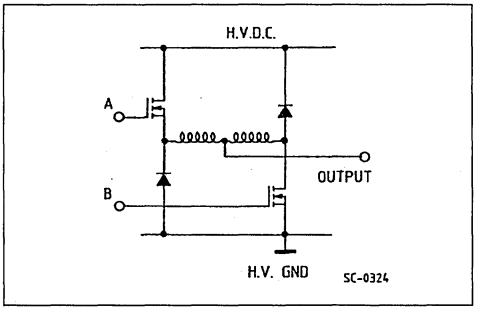
H-BRIDGE USING POWER MOSFETs

Three POWER MOSFET based bridge configurations are illustrated in figure 1. Figure 1a illustrates a bridge-leg which uses the internal parasitic diode as a free-wheeling diode thus reducing cost. However, since the reverse recovery of this parasitic diode is in the order of a microsecond, the turn-on switching times of the POWER MOSFET have to be increased in order to reduce the reverse recovery current. The turn-on time of the POWER MOSFET is controlled such that the pulse current rating of the internal diode is not exceeded. Hence a compromise is made between maintaining the safe operating area of the MOSFET and reducing turn-on switching losses. For example, an SGSP477 MOSFET has a diode pulse current rating in excess of 80A and a typical diode reverse recovery time of 300ns. A rate of change of current at turn-on, limited to 50A/s, is a realistic compromise between reverse recovery current magnitude and turn-on losses. Consequently switching speed is sacrificed for cost. For switching frequencies up to 10kHz, when operating on a 400V DC high voltage rail, this configuration can be chosen as switching losses are limited, thus enabling a realistic thermal design.

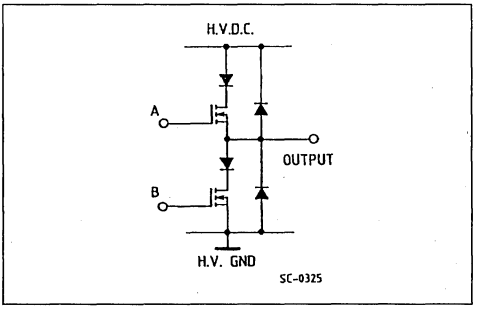
Figure 1 : Bridge Configurations.



a) Bridge-leg using Internal Parasitic Diode.



b) Asymetrical Bridge-leg providing di/dt Protection.



b) Bridge-leg with blocking Diodes.

The turn-off speed of the POWER MOSFET in this configuration has no restrictions. Thus a fast turn-off is desirable to reduce turn-off losses. As the rate of change of current is limited, radio frequency interference (RFI) and electromagnetic interference (EMI) are reduced.

An asymmetrical bridge-leg, illustrated in figure 1b ; can be used to limit di/dt during a short-circuit condition thus providing sufficient time to switch-off the appropriate power devices. The inductors limit the rate of rise of output current. They also limit the free-wheeling current through the internal parasitic diodes of the MOSFETs. Adding external free-wheel diodes and inductors increases reliability at the cost of increased complexity. The inductors reduce RFI and EMI as the rate of change of current is limited.

The configuration illustrated in figure 1c has Schottky "blocking" diodes to prevent current going through the MOSFET internal parasitic diodes. Schottky diodes are often used since conduction losses are kept to a minimum.

Bridge configurations shown in figure 1b and 1c are considered for high frequency switching applications. The advantage of the asymmetrical bridge-leg configuration over the bridge configurations in figures 1a and 1c is that the bridge-leg is capable of withstanding simultaneous conduction of the two devices in the bridge-leg since there are series inductors which reduce the dI/dt under this condition. Hence the short-circuit detection loop time is not so critical and the devices are not stressed with high dI/dt and high pulse currents.

The choice of the bridge configuration depends on the technical specification of the application. For example, if the technical specification for a specific application can be met by using the configuration shown in figure 1a, then this configuration should be used as costs are lower than with the other two configurations shown in figures 1b and 1c.

GATE DRIVE CIRCUITS

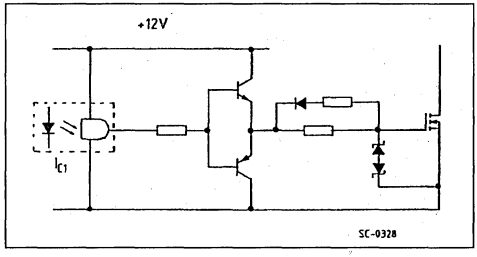
The POWER MOSFET is a voltage controlled device, unlike the bipolar transistor which requires a continuous base drive. An application of a positive voltage between the gate and the source results in the device conducting a drain current. The gate to source voltage sets up an electric field which modulates the drain to source resistance. The following precautions should be considered when designing the gate drive ;

1 - Limit V_{GS} to 20V maximum. Use of a gate to source voltage in excess of 16V has a marked effect on the lifetime of the device.

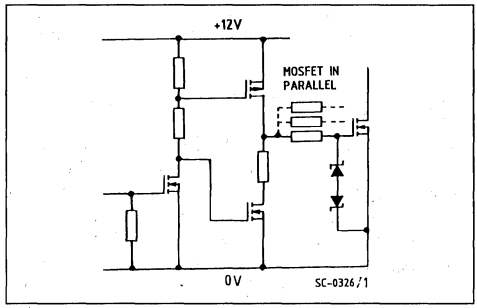
2 - Gate drive parasitic inductance can cause oscillations with the MOSFET input capacitance. This problem becomes more pronounced when connecting devices in parallel.

3 - There should be sufficient gate to source voltage for the transistor to be fully conducting.

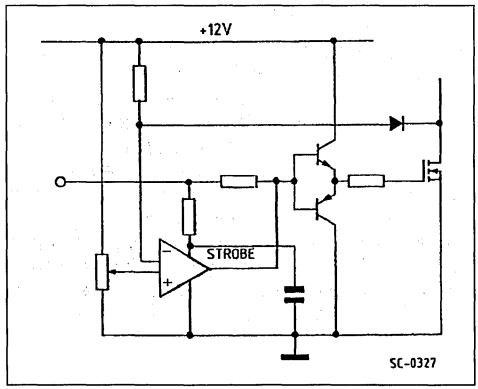
Figure 2 : Gate Drive Circuits.
a) Isolated gate drive with controllable switching times.



b) Simple gate drive for N-Channel MOSFETs in parallel.



c) Gate drive with VDS (on) control for short-circuit protection.



Bipolar, MOSFET, CMOS or open-collector TTL logic can be used in the design of simple high performance gate drives. Totem-pole buffers, (figure 2a), are often effectively used to control the turn-on and turn-off individually. Figure 2b illustrates a total MOSFET based gate drive with which the switching speeds at turn-off can be individually controlled. CMOS or open-collector TTL logic can be used to drive MOSFETs directly, provided an ultrafast switching speed (50ns) is not necessary. In motor drive applications switching speeds of 100 to 200 nanoseconds are sufficient as switching frequency is seldom in excess of 50kHz. Discrete buffers are used to provide high current source and sinking capability when improved switching speeds are required or when MOSFETs are connected in parallel.

Short-circuit protection techniques similar to bipolar transistors may be considered for MOSFETs. $V_{DS(on)}$ monitoring permits the detection of short-circuit conditions which lead to device failure. The device can be switched off before the drain current reaches a value in excess of the peak pulse current capability of the MOSFET. This form of protection is very effective with MOSFETs as they can sustain a pulse current in excess of three times the nominal continuous current. Figure 2c illustrates a gate drive which incorporates $V_{DS(on)}$ monitoring and linear operating mode detection for the MOSFET in the case of short-circuit conditions. When the MOSFET is turned on the on-state voltage of the device ($V_{DS(on)}$) is compared with a fixed reference voltage. At turn-on, $V_{DS(on)}$ monitoring is inhibited for a period of approximately 400ns in order to allow the MOSFET to turn-on fully. After this period, if $V_{DS(on)}$ becomes greater than the reference value, the device is latched-off until the control signal is turned-off and turned-on again.

"HIGH-SIDE" SWITCH GATE DRIVES

The top transistor in a bridge-leg requires a "high-side" gate drive circuit with respect to the bridge ground. Three possible gate drive concepts are shown in figure 3 :

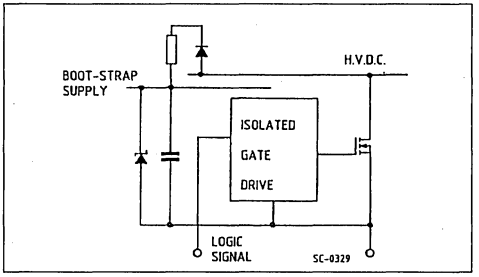
a) The "bootstrap" drive, requiring logic signal isolation, but no auxiliary floating supply.

b) The level shifting drive.

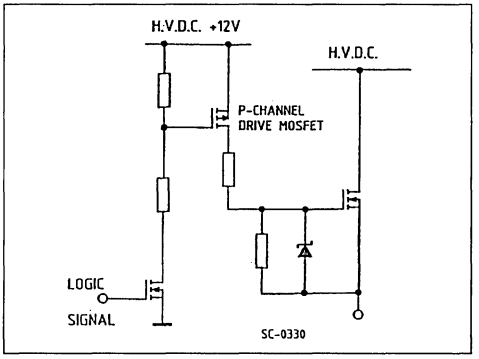
c) The floating gate drive with optically coupled isolators, pulse transformers or DC to DC chopper circuit with transformer isolation.

Figure 3 : Gate Drives for Top Transistor of Inverter Leg.

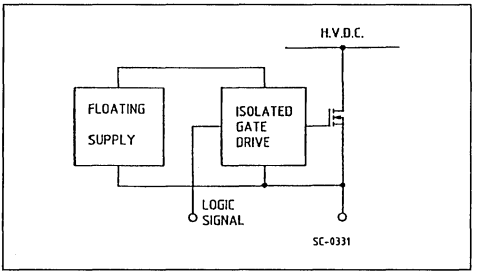
a) "Bootstrap" supply floating gate drive.



b) Level shifting gate drive.



c) Floating supply isolated gate drive.



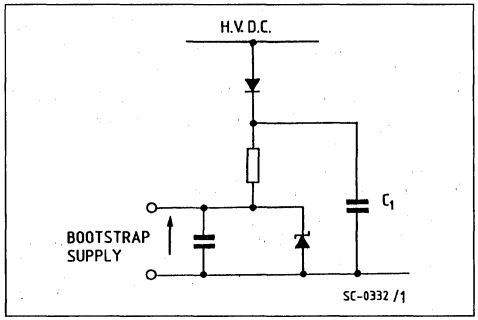
Bootstrap supplies are particularly well suited to POWER MOSFET gate drives which require low power consumption. Figure 4 illustrates two bootstrap supply techniques. Bootstrap supplies limit transistor duty cycle since they require a minimum transistor off time during which they are refreshed.

Supply efficiency and maximum duty-cycle are parameters which govern the design of the bootstrap. Figure 4a illustrates a conventional bootstrap with an additional capacitor, C1, which improves the maximum duty cycle as the supply is refreshed even during transistor on time by this capacitor. Figure 4b illustrates a high efficiency bootstrap supply which uses a small MOSFET, Q1, for regulation. In this design a low power bootstrap drives the gate of Q1.

The level shifting gate drive, (figure 3b), requires a high voltage p-channel MOSFET which drives the n-channel power device. The p-channel MOSFET is switched using a resistor divider network. No floating supplies are required. A power supply of 12V, referenced to the high voltage d.c., is used to provide positive gate source voltage for n-channel POWER MOSFET. This circuit eliminates the need for logic signal isolation and a floating supply. The disadvantage of this circuit is the high cost of the p-channel drive MOSFET.

Figure 3c illustrates a floating gate drive with a floating supply. This drive is the most expensive out of the three shown in figure 3. However, the floating supply need only have a low output power, since MOSFETs are voltage controlled devices. The advantages of this drive are its high efficiency and unrestricted transistor duty-cycle.

Figure 4 : Bootstrap Supply Techniques.
a) Conventional bootstrap with additional capacitor C1.



b) High efficiency bootstrap.

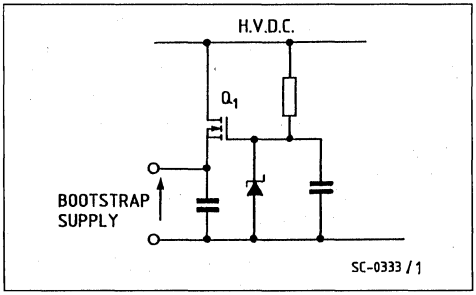
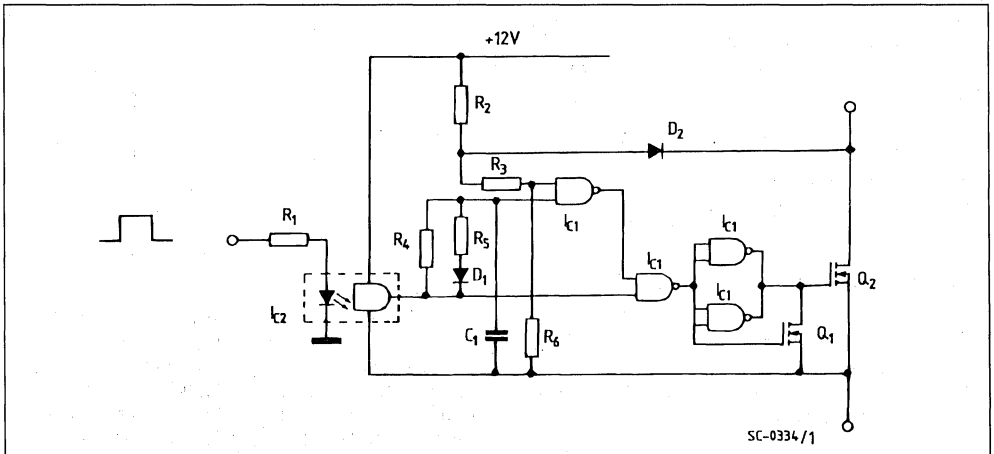


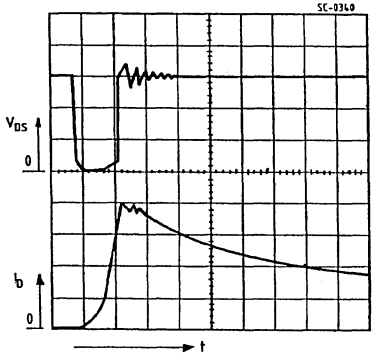
Figure 5 : Isolated CMOS Drive with V_{DS} Control for Short-circuit Protection.



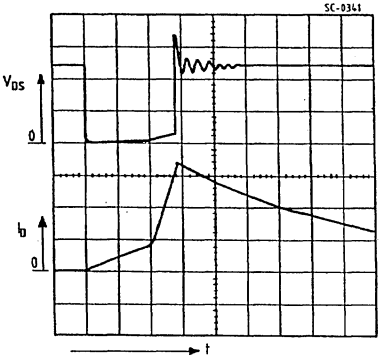
R1	= Dependent on application	R4	= 1kΩ	I_{C2}	= HCPL2200	Q1	= BSS100
R2	= 10kΩ	R5	= 120kΩ	C1	= 560pF	Q2	= SGSP477
R3	= 22kΩ	R6	= 56kΩ	D1	= 1N41448		
		I_{C1}	= HCF4093	D2	= BYT11/600		

Figure 6 : Short-circuit Conditions for an SGSP477 V_{DS} & I_D.

V_{DS} : 50V/DIV
I_D : 10A/DIV
t : 2µs/DIV
a) Output to high voltage short-circuit.



b) Output to Output Short-circuit.



PROTECTION

Power electronic circuits such as bridge-legs are often required to have protection against output to output short-circuit, over-temperature, simultaneous conduction of devices in series in a bridge-leg and output to high voltage supply or ground rail short-circuit. These power stages are generally part of an expensive system such as a machine-tool or a robot motor drive. Thus the additional cost of protection circuitry is commercially acceptable. A compromise is generally reached between equipment costs and the degree of protection required.

Short-circuit protection of a power MOSFET can be achieved by either $V_{DS(on)}$ monitoring or a current sense. In the previous section gate drives using the $V_{DS(on)}$ monitoring technique were presented. Figure 6 illustrates the MOSFET drain to source voltage, V_{DS}, and the drain current, I_D, when short-circuits are experienced by the POWER MOSFET, SGSP477, driven by the gate drive illustrated in figure 5.

The MOSFET is turned-off when the drain current increases sufficiently and $V_{DS(on)}$ monitoring is inhibited for a period of 400ns to allow the device to turn-on fully.

An inductor is used in series with the device, as illustrated in figure 1b. This inductor saturates when a large short-circuit current flows. The rate of change of the short-circuit current due to the saturation of this inductor is illustrated in figure 6a and 6b. Figure 6a illustrates the POWER MOSFET drain to source voltage, V_{DS}, and the drain current, I_D, when a bridge-leg output to high voltage supply rail short-circuit occurs. Figure 6b illustrates an output to output short-circuit of two bridge-legs.

Another protection technique uses the "current mirror concept", (1). An image of drain current is obtained by having a small MOSFET, (integral or discrete), in parallel with the main power MOSFET as illustrated in figure 7.

Figure 7 : The Current Mirror.

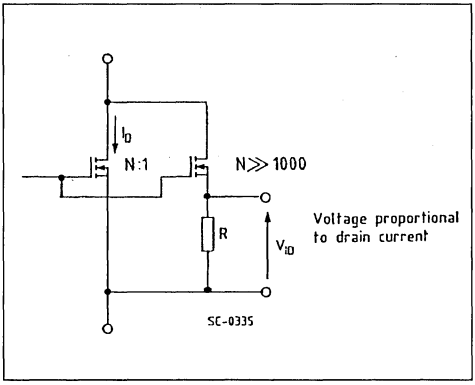
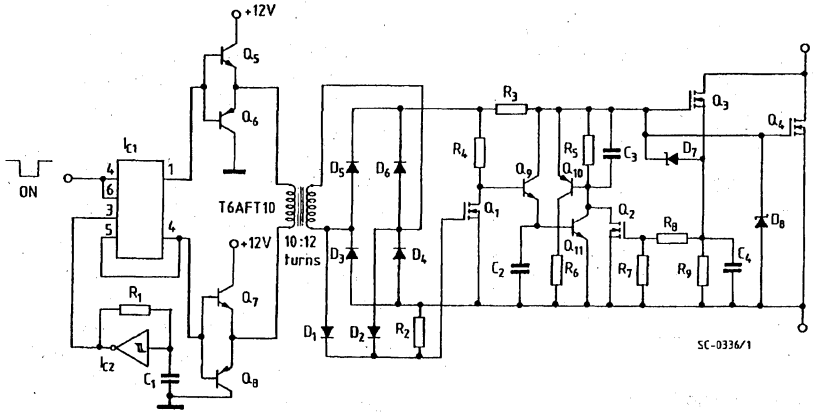


Figure 8 illustrates a floating gate drive which utilizes a pulse transformer for transmitting simultaneously the MOSFET on-signal together and the gate to source capacitance charging current. The current mirror technique is used to provide short-circuit and over-load current protection. The pulse transformer operates at an oscillating frequency of 1MHz when a turn-on control signal is present.

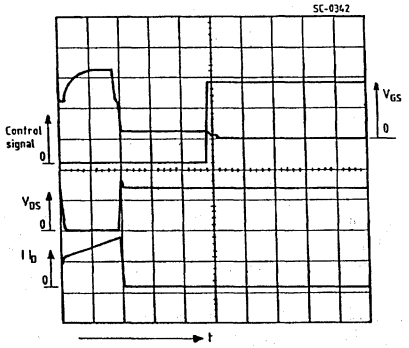
The secondary is rectified to provide the gate source capacitance charging voltage. The current mirror provides a voltage "image" of the main MOSFET drain current. This voltage is compared with a fixed reference voltage in order that the gate drive be latched-off when the drain current becomes in excess of a specificed value. Figure 9 illustrates how the MOSFET, SGSP477, is latched-off when the drain current exceeds 10A with this gate drive circuit.

Figure 8 : Pulse Transformer Gate Drive with Current Mirror Protection for an SGSP477.



R1 = 470Ω	R9 = 100Ω	D4 = 1N4148	Q4 = SGS477
R2 = 1kΩ	C1 = 330pF	D5 = 1N4148	Q5 = BC337
R3 = 33Ω	C2 = 10nF	D6 = 1N4148	Q6 = BC327
R4 = 2kΩ	C3 = 10nF	D7 = BZX85C15	Q7 = BC337
R5 = 100Ω	C4 = 220pF	D8 = BZX85C15V	Q8 = BC327
R6 = 100Ω	D1 = 1N4148	Q1 = small	Q9 = BC337
R7 = 100Ω	D2 = 1N4148	Q2 = signal	Q10 = BC327
R8 = 100Ω	D3 = 1N4148	Q3 = n-channel MOSFETs	Q11 = BC337

Figure 9 : Overload Current Protection using Current Mirror Concept with the Gate Drive of Figure 8 for an SGSP477.



Time scale : 5µs/DIV – I_D : 5A/DIV – V_{DS} : 100V/DIV
Control signal : 5V/DIV – V_{GS} : 5V/DIV.

CONCLUSION

MOSFET based bridge-leg configurations requiring protection and floating gate drives have been presented. Novel self-protecting gate drives for the "high-side" and "low-side" switching have been discussed. These drives provide protection against output to high voltage d.c., output to ground and output short-circuit. For the high-side switch "bootstrap" supply gate drive, level shifting gate drive and floating supply isolated gate drives have been compared.

Protection against short-circuit condition has been demonstrated using $V_{DS(on)}$ monitoring and the current mirror concept. Both techniques are well suited for protection against short-circuit conditions. However, the current mirror concept also provides a sufficiently linear image of the current for regulation.

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1. Fuy G.
Current-mirror FETs cut costs and sensing losses EDN September 4 th, 1986.

USE OF INTERNAL MOSFET DIODE IN BRIDGE-LEGS FOR HIGH FREQUENCY APPLICATIONS

By C.K. PATANI - D. STEED - J.M. CHARRETON

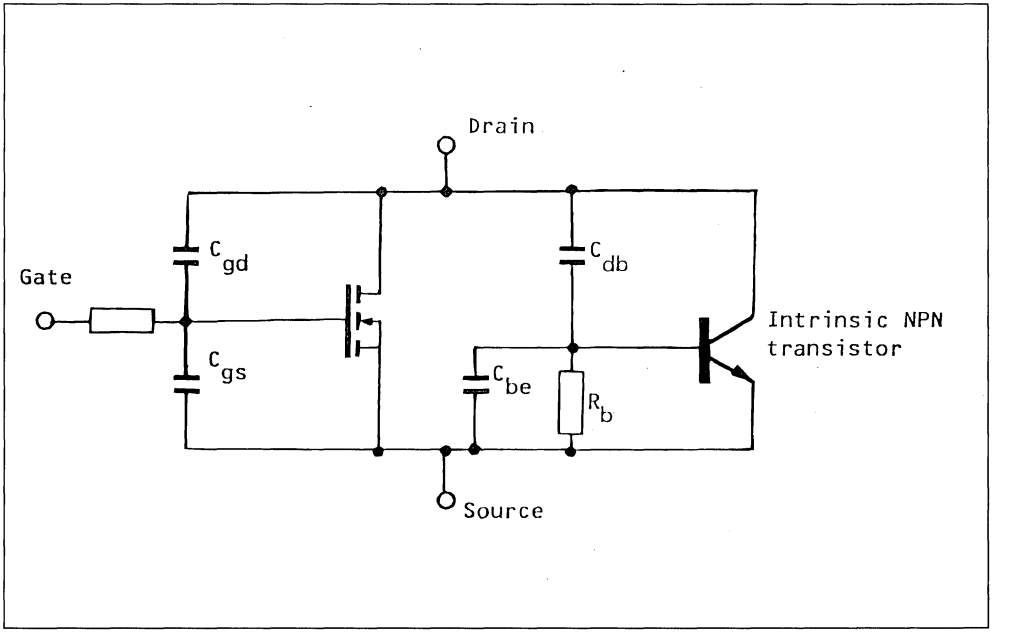
ABSTRACT

Reverse recovery of the intrinsic MOSFET diodes is investigated for the classical MOSFET and the MOSFET with minority carrier lifetime control. Turn-on losses in bridge-legs using intrinsic MOSFET diodes limit the switching frequency particularly in the case of the classical MOSFET. Adapted bridge-leg configurations are presented which enable the use of the intrinsic MOSFET diodes for the free wheeling function in inductive load switching without any appreciable reverse recovery current and MOSFET turn-on switching losses !

INTRODUCTION

The MOS field effect transistor (MOSFET) contains an intrinsic PN diode within the structure which can conduct a current from source to drain. The PN junction diode is in fact part of a parasitic NPN bipolar transistor as shown in figure 1. Free-wheeling diodes in bridge-legs are necessary when switching inductive loads. The intrinsic diode can be used to fulfil this free-wheeling function. However, the intrinsic diode of the classical MOSFET has a long reverse recovery time and "snap-off" characteristic which can cause large dV/dt. The snap-off can result in the device failing in one of two ways. Firstly, due to internal capacitances, C_{db} and C_{be}, a base current may be established which turns-on the intrinsic bipolar transistor (see figure 1)[1]. Secondly, the dV/dt may be such that the drain to source voltage of the MOSFET exceeds the blocking voltage thus causing avalanche breakdown. This paper investigates various means of limiting the maximum reverse recovery current of the intrinsic diode to ensure reliable operation. A comparison is made between the novel solutions presented permitting the use of internal diode, and conventional solutions for using MOSFETs in bridge-legs, such as lifetime controlled MOSFETs and series blocking diodes.

Figure 1 : Equivalent Circuit for a MOS Field Effect Transistor (MOSFET).



METHODS OF LIMITING REVERSE RECOVERY CURRENT

Limiting the reverse recovery current of the intrinsic diode can be achieved by stopping current from passing through the blocked MOSFET by means of a series blocking diode or limiting the rate of change of current in the intrinsic diode. The snap-off characteristics of the internal diode can be limited by having small RC snubbers across the drain to source of MOSFETS in bridge-leg configuration. Solutions which limit the rate of change of current in the intrinsic diode are discussed below.

BRIDGE-LEG DESIGNS UTILIZING MOSFET INTRINSIC DIODES

a) SOLUTION WITH UNCOUPLED UNSATURABLE INDUCTORS

In the circuit shown in figure 2, if T1 is blocked and T2 is conducting, the load current flows through T2. As T2 turns-off the current transfers to the freewheeling diode D2, as the rate of change of current into the intrinsic MOSFET diode of T1 is limited by inductors L1 and L2. The zener voltage across Z2 causes the current to transfer from the external freewheeling diode D2 to the intrinsic MOSFET diode in T1 until D2 no longer conducts (as shown in figure 3). When T2 is turned-on subsequently the current transfers from the intrinsic diode of T1 to T2. The reverse recovery of the intrinsic diode is, however, limited by inductances L1 and L2. This can be seen clearly in figure 4. The bridge-leg can be designed (by dimensioning L1, L2 and V_Z) such that the external freewheeling and zener or transil diodes only conduct for a small fraction of the freewheeling period. Consequently, they do not have to be mounted on a heatsink. The disadvantage of using the zener is that the MOSFETs must now be rated for at least the high voltage DC rail, HVDC, plus the zener voltage.

Figure 2 : Bridge-leg with Uncoupled Unsaturable Inductors.

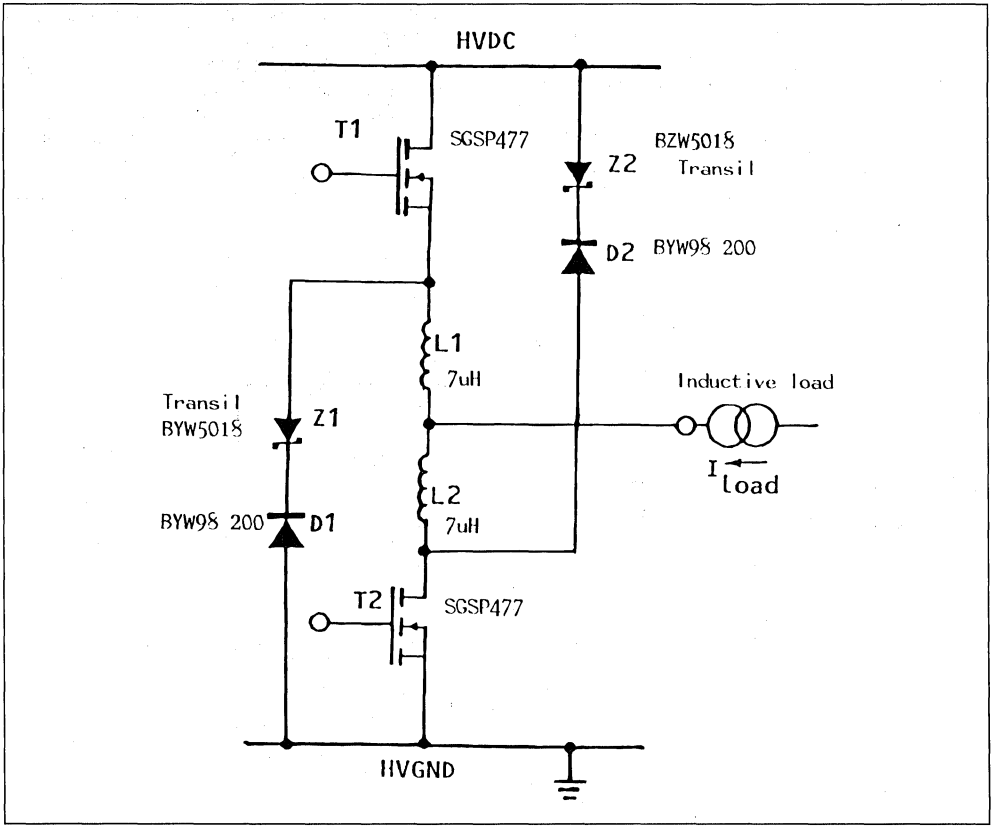
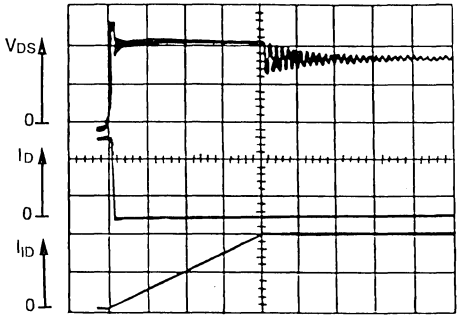


Figure 3 : Transfer of Current to Intrinsic Diode.

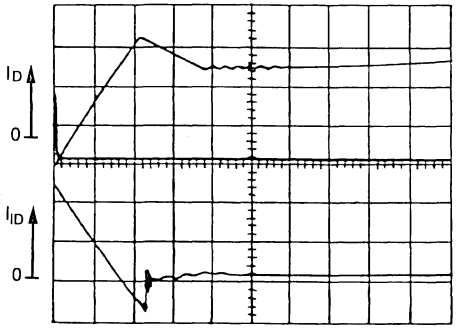


Time scale : 2µs/DIV
V_{DS} : 50V/DIV
I_D : 10A/DIV

Intrinsic
Diode : 10A/DIV
Current (I_{ID})

MOSFET : SGSP477

Figure 4 : Turn-off of the Intrinsic Diode.



Time scale : 1µs/DIV
V_{DS} : 50V/DIV
I_D : 10A/DIV

Intrinsic
Diode : 10A/DIV
Current (I_{ID})

MOSFET : SGSP477

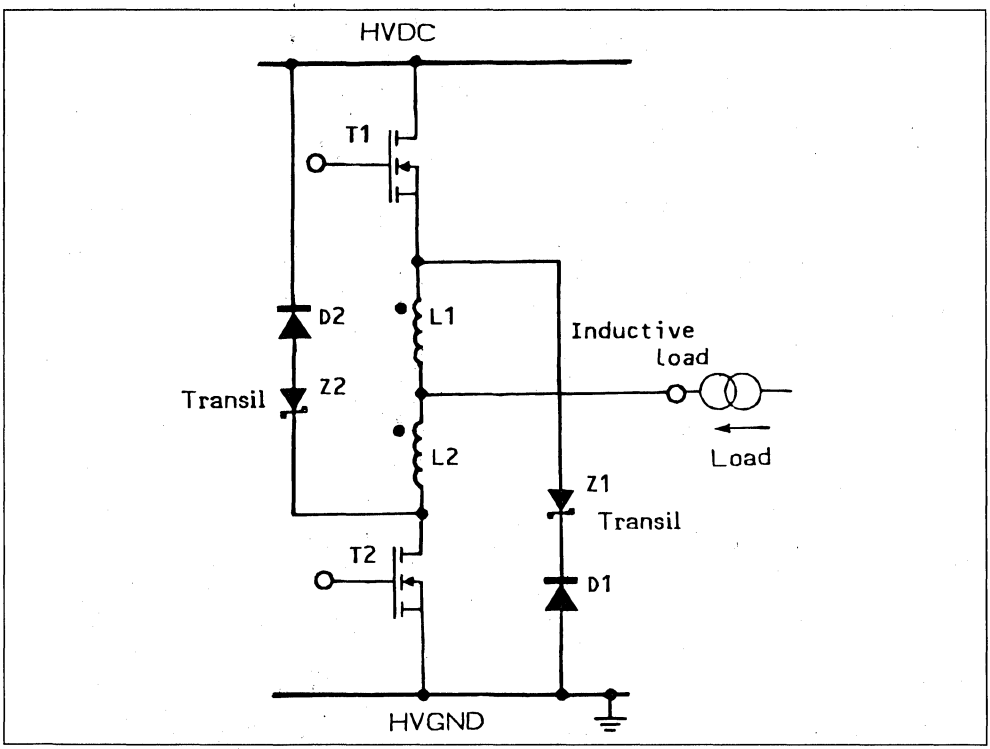
Another advantage of inductances L1 and L2 in the circuit is that they limit the build up of current during fault conditions such as simultaneous conduction of the two devices.

L1 and L2 must be chosen such that their inductances are big enough to prevent intrinsic diode reverse recovery problems hence reduce losses. They must be small enough to allow current to transfer from the freewheeling diodes D2 and D1 to the intrinsic MOSFET diodes in T1 and T2 such that the average current passing through the external diode and zener or transil is low.

b) SOLUTION WITH MUTUALLY COUPLED INDUCTORS

Inductors L1 and L2 can be mutually coupled as shown in figure 5. Coupling L1 and L2 doubles the inductance between transistors T1 and T2 (SGSP477), thus reducing the reverse recovery problem of the intrinsic diode as the rate of change of current is reduced. Coupling, therefore, saves the cost of one core and less windings are necessary to provide the same degree of protection as in the case of uncoupled inductors. The voltage and current waveforms of the MOSFETs and their intrinsic diodes for this solution are similar to that obtained with solution (a).

Figure 5 : Bridge-leg with Mutual Inductors.



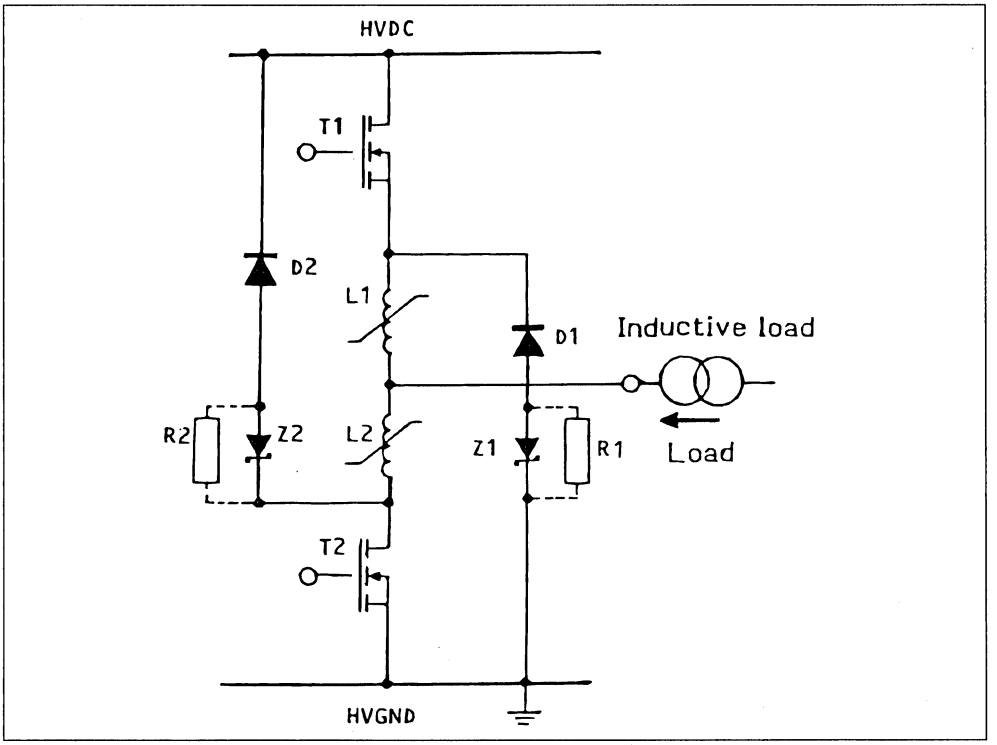
C) SOLUTION WITH SATURABLE INDUCTORS

Saturable inductors such as toroids with a few turns can be used in the bridge configuration shown in figure 6. Saturable inductors are better suited than non-saturable inductors in so much as they can be used to limit the reverse recovery of the intrinsic diode to an almost negligible level. The saturable inductor is designed to saturate after the intrinsic diode has reverse recovered. Before saturation the inductor presents a high impedance and only a low magnetising current flows.

In figure 6, it is assumed that T1 and T2 are blocked and the intrinsic diode of T1 is conducting. If T2 is now turned-on, the current in the intrinsic diode decreases rapidly since inductor L1 is saturated until this current reverses resulting in negative volts-seconds across the inductor which thus desaturates. The inductor thus presents a high impedance while the current through it is equal to or less than the magnetising current. The intrinsic MOSFET diode begins to reverse recover as the current through it becomes negative. The inductor is designed not to saturate for a period of at least 1µs, thus enabling the reverse recovery of the intrinsic diode without excessive reverse recovery current. There is a certain degree of minority carrier recombination while the inductor is unsaturated which also reduces the maximum reverse recovery current, I_{RM}. The reverse recovery of the intrinsic diode can be seen in figure 7.

While T2 is conducting the load current inductor L2 is saturated. When T2 turns-off the MOSFET current transfers to diode D2. The free-wheeling current path through the intrinsic diode of T1 has a high impedance due to L1 being unsaturated. Consequently the build-up of current through the intrinsic diode of T1 is slow until this current reaches a value equal to the magnetising current, I_{mag}, of inductor L1 which then saturates. This effect can be clearly seen in figure 8.

Figure 6 : Bridge-leg with Saturable Inductors.



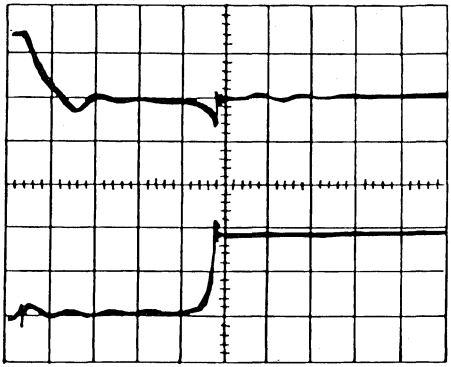
The turn-on of the MOSFET in the solution with saturable inductors (shown in figure 6) is illustrated in figure 9. It can be seen that the MOSFET losses are negligible, since the saturable inductor in series with the MOSFET that turns-on, limits the rate of rise of current while it is unsaturated. Figure 9 also illustrates that the reverse recovery of the intrinsic diode of the free wheeling MOSFET is also limited..

In the bridge-leg with saturable inductors (figure 6), if transils (Z1 and Z2) and resistors (R1 and R2) are removed, the external free-wheeling diodes have to be of high current rating as they conduct all the load current until the saturation of L1 and L2. Subsequently the external diode shares part of the free-wheeling current with the intrinsic diode. It is advantageous to reduce the current through the external free-wheel diodes D1 and D2 as rapidly as possible for the following reasons :

1. If D1 and D2 conduct for a small fraction of the maximum free-wheeling duty cycle, then their power rating is substantially reduced.
2. If the free wheeling current through the external diode D1 or D2 is reduced rapidly, the inductor in series (L1 or L2) is no longer saturated. At the consecutive turn-on of T1, L1 presents a high impedance thus performing a turn-on snubber function. Transistor turn-on losses are thus minimised particularly for inductive loads.
3. Output short-circuit protection is also enhanced if the inductors are unsaturated prior to transistor turn-on.

The current through the external free-wheeling diodes can be reduced rapidly by increasing the rate of release of inductor stored energy by transils (Z1 and Z2) and/or resistors (R1 and R2) as shown in figure 6.

Figure 7 : Reverse Recovery of Intrinsic Diode using Saturable Inductors in the Configuration of Figure 6.



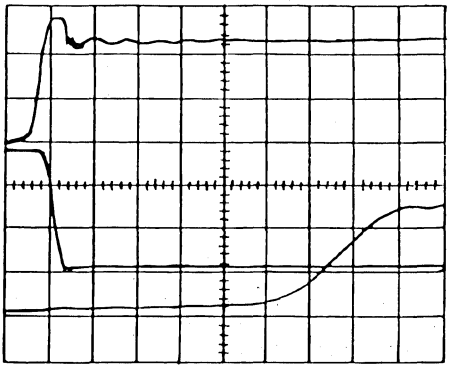
Time scale : 500ns/DIV

Intrinsic
Diode Current
I_{ID} : 10A/DIV

Voltage across
MOSFET intrinsic
diode
V_{ID} : 50V/DIV

Time scale : 500ns/DIV

Figure 8 : Transfer of Current to Intrinsic Diode using Saturable Inductors in the Configuration of Figure 6.

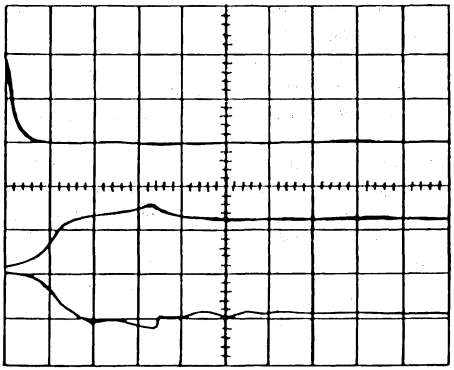


V_{DS} : 50V/DIV
I_D : 5A/DIV

Intrinsic
Diode : 5A/DIV
Current (I_{ID})

MOSFET : SGSP477

Figure 9 : Turn-on of the MOSFET in the Configuration with Saturable Inductors.
(The turn-on snubber and the intrinsic diode reverse recovery actions are illustrated).



Time scale : 500ns/DIV
V_{DS} : 50V/DIV
I_D : 10A/DIV

Intrinsic
Diode : 10A/DIV
Current (I_{ID})

MOSFET : SGSP477

Table 1 : Advantages and Disadvantages of Solutions for limiting Reverse Recovery Current in the Intrinsic MOSFET Diode.

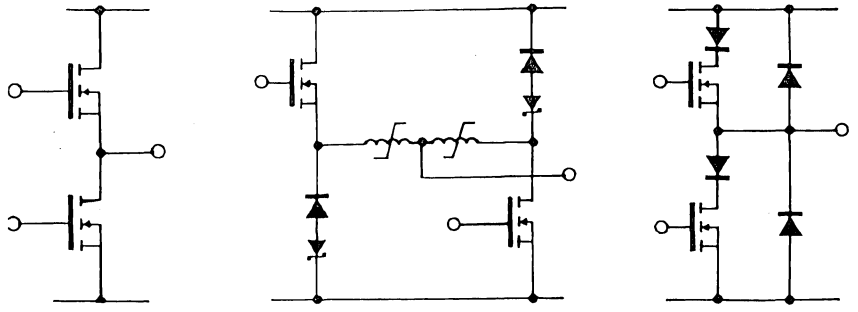
Sol.	Type of Protection Used	Advantages	Disadvantages
a)	Unsaturable Inductors	– Reduction of turn-on losses. – Controlled dI/dt at turn-on. – Controlled reverse recovery of intrinsic diode.	– In order to use low current rated freewheeling diodes, transil diodes have to be used . increasing the voltage rating of the MOSFETs in the circuit.
b)	Unsaturable Mutual Inductances	– Smaller and less expensive than two inductors since only one coupled inductor. – As above.	– As above.
c)	Saturable Inductors	– Negligible turn-on losses. – Negligible intrinsic MOSFET diode reverse recovery losses. – Controlled dI/dt turn-on.	– As above.

COMPARISON OF USE OF INTRINSIC MOSFET DIODE WITH ALTERNATIVE SOLUTION

Figure 10 illustrates three bridge-leg configurations that can be used with MOSFETs when switching inductive loads. Figure 10a) illustrates a bridge-leg which uses the intrinsic diode of a classical MOSFET having a reverse recovery in the order of a microsecond. The same configuration can be used with a lifetime controlled MOSFET which has an intrinsic diode having a reverse recovery time around 250ns. An asymmetrical bridge-leg illustrated in figure 10b), is similar to the above mentioned solutions permitting the use of the intrinsic diode. The configuration illustrated in figure 10c) has series "blocking" diodes which prevent conduction of the intrinsic MOSFET diodes and thus avoid reverse recovery problems associated with the slow intrinsic diodes. In this configuration fast recovery epitaxial diodes are used as external free wheeling diodes.

Tests were performed using 500V, 0.6 ohm at 25°C classical MOSFETs (BUZ353) and lifetime controlled MOSFETs in the bridge-leg illustrated in figure 10a). Experimentally obtained losses within the diode and the MOSFET at turn-on are presented in figure 11. The solution enabling the use of the intrinsic diode without reverse recovery problems (figure 10b) has practically no losses due to reverse recovery of the intrinsic diode.

Figure 10 : Bridge-leg Configurations.



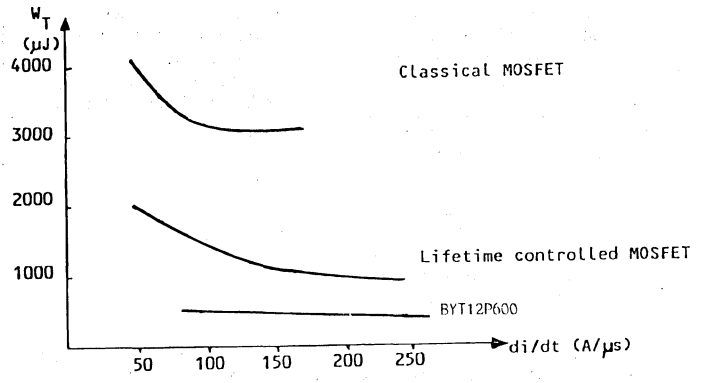
a) Bridge-leg using intrinsic MOSFET diode

b) Asymmetrical bridge-leg providing di/dt protection, turn-on snubber and limited reverse recovery problems

c) Bridge-leg with series blocking diodes and fast freewheeling diodes

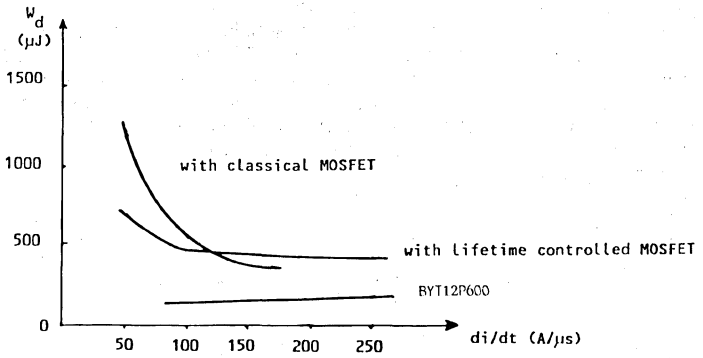
Figure 11 : Turn-on Losses in a Bridge-leg.

Turn-on Losses in the MOSFET



a) Turn-on losses in the MOSFET when switching 10A inductive load current on 400V_{DC} rail as a function of the rate of change of MOSFET drain current (dI_D/dt)

Reverse Recovery Losses in the Diode

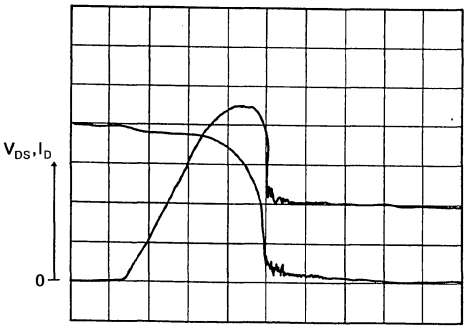


b) Reverse recovery losses in the freewheeling diode when switching 10A inductive load current on 400V_{DC} rail as a function of the rate of change of freewheeling diode current (dI_{FD}/dt) during diode turn-off.

Figure 12 : Turn-on Ilustrations of the MOSFET Drain to Source Voltage (V_{DS}) and Current (I_D) at Turn-on of the Transistor Limited to 100A/µs.

a) Classical MOSFET
(500V, 0.6 ohm)
BUZ353
Diode losses = 540µJ
MOSFET losses = 3200µJ

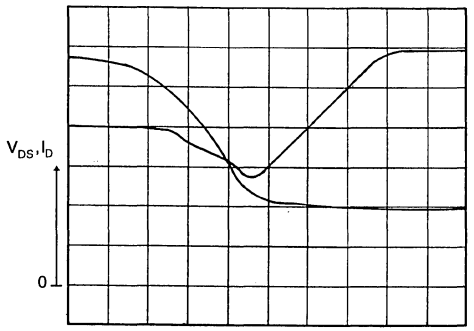
V_{DS} MOSFET drain to source voltage
100V/DIV
I_D Drain current
5A/DIV
Time 200ns/DIV



b) Lifetime controlled MOSFET
(500V, 0.6 ohm)

Diode losses = 460µJ
MOSFET losses = 1600µJ

V_{DS} 100V/DIV
I_D 5A/DIV
Time 100ns/DIV



c) External fast diode
BYT12P-600

Diode losses = 130µJ
MOSFET losses = 560µJ

V_{DS} 100V/DIV
I_D 5A/DIV
Time 50ns/DIV

It can be seen that due to the slow intrinsic diode of the classical MOSFET, turn-on losses are twice that with a lifetime controlled MOSFET. With external fast freewheeling diodes losses are only 20% of the losses in the classical MOSFET.

CONCLUSION

Reverse recovery of the intrinsic MOSFET diode has been investigated. Losses caused by slow intrinsic diode recovery for the classical MOSFET have been compared with losses using lifetime controlled MOSFETs in a bridge-leg and losses using fast external freewheeling diodes. It has been shown that turn-on losses in a bridge-leg using classical MOSFETs are five times greater than losses in bridge-legs with fast external freewheeling diodes and two times greater than losses in bridge-legs using lifetime controlled MOSFETs.

By using different types of inductors (such as saturable inductors) in bridge-legs it has been shown that negligible turn-on losses can be achieved as reverse recovery of the intrinsic MOSFET diode can be limited. Practical results confirm that by using saturable inductors astutely in bridge-legs, it is possible to use the intrinsic diode of the classical MOSFET in high frequency inductive load switching applications with negligible turn-on losses.

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"Power MOS Devices", 1st Edition, October 1985.

2 J.T. DAVIES - P. WALKER - K.I. NUTTALL

"Optimisation of VDMOS power transistors for minimum on-state resistance", IEE Proceeding, vol. 134, PT.1, No. 3, June 1987.

ENVIRONMENT DESIGN RULES OF MOSFET IN MEDIUM POWER APPLICATION

BY B. MAURICE

ABSTRACT

The use of POWER MOSFET allows high switching speed in power applications above 10kW. Nevertheless the main limitations come from the characteristics of the circuit design. From a practical example, this paper analyses and proposes solutions to adapt the POWER MOSFET and the layout in order to minimize parasistic inductances. Special emphasis is given to the driver circuit, package, wiring rules and voltage spike protection at turn-off.

I - INTRODUCTION

POWER MOSFETs are now considered standard tools by circuit designers working at tens of Amps and hundreds of Volts. Their traditional advantages (easy drive and over current capability) remain true when switching over 10KWatts. Nevertheless, the main limitations encountered are not from the MOSFET itself as it can switch high current at high speed (over 1000Amps/sec), but from characteristics of the circuit design. After presentation of a specific example of Power MOS drive, the optimisation of the power devices and the layout will be analysed in the practical example of a chopper operating with ISOFET (1000V - 0.7Ω or 100V - 0.014Ω). Finally, an over-voltage protection circuit is presented.

II - HIGH POWER MOS DRIVE

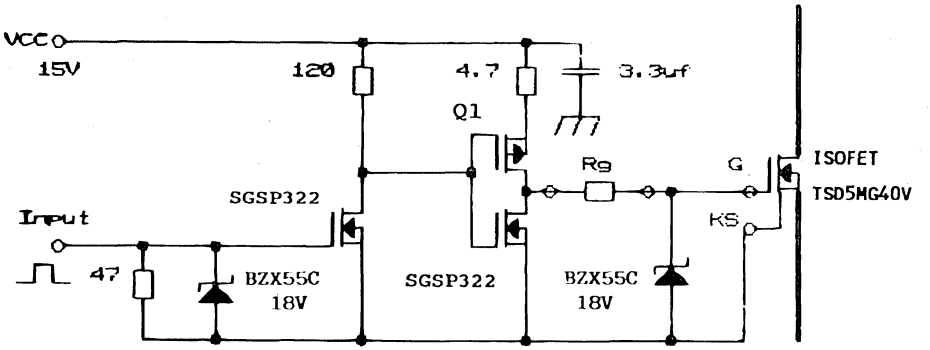
Even with high power switching (over 10KW), the driver circuit can be very simple (fig. 1), comparable to the ones used for low power circuits.

The major characteristics of a POWER MOSFET is its high input capacitance (ie : $C_{iss} \approx 12nF$ for 100V - 14mΩ MOSFET) which must be rapidly charged and discharged when switching without creating oscillations.

The following rules have been used for the design of the driver :

- A low dynamic internal impedance which permits peak current greater than 1Amp for 300nanosec to charge and discharge the ISOFET input capacitance.
- A low impedance circuit reduces the sensitivity to dV_{DS}/dt at turn-off of the ISOFET.
- The total resistance of the gate circuit must be greater than 5Ω in order to sufficiently damp the circuit preventing oscillations and possible parasitic turn-on of the ISOFET.

Figure 1 : Driving Circuit for ISOFET Over 10kW Switching.



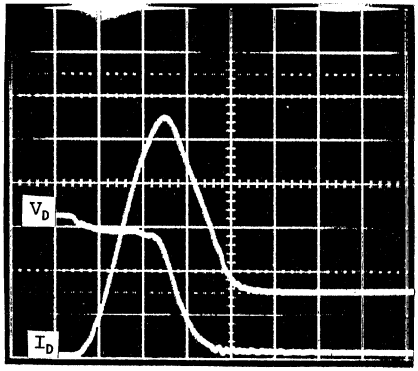
Q_i = 100V 0.4Ω P-channel MOSFET

- The links between drive and gate, short and non-inductive, are made between the gate pin and the "Kelvin Source" pin. The use of the "Kelvin Source" pin is very important when driving Power MOS. It avoids parasitic effects caused by dI/dt in the source lead.
- The gate protection Zener diode has to be mounted close to the ISOFET package.

Figure 2 : Over Current Capability and Switching Speed with ISOFET TSD5MG40 (1000V – 0.7Ω – I_D = 13A).

a. Turn-on ; the ISOFET controls 30A-650V and sustains 110A peak (8 x I_D). The over current is due to the recovery of the free-wheeling diode (BYT230PIV 1000).

b. Turn-off ; with dI/dt = 1600A/usec ; and dV/dt = 15000V/usec. The switched power = 25kW ; and the switching losses = 1.3mj



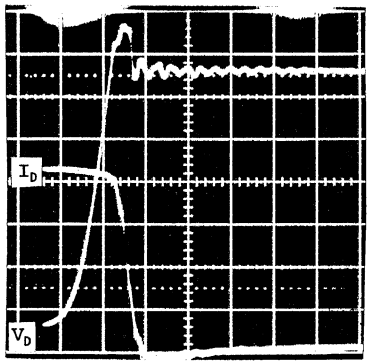
a. Turn-on

VD = 200V/div

ID = 20A/div

t = 50ns/div.

Rg = 5Ω



b. Turn-off

VD = 100V/div

ID = 10A/div

III - LAYOUT DESIGN FOR HIGH SPEED SWITCHING

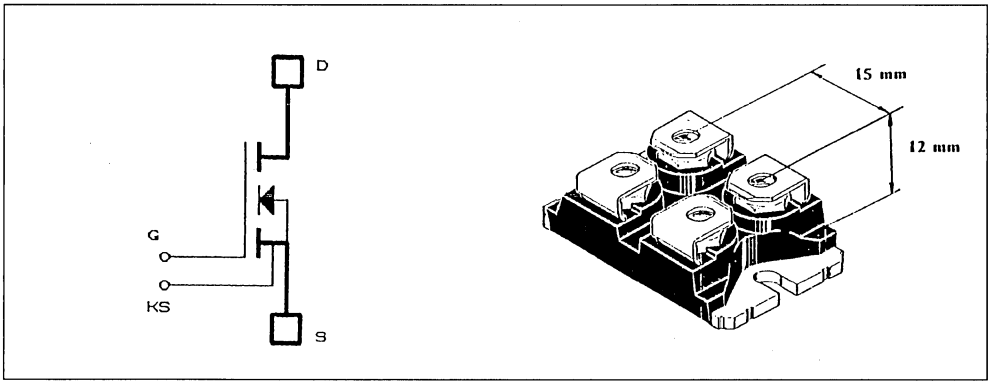
The reduction of the parasitic inductances is a major challenge for power switching especially with a power MOSFET switching over 1000Amps/usec (figure 2). With this switching leading edge, a 10cm diameter wiring loop causes a 100V voltage overshoot. To solve this potential problems two actions are necessary : choosing a well adapted device and optimise the layout design.

a. Adapting the device to the layout

ISOFET is a MOSFET housed in an ISOTOP package (figure 3) :

- The ISOTOP package can be directly screwed on the printboard because all of its terminals are at the same level. Therefore, all inductances due to the length of external wiring connexions, are eliminated.
- As a result of a low profile package (12mm), the internal parasitic inductance is less than 10nH. Moreover, its Kelvin source (KS) enables the minimisation of disturbances induced by the power circuit in the driver circuit.
- Even though it has a thermal resistance value of only 0.25°C/W, the case is fully internally insulated at 2.5kV_{RMS}. Therefore it can be mounted near to the diode package on a common heatsink in order to obtain a very compact circuit layout.

Figure 3 : An ISOFET is a MOSFET housed in an ISOTOP package, which has a low profile.
It is easily integrated in low inductive layouts.
The "Kelvin Source" lead (KS) separates the gate circuit from the internal inductance of the source connection.

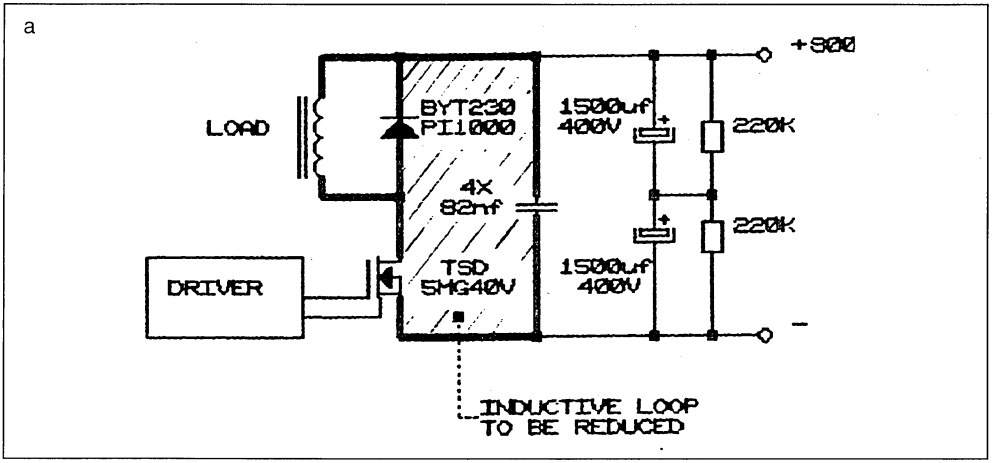


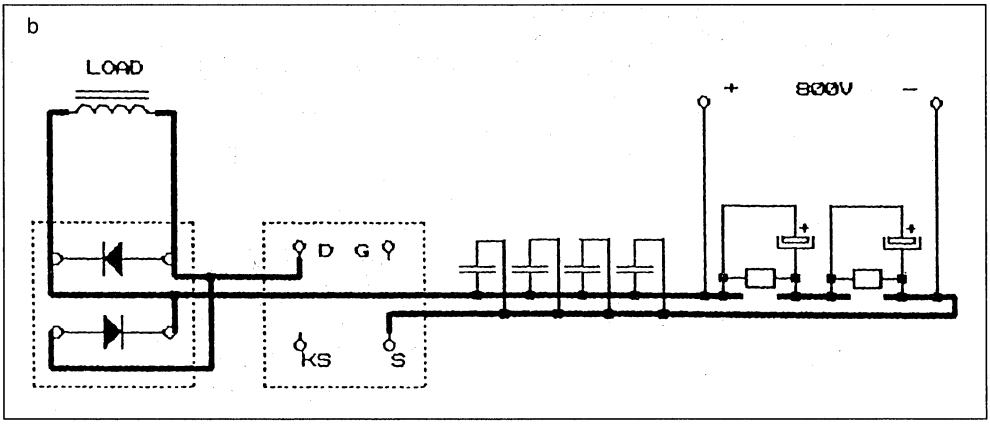
b. Design of the layout

The chopper shown in figure 4 contains two active components : the Power MOS and the freewheeling diode ; both in ISOTOP package screwed side by side, on a common heatsink and directly connected on the printed circuit board (PCB).

Figure 4 : a. Chopper Schematic showing the Inductive Loop to be Reduced.
b. The Same Circuit with two ISOTOP Packages (diode and ISOFET). The packages and links adopt an "in line" configuration in order to reduce the inductive loop.

a





By observation of the facts presented in appendix 1, the design rules used for the layout are summarized :

- Use of double sided PCB where each high current path is immediately above its returns path on the other side of the board.
- The current densigy has been reduced by enlarging the copper tracks in order to decrease the local dI/dt and consequently the resulting induced voltage.
- Use of several links instead of one, between two large copper tracks, avoids high current concentrations and reduces the inductance (figure 5).
- Decoupling capacitors have been configured in the same direction as the direction of current flow. This prevents the formation of an inductive loop. (compare figure 6a and figure 6b hatched surfaces).
- The use of several smaller capacitors in parallel permits reduction of the equivalent internal parasitic inductance. (figure 6c).
- Choose components (e.g. capacitors) specified with a low internal inductance. (electrolytical capacitor 700µF/400V can have a parasitic inductance of several tens of nH). Prefer the capacitor packages which minimize the inductive connection length.

Figure 5 : Junction between two wide copper tracks is less inductive when several spaced links are used rather then a single link.

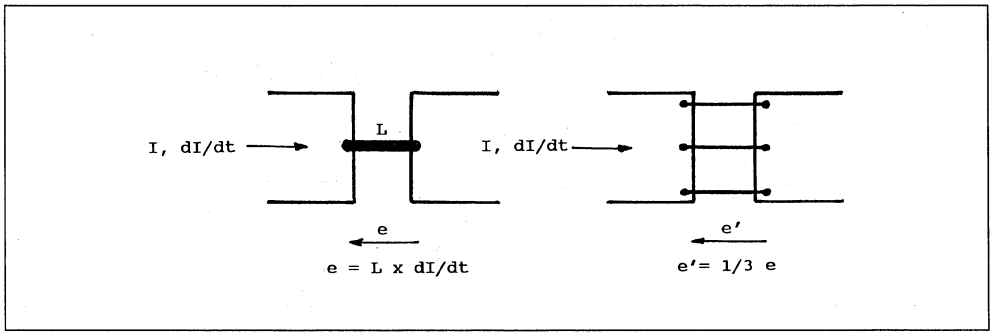
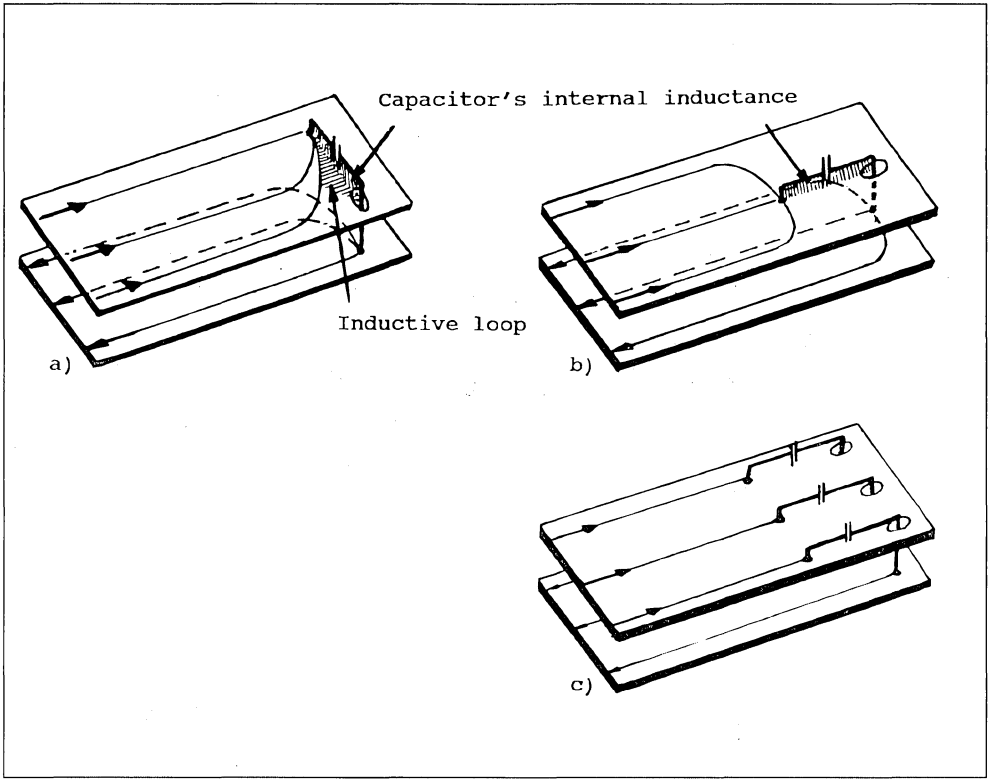


Figure 6 : Configuration of Decoupling Capacitors :

a. An inductive loop is formed, perpendicular to the current flow, because the current flow is not super imposed near the capacitor,

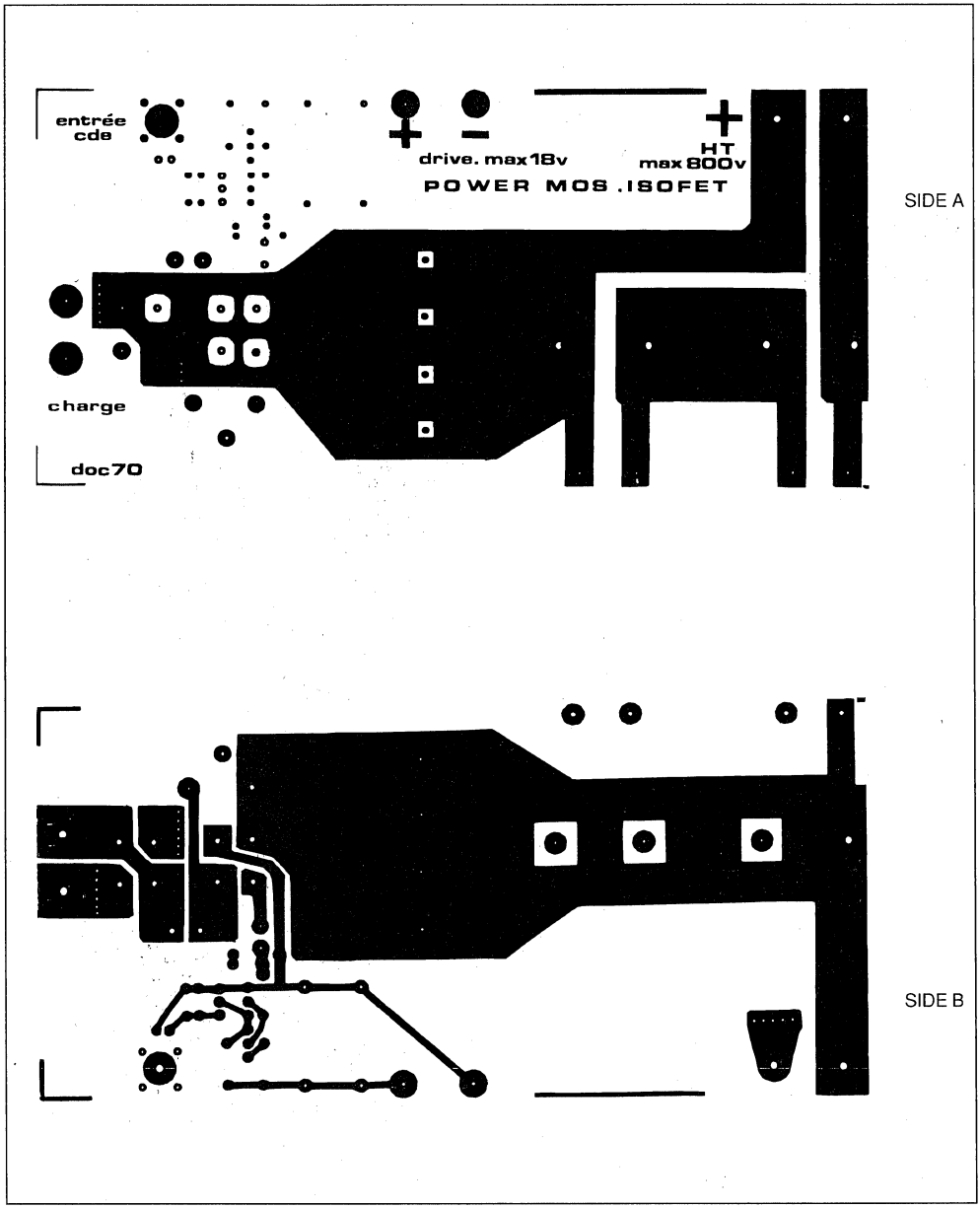
b. Capacitor lying in the same direction as the direction of current flow. inductive loop minimised.

c. Several smaller capacitors in parallel reduce their equivalent internal parasitic inductance for the optimum solution.



As a result the residual inductance of the finished layout (fig. 7) has been measured as 35nH, (fig. 8) plus 15nH when a current sensing loop (15mm^2) is added to the layout.

Figure 7 : A Double Side Very Low Inductive Print Circuit Board. (scale : 0.5)
Note the Multi Links (A) to connect One Side to the Other.



IV - OVERVOLTAGE DURING TURN OFF

We have previously seen that by following these sound rules a parasitic inductance value of 35nH can be achieved. It represents the sum of several small components : active components, passive components and PCB. It seems difficult to reduce it further in a circuit without paralleling several power switches.

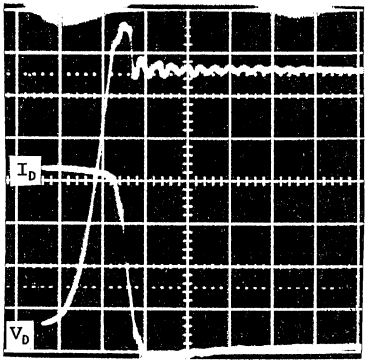
In view of the ISOFET fast switching speed at turn-off (1000Amp/usec), the inductive voltage spike with 35nH will be 35 Volts. This overvoltage is acceptable for devices rated over 500V. It is not negligeable in low voltage applications such as battery powered equipment.

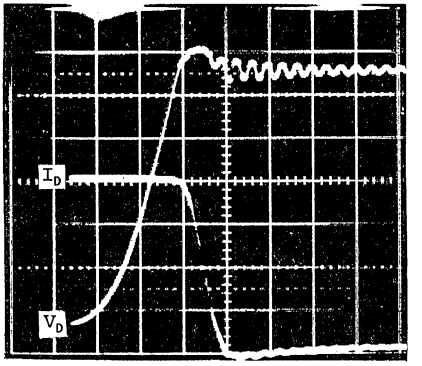
Two solutions are possible :

a. Slowing down the ISOFET

The switching speed at turn-off can be slowed down by increasing the gate resistor value. This method increases the commutating time and consequently the switching losses. These losses are increased by 50% when R_g increases fro 5 to 10Ω. (figure 8).

Figure 8 : Increased Gate Resistor reduces dI/dt and Overvoltage at Turn-off. (driver circuit fig. 1). The total parasitic inductive loop (50nH) includes the inductance of the sense current loop.
I_D = 10A/div V_D = 100V/div t = 50ns/div (ISOFET TSD5MG40V 1000V – 0.7Ω)
Switched power = 25kW ; Switching losses = 1.3mJ in (a) and 2.0mJ in (b).





b. Protection against over-voltage at turn-off

Use of a MOSFET with a low margin for the rating voltage ($V_{BR(DSS)}$) can be achieved by using active protection (i.e. Transil) in order to clamp the voltage spikes.

One solution is to connect a Transil acros the drain-source leads. In this case, the energy is dissipated in the Transil which has to be cooled in order to dissipate the average power.

(1/2 LI^2f = 20W with 40nH, 100A, 100kHz)

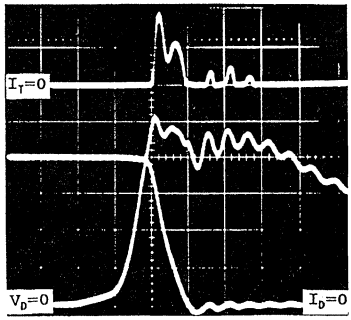
We have chosen another solution by connecting the Transil across the drain-gate leads (figure 9). When the over voltage transient reaches the clamping voltage, the clamping current goes through the gate resistance and biases gate above 5V. (ex : 1A into 5Ω).

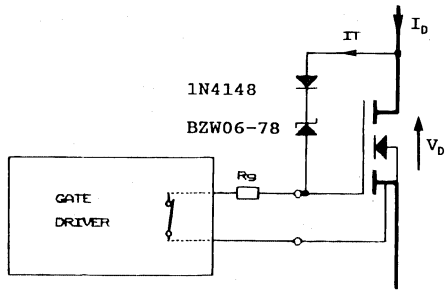
This way, the clamping power is dissipated in the MOSFET and a smaller Transil is required (P ≈ 1W at 100kHz in our case).

As the Transil does not heat up, the clamping voltage does not vary with temperature. The equivalent dynamic resistance is very low because the serial resistance of the Transil is divided by R_g and by the MOSFET transconductance.

The current though the Transil being low, the voltage to be considered for its choice is the breakdown voltage at test level (V_{BR} at I_R) instead of the surge clamping voltage (V_{CL}). The Transil breakdown voltage should be chosen to be lower than the maximum desired clamping voltage less 5 Volts to take into account the MOSFET gate threshold voltage.

Figure 9 : Over Voltage clamping by a Transil across the Drain-gate Leads durring turn-off. (ISOFET TSD4M150V 100V – 14mΩ). Upper Trace shows the Current in the Transil (IT). I_D = 20A/div, V_D = 20V/div, I_T = 1A/div, t = 100ns/div.





V - CONCLUSION

MOSFETs switching power over 10kW have the same basic advantages as lower power Mosfet. The driving circuit remains very simple and the over current capability is huge. A specific emphasis has been placed on the minimization of circuit layout inductance. Because of the very fast switching (easily over 1000A/s) it is advantageous to use :

- packages like ISOFET which minimise their internal inductance and allow easy connection to printed circuit board and to heatsink. Also Kelvin Source contact to minimise drive circuit interference.
- double side printed circuit board with symmetrical copper tracks, reduced current concentration, and components positioned in order to minimise parasitic inductance.
- overvoltage protection which avoids oversizing the voltage rating of MOSFETs in low voltage applications.

BIBLIOGRAPHY

[1] An Innovative High Frequency High Current Transistor Chopper. L. PERIER ; E.P.E. Bruxelles 1985.

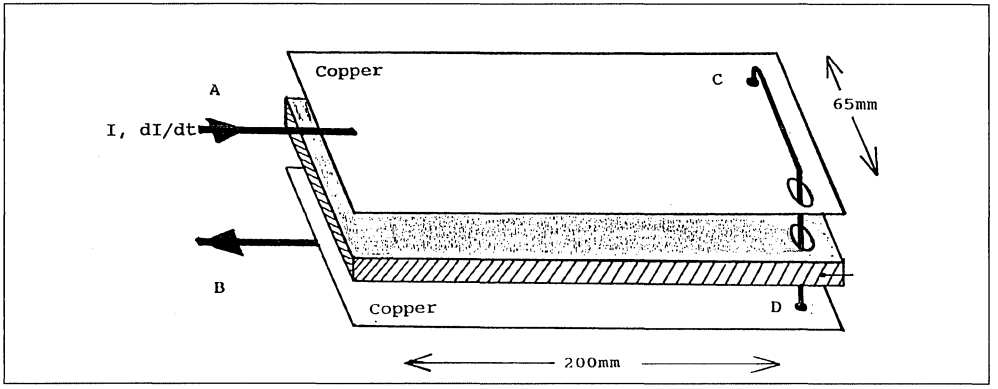
[2] POWER MOS DEVICES Data Book 1st edition June 1988 SGS-THOMSON Microelectronics.

APPENDIX 1

MEASUREMENT OF PARASITIC INDUCTANCES ON A DOUBLE SIDED PCB

- In the figure below, the link between points C and D simulates the connection of a capacitor with nop internal inductance, connected on double sided Printed Circuit Board.

Figure 10.

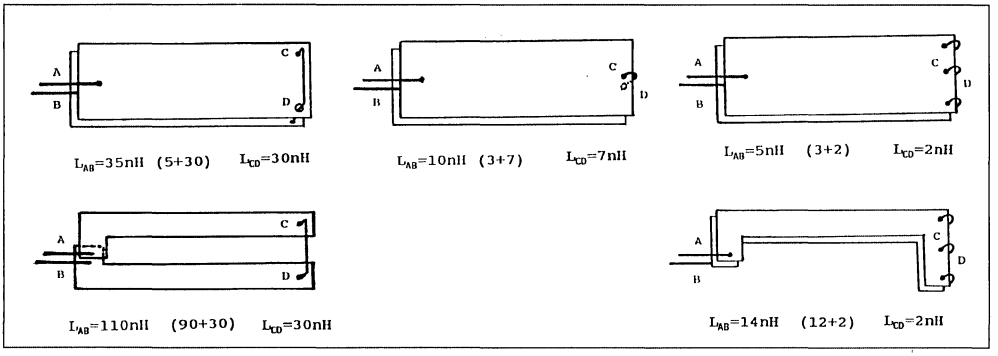


- The measurements are made with a dI/dt generator :
- I = 0 to 40Amps with a dI/dt = 1000A/s

The measurement of the induction voltage VL between A to B, and C to D, permits calculation of L = V_L / (dI/dt)

MEASUREMENT RESULTS

Figure 11.



MEASUREMENT CONCLUSIONS

- Capacitors should be positioned in the same direction as direction of current flow.
  Compare : a. to b.
- Several links between two large copper tracks are less inductive than a single link.
  Compare : b. to c.
- Every current path should be exactly above its return path on the other side of the board.
  Compare : d. to e.
- Decrease local dI/dt density by enlarging copper tracks.
  Compare : c. to e.

COMPACT HIGH PERFORMANCE BRUSH D.C. MOTOR SERVO DRIVES USING MOSFETS

By C.K. PATNI

ABSTRACT

For medium power (200VA to 6kVA) brush D.C. motor servo drives, MOS field effect transistors (MOSFET) are ideally suited. A compact high performance (20 to 50kHz) 1.2kVA brush D.C. motor velocity servo drive, which has been developed and tested, is presented. SGSP477 and BYW8PI200 high efficiency fast recovery epitaxial diode (FRED) are used in the 1.2kVA power stage. A 6kVA motor drive design using ISOFETs is also presented.

TSD4M250 (ISOFET) and BYV54V200 FRED diodes are utilized in the 6kVA design in which FREDs are used as the MOSFET series blocking diode and the freewheel diode. Different power H-bridge configurations are chosen and justified for the 1.2 and 6kVA drives. Particular emphasis is placed on short-circuit protection techniques and simple gate drives.

INTRODUCTION

Brush D.C. permanent magnet motors are extensively used as velocity servo drives for high performance applications such as robotics and machine-tools. The high voltage D.C. (HVDC) supply of the power stage for such motors rated up to 6kVA is generally limited to 200V D.C. because of sparking of the commutator and brush assembly.

The commutator has a maximum volts per segment rating at rated power above which there is excessive brush wear. MOSFETs are well adapted for medium power applications at voltages up to 500V. Consequently the ease of paralleling, high peak current capability and the ease with which MOSFETs can be controlled and protected make them ideal power semiconductor switching devices for such motor drives. Medium power brush D.C. motor voltage limitation of 200V D. C. enables fast recovery epitaxial diodes (FRED) to be used which have high efficiency due to very low conduction losses and negligible switching losses :

BYW81PI-200 : FRED :

$V_f < 0.85V$ ($I_F = 12A$; $T_j = 100°C$)

$t_{rr} < 35ns$

Block diagram schemes for brush D.C. permanent magnet velocity servo drives are discussed. Servo drive specifications shown in table 1 are considered and solutions for the 1.2kVA and 6kVA motor drives are presented. The 1.2kVA motor drive is developed and tested. Protection, efficiency and switching frequency requirements have strongly influenced the designs.

Other than the power ratings, the parameters listed in the specification are common for many high performance servo drives. The main component in the design of the hardware is the power H-bridge switching ideally above the audio-frequency range. High frequency switching permits a compact power output filter to be used to filter the switching frequency if so desired.

SWITCH-MODE MOTOR DRIVE CONCEPTS

Figure 1 illustrates a conventional pulse width moldulated (PWM) D.C. motor servo drive. The velocity demand and the tachogenerator feedback signals are compared and the resultant velocity error is amplified. This error is fed to the current servo amplifier where it is compared with the actual current flowing in the motor armature. The amplified current error is fed into a linear PWM generator. The control of the mark to space ratio of the PWM generator is achieved by comparing the input error signal with a constant frequency triangular waveform. This results in a fixed frequency PWM signal which is fed to the power stage.

A switch-mode drive designed to the specification in table 1 comprises of :

1/ Drive and protection for power devices
2/ Power supplies
3/ Regenerative energy clamp (4 quadrant control)
4/ Current loop
5/ Control and logic for PWM and velocity servo.

The block diagram of the drive which has been developed is outlined in figure 2. (The complete circuit diagram is provided in figure 14). The differences between the two schemes outlined in figures 1 and 2 are that the current control loop and the PWM integrated circuit are eliminated in the second scheme. In the second scheme the velocity error is fed directly into a velocity compensation and modulation circuit. The elimination of the current feedback loop limits this scheme in so much as it can not be used in torque control applications.

Table 1 : Typical Brush D.C. Servo Drive Specification.

Specification	1.2kVA	6.0kVA
Modulation Frequency	> 20kHz < 50kHz	
Continuous Power	1300VA	6000VA
Maximum Continuous Current	10A	50A
Bus Voltage Input	$120V_{DC}$	
Efficiency	> 90%	
Short to Ground	Shut down	
Short to Bus Voltage	Shut down	
Armature Short	Shut down	
Operating Temperature	0 to 50°C	
Velocity Demand	10V	
Regenerative Energy Dissipation	10% of Continuous Rating	

Figure 1 : PWM D.C. Servo Drive.

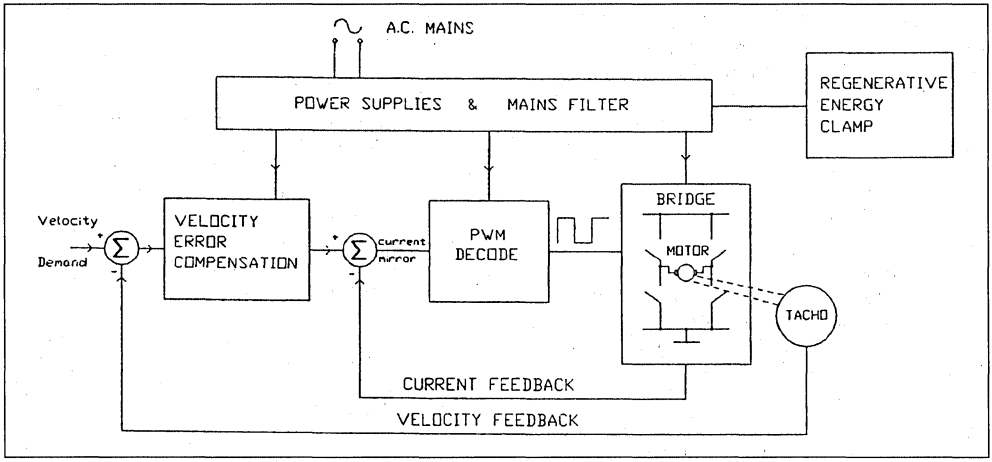
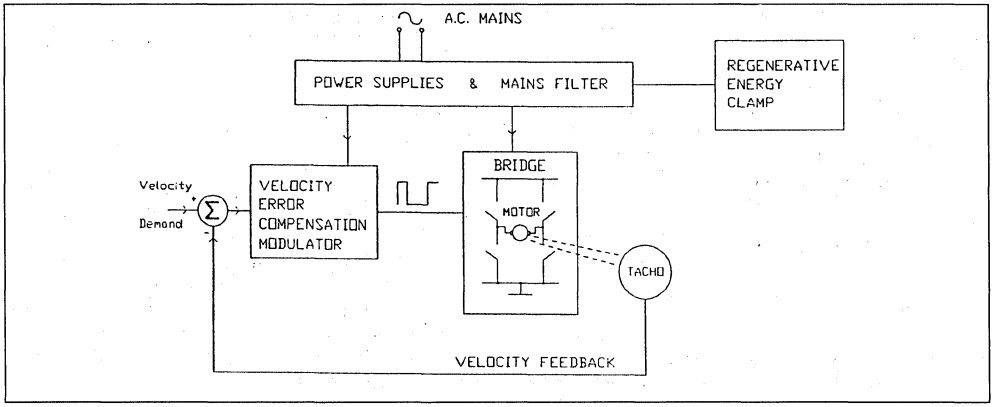


Figure 2 : Schematic Diagram of Brush D.C.P.M. Motor Drive.



BRIDGE CONFIGURATIONS & MODULATION TECHNIQUES

The bridge design must be capable of supplying bi-directional current to the motor for optimal four quadrant control. This can be achieved by using a "T-bridge" or an "H-bridge", as shown in figure 3. The H-bridge is generally chosen since it requires a single power supply. The voltage rating of the power semiconductor devices matches the motor voltage rating for the H-bridge alternative.

The H-bridge has eight operating modes when connected to a D.C. motor load. These modes can be seen in figure 4. Two of the modes increase current supplied to the motor winding in either direction. The other six operating modes reduce current in the motor winding and are commonly known as free-wheeling modes. Numerous switching modes are possible for PWM and current control. For example, it is possible to PWM both the top and bottom devices in the bridge or simply either the top or bottom device. It is possible to use the PWM mark to space ratio such that the mark provides a positive rate of change of current in the motor winding and the space provides a negative rate of change of current. The control of the pulse width thus establishes an adjustable average voltage across the motor load.

A modulation technique used in the developed servo drive is illustrated in figure 5. This modulator is based on "delta modulation" (reference 1). The mark to space ratio of the modulator output (0(t)), determines the conduction period of the MOSFETs in the H-bridge. The modulator comprises of the standard delta modulator (part A), the proportional term (part B) and the integral term (part C) of the PID controller.

Figure 3 : Bridge Configurations.

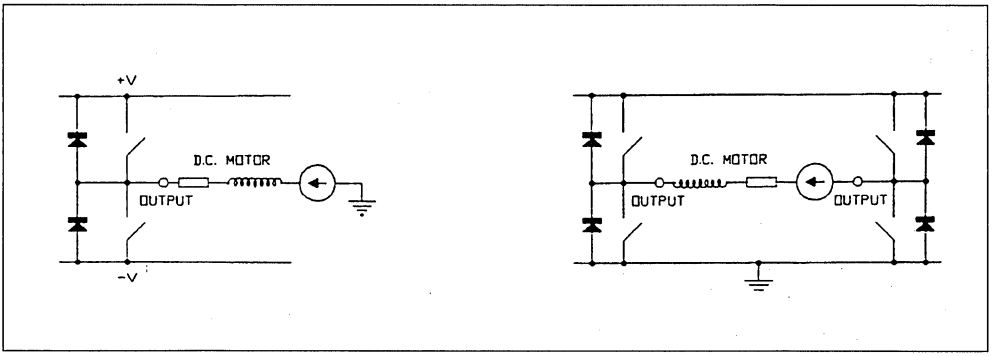


Figure 4 : Operating Modes of the H-bridge Showing Current Flow Paths.

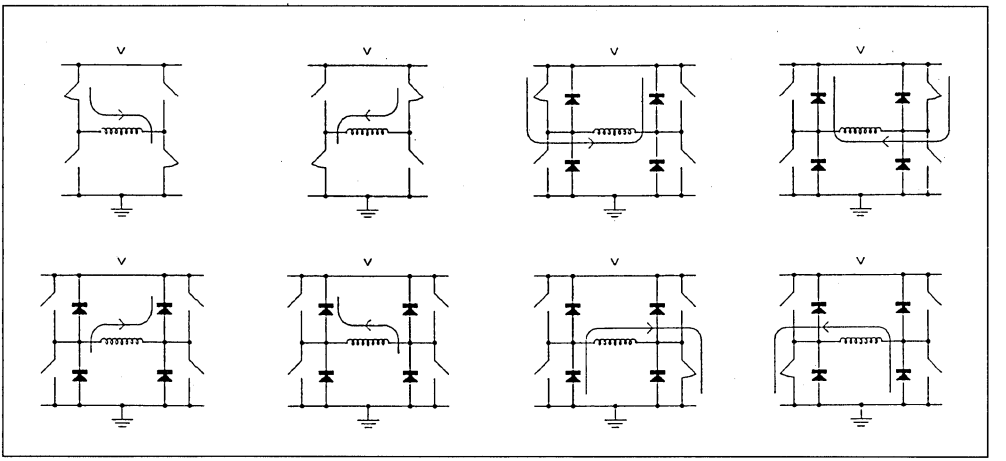
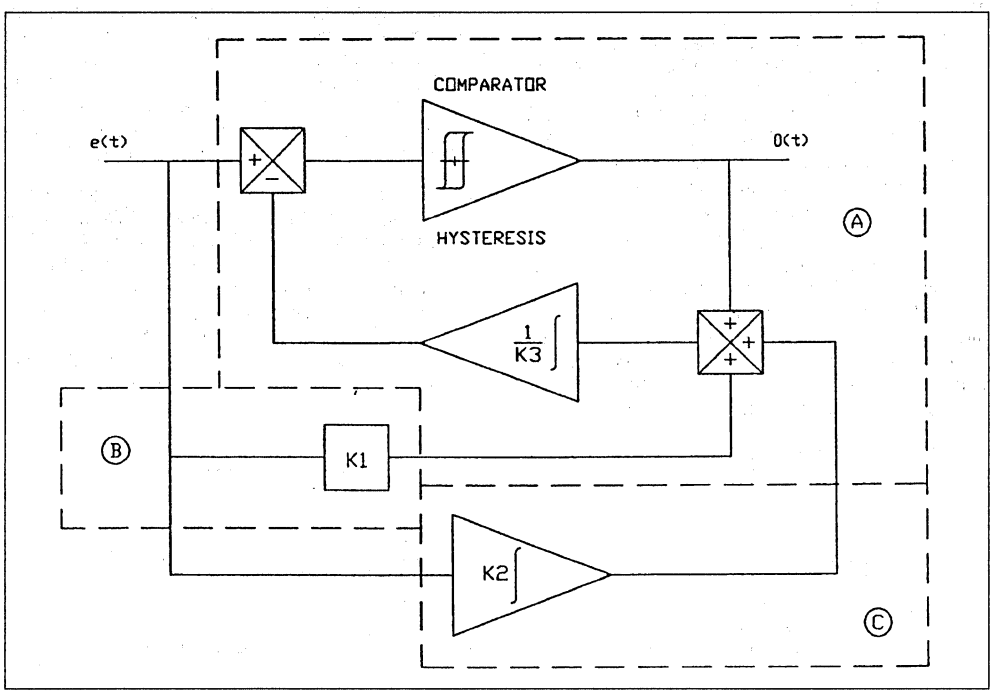


Figure 5 : A PID Controller with Binary Output.



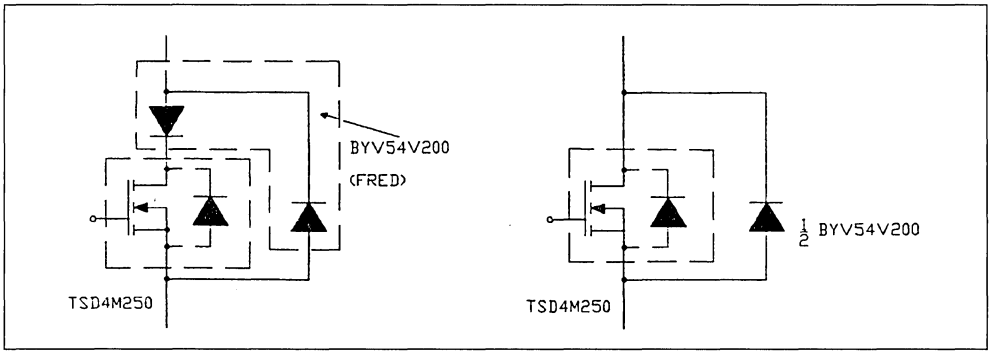
SWITCHING DEVICES FOR A RANGE OF D.C. MOTOR SERVO DRIVES

At medium power levels the MOSFET is ideally suited offering high switching speed, ease of paralleling and simple gate drive and protection. SGS-Thomson has introduced a range of MOSFET devices in plastic isolated packages. The 200V devices, summarised in table 2, can be used to design a servo drive range from 600VA to 6kVA without the need to parallel MOSFETs in separate plastic packages.

The MOSFET internal parasitic diode is too slow for applications requiring ultrasonic switching frequencies. Excessive switching losses in the MOSFET can result from the reverse recovery time of the internal parasitic diode (greater than 600ns). Noise is also induced on the supply rails when the conducting diodes reverse recover. Table 2 specifies high efficiency ultra fast recovery epitaxial diodes for freewheeling. These diodes, having a conduction voltage of less than 0.85V at rated nominal current, are ideally suited as MOSFET series blocking diodes used to prevent the conduction of the internal parasitic diode.

Figure 6 illustrates possible techniques for utilizing fast external diodes for the 6kVA brush D.C. motor design.

Figure 6 : 6kVA MOSFET Switch Configurations Using ISOFETs and FREDs.



Manufacture : SGS - THOMSON MICROELECTRONICS							Basic Brush D. C. Motor Drive Spec. Switching Freq. > 20kHz		
Part N° MOSFET	$R_{DS(ON)}$ T_j = 25°C (Ω)	I_D T_c = 100°C (A)	R_{TH} (°C/W)	Part N° Diode FRED	V_F at T_j = 100°C (V)	I_F (A)	POWER (VA)	V_{nom} (V)	I_{nom} (A)
SGSP367[1]	0.45	10	1	BYW80PI200	0.85	7	600	120	5
SGSP477[1]	0.17	20	0.83	BYW81PI200	0.85	12	1200	120	10
TSD4M250[2]	0.021	68	0.25	BYV54V200	0.85	50	6000	120	50

Table 2 A range of brush D. C. motor velocity servo drives.

1 - without insulation.

2 - ISOFET : MOSFET chips in parallel in ISOTOP package.

1.2.KVA BRUSH D.C. SERVO DRIVE

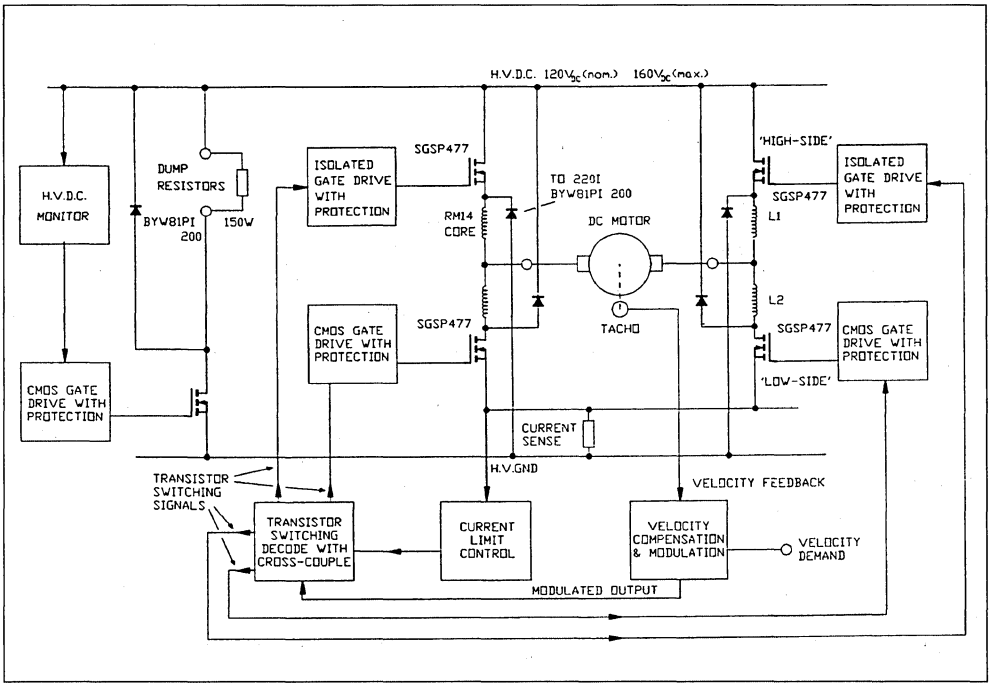
Figure 7 illustrates the block diagram of the developed 1.2kVA brush D.C. servo drive. The H-bridge operates at a nominal voltage of 120V_{DC}. The D.C. motor in certain applications is driven by its load and hence is a generator of energy. This regenerative energy causes the HVDC rail voltage to increase as energy is stored in the smoothing capacitors.

At a maximum voltage of 160V_{DC}, a resistive dump is turned-on to dissipate the regenerative energy and thus limit the HVDC to 160V_{DC}. The drive utilizes the velocity PID controller illustrated previously in figure 5. A current sense resistor is incorporated in the H-bridge to provide load current feedback necessary to limit this load current to the maximum continuous current rating of the drive.

MOSFET based bridge-leg configurations have previously been discussed (reference 2). The bridge-leg utilized comprises of "low-side" and "high-side" switches connected in series across the HVDC. In this asymetrical bridge-leg, (illustrated in figure 7), the rate of change of short-circuit current is limited by inductors (L1 and L2 : RM14 cores) which also limit freewheeling current from going through the parasitic diodes of the MOSFETs. At the 10A maximum continuous current rating of the drive, these inductors are still a managable size. This bridge-leg configuration is capable of withstanding simultaneous conduction of the two devices in the bridge-leg since there are series inductors which reduce the rate of change of drain current. This provides sufficient time for the short-circuit detection loop to operate. The power devices are thus turned-off without being stressed with high rates of change of pulse currents.

At a maximum continuous current rating of 10A, SGSP477 MOSFETs and BY81PI200 fast freewheel diodes plastic packages are optimally rated for the 1.2kVA power stage.

Figure 7 : 1.2 Brush D.C. Motor Velocity Servo Drive (120V_{DC} ; 10A : nom.).

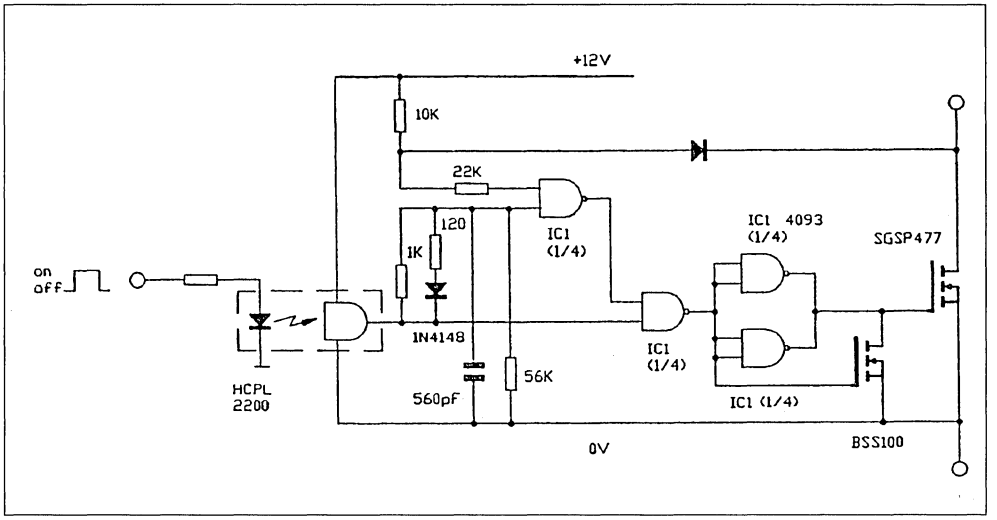


GATE DRIVES AND PROTECTION

Similar gate drives and protection circuits, (illustrated in figure 8), have been used for the "high-side" and "low-side" switches. This CMOS gate drive is well suited as switching speeds of 100 to 250 nanoseconds are sufficient in motor drive applications requiring a switching frequency of around 20 to 30kHz. Monitoring of the drain to source voltage while the device is conducting permits the detection of short-circuit conditions which lead to device failure. The device is turned-off before the drain current reaches a value in excess of the peak pulse current capability of the MOSFET. When the MOSFET is turned-on the on-state voltage of the device ($V_{DS(on)}$) is compared with a fixed reference voltage of approximately 8V. At the turn-on instant, $V_{DS(on)}$ monitoring is inhibited for a period of approximately 400 nanoseconds in order to allow the MOSFET to turn-on fully. After this period, if $V_{DS(on)}$ is detected to be greater than the fixed reference voltage, the device is latched-off until the control signal is turned-off and turned-on again.

The "high-side" gate drives have isolated low voltage supplies and isolated command signals using high speed opto-couplers.

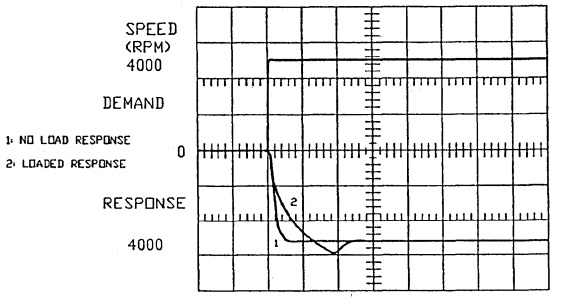
Figure 8 : An Isolated CMOS Gate Drive with Protection.



MOTOR DRIVE PERFORMANCE

Figure 9 illustrates the dynamic response of the motor drive to a step demand of 4000rpm. The response has been optimised for the no-load case (trace 1). Under heavy load inertia there is an overshoot in the velocity response (trace 2). The effects of changing the proportional gain and the integrator time constant of the PID controller can be seen in figures 10 and 11.

Figure 9 : Velocity Response of Motor Drive.



Time scale : 0.5s/div

Figure 10 : The Effect Upon the Dynamic Response of the Analogue Velocity Servo System, When the Gain of the Proportional Term in the PID Controller is Varied.

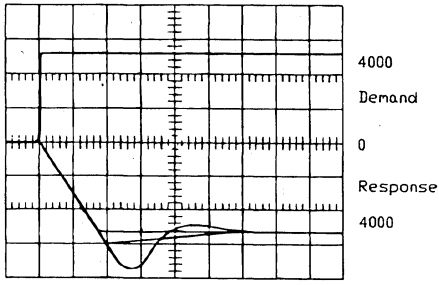
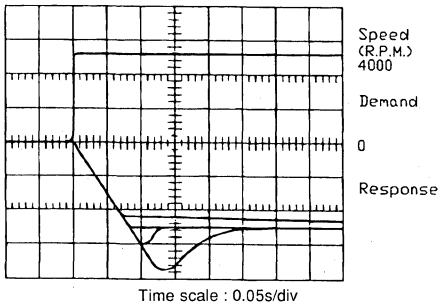


Figure 11 : The Effect Upon the Dynamic Response of the Analogue Velocity Servo System, when the Time Constant of the Integrator in the PID Controller is Varied.



6KVA BRUSH D.C. MOTOR SERVO DRIVE

Figure 12 illustrates the block diagram of the proposed 6kVA ($120V_{DC}$; 50A) motor drive using ISOTOP packages for the MOSFETs in parallel (ISOFET) and the FRED diodes.

Blocking diodes in series with the MOSFETs are proposed to prevent the MOSFET internal parasitic diodes from conducting. The asymetrical bridge-leg configuration is not a cost-effective solution since inductors rated for 50A continuous operation are large and expensive. The series blocking diode has to be an ultra fast high voltage type. If the transistor F2 (shown in figure 12) is conducting, the drain to source capacitance of the transistor F1 is charged to the HVDC voltage. If F2 is turned-off, the load current transfers from F2 to the free-wheel diode, D1. Consequently the series blocking diode, D2, supports the drain to source capacitance voltage of F1 (equal to HVDC) provided this capacitance is not discharged by turning-on F1.

An isolated D.C. current measurement device, (such as an Hall-effect current sensor, LT80-P, manufactured by LEM), is recommended for the measurement of load current necessary for current limit control.

Pulse transformer based floating gate drives illustrated in figure 13 can be used for the TSD4M250 ISOFETs. The pulse transformer is used to transmit simultaneously the ISOFET logic command signal together with the gate to source capacitance charging current. The current mirror technique (reference 2) is used to provide short-circuit and over-load current protection. The pulse transformer operates at an oscillating frequency of 1MHz when a turn-on control signal is present. The secondary is rectified to provide gate source capacitance voltage. The current mirror provides a voltage "image" of the main drain current. This voltage is compared with a fixed reference voltage in order that the gate drive be latched-off whenever the drain current exceeds the specified overload current level.

Figure 12 : 6kVA Brush D.C. Motor Velocity Servo Drive (120V_{DC} ; 50A : nom.).

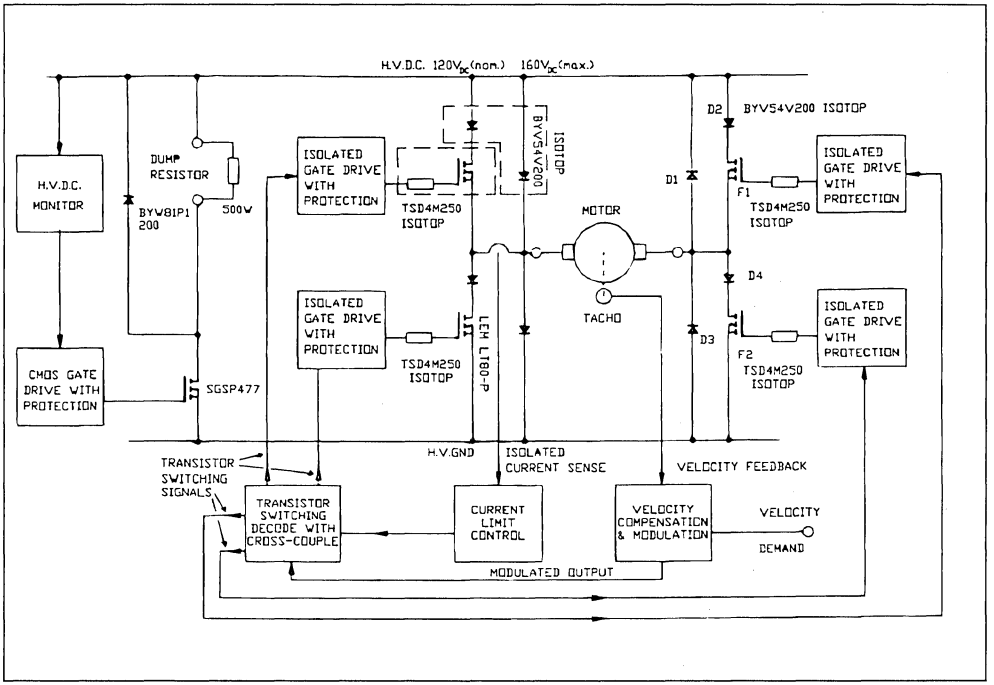
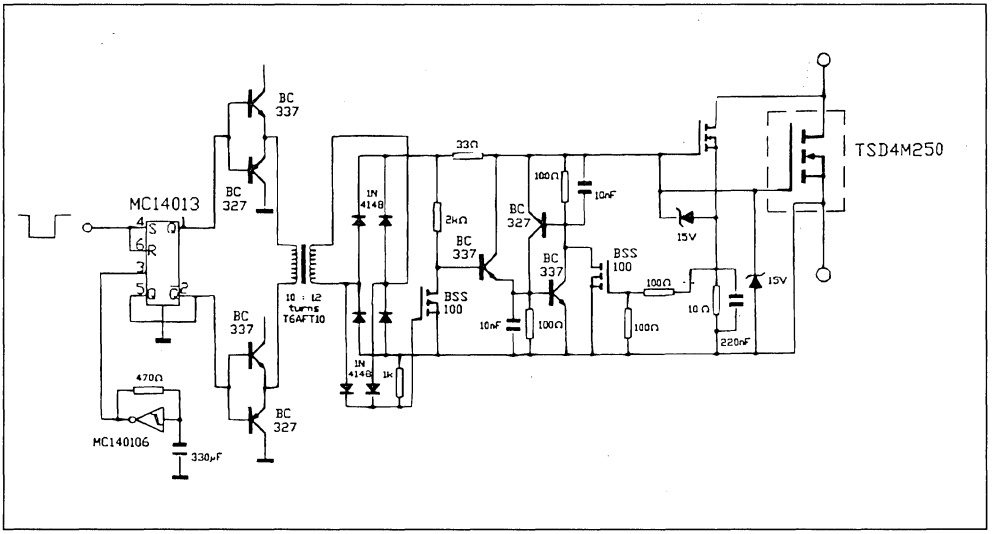


Figure 13 : Pulse Transformer Gate Drive with Current Mirror Protection for a TDS4M250.

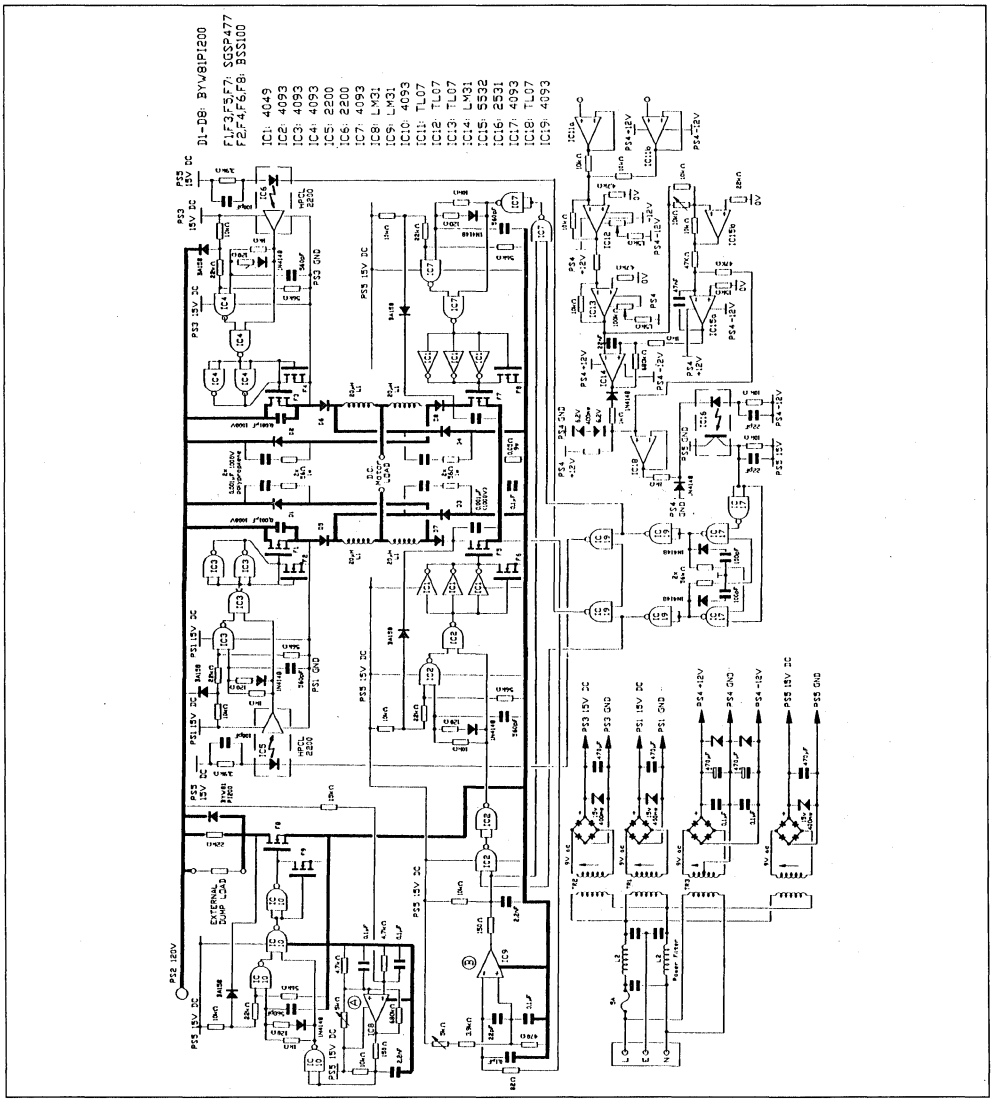


CONCLUSION

MOSFET based brush D.C. motor velocity servo drives have been described, with particular emphasis placed on the bridge-leg configuration, the PID compensation and modulation, the gate drive and protection techniques. The PID compensation and modulation circuits require few components to achieve good velocity servo performance.

The development has led to a compact high performance 1.2kVA drive which is fully protected against output short-circuit conditions. A 6kVA motor drive is proposed using ISOFETs. MOSFET switching devices and their associated free-wheel and blocking diodes have been specified for a range of brush D.C. motor drives rated between 600VA to 6kVA without the need to parallel MOSFETs in separate plastic packages.

Figure 14 : 1.2kVA Switched-mode Motor Drive.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SWITCHING WITH MOSFETs AND IGBTs: 50Hz TO 200kHz

by K.G. Rischmüller

ABSTRACT

The basics of IGBT and Power MOSFET characteristics are discussed and their switching behaviour analysed. Circuits for loss evaluation of MOSFETs and IGBTs are described and evaluation methods for output charge and energy are shown. It is demonstrated that on-resistance and output capacitance are related and how loss minimization can be achieved in different PWM and resonant topologies. Gate drive methods enabling reduced switching loss, better overload behaviour and less driver energy consumption are also shown.

INTRODUCTION

The excellent switching behaviour of Power MOSFETs is an incentive to power supply designers to increase switching frequencies and thus reduce the cost and size of the magnetics. Nevertheless, low frequency switching with controlled current and voltage rise times can also lead to new concepts and cost reduction. When optimising low and high frequency power control circuits, the neglected parasitic effects of Power MOSFETs and their bipolar counterparts, IGBTs, become important and have to be taken into account for circuit - design.

A: UNDERSTANDING POWER MOSFET AND IGBT BEHAVIOUR

Over the last few years, Power MOSFET high voltage capability and on-resistance have been very much improved. The on-resistance per die area is a means by which these improvements can be measured (fig.A1).

On resistance per die area is close to the physical limits for Power MOSFETs having a 600 - 1000V breakdown voltage, thus major improvements in the on-resistance of these devices can be obtained only by increasing the die area.

Bipolar operation is the only way to decrease on-resistance per unit area to below the physical limit dictated by the resistance of the n-body of the MOSFET.

The Insulated Gate Bipolar Transistor (IGBT), the Bipolar Modulated FET (BM-FET) and the Field Controlled Thyristor (FCTh) have bipolar modes of operation.

THE DIFFERENCE BETWEEN POWER MOSFETS AND IGBTS

The IGBT can be understood as a Power MOSFET driving a PNP-transistor (fig.A2). During conduction, the p-layer injects minority carriers into the resistive n-layer, thus significantly reducing the on-resistance of the device (fig.A2).

The higher the breakdown voltage of the device, the higher the difference in on-resistance between a unipolar Power MOSFET and a bipolar IGBT. Fig.A3 shows the output characteristics of 1000V devices having similar die-size.

The reduced on-resistance of IGBTs does not come for free: IGBTs exhibit more turn-off losses than Power MOSFETs (fig.A4) and their protection against overload is more difficult.

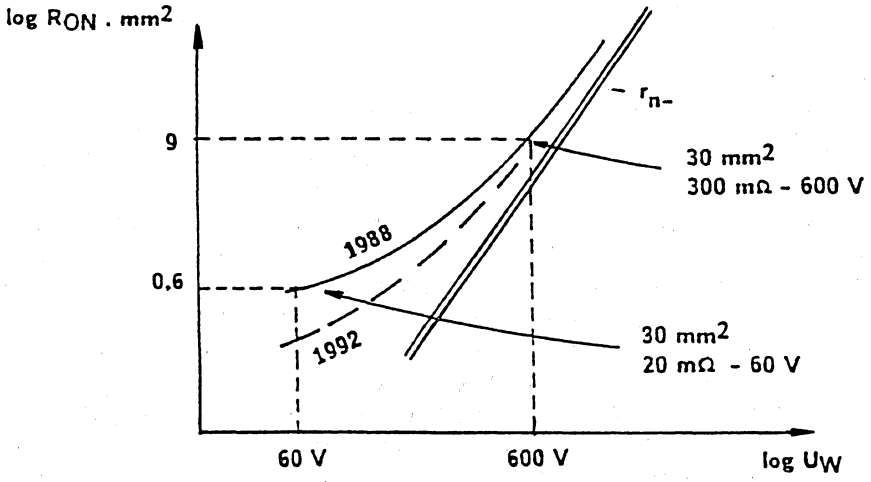


Fig. A1: MOSFET's on-resistance per silicon area versus breakdown voltage. With high voltage devices it is close to bulk-resistance. Low voltage devices have much potential for improvement.

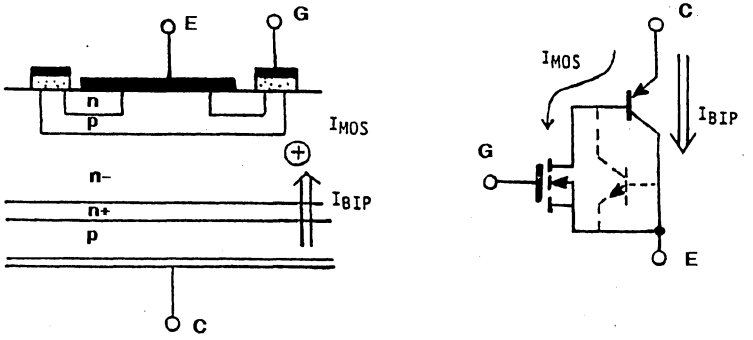


Fig. A2: Cross section and simplified equivalent circuit of an Insulated Gate Bipolar Transistor (IGBT). This device combines low on-resistance with simple drive requirements.

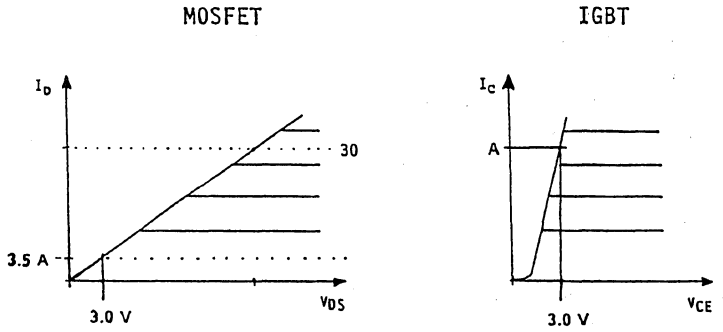


Fig.A3: Output characteristics of a 1000V-MOSFET and an IGBT having similar die-size.

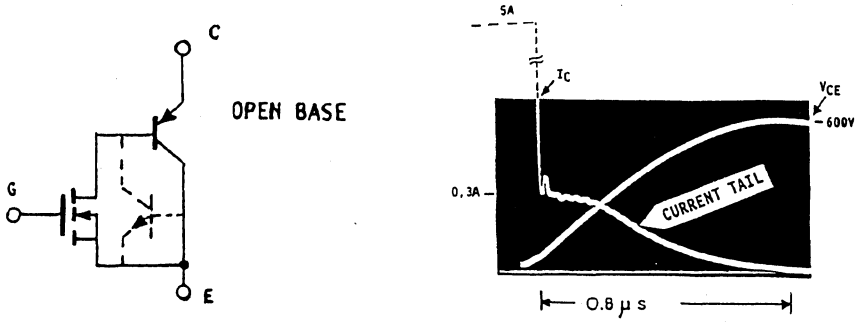


Fig. A4: IGBTs exhibit a turn-off collector current tail and significant turn-off losses in PWM circuits.

HOW TO CONTROL TURN-ON SWITCHING

Turn-on switching when the freewheeling diode is conducting leads to losses in a Power MOSFET and to similar losses in an IGBT (fig.A5). Increasing the di/dt of the drain current, or for an IGBT the collector current, leads to reduced turn-on losses. Reducing di/dt leads to higher losses, but makes the reverse recovery behaviour of the freewheeling diode "softer", thus reducing RFI problems.

When switching a short circuit, drain-source or collector-emitter voltage is at a constant high level while the drain or collector current increases at a certain di/dt (fig.A6). It stabilises at a certain current value, I_{SC} . The amplitude and duration of this current should be minimised in order to minimise energy stress on the semiconductor device. The output characteristics of the Power MOSFET IRFP450 helps us to understand how we can control di/dt and I_{SC} (fig.A7). The time needed to move the gate - source voltage from approximately 2V to about 6V determines the rate of rise (di/dt) of drain-current. The amplitude of a short circuit current, I_{SC} , is controlled through applied gate-source voltage. An IGBT behaves similary (fig.A7b). The di/dt and I_{SC} control can be implemented with a driver stage which monitors drain-source or collector-emitter voltage (fig.A8). The rate of rise of gate-voltage is controlled through R1. The Zener diode, D2, clamps the gate voltage to, for example, 6V and thus limits I_{SC}.

Under normal operating conditions, the drain-source or collector-emitter voltage decreases after the reverse recovery of the freewheeling diode, T1 blocks and the gate voltage can increase to about 10V.

Such a circuit greatly limits energy stress under short circuit conditions.

TURN-OFF SWITCHING

The switching device should not be damaged during turn-off switching. A power transistor datasheet usually contains the test circuit used for establishing the safe operating area (SOA) of the device (fig.A9). During operation the load line should not cross the limits of the SOA, but it is important to remember that the SOA itself is valid for given drive, junction temperature and dV/dt conditions.

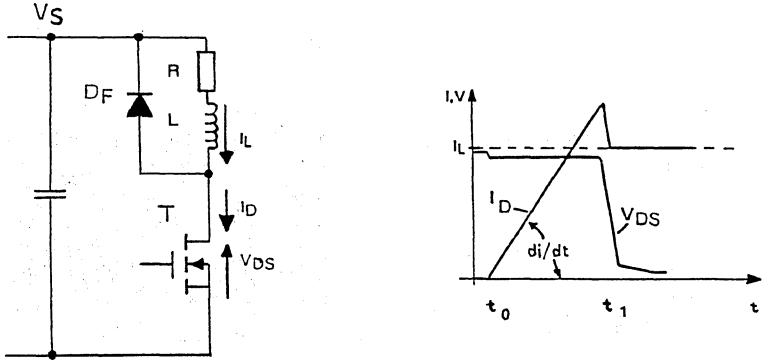


Fig. A5: Turn-on switching with a conducting freewheeling diode.

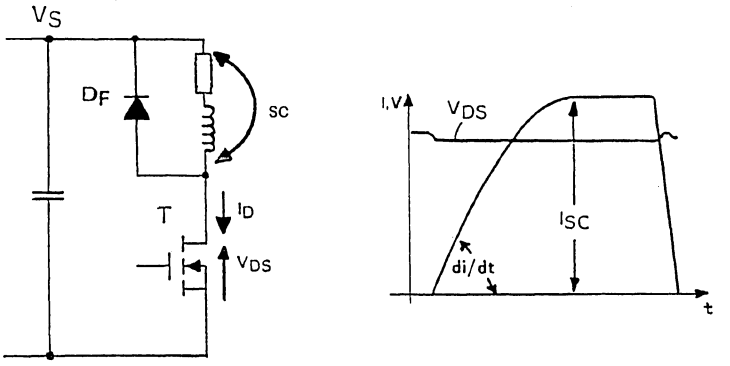
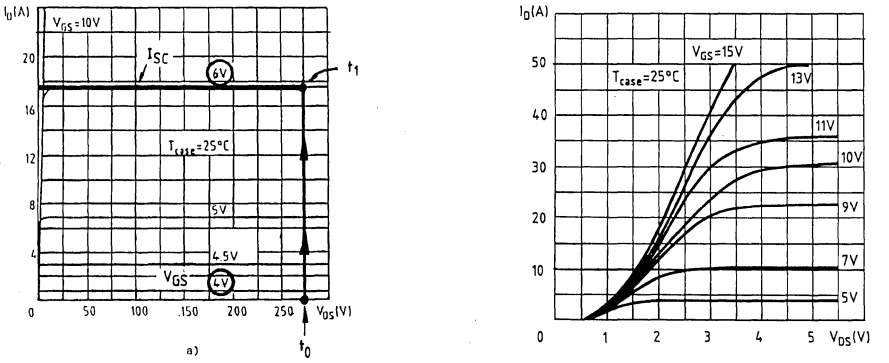


Fig. A6: Switching-on to a short circuit.



POWER MOSFET IRFP450 IGBT STGH20N50

Fig. A7: Output characteristics of a POWER MOSFET and an IGBT

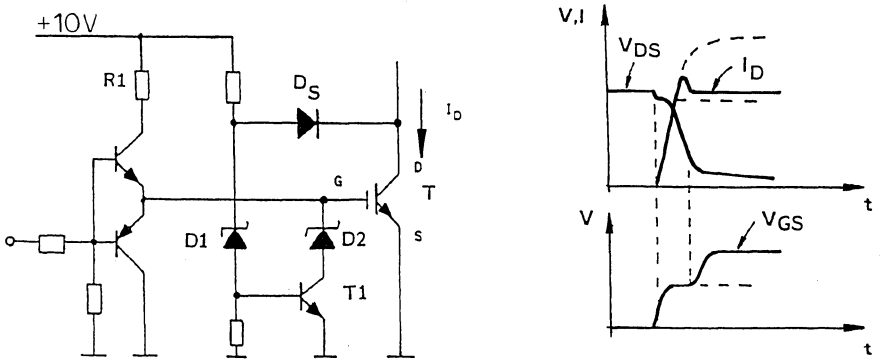
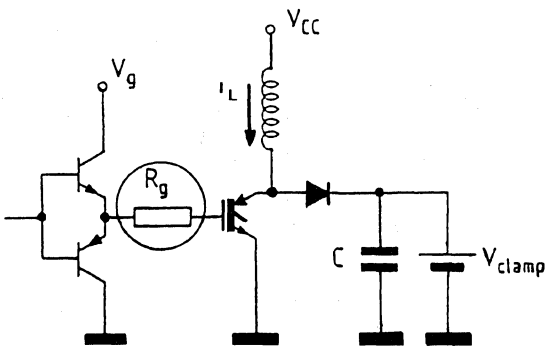
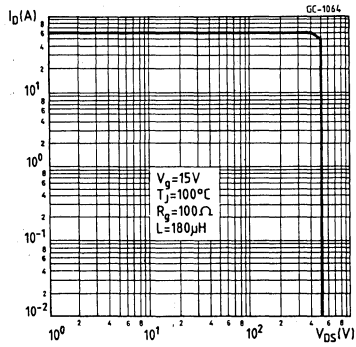


Fig. A8: Principle of driver stage controlling di/dt and short circuit current amplitude.



(a)

Reverse biased SOA



(b)

Fig. A9: Test circuit for the safe operating area (a) and SOA of IGBT STGH20N50 (b).

The rate of rise of collector-emitter-voltage (dv/dt), junction operating temperature, Tj, and drive conditions strongly affect the turn-off behaviour of IGBTs. In particular, the latching current is modified by these parameters.

The simplified equivalent circuit of an IGBT (fig.A10) can be used to understand modifications of latching current: transistor T1 conducts when the Power MOSFET structure is on; T2 will conduct when the voltage drop across Rs exceeds about 0.6V; the IGBT "latches" if this happens. Once the device latches removing the gate-emitter voltage will not turn off the device and the device may be destroyed.

The value of Rs doubles between 25°C and 125°C. The base-emitter threshold voltage of T2 diminishes at about 2mV/°K - both contributing to a reduction of latching current from 100% at 25°C to 30% at 125°C. At turn-off switching, a dv/dt between collector and emitter will add a capacitive current flowing into Rs, thus reducing latching current further and making it dependent upon dv/dt (fig.A11).

The resistance Rg between gate and emitter, strongly affects turn-off behaviour of Power MOSFETs and IGBTs. When the collector-emitter (drain-source) voltage increases, capacitive current flows into the drive circuit and leads to a voltage drop across Rg, thus maintaining V_{ge}(V_{gs}) at a dv/dt dependent level. The resistor Rg can be used to control dv/dt during turn-off. Thus turn-off losses, RFI and latching current can be set to desired values. The higher the Rg value, the lower the turn-off dv/dt and the higher the latching current.

B - DRIVER CIRCUITS FOR POWER MOSFETs AND IGBTs

Driver circuits have an influence on cost, performance and reliability of the whole power switching function.

Driver circuits should transform the logic level control signal into a suitable voltage/current waveform, exhibit low power consumption and often offer galvanic isolation between input and output.

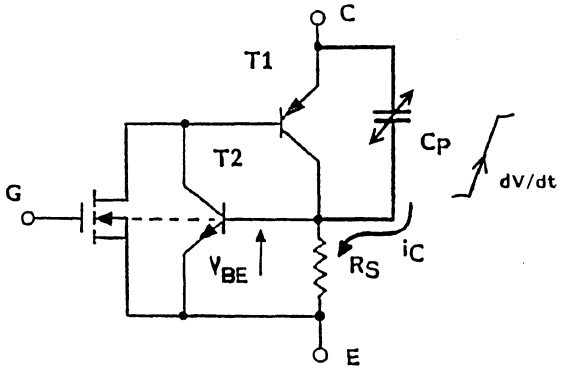


Fig. A10: Equivalent circuit of an IGBT for understanding the latching behaviour.

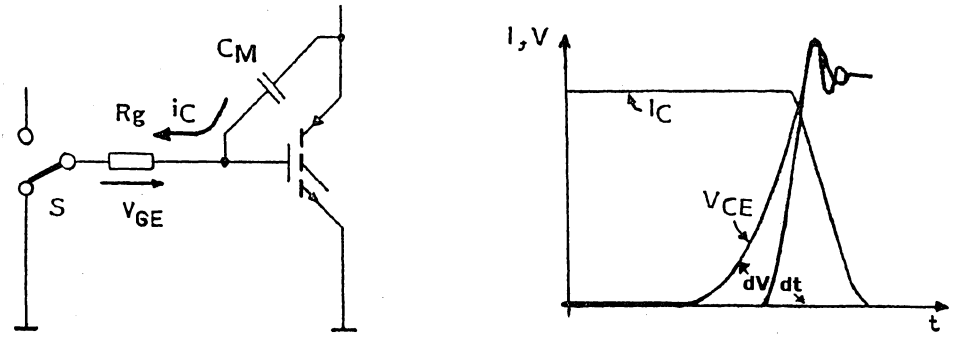


Fig. A11: Turn-off dv/dt as a function of gate resistance.

AVOIDING SPURIOUS TURN-ON

In bridge legs, Power MOSFETs and IGBTs are subject to dv/dt, when the opposite transistor switches on (fig.B1). This dv/dt will charge the parasitic drain-source or collector-gate capacitance and lead to a current flow out of the gate. If the voltage drop across Lp, Rp and Rg exceeds about 1V to 2V, the Power MOSFET/IGBT will conduct, leading to extra switching losses.

A driver stage having three different states gives a good compromise (fig.B2): dv/dt during turn-off switching can be set by means of Rg, thus obtaining excellent safety against latching and low RFI. After turn-off switching, a low driver output impedance gives good immunity against spurious conduction.

Nevertheless the parasitic resistance, Rp and inductance, Lp, should not exceed certain limits depending on dv/dt, die-size and parasitic package inductances.

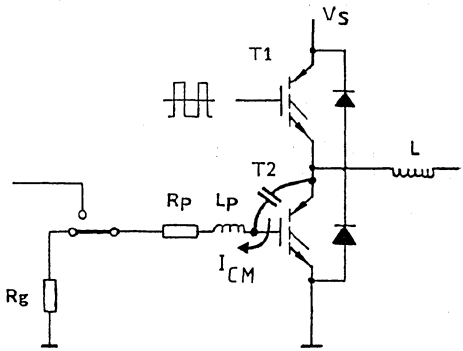


Fig. B1: Bridge leg with inductive load, where transistor T2 is subject to "passive" dv/dt.

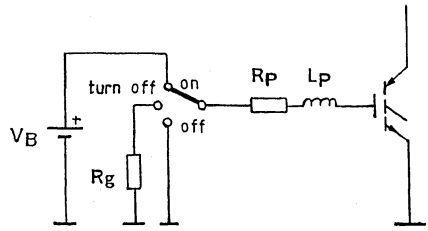


Fig. B2: Tri-state driver limiting turn-off dv/dt and having high immunity against passive dv/dt.

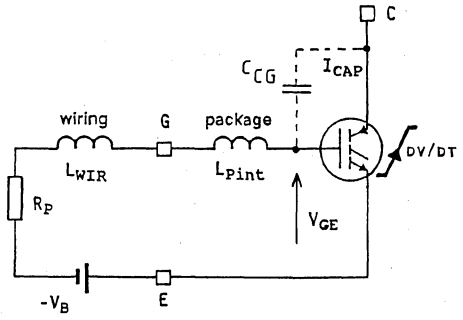


Fig. B3: IGBT with parasitic capacitances and inductances.

PACKAGE	MAXIMUM DRIVER IMPEDANCE
TO 220	10 Ω / 300 nH
TO 218	5 Ω / 150 nH
ISOTOP	2 Ω / 60 nH
TO 240	NEGATIVE BIAS
MODULE	NEGATIVE BIAS

dV/dt = 10kV/ µs

TABLE I: Maximum driver impedance as a function of device package.

MAXIMUM DRIVER IMPEDANCE/ NEGATIVE BIAS?

During dv/dt, the gate voltage should not exceed about 1 volt. The maximum driver impedance must be fixed at a value that is dependent on the die size, which is related to C_{CG} and the parasitic package inductance $Lp_{(int)}$ (fig.B3). If $Lp_{(int)}$ is very high, negative bias may be required in order to avoid spurious conduction. Table I indicates the maximum required driver impedance for a dv/dt of 10kV/µs.

PULSE CONTROLLED DRIVER SUITABLE FOR 0 - 1 MHz OPERATION

When applying a voltage pulse with, for example, a 10V amplitude and 500ns duration, to the gate of a Power MOSFET (T) or an IGBT,

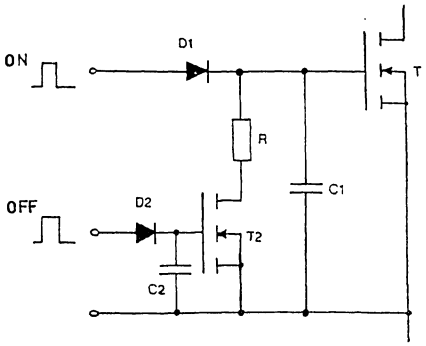


Fig. B4: Pulse controlled driver circuit memorizing on-state and off-state.

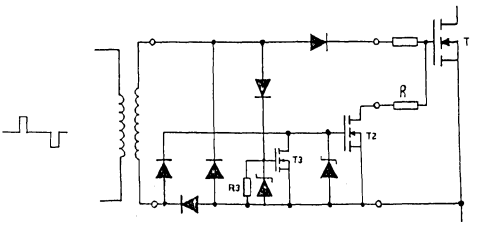


Fig. B5: Pulse controlled drive with transformer isolation. Even though there is no auxiliary supply, any pulse width, at virtually any relevant frequency, can be controlled.

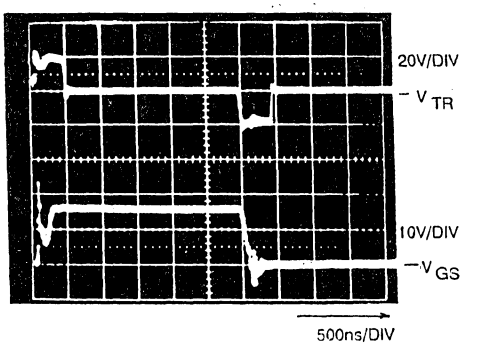


Fig. B6: Transformer output signal at gate-emitter/ gate-source voltage with pulse controlled driver.

harge will be stored in the gate capacitance fig.B4). Thus the power device will remain onducting, even after removal of the input ulse. This is called the "memory-effect".

f a similar pulse is applied to a second Power MOSFET (T2), the latter will conduct, lischarge the gate of Power MOSFET (T) and emain conducting - the off-state is memorised. Supposing R is low enough, dv/dt applied to Power MOSFET (T) does not lead to spurious conduction.

It is possible to add a pulse transformer for galvanic isolation and a third Power MOSFET (or bipolar transistor) can be used to discharge the gate of T2, whenever an "on-signal" is generated (fig.B5).

When using the "memory-effect", only pulses of about 5μVs have to be transmitted by the transformer; a very small toroid transformer is sufficient. Figure B6 shows the transformer output voltage and resulting gate-source/gate-emitter voltage. The circuit can handle any duty cycle.

RESONANT DRIVER FOR POWER MOSFETs AND IGBTs

Power MOSFET and IGBT driver circuits for high frequency conversion should drive the power devices in such away that the resulting switching losses are low. Even at high

operating frequency, the driver circuit should have negligible power consumption. Power MOSFETs and IGBTs are charge controlled devices. For turn-on one has to supply a certain amount of charge into the gate. For turn-off, charge has to be removed.

During switching, one can consider the drain source path of a Power MOSFET as a fast varying current source - moving in a drive determined time from conduction to zero current or vice versa.

Driving the gate with a rectangular shape current (constant amplitude during a certain amount of time) would enable faster charge removal and faster switching but it is difficult to realise. Resonant gate drive with an inductance between driver and gate is easy to realise - one can even use an increased parasitic wiring inductance. With this approach, the time to charge or discharge the gate can be reduced by a factor of about two. Depending on the circuit, gate charge can be recovered and gate drive power consumption reduced.

One of the possible resonant gate driver circuits can be supplied from a single 5V source, and it generates a ten volt gate voltage for conduction and a negative bias for the off-state.

Conventional gate driver circuits charge and discharge a Power MOSFET's input capacitance through resistors and a parasitic inductance Lp (fig.B7).

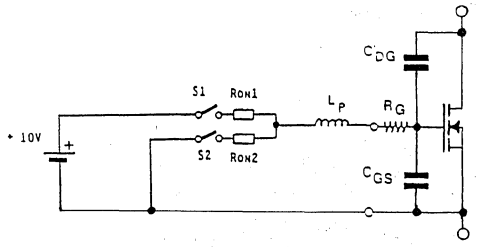


Fig. B7: Principle of conventional driver circuit with simplified equivalent circuit of MOSFET

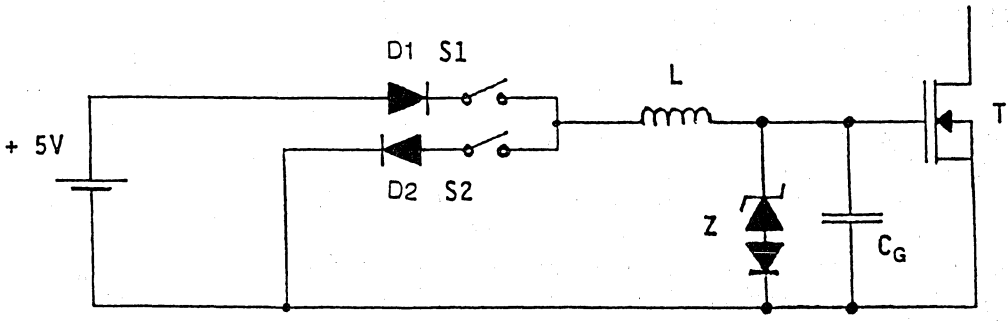


Fig. B8: Resonant gate driver. Power consumtion of the driver is 1/4 of a conventional driver.

At turn-on switching $E = {}^1/_2 CV^2$ is lost in $R_{on}1$. At turn-off switching, same amount of energy is lost in $R_{on}2$. When driving power Power MOSFETs at high frequency these losses become significant and should be reduced. Resonance effects can be used for this purpose (fig.B8).

When driver transistor S1 is turned on; a sinusoidal current flows into the gate capacitance of the power device. The gate voltage reaches about twice the driver supply voltage $V_{aux.}$ Thus, a Power MOSFET requiring a gate-source voltage of 10V can be driven from a 5V-supply. The diode D1 avoids discharging the gate. For turn-off switching, S2 is closed, a sinusoidal current removes the charge from the gate. The gate-source, or gate-emitter in the case of an IGBT, voltage of the power device is inverted (negative). Most of the stored energy is used to generate a negative bias voltage (fig.B9). Diode D2 avoids discharging the negative gate charge. Due to resonance overvoltage, gate voltage would reach the breakdown voltage of the gate oxide after a number of switching cycles.

A Zener diode, Z, has to be used to limit gate voltage. The energy consumption of a resonant gate driver is about a quarter of that of a conventional driver.

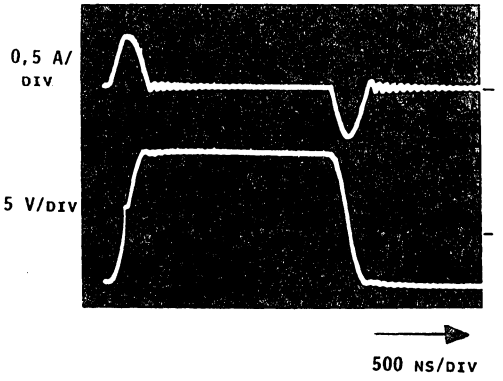
The charging and discharging of a capacitor with a given peak current, is achieved more rapidly through an inductance of an appropriate value. Resonance driver circuits therefore have the ability for the fast switching of power devices (fig.B10).

C - LOSS REDUCTION IN PWM CONVERTERS

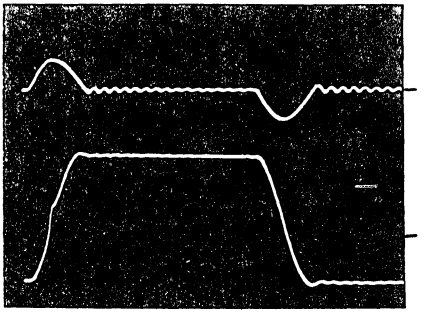
PARASITIC CAPACITANCES CONTRIBUTE TO LOSSES

The influence of the Power MOSFET output capacitance is negligible in low voltage, low frequency applications. This changes greatly when increasing operating voltage and switching frequency. The effect of the output capacitance, C_{out}, has to be taken into account in high voltage, high frequency applications.

For switching loss evaluation, it is possible to



a) POWER - MOSFET IRFP450



b) IGBT STGH20N50

Fig. B9: Gate-current and gate-source/gate-emitter voltage waveforms.

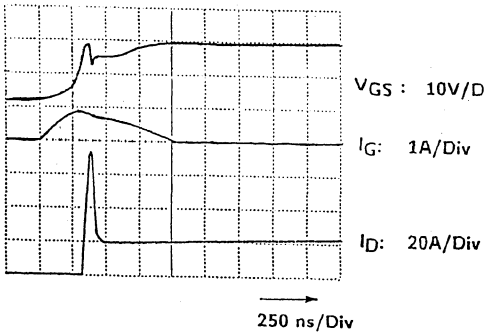


Fig. B10: An ISOFET TSD5MG40V (1000V, 0.7Ω) driven by a resonant driver. Switching losses are greatly reduced.

use a simplified equivalent circuit of Power MOSFETs (fig.C1).

The function of the output capacitance can be understood as a built-in capacitive snubber. At turn-off switching, this capacitance is charged from V_{on} to the maximum voltage $V_{DS(off)}$ applied to the Power MOSFET (fig.C2). Once charged, the capacitor contains energy. Depending on the converter structure, this energy may either be recovered or dissipated.

In PWM circuits (fig.C3) the Power MOSFET discharges its output capacitance at turn-on switching and ($0.5 * C_{out} * V_{DS(off)}^2$) Joules are lost. ($C_{out}$ is the effective output capacitance of the Power MOSFET, $V_{DS(off)}$ the drain source voltage just before turn-on switching).

The discharge-current flows inside the Power MOSFET, it cannot be observed on an oscilloscope.

HOW TO MEASURE STORED CHARGE ?

A simple circuit can be used for evaluation and specification of the output capacitance (fig.C4): The device under test (DUT) is connected to a high voltage supply via a resistor. A second Power MOSFET is paralleled to the DUT. The Power MOSFET under test is permanantly blocked, the second Power MOSFET switches periodically. At turn-on of the latter, you can observe the discharge current and time on an oscilloscope and determine the amount of charge, energy and the value of the capacitance.

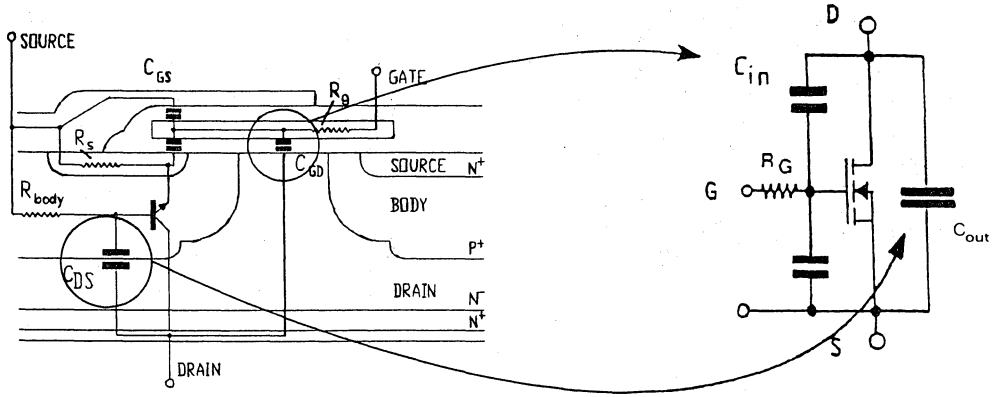


Fig. C1: Power MOSFET cross section - a) parasitic capacitors b) equivalent circuit.

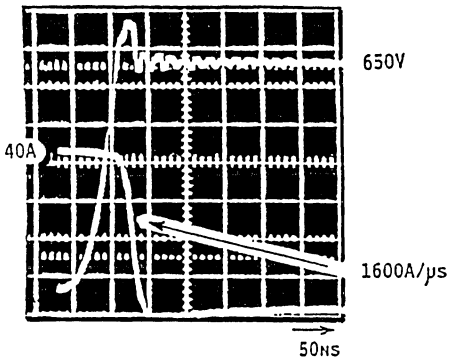


Fig. C2: Turn-off switching of a 1000V-0.7Ω Power MOSFET.

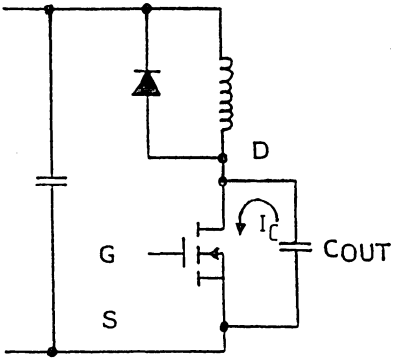
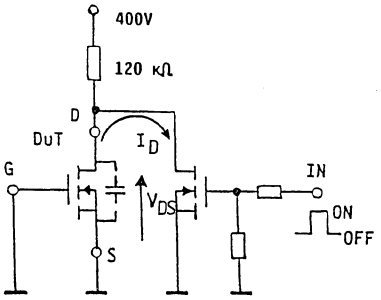


Fig. C3: Discharging output capacitance during turn-on switching.



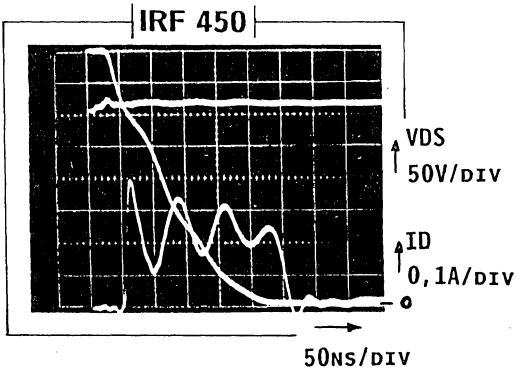


Fig. C4: Evaluation of Power MOSFET output capacitance,
a) test circuit,
b) waveforms with IRF450, $V_{DS(off)}$ = 400V.

ON-RESISTANCE - CAPACITIVE LOSSES

A Power MOSFET's contribution to converter losses are conduction, switching and gate drive losses. Conduction losses can be reduced by increasing the die size, leading to smaller on-resistance. Increased die size introduces increased output capacitance and switching losses (fig.C5).

Minimum losses are obtained when losses due to discharge of the output capacitance and conduction losses are equal (fig.C6). Optimisation depends on the supply voltage, the converter structure and the switching frequency.

The consequences are: from a certain

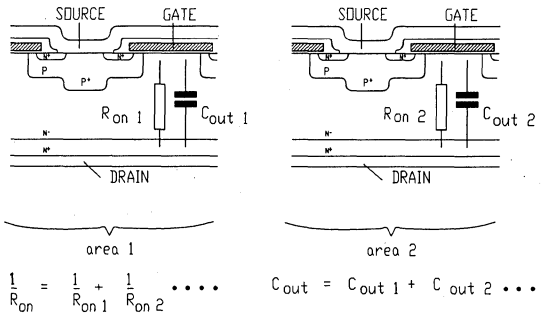


Fig. C5: Power MOSFET cross section. Increase of silicon area or paralleling discrete devices reduces on-resistance but increases output capacitance.

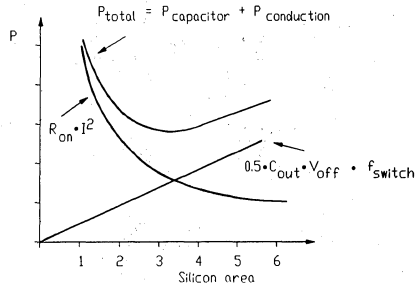


Fig. C6: Conduction and switching losses versus area. Total loss has a frequency dependent minimum.

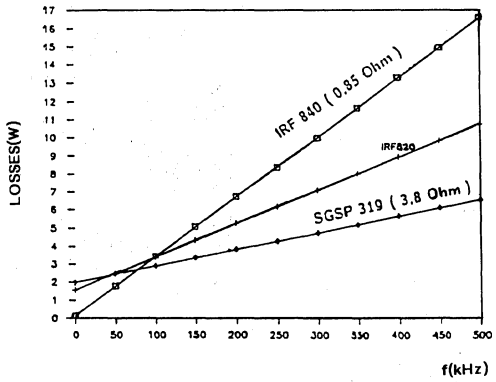


Fig. C7: Total losses versus frequency calculated asymmetrically with three 500V Power MOSFETs (same technology, different on-resistance).

switching frequency upwards, a size reduction of the Power MOSFET leads to improved efficiency, even when it is associated with an increased on-resistance.

In SMPS applications with PWM and with a maximum drain-source voltage of 400V, switching losses due to the discharge of the output capacitance are dominant at switching frequencies exceeding 100kHz to 150kHz (fig.C7). For loss reduction in SMPS operating below 100kHz Power MOSFETs with low on-resistance are preferable - above 100kHz Power MOSFETs with low output capacitance and higher on-resistance are better.

INFLUENCE OF TOPOLOGY

Comparing energy stored in the two Power MOSFETs of an asymmetrical half bridge

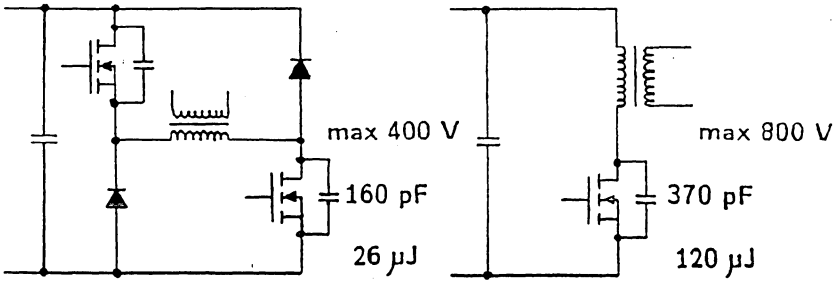


Fig. C8: Energy stored in the output capacitance of two 0.4Ω 1000V Power MOSFETs and in one 0.8 Ω - 1000V MOSFET.

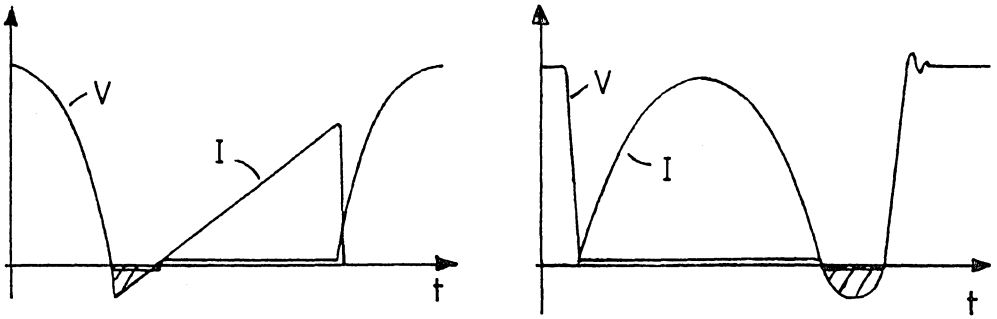


Fig. D1: Typical waveforms with zero voltage switching (a) and zero current switching (b).

flyback converter with a single switch flyback shows that significantly more energy is stored in the high voltage device used in the single switch flyback (fig.C8). It is possible to estimate that between 30% to 60% of that energy is dissipated.

D - POWER MOSFETs AND IGBTs IN RESONANT CONVERTERS

A large number of different resonant and quasi-resonant topologies exist. For the purpose of choosing semiconductors, one can distinguish two basic modes of operation: Zero voltage switching and zero current switching (fig.D1). The other modes are in between. IGBTs are as simple to drive as Power MOSFETs and offer, in the area of high voltage switching, much better on-resistance per unit silicon area and may offer less conduction losses or lower costs. Depending on the converter topology, either Power MOSFETs or IGBTs may be more suitable.

ZERO VOLTAGE SWITCHING

A typical circuit with zero voltage switching consists in a switch, T, with paralleled capacitor and series choke (fig.D2). The whole is supplied from a voltage source. During conduction in the switch, the choke current increases with time. At turn-off, the voltage across C and the switch increases as a sinuoidal function and may reach several times the supply voltage (fig.D3). Afterwards it swings back to below zero where it is clamped by the diode. The output capacitance of the semiconductor switch and the capacitor are discharged via the inductance. Thus the energy is recovered. The only losses are due to the parasitic resistance Rs, which is a part of the Power MOSFET's on-resistance. Increasing silicon area reduces on-resistance, Ron, and parasitic damping resistance, Rs. An increase of silicon area is not paid for with an increase of capacitive loss. Power MOSFET switching losses can be considered as negligible with this operation mode.

High voltage IGBTs exhibit significantly lower conduction losses than high voltage Power MOSFETs with similar die size. The IGBT can be understood as a Power MOSFET driving a PNP-bipolar transistor (fig.D3). The on-resistance of the Power MOSFET is virtually divided by the bipolar gain. It is possible to compare the switching to that of a high voltage PNP-transistor, switching with open base - resulting in a collector current tail. This tail cannot be ignored as the resulting loss is a major limitation for the application of IGBTs in converters with zero voltage switching.

ZERO CURRENT SWITCHING

A typical circuit using zero current switching consists of a switch with a series choke, the whole paralleled with a capacitor and supplied

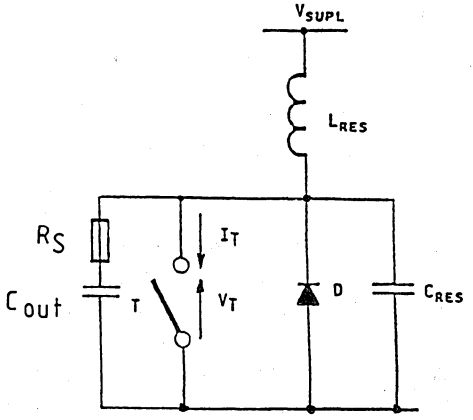


Fig. D2: Typical circuit with zero voltage switching.

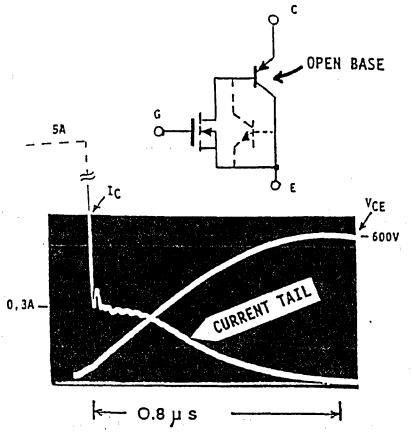


Fig. D3: Equivalent circuit of an IGBT and waveforms in a ZVS-circuit. Even a small tail current leads to significant turn-off energy loss.

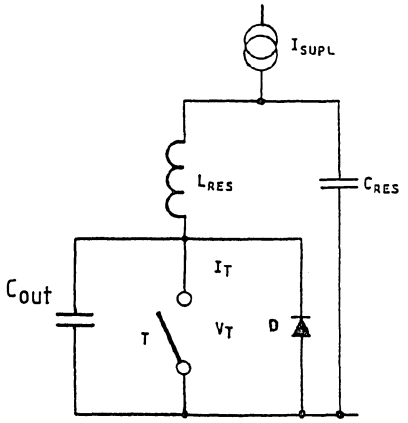


Fig. D4: Typical circuit with zero current switching.

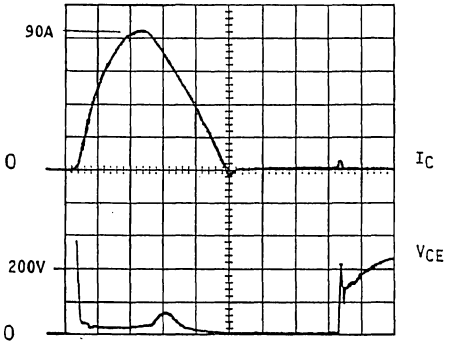


Fig. D5: Collector current and collector emitter voltage of a 10 Amp-500Volt IGBT (STGP10N50) with zero current switching.

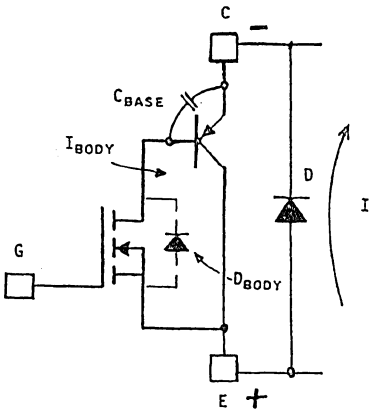


Fig. D6: Equivalent circuit explaining the absence of a current tail. When the collector-emitter voltage of the IGBT is negative, a current flows thourgh the body diode into the base of the PNP. This current blocks the PNP structure efficiently.

from a current source (fig.D4). At turn-on, the current through the switch increases with a sinuoidal function and then swings below zero (fig.D1). The negative half wave flows through the diode.

At turn-on switching, output capacitance is discharged into the switch; capacitive losses similar to PWM-converters can be observed. IGBTs do not show current tail in this configuration! After the zero crossing of the collector current a short negative current pulse can be observed (fig.D5). It flows through the body diode into the base of the PNP, sweeping stored carriers away, thus avoiding current tail and corresponding losses (fig.D6). IGBTs are very suitable for resonance converters with zero current switching where they offer a better cost/performance compromise than Power MOSFETs and can be operated at frequencies of several hundred kHz.

RESONANCE IN PWM CIRCUITS

The advantages of zero current switching with IGBTs can also be used in PWM converters: (this is similar to forced switching circuits as used with SCRs - improved MORGAN circuit (fig.D7).

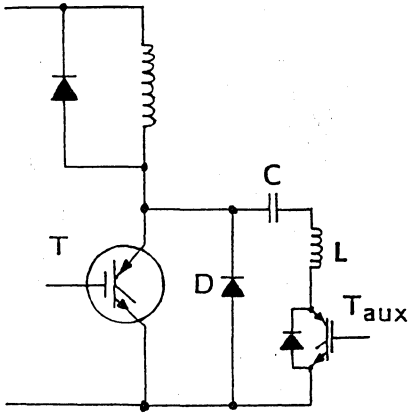


Fig. D7: Circuit using resonance in a PWM converter. With this circuit the IGBT is virtually free from turn-off losses and can be used at inaudible frequencies.

With these circuits it is possible to take advantage of the high current handling capability of IGBTs without any risk of loosing control as is the case with these earlier thyristor circuits. Thus PWM operation of IGBTs at inaudible switching frequencies is possible.

CONCLUSION

Investing more effort into understanding and designing driver circuitry for Power MOSFETs and IGBTs opens the way to better performance, lower costs and new applications.

Through suitable gate control, Power MOSFETs can be made even faster. However, it is also possible to slow them down in order to reduce RFI-filter requirements in phase control, soft start circuits etc...

Through zero current mode operation, the current tail of IGBTs can be avoided, and then IGBTs can be operated in PWM circuits at up to 20kHz and resonant converters even at 200kHz. Maybe some of the well proven thyristor circuit topologies could be used and even improved with IGBTs.

The key to all these new applications with improved performance is in forgetting prejudice and thinking about what really happens inside the power semiconductor devices.

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SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

INSULATED GATE BIPOLAR TRANSISTORS IN HIGH FREQUENCY RESONANT CONVERTERS

by J.M. Burgeois, B. Maurice

ABSTRACT

IGBT technology produces devices that are easy to drive, are capable of switching at high voltages and currents and operate at high current density.

A common application for this class of device is in off-line motor drives that use them in a "hard" switching mode.

Designs are now begining to be made that use the IGBT in resonant converters with "soft" switching and that operate at higher frequencies.

This paper discusses the operating limits of IGBTs in resonant circuits. In particular, this analysis considers the thermal balance and the maximum current density that can be achieved by IGBTs in this type of application. The major resonant sub-circuits are highlighted and the duality rules that permit the use of these circuits in place of other configurations, discussed.

Finally, a practical circuit is given for driving and protection of IGBTs.

1. INTRODUCTION

Resonant converters will operate at much higher frequencies than conventional designs of converters. For this reason they are attractive because using a higher operating frequency means that the size of passive components in the circuit will be smaller. The higher frequency is possible because the converter switching losses are lower. The extent of this improvement is dependent on the converter structure and mode of operation. Until recently resonant converters used SCRs, bipolar transistors or Power MOSFETs as switching elements.

The purpose of this paper is to consider the use of IGBTs in resonant converters. IGBTs combine some of the advantages of bipolar transistors and Power MOSFETs. For example easy voltage drive, fast and efficient protection and low on-state dynamic resistance. The paper also analyses IGBT losses and the dependence of their maximum operating frequency on the converter structure and mode of operation. A practical example is discussed that uses a fast IGBT, the STGP10N50, which is rated at 10 Amps/500 volts.

2. RESONANT STRUCTURE

The resonant switch is the basic element of any resonant converter. It is a single tuned sub-circuit that includes a switching component, a diode, an inductor and a capacitor. Depending on the position of the diode, this resonant switch is uni- or bi-directional, thus providing half or full wave operation. The major feature of this type of sub-circuit is its ability to switch at zero current (or zero voltage). This reduces the switching losses as compared to "hard" switching circuits. This means that current and voltage do not occur simultaneously across the switch. As a result the switch will only experience either a voltage or a current.

There are two main resonant converter configurations:

a) A quasi resonant converter which uses one resonant switch excited in discontinuous operating mode by pulse frequency modulation. Because the current (or voltage) wave is whole (the waveform is unbroken) the switching behaviour of the resonant switch is maintained. Evaluation of the losses in the IGBT in these converters is made using the two basic operating modes: zero current mode (ZCM) and zero voltage mode (ZVM).

b) A resonant converter uses a minimum of two resonant switches in a symmetrical structure. It allows continuous operating mode operation which changes the switching conditions of the resonant switch: it is not a whole wave mode and zero current (or zero voltage) switching occurs, depending on the switching frequency, only at turn on or at turn off. So, a large fraction of the IGBT's losses can be deducted from the quasi resonant analysis.

Section 3 gives an accurate analysis of IGBT losses in quasi resonant converters. The overview of switching conditions in resonant converters provides the basis for loss evaluation using the analysis of the previous section.

3. IGBTs IN QUASI RESONANT CONVERTERS

As already stated previously, in quasi resonant converters the IGBT operates as a single tuned resonant switch with a quasi sinusoidal current (or voltage) waveform. This analysis examines each mode.

3.1 IGBTs IN ZERO CURRENT SWITCHING QUASI RESONANT CONVERTERS.

a. Switching: The IGBT's switching behaviour is analysed using the circuit shown in figure 1 - full wave mode zero current switching (ZCS) quasi resonant converter.

Because the collector current is zero during switching (see fig 2 & 3), the only switching losses occuring are due to the internal discharge of the IGBT output capacitance at turn-on. The discharge current is not detectable externally, but the charging current appears in figure 3 when voltage is re-applied to the collector. Integration of the current waveform shows that the energy stored in the output capacitance of this IGBT is about 10µJ at 400V.

b. Conduction: Figure 4 shows that the current factor is low due to the discontinuous operating mode of the quasi resonant converter. For this reason it is important to be able to use the switch at high current density and this is the major characteristic of an IGBT.

Figure 5 shows the IGBT saturation at high current and its dependence on gate source voltage. The current saturation threshold is virtually independent of temperature (less than 10% between 85°C and 95°C) and conduction time (unchanged between 1µsec and 5µsec).

An IGBT with a nominal current of 10A can conduct more than 80A without saturation. However, with a ZCS quasi resonant converter, the maximum operating current is limited by conduction losses as follows:

Considering the maximum switching frequency (duty cycle < 50%) and the transfer characteristics given in figure 6, the conduction losses are:

$$P_{cond} < (1.4\ I_{pk}/\pi) + (0.118\ I_{pk}^2/4) \text{ watts}$$

for a 30A peak P_{cond} < 40W - a maximum realistic value for a TO-220 package.

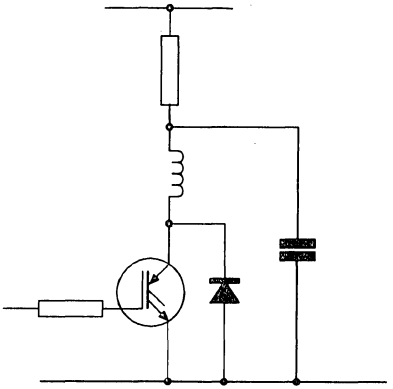


Fig.1: Full-wave mode ZCS quasi resonant converter IGBT STGP10N50 10A/500V.

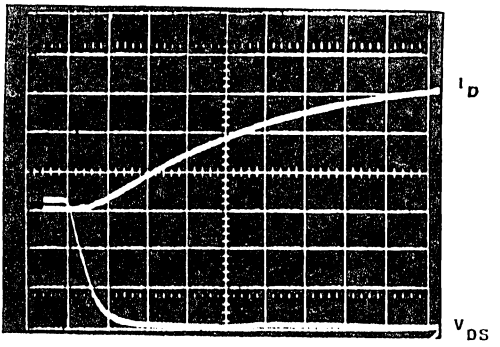


Fig.2:Turn on switching circuit defined in figure 1

V_{DS} = 100V/div R_C = 50 Ohms

I_D = 20A/div t = 100nsec/div

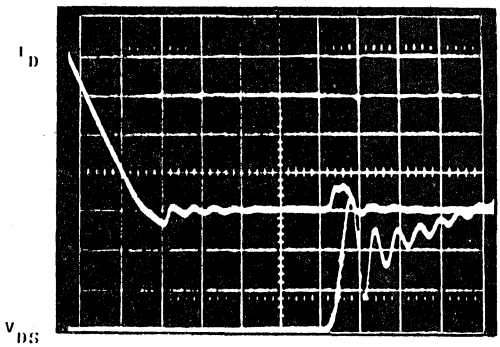


Fig.3:Turn on switching circuit defined in figure 1
V_{DS} = 100V/div T_{case} = 50°C
V_{GS} = 5V/div R_G = 10 Ohms
I_D = 20A/div t = 100nsec/div

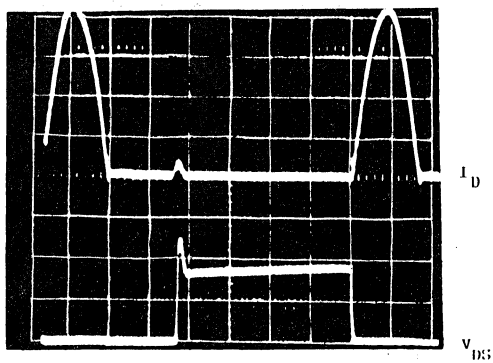


Fig.4: Drain current and voltage wave form.
Circuit defined in fig. 1 (a snubber is used in order to avoid voltage oscillations)
I_D = 1A/div V_{DS} = 100V/div t = 5msec/div

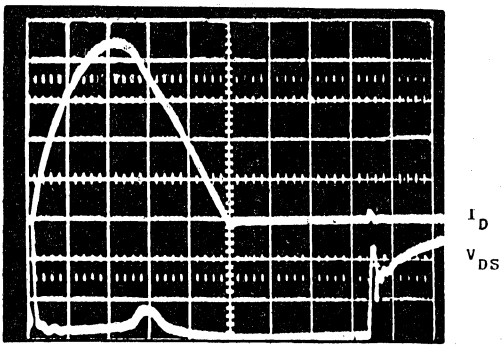


Fig.5: Saturation test circuit defined in figure 1
I_D = 20A/div V_{DS} = 5V/div V_{DS} = 100V/div
t = 1msec/div

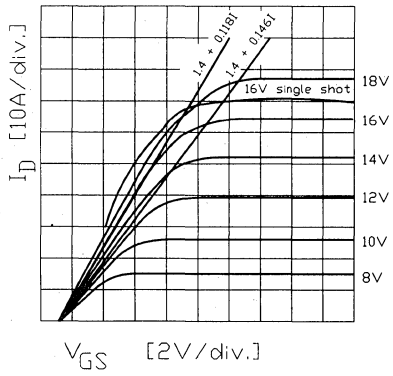


Fig.6: Characteristics of STCP10N50
Tj = 100°C
$V_{DS(on)}$ = 1.4 + (0.118 x 1) for V_{GS} = 15V

c. Operating range and limits: When the STGP10N50 operates over its full frequency range the peak current in this converter should be limited to 30A by the conduction losses. In any case the RMS current is compatible with die bonding:

$$I_{RMS} = \sqrt{d}\, I_{pk} / \sqrt{2} = I_{pk} / 2$$

at maximum frequency with 30A peak I_{RMS} < 15A.
As there are no major switching losses (10 µJ), a ZCS converter is able to operate at several hundred kilohertz.

3.2 IGBTs IN ZERO VOLTAGE SWITCHING RESONANT CONVERTERS.

a. Switching: The IGBT's switching behaviour is analysed using the circuit in figure 7, a half-wave zero voltage switch (ZVS) quasi resonant converter.

The intrinsic properties of an IGBT create specific losses due to the current tail induced by stored minority carriers, in spite of the "soft" voltage switching. Contrary to bipolar transistors, these carriers are not discharged rapidly as there is no access to the base and they induce losses when voltage is re-applied after current turn-off.

Figure 8 shows current and voltage waveforms in the IGBT during conduction and after current turn-off. Figure 9 shows an example of the evaluation of the turn-off energy (E_{ct}) by integration of the current, time and voltage.

Current tail losses were measured with respect to temperature, switched current and re-applied voltage. The results of these measurements are shown in figures 10 to 15. They show that turn-off losses are proportional to dV/dt when current and temperature are constant and proportional to the square of the current when temperature and dV/dt are constant.

- Current tail losses = $P_{ct} = K_{(dv/dt,Tj)} \cdot I^2 \cdot f$
- As K is proportional to dV/dt (ref: figures 13, 14, 15 - gradients of the curves) and dV/dt is proportional to I in such an inverter, the losses can be expressed as:

$$P_{ct} = K'_{(Tj)} \cdot I^3 \cdot f$$

where I = switched current.

As K' increases rapidly compared to T_j, the maximum switched current must be strictly limited and the heatsink sufficiently sized to avoid thermal runaway.

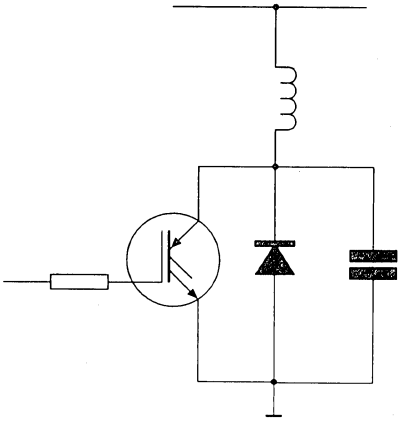


Fig. 7: Half wave mode ZVS quasi resonant converter

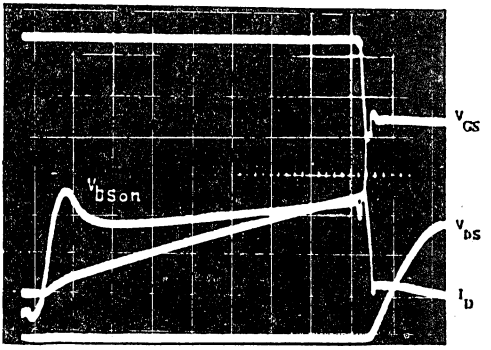


Fig. 8: Drain current and voltage wave form. Circuit defined in figure 7.
I_D = 5A/div V_{DSon} = 1V/div
V_{DS} = 100V/div V_{GS} = 10V/div

b. Conduction. In this type of converter, IGBT conduction losses are not a constraining factor due to the low average current. They can easily be calculated by integration, (current x voltage) figure 8.

c. Thermal balance. The circuit shown in figure 7 is used where:

switched current = I_p = 20A

dV/dt = 1500V/sec

t_{on} = 9.5 msec

The losses due to the current tail can be calculated by subtracting the conduction losses from the total measured losses (thermal balance). An alternative method is to use the numerical integration as shown in figures 9 to 15:

As the results are similar, the numerical integration allows easy calculation of the losses.

d. Operating range and limits. Considering the IGBT switching its normal current, the

Frequency	E_{ct} (Thermal balance)	E_{ct} (numerical integration)
6kHz	566mJ	420mJ
8kHz	725mJ	600mJ

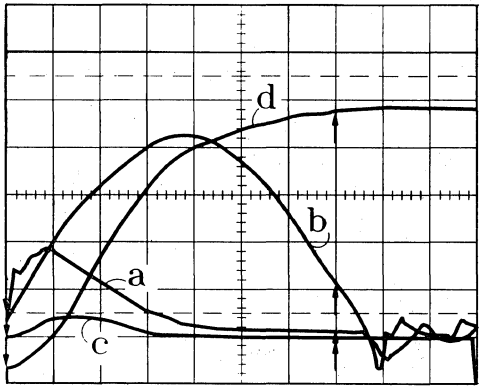


Fig. 9: Energy evaluation circuit defined in fig. 7.
curve a: current tail (1A/div)
curve b: drain voltage (100V/div)
curve c: (curve a) x (curve b)
curve d: curve c x dt

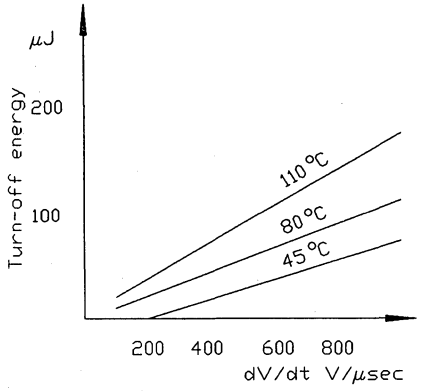


Fig. 10: Turn-off energy E_{ct} 10A switching

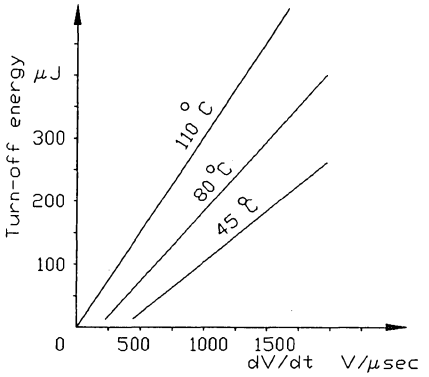


Fig. 11: Turn-off energy E_{ct} 15A switching

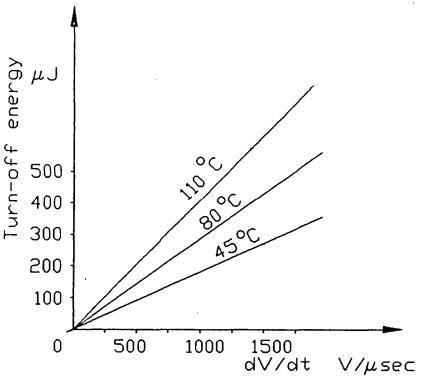


Fig. 12: Turn-off energy E_{ct} 20A switching

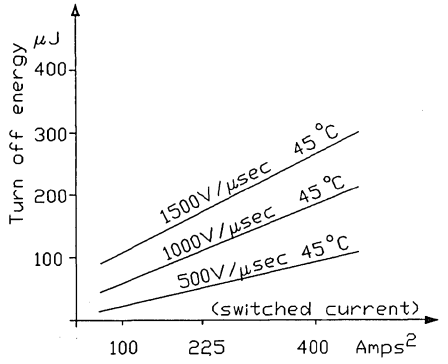


Fig. 13: Turn-off energy E_{ct} - T_j = 45°C

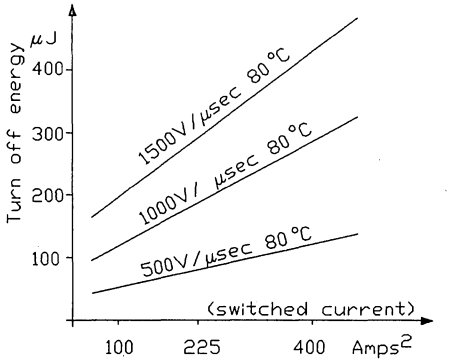


Fig. 14: Turn-off energy E_{ct} - T_j = 80°C

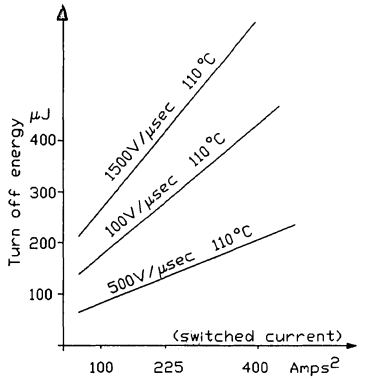


Fig. 15: Turn-off energy E_{ct} - T_j=110°C

maximum switching frequency can be evaluated with, for example, the following conditions:

I_{peak} = 10A dV/dt = 500V/msec

Switching losses = 10W

(Safety margin = 33%) ref:- figures 10-15

T_j = 80°C operating frequency = 110kHz

T_j = 110°C operating frequency = 80kHz

This shows that using IGBTs in this configuration is possible up to 80kHz with fast IGBTs .

4. IGBTs IN RESONANT CONVERTERS.

The switching conditions of this type of converter are dependent on the switching frequency because they work in the continuous operating mode. For this reason, close to the resonant frequency, the constraints on the IGBT are similar to those of the quasi resonant converter in the ZCS or ZVS mode, whereas above or below the resonant frequency, a different switching mode occurs.

4.1 Voltage excited resonant converter.

An example of a voltage excited resonant converter circuit is shown in figure 16. Voltage excitation requires a current load, i.e. a series resonant circuit.

a. Operating above the resonant frequency
At switch-on: IGBTs operate in the ZCS mode without dV/dt and therefore have negligible losses.
At switch-off: Current and voltage are switched together; as dV/dt is generally reduced by using an external capacitor, the turn-off losses are limited to current tail losses. Consequently, in this situation, the results of the ZVS quasi resonant converter analysis can be applied again.
Conduction in the on-state: The maximum conduction losses occur close to the resonant frequency. They can be calculated using the ZCS quasi resonant converter analysis.

An example:

Conditions: Device STGP10N05 IGBT

T_j = 110°C maximum

dV/dt = 1000V/msec

maximum peak current = 16A (close to f_r)

maximum switched current ≈ 8A ($f \approx 2f_r$)

Considering that the maximum conduction losses = maximum switching losses

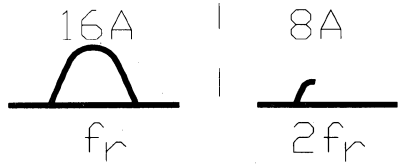
maximum conduction losses =

$(0.445 \cdot I) + (0.0295 \cdot I)^2$ = 15W (for 16A)

maximum switching losses = $E_{ct} \cdot f$

(for 8A see the curve in figure 15)

The corresponding operating frequency is from 30kHz (f_r) to 60kHz ($2f_r$). As in the case of the ZVS quasi resonant converter, the maximum switched current must be strictly limited and the heatsink sufficiently sized in order to avoid thermal runaway.



b. Operating below the resonant frequency:
At switch-on: Current and voltage are switched together. The losses are due to the discharge of the IGBT's output capacitance and to the recovery of the diode on the other IGBT.

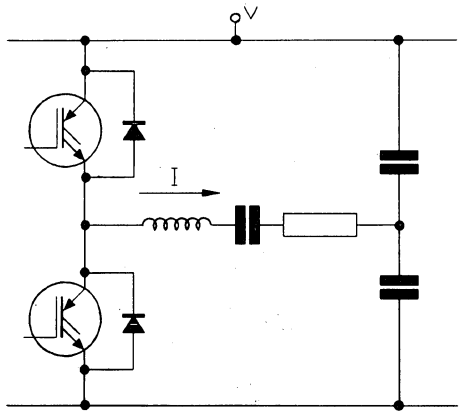


Fig. 16: Voltage excited resonant converter

The maximum losses can be evaluated as:

$$1/2\ Vf(I_{peak\ max/}2 + I_{RM})^2\ dt/dI$$

I_{RM} = diode peak reverse current

At switch off the IGBT is operating in ZCM without switching losses.
Conduction: the maximum conduction losses can be evaluated as for the ZCS quasi resonant converters because it is operating in full wave mode close to the resonant frequency.

An example:
Conditions IGBT = STGP10N50

dI/dt = 300A/sec
V = 300V
T_j = 110°C
I_{RM} = 16A
maximum peak current = 20A
maximum switched current ≈ 10A

Considering:

maximum conduction losses = maximum switching losses

maximum turn-on losses = 338J

maximum conduction losses = 24W

The corresponding operating frequency is from 70kHz (f_r/2) to 140 kHz (f_r). Contrary to the previous mode, there is no risk of thermal runaway and the IGBT seems to be a good alternative to SCRs in this type of high frequency converter.

4.2 CURRENT EXCITED RESONANT CONVERTER.

An example of a current excited resonant circuit is shown in figure 17. It is the duality of the previous circuit shown in figure 16. The current excitation requires a voltage load giving a parallel resonant circuit. The switching behaviour depends on the operating frequency.

a. Operating above resonant frequency:
When one IGBT is switched on there is reverse recovery current from the diode of the second IGBT through the capacitor. This means both current and voltage are switched. The maximum losses can be evaluated as:

$$1/2\ f.V(I_{RM} + I_D)^2\ dt/dI$$

where:

V = maximum switched voltage
I_{RM} = diode recovey current
I_D = maximum switched current

At switch-off: the serial diode recovery current reverses the IGBTs current and its collector-emitter voltage. Because of this the reverse recovery charge, Qrr, of the series diode must be kept lower than that of the internal P/N diode of the IGBT as this would cause the IGBT's diode to exceed its breakdown voltage, and conduct the leakage current of the series diode.
However, current tail losses can occur when re-applying voltage during the off state, and depend on the minority carrier lifetime versus the delay between the diode recovery and the positive collector voltage rise. The maximum turn-off losses occur close to the resonant frequency and are similar to those of ZVS quasi resonant converters.
Conduction: The current flowing is continuous and the duty cycle is 50%. The losses are:

$$\approx 1/2\ I_D \cdot V_{DS(on)}$$

b. Operating below resonant frequency.
At switch-on: The IGBTs operate in ZVS mode giving negligible switching losses.
At switch-off: Current and voltage are

switched-off. Consequently, losses can be evaluated using the ZVS quasi resonant converter results.

Conduction: The duty cycle is not dependent on the frequency so the losses are similar to those above.

5. DRIVE AND PROTECTION CIRCUIT.

The analysis of IGBTs in resonant converters shows that many different switching conditions can occur. The circuit shown in figure 18 is suitable for driving an IGBT gate as it provides the following functions:

- Short circuit protection and current limiting.
- Adjustable sinking and sourcing output current.
- Very low output impedence after turn-off, masking the Miller effect.

6. CONCLUSION

This analysis shows that IGBTs are perfectly suited to resonant converters when the turn off switching is zero current mode. In this situation the switching frequency can rise to several hundred k Hertz giving a controlled current several times its own nominal current. IGBT's are an attractive replacement for more traditional switching components already in use in resonant converters. They offer the following advantages when replacing:

SCRs: the IGBT provides high dV/dt immunity and virtually no dI/dt limit, no t_q and very fast dynamic behaviour. It is very easy to protect under both dynamic and static conditions.

Bipolar Transistors: the IGBT offers very easy gate drive.

Power MOSFETs: IGBTs have a higher current density.

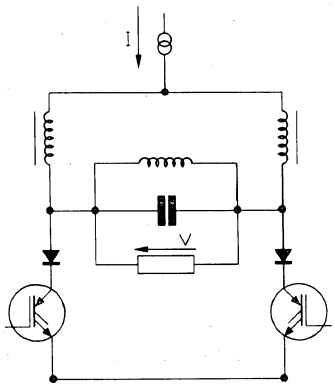


Fig. 17: Current ecited resonant converter

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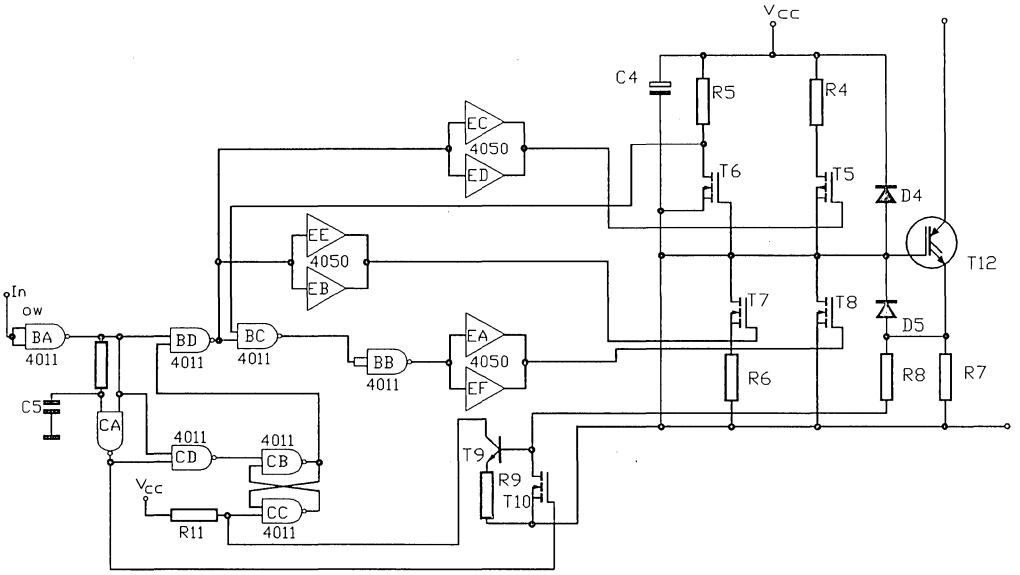
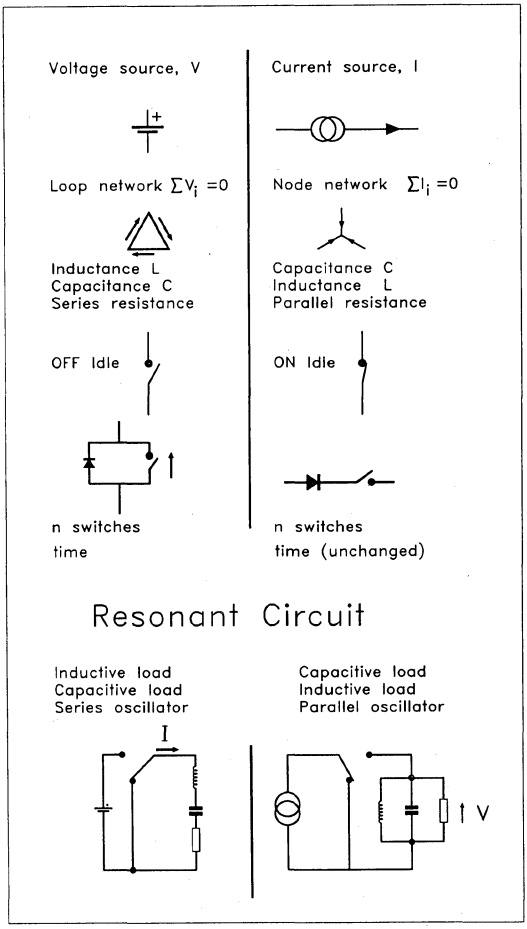


Fig. 18: Gate drive circuit.

APPENDIX .

DUALITY CONSIDERATIONS
OF AN ELECTRIC CIRCUIT

1. Every voltage source (or load) has a capacitive nature.
   Every current source (or load) has an inductive nature.
2. Connected source and load must always have opposing natures:
   - Capacitive source with inductive load
   - Inductive source with capacitive load.
3. A voltage source becomes inoperative when the output is open.
   A current source becomes inoperative when the output is shorted.
4. Every circuit has duality. The duality rules are set out below.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

BIPOLAR JUNCTION TRANSISTORS, POWER MOSFETs OR IGBTs IN RESONANT CONVERTERS

by P. Fichera

ABSTRACT

Resonant switch topologies operating on the principle of zero-current and zero-voltage switching are discussed. Their advantages with respect to the conventional PWM converter are shown.

The main advantages and disadvantages of some resonant structures are considered when the ideal active switch is either a bipolar junction transistor (BJT), a power MOSFET, or an insulated gate bipolar transistor (IGBT). Practical examples of power semiconductor choices in these resonant topologies are given.

1. INTRODUCTION

The main advantage of resonant structures is the reduction of switching losses, and also less stress on the electronic switch occurs compared with PWM structures.
These two advantages (lower switching losses, less device stress) are generally paid for in terms of higher conduction losses.
The purpose of this paper is to present the elements that permit the most suitable choice of power semiconductor to be made in some types of resonant structures.

2. RESONANT SWITCH

The resonant switch represents the basic element of converters with resonance or quasi resonance. It consists of semiconductors and LC resonant elements. Depending on the configuration of the resonant elements one can obtain the structures of fig. 2 [1,2]
A family of quasi resonant converters (QRC) is obtained by simply replacing the conventional chopper power switch with a resonant switch as shown in fig. 3.
In each case there is controlled switching either at turn-on in the ZCS or at turn-off in the ZVS.

3. ZERO-CURRENT AND ZERO-VOLTAGE SWITCHED QUASI-RESONANT CONVERTERS (ZCS-QRC and ZVS-QRC)

3.1 ZCS-QRC

This configuration permits the switch to be controlled at turn-on, while the turn-off occurs with zero current. The switched current, I_s is a quasi-sine-wave and is reduced to zero at turn-off.
Switching losses are due to:
1) turn-on switching (although these losses are much lower in comparison to the PWM converter),
2) internal discharge of the power semiconductor output capacitance C_{oss} at turn-on (see waveforms fig.4)[7]
3) rectifier diode switch-off.

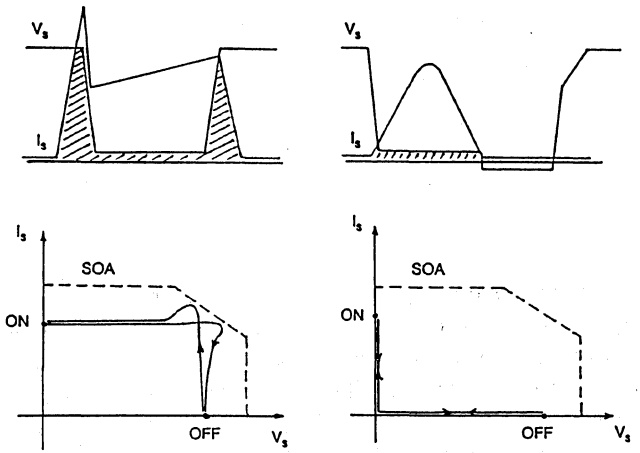
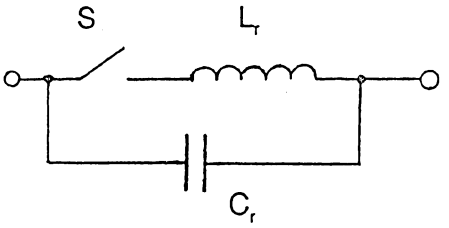


Fig. 1 Hard switching Soft switching



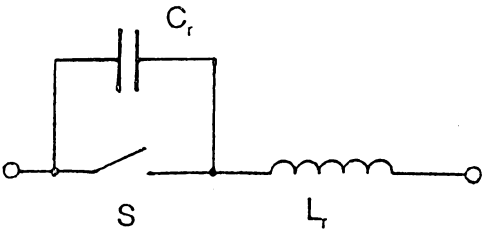


Fig.2 ZC-QR switch (thyristor) ZV-QR switch (Dual thyristor)

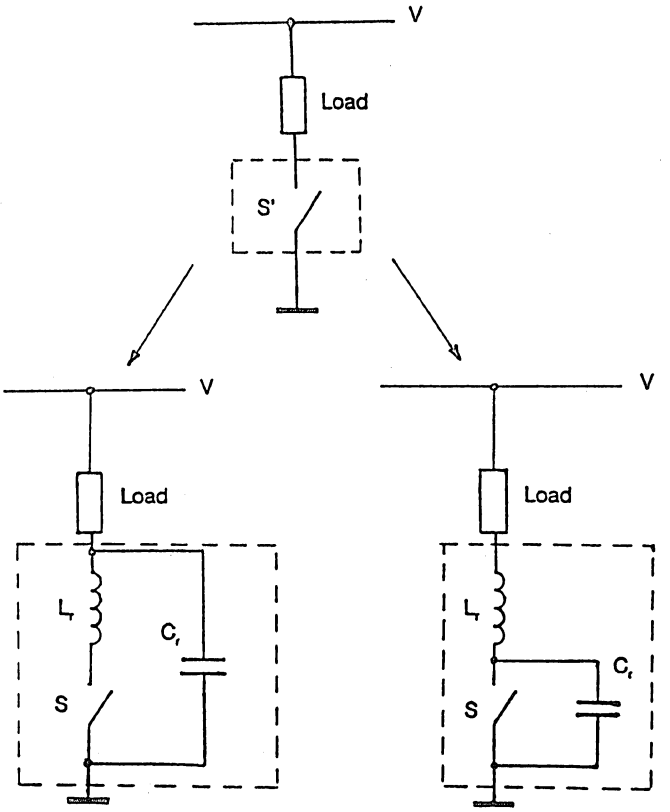


Fig. 3 ZCS-QRC ZVS-QRC

3.2 ZVS-QRC

This configuration permits the switch turn-off to be controlled; the turn-on occurs with zero voltage (the capacitive turn-on problem of ZCS-QRC is eliminated). This operating mode is called "dual thyristor" because the switching properties follow the duality rules of the thyristor, i.e. spontaneous turn-on at zero voltage and controlled turn-off [Ref.1].
The voltage across the switching device is quasi sine wave and is reduced to zero at turn-on. The only switching losses occur at turn-off as shown in the waveforms of fig.5.

4. WHICH SWITCH?

We are interested in analysing the behaviour of the two quasi resonant (QR) topologies when the active switch, S, is a BJT, a Power MOSFET or an IGBT.
Table 1 shows the main features of each power semiconductor (V > 400V).
Because the cost of a power semiconductor varies with the chip-size the curve of fig.6 gives a cost analysis.

4.1 THE PHYSICAL LIMIT OF A POWER BIPOLAR TRANSISTOR.

The presence of storage time, t_s, limits the maximum frequency of operation. Extra losses are due to the presence of $V_{CEsat(dyn)}$ at turn-on.

4.1.1 A BIPOLAR JUNCTION TRANSISTOR IN ZCS.

The storage time, t_s, limits the duration of t_d between the time that the current is zero and the re-applied voltage (t_d is in the order of t_s). The transistor voltage does not reach zero instantaneously at turn-on ($V_{CEsat(dyn)}$). This phenomenon could increase the conduction losses for a short time.

4.1.2 A BIPOLAR JUNCTION TRANSISTOR IN ZVS.

The storage time, t_s, limits the maximum frequency of operation of the converter.

4.2 THE PHYSICAL LIMIT OF A POWER MOSFET.

If there are no economic limits the Power MOSFET is almost a perfect component for many applications, but has two real limitations:
a) internal capacitance;
b) the presence of the body drain diode. This diode is:
b.1) a good diode during its turn-on behaviour (very low peak voltage)
b.2) a poor diode during turn-off.

4.2.1. A Power MOSFET in ZCS

The Power MOSFET is not adapted well to ZCS operation because the body drain diode is subjected to very hard stress due to the recovery phenomenon.
The only solution when using a Power MOSFET in the ZCS mode at high frequency (> 20kHz) is to add a fast diode (D2) and a Schottky diode (D1) as shown in fig.8
The maximum frequency will be limited by the losses due to the Power MOSFET internal capacitance.

4.2.2. A Power MOSFET in ZVS.

In this type of operation, as in the "dual thyristor" operation, the body drain diode is not subjected to stress after it's current becomes zero.
In addition, the turn-on occurs at zero voltage and consequently the energy stored in the parasitic MOS capacitance is not lost. The nature of a Power MOSFET makes it very suitable for ZVS operation.

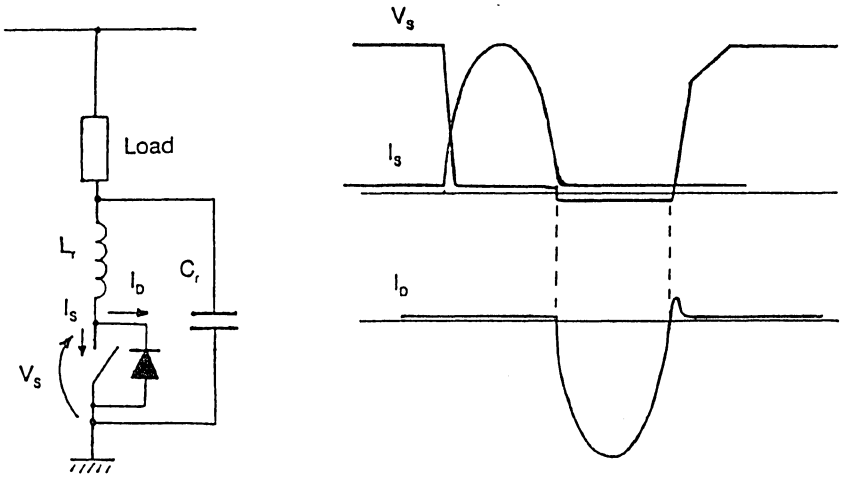


Fig. 4 ZCS-QRC (with bidirectional current switch) and corresponding waveforms.

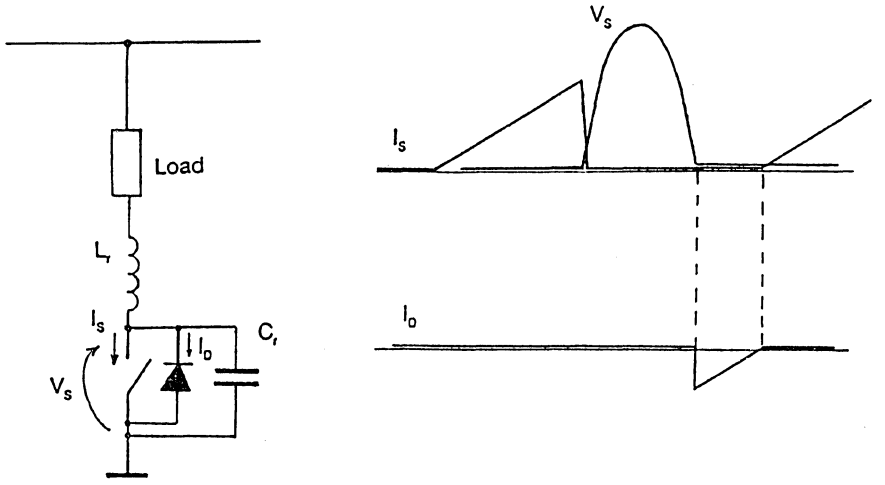
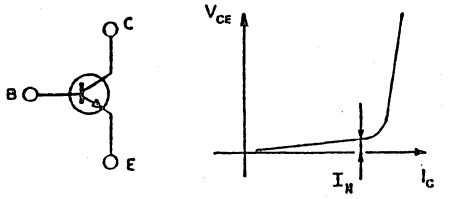
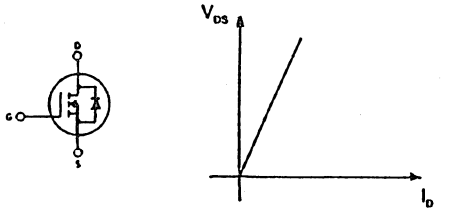


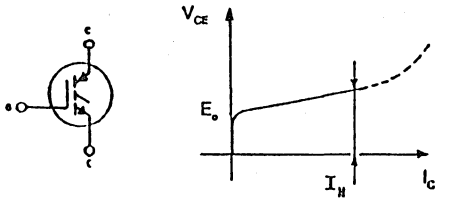
Fig. 5 ZVS-QRC (with unidirectional voltage switch) and corresponding waveforms.



ADVANTAGES	DISADVANTAGES
- Very low on-state voltage drop - Reduced silicon area - Low cost	- Cost of base drive - Storage time (t_s)



ADVANTAGES	DISADVANTAGES
- Low voltage drop is obtained with large silicon area - Cheap gate drive - Reduced turn-off delay time - Anti-parallel body-drain diode can be used	- Cost - In some cases dangerous to use body drain diode



ADVANTAGES	DISADVANTAGES
- Low voltage drop at high current density - Cheap gate drive	- Presence of threshold voltage E_o - Current tail effect at turn off

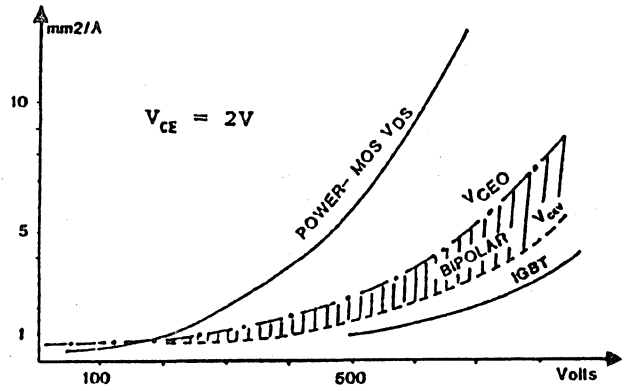
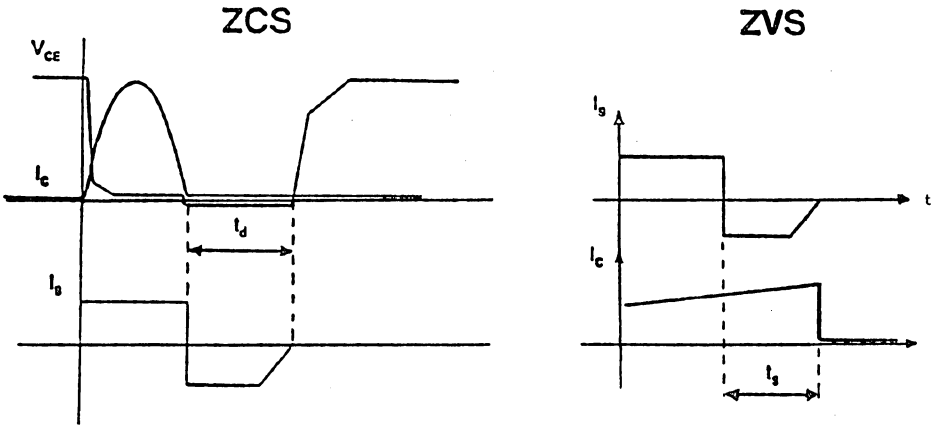


Fig. 6 Chip surface vs maximum rated voltage



- Presence of a dead time t_d which limits f_{max} (t_d is in the order of ts and depends on the base drive circuit)
- $V_{CEsat\ (dyn)}$

- The storage time (t_d) limits f_{max}

Fig. 7 - The physical limit of Power Bipolar Transistors in quasi resonant circuits.

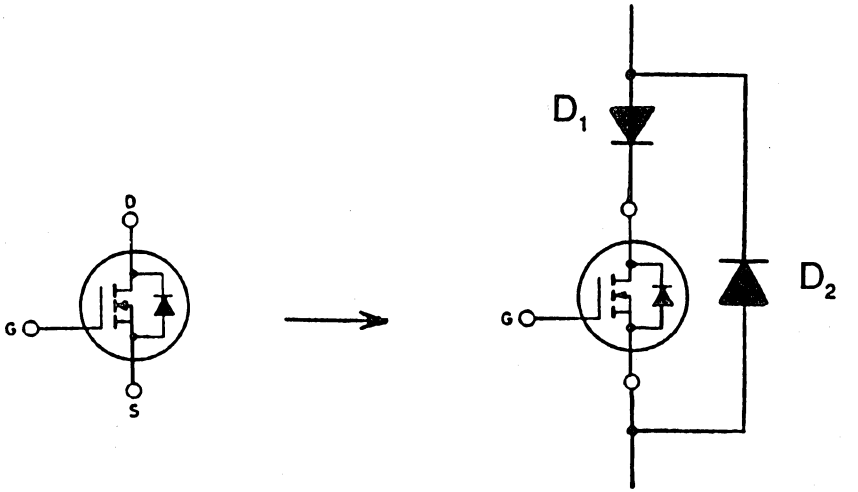
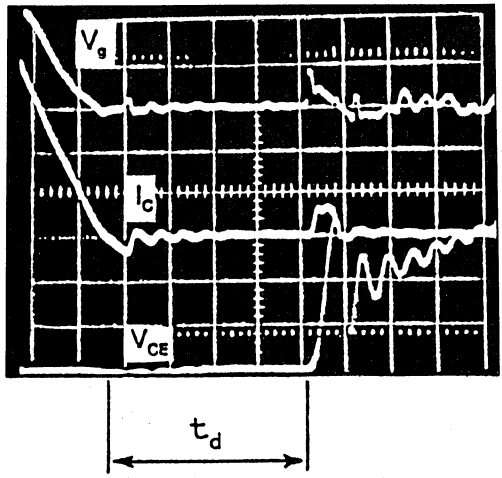


Fig.8 Disabling a Power MOS body drain diode



- t = 0.2 ms/div.
- V_{CE} = 100V/div.
- I_c = 5A/div.
- V_g = 5A/div.
- T_c = 50°C
- dV/dT = 400V/ms

Fig. 9 IGBT behaviour during turn-off in ZCS mode. The waiting time, t_d, is not enough and a current peak, bigger than that due to the capacitive effect, appears due to the effect of the re-applied voltage.

4.3 THE PHYSICAL LIMIT OF AN IGBT.

The IGBT has an economic advantage in comparison to the Power MOSFET (smaller silicon area for the same voltage drop), but its turn-off is influenced by the bipolar transistor section. At turn-off, the minority carriers which remain in the base-collector junction of the bipolar section increase the turn-off losses (current tail effect). If the IGBT turn-off is controlled by only acting on the gate, it is necessary to wait for a time, t_d, before re-applying the voltage, otherwise extra losses generated may make the device fail due to thermal run-away. This time, t_d, must be longer than the duration of the current tail effect (in the order of 3-4µs for a 1000V IGBT)[8].

4.3.1 AN IGBT IN ZCS.

The frequency is limited by t_d, consequently the IGBT in ZCS can attain a relatively high frequency (around 120kHz). The losses due to the internal IGBT capacitance in this frequency range are smaller than Power MOSFET losses. In fact, for a given current rating the IGBT capacitance is much smaller than the Power MOSFET capacitance. The only other limitations are the conduction losses.

4.3.2 AN IGBT IN ZVS.

The main limitation of the IGBT in this configuration is the high switching losses due to the current tail effect. A larger value capacitor, Cr, acting as a snubber, reduces dV/dt at turn-off and, consequently, turn-off losses [5].

SUMMARY OF THE PHYSICAL LIMITS OF SEMICONDUCTORS

TABLE II

BJT	- Storage time —> frequency limitation - $V_{CEsat(on)}$ —> turn-on losses	- Storage time —> frequency limitation
Power MOSFET	- Recovery of body drain diode - Capacitive turn-on losses at high frequency - Conduction losses	- High voltage
IGBT	- Deadtime —> frequency limitation - $V_{on\text{-}state}$ —> conduction losses	- Turn-off tail problems

5. TWO PRACTICAL EXAMPLES.

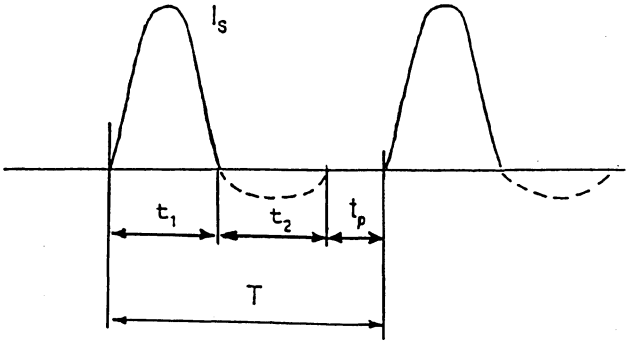
5.1 The first example we are going to consider is a single-switch ZCS-QRC with the following characteristics:
1.5kW - 50kHz - 220V mains.
The switch current waveform will be characterized by:

$t_1/T = 0.4$

$I_{AVG} = 5A$

$I_{peak} = 20A$

$I_{RMS} = 9A$



Because the time $t_2 < t_1 = 8\mu s$ (conduction time of the antiparallel diode), this time is large enough if compared with the fall-time, t_f of an IGBT (< 1μs) or the storage time, t_s, of a bipolar transistor (1-3μs) there are no problems in using these semiconductors.

ANALYSIS OF DIFFERENT POWER SEMICONDUCTORS

(Devices selected with similar current rating)

BUF420 450/850V - 20A ETD Bipolar Junction Transistor) [54 square mm. silicon area]. Conduction losses calculation gives P_{cond} = 8.1W.

TSD4M451 (450V/$R_{DS(on)}$ = 0.15 Ohms at 100°C ISOFET) [176 square mm. silicon area] To obtain conduction losses comparable to BJT losses, it is necessary to choose a large silicon area Power MOSFET (P_{cond} =12.1W). The main disadvantages are:
1) turn-on capacitive losses 5.5W at 50 kHz due to the big chip-size (176 square mm total silicon area)
2) extra conduction losses (3W) due to the use of a power Schottky diode

STGH20N50 IGBT 500V/20A) [32 square mm. silicon area] conduction losses calculation [5] gives P_{cond} = 12W.

STGP10N50 (IGBT 500V/10) [16 square mm. silicon area]. Due to its over current capability a 10A/500V IGBT can be used in this application. Conduction losses calculation [5] gives P_{cond} = 18.6W.

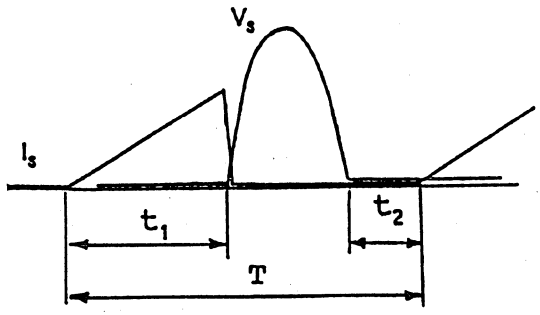
CONCLUSION: IGBTs and BJTs are concurrent solutions. IGBT advantages are:
1) gate drive simplicity
2) saving in silicon area.

BJT advantage is due to the optimum ratio of conduction losses to device cost. However the storage time limits the BJT frequency operation to no more than 70kHz.

5.2 The second example we are going to consider is a single - switch ZVS-QRC with the following characteristics:

$(t_1+t_2)/T$ = 0.6
I_{AVG} = 2A
I_{peak} = 10A
I_{RMS} = 3.65A
$V_{s(peak)}$ = 750V (max.)

300W - 150kHz - 110V mains (± 20%). The switch current waveform will be characterized by:



ANALYSIS OF DIFFERENT POWER SEMICONDUCTORS.

(Devices selected with similar current rating)

BUF410 (450/850V - 10A ETD bipolar junction transistor). The storage time t_s (1 - 3µs) is comparable with $t_1 + t_2$ = 4µs. The use of a BJT at this frequency of operation is not possible. For the ETD BJT technology an upper frequency of operation is around 100kHz.

STH9N80 (800V/$R_{DS(on)}$ = 1.5 Ohms at 100°C Power MOSFET). Conduction loss calculations give P_{cond} = 20W. Turn-off losses are negligible. The Power MOSFET body drain diode is not subjected to any stress and can be used as an anti-parallel diode.

STGH8N100 (1000V/8A IGBT). At I_{switch} = 10A and dV/dt = 1000V/µs the IGBT turn-off losses can be evaluated at around 0.6-0.7mJ/Hz. It means roughly 105W at 150kHz only for turn-off losses. Conduction loss evaluations give P_{cond} = 4.6W.

CONCLUSION: For this single-switch application, the Power MOSFET is the most suitable choice.

At the given frequency of operation and duty cycle one obtains: $t_1 + t_2$ = 4 µs

SUMMARY OF EXAMPLES

The physical limit of the semiconductors examined and the examples taken into consideration show that in a single switch QRC a correct choice of the switch is the following:

IF

ZCS - QRC:

Bipolar Junction Transistor (f < 70kHz)

Power MOS (f < 20kHz).

Higher frequency of operation could be obtained disabling internal body drain diode or using a FREDFET.

IGBT (f < 120 kHz)

IF

ZVS - QRC:

Bipolar Junction Transistor (f < 100kHz)

(f = 0.5 to 1MHz)

IGBT (f < 20 - 30kHz)

Power MOSFET (0.5 MHz -1MHz)

CONCLUSION

Each power semiconductor we took into consideration shows physical characteristics that limit its operation in single switch quasi resonant converters.

In particular the bipolar solution is acceptable for both QRC topologies at frequencies lower than 100kHz. The power MOSFET solution is disadvantageous in applications at high

RMS currents such as those in discontinuous ZCS-QRC. Despite this, power MOSFETs are most suited to the ZVS-QRC due to their fast switching times and the possibility of using the body drain diode even with their inferior performance.

The IGBT solution is today the most popular for resonant and quasi resonant applications. However in ZCS-QRC where its use seemed to permit very high working frequencies, the dynamic dV/dt phenomenon may lead the device to fail due to thermal runaway. This can be overcome by careful design and the use of an efficient heatsink.

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AN ANALYSIS OF LOSSES IN AN IGBT

by P. Fichera

1. INTRODUCTION

Insulated gate bipolar transistors are now being used in a variety of switching applications. These range from automotive ignition, where they replace the mechanical contact breaker, to electric motor drives, where they provide an economic, easy to drive chopper switch with high voltage capability.

More recently work has been done in using these devices in various types of power supplies.

They are attractive to use due to the high impedance input, a MOS gate that requires a mimimum of only 8V and microjoules of energy to turn it on and off and the bipolar nature of the output that makes them capable of controlling high current densities.

To obtain the optimum performance from IGBTs it is necessary to understand the limits imposed by the structure of the device and their particular operating conditions.

This paper looks at the use of IGBTs in chopper circuits and shows how to evaluate the losses during switching and conduction.

2. LIMITING FACTORS FOR IGBTS IN CHOPPER CIRCUITS

Chopper circuits operate at frequencies determined by the nature of the application and of the power switch employed to control the current flow. As is the case with Power MOSFETs, power is dissipated in IGBTs at turn-on of the device, during conduction and at turn-off. The major difference between IGBT and Power MOSFET switching losses occurs in the turn-off switching behaviour. Figure 1 illustrates the typical losses for an IGBT used in a chopper application.

2.1 TURN-ON LOSSES

It is not sufficient to know the rise time, tr, of the turn-on current. The free-wheeling diode used in conjunction with the IGBT, figure 8, is responsible for a large amount of the losses as a result of its reverse recovery current. Within a given application it is necessary to know the $(dI_D/dt)_{on}$ for this diode in order to evaluate the reverse recovery current, I_{RM}. Once I_{RM} is known it is possible to calculate the turn-on losses.

2.2 CONDUCTION LOSSES

The following simple expression shows how to calculate the conduction losses.

$$P_{on} = E_o I_{AVG} + R_o I^2_{RMS}$$

where:

P_{on} = on-state power dissipation

I_{RMS} = RMS current value for the application

I_{AVG} = average current value of the application

E_o,R_o = are parameters defined by the IGBT output characteristic I_c, V_{ce} - see figure 2.

E_o = abscissa of the intersection between the tangent to the output characteristic calculated at $I_c = I_o$ and the V_{ce} axis.

R_o = inverse slope of the tangent to the output characteristic curve I_C, V_{CE}, calculated at $I_c = I_o$.

The area B in figure 1 illustrates these losses.

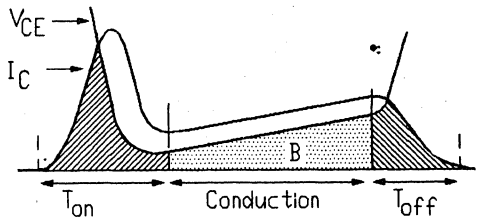


Fig. 1 - Typical IGBT losses

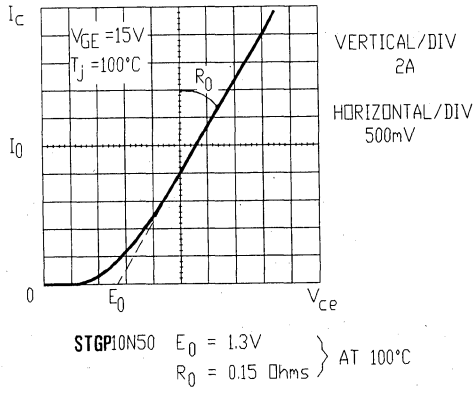


Fig. 2 - Output characteristics of STGP10N50

2.3 TURN-OFF LOSSES

Calculation of the turn-off losses in an IGBT requires more information than just the fall time, t_f. On its own it leads to erroneous results. It is necessary to know how other parameters influence these losses.
Most care has to be taken with the current tail phenomenon of the IGBT when it is operated in hard switching. Two parameters define the current tail: its amplitude, I_t, and its duration, t_t.

A) THE INFLUENCE OF THE SUPPLY VOLTAGE ON TURN-OFF LOSSES.

The supply voltage and the current tail amplitude are directly proportional. However, the duration of the tail remains almost constant when the supply voltage is varied.

B) THE INFLUENCE OF DV/DT ON THE TURN-OFF LOSSES

A low dV/dt value at turn-off (imposed by an external circuit, e.g. a snubber) reduces the current tail amplitude, I_t. The tail duration does not change when dV/dt is varied.

C) THE INFLUENCE OF TEMPERATURE ON TURN- OFF LOSSES.

Operating temperature affects the duration and amplitude of I_t and t_t. Experimental analysis shows that both increase in value by the same percentage as the temperature increases.

D) THE INFLUENCE OF THE GATE RESISTANCE, $R_{g(off)}$.

The gate resistance does not affect the current tail. Varying $R_{g(off)}$ controls the slope of dV/dt at turn off and consequently can give some reduction in the turn-off losses. A minimum value of $R_{g(off)}$ is required to prevent oscillations occuring during turn-off (as is the case with power MOSFETs).

5 CALCULATING CONDUCTION LOSSES

When calculating conduction losses at 100°C it is better to base the calculation on the output characteristics of the IGBT (I_c versus V_{ce}) at a given V_{ge}.

Table 1. *Additional parameters required to calculate turn-off losses in IGBTs.*

V	- the re-applied supply voltage
dV/dt	- slope of re-applied supply voltage
T_j	- junction temperature
$R_{g(off)}$	- gate resistance at turn off.

3. SAMPLE CALCULATIONS.

It is possible, using the curves given in figure 9 and the energy curves characteristic of figure 10 for different operating conditions, to calculate the switching losses for a given set of conditions. This in turn allows the maximum operating frequency for the IGBT to be calculated.
The basic circuit in figure 8 shows the configuration used for the STGP10N50 500V, 10A IGBT and its switching waveforms.

3.1 CALCULATION OF THE TURN-ON LOSSES AT T_j = 100°C.

The value of the gate resistor during turn-on is 47 Ohms. Using the graph in figure 9a this gives a value for dI_D/dt_{on} of 100A/µs. As the IGBT controls dI/dt it follows that the recovery current of the free-wheeling diode can be determined from the diode datasheet (graph of I_{RM} versus dI/dt is shown in figure 9b). This gives a value of I_{RM} = 10A.
Applying the formula for the turn-on losses:

$$W_{t(on)} = 1/2\ V_{supply}\ (I_O + I_{RM})^2 \cdot 1/(dI/dt)on$$

$W_{t(on)}$ is calculated to be: $W_{t(on)}$ = 0.4mJ

3.2 CALCULATION OF CONDUCTION LOSSES AT T_j = 100°C.

The value of the parameters E_o and R_o have been evaluated from the graph of I_c versus V_{ce} shown in figure 2.

$$E_o = 1.3V$$

$$R_o = 0.15 \text{ Ohms}$$

Taking I_{AVG} to be 3.5A and I_{RMS} as 5.8A, P_{on} can be calculated using the equation from section 2.2

$$P_{on} = 9.6W$$

3.3 CALCULATION OF THE TURN-OFF LOSSES.

A. High dV/dt (2500V/µs)

Using a value for $R_{g(off)}$ = 47Ohms and taking into account the dV/dt curve of figure 10 a; at a switched current of 10A the energy dissipated in turning off is

$$W_{t(off)} = 1.1 \text{ mJ/cycle}$$

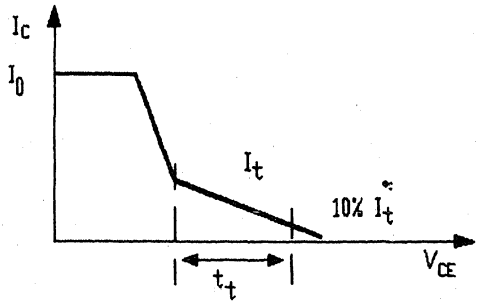


Fig. 3 - Turn-off losses

B. LOW dV/dt (500V/µs)

Using $R_{g(off)}$ = 47 Ohms and switched current of 10A again

$$Wt_{t(off)} = 0.3 \text{ mJ/cycle.}$$

Summarising these values show that the total power dissipated is dependent on the operating frequency.

Accepting that the maximum power that can be dissipated from the device at 100°C is 40 Watts for this device in a TO-220 package, it is simple to calculate that using high dV/dt the IGBT has an upper limit of operation of 20kHz while with low dV/dt operation is possible up to 40kHz.

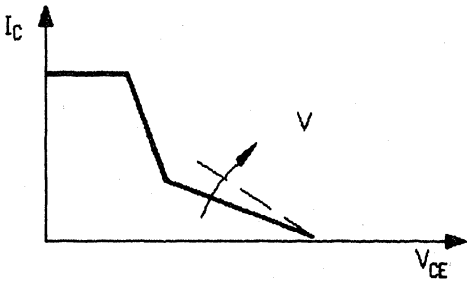


Fig. 4 - Influence of supply voltage on turn-off losses

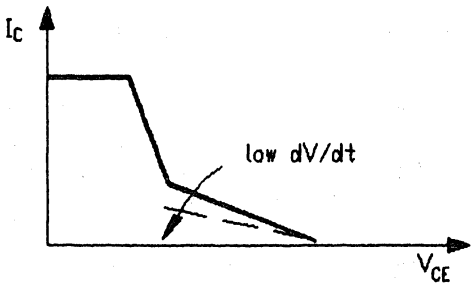


Fig. 5 - Dv/dt effect

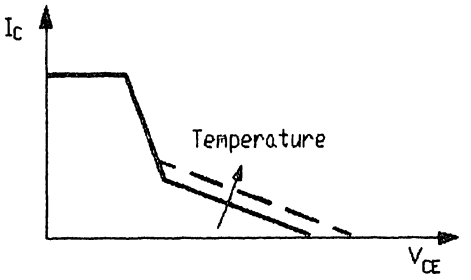


Fig. 6 - The effect of temperature on I_t and t_t

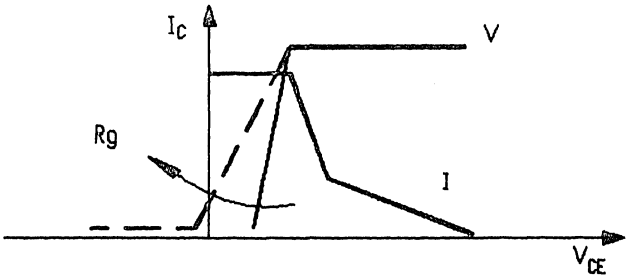


Fig. 7 - The influence of gate resistance

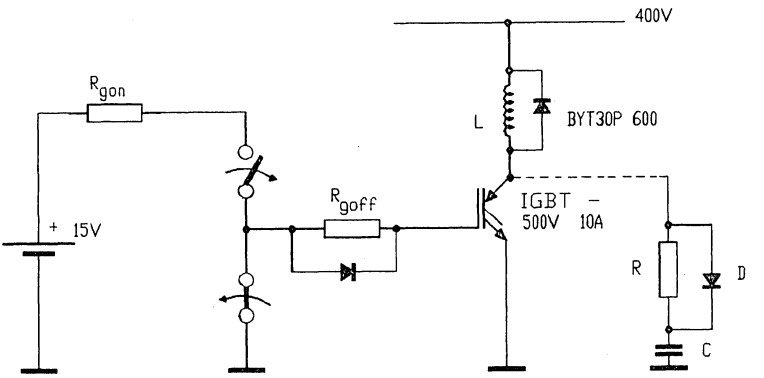
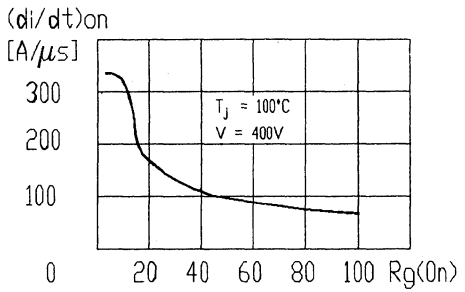
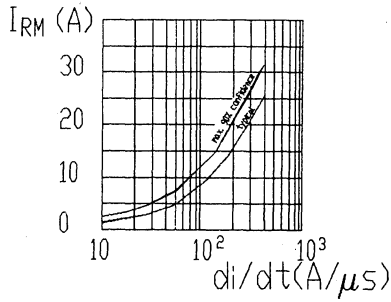


Fig. 8 - Basic circuit

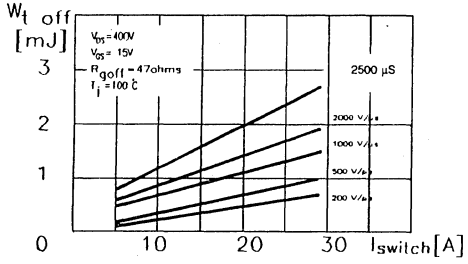


9a

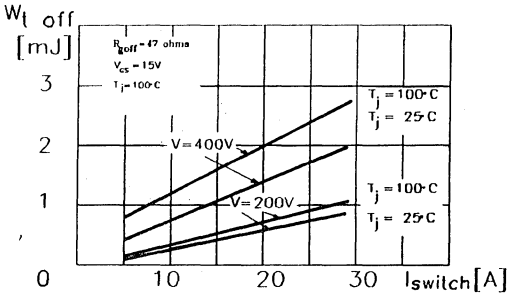


9b

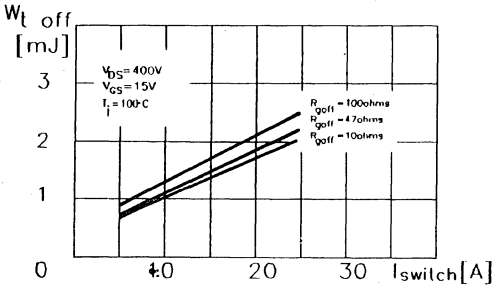
Fig. 9



(a) influence of dv/dt



(b) influence of T_j and V supply



(c) influence of Rgoff, gate resistance at turn-off

Fig. 10 (a,b,c) - Controlling factors for turn-off losses in a "2nd generation"500V/10A IGBT

	Wt(on)+Wt(off)	P(on)	Total Power Dissipated
High dV/dt	1.5mJ/cycle	9.6W	$1.5 \cdot 10^{-3} \cdot$ frequency + 9.6W
Low dV/dt	0.7mJ/cycle	9.6W	$0.7 \cdot 10^{-3} \cdot$ frequency + 9.6W

4. CONCLUSION

IGBTs are rugged, easy to drive and cost effective switches for high voltage chopper applications. They are capable of sustaining high current densities. Their operating frequency has been shown to be dependent on the operating conditions and a straight forward method of estimating this was discussed.

For applications such as motor drives they are robust and reliable alternatives to bipolar transistors and Power MOSFETs.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

A NEW ISOLATED GATE DRIVE for Power MOSFETs and IGBTs

by JM. Bourgeois

INTRODUCTION

Isolated power switches are very often used for applications in motor drives, uninterruptible power supplies, and AC switches. It allows the safety norms to be met and provides the operating isolation required when the switch is floating with respect to ground. Today, the isolated base drive design of bipolar power transistors is well understood (see bibliography), whilst those for Power MOSFET designs are less well known and are still improving. This paper highlights and uses the specific behaviour of a Power MOSFET, and area often neglected: the gate drive described capitalises on the opportunity to use the gate input capacitor as an no-state memory. Driving a transistor requires supplying signals and energy. If switch isolation is needed, optical links and /or transformers are used according to the specified norms and operating dV/dt. This paper proposes an innovative isolated gate drive using the memory effect of the Power MOSFET input capacitor and an associated pulse transformer that provides both signal and energy to this capacitor.

GENERAL CHARACTERISTICS OF A POWER MOSFET ISOLATED DRIVER

Safety norms impose a minimum creepage distance and clearance as well as insulation resistance between control circuit and power switches. These isolation requirements have to be respected by any opto-coupler, pulse transformer or auxiliary power supplies. Electrically, its power switches often float above ground and any isolation must withstand a dV/dt above 20V/nsec. Because a high dV/dt induces a large Miller effect, a low gate drive impedance has to be used during the off-state to avoid any spurious unwanted turn-on of the power switch. As these switches are generally used in PWM circuits, the minimum ON or OFF time must be as low as possible, so enabling a large duty cycle range to be available. Short circuit detection that, via the control circuit, ensures safe operation.

THE NEW CONCEPT

The basic principle consists in using the Power MOSFET input Capacitor to memorize its ON-state, another auxiliary MOSFET to memorise the OFF-state and give a low gate drive impedance. Isolation is provided by a pulse transformer which charges or discharges the transistor input capacitance. The pulse transformer is used as a bi-directional energy/signal channel as follows:

- During the primary pulse, energy is transmitted and the state of the Power MOSFET gate is defined.
- After primary pulse and during the steady state, an alarm signal is transmitted from secondary to primary if a short circuit occurs in the power circuit.

The main advantages of this isolated gate drive are:

A High Operating Frequency Range: This driver is able to operate from d.c. to several hundreds of kiloHertz because the transformer delivers very short pulses:

- Continuous ON and OFF states are possible when automatic refresh pulses at about 1 kHz are used.
- High frequency operation is possible because pulse time and delay time are less than 1 msec.

Duty cycle is not limited. For the same reasons as in 3.1, the duty cycle range is large: the minimum ON time or OFF time is about 500nsec enabling the duty cycle to range from 0.01 to 0.99 at 20kHz.

No floating auxiliary supply: All the switch driving energy is supplied by the pulses from the transformer, the driver does not require an auxiliary power supply.

Low energy requirement. The energy supplied by the pulse transformer is, on averange, twice the gate capacitor stored energy. The global driver energy consumption is very small, hence the cost of the gate drive voltage supply is low.

Good ground-to-gate drive isolation: Because the pulse transformer provides the isolation, the creepage distance and clearance are easily adjusted to suit the requirements of the application.

Perfect dV/dt immunity: The pulse transformer is sized so as to sustain 15 Volts for 500 nsec. This can be achieved by using a small ferrite torroid with

just a few turns. The primary-secondary electrostatic coupling effects are negligible and the immunity to voltage fluctuations is perfect. An additional benefit is that a torroid of less than 10mm external diameter can be used - possibly a surface mounting version.

Low Gate Drive output impedance during OFF state: During the OFF-state, a low impedance is maintained across the gate-source of the Power MOSFET which avoids any unwanted turn on should any external dV/dt be experienced.

Short circuit protection: The secondary circuit has an automatic short circuit protection; this protection is inhibited during turn-on pulses in order to mask the diode recovery current of the power circuit. It can operate with current sensing or a shunt resistor.

Alarm signal: When the short circuit protection operates, it discharges the Power MOSFET input capacitor through the pulse transformer. Then, it operates in reverse mode and transmits an alarm signal from the secondary to primary of the pulse transformer.

FUNCTIONAL DESCRIPTION

Figure 1 shows a block diagram of the circuit. It is made up of a primary pulse generator, a pulse transformer and an isolated secondary circuit operating without any auxiliary supply.

Secondary Circuit : Figures 2a to 2e allow a step by step analysis of the secondary circuit to be made as follows.

Turn ON pulse: Figure 2a shows the charge current, I_1, of the Power MOSFET T_p input capacitor when a positive pulse is applied to the pulse transformer primary. The gate voltage, V_g, rises to V_1, depending on the resistance R_C. When the primary pulse disappears, V_1 is about zero and the diode D prevents C_g from being discharged. The Power MOSFET keeps its gate charge and remains in the conducting state.

Turn OFF pulse: Figure 2b shows the Power MOSFET input capacitor discharge current, I_3, through R_d and T_d. The discharge occurs when the capacitor, C_m, is charged through D_2 by means of circuit W biased by V_2. Zener diode, D_z, is required to limit the gate-source voltage of T_d at the beginning of the negative pulse, V_2. Details of the circuit W are given in figure 2c.

Figure 1: Block Diagram

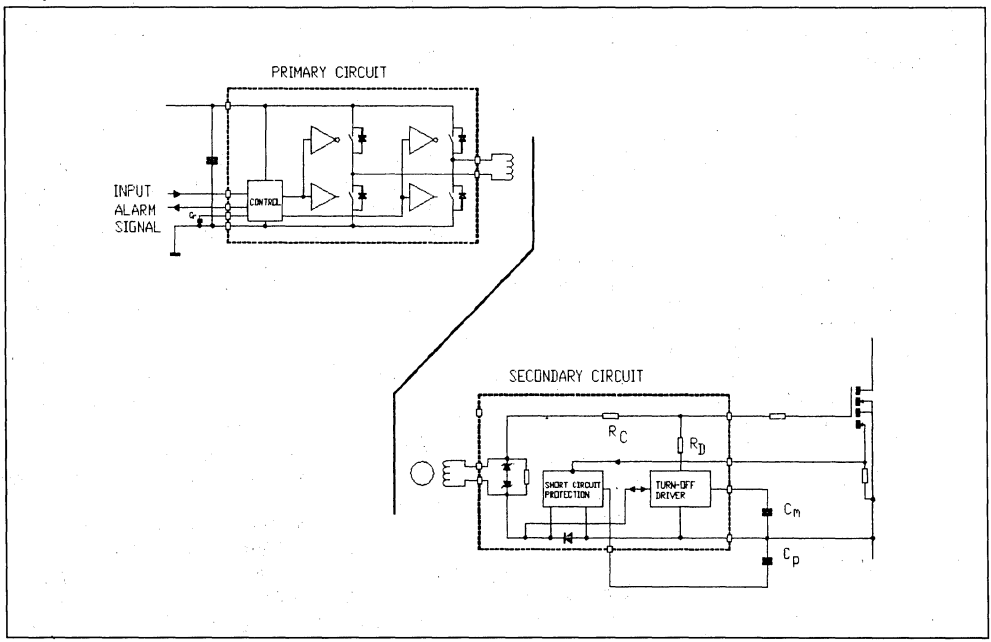


Figure 2a: Charge current for the Power MOSFET, Tp, input capacitor when a positive pulse is applied to the transformer

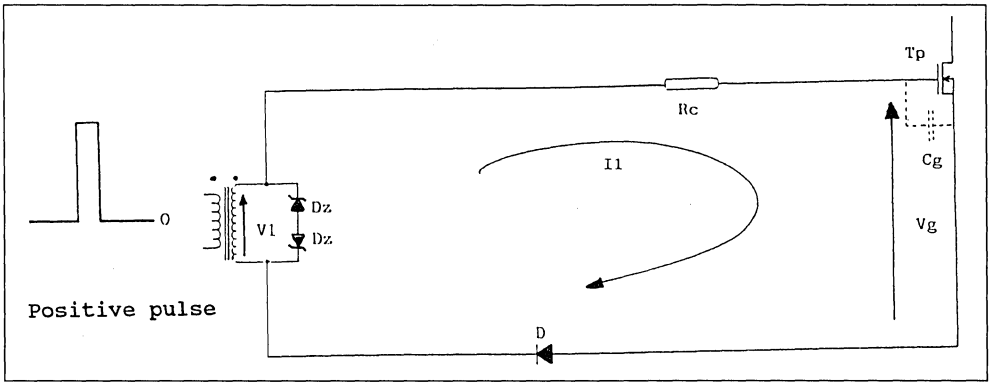
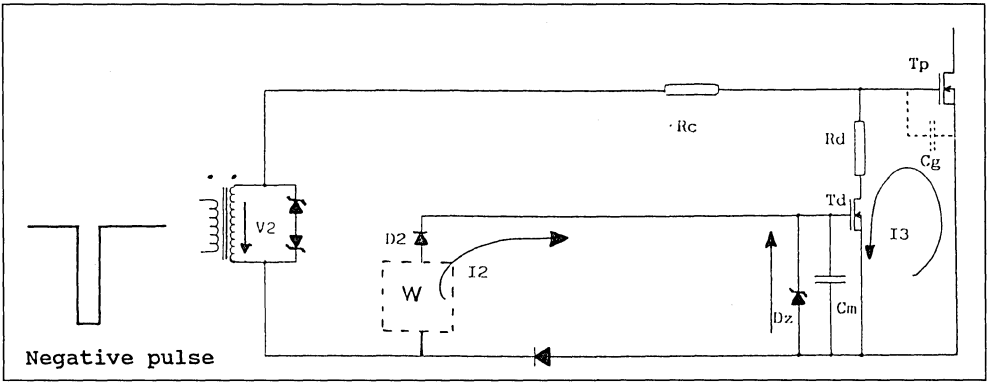


Figure 2b: Power MOSFET, T_p, input capacitor discharge current



Short circuit protection: A short circuit can be detected by means of a shunt resistor, or current sense (see figure 2d and 2e). It induces a rise of V_S which charges C_p which in turn makes T_3 conduct. The power transistor input capacitor is discharged through the pulse transformer and the transistor T_3. It produces a current pulse in the transformer secondary enabling a short circuit to be detected via the primary winding.

Diode recovery current: Generally, power switches have an associated diode recovery current at turn-on. This creates a brief over-current in the switch that requires masking from the short circuit detection circuit during this recovery time.

Due to the Miller effect, the current I_1 lasts for as long as the collector/drain voltage falls. Inhibiting short circuit detection by means of I_1 masks all the diode recovery current.

This function is carried out by T_5 which detects I_1 through R_c and makes T_4 conduct. The current I_5 flows through T_4 instead of charging C_p during the diode recovery time, avoiding spurious cunduction of T_3.

Application: Figure 3 shows the short circuit behaviour of the STHI20N50 (20A/500V IGBT). Note that the short circuit protection acts immediately after a 400nsec delay, that is, after the turn-on pulse.

Primary circuit: The primary circuit can be made by simply using a full bridge with a single primary winding. The primary control sequence is described in Figure 4.

A pair of sense diodes are located at the bottom of the left hand half-bridge; they control the demagnetisation current used to detect the short circuit alarm signal.

Figure 2c: Details of the circuit W from fig. 2b

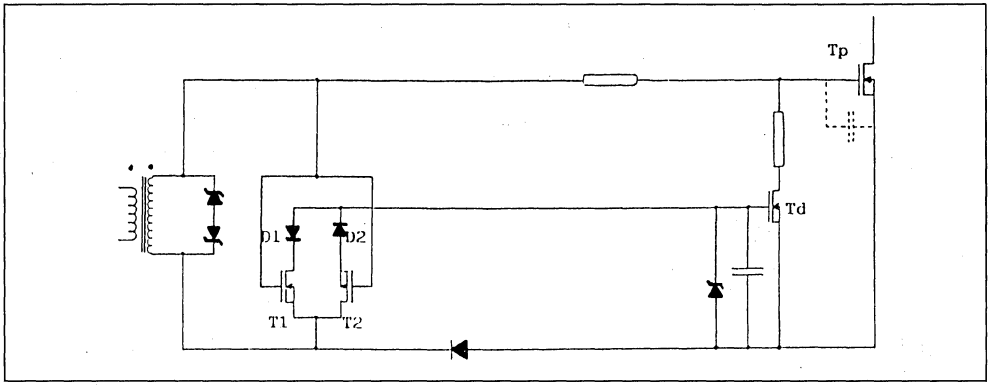


Figure 2d: Over current detection and short circuit protection

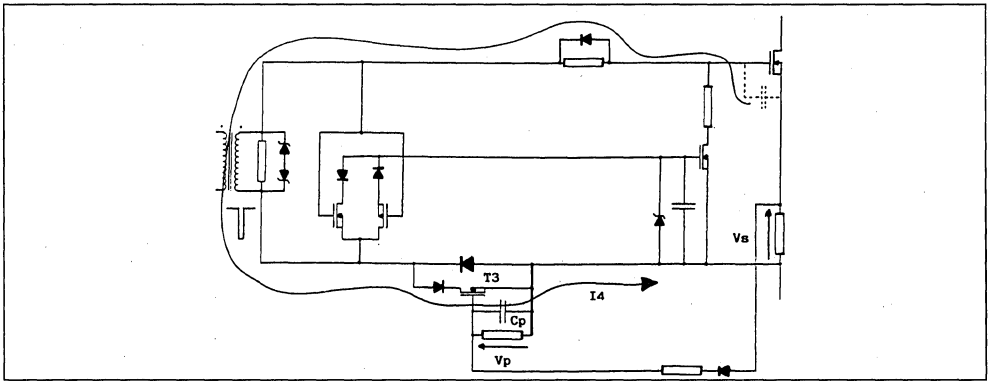


Figure 2e: Protection inhibition during diode recovery current

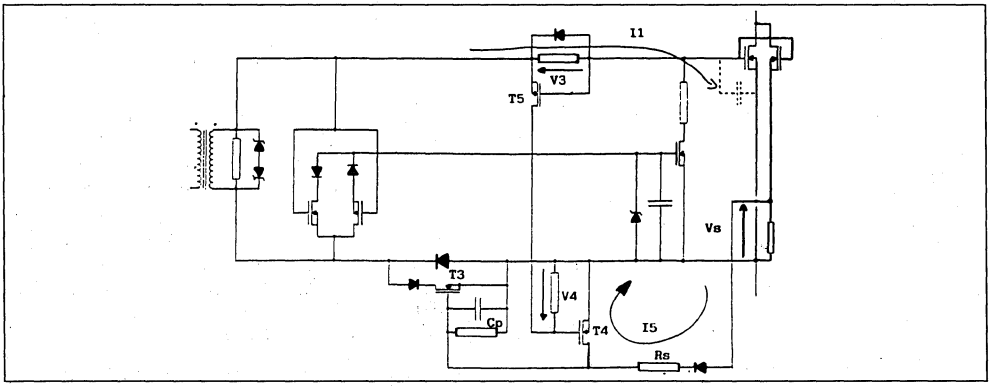


Figure 2a-2e: A step-by-step analysis of the secondary circuit

Figure 3: Short circuit behaviour at turn ON with a 20A/500V IGBT - STHI20N50.

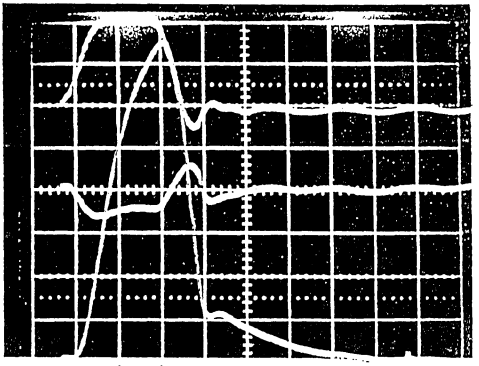


Figure 4: The primary circuit control sequence.

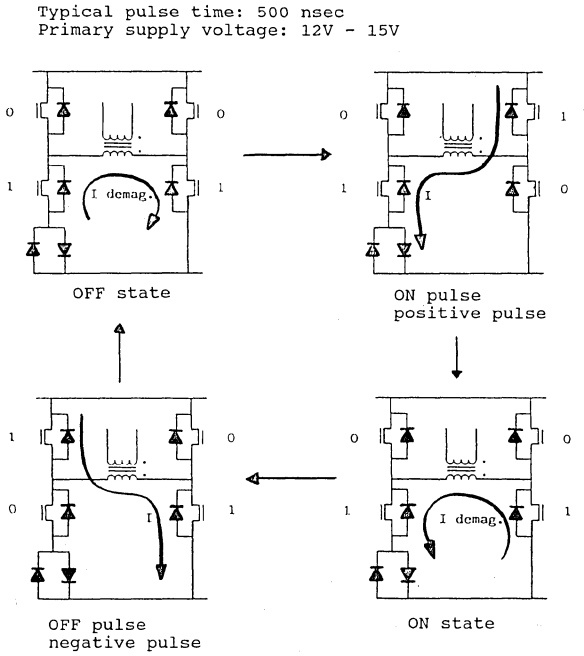


Figure 5 : The primary alarm signal - pulsed controlled driver with memory effect.

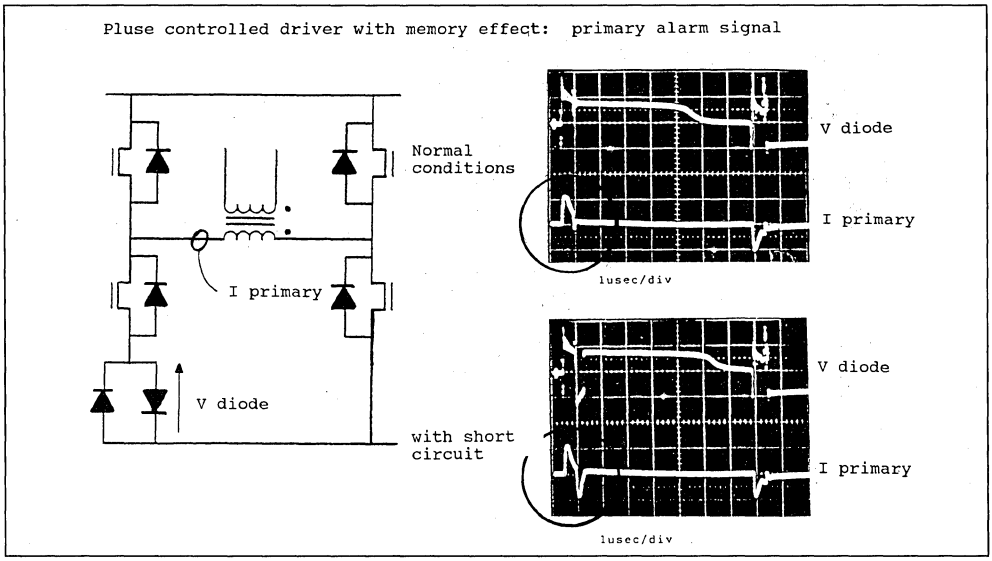


Figure 5 shows the primary circuit behaviour under normal conditions and with the power stage short circuited.

Normal conditions: The positive current pulse corresponds to the turn ON signal and is followed by the demagnetisation current. The negative current pulse is due to the turn OFF signal. It is possible to see that the voltage across the sense diode is always positive during the turn ON pulse and the corresponding demagnetisation.

Short circuit conditions: The waveforms are similar to the previous ones, except for the current after the positive pulse. Due to the discharge of the input capacitor, T_p, through the transformer secondary, a negative current pulse occurs at across the primary at the beginning of the demagnetisation, inverting the voltage across the sense diode. By sampling and latching this voltage 100nsec after the end of the turn-ON pulse, it is simple to provide an alarm signal.

If the alarm signal is not required the integrated circuit L293D, can be used to drive the pulse transformers. This is contains two full bridge drivers enabling it to drive 2 transformers. It makes an excellent interface between a digital control circuit and the two pulse transformers of an isolated bridge leg.

CONCLUSION

This new concept for a Power MOSFET driver is perfectly suited to drive floating and/or isolated switches. Moreover, it also provides important cost reduction compared to standard solutions.

Its operating mode permits a large duty cycle range, requires no floating auxiliary supply, has perfect dV/dt immunity and a short circuit protection feature that provides an alarm signal to the grounded control circuit. Lastly, it is now feasable to make a fully SMD circuit due to the availability of SMD pulse transformers.

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SCRs & TRIACs

THE TRIAC

The TRIAC* is a semi-conductor device with has been specifically designed to operate as a controlled switch in an AC power system.

With the introduction of electronic component into industrial application, the utilization of the Triac as a complement, the utilization of the Triac as a complement to, or replacement for, electromechanical switches or relays and magnetic control systems, has been rapidly expanding in this field. In addition, its availability has led to the development of new control systems which were not feasible with the previously devices.

The advantages of the Triac are its noiseless operation, its ability to be controlled at precise instants and without rebounds, its automati turn-off when the current reaches zero after the control has been removed, and its ability to withstand without wear an unlimited number of operating cycles when used in the conditions specified by the manufacturer.

We shall briefly describe the principle of operation of triacs used as controlled switches, then insist on the precautions required during utilization to maintain high reliability (section 2 and appendix 1) and, finally, give, in Section 3, examples of applications as on-off control switches, static relays and power variations units.

SYMBOLS AND TERMINOLOGY

Half wave: half cycle of the alternating input voltage V_a. The polarity (positive or negative) of each half wave is defined with reference to the potential of the triac electrode A_1.

Full wave: couple of consecutive half waves (one positive, one negative).

Trigger pulse: gate current pulse switching on the triac.

Firing: change to conduction of the triac until the current i_T flowing through it reaches the value I_L enabling it to remain in the conducting state up to the end of the half wave (until i_T has dropped below I_H): see I_H and I_L below.

v_a: instantaneous value of the alternating input voltage (mains voltage, as a generate rule)

V_{RMS}, I_{RMS}: rms values of V_a and of the load current.

V_T, i_T: voltage across the triac in the conduction mode, and current flowing through the triac.

V_M: "breakover voltage": voltage applied, in the static state, between A_2 and A_1 and beyond which the triac is changed to the conduction mode without gate current.

V_{DWM}: minimum guaranteed value of V_M (= peak working forward voltage: see 2.3).

I_G: gate current, or trigger pulse peak value.

I_{GT}: minimum gate current I_G required to switch-on the triac (if permitted by the load conditions: see I_L).

I_H: "holding current": minimum value of i_T required to maintain the triac in the on state (below which the triac turns off).

I_L: "latching current": minimum value of i_T required to hold the triac in the steady conducting state after the triggering pulese has been removed.

I_{TSM}: non-repetitive peak overload current in the conduction mode.

I_{RSM}: repetitive peak overload current in the conduction mode.

$\propto$: "angle of conduction" of the triac ($\propto/\pi$ represents the fraction of each half wave during which power is applied to the load).

φ: load current phase shift with respect to the input voltage v_a.

di/dt: see 2-2

dv/dt, $(dv/dt)_c$, : see 2-3.

* The word "TRIAC" is an acronym for "TRIode for Alterning Current".

1. OPERATION OF THE TRIAC AS A CONTROLLER SWITCH

1.1. STRUCTURE

Like the transistor or the thyristor, the triac consist of alternate layers of p-type (majority carrier = holes) and n-type (majority carriers = electrons) semiconductor material. In the case of the triac, the imbrication of these layers is such, that the device can be compared to a power monolithic integrated circuit. Figure A illustrates a possible arrangement of the p and n regions (scale enlarged in the direction of thickness).

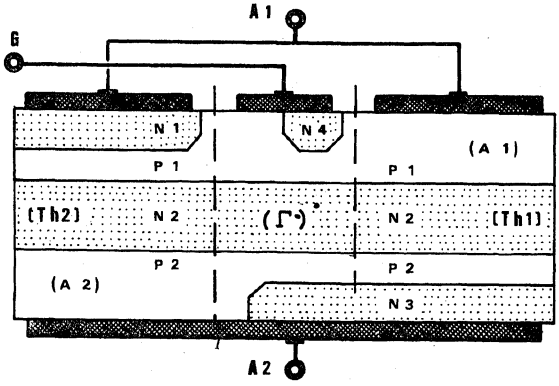
Layers P1 N2 P2 N3 form a thrystor Th 1 whose anode consists of layer P1, and the cathode, of layer N3.

Layers P2 N2 P1 N1 form a thyristor Th 2 with anode A2 on P2, which is, therefore and through the external metal connections, antiparallel connected with Th 1 as regards terminals A2 and A1.

Finally, layers P2 N2 P1 N4 form auxiliary element Γ which couples gate G of the triac with the cathode and anode gates of Th 1 and Th 2 in order to permit triggering of the triac in the various possible polarities of the gate and of electrode A2 with respect to electrode A1. Consequently, the triac can be roughly represented by the equivalent electrical schematic of Figure 1B.

Figure 1 : Structure of a Triac.

A : Example of a triac structure (vertically exaggerated sketch).



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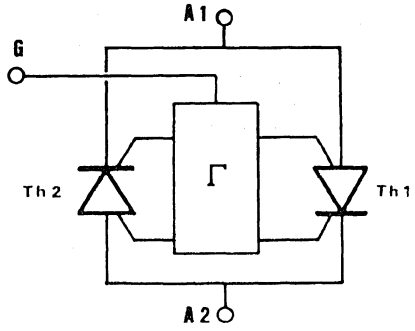
B : Simplified Equivalent Schematic.



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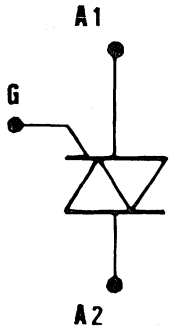
C : Circuit Symbol.



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With no pulse applied to the gate, the current cannot begin to flow spontaneously between A1 and A2. The triac is in the "blocked state".

The application of a current pulse to gate G causes Th1 and Th2 to change to the conducting state (through auxiliary element Γ), in accordance with the polarity of the terminal voltage. Electrode A1 being taken as reference for the potentials, Th1 conducts during negative half waves (A2 negative with respect to A1) while Th2 conducts during positive half waves (A2 positive with respect to A1). The triac is said to be in the "conducting state" (refer to figure 3, P.7). When the gate current pulse is suppressed, for instance during a positive half wave, elementary triac Th2 continues to conduct and, consequently, the triac remains in the conducting state until the current decreases to almost zero, below the holding current of Th2.

1.2. OPEN-GATE STATIC CHARACTERISTICS

The study of the operation in conditions in which the voltages and currents change slowly, as in the case of a 50 or 60 Hz AC supply mains without any superimposed interference, can be carried out by starting from the I/V static characteristics of the triac (plotted point by point or observed with the aid of a curve plotter) V (on the X-axis) is the voltage applied between main terminals A2 and A1, with A1 as reference, and I is the current flowing from A2 to A1 in the triac.
The graph of figure 2 corresponds to the case where the triac is not controlled, i.e. where its gate is open ($I_G = 0$).
When a peak-amplitude alternating-current voltage V_a lower than both V_M in positive half-waves and V'_M in negative half-waves, is applied to A2, current I always remains very low and, in any case, negligible when compared with the nominal operating current. The triac is in the blocking condition.
When the load is a resistor R, its L/V characteristic in this diagram is a straight line of slope 1/R, which moves parallel to itself when the instantaneous value V_a of the supply voltage varies. The operating point moves along section A'A to the points of intersection of the static characteristic of the trias in the blocked state, with the individual load straights corresponding to the various values of V_a.
However, when an overvoltage V_P higher than V_M is temporarily applied to the circuit, the load straight can reach the position indicated by a dotted line, thus moving the operating point to B. Following the removal of the overvoltage, the operating point moves down along section CD of the static characteristic, where voltage V is low and the current high. Thus, this section corresponds to the conditions in which the triac is in the conducting state. It has been "fired" by overvoltage V_P. This hind of firing produces dangerous stresses in the triac and user circuit.

1.3. FIRING THROUGH GATE CURRENT

When a current I_G is caused to flow between gate G and electrode A1, the blocking voltage decreases abruptly when this current reaches a critical value I_G mini.

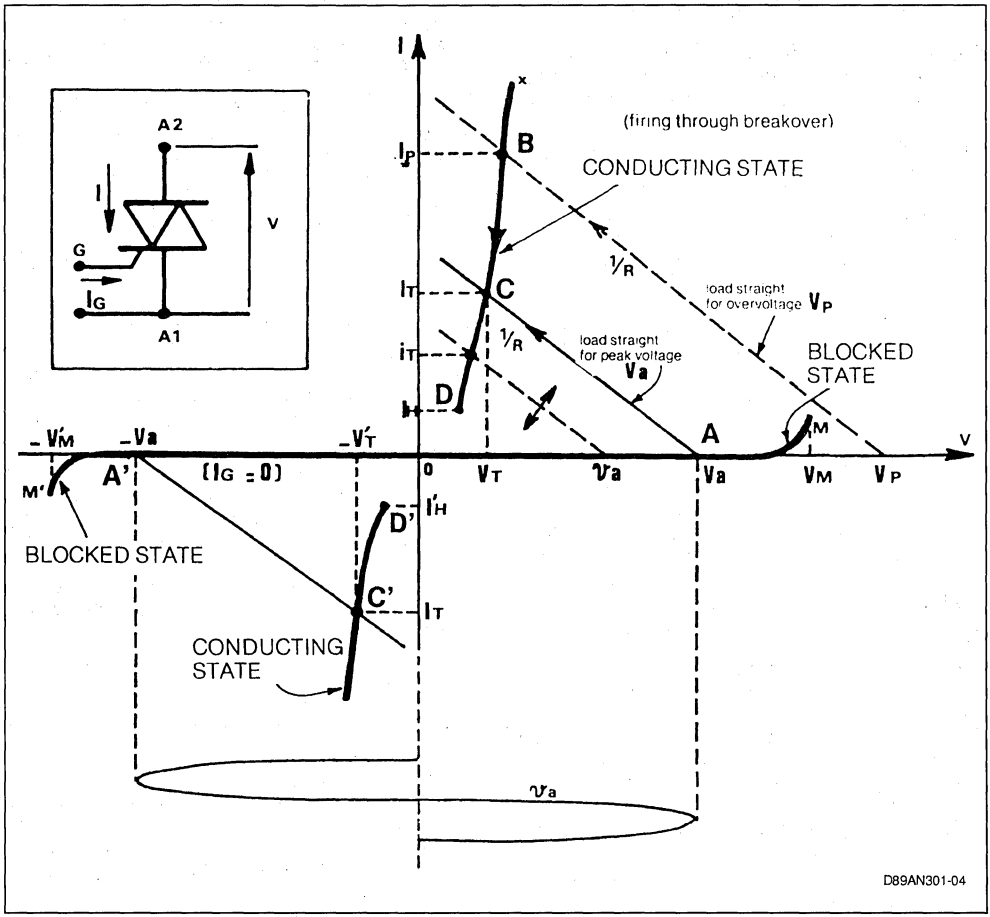
As long as I_G is equal to, or higher than, I_G mini, section MOM' of the characteristic of Figure 2 is replaced by section E'OE of the curve in dotted line (Figure 4), which joins together the "conducting state" characteristics D'x' Dx. Now, when the applied voltage varies from V_a to + V_a, the operating point describes curves C'C of these characteristics. The current varies from I_T to + I_T and the voltage across the triac varies from V_T to + V_T.

This voltage drop V_T generally ranges from 1 to 2 V for a peak current $i_T$eff $\sqrt{2}$ corresponding to the triac nominal current. Its maximum possible value V_{TM} at 25 °C is given for each triac in the applicable sheets of characteristics.

If I_G is interrupted at instant t_2 (Figure 3) when the instantaneous value of the current is still high, the operating point remains on the conducting-state characteristic drawn in full line on Figure 4, up to instant t_3 (point D) when the current has decreased to a sufficiently low value I_H. The minimum anode current I_H for which the triac remains conducting without gate current, is called **holding current** (or hypostatic current)* as in the case of the thyristors.

* As a matter of fact, there are two holding current values I_H and I'_H depending upon the polarity of V_a. These two values are generally very close to each other.

Figure 2 : Triac Static Characteristics with Open Gate (not to scale).



I_H is very low with respect to the triac nominal current (in the cold condition the maximum value of I_H guaranteed by the specifications never exceeds a hundred mA, even for very large triacs; in the warm condition, the value of I_H decreases considerably). Therefore, its influence on the operation as a switch does not have to be taken into consideration, as a general rule, in practical applications, except in operating conditions in which the load temporarily offers a high impedance at an instant at which the effective supply voltage is low.

The delay in the rise of the current following the application of the control does not exceed a few microseconds. But, to achieve steady firing, current I_G must be applied for a sufficiently long time.

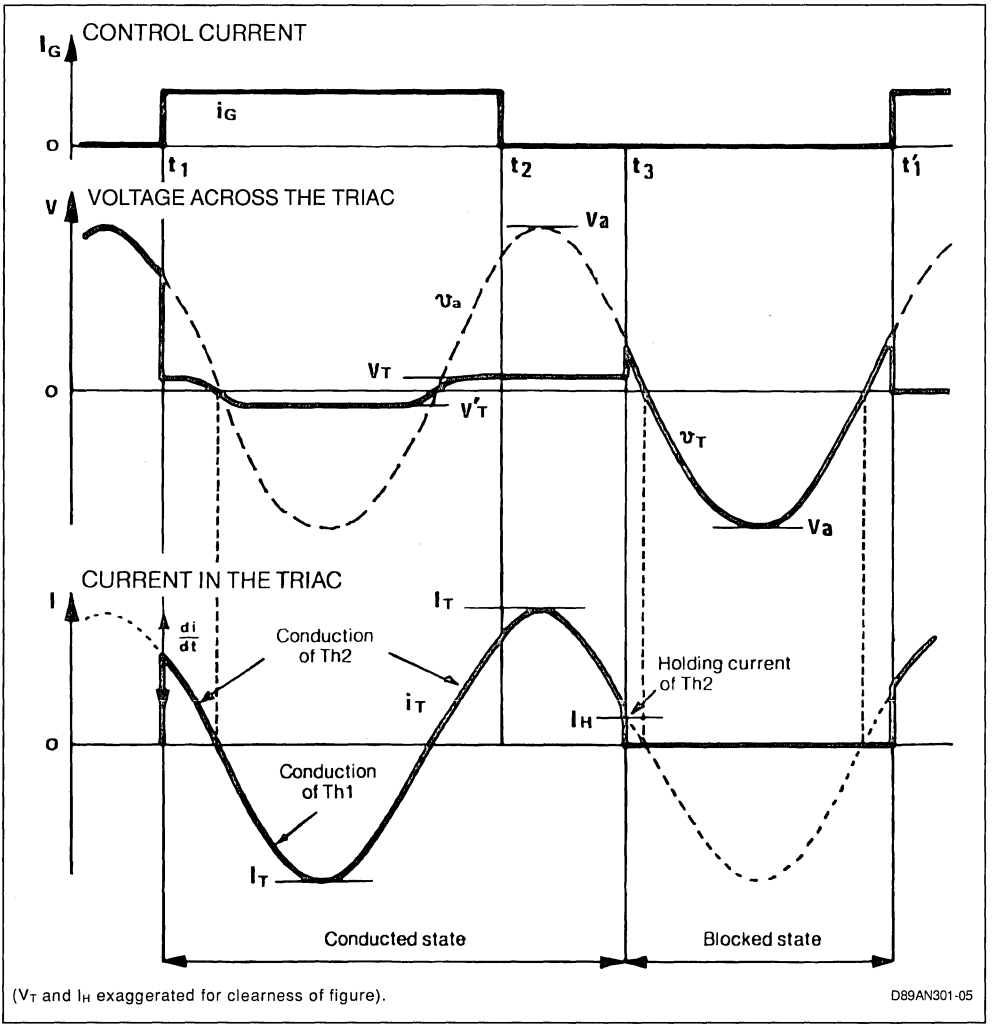
The gate pulse duration must a least be long enough for a sufficient charge to be injected into the gate region. The minimum duration Δt of a rectangular-wave pulse of current I_G having just the specified value I_{GT} min is on the order of about twenty µs.

This required duration decreases when the value of I_G increases.

If current I_C in the load does not immediately build up (inductive load) it is necessary, in addition, to hold the gate current until the load has given passage to a minimum current I_L. The 2**latching current**" is equal to, or higher than, i_H, depending upon the respective polarities of A2 and G. It corresponds to point E on the conducting-state characteristic (*Figure 4*).

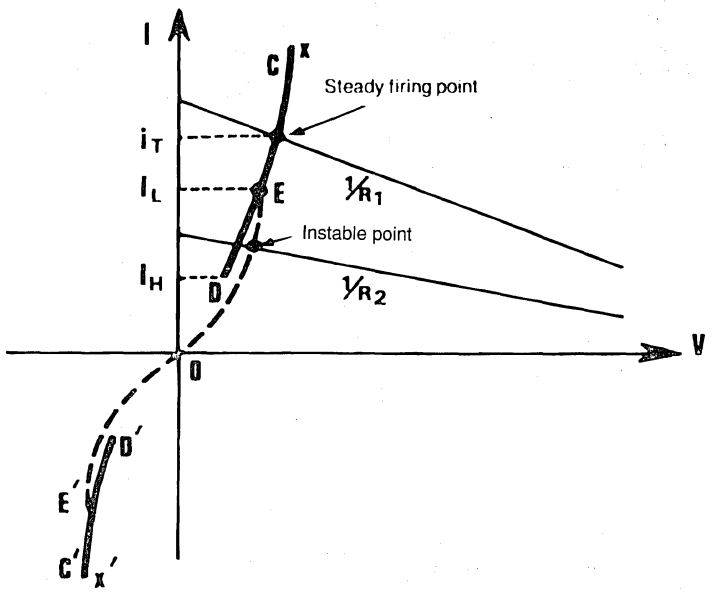
Current I_G applie dto the gate to fire the triac with either polarity of the supply voltage, can indifferently be of positive or negative sign with, however, triggering abilities which, for average-power triacs, can be somewhat different depending upon these polarities*. There are four possible cases which are determined in accordance with four "triggering quadrants" defined in Table 1.

Figure 3 : Waveforms in a gate-controlled triac with resitive load.



Certain series are not specified in quadrat IV as regards firing current.

Figure 4 : Static Characteristics with $I_G = I_{GT}$ (exaggerated around zero).



Load straight 1/R1 : ensures steady firing ($i_T > I_L$).
Load straight 1/R2 : does not ensure steady firing ($i_T < I_L$).

Table 1.

Triggering Quadrant	Polarity with Respect to A1		Firing Conditions for Small Triacs	
	of A2	of G	I_{GT}	I_L/I_H
Q. I	+	+	Low	= 1
Q. II	+	—	Medium	2 to 5
Q. III	—	—	Medium	= 1
Q. IV	—	+	High	1.5 to 3

1.4. VARIOUS MODES OF CONTROL OF THE TRIAC

On Figure 3, instants t_1 of gate current application were supposed to occur randomly with respect to input voltage V_a. This operation is similar to that of an electromechanical relay; the difference, however, is that the triac switch becomes conducting at the precise instant (to within a microsecond) of application of the control, and blocks again, after the control has been removed, at the precise instant at which the current drops below I_H (i.e. practically to zero with respect to the nominal current).

This precision can be made use of to carry out the control in exact synchronism with voltage V_a, in order to sample periodically the voltage applied to the load over intervals of several half waves * (control by half-wave trains), or over half-wave fractions (control by conduction angle). By causing the respective durations of the "conducting" intervals to vary with respect to the "blocked" intervals, a variation of the power applied to the load is achieved.

Whenever permitted by the inertia of the user circuits, the control by half-wave trains offers substantial advantages when, in addition, the firing of the triac is allowed to occur only close to the point where the voltage across the triac goes through zero (i.e. just after zero crossing of the current). Since the triac will next stop conduction also at the zero crossing of the current, this mode of control always ensures a whole number of complete "conducting" half waves (*Figure 5 a*). On the other hand, triggering on going through zero eliminates any sudden variation of the current flowing through the load, which avoids parasitic radiations and strains in the triac and user circuits. With this type of control, the mean power allied to the load is merely:

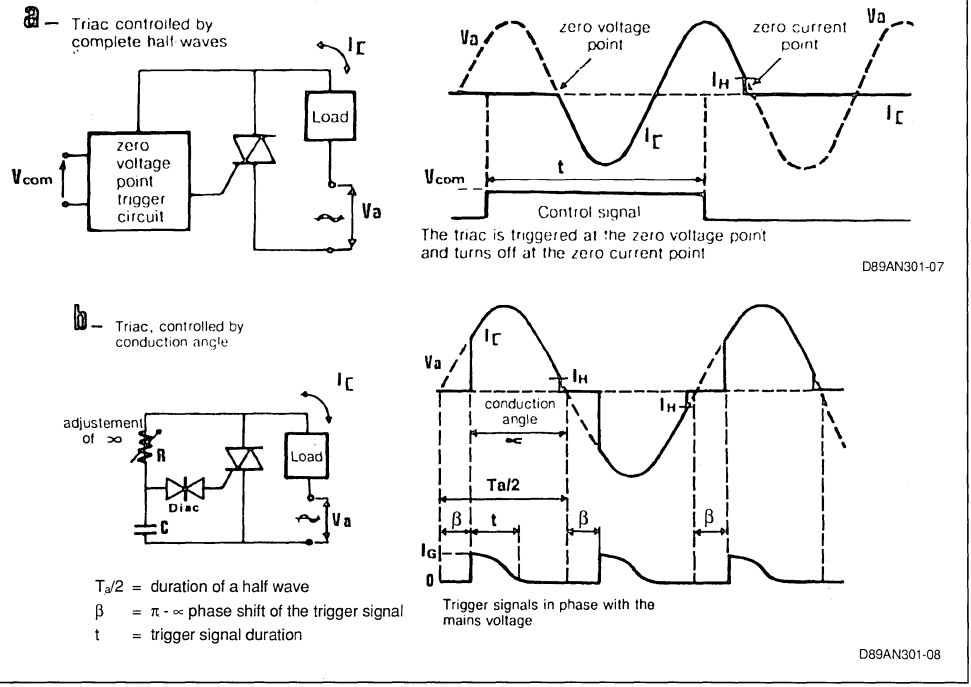
$$P_{AV.} = \frac{n\,T_a}{2\,T_e}\ V_{RMS} \cdot I_{RMS} \qquad (1)$$

with: n = number of "conducting" half waves in each sampling period T_e.

T_a = period of the mains current (20 ms in the case of a 50 Hz mains).

V_{RMS}, I_{RMS} = rms values of the input voltage and current.

Figure 5 : Modes of Control of the Triac in Syncronism with the Mains Voltage (theoretical waveforms on resistive load).



$T_a/2$ = duration of a half wave

β = $\pi - \alpha$ phase shift of the trigger signal

t = trigger signal duration

* The term « half wave » designates each (positive or negative) half of the mains current alternating wave.

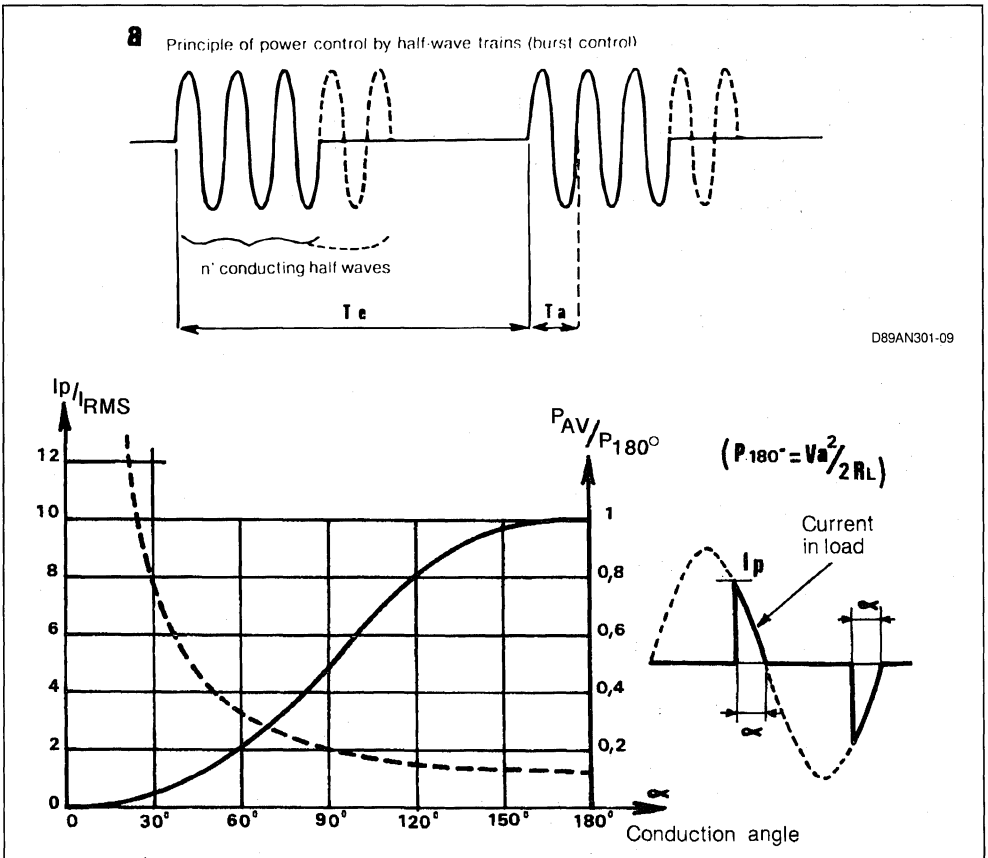
The fineness of adjustment of P_{AV} obviously improves when T_e increases with respect to T_a. A sampling period of 1 second permits adjustment in steps of 1/100. If the load does not not stand any dc component, it is necessary to add to the circuit a system of variation per couples of half waves (full waves) requiring, for the same fineness of adjustment, a double sampling period.

In many cases, however (for instance for light dimmers, for the control of highly loaded low-inertia motors or for regulators with low time constant), it is necessary to sample the power at the frequency of the ac supply mains. To do this, it is only necessary to control the gate by current pulses occuring with a phase shift (π α) with respect to the beginning of each half wave. Figure 5b illustrates the principle of this control, with waveforms obtained on resistive loads as well as a simple example of practical application. The conduction angle of the current is α and the mean applied to the load is fairly equal to:

$$P_{AV.} = \frac{1}{\pi} \frac{(V_{RMS})^2}{R_L} \int_0^{\alpha} \sin^2 \alpha . d\alpha$$

$$\text{or } P_{AV.} = \frac{2\alpha + \sin^2 \alpha}{2\pi} \frac{(V_{RMS})^2}{R}$$

Figure 6 : Triac Power Control.



In full line (right-hand scale) = Relative change of the power delivered to a resistive load R_L (operation at constant input power).
In dotted line (left-hand scale) = Change in the ratio I_P/I_{RMS} of the peak current to the effective current on resistive load R_L (operation at constant delivered current).

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Figure 6 b shows the change in the delivered power P as a function of conduction angle α, when the input power is kept constant. As can be seen, the relationship between P and α is highly non-linear. To obtain a linear relationship between the mean vol-tage on the load and an adjustment voltage V_r, the latter must act on α with an inverse law.

Figure 6 b also shows (in dotted line) the curve of the change in peak current I_p as a function of the conduction angle with left kept constant, i.e. for a constant power in the load. The curve clearly shows the dangerous condition which exists in case of operation at low power with a low conduction angel when I_p exceeds the permissible repetitive surge current.

1.5. OPERATION ON INDUCTIVE LOAD

In the case illustrated by figure 3, where the triac operates on a pure resistive load (cos φ = 1), the current reaches immediately the value V_a/R_L when the gate current I_G is applied. This is a theoretical case, for the leads connecting the triac to the mains and load always offer an inductive component which slows down the rate of rise di/dt of the current, and causes a slight phase shift of the instant of current interruption with respect to the zero input voltage point.

With a load offering a high inductive component (cos φ lower than 1), inductance L limits the current rate of rise to:

$$\frac{di}{dt} = \frac{V_a}{L} \qquad (3)$$

where V_a is the instantaneous value of the input voltage at the instant of application of the firing control. If the gate signal is applied for a duration which is long with respect to that, $T_a/2$, of a half wave of V_a, the waveforms shown in full lines on figure 7 are obtained. Following a periodo of transition, current I_C reaches the value:

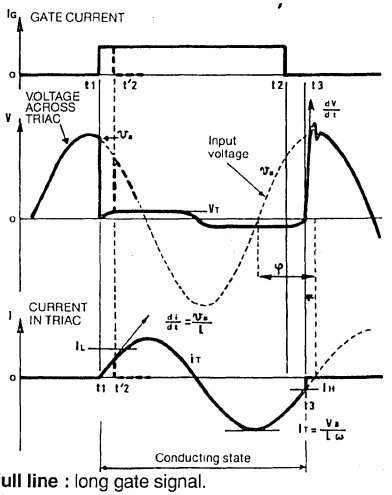
$$\frac{V_a}{L\omega} \sin(\omega t + \varphi), \text{ with } \omega = \frac{2\pi}{T_a}$$

φ represents the phase shift of I_C with respect to V_a, close to /2 when the load is highly inductive. After $\pi/2$ the control has been removed, the current is maintained in the load, as mentioned previously, until its instantaneous value drops below I_H. But, due to phase shift φ, the value of the input voltage is different from zero at that instant. Consequently, the vol-tage across the triac increases suddenly up to value v_a (close to V_a), at a high rate of rise dV/dt which is limited only by capactive elements possibly present in the circuit.

If the triac control had been removed at time t_2, immediately after reaching value I_G (short-duration gate pulse), the current in the inductance might not have had the time to reach value I_L of the triac latching current. Firing would not have taken place in a steady way, and the voltage would have increased again up to v_a as indicated by the dotted lines on figure 7.

During operation on an inductive load with short-during gate pulses, other unwanted conditions may be present when these pulses are applied at the beginning of each half wave of V_a, within angle φ.

Figure 7 : Waveforms with Inductive Load.



– **in full line** : long gate signal.
– **in dotted lines** : effects of too short a gate signal.

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These conditions are represented by the full-line waveforms on figure 8: when the first gate pulse (a) appears, for instance at the beginning of a positive half wave, current I_C increases up to a value at least equal to that of the steady state current and, then, decreases again to a value below I_H only after the time corresponding to angle φ during the next negative half wave. Since the new control pulse (a') already ends at t'_2, i.e. prior to the cancellation of the current, there will be no gate current at t_3 to fire agin the triac during the negative half wave. The next firing will not occur until t''_1, through pulse a", during the subsequent positive half wave.

Thus, with this control, the triac behaves like a unilaterai switch, conducting only on the positive half waves (similarly, if the first pulse (a) had appeared during a negative half wave, the current would pass only during negative half waves). This results in a rectifying effect introducing a high mean positive (or negative) current into the load. When the latter consists of a coil wound on a magnetic core with small air gap, or of a transformer primary coil, the operating point describes a large portion of the hysteresis loop. This presents the risk of creating a situation in which the core is almost satured, with the disastrous consequence of an extremely high surge current.

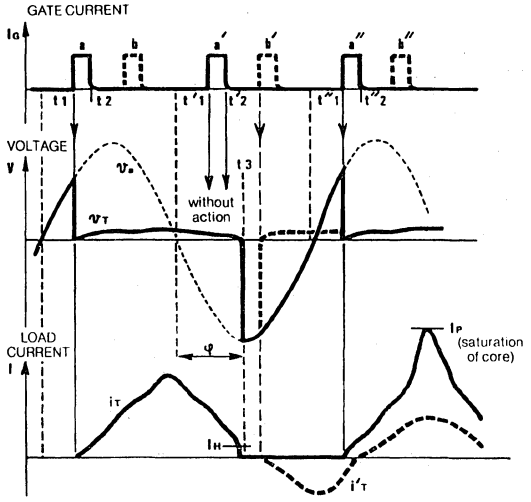
This abnormal operation woud not have taken place if the pulses had a duration equal to, or higher than, that corresponding to angle φ, at the price higher control energy. The effect of the rectification phenomenon can suppressed through a power-saving means which consist in controlling the triac by pulse trains instead of only one pulse for each half wave. As a matter of fact, figure 8 shows (waveforms in dotted lines) that a new pulse (b') occuring immediately after the current has been concelled, permits triggering again the triac during the negative half wave. There still remains a dissymmetry between the positive and negative current arches, but the rectifying effect can be considered negligible when the pulses are sufficiently closely spaced.

The various modes of control illustrated by figure 5 in the case of a resistive load, can be used as well with an inductive load, provided the following precautions are taken:

A) - For control by half-wave trains, the gate pulses should be centred around the zero point of the current that is to say when the voltage is re-applied. This permits ensuring re-firing of the triac immediately after the cancellation of the current (instant t''_2 on figure 8).

B) - For control by conduction angle, gate pulses of sufficiently long duration, or pulse trains starting from (π - α) corresponding to the required opening angle, and ending toward the end of the half wave, should be used.

Figure 8 : Control by Wide Conduction Angle on Inductive Load with Short-Duration Gate Pulses.



– **in full lines :** Rectification effect due to the combination of a narrow pulse with a wide angle.
– **in dotted lines :** Waveforms with two-pulse trains for each half wave.

2. SAFE-OPERATION PARAMETERS

The reliability of the triac is dependent upon a number of utilization precautions which cannot be taken without a thorough knowledge of the stresses or spurious phenomena to which the triac is liable to be exposed.

We shall examine the influence of thermal stresses and of current surges on its service life, and of overvoltages on its blocking capability. Finally, we shall indicate a few means of protection against these parasitic conditions.

2.1. THERMAL STRESSES

The data sheets give a limit value of the junction temperature: (T_j) max. When the effects of a high-temperature operating environment and of the increase of semiconductor self heating due to the dissipated power, cause the triac junctions to reach a temperature higher than (T_j) max, the result can be a temporary alteration of the performances, then a irreversible degradation gradually evolving to the complete destruction of the device when that situation remains unchanged for an extended period of time, or occurs repeatedly. Any degradation will be accelered in cases where an excessive temperature combines with other stresses (overvoltages, short spikes of current or of di/dt etc). In case where the occurence of such conditions in anticipated, appropriate measures have to be taken to keep the junctions at a temperature substantially lower than the maximum specified value.

Direct measurement of junction temperature T_j is hardly possible during operation. An approximation of its average value can be obtained from the case temperature t_{case}, specified junction/case thermal resistance $(R_{th})_{jc}$ and dissipated power P_{AV}:

$$T_j - T_{case} = (R_{th}\ j\text{-}c).\ P_{AV} \quad (5)$$

The data sheets often give curves of P_{AV} versus condition angle α, showing a decrease of P_{AV}, and consequently of the mean temperature, at small angles α. But, it is to be remembered that the instantaneous junction temperature at small conduction angles may rise substantially higher than T_j AV.

In case of full conduction, an excess value for the dissipated power can be easily calculated by considering that voltage drop V_T in the triac is of the form:

$$V_T = Vto + Rt.I_T$$

In which Vto is the threshold voltage and Rt, is the dynamical resistance of the on-state characteristic. These 2 parameters are given in the data sheet of each part number. For a sinusoidal current I_{TRMS} the power dissipation of the triac is:

$$P = 2\sqrt{2/\Pi})\ I_{TRMS}\ Vto + Rt.I^2_{TRMS}$$

2.2. CURRENT STRESSES

In many practical applications the triac may have to withstand current surges. Let us mention more particularly:

- shor-circuits of the load,
- user circuits including a capacitive component,
- utilization with incandescent lamps (resistance when cold 10 to 20 times lower than when hot),
- utilization with coils wound on magnetic cores liable to saturation,
- spurious firing of the triac by high-energy overvoltages.

NON-REPETITIVE CURRENT SURGES

The dtasheet indicates a limit value I_{TSM} for the peak of the non repetitive* current allowed to flow through the triac during one, half cycle of the supply mains.

As a general rule, this limit value is 6 to 7 times higher than the nominal peak current I_{TM} of the triac (i.e. 8 to 10 times higher than the nominal rms current). Most of the devices are capable of withstanding without destruction an even higher non-repetitive current peak when its duration is lower than 10 ms.

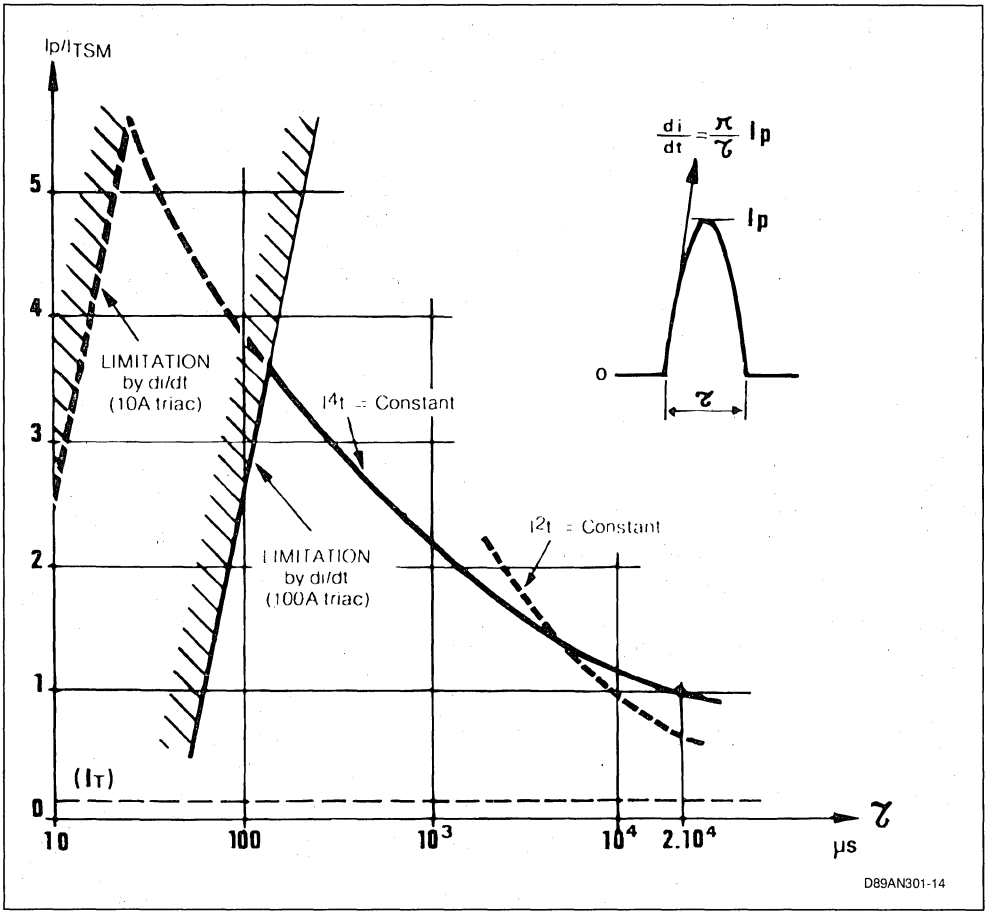
The specification give a limit value for the expression $\int i^2dt$ for current surge durations ranging from a few milliseconds to some ten milliseconds. This expression fairly well characterizes the operation of a cutout; its value is helpfull in selecting the "I^2t" of a fastacting fuse intended to protect the device against possible shor-circuits of the load. However, it should be used cautiously when the value of the permissible peak current is to be deduced from it, because it is only valuable to represent the surge capability of the triac for a given pulse duration within a narrow interval. For lower durations ranging from a hundred microseconds to a few milliseconds, the permissible non-repetitive current surge in the triac follows a curve closer to that given by the expression:

$$\int i^4dt = \text{constant}$$

as repsented on the theoretical curves of figure 9.

* The device is supposed to withstand this non-repetitive anomaly a limited number of times (a hundred times, according to the JEDEC standards) during its lifetime

Figure 9 : Permissible non-repetitive current surge Ip in the case of a sine wave arch of duration τ.



Finally, for very short current-pulse durations, the permissible current surge is mainly limited by the rate of rise di/dt of the current, which necessarily associated (figure 9).

The limitation by di/dt occurs in a more critical way at the instant the triac is fired (willingly or accidentally) on a low-resistante load with low inductance. An examination of the waveforms of figure 3 shows that firing on a purely resistive load outside of the zero voltage point, entails an extremely fast increase of the current. Practically, there always exists, fortunately, a small inductive component (due to the leads connecting the device to the mains and load) which limitis the rate of rise of the current. But, that rate of rise can reach prohibitive values at the instant the current reaches an high value due, for instance, to the presence of capacitances on the triac terminals, or to a very low instantaneous value of the voltage (spurious firing by an overvoltage).

The harmful effect of a high rate of rise di/dt can be explained, as for the thyristors, by the concentrations of current, and, consequently, by hot points, produced at the instant of the firing, due to the fact that firing first occurs in a very narrow region before spreading out over the full area of the junctions. Since the spreading speed of the conducting region increases when the gate current increases, the behaviour in the presence of non-repetitive high di/dt values will be considerably improved when the triac is fired by a current I_G rapidly reaching a high value.

REPETITIVE CURRENT SURGES

Repetitive stresses with surge current values much lower than the limit value indicated for non-repetitive stresses can lead to an alteration of the triac performances as a result of the cumulative elevation of the instantaneous junction temperature which accompanies them.
This is particularly the case when the triac operates continuously with a small conduction angle while delivering high power. This mode of operation corresponds to high peak currents during short periods of time. At the instant of each passage of the current peak, thereis a risk of the triac junctions reaching a prohibitive temperature. The knowledge of the global transient thermal impedance of both the triac and the heat sink, permits verifying that the instantaneous value of the junction temperature does not exceed (T_j) max.
For very small conduction angles with a resistive or capacitive load, another limitation is given by the rate of rise di/dt of the current in the repetitive state, as will be seen hereafter.
The value of di/dt repetitive is lower (in a ratio of 2 to 3, as a general rule) than the value of di/dt specified for non-repetitive current surges. Such repetitive di/dt values are particularly harmful when the circuit is capacitive. For asynchronous operation (*figure 3*) or for operation with a small conduction angle (*figure 5b*), it is highly recommended to connect a low-value resistor (a few tens of ohms) in series with the capacitances possibly present on the triac terminals.
Operation with "zero voltage point" triggering (*figure 5 a*) does not give rise to any difficulty due to a **repetitive** di/dt subce tge truac us fured at the precise instant at which the voltage, hence the current draw, is null. (but, non-repetitive di/dt values are still liable to occur when all the required precautions have not been taken for the avoidance of untimely triggering at instants at which the voltage value is different from zero).

2.3. BLOCKING CAPABILITIES

PEAK VOLTAGE AT BLOCKED STATE: V_{DWM}.

In normal working conditions, with an input voltage of low frequency (lower than 100 Hz) free of strong parasitic transients, the triac behaves like an open circuit so long as no gate current is applied and that the ac voltage amplitude does not exceed the V_{DWM} value guaranteed by the data sheet particular to this triac. That specified vol-tage V_{DWM} is actually guaranteed for a value notably lower than V_M and V'_M (figure 2) throughout the authorized temperature range. For that voltage, the leakage current, "peak current in the blocked state", has a maximum value guaranteed at the maximum authorized temperature.

CRITICAL RATE OF RISE OF THE VOLTAGE IN THE BLOCKED STATE: "STATIC" dv/dt.

During operation in the presence of parasitic transients, the triac may lose its blocking capabilities, even if the peak voltage of the transient does not exceed V_{DWM}, but when its rate of rise dv/dt is higher than a critical value. As a matter of fact, in such a case current C_T dv/dt developed across the spacecharge capacitance C_T of the reverse biased junction with reverse bias in the blocked state, acts as a gate current liable to fire the triac. This susceptibility to steep voltage leading edges obviously increases with a higher sensitivity of the triac (low I_{GT}) and a higher temperature of the semiconductor. The datasheets indicate a value of dv/dt withstanding capability with a leading edge of 0.6 V_{DWM} amplitude and with a junction temperature close to the permissible maximum. These values are typically on the order of a few hundreds of volts/µs for low-sensitivity devices and decrease down to some ten volts/µs for highly sensitive devices.

CRITICAL RATE OF RISE OF THE VOLTAGE DURING SWITCHING: $(dv/dt)_c$

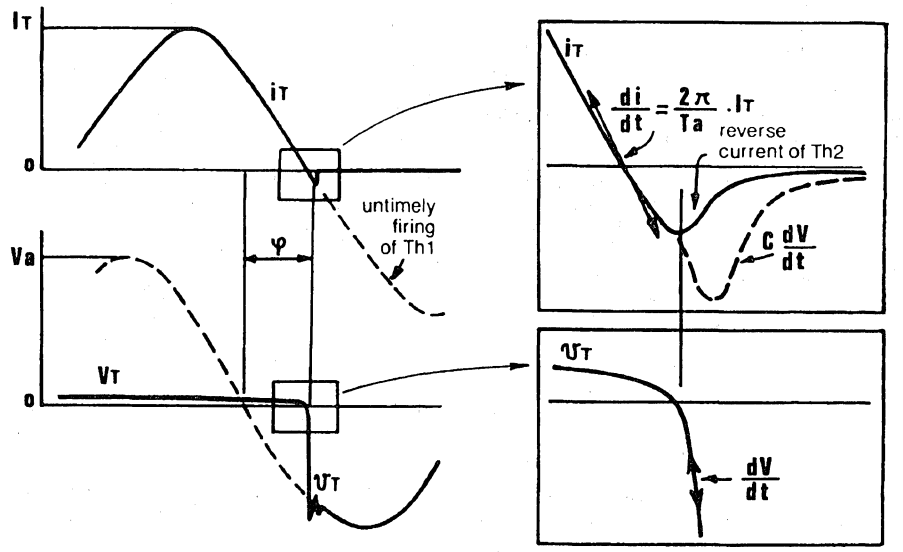
The susceptibility to dv/dt of the triac in the blocked state is based on the same phenomenon, and leads to values of the same order as in the case of the thyristors. However, in a conventional triac, the two elementary thristors Th1 and Th2 illustrated by figure 1 (section 1) being strongly coupled, one can expect reactions between these elements, which are liable to affect the blocking capabilities when the current cancels after each reversal of the input voltage polarity.

In extreme cases, this coupling can cause the triac to remain conducting without gate current, through the following process: when, following the suppression of the control signal, the current reverses in the load, for instance, by positive values (*figure 11A*), "internal thyristor" element Th2, which was in the conducting state, keeps stored charges. The discharge of these charges results in a reverse current (curve in full lines of figure 11 B) which can act as gate current for the other "internal thyristor" element Th1 of the triac and, thus, spontaneously fire the triac on the subsequent negative half wave.

However, the risk of spontaneous self-firing of the triac from one half wave to the other, exists only if the slope of the current decay $(di/dt)_c$ at the instant of turn-off is too high.

With the usual passive loads of fairly linear I/V characteristics, the di/dt at turn-off is proportional to I_{RMS}/Ta. With a 50 or 60 Hz supply mains and a junction temperature lower than t_{vj} MAX, the first unfavourable condition only arises, when the triac controls a very high rms current I_{RMS} (high-power applications). However, there are risks of high di/dt

Figure 10 : Spurious re-firing by " commutating dv/dt" on inductive load (cos ≠ 1).



A : Application of the voltage at the instant of commutation.

B : Exaggerated commutation region

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values occuring on turn-off, even with effective currents of not very high nominal intensity:

a) when the frequency of the ac input voltage is much higher than 60 Hz

b) or when the triac switches the ac terminals of a single-phase rectifier with inductive load, or, still, in certain cases of switching on polyphase rectifers,

c) or, finally, after the passage of a high current surge, as can be the case when turn-on occurs on a load including a saturable core, or on lamps of very low resistance when cold.

However, on a resistive load there is a risk of spontaneous self-firing only when the junction reaches an instantaneous temperature higher than the specified limit value. (this situation can arise, for instance, following an overload, or when, through poor knowledge of the transiente thermal impedance, the user operates the triac at a small opening angle with high peak currents and a high case temperature).

A second parasitic phenomenon occurs when the load is an inductive one: since the inductive component of the load causes a phase shift of the current with respect to the voltage, the voltage across the triac tends to change, at the instant of turn-off of Th2, from a very low value (V_T at low current) to a high value which is the input voltage value at that instant (*figure 10 A*). The resulting voltage wavefront adds to the reverse current and additionnal current C dV/dt (in dotted line on figure 10 B) which contributes to the firing of the other element Th1.

Conventionally, the immunity of triacs to self-firing is characterized by the value of dV/dt to be introduced by an inductive load at the instant of switching, in order to cause the spontaneous re-firing of a triac from one half wave to the other.

This "commutating dv/dt" parameter is generally given by the data sheets for a specified value of di/dt on turn-off (as a general rule, the value corresponding to the nominal operating current at 50 Hz of the triac), and for specified values of the peak voltage and junction temperature (voltage V_{DWM} and maximum permitted temperature, as a general rule).

In all usual circumstances, without turn-off di/dt higher than the nominal value for the 50 or 60 Hz supply mains, the most appropriate precautions warranting the triac blocking capabilities at commutation, consist in selecting a device of not too high a sensitivity and, above all, in using a heat sink sufficient to prevent the instantaneous junction tem-

perature from ever exceeding 80° to 90°C. An additional preventive measure in case of an inductive load is the addition, to the triac terminals, of an RC network limiting the rate of rise of the voltage. The dimensioning of such a protective network will be discussed later on.
Spurious firing actions through dV/dt are detrimental to the triac only when the entail excessive overloads through surge current and di/dt.

3. APPLICATION EXAMPLES

The filed of application of the triac is extremely wide. As a matter of fact, it covers the control of all the equipment operating on alternating current. We shall merely give here the diagrams of a few examples of typical application, and recall, at the end of this note, the general precautions recommended for the utilization of triac (APPENDIX 1).

Before describing these examples, we shall add a few precisions of pratical order to the information given in Sub-section 1.3 about the control of triacs, by referring more particularly to Table I.

As can be seen on table I, the best gate sensitivity homogeneity with either polarity of the mains voltage (applied to A2) is obtained in firing quadrants II and III, which corresponds to gate pulses of negative polarity with respect to A1 (*figure 11 b*). Recent triac control ICs are, generally, designed for this mode of firing.

But, when the latching current constitutes a critical parameter (operation at very low or highly variable current, or at low conduction angle on an inductive load), it is preferable to control the gate by alternate pulses in accordance with the mains voltage polarity (quadrants I, III, figure 11 a). The switches shown on figure 13 and 14, and the diac controllers which will be described in Sub-section 3.2 operate in these conditions.

When the control circuit does not directly deliver alternate pulses, or when the control power is insufficient with respect to the gate sensitivity of the triac to be used, there always remains the possibility of controlling that triac through low-energy pulses by inserting a sensitivie auxiliary static switch between A2 and G. Such a switch can consist either of a small triac (*figure 12 A*), or of a diode bridge switched by a sensitive thyristor (*figure 12 B*). Thus, the main triac will be fired in quadrants I, III, and its

Figure 11.

Mains voltage
a - Firing in quadrants I, III.
b - Firing in quadrants II, III.

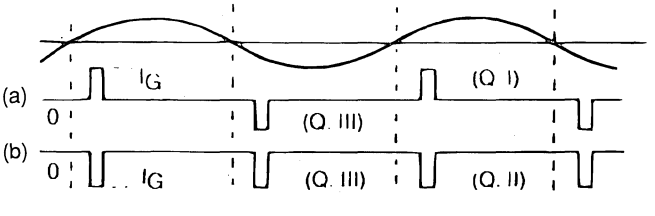
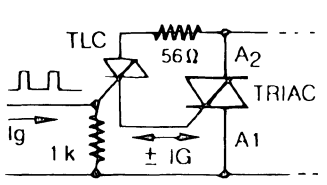
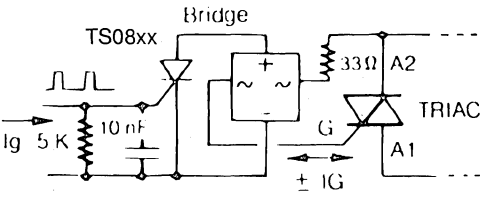


Figure 12.



A) 5 mA control pulse



B) 0.1 mA control pulse

gate current automatically adjusted for the amplitude and duration required for steady firing of the triacs.

3.1. STATIC SWITCHES

The use of a triac as an "on/off" device in an alterning-current circuit represents the simplest application of that semiconductor switch. Such a utilization offers many advantages with respect to mechanical and electromechanical devices:

low control power with respect to the controlled power,

short response time on closing of the circuit, and absence of contact bounce,

possibility to select the firing instant within the phase,

in particular, possibility of firing at the zero voltage point, thus minimizing interference caused by the mains and environment,

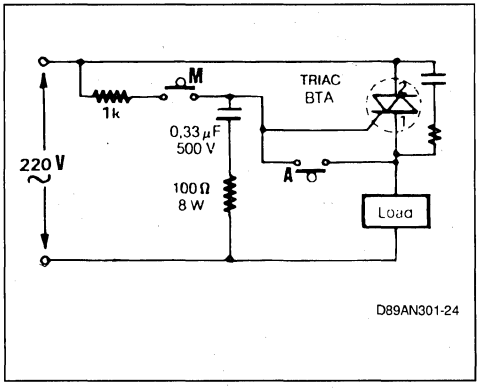
no wear related to the number of switching cycles,

automatic breaking of the circuit at the zero current point, i.e. without arcing, even an inductive load.

MICROSWITCH-CONTROLLED STATI SWITCH (PERMANENT CONTACT).

With the circuit represented by the diagram of figure 13, the control energy is taken from anode A2 of the triac, i.e. directly from the mains power through the load, which permits providing a gate current of the

Figure 13 : Asynchronous Triggering Through Microswith.



load current and mains voltage (inductive load or polyphase circuits), it is absolutely necessary to synchronize the gate pulses with the voltage across the triac (see sub-section 1.5) and not with the mains voltage.

STATIC RELAY INSERTED ON ONE LEAD.

The switche shown by figure 13 can be inserted on one lead, without access to the other mains pole.

required intensity. As soon as triac T is fired, the voltage across it almost cncels, as well as the gate current which is thene exactly proportioned to achieve steady firing (R_1 is of low value, 15 to 50 ohms, so that each re-firing after closing occurs near the zero voltage point, with a sufficiently steep leading edge).

"ON/OFF" SWITCH CONTROLLED BY MOEMENTARY-CONTACT SWITCH (*fig. 14).*

Closing of the "on/off" switch is controlled through a (momentary-contact) push-button switch M; operation is then ensured by the capacitor current which is in phase quadrature with the input voltage.

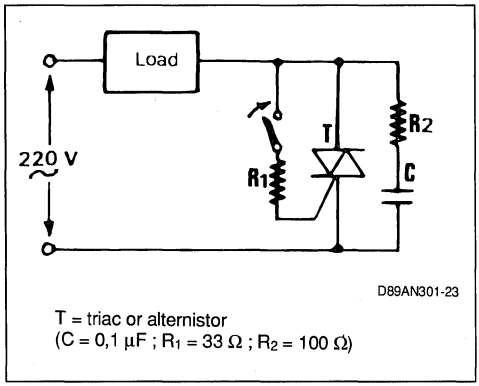
Opening of the switch is then achieved either by short circuting between the control electrode and electrode "1" of the triac (momentary-contact switch A), or by opening the gate circuit.

STATI SWITCHES CONTROLLED AT THE "ZERO VOLTAGE POINT"

To meet the requirements of the standards concerning the limitation of interference injected into the mains through electrical house appliances, it is necessary to eliminate any sudden current surge at each firing and re-firing of the triac.

With single-phase voltage and a purely resistive load (cos φ = 1), this is achieved by firing the triac with pulses centred on the zero crossing of the mains voltage. But, with a phase shift φ between

Figure 14 : Setup of an «On/Off» Switch.



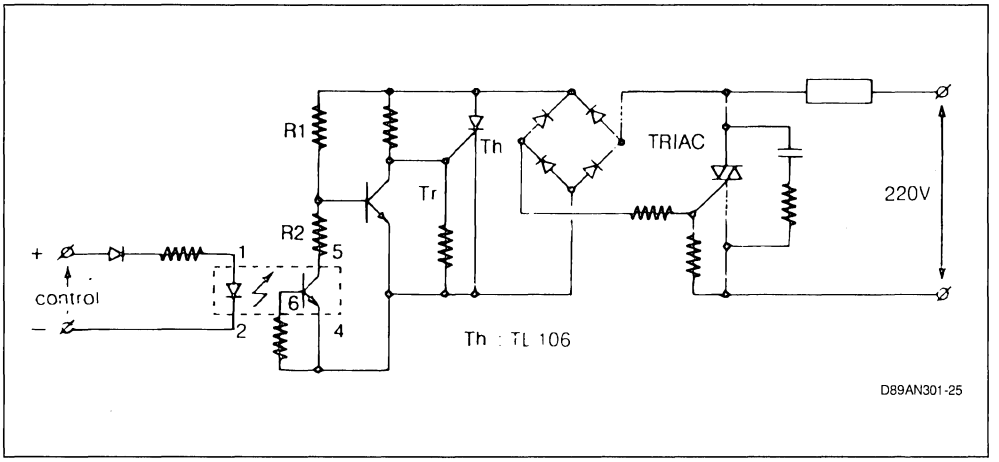
T = triac or alternistor
(C = 0,1 µF ; R_1 = 33 Ω ; R_2 = 100 Ω)

But, it cannot be directly used for the synchronization on a zero crossing of the AC voltage. However, it is possible to set up a static relay with zero-point firing, in accordance with the same principle of gate current supply from the voltage across the triac, by replacing the mechanical contact with the arrangement shown by figure 12 B, and by controlling the sensitive thyristor through a photocoupler (*fig. 15*).

The triac gate pulse is provided by the thyristor. Transistor Tr enables inhibiting firing of the thyristor depending on the instantaneous amplitude of the mains voltage and the photocoupler control.
If the photocoupler is not supplied, transistor Tr is continuously saturated. It prevents firing of the thyristor.

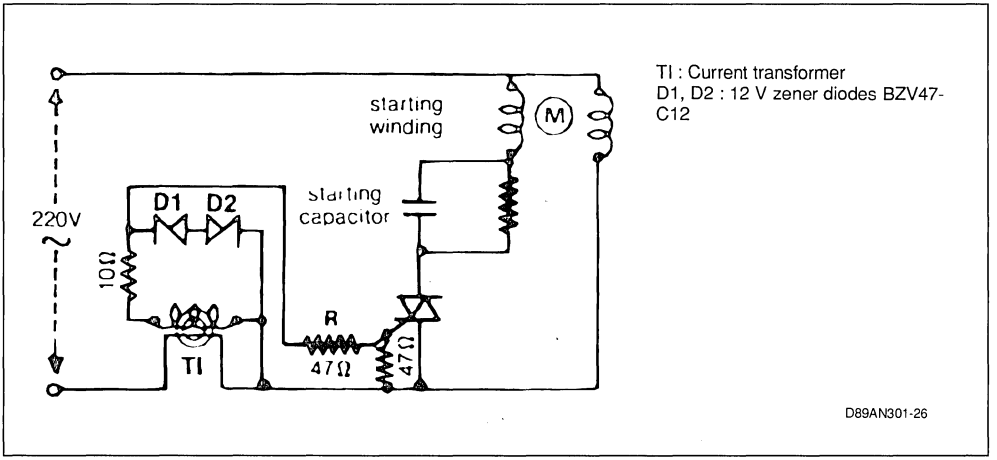
When the photocoupler is controlled by the voltage divider consisting of resistor R1 and R2, transistor Tr is blocked only when the mains voltage is close to 0 V. The triac is then controlled at the mains zero voltage point.

Figure 15.



STARTING OF AC MOTORS (*figure 16*).
The triac is controlled by means of two zener diodes which detect, on the secondary side of a current transformer, the current surge due to the starting of the motor. The semi-conductor device operates only during the time required by the motor to reach synchronism. Consequently, it is not necessary to use a large heat sink. But the compromise between I, R and the transformation ratio of TI has to be correctly adjusted.

Figure 16 : AC Motor Starting Control



3.2. POWER CONTROLLERS

The systems for burst or phase control mentioned in Sub-section 1.4 (*figures 5 and 6*) are used to vary the average power delivered to a load (lamp, motor, heating elements, transformers etc).

We shall give the diagrams of a few power controllers as examples. By feeding back to their control terminals the information provided by suitable sensors coupled to the user circuits, it is possible to make up lighting, speed, pressure, temperature, voltage or current regulators.

DIAC CONTROLLERS.

This is the simplest method for power variation through phase control. In spite of its lowe accuracy, this method is applicable without particular difficulty for power control on resistive loads, or for speed variation of small motors.

To ensure a satisfactory adjustment range, and improve the reversibility of the adjustment, it is advisable to complete the circuit shown by figure 5 b, by an additional RC network, known as "antihysteresis" network (6.8 kΩ and 100 nF on the light dimmer diagrams of *figure 17*).

Slave control of the phase angle by the ambiant lighting, or by an external light phenomenon bay be required to ensure a constant illumination level. With the circuit shown by figure 25 a, this will be achieved by connecting a photoresistor in parallel with the phaseshift capacitor for varying the charging voltage of the latter in accordance with the illumination level.

A variation of the luminous flux of a fluorescent strip light can be obtained in the same manner. This is a particularly attractive application, since the colour of the visible light produced by a fluorescent lamp is almost entirely independent of the luminous intensity, which is not the case with incandescent lamps. With the set-up shown by figure 17 b, highly progressive intensity variation is achieved over a wide luminosity range by connecting the triac in parallel with the fluorescent lamp. Thus, the lamp conduction angle corres-ponds to the triac off-state angle and, consequently, commences at the beginning of each mains voltage half wave.

Figure 18 illustrates a circuit used for speed control of a fan drive motor. Since this type of motor generally comes to a stop long before the conduction angle has decreased down to the triac turn-off point, no antihysteresis network is required. A limitation of the speed adjustment range (resistor R3, possibly adjustable) may be sufficient to avoid hysteresis problems.

However, in this example a partial antihysteresis effect is accessorily produced by the circuit consisting of R_1, R_2 and dioded D_1, D_2, the main purpose of which is to linearise the speed adjustment and, above all, to render it substantially independent of mains voltages variations.

Figure 17 : Luminosity Adjustment of an Incandescent (a) or Fluorescent (b) Lamp.

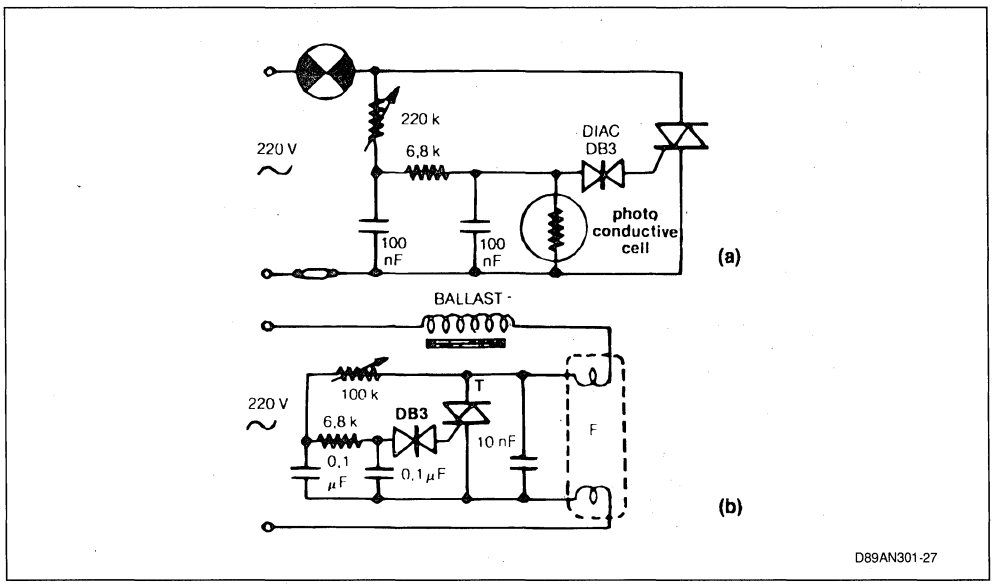
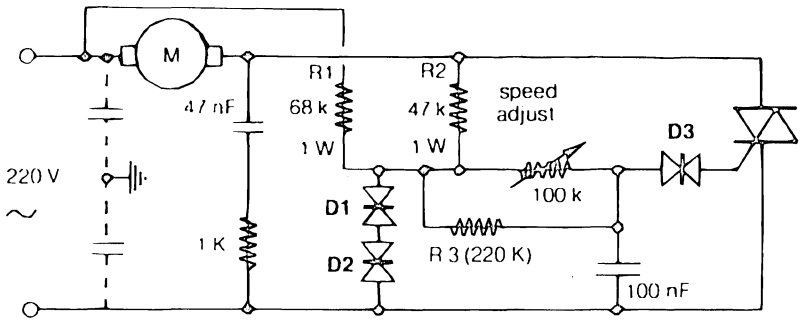


Figure 18 : Motor Speed Adjustment with Compensation of Mains Voltage Variations.



(D1, D2, D3 = diacs DB3)

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3.3. SWITCHING OF TRANSFORMERS

As a general rule, the switching of taps on the secondary does not give rise to any particular overload difficulties: it is only necessary to comply with the previously given instructions relative to thermal dissipation (sub-section 2.1), and operation on inductive load (Sub-sections 1.5 and 2.3), particularly when the load on the secondary is a rectifier.
When switching the primary connections (figure 19 a), applying power at a random instant can entail destructive current surges. Such current surges have two origins:

building up of the magnetizing current to a value twice that of the transformer nominal current,

remanence of the magnetic circuit consecutive to the preceding turn off, which can lead to its saturation when power is applied.

To avoid these two difficulties, it would be advisable to control the triac at the maximum of the supply voltage, and at a polarity of this voltage opposite to that in which the transformer remained at the preceding turn-off. Unless the switching of the primary of a transformer of very high induction is concerned, such a sophisticated control circuit is not required, as a general rule, and the following recautions may be sufficient:

In the case of phrase control, or when there are no difficulties due to interference from the environment, proceed to a starting up at progressively increasing conduction angle. Figure 20 illustrates the example of a simple controller. Progressive energization is achieved at the opening of switch S through the charge of capacitor C (2 to 10 µF, 100 V), potentiometer P is used for ower adjustment in normal operation.

For on-off control at the zero voltage point, carry out the first firing of the triac at the beginning of a half wave whose polarity is opposite that of the half wave at the end of which the triac has ceased conducting.

In any case, these cares will be illusory if no precautions (as described in sub-section 2.4) are taken against untimely triac firing on violent interference or mains overvoltages occuring at any instant.
Anyway, it is recommended, for these applictions, to use preferably "alternistors" of a rating overdimensioned with respect to the continuous-duty nominal current, and to protect the circuit by means of fast-acting fuses (refer to sub-section 2.2).

Figure 19 : Switching with Triacs on the Primary (a), or Secondary (b) of a Transformer.

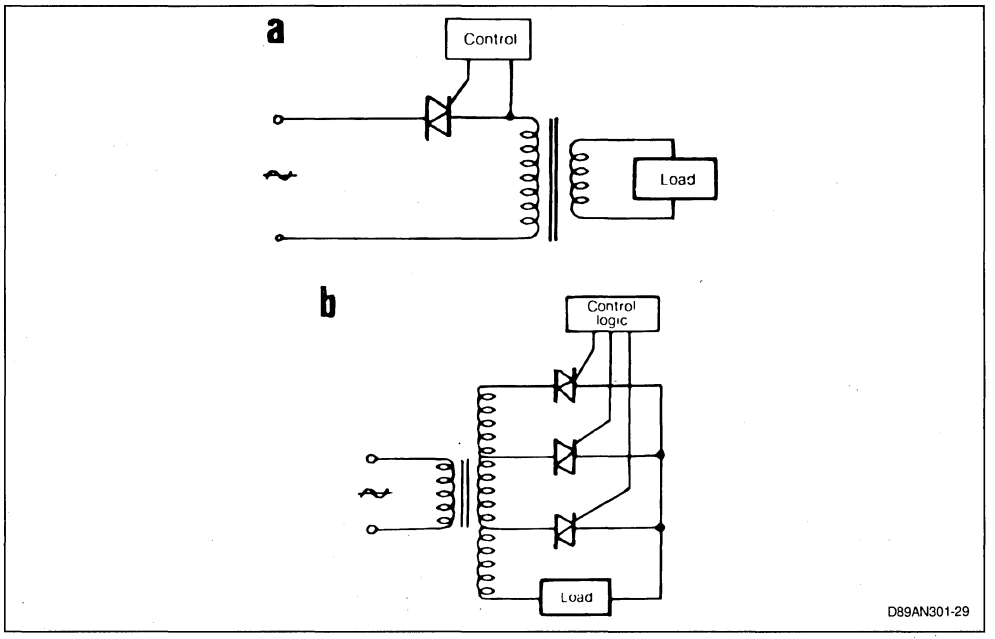
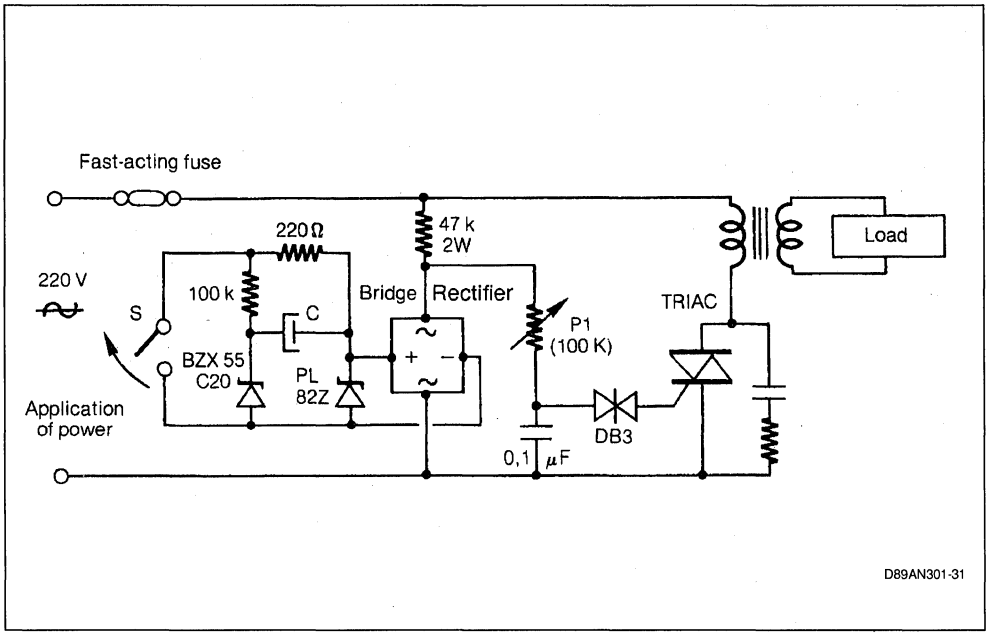


Figure 20 : Diac Controller with Progressive Energization of the Transformer.



CONCLUSION

The triac is a AC switch which changes from the blocked to the conducting state when a current or current pulses of any polarity are applied to the control electrode. Turn-on of the device can be achieved with precision in synchronism with the AC input voltage, while turn-off occurs when the current passes through zero following the control signal removal.

This permits setting up systems for the switching, variation or regulation of the power delivered to any load (lamp, resistor, transformer, motor). Provided an appropriate heat sink keeps the junction temperature below the specified maximum value, the service like of the triacs used in these systems is almost unlimited.

Owing to the remarkable overloads capabilities of the triacs, users will but exceptionally experience difficulties as regards the reliability of these devices. We have insisted on the various cases of applications requiring particular precautions, in order to give all the information necessary to solve possible problems in the best possible way. Appendix I sums up all useful instruction, in relation with the parameters specified by the individual datasheets.

APPENDIX

RELATIVE CONSIDERATIONS TO A FEW TRIAC UTILIZATION PARAMETERS

Parameters	To be Particularly Consideredfor	Precautions to be Taken (together or separately)
1) Thermal Stresse **I_{TRMS}: Triac Nominal Current** (rms current at 80 °C case temperature). **$R_{th(jc)}$: Junction/case Thermal Resistance;** see Sub-section 2.1	**Continuos Operational ITeff in High Ambient Temperature t_{amb}** **Permanent Operation at Small Conduction Angle, with High Peak Currents** **Operation with High-frequency ac Input Voltage**	**Suitable Heat Sink** Its thermal resistance with respect to t_{amb} should e at the most: $\frac{Tj - t_{amb}}{P} - R_{th(jc)} - R_{tj(cd)}$ With: P = Dissipated power : fig. 3, 4 Tj = max. permissible junction temperature : see Sub-section 2.1 and 4) below (untimely firing)
2) Current Stresse **I_{TSM}: non repetitive peak overload current** (peak current permissible during one period only) **di/dt: critical rate of rise of the current** at turn-on; see Sub-section 2.2	**- Capacitive Load** (or capacitor across the triac terminals) **- Utilization on Incandescent Lamps** (high current inc old condition) **- Windingson Saturable Core,, transformer primary** (magnetizing current) **- Risk of Short-circuit on Load** **- Risk of Untimely** firing occuring on overvoltages (see 4) below	**- Inductive Circuit** (addition of L higher than a few hundreds of µH); see figure 13 **- At least 30 Ω** in series with **possible capacitor** **- Triggering at zero voltage point** **- Triggering through gate pulse of steep leading edge,** with peak much higher than specified I_{GT} **- Non-delayed fuse** rated for less than 2/3 of triac I_{Teff}
3) Holding of Firing Instantaneous output value (current in load) below which the triac turns off (I_H) or does not steadily fire (I_L) after the removal of the gate current (see Sub-section 1.3) a) at End Conduction: holding Current I_H b) at Beginning of Conduction: Latching Current I_L	**- Highly Variable Loads** (low currents) **- Highly Inductive Loads** (see fig. 7) **- Presence of an LC Resonant Circuit** (for instance, underdamped interference filter)	**- Long trigger pulse** or long trains of closely spaced pulses **- RC network across triac terminal** (see fig. 15) **- Triac of Low IH** (sensitive series)
4) Untimely Firing **a) Firing through breakower** (through momentary over-shooting of the maximum specified voltage V_{DMW}; see sub-section 2.3) **b) Firing by dv/dt** (critical rate of rise of the voltage in the blocked state-parasitic triac firing, without gate signal, by a voltage wavefront acting on the triac terminals **c) Commutating dv/dt** (critical rate of rise of the voltage at commutation-see fig. 11); spontaneous triac re-firing through the voltage slope on inductive load at the end of a current half wave	**- High Mains Interference** **- Atmospheric Interference** **- Commutator-type Motors, intermittent contacts** **- Under-dimensioned heat sink** **- High Input Voltage Frequency** **- Forced commutation, rectifiers switch inductive load**	- Limit Junction Temperature (largely dimensioned heat sink); **- ALTERNISTOR** **- RC Network on Triac Terminals**

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

THYRISTORS AND TRIACS, AN IMPORTANT PARAMETER : THE HOLDING CURRENT

By E. Leblanc

The purpose of this note is to familiarize the user of a triac (or a thyristor) with the parameter I_H : hypostatic current or holding current.

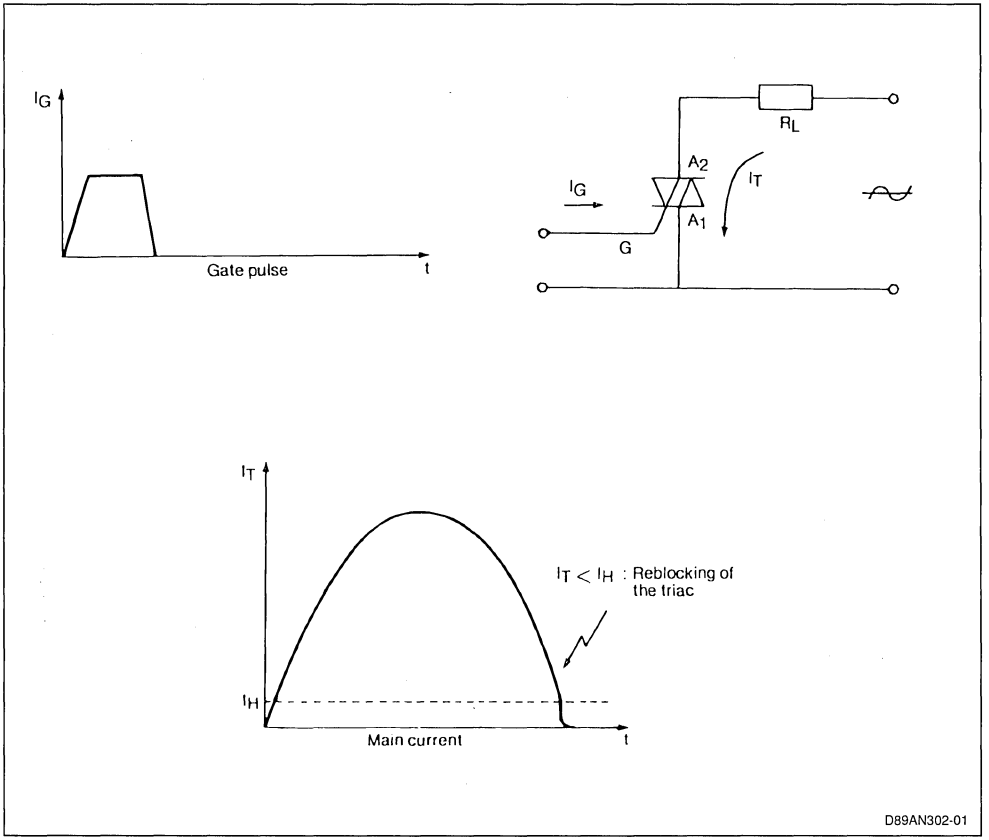
After a short definition, we will illustrate the importance of this parameter by concrete examples. Then we will describe how to measure it and finally its variation with the conditions of use and the sensitivity of the components.

In all cases we speak of triacs. However, the statements are also valid for thyristors.

DEFINITION

To keep an electromagnetic relay in the conducting state, it is necessary for a minimum current to circulate in its coil. Otherwise it would return to the blocked state. The same phenomenon can be observed for a triac. This minimum current which keeps the triac conducting is called the hypostatic or holding current (figure 1).

Figure 1 : Controlled by gate pulse I_G, the triac is fired and a current I_T flows through it, fixed by the main circuit. When the current I_T falls below the triac hypostatic current I_H, it is reblocked.



APPLICATIONS

Example 1 : Light dimmer (figure 2).

Figure 2 : Dimmer with Interface Suppression Coil and Capacitor (RFI filter).

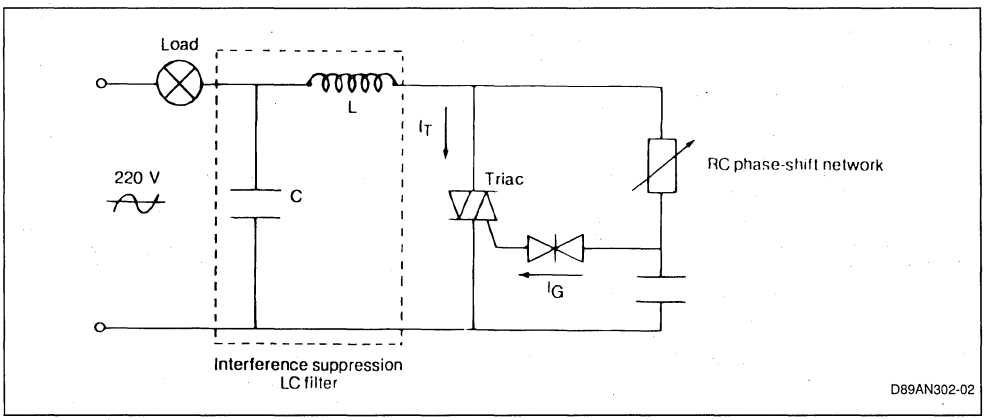
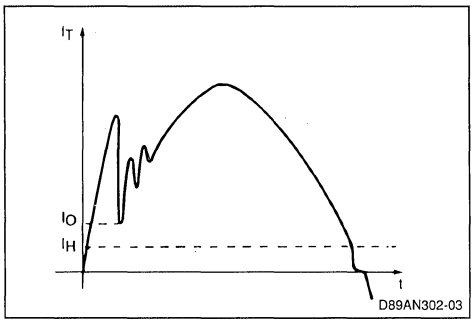


Figure 3 : Current in the dimmer triac :
The interference suppression filter produces oscillations. If $I_O > I_H$ (as in the figure) the triac remains fired. But if I_O falls below I_H, the triac will be blocked.



If the coil is a poor quality one, the oscillation is insufficiently damped. If the current in the triac falls below the hypostatic current, I_H, this results in untimely blocking of the triac. It is fired at the next current pulse I_G and is blocked again. The lamp flickers. This is known as the "flicker effect".

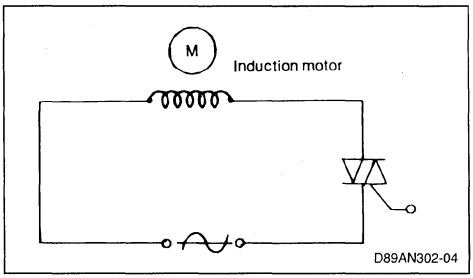
How can it be prevented ? By eliminating the cause, i.e. using an appropriate interference suppression filter which does not produce extensive oscillations, and then by choosing a triac with a lower hypostatic current I_H.

SGS-THOMSON Microelectronics has developped a triac specially designed for applications where a low hypostatic current I_H is required, the BTA 06 400 GP.

This device is specified with a maximum holding current I_H of 13mA in both current flow directions.

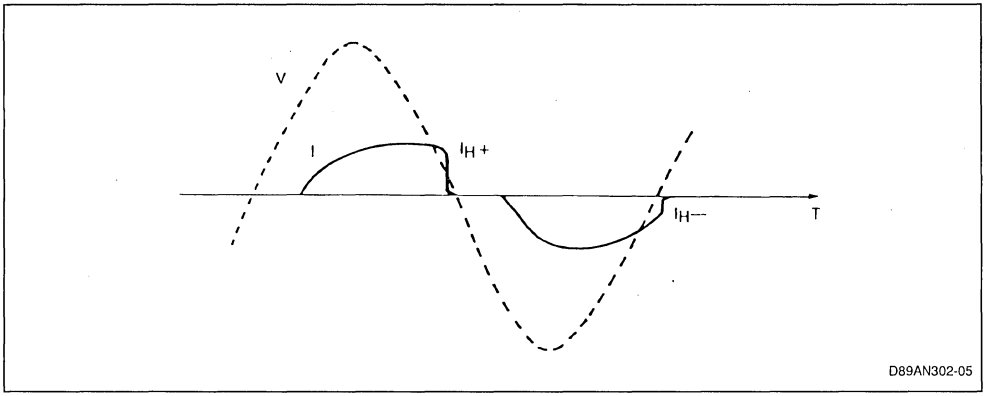
Example 2 : Motor Control (figure 4).

Figure 4 : Control of a Small Motor by Triac.



The designer wishes to control a small high-impedance motor (2500ohms for example) by triac. He obtains the parts and an operating manual and carries out tests. The circuit operates smoothly. After one year of production, the manufacturer complains of low torque in his motor and blames the triac. What's happened ?

Figure 5 : Voltage Accross the Triac and Current in the Circuit of Figure 4.



The circuit was designed with a type of triac whose maximum specified holding current I_H was 50mA. But the components used for the tests were more sensitive : $I_H+ = 13mA$ and $I_H- = 8mA$ and the designer based his choice on these results. After a year of delivery, the component manufacturer continues to deliver parts which are in conformity with the specification but less sensitive : $I_H+ = 40mA$ and $I_H- = 20mA$. The conduction time decreases *(figure 5)*, the dissymmmetry is greater, a DC component appears and the motor loses torque.

To prevent this kind of difficulty, when designing the circuit it is thus necessary to take into account not the typical value of the sample used but the maximum value specified by the component manufacturer.

Example 3 :

Take the diagram of the previous example *(figure 4)*, the control of a small high-impedance motor by triac.

This time, the designer selects a triac with a lower maximum specified holding current, I_H. The motor seems to operate without problems. The motor is meant for mounting on out-door equipment. The equipmynt is installed in summer and works well. But in winter, the fault described above occurs. What has happened ? The designer studied the operation of his circuit at an ambient temperature of 25°C. But the holding current I_H varies with the temperature : when the temperature decreases, the holding current increases (we will study this variation in paragraph 4.6) and the phenomenon described in example 2 occurs.
Thus when designing a circuit which is to operate at low temperatures, it is essential to take into account the corrected value of the holding current and not its value at an ambient temperature of 25°C.

These three examples illustrate the importance of this parameter and the different problems it can cause in a circuit if it is insufficiently known.

If the device is to remain in the conducting state, it is imperative that the circuit in which it is used ensures a current higher than the holding current I_H of the device.

In our data sheets, for all the types of triacs, the hypostatic current I_H is specified as a maximum value. A suitable triac should then be chosen whose holding current I_H is lower than the minimum value of the current in the circuit, if the triac is to remain in the conducting state ; make the necessary corrections to compensate for temperature variations.

MEASUREMENT OF THE HYPOSTATIC CURRENT I_H

Pushbutton P is used to fire the triac. The value of current I_T is chosen much higher than the latching current. By increasing the value of the variable resistor R, current I_T will decrease. The value of the hypostatic current I_H is the value of I_T read just before the triac is blocked.

The hypostatic current I_H is always measured with the gate unconnected, i.e. disconnected from the trigger circuit. Only sensitive thyristors ($I_{GT} \leq 500\mu A$) are measured with a 1kohm resistor connected between gate and cathode.

For the measurement to be regularly repeatable, the triac should be suitably fired. The following rules should be observed :

- Before decreasing current IT, it should be equal to at least 5 times the triac I_L current.

Example : BTA 12 600C

I_L typ (QI and III) = 20mA thus I_T = 500mA.

- if the I_H current is measured by pulses (automatic testers, for example), the triac should consult for at least 500µs before performing the measurement.

For a triac, the IH current has two values : (I_H +) when electrode A2 is positive with respect to electrode A1 and (I_H –) when electrode A2 is negative with respect to electrode A1. In the documentation only one value is given for both quadrants. This value is always the maximum value.

Example : BTA 12 600C : $I_{H\,max}$ = 25mA.

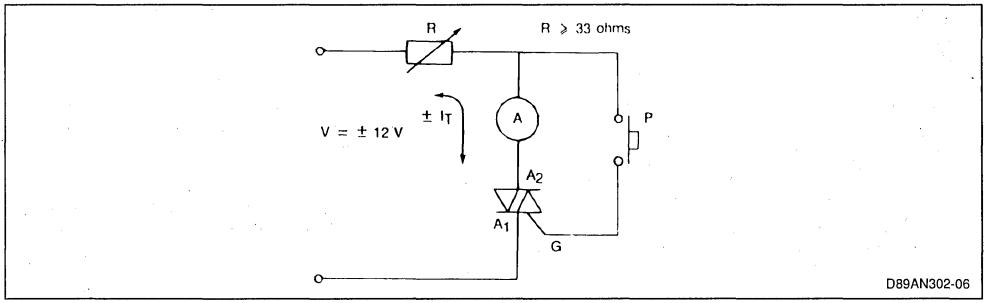
Depending on the production batch, I_H can vary. However, the dispersion remains below the limits specified in the catalogue.

To give an idea of this dispersion :

- Sensitive triacs : I_{GT} (QI) 5mA (type T) : 2mA ≤ I_H ≤ 8mA (Specified $I_{H\,max}$: 15mA).
- Standard triacs : I_{GT} (QI) 50mA (type B) : 8mA ≤ I_H ≤40mA (Specified $I_{H\,max}$: 50mA).

Note : The minimum value of the I_H parameter is never specified in the data sheets.

Figure 6 : Circuit for Measurement of the Holding Current I_H.



VARIATION OF THE HOLDING CURRENT, I_H

a) Variation of current I_H with the sensitivity of the devices and the direction of conduction (typical value)

For low components (thyristors and triacs whose rated current is less than 60A), the hypostatic current, I_H, is related to the firing current, I_{GT} (see figure 7).

Figure 7 : Ratio between the Holding Current, I_H (A2 +) and Current I_{GT} (QI) for Sensitive and Standard Triacs.

	I_H +/I_{GT} (Q1)
Sensitive triac 6 A_{rms} (T type)	3
Standard triac 12 A_{rms}(C type)	1.5

Example 1 :

BTA 06 600T : if I_{GT} (QI) = 1.5mA then I_H + = 4.5mA.
BTA 12 600C : if I_{GT} (QI) = 10mA then I_H = 15mA.

In the case of the triac (as distinguished from the thyristor) it is important to note that current I_H – (electrode A2 negative with respect to A1) is generaly lower than I_H + (see figure 8).

Figure 8 : Ratio between Holding Current I_H + (A2 +) and Holding Current I_H – (A2 –) for Sensitive and Standard Triacs.

	I_H + / I_H -
Sensitive triac 6 A_{rms} (T type)	1.2
Standard triac 12 A_{rms} (C type)	1.2

Example 2 :

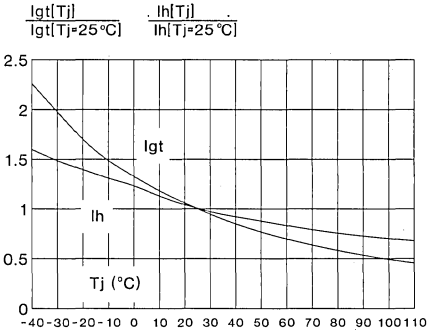
BTA 06 600T : if I_H + = 4.3mA, I_H – = 3.8mA.
BTA 12 600B : if I_H + = 15mA, I_H – = 12.5mA.

b) Variation of the hypostatic current, I_H, with the junction temperature :

The value of the hypostatic current is physically related to that of the firing current, I_{GT}. These two parameters thus vary with the junction temperature in accordance with an analog law *(see figure 9)*.

Example : Triac TO 220, type BTA 12 600C
I_H = 20mA at Tj = 25°C,
thus I_H = 14mA at Tj = 110°C.

Figure 9 : Relative Variation of the Holding Current I_H, with the Junction Temperature, Tj (typical values).



c) Influence of the reapplied voltage :

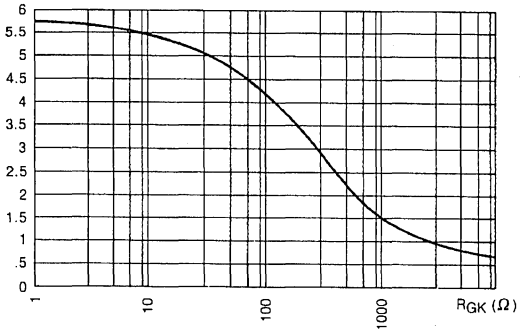
The rise time and the level of the reapplied reverse voltage across the triac after blocking have no influence on the value of its holding current, I_H.

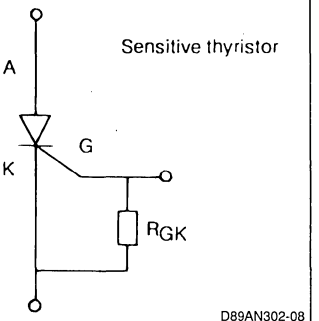
d) Influence of the external gate cathode resistor, R_{GK}

The user can wire a resistor, R_{GK}, between the gate and the cathode of the component, either to improve its behaviour under voltage at high junction temperatures (by-pass for leakage current) in the case of sensitive thyristors, or because it forms part of the fliring circuit. This resistor has an influence on the holding current, I_H, in different proportions depending on its resistive value and the sensitivity of the components :

1 - Sensitive thyristors ($I_{GT} \leq 500\mu A$)
Resistor R_{GK} connected between the gate and the cathode *(figure 10)* has an important influence on the I_H parameter of sensitive thyristors. For certain applications, the designer would be well-advised to define a high impedance control circuit.

Figure 10 : Variation of the Hypostatic Current, I_H, of a Sensitive Thyristor (e. g. TLS 106-6) as a Function of the Gate-cathode Resistor (typical values).





Note : The hypostatic current for sensitive thyristors is always specified for R_{GC} = 1000ohms.

2 - Standard thyristors, sensitive and standard triacs

A resistor between gate and cathode on one of these components has no significant influence on the value of its holding current, I_H (on condition that it is not too low, R_{GC} > 20ohms).

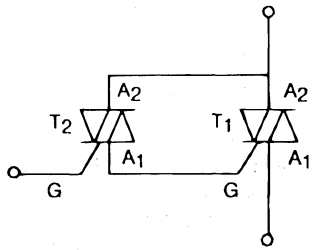
e) Note :

We have seen that the more sensitive the triac (Low I_G), the lower the value of the holding current, I_H.

Now, in certain applications, a sensitive triac (direct control by integrated circuit) with a high I_H (or I_L) may be useful.

In this case, the circuit of *figure 11* could be used. The assembly is sensitive but has a higher hypostatic current.

Figure 11 : This Component, a «DARLINGTON TRIAC» combines a High Sensitivity with a High Hypostatic Current.



T_1 : standard triac

e. g. BTA 12 600B I_{GT} (QI) ≤ 50mA

I_H + ≤ 50mA

T_2 : sensitive triac

e. g. TLC 336T I_{GT} (QI) ≤ 5mA

I_H + ≤ 15mA

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CONCLUSION

The choice of a thyristor or a triac does not depend only on the voltage, the rated current and the sensitivity. Other parameters should be taken into account.

The hypostatic current, I_H plays an important role in many circuits.

The value of this parameter varies with :

- dispersion of characteristics at manufacture,
- temperature,
- eventually the control circuit (in the case of sensitive thyristors),
- the direction of current flow.

Taking into account these elements, the designer can obtain satisfactory operation of his circuit in industrial real life applications.

Knowing the problems which could be created by this parameter, SGS-THOMSON Microelectronics has introduced a new triac, BTA 06 400 GP, now available for the designers. Its low holding current, specified with a maximum value, enables it to be used in most applications.

LATCHING CURRENT

By E. Leblanc

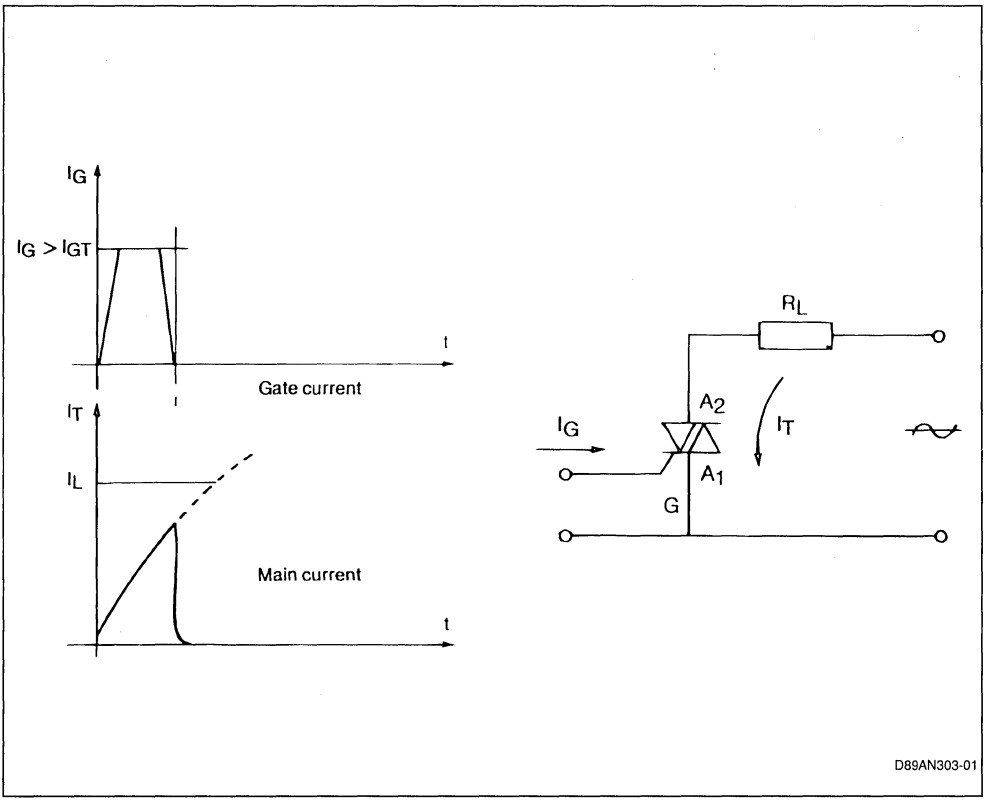
An important problem concerning the utilization of components such as thyristors or triacs is the holding of the component in the conducting state after the trigger current has disappeared during firing. Very often, the firing problems supposedly due to the gate current I_G or to the firing time t_{GT} are in reality due to the latching current I_L.
After a definition we will illustrate the importance of this parameter by concrete examples. Then we will describe how to measure it and its variation according to the utilization conditions of the components.

The study will be based on the triac. The points treated are valid for thyristors (except for the various conduction modes).

DEFINITION

The latching current, I_L, of a triac is the minimum value of the main current (current flowing between electrodes A_2 and A_1) which enables the component to remain in the conducting state after the gate current I_G has ceased (*Figure 1*).

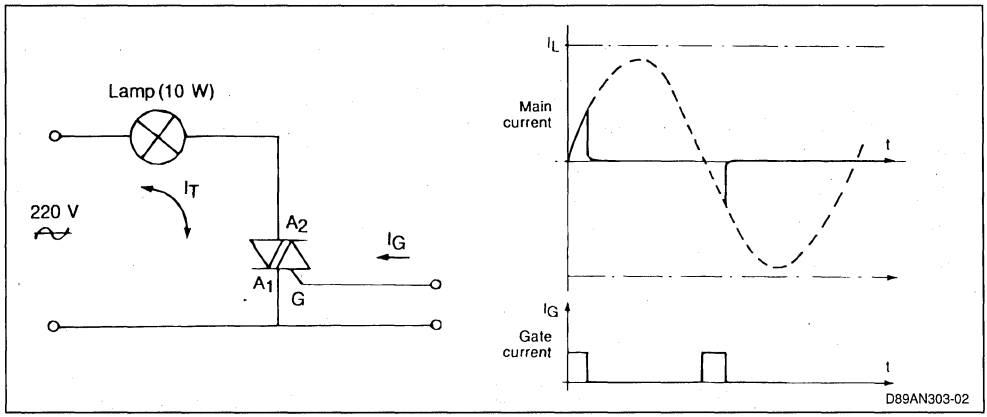
Figure 1 : Controlled by the gate pulse, I_G, the triac is fired, and a current I_T flows through it, imposed by the main current. If the gate current I_G is stopped before current I_T reaches the value of the latching current I_L, the triac is blocked (as shown in the figure).



APPLICATIONS

Example 1 : Control of a low power signalling lamp by triac.

Figure 2 : Control of a Low Power Signalling Lamp by Triac.

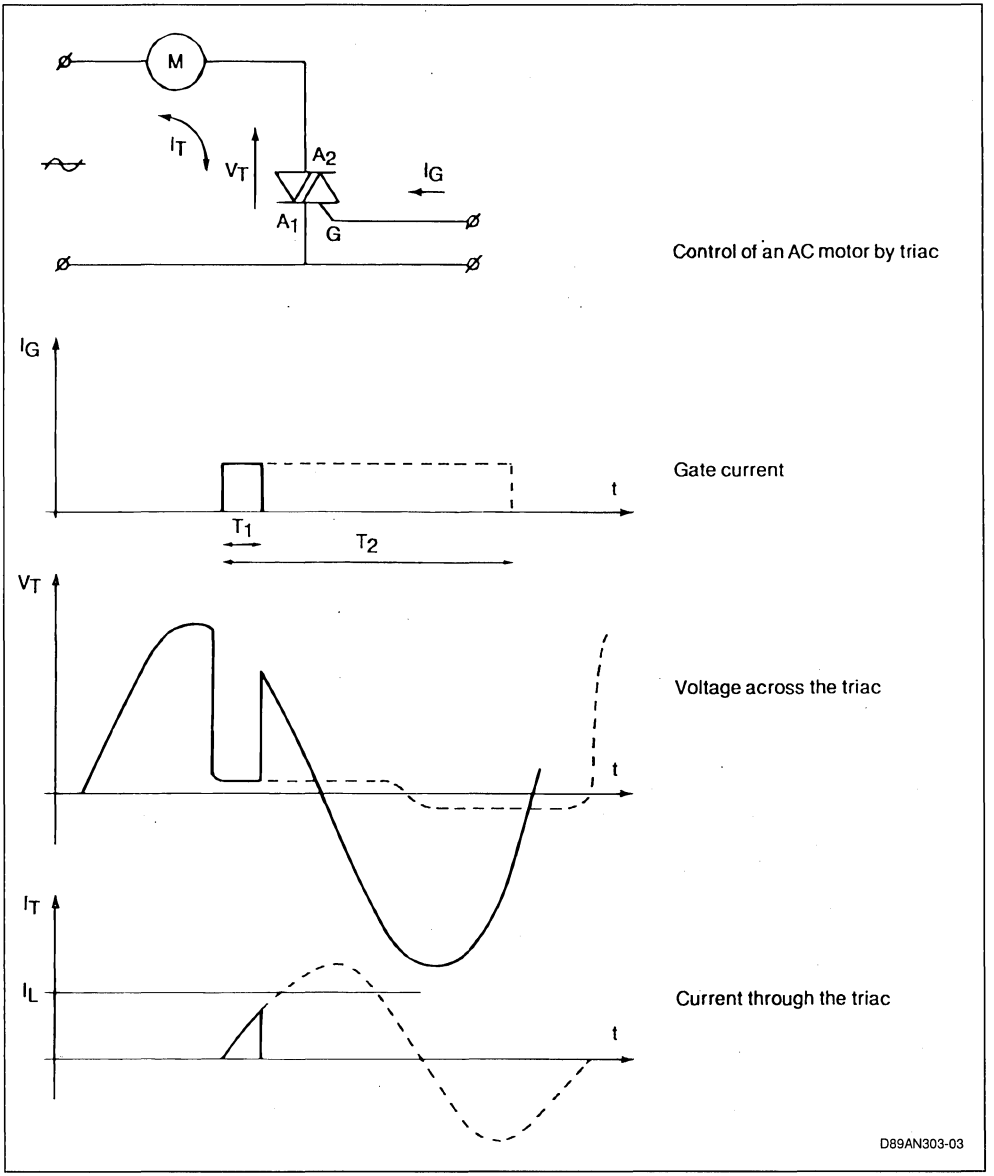


Current in the main circuit of the triac and gate current. The lamp power is too low (eg. : P ≤ 10 W and the triac BTA 12.400 B) to impose a sufficient current (shown in dotted lines in the diagram) in the triac to keep it in the conducting state after interruption of the gate current I_G. The triac does not conduct.

A BTA 12.400 B triac is used to control the flashing of a 10 W signalling light. The peak current in the circuit will therefore be 65 mA. This value is very close to that of the typical latching current given in the data book for this type of triac : 50 mA (quadrant 1, 3 and 4). Thus the user's case could be that described in figure 2, that is, a triac whose latching current I_L in the first quadrant is equal to 70 mA. His triac will never be fired. For correct operation, the user should thus employ a sensitive triac (e.g. T08-6A I_L : 8 mA).

Example 2 : Control of an inductive load by triac.

Figure 3 : Voltage Accross and Current Through the Triac.



In continuous lines : short gate signal : the triac does not remain in the conducting state because the main current did not reach the value of the triac latching current before suppression of the gate current.

In dotted lines : long gate signal : the triac is fired and remains in the conducting state until its current falls below the holding current I_H after suppression of the gate current I_G.

On a highly inductive load, the inductance limits the current rise time to :

$$\frac{dI_T}{d_t} = \frac{Va}{L}$$

(Va : power supply voltage at the time the gate signal is applied ; L : load inductance).

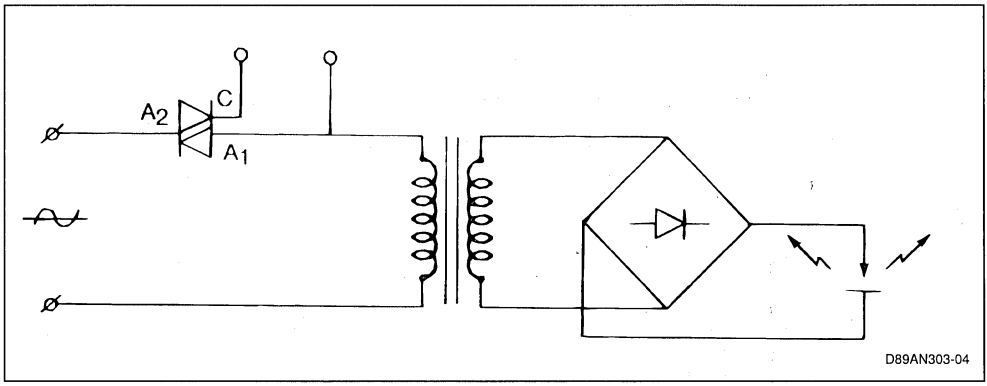
Consider the operation on one full-wave of the power supply voltage. If the duration t_1 of the gate current pulse I_G is very small compared with a half-wave of the power supply voltage, the triac current cannot reach the triac latching current level in the firing mode considered (here the 1st quadrant). Thus firing will not take place and the voltage across the triac increases. For triggering to be steady, the duration of pulse t_2 should be long when compared with a half-wave of the power supply voltage. The current set up in the triac is imposed by the load impedance. The triac remains in the conducting state until the current falls below the holding current I_H. It is blocked if the I_G current pulse has ended.

Another method consists of applying a train of closely spaced pulses to the triac gate instead of a square wave.

The SGS-THOMSON Microelectronics applications laboratories have developed a number of triac control circuits, specially designed to work on inductive loads (see bibliography, ref. N° 1).

Example 3 : Control by triac of a load whose power varies considerably.

Figure 4 : Control of an Arc Welding Set by Triac.



The designer of an arc welding set whose power is adjustable by triac, chooses a component capable of controlling high currents. For example, if the maximum current to be controlled is 40 A_{rms}, the designer, for safety, will choose a triac rated at 60 A_{rms}, thus a triac with a high latching current. Now, off-load, the transformer magnetizing current could be very low or even below the triac latching current I_L in one of the quadrants. This means that the triac could fire correctly in the first quadrant and then not fire if the next firing is to take place in the second quadrant where the I_L is much higher. A considerable unbalance then occurs, generating a DC current heating the transformer and preventing the equipment from operating correctly.

Since the latching current I_L increases with the size of components, and thus with their rating, the user would thus be well advised not to select an excessively high rating for his triac in order to have the lowest possible latching current.

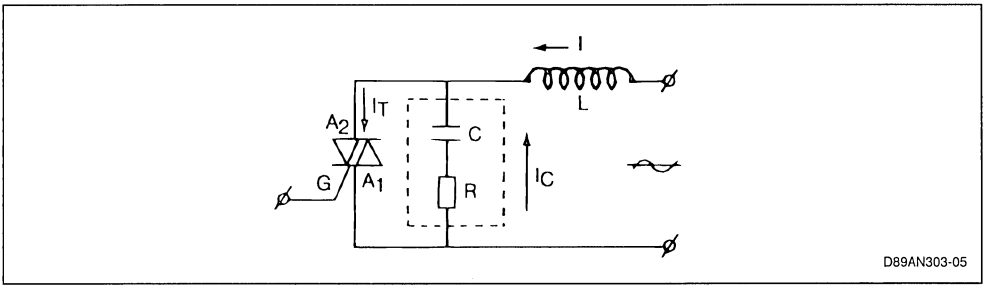
A.N : For this type of application, the SGS-THOMSON Microelectronics applications laboratories place at the disposal of designers a number of schematics meant for this type of circuit (see bibliography, ref. N°1).

These three examples illustrate the importance of the I_L parameter and the problems that it can cause in a circuit. To ensure stable firing of a triac or a thyristor, it is absolutely necessary for the circuit which is controlled to impose a current which is higher than its latching current.

FAVORABLE EFFECT OF AN RC CIRCUIT ON THE FIRING OF A THYRISTOR OR A TRIAC

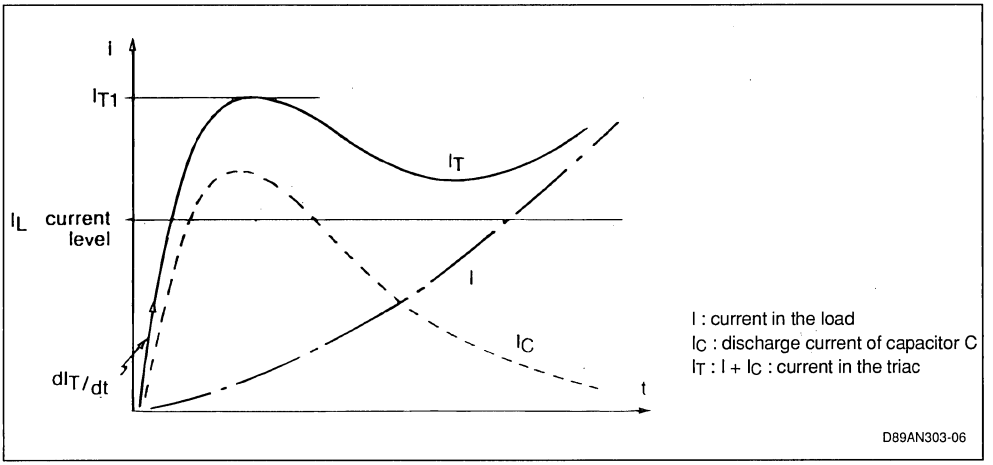
In most inductive load applications of triacs or thyristors, the user connects an RC network between the anode and cathode of the device to eliminate the risk of premature firing by transients or spontaneous firing by (dv/dt)c (case of triacs) (*see figure 5*). Capacitance C and the load impedance attenuate steep voltage transients transmitted by the mains or resulting from switching inductive loads.

Figure 5 : Reducing the Risk of Untimely Firing on Inductive Loads : the RC Circuit (called « Snubber »).



This RC network has also a second advantage. In fact, the energy accumulated in capacitor C after turning off is fed back to the triac when firing. The speed at which the current increases in the triac during discharge of the capacitor is then limited only by the peak charge voltage of the capacitor and the inductance of the circuit connecting the SNUBBER to the triac. The current amplitude is the quotient of peak charge voltage of the capacitor by the series resis-tance R. This circuit thus helps the current to rise very quickly above the latching current I_L of the device (*see figure 6*).

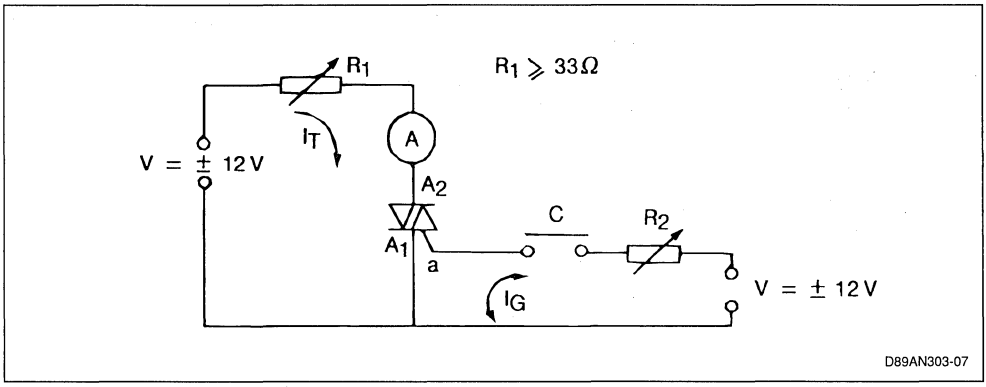
Figure 6 : Favorable Effect of the RC Circuit for Firing on a Highly Inductive Load.



Note : When using an RC circuit, it is not advisable to work with a series resistance R which is too low. In fact, the combined effect during firing of I_{T1} (*figure 6*) (equal to the quotient of the capacitor peak charge voltage and resistance R) and the current slope dI_T/dt (equal to the quotient of the capacitance charging voltage by the inductance of the connection between the triac and the RC circuit) could be dangerous for the triac. A value for R higher than 100 ohms is recommended.

LATCHING CURRENT (I_L) MEASUREMENT

Figure 7 : Latching Current (IL) Measurement Circuit.



The closing of contact C enables passage of the gate current whose is selected higher than that of the triac firing current, I_{GT} to be measured. By gradually decreasing the value of resistance R_1, while continuing to transmit pulses of gate current I_G, the main current I_T is increased. As long as the value of the I_T current is lower than that of the device latching current I_L, the device does not remain in the conducting state. The value of the latching current I_L is the value of the I_T current read as soon as the triac remains on, after suppressing the gate current I_G.

Only sensitive thyristors ($I_{GT} \leq 500\ \mu A$) are measured with a 1 KΩ resistor between gate and cathode.

Parameter I_L varies with the width of the gate current pulse I_{GT} and its level. For the measurement to be reproduced correctly, the following rules should thus be observed :

Fix a sufficiently wide control pulse I_G. The width of the pulse should be at least equal to 1 ms.

Impose a gate current I_G sufficiently high with respect to that of the triggering current I_{GT} of the device to be measured.
An $\frac{I_G}{I_{GT}}$ ratio higher than or equal to 1.2 is advisable.

Example : BTA 12.600 C
I_{GT} max (Q IV) = 50 mA therefore
I_G = 60 mA

In the case of a triac, there are four latching current I_L values that correspond to the four quadrants of triac operation :

- (I_L + +) when the electrodes A_2 and G are positive with respect to electrode A_1.

-(I_L + −) when electrode A_2 is positive with respect to electrode A_1 and electrode G is negative with respect to electrode A_1.

- (I_L − −) when electrodes A_2 and G are negative with respect to electrode A_1.

- (I_L − +) when electrode A_2 is negative with respect to electrode A_1 and electrode G is positive with respect to electrode A_1.

VARIATIONS OF LATCHING CURRENT I_L WITH THE UTILIZATION CONDITIONS

a) Variations of the I_L current with sensitivity of triacs and the various directions of conduction (typical values).

For the low power components (thyristors and triacs whose rated current is lower than 60A) the latching current I_L is dependent on the value of firing current I_{GT} (*see figure 8*).

Figure 8 : Ratio of the Latching Current IL in the Different Quadrants to the Triggering Current IGT in the First Quadrant, for Sensitive and Standard Triacs (typical values).

	$\frac{I_L (QI)}{I_{GT} (QI)}$	$\frac{I_L (QII)}{I_{GT} (QI)}$	$\frac{I_L (QIII)}{I_{GT} (QI)}$	$\frac{I_L (QIV)}{I_{GT} (QI)}$
6 Arms Sensitive Triacs (T type)	3.5	15	5	3
12 Arms Standard Triacs (B type)	2	5	1.5	1.7

Example 1 :

BTA 06.600 T : if I_{GT} (QI) = 1 mA
then : I_L (QI) ≈ 3.5 mA ;
I_L (QII) ≈ 15 mA
I_L (QIII) ≈ 5 mA;
I_L (QIV) ≈ 3 mA

and BTA 12.600 B if I_{GT} (QI) = 15 mA
then : I_L (QI) ≈ 30 mA;
I_L (QII) ≈ 75 mA
I_L (QIII) ≈ 22 mA ;
I_L (QIV) ≈ 25 mA

In the case of triacs, as opposed to that of thyristors, note that : as underlined in the table of *figure 8*, the current I_L + – (electrode A_2 positive with respect to electrode A_1 and electrode G negative with respect to electrode A_1 – QII) is much higher than the I_L current in the three other quadrants.

In the data sheets two values are specified : one value for quadrants I, III and IV and one value for quadrant II. In general these values are typical.

b) Relation between the latching current I_L and the holding current I_H

The holding current value I_H (see bibliography, note N° 2) is linked to the latching current value, I_L. By definition, the I_L current value will always be higher than the I_H current value.

The I_L / I_H ratio varies following the sensitivity of the triacs and their ratings (see figure 9).

Example 2 :

BTA 12.600 C : I_L typ = 40 mA QI, III, IV
I_L typ = 70 mA QII

Depending on the production batches, parameter I_L shows dispersion. Shown below are approximate values :

sensitive triacs :
I_{GT} (QI) ≤ 5 mA (type T):
QI, III, IV : 2 mA ≤ I_L ≤ 8 mA
QII : 10 mA ≤ I_L ≤ 40 mA

standard triacs :
I_{GT} (QI) ≤ 50 mA (type B):
QI, III, IV : 15 mA ≤ I_L ≤ 50 mA
QII : 50 mA ≤ I_L ≤ 120 mA

Figure 9 : Ratio of the Latching Current I_L to the Holding Current I_H Depending on the Sensitivity and Ratings of the Devices (typical values).

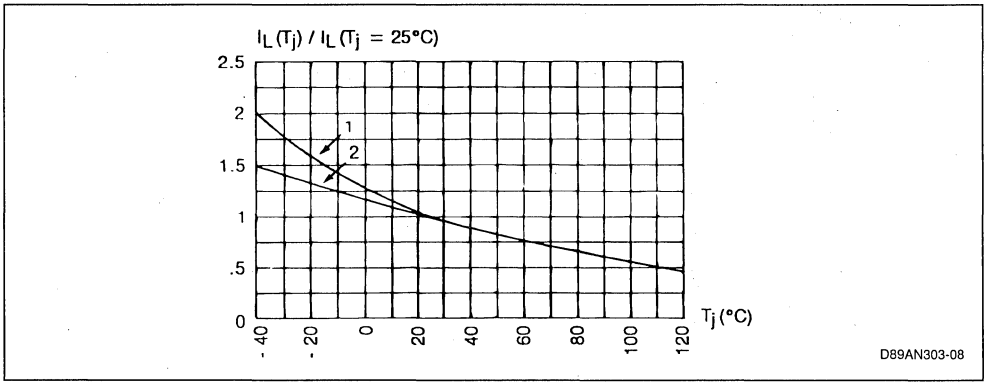
	Sensitive Triacs and Thyristors I_{RMS} ≤ 6 A	**Medium Power Thyristors and Triacs 6 A ≤ I_{RMS} ≤ 60 A**	**High Power Thyristors and Triacs 60 A ≤ I_{RMS} ≤ 300 A**
IL / IH (1)	1.1 to 1.5	1.5 to 2	2 to 5

(1) 1 st quadrant in the case of triacs.

c) Variations of the latching current I_L with the junction temperature.

The value of the latching current I_L is physically linked that of the triggering current I_{GT}. These two parameters therefore way analogously with the junction temperature (*see figure 10*).

Figure 10 : Relative variations of the latching current i| versus the junction temperature tj (typ. values).
1. Quadrant 2
2. Quadrants 1, 3 and 4.



Example 3 : Triac TO 220, type BTA 12.600 C

If I_L (QI) = 20 mA at Tj = 25 °C, then I_L (QI) = 30 mA at Tj = – 40 °C

d) Influence of the external gate-cathode resistor R_{GC}

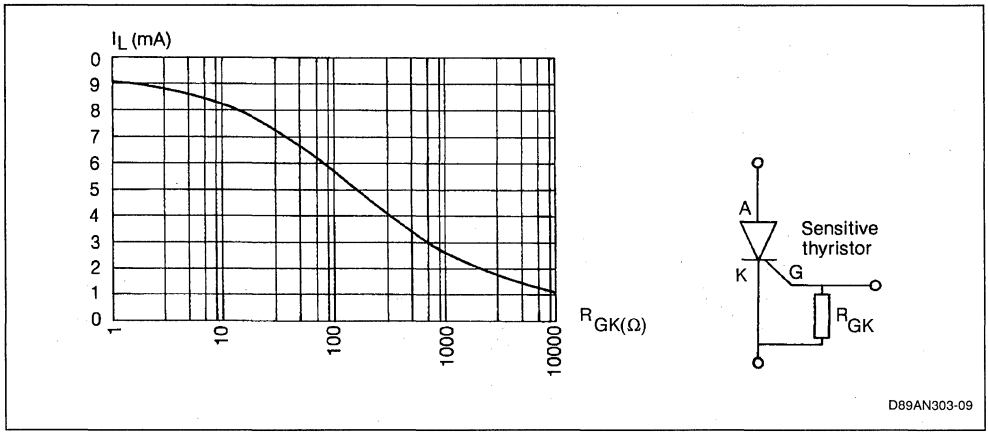
When using sensitive thyristors, the designer could wire a resistor R_{GC} between cathode and gate to improve their voltage capability at high temperatures (shunting of leakage currents).

This resistor affects the value of the latching current I_L in different proportions depending on its resistive value and the sensitivity of the component.

1. Sensitive thyristors (I_{GT} < 500 µA)

Resistor R_{GC} connected between gate and cathode (*figure 11*) has an important influence on the latching current I_L of sensitive thyristors. For some applications, the designer would be well advised to define a high impedance triggering circuit.

Figure 11 : Variation of the latching current I_L of a sensitive thyristor (e. g. TLS106-6) as a function of the gate-cathode resistance R_{GC} (typ. values).



Note : The latching current of sensitive thyristors is always specified with a 1000-ohm gate-cathode resistor.

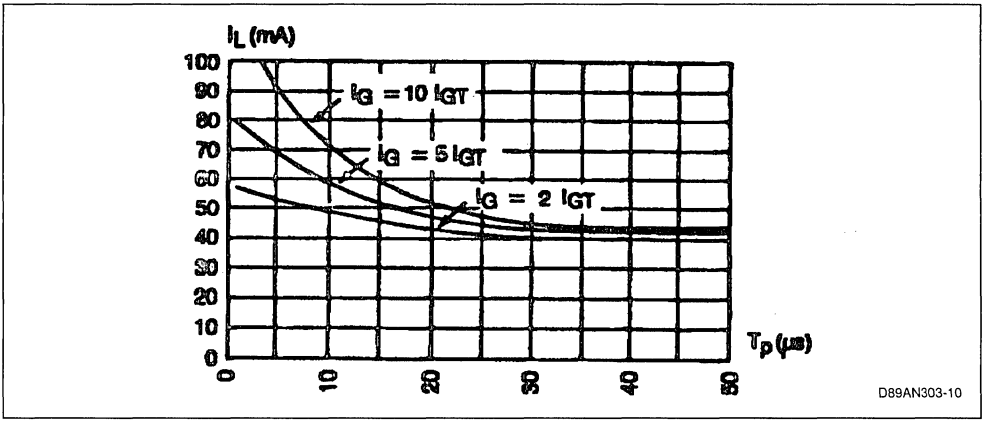
2. Standard thyristors, sensitive and standard triacs

A resistor connected between the gate and cathode of one of these components does not have a significative influence on the value of its latching current I_L (on condition that its value is not too low $R_{GC} > 20$ ohms).

e) Variation of the latching current I_L with the control conditions

The latching current I_L of a triac or a thyristor rated at less than 60 A_{rms} varies with the amplitude and the width of the triggering pulse I_G. With a constant pulse width(< 50 µs), an increase in the amplitude of I_G will lead to an increase in the latching current I_L and vice versa, if the amplitude of I_G is kept constant, a decrease in the width of the triggering pulse will lead to an increase in the latching current I_L that can even lead to an absence of firing of the device (*figure 12*).

Figure 12 : Variation of the Latching Current I_L versus the Width tp and the Level of the Gate Current I_G (represented here as a multiple of the triggering current I_{GT} of the triac under consideration) Triac BTB 16.600 B (quadrant 1) (typical values).



Negative biasing of the gate circuit (example : shape of the pulse in *figure 13a*) increases the latching current I_L in considerable proportions. If the decreasing speed dI_G/dt of the gate current is low (example : pulse shape of *figure 13 b*) (less than 0.5 A/µs) the value of the latching current approaches the holding current I_H.

Figure 13a : Gate Current Pulse with Negative Current at the end of the Pulse : Increase of the Latching Current IL.

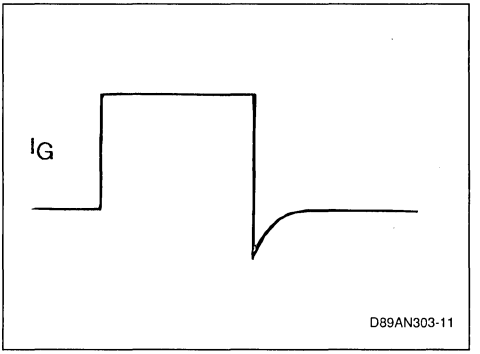
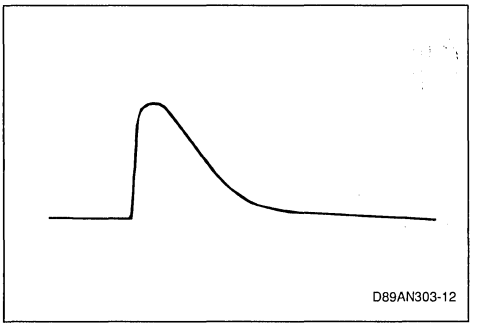


Figure 13b : Gate Current Pulse (diac controlled type) with tailing and without Negative Current : decrease of the Latching Current IL.



In order to obtain the lowest possible values for the latching current I_L, and thus ensure correct firing of the device, it is advisable to work with an amplitude of I_G equal to 1.2 I_{GT} and a width of the control current as high as possible. The firing technique using trains of closely spaced pulses ensures stable firing in total security. Control pulses with smooth tailing edges and without reverse current allo reducing the latching current.

CONCLUSION

The choice of a thyristor or of a triac does not depend only on the rated current, voltage and sensitivity. Other parameters also play an important part in the correct operation of a circuit and should be taken into account. The latching current I_L is one of these. Its value varies with :

- the way in which the device is controlled (shape of the gate pulse)
- the temperature
- the trigger circuit (case of sensitive thyristors)
- the direction of the current.

Triac and thyristor applications involving highly inductive loads or loads with considerable variations of controlled power are the main applications where the latching current I_L plays a determining role.

Taking these elements into account will enable the designer to obtain satisfactory operation of his circuit in industrial applications.

BIBLIOGRAPHIE

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2 - "Hypostatic current or holding current" by E. LEBLANC.

DESIGN OF A STATIC RELAY

By X. Durbecq

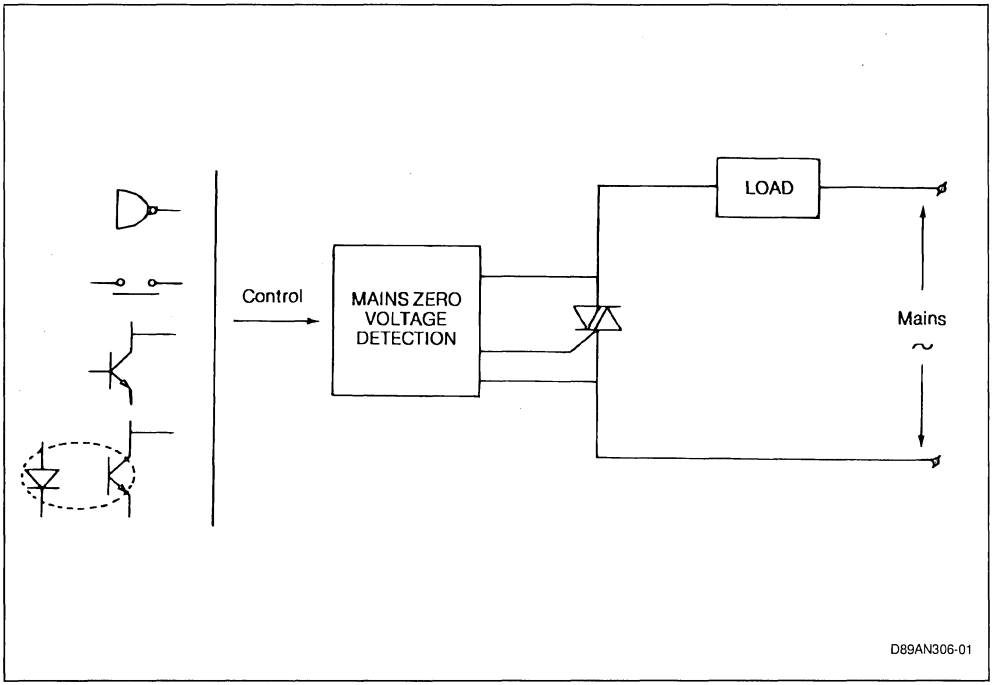
The switching of a resistive load on the mains generates electromagnetic disturbances whose level is in keeping with the voltage at the time of firing.
These disturbances can be reduced by switching on the load when the mains voltage approaches 0.
The convenience of firing control, the absence of rebound, and the response time of a semiconductor device enable designing static relays which guarantee this synchronous type of switching.
The "mains zero" detection function can be obtained by a circuit using discrete components.

This note provides a review of the principle of static relays as well as the method of calculation for the circuit component.

OPERATION A STATIC RELAY

The static relay consists of a power component, the triac, triggered by a circuit ensuring the functions of "mains zero" detection and interfacing with the input signal.

Figure 1 : Block Diagram of Static Relay.



OPERATING PRINCIPE

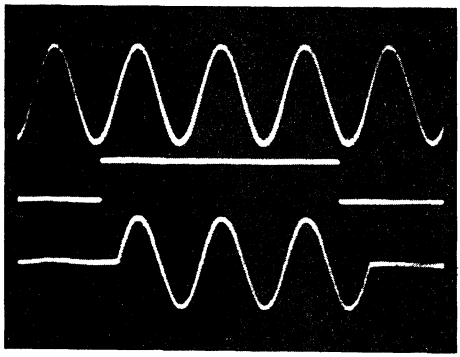
The firing of the triac can only take place when the mains voltage is close to 0 volt (± 30 V max).

For a long-duration input signal (> 10 ms), the triac is fired at the mains voltage zero. It continues to conduct for the full duration of this signal until the current drops to zero after disappearance of the input signal.

An input pulse (< 10 ms) should coincide with the passing through zero of the mains voltage to enable conduction of the triac (figure 2b).

Figure 2 : Synchronous Static Relay: Waveforms

Figure 2a : Long Duration Input Signal (> 10 ms).



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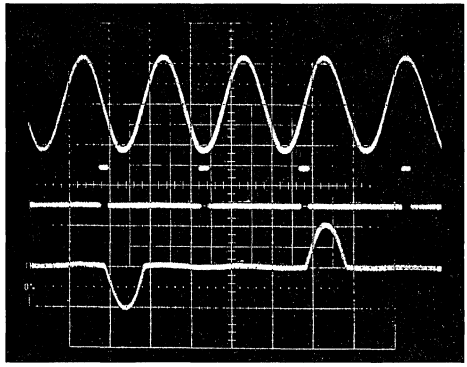
Mains voltage : V = 300 V/d.
Input signal : V = 10 V/d.
Mains current : I = 1 A/d.
T = 10 ms/d.

Figure 2b : Short Duration Input Pulse (< 10 ms).



D89AN306-02B

The triac is fired only when the input signal coincides with the passage through zero of the mains voltage.
Mains voltage : V = 300 V/d.
Input signal : V = 10 V/d.
Main current : I = 1 A/d.
T = 10 ms/d.

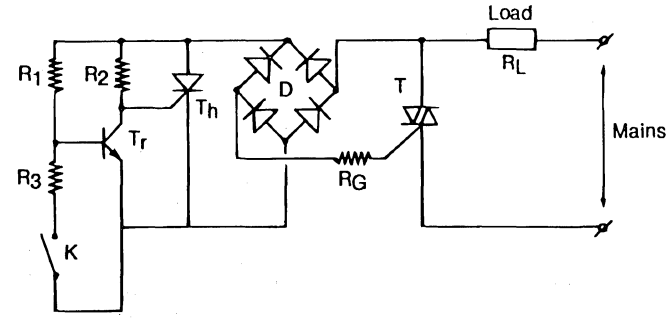
CHARACTERISTICS OF THE STATIC RELAY :

- Closing of the circuit when the mains voltage passes through zero (resistive and capacitive loads).
- Control of the static relay by very low signals (logic circuits, optocouplers, etc.).
- Insensitive to shocks and vibrations.
- High switching speed.
- No rebound.
- No electromagnetic disturbances.
- Opening of the circuit when the current passes through zero.

STATIC RELAY WITH DISCRETE COMPONENTS:

The triac triggering circuit consists of a transistor T_r and a sensitive thyristor T_h. This circuit is biased by the mains voltage after full wave rectification (figure 3).

Figure 3 : Schematic Diagram of a Static Relay with Discrete Components.



Triggering by closing control at mains zero voltage

D89AN306-03

OPERATION OF THE CIRCUIT :

Two distinct states can be observed :

1) Relay blocked : switch K open.

As soon as the mains voltage passes through zero, the current in resistor R_1 saturates transistor T_r, inhibiting the firing of thyristor T_h by shunting the gate current transmitted by R_2.

2) Relay fired : switch K closed.

The voltage divider composed of resistors R_1 and R_3 results in blocking of transistor T_r, as long as the mains voltage is lower than V_o (generally 30 V).

The current which flows through resistor R_2, passes through the gate of the thryristor.

The thyristor T_h can therefore be fired only during this time T_o, which defines the mains zero operating tolerance.

EQUATIONS OF THE CIRCUIT : Switch K closed.

1) Maximum firing time of triac, at the beginning of each half-period.

$$T_o = \frac{V_o}{V_{rms} \times \sqrt{2} \times \omega} \quad ; \quad \text{If } V_o << V_{rms}$$

2) Calculation of R_2. A sensitive thyristor is used.

E.g. TLS 106-4 :

I_{gt} max = 200 µA at 25 °C

$$R_2 < \frac{V_o - V_{gt}\ \text{max}\ (T_h)}{I_{gt}\ \text{max}\ (T_h)} \quad ; \quad P(R_2) = \frac{(V_{rms})^2}{R_2}$$

3) For R_3, a resistor of relatively low value (4.7 kohms) is used in order to sufficiently bias all the types of transistors which replace switch K.

4) Calculation of R_1 : switch K closed.

Transistor T_r is saturated only if the mains voltage is higher than V_o.

$$R_1 = \frac{\beta \times R_2 \times R_3 \times (V_o - 1)}{0.7 \times \beta \times R_2 + R_3 \times V_o} \quad ; \quad P(R_1) = \frac{(V_{rms})^2}{R_1}$$

The value of R_1 determines the tolerance on voltage V_o. The value selected for resistor R_1 is the standard value immediately above the calculated value.

5) Calculation of R_g

In order to have a gate current I_g sufficiently high to fire the triac, R_g is selected so that :

$$R_g << \frac{V_o - 4}{I_{gt}\ \text{max triac}} - R_L$$

ADVANTAGES

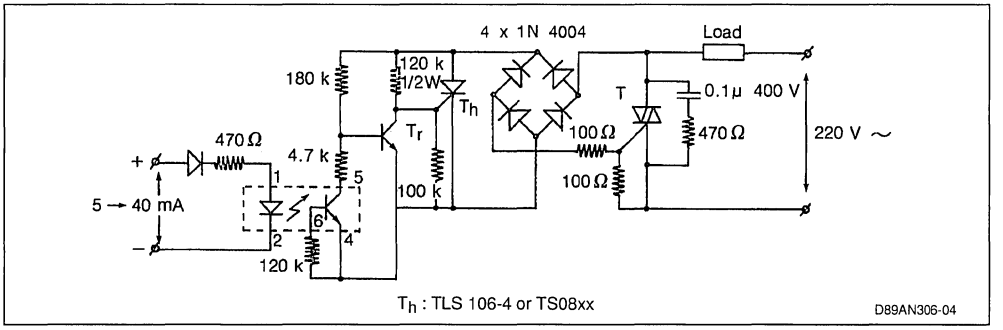
- Very low power dissipated in the control circuit. (< 500mW).
- Operation of the triac in quadrants 1 and 3 ensuring a good symmetry of the latching current I_L.
- High gate current available enables firing non sensitive triacs.

DISADVANTAGES

- Utilization of a sensitive thrysitor requires the use of an R.C. circuit across the triac, to prevent untimely triggering by transients transmitted by the mains.

EXAMPLE OF APPLICATIONS :

Figure 4 : Static Relay with Discrete Components and Isolated Control.



CONCLUSION

Using discrete components allows the design of simple circuits which achieve the synchronous static relay work.

Their main advantages are to provide a high gate current for the triac and to dissipate very low power.

USE OF TRIACS ON INDUCTIVE LOADS

By J. Bellin

Although triac circuits are now well known by designers. The use of these components for inductive loads requires certain precautions which should not be neglected of optimum use is to be made of them. That is the purpose of this article which reviews the various triac control modes and recalls the principles which guarantee its correct operation.

PHENOMENA OCCURING WHEN THE CIRCUIT IS CLOSED.

The triac is known as a component which is essential in controlling power from an AC source (mains).

In most cases, the circuit has an inductive component : either because of the nature of the load itself : motors, transformers, ballast inductance ; or because of the source impedance : utilization of the secondary of a transformer, length of the supply line, etc. On inductive loads, the operating conditions vary considerably, when closing the circuit, depending on the control mode (gate current, polarity and width) and synchronization of the firing. In order to build an optimal control circuit it is indispensable to analyse the various possibilities.

FIRING

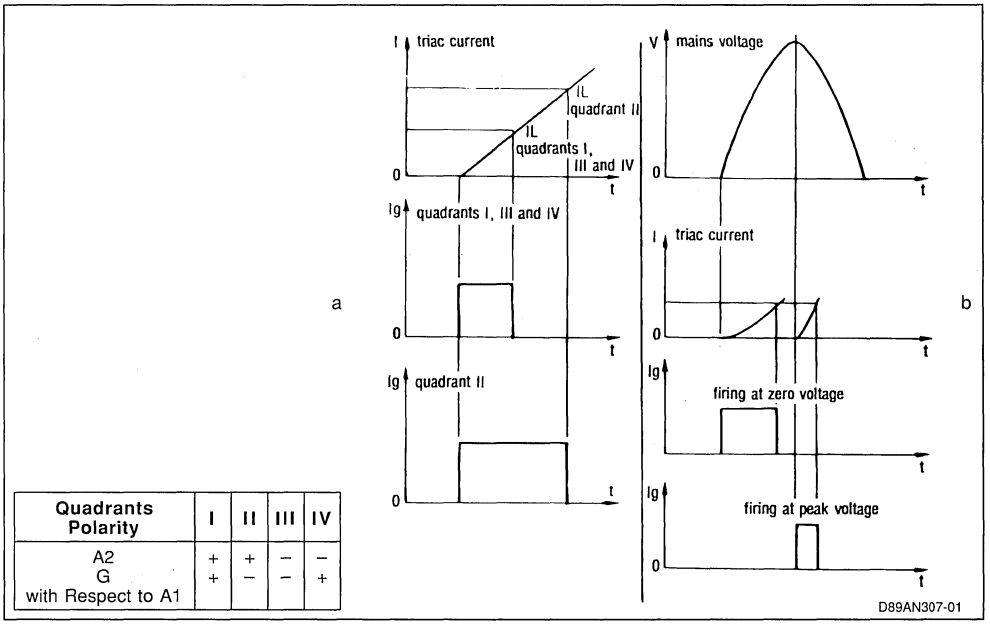
CONTROL SIGNAL

The triac is fired by a gate current Ig > Igt whose duration should enable the main current to reach the triac holding current value (I_L).

The width of the control signal is determined by the rate of increase of the main current (di/dt), limited by the load inductance and by the choice of the firing quadrant.

The loading current, I_L, is highest in the second quadrant (A_2 positive with respect to A_1, I_g negative) : (*figure 1-a*).

Figure 1 : Width of Control Signal Required as a Function of the Firing Quadrant (a) ; width of Control Signal Required as a Function of the Moment of Firing (b).



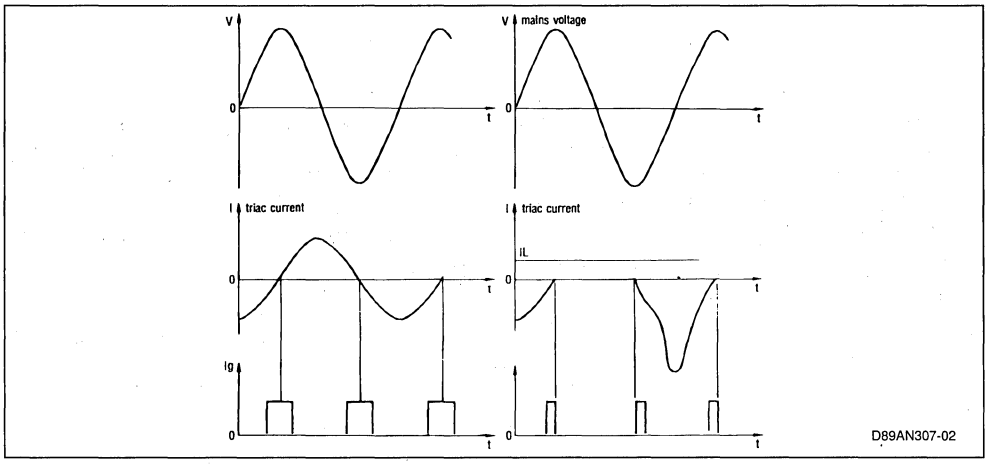
Quadrants Polarity	I	II	III	IV
A2	+	+	−	−
G with Respect to A1	+	−	−	+

The rate of rise of the main current, di/dt, is proportional to the amplitude of the power supply voltage at the moment of firing (di/dt = V/L). The width of the firing signal required is less when firing occurs near the peak of the mains voltage than when its occurs around zero of that voltage (*figure 1-b*).
To fire the triac and to ensure conduction in continuous operation, we can compare various types of control circuits.

GATE CURRENT CONTROL BY SINGLE PULSE
To ensure correct operation, the gate pulse should be synchronized with the triac current zero point and should be long enough to enable the main current to reach the latching current I_L level (*figure 2-a*).

In case the pulse occurs before the triac current reaches its zero point (incorrect synchronization) or if its duration is too short to allow the main current to exceed the latching current I_L, the triac conducts only during alternate half-cycles. The high DC component thus introduced in the load can produce considerable overloads due to saturation of magnetic materials.

Figure 2 : Gate Control by a Single Pulse Synchronized with Zero Current (a) ; in Case of a Single Pulse whose Duration is too Short, the Triac only Conducts during Alternate Half-cycles (b).

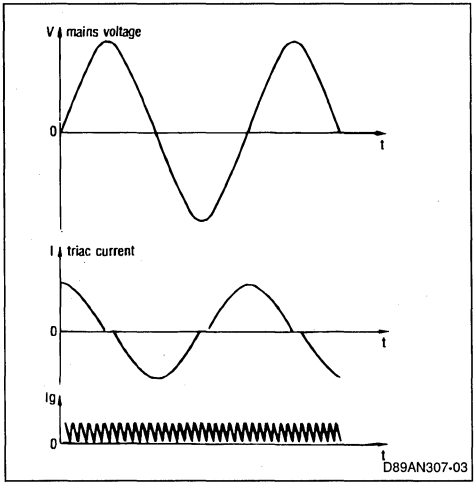


GATE CONTROL BY PULSE TRAIN
The control by gate pulse train eliminates problems of synchronization on the current. A recurrence frequency of several kilohertz guarantees correct operation of this type of control (*figure 3*).
This procedure, whose results are satisfactory, is often used for controlling triacs in inductive circuits.

A variant of this principle consists in making use of a circuit which monitors firing and which delivers pulses to the gate as long as the voltage across the triac is higher than a threshold, usually fixed at about 10 volts (*figure 4*). This type of circuit enables delivering just the amount of gate current required for firing.

GATE CONTROL BY DC CURRENT
Gate control by DC guarantees ideal firing but has the disadvantage of high consumption, specially when the control power supply is provided by the mains. In this case, it is preferable to use a negative current for the gate control (quadrants II and III).

Figure 3 : Gate Control by Pulse Train.



TRANSIENT PHENOMENA DURING TRIGGERING

Principles

During continuous operation, the magnetic field H, proportional to the current in the coil, varies with respect to the induction B, with a delay as shown by the hysteresis cycle in figure 5.

In transient operation, the induction can follow a different path and reach the saturation value B_S for which the magnetic field H (according to the coil current) increases very rapidly (*figure 6*).

Figure 4 : Firing Monitoring Circuit : the Control Signal is repeated until Firing.

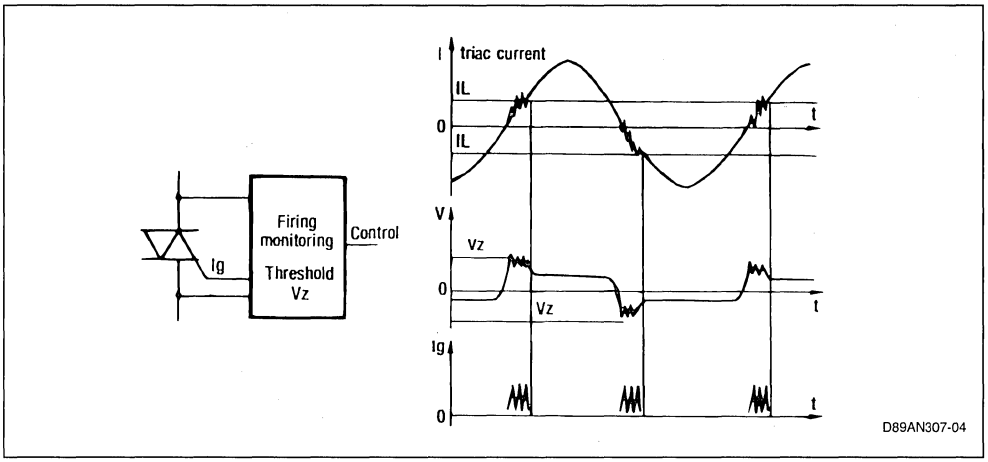
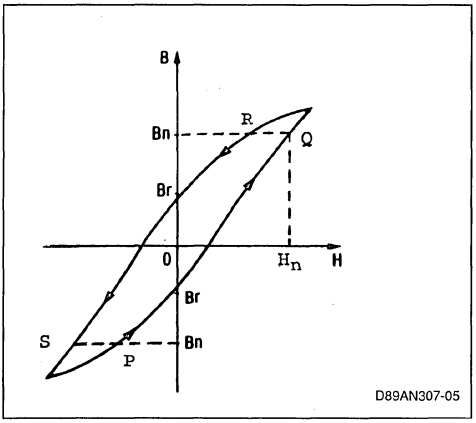
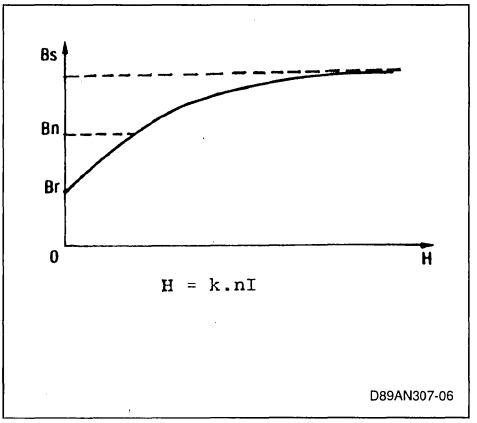


Figure 5 : Magnetic Field H with Respect to Induction B in Continuous Sinusoidal Phase.



In the circuits controlled by a triac, opening occurs when the current is at zero. The induction thus has a remanent value Br, corresponding to H = 0 (*figure 5*).

Figure 6 : Induction Bs Versus Field H Variation.



When the triac begins to conduct, the transients depend on the instant of synchronization of the control signal with respect to the mains voltage.

FIRING AT ZERO MAINS VOLTAGE

Peak induction tends to the value :

$B_{max} = 2\ B_n + B_r$,

thus in most cases reaching saturation induction Bs. The amplitude of the current proportional to the magnetic field H becomes very high ; this type of control produces the highest transient overloads (*figure 7-a*).

In order to limit the over current during firing at zero voltage, control must be done by complete periods. Since the triac allows an integral number of half-cycles to pass, the polarity of the mains voltage at the moment of firing is the reverse of that at the moment the circuit is opened.

Peak induction thus reaches the value :

$B_{max} = 2\ B_n - B_r$, because B rises between P and Q on the hysteresis cycle.

The overload is lower than previously but still remains high (*figure 7-b*).

FIRING AT PEAK MAINS VOLTAGE

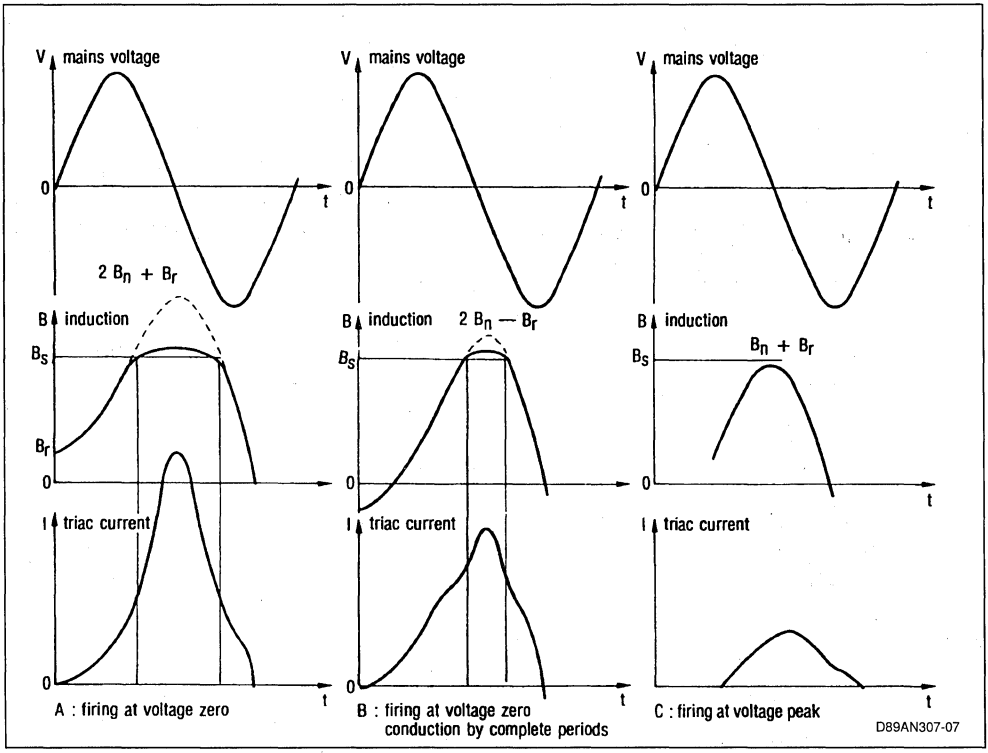
Peak induction takes the value :

$B_{max} = B_n + B_r$

In general, the threshold of saturation Bs is not reached and amplitude of the current remains within acceptable limits (*figure 7-c*).

This type of synchronization is simple and efficient and should be adopted whenever possible on loads composed of materials which can be saturated.

Figure 7 : Transient Induction and Current at Beginning of Conduction.



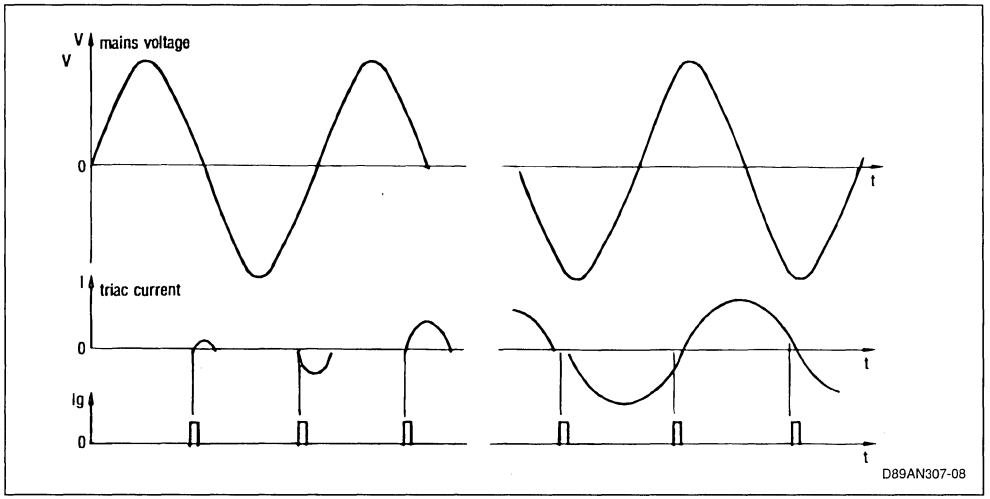
FIRING AT INDUCTANCE PHASE SHIFT WITH CONDUCTION BY COMPLETE PERIODS

Firing at the real inductance phase shift with conduction by complete periods places the magnetic field and the induction on the hysteresis cycle of continuous operation : consequently, transients are eliminated. However, the design of the control circuit for this firing mode is complex and consequently it is reserved for special applications.

FIRING BY PHASE SWEEP

The triac is first fired at the end of a half-cycle. Then progressively the difference of phase between the voltage zero and the instant of firing decreases until total conduction. With a sufficiently low sweep speed, any transient overload is thus avoided (*figure 8*). This procedure is widely used and gives very good results.

Figure 8 : Firing by Phase Sweep.



SPURIOUS FIRING

The control circuit plays an important role in normal operation. However, in case of spurious firing, the triac may have to withstand an accidental overload. The peak amplitude of the current which could flow through the triac should be known to select its rating : the maximum current which could flow through the circuit should not be higher than the accidental overload capacity of the triac (I_{TSM}).
In this care the triac is oversized.

CONCLUSION

We have seen the essential points guaranteeing correct operation of a triac. If the circuit is closed on an inductive load, you need to :

Fire the triac :

With a sufficiently wide gate control signal, in the choosen quadrants (depending on whether higher sensitivity or a low latching current is required).

Avoid transient overloads :

By synchronizing the control signal with respect to the mains at the moment of firing (firing of the triac at zero voltage should be avoided).

Keep the triac in conduction :

By selection of the type of control (avoid gate control by a single short pulse).

CONTROL BY A TRIAC FOR AN INDUCTIVE LOAD HOW TO SELECT A SUITABLE CIRCUIT

By X. Durbecq

Today triacs are well suited to the requirements of switching inductive loads.

Nevertheless many users still encounter difficulties when designing triac control circuits which are to be both economical and applicable to inductive loads.

The purpose of this article is to present different methods of triac control with their applications and to analyze their relative advantages and disadvantages.

A simple circuit offering all the guarantees of reliability is proposed for industrial loads.

TRIGGERING WITH SYNCHRONIZATION ACROSS THE TRIAC

The triggering circuit with "synchronization across the triac" (fig. 1 and 2) turns on the component at an angle β after the current drops to zero, such that $\beta = \omega$ Tr.

Time Tr is defined by the time constant (P + Rt)C.

$\omega = 2 \cdot \pi \cdot f$ with f = mains frequency.

Figure 1 : Typical Circuit : Synchronization Across the Triac.

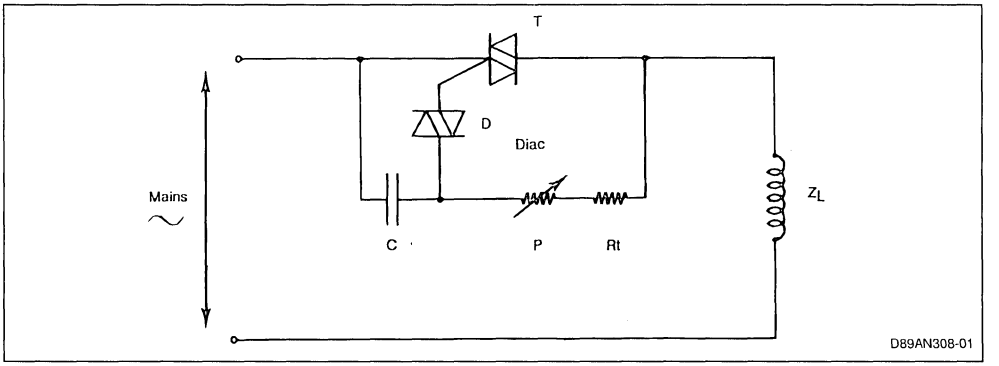
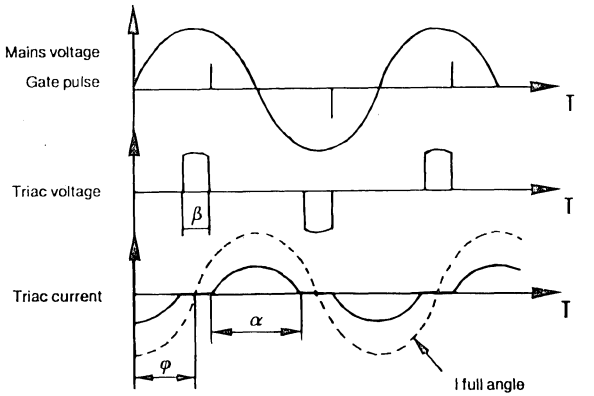


Figure 2 : Synchronization Across the Triac. Shape of the Signals ; General Case.



φ : Current lag (full angle).

β : Blocking of the component.

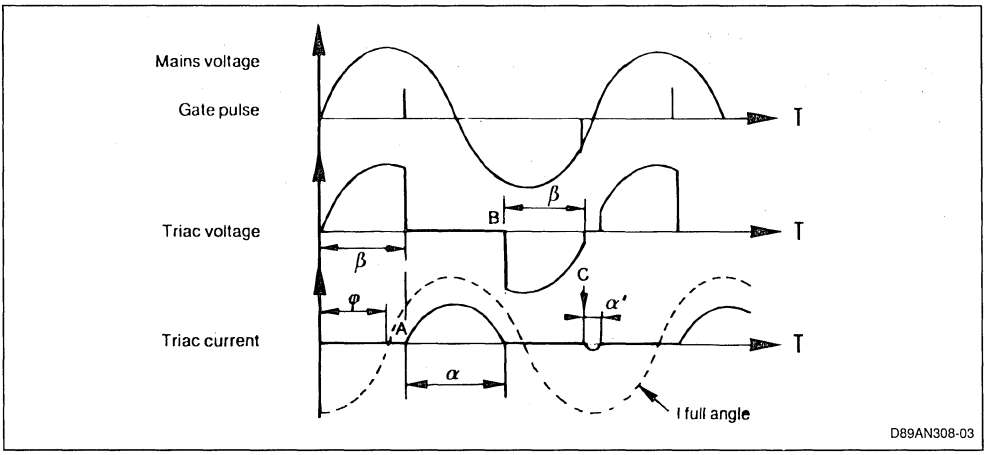
α : Conduction angle.

This is the simplest possible circuit but in certain cases of utilization it can have an important drawback.

For example, consider a highly inductive load ($L\omega / R > 4$) where the triac is turned on with a considerable delay $\beta = 100°$ after the mains voltage zero (figure 3).

The duration of conduction α of the triac turned on at point A, is about 150°. The triac is blocked at point B at $\alpha + \beta = 250°$ after the zero voltage point. At that instant a negative voltage is applied to the triggering circuit which turn on the triac at point C after an angle β of 100°, i.e. 350° from the starting point.
The second turn-on will occur at a very low voltage and the angle α' will be much smaller than α. The following period begins under similar conditions and the unbalance persists. This type of asymmetrical operation is not only unacceptable but can be dangerous (saturation of the load by a DC component).
The unbalance is illustrated for a particular case, starting from zero of the mains voltage. Other causes also produce this fault : variation of the load impedance, transient operation, modification of the adjustement... The reason for this is the principle of the circuit which does not take its reference from the mains voltage zero. Synchronization is by the voltage across the triac, which is a function of the current in the load.

Figure 3 : Synchronization Across the Triac. Shape of the Signals.



Summing up, this first very simple triggering circuit, synchronized by the voltage across the triac, has :

1) Definite advantages :

- Simple design and low cost.
- **Connection by two wires**, without polarity.
- Absence of a separate power supply.
- Little power dissipated in P and Rt.

2) A serious disadvantage :

Because of its principle, this circuit cannot be used for highly inductive loads with a narrow conduction angle because it can result in unacceptable asymmetrical operation.

This very simple triggering circuit should be reserved for low-cost applications with the following characteristics :

- Resistive or slightly inductive loads.
- No stringent requirements concerning the accuracy of regulation.
- Variation on highly inductive loads between 85 and 100 % of the maximum power.

TRIGGERING WITH SYNCHRONIZATION BY THE MAINS VOLTAGE

This triggering circuit (figure 4) is synchronized by the mains voltage. The pulses are always shifted by 180° with respect to each other, whatever the type of load.

Figure 4 : Typical Circuit - Synchronization by Mains Voltage.

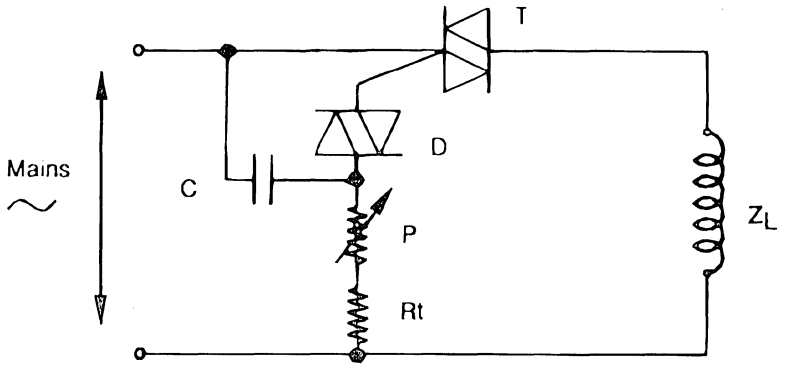
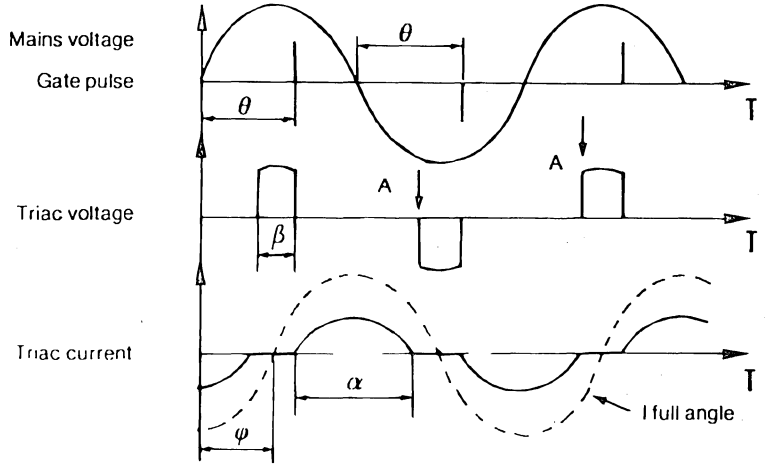


Figure 5 : Synchronization by the Mains Voltage : Shape of Signals.



φ : Current lag at full angle.
β : Blocking of component.
α : Angle of conduction.
θ : Triggering delay angle.

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Angle θ, characterizing the delay between the mains voltage zero and the triggering pulse, can be adjusted by means of potentiometer P from 0 to 180° to vary the voltage across the load. The current in an inductive load (L.R) lags with respect to the voltage by an angle φ :

(tan φ = L.ω / R).

For triggering angles θ higher than φ,operation is perfectly symmetrical and stable.

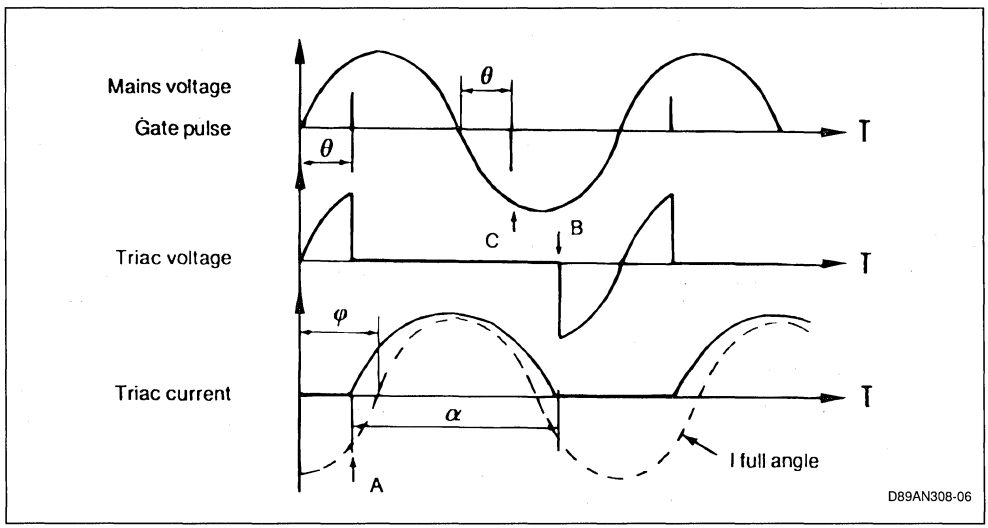
This simple circuit can still present the risk of a fault in case angle θ is smaller than angle φ (figure 6).

As an example, take the case of a highly inductive load and an angle θ = 60° . The triac is turned on at point A (60°).

It will conduct during an angle α greater than 180°, in the neighbourhood of 250° . It is blocked at point B : (290°). The second triggering pulse occurs at point C : (θ + α = 240°).

It has no action on the triac which is still conducting. The triac is not turned on for the other half-wave. As in the previous case, the operation is asymmetrical, and thus unacceptable.

Figure 6 : Synchronization by the Mains Voltage - Shape of the Signals for θ < φ - Asymmetrical Operation.



To prevent this fault, it is necessary to insert a "stop" to maintain θ > φ . This is possible for loads whose L and R parameters remain strictly constant.

Experience shows that for the majority of inductive loads used in industrial applications (motor controls, transformers, etc...) it is not possible to insert the "stop" without considerably limiting the voltage excursion, since the values of L and R vary a great deal during operation.

Summing up, this simple triggering circuit, synchronized by the mains voltage, is more developed than the previous one. It has :

1) Advantages :

- Simple design.
- More accurate control than the previous circuit.
- No auxiliary power supply or transformer required.

2) Disadvantages :

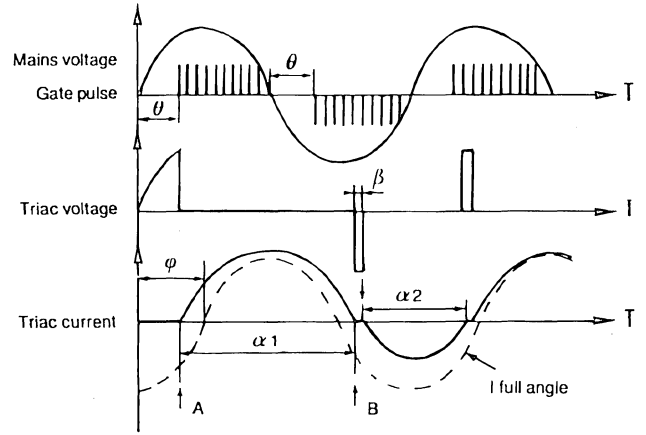
- Connection of the circuit by 3 marked wires, instead of 2 without polarity in the previous circuits.
- Power dissipated in passive components P and Rt.
- Operation becomes completely asymmetrical if the control angle θ is less than φ.

This triggering circuit can only be used for applications in which the phase shift of the load remains constant (air inductor) or if operation is restricted to values of θ much higher than φ i.e. at low voltage.

TRIGGERING SYNCHRONIZED BY THE MAINS VOLTAGE AND SUITABLE FOR INDUSTRIAL APPLICATIONS

This new circuit is derived from the previous one by improving the triggering pulse generator. The improvement consists in maintaining the triggering signal during each half-wave between values θ and 180°. This is done simply by sending a pulse train after the initial pulse so as to maintain the triggering order (figure 7).

Figure 7 : New Circuit - Triggering by Pulse Train Synchronization by the Mains Voltage.



φ : Current lag full angle.
α : 1st angle of conduction.
α 2 : 2nd angle.
β : Blocking of triac.
θ : Triggering delay time.

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For example, suppose that angle φ is equal to 85° and θ is equal to 60°. At the first pulse, the triac is turned on at point A (60°). It conducts for angle α 1 greater than 180° and close to 240°. It is blocked at point B but is immediately triggered at point B' by the next repetitive pulse. During the first half-waves, operation is slightly asymmetrical but gradually the durations of conduction become balanced (dotted line curve in figure 7).

Figure 8 : Circuit with Triggering by Pulse Train Synchronization by Mains Voltage.

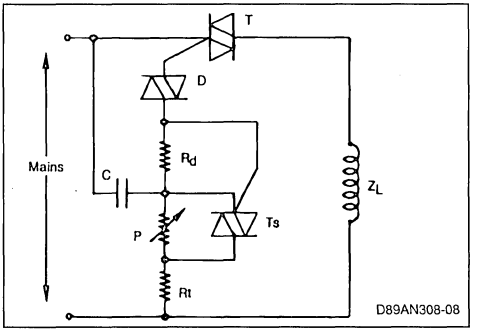


Figure 8 gives the circuit diagram. A small sensitive auxiliary triac is used to produce the pulse train necessary for maintaining the control signal.

Capacitor C, compensating resistor Rt and potentiometer P define the angle θ or delay time constant. The capacitor is charged from 0 V and diac D triggers as soon as its breakover voltage (Vbo) is reached. The angle is positioned identically for both half-waves.

A first pulse is applied to the gate of the main triac, T. A voltage pulse occurs across Rd and triggers sensitive triac Ts. Once it has been turned on, this triac bypasses potentiometer P. The remaining charging cycles of the capacitor have a much shorter time constant Rt x C.

A succession or train of pulses is applied to the gate of the main triac, T, enabling elimination of the defects explained above. The pulse train continues until the mains voltage crosses the O point. Triac Ts, supplied through a resistive load, is blocked.

For the following half-cycle, the capacitor load is once more based on the time constant determined by the potentiometer. The cycle is resumed in inverse.

Summing up, the improved triggering circuit synchronized by the mains voltage has a number of advantages.

- Simplicity of design.
- Excellent accuracy of control.
- Absence of auxilliary separate power supply.
- Utilization of the circuit for all types of loads with different cos φ or variable cos φ values.
- No risk of failure over the whole adjusting range.

This circuit has been developed by the SGS-THOMSON Microelectronics applications laboratory and used with success for a wide range of equipment.

CONCLUSION :

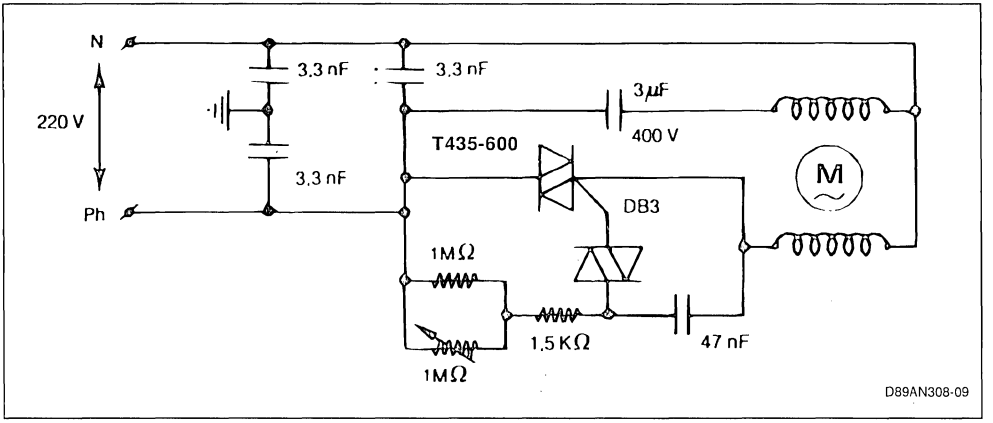
The difficult conditions of an inductive environment require a critical choice of the triggering circuit. The first two circuits described leave the user a very limited adjusting range. A universal circuit can be obtained by taking into account two decisive factors :

- To obtain perfect symmetry of the first gate pulses in both half-cycles, the triggering circuit should be synchronized by the mains voltage.
- The variation in phase angle enables perfect symmetry of the current if the triac is continuously triggered.

The circuit described in the last paragraph combines these two principles in a very simple manner. It enables complete variation of power on an inductive load without particular problems. It can thus serves as the basis for a universal circuit for control by phase splitting on a inductive load.

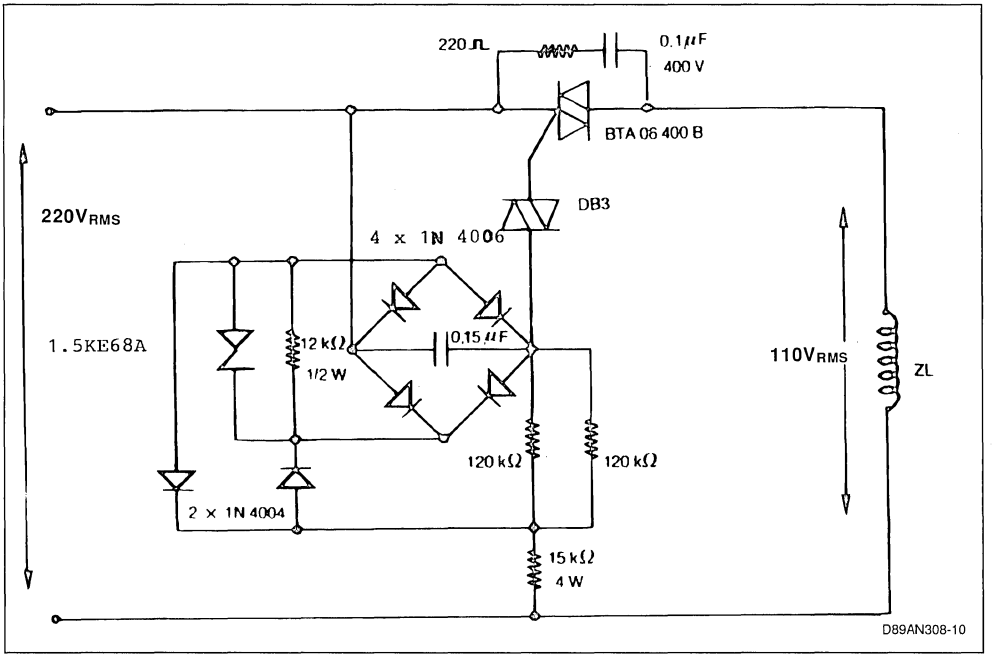
SYNCHRONIZATION ACROSS THE TRIAC

Figure 9 : Example of an Application : Speed-control Circuit for a Small Asynchronous Motor.



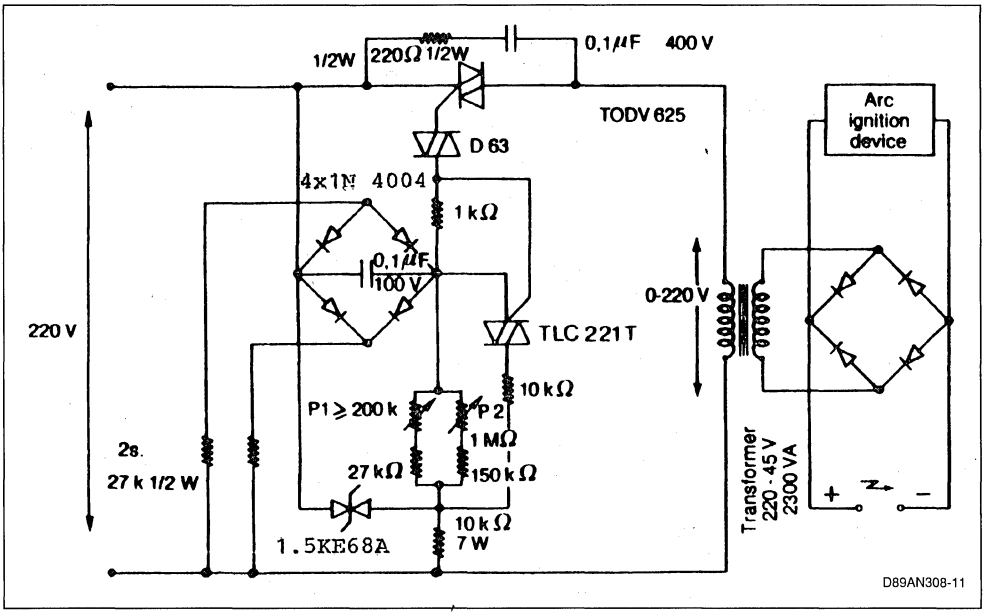
SYNCHRONIZATION BY THE MAINS VOLTAGE

Figure 10 : Example of an Application : 220/110 V Step-down Circuit.



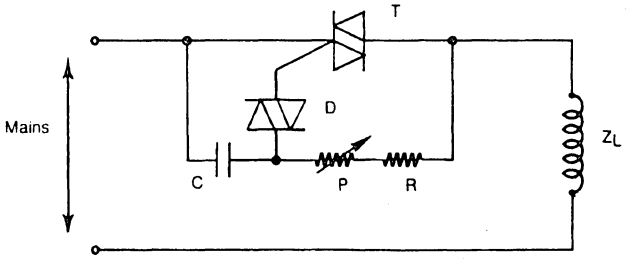
NEW TRIGGERING CIRCUIT

Figure 11 : Example of an Application : Power Variation Circuit for Arc Welding Transformer.



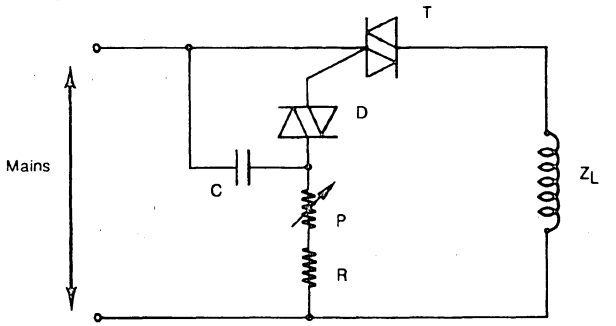
APPENDIX
CONTROL BY TRIAC FOR INDUCTIVE LOADS
SUMMARY OF SOLUTIONS

A SYNCHRONOUS TRIGGERING ACROSS THE TRIAC



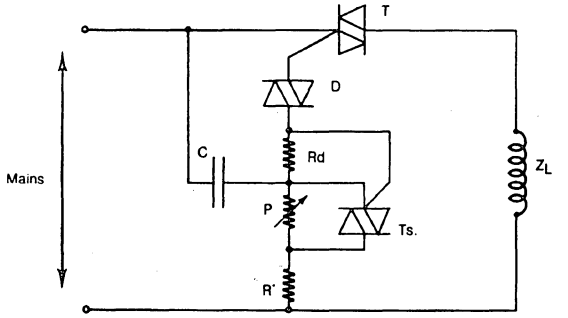
Synchronization across the triac based on crossing of the zero point by the current.

B TRIGGERING SYNCHRONIZED BY THE MAINS VOLTAGE



Synchronization based on crossing of the zero point by the mains voltage

C NEW TRIGGERING CIRCUIT



Synchronization by crossing of the zero point by the mains voltage and generation of a pulse train from then onwards.

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TRIGGERING SYNCHRONIZED ACROSS THE TRIAC

SCHEMATIC DIAGRAM (see page 10-A)

RESISTIVE LOAD :

Current and voltage are in phase : good synchronization. No fault over the whole adjusting range.

INDUCTIVE LOAD :

The current lags by $\pi/2$. Two cases should be considered :

- Broad conducting angle ; narrow lag angle.

The time separating two conducting periods is very brief. The positive and negative currents are practically equivalent. Little dissymmetry. Certain applications are covered by this case.

e.g. speed-control circuit for AC motors.

- Narrow conducting angle ; broad lag angle.

The flow of current in one direction is a function of the control and thus of the duration of the current flow in the previous direction.

The triac can be triggered at the end of the mains half-cycle. In this case no current flows through the circuit and it acts as a rectifier.

ADVANTAGES OF THE CIRCUIT :

- Connection by two wires without polarity.
- No power dissipated by the passive components.
- Excellent power variation circuit for resitive or slightly inductive loads.
- With highly inductive loads, the circuit can only give satisfaction within the limits of a slight decrease in the conducting angle.

DISADVANTAGES :

- For inductive loads, large current dissymmetry for a variation towards the narrowest conduction angles. For this type of application the circuit cannot be used at all.

TRIGGERING SYNCHRONIZED BY THE MAINS VOLTAGE

SCHEMATIC DIAGRAM (see page 10-B)

RESISTIVE LOAD :

No fault over the whole adjusting range.

INDUCTIVE LOAD :

Two cases should be considered :

- Delay angle $\theta >$ the lag, φ.

Correct synchronization of the triggering pulses enables balanced conduction for all variations up to the lag angle.

Certain applications use this principle :

e.g. 200 V – 100 Vrms step-down circuit.

- Delay angle $\theta < \varphi$.

Triggering occurs before the lag angle is reached. The triac will conduct for an angle $\alpha > 180°$. It is blocked after the gate pulse of the following half-cycle. The current does not flow in that direction. The circuit thus acts as a rectifier.

ADVANTAGES OF THE CIRCUIT

- Accuracy of the triggering pulses.
- Current operation with a resistive load but circuit too complex.
- Excellent operation for power variation circuits limiting conduction to small angles with inductive loads.

DISADVANTAGES :

- Connection by three wires. Necessity to obtain access to the mains terminals.
- Permanent power supply with power dissipated by the passive components.
- Impossible to adjust the delay angle to values approaching or inferior to the current lag. This circuit cannot be used for inductive loads where a variation close to the highest conduction angles is required.

NEW TRIGGERING CIRCUIT

SCHEMATIC DIAGRAM (see page 10-C)

RESISTIVE LOAD :

Absence of fault over the whole adjusting range.

INDUCTIVE LOAD :

Operation in the two possible cases :

- Delay angle $\theta > \varphi$

Balanced conduction due to perfect synchronization of the triggering pulses.

- Delay angle $\theta < \varphi$

For a conduction angle higher than 180° , the triac is blocked after the 1st pulse of the following half-cycle. It is immediately retriggered by the next repetitive pulse. The two currents are mutually modified until a balance is reached.

DISADVANTAGES OF THE CIRCUIT :

- Connection by 3 wires. Access to the mains terminals.
- Permanent power supply with power dissipated in the passive components.

ADVANTAGES :

- Accuracy of the triggering pulses.
- Correct operation for resistive loads.
- Complete absence of faults for inductive loads.

Power variation over the whole range.
Perfectly balanced positive and negative current.

PROTECT YOUR TRIACS

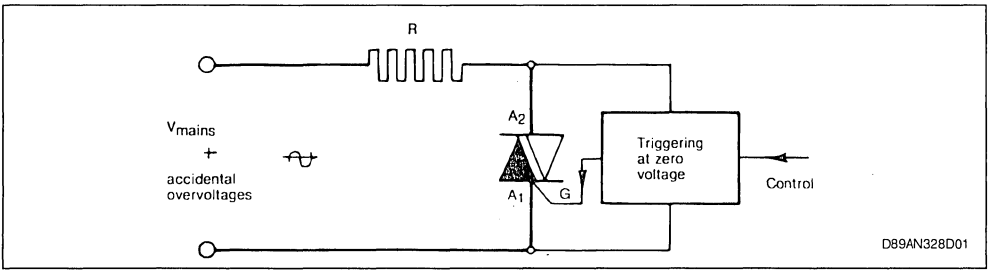
By P. RAULT

In most of their applications, triacs are directly exposed to overvoltages transmitted by the mains. When used to drive resistive loads (temperature regulation), it is indispensable to provide them with eficient protection.

WHY PROTECTION ?

In a typical utilization circuit (figure 1), an overvoltage superimposed on the network voltage can turn on the triac by exceeding its avalanche voltage. Under these conditions, because of its internal structure, only part of triac is effectively turned on and can thus withstand only very low di/dt. This explains the considerable danger of damage to the component when used to drive purely resistive loads. In reality, the di/dt when turning on can, in this case, reach very high values (> 100 A/µs) since only the inductance of the connections limits the rate at which the current can increase.

Figure 1 : Typical Circuit.
The Triac is directly connected to the distribution network : risk of damage.



WHAT WE PROPOSE

The principle of the protection which we have studied consists in turning on the triac by the gate, as soon as the voltage across it exceeds a certain value (figure 2), thus under conditions which ensure a high level of safety. To do this we use a bidirectional TRANSIL diode whose current/voltage characteristic is recalled in figure 3.
When the voltage applied to the triac reaches the VBR voltage of the TRANSIL, the latter conducts, producing a current in the triac gate and turning it on (figure 4). The triac continues to conduct till the half cycle current passes through zero (figure 5).

Figure 2 : Protection of the Triac by a Bidirectional TRANSIL Diode.
The Triac is turned on by gate (current i) as soon as voltage A_2 exceeds the voltage V_{BR} of the TRANSIL.

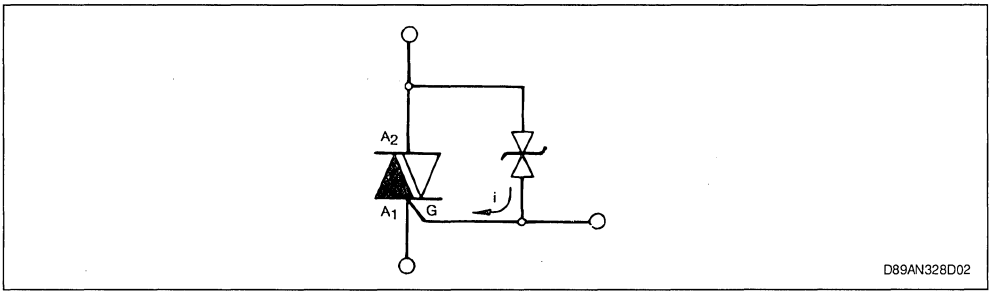


Figure 3 : Voltage-current Characteristic of a TRANSIL Diode.
V_{BR} Specified at 1mA (tolerance 5 or 10%)
V_{CL} limitation voltage, given for a high I_{PP} current level (from several amperes to several tens of amperes, depending of the type.

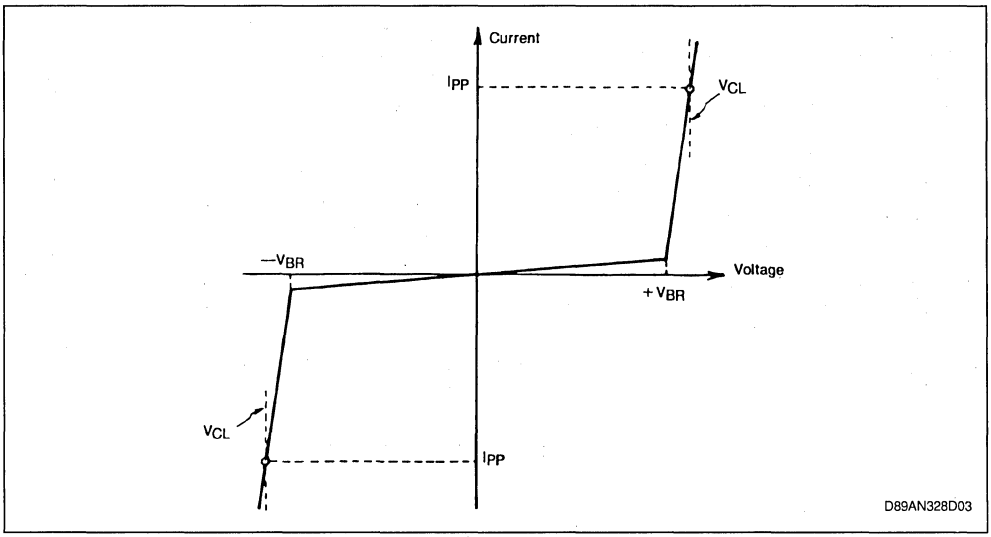


Figure 4 : Characteristic of the TRIAC + TRANSIL Assembly.
Case of a 600V/12A triac protected by a 440V TRANSIL diode (the dotted line gives the characteristic of the triac alone).

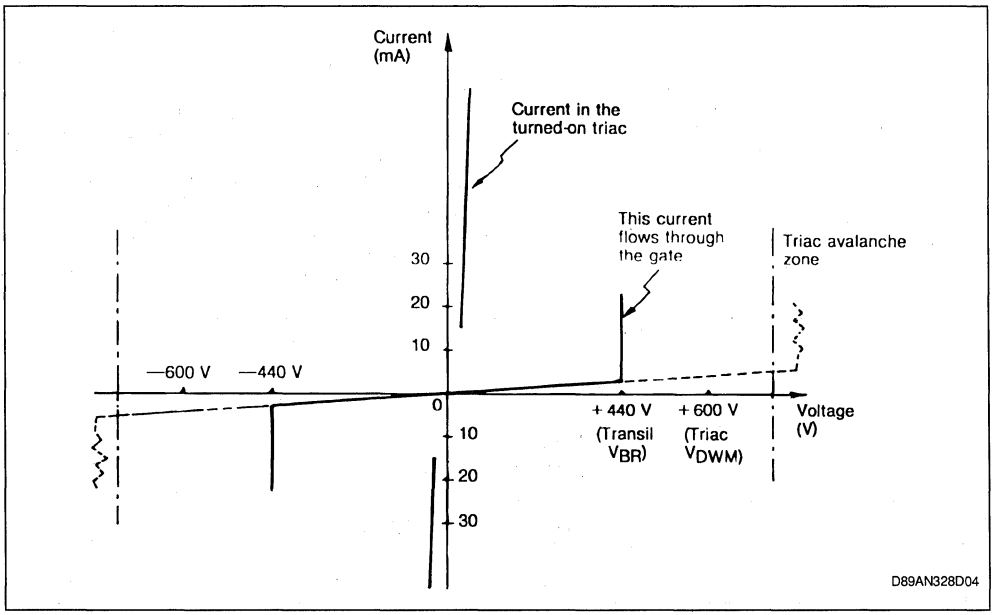
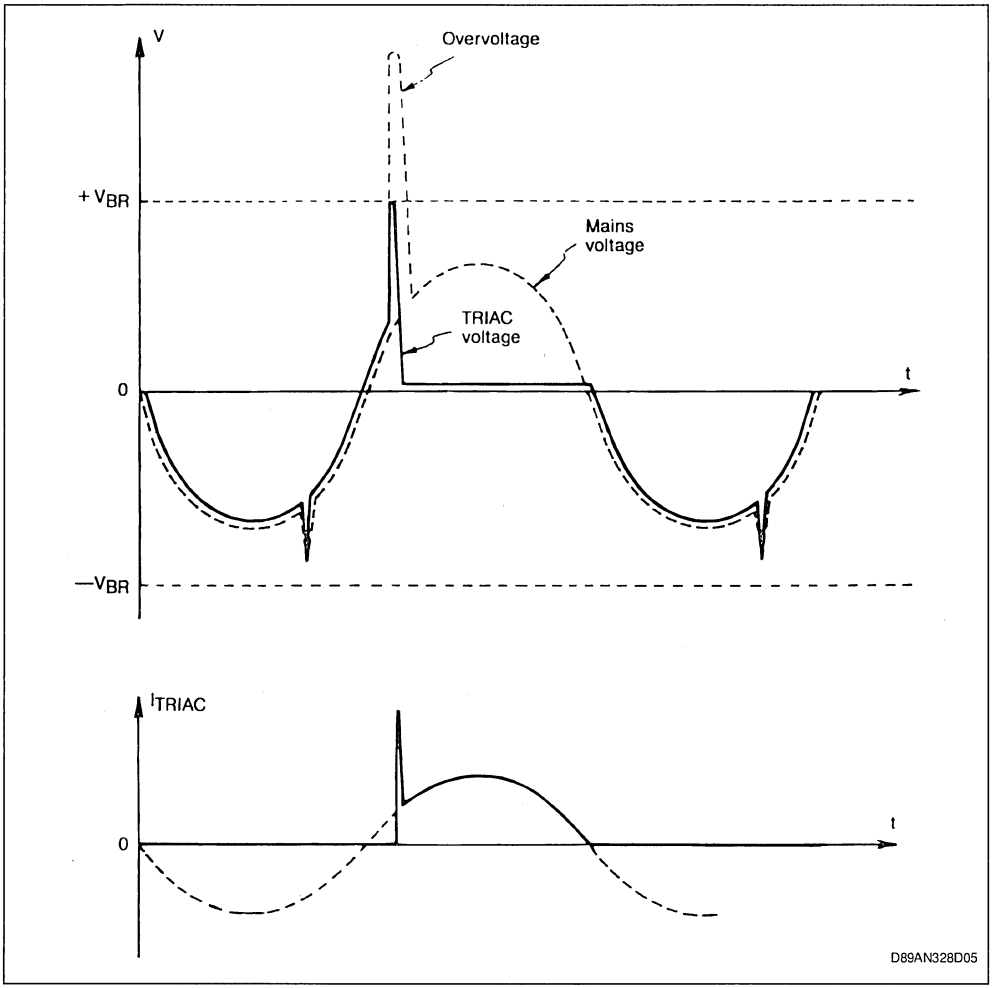


Figure 5 : Behaviour of a Triac Protected by a TRANSIL Diode.
(the triac is turned on by the gate at the beginning of the overvoltage and continues conduction-through the rest of the half-wave).



THE ADVANTAGES OF THIS SOLUTION

- The triac will always operate within the voltage limits given by the manufacturer (± VDWM) and thus far from the avalanche zone.
- Not much power is dissipated in the triac during the disturbance : when it is turned on, the dissipated power is localized in the protection component (the TRANSIL is made for that !).
- The triac is turned on by a gate current which will ensure optimal di/dt conditions.

THE RESULT OBTAINED

We have carried out tests with repetitive overloads (1Hz) under various conditions :

Exponential shock waves of about 1ms, calibrated in voltage (up to 2000V) and controlled in di/dt (500A/µS maxi).

The tests were carried out with steep-edged voltage pulses (dV/dt > 1000V/µs) and also with gradual slopes (< 50V/ms).

All these tests were successful : zero failure.

SELECTION OF THE TRANSIL DIODE REQUIRED FOR PROTECTING A TRIAC

VOLTAGE : VR

Obviously the triac associated with the TRANSIL diode should not be turned on by the maximum mains voltage. An additional safety margin should be given to prevent untimely turning on by the small voltage spikes, often repetitive, which are always present on a «normally» disturbed mains line.

$VR > Vmains \times \sqrt{2}$ + safety margin

In the absence of accurate specifications, add 20% for the safety margin.

Example : 220V network :

$VR > 220 \sqrt{2}$ + 20% = 375V

POWER

The TRANSIL only conducts when turning on the triac (t ≡ 1µs).

The current, during this time, can reach very high levels (several tens of amperes) in the case of disturbances with steep edges (> >1000V/µS), however the dissipated power remains well within the possibilities of TRANSILS.

The BZW 04 (400W/1ms) suffices in all cases.

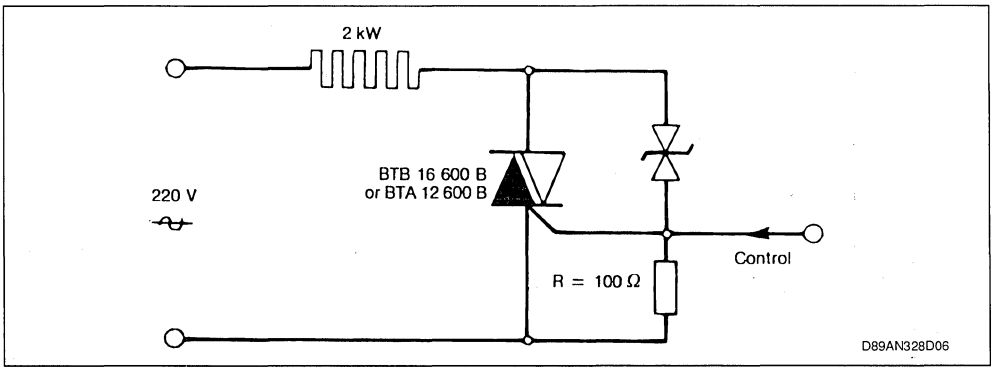
PRACTICAL EXAMPLE

Drive circuit for a 2kW heating element on 220V mains (figure 6).

The BZW 04.376 type TRANSIL perfectly protects the BTB 16.600 B triac (VDWM = ± 600V).

The 100 – Ω resistor, R, between the gate and A1 is not absolutely indispensable but it enables preserving the dV/dt characteristic of the triac which is reduced (by about 20%) by the junction capacitance of the TRANSIL between anode and gate.

Figure 6 : Practical Example of the Protection of a 12 or 16A Triac against Overvoltages.



CONCLUSION

With the protection circuit proposed by us, the triac always operates under perfectly defined conditions in case of overvoltages :

- The voltage remains limited to the maximum specified for the triac
- Turn-on is ensured by a gate current.

This circuit, which we have tested in a number of different setups (different loads, high amplitude overvoltages, disturbances of long duration, etc...), enables a considerable increase in the reliability of circuits using triacs and is indispensable for driving resistive loads on highly disturbed networks.

POWER CONTROL WITH ST6210 MCU AND TRIAC

Philippe RABIER - Laurent PERIER

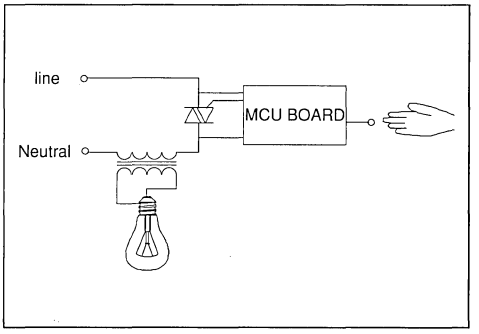
INTRODUCTION

Microcontroller (MCU) systems are progressively replacing analog controllers even in low cost applications. They are more flexible, provide a faster time to market and need few components.

With an analog IC, the designer is limited to a fixed function frozen inside the device. With a DIAC control, features such as sensor feedback or enhanced motor drive can not be implemented. With the MCU proposed in this note (ST6210), the designer can implement his own ideas and test them directly using EPROM or One Time Programmable (OTP) versions.

The LOGIC LEVEL triac BTA08-600SW is a good complement to this MCU for low cost off-line power applications. This triac requires a low gate current, and can be directly triggered by the MCU, while still maintaining a high switching capability.

This application note describes the main aspects of a highly flexible, low cost power application designed around an ST6210 MCU and a LOGIC LEVEL triac.



BOARD OPERATION

Basic function

Light dimmers with DIAC or analog controllers are currently used today. These circuits have the disavantage that they can not easily drive inductive loads like halogen lamps on the secondary of a 220V/12V transformer. They are also limited in the choice of user interfaces.

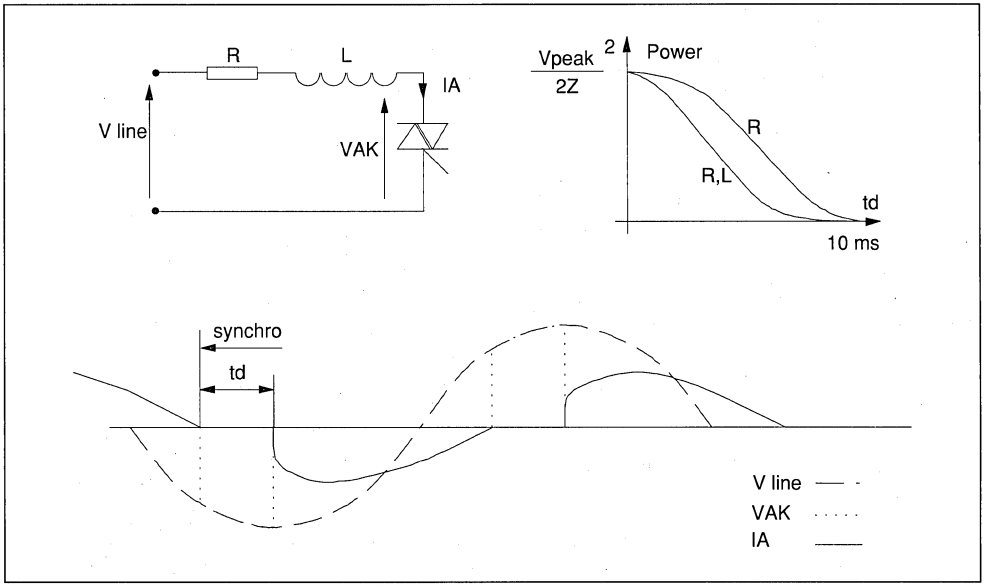
A light dimmer circuit, supplied directly from the 110V/240V mains, has been realized using a MCU ST6210 and a LOGIC LEVEL triac. This circuit drives both resistive and inductive loads (e.g. halogen or incandescent lamps, transformers). The control method is such that the same board can drive a universal motor. The user interface is either a touch sensor, a push button or a potentiometer. The board contains a minimum of components therefore saving cost and space. The auxiliary supply is derived from the voltage across the triac.

Power control

The output power is controlled by the phase delay of the triac drive. In classical designs, the delay is refered to the zero crossing of the line voltage. The detection of the zero voltage normally requires an additional connection to the mains neutral. In order to avoid this connection and connect the circuit directly in series with the load, the trigger delay is referred to the previous zero crossing of the current (fig.1).

BOARD OPERATION (Continued)

Figure 1. The Power Control Is Based On The Monitoring Of The Zero Crossing Of The Current



Mains synchronisation

When the current in the triac is zero, the mains voltage is re-applied across the triac. Synchronisation is achieved by measuring this voltage. This voltage is monitored in each halfwave, which allows the detection of spurious open load conditions. The triac is retrigged with multipulse operation if it is not latched after the first gate pulse.

Changing operation from 50Hz to 60Hz can be achieved by making simple modifications to the microcontroller EPROM/ROM table defining the triac conduction angle versus the power level.

Operation with a transformer

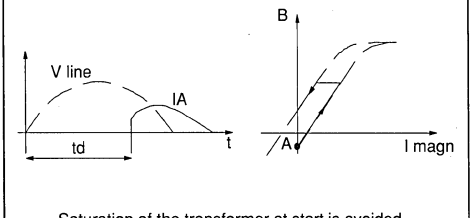
Low power halogen spots use low voltage lamps (12V typ.) usually supplied through a low voltage transformer. The light dimming of these lamps is simple with this circuit.

A phase lag between current and voltage as high as 90 does not disturb the circuit because the control method is based only on monitoring the zero current crossing.

The risk of saturation of the transformer core is avoided because the controller includes the following features:

At the start, the delay time between the first gate pulse and the synchronisation instant is greater than 5ms. This limits the induction in the transformer and hence reduces the risk of saturation.

Figure 2. First Gate Pulse Delay

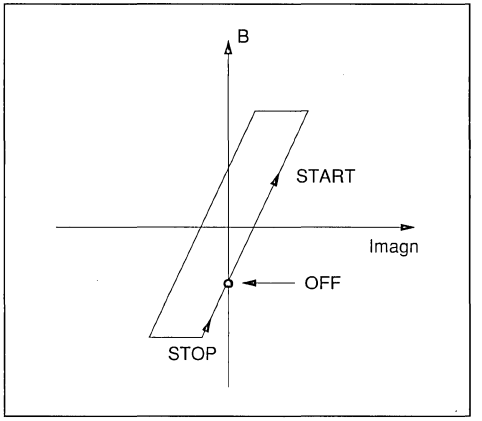


Saturation of the transformer at start is avoided.

BOARD OPERATION (Continued)

The circuit starts on a positive halfwave and stops on a negative halfwave (fig.3). So it starts with positive induction and stops after negative induction has been applied. This helps to minimize the size of the magnetic material.

Figure 3. Hysteresis Cycle in off/start/stop Phases



The timer is very precisely tuned in order to obtain precisely 10ms delay between two gate pulses. As a result, the triac is driven symetrically in both phases so continuous voltage in the transformer is avoided.

The voltage across the triac is monitored in order to detect a spurious open load condition on the secondary of the transformer.

The inrush current at the turn-on of a lamp (halogen or incandescent) is also reduced due to the soft start feature of the circuit (fig.8).

Triac drive

The triac is multi-pulse driven. Therefore, inductive loads can be driven without the use of long pulse drives. As a result, the consumption on the +5V supply can be minimized and the supply circuit made very small.

The pulse driving the triac is 50µs long. The LOGIC LEVEL triac is driven in quadrants QII and QIII with a gate current of 20mA provided by two I/O bits of the ST6210 in parallel. The LOGIC LEVEL triac has a maximum specified gate triggering current of 10 mA at 25°C.

Before supplying the first drive pulse, the triac voltage is tested. If no voltage is detected, a spurious open load or a supply disconnection is assumed to have occured and the circuit is stopped.

After the first driving pulse, the triac voltage is monitored again. If the triac is not ON, another pulse is sent. The same process can be repeated up to four times. Thereafter, if the triac is not ON, the circuit is switched off.

User Interfaces

There are three different user interfaces: a touch control, a push button or a potentiometer. Four modes can be selected on the board in order to define how the transmitted power is related to the user interface.

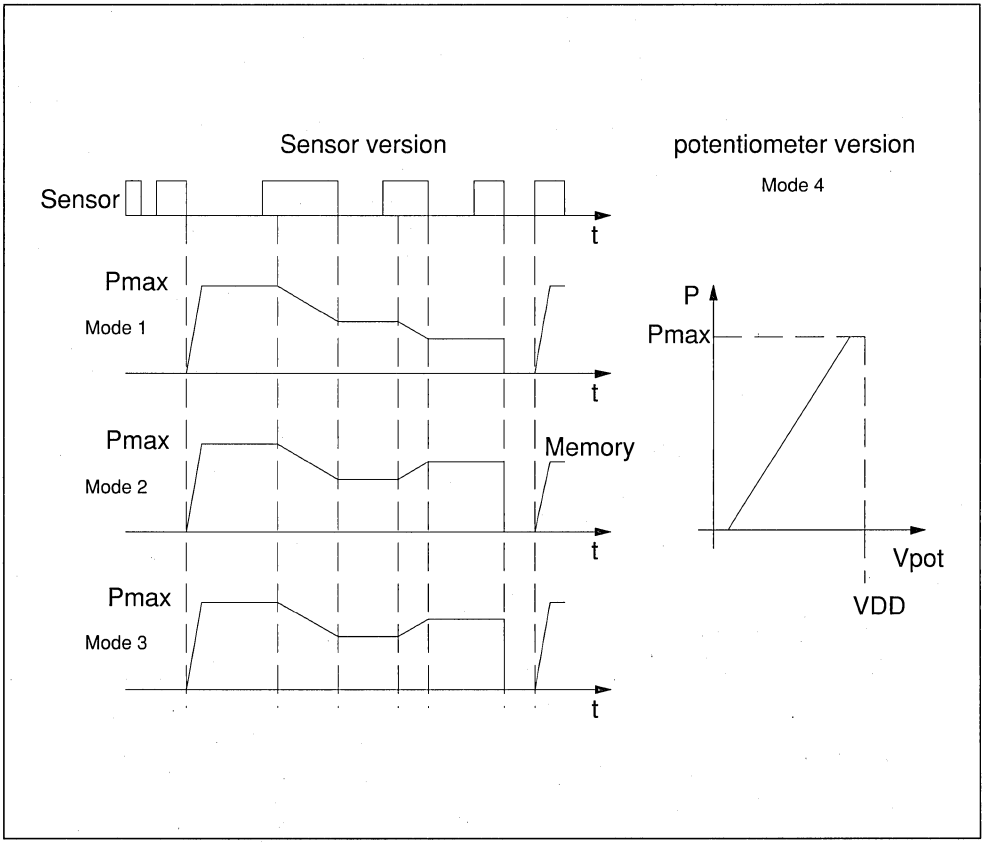
Three modes operate with the touch sensor or the push button. Dimming is obtained when the sensor or the button is touched for more than 400 ms. If the touch duration is between 60 ms and 400 ms, the circuit is switched on or off. A contact of less than 60 ms has no effect. Modes 1,2,3 differ in the way the ouput power is influenced by the contact on the sensor or on the button.

Mode 4 directly relates the transmitted power to the position of the potentiometer (fig.4).

All modes include a soft start function.

BOARD OPERATION (Continued)

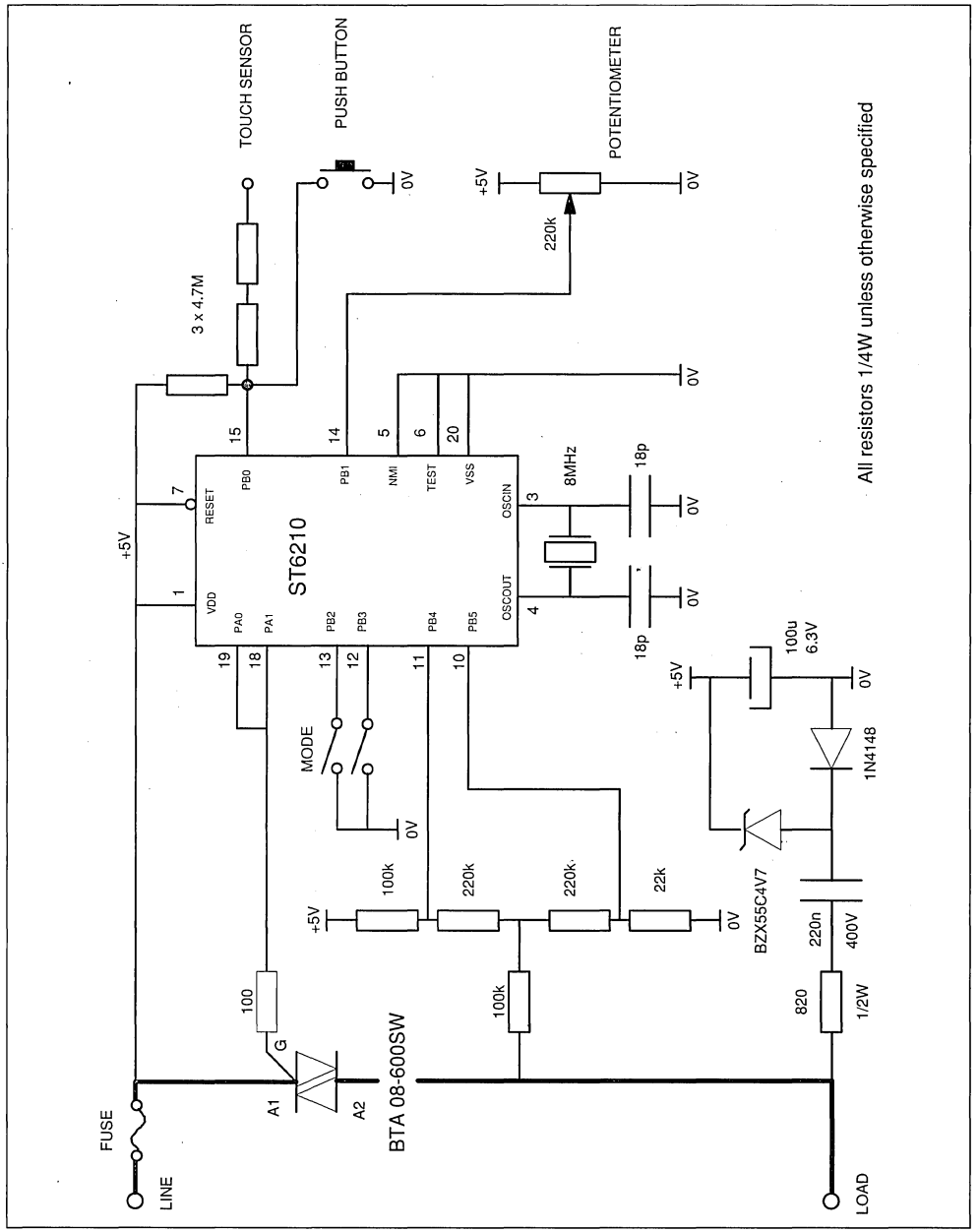
Figure 4. User Interface



Sensor Contact Duration	< 60ms	60ms to 400ms	> 400ms
Mode 1	No effect	Switched ON to full power or switched OFF	Same sense of variation as previous action
Mode 2	No effect	Switched ON to previous level or switched OFF	Opposite sense of variation to previous action
Mode 3	No effect	Switched ON to full power or switched OFF	Opposite sense of variation to previous action

BOARD OPERATION (Continued)

Figure 5. Circuit Diagram



HARDWARE

The circuit uses an 8 bit MCU ST6210 and a LOGIC LEVEL triac directly driven by the MCU (fig.5). It operates with 3 user interfaces, 4 modes of operation and 4 kinds of loads. When the board is dimming a resistive load, an RFI filter must be used in order to meet RFI standards (eg. VDE 875).

The ST6210 includes 2K ROM, 64 bytes RAM, an 8bit A/D converter that can be connected to eight different inputs, 4 I/O ports with 10mA sink current capability and a timer. Hysteresis protection is included in series with each I/O pin. The ST6210 is packaged in PDIP or SMD packages. The ports, timer and interrupts configurations can be chosen by software, providing great flexibility. With EPROM and OTP versions, the equipment development and preproduction can be carried out directly from the design lab thus providing a fast time to market.

The LOGIC LEVEL triac (BTA08-600SW) has been especially designed to operate with MCUs. It is a sensitive triac (I_{GT}=10 mA, I_L=50 mA) trigged in quadrants QII and QIII. In this application it is driven by two I/O bits of the ST6210 in parallel. This triac has high switching capabilities ([dI/dt]c=3.5 A/ms), ([dV/dt]c=50 V/µs), so in this circuit, it can operate without a snubber.

Total consumption of the board is less than 3mA with an 8MHz oscillator. The board receives its supply only when the triac is off. So a minimum off time of the triac (2ms) is necessary to ensure its supply.

The 5V supply capacitance is mounted as near as possible to the MCU with very short interconnecting tracks in order to maximize the RFI/EMI immunity.

The touch sensor is a voltage divider between line and neutral potentials. It operates when the supply of the circuit is connected at the line potential and not at the neutral. The user is protected from electrical shock by a very high impedance (10MΩ) connecting the sensor to the circuit.

SOFTWARE

All the features are included in a 700 byte program. More than 1kbyte of ROM is available for additional features. The architecture of the software is modular in order to provide maximum flexibility.

The table relating the delay time to the power requirement contains 64 different levels. The conduction time of the triac can vary from 2ms to 8ms. The user can easily adjust the minimum and maximum power levels because the corresponding delay times change with smaller increments at the top and bottom of the table.

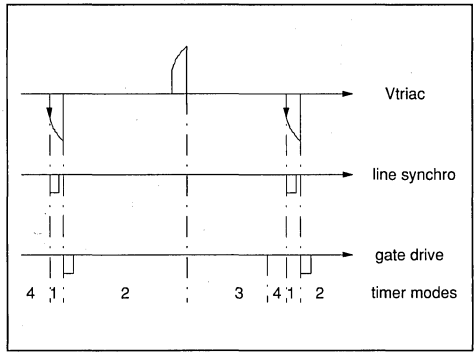
The table can be easily modified in the ROM/EPROM space to meet different conditions e.g. 60Hz operation or varying loads.

Software versions cover the four user interface modes of operation without hardware change.

All inputs are digitally filtered, so that an input is valid only if it remains constant for 10µs or more. This reduces the number of passive components required.

The mains supply carries disturbances (e.g. glitches, telecommand signals) which can disturb the triac drive and generate lamp flickering. For this

Figure 6. Internal Timer Operation

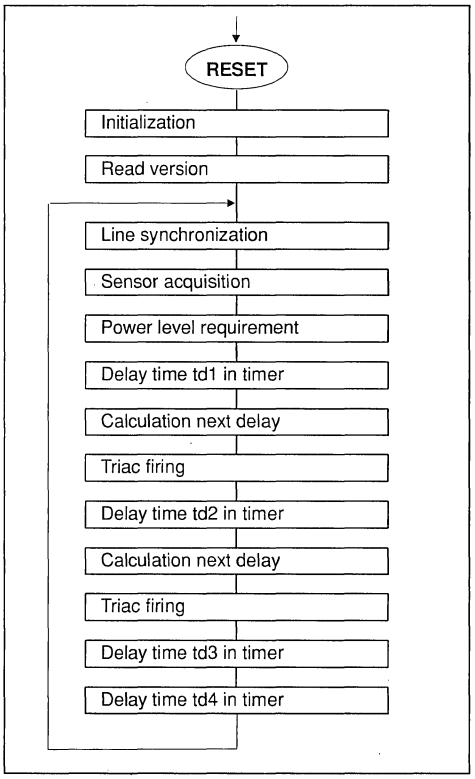


SOFTWARE (Continued)

reason, the triac voltage is not used directly as the synchronisation parameter. The timing is carried out internally by the MCU timer. The period of operation can be slowly modified to follow the variations of the mains frequency but not the spurious disturbances. The mains synchronization signal is received every cycle. The corresponding mains period is measured and compared to the internal timer period. If a difference remains for a long time, the timer period is modified to follow the mains. This block acts like a low band filter which saves external filtering components.
Each 50Hz period, the timer operation is separated in four steps (fig.6). The triac voltage synchronisation can only be validated during phase 4.

The software has been written with modular blocks (fig.7). It can be enlarged to other applications such as motor speed regulation, telecommand input or IR remote control with additional blocks.

Figure 7. Major Steps of the Software



PRACTICAL RESULTS

Figure 8 shows the soft start operation with a halogen lamp operating from the secondary of a low voltage transformer and with a tungsten filament lamp.

Figure 8. Soft Start With Lamps

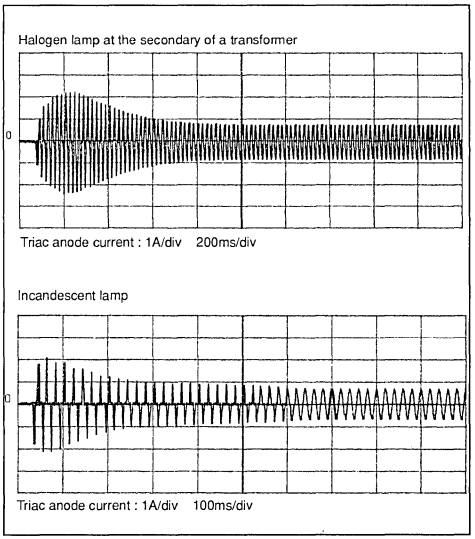
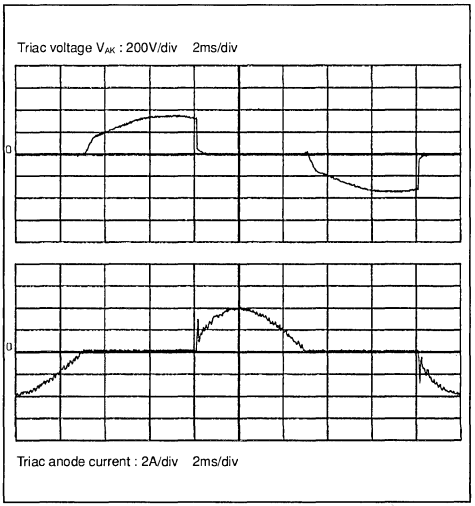


Figure 9. Universal Motor Drive



PRACTICAL RESULTS (Continued)

Due to the soft start, the peak in-rush current is about 3 times the nominal current compared with 10 to 15 times without soft start. This extends the lamp life time and prevents the input fuse from blowing.

The figure 9 shows the current and voltage in a triac driving a universal motor.

SUMMARY

Microcontrollers (MCU) are in common use in most areas of electronics. They now penetrate the very cost sensitive arena of home appliance applications.

The application described in this paper shows that enhanced appliance circuits can be designed with fast prototyping time using a ST6210 MCU and a BTA08-600SW LOGIC LEVEL triac. These circuits are low cost and provide more features with less components than classical solutions.

The circuit presented is an enhanced light dimmer operating from the 120V/240V mains. It drives incandescent and halogen lamps supplied either directly from the mains or through a low voltage transformer. The same circuit can also drive a universal motor. It includes soft start and protection features. Different user interfaces can be chosen: touch sensor, push button or potentiometer.

All this is achieved with only few components: a ST6210 MCU in PDIP/PSO package with a BTA08-600SW LOGIC LEVEL triac in TO220 package and some passive components.

Additional features like presence detection, IR remote control, homebus interface, motor speed control or 60Hz operation can be implemented from the existing solution.

Bibliography

Thyristors and triacs application manual 1989

Microcontroller based universal motor speed control . M.Querol / SGS-Thomson Microelectronics

Application Note:

Universal Motor Speed Control / P.Rault + Y.Bahout / SGS-THOMSON Microelectronics

ANNEX : Choice of a triac driven by a MCU.

When the software includes a soft start, the inrush current in the load and therefore the current rating in the triac can be reduced.

When using a LOGIC LEVEL or a SNUBBERLESS triac the current rating of the triac can be reduced, keeping fast commutation characteristics. For instance, a LOGIC LEVEL triac BTA08-600SW can drive a 600W lamp and a SNUBBERLESS triac BTA10-600BW a 1200W universal motor.

LOGIC LEVEL triacs are optimized on the drive view point. Therefore they can be driven directly by the ST621X I/O.

SNUBBERLESS triacs are optimized on the power view point, so they can drive loads which generate very strong dynamic contraints.

These triacs are specified in a way that their behaviour can be pre-determined. The tables below present with two examples the relation between the major application constraints and the key parameters of the triac.

LIGHT DIMMER

Constraint	Key parameters on a LOGIC LEVEL triac BTA08-600 SW
Simple Drive	I_{GT} = 10mA - V_{GT} = 1.5V
No flicker	I_H = 25mA
Max power on the load	I_{RMS} = 8A
Max inrush current	$(dI/dt)_C$ = 4.5A/ms
No flashing (1)	I_{TSM} = 80A
Flash over (filament failure)	

Note 1 : When the lamp is cold (start or low light intensity), there must not be spurious turn-on of the triac (flashing) due to a high commutation dI/dt.

UNIVERSAL MOTOR DRIVE

Constraint	Key parameters on a SNUBBERLESS triac BTA10-600 BW
Simple drive	I_{GT} = 50mA - V_{GT} = 1.5V
Max. start current	I_{TSM} = 100A I_{RMS} = 10A $(dI/dt)_C$ = 9A/ms dV/dt = 500V/µs
Max. power on the load	
Fuse sizing	I^2t = 50A^2.s

TRIAC CONTROL BY PULSE TRANSFORMER

Ph. Rabier

Among the many ways to drive a triac the pulse transformer is one of the easiest. By applying some simple rules it can be used to design an efficient triac triggering circuit without reduction of the commutation capability of the triac.

I. WHY USE A PULSE TRANSFORMER ?

The use of pulse transformers in triac triggering circuits offers many advantages :

- galvanic insulation between the power and gate drive circuit (a few kV).
- gate drive circuit with a few components.
- choice of the gate current polarity (triggering in the 2nd and 3rd quadrants for SNUBBERLESS triacs).
- optimization of gate signal (single pulse or train of pulses).
- possibility to drive several triacs with only one drive circuit

II. THE PULSE TRANSFORMER :

To optimize the triac and the pulse transformer in the application it is necessary to know the main characteristics of the transformer :

1/ The transformer ratio :

It is the N2/N1 ratio, where N1 corresponds to the primary winding and N2 to the secondary.

2/ The Lp inductance :

the primary winding inductance measured at a given frequency.

3/ The Rp resistance :

The primary winding resistance

4/ The area of the output pulse :

For a given magnetic material the voltage.time product Vo.to of the output pulse is constant. For each type of transformer the manufacturer gives the maximum voltage.time product under no load operation which corresponds to the figure 1.

5/ The rise time tr :

This parameter tr defines the rise time of the output pulse as shown in figure 2.

Figure 1 : Voltage across the secondary winding for a rectangular pulse across the primary.

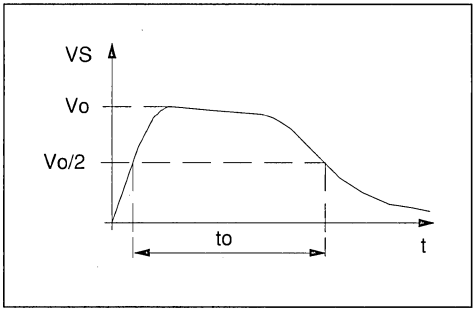


Figure 2 : Specification of the rise time at the output of the transformer.

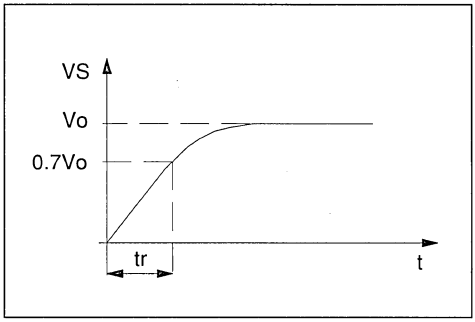
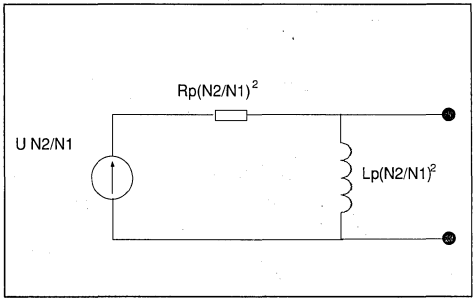


Figure 3: Equivalent diagram of the transformer.



The figure 3 shows the diagram of the secondary of the transformer :

III. GATE PULSE :

1/ Peak value :

The transformer ratio and the power supply of the primary winding define the secondary voltage. With the equivalent diagram and triac gate characteristics it is possible to determine the output current. This has to be higher than the specified gate triggering current (IGT). To have an efficient triggering it is suitable to use a safety coefficient of 2 :

$$I_G > 2\, I_{GT}$$

2/ Duration :

The Vo.to product defines the maximum pulse duration at the output of the transformer. The anode current has to be higher than the specified latching current (IL) at the end of the gate pulse.

For drives with a pulse train we can sometimes use very short pulses (for example tp =10µs with a 15µs cycle).

For proper triac triggering the gate current rise time is very important in a circuit with very high di/dt (>20 A/µs) : case of resistive load.

IV. THE COMMUTATION :

The use of a triac with a pulse transformer needs some precautions in order not to decrease the commutation capability.

1/ The commutation :

Review : during the conduction a certain quantity of charges is injected into the triac.

During the fall of the current most of them disappear by recombination. If the current decreases too fast the charges do not have time to recombine and some charge stays in the gate area. This can provoke a spurious firing.

The parameter which characterizes the commutation is the anode current slope (di/dt)c, that is to say the slope of current before zero crossing.

The specified value in the data sheet is the critical (di/dt)c. Above this value the triac is liable to fire spuriously. Figure 5 shows the spurious firing due to (di/dt)c.

2/ Case of a triac triggered by a transformer :

When the triac is on, a voltage of about 0.6 V appears across the gate and cathode. This voltage is either positive or negative depending on the anode current polarity. A current i can flow through the secondary winding of the transformer (see figure 4).

Due to the inductance of the transformer, at the end of the half wave the current i continues to flow in the gate and increases the risk of spurious firing at the next cycle. (figure 5).

Figure 4 : Use of a triac with a pulse transformeur : when the Triac is on a current i flows through the gate.

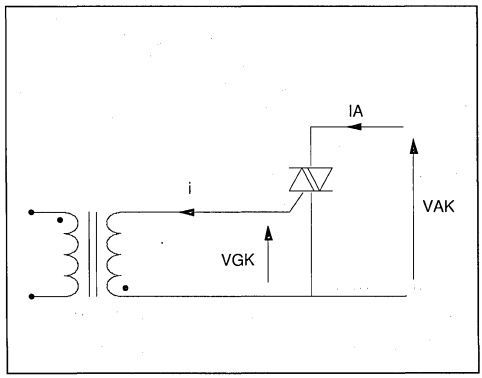
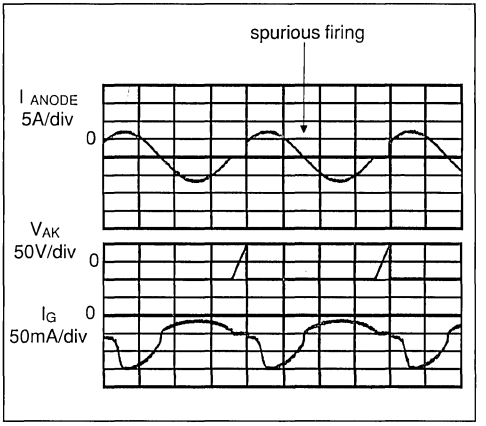


Figure 5: Spurious firing of the triac.



The influence of the transformer can be estimated by measuring the critical (di/dt)c of the triac with and without the transformer.

Example : BTA06-400CW

The specified (di/dt)c of this triac is :

3.5 A/ms min at Tj = 125°C

Measurement of a sample without transformer :

(di/dt)c = 6 A/ms

Measurement with transformer :
(di/dt)c = 3 A/ms → on this sample the commutation capability is divided by 2 !

It is necessary to consider this phenomena and to take some safety margin (in some cases the critical (di/dt)c of the triac + transformer can be lower than the specified (di/dt)c of the triac as shown in the previous example). This is very important in the case of transient currents higher than the nominal value, as is the case with the cold filament of incandescent lamp, load dispersion, etc...

One has to take into account the maximum (di/dt)c in the application in all cases, especially in the transient state where (di/dt)c can be higher than it is in the steady state. The following example shows values for an incandescent lamp and universal motor.

	INCANDESCENT LAMP	UNIVERSAL MOTOR
NOMINAL CURRENT $I_{A_{RMS}}$	1.35 A	3.8 A
STEADY STATE (di/dt)c	0.6 A/ms	1.7 A/ms
TRANSIENT STATE (di/dt)c	2.6 A/ms	5 A/ms

V. THE SOLUTION :

To avoid the reinjected current through the transformer it is necessary to connect a diode in series with the gate (figure 6).

The drop voltage V_F of the diode avoid the reinjected current. The triac is triggering in the 2nd and 3rd quadrants (figure 7).

Figure 6 : Bearing of the commutation capability.

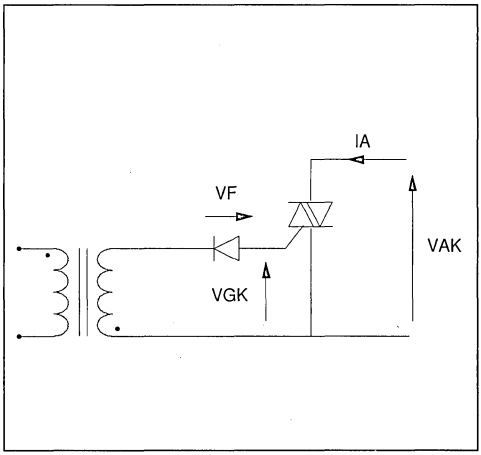


Figure 7 : Correct running with diode.

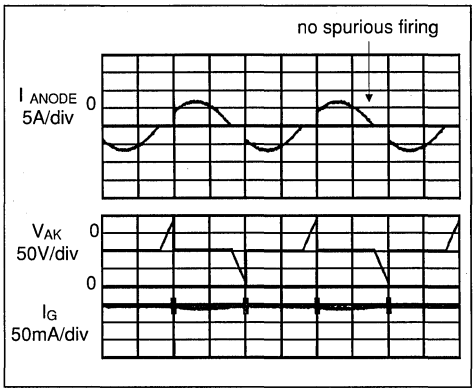
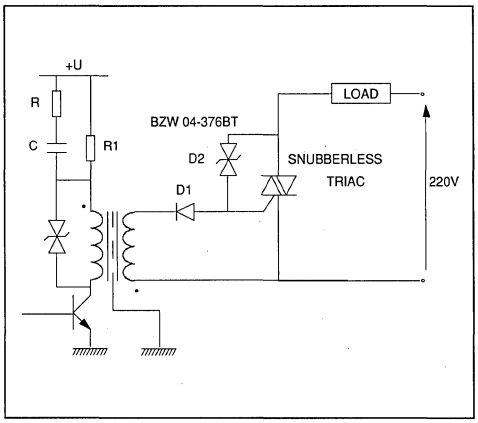


Figure 8: Typical application diagram.

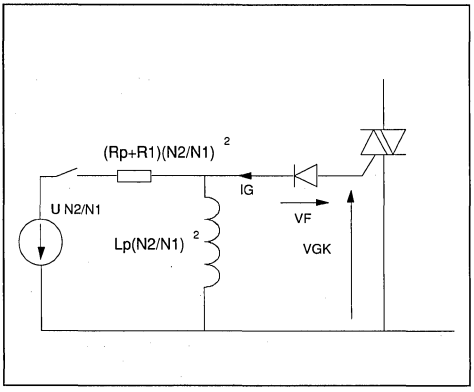


VI. TYPICAL APPLICATION EXAMPLE :

The D2 transil diode protects the triac against overvoltages (see "Protection of triacs and their control circuits" in the "Thyristors and Triacs Application manual").

The RC circuit across R1 allows an increase in the current in the transformer at the beginning of the pulse. When C is charged the resistance R1 limits the current through the transistor.

Figure 9: Equivalent diagram.



The gate current is given by the following formula (without RC).

$$I_G = \frac{(V_{GK} - V_F)tp}{L_p\left(\frac{N2}{N1}\right)^2} + \frac{V_{GK} - V_F + U\left(\frac{N2}{N1}\right)^2}{(R_p + R1)\left(\frac{N2}{N1}\right)^2}$$

Where : tp is the pulse duration

Keep in mind that V_{GK} is negative because the triac is triggering in the 2nd and 3rd quadrants.

In practice the area of the pulse has to be lower than 60 or 70% of the maximum voltage.time product Vo.to.

The maximum pulse duration in the output is :

$$tp = \frac{0.7\ Vo.to}{V_F - V_{GK}}$$

These two formulae allow us to define the pulse transformer according to the triac sensitivity.

Example : Numerical application with a transformer having the following characteristics :

N2/N1 = 1 Rp = 0.6 Ohm
Lp = 2.5 mH Vo.to = 250 Vµs

Triac : BTA08-700CW

I_{GT} = 35 mA V_{GK} = -2 V at $I_G = 2\ I_{GT}$ (quadants II and III)

diode : V_F = 0.7 V
power supply :

U = 12 V
R1 = 100 Ohms
tp max = 65 µs
I_G = 70 mA
t = 21 µs

We have measured :

I_G = 85 mA at t = 21µs

VII. CONCLUSION :

The pulse transformer provides an excellent method to trigger a triac when galvanic insulation is required. This system is appropriate to microprocessor systems.

Nevertheless it needs some precautions to avoid a decrease of the triac commutation behavior. This precaution is achieved by adding a diode in series with the gate.

NEW TRIACS : IS THE SNUBBER CIRCUIT NECESSARY ?

T. Castagnet

On inductive load triacs are designed with RC snubber : these commutation aid networks are badly optimized in most of applications.

The subject of this paper is, first of all, to analyze the functions of snubber circuits for triacs and to propose calculation methods.

But today snubber circuits must be reconsidered by taking into account the progress of the triac technology. This article explains how it is now possible to reduce or to eliminate the snubber, and thus simplify the AC switch function, thanks to the high performance in commutation of the SNUBBERLESS™ triacs.

INTRODUCTION:

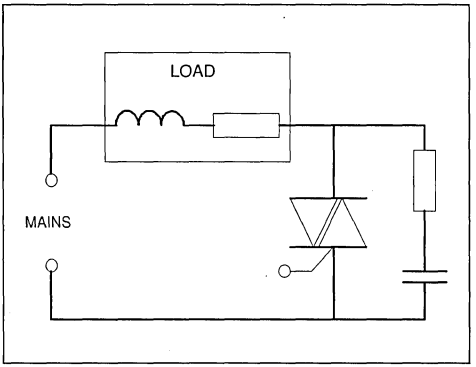
The triac is today the only bidirectional device able to control various loads supplied by the domestic and industrial mains. It is often designed with a network made of a resistor R and a capacitor C, the SNUBBER circuit.

This circuit improves the operation of the triac in its environment but what is its real function ?

USE OF THE SNUBBER CIRCUIT ASSOCIATED WITH TRIACS.

The main function of this circuit is to improve the switching behavior of the triac at turn off : we will explain how and suggest some methods to define it.

Figure 1 : Synoptic of application circuit with triac.



DESCRIPTION OF THE TRIAC COMMUTATION.

The triac is a device similar to two SCR back to back with a common control area.
At turn off the commutation of the triac is the transient phase during which the load current is passing through zero and the circuit voltage is reapplied to its terminals.

Figure 2 : Example of triac structure and its equivalent simplified circuit.

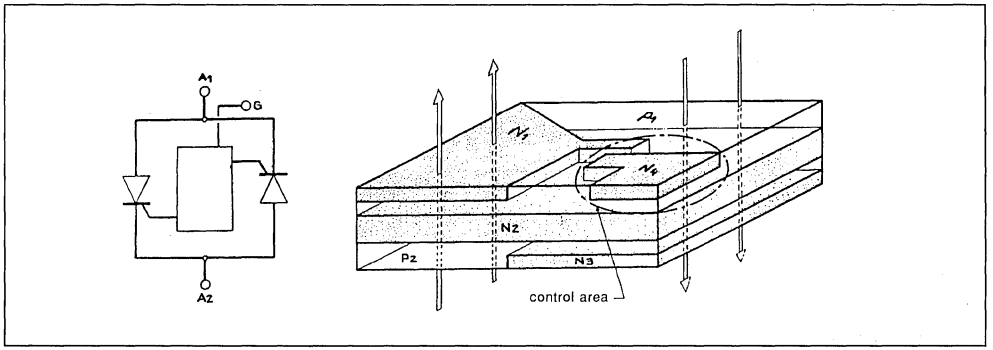
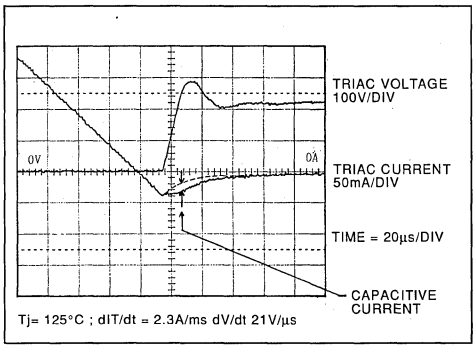


Figure 3 : Commutation on inductive load of BTB10-600BW



PARAMETERS OF COMMUTATION.

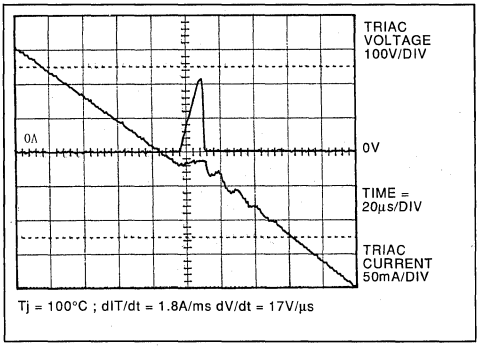
For a given device and a determined junction temperature the risk of a spurious firing is possible. It is linked to:

The rate of removal of the triac current dI_T/dt before zero crossing because it determines the quantity of stored carriers which could be injected in the gate area or the opposite thyristor ;

The rate of rise of the reapplied triac voltage, dV/dt, which creates a current through the gate because of the junction capacitance.

The parameters which characterize the performance of the triac commutation are the critical rate of removal of the current $(dI/dt)_c$ and the critical rate of rise of voltage, $(dV/dt)_c$: above these values the triac fires again spontaneously.

Figure 4 : Spurious firing at commutation for a BTB06-600S



MAIN HYPOTHESIS ON COMMUTATION :

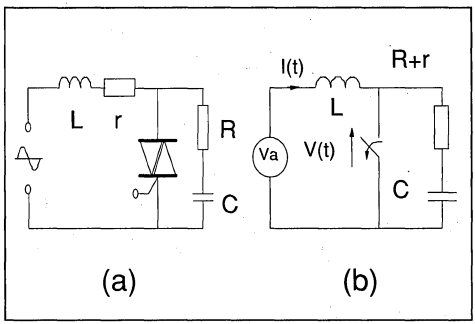
The analysis of commutation shows that :

At turn off a recovery current, I_R,appears commonly when $dI_T/dt > 0.1 \times (dI/dt)_c$; (see fig. 3).

The circuit voltage V_a is reapplied to the device when $I_T = I_R$;

The spurious firing is possible as far as there is a reverse current (made of recovery or capacitive current) : mean while each dV/dt is able to provoke the triac refiring ; (see fig. 4).

Figure 5 : Application circuit (a) and its equivalent diagram at commutation (b).



AIM OF THE SNUBBER CIRCUIT.

The today method to choose a triac on inductive load consists in :

- selecting one triac with RMS current, I_{TRMS}, suitable with dI_T/dt of circuit ; because for conventional triac the specified $(dI/dt)_c$ values is linked to the current rating by the relation :

$$(dI/dt)_c = 2 \times \Pi \times f \times \sqrt{2} \times I_{TRMS}$$

This value must be higher than dIT/dt of circuit.

- limiting the maximum reapplied dV/dt below the specified value $(dV/dt)_c$: this is the main function of the snubber circuit.

CHOICE OF THE SNUBBER CIRCUIT.

The aid circuit makes up a resonant circuit with the load. At turn off it limits the slope of reapplied voltage dV/dt but generates an overvoltage V_M. Its choice results of a compromise in order to respect triac specification ($(dV/dt)_c$ and repetitive peak off state voltage (V_{DRM}).There are two possibilities :

1/ for low V_{DRM} the resonant circuit must be damped, reducing V_M and dV/dt - (§ 2 of annex) ;

2/ with higher voltage possibilities the circuit can oscillate and the capacitor adjusts straightly the dV/dt (§ 3 of annex)

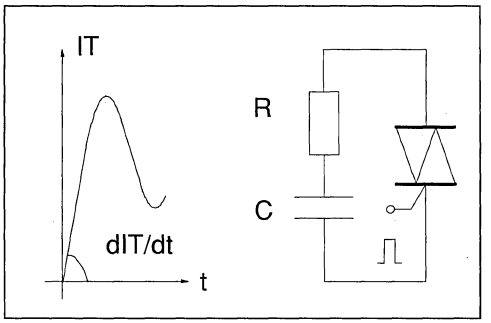
Today we use commonly triacs with V_{DRM} = 600 V or more. Therefore we suggest the second way because capacitor is smaller (reduced 4 times).

THE DISADVANTAGES OF THE SNUBBER CIRCUIT.

The snubber circuit improves the triac behavior but it imposes to the device stresses which limit its use .

At turn on the discharge of the capacitor creates a pulse current with high repetitive dIT/dt which can destroy the triac by local overheating near the gate. It is recommended to limit the amplitude of current with a resistor higher than 50 Ohms and the turn on dI/dt below 20 A/µs.

Figure 6 : Triac turn on with snubber circuit



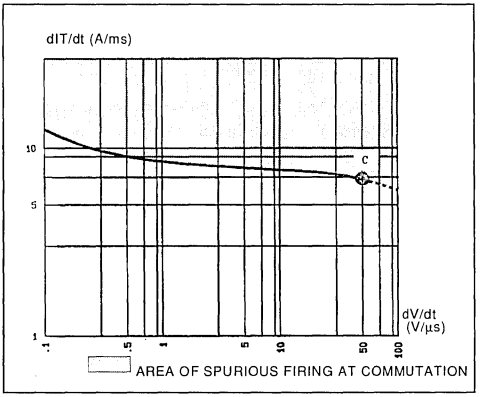
The current, which flows through the snubber circuit when the triac is off decreases the off state quality of the switch : this leakage current (several mA) could create problems for small loads like electro-valves, micro motors.....

PROGRESS MADE ON TRIACS.

PREDOMINANCE OF $(dI/dt)_c$ AND LIMITATION OF dV/dt :

The study of the commutation behavior of triac can be made thanks to the curve of the critical commutation performance of each sample : $(dI/dt)_c$ versus various reapplied $(dV/dt)_c$.

Figure 7 : Critical $(dI/dt)_c$ versus $(dV/dt)_c$ for BTB10-600B sample



For a conventional triac (I_{GT} > 25 mA) the critical $(dI/dt)_c$ is not much sensitive to the $(dV/dt)_c$: so it represents the most significant parameter to characterize the triac behavior in commutation (fig.7).
Without snubber circuit the $(dV/dt)_c$ is limited by the junction capacitance of the triac (point C).

In order to improve commutation behavior of triac and to eliminate the snubber circuit the parameter $(dI/dt)_c$ has to be increased on all range of dV/dt.

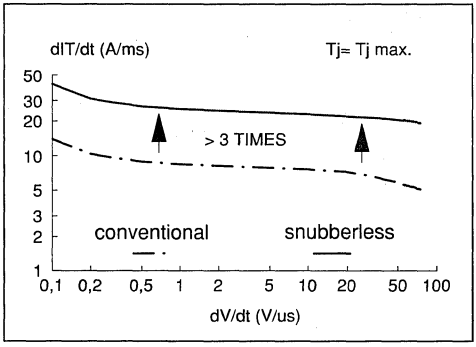
We also notice the efficiency of the snubber circuit in commutation -$(dI/dt)_c$- is lower than two by reduction of dV/dt from its natural limitation (point C) to 0.1V/µs.

PERFORMANCES OF THE SNUBBERLESS TRIACS :

This analysis permitted the development of new triacs with better performances in commutation : the SNUBBERLESS triacs which have got a new design with improved triggering mechanism and better decoupling of single integrated thyristors.

For same size and gate sensitivity the improvement ratio on $(dI/dt)_c$ is higher than 3.

Figure 8 : Comparison between conventional and snubberless 10 A triacs.



So we can specify now the commutation behavior with $(dI/dt)_c$ for a value dV/dt from 0 to its natural limitation by the junction capacitance (without snubber circuit).

Table 1 : Commutation specification $(dI/dt)c$ of some SNUBBERLESS triacs (A/ms)

CURRENT RANGE (A)	TRIAC SUFFIX			dI/dt on 50Hz sine pulse (A/ms)
	AW	BW	CW	
6	8	5	3.5	2.7
10	12	9	5.5	4.4
16	21	14	8.5	7
25	33	22	13	11.1

CONSEQUENCES ON APPLICATION CIRCUITS :

The SNUBBERLESS triacs offer application advantages :

- The function of commutation aid of the snubber circuit disappears : we can remove it ;

- In application the dI_T/dt through the triac is not adjustable because it is given by the circuit (V_a and L) ; its measure permits the choice of this triac with the commutation parameter, $(dI/dt)_c$.

- The commutation behavior is no more straightly linked to the current range and the high $(dI/dt)_c$ allows a reduction of the die size.
For example a universal motor of 1200 W - 220 V can be driven by a BTB10-600 BW (*) instead of the BTB15-600B(**).

(*) 10 Amps SNUBBERLESS triac with V_{DRM} = 600 V and I_{GT} = 50 mA; specified at 9 A/ms without snubber.

(**) 15 Amps conventional triac with V_{DRM} = 600 V and I_{GT} = 50 mA; specified at 6.7A/ms with dV/dt limited to 10 V/µs.

IS IT ALWAYS POSSIBLE TO REMOVE THE SNUBBER CIRCUIT ?

The answer is not in the affirmative because sometimes it has other functions :

- improvement of the triac immunity against transients in the off state ;

- compensation of latching current at turn on (not dealt in this paper).

Switching on and voltage perturbations can provoke overvoltages and fast voltage variations across the triac :

- this one could break over when the overvoltages are higher than its repetitive peak off state voltage, V_{DRM} ;
- due to the junction capacitance fast voltage variations create a gate current and could trigger the triac; the device limit is the rate of rise of the off-state voltage, dV/dt.

The snubber circuit can improve the triac behavior in off-state. But its efficiency is linked to the values of series inductance L at the oscillation frequency of perturbations (typically 100 kHz).

We could add a saturable inductor in series with the triac when L is too low : particularly this is the case of resistive load.

IMPROVEMENT OF THE IMMUNITY TO TRANSIENT VOLTAGES (STATIC DV/DT) :

When the circuit has its specific overvoltage suppressor, as clamping diodes (TRANSIL), the aim of the snubber circuit is to reduce only dV/dt for

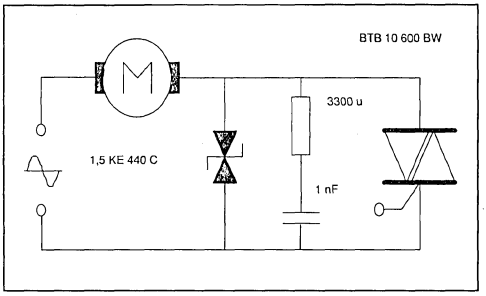
triac voltage lower than V_{DRM}. It must be damped, limiting its overvoltage and the current in the suppressor. The § 2 of annex permits to choose the values :

$$C > 3 \times (V_{DRM})^2 / (L \times (dV/dt)^2)$$

$$R < 0.8 \times L \times (dV/dt) / V_{DRM}$$

For a 1200 W motor with L (100 kHz) # 5 mH a BTB10-600BW triac needs a snubber circuit of 3.3 kΩ and 1 nF (fig.8).

Figure 9 : Example of improved off-state immunity for triac



PROTECTION AGAINST OVERVOLTAGES :

The snubber circuit could be a simple circuit in order to reduce overvoltage V_M. It must operate as a low pass filter with minimum resistance (50 Ohms) avoiding turn on current stresses.

Figure 10 : Snubber circuit efficiency against overvoltage V_{PP} (Triac voltage<600V)

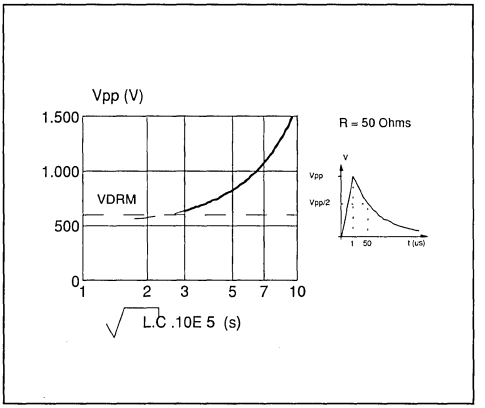


Figure 10 shows the maximum allowed overvoltage V_p versus $\sqrt{L \times C}$ remaining the triac voltage below 600 V.

But the efficiency of this circuit is poor and we prefer use other ways of overvoltage protection : input filters and suppressor (see fig.8).

CONCLUSION :

Used today as commutation aid network the snubber circuit can be well optimized thanks to higher blocking voltage V_{DRM} : we obtain a reduction of the capacitor size.

But with the SNUBBERLESS triacs the aid function of the snubber circuit disappears. Because of the improvement of the commutation performance (higher critical $(dI/dt)_c$) these new triacs offer a cost reduction by decreasing of their size, and permit to eliminate the snubber circuit in most of applications.

However the snubber circuit, associed to series inductance, could limit the off state voltage variations. But its efficiency against overvoltages is poor and we prefer to replace it by specific protection devices.

REFERENCES :

- Improvement in the triac commutation 1989. P.RAULT SGS THOMSON-Microelectronics.

- Analysis and design of snubber networks for dv/dt suppression in triac circuits (RCA) AN 4745 - 1971
JE WOJSLAWOWICZ.

- For energy conversion and motor control - triacs or alternistors.
Pierre RAULT and Jean Marie PETER ; THOMSON CSF for PCI September 1982.

Annex :

DETERMINATION OF THE COMPONENTS OF SNUBBER CIRCUIT.

• **1 -** SNUBBER CIRCUIT OPERATION

The load inductance L and the snubber circuit make up a resonant circuit across which the mains voltage is reapplied at turn off. The RC circuit limits dV/dt but generates an overvoltage V_M which must be lower than V_{DRM}.

We can analyse V_M and $(dV/dt)_{max}$ with their relative parameter versus the damping factor F :

Figure A1 : overvoltage (e) versus damping factor F.

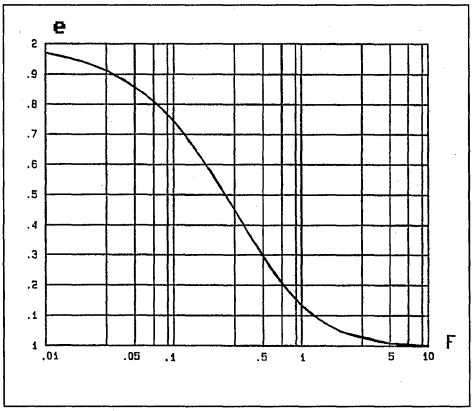
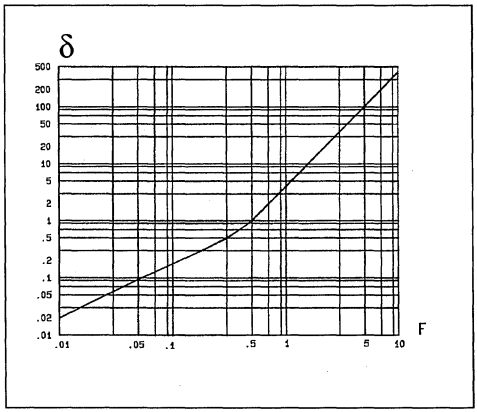


Figure A2 : rise slope (δ) versus damping factor F.



$$e = V_M / V_a$$

$$\delta = R \times C \times \left({}^{dV}/_{dt} \right)_{MAX} / V_a$$

$$F = R \times \sqrt{C/L} / 2$$

These curves show there are two intervalles where variations if F -due to the tolerance of the components- don't almost modify the overvoltage value :

$$F > 0.5 \text{ and } F < 0.1$$

Therefore these are the two methods in order to choose the snubber circuit.

• **2 -** DETERMINATION OF THE SNUBBER CIRCUIT WHEN F > 0.5 :

V_M is limited first of all (e < 1.3) thanks to the capacitor C ; the resistance R sets the slope $(dV/dt)_{max}$.

$$R \times \sqrt{{}^{C}/_{L}} / 2 > 0.5 \text{ and } \left({}^{dV}/_{dt} \right)_c > V_a \times R / L$$

However F must be low (F = 1) in order to reduce the capacitor and the resistor dissipation power P_R :

$$C > 4 \times (Va)^2 / (L \times \left({}^{dV}/_{dt} \right) c^2)$$

and

$$R < L \times \left({}^{dV}/_{dt} \right)_c / V_a$$

with

$P_R < 2.C.Va^2.f$
$V_M/V_a < 1.2$
$V_a = V_{ac} \times \sqrt{2} \times \sin\phi$
V_{ac} = RMS mains voltage
f = mains frequency
$\cos\phi$ = power factor of load
L = inductance of load when zero crossing
r = resistance of load

An inductive load of 2000 VA - $\cos\phi$ = 0.6 on 220 V - 50 Hz mains can be controlled with a

triac specified @ $(dV/dt)_c$ = 10 V/µs by using :

C = 30 nF and R = 3.5 kOhms

with
L = 100 mH
r = 40 Ohms
P_R = 0.23 W
V_M = 332 V (choose a triac with V_{DRM} = 400 V)

• **3** - DETERMINATION OF THE SNUBBER CIRUIT F< 0.1 :

dV/dt is optimized first of all (δ < 0.18) thanks to the capacitance C ; V_M is only set by the resistance R :

$$R \times \sqrt{C/L}/2 < 0.1 \quad \text{and} \quad (dV/dt)_c > V_a/(L \times C)$$

The resistance value has to keep a sufficient value (F = 0.05) in order to limit stresses on triac at turn on (see 1.5)

$$C > V_a{}^2/(L \times (dV/dt)_c{}^2)$$

and

$$R + r < 0.1 \times L \times (dV/dt)_c / V_a$$

with
$P_R < 2.C.Va^2.f$
$e = V_M/Va < 1.9$
$V_a = V_{ac} \times \sqrt{2} \times \sin\phi$

With the same load 2000 VA - $\cos\phi$ = 0.6 on 220 V - 50 Hz mains and with the same triac :

C = 10 nF and R = 300 Ohms

P_R = 0.08 W
V_M = 525V (choose a triac with V_{DRM}=600 V)

• 4 - COMMENTS :

Today the triac offers blocking voltage V_{DRM} up to 800 V : so we suggest the second method because the capacitor is smaller, (reduced by 4) and the reapplied slope dV/dt is less sensitive to damping factor variation and so better controlled.

These values obtained by calculation are slightly overrated because the real slope of the reapplied voltage is limited also by the junction capacitance of triac.

TRIAC + MICROCONTROLLER SAFETY PRECAUTIONS FOR DEVELOPMENT TOOL

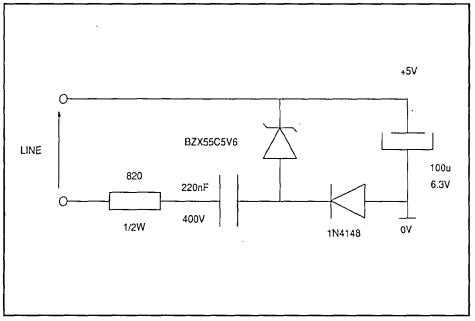
Ph. Rabier

The goal of this paper is to analyse the different ways to configure a micro-controller and a development tool during the debbugging phase. The major problem is due to the direct connection of the computer I/O lines with the mains power. Some precautions have to be taken during the emulation in order to avoid destruction.

I - LOW COST POWER SUPPLY

In most low cost applications the step down transformer is not used and the power supply delivers low current, as shown for example in figure 1.

Figure 1 : Uninsulated power supply.



In domestic appliance applications, one of the most important power switches is the triac.

The function of driving the triac becomes more and more complex. For this reason, microcontrollers are becoming more and more common. Furthermore, sensitive triacs with high commutation parameters, for example LOGIC LEVEL triacs can be triggered directly by the microcontroller without any buffer. Sensitive triacs and microcontrollers allow decrease in power consumption.

In this way the power supply can be optimized to reduce the cost. Optimisation can be achieved by removing the transformer.

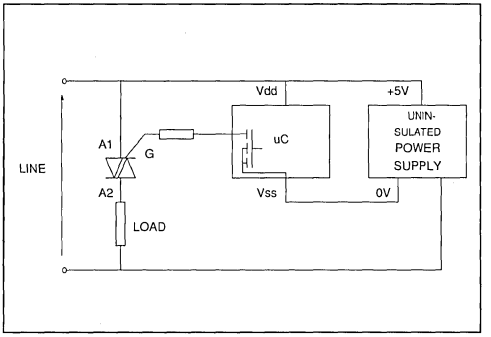
The consequence is that there is no insulation, the microcontroller is connected directly on the line !

When the software is emulated on the application board, the output port (RS232 port) of the computer is connected on the line via the emulator.

If some precaution is not taken "something" will be destroyed !

Figure 2 gives an example of an application using a triac and a microcontroller.

Figure 2 : Triac and microcontroller on the line.



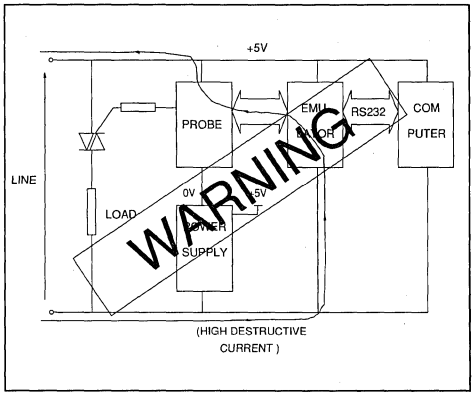
In this case the micro-controller is supplied by an uninsulated +5 V power supply connected directly to the line, and a low level (0V) on the output ports of the micro-controller is needed to trigger the triac.

II - USE OF A DEVELOPMENT TOOL

During the debbuging phase, the micro-controller is removed and is replaced by the emulation probe. The circuit corresponding to the emulation phase of the previous example is shown in fig. 3.

The line is connected directly to the +5V of the emulator and a high (destructive) current can flow through the emulator and/or the computer.

Figure 3 : Circuit without protection
(Beware : this circuit is dangerous).

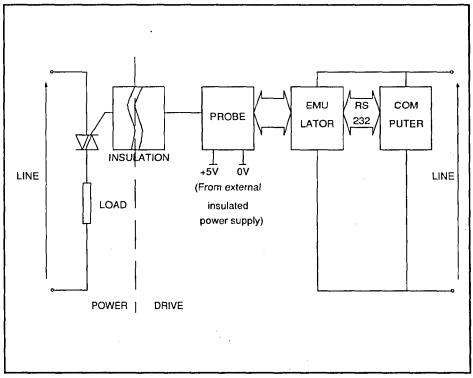


III - INSULATED SYSTEM

To avoid destruction of the development tool it is necessary to have an insulation between line and probe. This insulation can be achieved by optocouplers, pulse transformers, or insulation transformers.

Figure 4 shows the topology of the most common insulation.

Figure 4 : Conventional insulation.

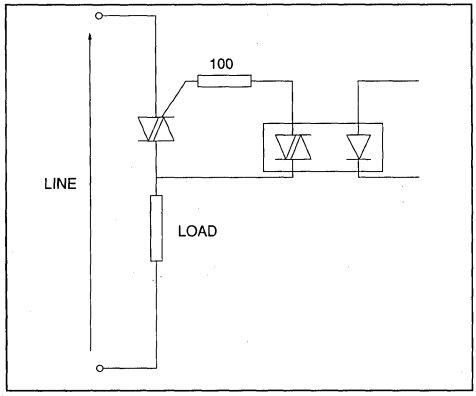


1/ Optotriac

Figure 5 shows the circuit with triac and optotriac.

The triac is working in the 1st and in the 3rd quadrants.

Figure 5 : Optotriac drive.



The main advantage of a such system is the low cost of the optotriac, but it needs an isolated auxiliary power supply.

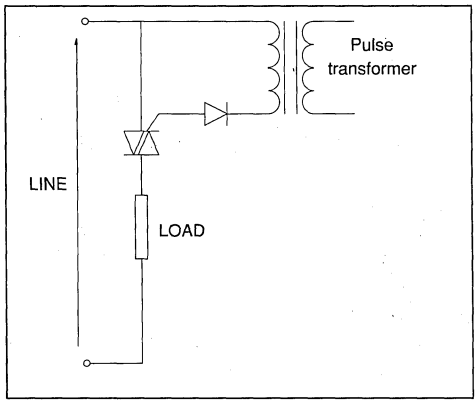
For a zero crossing optotriac, the triac is triggering with a gate current equal to the gate trigger current with a very low dI_G/dt. This does not allow high di/dt at turn on. That is to say the control of high current resistive load is not recommended with this method.

2/ The pulse transformer

Figure 6 shows the circuit with a triac and a pulse transformer.

The triac is working in the 2nd and 3rd quadrants.

Figure 6 : Pulse transformer insulation.



This system is simple to use when the triac was initially driven by a buffer transistor, but it needs an external power supply. The high dI_G/dt through the gate allows high current resistive loads to be driven. Due to the saturation of the magnetic material, this system cannot drive small loads because the gate current is cancelled before the latching current has been reached.

For more information refer to the application note "Triac control by pulse transformer".

3/ The line insulation transformer

In the previous examples,the insulation was between the triac and the microcontroller.

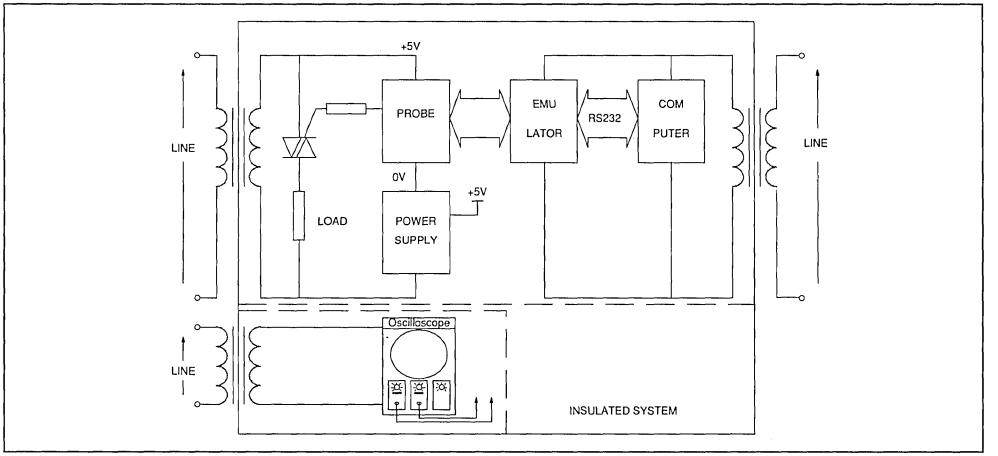
Another solution is to supply each equipment connected to the board from the mains through an insulation transformer.

If an oscilloscope is used, it also has to be separately insulated.

The main advantage of this system is that we do not need to modify the target system during the debbuging phase and it can be used with the microcontroller.

When a transformer is used between line and triac it should be noted that the line impedance is modified and then the behaviour of the triac, load and line set can be different (waveform of current).

Figure 7: Insulation with transformers.



IV - SUMMARY

New LOGIC LEVEL and SNUBBERLESS triacs can be connected directly to the microcontroller without buffers or insulation. Furthermore, low cost power supplies without a transformer are becoming more common. There is an increasing number of applications supplied directly from the mains, and the microcontroller is directly connected to it.

During the debbuging phase when connecting the development tool, a galvanic insulation is absolutely necessary.

This insulation can be done in 3 ways :

- With optotriacs :
  - Need modifications on the target system
  - Need external power supply
- With pulse transformer :
  - Need modifications (transistor to drive the pulse transformer)
  - Need an external power supply
  - Cannot drive small loads
- With insulation transformer :
  - No modification on the application board.
  - Modification of the line impedance due to the transformer between line and load.

Therefore a microcontroller operating on the mains with a triac may be directly connected to the line.

IMPROVEMENT IN THE TRIAC COMMUTATION

P. Rault

In the last few years, the use of triacs has spread to all areas of electronics, including domestic appliances and industrial applications.

The use of triacs has been traditionally limited by their switching behavior in applications where there is a risk of spontaneous firing after conduction. In order to obtain the required reliability in today's equipment, the designer must take a certain number of precautions: over dimensioning of the device, switching aid networks (snubber), significant margin of security of the junction temperature,etc. This generally involves additional costs.

After a brief discussion of commutation problem when a triac is turned off, this article will describe the progress made in this area and the newest possibilities now offered to triac user thanks to the new series Logic Level and SNUBBERLESS™ triac.

THE COMMUTATION PROBLEM OF THE TRIAC

In its electrical representation the triac can be compared to two thyristors mounted in anti-parallel and coupled with a control device which allows activation of this AC switch with only one gate (fig. 1a).

In considering the structure of a triac (fig. 1b), one notices that the conduction zones, corresponding to these two thyristors and which control the current in one direction and then in the other, narrowly overlap each other and the control zone.

During the conduction time, a certain quantity of charges is injected into the structure. The biggest part of these charges disappears by recombining during the fall of the current in the circuit, while another part is extracted at the moment of blocking by the inverse recovery current. Nonetheless an excess charge remains, particularly in the neighboring regions of the gate, which can provoke in certain cases the firing of the other conduction zone at the moment when the supply voltage of the circuit is reapplied across the triac. This is the problem of commutation.

For a given structure at a determined junction temperature, the switching behavior depends on:

1/ The quantity of charges which remains at the moment when the current drops to zero. this number of charges is linked to the value of the current which was circulating in the triac approximately 100 microseconds before the cut-off. (This time corresponds to two or three times the life time of the minority carriers). Thus, the parameter to consider here will be the slope of the decreasing current which is called the commutating di/dt, or (di/dt)c. (fig. 2)

2/ The speed at which the reapplied voltage increases at the moment when the triac turns off, which is called the commutating dv/dt, or (dv/dt)c. (fig. 2)
A capacitive current, proportional to the (dv/dt)c, flows into the structure, and therefore injected charges are added to those coming from the previous conduction.

Figure 1 : (A) Simplified equivalent schematic of triac circuit.
(B) Example of a triac structure.

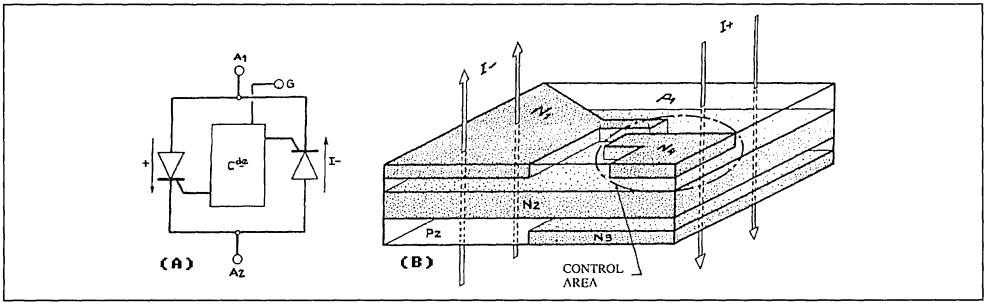
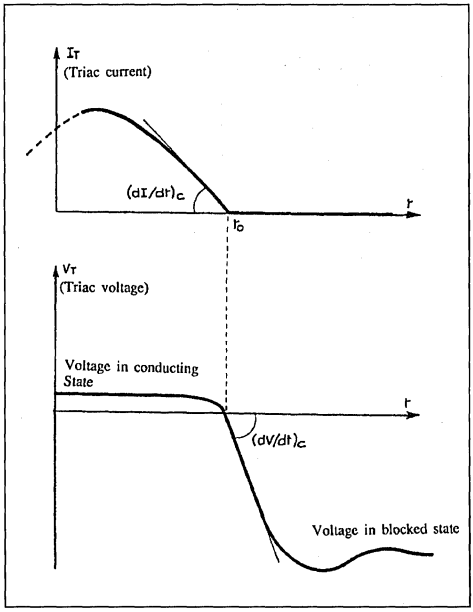


Figure 2 : Triac voltage and current at commutation.



CHARACTERIZATION

In order to characterize the switching behavior of a triac when it turns off, we consider a circuit in which we can vary the slope of the decrease in current (di/dt)c. In addition, we control the slope of the reapplied voltage by using, for example, a circuit of resistors and capacitors connected across triac to be measured. For a determined (dv/dt)c, we progressively increase the (di/dt)c until a certain level which provokes the spontaneous firing of the triac. This the critical (di/dt)c value.

Therefore, for different (dv/dt)c values, we note the critical (di/dt)c value for each sample. This makes possible to trace the curve of the commutation behavior of the triac under consideration.

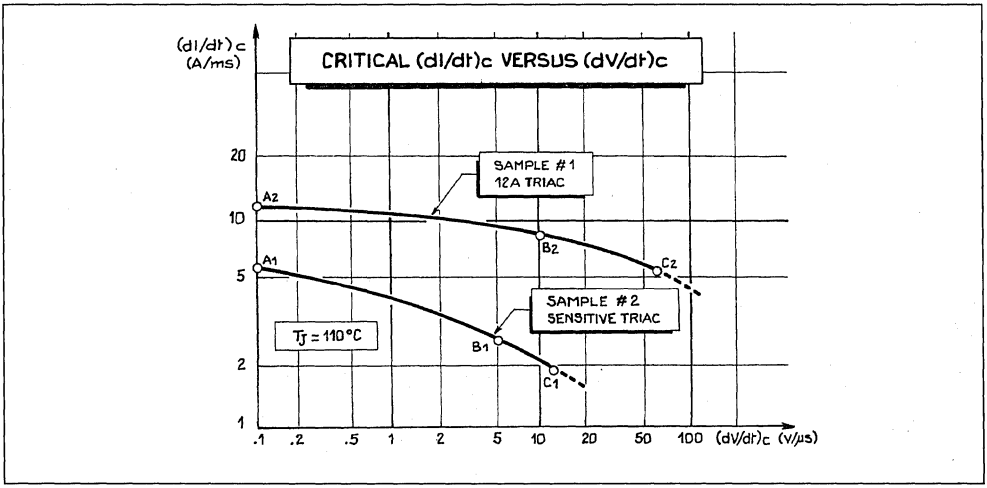
Figure 3 represents the results obtained with a standard 12 Amp triac (I_{GT} 50mA) and a sensitive gate, 6 Amp triac (I_{GT} 10mA). For standard triacs the critical (di/dt)c is sightly modified when we vary the (dv/dt)c. For sensitive gate triacs, this parameter noticeably decreases when the slope of the reapplied voltage is increased.

Figure 3 : Critical (di/dt)c versus (dv/dt)c (below the curve the triac turns on spontaneously.)

A1 and A2 : The rate of re-application of the off-state voltage of these points corresponds to the mains (sinusoidal wave form) at zero crossing.

B1 and B2 : The (dv/dt)c is limited by a snubber at the values generally specified in the data sheets (5V/µs or 10V/µs).

C1 and C2 : These points are obtained without snubber.



In practice, the current wave form, and thus the (di/dt)c, is imposed by the circuit. Generally we cannot change it.

So, in triacs applications it is always necessary to know the (di/dt)c of the circuit in order to choose a triac with a suitable critical (di/dt)c. This is the most important parameter.

Suppose a circuit in which the (di/dt)c reaches 15 A/ms. The triac N°1 characterized by the upper curve in figure 3 is not suitable in such a circuit even if the (dv/dt)c is reduced nearly to zero by connecting a huge snubber network across it.

APPLICATIONS IN BASIC CIRCUITS

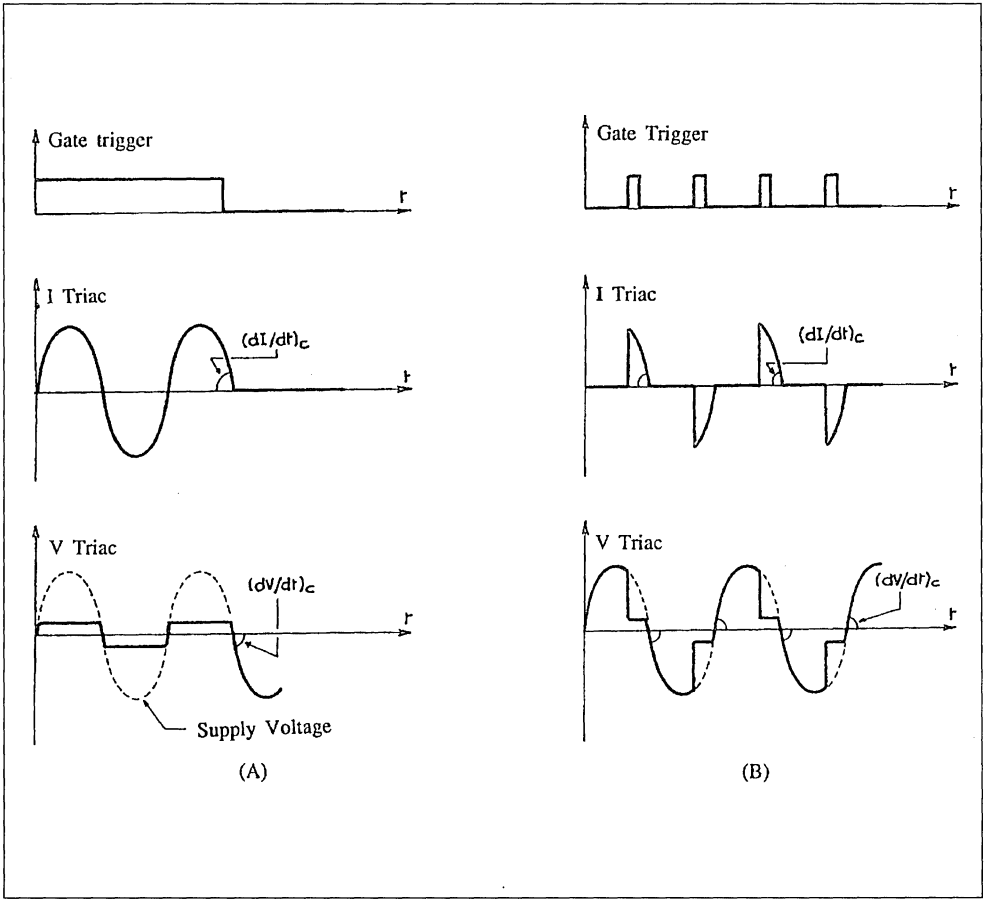
When considering the constraints in commutation at the turn off of a triac, we can distinguish two cases:

1/ The use of a triac on resistive load (fig. 4)

In this case the current and the voltage are in phase. When the triac switches off (i.e. when the current drops to zero), the supply voltage is nullified at this instant and will increase across the triac according to the sinusoidal law :

$$V = Vm \sin\omega t$$

Figure 4 : Current and voltage ware forms for resistive loads
(A) Case On / Off switching
(B) Case of phase control



Example :

For the European mains of Vrms = 220 volts at 50Hz, the slope will be:

$$(dv/dt)c = Vm \times \omega = Vrms \times \sqrt{2} \times \omega = 0.1 V/\mu S$$

This relatively low (dv/dt)c corresponds to points A1 and A2 on the curves in figure 3. As far as the (di/dt)c is concerned in the circuit, it depends on the load. For a resistance of loads R and under a Vrms voltage, we will have:

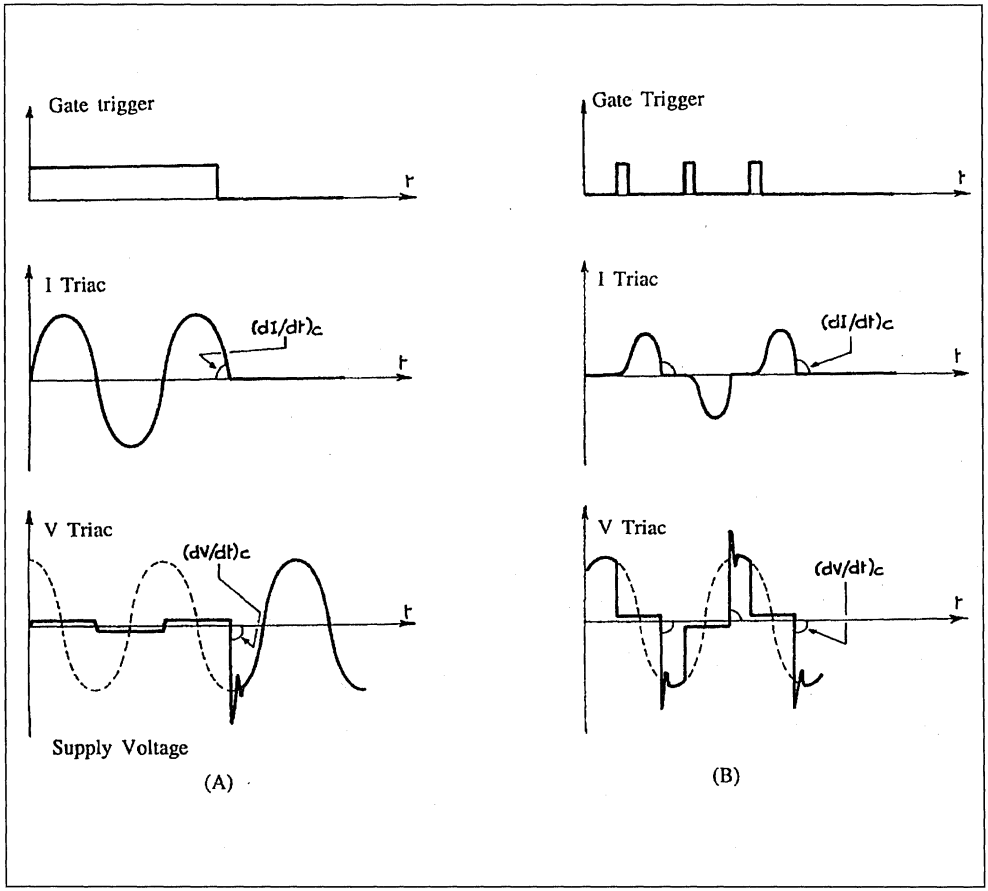
$$(di/dt)c = Im \times \omega = (Vrms \times \sqrt{2}/R) \times \omega$$

2/ The use of a triac on inductive load

In this case there is a phase lag between the current and the supply voltage (fig. 5).

When the currents drops to zero the triac turns off and the voltage is abruptly pushed to its terminals. To limit the speed of the increasing voltage, we generally use a resistive/capacitive network mounted in parallel with the triac. This "snubber" is calculated to limit the (dv/dt)c to 5 or 10 volts/µS according to the specified value in the data sheet. This case corresponds to points B1 and B2 in figure 3.The (di/dt)c is also determined in this case by load impedance (z) and the supply voltage.

Figure 5 : Current and voltage ware forms for inductance loads
(A) Case On / Off switching
(B) Case of phase control



THE USE OF A TRIAC WITHOUT A SNUBBER NETWORK

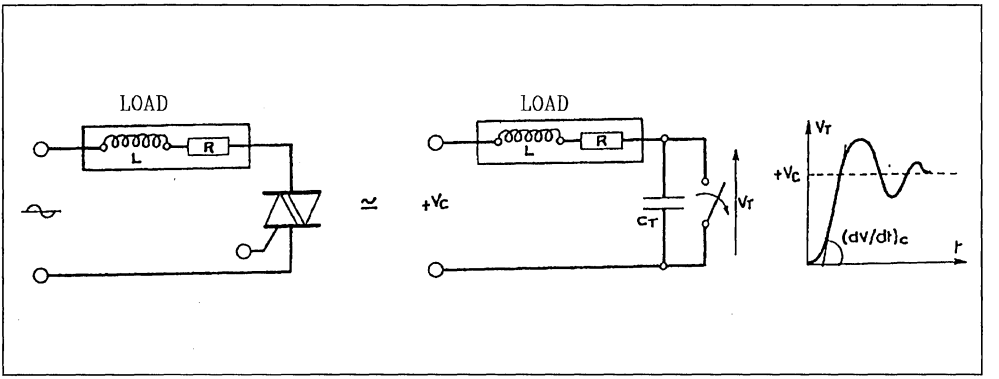
The triac can thus be considered as a switch which turns off at the moment when the current is cut off in the dampened oscillating circuit constituted by the loads L and R and the internal capacity of the triac Ct (fig. 6). In the case of a pure inductive load, the maximum reapplied (dv/dt) is:

$$(dv/dt)c = \sqrt{2}\, Vrms \times Irms \times \omega / Ct$$

For example, the internal capacitance of a 12 Amp triac is about 70pF. Therefore, on inductive load, the maximum (dv/dt)c without snubber will be limited to 50 or 100 V/S according to the characteristics of the load.

It is interesting to know the behavior of the triac, in particular the critical (di/dt)c value, in these conditions. This characterization corresponds to the points C1 and C2 of the curve fig 3.

Figure 6 : Triac commutation on an inductance load without a snubber network

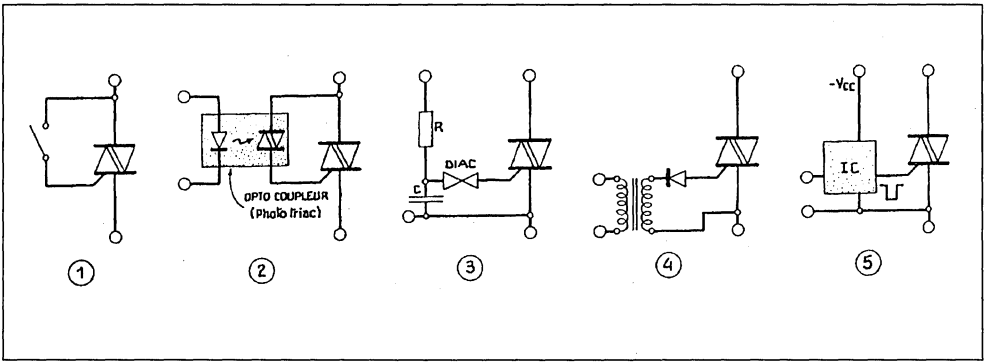


A progress: THE NEW TECHNOLOGY

To make significant progress in the triac area is to essentially improve the commutating behavior at the turn off of the triac. In other words the critical (di/dt)c has to be improved.

In order to reach this goal, a new structure has been developed. In this structure, the different active zones have been de-coupled to the maximum in such a way as to separate the elementary thyristors and the gate area. This is made possible by sacrificing the gate triggering in the fourth quadrant. In practice this does not pose a problem because the gate drive circuits of a triac generally use two of the third first quadrants. (fig. 7)

Figure 7 : Basic gale drive circuits (the fourth quadrant is not used)

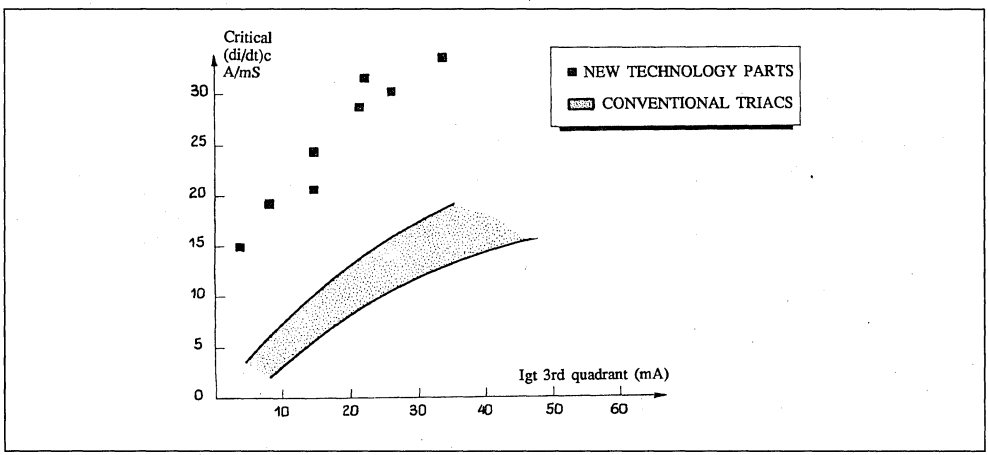


For a given technology, the commutating behavior of triacs depends on the sensitivity of the gate. The correlation between the critical (di/dt)c and the gate current for 12 Amp triacs is represented in figure 8.

In the same chart, we can see the results obtained with conventional triacs versus the new technology triacs. As can be seen, the progress that has been made at this level is significant.

1/ The performances and specifications

Figure 8 : Correlation between commutating behavior and sensitivity.
(Measurements performed on several lots of 12 A triacs)



The new technology has been put into place with the manufacturing of the two new series, Logic Level and SNUBBERLESS Triacs. In the data sheets of these new triacs a critical (di/dt)c limit is specified at the maximum junction temperature (Tj max).

a- Logic Level triacs

In this category we consider sensitive triacs in which the maximum gate current (I_{GT}) is 5mA for the TW type and 10mA for the SW one.

In the data sheets of the Logic Level triacs a minimum (di/dt)c is specified for the following cases:

* Resistive load with a (dv/dt)c of 01.V/µs.
* Inductive load with a (dv/dt)c of 20 V/µs

For example the 6 Amp triac is specified as follows:

Symbol	Test conditions		Quadrant		Suffix		Unit
					TW	SW	
tgt	$V_D = V_{DRM}$ I_G = 90 mA dI_G/dt = 0.8 A/ms	Tj = 25°C	I - II - III	TYP	2	2	µs
(dI/dt)c *	dV/dt = 0.1 V/µs	Tj = 110°C		MIN	3.5	4.5	A/ms
	dV/dt = 20 V/µs			MIN	1.8	3.5	

* For either polarity of electrode A_2 voltage with reference to electrode A_1.

b- SNUBBERLESS TRIACS

This series of triacs presently covers the range 6 to 25 Amps with gate currents of 35mA (CW type) and 50mA (BW type) according to the type required.This series has been specially designed so that the triacs switches from the on state to the off state without the use of an external snubber circuit.

Whatever the nature of the load, there is absolutely no risk of spurious firing at the turn off of the triac as long as it is functioning under the specified (di/dt)c value.

The SNUBBERLESS triacs are specified at critical (di/dt)c values which are greater than the decreasing slope of the nominal current in a sinusoidal configuration. For example, the slope of the current in a triac conducting 16 Amp when the current drops to zero is:

$$(di/dt)c = Irms \times \sqrt{2} \times \omega = 7A/mS \text{ at } 50Hz$$

The BTA/BTB16-600BW is specified at (di/dt)c = 14A/ms.

The following table summarizes the characteristics of the BW, CW SNUBBERLESS triacs which are presently available:

					WITHOUT SNUBBER
TYPE	CURRENT / VOLTAGE	SUFFIX	I_{GT} MAX (mA)	STATIC dV/dt MIN (V/µs)	(dI/dt)c MIN (A/ms)
BTA / BTB	06A 200 to 800V	BW	50	500	5
		CW	35	250	3.5
BTA / BTB	08A 200 to 800V	BW	50	500	7
		CW	35	250	4.5
BTA / BTB	10A 200 to 800V	BW	50	500	9
		CW	35	250	5.5
BTA / BTB	12A 200 to 800V	BW	50	500	12
		CW	35	250	6.5
BTA / BTB	16A 200 to 800V	BW	50	500	14
		CW	35	250	8.5
BTA / BTB	20A 200 to 800V	BW	50	500	18
		CW	35	250	11
BTB	24A 200 to 800V	BW	50	500	22
		CW	35	250	13
BTA	26A 200 to 800V	BW	50	500	22
		CW	35	250	13

2/ The advantages and Applications

a - Logic Level

The goal of these triacs is to be controlled directly by logic circuits and microcontrolers like the ST6 series:

Outputs of ST6 can sink currents up to 20mA per I/o line, and therefore drive TW and SW.

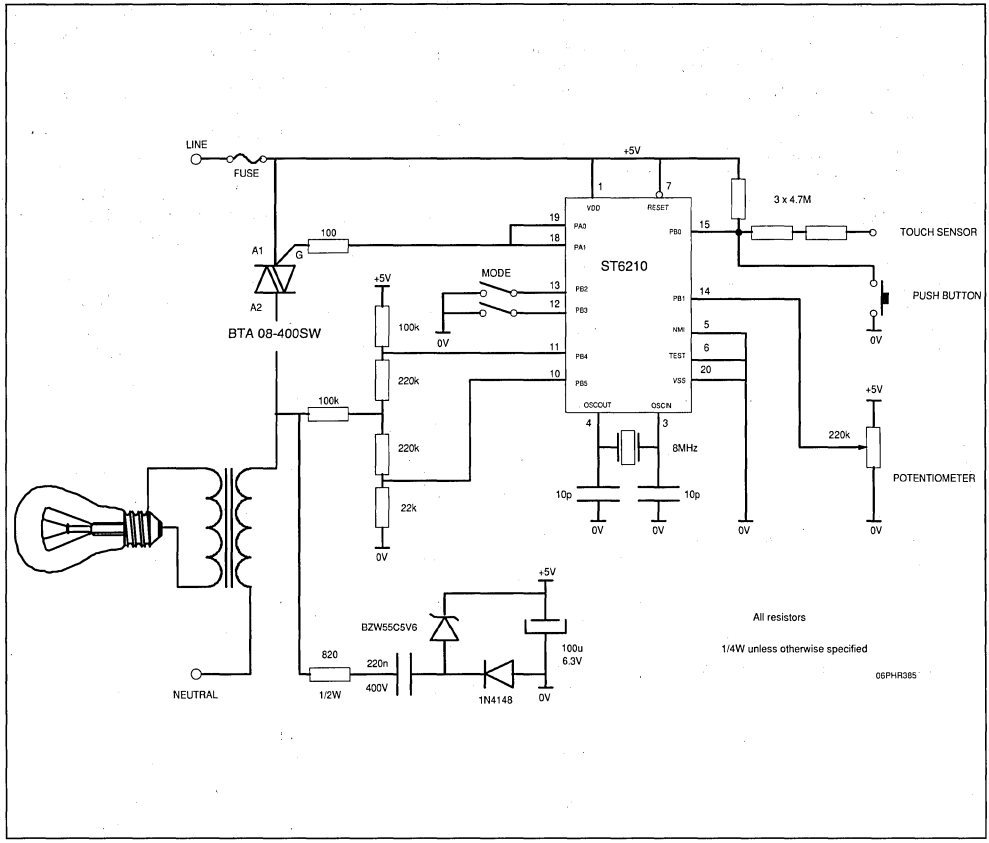
These triacs are ideal interface for power components supplied by 110 or 220 volts, such as valves, heating resistances, and small motors.

The specification of the critical (di/dt)c value on both resistive and inductive loads allows one

1/ to know the margin of security of the circuit in relation to the risk of the spurious firing, which results in improved reliability, and

2/ to optimize the performance of the triac to be used, which results in a cost reduction.

Figure 9 : Light dimmer circuit with ST6210.



b - SNUBBERLESS Triacs

The commutation of SNUBBERLESS triacs is specified without a limitation (dv/dt)c. With the suppression of the snubber in the circuit, there is a noticeable cost reduction.

Each SNUBBERLESS triac series is specified with a critical (di/dt)c value and the static (dv/dt) at the highest possible level, taking into consideration the gate sensitivity (Igt). The minimum specified levels for these two parameters allows the use of these products in circuits where there is a need for high safety factor, such as:

1. Static relays in which the load is not well defined. With conventional triacs it is difficult to adapt the snubber to all possible cases. SNUBBERLESS triacs resolve this problem. (fig. 10).

Figure 10 : Solid state relay diagram

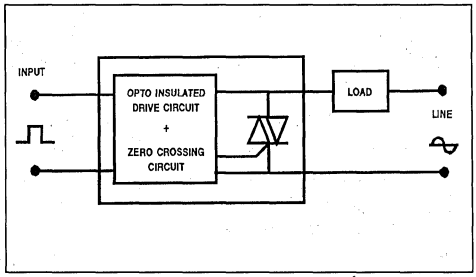
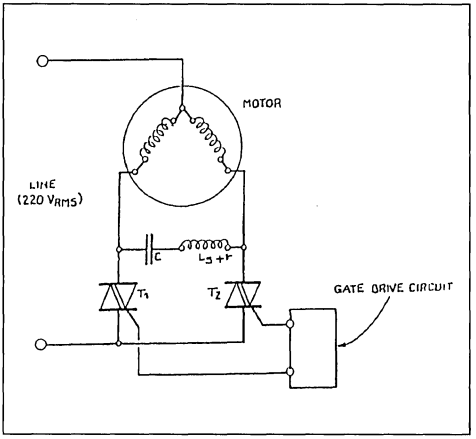


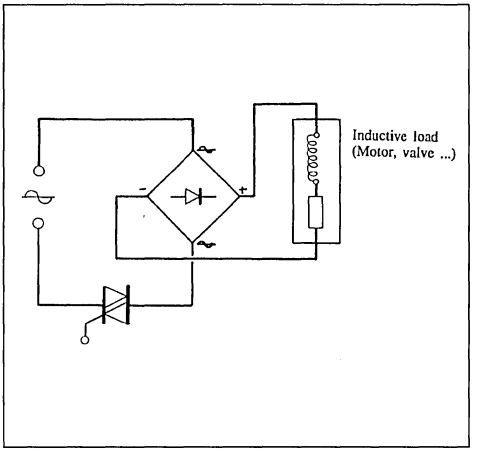
Figure 11 : Motor control circuit using SNUBBERLESS triacs
(Ls + r = network for series protection)



2. Motor drive circuits. Figure 11 shows an inversion circuit of an asynchronous motor where spurious firing of the triac, normally assumed to be in off- state, must be absolutely be avoided.

The critical (di/dt)c of SNUBBERLESS triacs is greater than the slope of the nominal current of the specific type under consideration. This is important for several applications, including : Circuits in which the (di/dt)c in a transient state is greater than in the steady state. This is the case for universal motors controlled by AC phase control circuit. The table in figure 12 shows how to the use of a SNUBBERLESS triac can optimize the efficiency of the circuit.

Figure 13 : Example of a circuit with high (di/dt)c



Circuits which generate wave forms with a very high (di/dt)c, such as inductive load supplied by a diode bridge (fig. 13). It is only limited by the parasitic inductance of the AC circuit.

Figure 12 : Universal motor control : Triac choise must comply with maximum (dI/dt)c For example, a SNUBBERLESS 10 A triac is sufficient to control a 110 V AC 600 W moytor

POWER	SUPPLY VOLTAGE	NOMINAL CURRENT	MAX CURRENT TO CONTROL	TRIAC RANGE	(dI/dt)c MAX (1)	STANDARDS TRIAC	SNUBBERLESS TRIAC
600 W	220V/50Hz	3 ARMS	3.5 A	6 A	A A/ms	BTA10-600B	BTA06-600BW
	110V/60Hz	6 ARMS	7 A	10 A	7 A/ms	BTA16-400B (2)	BTA10-400BW
1200 W	220V/50Hz	6 ARMS	7 A	10 A	7 A/ms	BTA16-600B	BTA10-600BW
	110V/60Hz	12 ARMS	14 A	16 A	15 A/ms	BTB24-400B	BTA20-600BW

(1) Maximum transient (dI/dt)c. This parameter depends very much on the type of the motor.
(2) This type specified at 7 A/ms munumum can be too small certain applications could need 25 A standard triac.

CONCLUSION

Thanks to the recent progress made in triac technology, the designer now has at disposal devices with a commutating behavior which is compatible with all applications in the 50 or 60Hz range. This includes phase control and static commutation for loads going from a few watts to several kilowatts.

The capability of this new generation of triacs allows :

1/ To increase the reliability of circuits, particularly where there is a risk of spontaneous firing even in the most difficult configurations.

2/ To reduce the cost by using sensitive gate, LOGIC LEVEL triacs without the need for an interface between the gate and the logic circuit, or utilizing SNUBBERLESS triacs which are specified without a resistive/capacitive network.

Additionally, the limit of the (di/dt)c parameter is now listed in SGS-Thomson Microelectronics data sheets.

This permits the optimization of the circuit by specifying stricter guidelines in the choice of the component.

TRIAC DRIVE CIRCUIT FOR OPERATION IN QUADRANTS I AND III

Ph. Rabier

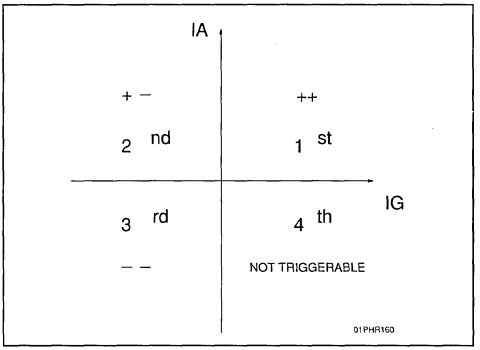
New triacs with high commutation and dv/dt performances are now available on the market.

Generally these triacs are only triggerable in the 3 first quadrants (case of SNUBBERLESS and LOGIC LEVEL triacs) as shown in figure 1.

This paper describes a trigger circuit supplying a negative gate current for quadrants II and III implemented in a system using a positive power supply.

Without a new design, just by adding a capacitor and a diode new W series triacs can replace conventional triac.

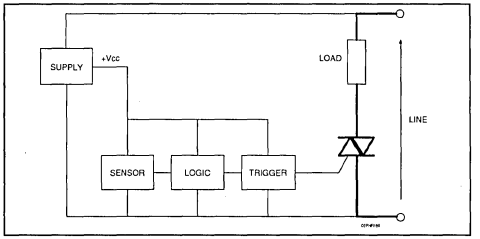
Figure 1 : The quadrants of a W series triac.



I - PRINCIPLE :

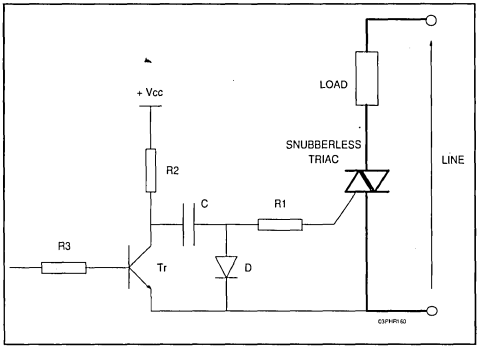
Figure 2 shows the schematic of a system with a sensor, logic and positive power supply (with respect to the anode 1 of the triac).

Figure 2 : Synoptical diagram of a classical system.



To drive the triac in the 2nd and 3rd quadrants a discharge capacitor is used as shown in figure 3.

Figure 3 : Basic diagram of the trigger.



1/ Principle :

- The transistor is switched off, capacitor C is charged through resistance R2 and diode D.

The diode is used to avoid a capacitor load current through the gate of the triac. A schottky diode could be used to improve the voltage drop level lower than the gate non trigger voltage (V_{GD}).

- When the triac is triggered, the transistor Tr is switched on, C is discharged through R1 and Tr and a negative current flows through the gate of the triac.

The capacitor C acts as a differentiation. We have to consider different parameters to define all the components :

- The gate trigger current of the triac (I_{GT})

- The time duration of the gate current

- The latching current (I_L) especially for small or inductive loads.

2/ Review :

Définition of the latching current (I_L) :

The I_L of a triac is the minimum value of the main current which allows the component to remain in the conducting state after the gate current I_G has been removed.

That is to say the gate current has to be higher than I_{GT} until the main current reaches the latcing current.

Example : for the CW SNUBBERLESS triac :
Q1 - Q3 : $I_L$max = 50 mA
Q2 : $I_L$max = 80 mA
With : gate pulse duration of 20µs at Tj = 25°C

I_L max is specified in the CW series triac data sheet.
Statistically, for BW series triacs we can use the K ratio

$K = I_L max / I_{GT} max$

K = 2,3

Two solutions are possible :

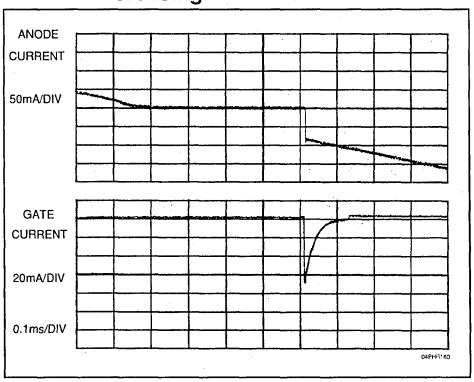
- Triggering with a delay after zero voltage crossing such that the main current is higher than I_L.

- Triggering at zero voltage crossing with a long discharge time in order to have no problem with I_L.

II - THE CASE WITH A RESISTIVE LOAD :

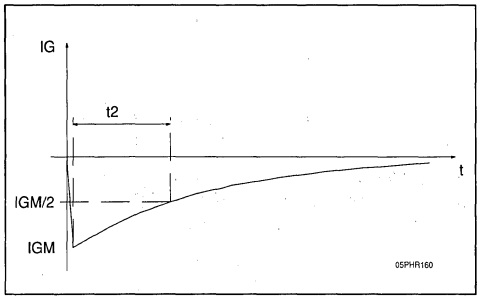
1/ First solution: delayed pulse current (figure 4).

Figure 4 : Triggering with delay t1 after zero crossing.



The gate pulse is shown in Figure 5 :

Figure 5 : Gate pulse.



t1 calculation :

The triac has to be triggered when the main current is higher than the latching current, that is to say t1min is :

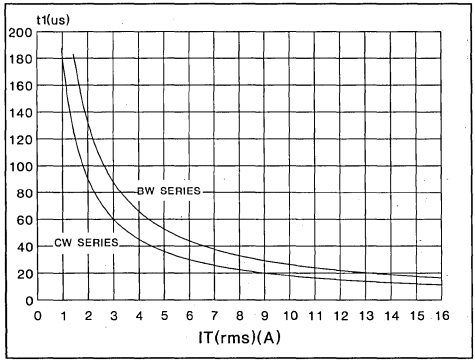
$$t1 = \frac{1}{\omega} arcsin\left(\frac{I_L \max}{I_{RMS}\sqrt{2}}\right)$$

where $\omega = 2 . \pi . f$

I_{RMS} : minimum RMS current in the worst case (depending on line and load dispersion).

The curve given shows the minimum time versus I_{RMS} current through the anode (figure 6).

Figure 6 : t1 time versus I_{RMS} for different latching currents.



The gate current calculation :

I_{GT} is the maximum gate trigger current specified in the data sheet. To ensure a good safety margin and good triggering we have chosen I_G = 2.I_{GT} with a pulse duration t2 higher than 20µs.

All the components can be defined by the following formulae :

R1max = (V_{CC} - V_{GK} - VCE)/(2.I_{GT})

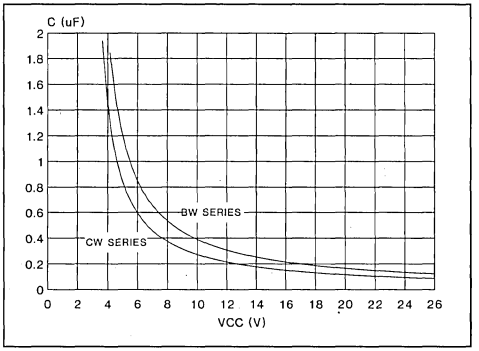
with V_{GK} = 2 V at I_G = 2.I_{GT}

Cmin = t2/(R1.log2) with t2 = 20µs

R2max = 0,001/C

Curve 7 gives the minimum capacitance versus supply voltage for different sensitivity.

Figure 7 : Capacitance value versus supply voltage for different sensitivity.



In this way the RMS current is lower than the full wave current, the RMS current/full wave current ratio is :

$$K^2 = 1 - 2 \cdot \frac{t1}{T} + \frac{1}{2\pi} \cdot sin\left(4\pi \frac{t1}{T}\right)$$

The calculation gives for a 6 Amps CW triac with a 2 Amps sine current and with an IL = 80 mA.

t1 = 90µs

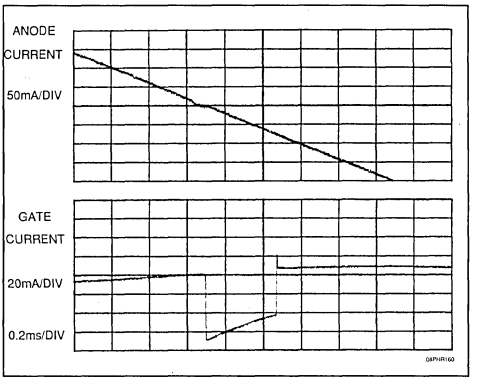
K = 0,99

That means the losses are lower than 1%.

2/ Second solution : Wide current pulse at zero crossing.

It consists of triggering the triac at zero voltage crossing voltage as shown in figure 8.

Figure 8 : Triggering at zero voltage.



Note : In figure 8, the pulse through the transistor base is cancelled before the capacitor is fully discharged to save energy.

All the components can be defined by the following formulae :

$$t2\ \min = \frac{1}{\omega} arcsin\left(\frac{I_L}{I_{RMS}\sqrt{2}}\right) + 20\mu s$$

R1max = (V_{CC}-V_{GK}-V_{CE})/(2.I_GT)

Cmin = t2/(R1.log2)

R2max = 0,001/C

In this way the RMS current is equal to the full wave current.

3/ Comparison between these two solutions :

The calculation of all the components is shown in the following table for 3 differents cases

Figure 9 : Component values for 3 differents cases : triac used : BTA08-600CW (I_{GT} = 35 mA)

	I_{RMS} = 5 A V_{CC} = 10 V		I_{RMS} = 2 A V_{CC} = 5 V		I_{RMS} = 5 A V_{CC} = 5 V	
	with delay	at zero crossing	with delay	at zero crossing	with delay	at zero crossing
t1 min (µs)	36	0	91	0	36	0
t2 min (µs)	20	56	20	111	20	56
R1 max (Ω)	105	105	34	34	34	34
C min (µF)	0.275	0.77	0.85	4.7	0.85	2.37
R2 max (Ω)	3.7	1.3	1.18	0.212	1.18	0.42

III - CASE OF INDUCTIVE LOAD :

With an inductive load another problem occurs : the problem of the phase lag between load current and load voltage.

It can be solved by taking into account :

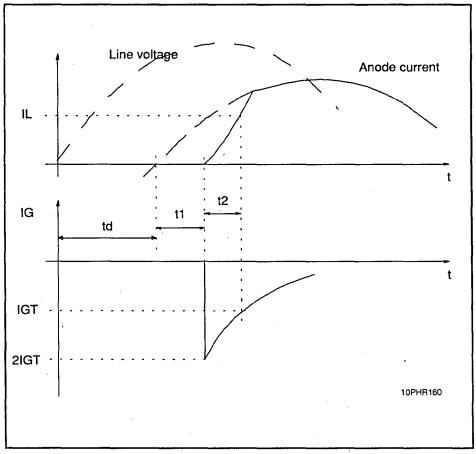
- the maximum phase lag to define a delay time td.

- the latching current to define the time t1

- the inductance to define the time t2= V/L at the moment when the triac is fired (t2 > 20µs) to have an anode current higher than the latching current I_L.

The figure 10 shows the anode current and the gate current in the triac, is the case of an inductive load.

Figure 10 : Current through an inductive load.



If the phase lag is not constant a gate pulse train can be used, the calculation parameters are the same, except for R2 : the capacitor C has to be charged between 2 pulses so the equation is :

R2=(time between 2 pulses)/(5xC)

IV - THE CASE OF A SMALL LOAD :

This trigger circuit can not be effectively used to drive small loads (like valves, fan etc...) because the latching current value is not very small compared to the load current. In this case a DC gate current is needed.

V - CONCLUSION :

In the case of controllers supplied by positive voltage this solution allows of the replacement of conventional triacs used in the 1st and 4th quadrants by SNUBBERLESS or LOGIC LEVEL triacs triggerable only in the 3 first quadrants without a new design but only by adding a capacitor and a diode.

Two configurations are possible :

First solution : Triggering after the zero voltage crossing.
Advantage : capacitor value lower than 1µF.
Disadvantage : the need to have a delay after the zero voltage crossing (delay system needed).

Second solution : Triggering at zero voltage crossing.
Advantage : 100% of the power used in the load.
Disadvantage : capacitor value of a few microfarads.

With inductive loads (motor, transformer, etc...) a pulse train can be used because of the phase lag between current and voltage.

With small loads (valve, fan,...) a DC gate current has to be used to drive the triac because of the latching current.

In case of logic or transistor failure, the capacitor C operates as an open circuit for DC current and avoids all triggering. This factor acts as a safety feature.

TRIACS FOR MICROWAVE OVEN

P. Rault

Triacs are now commonly used in microwave ovens as static switches to control the power transformer, the heating resistor for grill and sometimes the motor for plate rotation.

The conditions of operation of triacs for transformer control and for heater control are analysed here after in order to select the suitable device, to define the gate drive circuit and to implement an efficient protection.

I . POWER TRANSFORMER CONTROL :

The magnetron of a microwave oven is generally supplied by rectified high voltage obtained with a 50/60 Hz transformer. The power supplied to the oven is controlled by a triac in series with the primary (fig.1).

1/ Current stresses :

The power to be controlled is typically 1 to 2 KW and the nominal RMS current is in the range of 10 to 16 Amp according to the line voltage but it is necessary to take into account an overload due to the magnetizing current through the transfomer at turn on.
Due to the high turns ratio of this transformer this overcurrent can reach a peak up to 20 times the RMS current in steady state !
To reduce the stresses at every switching on the circuit and particularly on the triac it is important to limit the overcurrent by using a proper triggering synchronization.

Transient operation in inductive circuit with iron core :

During continuous operation, the magnetic field H, proportinal to the current in the coil,generates an induction B in the iron core with a delay as shown by the hysteresis cycle in figure 2A.

In transient operation, the induction can follow a different path and reach the saturation value BS for which the magnetic field H (according to the coil current) increases very rapidly (Fig.2B).

Figure 1 : Magnetron power supply controlled by a triac.

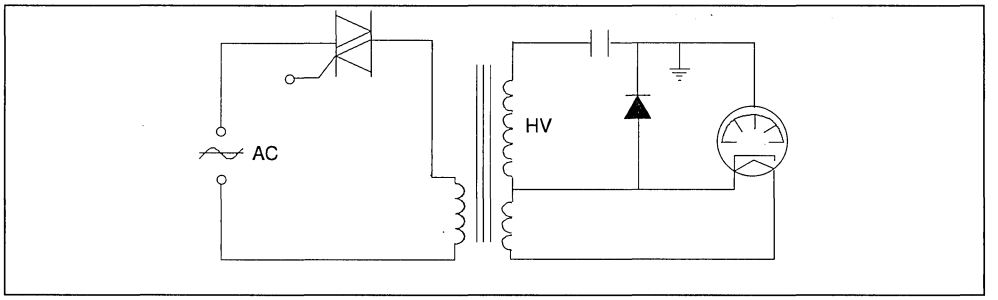
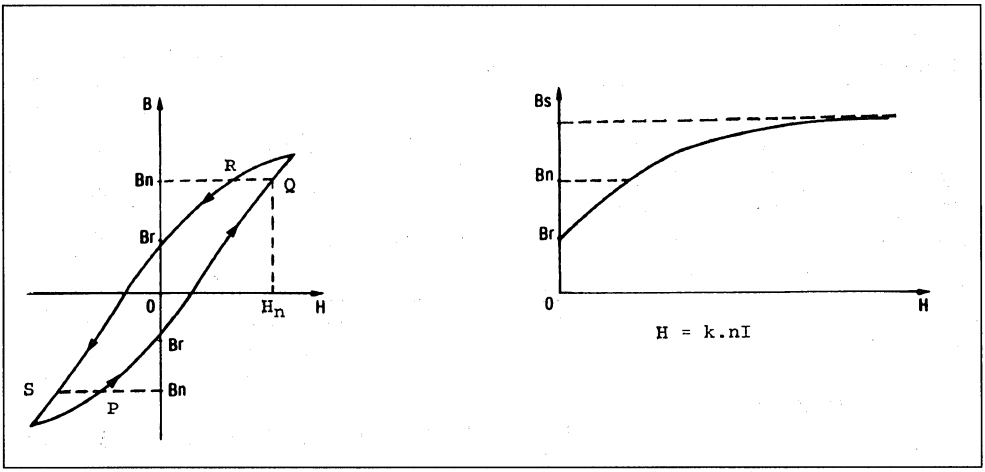


Figure 2 : A - Magnetic field H versus induction B (continous rating)
B - Saturation induction BS



In the circuits controlled by a triac, switching OFF occurs when the current is at zero. Thus the induction has a remanent value Br (positive or negative), corresponding to H = 0 (Fig.2A).

When the triac begins to conduct, the transient current depends on the instant of synchronization of the control signal with respect to the mains voltage.

FIRING AT ZERO MAINS VOLTAGE :

Peak induction tends to the value :

Bmax = 2 Bn + Br

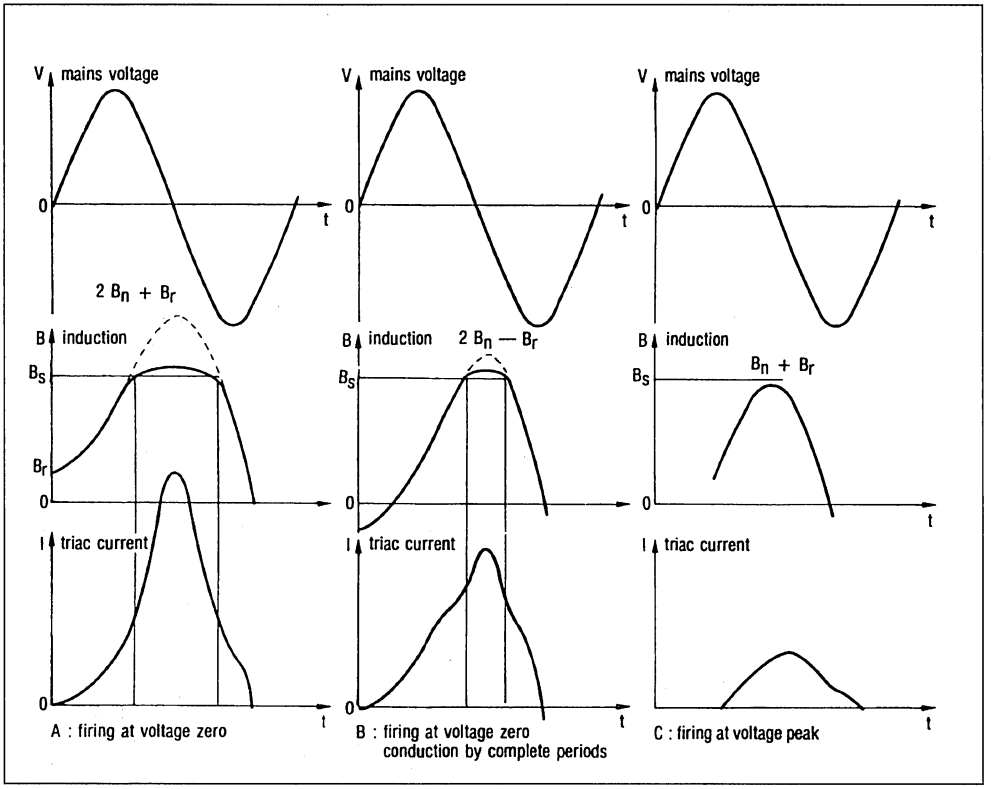
Thus in most cases B reaches the saturation induction BS. The amplitude of the current proportional to the magnetic field H becomes very high ; this type of control produces the highest transient overloads (Fig.3A).

In this case the transformer behaves like a short circuit and peak current is limited only by the series resistances of this circuit.
Nevertheless it is possible to reduce the overcurrent if control at zero voltages done by complete cycles i-e the polarity at the moment of firing is the reverse of that at moment the circuit is switched OFF.
Peak induction thus reaches the value :

Bmax = 2 Bn - Br.

The overload is lower than previously but still remains high (Fig.3B).

Figure 3 : Transient induction and current at beginning of conduction.

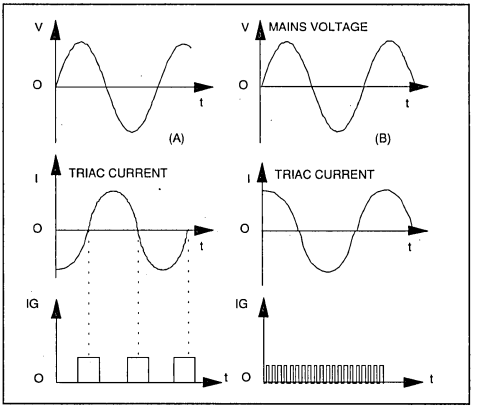


FIRING AT PEAK MAINS VOLTAGE :

In this case the peak induction takes the value : Bmax = Bn + Br
The level of saturation is not reached and amplitude of the current remains with in acceptable limits (Fig.3c).

→This type of synchronization must be used for transformer control.
See in appendix actual oscillogrammes of current through a transformer for different synchronization modes.

Figure 4 : A - gate control by single pulse synchronized with zero current
B - gate control by pulse train.



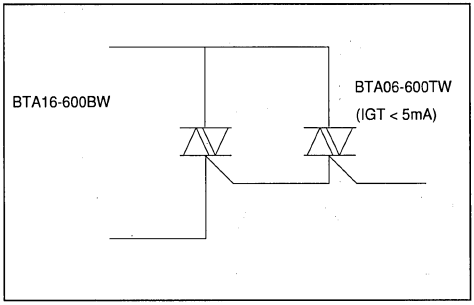
2/ Gate control :

After the first firing the gate pulse should be synchronized with the triac current zero point (Fig.4A).

The pulse duration must be sufficient to be sure the main current through the circuit reaches the triac latching current.(IL)
A pulse train can be used to avoid the problem of misfiring or wrong synchronization (Fig.4b).
A frequency of several,kilohertz garantees a correct operation.

Gate control by DC current is also an efficient method to keep the triac on in case of inductive load.
To reduce the consumtion of this kind of trigger circuit a sensitive triac can be used as a driver (Fig.5).

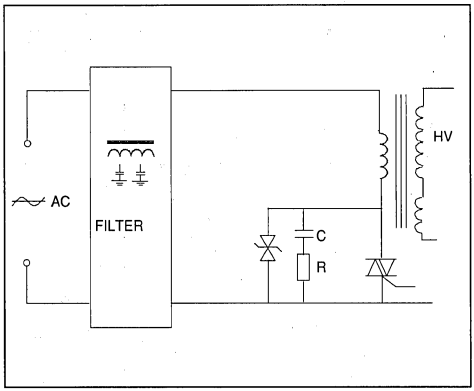
Figure 5 : Use of sensitive triac (5 mA) as driver to reduce gate control circuit consumtion.



3/ Protection :

It is important to avoid as much as possible all risk of misfiring of triac specially by overvoltage.
Transient voltages can be generated by internal mechanical switches used for security system (door, overbreak protection etc ....) or supperimposed to the line voltage. These last ones must be attenuated by a filter at the input.
An efficient protection at the triac level consists in use of TRANSIL diode across the triac to clamp the spikes higher than its voltage ratings (V_{DRM}) associed with our RC network to limit the off state dv/dt under the specified value . (Fig.6)

Figure 6 : TRANSIL diode and RC network are necessary to prevent spurious firing by overvoltages and/or dv/dt.



Nevertheless one accidental misfiring is always possible and in this case the triac must be able to hold the surge current. Therefore it is necessary to select a device with a sufficient ITSM (max peak current for 10 ms) for example 120 to 250 Amp.

4/ Prefered devices :

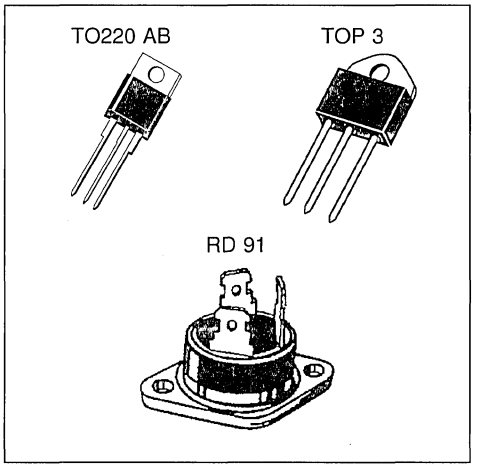
- Current ratings :
  The nominal RMS current through the circuit is not the main criteria but the surge current capability. We suggest the following current ranges.
  I_{TRMS} = 12 A with I_{TSM} = 120 A
  I_{TRMS} = 16 A with I_{TSM} = 160 A
  I_{TRMS} = 25 A with I_{TSM} = 250 A
- Voltage rating :
  V_{DRM} = 600 V provides a good safety margin for 220 VAC mains.
- Package :
  Insulated cases are generally used to make easier mounting on chassis and thus reduce the cost.
  TO220AB and TOP3 cases are suitable for printed board assembly. If the triac is mounted close of transformer (far from electronics board) RD92 with "FAST ON" connections is a convenient solution.
- Protection devices :
  A bidirectional silicon diode suppressor (TRANSIL) with a peak power capability of 1500 W (1 ms) is a good compromise if there is a filter (coil + capacitor) at the line input. In fact it is necessary to have a

current limitation (series indepance) in case of overvoltage.
The breakdown voltage compatible with 220 VAC supply is V_{BR} = 440 V.

– Part numbers :
triac
BTA12-600B/BW(1) 12 Amp TO220 AB
BTA16-600B/BW(1) 16 Amp TO220 AB
BTA26-600B/BW(1) 25 Amp TOP 3
BTA25-600B 25 Amp RD 91

TRANSIL 1.5KE440CP

Figure 7 : Triacs in insulated cases (UL approved)



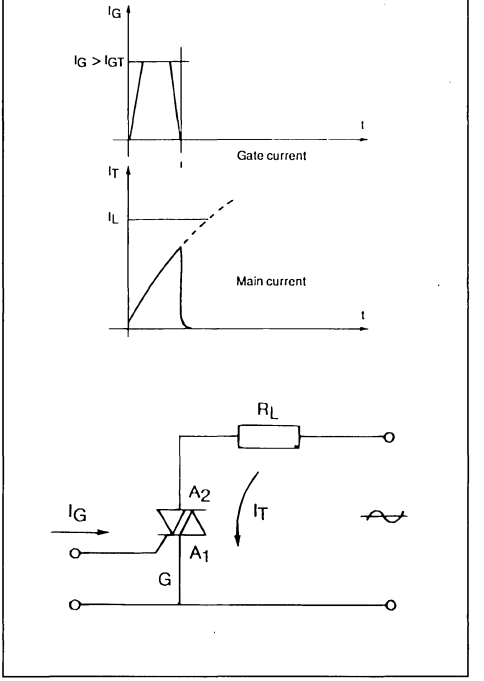
II . HEATING RESISTOR CONTROL :

1/ Triggering :

In this application the triac is used as a ON/OFF switch to control the power in the grill heater.
It is the case of resistive load. Therefore it is absolutely necessary to trigger the triac at zero voltage in order to eliminate the turn on di/dt stresses and RFI problems.
To keep the triac on, a single gate pulse can be supplied at every zero crossing of voltage that is also the zero point of current in this case.
The pulse duration must be calculated in order to allow the load current to reach the latching current (IL) of the triac.

(1) BW : SNUBBERLESS TRIAC series with high switching performance and high dv/dt capability.

Figure 8 : Controlled by the gate pulse, I_G, the triac is fired, and a current I_T flows through it. If the gate current I_G is stopped before current I_T reaches the value of the latching current I_L, the triac turns off.



For triacs with max gate triggering current of 50 mA the latching current is lower than 120 mA.

2/ Current rating :

For normal operation there is no particular current stresses efficient cooling is required to minimize the thermal fatigue due to the variation of junction temperature and consequently increase the life time of the equipment.

3/ Protection :

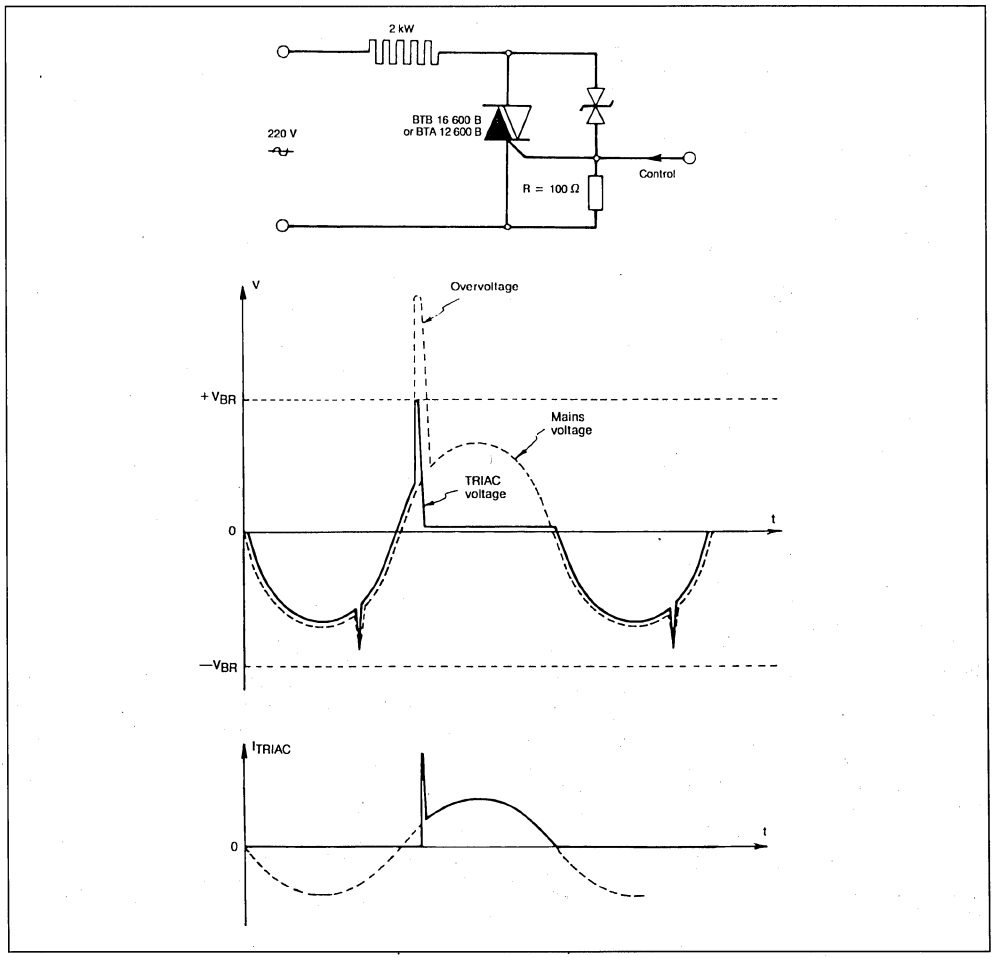
With the new generation of triacs, SNUBBERLESS triacs, the commutation (turn-off) is possible without external limitation of (dv/dt)c, that is to say without RC network even

if the load is inductive.
In case of overvoltages the triac could be fired by exceeding its breakover voltage and generally it is distroyed because of the too high di/dt, that is limited only by the inductance of the load (very low for a heating resistor) and of the wiring.
A RC network across the triac cannot reduce the spikes because there is not enough inductance in series in the kind of circuit.
→RC snubber circuit in useless !

HOW TO PROTECT ?

The solution consists in turning on the triac by a gate current as soon as the voltage across it exceeds a certain value which ensures a high level of safety.
To do it we use a low power (i-e low cost) bidirectional TRANSIL diode according to the diagram. Fig.8
When the overvoltage reaches the breakdown voltage VBR of the TRANSIL the latter conducts and the current flows through the gate and turns the triac on. Fig.7

Figure 9 : Protection by TRANSIL the triac is turned on by the gate at the beginning of the overvoltage and continues conducting during the rest of the half cycle.



What part number ?

to protect a 600 V triac generally used for 220 VAC operation we recommend : BZW04376B or BT.
for a 400 V triac (110 VAC mains) we propose a BZW04188B.

III . TO SUMMARIZE :

Transformer control :

Select triac with high surge current capability and with high transient immunity (SNUBBERLESS series).

Triggering :
first switching on, firing at peak line voltage to reduce peak inrush current, then triggering with pulse train synchronized at zero current point.

Protection :
TRANSIL and RC network across the triac to avoid all risk of firing by overvoltage and/or dv/dt.

Heating resistor control :

Triggering at zero voltage absolutely necessary.
Protection :

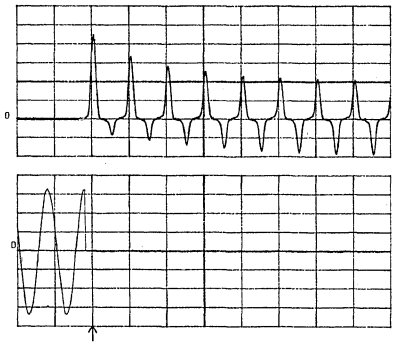
* with SNUBBERLESS triac, RC snubber circuit is useless.

* TRANSIL diode connected between gate and A2 achieves an efficient protection against overvoltages.

ANNEX

TRANFORMER CONTROL BY TRIAC

Triggering at voltage peak —-> peak current = 22 A



CURRENT

5 A / div
20 ms / div
(unloaded transformer)

TRIAC VOLTAGE

100 V / div
20 ms / div

Triggering at zero voltage —-> peak current reaches 130 A !

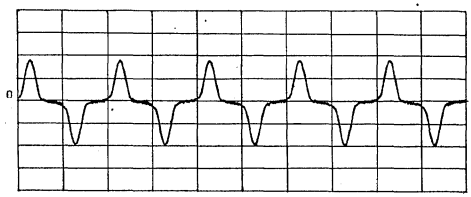
TRIAC VOLTAGE

100 V / div
20 ms / div
(line voltage = 220 VAC)

CURRENT

50 A / div
20 ms / div
(unloaded transformer)

Steady state (without load)



TRIAC CURRENT

50 A / div
10 ms / div

TRIAC & MICROCONTROLLERS : THE EASY CONNECTION

Ph. Rabier

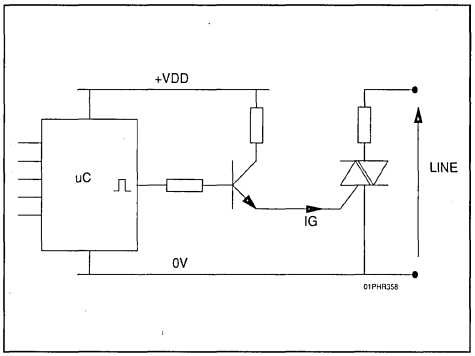
The aim of this note is to show how to connect an SGS-THOMSON triac and an SGS-THOMSON microcontroller.

I - CONVENTIONAL SOLUTION

For many years the triac has been used to switch load on the AC mains and thanks to the low cost of microcontrollers (µC) this solution is widely used in the appliance market.

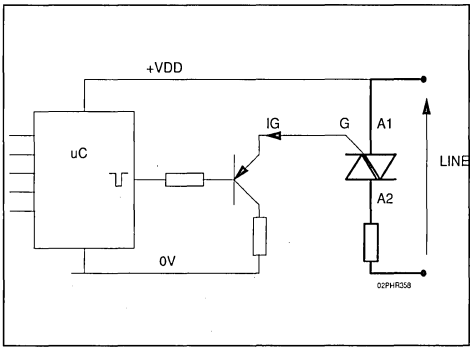
All the system use a buffer transistor between the output port of the microcontroller and the triac as shown in the figure 1.

Figure 1 : Drive in the 1st and 4th quadrants.



Because of the low sensivity of the triac in the 4th quadrant this type of drive is often unpractical, and is replaced by the topology of the figure 2 :

Figure 2 : Conventional drive in the 2nd and 3rd quadrants.



To save cost, manufacturers want to use fewer and fewer components and of course want to remove the buffer transistor, but a problem arises.

Due to the low output current of the microcontroller, the triac had to be very sensitive and consequently was not able to withstand for example the static dv/dt, and the commutation.

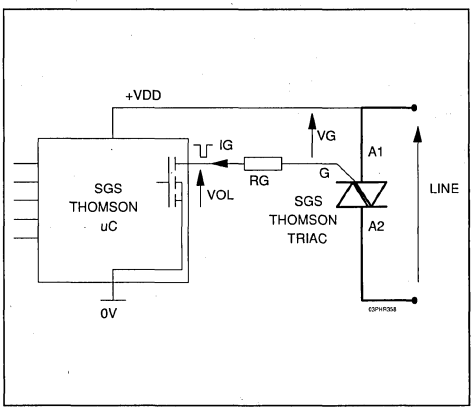
II - NEW SGS-THOMSON SOLUTION

Two parameters have been improved :

- The sensitivity of the triacs.
- The output capability of the microcontrollers in terms of sunk current.

A microcontroller is now able to drive one standard triac or several sensitive triacs, without buffer transistors (see figure 3).

Figure 3 : An easy connection



Where : V_{DD} supply voltagage
V_{OL} output low voltage of the microcontroller
V_G gate - anode 1 voltage at I_G

With : V_{DD} = +5 V
V_{OL} = 1.3 V
V_G = 1.5 V
I_G = 20 mA

Therefore : R_G = 110 Ohms

Figure 4 shows the output capability of a range of controllers and the sensitivity of the triacs.

Figure 4 : Triac and microcontroller characteristics.

MICROCONTROLLERS & OUTPUT CAPABILITIES	TRIAC	SENSITIVITY	GATE PARAMETERS	CONNECTION
ST621x SERIES ST622x SERIES IOL=20mA AT VOL=1.3V IVSS=100mA	T & TW SERIES Tx05 SERIES	IGT=5mA	VG =1.5V AT IG = 10mA	1 PORT/TRIAC
	S & SW SERIES Tx10 SERIES	IGT=10mA	VG =1.5V AT IG=20mA	1 PORT/TRIAC
	C SERIES	IGT=25mA	VG =1.5V AT IG =50mA	2 PORTS IN PARALLEL/TRIAC
	CW SERIES	IGT=35mA	VG = 2V AT IG =70mA	3 PORTS IN PARALLEL/TRIAC
	B & BW SERIES	IGT=50mA	VG = 2V AT IG= 100mA	4 PORTS IN PARALLEL/TRIAC

To take into account of the dispersion on R_G , V_{DD} and on the temperature variation, we generaly choose about:

$I_G = 2 . I_{GT}$ (I_{GT}=Specified gate trigger current)
tp > 20µs

Where tp is the pulse duration of gate current.

EXAMPLE :

For +5V supply voltage and a LOGIC LEVEL triac with I_{GT} = 10 mA, we have :

III - CONCLUSION

Use SGS-THOMSON sensitive triacs driven by an SGS-THOMSON microcontrollers and remove the buffer transistors.

This can be achieved thanks to the high current capability of our microcontrollers which are compatible with our new sensitive triacs (T410, T, TW, S, SW series).

Furthemore a non sensitive triac can be driven by several output ports in parallel.

SERIES OPERATION OF FAST RECTIFIERS

B. Rivet

The use of several rectifiers connected in series is necessary to obtain voltage ratings beyond the capabilities of single diodes and also when some special requirement, such as very low switching losses, oblige to implement several low voltage ultra fast diodes.

Rectifiers connected in series tend to share unequally the voltage across the string in blocking conditions because of the variations in reverse characteristics : leakage currents and turn off switching parameters.

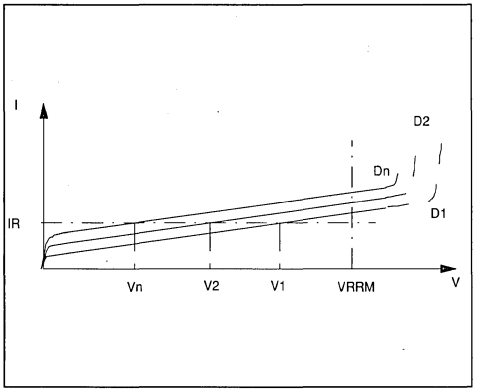
To ensure that each diode operates within its voltage rating it is generally necessary to add a voltage sharing network.

This paper gives the rules of calculation of this auxiliary network and shows how this circuit could be optimized : reduction of power dissipation and cost.

I - STEADY STATE VOLTAGE SHARING :

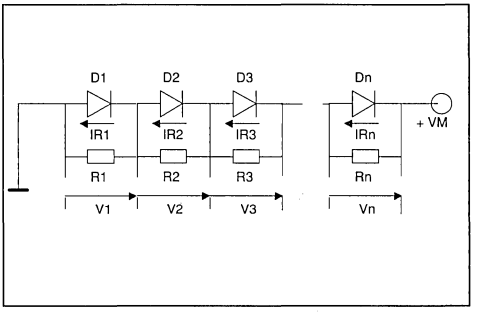
The difference in blocking characteristics results in unequal steady state voltage (fig.1).

Figure 1 : Dispersion of diodes reverse characteristics. The reverse current through the string D1, D2, ...Dn is I_R and the voltages across the diodes are respectively V1, V2; ...Vn.



In order to equlize the voltage, a resistor is connected across each diode (Fig.2).

Figure 2 : Use of shunt resistors for steady state voltage sharing.



1) Calculation of sharing resistors :

The calculation of these resistances is based on the worst case situation.

The maximum unbalance in blocking voltage when n diodes are connected in series occurs when (n-1) diodes have the maximum leakage current and one diode D1 has the lowest possible leakage current.

In this case D1 will support the highest voltage V1 and this tendency is aggravated by the assumption that the corresponding resistor R1 is at the upper limit of its tolerance (a), while all the others are at the lowest limit so,

$$R1 = R(1+a)$$

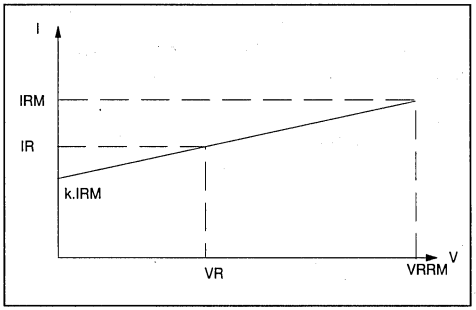
$$R2 = R3 = ... Rn = R$$

In order to calculate the current in the string we approximate the reverse characteristic with a straight line. We define the slope by the coefficient k according to fig.3.

Figure 3 : Reverse characteristic modelisation of a fast rectifier.

$$I_R + I_{RM}(Tj).[k+\frac{V_R(1-k)}{V_{RRM}}]$$

With k = 0.8



So the leakage current I_{RM} of diodes D2 ... Dn under the blocking voltage V2 ... Vn is :

$$I_{R2} = I_{R3} = ... I_{Rn} = I_{RM}[k+\frac{V_n(1-k)}{V_{RRM}}]$$

where IRM is the maximum leakage current at VRRM (maximum voltage specified for this diode), and at the operating junction temperature. For D1 the maximum reverse current at V_{RRM} is :

$$I_{RM} - \Delta I_R$$

In these conditions the leakage current of diode D1 is :

$$I_{R1} = (I_{RM} - \Delta I_R)(k+\frac{V_1(1-k)}{V_{RRM}})$$

Taking into account all these parameters, the voltage V1 across the diode D1 is given by the relation :

$$V_1 = \frac{V_M(1+a)(V_{RRM}+(1-k)I_{RM}R)+k(n-1)(1+a)\Delta I_R R V_{RRM}}{R I_{RM} n(1-k)(1+a)+V_{RRM}(n+a)-R\Delta I_R(1-k)(1+a)(n-1)} \quad (1)$$

The resistance R must be choosen to limit the voltage V1 under the maximum value V_{RRM} specified for this rectifier. Thus :

$$R < \frac{V_{RRM}(V_{RRM}(n+a)-V_M(1+a))}{\Delta I_R V_{RRM}(1+a)(n-1)-I_{RM}(1-k)(1+a)(nV_{RRM}-V_M)} \quad (2)$$

For the to-day fast rectifiers we can use k=0.8

2) I_{RM} evaluation

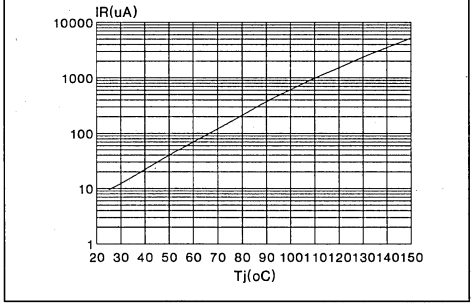
I_{RM} is the maximum leakage current at the maximum reverse voltage V_{RRM}. This current depends on the junction temperature (Fig.4).

Generally in the data sheet the manufacturer specifies a maximum value I_{RM} at V_{RRM} at Tj=100°C.

When we know the operating junction temperature (Tj) it is possible to calculate I_{RM} by using the following relation :

$$I_{RM}(Tj) = I_{RM}(100°C)\exp[-0.054(100-Tj)]$$

Figure 4 : Reverse leakage current versus junction temperature.
Example :
BYT 261-1000 (typical value)



3) Δ I_R estimation

In fact Δ I_R is the sum Δ I_{R1} and Δ I_{R2}

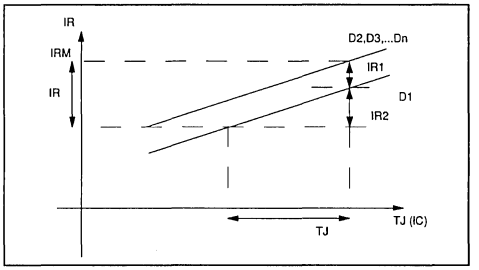
- Δ I_{R1} is due to the leakage current dispersion of the rectifiers in the same conditions of voltage and temperature.
For the fast rectifiers to day available on the market the dispersion of the reverse current at $V_R = V_{RRM}$ and Tj = 100°C is about :

$$\Delta I_{R1} = 0.6\ I_{RM}$$

This dispersion varies from one batch to another.

- Δ I_{R2} is due to the difference between the junction temperatures of each devie (ΔTj).

Figure 5 : The variation ΔI_R is the dispersion of I_R at max operation junction temperature (ΔI_{R1}) plus the variation due to Tj (ΔI_{R2})



The junction temperature is given by the thermal resistance junction to ambient Rth (j-a) and the power dissipation due to the conduction losses (PC) and the switching losses (PS).

PC is linked to the forward voltage (V_F) and PS is linked to the reverse recovery charge (Q_{RR}). So the variation of the junction temperature is :

$$\Delta Tj = \Delta Rth\,(PC+PS) + Rth\,(\frac{\Delta V_F}{V_F}PC + \frac{\Delta Q_{RR}}{Q_{RR}}PS)$$

Where ΔV_F is the dispersion of the forward voltage and Q_{RR} the dispersion of the reverse recovery charge.

For series operation, it is recommended to use pieces coming from the same lot, so the dispersion on the parameters V_F, Q_{RR} and Rth is minimized;

In most cases the evaluation of ΔTj is difficult but, from experience, it is generally lower than 10°C.

We propose to take a safety margin and to use :

$$\Delta I_R = 0.85\ I_{RM}$$

4) Simplified formula

The relation (2) is often used by using the following approximations

k = 1 : supposing the reverse current I_{RM} constant, whatever the blocking voltage across the diode.

a = 0 : Neglecting the effect of the tolerance of resistors. thus :

$$R < \frac{n\,V_{RRM} - V_M}{(n-1)\Delta\,I_R}$$

As for the ΔI_R the worst case is taken into account.

$\Delta I_R = I_R$ with $I_R = I_R$ max at Tj max specified (100°C)

$$R < \frac{n\,V_{RRM} - V_M}{(n-1)\,I_R}$$

This formula is "pessimistic" and induces a low resistance and then a high power dissipation.

5) Example

- Given
Maximum blocking voltage : V_M = 2500V
Part number used : BYT12-PI1000
Power dissipation per diode : P = 7W
Case temperature : Tcase = 52°C

- Rectifier specification :
V_{RRM} = 1000V
I_R (Max at Tj=100°C) = 2.5mA
Rth j-c = 4°C/W

- Problem :

Calculation of sharing resistors for 3 diodes in series.

- Solutions :

a) Simplified method :

$$R < \frac{n\,V_{RRM} - V_M}{(n-1)\,I_R}$$

With n = 3
V_{RRM} = 1000V
V_M = 2500V
I_R = 2.5mA
Thus Rmin = 100 kOhms

Power dissipation per resistor : 3.45 W ! (with duty cycle δ = .5)

b) Calculation with relation (2) :

$$R < \frac{V_{RRM}\,(V_{RRM}\,(n+a) - V_M\,(1+a))}{\Delta I_R\,V_{RRM}\,(1+a)(n-1) - I_{RM}\,(1-k)(1+a)(nV_{RRM} - V_M)}$$

General data for fast rectifiers :

$$\Delta I_R = 0.85\ I_{RM}$$
$$k = 0.8$$

Intermediate calculations :

$$Tj = P.Rth\ j\text{-}c + Tcase = 80°C$$

$$I_{RM} = I_{RM}(80°C) = I_{RM}(100°C)\ \exp[-0.0054(100-80)] = 0.85mA$$

$$\Delta I_{RM} = 0.72mA$$

Assuming we use resistors with 5% of tolerance, then a = .10
Let : Rmin = 220 kOhms

Power dissipation per resistor=1.58W(with δ=.5)

6) Question : is it possible to remove the sharing resistors ?

With the relation (1) we can find the value of V1 when the value of R tends to infinite. Then we calculate the condition to have

$$V1 < V_{RRM}$$

Solving we find

$$\frac{\Delta I_R}{I_{RM}} < \frac{(1-k)\,(n\,V_{RRM} - V_M)}{V_{RRM}\,(n-1)}$$

In the previous example this condition should be

$$\frac{\Delta I_R}{I_{RM}} = 5\%$$

If is obvious that this condition is generally very difficult to meet without hard selection.

II - TRANSIENT VOLTAGE SHARING

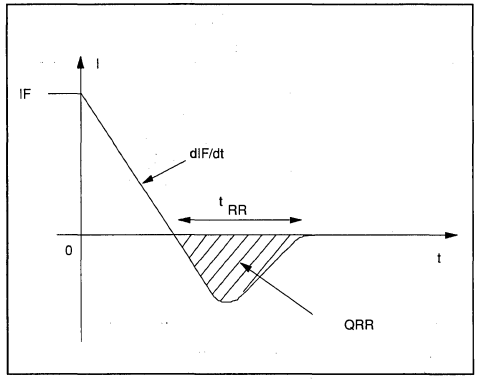
1) The problem

When a diode is switched from the forward conduction to the reverse blocking state, a reverse current flows through the device during the reverse recovery time trr.

After this delay all the charges (minority carriers) stored in the junction are eliminated and the diode turns off. The time integral of the reverse recovery current is called reverse recovery charge (Q_{RR}).

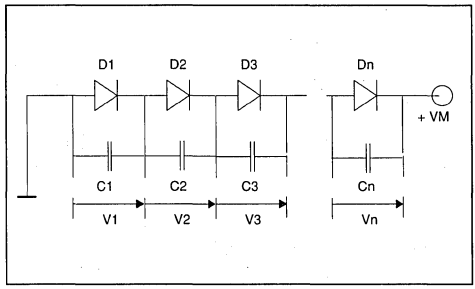
Fig.6 defines the reverse recovery parameters. When a string of n diodes in series switches off, the diode which has the lowest recovery charge turns off the first and supports an important proportion of the total voltage VM and its maximum reverse voltage V_{RRM} could be reached or exceeded.

Figure 6 : Reverse recovery current waveform.



Voltage sharing during the reverse recovery phase is achieved by using a shunt capacitors string connected across the diodes (Fig.7).

Figure 7 : Use of shunt capacitors for transient voltage sharing.



2) Calculation of sharing capacitors

The calculation of capacitance C is also based on the worst case situation.

We assume that (n-1) diodes D2, D3 ... Dn with a reverse recovery charge $Q_{RR} + \Delta Q_{RR}$, and one diode D1 with lowest value Q_{RR}.

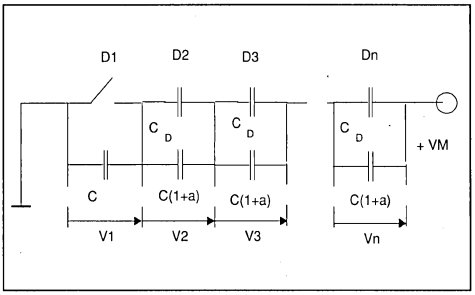
We suppose also that the corresponding capacitor C1 is at the lowest limit of tolerance (a) while the others are at the upper limit
so : C1 = C
C2 = C3 = ... = Cn = C(1+a)
When all the stored charges of diode D1 have been evacuated, the charge remaining in the other diodes is ΔQ_{RR}.
At this time the voltage across D1 is V1 and the voltage across the other diodes of the string is :

$$V_2 = V_3 = \ldots V_n = \frac{V_M - V_1}{(n-1)}$$

So these diodes can be assimilated to a capacitor

$$C_D = \frac{\Delta Q_{RR}}{V_n} = \frac{\Delta Q_{RR}\,(n-1)}{V_M - V_1}$$

Figure 8 : Equivalent diagram when D1 swtches off. Diodes D2, D3, ...Dn are equivalent to a capacitor CD = ΔQ_{RR}(n-1) / (VM-V1)



In these conditions the voltage across D1 is :

$$V_1 = \frac{\Delta Q_{RR}\,(n-1) + C\,V_M\,(1+a)}{C\,(n+a)}$$

In order to limit the voltage across D1 under the specified value V_{RRM} we calculate C by solving thus : $V1 < V_{RRM}$

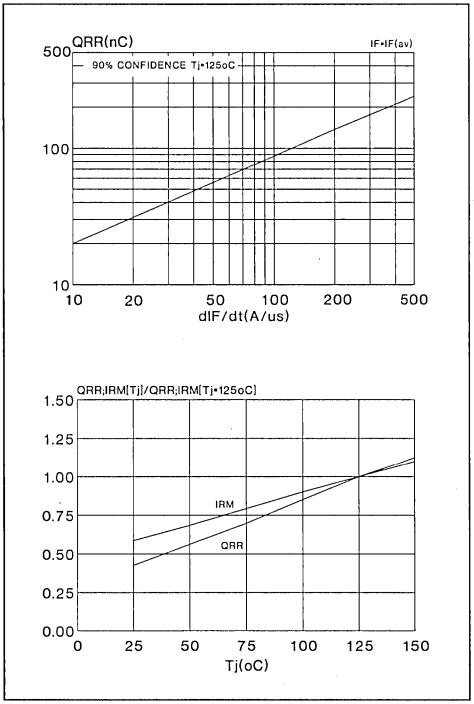
$$C > \frac{(n-1)\Delta Q_{RR}}{(n+a)V_{RRM} - V_M(1+a)}$$

3) Q_{RR} and ΔQ_{RR} consideration

For a given diode the reverse recovery charge QRR is function of the circuit commutation conditions such as the magnitude of forward current (I_F), the rate of decay of this current (dIF/dt) and the junction temperature.

Typical values of QRR are given in the data sheet of each part number (Fig.9).

Figure 9 : Example of reverse recovery charge specification. (case of BYW 51)



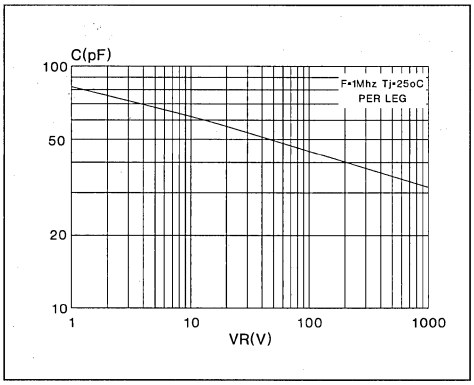
For fast rectifiers coming from the same lot the dispersion of this parameter is low and we can use, with a good safety margin :

$$\Delta Q_{RR} = .30\ Q_{RR}$$

4) Is it possible to remove the equalizing capacitor ?

In blocking state diodes have a junction capacitance. For a given diode this capacitance decreases with an increase in the applied reverse voltage according to Fig.10.

Figure 10 : Junction capacitance versus reverse voltage (example : BYT 261-1000)



When D1 has evacuated all its stored charge it is equivalent to a capacitor CJ1 and the other diodes D2, D3 ... Dn are equivalent to a capacitor which is the sum of the junction capacitance CJ2, CJ3 ... CJn and the capacitance

$$C_D = \frac{\Delta Q_{RR}\,(n-1)}{V_M - V_1}$$

Figure 11 : Equivalent diagram when D1 switches off in case of low QRR : The junction capacitances CJ1, CJ2; ....CJn, play the role of sharing capacitors.

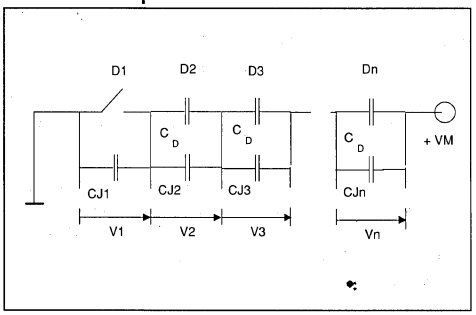


Fig.11 shows the equivalent circuit

In the worst case CJ1 is the junction capacitor of D1 at the maximum voltage V_{RRM}
Putting

$$CJ1 = CJ \text{ at } V_{RRM}$$

$$C_{J2} = C_{J3} \ldots C_{Jn} = C_J \text{ at } \frac{V_M - V_{RRM}}{n-1}$$

We have

$$V_1 = \frac{\Delta Q_{RR}\,(n-1) + V_M\,C_{Jn}}{C_{J1}\,(n+1) + C_{Jn}}$$

Auxiliary capacitors are not necessary if

$$V1 < V_{RRM}$$

$$\text{or} \quad \Delta Q_{RR} < \frac{V_{RRM}\,[C_{J1}\,(n-1) + C_{Jn}] - V_M\,C_{Jn}}{n-1}$$

Generally, the value of the junction capacitance at the operating voltage is very close to the value at V_{RRM} (CJ1) so we can write

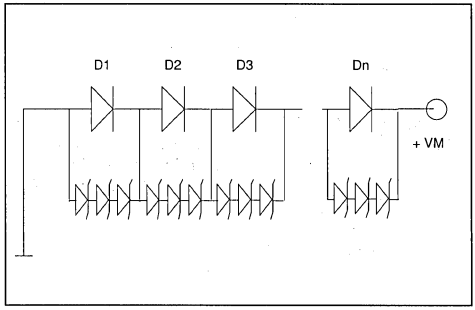
$$\Delta Q_{RR} < \frac{C_{J1}\,(n\,V_{RRM} - V_M)}{n-1}$$

This condition can be met by using very fast rectifiers in applications where the dIF/dt is low (like in some resonant converters or flyback converters) and consequently low Q_{RR}.

III - EQUALIZATION BY TRANSIL DIODES

TRANSIL are avalanche diodes designed for operation in breakdown characteristic and they are used as clamping device in a wide field of applications. To limit the voltage across the rectifiers of a string below the maximum value, TRANSIL diodes can be used according to diagram Fig.12.

Figure 12 : Voltage sharing by TRANSIL diodes.



TRANSIL operates as a voltage limiter at steady state, during the switching phase, and also in case of external voltage transients.

1) Steady state

In blocking condition the TRANSILS connected across the diode D1 (Which has the lowest reverse current) operate in the breakdown

characteristic. The current through these TRANSILS is I_R and the power dissipation is :

$$V_{BR}.\Delta I_R.\delta \quad (\delta = \text{duty cycle})$$

Where V_{BR} is the maximum breakdown voltage of TRANSILS. In general this extra power dissipation is lower than in the case of sharing by resistors and TRANSILS in axial packages can be used.

2) Switching phase

When the fastest diodes of the string switches off the TRANSILS across it operate in breakdown characteristic and the reverse recovery current of the other diodes flows through these TRANSILS. The charge remaining in the string at this moment is :

$$(n-1)\ \Delta Q_{RR}$$

and we can estimate the maximum energy in the TRANSILS with

$$E < 1/2(n-1)\ .\ \Delta Q_{RR}\ .\ V_{BR}$$

This relation does not take into account the losses due to the capacitive current through the string.

3) Example

GIVEN :
Use of a 3-BYT12-PI1000 for V_M = 2500V
Operating conditions :
T_j = 100°C
di/dt = 20A/µs
F = 25 kHz
δ= .5
RECTIFIER SPECIFICATION :
V_{RRM} = 1000V
I_{RM} at V_{RRM} = 2.5mA at T_j = 100°C
Q_{RR} = .5µC (in operating conditions)

PROBLEM :
3 TRANSILS diodes are connected in series across each rectifier. What is the suitable part number ?

DESIGN STEPS :

- V_{BR} calculation :

$$V_{BR}\,\text{min} > \frac{2500}{3x3} = 277V$$

$$V_{BR}\,\text{max} < \frac{1000}{3} = 333V$$

- Power dissipation in steady state :
$P1 < I_R\ .\ V_{BR}\ \text{max}\ .\delta$

with I_R = .85 x 2.5 ≈ 2mA
V_{BR}max = 330V
P1<330mW

- Power dissipation in switching phase :
$P2=E.F<1/2\ (n-1)\ Q_{RR}\ .\ V_{BR}\text{max}\ .\ F$
with ΔQ_{RR} = .5 x .3 = .15µC
F = 25 kHz and n = 3
then P2 < 1.2W

- Max total power dissipation P1 + P2 1.530 W

Solution : 1.5 KE series can be used (1.5KE300CP)

CONCLUSION

When using several fast rectifiers in series it is necessary to make sure that any diode will not be subjected to continuous or transient voltages in excess of their ratings.
In most cases, this is achieved by using sharing networks across each diode. It is important to optimize this circuit in order to reduce power consumption and to save space.
Parallel resistor can be optimized by using the modelisation of the fast recovery diodes reverse characteristic proposed in this paper. Then, thanks to a good knowledge of the reverse current and its variation in the operating conditions (possibly by measurement and selection) it is possible to implement a resistor with a value as high as possible.
Parallel capacitors also have to be reduced as much as possible with the knowledge the switching characteristics of the string in the actual conditions. The reverse recovery charge (Q_{RR}) is not always accessible with the datasheet and a measurement is often necessary.
In certain applications using ultra fast diodes of the same lot, where the Q_{RR}, and therefore the ΔQ_{RR} is very low, the sharing capacitor can be reduced to zero.
In systems where there is a risk of external overvoltages or where there are transient states not well known, TRANSIL diodes are a solution to the sharing voltage problem in sofar as the total power dissipation of the TRANSIL string remains compatible with the existing packages for these devices.

References :
1. B.M. BIRD and K.G. KING :
"An introduction to Power Electronics"
2. J.M. PETER - SGS-THOMSON
Microelectronics : "Analysis and optimisation of high frequency Power rectification"

TRANSISTOR PROTECTION BY TRANSIL : DISSIPATION POWER AND SURGE CURRENT DURATION

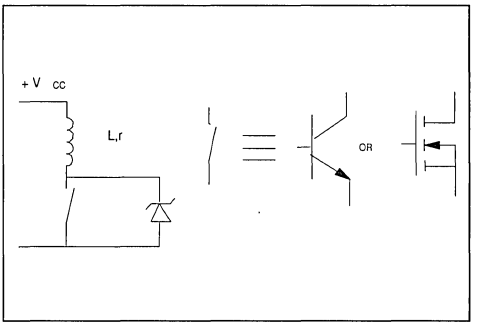
B. Rivet

I - INTRODUCTION

In a great number of applications, we find the diagram FIG.1 where a TRANSIL is used to protect a switch which controls an inductive load. The switch can be a bipolar or a MOS transistor.

The purpose of this paper is to calculate the dissipated power in the Transil and the pulse current duration.

Figure 1 : Basic Diagram

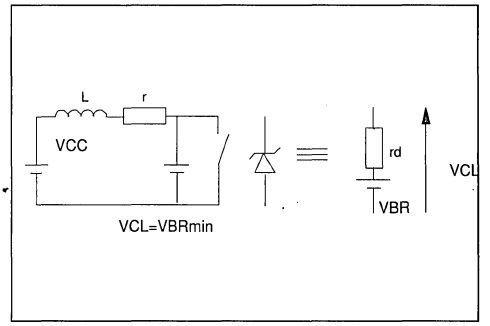


II - CIRCUIT MODELISATION

When the switch turns off we use the equivalent circuit represented FIG.2.

The worst case is to consider V_{CL} = V_{BR} min. This hypothesis will be used in all formulas.

Figure 2 : Equivalent Circuit



V_{CL} : clamping voltage
V_{BR} : breakdown voltage
rd : apparent resistance

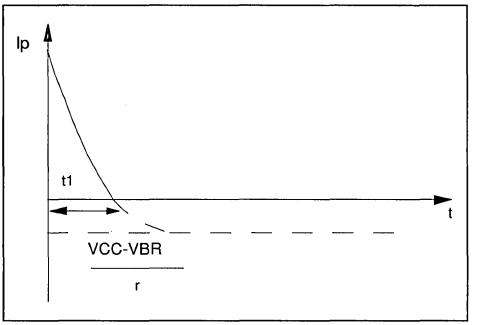
III - CURRENT IN THE TRANSIL

We can express the current i through the TRANSIL by the following formula :

$$i = (Ip + \frac{V_{BR}min - V_{CC}}{r}) exp\,(-r\frac{t}{L}) + (\frac{V_{BR}min - V_{CC}}{r})$$

Ip is the current through the coil when the transistor switches off. The FIG.3 shows the current variation versus time.

Figure 3 : Current Waveform



t1 can be calculated by

$$t1 = -\frac{L}{r} \ln (\frac{V_{BR}min - V_{CC}}{V_{BR}min - V_{CC} - rIp})$$

IV - TRANSIL POWER DISSIPATION

We can consider two cases, single pulse operation and repetitive pulses operation.

a) Single pulse operation

In this case, in order to define a TRANSIL we need peak power Pp and the pulse current standard duration tp.

Pp is given by

Pp = V_{BR} min x Ip

If we assimilate the pulse current with a triangle the standard exponential pulse duration tp is calculated by the formula :

$$tp = -\left(\frac{1,4L}{2r}\right) \ln \left(\frac{V_{BR}\text{min} - V_{CC}}{V_{BR}\text{min} - V_{CC} + rIp}\right)$$

The energy in the Transil can be expressed by :

$$W = \frac{V_{BR}\text{min}.L}{r}\left[Ip + \left(\frac{V_{BR}\text{min} - V_{CC}}{r}\right) ln\left(\frac{V_{BR}\text{min} - V_{CC}}{V_{BR}\text{min} - V_{CC} + rIp}\right)\right]$$

When r tends to zero we find :

$$W = \frac{1}{2} LIp^2 \left(\frac{V_{BR}\text{min}}{V_{BR}\text{min} - V_{CC}}\right)$$

b) Repetitive pulses operation

In repetitive pulse operation the power dissipation can be calculated by the following formula.

$$P = F \times \frac{V_{BR}\text{min}.L}{r}\left[Ip + \left(\frac{V_{BR}\text{min} - V_{CC}}{r}\right) ln\left(\frac{V_{BR}\text{min} - V_{CC}}{V_{BR}\text{min} - V_{CC} + rIp}\right)\right]$$

When r tends to zero we find :

$$P = \frac{1}{2} LFIp^2 \left(\frac{V_{BR}\text{min}}{V_{BR}\text{min} - V_{CC}}\right)$$

Where F is the commutation frequency.

V - EXAMPLE OF APPLICATION

Commutation of a coil supplied by a battery. The different parameters of the application are :

V_{CC} = 14V L = 10mH r = 3 0hms Ip = 4A

TRANSIL : 1.5KE36P V_{BR}min = 34.2V (cf data sheet)

a) Single pulse

We find

Pp = 34.2 x 4 = 136.8W

$$tp = -\left(\frac{-1.4.10.10^{-3}}{2x3}\right) \ln \left(\frac{34.2-14}{34.2-14+3x4}\right)$$

tp = 1.08ms

The data sheet gives Pp 1500W for tp = 1.08ms then this 1.5KE36P can be used in this application.

b) Repetitive pulse operation

The commutation frequency is equal to 10HZ so

$$P = 10x\left(\frac{34.2x10.10^{-3}}{3}\right)\left[4+\left(\frac{34.2-14}{3}\right) \ln \left(\frac{34.2-14}{34.2-14+3x4}\right)\right]$$

= 980mW

Rth = 75°C/W and Tj max. = 175°C

So Tj = P x Rth + Tamb.max.

With Tamb.max. = 50°C we find :

Tj = 0.98 x 75 + 50 = 123.5°C < Tj max

So we can also use this Transil in repetitive pulse operation.

MONITOR & TV CIRCUITS

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

VERTICAL DEFLECTION CIRCUITS FOR TV & MONITOR

by Alessandro MESSI

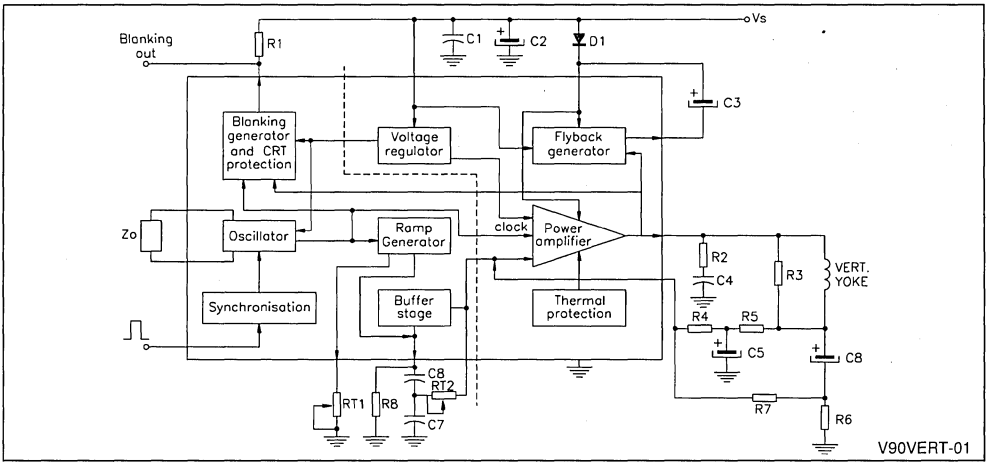
INDEX

1. INTRODUCTION

In a general way we can define vertical stages circuits able to deliver a current ramp suitable to drive the vertical deflection yoke.

In Figure 1 is represented the more general possible block diagram of a device performing the vertical deflection.

Figure 1 : Block Diagram of a General Deflection Stage.

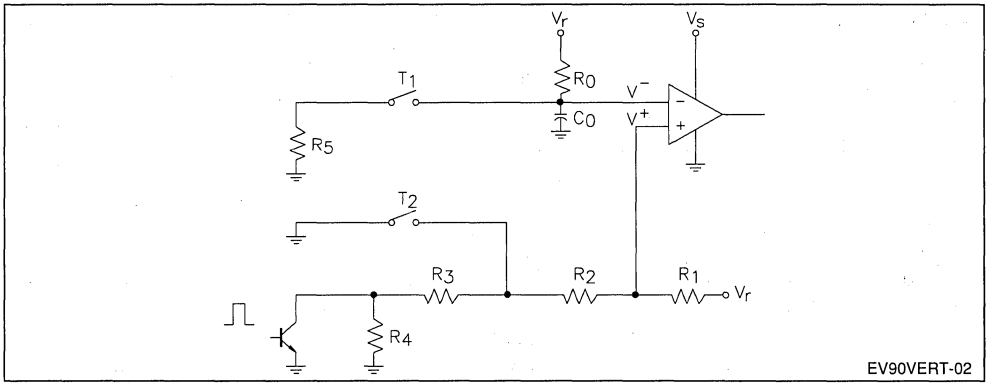


Such a device will be called "complete vertical stage" because it can be simply driven by a synchronization pulse and it comprises all the circuitry necessary to perform the vertical deflection that is : oscillator, voltage ramp generator, blanking genetor, output power and flyback generator.
At the right side of the dotted line in Figure 1 is represented the circuitry characterizing a "vertical output stage". This kind of device comprises only the power stages and it has to be driven by a voltage sawtooth generated by a previous circuit (for example a horizontal and vertical synchronization stage.
In the first class there are the following devices : TDA1170D, TDA1170N, TDA1170S, TDA1175, TDA1670A, TDA1675, TDA1770A, TDA1872A, TDA8176.
In the second class there are : TDA2170, TDA2270, TDA8170, TDA8172, TDA8173, TDA8175, TDA8178, TDA8179.
There is also a third class of vertical stages comprising the voltage ramp generator but without the oscillator; these circuits must be driven by an already synchronized pulse. In this third class there are : TDA1771 and TDA8174.

2. OSCILLATOR

There are two different kinds of oscillator stages used in SGS-THOMSON complete vertical deflections, one is used in TDA1170D, TDA1170N, TDA1170S, TDA1175 and TDA8176, the other in TDA1670A, TDA1675, TDA1170A and TDA1872A.
The principle of the first kind of oscillator is represented in Figure 2.
The following explanations will be the more general possible; we shall inform the reader when we refer to a particular device.

Figure 2 : First Kind of Oscillator Stage.

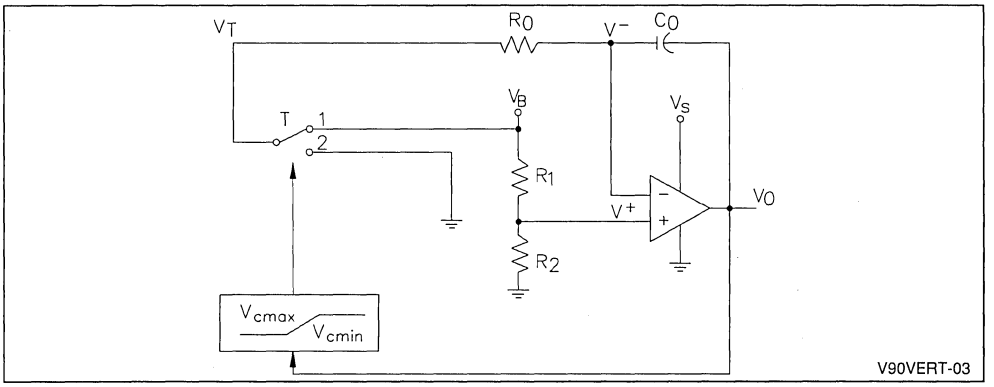


When the switches T_1 and T_2 are opened the C_O capacitor charges exponentially through R_O to the value $V^+_{(MAX)}$ determined by the integrated resistors R_1, R_2, R_3 and R_4. At this point the switches are closed, short-circuiting R_3 and R_4, so the voltage at the non-inverting input becomes $V^+_{(MIN)}$. The capacitor C_O discharges to this value through the integrated resistor R_5.
The free running frequency can be easily calculated resulting in :

$$T_O = R_O \cdot C_O \cdot \log \frac{V_R - V^+_{(MIN)}}{V_R - V^+_{(MAX)}} + R_5 \cdot C_O \cdot \log \frac{V^+_{(MAX)}}{V^+_{(MIN)}} \qquad (1) \qquad f_O = \frac{1}{T_O}$$

with R_O = 360 kΩ and C_O = 100 nF, it results in 43.7 Hz.
The oscillator synchronization is obtained reducing the superior threshold $V^+_{(MAX)}$ short-circuiting the R_4 resistor when a vertical synchronization pulse occurs.
The second kind of oscillator is represented in Figure 3.

Figure 3 : Second Kind of Oscillator Stage.



When the switch T is in position 2, a constant current $I_{CO} = V^- / R_O$ flows through C_O charging it with a voltage ramp. When the voltage V_O reaches $V_{O(MAX)}$, T passes in position 1, so a constant current $I_{CO} = (V_B - V^-) / R_O$ discharges the capacitor causing the inversion of the voltage ramp slope at the output V_O (t). The discharges stops when V_O reaches the value $V_{O(MIN)}$ and the cycle takes place again.

It is possible to calculate the free running frequency f_O with the following formula :

$$T_O = \frac{(V_{O(MAX)} - V_{O(MIN)}) \cdot R_O \cdot C_O}{V^-} + \frac{(V_{O(MAX)} - V_{O(MIN)}) \cdot R_O \cdot C_O}{V_B - V^-} \qquad (2)$$

with $V_{O(MAX)} - V_{O(MIN)} = 3.9V$, $V_B = 6.5V$, $V^- = 0.445V$, $R_O = 7.5k\Omega$ and $C_O = 330nF$ it results in : $f_O = 43.8Hz$.

The oscillator synchronization is still obtained in the above mentioned way.

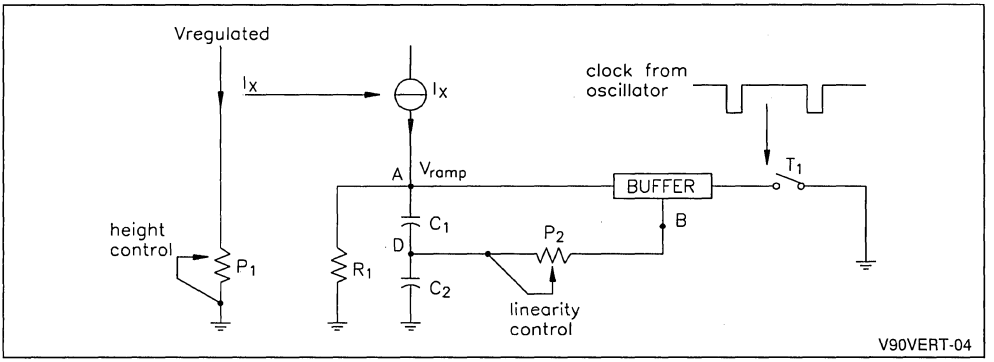
In order to guarantee a minimum pull-in range of 14Hz the threshold value has been chosen in $V_P = 4.3V$.

The spread of the free running frequency in this kind of oscillator is very low because it mainly depends from the threshold values $V_{O(MAX)}$, $V_{O(MIN)}$ and V^- that are determined by resistor rates that can be done very precise.

3. RAMP GENERATOR

The ramp generator is conceptually represented in Figure 4.

Figure 4 : Ramp Generator.



The Voltage ramp is obtained charging the group R_1, C_1 and C_2 with a constant current I_X.

It is easy to calculate the voltage V_{RAMP} That results in :

$$V_{RAMP}(t) = (V_{(MIN)} - R_1 \cdot I_X)\ e^{-\frac{t}{R_1 \cdot C}} + R_1 \cdot I_X \qquad (3)$$

where $V_{(MIN)}$ is the voltage in A when the charge starts and C is the series of C_1 and C_2.
The resistor R_1 is necessary to give a "C correction" to the voltage ramp. The ramp amplitude is determined by $I_X = V_{REG} / P_1$,so the potentiometer P_1 is necessary to perform the height control.
The voltage ramp is then transferred on a low impedence in B through a buffer stage.
Te P2 potentiometer connected between D and B performs the ramp linearity control or "S correction" that is necessary to have a correct reproduction of the images on the TV set.
The voltage ramp in B grows up until the switch T_1 is closed by a clock pulse coming from the oscillator; in this way the capacitors discharge fastly to $V_{(MIN)}$ that is dependent upon the saturation voltage of the transistor that realizes the switch.
At this point the exponential charge takes place again.

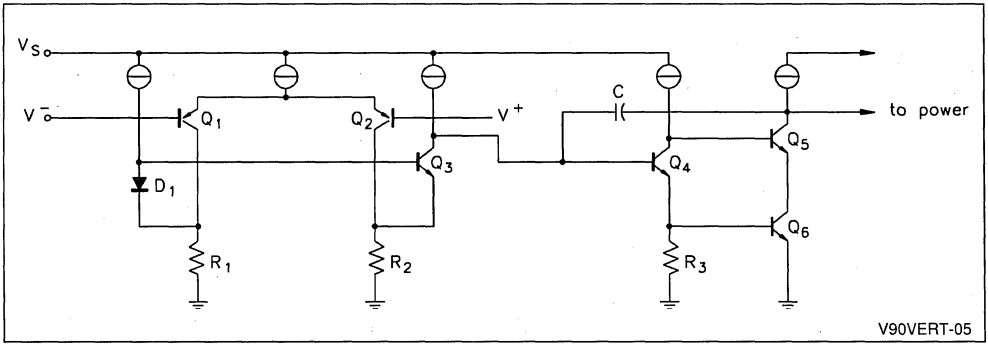
4. BLANKING GENERATOR AND CRT PROTECTION

This circuit senses the presence of the clock pulse coming from the oscillator stage and the flyback pulse on the yoke. If both of them are present a blanking pulse is generated able to blank the CRT during the retrace period. The duration of this pulse is the same of the one coming from the oscillator.
If for any reason the vertical deflection would fail, for instance for a short circuit or an open circuit of the yoke, the absence of the flyback pulse puts the circuit in such a condition that a continuous vertical blanking is generated in order to protect the CRT against eventual damages.
This circuit is available only in the following devices : TDA1670A, TDA1675, TDA1770A and TDA1872A.
The stages we will consider starting from this point are common both to complete vertical stages and vertical output stages.

5. POWER AMPLIFIER STAGE

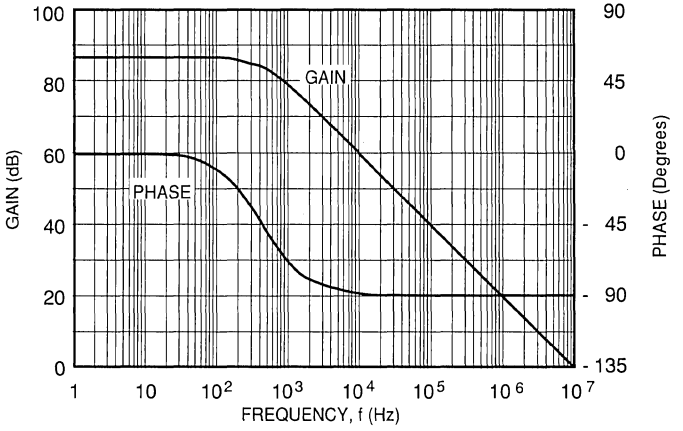
This stage can be divided into two distinct parts : the amplifier circuit and the output power.
The amplifier is realized with a differential circuit; a schematic diagram is represented in Figure 5.

Figure 5 : Amplifier Stage.



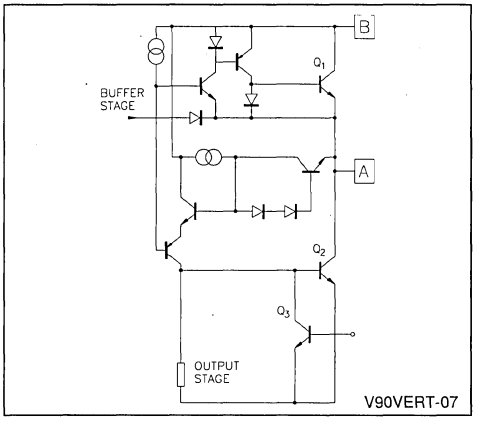
The open-loop gain of the circuit is variable from 60dB to 90dB for the different integrated circuits.
The compensation capacitor C determines the dominant pole of the amplifier. In order to obtain a dominant pole in the range of 400Hz, the capacitor must be of about 10pF.
As an example in Figure 6 is represented the boole diagram of the amplifier open loop gain for TDA8172.

Figure 6 : Amplifier Open Loop Gain and Phase.



The output power stage is designed in order to deliver to the yoke a vertical deflection current from 1 to 2 Apeak, depending upon the different devices, and able to support flyback voltages up to 60V. A typical output stage is depicted in Figure 7.

Figure 7 : Power Stage.



The upper power transistor Q_1 conducts during the first part of the scanning period when the vertical deflection current is flowing from the supply voltage into the yoke; when the current becomes negative, that is it comes out of the yoke, it flows through the lower power transistor Q_2.The circuit connected between the two output transistors is necessary to avoid distortion of the current at the crossing of zero, when Q_1 is turned off and Q_2 is turned on. When the flyback begins, Q_2 is switched-off by Q_3 in order to make it able to support the high voltage of the flyback pulse.
The circuit behaviour during flyback is explained in chapter 7.

6. THERMAL PROTECTION

The thermal protection is available in all the devices except the TDA1170 family and the TDA8176.
This circuit is usefull to avoid damages at the integrated circuit due to a too high junction temperature caused by an incorrect working condition.
It is possible to sense the silicon temperature because the transistor V_{BE} varies of - 2 mV/ °C, so a temperature variation can be reconducted to a voltage variation.
If the temperature increases and it is reaching 150°C, the integrated circuit output is shut down by putting off the current sources of the power stage.

7. FLYBACK BEHAVIOUR

In order to obtain sufficiently short flyback times, a voltage greather than the scanning voltage must be applied to the deflection yoke.
By using a flyback generator, the yoke is only supplied with a voltage close to double the supply during flyback.
Thus, the power dissipated is reduced to approximately one third and the flyback time is halfed.

The flyback circuit is shown in Figure 8 together with the power stage.

Figure 8 : Output Power and Flyback stages.

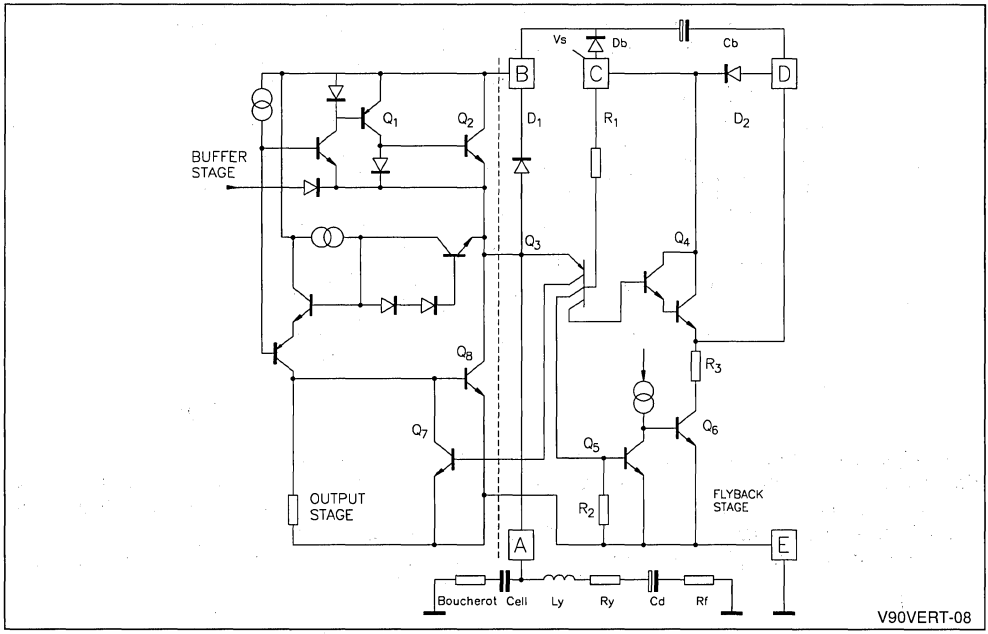
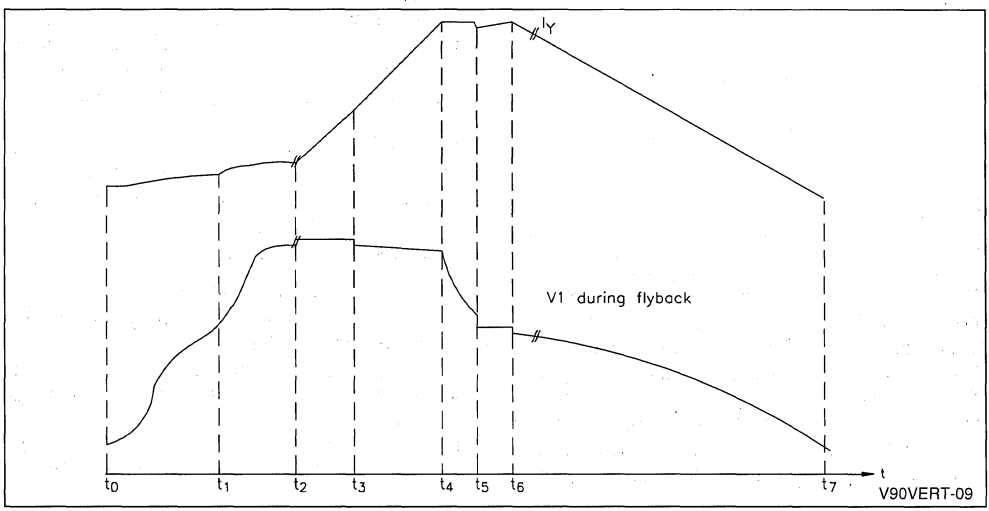


Figure 9 shows the circuit behaviuor, to show operation clearly. The graphs are not drawn to scale. Certain approximations are made in the analysis in order to eliminate electrical parameters that do not significantly influence circuit operations.

Figure 9 : Current in the Yoke and Voltage Drop on the Yoke during Vertical Deflection.



a) Scan period (t_6 - t_7) : Figure 10

During scanning Q_3, Q_4 and Q_5 are off and this causes Q_6 to saturate.

A current from the voltage supply to ground flows through D_B, C_B and Q_6 charging the C_B capacitor up to :

$VC_B = V_S - VD_B - VQ_{6SAT}$ (4)

At the end of this period the scan current has reached its peak value (I_P) and it is flowing from the yoke to the device. At the same time V_A has reached its minimum value.

In Figures 11 and 12 are depicted the voltage drop on the yoke and the currents flowing through D_B and the yoke.

Figure 10 : Circuit Involved during Scan Period.

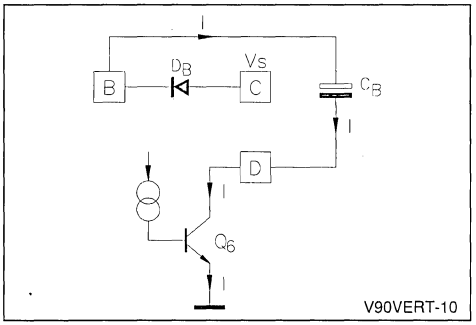


Figure 11 : Voltage Drop on the Yoke and Current Flowing through D_B.
V = 10V/div.
I = 0.5A/div.
t = 2ms/div.

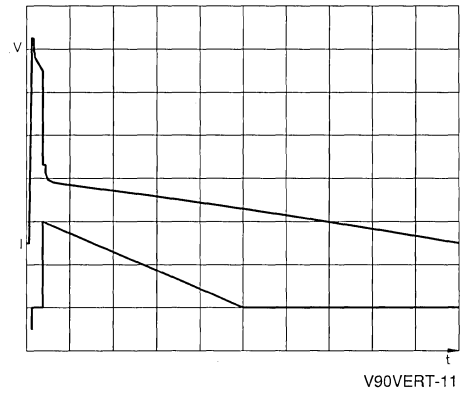


Figure 12 : Voltage Drop on the Yoke and Current Flowing through the Yoke.
V = 10V/div.
I = 1A/div.
t = 5ms/div.

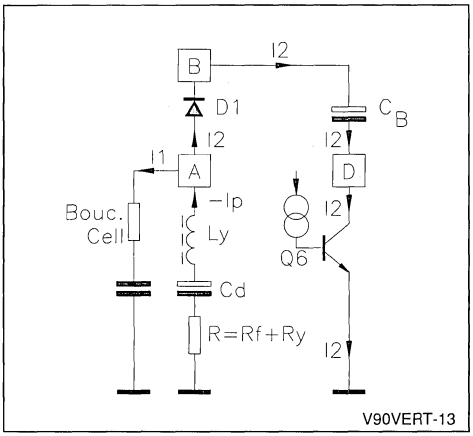
b) Flyback starting (t_0 - t_1) : Figure 13

Q_8, that was conducting the - I_P current, is turned off by the buffer stage.

The yoke, charged to I_P, now forces this current to flow partially through the Boucherot cell (I_1) and partially through D_1, C_B and Q_6 (I_2).

In Figures 14, 15 and 16 are represented the currents flowing through the yoke, the Boucherot cell and D_1.

Figure 13 : Circuit Involved during Flyback Starting.



c) Flyback starting (t_1 - t_2)

When the voltage drop at pin A rises over V_S, Q_3 turns on and this causes Q_4 and Q_5 to saturate. Consequently Q_6 turns off.

During this period the voltage at pin D is forced to :

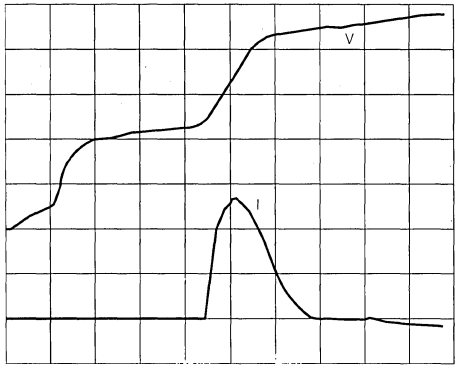
$$V_D = V_S - VQ_{4SAT} \qquad (5)$$

Therefore the voltage at pin B becomes :

$$V_B = V_{CB} + V_D \qquad (6)$$

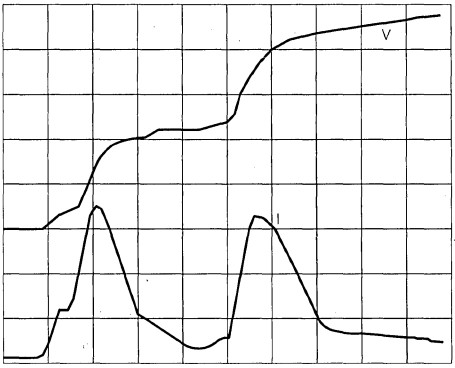
The yoke current flows in the Boucherot cell added to another current peak flowing from V_S via Q_4 and C_B (Figures 14 and 15).

Figure 15 : Voltage Drop on the Yoke and Current Flowing through D_1.
V = 10V/div.
I = 1A/div.
t = 1µs/div.



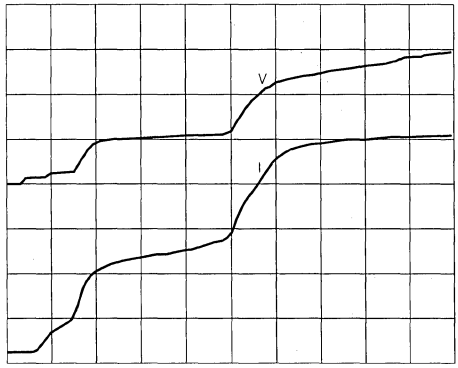
V90VERT-15

Figure 14 : Voltage Drop on the Yoke and Current Flowing through the Boucherot Cell.
V = 10V/div.
I = 1A/div.
t = 1µs/div.



V90VERT-14

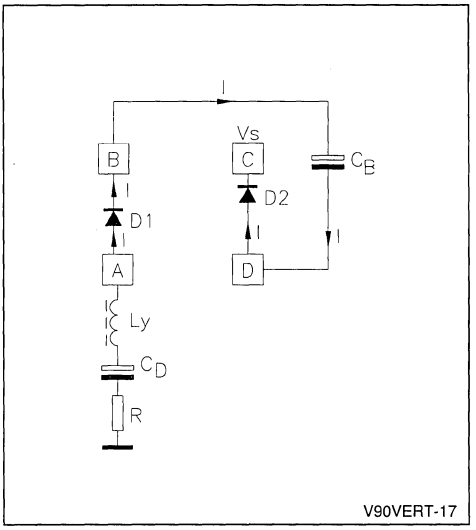
Figure 16 : Voltage Drop on the Yoke and Current Flowing through the Yoke.
V = 10V/div.
I = 100mA/div.
t = 1µs/div.



V90VERT-16

d) Negative current rise (t_2 - t_3) : Figure 17

Figure 17 : Circuit Involved during the Negative Current Rise.



During this period, the voltage applied at pin A is :

$$V_A = V_B + V_{D1},$$
$$V_A = V_{CB} + V_D + V_{D1},$$
$$V_A = V_S - V_{DB} - VQ_{6SAT} + V_S + V_{D2} + V_{D1},$$
$$V_A = 2 \cdot V_S + V_{D1} + V_{D2} - V_{DB} - VQ_{6SAT} \qquad (7)$$

It is possible to calculate the current solving the following equation :

$$V_A = L_Y \frac{di}{dt} + \frac{1}{C_D} \int i \cdot dt + R \cdot i \qquad (8)$$

where $R = R_F + R_Y$

Because the voltage at pin A is approximatively constant (error less than 2%) we can simplify the (8) in the following equation :

$$\frac{d^2 i}{dt^2} + \frac{R}{L_Y} \frac{di}{dt} + \frac{1}{L_Y C_D} i = 0 \qquad (9)$$

It results in :

$$i(t) = \frac{I_P}{e^{2\beta \Delta T_1} - 1} e^{(-\alpha + \beta)t} - \frac{I_P}{1 - e^{-2\beta \Delta T_1}} e^{(-\alpha - \beta)t} \qquad (10)$$

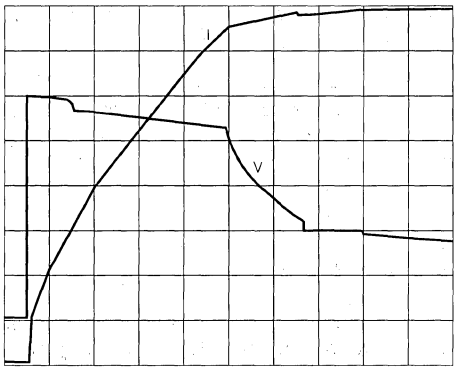
where :

$$\alpha = \frac{R}{2\ L_Y} \qquad \beta = \sqrt{\frac{R^2}{4 \cdot L_Y^2} - \frac{1}{L_Y C_D}} \qquad \Delta T_1 = t_3 - t_2$$

Because of ΔT_1 is two orders of magnitude lower than the scan time, we can apply an exponential sum to obtain the following equation :

$$i(t) = I_P \frac{\alpha \cosh(2\beta \Delta T_1) + \beta \sinh(2\beta \Delta T_1) - \alpha}{\cosh(2\beta \Delta T_1) - 1} t - I_P \qquad (11)$$

Figure 18 : Voltage Drop on the Yoke and Current Flowing through the Yoke.
V = 10V/div.
I = 250mA/div.
t = 100µs/div.



V90VERT-18

Simplifying :

$$i(t) = I_P \left(\alpha + \frac{1}{\Delta T_1} \right) t - I_P \qquad (12)$$

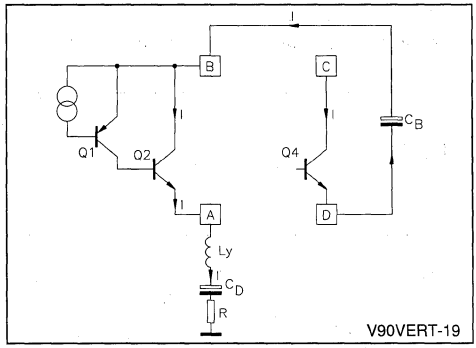
The slope of the current is therefore :

$$\frac{di}{dt} = \left(\frac{R}{2\,L_Y} + \frac{1}{\Delta T_1} \right) I_P \quad (A/s) \qquad (13)$$

The current flows from the yoke to V_S through D_1, C_B and D_2, and it is depicted in Figure 18.

e) Positive current rise (t_3 - t_4) : Figure 19

Figure 19 : Circuit Involved during the Positive Current Rise.



V90VERT-19

When the current becomes zero, D_1 turns off and Q_2 saturates; so the pin A voltage becames :

$$V_A = V_B - VQ_{2SAT}$$
$$V_A = 2 \cdot V_S - V_{DB} - VQ_{6SAT} - VQ_{4SAT} - VQ_{2SAT} \qquad (14)$$

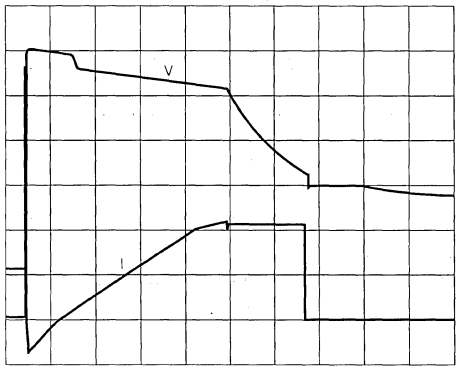
The current flows from $+V_S$ into the yoke through Q_4, C_B and Q_2 and rises from zero to I_P as it can be seen in Figure 18.
By using the previous procedure explained in section d), we can obtain the slope of the current :

$$\frac{di}{dt} = \left(\frac{R}{2\,L_Y} + \frac{1}{\Delta T_2} \right) I_P \quad (A/s) \qquad (15)$$

where $\Delta T_2 = t_4 - t_3$

f) Flyback decay (t_4 - t_5)
When the yoke current reaches its maximum peak, Q_2 desaturates and conducts the maximum peak current flowing from V_S via Q_4 and C_B into L_Y; the current flowing through C_B is depicted in Figure 20.

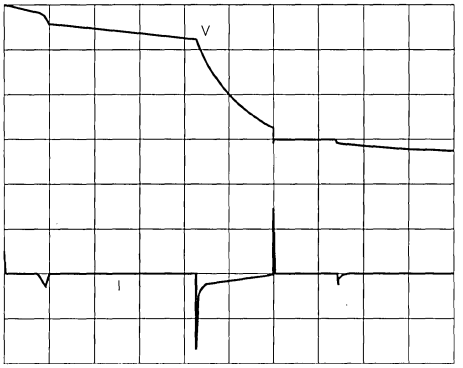
Figure 20 : Voltage Drop on the Yoke and Current Flowing through C_B.
V = 10V/div.
I = 0.5A/div.
t = 100µs/div.



V90VERT-20

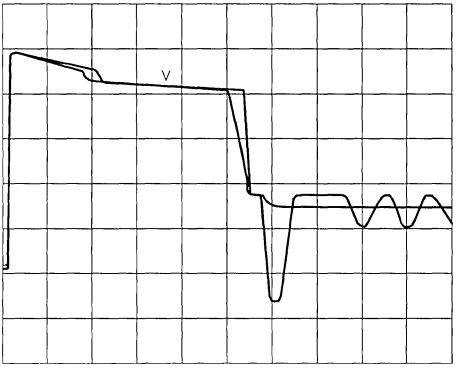
An eventual antiringing parallel resistor modify the linear decay slope in an exponential one, as it can be seen in Figure 22.
This continues until the buffer stage turns Q_2 on. The effect of the Boucherot cell during this periode is negligible (see Figure 21).

Figure 21 : Voltage Drop on the Yoke and Current Flowing through the Boucherot Cell.
V = 10V/div.
I = 100mA/div.
t = 100µs/div.



V90VERT-21

Figure 22 : Effect of the Resistor in Parallel connected to the yoke.
V = 10V/div.



V90VERT-22

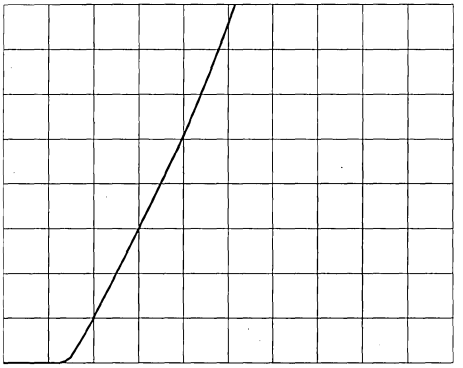
g) V_A pedestal (t_5 - t_6)

When V_A reaches the value V_S of the supply voltage, the flyback generator stops its function.
Q_3 is turned off and turns off Q_4 that open the connection between pin D and V_S.
Therefore V_B drops to V_S - V_{DB} while : $V_A = V_S - V_{DB} - VQ_{2CE\ on}$
At this point the normal scan takes place.

8. CURRENT-VOLTAGE CHARACTERISTICS OF THE RECIRCULATING DIODES.

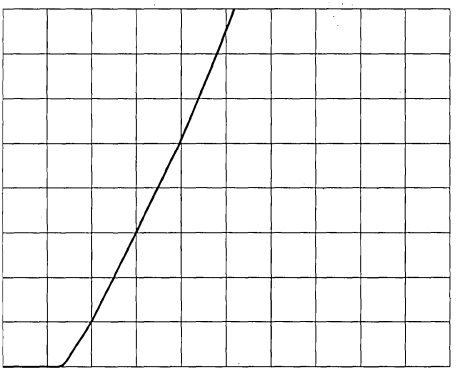
The following Figures 23 and 24 reproduce the I - V characteristics of the integrated recirculating diodes D_1 and D_2 (see Figure 8).

Figure 23 : I - V Characteristic of the Diode D_1.
V = 500mV/div.
I = 200mA/div.



V90VERT-23

Figure 24 : I - V Characteristic of the Diode D_2.
V = 500mV/div.
I = 200mA/div.



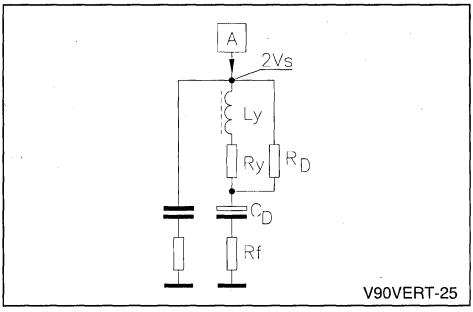
V90VERT-24

These characteristics are useful in order to calculate the maximum voltage reached at pin A with the formula (7) explained in chapter 7.

9. CALCULATION PROCEDURE OF THE FLY-BACK DURATION

The flyback duration can be calculated using the following procedure (referring to Figure 25).

Figure 25 : Circuit Involved in the Calculation of Flyback Duration.



During the flyback period the voltage applied at pin A is about 2 V_S, as previously explained in chapter 7. The voltage drop across C_D is approximatively a constant voltage little less than V_S /2. The voltage on the feedback resistor R_F is :

$VR_F(t) = R_F \; I_Y(t)$

so in the period which we are considering it is negligible respect to $V_S/2$.

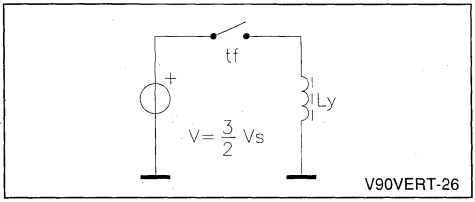
The effect of the Boucherot cell during this period is not sensible as it can be seen in Figure 21; while R_D acts principally during the flyback decay time (Figure 9 : t_4 - t_5) reducing its slope and the resulting oscillations but doesn't influence the total flyback time as shown in Figure 22. So their influences are also negligible.

Now the effective voltage drop across the yoke can be approximated to :

$$2 \cdot V_S - \frac{V_S}{2} = \frac{3}{2} V_S$$

Figure 25 can be simplified as shown in Figure 26.

Figure 26 : Simplified Circuit for the Calculation of Flyback Duration.



The voltage charges the coil with a linear current that can be calculated in the following way :

$$i(t) = \frac{1}{L_Y} \int V \cdot dt = \frac{1}{L_Y} \int \frac{3}{2} V_S \cdot dt \quad (16)$$

$$i(t) = \frac{1}{L_Y} \frac{3}{2} V_S \cdot t + K$$

K is calculated imposing that the current at the beginning of the flyback is - I_P.

$$i(0) = -I_P \qquad K = -I_P$$

$$i(t) = \frac{3}{2} \frac{V_S}{L_Y} t - I_P \quad (17)$$

At the end of the flyback period the current will be + I_P, so we can write :

$$I_P = \frac{3}{2} \frac{V_S}{L_Y} t_F - I_P$$

The duration of the flyback period is then :

$$t_F = \frac{4}{3} \frac{I_P L_Y}{V_S} = \frac{2}{3} \frac{I_Y L_Y}{V_S} \quad (18)$$

10. APPLICATION INFORMATION

The vertical deflection stages producted by SGS-THOMSON are able to cover the complete range of applications that the market need for color television and high/very high resolution monitors.

Television and monitor applications are not very different but in monitor field, in addition to the linearity and interlacing problems, we have to pay attention to the flyback time that must be very short for very high resolution models.

In television applications the most important requirement is to choose the lowest supply voltage possible in order to minimize the power dissipation in the integrated circuit, reducing the dimension of the heatsink, and the power dissipation from the voltage supplier.

These results can be reached very easily with SGS-THOMSON deflection stages because of the high efficiency of the flyback generator circuit used.

In high resolution monitors one of the main problems is to reach the very short flyback time requested; the flyback generator, together with the high current and power dissipation capabilities, solve all the problems in a simple way.

In Figures 27, 28 and 29 are depicted three typical application circuits for the different kinds of integrated circuits available.

Figure 27 : Application Circuit for TDA1170.

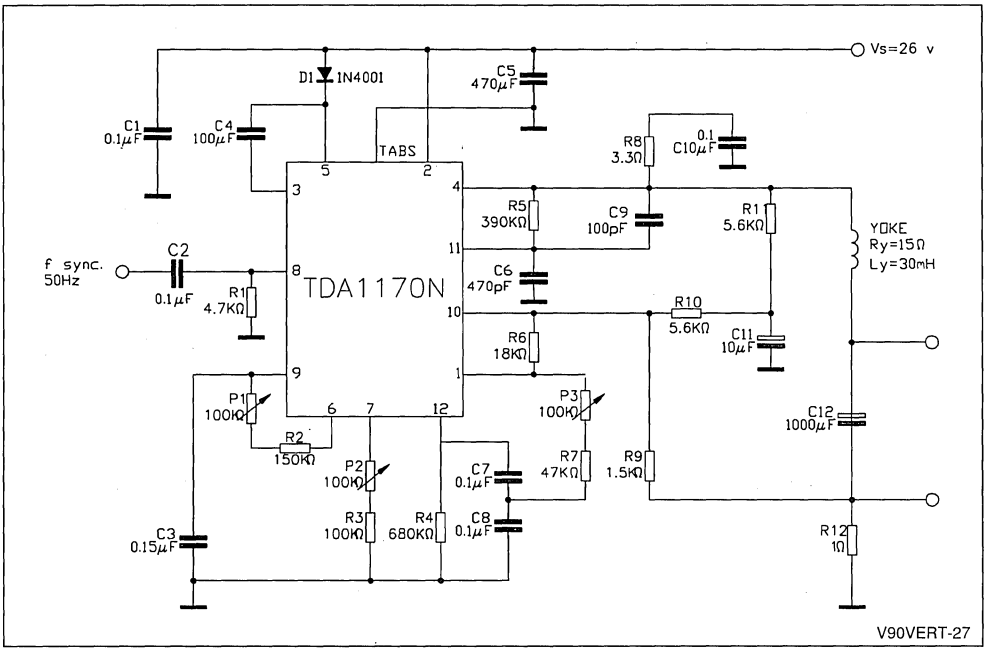


Figure 28 : Application Circuit for TDA1670A.

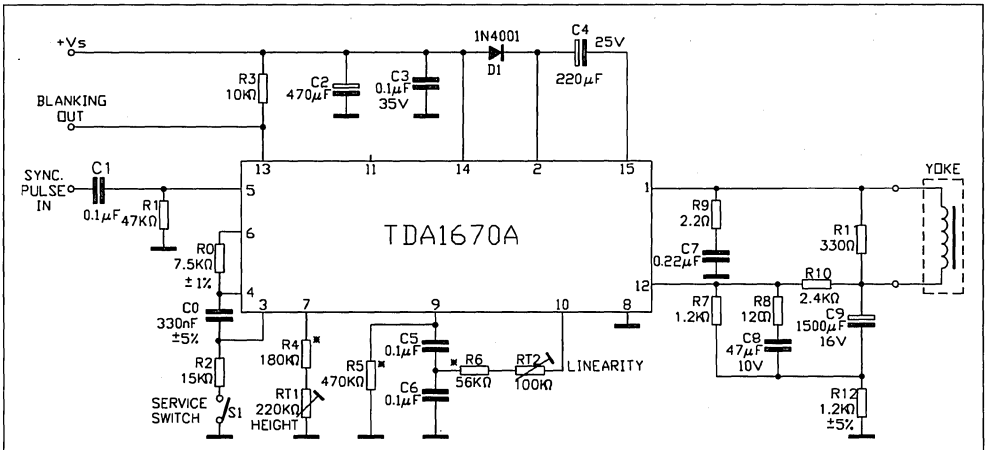
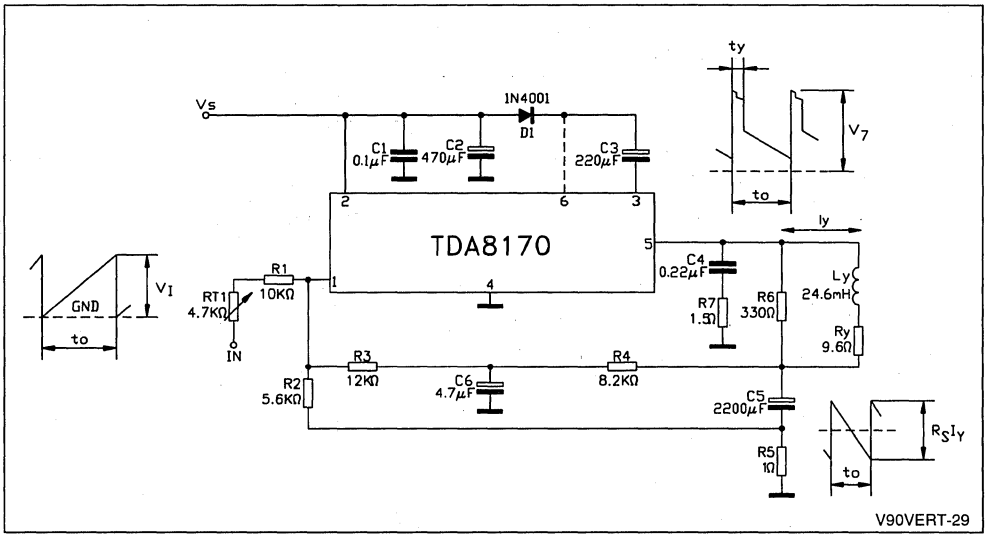


Figure 29 : Application Circuit for TDA8170.



In the following chapters we shall do the calculation for television and monitor in order to choose the right voltage supply and external network for the yoke used and the current requirements.

11. SUPPLY VOLTAGE CALCULATION

For television applications we shall calculate the minimum supply voltage necessary to have vertical scanning knowing the yoke characteristics and the current required for the given application.
Figure 30 shows the terms used in this section, while the circuit part involved in the following calculations is depicted in Figure 31.

Figure 30 : Parameters Used in the Calculation of the Supply Voltage.

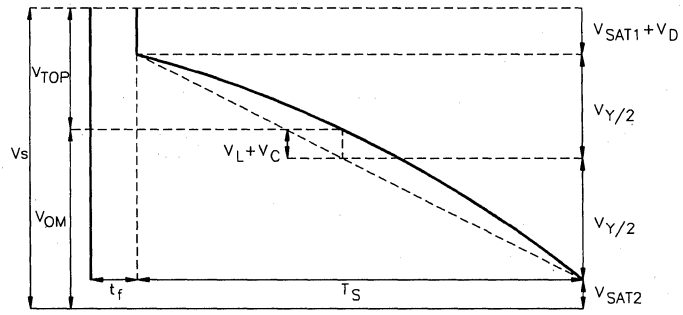
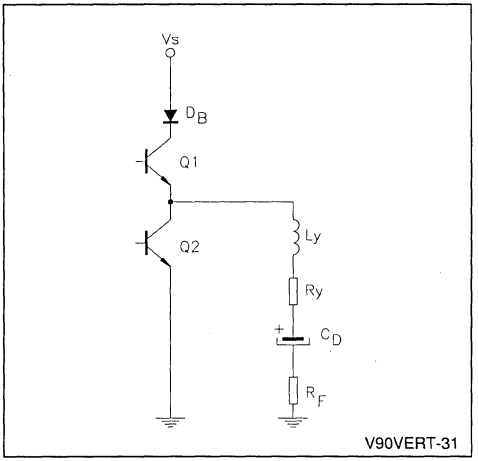


Figure 31 : Circuit Involved in the Calculation of the Supply Voltage.



V_S = supply voltage.
V_Y = nominal voltage required to produce the scanning current including the feedback resistance and the 20% increasing for temperature variations in the yoke current;

$$V_Y = (1.2\ R_Y + R_F)\ I_Y \qquad (19)$$

V_{SAT1} = nominal output saturation voltage due to the upper power transistor Q_1 (see Figure 32);
V_{SAT2} = nominal output saturation voltage due to the lower power transistor Q_2 (see Figure 33);
V_{OM} = nominal quiescent voltage (midpoint) on the output power transistors;
V_C = voltage peak due to the charge of C_D capacitor;

$$V_C = \frac{I_Y \cdot t_S}{8 \cdot C_D} \qquad (20)$$

V_L = voltage drop due to the yoke inductance L_Y;

$$V_L = \frac{L_Y \cdot I_Y}{t_S} \qquad (21)$$

Figure 32 : Saturation characteristic of the Upper Power Transistor.

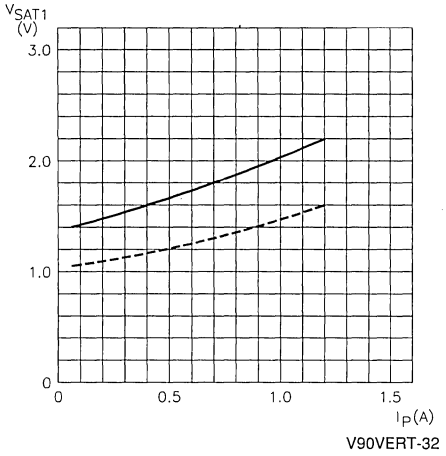
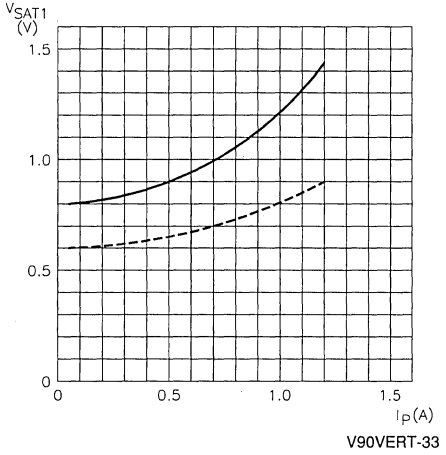


Figure 33 : Saturation characteristic of the Lower Power Transistor.



V_D = nominal voltage drop on D_B diode in series with the supply;
T = vertical scan period;
t_F = flyback time;

$$t_F = \frac{2}{3} \frac{I_Y \cdot L_Y}{V_S}$$

t_S = scanning time;

$$t_S = T - t_F$$

I_Y = peak to peak deflection current;
R_Y = nominal yoke resistance;
L_Y = nominal yoke inductance;
R_F = feedback resistor.

Referring to Figure 30 it is easy to see that the minimum supply voltage is given by :

$$V_S = V_{OM} + V_{TOP} \qquad (22)$$

where :

$$V_{OM} = \frac{V_Y}{2} + V_{SAT2} + V_C + V_L \qquad (23)$$

and :

$$V_{TOP} = \frac{V_Y}{2} + V_D + V_{SAT1} - V_L - V_C \qquad (24)$$

So we obtain :

$$V_S = V_Y + V_D + V_{SAT1} + V_{SAT2} \qquad (25)$$

The (25) gives the minimum voltage supply if we do not consider the tolerances of the integrated circuit and of the external components, but the calculation, even if it was not realistic, it was useful in order to understand the procedure.
Now we shall do the same thing considering all the possible spreads; we can in this way obtain the real minimum supply voltage.
We shall follow the statistical composition of spreads because it is never possible that all of them are present at the same time with the same sign.

We must consider the following spreads :

- ΔV_Y due to the variation of yoke and feedback resistance and yoke current, supposing a 10% of regulation range in scanning current and a precision of 7% for resistors;

$$\Delta V_Y = (1.2\, R_Y + R_F)\ 1.07\ (1.1\, I_Y) - V_Y \qquad (26)$$

- ΔV_C due to the tolerance of C_D and yoke current regulation;

$$\Delta V_C = \frac{1.1\, I_Y\, t_S}{8\, C_{D(MIN)}} - V_C \qquad (27)$$

- ΔV_L due to the tolerance of L_Y (± 10%) and yoke current regulation;

$$\Delta V_L = \frac{1.1\, I_Y\ 1.1\, L_Y}{t_S} - V_L \qquad (28)$$

$$\Delta V_{SAT1} = V_{SAT1(MAX)} - V_{SAT1}$$
$$\Delta V_{SAT2} = V_{SAT2(MAX)} - V_{SAT2}$$

For each parameter, it is necessary to calculate the factor ρ, expressing the percentual influence of every parameter variation on the nominal supply voltage, with the following formulas :

for V_{OM} :

$$\rho = \frac{\Delta V}{V_{OM}}$$

for V_{TOP} :

$$\rho = \frac{\Delta V}{V_{TOP}}$$

We have then to calculate the square mean root of the spreads expressed as :

$$\sqrt{\Sigma\ \rho^2}$$

So if we call :

$$V_{OM1} = V_{OM}\left(1 + \sqrt{\Sigma\ \rho^2}\right)$$

and :

$$V_{TOP1} = V_{TOP}\left(1 + \sqrt{\Sigma\ \rho^2}\right)$$

We can write :

$$V_S = V_{OM1} + V_{TOP1} \qquad (29)$$

An example of calculation will better explain the procedure. We shall consider a 26", 110°, neck 29.1mm tube whose characteristics are :
I_Y = 1.2 App;
R_Y = 9.6Ω ± 7%;
L_Y = 24.6mH ± 10%.

We shall use a coupling capacitance C_D of 1500µF with + 50% and - 10% tolerance and a feedback resistance R_F of 1.2Ω.

a) Nominal minimum supply voltage :

$$V_Y = (1.2\,R_Y + R_F)\,I_Y = 15.264\ V$$

$$V_C = \frac{I_Y \cdot t_S}{8 \cdot C_D} = 2\ V$$

$$V_L = \frac{L_Y \cdot I_Y}{t_S} = 1.476\ V$$

V_{SAT1} = 1.25 V V_{SAT2} = 0.68 V
V_D = 1 V
V_{OM} = 11.788 V V_{TOP} = 6.406 V

We obtain : V_S = 18.2V

b) Statistical minimum supply voltage :

ΔV_C = 2.702V

$$\rho V_{YM} = \frac{V_{Y/2}}{V_{OM}} \qquad \rho^2_{V_{YM}} = 1.313 \cdot 10^{-2}$$

$$\rho V_{YT} = \frac{V_{Y/2}}{V_{TOP}} \qquad \rho^2_{V_{YT}} = 4.447 \cdot 10^{-2}$$

ΔV_C = 0.445 V $\rho^2_{V_{CM}} = 1.421 \cdot 10^{-3}$
$\rho^2_{V_{CT}} = 4.813 \cdot 10^{-3}$

ΔV_L = 0.31 V $\rho^2_{V_{LM}} = 6.914 \cdot 10^{-4}$
$\rho^2_{V_{LT}} = 2.341 \cdot 10^{-3}$

ΔV_{SAT1} = 0.45 V $\rho^2_{V_{SAT1T}} = 4.935 \cdot 10^{-3}$

ΔV_{SAT2} = 0.27 V $\rho^2_{V_{SAT2M}} = 5.246 \cdot 10^{-4}$

$$V_{OM1} = V_{OM}\left(1 + \sqrt{\Sigma\,\rho^2}\right) = 13.268\ V$$

$$V_{TOP1} = V_{TOP}\left(1 + \sqrt{\Sigma\,\rho^2}\right) = 7.930\ V$$

$$V_S = V_{OM1} + V_{TOP1} = 21.2\ V$$

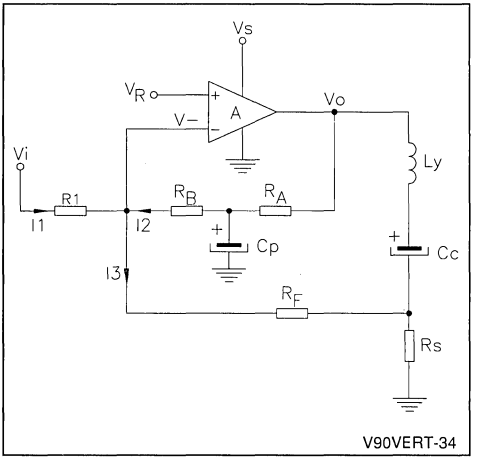
This is a real value for the minimum supply voltage needed by the above mentioned application.
In this case we obtain a flyback duration of about :

$$t_F = \frac{2}{3}\,\frac{I_Y \cdot L_Y}{V_S} \approx 900\ \mu s$$

12. CALCULATION OF MIDPOINT AND GAIN

For the calculation of the output midpoint voltage, it is necessary to consider the different feedback network for the applications of the various integrated circuits.
We shall first consider the TDA1170 family, the TDA1175, TDA2170, TDA2270, TDA8170, TDA8172, TDA8173, TDA8175 and TDA8176.
The equivalent circuit of the output stage is represented in Figure 34.

Figure 34 : Circuit Utilized for the Calculation of midpoint and gain for TDA1170, TDA1175, TDA8176, TDA2170, TDA2270, TDA8170, TDA8172, TDA8173 and TDA8175.



For DC considerations we shall consider the two capacitors as open circuits. Because of the very high gain of the amplifier we can suppose :
$V^- = V_R$.
We can so write :

$$I_1 + I_2 = I_3 \qquad (30)$$

where :

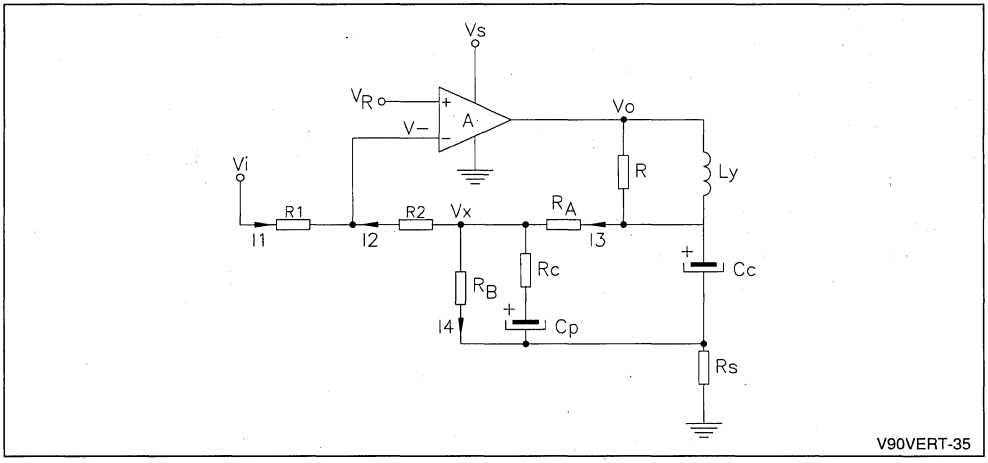
$$I_1 = \frac{V_i - V_R}{R_1} \qquad I_2 = \frac{V_O - V_R}{R_A + R_B} \qquad I_3 = \frac{V_R}{R_F + R_S}$$

Substituting into the (30) we obtain :

$$V_O = V_R \left(1 + \frac{R_A + R_B}{R_F + R_S}\right) - (V_i - V_R)\frac{R_A + R_B}{R_1} \qquad (31)$$

Let's consider now TDA1670A, TDA1675, TDA1770A, TDA1771, TDA1872A and TDA8174. The equivalent output circuit is depicted in Figure 35.

Figure 35 : Circuit Utilized for the Calculation of Midpoint and Gain for TDA1670A, TDA1675,TDA1770A, TDA1771, TDA1872A and TDA8174.



We can write :

$$I_1 = I_2 \qquad (32)$$

$$I_2 + I_3 = I_4 \qquad (33)$$

where :

$$I_1 = \frac{V_i - V_R}{R_1} \qquad I_2 = \frac{V_R - V_X}{R_2} \qquad I_3 = \frac{V_O - V_X}{R_A} \qquad I_4 = \frac{V_X}{R_B + R_S}$$

with the (32) and (33) we can calculate the DC output voltage. It results in :

$$V_O = V_R \left(1 + \frac{R_A + R_2}{R_1} + \frac{R_A(R_1 + R_2)}{R_1(R_B + R_S)}\right) - V_i \left(\frac{R_A + R_2}{R_1} + \frac{R_A \cdot R_2}{R_1(R_B + R_S)}\right) \qquad (34)$$

Referring to Figures 34 and 35, it is possible to calculate the transconductance gain of the power amplifier. For this calculation we shall do the following approximations :

- the capacitors are practically short circuits;
- the gain A of the amplifier is very high ($A \rightarrow \infty$).

For the circuit represented in Figure 34 we obtain :

$$I_Y = \frac{R_F}{R_1 \cdot R_S} V_i \qquad (36)$$

Using the (31), (34), (35) and (36) it is possible to calculate the external feedback network for every

while for the application in Figure 35 the yoke current results in :

$$I_Y = \frac{R_2 + R_A // R_B // R_C}{R_1 \cdot R_S} V_i \qquad (37)$$

different yoke known the scanning current and the midpoint output voltage.

Figure 36 : Open Loop Gain and Phase for the Application Circuit in Figure 27.

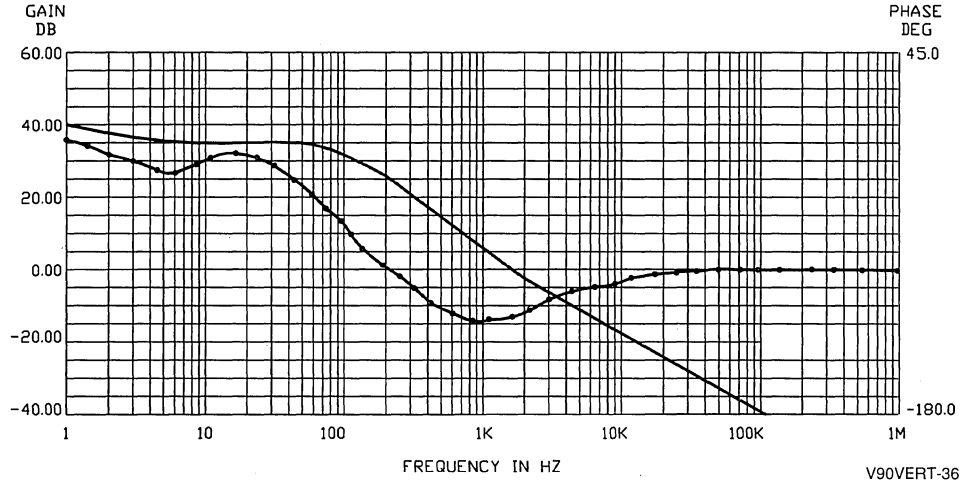
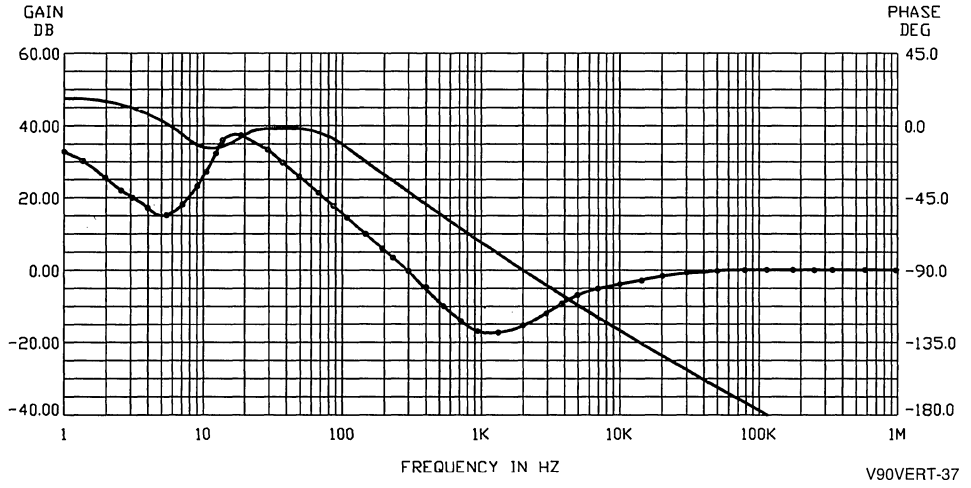
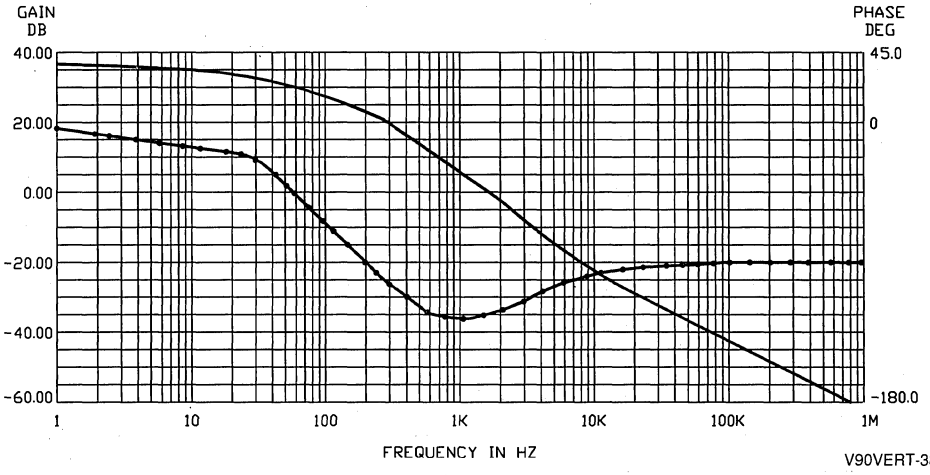


Figure 37 : Open Loop Gain and Phase for the Application Circuit in Figure 28.



We can now consider the open loop gain of the whole system amplifier plus external feedback network. This calculation is useful in order to verify that no oscillations can occur at any frequency.

Figure 38 : Open Loop Gain and Phase for the Application Circuit in Figure 29.



We shall consider some typical applications; the results are reported in Figures 36, 37 and 38.
It is easy to verify that in all cases, when the gain reaches 0dB, the phase margin is about 60°, so the stability of the system is assured.

13. MONITOR APPLICATIONS

In monitor applications the flyback time needed could be very smaller than the one we get using the minimum supply voltage calculation.

It is possible to reduce the flyback time in two different ways :
a) increasing the supply voltage, when the nominal value calculated is lower than the integrated circuit limit;
b) choosing a yoke with lower values in inductance and resistance and by supplying the circuit with the voltage needed for getting the right flyback time.

In both cases we have to calculate the biasing and the gain conditions using the nominal voltage and then we fix the supply voltage for the flyback time requested with the formula (18) :

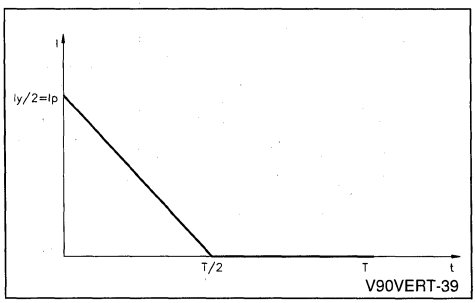
$$V_S = \frac{2}{3} \frac{I_Y \cdot L_Y}{t_F}$$

The calculation procedure for monitors is so the same as the one we have explained in the previous chapters for television applications.

14. POWER DISSIPATION

We shall now examine the power dissipation of the integrated circuit and the dimensions of the heatsink.
To calculate the power dissipated we must consider the maximum scanning current required to drive the yoke $I_{Y(MAX)}$ and the maximum supply voltage $V_{S(MAX)}$ because we have to dimension the heatsink for the worst case.
The current absorbed from the power supply is depicted in Figure 39.

Figure 39 : Current Absorbed from the Power Supply during Scanning.



The equation of the curve is :

$$i(t) = \frac{I_Y}{2} - \frac{I_Y}{T}\,t \qquad \text{for } 0 < t \le T/2$$

$$i(t) = 0 \qquad \text{for } T/2 < t \le T \qquad (37)$$

To the previous one we have to sum the DC current necessary to supply the other parts of the circuit (quiescent current).

The power absorbed by the deflection circuit is then :

$$P_A = \int_0^{T/2} V_{S(MAX)} \cdot i(t) \cdot dt + V_{S(MAX)} \cdot I_{DC}$$

$$= V_{S(MAX)} \int_0^{T/2} \left(\frac{I_{Y(MAX)}}{2} - \frac{I_{Y(MAX)}}{T}\,t \right) dt + V_{S(MAX)} \cdot I_{DC}$$

The solution is :

$$P_A = V_{S(MAX)} \left(\frac{I_{Y(MAX)}}{8} + I_{DC} \right) \qquad (38)$$

The power dissipated outside the integrated circuit is formed by the three following fundamental components : the scanning power dissipated in the yoke for which the minimum resistance of yoke $R_{Y(MIN)}$ and the maximum scanning current $I_{Y(MAX)}$ must be considered, the power dissipated in the feedback resistance R_F and that one dissipated in the diode for recovery of flyback.
The power dissipated outside the integrated circuit is then :

$$P_Y = \int_0^{T} (R_{Y(MIN)} + R_f)\, i^2(t) \cdot dt + \int_0^{T/2} V_D\, i(t) \cdot dt$$

$$= (R_{Y(MIN)} + R_f) \int_0^{T} \left(\frac{I_{Y(MAX)}}{2} - \frac{I_{Y(MAX)}}{T}\,t \right)^2 dt + V_D \int_0^{T/2} \left(\frac{I_{Y(MAX)}}{2} - \frac{I_{Y(MAX)}}{T}\,t \right) dt$$

The solution is :

$$P_Y = \frac{I^2_{Y(MAX)}\,(R_{Y(MIN)} + R_f)}{12} + \frac{I_{Y(MAX)} \cdot V_D}{8} \qquad (39)$$

The power dissipated inside the integrated circuit is :

$$P_D = P_A - P_Y \qquad (40)$$

The thermal resistance of the heatsink to be used with the integrated circuit depends upon the maximum junction temperature $T_{J(MAX)}$, the maximum ambient temperature T_{AMB} and the thermal resistance between junction and tab $R_{TH\ (J\text{-}TAB)}$ that is different for the various packages used. The thermal resistance of the heatsink is expressed by the following formula :

$$R_{TH\ J\text{-}AMB} = \frac{T_{J(MAX)} - T_{AMB(MAX)}}{P_{D(MAX)}} - R_{TH\ J\text{-}TAB} \qquad (41)$$

As an example we can calculate the dissipated power and the thermal resistance of the heatsink for the 26", 110°, neck 29.1mm tube for which we calculated the minimum supply voltage in chapter 11.

We shall consider the integrated circuit TDA1670A and we can suppose a maximum supply voltage of 25V.
The power absorbed from the supply is :

$$P_A = 25 \left(\frac{1.2}{8} + 0.04 \right) = 4.75\ W$$

The power dissipated outside the integrated circuit is :

$$P_Y = \frac{1.2^2 (9.6 \cdot 0.93 + 1.2)}{12} + \frac{1.21}{8} = 1.37\ W$$

therefore the power dissipated by the integrated circuit is :

$$P_D = 4.75 - 1.37 = 3.38\ W$$

The thermal resistance of the heatsink, considering the $R_{TH\ J\text{-}TAB}$ for the multiwatt package of 3°C/W, a maximum junction temperature of 120°C and a maximum ambient temperature of 60°C is :

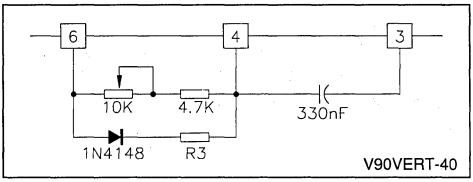
$$R_{TH\ H\text{-}AMB} = \frac{120 - 60}{3.38} - 3 = 15°C/W$$

For the same application with TDA1170S we have a thermal resistance for the heatsink of about 8°C/W.

15. BLANKING PULSE DURATION ADJUSTMENT

For the devices that have the blanking generator it is possible to adjust the blanking pulse duration. We shall consider as an example the TDA1670A; the circuit arrangement is depicted in Figure 40.

Figure 40 : Circuit Arrangement for Blanking Pulse Duration Adjustment.



By adjusting R_3 the blanking pulse duration will be adapted to the flyback time used and the picture tube protection will be ready to work properly.

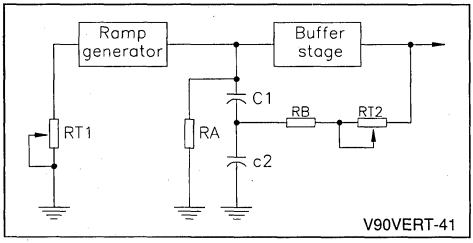
When necessary, it is possible to use a trimmer system to adjust it very carefully.

16. LINEARITY ADJUSTMENT

The complete vertical stages have the possibility to control the linearity of the vertical deflection ramp. There are two different methods to obtain the above mentioned performance.

a) For the first method we shall refer to Figure 41.

Figure 41 : Circuitry for Ramp Linearity Regulation.



The linearity regulation is obtained by means of R_A, R_B and R_{T2}.

In order to choose the right values of this components we suggest to follow the following procedure :
1 - Set the amplitude regulation potentiometer R_{T1} for the nominal raster size;
2 - Disconnect the R_A resistance;
3 - Adjust the linearity control potentiometer R_{T2} in order to obtain the top and the bottom of the raster with the same amplitude;
4 - In this condiotion the center of the raster must be narrower then the top and the bottom. If with R_A

disconnected the center is larger than the top and the bottom it is necessary to act on the feedback network. Referring to Figures 27, 28 and 29 it is necessary to increase the capacitors C_{11}, C_8 or C_6;
5 - After increasing the capacitors it is necessary to repeat the linearity adjustment (R_{12} potentiometer) in order to get the top and the bottom with the same amplitude again;
6 - Connect the R_A resistor and repeat the linearity adjustment (point 3 regulation);
7 - Check the top and the bottom amplitude comparing it with the center. If the center amplitude is still narrower it is necessary to reduce R_A. If the center amplitude becomes larger it is necessary to increase R_A.

Note : Every time the linearity conditions are changed (for adjusting or setting) before checking the linearity status, the point 3 adjustment must be repeated.

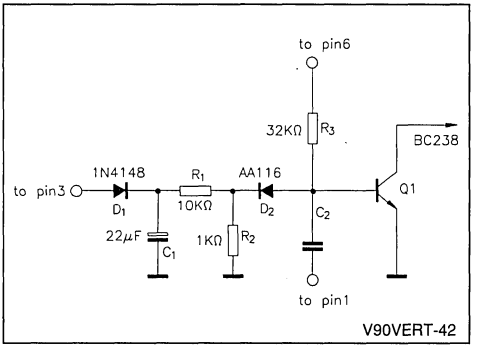
b) For the second method we shall refer to Figure 28.
In this case the linearity regulation is obtained acting directly on the feedback network, that is substituting the R_8 resistance with a potentiometer. This solution is cheaper than the first one, because it is possible to save the resistors R_A, R_B (see Figure 41), the potentiometer R_{T2} and to use only a capacitor instead of the series C_1 and C_2.
On the other hand a disadvantage is due to the fact that the resistance R_8 influences not only the linearity of the ramp but also the gain of the amplifier, as it can be seen in the equation (36). So to perform a linearity adjustment it is necessary to act at the same time on the potentiometer in the feedback loop and on the potentiometer R_{T1} (see Figure 41) in order to correct the vertical amplitude variations. On the contrary, in the method a) the linearity control network doesn't influence any other parameters. this is the reason why the a) method is generally adopted by all television set producers.

17. FACILITIES AND IMPROVEMENTS

In this section we shall briefly examine some facilities which may be useful to improve operations of the television set.

a) Blanking generator and CRT protection for TDA1170 family.
At pin 3 a pulse is available which has the same duration and phase as the flyback and amplitude equal to the supply voltage.
If the retrace duration is not sufficient for carrying out correct vertical blanking, for instance in the presence of text and teletext signals the circuit of Figure 42 can be used.
The true blanking generator is formed by Q_1,R_3 and C_2 and the blanking duration is dependent upon the values of R_3 and C_2. The other components are used for picture tube protection in the event of loss of vertical deflection current. If for any reason there is no flyback, the transistor Q_1 is permanently inhibited and provides continuous switch off which eliminates the white line at the center of the screen. Thermal stability and stability with the supply voltage is good in relation to the simplicity of the application.

Figure 42 : Blanking Generator and CRT Protection for TDA1170.



b) Vertical deflection current compensation to maintain picture size with beam current variations.

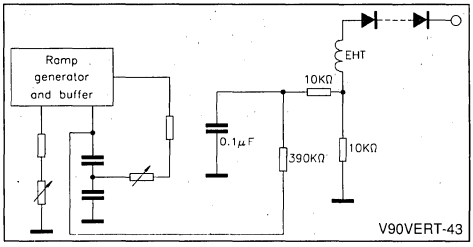
Changes in the supply voltage or the brightness and contrast controls will bring out changes of the beam current, thus causing EHT and picture size variations.
The rate of change of the picture size is mainly dependent upon the EHT internal resistance.
In order to avoid variations of the vertical picture size it is necessary to track the scanning current to the beam current. Because the tracking ratio :

$$\frac{\Delta I_{YOKE}}{\Delta I_{BEAM}} \cdot 100 \qquad (42)$$

varies from one chassis design to another, three suggested tracking circuits are shown in Figures 43, 44 and 45.

The circuit in Figure 43 adopts the straight forward technique of linking the vertical scanning current directly to the beam current .Its drawback lies in the fact that a long wire connection is required between the EHT transformer and the vertical circuit, and the layout of this connection could be critical for flashover.

Figure 43 : Circuit for Vertical Scanning Current Variation according with the Beam Current.



The circuit of Figure 44, which links the vertical scanning current directly to the supply voltage, is the simplest one. Its drawback could be incorrect tracking ratio and ripple on the supply voltage.To overcome the drawbacks of the preceding circuit it is usefull to filter out the supply voltage ripple and adjust the tracking ratio by transferring the supply voltage to a lower level by means of a Zener diode as shown in Figure 45. Tracking ratio is adjusted by choosing a suitable Zener voltage value.

Figure 44 : Circuit for Vertical Scanning Current Variation according with the Supply Voltage.

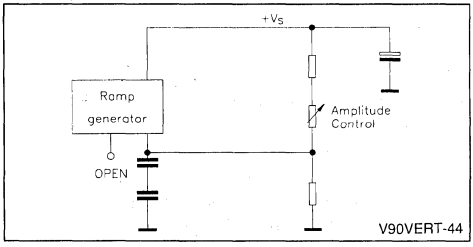
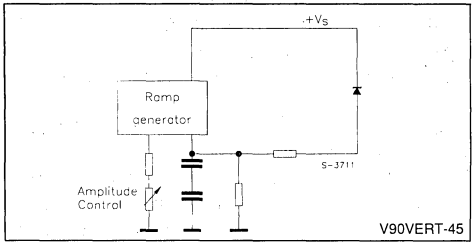


Figure 45 : Circuit for Vertical Scanning Current Variation according with the Supply Voltage.



18. GENERAL APPLICATION AND LAYOUT HINTS

In order to avoid possible oscillations induced by the layout it is very important to do a good choice of the Boucherot cell position and ground placing. The Boucherot cell must be placed the most possible closed to the vertical deflection output of the integrated circuit, while the ground of the sensing resistor in series connected with the yoke must be the same as the one of the integrated circuit and different from the one of other power stages. Particular care must be taken in the layout design in order to protect the integrated circuit against flashover of the CRT. For instance the ground of the filter capacitor connected to the power supply must be near the integrated circuit ground.

19. REFERENCES

1) Television Deflection Systems - A. Boekhorst, J. Stolk - Philips Technical library.
2) TV Vertical Deflection System TDA1170S - SGS-THOMSON Application Notes.
3) TDA1670A Technical Note - SGS-THOMSON Technical Note.
4) TV and Monitor Vertical Deflection using TDA1670A - O. Cossutta, F. Gatti SGS-THOMSON Application Notes.
5) TDA1670A Flyback Stage Behaviour - A. Messi, G. Nardini - SGS-THOMSON Application Notes.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TDA8102A

by Fabio GRILLI

TECHNICAL INFORMATION

APPLICATION INFORMATION

TECHNICAL INFORMATION

1. ABSTRACT

The system evolution in the monitor field leads to develop suitable I.C.'s whose performances and characteristics are mainly monitors oriented rather than TV oriented. The automatic frequencies raster preset of the monitor by computer and optical equipments leads to the adoption of Digital to Analog converters in order to set the different parameters, and consequently all regulation must be DC compatible.

High scanning frequency and low jitter are additional factors that characterize the quality and the resolution of the monitor. In this note new circuit solutions on silicon, concerning the monitor field, are described. In a single I.C., making use of TTL compatible synchro pulses, horizontal and vertical processing functions and vertical ramp generation are implemented.

INTRODUCTION

In Fig.1 is shown the block diagram of TDA8102A.

Horizontal frequency and phase as well as vertical frequency, amplitude and linearity are all DC adjustable on different terminals.The horizontal phase adjustment within ± 45° is implemented on first PLL (sync-oscillator) rather than on the second PLL (flyback-oscillator) allowing the raster to be centered in case of no standard phase sync position.

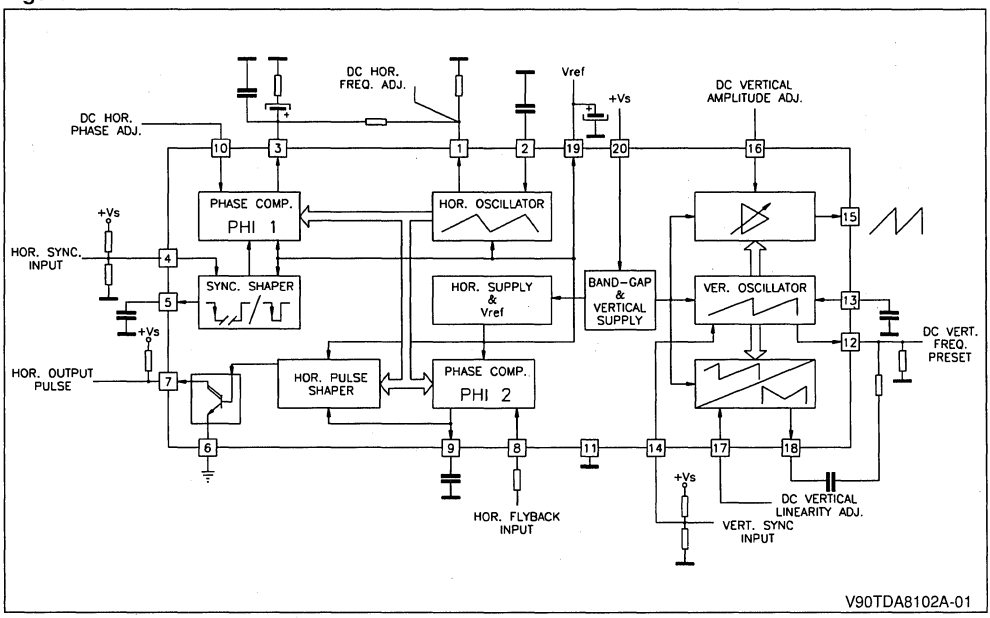
An additional feature makes the raster phase independent by the duty-cycle of the input synchronizing pulse thanks to an internal shaper circuit generating a standard sync pulse starting from the leading edge of input signal.

The vertical amplitude changes depending on a voltage amplifier whose gain is set on Pin 16 ; the peak to peak voltage of the sawtooth does not influence its average value which is maintained constant.

The current capability of the horizontal output stage (Pin 7) is such to directly drive an external darlington used as line power switch.

Since part of the jitter effect is due to the internal voltage reference circuits, an external pin connected to the V_{CO} supply voltage is got available for noise filtering (Pin 19).

Figure 1.



3. FUNCTIONAL DESCRIPTION

Here following are briefly described all the functional blocks of TDA8102A.

3.1 Horizontal oscillator

The circuit in Fig.2 is a Current Controlled Oscillator, it works charging and discharging the capacitor at pin 2 between two thresholds V_{S1} = 2.5V and V_{S2} = 6.5V coming from an internal resistor divider. This one is also used to provide a voltage reference at pin 1 (V_1 = 3.5V) by means of a unity gain amplifier.

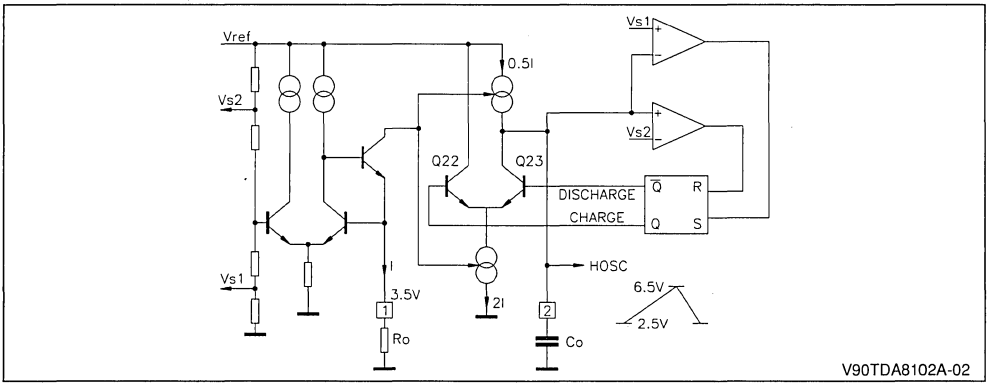
An external resistor connected between Pin 1 and ground sets the current reference.

This current is mirrored with 0.5 : 1 ratio to charge the capacitor C_O at Pin 2, and with 2 : 1 ratio to discharge C_O.

The charging and discharging time ratio will result in 3 : 1.

The differential switch Q_{22}-Q_{23} is driven by a S-R flip-flop, which changes its state every time that the peak of the triangular waveform reaches one of the two thresholds V_{S1} or V_{S2}.

Figure 2.



3.2 Horizontal synchronism shaper circuit

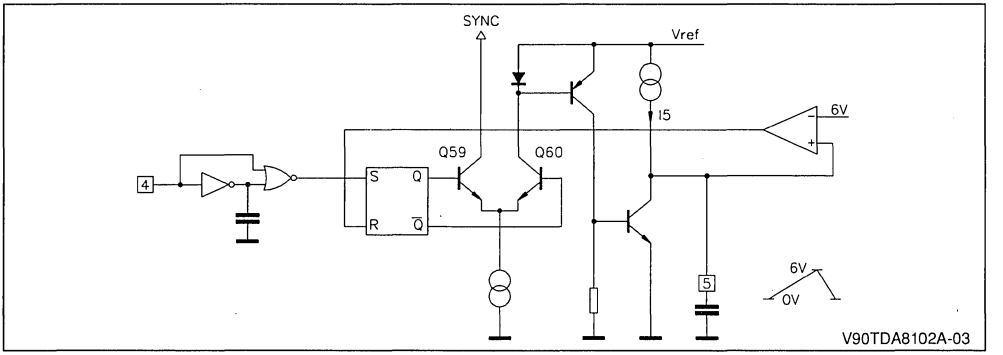
The electric diagram shown in Fig.3 can be divided in three stages. The first of which is a negative edge detector able to set the S-R flip-flop each time that a negative edge of the sync pulse is applied to the input (Pin 4).

The second one is a differential stage that feeds the first phase comparator (φ 1).

The third stage uses an external capacitor to produce a ramp on the Pin 5. As soon as the peak of the ramp reaches the internal threshold (6V) the external capacitor is suddenly discharged and the flip-flop is reset.

The horizonal sync pulse width on the collector of Q_{59} will depend on the value of the capacitor at Pin 5.

Figure 3.



3.3 First phase comparator (φ 1) and phase adjustment interface circuit

In the circuit of Fig.4, a comparator squares the horizontal waveform using as voltage reference Vref1 which represents the output of the phase adjustment interface circuit.

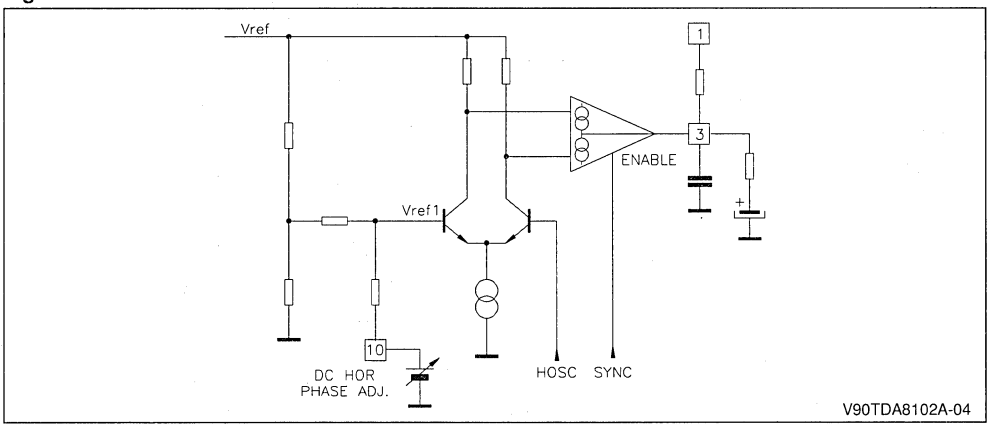
If the voltage at Pin 10 changes in the range from 0.5V to 4.5V, the phase will shift of ± 45° between the sync and the flyback pulse.

The rectangular waveforms that are the outputs of first differential amplifier are applied to another differential stage which is activated only during the horizontal sync pulse coming from the horizontal sync shaper circuit.

The product in terms of current of the sync signal and the oscillator signal is available at Pin 3.

Two clamp limit the maximum voltage range of Pin 3 (from 1V to 6V) and consequently the hold in range of the CCO.

Figure 4.



3.4 Second phase comparator (φ 2) between flyback and oscillator

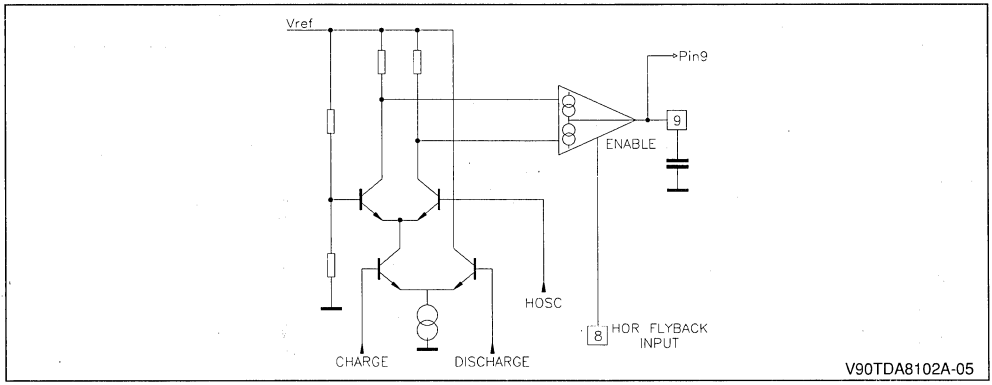
This circuit recovers dynamically the deflection delay of line output transistor.

The flyback pulse applied to Pin 8 (see Fig.5) is detected and clamped at a voltage level of 0.7V.

This circuit is similar to φ 1, the substantial differences are two, the input pulse is the flyback pulse instead of sync pulse and the first differential stage is activated by S-R flip-flop of horizontal oscillator.

The φ 2 output acts on the horizontal output stage in order to shift the output pulse to recover the deflection delay.

Figure 5.



3.5 Phase shifter, output stage and start up circuit

The storage time ts of the line output transistor is recovered by advancing the leading edge of the output pulse of ts with respect to the phase of the sync reference.

The triangular oscillator waveform (Fig.6a) is compared with internal threshold S_1 and S_2 whose voltages depend upon the voltage level present at the output of phase comparator φ 2.

The voltage difference S_1-S_2 is constant and this value fixes the duty-cycle of the horizontal output pulse present at Pin 7.

During the positive slope of the oscillator the output pulse (Pin 7) is low when the triangular waveform voltage is in the voltage range established by S_1 and S_2; whereas during the negative slope of the oscillator the output pulse is always at high level thanks to a comparator drived by S-R flip-flop of horizontal oscillator.

As shown in Fig.6a, a transistor insures that the output pulse is low when the flyback pulse is present.

At the switch on, the horizontal output stage (Pin 7) is inhibited until the power supply does not overcome 8 V.

Figure 6a.

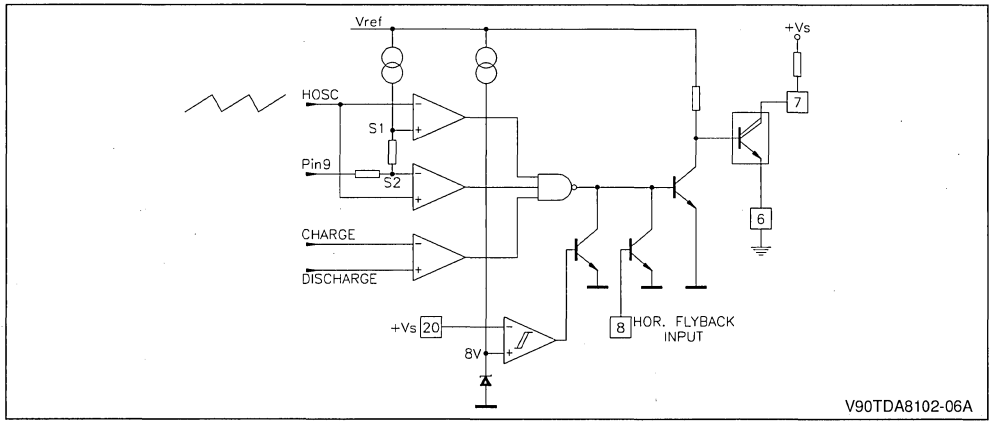
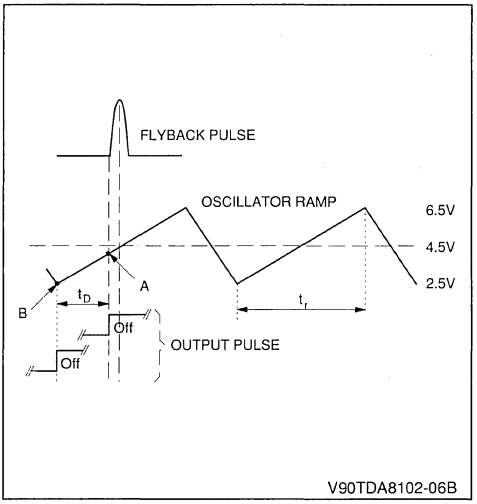


Figure 6b.



About the maximun allowable delay, it depends on the flyback time and the working frequency (see Fig.6b).

The PLL2 works in such a way to maintain the middle of the flyback exactly in correspondence between the crossing of the V_{REF} = 4.5V and the oscillator ramp.

Then if you suppose to have zero delay time, the switch-off edge of the output pulse will rise at point "A" now if the delay time increases the switch-off edge will move to point "B" to recover the delay.

The equation to calculate the t_D with a good approximation is the following :

Maximum Allowable Delay :

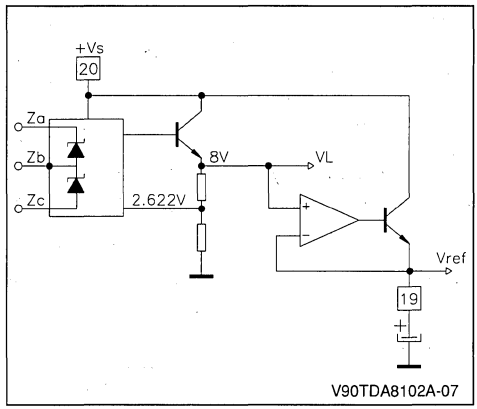
$$t_D = \frac{t_r}{2} - \frac{t_{FLY}}{2}$$

where t_R is the rise time of the horizontal ramp = 3/4 T and t_{FLY} is the flyback time.

3.6 Voltage regulator 8 V

The voltage reference, Fig.7, is a band-gap circuit that allows on the output a voltage reference equal to 2.622V that means a voltage V_L = 8V.
By means of zener zap is possible to adjust, during the testing, the voltage reference from ± 6% into a ± 2% range.
V_L feeds all the circuits of the vertical side and, by means of a unity gain amplifier, provides a voltage reference (V_{REF}) at Pin 19 to supply all the circuits of the horizontal side.
The unity gain amplifier is necessary to avoid all the possible interactions between the horizontal and vertical sections.
Moreover, to minimize jitter on the horizontal oscillator, is possible to connect an external capacitor between Pin 19 and ground.

Figure 7.



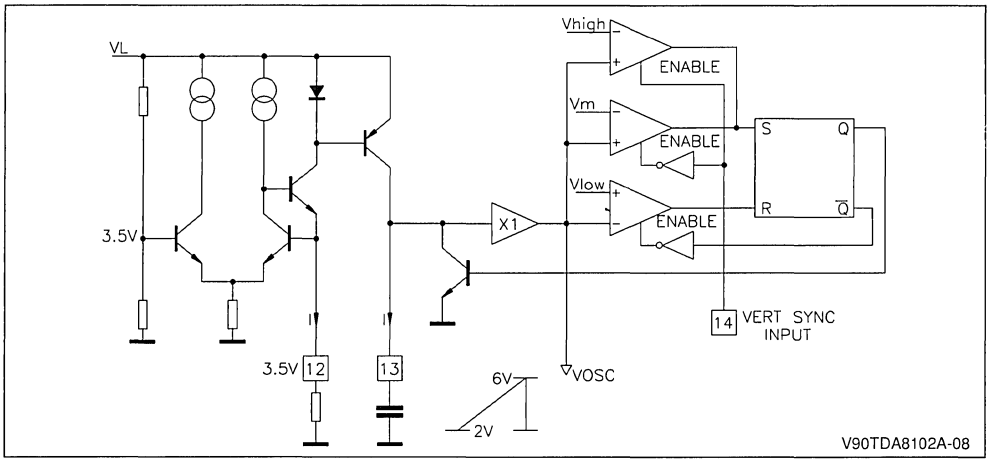
3.7 Vertical oscillator

A new concept of vertical oscillator is implemented in this I.C. whose resistor divider, used to set the lower and higher thresholds (V_{low} = 2V ; V_{high} = 6.8V), is not commutated .
The circuit shown in Fig.8 works charging an external capacitor connected at Pin 13 with a current set at Pin 12 and reflectd to Pin 13 through a current mirror.
As soon as the ramp gets V_m or V_{high} the capacitor is quickly discharged by a darlington, the voltage on the capacitor will fall down till to get the lower threshold; at this point the darlington will be driven off and the current will charge again the capacitor.
A buffer is used to decouple the ramp generator from other circuits (like linearity correction and amplitude regulation circuits).
The lower threshold is detected by a differential stage whose current generator is only activated during the discharge phase.
A comparator detects the higher threshold corresponding to the free running frequency; if no sync pulse (negative edge) is applied on Pin 14, this stage is continually fed and the capacitor at Pin 13 is discharged when the vertical ramp reaches V_{high}.
If the sync pulse is present the previous comparator will be inhibited and another comparator, which has the threshold at 5.2V (V_m), will be activated.
This last comparator, when it is set going, is able to cause the discharge of the capacitor at Pin 13 if the vertical ramp is between the thresholds Vm and V_{high}.
In this way the vertical synchronization is established.
To guarantee that the vertical oscillator is locked in the middle of the pull-in range is necessary to adjust the current at Pin 12 until the peak of the vertical sawtooth, in locking condition, reaches the voltage equal to:

$$V_P = \frac{V_m + V_{high}}{2} = 6\ V$$

that means V_{pp} = 4V.

Figure 8.



3.8 S Correction circuit and DC linearity adjustment

The circuit which is used to realize a new concept of vertical linearity regulation is shown in Fig.9.

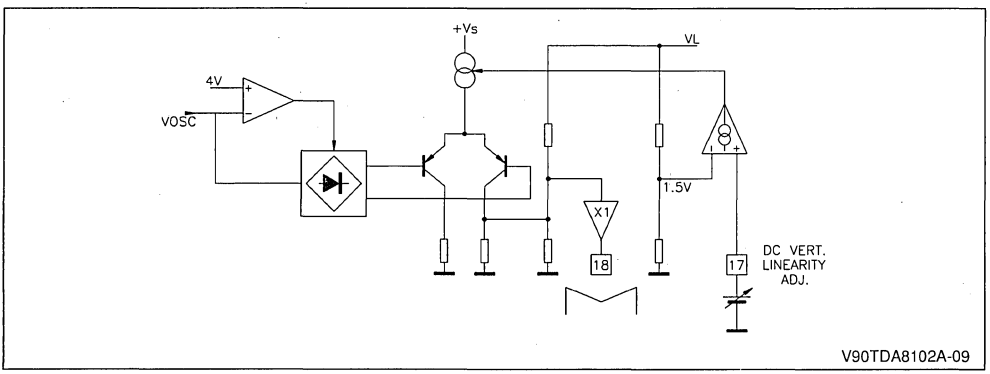
A comparator squares the vertical sawtooth using as voltage reference a fixed value (4V) that is the average value of sawtooth.

This squared signal is used to drive a particular configuration of differential stage in order to obtain, in terms of current, a triangular waveform which inverts its slope just when the original sawtooth crosses the voltage reference.

This current signal is converted in voltage by a resistor divider and transferred on Pin 18 through a buffer.

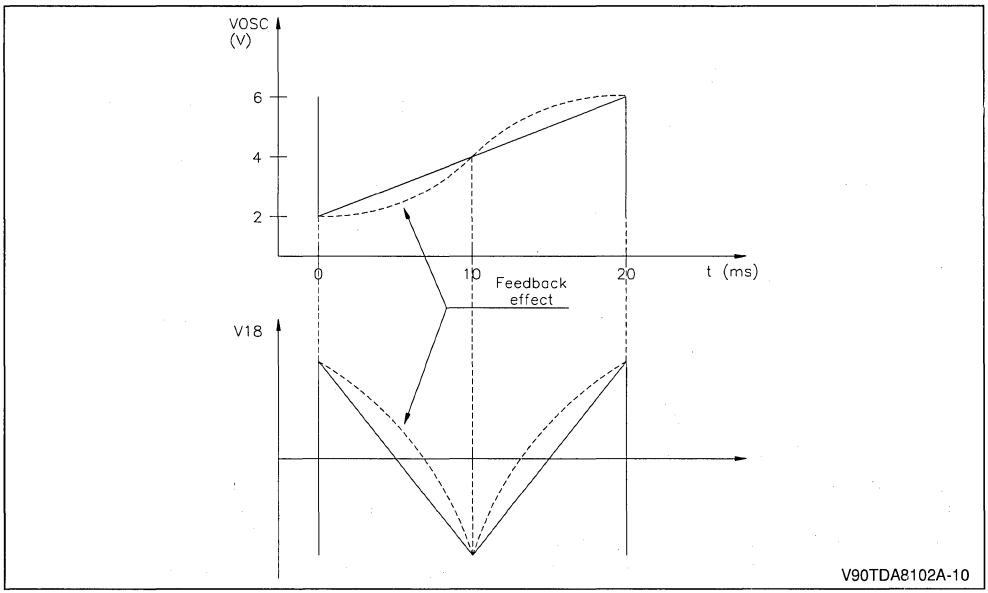
The peak to peak voltage on this pin depends on the maximum current that the output differential stage is able to handle, the value of this current can be externally regulated by means of Pin 17 through a transconductance amplifier.

Figure 9.



An external feedback resistor in series to a capacitor (to avoid any DC offset) must be connected between Pins 18 and 12 in order to obtain the proper S correction as shown in Fig.10.

Figure 10.



3.9 Vertical amplitude regulation circuit

This function has been implemented using the circuit configuration that can be seen in Fig.11.

It consists of an Op-Amp in non inverting input configuration and of a variable gain OTA whose gain can be set by means of the Pin 16 through a transconductance amplifier.

Both the inputs of the two circuit handle the vertical ramp and the output of the multiplier is fed back to the inverting input.

The control circuit is a transconductance amplifier that modulates the current of the variable gain OTA depending on the DC voltage applied on Pin 16.

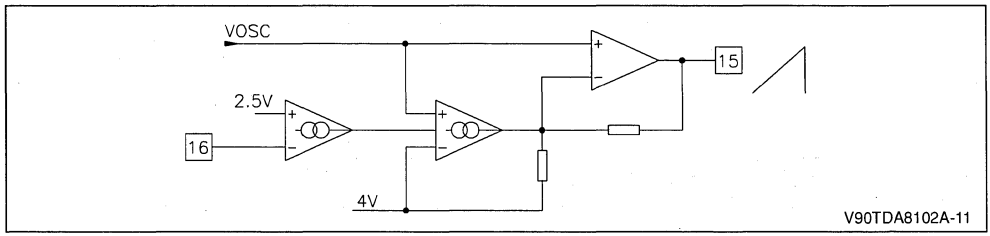
This circuit guarantees a gain adjustment of ± 20% around the nominal value.

4. CONCLUSION

This new I.C. can be considered as a first step towards a new generation of serial bus compatible LSI circuits in which additional logic function can be implemented and all the D/A converters can be included.

It is assembled in 20 pins DIL plastic package able to dissipate the 0.7W required by a typical application.

Figure 11.



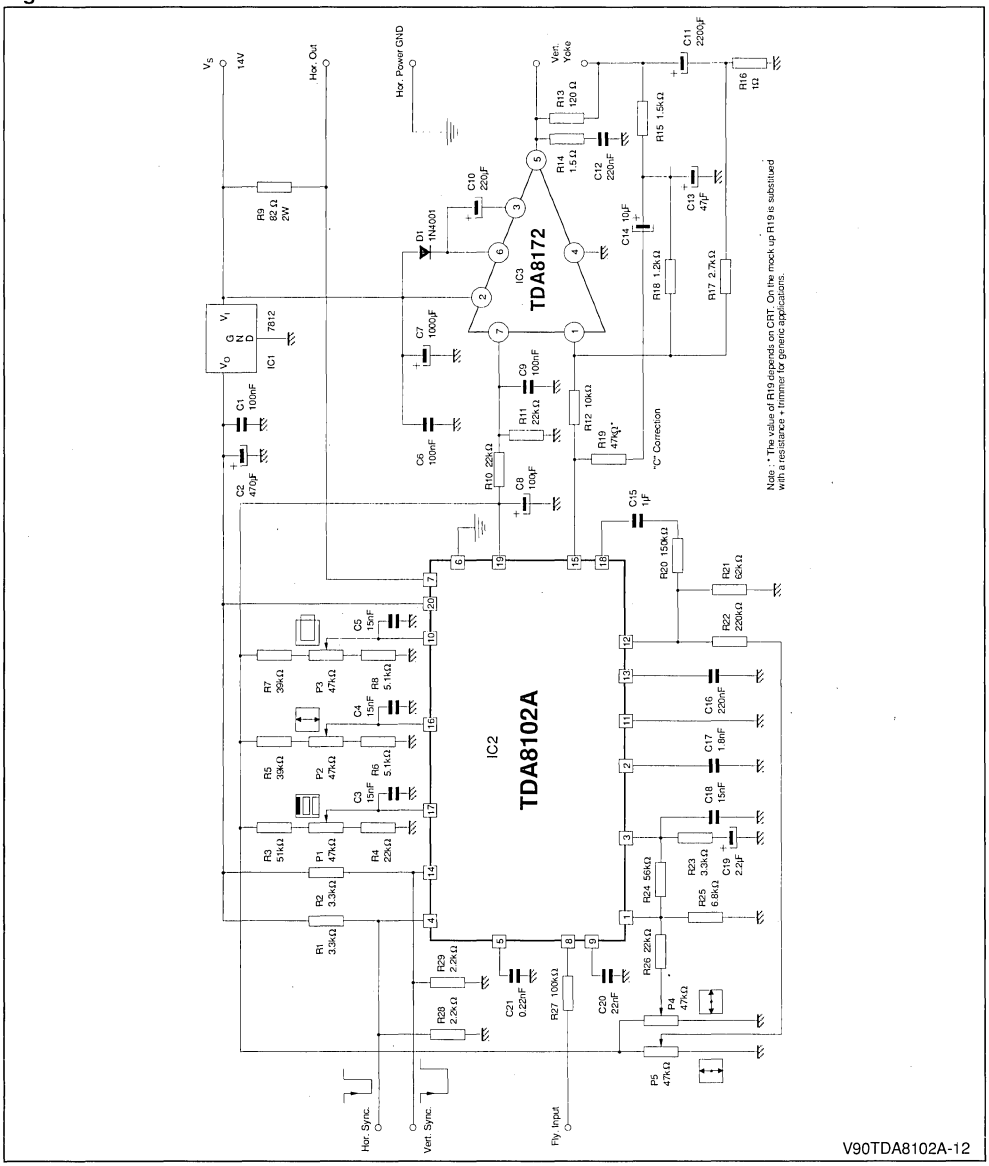
APPLICATION INFORMATION

In Fig.12 is shown a typical application of the TDA8102 A with the TDA8172, which is a vertical booster; for further information regarding TDA8172 consult the note :

SGS-THOMSON "Vertical Deflection Stages for TV and Monitor" by A. MESSI

All the information is referred to the above mentioned figure.

Figure 12.



5. HORIZONTAL SECTION

5.1 Frequency

The device is able to work from 15 KHz to 100 KHz. The free running frequency is fixed by the resistor at Pin 1 (R_{25}) and by the capacitor at Pin 2 (C_{17}) with the following formula:

$$f_O = \frac{1}{K_O \times R_{25} \times C_{17}}$$

where K_O is typically 3.0476 ± 5% (see data-sheet). In the aplication of Fig.12, using $R_{25} = 6.8k\Omega$ and $C_{17} = 1.8nF$, we obtain:

$$f_O = \frac{10^6}{3.0476 \times 6.8 \times 1.8} = 26.808kHz$$

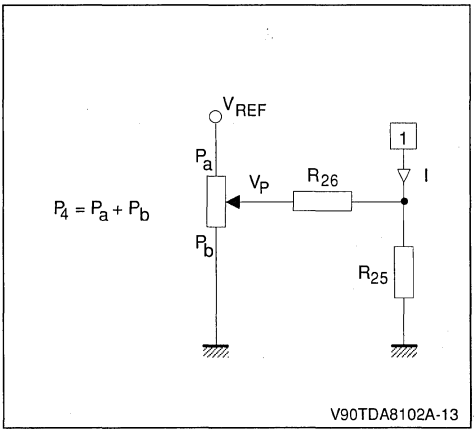
The maximum available current at Pin 1 is 1mA, so it must be $\frac{V_1}{R_{25}} \leq 1mA$.

By means of trimmer P_4 , it is possible to adjust the horizontal free running frequency, that changes accordingly with the following formula:

$$f_H = f_O \left\{ 1 - \frac{(V_p - V_1) / R_{26}}{V_1 / R_{25}} \right\}$$

where $0 \leq V_p \leq 8V$ is the voltage at the central point of the trimmer (see Fig.13).

Figure 13.



5.2 Pull-in range

This range is determined by the ability of the first comparator (φ 1) to correct the difference between the sync frequency and the free running frequency and it is set by R_{24} and R_{25}.

$$f_{pull-in} = f_O \frac{|V_3 - V_1| / R_{24}}{V_1 / R_{25}}$$

$|V_3 - V_1|$ is typically 2.5V, while $V_1 = 3.5V$.

This is the theoretical value calculated if the frequency adjustment is disconnected.

In the application inf Fig.12 we have:

$$f_{pull-in} = 26808 \frac{2.5}{3.5} \frac{6800}{56000} = \pm 2.3kHz$$

When the frequency adjustment is connected the pull-in range changes due to the fact that in parallel with R_{25} are connected $R_{26} + P_b$ (see Fig.13).

When the device is synchronized and perfectly tuned, $V_3 = V_1$ and the φ 1 will work in the best way.

C_{17}, on the contrary of R_{25}, is influential only for the free running frequency of the horizontal oscillator; it has no effect on the pull-in range, which doesn't change in percentage with respect to the free running frequency.

If you change the horizontal frequency changing R_{25} the pull-in range changes accordingly with the previous formula.

5.3 Internal sync. width

The internal sync. pulse is made by current generator (I_5) that charges an external capacitor at Pin 5 (C_{21}) up to the trigger threshold $V_5 = 6V$.

$$t_5 = \frac{C_{21} \times V_5}{I_5}$$

$t_5 = 1 / (12 \times f_O)$ is recommended.

5.4 Phase adjustment range

The voltage range accepted at Pin 10 is from 0.5V to 4.5V, so the resistor divider must be dimensioned to supply these values.

In our application we have :

$$V_{10\,min} \begin{cases} = \dfrac{V_{19}}{R_7 + P_3 + R_8} R_8 \\ = \dfrac{8}{39 + 47 + 5.1} 5.1 \\ = 0.447V \end{cases}$$

$$V_{10\,max} \begin{cases} = \dfrac{V_{19}}{R_7 + P_3 + R_8} (P_3 + R_8) \\ = \dfrac{8}{39 + 47 + 5.1} 52.1 \\ = 4.575V \end{cases}$$

5.5 Flyback input

The resistor in series at Pin 8 (R_{27}) must be dimensioned in order to have an input current included between 0.7mA and 2mA (typ 1mA), according with the following formula:

$$R_{27} = \frac{V_{fly} - 0.6V}{1mA}$$

6. VERTICAL SECTION

6.1 Frequency

The device is able to work form 30Hz to 120Hz.
The free running frequency is fixed by R_{21} and C_{16}.
The formula to calculate the free running frequency is the following:

$$f_v = \frac{I_C}{(V_{high} - V_{low}) \times C_{16}}$$

but

$$I_C = I = \frac{V_{12}}{R_{21}} \leq 0.5mA$$

then

$$f_v = \frac{V_{12}}{(V_{high} - V_{low}) \times C_{16} \times R_{21}}$$

where $V_{12} = 3.5V$, $V_{high} = 6.8V$ and $V_{low} = 2V$.
In the application proposed the free running frequency is:

$$f_v = \frac{3.5 \times 10^6}{(6.8 - 2) \times 220 \times 62} = 53.4Hz$$

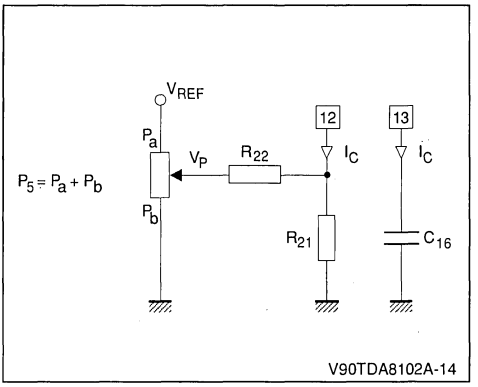
With the trimmer P_5 is possible to change the current that charges C_{16} and consequently to change the free running frequency.

The current in C_{16} due to this correction become:

$$I_C = \frac{V_{12}}{R_{21}} - \frac{V_P - V_{12}}{R_{22}}$$

where $0 \leq V_P \leq 8V$ is the voltage at the central point of the trimmer (see Fig.14).

Figure 14.



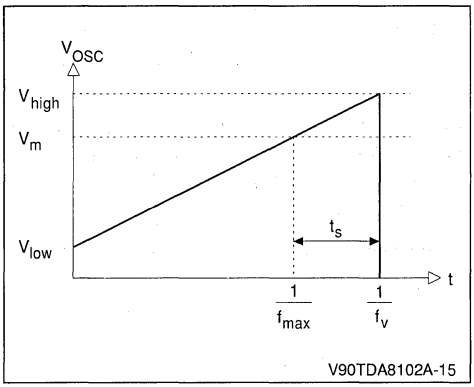
It is easy to substitute the new I_C in the formula in order to obtain the new free running frequency.

6.2 Pull-in range

The vertical pull-in range is fixed by internal thresholds.

With reference to figure 15 :

Figure 15.



we can write :

$f_{pull\text{ - }in} = f_{max} - f_v$

$$f_{max} = \frac{1}{t_v - t_s}$$

$$t_s = \frac{(V_{high} - V_m)}{(V_{high} - V_{low})} \times t_v = K_{14} \times t_v$$

the value of K_{14} is 0.333 (see data-sheet).

6.3 Amplitude adjustment range

The voltage range accepted at pin 16 is from 0.5V to 4.5V.

So the resistor divider must be dimensioned to supply these values.

In our application we have:

$$V_{16min} \begin{cases} = \dfrac{V_{19}}{R_5 + P_2 + R_6} R_6 \\ = \dfrac{8}{39 + 47 + 5.1} 5.1 \\ = 0.447V \end{cases}$$

$$V_{16max} \begin{cases} = \dfrac{V_{19}}{R_5 + P_2 + R_6} (P_2 + R_6) \\ = \dfrac{8}{39 + 47 + 5.1} 52.1 \\ = 4.575V \end{cases}$$

This system allows a vertical ramp amplitude variation of ± 20% around the nominal value; the value of amplitude of vertical ramp at Pin 15 can be determined with the following formula:

$$V_{15\,pp} = [K_{16}(V_{16} - 2.5) + K_{15}]\, V_{13pp}$$

Where K_{15} is typically 1 and K_{16} is typically 0.1 (as you can see on the data-sheet).

6.4 Vertical DC reference

The average value of the vertical ramp at Pin 15 is the half of V_{19}, then with a resistive divider this DC voltage can be used as reference for the vertical booster as shown in Fig.12.

For a best noise immunity we suggest to filter V_{19} with an electrolytic capacitor.

6.5 Linearity correction

The "S" correction is performed with the new concept described in chapter 3.8.

The adjustment is obtained varying the DC voltage at Pin 17 from 1.5 to 4.5V, then the resistor divider (R3, P1 and R4) must be dimensioned for obtaining this range of values.

In our application we have:

$$V_{17min} \begin{cases} = \dfrac{V_{19}}{R_3 + P_1 + R_4} R_4 \\ = \dfrac{8}{51 + 47 + 22} 22 \\ = 1.466V \end{cases}$$

$$V_{17max} \left| \begin{array}{l} = \dfrac{V_{19}}{R_3 + P_1 + R_4} (P_1 + R_4) \\ = \dfrac{8}{51 + 47 + 22} 69 \\ = 4.6V \end{array} \right.$$

The "S" correction is not performed when the voltage at Pin 17 is 1.5V, while it is maximum when the Pin 17 voltage is 4.5V.
You can verify this using the following formula:

$$V_{18pp} = K_{18} (V_{17} - 1.5)$$

where K_{18} is typically 1.
If the CRT requires a higher "S" correction, it is possible to obtain it reducing the value of R_{20}; however take care that C_{15} in series with R_{20} is a high-pass filter with the purpose to cut only the D_C.
In our application we have:

$$f_t \left| \begin{array}{l} = \dfrac{1}{6.28 \times R_{20} \times C_{15}} \\ = \dfrac{10^3}{6.28 \times 150 \times 1} \\ = 1.06 \text{ Hz} \end{array} \right.$$

The "C" correction is obtained with a resistor in series to a capacitor connected between Pin 15 and the central point of the vertical DC feedback of vertical booster (R_{19} and C_{14}).
The value of R_{19} is strictly dependent on CRT used.

7. LAY-OUT SUGGESTIONS

It is necessary to take care not to connect the horizontal output ground (Pin 6) directly to Pin 11, to avoid horizontal interference on vertical stages.
The 15nF capacitors connected on Pins 10, 16 and 17 have the only aim to filter the DC control voltage against horizontal noise, so they must be connected as close as possible to the above mentioned pins.

8. ADJUSTING PROCEDURE

Here following it is shortly described the procedure to adjust horizontal and vertical frequencies, vertical amplitude, linearity and horizontal phase.
Before starting these operations take care that the horizontal and vertical synchronization pulses are properly applied to the device inputs.

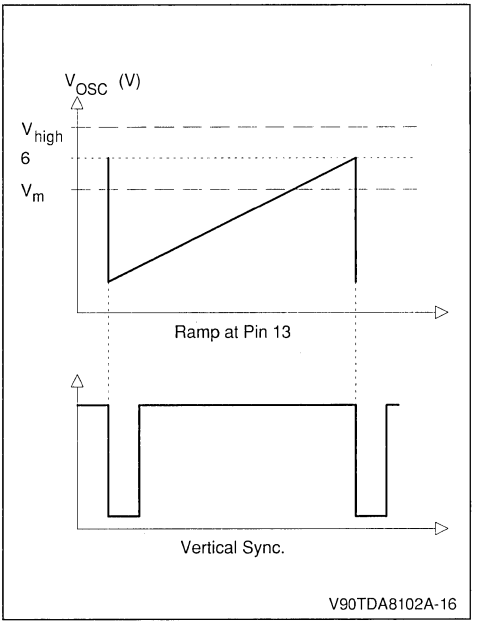
8.1 Horizontal frequency

Adjust P_4 in order to obtain $V_3 = V_1$; in this way the horizontal synchronisation is perfect, and the pull-in range is maximum in both directions.

8.2 Vertical frequency

Adjust the vertical ramp amplitude using P_5 in order to have $4V_{pp}$; in this way the vertical frequency value is in the middle of the synchronization range; as shown in Fig.16.

Figure 16.



This operation is important because some internal circuits are dimensioned for a $4V_{pp}$ ramp.

8.3 Vertical amplitude and horizontal phase

Looking at the display correct P_2 for the right vertical amplitude and adjust P_3 in order to have the correct horizontal phase.

8.4 Vertical linearity

If the vertical ramp at Pin 13 is correctly set the central point of the "M" waveform at Pin 18 will be at the center of the scan; in other case, using P_5, lead the central point of "M" in correspondence of the scan center (see Fig.17).

where : t_S = scan time
$t_V = 1/f_V$ = vertical period
t_{SC} = scan centre
t_C = period centre

In this way the S linearity correction has a uniform behaviour on the top and bottom sides of the CRT. Now looking at the display, adjust P_1 to obtain a right S correction and select R_{19} value to optimise the C correction.

Figure 17.

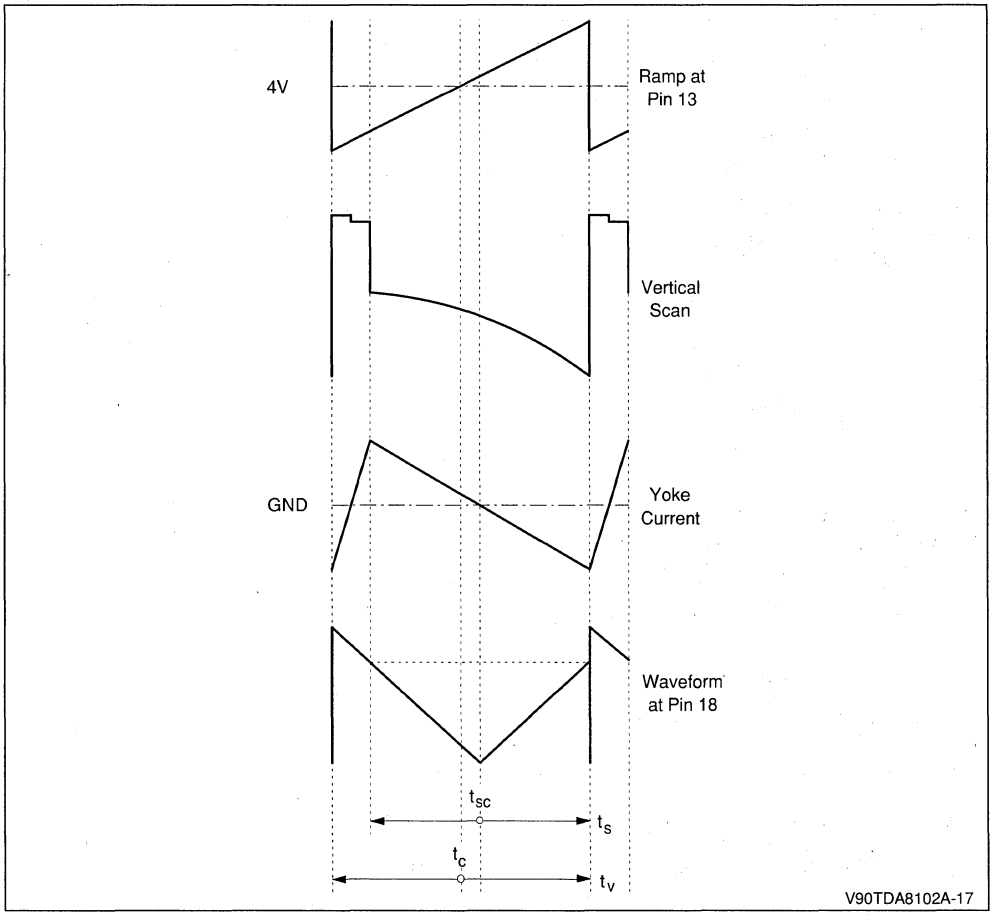
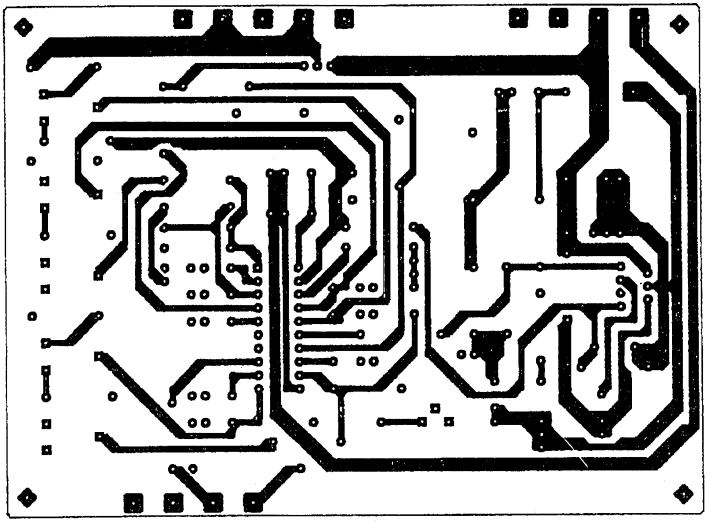
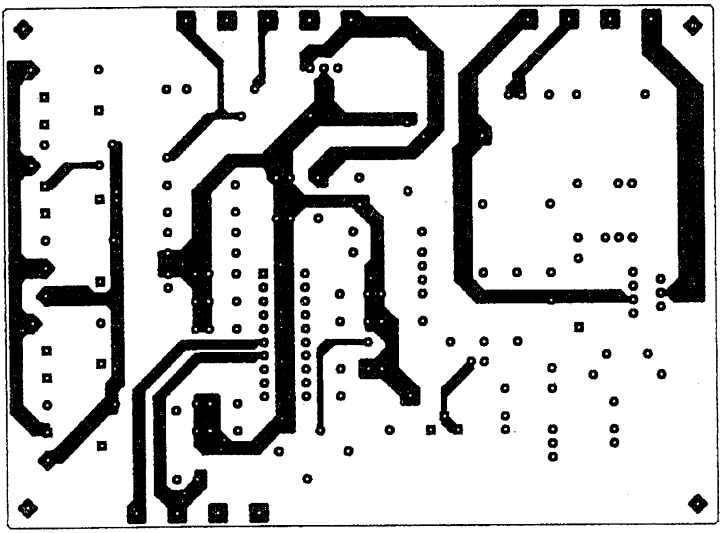


Figure 18 : Solder Side.



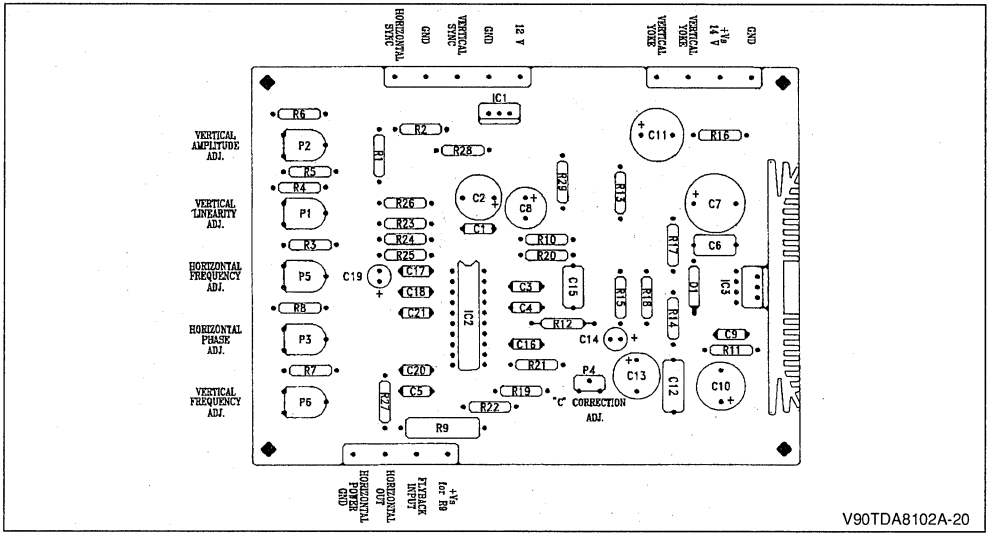
V90TDA8102A-18

Figure 19 : Component Side.



V90TDA8102A-19

Figure 20 : PCB Layout.



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9. COMPONENT LIST

Component	Value	Component	Value	Component	Value
R_1, R_2, R_{23}	3.3kΩ	R_{20}	150kΩ	C_{10}	220µF / 25V
R_3	51kΩ	R_{21}	62kΩ	C_{11}	2200µF / 16V
R_4, R_{10}, R_{11}, R_{26}	22kΩ	R_{22}	220kΩ	C_{12}, C_{16}	220nF
R_5, R_7	39kΩ	R_{24}	56kΩ	C_{14}	10µF / 63V
R_6, R_8	5.1kΩ	R_{25}	6.8kΩ	C_{15}	1µF
R_9	82Ω / 2W	R_{27}	100kΩ	C_{17}	1.8nF
R_{12}	10kΩ	R_{28}, R_{29}	2.2kΩ	C_{19}	2.2µF / 63V
R_{13}	120Ω	P_1, P_2, P_3, P_5, P_6	47kΩ hor.	C_{20}	22nF
R_{14}	1.5Ω	P_4	47kΩ ver.	C_{21}	220pF
R_{15}	1.5kΩ	C_1, C_6, C_9	100nF	D_1	1N4001
R_{16}	1Ω	C_2, C_{13}	470µF / 16V	IC_1	L7812
R_{17}	2.7kΩ	C_3, C_4, C_5, C_{18}	15nF	IC_2	TDA8102A
R_{18}	1.2kΩ	C_7	1000µF / 25V	IC_3	TDA8172
R_{19}	33kΩ	C_8	100µF / 16V		

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA5101A - RGB HIGH VOLTAGE VIDEO AMPLIFLIER BASIC OPERATION AND APPLICATIONS

By: Ch. MATHELET

SUMMARY

The aim of this Application Note is to describe the basic operation of the TEA5101A video amplifier and to provide the user with basic hints for the best utilization of the device and the realisation of high performance applications. Application examples are also provided to assist the designer in the maximum exploitation of the circuit.

GENERAL

The control of state-of-the-art color cathode ray tubes requires high performance video amplifiers which must satisfy both tube and video processor characteristics.

When considering tube characteristics (see fig 13-14 on page 14),we note that a 130V cutoff voltage is necessary to ensure a 5mA peak current.However 150V is a more appropriate value if the saturation effect of the amplifier is to be taken into account. As the dispersion range of the three guns is ± 12%, the cutoff voltage should be adjustable from 130V to 170V. The G2 voltage, from 700 to 1500V allows overall adjustment of the cutoff voltage for similar tube types.

A 200V supply voltage of the video amplifier is necessary to achieve a correct blanking operation. In addition, the video amplifier should have an output saturation voltage drop lower than 15V, as a drive voltage of 130V (resp. 115V) is necessary to obtain a beam current of 4 mA for a gun which has a cutoff point of 170V (resp. 130V).

Note : For all the calculations discussed above, the G1 voltage is assumed to be 0V.

The video processor characteristics must also be considered. As it generally delivers an output voltage of 2 to 3V, the video amplifier must provide a closed loop DC gain of approximately 40.

The video amplifier dynamic performances must also meet the requirements of good definition even with RGB input signals (teletext,home computer...), e.g. 1mm resolution on a 54cm CRT width scanned in 52µs. Consequently, a slew rate better than 2000V/µs, i.e. rise and fall times lower than 50ns, is needed. In addition, transition times must be the same for the three channels so as to avoid coloured transitions when displaying white characters. The bandwidth of a video amplifier satisfying all these requirements must be at least 7MHz for high level signals and 10MHz for small signals.

One major feature of a video amplifier is its capability to monitor the beam current of the tube. This function is necessary with modern video processors:

- for automatic adjustment of cutoff and also, where required,video gain in order to improve the long term performances by compensation for aging effects through the life of the CRT. This adjustment can be done either sequentially (gun after gun) or in a parallel mode.
- for limiting the average beam current

A video amplifier must also be flashover protected and provide high crosstalk performances. Crosstalk effects are mainly caused by parasitic capacitors and thus increase with the signal frequency. A crosstalk level of -20dB at 5MHz is generally acceptable.

Table 1 summarizes the main features of a high performance video amplifier.

The SGS-THOMSON Microelectronics TEA5101A is a high performance and large bandwidth 3 channel video amplifier which fulfills all the criteria discussed above. Designed in a 250V DMOS bipolar technology, it operates with a 200V power supply and can deliver 100V peak-to-peak output signals with rise and fall times equal to 50ns.

The 5101A features a large signal bandwidth of 8MHz, which can be extended to 10MHz for small signals (50 Vpp).

Each channel incorporates a PMOS transistor to monitor the beam current. The circuit provides internal protection against electrostatic discharges and high voltage CRT discharges.

The best utilization of the TEA 5101A high performance features such as dynamic characteristics, crosstalk,or flashover protection requires optimized application implementation. This aspect will be discussed in the fourth part of this document.

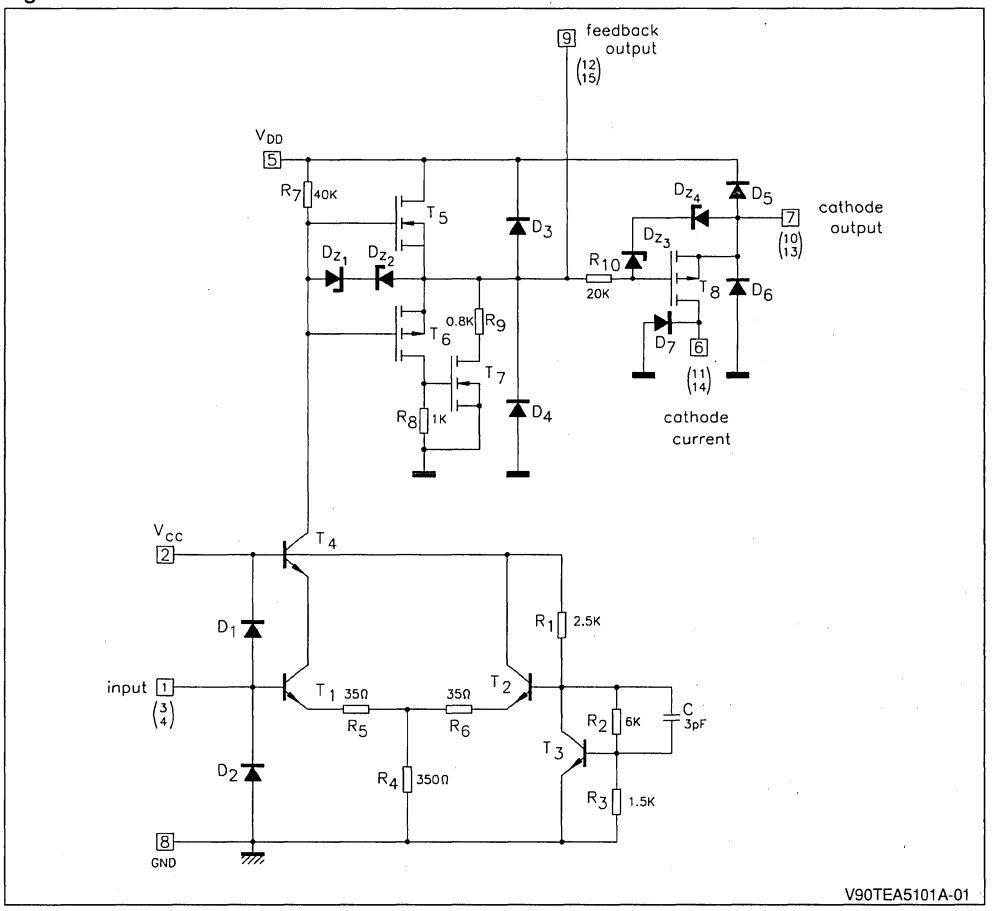
Table 1: Main features of a high performance video amplifier.

· Maximum Supply Voltage	220V
· Output voltage swing "Average"	100V
· Output voltage swing "Peak"	130V
· Low level saturation (refered to VG1)	15V
· Closed loop gain	40
· Transition time	50ns
· Large signal bandwidth	7MHz
· Small signal bandwidth	10MHz
· Beam current monitoring	
· Flash over protection	
· Crosstalk at 5 MHz	-20dB

I - DESCRIPTION

The complete schematic diagram of one channel of the TEA5101A is shown in fig 1.

Figure 1.



I.1 INPUT STAGE

The differential input stage consists of the transistor T_1 and T_2 and the resistors R_4,R_5 and R_6.

This stage is biased by a voltage source T_3,R_1,R_2 and R_3.

$$V_B(T_1) = (1 + \frac{R_2}{R_3}) \times V_B(T_3) \cong 3.8V$$

Each amplifier is biased by a separate voltage source in order to reduce internal crosstalk. The load of the input stage is composed of the transistor T_4 (cascode configuration) and the resistor R_7. The cascode configuration has been chosen so as to reduce the Miller input capacitance. The voltage gain of the input stage is fixed by R_7 and the emitter degeneration resistors R_5,R_6,and the T_1,T_2 internal emitter resistances. The voltage gain is approximately 50dB.

Using a bipolar transistor T_4 and a polysilicon resistor R_7 gives rise to a very low parasitic capacitance at the output of this stage (about 1.5pF). Hence the rise and fall times are about 50ns for a 100V peak-to-peak signal (between 50V and 150V).

I.2 OUTPUT STAGE

The output stage is a quasi-complementary class B push-pull stage. This design ensures a symetrical load of the first stage for both rising and falling signals. The positive output stage is made of the DMOS transistor T_5,and the negative output stage is made of the transistors PMOS T_6 and DMOS T_7. The compound configuration T_6-T_7 is equivalent to a single PMOS. A single PMOS transistor capable of sinking the total current would have been too large.

By virtue of the symetrical drive properties of the output stage the rise and fall times are equal (50ns for 100V DC output voltage).

I.3 BEAM CURRENT MONITORING

This function is performed by the PMOS transistor T_8 in source follower configuration. The voltage on the source (cathode output) follows the gate voltage (feedback output). The beam current is absorbed via T_8 . On the drain of T_8, this current will be monitored by the videoprocessor.

I.4 PROTECTION CIRCUITS

I.4.1. MOS protection

Four zener diodes $DZ_{(1-4)}$ are connected between gate and source of each MOS in order to prevent the voltage from reaching the breakdown voltage.Hence the V_{GS} voltage is internally limited to ± 15V.

I.4.2. Protection against electrostatic discharges

All the input/output pins of the TEA5101A are protected by the diodes D_1-D_7 which limit the overvoltage due to ESD.

I.4.3. Flashover protection

A high voltage and high current diode D_5 is connected between each output and the high voltage power supply. During a flash, most of the current is generally absorbed by the spark gap connected to the CRT socket. The remaining current is absorbed by the high voltage decoupling capacitor through the diode D_5. Hence the cathode voltage is clamped to the supply voltage and the output voltage does not exceed this value.

II - FUNCTIONAL DESCRIPTION

The schematic diagram of one TEA5101A channel with its associated external components is shown in fig.2

II.1 VOLTAGE AMPLIFIER

II.1.1. Bias conditions $V_{in} = V_{ref}$

The bias point is fixed by the feedback resistor R_f,the bias resistor R_p, and by the internal reference voltage when $V_{in} = V_{ref}$.

If V_O is the output voltage (pin 9) :

$$V_O = (1 + \frac{R_f}{R_p}) \times V_{ref} \qquad (1)$$

In this state T_1 and T_2 are conducting. A current flows in R_7 and T_4 soT_5 is on. The T_5 drain current is fed to the amplifier input through the feedback resistor. The current in R_7 is:

$$I(R_7) = \frac{V_{DD} - V_O - V_{GS(T_5)}}{R_7} \cong \frac{V_{DD} - V_O}{R_7}$$

and the current in T_5 and R_f is :

$$I(T_5) = \frac{V_O - V_{ref}}{R_f} \cong \frac{V_O}{R_f}$$

Thus the total current absorbed by each channel of the TEA5101A is :

$$\frac{V_{DD}}{R_7} + V_O \times (\frac{1}{R_f} - \frac{1}{R_7})$$

The cathode (pin 7) output voltage is:

$$V_O + V_{GS(T_8)} = V_O$$

The beam current is absorbed by T_8 and R_m. The voltage developed across R_m by this current is fed to the videoprocessor in order to monitor the beam current.

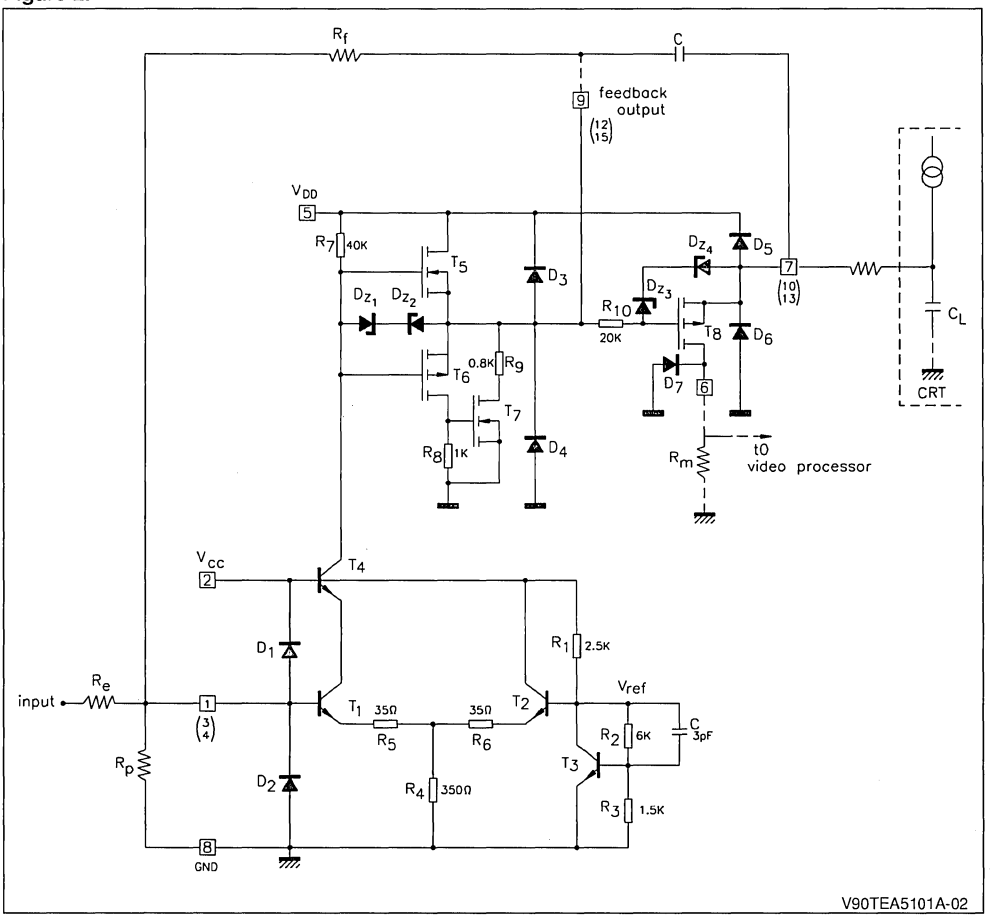
II.1.2. Dynamic operation

The TEA5101A operates as a closed loop amplifier, with its voltage gain fixed by the resistors R_f and R_e.

Since the open loop gain A is not infinite, the resistor R_p and the input impedance R_{in} must be considered.Hence the voltage gain is

$$G = -\frac{R_f}{R_e} \times \frac{1}{1 + \frac{1}{A}(1 + \frac{R_f}{R_p \,//\, R_e \,//\, R_{in}})} \qquad (2)$$

Figure 2.



II.1.2.1. Input voltage $V_{in} < V_{ref}$ (black picture)

In this case the current flowing in R_7 and T_1 decreases whilst the collector voltage of T_4 and the output voltage both increase. In the extreme case, $I(T_1) = I(R_7) = 0$ and $V_O = V_{DD} - V_{GS}(T_5)$

In order to charge the tube capacitor the voltage is fed to the cathode output in two ways:

- through the PMOS (with a VGS difference) for the low frequency part
- through the capacitor C for the high frequency part (output signal leading edge)

To correctly transmit the rising edge, the value of the capacitor C must be high compared to C_L.

With the current values used (C = 1nF, C_L = 10pF), the attenuation is very small (0.99)

II.1.2.2. Input voltage $V_{in} > V_{ref}$ (white picture)

In this case,the current in R_7 and T_1 increases with an accompanying drop of T_4's collector voltage until T_1 and T_4 are saturated. At this point:

$V_O \cong V_C(T_4) \cong V_{CC}$

During a high to low transition (i.e. black-white picture), the beam current is absorbed in two ways:

- through the capacitor C and the compound PMOS T_6-T_7 for the high frequency part (falling edge)
- through the PMOS T_8 and the resistor R_m for the low frequency part.

II.2 BEAM CURRENT MONITORING

II.2.1. Stationary state

The beam current monitoring is performed by the PMOS T_8 and the resistor R_m. When measuring low currents (leakage, quasi cutoff),the R_m value is generally high. When measuring high currents (drive, average or peak beam current),R_m is generally bypassed by a lower impedance.

It should be noted that the current supplied by the three guns flows through this resistor.Hence,with too large a value for the resistor R_m,the cathode voltage of the tubes will become too high for the required operating current values.This is a fundamental difference between the TEA5101A and discrete video amps. In discrete video amps, the current monitoring transistor is a high voltage PNP bipolar which may saturate. In this case the beam current can flow through the transistor base and it is no longer monitored by the video processor. This effect does not occur with the TEA 5101A.

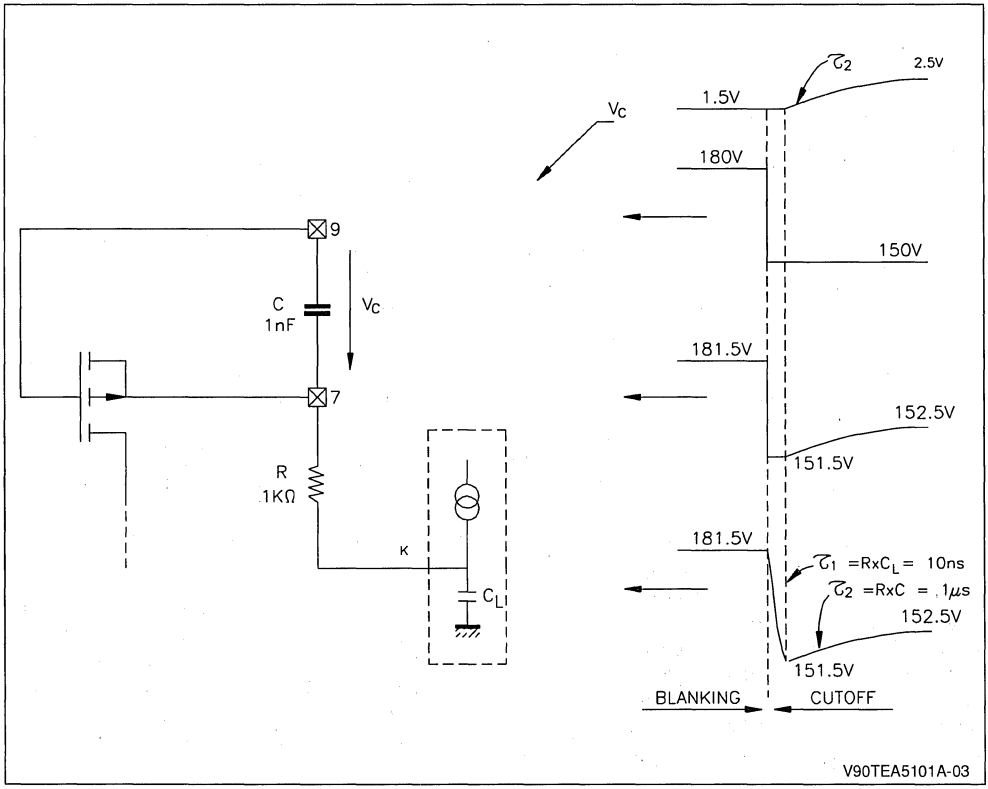
II.2.2. Transient phase : low current measurements

The cut-off adjustment sequence is generally as follows:

In a first step, the cathode is set to a high voltage (180V) in order to blank the CRT and to measure the leakage current. In a second step, the tube is slighly switched on to measure a very low current (quasi cut-off current). This operation is performed by setting the cathode voltage to about 150V and adjusting it until the proper current is obtained. The maximum time available to do this operation is generally about 52µs.

Fig.3 shows the simplified diagram of the TEA5101A output, the voltages during the different steps,and the stationary state the system must reach for correct adjustment.

Figure 3.



During the blanking phase, the tube is switched off, the PMOS is switched off and its V_{GS} voltage is equal to the pinch-off voltage (about 1.5V). The voltages at the different nodes are shown in figure 3 (V(9) = 180V, V(k) = 181.5V). The falling edge of the cutoff pulse is instantaneously transmitted by the capacitor C. When the stationary state is reached, the cathode voltage will be 152.5V if the voltage on pin 9 is 150V, as the VGS voltage of the conducting PMOS is about 2.5V.

We can see that the voltage on C must increase by an amount of $\Delta Vc = 1V$. This charge is furnished by the tube capacitor which is discharged by an amount of $\Delta VC_L = 29V$ with a time constant equal to R x C_L (10 ns). By considering the energy balance, we can calculate the maximum charge $\Delta Vmax$ that C_L can furnished to C

$$\Delta V_{max} = \sqrt{\frac{C_L}{C}} \times \Delta V_{CL} \cong 3V$$

Since this voltage is greater than ΔV_C, the capacitor C can be charged and the stationary state is reached without any contribution being required from the tube current,i.e. the whole tube current can flow through the PMOS and the adjustment can be performed correctly.

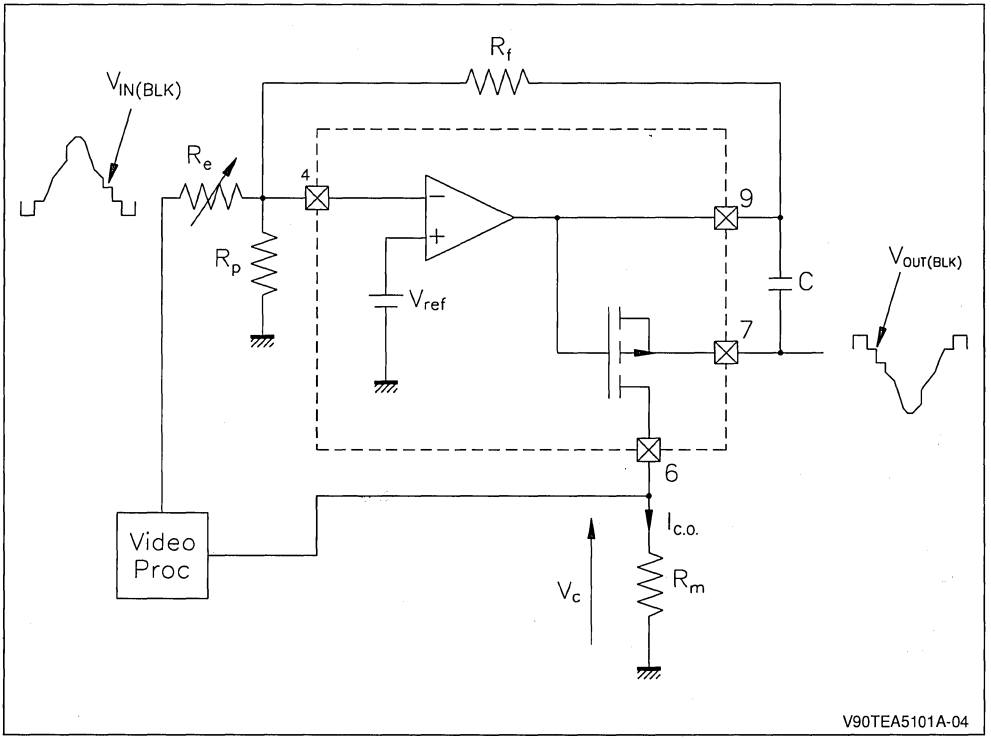
Considering higher voltage and beam current swings, the margin is greater because:

- the voltage swing across the tube capacitor is greater
- the tube current is higher and the picture is not disturbed even if part of the beam current is used to charge the capacitor C.

III - EXTERNAL COMPONENTS CALCULATION

The implementation of the TEA5101A in an application requires the determination of external component values. These components are R_f, R_e, R_p and R_m (see fig.4). The dissipated power in the IC and in the feedback resistor R_f must also be calculated in order to correctly choose the power ratings of the heatsink and resistors.

Figure 4.



III.1 COMPONENTS VALUE CALCULATION

From equations 1 and 2 in section II-1, both the value of the DC output voltage and the voltage gain depend directly on the resistor R_f. Hence R_f must be determined first before calculating the value of R_e and R_p in order to obtain the correct gain and DC output voltage.

III.1.1. Feedback resistor R_f

The value of R_f must be as low as possible in order to obtain the optimum dynamic performance from the TEA5101A (see section IV-1). A typical value of R_f is 39 kΩ.

III.1.2. Input resistor Re

The voltage gain is calculated from the following formula (see section II-1):

$$G = -\frac{R_f}{R_e} \frac{1}{1+\frac{1}{A}(1+\frac{R_f}{R_p \,//\, R_e \,//\, R_{in}})}$$

Since the open loop gain A is high enough (50dB), we can approximate the calculation:

$$G @ -\frac{R_f}{R_e}$$

where R_e is generally implemented as a variable value for channel gain adjustment.

If the gain adjustment range G_{min}, G_{max} is known:

$$R_{e\,min} = \frac{R_f}{G_{max}} \text{ and } R_{e\,max} = \frac{R_f}{G_{min}}$$

With G_{min} = 15 and G_{max} = 80 :

$R_{e\,min}$ = 470Ω
$R_{e\,max}$ = 2.6kΩ

R_e will be made of a 2.2kΩ potentiometer and 470Ω fixed resistor.

III.1.3. Bias resistor R_p

R_p must be chosen in such a way that the black level output voltage $V_{OUT(BLK)}$ is equal to the cutoff voltage, which is a characteristic of the tube currently used, when the DC black level input voltage $V_{IN(BLK)}$ is the mean value of the adjustment range of the video processor. This is the optimum condition to ensure a correct adjustment during the lifetime of the tube. R_p can be calculated by considering the TEA5101A as an operational amplifier and applying the usual formula :

$$R_p = \frac{V_{ref}}{\frac{V_{out\,(BLK)} - V_{ref}}{R_f} + \frac{V_{in\,(BLK)} - V_{ref}}{R_e}}$$

- If $V_{in(BLK)} = V_{ref}$ $\quad R_p = \frac{V_{ref}}{V_{out\,(BLK)} - V_{ref}} \times R_f$

For a 150V black level :

R_p = 1kΩ with R_f = 39kΩ

- If $V_{in\,(BLK)} \neq V_{ref}$:

R_p = 1.2kΩ with $V_{in\,(BLK)}$ = 2.7V, R_f = 39kΩ, R_e = 1.5kΩ

Or

R_p = 680Ω with $V_{in\,(BLK)}$ = 6.7V, R_f= 39kΩ, R_e = 1.5kΩ

for a 150V black level

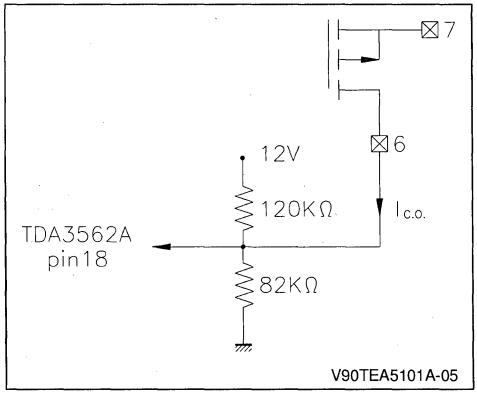
III.1.4. Current measurement resistor R_m

R_m must be determined by taking into account the quasi cutoff current I_{co} and the input voltage V_C of the video processor.

$$R_m = \frac{V_C}{I_{CO}}$$

- With the videoprocessor TEA5031D (V_C = 2V) : R_m = 120kΩ with I_{CO} = 16µA
- With the videoprocessor TDA3562A (V_C = 0.5V) which requires a DC biased input "Black current stabilization" (pin 18), the schematic diagram is the following :

Figure 5.



The DC bias is $12 \times \frac{82}{120+82} = 5V$

The quasi cutoff current is

$0.5 (\frac{1}{120} + \frac{1}{82}) \times 1 \times 10^{-3} = 10\mu A$

III.2 DISSIPATED POWER IN EXTERNAL COMPONENTS

The only components dissipating power are the TEA5101A and the feedback resistor. The dissipated power has a constant static component and a dynamic component which increases with frequency. The theoretical calculation is not sufficiently accurate to determine the correct dissipated power. The best way consists of measuring the power in different configurations of the circuit: steady state (no input), sinusoidal input,and in situ (in a TV set with a video input signal). The measurement method will be described first and then the results and calculations will be discussed.

III.2.1. Measurement method

The dissipated power can be determined by measuring the average supply current I_{DD} (principally high voltage supply current V_{DD}) and by subtracting the power dissipated in the external components from the calculated power delivered by this supply voltage.

The power delivered by the high voltage power supply is : $P = V_{DD} \times I_{DD}$

The power dissipated in the external components (principally the feedback resistor R_f) is:

- for the static part: $P_{SR} = \frac{3 \times V^2_{OUT\ (AVG)}}{R_f}$

- for the dynamic part: $P_{DR} = \frac{3 \times V^2_{OUT\ (RMS)}}{R_f}$

When the IC is driven by a sinusoidal signal (capacitive drive),the measurement and calculation are straightforward:

$V_{OUT}(AVG) = V_{OUT}(DC)$

$V_{OUT}(RMS) = \frac{V_{OUT\ (peak\ to\ peak)}}{2 \times \sqrt{2}}$

With V_{OUT} (DC) = 100V and
V_{OUT} (peak to peak) = 100V and $R_f = 39k\Omega$

$P_{SR} = 0.8W$
$P_{DR} = 0.1W$

Measurements are more difficult to carry out when the IC is working in a TV set. $V_{OUT}(AVG)$ can be measured with an oscilloscope (difference of level between AC and DC coupling) and V_{OUT} (RMS) can be measured by connecting an RMS voltmeter to the feedback resistor. In this case we have the following results (see section 2.2.3):

V_{OUT} (AVG) = 130V and P_{SR} = 1.3W

V_{OUT} (RMS) = 32V and P_{DR} = 80mW

In each case, the term P_{DR} can be neglected as a reasonable approximation.Hence, the power dissipated by the IC will be:

$P_i = V_{DD} \times I_{DD} - \frac{3V^2_{OUT\ (AVG)}}{R_f}$

and the power dissipated in R_f will be :

$P_r = \frac{V^2_{OUT\ (AVG)}}{R_f}$

III.2.2. Results

III.2.2.1. Static power

Table 2 shows the measured values of I_{DD} and the calculated power for three values of Vout and for V_{DD} = 200V

Table 2.

V_{OUT} (V)	I_{DD} (mA)	P_i (W)	P_r (W)
50	16	3	0.065
100	15	2.2	0.25
150	14.6	1.2	0.6

We can see that the static power dissipated in the IC decreases with V_{OUT} increasing, but obviously the power dissipated by R_f increases as V_{OUT} increases.

III.2.2.2. Measurement with sinusoidal input

Table 3 summarizes the results obtained from practical measurements as functions of V_{OUT}(DC) and of the frequency (the three channels are driven simultaneously).

Table 3.

V_{OUT} (V)	I_{DD} 1MHz (mA)	I_{DD} 7MHz (mA)	V_{OUT} (PP) 1MHz (V)	V_{OUT} (PP) 7MHz (V)	P_i 1MHz (W)	P_i 7MHz (W)	P_r (W)
50	20.7	44.6	66	50	3.9	8.7	0.065
100	20	59.5	100	80	3	11	0.25
150	18	45	100	67	1.7	8.2	0.6

We can see that when driving the IC with a HF sinusoidal signal, care must be taken to avoid excessive temperature increase.

III.2.2.3. Measurement in a TV set

We have determined the worst cases of dissipation in a TV set. These trials have been carried out on one particular TV set, and may not be representative for all TV sets. In this particular TV set, the worst cases of dissipation occur with noise signal (from HF tuner) and with a multiburst pattern (0.8 to 4.8MHz) in RGB mode.

Table 4 summarizes the results in these two cases when the brightness control is set to min and max value (the contrast control is set to max).

Table 4.

	V_{OUT} (AVG) (V)	I_{DD} (mA)	V_{DD} (V)	P_i (W)	P_r (W)
Bright.max Noise	148	22.2	218	3.15	O.56
Bright.min	188	23.3	224	2.5	0.9
Bright.max Multiburst	131	23.6	213	3.7	0.44
Bright.min	158	22	221	2.9	0.64

III.2.3. Design of heatsink and external components

III.2.3.1. Heatsink

As discussed above, the power dissipated in the IC in a TV set can reach about 4W. In this case, a 12°C/W heatsink seems to be sufficient. Such a heatsink will give $T_j = 115°C$ for $T_{room} = 60°C$.

The resulting margin guarantees correct reliability.

III.2.3.2. Feedback resistors

1 Watt type feedback resistors must be used, as they may need to dissipate 0.9W when the TV set is working and up to 1W when the TV is blanked (V_{OUT} = 200V), for example when the security of the scanning processor is activated.

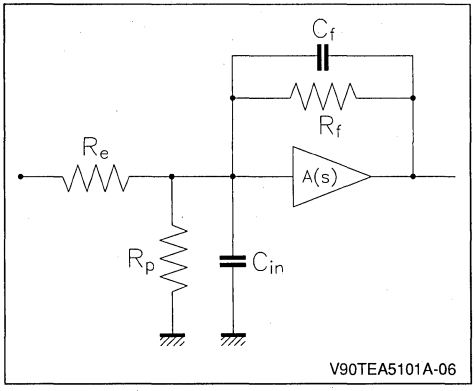
IV - APPLICATION HINTS

IV.1 DYNAMIC PERFORMANCES

Figure 6 shows the simplified schematic diagram of the TEA5101A in AC mode.

C_f is the parasitic capacitor between the input and the output.

Figure 6.



C_{in} is the parasitic capacitor between the input and ground. The voltage gain versus frequency can be deduced from the formula (2) in chapter II section 1.2 :

$$G(s) = -\frac{R_f}{R_e\,(1 + R_f\,C_f\,s)} \times \frac{1}{1 + \frac{1}{A(s)}\left(1 + \frac{R_f}{R_{eq}}\,\frac{1 + R_{eq}\,C_{in}\,s}{1 + R_f\,C_f\,s}\right)}$$

with $R_{eq}=R_p//R_e//R_{in}$ and A(s) open loop gain.

A(s) is a second order function such as $\frac{AO}{1 + bs + as^2}$

with $a = 9 \times 10^{-16}\ s^2$

$b = 60 \times 10^{-9}\ s$

$AO = 400$

Assuming $R_{eq} \times C_{in} = R_f \times C_f$, we find:

$$G(s) = -\frac{R_f}{R_e\,(1 + R_f C_f s)} \times \frac{1}{1 + \frac{B}{AO}} \times \frac{1}{1 + \frac{B}{AO+B} bs + \frac{B}{AO+B} as^2}$$

with $B = 1 + \frac{R_f}{R_{eq}}$

We see that the closed loop amplifier is equivalent to a combination of a second order circuit and a first order one. The latter comprises the feedback resistor and the parasitic capacitor between input and output. With the current values

$R_f = 39k\Omega$ $C_f = 0.5pF$

$R_e = 2k\Omega$ $C_{in} = 15pF$

$R_{in} = 14k\Omega$

$R_p = 1.2k\Omega$

we have

$R_{eq} \times C_{in} = 10ns$

$R_f \times C_f = 20ns$

$B = 56$

The second order circuit characteristics are :

Natural frequency:

$$F_n = \frac{1}{2 \times \pi \times a} \times \frac{AO + B}{B} = 15MHz$$

damping factor :

$$z = \frac{b}{2 \times a} \times \frac{B}{AO + B} = 0.35$$

The cut off frequency of the first order circuit is :

$$f_C = \frac{1}{2 \times \pi\ R_f \times C_f} = 8MHz$$

The amplifier response is thus the combination of the responses of these two circuits. The contribution of the parasitic capacitor C_f to the frequency response is very important. If the value of C_f is too high, the contribution of the first order circuit will be of overriding importance and the resulting bandwidth of the amplifier will be too small. If the value of C_f is too low, the response curve will have a peak (due to the second order circuit). A "ringing" effect will be present on pulse-type signals and an instability and oscillation can occur at some frequencies.

This capacitor is generally too high. It consists of:

- the self parasitic capacitor of the feedback resistor
- the parasitic capacitor due to the PCB layout.

Practically,the best bandwidth performances are achieved by:

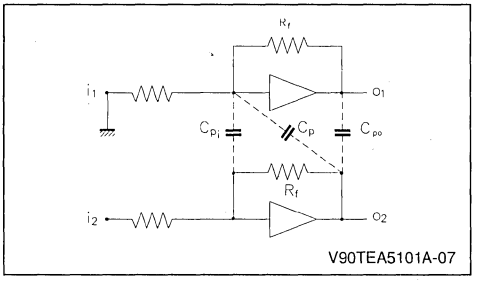
- the smallest input-output capacitor and the smallest capacitor between an input and ground
- using a feedback resistor with the smallest possible value but large enough to yield a sufficiently high gain.
- using a feedback resistor with small parasitic capacitance (typ 0.2pF). Some resistors have 0.5 or 0.8 pF parasitic capacitor.

The parasitic capacitors discussed above are usually the ones which need to be taken into account. However any other parasitic capacitor or inductor can modify the frequency response. For instance,a too large capacitor value between the feedback output and ground can create a dominant pole and cause a potential risk of oscillation .

IV.2 CROSSTALK

Figure 7 shows the different parasitic links inducing crosstalk.

Figure 7.



The crosstalk can be caused by:

- parasitic coupling between the inputs (C_{pi})
- parasitic coupling between the outputs (C_{po})
- parasitic coupling between an output and a near input of another channel (C_p).

Parasitic coupling may be capacitive or be caused by HF radiations.

The third type of parasitic coupling is predominant since it involves the addition by feedback at relatively high level(output) signals to relatively low level (input) signals. For example, a 0.1pF C_p parasitic capacitor between an output and the input of another channel will act as a differenciator with the feedback resistor $R_f = 39K\Omega$.

The transfer function of this integrator will be $\mathbf{R_f \times C_p \times s}$ (0.2j at 8MHz) and thus the crosstalk will be -14dB at 8MHz. The parasitic coupling between inputs and outputs must be minimized to achieve an acceptable crosstalk (-20dB at 5MHz). This can be done by crossing only the input wires and separating the input and output leads. High voltage components and wires must be laid out as far as possible from small signal wires,even if this results in a larger circuit board.

HF radiations from the feedback resistor must not induced a voltage signal at the input of another channel. This can be achieved by:

- spacing out the feed back resistors
- mounting these resistors in the same direction and strictly aligned one under another.
- mounting these resistors 1cm above the PC board
- using ground connections to insulate the input wires

IV.3 FLASHOVER PROTECTION

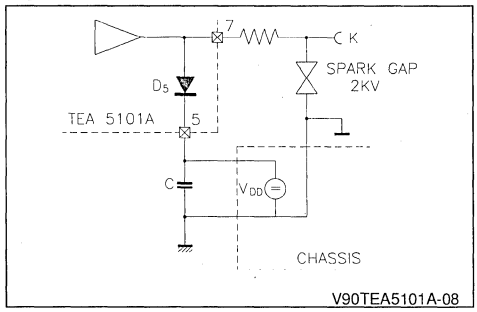
A picture tube has generally several high voltage discharges in its lifetime. This is due to the fact that the vacuum is not perfect coupled with the presence of metallic particles evaporated from the electrodes.Hence, short circuits (very brief fortunately) can occur between two electrodes,one of which is usually the anode (at EHT potential). An overvoltage can be induced on the cathodes or on the supplies even if a flash occurs on an electrode other than a cathode, because of the possibility of flashes in series or overvoltages due to inductive links on the video board or on the chassis. These overvoltages can destroy an IC particularly the video amplifier which is the most vulnerable since it is directly connected to the tube.

The tube manufacturers have made much progress in technology in order to reduce the frequency of flashes and their associated energy (increased quality of vacuum, internal resistance for "soft flash" tubes). Nevertheless, some protection measures are suggested by the tube manufacturers:

- connect spark gaps on each electrode (1 to 3kV or 12kV for focus)
- connect the spark gaps to a separated ground directly connected to the chassis ground by a non inductive link
- connect the cathodes or grids by protective resistors.These resistors must be able to withstand 12kV (20kV for focus)instantaneous voltages without breakdown and without any change of value following successive flashes. These resistors must be of a non-capacitive type. 1/2W (1W for focus) hot molded carbon type resistors are well suited for this application.
- the grid and cathode connections on the PC board must be as short as possible and spaced well away from other connections in order to avoid parasitic inductions.

Furthermore, the TEA5101A has been provided with an additional effective feature to improve the flashover protection.As described in section I-4, a protection device has been included comprising a high voltage high current diode which is connected between each output and the high voltage power supply. The equivalent diagram of this protection is shown in Figure 8.

Figure 8.

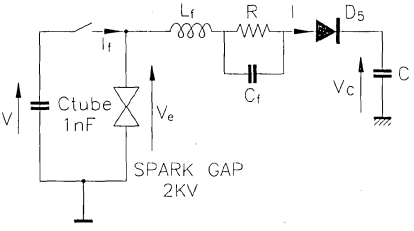


The flash current is diverted to the ground through the diode and the decoupling capacitor C.

Two kinds of flashes can occur:

1) low resistance flashes during which the spark gaps are activated since the cathode voltage exceeds the breakdown value of the spark gap. In this case the equivalent diagram is the following:

Figure 9.



I_f flash current (≅ 1000A)
L_f inductance of the connection (≅ 10µH)

V90TEA5101A-09

Ctube previously charged to 28kV is instantaneously discharged during

$$\Delta t = C_{tube} \times \Delta\frac{V}{I_f} = 30ns$$

Since the voltage across the spark gap falls almost instantaneously to 2000V, the peak current I flowing into the diode is (assuming V_C is held by good decoupling) :

$$I = \frac{V_e \times \Delta_t}{L_f} = 6A$$

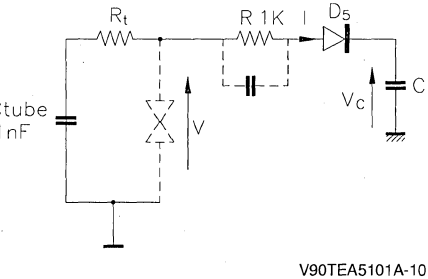
To ensure a variation of V_C less than 10V, C must be

$$C > \frac{I \times \Delta_t}{\Delta V_C} \quad eg \quad C > 18nF$$

The decoupling must have good HF characteristics.

2) high resistance flashes in which the spark gaps are not activated. In this case the equivalent diagram is the following:

Figure 10.



V90TEA5101A-10

If $V < 2$ kV, $I < \frac{2000}{R}$, $I < 2A$ and $R_t \cong 12k\Omega$

The time constant of the flash is $R_t \times C_{tube} = 12$ µs, the decay time is approximatevely 30 µs. The value of C must be

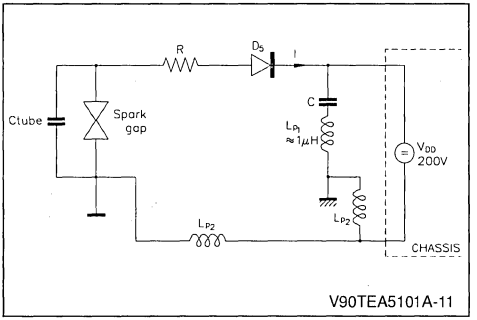
$$C > \frac{\Delta_t \times I}{\Delta V_C} \quad eg \quad C > 6\mu F$$

in order to ensure a VC variation less than 10V.

The total decoupling will be made up by a 10µF electrolytic capacitor connected in parallel with a 22nF plastic film capacitor with good HF properties.

It must be placed very close to the TEA5101A to be efficient. Otherwise, the equivalent diagram will be the following (case of low resistance flash).

Figure 11.



V90TEA5101A-11

$$\Delta V_C = \frac{I \times \Delta_t}{C} + \frac{L_{P1} \times I}{\Delta_t}$$

$\Delta V_C = 210V$ with $L_{p1} = 1$ µH and $L_{p2} = 0$

In this case the V_{DD} voltage can rise to a dangerous value (+210V increase) and the protection is not efficient.

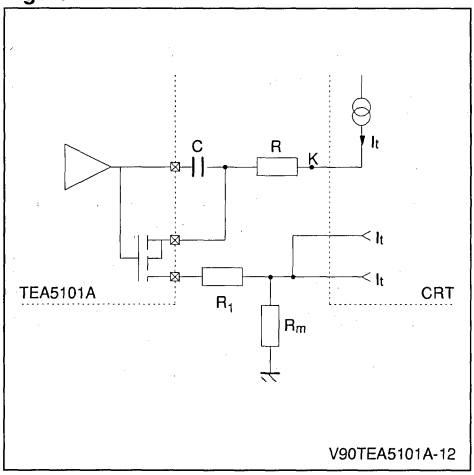
If the connection between the socket ground and the chassis ground is inductive ($L_{p2} \neq 0$), the effect is the same.

However in this case, all the TV IC's,and not only the TEA5101A,will be exposed to destructive overvoltages.

IV.4 OUTPUT SWING

The simplified diagram of this function is shown below (See Chapter II and chapter III):

Figure 12.



The current delivered by a CRT is given by the characteristic curves (fig 13-14).

The minimum value of V_k (due to all the voltage drops in the resistors and in the amplifier) is given by the equation (see fig 12 above):

$V_k = (R + R_{on} + R1 + 3 \times R_m) \times I_t = R_{eq} \times I_t$ (1)

with R_{on} : on state PMOS resistance

To find the maximum available current I_{tmax}, we can draw the curves of the equation (1) on the tube characteristics. I_{tmax} will be given by the intersection point of the curves. Since the tube characteristics are: I_t vs $V_{cutoff} + V_{G1} - V_k$ the equation (1) must be changed to

$$I_t = \frac{V_{CUTOFF} + V_{G1} - V_k}{R_{eq}} \quad (2)$$

Assuming V_{G1}= 0, we can draw the curves of equation (2) for several values of V_{cutoff} (eg 150V and 200V) and several values of R_{eq} (eg 5k,10k,15k,20k) (see fig 13 and 14). We can see from these curves that R_{eq} must have the following values to allow the tube to source 4mA per gun :

Figure 13.

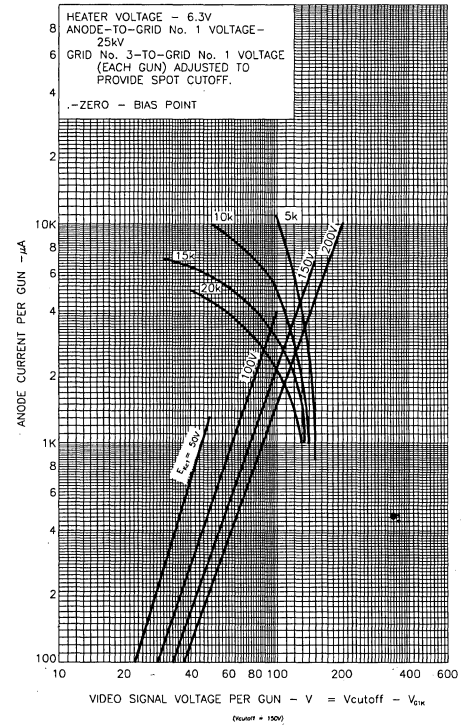
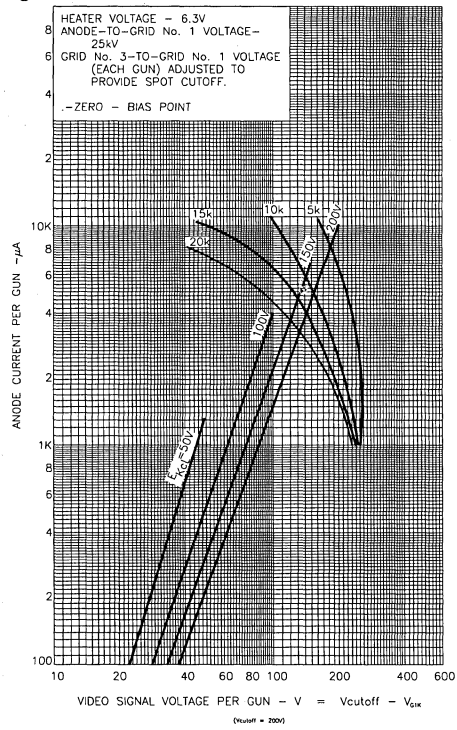


Figure 14.



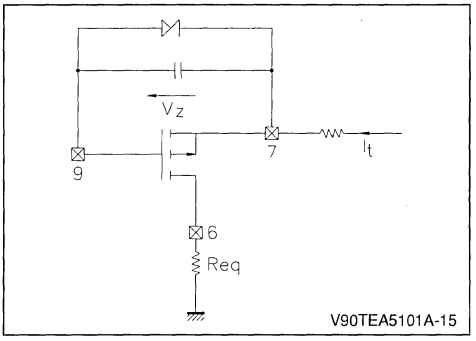
$R_{eq} \leq 5k\Omega$ for a 150V cutoff point
or $R_{eq} \leq 15k\Omega$ for a 200V cutoff point

As R_{on} value is approximatively 1.7kΩ, the measurement resistor must be as low as possible.

Working with higher cutoff point would be an alternative solution. But a 200V cutoff point seems to be too high a value since in this case the supply voltage would be greater than 200V and would affect reliability performances.

Another solution consists of connecting a zener diode as shown in Figure 15.With this device the high current operation of the TEA5101A is similar to that of a discrete amplifier (with PNP) operation.

Figure 15.



For low currents, if the zener voltage is greater than the V_{GS} voltage, the zener diode is biased off and the beam current flows through the measurement resistor. When the cathode voltage (pin 7) drop is limited because of the pin 6 voltage and when the pin 9 voltage continues to decrease,the zener diode is switched on when $V_7 - V_9 = V_Z$. In this case the beam current is absorbed by the voltage amplifier and the tube can provide larger current values.Nevertheless, the pin 7 output voltage will follow the pin 9 voltage with a V_Z difference.

Since the pin 9 voltage is internally limited to 14V, the output voltage will be limited to 22V with a 8V zener diode.

The CRT bias voltages shown on the previous curves are referenced to the G_1 voltage. The TEA5101A is referenced to ground. We can choose to work with a G_1 voltage greater than ground and thus the low level saturation is not taken into account. In this case, the cutoff points must be increased. When choosing V_{G1} = 12V, the cutoff points will be adjusted to 170V (instead of 150V).

Since the power supply is 200V, 30V are available to ensure correct blanking operation. The DC output voltage must be increased by 12V from its previous value.

Note that all the phenomena described in this section concern a static or quasi-static (15kHz) operation (e.g. white picture or rather large white pattern on a black background). When current peaks occur (e.g white characters insertion or straight luminance transition), the peaks will be absorbed by the coupling capacitor and the voltage amplifier,and hence the tube will be able to source a greater current.

IV.5 LOW CURRENT MEASUREMENTS

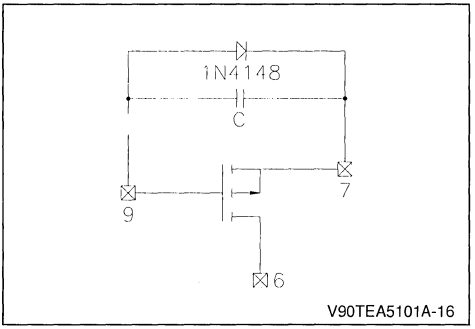
We have seen in section II-2.2 how the beam current monitoring works (see fig.3 page 6). We have seen that the capacitor C must charge again after the blanking phase.

This charge is generally furnished by the tube capacitor independently from the beam current.However,if during the blanking phase, the output voltage is too low (e.g. the PMOS is reverse biased (- 20V) because of a too high leakage current or when measuring with an oscilloscope probe), the ΔVC required to charge C again will be greater than the maximum charge available from the tube capacitor.Hence the beam current will have to charge C in a first step.

Since this current is rather low during the cutoff adjustement phase, a long time will be spent to charge C. The current absorbed by the PMOS and fed to the videoprocessor will not be equal to the beam current and the cutoff adjustement will not be correct.

Hence the reverse voltage across the capacitor C must be limited by a diode connected as follows :

Figure 16.



With this configuration, the voltage across C will be -0.6V max. Since this voltage must be 2.5V in the stationary state (see section II-2.2), the voltage across C must be increased by 3.1V and this charge can be supplied by C_L. We can also slightly decrease the value of C. However if C is too low, the HF behaviour will be impaired.

V - APPLICATION EXAMPLES

V.1 APPLICATION DESCRIPTION

Figures 17 and 18 show two applications, one for a 45AX tube and the videoprocessor TDA3562A (application 1), the other designed for S4 type tube and the videoprocessor TEA5031D (application 2). In these two applications, the nominal gain is 28dB and the output black level is 150V. The quasi cutoff currents are respectively 10µA and 16µA for applications 1 and 2.

These applications are implemented using the same PC board especially designed to allow different options for tube biasing, power supply decoupling and connections. This PC board allows also two different tube sockets (jedec B8274 or B10277) to be connected. Both beam current monitoring modes (sequential and parallel) are possible.

The layout and the electrical diagram of the PC board are shown in Figures 19 and 20.

V.2 PERFORMANCE EVALUATION

As seen in chapter IV, the dynamic performances (bandwidth, crosstalk) of the TEA5101A is very dependent on the PCB layout.Consequently, the evaluation board has been designed to obtain the best results.

To evaluate the performance, the best way is to work outside of the TV set by driving the amplifier by an HF generator (or a network analyser) while simulating the load conditions fixed by the CRT, since AC performances are directly determined by the load.

V.2.1. Measurement conditions

The schematic diagrams of the AC measurements are shown in Figures 21 and 22. The conditions are as follows:

- BIASING : V_{OUTDC} = 100V by choosing $R_{11} = R_{21} = R_{31} = 1.5k\Omega$ and V_{DD} = 200V
- AC GAIN = 50 by adjusting P10, P20, P30
- LOADING :
  - by a 8.2pF capacitor and the probe capacitor (2pF), the sum is equivalent to the capacitance of a CRT with the socket and the spark gaps
  - the 1MΩ resistors connected between each output and V_{DD} allow the conduction of the beam current monitoring PMOS transistor in such a way that $VA_{DC} = VB_{DC}$= 100V.
- DRIVING by a 1µF capacitor, the HF generator being loaded by 50Ω.
- the dynamic power dissipated in the IC will increase with frequency. To avoid the temperature increasing, it is necessary to do very quick measurements or to use a low R_{th} (7°C/W) heatsink in forced convection configuration. Such conditions are not present in a TV set since the driving signal will be a video signal instead of a pure HF signal.

V.2.2. Results

V.2.2.1. Bandwidth

The curves Figures 23 and 24 show the frequency responses of one channel with $100V_{pp}$ and $50V_{pp}$ output voltages.

The bandwidths are approximatively 8MHz at $100V_{pp}$ and up to 10MHz at $50V_{pp}$.

V.2.2.2. Crosstalk

The curves Figures 25, 26 and 27 show the crosstalk for this application.The crosstalk is almost the same for the six different combinations of the three channels. The worst value is -24dB at 5MHz.

V.2.2.3. Transition times

The curves Figure 28 show respectively the R, G, B rise and fall times of respectively 49 ns and 48 ns with a $100V_{pp}$ output voltage (between 50 and 150V).

The difference between rise times of the three channels is less than 1ns.

The difference between fall times of the three channels is less than 2ns.

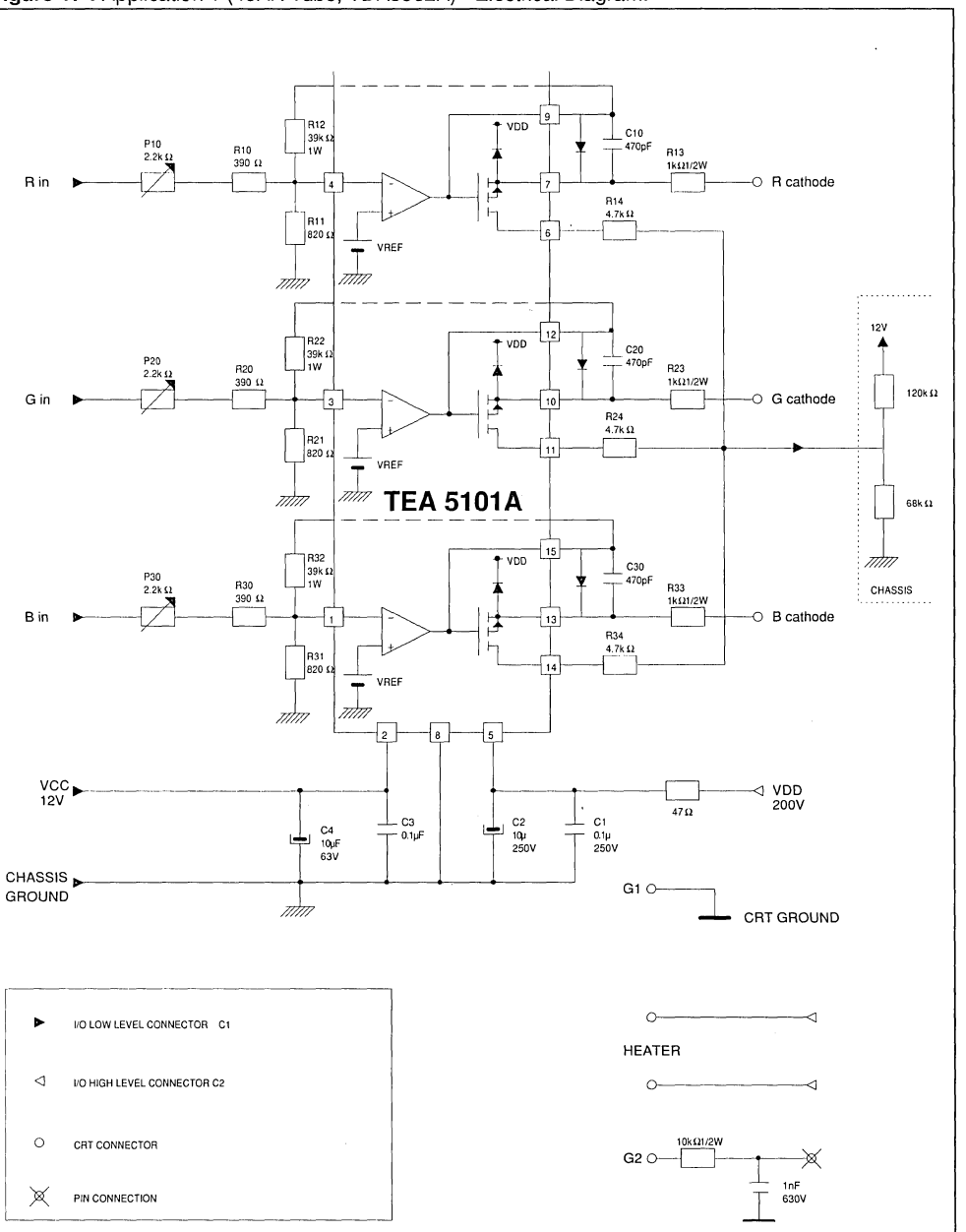
The delay time at rising output is 48ns.

The delay time at falling output is 50ns.

The difference between the delay times is less than 2ns.

The slew rate is about 2000V/µs.

Figure 17 : Application 1 (45AX Tube, TDA3562A) - Electrical Diagram.



V90TEA5101A-17

Figure 18 : Application 2 (PIL24 Tube, TEA5031D) - Electrical Diagram.

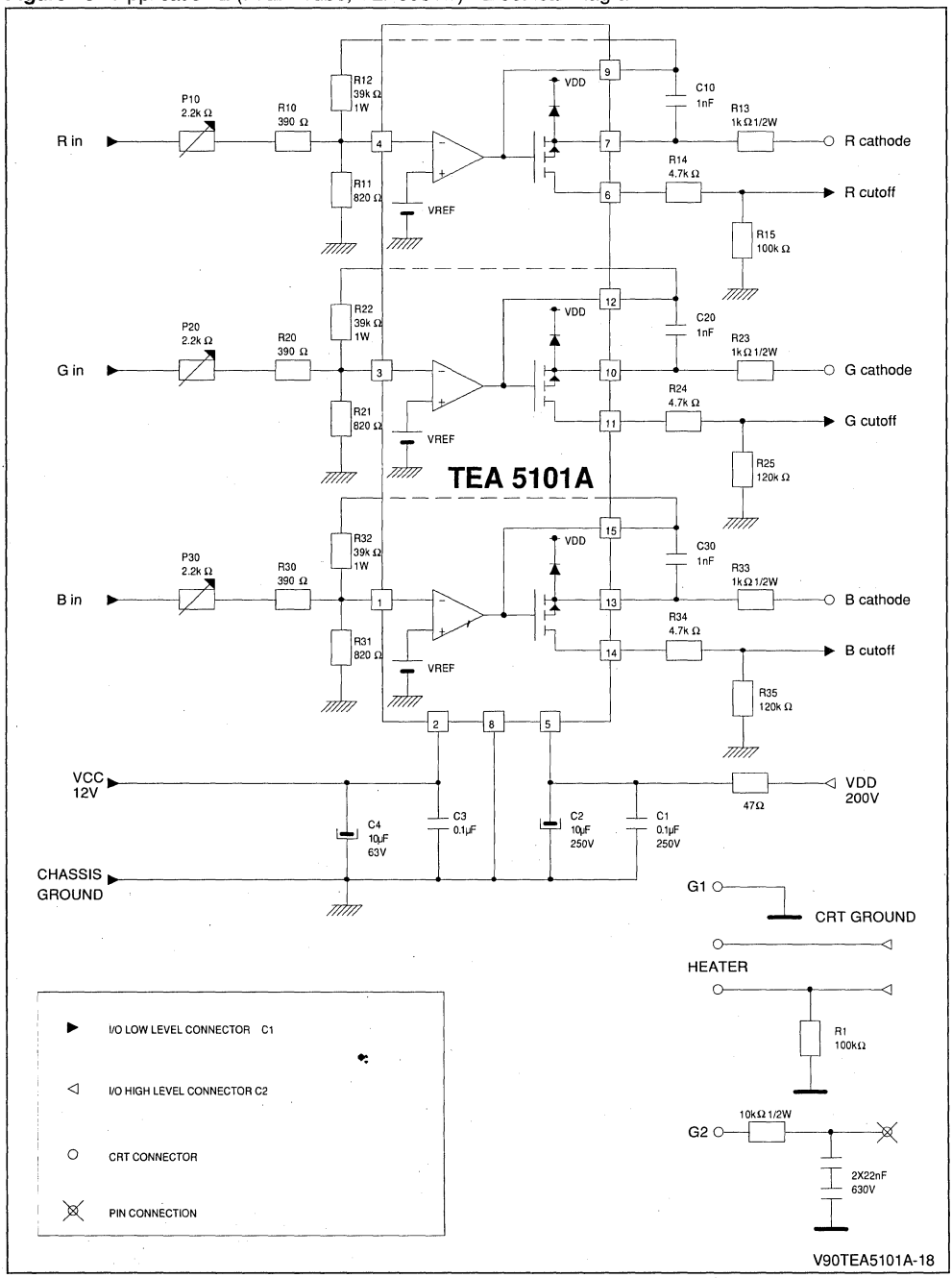
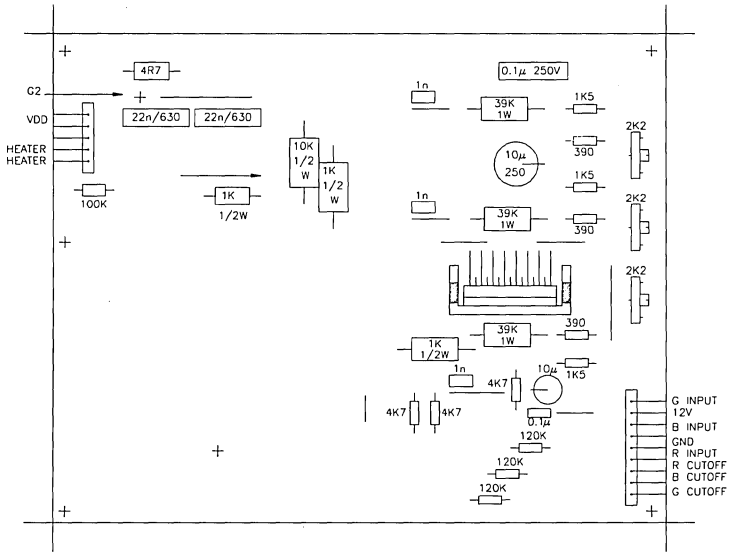
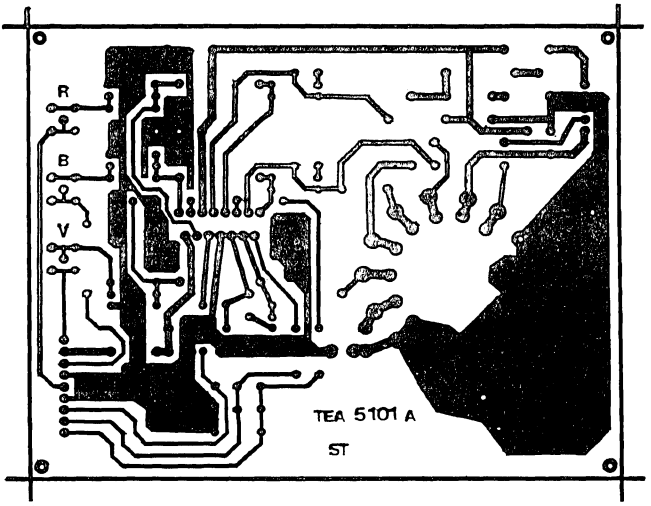


Figure 19 : TEA5101A Evaluation Board Layout and Components View.



COMPONENT SIDE

V90TEA5101-19A



COPPER SIDE

V90TEA5101-19B

Figure 20 : TEA5101A Evaluation Board Electrical Schematic Diagram.

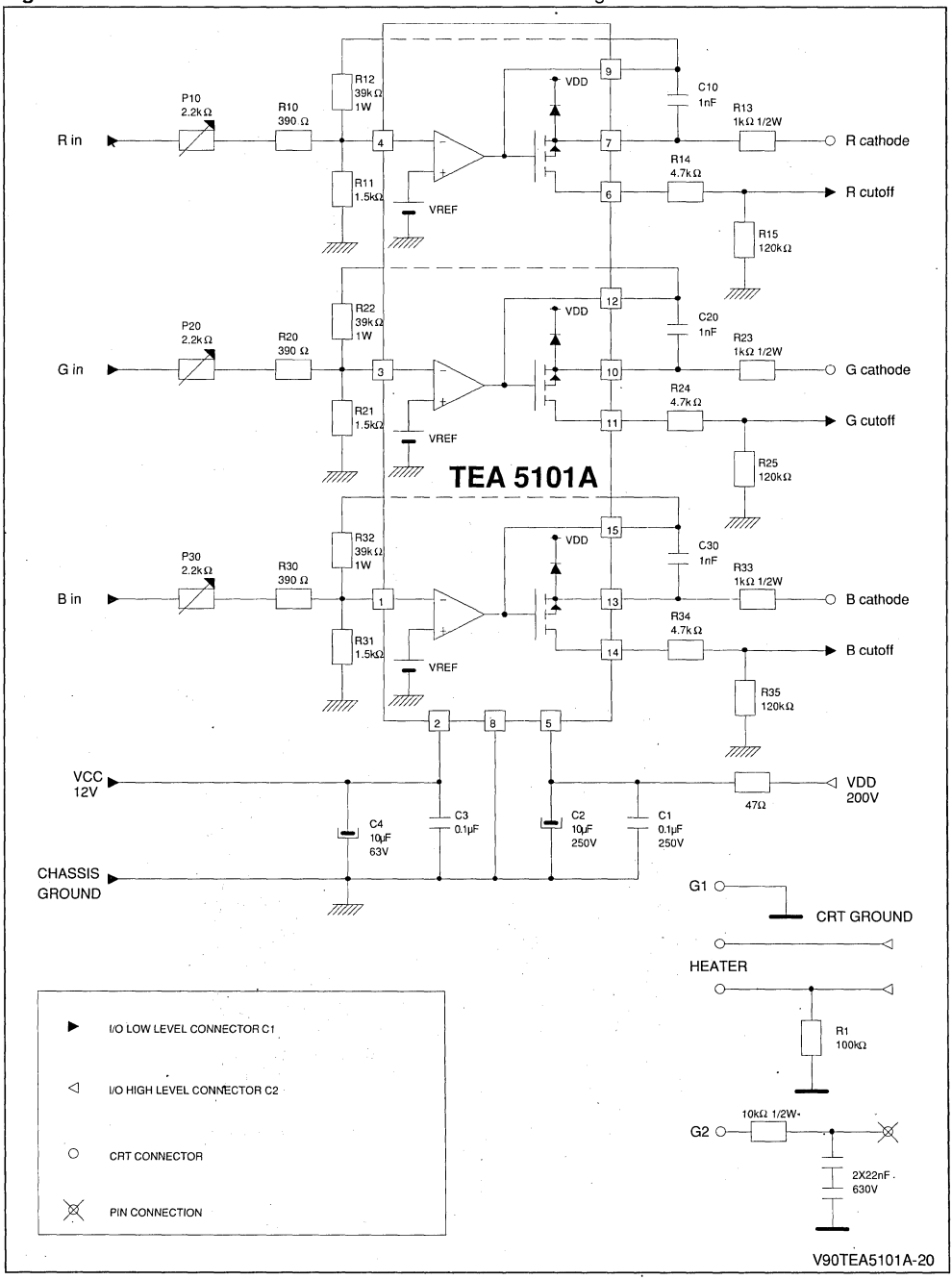


Figure 21 : Bandwith Measurement Configuration.

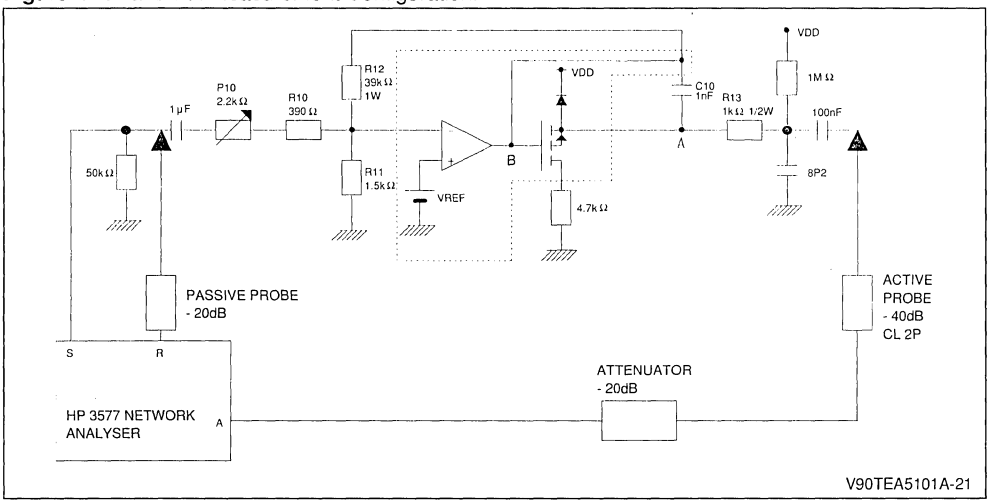


Figure 22 : Crosstalk Measurement Configuration.

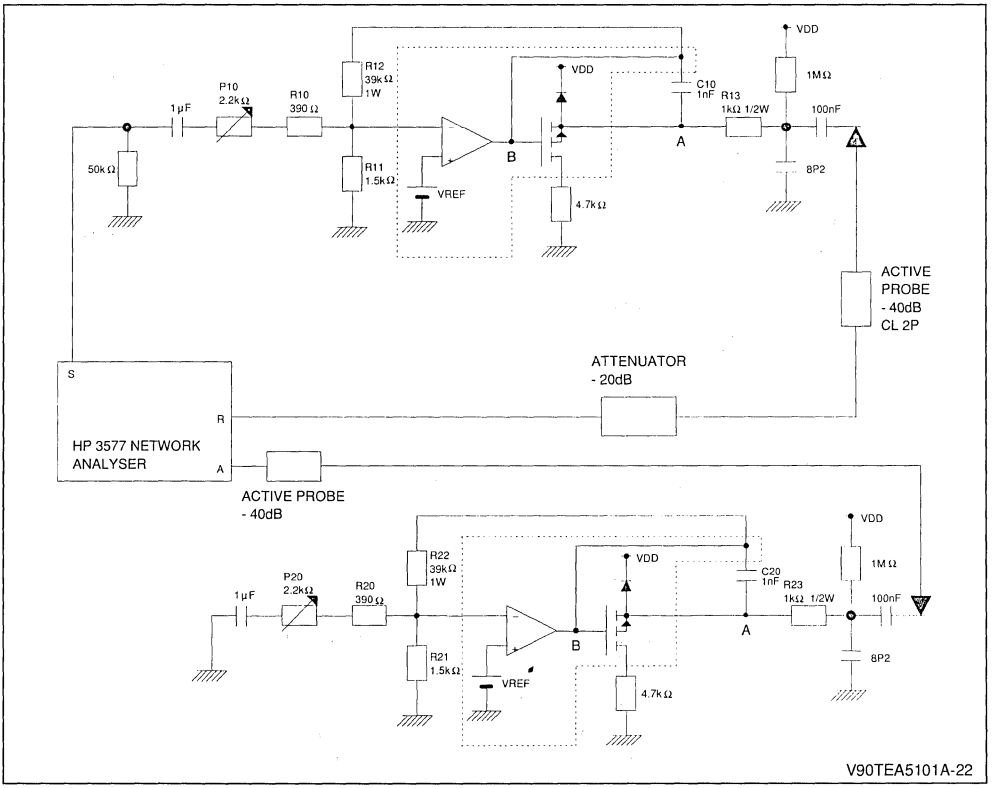
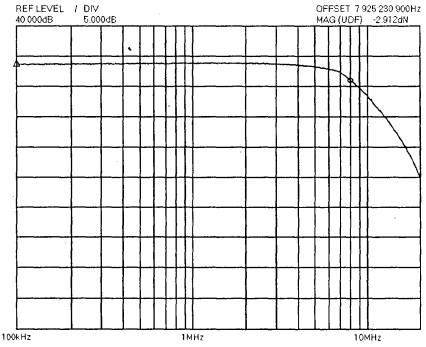
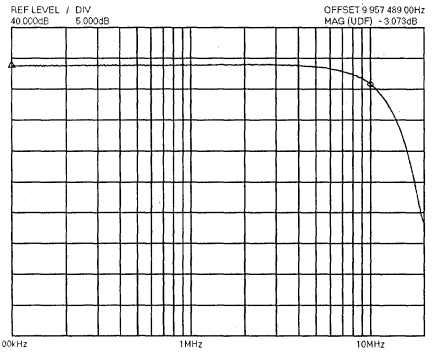


Figure 23 : Frequency Response of R Channel ($100V_{pp}$).



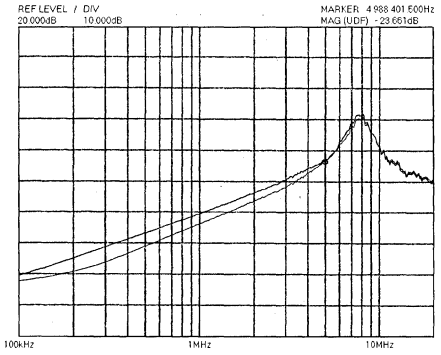
V90TEA5101A-23

Figure 24 : Frequency Response of R Channel ($50V_{pp}$).



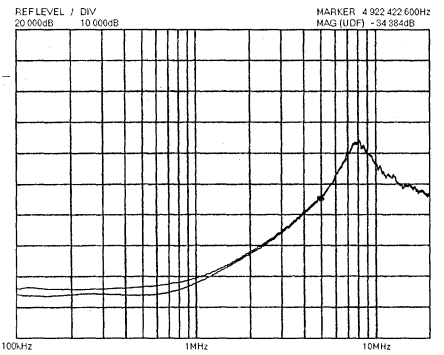
V90TEA5101A-24

Figure 25 : Crosstalk between R Channel and G and B Ones.



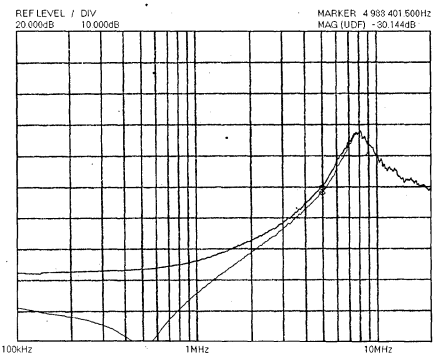
V90TEA5101A-25

Figure 26 : Crosstalk between G Channel and R and B Ones.



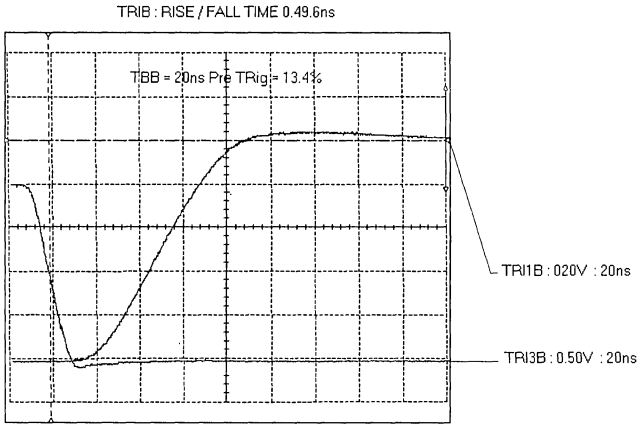
V90TEA5101A-26

Figure 27 : Crosstalk between B Channel and R and G Ones.



V90TEA5101A-27

Figures 28A and 28B : TEA5101A R Channel Step Response.



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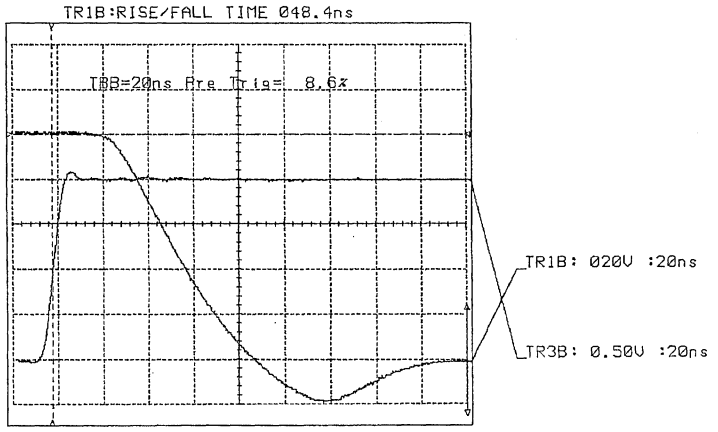


V90TEA5101A-28B

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TV EAST/WEST CORRECTION CIRCUITS

SUMMARY

SUMMARY (continued)

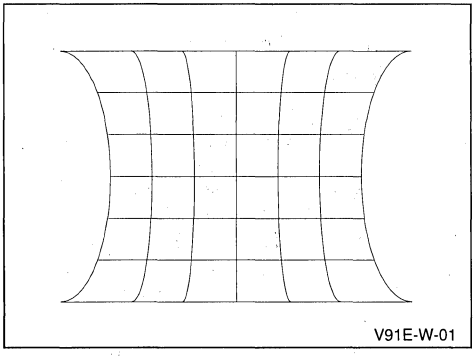
I - TV EAST/WEST CORRECTION GENERAL PRINCIPLES

I.1 - INTRODUCTION

All color picture tubes which are used in the present TV-sets have a magnetic deflection system. Using a homogenous magnetic field, we have generally a pillow-distortion of a rectangular picture on the screen. This is mainly due to the tangens relation between the deflection angle and the beam position on the screen

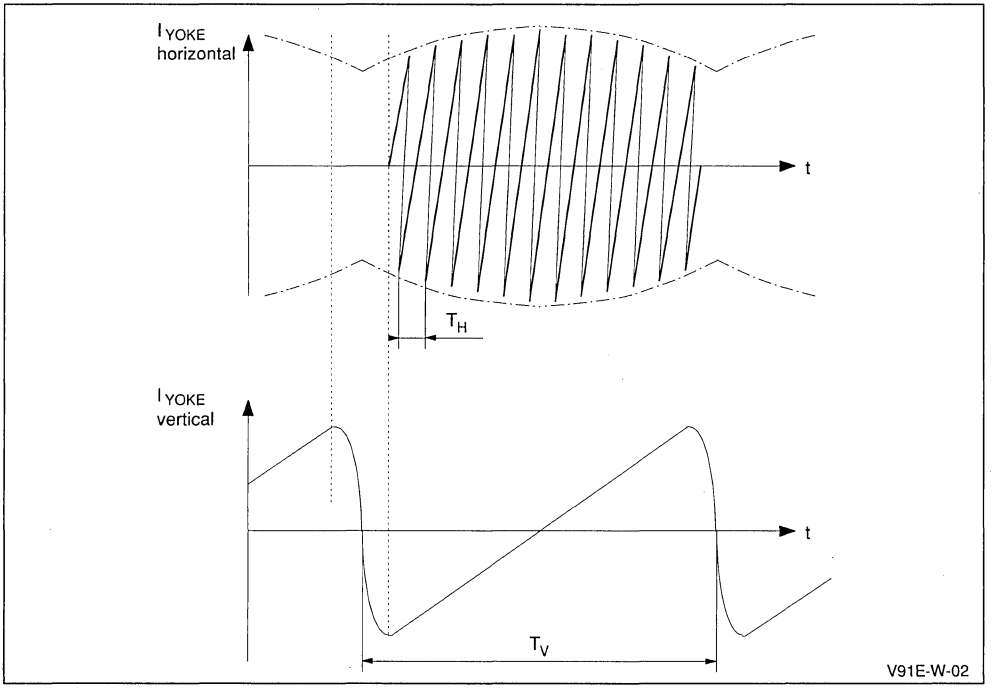
Using a well dimensioned and optimized inhomogenous magnetic deflection field, this distortion can be eliminated completely for picture tubes with a deflection angle of 90°. In the same way the pillow-distortion of 110° deflection tubes can be eliminated in the vertical direction (North-South direction). But until now the distortion in the horizontal direction (East-West direction) can not eliminated with special designed deflection yokes. A distortion remains in Figure 1.

Figure 1 : Test Grid on a 110° Color Tube



In order to compensate this effect, the horizontal deflection current in the yoke must be modulated. This means a large amplitude of the deflection current in the middle of the screen and a small amplitude on the top and the bottom of the screen. The general behaviour of the deflection currents is illustrated in Figure 2.

Figure 2 : Horizontal and Vertical Yoke Current (T_H = 64µs, T_V = 20ms)



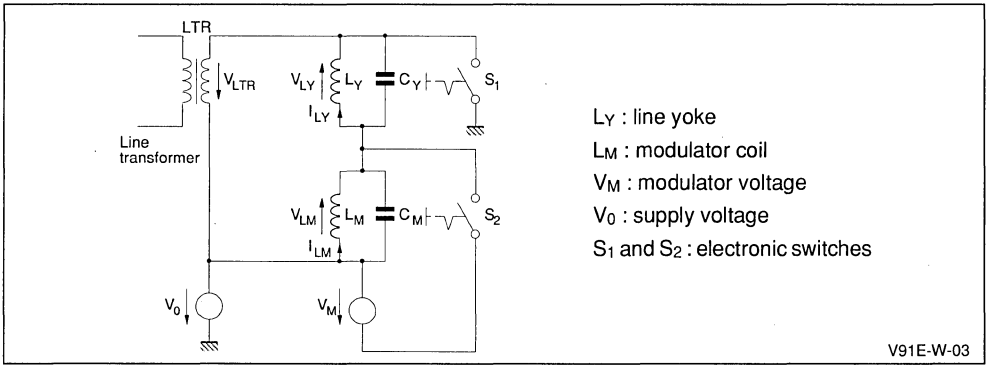
In this picture T_V and T_H are the time periods for the vertical and the horizontal deflection. Note that the envelope of the horizontal yoke current must be a parabola with the same phase as the vertical saw-tooth current. This means an East/West correction can be reached by modulating the horizontal yoke current with a parabola.

There are different possibilities to modulate the yoke current. The most convenient modulator is the so-called **Diode Modulator** described in the next chapter.

I.2 - DIODE MODULATOR PRINCIPLE

Let us consider the basic circuit of the horizontal deflection unit as shown in Figure 3.

Figure 3 : Basic Circuit of the Horizontal Deflection Power Stage including Modulator



L_Y : line yoke
L_M : modulator coil
V_M : modulator voltage
V_0 : supply voltage
S_1 and S_2 : electronic switches

For the sake of simplicity, the electronic switches (diodes and transistors) are drawn as simple switches S_1 and S_2. The deflection time T_H of 64µs can be divided in two parts : the scan time T_S at which the electronic switches S_1 and S_2 are closed and the flyback time T_F (S_1 and S_2 opened). The total time period is the

$$T_H = T_F + T_S \quad (1.1)$$

We assume now that the line transformer L_{TR} have a neglectable high inductance and the time behaviour is mainly determined by L_Y, L_M, C_Y, C_M. Small modifications are necessary to consider also the electrical characteristics of L_{TR}, but they should not be discussed here.

During the scan time the inductors L_Y and L_M are directly connected to the voltage sources V_0 and V_M :

$$\left.\begin{aligned} V_{LY} &= V_0 - V_M \\ V_{LM} &= V_M \end{aligned}\right\} \text{ } S_1 \text{ and } S_2 \text{ closed (scan time)} \quad (1.2)\ (1.3)$$

Neglecting any power consumption in possible series resistors, the current in the two inductors increases linear in time :

$$i_{LY} = \frac{t\,(V_0 - V_M)}{L_Y} \quad (1.4)$$

$$i_{LM} = \frac{t\,V_M}{L_M} \quad (1.5)$$

Since the current i_{LY} and i_{LM} must be zero-symmetrical (average value = 0), the peak value of i_{LY} and i_{LM} is obtained after half of the scan time $T_S/2$

$$\hat{i}_{LY} = \frac{T_S\,(V_0 - V_M)}{2\,L_Y} \quad (1.6)$$

$$\hat{i}_{LM} = \frac{T_S\,V_M}{2\,L_M} \quad (1.7)$$

After this time, S_1 and S_2 are opened and the energy in the inductors L_Y and L_M changes to the capacitors C_Y and C_M. We assume now the same resonance frequency for both LC parts

$$L_Y\,C_Y = L_M\,C_M = L\,C \quad (1.8)$$

Under this condition, both capacitors C_Y and C_M have its peak voltage at the half of the flyback time $T_F/2$. The energy in the inductors stored at the end of the scan period

$$E_L = \frac{1}{2}\,L\,(i_L)^2 \text{ is then} \quad (1.9)$$

completely transformed into the capacitor

$$E_C = \frac{1}{2}\,C\,(V_C)^2 \quad (1.10)$$

Under this condition, we obtain the general equation for the peak voltage in the middle of the flyback period

$$\hat{V}_C = -\,\hat{i}_L\,\sqrt{\frac{L}{C}} + V_{init} \quad (1.11)$$

This voltage is the addition of the initial voltage and the voltage increase due to the energy transfer. With (1.6) and (1.11) we get

$$\hat{V}_{LY} = \hat{V}_{CY} = -\,\frac{V_0 - V_M}{\sqrt{L_Y\,C_Y}}\,\frac{T_S}{2} + (V_0 - V_M)$$

$$= (V_0 - V_M)\,(1 - \frac{T_S}{2\sqrt{L\,C}}) \quad (1.12)$$

in the same way (1.7 and 1.11) we obtain

$$\hat{V}_{LM} = \hat{V}_{CM} = V_M\,(1 - \frac{T_S}{2\sqrt{L\,C}}) \quad (1.13)$$

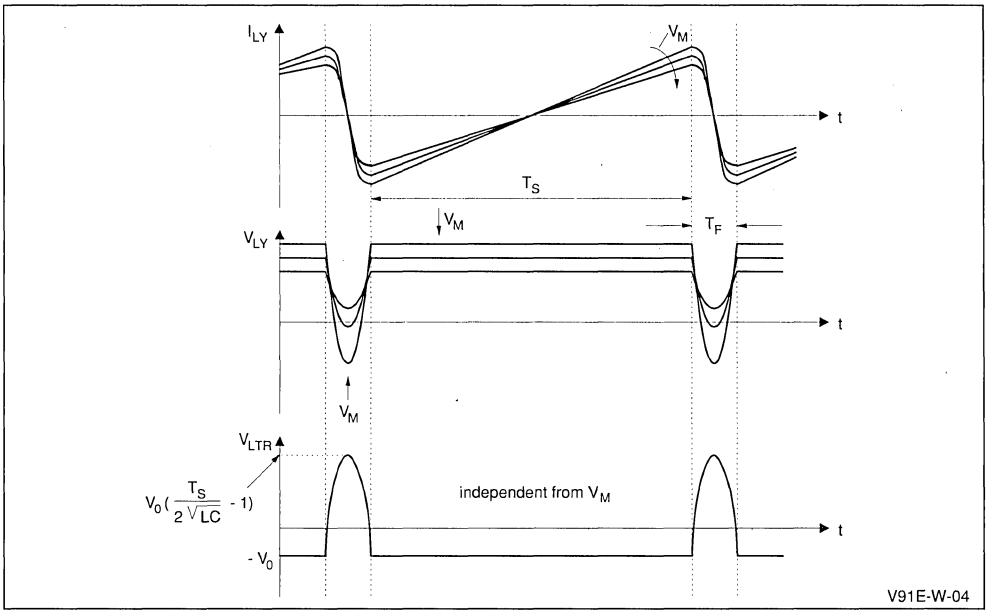
The resulting peak voltage during the flyback time at the line transformer is then

$$\hat{V}_{LTR} = -\,\hat{V}_{LY} - \hat{V}_{LM} = V_0\,(\frac{T_S}{2\sqrt{L\,C}} - 1) \quad (1.14)$$

Please note that in this circuit, the horizontal flyback voltage $\hat{V}_{LTR}$ (1.14) is independent from the modulation voltage V_M, though the yoke current I_{LY} can be changed via the modulator voltage V_M (see 1.6)

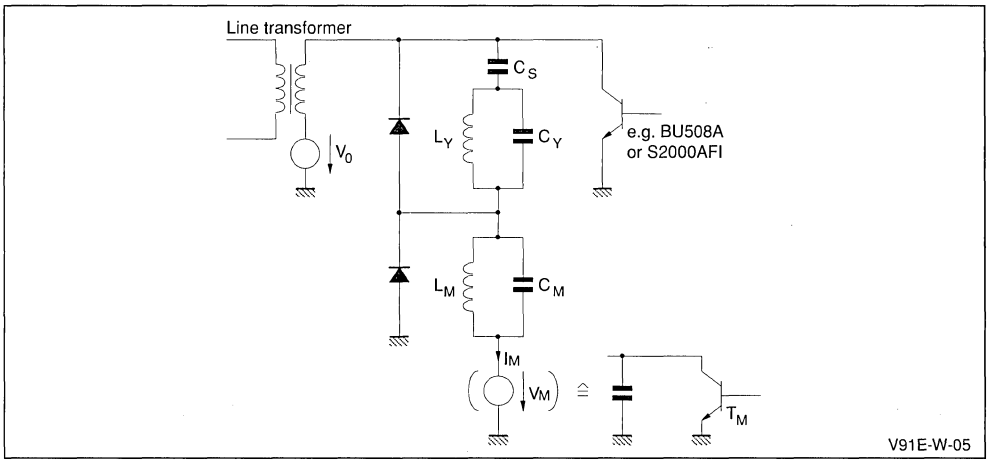
An overview of the currents and voltages is given in Figure 4.

Figure 4 : Currents and Voltages of the Basic Circuit



For a practical application, a large capacitor C_S can be inserted in series to the yoke to get an S-correction of the deflection current I_{LY}. Simultaneously, the voltage V_M can be grouded to have a simpler handling of the modulator driver. The switch S_1 is a standard high voltage power transistor (e.g. BU508A or S2000AFI), the switch S_2 can be replaced by 2 diodes as shown in Figure 5.

Figure 5 : Standard Diode Modulator with Class-A Modulator Driver

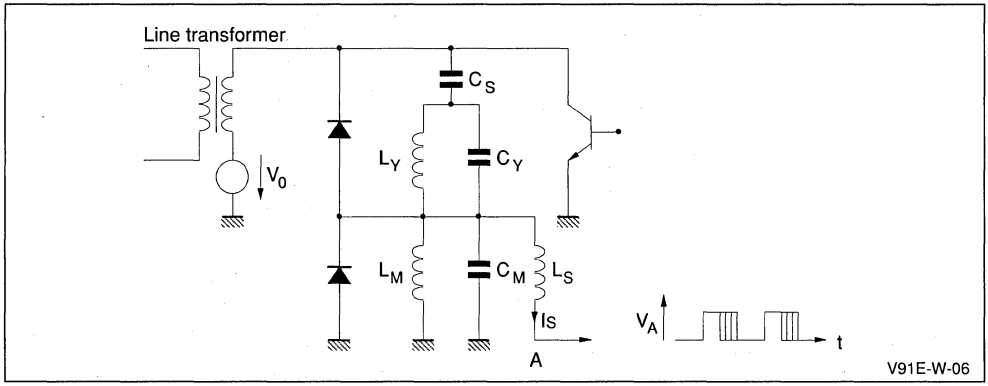


Normally, the current I_M into the modulator voltage source is positive and V_M must only be realized as a variable resistor (e.g. transistor T_M).

Many manufacturers use this simple diode modulator with such active load. A disadvantage of this application is the power consumption in the power transistor T_M (~2W). Under ideal conditions, V_M should have no power consumption (average $i_M = 0$), but in practice the coils and the line transformer are not free from parasitic resistors. Furthermore a reasonably large power is used from the various loads on the line transformer.

An improvement from the power consumption point of view is the use of a switched power stage V_M. For this purpose, an additional inductance L_S (5...20mH) is used and connected as shown in Figure 6.

Figure 6 : Standard Diode Modulator with Class D Modulator Driver (pulse-width modulator)

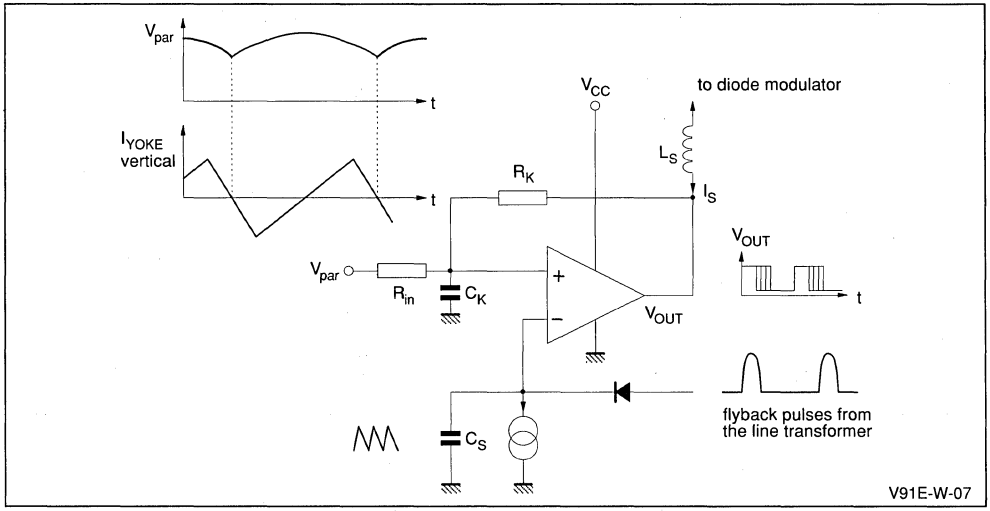


Point A is biased from a pulse-width modulated rectangular wave. The frequency is arbitrary, for a simple pulse-width modulator, The horizontal line frequency is used normally.

I.3 - PULSE-WIDTH MODULATOR PRINCIPLE

The pulse-width modulator for driving the diode modulator contains mainly one power comparator with the external circuitry shown in Figure 7.

Figure 7 : Pulse-Width Modulator

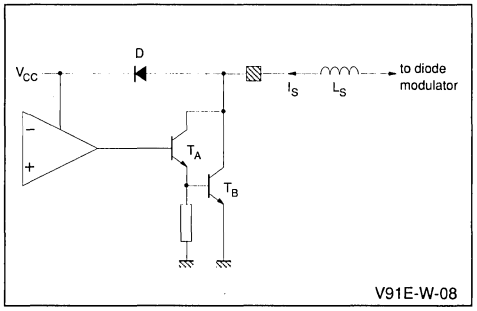


The working frequency is determined by the linear saw-tooth voltage biasing the positive comparator input. It is generated by the flyback pulses of the line transformer. The current sink on the positive input discharges the capacitor C_S during the scan time T_S and yields the negative slope of the saw-tooth voltage.
The negative input is biased from a parabola voltage, its generation is discussed later.

To improve the performance of this pulse-width modulator, a feedback path R_K is provided compensating variations in the power supply V_{CC} of the comparator. The capacitor C_K together with R_{in} and R_K serves as a low-pass filter to suppress the line frequency coming from the comparator output.

If the current I_S in the inductor L_S (see Figures 6 and 7) is only positive, the output stage can have a simple darlington transistor and a diode as seen in Figure 8.

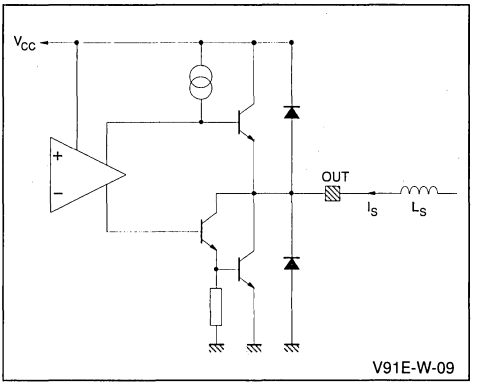
Figure 8 : Comparator Output Stage, only positive modulator current I_S is allowed



If the darlington stage is switched on, the current I_S is flowing through T_A and T_B into ground. Otherwise, the diode D is conducting and I_S flows into the supply voltage.
The power, consumed normally in L_M (see Figure 5) is then redelivered into this supply voltage.

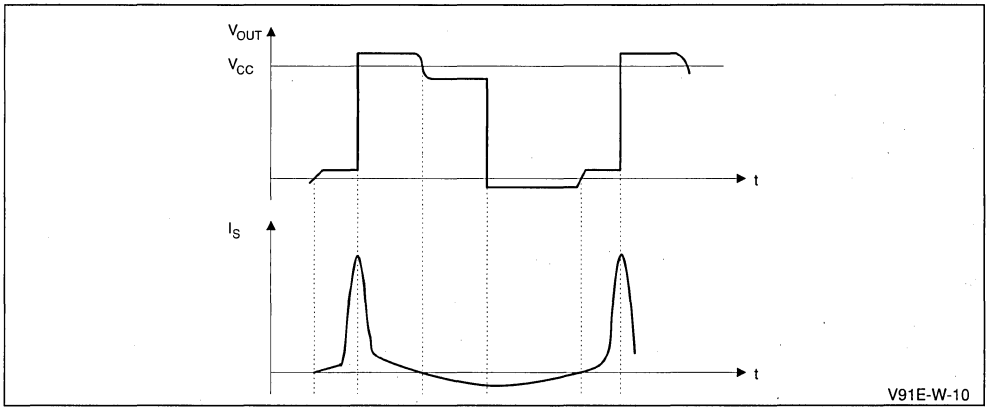
A greater flexibility in the design of the diode modulator can be reached, if the current I_S is allowed to have negative values. For this case, the comparator power stage must be realized as push-pull stage (see Figure 9).

Figure 9 : Comparator Output Push-pull Stage, negative and positive modulator current I_S allowed



Due to the voltage drop across the transistors and diodes, the transition from positive values I_S and negative values I_S yields a voltage step on the output as illustrated in Figure 10.

Figure 10 : Voltage on the comparator output by zero crossing of I_S



In this case the steps in the output voltage produce an additional undesired modulation of the yoke current. Then you can see some irregularities in the vertical lines of the test grid on the screen. With the aid of a reasonable large fedback factor (small R_K, small C_S, large parabola amplitude) this effect becomes neglectable.

I.4 - GENERAL CONSIDERATIONS TO GENERATE THE CORRECTION PARABOLA

The correction parabola which drives the pulse-width modulator (Figure 7) must have the same frequency and phase as the vertical deflection current in the yoke. Therefore, the parabola can be generated directly from the vertical saw-tooth signal which drives the deflection output stage. Principally there are two different kinds for generating the parabola:

a) integrator-network (linear)

b) functional-network (non linear)

Let us consider first the integration method :
The vertical saw-tooth signal can be described with the following simple equation, valid for one period

$$S_{saw\text{-}tooth}(t) = A\frac{t}{T_V} \quad 0 < t < T_V \qquad (1.15)$$

where A is the amplitude, T_V the time period and t the time.

Integrating this signal we get

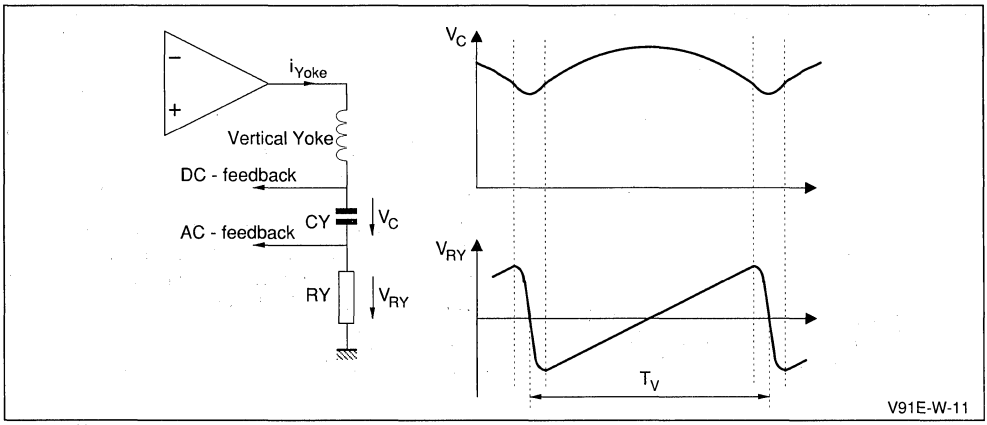
$$\int_0^t S_{saw\text{-}tooth}(t)\,dt = \int_0^t A\frac{t}{T_V}\,dt = \frac{A}{2\,T_V}t^2 \qquad (1.16)$$

Since the relation between the current and the voltage on a capacitor is given by

$$V_C(t) = \int i_C(t)\,dt \qquad (1.17)$$

the parabola can be obtained directly from the coupling capacitor C_Y in the vertical output stage as illustrated in Figure 11.

Figure 11 : Vertical Output Stage and Corresponding Voltages



Due to the aging and the temperature dependence of this (electrolytic) capacitor C_Y, some manufacturers prefer to generate the parabola from the voltage drop across R_Y (V_{RY}) with the aid of a separate integrator.
Due to the small amount of active and passive components, this integration method is the usual method to realize the East/West correction circuit with discrete elements.

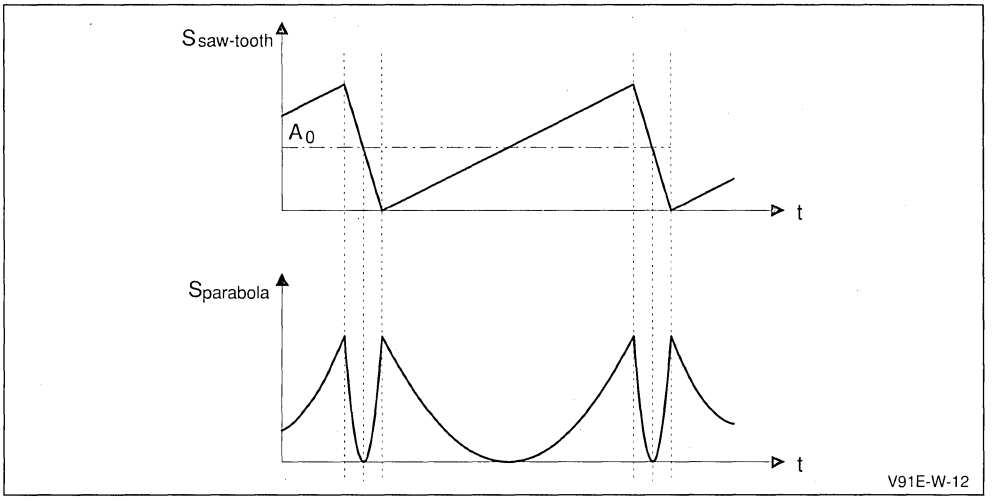
The functional network realization requires a quite larger amount of active components and is therefore especially suited for integrated circuits. The input signal for this kind of parabola generation is also the vertical saw-tooth signal corresponding to (1.15). With the aid of a functional (square) network, the square of this signal can be formed according to the following equation :

$$S_{parabola} = k\,(S_{saw\text{-}tooth} - S_0)^2 = k\,(A\frac{t}{T_V} - A_0)^2 \qquad (1.18)$$

and is illustrated in Figure 12.

Thereby, k is the gain and A_0 is a DC-level which allows to adjust the symmetry of the parabola ("trapezoidal" or "keystone" correction).

Figure 12 : Generation of the Parabola with Functional Network



Comparing the two methods, the following properties are evident :

- the parabola amplitude using the integration method is frequency dependent : assuming a constant amplitude of the saw-tooth signal, the amplitude of the parabola is linear in the time period T_V (see 1.16) . This means different adjustments between 50 and 60Hz TV-sets. The functional (square) method gives a frequency-independent amplitude of the parabola, if a constant saw-tooth signal is provided.
- during the flyback time of the saw-tooth signal, the functional network produces a second (parasitic) parabola as shown in Figure 12

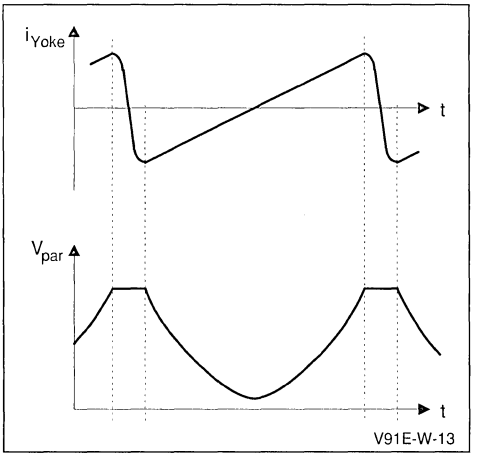
Although this parasitic parabola is present during the vertical flyback time (dark screen) this small parabola (like a spike) produces a damped oscillation of the diode modulator. The result is a damped sinusoidal vertical line on the top of the screen, if a test-grid is on the screen (the vertical lines are similar to a crutch-stick).

The maximum amplitude of this oscillation is present on the left and right top of the screen. Though its amplitude is normally only about 3mm, this effect must be suppressed.

This can be reached by two different methods :

- the linear saw-tooth voltage generating the parabola must have an extremely small flyback time. Then the very small parasitic parabola is integrated in the capacitor C_K of the comparator and has no effect (see Figure 7). The saw-tooth voltage coming from the vertical oscillator fulfills this requirement wherefore the deflection yoke-current has a too large flyback time.
- another possibility is to hold the parabola signal constant during the flyback time as illustrated in Figure 13.
  This behaviour can be reached by providing a parabola output limitation and then overmodulating the functional network during the flyback time.

Figure 13 : Modified parabola : constant during the flyback time



Overcoming the problems of the parasitic parabola, the functional method should be preferred due to the independence of the frequency (50/60Hz compatibility).

The nonlinearity which forms the parabola can be realized in two different ways :

- use of an analog multiplier
- forming a nonlinear network by piece wise linearization.

I.5 - ADJUSTMENTS

I.5.1 - Horizontal size adjustment

Adjustment of horizontal amplitude is made by modifying the mean cyclic ratio (duty factor) of the output pulses. When this mean cyclic ratio is minimum, the picture width is maximum, because the output is more frequently in the low state, and therefore the highest current is drawn from the diode modulator and the deflection current is maximum.

To change the mean cyclic ratio of the pulse train (in addition to the change due to the parabolic shape of the signal) it is necessary to change the continuous level of the sawtooth pulse train (see Figure 14).

The rise of the continous level of the parabola is due to the increase of the cyclic ratio, as we have seen above. The value of pincushion correction is not modified since the parabola peak-to-peak amplitude is kept the same. Only the mean cyclic ratio varies, i.e. also the horizontal scan width.

I.5.2 - Pincushion correction adjustment

Pincushion correction is made by varying the peak-to-peak amplitude of the parabola. The greater this amplitude,the greater the variation of the output signal cyclic ratio is between the ends and the top of the parabola, and therefore the more important is the parabolic modulation of the current drawn from the diode modulator (see Figure 15).

Figure 14 : Horizontal Size Adjustment

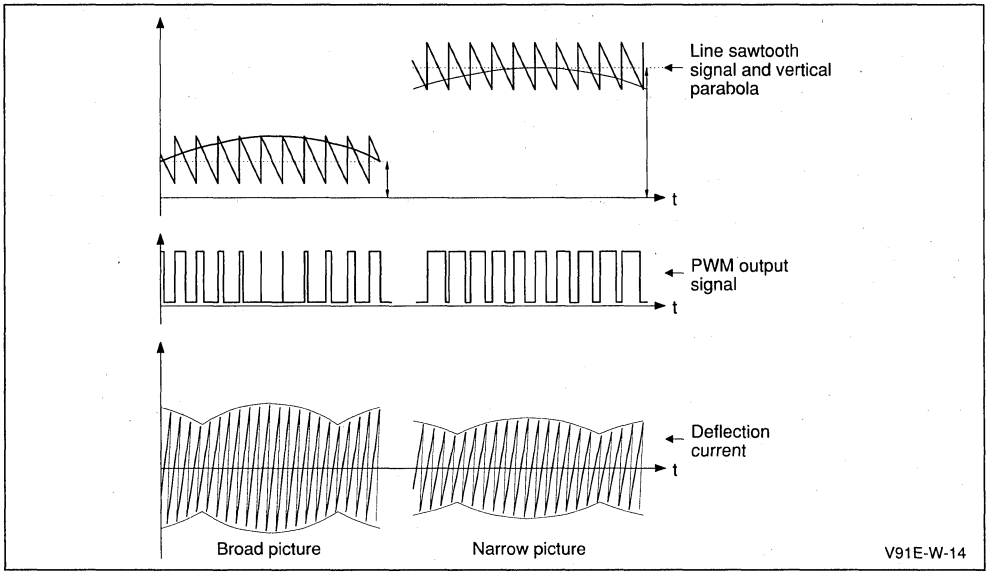
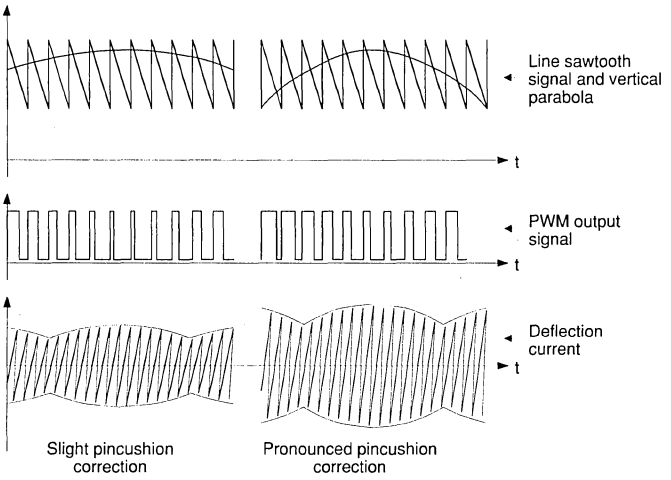


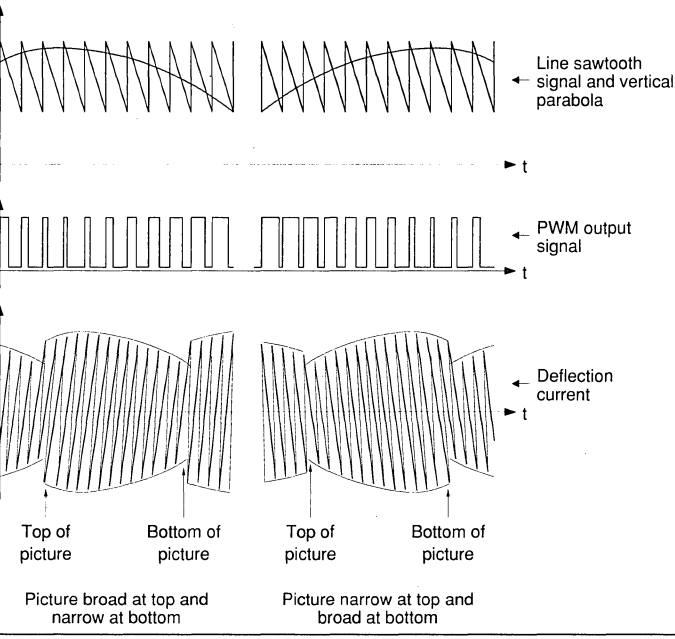
Figure 15 : Pincushion Correction Adjustment



I.5.3 - Trapezium correction adjustment (keystone correction)

Trapezium correction is made by modifying the symmetry of the left and right sides of the parabola (Figure 16).

Figure 16 : Keystone Correction



I.6 - PRODUCTS PRESENTATION

All the East/West correction devices are with class D diode modulator driver. Concerning the frame parabola generation, TDA4950, TDA8145 and TDA8146 use a non-linear network whereas TEA2031A uses an analog multiplier. TDA4950 and TDA8145 generate a parabola with a fixed shape; this shape is different between the two devices and makes the TDA4950 intended for standard CRT and TDA8145 for square tubes. These two devices have a parasitic parabola suppression (during vertical flyback time) by current limitation. TDA8146 has a programmable parabola shape generation by segments which makes it suitable for different CRTs. It has also a parasitic parabola suppression by pulse during vertical flyback.

All the devices can support a keystone correction adjustment (parabola symmetry) and have 50/60Hz capability. Some others adjustments are possible (picture width...).

Finally, another available device the TDA8147 has been designed for use in the East/West pincushion correction by driving a diode modulator but since this device has not the parabola generator and is drived by a PWM, it is very useful in digital TV-sets.

A detailed description about all the devices is done in the next chapters.

II - TEA2031A GENERAL DESCRIPTION

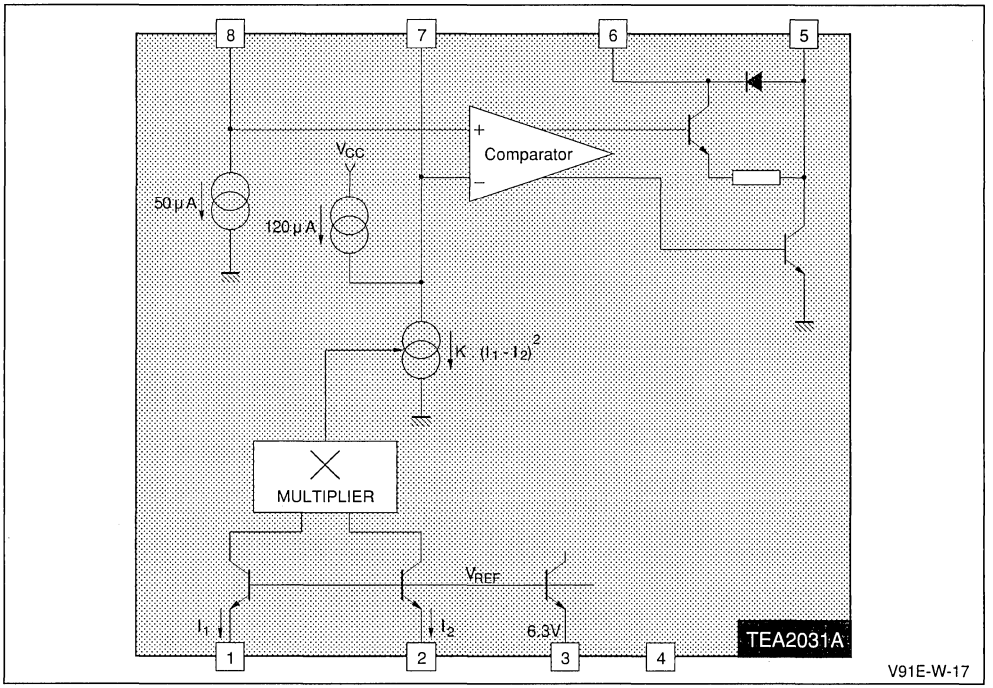
II.1 - INTRODUCTION

The TEA2031A circuit comprises (see Figure 17) : an analog multiplier that uses a frame sawtooth signal applied on Pin 1 so that the current on Pin 7 has a parabolic modulation.
This multiplier operates in current differential mode and uses a reference DC voltage, selected according to the continuous level of the sawtooth voltage, and applied on Pin 2.
The level of this DC voltage also serves to correct trapezium distortion.

- a reference voltage available on Pin 3 that can be used (via a voltage divider) to provide input 2 of the multiplier with a reference voltage.
- a current generator, producing a line frequency sawtooth signal by integrating the line flyback signal and generating current available on Pin 8.
- a comparator controlling the output stage by using the line sawtooth signal applied on its +input (Pin 8) and the parabolic signal generated by the multiplier and applied on its -input (Pin 7).

An output stage that can absorb or deliver current and comprises a diode connected to the DC voltage supply in order to limit the voltage applied on the output terminal during line flyback. This stage enables the diode modulator of the line scan circuit to be driven directly with a maximum current of 0.5A.
This maximum current that the output can absorb is not limited by the size of the transistors but by the maximum power dissipated by the package (Minidip).

Figure 17 : Block Diagram



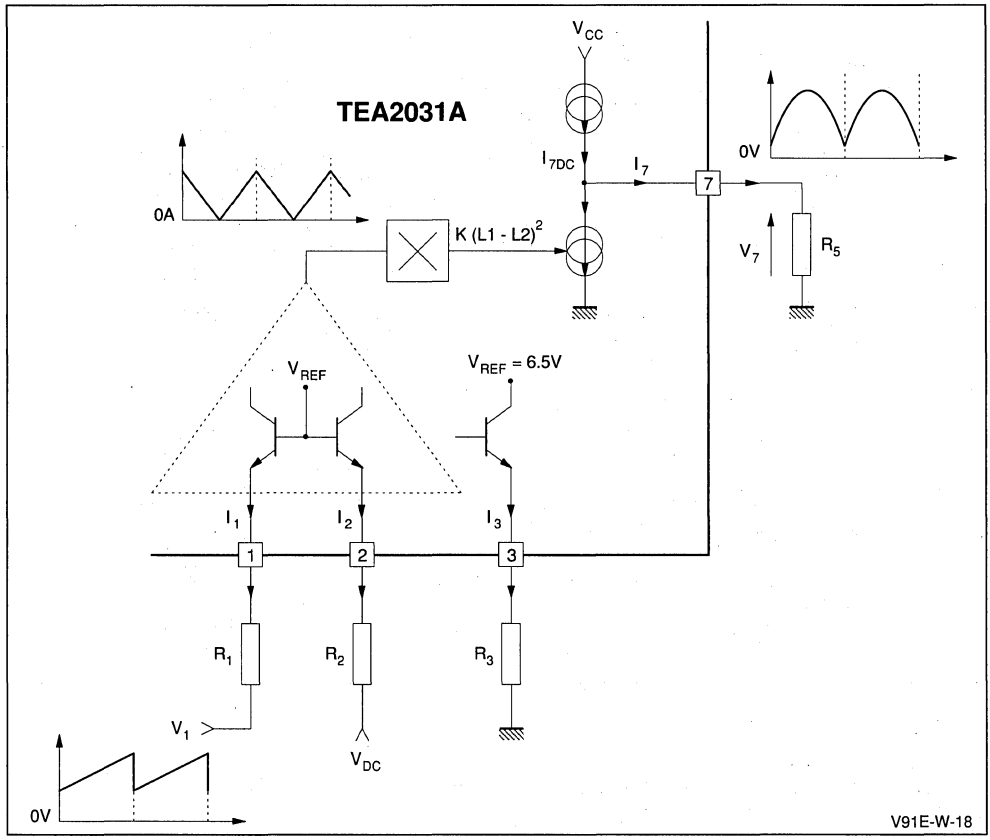
II.2 - PARABOLA GENERATION

Using a fixed continuous current and a vertical sawtooth current, the multiplier generates an output current on Pin 7 with parabolic modulation.

II.2.1 - Multiplier stage operation

The multiplier inputs (Pins 1 and 2) operate in current differential mode (Figure 18).

Figure 18 : Multiplier Stage



The output current is given by :

$$i_7 = i_{7DC} - k\,(i_1 - i_2)^2$$

i_{7DC} and k depend on the current reference on Pin 3.

Remarks : As we can see, the two inputs can be inverted and the slope of the sawtooth has no influence on the parabola shape.

II.2.1.a - Operation without keystone correction

In order to eliminate supply and thermal drift influences, R_1 is taken equal to R_2. In this case, $V_{1DC} = V_{2DC}$ (Figure 19).

II.2.1.b - Operation with keystone correction

In order to correct keystone correction, V_2 voltage becomes adjustable. In this case, the parabola shape presents a dissymmetry (Figure 20).

Figure 19 : Operation without Keystone Correction

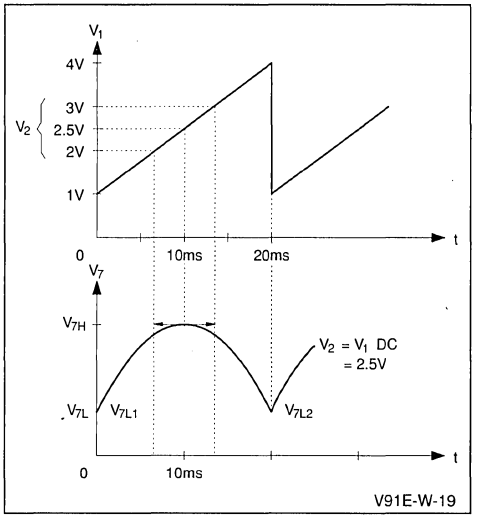
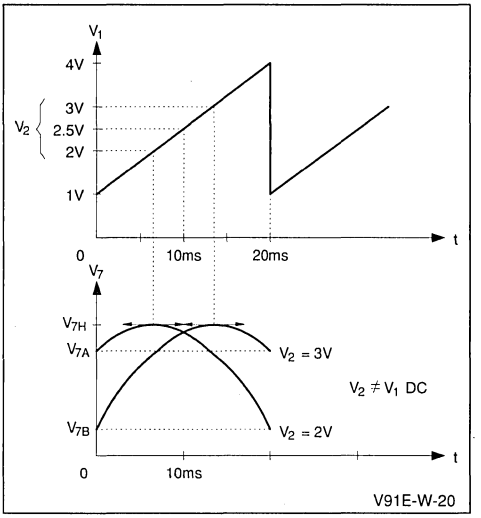


Figure 20 : Operation with Keystone Correction



II.2.1.c - Example of applications

1. Sawtooth coming from the horizontal:vertical processor (e.g. TDA8185, TEA2028B, ...)
   In this case, V_{1DC} = 2.5V (Figure 21).
   For practical reason, the DC voltage comes from internal voltage reference.Impedance value seen between Pin 3 and ground must be 22kΩ for best conditions of operation (to have the good internal current reference).
2. Sawtooth coming from the vertical output stage (Figure 22)
   In this case V_{1DC} = 0V and $R1 = R2 + \frac{1}{2} RT2$

Figure 21 : Sawtooth coming from H/V Processor

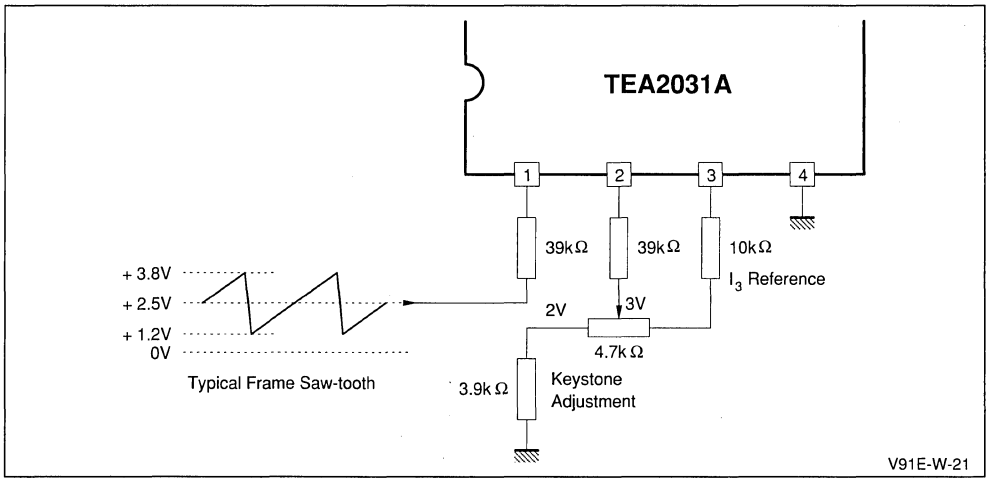
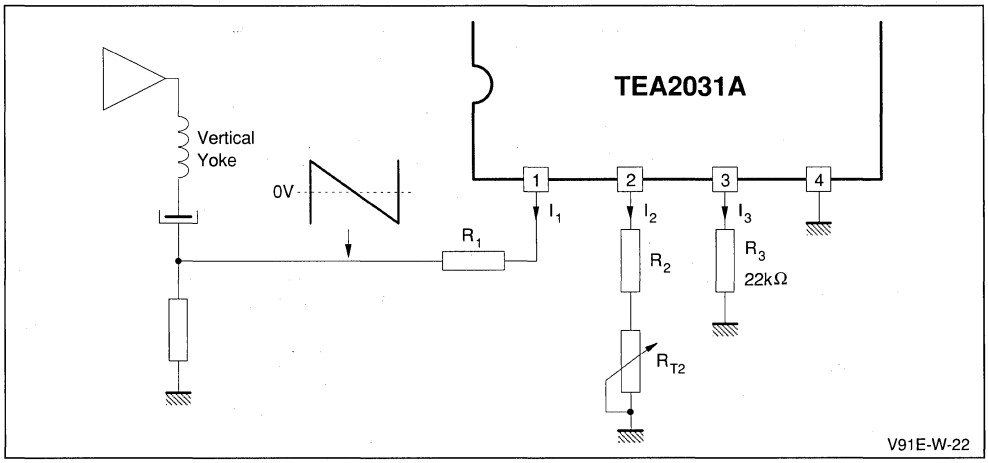


Figure 22 : Sawtooth coming from Vertical Output Stage



II.3 - LINE SAWTOOTH GENERATION

The line sawtooth signal is applied as a reference at the +input terminal of the comparator. It is obtained by integrating the line flyback and the constant current discharge of capacitor C3 in Pin 8 (Figure 23).

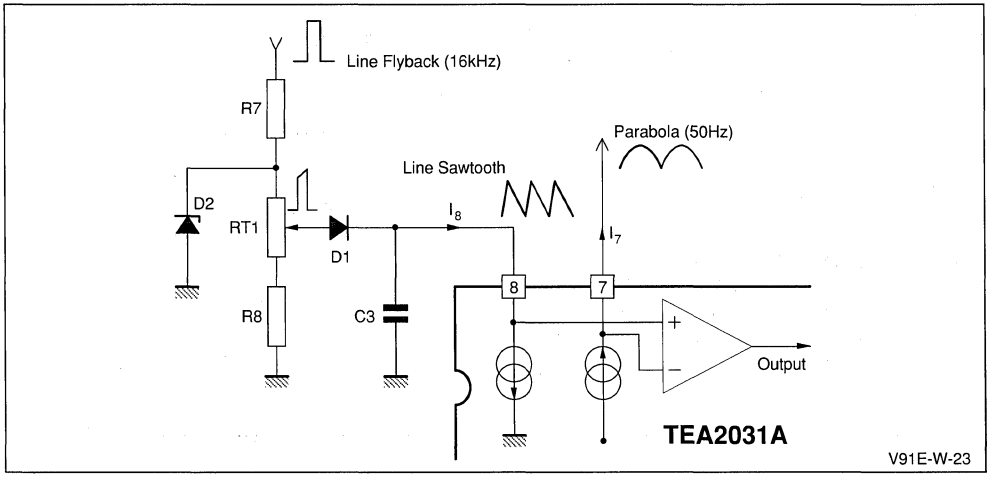
II.3.1 - Role of resistors R7, R8, RT1 and D2

By means of the voltage divider bridge comprising resistors R7, RT1 and R8, a signal that is the image of the line flyback signal applied on R7, is obtained on the slide contact of potentiometer RT1. The peak amplitude of this signal depends on the nominal voltage of the Zener diode D2 and on the adjustment of RT1.

The role of Zener diode D2 is to maintain a constant amplitude of the signal on the slide contact of RT1 whatever the variations in amplitude of the line flyback signal.

This diode D2 can be also replaced by a single diode connected to a regulated 12V or 15V power supply.

Figure 23 : Line Sawtooth Generation



II.3.2 - Role of diode D1 and capacitor C3

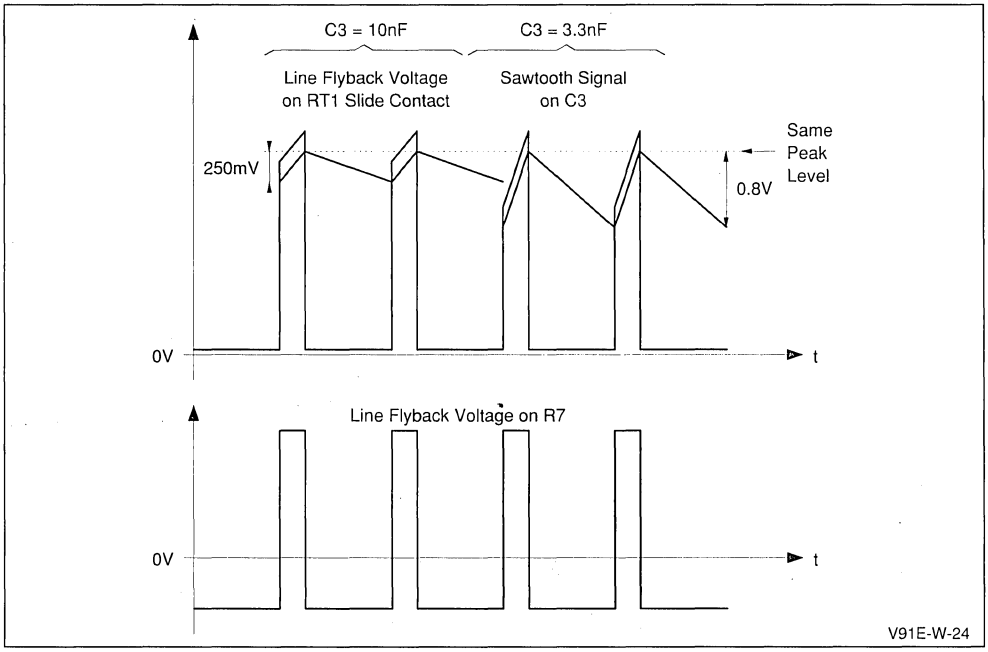
During line flyback, diode D1 rapidly charges capacitor C3 at the potential available on the slide contact of RT1.
Then during line scanning, D1 is blocked and C3 is discharged at constant current (about 50µA) through Pin 8.
The peak-to-peak amplitude of the line frequency sawtooth signal obtained in this way depends directly on the value of capacitor C3 since it is defined by the discharge current of the capacitor and the line period (Figure 24).

This amplitude can be calculated using the following equation :

$$V_{8\,(peak\text{-}to\text{-}peak)} = \frac{dt \cdot i_8}{C3}$$

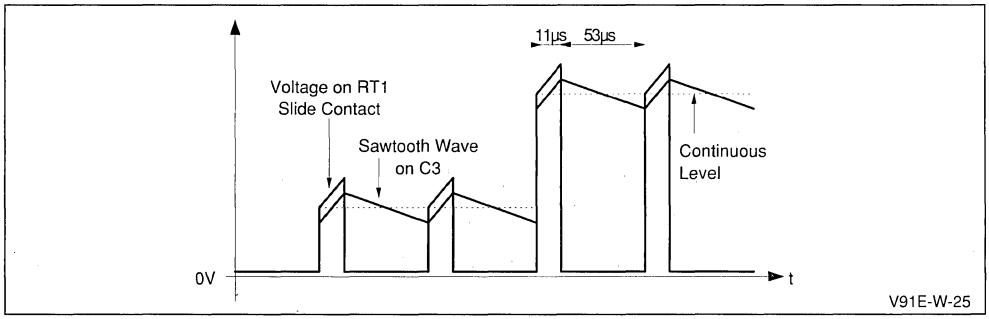
where Dt = duration of line and i_8 = current in Pin 8.

Figure 24 : Peak-to-peak Amplitude of Sawtooth Signal versus Two Different Values of C3 (with RT1 = constant)



The continuous level of this sawtooth signal is set by adjusting potentiometer RT1 (Figure 25).

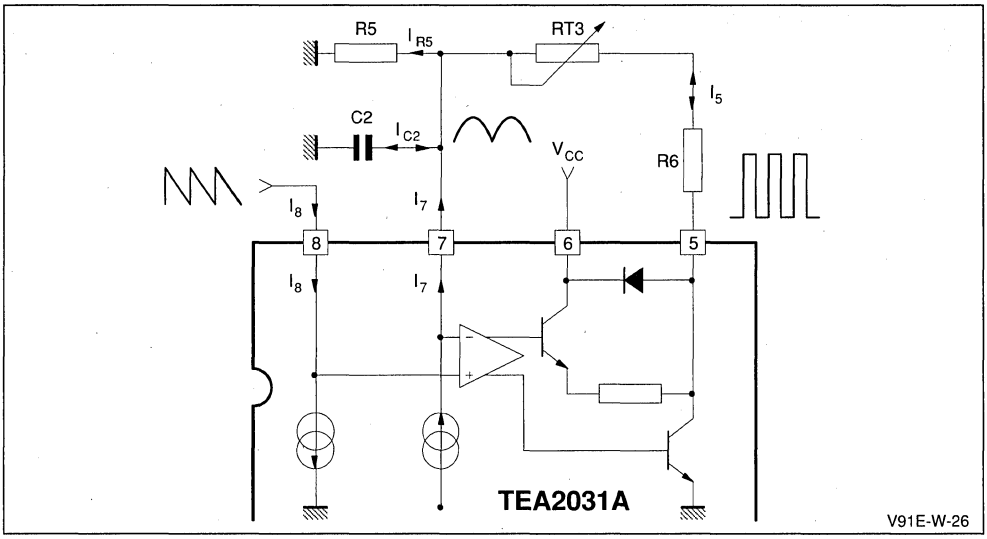
Figure 25 : Continuous Level of Sawtooth Signal for Two Different Adjustments of RT1



II.4 - OUTPUT STAGE

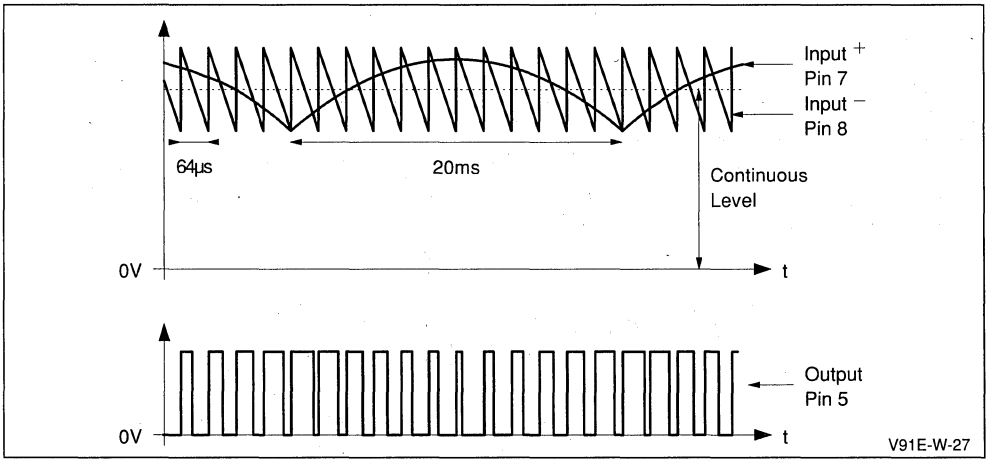
The output stage is controlled by the comparator fed by signals applied on its inputs, i.e. the sawtooth signal at line frequency on +input (Pin 8) and the parabola at vertical frequency on -input (Pin 7) (see Figure 26).

Figure 26 : Output Stage



The comparison between the 50Hz parabola and the sawtooth signal at line frequency (16kHz) produces pulses at line frequency with a duty cycle that is modulated at vertical frequency. This allows, by means of the diode modulator, the modulation of the line scanning current during each field period in order to carry out the pincushion correction (or East/West correction) (see Figure 27).

Figure 27 : PWM Output Signal (with adaptation of time scales)



The role of the filter C2 and RT3 + R6 is to suppress the line frequency of the feedback output signal.

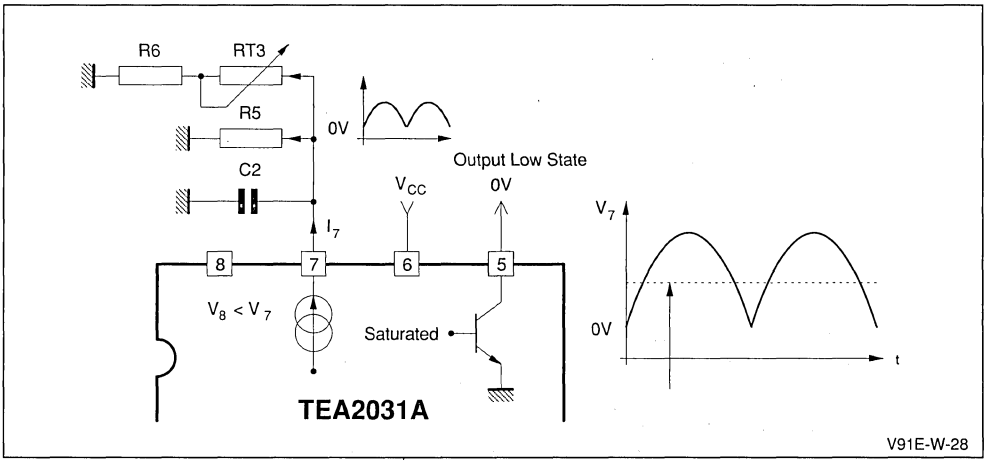
II.4.1 - Operation of the Output Stage

The operation of the output stage can be considered as 3 separate cases according to the 3 possible states of output Pin 5.

II.4.1.a - Output in the low state (Figure 28)

In this case resistances R6 and RT3 are connected to the ground, therefore they are in parallel with R5, according to the following diagram.

Figure 28 : Output in Low State



The continuous level and the peak-to-peak amplitude of the parabola are at their minimum when the RT3 value is minimum.

It is possible to calculate the voltage for a given point of the parabola (Pin 7) using the following equation :

$$V_{7b} = i_7 \cdot \frac{R5 \cdot (R6 + RT3)}{R5 + R6 + RT3}$$

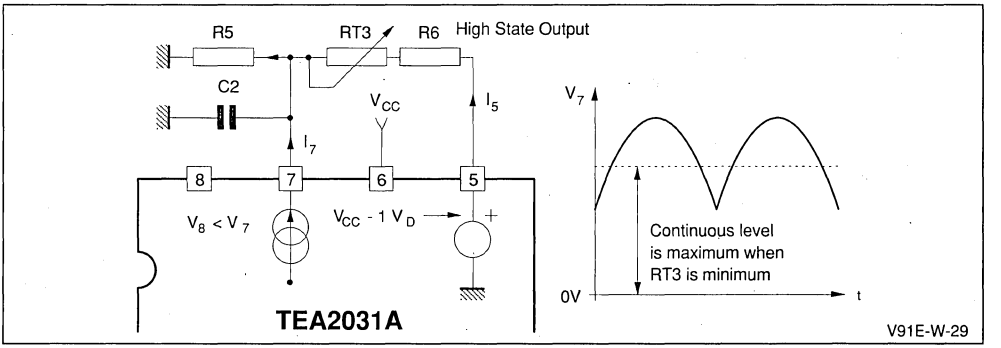
The capacitance of C2 is neglected as this capacitor is equivalent to an open-circuit at vertical frequency.

II.4.1.b - Output in the high state (Figure 29)

In this case, resistances R6, RT3 and R5 form a voltage divider bridge which returns on Pin 7 and capacitor C2 part of the continuous voltage available on the output terminal that is added to the parabola voltage.

The equivalent circuit diagram is the following :

Figure 29 : Output in High State



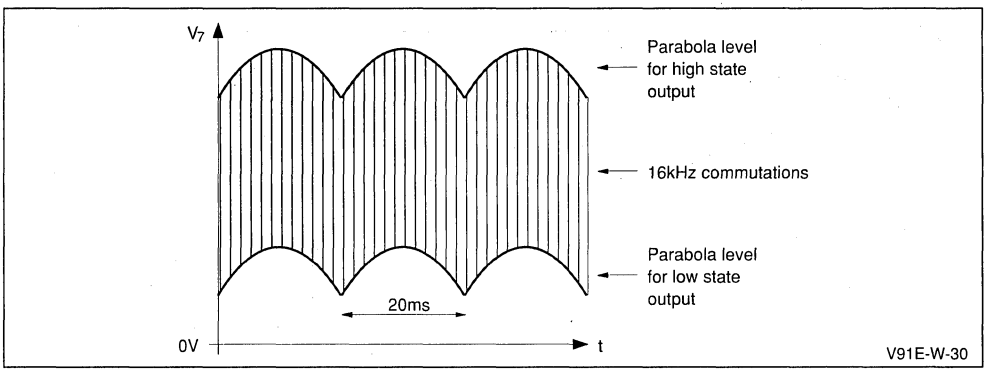
It is possible to calculate the voltage for a given point of the parabola (Pin 7) with the following equation :

$$V_{7h} = i_7 \cdot \frac{R5 \cdot (R6 + RT3)}{R5 + R6 + RT3} + V_5 \cdot \frac{R5}{R5 + R6 + RT3}$$

II.4.1.c - Output with commutation

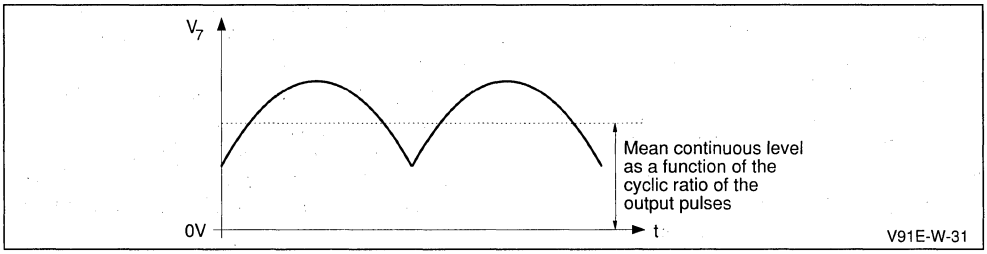
In this case and if capacitor C2 is eliminated, Figure 30 gives the signal obtained on Pin 7. It corresponds exactly to the levels and amplitudes of the parabolas for output in the high state and the low state, linked by 16kHz commutations.

Figure 30 : Output with Commutation (without C2)



In normal circuit configuration, capacitor C2 is connected and constitutes a filter with R6 and RT3. The preceding signal is filtered and is transformed into the signal shown in Figure 31.

Figure 31 : Output with Commutation (with C2)



The 16kHz line frequency component has disappeared in the signal and only the 50Hz parabola remains, but slightly modulated at line frequency by the C2 charge when the output is in the high state, and by the C2 discharge when the output is in the low state; this gives a tiny triangular modulation signal.

So the continuous level of the parabola depends only on the cyclic ratio of the output pulse train. This level can be calculated by means of the following equation : $V_{mean} = M \cdot V_{7h} + (1 - M) \cdot V_{7b}$

where

M : output pulse cyclic ratio

V_{7h} : mean level on Pin 7, output blocked in the high state

V_{7l} : mean level on Pin 7, output blocked in the low state

We see that, when the cyclic ratio increases, the continuous level of the parabola also increases and approaches its maximum level when the output is in the high state. Conversely, when the cyclic ratio decreases, the continuous level of the parabola also decreases since it approaches its minimum continuous level when the output is in the low state.

II.4.1.d - Conclusion

For a given parabolic current i_7, the parabola peak-to-peak amplitude depends only on resistance values R5,R6 and RT3. Therefore by adjusting RT3, it is possible to obtain a more or less pronounced parabola and so adjust the importance of pincushion correction.

The continuous level of the parabola depends principally on the mean cyclic ratio at the output, and much less on the adjustment of RT3.

II.4.2 - Operation in association with the diode modulator

In the majority of cases, the system operates by drawing more or less high current from the modulator through the connecting inductor. The current through terminal Pin 5 of TEA2031A is entering into the circuit. It flows, either to the ground when the output is in the low state, or to V_{CC} through the internal diode when the output is in the high state and the output voltage tends to exceed V_{CC}. The circuit can also produce current.

Figure 32 : Operation with Diode Modulator

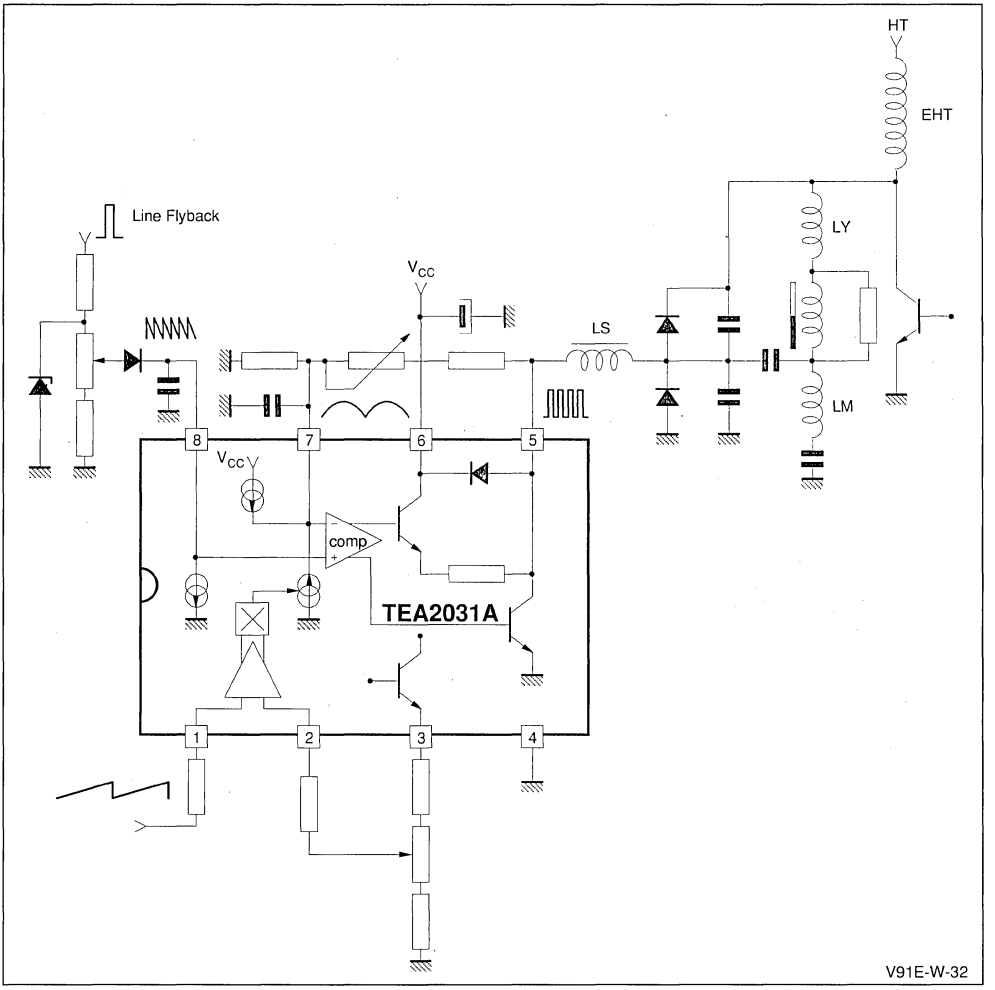
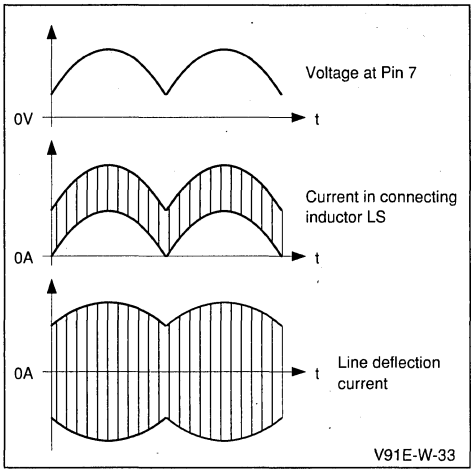


Figure 33 : Output Oscillagrams



II.5 - SELECTION OF THE VALUES OF CAPACITORS C2 AND C3

Correct operation of TEA2031A depends partly on the choice of these values for two reasons :

- for a given amplitude of the parabola, the importance of final pincushion correction at the output of TEA2031A is determined by defining, by means of C3, the amplitude of the line sawtooth wave.
- the absence of oscillation at circuit output is controlled through adjustment of the value of C2 as described below.

II.5.1 - Selection of C3

As seen before (chapter II.3.2), the value of C3 and only this value (in the limits of the available voltage on the slider of RT1) can fix the value for the amplitude of the line sawtooth wave. Now this amplitude must be greater than the parabola amplitude (Pin 7) but not so far in order to have a correction amplitude sufficient but permitting also an horizontal amplitude adjustment :

- if the line sawtooth wave and the parabola have the same amplitude, the pincushion correction is maximum but the horizontal amplitude adjustment range is non-exutent
- if the line sawtooth amplitude is much greater than the parabola's one, we will have a large range for the horizontal amplitude adjustment, but it will be to the detriment of the pincushion correction amplitude.

Once the desired line sawtooth amplitude has been fixed, we can calculate the value of C3 with the following formula

$$C3 = \frac{Dt \cdot i_8}{V_8}$$

where

Dt : line scan duration (around 53µs)

i_8 : Pin 8 current (around 50µA)

V_8 : line sawtooth peak-to-peak amplitude (Pin 8)

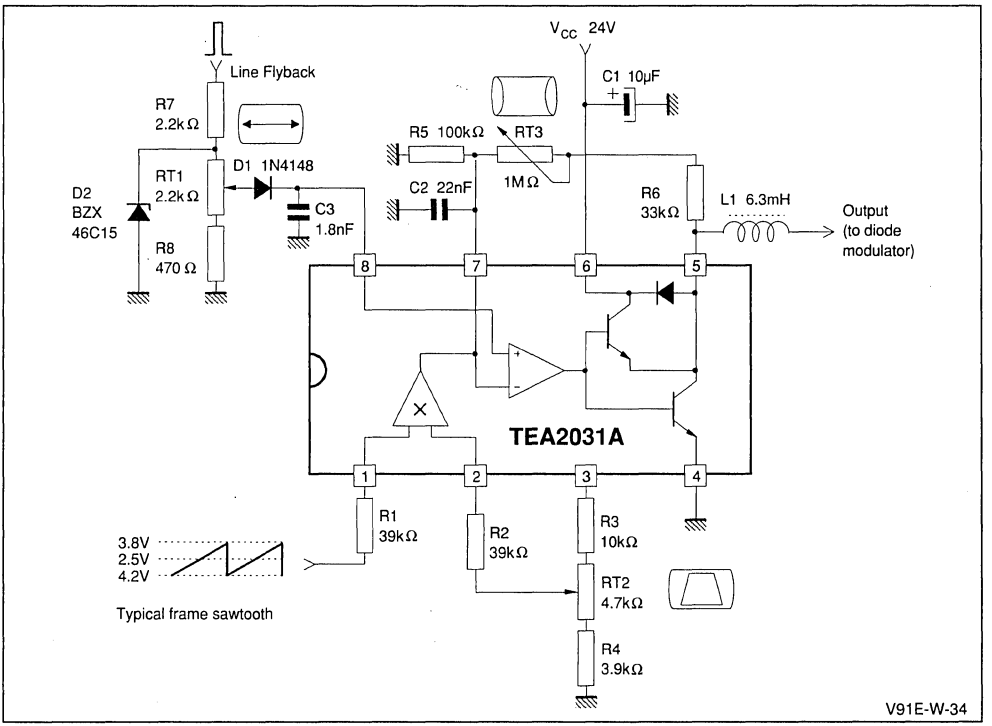
II.5.2 - Selection of C2

The selection of C2 is related to the values of R5, R6 and RT3. The value of C2 must be large enough to avoid any risk of oscillations at output for the entire range of adjustment of potentiometers RT1 and RT3. The value of C2 must be small enough not to influence the shape of the vertical frequency parabola.

II.6 - APPLICATION EXAMPLE

A typical application diagram is given in Figure 34.

Figure 34 : Typical Application



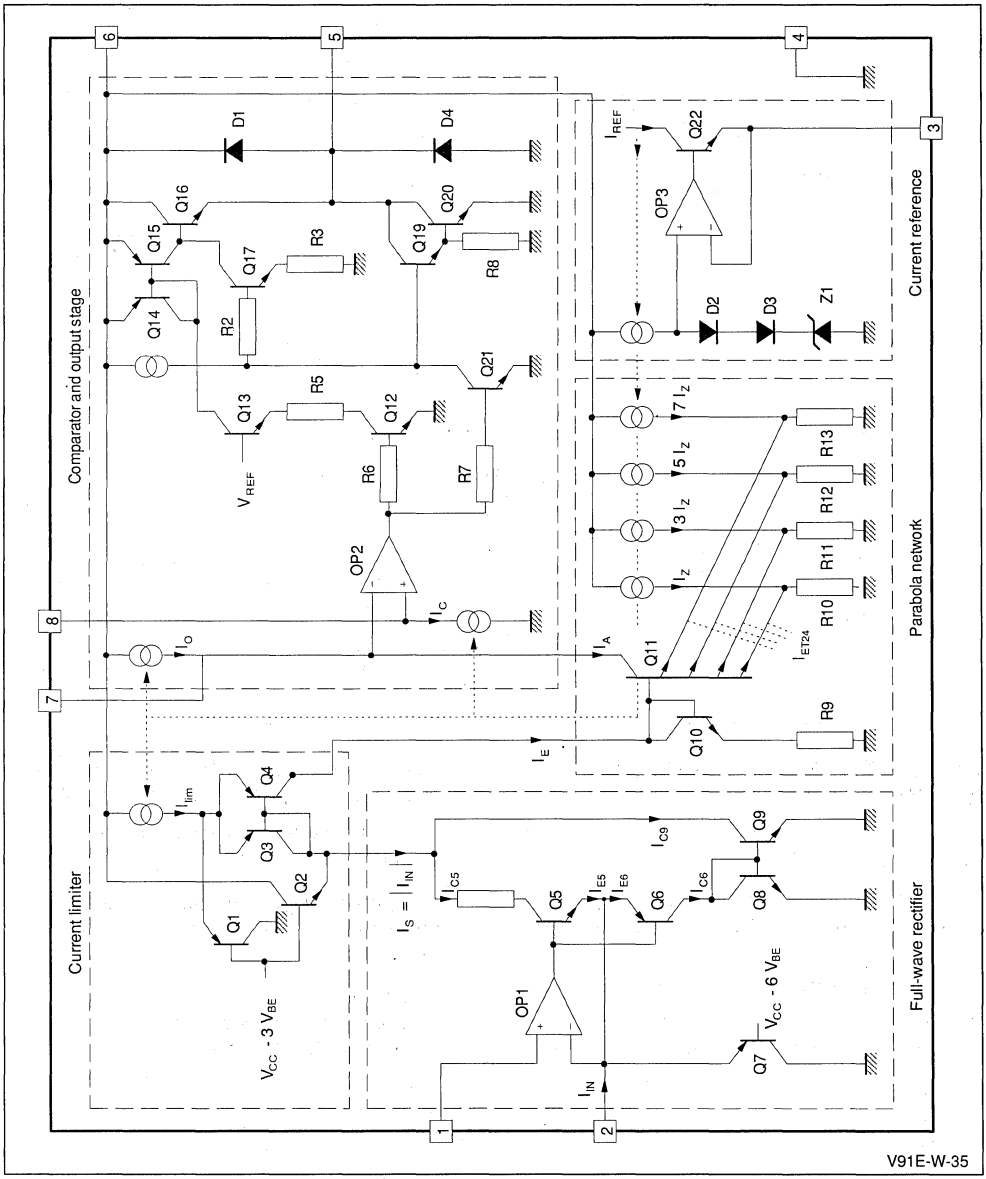
III - TDA4950 - TDA8145 GENERAL DESCRIPTION

III.1 - INTRODUCTION

The TDA4950 and TDA8145 consist mainly of 5 parts as seen in the simplified circuit diagram (Figure 35).

1. Full-wave rectifier for the input current I_{IN}.
2. Current limiter in order to limit the rectified current I_{IN} to the maximum value of 40µA (with this functional block a suppression of the parasitic parabola is possible, see chapter I.4).
3. Parabola network producing the current $I_A = k(I_{IN})^2$ (k = constant).
4. Comparator and output stage working as a pulse-width modulator for driving the diode modulator.
5. Voltage reference and current reference which produces the reference current I_{REF} via external resistor RI between Pin 3 and Ground.

Figure 35 : Simplified Circuit Diagram for TDA4950 - TDA8145



III.2 - DESCRIPTION

Let us consider the blocks in detail :
The input amplifier OP1 drives the transistor Q5 or Q6. They offer two different signal paths, depending on the sign of the input current I_{IN}.

Assuming that I_{IN} is negative, the feedback loop is closed via the transistor Q5 and the output current I_{C5} is given by

$$I_{C5} = I_{E5}\left(\frac{\beta_5}{1+\beta_5}\right) = -I_{IN}\left(\frac{\beta_5}{1+\beta_5}\right)$$

where β_5 is the current gain of the transistor Q5. β_5 can be assumed to be more than 100, so the mismatching between I_{C5} and I_{IN} is less than 1%.

For a positive current I_{IN} the output voltage of OP1 decreases : Q5 is switched off the current I_{IN} is the emitter current I_{E13} of Q6.

Its collector current I_{C6} is given by

$$I_{C6} = I_{IN}\left(\frac{\beta_6}{1+\beta_6}\right)$$

Since the maximum input current is 40µA, the current gain of this PNP transistor is still high enough to give a reasonable small error. This current biases the current mirror Q8 and Q9. A good matching between the current I_{C8} and I_{C9} must be provided. Thus the current I_S is given by

$$I_S = \begin{cases} -I_{IN}\left(\frac{\beta_5}{1+\beta_5}\right) & I_{IN} < 0 \\ +I_{IN}\left(\frac{\beta_6}{1+\beta_6}\right) & I_{IN} > 0 \end{cases}$$

Neglecting the base current of Q6 and Q5, I_S is nearly the absolute value of I_{IN}.

Note that for both signal paths, the OP1 has a feedback factor of 1. This means OP1 must be frequency compensated for unity gain.

The transistors Q3 and Q4 work as a normal current mirror if the current I_S plus I_E is smaller than the current I_{lim} :

$$2\,I_S < I_{lim}$$

In this case the excess current is shunted via the PNP transistor Q1.

If the current I_S becomes higher

$$I_S > I_{lim}/2$$

the transistor Q1 switches off and Q2 picks up the current I_S from the rectifier which exceeds the maximum value of $I_{lim}/2$.

Using the proposed reference resistor RI between Pin 3 and Ground (11kΩ) the current I_E can be described with

$$I_E = \begin{cases} I_{IN} & I_{IN} < 40\mu A \\ 40\mu A & I_{IN} > 40\mu A \end{cases}$$

The parabola network produces an output current I_A which is approximately a parabola : $I_A = k\,I_E^2$

The parabolic behaviour I_A is obtained via piecewise linear approximation. For this purpose the identical resistors R_Z are connected with the four emitters. The four different biasing currents i_Z, $3i_Z$, $5i_Z$, $7i_Z$ yield four different threshold voltages, so the four emitter currents of Q11 are switched stepwise. A schematic illustration of the single emitter currents I_{EQ11} (1...4) of Q11 as a function of the current I_E is given in Figure 36.

Due to the exponential character of the emitter current as a function of the base emitter voltage, the output current I_A is smoothed.

For designing the values of R_Z and i_Z of this parabola network we must take a compromise between the smoothing effect and the temperature dependence. Small values of R_Z and i_Z yield small threshold voltages for the 4 emitters of Q11. This means a good smoothing of the edges, but a worse temperature dependence.

Large values of R_Z and i_Z yield the opposite result. Practical experiences show that a value of 0.5V for the 4th emitter (R13 $7i_Z$) for I_{IN}= 0 gives an acceptable cmpromise.

Due to different values of resistor R_Z, the TDA8145 is adapted to flat square tubes (see Figure 37 for the two different shapes of the parabola).

Figure 36 : Transfer Characteristic of the Parabola Network

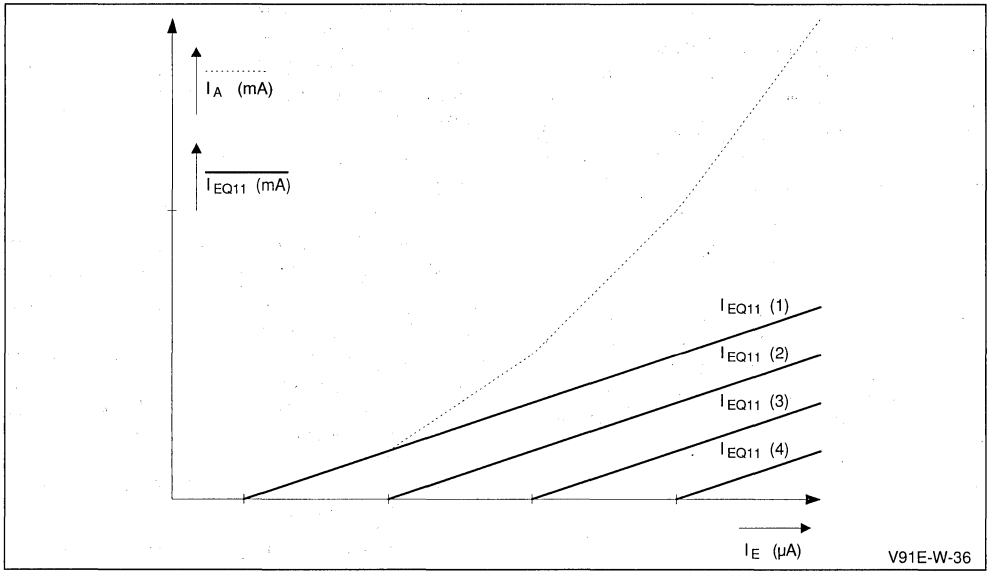
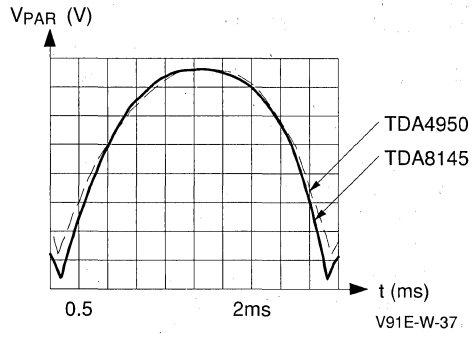


Figure 37 : Parabola Shapes for TDA4950 and TDA8145



The parabolic output current I_A produces a corresponding voltage drop across an external resistor between Pin 7 and Ground (18kΩ). The additional constant current source I_0 shifts the D.C. voltage level to achieve an appropriate operating point of the comparator. Its non-inverting input is connected with a horizontal saw-tooth voltage. For this purpose an external capacitor is connected with Pin 8 and Ground which is discharged with the internal current source I_C. It will be charged with the positive flyback pulses produced in the line transformer during the flyback time.

Due to the linear saw-tooth voltage on Pin 8 this comparator works as a pulse-width modulator.
The output of this comparator controls the output stage. If the output of the comparator OP2 is high, Q21 and Q12 are saturated. Therefore, the Darlington output transistor Q19, Q20 is switched off. The transistor Q13 and the resistor R5 acts as a current source biasing the current mirror Q14, Q15. The transistor Q16 is switched on.

If the output of OP2 becomes low, Q12 and Q21 are switched off. In this case the current in Q14 and Q15 dissappears and Q16 is switched off. Synchronously the darlington stage Q19 and Q20 is saturated.

In order to achieve a fast commutation from Q16 to Q19/Q20 an active discharging of Q16 is provided with the aid of the transistor Q17.
During a normal operation range if the output current i_{OUT} is positive, only the Darlington stage (Q19, Q20) and the diode D1 are necessary to drive the external inductor. With the aid of Q16 and the intrinsic substrate diode D4 the output current i_{OUT} can become negative, too; so that the modulation range of the diode modulator becomes larger.

The Zener diode Z1 serves as the voltage reference. With the aid of the diodes D2 and D3, a good temperature compensation can be achieved.
Using an external resistor of R_I = 11kΩ between Pin 3 and Ground we get an accurate and temperature independent current reference to bias the internal current sources.

III.3 - APPLICATION

A standard application diagram is given in Figure 39.
Pin 2 is biased from a linear saw-tooth voltage, the resistor R_{IN} produces the input saw-tooth current. The non-inverting input (Pin 1) is connected with an adjustable voltage (keystone correction). With the aid of this trimmer, the symmetry of the parabola can be adjusted in order to correct a trapezoidal error in the colour picture tube. A further adjustment trimmer is responsible for the picture width and influences only the DC-level of the comparator input (Pin 8). (Since the discharging current sink on Pin 8 is constant, the amplitude of the horizontal saw-tooth voltage (V_{PP}) remains constant).

The thrid trimmer is in the feedback path and is responsible for the parabola correction factor. With the aid of this trimmer the distortion on the screen can be changed from pillow-distortion up to an over-correction (tun-distorsion).

For some applications the keystone adjustment trimmer is not necessary (small trapezoidal error of the picture tube). In this case, a symmetric parabola should be produced.

This can easily be obtained by AC-coupling the input (Pin 2) as seen in Figure 38.

Figure 38 : AC-coupled Vertical Saw-tooth Voltage, no Keystone (trapezoidal) Correction

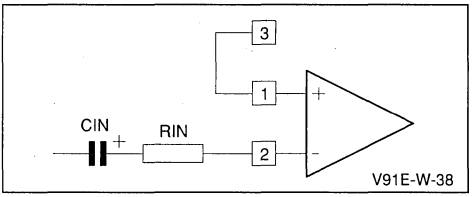
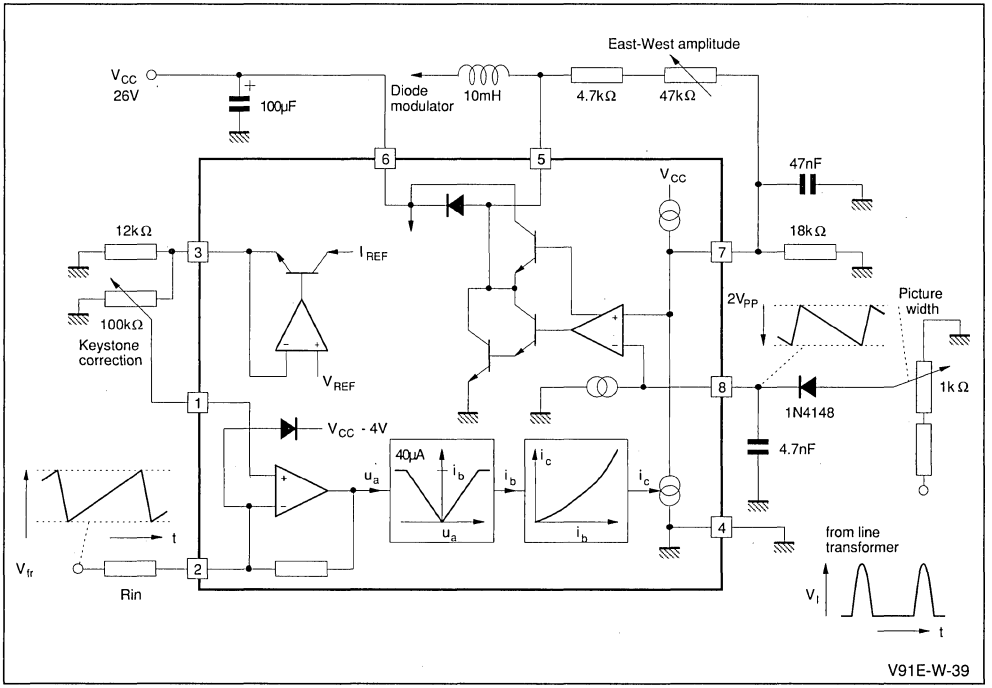


Figure 39 : Standard Application Diagram of TDA4950 and TDA8145



In order to avoid any distorsion, the time constant $C_{IN} \cdot R_{IN}$ should be at least 10 times larger than the time period ($C_{IN} \cdot R_{IN} > 10 \cdot 20ms$). On the other hand a too large time constant yields an undesired bouncing effect in the East/West correction.
The DC voltage on Pin 1 is arbitrary.
For the sake of simplicity, connect Pin 1 with Pin 3. Another possible application with parasitic parabola suppression is given in Figure 40.

The input current into Pin 2 is generated via the voltage drop on R_M. Due to the common mode rejection of the input operational amplifier, the voltage change during the vertical scan time (sawtooth voltage) has nearly no effect. During the flyback time, a positive pulse (> V_{CC}) is present on Pin 1 and Pin 2. With this flyback pulse the current limitation in the parabola generation circuit is activated and limits the parabola amplitude. Since the flyback time is relatively long, this limitation is necessary to suppress the parasitic parabola (see chapter I.4).

IV - TDA8146 GENERAL DESCRIPTION

IV.1 - INTRODUCTION

The TDA8146 was designed for TV and monitor sets with various types of picture tubes, where a programmable parabola is mandatory. The complete block diagram is shown in Figure 41.

The following features confer to this IC an all-purpose suitability :

- programmable parabolic current generator
- parasitic parabola suppression during vertical flyback
- output sink current up to 800mA and source current up to 100mA
- vertical current sense inputs ground compatible

Figure 40 : Application of TDA4950 and TDA8145 with Parasitic Parabola Suppression

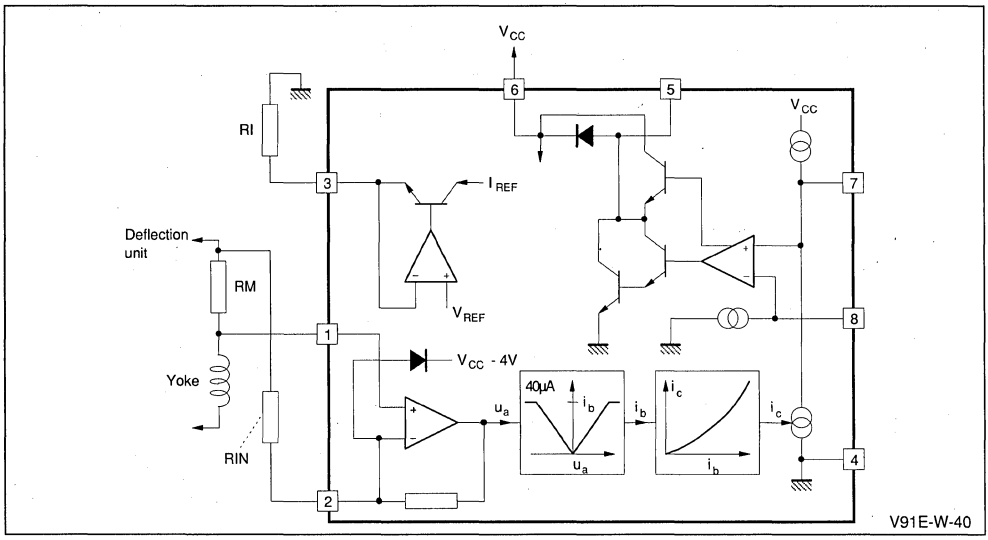
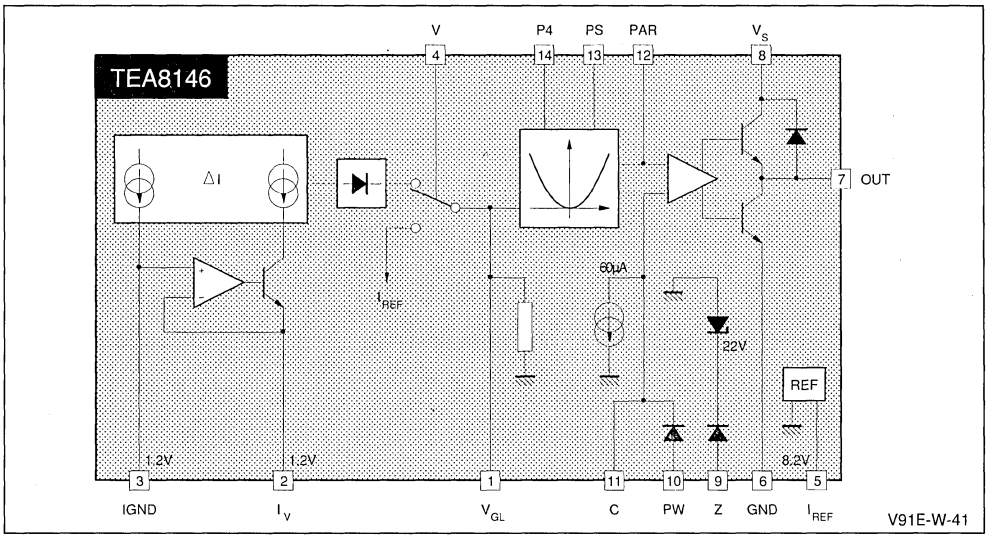


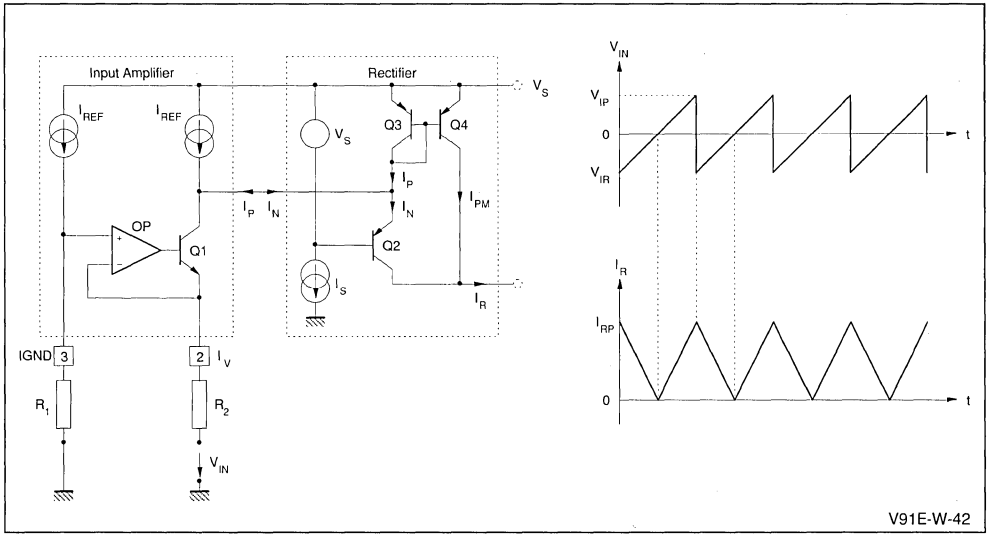
Figure 41 : Block Diagram



IV.2 - INPUT AMPLIFIER AND RECTIFIER

The input circuitry (Figure 42) is designed for a common mode range up to 12V.

Figure 42 : Input and Rectifier Principle Diagram



The voltage drop on R1 gives on I_{GND} (Pin 3) : $V_{R1} = R1 \cdot I_{REF}$

The operational amplifier OP regulates the current through R2, thus :

$I_{R2} = (V_{R1} - V_{IN}) / R2 = (R1 \cdot I_{REF} - V_{IN}) / R2$

For $V_{IN} > 0$, we note the output current of the input amplifier I_N :

$$I_N = I_{REF} - I_{R2} = I_{REF} - (R1 \cdot I_{REF} - V_{IN}) / R2$$

For $V_{IN} < 0$, we note the output current of the input amplifier I_P :

$$I_P = I_{R2} - I_{REF} = (R1 \cdot I_{REF} - V_{IN}) / R2 - I_{REF}$$

The rectifier is formed by Q2, Q3 and Q4. For $V_{IN} > 0$, I_N flows through Q2 to the rectifier output, thus $I_R = I_N$.
For $V_{IN} < 0$, I_P flows through Q3 from V_S into the output of the input amplifier. Q4 reflects the I_P current, thus the rectifier output currrent will be $I_R = I_{PM} = I_P$.

If the sign convention of I_R is considered, we have :

$$I_R = \left| \frac{(R1 \cdot I_{REF} - V_{IN})}{R} - I_{REF} \right| = \left| I_{REF} \left(\frac{R1}{R2} - 1 \right) + \frac{V_{IN}}{R2} \right|$$

In our case, R1 = R2 = 10kΩ and $I_{REF} = 120\mu A$

Thus, $I_R = \left| \frac{V_{IN}}{R2} \right|$

If V_{IN} is a symmetrical saw-tooth with GND as the average value and 1.6 $V_{peak\text{-}to\text{-}peak}$, the rectified peak current will be :

$$I_{RP} = \frac{0.8}{10 \cdot 10^{-3}} = 80\mu A$$

IV.3 - VERTICAL CLAMPING

To avoid the parasitic parabola during the vertical flyback time a vertical clamp circuit was used.

The vertical clamping principle is presented in Figure 43.

The rectified sawtooth current I_R Flows through D2 to the output.

When V goes over V_S, Q1 switches off and Q2 on. I_{REF} flows now through D1 to the output and I_R through Q2 to the ground. $I_{RC} = I_{REF}$ is now the clamped value of the output current.

IV.4 - REFERENCE AND STARTING CIRCUIT

Figure 44 presents the complete voltage and current reference circuitry.

The reference current is $I_{REF} = \frac{8.2V}{100k\Omega} = 82\mu A$

To guarantee the start of the device, it is necessary to choose the value of the resistor R5 in order to have a minimum current of 56μA.

Figure 43 : Vertical Clamping Principle Diagram

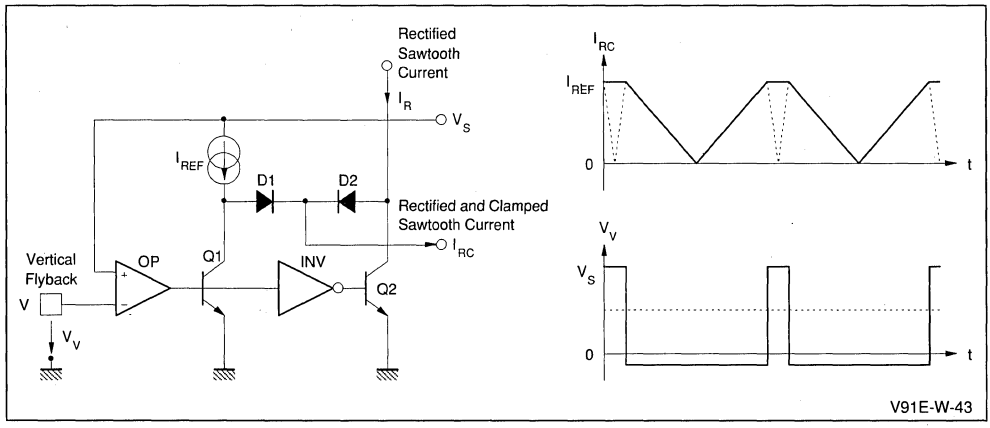
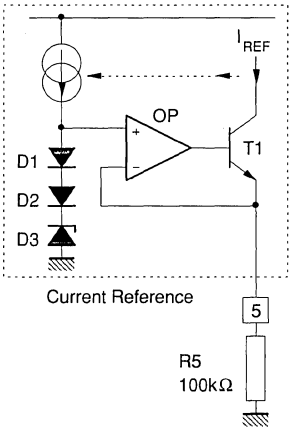


Figure 44 : Reference and Starting Circuit

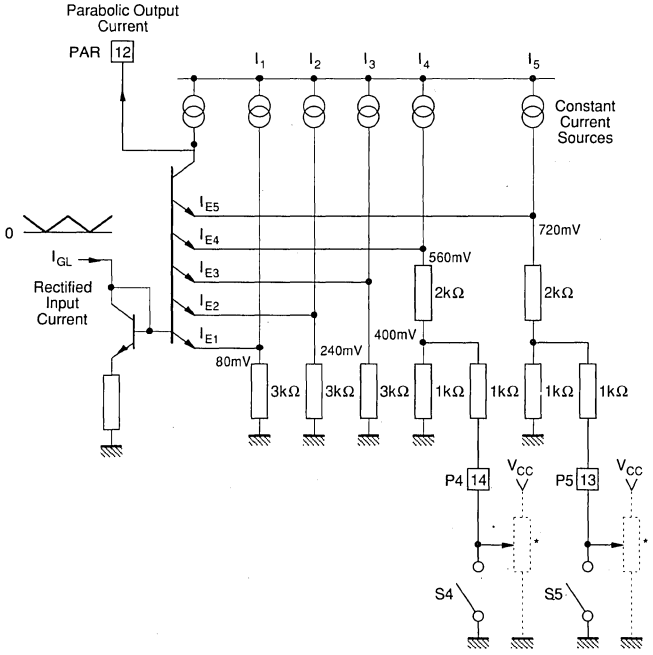


V91E-W-44

IV.5 - PARABOLA GENERATOR

Figure 45 presents the simplified circuit diagram of the parabola generator.

Figure 45 : Parabola Generation



Note : * It is possible to replace the switches S4 and S5 by this configuration in order to have a continuous shape variations.

V91E-W-45

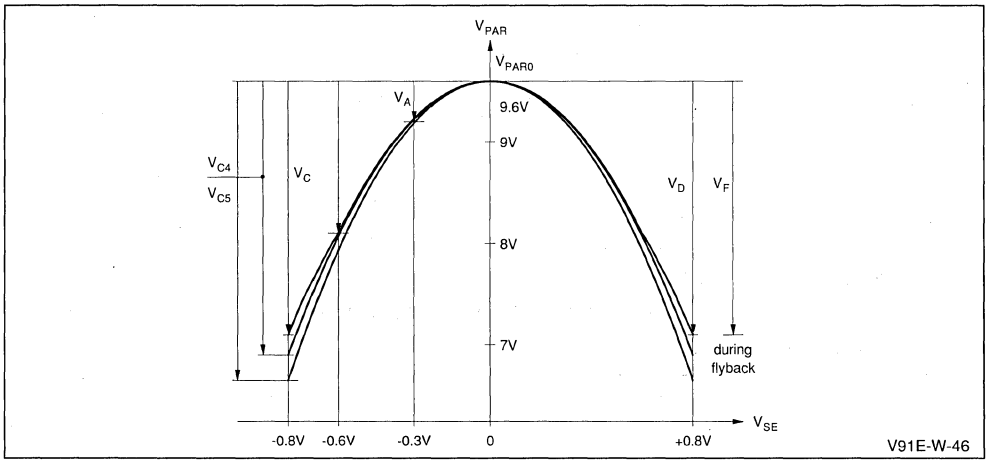
The parabolic behaviour of the parabola output current is obtained via piecewise linear approximation.
Two external pins permit an external adjustment of the parabola shape (these pins can be connected to ground or to resistors).

The parabolic output current on Pin 12 Produces a corresponding voltage drop across an external resistor between Pin 12 and ground.

As it can be seen in Figure 46 the parabola can be corrected in the following limits :

$V_{C5}/V_C = K5 = 1.07$ with Pin 5 to GND
$V_{C4}/V_C = K4 = 1.17$ with Pins 4 and 5 to GND

Figure 46 : Parabola Correction

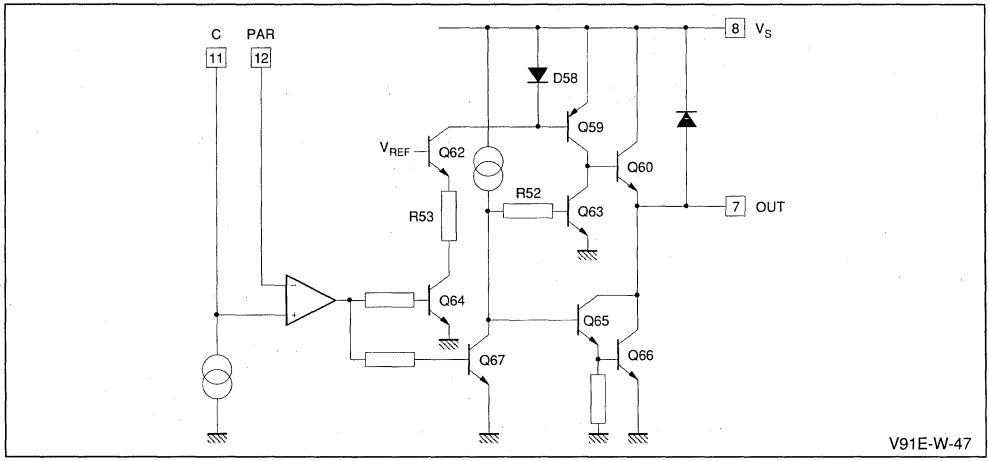


An application specific correction can be thus obtained for various picture tube types.

IV.6 - PULSE-WIDTH MODULATOR AND OUTPUT

The simplified diagram of the pulse-width modulator and output is presented in Figure 47.

Figure 47 : Pulse-width Modulator and Output



The non-inverting input of the comparator (Pin 11) is connected to a horizontal saw-tooth voltage. An external capacitor connected on Pin 11 is charged during the flyback time and then discharged by the internal current source generating the saw-tooth voltage.

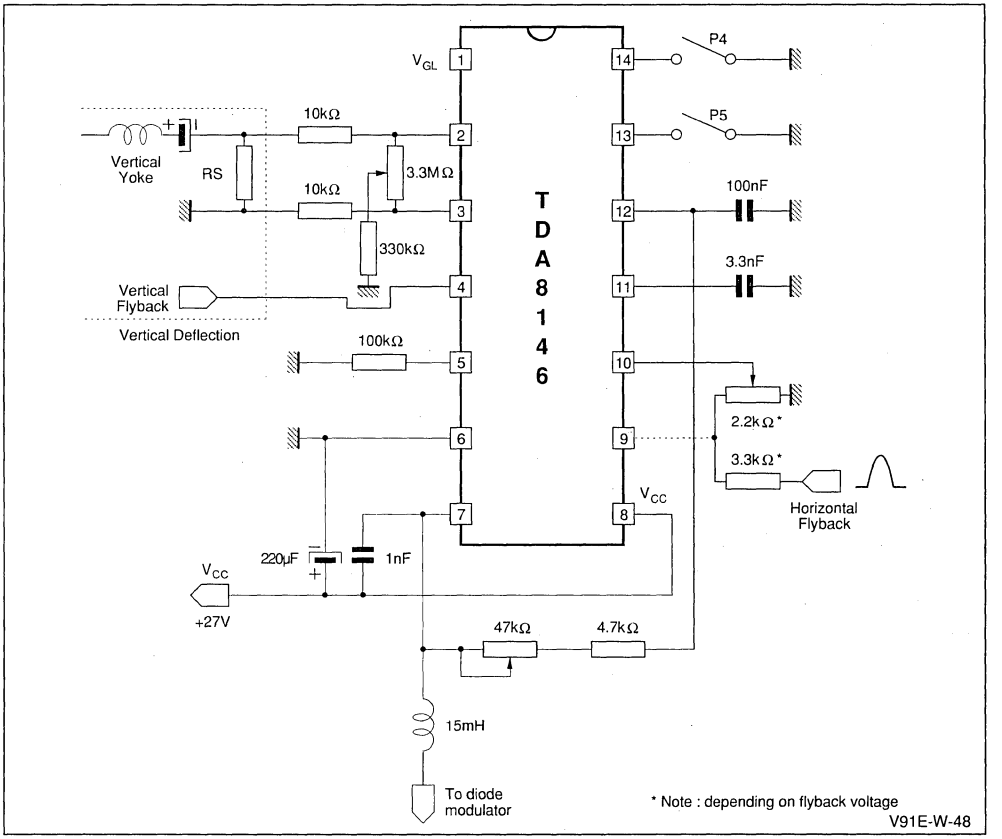
Due to the linear saw-tooth voltage on Pin 11, the comparator works as a pulse-width modulator. The output of this comparator controls the output stage. If the output of the comparator is high, Q67 and Q64 are saturated. The Darlington output configuration Q65/Q66 is switched off. Q62 acts together with R53 as a current source, biasing the current mirror Q58/Q59. The transistor Q60 is switched on.

If the output of the comparator becomes low, Q64 and Q67 are switched off. The current through D58/Q59 disappears and Q60 is switched off. Synchronously the Darlington stage Q65/Q66 is saturated. In order to achieve a fast commutation, an active discharging of the Q60 base charge is provided with the aid of Q63.

IV.7 - APPLICATION

An application diagram is presented in Figure 48. The internal Zener configuration on Pin 9 can be useful in certain application.

Figure 48 : Application Diagram

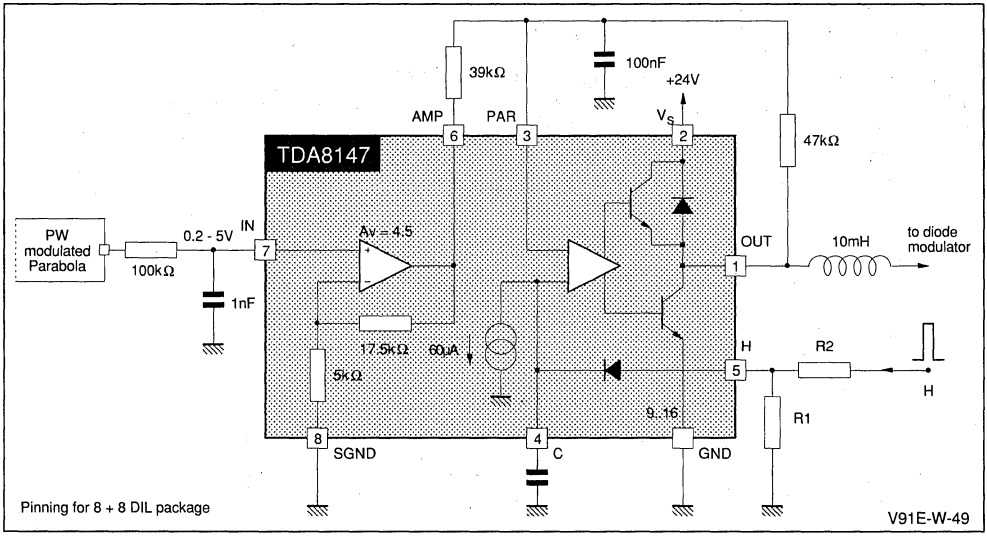


V - TDA8147 GENERAL DESCRIPTION

V.1 - INTRODUCTION

The TDA8147 was designed as an interface IC between the digital circuitry and the diode modulator in digital chassis. The complete block diagram is shown in Figure 49.

Figure 49 : TDA8147 Block Diagram



V.2 - INPUT AMPLIFIER

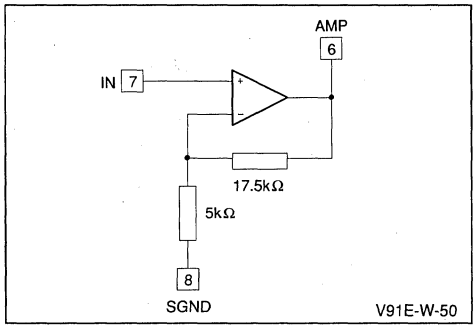
The pulse-width modulator of the TDA8147 is working with input voltages from 1V to 23V. To have the same range for the parabola voltage an input amplifier is necessary. Digital TV sets deliver an analog parabola or a PWM-signal with small amplitude (2V to 3V).

An additional signal ground (SGND Pin) separates the digital ground from the deflection circuit ground.

The internal feedback loop of the amplifier gives a voltage gain

$$A_V = \frac{17.5}{5} + 1 = 4.5 \text{ (see Figure 50)}$$

Figure 50 : Input Amplifier



V.3 - VOLTAGE REFERENCE AND STARTING CIRCUIT

The voltage reference and starting circuit have the same configuration as for the TDA8146 (see paragraph IV.4).

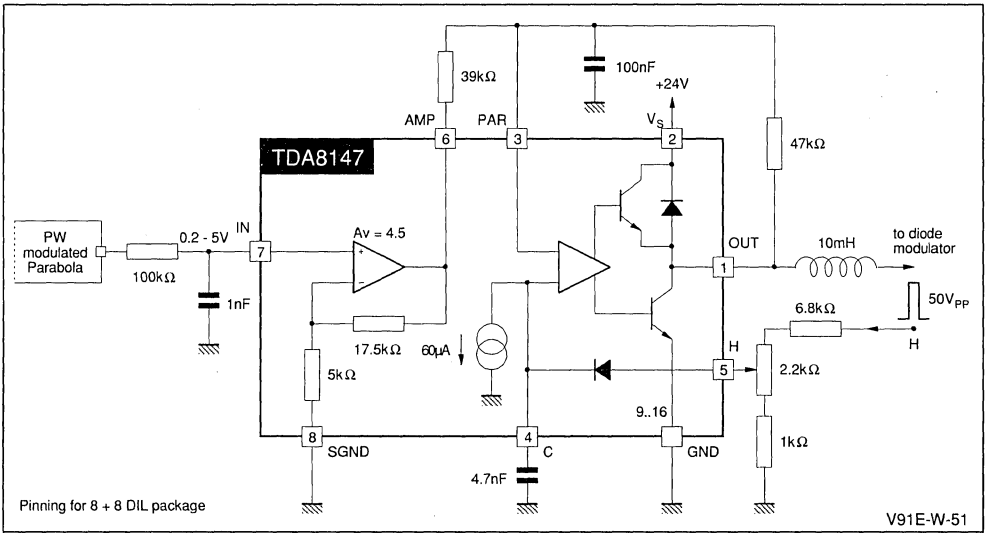
V.4 - PWM MODULATOR AND OUTPUT

The PWM modulator (Figure 51) has the same configuration as for the TDA8146. So see paragraph IV.6 for explanation.

V.5 - APPLICATION

A Standard application diagram is given in Figure 51.
Since all the adjustment of the parabola are made by the digital processor, only the feedback loop of the PWM modulator must be carefully designed. The TDA8147 is well-suited for new TV concepts with 32kHz line frequency.

Figure 51 : Application Diagram



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2028-2029

By : J-M.MERVAL / B. D'HALLUIN

SUMMARY

SUMMARY *(continued)*

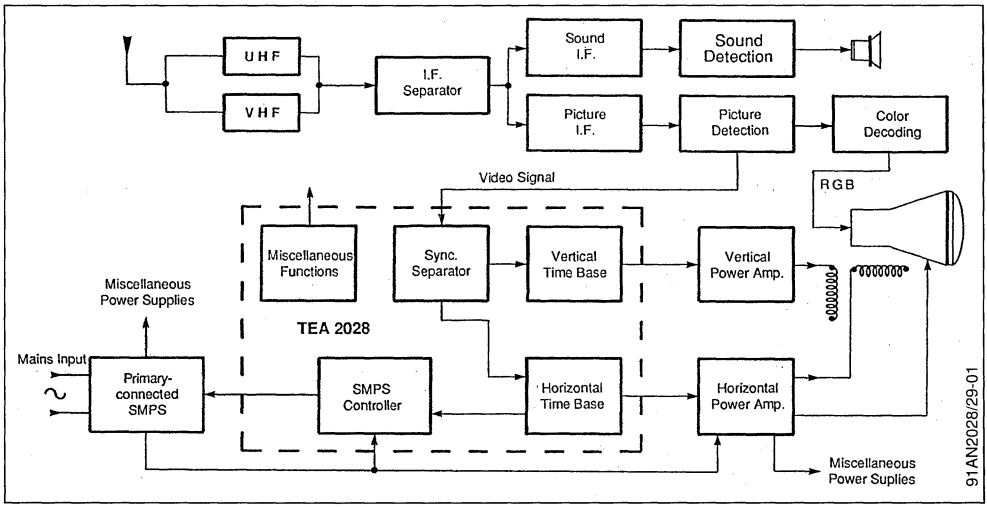
SUMMARY *(continued)*

I - GENERAL DESCRIPTION

As depicted in figure below, the TEA2028 combines 3 major functions of a TV set as follows :

- Horizontal (line) and vertical (frame) time base generation for spot deviation. The video signal is used for the synchronization of both time bases.
- On-chip switching power supply controller synchronized on line frequency.

Figure 1



This integrated circuit has been implemented in bipolar I^2L technology, and various functions are digitally processed. In fact, resorting to logic functions has the advantage of working with pure and accurate signals while full benefit is drawn from high integration of logic gates (approx. 110 gates per mm^2).

The main objective is to drive all functions using an accurate time base generated by a master 500 kHz oscillator.

Also, horizontal and vertical time bases, are obtained by binary division of reference frequency. This has the advantage of eliminating the 2 adjustments which were necessary in former devices.

One section of this integrated circuit is designed to drive a switching power supply of recent implementation called "master-slave". Switching takes place on the primary side (i.e., directly on mains) of a transformer. The device ensures **SMPS Control**, **Start-up** and **Protection** functions. Control signals go through a small pulse transformer thereby providing full isolation from mains supply.

This new approach fully eliminates the bulky mains transformers used in the past. In addition, it offers optimized power consumption and reduction of TV cost-price.

II - MAIN FUNCTIONS

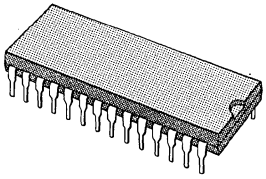
- Detection and extraction of line and frame synchronization pulses from the composite video signal.
- Horizontal scanning control and synchronization by two phase-locked loop devices.
- Video identification.
- 50 or 60Hz standard recognition for vertical scanning.
- Generation of a self-synchronized frame sawtooth for 50/60Hz standards.
- Line time constant switching for VCR operation through an input labeled "VCR" (Video Cassette Recorder).
- Control and regulation of a primary-connected switching power supply by on-chip controller device combining :
  - an error amplifier
  - a pulse width modulator synchronized on line frequency
  - a start-up and protection system

- Overall TV set protection input
- Frame blanking and super sandcastle output signals
- Frame blanking safety input for CRT protection in case of vertical stage failure.

III - PIN CONNECTION (TEA2028B)

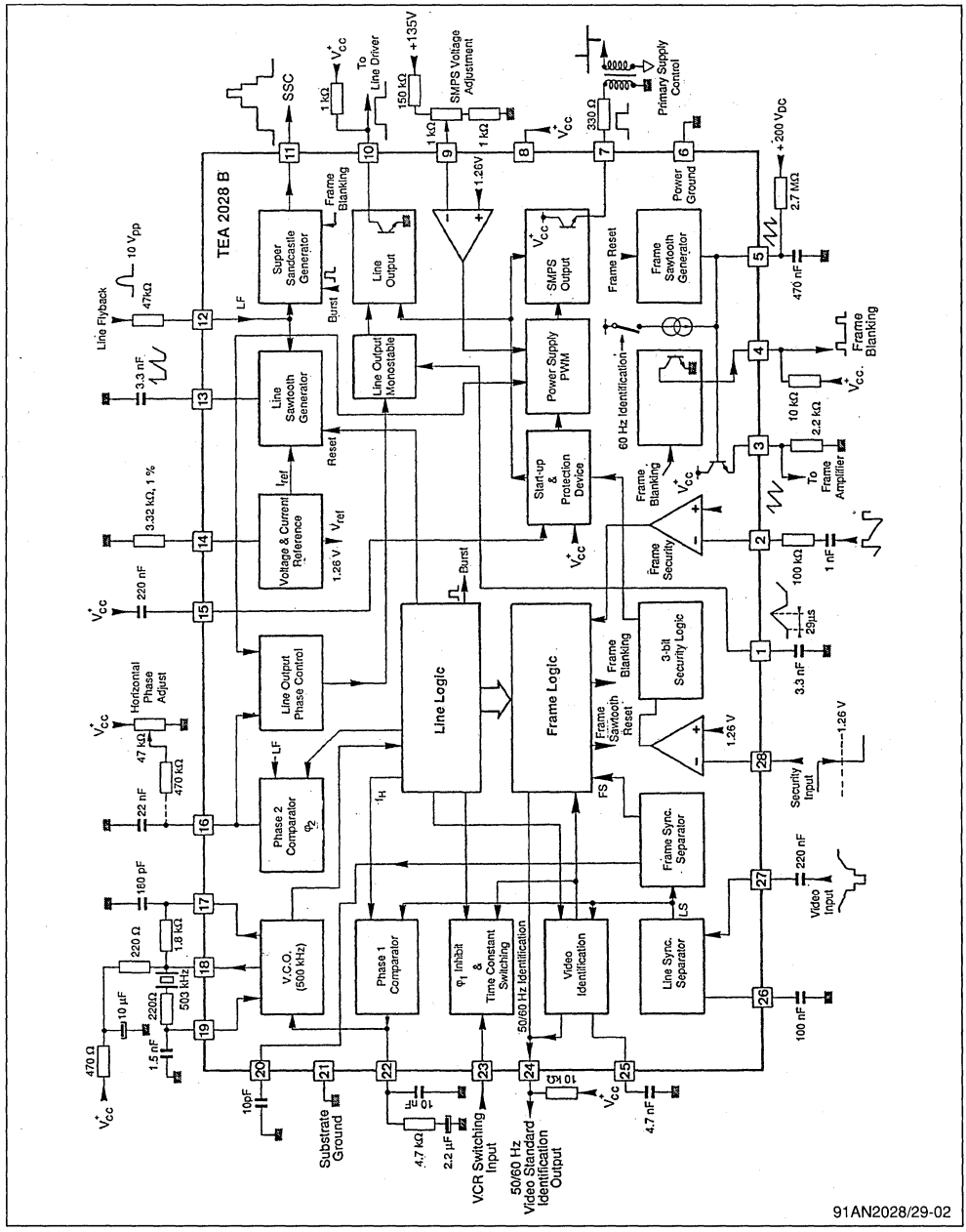
Pin Number	Description
1	Horizontal output monostable capacitor
2	Frame blanking safety input
3	Frame saw-tooth output
4	Frame blanking output
5	Frame ramp generator
6	Power ground
7	SMPS control output
8	Supply voltage (V_{CC})
9	SMPS regulation input
10	Horizontal output
11	Super-sandcastle output
12	Horizontal flyback input
13	Horizontal saw-tooth generator
14	Current reference
15	SMPS soft-start and safety time constant capacitor
16	$\phi 2$ phase comparator capacitor (and horizontal phase adjustment)
17	V_{CO} phase shift network
18	V_{CO} output
19	V_{CO} input
20	Frame sync time constant adjustment capacitor
21	Substrate Ground
22	$\phi 1$ phase comparator capacitor
23	VCR switching input
24	Video and 50/60Hz identification output (Mute)
25	Video identification capacitor
26	Horizontal sync detection capacitor (50% of peak to peak sync level)
27	Video input
28	Safety input

Package : DIP28



IV. INTERNAL BLOCK DIAGRAM

Figure 2



V. FUNCTIONAL DESCRIPTION

Majority of the on-chip analog functions were computer simulated and results such as temperature variation, technological characteristic dispersion and stability, have led to the enhancement and implementation of actually employed structures. A parallel in-depth study of the device implemented in form of integrated sub-sections is provided to analyze the overall performance in a TV set.

V.1 - Internal voltage and current references

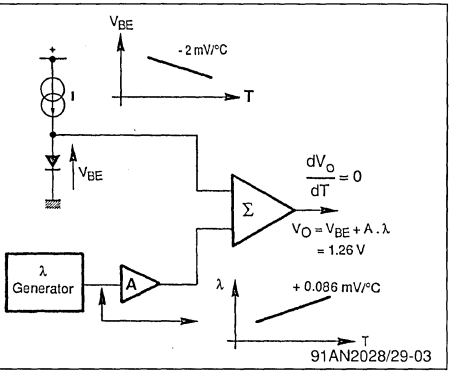
V.1.1 - 1.26V Voltage reference

For optimum operation of the device, an accurate and temperature-stable voltage generator independent from V_{CC} variations is used (Band-gap type generator).

The generated 1.26 V is particularly used as reference setting on input comparators.

V.1.1.1 - Generator block diagram

Figure 3



$$\text{with } \lambda = \frac{K \cdot T}{q} = 25.7\text{mV at } +25^{\circ}\text{C}$$

$$\frac{d\lambda}{dT} = \frac{K}{q} = +0.086\text{mV}/^{\circ}\text{C}$$

$$\frac{dV_{BE}}{dT} = \frac{V_{BE(25^{\circ})} - 1.26}{T} = -2\text{mV}/^{\circ}\text{C}$$

If $A\lambda = 1.26 - V_{BE}$

Then : $V_O = 1.26\text{V}$ (temperature-independent)

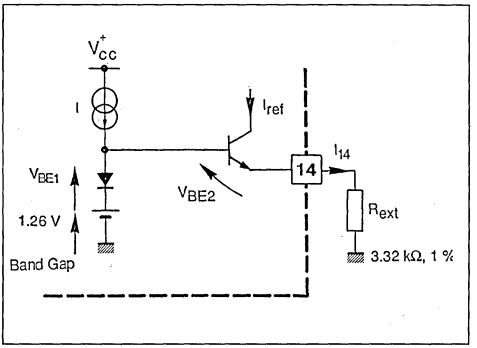
In practice, maximum drift due to temperature can be +0.23 mV/°C

i.e., ± 1.5 % for a ΔT of 80°C.

V.1.2 - Current reference

This is implemented using the 1.26V generator in combination with an external resistor.

Figure 4



$$I_{REF} \approx I_{14} = \frac{V_{14}}{R_{EXT}} = \frac{1.26 + V_{BE1} - V_{BE2}}{R_{EXT}}$$

Let's $I_{14} = I$ and $V_{BE1} = V_{BE2}$

$$\text{then : } I_{REF} = \frac{1.26}{R_{EXT}} = 380\mu\text{A}$$

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Thus, it follows that I_{REF} is accurate and independent of both V_{CC} and temperature.

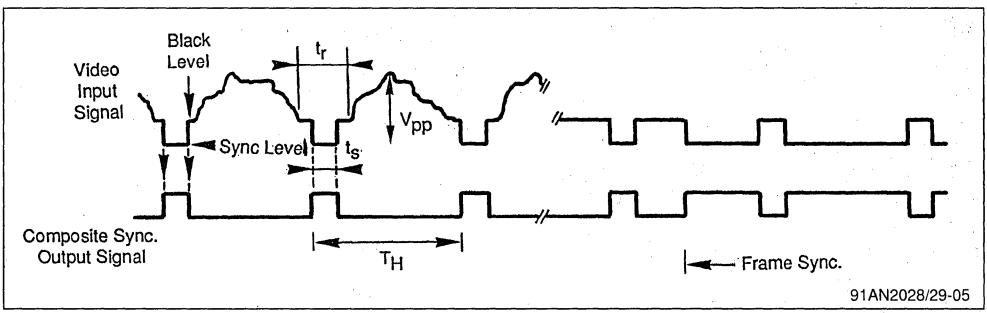
A set of current generators proportional to I_{REF} current are used in various circuit blocks.

V.2 - Line sync. extraction

Horizontal and vertical time bases should be synchronized with corresponding sync. pulses transmitted inside the infra-black portion of video signal. The duty of this stage is to extract these sync pulses. The output signal, called composite sync, contains the vertical sync which is transmitted by simple inversion of line sync. pulses.

The vertical sync pulse is then extracted from this composite signal.

Figure 5



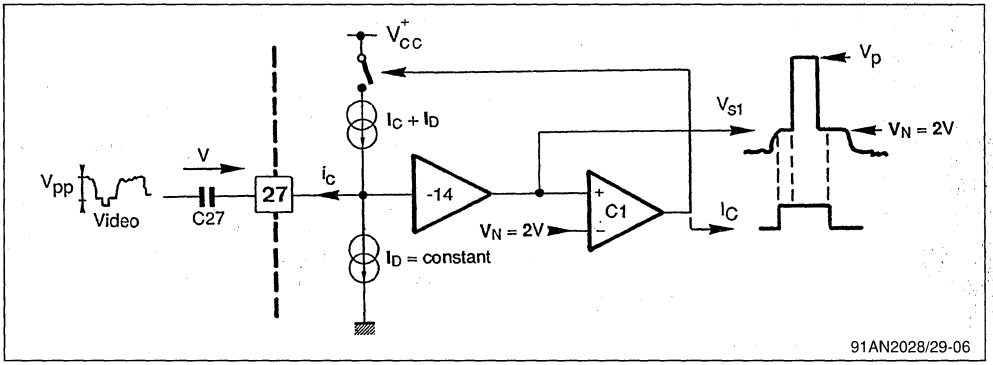
The main advantage of this arrangement is its ability to operate at video input signal levels falling within 0.2V to 3V peak-to-peak range and at any average value.

The operating principle is to lock the black level of the input signal (pin 27) onto internaly fixed voltage (V_N) and then memorize the average voltage of the sync pulse by using an integrating capacitor connected to pin 26.

Finally, the composite sync signal is delivered by a comparator the inputs of which are driven by $V_{50\%}$ and video signals.

V.2.1 - Black level locking

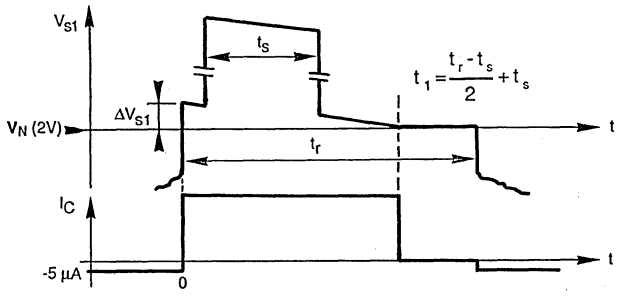
Figure 6



The video signal is applied to pin 27 through the coupling capacitor "C27". Since the sync pulse amplitude is generally equal to 1/3 of V_{PP} (i.e. 66mV to 1V) and in order to obtain a good precision of the black level, the sync pulse should be amplified by a coefficient of - 14 before being applied to the comparator "C1". This comparator will charge the "C27" capacitor as long as $V_{S1} > V_N$. V_{S1} will stabilize at V_N during the line flyback interval "T_r" if the average charge of "C27" capacitor is nil for one T_H period.

I_C/I_D is calculated such that the locking occurs at the middle of the back porch.

Figure 7



The ΔV_{S1} produced by I_D during the line trace which is :

$$14 \times \frac{I_D \cdot t_A}{C_{27}}$$

must be equal to ΔV_{S1} during the time interval "t1", i.e. :

$$14 \times \frac{I_C \cdot t_1}{C_{27}}$$

It follows that :

$$\frac{I_C}{I_D} = \frac{t_A}{t_1} = \frac{T_H - t_R}{t_s + \frac{t_R - t_s}{2}}$$

substituting $T_H = 64\ \mu s$, $t_r = 12\ \mu s$, $t_S = 4.7\ \mu s$ (which are standard and constant values) into above *equation* : $\frac{I_C}{I_D} = 6.23$

V.2.1.1 - Application

At $I_C = 5\mu A \Rightarrow I_D = 31\ \mu A$

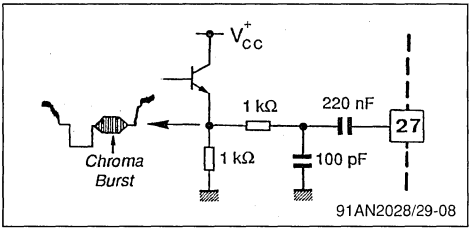
- With C27 = 220nF, ΔV_S will be

$$14 \times \frac{5 \times 52}{220} = 16\ mV$$

which yields 0.8 % maximum error in black level with respect to $V_N = 2V$ at the beginning of retrace time

- Due to transposition on amplifier stage, the black level voltage on pin 27 is equal to 2V.
- In practice, at low amplitude video signals, it is recommended to insert a low-pass filter before the "C27" capacitor so as to attenuate the chrominance sub-carrier and the noise components. The aim is to reduce the phase variations of the detected sync pulse and thus enhance the horizontal scanning stability.

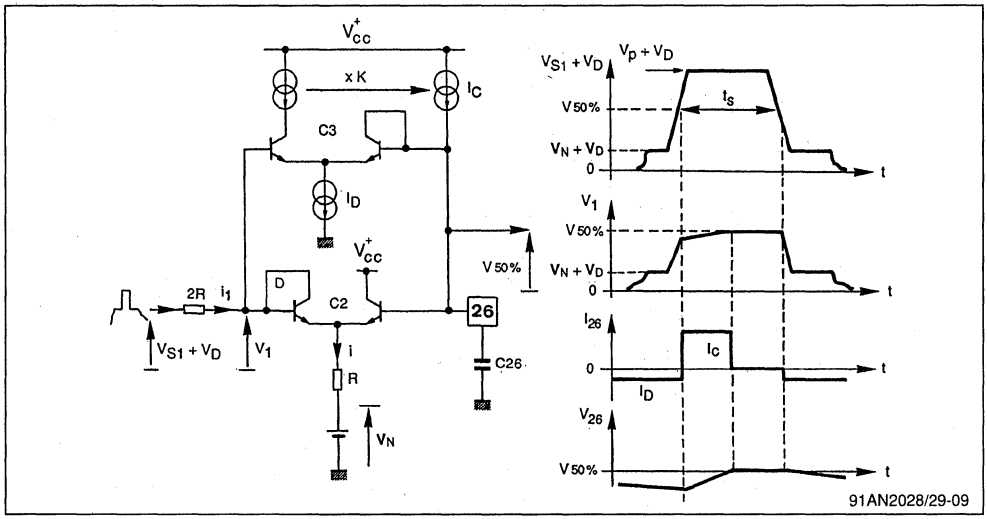
Figure 8



V.2.2 - Memorizing the sync pulse 50% value

The objective is to memorize the voltage corresponding to 50 % of the line sync pulse V_{S1} by using an external capacitor connected to pin 26.

Figure 9



The overall arrangement comprises two comparators.

- Comparator C2 : delivers an output voltage "V1" by comparing $V_{S1} + V_D$, V_{26} and the voltage drop across two resistors.
- Comparator C3 : which delivers a constant output current thereby maintaining on capacitor "C26", the voltage $V_{50\%}$ corresponding to 50% of peak to peak sync pulse.

During the line scanning, diode "D" is reverse biased : $V_{S1} + V_D = V_1 < V_{26}$ and C3 will deliver a current I_D which will discharge the capacitor.

During sync pulse interval, $V_{S1} + V_D = V_P + V_D$, diode "D" begins conducting and thus :
$V_1 = (V_P + V_D) - (2\ R\ i_1)$. Since the capacitor has been slightly discharged $\Rightarrow V_1 > V_{26}$, comparator C3 begins charging the capacitor until C2 is brought to equilibrium. At this time,

$$I_1 = \frac{i}{2} \text{ where } i = \frac{V_{26} - V_D - V_N}{R}$$

$$\text{thus } V_1 = V_P + V_D - 2R\frac{i}{2} = V_P + V_N + 2V_D - V_{26}$$

$$\text{and } V_1 = V_{26} \Leftrightarrow V_{26} = \frac{V_P + V_N}{2} + V_D = V_{50\%}$$

A high value C26 capacitor will thus memorize the voltage level corresponding to 50% of the line sync. pulse.

V.2.2.1 - $\frac{I_C}{I_D}$ Ratio calculation

During the line scanning period (T_H - T_S), the capacitor C26 will loose a charge equivalent to : $I_D (T_H - T_S)$.
This energy must be recovered before the end of sync pulse such that : $I_C \cdot t_S > I_D (T_H - T_S)$

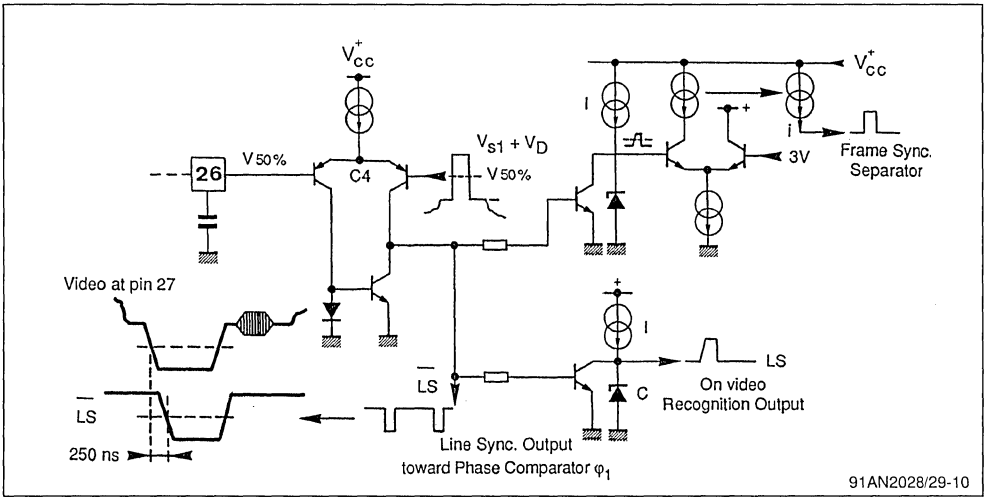
$$\text{therefore } \frac{I_C}{I_D} > \frac{T_H - t_S}{t_S} \quad \frac{I_C}{I_D} > 12.6$$

In practice, for C26 = 100nF, I_D = 25µA and I_C = 800µA

V.2.3 - Sync pulse detection

This function is fulfilled by comparing the inverted video signal ($V_{S1} + V_D$) whose black level is constant at 2V, with the sync 50% voltage level on pin 26.

Figure 10



Comparator C4 will deliver the line sync pulse (LS) which will be used for 3 functions :

- Horizontal scanning frequency locking : output to $\phi 1$ phase comparator.
- Frame sync extraction for vertical scanning synchronization.
- Detecting the presence of a video signal at circuit input.

The LS signal in two latter functions is filtered for noise by using combination of current generator I and a zener diode equivalent to a capacitor.

Using this extraction technique at a very noisy video signal yields remarkable display stability.

The device also provides for scanning synchronization at aerial signal attenuation of approximately 75dB, i.e. 15 to 20dB better than other sync processors.

V.3 - First phase locked-loop stage "$\phi 1$"

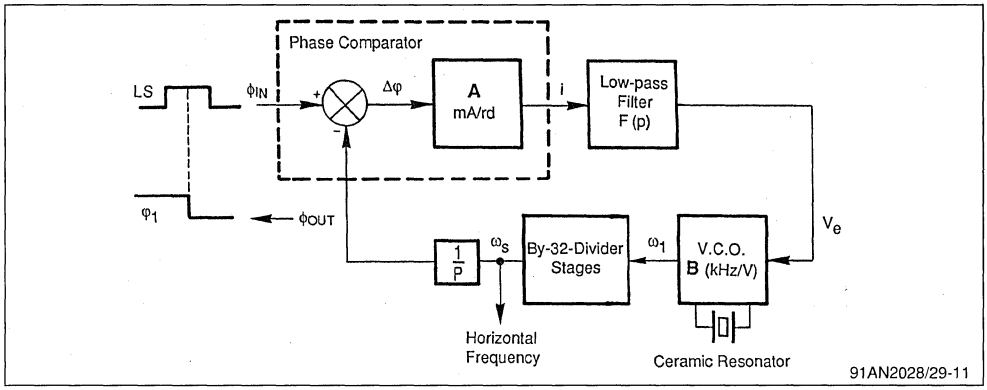
This stage is commonly called the first Phase Locked-Loop "$\phi 1$".

Its duty is to lock the frequency and the phase of the horizontal time base with respect to the line sync signal.

In the absence of transmission (i.e. lack of line sync), the horizontal scanning frequency is obtained by dividing the output frequency of a VCO device. This VCO oscillates at approximately 500kHz and uses a low frequency drift ceramic resonator. This method eliminates the need of horizontal frequency adjustment.

V.3.1 - Phase locked-loop "ϕ1" block diagram

Figure 11



V.3.2 - Functional duty of individual blocks

V.3.2.1 - Phase comparator

The duty of this comparator is to issue an output current proportional to the phase difference between ϕ_{IN} and ϕ_{OUT}.

V.3.2.2 - Low-pass filter

This filter suppresses the parasitic component containing the sum of phases, smoothens the phase difference component and determines the timing characteristics of the loop.

V.3.2.3 - VCO centered on 500kHz

This is a voltage-controlled oscillator which generates an output frequency proportional to the voltage applied to its input.

This voltage is delivered by low-pass filter.

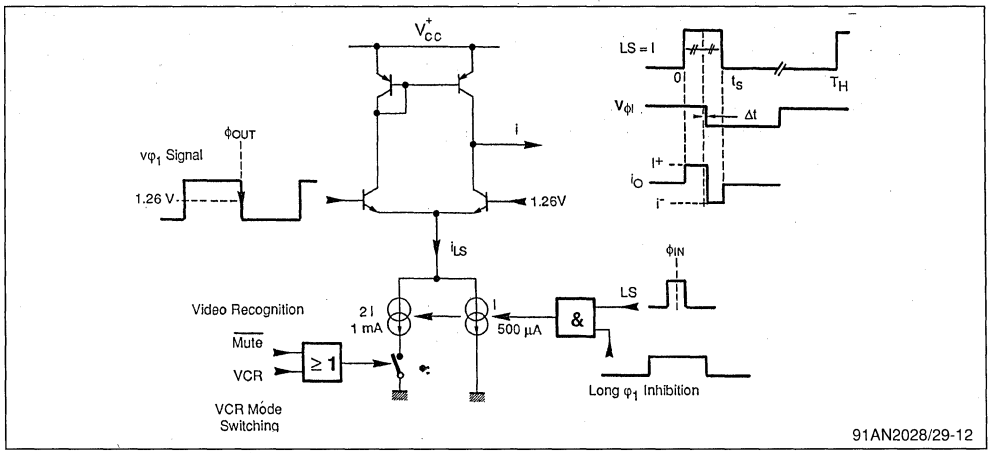
V.3.2.4 - Divider stage

It is used to divide the VCO frequency (500kHz) by 32 so that it can be compared with the line sync signal frequency of 15625Hz.

V.3.3 - Functional description of building blocks

V.3.3.1 - Phase comparator "ϕ1"

Figure 12

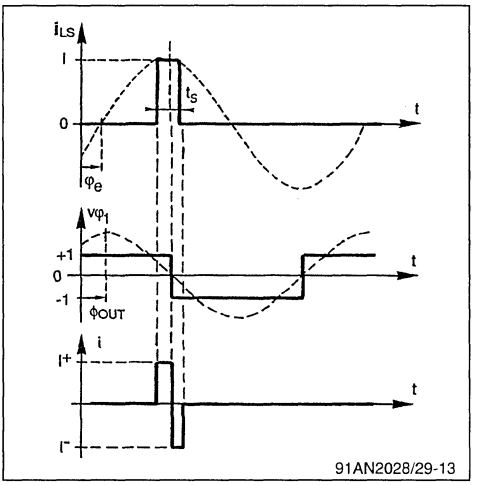


The comparator is functionally equivalent to a signal multiplier.

Let's assume that :
$i_{LS} = I \sin(\omega_H t + \phi_{IN})$
and $V_{\phi 1} = k \cos(\omega_H t + \phi_{OUT})$
then :

$$i = \frac{i_{LS} \cdot k}{2}\left[\sin\Phi_{IN} - \Phi_{out}) + \sin(2\omega_H t + \Phi_{IN} + \Phi_{out})\right]$$

Figure 13



- the low-pass filter will suppress the $2f_H$ frequency component
- ϕ_{IN} - ϕ_{OUT} difference being low :
  $\sin(\phi_{IN} - \phi_{OUT}) \approx \phi_{IN} - \phi_{OUT}$
- the output current will be therefore proportional to the phase difference between the signals compared.

In other words, the average current over one period is :

$$i_{AV} \times T_H = I\left(\frac{ts}{2} + \Delta t\right) - I\left(\frac{ts}{2} - \Delta t\right) = 2I\,\Delta t$$

$$i_{AV} = 2I\frac{\Delta t}{T_H} \text{ and } \Delta t = \Delta\Phi\frac{T_H}{2\pi}$$

The comparator conversion gain is thus :

$$A = \frac{i}{\Delta\Phi} = \frac{I}{\pi} \text{ (inA/rd)}$$

Later in our discussion we shall consider the two possible values of the current I.

For the time being, let's define these values as follows :

- I = 500µA for "long time constant" or normal operation
- I = 1.5mA for "short time constant" VCR mode or synchronization search (Mute).

The values of A are therefore :

- A_{LONG} = 0.16 mA/rd
- A_{SHORT} = 0.47 mA/rd

Use of comparator inhibition signal is quite useful under noisy transmission conditions. It eliminates risk of incorrect comparison during the line scanning phase which would be due to the noise present on LS signal. Horizontal phase and image stability are thus highly enhanced.

Characteristics of this inhibition signal will be discussed at the end of this chapter.

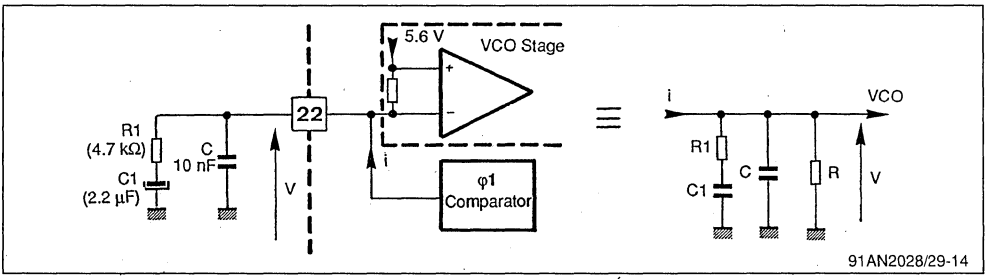
V.3.3.2 - Low-pass filter

- Its main function is to reject the $2f_H$ (31kHz) frequency component delivered by the phase comparator.
- It also defines the characteristics of the loop in transient mode.

The filter is built around two sub-sections which determine the stability and the response time of the loop in the following modes of transmission :

- Normal or VCR modes. See section V.3.6 "Dynamic study of φ1".

Figure 14



R is the dynamic input resistance of the VCO.
The filter transfer function may be defined as follows :

$$f(p) = \frac{V}{i} = Z(p)$$

$$Z(p) = R\frac{1 + R1C1p}{1 + p(RC + R1C1 + RC1) + RR1CC1p^2}$$

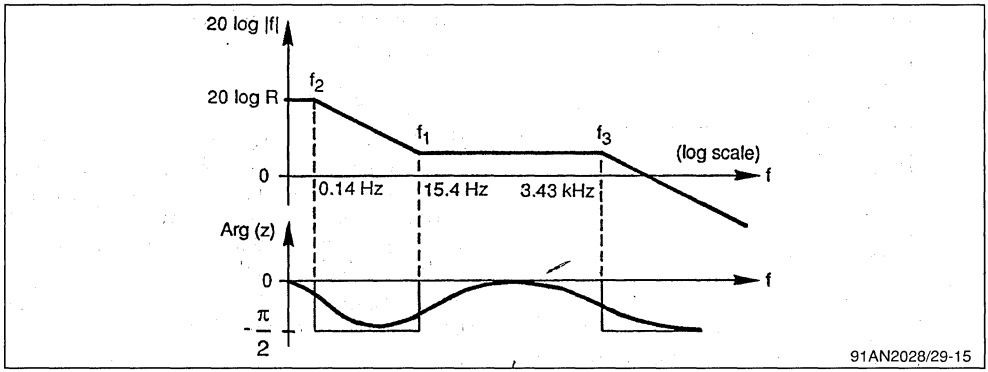
The second order terms of the denominator can be converted to first order products as a function of frequency as follow :

$$f(jf) = R\frac{1 + j\frac{f}{f1}}{(1 + j\frac{f}{f2})(1 + j\frac{f}{f3})}$$

with R1 = 4.7kΩ, R = 500kΩ, C1 = 2.2µF, C = 10nF we obtain :

- $f1 = \frac{1}{2\pi R1C1} = 15.4Hz$
- $f2 = \frac{1}{2\pi(RC1 + RC + R1C1)} = 0.14Hz$
- f3 = 3.43kHz

Figure 15



V.3.3.3 - VCO (Voltage Controlled Oscillator)

Its function is to generate a frequency proportional to a control voltage issued externally, by the low-pass filter in our case.

The period of the output signal is used as timing reference for various functions such as, horizontal and vertical time bases. The frequency range must be short and accurate :

- It must be short since the power dissipated within the horizontal scanning block is inversely proportional to the line frequency.
- The accuracy is required if the adjustment is to be omitted.

The basic arrangement is to employ a ceramic resonator (or ceramic filter) which has quite stable characteristics as a function of frequency.
A filter whose resonating frequency is a multiple of line frequency (15625Hz) is to be selected. An example is 32 x 15625 = 500kHz.

a. 503 kHz Ceramic Filter

Figure 16

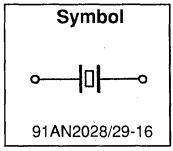
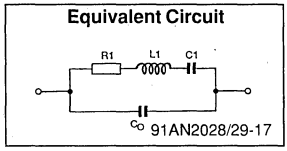


Figure 17



Where :

R1 = 7Ω, L1 = 1.26 mH, C1 = 78 pF, CO = 507 pF

- Series resonance frequency :

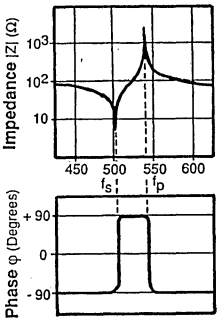
$$f_S = \frac{1}{2\pi\sqrt{L1C1}} = 503kHz$$

- Parallel resonance frequency :

$$f_P = f_S \cdot \sqrt{1 + \frac{C1}{C_0}} = 540kHz$$

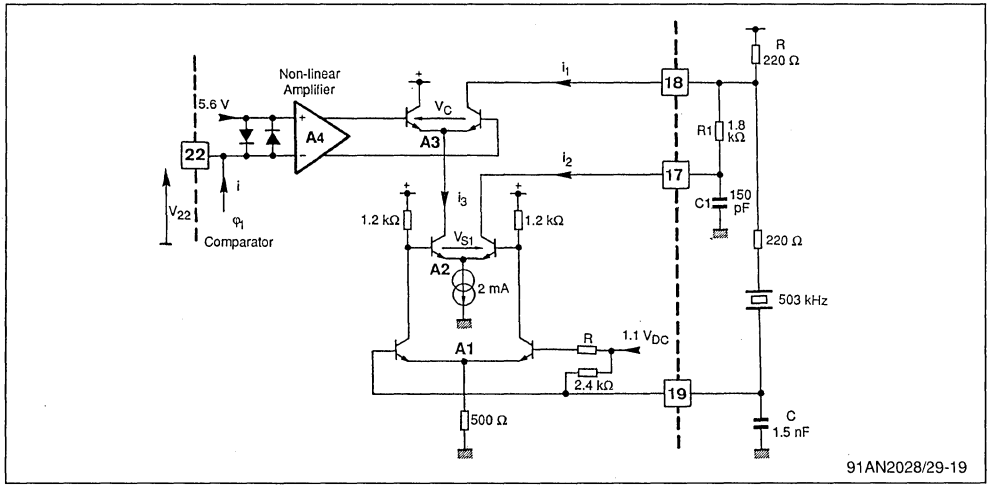
- Tolerance within the resonance area :
  503kHz ± 0.3 %
- Temperature stability :
  ±0.3 % of f_O at $\Delta T = 100\ ^{\circ}C$

Figure 18



b - Simplified Block Diagram of VCO

Figure 19



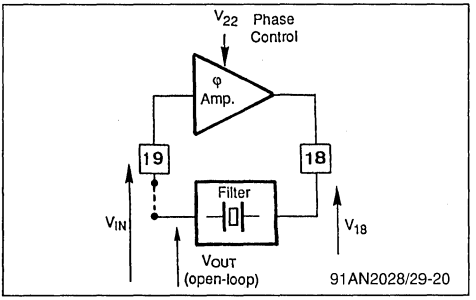
The overall arrangement is equivalent to a variable-phase amplifier configured in closed loop with the external passive filter.

The system will oscillate if the open-loop gain is 0dB and if VOUT leads VIN.

In closed-loop oscillating mode, the phase variation of V_{18}/V_{IN} imposed by V_{22} will result in same V_{OUT}/V_{18} variation but of opposite sign.

This phase change will finally correspond to a change in frequency.

Figure 20

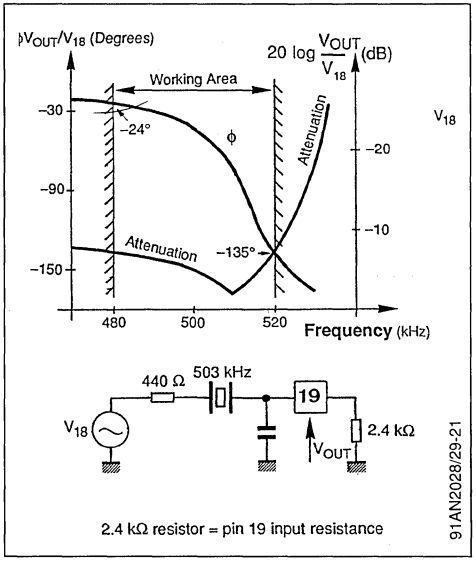


c. - Characteristics of the External Filter

The ceramic resonator behaves as a capacitor at $f < f_S$ (f_S : series resonance frequency) and as an inductor at frequencies falling between its two resonance frequencies.

Combined with a "R.C" network to generate a 90° phase lag, the overall arrangement will exhibit the following characteristics :

Figure 21



Thus, a variable (24° to + 135°) phase lead with a gain higher than 10 dB, must be implemented on-chip so as to enable the system to enter into oscillation.

The frequency dead points correspond to the maximum internal phase variations. This phase shift is controlled by voltage V_{22} whose value of 5.6V ± 0.7 is determined by two diodes.

From the above Figure, the non-linearity of phase-frequency characteristics is clearly apparent. If linear voltage-frequency response is required for a symmetrical gain of ϕ1 loop, it would then be necessary to implement a non-linearity, on the phase control amplifier A4, but in the opposite direction.

d. - Study of the Internal Amplifier

Let's study the gain and phase response of $\frac{V_{18}}{V_{IN}}$

as a function of V_{22}.

$V_{22} = \frac{V_C}{K}$ where K is a non-linear coefficient

To start with, the "V_C" voltage of comparator "A3" is taken as reference parameter.

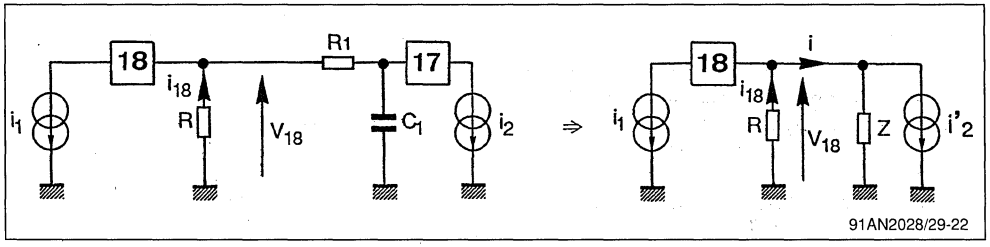
The dynamic representation of the output stage can be depicted as below (figure 22).

with : $I_2' = \frac{i_2}{1 + j\omega R_1 C_1}$ (at f = 500kHz)

$R_1C_1\omega = 1 \Rightarrow i_2' = \frac{i_2}{1+j}$

and $Z = R_1 + \frac{1}{j\omega C} << R \Leftrightarrow i \approx i_2'$

Figure 22



R1C1 network produces -45° phase lag of "i" with respect to "i2", around 500kHz.

$V_{18} \approx -R \cdot (i1 + I'_2)$

i1 AND i2 calculation as a function of "V_{in}" on pin 19

- A1 Amplifier : $\frac{V_{S1}}{V_{In}} = \frac{R_C}{dr_1} = \frac{1200}{57} = 21$

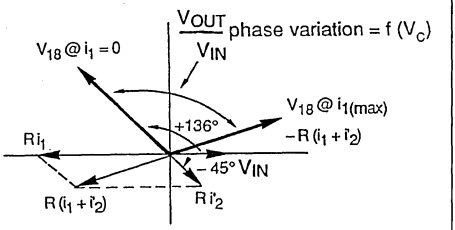
dr : dynamic resistance = $\frac{\lambda}{I}$

- A2 Amplifier : $\frac{i_2}{V_{S2}} = \frac{1}{2dr_2} = \frac{1}{54}$

$\Leftrightarrow \frac{i_2}{V_{IN}} = \frac{V_{S1}}{V_{IN}} \times \frac{i_2}{V_{S1}} = 0.395 \rightarrow i_2 = 0.39\ V_{IN}$

- i_2 is in phase with V_{IN} therefore :
  $i_3 = -i_2 = -0.39\ V_{IN}$

Figure 23 : Vector representation of V_{18}/V_{IN}



- A3 Amplifier :

$$i_1 = i_3 - \left(\frac{V_C}{4\lambda} + \frac{1}{2}\right) = -0.39\ V_{IN}\left(\frac{-V_C}{4\lambda} + \frac{1}{2}\right)$$

"V_{IN}" always leads the "i_1" by 180, only the amplitude of i1 is a function of V_C (See figure 23).

- $\frac{V_{OUT}}{V_{IN}} = -R\,\frac{i_1(1 + jR_1C_1\omega) + i_2}{1 + j(R_1 + R)C_1\omega}$
- $i1 = -0.39\ V_{IN}\left(\frac{i}{2} - \frac{V_C}{4\lambda}\right)$ and $i2 = 0.39\ V_{IN}$

The following figure 24 illustrates the characteristics of V_{18}/V_{IN} phase versus V_C.

- Phase variation determined by V_C falls between +24° and +135° range
- The gain is higher than 10 dB. The pin 18 output signal of 30 to 40 dB has a rectangular component (See figure 24).

e. - Characteristics of the non-linear Amplifier "A4"

This is a differential amplifier whose equivalent feed-back resistors of emitters vary as a function of its input voltage.

Figure 24

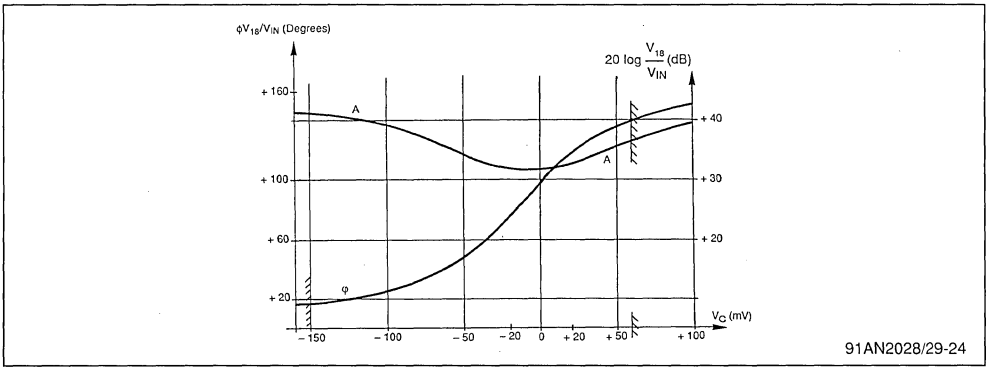


Figure 25 : $V_C = F(V_{22})$

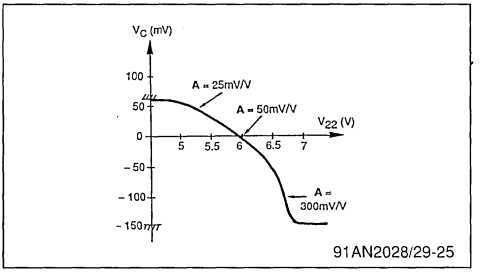
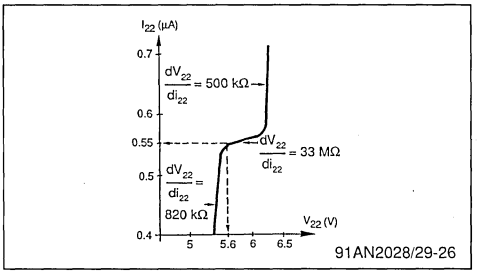


Figure 26 : $I_{22} = F(V_{22})$



The maximum output voltage swing is set by two "clamp" diodes connected to "V_{22}" input.

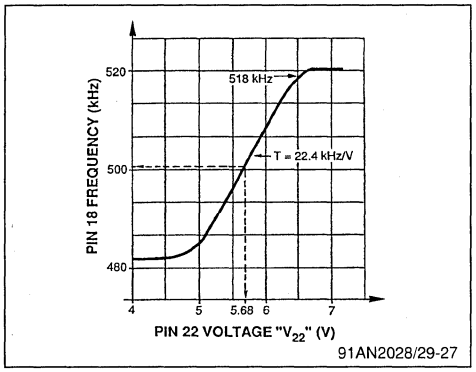
f. - Voltage-frequency transfer characteristics of VCO

The transfer characteristic is linear and centered at 5.6V at 500kHz operating frequency.

- T transfer = $\frac{\Delta f}{\Delta V} = 22.4$kHz/V and once it goes through five divide-by-two stages :

$T = \frac{22.4}{32} = 0.7$kHz/V

Figure 27



V. 3.4. - "ϕ1" time constant switching

When switching between stations or receiving signal via a VCR, the loop locking interval must be as short as possible so as to avoid unwanted visible effect on the picture. In fact, since the synchronization between the VCR motor drive and the playback head is rather imperfect, it will produce frequency and phase fluctuations in the output composite video signal. Under these conditions, phase locking interval must be "short" (VCR Mode).

In the case of broadcast transmission, this loop must also filter all phase variations produced by noisy sync signal. In this case, its locking time constant must be "long" (normal mode).

In other "jungle" circuits, this time constant switching is carried out by capacitor switching within the filter loop. In our case, this function is achieved by changing the current amplitude of the phase comparator.

This amplitude changing modifies the open-loop system gain and therefore the damping coefficient and the locking time constant.

The device will be in short time constant mode under the following two conditions :

- VCR Mode or SCART Connector Mode :
  This mode is enabled by a low state on pin 23.
  V23 < 2.1 V.
- Transmitter search and tunning.
  In order to accelerate the capture, a "Video Identification" stage will detect the presence or the absence of a video signal on input pin 27, and deliver accordingly a signal called "Mute".

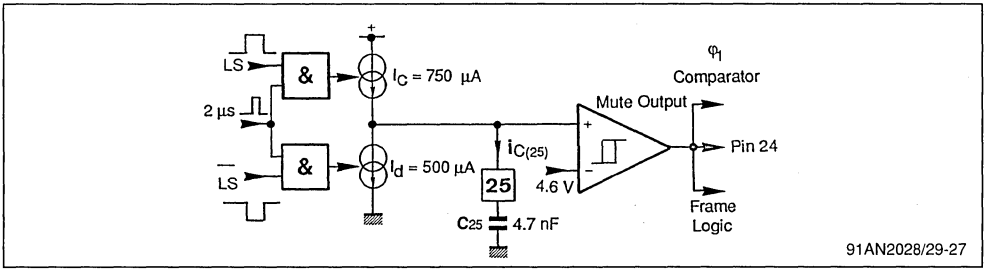
V.3.5 - Video identification stage

This stage will detect the coincidence between the line sync pulse (if present) and a 2µs pulse issued from the logic block. This 2µs pulse at line frequency is positionned at the center of line sync pulse when the first loop "φ1" is locked.

This sampled detection is stored by an external capacitor connected to pin 25. The video recognition status is also available on pin 24 so as to enable Sound Muting during station search process and the inhibition of Automatic Frequency Tuning.

V.3.5.1 - Block diagram

Figure 28



The video recognition signal is delivered by a hysteresis comparator.

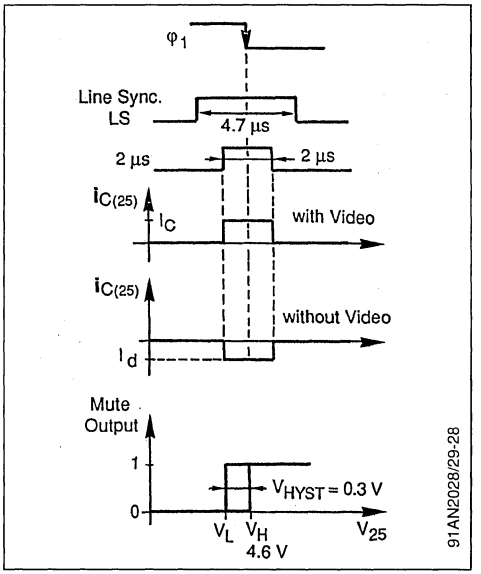
The recognition time "Tr" is adjustable by an external capacitor, as soon as φ1 is locked :

- $I_{C25(AV)} = I_C \times \frac{2\ \mu s}{64\ \mu s}$

and :

- $T_R = C_{25} \times \frac{V_H}{I_{C25(AV)}} = 1.96 \times 10^5 \times C_{25}$
- with C_{25} = 4.7 nF ⇒ Tr = 1 ms (which is clearly quite fast)

Figure 29



V.3.6 - Characteristics of loop ϕ1

V.3.6.1 - Locking accuracy

Let's study the phase error "φ_{OUT} - φ_{IN}" under steady state conditions :

The open-loop gain is :

- $T(p) = \frac{AB\ f(p)}{f}$

Where :

- A = 0.16 mA/rd (long time constant)
- A = 0.47 mA/rd (short time constant)
- B = 0.7 kHz/V or B = 4.4 10^3 rd/s

- $f(p) = R \times \frac{1 + \tau_1 p}{(1 + \tau_2 p)\ (1 + \tau_3 p)}$

Where :

- R = Dynamic input resistance of VCO.

If a phase step of $\Delta\varphi$ is applied to the input, the following would be obtained as a function of (p) :

$$\Phi_{IN}(p) = \frac{\Delta\Phi}{p}$$

Using the last value theorem : lim f(t) = lim p . f(p)

Let's calculate $\lim_{p \to 0} (\varphi_{IN} - \varphi_{OUT})$

- The closed-loop gain is :

- $H(p) = \frac{T(p)}{1 + T(p)} = \frac{ABf(p)}{p + ABf(p)} = \frac{\Phi_{OUT}(p)}{\Phi_{IN}(p)}$

that is : $\lim_{p \to 0} (\Phi_{IN} - \Phi_{OUT}) = \lim_{p \to 0} \frac{p\Delta\Phi}{p + AB\ f(0)} \to 0$

It is therefore deduced that the system can follow all input phase variations without producing any static error.

In practice, there will be a slight error due to the input bias current "I_B" of VCO, which is 0.55µA at f_O = 500kHz. This DC current is delivered by a phase comparator which will generate a phase error of :

- long time constant :

$$\Delta\Phi_{LONG} = \frac{I_B}{A_{LONG}} = 0.55 \times \frac{10^{-3}}{0.16} = 3.4 \times 10^{-3} rd$$

or 35ns in Δt

- short time constant :

$$\Delta\Phi_{SHORT} = \frac{I_B}{A_{SHORT}} \equiv 12ns$$

These two errors cause a horizontal picture displacement. On a large screen of 54cm wide, this will be : 64 - 12 = 52µs, which for both modes corresponds to a shift of :

$$\Delta_{LINE} = \frac{\Delta\Phi_{LONG} - \Delta\Phi_{SHORT}}{52} \times 520 = 0.24 \text{ mm}$$

It is obvious that such displacement can be fully neglected.

Response to a Frequency Step

The input phase is : $\Phi_{IN}(t) = \Delta\omega t$

which as a function of (p) is : $\Phi_{IN}(p) = \frac{\Delta\omega}{p^2}$

The accuracy is :

$$\lim_{p\to 0} (\Phi_{IN} - \Phi_{OUT}) = \lim_{p\to 0} \frac{\Delta\omega}{p + ABf(o)} = \frac{\Delta\omega}{ABR}$$

where R = 500kΩ at f(o)

In this case, the phase error depends on both, the magnitude of the frequency step and the static gain ABR.

In general, $\frac{\Delta f}{\Delta f}$ which is the open-loop static gain, is taken into consideration.

$$\frac{\Delta\omega}{\Delta\Phi} = ABR = \frac{2\pi\Delta f}{\Delta t \times 2\pi} = A \cdot 2\pi \cdot B' \cdot R$$

$$\Rightarrow \frac{\Delta f}{\Delta t} = AB'R \times \frac{2\pi}{T_H} \quad (B' \text{ in kHz/V})$$

- In normal mode : A_{LONG} = 0.16 mA/rd

$$\Rightarrow \frac{\Delta f}{\Delta t} = 5.5 kHz/\mu s \quad R = 500k\Omega$$

- In VCR mode : A_{SHORT} = 0.47 mA/rd

$$\Rightarrow \frac{\Delta f}{\Delta t} = 16.5 kHz/\mu s$$

Note : The capture range is specified within ± 500 Hz with respect to 15625 Hz.

Numerical Example

Let's suppose that in VCR mode there is a frequency variation of ± 100Hz, this will yield a phase variation of 0.1/16.5, i.e. ± 6ns which, on a 54 cm wide screen, will produce a horizontal shift of Δ_{LINE} = ± 0.06 mm !

It is obvious that an excellent image stability is thus obtained.

V.3.6.2 - Dynamic study

The loop response in transient mode is quite important. It determines the overall system stability and the phase recovery time, which are imposed by the external filter "f(p)".

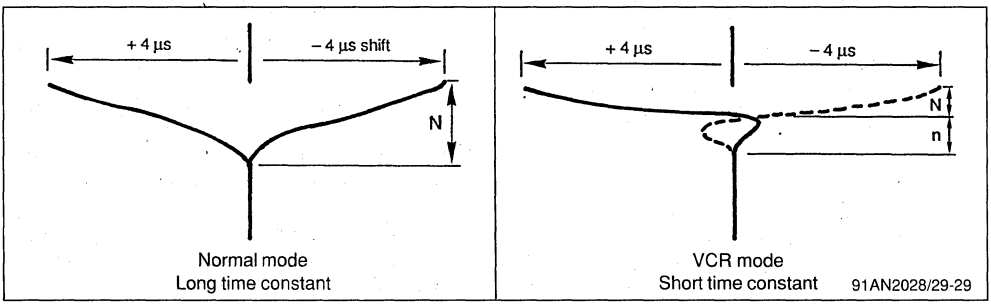
The close-loop transfer function is equivalent to a second order system. These time constants are in practice displayed on screen by a bar delivered by a special pattern generator representing the phase errors.

The following optimized results were obtained from filter f(p) connected to pin 22.

Filter component values are :

R1 = 4.7kΩ, C1 = 2.2µF, C = 10nF

Figure 30 : On Screen Display of Time Constants



Where :

N : number of lines required for phase correction

n : number of lines required for the horizontal oscillator to fully stabilize

a. Long time constant

- At Δt of 4µs ⇒ N=18 lines, i.e. τ_{LONG} = 1.15ms. System oscillations are perfectly damped. Image stability with a noisy video signal is very satisfactory.

b. Short time constant

- At Δt = 4µs ⇒ N = 5 lines, i.e. τ_{SHORT} = 0.32ms
- n = 5 lines

One should notice fast phase recovery, naturally followed by bounced oscillations due to the characteristics of a second order device.

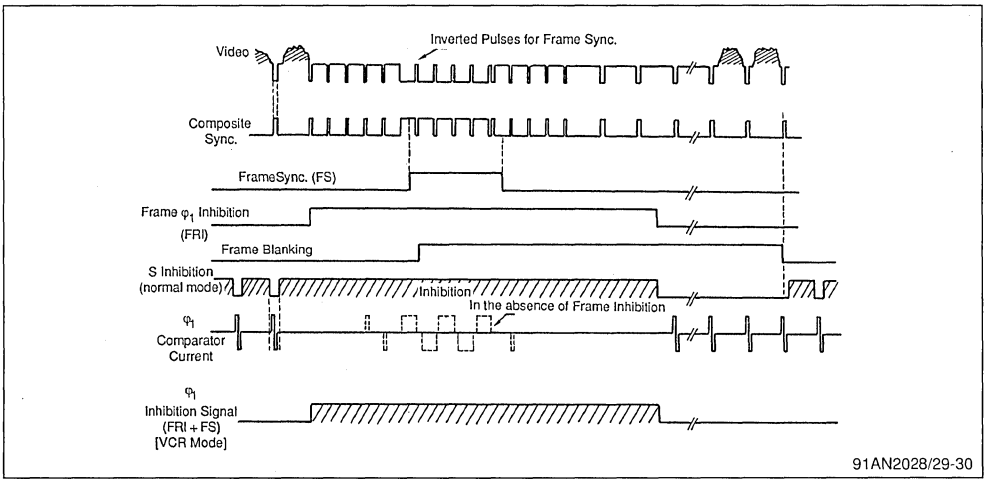
As given in application diagram section 6, an other alternative would be to use the following component values :R1 = 3.9kΩ, C1 = 4.7µF, C = 15nF

V.3.7 - Phase comparator inhibition

The phase comparator is disabled under two conditions :

- During frame sync pulse (see figure 30)

Figure 31



Inverting the line sync pulse contained within the video signal will provide the frame sync pulses required for the synchronization of vertical scanning.

Since the current supply to comparator ϕ1 is controlled by the line sync pulse, the comparator must be inhibited at the time of line sync inversions so as to avoid occurence of phase errors at the beginning of each frame.

This inhibition is activated during FRI (Frame Retrace Inhibition) issued by frame logic circuitry. If ϕ1 is locked before the vertical scanning synchronization occurs, (e.g. when switching between channels), and since FRI phase is not yet correctly positioned, the φ1 must be further inhibited by FS signal which is the extracted frame sync pulse.

- During line scanning (see figures 31 and 32)

This inhibition will eliminate the occurrence of all possible phase errors due to a noisy sync signal or parasitics during the line scanning phase. It yields excellent display stability at noisy video signals.

Figure 32

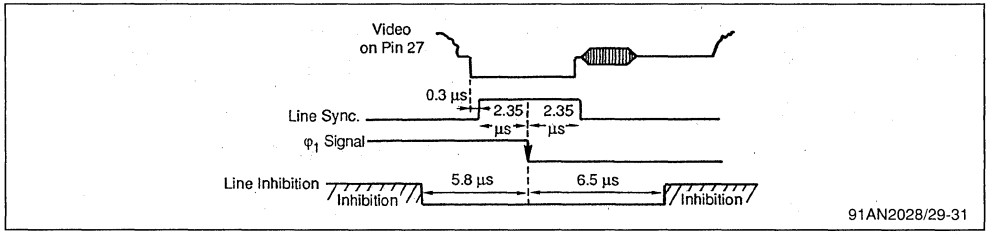
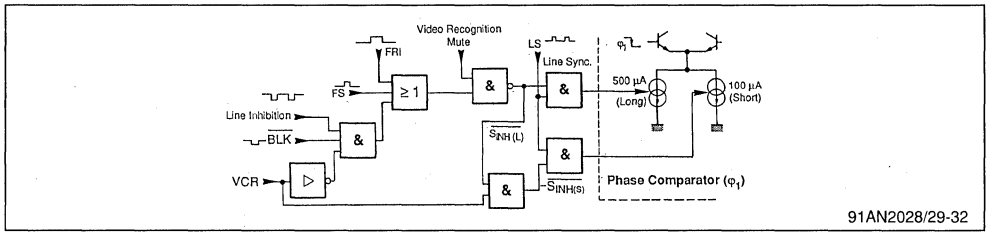


Figure 33 : ϕ_1 Inhibition logic block diagram



- ϕ1 Inhibition in long time constant mode (VCR = 0)
  - $S_{INH(LONG)}$ = Mute . (FRI + FS + $\overline{BLK}$. $LINE_{INH}$) and
  - $S_{INH(SHORT)}$ = 1
    Inhibition is activated during, frame sync, FRI and each time line trace interval - except at frame beginning between lines 8 and 21.
- ϕ1 Inhibition in short time constant mode (VCR = 1)
  - $S_{INH(SHORT)}$ = Mute . (FRI + FS) = $S_{INH(LONG)}$
    In VCR mode, inhibition is disabled during line trace since phase or frequency variations are not taken into account instantenously.

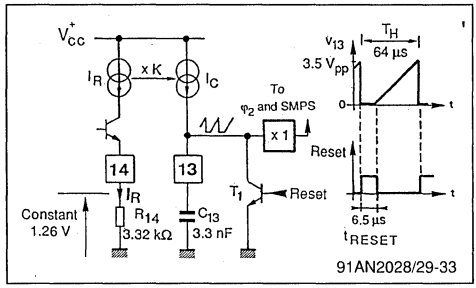
V.4 - Line saw-tooth generator

Before going through a detailed study of the second phase locked loop "ϕ2", let's have an overview of the line saw-tooth generator which has been mainly implemented for ϕ2 phase variations and also the phase modulation of the switching power supply.

It uses the combination of an external capacitor connected to pin 13 and an internally implemented constant current generator to generate a saw-tooth voltage at line frequency.

Its frequency is determined by the reset frequency of the capacitor "C_{13}". This reset signal is issued by

Figure 34



the line logic circuitry at a period multiple of VCO period (×32).

- $I_C = K \cdot I_R = K \cdot \frac{1.26}{R_{14}} = 200\mu A$
- $V_{13PP} = \frac{I_C(T_H - t_{reset})}{C_{13}}$
  $= \frac{K \times 1.26(T_H - t_{reset})}{R_{14} \cdot C_{13}} = 3.48V$
- $V_{CE(SAT)T1} \approx 20\ mV \Rightarrow V_{13(MAX)} = 3.5V$
- In sync mode :
  - T_H = 64µs, t_{RESET} = 6.5µs
  - K = 0.527 ± 2 %

V.5 - Second phase locked loop "$\phi 2$"

This stage controls the horizontal deflection of the electron beam i.e., the horizontal picture scanning. The frequency of operation, in the absence of video signal, is a multiple of the VCO frequency, i.e. 15625Hz - 500Hz.

When video signal is present, the scanning frequency is synchronized with the video signal through the first phase locked-loop "$\phi 1$".

The output rectangular waveform signal drives the line switching transistor. This transistor, when turned-off, generates what is commonly called the "line flyback".

In order to obtain a horizontally centered picture, the line flyback (LF) must coincide with the blanking time on tube cathodes.

The turn-off delay is due to transistor base storage time. This time varies in different TV sets as the transistors employed may have different operating characteristics which are functions of temperature variations, power rating and base drive.

Therefore, it follows that in order to obtain stable image centering, the line flyback must be phase-locked with respect to the video signal.

The second phase-locked loop also offers the possibility of horizontal phase-shift adjustment.

Figure 35

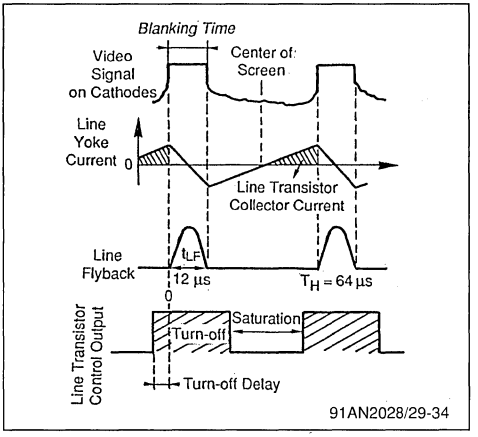
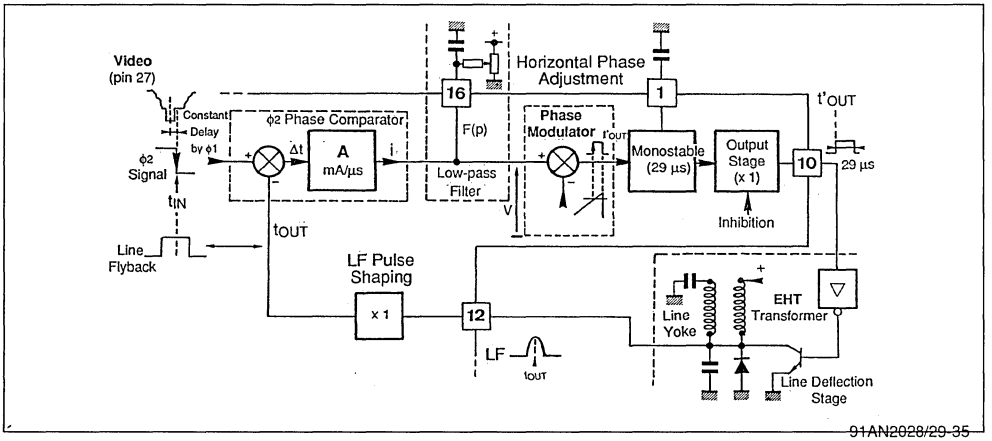


Figure 36 : Second Phase Locked Loop " ϕ_2" Block Diagram



V.5.1 - Duty of different building blocks

V.5.1.1 - "$\phi 2$" Phase comparator

This block generates a current proportional to the phase difference between the phase reference "$\phi 2$" and the middle of the line flyback to be phase-locked.

V.5.1.2 - Low-pass filter

- Rejects the parasitic component "sum of phases"
- Smoothens the "phase difference" component
- Allow "phase adjustment" by generating an error within the loop

V.5.1.3 - Phase modulator

Uses the line saw-tooth voltage to convert the voltage delivered by the low-pass filter into a phase corresponding to the line transistor turn-off control signal.

V.5.1.4 - Flip-flop

Generates the turn-off control signal for a constant time (fixed by the external capacitor), the phase of which is set by the modulator.

V.5.*1.5 - Output stage*

- Delivers the control signal for line transistor driver
- Disables the output during start-up and protection phases

V.5.1.6 - Line deflection stage

- Generates the saw-tooth current for line yoke
- Generates the high voltage required by picture tube and other supply voltages

The line flyback information is provided by the EHT transformer

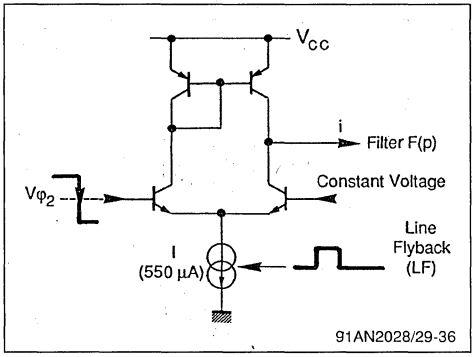
V.5.2 - Operation of building blocks

To provide an easier understanding of the subject, the "$\phi 2$" loop study will be covered as a function of various time intervals and not as a function of phase.

V.5.2.1 - Phase comparator "$\phi 2$"

The operation is identical to that of "$\phi 1$" loop.

Figure 37



The $V_{\phi 2}$ signal issued by logic block is phased with respect to the middle of line sync pulse on pin 27 and delayed by a 2.6 µs interval so as to be at the middle of blanking time on video cathodes.

The output current component "$2f_H$" is rejected by the low-pass filter.

- The average current is $i = 2I\frac{\Delta t}{T_H}$

  Where : $\Delta t = t_{IN} - t_{OUT}$

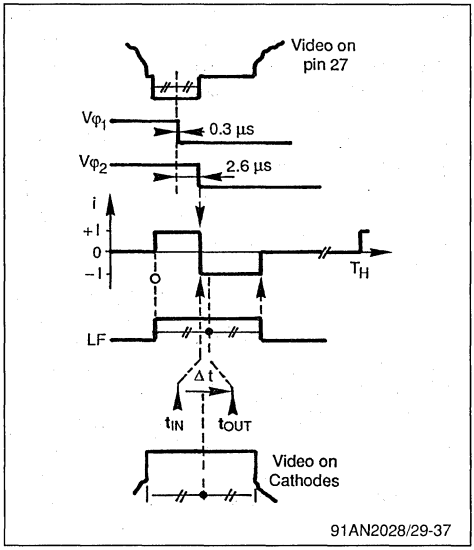
- The conversion gain is therefore :

$$A = \frac{i}{\Delta t} = \frac{2I}{T_H} = 17\mu A/\mu s$$

At : I = 550 µA and T_H = 64 µs

"A" will remain constant since "I" is a multiple of "I_{REF}" current on pin 14.

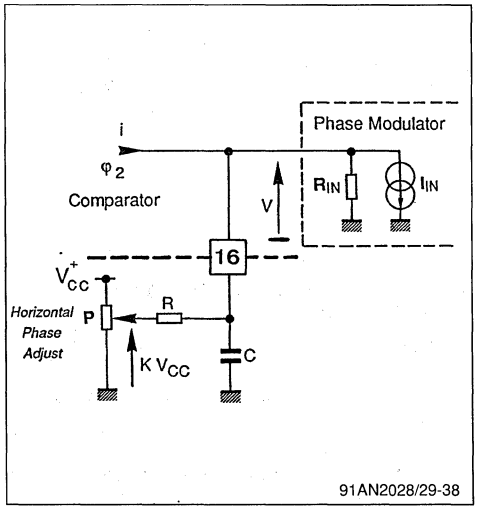
Figure 38



V.5.2.2 - Low-pass filter f(p)

The horizontal phase-shift adjustment is taken into account :

Figure 39



- Filter V = f(i) transfer characteristic is given as :

$$V = Zi + \frac{Z}{R} \cdot K \cdot V_{CC} - Z \cdot I_{IN}$$

Where :

- $Z = R_{IN} // R // \frac{1}{C \cdot p}$
- R_{IN}, I_{IN} : modulator input characteristics

In Dynamic Mode

$$- V = Zi \Rightarrow f(p) = \frac{V}{i} = Z(p) = \frac{R'}{1 + \tau p}$$

Where :

- $R' = R_{IN} // R$ (R >> Potentiometer P)
- $\tau = R' . C$: Filter time constant

The network behaves as a first order low-pass filter whose cut-off frequency at -3 dB is :

$$f_{-3dB} = \frac{1}{2\pi R'C}$$

Filter component values

- R = 470kΩ and C = 22nF
  - In practice, ($K \in [0,1]$) V_{CC} = 12 V
- R_{IN} = 25MΩ , I_{IN} = 0.65µA (base input current)

F_{-3db} = 15.7 Hz with adjustment and 0.3Hz without adjustment

V.5.2.3 - Phase modulator

This is built around a comparator which converts the filter voltage to a rectangular waveform such that its rising edge phase, variable as a function of filter voltage "V", will trigger the line transistor turn-off control circuitry.

The conversion gain is determined by the slope of the line saw-tooth applied to comparator.

Figure 40

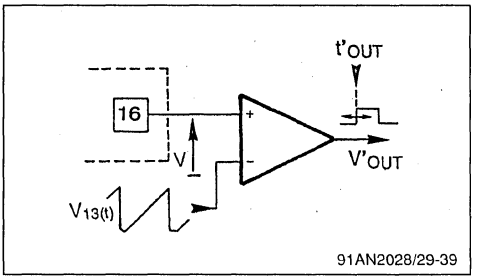
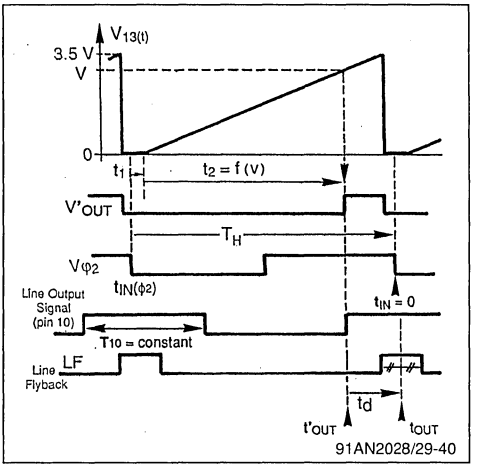


Figure 41



- Transfer characteristic is given by :

$$\frac{\Delta t'_{OUT}}{\Delta V} = \frac{\Delta t_{13}}{\Delta V_{13}} = B = 16.4\mu s/V$$

therefore $t_2 = B.V$

Let's consider the delay interval between "t_{OUT}" and the reference time "t_{IN}"

where t_{OUT} is the middle of line flyback :

- $t_{OUT} - t_{IN} = t_2 + t_d + t_1 - t_H$

Where :

- $t1 = 4.3\mu s$

(Reset for V_{13} and $V_{\phi 2}$ are signals coming from line logic block and are synchronized on line sync.)

- t_d = 2 to 15µs

(Delay between leading edge of output signal - pin 10 - and the middle of line flyback)

- $t_H = 64\mu s$
- $t_{OUT} - t_{IN} = B.V + t_d - 59.7\mu s$

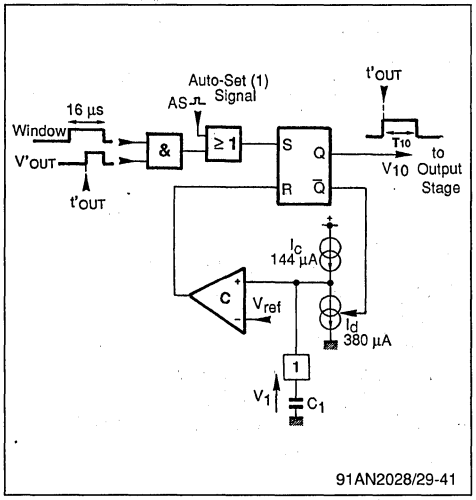
V.5.2.4 - Line flip-flop (TEA2028 only for TEA2029 refer to Section VII.6)

It generates a constant duration rectangular signal used to turn-off the line transistor. It is triggered by the rising-edge of the phase comparator output voltage and reset after capacitor on pin 1 is charged.

a. Block diagram

"V'$_{OUT}$" will set the flip-flop thereby allowing the capacitor "C1" to be charged by current "I_C" delivered through current generator. The voltage across capacitor begins rising until it reaches "V_{REF}". At this time, comparator "C" is triggered, the output of which will in turn reset the flip-flop. The capacitor "C" is consequently discharged by current I_D - I_C.

Figure 42



b. T10 Calculation

$$T_{10} = \frac{C1 \cdot \Delta V_1}{I_C} = \frac{C1 \cdot V_{REF}}{I_C}$$

"I_C" is a fraction of "I_{REF}" on pin 14

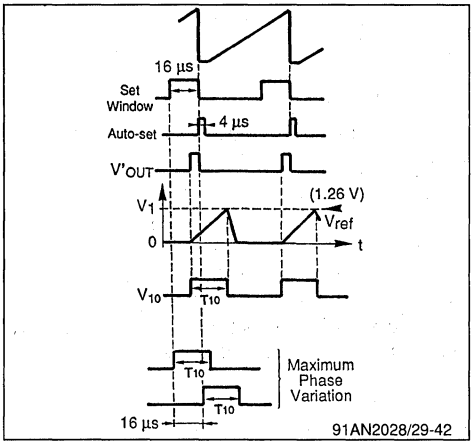
$$I_C = \frac{I_{REF}}{\alpha} = \frac{V_{REF}}{\alpha \cdot R14} = 144\mu A$$

$$\Rightarrow T10 = \alpha \cdot R14 \cdot C1 = 2.64 \times R14 \times C1$$

- R14 = 3.32kΩ $\Rightarrow$ T10 = 29µs
- C1 = 3.3nF

  - T10 is independent from temperature and V_{CC}
  - α has a maximum dispersion of ± 3% from device to device

Figure 43



c. 16µs Window

This window is generated by the line logic circuitry and sets the maximum phase variations of the output signal "V_{10}".

Also, for protection purposes, should "V_{16}" voltage equal "0", the output signal will be always present and have a maximum phase shift of 16µs with respect to the falling-edge of the line saw-tooth.

d. Auto-set to "1"

To provide protection, this function will trigger the flip-flop if the modulator is disabled, i.e. $V_{16} > V_{13(MAX)}$.

e. Maximum "T_{10}" value as a function of "C1"

$T_{10(MIN)}$: 16µs(window) + 4µs(auto set) = 20µs

$$\Rightarrow C_{1(MIN)} = 2.3\ nF$$

$$T_{10(MAX)} : \text{for } \frac{C_1 \cdot V_{REF}}{I_d - I_C} + \frac{C_1 \cdot V_{REF}}{I_C} \leq 64\mu s$$

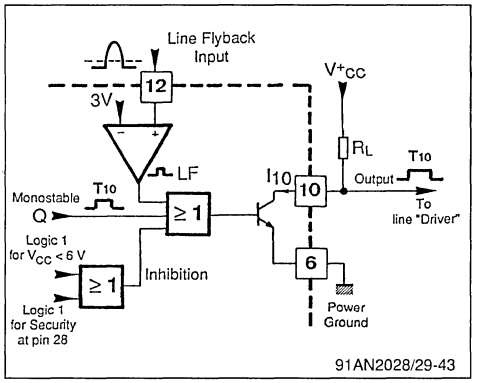
$$\Rightarrow T_{10(MAX)} = 40\mu s \Rightarrow C_{1(MAX)} = 4.6\ nF$$

For normal operation, C1 value has to be chosen between 2.3nF and 4.6nF.

If pin 1 is grounded, output signal (pin 10) is inhibited and goes high.

V.5.2.5 - *Line output stage & inhibitions*

Figure 44



- Open-collector output : $V_{10(SAT)}$ < 1.5V at $I_{10(MAX)}$ = 20mA

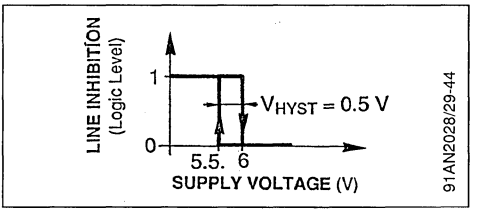
The line output (pin 10) will go high if either the following three inhibitions is activated :

a. Inhibition at start-up

This is generated by a hysteresis comparator which is driven by "KVCC" and the "1.26V" reference voltage.

This inhibition is mandatory since the device will operate only at $V_{CC} \geq 5$ V.

Figure 45



b. Inhibition during line flyback

The output signal pin 10 is high during line transistor turn-off. The leading edge of output signal pin 10 turns off the line transistor after a delay interval (storage time).

The line transistor turn-off generates an overvoltage on the collector corresponding to the line flyback pulse. During this interval, in order to avoid transistor destruction, the pin 10 output must absolutely remain high.

This is done internally with the line flyback pulse (pin 12), which forces pin 10 output to high level during the line flyback time.

c. Safety inhibition

The device has a security input terminal "pin 28". If a signal lower than V_{REF} (1.26V) is applied to this pin, line and power supply outputs are all inhibited.

This function is particularly useful for TV chassis protection. Refer to section V.7.5 for further details.

V.5.2.6 - Line deflection stage

This chapter will cover a general description of the "horizontal deflection stage" employed almost commonly in all recent TV sets.

Deflection of electron beam is proportional to the intensity of magnetic field induced by the line yoke. This yoke is equivalent to an inductor. The deflection is therefore proportional to the current through inductor.

In order to obtain a linear deflection from left to right as a function of time, a saw-tooth current must be generated within the yoke. The approach is to apply a switched DC voltage to the line yoke.

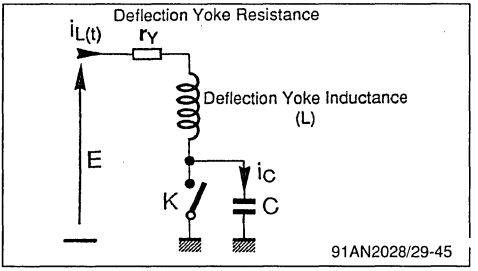
- When K is closed :

$$i_{L(t)} = \frac{E}{r_y}\left(1 - e^{-\frac{r_y t}{L}}\right)$$

- $\frac{L}{r_y}$ is always higher than half of trace time :

$$\frac{t_{trace}}{2} = \frac{T_H - t_{LF}}{2} = \frac{64 - 12}{2} = 26\mu s$$

Figure 46



- "i_L" variations as a function of time :

$$\frac{di_L}{dt} = \frac{E}{L} e^{-\frac{rt}{L}} \approx \frac{E}{L} \left(\text{for } t << \frac{L}{r_y} \right)$$

The current will therefore be linear as a function of time $i_L(t) = \frac{E}{L} \cdot t$ from "t_1" to "t_2" which is the second portion of the line trace interval.

- Current at the end of trace : $I_M = \frac{E}{L} \cdot \frac{t_{TRACE}}{2}$

- Energy stored within inductor : $W = \frac{1}{2} \cdot L \cdot I_M^2$

If the switch is opened at $t = t_2$, the "L.C" combination will enter into oscillation, the energy stored within inductor is transfered to the capacitor, which will return it to the inductor and so on.

The circuit period is classically given by :
$T = 2\pi \cdot \sqrt{LC}$

If "K" is closed at time "t_3", the inductor will once again have a voltage "E" across its terminals. The current falls linearly until "t_4". This phase corresponds to the first half of line trace interval.

The overvoltage across C is :

$$V_P = E \frac{t_{trace}}{2\sqrt{LC}} + E$$

during $t_{LF} \approx \pi\sqrt{LC}$

That is : $V_P = E \frac{t_{TRACE} \cdot \pi}{2t_{LF}} + E$

In practice, E is higher than 100V.

- $t_{TRACE} = 52\mu s$
- $t_{LF} = 12\mu s$

$\Rightarrow V_P \geq 780V$

Note that this overvoltage is almost 8 times higher than the source voltage "E". This overvoltage is applied to the primary winding of a "step-up transformer" (EHT Transformer) in order to generate the high voltage required by picture tube anode.

In practice, the power switch "K" is built by a combination of "High Voltage Switching Transistor" and "Fast Recovery Diode".

Figure 47

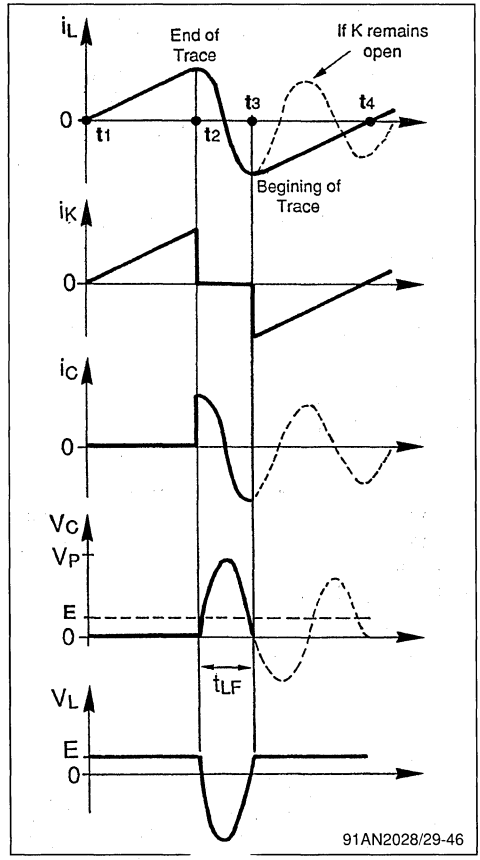
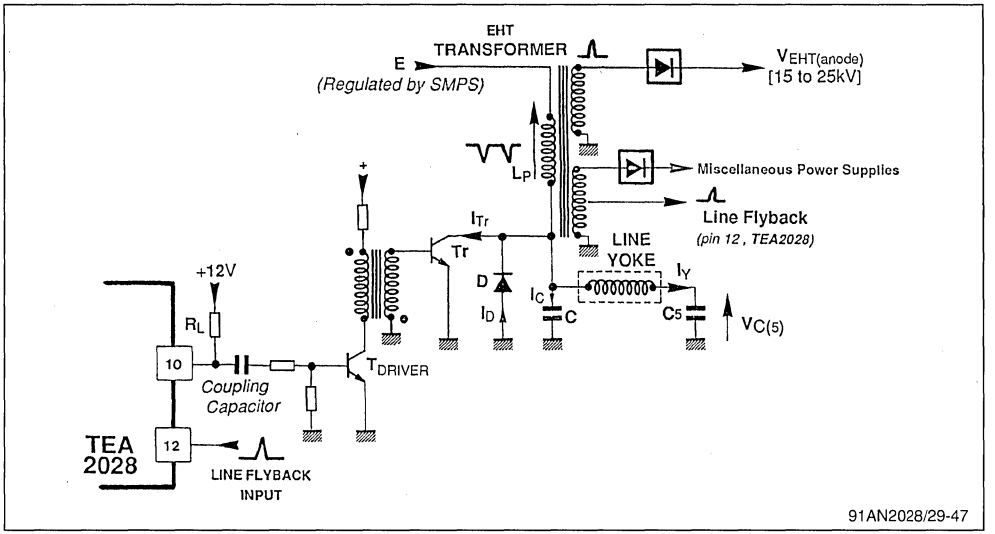


Figure 48 : Simplified diagram of the horizontal deflection stage



If considered in average value, it is seen that the voltage across capacitor "CS" is almost equal to the source voltage "E". The saw-tooth current through this capacitor will produce a parabolic ripple around "E", which will thus modify the equivalent source of the line yoke and induce a modified current of "S" shape within the yoke. This "S" current is used to produce a linear picture as a function of the picture tube geometry.

The basic arrangement can be reconstructed by assuming that the equivalent inductor "L" is the transformer "L_P" and line yoke inductors put in parallel (since $VC_{S(AV)} = E$).

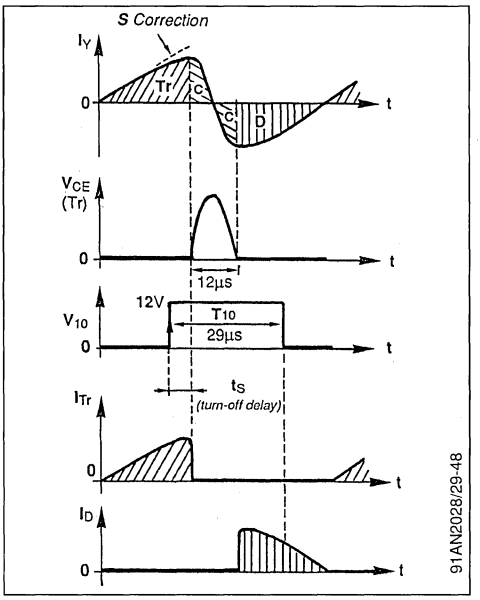
The output pin 10 of TEA2028 is applied to a matching stage called "line driver" the output of which drives the power transistor "T_r". The matching stage is necessary for optimized base drive.

At middle of trace, the transistor enters into saturation and its current rises linearly. V10 will then issue a control signal to turn the transistor off. The transistor will be in fact turned-off after a delay interval "t_S" (storage time) varying from 2 to 8 µs depending on application. The system will then enter into oscillation during its half-period thereby generating the line flyback. At the end of flyback time, the line yoke current is negative while the voltage across capacitor "C" has fallen to zero. The energy transfer automatically takes place by the recovery diode during the first portion of trace time.

Also, it is clear that the line scanning phase with respect to video signal is determined by the rising-edge of pin 10 output signal.

High level duration (T10) of pin 10 output signal

Figure 49



must be higher than the delay interval "$t_{S(MAX)}$" + the flyback time (i.e. 8 + 12 = 20µs) and must turn-off before the end of diode conduction :

$$T10 < t_{S(MIN)} + t_{LF} + \frac{t_{TRACE}}{2} \Rightarrow < 40\mu s$$

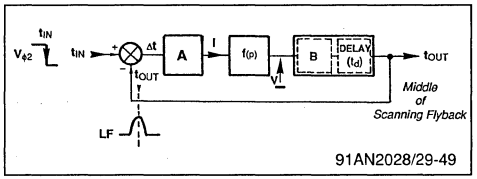
In practice, one will select the pin 1 capacitor C1 = 3.3nF to yield T10 = 29µs.

V.5.3 - Characteristics of loop "ϕ_2"

The function to calculate is a time with respect to the origin time set by "$V_{\phi 2}$". In fact, it is an easy task to inter-relate the horizontal displacement (in mm) to a time interval specified in µs.

For a large screen width of 540 mm, the horizontal scanning time :64 - 12 = 52µs, which corresponds to : ≈ 10mm/µs.

Figure 50



- $i = A \cdot (t_{IN} - t_{OUT})$ (1)
- $V = Z \cdot i + \frac{Z}{R} \cdot K \cdot V_{CC} - Z \cdot I_{IN}$ (2)
- $t_{OUT} - t_{IN} = B \cdot V + t_d - 59.7\mu s$ (3)
- $Z = \frac{R'}{1 + \tau p}$
- $R' = R_{IN} // R$
- $A = 17\mu A/\mu s$
- $\tau = R'C$
- $B = 16.4\mu s/V$

The open-loop dynamic gain is :

- $T = ABf(p) = ABZ = \frac{ABR'}{1 + \tau p}$ (4)

The system exhibits the characteristics inherent to a first order circuit and is therefore stable.

combining equations (1), (2), (3) and (4), the t_{OUT} delay is found as follows :

$$t_{OUT} = t_{IN} - \frac{BZI_{IN}}{1+T} + \frac{t_D - 59.7\mu s}{1+T} + \frac{B\frac{Z}{R} \cdot KV_{CC}}{1+T}$$

- Dynamic gain = 1
- Error term due to the input current "I_{IN}"
- Error term due to delay
- Error term due to phase shift adjustment (if applicable)

It is therefore clear that the second phase-locked loop does not cause any dynamic delay.

This can be explained by the fact that the phase modulator responds instanenously to all variations of "ϕ_2".

V.5.3.1 - Study of the Static Error

t_{IN} = 0 (phase of $V_{\phi 2}$) is taken as timing reference.

The equivalent impedance of F(p) filter is :

- R' = 460kΩ (R // R_{IN}) : if an adjustment is applied to pin 16, or
- Modulator input resistance RIN = 25MΩ : without adjustment

a. Phase shift error in case of no adjustment

Equation (5) becomes :

$$T_{OUT} = \frac{BR_{IN}I_{IN}}{1+T_1} + \frac{t_D - 59.7\mu s}{1+T_1}$$

with : T1 = ABR_{IN}

Where :

- R_{IN} = 25MΩ
- I_{IN} = 0.65mA
- t_d = 10µs
- T1 = 6.8 x 10^3 = 76dB

} t_{OUT} = - 46ns which corresponds to a picture shift of 0.46 mm !

The error is quite negligible and thanks to rather high open-loop gain, the display accuracy with respect to the phase set by "ϕ_2", is very satisfactory.

b. Study of shift adjustment

With R, P network connected to pin 16, the t_{out} becomes :

$$t_{OUT} = \frac{-BR'I_{IN}}{1+T_2} + \frac{t_D - 59.7\mu s}{1+T_2} + \frac{B\frac{R'}{R} \cdot KV_{CC}}{1+T_2}$$

With : T2 = ABR' (where R' = R // R_{IN})

and K ∈ [0;1]

Substituting the following values into above equation :

- R = 470kΩ
- R' = 470kΩ // 25MΩ = 461kΩ
- A = 17×10^{-6} A/µs
- B = 16µs/V
- td = 10µs
- T_2 = 125
- V_{CC} = 12V

t_{OUT} = - 38ns - 390ns + 1.5µs×K

therefore t_{out} = 1.5×K - 0.43 (in µs)

If K varies between 0 and 1

⇒ t_{out} [- 0.43ms to 1.07µs]

which corresponds to a picture displacement of : Δ_{LINE} [- 4mm to + 11mm].

Shift variations as a function of V_{CC} (with adjustment)

$$\frac{dt_{out}}{dV_{CC}} = \frac{B\frac{R'}{R} \cdot K}{1 + T_2} \approx \frac{B\frac{R'}{R} \cdot K}{T_2} \approx \frac{K}{AR}$$

$$= K \times 0.12\mu s/V \begin{cases} \frac{dL}{dV_{CC}} = 0.34mm/V \\ \text{at } K_{NOMINAL} = 0.28 \end{cases}$$

Therefore, a constant V_{CC} must be applied to the potentiometer.

V.6 - Vertical deflection driver stage

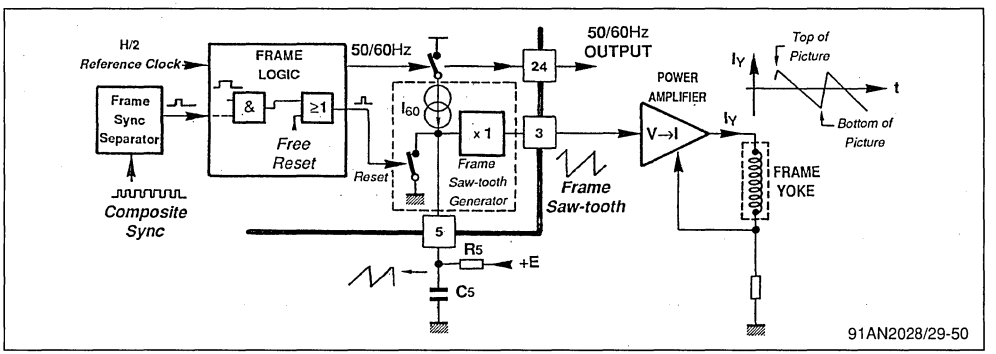
This stage must constantly drive the vertical spot deflection. Such deflection will horizontally scan the screen from top to bottom thus generating the displayed image. Similar to horizontal deflection, the vertical deflection is obtained by magnetic field variations of a coil mounted on the picture tube.

A saw-tooth current at frame frequency will go through this coil commonly called "frame yoke". Frame period is the time required for the entire screen to be scanned vertically.

C.C.I.R. and N.T.S.C. TV standards require respectively 50Hz and 60Hz Frame Scanning Frequencies. Also, a full screen display is obtained by two successive vertical scannings such that the second scanning is delayed by a half line period with respect to the first.

This method increases the number of images per second (50 half images/s or 50 frames/s in 50 Hz standard). This scanning mode called "Interlaced Scanning" eliminates the fliker which would have been otherwise produced by scanning 25 entire images per second.

Figure 51 : Block Diagram of the Vertical Deflection Stage



The circuit will generate a saw-tooth voltage which is linear as a function of time and called "frame saw-tooth". A power amplifier will deliver to the "frame yoke" a current proportional to this saw-tooth voltage. It is thus clear that this saw-tooth voltage reflects the function of the vertical spot deflection; which must itself be synchronized with the video signal. Synchronization signals are obtained from an extraction stage which will extract the useful signal during line pulse inversion of the composite sync signal.

Synchronization occurs at the end of scanning, in other words, when the saw-tooth voltage at pin 5 is reset. This function is accomplished by the "frame logic circuitry" of full digital implementation.

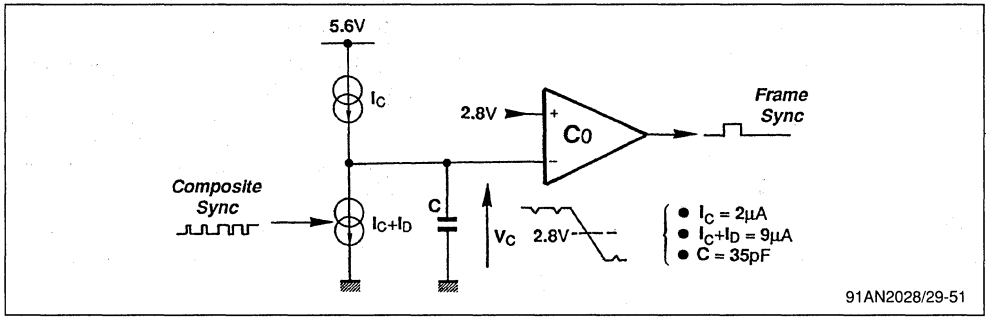
This processing method offers various advantages :

- **Accurate free-running scanning frequency** eliminates the frequency adjustment required by previous devices.
- **Digital synchronization** locked onto half line frequency thereby yielding perfect interlaced display and excellent stability with noisy video signal.
- **Automatic 50/60 Hz standard recognition** and switching the corresponding display amplitude.
- **Optimized synchronization in VCR mode.**
- **Generation of various accurate time intervals**, such as narrow "sync windows" thus reducing considerably the vertical image instability in case of for instance, mains interference, superimposed on frame sync pulse.
- **Generation of vertical blanking** signal for spot flyback and to **protect the picture tube in case of scanning failure.**

V.6.1 - Frame sync extraction

The main duty of this stage is to extract the frame sync pulses contained in composite sync signal.

Figure 52 : Sync extractor block diagram



Two current generators are used to charge and discharge the integrated capacitor "C". The discharge generator ($I_C + I_D$) is driven by the composite sync signal.

The ΔV_C across capacitor is : $-\frac{I_D \cdot t_{SYNC}}{C}$

During frame trace, the capacitor is discharged at each line sync pulse thereby generating a ΔV of -0.94V with respect to 5.6V and then recovers the charge by current "I_C". The comparator output remains low.

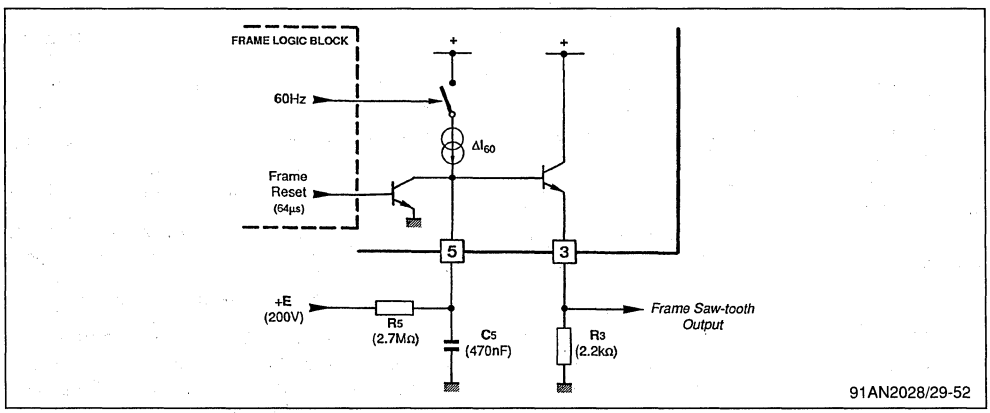
The discharge time is 27µs at the first line sync inversion applied to comparator input. The voltage "V_C" then falls from 5.6V to 0.2V and triggers the comparator "C_0" which will deliver a frame sync pulse when "V_C" crosses the 2.8V level.

The overall arrangement behaves as an integrator and will therefore suppress any noise susceptible to be present on input signal.

An external capacitor pin 20 can be added to the integrated capacitor C to increase the frame sync time constant.

V.6.2 - Frame saw-tooth generator

Figure 53

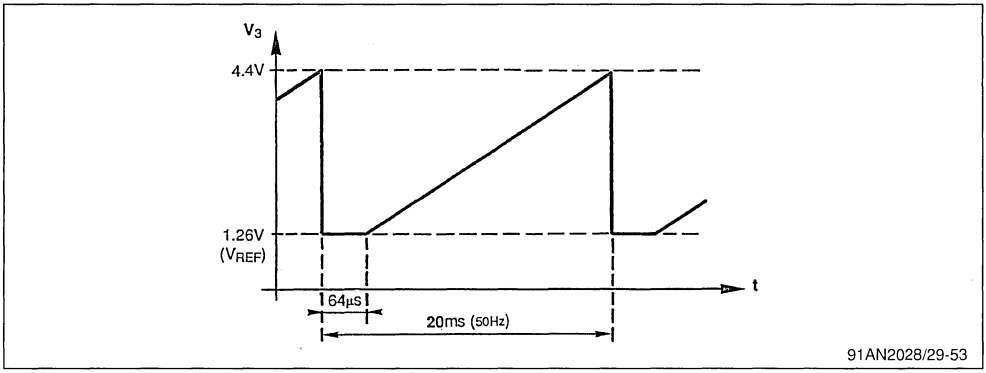


The frame saw-tooth is generated by an external RC network on pin 5.

The time constant "R5 x C5" is much higher than the frame period. Therefore, the generated saw-tooth is quite linear.

The network is discharged by an internal transistor, controlled by the frame logic block.

Figure 54



V.6.2.1 - *60Hz STANDARD SWITCHING*

The NTSC standard requires a vertical picture scanning frequency of 60Hz, i.e. a saw-tooth period of 16.66ms.

In order to obtain an identical deflection amplitude whatever the standard (50 or 60Hz), the saw-tooth amplitude for both periods must be the same.

60Hz standard recognition is performed automatically by the frame logic block, which will issue a signal to drive a current generator "ΔI_{60}". This current will be summed with the external charge current and will increase the saw-tooth slope, so as to yield same saw-tooth amplitude to that set in 50Hz standard. This current is centered around 14µA and is a fraction of I_{REF} applied to pin 14.

Employing the recommended component values for network connected to pin 5, this current will result in identical amplitude in both standards.

$$\Delta V_5 = \frac{I_{60} \times T_{60}}{C_5} = \frac{I_{50} \times T_{50}}{C_5} \Rightarrow I_{60} = I_{50} \times \frac{60}{50} = 1.2 \times I_{50}$$

$$I_{50} = \frac{E}{R_5} = \frac{200V}{2.7M\Omega} = 74\mu A \Rightarrow I_{60} = 88\mu A$$

therefore $\Delta I_{60} = 14\mu A$

V.6.3 - Functions of frame logic block

This section is fully implemented by I^2L logic gates. It is clocked by an accurate "H/2" clock running at half line period (32µs). The required periods and time intervals are obtained by counting the clock pulses.

For the sake of clarity, timing signals so obtained are labeled by the line number corresponding to video signal.

The time corresponding to "x" scanned lines with respect to the beginning of frame saw-tooth (RESET) is therefore :

$t_x = 64\mu s\ (x - 1) + 32\mu s$

Figure 55

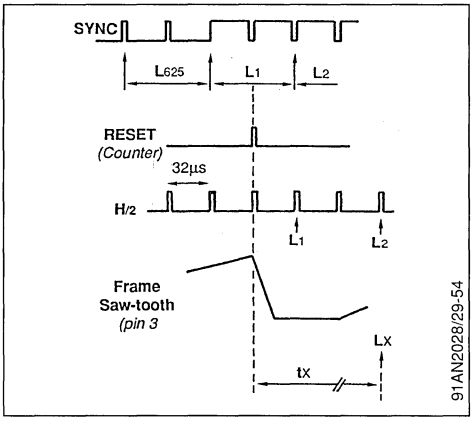
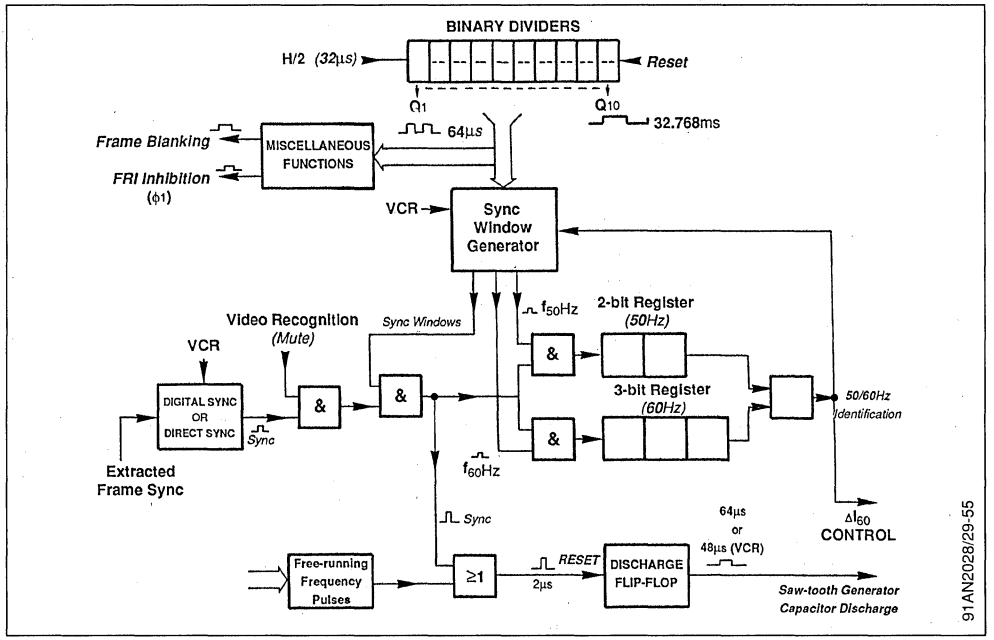


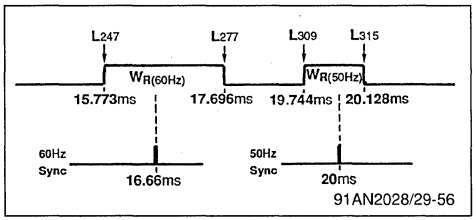
Figure 56 : Block Diagram



V.6.3.1 - 50/60 Hz Standard recognition

This function is performed by two shift registers which are loaded by sync pulses (if present) and if these pulses fall within the time interval specific to each standard. These intervals are called "Register Windows" and labeled "$W_R(50)$" and $W_R(60)$.

Figure 57



a. 50 Hz Standard Recognition

This identification is considered valid if two sucessive sync pulses applied to 50 Hz shift register fall within the 50Hz window "$W_R(50)$". At the time of synchronization capture, the first pulse will reset the counters. The second pulse, if present, will then trigger the 50Hz identification 20ms later [$I_D(50) = 1$].

The identification is not valid if two sucessive 50Hz pulses are not detected. Identification signal is also used to reduce the vertical synchronization window in 50Hz standard thereby offering excellent noise immunity against noise susceptible to be present in sync signal and hence good display stability.

b. - 60 Hz Standard Recognition

This identification is validated after three sucessive sync pulses at 16.6µs period have been detected. Three pulses are necessary to ascertain the identification prior to switching the saw-tooth amplitude. The identification signal [$I_D(60) = 1$] is also used to reduce the synchronization window and, in case of one or two missing pulses close to 60Hz, to set the free-running frequency.

V.6.3.2. - Vertical synchronization window - Free-running period

In the absence of sync pulse various free-running periods are specified. Since vertical scanning must be always active, these free-running periods must be higher than those of 50 and 60Hz standards so as to ensure synchronization.

An other window, allowing synchronization only at the end of scanning, is also necessary. Upon syn-

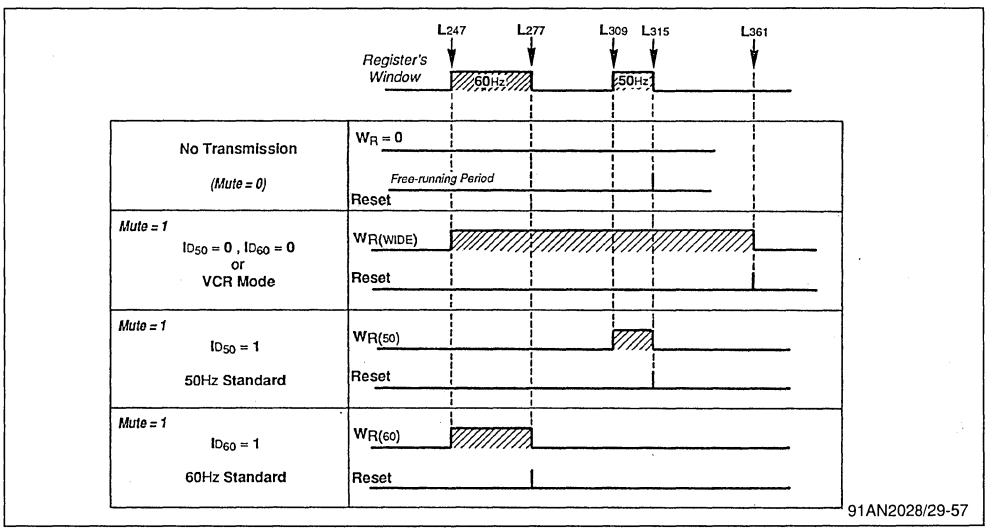
chronization, this window will allow vertical flyback only at the bottom of screen. This window should be narrow for good noise immunity but also wide enough to yield, upon synchronization, a capture time unperceptible on screen.

In our case, as long as no standard identification takes place the window will remain wide, and once one of the standards has been identified, the window will be considerably reduced.

In VCR mode, this window will be always wide since frame frequencies delivered in high-speed search, slow review and picture pause modes are very much variable and must be taken into consideration.

In the absence of transmission (Mute = 0), synchronization is disabled (so as to avoid incorrect synchronization due to noise) and the free-running frequency is around 50Hz. This will eliminate the occurrence of picture overlay at the end of trace at a lower free-running frequency.

Figure 58 : Definition of Synchronization Windows and Free-running Periods



Maximum capture time

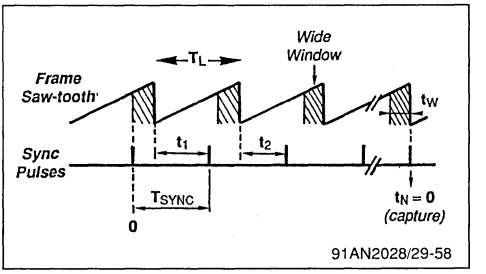
The worst case capture time occurs when the first sync pulse just precedes the sync window.

Let's find the number of periods necessary for the capture to occur, i.e. tn = 0.

$$\Rightarrow n = \frac{T_L - T_W}{T_L - T_{SYNC}}, \; T_L = 23ms, \; T_W = 7.3ms$$

- 50Hz : the number of periods is 6
  $\Rightarrow T_{CAPTURE(MAX)} = 120ms$
- 60Hz : the number of periods is 3
  $\Rightarrow T_{CAPTURE(MAX)} = 50ms$

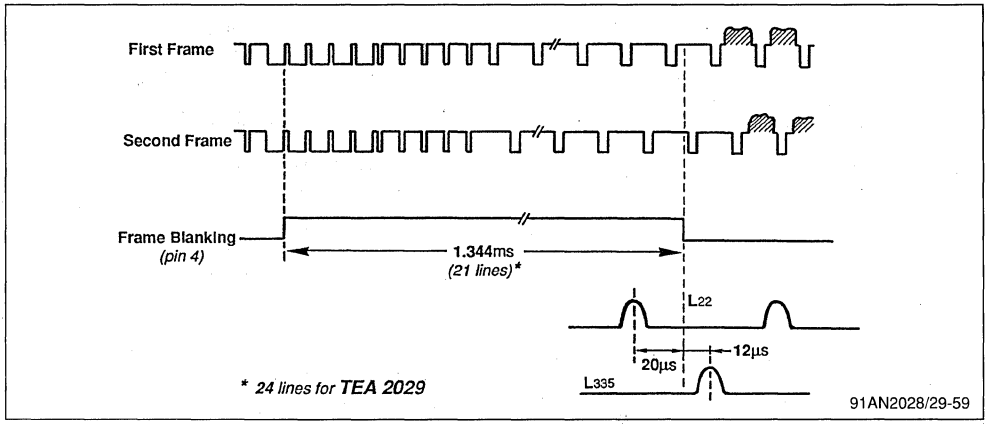
Figure 59



V.6.3.3 - *Frame blanking signal*

This signal is necessay to blank the display during each frame flyback. It is triggered at the beginning of frame saw-tooth flyback. The duration of this signal is 1.344 ms (or 21 lines).

Figure 60



This "frame blanking" signal is available through pin 4 (TEA2028 only) which is an open-collector output.

It is also present within the normalized super sandcastle signal on pin 11 (TEA2028 and TEA2029).

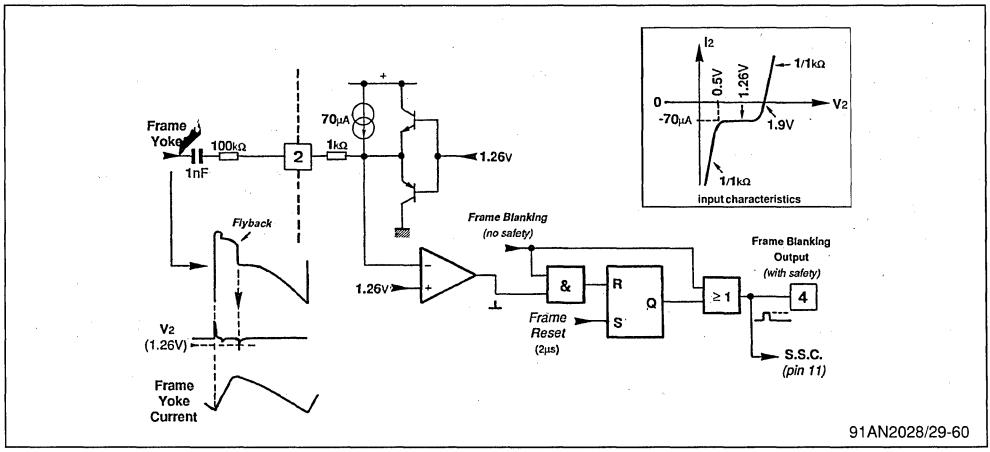
V.6.3.4. - Frame blanking safety (TEA2028 only, for TEA2029 refer to section VII.5)

Its duty is to protect the phosphor coating of picture tube in case of any problem with vertical deflection function such as scanning failure.

A signal to monitor correct scanning is provided by the frame yoke and applied to pin 2.

In case of any failure, all frame blanking outputs are disabled and go high thereby blanking the entire screen.

Figure 61 : Block diagram



During trace phase, the voltage across frame yoke has a parabolical shape due to the coupling capacitor in series with yoke. During frame flyback, the current through frame yoke must be rapidly in-

verted. Conventionally, a two-fold higher supply voltage is applied across the yoke. This will produce an overvoltage called "flyback".

The safety monitoring status is detected on the falling-edge of flyback, i.e. at the beginning of scanning. A differentiator network is used to transmit only fast voltage variations.

The required pulse is then compared to 1.26 V level. Frame blanking goes high in the absence of negative pulse (zero deflection current) or if the pulse does not fall within the first 21 lines (exagerated over-scanning).

V.7 -Switching power supply driver stage

Switching takes place on the primary side (mains side) of a transformer by using TEA2164 SMPS Controller manufactured by SGS-THOMSON Microelectrics.

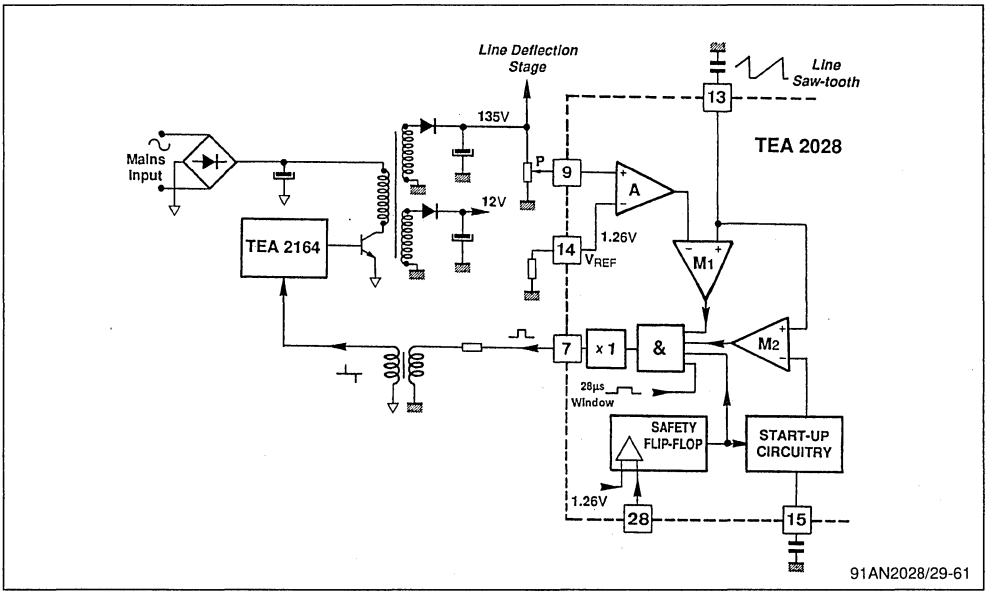
Required voltage values are obtained by rectifying different voltage outputs delivered through secondary windings. The horizontal deflection stage is powered by one of these outputs delivering around hundred volts.

This voltage source must be regulated since any voltage fluctuation will yield variations of the horizontal display amplitude.

The TEA2028 monitors this voltage and transmits the regulation signal to the primary controller circuitry via a small pulse transformer. The characteristics of this regulation signal are directly related to the conduction period of switching transistor.

V.7.1 - Power supply block diagram

Figure 62



V.7.2 - General operating principles

A fraction of the 135V output voltage to be regulated is compared to the 1.26V reference voltage. Resulting error signal is amplified and then applied to phase modulator "M_1", which will deliver a square waveform at line frequency whose duty cycle depends on the value of input voltage "V_9".

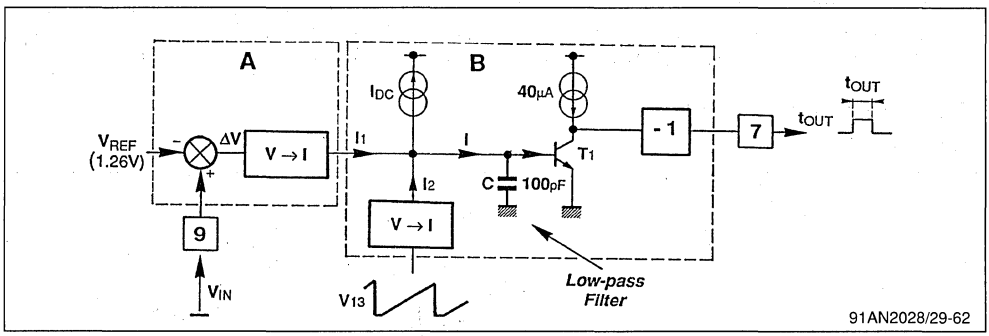
A second phase modulator "M_2" will determine the conduction period as a function of voltage on pin 15. This function is mandatory for system start-up.

A 28µs window is used to limit the conduction period of the primary-connected transistor.

Supply output (pin 7) and line output (pin 10) will be disabled if any information indicating abnormal operation is applied to safety input (pin 28). Consequently, all power stages are disabled and the TV set is thus protected.

V.7.3 - Electrical characteristics of the internal regulation loop

Figure 63



The phase modulator implemented by a simple transistor "T1" will compare in current mode, the image of amplified input (i_1) with saw-tooth current (i_2) at line frequency. With "i_2" rising, as soon as the sum of "$i_1 + i_2 - I_{DC}$" goes positive, the transistor enters into saturation thus determining the output conduction period.

A low-pass filter implemented by combination of a 100pF capacitor and the input impedance of transistor "T_1", attenuates all frequency variations higher than the line frequency.

- Input Amplification :

$$A = \frac{di_1}{dV_{IN}} = 3.3\mu A/mV$$

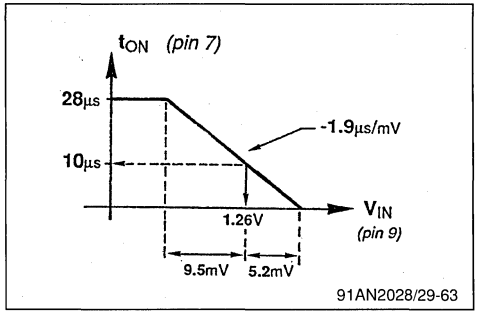
- Modulator conversion gain :

$$B = \frac{dt_{OUT}}{di_1} = -0.558\mu s/\mu A$$

- Overall gain of the internal loop :

$$\frac{dt_{OUT}}{dV_{IN}} = -1.9\mu s/mV \times \frac{1}{1 + j\frac{f}{f_0}} \quad (f_0 = 15kHz)$$

Figure 64 : Conduction period (pin 7) versus Input voltage (pin 9)



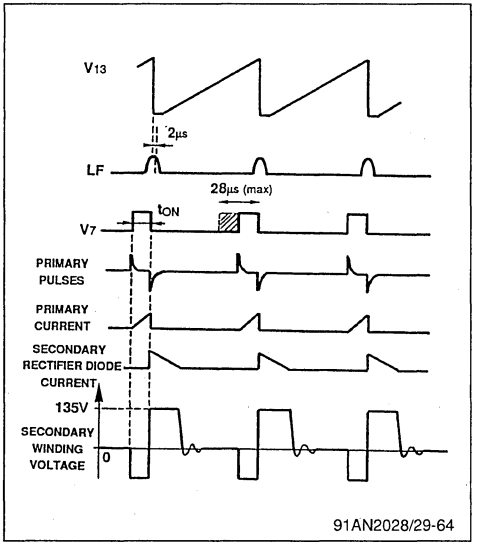
SMPS WAVEFORMS

For discontinous mode "flyback" configuration

The primary-connected transistor is turned-off during the line flyback.

All interference signals due to switching and susceptible to affect the video signal will not therefore be visible on screen.

Figure 65



Regulation Characteristics

The following characteristics have been measured on a large screen and yield excellent results :

- 135V voltage regulation as a function of mains voltage : better than 0.5% for mains voltage variations of $170V_{RMS}$ to $270V_{RMS}$ (P = 60W at 135V)
- 135 V voltage regulation as a function of load : better than 0.5% for a delivered power of 35W to 120W.

This type of power supply offers the following advantages :

- Overall efficiency enhancement : better than 80%
- Reduction of interferences by synchronization on horizontal frequency
- Full protection of the primary-connected transistor in case of short-circuit or open-load on secondary terminals
- Can provide 1W to 7W, for TV standby mode operation (refer to TEA2164 application note).

V.7.4 - Power supply soft-start

When the TV set is initially turned on, control pulses are not yet available and consequently the controller block on primary side will impose a low-power transfer to the secondary winding. This power is produced by an intermittent switching mode called "Burst Mode".

As soon as the V_{CC} supply to TEA2028 exceeds 6V level, line and SMPS outputs are enabled. Since the filtering capactitors on secondary side cannot charge up instantaneously, the voltage to be regulated would not yet be at its nominal value. Without conduction period limitation upon start-up, the device will set a maximum cycle of 28µs which will result in a high current flow through the primary winding and thus through the switching transistor which will in turn activate the protection function implemented on primary side.

Consequently, the primary controller block will be inhibited and the set will not turn-on.

A start-up system has been implemented within TEA2028 to overcome this problem.

This soft start system, will upon initial start-up, use the image of the falling voltage on pin 15 to increase progressively the conduction cycle. The phase modulator "M2" compares this voltage with line saw-tooth voltage and delivers the corresponding limitation cycle.

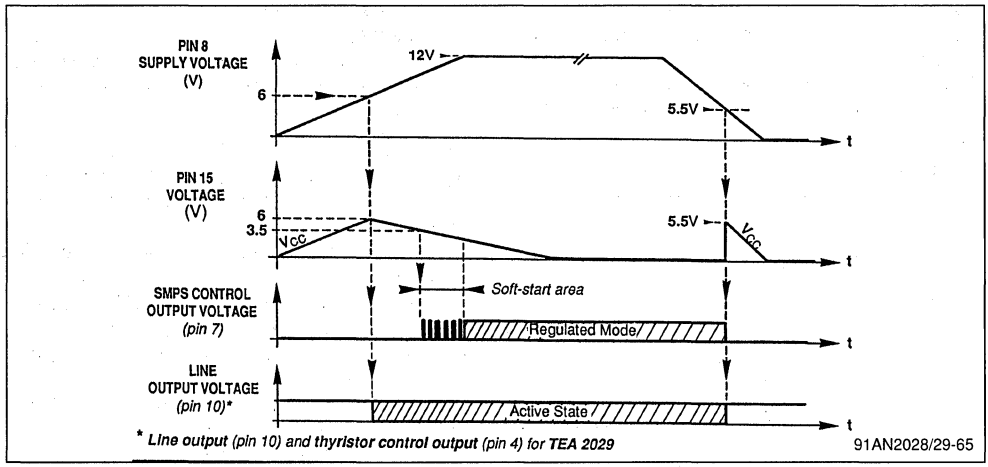
During supply voltage rising cycle [V_{CC} (pin 8) < 6V], the capacitor pin 15 will charge up rapidly while the voltage across it follows V_{CC}.

At $V_{CC} \geq 6V$, the capacitor is discharged via an internal current generator and the voltage across it decays linearly.

At $V_{15} \leq 3.5V$ (line saw-tooth peak-to-peak voltage), phase comparator "M2" delivers a low conduction period which will gradually increase.

The conduction period (pin 7) will rise until the secondary voltage reaches the value set by potentiometer "P". When this occurs, the loop is activated.

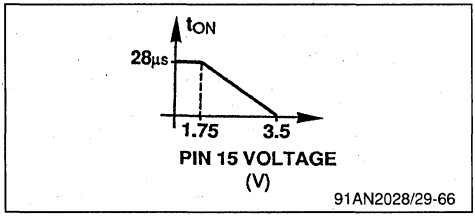
Figure 66



The pin 15 discharge current value is 100µA for a duration of 2µs line frequency.

Therefore $I_{D(AV)} = 100 \times \frac{2}{64} = 3.1\mu A$

Figure 67



Conduction period limitation voltage (pin 15)
$T_{ON(LIM)} = 56\mu s - 16 \times V_{15}$ (in µs)

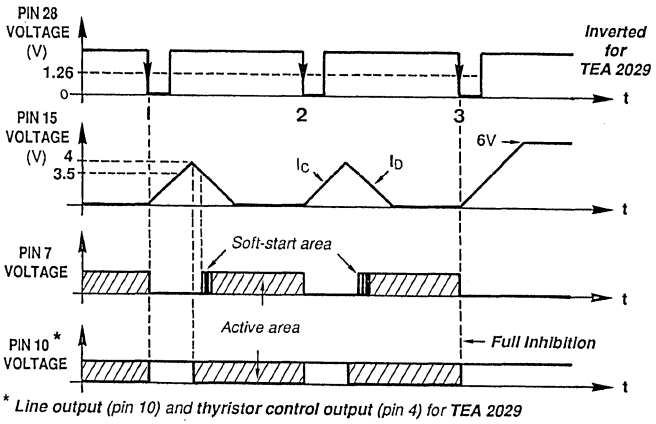
V.7.5 - Protection features

As soon as a safety signal ($V \leq 1.26$ V) is applied to pin 28, line and supply outputs (pins 10 and 7) are both disabled. Capacitor "C15" begins charging up until the voltage across it reaches 4 V ($K \times V_{CC}$). Outputs are again enabled and conduction period gradually increases as it occurs upon initial start-up.

The device will be definitively inhibited if the cycle of events is repeated 3 times.

For the device to restart, the internal 3-bit register should be reset which requires the V_{CC} to fall below 4 V.

Figure 68



Pin 15 charging current : $I_{C(AV)} = - I_{D(AV)} = - 3.1\mu A$

V.7.6 - TV Power supply in standby mode

V.7.6.1 - Regulation by primary controller circuit

This mode of regulation called "Burst Mode" is performed only by the primary controller circuit and is activated in the case of missing control pulses or in the absence of power supply to TEA2028.

In this mode, power available through secondary winding is limited. Refer to TEA2164 Application Note for further details.

Higher powers can be obtained by using the regulation feature offered by TEA2028. In this case, the horizontal output (pin 10) must be disabled.

V.7.6.2 - Regulation by TEA2028

In this case, all that is required is to disable the line scanning function thus reducing the overall power by 90%.

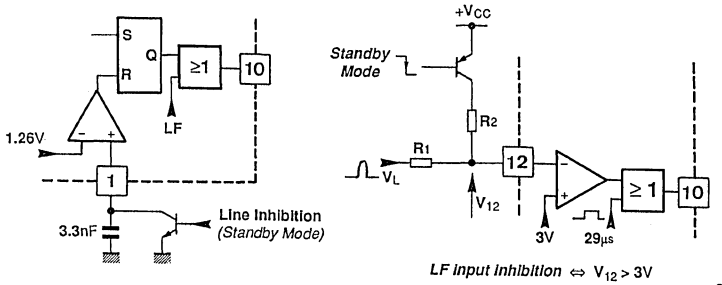
The device power supply regulation loop remains active, for minimum conduction period to be 1.5 ms the power delivered through secondary must be higher than 3 W.

Line Output Inhibition

Two alternatives are possible :

- Grounding flip-flop pin 1
- Apply a voltage higher than 3 V to pin 12.

Figure 69



V.8 - Miscellaneous functions

V.8.1 - Super sandcastle signal generator

This signal used in video stage, is available on pin 11.

It has 3 levels at specified time intervals :

- 2.5 V level

  Used for vertical blanking at each frame flyback. Its duration is 21 lines and is generated by the frame logic.

  This level will be maintained if vertical scanning failure is detected on pin 2.

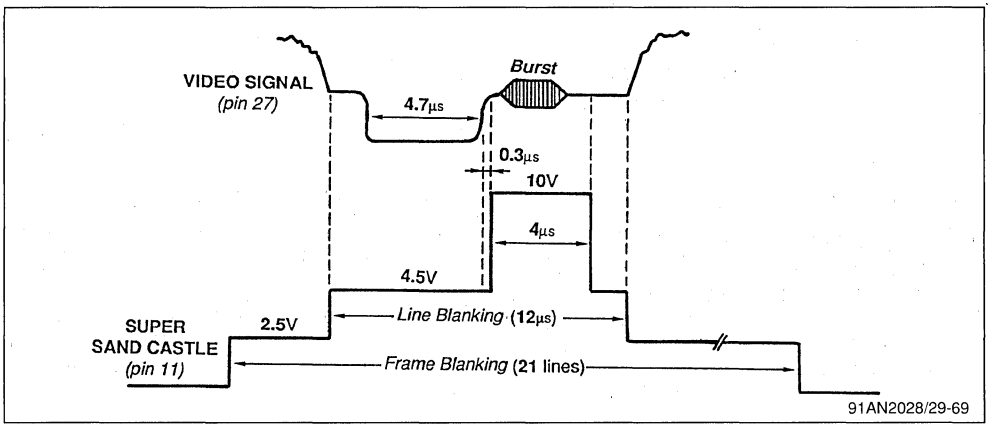
- 4.5V level

  Used for horizontal blanking, its duration is determined by comparing the line flyback signal on pin 12 to an internal voltage of 0.25V.

- 10 V level

  This signal is used by color decoding stage. Its duration of 4µs is determined by line logic circuitry. With respect to the video signal on pin 27, this level is positioned such that it is used to sample the burst frequency transmitted just after the sync pulse.

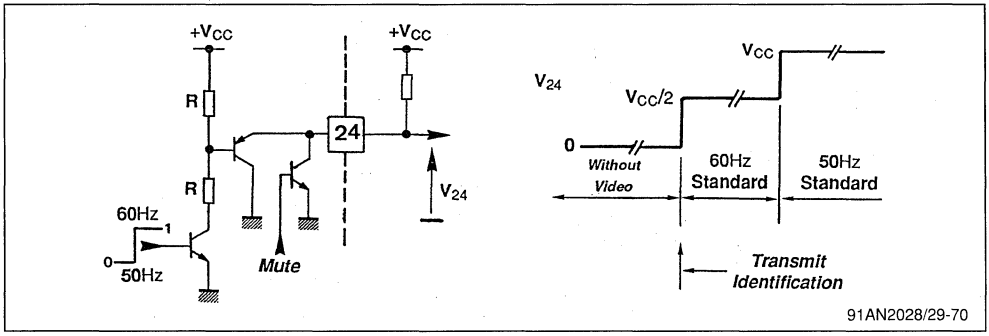
Figure 70



V.8.2 - Video and 50/60Hz standard recognition output

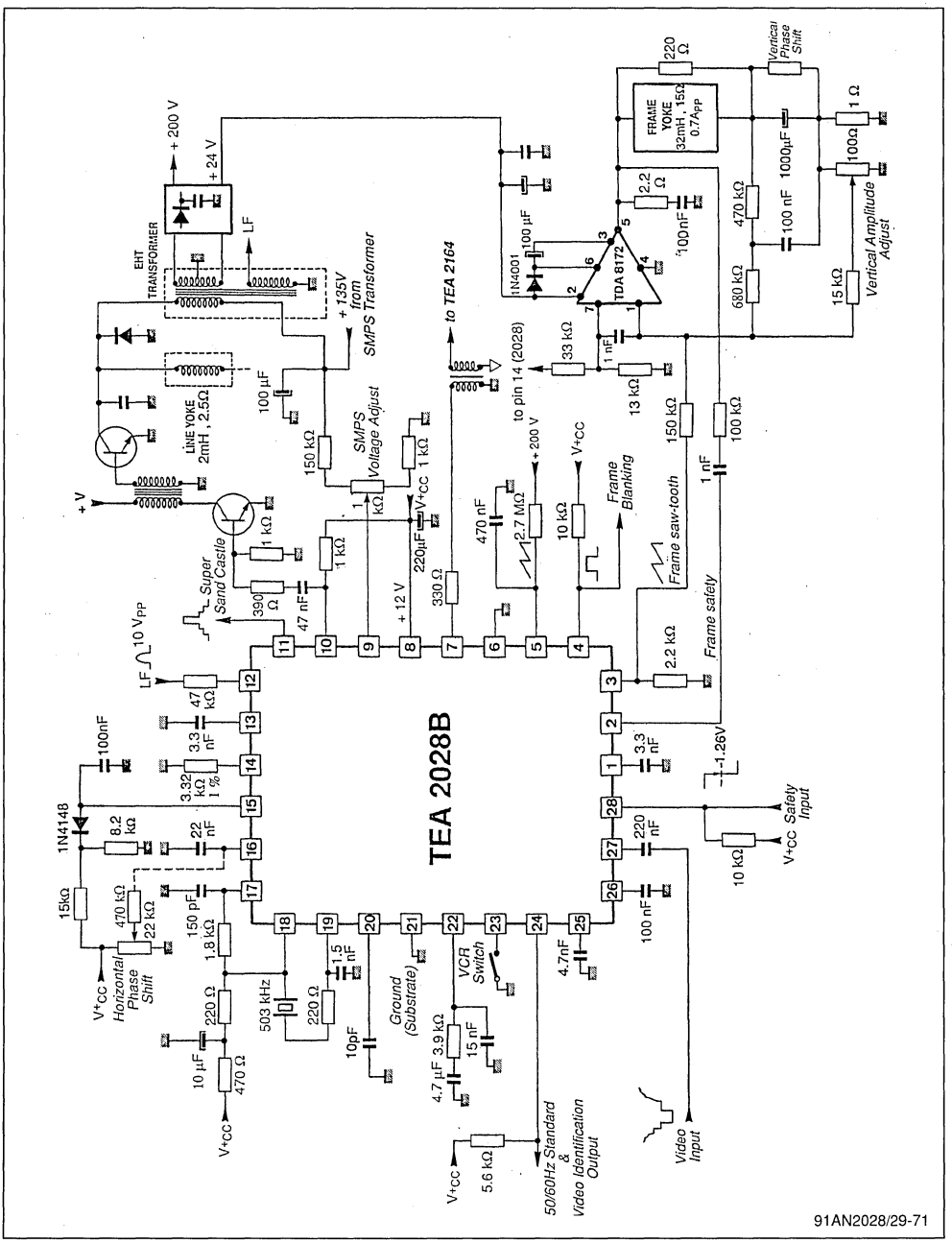
A 3-level signal is available at pin 24 for video identification (Mute) and for 50 and 60Hz standards recognition.

Figure 71



VI - TEA2028 APPLICATION DIAGRAM

Figure 72



VII - TEA2029 : DIFFERENCES WITH TEA2028

VII.1 - General

The TEA2029 has quite the same functions compared to TEA2028.

The main difference is that the TEA2029 incorporates a frame phase modulator intended to work with a switched mode vertical stage using a thyristor.

The TEA2029 can also be used with a linear vertical power amplifier such as the TDA 8170.

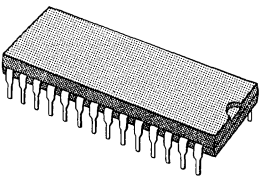
VII.2 - Pin by pin differences

Pin number	TEA2029C	TEA2028B
1	Differential inputs of the frame error amplifier (including frame blanking safety in case of vertical stage failure).	Capacitor for horizontal output duration adjustment (29µs typ. with c1 = 3.3nF)
2		Vertical blanking safety input
4	Frame output for thyristor control	Vertical blanking output (21 lines duration)
10	Horizontal output (26µs typ. duration)	Horizontal output (duration is adjustable)
11	Supersandcastle output (with a frame blanking duration of 24 lines)	Supersandcastle output (with a frame blanking duration of 21 lines)
12	Negative horizontal flyback input (115 V_{PP} through a 47 kΩ resistor)	positive horizontal flyback input ($10V_{pp}$ through a 47kΩ resistor)
20	Positive AGC key pulse output (low level when no video)	Capacitor for frame sync. time constant adjustment
28	Safety input (inhibition of SMPS, Horizontal and Frame outputs when $V_{28} > 1.26V$)	Safety input (inhibition of SMPS, Horizontal outputs when $V_{28} < 1.26V$)

VII.3 - TEA2029C Pin connections

Pin number	Description
1	Frame error amplifier non-inverting input
2	Frame error amplifier inverting input
3	Frame saw-tooth output
4	Frame output (for thyristor control)
5	Frame ramp generator
6	Power Ground
7	SMPS control output
8	VCC Supply voltage
9	SMPS regulation input
10	Horizontal output
11	Supersandcastle output
12	Horizontal flyback input
13	Horizontal saw-tooth generator
14	Current reference
15	SMPS soft-start and safety time constant
16	Φ2 phase comparator capacitor (and horizontal phase adjustment)
17	VCO phase shift network
18	VCO output
19	VCO input
20	AGC key pulse output
21	Substrate Ground
22	Φ1 phase comparator capacitor
23	VCR switching input
24	Video and 50/60Hz identification output (Mute)
25	Video identification capacitor
26	Horizontal sync detection capacitor (50% of peak to peak sync level)
27	Video input
28	Safety input

Package : DIP28



VII.4 - Frame phase modulator

The Tranconductance Amplifier "A1" converts the differential input voltage into two output currents "I_{S1}" and "I_{S3}".

- A1 transconductance = $\frac{I_{S1}}{V_{IN}} = 10\mu A/mV$
- B transconductance = $\frac{I_{S2}}{V_2} = 40\mu A/V$
- Transfer characteristic = $\frac{\Delta t_{OUT}}{\Delta V_{IN}} = 6.4\mu s/mV$

The filter time constant is maximum near the operating point when $I_{S1} \cong I_{S2}$

In this case :

- The base current of T_1 = "I_{S2} - I_{S1}"
- The filter band-pass = 15kHz

The maximum conduction period of "40µs" is determined by the horizontal logic circuitry.

The frame frame flyback is detected by transistor "T3".

There is no feed-back during frame flyback and "I_{S3}" is maximum (higher than I_4) which will drive the "T3" into conduction.

Figure 73

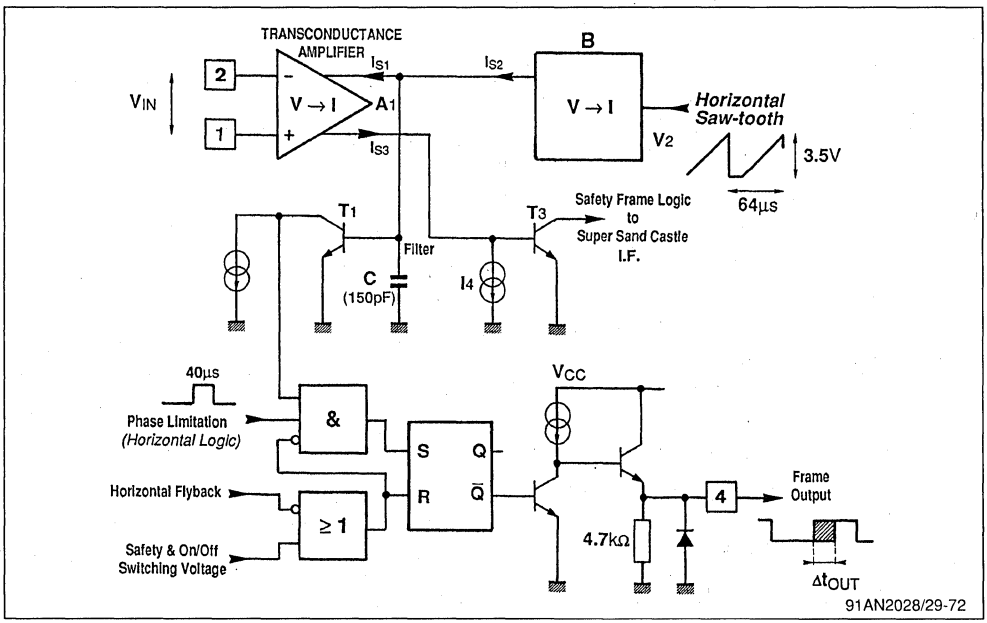
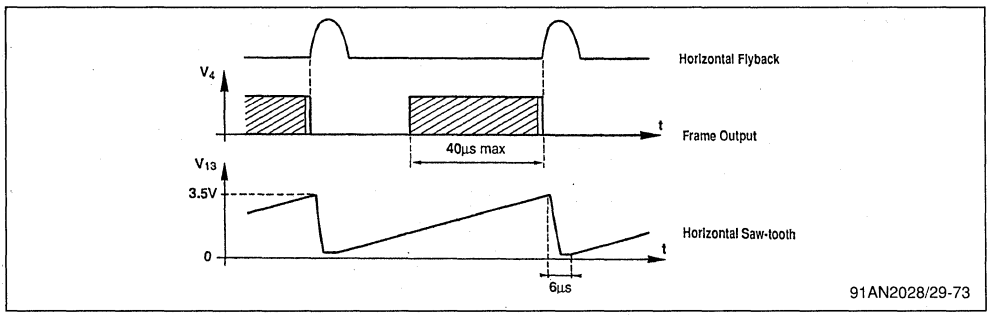


Figure 74

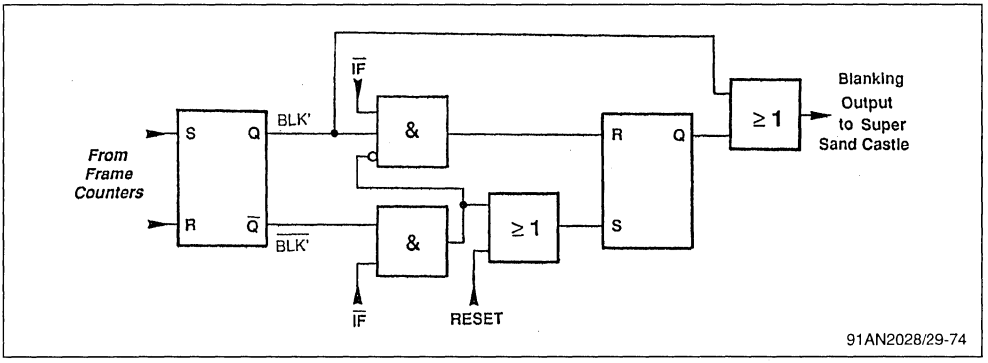


VII.5 - Frame blanking safety

- During trace : $I_{S3} < I_4 \Rightarrow$ T3 is blocked.
- During flyback : $I_{S3} > I_4 \Rightarrow$ T3 conducts.

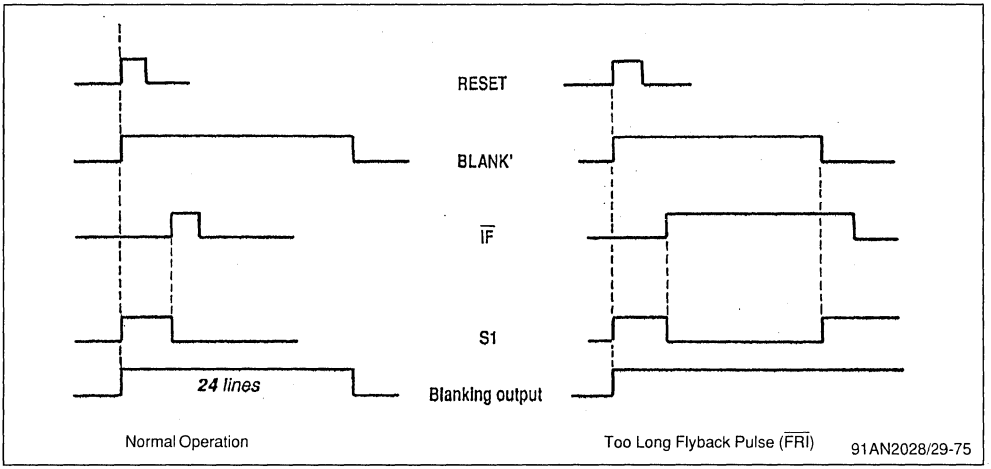
In the absence of flyback detection or if the flyback interval is longer than the blanking time, the sandcastle low level remains constant at 2.5V so as to protect the picture tube in the absence of frame scanning.

Figure 75 : Frame Blanking Safety Block Diagram



- "IF" signal is delivered by Frame Error Amplifier (see Frame phase modulator figure)
- $\overline{IF}$ is high during the Frame Flyback interval

Figure 76



VII.6 - On-chip line flip-flop

Figure 77

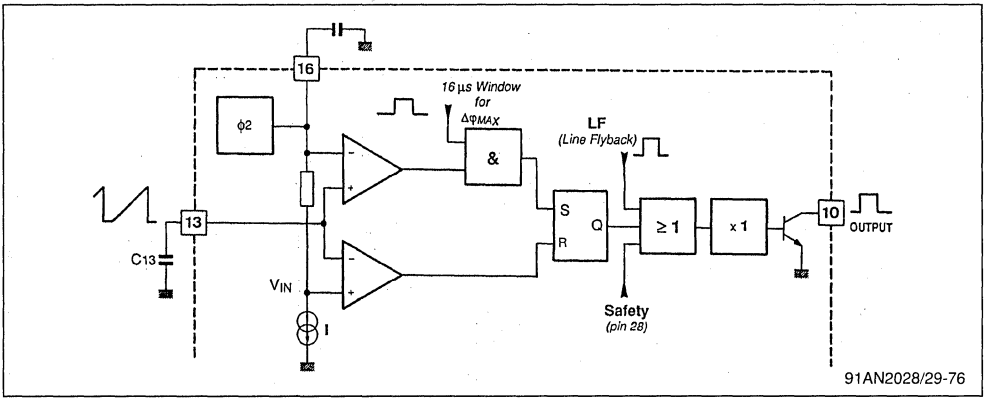
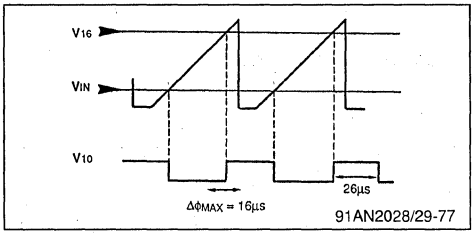


Figure 78



$T_{10} = 35 \times T_{VCO} - K \cdot R14 \cdot C13$

$= 70 \times 10^{-6} - 4R14 \cdot C13$

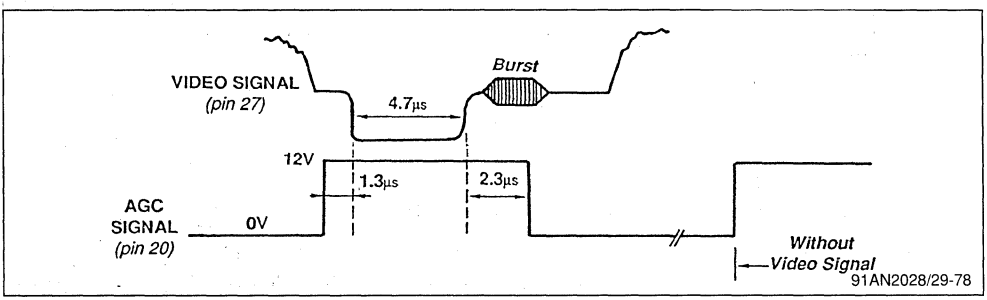
Where T_{VCO} is the V_{CO} period of oscillation on pin 18.

- If in synchronized mode :
- $T_{VCO} = 2\mu s$
- $R14 = 3.32k\Omega$
- $C13 = 3.3nF$

ThereforeT10 = 26µs (nominal value)

VII.7 - AGC key pulse

Figure 79



As illustrated below, this signal is used in some TV sets to perform sampling window for Automatic Gain Control of picture demodulation network.

This system is called "clamped" AGC, and locks the demodulated line sync amplitude and hence sets the video signal amplitude.

This signal generated by line logic circuitry is correctly positioned by the first phase locked loop "φ1" and includes the line sync pulse of the video signal. This is an open-collector output.

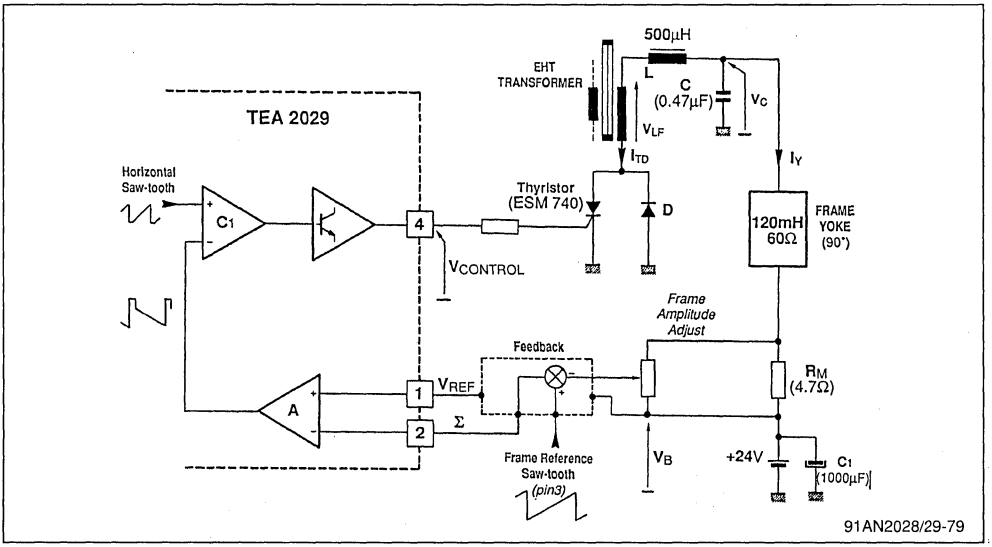
VIII - APPLICATION INFORMATION ON FRAME SCANNING IN SWITCHED MODE (TEA2029 ONLY)

VIII.1 - Fundamentals

The secondary winding of EHT transformer provides the energy required by frame yoke.

The frame current modulation is achieved by modulating the horizontal saw-tooth current and subsequent integration by a "L.C" network to reject the horizontal frequency component.

Figure 80 : Block diagram



VIII.2 - General description

The basic circuit is the phase comparator "C_1" which compares the horizontal saw-tooth and the output voltage of Error Amplifier "A".

The comparator output will go "high" when the horizontal saw-tooth voltage is higher than the "A" output voltage. Thus, the pin 4 output signal is switched in synchronization with the horizontal frequency and the duty cycle is modulated at frame frequency.

A driver stage delivers the current required by the external power switch.

The external thyristor provides for energy transfer between transformer and frame yoke.

The thyristor will conduct during the last portion of horizontal trace phase and for half of the horizontal retrace.

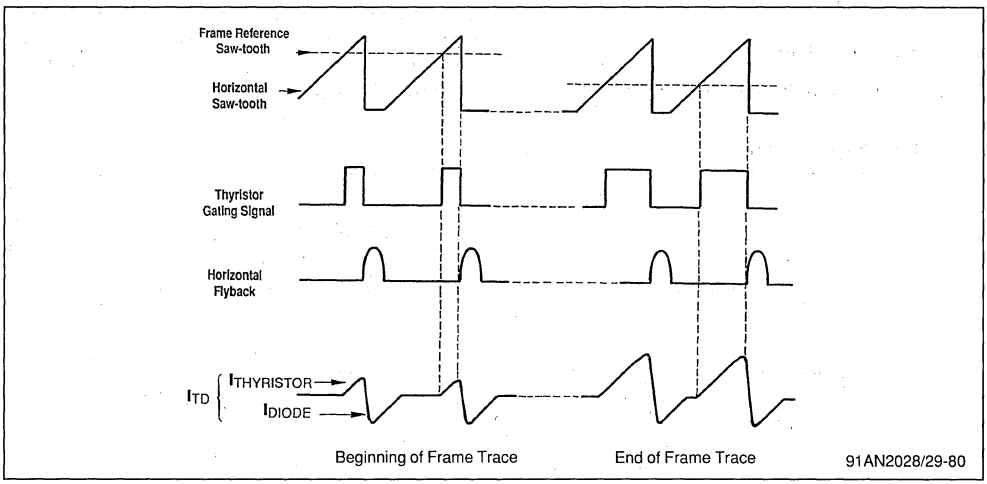
The inverse parallel-connected diode "D" conducts during the second portion of horizontal retrace and at the beginning of horizontal trace phase.

Main advantages of this system are :

- **Power thyristor soft "turn-on"**
  Once the thyristor has been triggered, the current gradually rises from 0 to IP, where IP will reach the maximum value at the end of horizontal trace. The slope current is determined by, the current available through the secondary winding, the yoke impedance and the "L.C." filter characteristics.
- **Power thyristor soft "turn-off"**
- The secondary output current begins decreasing and falls to 0 at the middle of retrace. The thyristor is thus automatically "turned-off".
- **Excellent efficiency of power stage** due to very low "turn-on" and "turn-off" switching losses.

VIII.3 - Typical frame modulator and frame output waveforms

Figure 81



VIII.4 - Frame power stage waveforms

Figure 82

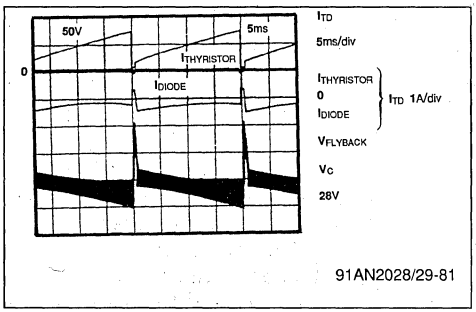


Figure 83

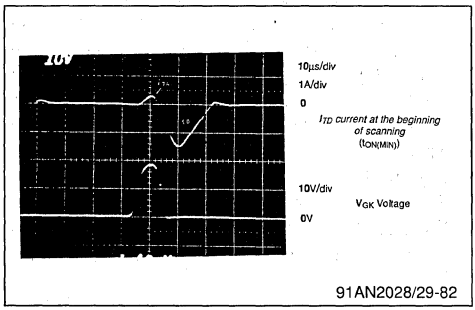


Figure 84

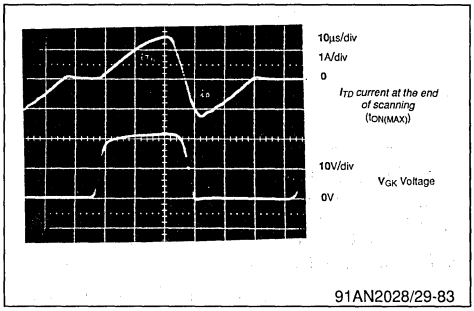


Figure 85 : Different horizontal conducting times during frame

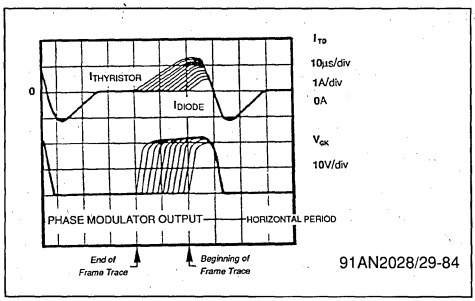
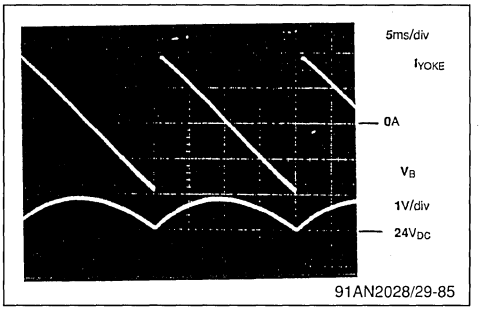


Figure 86



The bias voltage "V_B" is supplied by the secondary winding of EHT transformer. The parabolic effect is due to the integration of frame saw-tooth by the filtering capacitor "C1".

$$\Delta V_B = \frac{I_Y \cdot T}{8 \cdot C1} = 0.95V$$

Where :

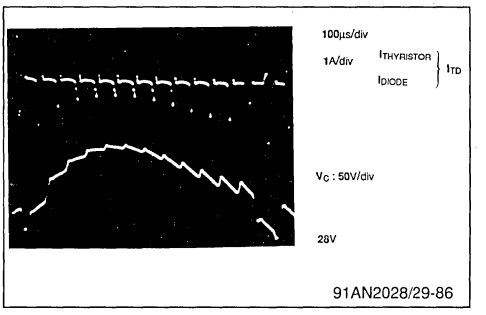
- I_Y : Peak-to-peak yoke current = 380mA$_{pp}$
- T : 20ms
- C1 = 1000µF

VIII.5 - Frame flyback

During flyback, due to the loop time constant, the frame yoke current cannot be locked onto the reference saw-tooth. Thus the output of amplifier "A" will remain high and the thyristor is blocked.

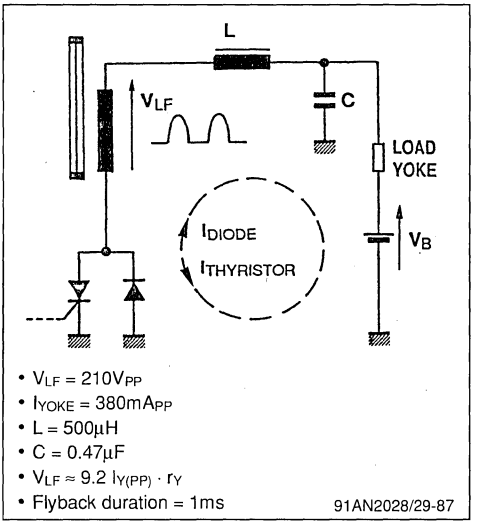
The scanning current will begin flowing through diode "D". As a consequence, the capacitor "C" starts charging up to the flyback voltage. The thyristor is triggered as soon as the yoke current reaches the maximum positive value.

Figure 87



EHT transformer winding
(for 90° tube : Yoke ⇒ L = 120mH, r_Y = 60Ω)

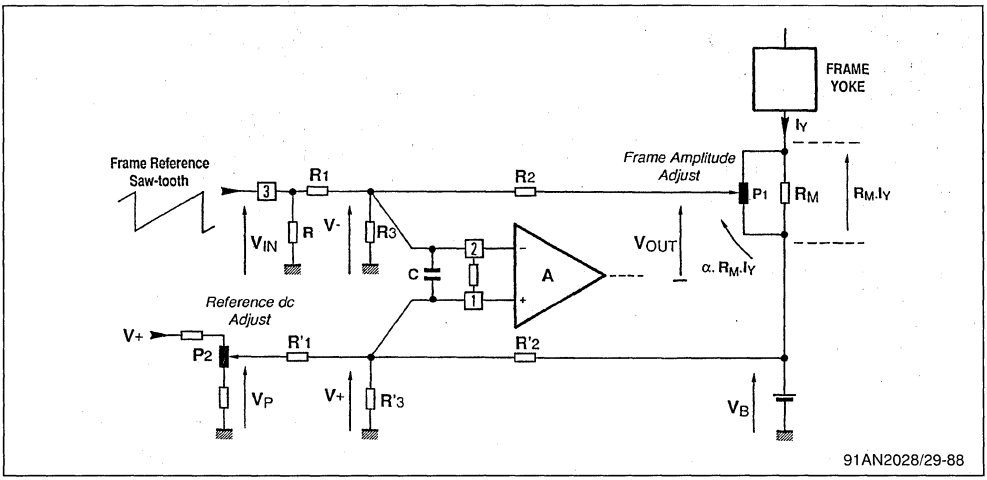
Figure 88



VIII.6 - Feed-back circuit

VIII.6.1 - Frame power in quasi-bridge configuration

Figure 89



This stage measures the frame scanning current in differential mode and compares it to the reference saw-tooth on pin 3.

The overall configuration is built around two symmetrical networks :

- "R_1, R_2, R_3" network : determines the dynamic saw-tooth voltage
- "R'_1, R'_2, R'_3" network : sets the bias voltage and the d.c. shift control.

$$\text{a.c. gain : } G = \frac{R_2}{R_1} = \frac{I_Y}{V_{IN}} \cdot \alpha \cdot R_M$$

where :

- I_Y : Peak-to-peak Yoke Current
- V_{IN} : Peak-to-peak saw-tooth voltage (pin 3)
- $\alpha \in [0,1]$: amplitude adjustment

VIII.6.1.1 - Choice of "R" value

The saw-tooth generator output is an emitter follower stage. Pin 3 output current must therefore be always negative.

$$R << R_1 \frac{V_{IN(MIN)}}{V_{BIAS} - V_{IN(MIN)}}$$

Where :

- V_{BIAS} : Bias voltage for pins 1 and 2
- $V_{IN(MIN)}$: Saw-tooth voltage low level

Example :

- $R1 = 22k\Omega$
- $V_{BIAS} = 5V$
- $V_{IN(MIN)} = 1.26V$

$$\Rightarrow R \approx \frac{R_1}{10}$$

VIII.6.1.2 - Influence of R_3 value

R_3 sets the bias voltage for pins 1 and 2. This voltage should be lower than 5.5V so as to enable the frame to function upon initial start-up at $V_{CC} = 6V$.

If the bias voltage is higher than this 5.5V level, the d.c. open-loop gain will fall thereby rendering the system more sensitive to d.c. drift.

Satisfactory results are obtained at V_{BIAS} values falling within 4V to 5V range.

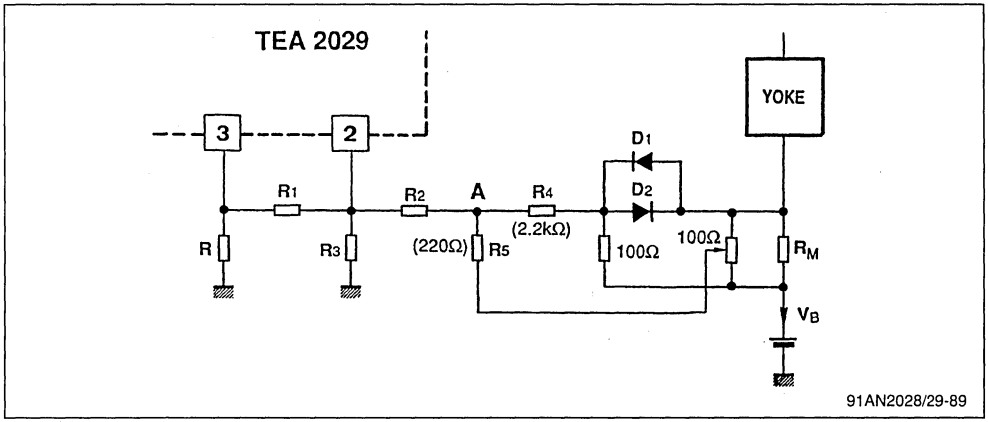
$$R_3 = R_2 \frac{V_{BIAS}}{V_B\,(V_{IN(MEAN)} \cdot G) - V_{BIAS}(1 - G)}$$

Where : $V_{IN(MEAN)}$: saw-tooth mean value (pin 3)

Capacitor "C" connected between pins 1 and 2 determines the system stability. Its value must be appropriately calculated as a function of "R_1, R_2 and R_3" values so as to reject the line frequency component.

VIII.6.1.3 - "S" Correction circuit in quasi-bridge configuration

Figure 90

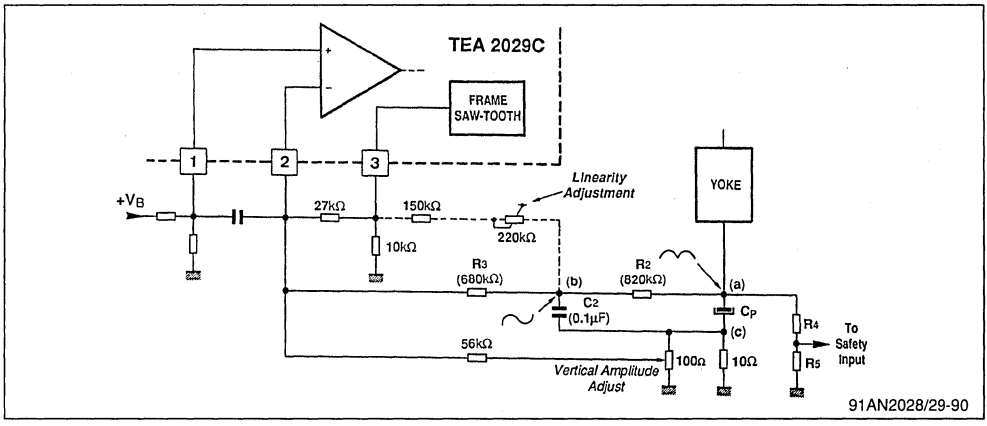


The "S" correction waveform is obtained using the non-linear "V_{DIODE}" versus "I_{DIODE}" characteristics of "D1" and "D2" diodes.

The signal pre-corrected by "D1", "D2" diodes and the feed-back signal through "R5", are summed at "A". The "S" correction level is determined by the ratio between "R4" and "R5" resistors.

VIII.6.2 - Frame scanning in switched mode using coupling capacitor

Figure 91



The parabolic voltage at (a) is integrated by "R2, C2" network and used for "S" correction.
The "S" waveform voltage at (b) is added to the saw-tooth voltage at (c). The "S" level is determined by "C2, R2, R3" network.

VIII.6.3 - Frame safety

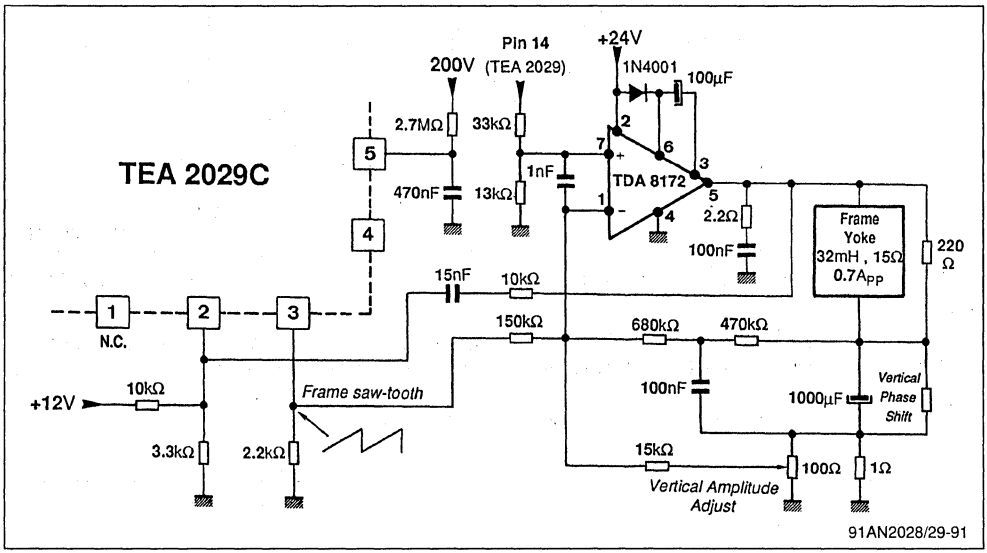
In case of failure in the loop, the thyristor may remain turned-off while the inverse parallel-connected diode conducts. This will result in a hazardeous situation where the voltage across the coupling capacitor "C_P" will reach an excessively high value.

To avoid such situation, the voltage at point (a) should be applied to the "Safety" input pin 28 after it has gone through the matching network "R4, R5".

VIII.7 - Frame scanning in class B with flyback generator

VIII.7.1 - Application diagram

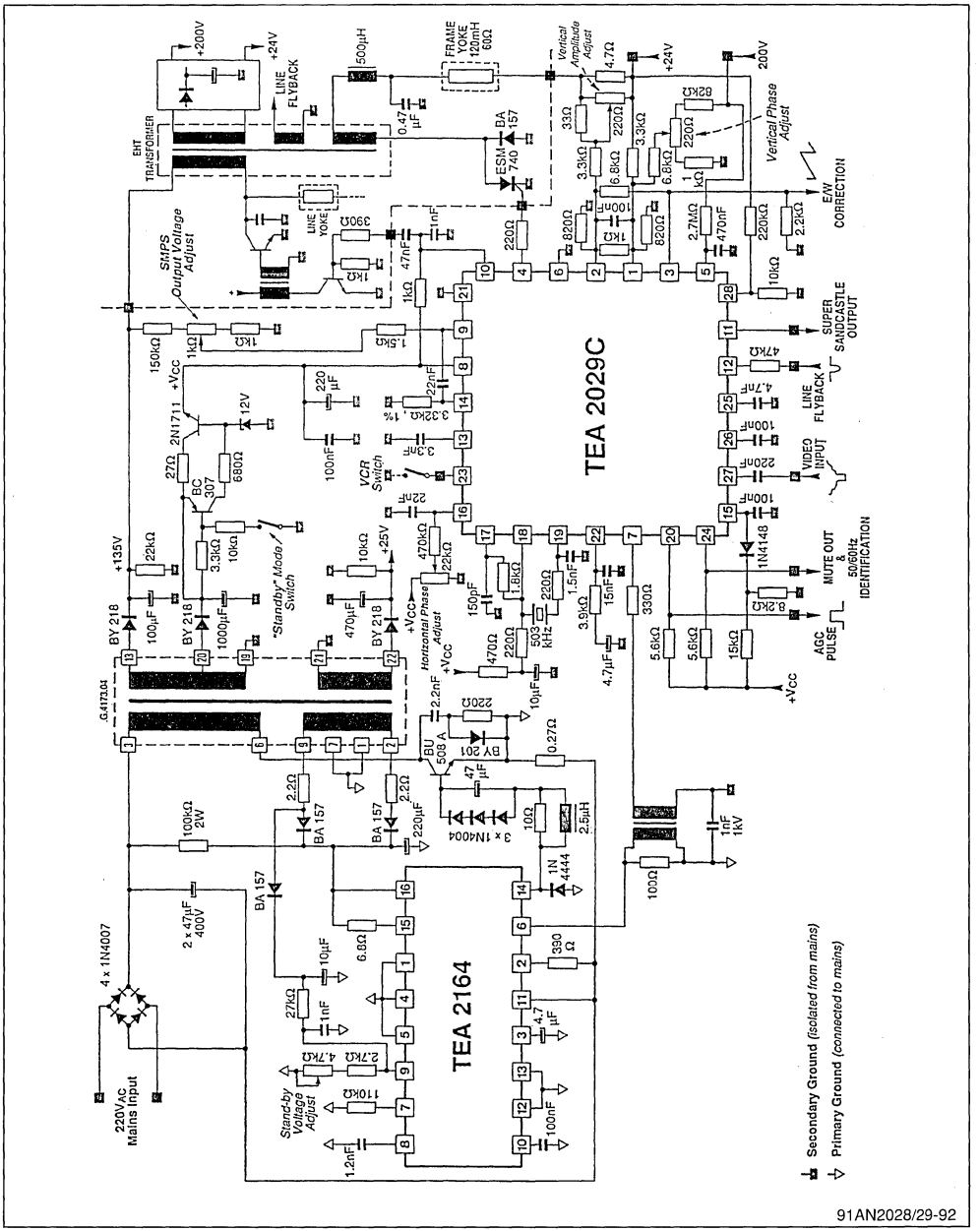
Figure 92



IX - TEA2029 APPLICATION DIAGRAM

Complete application with TEA2164

Figure 93



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA5170
SECONDARY CONTROLLER FOR MASTER-SLAVE STRUCTURE

By : T. PIERRE

SUMMARY

I - INTRODUCTION

The TEA 5170 is designed to work in the secondary part of SMPS, sending pulses to the slave TEA2164 which is located on the primary side of the main transformer.

The function of the regulation and synchronization are carried out by the TEA5170.

An accurate regulated voltage is obtained by duty cycle control.

The TEA5170 can be externally synchronized by a frequency higher or lower than the free-running frequency. This feature is particularly suitable for TV applications.

II - OPERATING PRINCIPLES OF MASTER-SLAVE STRUCTURE

This architecture offers two modes of operation :

- Master-slave mode (for normal operation)
- Burst mode (used during start-up and stand-by phases)

II.1 - Master-Slave mode

In this configuration, the master circuit located on the primary side, issues PWM pulses used for output voltage regulation. These pulses are sent via a pulse tranformer to the slave circuit (Figure 1). In this mode of operation, the falling edge of PWM signal may be synchronized by an external signal (e.g. by line flyback signal in TV applications).

II.2 - Burst Mode

During start-up and stand-by phases, no regulation pulses are issued by the master circuit and thus the slave circuit operates in burst mode. In this configuration, the slave circuit determines the switching frequency and the burst period. (See figure 2)

Figure 1

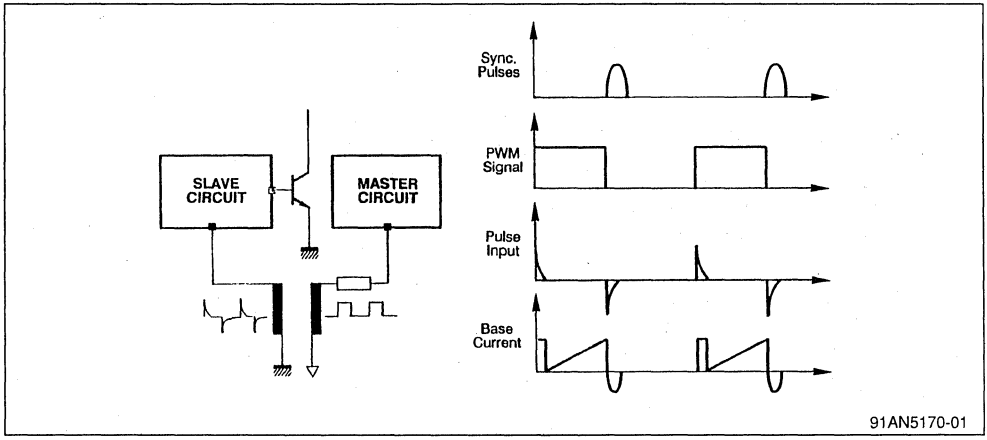
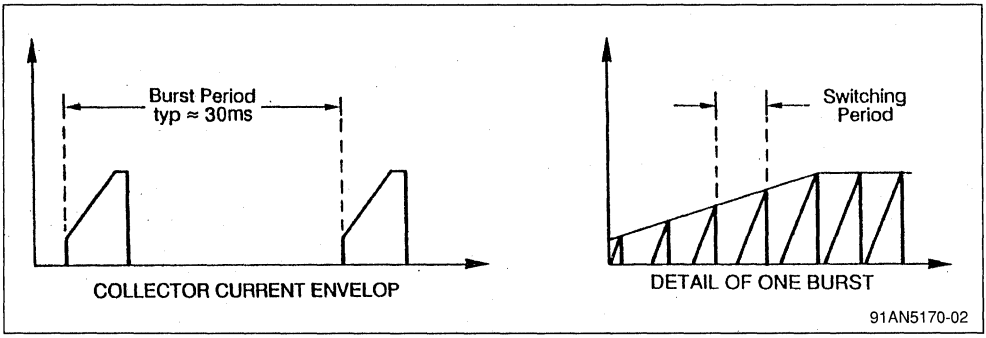


Figure 2 : Burst Mode Operation



II.3 - Operation of a Master-Slave Supply in TV Application

The arrangement generally employed is depicted in Figure 3. On the secondary side, a microcontroller is connected to the remote control receiver which issues control signals for stand-by and normal modes of operation. (Figure 4).

- In stand-by mode, the device power consumption is low (few Watts). The master will no longer send any control pulses to the slave which will consequently begin operating in burst mode.

Power supply regulation is performed by the slave circuit through the auxiliary winding.

- In normal mode of operation, the master circuit issues the PWM signal for regulation. The power supply operates in master-slave mode. The master circuit is simultaneously synchronized with the line flyback signal.
- Power supply start-up. As soon as the $V_{CC(START)}$ threshold is reached, the slave circuit begins operating in burst mode. While the secondary voltages are being stabilized, the microcontroller holds the TV set in stand-by mode.

Once the start-up phase is terminated, the set may remain in stand-by mode or switch into normal mode of operation.

Figure 3

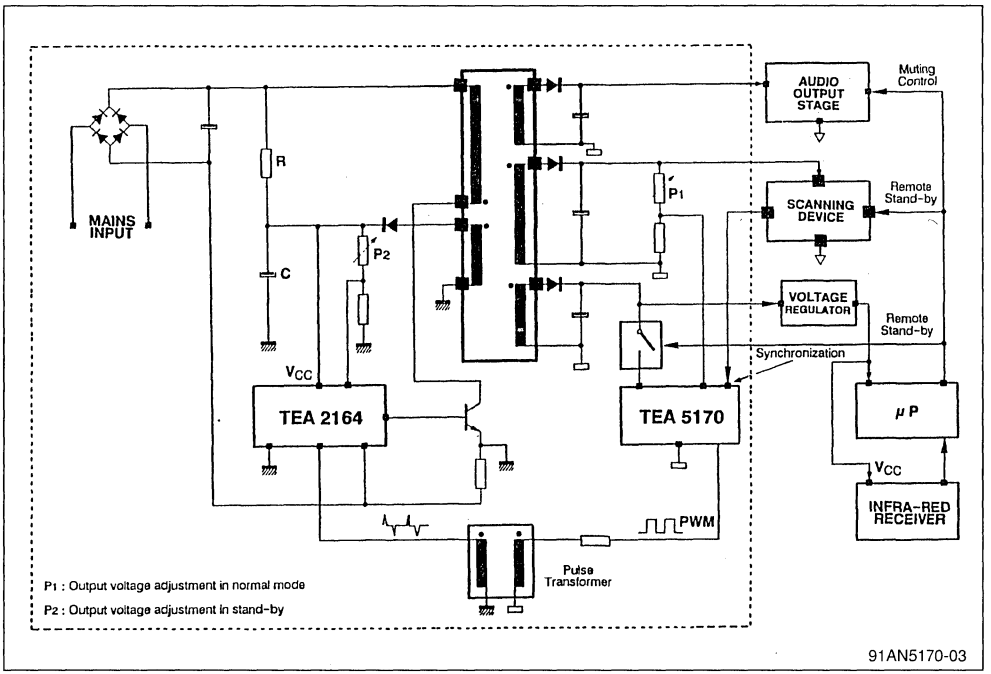
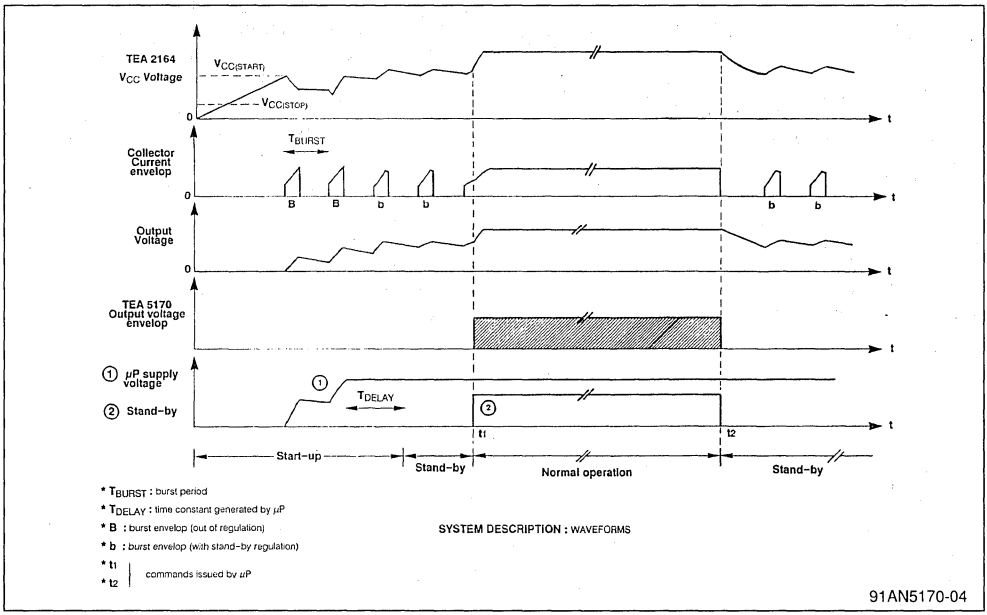


Figure 4

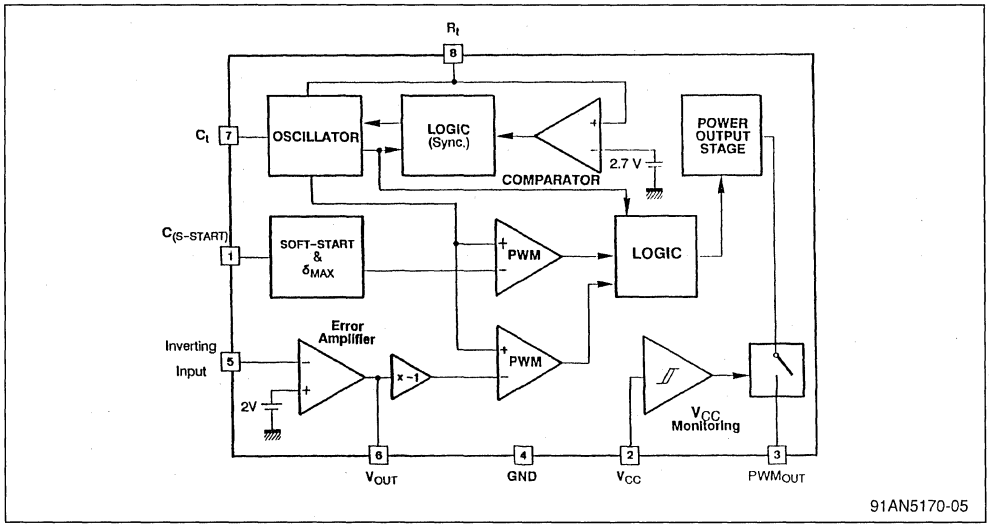


III - Description of TEA 5170

The TEA 5170 is a fixed frequency PWM signal generator operating in voltage mode regulation.

III.1 - Block Diagram

Figure 5



III.2 - Oscillator

The oscillator generates a linear saw-tooth signal and sets the free-running frequency. This oscillator can also operate in synchronized mode.

III.2.1 - Operation in free-running frequency mode. (See figure 6).

III.2.2 - Operation in synchronized mode

The oscillator is synchronized by forcing the saw-tooth return.

Enabling the synchronized mode (Figure 7)

The synchronized mode is enabled when the signal pulse on pin 8 (R_t) coincides with the oscillator saw-tooth return. The "C_t" capacitor charge current is then multiplied by a factor of 0.75.

The TEA 5170 will remain in synchronized mode as long as the synchronization pulses fall within the following window :

$(0.8\ T1 + T2) < T_{SYNC} < (1.33\ T1 + T2)$

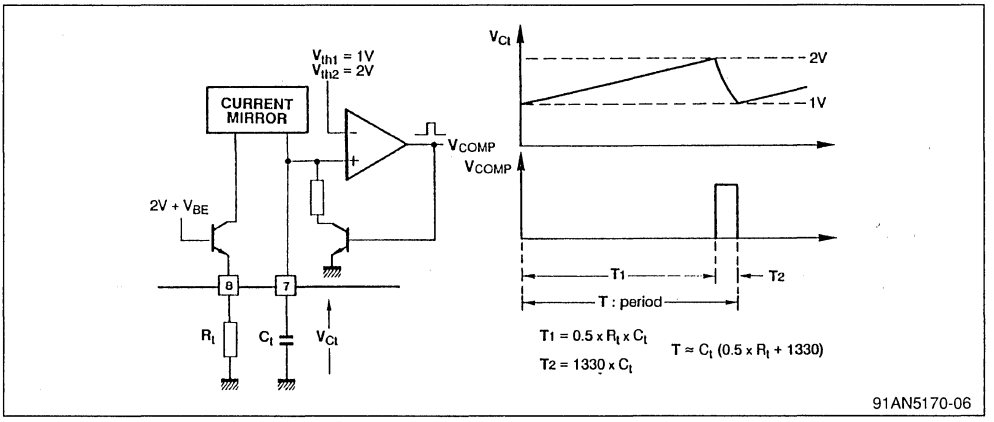
Where :

- T1 : C_t charge time in non synchronized mode.
- T2 : C_t discharge time

Synchronization signal (Figure 8)

Synchronization signal is applied to pin 8 "R_t" and the capacitor "C_t" is discharged when voltage "V_{Rt}" exceeds the "2.7 V" threshold.

Figure 6



Comment :

The internal current generator used to charge the "C_t" capacitor is disabled for the entire phase where "V_{Rt}" is higher than 2V. Thus, in order to maintain the saw-tooth shape of the oscillator signal, the "V_{Rt}" voltage should fall to 2V before the capacitor "C_t" full discharge.

Figure 7

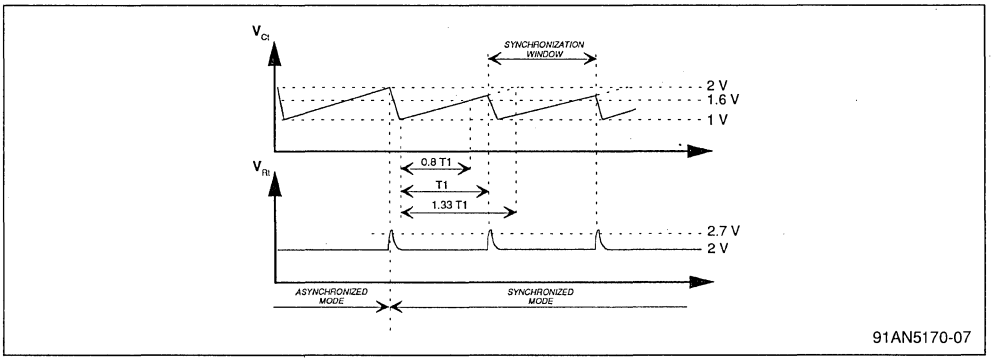
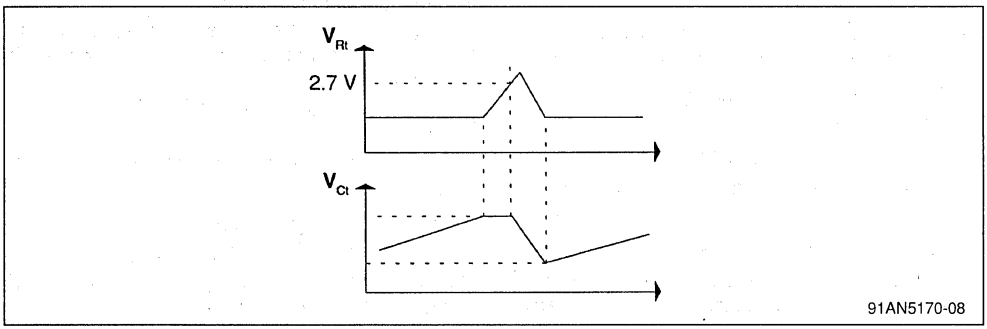


Figure 8



III.3 - Error Amplifier (Figure 9)

The on-chip error amplifier can be accessed through its inverting and output terminals.

The non-inverting input is internally tied to reference voltage level.

Comment :

An internal inverting amplifier sets the correct phase polarity of the error amplifier output signal for regulation.

III.4 - Pulse Width Modulation (Figure 9)

The TEA 5170 is a PWM signal generator operating in voltage mode. The pulse width is determined by comparing the error signal "V_{OM}" with the oscillator saw-tooth.

When the error signal "V_{OM}" exceeds the regulation range, internal threshold components will set a minimum conduction time $t_{ON(MIN)}$ and also limit the maximum conduction time $t_{ON(MAX)}$.

At initial start-up, a soft-start function implemented by linear charge of soft-start capacitor "$C_{(S\text{-}START)}$" is used to vary gradually the $t_{ON(MAX)}$ threshold. The output pulse width varies from $t_{ON(MIN)}$ to $t_{ON(MAX)}$ nominal value for $V_{C(S\text{-}START)}$ voltage variation of 0 to 2V.

Figure 9

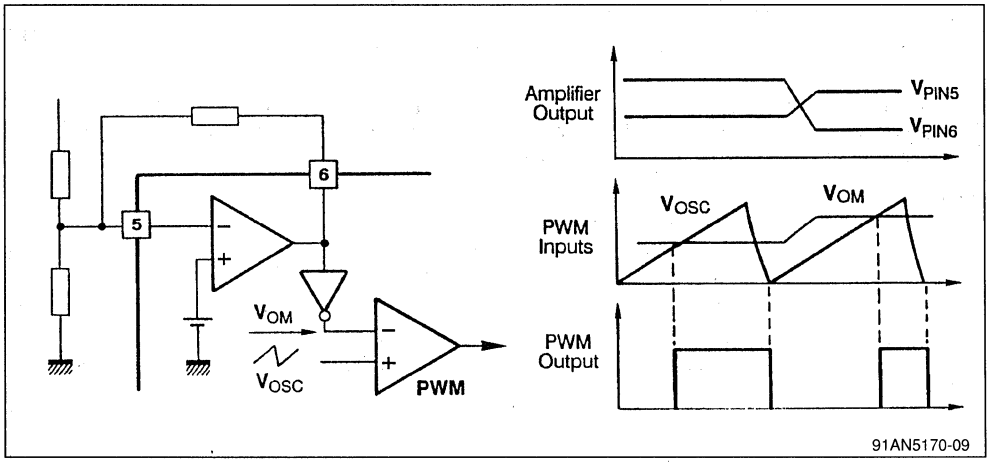
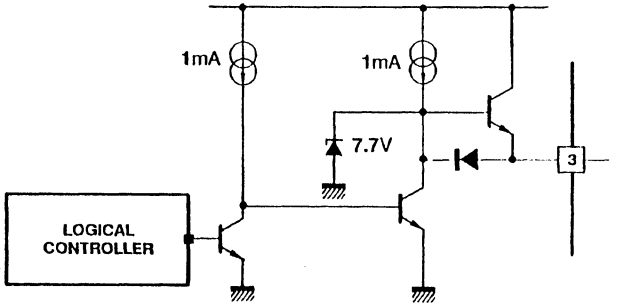


Figure 10



III.5 - Output Stage (see figure 10)

The output stage operates in on/off mode. For a supply voltage higher than 8V, the output signal value is independent of the supply voltage. (Typical value : 7V)

III.6 - V_{CC} Monitoring

V_{CC} Rising : When V_{CC} reaches the value "$V_{CC(START)}$", an internal switch enables the operation of the output stage and the soft-start capacitor begins charging.

The internal logic circuitry becomes operational before V_{CC} has reached the "$V_{CC(START)}$" value.

V_{CC} Falling : When V_{CC} falls below the "$V_{CC(STOP)}$" level, the negative output stage is switched-on, the transistor is turned off and the soft-start capacitor is discharged.

IV - TV POWER SUPPLY APPLICATION BUILT AROUND TEA5170 (Figure 15)

General structure and operational features of this power supply were outlined in section 1.

The details covered below apply to a power supply configuration using the slave "TEA2164" device.

(Refer to TEA2164 data sheet and application note "AN409/0591" for further details).

IV.1 - Main Application Characteristics

Characteristic	Value
Input voltage	170V_{AC} to 270V_{AC}
Output power	20W to 120W
Output power in stand-by mode	1W to 6W
Switching frequency	32kHz
Synchronization on line flyback signal (positive)	

IV.2 - Components External To TEA5170

Component Value Calculation

Also refer to TEA2164 application note "AN-409/0591" for calculation methods applicable to other power supply elements.

The external components determine the following parameters :

- Operating frequency
- $t_{ON(MIN)}$
- Soft-start
- Error amplifier gain

Ideal Values

- Period of operation "T_{OSC}" : 32µs
- $t_{ON(MIN)}$ duration : 1.2µs
- soft-start duration : 20ms
- Error amplifier gain :
  - DC gain G_{DC} = 35
  - AC gain at 1/10 x T_{OSC} : $G_{AC} = G_{DC}/5 = 7$

IV.3 - Free-Running Oscillation Frequency

For efficient use of TEA5170 and TEA2164 synchronization windows, the periods of both devices are determined as folows :

$$T_{OSC(5170)} = \frac{T_{SYNC}}{1.06}$$

$$T_{OSC(2164)} = \frac{T_{OSC(5170)}}{1.223}$$

Where :

- T_{SYNC} : line flyback signal period
- $T_{OSC(5170)}$: TEA5170 free-running period
- $T_{OSC(2164)}$: TEA2164 free-running period

Numerical Application

Period of synchronization signal being

$T_{SYNC} = 32\mu s$:

$$T_{OSC(5170)} = \frac{T_{SYNC}}{1.06} = 30.2\mu s$$

$$T_{OSC(2164)} = \frac{T_{OSC(5170)}}{1.223} = \frac{30.2}{1.223} = 24.7\mu s$$

The TEA5170 free-running period is determined as follows :

$T_{OSC(5170)} = C_t\ (0.5 \times R_t + 1330)$

Where :

$$C_t = \frac{t_{ON(MIN)} - 0.5 \times 10^{-6}}{1330}$$

- $R_t = 105k\Omega$ (1%)
- $C_t = 560$ pF (2%)

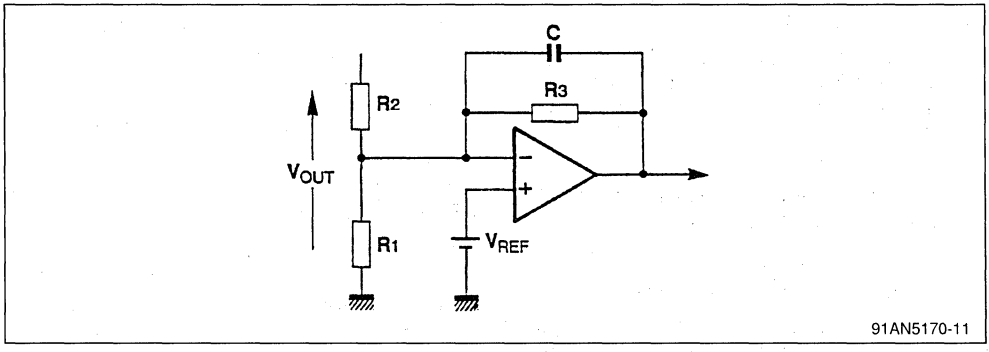
IV.4 - Error Amplifier Compensation

- A high DC gain is required for good accuracy.
- For stability reasons, the AC gain must be attenuated so as to avoid injection of the switching frequency component into the regulation loop.
- DC Gain : $G_{DC} = R3 \times \frac{R2 + R1}{R2 \times R1}$
- AC Gain : $G_{AC} = \frac{R3 \times \frac{1}{j\omega C}}{R3 + \frac{1}{j\omega C}} \times \frac{R2 + R1}{R2 \times R1}$

Assumptions :

- R2 > > R1 since V_{OUT} >10 V_{REF} so the value of R2 does not modify the result of calculation and only R1 and R3 influence may be taken into consideration.
- R1 = 2.2kΩ , R3 = 75kΩ
- With cut-off frequency in AC regulation mode :
- $f_C = \frac{1}{10 \times T_{OSC}} \Rightarrow C = 2.2nF$

Figure 11



IV.5 - Synchronization Signal Matching Stage
(Figure 12)

The synchronization signal is generated from the line flyback.

The pulse amplitude is given by :

$$\frac{V_{PIN8(MAX)}}{V_{SYNC}} = \frac{R}{R + R_P} \text{ With } R_t >> R$$

The pulse time constant is (R+ R_P)C and should be lower than the saw-tooth fall time.

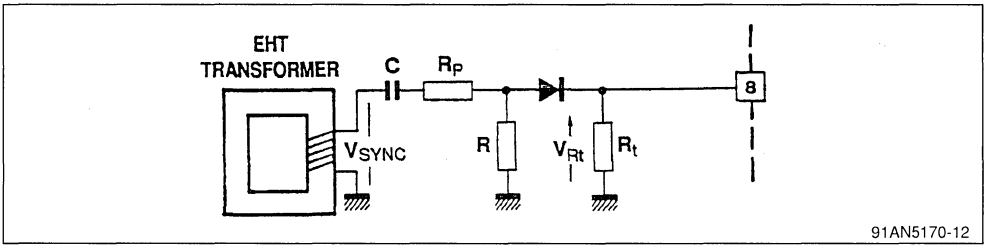
Thus, for a line flyback signal amplitude of 50V :

R = 6.8kΩ , R_P = 75kΩ , C = 150pF

Comment :

Practical and theoretical values may differ slightly since the rise time of the line flyback signal is not generally negligible.

Figure 12



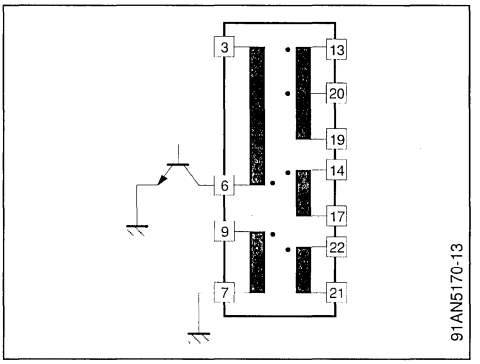
IV.6 - Soft-Start Period Duration

In this application, the duration of soft-start is around 20ms,

With :

- $C_{(S\text{-}START)} = T_{(S\text{-}START)} \times 2 \times 10^{-6} = 47nF$

Figure 13



IV.7 - Transformer Characteristics
(Reference : G4453-02 OREGA)

Winding	Pin	Inductance
n_P	3-6	680 µH
n_{AUX}	7-9	7 µH
n2	19-13	592 µH
n3	19-20	12 µH
n4	14-17	5 µH
n5	22-21	25 µH

IV.8 - Operation

IV.8.1 - Start-Up

The power supply of TEA5170 begins rising gradually upon initial start-up of the primary circuit. When V_{CC} reaches the value $V_{CC(START)}$ = 4V, the oscillator has already begun running and the soft-start capacitor "$C_{(S-START)}$" begins charging. The conduction time is $t_{ON(MIN)}$ and rises gradually.

IV.8.2 - Stand-By

This function is externally activated by grounding the *"stand-by"* input thereby disabling the power supply of TEA5170. (Figure 15).

To return to normal mode of operation, this pin should be left floating.

IV.8.3 - Synchronized Mode

The differentiator at synchronization input will transform the line flyback signal into a rectangular pulse whose time constant is around 1ms.

In this mode of operation, there is a lapse of time between the falling edge of the synchronization signal and the real transistor turn-off (Figure 13).

In TV applications, this time should be less than the line flyback duration so as to avoid the occurrence of on-screen visible disturbances.

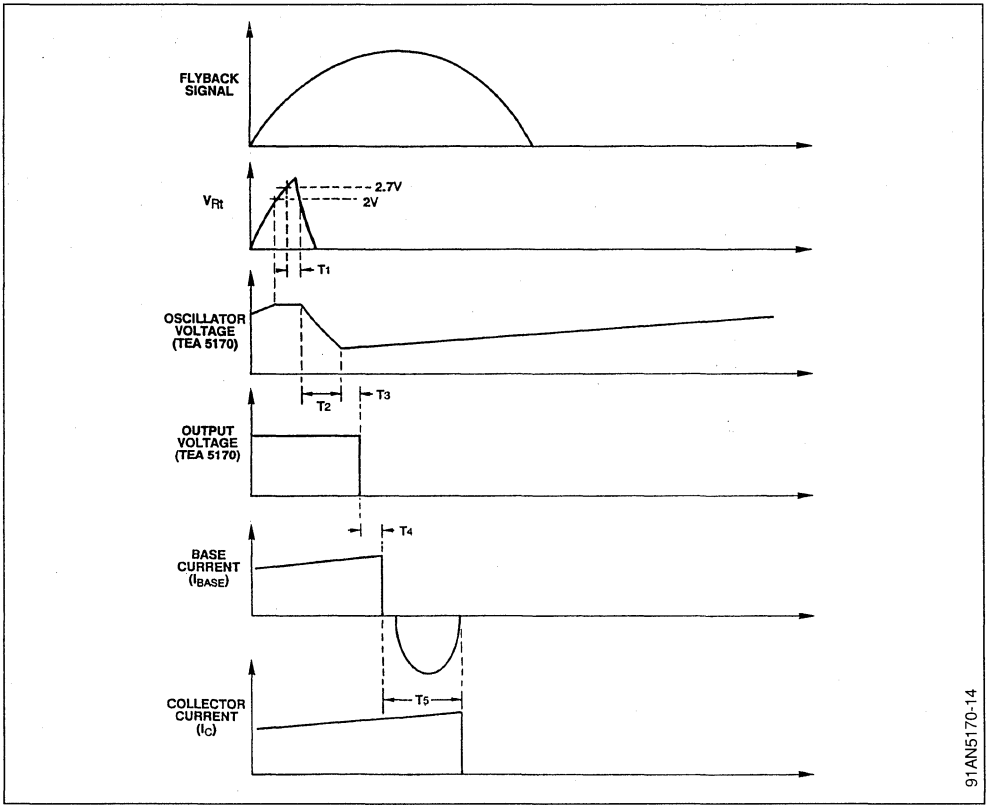
t1 and t3 times are specific to TEA5170 (t1 + t3 = 800ns typ.)

t4 is specific to the primary circuit (= 800ns typ. with TEA2164).

Only t2 = $t_{ON(MIN)}$ and t5 = t_{STG} of the switching transistor can be modified according to individual application requirements.

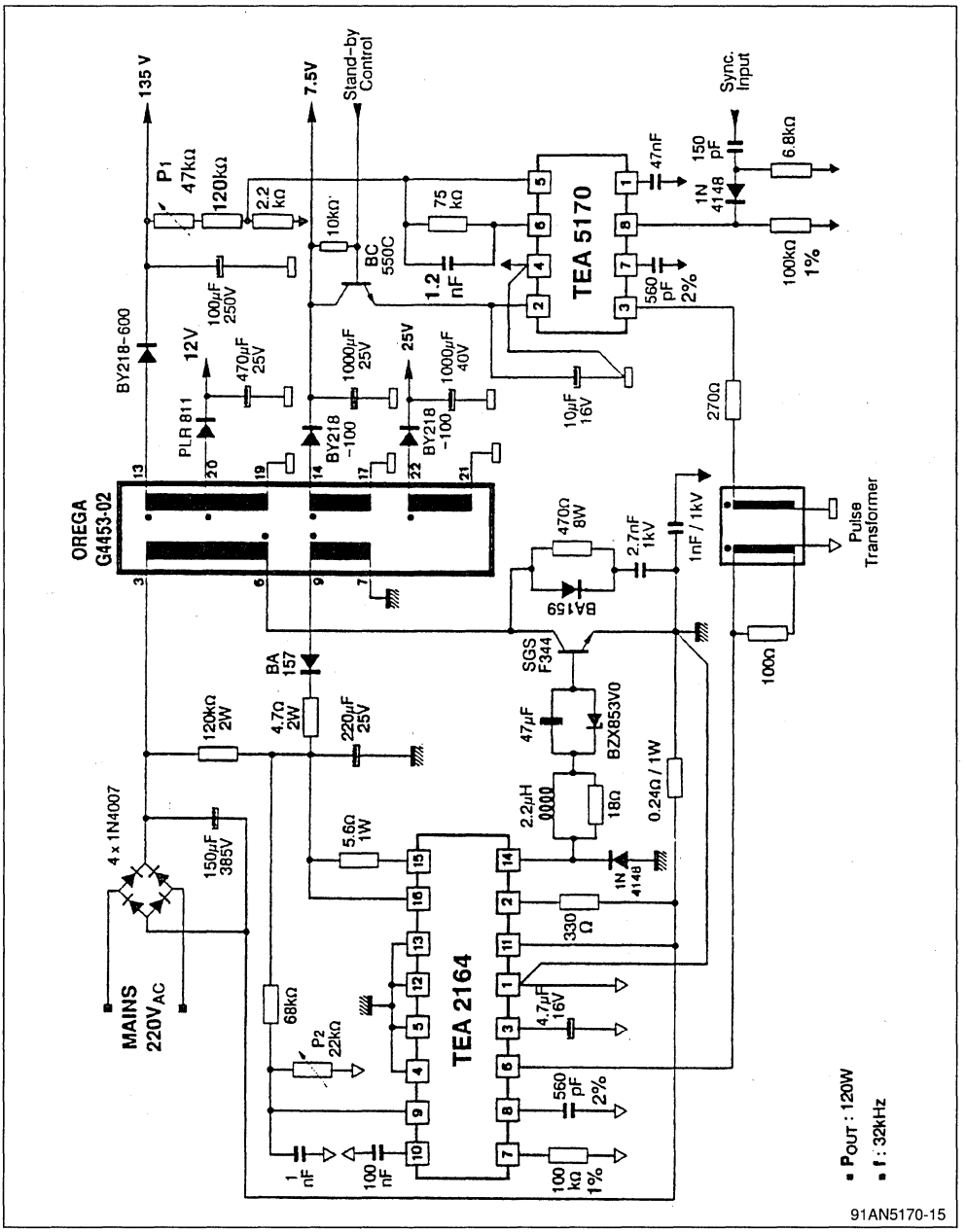
IV.9 - Delay Time In Synchronized Mode

Figure 14



IV.10 - Electrical Diagram

Figure 15



V - DC-DC CONVERTER

(9V ± 40% => 24V , 1.5W) (Figure 16)

This low power converter employs a transformer wound on a low-cost ferrite former.

The configuration is protected against open loads and short-circuits.

Transformer characteristics

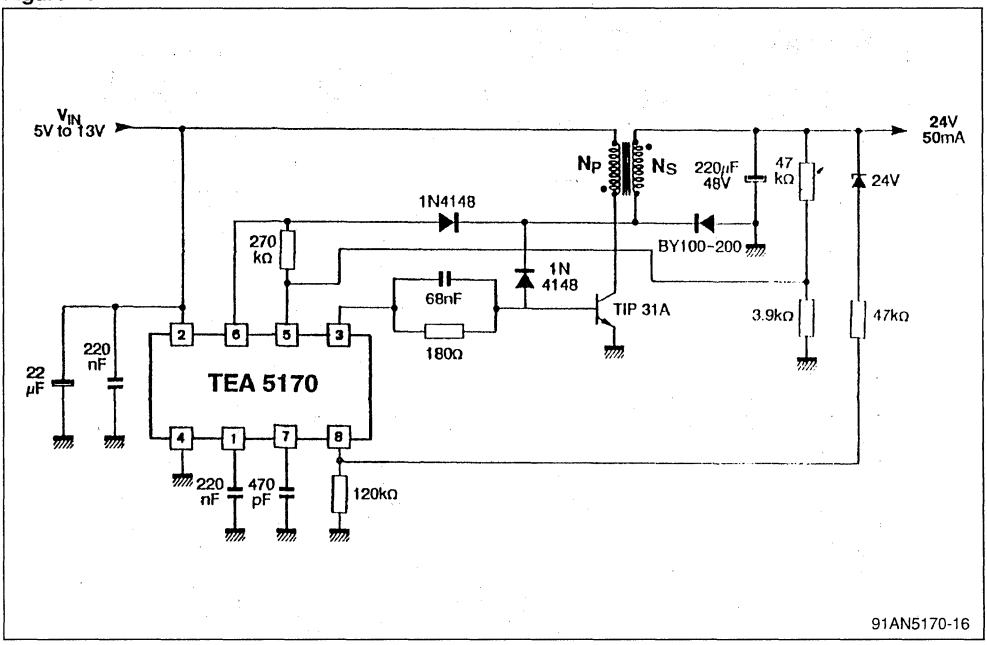
- Primary inductance : 53.5 µH
- Transformation ratio for 24V : $n_S / n_P = 2$

Regulation Characteristics

- Line regulation at 4.9V to 15V : 24V ± 0.22%
- Load regulation for ($0.4P_{MAX}$ - P_{MAX}) : 24V ± 0.12%
- Power range : 0.24W to 1.6W
- Efficiency : 40%

V.1 - Electrical Diagram

Figure 16



V.2 - Operation

- The period of operation is determined by R_t and C_t components.
- Minimum conduction duration : 0.6 µs
- Free-running period : 29 µs
- Soft-start period duration : preset at 100 ms.

V.2.1 - Open-load Protection

In case of low load values, the minimum conduction time $t_{ON(MIN)}$ with respect to the period of operation is too high to maintain the output voltage at its nominal value. The only solution to stabilize the voltage is to increase the period of operation by reducing the charge current of the oscilator capacitor C_t. This is obtained by injecting additional current into resistor R_t as soon as the output voltage V_{OUT} rises.

V.2.2 - Short-circuit Protection

When the current through transistor becomes substantially high, the transistor is saturated and induces a high dI_C/dt . The diode on switching transistor base is then forward biased and begins deviating a portion of the base current. This phenomenon is self amplified and therefore results in rapid transistor turn-off.

V.2.3 - Demagnetization Monitoring

In order to avoid magnetic flux runaway, the transistor should be driven into conduction only once the transformer has been fully demagnetized.
While the transformer is being demagnetized, the secondary-connected rectifier diode is forward biased and thus maintains the error amplifier output at 0 potential. The allowed conduction period is consequently $t_{ON(MIN)}$.

VI - CONCLUSION

The TEA5170 requires a very simple configuration and yet offers excellent regulation quality combined with synchronization possibility for flyback-type converters.

The TEA5170 can be used in converters operating at 16 kHz to over 100 kHz frequency range.

Access to error amplifier and soft-start input are some of the remarkable features offered by this device whose application areas are by no means limited.

The TEA5170 belongs to the family of master controller devices characterized by their outstanding flexibility of use and application performances.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2164
MASTER-SLAVE SMPS FOR TV & VIDEO APPLICATIONS

By : B. D'HALLUIN

SUMMARY

SUMMARY *(continued)*

I - INTRODUCTION

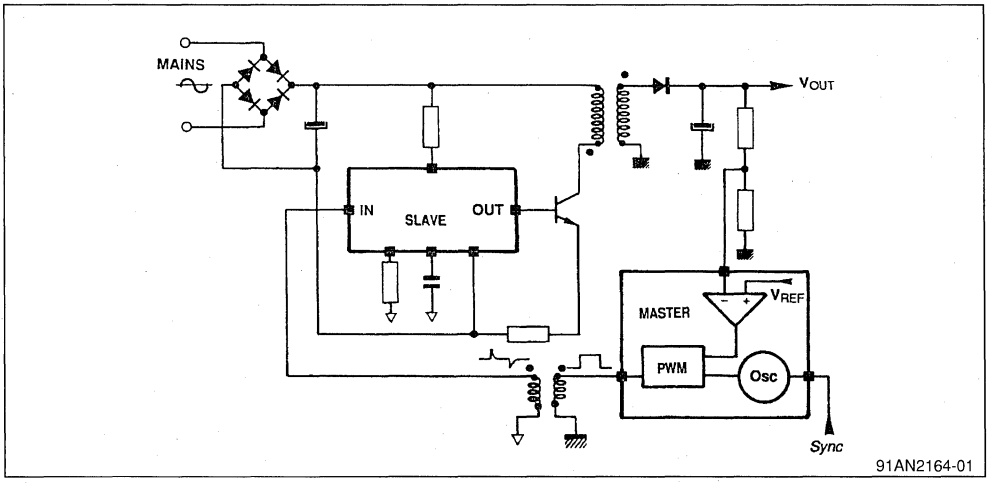
The TEA2164 is a Switching Power Supply Controller circuit designed to operate in Master-Slave structure.
This device is located on the primary side of power supply and requires the addition of other controller device such as TEA2028 or TEA5170 connected to the secondary side.

The main application of this circuit is in switching mode power supplies operating in discontinuous mode flyback configurations used in TV receivers at 60 W to 150 W power ratings.
The device incorporates a "Burst Mode" feature which offers excellent functional efficiency in "Stand-by" mode of operation.

I.1 - Master-slave structure

I.1.1 - Block diagram

Figure 1



I.1.2 - Fundamentals

The "Master" device located on the secondary side of the power supply performs the following functions :

- Output Voltage Control : Monitors the Conduction Period of the "Slave" circuit so as to provide Output Voltage Regulation as a function of Mains and Load variations.
- Switching Frequency Synchronization on Horizontal Scanning Frequency

The "Slave" circuit provides for the following functions :

- Power supply start-up
- Optimized Switching Transistor base drive
- Power supply regulation during stand-by operation
- Protection against
  - Overloads
  - Short-circuits
  - Open-loads
  - Missing control pulses normally delivered by secondary block.

I.1.3 - Principles of regulation

A fraction of the voltage to be regulated is obtained from a voltage divider network and compared to an internal reference voltage. The error voltage delivered by comparator is used to modulate the duration of the output pulse delivered by PWM (Pulse Width Modulation) Controller. The frequency of these pulses is determined by an internal oscillator synchronized on the horizontal scanning of the TV set.

PWM output signal is differentiated and forwarded towards the primary controller via a small low-cost pulse transformer which provides galvanic isolation between primary and secondary sections.

The differentiated positive signal pulse will turn the transistor on while the negative pulse will turn it off.

Conduction period variation will determine the amount of energy stored within the transformer during each cycle so as to maintain a constant output voltage whatever load and mains voltage variations.

I.1.4 - Advantages offered by this architecture

The "Master-slave" architecture offers the following advantages :

- Excellent output voltage regulation
- Main output voltage is not influenced by significant variations of auxiliary voltages (no sound interference within image display, even at audio power levels as high as 2 x 30 W).
- The coupling between transformer primary and secondary windings is no longer a critical requirement for regulation; which allows use of low-cost transformers (such as SMT5 series manufactured by OREGA)
- Synchronization on TV line scanning frequency will suppress any on-screen interference produced by power transistor turn-off, and eliminate the need of additional output voltage filtering components.
- All power supply protection features are implemented on primary side thereby allowing efficient and fast response to :
  - Current limitation
  - Overvoltage protection
  - Persisting overloads
- Other protections can be implemented to limit or disable the duration of regulation pulses issued by PWM, in case of failure detected within any section of the TV set.

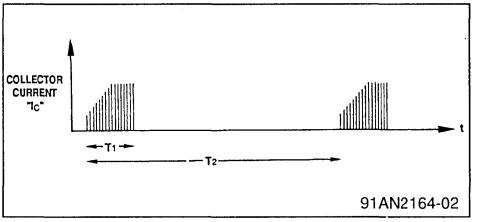
I.2 - Stand-by in burst mode

The secondary power required in stand-by mode is often quite low (1 W to 5 W in majority of cases).

Instead of operating the system at low t_{ON} duration, which is a difficult task with discontinuous mode transformer, the TEA2164 offers a "Burst Mode" to perform the stand-by function.

- T_1 : Burst duration

Figure 2



- T_2 : Burst period (period of VLF oscillator)

The T_1/T_2 ratio is fixed internally.

The TEA2164 allows the switching transistor to conduct only for typically 13% of the internal VLF oscillator period.

A pulse train "T_1" called "Burst" is thus obtained. The repetition period "T_2" can be set externally by capacitor "C_1" connected to pin 10.

In this mode of operation, the power transferred to the secondary windings is very low.

The collector current envelope has been optimized to yield efficient soft start and to minimize the audio

noise generated by switch mode transformer. Also, the free-running frequency "f_{OSC}" is shifted towards 20kHz so as to eliminate all audible noise in stand-by mode.

In this mode, the secondary output voltages are regulated by a feed-back loop on primary side. The TEA2164 will switch from synchronized mode (regulation by master circuit on secondary side) to burst mode (stand-by) as soon as the synchronization pulses, normally delivered by secondary block, are no longer available.

It is therefore obvious that the most efficient solution to implement the burst mode is to cut supply to master which will consequently be unable to deliver any synchronization pulse.

The stand-by function in burst mode offers the following advantages :

- Eliminates the need for auxiliary stand-by power supply and therefore its costly building elements such as stand-by mains transformer, relay or other specific components.
- Good power supply efficiency, thanks to burst mode, allows low mains power consumption in stand-by.

II - THE TEA2164 INTEGRATED CIRCUIT

II.1 - Description

The TEA2164 is cased in a 16-pin DIL package. The 4 center pins (2 on each side) are connected together and used to evacuate the heat.

The device includes the following functional blocks :

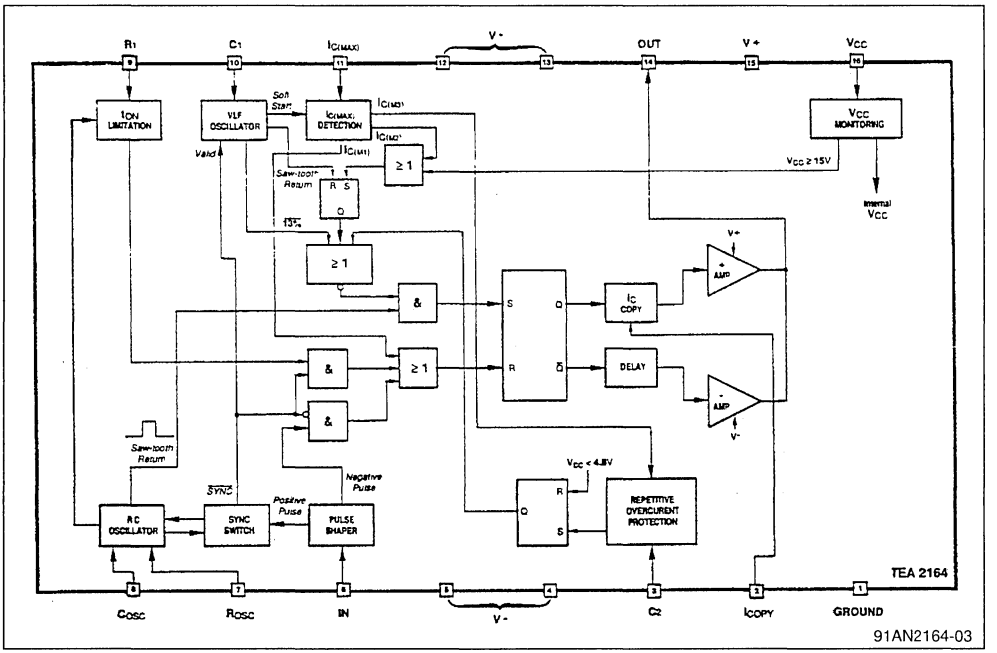
- A free-running oscillator which can be synchronized on the frequency of pulses issued from secondary.
- A Very Low Frequency (VLF) oscillator used for burst mode.
- An input stage to shape positive and negative input pulses.
- An output stage with two complementary amplifiers :
  - one, to provide the positive base current to turn the switching transistor on,
  - the other, to provide the negative base current required to turn the transistor off.

The positive base current is proportional to the collector current.

- A sophisticated protection system featuring :
  - Collector current limitation at 2 threshold levels
  - A device to memorize the occurrence of overloads and short-circuits, and to disable the power supply completely after a pre-determined time constant.
  - V_{CC} monitoring device with 2 thresholds :
    - Upper threshold : for overvoltage protection
    - Lower threshold with hysteresis : for system start-up
- Supply Voltages :
  - one pin for general supply (V_{CC})
  - one pin for power supply of the positive output stage (V^+)
  - four pins for power supply of the negative output stage (V^-)
    (according to application type, these pins can be grounded)
  - one pin for ground connection

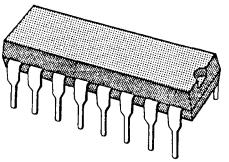
II.2 - TEA2164 Simplified block diagram

Figure 3



II.3 - Pin configuration

1	Ground
2	I_{COPY}
3	C_2
4	V^-
5	V^-
6	Input
7	R_{OSC}
8	C_{OSC}
9	R_1
10	C_1
11	I_{CMAX}
12	V^-
13	V^-
14	Output
15	V^+
16	V_{CC}



Batwing DIP16
(plastic package)

II.4 - Operating modes

II.4.1 - General description

The TEA2164 can operate in two distinct modes :

- "Normal" (or synchronized) mode :
  Synchronization and regulation by secondary controller circuit.
- "Burst" mode :
  In this mode, the TEA2164 operates as a stand-alone device.
  This mode is used upon start-up and in stand-by mode.

Two additional modes are also available :

- Long interval safety mode : the device is fully turned-off although it is correctly supplied (pin 3 capacitor has stored the occurrence of repetitive overcurrent)
- Start-up mode : the device is in low-consumption mode, its V_{CC} has not yet reached the $V_{CC(START)}$ threshold.

The normal start-up sequence is :

- Start-up Mode
- Burst Mode
- Synchronized Mode

II.4.2 - Synchronized mode

In synchronized mode, control pulses delivered by secondary block are differentiated and then applied to pin 6 input.

The positive pulse will synchronize the internal oscillator by discharging the "C_{OSC}" capacitor, which will generate a constant width pulse called "START" signal to be applied to positive stage output amplifier.

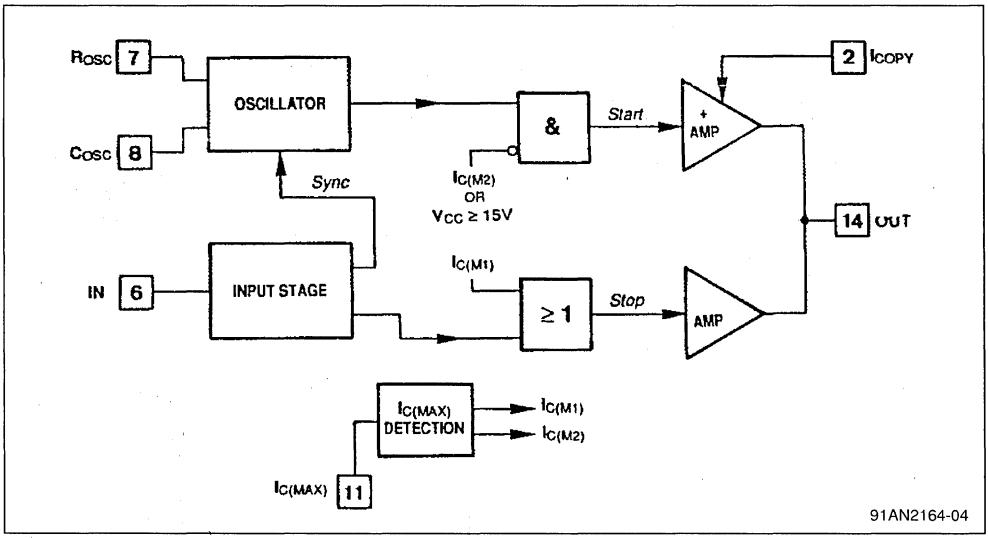
Similarly, the negative input pulse generates a "STOP" pulse which is applied to negative stage amplifier whose output is used to turn-off the switching transistor.

The "START" signal is disabled under following conditions :

- voltage applied to V_{CC} terminal is higher than +15V
- current protection device has detects a collector current higher than "$I_{C(M2)}$".

If the current reaches "$I_{C(M1)}$" threshold, the current limitation device will generate the "STOP" pulse.

Figure 4



II.4.3 - Burst mode

If no control pulses are present at device input terminal, the TEA2164 will operate as stand alone in burst mode.

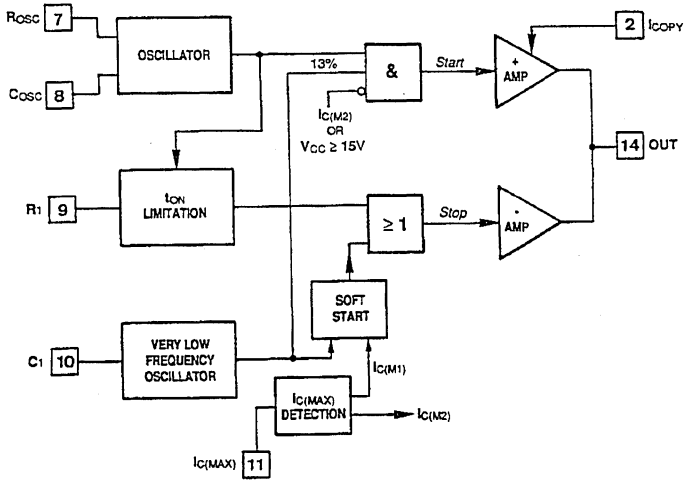
The switching frequency is given by the internal oscillator whose value depends on external components "R_{OSC}" (pin 7) and "C_{OSC}" (pin 8).

The "START" signal is generated by the oscillator and is used to turn the switching transistor on.

Transistor turn-off is performed by "$I_{C(M1)}$" current limitation through soft-start block or by "$t_{ON(MAX)}$" value set by resistor "R_1" connected to pin 9 (or voltage applied to pin 9).

The VLF oscillator will enable the "START" signal for 13% of its periode duration.

Figure 5



III - APPLICATION EXAMPLE
(120 W - Discontinuous mode flyback power supply with stand-by in burst mode)

III.1 - Characteristics & application diagram

III.1.1 - Characteristics

- Discontinuous mode flyback SMPS
- Standby function using the burst mode of TEA2164
- Switching frequency :
  - Normal mode : 15625Hz (synchronized on horizontal deflection frequency)
  - Stand-by mode : 19kHz
- Nominal mains voltage : 220V_{AC} (50Hz or 60Hz)
- Mains voltage range : 170V_{AC} to 270V_{AC}
- Nominal output power : 120W
- Mains power consumption :
  - Normal mode : 150W max
  - Stand-by mode : 5W (with 3W at secondary side)
- Efficiency :
  - Normal mode : 85% (under nominal conditions)
  - Stand-by mode : 60%
- Regulation performance at high voltage output :
  - better than 0.5% versus mains variations of 170V_{AC} to 270V_{AC}
  - better than 0.5% versus load variations of 35W to 120W
- Overload and short-circuit protection with complete power supply shut-down after a pre-determined time constant
- Open-load protection by output overvoltage detection

III.1.2 - Application diagram

The first diagram illustrates the primary block built around TEA2164.

The system is set into stand-by mode of operation by the switch connected to +15V supply.

Regulation pulses can be generated by a PWM device such as TEA5170 or delivered by a deflection circuit such as TEA2028 or TEA2029 which includes on-chip power supply regulation.

The second diagram depicts the full application diagram for a complete TV set power supply and scanning built around TEA2164 and TEA2029.

A microprocessor will introduce 100ms delay interval for the system to start-up in stand-by and then to switch into normal mode (synchronized and regulated by TEA2029).

Figure 6 : TEA2164 typical application

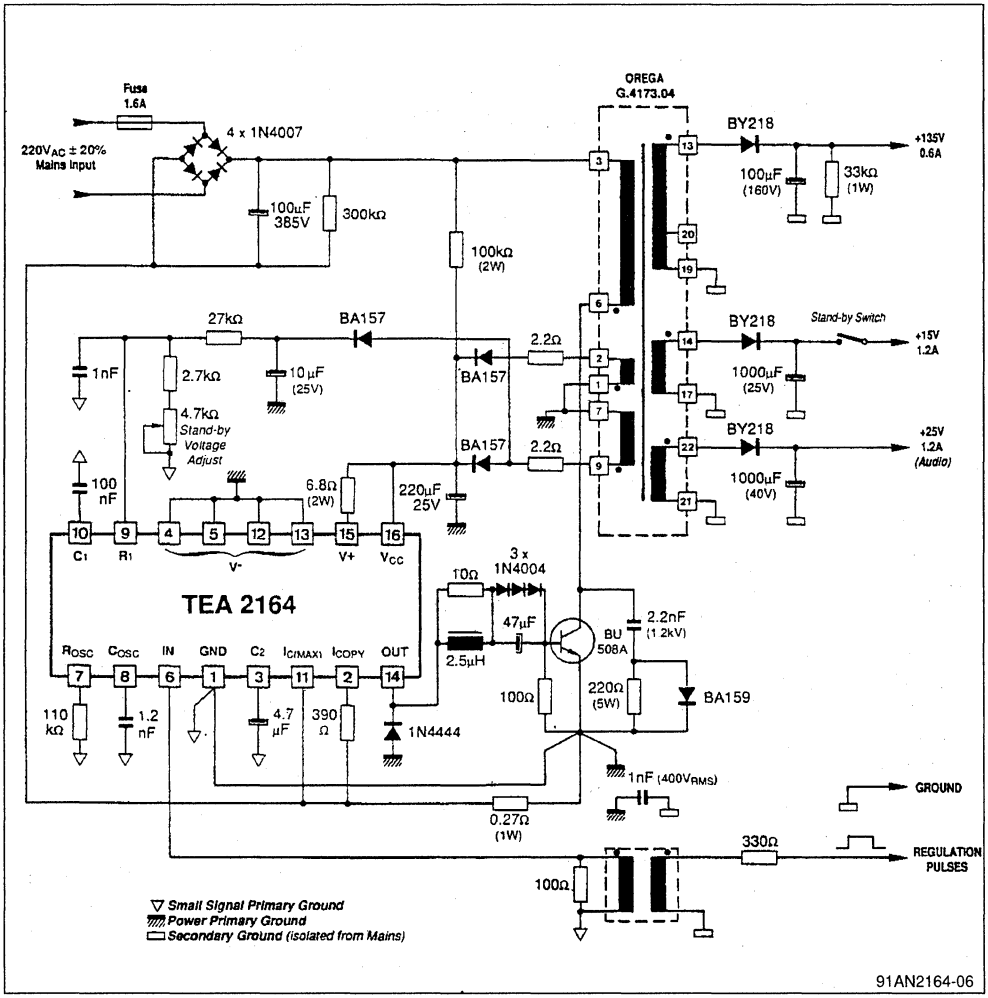
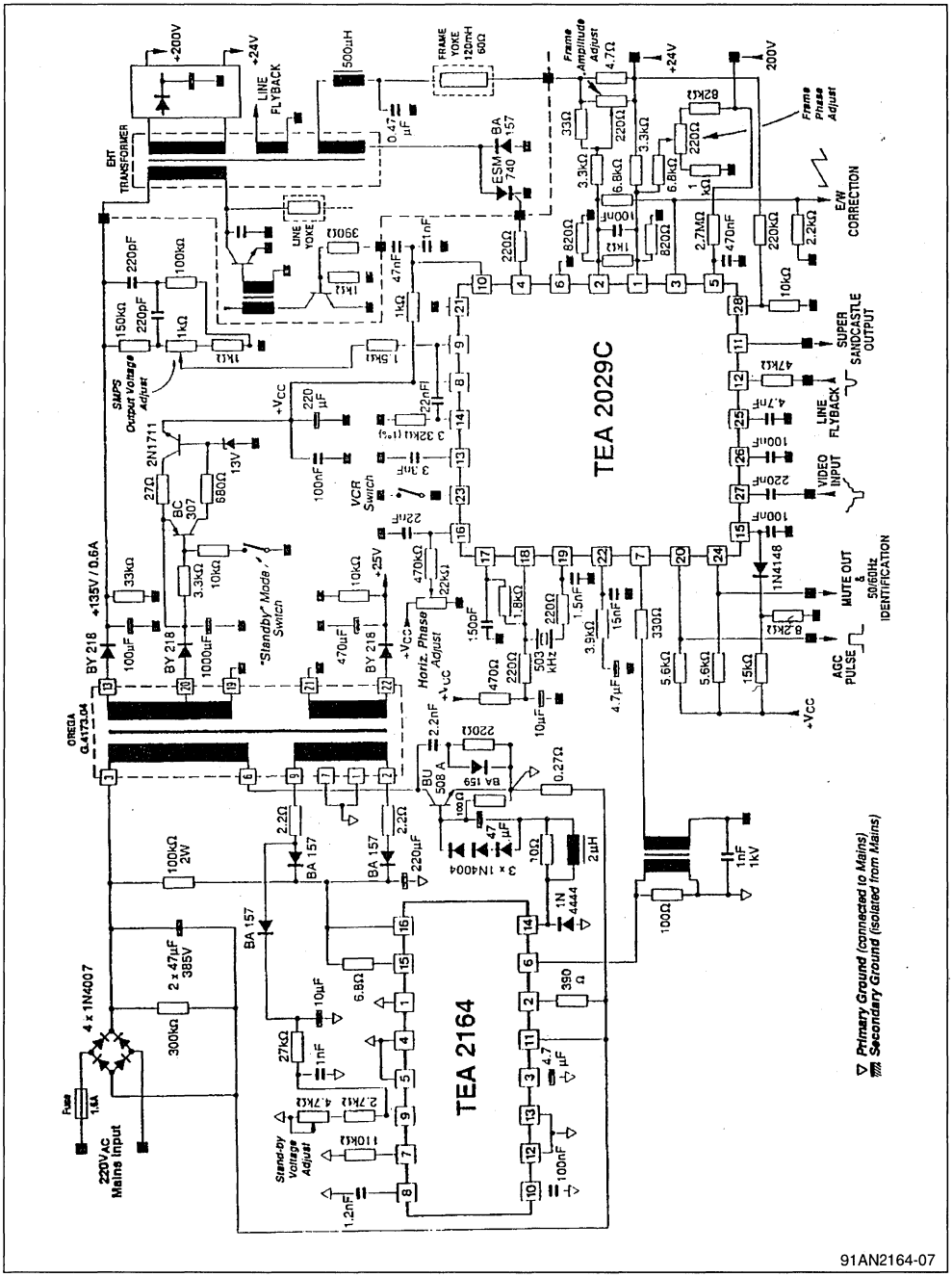


Figure 7 : SMPS & deflection complete application diagram

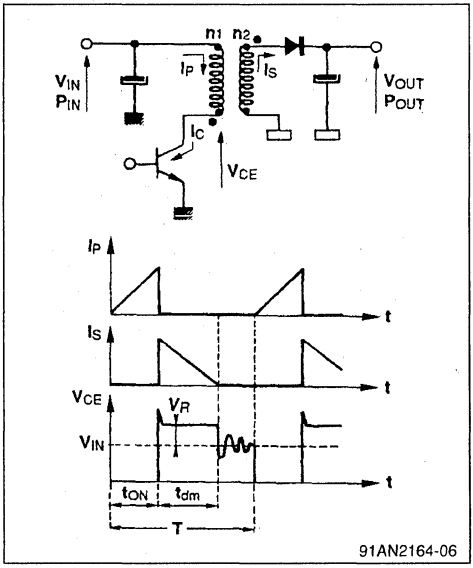


III.2 - Transformer calculation

The power supply must meet the following specification requirements :

- Mains voltage range : 170V_{AC} to 270V_{AC} (50Hz or 60Hz)
  i.e. 200V_{DC} to 380V_{DC} taking into account the supply ripple
- Output power : 10W to 120W max
  i.e. 150W at input
- Switching frequency : 15625Hz
- Main output voltage : +135V

Figure 8



The transformer primary inductance "L_P" and transformation ratio "n2/n1" are to be calculated while taking into consideration limits related to conduction time "t_{ON}" and switching transistor currents and voltages (I_C and V_{CE}).

Following conventional expressions are employed :

$$P_{IN} \approx \frac{L_P \times I_P^2}{2T} \quad (1)$$

$$I_P = \frac{V_{IN} \times t_{ON}}{L_P} \quad (2)$$

$$t_{dm} = \frac{n2}{n1} \times \frac{V_{IN} \times t_{ON}}{V_{OUT}} \quad (3)$$

combining (1) and (2)

$$t_{ON} = \frac{1}{V_{IN}} \times \sqrt{2P_{IN} \times T \times L_P} \quad (4)$$

combining (3) and (4)

$$t_{dm} = \frac{n2}{n1} \times \frac{1}{V_{OUT}} \sqrt{2P_{IN} \times T \times L_P} \quad (5)$$

First limit : The system should always operate in discontinuous mode

$$\text{therefore : } t_{ON(MAX)} + t_{dm(MAX)} \leq T \quad (6)$$

The worst case is specified with $P_{IN(MAX)}$ and $V_{IN(MIN)}$:

$$\left(\frac{1}{V_{IN(MIN)}} + \frac{\frac{n2}{n1}}{V_{OUT}}\right)\sqrt{L_p} \leq \sqrt{\frac{T}{2P_{IN(MAX)}}} \quad (7)$$

Second limit : Maximum voltage across the switching transistor :

$$V_{CE(MAX)} = V_{IN(MAX)} + V_R \quad (8)$$

where : $V_R = V_{OUT} \times \frac{n1}{n2}$

Third limit : Maximum current through the switching transistor :

$$I_{C(MAX)} = \sqrt{\frac{2P_{IN(MAX)}}{L_P} \times T} \quad (9)$$

To minimize the voltage across the power switch, we shall select a reflected voltage of V_R = 150V.

Therefore :

$$\frac{n2}{n1} = \frac{135V}{50V} = 0,9$$

- In order to take full advantage of the transformer ferrite core, one shall select the extreme limit of demagnetization :

therefore :

$t_{ON(MAX)} + t_{dm(MAX)} = T$

$$L_p = \frac{T}{2P_{IN(MAX)}} \times \left(\frac{V_{IN(MIN)} \times V_{OUT}}{V_{OUT} + \frac{n2}{n1} V_{IN(MIN)}} \right)^2 \quad (10)$$

$$L_P = \frac{64 \times 10^{-6}}{2 \times 150} \times \left(\frac{200 \times 135}{135 + 0.9 \times 200} \right)^2$$

$L_P = 1.55mH$

Characteristics of the ferrite core used in this case will require 80 primary and 72 secondary turns.

TRANSFORMER SPECIFICATIONS

- Reference : OREGA - SMT5 - G.4173-04
- Mechanical Data :
  - Ferrite : B50
  - 2 cores : 53 x 18 x 18 (THOMSON-LCC)
  - Airgap : 1.7 mm
- Electrical Data :

	Pin Number	Number of Turns	Wire Size (mm)	Inductance (µH)
Primary	3-6	80	0.45	1550
Forward	2-1	3	0.45	3
Flyback	7-9	7	0.45	14.5
Secondary				
+ 135V	19-13	72	0.45	1240
+ 15V	17-14	9	2 x 0.45	22
+ 25V	21-22	14	2 x 0.45	52

Using this transformer :

- maximum voltage across the switching transistor :

$$V_{CE(MAX)} = V_{IN(MAX)} + V_R$$

$V_{CE(MAX)} = 380 + 150 = 530V$

- maximum current :

$$I_{C(MAX)} = \sqrt{\frac{2P_{IN(MAX)}}{L_P}} \times T$$

$$I_{C(MAX)} = \sqrt{\frac{2 \times 150 \times 64 \times 10^{-6}}{1.55 \times 10^{-3}}} = 3.5A$$

- Maximum conduction time at $P_{IN(MAX)}$:

$$t_{ON(MAX)} = \frac{1}{V_{IN(MIN)}} \sqrt{2 \times P_{IN(MAX)} \times T \times L_P}$$

$$t_{ON(MAX)} = \frac{1}{200} \sqrt{2 \times 150 \times 64 \times 10^{-6} \times 1.55 \times 10^{-3}}$$

$t_{ON(MAX)} = 27.3\mu s$

- Minimum conduction time at $P_{IN(MIN)}$:

$$t_{ON(MIN)} = \frac{1}{V_{IN(MAX)}} \sqrt{2 \times P_{IN(MIN)} \times T \times L_P}$$

$$t_{ON(MIN)} = \frac{1}{380} \sqrt{2 \times 12.5 \times 64 \times 10^{-6} \times 1.55 \times 10^{-3}}$$

$t_{ON(MIN)} = 4.1\mu s$

Comment :

When using high value secondary filtering capacitors or if the switching transistor storage time is too long, the system start-up at high mains voltages may be difficult.

In fact, upon start-up, the secondary filtering capacitors are discharged which will result in very long demagnetization time. According to both, transformer characteristics and minimum conduction time, the transformer is magnetized and the peak primary current begins rising (the current does not any longer begin rising from zero).

In worst case, the current can reach the threshold level "$I_{C(M2)}$" which will consequently prevent the power supply start-up.

Two solutions are available :

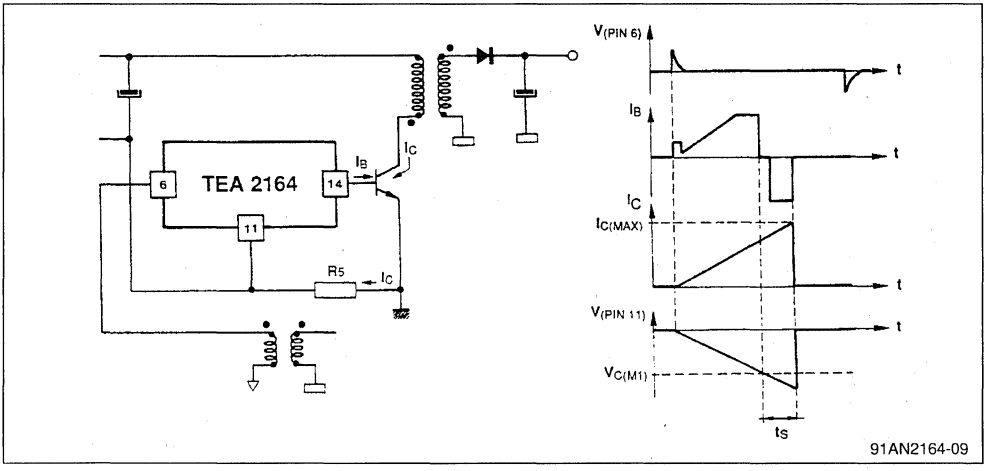
- Reduce the number of secondary turns which will decrease the demagnetization time (but also increase the switching transistor reflected voltage)
- Reduce the primary inductance while keeping the transformation ratio constant (which will also increase the RMS and peak current values)

Under all circumstances, an efficient transistor base drive combined with a not too long storage time (3.5µs to 4µs) are required.

III.3 - Switching transistor & its base drive

III.3.1 - Current limit calculation

Figure 9



The "R_S" resistor sets the switching transistor collector current limitation value. Power supply reliability is directly dependent on the value of this resistor, which is calculated as a function of the maximum power required from the secondary winding.

Lets set the secondary power limit at 150W value :

$$P_{IN} = \frac{P_{OUT}}{n} \Rightarrow P_{IN} = 175W$$

(with efficiency n = 0.85)

$$I_{C(MAX)} = \sqrt{\frac{2P_{IN(MAX)} \times T}{L_P}}$$

$$I_{C(MAX)} = \sqrt{\frac{2 \times 175 \times 64 \times 10^{-6}}{1.55 \times 10^{-3}}} = 3.8A$$

The storage time at this current value is approximately 4µs (with BU508A).

The collector current slope at nominal mains voltage is 0.2A/µs .

The current limitation threshold level must therefore be fixed at 3A.

The "$I_{C(M1)}$" voltage threshold is typically 0.84V :

$$\text{therefore : } R_s = \frac{0.84}{3} = 0.28\Omega$$

In practice, the selected value is $R_S = 0.27\Omega$

At minimum mains voltage level, the slope is smaller and the maximum current therefore becomes :

$$I_{C(MAX)} = \frac{0.84}{0.27} + \frac{200}{1.55 \times 10^{-3}} \times 4 \times 10^{-6} = 3.6A$$

At maximum mains voltage level, the slope is sharper and the maximum current therefore becomes :

$$I_{C(MAX)} = \frac{0.84}{0.27} + \frac{380}{1.55 \times 10^{-3}} \times 4 \times 10^{-6} = 4.1A$$

III.3.2 - Switching transistor

It was demonstrated that under normal operating conditions, the maximum collector current value is around 4.1A while the maximum collector voltage is approximately 530V.

Factors such as the overvoltage produced at the time of transistor turn-off, transformer leakage inductance and peak currents generated in the event of short-circuits, must be also taken into account.

At the time of transistor turn-off and under worst case conditions (maximum mains voltage, significant overload), the "V_{CE}" voltage across the transistor can reach 1000V.

Therefore, a transistor with $V_{CES} \geq 1200V$ must be selected.

In case of short-circuit, transformer is magnetized and the collector current value will reach 5A (with 0.27Ω measurement resistor and 1.35V typ. $V_{C(M2)}$ threshold).

Therefore, a transistor with $I_{C(MAX)} \geq 7A$ must be selected.

The BU508A and equivalents are perfectly suitable.

III.3.3 - Switching aid (snubber) network

The "Snubber" network is built using a combination of "R , C , D" components to limit the dV/dt slope and to reduce the collector current rise up at the time of transistor turn-off.

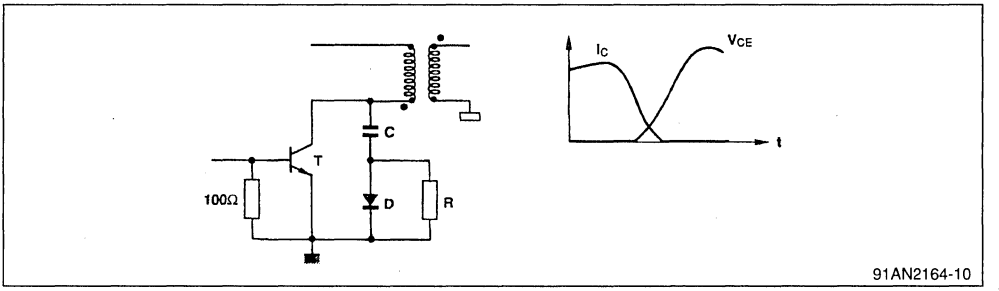
Switching losses at turn-off which are proportional to "V x I" product are thus minimized.

- C = 2.2nF
- R = 220Ω
- D : BA159
- T : BU508A

Whatever load and input voltage conditions, it must be ensured that the system will operate permanently within the safe operating area of the transistor.

A 100Ω resistor connected between transistor base and emitter terminals will improve the voltage behaviour.

Figure 10

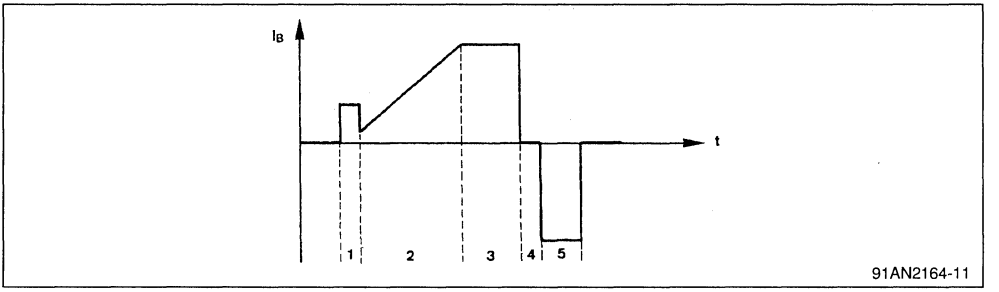


III.3.4 - Base drive

A bipolar switching transistor requires a positive base current to enter into saturation while a negative base current is necessary to turn it off.

The shape of base current waveform is illustrated in the following Figure.

Figure 11



1 - Constant amplitude pulse to turn the transistor on (duration depends on oscillator saw-tooth return)

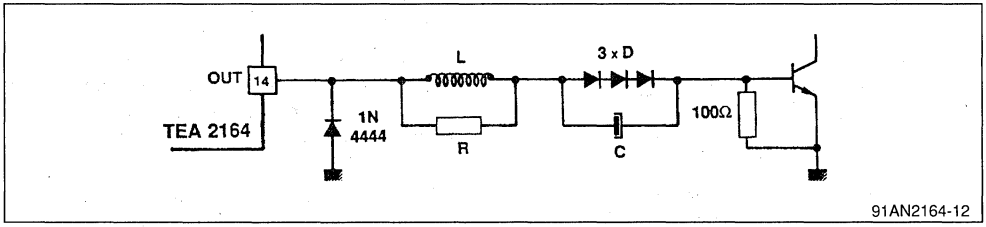
2 - Base current proportional to the collector current (I_{COPY} function on pin 2)

3 - Saturated base current to limit the circuit power dissipation (function implemented through the resistor in series with pin 15)

4 - On-chip delay interval of "0.7µs" to prevent simultaneous conduction of positive and negative stages

5 - Negative base current to remove the charge stored within base (storage time - duration of which depends on type of switching transistor)

Figure 12



- L = 2.5µH
- R = 10Ω
- C = 47µF
- D : 1N4001

The base drive circuit is a "capacitive coupled" device. There is therefore no need to apply a negative voltage "V -" to pins 4, 5, 12 and 13 which will be grounded. P.C.Board tracks connected to these pins must be wide enough to allow efficient evacuation of the power dissipated by device.

The positive base current goes through 3 diodes connected in series. Capacitor connected across these diodes will be charged to a value equal to 3 times forward diode voltage drop. This voltage is sufficient to turn the transistor off.

This capacitor must be selected to withstand the effective current through it, which is mainly the negative turn-off current.

The inductor in series with base, limits the dIB/dt slope and thus the base current, at the time of transistor turn-off. The inductance value must be adjusted to yield efficient turn-off while the negative current delivered by TEA2164 should not exceed -1.7A . The 10Ω resistor connected across this inductor helps the damping of base current oscillations at the beginning of transistor conduction.

Comment :

In order to avoid all problems at TEA2164 output stage, it is recommended to connect a 1N4444 diode between the output terminal (pin14) and the ground, as illustrated in Figure 12 above.

In case of capacitive drive and if a negative voltage appears across output terminal (due to inductor L), this diode will deviate the current towards ground thereby preventing reverse bias of the negative output stage.

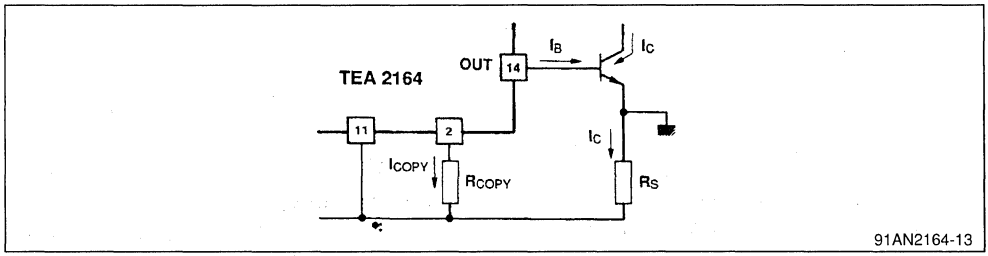
III.3.5 - R_{COPY} Resistor Calculation

This input is used to set the switching transistor forced gain, that is, to deliver the base current necessary for a required collector current.

Input pin 2 can be considered as a virtual ground terminal and therefore :

$R_S \times I_C = R_{COPY} \times I_{COPY}$

Figure 13



Also, the current gain between input (pin 2) and the output (pin 14) is :

$1000 \Rightarrow I_B = 1000 \times I_{COPY}$

The forced gain is therefore :

$$\frac{I_C}{I_B} = \frac{R_{COPY}}{R_S} \times \frac{1}{1000}$$

A forced gain of 2.25 (BU508A) with $R_S = 0.27\Omega$ will yield : $R_{COPY} = 600\Omega$

In practice, one would select the optimal value by observing the dynamic aspect of the saturation voltage on an oscilloscope. This is why $R_{COPY} = 390\Omega$ is selected with BU508A.

III.3.6 - Calculating the value of resistor connected to v+

In order to prevent high current flow through the integrated circuit and also to limit the power dissipation, the output stage is operated in saturated mode in high positive output currents.

The maximum recommended positive base current is 1.2A.

Selected maximum power supply voltage is +12V. Lets calculate the resistor value required to yield a maximum current of +1A.

The voltage drop across three diodes connected in series is typically 0.9V x 3 = 2.7V at 1A.

The base-emitter saturation voltage of BU508A is around 1V. The TEA2164 output stage voltage drop is approximately 1.4V.

Therefore :

$$R_{V+} = \frac{12V - 1V - (3 \times 0.9V) - 1.4V}{1A} = 6.9\Omega$$

Preferred value $R_{V+} = 6.8\Omega$ is selected.

Comment :

- It is obvious that the maximum I_{B+} value is directly dependent on the power supply voltage. Therefore, V_{CC} variations as a function of mains voltage, through the forward self-supply winding, must be taken into consideration.
- All calculated values must be optimized on the prototype board by taking into account all operating conditions of the switching transitor to be used.

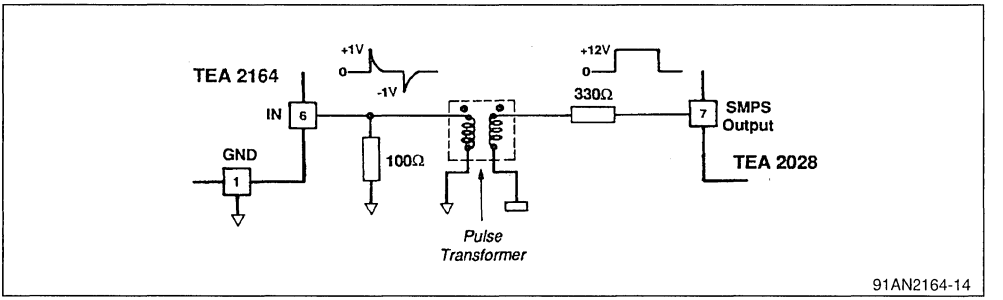
III.4 - Input pulses & oscillator

III.4.1 - Input pulses (pin 6)

The regulation PWM and sync pulses issued by the controller circuit on secondary side are sent to the primary side through a pulse transformer that ensures galvanic isolation between primary and secondary sections. The PWM pulse is differentiated by the pulse transformer.

The input signal (pin 6 of TEA2164) frequency must

Figure 14



fall within the sync window :

$0.65\ f_{OSC} < f_{SYNC} < f_{OSC}$

The positive drive pulse will turn the transistor on while the negative pulse will turn it off. Prior to transistor turn-off, the positive base current is interrupted and then after a constant time interval, the negative base current is applied to turn the transistor off.

For appropriate system operation, the amplitude of pulses applied to input pin 6 must fall within ± 0.5V to ± 1V range.

The pulse transformer can be built by 2 few turn windings wound on a tore or ferrite rod.

III.4.2 - Oscillator (R_{OSC} , C_{OSC} - pin 7 and pin 8)

The free-running frequency is given by :

$$f_{OSC} = \frac{1}{0.4 \times R_{OSC} \times C_{OSC} + 470 \times C_{OSC}}$$

Choice of f_{OSC} must take into account the following constraints :

- f_{OSC} must fall within the sync range :
  $0.65 \times f_{OSC} < f_{SYNC} < f_{OSC}$
- the free-running frequency f_{OSC} must not fall inside audible frequency range in stand-by mode :
  $f_{OSC} \geq 20kHz$

The sync frequency value used in TV applications is 15.7kHz.

The free-running frequency "f_{OSC}" value is selected to be 19kHz so as to fall at the center of sync frequency range. This frequency is close to 20kHz and is therefore not audible.

The value of "C_{OSC}" capacitor determines the oscillator saw-tooth discharge time. This time has a direct influence on "$t_{ON(MIN)}$" used by TEA2164 and therefore should not be too long so as to allow a

low "$t_{on(min)}$".
We shall select C_{OSC} = 1.2nF
The corresponding value of R_{OSC} is calculated as follows :

$$R_{OSC} = \frac{1}{0.4 \times 19 \times 10^3 \times 1.2 \times 10^{-9}} - \frac{470}{0.4} = 108k\Omega$$

Selected value is : R_{OSC} = 110kΩ
The tolerance of these components is calculated as a function of maximum admissible free-running frequency dispersion while also taking into account the minimum and maximum limits of the horizontal scanning frequency.

III.5 - Stand-by

The system will enter into stand-by mode by simply disconnecting the power supply to the secondary-connected PWM regulation device (TEA5170 or TEA2028). In the absence of control pulses normally delivered by the secondary block, the TEA2164 will switch to "burst" mode in which case, the power transfer falls to a low value.

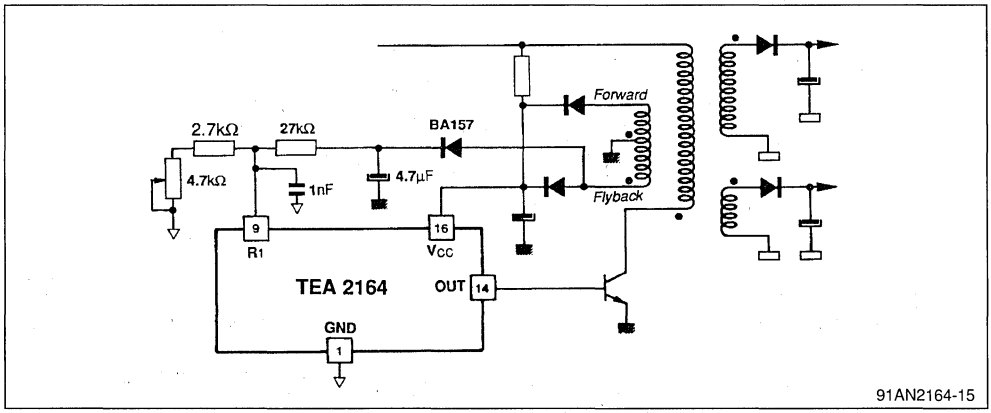
III.5.1 - Very low frequency oscillator

The period of this VLF Oscillator is determined by capacitor "C_1" connected to pin 10.
For C_1 = 100nF, the VLF oscillator period is approximately 30ms. The typical burst duration is therefore 3.9ms - which is 13% of the VLF oscillator period.
The ripple ratio of secondary output voltages in stand-by mode depends on VLF oscillator period and hence on the value of capacitor C1.

III.5.2 - Regulation in stand-by mode

A feed-back loop connected to pin 9 is used to modify the maximum conduction period in burst mode and to allow the regulation of secondary output voltages in stand-by.
The feed-back information is delivered by the self-supply flyback winding of TEA2164. This signal, once rectified and filtered, is an image of secondary voltages. This voltage is applied to an adjustable

Figure 15



divider bridge and then to pin 9 which is used for output voltage adjustment in stand-by operation. It is recommended to choose the voltage values in stand-by slightly lower than nominal values used under normal operating conditions. A 1nF capacitor has been added to pin 9 which will improve the filtering of the regulation voltage.

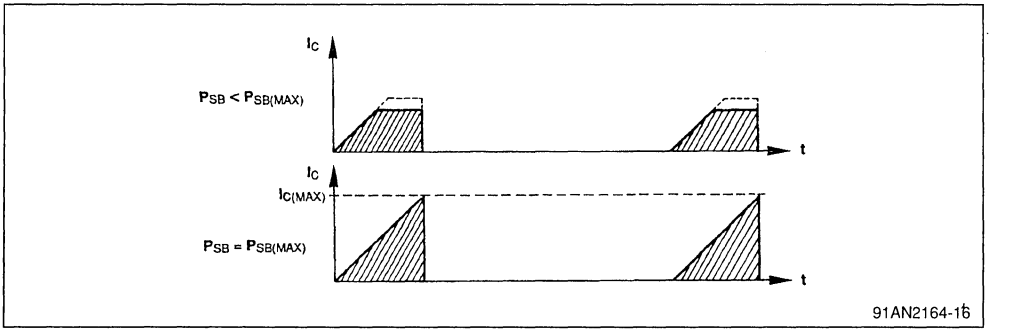
III.5.3 - Maximum power in stand-by operation

The collector current envelope shape varies as a function of the secondary power consumption in stand-by.

It follows that the power which may be tranferred to the secondary winding in stand-by is therefore limited.

The maximum power in stand-by can be estimated as follows :

Figure 16



$$P_{SB(MAX)} \approx \frac{P_{MAX}}{3} \times 0.13 \times \frac{f_{SB}}{f_{SYNC}}$$

$$\Rightarrow P_{(SBMAX)} \approx \frac{150}{3} \times 0.13 \times \frac{19 \times 10^3}{15.7 \times 10^3} = 8W$$

Comment :

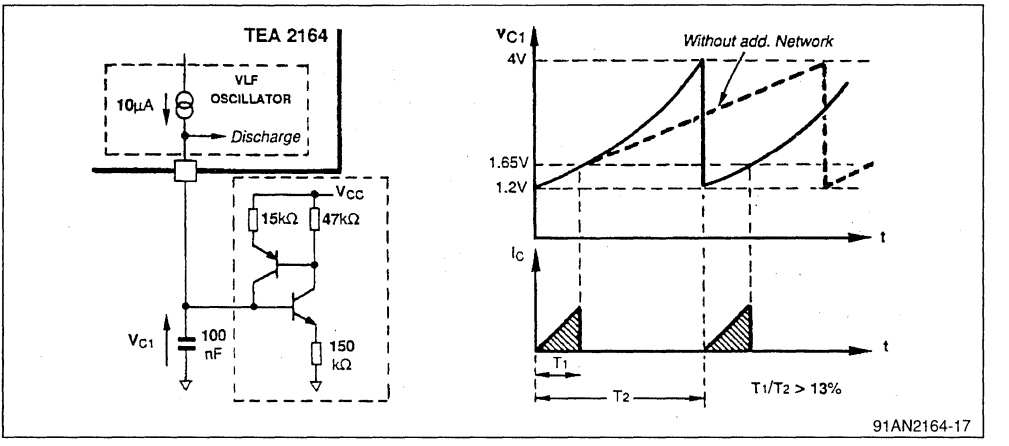
- at $P_{SB} = P_{SB(MAX)}$, C_3 capacitor (pin3) is slowly charged and the voltage on pin 3 will reach the protection threshold value (3V typ.) and the SMPS is shut down.

III.5.4 - Booster circuit for higher stand-by output power

When higher stand-by output power is required, it is possible to add a network on pin 10, which modifies the shape of the VLF oscillator saw-tooth and increase the T1/T2 ratio.

The burst duration "T1" is not modified, only the VLF oscillator period "T2" is shorter, which will increase the available stand-by output power.

Figure 17



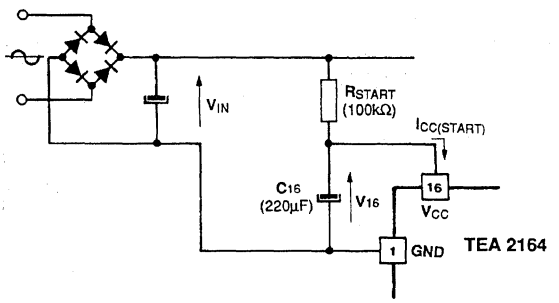
III.6 - Start-up

III.6.1 - Start-up resistor

Upon initial system start-up, the mains filtering capacitor is charged through the rectifier diode bridge.

The voltage across the device power supply capacitor (pin 16) is low and less than the "$V_{CC(START)}$" value. The TEA2164 is therefore in low consumption state. The supply voltage capacitor "C_{16}" begins charging through a high value (100kΩ) resistor "R_{START}" connected to the rectified mains voltage.

Figure 18



The capacitor charge up time is given by :

$$t_{CHARGE} = \frac{V_{CC(START)} \times C_{16}}{\frac{V_{IN}}{R_{START}} - I_{CC(START}}$$

$$t_{CHARGE} = \frac{9 \times 220 \times 10^{-6}}{\frac{310}{100 \times 10^{-3}} - (0.8 \times 10^{-3})} = 0.85s$$

At minimum mains voltage level : t_{CHARGE} = 1.2s

- The power dissipated within "R_{START}" resistor is :

$$P = \frac{(V_{IN} - V_{CC})^2}{R_{START}}$$

$$P = \frac{(310 - 12)^2}{100 \times 10^3} = 0.9W \text{ (P = 1.4W at Mains max level)}$$

An application variant is when the start up resistor is directly connected to non-rectified mains.

In this case and in order to obtain an identical start-up time, the value of "R_{START}" resistor must be divided by π. The power dissipation is thus reduced by approximately 30%.

III.6.2 - Self-supply

As soon as the voltage on pin 16 reaches the $V_{CC(START)}$ level of 9V, the TEA2164 will start-up and deliver the base drive pulses to the switching transistor at internal oscillator frequency (set by R_{OSC} and C_{OSC}). The duty cycle of these pulses gradually increases (soft-start). During this cycle of operation, the device does not receive any control pulse from the secondary controller circuit and therefore operates in "Burst mode".

The start-up will correcty take place if the device is rapidly self-supplied, that is, before the voltage across the supply capacitor on pin 16 falls below $V_{CC(STOP)}$ threshold.

The TEA2164 is supplied by two distinct secondary windings, one connected in flyback and the other in forward configuration.

The forward voltage will rapidly provide the supply required by TEA2164 whereas the flyback voltage will begin rising slowly and depends on various secondary time constants.

Main advantage of the flyback voltage is that it provides a regulated supply voltage proportional to the secondary voltages.

A +12V voltage has been selected for device power supply at nominal mains voltage level. A lower value such as +10V can be selected which will also reduce the power dissipation. Note however that since the overvoltage protection threshold is internally set at +15V, then the lower is the supply voltage level the greater will become threshold margin.

At nominal mains voltage, the forward voltage value is selected to be 1V below the flyback voltage value so that, the supply voltage at maximum mains voltage, will not rise much above its nominal value (and will remain below 15V threshold level).

III.6.3 - Secondary controller circuit start-up

After a time interval required for the secondary

power supply capacitors to charge up, the secondary-connected regulation controller circuit will be powered and as soon as its supply voltage "V_{CC}" reaches the "$V_{CC(START)}$" level, it will begin delivering regulation and synchronization pulses. The TEA2164 will receive these pulses and will consequently switch from "Burst Mode" to "Normal Mode" synchronized and regulated by the secondary controller circuit.

The secondary controller circuits (TEA2028, TEA2029 and TEA5170) have a "soft-start" function. This system allows better transition when switching from stand-by mode to normal mode.

The TEA2028 and TEA2029 controllers have no "$t_{ON(MIN)}$" function, and for this reason, it is necessary to choose lower voltage in stand-by mode than in normal mode. Otherwise, switching from stand-by mode to normal mode will not be possible (secondary controller circuit will not issue regulation pulses as long as the output voltage remains above its nominal value).

The TEA5170 has a "$t_{ON(MIN)}$" function, but it is also recommended to choose the stand-by voltage under the nominal value so as to avoid overvoltage when switching from stand-by mode to normal mode.

For further details on secondary controller circuits, please refer to TEA5170 and TEA2028-TEA2029 Application Notes (AN407/0591).

III.7 - Protection features

III.7.1 - Overload protection

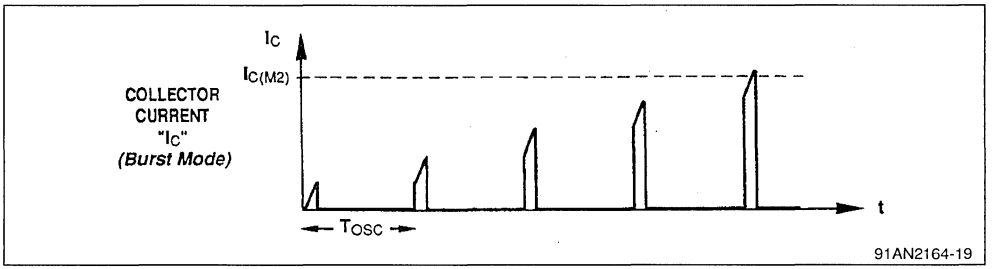
The current limitation is set by resistor "R_S" as a function "$I_{C(M1)}$" threshold, such that the power transfer is limited at 150W. If the load connected to secondary requires higher power, the current limitation is activated and will limit the power transfer by lowering the output voltage.

III.7.2 - Short-circuit protection

In case of short-circuit, the secondary voltage falls to zero and the time required for the transformer to demagnetize becomes very long. The collector current will no longer start at zero level but at the final value of the preceding period. The current value will rapidly reach "$I_{C(M1)}$" and then "$I_{C(M2)}$" threshold levels.

Only the "$I_{C(M2)}$" threshold will disable the device and switch it into "Burst Mode". The device will re-start at the beginning of the following VLF oscillator period. However, if the short-circuit still persists, the "$I_{C(M2)}$" protection threshold is once again activated.

Figure 19



III.7.3 - Repetitive overcurrent protection

Each time that "$I_{C(M1)}$" or "$I_{C(M2)}$" thresholds are reached, an event counter will charge up the capacitor "C2" connected to pin 3. If the overload persists, the voltage across capacitor will reach the 3V threshold level and TEA2164 is consequently disabled (no power transfer to secondary will take place).

To exit this protection mode, the mains voltage must be disconnected during a time interval long enough for all capacitors to fully discharge. The system can re-start only once the capacitors have been discharged.

III.7.4 - Overvoltage protection

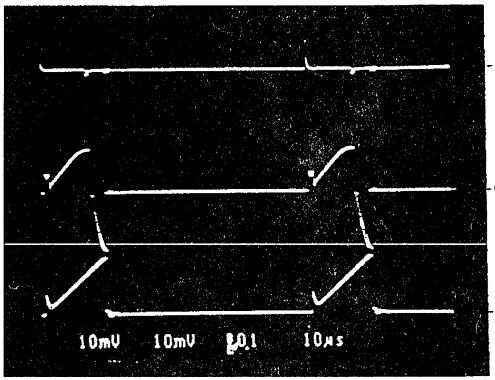
If an overvoltage (produced by improper adjustment or failure) appears at secondary terminals, the primary flyback voltage will rise and if the +15V threshold level is reached, the TEA2164 is disabled.

An overvoltage would be also generated if the load on secondary terminals is disconnected. In this case, if the secondary controller device is not equiped with $t_{ON(MIN)}$ feature (TEA2028 , TEA2029), it will stop sending the regulation pulses and the TEA2164 will consequently enter into "Burst Mode".

If the secondary controller device has a "$t_{ON(MIN)}$" function (TEA5170), the protection is performed at the primary side by the +15V overvoltage threshold level.

III.8 - Oscillograms

Figure 20



1 - NORMAL MODE : *Base Current*

$V_{PIN\ 6}$: 1V/div

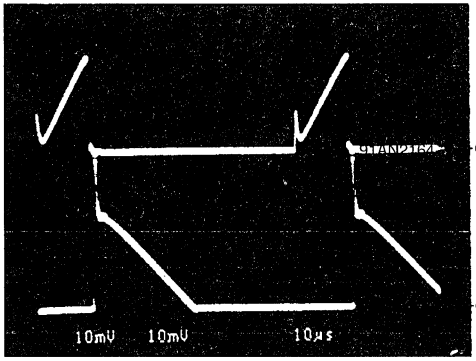
I_B : 1A/div

I_C : 2A/div

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

Figure 21



2 - NORMAL MODE : *Primary and Secondary Currents*

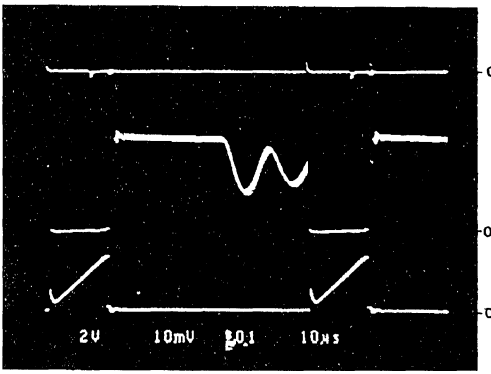
I_C : 1A/div

I_S : 1A/div

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

Figure 22



3 - NORMAL MODE : *Collector-emitter Voltage*

$V_{PIN\ 6}$: 1V/div

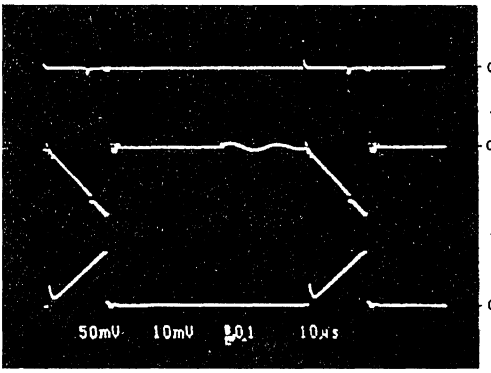
V_{CE} : 200V/div

I_C : 2A/div

Mains : $220V_{AC}$
Load : 90W

Scale : 10µs/div

Figure 23



4 - NORMAL MODE : *Current Limitation Voltage*

$V_{PIN\ 6}$: 1V/div

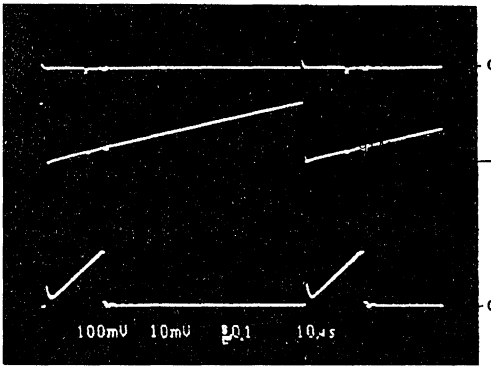
$V_{PIN\ 11}$: 0.5V/div

I_C : 2A/div

Mains : $220V_{AC}$
Load : 90W

Scale : 10µs/div

Figure 24



5 - NORMAL MODE : *Oscillator Saw-tooth*

$V_{PIN\ 6}$: 1V/div

$V_{PIN\ 8}$: 1V/div

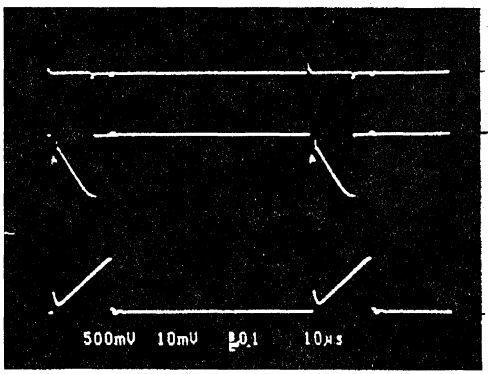
1.6V

I_C : 2A/div

Mains : $220V_{AC}$
Load : 90W

Scale : 10µs/div

Figure 25



6 - NORMAL MODE : *V+ Supply Voltage*

$V_{PIN\ 6}$: 1V/div

12V

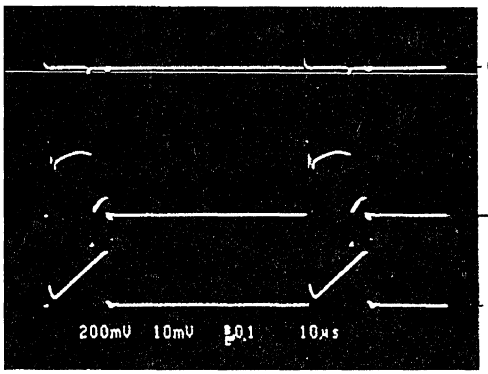
$V_{PIN\ 15}$: 5V/div

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

I_C : 2A/div

Figure 26



7 - NORMAL MODE : *Output Voltage*

$V_{PIN\ 6}$: 1V/div

$V_{PIN\ 14}$: 2V/div

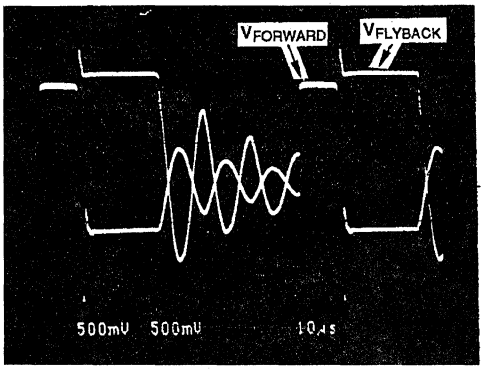
0.5V

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

I_C : 2A/div

Figure 27



8 - NORMAL MODE : *Flyback and Forward Voltages*
(TEA 2164 Power Supply)

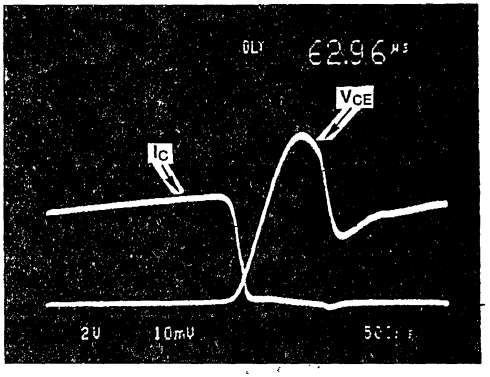
$V_{FORWARD}$: 5V/div

$V_{FLYBACK}$: 5V/div

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

Figure 28



9 - NORMAL MODE : *Transistor turn-off*

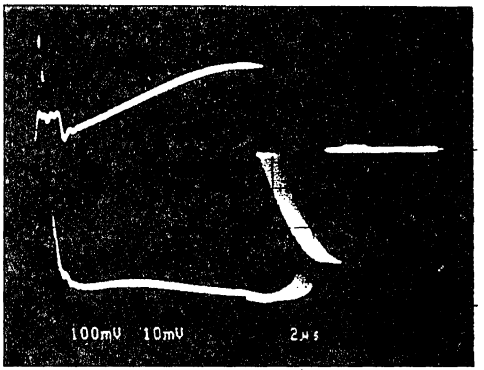
V_{CE} : 200V/div

I_C : 1A/div

Mains : 220V_{AC}
Load : 90W

Scale : 500ns/div

Figure 29



10 - NORMAL MODE : *Saturation Voltage*

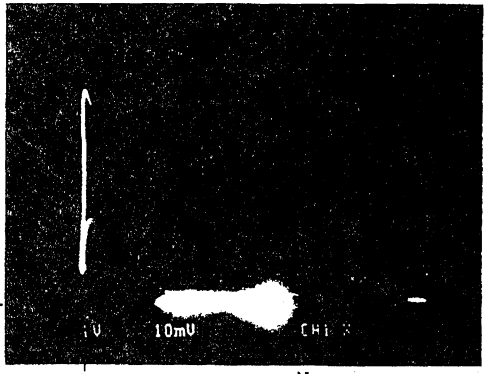
I_B : 0.5A/div

Mains : 220V_{AC}
Load : 90W

Scale : 2µs/div

$V_{CE(SAT)}$: 1V/div

Figure 30



11 - NORMAL MODE : *Safe Operating Area*

Mains : 220V_{AC}
Load : 90W

I_C : 0.5A/div

V_{CE} : 100V/div

Figure 31

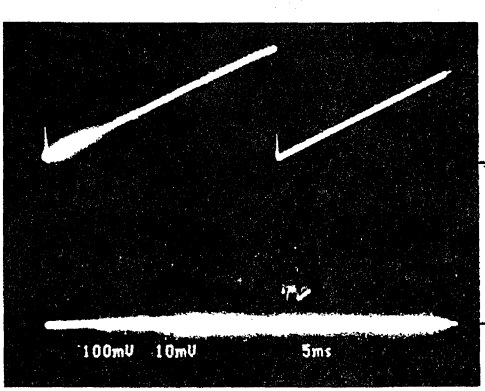


Figure 32

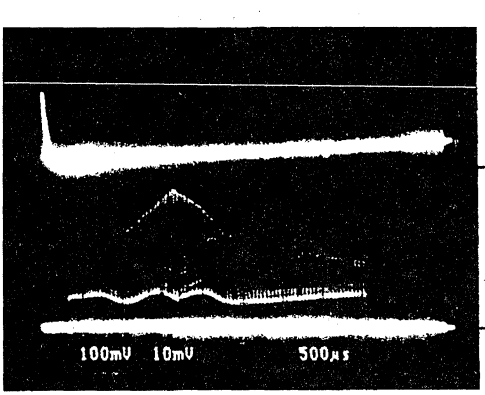


Figure 33

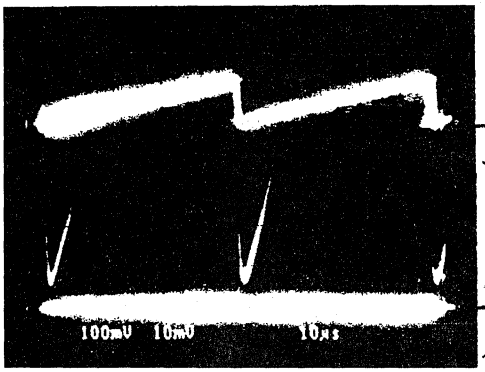


Figure 34

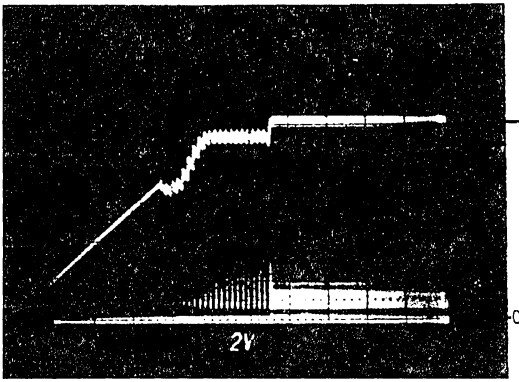


Figure 35

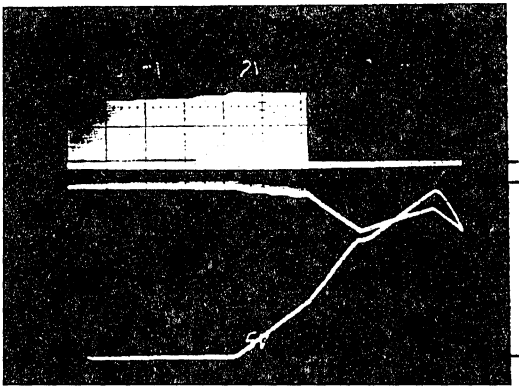
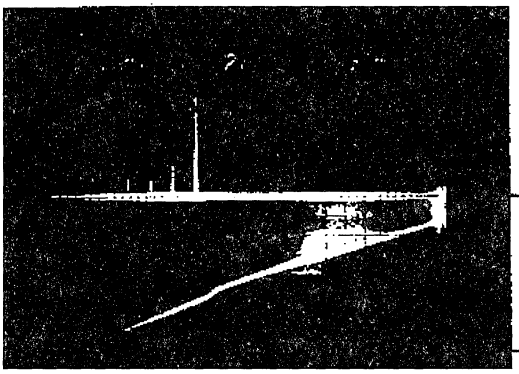


Figure 36



IV - APPLICATION VARIANTS

V.1 All mains application

IA wide input voltage range application can be configured around TEA 2164. We have built a power supply delivering 90W output power at mains input voltage range of $90V_{AC}$ to $260V_{AC}$.
Difficulties encountered in such application are given below :

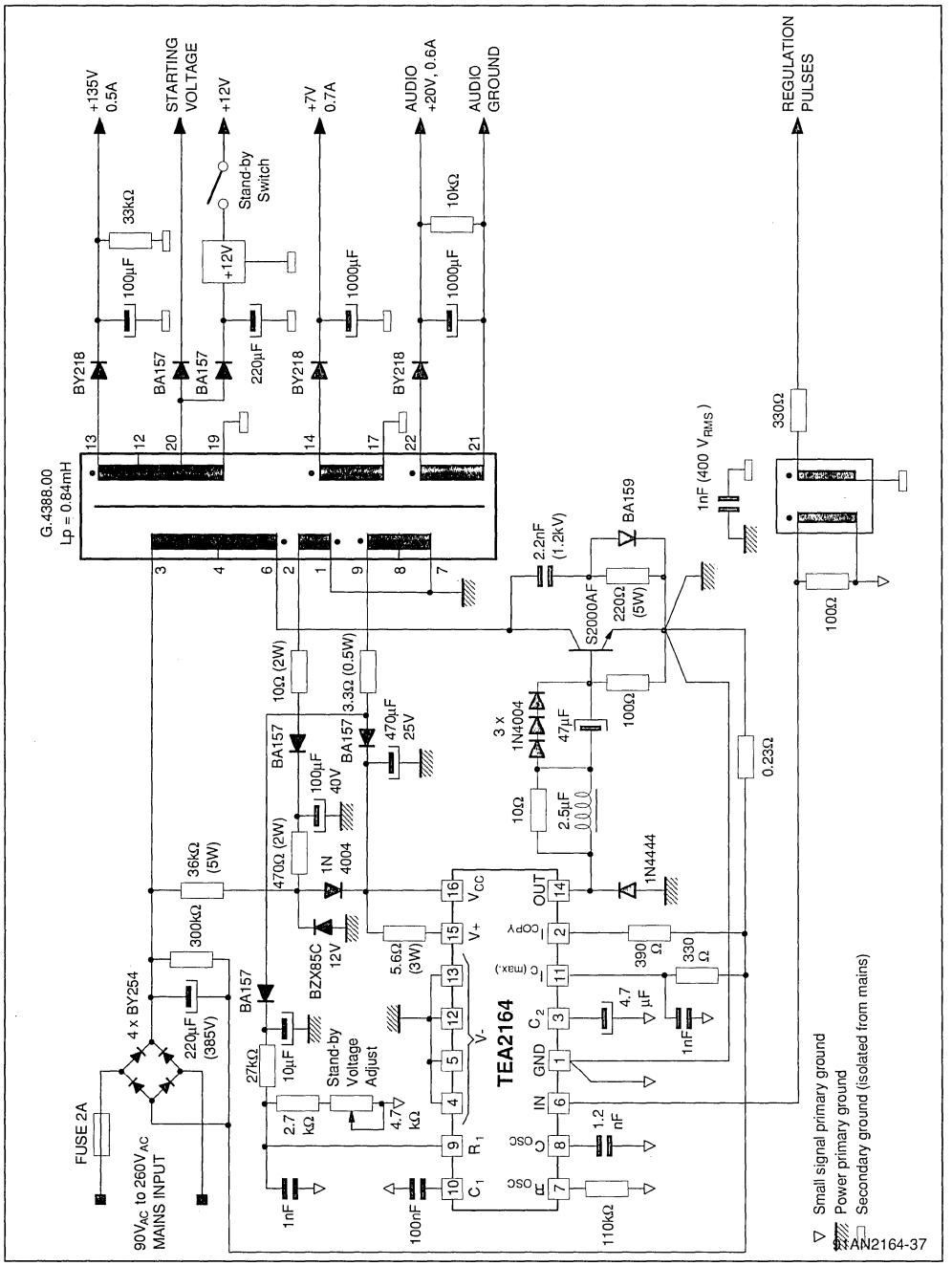
- Very wide regulation range : if a discontinuous mode flyback transformer is employed, the conduction time would be highly variable.
  The "$t_{ON(MAX)}$" duration is determined as a function of maximum power output and the minimum mains voltage level.
  The "$t_{ON(MIN)}$" duration is determined as a function of minimum power output and the maximum mains voltage level.
- Start-up at minimum mains level : appropriate selection of start-up resistor and self-supply windings.
- Optimized switching transistor base drive and appropriately dimentioned protection features to operate over the whole mains voltage range :

both, the base current, and supply voltage values and hence the self-supply windings, must be appropriately calculated.

FEATURES

- Discontinuous mode flyback SMPS (L_P = 0.84mH)
- Standby function using the burst mode of TEA2164
- Switching frequency :
  - Normal mode : 15625 Hz (synchronized on horizontal deflection frequency)
  - Stand-by mode : 19 kHz
- Mains voltage range : 90 V_{AC} to 260 V_{AC}
- Mains power consumption :
  - Normal mode : 110 W max
  - Stand-by mode :
    6.7W (at 110V)
    9.8W (at 220V)
    (without degaussing coil)
- Efficiency :
  - Normal mode :
    83% (at 110V)
    80% (at 220V)
    (measured with 86W output power)

Figure 37 : 90 Volts to 260 Volts Application Diagram



IV.2 - 117 Volts application

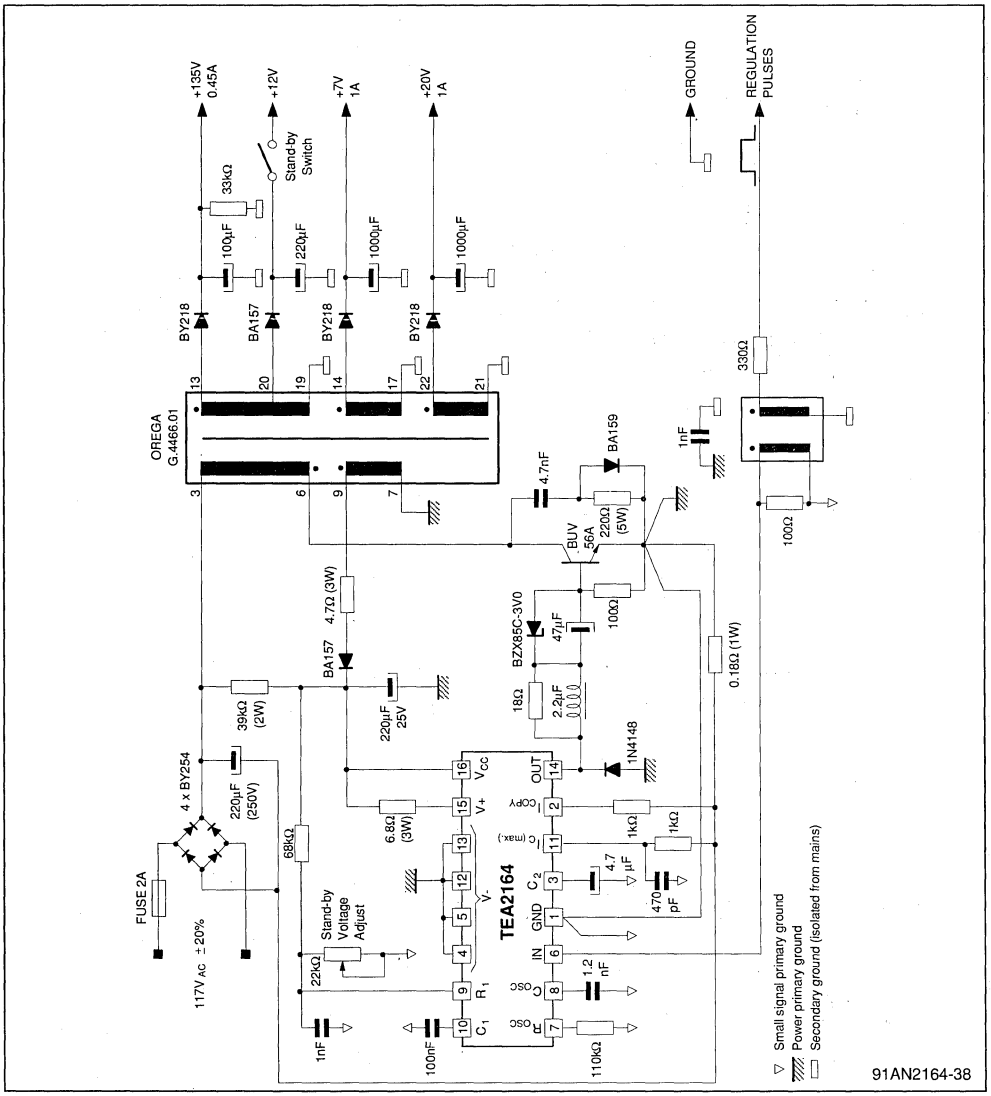
Main Features :

- Discontinuous mode flyback SMPS (L_P = 0.62mH)
- Switching Frequency : 15.7kHz
- Mains Voltage Range : 90V_{AC} to 140V_{AC}
- Output Power : 90W
- Stand-by using the burst mode of TEA2164

Comment :

An optimization of the start up has permitted to eliminate the need of the self-supply forward winding and therefore to suppress some components.

Figure 38 : 117 Volts Application Diagram

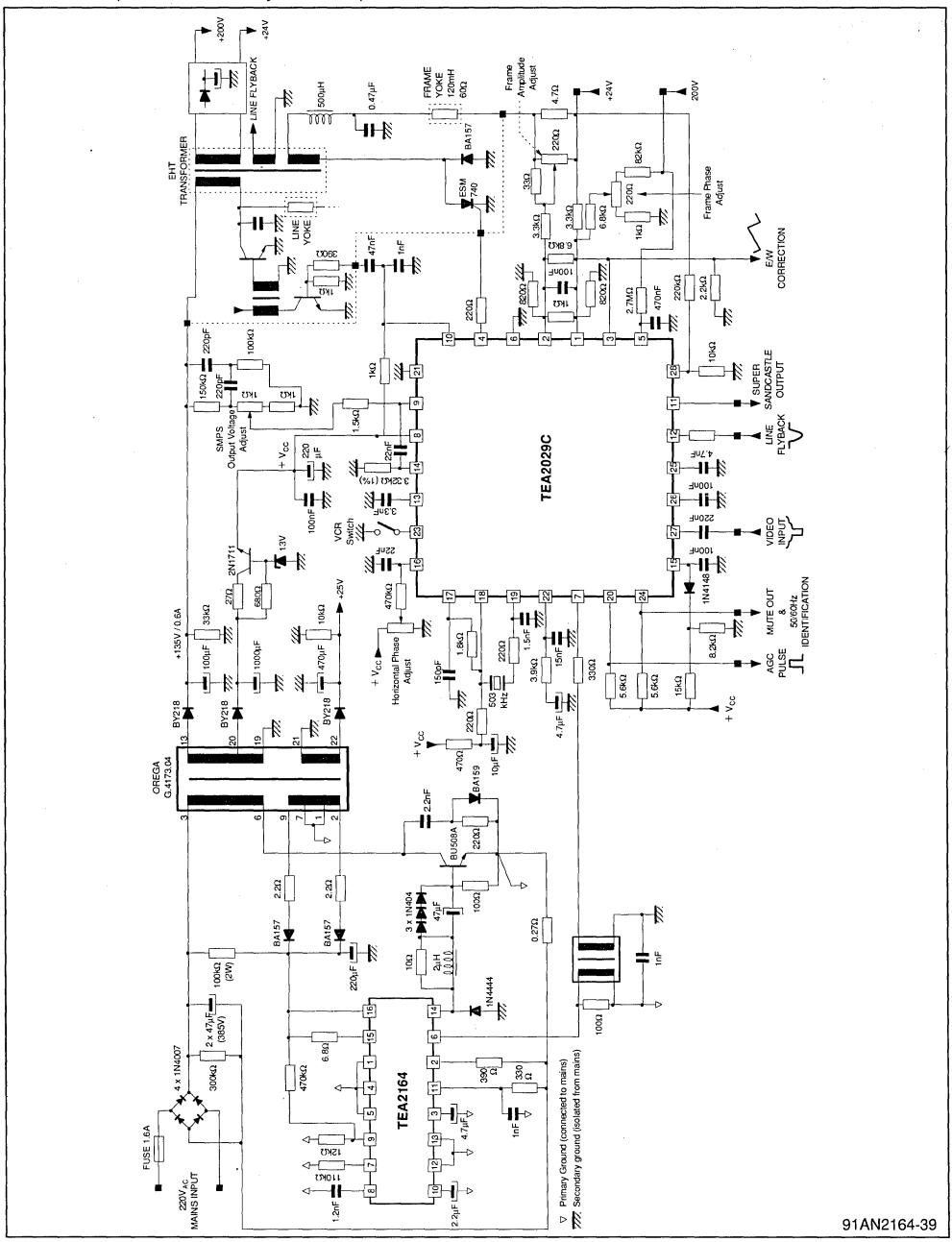


IV.3 - Application without stand-by

The application arrangement is simplified if the stand by function is not required :

- The "Master" circuit on the secondary side is permanently powered and as a consequence the transistors used to cut its power supply are no longer needed and can be eliminated.
- The feedback used for "stand-by" regulation function on the primary side configured around pin 9 of TEA 2164, can be simplified.
- The value of "C1" capacitor connected to pin 10 of TEA 2164 used to set the burst period and therefore its duration, is increased (1µF or 2.2µF) so as to enable full load system start-up as soon as the first burst is available.

Figure 39 : Complete Application Diagram (SMPS + Deflection)
(Without Stand-by Function)



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2037
HORIZONTAL & VERTICAL DEFLECTION CIRCUIT

By : B. D'HALLUIN

SUMMARY

I - INTRODUCTION

The TEA2037 is a horizontal and vertical deflection circuit for monitors and black and white TV sets.

This device includes all functions required for deflection, namely :

- Line and frame sync separation
- Line oscillator with phase comparator
- Driver stage for line deflection darlington transistor
- Frame oscillator
- Frame amplifier with flyback generator for direct drive of the vertical deflection yoke.

The TEA2037 is particularly well-suited for low-cost monitors since it is cased in a low-cost package and requires a few number of external components and hence optimized for small displays.

However, application areas are by no means limited. Sophisticated applications requiring various adjustment possibilities such as for display geometry and centering settings (amplitude, linearity,...) and operating at different line and frame frequencies (line frequencies up to 64kHz), are readily configured around TEA2037.

In large screen applications, addition of a heatsink mounted on TEA2037 will enable the vertical deflection yoke current to be boosted to 2A peak-to-peak.

II - FUNCTIONAL DESCRIPTION OF TEA 2037

II.1 - General description

The TEA2037 is a 16-pin DIP package. The 4 center pins (2 on each side) are connected together and used as heatsink.

From composite video or TTL-compatible sync. signals, the device will extract and generate all signals required for the line scanning darlington transistor and direct drive of the frame yoke.

The following functional blocks are implemented on-chip :

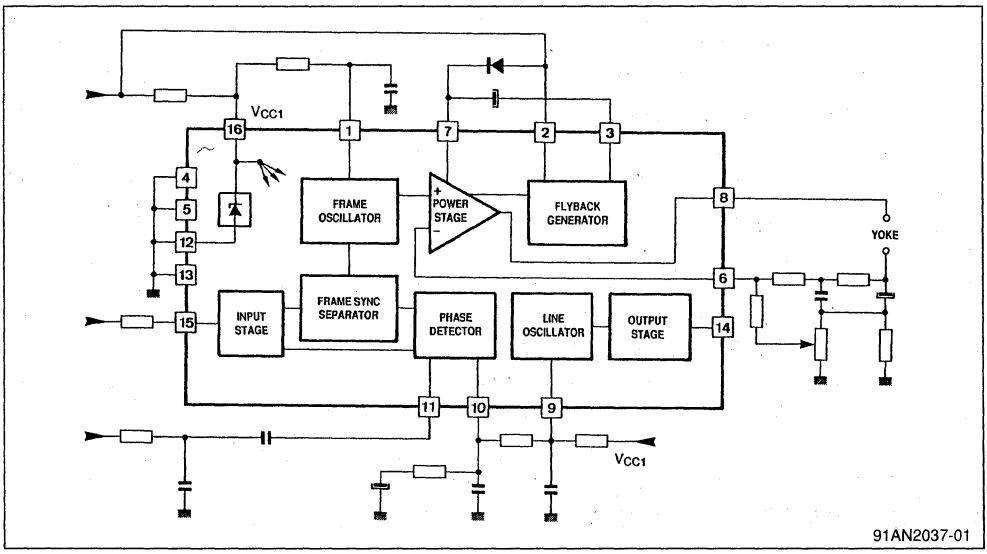
- Line and frame sync. separator
- Line oscillator
- Line phase comparator
- Line output stage
- Frame oscillator
- Frame amplifier
- Frame flyback generator
- Shunt regulator

The common device power supply is implemented by the on-chip shunt regulator.

In order to optimize the drive to frame deflection yoke and also enable appropriate use of the flyback generator, the frame amplifier is powered by an independent supply.

The ground is connected to the 4 center pins of the device.

Figure 1 : Block Diagram

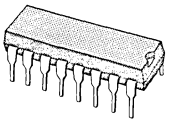


Pin description

1	Frame Oscillator
2	V_{CC2} (Flyback generator power supply)
3	Flyback generator output
4, 5	Ground
6	Frame feed-back (frame amplifier inverting input)
7	V_{CC2} (positive power supply for frame output stage)
8	Frame output (direct drive to frame yoke)
9	Line oscillator
10	Phase comparator output
11	Phase comparator input (line flyback)
14	Line output (drive to line darlington transistor)
15	Video input (or TTL-compatible sync.)
16	V_{CC1} (shunt regulator)

Package

Batwing DIP16
(plastic package)



II.2 - Sync. pulse separator

The TEA2037 extracts, first the line and frame sync. pulses from the composite video signal and then the largest pulses, i.e., the frame syncs.

II.2.1 - Extraction of sync. pulses from the composite video signal (TV application).

Figure 2

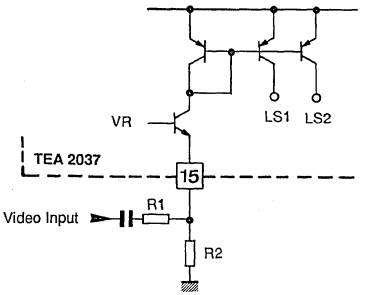
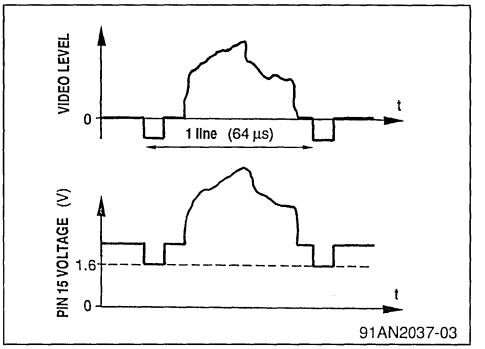
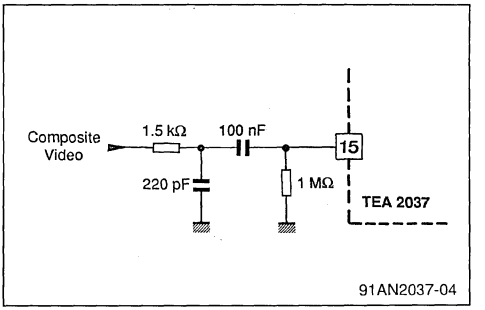


Figure 3



- The sync. detection level is set at 1.6 V.
- The value of R2 is typically 1 MΩ (fixed for a good internal bias).
- Resistor R1 limits the output current of pin 15.

Figure 4



As illustrated in the above Figure, it is recommended to employ a low-pass filter which will suppress high-frequency harmonics susceptible to produce jitters on line sync signal in composite video TV applications.

II.2.2 - Negative TTL SYNC. (Monitor application)

Figure 5

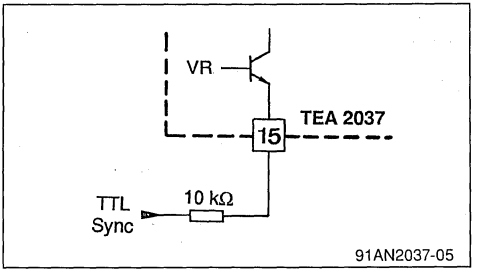
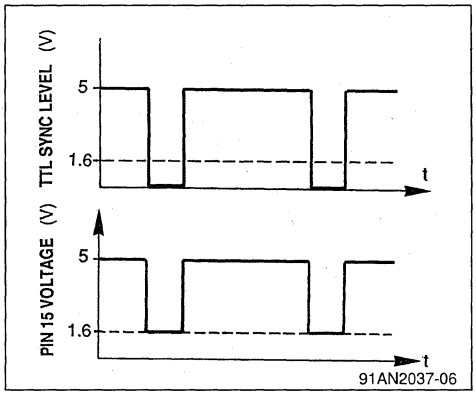


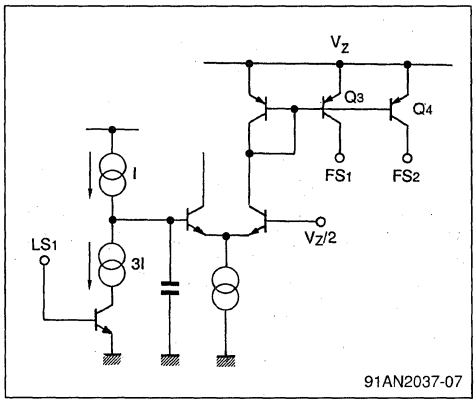
Figure 6



In monitor application, the sync. signal is generally separated from the video signal.
In this case, the sync. signal is applied to pin 15 through a single limiting resistor. Similar to the former case, the sync. is detected when the input voltage falls below 1.6 V level.

II.2.3 - Frame sync. extraction

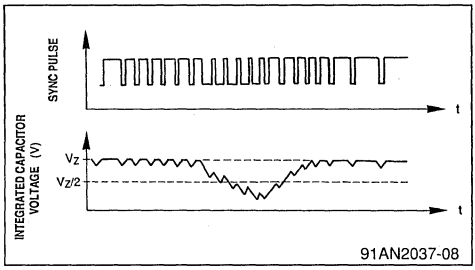
Figure 7



This function is processed internally and hence does not require any external component. Line and frame sync. pulses are distinguished by an integrated capacitor which is more or less discharged during each sync. pulse interval as follows :

- if the sync pulse duration is short, i.e. it is line sync, then the capacitor is slightly discharged
- on the other hand, if the pulse width is larger, the capacitor is fully discharged and an internal frame signal is thus generated.

Figure 8



II.3 - Line oscillator

Figure 9

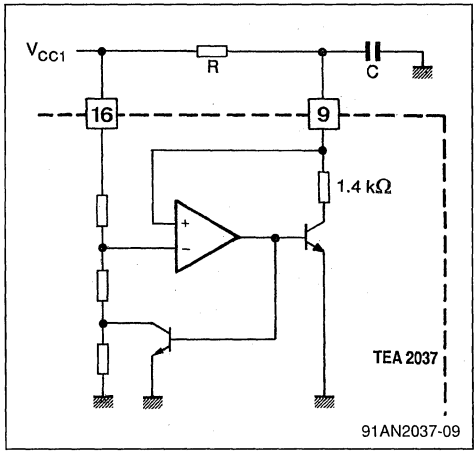
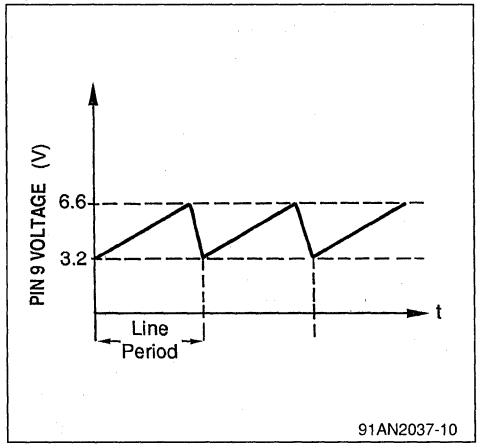


Figure 10



The line saw-tooth is generated by charging an external capacitor on pin 9 via a resistor connected to V_{CC1} (pin 16).

The capacitor is discharged via an internal 1.4 kΩ resistor. The saw-tooth amplitude is set by two on-chip threshold levels :

- lower threshold : 3.2 V
- higher threshold : 6.6 V

The free-running period is approximately given by the following relationship :

$$T_{OSC} \approx 0.85\ RC$$

The phase comparator will modify the capacitor charge by injecting a positive or negative current so as to produce correct phase and frequency relationships with respect to the synchronization signal.

II.4 - Line output stage

The line output stage has been designed for direct base drive of the horizontal scanning darlington transistor.

The low level interval on pin 14, i.e. the power line transistor blocking period, is determined by the time when the voltage of the line oscillator capacitor (pin 9) is below 4.8 V (internally set threshold level). In a typical application, this interval corresponds to 22µs at 64µs free-running period.

Figure 11

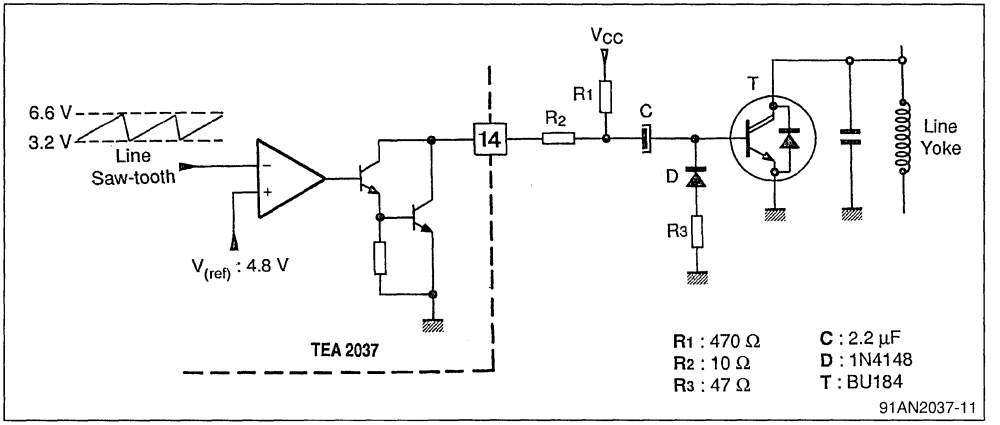
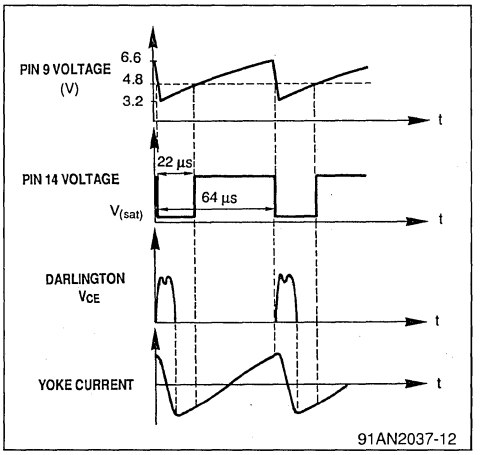


Figure 12

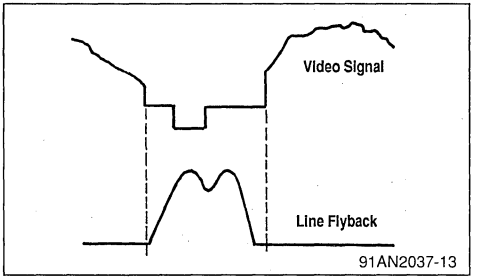


II.5 - Phase comparator (PLL)

II.5.1 - Functional description

The duty of phase comparator is to synchronize the horizontal scanning with the line sync pulse and ensure correct line flyback during the horizontal blanking phase.

Figure 13



The line flyback signal (i.e. the pulse on the collector of the line scanning transistor) is compared with the line sync. signal issued by sync. separator. If the detected coincidence is incorrect, the comparator will then generate an appropriate positive or negative current so as to charge or discharge the line oscillator capacitor thereby providing for frequency and phase locking.

II.5.2 - Phase comparator operation

Figure 14

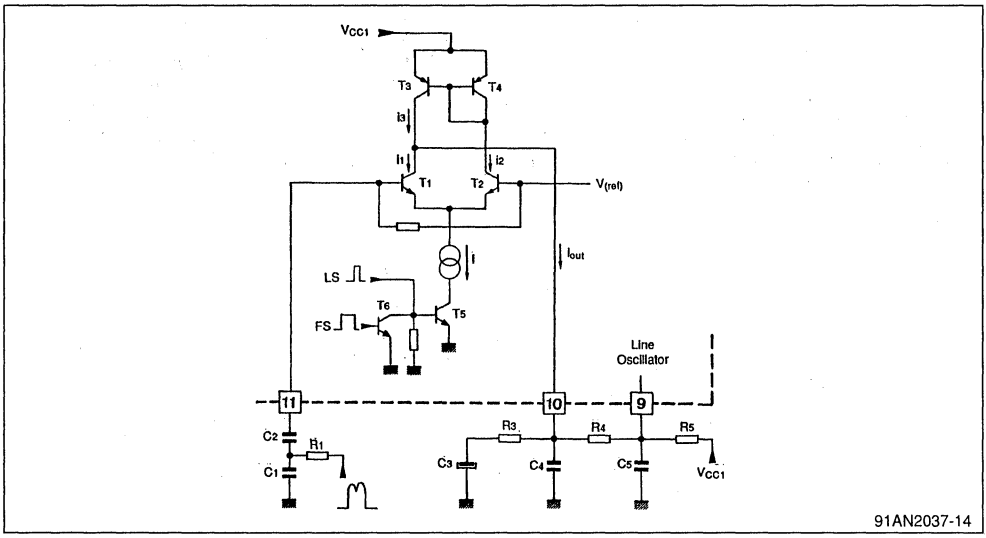
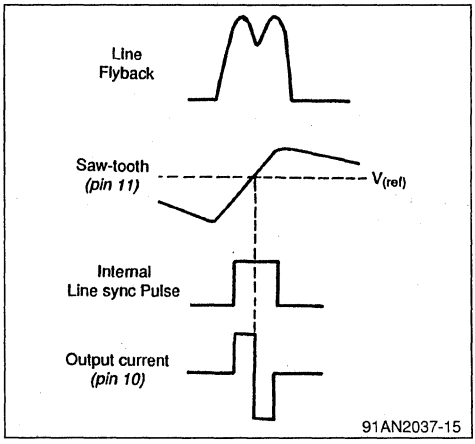


Figure 15



The line flyback signal goes through integrator network R1C1 the output of which, a saw-tooth signal, is applied to comparator input (pin 11) via capacitor C2.

The comparator input stage is formed by the differential pair T1 and T2. T3 and T4 transistors are arranged in current mirror configuration and thus : $i_3 = i_2$

The sum of currents going through T1 and T2 transistors is determined by the current generator "I" so that : $I = i_1 + i_2$.

The comparator output current is the difference current through the differential pair, i.e. :

$$i_{OUT} = i_2 - i_1$$

The comparator is enabled by T5 transistor only during the line sync. interval.

Transistor T6 inhibits the phase comparison during the frame sync. interval.

During the first portion of the flyback, the voltage at comparator input (pin 11) is lower than the reference voltage. T1 is off and T2 conducts ; consequently the comparator output goes positive :

$$i_{OUT} = +I$$

During the second portion, the input voltage ex-

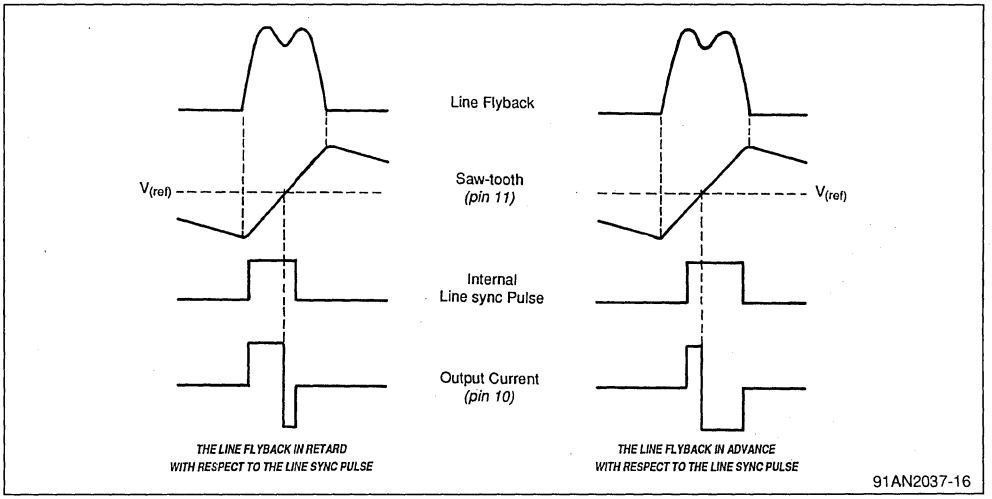
ceeds the reference voltage and as a result, the comparator ouput falls to negative level :

$$i_{OUT} = -I$$

If the line flyback is in retard with respect to the horizontal sync. pulse (which is the case of too long line periods), the interval for which the phase comparator's output current is positive would increase. This current is then filtered and applied to the line oscillator capacitor (C5) thereby accelerating its charge-up phase and hence reducing the line period.

Inverse action takes place if the line flyback is in advance - the negative current at comparator's output will rise, C5 is charged more slowly and the line period is thus increased.

Figure 16



II.5.3 - Output filter

Figure 17

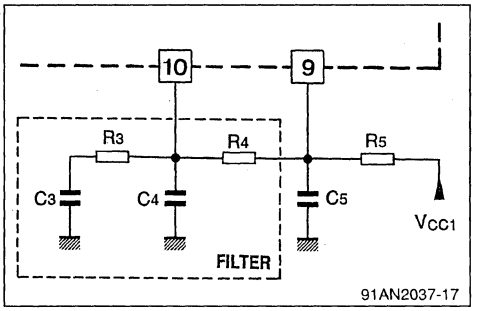
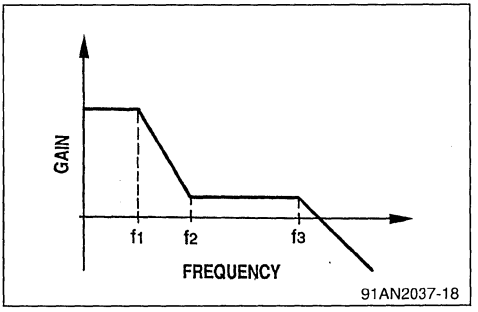


Figure 18



$$f_1 = \frac{1}{2\pi\,(R3 + R4)\,C3} \qquad f_2 = \frac{1}{2\pi R3C3} \qquad f_3 = \frac{R3 + R4}{2\pi R3R4C4}$$

The duty of the output filter is to ensure the stability of the locked loop and its characteristics will have a partial influence on capture range and also on capture time.
The holding range, which is larger than the capture range, depends on the ratio of the current available at the comparator output and the charging current of the line oscillator. The holding range does not depend directly on the cut-off frequencies of the output filter. But, as the voltage range at the comparator output is limited, a too high value for R4 will limit the holding range.
The sync. pulse duration has significant influence on capture range and also on the holding range of the device. The output current duration is directly related to synchronization pulse width.

- First the R5 x C5 product is selected to yield the required free-running line oscillator frequency.
- Then, the value of C5 capacitor is selected as follows :
  - for monitor applications (large holding range) low value; e.g. :2.2 nF @ 16 kHz, 1 nF @ 32 kHz
  - for TV applications higher value; e.g. : 4.7 nF @ 16 kHz

  Finally, the filter components are selected to match the required capture range.
  (R4 ≤ 100 kΩ to prevent comparator output saturation)

II.6 - Frame oscillator

Similar to line oscillator, the frame saw-tooth is generated by charging an external capacitor on pin 1 through a resistor connected to V_{CC1}.

Figure 19

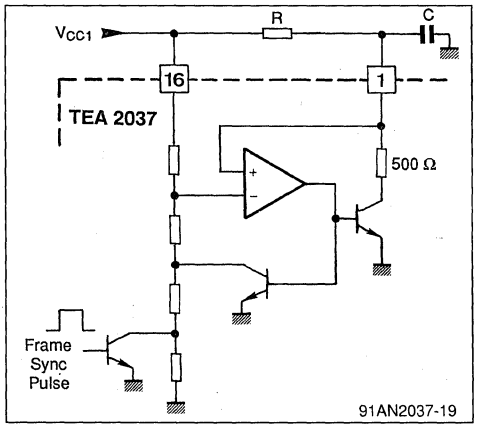
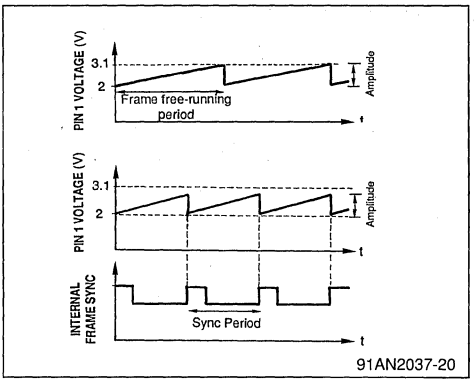


Figure 20



The capacitor is discharged via an internal 500 Ω resistor. The saw-tooth amplitude is set at two on-chip threshold levels.
The free-running period is approximately given by :

$$T_{OSC} \approx 0.15\ RC$$

Synchronization is achieved by period reduction.
The frame sync. pulse issued by the sync. separator will modify the current through the resistor bridge which is used to set the saw-tooth threshold levels.
The minimum synchronized frame period (MSFP) is given by :

$$MSFP \approx \frac{T_{OSC}}{1.8}$$

II.7 - Frame output amplifier

The frame saw-tooth generated by frame oscillator is first inverted (Gain : - 0.4) and then applied to the non-inverting input of the frame amplifier. The output current capability of this amplifier is as high as ± 1A thus enabling to drive vertical deflection yokes requiring 2A peak-to-peak.
As a function of dissipated power, the device may require the addition of a heatsink.
A feed-back loop is connected to the inverting input of the frame amplifier (pin 6).
As the CRT screen is not part of a sphere centered on the deflection center point, if the yoke is actually driven by a saw-tooth waveform, the image is expanded at the top and bottom. The yoke must therefore be provided with an "S" waveform current, by applying linearity correction.
The circuit configuration depicted above does not require any linearity adjustment - only an amplitude

Figure 21

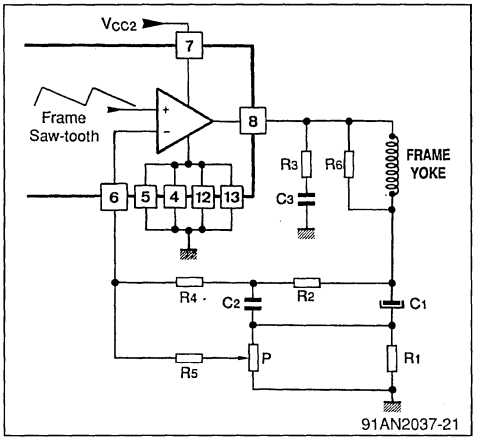
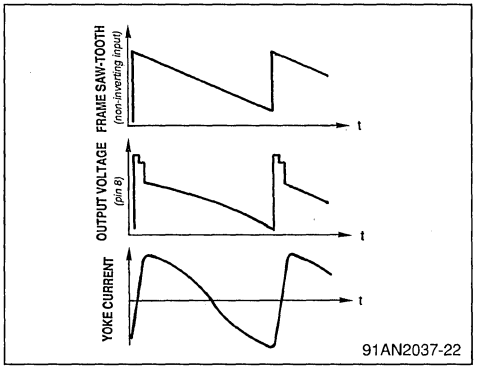


Figure 22



adjustment potentiometer "P" has been provided for.

- **D.C. Feedback :** The C1 capacitor is charged to approximately 1/2 x V_{CC2}. Divider bridge formed by R2 + R4 and R5 networks will set the d.c. feedback. The component values of this divider network will be choosen to avoid saturation at top and bottom of the output voltage. (pin 6 biasing voltage is approximately 0.6 V)
- **Linearity Correction :** A parabolic signal at frame frequency is available on "+" terminal of the C1 capacitor. This signal is integrated by R2, C2 network. An "S" waveform is thus obtained, which is applied to pin 6 via resistor R4.

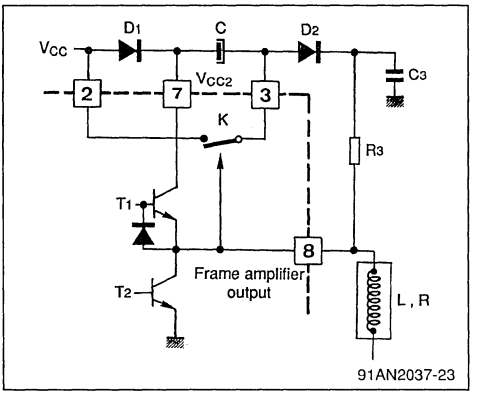
  Any correction to this "S" waveform depends on C1 and C2 values. The linearity correction depends on ratio : R2/R4
- **Vertical Amplitude :** Frame current amplitude is determined by the value of measurement resistor "R1", potentiometer "P" settings and the value of "R5" resistor.

II.8 - Frame flyback generator

The output stage of the vertical amplifier includes a frame flyback generator connected to pin 3. During the vertical scanning flyback time, the value of the yoke inductance "L" must be taken into account since the time constant L/R is no longer negligible. In television applications, the frame blanking time is 1.6 ms. Thus when $L/R > 1.6 \times 10^{-3}$, it is necessary to increase the supply voltage to the frame output amplifier so as to reduce the flyback time. This surplus is required only for the frame flyback and energy is wasted by boosting the supply to the amplifier at all times (during the frame scanning time, the minimum voltage is substantially RI, where I is peak-to-peak frame current).

The configuration of the flyback generator is depicted in Figure below :

Figure 23

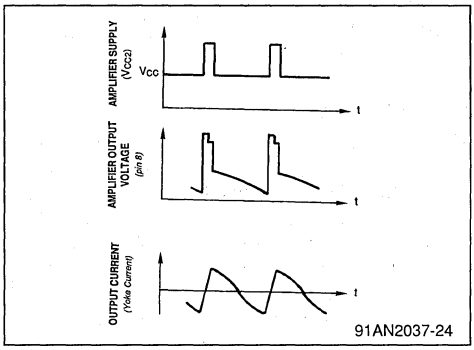


During the second half of the vertical scanning time, transistor T2 conducts and capacitor C is charged to V_{CC} through D1, D2, R3 and T2. (Switch K open)

On flyback, switch K closes and pin 3 is connected to V_{CC}. The voltage at pin 7 (V_{CC2}), which was equal to $V_{CC} - V_{D1}$, is almost doubled during the flyback time. The only external components required are therefore D1, D2 and C.

In addition to reducing the flyback time, the flyback generator reduces the power consumed by the power stage, and can in certain cases avoid the

Figure 24

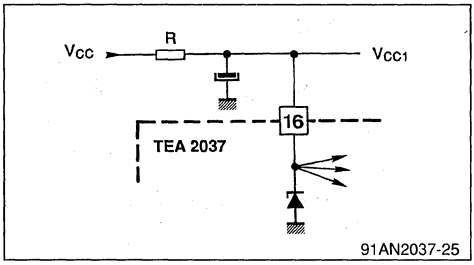


need to use a heatsink.
Diode D2 is a low-signal diode (1N4148) but diode D1 must be appropriately rated since the positive current in the first part of the saw-tooth is supplied to the yoke through D1 and T1. A 1N4001 is generally used.

II.9 - The shunt regulator

The TEA2037 incorporates an internal shunt regulator which delivers the common supply voltage V_{CC} to various blocks such as oscillators, comparator, sync separator and so on.
The voltage on pin 16 is 9.7 V (9 V min, 10.5 V max). The value of the series resistor R must be so calculated to obtain a 15 mA current on pin 16 - this

Figure 25



current can be 10 mA min. and 20 mA max.
The external current supply from V_{CC1} to both oscillators (i.e. line and frame) can be neglected in majority of cases.
The resistor value is found to be 1.2 kΩ at V_{CC} = +28V.
At V_{CC} = + 12 V, and taking into account the voltage tolerance on pin 16, a 150 Ω series resistor must be used.

II.10 - Thermal considerations

In order to ensure reliable device operation, the dissipated power should be accurately determined. Calculation will allow an evaluation of the dissipated power and should be completed by package temperature measurements in actual applications. According to results obtained, a heatsink may or may not be required.

■ Power drawn from V_{CC1} supply :

$$P1 = V_{CC1} \cdot I_1$$

Where I_1 is the current through the shunt regulator (pin 16)

■ Power drawn from V_{CC2} supply :

$$P2 = V_{CC2}\left(\frac{I_{PP}}{8} + I_2\right)$$

Where :

- Ipp = peak-to-peak current through the vertical deflection yoke.
- I_2 = Pin 7 quiescent current.
- V_{CC2} = Pin 7 voltage.

■ Power dissipated in deflection yoke and the measurement resistor :

$$P_Y = (R_Y + R_M)\frac{I^2pp}{12}$$

Where :

- R_y = Frame deflection yoke resistance
- R_M = Measurement resistor value

Thus, the overall power dissipated in the integrated circuit is :

$$P_D = P1 + P2 - P_Y$$

$$P_D = \left[V_{CC1} \cdot I_1\right] + \left[V_{CC2}\left(\frac{Ipp}{8} + I_2\right)\right] - \left[(R_Y + R_M)\frac{I^2pp}{12}\right]$$

In application using the flyback generator, the V_{CC2} specified above becomes "V_{CC2} - V_D", where V_D is the voltage drop across the series diode.

Figure 26

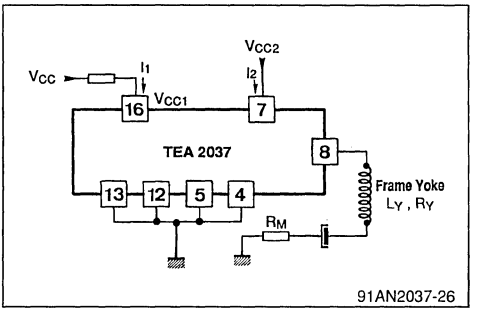
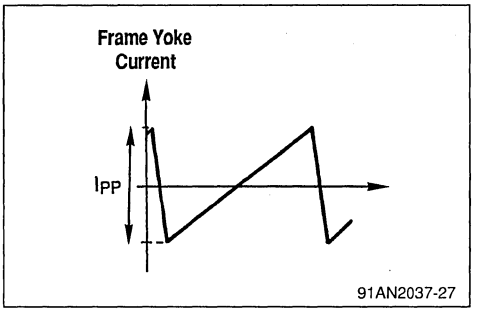


Figure 27



III - APPLICATION EXAMPLES

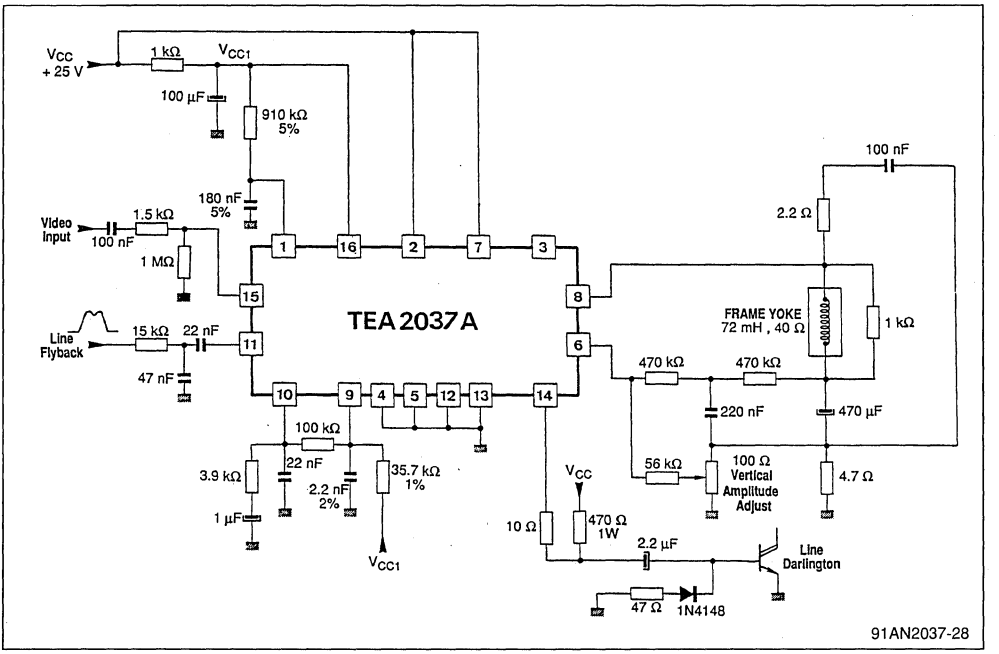
III.1 - Monitor applications

III.1.1 - Low-cost monitor (French Minitel Type)

CHARACTERISTICS

- Screen : 9" Monochrome
- Frame deflection yoke : 72 mH, 40 Ω, 220 mA peak-to-peak
- V_{CC} = + 25 V without flyback generator
- Frame flyback time : 1.2 ms
- Vertical frequency : 50 Hz (20 ms)
- Vertical free-running period : 24.5 ms
- Horizontal frequency : 15 625 Hz
- Capture range : ±5µs
- Holding range : ±10µs
- Input signal : composite video
- Dissipated power : 1.15 W
- Only one adjustment : vertical amplitude

Figure 28



- This is a low-cost application used in French Minitel type configurations and requires minimum number of additional components and adjustments. The input is a composite video signal at line frequency = 15 625 Hz and frame frequency of 50 Hz.
- The free-running horizontal frequency is determined by the component values of RC network on pin 9. Since no adjustment is available, precision components must be used to ensure correct synchronization :

[R = 35.7kΩ, 1% and C = 2.2nF, 2% for f_H = 15 625Hz]

The capture range is large enough to compensate for possible variations.

- Synchronization range of the vertical oscillator is quite large which consequently allows use of less accurate components :

[R = 910 kΩ, 5 % and C = 180 nF, 5 %]

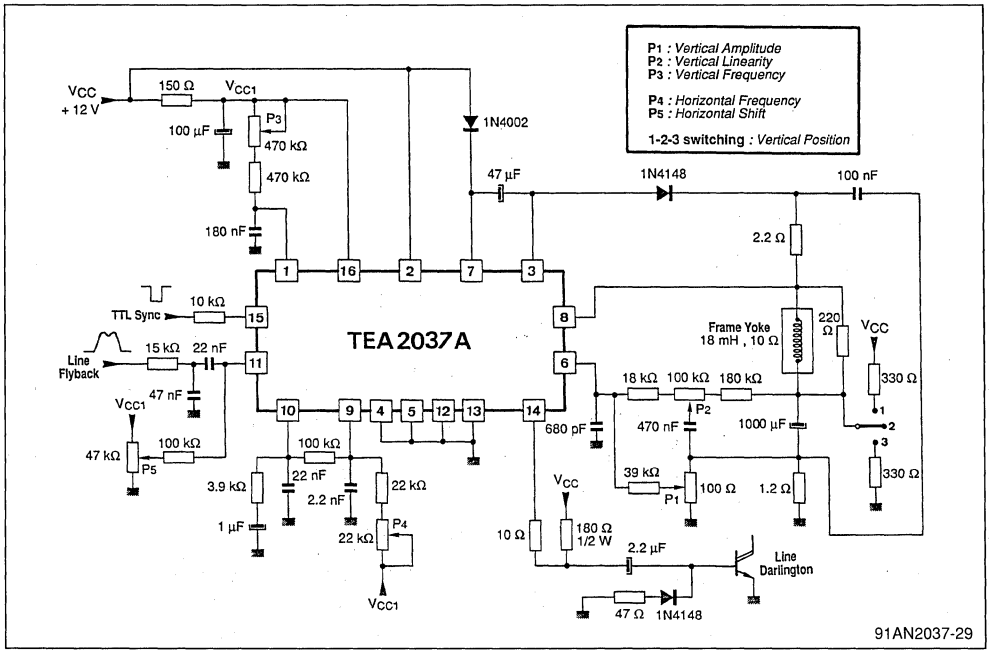
- Since the frame flyback time is short enough at supply voltage used here, the flyback generator is not used in this application.

III.1.2 - Monitor with geometry and frequency adjustments

CHARACTERISTICS

- Screen : 12" Colour
- Frame deflection yoke : 18 mH, 10Ω, 500 mA peak-to-peak
- V_{CC} = + 12V with flyback generator
- Frame flyback time : 0.7 ms
- Vertical frequency : 50/60 Hz
- Vertical free-running period : 23 ms (adjustable)
- Horizontal frequency : 15.7 kHz (adjustable)
- Capture range : = ±5µs
- Holding range : ±10µs
- Input signal : negative TTL sync (line + frame)
- Dissipated power : 0.9 W
- Adjustments :
  - Vertical amplitude
  - Vertical linearity
  - Vertical frequency
  - Horizontal frequency
  - Horizontal phase-shift

Figure 29

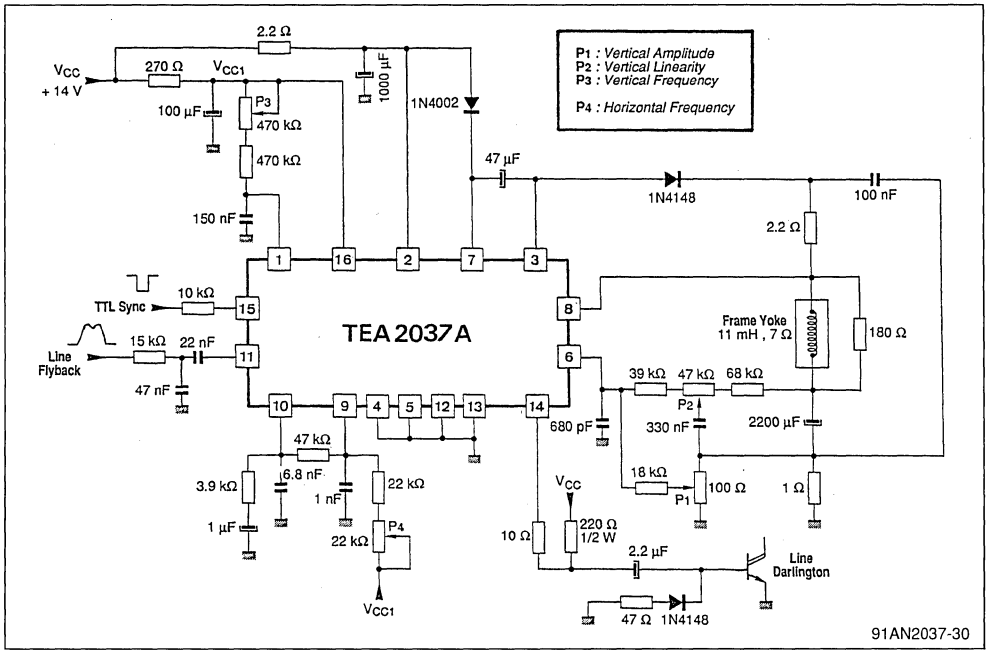


III.1.3 - High frequency monitor

CHARACTERISTICS

- Screen : 14" Colour
- Frame deflection yoke : 11 mH, 7 Ω, 750 mA peak-to-peak
- V_{CC} = + 14 V with flyback generator
- Frame flyback time : 0.6 ms
- Vertical frequency : 72 Hz
- Vertical free-running period : 16 ms (adjustable)
- Horizontal frequency : 35 kHz (adjustable)
- Line flyback time : 5.5µs
- Capture range : 5µs (@sync pulse = 4.7µs)
- Input signal : negative TTL sync (line + frame)
- Dissipated power : 1.4 W (heatsink required)
- Adjustments :
  - Vertical amplitude
  - Vertical linearity
  - Vertical frequency
  - Horizontal frequency

Figure 30

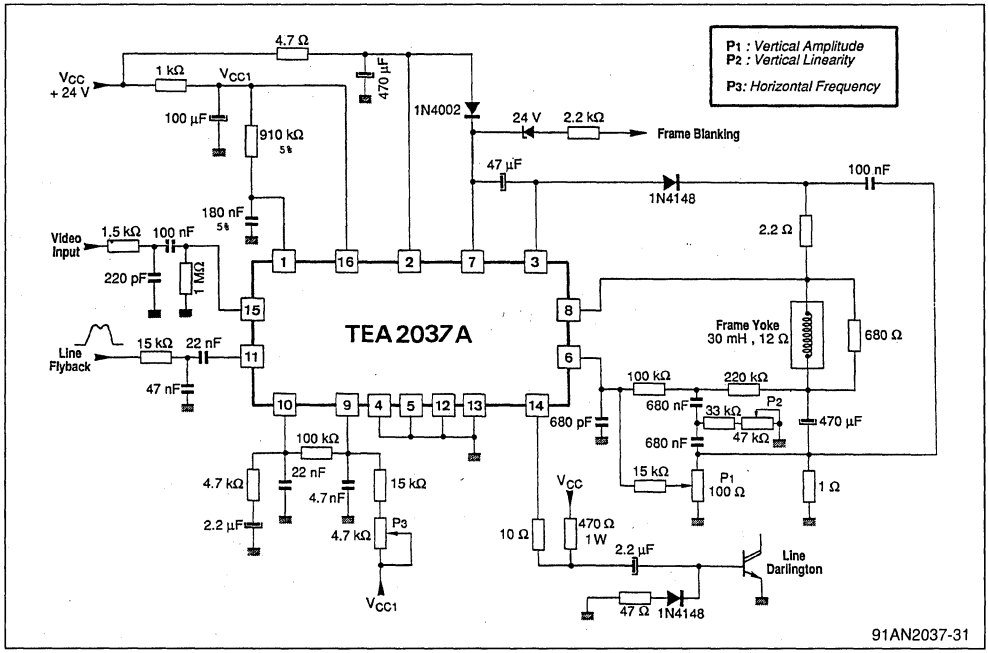


III.2 - Black & white TV application

CHARACTERISTICS

- Screen : 20" B & W 110°
- Frame yoke : 30mH, 12Ω, 850mA peak-to-peak
- V_{CC} = + 24 V with flyback generator
- Frame flyback time : 1ms
- Vertical frequency : 50Hz
- Vertical free-running period : 24.5 ms
- Horizontal frequency : 15 625 Hz (adjustable)
- Capture range : ±2 µs
- Holding range : ±4.5 µs
- Input signal : composite video
- Dissipated power : 2.3 W (10°C/W - heatsink required)
- Adjustments :
  - Vertical amplitude
  - Vertical linearity
  - Horizontal frequency

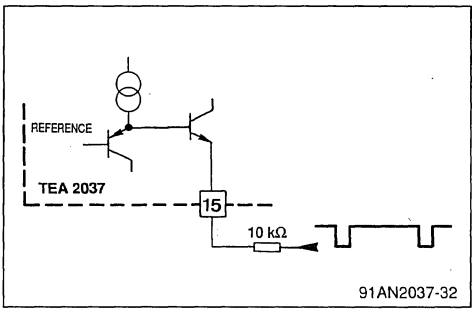
Figure 31



III.3 - Using composite TTL synchronization

Since the threshold level on input pin 15 is internally set at 1.6 V, the device can directly accept TTL signals.
However, a series resistor is required to limit the current sunk by the on-chip transistor (pin 15).

Figure 32



If composite sync signal is not available, line and frame sync signals can be recombined at circuit input as illustrated below.

Figure 33

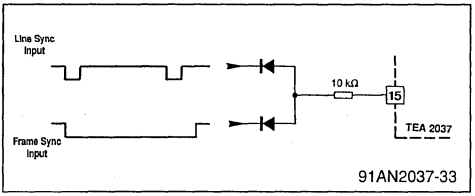
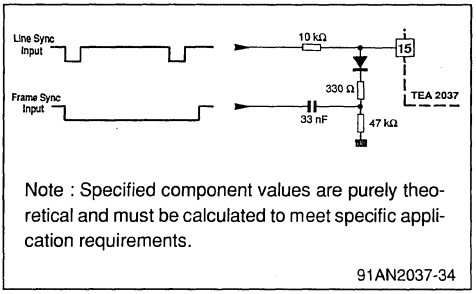


Figure 34 : Application example

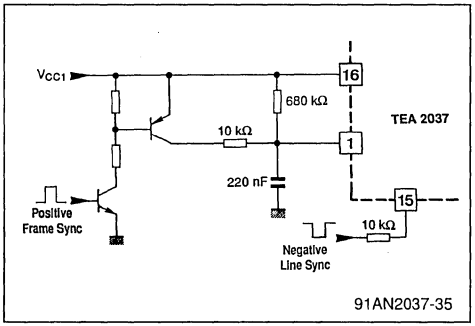


This arrangement is particularly interesting in applications where the available signals differ from those commonly used. An example is the case where the frame signal is of quite long duration (sometimes as long as frame blanking period). In such case, efficient synchronization can be achieved by differentiating the signal so that it will behave as a signal of only few lines duration which is the condition required for appropriate frame and line sync separation and also a picture without flag effect.

III.4 - Direct frame synchronization

The vertical scanning can be directly synchronized by the frame oscillator (pin 1) and without any need of using the synchronization input (pin 15).
Figure 35 illustrates an example :
In this case, only the line sync pulse is applied to pin 15.

Figure 35



III.5 - Constant amplitude 50/60 Hz switching

In applications requiring 50/60 Hz standard switching feature, the arrangement shown below allows to maintain the amplitude of the oscillator sawtooth (pin 1) constant thus yielding uniform vertical scanning.

Figure 36

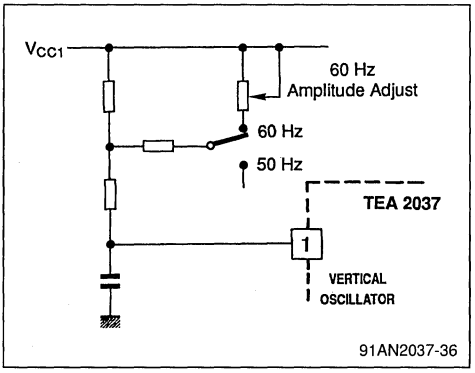
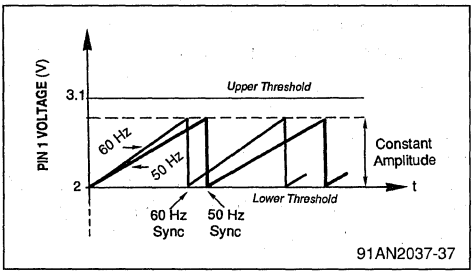
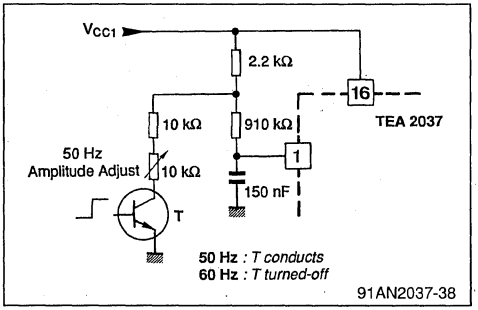


Figure 37



A practical application configuration is illustrated below.

Figure 38



III.6 - Modifying the line output duration

The line output pulse duration is determined by two internally set threshold levels. This interval can be altered by modifying the charge current of the line oscillator (pin 9)

Figure 39

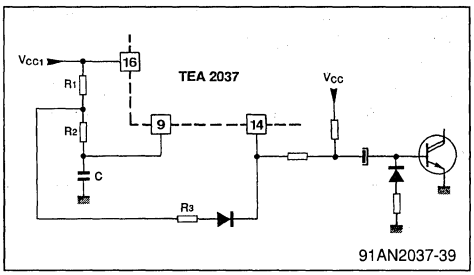
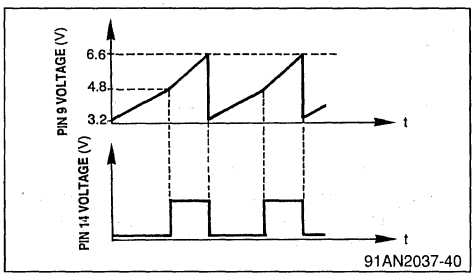


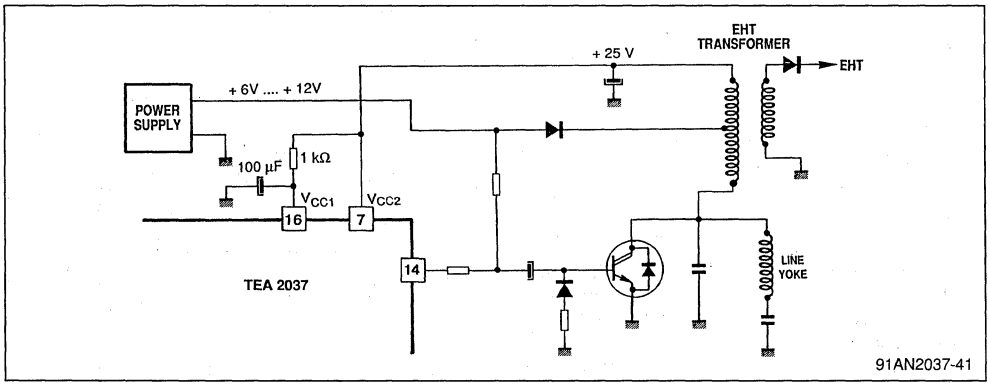
Figure 40



III.7 - Starting the TEA2037 from a +6V power supply

The line oscillator of TEA2037 is capable of starting at a low supply voltage (< 6V). The period of oscillation is practically the same as at nominal operation. It is thus possible to initiate the line scanning at a reduced supply voltage (e.g. +6V) and then supply the overall configuration by the power available on the line transformer.

Figure 41



IV - DESIGN CONSIDERATIONS

IV.1 - Precautions for interlaced scanning

- The links interconnecting the ground terminals of V_{CC} and V_{CC1} power supplies, as well as those of device decoupling capacitors, must be kept to as short as possible
- A high value decoupling capacitor can be used for V_{CC} supply, provided that a good quality low series resistance capacitor is employed. Interlacing is very sensitive to decoupling quality. The value of the decoupling capacitor can vary from 22µF to 100µF.
- The interconnecting links between the frame oscillator capacitor, the line oscillator capacitor and TEA2037 grounds must be kept to as short as possible.

Perfect line and frame synchronization is achieved by observing the above guidelines and recommendations.

IV.2 - Printed circuit board layout

- The usual precautions observed in design of TV timebase pc boards must be employed
- The line output stage handles high amounts of voltage and current. Components employed must therefore be appropriately rated, the width of and the clearance between the wiring tracks should be carefully selected. All connections must be as short as possible and all signals at the line frequency gathered at this section.
- The supply to the frame scanning section of the circuit must not be influenced by the horizontal scanning function, particularly when interlaced scanning is used.
- Generally speaking, interactions on the pc board between the high-gain/low-level and the high-current sections of the output stages must be minimized by as much as possible.
- As indicated in previous chapters, the four center pins of the device must be earthed. The pad used for this purpose must be as large as possible since it acts as the heatsink for the device. A cruciform pad underlying the circuit should be employed.
- There should be a single connection to the chassis earth terminal.

THERMAL MANAGEMENT

THE POWER DIP (16+2+2, 12+3+3) PACKAGES

by R. Tiziani

INTRODUCTION

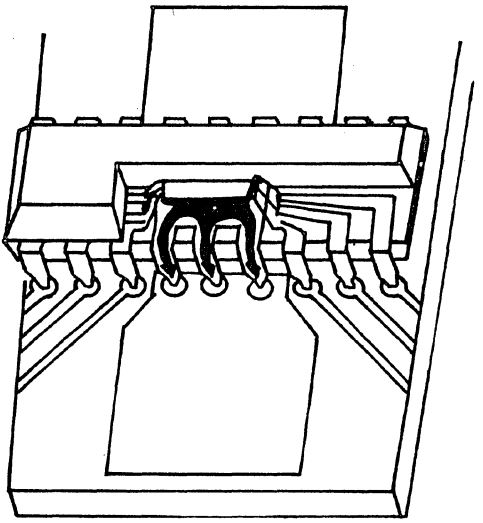
This Application Note is aimed to give a complete thermal characterization of the (16+2+2) power DIP (modified 20 lead DIP with 4 heat transfer leads) and of the (12+3+3) power DIP (modified 18 lead DIP with 6 heat transfer leads) in association with thermal modules integrated on the PCB.

Characterization is performed according with recomendations included in G32-86 SEMI guideline, by means of a dedicated test pattern developed by SGS-THOMSON. It refers to:

1. Junction to pin thermal resistance Rth(j-p)
2. Junction to ambient thermal resistance Rth(j-a)
3. Thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techiniques.

Figure 1. POWER DIP application on PC board



Experimental conditions

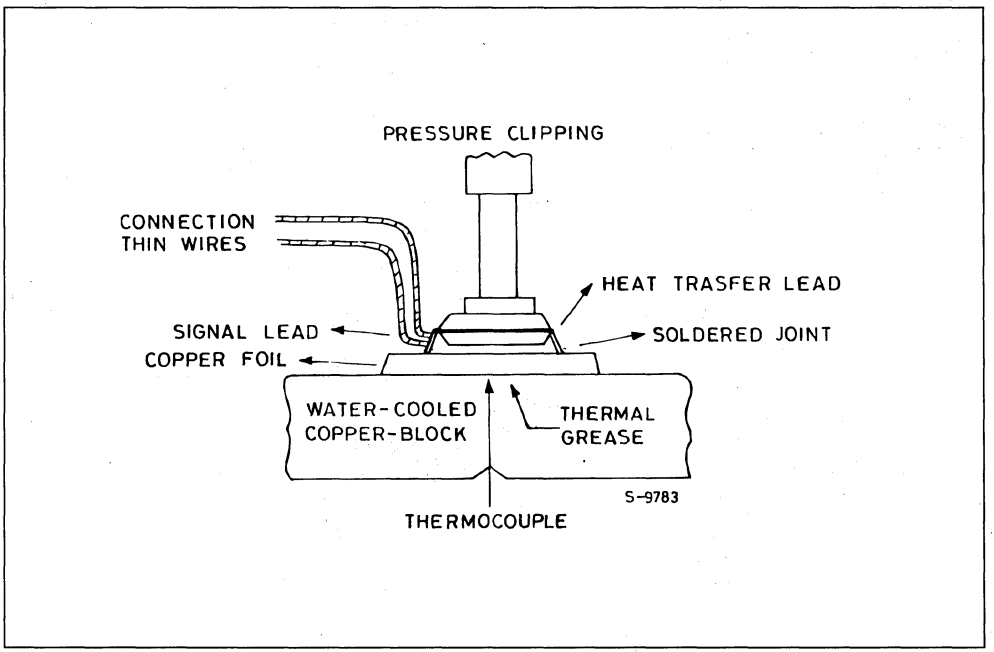
The thermal evaluation was performed by means of the test pattern P638, which is a 80x80 *mils*^{2} die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 3000 *mils*^{2}, with a power capability of 20 W. Measurement method is described in Appendix. A.

Samples with the indicated characteristics were prepared:

Package	DIP (16+2+2)	DIP (12+3+3)
Frame Material	Copper	Copper
Frame Thickness	0.4*mm*	0.4*mm*
Frame Thermal Conductivity	3.9*W/cm*°C	3.9*W/cm*°C

Measurement of junction to pin thermal resistance Rth(j-p) is performed by holding the package (with the heat transfer leads soldered on a copper plate) against a water cooled heat sink, according with fig. 2. A thermocouple placed in contact with the plate measures the reference temperature.
For junction to ambient thermal resistance Rth(j-a) the samples are suspended horizontally in a one cubic foot box, to prevent drafts.
The effect of "on board" external heat sinks shown in fig. 1 is quantified, using a test board which has two 4 x 4 cm^2 dissipating areas, one of each side of the package. These areas are mechanically reduced in order to study the effect of their size on thermal performance.
The measurement circuit shown in fig. A3 is used for all of the thermal evaluations.

Figure 2. Measurement of Rth(j-p)



JUNCTION TO PIN THERMAL RESISTANCE

The dependance of Rth(j-p) on the dissipated power is negligeable compared to the absolute value: starting from 1 Watt to 10 Watts the Rth(j-p) increases of about 0.5C/W due to the lowering of silicon thermal conductivity with the increasing of temperature. An important contribution to Rth(j-p) is given by the silicon die and in fig. 3,4 is showed the relationship between Rth(j-p) and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

In the figures two curves area reported: the lower one is referring the Rth(j-p) measured at the pin stand-off, the upper one is referring to the Rth(j-p) measures at 1.5 mm from the pin stand-off (1.5 mm is the typical thickness of FR4 board).

The upper curve must be used for the application in which the heat sink is placed in the lower side of PCB and the lower curve must be used when the heat sink is placed on the upper side of PCB.

Figure 3 - POWER DIP 16+2+2 $R_{th(j-p)}$ vs on die dissipating area

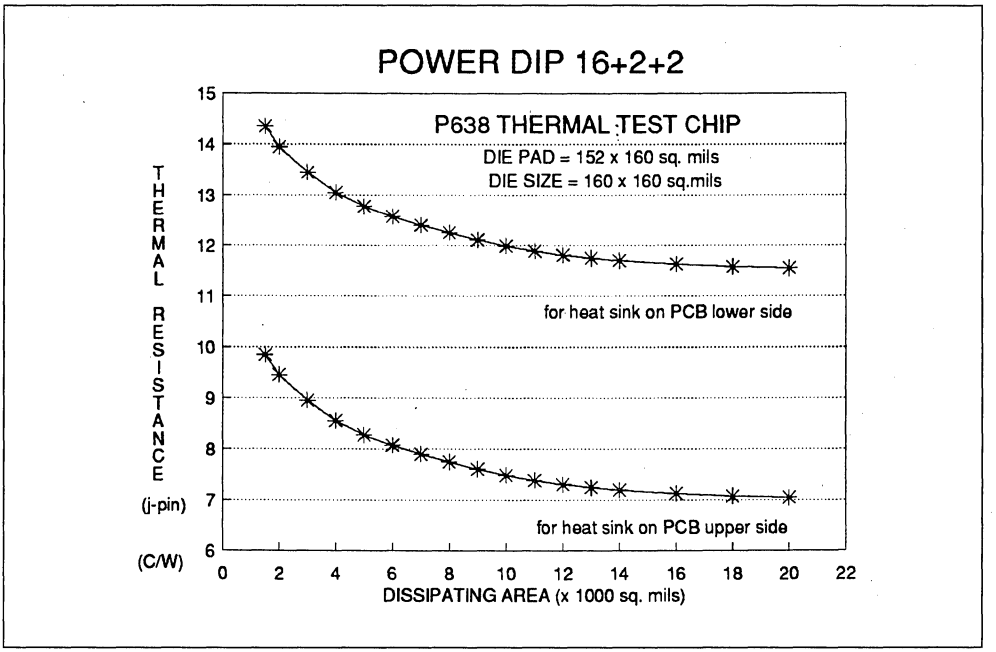
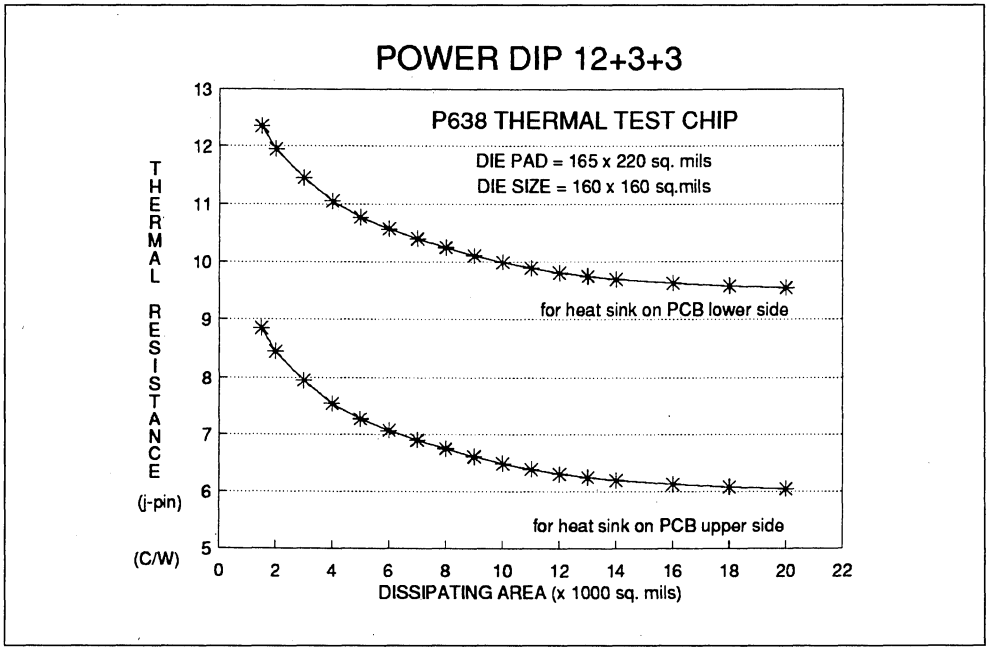


Figure 4 - POWER DIP 12+3+3 $R_{th(j-p)}$ vs on die dissipating area



JUNCTION TO AMBIENT THERMAL RESISTANCE

Fig. 5,6 give the junction to ambient thermal resistance Rth(j-a) of the package vs dissipated power; it evidences the effect of the board in improving the exchange of the heat towards the ambient. The upper curve refers to samples suspended in air, with eight thin wire connecting the dissipating transistors and the sensing diode. The lower curve is obtained with a very large heat sink (35 µm thick 4 x 4cm^2 copper area for each side) while the other curve refers the packages mounted on board with no heat sink.

Rth is decreasing when power is increased, due to a better heat transfer efficiency at higher temperature.

Figure 5 - $R_{th(j-a)}$ of DIP (16+2+2) package vs dissipated power

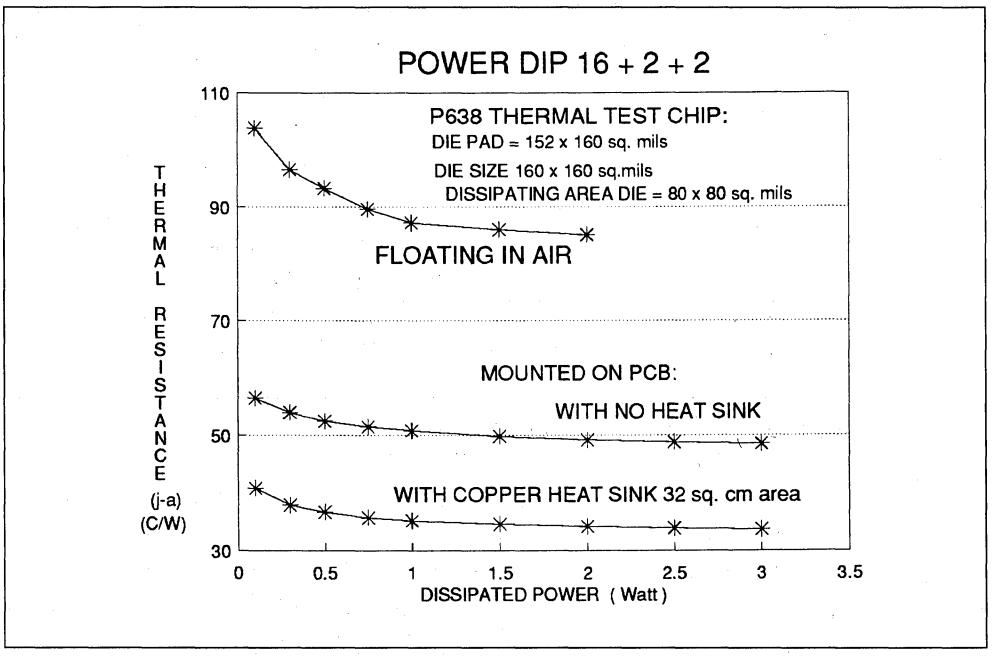
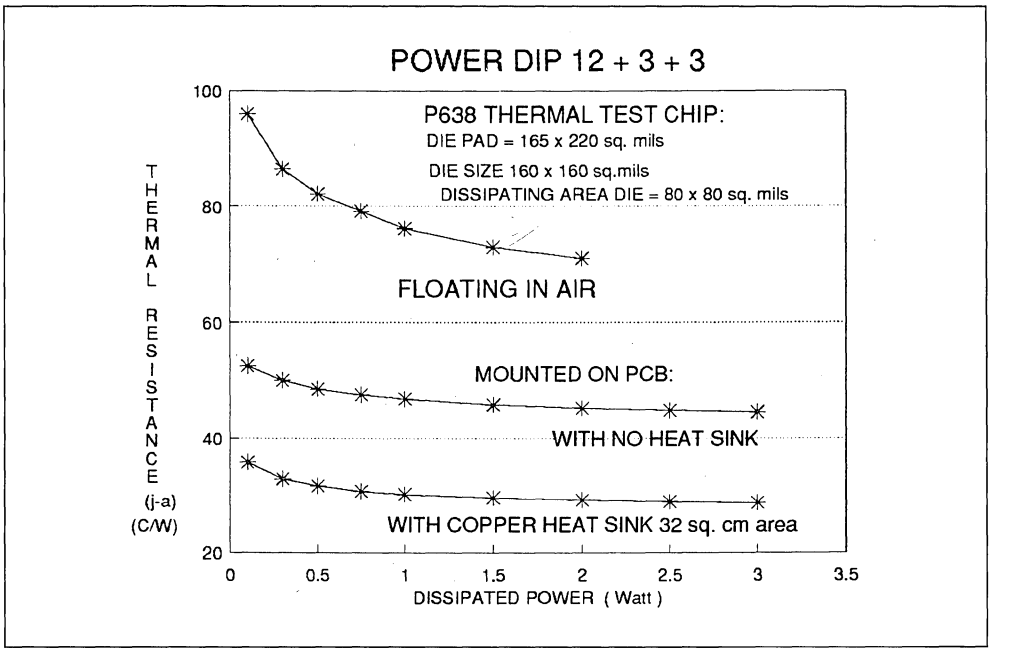


Figure 6 - Rth(j-a) of DIP (12+3+3) package vs. dissipated power



The effect of on board heat sinks with different size is summarized in fig. 8,9; thermal resistance in given vs the side l of the two thick copper squares, obtained in the lower side of the test board and dedicated to heat dissipation (see fig. 7 for test board). Standard thickness of 35µm was used for the characterization as the most part of PCb application but a large improvement can be easily obtained with a thicker copper heat sink on board: 70µm and 105µm (respectively 2 and 3 oz.) are strongly increasing the thermal performances of the considered POWER DIP application. These solutions can be attractive for low complex PC board with a cost saving in avoiding large external heat sink or forced ventilation.

Figure 7 - Test board with two "on board" square heat sinks vs side l

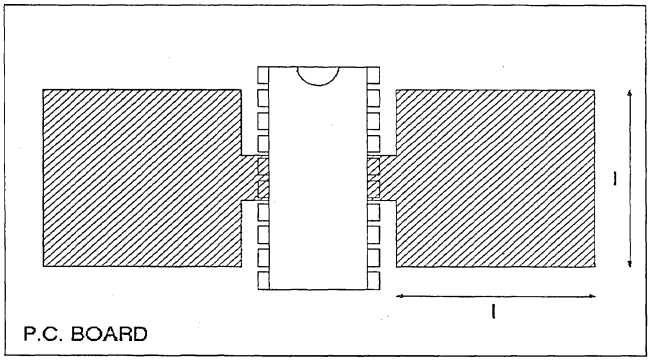


Figure 8 - $R_{th(j-a)}$ of POWER DIP 16+2+2 vs side l for heat sink on the PCB lower side

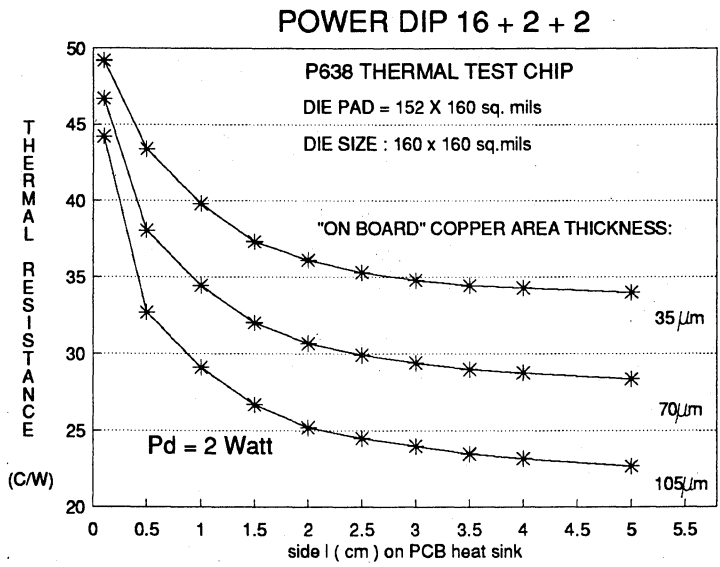
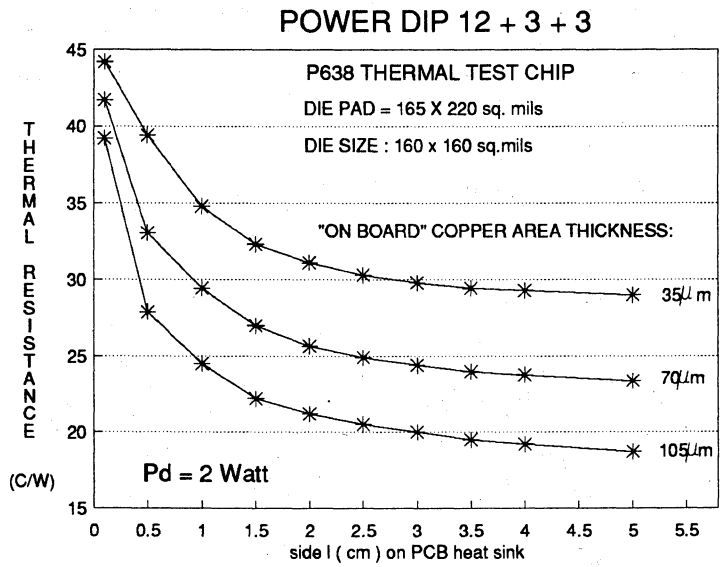


Figure 9 - $R_{th(j-a)}$ of POWER DIP 12+3+3 vs side l for heat sink on the PCB lower side



TRANSIENT THERMAL RESISTANCE

The effect of single pulse of different length and height, is shown in fig. 10,11 for POWER DIP 16+2+2 and 12+3+3. Thicker copper heat sink on PCB is effective also for short pulse width (less 1 sec.). Due to a significant thermal capacitance a correspondingly long risetime, single pulse up to 10W can be delivered to the system for 1s with acceptable junction temperature increase.

Figure 10 - DIP 16+2+2 Transient thermal resistance for single pulses

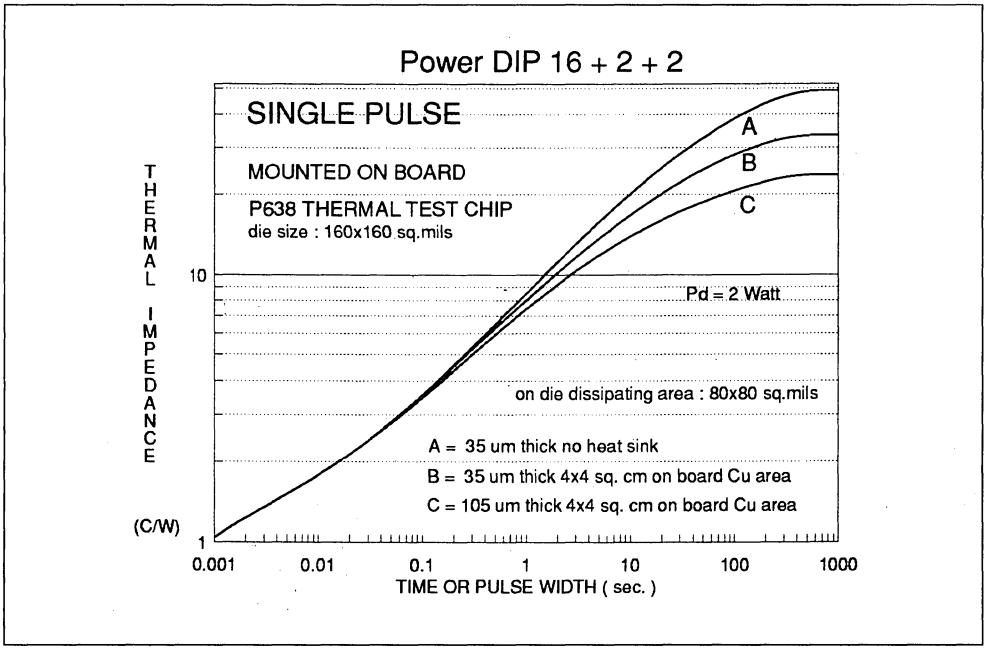
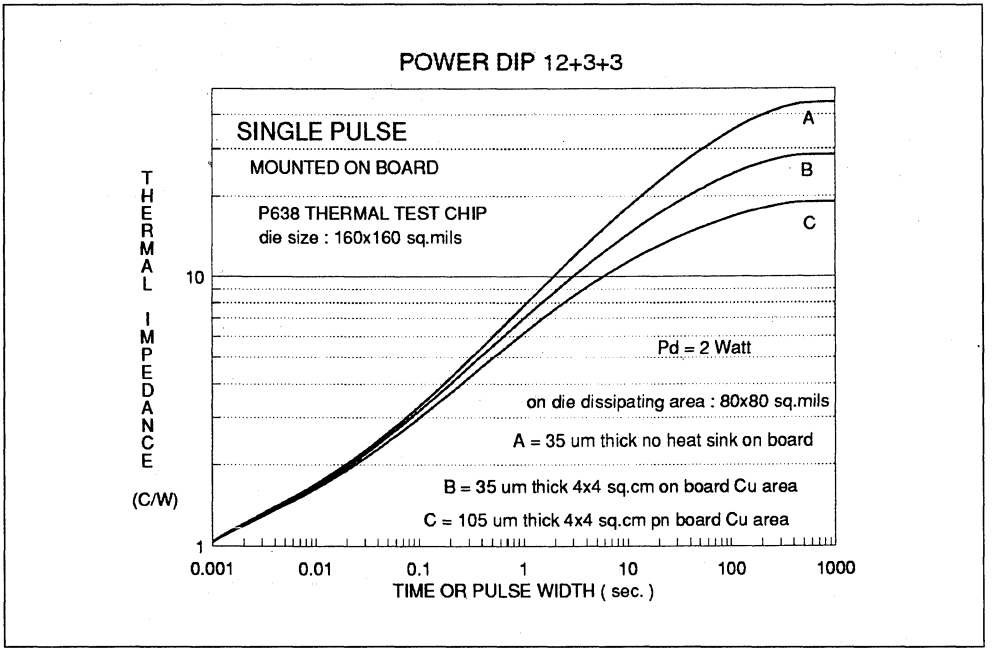


Figure 11 - DIP 12+3+3 Transient thermal resistance for single pulses



Repeatition of pulses with defined Pd, period and duty cycle DC (ratio between pulse length and signal period), gives rise to an average temperature increase:

$\Delta T_{avg} = Rth \times Pd_{avg} = Rth \times Pd \times DC$

Junction temperature is oscillating about the mean value as qualitatively shown in fig. 12. The transient thermal resistance corresponding to the upper limit (peak transient thermal resistance) is reported in fig. 13,14 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

Figure 12

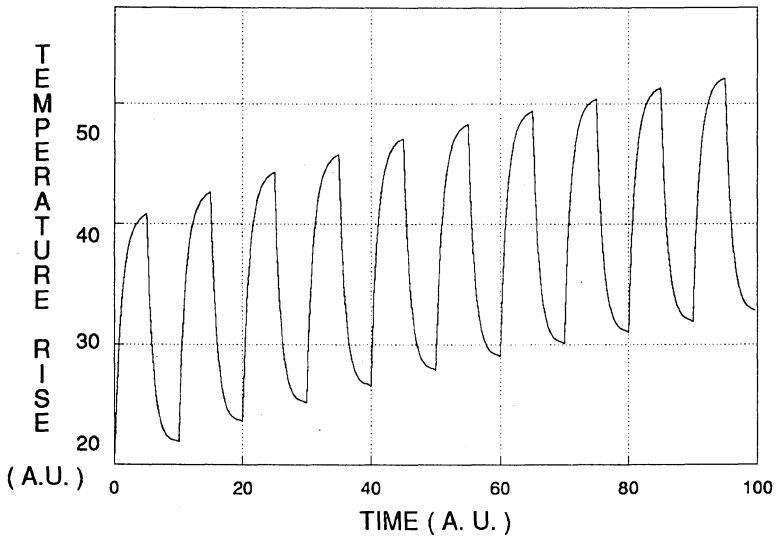


Figure 13 - Peak Transient Thermal resistance of DIP (16+2+2)

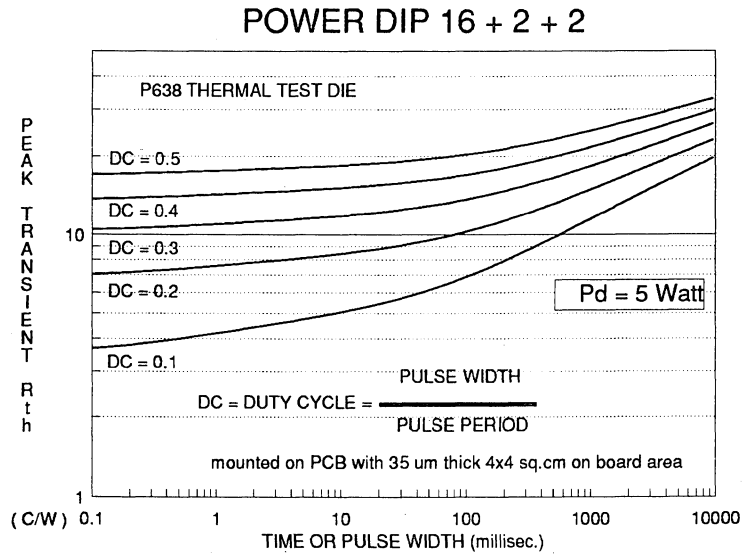
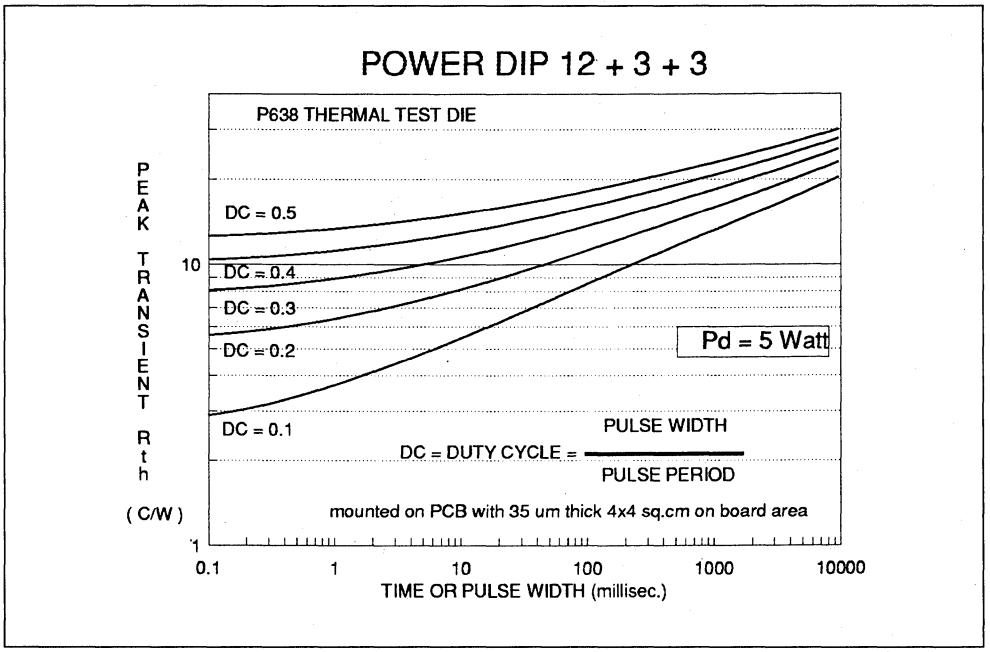


Figure 14 - Peak transient thermal resistance of DIP (12+3+3)



APPENDIX

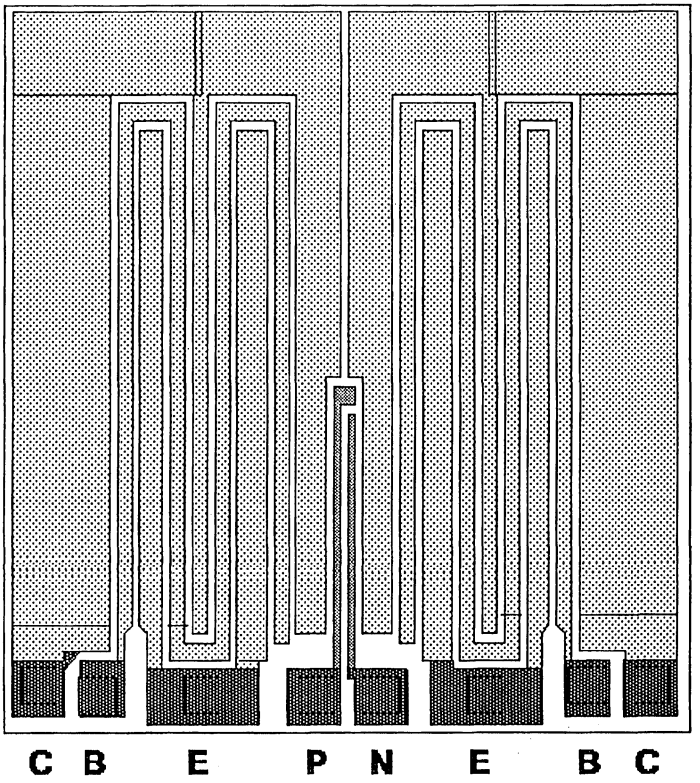
TEST PATTER P638

For thermal measurement

Test patterm P638 is designed for thermal measurement following SEMI guideline G32 (see SEMI Standard Handbook, 1986/87).

It has two bipolar power transistor with area of about 3000 sq. mils and one sensing diode (see Fig. A1). The lay-out is optimized in order to have a uniform temperature, once the two transistors are powered: the sensing diode is placed at the center of this area.

Figure A1 - P638 test pattern



Die size of single unit is 80 x 80 sq. mils; wafer thickness is about 280 microns.

The relationship between the forward voltage V_f of the diode at a constant current of **100** μA and the temperature is linear, with a coefficent **K = 1.85 mV/C** (see Fig. A2).

Therefore changes ΔT_j in junction temperature of the dissipating element formed by the two transistors, can be easily obtained from the diode forward voltage drop:

$$\Delta T_j = \frac{(V_{f1} - V_{f2})}{K}$$

(V_{f2} is the diode forward voltage at ambient temperature and V_{f1} is the voltage when the transistors are dissipating).

For thermal resistance evaluation the measurement circuit is showed in Fig. A3.

Figure A2 - Calibration curve (sensig diode).

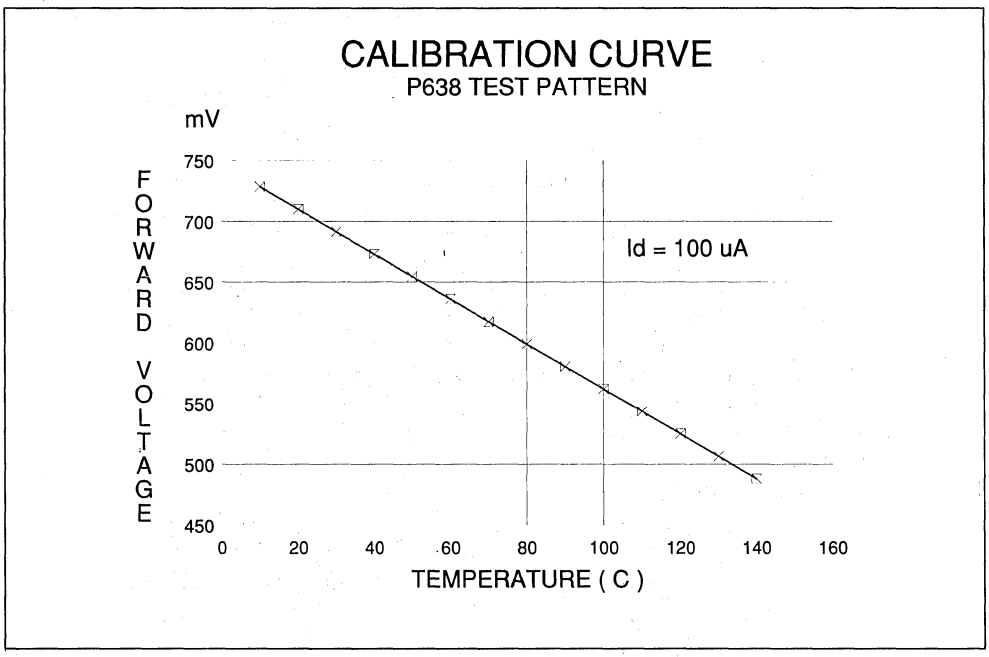
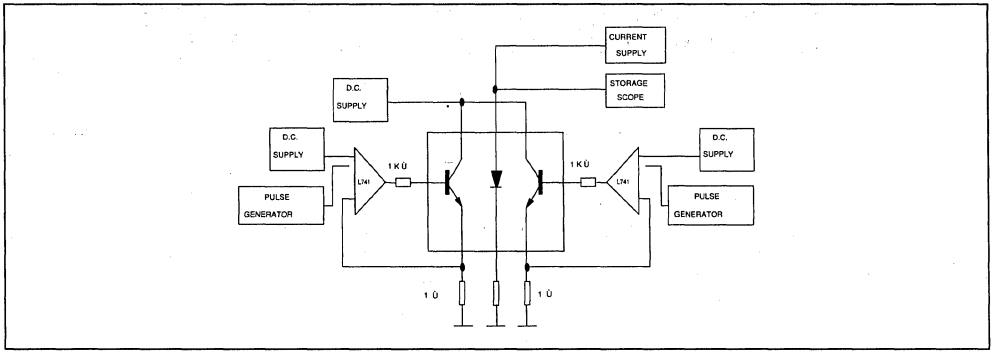


Figure A3 - Measurement System



Tipical conditions are:

P_d (Watt)	V_{ce} (Volt)	I_c (mA)
0.1	1.0	100
0.2	2.0	100
0.3	3.0	100
0.5	5.0	100
0.75	7.5	100
1.0	10.0	100
1.5	15.0	100
2.0	20.0	100
3.0	15.0	200
5.0	25.0	200
10.0	25.0	400

Each transistor is able to dissipate up to 10 Watt due to presence of second breakdown.

DESIGNING WITH THERMAL IMPEDANCE

BY T.HOPKINS, C.COGNETTI, R.TIZIANI

REPRINT FROM "SEMITHERM PROCEDINGS" S.DIEGO (U.S.A.) 1988.

ABSTRACT

Power switching techniques used in many modern control systems are characterized by single or repetitive power pulses, which can reach several hundred watts each. In these applications where the pulse width is often limited to a few milleseconds, cost effective thermal design considers the effect of thermal capacitance. When this thermal capacitance is large enought, it can limit the junction temperature to within the ratings of the device even in the presence of high dissipation peaks. This paper discusses thermal impedance and the main parameters influencing it. Empirical measurements of the thermal impedance of some standard plastic packages showing the effective thermal impedance under pulsed conditions are also presented.

INTRODUCTION

Power switching applications are becoming very common in many industrial, computer and automotive ICs. In these applications, such as switching power supplies and PWM inductive load drivers, power dissipation is limited to short times, with single or repeated pulses. The normal description of the thermal performance of an IC package, Rth(j -a) (junction to ambient thermal resistance), is of little help in these pulsed applications and leads to a redundant and expensive thermal design.

This paper will discuss the thermal impedance and the main factors influencing it in plastic semiconductor packages. Experimental evaluations of the thermal performance of small signal, medium power, and high power packages wil be presented as case examples. The effects of the thermal capacitance of the packages when dealing with low duty cycle power dissipation will be presented and evaluated in each of the example cases.

THERMAL IMPEDANCE MODEL FOR PLASTIC PACKAGES

The complete thermal impedance of a device can be modeled by combining two elements, the thermal resistance and the thermal capacitance.

The thermal resistance, Rth, quantifies the capability of a given thermal path to transfer heat. The general definition of resistance of the thermal path, which includes the three different modes of heat dissipation (conduction, convection and radiation), is the ratio between the temperature increase above the reference and the heat flow, DP, and is given by the equation :

$$R_{th} = \frac{\Delta T}{\Delta P} = \frac{\Delta T}{\frac{\Delta Q}{\Delta t}}$$

Where : ΔQ = heat
Δt = time

Thermal capacitance, C_{th}, is a measure of the capability of accumulating heat, like a capacitor accumulates a charge. For a given structural element, C_{th} depends on the specific heat, c, volume V, and density d, according to the relationship :

$$C_{th} = c\ d\ V$$

The resulting temperature increase when the element has accumulated the heat Q, is given by the equation :

$$\Delta T = \Delta Q / C_{th}$$

The electrical analogy of the thermal behaviour for a given application consisting of an active device, package, printed circuit board, external heat sink and external ambient is a chain of RC cells, each having a characteristic time constant :

$$\tau = RC$$

To show how each cell contributes to the thermal impedance of the finished device consider the simplified example shown in figure 1. The example device consists of a dissipating element (integrated circuit) soldered on a copper frame surrounded by a plastic compound with no external heat sink. Its equivalent electrical circuit is shown in figure 2.

The first cell, shown in figure 2, represents the thermal characteristics of the silicon itself and is characterized by the small volume with a correspondingly low thermal capacitance, in the order of a few mJ/C. The thermal resistance between the junction and

the silicon/slug interface is of about 0.2 to 2 °C/W, depending on die size and on the size of the dissipating elements existing on the silicon. The time constant of this cell is typically in the order of a few milliseconds.

The second cell represents the good conductive path from the silicon/frame interface to the frame periphery. In power packages, where the die is often soldered directly to the external tab of the package, the thermal capacitance can be large. The time constant for this cell is in the order of seconds.

From this point, heat is transferred by conduction to the molded block of the package, with a large thermal resistance and capacitance. The time constant of the third cell is in the order of hundreds of seconds.

After the plastic has heated, convection and radiation to the ambient starts. Since a negligible capacitance is associated with this phase, it is represented by a purely resistive element.

When power is switched on, the junction temperature increase is ruled by the heat accumulation in the cells, each following its own time constant according with the equation :

$$\Delta T = R_{th}\, P_d\, [1 - e^{(t/\tau)}]$$

The steady state junction temperature, T_j, is a function of the $R_{th\,(j\ a)}$ of the system, but the temperature increase is dominated by thermal impedance in the transient phase, as is the case in switching applications.

A simplified example of how the time constants of each cell contribute to the temperature rise is shown in figure 3 where the contribution of the cells of figure 2 is exaggerated for a better understanding.

When working with actual packages, it is observed that the last two sections of the equivalent circuit are not as simple as in this model and possible changes will be discussed later. However, with switching times shorter than few seconds, the model is sufficient for most situations.

Figure 1 : Simplified Package Outline.

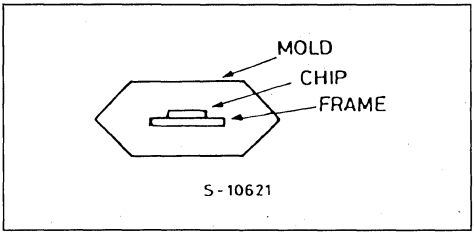


Figure 2 : Equivalent Thermal Circuit of Simplified.

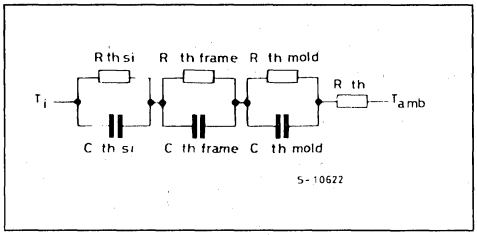
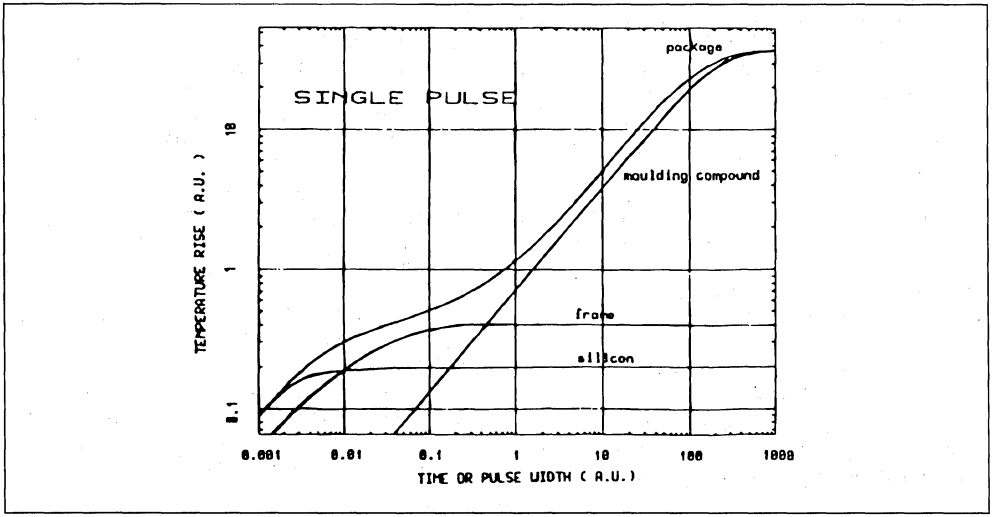


Figure 3 : Time Constant Contribution of Each Thermal Cell (qualitative example).



EXPERIMENTAL MEASUREMENTS

When thermal measurements on plastic packages are performed, the first consideration is the lack of a standard method. At present, only draft specifications exist, proposed last year and not yet standardized (1).

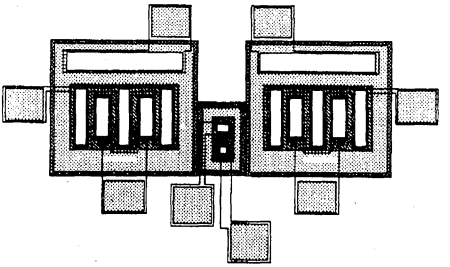
The experimental method used internally for evaluations since 1984 has anticipated these preliminary recomendations to some extent, as it is based on test patterns having, as dissipating element, two power transistors and, as measurement element, a sensing diode placed in the thermal plateau arising when the transistors are biased in parallel.

The method used has been presented elsewhere (2) for the pattern P432 (shown in figure 4), which uses two small (1000 sq mils) bipolar power transistors and has a maximum DC power capability of 40 W (limited by second breakdown of the dissipating elements).

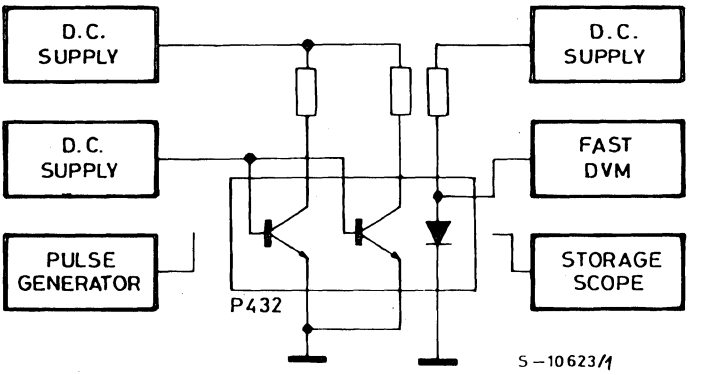
A similar methodology was followed with the new H029 pattern, based on two D-Mos transistors (3) having a total size of 17.000 sq mils and a DC power capability of 300 W on an infinite heat sink at room temperature (limited by thermal resistance and by max operating temperature of the plastics).

Figure 4.

a) P432 Test Die



b) P432 Measurement System

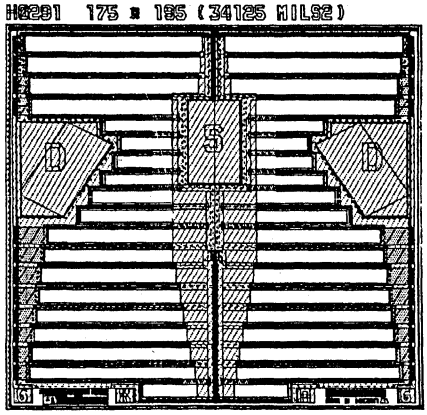


Using the thermal evaluation die, four sets of measurements were performed on an assortment of insertion and surface mount packages produced by SGS-Thomson Microelectronics. The complete characterization is available elsewhere (4). The four measurements taken were :

1) Junction to Case Thermal Resistance (Power Packages)
2) Junction to Ambient Thermal Resistance
3) Transient Thermal Impedance (Single Pulse)
4) Peak Transient Thermal Impedance (Repeated Pulses)

Figure 5.

a) H029 Test Die



b) H029 Measurement System

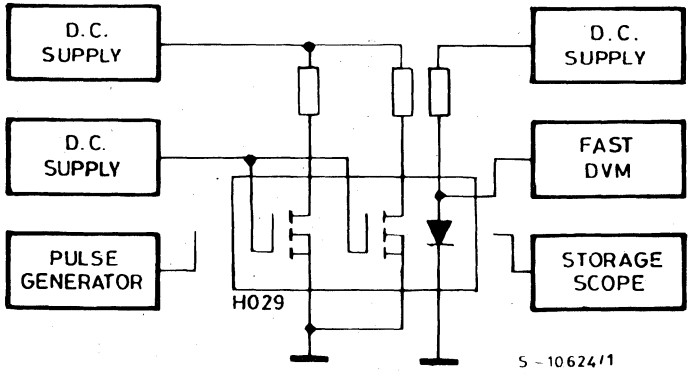
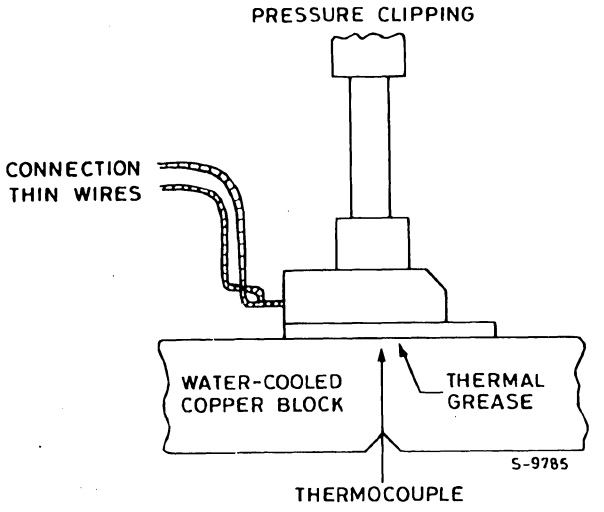


Figure 6 : Set-up for $R_{th\ (j-c)}$ Measurement.

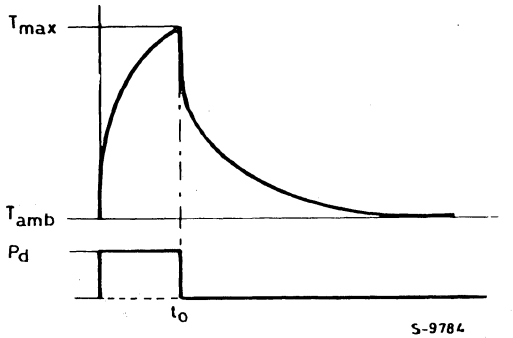


The junction to case thermal resistance measurements were taken using the well known setup shown in figure 6 where the power device is clamped against a large mass of controlled temperature.

The junction to ambient thermal resistance in still air, was measured with the package soldered on standard test boards, described later, and suspensed in 1 cubic foot box, to prevent air movement.

The single pulse transient thermal impedance was measured in still air by applying a single power pulse of duration t_0 to the device. The exponential temperature rise in response to the power pulse is shown qualitetively in figure 7. In the presence of one single power pulse the temperature, ΔT_{max}, reached at time t_0, is lower than the steady state temperature calculated from the junction to ambient thermal resistance. The transient thermal impedance R_o, is obtained from the ratio $\Delta T_{max}/Pd$.

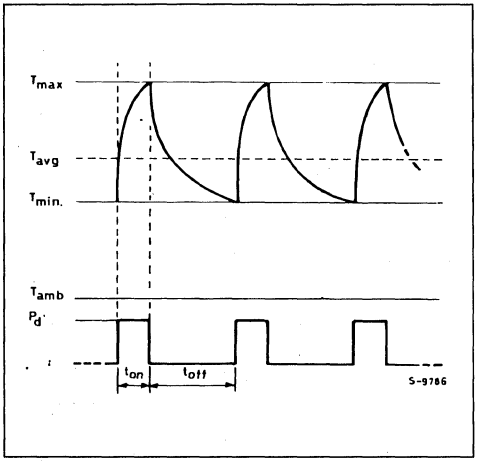
Figure 7 : Transient Thermal Response for a Single Pulse.



The peak transient thermal impedance for a series of repetitive pulses was measured by applying a string of power pulses to the device in free air. When power pulses of the same height, P_d, are repeated with a given duty cycle, DC, and the pulse length, t_p, is shorter than the total time constant of the system, the train of pulses is seen as a contiuous source with mean power level given by the equation :

$$P_{davg} = P_d \, DC$$

Figure 8 : Transient Thermal Response for Repetitive Pulses.



On the other hand, the silicon die has a thermal time constant of 1 to 2 ms and the die temperature is able to follow frequencies of some kHz. The result is that T_j oscillates about the average value :

$$\Delta T_{javg} = R_{th} \, P_{davg}$$

The resulting die temperature excursions are shown qualitatively in figure 8. The peak thermal impedance, R_{thp}, corresponding to the peak temperature, DT_{max}, at the equilibrium can be defined :

$$R_{thp} = \Delta T_{max}/P_d = F\,(t_p, DC)$$

The value of R_{thp} is a function of pulse width and duty cycle. Knowledge of R_{thp} is very important to avoid a peak temperature higher than specified values (usually 150°C).

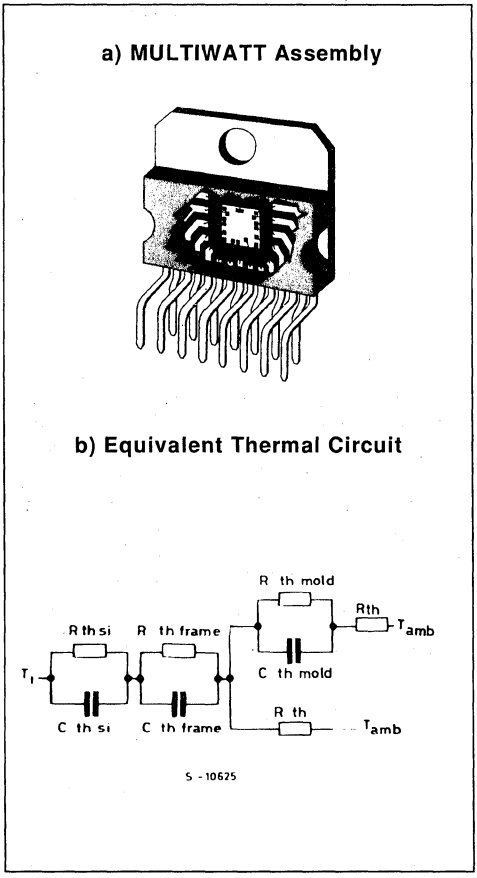
EXPERIMENTAL RESULTS

The experimental measurements taken on several of the packages tested are summarized in the following sections.

MULTIWATT PACKAGE

The MULTIWATT (R) package, shown in figure 9a, is a multileaded power package in which the die is attached directly to the tab of package using a soft solder (Pb/Sn) die attach. The tab of the package is a 1.5 mm thick copper alloy slug. The thermal model of the MULTIWATT, shown in figure 9b, is not much different from that shown in figure 2. The main difference being that when heat reaches the edge of the slug, two parallel paths are possible ; conduction towards the molding compound, and convection and radiation towards the ambient. After a given time, convection and radiation taked place from the plastic.

Figure 9.



Using the two test die, the measured junction to case thermal resistance is :

P432 $R_{th\,(j\,c)} = 2°C/W$

H029 $R_{th\,(j\,c)} = 0.4°C/W$

The measured time constant is approximately 1 ms for each of the two test patterns, but the two devices have a different steady state temperature rise.

The second cell shown in figure 9 is dominated by the large thermal mass of the slug. The thermal resistance of the slug, R_{thslug} is about 1 °C/W and the thermal time constant of the slug is in the order of 1 second.

The third RC cell in the model has a long time constant due to the mass of the plastic molding and its low thermal conductivity. For this cell the steady state is reached after hundreds of seconds.

For the MULTIWATT the DC thermal resistance of the package in free air, $R_{th\ j\ a}$, is 36 °C/W with the P432 die and 34.5°C/W with the H029 die.

Figure 10 shows the single pulse transient thermal impedance for the MULTIWATT with both the P432 and H029 test die. As can be seen on the graph, the package is capable of high dissipation for short periods of time. For a die like the H029 the power device is capable of 700 to 800 W for pulse widths in the range of 1 to 10 ms. For times up to a few seconds the effective thermal resistance for a single pulse is still in the range of 1 to 3 °C/W.

The peak transient thermal impedance for the MULTIWATT package containing the P432 die in free air is shown in figure 11.

POWER DIP PACKAGE

The power DIP package is a derivative of standard small signal DIP packages with a number of leads connected to the die pad for heat transfer to external heat sinks. With this technique low cost heat sinks can be integrated on the printed circuit board as shown in figure 12a. The thermal model of the power DIP, shown in figure 12b accounts for the external heat sink on the circuit board by adding a second RC cell in parallel with the cell corresponding to the molding compound.

In this model, the second cell has a shorter time constant than for the MULTIWATT package, due in large part to the smaller quantity of copper in the frame (the frame thickness is 0.4 mm compared to 1.5 mm). Thus the capacitance is reduced and the resistance increased.

The increased thermal impedance due to the frame can partially be compensated by a better thermal exchange to the ambient by adding copper to the heat sink on the board. The DC thermal resistance between the junction and ambient can be reduced to the same range as the MULTIWATT package in free air, as shown in figure 13.

Figure 10 : Transient Thermal Response MULTIWATT Package.

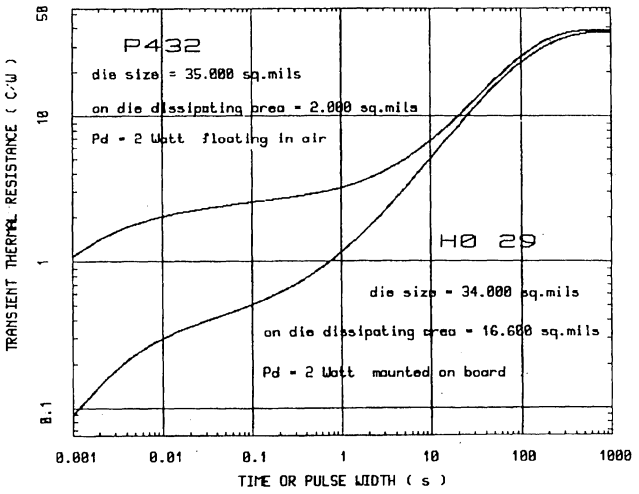


Figure 11 : Peak Thermal Resistance MULTIWATT Package.

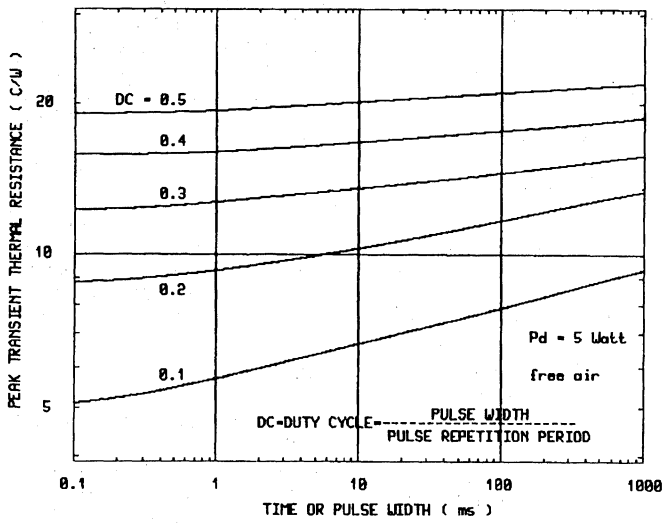
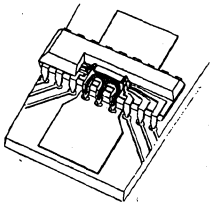
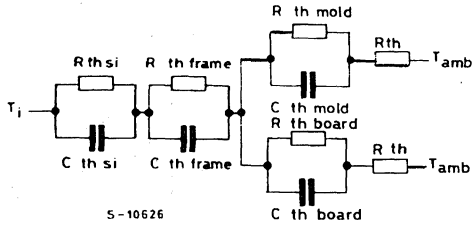


Figure 12.

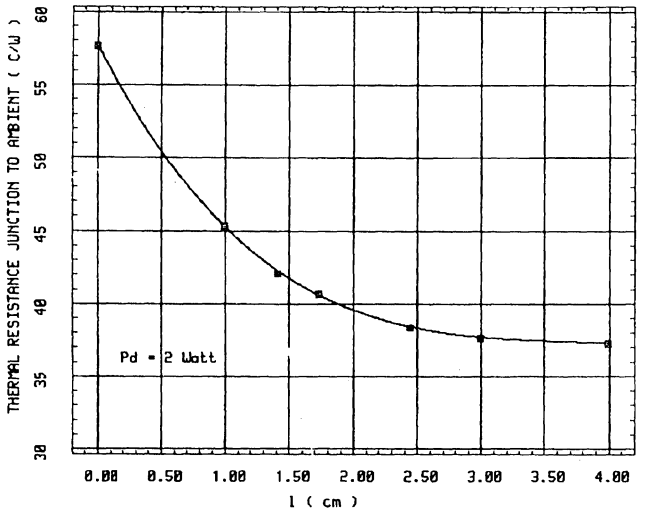


a) Power DIP Package



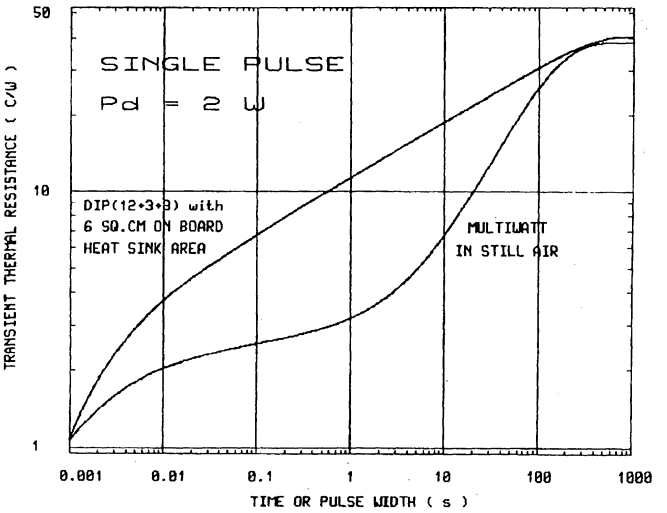
b) Equivalent Thermal Circuit

Figure 13 : Rth (j – a) vs. PCB Heat Sink Size 12 + 3 + 3 Power Dip.



As a comparison, figure 14 compares the thermal performance of the power DIP and the MULTIWATT package. It is clearly seen that even though the DC thermal resistance may be similar, the MULTIWATT is superior in its performance for pulsed applications.

Figure 14 : Transient Thermal Impedance for Single Pulses in Power DIP and MULTIWATT Packages.



STANDARD SIGNAL PACKAGES

In standard, small signal, packages the easiest thermal path is from the die to the ambient through the molding compound. However, if a high conductivity frame, like a copper lead frame, is used another path exists in parallel. Figure 15 shows the equivalent thermal model of such a package. The effectiveness of a copper frame in transferring heat to the board can be seen in the experimental results in DC conditions.

Table 1 shows the thermal resistance of some standard signal packages in two different conditions ; with the device floating in still air connected to the measurement circuit by thin wires and the same device soldered on a test board.

Table 1 : Thermal Resistance of Signal Packages

Package	Frame Thickness & Material	Rth (j-a) Floating	°C/W on Board
DIP 8	(0.4 mm Copper)	125-165	78-90
DIP 14	(0.4 mm Copper)	98-128	64-73
DIP 16	(0.4 mm Copper)	95-124	62-71
DIP 20	(0.4 mm Copper)	85-112	58-69
DIP 14	(0.25 mm Copper)	115-147	84-95
DIP 20	(0.25 mm Copper)	100-134	76-87
DIP 24	(0.25 mm Copper)	67-84	61-68
DIP 20	(0.25 mm Alloy 42)	158-184	133-145
SO 14	(0.25 mm Copper)	218-250	105-180
PLCC 44	(0.25 mm Copper)	66-83	48-72

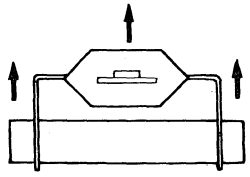
The transient thermal resistance for single pulses for the various packages are shown in figures 16 through 20.

The results of the tests, as shown in the preceding figures, show the true capabilities of the packages. For example, the DIP 20 with a Alloy 42 frame is a typical package used for signal processing applications and can dissipate only 0.5 to 0.7 W in steady state conditions. However, the transient thermal impedance for short pulses is low (11 C/W for t_p = 100 ms) and almost 7 Watts can be dissipated for 100 ms while keeping the junction temperature rise below 80°C.

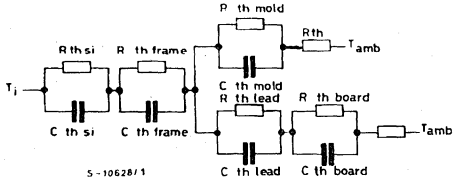
The packages using a 0.4 mm Copper frame have a low steady state thermal resistance, especially in the case of the DIP 20. The thicker lead frame increases the thermal capacitance of the die flag, which greatly improves the transient thermal impedance. In the case of the DIP 20, which has the largest die pad, the transient R_{th} for 100 ms pulses is about 4.3°C/W. This allows the device to dissipate an 18 Watt power pulse while keeping the temperature rise below 80°C.

As with the previous examples the peak transient thermal impedance for repetitive pulses depends on the pulse length and duty cycle as shown in figure 14. With the signal package, however, the effect of the duty cycle becomes much less effective for longer pulses, due primarily to the lower thermal capacitance and hence lower time constant of the frame.

Figure 15.



a) DIP Package Mounted on PCB



b) Equivalent Thermal Circuit DIP Package on PCB

Figure 16 : Transient Thermal Impedance DIP 20 (alloy 42).

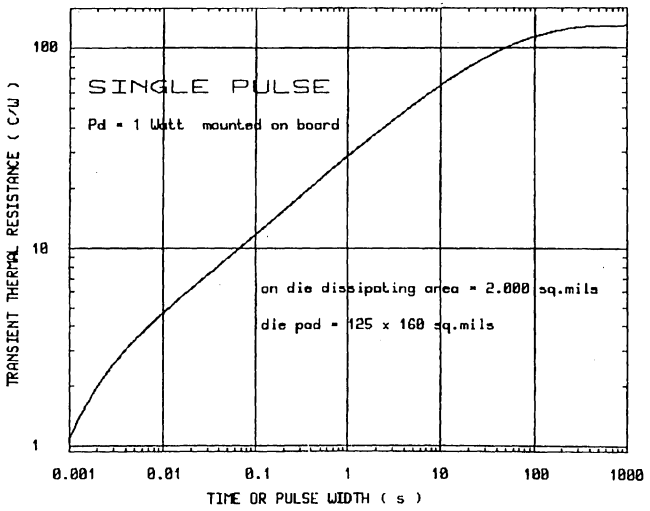


Figure 17 : Transient Thermal Impedance 0.4 mm Copper Frame DIP Packages.

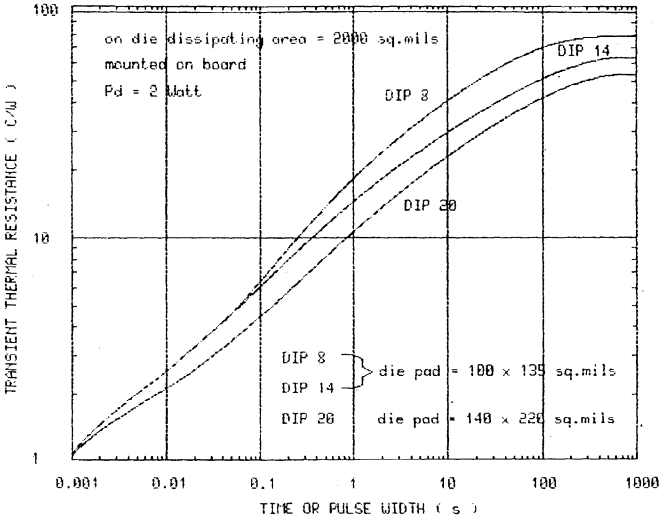


Figure 18 : Transient Thermal Impedance 0.25 mm Copper Frame DIP Packages.

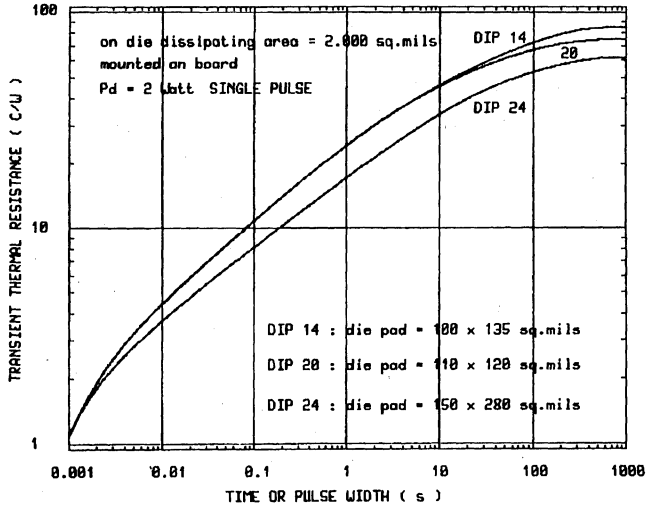


Figure 19 : Transient Thermal Impedance 0.25 mm Frame PLCC Package.

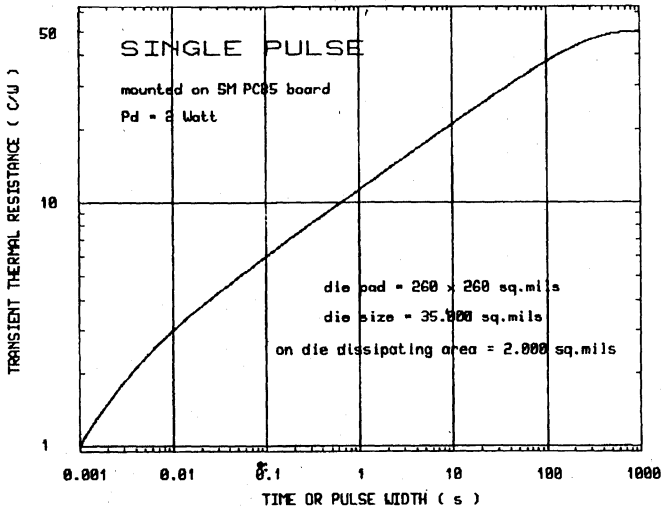


Figure 20 : Transient Thermal Impedance 0.25 mm Copper Frame SO14 Package.

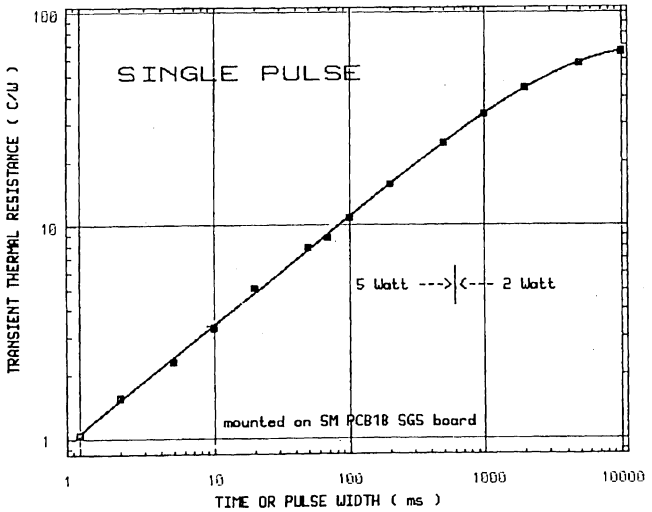
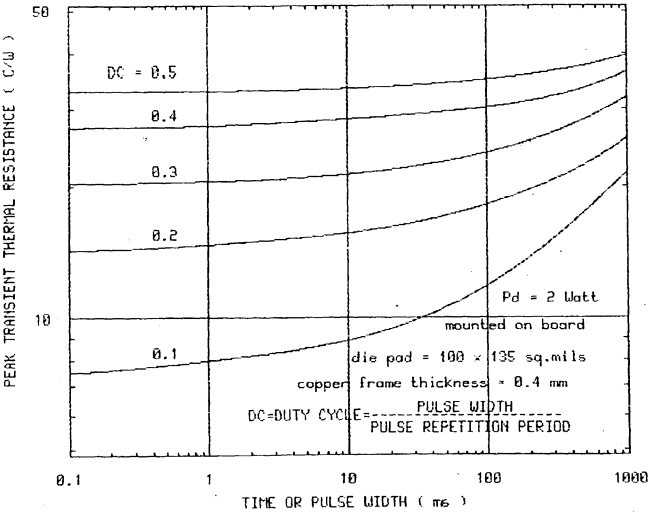


Figure 21 : Peak Thermal Impedance 0.25 mm Copper Frame 14 Lead DIP.



CONCLUSION

This paper has discussed a test procedure for measuring and quantifying the thermal characteristics of semiconductor packages. Using these test methods the thermal impedance of standard integrated circuit packages under pulsed and DC conditions were evaluated. From this evaluation two important considerations arise :

1) The true thermal impedance under repetitive pulsed conditions needs to be considered to maintain the peak junction temperature within the rating for the device. A proper evaluation will result in junction temperatures that do not exceed the specified limits under either steady state or pulsed conditions.

2) The proper evaluation of the transient thermal characteristics of an application should take into account the ability to dissipate high power pulses allowing better thermal design and possibility reducing or eliminating expensive external heat sinks when they are oversized or useless.

REFERENCES

(1) SEMI Draft Specifications 1377 and 1449, 1986

(2) T. Hopkins, R. Tiziani, and C. Cognetti, "Improved thermal impedance measurements by means of a simple integrated structure", presented at SEMITHERM 1986

(3) C. Cini, C. Diazzi, D. Rossi and S. Storti, "High side monolithic switch in Multipower-BCD technology", Proceedings of Microelectronics Conference, Munchen November 1986

(4) Application Notes 106 through 110, SGS-THOMSON Microelectronics, 1987

THERMAL MANAGEMENT IN SURFACE MOUNTING

The evolutionary trends of integrated circuits and printed circuits boards are, in both cases, towards improved performance and reduced size. From these points of view, a factor of major importance has been mutual thermal interaction between ICs, even those with low dissipation.

It follows then that thermal design of medium and high density applications has evolved to include factors such as power effects, die size, package thermal resistance, **integration level of active devices** and substrate type. Added to this a trend towards greater use of switching techniques exists.

Today, in order to design reliable application circuits, it is necessary to have complete data on package thermal response characteristics. In fact, it is a well known and long established fact that device lifetime has an exponential relationship with junction temperature.

PRELIMINARY CONSIDERATIONS

Heat dissipation for DIPs with a low thermal conductivity frame (e.g. Alloy42) is due to convection and **irradiation** from an emiting area corresponding to the silicon die and the package die pad.

Since heat transmission through the lead frame is very poor, dissipation does not depend greatly on substrate type. In fact, samples soldered on printed circuit boards, or inserted in **connectors** have nearly the same dissipation capability as samples suspended in air. The difference, in the range of just 10%, is commonly ignored and specifications for insertion ICs only give one thermal resistance value, which is more than adequate for good thermal design.

The question then arises, is the approximation valid for SO and PLCC packages ?

The answer is no ! Thermal characteristics for these devices are influenced by many factors.

1) Device Related Factors
   - size of the dissipating element
   - dissipation level
   - pulse length and duty cycle

2) Package Related Factors
   - thermal conductivity of the frame
   - frame design

3) Substrate Related Factors
   - thermal conductivity of the substrate
   - layout

Therefore a number of parameters can change the thermal characteristics. These cannot be described by a single thermal resistance, in fact a set of experimental curves gives the best presentation.

JUNCTION TO AMBIENT THERMAL RESISTANCE $R_{th(j-a)}$

$R_{th(j-a)}$ represents the thermal resistance of the system and comprises the silicon die, the package, and any thermal mass in contact with the package to dissipate heat to the ambient.

At a given dissipation level P_d, the increase in junction temperature ΔT_j over ambient temperature T_a is given by :

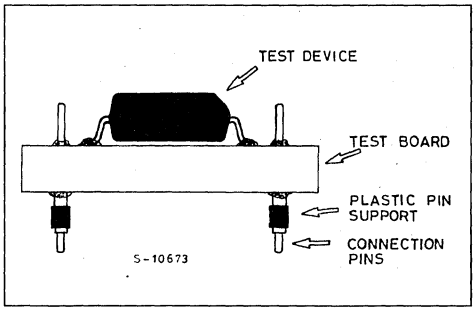
$\Delta T_j = R_{th(j-a)} \times P_d$

$R_{th(j-a)}$ is made up of many elements both within the device and external to it.

If the device is considered alone, $R_{th(j-a)}$ is given by the dissipation path from the silicon die to the leadframe, to the molding compound, to the ambient. **Experimental values are very large in this condition, especially for small packages such as Small Outline types.**

However, this situation is not met in practice and experimental data included in the present work indicates the worst case (floating samples). In most applications, Surface Mount Devices are soldered onto a substrate (commonly epoxy glass (FR4) and are in thermal contact with it through the soldered joints and the copper interconnections. In this case, the heat generated by the active circuit is transferred to the leadframe and then to the substrate. A new dissipation path thus exists in parallel with the previous one whose efficiency depends on the thermal conductivity of the frame and on the length of the printed circuit's copper tracks. Figure A shows the experimental module.

Figure A : Device Soldered to the Best Board, for Junction to Ambient Thermal Resistance Measurement.

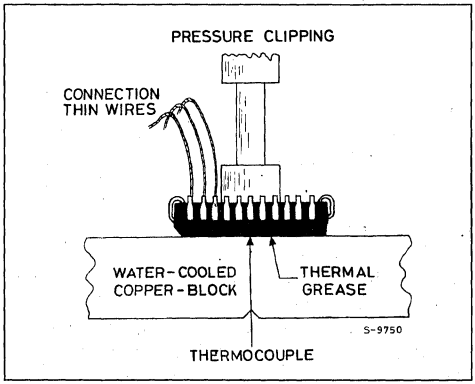


JUNCTION TO CASE THERMAL RESISTANCE $R_{th(j-c)}$

$R_{th(j-c)}$ is the thermal resistance from the junction to a given area of the peackage's external surface where a heatsink is applied.

In signal packages, a suitable area is its upper surface. **Measurements are made with the samples in good thermal contact with an infinite heatsink (fig. B).**

Figure B : Junction to Case Thermal Resistance Measurement.



When a heatsink of thermal resistance R_{hs} is attached to the package, the following relationship is valid :

$$R_{th(j-a)} = R_{th(j-c)} + \frac{R_{hs} \times R^*}{R_{hs} + R^*}$$

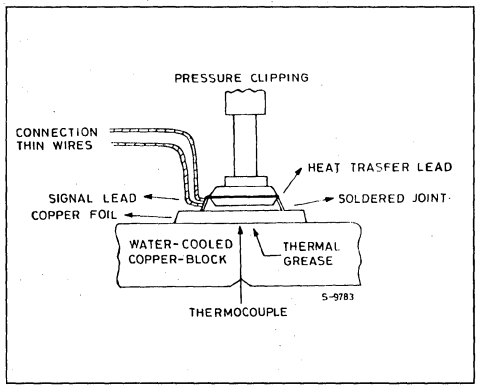
Where R^* takes into account all the other dissipation paths (i.e. junction/frame/substrate). R^* is the lowest with low thermal conductivity frames.

In high power applications $R^* \approx R_{hs}$ and $R_{th(j-a)} = R_{th(j-c)} + R_{hs}$

JUNCTION TO PIN THERMAL RESISTANCE $R_{th(j-p)}$

In medium power packages $R_{th(j-p)}$ is the thermal resistance of the heat transfer leads, from the junction to the external heatsink. In most cases the external heatsink is integrated on the board. Figure C shows the experimental setup.

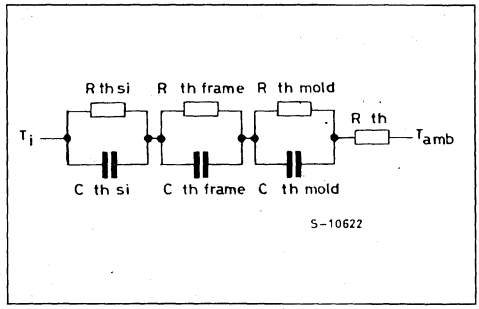
Figure C : Junction to Pin Thermal Resistance Measurement.



TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

The electrical equivalent of heat dissipation for a module formed by an active device, its package, a PCB and the ambient, is a chain of RC cells, as shown in fig. D, each with a characteristic rise time (τ) = RC.

Figure D : Equivalent Thermal Circuit Simplified Package.

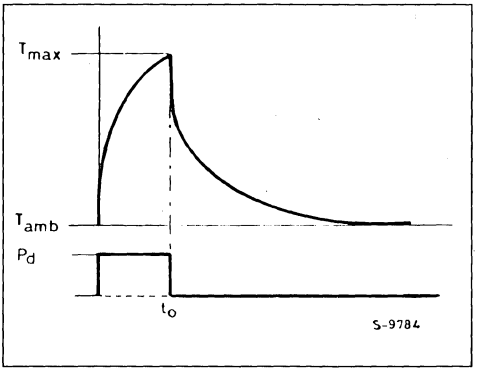


The thermal capacitance of each cell is a measure of its ability to accumulate heat and depends on the specific heat, volume and density of the constituent materials.

When power is switched on, the junction temperature after time it is governed by the heat impedance of the cells, each of which follows its own time constant - this is analogous to the exponential charge of RC cells in an electrical circuit.

For a pulse lenght t_o, the effective T_j can be significantly lower than the steady state T_j (fig. E) and the transient thermal resistance $R_{th(to)}$ can be defined from the ratio between the junction temperature at the end of the pulse and the dissipated power.

Figure E : Temperature Rise for Single Power Pulse.



Obviously, this parameter is smaller for shorter pulses and higher power can be dissipated without exceeding the maximum junction temperature defined from a reliability point of view.

The knowledge of transient thermal data is an important tool for cost effective thermal design of switching applications.

PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES

When pulses of the same height Pd are repeated with a duty cycle, DC, and a pulse width t_o, which is shorter than the overall system time constant, the train of pulses is seen as a continuous source of mean power Pd_{avg}, where :

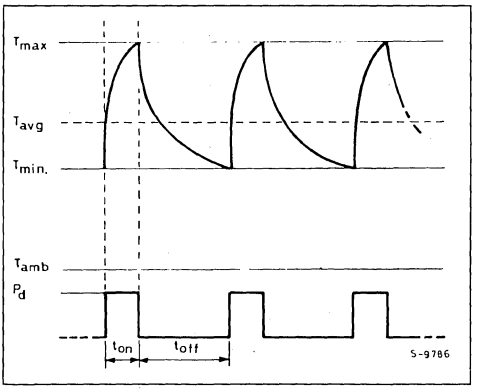
$Pd_{avg} = Pd \times DC$

However the silicon die has a time constant in the order of 1 to 2ms and is able to follow frequencies in the kHz range. Thus junction temperature oscillates about an average value given by :

$T_{javg} = R_{th} \times Pd_{avg}$

as is graphically shown in fig. F.

Figure F : Temperature Rise for Repeated Power Pulses.



The thermal resistance corresponding to the peak of the steady state oscillations (peak thermal resistance indicates the maximum temperature reached by the junction and, depending on duty cycle and pulse width, may be much lower than the DC thermal resistance.

EXPERIMENTAL METHOD

Measurements were performed by means of the especially developed thermal test pattern P432, which is designed according to the Semiconductor Equipment and Materials Institute (SEMI) G32 guideline.

Test chip P432 is based on a dissipating element formed by two npn transistors, each with 10W power capability, and one sensing diode (fig. G). The diode is placed on the temperature plateau generated when the two transistors are biased in parallel, and gives the actual junction temperature T_j of the dissipating element, through the calibration curve (fig. H) of its forward voltage Vf versus temperature at a constant current of 100µA.

Figure G : Thermal Test Pattern P432.

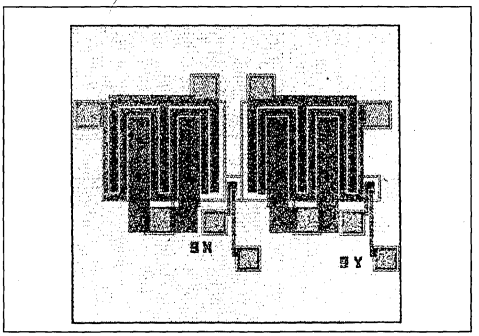
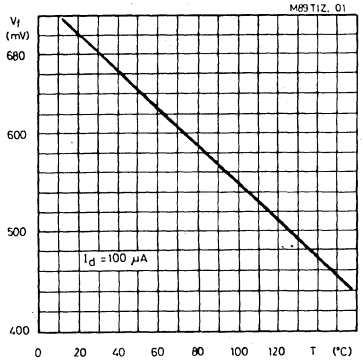


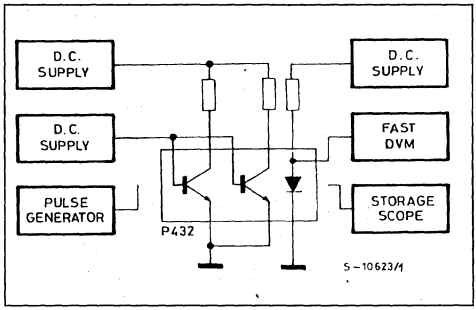
Figure H : Calibration Curve of P432 Temperature Sensing Diode.



Transistor size is intentionally limited to 1000sq. mils, in order to simulate high power density, characterizing a worst case. Die size, which is found to have little influence on thermal resistance when a copper frame is used, is slightly smaller than the die pad size and never exceeds 30k sq mils even in the largest packages such as high pin count PLCCs.

The measurement setup is shown in fig. I. it is compatible with DC and AC supplies and has an accuracy of better than 5%.

Figure 1 : Experimental Setup.



The advantages offered by the test pattern are :

- high power capability
- repeatable V_f and temperature coefficient (1.9mv/C) of the sensing element
- high resolution in pulsed conditions (100µs)
- better correlation from one package to another.

Both Alloy 42 and copper frames were considered for narrow SO packages (150mils body). For wide SO (300mils body) and PLCC packages only copper frames were examined. Suitable test boards were developed (figs J, K and L).

Figure J : Test Board Lay-out for SO Packages (150 mils body width)
Board size is : 23 x 42mm^2.

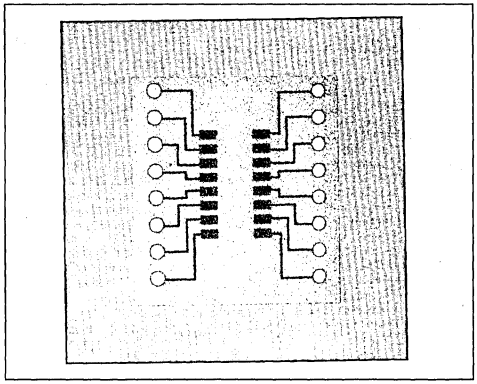


Figure K : Test Board Lay-out for SO Packages (3000 mils body width)
Board size is 38 x 43mm^2.

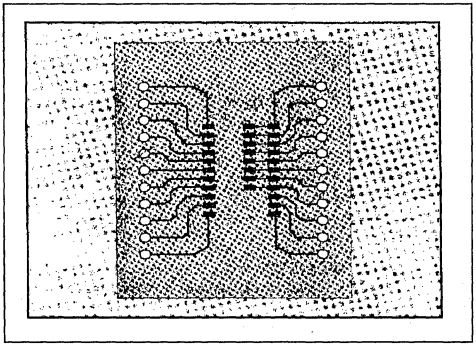
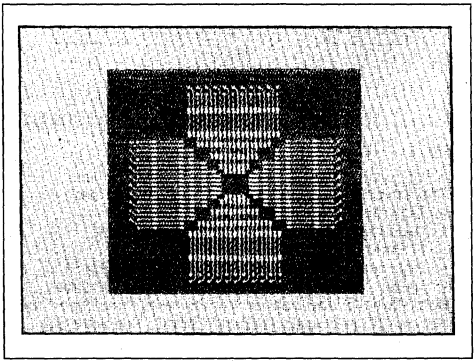


Figure K : Test Board for PLCCs
Board size is 58 x 58mm^2.



MEDIUM POWER PACKAGES

While surface mount signal ICs are readily available, almost all power ICs are still assembled in traditional insertion packages.

Medium power SM packages (Pd < 2W) can readily be derived from existing small outline and chip carrier packages by modifying the leadframe - in much the same way that Powerdip packages were derived from standard Dips.

This approach is particularly attractive because the external dimensions of the package are identical to existing low power packages, allowing the use of standard automatic assembly and test equipment. Frame modification is aimed at obtaining a low junction to pin thermal resistance path for the transfer of heat to a suitable external heatsink. A number of leads are connected to the die pad for this purpose. Two possibilities are considered here : a medium power PLCC44 with 11 heat transfer leads (fig. M) and a medium power SO20 with 8 heat transfer leads (fig. N).

A cost effective heat spreader can be obtained on the board by means of suitably dimensioned copper areas. The heat transfer leads are soldered to there areas (fig. M1, N1).

Figure M : Lead Frame for Medium Power PLCC44.

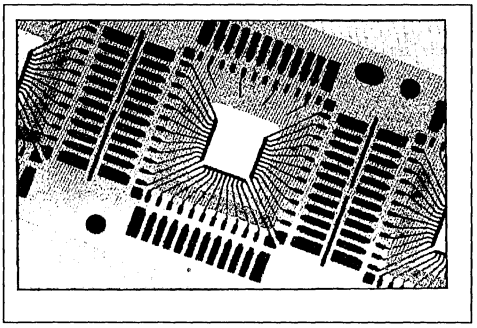


Figure N : Lead Frame for Medium Power SO20.

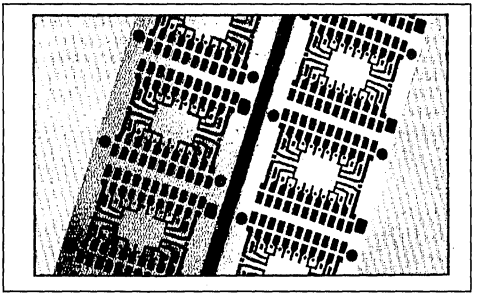


Figure M1 : Test Board for Medium Power PLCC44.

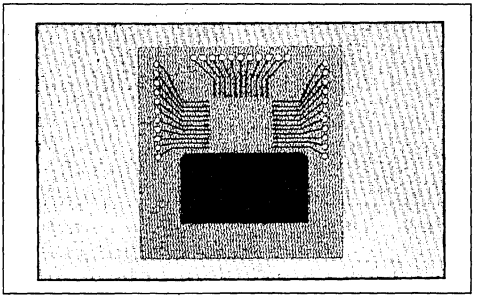
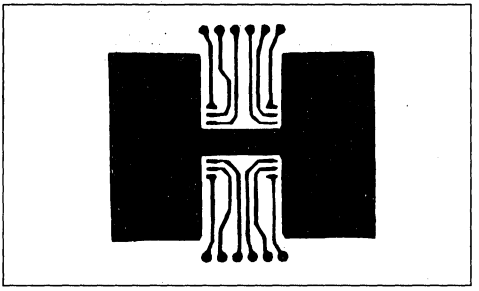


Figure N1 : Test Board for Medium Power SO20.



THERMAL DATA OF SIGNAL PACKAGES

SUMMARY OF JUNCTION TO AMBIENT THERMAL RESISTANCE IN STEADY STATE POWER DISSIPATION (SGS-THOMSON test board)

	Die Size (millinches)	**Power PD [W]**	$R_{th(j-a)}$ [°C/W] on Board
SO8 Alloy 42	90 x 100	0.2	250-310
Copper	94 x 125	0.2	130-180
SO14 Alloy 42	98 x 100	0.3	200-240
Copper	78 x 118	0.5	120-160
Copper	98 x 125	0.7	105-145
SO16 Alloy 42	98 x 118	0.3	180-215
Copper	94 x 185	0.5	95-135
SO16W Copper	120 x 160	0.7	90-112
SO20 Copper	140 x 220	0.7	77-97
PLCC-20 Cu	180 x 180	0.7	90-110
PLCC-44 Cu	260 x 260	1.5	50-60
PLCC-68 Cu	425 x 425	1.5	40-46
PLCC-84 Cu	450 x 450	2.0	36-41
$R_{th(j-a)}$ values correspond to low and high board density			

SUMMARY OF JUNCTION TO CASE THERMAL RESISTANCE

	Die Pad Size (millinches)	$R_{th(j-a)}$ [°C/W]
PLCC20	140 x 140	25
PLCC44	260 x 260	13
PLCC68	425 x 425	10
PLCC84	450 x 450	9

JUNCTION TO AMBIENT THERMAL RESISTANCE IN STEADY STATE POWER DISSIPATION

Figure 1 : SO8.

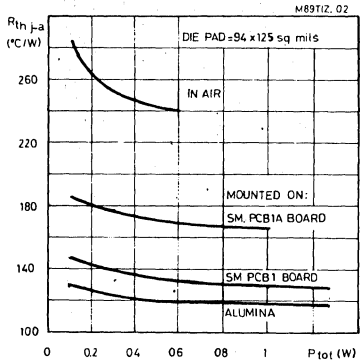


Figure 2 : SO14.

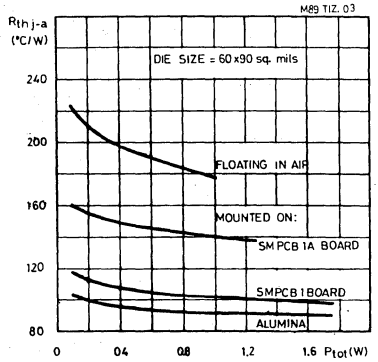


Figure 3 : SO16.

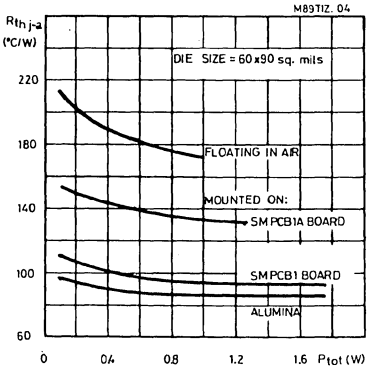


Figure 4 : SO20.

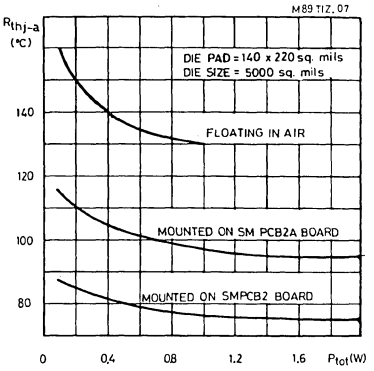


Figure 5 : PLCC20.

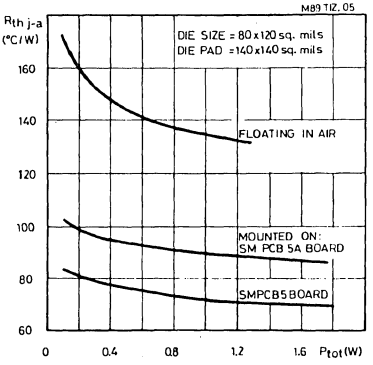


Figure 6 : PLCC44.

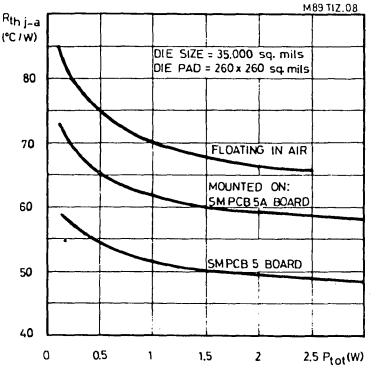


Figure 7 : PLCC68.

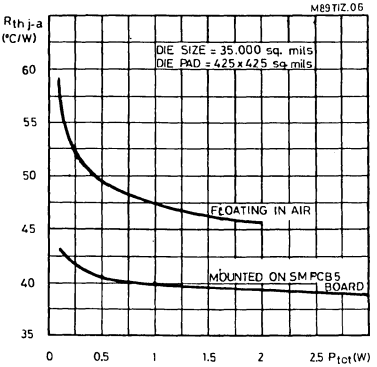
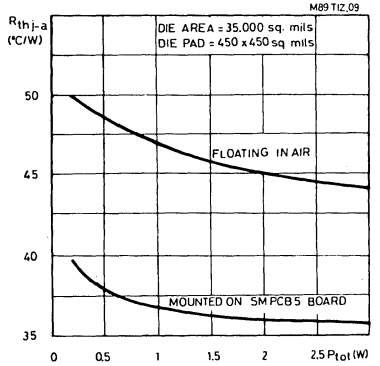


Figure 8 : PLCC84.



JUNCTION TO AMBIENT THERMAL RESISTANCE VS BOARD LAY-OUT
(area of copper tracks on the board)

Figure 9 : SO16.

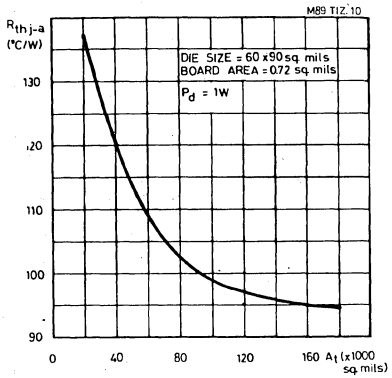


Figure 10 : SO20.

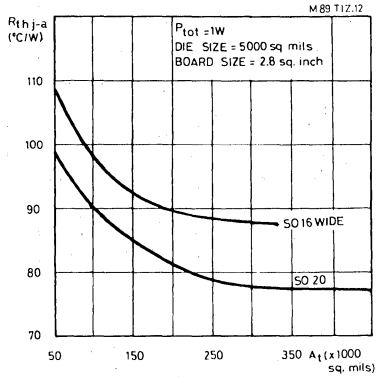


Figure 11 : PLCC44.

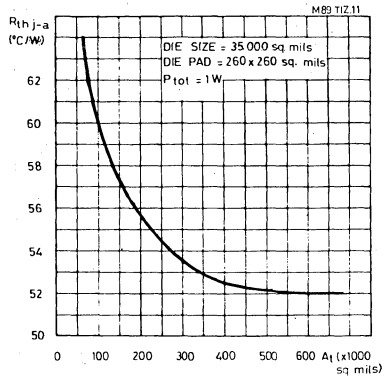
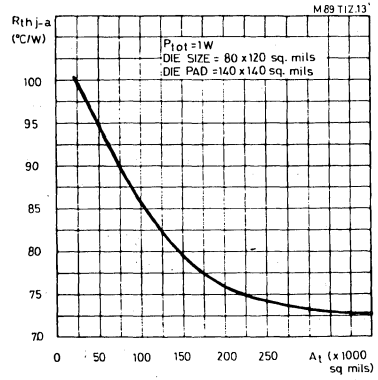


Figure 12 : PLCC20.



TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

Figure 13 : SO8.

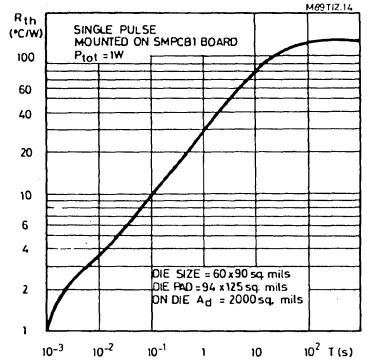


Figure 14 : SO14, 16.

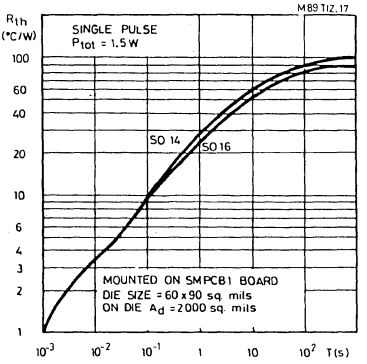


Figure 15 : SO20.

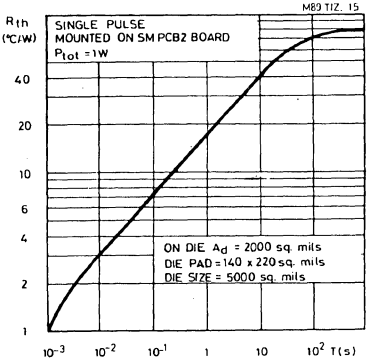


Figure 16 : PLCC44.

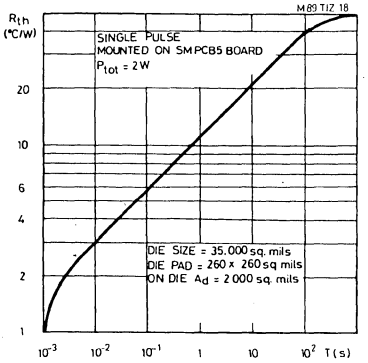


Figure 17 : PLCC68.

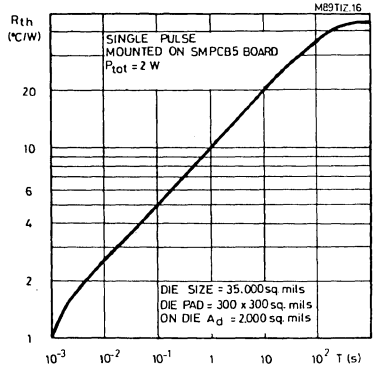
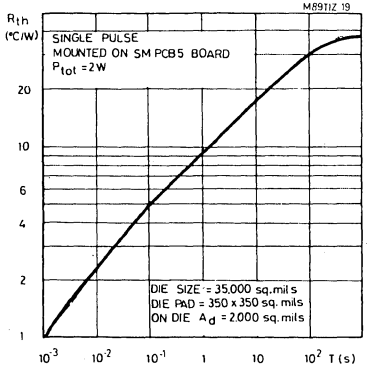


Figure 18 : PLCC84.



PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES

Figure 19 : SO14.

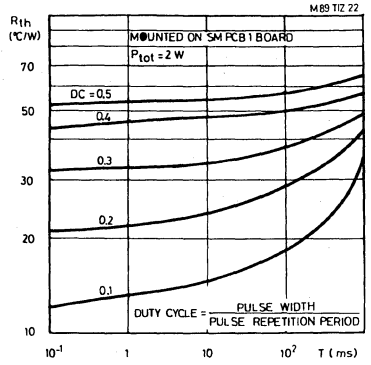


Figure 20 : SO20.

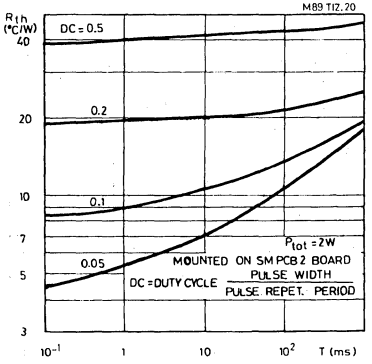


Figure 21 : PLCC44.

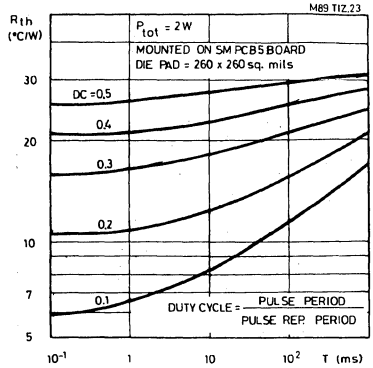


Figure 22 : PLCC68.

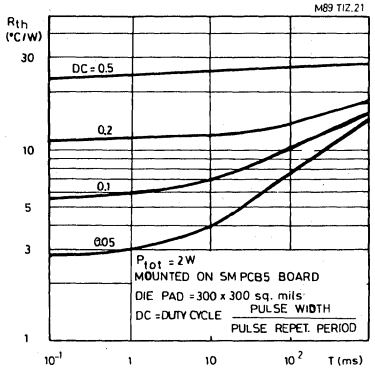
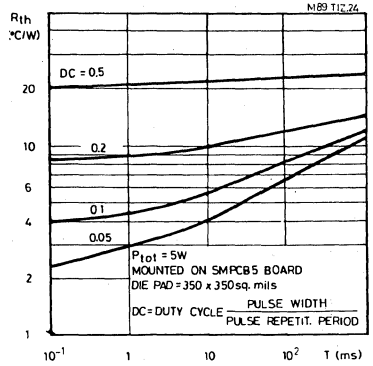


Figure 23 : PLCC84.



THERMAL DATA OF MEDIUM POWER PACKAGES

	$R_{th(j-p)}$ [°C/W] (AVERAGE)	$R_{th(j-a)}$* [°C/W]
SO (12 + 4 + 4)	14	50
PLCC (33 + 11)	12	41

* with 6 sq. cm. on board heat-sink.

JUNCTION TO PINS THERMAL RESISTANCE VS ON DIE DISSIPATING AREA

Figure 24 : SO (12 + 4 + 4).

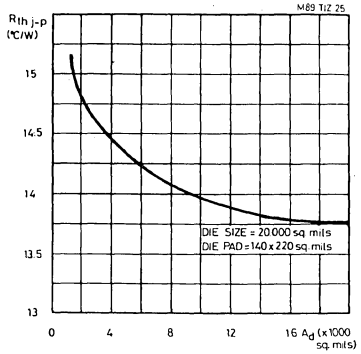
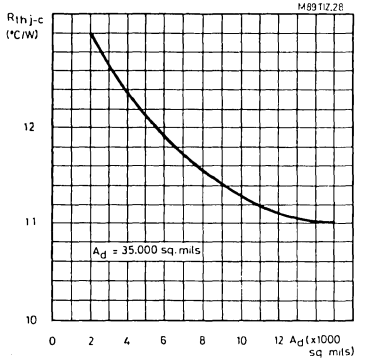
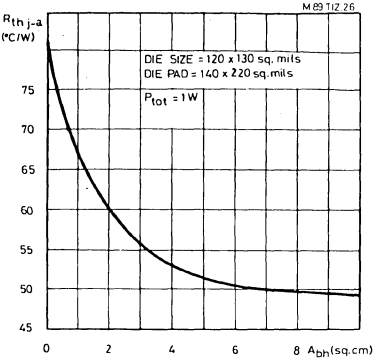


Figure 25 : PLCC (33 + 11).



JUNCTION TO AMBIENT THERMAL RESISTANCE VS AREA ON BOARD HEAT-SINK

Figure 26 : SO (12 + 4 + 4).



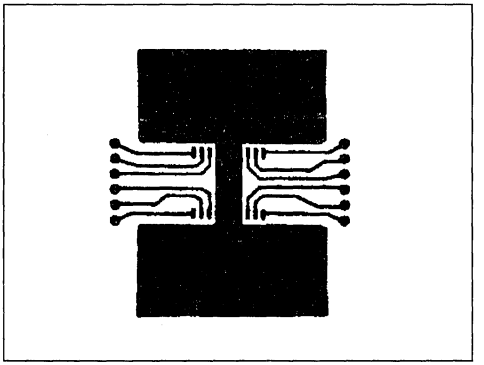
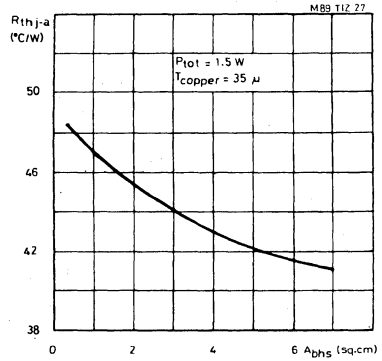
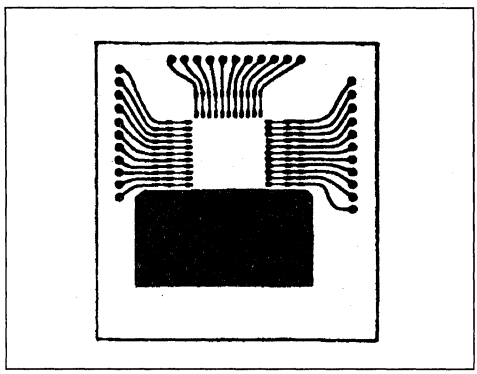


Figure 27 : PLCC (33 + 11).





TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

Figure 28 : SO (12 + 4 + 4).

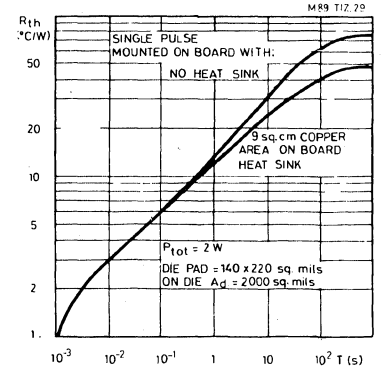
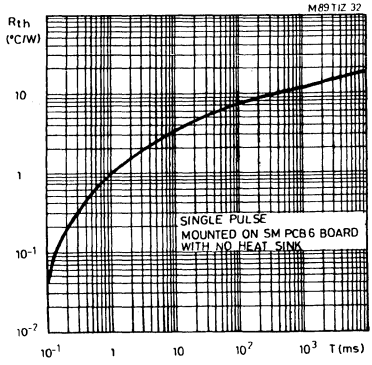
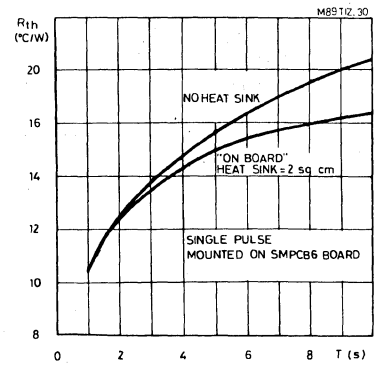


Figure 29 : PLCC (33 + 11).



pulse length = 0.1 – 10ms.

Figure 30 : PLCC (33 + 11).



pulse length = 1 – 10s.

PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES.

Figure 31 : PLCC (12 + 4 + 4).

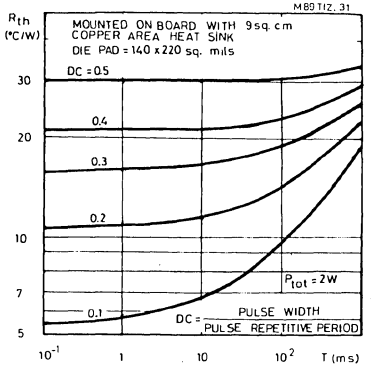
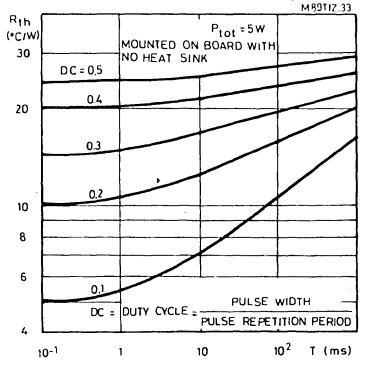


Figure 32 : PLCC (33 + 11).



APPLICATION EXAMPLES OF THERMAL DATA

Good thermal design begins with system and reliability considerations. This turn is based on correct consideration of ambient and device temperature parameters.

The ambient temperature T_a defined for applications can range from 50 to 55°C, as is common in many consumer and computer applications, through to 80°C or more in applications such as automotive systems. The ambient temperature depends on the various heat and cooling sources surrounding the device. An important factor in device lifetime is junction temperature - lifetime is approximately halved when junction temperature T_j is increased by 10°C. The maximum junction temperature commensurate with good reliability, takes into account the activation energy of the failure mechanisms which may differ for various silicon and packaging technologies.

In plastic packages the maximum T_{jmax} is 150°C, but lower values (100 to 120°C) may be specified in high rel applications such as telecoms.

When T_{jmax} and T_a are known, their difference ΔT_j indicates the permissible junction temeperature rise for a given device. For a given power dissipation Pd, the thermal design must ensure that the product Pd x Rth(j-a) is lower than ΔT_j ; where $R_{th(j-a)}$ is the thermal resistance of the device from the junction to the ambient at temperature T_a. This takes into consideration the many elements connected to the heat source and includes the leadframe, moulding compound, substrate and heatsink, if used.

EXAMPLE 1 : Maximum dissipation for SO16 packaged device soldered onto an FR4 board (1 oz copper) under the following conditions :

- Ambient temperature : $T_a = 70°C$
- Maximum Junction Temperature : $T_{jmax} = 130°C$

The average length of the 12mils wide copper line connected to each pin is 80mils, soldering pads are 30 x 40mils. The total are is thus :

A = [(80 x 12) + 1200 x 16] = 34560sq.mils

SOLUTION

From fig. 13, the value for $R_{th(j-a)}$ is 125°C/W for a copper frame package. Comparing figs. 5 and 6, a value of about 240°C/W can be assumed for Alloy 42 packages. The allowed rise in junction temperature is : $\Delta T_{jmax} = 130 - 70 = 60°C$

Maximum dissipation is given by $\Delta Tjmax/R_{th(j-a)}$.

Therefore :

60/125 = 0.48W for Copper frame

60/240 = 0.25 for Alloy 42 frame

EXAMPLE 2 : Junction temperature for an SO20 packaged device soldered on FR4, under the following conditions :

- Ambient temperature T_a = 70°C
- Dissipated Power Pd = 0.6W

SOLUTION

A total trace-area of 200k sq.mils is assumed,this then gives, from fig. 14 :

- Thermal Resistance $R_{th(j-a)}$ = 90°C/W
- ΔT_j = Pd x $R_{th(j-a)}$
- ΔT_j = 0.6 x 90 = 54°C
- Junction Temperature T_j = 54 + 70 = 124°C

EXAMPLE 3 : To determine the size of an integrated heatsink for a medium power application using a PLCC (33 + 11) under the following conditions :

- Ambient temperature T_a = 50°C
- Max. Junction Temperature T_{jmax} = 150°C
- Dissipated Power Pd = 2.2W

SOLUTION

By calculation the application needs an $R_{th(j-a)}$ of : (150 - 50)/2.2 = 45.5°C/W

From figure 32 the on board heatspreader can thus be defined as needing an area of about 2 sq.cm.

EXAMPLE 4 : Given the application described in example 3 determine the maximum pulse width for a single 4W pulse superimposed on a continuous 1.5W dissipation

SOLUTION

The continuous steady state junction temperature at 1.5W dissipation is :

T_{jss} = (1.5 x 45.5) + 50 = 118.25°C

The single pulse is allowed to cause a maximum increase of (150 - 118.25°C) = 31.75°C.

The related transient thermal resistance is (31.75/4) = 7.9°C/W

From figure 33, the corresponding pulse width can be interpreted as being in the order of 200ms.

EXAMPLE 5 : In a medium power application using an SO (12 + 4 + 4) calculate the average junction temperature and the peak temperature for repeated pulses under the following conditions :

- Ambient temperature T_a = 70°C
- On board heatsink area A = 9 sq.cm.
- Pulse length = 100ms
- Pulse height = 5W
- Duty cycle = 20%

SOLUTION

From figure 31, the thermal resistance is found to be 49°C/W. Thus the average junction temperature can be calculated :

T_{javg} = (5 x 49 x 0.2) + 70 = 119°C

From figure 36, the peak thermal resistance is given as around 15°C/W. The peak temperature can thus be calculated as :

T_p = (5 x 15) + 70 = 145

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

THERMAL CHARACTERISTICS OF THE MULTIWATT PACKAGE

By R. TIZIANI

INTRODUCTION

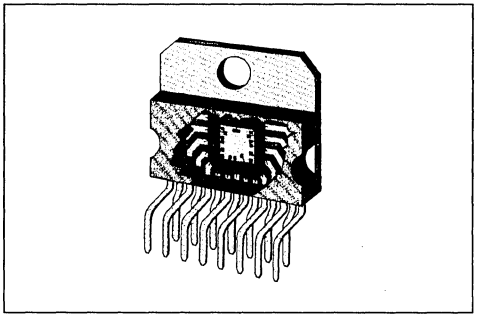
This Application Note provides a complete thermal characterization of the Multiwatt ® package (multilead double TO-220 - fig. 1).

Characterization is performed according with recomandations included in the G32-86 SEMI guideline, by means of a dedicated test pattern. It refers to :

1. Junction to case thermal resistance $R_{th(j-c)}$
2. Junction to ambient thermal resistance $R_{th(j-a)}$
3. Junction to ambient thermal impedance for single pulses and repated pulses, with different pulse width and duty cycle ;
4. Thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techniques.

Figure 1 : Multiwatt Assembly.



EXPERIMENTAL CONDITIONS

The thermal evaluation was performed by means of the test pattern P432, which is a 20K $mils^2$ die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 2K $mils^2$ with a power capability of 20W. Measurement method is described in Appendix A.

Samples with the indicated characteristics were prepared :

Package Multiwatt 15 leads

Frame Material	Copper
Slug Thickness	1.5mm
Slug Thermal Conductivity	3.9W/cm°C
Die Attach	Soft (PbSn)

Measurement of junction to case thermal resistance $R_{th(j-c)}$ is performed by holding the package against a water cooled heat sink, according with fig. 2. A thermocouple placed in contact with the slug measures the reference temperature of the case.

For junction to ambient thermal resistance $R_{th(j-a)}$ the samples are suspended horizontally in a one cubic foot box, to prevent drafts.

Both DC and pulsed conditions are used ; in the second case the contribution of package thermal capacitance is effective and transient thermal resistances much lower than the steady stata $R_{th(j-a)}$ can be found, according to pulse length and duty cycle.

The effect of the external heat sink is quantified, using as test vehicle the commercially available heat sink THM7023 especially developed by Thermalloy for the Multiwatt package, whose thermal resistance in still air is about 9°C/W.

The measurement circuit shown in fig. A3 was used for all the thermal evaluations.

JUNCTION TO CASE THERMAL RESISTANCE

The dependance of $R_{th(j-c)}$ on the dissipated power is reported in fig. 3.

It is well known that the main contribution to $R_{th(j-c)}$ of power packages in given by the silicon die.

Figure 2 : Measurement of $R_{th\ (j-c)}$.

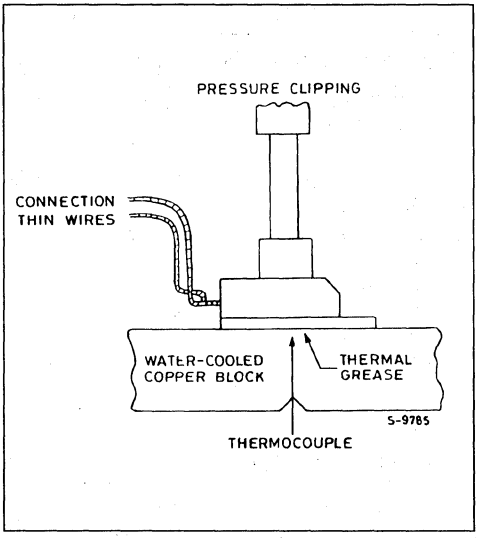
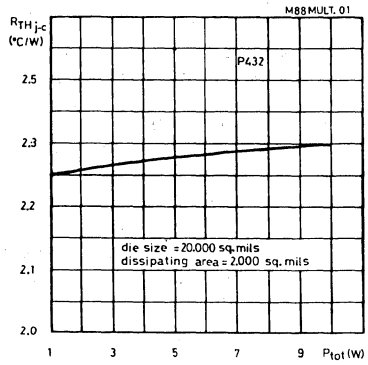


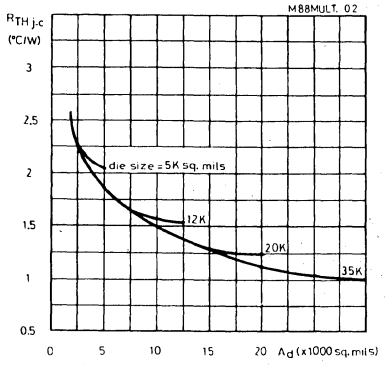
Figure 3 : $R_{th\ (j-c)}$ of Multiwatt Package vs. Power Level.



FOR DEVICES OTHER THAN THE TEST PATTERN P432 THE CALIBRATION CURVE OF FIG. 4 IS NEEDED.

It shows the relationship between $R_{th(j-c)}$ and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

Figure 4 : $R_{th(j-c)}$ Thermal Resistance vs. Die Size and on Die dissipating Area.



JUNCTION TO AMBIENT THERMAL RESISTANCE

In medium power applications (1.5-2W), the Multiwatt package can be used without external heat sink, thanks to the significant size (about 3.5cm^2) of its integrated thermal mass.

Its $R_{th(j-a)}$ has two contributions : the $R_{th(j-c)}$, mainly due to the silicon die (as shown in fig. 4) and the thermal resistance of the copper slug $R_{th\ slug}$.

Figure 5 : $R_{th(j-a)}$ of Multiwatt Package vs. dissipated Power.

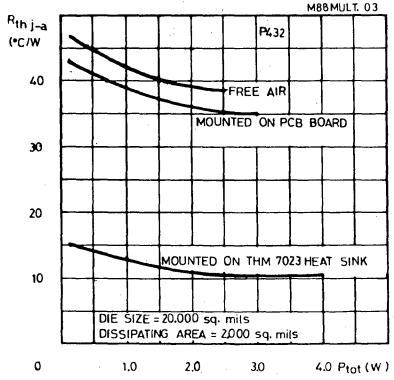


Fig. 5 gives the relationship between $R_{th(j-a)}$ and the power dissipation level for the P432 test pattern is still air, on PC board and on a commercial heat sink.

IN ORDER TO HAVE AN ACCURATE VALUE FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 5 SHOULD BE CORRECTED THROUGH THE CALIBRATION CURVE OF FIG. 4 CORRECTION TERM IS ALWAYS IN THE RANGE OF 0-2°C/W ; THEREFORE, IT AFFECTS THE $R_{th(j-a)}$ OF NO MORE THAN 5% IN STILL AIR OR WITH THE PACKAGE MOUNTED ON PC BOARD.

TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (without external heat sink)

The effect of single pulses of different length and height for the Multiwatt package without any external heat sink is shown in fig. 6.

This behaviour is discussed in Appendix B. Due to a significant thermal capacitance (C = 2J/°C) and correspondingly long risetime (τ = 80s), single pulses up to 30W can be delivered to the Multiwatt package for 1s with acceptable junction temperature increase.

IN ORDER TO HAVE ACCURATE R_{th} (t_o FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 7 MUST BE CORRECTED AS DESCRIBED IN EXAMPLE 2 OF THE LAST SECTION.

Repetition of pulses with defined P_d, period and duty cycle DC (ratio betwen pulse length and signal period), gives rise to oscillations in junction temperature as described in Appendix B.

The transient thermal resistance corresponding to the upper limit of the curve of fig. B4 (peak transient thermal resistance) is reported in fig. 7 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (with external heat sink)

Characterization has been repeated with a commercial heat sink (Thermalloy THM7023) in order to have an example of the effect of an external thermal mass on the impedance of the thermal module.

Relationship between transient R_{th} and pulse length is reported in fig. 8.

The effect of the increased thermal capacitance is evident in fig. 9, where thermal data of fig. 6 and 8 are compared : it can be noticed that the curves are definitely different for pulses longer than 1s, corresponding about to the rise time of the slug. The effect of the thermal mass is to keep low the heating rate of the silicon die thus allowing a better power management of long power pulses. This conclusion has general validity and can be applied to other heat sinks than the one considered in this note.

Figure 6 : Transient Thermal Resistance for Single Pulse.

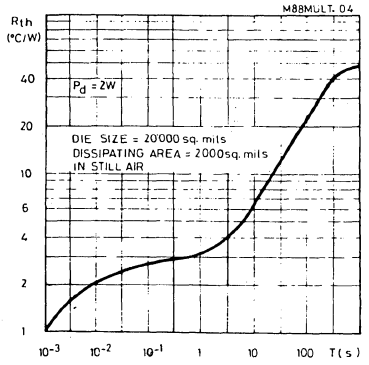


Figure 7 : Peak Transient R_{th} vs. Pulse width and Duty Cycle.

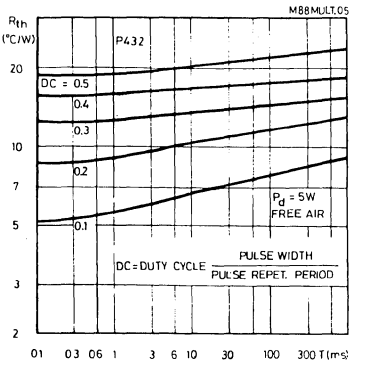


Figure 8 : Transient R_{th} for single pulses, with Heatsink.

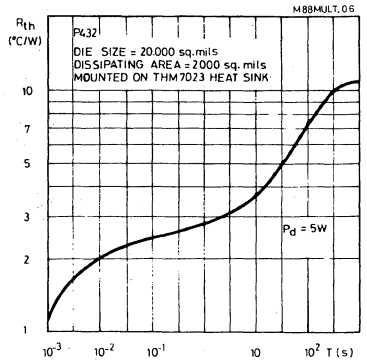
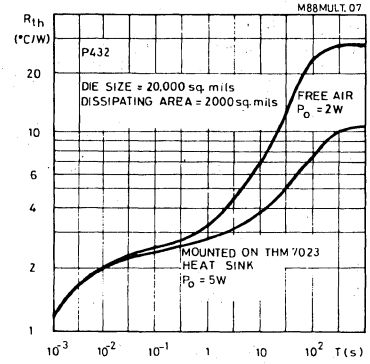


Figure 9 : Comparison of Transient R_{th} for single pulses, with and without Heat Sink.



APPENDIX A

The thermal resistance evaluation is performed with the especially designed test chip P432 which has two bipolar power transistor and one sensing diode (fig. A1). The active area is about 2000 $mils^2$ on a 35000$mils^2$ chip. Its lay-out was optimized in order to have a uniform temperature area, once the two transistor are powered ; the sensing diode is placed at the center of this area.

The relationship between the forward voltage V_f of the diode at the constant current of 100µA and the temperature is shown in fig. A2. The curve calibrates the junction temperature through the voltage drop of the diode.

The measurement circuit is shown in fig. A3. A storage oscilloscope or a fast digital voltmeter can be used for recording the V_f value.

Figure A1 : Test Pattern P432 Lay-out.

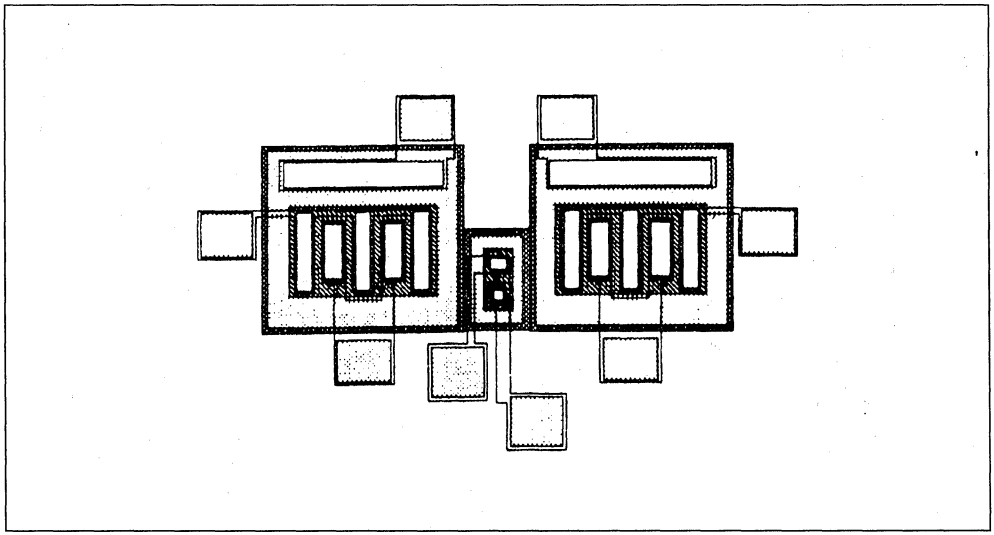


Figure A2 : Calibration Curse (sensing diode).

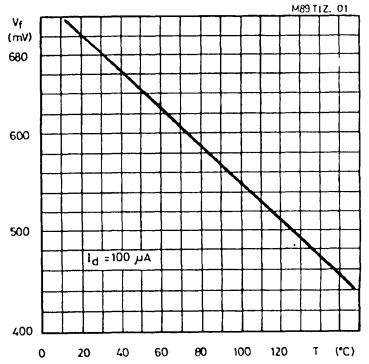
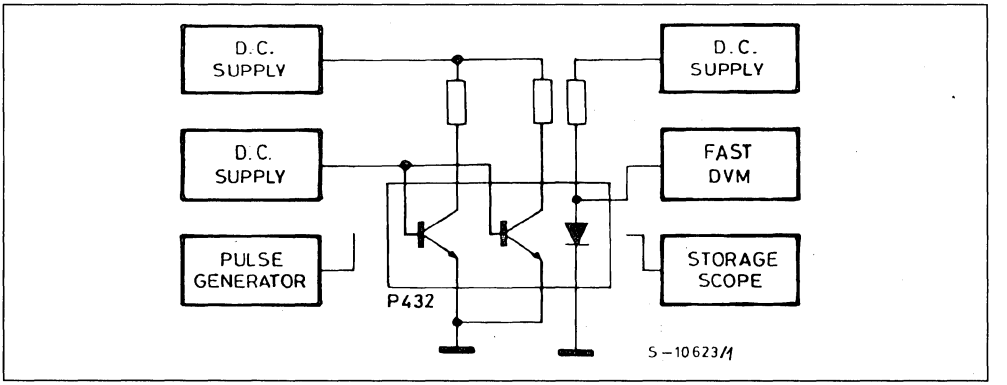


Figure A3 : Measurement Circuits.



APPENDIX B - THERMAL MANAGEMENT IN PULSED CONDITION

THERMAL RESISTANCE AND CAPACITANCE

The electrical equivalent of heat dissipation, for a thermal module formed by the active device with its package and the external heat sink is shown in fig. B1.

To each cell of the thermal chain are associated a value of thermal resistance R_{th} (°C/W) and a value of thermal capacitance C_{th} (J/°C). The former informs about temperature increase due to the element represented by the cell ; as, in the example under consideration, heat transfer is mainly based on conduction for the silicon, the copper integrated heat sink and to metallic body of the external heat sink R_{th} can be calculated from the relationship :

$$R_{th} = \frac{\gamma}{K \times S}$$

where K is the thermal conductivity of the material, the length of the conductive path and S its section.

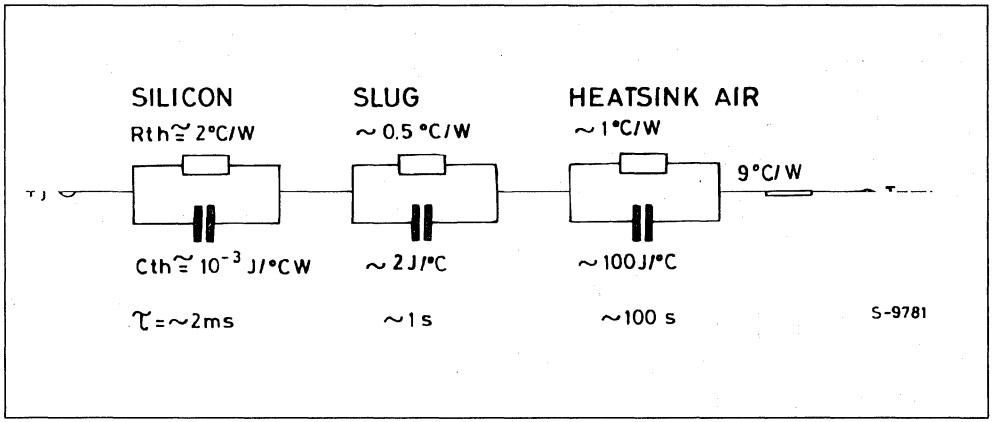
Thermal capacitance C_{th} is the capability of heat accumulation ; it depends on the specific heat of the material and on the volume effectively interested by heat exchange (this means that the parts which are not heated during heat dissipation DO NOT contribute to thermal capacitance). Thermal capacitance is given by :

$$C_{th} = d \times c_t \times V$$

where d is the density of the material, c_t its specific heat and V the volume interested to heat accumulation.

The last element of the network, assumed as purely resistive, is due to convection and radiation from the external heat sink towards the ambient.

Figure B1 : Electrical Equivalent of Multiwatt Package Mounted on the External Heatsink.



Each cell has its own risetime τ , given by the product of the thermal resistance and capacitance :

$$\tau = R_{th} \times C_{th}$$

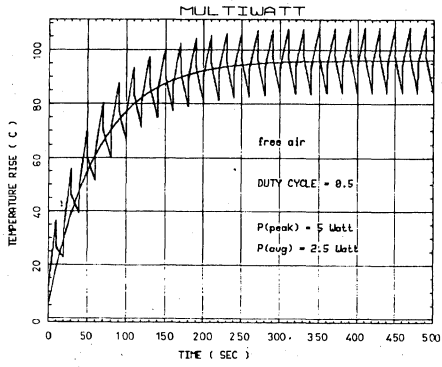
The value of the time constant determines whether a cell approaches equilibrium rapidly of slowly : if R_{th} or C_{th} increases, equilibrium is reached at a slower rate. The following relationship is valid for each cell :

$$\Delta T = R_{th} \times P_d \left[1 - e^{-t/r}\right] (1)$$

Typical values of R_{th}, C_{th} and τ for Multiwatt application are shown in fig. B1.

When power is switched on, temperature increase is ruled by subsequent charging of thermal capacitances while the value reached in the steady state depends on thermal resistances only. Qualitative behaviour of the network of fig. B1 is shown in fig. B2.

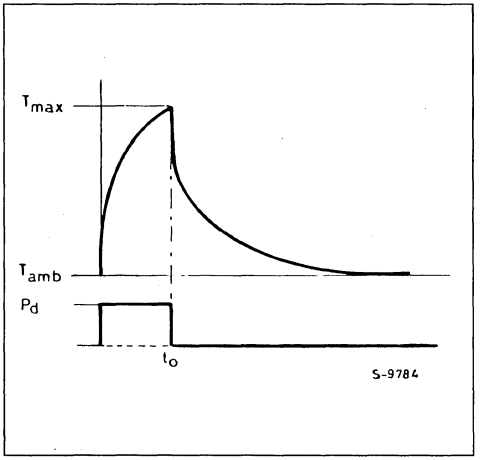
Figure B2 : Qualitative T_j increase (network of fig. B1) for repeated Power Pulse.



SINGLE POWER PULSE

When the pulse length has an assigned value, effective T_j can be significantly lower than the steady state T_j (fig. B3.).

Figure B3 : Effect of a Single Power Pulse.



For any pulse length t_o, a transient thermal resistance R_{th} (t_o) is defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power. Obviously, for shorted pulses, R_{th} (t_o) is lower and a higher power can be dissipated, without exceeding the maximum junction temperature $T_{j\text{-}max}$ allowed to the IC from reliability considerations. Fig. 7 and 9 of this Application Note give experimental values of R_{th} (t_o) for the two cases of the Multiwatt package without and with external heat sink.

REPEATED PULSES

When pulses of the same height P_d are repeated with a defined duty cycle DC and pulse length is short in comparison with the total risetime of the system (many tens of seconds) the train of pulses is seen by the system as a continuous source, at a mean power level of

$$P_{davg} = P_d \times DC$$

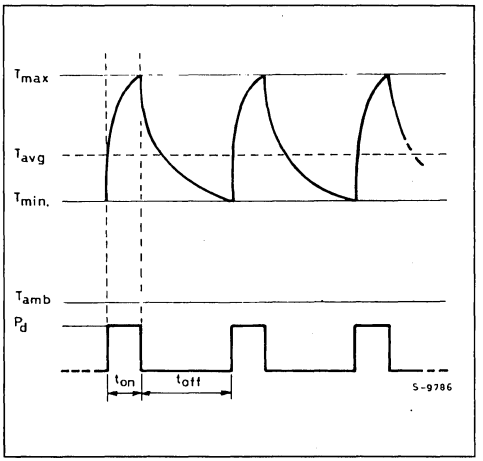
The average temperature increase is :

$$\Delta T_{avg} = R_{th} \times P_{davg} = R_{th} \times P_d \times DC$$

On the other hand, the silicon die (τ_S = 1– 3ms) is able to follow frequencies of some KHz and junction temperature oscillates about the average as qualitatively shown in fig. B4.

The thermal resistance corresponding to the peak of the oscillation at equilibrium (peak thermal resistance $R_{th\,peak}$) is now given by fig. 5, and can be obtained if pulse length and duty cycle are known ; P_{dmax} is derived from the same figure.

Figure B4 : Junction Temperature increase for repeated Pulses.



APPLICATION EXAMPLES

EXAMPLE 1 - MAXIMUM P_d FOR SINGLE PULSE OF ASSIGNED LENGTH

PROBLEM : define the maximum P_d for a single pulse with a length of 20ms in the case of Multiwatt package used without heat sink. Ambient temperature is 50°C ; maximum temperature is 130°C. Die size is 20K mils^2, with dissipating area of 2K mils^2 (as in P432 test pattern).

SOLUTION : allowed temperature increase ΔT is 80°C. Having a $R_{th(j\text{-}a)}$ of 39°C/W, Multiwatt package can dissipate about 2W in steady state. From fig. 7 the transient thermal resistance corresponding to one single pulse of 20ms is R_{th} $(20ms)_{P432}$ = 2.2°C/W. A peak of 80/2.2 = 36.3W can be applied to the circuit.

EXAMPLE 2 - CORRECTION FOR DIE SIZE AND DISSIPATING AREA

PROBLEM : correct the results obtained in example 1, for assigned die size and dissipating area. Practical case : IC having a die size of 35K mils^2 with a dissipating area of 20k mils^2.

SOLUTION : from fig. 5, thermal resistances of P432 and of the IC under consideration are $R_{th\,P432}$ = 2.3°C/W and $R_{th(j\text{-}c)IC}$ = 1.2°C/W.

As the length of the pulse is 10-15 times longer than the rise time of the silicon, the die (first cell of fig. B1) can be assumed to have reached its equilibrium condition.

R_{th} (20ms) found in previous example has to be corrected in order to take into account the new value of $R_{th(j-c)}$:

$$R_{th}\ (20ms)_{IC} = R_{th}\ (20ms)_{P432} - R_{th(j-c)P432} + R_{th(j-c)IC} =$$
$$= 2.2 - 2.3 + 1.2°C/W = 1.1°C/W$$

A single pulse of 80/1.1 ≅ 72W can be delivered to such device.

When the pulse has the same order of silicon rise time τ P432 is about 1ms) another type of correction is needed. In first approximation, τ increase with dissipating area with the relationship :

$$t_{IC} = \sqrt{20K_{IC}/2K_{P432} \times \tau_{P432}} \equiv 3.1ms$$

Expansion of the exponential term of relationship (1) limited to the first term term, is :

$$R_{th\ IC}\ (t_o) \cong R_{th\ P432}\ (t_o)\ /3.1$$

for t_o = 1ms :

$$R_{th\ IC}\ (1ms) = 1.05/3.1°C/W \cong 0.34°C/W$$

A single pulse of 80/0.34 ≅ 235W can be delivered to such device.

EXAMPLE 3 – R_{th} WITH REPEATED PULSES

PROBLEM : find the peak power which can be dissipated by Multiwatt package without heatsink, when power is continuously switched on 10ms and switched off 90ms. Ambient temperature is 50°C, maximum temperature is allowed to be 125°C.

SOLUTION : a maximum ΔT = 75°C has to be considered. Fig. 5 indicated that for a pulse width of 10ms and a duty cycle of 0.1, $R_{th\ peak}$ is 6.7°C/W. Maximum P_d is 75/6.7 = 11.2W, with an average temperature increase ΔT_{peak} of 39 x 0.1 x 11.2 ≅ 43°C.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

THERMAL CHARACTERISTICS OF THE PENTAWATT-HEPTAWATT PACKAGES

By R. TIZIANI

INTRODUCTION

This Application Note is aimed to give a complete thermal characterization of the Heptawatt and Pentawatt package (fig. 1, 2).

Characterization is performed according with recomendations included in the G32-86 SEMI guideline, by means of a dedicated test pattern. It refers to :

1. Junction to case thermal resistance $R_{th(j-c)}$
2. Junction to ambient thermal resistance $R_{th(j-a)}$
3. Junction to ambient thermal impedance for single pulses and repeated pulses, with different pulse width and duty cycle ;
4. thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techniques.

Figure 1 : Pentawatt.

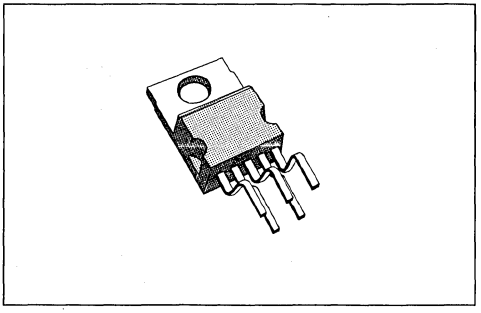
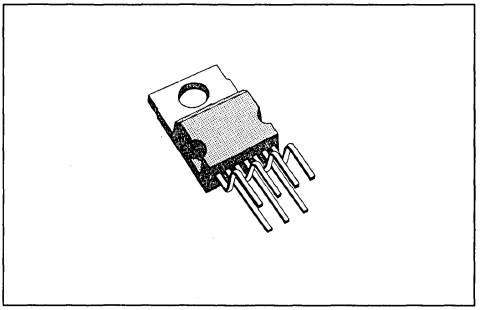


Figure 2 : Heptawatt.



EXPERIMENTAL CONDITIONS

The thermal evaluation was performed by means of the test pattern P432, which is a 15k mils^2 die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 2k mils^2 with a power capability of 20W. Measurement method is described in Appendix A.

Samples with the indicated characteristics were prepared :

Package	Pentawatt - Heptawatt
Frame Material	Copper
Slug Thickness	1.25mm Typ.
Slug Thermal Conductivity	3.9W/cm°C
Die Attach	Soft (PbSn)

Measurement of junction to case thermal resistance $R_{th(j-c)}$ is performed by holding the package against a water cooled heat sink, according with fig. 3. A thermocouple placed in contact with the slug measures the reference temperature of the case.

For junction to ambient thermal resistance $R_{th(j-a)}$ the samples are suspended horizontally in a one cubic foot box, to prevent drafts.

Both DC and pulsed conditions are used ; in the second case the contribution of package thermal capacitance is effective and transient thermal resistances much lower than the steady state $R_{th(j-a)}$ can be found, according with pulse length and duty cycle.

The effect of the external heat sink is quantified, using as test vehicle the commercially available heat sink THM7023 (Thermalloy) whose thermal resistance in still air is about 9°C/W.

The measurement circuit shown in fig. A3 was used for all of the thermal evaluations.

JUNCTION TO CASE THERMAL RESISTANCE

The dependance of $R_{th(j-c)}$ on the dissipated power is reported in fig. 4. The absolute value and the behaviour with the dissipated power are the same for

both packages as the slug thickness and the die - attach are equal.

Figure 3 : Measurement of $R_{th\ (j-c)}$.

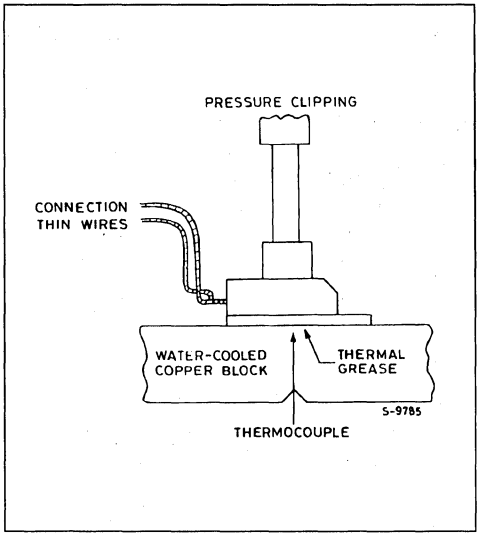
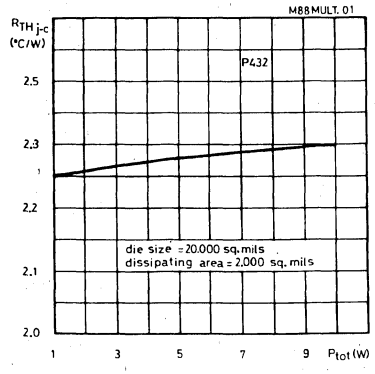


Figure 4 : $R_{th\ (j-c)}$ of Pentawatt and Heptawatt Package vs. Power Level.

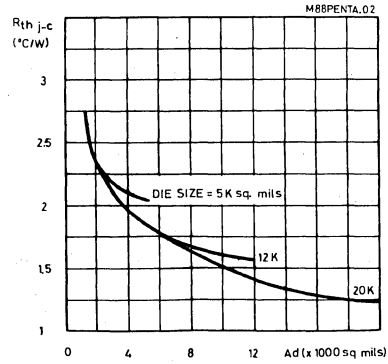


It is well known that the main contribution to $R_{th(j-c)}$ of power packages is given by the silicon die.

FOR OTHER DEVICES THAN THE TEST PATTERN P432 THE CALIBRATION CURVE OF FIG. 5 IS NEEDED.

It shows the relationship between $R_{th(j-c)}$ and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

Figure 5 : $R_{th\ (j-c)}$ Thermal Resistance vs. Die Size and on Die dissipating Area.



JUNCTION TO AMBIENT THERMAL RESISTANCE

In medium power application (1W), the Pentawatt and Heptawatt packages can be used without external heat sink thanks to the significant size (about 1.5cm^2) of its integrated thermal mass.

An effective cost solution for higher power application (1.5-2.0W) is using a copper area heat sink.

An board with the external leads bent down as shown in fig. 7.

Fig. 6 gives the relationship between $R_{th(j-a)}$ and the power dissipation level for the P432 test pattern in still air, on PC board, on integrated heat sink on board and on a commercial heat sink.

IN ORDER TO HAVE AN ACCURATE VALUE FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 6 SHOULD BE CORRECTED THROUGH THE CALIBRATION CURVE OF FIG. 5 CORRECTION TERM IS ALWAYS IN THE RANGE OF 0-2°C/W ; THEREFORE, IT AFFECTS THE $R_{th(j-a)}$ OF NO MORE THAN 5% IN STILL AIR OR WITH THE PACKAGE MOUNTED IN PC BOARD.

Figure 6 : $R_{th\ (j\text{-}a)}$ vs. dissipated Power (heptawatt).

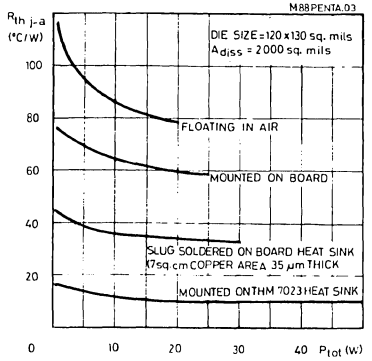
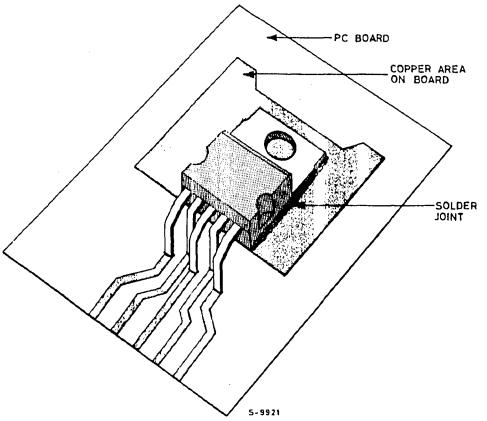


Figure 7 : Pentawatt Soldered on Copper Heatsink on P.C Board.

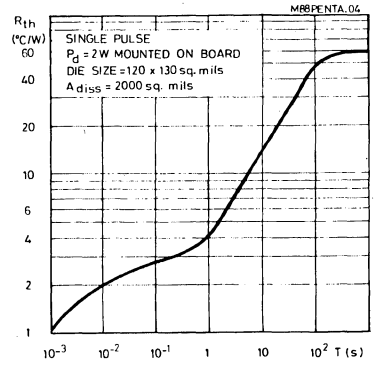


TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (without external heat sink)

The effect of single pulses of different length and height without any external heat sink is shown in fig. 8.

This behaviour is discussed in Appendix B. Due to a significant thermal capacitance (C = 1J/°C) and a correspondingly long risetime (τ = 80s), single pulses up to 20W can be delivered for 1 s with acceptable junction temperature increase.

Figure 8 : Transient Thermal Resistance for Single Pulses (heptawatt).

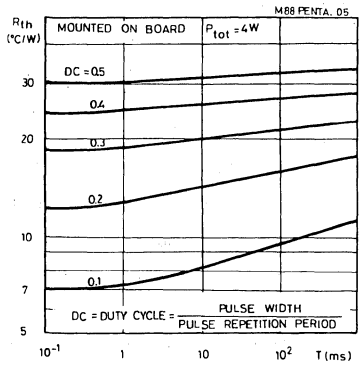


IN ORDER TO HAVE ACCURATE $R_{th}(t_o)$ FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 7 MUST BE CORRECTED AS DESCRIBED IN EXAMPLE 2 OF THE LAST SECTION.

Repetition of pulses with defined Pd, period and duty cycle DC (ratio between pulse length and signal period), gives rise to oscillations in junction temperature as described in Appendix B.

The transient thermal resistance corresponding to the upper limit of the curve of fig. B4 (peak transient thermal resistance) is reported in fig. 9 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

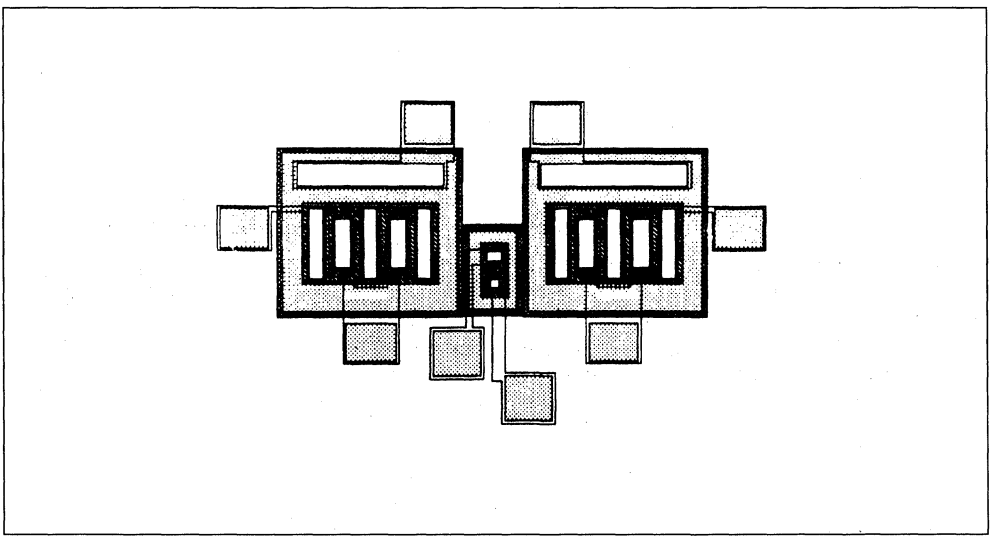
Figure 9 : Peak Transient R_{th} vs Pulse width and Duty Cycle (heptawatt).



APPENDIX A

The thermal resistance evaluation is performed with the especially designed test chip P432 which has two bipolar power transistor and one sending diode (fig. A1). The active area is about 2000 $mils^2$ on a 15000 $mils^2$ chip. Its lay-out was optimized in order to have a uniform temperature area, once the two transistor are powered ; the sensing diode is placed at the center of this area.

Figure A1 : Test Pattern P432 Lay-out.



The relationship between the forward voltage V_f of the diode at a constant current of 100µA and the temperature is shown in fig. A2. The curve calibrates the junction temperature through the voltage drop of the diode.

The measurement circuit is shown in fig. A3. A storage oscilloscope or a fast digital voltmeter can be used for recording the V_f value.

Figure A2 : Calibration Curve (sensing diode).

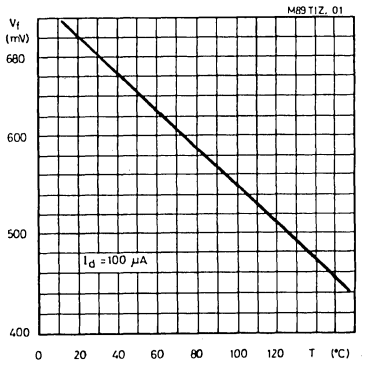
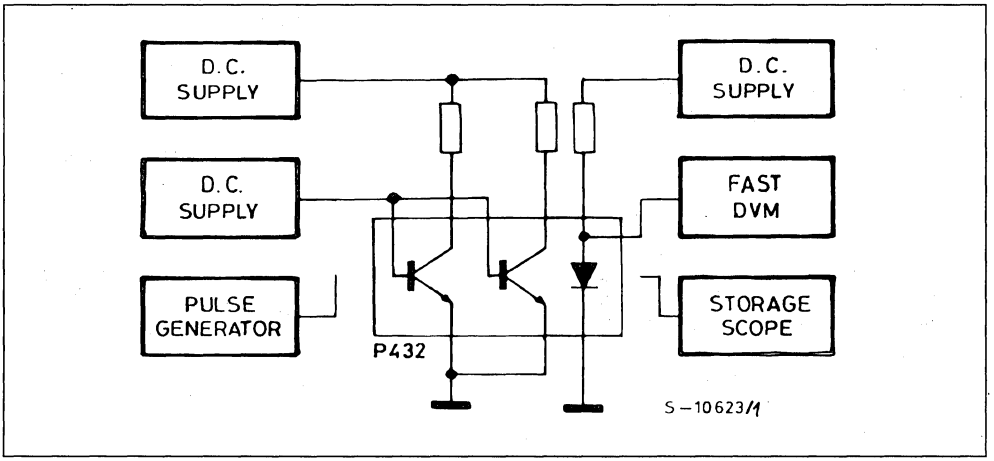


Figure A3 : Measurement Circuit.



APPENDIX B - THERMAL MANAGEMENT IN PULSED CONDITION

THERMAL RESISTANCE AND CAPACITANCE

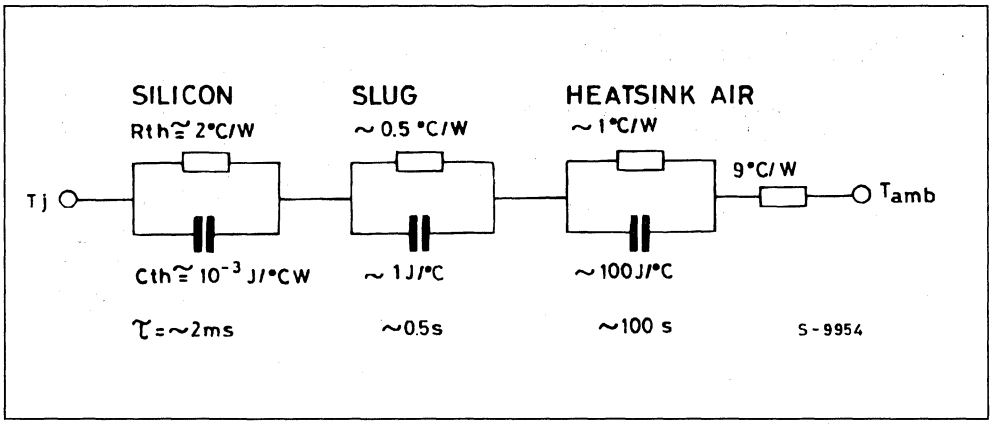
The electrical equivalent of heat dissipation, for a thermal module formed by the active device with its package and the external heat sink is shown in fig. B1.

To each cell of the thermal chain are associated a value of thermal resistance R_{th} (C/W) and a value of thermal capacitance C_{th} (J/°C). The former informs about temperature increase due to the element represented by the cell ; as, in the example under consideration, heat transfer is mainly based on conduction for the silicon, the copper integrated heat sink and to metallic body of the external heat sink Rth can be calculated from the relationship :

$$R_{th} = \frac{1}{K \times S}$$

Where K is the thermal conductivity of the material, 1 the length of the conductive path and S its section.

Figure B1 : Electrical Equivalent of Pentawatt and Heptawatt Package mounted on the External Heatsink.



Thermal capacitance C_{th} is the capability of heat accumulation ; it depends on the specific heat of the material and on the volume effectively interested by heat exchange (this means that the parts which are not heated during heat dissipation DO NOT contribute to thermal capacitance). Thermal capacitance is given by :

$$C_{th} = d \times c_t \times V$$

where d is the density of the material, c_t its specific heat and V the volume interested to heat accumulation.

The last element of the network, assumed as purely resistive, is due to convection and radiation from the external heat sink towards the ambient.

Each cell has its own risetime τ, given by the product of thermal resistance and capacitance :

$$\tau = R_{th} \times C_{th}$$

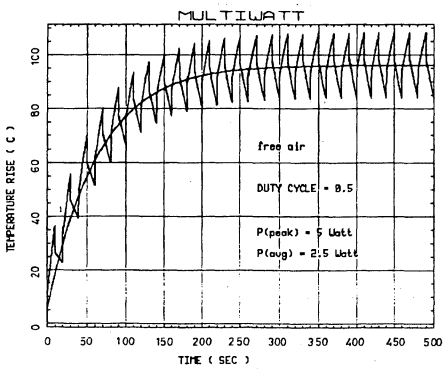
The value of the time constant determines whether a cell approaches equilibrium rapidly or slowly : if R_{th} or C_{th} increases, equilibrium is reached at a slower rate. The following relationship is valid for each cell :

$$\Delta T = R_{th} \times P_d \times [1 - e^{-t/\tau}] \quad (1)$$

Typical values of R_{th}, C_{th} and τ for Heptawatt and Pentawatt application are shown in fig. B1.

When power is switched on, temperature increase is ruled by subsequent charging of thermal capacitance while the value reached in the steady state depends on thermal resistance only. Qualitative beahaviour of the network of fig. B1 is shown in fig. B2.

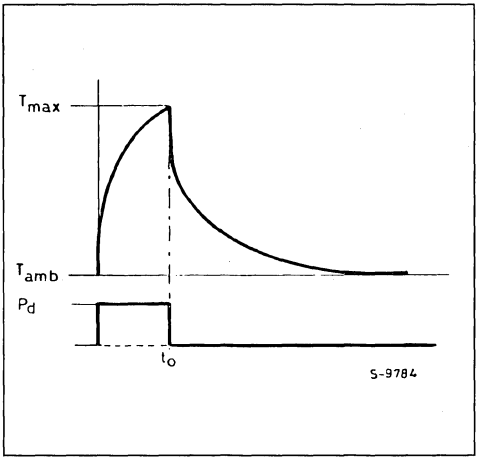
Figure B2 : Qualittative T_j increase (network of fig. B1) for repeated power pulse (heptawatt).



SINGLE POWER PULSE

When the pulse length has an assigned value, effective T_j can be significantly lower than steady state T_j (fig. B3.).

Figure B3 : Effect of a Single Power Pulse.



For any pulse length t_o, a transient thermal resistance R_{th} (t_o) is defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power. Obviously, for shorter pulses, R_{th} (t_o) is lower and a higher power can be dissipated, without exceeding the maximum junction temperature $T_{j\,max}$ allowed to the IC from reliability considerations. Fig. 7 and 9 of this Application Note give experimental values of R_{th} (t_o) for the two cases of the Heptawatt package without and with external heat sink.

REPEATED PULSES

When pulses of the same height Pd are repeated with a defined duty cycle DC and pulse length is short in comparison with the total risetime of the system (many tens of seconds) the train of pulses is seen by the system as a continuous source, at a mean power level of

$$P_{davg} = Pd \times DC$$

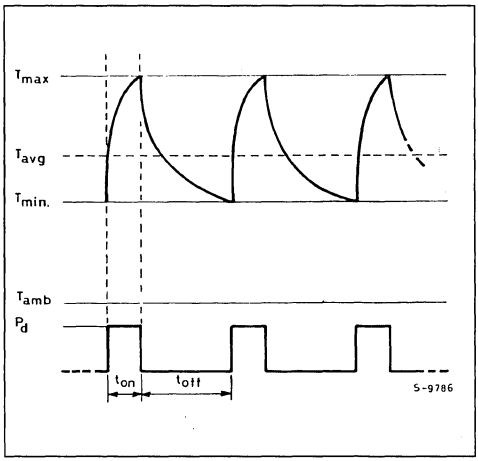
The average temperature increase is :

$$\Delta T_{avg} = R_{th} \times Pd_{avg} = R_{th} \times Pd \times DC$$

On the other hand, the silicon die ($\tau_{SI} = 1 \div 2ms$) is able to follow frequencies of some kHz and junction temperature oscillates about the average, as qualitatively shown in fig. B4.

The thermal resistance corresponding to the peak of the oscillation at equilibrium (peak thermal resistance $R_{th\,peak}$) is now given by fig. 5, and can be obtained if pulse length and duty cycle are known ; Pd_{max} is derived from the same figure.

Figure B4 : Junction Temperature increase for operated Pulses.



APPLICATION EXAMPLES

EXAMPLE 1 - MAXIMUM Pd FOR SINGLE PULSE OF ASSIGNED LENGTH

PROBLEM : define the maximum Pd for a single pulse with a length of 20ms in the case of Heptawatt package used without heat sink. Ambient temperature is 50°C ; maximum temperature is 130°C. Die size is 15k mils^2, with dissipating area of 2k mils^2 (as in P432 test pattern).

SOLUTION : allowed temperature increase ΔT is 80°C. Having a $R_{th(j\text{-}a)}$ of 60°C/W, Heptawatt package can dissipate about 1.3W in steady state From fig. 8 the transient thermal resistance corresponding to one single pulse of 20ms in R_{th} $(20ms)_{P432}$ = 2.2°C/W. A peak of 80/2.2 = 36.3W can be applied to the circuit.

EXAMPLE 2 - CORRECTION FOR DIE SIZE AND DISSIPATING AREA

PROBLEM : correct the results obtained in example 1, for assigned die size and dissipating area.

Pratical case : IC having a die size of 15k mils^2 with a dissipating area of 10k mils^2.

SOLUTION : from fig. 5, thermal resistance of P432 and of the IC under consideration are $R_{th\ P432}$ = 2.3°C/W and $R_{th(j\text{-}c)IC}$ = 1.5°C/W.

As the length of the pulse is 10-15 times longer than the risetime of the silicon, the die (first cell of fig. B1)

can be assumed to have reached its equilibrium condition.

R_{th} (20ms) found in previous example has to be corrected in order to take into account the new value of $R_{th(j-c)}$.

$$R_{th}\ (20ms)_{IC} = R_{th}\ (20ms)_{P432} - R_{th(j-c)P432} + R_{th(j-c)IC} =$$
$$= 2.2 - 2.3 + 1.5^{\circ}C/W = 1.4^{\circ}C/W$$

A single pulse of 80/1.4 ≡ 57W can be delivered to such a device.

EXAMPLE 3 - CORRECTION FOR SINGLE PULSES OF 1–3ms

PROBLEM : Correct the results of example 2, for pulse length of 1ms.

SOLUTION : when the pulse has the same order of magnitude of silicon rise time (τ_{P432} is about 1ms) another type of correction is needed. In first approximation it is considered that remains constant when the dissipating area gets higher and the Rth for the silicon die decreases as the reciprocal of the dissipating area. From relationship (1) :

$\Delta T = R_{th}\ (1ms)_{P432} \times 2K/10K \times Pd \times [1 - e^{-t/\tau}]$ for t_o = 1ms :

$$R_{thIC}\ (1ms) = 1.05/0.5^{\circ}C/W \equiv 0.21^{\circ}C/W$$

A single pulse of 80/0.21 ≡ 380W can be delivered to such a device.

EXAMPLE 4 - Rth REPEATED PULSES

PROBLEM : find the peak power which can be dissipated by Heptawatt package without heatsink, when power is continuously switched on 10ms and switched off 90ms. Ambient temperature is 50°C. maximum temperature is allowed to be 125°C.

SOLUTION : a maximum $\Delta T = 75^{\circ}C$ has to be considered. Fig. 9 indicated that for a pulse width of 10ms and a duty cycle of 0.1, Rth_{peak} is 8.5°C/W. Maximum Pd is 75/8.5 = 8.8W, with an average temperature increase ΔT_{peak} of 60 x 0.1 x 8.8 ≡ 68°C.

REFERENCES

"Improved thermal evaluation, by means of a simple integrated structure" T. Hopkins, C. Cognetti, R. Tiziani - SEMI THERM (USA, 1986).

RESISTANCE TO SOLDERING HEAT AND THERMAL CHARACTERISTICS OF PLASTIC SMDs

By C. Cognetti, E. Stroppolo and R. Tiziani

INTRODUCTION

Surface Mount Technology (SMT) has introduced a number of new technical problems, which have delayed the conversion from insertion assembly.

This is not strange : what readily available source of expertise existed a few years ago ?

Plastic SO packages were introduced in Europe in the early '70s and widely used in hybrids, but hybrid assembly has little relationship with the placement, soldering, handling tools now considered for SM PCB production. Was it surprising that even the semiconductor suppliers with sound experience in SO production could not give all of the answers needed by the PCB manufacturer ?

Japanese experience in SMT based consumer products is impressive : 87% of components used for cameras are in SM versions. However, the degree of complexity and performance of consumer products are somewhat different from the industrial, automotive and telecoms applications the Western world is interested in. On the other hand, in 1985 the percentage of SMDs (active and passive) used in industrial systems produced in Japan was 16.6% in telephones, 5.5% in automotive applications, 5.1% in cable communication, 0.7% in minicomputers[1] ; that is, a level similar to US and European production, presumably with a similar level of expertise.

In the past few years confidence in SMT has increased. More experience exists, which is the result of an expensive learning phase covered by both SMD manufacturers and users.

The reliability of plastic SMDs has an important place in this work. It needs a new approach in comparison with equivalent insertion devices, due to the completely different use.

In 14 years of production, no distinction was made in the authors' company between SO and DIP, from the point of view of reliability. They had the same reliability targets and similar evaluation methodology ; the former was often hot plate soldered on leaded ceramics for more convenient handling but no difference in long-term reliability existed.

With SMT, this is inadequate. Negative effects due to the various assembly processes, and to some thermomechanical influence of the board, can limit the device life.

The present work is focused on SMDs soldered onto a plastic substrate, by means of the most common industrial processes, and takes into account two aspects of reliability :

1. Resistance to soldering heat, i.e., the suitability to withstand the thermal shock associated with the soldering cycle, without reducing reliability. This information is obtained by performing moisture resistance tests. Data about SO packages will be presented. For PLCCs, evaluation is in progress and will be concluded in the first half of 1988.
2. Heat dissipation, which influences the failure rate. This information is obtained with test patterns and test boards designed by SGS-THOMSON Microelectronics and includes thermal impedance in pulsed conditions. A few case studies will be included in this paper but complete characterisations are available elsewhere.[2]

RESISTANCE TO SOLDERING HEAT

In through-hole technology, devices are inserted from the upper side of the board and wave soldered from its lower side.

Only the lead extremities reach the temperature (250-260°C) of the molten solder ; the maximum specified soldering time of 10s is short enough to avoid over-heating of the package body, which generally does not exceed 120-130°C during the whole process.

This temperature is lower than the moulding compound glass transition temperature (160-170°C) and the risk of permanent damage to the package structure or to the silicon die is excluded.

Device reliability is defined almost independently of the soldering time and temperature ; devices under reliability test are mounted on sockets, thus neglecting the effect of the assembly process.

On the contrary, in all industrial SMT processes, devices are soldered in a high temperature ambient (215-260°C), with high heating rate, and the plastic package is kept in glass transition conditions

(figure 1) for a relatively long time (up to 60s). This situation was never encountered before.

Concern over reduced reliability is justified and explains the trend towards defining SMD reliability *after* the soldering cycle, in order to include the effects summarised in table 1.

Figure 1 : Thermal Expansion of Moulding Compounds, Compared with the Temperature of Different Soldering Techniques.

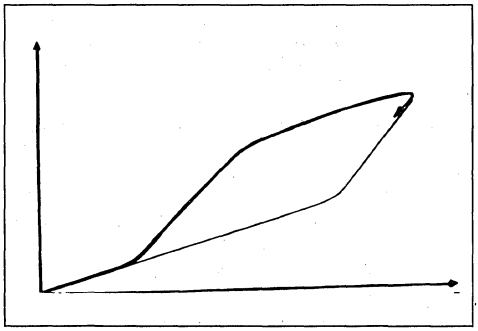


Table 1 : Factors Affecting SMD Reliability on Printed Board.

SMD Package	
Design and Structure	Volume and Thermal Inertia
Internal Contamination	Water Content
Thermomechanical Properties	Lead Solderability
Assembly Process	
Soldering Method	Contamination Level (flux)
Soldering Time/temperature	Rinsing
Substrate	
Thermomechanical Properties	Thermal Dissipation

EXPERIMENTAL

Reliability tests are performed on parts soldered onto test boards (4.5 in. x 6.5 in. FR-4 substrates).

SM PCB1 test board can accept SO-8, 14, 16. It is pre-grooved, in order to be cut in 35 positions, having the lay-out shown in figure 2 ; the SMD footprints are electrically connected to through-holes, with a pitch of 100 mils and placed in two parallel rows, 600 mils apart. Commercial pins inserted in the through-holes give the possibility of using the same equipment needed by DIPs.

The soldering processes from table 2 were used for SO packaged bipolar Operational Amplifiers and C-Mos Standard Logic. In order to simulate a rework, the soldering cycle was repeated on a number of devices. Soldering is followed by the usual rinsing in water or Freon, with or without ultrasonics.

Figure 2 : SM PCB1 Test Board.

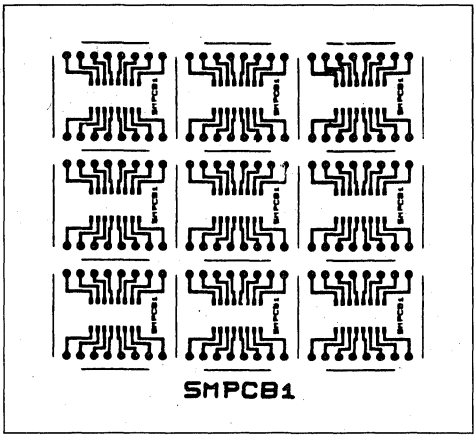


Table 2 : Soldering Processes Evaluated with SO Packaged Devices.

	Pre-heating	Soldering	Number of Cycles
Double Wave	120°C/30s	225°C/4s	1
Double Wave	120°C/30s	250°C/4s	1
Double Wave	110°C/30s	250°C/3.4s	1, 2, 3, 4
Triple Wave	110°C/30s	260°C/3s	1, 2, 3
Vapour Phase		215°C/20s	1, 2
Infra-red	160°C/30s	> 210°C/60s	1

The reliability evaluation was performed by means of the following tests :

Operating Life	150°C
Pressure Pot	121°C/2atm
THB	85°C/85% RH 15V (bips) 6V (CMos)
HAST	130°C/85% RH 15V (bips) 6V (CMos)
Thermal Cycles	– 55/+ 150°C (30/5/30 min)
Thermal Shocks	– 55/+ 150°C (5/1/5 min liquid)

130°C/85%RH Highly Accelerated Steam Test (HAST) has an acceleration factor of about 18-20 (ref. 3) in comparison with 85C/85%RH, and the concrete possibility of reaching wear-out exists with this test, after an acceptable time.

For PLCC packages a similar methodology is followed. At the time of writing, only partial data are available, which will not be included here.

EXPERIMENTAL RESULTS

Experimental results are summarised in tables 3-6.

Table 3 : Cumulative Reliability Data after Multiple Wave Soldering.

Test Vehicles : LM2904 (SO-8), LM2901 (SO-14) and M74HC74 (SO-14)		
Double Wave	225°C/4s	250°C/4s
Triple Wave		260°C/3s
Operating Life 1000h	0/154	0/32
Pressure Pot 96h	0/104	0/62
THB 85°C/85%RH 1000h 2000h	1/105*	0/32 0/32
HAST 130°C/85%RH 100h 200h		0/64 0/64
Thermal Shocks 500	0/231	0/77
* Parametric Failure		

Table 4 : Reliability Data after Vapour Phase Reflow.

Test Vehicle : LM2901 (SO-14)		
	215°C/20s	215°C/40s
Operating Life 1000h		0/32
Pressure Pot 96h		0/32
THB 85°C/85%RH 1000h 2000h		 0/32 0/32
HAST 130°C/85%RH V = 15V 100h 200h 372h 458h 635h	 0/56 0/56 0/24 2/24 5/22	 0/12 0/12 1/12 1/11 3/10
Thermal Cycles 500		0/32
All failures due to pad corrosion		

Table 5 : Cumulative Reliability Data after Infra-red Reflow.

Test Vehicles : M74HC00 and M74HC74 (SO-14)	
	> 210°C/60s
Operating Life 1300h	0/34
THB 85°C/85%RH 1300h	0/34
HAST 130°C/85%RH 100h 200h 500h 672h	 0/32 0/32 0/32 0/32
Thermal Cycles 750	0/70

Table 6 : Cumulative Reliability Data in Multiple Wave Soldering with Repetition of the Soldering Cycle.

Test Vehicles : LM2903 (SO-8), LM2901 and M74HC00 (SO-14)							
		Double Wave 250°C/3.4s			**Triple Wave 260°C/3s**		
Number of Cycles	1	2	3	4	1	2	3
Pressure Pot 96h 504h		 0/56 0/56					
100 Thermal Cycles (– 40/150°C) Followed by Pressure Pot 96h 168h 240h					 0/30 0/30 0/30	 0/30 0/30 0/30	 0/60 0/60 0/60
HAST 130°C/85%RH V = 6V 100h 500h 1000h 1150h 1300h	 0/32	 0/32	 0/32 0/18 0/18 1/18 17/17	 1/32* 0/18 0/18 1/18** 17/17**			
* Parametric Failure ** Pad Corrosion							

COMMENTS ON THE RELIABILITY RESULTS

Previous results do not reveal negative effects due to the exposure of SM devices to the soldering heat, for all of the industrial SMT soldering methods, in combination with the most common solders and cleaning solvents (Freon, water with and without ultrasonics).

Wear-out in the HAST test (130°C/85%RH) is between 1100 and 1300 hours when the soldering cycle is repeated up to 4 times with high temperature (250-260°C) multiple wave soldering, which is considered to transfer the highest thermal stress to the package body.

Pad corrosion is the final failure mechanism for all samples.

This performance is about 7-10 times better than the 2000-3000 h THB 85°C/85%RH, which is currently requested as qualification target in moisture resistance biased tests. Therefore, the reliability of surface mounted devices considered in this work is high enough to meet the most stringent requirements of the professional market.

No evidence of cracks in the plastic case was found in the previous evaluations. This effect (referred to also as 'pop corn' effect) is attributed to some anom-

alous thermal expansion of the package in the soldering phase, caused by water absorbed by the plastic encapsulation : a thermal treatment at a temperature higher than 100°C for a few hours is suggested in order to remove the absorbed water.[4]

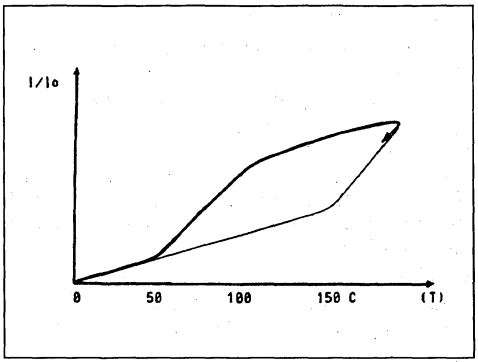
As this thermal pre-conditioning should be performed shortly before soldering, a serious problem arises in the assembly line. Such thermal annealing is not practical when the parts are supplied in plastic tapes or sticks : they should be removed from the packs by the user, heat treated, and packed again with additional costs and risks (co-planarity).

In this company's experience, the 'pop corn' effect can be completely avoided by controlling the frame-encapsulant interface, which is the easiest path for the water. Furthermore, experience has indicated that water at that interface does change the expansion characteristics of the package. About five years ago, the curve of figure 3 was found in some parts (coming from lots affected by the 'pop corn' problem) using Thermo-Mechanical Analysis (TMA). Devices under test were placed between the probes of the TMA transducer and their expansion characteristics recorded.

In the first ramp (5°C/min), package expansion was much higher than the moulding compound expansion between 50 and 100°C ; over 100°C, it returned on the curve typical of the encapsulant. Cooling down and repeating the measurement, only the lower curve of figure 3 was covered.

This behaviour was attributed to water having penetrated between the frame and the plastic body, whose expansion was responsible for the package deformation during the slow heating in TMA. When the parts were soldered on the substrate, cracks could occur due to the much faster heating rate.

Figure 3 : Thermal Expansion of SO Packages.



The problem was solved when the possibility of controlling the water content was found, by means of an improved frame design and some dedicated production steps.

Millions of parts assembled in recent years showed no evidence of the 'pop corn' effect, without any pre-conditioning before use.

The same solutions are successfully adopted for PLCC packages.

THERMAL CHARACTERISTICS

Correlation between reliability and junction temperature Tj is known :

the device lifetime is roughly halved when Tj is increased by 10°C.

Mainly due to this fact, thermal dissipation is a second factor which can influence SMD reliability : a reduced body means worse dissipation and higher power density on the board.

As careful thermal design is the key to improved reliability, a systematic characterisation of SM packages was performed, in order to study the main factors affecting thermal dissipation at both levels of package design and board design.

In the course of this work, the need for some critical revision of the way of producing and using thermal data was evident.

A point which cannot be under-evaluated is the choice of measurement method, as will be discussed later.

Another important point is the following : the common way of specifying the junction to ambient thermal resistance Rth(j-a) is to associate one value of Rth(j-a) to each device.

In the majority of data books, including this company's previous literature, little information is given on the experimental conditions used to obtain that value : the dissipated power and , above all, the kind of interconnection between the package and the measurement set-up (wires, socket or board), which in some cases can become a far from negligible heat transfer element.

Ignoring this contribution was probably justifie with packages having a low thermal conductivity frame, such as Alloy 42 or Kovar.

For those packages, heat spreading was limited to the silicon die and to the die pad ; thermal dissipation was little affected by the surroundings and the measurement assembly had little influence on the final value of Rth(j-a).

This is not the case concerning the same packages with a copper frame, introduced a few years ago to achieve a higher power capability ; due to better thermal conductivity of the leads they are much more sensitive to external dissipating media, eventually used for the measurement.

Similar statements are valid for SMDs and become more important on account of their reduced dimensions.

The concept is summarised in table 7, where the thermal resistance of some dual-in-line (DIP), Small Outline (SO) and Plastic Leaded Chip Carrier (PLCC) packages is given. The influence of the frame thermal conductibity is remarkable ; but likewise remarkable are the differences obtained for the same package, when it is connected by thin wires (and 'floating' in still air) or soldered on a PC board during the measurement.

Table 7 : Junction to Ambient Thermal Resistance (C/W) for DIP and SM Packages in Different Experimental Conditions.

	Power Pd[W]	'Floating' in Air	On SGS Test Board	Ratio
DIP 14 Leads (*)				
Alloy 42 0.25mm	0.5	156	138	1.13
Cu 0.25mm	0.6	125	90	1.39
SO-14 Leads (**)				
Alloy 42 0.25mm	0.4	280	195	1.43
Cu 0.25mm	0.6	190	105	1.80
PLCC-44 Leads (***)				
Cu 0.25mm	1.0	70	52	1.35
die size : (*) = 0.095 in. x 0.110 in. (**) = 0.060 in. x 0.090 in. (***) = 0.180 in. x 0.180 in.				

Especially for SO packages the influence of the substrate on thermal dissipation is noticeable. This fact can help to explain the following points :

1. The Rth(j-a) values published by different SMD suppliers are distributed in too wide a range (more than 70°C/W for SO packages) which handicaps a correct thermal design. Most of the difference is probably due to different test boards, and the availability of standardised measurement methodology should help to give more accurate information.
2. The board lay-out contribution should be studied, in order to quantify the effect of device density : a suitable distance between two or more dissipating elements can be an effective solution for improved reliability.
3. Specification of thermal characteristics should include more elements (power level, board density, package design) which cannot be summarised in one single thermal resistance value, as was commonly the case with Alloy 42 DIPs.

A set of experimental curves was obtained for each SM package,[2] which gives the relationship between these factors ; if used to feed back the board design, they should help to achieve a better thermal performance.

The most significant results will be discussed here.

Moreover, two other factors will be considered.

1. The thermal capacitance of the package, which is significant especially in higher pin count PLCCs ; it delays Tj increase during power transients and is important in switching applications.
2. The frame design in association with a suitable board design ; a low resistance thermal path can be obtained with modified frames ; heat is then conveyed to copper areas obtained on the board and dissipated power can be increased to 2W with SOs and PLCCs.

EXPERIMENTAL METHOD

When thermal measurements on plastic packages are performed, the first consideration is the lack of a standard method : at present, only draft specifications[5] exist, proposed in 1986 and not yet standardised.

The experimental method used in this company since 1984 has anticipated these preliminary recommendations to some extent, as it is based on the P432 thermal test pattern (figure 4) having two npn transistors, with 10W each power capability. A sensing diode is placed on the thermal plateau arising when the transistors are operating in parallel and gives the actual value of Tj, through the calibration curve of its forward voltage Vf (at constant current) vs temperature.

Transistor size, which is not fixed by the documents proposed for standardisation, was intentionally limited to 1000 mils^2, in order to simulate a high power density and characterise the worst case. Die size, which is found to have some influence on thermal resistance when copper frame is used, is slightly smaller than the die pad size and never exceeds 30000 mils^2 in larger packages, such as high pin count PLCCs.

The measurement set-up is shown in figure 5. It is compatible with DC and AC power supply and has an accuracy better than 5%.

The advantages offered by the test pattern are :

(i) high power capability (wider evaluation range) ;

(ii) repeatable electrical characteristics (Vf) and temperature coefficient (1.9mV/C) of the sensing element (accuracy) ;

(iii) high resolution in pulsed conditions (evaluation down to 100s pulses) ;

(iv) better correlation from one package to another.

Alloy 42 frames and copper frames were used for narrow SO packages (150 mils body) ; only copper frames were considered for the others : wide SO (300 mils body) and PLCC packages.

Suitable FR-4 test boards were developed, which will be described case by case.

Figure 4 : Test Pattern P432 Layout.

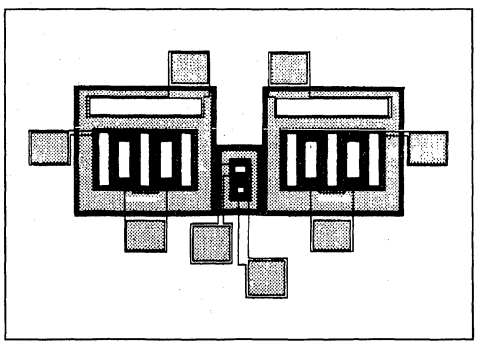
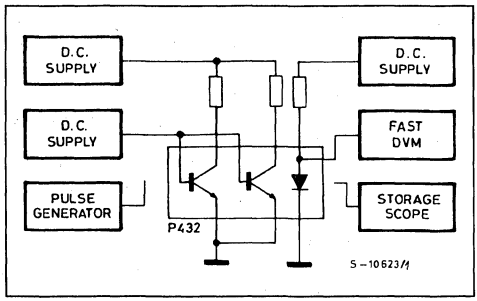


Figure 5 : Measurement System.



THERMAL CHARACTERISTICS IN DC CONDITIONS

Thermal characteristics of the SO-14 package in DC conditions are shown in figure 6.

The upper curve is related to samples floating in still air and connected to 8 thin wires needed for biasing the dissipating transistors and the sensing diode of the P432 test pattern.

Samples soldered on the FR-4 test board shown in figure 2 have an approximately halved thermal resistance ; by reducing the copper pattern length of the test board, different component densities are simulated : thermal resistance is increased by about 30% when the track length has the minimum value.

Dependence of the thermal resistance on the total area of the traces connected to the package is represented by the curve of figure 7. It quantifies the effectiveness of the board lay-out to spread the heat and dissipate it towards the ambient and can be conveniently used for determining the thermal resistance value associated with a given board design.

Figure 6 : Rth(j-a) of SO-14 Package vs. Power Level.

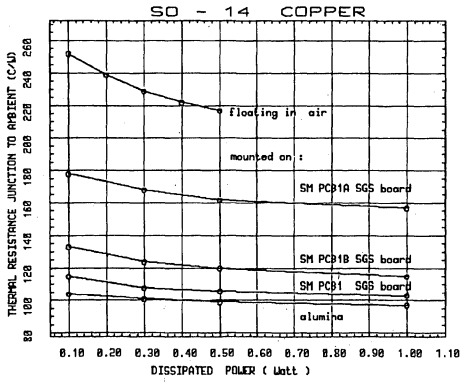


Figure 7 : Rth(j-a) of SO-14 vs. on Board Trace Area.

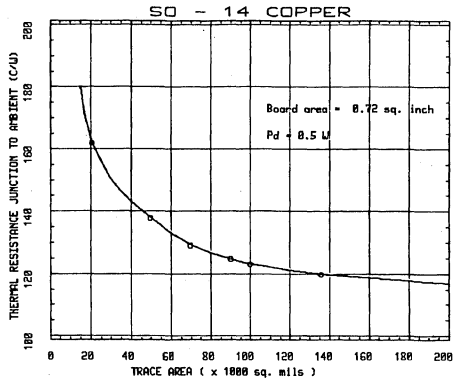
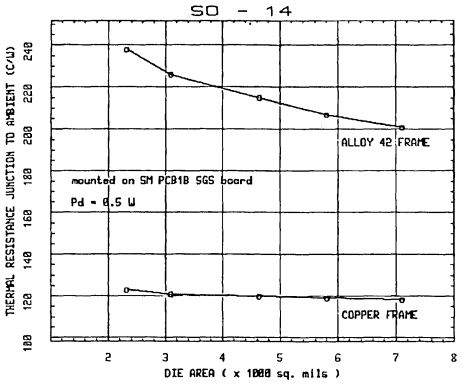


Figure 8 : Rth(j-a) of SO-14 with Copper (SGS-THOMSON) and Alloy 42 Frame.



Comparison of low conductivity (Alloy 42) and high conductivity (copper) frames is shown in figure 8.

The data obtained for the different SM packages are summarised in table 8 ; the two thermal resistance values refer to the two extreme cases of a low density and a high density board.

Table 8 : Summary of Junction to Ambient Thermal Resistance in Steady State Power Dissipation (SGS-THOMSON test boards)

	Die Pad Size (milinches)	**Power Pd [W]**	**Rth(j-a) [°C/W] on Board**
SO-8 Alloy 42	90 x 100	0.2	250-310
Copper	95 x 100	0.2	160-210
SO-14 Alloy 42	98 x 118	0.3	200-240
Copper	78 x 118	0.5	120-160
Copper	98 x 125	0.7	105-145
SO-16 Alloy 42	98 x 118	0.3	180-215
Copper	94 x 185	0.5	95-135
SO-16W Copper	120 x 160	0.7	90-112
SO-20 Copper	140 x 220	0.7	77-97
PLCC-20 Cu	180 x 180	0.7	90-110
PLCC-44 Cu	260 x 260	1.5	50-60
PLCC-68 Cu	425 x 425	1.5	40-46
PLCC-84 Cu	450 x 450	2.0	36-41
Rth(j-a) values correspond to low and high board density			

THERMAL IMPEDANCE IN PULSED CONDITIONS

The electrical equivalent of heat dissipation for a module formed by the active device, its package, the board and the external ambient is a chain of RC cells each having a characteristic risetime $\tau = RC$.

Thermal capacitance is the capability of heat accumulation and depends on the heat capacitance of the materials, their volume and their density.

When the power is switched on, the junction temperature after a time t is the result of the subsequent charge of the RC cells, according to the well known exponential relationship :

$$\Delta T_j = Rth \times Pd \times (1 - et/\tau)$$

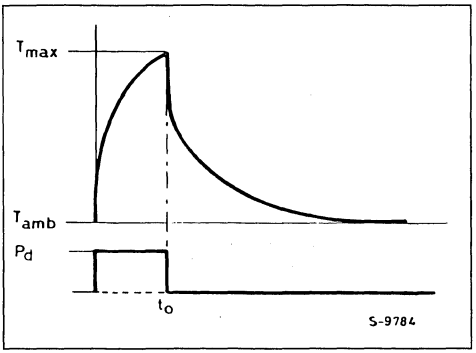
When the pulse length t_o is an assigned value, effective T_j can be significantly lower than the steady state T_j (figure 9) and a transient thermal resistance $Rth(t_o)$ can be defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power.

Obviously, for shorter pulses, transient thermal resistance is lower and a higher power can be dissipated without exceeding the maximum junction temperature defined in reliability considerations.

In a similar way, when pulses of the same height Pd are repeated with a defined duty cycle DC and the pulse is short in comparison with the total risetime of the system, the train of pulses is seen as continuous source at a mean power level :

$$Pd_{avg} = Pd \times DC$$

Figure 9 : Qualitative Tj Increase for Single Power Pulse.



On the other hand, the silicon die has a risetime of 1-2ms and is able to follow frequencies of some kHz : junction temperature oscillates about the average value :

$$\Delta T_{javg} = Rth \times Pd_{avg}$$

as qualitatively shown in figure 10.

The thermal resistance corresponding to the peak of the oscillation at the equilibrium (peak thermal resistance) gives information on the maximum temperature reached by the device and, depending on DC and pulse width, can be much lower than DC thermal resistance.

Figure 10 : Qualitative Tj Increase for Repeated Power Pulse.

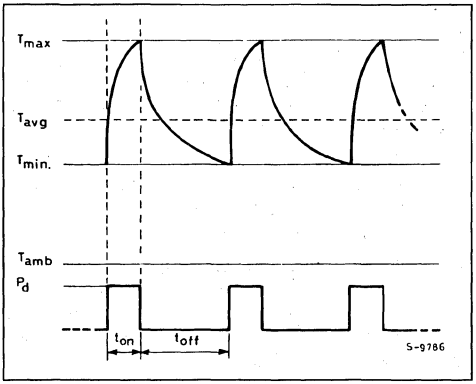
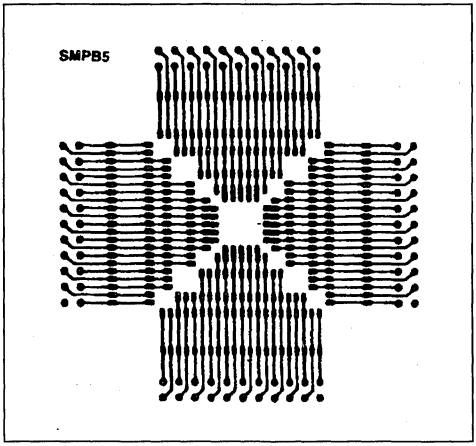
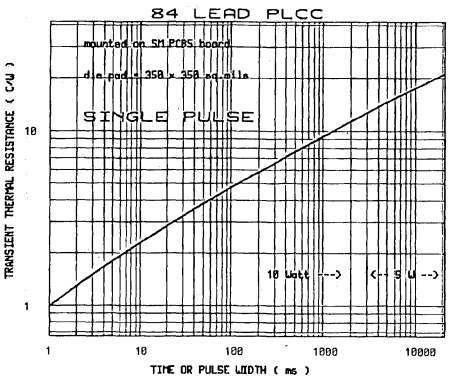


Figure 11 : Test Board for PLCC.



The knowledge of thermal characteristics in the AC condition is a valid tool to reduce redundancy (and cost) in the thermal design of pulsed applications.

Figure 12 : Transient Thermal Resistance for PLCC-84 on Board.



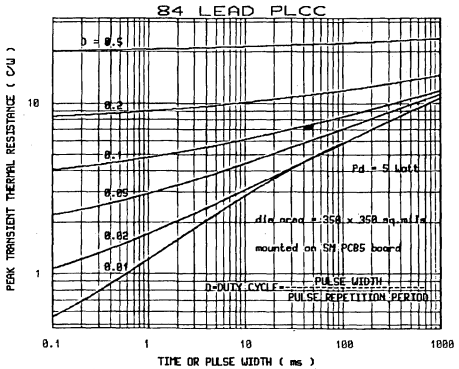
The example is now given of a high pin count PLCC, which has a large thermal capacitance, due to its volume and weight.

Temperature increase for 84 lead PLCCs soldered on the SM PCB5 test board (figure 11) for single pulses of different length is given in figure 12. A risetime of 50-60s is typical for this package, having a thermal resistance of 38°C W in steady state (see table 8).

For single pulses, the effective thermal resistance is much reduced and acceptable junction temperature is observed even for high power pulses. 10W can be delivered for about 1s (9°C/W) and 5W for 10s (18°C/W).

Peak thermal resistance for repeated pulses, with different duty cycles, is represented in figure 13 and the above considerations are valid in this case also.

Figure 13 : Peak Transient Rth for PLCC-84 on The Board.



MEDIUM POWER APPLICATION

The lack of power packages suitable for SMT requirements (standard outline, automatic handling) is known.

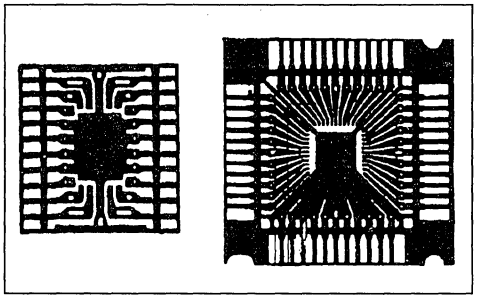
A simple way to achieve power dissipation in the medium range (1-2W) is to transform the available signal packages and modify their frame to obtain a high conduction path.

In figure 14 the frame of medium power SO and PLCC packages is shown : some leads are connected to the die pad, in order to have a low junction-to-pin thermal resistance Rth(j-p). Typical values of this parameter are in the range of 12-15°C/W, with a high conductivity lead frame.

Modification involves the internal part of the frame only, while the external dimensions of the package are not changed ; the solution offers the undoubted advantage of being compatible with existing handling and testing tools.

The heat produced by the IC, and conveyed externally by the heat transfer leads, can be cost effectively transferred to the ambient by means of dedicated copper heatsinks, integrated on the board.

Figure 14 : Medium Power SO and PLCC Frame.



In figure 15, the layout of test boards used for the thermal characterisation of medium power SO-20s (with 8 heat transfer leads) and PLCC-44s (with 11 heat transfer leads) is represented.

The area of the integrated heatsink can be optimised for cost reduction, depending on the dissipation level. In figure 16 the relationship between the Rth(j-a) of the PLCC (33 + 11) and the total dissipating area is given.

It can be noticed that, with 6-7 sq cm of substrate, the thermal resistance of PLCC-44s can be decreased from 55°C/W to 40°C/W, for 1.5-2W dissipation.

A similar performance is possible with the medium power SOs.

Figure 15 : Test Boards for Medium Power SO-20 and PLCC-44 Package.

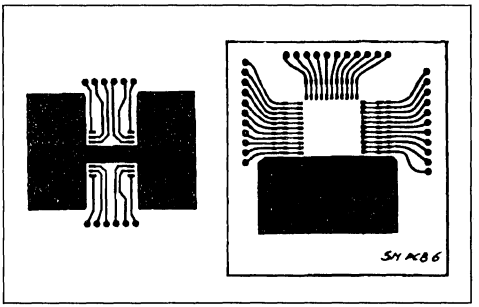
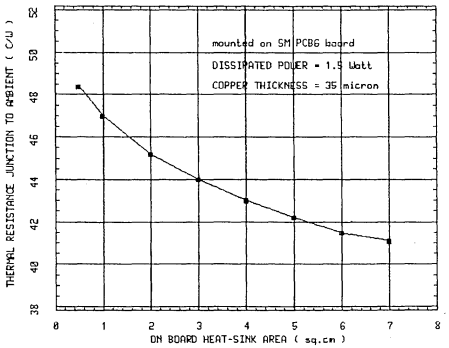


Figure 16 : Rth(j-a) of Medium Power PLCC-44 vs. Dissipating Area on Board.



CONCLUSIONS

In SMT, two main reliability related concerns are resistance to soldering heat and heat dissipation.

RESISTANCE TO SOLDERING HEAT

After extensive evaluation of devices soldered on plastic substrates by means of the three industrial soldering methods (multiple wave soldering, vapour phase and IR reflow), no reliability degradation was found.

The following soldering conditions are possible with SO packaged devices :

- Multiple Wave : T = 250 - 260°C/t = 4s (repetition allowed)
- Vapour Phase : T = 215°C/t = 20s (repetition allowed)
- Infra-red : T > 210°C/t = 60s (Tmax = 225°C)

No crack in the plastic case was evidenced during the above work or in the field, in recent years of production, and no thermal preconditioning was needed. However, this result was obtained after optimisation of the frame design and of the production process. Its extension to the totality of the products existing on the market might be too arbitrary, but it is possible to conclude that the structure of SM packages, when associated with suitable materials and processes, is able to meet the user's requirements.

A similar evaluation is running for PLCC packages and will be completed in the first half of 1988.

HEAT DISSIPATION

Some considerations have been made about the consequence of the lack of some standard evaluation methodology. To standardise test chips and test boards is very important, in order to reach a better knowledge and a better information exchange.

By means of an internally developed test pattern and suitable test boards, three points have been studied :

1. The influence of the substrate on thermal dissipation, whose effect has to be taken into account much more than for insertion packages. With a proper layout it is effective in reducing thermal resistance. For example, dissipation of copper frame SO package can become better than the equivalent Alloy 42 DIP and only 10-20% higher than the equivalent copper DIP.
2. The thermal impedance, whose value is much more suitable for the thermal design of switching applications and can contribute to reduce the cost of the system.
3. The new medium power SO and PLCC packages, which offer the possibility of cost-effective power dissipation in the range of 1.5-2W, still maintaining a standard outline.

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2. SGS-THOMSON Application Notes 106 to 110 on SO-8, 14, 16, 16W, 20 and PLCC-20, 44 (33 + 11), 68, 84.
3. Peck. D. S., 'Comprehensive Model for Humidity Testing Correlation', Proceedings IRPS, p. 44 (1986).
4. Fukuzawa, 1. et al, 'Moisture Resistance Degradation of Plastic LSI by Reflow Soldering', Proceedings IRPS, p. 192 (1985).
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SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

HANDLING AND MOUNTING ICs IN PLASTIC POWER PACKAGES

Integrated circuits mounted in plastic power packages can be damaged, or reliability compromised, by inappropriate handling and mounting techniques. Avoiding these problems is simple if you follow the suggestions in this section.

Advances in power package design have made it possible to replace metal packages with more economical plastic packages in many high power applications. Most of SGS-THOMSON Microelectronics power driver circuits, for example, are mounted in the innovative MULTIWATT® package, developed originally for high power audio amplifiers. Though the intrinsic reliability of these packages is now excellent the use of inappropriate techniques or unsuitable tools during mechanical handling can affect the long term reliability of the device, or even damage it. With a few simple precautions, careful designers and production engineers can eliminate these risks, saving both time and money.

BENDING AND CUTTING LEADS

The first danger area is bending and cutting the leads. In these processes it is important to avoid straining the package and particularly the area where the leads enter the encapsulating resin. If the package/lead interface is strained the resistance to humidity and thermal stress are compromised, affecting reliability.

There are five basic rules to bear in mind :

- Clamp the leads firmly between the package and the bend/cut point (figure 1).
- Bend the leads at least 3mm from the package (figure 2a).
- Never bend the leads more than 90° and never bend more than once (figure 2b).
- Never bend the leads laterally (figure 2c).
- Make sure that he bending/cutting tool does not damage the leads.

Figure 1 : Clamp the Leads between the Package and Bend/cut Point.

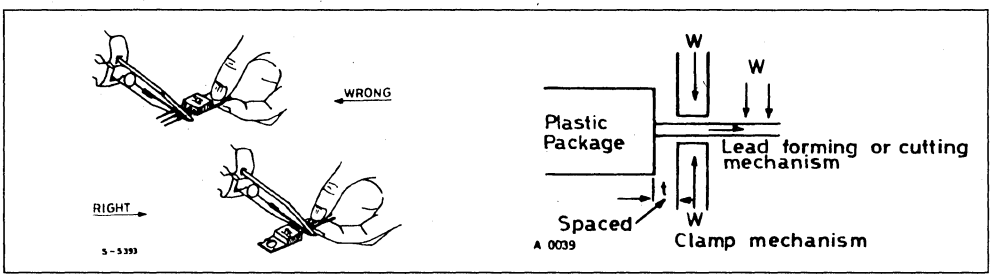
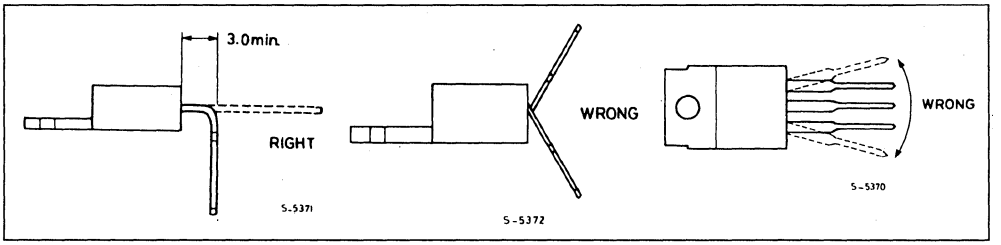


Figure 2 : Bend the Leads at Least 3mm. from the Package, never Bend Leads more than 90° and never Attempt to Splay the Leads Out.



INSERTION

When mounting the IC on a printed circuit board the golden rule is, again, to avoid stress. In particular :

- Adhere to the specified pin spacing of the device ; don't try to bend the leads to fit non-standard hole spacing.
- Leave a suitable space between the IC and the board. If necessary use a spacer.
- Take care to avoid straining the device after soldering. If a heatsink is used and it is mounted on the PC board it should be attached to the IC before soldering.

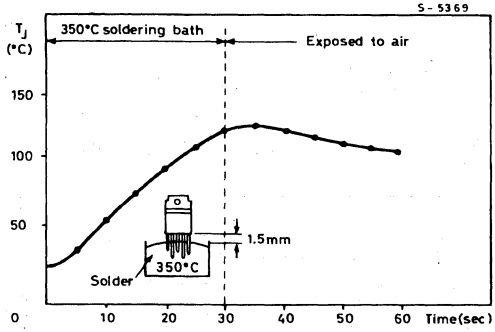
SOLDERING

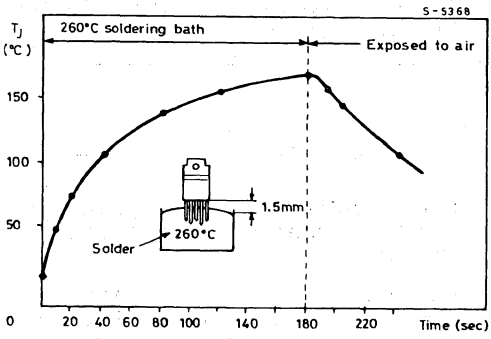
The greater danger during soldering is overheating. If an IC is exposed to high temperature for an excessive period it may be damaged or reliability reduced.

Recommended soldering conditions are 260°C for ten seconds or 350°C for three seconds. Figure 3 shows the excess junction temperature of a PENTAWATT package for both methods.

It is also important to use suitable fluxes for the soldering baths to avoid deterioration of the leads or package resin. Residual flux between the leads or in contact with the resin must be removed to guarantee long term reliability. The solvent used to remove excess flux should be chosen with care. In particular, trichloroethylene (CHCl : CCl_2) - base solvents should be avoided because the residue can corrode the encapsulant resin.

Figure 3 : The Excess Junction Temperature of a PENTAWATT Package in the suggested Soldering Conditions.





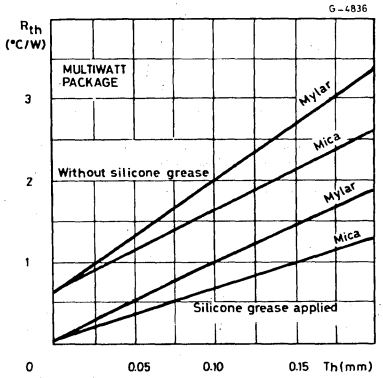
HEATSINK MOUNTING

To exploit the full capability of a power device a suitable heatsink must be used. The most important aspect from the point of view of reliability is that the heatsink is dimensioned to keep the junction temperature as low as possible. From a mechanical point of view, however, the heatsink must be designed so that it does not damage the IC. Care should also be taken in attaching the IC to the heatsink.

The contact thermal resistance between the device and the heatsink can be improved by adding a thin layer of silicon grease with sufficient fluidity to ensure uniform distribution. Figure 4 shows how the thermal resistance of a MULTIWATT package is improved by silicone grease.

An excessively thick layer or an excessively viscous silicon grease may have the opposite effect and could cause deformation of the tab.

Figure 4 : The Thermal Resistance of a MULTIWATT Package is improved by Silicon Grease. Here Thermal Resistance is plotted against Grease Thickness.



SGS-THOMSON plastic power packages - MULTIWATT, PENTAWATT and VERSAWATT - are attached to the heatsink with a single screw. A spring clip may also be used as shown in figure 5. The screw should be properly tightened to ensure that the package makes good contact with the heatsink. It should not be too tight or the tab may be deformed, breaking the die or separating the resin from the tab.

The appropriate tightening torque can be found by plotting thermal resistance against torque as shown in figure 6.

Suggested tightening torques for 3MA screws are 8Kg/cm for VERSAWATT, PENTAWATT and MULTIWATT packages. If different screws, or sping clips, are used the froce exerted by the tab must be equivalent to the force produced with these recommended torques.

Even if the screw is not overtightened the tab can be deformed, with disastrous results. If the surface of the heatsink is not sufficiently flat. The planarity of the contact surface between device and heatsink must be better than 50µm for PENTAWATT and VERSAWATT packages and less than 40µm for MULTIWATT packages.

Figure 5 : MULTIWATT, PENTAWATT and VERSAWATT Packages are attached to the Heatsink with a Single Screw or a Spring Clip.

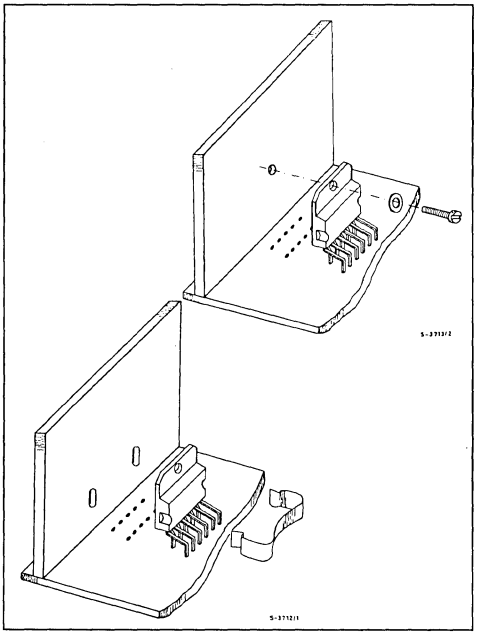


Figure 6 : Contact Thermal Resistance depends on Tightening Torque.

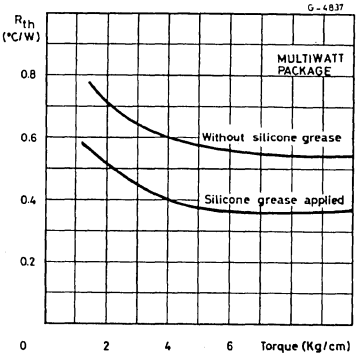
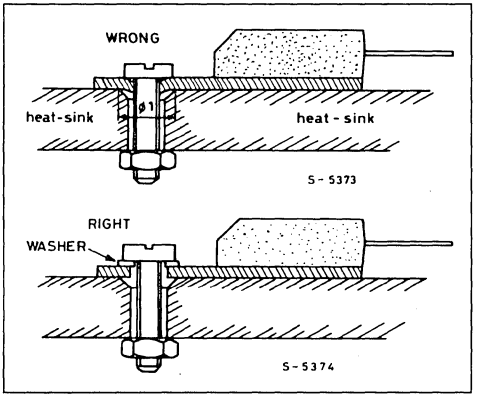


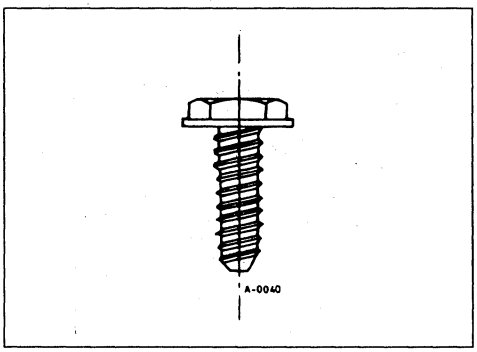
Figure 7 : The Heatsink Tab may be deformed it a Washer or a Wide-headed Screw is not used.



Similar problems may arise if the screwhead is too narrow compared to the hole in the heatsink (figure 7).

The solution here is to use a washer to distribute the pressure over a wider area. An alternative is to use screws of the type shown in figure 8 which have a wide flat head. When self-tapping screws are used it is also important to provide an outlet for the material deformed as the thread is formed. Poor contact will result if this is not done. Another possible hazard arises when the hole in the heatsink is formed with a punch : a circular depression may be formed around the hole, leading to deformation of the tab. This may be cured by using a washer or by modifying the punch.

Figure 8 : The recommended Screw Type Looks Like this.



Serious reliability problems can be encountered if the heatsink and printed circuit board are not rigidly connected. Either the heatsink must be rigidly attached to the printed circuit board or both must be securely attached to the chassis. If this is not done the stresses and strains induced by vibration will be applied to the device and in particular to the lead/resin interface. This problem is more likely to arise when large boards and large heatsinks are used or whenever the equipment is subjected to heavy vibrations.

TO 220AB - TOP 3 - TOPLESS THERMAL RESISTANCE AND MECHANICAL ASSEMBLY

By O. DELA PATELLIERE

The behaviour of a semiconductor device is directly related to the temperature of its silicon chip.

To preserve the performances of the component and to ensure optimal reliability, is to limit temperature by mastering the heat transfer between the chip and the ambient atmosphere.

The purpose of this note is to underline the importance of the mechanical assembly of the component on its heat sink by comparing different possibilities.

A - IMPORTANCE OF THE MECHANICAL ASSEMBLY

1 - THERMAL RESISTANCE

Review : The thermal resistance (R_{th}) of a semiconductor assembly is the parameter which characterizes its aptitude to channel the heat flow generated by the junction during operation.

It is expressed by : $R_{th} = \frac{\Delta T\ (°C/W)}{P}$

Where P is the power dissipated by the component.

When a semiconductor component is assembled on a heat sink, the total thermal resistance should be taken into account. It is given by the following equation

Thermal resistance between junction and case

$$R_{th(j-c)} = \frac{T_j - T_c}{P}$$

T_j : Junction temperature

T_c : Case temperature

This value is specified in the data sheets and it varies according to the type of component.

Thermal resistance between case and heat sink or contact thermal resistance.

$$R_{th(c-h)} = \frac{T_c - T_h}{P}$$

T_h : Heat sink temperature

Thermal resistance between heat sink and ambient air.

It is related mainly to the quality of the contact.

$$R_{th(ha)} = \frac{T_h - T_a}{P}$$

T_a : Ambient temperature

The thermal balance is expressed by the equation :

$T_j - T_a = P \times R_{th(j-a)}$

where the thermal resistance between junction and ambient air is :

$R_{th\ (j-a)} = R_{th\ (j-c)} + R_{th\ (c-h)} + R_{th\ (h-a)}$

This equation of thermal balance helps to calculate the junction temperature of the component.

A junction temperature which approaches the maximum temperature of the component could lead to a decrease in the electrical characteristics and a reduction of the safety margin. A temperature exceeding the maximum junction temperature risks damaging the semiconductor device. The junction temperature should be known at all times.

2 - TYPES OF ASSEMBLY

The conventional assemblies can be divided into two types :

- assembly on heat sink,
- assembly in the air (without heat sink).

The choice of the assembly results in a compromise between the following criteria :

- convenience of use : the component should be connectable and accessible for testing or replacement,
- cost,
- possibility of heat dissipation,
- mechanical resistance,
- aging and fiability.

TYPES OF ASSEMBLY AS A FUNCTION OF THE POWER (P) AND THE TYPE OF CASE USED BY THE COMPONENT.

Power Range	Types of Cases			Types of Assembly
$P \geq 50$ W	TOP 3			Heat Sink with Cooling Fins
2 W < P < 50 W	TO 220	TOP 3		Plain Heat Sink
$P \leq 2$ W	TO 220	TOP 3	TOPLESS	Assembly in the Air (printed circuit board)

B - ASSEMBLY OF TOP 3 AND TO 220 ON HEAT SINKS

Among the various parameters of assembly on heat sinks, three are particularly important :

- the shape and condition of the heat sink surface,
- the pressure of the component on the heat sink,
- the contact grease (different types exist).

The layer spread on the flat heat sink surface should be thin and uniform.

The $R_{th\,(c-h)}$ of contact without grease $\approx 1.5 R_{th\,(c-h)}$ of contact with grease.

1 - ATTACHMENT BY SCREW (figure *1*)

Example : TO 220

$R_{th\,(c-h)} = 2°C/W$ for F = 25N

$R_{th\,(c-h)} = 1.5 \times 2 = 3°C/W$ for F = 5N

with F = force

Advantages

- good mechanical resistance
- easy and quick disassembly
- easy to perform for short series.

Figure 1 : Attachment of the TO 220 or TOP 3 (insulated) by M3 Screw.

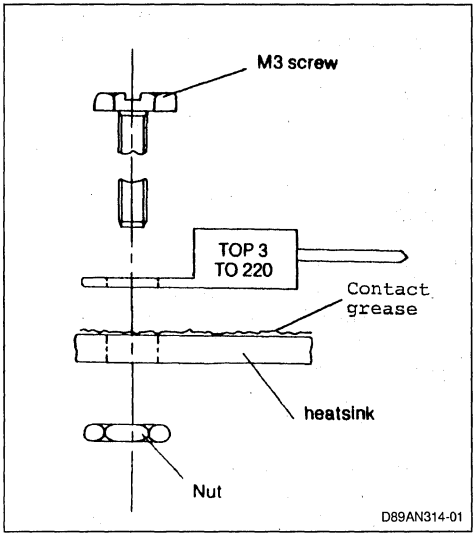
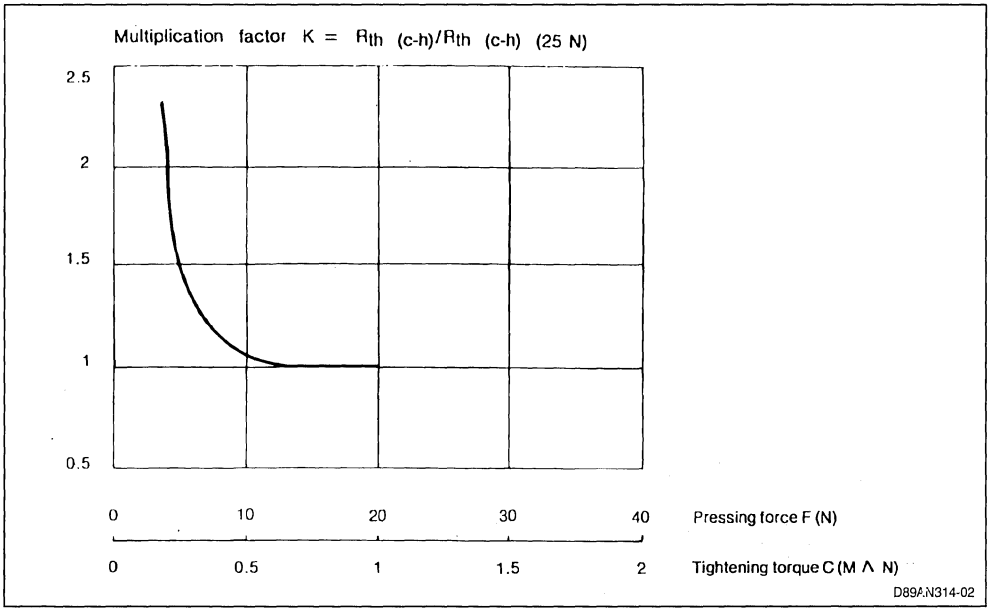


Figure 2 : Relative Variation of the Thermal Resistance of the Contact as a Function of the Pressure and the Tightening Torque for an M3 Screw like Figure 1.



The contact thermal resistance of assembly by screw changes with the pressure of the case on the heat sink. This force depends on the tightening torque (*figure 2*).

Disadvantages :

- deburring of the heat sink hole
- mastering of the screw tightening torque
- assembly not suitable for long series.

2 - ATTACHMENT BY RIVET (*figure 3*)

Advantages :

- good mechanical resistance
- quick assembly suitable for long series

Disadvantages :

- difficult to disassemble
- risk of deforming the plastic case during assembly
- deburring of the attachment hole
- difficult to master the force applied by the riet.

3 - ATTACHMENT BY CLIP

Two types of assembly by clip exist : (*figures 4a and 4b*)

Figure 3 : Attachment of the TO 220 or TOP 3 (insulated) by Rivet.

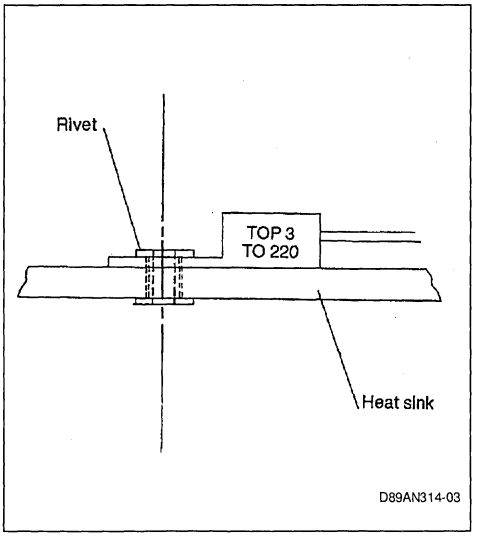
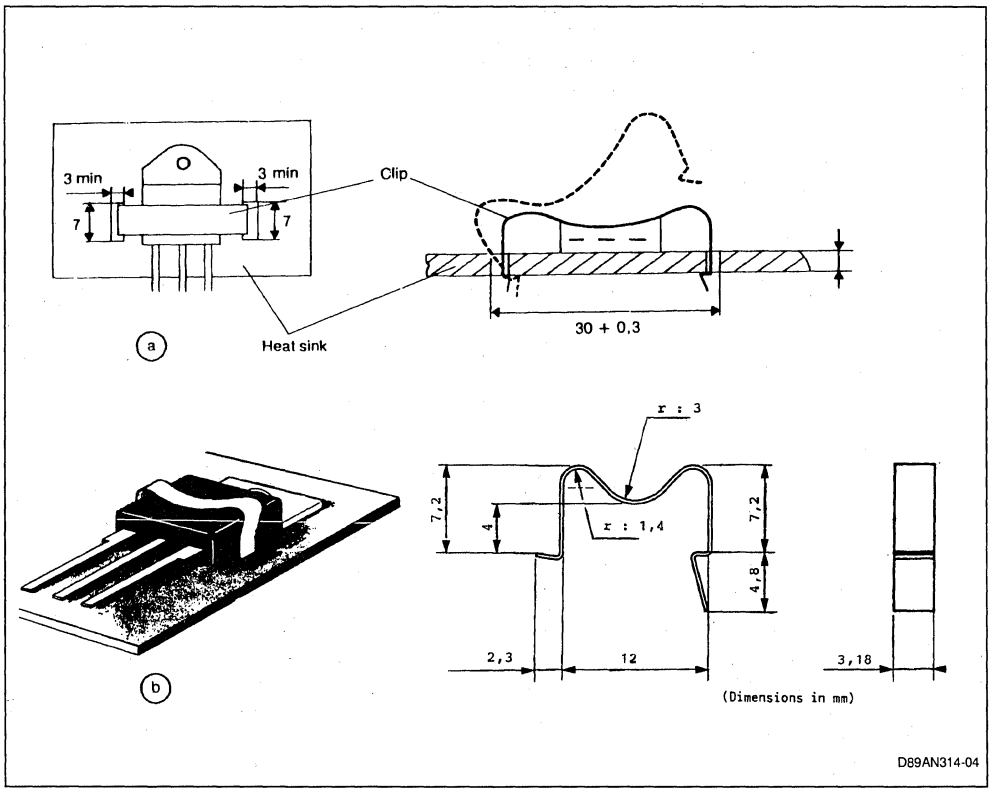


Figure 4 : Example of Attachment by Clip a. for TOP 3 (ref. mP 18055) b. for TO 220.



Advantages :

- rapidity of assembly and disassembly (automatization),
- low cost,
- facility in controlling the pressure exercised by the component on the heat sink,
- stability in time.

Example :

Clip MP 18055

F = 20N

Disadvantages :

- difficulty in positioning the case with respect to the heat sink.

N.B. : The fact of using a non-insulated component for an application in which the case should not be at the same potential as the heat sink makes the use of an insulator necessary (mica).

This insulator whose thickness is about 0.1 mm introduces an additional thermal (contact) resistance of :

- $R_{th\ (c-h)} \equiv 0.8$ °C/W for the TO 220 case
- $R_{th\ (c-h)} \equiv 0.5$ °C/W for the TOP 3

} Mica insulator

C - ASSEMBLY IN THE AIR (WITHOUT HEAT SINK) OF THE TO 220 - TOP 3 - TOPLESS

The components in direct contact with the air (on a printed circuit board) can only dissipate low power. For example :
TO 220 :

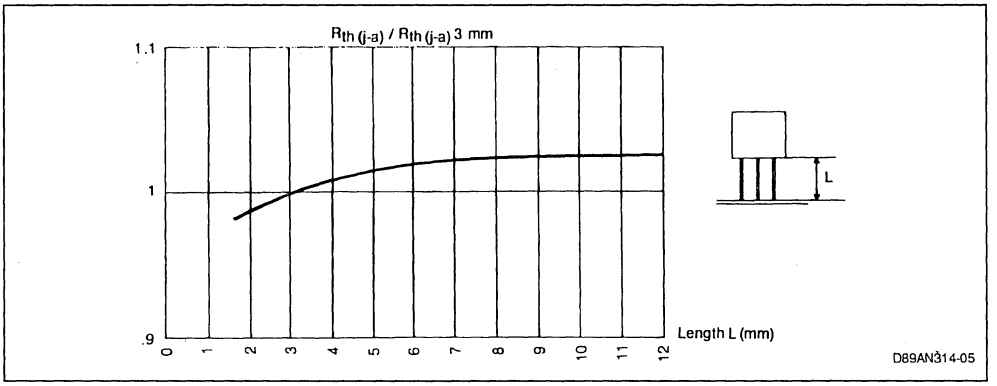
$$\text{Maximum dissipated power} = \frac{T_j - T_a}{R_{th\ (j-a)}} = \frac{110 - 50}{60} = 1W$$

The evacuation of the heat produced during operation takes place at several levels :

- the case,
- the connections,
- the soldering points of connections on the PC board.

The influence of the length of connections, on one hand, and the area of copper at the soldering point, on the other hand, is given on figure 5 and figure 6.

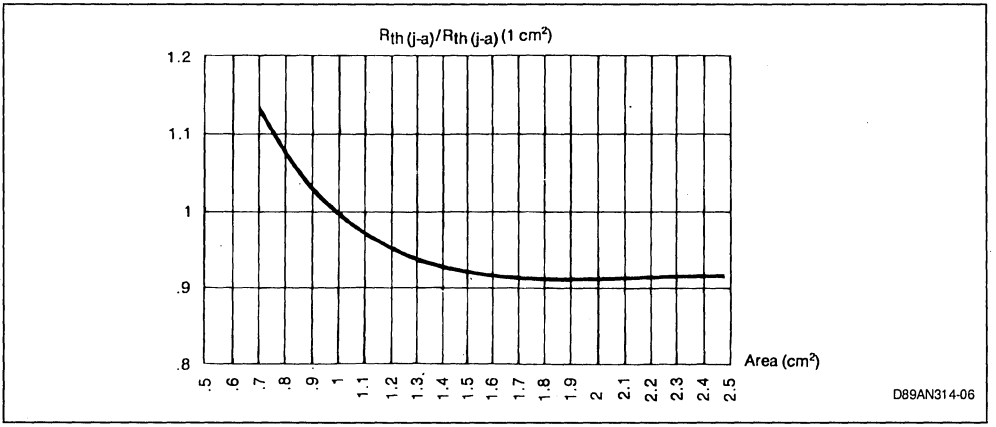
Figure 5 : Relative Variation of the Thermal Resistance (junction-air) as a Function of the Length L of Connections.



THERMAL RESISTANCE VALUES (junction-air)

	TOPLESS	TO 220	TOP 3
Rth (j-a) (°C/W)	75	60	50

Figure 6 : Relative Variation of the Thermal Resistance (junction-air) as a Function of the Area of Copper at the Soldering Point.

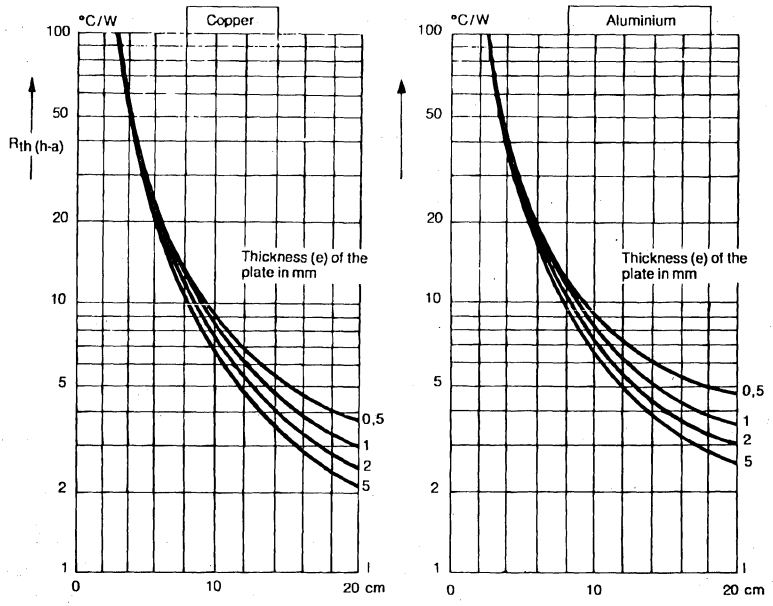


CONCLUSION

When designing assembly of a plastic-case semiconductor device on a heat sink, several precautions need to be taken, particularly never to exceed the maximum junction temperature (Tj max.).

The best assembly system is the one which satisfies the thermal requirements in the simplest manner. The clip assembler, in most cases, meets these requirements. This assembly, because of the ease with which it can be performed, the uniform pressure exercised on the case and the low cost, enables obtaining optimal contact thermal resistance and mechanically reliable assembly.

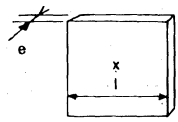
CHART FOR EVALUATION OF A FIAT HEAT SINK



Conditions :

- Bare convector
- Vertical
- Semiconductor device at the centre
- No ventilation
- x 0.7 if painted black
- square

l = length of one side of the square with an area S



Example : Copper heat sink, thickness e = 1 mm
$R_{th\ (h-a)}$ = 9°C/W l = 10 cm

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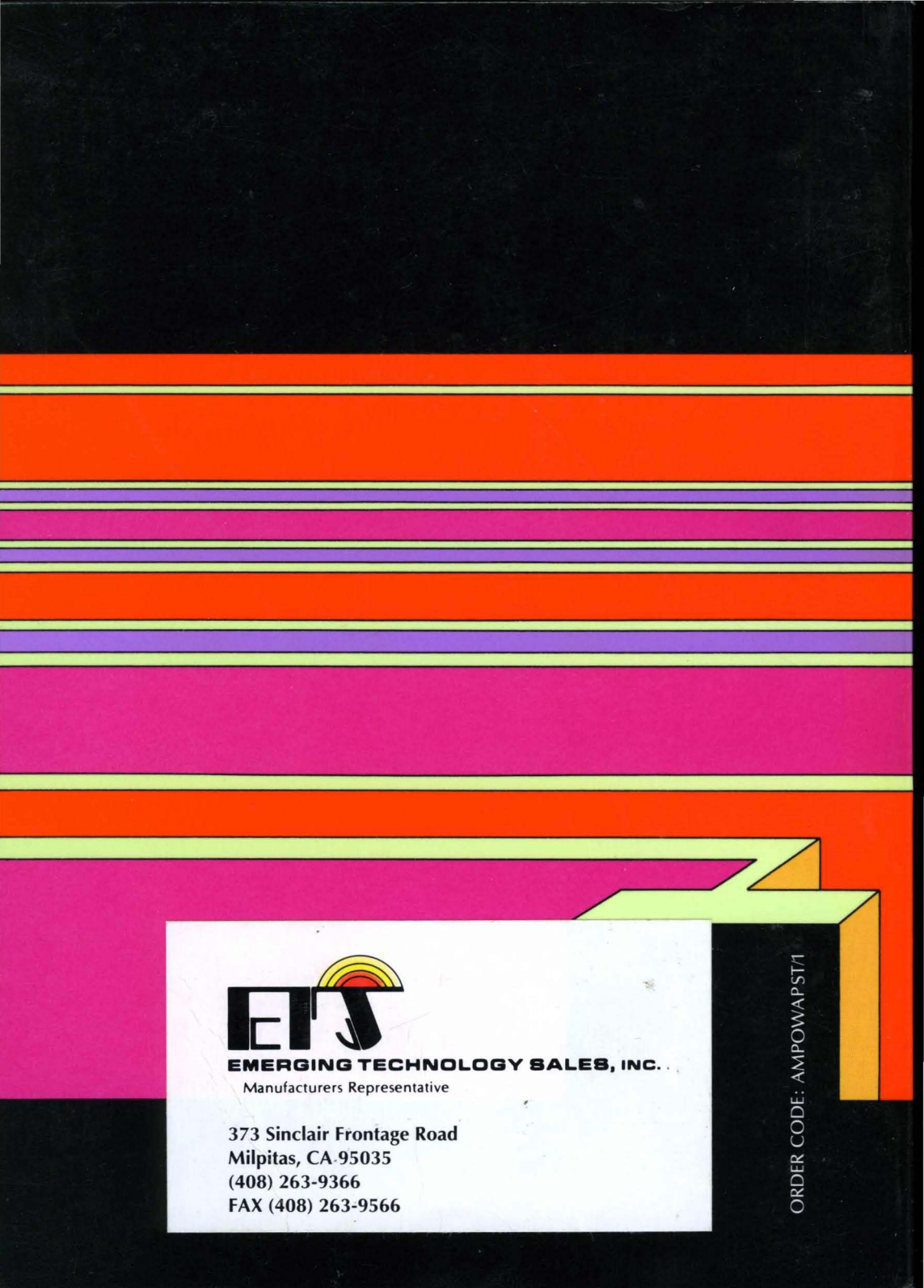

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