AUTOMOTIVE PRODUCTS

DATABOOK

2nd EDITION

SGS-THOMSON MICROELECTRONICS

AUTOMOTIVE PRODUCTS

SGS-THOMSON MICROELECTRONICS

AUTOMOTIVE PRODUCTS

DATABOOK

2nd EDITION

JANUARY 1993

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TABLE OF CONTENTS

AUTOMOTIVE POWER IC TECHNOLOGY

Since the early seventies, more and more functions have been added to our cars not only with the purpose of guaranteeing a better confort to drivers and passangers, but also to reduce operating costs and finally to ensure compliance with new regulations concerning noise and pollution. Because of all these needs, cars have to house more and more modules designed to perform more or less complex operations.

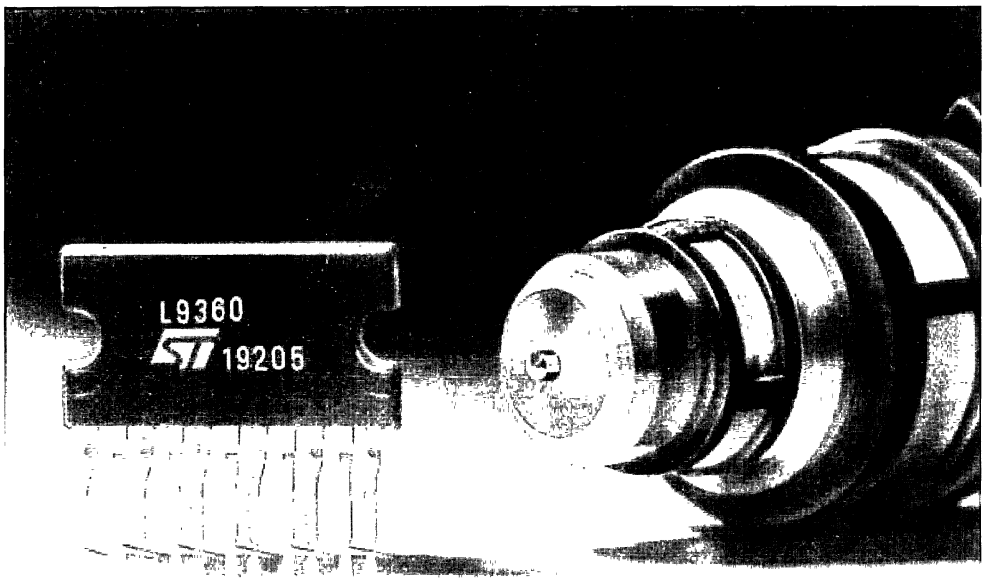
This growth makes more and more evident the need to reduce the room taken by each module, with the double target of minimizing the cost of the particular function and increasing the number of functions in a specific car; in parallel, by increasing the number of modules, it becomes mandatory to increase the reliability of each of them, otherwise the reliability of the total car would be badly affected.

All these issues recently pushed the manufacturers of automotive systems to refer very often to producers of integrated circuits asking for the development of monolithic devices capable of replacing effectively a number of discrete components, passive parts included; anyway the trend to a total integration is not over by just designing onto a simple piece of silicon a complete function, but it carries on implementing in the same device a number of auxiliary services, that would add a substantial cost if achieved by discrete components, but can easily find place on a few extra square millimeters of silicon.

It is evident that the key issue to pursue the monolithic design of very complex functions in the automotive enviroment is the availability of very capable processes.

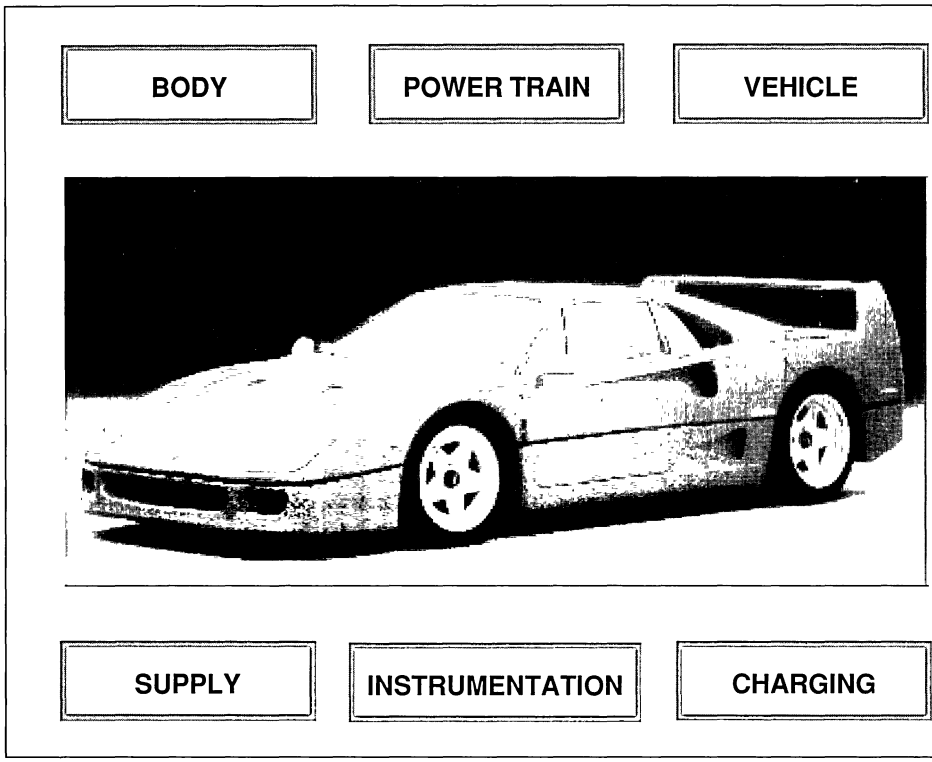
There is no single IC technology that is superior to all others in every aspect: for each application the choice of technology must be a tradeoff depending on the type of load and on the circuit complexity required. Consequently, the availability of many technologies (high density, high power, purely Bipolar, purely MOS and finally Mixed) is mandatory allowing the best choice in terms of both technical characteristics and cost.

Today, however, the strong need to host on the same chip high density signal circuitry together with power stages managing currents of several amperes, has driven the main focus to various



L9360 DUAL INJECTOR DRIVER. Designed for multipoint fuel injection systems, the L9360 contains two smart power circuits that drive fuel injector solenoids. This device is produced using mixed Bipolar-CMOS-DMOS technology which guarantees very low power dissipation.

INTRODUCTION



SGS-THOMSON's automotive product portfolio covers a very broad range of applications in Car applications enviroment.

mixed processes usually identified as "Smart Power". The technologies used to manufacture ICs that can be defined Smart Power are divided into two main families: bipolar and mixed. These are divided in turn into horizontal and vertical structures; the choice of one technology rather than another depending on various elements, such as the number of power stages and the value of their resistance in the "ON" condition.

Regardless of the process choice, for an integrated circuit the electrical and physical enviroment of a vehicle is extremely hostile. Any electronic component designed for automotive applications must operate over a very wide temperature range, it must operate on a wide range of supply voltages, it must be able to survive accidental battery reversal and it must be robust enough to withstand the high energy transients which sometimes occur on the battery rail. When the battery is accidentally disconnected from the alternator during a high current charging phase, for example, a transient is generated which can exceed 100V.
Transients of up -100V can also be generated if an inductive load is de-energized suddenly.
Finally it is worth to underline that an integrated circuit does not consist of just silicon technology, but relies heavily on package and bonding technology, and that is particularly true for a Smart Power device. SGS-THOMSON is able to optimize the use of silicon area by using a mixed bonding process, where signal pads are bonded thin gold wires and power pads with thick aluminium wires.

This is only one of the many achiviements gained by SGS-THOMSON during nearly 15 years spent designing components dedicated to the Automotive Market, and today SGS-THOMSON offers one of the widest choice of rugged and cost effective solutions for any kind of application in the car enviroment

SGS-THOMSON's automotive product portfolio covers a very broad range of powertrain, body electronics, instrumentation, vehicle control charging and power supply applications. For most of your design needs you will find the solution in this book.

ALPHANUMERICAL INDEX

ALPHANUMERICAL INDEX

ALPHANUMERICAL INDEX

ALPHANUMERICAL INDEX

SELECTION GUIDE

For detailed information on products referred to in the selection guide but not included as datasheet in this book, please refer to the databook indicated in colum "DB"

SGS-THOMSON DATABOOKS

DB	DESCRIPTION	ORDER CODE
a	4 BIT MCU FAMILY ET9400	DBET9400ST/1
b	8 BIT MCU FAMILIES EF6801/04/05	DB68XXST/1
c	16 BIT MPUs & ASSOCIATED PERIPHERALS	DB6800ST/1
d	AUDIO POWER and PROCESSING ICs	DBAUDIOPROST/1
e	AUTOMOTIVE PRODUCTS	DBAUTOMOTIVEST/2
f	CB12000 SERIES STANDARD CELLS	DBCB12/1
g	CB12000 SERIES STANDARD CELL MODULE GENERATORS	DBCB12GEN/1
h	ANALOG CELLS AND ARRAYS	DBANACA/1090
i	HIGH SPEED CMOS	DBHSCMOSST/1
j	IMAGE PROCESSING	DBIMAGEPROST/2
k	INDUSTRIAL and COMPUTER PERIPHERAL ICs	DBINCOMPEST/2
l	CB22000 SERIES STANDARD CELLS	DBCB22KST/1
m	ISB12000 SERIES CONTINUOUS ARRAYS	DBISB12KST/1
n	ISB24000 SERIES CONTINUOUS ARRAYS	DBISB24KST/1
o	LINE CARD ICs (Q1'93)	DBLINCARDST/2
p	LOW POWER SCHOTTKY TTL ICs	DBLPSST/1
q	VOLTAGE REGULATORS	BKVOLTAREST/1
r	POWER BIPOLAR TRANSISTORS	DBBIPTRANST/1
s	POWER MODULES	DBPOMODULEST/1
t	POWER MOS DEVICES	DBPOWERMOSST/2
u	GAL PROGRAMMABLE LOGIC DEVICES	DBPROLOGICST/1
v	PROTECTION DEVICES (Q1'93)	DBPROTECST/2
w	RF & MICROWAVE POWER TRANSISTORS (Q1'93)	DBRFST/2
y	SMALL SIGNAL TRANSISTORS	DBSMSIGST/1
z	CMOS B SERIES	DBCMOSBST/1
aa	CMOS LINEAR	EKCMOSLINST/3
ab	POWER SKOTTKY DIODES	DBPOSCHODIOST/1
ab	STATIC RAMs	DBSRAM/1
ac	ISDN & DATACOM PRODUCTS	DBISDNICST/1
ad	TELEPHONE SET ICs (Q1'93)	DBTELSETST/2
ae	COMPUTER GRAPHICS	DBGRAPHICST/2
af	THE L4970 SWITCHING REGULATOR IC FAMILY	BKL4970FA/0489
ag	THE TRANSPUTER DATABOOK	DBTRANST/3
ah	THE TRANSPUTER DEVELOPMENT AND iq SYSTEMS DATABOOK	72TRN21901
ai	SCRs & TRIACS	DBSCRTRIST/2
aj	VIDEO PRODUCTS SIGNAL PROCESSING	DBTVCRSPST/1
ak	VIDEO PRODUCTS POWER & GRAPHICS	DBPOMGRAST/1
al	Z80 MICROPROCESSOR FAMILY	DBZ80ST/1
am	ZENER, SCHOTTKY & RECTIFIER DIODES	DBDIODEST/1
an	MEMORY DATABOOK	DBMEMORYST/2
ao	ST6210/ST6215/ST6220/ST6225	DBST6ST/2
ap	ST624X Family LCD DISPLAY CONTROL (Q1'93)	DBST624XFST/1
aq	ST9 FAMILY 8/16 BIT MCU	DBST9ST/1
ar	SUBSYSTEMS PRODUCT PROFILE	BKSUBST/1
as	ST10 USER MANUAL	UMST10ST/1
(*)	NOT INCLUDED IN CURRENT DATABOOKS CONTACT YOUR NEAREST SGS-THOMSON SALES OFFICE	

IGNITION CONTROLLERS

Device	Function	Package	DB	Page
L482	Half-effect Pickup Ignition Controller	DIP16/SO16	–	39
L484	Magnetic Pickup Ignition Controller	DIP16/SO16	–	47
L497	Half Effect Pickup Ignition Controller	DIP16/SO16	–	57
L530	Electronic Ignition Interface	DIP16/SO16	–	67
VB020	Smart Monolithic High Voltage Driver for Electronic Ignition	ISOWATT5	–	467
VB024	Smart Monolithic High Voltage Driver for Electronic Ignition	ISOWATT7	–	471
VB027	Smart Monolithic High Voltage Driver for Electronic Ignition	TO-220 5 Lead	–	477
VB921Z	High Voltage Ignition Coil Driver Power IC	TO-220	–	483
VB921ZFI	High Voltage Ignition Coil Driver Power IC	ISOWATT220	–	483
VB921ZV	High Voltage Ignition Coil Driver Power IC	TO-220	–	485
VB921ZVFI	High Voltage Ignition Coil Driver Power IC	ISOWATT220	–	485

IGNITION DARLINGTONS/IGBT

Device	Function	Package	DB	Page
BU911	High Voltage Driver for Electronic Ignition	TO-220	r	–
BU912	High Voltage Driver for Electronic Ignition	TO-220	r	–
BU921	High Voltage Ignition Coil Drive NPN Power Darlington	TO-3	r	–
BU921P	High Voltage Ignition Coil Drive NPN Power Darlington	TO-218	r	–
BU921PFI	High Voltage Ignition Coil Drive NPN Power Darlington	ISOWATT218	r	–
BU921T	High Voltage Ignition Coil Drive NPN Power Darlington	TO-220	r	–
BU921TFI	High Voltage Ignition Coil Drive NPN Power Darlington	ISOWATT218	r	–
BU931	High Voltage Ignition Coil Drive NPN Power Darlington	TO-3	–	589
BU931P	High Voltage Ignition Coil Drive NPN Power Darlington	TO-218	–	589
BU931PFI	High Voltage Ignition Coil Drive NPN Power Darlington	ISOWATT218	–	589
BU931T	High Voltage Ignition Coil Drive NPN Power Darlington	TO-220	–	593
BU931TFI	High Voltage Ignition Coil Drive NPN Power Darlington	ISOWATT218	–	593
BU931SM	High Voltage Ignition Coil Drive NPN Power Darlington	POWER SO-10	–	593
BU931Z	High Voltage Ignition Coil Drive NPN Power Darlington	TO-3	–	597
BU931ZP	High Voltage Ignition Coil Drive NPN Power Darlington	TO-218	–	597
BU931ZPFI	High Voltage Ignition Coil Drive NPN Power Darlington	ISOWATT218	–	597
BU931ZT	High Voltage Ignition Coil Drive NPN Power Darlington	TO-220	–	601
BU931ZTFI	High Voltage Ignition Coil Drive NPN Power Darlington	ISOWATT220	–	601
BU931ZSM	High Voltage Ignition Coil Drive NPN Power Darlington	POWER SO-10	–	601
STGH20N50	IGBT Driver for Electronic Ignition	TO-218	*	–
STGH20N50FI	IGBT Driver for Electronic Ignition	ISOWATT218	*	–
STGP10N50A	IGBT Driver for Electronic Ignition	TO-220	–	673
STGP10N50L	Logic Level Input IGBT Driver for Electronic Ignition	TO-220	*	–

FUEL INJECTION

Device	Function	Package	DB	Page
L584	Multifunction Injection Interface	DIP16	–	75

ALTERNATOR REGULATORS

Device	Function	Package	DB	Page
L585	Car Alternator Regulator	DIP16/SO16	–	87
L9444VB	One Chip Car Alternator Regulator	TO-220	–	293
L9448VB	One Chip Car Alternator Regulator	TO-220	–	293
L9480VB	One Chip Car Alternator Regulator	TO-220	–	293

ACTUATORS

Device	Function	Package	DB	Page
L9222	Quad Inverting Transistor Switch	POWERDIP (12+2+2)	–	235
L9305A	Dual High Current Relay Driver	POWERDIP (8+8)	–	239
L9307	Dual High Current Low Side Driver	MULTIWATT11	–	243
L9308	Dual Low Side Driver	MINIDIP	–	247
L9309	Dual High Current Low Side Driver	SIP10	–	243
L9326	Dual Intelligent Power Low Side Switch	SO24 (16+4+4)	–	261
L9341	Quad Low Side Driver	MULTIWATT15	–	267
L9351	High Side Driver	PENTAWATT	–	275
L9360	Dual Injection Driver	CLIP/MULTIWATT11 SO20L (12+4+4)	–	279
L9363	Quad Integrated Low Side Driver	MULTIWATT15	–	287
L9811	High Side Driver Circuit	HEPTAWATT	–	335
L9812R	High Side Driver Circuit	HEPTAWATT	–	339
L9821	High Side Driver	PENTAWATT	–	343
L9822	Octal Serial Solenoid Driver	MULTIWATT15	–	349
L9822E	Octal Serial Solenoid Driver	MULTIWATT15	–	357
L9842	Octal Parallel Low Side Driver	DIP20/SO20	–	371
L9930	Dual Full Bridge	MULTIWATT11	–	385
L9936	Half Bridge Motor Driver	MULTIWATT8	–	391
L9937	Full Bridge Motor Driver	MULTIWATT11	–	399
L9946	Multiple Half Bridge Driver	MULTIWATT15	–	407
L9947	Quad Half-Bridge and Single High-Side Driver	MULTIWATT15	–	411
VN02N	High Side Smart Power Solid State Relay	PENTAWATT	–	487

ACTUATORS (Cont'd)

Device	Function	Package	DB	Page
VN03	(ISO) High Side Smart Power Solid State Relay	PENTAWATT	–	495
VN05N	High Side Smart Power Solid State Relay	PENTAWATT	–	503
VN06	(ISO) High Side Smart Power State Relay	PENTAWATT	–	511
VN16B	High Side Smart Power Solid State Relay	PENTAWATT	–	519
VN20N	High Side Smart Power Solid State Relay	PENTAWATT	–	527
VN21	(ISO) High Side Smart Power State Relay	PENTAWATT	–	535
VN30N	High Side Smart Power Solid State Relay	PENTAWATT	–	543
VN31	(ISO) High Side Smart Power State Relay	PENTAWATT	–	549
VND05B	Smart Dual High Side Driver	HEPTAWATT	–	557
VND10B	Smart Dual High Side Driver	HEPTAWATT	–	565

VOLTAGE REGULATORS

Device	Function	Package	DB	Page
L387A	Very Low Drop 5V Regulator with Reset	PENTAWATT	–	35
L2605	5V - 500mA Low Dropout Regulator	TO-220/SOT-82	–	93
L2610	10V - 500mA Low Dropout Regulator	TO-220/SOT-82	–	93
L2685	8.5V - 500mA Low Dropout Regulator	TO-220/SOT-82	–	93
L4805	400mA - 5V Very Low Drop Regulator	TO-220/SOT-82	–	105
L4808	400mA - 8V Very Low Drop Regulator	TO-220/SOT-82	–	105
L4810	400mA - 10V Very Low Drop Regulator	TO-220/SOT-82	–	105
L4812	400mA - 12V Very Low Drop Regulator	TO-220/SOT-82	–	105
L4885	400mA - 8.5V Very Low Drop Regulator	TO-220/SOT-82	–	105
L4892	400mA - 9.2V Very Low Drop Regulator	TO-220/SOT-82	–	105
L4901A	Dual 5V Regulator with Reset	HEPTAWATT	d,ak	109
L4902A	Dual 5V Regulator with Reset and Disable	HEPTAWATT	d,ak	119
L4903	Dual 5V Regulator with Reset and Disable Functions	MINIDIP	d,ak	129
L4904A	Dual 5V Regulator with Reset	MINIDIP	d,ak	137
L4905	Dual 5V Regulator with Reset	HEPTAWATT	d,ak	145
L4915	Adjustable Regulator Plus Filter	MINIDIP (4+4)	d	153
L4916	Regulator Plus Filter	MINIDIP (4+4)	d	159
L4918	Regulator Plus Filter	PENTAWATT	d	165
L4920	Very Low Drop Adjustable Regulator	PENTAWATT	d	171
L4921	Very Low Drop Adjustable Regulator	MINIDIP (4+4)	d	171
L4922	Very Low Drop Regulator with Reset	PENTAWATT	–	175
L4923	5V - 1A Very Low Drop Regulator with Reset and Inhibit	HEPTAWATT	–	179
L4925	Very Low Drop Regulator	PENTAWATT	–	183
L4936	Dual Multifunction Regulator	MULTIWATT11	–	189

VOLTAGE REGULATORS (Cont'd)

Device	Function	Package	DB	Page
L4937	Dual Multifunction Regulator	HEPTAWATT	–	197
L4938	Dual Multifunction Regulator	POWERDIP (12+2+2)	–	189
L4939	Dual Multifunction 5V Regulator	POWERDIP (12+2+2)	–	205
L4945	5V - 500mA Very Low Drop Regulator	TO-220	–	213
L4947R	5V - 500mA Very Low Drop Regulator with Reset	PENTAWATT	–	217
L4948	Quad Regulator with Inhibit and Reset	MULTIWATT11	–	221
L4949	Multifunction Very Low Drop Regulator	MINIDIP/SO8	–	229
L4950	8.5V - 500mA Very Low Drop Regulator	TO-220	–	213
L4951	10V - 500mA Very Low Drop Regulator	TO-220	–	213
TEA7605	Low-Drop Voltage Regulator	TO-220	ak	455
TEA7610	Low-Drop Voltage Regulator	TO-220	ak	459
TEA7685	Low-Drop Voltage Regulator	TO-220	ak	463

SPECIAL FUNCTIONS

Device	Function	Package	DB	Page
L4620	Liquid Level Alarm	MINIDIP	–	97
L9324	Window Lift Controller	DIP20	–	253
L9610C	PWM Power Mos Controller	SO16	–	297
L9611C	PWM Power Mos Controller	DIP16	–	297
L9686	Automotive Direction Indicator	MINIDIP	–	307
L9700	Hex Precision Limiter	MINIDIP	–	311
L9703	Octal Ground Contact Monitoring Circuit	DIP20/SO20L	–	317
L9704	Octal Supply Contact Monitoring Circuit	DIP20/SO20L	–	323
L9705	Double Quad Contact Interface Circuit	DIP20/SO20L	–	329
L9830	Monolithic Lamp Dimmer	HEPTWATT	–	365
L9907	Motor Bridge for Head light Adjustment	MINIDIP/POWERDIP SO20L	–	379
ST9560	Data Link Controller for Vehicle Area Network	DIP28/SO28	–	423
ST9561	Data Link Controller for Vehicle Area Network	PLCC44	–	423

POWER DISCRETES FOR ACTUATORS APPLICATIONS

Device	Function	Package	DB	Page
BU82Z	NPN Power Darlington Transistor	TO-218	*	–
BUZ10	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
BUZ11	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
BUZ11A	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
BUZ11FI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	–
BUZ71	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
BUZ71FI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	–
BUZ71A	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
BUZ71AFI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	–
BUZ72A	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
IRF520	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
IRF520FI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	–
IRF530	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
IRF530FI	N-Channel Enhacement Mode Power Mosfet Transistor	ISOWATT220	t	–
IRF540	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
IRF540FI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	–
MTP3055E	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	625
MTP3055EFI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	625
STK7N10L	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	SOT-82	t	–
STK9N10	N-Channel Enhancement Mode Power Mosfet Transistor	SOT-82	t	–
STK12N05L	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	SOT-82	t	679
STK12N06L	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	SOT-82	t	679
STK14N05	N-Channel Enhancement Mode Power Mosfet Transistor	SOT-82	t	–
STK14N06	N-Channel Enhancement Mode Power Mosfet Transistor	SOT-82	t	–
STK16N05	N-Channel Enhancement Mode Power Mosfet Transistor	SOT-82	t	–
STK16N06	N-Channel Enhancement Mode Power Mosfet Transistor	SOT-82	t	–
STK16N10L	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	SOT-82	t	–
STK17N10	N-Channel Enhancement Mode Power Mosfet Transistor	SOT-82	t	–
STK20N06	N-Channel Enhancement Mode Power Mosfet Transistor	SOT-82	t	–
STK22N05	N-Channel Enhancement Mode Power Mosfet Transistor	SOT-82	t	685
STK3055E	N-Channel Enhancement Mode Power Mosfet Transistor	SOT-82	t	–
STLT19	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	TO-220	t	–
STLT19FI	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	ISOWATT220	t	–
STLT20	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	TO-220	t	–

POWER DISCRETES FOR ACTUATORS APPLICATION (Cont'd)

Device	Function	Package	DB	Page
STLT20FI	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	ISOWATT220	t	–
STLT29	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	TO-220	t	–
STLT29FI	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	ISOWATT220	t	–
STLT30	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	TO-220	t	–
STLT30FI	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	ISOWATT220	t	–
STP8N10L	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	TO-220	t	–
STP17N05L	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	TO-220	t	–
STP19N05L	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	TO-220	t	693
STP19N06L	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	TO-220	t	693
STP20N06	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
STP20N06FI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	–
STP20N10L	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	TO-220	t	–
STP20N10LFI	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	ISOWATT220	t	–
STP25N05	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
STP25N05FI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	–
STP25N06	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	697
STP25N06FI	N-Channel Enhancement Mode Power Mosfet Transitor	ISOWATT220	t	697
STP30N05	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
STP30N05FI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	–
STP30N06	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
STP30N06FI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	–
STP36N06	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	705
STP36N06FI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	705
STP40N05	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
STP40N05FI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	–
STP40N06L	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	TO-220	t	713
STP40N06LFI	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	ISOWATT220	t	713
STP45N05L	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	TO-220	t	–
STP45N05LFI	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	ISOWATT220	t	–
STP50N06	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	717

POWER DISCRETES FOR ACTUATORS APPLICATION (Cont'd)

Device	Function	Package	DB	Page
STP50N06FI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	717
STP55N06	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	723
STP55N06FI	N-Channel Enhancement Mode Low Threshold Power Mosfet Transistor	ISOWATT220	t	723
STVHD90	N-Channel Enhancement Mode Power Mosfet Transistor	TO-220	t	–
STVHD90FI	N-Channel Enhancement Mode Power Mosfet Transistor	ISOWATT220	t	–

POWER DISCRETES FOR VOLTAGE REGULATORS

Device	Function	Package	DB	Page
BDW93	NPN Power Darlington Transistor	TO-220	r	583
BDW93A	NPN Power Darlington Transistor	TO-220	r	583
BDW93B	NPN Power Darlington Transistor	TO-220	r	583
BDW93C	NPN Power Darlington Transistor	TO-220	r	583
BDW94	PNP Power Darlington Transistor	TO-220	r	583
BDW94A	PNP Power Darlington Transistor	TO-220	r	583
BDW94B	PNP Power Darlington Transistor	TO-220	r	583
BDW94C	PNP Power Darlington Transistor	TO-220	r	583
TIP140	NPN Power Darlington Transistor	TO-218	r	–
TIP145	PNP Power Darlington Transistor	TO-218	r	–

SPECIAL PROTECTION FUNCTIONS

Device	Function	Package	DB	Page
RBO08-40	Reverse battery and Over Voltage Protection	TO220 AB	v	645
RBO40-40	Reverse battery and Over Voltage Protection	TO220 AB	v	649

TRANSIL

P_P (W)	V_{RM} (V)	Type		Case	Page
		Unidirectional	Bidirectional		
400/1 ms	5.8 to 376	BZW04../BZW04P..	BZW04..B/BZW04P..B	F126	605
600/1 ms	5.8 to 376	P6KE.. P,A	P6KE.. CP, CA	CB-417	631
300/1 ms	270	PL360D	–	F126	639
1500/1 ms	5.8 to 376	1.5KE... P, A	1.5KE...CP, CA	CB-429	575
5000/1 ms	10 to 180	BZW50...	BZW50...B	AG	613
7000/1 ms	24	LDP24AS	–	AG	619

SURFACE MOUNT TRANSIL

P_P (W)	V_{RM} (V)	Type		Case	Page
		Unidirectional	Bidirectional		
400/1 ms	5.5 to 188	SM4T..., A	SM4T..C,A	SOD6	655
600/1 ms	5.5 to 188	SM6T..., A	SM6T...C,A	SOD6	661
1500/1 ms	5.5 to 188	SM15T..., A	SM15T...C,A	SOD15	667

SERIAL ACCESS EEPROM MEMORIES

Serial access EEPROMs guarantee 1,000,000 Erase/Write cycle endurance.
With SGS-THOMSON major advantage in EEPROM, 1,000,000 Erase/Write cycle endurance, combined with 3V to 5.5V voltage operation and memory protect features, the EEPROM has become the memory for reference data storage in many kinds of equipment. They are ideally suited for printers, telephone sets and all equipment requiring non-volatile set-up or temporary data storage.

SGS-THOMSON's EEPROMs are suitable for use with I^2C and MICROWIRE® serial bus interfaces.

I^2C Serial Bus EEPROM Range

Size	Part Number	Organisation	V_{CC} Range	Feature	Package	DB
1K bit	ST24C01BX	128 x 8	4.5 to 5.5V		PDIP8	an
	ST24C01MX	128 x 8	4.5 to 5.5V		PS08	an
2K bit	ST24C02ABX	256 x 8	4.5 to 5.5V		PDIP8	an
	ST24C02AMX	256 x 8	4.5 to 5.5V		PS08	an
4K bit	ST24C04BX	512 x 8	4.5 to 5.5V	Write Protect	PDIP8	an
	ST24C04CMX	512 x 8	3.0 to 5.5V	Write Protect	PS08	an
	ST24C04MLX	512 x 8	4.5 to 5.5V	Write Protect	PS014	an
8K bit	ST24C08BX	1k x 8	4.5 to 5.5V	Write Protect	PDIP8	an
16K bit	ST24C16BX	2k x 8	4.5 to 5.5V	Write Protect	PDIP8	an

Note: In the Part Number X means three temperature ranges: 1 = 0 to 70 °C, 6 = –40 to 85 °C, 3 = –40 to 125 °C.

MICROWIRE Serial Bus EEPROM Range

Size	Part Number	Organisation	V_{CC} Range	Feature	Package	DB
256 bit	ST93C06BX	32x8 or 16x16	4.5 to 5.5V	Dual Organisation	PDIP8	an
	ST93C06MX	32x8 or 16x16	4.5 to 5.5V	Dual Organisation	PSO8	an
1K bit	ST93C46ABX	128x8 or 64x16	4.5 to 5.5V	Dual Organisation	PDIP8	an
	ST93C46AMX	128x8 or 64x16	4.5 to 5.5V	Dual Organisation	PSO8	an
	ST93C46TMX	128x8 or 64x16	4.5 to 5.5V	90° Turn Pin Out	PSO8	an
	ST93CS46BX	64 x 16	4.5 to 5.5V	Write Protect	PDIP8	an
	ST93CS46MX	64 x 16	4.5 to 5.5V	Write Protect	PSO8	an
2K bit	ST93C56BX	128x8 or 256x16	4.5 to 5.5V	Dual Organisation	PDIP8	an
	ST93C56MX	128x8 or 256x16	4.5 to 5.5V	Dual Organisation	PSO8	an
	ST93CS56BX	128 x 16	4.5 to 5.5V	Write Protect	PDIP8	an
	ST93CS56MX	128 x 16	4.5 to 5.5V	Write Protect	PSO8	an
	ST93CS56MLX	128 x 16	4.5 to 5.5V	Write Protect	PSO14	an
4K bit	ST93CS66BX	256 x 16	4.5 to 5.5V	Write Protect	PDIP8	an
	ST93CS66MLX	256 x 16	4.5 to 5.5V	Write Protect	PSO14	an

Note: In the Part Number X means three temperature ranges: 1 = 0 to 70 °C, 6 = –40 to 85 °C, 3 = –40 to 125 °C.

CMOS UV EPROM

Size	Part Number	Organi-sation	Speed (ns)						Package			Feature	DB
			80	100	120	150	200	250	FDIP	JLCC	LCCC		
64K	TS27C64A	8K x 8					■	■	●				an
	M27C64A	8K x 8				■	■	■					an
128K	M27C128A	16K x 8	▲	■	■	■	■	■	●				an
256K	M27C256B	32K x 8	▲	■	■	■	■	■	●				an
256K	M87C257	32K x 8			▲	■	■	■	●			Latched	an
512K	M27C512	64K x 8	▲	■	■	■	■	■	●				an
512K	M27C516	32K x 16				■	■	■	●				an
1M	M27C1001	128K x 8	▲	■	■	■	■	■	●		●		an
	M27V101	128K x 8					▲	▲	●		●	V_{CC} 3.2V to 5V	an
	M27V101	128K x 8						▲	●		●	V_{CC} 3V to 5.5V	an
	M27C1000	128K x 8			▲	▲			●			ROM compatible	an
	M27C1024	64K x 16			▲	■	■		●				an
2M	M27C2001	256K x 8	▲	■	■	■	■	■	●		●		an
	M27V201	256K x 8					▲	▲	●		●	V_{CC} 3.2V to5.5V	an
	M27V201	256K x 8						▲	●		●	V_{CC} 3V to 5.5V	an
4M	M27C4001	512K x 8	▲	■	■	■	■	■	●		●		an
	M27V401	512K x 8					▲	▲	●		●	V_{CC} 3.2V to 5V	an
	M27V401	512K x 8						▲	●		●	V_{CC} 3V to 5.5V	an
	M27C4002	256K x 16		■	■	■	■	■	●	●			an

NMOS UV EPROM: A product range from 16K up to 512K density is available

Notes:

● = Available

▲ = Speed available in Commercial Temperature ragne only.

■ = Speed available in Commercial and Automotive Temperature range.

OTP ROM CMOS

Size	Part Number	Organisation	Speed (ns)						Package				Feature	DB
			90	100	120	150	200	250	PDIP	PLCC	PSO	PTSO		
256K	ST27C256	32K x 8					■	■	●	●				an
	M27C256B	32K x 8	▲	▲	■	■	■	■	●	●	UD	UD		an
256K	M87C257	32K x 8			▲	■	■	■		●			Latched	an
512K	M27C512	64K x 8	▲	▲	■	■	■		●	●		UD		an
512K	M27C516	32K x 16				■	■			●				an
1M	M27C1001	128K x 8		▲	■	■	■			●				an
	M27C1000	128K x 8				▲			●				ROM compatible	an
	M27C1024	64K x 16			▲	■	■			●				an
2M	M27C2001	256K x 8		▲	■	■	■			●				an
4M	M27C4001	512K x 8		▲	■	■	■			●				an
	M27C4001	256K x 16			■	■	■			●				an

Notes:

● = Available

▲ = Speed available in Commercial Temperature range only.

■ = Speed available in commercial and automotive Temperature range.

UD = Under development

FLASH MEMORIES

Size	Part Number	Organisation	Speed (ns)					Package			Feature	DB
			100	120	150	200	250	PDIP	PLCC	PSO		
256K	M28F256	32K x 8	▲	■	■	■		●	●			an
256K	M28F256A	32K x 8	▲	■	■	■		●	●			an
512K	M28F512	64K x 8	▲	■	■	■		●	●			an
1M	M28F101	128K x 8	▲	■	■	■		●	●	●		an
1M	M28F102	64K x 16	▲	■	■	■		●	●	●		an

Notes:

● = Available

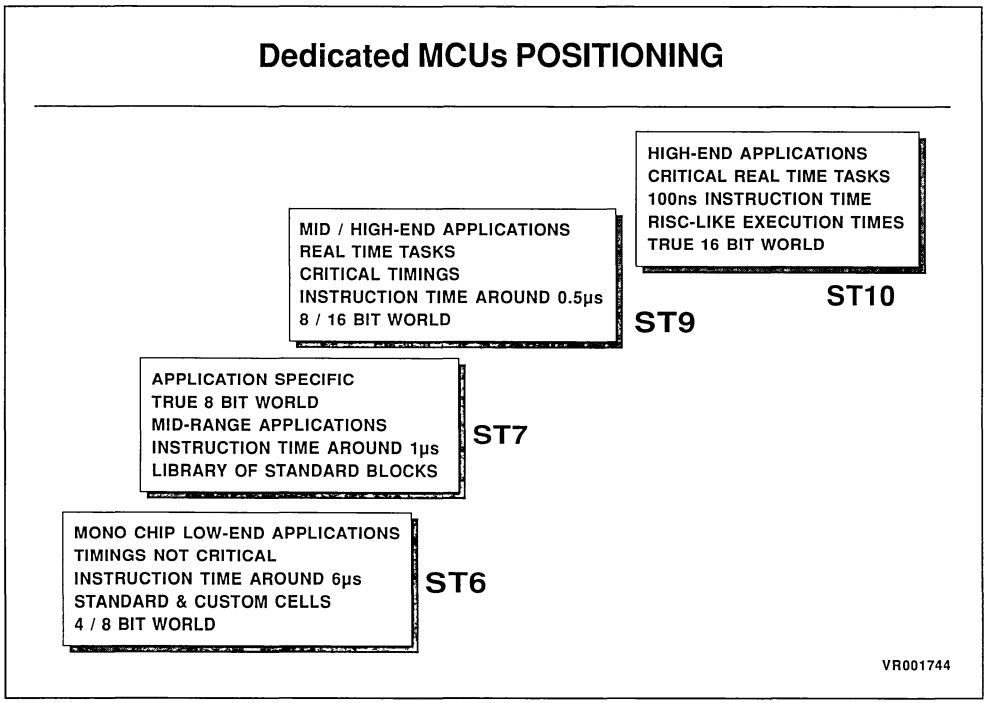
▲ = Speed available in Commercial Temperature range only.

■ = Speed available in Commercial and Automotive Temperature range.

UD = Under development

DEDICATED MICROCONTROLLERS FOR AUTOMOTIVE

SGS-THOMSON is supporting a wide range of automotive applications, including power train, car-body, instrumentation and car-radio, with its portfolio of 8-bit, 8/16 and 16-bit dedicated microcontrollers. These families are adapted to the requirements of the automotive environment, with a wide range of cost/performance tradeoffs. All MCUs interface directly to the SGS-THOMSON Automotive dedicated peripheral devices.



PRODUCT OVERVIEW

In the field of micro-controllers, the combination of architectural innovation, advanced process technology and modular, macrocell-based design has given SGS-THOMSON a strong position.

The 8-bit ST62 products is particularly successful in low end, cost-sensitive applications, while the proprietary 8/16-bit ST9 family offers real-time performance to Mid/High-end Systems.

To cover the requirements of Medium-range applications, SGS-THOMSON is developping the ST7. Thanks to its industry-standard Core and its library of peripherals, the ST7 can easily be customized to fullfill the needs of systems such as Multiplexed Control Functions in Car-Body, as well as RDS Signal processing for car-radio.

Already attracting great interest, the ST10 high-end 16-bit series, which will be available in Q4, will feature a highly sophisticated register file-based, four-stage pipelined architecture and very fast RISC-like execution (100ns instruction execution) and will include a version with on-chip flash memory.

DEDICATED MCUs MAIN CORE FEATURES

	ST6	ST7	ST9	ST10
APPLICATION	LOW END	MID RANGE	MID/HIGH RANGE	HIGH RANGE
ARCHITECTURE	SERIAL 8 BIT Accumulator	PARALLEL 8 BIT Accumulator	PARALLEL 8/16 BIT Register File	Full 16 BIT Parallel Register File 4 Stages Pipe Line
FEATURES				
ADDRESS SPACE	4K	64K	128K	256K BYTES LINEAR
ROM/EPROM	16K (PAGES)	8K	32K	32K
RAM	512 BYTES	512 BYTES	1,2 KBYTES	1K BYTES
CLOCK SPEED (MAX)	8 MHZ	4 MHZ	12 MHZ	20 MHZ
INSTRUCTION SPEED	6.5us	0.5us	0.5us	0.1us
NUMBER OF INST.	42	72	89	>100
16 BIT INSTRUCTION	NO	NO	YES	YES
MULTIPLY (8*8)	NO	YES (2.75us)	YES (1.8us)	YES (0.5us - 16x16)
DIVIDE (16:8)	NO	NO	YES (2.3us)	YES (1us - 32x16)
DMA	NO	NO	YES	YES
INTERRUPT	8 VECTORS	8 VECTORS	128 VECTORS	Fast Context Switching

VR001745

ST6

The ST6 is the entry point to SGS-THOMSON MCU world. Members of this family are tailored to allow an easy integration of the different electronic systems found inside a vehicle.

The ST621x/2x provides a flexible, cost effective solution to simple control requirements (window lift, central lock, mirror control...). The on-chip A/D converter enables intelligent feedback to an evolutive environment by directly connecting eight to sixteen analog input channels of the MCU to sensors. The human interface can be handled by both a keyboard and LEDs without any external components, using the flexible software configuration and direct drive capabilities of the I/O ports.

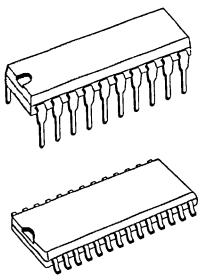
The ST624x includes a versatile LCD controller/driver capable of managing up to 4 x 45 Segments. It also features two Timer peripherals, each including an 8-bit counter with a 7-bit software programmable prescaler, a Digital Watchdog Timer, an 8-bit A/D converter with 12 analog inputs, a Power Supply Supervisor, and a synchronous Serial Peripheral Interface (SPI). 64 to 128 bytes of EEPROM is available, with over 300K erase/write cycle endurance, for non-volatile data storage.

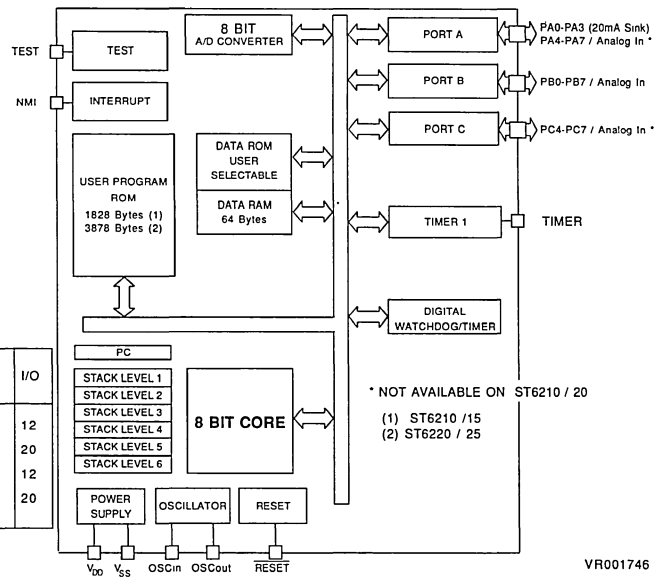
The ST628x family has the same architecture as the ST624x family, but includes a Dot Matrix LCD Driver in place of the ST624x segment based LCD Driver.

ST624x and ST628x are ideally suited for Dashboard, Climate Control and car-Radio applications.

Thanks to its low power consumption, high noise immunity and low noise sensitivity, the ST6 family allows substantial savings in component count in cost sensitive automotive systems.

ST6210/15/20/25 BLOCK DIAGRAM

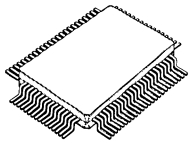


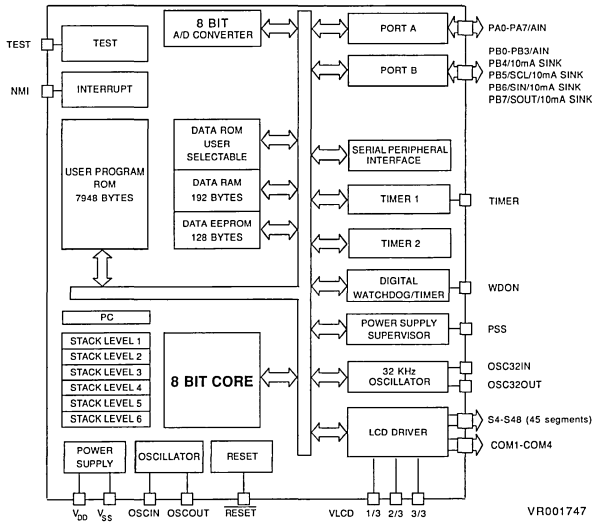


DEVICE	ROM (Byte)	A / D (Channels)	I/O
ST6210	2k	8	12
ST6215	2k	16	20
ST6220	4k	8	12
ST6225	4k	16	20

ST6240 BLOCK DIAGRAM

80 PIN PQFP





ST624X LCD DRIVER FAMILY

PRODUCT	ST6245	ST6242	ST6240	ST6285 / 80
DISPLAY	4x24 (Seg)	4x40 (Seg)	4x45 (Seg)	16x40 / 16x48 (Dot) 8x48 / 8x56 (Dot)
ROM	4k	8k	8k	8k
RAM+LCDRAM	128+12	128+24	192+24	192+96 / 192+128
EEPROM	64	-	128	- / 128
8 BIT A/D (Channel)	7	6	12	8 / 12
TOTAL I/O	11	10	16	12 / 22
TIMERS	2xT1	T1	2xT1	T1 / T1,T3
WATCHDOG TIMER	1	1	1	1
SPI	1	1	1	1
32kHz Clock	Yes	-	Yes	- / Yes
PSS	-	-	Yes	-
PACKAGE	QFP52	QFP64	QFP80	QFP80 / 100

VR001750

ST9

The ST9 is a high performance 8-bit micro-controller with 16-bit instruction capabilities, optimized for real time tasks and high level language development.

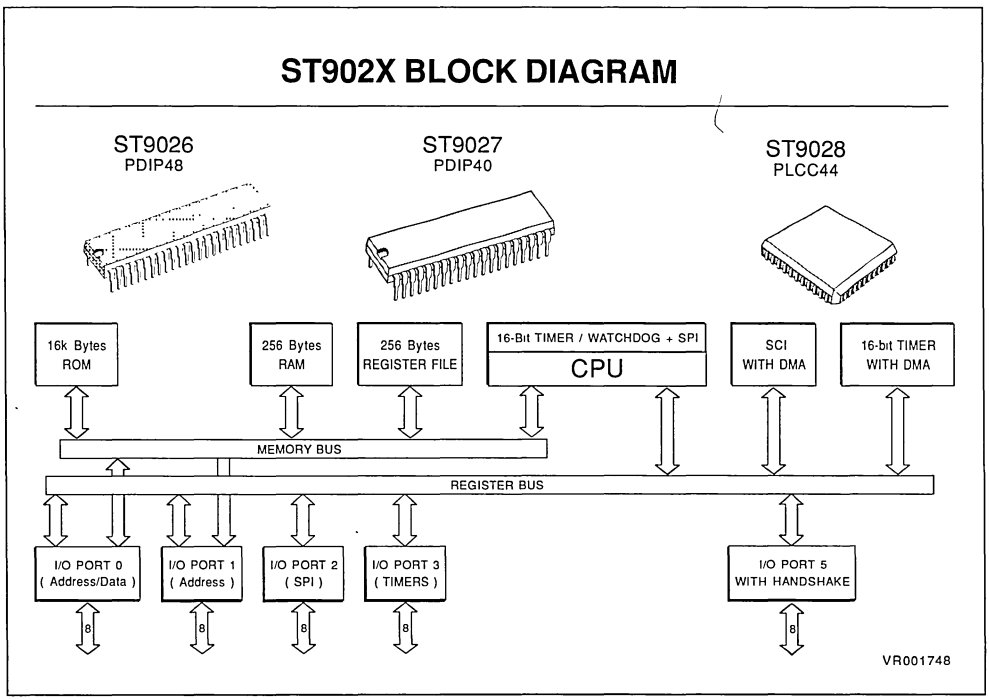
The common core has built-in Timer Watchdog functions for secure operations, Serial Peripheral Interfaces adaptable to low-cost external I^2C-bus and Microwire-bus, and an external memory interface with full, expandable vectored interrupt and DMA facilities.

Variations in the peripheral organization suit the different requirements of the middle to high end embedded applications.

The library of peripherals includes a Multifunction Timer, with operating modes to cover almost all timing requirements, including the option of DMA to the timing constants and the triggering of other on-chip peripherals such as the A/D Converter.

The A/D converter, offering 8-bit resolution, features an automatic threshold sensing watchdog on two of its eight multiplexed input channels. Serial communication is handled by the Serial Communication Interface with fast asynchronous and byte synchronous capabilities, thanks to its Receive and Transmit DMA channels.

The smallest member of the family, the ST902x offers 16K bytes of ROM and 256 bytes of RAM in addition to the 224 general purpose registers available as user RAM in the standard ST9 core. Thanks to its full feature DMA controller, powerful SPI and Interrupt Handler, 16-bit programmable Timer/Watch Dog ensuring system integrity, 16-bit Multifunction Timer with 8-bit prescaler and 12 operating modes allowing the easy generation or measurement of complex waveforms, and up to five I/O ports with programmable input threshold and output characteristics, the ST902x family provides the Automotive System Designer with the computation power of the ST9 at a particularly attractive price/performance ratio.

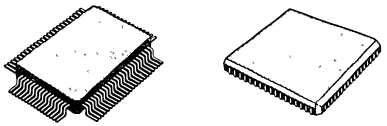


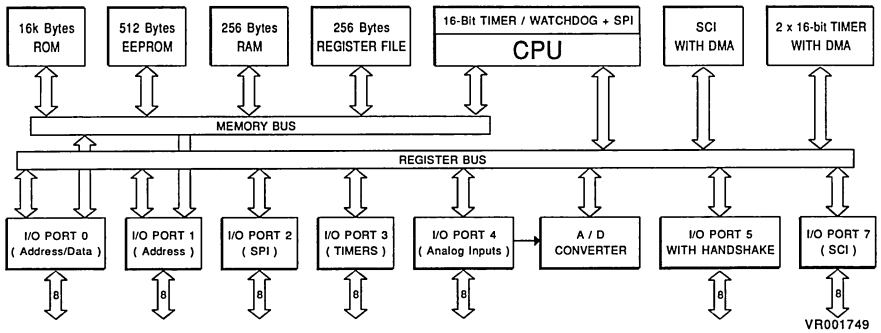
ST9040 BLOCK DIAGRAM

ROM (kByte)	EEPROM (Byte)	RAM (Byte)	PRODUCT
8	-	-	ST9030
12	-	-	ST9032
16	-	256	ST9036
16	512	256	ST9040

ALL PRODUCTS ARE PIN TO PIN COMPATIBLE

PQFP80 PLCC68





For applications requiring an A/D converter and additional Timing functions, SGS-THOMSON proposes a complete set of pin-to-pin compatible devices allowing the easy upgrade of system performance while avoiding complete hardware and software rework.

Starting with the ST9030 and ST9032, with 8K and 12K of ROM respectively and 224 bytes of RAM, the designer can enhance his application by plugging into the same socket, either an ST9036 with 16K ROM and an additional 256 bytes of RAM, or an ST9040 with 512 bytes of EEPROM for the storage of non volatile parameters, such as system in-site customization, driver's personalization...

ST9 microcontrollers are particularly well suited for car-body applications, such as Multiplexed networks, brushless motor control for Climate control, airbag... They can be directly interfaced to the ST9560 VAN Data Link Controller.

Thanks to its Multifunction Timer, ST9 can fully emulate J1850 Protocols while keeping the CPU available for Application Management.

The ST9 also covers the requirements of Vehicle Control applications such as ABS, Active Suspension and Power Steering. Finally, the ST9 is ideally suited for high-end Car-radio.

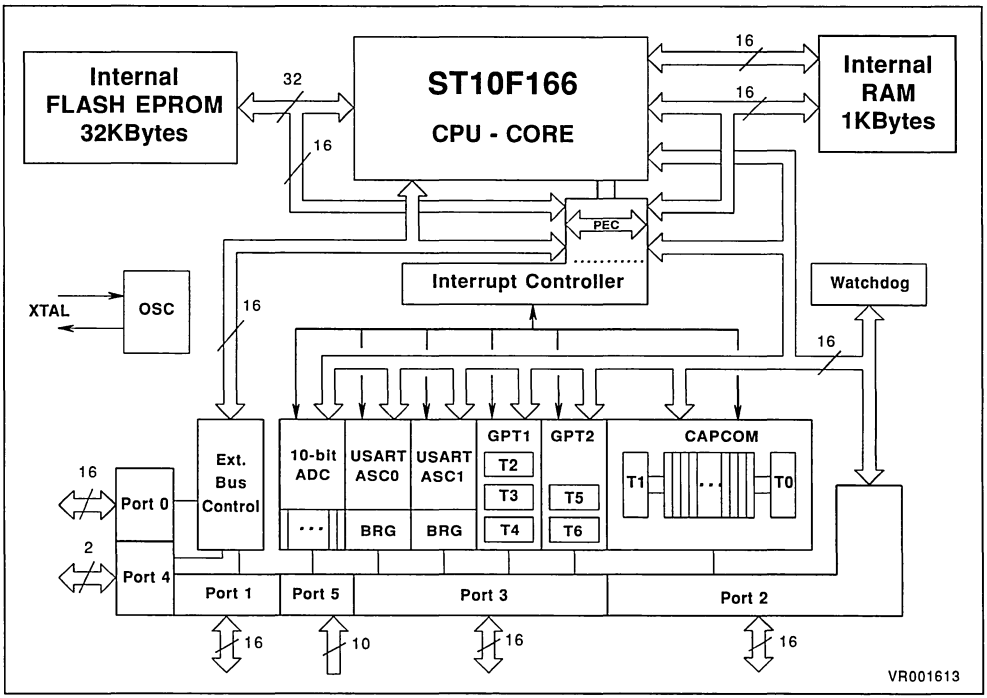
ST10

The ST10 is a high performance 16-bit RISC-like microcontroller with a CISC-like Instruction Set, offering a 100ns instruction cycle time at an internal clock speed of 20MHz.

Thanks to its powerful Timer Systems and a 10 bit A/D Converter, the ST10 suits the needs of High-end Engine Management Systems.

The ST10F166 is the first member of the ST10 family, featuring 32K bytes of Flash EPROM and 1K byte of RAM.

Soon to be introduced are ROM and ROMLESS versions of this device.



THE CONCEPT OF SGS-THOMSON MICROCONTROLLERS

All SGS-THOMSON microcontrollers are designed with a building block approach.

CPU Cores are surrounded by a combination of on-chip peripherals available as macro-cells from a standard library, which includes ROM, RAM, EPROM, EEPROM, FLASH EPROM, WATCHDOG TIMER, MULTIFUNCTION TIMER, A/D CONVERTER, LCD DRIVER and I/O PORTS.

Protocol Handlers for Multiplexed Network Systems are presently under development, to be used as standard peripherals in future versions of ST7and ST9.

The Cores, as well as the macro-cells, are fully characterized and fully qualified to meet the requirements of the Automotive Environment.

SGS-THOMSON guarantees all its microcontrollers for the temperature range of -40°C to +85°C. For some specific applications, a higher limit such as +105°C or +125°C with adapted electrical specifications can be warranted.

For each family of microcontrollers, SGS-THOMSON offers EPROM versions for development, OTP for pre-series, and ROM for full production.

Development tools include Real-time emulators, software simulators, C Compilers (except for ST6), EPROM and GANG Programmers, and a Real Time Kernel for the ST9.

Starter-Kits provide a low cost evaluation system for ST62 micro-controllers.

TECHNICAL DOCUMENTATION

All SGS-THOMSON microcontrollers have their datasheets provided individually or inside a databook. They are listed in the following pages.

To be able to program microcontrollers, users need good reference material;

Thus, a complete set of supporting literature is available, including Technical Manuals, Programming Manuals, User Guides and Application notes.

ST62XX Family

Type	Function	DB	Page
ST6210	Gen. Purpose with A/D Converter	ao	–
ST62E10	EPROM & OTP version	ao	–
ST6215	Gen. Purpose with A/D Converter	ao	–
ST62E15	EPROM & OTP version	ao	–
ST6220	Gen. Purpose with A/D Converter	ao	–
ST62E20	EPROM & OTP version	ao	–
ST6225	Gen. Purpose with A/D Converter	ao	–
ST62E25	EPROM & OTP version	ao	–
ST6240	Alphanum. LCD Driver, PQFP80	▲	–
ST62E40	EPROM & OTP version	▲	–
ST6242	Alphanum. LCD Driver, PQFP80	▲	–
ST62E42	EPROM & OTP version	▲	–
ST6245	Alphanum. LCD Driver, PQFP80	▲	–
ST6280	Dot Matrix LCD Driver, PQFP100	▲	–
ST62E80	EPROM & OTP version	▲	–
ST6285	Dot Matrix LCD Driver, PQFP80	▲	–
ST6291/92	Low Voltage/Low Current Applications	■	–
ST6293/94	Low Voltage/Low Current Applications	■	–
ST62E93/94	EPROM & OTP version	■	–

▲ Included in to the ST624X LCD DISPLAY Databook for seen for Q193

■ Available datasheets only.

ST9 Family

Type	Function	DB	Page
ST9026/27/28	16K ROM	aq	–
ST90E26/27/28	16K EPROM	aq	–
ST90R26	ROMLESS Version	aq	–
ST9030	8K ROM with A/D Converter	aq	–
ST90R30	ROMLESS Version	aq	–
ST9032	12K ROM with A/D Converter	■	–
ST9036	16K ROM with A/D Converter	aq	–
ST9040	16K ROM with A/D Converter and EEPROM	aq	–
ST90E40	16K EPROM with A/D Converter and EEPROM	aq	–
ST90R40	ROMLESS Version	aq	–
ST90R50	ROMLESS with Bankswitch and A/D Converter	aq	–
ST9560/61	Data Link Controller for **V**ehicule **A**rray **N**etwork	–	423

■ Available datasheets only

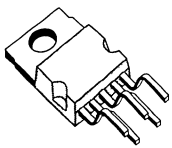
ST10 Family

Type	Function	DB	Page
ST10F166	256K FLASH Memory with A/D Converter	as	–
ST10166	16K ROM with A/D Converter	as	–
ST10R166	ROMLESS Version	as	–

INTEGRATED CIRCUITS DATASHEETS

VERY LOW DROP 5V REGULATOR WITH RESET

- PRECISE OUTPUT VOLTAGE (5 V ± 4 %)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)
- HIGH NOISE IMMUNITY ON RESET DELAY CAPACITOR



Pentawatt®

ORDERING NUMBER : L387A

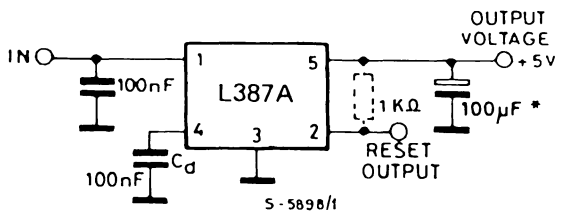
DESCRIPTION

The L387A is a very low drop voltage regulator in a Pentawatt® package specially designed to provide stabilized 5V supplies in consumer and industrial applications. Thanks to its very low input/output voltage drop this device is very useful in battery powered equipment, reducing consumption and prolonging battery life. A reset output makes the L387A particularly suitable for microprocessor systems. This output provides a reset signal when power is applied (after an external programmable delay) and goes low when power is removed, inhibiting the microprocessor. An hysteresis on reset delay capacitor raises the immunity to the ground noise.

ABSOLUTE MAXIMUM RATINGS

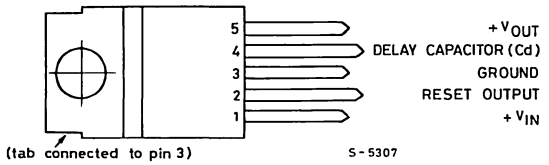
Symbol	Parameter	Value	Unit
V_I	D.C. Input Voltage	35	V
T_j, T_{stg}	Junction and Storage Temperature Range	–55 to 150	°C

APPLICATION CIRCUIT

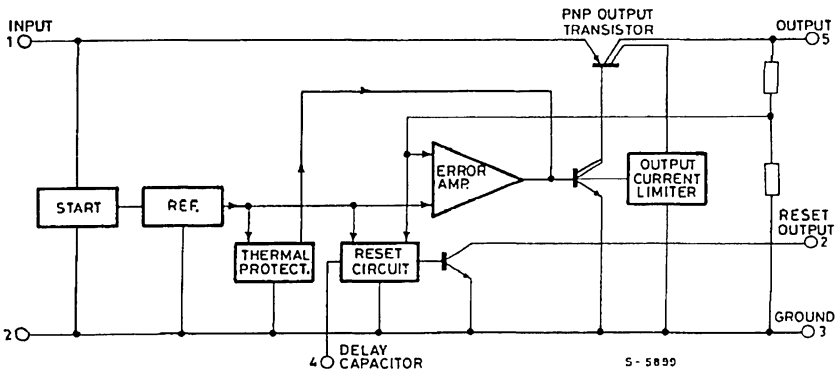


* Min 33 µF and max. ESR ≤ 3 Ω over temperature range.

PIN CONNECTION (Top views)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_i = 14.4 V, T_j = 25 °C, C_o = 100 µF; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 5 mA to 500 mA T_j = 25 °C $-40 \le T_j \le 125$ °C	4.80 4.75	5.00 5.00	5.20 5.25	V
V_I	Operating Input Voltage	(*), Over Full T Range (– 40 to 125 °C) (see note **)			26	V
ΔV_o	Line Regulation	V_i = 6 V to 26 V I_o = 5 mA		5	50	mV
ΔV_o	Load Regulation	I_o = 5 mA to 500 mA		15	60	mV
$V_I - V_o$	Dropout Voltage	I_o = 350 mA I_o = 500 mA $V_O = V_{O\,NOM} - 100$ mV		0.40 0.60	0.65 0.8	V
I_q	Quiescent Current	I_o = 0 mA I_o = 150 mA I_o = 350 mA I_o = 500 mA		5 20 60 100	15 35 100 160	mA
		V_i = 6.2 V I_o = 500 mA		160	180	
$\frac{\Delta V_o}{\Delta T}$	Temperature Output Voltage Drift			– 0.5		mV/°C
SVR	Supply Voltage Rejection	I_o = 350 mA f = 120 Hz C_o = 100 µF V_i = 12 V ± 5 V_{pp}		60		dB
I_{SC}	Output Short Circuit Current			1.2	1.6	A
V_R	Reset Output Voltage	I_R = 3 mA 1 < V_o < 4.70 V I_R = 16 mA 1.5 < V_o < 4.70 V Over Full T (– 40 °C ≤ T_j ≤ 125 °C)			0.5 0.8	V
I_R	Reset Output Leakage Current	V_o in Regulation V_R = 5V Over Full T Range			50	µA
t_d	Delay Time for Reset Output	Cd = 100 nF Over Full T Range		25		ms
$V_{RT\,(off)}$		V_o @ Reset out H to L Transition, Over Full T Range	4.70	V_o – 0.15		V
I_{C4}	Charging Current (current generator)	V_4 = 3 V	10	20	30	µA
$V_{RT\,(on)}$	Power on V_oThreshold	V_o @ Reset out L to H Transition , Over Full T Range		$V_{RT\,(off)}$ + 0.05 V	V_o – 0.04 V	V
V_4	Comparator Threshold (pin 4)	V_4 @ Reset out H to L Transition	3.2		3.9	V
		V_4 @ Reset out L to H Transition	3.7		4.3	V
V_H	Hysteresis Voltage	Over Full T Range		450		mV

(*) For a DC voltage 26 < Vi < 37 V the device is not operating.
(**) Design limits are guaranteed (but not 100 % production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Figure 1 : Dropout Voltage vs. Output Current.

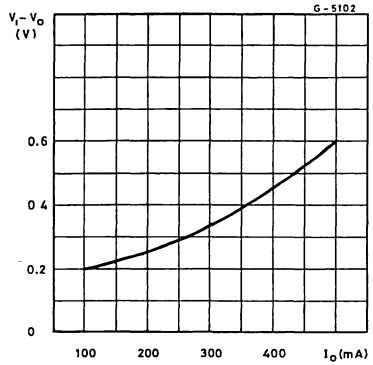


Figure 2 : Quiescent Current vs. Output Current.

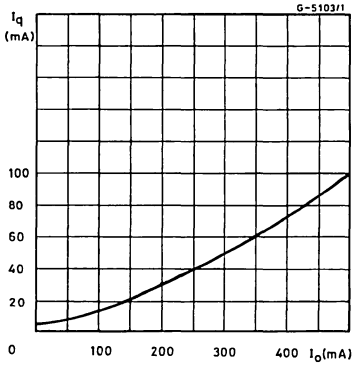
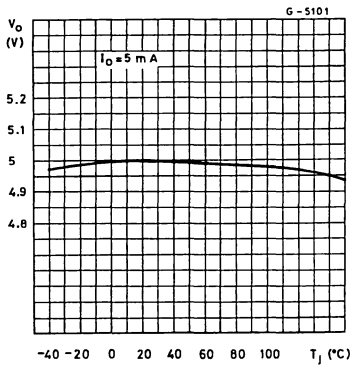
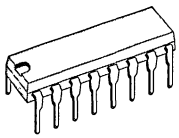


Figure 3 : Output Voltage vs. Temperature.

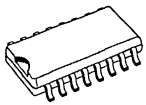


HALL–EFFECT PICKUP IGNITION CONTROLLER

- DIRECT DRIVING OF THE EXTERNAL POWER DARLINGTON
- COIL CURRENT CHARGING ANGLE (DWELL) CONTROL
- COIL CURRENT PEAK VALUE LIMITATION
- CONTINUOUS COIL CURRENT PROTECTION
- CONDUCTION AND DESATURATION TIME OUTPUT SIGNALS
- PERMANENT CONDUCTION PROTECTION RESET OUTPUT SIGNAL
- OVERVOLTAGE PROTECTION FOR EXTERNAL DARLINGTON
- LOAD DUMP PROTECTION



DIP16



SO16

ORDERING NUMBERS : L482 (DIP16)
L482D1 (SO16)

DESCRIPTION

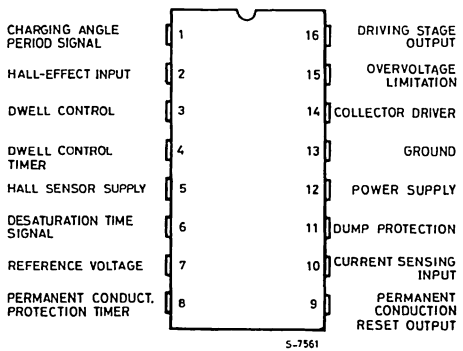
The L482 is an integrated circuit designed for use with an NPN darlington in breakerless ignition systems with hall-effect pickup sensors and high energy ignition coils.

It controls the energy stored in the ignition coil and the desaturation time of the external darlington to limit the power dissipation.

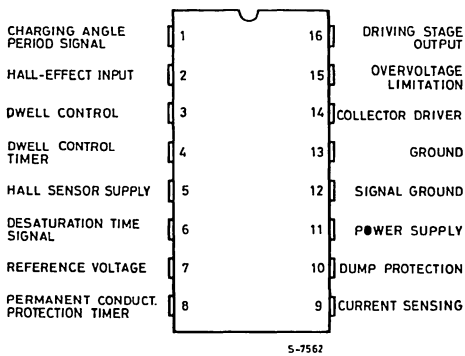
The L482 is also particularly suitable for use as ignition control and driving stage in more sophisticated car electronic systems which employ microprocessor circuits.

PIN CONNECTIONS (top views)

DIP16



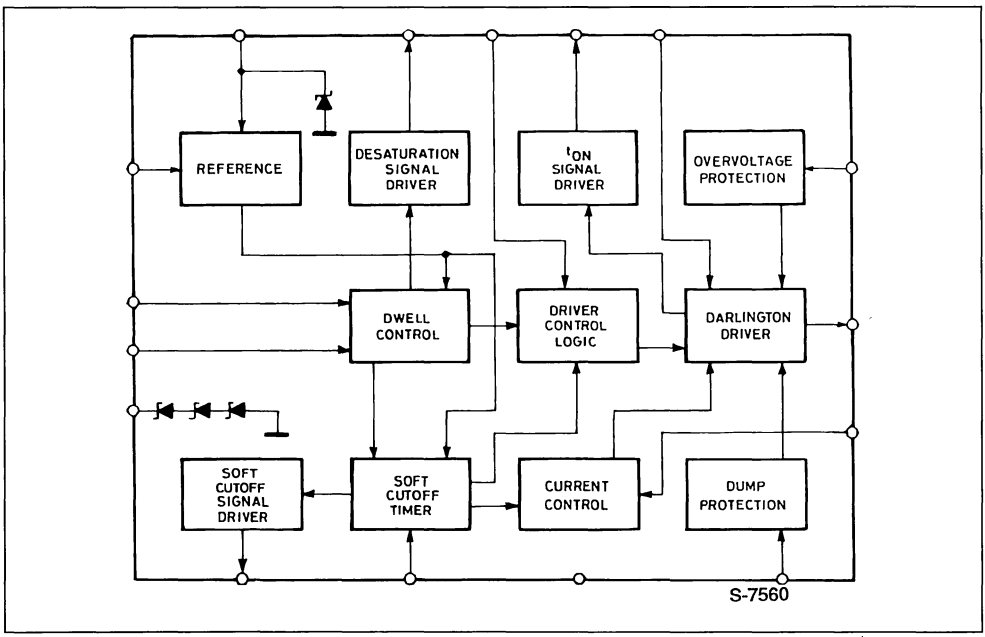
SO16J



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_R	Reverse Battery Voltage	– 14	V
V_D	Dump Voltage (t_n = 5ms, τ_f = 100ms)	100	V
P_{tot}	Power Dissipation at T = 90°C S016 DIP	1.2 0.65	W W
T_j, T_{stg}	Junction and Storage Temperature	– 55 to 150	°C

BLOCK DIAGRAM



THERMAL DATA (DIP-16)

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	90	°C/W

THERMAL DATA (SO-16)

$R_{th\ j\text{-}alumina}$*	Thermal Resistance Junction-alumina	Max	50	°C/W

(*) Thermal resistance junction-aluminia with the device soldered on the middle of an aluminia supporting substrate measuring 15 x 20mm ; 0.65mm thickness with infinite heatsink.

PIN FUNCTIONS (refer to fig. 3 for DIP-16 package)

N°	Name	Function
1	CONDUCTION TIME SIGNAL	A low level on this output signal indicates when the external darlington is in the ON condition i.e. when the current flows through the coil (t_{on} in fig. 1).
2	HALL-EFFECT INPUT	Hall-effect Pickup Input. A high level on this pin enables the current driving into te coil. The effective coil charge will be a function of the dwell control logic. A High to Low transition from the Hall-effect pickup is the signal for ignition actuation. The input signal, supplied by the open collector output stage of the Hall-effect sensor, has a duty cycle typically about 70%.
3	DWELL CONTROL	The average voltage on the capacitor C_2 connected between this pin and ground depends on the motor speed and the voltage supply. The comparison between V_{C2} and V_{C5} voltages determines the timing for the dwell control. The recommended value is 100nF using a 100KΩ resistor at pin 7. For the optimized operation of the device, C_2=C_5.
4	DWELL CONTROL TIMER	The capacitor C_5 connected between this pin and ground is charged when the Hall-effect output is high and is discharged at the High to Low transition of the Hall-effect signal. The recommended value is 100nF using a 100KΩ resistor at pin 7.
5	HALL SENSOR SUPPLY	This pin can be used to project the Hall-effect pickup against the voltage transients. The resistor R_a limits the currrent into the internal zener.
6	DESATURATION TIME SIGNAL	Open Collector Output Signal. This output is high when the external darlington is in desaturatiuon condition (current limitation), see t_d pulse in fig. 1.
7	REFERENCE VOLTAGE	A resistor R_{11} connected between this pin and ground sets the internal current used to drive the external capacitors of the dwell control (C_2 and C_5) and permanent conduction protection (C_1). The recommended value is 100KΩ.
8	PERMANENT CONDUCT. PROTECTION TIMER	A capacitor C_1 connected between this pin and ground determines the intervention delay of the permanent conduction protection, t_{pc} of the figure 2. With a 1µF capacitor and 100KΩ resistor R_{11} at pin 7 the typical delay is 1s.
9	PERMANENT CONDUCT. RESET OUTPUT (no available in Micropackage) (*)	A low pulse on this output detects the intervention of the permanent conduction protection, as shown in figure 2. Typically the duration of the time t_r is more than 100µs.
10	CURRENT SENSING INPUT (*)	Connection for coil current limitation. The current is measured on the sensing resistor R_s and divided on R_1/R_2 resistors. The current limitation value is given by : $I_{SENS} = \mathbf{Vsens} \frac{R_1 + R_2}{R_s \cdot R_2}$
11	DUMP PROTECTION (*)	The device is protected against the load dump. In load dump condition an internal circuit, based on a zener diode and a darlinton transistor, switches off the external darlington and short circuits the supply. By means of the external divider R8/R9 the protection threshold can be changed and is given as first approximation by : $V_{Dth} = 8.5 \cdot \frac{R_8 + R_9}{R_9} + 5 \cdot 10^{-4} \cdot R_8$ (the resistor R8 value must be higher than 4KΩ).
12	POWER SUPPLY (*)	Supply Voltage Input. A 7V (typ) zener is present at the input. The external resistor R_7 limits the current through the Zener for high supply voltages.

PIN FUNCTIONS (continued)

N°	Name	Function
13	GROUND	This pin must be connected to ground.
14	DRIVER COLLECTOR	The collector current of the internal driver which drives the external darlington is supplied through this pin. The external resistor R_{10} limits the dissipation in the I.C. The value of the resistor is a function of the darlington used and of the limiting current in the coil.
15	OVERVOLTAGE LIMITATION	The darlington is protected against overvoltage by means of an internal zener available at this pin. The external divider R_5/R_6 defines the limitation value, given as first approximation by : $V_{ovp} = (\frac{30}{R_5} + 5 \cdot 10^{-3}) \cdot R_6 + 30$
16	DRIVING STAGE OUTPUT	Current driver for the external darlington. To ensure stability and precision of T_{desat} C_3 and R_3 must be used. Recommended value for R_3 is 2KΩ in order not to change the open loop gain of the system. R_C may be added to C_3 to obtain greater flexibility in various application situations. C_3 and R_C values ranges are 1 to 100nF and 5 to 30KΩ depending on the external darlington type.

(*) These pins refer only to the DIP package type.
For the SO 16 version the permanent conduction reset output signal is not available and the pin 9 becomes the current sensing input. Pin 10 replaces the pin 11 function, pin 11 becomes the power supply input and pin 12 is used as the signal ground.

ELECTRICAL CHARACTERISTICS (V_S = 14 V, $-40°C \leq T_j \leq 125°C$ referred to application circuit of figure 3 regarding DIP-16 package version)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage		6		28	V
I_S	Supply Current	V_{12} = 4.5V			25	mA
V_Z	Zener Voltage (pin 12)	I_Z = 80mA	6.5		8.8	V
V_I	Sensor Input (pin 2) LOW Voltage HIGH		 2.5		 0.5	 V V
I_I	Sensor Input Current (pin 2)	V_I = LOW V_S = 6 to 16V	–12		–1	mA
V_{Hz}	Hall-cell Supply Zener Voltage (pin5)	I_{Hz} = 10mA	19	22	25	V
I_{HZ}	Hall-cell Supply Zener Current (pin5)	t = 10ms T_{AMB} = 25°C	100			mA
$V_{CE\ sat}$ (V_{14}–V_{16})	Series Darlington Driver Sat. Voltage	I_o = 70mA I_o = 150mA		 0.4	0.6 1.0	V V
V_{SENS}	Current Limit. Sensing Voltage (pin10)	V_S = 6 to 16V	200		400	mV
I_{3D} I_{3C} I_{3C}/I_{3D}	C2 Discharge Current C2 Charge Current	V_S = 6 to 16V (*) Note 1	0.2 5 6		3.4 20 35	µA µA
V_{OVZ}	External Darlington Overvoltage Protection Zener Voltage	I_{OVZ} = 5mA to 15mA T_{AMB} = 25°C	25	30	35	V
V_7	Reference Voltage		2.5		3.5	V
t_d	Desaturation Time	f = 40Hz V_S = 14V	0.6	1.2	1.57	ms

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PC}	Permanent Conduction Protection Time (pin 8) (see fig. 2)	V_I = H C_I = 1µF	1	3	5	s
V_1	Charging Angle Output Voltage LOW HIGH	 I_{SINK} = 0 I_{SINK} = 1mA I_{SOURCE} = 1.5mA I_{SOURCE} = 2.5mA	 3 5		 0.5 1.2	 V V V V
V_6	Desat. Time Output Low Voltage	$I_{6\ (sink)}$ = 0.5mA			0.7	V
I_{6L}	Desat. Time Leakage Current (pin6)	V_6 = 5V			10.5	µA
I_{9L}	Permanent Conduction Reset Leakage Current (pin9)	V_9 = 5V			10.5	µA

APPLICATION INFORMATION

Figure 1 : Main Waveforms.

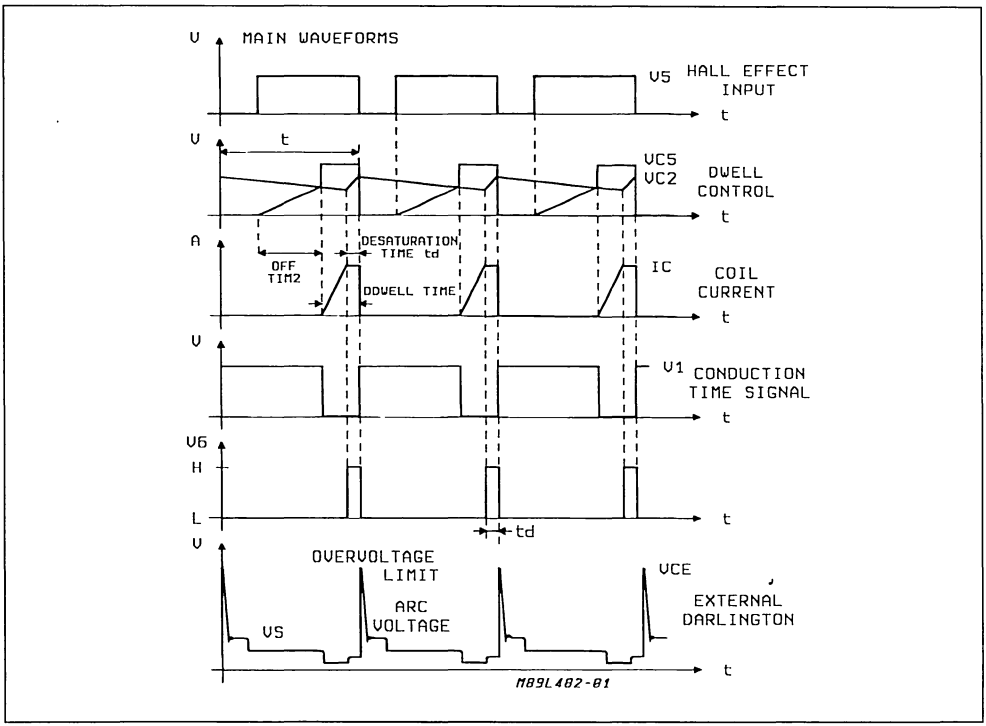


Figure 2 : Low Frequency Condition and Permanent Conduction Protection.

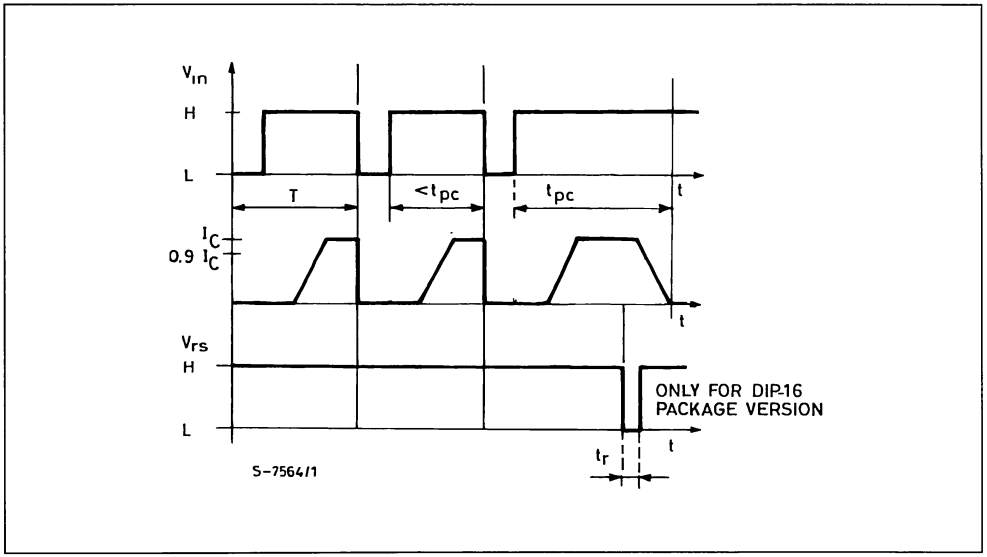


Figure 3 : Application circuit (DIP–16).

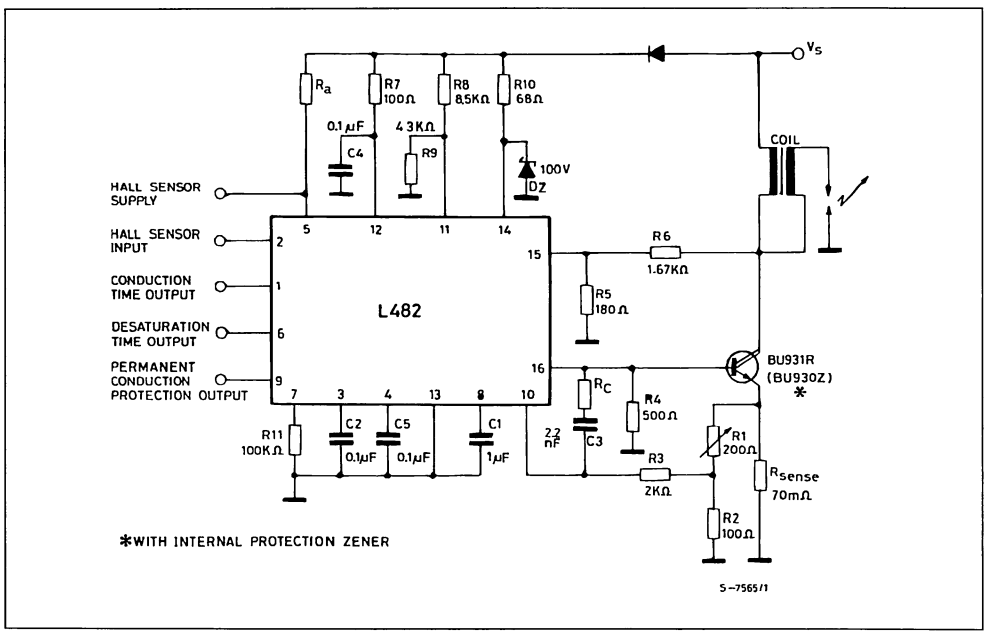
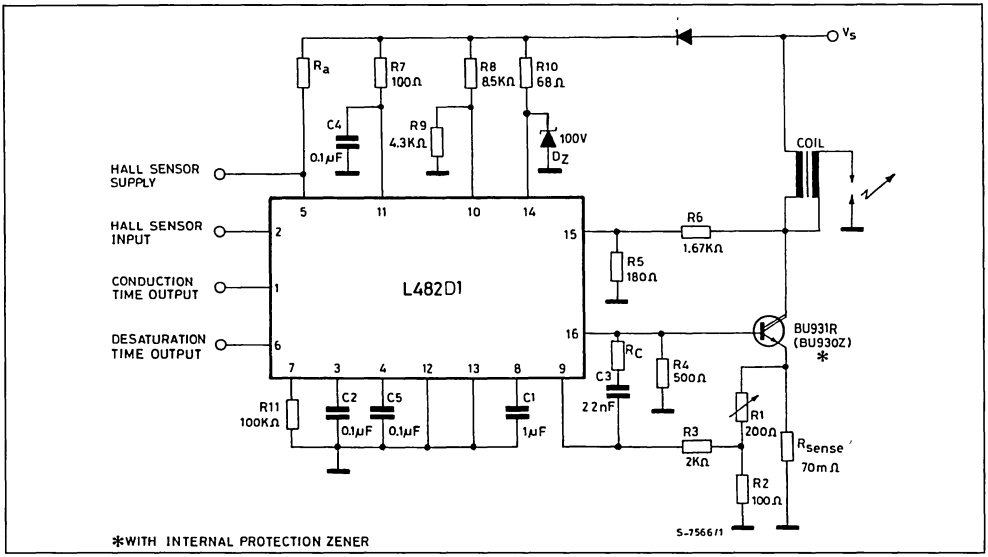


Figure 4 : Application Circuit (SO–16).



CIRCUIT OPERATION

The L482 control the conduction time (dwell) and the peak value of the primary current in the coil over the full range of operating conditions.

The coil current is limited to a predetermined level by means of a negative feedback circuit including a current sensing resistor, a comparator, the driver stage and the power switch.

The dwell control circuit maintains the output stage in its active region during current limitation. The time the output stage is in the active region (desaturation time) is sufficient to compensate for possible variations in the nergy stored due to the acceleration of the motor ; moreover this time is limited to avoid excessive power dissipation.

CONTROL OF THE DWELL ANGLE (fig. 1 and 4)

The dwell angle control circuit calculates the conduction time D for the output transistor in relation to the speed of rotation, to the supply voltage and to the characteristic of the coil.

On the negative edge of the Hall-effect input signal the capacitor C_2 begins discharging with a constant current I_{3D}. When the set peak value of the coil current is reached, this capacitor charges with a constant current $I_{3C} = 13.3 \times I_{3D}$ and the coil current is kept constant by desaturating the driver stage and the external darlington.

The capacitor C_5 starts charging on the positive edge of the Hall-effect input signal with a constant current I_{4C}.

The dwell angle, and consequently the starting point of the coil current production, is decided by the comparison between V_{C2} and V_{C5}. A positive hysteresis is added to the dwell comparator to avoid spurious effects and C_5 is rapidly discharged on the negative edge of Hall-effects input signal.

In this way the average voltage on C_2 increases if the motor speed decreases and viceversa in order to maintain constant the ratio $\frac{td}{T}$ at any motor speed.

td is kept constant (and not d = cost) to control the power dissipation and to have sufficient time to avoid low energy sparks during acceleration.

The charging time D – td depends on the coil and the voltage supply.

DESATURATION TIMES IN STATIC CONDITION-S.In static conditions, if $C_2 = C_5$ as recommended and if the values of the application circuit of fig. 3, 4 are used.

$$\frac{td}{T} = \frac{1}{1 + I_{3C}/I_{3D}}$$

DESATURATION TIMES IN LOW AND HIGH FREQUENCY OPERATION. Due to the upper limit of the voltage range of pin 3, if the components of fig. 3, 4 are used, below 10Hz (300RPM for a 4 cylinder engine) the OFF time reaches its maximum value (about 50ms) and then the circuit gradually loses the control of the dwell angle because D = T – 50ms

Over 200Hz (6000RPM for a 4 cylinder engine) the available time for the conduction is less than 3.5ms.

If the used coil is 6mH, 6A, the OFF time is reduced to zero and the circuit loses the dwell angle control.

TRANSIENT RESPONSE. The ignition system must deliver constant energy even during the condition of acceleration and deceleration of the motor below 80Hz/s. These conditions can be simulated by means of a signal generator with a linearly modulated frequency between 1Hz and 200Hz (this corresponds to a change between 30 and 6000RPM for a 4 cylinders engine.

CURRENT LIMIT. The current in the coil is monitored by measuring the I_{sense} current flowing in the sensing resistor R_S on the emitter of the external darlington. I_{sense} is given by :

$$I_{sense} = I_{coil} + I_{16}$$

When the voltage drop across R_S reaches the internal comparator threshold value the feedback loop is activated and I_{sense} kept constant (fig. 1) forcing the external darlington in the active region. In this condition :

$$I_{sense} = I_{coil}$$

When a precise peak coil current is required R_5 must be trimmed or an auxiliary resistor divider (R_1, R_2) added :

$$Icpeak\ (A) = \frac{V_{SENS}}{R_S} \left(\frac{R_1}{R_2} + 1 \right)$$

PROTECTION CIRCUIT

PERMANENT CONDUCTION PROTECTION

The battery voltage is applied to ignition module by means of the ignition key. In these conditions, with the motor stopped, it is necessary that there is no permanent conduction in the ignition coil irrespective of the polarity of the input signal.

The L482 incorporates a timing circuit to implement this protection ; the duration of the intervention is set by means of a capacitor C_1 at pin 8 = 1µF, and R_{11} = 100kΩ, when the input signal is high for more than 1 s, the coil current gradually decreases down to zero to avoid spurious sparks (see fig. 2).

This timing allows normal operation of the module above 30RPM.

DARLINGTON OVERVOLTAGE LIMITATION

The darlington is protected against overvoltage by means of an external divider R_5/R_6 (pin 15) and an internal zener. This zener drives the external darlington in order to limit the collector voltage.

REVERSE BATTERY PRTOTECTION. Due to the presence of external impedance at pin 5, 10, 11, 14, 15, L482 is protected against reverse battery voltage.

DUMP PROTECTION.

The load dump protection withstands up to 100V with a decay time ≤ 300ms. The intervention threshold for load dump is fixed by means of an external divider connected to pin 11 (DIP-16 package version) or to pin 10 using a Micropackage type.

NEGATIVE SPIKE PROTECTION.If correct operation is requested also during short negative spikes, the diode DS and capacitor C_S must be used.

USE OF THE IC ELECTRONIC ADVANCE SYSTEM

When the device is digitally controlled the control unit transmits a suitable input signal to the power module, receiving in turn information that allows the control of the dwell and the on time of the final transistor.

For this reason L482 provides the following outputs :

- a time signal equal to the time in which the final Darlington is in the active region i.e. when the coil current is limited (V_{ds}) as shown in figure 1. This signal must be TTL compatible.

- a TTL compatible output from the timing circuit (V_{rs} in figure 2). This pulse, available only using the DIP-16 package version is present after the protection against cranking transients.

- a time signal equal to the time in which the final Darlington, is in "on" condition (V_{on}) i.e. when the current flows through the coil, see fig. 1.

OTHER APPLICATION INFORMATION

If the supply voltage is disconnected - or the battery wire is broken - while the current is flowing through the coil, the external diode D_1 keeps the coil current from recirculating into the device : in this way both device and darlington are protected.

MAGNETIC PICKUP IGNITION CONTROLLER

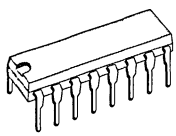
- DIRECT DRIVING OF THE EXTERNAL DARLINGTON
- OPERATES WITH A WIDE RANGE OF MAGNETIC PICKUP TYPES
- CHARGING ANGLE (DWELL) CONTROL
- COIL CURRENT PEAK LIMITATION
- CONTINUOUS COIL CURRENT PROTECTION
- TACHOMETER SIGNAL OUTPUT
- EXTERNAL DARLINGTON OVERVOLTAGE PROTECTION
- LOAD DUMP AND REVERSE BATTERY PROTECTION
- POSSIBILITY OF SPARK POINT DELAYING (ANTI KNOCK SYSTEM)

DESCRIPTION

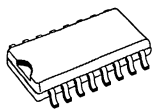
The L484 is an integrated circuit designed for use with an NPN darlington in breakerless ignition systems with magnetic pickup sensors and high energy ignition coils.

A key feature of the L484 is flexibility. It can be used with a wide variety of magnetic sensors thanks to the special design which has two input pins from the pickup ; the first is the zero crossing detector for the ignition command and the second pin is used to calculate the dwell time. Moreover another pin is used to adapt the L484 to various pickup types.

Other features of the device include darlington overvoltage protection, dump protection, a supply voltage range of 6-28 V.



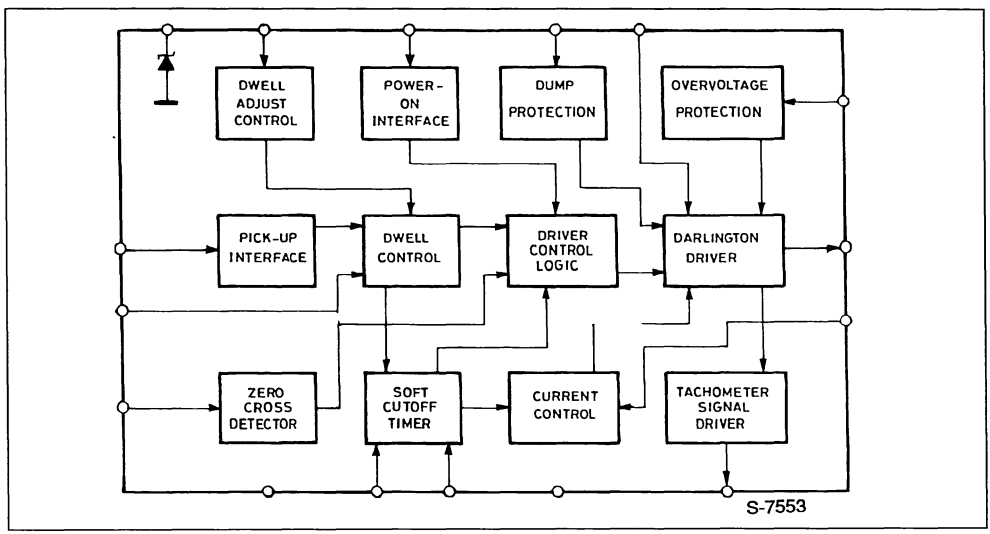
DIP16



SO16

ORDERING NUMBERS : L484 (DIP16)
L484D1 (SO16)

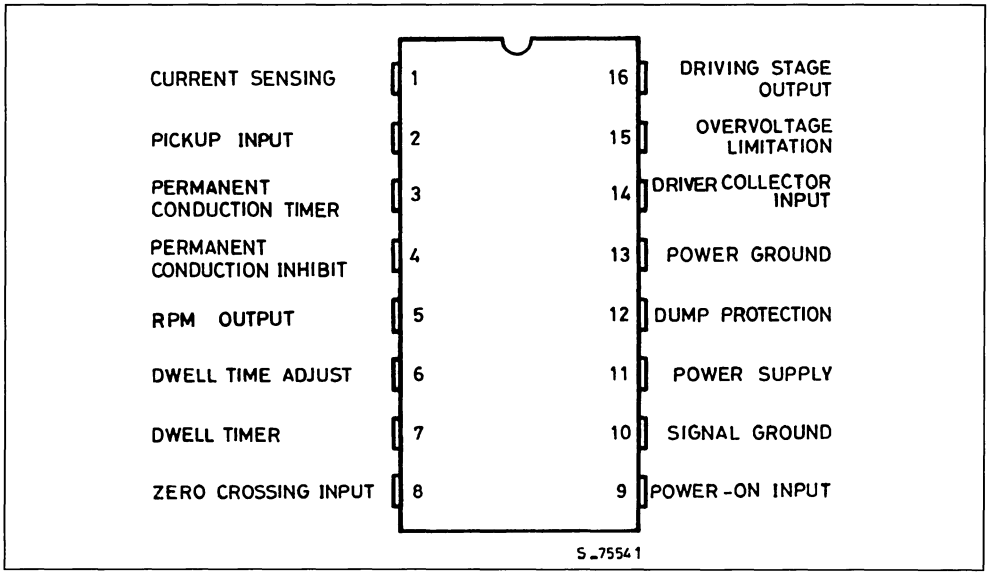
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_R	Reverse Battery Voltage	– 14	V
V_D	Dump Voltage	100	V
P_{tot}	Power Dissipation at T_{amb} = 90°C	0.75	W
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

PIN CONNECTION



THERMAL DATA (DIP-16)

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

THERMAL DATA (SO-16)

$R_{th\ j\text{-}al}$	Thermal Resistance Junction-alumina	Max	50	°C/W

PIN FUNCTIONS (refer to fig. 2)

N°	Name	Function
1	CURRENT SENSING INPUT	Connection for Coil Current Limitation. The current is measured on the sense resistor R_{SENS} and divided on R1/R2. The current limitation value is given by : $I_{SENS} = \frac{R1 + R2}{R_{SENS}\ R2}$
2	PICKUP INPUT	Magnetic Pickup Signal Input. This pin sets the dwell time, i.e. the max negative pickup voltage value starting from which the device can drive the current into the coil. The real dwell time will be a function of the dwell control logic. Increasing the resistor R11 the maximum conduction time increases. The max input current foreseen is 2mA.
3	PERMANENT CONDUCT. PROTECTION TIMER	A capacitor C1 connected between this pin and ground sets the delay of the permanent conduction protection in the coil current. Using a 50nF capacitor the typical desaturation time delay for the protection is 75ms.
4	PERMANENT CONDUCT. PROTECTION INHIBIT	A low level on this input (max 0.7V) disables the protection, irrespective of the state of pin 3. If the protection is used this pin must be left open.
5	RPM OUTPUT	Open collector output signal which is at a low level when the final darlington is in ON status. The current is internally limited at 10mA.
6	DWELL TIME ADJUST	At high motor rotation speeds, i.e. when the peak value of the magnetic pick-up signal exceedes 6V using R12 = 100KΩ, this pin may be used to vary the dwell ratio. Adding a resistor in series R_a between this pin and pin 11 the desaturation time is reduced. It is therefore possible to use this pin to adapt the L484 to various pickup types. The maximum value of the resistor R_a is 200KΩ.
7	DWELL CONTROL TIMER	A capacitor C2 connected between this pin and ground sets the timing for the dwell control. The recommended value is 100nF. The resistors R_b/R_c provide an hysteresis to confirm ON state and avoid spurious sparks.
8	ZERO CROSSING INPUT	Zero cross detector input of the magnetic pickup signal for the ignition actuation. At high motor rotation speeds, the external resistor R12 may be used to vary the desaturation time ratio, to adapt the L484 to various signal waveforms of time magnetic pick-up. Reducing the resistor value the dwell time increases. Typically the range of values for resistor R12 is from 50KΩ to 150KΩ.
9	POWER-ON INPUT	A low level on this pin forces the external darlington into conduction particularly useful in anti knock system. This function is particularly useful in antiknock system because provides a spark time delay. Anyway the current limitation, the permanent conduction protection and the dump protection are operating even when pin 9 is at a low level. If this function is not used it must be left open.
10	SIGNAL GROUND	This pin must be connected to ground.
11	POWER SUPPLY	Supply Voltage Input. A 7V (typ) zener is present at the input. The external resistor R9 limits the current through the zener for higher supply voltages.

* this function is particularly useful in antiknock systeme because provides a spark time delay. anyway the current limitation, the pemanent con duction protection and the dump protection are operating even when pin 9 is at a low level.

PIN FUNCTIONS (continued)

N°	Name	Function
12	DUMP PROTECTION	The device is protected against the load dump. In load dump condition an internal circuit, based on a zener diode and a darlington transistor, switches off the external darlington and short circuits the supply. By means of the external divider R8/R9 the protection threshold can be changed and is given as first approximation by : $V_{Dth} = 8.5 \left(\frac{R8 + R9}{R9} \right) + 5 \cdot 10^{-4} R8$ (the resistor R9 value must be higher than 4KΩ).
13	POWER GROUND	This pin must be connected to ground.
14	DRIVER COLLECTOR INPUT	The collector current for the internal driver which drives the external darlington is supplied through this pin. The external resistor R10 limits the dissipation in the IC. The value this resistor depends on the darlington used and on the limiting current in the coil.
15	OVERVOLTAGE LIMITATION	The external darlington is protected against overvoltage by means of an internal zener available at this pin. The external divider R5/R6 defines the limitation value, typically given by : $V_{ovp} = \left(\frac{30}{R5} + 5 \cdot 10^{-3} \right) \cdot R6 + 30$
16	DRIVING STAGE OUTPUT	Current Driver for the External Darlington. To ensure stability on the current limitation loop a capacitor C3 (typically 2.2nF, this value depending on the darlington used) must be connected between this pin and the current sensing input (pin 1).

ELECTRICAL CHARACTERISTICS (V_S = 14.4V ; T_J = - 40 to 125°C unless otherwise specified ; referred to the test circuit)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage		6		28	V
V_{IS}	Input Stage Voltage (pin 2 with 10KΩ resistor)		160	200	240	mV
V_{TH}	On Pick-up Thresh. Voltage at LOW RPM (pin 2)		V_{IS}–30		V_{IS}+30	mV
V_{SENS}	Current Limitation Sensing Voltage (pin 1)	V_S = 6 to 16V	200		320	mV
V_{ZC}	Zero Crossing Thresh. Voltage (pin 8)		3	20	65	mV
V_H	Hysteresis Voltage (pin 8)		100		200	mV
I_{7C}	$C_{D\ WELL}$ Charge Current	at LOW RPM	0.7		3	µA
I_{7D}	$C_{D\ WELL}$ Discharge Current	$V_{pick\text{-}up}$ = 0.5V ; or pin 6 not connected	7		30	µA
I_{7D}/I_{7C}		(*) Note 1	7		15	
I_{7C}	$C_{D\ WELL}$ Charge Current	at HIGH RPM	8		33	µA
I_{7D}	$C_{D\ WELL}$ Discharge Current	$V_{pick\text{-}up}$ = 9V	13		44	µA
I_{7D}/I_{7C}		(**) Note 2	0.7		3.2	
V_{pin3}	Threshold Voltage	T_{amb} = 25°C	0.85		4	V
I_3	Output Current	(***) Note 3			3	µA
V_{Cp}	Continuous Coil Current Protection Inhibit LOW Voltage (pin 4).		0		0.7	V
V_{CEsat}	Series Darlington Driver Saturation Voltage ($V_{pin\ 14\ -\ 16}$)	I_{pin14} = 150mA I_{pin14} = 50mA		0.4	1 0.6	V V
V_Z	Zener Volt. Pin 11	I_{pin11} = 140mA	6.5		8.8	V
V_{OVZ}	External Darlington Overvoltage Protection Zener Voltage	T_{amb} = 25°C ; I_{pin15} = 5 to 15mA	25		35	V
I_{09}	Pin 9 Output Current in Low Status	V_9 = 0V			3	mA
V_{CH}	Tachometer Signal Output LOW Voltage. (pin 5)	ON Condition I_{sink} = 0.5mA			0.7	V
I_{CH}	Output Leakage (pin 5)	OFF Condition V_{pin5} = 5V			10	µA

DUMP PROTECTION

Symbol	Paramater	Test Conditions	Min.	Typ.	Max.	Unit
V_{DZ}	Zener Dump (pin 12)	I_{pin12} = 2mA	7.5		9.5	V

(*) Note 1 : TD/T is given by the formula :

$$\frac{TD}{T} = \frac{1}{1 + I7D/I7C}$$

(**) Note 2 :

$$\frac{TD}{T} = \frac{K}{1 + I7D/I7C}$$

K value depends on the pick–up used in the application ; typically K = 0.1
(***) Note 3 : the permanent conduction protection is guaranteed over the full temperature range

CIRCUIT OPERATION

The L484 controls the charging angle (dwell) and the peak value of the primary current in the coil over the full range of operating conditions.

The coil current is limited to a predetermined level by means of a negative feedback circuit including a current sensing resistor, a comparator, the driver stage and the power switch.

The dwell control circuit keeps the output stage in its active region during current limitation. The time the output stage is operating in the active region (desaturation time), is sufficient to compensate for possible variation in the energy stored due to the acceleration of the motor ; moreover this time is limited to avoid excessive power dissipation.

MAGNETIC PICK–UP CHARACTERISTICS

The typical magnetic pickup waveforms are shown in fig. 1, the amplitude of the signal being a function of the frequency. However on the market there are many types of magnetic pickup, of which the waveforms may differ very much. Adjusting the value of the resistor R_{11} on pin 2 and/or adding a resistor R_a between the pin 6 (dwell adjust) and pin 11, as shown in the application circuit, it is possible to adapt the L484 to a wide range of magnetic pickup waveforms.

Particularly by means of the resistor R_{11} on pin 2 it is possible to define the maximum advance of the conduction start into the coil . This is very useful at high pick–up frequency.

CONTROL OF THE DWELL ANGLE

The dwell angle control circuit defines the conduction time of the output darlington, versus the speed of rotation, the supply voltage and the characteristics of the coil.

In each cycle the time the transistor operates in the active region is compared with a reference time and the error signal amplified to advance or delay the conduction in the next cycle. To limit the power dissipation the desaturation time is typically fixed to 10% of the period T.

At very low frequencies the ON thershold is fixed at 200mV of the input signal and the desaturation time is mainly determined by the peak waveform. This positive threshold also prevents permanent conduction when the motor is stopped. When the input frequency increases the dwell control gradually sets the desaturation time to 10% of the period. At higher frequencies the ON threshold becomes negative to permit a conduction angle of more than 50% always keeping desaturation time to 10% of the period.

CURRENT LIMITING

The current in the coil is measured by means of a voltage drop across a suitable resistor in the emitter lead of the power transistor. When the threshold voltage (260mV typ) is reached, the coil current is kept constant via a feedback loop.

DARLINGTON OVERVOLTAGE LIMITATION

The darlington is protected against overvoltage by means of an external divider R_5/R_6 (pin 15) and an internal zener. This zener drives the external darlington in order to limit the collector voltage.

CHARGING ANGLE SIGNAL OUTPUT

This signal is intended for tachometer applications (pin 5). It consists of an open collector stage with current internally limited at 10mA

"POWER ON" SIGNAL INPUT

In the low status this input forces the external darlington into conduction (pin 9). This control input can be used together with the conduction time information coming from pin 5 to bypass the normal dwell time calculation. When an external logic control is used to recognize particular engine condition (as in anti Knock system).

PROTECTION CIRCUITS

PERMANENT CONDUCTION PROTECTION

This function is intended to prevent continuous current conduction in the final stage when the magnetic pickup is open or intermittent. The duration of the intervention is set by means of a capacitor 1 at pin 3. Grounding pins 3 or 4, this protection is eliminated. The inhibit function at pin 4 is particularly useful when an external logic control is used to disable the permanent conduction protection.

REVERSE BATTERY AND DUMP PROTECTION

Due to the external resistors R_6, R_7, R_8, R_{10} the device is protected against reverse battery. The load dump protection withstands up to 100V with a decay time ≤ 300ms. The intervention threshold for load dump is fixed by means of an external divider connected to pin 11.

OTHER APPLICATION INFORMATION

If the supply is voltage disconnected - or the battery wire is broken - while the current is flowing through the coil, the external diode D_1 keeps the coil current from recirculating into the device : in this way both device and darlington are protected.

The zener diode Dz, connected between pin 14 and GND, allows to withstand positive spikes up to 200V.

The device - used in the recommended application circuit - satisfies the ISO/DP 7637/1 overvoltage standard.

Figure 1 : Typical Magnetic Pick–up Waveform and L484 Response at low and high fequency.

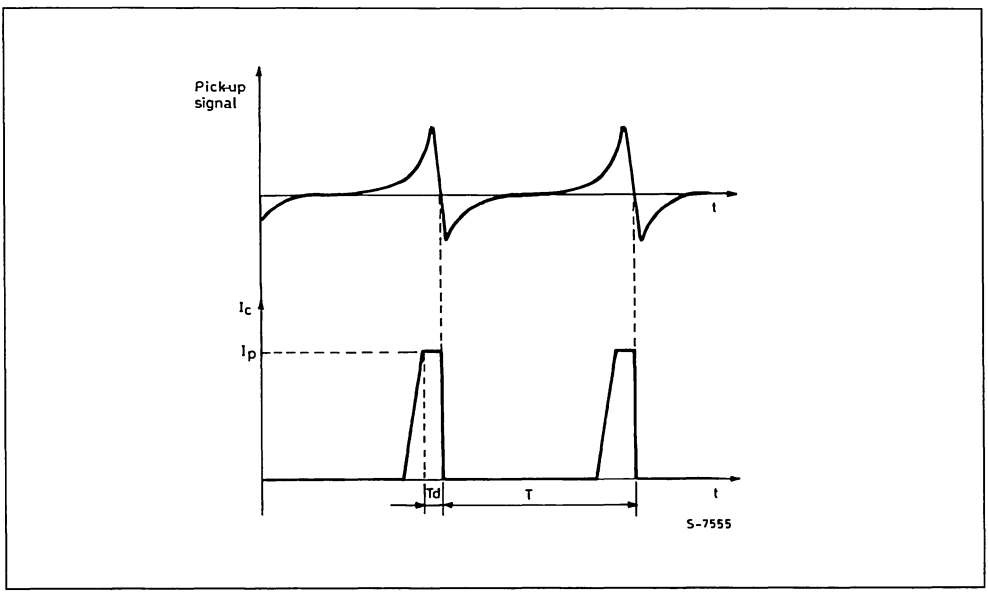


Figure 1 : Typical Magnetic Pick-up Waveform and L484 Response at Low and High Frequency (continued).

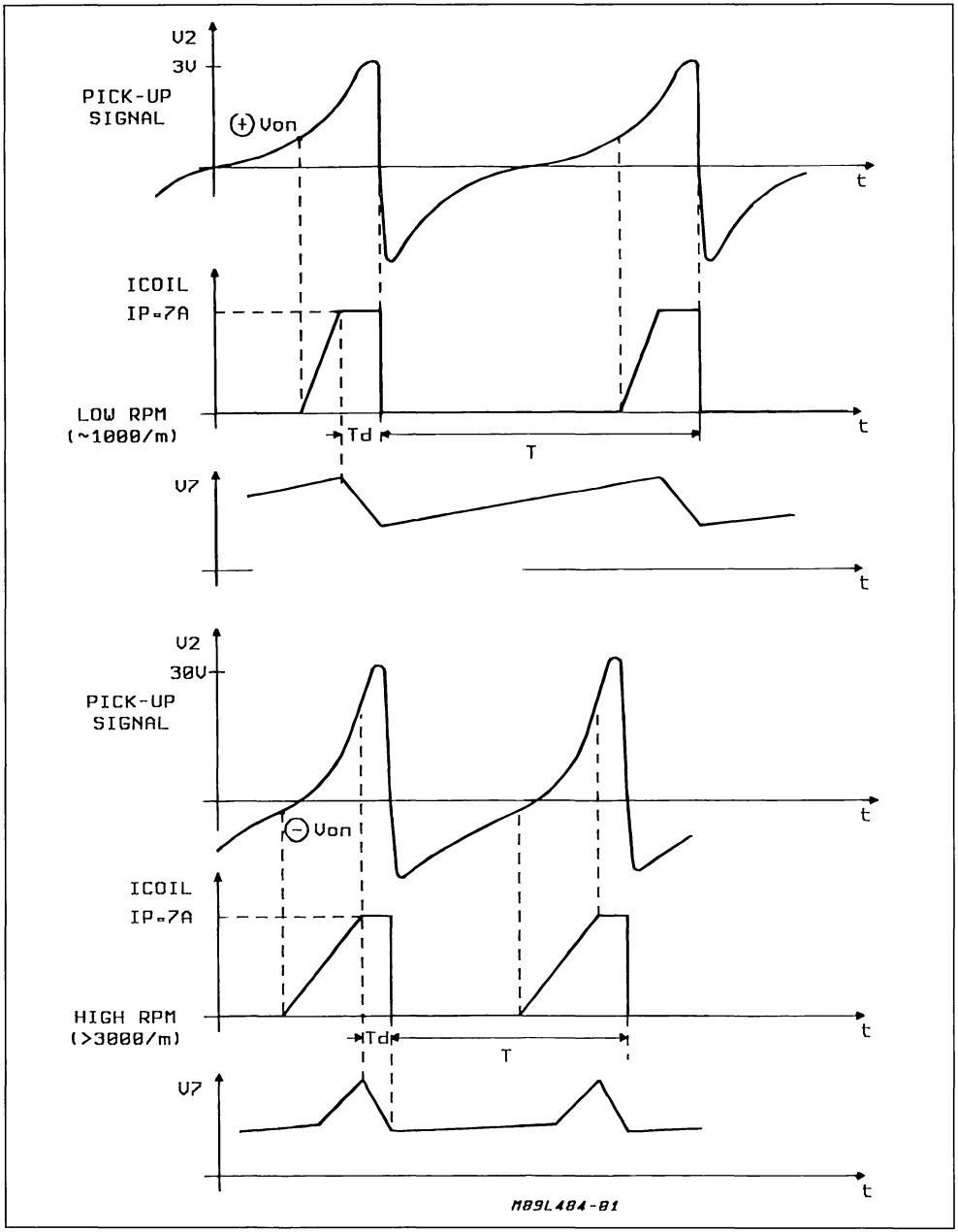
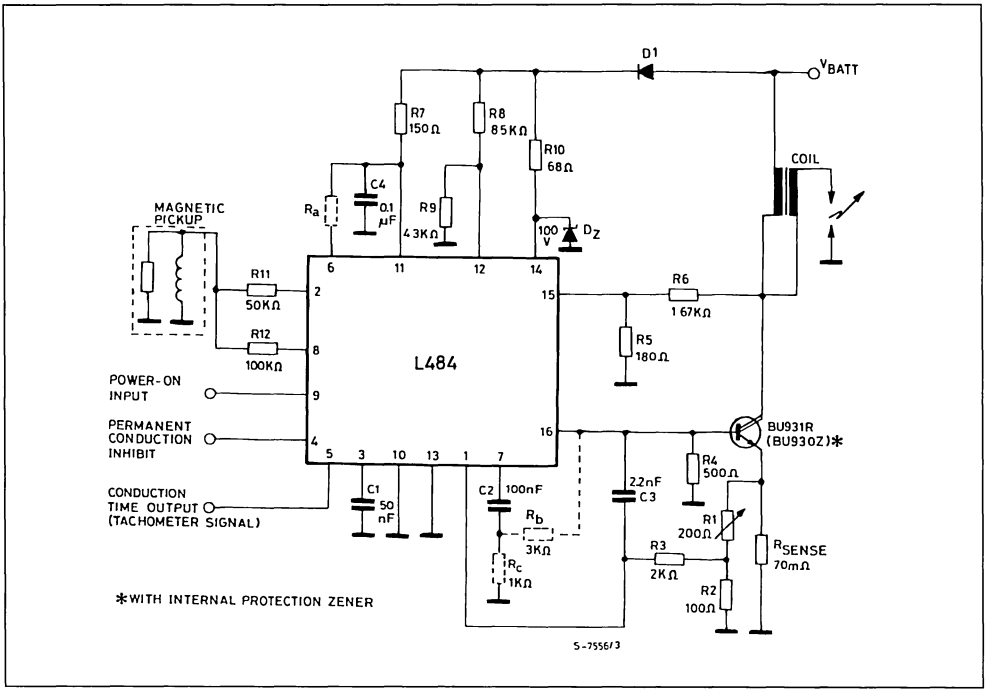
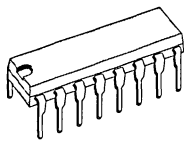


Figure 2 : Application Circuit.



HALL EFFECT PICKUP IGNITION CONTROLLER

- DIRECT DRIVING OF THE EXTERNAL POWER DARLINGTON
- COIL CURRENT CHARGING ANGLE (dwell) CONTROL
- PROGRAMME COIL CURRENT PEAK LIMITATION
- PROGRAMMABLE DWELL RECOVERY TIME WHEN 94% NOMINAL CURRENT NOT REACHED
- RPM OUTPUT
- PERMANENT CONDUCTION PROTECTION
- OVERVOLTAGE PROTECTION FOR EXTERNAL DARLINGTON
- INTERNAL SUPPLY ZENER
- REVERSE BATTERY PROTECTION



DIP16 SO16

ORDERING NUMBERS : L497B (DIP16)
L497D1 (SO16)

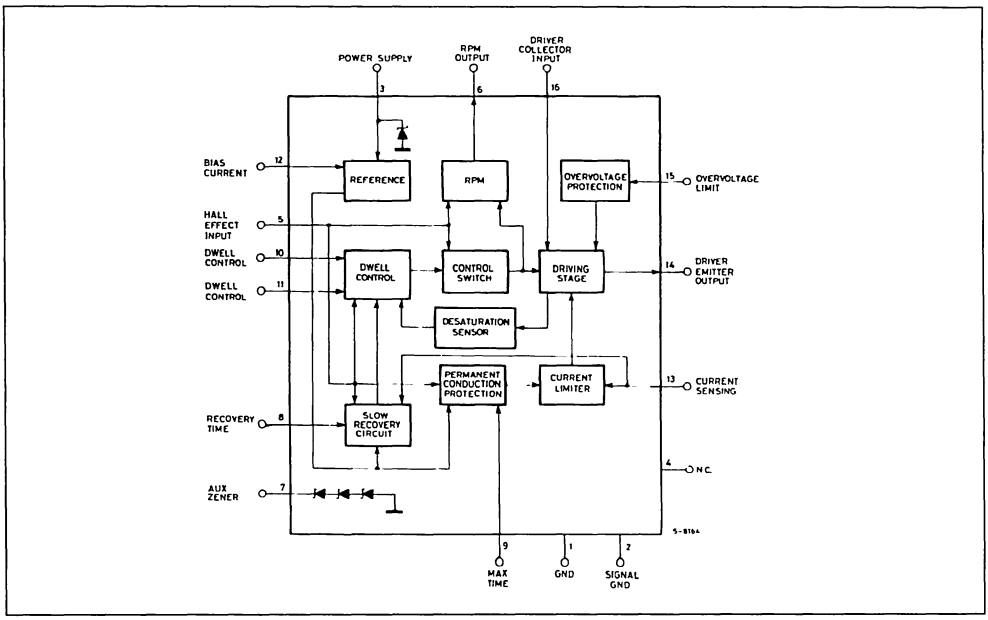
DESCRIPTION

The L497 is an integrated electronic ignition controller for breakerless ignition systems using Hall effect sensors.

The device drives an NPN external darlington to control the coil current providing the required stored energy with low dissipation.

A special feature of the L497 is the programmable time for the recovery of the correct dwell ratio t_d/T when the coil peak current fails to reach 94% of the nominal value. In this way only one spark may have an energy less than 94% of the nominal one during fast acceleration or cold starts.

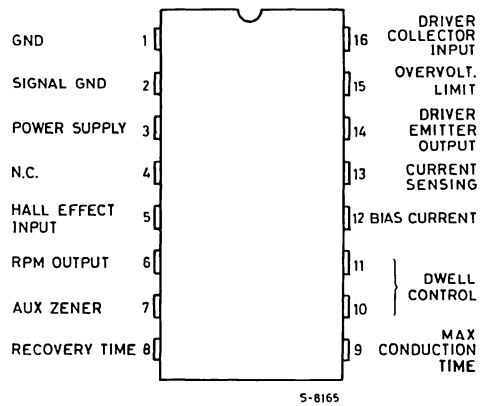
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_3	D.C. Supply current Transient Supply Current (t_f fall time constant = 100ms)	200 800	mA mA
V_3	Supply Voltage	Int. Limited to V_{z3}	
V_6	RPM Voltage	28	V
I_{16}	D.C. Driver Collector Current Pulse " " ($t \leq 3ms$)	300 600	mA mA
V_{16}	Driver Collector Voltage	28	V
V_{15}	D.C. Overvoltage Zener Current Pulse " "$t_{fall} = 300\mu s$, t_{reo} Repetition Time $\geq$ 3ms	 15 35	 mA mA
V_R	Reverse Battery Voltage if Application Circuit of Fig. 4 is used	−16	V
T_j, T_{stg}	Junction and Storage Temperature Range	−55 to 150	°C
P_{tot}	Power Dissipation at $T_{aluminia}$ = 90°C for SO-16 T_{amb} = 90°C for DIP-16	 1.2 0.65	 W W

PIN CONNECTION (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient for DIP-16	Max	90	°C/W
$R_{th\ j\text{-}alumin}$ (*)	Thermal Resistance Junction-alumina for SO-16	Max	50	°C/W

(*) Thermal resistance junction-aluminia with the device soldered on the middle of an aluminia supporting substrate mesuring 15 x 20 ; 0.65mm thickness.

PIN FUNCTIONS (refer to fig. 4)

N°	Name	Function
1	GND	This pin must be connected to ground.
2	SIGNAL GND	This pin must be connected to ground.
3	POWER SUPPLY	Supply Voltage Input. An internal 7.5V (typ. value) zener limits the voltage at this pin. The external resistor R_5 limits the current through the zener for high supply voltages.
4	N.C.	This pin must be connected to ground or left open.
5	HALL-EFFECT INPUT	Hall-effect Pickup Signal Input. This input is the dwell control circuit output in order to enable the current driving into the coil. The spark occurs at the high-to-low transition of the hall-effect pickup signal. Furthermore this input signal enables the slow recovery and permanent conduction protection circuits. The input signal, supplied by the open collector output stage of the Hall effect sensor, has a duty cycle typically about 70%. V_5 is internally clamped to V_3 and ground by diodes.
6	RPM OUTPUT	Open collector output which is at a low level when current flows in the ignition coil. For high voltages protection of this output, connection to the pin 7 zener is recommended. In this situation R_8 must limit the zener current, too, and R_1 limits pin 6 current if RPM module pad is accidentally connected to V_S.
7	AUX. ZENER	A 21V (typ) General Purpose Zener. Its current must be limited by an external resistor.
8	RECOVERY TIME	A capacitor connected between this pin and ground sets the slope of the dwell time variation as it rises from zero to the correct value. This occurs after the detection of $I_{coil} \leq 94\% I_{nom}$, just before the low transition of the hall-effect signal pulse. The duration of the slow recovery is given by : $t_{src} = \mathbf{12,9\ R_7\ C_{src}}$ (ms) where R_7 is the biasing resistor at pin 12 (in KΩ) and C_{src} is the delay capacitor at pin 8 (in µF).
9	MAX CONDUCTION TIME	A capacitor connected between this pin and ground determines the intervention delay of the permanent conduction protection. After this delay time the coil current is slowly reduced to zero. Delay Time T_p is given by : $T_p = \mathbf{16\ C_p\ R_7}$ (ms) where R_7 is the biasing resistor at pin 12 (in KΩ) and C_P is the delay capacitor at pin 9 (in µF).
10	DWELL CONTROL TIMER	The capacitor C_T connected between this pin and ground is charged when the Hall effect output is High and is discharged at the High to Low transition of the Hall effect signal. The recommended value is 100nF using a 62KΩ resistor at pin 12.
11	DWELL CONTROL	The average voltage on the capacitor C_W connected between this pin and ground depends on the motor speed and the voltage supply. The comparison between V_{CW} and V_{CT} voltage determines the timing for the dwell control. For the optimized operation of the device $C_T = C_W$; the recommended value is 100nF using a 62kΩ resistor at pin 12.
12	BIAS CURRENT	A resistor connected between this pin and ground sets the internal current used to drive the external capacitors of the dwell control (pin 10 and 11), permanent conduction protection (pin 9) and slow recovery time (pin 8). The recommended value is 62KΩ.

PIN FUNCTIONS (continued)

N°	Name	Function
13	CURRENT SENSING	Connection for the Coil Current Limitation. The current is measured on the sensing resitor R_S and divided on R_{10}/R_{11} resistors. The current limitation value is given by : $I_{sens} = 0.32 \cdot \frac{R_{10} + R_{11}}{R_S \cdot R_{11}}$
14	DRIVER EMITTER OUTPUT	Current Driver for the External Darlington. To ensure stability and precision of T_{desat} C_c and R_9 must be used. Recommended value for R_9 is 2 KΩ in order not to change the open loop gain of the system. R_c may be added to C_c to obtain greater flexibility in various application situations. C_c and R_c values ranges are 1 to 100nF and 5 to 30KΩ depending on the external darlington type.
15	OVERVOLTAGE LIMIT	The darlington is protected against overvoltage by means of an internal zener available at this pin and connected to pin 14. The external divider R_3/R_2 defines the limitation value given by : $V_{ovp} = (\frac{22.5}{R_3} + 5.10^{-3})\ R_2 + 22.5$
16	DRIVER COLLECTOR INPUT	The collector current of the internal driver which drives the external darlington is supplied through this pin. Then the external resistor R_6 limits the maximum current supplied to the base of the external darlington.

ELECTRICAL CHARACTERISTICS (V_S = 14.4V, –40°C ≤ T_J ≤ 125°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_3	Min Op. Voltage		3.5			V
I_3	Supply Current	V_3 = 6V V_3 = 4V	5 7	18	25 16	mA mA
V_S	Supply Voltage				28	V
V_{Z3}	Supply Clamping Zener Voltage	I_{Z3} = 70mA	6.6	7.5	8.2	V
V_5	Input Voltage	Low Status High Status	 2.5		0.6	V V
I_5	Input Current	V_5 = LOW	–400		–50	µA
V_{16-14}	Darlington Driver Sat. Current	I_{14} = 50mA I_{14} = 180mA			0.5 0.9	V V
V_{SENS}	Current Limit. Sensing Voltage	V_S = 6 to 16V	260	320	370	mV
I_{11C}	C_W Charge Current	V_S = 5.3 to 16V V_{11} = 0.5V T = 10 to 33ms	– 11.0	– 9.3	– 7.8	µA
I_{11D}	CW Charge Current	V_S = 5.3 to 16V V_{11} = 0.5V T = 10 to 33ms	0.5	0.7	1.0	µA
I_{11C} / I_{11D}		VS = 5.3 to 16V V_{11} = 0.5V T = 10 to 33ms See note 1	7.8		22.0	
$\frac{I_{SRC}}{I_{SENSE}}$	Percentage of Output Current Determining the Slow Recovery Control Start (fig. 2), note 2		90	94	98.5	%
T_{SRC}	Duration of Altered t_d/T Ratio after SRC Function Start (fig. 2)	C_{SRC} = 1µF R_7 = 62KΩ		0.8		s
V_{Z15}	External Darlington over Voltage Protection Zener Voltage	I_{15} = 5mA I_{15} = 2mA	19 18	22.5 21.5	26 25	V V
T_P	Permanent Conduction Time	V_5 = High C_P = 1µF R_7 = 62KΩ	0.4	1.1	1.8	s
V_{6SAT}	RPM Output Saturation Voltage	I_6 = 18.5mA I_6 = 25mA			0.5 0.9	V V
$I_{6\ leak}$	RPM Output Leakage Current	V_6 = 20V			50	µA
V_{Z7}	Auxiliary Zener Voltage	I_7 = 200mA	18		27	V
V_{12}	Reference Voltage		1.20	1.25	1.35	V

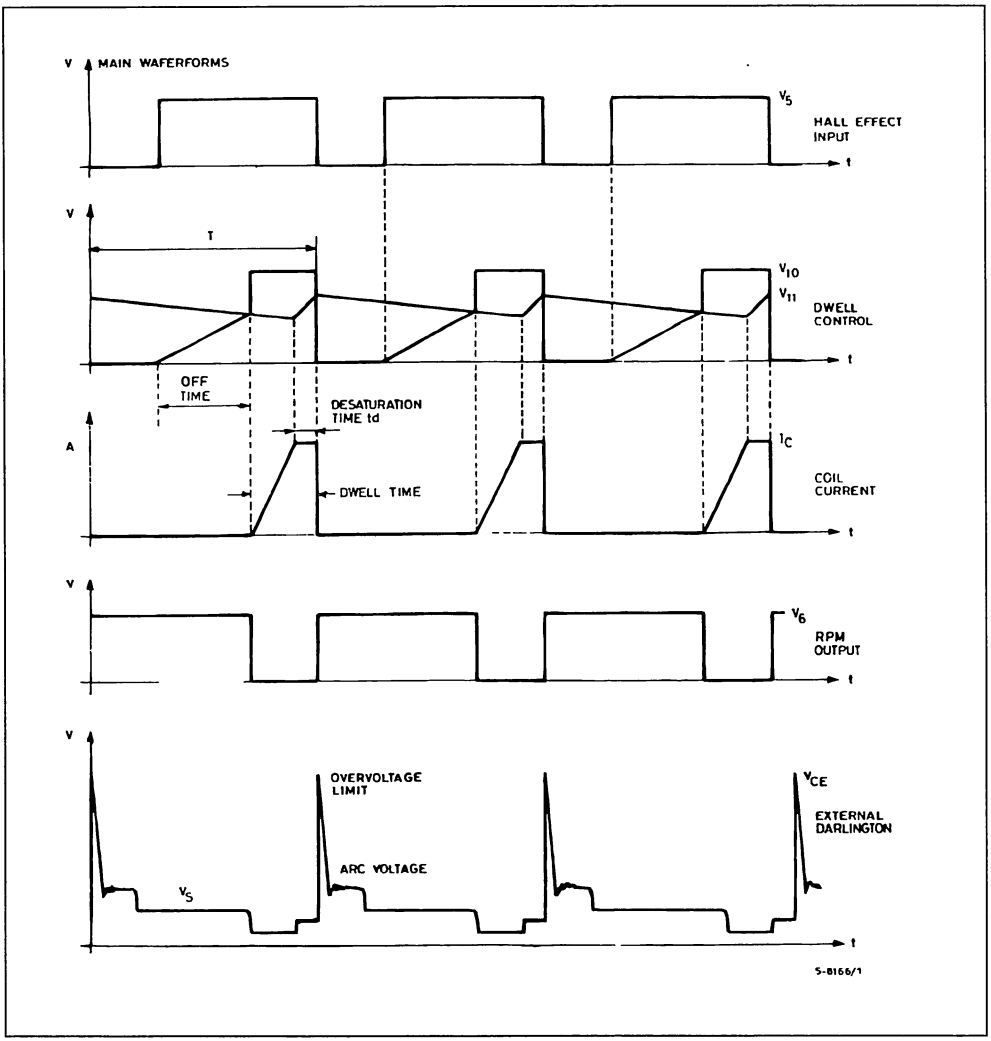
Notes: 1. td/t desaturation ratio is given by:

$$\frac{td}{T} = \frac{1}{1 + I_{11C} / I_{11D}}$$

2. I_{SENSE} = I_{COIL} when the external Darlington is in the active region

APPLICATION INFORMATION

Figure 1 : Main Waveforms.



DWELL ANGLE CONTROL

The dwell angle control circuit calculates the conduction time D for the output transistor in relation to the speed of rotation, to the supply voltage and to the characteristics of the coil.

On the negative edge of the Hall-effect input signal the capacitor C_W begins discharging with a constant current I_{11D}. When the set peak value of the coil current is reached, this capacitor charges with a constant current $I_{11C} = 13.3 \times I_{11D}$, and the coil current is kept constant by desaturathing the driven stage and the external darlington.

The capacitor C_T starts charging on the positive edge of the Hall-effect input signal with a constant current I_{10C}. The dwell angle, and consequently the starting point of the coil current conduction, is decided by the comparison between V_{10} and V_{11}.

A positive hysteresis is added to the dwell comparator to avoid spurious effects and C_T is rapidly discharged on the negative edge of Hall-effects input signal.

In this way the average voltage on C_W increases if the motor speed decreases and viceversa in order to maintain constant the ratio $\frac{t_d}{T}$ at any motor speed.

$\frac{t_d}{T}$ is kept constant (and not $\frac{D}{T}$ = cost) to control the power dissipation and to have sufficient time to avoid low energy sparks during acceleration.

DESATURATION TIMES IN STATIC CONDITIONS

In static conditions, if $C_T = C_W$ as recommended and if the values of the application circuit of fig. 4 are used,

$$\frac{t_d}{T} = \frac{1}{1 + I_{11C}/I_{11D}}$$

DESATURATION TIMES IN LOW AND HIGH FREQUENCY OPERATION

Due to the upper limit of the voltage range of pin 11, if the components of fig. 4 are used, below 10Hz (300 RPM for a 4 cylinder engine) the OFF time reaches its maximum value (about 50ms) and then the circuit gradually loses control of the dwell angle because D = T – 50ms.

Over 200Hz (6000 RPM for a 4 cylinder engine) the available time for the conduction is less than 3.5ms.

If the used coil is 6mH, 6A, the OFF time is reduced to zero and the circuit loses the dwell angle control.

TRANSIENT RESPONSE

The ignition system must deliver constant energy even during the condition of acceleration and deceleration of the motor below 80Hz/s. These conditions can be simulated by means of, a signal gene-rator with a linearly modulated frequency between 1Hz and 200Hz (this corresponds to a change bet-ween 30 and 6000 RPM for a 4 cylinders engine).

CURRENT LIMIT

The current in the coil is monitored by measuring the I_{sense} current flowing in the sensing resistor R_S on the emitter of the external darlington. I_{sense} is given by :

$$I_{sense} = I_{coil} + I_{14}$$

When the voltage drop across Rs reaches the internal comparator threshold value the feedback loop is activated and I_{sense} kept constant (fig. 1) forcing the external darlington in the active region. In this condition :

$$I_{sense} = I_{coil}$$

When a precise peak coil current is required R_S must be trimmed or an auxiliary resistor divider (R_{10}, R_{11}) added :

$$Icpeak\ (A) = \frac{0.320}{RS} \cdot \left(\frac{R10}{R11} + 1\right)$$

SLOW RECOVERY CONTROL (fig. 2)

If I_{sense} has not reached 94% of the nominal value just before the negative edge of the Hall-effect input signal, the capacitor C_{src} and C_W are quickly discharged.

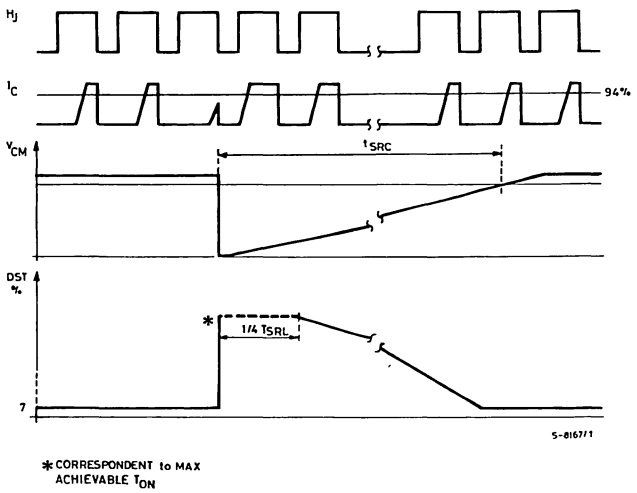
These capacitors remain discharged as long as the pick-up signal is "low". At the next positive transition of the input signal the load current starts immediately, producing the maximum achievable T_{desat} ; then the voltage on C_{SRC} increases linearly until the standby value is reached. During this recovery time the C_{SRC} voltage is converted into a current which, subtrated from the charging current of the dwell capacitor, produces a T_{desat} modulation. This means that the T_{desat} decreases slowly until its value reaches, after a time T_{SRC}, the nominal 7% value.

The time T_{SRC} is given by :

$$T_{rsc} = 12{,}9\ R_7\ C_{SRC} \qquad (ms)$$

where R_7 is the biasing resistor at pin 12 (in KΩ) and C_{src} the capacitor at pin 8 (in μF).

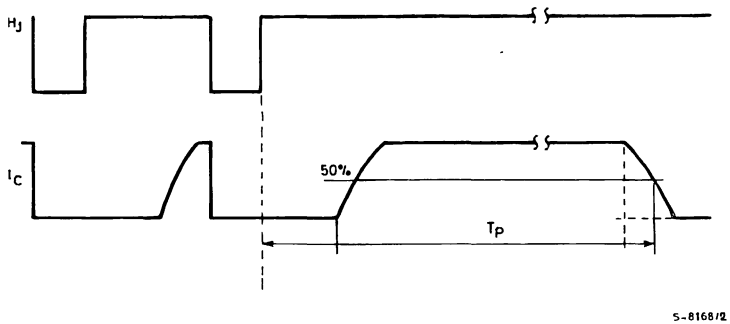
Figure 2 : SRC : I_{coil} Failure and Time Dependence of Active Region.



H_J : Input signal
I_C : Coil current

V_{CM} : Voltage on capacitor C_{SRC}
D_{ST} : Percentage of imposed desaturation time.

Figure 3 : Permanent Conduction Protection.



PERMANENT CONDUCTION PROTECTION (fig. 3)

The permanent conduction protection circuit monitors the input period, charging C_P with a constant current when the sensor signal is high and discharging it when the sensor signal is low. If the input remains high for a time longer than T_P the voltage across C_P reaches an internally fixed value forcing the slow decrease of coil current to zero. A slow decrease is necessary to avoid undesired sparks. When the input signal goes low again C_P is swiftly discharged and the current control loop operates normally.

The delay time T_P is given by :

$$T_P \text{ (sec)} = 18\ C_P\ R_7$$

Where R_7 is the biasing resistor on pin 12 (in KΩ) and Cp the delay capacitor at pin 9 (in μF).

OTHER APPLICATION NOTES

DUMP PROTECTION

Load dump protection must be implemented by an external zener if this function is necessary. In fig. 4 DZ_2 protects the driver stage, the connection between pin 6 and 7 protects the output transistor of pin 6. Moreover DZ_1 protects both the power supply input (pin 3) and Hall-effect sensor.

Resistor R_4 is necessary to limit DZ_1 current during load dump.

OVERVOLTAGE LIMITATION

The external darlington collector voltage is sensed by the voltage divider R_2, R_3. The voltage limitation increases rising R_2 or decreasing R_3.

Due to the active circuit used, an R_o C_o series network is mandatory for stability during the high voltage condition.

R_o C_o values depend on the darlington used in the application.

Moreover the resistor R_{13} is suggested to limit the overvoltage even when supply voltage is disconnected during the high voltage condition.

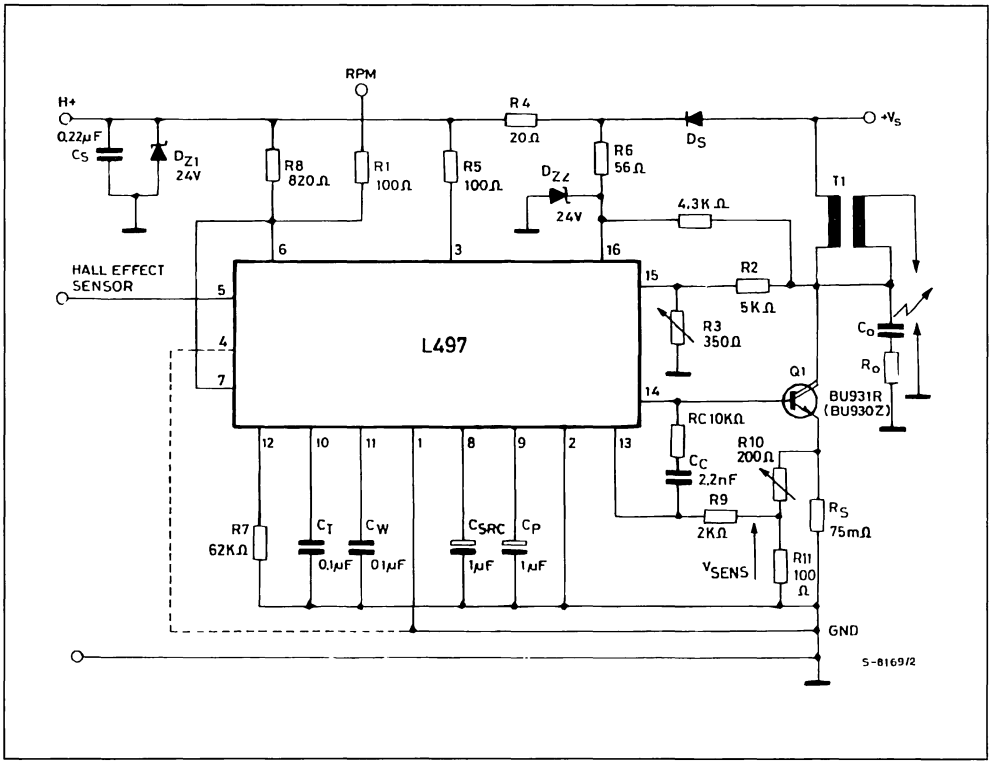
REVERSE BATTERY PROTECTION

Due to the presence of external impedance at pin 6, 3, 16, 15, L497 is protected against reverse battery voltage.

NEGATIVE SPIKE PROTECTION

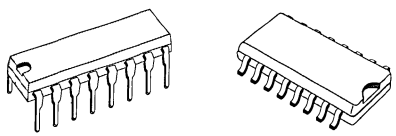
If correct operation is requested also during short negative spikes, the diode D_S and capacitor C_S must be used.

Figure 4 : Application Circuit.



ELECTRONIC IGNITION INTERFACE

- DIRECT DRIVING OF THE EXTERNAL POWER DARLINGTON
- SEPARATE INTERFACE FOR HALL EFFECT OR INDUCTIVE SENSOR
- SEPARATE OPEN COLLECTOR BOOSTER
- COIL CURRENT PEAK VALUE LIMITER
- SIGNAL TO μP WHEN 85% AND FULL NOMINAL COIL CURRENT ARE REACHED
- CONTINUOUS COIL CURRENT PROTECTION
- EXTERNAL DARLINGTON OVERVOLTAGE PROTECTION



DIP 16 **SO-16**

ORDER CODES : L530
L530 D1

DESCRIPTION

The L530 is an integrated circuit designed for use with an NPN darlington in microprocessor controller ignition systems.

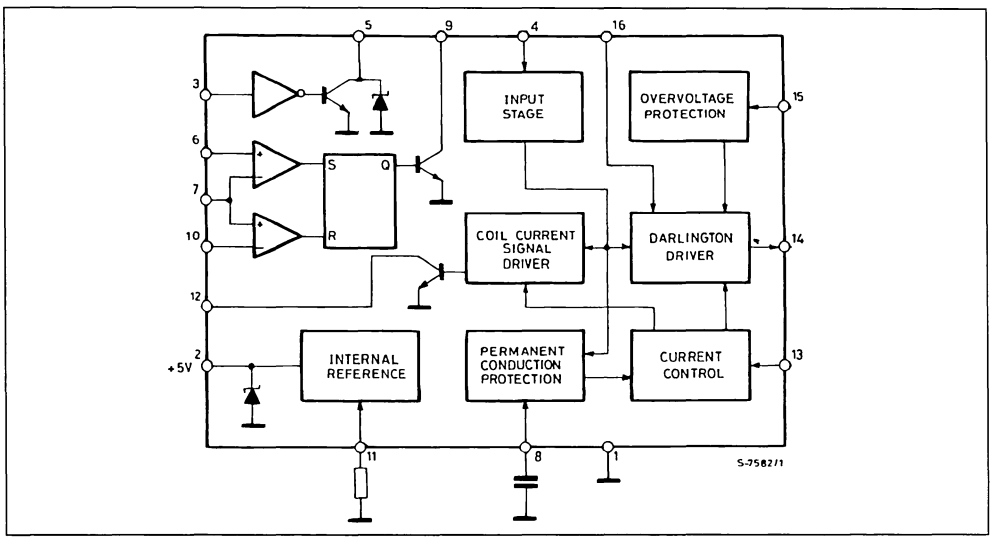
Primarily it acts as an independent controller for the current in the high voltage spark coil.

Charging of the coil is enabled under control of the micro. The device generates a feedback signal for the micro when a fixed percentage and the full nominal current into the coil are reached.

If the enable coil current input signal is active for more than a programmable time, the coil current is switched off slowly to protect the coil and avoid spurious pulses.

The L530 also contains a pulse shaper for the position sensor (both hall effect or magnetic) and an open collector booster which may be used, for example, for the RPM output.

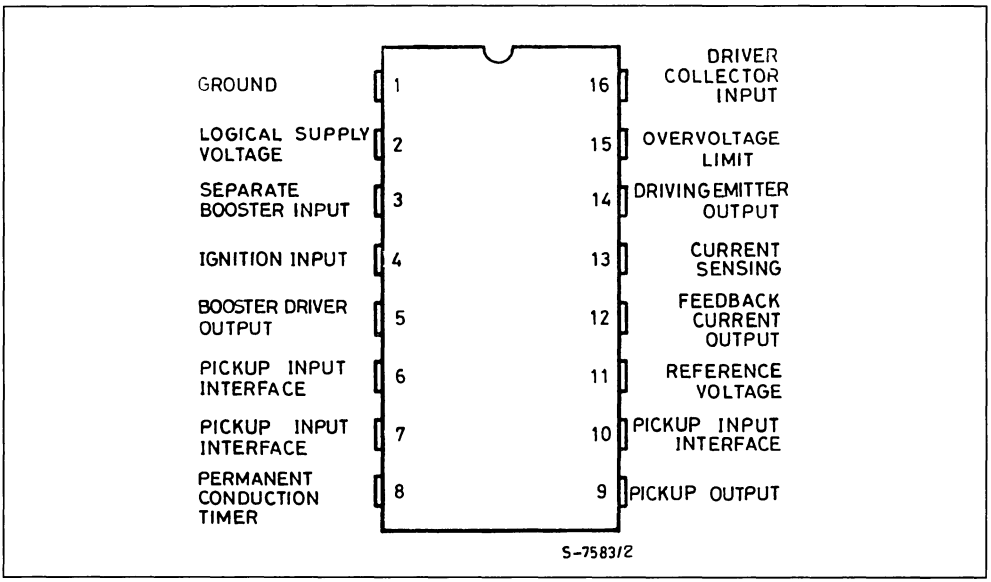
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Max. Supply Voltage (pin 16)	24	V
V_R	Reverse Battery Voltage	– 16	V
P_{tot}	Power Dissipation at T = 90°C	1.2	W
T_j, T_{stg}	Junction and Storage Temperature	– 55 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

$R_{th\ j\text{-}alumina}$ (*)	Thermal Resistance Junction-alumina for SO 16	Max	50	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient for DIP 16	Max	80	°C/W

(*) Thermal resistance junction-pins with the middle of an alumina supporting substrate measuring 15x20mm ; 0.65mm thickness and infinite heathsink.

ELECTRICAL CHARACTERISTICS (V_B = 14.4V, – 40°C ≤ T_J ≤ 125°C unless otherwise specified ; referred to the application circuit of fig. 2)

Symbol	Parameter	Test Conditons	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage (pin 2)		4.5		5.5	V
I_S	Operating Supply Current (pin 2)	V_S = 5V, V_{4H}	8	13	18	mA
V_Z (*)	Internal Zener Voltage (pin 2)	I_S = 80mA	6	7.5	9	V
I_3	Input Current (pin 3)	V_3 = 2V		0	230	µA
V_{REF}	Reference Voltage at pin 11	I_{11} = – 20µA	1.18	1.23	1.35	V
V_{L3}	Input Low Voltage (pin 3)				0.4	V
V_{H3}	Input High Voltage (pin 3)		2.0			V
V_{L4}	Input Low Voltage (pin 4)				0.4	V
V_{H4}	Input High Voltage (pin 4)		2.0			V
V_{SENS}	Current Limit. Sensing Voltage (pin 13)		210	260	310	mV
V_{CEsat}	Series Darlington Driver Sat. Voltage (pin 16-14).	I_O = 50mA I_O = 180mA			0.5 1.0	V V
P_{ON}	Percentage of Coil Current Determining the Feedback ON (pin 12).		75	85	90	%
V_{OVP}	Overvoltage Protect. Zener Voltage (pin 15)	I_{OVP} = 7mA	21	25	30	V
T_{PC}	Permanent Conduction Protection Time (**)		0.25	0.35	0.5	sec.
V_{FL}	Feedback Ouptut Sat. Voltage (pin 12)	$V_{pin\ 4}$ = H $I_{pin\ 12}$ = 5mA			1.0	V
I_{L12}	Leakage Current (pin 12)	V_S = 5V			10	µA
V_{ZRPM}	RPM Output Int. Zener Voltage (pin 5)	I_Z = 20mA	19		29	V
V_{SATRPM}	RPM Output Sat. Voltage (pin 5)	I_{RPM} = 10mA I_{RPM} = 20mA			0.5 1.0	V V
V_{OS}	Comparator Inputs Offset Voltage (pins 6, 7, 10)				± 15	mV
I_{BIAS}	Comparator Inputs Bias Current			– 50	– 300	mA
I_{OS}	Comparator Inputs Offset Current			± 20	± 100	nA
CMR	Common Mode Range		0		V_S – 1.6	V
V_{PF}	Pulse Former Output Low Voltage (pin 9)	$V_{pin\ 6} - V_{pin\ 7}$ > 10mV $V_{pin\ 6} = V_{pin\ 10}$			0.8	V
I_{L9}	Pulse Former Output Leakage Current	$V_{pin\ 7} - V_{pin\ 6}$ > 10mV $V_{pin\ 6} = V_{pin\ 10}$ $V_{pin\ 9}$ = 5V			20	µA
I_4	Output Current (pin 7)		– 650	– 380	– 180	µA
$I_{L\ 5}$	Leakage Current (pin 5)	V_S = 16V			22	µA

(*) This parameter measurement must be considered if the IC is not directly supplied by 5V voltage regulator. In this case a suiited external resistor must be used to limit pin 2 current.

(**) See Fig.4.

PIN FUNCTIONS (refer to fig. 2)

N°	Name	Function
1	GROUND	This pin must be connected to ground.
2	SUPPLY VOLTAGE	5V Supply input.
3	BOOSTER INPUT SIGNAL	Input signal to separate booster stage. This drive circuit may be used, for example, for the RPM output signal of the micro.
4	IGNITION INPUT SIGNAL	When this pin is kept low the external darlington is switched on and the current flows through the coil for all the time the input is low, being active the internal current limitation.
5	BOOSTER DRIVER OUTPUT	Open collector output signal of the separate booster circuit. The phase is the same as the input command at pin 3.
6-7	PICKUP INPUT INTERFACE	Together with pin 10, these inputs realize a separate interface stage for both hall effect or magnetic sensor. Pin 6 is the non-inverting input of the internal comparator which sets, the internal flip-flop. Pin 7 is connected both to the inverting input of the comparator setting the latch and the non-inverting input of the second internal comparator which resets the flip-flop. See fig. 4.
8	PERMANENT CONDUCT. TIMER	A capacitor C_1 connected between this pin and ground sets the delay of the permanent conduction protection in the coil current. The typical delay time value T_{PC} is given by : $T_{PC} = 17\ C_1\ R_{10}$ Where R_{10} is the biasing resistor at pin 11 (in kΩ) and C_1 is the delay capacitor at pin 8 (in µF).
9	PICKUP OUTPUT	Open collector output from the internal flip-flop of the interface circuit for the sensor. This memory is set by the comparator connected to pin 6 and 7 and it is reset by the second comparator connected to pin 7 and 10. The output is a negative logic. See fig. 4.
10	PICKUP INPUT INTERFACE	Inverting input of the second comparator which resets the internal flip-flop of the sensor interface circuit. See pin 6 and 7 Description.
11	REFERENCE VOLTAGE	A resistor R_{10} connected between this pin and ground sets the current used for the internal references and to drive the external capacitor of the permanent conduction protection. The recommended value is 62kΩ.
12	FEEDBACK CURRENT OUTPUT	Open collector output that indicates to micro when the 85% (typ) and the full current flows through the coil. As shown in the fig. 3, this signal goes high when the fixed percentage is reached and goes low when the full programmed coil current is detected.
13	CURRENT SENSING	Connection for coil current limitation. The current is measured on the sense resistor R_{sense} and divided on R_1/R_2. The current limitation value is given by : $I_{SENS} = 0.26 \frac{R_1 + R_2}{R_{sens}\ R_2}$
14	DRIVER EMITTER OUTPUT	Current driver for the external darlington. To ensure stability and precision of T_{desat} C_a and R_3 must be used. Recommended value for R_3 is 2kΩ in order not to change the open loop gain of the system. R_a may be added to C_a to obtain greater flexibility in various application situations. C_a and R_a values ranges are 1 to 100nf and 5 to 30kΩ depending on the external darlington type.

PIN FUNCTIONS (refer to fig. 2) (continued)

N°	Name	Function
15	OVERVOLTAGE LIMIT	The darlington is protected against overvoltage by means of an internal zener available at this pin and connected to pin 14. The external divider R_4/R_5 defines the limitation value given as first approximation by : $V_{ovp} = (\frac{22.5}{R_5} + 7 \cdot 10_{-3}) R_4 + 22.5$
16	DIRVER COLLECTOR INPUT	The collector current of the internal driver which drives the external darlington is supplied through this pin. The maximum current supplied through this pin. Then the external resistor R_6 limits the maximum current supplied to the base of the external darlington.

CIRCUIT OPERATION

As shown in the fig.1, the L530 is particularly suitable for use with a microprocessor as an electronic ignition interface, driving the current through the coil by means of an external darlington.

The device takes the ignition input signal (pin 4) from the microprocessor to drive the darlington, and the output active for all the time in which the input is low.

The ignition input signal (active Low) coming from the microprocessor switches on the device output stage driving the external darlington.

The peak value of the primary current flowing into the coil is limited to a predetermined level by means of a negative feedback circuit including a current sensing resistor, a comparator, the driver stage and the power switch.

An output signal, High when the current flowing into the coil has reached 85% of the final value and Low when the full nominal current has been reached is available at pin 12. This signal is used by the microprocessor to control the dwell time. As shown in the fig. 3 three cases are possible.

In the first case the current limitation is reached ; then, when the input command goes high (spark command) the feedback to microprocessor has already gone low.

In the second case the full current is not reached (very high speed/acceleration or very low battery voltage). Then the output signal goes low together with the spark command.

In the last case a feedback pulse is not present ; this means that the 85% of the programmed current is not reached.

Figure 1 : Typical System Configuration.

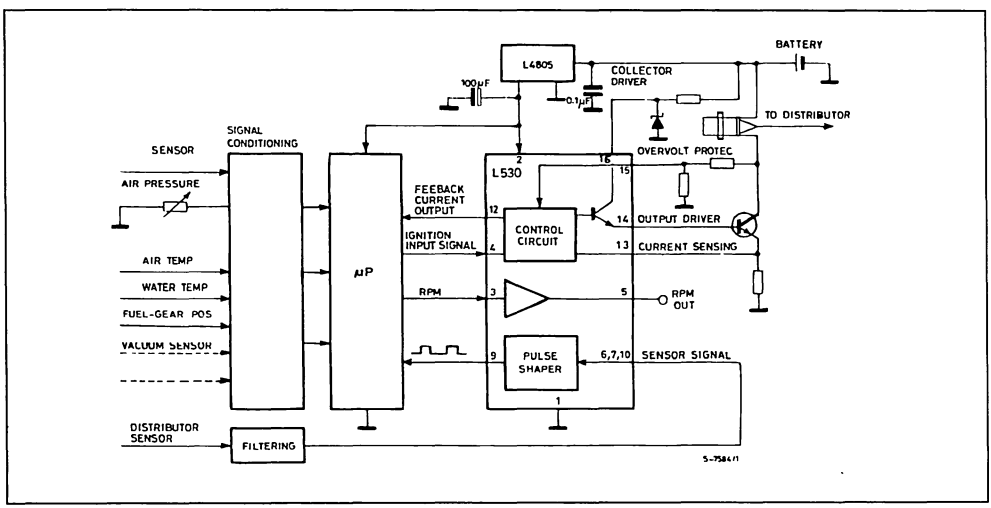


Figure 2 : Application Circuit.

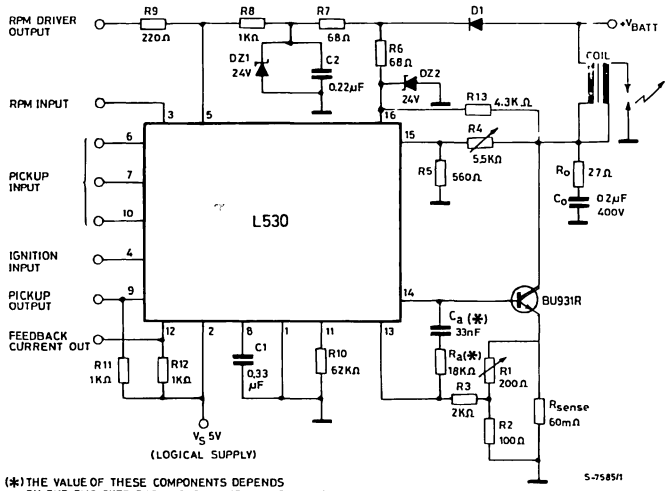
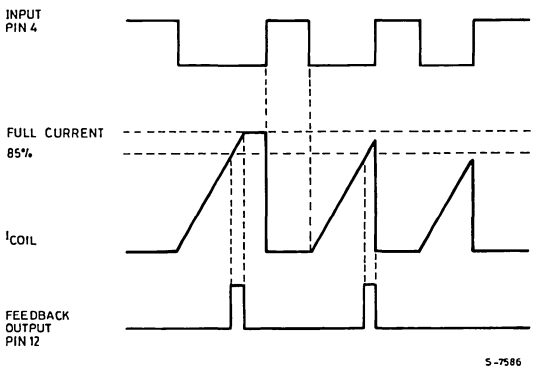


Figure 3 : Typical Operation Waveforms.



CURRENT LIMIT

The current in the coil is monitored by measuring the I_{sense} current flowing in the sensing resistor R_{sense} on the emitter of the external darlington. I_{sense} is given by :

$$I_{sense} = I_{coil} + I_{14}$$

When the voltage drop across R_{sense} reaches the internal comparator threshold value the feedback loop is activated and I_{sense} kept constant (fig. 3) forcing the external darlington in the active region. In this condition :

$$I_{sense} = I_{coil}$$

When a precise peak coil current is required R_{sense} must be trimmed or an auxiliary resistor divider (R_1, R_2)added :

$$I_{cpeak}\,(A) = \frac{V_{sense}}{R_{sense}} \left(\frac{R_1}{R_2} + 1\right)$$

PERMANENT CONDUCTION PROTECTION (fig.4)

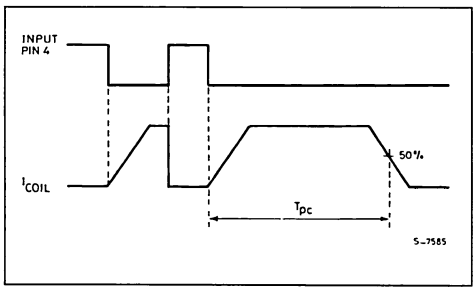
The permanent conduction protection circuit monitors the input period, charging C_1 with a constant current when the sensor signal is Low and discharging it when the sensor signal is High. If the input remains Low for a time longer than T_{PC} the voltage across C_1 reaches an internally fixed value forcing the slow decrease of coil current to zero. A low decrease is necessary to avoid undesired sparks. When the input signal goes High again C_1 is swiftly discharged and the current control loop operates normally.

The typical delay time value T_{PC} is given by :

$$T_{PC}\ (ms) = 17\ C_1\ R_{10}$$

Where R_{10} is the biasing resistor on pin 11 (in K ohm) and C_1 the delay capacitor at pin 8 (in uF).

Figure4 : Permanent Conduction Protection Tim ing.



OTHER APPLICATION NOTES

DUMP PROTECTION

Load dump protection must be implemented by an external zener if this function is necessary. In fig. 2 DZ_2 protects the driver stage.

OVERVOLTAGE LIMITATION

The external darlington collector voltage is sensed by the voltage divider R_4, R_5. The voltage limitation increases rising R_4 or decreasing R_5.

Due to the active circuit used, an Ro Co series network is mandatory for stability during the high voltage condition.

Ro Co values depend on the darlington used in the application.

Moreover the resistor R_{13} is suggested to limit the overvoltage even when supply voltage is disconnected during the high voltage condition.

REVERSE BATTERY PROTECTION

Due to the presence of external impedance at pin 5, 16, 15 L530 is protected against reverse battery voltage.

NEGATIVE SPIKE PROTECTION

If correct operation is requested also during short negative spikes, the diode D_1 and capacitor C_2 must be used.

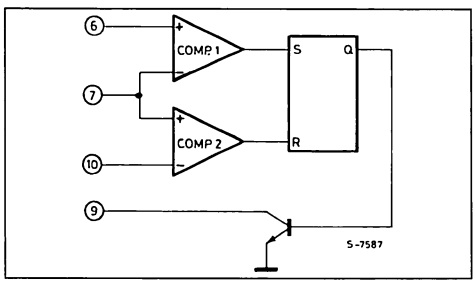
SENSOR INTERFACE

The device contains a separate pulse shaper for the sensor. As shown in fig. 5, this circuit is made by two comparators and flip-flop.

The internal flip-flop is set by the first comparator and reset by the second one. In this way it is possible to interface both the Hall effect and the magnetic pick-up sensor. Fig. 6 shows a typical solution that implements an input comparator with hysteresis able to detect the zero crossing during the input's negative edge (fig. 7). A small positive theshold guarantees the correct switch-on at low RPM.

Three pins allow the use of this interface in a wide range of configurations and, thanks to internal memory, it is possible to obtain a behaviour with hysteresis in order to have a good noise immunity.

Figure 5 : Interface for Hall Effect or Inductive Sen sor.



BOOSTER OUTPUT

An independent booster output is also included in the L530 to permit a separate driving stage from the microprocessor (typically employed for RPM output signal).

The open collector output is protected with an internal zener diode that allows the connection a unstabilized voltage by means of a limiting resistor.

Figure 6 : Input Comparator with Hysteresis.

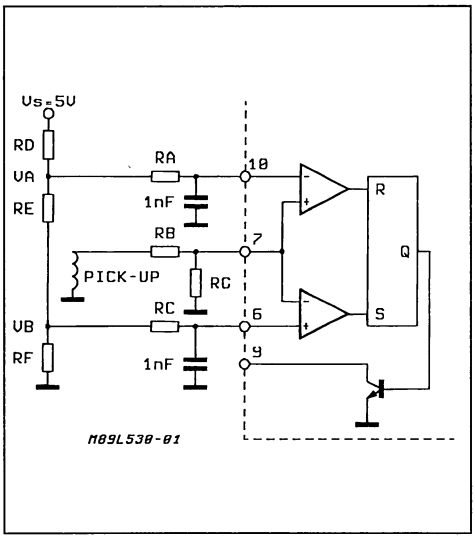
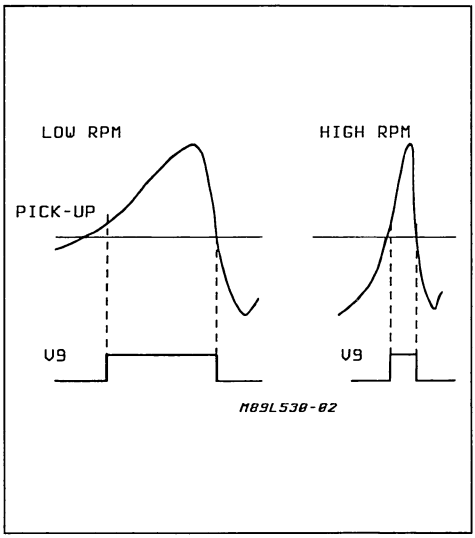
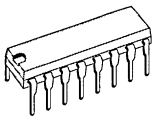


Figure 7 : Zero Crossing Detection.



MULTIFUNCTION INJECTION INTERFACE

- DRIVES ONE OR TWO EXTERNAL DARLINGTONS
- DUAL AND SINGLE LEVEL CURRENT CONTROL
- SWITCHMODE CURRENT REGULATION
- ADJUSTABLE HIGH LEVEL CURRENT DURATION
- WIDE SUPPLY RANGE (4.75 - 46V)
- TTL-COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION
- DUMP PROTECTION



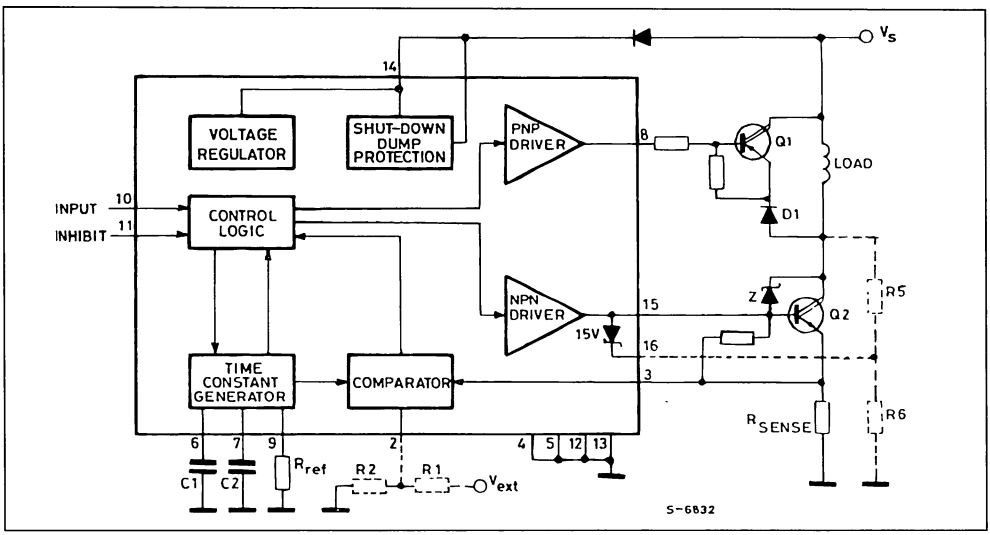
DIP16 (12+2+2)

ORDERING NUMBER: L584

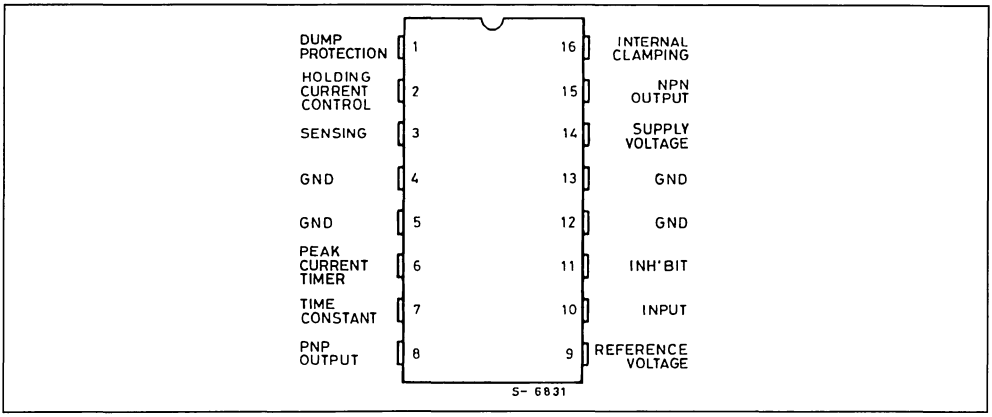
DESCRIPTION

The L584 is designed to drive injector solenoids in electronic fuel injection systems and generally inductive loads for automotive applications. The device is controlled by two logic inputs and features switchmode regulation of the load current driving an external darlington and an auxiliary one for the current recirculation. A key feature of the L584 is flexibility. It can be used with a variety of darlingtons to match the requirements of the load and it allows both simple and two level current control. Moreover, the drive waveshape can be adjusted by external components. Other features of the device include dump protection, thermal shutdown, a supply vol-tage range of 4.75 - 46V and TTL-compatible inputs. The L584 is supplied in a 16 lead Powerdip package which uses the four center pins to conduct heat to the PC board copper.

BLOCK DIAGRAM



PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value
V_s	DC Supply Voltage (pin 1 open) Positive Transient Voltage (pin 1 connected to V_S, τ_f fall time constant = 100ms) (5ms ≤ t_{rise} ≤ 10ms, R_{source} ≥ 0.5Ω)	– 0.2V min ; + 50V MAX + 60V MAX
V_1	Input Voltage (pins 10, 11)	– 0.2V min ; + 7V MAX
V_r	External Reference Voltage (pin 2)	– 0.2V min ; + 7V MAX
V_{sens}	Sense Voltage (pin 3)	– 0.2V min ; + 7V MAX
V_8	Max D. C. and Transient Voltage	50V
I_r	Reference Current (pin 9)	5mA MAX
T_{stg}, T_j	Storage and Junction Temperature Range	– 55 to 150°C

THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W*

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

N°	Name	Functions
1	Dump Protection	With pin 1 connected to pin 14 the device is protected against dump voltage ≤ 60V. The protection operates at $V_s \geq 32V$ (typ.). If this protection is not used the pin must be left open.
2	Holding Current Control	The voltage V_{set} applied to this pin sets the holding current level.
3	Sensing	Connection for load current sense resistor. Value sets the peak and holding current levels. $I_p = 0.45/R_s$ (typ.) ; $I_h = V_{set}/R_s$. (see block diagram and fig. 4).
4	Ground	Ground Connection. With pins 5, 12 and 13 conducts heat to pc board copper.
5	Ground	See pin 4.
6	Peak Current Timer	A capacitor connected between this pin and ground sets the duration of the high level current (t_2 in fig. 4). If left open, the switchmode control of the peak is suppressed. If grounded, the current does not fall to the holding level.
7	Discharge Time Constant	A capacitor connected between this pin and ground sets the duration of t_{off} (fig. 4). If grounded, the current switchmode control is suppressed.
8	PNP Driving Output	Current sink for external PNP darlington (for recirculation). $I_{dp} = 35\ I_r$ (typ.).
9	Reference Voltage	A resistor connected between this pin and ground sets the internal current reference, I_r. The recommended value is 1.2kΩ, giving I_r = 1mA (typ.).
10	Input	TTL-compatible Input. A high level on this pin activates the output, driving the load.
11	Inhibit	TTL-compatible Inhibit Input. A high level on this input disables the output stages and logic circuitry, irrespective of the state of pin 10.
12 & 13	Ground	See Pin 4
14	Supply Voltage	Supply Voltage Input
15	NPN Driving Output	Current Source for External NPN Darlington (load driver). $I_{dn} = 100\ I_r$ (typ.)
16	Internal Clamping	Internal Clamp Zener for Fast Turnoff

ELECTRICAL CHARACTERISTICS (V_s (pin 14) = 14.4 V ; – 40 ≤ T_j ≤ 105 °C ; R_{ref} = 1.20 kΩ unless otherwise noted ; refer to fig. 1)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_s	Operating Supply Voltage	Pin 1 Open	4.75		44	V
V_d	Dump Protection Threshold	Pin 1 = V_s	28		36	V
R_d	Dump Protection Input Resistance	Pin 1 to GND	18		50	kΩ
I_q	Quiescent Current	Pin 14			45	mA
V_I	Input Threshold Voltages	Pin 10 & 11 Low High	 2.0		0.8	V V
I_I	Input Current	Pin 10 & 11 Low High	– 100		 – 250	µA µA
V_r	Reference Voltage	Pin 9	1.15		1.35	V
R_r	Reference Resistor Range	Pin 9 to GND $I_r = V_r/R_r$	1		3.3	kΩ
I_6	Peak Duration Control Current	Pin 6 $V_{pin\ 6} \leq 1.8V$	I_r / 9.50		I_r / 6.00	A
V_{6th}	Peak Duration Control Comparator Threshold	Pin 6	1.20		1.60	V
V_{6SAT}	Pin 6 Saturation Voltage	Pin 6 (discharge state)			200	mV
I_7	Off Duration Control Current	Pin 7 $V_{pin\ 7} \leq 1.8V$	$(I_{r\ min})$/ 9.50		$(I_{r\ MAX})$/6.00	A
V_{7th}	Off Duration Control Comparator Threshold	Pin 7	1.20		1.60	V
V_{7SAT}	Pin 7 Saturation Voltage	Pin 7 (discharge state)			200	mV
V_{spt}	Peak Current Threshold Voltage	Pin 3	400		500	mV
V_{set}	Holding Current Set Voltage Range	Pin 2	0		2	V
V_{set}	Holding Current Threshold Voltage	Pin 3, Peak Value, $dV/dt \leq 1V/s$	V_{set} – 0.01		V_{set} + 0.01	V
I_3	Pin 3 Bias Current	$V_{pin\ 3}$ = 600mV	– 200			µA
V_{cl}	Recirculation Zener Clamping Voltage	Pin 16 to Pin 15 @ 200µA into Pin 16	13.5		18.5	V
I_{dn}	NPN Driver Source Current	$V_{pin\ 15}$ = 0V	70 x I_r		140 x I_r	A
I_{dp}	PNP Driver Sink Current	$V_{pin\ 8} \geq 4.75V$	25 x I_r		60 x I_r	A

APPLICATION INFORMATION

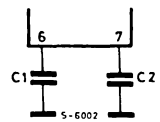
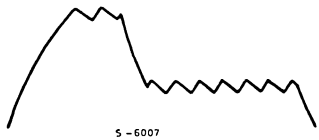
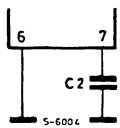
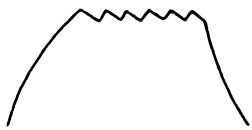
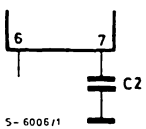
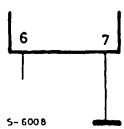
Controlled by a logic input and an inhibit input (both TTL compatible), the device drives the external darlington(s) to produce a load current waveform as shown in figure 4. This basic waveform shows that the device produces an initial high level current in order to ensure a fast opening, followed by a holding level current as long as the input is active. Both the peak and holding current are regulated by the L584's switchmode circuitry.

The duration of the high level current and the values of the peak and the holding currents can be adjusted by external components.

Moreover, by omitting C1, C2 or both it is possible to realize single-level current control, a transitory peak followed by a regulated holding current or a simple peak (figure 1).

The peak and holding current values are always

Figure 1 : Components Connected to Pins 6 and 7 Determine the Load Current Waveshape.

COMPONENTS ON PINS 6 AND 7	LOAD CURRENT WAVEFORM
	
	
	
	

referred, in the following formula, to I_E, emitter current of the external darlington Q2,

$$I_E = I_{LOAD} + I_{dn}$$

because the sensing detection is on the darlington emitter (not directly on the load).

The peak current level I_p, is set by the sensing resistor, R_s, and is found from :

$$I_p = 0.45 / R_s \text{ (typ)}$$

The peak value of holding current level, I_h, is set by a voltage (V_{set}) applied to pin 2, giving :

$$I_{hp} = V_{setth} / R_s = (V_{set} \pm 10mV)/R_s$$

The peak to hold current ratio is fixed by V_{set} :

$$I_p / I_{hp} = 0.45 / V_{setth}$$

V_{set} is fixed by an external reference and a voltage divider (V_{ext}, R1, R2 in fig 2) :
$V_{set} = V_{ext} * R2 / (R1 + R2)$

Due to the particular darlington storage time and the device reaction time not very significant differences can be found between I_p and I_h values based on the previous formula and the real values seen in the applications.

If the holding current function is not used, pin 2 cannot be left floating and it must be connected to GND.

Figure 2 : Application Circuit Showing the Optional Components. In particular it illustrates how the holding current level is adjusted independently of the peak current (with R1, R2, V_{ext}) and how the internal zener clamp is connected. This circuit produces the waveforms shown in Fig. 4.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
12	BDV64	BDV65

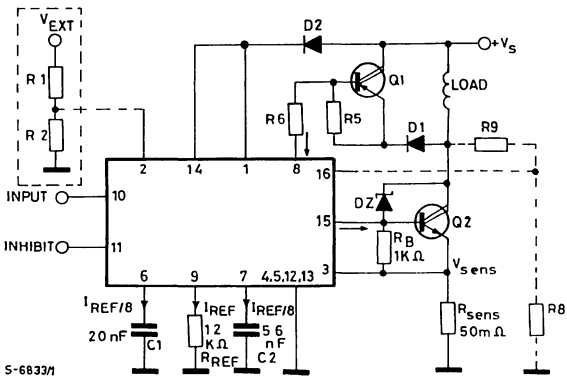
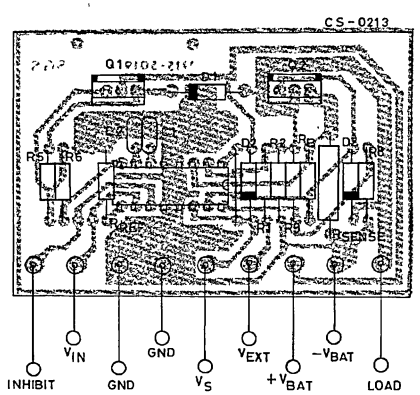


Figure 3 : P.C. Board and Components Layout of the Circuit of Fig. 2 (1 : 1 scale).



The drive current for the two darlingtons and the waveform time constants are all defined in turn by a resistor between pin 9 and ground.

The recommended value for I_r is 1mA which is obtained with a 1.2KΩ resistor. The darlington drive currents are given by :

PNP : $I_{dp} = 35\ I_r$ typ. NPN : $I_{dn} = 100\ I_r$ typ.

The duration of the high current level (t_2 in fig 4) is set by a capacitor connected between pin 6 and ground. This capacitor, C1 is related to the duration, t_2, by :

$$t_2 = C_1 \frac{V_{6th} - V_{6sat}}{I_6} = 12 \frac{C_1}{I_{ref}} \text{ (typ.)}$$

The discharge time constant (t_{off} in fig 4) is set by a capacitor C_2 between pin 7 and ground and is found from :

$$t_{off} = C2 \cdot \frac{V_{7th} - V_{7sat}}{I_7} = 12 \frac{C_r}{I_{ref}} \text{ (typ)}$$

Figure 4 : Waveforms of the Typical Application Circuit of Fig. 2.

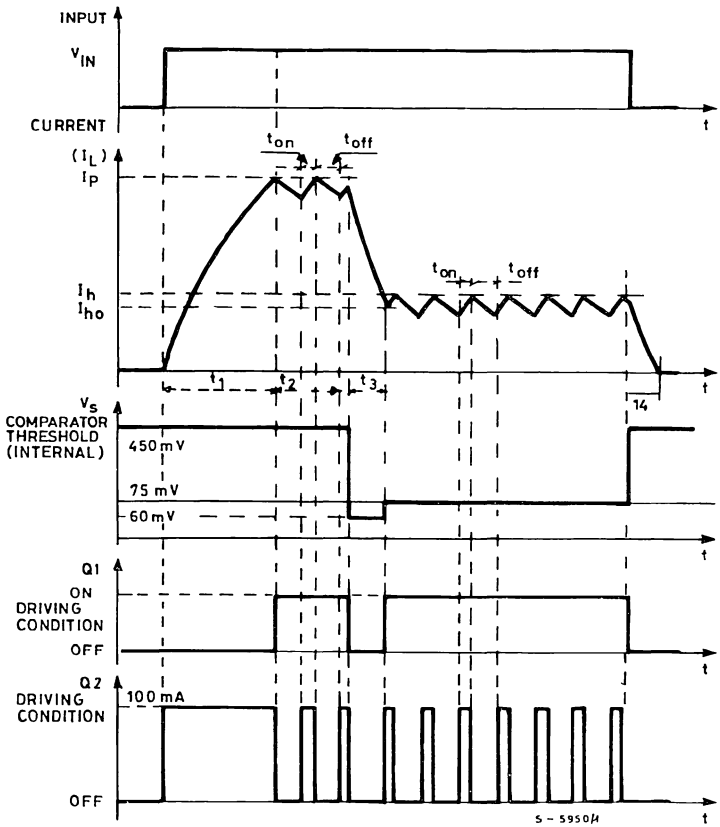
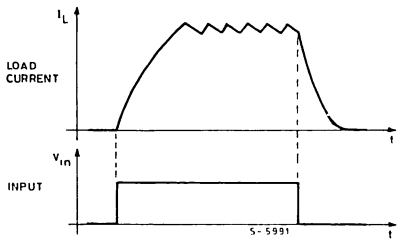


Figure 5 : When pin 6 is grounded, as shown here, the injector current is regulated at a single level.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65



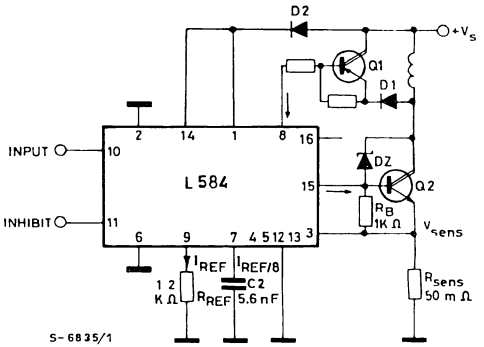
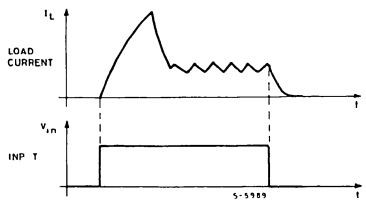


Figure 6 : In this application circuit, pin 6 is left open to give a single peak followed by a regulated holding current.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDX54	BDX53
16	BDW94	BDV65



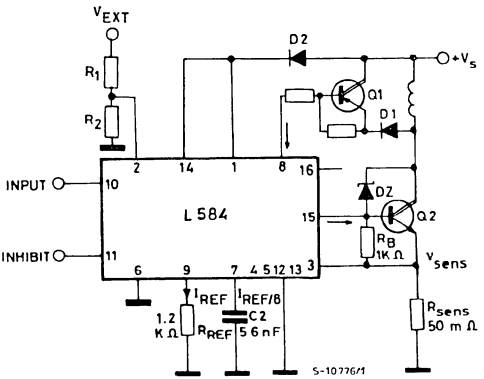
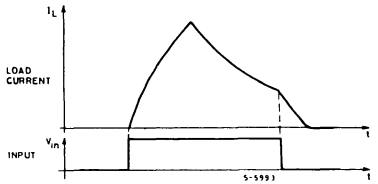


Figure 7 : Switchmode control of the current can be suppressed entirely by leaving pin 6 open and grounding pin 7. the peak current is still controlled.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65



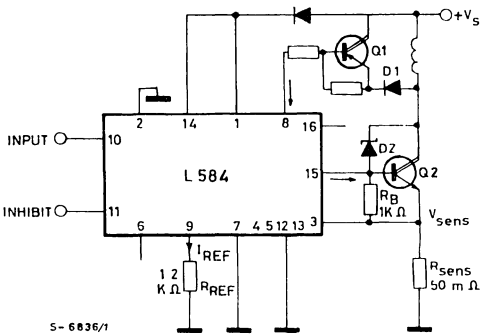
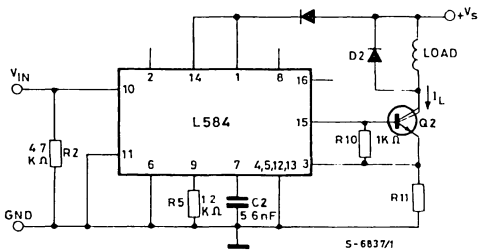
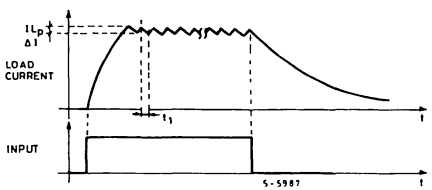


Figure 8 : Applications circuit using only one darlington with a single level of the injector current.





To have a very short off time when the L584 input goes LOW, an internal zener is available on pin 16. This zener is used with an external divider, R8, R9, as shown in figure 2. Suitable values can be found from :

$$V_{pin\ 16} \cong 15V + V_{BEQ2} + VRsense$$

$$V_{CQ2} \cong V_{pin\ 16} \cdot \frac{R9 + R8}{R8}$$

(V_{CQ2} is the voltage at the collector of Q2. V_{CQ2} max is 47V if the pin 8 is used for slow recirculation as in fig. 2).

To ensure stability, a small capacitor (about 200pF) must be connected between the base and collector of Q2 when pin 16 is used.

A different opportunity for a fast off time is based on the use of the external zener diode Dz. In this case also the maximum Dz voltage value is 47V.

LOAD DUMP PROTECTION

To protect the device against the positive load dump it is necessary to connect pin 1 to V_S. In this case, if V_S is higher than 32V, the device turns off Q_2 and turns on Q_1. The external resistor R_6 must be used (see application circuit) to avoid that pin 8 voltage exceeds 50V during load dump. R_6 must be :

$$R_6 > \frac{V_{DUMP} - V_8}{I_{dp}}$$

where V_{DUMP} is the dump voltage value and V_8 : $4.75V < V_8 < 47V$.

For this R_6 value, the minimum supply voltage V_{Smin} guaranteeing Q1 operation is given by :

$$V_{Smin} = R6 \left(\frac{Ip}{B_{Q1}} \quad (+2) \frac{V_{BEQ1}}{R_5} \right) + V_{8sat}$$

In relation to V_{Smin} it is no more verified $I_{dp} = 35\ I_{ref}$ (typ) even if the system correct operation is completely guaranteed.

The L584 application circuit suggested in these notes allows the use of inductive loads with the lowest possible series resistance (compatible with constructional requirements) and therefore reduces notably the power dissipation.

For example, an electronic injector driven from 14.4V which draws 2.4A has a series resistance of 6Ω and dissipates 34.56W. Using this circuit a injector with a 1Ω series resistance can be used and the power dissipation is :

$$P_d = R_L I_L^2 + V_D I_L (1 - \sigma) + V_{sat} \cdot IL\ \sigma + R_S\ I_L^2\ \sigma$$

where R_L = resistance of injector = 1Ω

V_D = drop across diode, $V_D \cong 1V$

V_{sat} = saturation voltage of Q2, $\cong 1V$

R_S = R11 = 185mΩ

σ = duty cycle = 20%

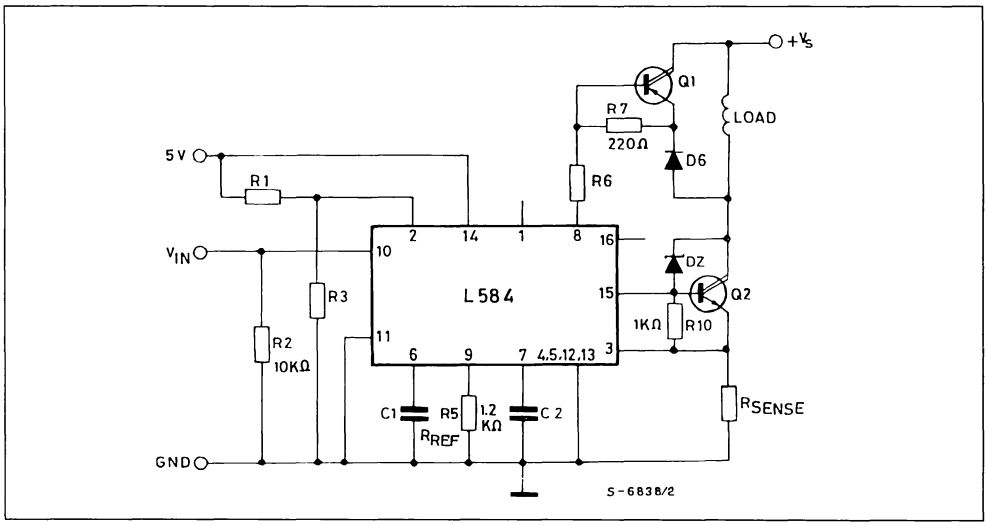
therefore :

$Pd \cong 5.76 + 1.92 + 0.48 + 0.21 = 8.37W$

This given two advantages : the size (and cost) of the injector is reduced and the drive current is reduced from 2.4A to about 0.4A.

The application circuit of figure 9 is very similar to figure 2 except that it shows the use of two supplies : one for the control circuit, one for the power stage.

Figure 9 : Application circuit showing how two separate supplies can be used.



In this application it is assumed that the 5V supply for L584 is taken from a logic supply, which is already protected, against load dump transients and voltage reversal.

Pin 1 must be left open, as shown in fig. 9, if V_S is always lower than 46V even during the voltage transients.

Note that t_{off} is also related to the required current ripple ΔI on the peak or on the holding current level by :

$$t_{off} = -\frac{L}{R} \ln \frac{(I_o - \Delta I)\, R_L + V_{off}}{I_o\, R_L + V_{off}}$$

Where : Io is the initial current value in OFF condition (equal to Ip or IH in accordance to the current level considered),

$$V_{OFF} = V_{DIODE} + V_{CEQ1}$$

R_L is the series resistance value of the inductance L :

Therefore C_2 can be dimensioned directly by :

$$C_2 = \frac{I_{REF}\, L}{12} \cdot \frac{\ln}{R_L} \cdot \frac{(I_o - \Delta I)\, R_L + V_{OFF}}{I_o\, R_L + V_{OFF}}$$

Note that t_{off} is the same for both the peak and holding current.

t_{on} time is given by :

$$t_{on} = \frac{L}{R} \ln \frac{V_{on} - R(I1 - \Delta I)}{V_{on} - RI1}$$

where : I1 is the final current value in ON condition (equal to I_p or I_H in accordance to the current level considered),

$$R = R_L + R_{SENSE}$$

$$V_{on} = V_S - V_{CE}satQ2$$

If the constant times are respectively

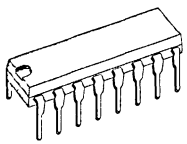
$$\frac{L}{R} > 20\, t_{off} \quad \text{and} \quad \frac{L}{R} > 20\, t_{on}$$

it is possible to consider a purely inductive load and therefore :

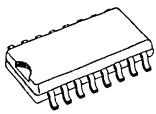
$$t_{off} = L \frac{\Delta I}{V_o} \; ; t_{on} = L \frac{\Delta I}{V_{on}}$$

CAR ALTERNATOR REGULATOR

- ALTERNATOR VOLTAGE CONTROL
- COMPLETE FAULT DIAGNOSTICS
- DRIVES 3 W LAMP DIRECTLY
- LAMP SHORT CIRCUIT PROTECTION
- SENSING INTERRUPT PROTECTION
- 100 V DUMP PROTECTION
- 300 V LOW ENERGY SPIKE PROTECTION
- THERMAL PROTECTION



DIP16



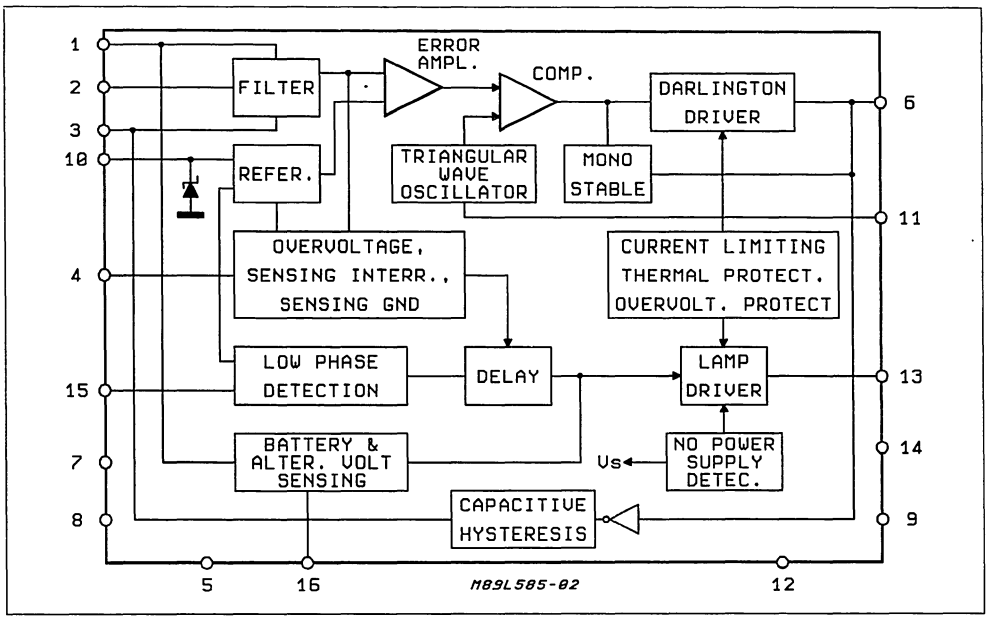
SO16

ORDERING NUMBERS : L585 (DIP16)
L585D1 (SO16)

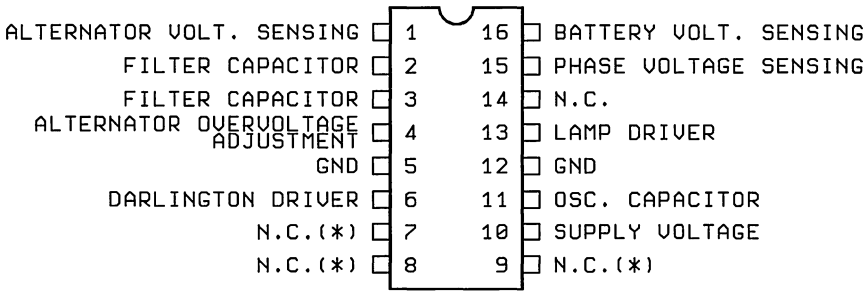
DESCRIPTION

The L585 is an integrated circuit designed for use with an NPN darlington as a voltage regulator in a threephase alternator charging system. It includes fault diagnostic circuitry which drives a 3 W warning lamp in fault conditions such as open or short circuit connections. Protection against load dump transients, short circuits and low energy spikes is incorporated.

BLOCK DIAGRAM



PIN CONNECTION



(*) MUST BE LEFT FLOATING

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage (through R_S)	28	V
V_D	Dump Voltage	100	V
T_j	Junction Temperature Range	– 40 to 150	°C
P_{tot}	Power Dissipation at T_{amb} = 80 °C	1	W
T_{stg}	Storage Temperature	– 65 to 150	°C
T_{op}	Operating Temperature Range	– 40 to 125	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (*) for DIP 16	Max	80	°C/W
$R_{th\ j\text{-}alumina}$(*)	Thermal Resistance Junction-alumina for SO-16	Max	50	°C/W

Note : Soldered on PC board that simulates an application with medium device density on board

(*) Thermal resistance junction-pins with the chip soldered on the middle of an alumina supporting substrate measuring 15 o 20 mm , 0 65 mm thickness and infinite heathsink.

PIN FUNCTIONS

N°	Name	Functions
1	Alternator Voltage Sensing	Connection for voltage regulation sensing. The regulation sensitivity is a function of R1 and is given by : $S = \frac{\Delta VA}{\Delta R1} = 0.5\ mV/\Omega$
2-3	Filter Capacitor	A capacitor connected between these two pins filters the feedback signal from the regulated output. Typically the input impedance is 15 KΩ.
4	Alternator Overvoltage Adjustment	When this pin is left open circuit the overvoltage threshold is a described in the specification. Typically the warning lamp is switched on when the voltage at this pin is greater than 3.5 V. This threshold can be modified with a resistor between either the ground or pin 2.
5	GND	This pin must be connected to ground.
6	Darlington Driver	This pin drives the external darlington disabling it by shorting the current in R_B to ground.
7-8-9	N.C.	These pins must be left floating.
10	IC Supply Voltage	Supply Voltage Input A 7.5 V (typical) Zener is present at the input.
11	Oscillator Capacitor	A capacitor connected to ground sets the frequency of the internal oscillator. The frequency is given by : $f_{osc} = \frac{20 \times 10^{-6}}{8.4 \times C_{osc}}$
12	GND	This pin must be connected to ground.
13	Lamp Driver	Current Driver for External Lamp for Diagnostics. Internally protected agains short circuits (current limiting), load dump transients and, by means of a zener, against low energy spikes.
14	NC	Not connected to die.
15	Phase Voltage Sensing.	Connection for no charge sensing from the alternator . The internal low threshold is typically 2.4 V. By means of the external divider R3/R4 the threshold can be adjusted to give the required sensitivity.
16	Battery Voltage Sensing	Connection for Voltage Battery Sensing This pin senses a failure of the alternator-battery lead as the voltage difference V_A-V_S. The external resistor R2 limits the current in overvoltage protection.

ELECTRICAL CHARACTERISTICS (V_S = 14.4 V ; – 30 °C ≤ T_j ≤ 100 °C unless otherwise specified ; refer to application circuit)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
REGULATION						
V_S	Operating Supply Voltage		6		25	V
I_d	Quiescent Drain Current (pin 10)	V_{10} = 5.5 V			24	mA
V_A	Alternator Reg. Voltage	T_j = 20 °C, t = 100 ms R_1 = 1.3 KΩ (1) T_j = – 30 °C T_j = + 100 °C	14.26 14.60 13.32	14.55	14.84 15.50 14.17	V V V
dV_A	Voltage Reg. Range	10 % < d < 90 %		± 60		mV
S	Sensitivity to R_1 Variation	$S = dV_A/dR_1$	0.35		0.65	mV/Ω
TC_{nS}	Normalized S Temperature Coeff.	1/S* dS/dT		– 2000		ppm/°C
$V_{6\ sat}$	Darlington Driver Satur. Voltage	I_6 = 20 mA			200	mV
f_s	Oscillation Frequency	C_{osc} = 20 nF	80		170	Hz
I_1	Standby Current (pin 1)	V_{batt} = 12 V			2	mA
DIAGNOSTIC						
V_{AH}	Overcharging Voltage Threshold (2)	T_j = 25 °C R_1 = 1.3 KΩ $V_S = V_{AH}$ (3) – 30 °C < T_j < + 100 °C	1.054V_A 1.049V_A		1.086V_A 1.091V_A	V V
V_{PL}	Low Level Phase Voltage Threshold (no load) (4)	f = 600 Hz, T_j = 25 °C – 30 °C < T_j < + 100 °C	5 4.5	6 6	7 7.5	V V
V_{AS}	Difference Between Altern. and Supply Voltage (5)	T_j = 25 °C – 30 °C < T_j < + 100 °C	2.33 2.00	3.10 3.31	3.88 4.18	V V
$V_{1\ 3\ sat}$	Lamp Driver Saturation Voltage	$I_{1\ 3}$ = 250 mA			1.5	V
$V_{1\ 3\ off}$	Lamp Driver Voltage Without Power Supply (6)	R_S > 48 Ω			4.5	V
t_d	Alarm Delay	C_{osc} = 20 nF	70		1.50	s

Notes : 1. d = 50 % the duty cycle of the output signal at pin 6
2. The lamp is switched on with a fixed delay when the alternator voltage becomes higher than V_{AH}. (overcharge indication)
3. Measured 100 ms after turn-on.
4. The lamp is switched on with a fixed delay when the voltage V_p becomes lower than V_{PL} (the alternator is not charging the battery).
5. The lamp is switched on when the cable B is broken (V_A - V_S becomes higher than V_{AS})
6. The lamp is switched on when the cable A is broken (IC without power voltage supply).
7. When the voltage at pin 1 is greater than $V_{1\ dp}$ the internal darlington of the lamp is switched off

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PROTECTION						
T_{sh}	Darlingtyon Thermal Shutdown Threshold		150			°C
V_{Zen}	(pin 10) Zener Voltage	I_O = 60 mA I_O = 130 mA	6 6.2		8 8.2	V V
V_{1dp}	Overvoltage Protection Threshold (7)	T_j = 25 °C – 30 °C < T_j < + 100 °C	25 23	32	38 40	V V
$I_{1\,3\,sc}$	Lamp Driver Circuit Current		300		1500	mA
I_{dump}	Pin 13 Dump Sustaining Capability Current	$V_{1\,3}$ = 110 V@ T_j = 25 °C V_1 = 50 V@ t = 100 ms			200	mA
V_{dump}	Pin 13 Dump Clamping Voltage	$I_{1\,3}$ = 100 mA@ t = < 3 ms	110			V
		$I_{1\,3}$ = 40 mA@ t = < 6 ms, full T T_j = – 30 °C	100 90			V V

Notes : 1. d = 50 % the duty cycle of the output signal at pin 6
2 The lamp is switched on with a fixed delay when the alternator voltage becomes higher than V_{AH} (overcharge indication)
3 Measured 100 ms after turn-on.
4 The lamp is switched on with a fixed delay when the voltage V_p becomes lower than V_{PL} (the alternator is not charging the battery).
5. The lamp is switched on when the cable B is broken (V_A - V_S becomes higher than V_{AS})
6. The lamp is switched on when the cable A is broken (IC without power voltage supply)
7. When the voltage at pin 1 is greater than $V_{1\,dp}$ the internal darlington of the lamp is switched off

CIRCUIT OPERATION

The L585 alternator regulator performs two main functions : regulation control and fault diagnostics.

REGULATION

The alternator voltage is compared with a reference voltage in an error amplifier (see block diagram), the output of which determines the duty cycle of the external darlington. This darlington switches the current in the excitation coil of the alternator.

The switching frequency is fixed and is set by the external capacitor C_{OSC} (see application circuit). Capacitive positive feedback and a monostable eliminates spurious switching caused by contact bounce. The base current delivered to the external darlington it set by the resistor R_B (see application circuit) and must be dimensioned according to the characteristics of this darlington and the maximum coil current.

DIAGNOSTIC

This circuit receives information from the battery, the alternator and one alternator phase. It indicates anomolous conditions by driving a 3 W lamp. To prevent spurious fault warnings some indications are not displayed immediately but are delayed by a fixed time. No external components are needed to implement this delay since it is produced internally by dividing the internal oscillator with an eight-stage divider to give a delay of 128 periods. For a one second delay the oscillator frequency must be 128 Hz.

The lamp is driven after a delay when the following conditions occur : no charge, break or short circuit in the alternator sense wire.

The diagnostic lamp is driven immediately when the cable connecting the alternator to the battery is broken (Va-Vbatt above 2.6 typ.) or when the IC is without power supply ($V_{CE\ sat}$ of the lamp driver is 2.4 V typ. in this case).

PROTECTION

SHORT CIRCUIT PROTECTION

The integrated darlington is protected against short circuits of the lamp. The short circuit current is limited at 600 mA and if this condition persistes thermal protection will intervene.

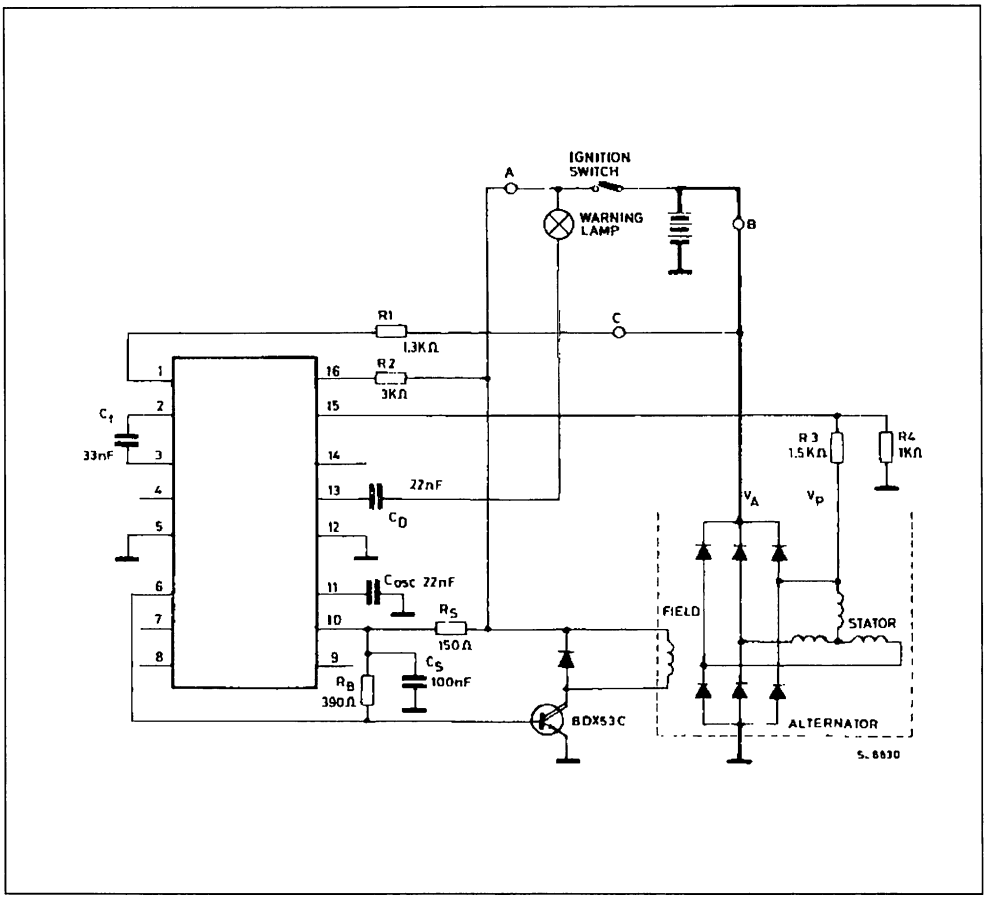
DUMP PROTECTION

The whole IC is protected against load dump transients (100 V, 300 ms with a rise time greater than 5 ms) in the typical application circuit. The only component to which this transient is directly applied (no series resistances) is the lamp driver darlington. During transients the darlington is kept off and can withstand peak voltages of 100 V. Additionally, the IC can withstand low energy spikes up to 300 V. These spikes are clamped by an internal 100 V zener on the collector of the lamp driver darlington.

THERMAL PROTECTION

When the IC temperature reaches 170 °C the lamp driver darlington is kept off.

Figure 1 : Application Circuit.



The device is able to withstand all the voltage transients mentioned in ISO DP7637/1. If voltage transients more severe than the above ISO standard have to be withstood, an external protection device (transil) must be connected between pin 15 and GND. For transients up to 250V, t_{pulse} = 500µs, R_{source} = 47Ω, the transil P6KE100P is recommended.

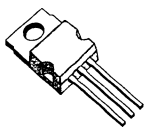
SGS-THOMSON MICROELECTRONICS

L2605
L2685-L2610

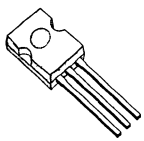
LOW DROPOUT VOLTAGE REGULATORS

- OUTPUT VOLTAGE OF 5, 8.5 AND 10 V
- OUTPUT CURRENT UP TO 500 mA
- NO EXTERNAL COMPONENTS
- LOW DROP-OUT VOLTAGE
- OVERVOLTAGE PROTECTION (± 100 V)
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION
- CURRENT LIMITING
- THERMAL SHUTDOWN

TO-220



SOT-82



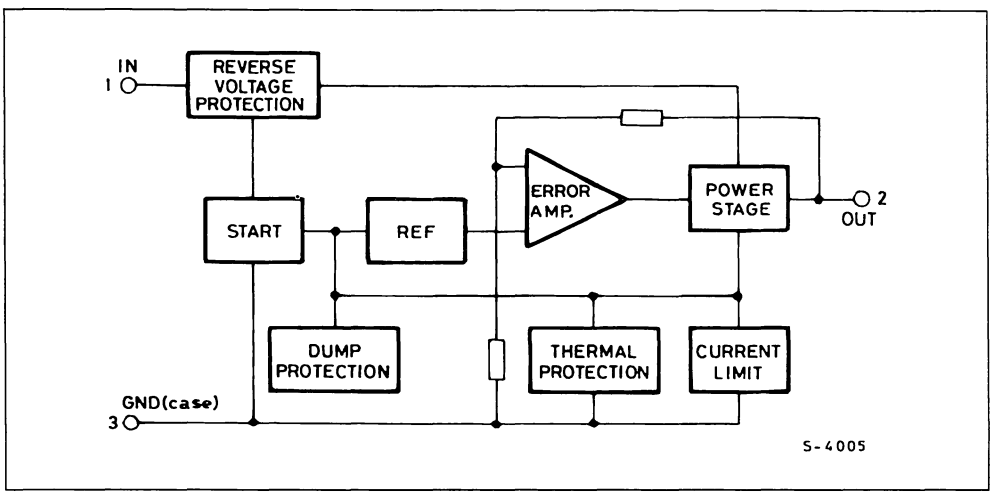
DESCRIPTION

The L2600 series of three terminal positive regulators is specially designed to stabilize power supplies car instrumentation in vehicles with 12V battery.Available with output voltages equal to 5V, 8.5V, 10V, they can supply an output current up to 500mA.

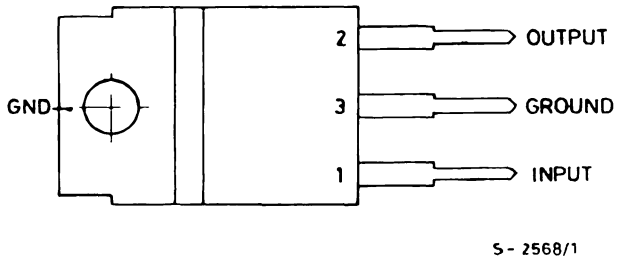
These devices are protected against load dump and field decay transients (± 100V), reverse battery, short circuit and thermal overload.

Order Codes		Output Voltage
TO-220	SOT-82	
L2605V	L2605X	5 V
L2685V	L2685X	8.5 V
L2610V	L2610X	10 V

BLOCK DIAGRAM



PIN CONNECTION (top view)



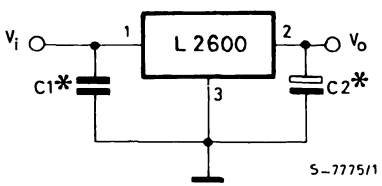
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage	35	V
	DC Input Reverse Voltage	– 28	V
	Transient Input Overvoltage :		
	Load Dump : $5ms \leq t_{rise} \leq 10ms$, τ_f Fall Time Constant = 100ms, $R_{source} \geq 0.5\Omega$	+ 100	V
	Field Decay : $5ms \leq t_{fall} \leq 10ms$ τ_r Rise Time Constant = 33ms, $R_{source} \geq 10\Omega$	– 100	V
P_D	Power Dissipation	Internally Limited	
T_J, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

THERMAL DATA

			SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	8 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100 °C/W	75 °C/W

APPLICATION CIRCUIT



(*) **Note :** C_1 and C_2 are only needed if the load capacitance exceeds 1000 pF, Recommended values are $C_1 = 0\ 1\ \mu F$ and $C_2 \geq 100\ \mu F$.

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, V_i = 14 V, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 500 mA	V_i = 12 to 16 V (L2605) V_i = 12 to 16 V (L2685) V_i = 12 to 16 V (L2610)	4.80 8.15 9.60	5.00 8.50 10.00	5.20 8.85 10.40	V
V_i	Operating Input Voltage	See Note (*)				28	V
$\frac{\Delta V_o}{V_o}$	Line Regulation	I_o = 50 mA	V_i = 12 to 20 V		2	8	mV/V
	Load Regulation	V_i = 14 V	I_o = 50 to 500 mA		4	9	mV/V
ΔV_{i-o}	Dropout Voltage	I_o = 500 mA				1.9	V
I_d	Quiescent Current	I_o = 50 mA			20	45	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 50 mA V_i = 14 V	T_{amb} = – 12 to 80 °C		– 1		mV/°C
I_{sc}	Output Short Circuit Current				1.1	1.8	A
SVR	Supply Voltage Rejection	V_i = 16 V f = 100 Hz	V_i = 2 V I_o = 500 mA		60		dB
R_o	Output Resistance	I_o = 500 mA			0.05		Ω
e_N	Output Noise Voltage	BW = 100 Hz to 10 KHz			20		μV

(*) **Note :** For DC input voltage 28 V < V_i < 35 V the device is not operating.

ELECTRICAL CHARACTERISTICS (– 40 ≤ T_j ≤ 125 °C (note 2), V_i = 14 V, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 500 mA	V_i = 12.5 to 16 V (L2605) V_i = 12.5 to 16 V (L2685) V_i = 12.5 to 16 V (L2610)	4.70 8.00 9.40	5.00 8.50 10.00	5.30 9.00 10.60	V
V_i	Operating Input Voltage	See Note (°)				26	V
$\frac{\Delta V_o}{V_o}$	Line Regulation	I_o = 50 mA	V_i = 12.5 to 20 V		3	12	mV/V
	Load Regulation	V_i = 14 V	I_o = 50 to 500 mA		5	13	mV/V
ΔV_{i-o}	Dropout Voltage	I_o = 500 mA				2.5	V
I_d	Quiescent Current	I_o = 50 mA			29	65	mA
I_{sc}	Output Short Circuit Current				1.1	2.1	A

Notes : (°). For a DCinput voltage 26 V < V_i < 35 V the device is not operating.

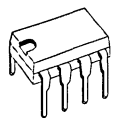
2. The limits are guaranteed by design, correlation and statistical control on production samples over the indicated temperature and supply voltage ranges.

SGS-THOMSON MICROELECTRONICS

L4620

LIQUID LEVEL ALARM

- DRIVES DIRECTLY 300 mA ALARM LOAD
- PROGRAMMABLE INPUT POLARITY TO ACTIVATE THE OUTPUT STAGE
- PROGRAMMABLE DELAY TIME
- PROGRAMMABLE OUTPUT DUTY CYCLE
- OUTPUT SHORT CIRCUIT PROTECTION
- OVERVOLTAGE AND THERMAL PROTECTION



Minidip

ORDERING NUMBER : L4620

DESCRIPTION

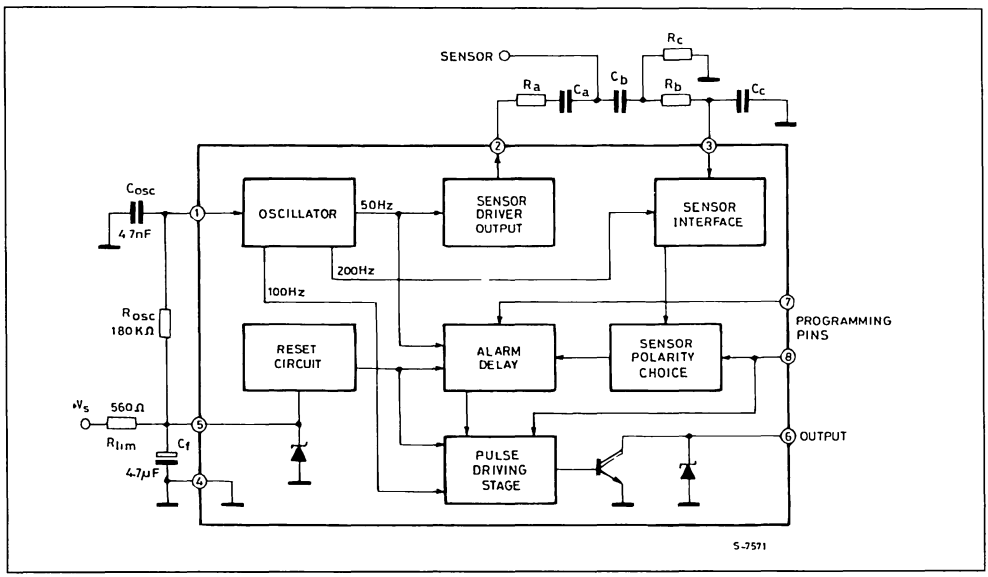
The L4620 is an integrated circuit, designed for the liquid level control in automotive applications. The liquid level is indicated by an attenuation between transmitted and received signal across a sensor tip in the liquid. If the attenuation exceedes an internal threshold - sensor tip outside the liquid or liquid temperature higher than a determined value - a squarewave alarm output indicates an unsufficient liquid condition. If the liquid level is restored before the end of a delay time the alarm is not activated.

Through two pins it is possible to program : the delay time to activate the alarm, the duty cycle of the output squarewave, the polarity of the input threshold of the sensor for alarm activation.

The above features make the L4620 particularly versatile for many applications and give the possibility to use various sensor types.

Internal circuits prevent spurious indications from the liquid sensor and a latch keeps the alarm activated until the supply voltage is switched off. The device includes thermal shutdown protections.

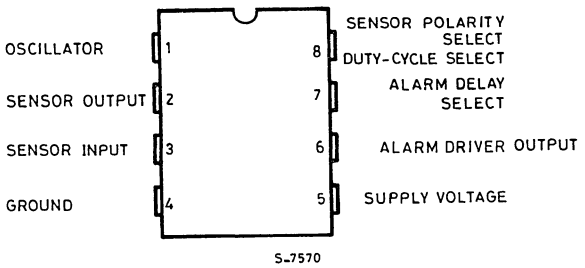
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_S	Supply Current ($V_S > V_Z$)	200	mA
V_3	Sensor Input Voltage (V_2 High)	7	V
I_{out}	Output Current	500	mA
P_{tot}	Power Dissipation at T_{amb} = 70°C	0.8	W
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

PIN FUNCTION (Block Diagram)

N°	Name	Function
1	Oscillator	A capacitor C_{osc} connected to ground and a resistor R_{osc} connected to pin 5 (supply voltage) set the frequency of the internal oscillator. The period is given by : $T_{osc} = 0.693 (R_{osc} + 5000) C_{osc}$
2	Sensor Output	A squarewave is available at this pin to drive the external sensor. The output frequency is 1/32 of the internal oscillator fosc, i.e. 50Hz using the values of $R_{osc} = 180k\Omega$ and $C_{osc} = 4.7nF$ for the external components.
3	Sensor Input	Connection for liquid level sensing. During the zero level of the squarewave signal at pin 2, the internal sensing circuit is disabled. During the high level of the wave shape the input is compared with a threshold which depends on the output sensor voltage at pin 2. When the voltage at this pin is low, the threshold value is given by : $V_{SENSH} = 0.4V_2$ (typ). If the input voltage becomes higher than the above V_{SENSH}, the V_{sens} value is reduced to $V_{SENSL} = 0.22V_2$ (typ), providing an hysteresis available with both the programmable polarities.
4	GND	This pin must be connected to ground.
5	Supply Voltage	Supply voltage input. A 4.5V (typical) zener is present at the input. The external resistor limits the current through the zener for high supply voltages. Moreover when the voltage at this pin is down 2.5V (typical) the internal reset circuit is activated to inizialize the counters and to reset the memory alarm latch.
6	Alarm Driver Output	An internal open collector stage is available at this pin to drive the external alarm indicator by a rectangular waveshape. The output period depends on the external component R_{osc} and C_{osc}. Using the recommended values of block diagram the period T is 320ms (typ). The duty cycle depends on the status of the programming pin 8 (see pin 8 function) and can be or 1 : 2 or 1 : 64 i. e., refer to fig. 2, t = 160ms or t = 5ms.
7	Alarm Delay Select	This program pin selects the alarm delay to activate the output stage after a low liquid level indication of the sensor. The delay depends on the internal oscillator frequency. Refer to application circuit, if this pin is kept low the typical delay is 10.24s. When this pin is kept high, the typ delay becomes 20.48s.
8	Sensor Polarity Select Output Duty-cycle Select	Through this pin it is possible to program both the sensor polarity with respect to the internal threshold and the duty-cycle of the output waveform which drives the alarm. When this pin is kept low the output rectangular wave duty cycle is 1:64 (T = 320ms, t = 5ms in fig. 2) and the output is activated, after the delay time, if the voltage at pin 3 is higher than V_{SENS}. When the voltage at this pin is high the output duty cycle is 50% (t = 160ms) and the output goes on, after the delay time, if the voltage at pin 3 is less than V_{SENS}.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified. Refer to block diagram for external component values)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_Z	Internal Zener Voltage (pin 5)	I_S = 24mA	4	4.5	5	V
I_S	Supply Current (pin 5)	V_s = 3.8V		6.5	11	mA
f_{osc}	Oscillator Frequency (pin 1)	R_{osc} = 180kΩ, C_{osc} = 4.7nF	1.45	1.6	1.75	kHz
V_7, V_8	Programming Pins Input Voltage (pin 7, 8)	Low State			0.3	V
		High state	2			V
I_7, I_8	Programming Pins Input Current (pin 7, 8)	$V_7 = V_8$ = 0V	− 1			µA
		$V_7 = V_8 = V_Z$			150	µA
V_2	Sensor Drive Output Voltage, (*)	V_2 = Low, I_2 = 1mA			0.4	V
		V_2 = High, I_2 = 1mA	V_Z−1		V_Z−0.4	V
I_2	Sensor Driver Output Current		− 1		1	mA
V_{SENSH}/V_2	Sensor Input High Threshold Voltage Versus V_2 (pin 3)	V_2 = High $V_{pin\ 3} < V_{sensL}$	0.33	0.4	0.47	
$\frac{V_{SENSL}}{V_2}$	Sensor Input Low Threshold Voltage Versus V_2 (pin 3)	V_2 = High $V_{pin\ 3} > V_{sensH}$	0.15	0.22	0.29	
$V_{CLAMP3L}$	Sensor Input Clamping Voltage (pin 3)	− 100µA < I_{sens} < 100µA V_2 = Low	− 0.1		0.1	V
$V_{CLAMP3H}$		V_2 = High I_3 = − 100µA	− 0.8	− 0.6	− 0.4	V
		I_3 = + 100µA	V_Z		V_Z + 0.8	V
I_{sens}	Sensor Input Bias Current (pin 3)	V_{sens} = High			1.2	µA
T_d	Delay Time	f_{osc} = 1.6kHz V_7 = Low		10.24		sec
		V_7 = High		20.48		sec
$V_{out(sat)}$	Output Stage Saturation Voltage (pin 6) (**)	I_{out} = 200mA			1.3	V
$V_{out(clamp)}$	Output Stage Overvoltage Protection (pin 6)	I_{out} = 70mA	19	21	23	V

*) This is a squarewave signal. The frequency is given by : $f = \frac{1}{32} f_{osc}$

**) The output squarewave signal frequency is given by $f = \frac{1}{512}$ fosc

The duty cycle depends on the state of the pin 8 and can be or 1 . 2 or 1 · 64, i.e refer to figure 2, T = 320 ms, t = 160 or 5 ms when the oscillator frequency f_{osc} = 1.6 KHz.

CIRCUIT OPERATION

The L4620 liquid level alarm is designed to operate with a variety of sensor types which change impedance depending on whether the sensor is above or below the level of a liquid. If the impedance variation of ther liquid itself is sensed, a very simple sensor (two electrodes) can be used. The output stage drives directly the alarm indicator with a 300mA rectangular wave signal, the duty cycle of which is programmable.

SENSOR INTERFACE.

As shown in the application circuit, the sensor is connected so that it varies the attenuation of a square-wave signal between pin 2 and pin 3 where its positive half cycle is compared with the reference threshold (with hysteresis).

This frequency, generated internally by a 50% duty cycle oscillator, is 50Hz in the typical application (R_{osc} = 180KΩ C_{osc} = 4.7nF).

The threshold of the sensor input is a function of the output voltage at pin 2. The hysteresis is provided by a Schmitt trigger comparator. As shown in figure 1, this gives hysteresis with either threshold polarity selected.

The AC driving of the level sensor allows the use of a capacitive filter (C_A, C_B, C_C in block diagram) which acts as a bandpass filter at the frequency used. The resistor R_C in the application circuit biases the sensor input stage. In this way the interference problems typical of automotive applications are reduced considerably. If, however, it is not necessary to decouple and filter the sensor a simple resistive network may be used, eliminating the capacitors.

SPURIOUS INDICATION PROTECTION.

To prevent spurious alarm signals when the liquid is agitated or in the presence of interference, the device includes two protection mechanism :

Firstly, the sensor interface which samples the positive half cycle of the sensor signal activates its output only if there are four consecutive alarm condition indications. Secondly, the alarm output stage is only activated after an externally programmable delay. During this delay if the alarm condition ceases the alarm output will not be activated.

Using the values C_{osc} = 4.7nF and R_{osc} = 180KΩ, which give a typical oscillator frequency of 1.6KHz, delays of about 10 s (programming pin 7 low) or 20s.

INTERNAL MEMORY.

When the alarm output has been activated an internal latch holds it in the active state until the power supply is removed. This feature ensures that the alarm will not be interrupted if the sensor connection breaks.

OUTPUT STAGE.

Through pin 8 it is possible to program the duty cycle of the alarm signal waveform (see figure 2). When pin 8 is high the output signal has a duty cycle of 50% ; if pin 8 is low the duty cycle is 1 : 64. The period of the output signal is always 320ms using the component values indicated in block diagram.

The output stage can deliver up to 300mA and is protected internally against overvoltages (by a zener).

A thermal shutdown circuit provides additional protection.

SENSOR INPUT WAVEFORM

Figure 1a : Pin 8 Low ; Alarm with Input Voltage > Threshold.

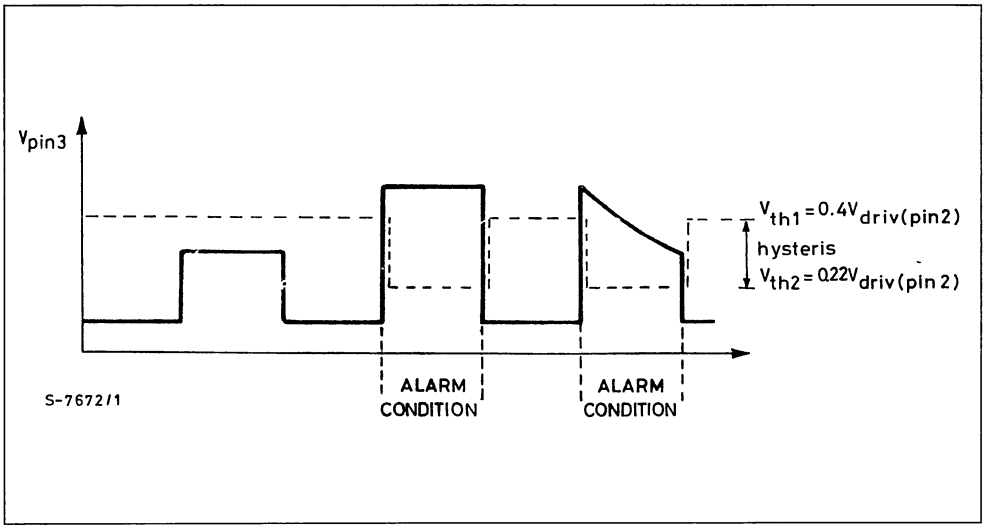


Figure 1b : Pin 8 High ; Alarm with Input Voltage < Threshold.

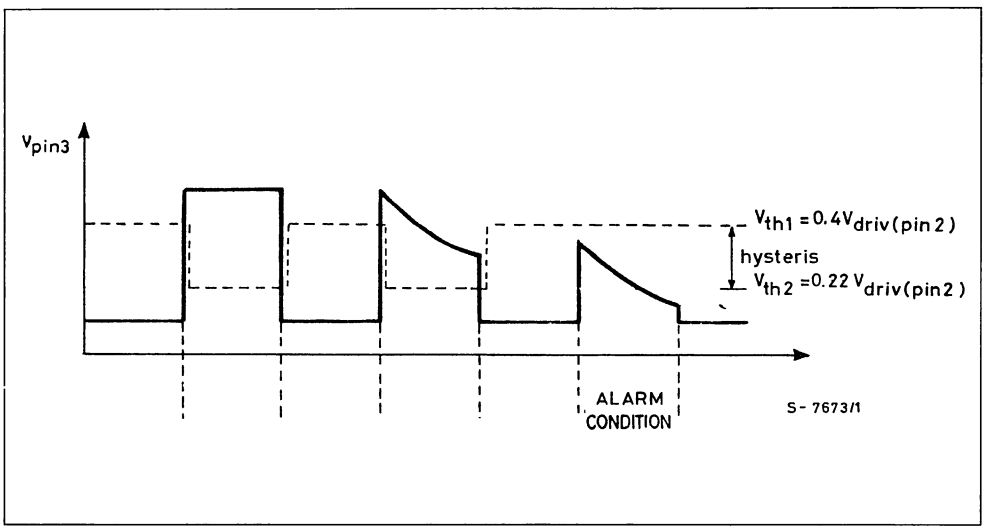


Figure 2a : Output Alarm Waveform with Pin 8 High : $t = \frac{1}{2} T$.

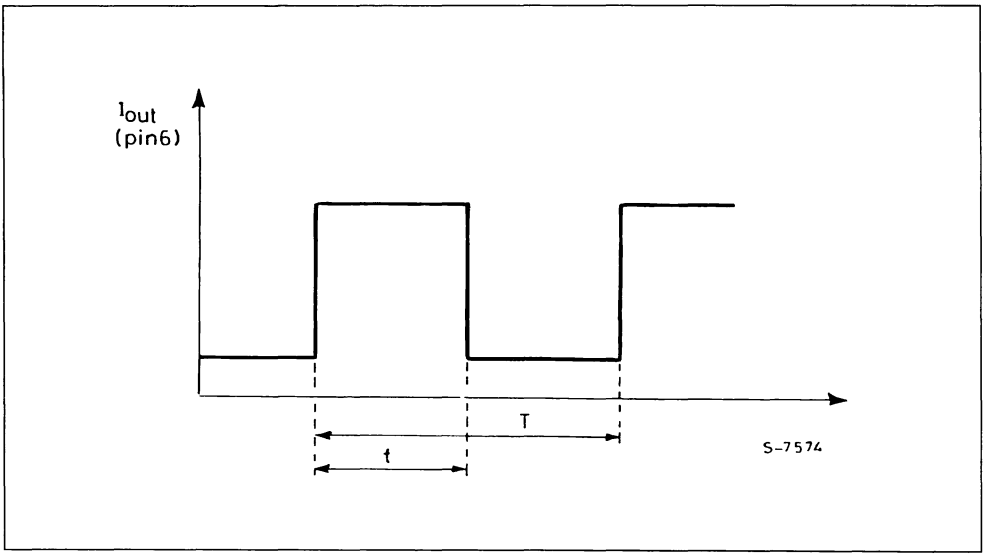
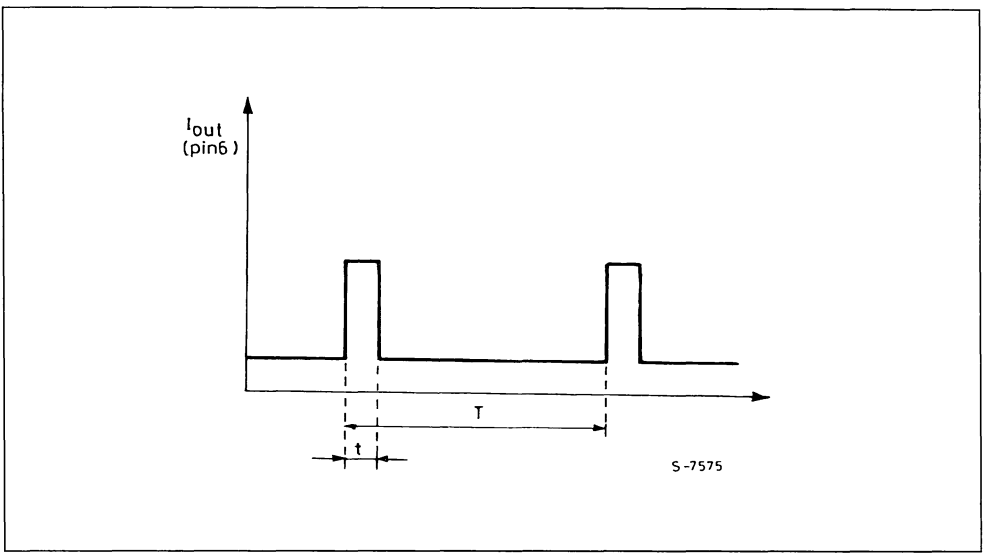


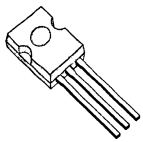
Figure 2b : Output Alarm Waveform with Pin 8 Low : $t = \frac{1}{64} T$.



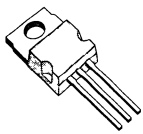
L4805-L4885-L4892
L4808-L4810-L4812

VERY LOW DROP VOLTAGE REGULATORS

- INPUT/OUTPUT DROP TYP. 0.4V
- 400mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- REVERSE POLARITY PROTECTION
- OVERVOLTAGE PROTECTION (± 60V)
- FOLDBACK CURRENT LIMITING
- THERMAL SHUTDOWN



SOT-82



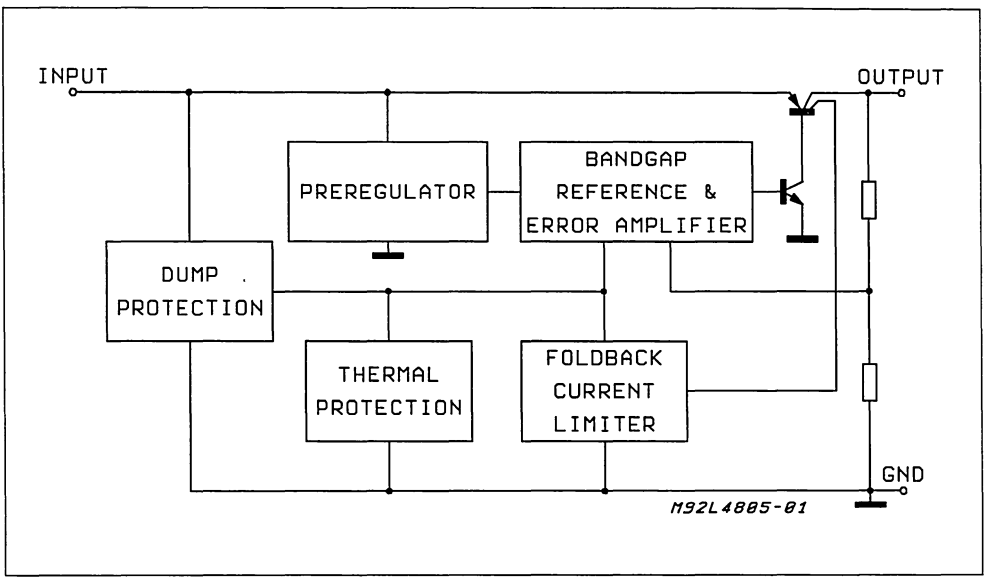
TO-220

DESCRIPTION

L4800 series devices are voltage regulators with a very low voltage drop (typically 0.4V at full rated current), output current up to 400mA, low quiescent current and comprehensive on-chip protection. These devices are protected against load dump and field decay transients of ± 60V, polarity reversal and overheating. A foldback current limiter protects against load short circuits. Available in 5V, 8.5V, 9.2V, 10V and 12V versions (all ± 4%, T_I = 25°C) these regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.

In automotive applications the L4805 is ideal for 5V logic supplies because it can operate even when the battery voltage falls below 6V. In battery backup and standby applications the low consumption of these devices extends battery life.

BLOCK DIAGRAM



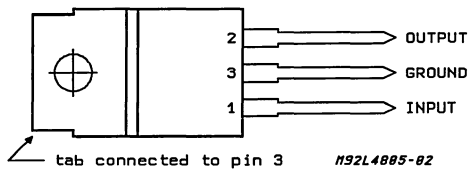
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage	+ 35	V
	DC Input Reverse Voltage	- 18	V
	Transient Input Overvoltages : Load Dump : $5ms \leq T_{rise} \leq 10ms$, τ_f Fall Time Constant = 100ms, $R_{source} \leq 0.5\Omega$ Field Decay : $5ms \leq t_{fall} \leq 10ms$, $R_{source} \leq 10\Omega$ τ_r Rise Time Constant = 33ms	60 - 60	V V
T_j, T_{stg}	Junction and Storage Temperature Range	- 55 to + 150	°C

THERMAL DATA

			SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	8 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100 °C/W	75 °C/W

PIN CONNECTION (top view)



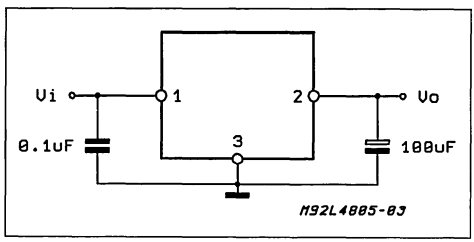
Order Codes		Output Voltage
TO-220	SOT-82	
L4805CV	L4805CX	5V
L4808CV	L4808CX	8V
L4885CV	L4885CX	8.5 V
L4892CV	L4892CX	9.2 V
L4810CV	L4810CX	10 V
L4812CV	L4812CX	12 V

TEST AND APPLICATION CIRCUIT

The output capacitor is required for stability. Though the 100 µF shown is the minimum recommended value, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristics of a particular system.

Capacitors must also be rated at all ambient temperature expected in the system. Many aluminum type electrolytics will freeze at temperatures less than – 30 °C, reducing their effective capacitance to zero. To maintain regulator stability down to – 40 °C, capacitors rated at that temperature (such as tantalums) must be used.



ELECTRICAL CHARACTERISTICS (V_I = 14.4V; C_O = 100µF; T_j = 25°C unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_O	Output Voltage	I_O = 5mA to 400mA (L4805)	4.80	5.00	5.20	V
		I_O = 5mA to 400mA (L4808)	7.68	8.00	8.32	V
		I_O = 5mA to 400mA (L4810)	8.16	8.50	8.84	V
		I_O = 5mA to 400mA (L4812)	8.83	9.20	9.57	V
		I_O = 5mA to 400mA (L4885)	9.60	10.00	10.40	V
		I_O = 300mA (L4892)	11.50	12.00	12.50	V
V_I	Operating Input Voltage				26	V
$\Delta V_O/V_O$	Line Regulation	VI = 13 to 26V; I_O = 5mA		1	10	mV/V
$\Delta V_O/V_O$	Load Regulation	IO = 5 to 400mA*		3	15	mV/V
$V_I - V_O$	Dropout Voltage	I_O = 400mA*		0.4	0.7	V
		I_O = 150mA		0.2	0.4	V
I_q	Quiescent Current	I_O = 0mA		0.8	2	mA
		I_O = 150mA		25	45	mA
		I_O = 400mA*		65	90	mA
$\frac{\Delta V_O}{\Delta T \bullet V_O}$	Temperature Output Voltage Drift			0.1		$\frac{mV}{°C \bullet V}$
SVR	Supply Voltage Rejection	I_O = 350mA; f = 320Hz; C_O = 100µF; $V_I = V_O + 3V + 2V_{pp}$		60		dB
I_O	Max Output Current			800		mA
I_{SC}	Output Short Circuit Current (fold back condition)			350	500	mA

* only for L4892 the current test conditions is I_O = 300mA

ELECTRICAL CHARACTERISTICS (V_I = 14.4V; C_O = 100µF; T_j = -40 to 125°C (note 1) unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_O	Output Voltage	I_O = 5mA to 400mA (L4805)	4.70	5.00	5.30	V
		I_O = 5mA to 400mA (L4808)	7.50	8.00	8.50	V
		I_O = 5mA to 400mA (L4810)	8.00	8.50	9.00	V
		I_O = 5mA to 400mA (L4812)	8.65	9.20	9.75	V
		I_O = 5mA to 400mA (L4885)	9.40	10.00	10.60	V
		I_O = 300mA (L4892)	11.30	12.00	12.70	V
V_I	Operating Input Voltage	see note 2			26	V
$\Delta V_O/V_O$	Line Regulation	VI = 14 to 26V; I_O = 5mA		2	15	mV/V
$\Delta V_O/V_O$	Load Regulation	IO = 5 to 400mA*		5	25	mV/V
$V_I - V_O$	Dropout Voltage	I_O = 400mA*		0.5	0.9	V
		I_O = 150mA		0.25	0.5	V
I_q	Quiescent Current	I_O = 0mA		1.2	3	mA
		I_O = 150mA		40	70	mA
		I_O = 400mA*		80	140	mA
I_O	Max Output Current			870		mA
I_{SC}	Output Short Circuit Current (fold back condition)			230		mA

Notes : 1. This limits are guaranteed by design, correlation and statistical control on production samples over the indicated temperature and supply voltage ranges
2. For a DC voltage 26V < V_I < 35V the device is not operating.

Figure 1: Dropout Voltage vs. Output Current

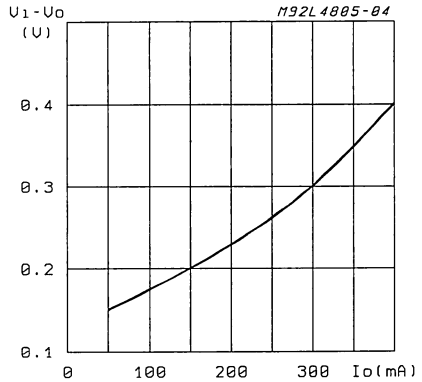


Figure 2: Quiescent Current vs. Output Current

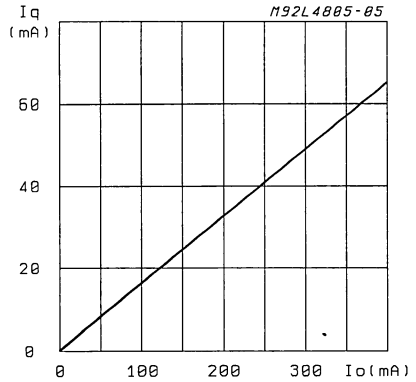


Figure 3: Output Voltage vs. Temperature

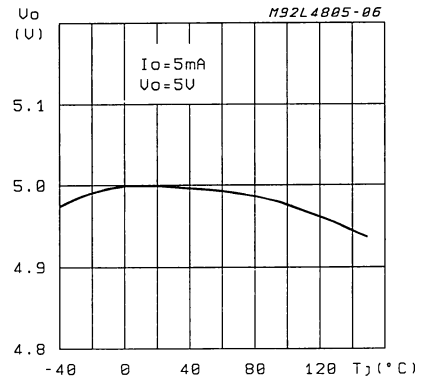


Figure 4: Foldback Current Limiting(L4805)

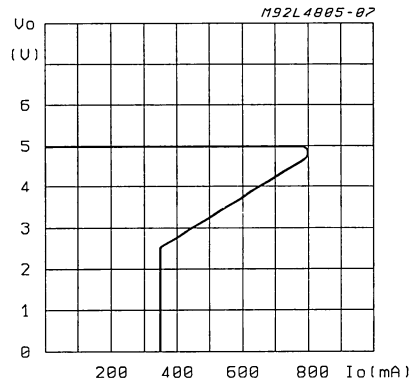
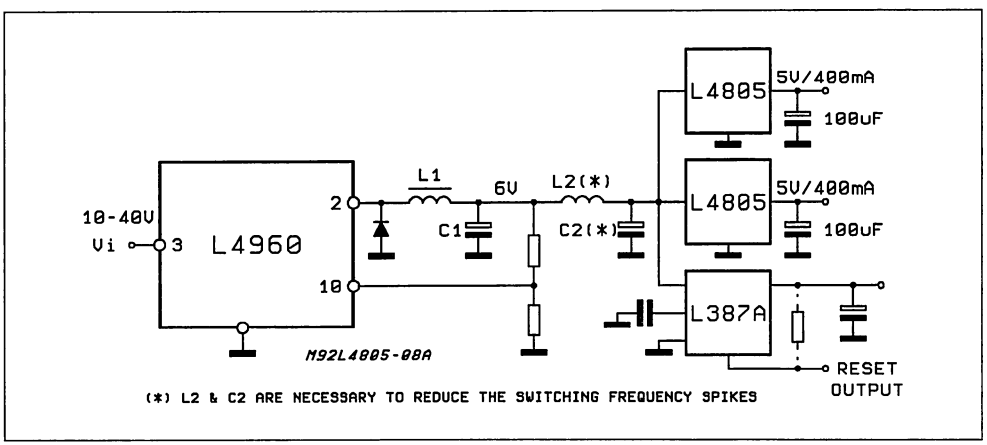


Figure 5: Preregulator for Distributed Supplies



SGS-THOMSON MICROELECTRONICS

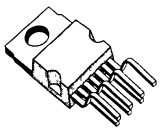
L4901A

DUAL 5V REGULATOR WITH RESET

- OUTPUT CURRENTS: I_{01} = 400mA
  I_{02} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4901A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



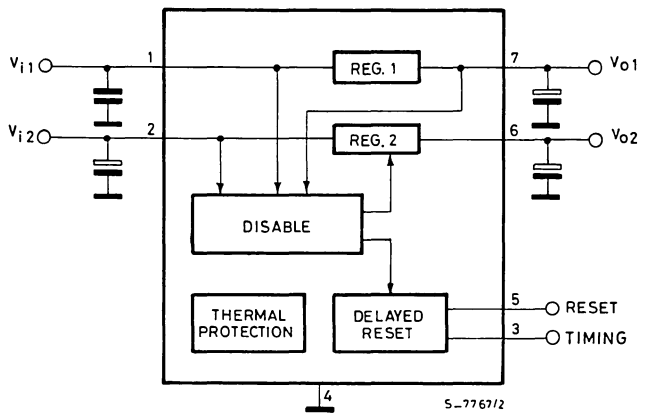
Heptawatt

ORDERING NUMBER: L4901A

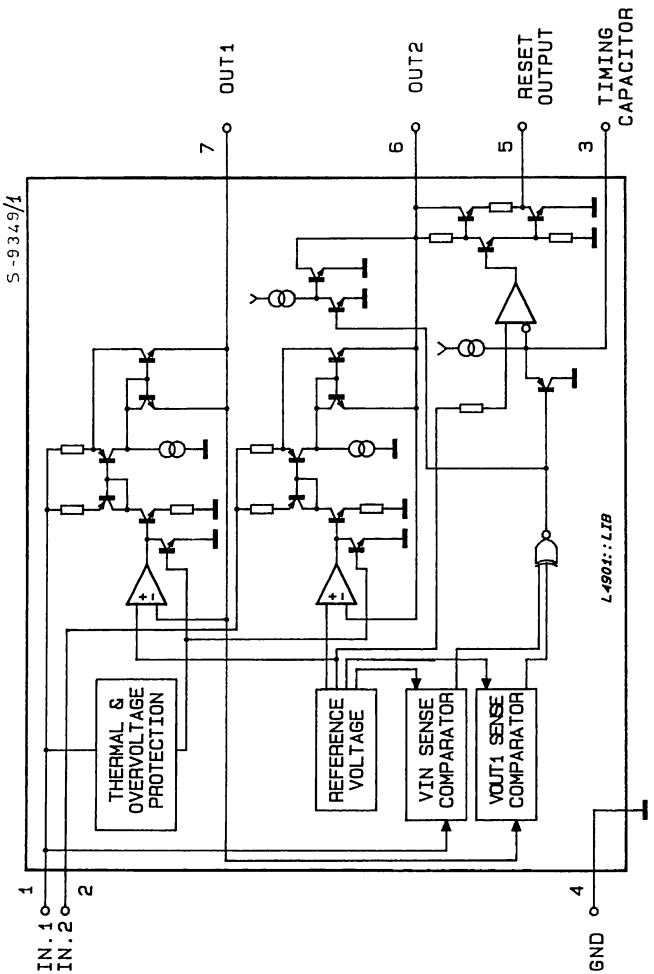
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

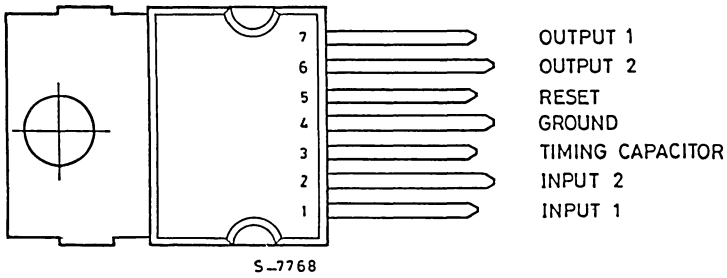
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



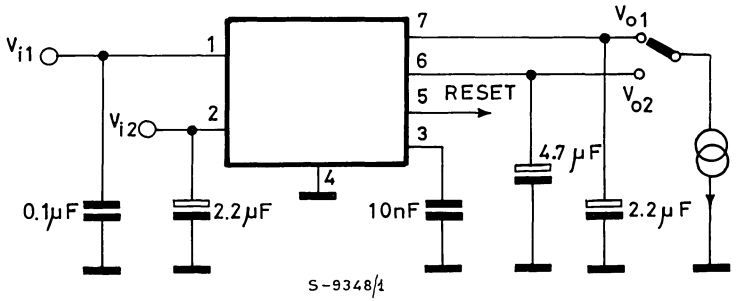
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 400mA regulator input.
2	INPUT 2	400mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF)
6	OUTPUT 2	5V - 400mA regulator output. Enabled if $V_{O1} > V_{RT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 400mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_{IN1} = V_{IN2} = 14,4V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	400			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	400			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 400mA		50	100	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 400mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4901A makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

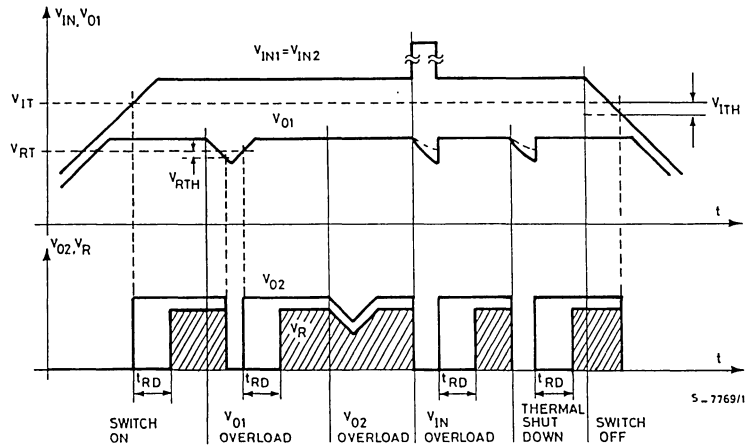
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4901A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

The L4901A is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shown in fig. 5 the reset output is used both to disable the μP and, through the address decoder M74HC138, to ensure that the RAMS are disabled as soon as the main supply starts to fall.

Another interesting application of the L4901A is in μP system with shadow memories. (see fig. 6)

When the input voltage goes below V_{IT}, the reset output enables the execution of a routine that saves the machine's state in the shadow RAM (xicor x 2201 for example).

Thanks to the low consumption of the Reg. 1 a 680μF capacitor on its input is sufficient to provide enough energy to complete the operation. The diode on the input guarantees the supply of the equipment even if a short circuit on V_I occurs.

APPLICATION SUGGESTION (continued)

Fig. 2

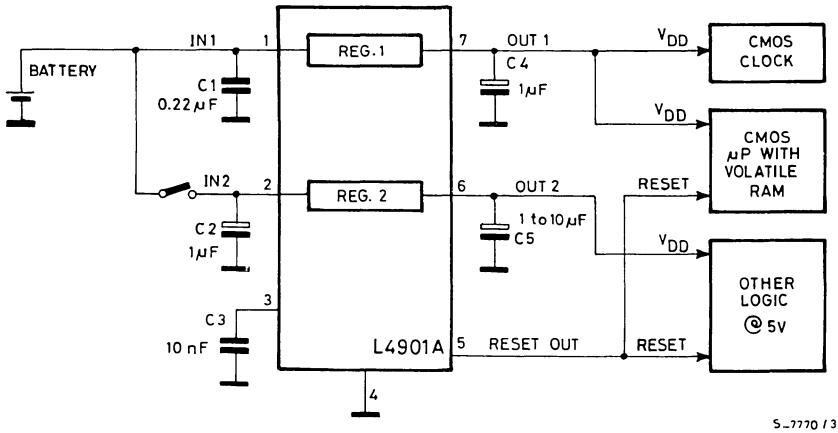
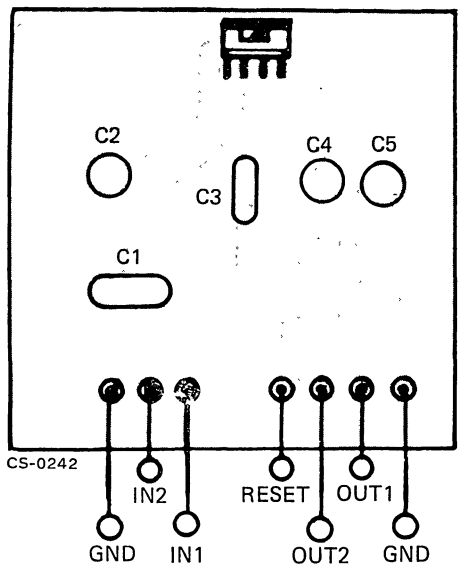


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

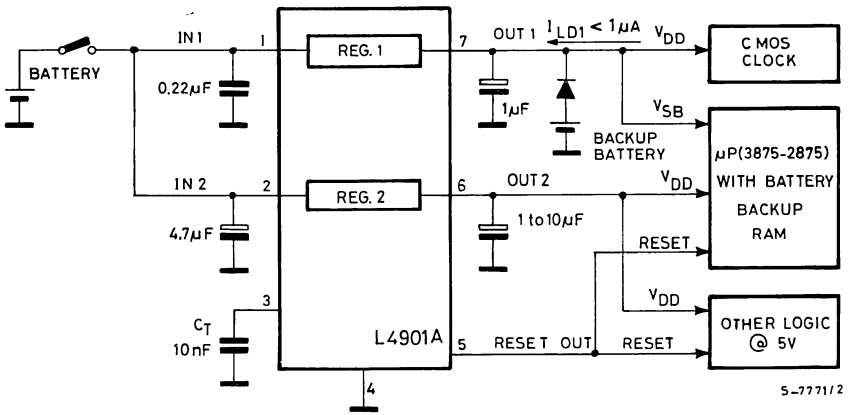
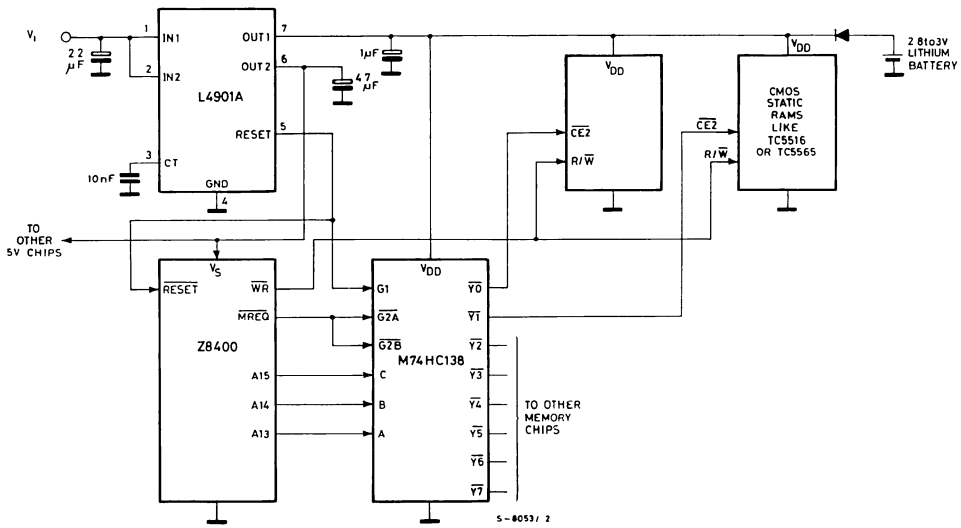


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6

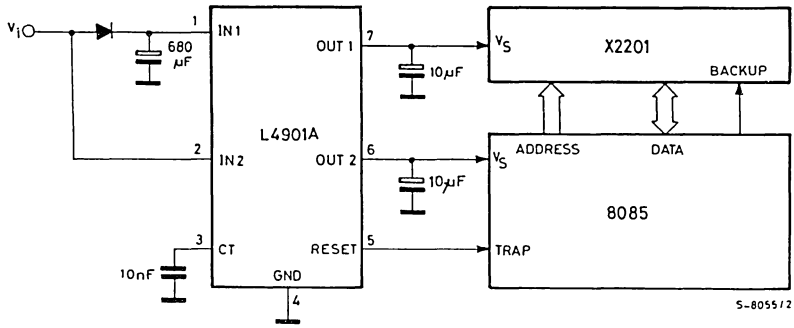


Fig. 7 - Quiescent current (Reg. 1) vs. output current

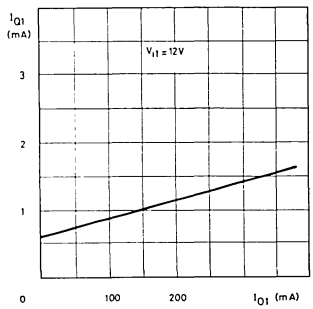


Fig. 8 - Quiescent current (Reg. 1) vs. input voltage

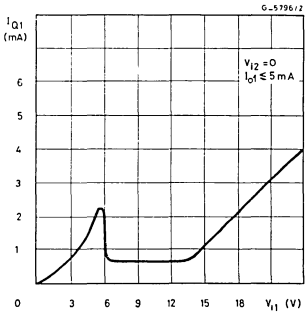


Fig. 9 - Total quiescent current vs. input voltage

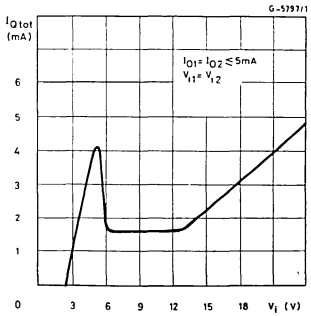


Fig. 10 - Regulator 1 output current and short circuit current vs. input voltage

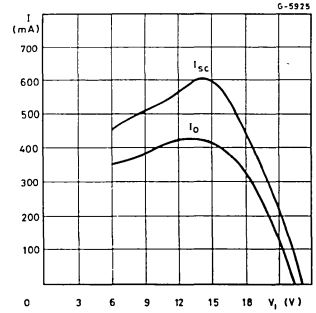


Fig. 11 - Regulator 2 output current and short circuit current vs. input voltage

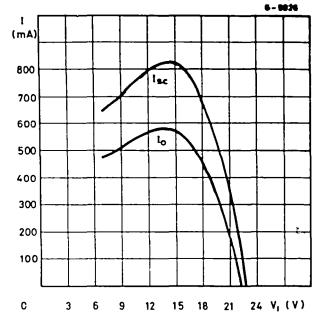
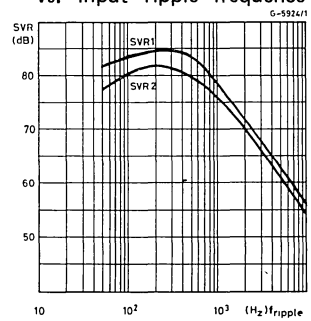


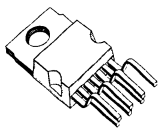
Fig. 12 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



DUAL 5V REGULATOR WITH RESET AND DISABLE

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: I_{01} = 300mA
  I_{02} = 300mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- RESET OUTPUT NORMALLY HIGH
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4902A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.
Reset and data save functions and remote switch on/off control can be realized.



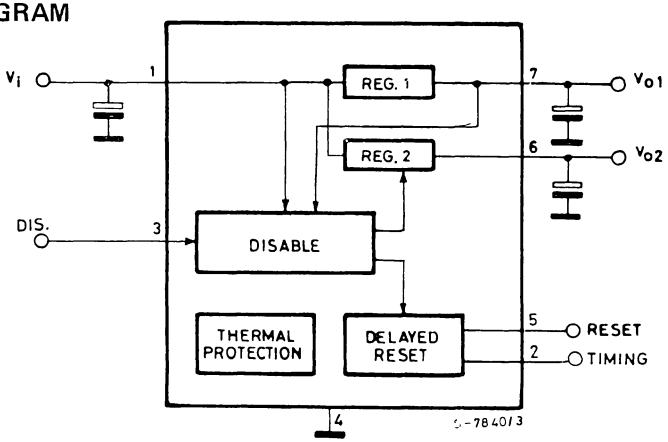
Heptawatt

ORDERING NUMBER: L4902A

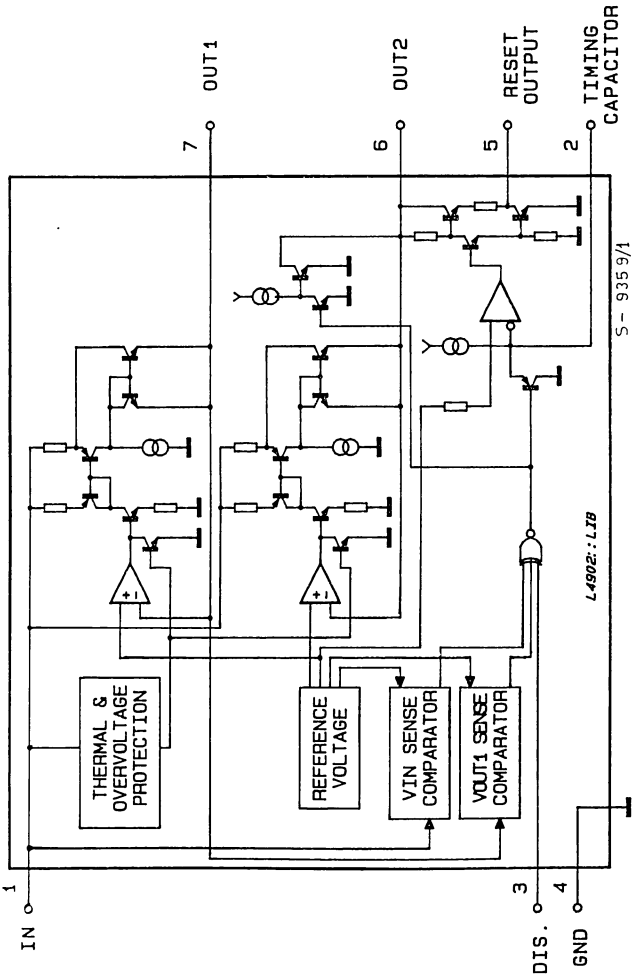
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
I_O	Output current	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

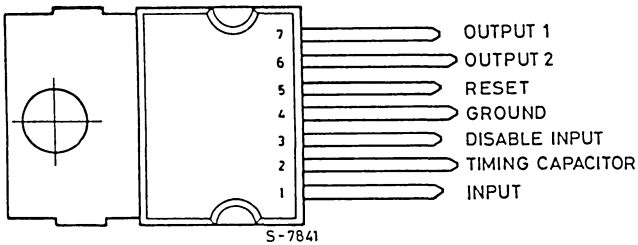
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



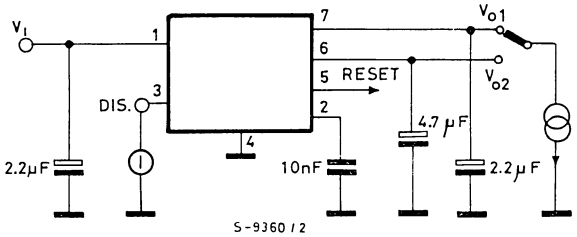
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Regulators common input.
2	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
3	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
4	GND	Common ground.
5	RESET OUTPUT	When pin 2 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF).
6	OUTPUT 2	5V - 300mA regulator output. Enabled if $V_O 1 > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 300mA. Low leakage (in switch-OFF condition) output.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				24	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max.	ΔV_{01} = -100mV	300			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2 max.	ΔV_{02} = -100mV	300			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 24V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 300mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 300mA		50	80	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -1mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	* 2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-150 -30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R=0.5V I_o = 100mA	50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4902A makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with common inputs plus a reset output for the data save function and a Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:
- a high level ($> V_{DT}$) is applied on pin 3;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:
- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

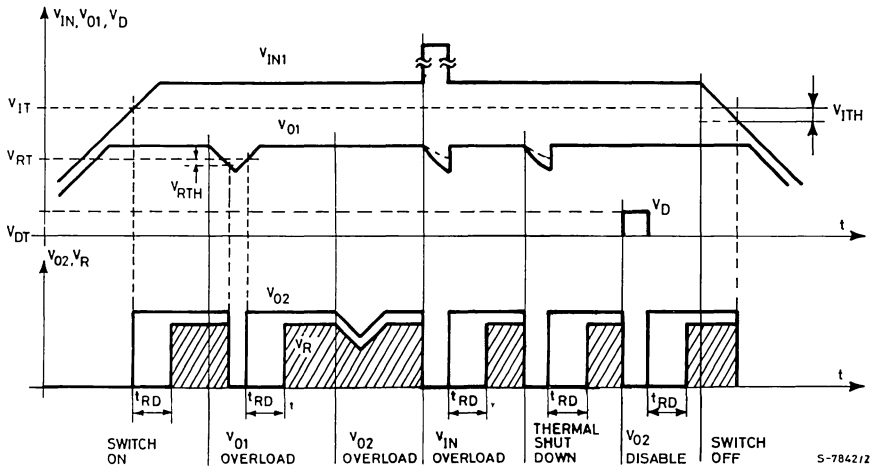
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



APPLICATION SUGGESTION

Fig. 2 illustrate how the L4902A's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Another application for the L4902A is supplying a shadow-ram microcomputer chip (SGS M38SH72 for exemple) where a fast NV memory is backed up on chip by a EEPROM when a low level on the reset output occurs.

By adding two CMOS-SCHMIDT-TRIGGER and few external components, also a watch dog function may be realized (see fig. 5). During normal operation the microsystem supplies a periodical pulse waveform; if an anomalous condition occours (in the program or in the system), the pulses will be absent and the disable input will be activated after a settling time determined by R1 C1. In this condition all the circuitry connected to V_{02} will be disabled, the system will be restarted with a new reset front.

The disable of V_{02} prevent spurious operation during microprocessor malfunctioning.

APPLICATION SUGGESTION (continued)

Fig. 2

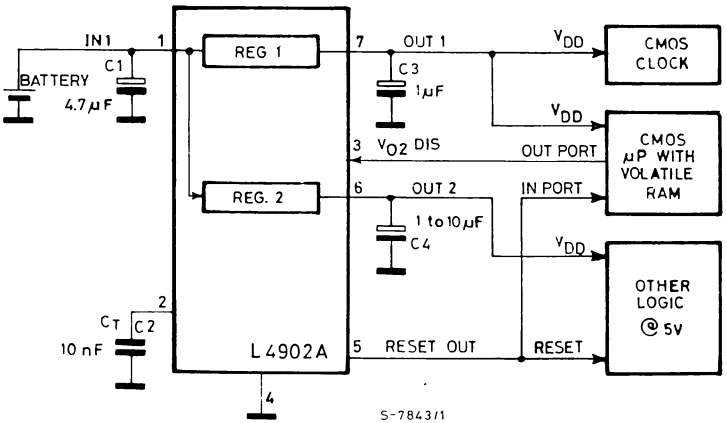
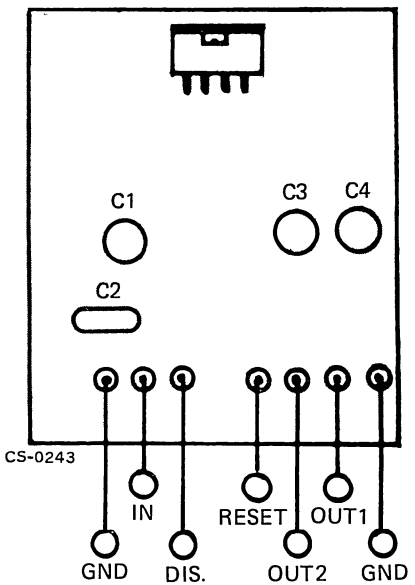


Fig. 3 - P.C. board and component layout of the circuit of Fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

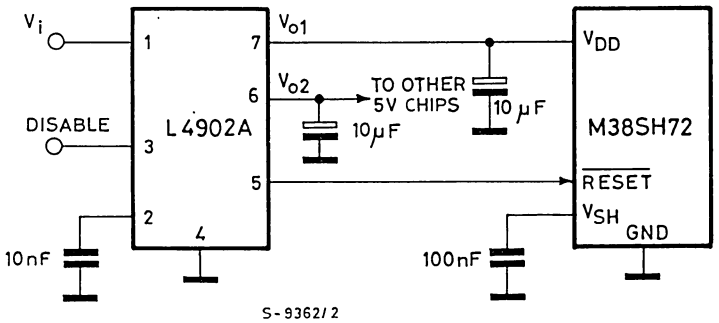
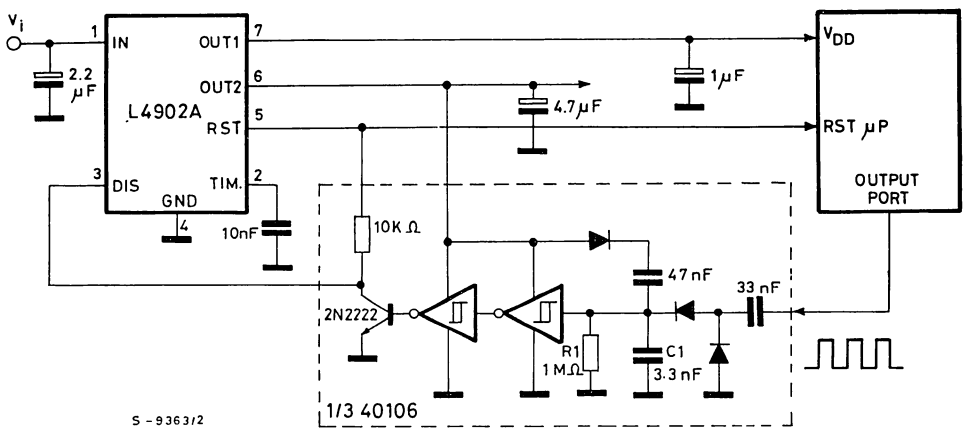


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6 - Quiescent current vs. output current

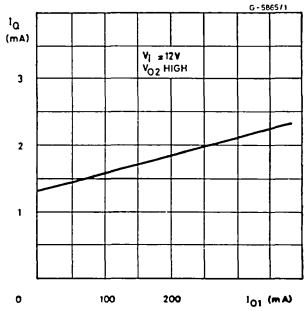


Fig. 7 - Quiescent current vs. input voltage

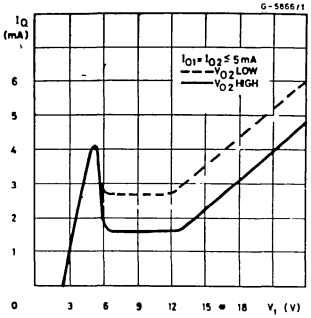
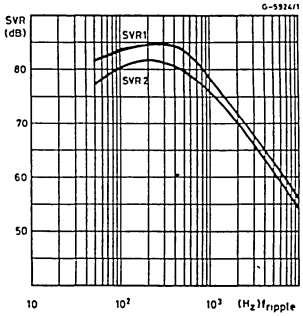


Fig. 8 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

- OUTPUT CURRENTS: I_{01} = 50mA
  I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ±2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4903 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset, data save functions and remote switch on/off control can be realized.

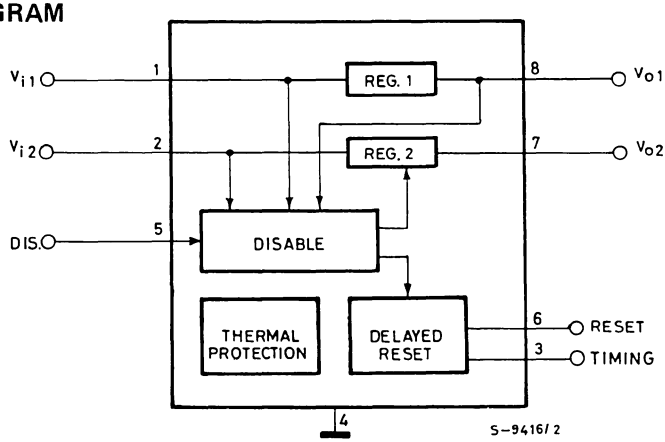
Minidip Plastic

ORDERING NUMBER: L4903

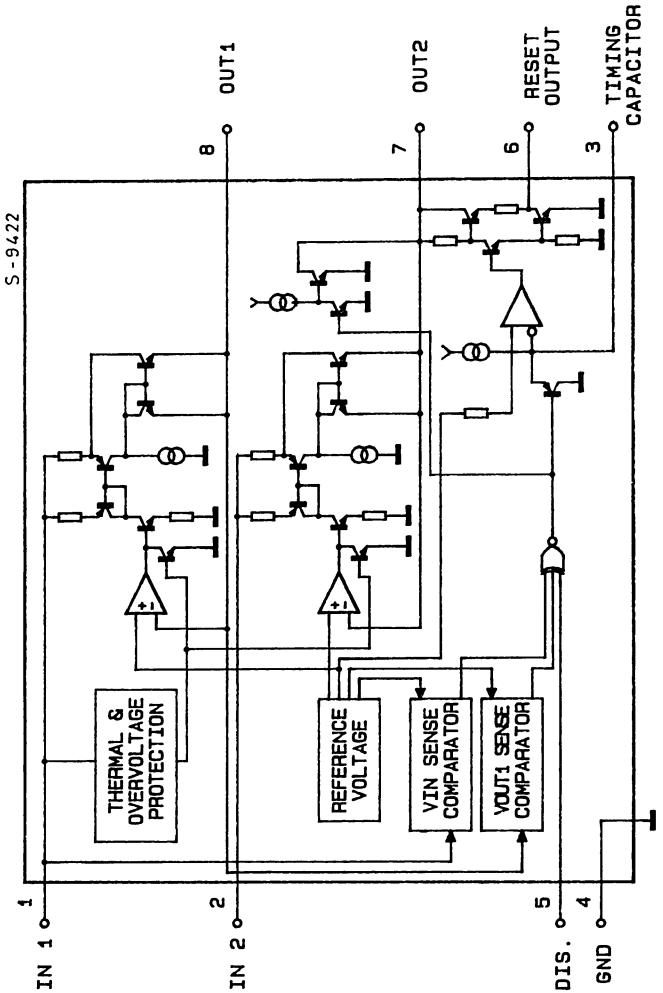
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
V_t	Transient input overvoltage (t = 40 ms)	60	V
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

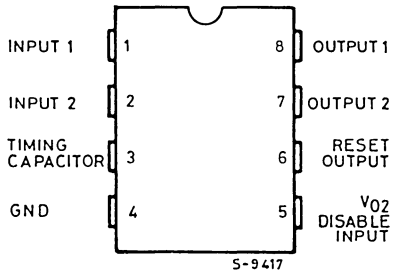
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



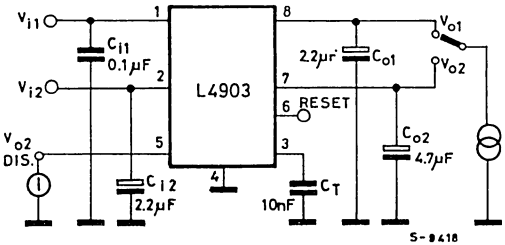
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disables output Reg. 2.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if V_O 1 $> V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

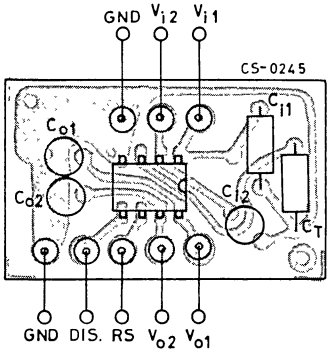
THERMAL DATA

$R_{th\,j\text{-}pin}$	Thermal resistance junction-pin 4	max	70	°C/W
$R_{th\,j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max. (*)	ΔV_{01} = -100mV	50			mA
I_{LO1}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2 max. (*)	ΔV_{02} = -100mV	100			mA
V_{I01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	V_{IN1} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 I_{01} < 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.4	4.7	V_{02}-0.2	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-150 30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	50	84		dB
SVR2	Supply voltage rejection	I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current conditions.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4903 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function and Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02} and V_R) switches on and the reset output (V_R) goes low after a programmable time T_{RD} (timing capacitor).

V_{02} is switched at low level and V_R at high level when one of the following conditions occurs:

- a high level ($> V_{DT}$) is applied on pin 5;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

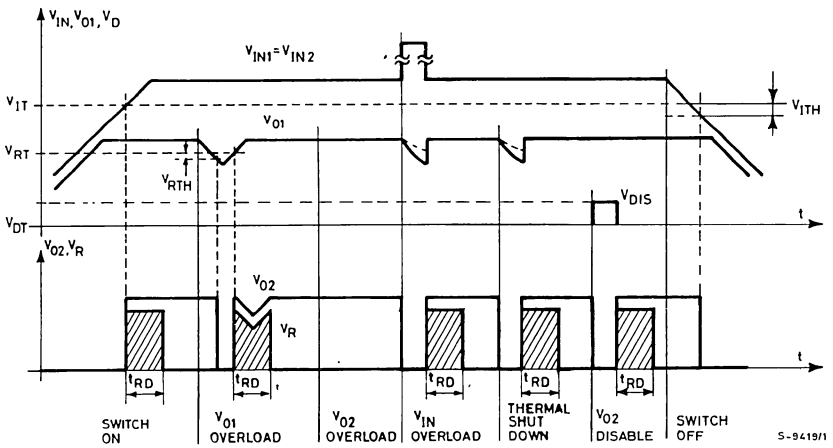
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



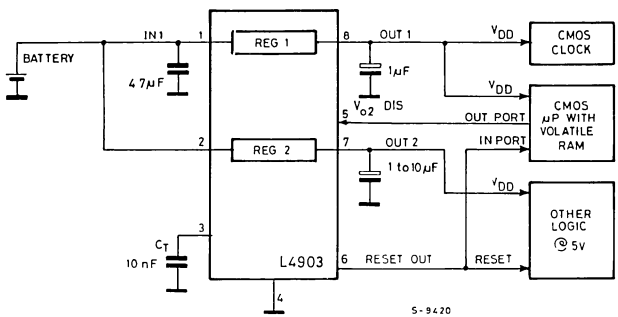
APPLICATION SUGGESTION

Fig. 2 illustrates how the L4903's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Fig. 2



APPLICATION SUGGESTIONS (continued)

Fig. 3 - Quiescent current (Reg. 1) vs. output current

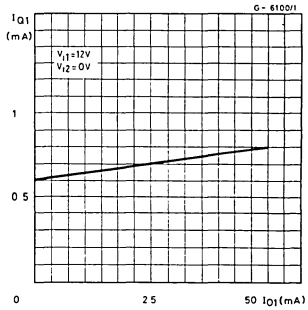


Fig. 4 - Quiescent current (Reg. 1) vs. input voltage

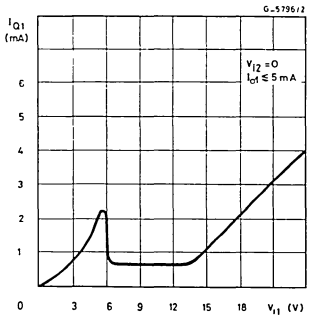


Fig. 5 - Total quiescent current vs. input voltage

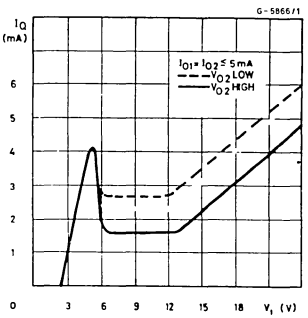
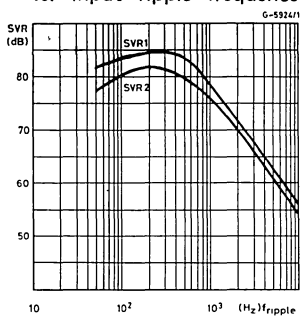


Fig. 6 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



SGS-THOMSON MICROELECTRONICS

L4904A

DUAL 5V REGULATOR WITH RESET

- OUTPUT CURRENTS: I_{o1} = 50mA
  I_{o2} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4904A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.

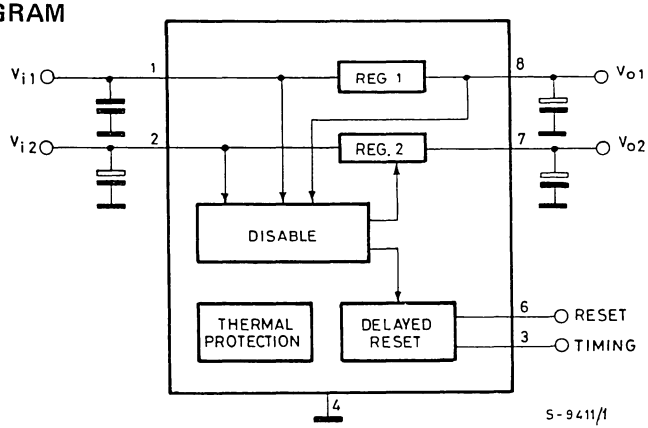
Minidip Plastic

ORDERING NUMBER: L4904A

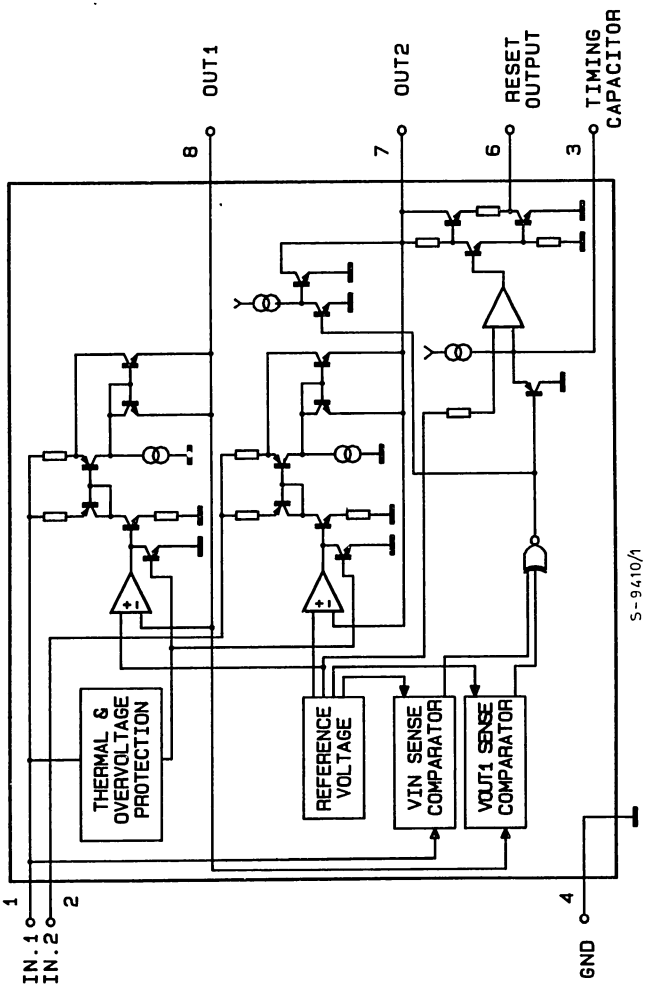
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_j	Storage and junction temperature	-40 to 150	°C

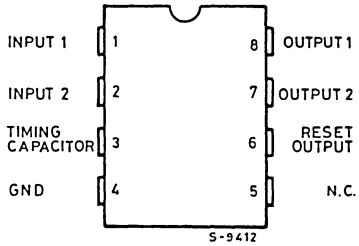
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



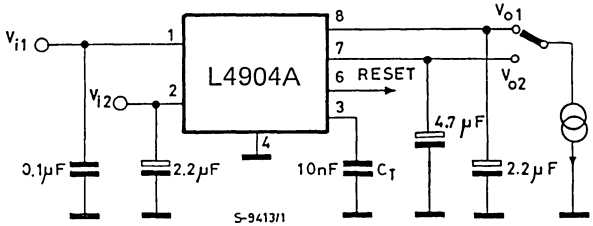
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN 2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

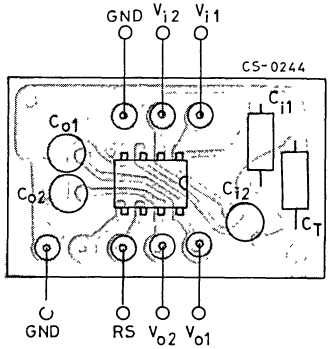
THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_I	DC operating input voltage				20	V
V_{O1}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{O2H}	Output voltage 2 HIGH	R load 1KΩ	V_{O1} -0.1	5	V_{O1}	V
V_{O2L}	Output voltage 2 LOW	I_{O2} = -5mA		0.1		V
I_{O1}	Output current 1	ΔV_{O1} = -100mV	50			mA
I_{LO1}	Leakage output 1 current	V_{IN} = 0 $V_{O1} \leq$ 3V			1	µA
I_{O2}	Output current 2	ΔV_{O2} = -100mV	100			mA
V_{IO1}	Output 1 dropout voltage (*)	I_{O1} = 10mA I_{O1} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{O1} +1.2	6.4	V_{O1} +1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{O1}	Line regulation	7V < V_{IN} < 18V I_{O1} = 5mA		5	50	mV
ΔV_{O2}	Line regulation 2	I_{O2} = 5mA		5	50	
ΔV_{O1}	Load regulation 1	V_{IN} = 8V 5mA < I_{O1} < 50mA		5	20	mV
ΔV_{O2}	Load regulation 2	5mA < I_{O2} < 100mA		10	50	
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{O2} = $I_{O1} \leq$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{O1} \leq$ 5mA I_{O2} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3		11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	50	84		dB
SVR2	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4904A makes it very easy to supply such equipments; it provides two voltage regulators (booth 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01} regulator also features low consumption (0.6mA

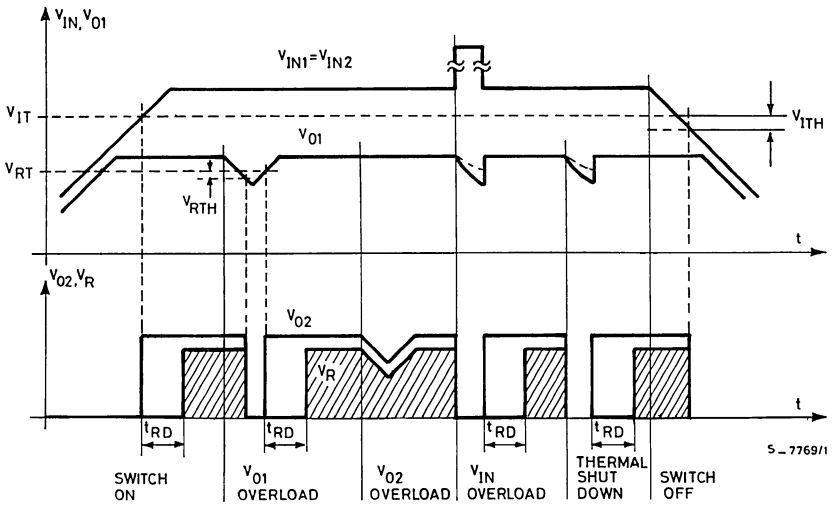
CIRCUIT OPERATION (continued)

typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 3 shows the L4904A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type C-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTIONS (continued)

Application Circuits of a Microprocessor system (Fig. 2) or with data save battery (Fig. 3). The reset output provide delayed rising front at the turn-off of the regulator 2.

Fig. 2

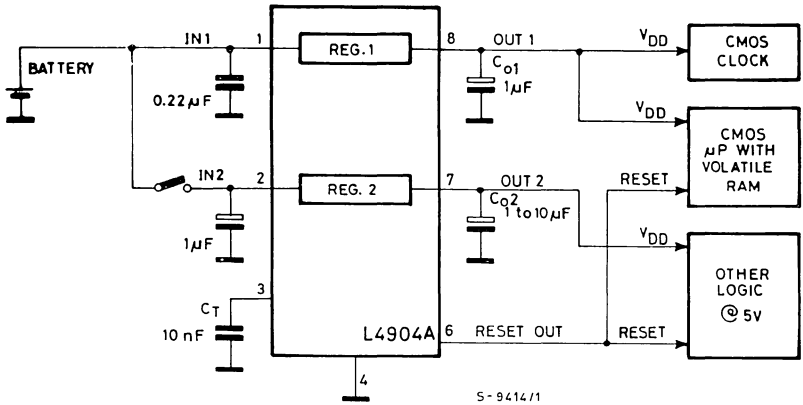
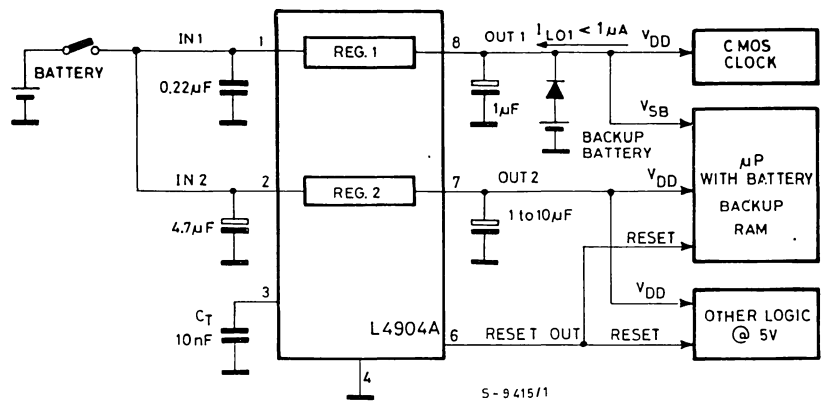


Fig. 3



APPLICATION SUGGESTIONS (continued)

Fig. 4 - Quiescent current (Reg. 1) vs. output current

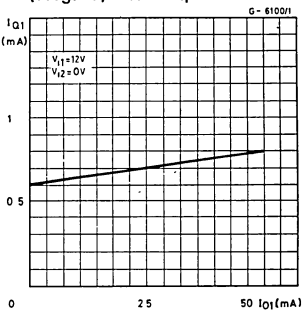


Fig. 5 - Quiescent current (Reg. 1) vs. input voltage

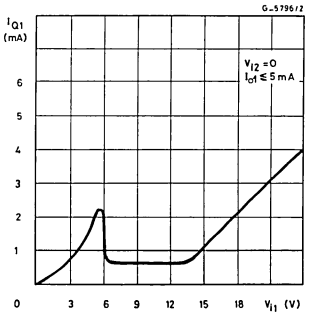


Fig. 6 - Total quiescent current vs. input voltage

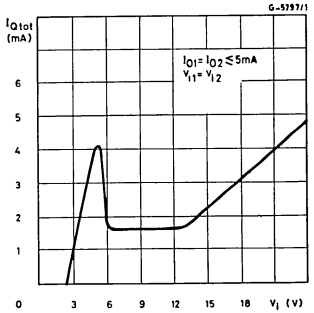
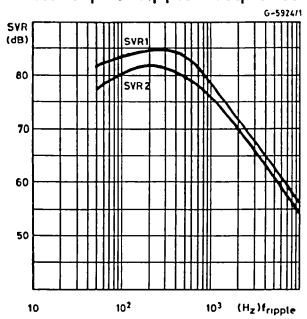


Fig. 7 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



SGS-THOMSON MICROELECTRONICS

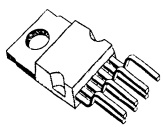
L4905

DUAL 5V REGULATOR WITH RESET

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: $I_{01} = 200mA$ $I_{02} = 300mA$
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 1%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCIENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4905 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



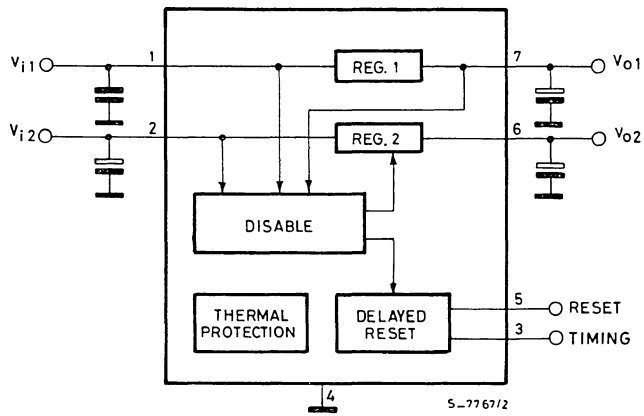
Heptawatt

ORDERING NUMBER: L4905

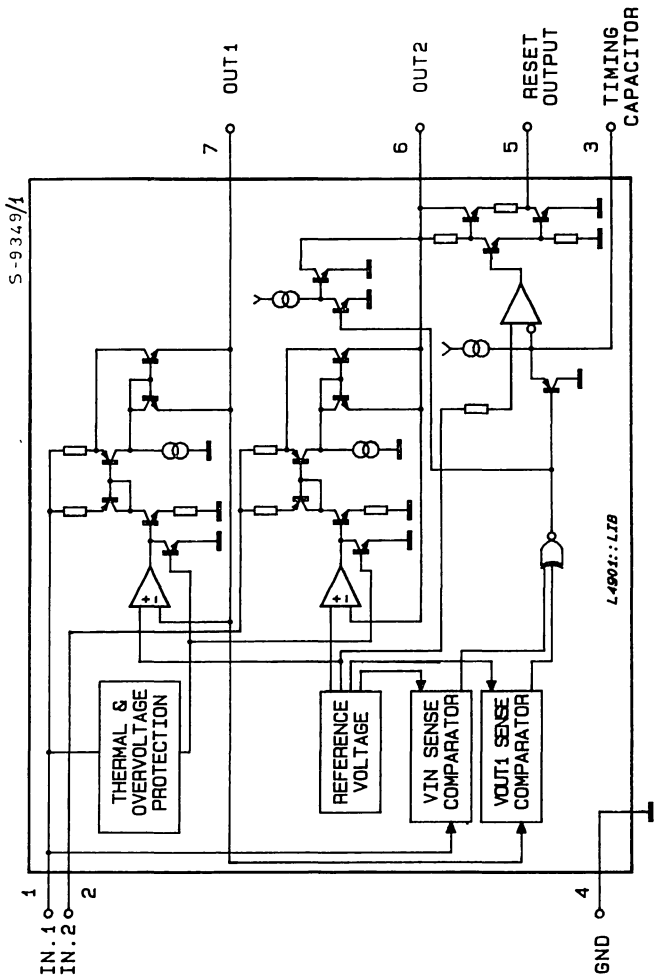
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

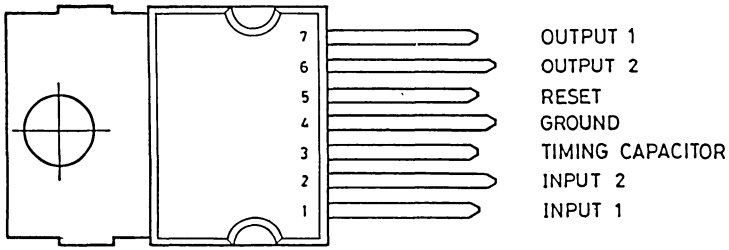
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



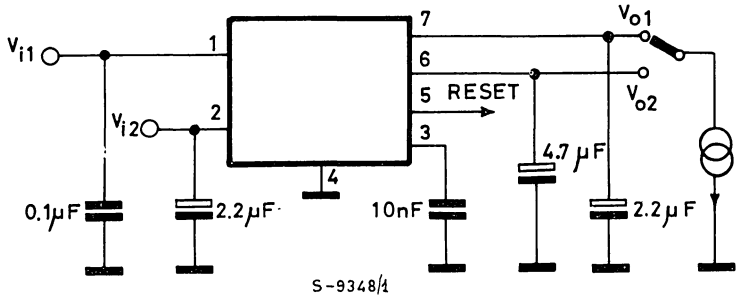
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 200mA regulator input.
2	INPUT 2	300mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A} \right)$; t_{RD} (ms) = C_t (nF)
6	OUTPUT 2	5V - 300mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 200mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{IN1} = V_{IN2} = 14,4V, T_{amb} = 25° unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_I	DC operating input voltage				24	V
V_{01}	Output voltage 1	R load 1KΩ	5.0	5.05	5.1	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	200			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	300			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 200mA		0.7 0.8 1.05	0.8 1 1.3	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 24V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 200mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 300mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	54 50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4905 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;
- permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

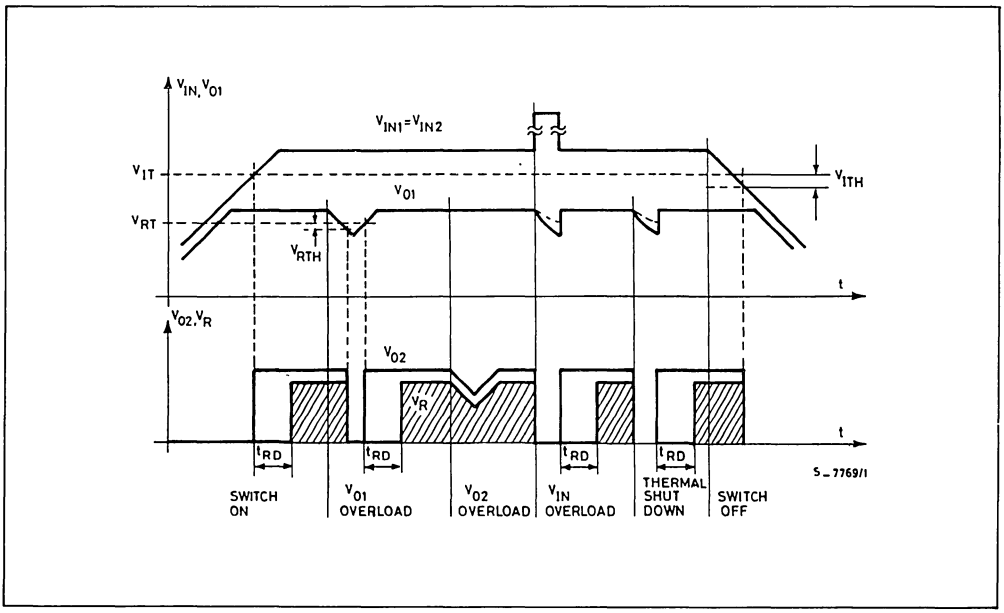
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a µP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4905 with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS µP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTION (continued)

Fig. 2

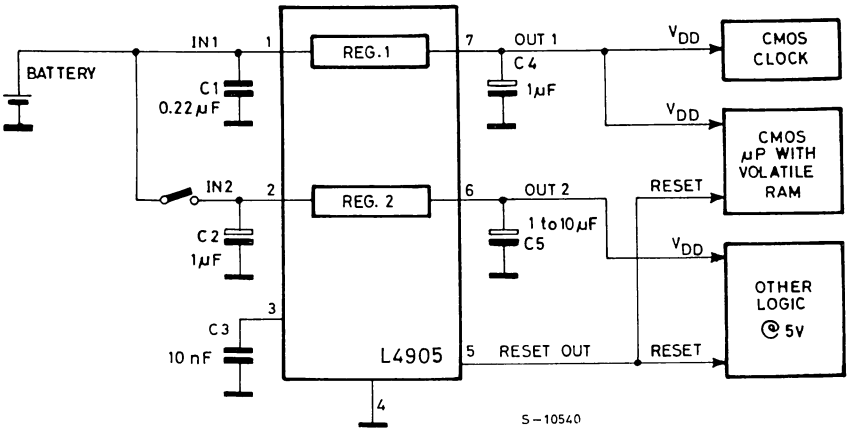
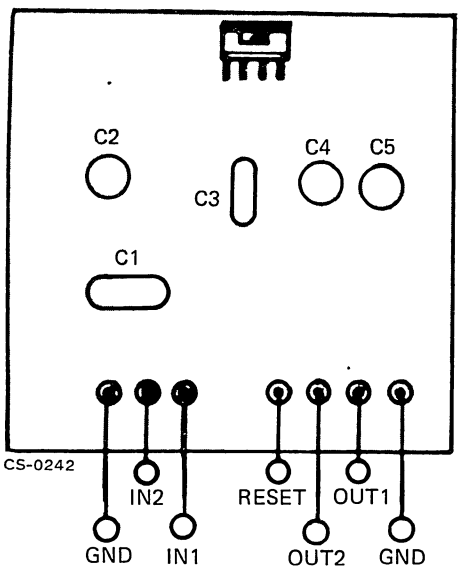


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

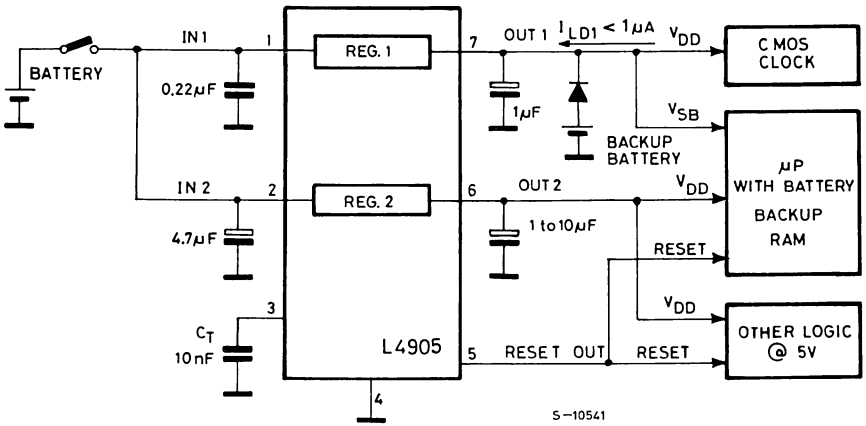


Fig. 5 - Quiescent current (Reg. 1) vs. output current

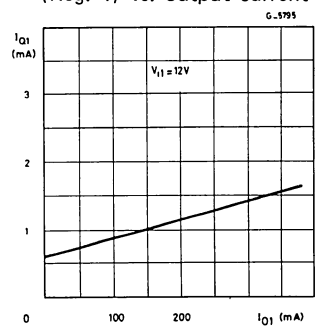


Fig. 6 - Quiescent current (Reg. 1) vs. input voltage

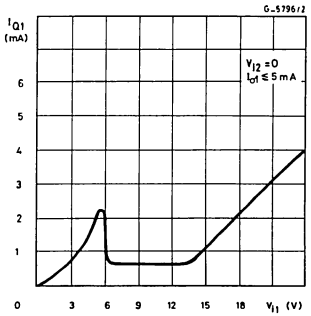
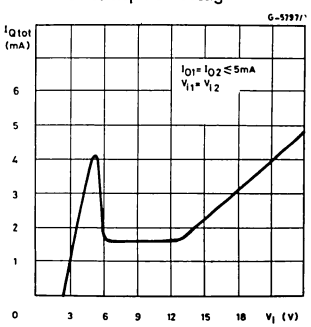


Fig. 7 - Total quiescent current vs. input voltage



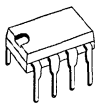
ADJUSTABLE VOLTAGE REGULATOR PLUS FILTER

- OUTPUT VOLTAGE ADJUSTABLE FROM 4 TO 11V
- HIGH OUTPUT CURRENT (UP TO 250mA)
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION

This circuit combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wide input voltage range.

A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltage.

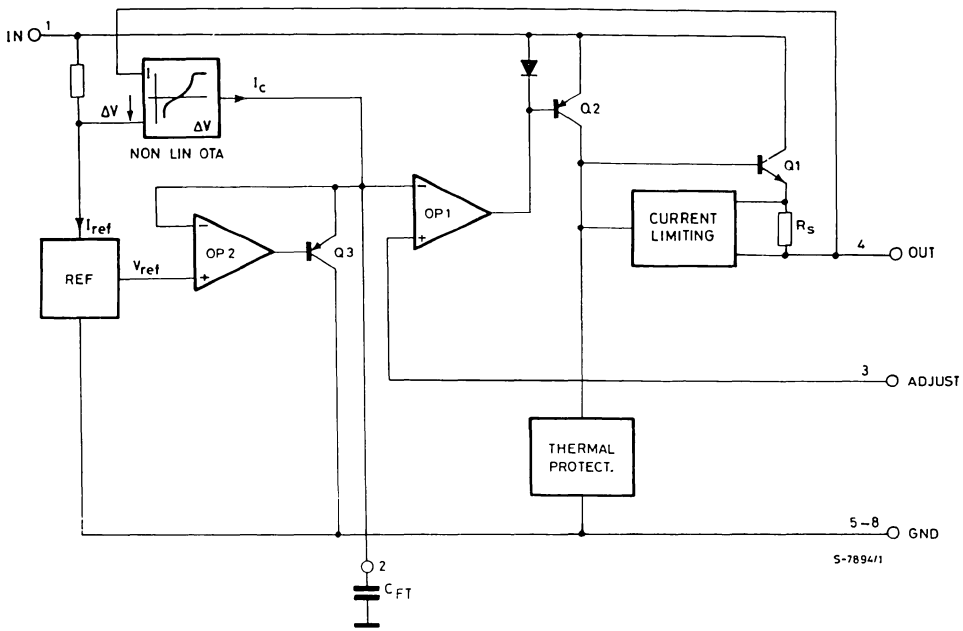
The non linear behaviour of this control circuitry allows a fast settling of the filter.



Power Minidip
(4 + 4)

ORDERING NUMBER: L4915

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_i	Peak input voltage (300ms)	40	V
V_i	DC input voltage	28	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM

(Top view)

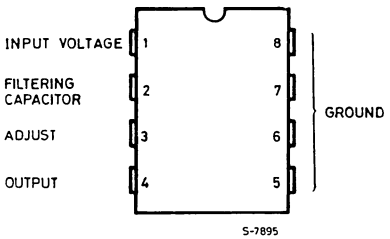
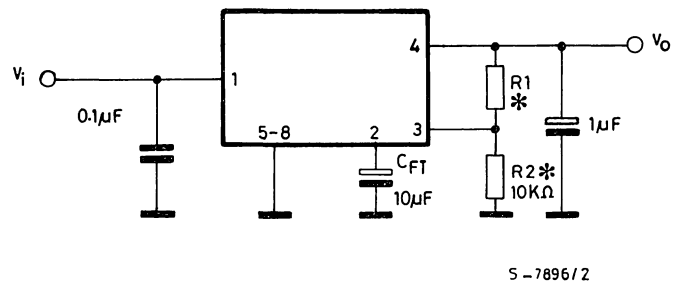


Fig. 1 - Application circuit



$$*\text{OUTPUT VOLTAGE } V_o = \frac{2.5(R1+R2)}{R2}$$

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	20	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_i = 13.5V, V_o = 8.5V, circuit of Fig. 1, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	Input voltage				20	V
V_o	Output voltage	V_i = 6 to 18V I_o = 5 to 150mA	4		11	V
$\Delta V_{I/O}$	Controlled input-output dropout voltage	I_o = 5 to 150mA V_i = 6 to 10V		1.6	2.1	V
ΔV_o	Line regulation	V_i = 12 to 18V I_o = 10mA		1	20	mV
ΔV_o	Load regulation	I_o = 5 to 250mA t_{on} = 30μs t_{off} = ⩾ 1ms		50	100	mV
ΔV_o	Load regulation (filter mode)	V_i = 8.5V I_o = 5 to 150mA t_{on} = 30μs t_{off} = ⩾ 1ms		150	250	mV
V_{ref}	Internal voltage reference			2.5		V
I_q	Quiescent current	I_o = 5mA		1	2	mA
ΔI_q	Quiescent current change	V_i = 6 to 18V I_o = 5 to 150mA		0.05		mA
I_{AD}	Adjust input current			40		nA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 10mA		1.2		mV/°C
SVR	Supply voltage rejection	V_{iac} = 1V_{rms} f = 100Hz I_o = 150mA Regulator		71		dB
		Filter mode		35 (*)		dB
I_{SC}	Short circuit current		250	300		mA
T_{on}	Switch on time	I_o = 150mA Filter mode		500 (*)		ms
		Regulator		300		ms
T_j	Thermal shutdown junction temperature			145		°C

(*) Depending of the C_{FT} capacitor.

PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{I\,MIN} = V_{OUT\,NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.
The series pass element uses a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from a REF through the OP2 and Q3, acting as an active zener diode of value V_{REF}.
In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig. 2).
The output voltage is fixed to its nominal value:

$$V_{OUT\,NOM} = V_{REF}\ (1 + \frac{R1}{R2}) =$$

$$V_{CFT}\ (1 + \frac{R1}{R2})$$

The ripple rejection is quite high (70dB) and independent to C_{FT} value.
On the usual voltage regulators, when the input voltage goes below the nominal value, the regulation transistors (series element) saturate bringing the system out of regulation and making it very sensible to every variation of the input voltage. On the contrary, a control loop on the L4915 consents to avoid the saturation of the series element by regulating the value of the reference voltage (pin 2). In fact, whenever the input voltage decreases below ($V_{I\,MIN}$ the supervisor loop, utilizing a non linear OTA, forces the reference voltage at pin 2 to decrease by discharging C_{FT}. So, during the static mode, when the input voltage goes below V_{MIN} the drop out is kept fixed to about 1.6V. In this condition the device works as a low pass filter in the range (2) of the OTA characteristic. The ripple rejection is externally adjustable acting on C_{FT} as follows:

$$SVR\ (j\Omega) = \left| \frac{V_i\ (j\Omega)}{V_{out}\ (j\Omega)} \right| =$$

$$\left| 1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}}\ (1 + \frac{R1}{R2})} \right|$$

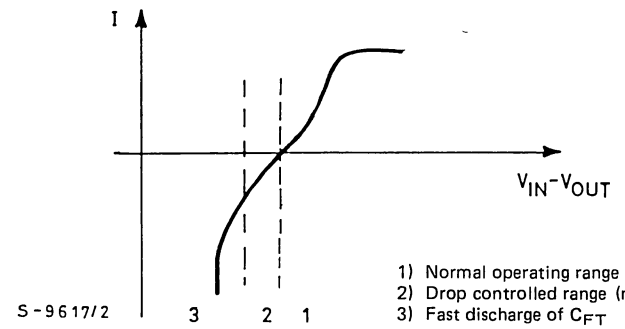
Where:
$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the transconductance of the OTA and by C_{FT}. When the value of the ripple voltage is so high and its negative peak is fast enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharges the capacitor rapidously.
If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection; the device's again working as a filter (fast transient range).
With C_{FT} = 10μF; f = 100Hz; V_o = 8.5V a SVR of 35 is obtained.

Fig. 2 - Nonliner transfer characteristic of the drop control unit



1) Normal operating range (high ripple rejection)
2) Drop controlled range (medium ripple rejection)
3) Fast discharge of C_{FT}

Fig. 3 - Supply voltage rejection vs. input voltage

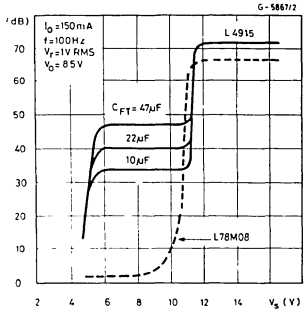


Fig. 4 - Supply voltage rejection vs. frequency

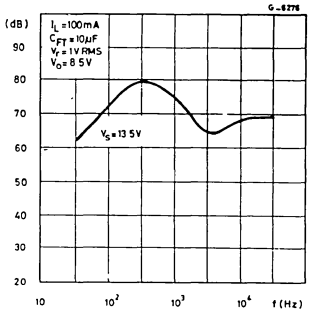


Fig. 5 - V_o vs. supply voltage (V_o = 8.5V)

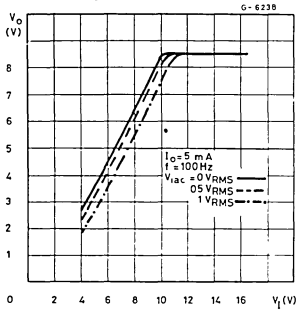


Fig. 6 - Quiescent current vs. input voltage (V_o = 8.5V)

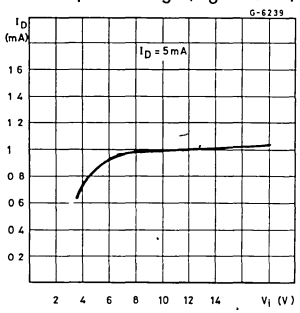
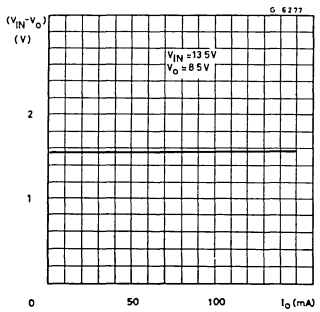


Fig. 7 - Dropout vs. load current



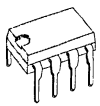
VOLTAGE REGULATOR PLUS FILTER

- FIXED OUTPUT VOLTAGE 8.5V
- 250mA OUTPUT CURRENT
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION

This circuit combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wider input voltage range.

A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltages.

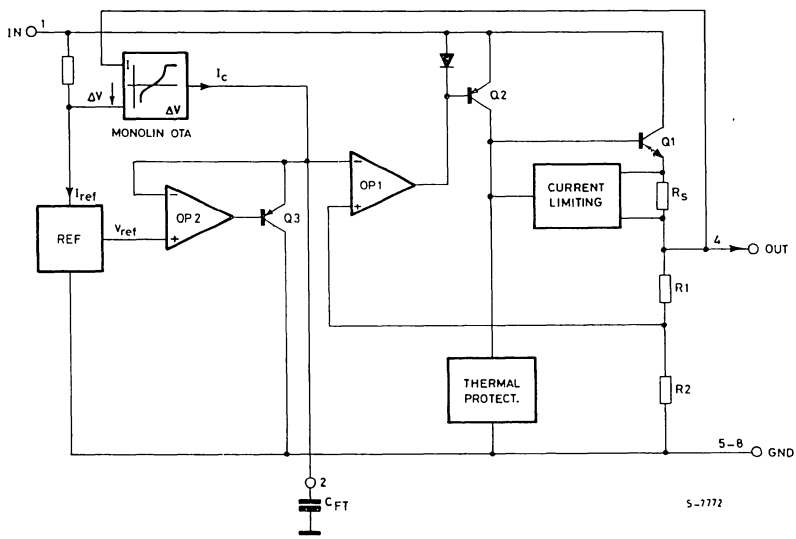
The non linear behaviour of this control circuitry allows a fast settling of the filter.



Power Minidip
(4 + 4)

ORDER CODE: L4916

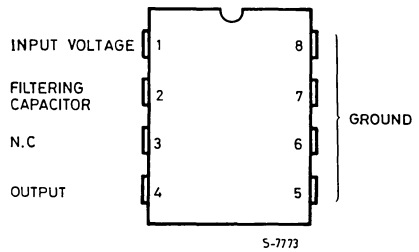
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_I	Peak input voltage (300 ms)	40	V
V_i	DC input voltage	28	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction pins	max	20	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_i = 13.5V, Test circuit of fig. 1, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	Input voltage				20	V
V_o	Output voltage	V_i = 12 to 18V I_o = 5 to 150mA	8.1	8.5	8.9	V
$\Delta V_{I/O}$	Controlled input-output dropout voltage	V_i = 5 to 10V I_o = 5 to 150mA		1.6	2.1	V
ΔV_o	Line regulation	V_i = 12 to 18V I_o = 10mA		1	20	mV
ΔV_o	Load regulation	I_o = 5 to 250mA t_{on} = 30μs t_{off} = ⩾ 1ms		50	100	mV
ΔV_o	Load regulation (filter mode)	V_i = 8.5V I_o = 5 to 150mA t_{on} = 30μs,. t_{off} = ⩾ 1ms		150	250	mV
I_q	Quiescent current	I_o = 5mA		1	2	mA
ΔI_q	Quiescent current change	V_i = 6 to 18V I_o = 5 to 150mA		0.05		mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 10mA		1.2		mV/°C
SVR	Supply voltage rejection	V_{iac} = 1V_{rms} f = 100Hz I_o = 150mA V_{IDC} = 12 to 18V V_{IDC} = 6 to 11V		70 35 (*)		dB dB
I_{SC}	Short circuit current		250	300		mA
T_{on}	Switch on time	I_o = 150mA V_i = 5 to 11V V_i = 11 to 18V		500 (*) 300		ms ms
T_j	Thermal shutdown junction temperature			145		°C

(*) Depending of the C_{FT} capacitor.

Fig. 1 - Test and Application Circuit

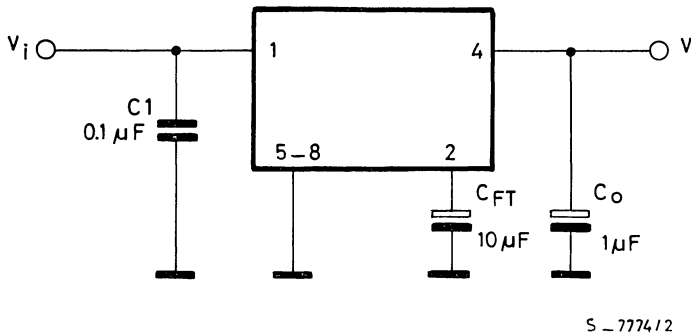
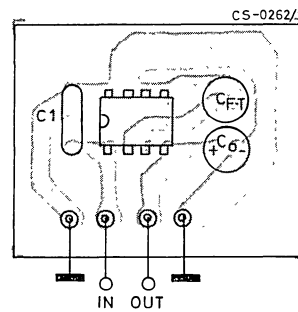


Fig. 2 - P.C. board and component layout of fig. 1 (1 : 1 scale)



PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{I\,MIN} = V_{OUT\,NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.
The series pass element use a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from a REF through the OP2 and Q3, acting as an active zener diode of value V_{REF}.
In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig. 3).
The output voltage is fixed to its nominal value:

$$V_{OUT\,NOM} = V_{REF}\,(1 + \frac{R1}{R2}) =$$

$$V_{CFT}\,(1 + \frac{R1}{R2})$$

$$\frac{R1}{R2} = \text{INTERNALLY FIXED RATIO} = 2.4$$

The ripple rejection is quite high (70 dB) and independent from C_{FT} value.
On the usual voltage regulators, when the input voltage goes below the nominal value, the regulation transistors (series element) saturate bringing the system out of regulation making it very sensible to every variation of the input voltage.
On the contrary, a control loop on the L4916 consents to avoid the saturation of the series element by regulating the value of the reference voltage (pin 2). In fact, whenever the input voltage decreases below $V_{I\,MIN}$ the supervisor loop, utilizing a non linear OTA, forces the reference voltage at pin 2 to decrease by discharging C_{FT}.

So, during the static mode, when the input voltage goes below V_{MIN} the drop out is kept fixed to about 1.6V. In this condition the device works as a low pass filter in the range (2) of the OTA characteristic. The fipple rejection is externally adjustable acting on C_{FT} as follows:

$$SVR\,(jw) = \left| \frac{V_I\,(jw)}{V_{out}\,(jw)} \right| = \left| 1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}}\,(1 + \frac{R1}{R2})} \right|$$

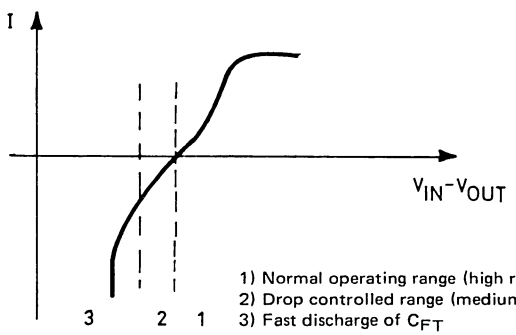
Where:
$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the transconductance of the OTA and by C_{FT}.
When the value of the ripple voltage is so high and its negative peak is fast enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharge the capacitor rapidously.
If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection; the device's again working as a filter (fast transient range).
With C_{FT}= 10 μF; f = 100 Hz a SVR of 35 is obtained.

Fig. 3 - Nonliner transfer characteristic of the drop control unit



1) Normal operating range (high ripple rejection)
2) Drop controlled range (medium ripple rejection)
3) Fast discharge of C_{FT}

S-9617/2

Fig. 4 - Supply voltage rejection vs. input voltage

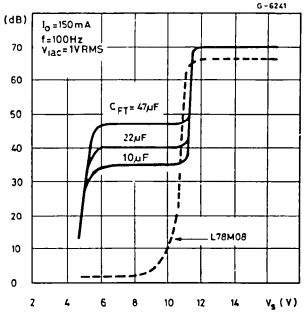


Fig. 5 - Supply voltage rejection vs. frequency

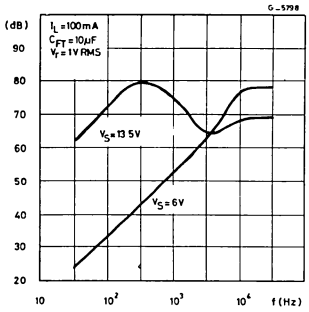


Fig. 6 - V_o vs. supply voltage

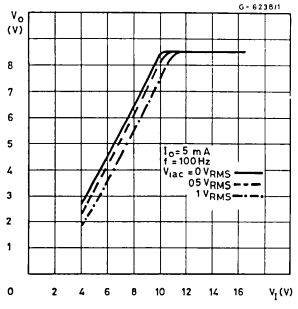


Fig. 7 - Quiescent current vs. input voltage

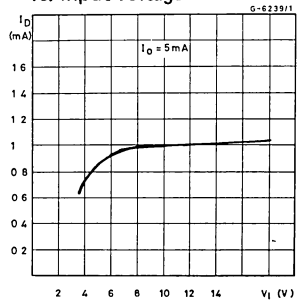


Fig. 8 - Dropout vs. load current

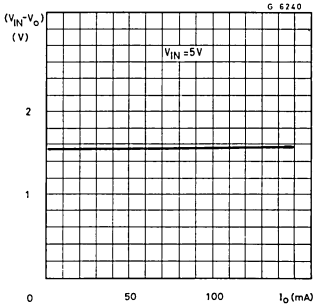
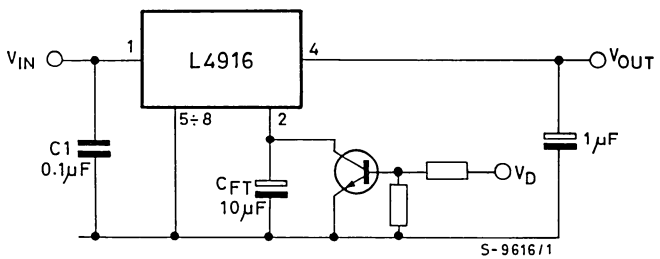


Fig. 9 - Inhibit function realized on C_{FT} pin.



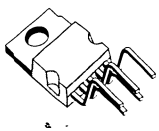
VOLTAGE REGULATOR PLUS FILTER

- FIXED OUTPUT VOLTAGE 8.5V
- 250mA OUTPUT CURRENT
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION

The L4918 combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wider input voltage range.

A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltages.

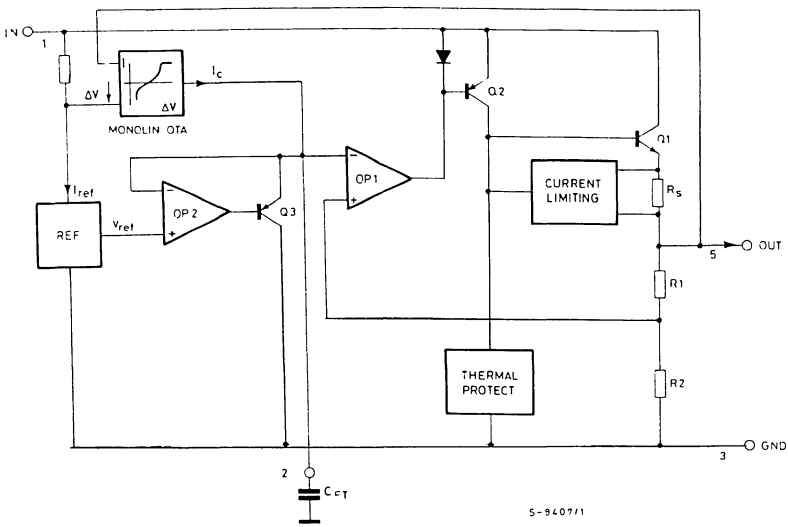
The non linear behaviour of this control circuitry allows a fast setting of the filter.



Pentawatt

ORDERING NUMBER: L4918

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Peak input voltage (300ms)	40	V
V_s	DC voltage	28	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(Top view)

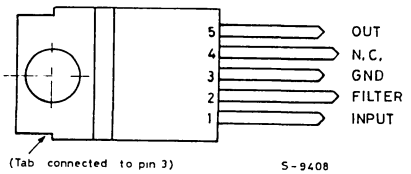
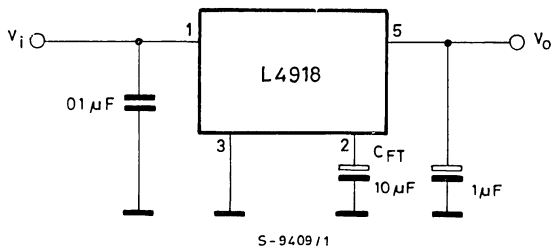


Fig. 1 - Application and test circuit



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_I = 13.5V unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_I	Input voltage				20	V
V_o	Output voltage	V_I = 12 to 18V I_o = 5 to 150mA	8.1	8.5	8.9	V
$\Delta V_{I/O}$	Controlled input-output dropout voltage	V_i = 5 to 10V I_o = 5 to 150mA		1.6	2.1	V
ΔV_o	Line regulation	V_i = 12 to 18V I_o = 10mA		1	20	mV
ΔV_o	Load regulation	I_o = 5 to 250mA t_{on} = 30μs t_{off} = $\geqslant$ 1ms			100	mV
ΔV_o	Load regulation	V_i = 8.5V I_o = 5 to 150mA t_{on} = 30μs t_{off} = $\geqslant$ 1ms		100	250	mV
I_q	Quiescent current	I_o = 5mA		1.0	2	mA
ΔI_q	Quiescent current change	V_i = 6 to 18V I_o = 5 to 150mA		0.05		mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 10mA		1.2		mV/°C
SVR	Supply voltage rejection	$\dot{V}_{Iac}$ = 1V_{rms} f = 100Hz I_o = 150mA V_{IDC} = 12 to 18V V_{IDC} = 6 to 11V		71 35 (*)		dB dB
I_{SC}	Short circuit current		250	300		mA
t_{on}	Switch on time	I_o = 150mA V_i = 5 to 11V V_i = 11 to 18V		500 (*) 300		ms ms
T_{JSD}	Thermal shut down			150		°C

(*) Depending of the C_{FT} capacitor

PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{I\,MIN} = V_{OUT\,NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.
The series pass element use a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from a REF through the OP2 and Q3, acting as an active zener diode of value V_{REF}.
In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig. 2)
The output voltage is fixed to its nominal value:

$$V_{OUT\,NOM} = V_{REF}\,(1 + \frac{R1}{R2}) =$$

$$V_{CFT}\,(1 + \frac{R1}{R2})$$

$$\frac{R1}{R2} = \text{INTERNALLY FIXED RATIO} = 2.4$$

The ripple rejection is quite high (71 dB) and independent from C_{FT} value.
On the usual voltage regulators, when the input voltage goes below the nominal value, the regulation transistors (series element) saturate bringing the system out of regulation making it very sensible to every variation of the input voltage. On the contrary, a control loop on the L4918 consents to avoid the saturation of the series element by regulating the value of the reference voltage (pin 2). In fact, whenever the input voltage decreases below $V_{I\,MIN}$ the supervisor loop, utilizing a non linear OTA, forces the reference voltage at pin 2 to decrease by discharging C_{FT}. So, during the static mode, when the input voltage goes below V_{MIN} the drop out is kept fixed to about 1.6V. In this condition the device works as a low pass filter in the range (2) of the OTA characteristic. The ripple rejection is externally adjustable acting on C_{FT} as follows:

$$SVR\,(jw) = \left|\frac{V_I\,(jw)}{V_{out}\,(jw)}\right| =$$

$$\left|1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}}\quad(1 + \frac{R1}{R2})}\right|$$

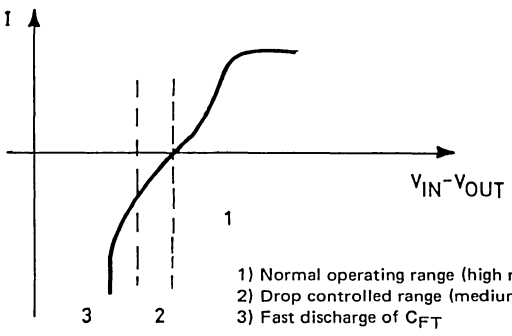
Where:
$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the tranconductance of the OTA and by C_{FT}. When the value of the ripple voltage is so high and its negative peak is fast/enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharge the capacitor rapidously.
If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection; the device's again working as a filter (fast transient range).
With C_{FT}= 10 μF; f = 100 Hz a SVR of 35 is obtained.

Fig. 2 - Nonliner transfer characteristic of the drop control unit



1) Normal operating range (high ripple rejection)
2) Drop controlled range (medium ripple rejection)
3) Fast discharge of C_{FT}

Fig. 3 - Supply voltage rejection vs. frequency

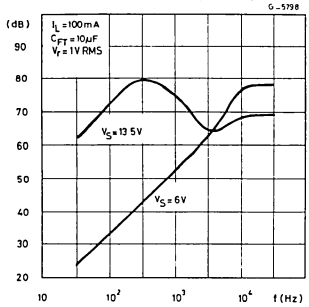


Fig. 4 - Supply voltage rejection vs. input voltage

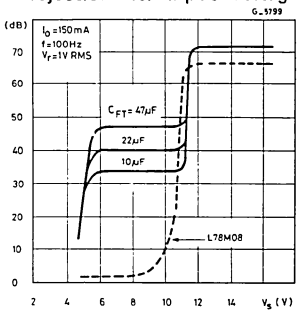
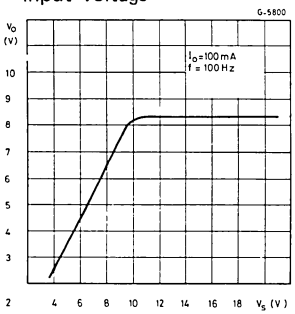
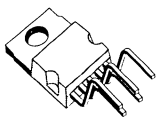


Fig. 5 - Output voltage vs input voltage



VERY LOW DROP ADJUSTABLE REGULATORS

- VERY LOW DROP VOLTAGE
- ADJUSTABLE OUTPUT VOLTAGE FROM 1.25V TO 20V
- 400mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- REVERSE VOLTAGE PROTECTION
- + 60/ – 60V TRANSIENT PEAK VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION WITH FOLD-BACK CHARACTERISTICS
- THERMAL SHUT-DOWN



Pentawatt

Minidip (4 + 4)

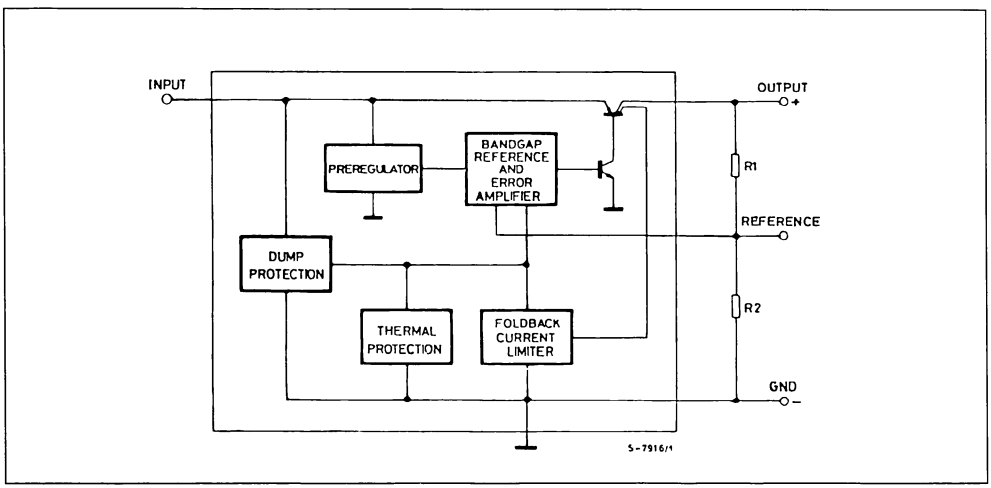
ORDER CODES : L4920 (Pentawatt)
L4921 (Minidip)

DESCRIPTION

The L4920 and L4921 are adjustable voltage regulators with a very low voltage drop (0.4V typ. at 0.4A T_J = 25°C), low quiescent current and comprehensive on-chip protection.
These devices are protected against load dump and field decay transients, polarity reversal and over heating.
A foldback current limiter protects against load short circuits.
The output voltage is adjustable through an external divider from 1.25V to 20V. The minimum operating input voltage is 5.2V (T_J = 25°C).

These regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.
In battery backup and standby applications the low consumption of these devices extends battery life.

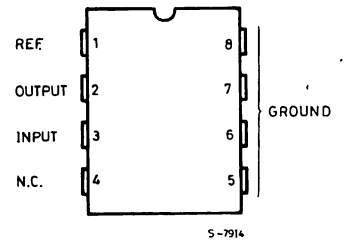
BLOCK DIAGRAM

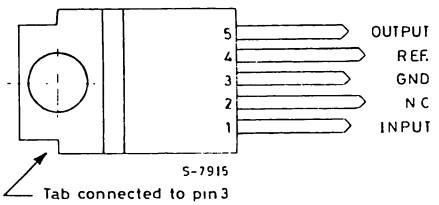


ABSOLUTE MAXIMUM RATINGS

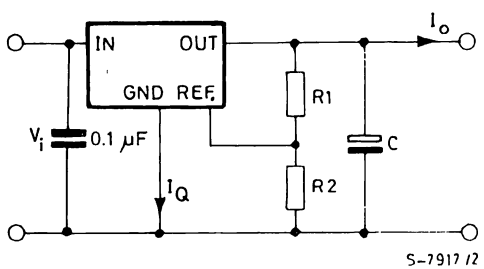
Symbol	Parameter	Value	Unit
V_I	DC Input Voltage	35	
	DC Reverse Input Voltage	- 18	V
	Transient Input Overvoltages :	60	V
	Load Dump :		V
	5ms ≤ t_{rise} ≤ 10ms		
	τ_f Fall Time Constant = 100ms		
	R_{SOURCE} ≥ 0.5Ω		
	Field Decay :	– 60	V
	5ms ≤ t_{fall} ≤ 10ms, R_{SOURCE} ≥ 10Ω		
	τ_r Rise Time Constant = 33ms		
T_J, T_{STG}	Junction and Storage Temperature Range	– 55 to 150	°C

PIN CONNECTIONS (top view)





TEST AND APPLICATION CIRCUIT



$$V_o = \frac{R1+R2}{R2} V_{REF}$$

C = 100µF is required for stability (ESR ≤ 3Ω over T range)
R2 = 6.2KΩ.

THERMAL DATA

			Minidip (4 + 4)	Pentawatt	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	60	°C/W
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	15		°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max		3.5	°C/W

ELECTRICAL CHARACTERISTICS (for V_I = 14.4V, T_j = 25°C, V_o = 5V, C_o = 100µF, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_I	Operating Input Voltage	$V_o \geq 4.5V$ I_o = 400mA	V_o + 0.7		26	V
		$V_{REF} \leq V_o < 4.5V$ I_o = 400mA	5.2		26	V
V_{REF}	Reference Voltage	5.2V < V_I < 26V 5mA ≤ I_o ≤ 400mA (*)	1.20	1.25	1.30	V
ΔV_o	Line Regulation	V_o + 1V < V_I < 26V $V_o \geq 4.5V$ I_o = 5mA		1	10	mV/V
ΔV_o	Load Regulation	5mA ≤ I_o ≤ 400mA (*) $V_o \geq 4.5V$		3	15	mV/V
V_D	Dropout Voltage	I_o = 10mA I_o = 150mA I_o = 400mA		0.05 0.2 0.4	 0.4 0.7	V V V
I_Q	Quiescent Current	I_o = 0mA V_o + 1V < V_I < 26V		0.8	2	mA
		I_o = 400mA (*) V_o + 1V < V_I < 26V		65	90	mA
I_o	Maximal Output Current			800		mA
I_{OSC}	Short Circuit Output Current (*)			350	500	mA

(*) Foldback protection

ELECTRICAL CHARACTERISTICS (for V_I = 14.4V ; – 40 ≤ T_j ≤ 125°C (note 1), V_o = 5V ; C_o = 100µF, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_I	Operating Input Voltage	$V_o \geq 4.5V$ I_o = 400mA	V_o + 0.9		26	V
		$V_{REF} \leq V_o < 4.5V$ I_o = 400mA	5.4		26	V
V_{REF}	Reference Voltage	5.4V < V_I < 26V	1.17	1.25	1.33	V
ΔV_o	Line Regulation	V_o + 1.2V < V_I < 26V $V_o \geq 4.5V$ I_o = 5mA		2	15	mV/V
ΔV_o	Load Regulation	5mA ≤ I_o ≤ 400mA (*) $V_o \geq 4.5V$		5	25	mV/V
V_D	Dropout Voltage	 I_o = 150mA I_o = 400mA		 0.25 0.5	 0.5 0.9	V V V
I_Q	Quiescent Current	I_o = 0mA V_o + 1.2V < V_I < 26V		1.2	3	mA
		I_o = 400mA (*) V_o + 1.2V < V_I < 26V		80	140	mA
I_o	Maximal Output Current			870		mA
I_{OSC}	Short Circuit Output Current (*)			230		mA

(*) Foldback protection

Note : 1 Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges These limits are not used to calculate outgoing quality levels.

Figure 1 : Output Voltage vs. Temperature.

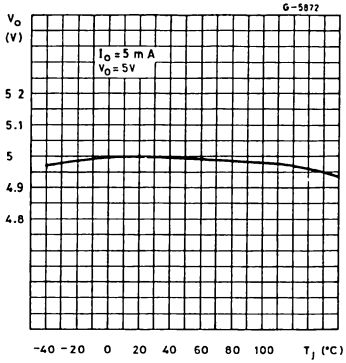


Figure 2 : Foldback Current Limiting.

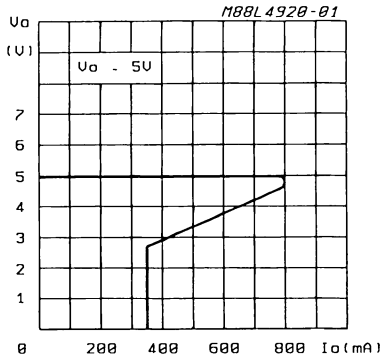
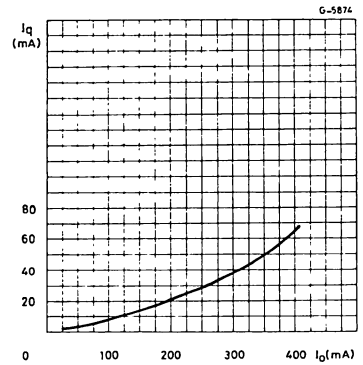


Figure 3 : Quiescent Current vs. Output Current (V_o = 5V).



APPLICATION INFORMATION

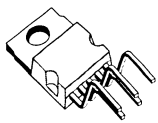
1) The L4920 and L4921 have $V_{REF} \cong 1.25V$. Then the output voltage can be set down to V_{REF} but V_i must be greater than 5.2V (T_j = 25°C).
2) As the regulator reference voltage source works in closed loop, the reference voltage may change in foldback condition.
3) For applications with high V_i, the total power dissipation of the device with respect to the thermal resistance of the package may be limiting . The total power dissipation is :

$$P_{tot} = V_i I_q + (V_i - V_o) I_o$$

A typical curve giving the quiescent current I_q as a function of the output current I_o is shown in fig. 3.

VERY LOW DROP REGULATOR WITH RESET

- VERY LOW DROP (max. 0.9 V at 1 A) OVER FULL OPERATING TEMPERATURE RANGE (– 40 / + 125°C)
- LOW QUIESCENT CURRENT (max 70 mA at 1 A) OVER FULL T RANGE
- PRECISE OUTPUT VOLTAGE (5 V ± 4 %) OVER FULL T RANGE
- POWER ON-OFF INFORMATION WITH SET-TABLE DELAY
- REVERSE BATTERY PROTECTION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN



Pentawatt

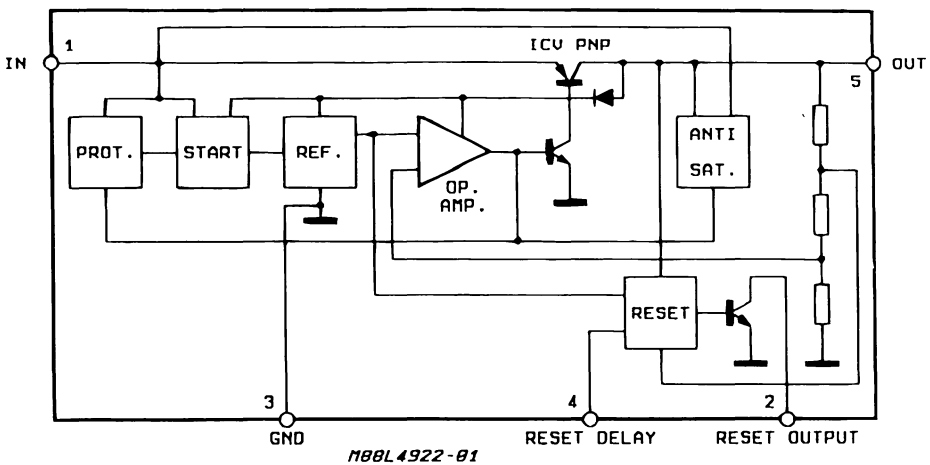
ORDERING NUMBER : L4922

DESCRIPTION

The L4922 is a high current monolithic voltage regulator with very low voltage drop (0.70 V max at 1 A, T_J = 25 °C).

The device is internally protected against load dumps transient of + 60V, reverse polarity, over-heating and output short circuit : thanks toted for the automotive and industrial applications.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

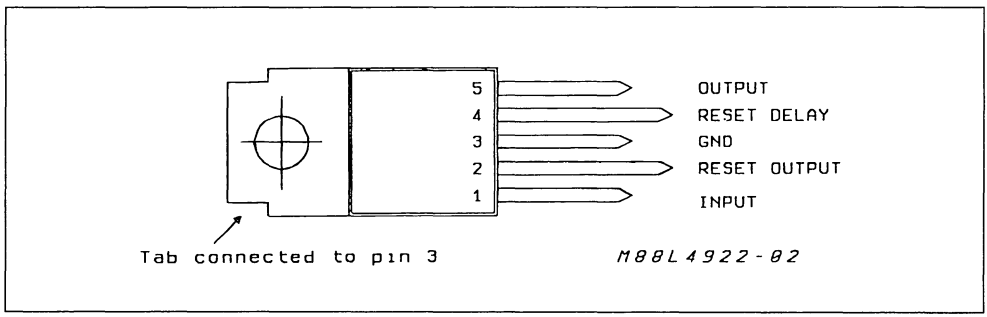
Symbol	Parameter	Value	Unit
V_I	DC Input Voltage	35	V
V_r	DC Reverse Voltage	– 18	V
V_D	Positive Load Dump Protection (t = 300 ms)	60	V
T_J	Junction Temperature Range	– 40 to 150	°C
T_{op}	Operating Temperature Range	– 40 to 125	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

Note: The circuit is ESD protected according to MIL-STD-883C

THERMAL RESISTANCE

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3.5	°C/W

PIN CONNECTION (Top view)



FUNCTIONAL DESCRIPTION

The operating principle of the voltage regulator is based on the reference, the error amplifier, the driver and the power PNP. This stage uses an Isolated Collector Vertical PNP transistor which allows to obtain very low dropout voltage (typ. 450mV) and low quiescent current (I_Q=20mA typically at I_o = 1A).

Thanks to these features the device is particularly suited when the power dissipation must be limited as, for example, in automotive or industrial applications supplied by battery.

The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (Co_{min} = 22µF) to guarantee the global stability of the system.

The antisaturation circuit allows to reduce drastically the current peak which takes place during the start up.

The reset function is LOW active when the output voltage level is lower than the reset threshold voltage V_{RthOFF} (typ. value : V_o – 150mV). When the output voltage is higher than V_{RthON} the reset becomes HIGH after a delay time settable with the external capacitor C_d. Typically t_d = 20ms, C_d = 0.1µF. The reset and delay threshold hysteresis improve the noise immunity allowing to avoid false switchings. The typical reset output waveform is shown in fig. 1.

ELECTRICAL CHARACTERISTICS (V_i = 14. 4V, $-40°C \leq T_J \leq +125°C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_I	Operating Input Voltage	(*) Note 1	6		26	V
V_o	Output Voltage	I_o = 0mA to 1A T_J = 25°C	4.8 4.9		5.2 5.1	V V
ΔV_{Line}	Line Regulation	V_i = 6 to 26V; I_O = 10mA		5	25	mV
SVR	Supply Voltage Rejection	I_o = 700mA f = 120Hz; C_o = 47µF $V_i = 12V_{dc} + 5V_{pp}$		55		dB
ΔV_{LOAD}	Load Regulation	I_o = 10mA to 1A		15	50	mV
$V_i - V_o$	Dropout Voltage	T_J = 25°C, I_O = 1A		0.45	0.70	V
		Over Full T, I_o = 1A			0.90	V
I_q	Quiescent Current	I_o = 10mA I_o = 1A		7 25	12 70	mA mA
I_{SC}	Short Circuit Current			1.8		A
V_R	Rset Output Saturation Voltage	$1.5V < V_O < V_{RT\ (off)}$, I_R = 1.6mA $3V < V_O < V_{RT\ (off)}$, I_R = 8mA			0.40 0.40	V V
$V_{RT\ peak}$	Power On-Off Reset out Peak Voltage	1KΩ Reset Pull-up to V_O		0.65	1.0	V
I_R	Reset Output Leakage Current (high level)	V_o in Regul. V_R = 5V			50	µA
t_D	Reset Pulse Delay Time	C_D = 100nF		20		ms
V_{RthOFF}	Power OFF V_o Threshold	V_o @ Reset out H to L Transition; T_J = 25°C $-40°C \leq T_J \leq +125°C$	4.75 4.70	V_o−0.15		V V
I_{C6}	Delay Capacitor Charging Current (current generator)	V_4 = 3V		20		µA
V_{RthON}	Power ON V_o Threshold	V_o @ Reset out L to H Transition		V_{rthOFF} + 0.03V	V_o − 0.04V	V
V_4	Delay Comparator Threshold	Reset out = "1" H to L Transition	3.2		3.8	V
		Reset out = "0" L to H Transition	3.7	4	4.4	V
V_{6H}	Delay Comparator Hysteresis			500		mV

(*) Note 1 : The device is not operating within the range : 26 V < V_i < 37 V.

EXTERNAL COMPENSATION

Since the purpose of a voltage regulator is to supply a fixed output voltage in spite of supply and load variations, the open loop gain of the regulator must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shifts due to other poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be the capacitor used to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequency too low to be compensated by a capacitor wich can be integrated. An external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The parassitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is 47µF.

Figure 1 : Typical Reset Output Waveform.

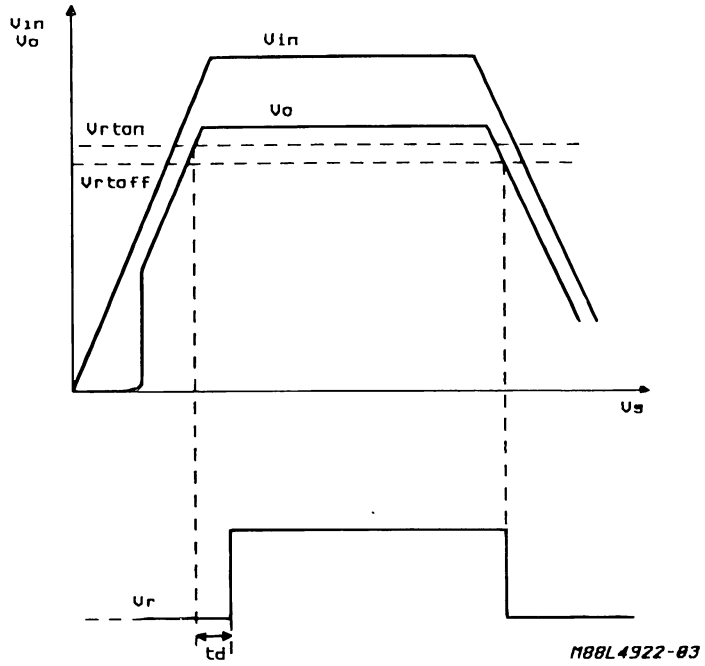
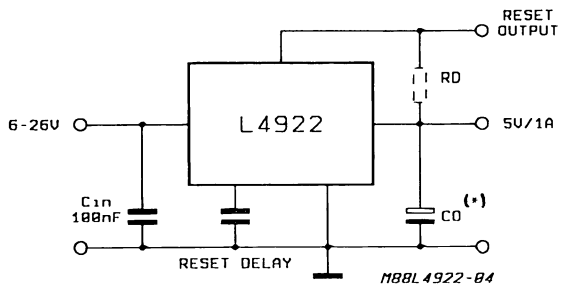


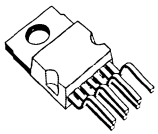
Figure 2 : Typical Application Circuit.



(*) RECOMMENDED VALUE : C_O = 47 µF, ESR < 10 ohm, (I_{out} > 10 mA) OVER FULL T_{range}.

5V–1A VERY LOW DROP REGULATOR WITH RESET AND INHIBIT

- VERY LOW DROP (max. 0.9V at 1A) OVER FULL OPERATING TEMPERATURE RANGE (– 40 / + 125 °C)
- LOW QUIESCENT CURRENT (max 70 mA at 1 A) OVER FULL T RANGE
- PRECISE OUTPUT VOLTAGE (5V ± 4%) OVER FULL T RANGE
- POWER ON-OFF INFORMATION WITH SETTABLE DELAY
- INHIBIT FOR REMOTE ON-OFF COMMAND (active high)
- LOAD STANDBY CURRENT
- LOAD DUMP AND REVERSE BATTERY PROTECTION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN



Heptawatt

ORDERING NUMBER : L4923

DESCRIPTION

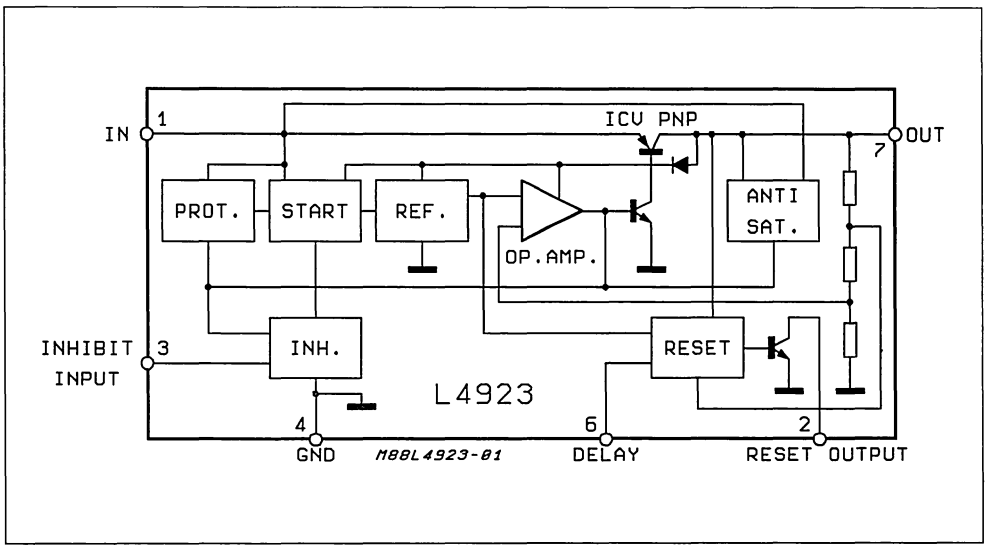
The L4923 is a high current monolithic voltage regulator with very low voltage drop (0.70 V max at 1 A, T_J = 25 °C).

The device is internally protected against load dumps transient of + 60 V, input overvoltage, reverse polarity, overheating and output short circuit : thanks to these features the L4923 is very suited for the automotive and industrial applications.

The reset function is very useful for power off and power on information when supplying a microprocessor.

The inhibit function reduces drastically the consumption when no load current is required : typically the standby current value is 300 µA.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	35	V
V_r	DC Reverse Voltage	– 18	V
V_D	Positive Load Dump Protection (t = 300 ms)	60	V
T_J	Junction Temperature Range	– 40 to 150	°C
T_{op}	Operating Temperature Range	– 40 to 125	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

Note: The circuit is ESD protected according to MIL-STD-883C

THERMAL RESISTANCE

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W

PIN CONNECTION

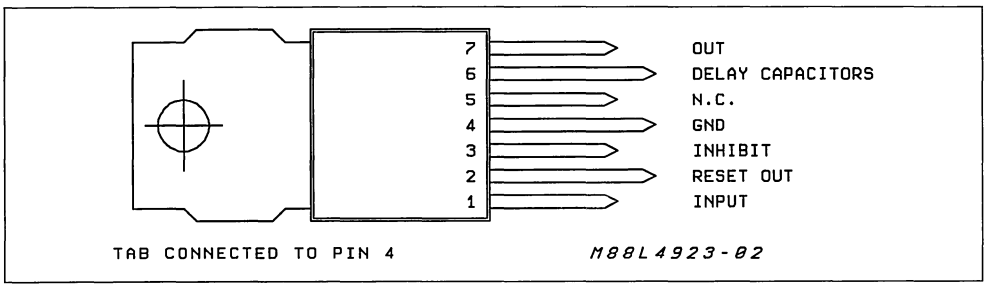
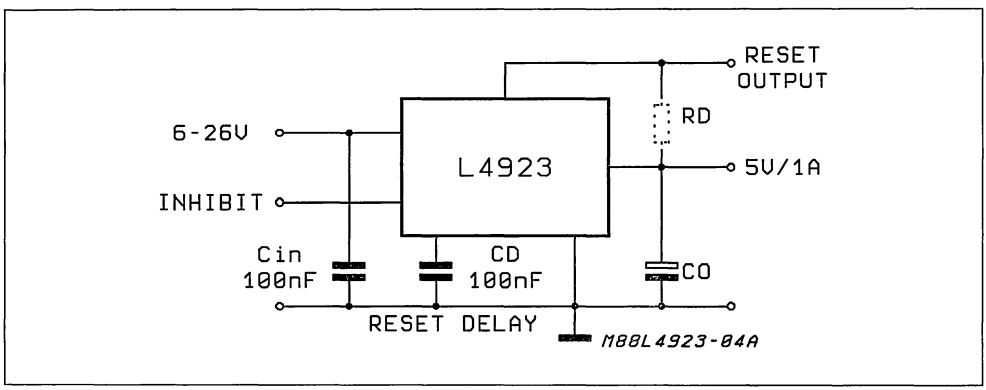


Figure 1 : Application Circuit.



(*) RECOMMENDED VALUE : C_0 = 47 µF, ESR < 10 Ω, (I_{out} > 10 mA) OVER FULL T_{range}.

ELECTRICAL CHARACTERISTICS (V_I = 14. 4V, $-40°C \leq T_J \leq +125°C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_I	Operating Input Voltage	(*) Note 1	6		26	V
V_o	Output Voltage	I_o = 0mA to 1A T_J = 25°C	4.8 4.9		5.2 5.1	V V
ΔV_{Line}	Line Regulation	V_I = 6 to 26V; I_O = 10mA		5	25	mV
SVR	Supply Voltage Rejection	I_o = 700mA f = 120Hz; C_o = 47µF $V_I = 12V_{dc} + 5V_{pp}$		55		dB
ΔV_{LOAD}	Load Regulation	I_o = 10mA to 1A		15	50	mV
$V_I - V_o$	Dropout Voltage	T_J = 25°C, I_O = 1A		0.45	0.70	V
		Over Full T, I_o = 1A			0.90	V
I_q	Quiescent Current	I_o = 10mA I_o = 1A Active High Inhibit		7 25 0.30	12 70 0.65	mA mA mA
I_{SC}	Short Circuit Current			1.8		A
SVR	Supply Volt. Rej.	I_o = 350mA ; f = 120Hz C_o = 100µF ; $V_I = 12V \pm 5V_{pp}$	50	60		dB
V_R	Rset Output Saturation Voltage	$1.5V < V_O < V_{RT\ (off)}$, I_R = 1.6mA $3V < V_O < V_{RT\ (off)}$, I_R = 8mA			0.40 0.40	V V
$V_{RT\ peak}$	Power On-Off Reset out Peak Voltage	1KΩ Reset Pull-up to V_O		0.65	1.0	V
I_R	Reset Output Leakage Current (high level)	V_o in Regul. V_R = 5V			50	µA
t_D	Reset Pulse Delay Time	C_D = 100nF		20		ms
V_{RthOFF}	Power OFF V_o Threshold	V_o @ Reset out H to L Transition; T_J = 25°C $-40°C \leq T_J \leq +125°C$	4.75 4.7	V_o−0.15		V V
I_{C6}	Delay Capacitor Charging Current (current generator)	V_6 = 3V		20		µA
V_{RthON}	Power ON V_o Threshold	V_o @ Reset out L to H Transition		V_{rthOFF} + 0.03V	V_o − 0.04V	V
V_6	Delay Comparator Threshold	Reset out = "1" H to L Transition	3.2		3.8	V
		Reset out = "0" L to H Transition	3.7	4	4.4	V
V_{6H}	Delay Comparator Hysteresis			500		mV
V_{InhL}	Low Inhibit Voltage				0.5	V
V_{InhH}	High Inhibit Voltage		2.0			V
I_{InhL}	Low Level Inhibit Current	$V_{Inh\ L}$ = 0.4V	− 40	− 10		µA
I_{InhH}	High Level Inhibit Current	$V_{Inh\ H}$ = 2.4V		6	20	µA

(*) Note 1 : The device is not operating within the range . 26 V < V_I < 37 V.

EXTERNAL COMPENSATION

Since the purpose of a voltage regulator is to supply a fixed output voltage in spite of supply and load variations, the open loop gain of the regulator must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shifts due to other poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be the capacitor used to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequency too low to be compensated by a capacitor wich can be integrated. An external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The parassitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is 47µF.

FUNCTIONAL DESCRIPTION

The operating principle of the voltage regulator is based on the reference, the error amplifier, the driver and the power PNP. This stage uses an Isolated Collector Vertical PNP transistor which allows to obtain very low dropout voltage (typ. 450 mV) and low quiescent current (I_Q = 20 mA typically at I_O = 1 A).

Thanks to these features the device is particularly suited when the power dissipation must be limited as, for example, in automotive or industrial applications supplied by battery.

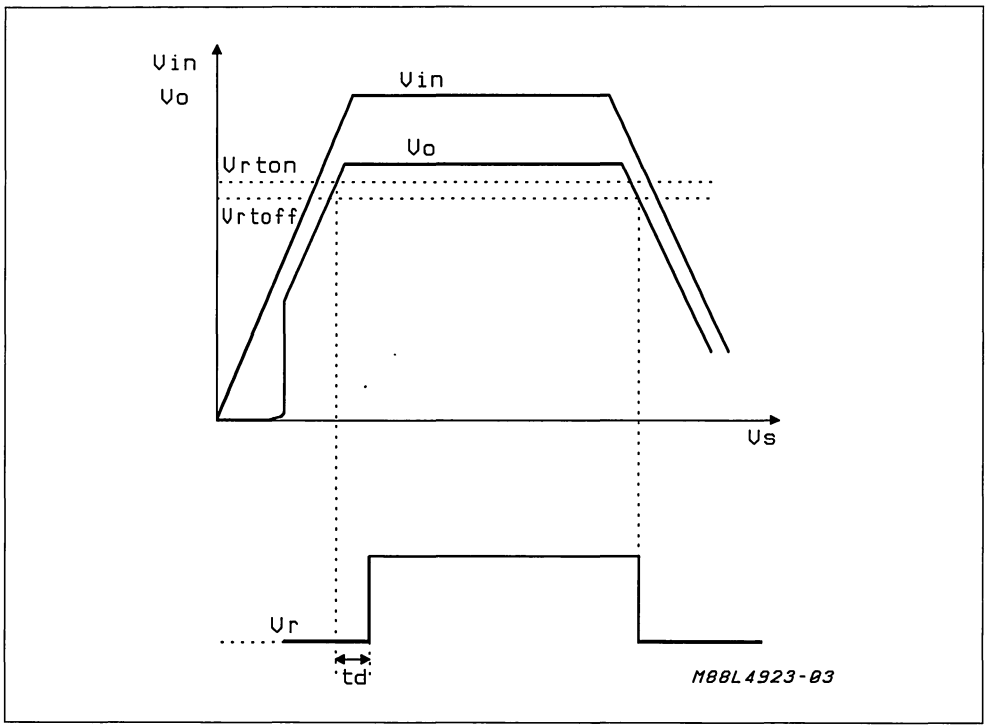
The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (C_{Omin} = 22 µF) to guarantee the global stability of the system.

The antisaturation circuit allows to reduce drastically the current peak which takes place during the start up.

The reset function is LOW active when the output voltage level is lower than the reset threshold voltage V_{Rth} (typ. value : V_O - 150 mV). When the output voltage is higher than V_{Rth} the reset becomes HIGH after a delay time settable with the external capacitor C_d. Typically t_d = 20 ms, C_d = 0.1 µF. The reset threshold hysteresis improves the noise immunity allowing to avoid false switchings. The typical reset output waveform is shown in fig. 2.

The inhibit circuit accepts standard TTL input levels : this block switches off the voltage regulator when the input signal is HIGH and switches on it when the input signal is LOW. Thanks to inhibit function the consumption is drastically reduced (650 µA max) when no load current is required.

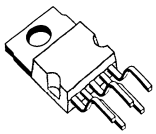
Figure 2 : Typical Reset Output Waveform.



VERY LOW DROP VOLTAGE REGULATOR

PRODUCT PREVIEW

- OPERATING DC SUPPLY VOLTAGE RANGE 5V TO 28V
- TRANSIENT SUPPLY VOLTAGE UP TO 40V
- EXTREMELY LOW QUIESCENT CURRENT IN STANDBY MODE
- HIGH PRECISION STANDBY OUTPUT VOLTAGE: 5V±1%
- OUTPUT CURRENT CAPABILITY UP TO 500mA
- VERY LOW DROPOUT VOLTAGE LESS THAN 0.6V
- RESET CIRCUIT SENSING THE OUTPUT VOLTAGE
- PROGRAMMABLE RESET PULSE DELAY WITH EXTERNAL CAPACITOR
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS



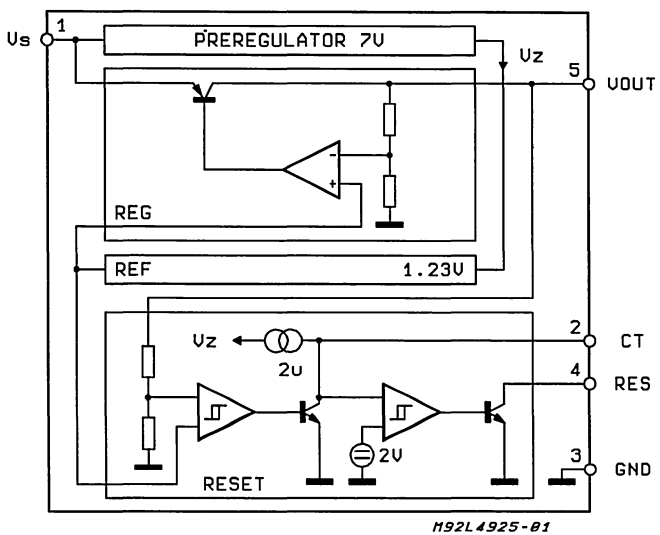
Pentawatt

ORDERING NUMBER: L4925 .

DESCRIPTION

The L4925 is a monolithic integrated 5V voltage regulator with a very low dropout output and additional functions such as power-on reset and programmable reset delay time. It is designed for supplying microcomputer controlled systems especially in automotive applications.

BLOCK DIAGRAM



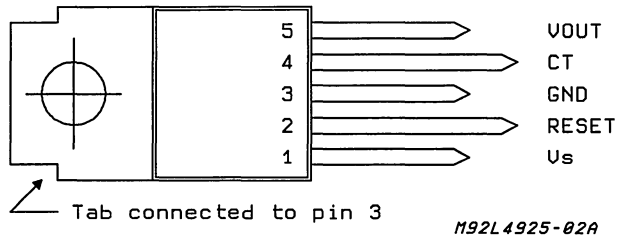
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{SDC}	DC Operating Supply Voltage	28	V
V_{STR}	Transient Supply Voltage (t < 1s)	40	V
I_O	Output Current	internally limited	
V_O	Output Voltage	20	V
V_{RES}	Output Voltage	20	V
I_{RES}	Output Current	5	mA
T_{stg}	Storage Temperature	-55 to 150	°C
T_j	Operating Junction Temperature	-40 to 150	°C
$T_{j\text{-}SD}$	Thermal Shutdown-Junction Temperature	165	°C

NOTE:

The circuit is ESD protected according to MIL-STD-883C. According to ISO/DIS 7637 the transients must be clamped with external circuitry (see Application Circuit).

CONNECTION DIAGRAM



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	max.	60	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction to case	max.	3.5	°C/W

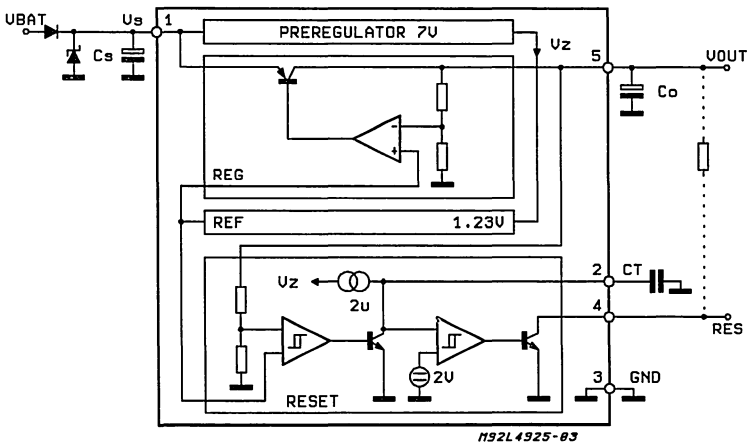
ELECTRICAL CHARACTERISTICS (V_S =14V T_j =–40 to 125°C unless otherwise specified;

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_j = 25 °C; I_O = 1mA	4.95	5	5.05	V
V_O	Output Voltage	V_I = 6 to 28V; I_O = 1 to 500mA	4.90	5	5.10	V
V_O	Output Voltage	V_I = 35V; T <1s; I_O = 1 to 500mA			5.50	V
V_{DP}	Dropout Voltage	I_O = 100mA I_O = 500mA		0.2 0.3	0.3 0.6	V V
V_{IO}	Input to Output Voltage Difference in Undervoltage Condition	V_I = 4V; I_O = 100mA			0.5	V
V_{OL}	Line Regulation	V_I = 6 to 28V; I_O = 1 to 1mA			10	mV
V_{OLO}	Load Regulation	I_O = 1 to 500mA			50	mV
I_{LIM}	Current Limit	V_O = 4.5V, V_O = 0; Foldback characteristic	550	1000 250	1500	mA mA
I_{QSE}	Quiescent Current	I_O = 0.3mA		150	250	µA
I_Q	Quiescent Current	I_O = 500mA			20	mA

RESET

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{RT}	Reset Threshold Voltage			V_O - 0.5		V
V_{RTH}	Reset Threshold		50	100	200	mV
t_{RD}	Reset Pulse Delay	C_T = 100nF; $t_R \geq$ 100µs	60	100	140	ms
t_{RR}	Reset Reaction Time	C_T = 100nF;		5	30	µs
V_{RL}	Reset Output LOW Voltage	R_{RES} = 10KΩ to V_O; V_S =≥ 3V			0.4	V
I_{RH}	Reset Output HIGH Leakage Current	V_{RES} = 5V			1	µA
V_{CTth}	Delay Comparator Threshold			2		V
$V_{CTth\ hy}$	Delay Comparator Threshold Hysteresis			100		mV

APPLICATION CIRCUIT DIAGRAM



For stability: $C_S \geq$ 1µF; $C_O \geq$ 10µF;ESR < 10Ω at 10 KHz
Recommended for application: $C_S = C_O$ = 10µF to 100µF

APPLICATIN NOTE

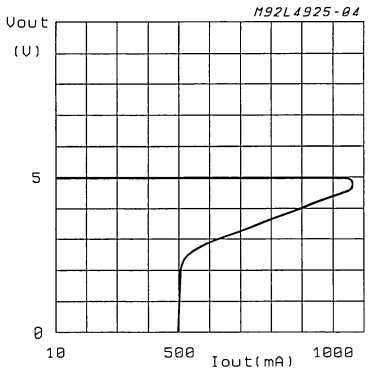
SUPPLY VOLTAGE TRANSIENTS

High supply voltage transients can cause a reset output signal disturbation.

For supply voltage greater than 8V the circuit shows a high immunity of the reset output against supply transients of more than 100V/µs.

For supply voltage lower than 8V, supply transients of more than 0.4V/µs. can cause a reset signal disturbation.

Foldback Characteristics Of Vo



FUNCTIONAL DESCRIPTION

The L4925 is a monolithic integrated voltage regulator, based on the STM modular voltage regulator approach. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications.

Nevetrheless, it is suitable also in other applications where the present functions are required. The modular approach of this device allows to get easily also other features and functions when required.

VOLTAGE REGULATOR

The voltage regulator uses an Isolated Collector Vertical PNP transistor as a regulating element. With this structure very low dropout voltage at currents up to 500mA is obtained.

The dropout operation of the standby regulator is maintained down to 3V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 35V. With this feature no functional interruption due to overvoltage pulses is generated.

The typical curve showing the standby output voltage as a function of the input supply voltage is shown in fig. 1.

The current consumption of the device (quiescent current) is less than 250µA.

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled.

The quiescent current as a function of the supply input voltage is shown in fig. 2.

Figure 1: Output Voltage vs. Input Voltage

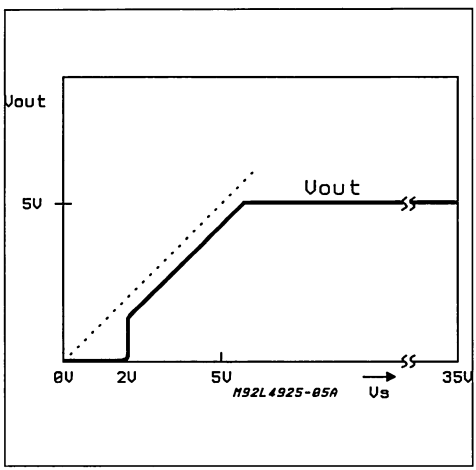
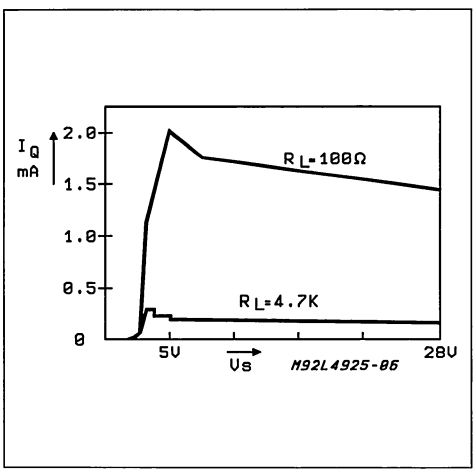


Figure 2: Quiescent Current vs. Supply Voltage



RESET CIRCUIT

The block circuit diagram of the reset circuit is shown in Figure 3. The reset circuit supervises the output voltage. The reset threshold of 4.5V is defined with the internal reference voltage and standby output divider.

The reset pulse delay time t_{RD}, is defined with the charge time of an external capacitor C_T:

$$t_{RD}=\frac{C_T \times 2V}{2\mu A}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor C_T and it is proportional to the value of C_T.

The reaction time of the reset circuit increases the noise immunity.Standby output voltage drops below the reset threshold only a bit longer than the reaction time results in a shorter reset delay time. The nominal reset delay time will be generated for standby output voltage drops longer than approximately 50µs. The typical reset output waveforms are shown in Figure 4.

Figure 3

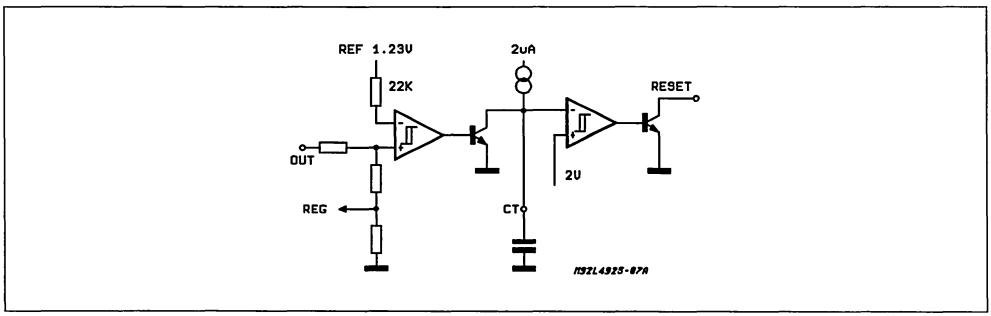
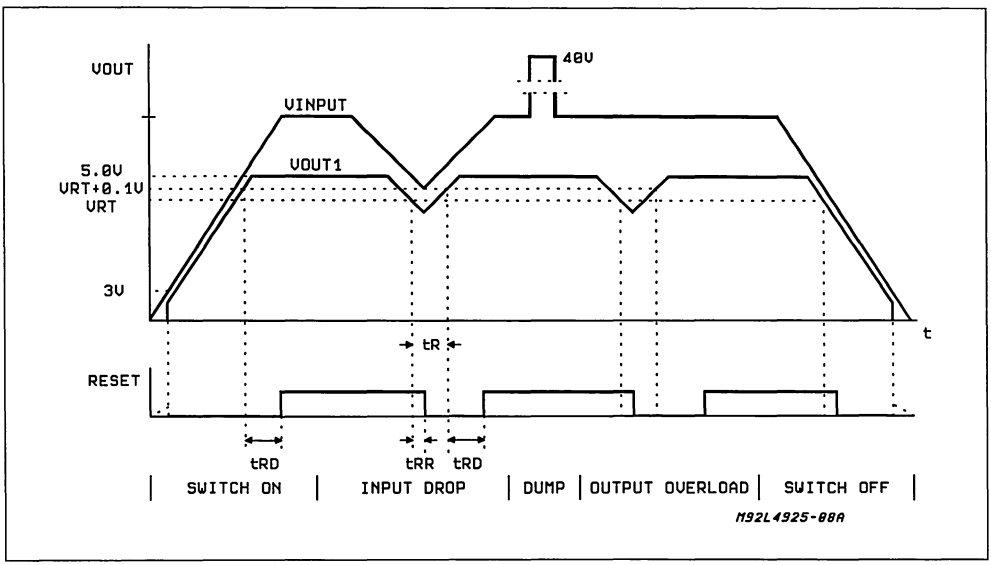


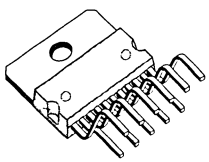
Figure 4



DUAL MULTIFUNCTION VOLTAGE REGULATOR

ADVANCE DATA

- STANDBY OUTPUT VOLTAGE PRECISION 5V ± 2%
- OUTPUT 2 TRACKED TO THE STANDBY OUTPUT
- OUTPUT 2 DISABLE FUNCTION FOR STANDBY MODE
- VERY LOW QUIESCENT CURRENT, LESS THAN 250µA, IN STANDBY MODE
- OUTPUT 2 VOLTAGE SETTABLE FROM 5 TO 20V
- OUTPUT CURRENTS : I_{O1} = 50mA, I_{O2} = 500mA
- VERY LOW DROPOUT (max 0.4V/0.6V)
- OPERATING TRANSIENT SUPPLY VOLTAGE UP TO 40V
- POWER-ON RESET CIRCUIT SENSING THE STANDBY OUTPUT VOLTAGE
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- EARLY WARNING OUTPUT FOR SUPPLY UNDERVOLTAGE
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS



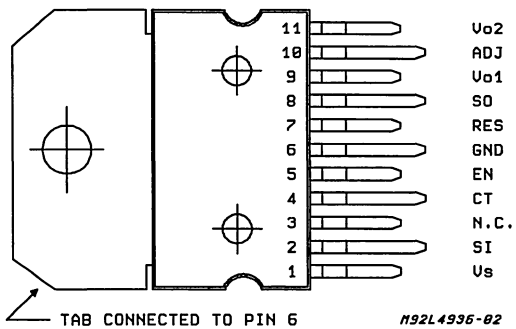
Multiwatt 11 **Powerdip (12+2+2)**

ORDERING NUMBERS: L4936 (Multiwatt–11)
L4938 (Powerdip 12+2+2)

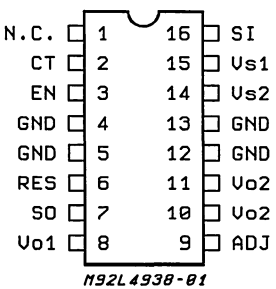
DESCRIPTION

The L4936/38 are monolithic integrated dual voltage regulators with two very low dropout outputs and additional functions such as power-on reset and input voltage sense. They are designed for supplying microcomputer controlled systems specially in automotive applications.

PIN CONNECTIONS (top view)

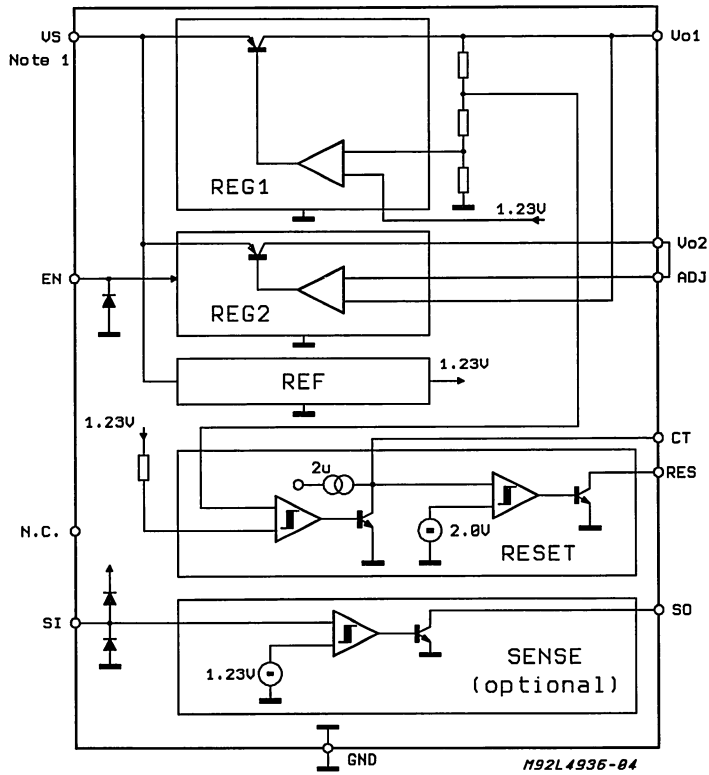


(Multiwatt–11)



(Powerdip 12+2+2)

BLOCK DIAGRAM



Note 1: For L4938, Vs is splitted as follow:
Vs1-PIN15-Output 1 supply
Vs2-PIN14-Output 2 supply

THERMAL DATA

$R_{th\ j\text{-}c}$	Thermal Resistance Junction - case (MW11)	Max	3	°C/W
$R_{th\ J\text{-}A}$	Thermal Resistance Junction Ambient (power DIP 12 + 2 + 2)		60	°C/W

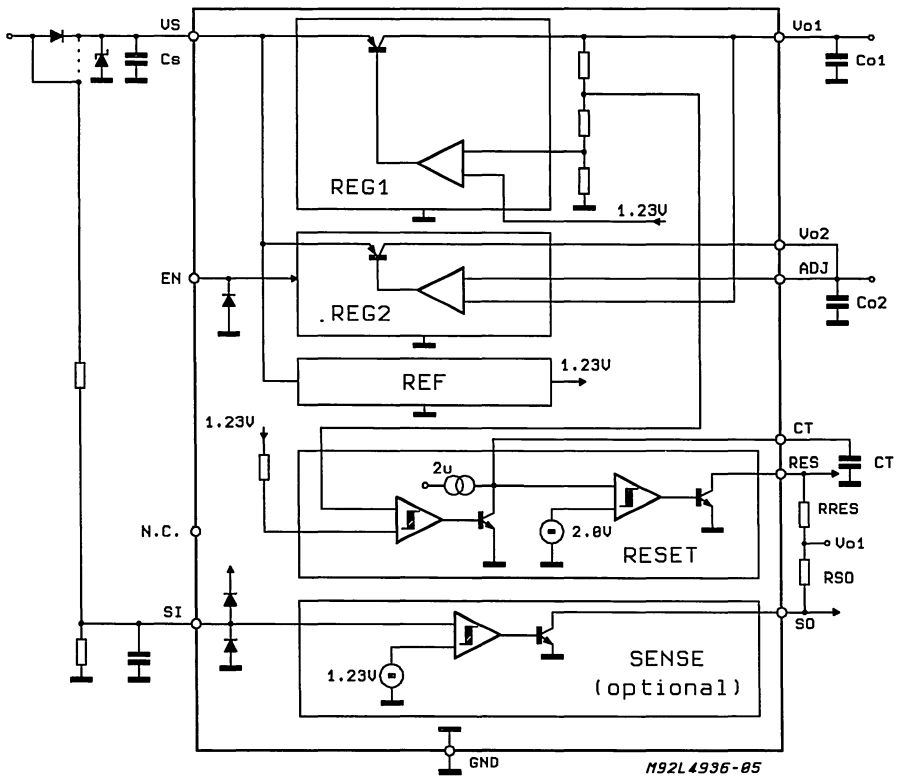
Note 1: For L4938, V_S is splitted as follow:
V_{S1} = Pin 15 = Output 1 Supply
V_{S2} = Pin 14 = Output 2 Supply

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	28	V
	Transient Supply Voltage (T < 1S)	40	V
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C
I_{SI}	Sense Input Current (V_{SI} < – 0.3V or V_{SI} > V_S)	± 1	mA
I_{EN}	Enable Input Current (V_{EN} < – 0.3V)	– 1	mA
V_{EN}	Enable Input Voltage	V_S	V
V_{RES}, V_{SO}	Reset and Sense Output Voltage	20	V
I_{RES}, I_{SO}	Reset and Sense Output Current	5	mA
P_D	Power Dissipation (T_A = 80°C, $R_{th\ heatsink}$ = 11°C/W) MW11 Power DIP 12 + 2 + 2	5 1166	W mW

Note : The circuit is ESD protected according to MIL–STD–883C.

APPLICATION CIRCUIT



C_S ≥ 1µF ; C_{O1} ≥ 6µF ; C_{O2} ≥ 10µF, ESR < 10Ω at 10KHz

ELECTRICAL CHARACTERISTICS (V_S = 14V ; – 40°C ≤ T_J ≤ 125°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage				25	V
V_{O1}	Standby Output Voltage	T_J = 25°C ; I_{O1} = 1mA	4.95	5.00	5.05	V
V_{O1}	Standby Output Voltage	6V ≤ V_S ≤ 25V 1mA ≤ I_{O1} ≤ 50mA	4.90	5.00	5.10	V
V_{O2} - V_{O1}	Output Voltage 2 Tracking Error (note 1)	6V ≤ V_S≤ 25V 5mA ≤ I_{O2} ≤ 500mA Enable = LOW	– 25		+ 25	mV
I_{ADJ}	ADJ Input Current	I_{O1} = 1mA ; I_{O2} = 5mA	– 1	0.1	1	µA
V_{DP1}	Dropout Voltage 1	I_{O1} = 10mA I_{O1} = 50mA		0.1 0.2	0.25 0.4	V V
V_{IO1}	Input to Output Voltage Difference in Undervoltage Condition	V_S = 4V, I_{O1} = 35mA			0.4	V
V_{DP2}	Dropout Voltage 2	I_{O2} = 100mA I_{O2} = 500mA		0.2 0.3	0.3 0.6	V V
V_{IO2}	Input to Output Voltage Difference in Undervoltage Condition	V_S = 4.6V,I_{O2} = 350mA			0.6	V
$V_{OL\,1\,2}$	Line Regulation	6V ≤ V_S ≤ 25V I_{O1} = 1mA, I_{O2} = 5mA			20	mV
V_{OLO1}	Load Regulation 1	1mA ≤ I_{O1} ≤ 50mA			25	mV
V_{OLO2}	Load Regulation 2	5mA ≤ I_{O2} ≤ 500mA			50	mV
I_{LIM1}	Current Limit 1	V_{O1} = 4.5V V_{O1} = 0V (note 2)	55 25	100 50	200 100	mA mA
I_{LIM2}	Current Limit 2	V_{O2} = 0V	550	1000	1500	mA
I_{QSB}	Quiescent Current Standby Mode (output 2 disabled)	I_{O1} = 0.3mA ; T_J < 100°C V_{EN} ≥ 2.4V Vs = 14V Vs = 3.5V		 150 300	 250 800	 µA µA
I_Q	Quiescent Current	I_{O1} = 50mA I_{O2} = 500mA			30	mA

ENABLE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ENL}	Enable Input LOW Voltage (output 2 active)		– 0.3		1.5	V
V_{ENH}	Enable Input HIGH Voltage		2.4		7	V
V_{ENhyst}	Enable Hysteresis		30	75	200	mV
I_{EN}	Enable Input Current	0V < V_{EN} < 1.2V 2.5V< V_{EN} < 7V	– 10 – 1	– 1.5 0	– 0.5 + 1	µA µA

RESET

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Rt}	Reset Low Threshold Voltage	Vs = 14V	V_{o1}-0.4	4.7	V_{o1}-0.1	V
V_{Rth}	Reset Threshold Hysteresis		50	100	200	mV
t_{RD}	Reset Pulse Delay	C_T = 100nF ; t_R > 100µs	55	100	180	ms
t_{RR}	Reset Reaction Time	C_T = 100nF	1	10	50	µs
V_{RL}	Reset Output LOW Voltage	R_{RES} = 10KΩ to V_{O1} V_S = 3V			0.4	V
I_{LRES}	Reset Output HIGH Leakage	V_{RES} = 5V			1	µA
V_{CTth}	Delay Comparator Threshold			2.0		V
$V_{CTth, hyst}$	Delay Comparator Threshold Hysteresis			100		mV

SENSE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SIth}	Sense Threshold Voltage		1.16	1.23	1.35	V
$V_{SIth,hyst}$	Sense Threshold Hysteresis		20	100	200	mV
V_{SOL}	Sense Output LOW Voltage	V_{SI} = 0.8V ; $V_S \geq$ 3V R_{SO} = 10KΩ to V_{O1}			0.4	V
I_{LSO}	Sense Output Leakage	V_{SO} = 5V ; $V_{SI} \geq$ 1.5V			1	µA
I_{SI}	Sense Input Current		− 1	0.1	1	µA

Note : 1 : V_{O2} connected to ADJ V_{O2} can be set to higher values by inserting an external resistor divider.
2 · Foldback characteristic

FUNCTIONAL DESCRIPTION

The L4936/8 are based on the SGS-THOMSON Microelectronics modular voltage regulator approach. Several out-standing features and auxiliary functions are provided to meet the requirements of supplying the microprocessor systems used in automotive applications.

Furthermore the device is suitable also in other applications requiring two stabilized voltages.

The modular approach allows other features and functions to be realized easily when required.

STANDBY REGULATOR

The standby regulator uses an Isolated Collector Vertical PNP transistor as the regulating element. This structure allows a very low dropout voltage at currents up to 50mA. The dropout operation of the standby regulator is maintained down to 2V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. This feature avoids functional interruptions which could be generated by overvoltage pulses.

The typical curve of the standby output voltage as a function of the input supply voltage is shown in fig. 1.

The current consumption of the device (quiescent current) is less than 250µA when output 2 is disabled (standby mode). The dropout voltage is controlled to reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region.

The quiescent current is shown in fig. 2 as a function of the supply input voltage 2.

OUTPUT 2 VOLTAGE

The output 2 regulator uses the same output structure as the standby regulator, but rated for an output current of 500mA.

The output 2 regulator works in tracking mode with the standby output voltage as a reference voltage when the output 2 programming pin ADJ is connected to V_{O2}. By connecting a resistor divider R_1, R_2 to the pin ADJ as shown in fig. 3, the output voltage 2 can be programmed to the value :

$$V_{O2} = V_{O1} (1 + R_1/R_2)$$

The output 2 regulator can be switched off via the Enable input.

Figure 1 : Output Voltage vs. Input Voltage.

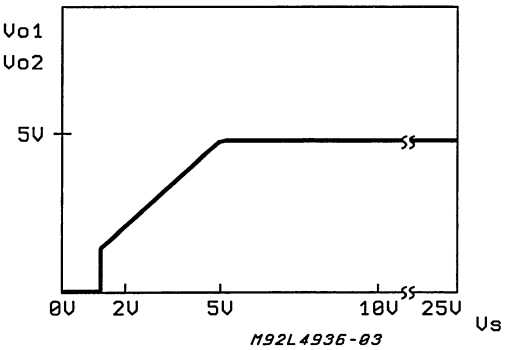


Figure 2 : Quiescent Current vs. Supply Voltage.

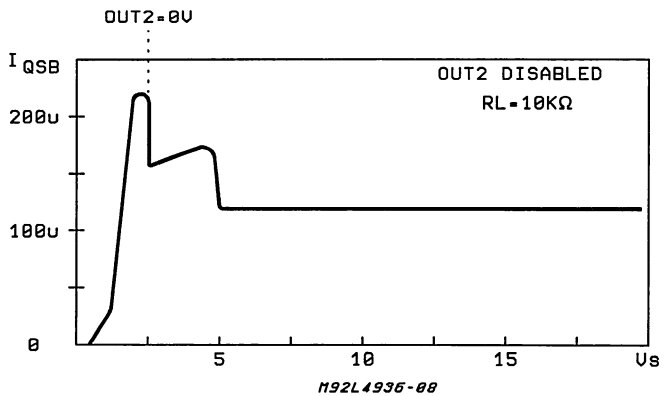
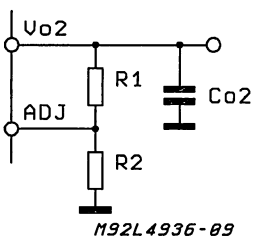


Figure 3 : Programmable Output 2 Voltage with External Resistors.



RESET CIRCUIT

The block circuit diagram of the reset circuit is shown in fig. 4. The reset circuit supervises the standby output voltage. The reset threshold of 4.7V is defined by the internal reference voltage and the standby output divider.

The reset pulse delay time t_{RD}, is defined by the charge time of an external capacitor C_T :

$$t_{RD} = \frac{C_T \times 2V}{2\mu A}$$

The reaction time of the reset circuit depends on the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T.

The reaction time of the reset circuit increases the noise immunity. In fact, if the standby output voltage drops below the reset threshold for a time shorter than the reaction time t_{RR}, no reset output variation occurs. The nominal reset delay is generated for standby output voltage drops longer than the time necessary for the complete discharging of the capacitor C_T. This time is typically equal to 50µs if C_T = 100nF. The typical reset output waveforms are shown in fig. 5.

SENSE COMPARATOR

This circuit compares an input signal with an internal voltage reference of typically 1.23V. The use of an external voltage divider makes the comparator very flexible in the application. This function can be used to supervise the input voltage - either before or after the protection diode - and to give additional information to the microprocessor such as low voltage warnings.

Figure 4 : Block Diagram of the Reset Circuit.

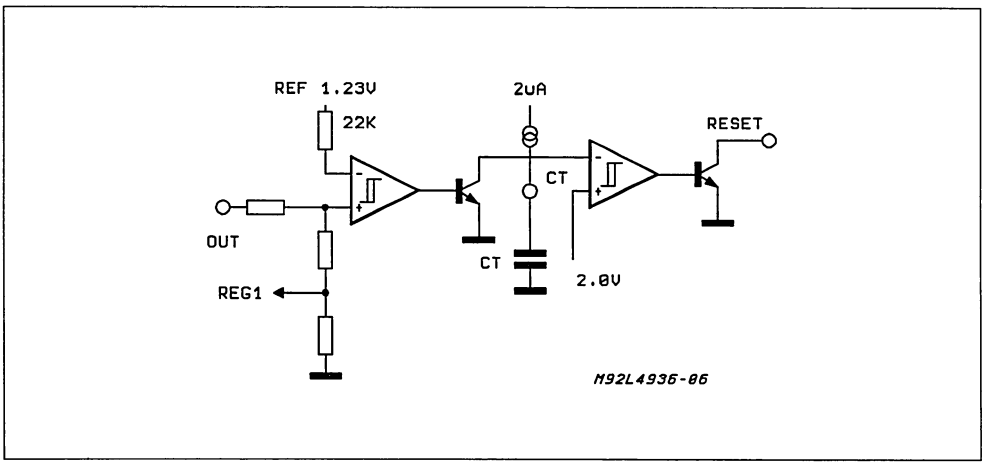
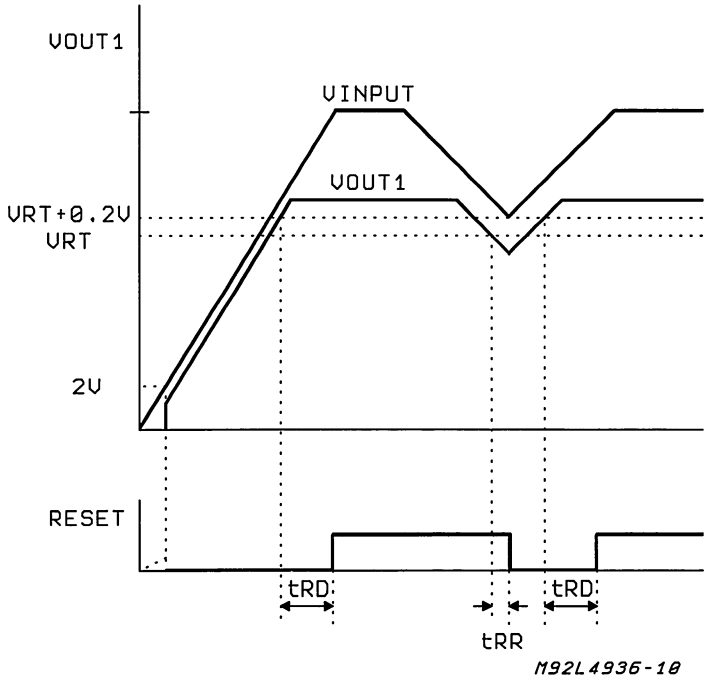


Figure 5 : Typical Reset Output Waveforms.



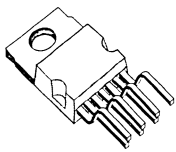
SGS-THOMSON MICROELECTRONICS

L4937

DUAL MULTIFUNCTION VOLTAGE REGULATOR

ADVANCE DATA

- STANDBY OUTPUT VOLTAGE PRECISION 5V ± 2%
- OUTPUT 2 TRACKED TO THE STANDBY OUTPUT
- OUTPUT 2 DISABLE FUNCTION FOR STANDBY MODE
- VERY LOW QUIESCENT CURRENT, LESS THAN 250µA, IN STANDBY MODE
- OUTPUT CURRENTS : I_{O1} = 50mA, I_{O2} = 500mA
- VERY LOW DROPOUT (max 0.4V/0.6V)
- OPERATING TRANSIENT SUPPLY VOLTAGE UP TO 40V
- POWER-ON RESET CIRCUIT SENSING THE STANDBY OUTPUT VOLTAGE
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS



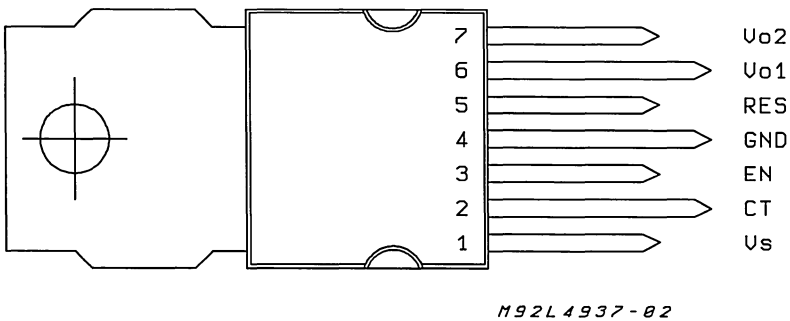
Heptawatt

ORDERING NUMBERS : L4937

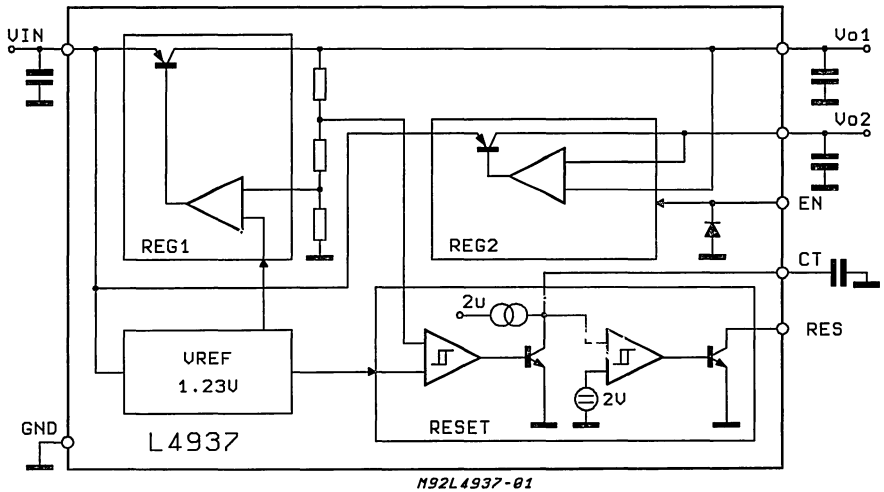
DESCRIPTION

The L4937 is a monolithic integrated dual voltage regulators with two very low dropout outputs and additional functions such as power-on reset and input voltage sense. It is designed for supplying microcomputer controlled systems specially in automotive applications.

PIN CONNECTION (top view)



BLOCK DIAGRAM



THERMAL DATA

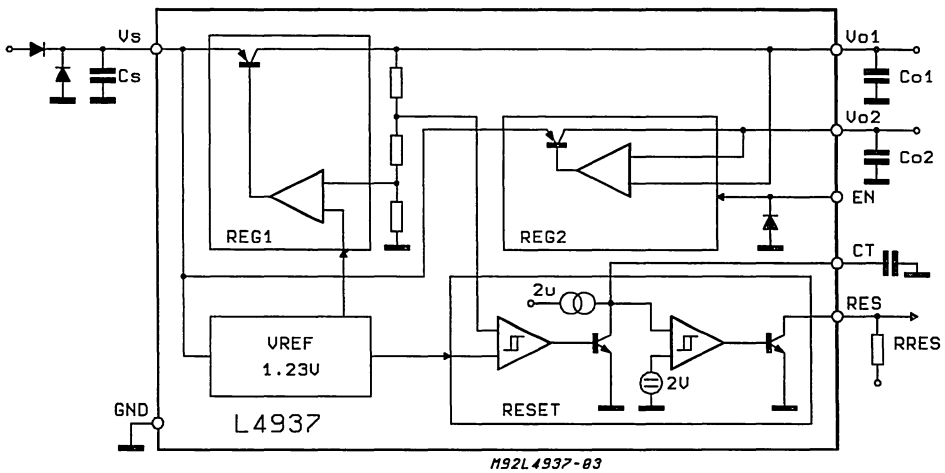
$R_{th\ j\text{-}c}$	Thermal Resistance Junction-case	Max	3	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	D.C. Supply Voltage Transient Supply Voltage (T < 1s)	28 40	V V
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C
I_{EN}	Enable Input Current (V_{EN} < – 0.3V)	– 1	mA
V_{EN}	Enable Input Voltage	V_s	V
V_{RES}	Reset Output Voltage	20	V
I_{RES}	Reset Output Current	5	mA
P_D	Power Dissipation (T_A = 80°C, $R_{th\ heatsink}$ = 9°C/W)	5	W

Note : The circuit is ESD protected according to MIL–STD–883C

APPLICATION CIRCUIT



C_S ≥ 1µF ; C_{01} ≥ 6µF ; C_{02} ≥ 10µF, ESR < 10Ω at 10KHz

ELECTRICAL CHARACTERISTICS (V_S = 14V ; – 40°C ≤ T_j ≤ 125°C unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage				25	V
V_{O1}	Standby Output Voltage	T_j = 25°C ; I_{O1} = 1mA	4.95	5.00	5.05	V
V_{O1}	Standby Output Voltage	6V ≤ V_S ≤ 25V 1mA ≤ I_{O1} ≤ 50mA	4.90	5.00	5.10	V
V_{O2}-V_{O1}	Output Voltage 2 Tracking Error (note1)	6V ≤ V_S ≤ 25V 5mA ≤ I_{O2} ≤ 500mA Enable = LOW	– 25		+ 25	mV
V_{DP1}	Dropout Voltage 1	I_{O1} = 10mA I_{O1} = 50mA		0.1 0.2	0.25 0.4	V V
V_{IO1}	Input to output Voltage Difference in Undervoltage Condition	V_S = 4V, I_{O1} = 35mA			0.4	V
V_{DP2}	Dropout Voltage 2	I_{O2} = 100mA I_{O2} = 500mA		0.2 0.3	0.3 0.6	V V
V_{IO2}	Input to output Voltage Difference in Undervoltage Condition	V_S = 4.6V, I_{O2} = 350mA			0.6	V
$V_{OL1\ 2}$	Line Regulation	6V ≤ V_S ≤ 25V I_{O1} = 1mA, I_{O2} = 5mA			20	mV
V_{OLIO1}	Load Regulation 1	1mA ≤ I_{O1} ≤ 50mA			25	mV
V_{OLO2}	Load Regulation 2	5mA ≤ I_{O2} ≤ 500mA			50	mV
I_{LIM1}	Current Limit 1	V_{O1} = 4.5V V_{O1} = 0V (note2)	55 25	100	200 100	mA mA
I_{LIM2}	Current Limit 2	V_{O2} = 0V	550	1000	1500	mA
I_{QSB}	Quiescent Current Standby Mode (output 2 disabled)	I_{O1} = 0.3mA ; T_j < 100°C V_{EN} ≥ 2.4V Vs = 14V Vs = 3.5V		 150 300	 250 800	 µA µA
I_Q	Quiescent Current	I_{O1} = 50mA I_{O2} = 500mA			30	mA

ENABLE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ENL}	Enable Input LOW Voltage (output 2 active)		– 0.3		1.5	V
V_{ENH}	Enable Input HIGH Voltage		2.4		7	V
V_{ENhyst}	Enable Hysteresis		30	75	200	mV
I_{EN}	Enable Input Current	0V < V_{EN} < 1.2V 2.5V < V_{EN} < 7V	– 10 – 1	– 1.5 0	– + 1	µA µA

RESET

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Rt}	Reset Low Threshold Voltage	Vs = 14V	V_{o1}-0.4	4.7	V_{o1}-0.1	V
V_{Rth}	Reset Threshold Hysteresis		50	100	200	mV
t_{RD}	Reset Pulse Delay	C_T = 100nF ; t_R > 100µs	55	100	180	ms
t_{RR}	Reset Reaction Time	C_T = 100nF	1	10	50	µs
V_{RL}	Reset Output LOW Voltage	R_{RES} = 10KΩ to V_{O1} $V_S \geq 3V$			0.4	V
I_{LRES}	Reset Output HIGH Leakage	V_{RES} = 5V			1	µA
V_{CTth}	Delay Comparator Threshold			2.0		V
$V_{CTth, hyst}$	Delay Comparator Threshold Hysteresis			100		mV

Note : 1 V_{O2} connected to ADJ V_{O2} can be set to higher values by inserting an external resistor divider.
2 Foldback characteristic

FUNCTIONAL DESCRIPTION

The L4937 is based on the SGS-THOMSON Microelectronics modular voltage regulator approach. Several out-standing features and auxiliary functions are provided to meet the requirements of supplying the microprocessor systems used in automotive applications.

Furthermore the device is suitable also in other applications requiring two stabilized voltages.

The modular approach allows other features and functions to be realized easily when required.

STANDBY REGULATOR

The standby regulator uses an Isolated Collector Vertical PNP transistor as the regulating element. This structure allows a very low dropout voltage at currents up to 50mA. The dropout operation of the standby regulator is maintained down to 2V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. This feature avoids functional interruptions which could be generated by overvoltage pulses.

The typical curve of the standby output voltage as a function of the input supply voltage is shown in fig. 1.

The current consumption of the device (quiescent current) is less than 250µA when output 2 is disabled (standby mode). The dropout voltage is controlled to reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region.

The quiescent current is shown in fig. 2 as a function of the supply input voltage 2.

OUTPUT 2 VOLTAGE

The output 2 regulator uses the same output structure as the standby regulator, but rated for an output current of 500mA.

The output 2 regulator works in tracking mode with the standby output voltage as a reference voltage.

The output 2 regulator can be switched off via the Enable input.

Figure 1 : Output Voltage vs. Input Voltage.

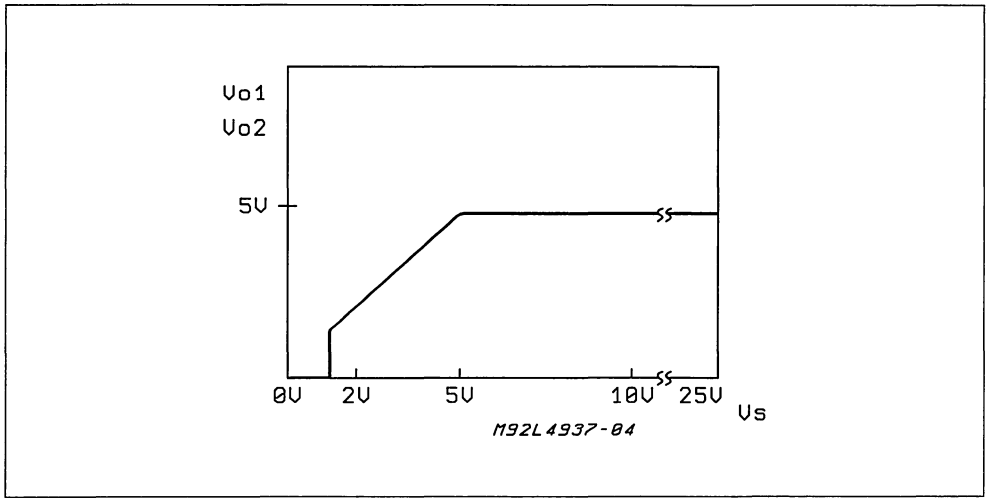
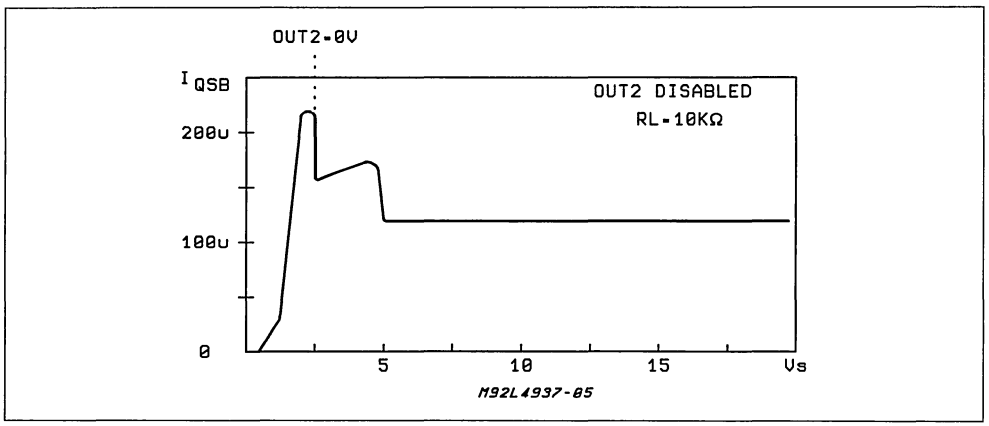


Figure 2 : Quiescent Current vs. Supply Voltage.



RESET CIRCUIT

The block circuit diagram of the reset circuit is shown in fig. 3. The reset circuit supervises the standby output voltage. The reset threshold of 4.7V is defined by the internal reference voltage and the standby output divider.

The reset pulse delay time t_{RD}, is defined by the charge time of an external capacitor C_T :

$$t_{RD} = \frac{C_T \times 2V}{2\mu A}$$

The reaction time of the reset circuit depends on the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T.

The reaction time of the reset circuit increases the noise immunity. In fact, if the standby output voltage drops below the reset threshold for a time shorter than the reaction time t_{RR}, no reset output variation occurs. The nominal reset delay is generated for standby output voltage drops longer than the time necessary for the complete discharging of the capacitor C_T. This time is typically equal to 50µs if C_T = 100nF. The typical reset output waveforms are shown in fig.

Figure 3 : Block Diagram of the Reset Circuit.

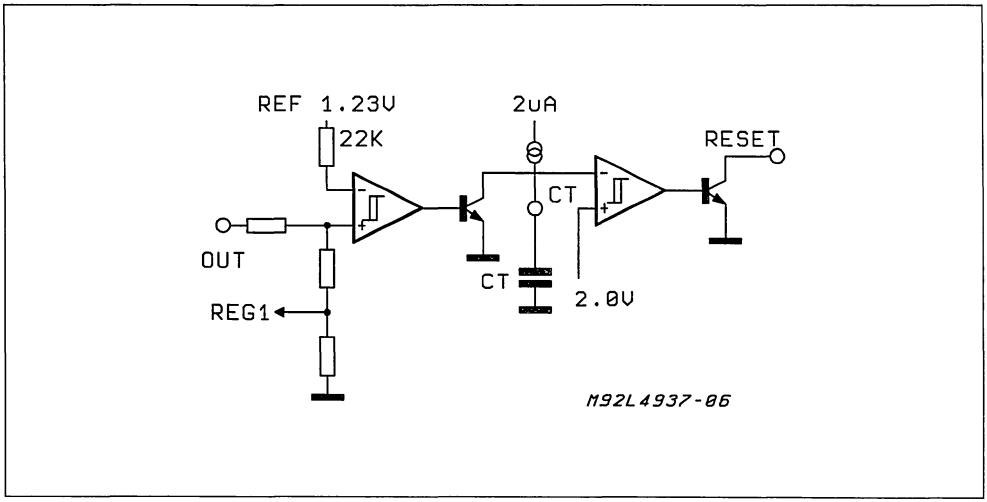
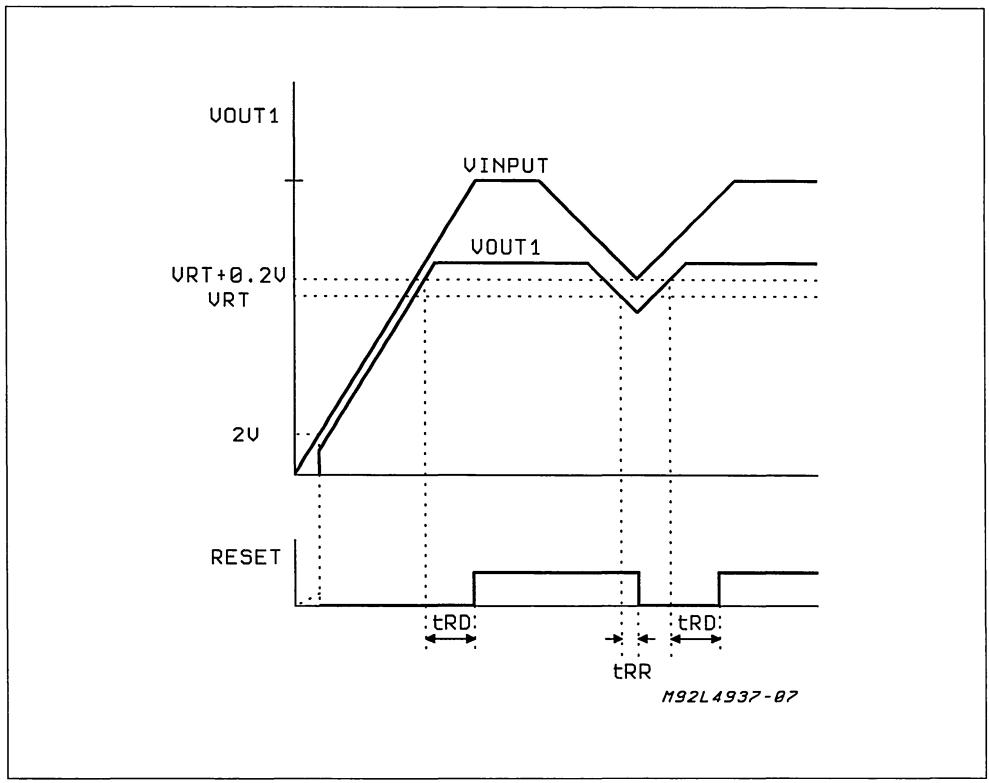


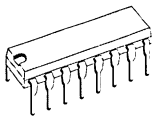
Figure 4 : Typical Reset Output Waveforms.



DUAL MULTIFUNCTION 5V VOLTAGE REGULATOR

ADVANCE DATA

- 50mA STANDBY AND 80mA SWITCHED 5V OUTPUTS
- LOW DROPOUT (LESS THAN 600mV)
- CURRENT LIMITING CIRCUITRY
- ANTI-SATURATION CIRCUITRY
- PROGRAMMABLE DELAY RESET FUNCTION
- LOW BATTERY SHUTDOWN FOR STANDBY REGULATOR
- COMPARATOR TO TRANSLATE BATTERY REFERENCED SIGNAL TO CMOS LOGIC LEVEL OUTPUT
- IGNITION SENSE COMPARATOR WITH CMOS LOGIC LEVEL OUTPUT
- LESS THAN 600µA QUIESCENT CURRENT IN STANDBY MODE
- 50V LOAD DUMP PROTECTED
- 100 x CURRENT MULTIPLIER FUNCTION



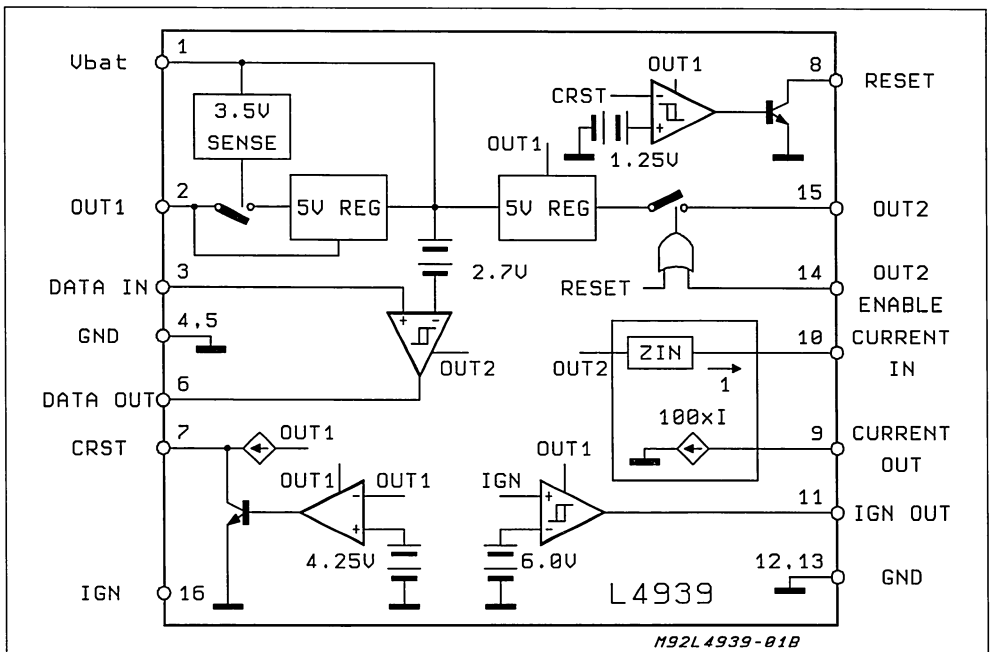
POWERDIP 12+2+2

ORDERING NUMBER: L4939

DESCRIPTION

The L4939 is a monolithic integrated 5V dual voltage regulator with data transmission and ignition sense functions.

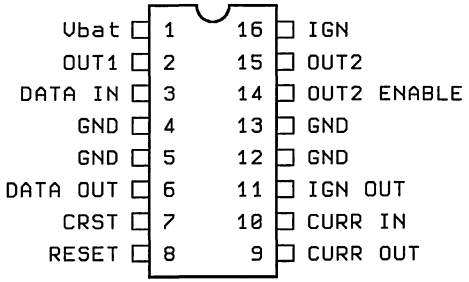
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-14 to 26	VDC
V (3)	Data In Voltage (pin 3)	0.7 to V_{BAT} + 0.5	VDC
V (16)	Ignition (pin 16) (with a 1K min. series resistance)	-14 to 26	VDC
P_{tot}	Power Dissipation derate at (40°C/W; T_{amb} = 85°C)	1.5	W
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature	-65 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
Rth j-case	Thermal Resistance Junction-case	max.	15	°C/W

PIN FUNCTIONS

N.	Name	Function
1	Vbat	Supply input from car battery
2	OUT 1	Standby 5V supply output
3	DATA IN	Data comparator input
4	GND	Ground and heat sink
5	GND	Ground and heat sink
6	DATA OUT	Data comparator output to micro
7	C_{rst}	Reset capacitor for controlling reset delay
8	RESET	Reset output
9	CURRENT OUT	Current mirror output
10	CURRENT IN	Current mirror input from micro
11	IGN OUT	Ignition comparator output to micro
12	GND	Ground
13	GND	Ground
14	OUT 2 ENABLE	Enable input for OUT 2 regulator
15	OUT 2	Switched 5V supply output
16	IGN	Ignition control input from car wiring

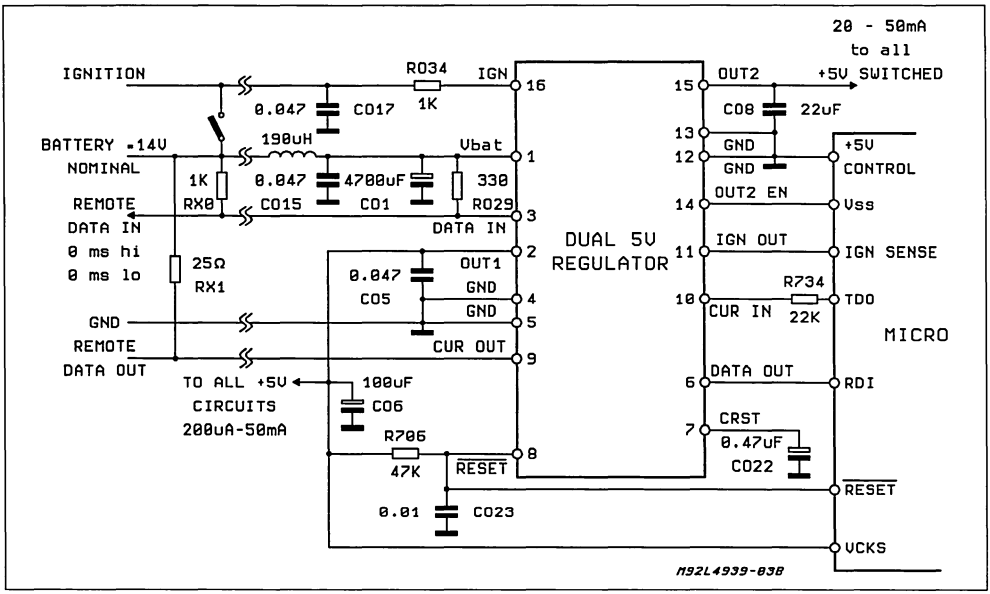
ELECTRICAL CHARACTERISTICS (V_{BAT} and IGN pins = 9 to 18V_{DC}; T_{amb} = -40 to 85°; unless otherwise specified.)

Symbol	Parameter	Pin	Test Condition	Min.	Typ	Max.	Unit
V_{O1}	Output Voltage	2	I_{OUT1} = 50mA; V_{bat} = 9 to 16V	4.75	5.00	5.25	V
V_{O1}	Dropout Voltage	2	V_{bat} = 4.75V; I_{OUT1} = 50mA	4.15			V
	Line Regulation	2	V_{bat}= 6.2 to 16V; I_{OUT1} = 50mA			40	mV
	Load Regulation	2	V_{bat} = 6.2, 11 & 18V; I_{OUT1} = 0.5 to 50mA			40	mV
I_{L1}	Current Limit	2	V_{bat}= 16V; V_{OUT1} = 3V; measure I_{OUT1}	60		250	mA
V_{O2}	Output Voltage ON	15	I_{OUT2} = 80mA; V_{bat} = 9 to 16V	4.75	5.00	5.25	V
V_{O2}	Output Voltage OFF	15	No Load on Out2; Out 2 Enable = 0V			150	mV
V_{O2}	Dropout Voltage	15	V_{bat} = 4.75V I_{OUT2} = 80mA	4.15			V
	Line Regulation	15	V_{bat} = 6.2 to 16V I_{OUT2} = 80mA			40	mV
	Load Regulation	15	V_{bat} = 6.2, 11 & 18V; I_{OUT2} = 0.5 to 80mA			40	mV
I_{L2}	Current Limit	15	V_{bat}= 16V, V_{OUT2} = 3V; measure I_{OUT2}	100		250	mA
	Enable ON Current	14	Out2 Enable = V_{OUT1}; measure $I_{(OUT2\ ENAB)}$	10		140	µA
I_q	Quiescent Current		Data IN = V_{bat} = Current out = 12.6V I_{OUT1} = 500µA; Out2 Enable = 0; Ign = 0		400	600	µA
	Reset Vo Low	8	V_{bat} = 3.75V			200	mV
	Data Comparator Vo Low	6	$I_{data\ out}$ = 50µA; Data IN = V_{bat} -5V			150	mV
	Data Comparator V_O High	18	$I_{data\ out}$ = 50µA; Data IN = V_{bat}	V_{out1} -0.2			V
	Current In Voltage	10	$I_{pin\ 10}$ =200µA, 250Ω from pin 9 to V_{bat}; V_{bat} = 13.5V	V_{out1} -1.5		V_{out1} -0.8	V
	Current Out Maximum	9	$I_{pin\ 10}$ =700µA, 250Ω from pin 9 to V_{bat}; V_{bat} = 13.5V	35			mA
I_9	Current Out	9	$I_{pin\ 10}$ =200µA, 250Ω from pin 9 to V_{bat}; V_{bat} = 13.5V	16	20	24	mA
			$I_{pin\ 10}$ =100µA, 250Ω from pin 9 to V_{bat}; V_{bat} = 13.5V	8	10	12	mA
			$I_{pin\ 10}$ =300µA, 250Ω from pin 9 to V_{bat}; V_{bat} = 13.5V	24	30	36	mA
V_9	Current Out V_{sat}	9	$I_{pin\ 10}$ =200µA, 1KΩ from pin 9 to V_{bat}; V_{bat} = 13.5V			1	V
	Thermal Shutdown		must open circuit Out1 and Out2	135		165	°C
	Overvoltage Shutdown	1	must operate over full range of I_{O1} and I_{O2}	18.5		23	V
	Noise Voltage ON Out 1	2	I_O =50µA; BW = 100Hz to 22KHz			200	µV
	Ripple Rejection ON Out 1	2	1V peak-peak sine on V_{bat}; f = 120Hz and 3KHz	45			dB
	Noise Voltage ON Out 2	15	I_O =80mA; BW = 100Hz to 22KHz			200	µV
	Ripple Rejection ON Out 2	15	1V peak-peak sine on V_{bat}; f = 120Hz and 3KHz	45			dB
	Reset Low Threshold	2	I_{O1} =500µA; V_{bat} ramps down, measure V_{O1} when reset goes Low	4	4.25	4.5	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Pin	Test Condition	Min.	Typ	Max.	Unit
R_d	Reset Delay	8	0.47 µF from pin 7 to GND, step V_{bat} from 0 to 14V; measure delay to RESET Low to High	50	150	250	ms
	Data IN Comparator Negative Threshold	3	Measured with respect to V_{bat}	-3.4	-2.7	-2	V
	Data IN Comparator Hysteresis	3		70	200	450	mV
	Ign Comparator Positive Threshold	16	Level of IGN required to toggle IGN Out on a rising edge	5.5	6	6.5	V
	Ign Comparator Hysteresis	16		70	200	450	mV
	Rise Time Data Out	6	V_{bat} = 9V; 10MΩ and 50pF from pin 6 to GND			10	µs
	Fall Time Data Out	6	V_{bat} = 9V; 10MΩ and 50pF from pin 6 to GND			10	µs
	Rise Time Ign Out	6	V_{bat} = 9V; 10MΩ and 50pF from pin 11 to GND			10	µs
	Fall Time Ign Out	11	V_{bat} = 9V; 10MΩ and 50pF from pin 11 to GND			10	µs
	Rise Time Reset	8	V_{bat} = 9V; 10KΩ from pin 8 to Out1, 50pF from pin 8 to GND			10	µs
	Fall Time Reset	8	V_{bat} = 9V; 10KΩ from pin 8 to Out1, 50pF from pin 8 to GND			10	µs
	Low Voltage Shutoff	1	Out1 Pass Element is open-circuited when V_{bat} is low-measured on falling edge	3.0	3 5	4.0	V
	Low Voltage Shutoff Hysteresis	1		100	200	300	mV

APPLICATION CIRCUIT



FUNCTIONAL DESCRIPTION

OUT1 AND OUT2

These are both 5V regulator outputs that utilize PNP pass elements and draw the current for their outputs from the battery line (pin 1). Out1 (pin 2) is designed to source a maximum of 50mA with a 100µF aluminium electrolytic capacitor and a 0.047µF ceramic capacitor connected in parallel as a load. Out2 (pin 15) is designed to source a maximum of 80mA with a 22µF aluminium electrolytic capacitor and 0.047µF ceramic capacitor connected in parallel as a load. Out 1 can be open-circuited by the Out1 Pass Element Shutdown described below and by an overvoltage condition on the battery line (pin 1).
Out 2 can be open-circuited by the Out 2 Enable line (pin 14) being held low (by external components or the internal pulldown resistor), a reset condition on Out 1 (described below), and an overvoltage condition on the battery line. Both outputs are current limited for short circuit protection and have anti-saturation circuits that prevent their dropout voltage from becoming too low.

IGNITION BUFFER

This circuit is a noninverting buffer that translates the Ignition Line Level to a 5V logic signal (pin 16). There is an external 1KΩ resistor between the Ignition line and the input to the IC (pin 16) to limit the current into and out of the part in overvoltage and reverse battery conditions. The nominal threshold of the comparator is 6V. Transitions of the Ignition line will have no effect upon Out1 (beyond that given in the spec parameters) or Out2, as long as the Ignition line voltage does not exceed the maximum limits given. This circuit will be powered from Out 1.

DATA BUFFER

This circuit is a noninverting buffer that translates the Data In (pin 3) voltage to a 5V logic signal Data Out (pin 6). The nominal threshold of this circuit is (V_{BAT} - 2.7V). This circuit is powered from Out 2, and will be disabled whenever Out 2 is disabled.

CURRENT MIRROR

This circuit will sink a current into pin 9 that is approximate equal to 100 times the current that is sourced from pin 10.
Current Mirror is powered from Out 2, and will be disabled when Out 2 is disabled. During an Out 2 shutdown, Current Out will be open circuit (Fig. 1 shows the above condition assuming that Current In is tied to GND through a 22KΩ resistor and that Current Out is tied to GND through a 250Ω resistor.

RESET

Pin 8 is NPN open collector output that is pulled low whenever Out1 falls below the reset thre-

shold, which is 4.25V nominally. When Out 1 goes back above 4.25V, the NPN will be held on for a period of time which is determined by the value of the capacitor which is tied from reset (pin 7) to ground (about 150ms for a 0.47µF capacitor). After this period of time, the NPN will be shut off and the voltage of pin 8 will be determined by the external components connected to it. Also, Out 2 will be disabled whenever Out 1 drops below the reset threshold, and the above mentioned delay time has passed (fig. 1).

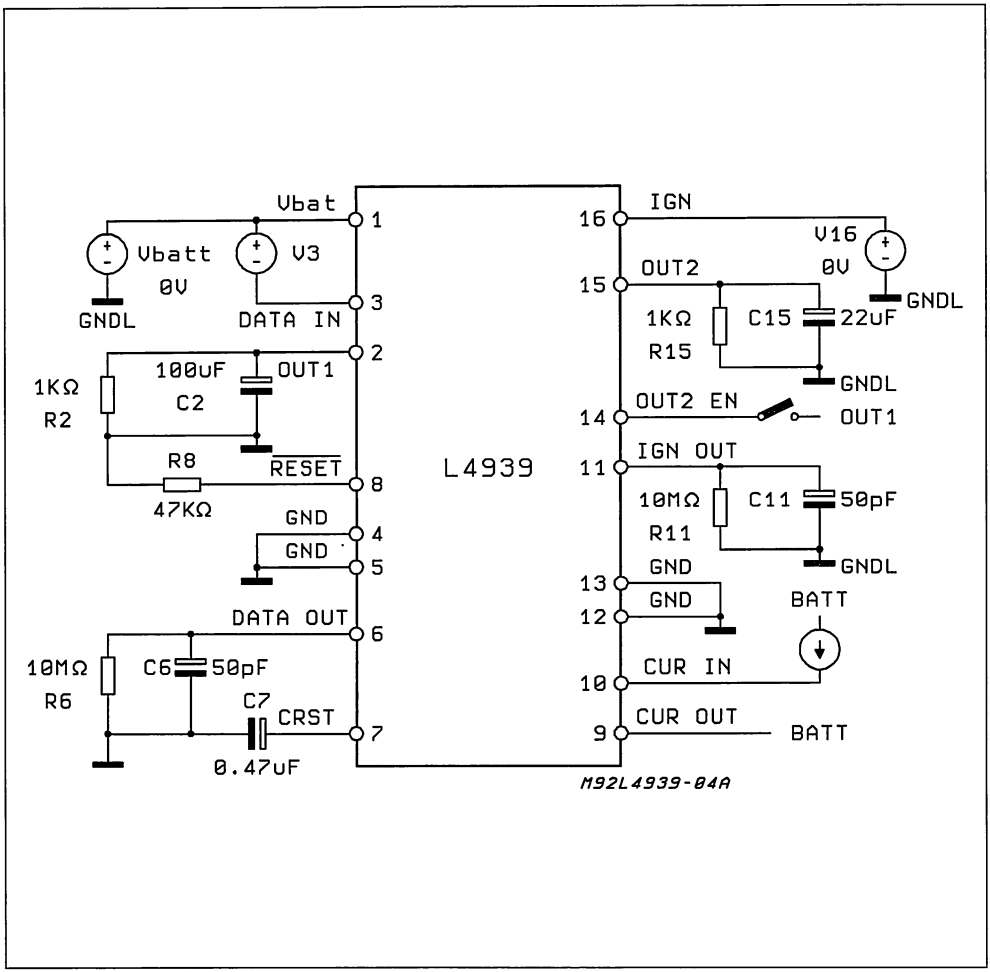
PASS ELEMENT SHUTDOWN

Upon ramp-down of the battery voltage, the output of the OTA is disabled at V_{batt} = 3.5V depriving the Out 1 PNP pass element of base current and open circuiting Out 1. This will prevent the regulator from conducting in reverse during low battery conditions. This circuit will exhibit nominal hysteresis of 200mV, meaning that Out 1 will be enabled again after the battery voltage rises above 3.7V (fig. 2).

OUT 1 DROP-OUT PROTECTION

Given that the battery voltage applied to pin 1 can vary between +18V and +5.6 during crank. Out 1 will display less than 250mV variation due to these battery fluctuations (assuming a constant load).

TEST CIRCUIT



Note: the following information for clarification not for specification definition.

Figure 1.

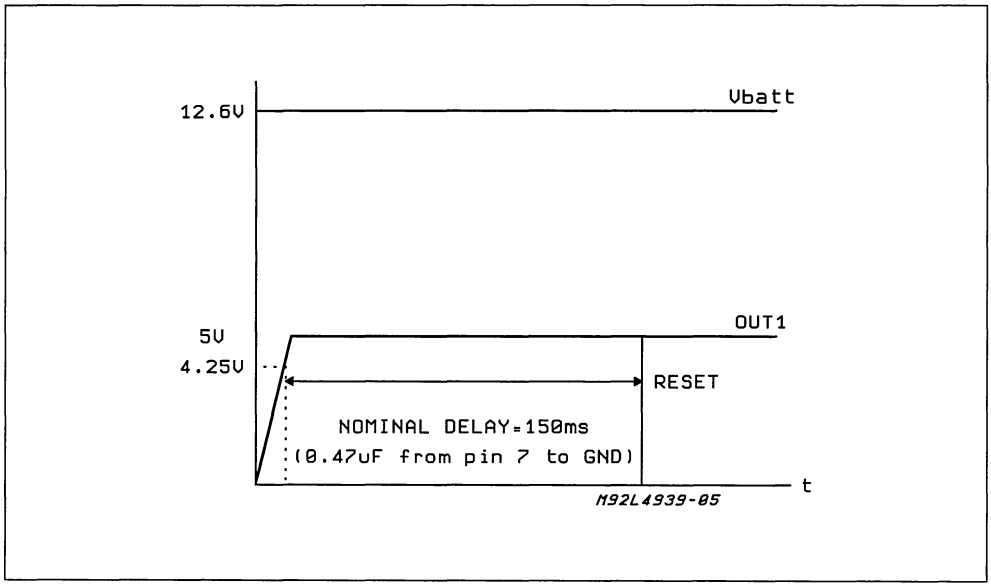
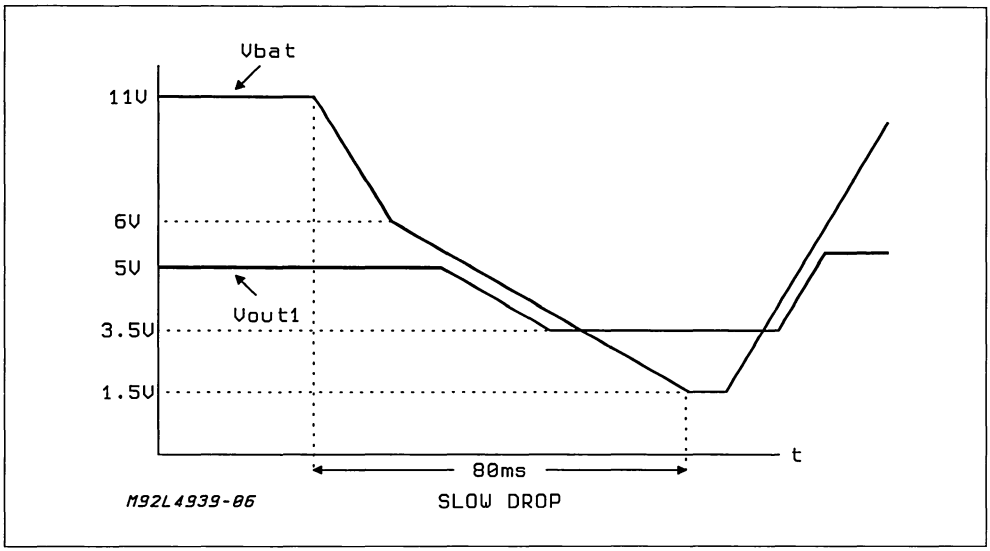
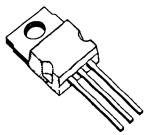


Figure 2.



5V/8.5V/10V VERY LOW DROP VOLTAGE REGULATORS

- PRECISE OUTPUT VOLTAGE:
  5V ± 4% (L4945)
  8.5V ± 4% (L4950)
  10V ± 4% (L4951)
  OVER FULL TEMPERATURE RANGE
  (– 40 / 125 °C)
- VERY LOW VOLTAGE DROP (0.75Vmax) OVER FULL TEMPERATURE RANGE
- OUTPUT CURRENT UP TO 500mA
- OVERVOLTAGE AND REVERSE VOLTAGE PROTECTIONS
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION AND THERMAL SHUT-DOWN (with hysteresis)
- LOW START UP CURRENT



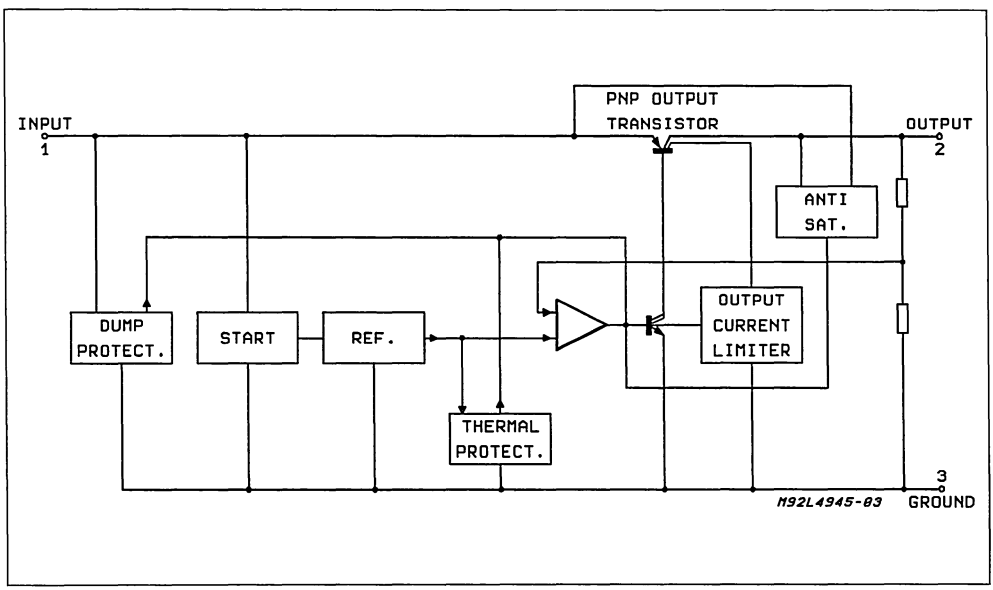
TO220

ORDERING NUMBER: L4945
L4950
L4951

DESCRIPTION

The devices are a monolithic integrated circuit in Versawatt package specially designed to provide a stabilized supply voltage for automotive and industrial electronic systems. Thanks to their very low voltage drop, in automotive applications the devices can work correctly even during the cranking phase, when the battery voltage could fall as low as 6V. Furthermore, they incorporate a complete range of protection circuits against the dangerous overvoltages always present on the battery rail of the car.

BLOCK DIAGRAM

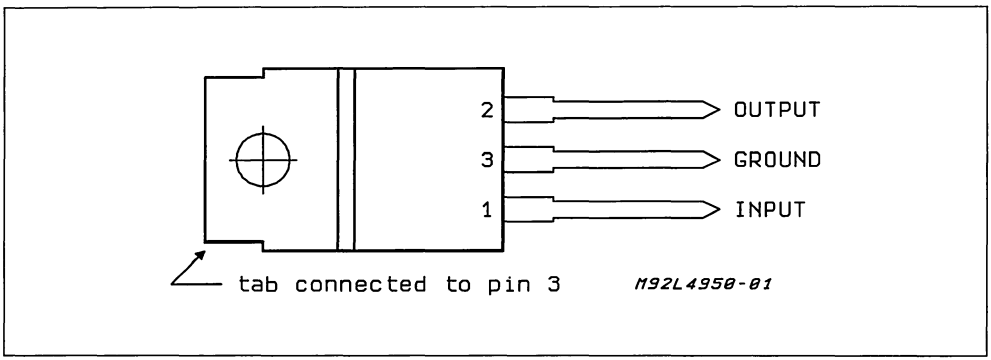


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage DC Reverse Input Voltage Transient Input Overvoltages : Load Dump : $5ms \leq t_{rise} \leq 10ms$ τ_f Fall Time Constant = 100ms $R_{SOURCE} \geq 0.5\Omega$ Field Decay : $5ms \leq t_{fall} \leq 10ms$, $R_{SOURCE} \geq 10\Omega$ τ_r Rise Time Constant = 33ms Low Energy Spike : $t_{rise} = 1\mu s$, $t_{fall} = 500\mu s$, $R_{SOURCE} \geq 10\Omega$ f_r Repetition Frequency = 5Hz	35 – 18 80 – 80 ± 100	V V V V V
T_J	Junction Temperature Range	– 40 to 150	°C
T_{OP}	Operating Temperature Range	– 40 to 125	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

Note: The circuit is ESD protected according to MIL-STD-883C.

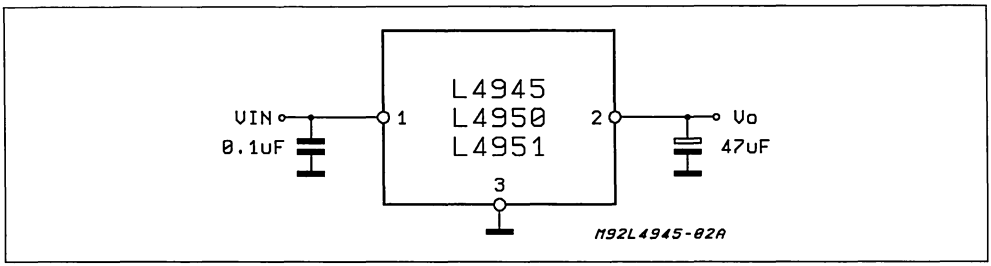
PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_I = 14. 4V, C_O = 47µF, ESR < 10Ω, R_p = 1KΩ, R_L = 1KΩ, −40°C ≤ T_J ≤ 125°C, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 0mA to 500mA					
		Over Full T Range	for L4945	4.80	5.00	5.20	V
			for L4950	8.16	8.50	8.84	V
			for L4951	9.60	10	10.4	V
		T_J = 25°C	for L4945	4.90	5.00	5.10	V
			for L4950	8.33	8.50	8.67	V
			for L4951	9.80	10	10.2	V
V_I	Operating Input Voltage	I_o = 0mA to (*) 500mA		6		26	V
ΔV_o	Line Regulation	V_I = 6V to 26V ; I_o = 5mA			2	10	mV
ΔV_o	Load Regulation	I_o = 5mA to 500mA			15	60	mV
$V_I - V_o$	Dropout Voltage	I_o = 500mA, T_J = 25°C			0.40	0.55	V
		Over Full T Range				0.75	V
I_q	Quiescent Current	I_o = 0mA, T_J = 25°C			5	10	mA
		I_o = 0mA Over Full T			6.5	13	mA
		I_o = 500mA Over Full T			110	180	mA
	Temperature Output Voltage Drift				− 0.5		mV/°C
SVR	Supply Volt. Rej.	I_o = 350mA ; f = 120Hz C_o = 100µF ; V_I = 12V ± 5V_{pp}		50	60		dB
I_{sc}	Output Short Circuit Current			0.50	0.80	1.50	A

(*) For a DC voltage 26 < V_I < 37V the device is not operating

FUNCTIONAL DESCRIPTION

The block diagram shows the basic structure of the devices : the reference, the error amplifier, the driver, the power PNP, the protection and reset functions.

The power stage is a Lateral PNP transistor which allows a very low dropout voltage (typ. 400mV at T_J = 25°C, max. 750mV over the full temperature range @ I_O = 500mA). The typical curve of the dropout voltage as a function of the junction temperature is shown in Fig. 1 : that is the worst case, where I_O = 500mA.

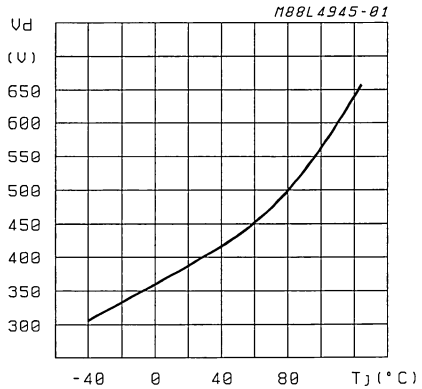
The current consumption of the devices (quiescent current) are maximum 10mA - over full T - when no load current is required.

The internal antisaturation circuit allows a drastic reduction in the current peak which takes place during the start up.

The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (C_{omin} = 20µF) to guarantee the global stability of the system.

Load dump and field decay protections (± 80V, t = 300ms), reverse voltage (− 18V) and short circuit protection, thermal shutdown are the main features that make the devices specially suitable for applications in the automotive enviroment.

Figure 1: Typical Dropout Voltage vs. T_j (I_o = 500mA).



EXTERNAL COMPENSATION

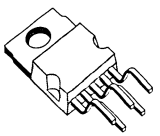
Since the purpose of a voltage regulator is to supply and load variations, the open loop gain of the regulators must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shift due to other poles at the unity gain frequency. The lower the frequency of these others poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be capacitor esed to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequencybtoo low to be compensated by a capacitor which can be integrated. An external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The paeassitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is 47µF.

5V-0.5A VERY LOW DROP REGULATOR WITH RESET

- PRECISE OUTPUT VOLTAGE (5V ± 4%) OVER FULL TEMPERATURE RANGE (– 40 / 125 °C)
- VERY LOW VOLTAGE DROP (0.75Vmax) OVER FULL T RANGE
- OUTPUT CURRENT UP TO 500mA
- RESET FUNCTION
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- + 80V LOAD DUMP PROTECTION
- – 80V LOAD DUMP PROTECTION
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION AND THERMAL SHUT-DOWN (with hysteresis)
- LOW START UP CURRENT



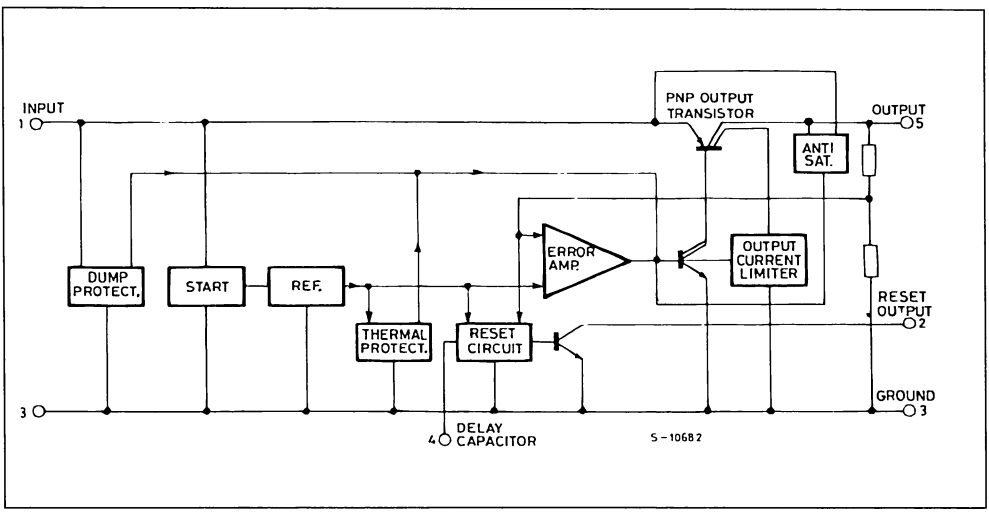
Pentawatt

ORDERING NUMBER: L4947/R

DESCRIPTION

The L4947/R is a monolithic integrated circuit in Pentawatt package specially designed to provide a stabilized supply voltage for automotive and industrial electronic systems. Thanks to its very low voltage drop, in automotive applications the L4947/R can work correctly even during the cranking phase, when the battery voltage could fall as low as 6V. Furthermore, it incorporates a complete range of protection circuits against the dangerous overvoltages always present on the battery rail of the car. The reset function makes the device particularly suited to supply microprocessor based systems : a signal is available (after an externally programmable delay) to reset the microprocessor at power-on phase ; at power-off, this signal becomes low inhibiting the microprocessor.

BLOCK DIAGRAM

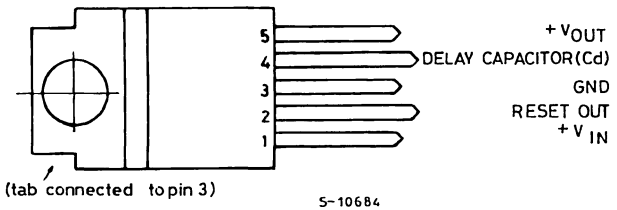


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage DC Reverse Input Voltage Transient Input Overvoltages : Load Dump : $5ms \leq t_{rise} \leq 10ms$ τ_f Fall Time Constant = 100ms $R_{SOURCE} \geq 0.5\Omega$ Field Decay : $5ms \leq t_{fall} \leq 10ms$, $R_{SOURCE} \geq 10\Omega$ τ_r Rise Time Constant = 33ms Low Energy Spike : $t_{rise} = 1\mu s$, $t_{fall} = 500\mu s$, $R_{SOURCE} \geq 10\Omega$ f_r Repetition Frequency = 5Hz	35 – 18 80 – 80 ± 100	V V V V V
V_R	Reset Output Voltage	35	V
T_J, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

Note: The circuit is ESD protected according to MIL-STD-883C.

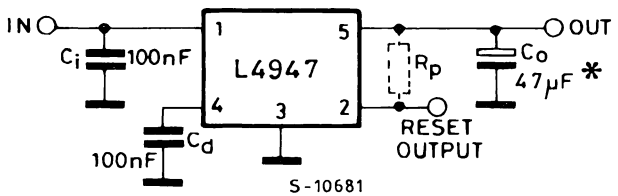
PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3.5	°C/W

TEST CIRCUIT



(*) Min. 20µF, ESR < 10Ω over full temperature range R_P (pull up resistor) and R_L (load) are both equal to 1KΩ.

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_i = 14. 4V, C_o = 47µF, ESR < 10Ω, R_p = 1KΩ, R_L = 1KΩ, –40°C ≤ T_J ≤ 125°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 0mA to 500mA Over Full T Range T_J = 25°C	4.80 4.90	5.00 5.00	5.20 5.10	V V
V_i	Operating Input Voltage	I_o = 0mA to (*) 500mA	6		26	V
ΔV_o	Line Regulation	V_i = 6V to 26V ; I_o = 5mA		2	10	mV
ΔV_o	Load Regulation	I_o = 5mA to 500mA		15	60	mV
$V_i - V_o$	Dropout Voltage	I_o = 500mA, T_J = 25°C Over Full T Range		0.40	0.55 0.75	V V
I_q	Quiescent Current	I_o = 0mA, T_J = 25°C I_o = 0mA Over Full T I_o = 500mA Over Full T		5 6.5 110	10 13 180	mA mA mA
$\frac{\Delta V_o}{T}$	Temperature Output Voltage Drift			– 0.5		mV/°C
SVR	Supply Volt. Rej.	I_o = 350mA ; f = 120Hz C_o = 100µF ; V_i = 12V ± $5V_{pp}$	50	60		dB
I_{sc}	Output Short Circuit Current		0.50	0.80	1.50	A
V_R	Reset Output Saturation Voltage	1.5V < V_o < $V_{RT\ (off)}$, I_R = 1.6mA 3.0V < V_o < $V_{RT\ (off)}$, I_R = 8mA			0.40 0.40	V V
I_R	Reset Output Leakage Current	V_O in Regulation, V_R = 5V			50	µA
$V_{RT\ peak}$	Power On-Off Reset out Peak Voltage	1KΩ Reset Pull-up to V_o, T_J = 25°C		0.50	0.80	V
$V_{RT\ (off)}$	Power OFF V_o Threshold	V_o @ Reset Out H to L Transition T_J = 25°C	4.70 4.75	 Vo–0.15		V V
$V_{RT\ (on)}$	Power ON V_o Threshold	V_o @ Reset Out L to H Transition		$V_{RT\ (off)}$ + 0.05	V_o – 0.04	V
V_{Hyst}	Power ON-Off Hysteresis	$V_{RT\ (on)} - V_{RT\ (off)}$		0.05		V
V_d	Delay Comparator Threshold	V_d @ Reset Out L to H Transition	3.65	4.00	4.35	V
		V_d @ Reset Out H to L Transition	3.20	3.55	3.90	V
V_{dH}	Delay Comparator Hysteresis			0.45		V
I_d	Delay Capacitor Charging Current	V_d = 3V, T_J = 25°C		20		/µA
V_{disch}	Delay Capacitor Discharge Voltage	V_o < $V_{RT\ (off)}$		0.55	1.20	V
T_d	Power on Reset Delay Time	C_d = 100nF, T_J = 25°C	10	20	30	ms

(*) For a DC voltage 26 < V_i < 37V the device is not operating

FUNCTIONAL DESCRIPTION

The L4947/R is a very low drop 5V/0.5A voltage regulator provided with a reset function and therefore particularly suited to meet the requirements of supplying the microprocessor systems used in automotive and industrial applications.

The block diagram shows the basic structure of the device : the reference, the error amplifier, the driver, the power PNP, the protection and reset functions.

The power stage is a Lateral PNP transistor which allows a very low dropout voltage (typ. 400mV at T_J = 25°C, max. 750mV over the full temperature range @ I_O = 500mA). The typical curve of the dropout voltage as a function of the junction temperature is shown in Fig. 1 : that is the worst case, where I_O = 500mA.

The current consumption of the device (quiescent

current) is maximum 13mA - over full T - when no load current is required.

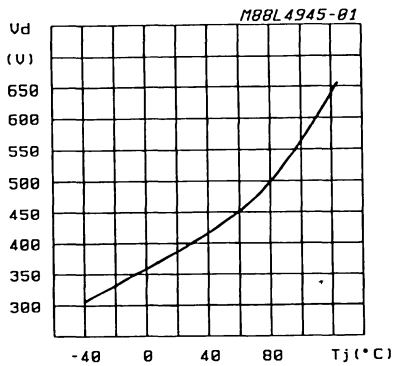
The internal antisaturation circuit allows a drastic reduction in the current peak which takes place during the start up.

The reset function supervises the regulator output voltage inhibiting the microprocessor when the device is out of regulation and resetting it at the power-on after a settable delay. The reset is LOW when the output voltage value is lower than the reset threshold voltage. At the power-on phase the output voltage increases (see Fig. 2) and - when it reaches the power-on V_O threshold V_{RT} (On) - the reset output becomes HIGH after a delay time set by the external capacitor C_d. At the power-off the output voltage decreases : at the $V_{RT(Off)}$ threshold value (V_O-0.15V typ. value) the reset output instantaneously goes down (LOW status) inhibiting the microprocessor. The typical power on-off hysteresis is 50mV.

The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (C_{omin} = 20µF) to guarantee the global stability of the system.

Load dump and field decay protections (± 80V), reverse voltage (– 18V) and short circuit protection, thermal shutdown are the main features that make the L4947/R specially suitable for applications in the automotive enviroment.

Figure 1: Typical Dropout Voltage vs. T_j (I_o = 500mA).



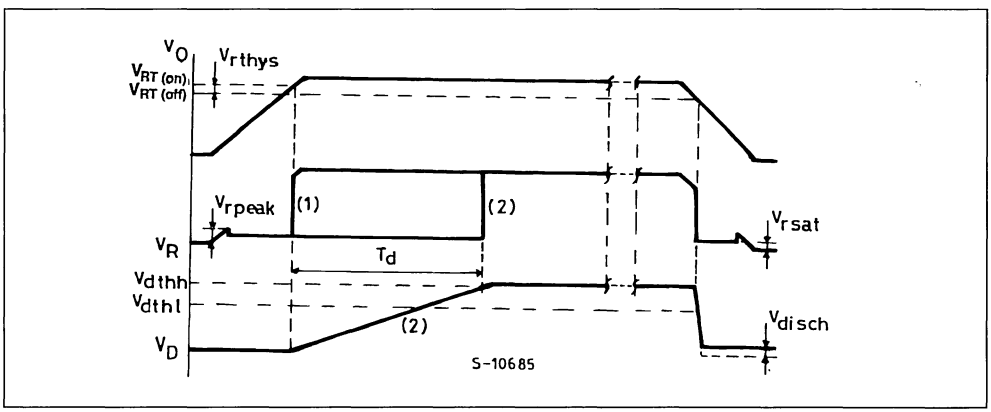
EXTERNAL COMPENSATION

Since the purpose of a voltage regulator is to supply and load variations, the open loop gain of the regulator must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shift due to other poles at the unity gain frequency. The lower the frequency of these others poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be capacitor esed to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequencybtoo low to be compensated by a capacitor which can be integrated. An external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The paeassitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is 47µF.

Figure 2: Reset Waveforms:
(1) Without External Capacitor C_d.
(2) With External Capacitor C_d.

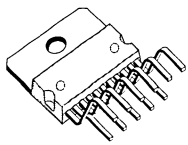


QUAD VOLTAGE REGULATOR WITH INHIBIT AND RESET

PRODUCT PREVIEW

- 4 OUTPUTS: 10V (300mA); 8V (400mA); 5V (600mA); 5V (100mA)
- 10V AND 5V (100mA) OUTPUT ARE LOW DROP
- 5V (100mA) ST-BY OUTPUT VOLTAGE
- EARLY WARNING OUTPUT FOR SUPPLY UNDERVOLTAGE (LVW)
- THERMAL SHUTDOWN AND CURRENT LIMITATION (FOLDBACK)
- REVERSE BATTERY AND LOAD DUMP PROTECTION
- INHIBIT (ON/OFF) AND RESET FUNCTIONS

MULTIPOWER BCD TECHNOLOGY



Multiwatt 11

ORDERING NUMBER: L4948

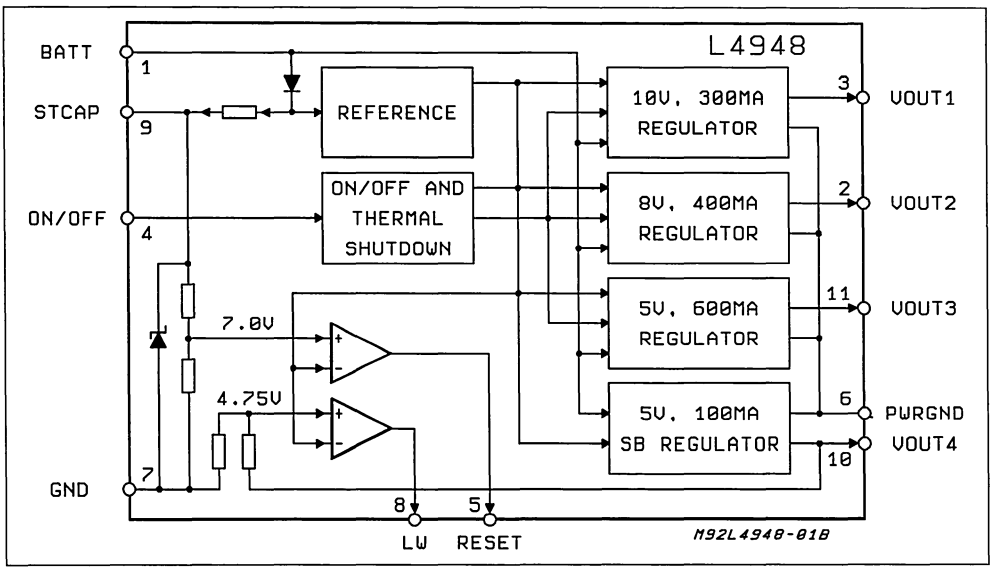
DESCRIPTION

The L4948 is a quad output low drop voltage regulator. The four outputs are a low drop 10V at 300mA (V_{O1}), a 8V at 400mA (V_{O2}), a 5V at 600mA (V_{O3}) and a low drop 5V st-by line at 100mA (V_{O4}).

The IC includes a monitoring circuit to warn if a low voltage or no voltage condition is occurring. $V_{O1,2,3}$ are off during st-by mode.

The STCAP pin allows the battery voltage to decay slowly giving the µP time to store data. This IC is designed for supplying microcomputer controlled systems specially in automotive applications.

BLOCK DIAGRAM



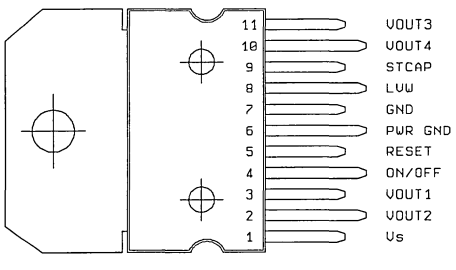
OPERATING CONDITION

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-15 to 27	V
I_L	Load Current I_{O1}	300	mA
	I_{O2}	400	mA
	I_{O3}	600	mA
	I_{O4}	100	mA

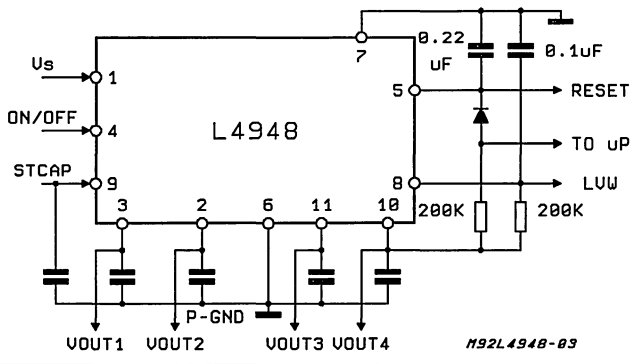
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-35 to 60	V
V_I	Input Voltage (ON/OFF)	0 to 12	V
V_O	Output Voltage (LVW, Reset)	0 to 12	V
T_{stg}	Storage Temperature Range	-65 to 150	°C
T_j	Junction Temperature Range	max 150	°C
	Load Dump (5ms rise, 115ms decay)	60	V

PIN CONNECTION



APPLICATION CIRCUIT



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	max	2	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 10.5 to 16V; I_{O1} = I_{O2} = I_{O3} = 5mA; I_{O4} = 0.5mA; C_O = 10µF max; T_{amb} = -40 to 85°C, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage	I_{O1} = 300mA; T_{amb} = 25°C; 11V < V_S < 16V all temps	9.7 9.5	10 10	10.3 10.5	V V
ΔV_{O1}	Load Regulation	I_{O1} = 6 to 300mA			150	mV
I_Q	Quiescent Current (ΔI_S)	V_S = 14V; I_{O1} = 6mA; V_S =14V ; I_{O1} = 300mA;			10 30	mA mA
V_S-V_{O1}	Dropout Voltage	I_{O1} = 300mA set V_S = V_{O1}+0.5V; T_{amb} = 25°C; set V_S = V_{O1}+0.8V;all			 600 900	 mV mV
		I_{O1} = 6mA set V_S = V_{O1}+0.15V; T_{amb} = 25°C; set V_S = V_{O1}+0.2V;all temps			 200 300	 mV mV
I_L	Current Limit	V_{O1} = 0V	150		800	mA
V_{O1}	Max Bat.Trans.	R_O = 100Ω Ramp V_S from 14 to 60V in 3-5ms			11	V
		Hold V_S at 60V for 10ms Ramp V_S from 60 to 14V in 3-5ms; T_{amb} = 25°C; all temps	 9.7 9.5	 10 10	2 10.3 10.5	V V V
V_{O1}	Rev. Voltage Trans.	V_S = -35V; t = 1ms; R_O = 100Ω Check V_{O1}, standard T_{amb} = 25°C; all temps	9.7 9.5	10 10	10.3 10.5	V V
V_{O1}	Rev. Voltage .	V_S = -15V; t = 30s; R_O = 100Ω	-0.4		1	V
	Ripple rejection	fo = 120-10KHz; 1V_{pp} AC ; V_S=14V I_{O1} = 180mA; I_{O2} = 200mA, I_{O3} = 400mA; I_{O4} = 40mA;	50			dB
		fo = 20-20KHz; 1V_{pp} AC ; V_S=14V I_{O1} = 180mA; I_{O2} = 200mA. I_{O3} = 400mA; I_{O4} = 40mA;	45			dB
ΔV_{O1}	Line Regulation ΔV_{O1} across V_S range ΔV_{O1} across V_S range V_{O1} - V_S across V_S range	 V_S = 11V to 26V V_S = 10.5V to 10.99V V_S = 10.2V to 10.49V			 50 500 300	 mV mV mV
V_{O2}	Output Voltage	I_{O2} = 400mA; T_{amb} = 25°C; all temps	7.75 7.60	8 8	8.25 8.40	V V
ΔV_{O2}	Load Regulation	I_{O2} = 8 to 400mA			150	mV
ΔI_Q	Quiescent Current (ΔI_S)	V_S = 14V; I_{O2} = 8mA; V_S = 14V; I_{O2} = 400mA;			10 30	mA mA
V_S-V_{O2}	Dropout Voltage	I_{O2} = 400mA set V_S = V_{O2}+1V; T_{amb} = 25°C; set V_S = V_{O2}+1.5V;all temps			1.1 1.6	V V
		I_{O2} = 8mA set V_S = V_{O2}+0.3V; T_{amb} = 25°C; set V_S = V_{O2}+0.4V;all temps			400 500	mV mV
I_L	Current Limit	V_{O2} = 0V	180		960	mA
V_{O2}	Max Bat.Trans.	R_O = 100Ω Ramp V_S from 14 to 60V in 3-5ms			9	V
		Hold V_S at 60V for 10ms Ramp V_S from 60 to 14V in 3-5ms; T_{amb} = 25°C; all temps	 7.75 7.60	 8 8	2 8.25 8.40	V V V
V_{O2}	Rev. Voltage Trans.	V_S = -35V; t = 1ms; R_O = 100Ω Check V_{O2}, standard T_{amb} = 25°C; all temps	7.75 7.60	8 8	8.25 8.40	V V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{O2}	Rev. Voltage .	V_S = -15V; t = 30s; R_O = 100Ω	-0.4		1	V
	Ripple rejection	fo = 120-10KHz; $1V_{pp}$ AC ; V_S=14V I_{O1} = 180mA; I_{O2} = 200mA, I_{O3} = 400mA; I_{O4} = 40mA;	50			dB
		fo = 20-20KHz; $1V_{pp}$ AC ; V_S=14V I_{O1} = 180mA; I_{O2} = 200mA, I_{O3} = 400mA; I_{O4} = 40mA;	45			dB
ΔV_{O2}	Line Regulation ΔV_{O2} across V_S range ΔV_{O2} across V_S range V_{O2} - V_S across V_S range	 V_S = 10.5V to 26V V_S = 9V to 10.49V V_S = 7V to 8.99V			 40 700 1.5	 mV mV V
V_{O3}	Output Voltage	I_{O3} = 600mA; T_{amb} = 25°C; all temps	4.85 4.75	5 5	5.15 5.25	V V
ΔV_{O3}	Line Regulation	V_S = 7V to 26V			40	mV
ΔV_{O3}	Load Regulation	I_{O3} = 4 to 600mA			100	mV
ΔI_Q	Quiescent Current (ΔI_S)	V_S = 14V; I_{O3} = 4mA; V_S = 14V; I_{O3} = 600mA;			8 40	mA mA
V_S-V_{O3}	Dropout Voltage	I_{O3} = 600mA set V_S = V_{O3}+1V; T_{amb} = 25°C; set V_S = V_{O3}+1.5V;all			 1.1 1.6	 V V
		I_{O3} = 4mA set V_S = V_{O3}+0.3V; T_{amb} = 25°C; set V_S = V_{O3}+0.4V;all			 400 500	 mV mV
I_L	Current Limit	V_{O3} = 0V	250		1440	mA
V_{O3}	Max Bat.Trans.	R_O = 100Ω Ramp V_S from 14 to 60V in 3-5ms			6	V
		Hold V_S at 60V for 10ms Ramp V_S from 60 to 14V in 3-5ms; T_{amb} = 25°C; all temps	 4.85 4.75	 5 5	2 5.15 5.25	V V V
V_{O3}	Rev. Voltage Trans.	V_S = -35V; t ≤ 1ms; R_O = 100Ω Check V_{O3}, standard T_{amb} = 25°C; all temps	 4.85 4.75	 5 5	 5.15 5.25	 V V
V_{O3}	Rev. Voltage .	V_S = -15V; t = 30s; R_O = 100Ω	-0.4		1	V
	Ripple rejection	fo = 120-10KHz; $1V_{pp}$ AC ; V_S=14V I_{O1} = 180mA; I_{O2} = 200mA, I_{O3} = 400mA; I_{O4} = 40mA;	50			dB
		fo = 20-20KHz; $1V_{pp}$ AC ; V_S=14V	45			dB
V_{O4}	Output Voltage	I_{O4} = 100mA; T_{amb} = 25°C; all temps	4.85 4.75	5 5	5.15 5.25	V V
ΔV_{O4}	Line Regulation	V_S = 7V to 26V			40	mV
ΔV_{O4}	Load Regulation	I_{O4} = 0.4 to 100mA			80	mV
ΔI_Q	Quiescent Current	V_S = 14V; I_{O4} = 2mA; V_S = 14V; I_{O4} = 100mA;			450 20	µA mA
V_S-V_{O4}	Dropout Voltage	I_{O4} = 100mA set V_S = V_{O4}+0.5V; T_{amb} = 25°C; set V_S = V_{O4}+0.8V;all temps			 600 900	 mV mV
		I_{O4} = 0.4mA set V_S = V_{O4}+0.15V; T_{amb} = 25°C; set V_S = V_{O4}+0.2V;all temps			 200 300	 mV mV
I_L	Current Limit	V_{O4} = 0V	50		300	mA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{O4}	Max Bat.Trans.	R_O = 1000Ω Ramp V_S from 14 to 60V in 3-5ms			6	V
		Hold V_S at 60V for 10ms Ramp V_S from 60 to 14V in 3-5ms; T_{amb} = 25°C; all temps	 4.85 4.75	 5 5	6 5.15 5.25	V V V
V_{O4}	Rev. Voltage Trans.	V_S = -35V; t = 1ms; R_O = 1000Ω Check V_{O4}, standard T_{amb} = 25°C; all temps	 4.85 4.75	 5 5	 5.15 5.25	 V V
V_{O4}	Rev. Voltage .	V_S = -15V; t = 30s; R_O = 1000Ω	-0.4		1	V
	Ripple rejection	f_O = 120-10KHz; 1V_{pp} AC ; V_S=14V I_{O1} = 180mA; I_{O2} = 200mA, I_{O3} = 400mA; I_{O4} = 40mA;	50			dB
		f_O = 20-20KHz; 1V_{pp} AC ; V_S=14V I_{O1} = 180mA; I_{O2} = 200mA, I_{O3} = 400mA; I_{O4} = 40mA;	45			dB
ON/OFF	Input Current	V_S = 14V; V_{IH} = >2V; V_S = 14V; V_{IL} = <0.8V;	 -1		1	µA µA
$V_{I\ ON/OFF}$	Input Threshold	V_S = 14V V_{IL} V_S = 14V V_{IH}	0 2		0.8 12	V V
V_R	Reset Output Voltage	V_S so that V_{O4} < 4.75V; R_O = 200KΩ to V_{04}; V_{IL} = "0"	0		0.75	V
		V_S so that V_{O4} >4.75V; R_O = 200KΩ to V_{04}; V_{IH} = "1"	2.75		12	V
	Reset Output Transition Time				20	ms
	LVW Output Threshold	Ramp V_S down until LVW switches from"1" to a "0"	7.0		8.2	V
	LVW Transition Time				20	ms
	LVW Output Voltage	STCAP <6.5V;R_O = 200KΩ to V_{O4}; V_{IL} = "0"	0		0.75	V
		STCAP >7.5V;R_O = 200KΩ to V_{O4}; V_{IH} = "1"	2.75		12	V
	Reset Output Stability	V_S is set such that 1 ≤ V_{04} ≤ 4V; I_{OUT4} = 2mA; $V_{ON/OFF}$ = 0 meas reset variation			50	mV
I_q	St-By Quiescent Current (ΔI_S)	$V_{ON/OFF}$ = 0V, $I_{O\ 4}$ = 100mA; V_S = 14V; $I_{O\ 1,2,3}$ = 0mA			20	mA
		$V_{ON/OFF}$ = 0V, $I_{O\ 4}$ = 2mA; V_{bat} = 14V; $I_{O\ 1,2,3}$ = 0mA			450	µA
	Maximum Quiescent Current (ΔI_S)	V_S = 14V; I_{O1} = 300mA; I_{O2} = 400mA, I_{O3} = 600mA; I_{O4} = 100mA; V_O = 5V			100	mA
	STCAP Output Voltage	V_S = 24V; V_S = 60V. 1ms	15		17 18	V V

FUNCTIONAL DESCRIPTION

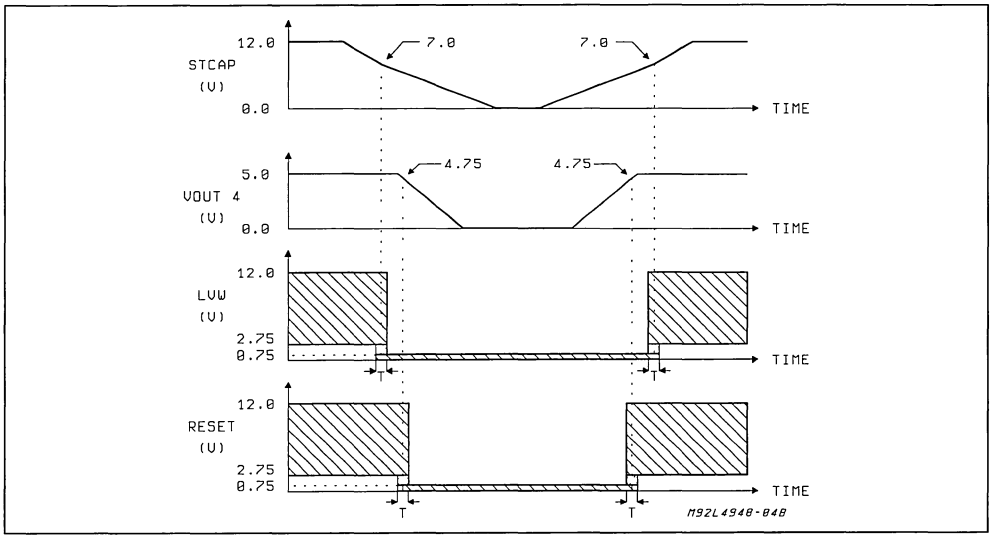
The L4948 includes a monitoring circuit to warn the microprocessor if a low voltage or no voltage condition is occurring. Between 6.5V and 7.5V on the STCAP pin, the LVW output will go low. This tells the microprocessor to stop executing code and save vital information. When the V_{04} drops between 4 and 5V the RESET output goes low. It is very important that the RESET output doesn,t go above 0.75V until the V_{04} output has gone back above 4.6V (typical). The microprocessor looks for a rising edge. So, any spike will tell the microprocessor to start operating. Once the STCAP line passes 7V (typical), the LVW output will also return to high state.

The STCAP pin acts like a delay circuit. Due to the large capacitor (470µF), the STCAP pin allows the battery voltage to decay slowly giving the microprocessor time to store data. Also, during short low voltage or negative voltage conditions,

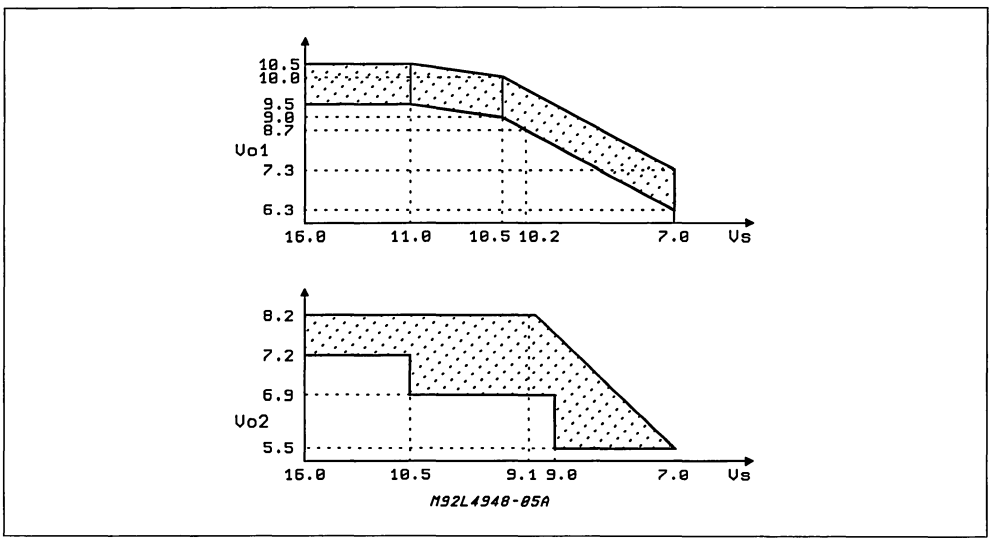
the STCAP pin protects the 5V st-by output from dropping below the RESET and LVW trip points The four output are expected to follow the battery voltage down to 7V. At 7V the outputs are expected to be remain alive and ready for a return of the battery.

The L4948 has a st-by mode to keep the microprocessor and memories allive during an ignition off conditions. The ON/OFF input pin in controlled by the microprocessor. An high on the ON/OFF pin places the part in normal mode. A low on the ON/OFF pin places the part in normal mode.

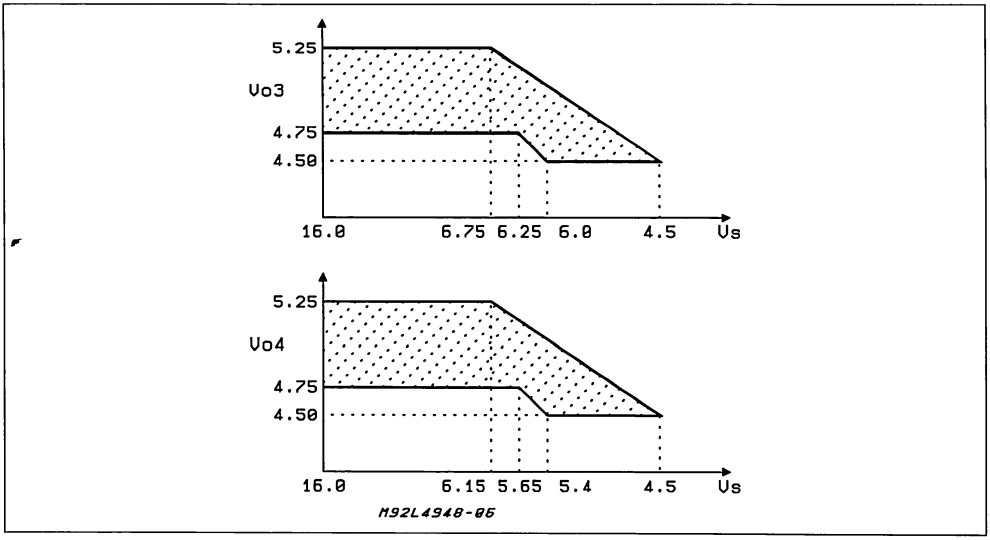
TIMING DIAGRAM



Graphs of the Output Curves for $V_{O1,2,3 \text{ and } 4}$



Graphs of the Output Curves for $V_{O1,2,3 \text{ and } 4}$ (Cont.)



Notes and Information
The following information is for clarification, not for specification definition.
Please use the information in this way

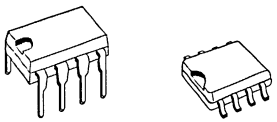
SGS-THOMSON MICROELECTRONICS

L4949

MULTIFUNCTION VERY LOW DROP VOLTAGE REGULATOR

ADVANCE DATA

- OPERATING DC SUPPLY VOLTAGE RANGE 5V - 28V
- TRANSIENT SUPPLY VOLTAGE UP TO 40V
- EXTREMELY LOW QUIESCENT CURRENT IN STANDBY MODE
- HIGH PRECISION STANDBY OUTPUT VOLTAGE 5V±1%
- OUTPUT CURRENT CAPABILITY UP TO 100mA
- VERY LOW DROPOUT VOLTAGE LESS THAN 0.4V
- RESET CIRCUIT SENSING THE OUTPUT VOLTAGE
- PROGRAMMABLE RESET PULSE DELAY WITH EXTERNAL CAPACITOR
- VOLTAGE SENSE COMPARATOR
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS



Minidip **SO-8**

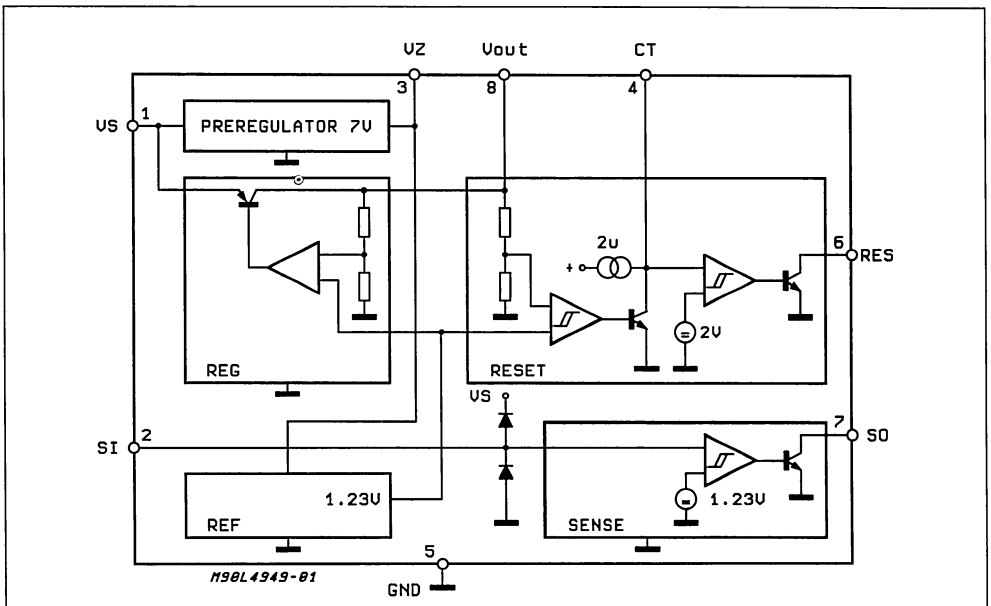
ORDERING NUMBERS:

L4949N L4949DN

DESCRIPTION

The L4949 is a monolithic integrated 5V voltage regulator with a very low dropout output and additional functions as power-on reset and input voltage sense. It is designed for supplying the microcomputer controlled systems especially in automotive applications.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{SDC}	DC Operating Supply Voltage	28	V
V_{STR}	Transient Supply Voltage (T < 1s)	40	V
I_O	Output Current	Internally Limited	
V_O	Output Voltage	20	V
I_{SI}	Sense Input Current	±1	mA
I_{EN}	Enable Input Current	-1	mA
V_{EN}	Enable Input Voltage	Vs	
V_{RES}, V_{SO}	Output Voltages	20	V
I_{RES}, I_{SO}	Output Currents	5	mA
V_Z	Preregulator Output Voltage	7	V
I_Z	Preregulator Output Current	5	mA
T_J	Junction Temperature	-40 to +150	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

Note: The circuit is ESD protected according to MIL-STD-883C

THERMAL DATA

Symbol	Description		Minidip	SO-8	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	200	°C/W
TJSD	Thermal Shutdown Junction temperature		165		°C

ELECTRICAL CHARACTERISTICS (V_S = 14V; -40°C < T_j < 125°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = 25°C; I_O = 1mA	4.95	5	5.05	V
V_O	Output Voltage	6V < V_{IN} < 28V, 1mA < I_O < 50mA	4.90	5	5.10	V
V_O	Output Voltage	V_{IN} = 35V; T < 1s 1mA < I_O < 50mA			5.50	V
V_{OP}	Dropout Voltage	I_O = 10mA I_O = 50mA I_O = 100mA		0.1 0.2 0.3	0.25 0.4 0.5	V V V
V_{IO}	Input to Output Voltage Difference in Undervoltage Condition	V_{IN} = 4V, I_O = 35mA			0.4	V
V_{OL}	Line Regulation	6V < V_{IN} < 28V; I_O = 1mA			20	mV
V_{OLO}	Load Regulation	1mA < I_O < 100mA			30	mV
I_{LIN}	Current Limit	V_O = 4.5V V_O = 0V (note 1)	105	200 50	400	mA mA
I_{QSE}	Quiescent Current	I_O = 0.3mA; T_J < 100°C		150	260	µA
I_Q	Quiescent Current	I_O = 100mA			5	mA

RESET

V_{RT}	Reset Thereshold Voltage			V_O-0.5V		V
V_{RTH}	Reset Thereshold		50	100	200	mV

Note 1. Foldback characteristic

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{RD}	Reset Pulse Delay	C_T = 100nF; T_R ≥100µs	55	100	180	ms
t_{RR}	Reset Reaction Time	C_T = 100nF		5	30	µs
V_{RL}	Reset Output Low Voltage	R_{RES} = 10KΩ to V_O V_S ≥ 3V			0.4	V
I_{RH}	Reset Output High Leakage Current	V_{RES} = 5V			1	µA
V_{CTth}	Delay Comparator Thereshold			2		V
$V_{CTth, hy}$	Delay Comparator Thereshold Hysteresis			100		mV

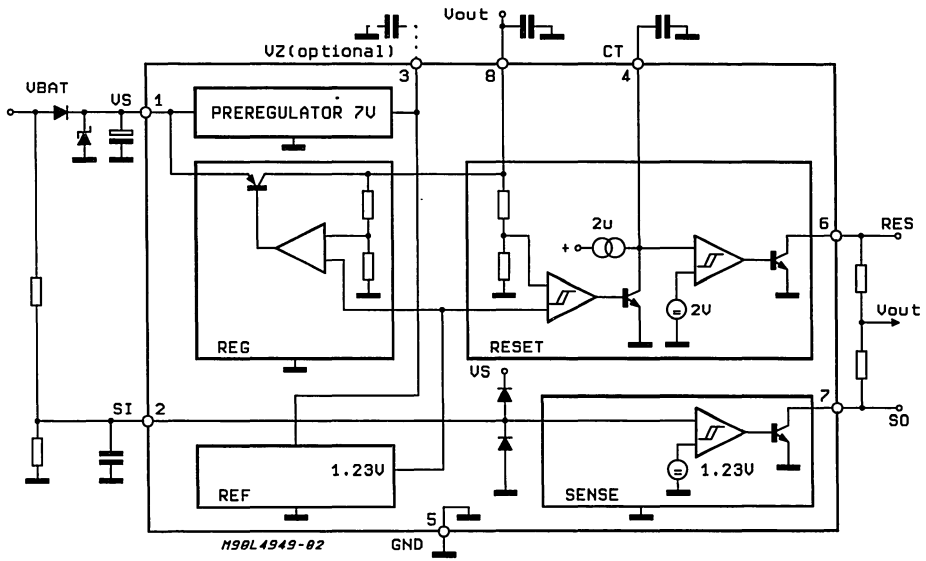
SENSE

V_{st}	Sense Low Thereshold		1.16	1.23	1.35	V
V_{sth}	Sense Thereshold Hysteresis		20	100	200	mV
V_{SL}	Sense Output Low Voltage	V_{SI} ≤ 1.16V; V_S ≥ 3V R_{SO} = 10KΩ to V_O			0.4	V
I_{SH}	Sense Output Leakage	V_{SO} = 5V; V_{SI} ≥ 1.5V			1	µA
I_{SI}	Sense Input Current		-1	0.1	1	µA

PREREGULATOR

V_Z	Preregulator Output Voltage	I_Z = 10µA		7		V
I_Z	Preregulator Output Current				10	µA

APPLICATION CIRCUIT



For stability: C_S ≥ 1µF, C_O ≥ 4.7µF, ESR < 10Ω at 10KHz
Recommended for application: C_S = C_O = 10µF

APPLICATION INFORMATION

Supply Voltage Transient

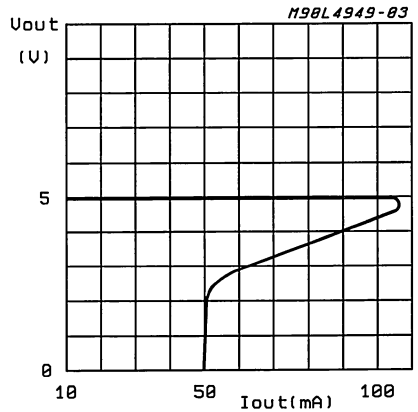
High supply voltage transients can cause a reset output signal disturbation.

For supply voltages greater than 8V the circuit shows a high immunity of the reset output against supply transients of more than 100V/µs.
For supply voltages less than 8V supply transients of more than 0.4V/µs can cause a reset signal disturbation.

To improve the transient behaviour for supply voltages less than 8V a capacitor at pin 3 can be used.

A capacitor at pin 3 (C3 ≤ 1µF) reduces also the output noise.

Figure 1: Foldback Characteristic of V_O



FUNCTIONAL DESCRIPTION

The L4949 is a monolithic integrated voltage regulator, based on the STM modular voltage regulator approch. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. Nevertheless, it is suitable also in other applications where the present functions are required. The modular approach of this device allows to get easily also other features and functions when required.

Voltage Regulator

The voltage regulator uses an Isolated Collector Vertical PNP transistor as a regulating element. With this structure very low dropout voltage at currents up to 100mA is obtained. The dropout operation of the standby regulator is maintained down to 3V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 35V. With this feature no functional interruption due to overvoltage pulses is generated.

The typical curve showing the standby output voltage as a function of the input supply voltage is shown in Fig. 2.

The current consumption of the device (quiescent current) is less than 200µA.

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled, the quiescent current as a function of the supply input voltage is shown in Fig. 3.

Preregulator

To improve the transient immunity a preregulator stabilized the internal supply voltage to 7V. This internal voltage is present at Pin 3 (V_Z). This voltage should not be used as an output because the output capability is very small (≤10µA). This output may be used as an option when a better transient behaviour for supply voltages less than 8V is required (see also application note). In this case a capacitor (100nF - 1µF) must be connected between Pin 3 and GND. If this feature is not used Pin 3 must be left open.

Figure 2: Output Voltage vs. Input Voltage

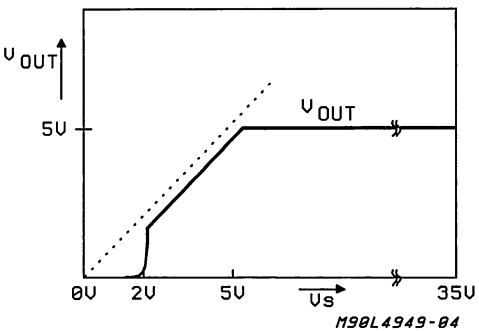
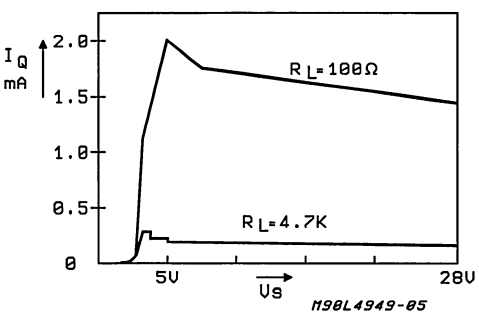


Figure 3: Quiescent Current vs. Supply Voltage



Reset Circuit

The block circuit diagram of the reset circuit is shown in Fig. 4. The reset circuit supervises the output voltage. The reset thereshold of 4.5V is defined with the internal reference voltage and standby output drivider.

The reset pulse delay time t_{RD}, is defined with the charge time of an external capacitor C_T:

$$t_{RD} = \frac{C_T \cdot 2V}{2\mu A}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T.

The reaction time of the reset circuit increases the noise immunity. Standby output voltage drops below the reset threshold only a bit longer than the reaction time results in a shorter reset delay time. The nominal reset delay time will be generated for standby output voltage drops longer than approximately 50µs.
The typical reset output waveforms are shown in Fig. 5.

Sense Comparator

The sense comparator compares an input signal with an internal voltage reference of typical 1.23V. The use of an external voltage divider makes this comparator very flexible in the application. It can be used to supervise the input voltage either before or after the protection diode and to give additional informations to the microprocessor like low voltage warnings.

Figure 4

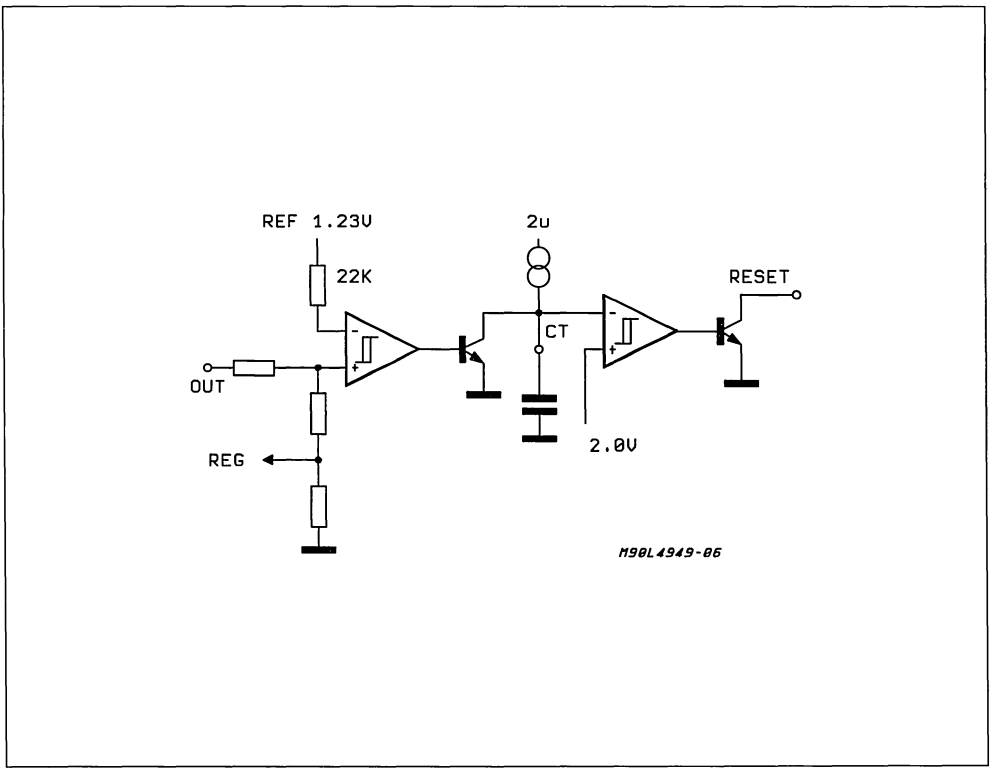
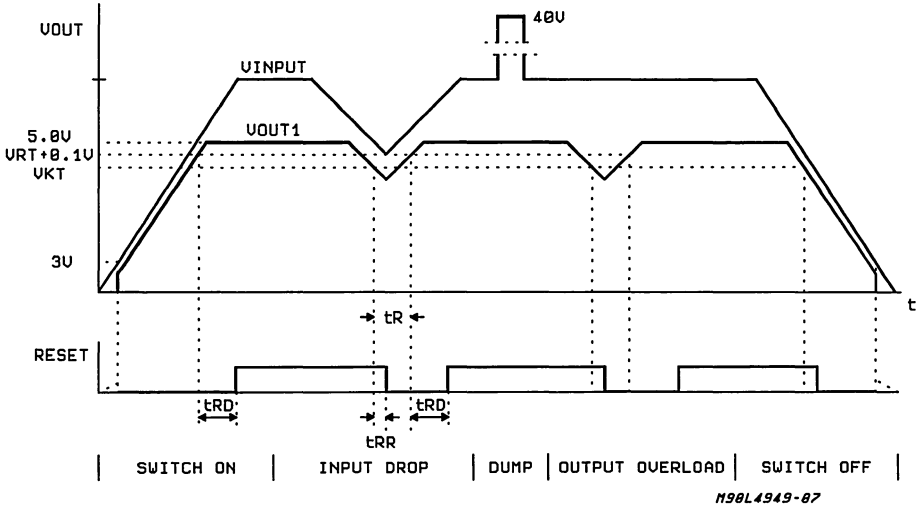
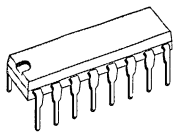


Figure 5


VOUT
40V
VINPUT
VOUT1
5.8V
VRT+0.1V
VKT
3V
t
tR
RESET
tRD
tRD
tRR
SWITCH ON
INPUT DROP
DUMP
OUTPUT OVERLOAD
SWITCH OFF
M98L4949-07

QUAD INVERTING TRANSISTOR SWITCH

- OUTPUT VOLTAGE TO 50V
- OUTPUT CURRENT TO 1.2A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL SUPPRESSION DIODE



Powerdip (12+2+2)

ORDERING NUMBER : L9222

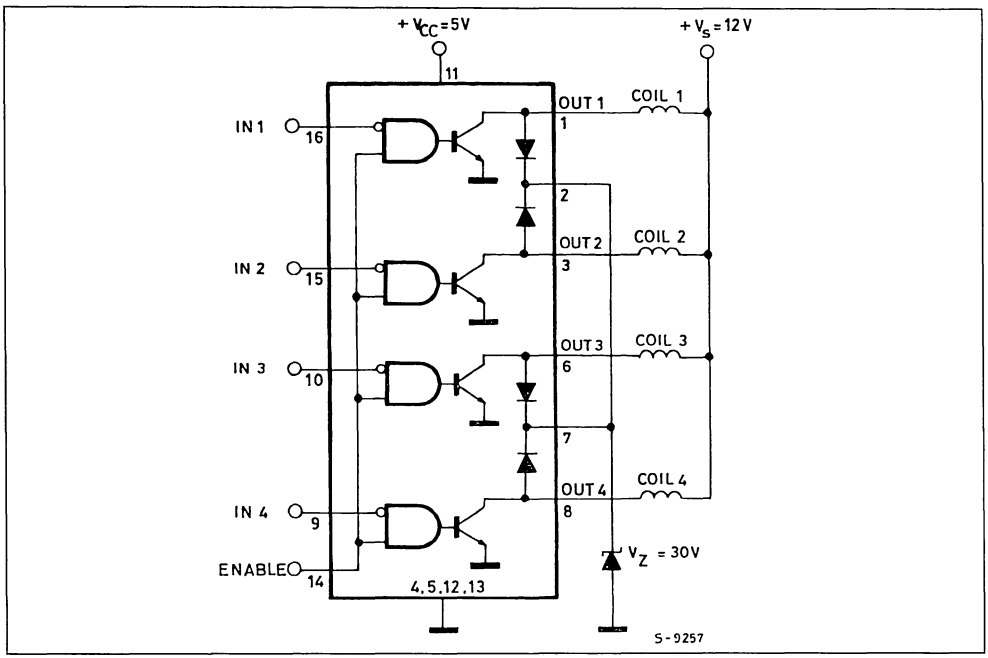
DESCRIPTION

The L9222 monolithic quad transistor switch is designed for high current, high voltage switching applications.

Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits. Each switch consists of an open-collector transistor plus a clamp diode for applications with inductive loads.

The emitters of the four switches are connected together to GND. The switches of the same device may be paralled. The device is intended to drive coils such as relays, solenoids, unipolar stepper motors, LED etc.

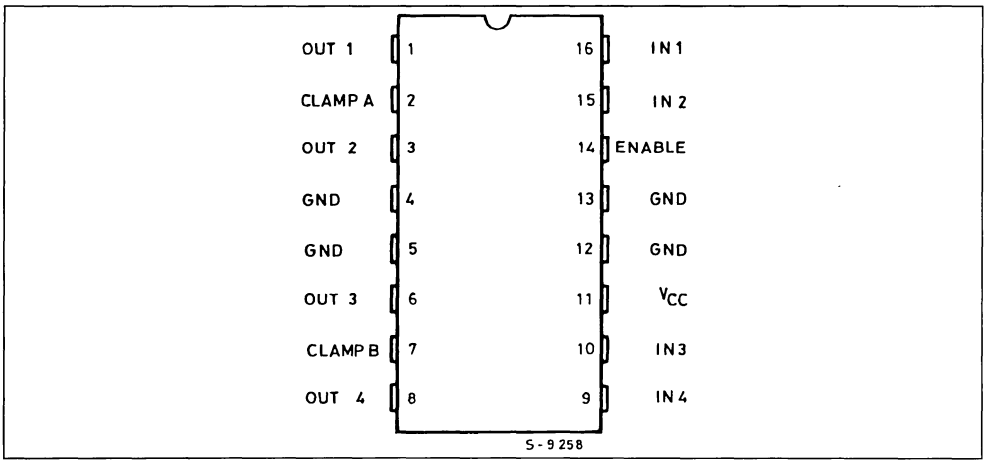
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{OUT}	Output Voltage	– 0.7 to 50	V
V_{CC}	Logic Supply Voltage	7	V
V_i	Input Voltage	– 0.7 to V_{CC} + 0.3	V
T_j, T_{ST}	Junction and Storage Temperature Range	– 55 to 150	°C

PIN CONNECTION (top view)



TRUTH TABLE

Enable	Input	Power Out
H	L	ON
H	H	OFF
L	X	OFF

For each input : H= High level
L= Low level
X = Don't care

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	90	°C/W
$R_{th\text{-}J\text{-}case}$	Thermal Resistance Junction-case	Max	14	°C/W

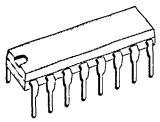
ELECTRICAL CHARACTERISTICS

(V_{CC} = 5Vdc ± 5% V_{EN} = 5V – 40 ≤ T_j ≤ 105°C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{CE(sus)}$	Output Sustaining Voltage	V_{IN} = 2V V_{EN} = 2V I_{OUT} = 100mA		46			V
I_{CEX}	Output Leakage Current	V_{CE} = 50V V_{IN} = 2V, V_{EN} = 0.8V				1	mA
$V_{CE(sat)}$	Collector Emitter Saturation	V_{IN} ≥ 0.8V	I_{OUT} = 0.1A			0.3	V
			I_{OUT} = 0.3A			0.5	
			I_{OUT} = 0.6A – 40 + 105°C			0.8	
V_{IL}	Input Low Voltage					0.8	V
I_{IL}	Input Low Current	V_{IN} = 0.4V		– 15			µA
V_{IH}	Input High Voltage			2.0			V
I_{IH}	Input High Current	V_{IN} ≥ 2.0V		– 15			µA
I_S	Logic Supply Current	All Outputs ON I_{OUT} = 06A			50	90	mA
		All Outputs OFF			10	20	mA
I_R	Clamp Diode Leakage Current	V_R = 50V Diode Reverse Voltage				100	µA
V_F	Clamp Diode Forward Voltage	I_F = 0.6A				1.8	V
		I_F = 1.2A				2.0	
I_{OUT}	Output Current	V_{IN} = 0.4V, V_S = 13V R = 10Ω		0.9	1.2		A
T_{PHL}	Propagation Delay Time (high to low transition)	T_j = 25°C I_L = 600mA				20	µs
T_{PHL}	Propagation Delay Time (low to high transition)	I_L = 600mA T_j = 25°C				20	µs
V_{ENL}	Low Enable Voltage					0.8	V
I_{ENL}	Low Enable Current	V_{EN} = 0.4V		– 15			µA
V_{ENH}	High Enable Voltage			2.0			V
I_{ENH}	High Enable Voltage	V_{EN} ≥ 2.0V		– 15		15	µA

DUAL HIGH CURRENT RELAY DRIVER

- HIGH OUTPUT CURRENT
- HYSTERESIS INPUT COMPARATOR WITH WIDE RANGE COMMON MODE OPERATION AND GROUND COMPATIBLE INPUTS
- INPUT COMPARATOR HYSTERESIS
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS
- INTERNAL OUTPUT OVERVOLTAGE CLAMPING
- SINGLE SUPPLY VOLTAGE (3.5V up to 18V)



Powerdip (8 + 8)

ORDERING NUMBER : L9305A

DESCRIPTION

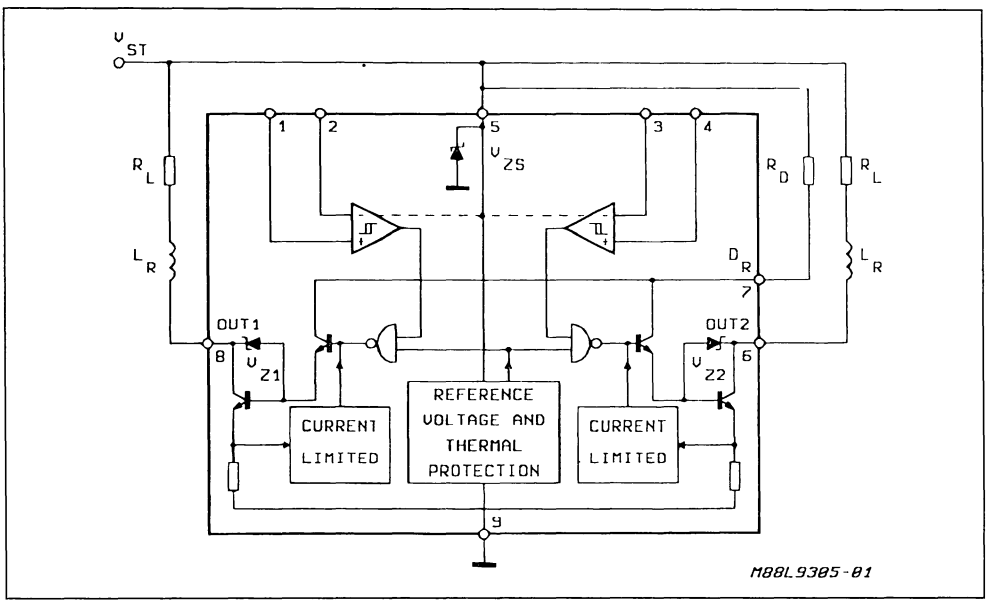
The L9305A is a monolithic interface circuit with differential input comparator and open collector output able to sink high current specifically to drive relays, lamps, d.c. motors.

Particular care has been taken to protect the device against destructive failures - short circuit of outputs to V_S, output overvoltages, supply overvoltage.

A built in thermal shut-down switches off the device when the IC's internal dissipation becomes too great and the chip temperature exceeds a set security threshold.

A hysteresis input comparator increases the interface's noise immunity, allowing the correct use also in critical environments as automotive or industrial applications.

BLOCK DIAGRAM

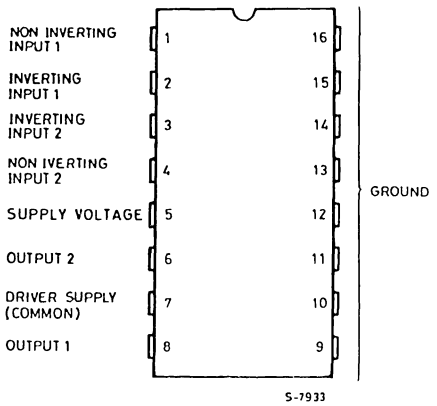


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_5	Supply Voltage	(*) 20	V
V_7	Driver Supply Voltage	26	V
I_{ZS}	Supply Zener Clamp Current (DC) (PULSED) (**)	30 80	mA mA
V_I	Comparator Input Voltage Range	– 0.2 to 24	V
V_I	Differential Input Voltage	24	V
T_j, T_{stg}	Junction and Storage Temperature	– 55 to 150	°C
P_{tot}	Power Dissipation at T_{amb} = 85°C	928	mW
I_o	Output Current	Int. limited	

(*) The maximum allowed supply voltage without series resistors is limited by the built-in zener protection diodes
(**) $T_{on} \leq 2.5$ ms ; repetition time ≥ 30 ms

PIN CONNECTION (top view)



THERMAL DATA

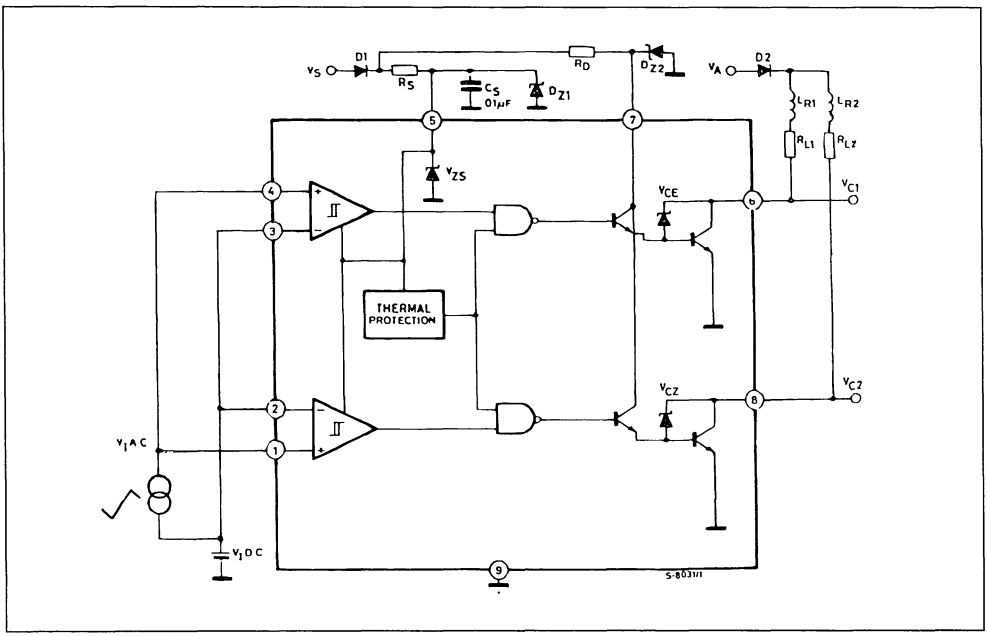
$R_{thj\text{-}pins}$	Thermal Resistance Junction-pins	Max	15	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W

ELECTRICAL CHARACTERISTICS (V_5 = 14.4V, T_{amb} = 25°C ; refer to block diagram unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_5	Supply Voltage		3.5		18*	V
I_S "st.by"	Supply Current	$V_I^+ - V_I^- \geq 70mV$		5	8	mA
I_{SON}	Supply Current	$V_I^- - V_I^+ > 70mV$		18	30	mA
V_{CZ}	Output Clamping Voltage (for each channel)	I_{OUT} = 1A	20		27	V
V_{ZS}	Supply Voltage Clamp	I_{ZS} = 10mA	20		27	V
V_{IH}	Comparator Hysteresis	$V_I^+ - V_I^-$ = 200mVpp f = 1kHz	20		70	mV
I_B	Input Bias Current	$V^+ = V^- = 0V$		0.2	1	µA
I_{OS}	Input Offset Current	$V^+ = V^- = 0V$		± 20	± 200	nA
CMR	Input Common Mode Range	V_5 = 3.5V to 18V	0		V_5 – 1.6	V
I_{SC}	Output Short Circuit Current for Each Channel	$V_I^- - V_I^+ \geq 70mV$ V_{out} = 16.5V			0.85	A
		V_{out} = 6V			2.5	A
I_{CD}	Driver Transistor Current Capability	$V_I^- - V_I^+ \geq 70mV$ DC			300	mA
		Pulsed (**)			600	mA
V_{CSAT}	On Status Saturation Voltage	$V_I^- - V_I^+ \geq 70mV$ I_{CD} = 100mA I_{COUT} = 1.2A			1	V
I_{OL}	Output Leakage Current	$V_I^+ - V_I^- \geq 70mV$			250	µA

* $T_{ON} \leq 2.5$ ms ; repetition time ≥ 30 ms.
** The maximum allowed supply voltage without limiting resistors is limited by the built-in protection zener diodes see V_{CZ}, V_{ZS} Spec velues

TEST AND APPLICATION CIRCUIT



APPLICATION INFORMATIONS (refer to application circuit)

D1 and D2 diodes are required only for reverse polarity protection.

If V_S may be higher than V_{ZS} a resistor R_S is necessary to limit the zener current I_{ZS}. In order to determine R_S value the following equations can be used :

1) $$\frac{V_{S\,MAX} - V_{D1} - V_{ZS\,min}}{R_S} < I_{ZS\,MAX}$$

2) $V_{S\,min} - V_{D1} - R_S - I_{SON\,MAX} > V_{ST\,min}$

where from T_{amb} = 25 °C :

- $V_{S\,MAX}$ and $V_{S\,min}$ are the maximum and minimum values of power supply voltage
- V_{D1} is the forward diode D1 voltage drop
- $V_{ZS\,min}$ = 20 V
- $I_{ZS\,MAX}$ = 30 mA for d.c. mode and $I_{ZS\,MAX}$ = 80 mA for pulsed mode (see Absolute maximum ratings)
- $I_{SOM\,MAX}$ = 30 mA
- $V_{ST\,min}$ = 3.5 V

If no R_S value can satisfy the system 1), 2) a more powerfull external zener D_Z = 18 V is required.

Then 1) becomes :

$$\frac{V_{S\,MAX} - V_{D1} - 18}{R_S} < I_{DZ\,MAX}$$

where $I_{DZ\,MAX}$ is the maximum allowed D_Z current.

V_A voltage cannot be higher than 20 V otherwise output overvoltage protection may be activated. Morever V_A must be less than 16 V if short circuit protection is required.

D_{Z2} = 22 to 24 V is a mandatory for output 7 protection if V_S may be higher than 26 V.

MOUNTING INSTRUCTION

The L9305A is assembled in a new plastic package, the Powerdip, in which 8 pins (from 9 to 16) are attached to the frame and remover the heat produced by the chip.

Figure 2 and 3 show two ways of heatsinking. In the first case, a PC board copper area is used as a heatsink l = 65 mm. While in the second case, the device is soldered to an external heatsink. In both examples, the thermal resistance junction-ambient is 35 °C/W.

Figure 2 : Example of Heatsink Using PC Board Copper (l = 65 mm).

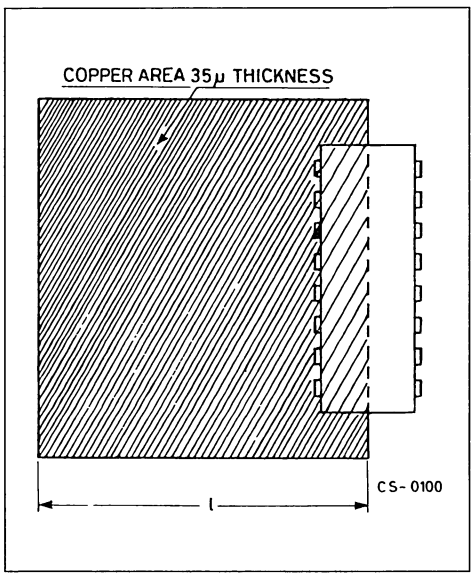
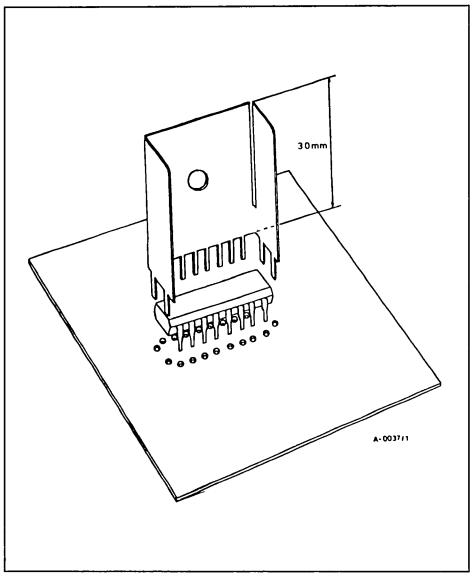
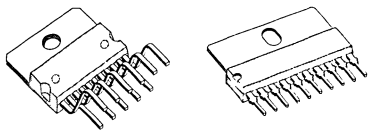


Figure 3 : Example of an External Heatsink.



DUAL HIGH CURRENT LOW SIDE DRIVER

- HIGH OUTPUT CURRENT
- INPUT COMPARATOR WITH WIDE RANGE COMMON MODE OPERATION AND GROUND COMPATIBLE INPUTS
- INPUT COMPARATOR HYSTERESIS
- SHORT CIRCUIT PROTECTION WITH SOA PROTECTION OF OUTPUT
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS
- SINGLE SUPPLY VOLTAGE (3.5 V to 28V)



Multiwatt 11 **SIP 10**

ORDERING NUMBERS:

L9307 L9309

DESCRIPTION

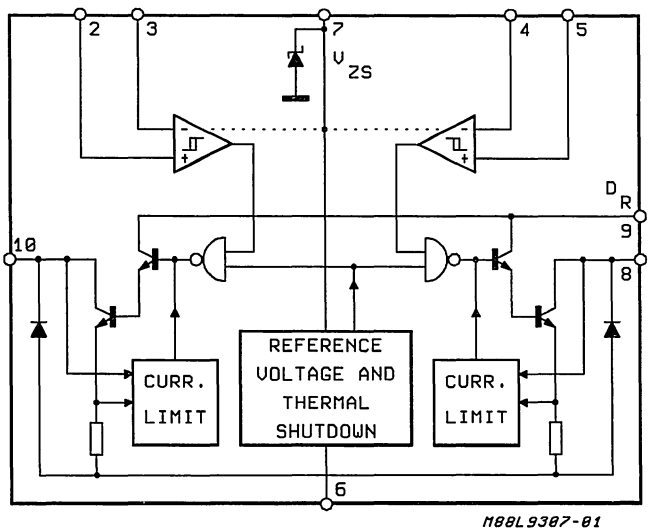
The L9307/9 is a monolithic integrated circuit with differential input comparator and open collector output able to sink high current specially to drive relays, lamps, d.c. motors.

Particular care has been taken to protect the device against destructive failures, i.c. short circuit of outputs to V_S, SOA protection, supply overvoltage.

A built in thermal shut-down switches off the device when the IC's internal dissipation becomes too high and the chip temperature exceeds security threshold.

The input comparator hysteresis increases the interface's noise immunity allowing the correct use critical environments as automotive applications.

BLOCK DIAGRAM

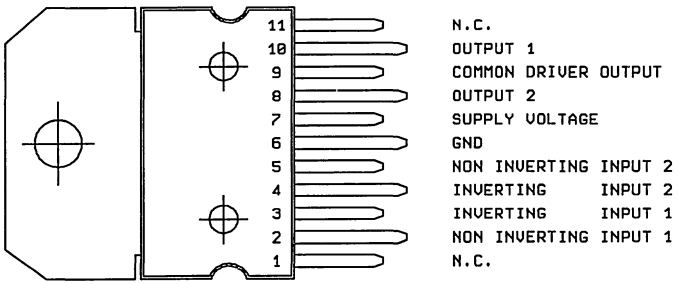


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
I_{ZS}	Current Into Supply Clamp Zener Diode	DC Conditions	30	mA
		Pulsed: Ton < 2.5ms; d < 8%	80	mA
V_S	Supply Voltage		28	V
I_O	Output Current		Internally Limited	°C
T_j, T_{stg}	Junction and Storage Temperature Range		– 55 to 150	°C
V_O 1,2	Output Voltage		– 0.3 to 28	V
P_{tot}	Power Dissipation at T_{amb} = 85°C	**for Multiwatt 11**	1.7	W
		for SIP 10	1.3	W

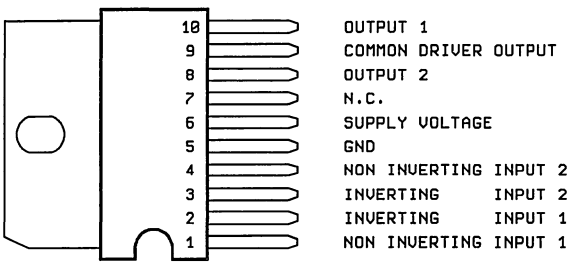
(*) T_{ON} 2.5ms; repetition time ≤ 30ms
(**) The maximum allowed supply voltage without limiting resistor is limited by the built-in protection zener diode· see V_{ZS} spec. values if V_S higher than V_{ZS} a resistor R_S is necessary to limit the zener current I_{ZS}.

PIN CONNECTIONS (Top view)



M88L9387-02

MULTIWATT 11



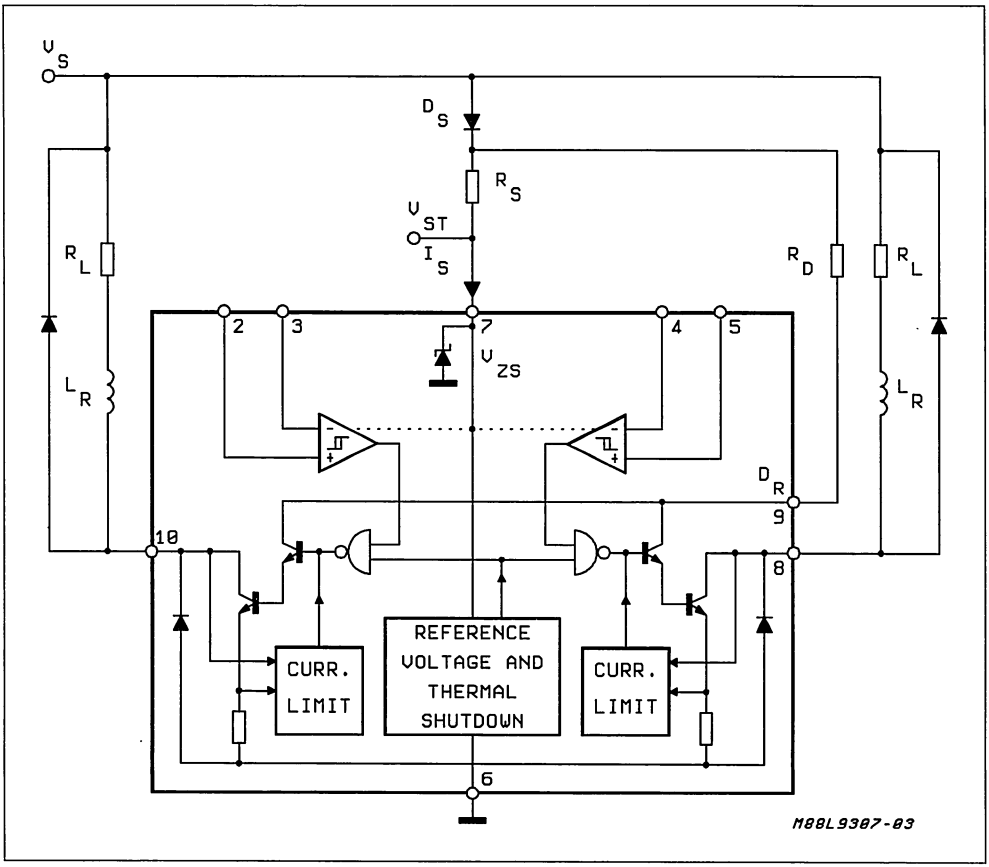
M88L9389-02

SIP 10

THERMAL DATA

Symbol	Parameter		Multiwatt	SIP	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	38	50	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	3	10	°C/W

Figure 1: Typical Application (for SIP 10 version)

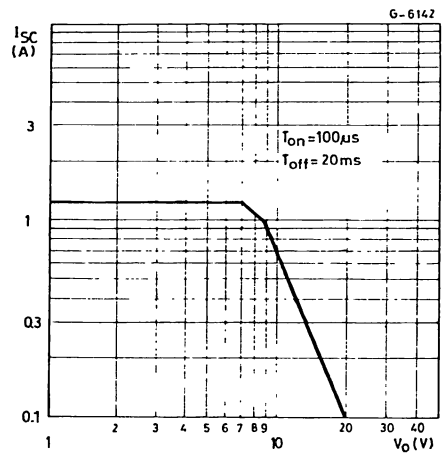


Note: a) RS required only limit I_{ZS} whenever V_S exceeds V_{ZS} voltage value.

ELECTRICAL CHARACTERISTICS (V_S = 14.4V; Tamb = –40°C to 85°C; R_S = 100Ω Refer to the block diagram, unless otherwise specified.)

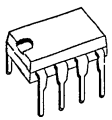
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IH}	Hysteresis of the Input Comparator	Vin = 200mVpp; f = 1KHz	20		80	mV
I_B	Input Bias Current			0.2	1	µA
I_{OS}	Input Offset Current			± 50	± 400	nA
CMR	Input Common Mode Range	V_S = 6 to 18V	0		V_{ST} - 1.6	V
I_{SC}	Output Short Circuit Channel (typ. SOA curve, see fig.2)	$V_I^- - V_I^+ > 70mA$ V_{out} 1, 2 = 16V T_{amb} = 25 to 85°C T_{amb} = –40 to 25°C V_{out} 1,2 = 6V			 0.8 0.9 2.5	 A A A
I_D	Driver Transistor Current Capability	$V_I^- - V_I^+ > 70mA$ V_S = 6 – 16V DC Conditions Pulsed: T_{on} = 2.5ms; d < 8%			 300 600	 mA mA
I_O 1, 2	Output Current for Each Channel	(see fig. 2) Vout 1, 2 < 2V; $V_I^- - V_I^+ > 70mV$ I_d = 100mA	1.5			A
V_{Csat}	On Status Saturation Voltage	$V_I^- - V_I^+ > 70mV$ I_d = 100mA I_{out} 1, 2 = 1.2A			1.2	V
I_{OL}	Output Leakage Current	$V_I^+ - V_I^- > 70mV$ V_S = 18V		10	250	µA
V_{st}	Supply Voltage (pin 7)		3.5		18	V
I "st.by"	Supply Current	$V_I^+ - V_I^- > 70mV$		5	8	mA
I "ON"	Supply Current	$V_I^+ - V_I^- > 70mV$		18		mA
V_{ZS}	Voltage Clamp Supply Protection	I_{ZS} = 10mA	20		27	V

Figure 2: SOA Protection.



DUAL LOW SIDE DRIVER

- DARLINGTON OUTPUT STAGE
- INPUT COMPARATOR WITH WIDE RANGE COMMON MODE OPERATION AND GROUND COMPATIBLE INPUTS
- INPUT COMPARATOR HYSTERESIS
- SHORT CIRCUIT PROTECTION OF OUTPUT WITH SOA PROTECTION
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS
- SINGLE SUPPLY VOLTAGE FROM 3.5V UP TO 28V



MINIDIP

ORDERING NUMBER : L9308

DESCRIPTION

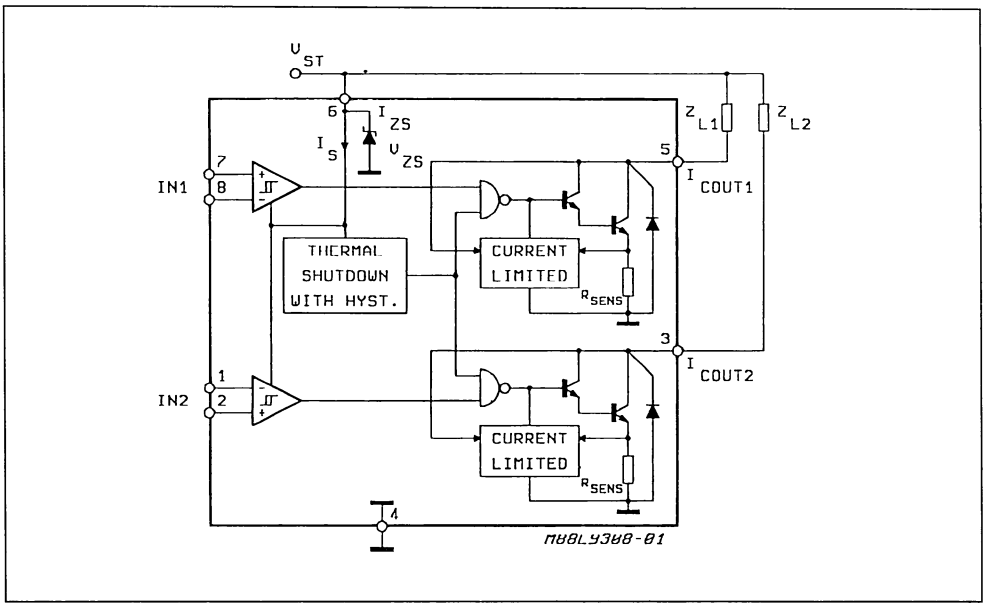
The L9308 is a monolithic interface circuit with differential input comparator and open collector output able to sink current specifically to drive lamps, relays, d.c. motors, electro valves etc.

Particular care has been taken to protect the device against destructive failures - short circuit of outputs to V_S, SOA protection, supply overvoltage.

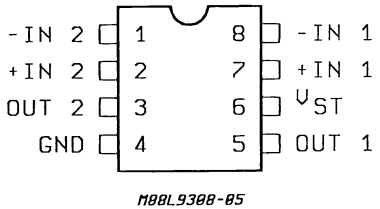
A built in thermal shut-down switches off the device when the IC's internal dissipation becomes too high and the chip temperature exceeds the security threshold.

The input comparator hysteresis increases the interface's noise immunity allowing the correct use in critical environments as automotive applications.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



M88L9308-05

1) -IN2 Inverting input2
2) +IN2 Non-inverting input2
3) OUT2 Output2
4) GND Ground
5) OUT1 Output1
6) V_{ST} Supply
7) +IN1 Non-inverting input1
8) -IN1 Inverting input1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
I_{SZ}	Current Into Supply Clamp Zener Diode	T_{amb} = 25°C, DC Pulsed (*)	30 80	mA mA
V_S	Supply Voltage		28	V(**)
I_O	Output Current		Internally Limited	
T_j, T_{stg}	Junction and Storage Temperature		– 55 to + 150	°C
P_{tot}	Power Dissipation at T_{amb} = 85°C		650	mW

(*) TON ≤ 2.5ms ; repetition time > 30ms.
(**) The maximum allowed supply voltage without limiting resistor is limited by the built-in protection zener diode : see V_{ZS} spec. values. If V_S is higher than V_{ZS} a resistor R_S is necessary to limit the zener current I_{ZS}.

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 14.4V ; – 40°C ≤ T_{amb}, ≤ 85°C; R_S = 100Ω unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Hysteresis of the Input Comparater	V_{IN} = 200mVpp ; f = 1kHz	20		80	mV
I_B	Input Bias Current	$V_I^+ = V_I^- = 0$		0.2	1.0	µA
I_{OS}	Input Offset Current	$V_I^+ = V_I^- = 0$		± 50	± 400	nA
CMR	Input Common Mode Range	V_s = 6 – 18V T_{amb} = 25°C	0		V_{ST} – 1.6	V
I_{SC}	Output Short Circuit Current for Each Channel (see fig. 4)	$V_{IN} - V_{IN}$ > 70mV V_S = 16V T_{amb} = 25°C to 85°C T_{amb} = – 40°C to 25°C $V_{OUT\ 1,2}$ = 6V			 0.6 0.7 1.2	 A A A
V_{CSAT}	On Status Saturation Voltage	T_{amb} = – 40°C to 25°C $V_I^- - V_I^+$ > 70mV $I_{OUT\ 1,2}$ = 300mA T_{amb} = 25°C to 85°C		 1.0	1.5 1.4	V V
I_{OL}	Output Leakage Current	$V_I^- - V_I^-$ > 70mV V_S = 18V V_S = 5V		10	300 20	µA µA
V_{ST}	Supply voltage (pin 6)		3.5		18	V
$I_{-st\ by-}$	Supply Current	$V_I^+ - V_I^-$ > 70mV		5	8	mA
I_{-ON-}	Supply Current	$V_I^- - V_I^+$ > 70mV		18		mA
V_{ZS}	Voltage Clamp Supply Protection	I_{ZS} = 10mA	20		27	V
I_{Omin}	Minimum Output Current with the Outputs connected Together	V_{CSAT} = 1.5V	400			mA
t_r t_f	Rise Time (see fig. 2) Fall Time	I_{OUT} = 50mA T_{amb} = 25°C			2 2	µs
t_{don} t_{doff}	Delay Time On Delay Time Off	I_{OUT} = 50mA T_{amb} = 25°C			10 10	µs

Figure 1 : Switching Time Test Circuit.

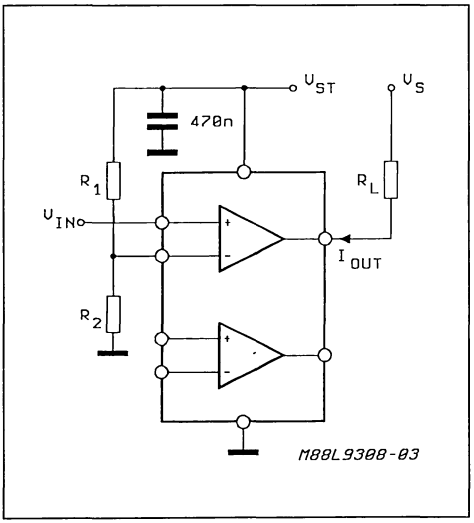


Figure 2 : Switching Time Waveforms for Resistive Loads.

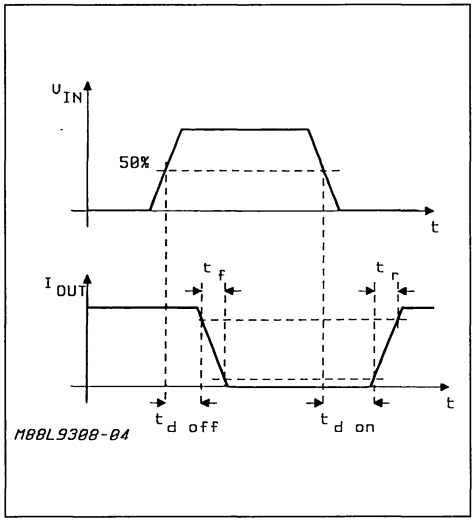
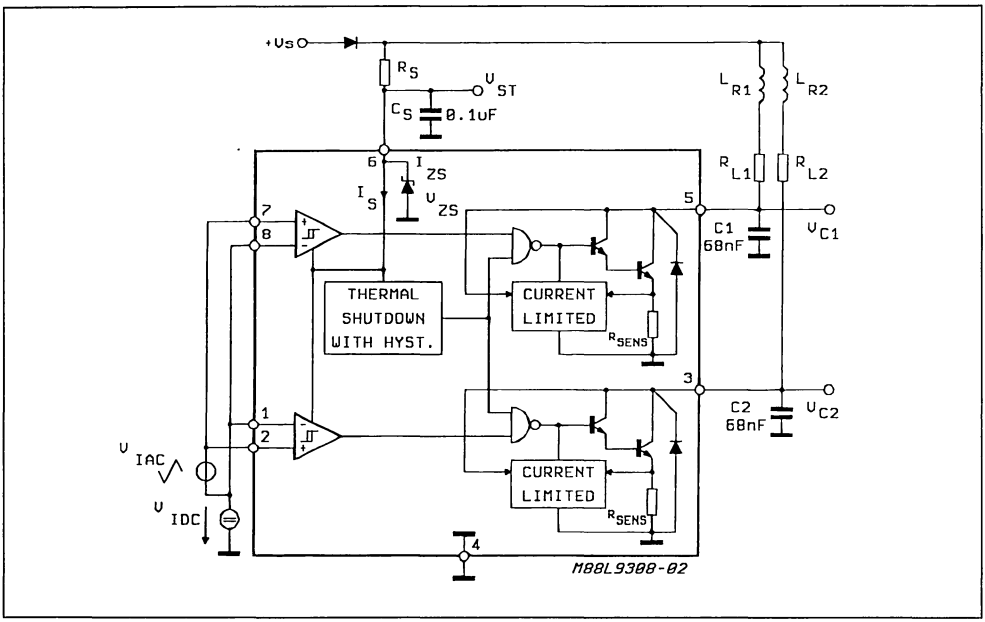
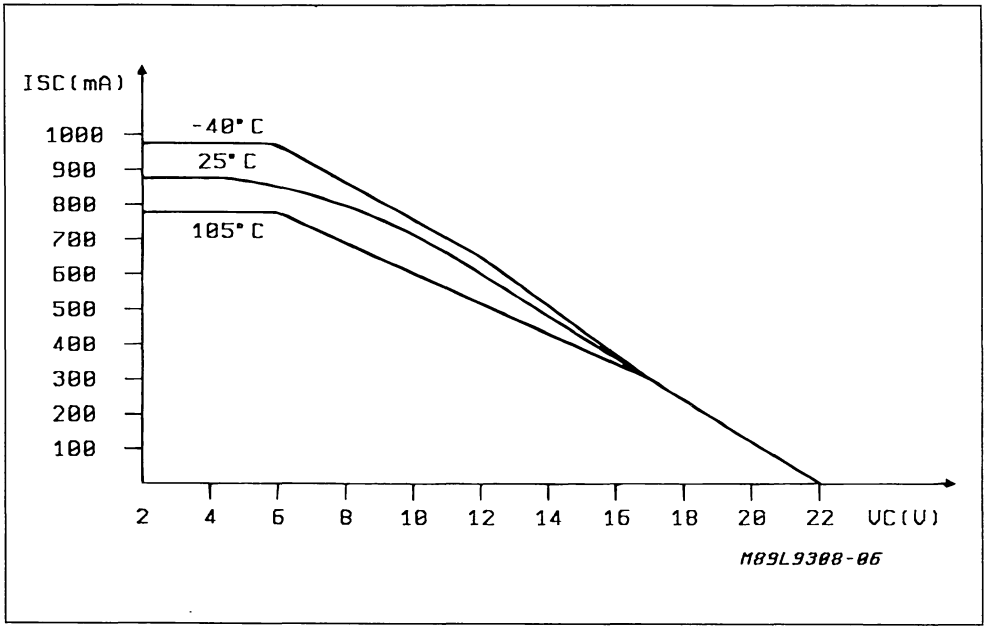


Figure 3 : Typical Application and Test Circuit.



Notes : a) R_S required only to limit I_{ZS} whenever V_S exceeds V_{ZS} voltage value.
b) C_1, C_2 cut high frequency gain during current limitng.

Figure 4 : Typical SOA Characteristic.



WINDOW LIFT CONTROLLER

ADVANCE DATA

- FOUR POWER OUTPUTS - UP TO 200 mA EACH ONE - FOR RELAIS DRIVING PROVIDED WITH INTERNAL RECIRCULATION
- TWO PROGRAMMING INPUTS FOR WINDOWS OPERATING MODE SELECTION
- ONLY TWO WIRES CONNECTING EACH KEYBOARD TO THE DEVICE
- WINDOW STATUS DETECTION BASED ON THE MOTOR CURRENT RIPPLE
- IGNITION KEY AND DOOR STATUS SENSING
- CLOCK FREQUENCY DEFINED BY AN EXTERNAL CAPACITOR
- ESD PROTECTION

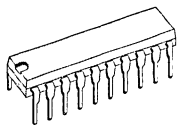
DESCRIPTION

The L9324 is a monolithic low side driver - realized with ST Multipower-BCD mixed technology - specially suited as window lift in automotive environment. The device drives four window motor control relais and it allows two possible window operating modes : the automatic (one touch) and the normal mode.

The window status (steady state, travel end) is checked by means of the ripple absence on the motor current.

The application circuit is able to withstand the load dump up to 80 V.

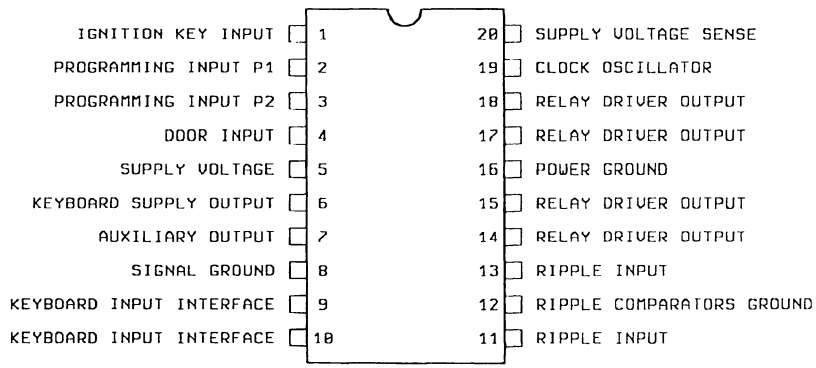
The device is assembled in 20 Lead Plastic DIP.



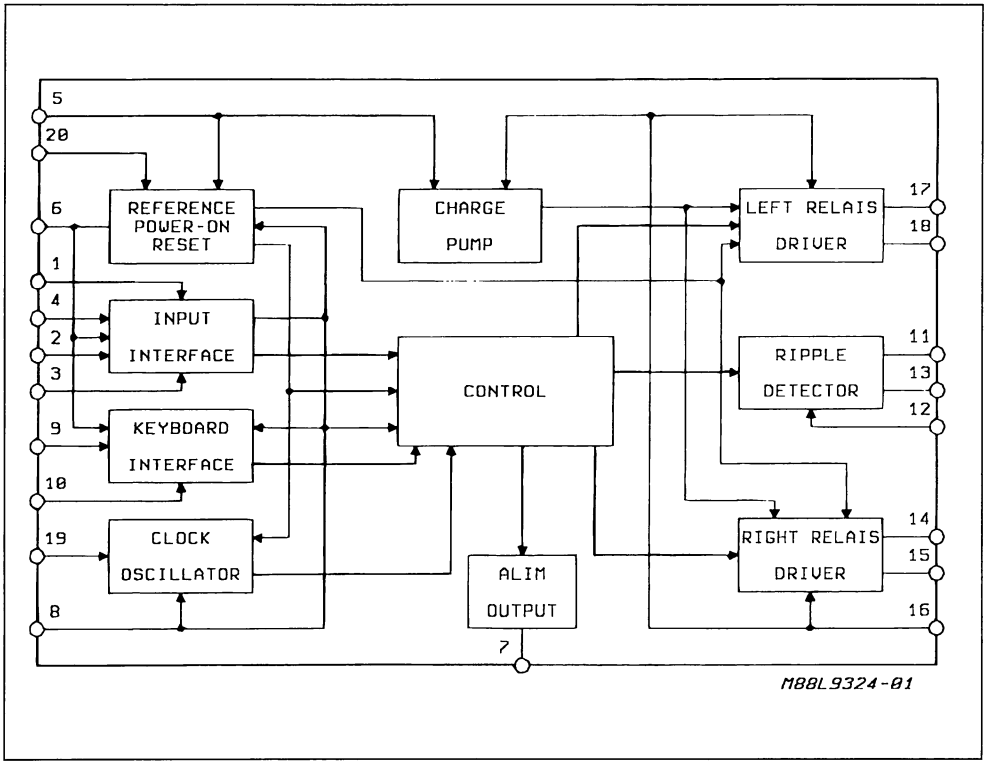
DIP20

ORDERING NUMBER : L9324

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_5	D.C. Supply Voltage D.C. Reverse Supply Voltage	25 – 0.7	V V
$I_{14,15,17,18}$	Max. Relais Driver Output Currents (in dump condition : V_{DUMP} = 80V 5ms ≤ t_{rise} ≤ 10ms) τ_f Fall Time Constant = 100ms R_{SOURCE} ≥ 0.5Ω	1	A
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

THERMAL DATA

$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	80	°C/W

ELECTRICAL CHARACTERISTICS (V_{BATT} = 14V, -20°C ≤ Tamb ≤ 85°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_5	Operating supply Voltage		8		16	V
I_{q5}	Quiescent Current (OFF Condition)			1	2	mA
I_{q5ON}	Quiescent Current (OFF Condition			30		mA
V_{OVth}	(pin 20) Overvoltage Protection Threshold (power output stage		17	22	27	V
$V_{14, 15, 17, 18}$	Relais Driver Output Saturation Voltage	$I_{14, 15, 17, 18}$ = 200mA		0.7	1	V
V_{CZ}	Intrnal Voltage Clamp at the Outputs (pin 14, 15, 17, 18)			26		V
$V_{11, 13th}$	Ripple Detection Threshold		6	20	40	mV
I_{AUX7}	Auxiliary Output Source Current			20		mA
V_6	Keyboard Reference Voltage	0 < I_6 < 100mA	3.8	4.5	5.2	V
I_6	Keyboard Reference Output Current			100	120	mA
R_9, R_{10}	Comparator Input Resistance		30			KΩ
V_{2th}, V_{3th}	Programming Input Threshold Voltage			1.5		V
V_{1th}	Ignition Key Threshold Voltage			1.5		V
V_{4th}	Door Input Thereshold Voltage			50		mV
T	Clock Period	C_{EXT} = 2.2nF	0.5	1.5	2.5	ms
t_{fd1}	Keyboard Filter Delay Time		16T		32T	ms
t_{fd2}	Door and Key Filter Delay Time		32T		64T	ms
t_{dabs}	Delay Time Between the Ripple Absence and the Motor Stop		30T		36T	ms
t_{fd3}	Ripple Filter Delay Time at Motor Start-up		32T		48T	ms
t_{stup}	Start-up Delay Time		50T		182T	ms

FUNCTIONAL DESCRIPTION

PIN FUNCTIONS

1 - Ignition key input. This pin must be connected, through a resistor, to the ignition key ; in this way, at ignition key turn on (high level at pin 1), the full operating mode of the device is enabled. The a.m. resistor, together an internal zener, provides to protect this input in load dump condition ; recommended value for this resistor is 47 K.

2 and 3 - Programming inputs P_1 and P_2. These two pins allow to programme the device operation mode, according to the following truthtable :

P1	P2	Operating Mode
0	X	The device is programmed to work in a rear module. The automatic mode is disabled for both the windows. The high to low transition of a signal applied to pin 4 changes, in this operating mode, the status of the auxiliary output ; the device is enabled only at ignition key turn-on. The input P2 has no effect when P1 is low.
1	1	The device is programmed to work in a front module. The automatic mode is enabled for both the windows if the ign. key is on ; if the key is in off condition, the device works in traditional mode if one of the front doors is open, or it is disabled if both the front doors are closed.
1	0	In this case too the device is programmed to work in a front module. The operating mode is as for the last case but the automatic mode, when enabled, is possible only for the left window.

Note : a logic level 0 in the above table means the pin connected to ground ; a logic level 1 means the pin open ; X = don't care.

4 - Door input. This input senses the doors status (open or close) when the device is programmed to work in a front module. This pin must be connected, via an external resistor, to the door switch normally present on all the cars for the inside lamp. A low voltage level on this input means that the door is open (inside lamp on), an high voltage level means that the door is closed (inside lamp off). In the rear module this pin is connected to a push button which allows to enable and disable the module. The external resistor, together an internal zener, provides to protect the input against overvoltages ; recommended value for the external resistor is 100 ohms.

5 - Supply voltage. This pin must be connected to the battery through a voltage limiter not to damage the device in load dump conditions (see the application circuit).

6 - Keyboard supply output. The voltage on this pin is about 4 V and the output current capability is 100 mA. An internal divider connected to this same voltage source generates the 4 thresholds for the keyboards interface input. This pin is connected to the two keyboards through two resistors (recommended value 100 ohms).

7 - Auxiliary output. This output, by an external transistor, drives the relay necessary to enable the rear keyboard when the device works in a rear module. The output current capability of this output is 20 mA.

8 - Signal ground.

9 and 10 - Keyboards input interfaces. This two pins are respectively connected to the left and to the right keyboard ; pushing one of the 4 pushbuttons of each keyboard a voltage is established on this pins. The device "understands", by this voltage level, which pushbutton has been pressed and execute the command. This concept allows to have many functions with a limited number of wires between the module and the keyboards. The voltage levels of the keyboards are then function of the pressed pushbutton as follow :

- traditional up.....3/4 * V_{pin6}
- automatic up.....1/2 * V_{pin6}
- traditional down.....1/4 * V_{pin6}
- automatic down.....0

The recommended values of the keyboards resistor necessary to have the a.m. values are respectively 180, 68 and 33 ohms (see schematic diagram).

11 and 13 - Ripple inputs. These inputs sense respectively the ripple of the right and the left motor through 2 decoupling capacitors connected to the sense resistors.

12 - Ripple comparators ground. This pin must be connected directly to the sense resistor ground, so to avoid bad operations of the ripple comparators.

14, 15, 17 and 18 - Relay driver outputs. These outputs control the relais to drive the window motors in the correct way. The 4 power devices are also switched on during the relais current recirculation and in overvoltage condition to protect themselves. In this way the device can withstand overvoltages up to 80 V (t = 300 msec), because the current flowing in the output power devices is limited by the relais resistance.

16 - Power ground. This pin is internally connected to the common power ground of the relay driver outputs.

19 - Clock oscillator. A capacitor connected bet-

ween this pin and ground set the clock frequency necessary for the correct operation of the internal logic. Recommended value for this capacitor is 2.2 nF.

20 - Supply voltage sense. This pin, connected by an external resistor to the battery supply voltage, allows the device to sense overvoltages ; in this condition, as said above, all the relay drivers are switched on to protect themselves.

APPLICATION INFORMATION

The L9324 can perform two possible window operating modes : the normal and the automatic mode. In the normal operating mode the window goes up or down until the keyboard push-button is pushed and the window is not stopped by obstacles. In the automatic mode, even after releasing the keyboard push-button, the window continues its movement that is interrupted if another push-button is pushed or by an obstacle. The window status (steady state, travel end) is detected by the absence of the ripple on the motor current. The delay time between the ripple absence and the motor switch off is about 50 ms. During the starting phase the motor is driven up to 250 ms even if the ripple is not present.

The complete window lift system using L9324 is based on two modules, one for the front windows and the other for the rear ones.

The possible operating modes, set by the programming inputs P_1 and P_2, are shown in the following diagram.

Figure 1 : Operating Modes.

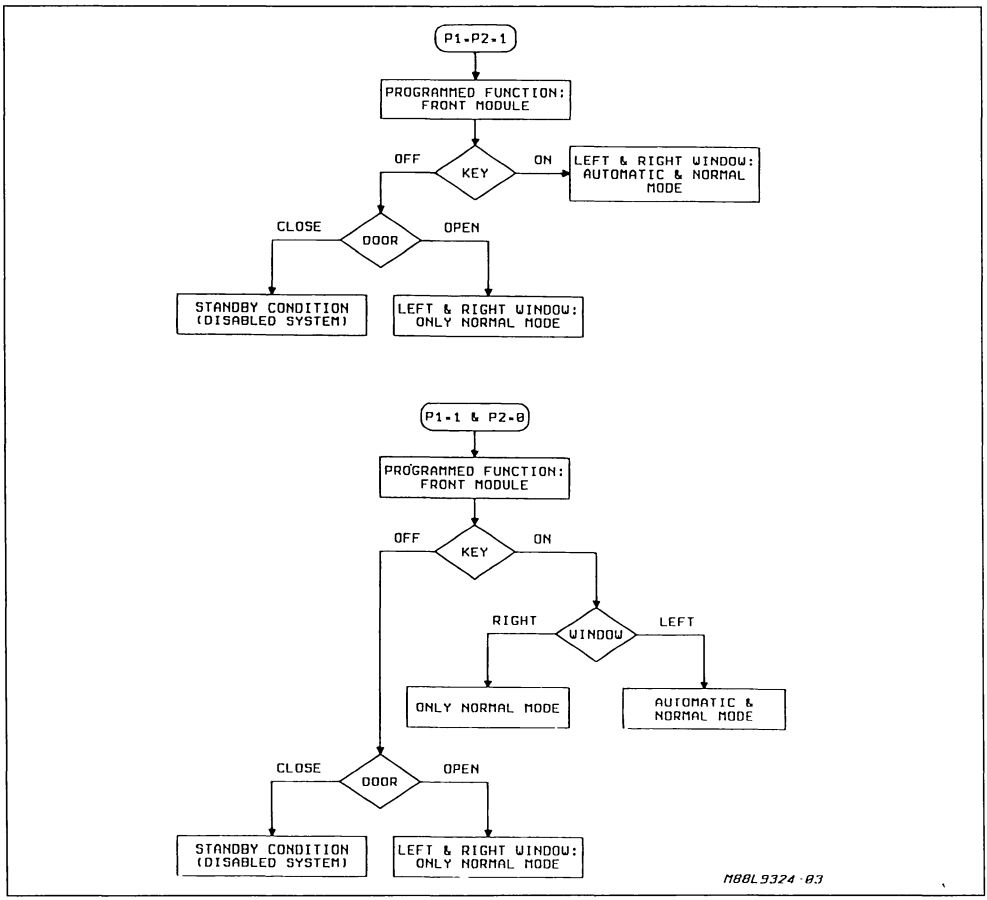


Figure 2 : Operating Modes.

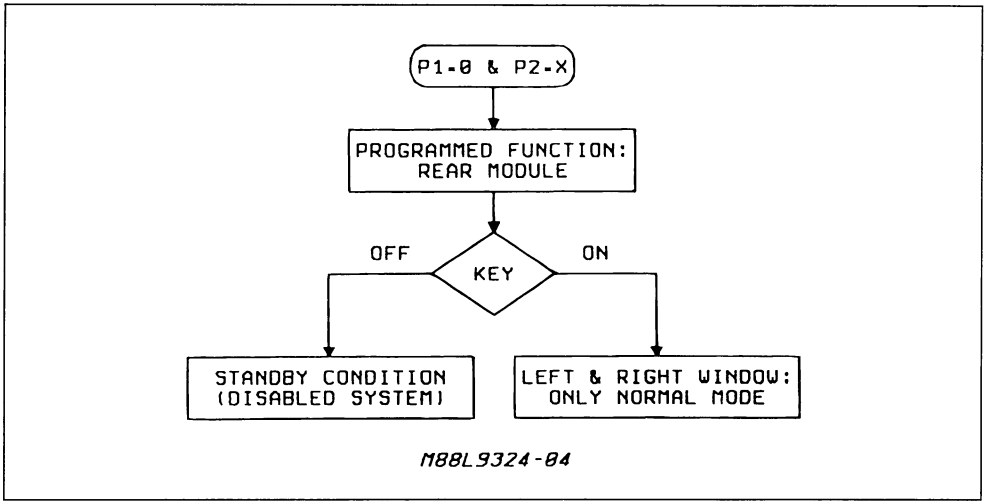


Figure 3 : Application Circuit.

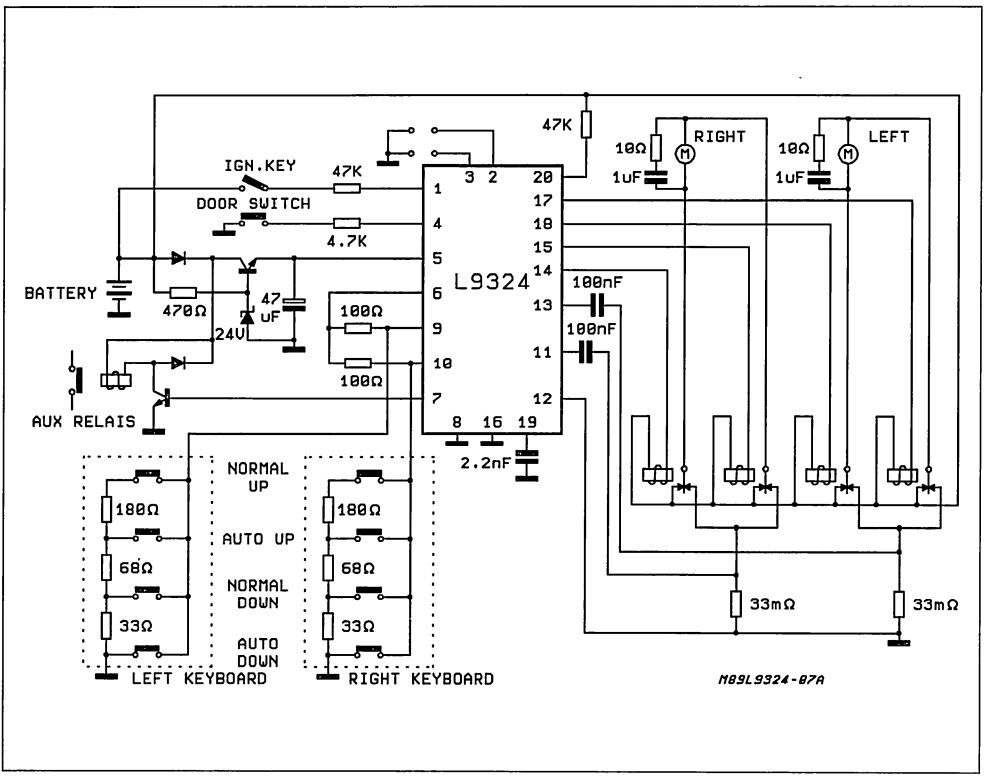
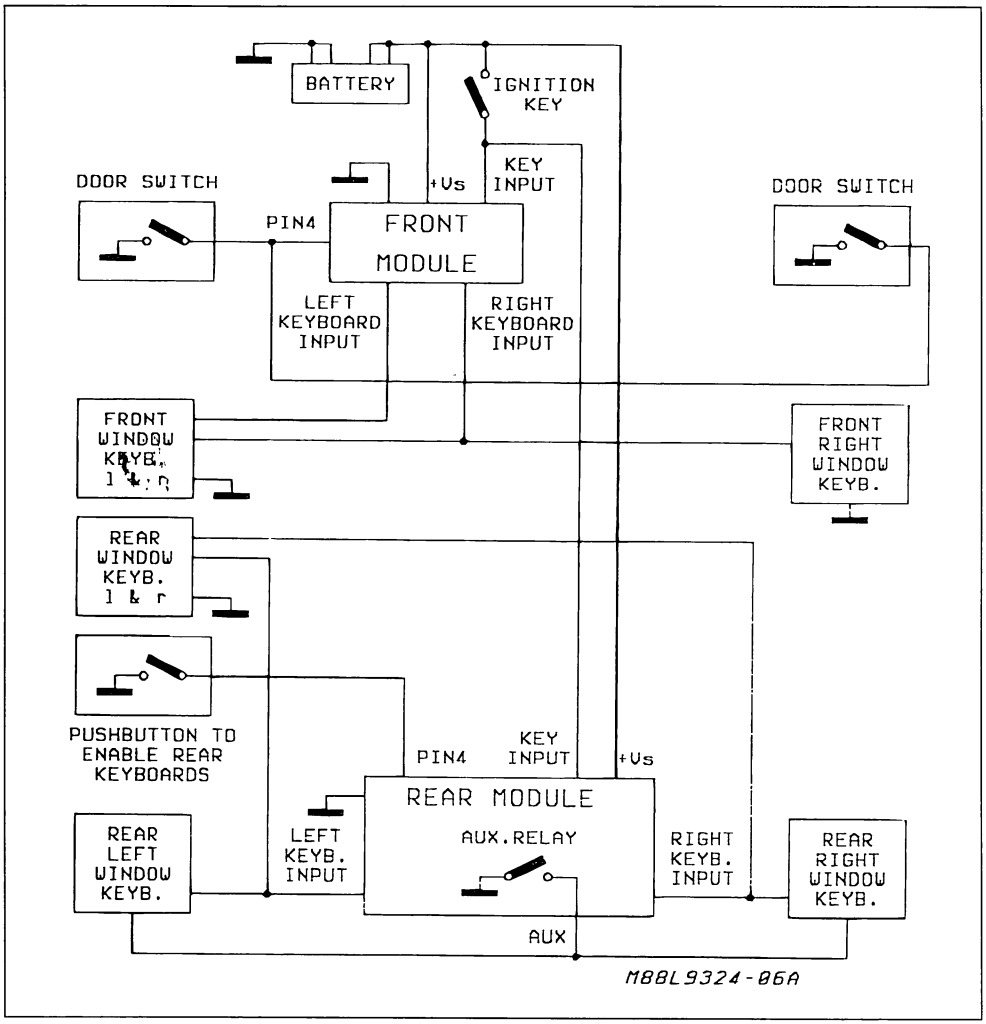


Figure 4 : Complete Window Lift System.

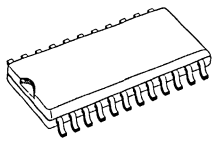


DUAL INTELLIGENT POWER LOW SIDE SWITCH

PRODUCT PREVIEW

- DUAL POWER LOW SIDE DRIVER WITH LOW R_{DSON} TYPICALLY 250mΩ (T_J = 25°C)
- INTERNAL OUTPUT CLAMPING DIODES V_{FB} = 50V FOR INDUCTIVE RECIRCULATION
- LIMITED OUTPUT VOLTAGE SLEW RATE FOR LOW EMI
- µP COMPATIBLE ENABLE AND INPUT
- WIDE OPERATING SUPPLY VOLTAGE RANGE 6.5V TO 40V
- REAL TIME DIAGNOSTIC FUNCTIONS:
  - OUTPUT SHORTED TO GND
  - OUTPUT SHORTED TO VSS
  - OPEN LOAD
  - OVERTEMPERATURE
- DEVICE PROTECTION FUNCTIONS
  - OVERLOAD DISABLE
  - THERMAL SHUTDOWN

MULTIPOWER BCD TECHNOLOGY



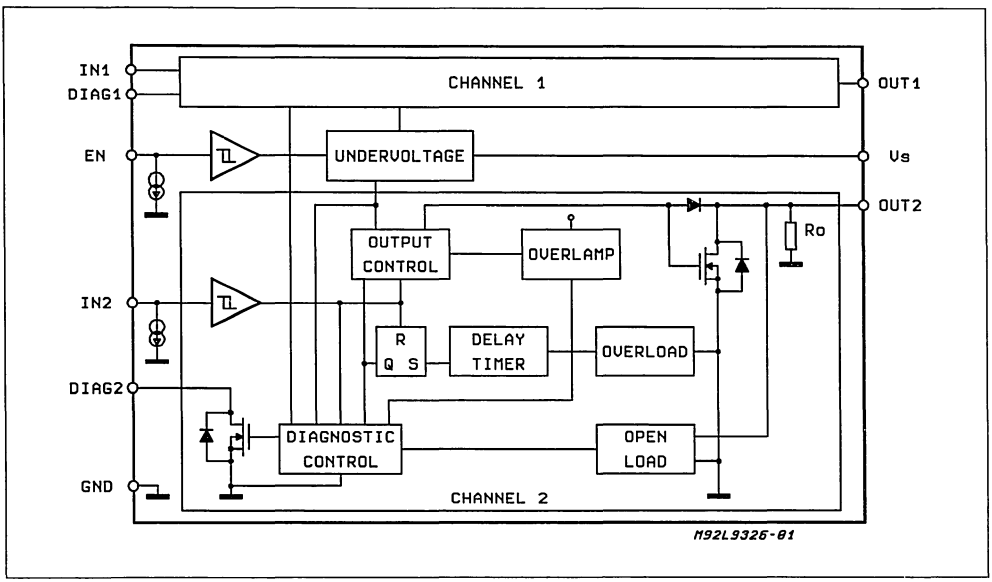
SO24 (16+4+4)

ORDERING NUMBER: L9326

DESCRIPTION

The L9326 is a monolithic integrated dual low side driver realized in an advanced Multipower-BCD mixed technology. It is especially intended to drive valves in automotive enviroment. Its inputs are µP compatible for easy driving. Particular care has been taken to protect the device against failures, to avoid electro-magnetic interferences and to offer extensive real time diagnostic.

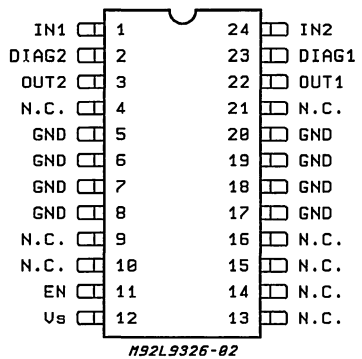
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{SDC}	DC Supply Voltage	– 1.5 to 40	V
VS_{TR}	Transient Supply Voltage $t \leq 500ms$	60	V
VIN,EN	Input Voltage |10mA|	– 1.5 to 6	V
I_O	Output Load Current	internal limited	
VO_{DC}	DC Output Voltage	45	V
VO_{TR}	Transient Output Voltage $R_L \geq 4\Omega$	60	V
IOR	Reverse Output Current (limited by load)	– 4	A
UD_{DC}	Diagnostic DC Output Voltage	– 0.3 to 20	V
EO	Switch-off energy $t_{EO} = 250ms$, $t = 5ms$	50	mJ
T_{JEO}	Junction Temperature during Switch-off	175	°C
T_j	Junction Temperature	– 40 to +150	°C
T_{stg}	Storage Temperature	– 55 to +150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter	Value	Unit
T_{JDIS}	Thermal Disable Junction Temperature Threshold	160 to 190	°C

ELECTRICAL CHARACTERISTICS (Operating range: 6.5V < VS ≤ 32V (45V for t ≤ 500ms), – 40°C ≤ T_J ≤ 150°C unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
IO_u	Open Load Current	$V_{EN} = V_{IN} = H$	2.5	125	250	mA
VO_u	Open Load Voltage	$V_{EN} = H$, $V_{EN} = L$	0.525V_S	0.55V_S	0.575V_S	
IO_O	Over Load Current Threshold	$T_j \leq 150°C$	5			A
RO	Internal Output Pull Down	$V_{EN} = L$	14	20	36	kΩ
$V_{(EN,IN)L}$	Logic Input Low Voltage	VS > 4.5V $I_{EN,IN} \leq 10mA$	– 1.5		1	V
$V_{(EN,IN)H}$	Logic Input High Voltage	VS > 4.5V	2		5.5	V
$V_{(EN,IN)hys}$	Logic Input Hysteresis	VS > 4.5V	0.2	0.4		V
I_{EN}	Logic Input Sink Current	VS > 4.5V $0.5V \leq V_{EN} \leq 5.5V$	21	30	39	µA
I_{IN}	Logic Input Sink Current	VS > 4.5V $0.5V \leq V_{IN} \leq 5.5V$	70	100	130	µA
R_{DSON}	Output on Resistance	$T_j = 150°C$ VS > 9.5V $I_O = 2A$		400	500	mΩ
VO_C	Output Voltage During Clamping		45	52	60	V
IS_{SB}	Static Standby Supply Current	$V_{EN} = L$		0.4	1	mA
IS	DC Supply Current	$V_{EN} = V_{IN} = H$		0.4	5	mA
VD_L	Diagnostic Output Low Voltage	$I_O = 2mA$ VS ≥ 4.5V			0.5	V
ID_{LE}	Diagnostic Output Leakage Current	VS = 0 or VS = Open; VD = 5.5V $T_j \leq 125°C$		0.1	10	µA
I_D	Diagnostic Output Current Capability	VD ≤ 20V DIAG = L		4		mA
t_{DOL}	Diagnostic Overload Delay Switch-off time	Fig. 1 $IO > IO_o$	50	100	200	µs
$S_{ON,OFF}$	Output (fall,rise) slew rate	Fig. 2 $R_L = 6Ω$	1000	1500	2000	V/ms
$t_{D\ ON}$		Fig.2			12.5	µs
$t_{D\ OFF}$	Output Delay Time	9V ≤ VS ≤ 16V	7.5		27.5	µs
$t_{D\ IOu}$	Open Load Diagnostic Delay Time	$R_L \leq 6Ω$			35	µs

DIAGNOSTIC TABLE

Operating Range: 6.5V < VS ≤ 32V (45V for t ≤ 500ms), – 40°C ≤ T_J ≤ 150°C

Conditions	EN	IN	Out	Diag
Normal Function	L H H	X L H	OFF OFF ON (*)	L L H
Over Load $I_O > 5A$	X	X	OFF	L
160°C < $T_j \leq$ 190°C Overtemperature	X X	L H	OFF OFF	H L
Open Load $V_O < 0.6V$ $I_O < 250mA$	X L H	L H H	OFF OFF ON (*)	H H L
Reset Over Load Latch	X		D.C.	D.C.

(*) For VS < 6 5V, Out = Undefined

Figure 1: Diagnostic Overload Delay Time

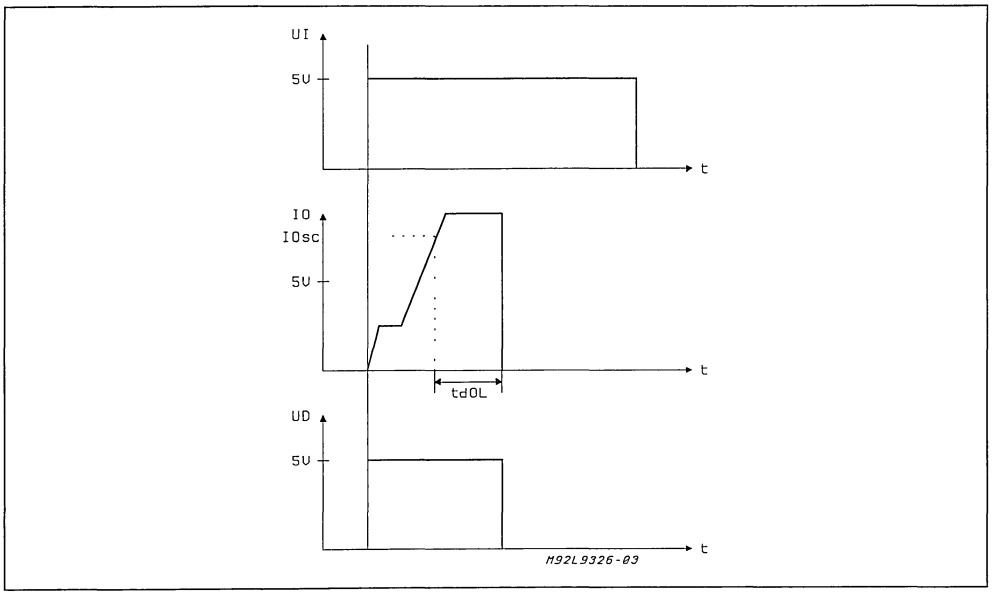


Figure 2: Output Slope

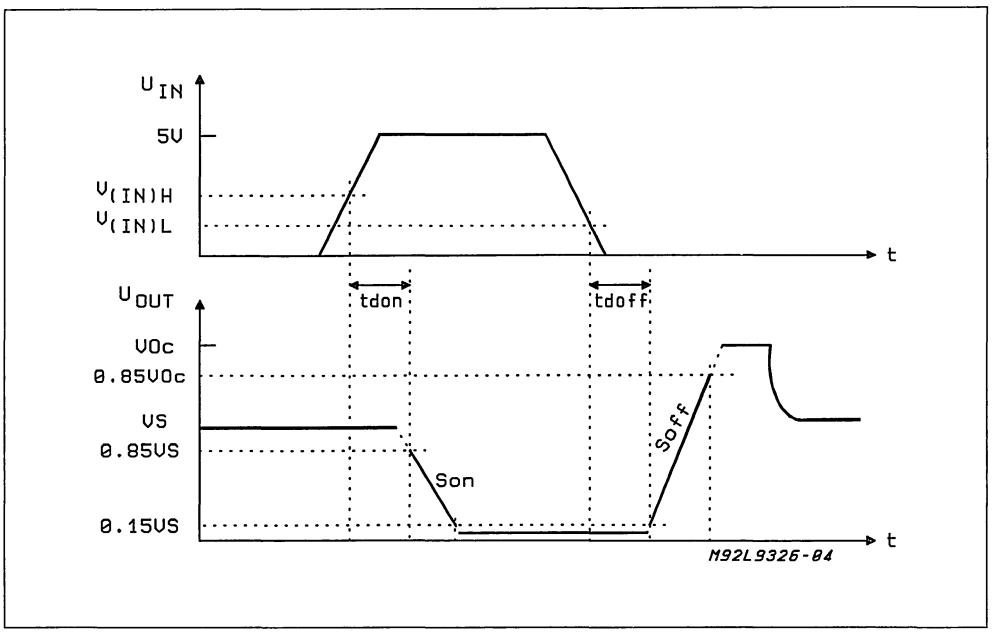
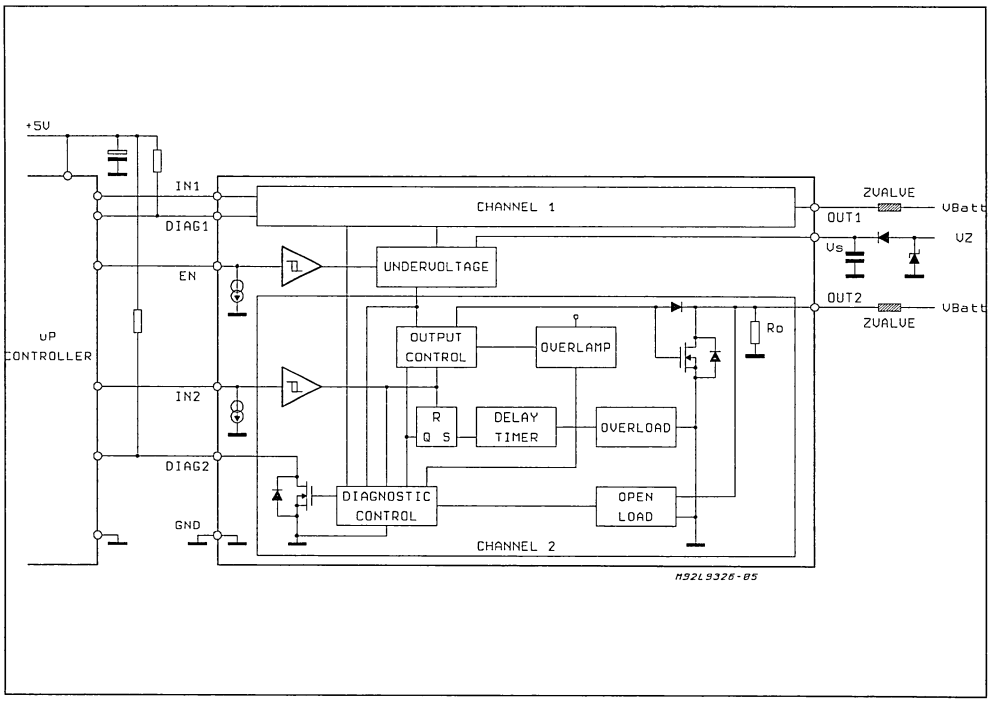


Figure 3: Application Circuit Diagram



CIRCUIT DESCRIPTION

The L9326 is a dual low side driver for inductive loads like valves in automotive enviroment. The device is enabled by a common CMOS compatible ENABLE high signal. The internal pull down resistances at the ENABLE and INPUT pins protect the device in open input conditions against malfunctions. An output slope limitation for du/dt is implemented to reduce the EMI. An integrated active flyback voltage limitation clamps the output voltage during the flyback phase to 50V.

Each driver is protected against short circuit condition [1] the output will be disabled after a short delay time tDOL to suppress spikes [2]. This disable is latched until a negative slope occure at the correspondent input pin. The Thermal disable of the output will be reseted if the junction temperature decreases below 160°C.

For the real time error diagnosis the voltage and the current of the output is compared with internal fixed values VO_U and IO_U to recognize open load ($R_L \geq 20\ K\Omega$) in ON anf OFF conditions.

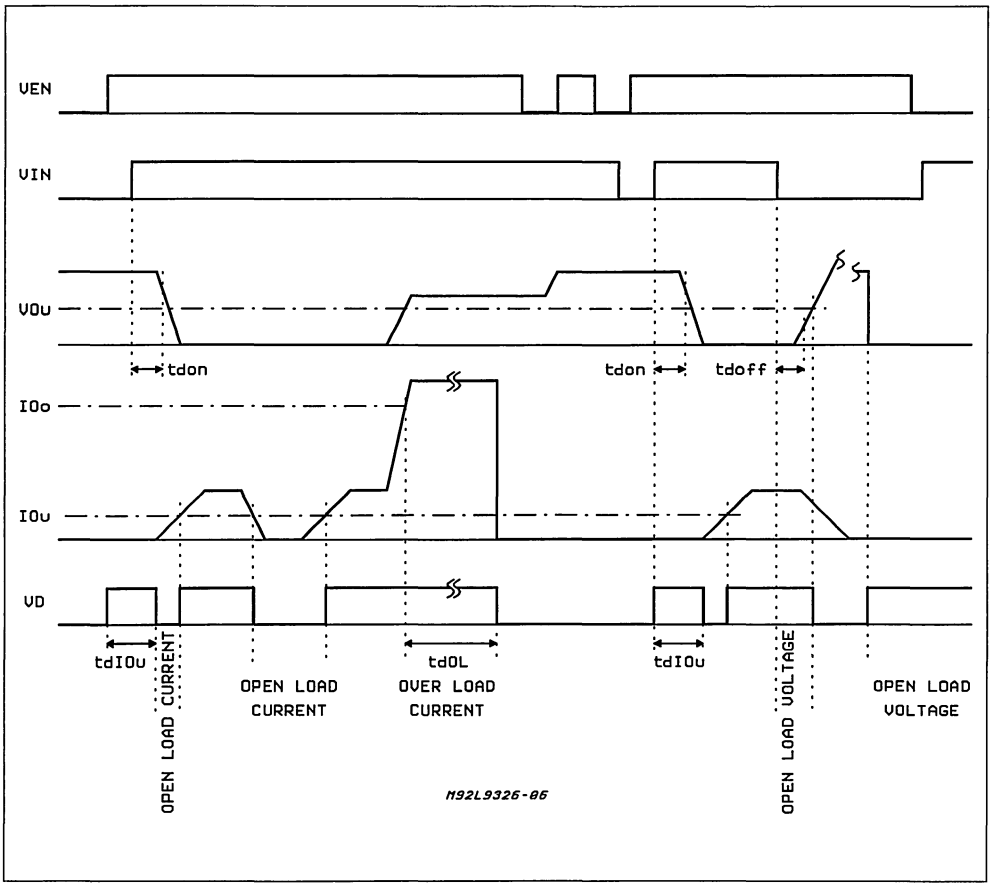
The diagnostic output level in connection with different ENABLE and INPUT conditions allows to recognize four different fail states, under voltage, over load, overtemp and open load.

The diagnostic output is also protected against short circuit up to UD_{max}.

1) overstepeing the over load current thereshold IO_o

2) During the diagnostic overload delay switch-off time t_{DOL} the output current will be limited only by the R_{DSON} of the output

Figure 4: Logic Diagram.



SGS-THOMSON MICROELECTRONICS

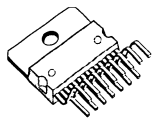
L9341

QUAD LOW SIDE DRIVER

PRODUCT PREVIEW

- DU/DT AND DI/DT CONTROL
- PWM CONTROLLED OUTPUT CURRENT
- SHORT CURRENT PROTECTION AND DIAGNOSTIC
- INTEGRATED FLYBACK DIODE
- UNDERVOLTAGE SHUTDOWN
- OVERVOLTAGE AND UNDERVOLTAGE DIAGNOSTIC
- OVERTEMPERATURE DIAGNOSTIC

MULTIPOWER BCD TECHNOLOGY



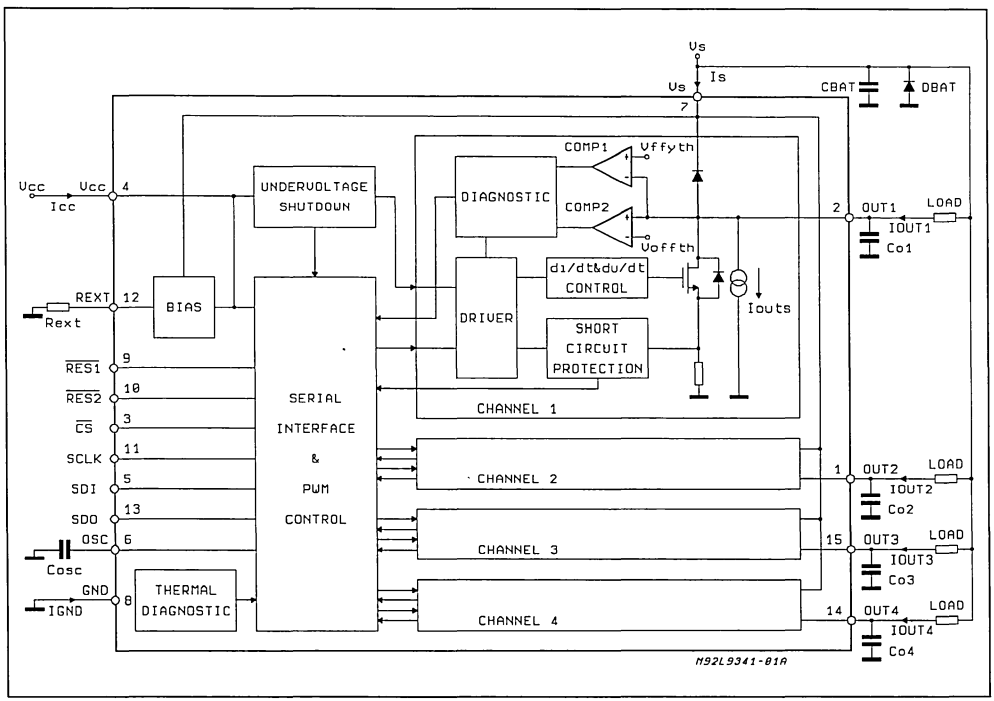
Multiwatt 15

ORDERING NUMBER: L9341

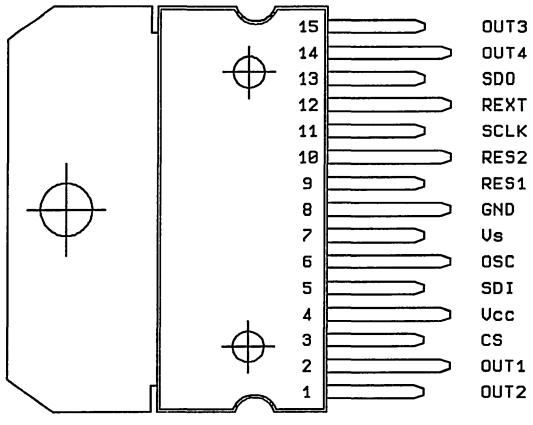
DESCRIPTION

The L9341 is a monolithic integrated circuit realized in Multipower BCD-II mixed technology. The driver is intended for inductive loads in synchronous PWM applications, especially for valve drivers. The output voltage and current rise and fall slopes du/dt and di/dt are controlled.

BLOCK APPLICATION DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} Voltage Range	-0.3 to 6	V
V_S	V_S Voltage Range	-0.3 to 24	V
V_{spmax}	VS Voltage Range for t ≤ 400ms	-2 to 40	V
V_{st}	Schaffner Transient Pulses on V_S	see note 1	V
V_{out}	Output Voltage Range for all Outputs: Negative Positive	 – 0.3 intern. clamped to V_S	 V V
I_{out}	Output Current for all Outputs: Negative Positive	 – 1 2.5	 A A
	Schaffner Transient Pulses on Output	see note 2	
V_{ESD}	ESD Voltage Capability (MIL 883 C)	2000	V

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction to Case	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient mounted on PC Board	35	°C/W
T_{sdh}	Thermal Hysteresis	20	°C
T_{sd}	Thermal Diagnostic	$T_j > 150$	°C

Notes:
1. Schaffner transient specification: DIN 40839 test waveforms of the following type: 1, 2, 3a, 3b, 5 and 6.
The pulses are applied to the application circuit according to fig. 3.

2. The maximum output current results from the Schaffner pulses specified in note 1.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified: 8V ≤ V_S ≤ 24V; 4.7V ≤ V_{CC} ≤ 5.3V; –40 °C ≤ Tj ≤ 150°C; I_O ≤ 1A (note 3); I_O ≤ 1.5A; V_{sp} = V_S for t ≤ 400ms; R_{ext} = 12.4KΩ ± 1%).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{ccq}	V_{cc} Quiescent Current	All Outputs Off			3	mA
I_{sq}	V_S Quiescent Current	All Outputs Off		17	25	mA
V_{ccu}	V_{cc} Undervoltage Threshold	See Note 4	3	4	4.7	V
V_{ccr}	V_{cc} Range for RES1 and RES2 Operation		3			V
R_{on}	On Resistance	I_o = 1A T_j = 125°C T_j = 25°C			750 450	mΩ mΩ
$I_{o\ off}$	Off State Output Current	Outputs Off 1.4V ≤ V_o ≤ V_S V_{outp} = V_{sp} = 40V	 2 2		 5 10	 mA mA
V_{outf}	Output Voltage During Flyback	I_o = 1A Output Off T_j = 25°C T_j = 125°C			 V_S +1.3 V_S +1.1	 V V
I_{gndf}	Current to GND during Flyback (see note 5)	I_o = 1A Output Off V_S = 24V V_{sp} = 40V			 44 52	 mA mA
I_{outr}	Reverse Leakage Current	V_{sp} - V_o = 40V			500	µA
V_{inH}	Low Input Level of SCLK, SDI, CS, RES1, RES2		0.7*V_{cc}		V_{cc}+0.3	V
V_{inH}	Low Input Level of SCLK, SDI, CS, RES1, RES2		– 0.3		0.3*Vcc	V
V_{REShys}	Hysteresis of Reset Inputs RES1, RES2		0.3		1	V
I_{inRESH}	Input Current on RES1,RES2	RES_i = H; 2V ≤ V_{sp} ≤ 8V RES_i = H; 8V ≤ V_{sp} ≤ 40V	– 10 5		10 10	µA µA
I_{in}	Input Current on SCLK,SDI,CS	– 2V ≤ Vsp ≤ 40V	– 10		10	µA
V_{SDOH}	High Level SDO Output Voltage	I_{SDO} = -1mA -2V ≤ V_{sp} ≤ 40V	0.9*V_{cc}		V_{cc}	V
V_{SDOL}	Low Level SDO Output Voltage	I_{SDO} = 1mA -2V ≤ V_{sp} ≤ 40V	0		0.4	V
I_{SDOZ}	SDO Tristate High-Z Leakage Current	0 ≤ V_{SDO} ≤ V_{cc} – 2V ≤ V_{sp} ≤ 40V	– 10		10	µA
PWM_{duty}	PWM Duty Cycle		1/16		15/16	
K_f	Frequency Accuracy Constant	See Note 6	0.93*K_{fn}	K_{fn}	1.07*K_{fn}	
V_{flyth}	Flyback Diagnostic Comparator Threshold	40 ≥ V_{sp} ≥ 8V V_S ≤ 8V	V_S – 1 1.5		V_S – 0.4	V V
V_{offth}	Off State Diagnostic Comparator Threshold		1.5		2	V
I_{outl}	Output Current Limitation Threshold	see Note 7	1.5		2.5	A
t_{dpo}	Delay Time PWM Signal to Out.		5		15	µs
S_{ov}	Output Voltage Rise and Fall Slope | du/dt |	(from 10 to 90% of V_o) Fig. 2	1.5		5	V/µs
S_{oc}	Output Current Rise and Fall Slope |di/dt|	0.5 ≤ Io ≤ 1.5A 0.1 ≤ Io ≤ 0.5A (from 10 to 90% of I_o)	50 25		100 100	mA/µs mA/µs

Notes:

3. The mean value is $I_o = \frac{1}{T}\int_0^T I_o(t)\,dt$;

4. The outputs are switced off for Vcc ≤ Vccu. The logic is not reseted For a reset, RES1 or RES2 must be used.

5. This current is measured in the GND - terminal when one single output is in flyback and consists of the supply current added to the value of the output current source and the leakage current of the flyback diode. This leakage current is less than 1% of the nominal flyback current.

6. The PWM frequency is defined by an external capacitor. The PWM oscillator frequency is: $f_{pwm} = \frac{f_{osc}}{32}$. with $f_{osc} = \frac{K_f}{C_{osc}} \cdot 1A/V$ and $k_{in} = 15 \cdot 10^{-6}$; the range is: 300Hz ≤ f_{pwm} ≤ 3000Hz. The OSC Pin can be alternatively driven by an external TTL / CMOS signal.

7. For $I_{out} \geq I_{outl}$ an internal comparator switches the corresponding output off for the current PWM cycle.

Figure 1: Logic Diagram of PWM Generation.

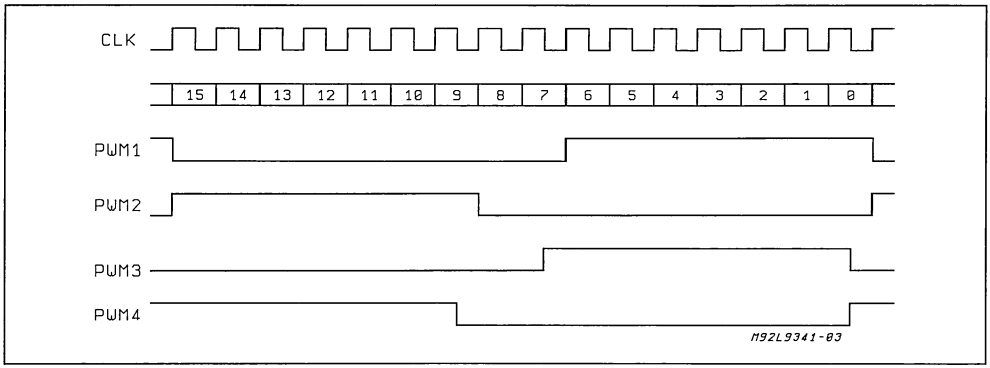


Figure 2: Output Switching Diagram.

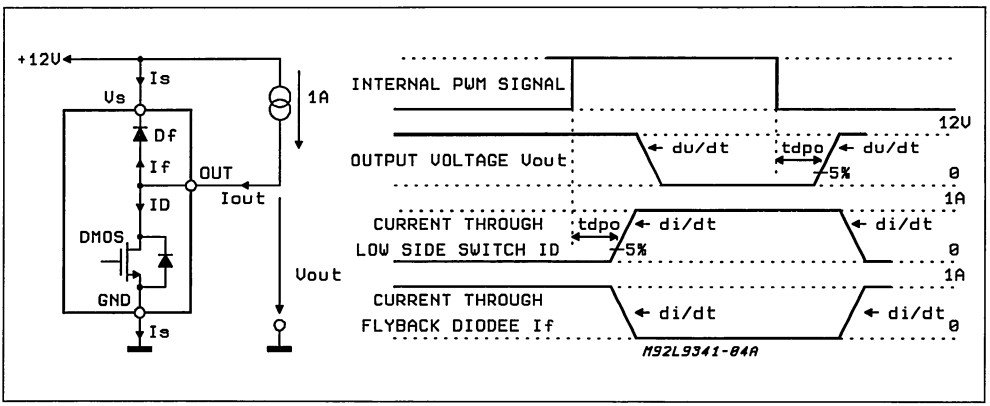


Figure 3: Test Circuit for Schaffner Pulses.

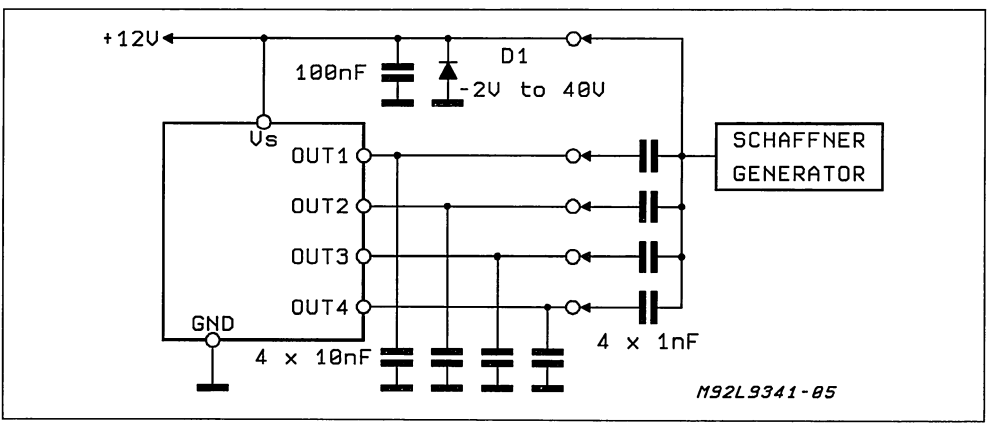
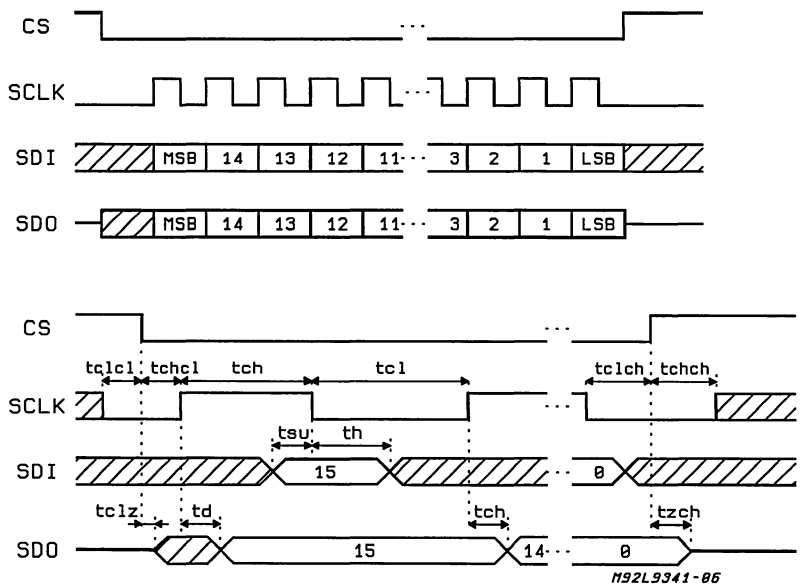


Figure 4: Synchronous Serial Interface Protocol.



f_{clock}	Clock Frequency	min. DC	max. 2MHz
t_{ch}	Width of Clock Input High Puls	min. 200ns	
t_{cl}	Widh of Clock Input Low Puls	min. 200ns	
t_{clcl}	Clock Low Before CS Low	min. 200ns	
t_{chcl}	Clock High After CS Low	min. 200ns	
t_{clch}	Clock Low Before CS High	min. 200ns	
t_{chch}	Clock High After CS High	min. 200ns	
t_{clz}	SDO Low-Z CS Low	min. 0ns	max. 280ns
t_{zch}	SDO High-Z CS High		max. 200ns
t_{su}	SDI Input Setup Time	min. 80ns	
t_h	SDI Input Hold Time	min. 80ns	
t_d	SDO Output Delay Time (C_L = 50pF)		max. 100ns
t_{oh}	SDO Output Hold Time	min. 0ns	

Figure 5: PWM Generation Function Table.

Bit 3 - 0	PWM1	PWM2	PWM3	PWM4	OUTPUT
0000	15/16	15/16	15/16	15/16	OFF
0001	1/16	15/16	1/16	15/16	ON
0010	2/16	14/16	2/16	14/16	ON
0011	3/16	13/16	3/16	13/16	ON
0100	4/16	12/16	4/16	12/16	ON
0101	5/16	11/16	5/16	11/16	ON
0110	6/16	10/16	6/16	10/16	ON
0111	7/16	9/16	7/16	9/16	ON
1000	8/16	8/16	8/16	8/16	ON
1001	9/16	7/16	9/16	7/16	ON
1010	10/16	6/16	10/16	6/16	ON
1011	11/16	5/16	11/16	5/16	ON
1100	12/16	4/16	12/16	4/16	ON
1101	13/16	3/16	13/16	3/16	ON
1110	14/16	2/16	14/16	2/16	ON
1111	15/16	1/16	15/16	1/16	ON

Figure 6: PWM Information From Microcontroller to QLSD.

Bit. Nr.	Name	Contents
0	P10	PWM Duty Cycle for Channel 1 / Bit 0: LSB
1	P11	PWM Duty Cycle for Channel 1 / Bit 1
2	P12	PWM Duty Cycle for Channel 1 / Bit 2
3	P13	PWM Duty Cycle for Channel 1 / Bit 3 : MSB
4	P20	PWM Duty Cycle for Channel 2 / Bit 0 : LSB
5	P21	PWM Duty Cycle for Channel 2 / Bit 1 :
6	P22	PWM Duty Cycle for Channel 2 / Bit 2 :
7	P23	PWM Duty Cycle for Channel 2 / Bit 3 : MSB
8	P30	PWM Duty Cycle for Channel 3 / Bit 0 : LSB
9	P31	PWM Duty Cycle for Channel 3 / Bit 1 :
10	P32	PWM Duty Cycle for Channel 3 / Bit 2 :
11	P33	PWM Duty Cycle for Channel 3 / Bit 3 : MSB
12	P40	PWM Duty Cycle for Channel 4 / Bit 0 : LSB
13	P41	PWM Duty Cycle for Channel 4 / Bit 1:
14	P42	PWM Duty Cycle for Channel 4 / Bit 2 :
15	P43	PWM Duty Cycle for Channel 4 / Bit 3 : MSB

Figure 7: PWM Information from QLSD to Microcontroller.

Bit Nr.	Name	Contents
0	F11	COMP1 State at Positive Edge of PWM1 (0: $V_{out1} > V_{flyth}$; 1: $V_{out1} < V_{flyth}$)
1	F12	COMP2 State at Negative Edge of PWM1 (1: $V_{out1} > V_{offth}$; 0 : $V_{out1} < V_{ofth}$)
2	F21	COMP1 State at Positive Edge of PWM2 (0: $V_{out2} > V_{flyth}$; 1: $V_{out2} < V_{flyth}$)
3	F22	COMP2 State at Negative Edge of PWM2 (1: $V_{out2} > V_{ofth}$; 0 : $V_{out2} < V_{ofth}$)
4	F31	COMP1 State at Positive Edge of PWM3 (0: $V_{out3} > V_{flyth}$; 1: $V_{out3} < V_{flyth}$)
5	F32	COMP2 State at Negative Edge of PWM3 (1: $V_{out3} > V_{offth}$; 0 : $V_{out3} < V_{ofth}$)
6	F41	COMP1 State at Positive Edge of PWM4 (0: $V_{out4} > V_{flyth}$; 1: $V_{out4} < V_{flyth}$)0
7	F42	COMP2 State at Negative Edge of PWM4 (1: $V_{out4} > V_{offth}$; 0 : $V_{out4} < V_{ofth}$)
8	RES1	Logic State of RES1 Input (0: RES1 = L ; 1: RES1 = H)
9	RES2	Logic State of RES2 Input (0: RES2 = L ; 1: RES2 = H)
10	TSDF	Thermal Flag (0: Overtemperature ; 1:Normal)
11	C1	Current at Negative Edge of PWM1 (0: $I_{out} > I_{outl}$; $I_{out} < I_{outl}$)
12	C2	Current at Negative Edge of PWM2 (0: $I_{out} > I_{outl}$; $I_{out} < I_{outl}$)
13	C3	Current at Negative Edge of PWM3 (0: $I_{out} > I_{outl}$; $I_{out} < I_{outl}$)
14	C4	Current at Negative Edge of PWM4 (0: $I_{out} > I_{outl}$; $I_{out} < I_{outl}$)
15	1	Framing Information (always 1)

FUNCTIONAL DESCRIPTION

The U511 is a PWM quad low side driver for inductive loads. The duty cycle of the internal generated PWM signal is set by a microcontroller via a serial interface for each output. An output slope limitation for both dv/dt and di /dt is implemented to reduce RFI. The PWM generation is realized avoiding a simultaneous output switching. As a result, di/dt becomes smaller. Integrated flyback diodes clamp the output voltage during the flyback phase of the low side switches.

The driver is protected against short circuit and thermal overload. An undervoltage shutdown circuit switches off all outputs if V_{cc} is less then V_{ccu}. Below the shutdown voltage all outputs remain in off state regardless of the input state. After each malfunction which resets the driver, only the serial link interface can reactivate the normal function. In case of overcurrent ($I_{out} = I_{out1}$), an internal comparator switches the output off. The overcurrent information can be read via the serial link for each driver separately at the negative edge of the corresponding PWM signal.

The interface to the microcontroller is realized with a 16 bit synchronous serial peripheral interface (SPI). If CS is switched low, the serial link becomes active and SDO goes to low impedance. At the rising edge of the SCLK signal, one of the 16 bit of data stored in a shift register appear sequencely at SDO. These data contain the 8 error flags, the status of thermal shutdown and the external reset sources RES1, RES2. The last bit is framing information (see fig. 7). At each falling edge of SCLK, one of the 16 bits of data sent by the microcontroller is transferred via the SDI input to the driver. These data contain the duty-cycle information for the internal PWM generation (4 times 4 bit).

On the rising edge of CS the previously stored information is transferred to the circuits. SDO become now high impedance and SDI is inactive. The serial interface of the QLSD is cascadable with the serial link interface of another QLSD, thus obtaining a 32 bit serial link information wich can control eight inductive loads. For a safety data transfer the takeover of data bits is only realized when the number of SCLK - clocks is n x 16 ($n \geq 1$).

The PWM duty cycle is set by 4 bit for each output independently via the serial link. If all four bits for an output are zero, the output is turned off, but the error diagnosis will work correctly (see fig. 6 and 7). The PWM frequency is defined by an external capacitor on the OSC pin. Rext defines through the reference current the output current slope, the diagnostic current sink and the internal oscillator frequency (together with C_{osc}).

For error diagnosis the voltage on the output is measured during the on and off state of the particular output driver. Upon the rising edge of the PWM signal (at this moment the power output is off and will be switched on) the status of COMP1 is stored into an internal latch. On the falling edge of the PWM signal (the power output is on and will be switched off) the status of COMP2 is stored into another internal latch. This information can be read via the serial link for each output driver separately (see fig. 7).

Overtemperature is diagnosed by a flag which goes to a low logic level if the junction temperature rises above 150°C. This flag can be read on the serial output.

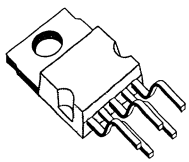
SGS-THOMSON MICROELECTRONICS

L9351

HIGH SIDE DRIVER

ADVANCE DATA

- LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUT
- WIDE SUPPLY VOLTAGE
- VERY LOW QUIESCENT CURRENT (30mA max)
- NO EXTERNAL COMPONENTS
- INTERNAL RECIRCULATION PATH FOR FAST DECAY OF INDUCTIVE LOAD CURRENT
- SHORT CIRCUIT PROTECTION
- FAILSAFE OPERATION : OUTPUT IS OFF IF THE LOGIC INPUT IS LEFT OPEN



Pentawatt

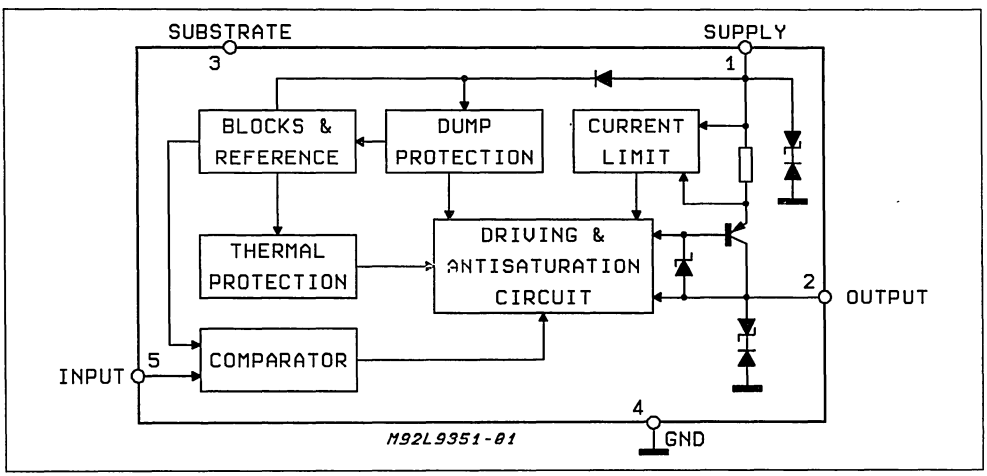
ORDERING NUMBER : L9351

DESCRIPTION

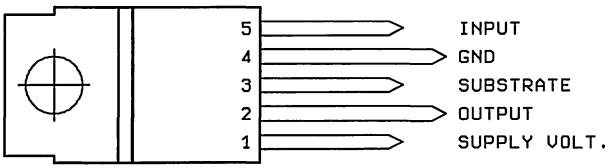
The L9351 is a monolithic integrated circuit designed to drive grounded resistive, inductive or mixed loads from the power supply positive side. Very low standby current (30mA max.) and internally implemented protections against load dump and reverse voltages make the device very useful in automotive applications. No external components are required because the output recirculation clamping zener is included in the chip. This zener can withstand a recirculation peak current of 550mA on a 80mH/25Ω load.

The device is self-protected against overtemperature, overvoltage and overcurrent conditions. The L9351 operates over the full battery voltage range, from 4.5V (cold cranking) up to 24V (jump starting). The L9351 withstands revers battery conditions (-13V) and supply voltage transients up to 80V limiting the maximum output transistor V_{EC} to 70V by an internal zener. ON and OFF delay times of 25µs max in any output status, including recirculating situation, allow PWM use of L9351.

BLOCK DIAGRAM



PIN CONNECTION (top view)



Note : Pin 3 must be left open or connected to ground.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	D.C. Supply Voltage D.C. Reverse Supply Voltage Load Dump : 5ms ≤ t_{rise} ≤ 10ms τ_f Fall Time Constant = 100ms, R_{source} ≥ 0.5Ω Low Energy Spikes : R_{source} ≥ 10Ω, t_{rise} = 1µs, tf = 2ms, fr Repetition Frequency = 0.2Hz	24 – 13 60 ± 85	V V V V
V_I	Input Voltage	– 0.3 to 7	V
I_O	Output Current	Internally Limited	
P_{tot}	Total Power Dissipation at T_{case} = 90°C	17.1	W
T_{JI} T_{stg}	Junction and Storage Temperature	– 55 to 150	°C

THERMAL DATA

R_{th}j-amb	Thermal Resistance Junction-ambient	Max	80	°C/W
R_{th}j-case	Thermal Resistance Junction-case	Max	3.5	°C/W

ELECTRICAL CHARACTERISTICS

(V_S = 14.4V, $-40°C \leq Tj \leq +125°C$ unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage		4.5		24	V
V_{IH}	Input Voltage High	4 5 < V_S < 24	2.0			V
V_{IL}	Input Voltage Low			1	0.8	V
I_I	Input Current	0 8 < V_I < 5.5V			40	µA
I_{PL}	Output Leakage Current	V_O = 0V V_S = 24V V_I < 0 8V			140	µA
V_{sat}	Output Saturation Voltage	I_O = 125mA V_S = 4.5V			0.5	V
		I_O = 225mA V_S = 14.4V			0.5	V
		I_O = 550mA V_S = 14.4V			0.7	V
I_{SC}	Output Short Circuit Current		0.6	1.5		A
I_Q	Quiescent Current	V_I > 2V			30	mA
		V_I < 0.8V Stand-by Condition		100	150	µA
V_{ZO}	Negative Output Zener Voltage	R_L = 25Ω L = 80mH on V_I Transition from "1" to "0"	− 36	− 30	− 24	V
T_{on}	Turn ON Delay	Resistive Load R_L = 25Ω, T_j = 25°C (fig.2)			20	µs
T_{off}	Turn OFF Delay				25	µs

Figure 1 : Typical Automotive Application Circuit.

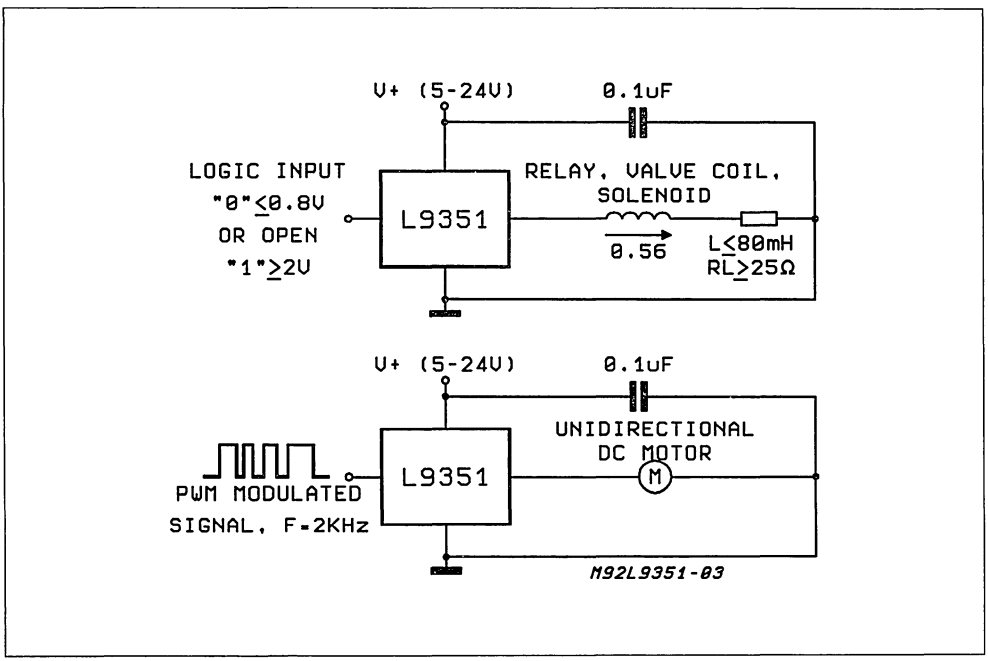


Figure 2 : Resistive Load.

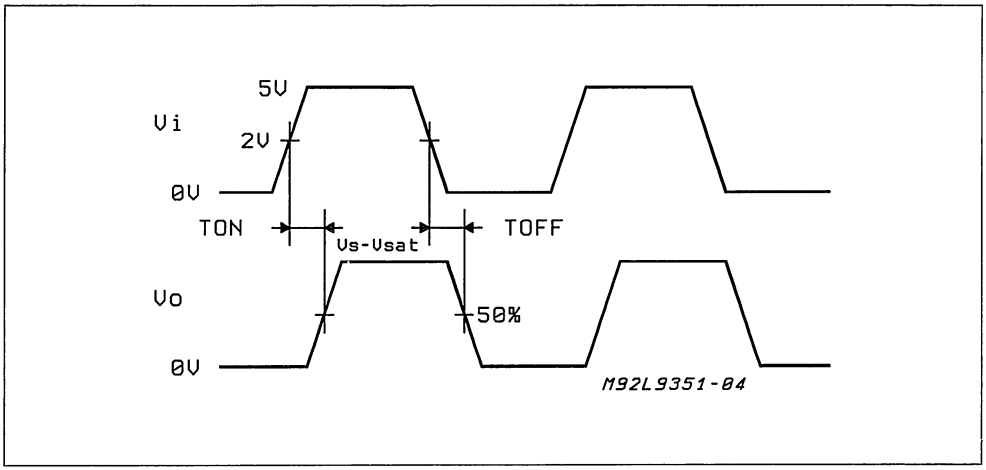
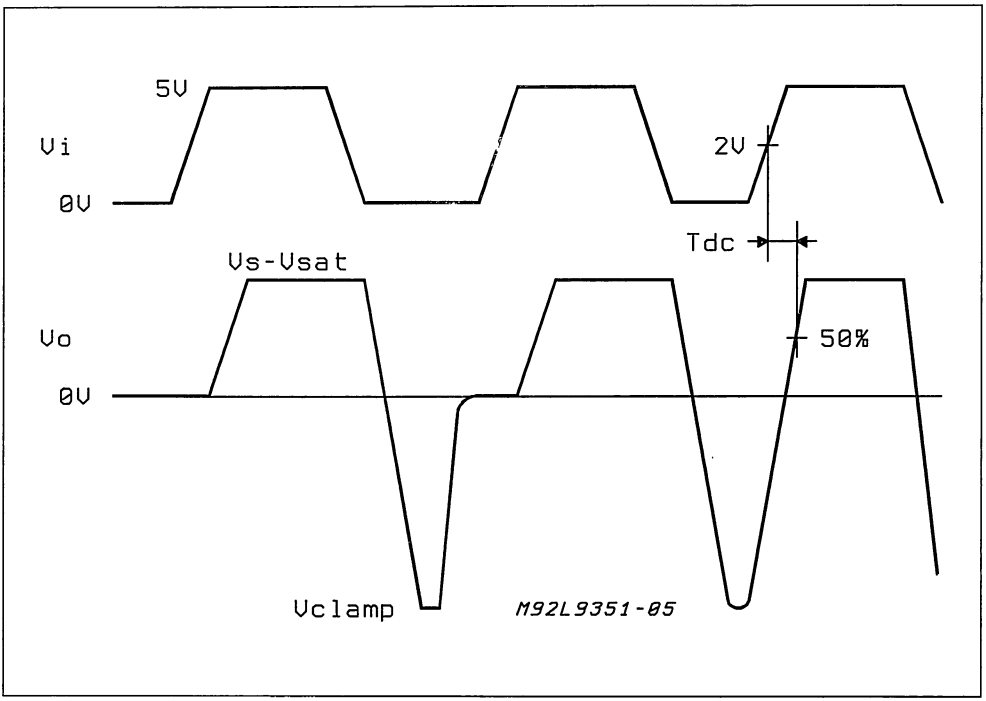


Figure 3 : Inductive Load.



SGS-THOMSON MICROELECTRONICS

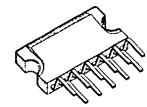
L9360

DUAL INJECTION DRIVER

ADVANCE DATA

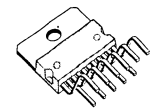
- WIDE SUPPLY RANGE (5.5 - 40V)
- VERY LOW ON RESISTANCE (TYP. 300mΩ)
- OUTPUT CURRENT UP TO 2A
- HIGH PERFORMANCE DIAGNOSTIC
- UNDERVOLTAGE DISABLE
- OVERVOLTAGE AND SHORT CIRCUIT PROTECTION
- CMOS COMPATIBLE CONTROL INPUTS

MULTIPOWER BCD TECHNOLOGY



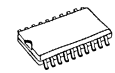
Clipwatt 11

ORDERING NUMBER: L9360



Multiwatt 11

ORDERING NUMBER: L9360M



SO20L (12+4+4)

ORDERING NUMBER: L9360D

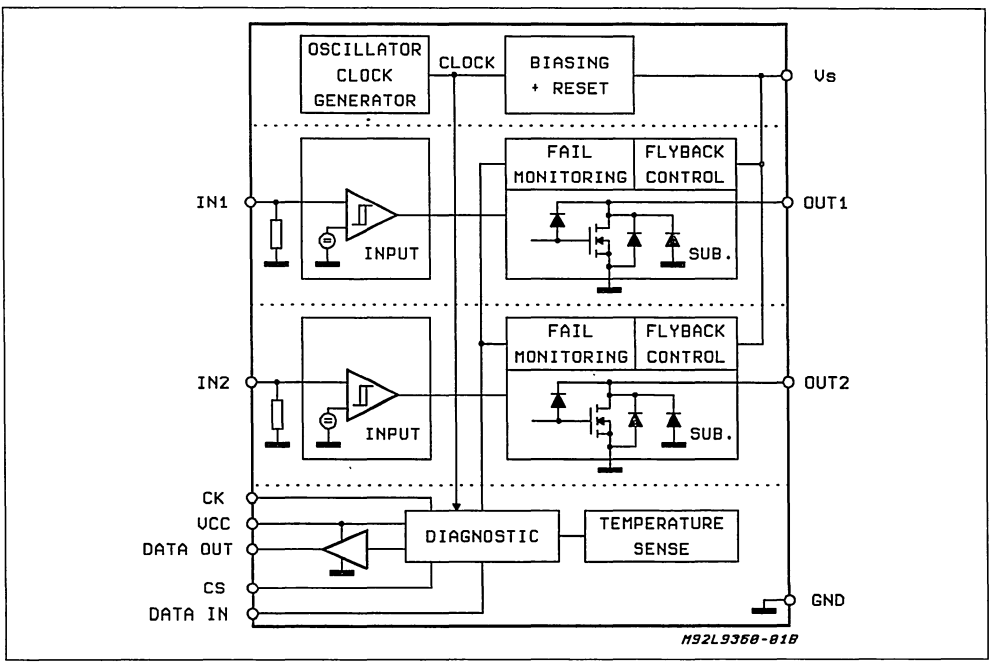
DESCRIPTION

The L9360 is a monolithic dual low side smart Power switch with DMOS power outputs, rated for operation in automotive environment.

It is intended to drive injectors connected to the positive battery voltage.

Thanks to its CMOS compatibility and its high performance diagnostic it is very well suited for handshake data with a microcontroller.

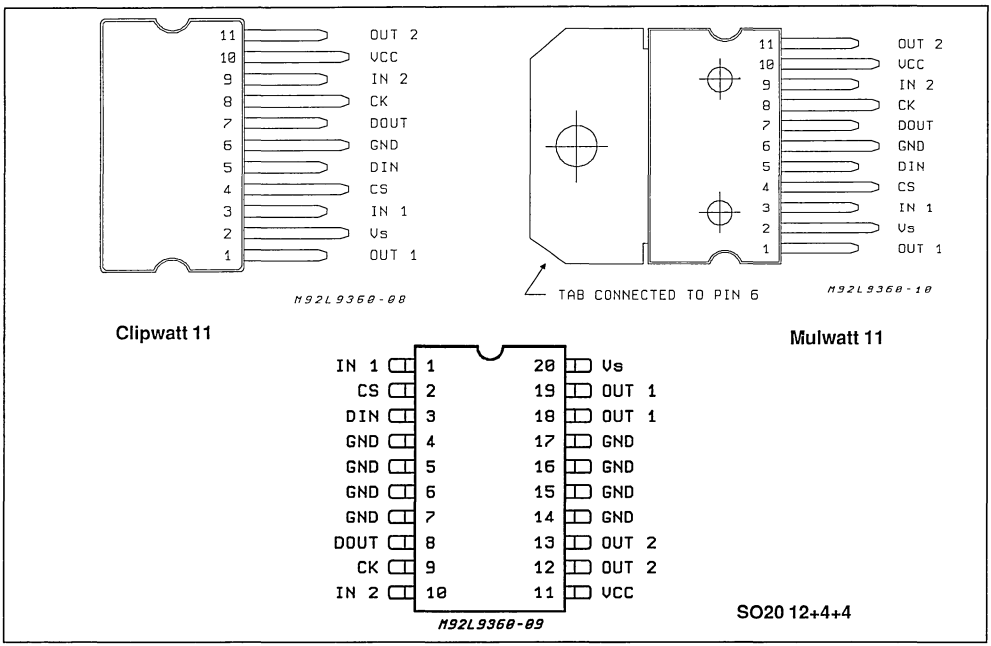
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	40	V
I_{OCL}	Output Clamping Current	2	A
E_{OCL}	Output Dissipated Energy	TBD	J
I_{or}	Reverse Output Current (Pd ≤ 1W)	-2	A
V_{CC}	Stabilized Logic Supply Voltage	7	V
V_{CCrev}	Reverse Stabilized Logic Supply Voltage	-0,3	V
V_I	Input Voltage	7	V
V_{Irev}	Reverse Input Voltage	-0.3	V
V_{Id}	Data Pin Voltage	7	V
V_{Idrev}	Reverse Data Pin Voltage	-0.3	V
T_{stg}	Storage Temperature	-55 to 150	°C
$T_{j\text{-case}}$	Operating Junction Temperature	-40 to 150	°C
$T_{j\text{-SD}}$	Thermal Overload Detection Temperature	150 to 165	°C
$T_{j\text{-SDH}}$	Thermal Threshold Hysteresis	Typ. 20	°C
V_{ESD}	Protected According to MIL883C		

PIN CONNECTIONS (top view)



Clipwatt 11

Mulwatt 11

SO20 12+4+4

THERMAL DATA

Symbol	Parameter		Max. Value	Unit
$R_{th\ j\text{-amb}}$	Thermal resistance junction to ambient	Clipwatt 11	70	°C/W
		Multiwatt 11	60	°C/W
$R_{th\ j\text{-pins}}$	Thermal resistance junction to pins	SO20L	20	°C/W
$R_{th\ j\text{-case}}$	Thermal Resistance junction-case	Multiwatt 11	3	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 5.5 to 25V, V_{CC} = 4.5 to 5.5V, T_j =–40 to 150°C unless otherwise specified; the voltage and currents are assumed positive, when oriented in the arrows direction shown in the application circuit diagram)

OUTPUT STAGE (EACH CHANNEL)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{DSON}	On Resistance	VI = HIGH, V_S >7V V_I = HIGH, V_S <7V		300 400	600 1000	mΩ mΩ
I_{OSC}	Out Short Circuit Current		2	3	4	A
V_{OCL}	Output Clamping Voltage	I_O = 0.2mA	70	80	100	V
V_{ODG}	Output Internal Voltage	V_I = LOW, see Fig. 5	0.45Vs	0.5V_S	0.55VS	V
$R1_{ODG}$	Internal Output Resistance	V_I = LOW, see Fig. 5		20		KΩ

SUPPLY VOLTAGE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CCDC}	DC Supply Current (VCC)			1	2	mA
I_S	Supply Current (V_S)	V_{I1} = V_{I2} = LOW		4	7	mA
		V_{I1} = V_{I2} = HIGH		16	25	mA
		V_{I1} = V_{I2} = HIGH; V_S= 14V		10		mA

CONTROL INPUTS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input LOW Level	VCC = 5V		2	1.5	V
V_{IH}	Input HIGH Level	V_{CC} = 5V	3.5	3.2		V
V_{ITH}	Input Threshold Hysteresis		1	1.2	1.6	V
td_{ON}	Input to Out Delay Time	R_L = 14Ω; V_S= 14V		1.5	10	µs
t_{OR}	Output Rise Time	R_L = 14Ω; V_S= 14V		3.5	10	µs
t_{dOFF}	Input to Out Delay Time	R_L = 14Ω; V_S= 14V		2	10	µs
t_{OF}	Output Fall Time	R_L = 14Ω; V_S= 14V		1.2	10	µs
R_{IN}	Input Resistance		100	200	300	KΩ

DIAGNOSTIC & PROTECTIONS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CSL}	CS Input LOW Level	V_{CC} = 5V		2	1.5	V
V_{OIL}	Data Input LOW Level	V_{CC} = 5V		2	1.5	V
V_{CKL}	CK Input LOW Level	V_{CC} = 5V		2	1.5	V
V_{CSH}	CS Input HIGH Level	V_{CC} = 5V	3.5	3.2		V
V_{DIH}	Data Input HIGH Level	V_{CC} = 5V	3.5	3.2		V
V_{CKH}	CK Input HIGH Level	V_{CC} = 5V	3.5	3.2		V
V_{DOL}	Data Output LOW	I_{DO} = 1mA		0.2	0.5	V
V_{DOH}	Data Output HIGH	I_{DO} = -200µA; V_{CC} = 5V	4			V
I_{DOL}	Data Output Leakage Current	V_{DO} = V_{CC}		1	10	µA
R_{LOL}	External Recognized Resistance for Open Load Detection	See fig. 5		10		KΩ
V_{OED}	Output Excessive Drop Thresh	See fig. 5	2	2.5		V
R_{OSG}	Output Resistance to GND for Short to GND Detection	See fig. 5		5		KΩ
t_{DOSG}	Output Short to GND Switch OFF			50	150	µs
t_{ES}	Error Recognition Time for the Stochastic Error	See fig. 4		5		µs
t_S	Time for Error Recognized	See fig. 4		50	150	µs
f_{OSG}	Internal Oscillator Frequency			500		KHz
f_{CLK}	External Clock Frequency				1	MHz

CIRCUIT DESCRIPTION

The device is realized in the BCD100 technology which combines CMOS logic, bipolar components and as output stages DMOS transistors which can withstands 100V drain-source voltage.

Via the CMOS compatible inputs (IN1, IN2) the power DMOS can be switched ON and OFF independently from each other. All functions of the device are guaranteed between 5.5V and 40V supply voltage. Between 5.5 to to 7V supply voltage the typical drain-source resistance increases from 250mΩ to 500mΩ typ. With this limitation a charge pump could be avoided.

For V_S below 5.5V the device can be disabled. Both outputs are switched OFF independently from the input status. The data output is switched to tristate. In the undervoltage mode (V_S < 5.5V) a possible failure status was reset. Below 3V the chip functions are not defined. The device is protected against short circuit to supply but not protected against thermal overload due to security reason. Only via the diagnostic the system is informed about a thermal overload and the other possible failure modes which are described separately. A quasi digital filter avoids that short time stochastic failures are stored in the diagnostic register.

When a short circuit to the supply is recognized and stored in the diagnostic register the output transistor is switched OFF. The output can be switched ON again only via a new input pulse.

The device needs a second supply voltage (V_{CC}) which comes normally from the same supply as for the µC.

This voltage supplies the logic and avoides problems whith logic level disturbances.

Figure 1: Two Chip Solution To Drive Four Valves: Parallel Data Out

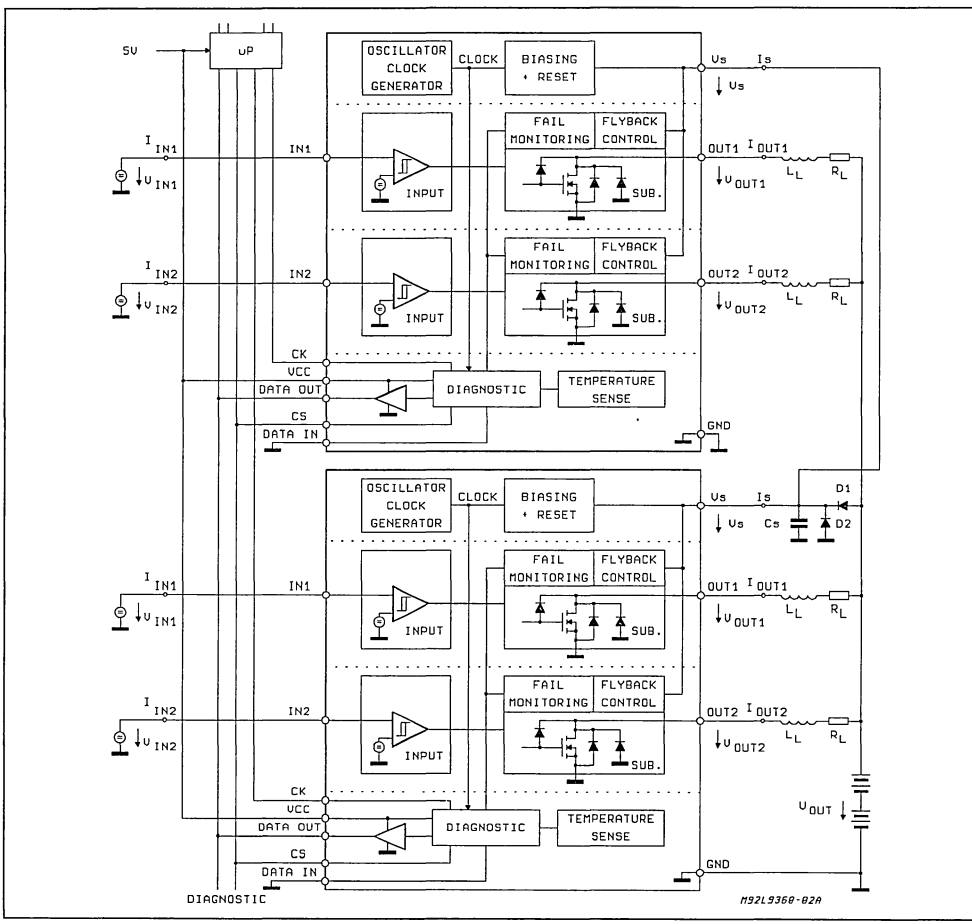
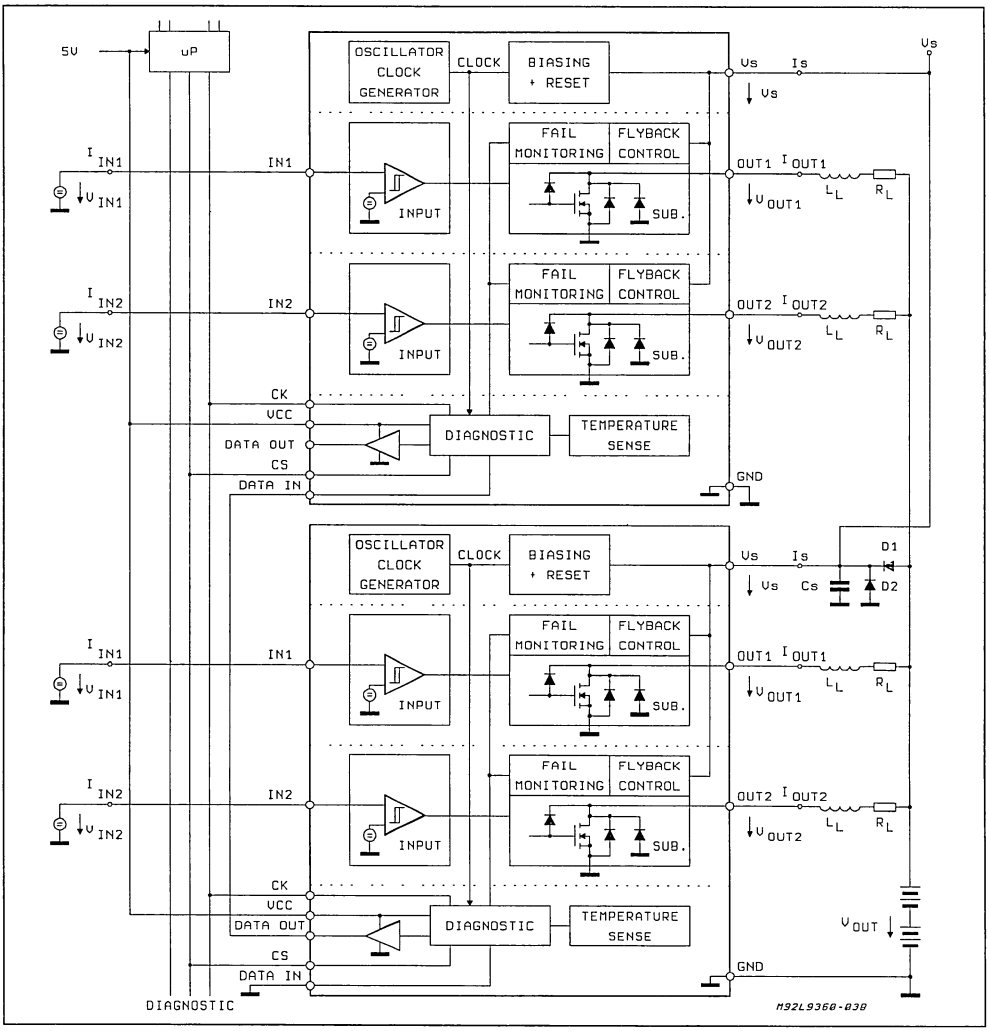


Figure 2; Two Chip Solution To Drive Four Valves: Serial Data Out



DIAGNOSIS

The diagnosis is able to detect the following states:

- OUTPUT SHORT-CIRCUIT TO BATTERY (SUPPLY VOLTAGE)
- OUTPUT SHORT-CIRCUIT TO GROUND
- OPEN LOAD
- THERMAL OVERLOAD

READING OF THE DIAGNOSIS REGISTER

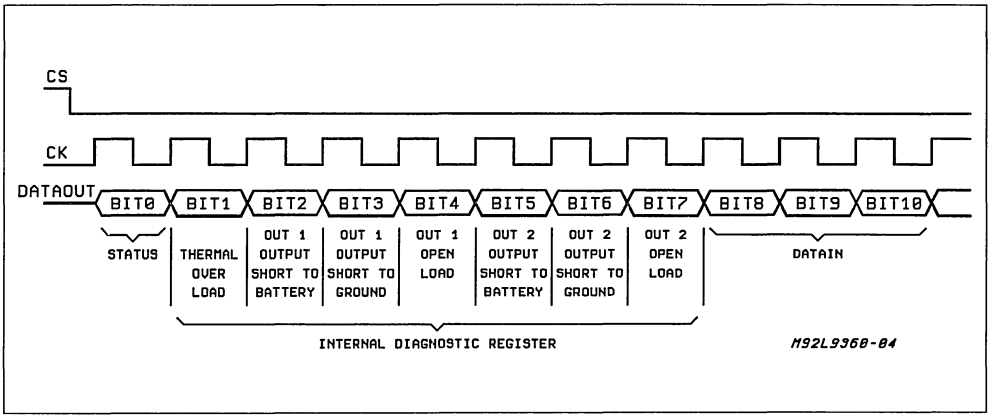
A low signal at the chip select CS-input and a positive edge of the clock signal at CK-input starts the reading of the diagnosis register.

The serial diagnosis register (Ref. to figure 3) is loaded synchronously with CK-signal at DATAOUT and new data fed through DATAIN as long as CS is "LOW".

After the nineth clock cycle the first DATAIN information is present at DATAOUT. The STATUS BIT 0 is "HIGH if one diagnosis register is set or the DATAIN-input is "HIGH", hence the presence of a failure can be detected by BIT 0.

The positive edge at CS clears the diagnosis register. During reading the diagnosis register (CS = "LOW") the single bits cannot be changed.

Figure 3: Serial Diagnostic



CASCADING OF SEVERAL INJECTOR DRIVERS

The possibility is given to read the diagnosis registers of several injector drivers via one diagnosis bus. Additionally the user can choose between two versions.

1. (figure 1):

The CK and DATAOUT terminals of the injector drivers are connected in parallel to the diagnosis bus. Each IC is provided with a separate CS-wire. The DATAIN-input is connected to GND.

2. (figure 2)

The CK and CS terminals are connected to the parallel diagnosis bus. The data line is connected in series through the terminals DATAIN and DATAOUT or each single IC. The DATAIN input of the first IC must be connected to GND.

The first version allow to read the desired diagnosis register immediately after the CS-signal is applied. in the other version all diagnosis registers have to be read one after the other whereby only a 3-wire bus is sufficient. In the other case each IC needs a separate CS-lead to the processor.

FAILURE DETECTION

Except the overtemperature signal all failure signals are filtered before setting the corresponding BIT in the diagnosis register.

The filter checks whether the failure signal is present during three times running the measure cycle within Ts. Spikes shorter than t_{ES} are ignored.

THERMAL OVERLOAD

If the chip exceeds T_{JSB} the "thermal overload"-BIT is set. Because the transistors are not switched off the element can be thermally destroyed if the control does not set the IN1 and IN2 inputs to "LOW".

OUTPUT SHOTR-CIRCUIT TO BATTERY (BIT2/5)

The output currents $I_{O1/2}$ are internally limited to 3A (typ).If the output current reaches the current limit the power DMOS leaves the resistive region and changes to the saturation region.

Consequently the drain source voltage increases and after reaching of typ. 2V the "output-short-circuit to battery" BIT is set and the power DMOS are switched off.

Repetitive control of IN_1 and IN_2 inputs (low-high sequence) switches on the DMOS again. But the bit in the diagnosis register is not resetted.

Figure 4

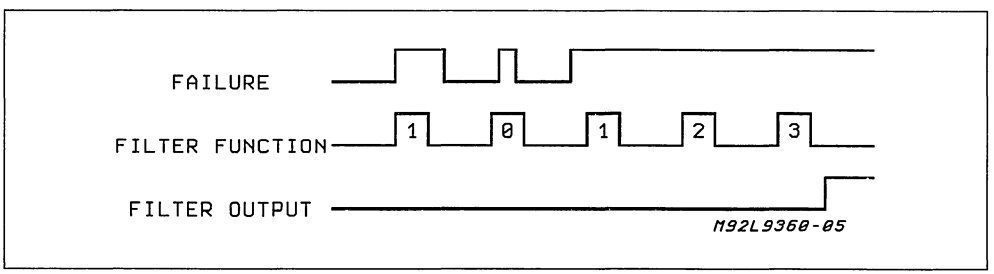
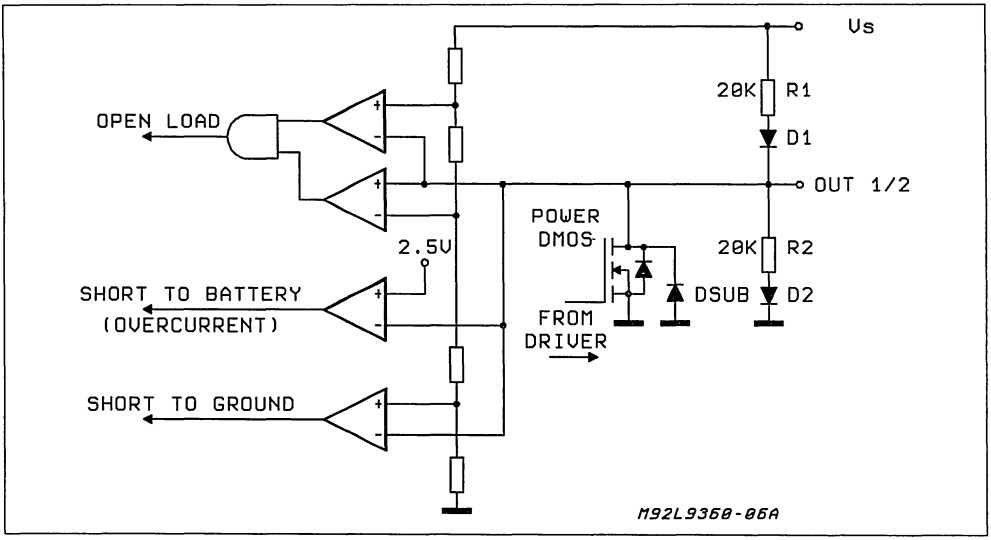


Figure 5: Principle Of Internal Diagnostic Detection

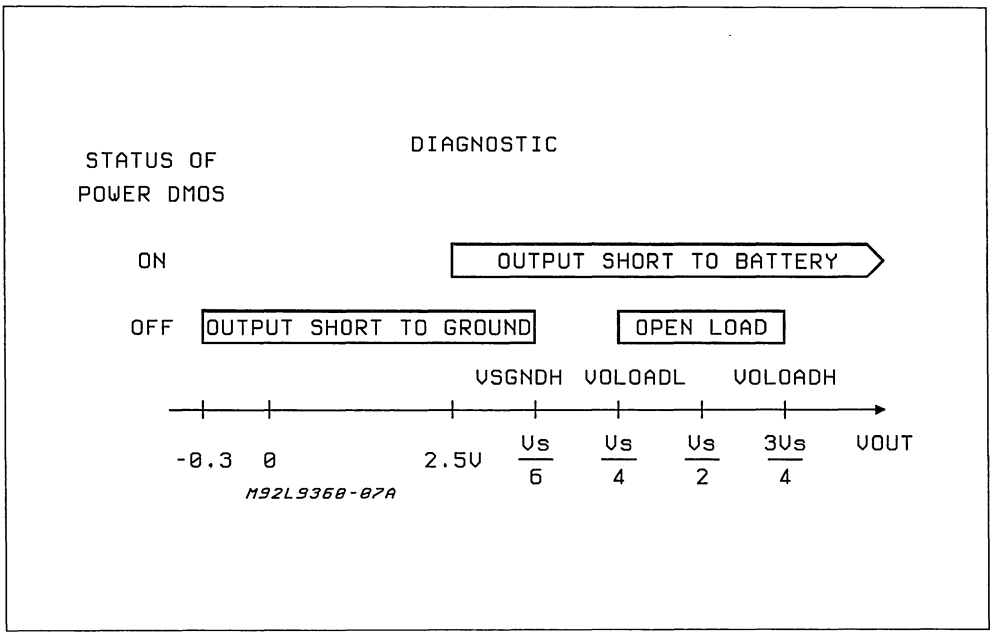


OUTPUT SHORT-CIRCUIT TO GND (BIT3/6) AND OPEN LOAD (BIT4/9).

In case of the switched off power DMOS the internal 20K resistors R_1 and R_2 divide the output voltage to half the supply voltage without load (fig.5).

A window comparator detects the output voltage and sets the "open load" BIT if the voltage deviates more than +/-0.25V_S from 0.5V_S. But if the output voltage decreases below 0.16V_S the "output short circuit to ground" BIT is set.

Figure 6: Diagnostic Detection Voltage Range



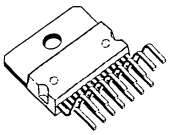
SGS-THOMSON MICROELECTRONICS

L9363

QUAD INTEGRATED LOW SIDE DRIVER

ADVANCE DATA

- LOW ON RESISTANCE (0.25Ω EACH OUTPUT)
- VARIOUS FAULT SITUATION DETECTOR (SHORT CIRCUIT, OPEN LOAD)
- LOAD DUMP PROTECTION
- OVER-VOLTAGE PROTECTION
- INDIVIDUAL OUTPUT OVER-CURRENT PROTECTION
- CLAMPING VOLTAGE (HIGHER THAN 60V) FOR DRIVING INDUCTIVE LOAD



MULTIWATT 15

ORDERING NUMBER: L9363

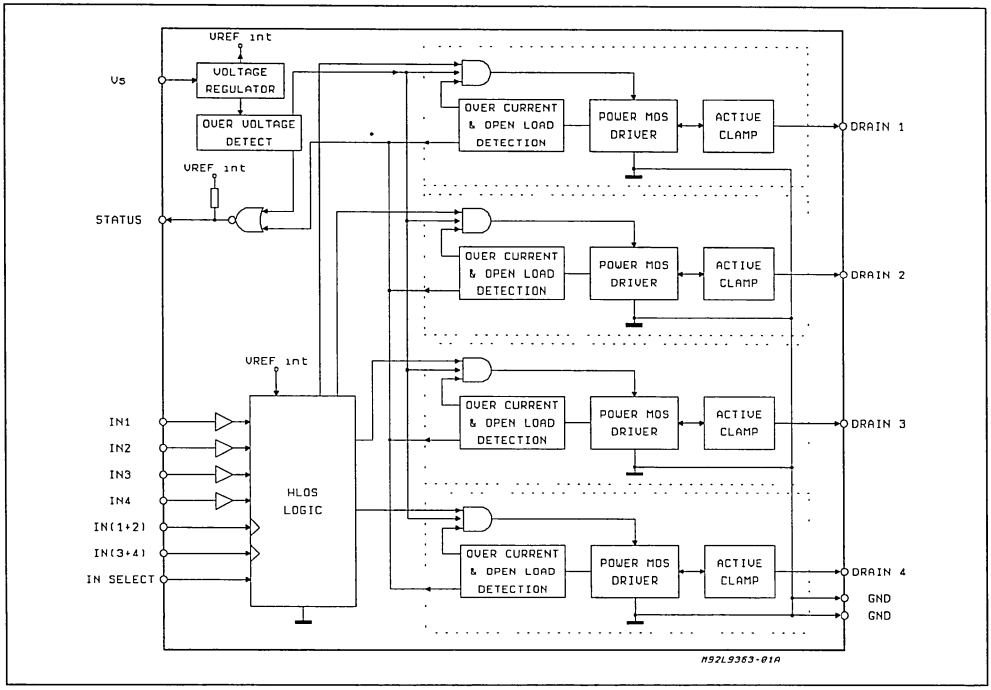
DESCRIPTION

The L9363 is a monolithic quad low side driver with DMOS outputs, designed for automotive environment especially in the injectors driving field.

Each output has a dedicated overcurrent protection and the device is overvoltage protected. The Status pin provides the microprocessor with the fault status feedback.

The device is housed in a Multiwatt 15 pin package. An internal zener diode connected between the source and the drain of each power DMOS allows a fast recirculation with a clamping voltage higher than 60V.

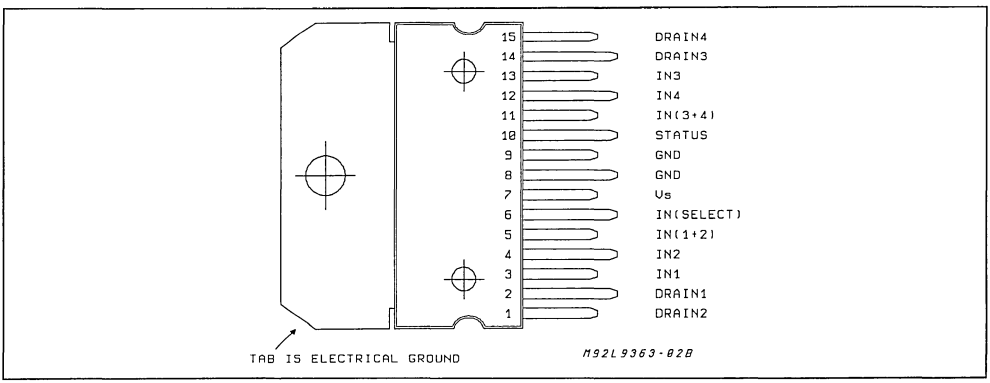
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	0 to 25	V
V_{STR}	Transient Supply Voltage	-1.5 to 60	V
V_{Cp}	Peak Clamping Voltage (Id = 20mA)	60 to 80	V
f_{max}	Ouperating Frequency	400	Hz
I_d	Drain Current Self Limiting (min)	3	A
V_{IN}	Input Voltage	-0.5 to 7.5	V
P_{tot}	Total Power Dissipation (max 25 °C)	42	W
T_j T_{stg}	Junction and Storage Temperature Range	-40 to 150	°C

BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	35	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction to case	3	°C/W

PIN FUNCTIONS

Pin	Symbols	Functions
1,2,14,15	DRAINS	Outputs 2, 1, 3, 4 respectively
3,4,13,12	IN	Input 1,2,3,4 respectively
5	IN (1+2)	This input pin drives output 1 and 2 in the same time when the IN select pin is "HIGH"
6	IN Select	This pin selects which input will be used to drive the outputs. When this pin is "LOW" the normal input pins drive the outputs. When it's "HIGH", the IN (x + y) (see below) drive the outputs.
7	V_S	This pin is connected to V_{bat}.
8,9	GND	Ground
10	STATUS	This pin provides fault status information about the device. The following faults will be indicated by a low state on this pin: 1) Short to V_{bat} or overcurrent condition on any output, 2) Open load condition on any output. 3) Over-voltage shutdown mode.
11	IN (3+4)	This input pin drives output 3 and 4 in the same time when the IN select pin is ":HIGH"

ELECTRICAL CHARACTERISTICS (V_S = 5.5 to 14.5V, T_j = –40 to 125°C unless otherwise specified;

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{S\ \&\ DRAIN}$	Operating Supply Voltage and Outputs		5.5		25	V
V_{IH}	Input High Voltage	I_D = 1A	3.0			V
V_{Ihyst}	Input High Voltage Hysteresis	I_D = 1A	0.4			V
V_{IL}	Input Low Voltage	I_D = 80µA			0.8	V
I_{IH}	Input High Current	V_I = 3V			50	µA
I_{IL}	Input Low Current	V_I = 0.8V			50	µA
I_{DSS}	Zero Input Voltage Drain Current	V_S = 14.5V; V_{LD} = 25V V_{LD} = 58V			500 2	µA mA
I_S	Logic Supply Current	VS = 13V; V_I = 0.4V			7	mA
$I_{d(lim)}$	On State Limiting Current	V_S = 13V; V_I = 5V	3.0			A
R_{dson}	Drain Source On Resistance	V_S = 13V; I_D = 1A; T_j = 25°C V_S = 8V; I_D = 0.7A; T_j = 25°C V_S = 5.5V; I_D = 0.4A; T_j = 25°C V_S = 13V; I_D = 1A; T_j = 125°C V_S = 13V; I_D = 1A; T_j = –40°C			0.25 0.4 0.5 0.5 0.25	Ω Ω Ω Ω Ω
t_{SS}	Short Circuit Sense Time (fig 2 and 3)	V_I = 5V; R_L = 0.05Ω; V_S ≥ 9V t_{SSAND}, t_{ref} must be set such that the short circuit duty cicle $t_{SS}/(t_{SS}+t_{ref})$ is less than 10%	10		250	µs
t_{ref}	Short Circuit Refresh Time (fig 2 and 3)	V_I = 5V; R_L = 0.05Ω; V_S ≥ 9V	1.5		7	ms
t_{SOFF}	Open Load Off Sense time (fig. 4)	V_S = 13V; V_I = 5V; Open Load	1.0	20	40	µs
t_{SON}	Open Load On Sense time (fig. 5)	V_S = 13V; V_I = 5V; Open Load	1.0	2	4.0	ms
t_{STO}	Fault Status Off Time (fig.2 and 3)	V_S = 13V; V_I = 5V; R_L = 0.05Ω; or Open Load		3	10	µs
t_{PHL}	Turn on Delay Time (fig.1)	V_S = 13V; R_L = 30Ω;		2	10	µs
t_{PLH}	Turn off Delay Time (fig.1)	V_S = 13V; R_L = 30Ω;		7.5	15	µs
t_r	Rise Time (fig.1)	V_S = 13V; R_L = 30Ω;		5.0	10	µs
t_f	Fall Time (fig.1)	V_S = 13V; R_L = 30Ω;		5.0	10	µs
	Device Turn On Threshould			5		V
	Over Voltage Shutdown Threshold		30		38	V
	Over Voltage Reset Hysteresis			5	7	V
	Status Low Voltage	I_{stl} = 10mA Open Load			0.4	V
	Status High Voltage	I_{stlh} = 30µA Open Load	3.0		5.5	V
Vooff	Open Load "OFF" Detection Voltage	V_S = 13V; V_I = 0V Open Load (fig. 4)	2.4		5	V
	Open Load Detection Current	V_S = 13V; V_I = 5V Open Load (fig. 5) T_j = 125°C T_j = 25°C T_j = 40°C		80 110 150	100 130 190	mA mA mA

FAULT LOGIC OPERATION

Faults conditions include fully shorted or partially shorted loads, open loads and overvoltage at Vs. An overvoltage condition will shutdown all the outputs while a shorted load will only shutdown the affected output. In either case the device shall resume normal operation when the fault situation no longer exists. The STATUS pin shall indicate a fault for any of the fault conditions described above. The fault status for overcurrent and open load conditions acts individually for each output, while overvoltage shutdown acts independently from the input. The output and STATUS line operation for each type of fault is described in more detail below.

SHORT TO V_S / OVER CURRENT FAULT

The status line will switch to a low level as long as the input is high, if the output current corresponding to that input reaches the Current Limit, $I_{D(lim)}$,

specified in the electrical specification for a period of time in excess of t_{SS}.

This condition indicates an over current fault and will cause that output to shutdown regardless of its input value, while other outputs will continue normal operation. As long as the input remains high, the device will continually retry energizing the load at a frequency defined by the Refresh Time, T_{ref}. The sense time and refresh time will determine the duty cycle at which a shorted load will be driven. This duty cycle must not cause the driver to exceed its thermal capabilities. During the overcurrent sense time the status C_{pin} will be at a high level and current limiting will take effect during the over current sense time. After the over current condition is removed, the output driver will operate normally and the Status line will remain high when that output is energized. Refer to Figure 2 & 3 for the over current condition waveforms.

OPEN LOAD FAULT

The status line will switch to a low level, if:

1) while all outputs are off, a drain voltage falls below the Open Load "OFF" Detection Voltage, V_{Ooff}, for a time exceeding the Open Load "OFF" Sense Time, tosoff, or
2) when an output is energized, that drain current fails to exceed the Open Load Detection Current, I_{oson}, after the Open Load On Sense Time, t_{oson}.

In case 1 the status line will remain low until the voltage level at that drain exceeds V_{Ooff} or until a non-faulted output is energized. In case 2 the Status line will remain low until the current is greater than I_{oson} or until that output is turned off. After the open condition is removed, the output will operate normally and the Status line will no longer indicat a fault.

Refer to Figure 4 & 5 for the open load condition waveforms.

OVER VOLTAGE SHUTDOWN

All outputs are disabled when V_S level exceeds the Overvoltage Shutdown threshold. In addition if any outputs are on when this condition occur, it will shutdown and STATUS pin will switch to a low level.

When V_S has dropped the Over Voltage Hysteresis, V_{ovhyst}, it has returned to a normal operating voltage, the Status line will switch high, and the device will resume normal operation.

INTEGRATED DRIVER FUNCTION TABLE

MODE OF OPERATION	STATUS	IN SELECT	IN (1+2)	IN (3+4)	IN1 & IN2 (note 1)	OUT 1 & OUT 2 (note 1)	IN 3 & IN 4 (note 1)	OUT 3 & OUT 4 (note 1)
NORMAL OPERATION	H H	L L	X X	X X	L H	H L	L H	H L
IN-SELECT MODE	H (note 2) H (note 2) H (note 2) H (note 2)	H H H H	H H L L	H L H L	X X X X	L L H H	X X X X	L H L H
OVER VOLTAGE SHUTDOWN (note 3)	L	X	X	X	X	H (note 3)	X	H (note 3)
OPEN LOAD FAULT "ON" (OFF") (note 4)	H(L) (note 4) L	X X	X X	X X	L H	? L	L H	? L
SHORT TO V_{bat} OVER CURRENT (note 5)	H L	X X	X X	X X	L H	H H	L H	H H

H = HIGH LEVEL L = LOW LEVEL X = IRRELEVANT ? = UNKNOWN

NOTES;

1. Inputs and outputs 1-4 are independent in normal operation. when one output is faulted the other three outputs will operate normally.
2. IN Select Mode outputs 1 & 2 are driven by IN (1+2) and outputs 3 & 4 are driven by IN (3+4). Depending on the load type and its mode of operation, the IN (x+y) inputs can be high, low, or pulse width modulated. Status is high except under a fault condition.
3. Over-voltage shutdown occurs when V_S exceeds the normal operating range. This condition disables ALL outputs regardless of the input values and causes the Status to go low.
4. The Status pin reveals the Open Load fault when the drain current fails to exceed a minimum level when an output is on; or when all outputs are off and a drain voltage falls below the minimum level expected when the output is off. See figures 4 and 5.
5. Short to Vbat/Over Current Shutdown occurs when the energized output's drain current reaches the current limit and the Over Current Sense time has elapsed. The Status pin indicates this fault only when the faulted driver is energized.

VOLTAGE CLAMP

Each output of each device provides active clamping of positive voltage transients due to the specified inductive loads.

IN SELECT OPERATION

In Select mode the IN-Select pin will be pulled to a high level. The device will than disable the normal inputs and enable the IN (x+y) Inputs. IN (1+2) will control outputs 1 and 2, while IN (3+4) will control outputs 3 and 4.

CURRENT LIMITING

Current limiting protection is provided individually to each output. If a load becomes shorted causing full battery voltage to be applied to the drain or any over current condition, the maximum drain current will be limited as specified in the electrical specifications. Normal device functioning with no degradation will resume upon removal of the over current condition. This current limiting for the time period needed for a shorted load to be sensed, t_{SS}, shall provide additional protection to the output until the current shutdown can take effect.

SYSTEM ACTUATOR

The system actuators are typically 13.8 ± 0.5Ω and 6.8 ± 0.7mH or 14.5 ± 0.72Ω and 7.2 ± 0.7mH (for fuel injectors and cold start injector). Other system actuators to be driven are variable cam timing solenoids which are 14.5 ± 0.72Ω and 20 ± 1 mH, shift solenoids which range from 15.7 ± 0.5Ω to 28 ± 2Ω and 24 ± 2 mH to 70 ± 35mH, fuel pump relay of 90 ± 10Ω and 130 ± 10mH and a GE194 incandescent light bulb (0.27A typ 2.7A cold inrush).

All drain (outputs) have a 0.001µF filter capacitor connected to case ground. The drains may also have an external high resistance (approximately 200KΩ) to ground for more accurate open load detection. Unused drain pins require 20KΩ tied to V_S to prevent false "off state' open load detecting and reporting.

All loads must be powered by module V_S to protect the device from full transient on V_S.

Figure 1: Response Times.

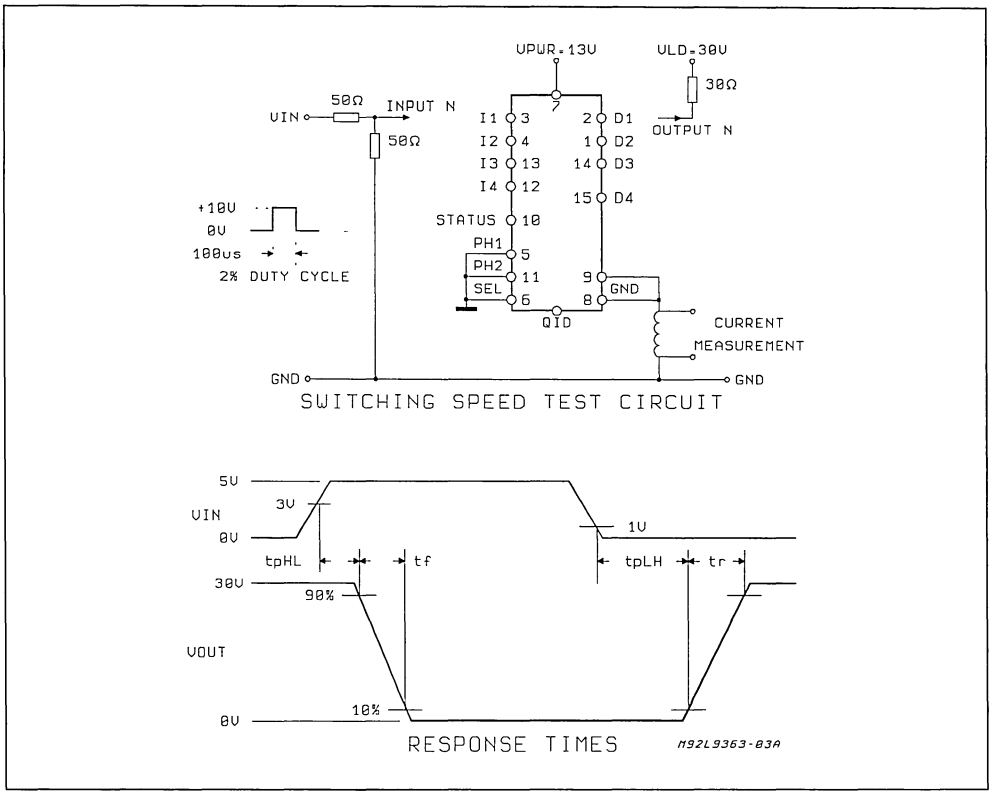


Figure 2: Over Current Status Operation

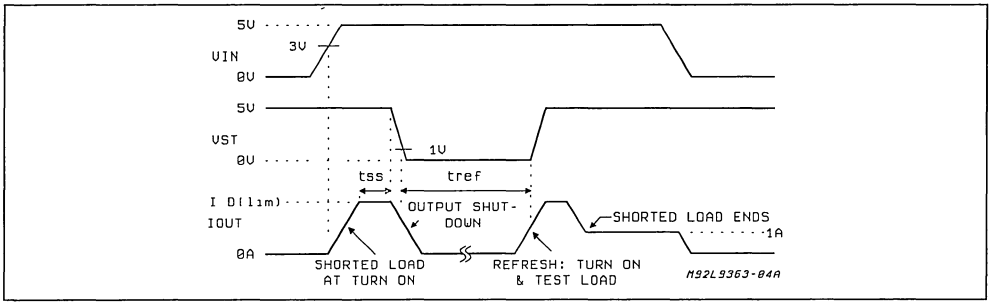


Figure 3: Over Current Status Operation

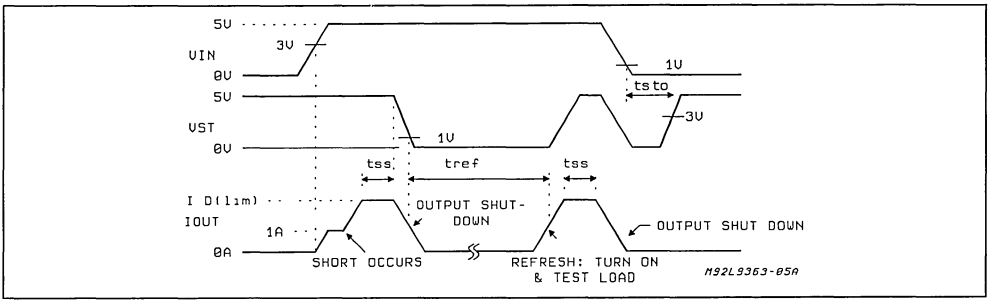


Figure 4: Off State Open Load Status Operation

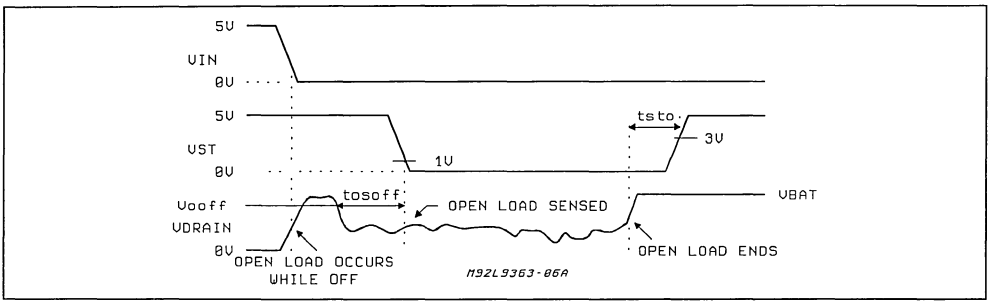
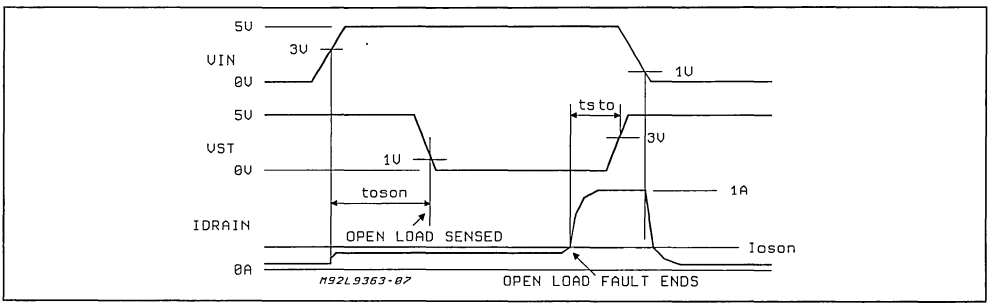


Figure 5: On State Open Load Status Operation



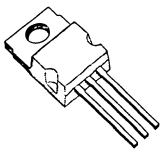
SGS-THOMSON MICROELECTRONICS

L9444VB/L9448VB L9480VB

ONE CHIP CAR ALTERNATOR REGULATOR

ADVANCE DATA

- NO EXTERNAL COMPONENTS
- PRECISE TEMPERATURE COEFFICIENT
- PRECISE REGULATED VOLTAGE
- HIGH OUTPUT CURRENT
- SHORT CIRCUIT PROTECTED
- REVERSE BATTERY PROTECTION
- + 80 V LOAD DUMP PROTECTION
- LOW ENERGY SPIKE PROTECTION
- THERMAL SHUTDOWN
- VERY LOW START UP VOLTAGE



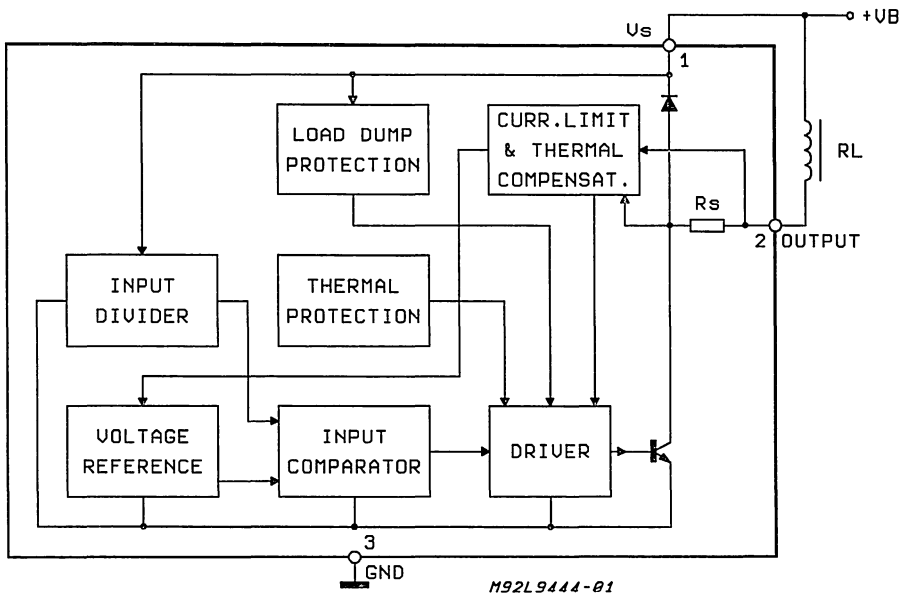
TO220

ORDERING NUMBER: L9444VB
L9448VB
L9480VB

DESCRIPTION

The devices are a "single function" self-oscillating voltage regulator for car alternators. Integrating both the control section and the output power stage on a single chip, the devices require no external components, reducing significantly the cost of the system and increasing reliability.

BLOCK DIAGRAM



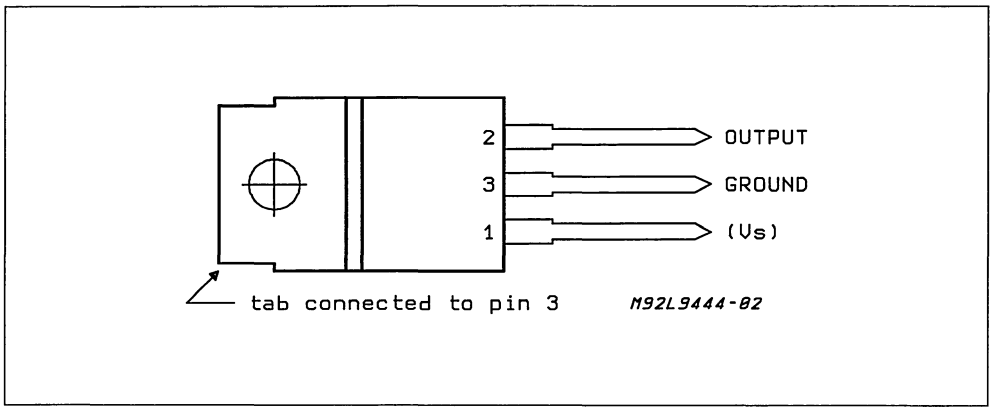
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Transient Overvoltage : Load Dump : 5ms ≤ T_{rise} ≤ 10ms, τ_f Fall Time Constant ≤ 100ms, R_{source} ≥ 0.5Ω	80	V
I_{clamp}	Current into Low Energy Clamping Zener (T_{rise} = 5µs ; T_{decay} ≤ 2ms ; duty cycle ≤ 5%)	100	mA
I_{out}	Maximum Output Current	5.5	A
T_j , T_{stg}	Junction and Storage Temperature Range	– 55 to + 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	3	°C/W

PIN CONNECTION (top view)



DEVICE OPERATION

The alternator voltage, rectified by the auxiliary diode trio, is compared with an external reference and the resulting signal switches the output stage, driving the alternator field coil.

As the regulator is a self-oscillating type, the switching frequency depends on the whole system parameter set (including the alternator characteristics).

The regulator has an integrated filter in the voltage sensing path. Consequently it doesn't need - in the standard application- any external component.

Anyway an external capacitor (0.1 - 1µF) must be inserted between V_S and Ground guaranteeing the correct behaviour of the device when the rectifying diodes feature very high switching spikes that are not filtered by the devices.

This external capacitor must also be used when the impedances of the cables connecting the alternator to the battery are so high to cause a superimposed ripple on the alternator voltage higher than 3-4V.

The devices regulation voltage and the temperature coefficient may be independently set by suited metal mask selections ; furthermore the regulation voltage is trimmed within ± 1% of the nominal value @ 25°C.

The devices have an unique -and patented- system to compensate the self-heating of the die due to the power dissipated in the output stage. In this way the internal reference voltage tracks the case temperature rather than the die one.

The device can withstand the reverse battery and the load dump (up to 80V) ; They can absorb, into the internal clamping zeners, low energy spikes up to a level of 100mA and its output is short circuit protected.

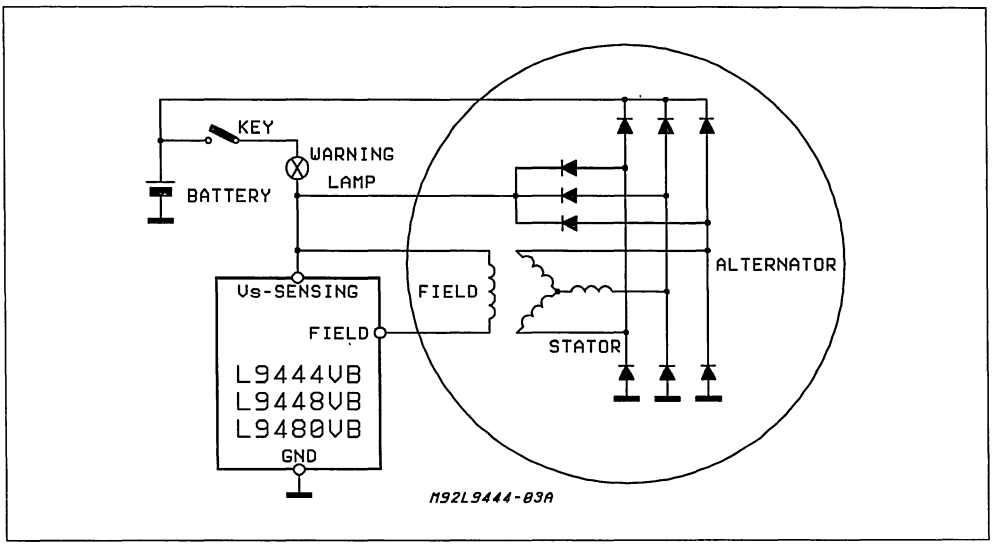
Finally the internal thermal shutdown avoids any possible device damage due to overtemperature problems.

ELECTRICAL CHARACTERISTICS (– 40 °C ≤ T_J ≤ 125 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_r	Regulation Voltage	T_j = –40°C for L9444VB	14.49	14.79	15.05	V
		for L9448VB	14.36	14.66	14.96	V
		for L9480VB	14.75	15.05	15.35	V
		T_j = 25°C	14.10	14.40	14.70	V
		T_j = 125°C for L9444VB	13.50	13.80	14.10	V
		for L9448VB	13.70	14.00	14.30	V
		for L9480VB	13.10	13.40	13.70	V
C_T	Temperature Coeff. of the Regulation Voltage	for L9444VB		- 6		mV/°C
		for L9448VB		- 4		mV/°C
		for L9480VB		- 10		mV/°C
eC_T	Error on Nominal Temperature Coeff.			± 30		%
V_r	Load Regualtion	0.1 I_n < I_{alt} < 0.9 I_n (note 1)		250		mV
V_{su}	Control Circuit Minimum Start up Voltage	Measured at Supply Pin		2	3	V
V_{sd}	Shutdown Voltage (dump protection threshold)			22		V
$V_{sat\,1}$	Output Saturation Voltage	I_{field} = 4 A_p		1.2	2	V
$V_{sat\,2}$	Start Up Saturation Voltage	I_{field} = 200 mA		0.7	1	V
I_q	Quiescent Current	Field Off		20		mA
I_s	Supply Current	I_{field} = 4 A_p		50		mA
I_{fs}	Field Pin Sink Current	Field Off			5	mA
		Field Pin @ 16 V				
$V_{1\,CLAMP}$	Low Energy Clamping Zener Voltage	I_{clamp} = 50 mA		120		V
f_{sw}	Switching Frequency	01 I_n < I_{alt} < 0.9 I_n	30		1000	Hz

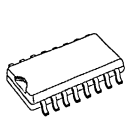
Note1: measured on an alternator with the following characteristics: I_n =<90A; I_{alt}/I_{field} >= 23

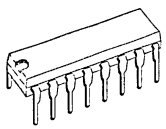
APPLICATION CIRCUIT



PWM POWER MOS CONTROLLER

- HIGH EFFICIENCY DUE TO PWM CONTROL AND POWERMOS DRIVER
- LOAD DUMP PROTECTION
- LOAD POWER LIMITATION
- EXTERNAL POWERMOS PROTECTION
- LIMITED OUTPUT VOLTAGE SLEW RATE





SO16 **DIP16**

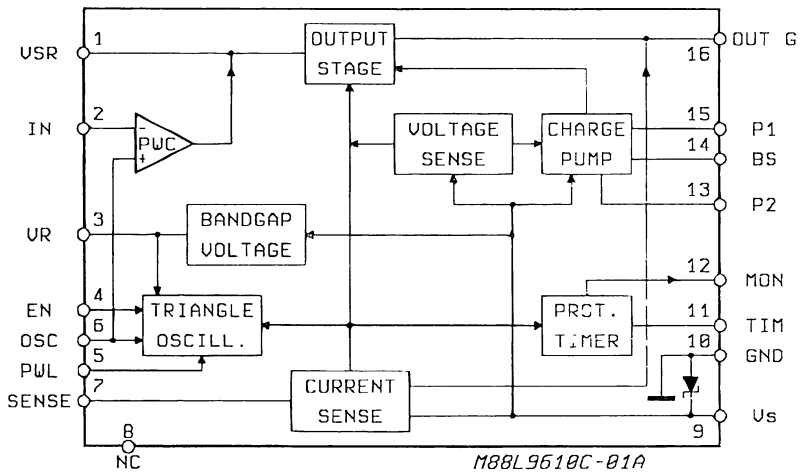
ORDERING NUMBERS: L9610C
L9611C

DESCRIPTION

The L9610C/11C is a monolithic integrated circuit working in PWM mode as controller of an external powerMOS transistor in High Side Driver configuration.

Features of the device include controlled slope of the leading and trailing edge of the gate driving voltage, linear current limiting with protection timer, settable switching frequency fo, TTL compatible enable function, protection status ouput pin. The device is mounted in SO16 micropackage, and DIP16 package.

BLOCK DIAGRAM



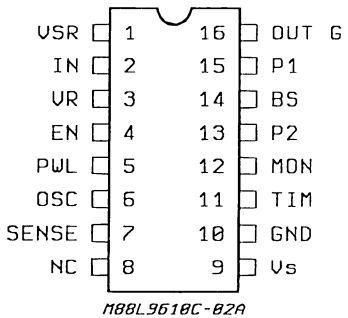
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	D.C. Supply Voltage	26	V
	Transient Peak Supply voltage ($R_1 \geq 100\Omega$) :		
	Load Dump : $5ms \leq t_{rise} \leq 10ms$ τ_f Fall Time Constant = 100ms $R_{SOURCE} \geq 0.5\Omega$	60	V
	Field Decay : $5ms \leq t_{fall} \leq 10ms$, $R_{SOURCE} \geq 10\Omega$ τ_r Rise Time Constant = 33ms	– 80	V
	Low Energy Spike : t_{rise} = 1µs, t_{Fall} = 2ms, $R_{SOURCE} \geq 10\Omega$	± 100	V
I_S	Maximum Supply Current (t < 300ms)	0.3	A
V_{IN}	Input Voltage	$-0.3 < V_{IN} < V_S - 2.5$	V
T_j, T_{STG}	Junction and Storage Temperature	– 55 to + 150	°C

THERMAL DATA

SO16J				
$R_{th\ j\text{-}a}$	Thermal Resistance Junction-alumina	Max	50	°C/W
DIP16				
$R_{th\ j\text{-}a}$	Thermal Resistance Junction-ambient	Max	90	°C/W

PIN CONNECTION (Top view)



PIN FUNCTIONS

Pin	Name	Functions
1	VSR	A capacitor connected between this pin and Out_G defines the GATE Voltage Slew Rate.
2	IN	Analog Input Controlling the PWM Ratio. The operating range of the input voltage is 0 to V_R.
3	V_R	Output of an Internal Voltage Reference
4	EN	TTL Compatible Input for Switching off the Output
5	PWL	If this pin is Connected to GND and V_S > 13V, the duty cycle and the frequency fo are reduced : this allows to transfer a costant power to the load.
6	Osc	The capacitor connected to this pin defines the frequency of the internal triangle oscillator.
7	SENSE	Input of an Operational Amplifier for Short Current Sensing and Regulation.
8	NC	Not Connected.
9	V_S	Common Supply Voltage Input
10	GND	Common Ground Connection
11	TIM	A capacitor connected between this pin and GND defines the protection delay time.
12	MON	Open Collector Monitoring Output off the PowerMOS Protection.
13,15	P2, P1	Connection for the Charge Pump Capacitor.
14	BS	The Capacitor Connected between this Pin and the Source of the Power MOS Allows to Bootstrap the Gate Driving Voltage.
16	Out G	Output for Driving the Gate of the External PowerMOS.

ELECTRICAL CHARACTERISITCS (T_{amb} = – 40 °C to 85 °C ; 6 V < V_S < 16 V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage		6		16	V
I_q	Quiescent Current			2.5	6	mA
V_{SC}	Internal Supply Voltage Clamp	I_S = 200mA	28	32	36	V
V_{SH}	Supply Voltage High Threshold		16	18.5	21	V
V_{SL}	Supply Voltage Low Threshold		4	5	6	V
V_R	Reference Voltage		3.3	3.5	3.7	V
I_R	Reference Current	$\Delta V_R \leq$ 100mV			1	mA
V_{INL}	Input Low Threshold		0.13	0.15	0.2	V_{IN}/V_R
K_F	Oscillator Freq. Constant	Note 1	800		2500	nF/s
K_S	Gate Voltage Slew Rate Constant	Note 2	3	5	9	nFV/ms
K_T	Protection Time Delay Constant	Note 3	0.12		0.44	ms/nF
V_{Si}	Sense Input Volt.		80	100	120	mV
V_{GON}	Gate Driving Volt. above V_S	V_S = 16V	8		16	V
V_{GOFF}	Gate Voltage in OFF Condition	I_G = 100 µA			1.2	V
I_{IN}	Input Current		– 5	– 1		µA
V_{ENL}	Low Enable Voltage				0.8	V
V_{ENH}	High Enable Voltage		2.0			V
IEN	Enable Input Current				2	µA
SR	Slew Rate	Without C_S		0.5		V/µs
V_{MONsat}	Saturation Voltage (pin 12)	I_{MON} = 2 5 mA			1.5	V

Notes : 1. $f_o = K_F/C_F$.
2. $dV_G/dt = K_S/C_S$.
3. $t_{prot} = K_T C_T$.

FUNCTIONAL DESCRIPTION

PULSE WIDTH COMPARATOR

A ground compatible comparator generates the PWM signal which controls the gate of the external powerMOS.

The slopes of the leading and trailing edges of the gate driving signal are defined by the external capacitor C_S according to :

$$dV_G/dt = K_S/C_S$$

This feature allows to optimize the switching speed for the power and RFI performance best suited for the application.

The lower limit of the duty cycle is fixed at 15 % of the ratio between the input and the reference voltage (see fig. 1). Input voltages lower than this value disable the internal oscillator signal and therefore the gate driver.

GROUND COMPATIBLE TRIANGLE OSCILLATOR

The triangle oscillator provides the switching frequency f_o set by the external capacitor C_F according to :

$$f_o = K_F/C_F$$

If the pin PWL (power limitation) is connected to ground and Vs is higher than the PWL threshold voltage, the duty cycle and the f_o frequency are reduced : this allows to transfer a costant power to the load (see fig. 2).

TIMER AND PROTECTION LATCH

When an overcurrent occurs, the device starts charging the external capacitor C_T ; the protection time is set according to :

$$t_{prot} = K_T \cdot C_T$$

After the overcurrent protection time is reached, the powerMOS is switched-off ; this condition is latched by setting an internal flip-flop and is externally monitored by the low state of the MON pin.

To reset the latch the supply voltage has to fall below V_{SL} or the device must be switched off.

UNDER AND OVERVOLTAGE SENSE WITH LOAD DUMP PROTECTION

The undervoltage detection feature resets the timer and switches off the output driving signal when the supply voltage is less than V_{SL}.

If the supply voltage exceeds the max operating supply voltage value, an internal comparator disables the charge pump, the oscillator and the external powerMOS.

In both cases the thresholds are provided with suitable hysteresis values.

The load dump protection function allows the device to withstand - for a limited time - high overvoltages. It consists of an active clamping diode which limits the circuit supply voltage to V_{CLAMP} and an external current limiting resistor R1. The maximum pulse supply current (see abs. max. ratings is equal to 0.3A. Therefore the maximum load dump voltage is given by :

$$V_{DUMP} = V_{SC} + 0.3R_1$$

In this condition the gate of the powerMOS is held at the GND pin potential and thus the load voltage is :

$$V_L = V_S - V_{CLAMP} - V_{GS}$$

Figure 1 : Typical Transfer Curve.

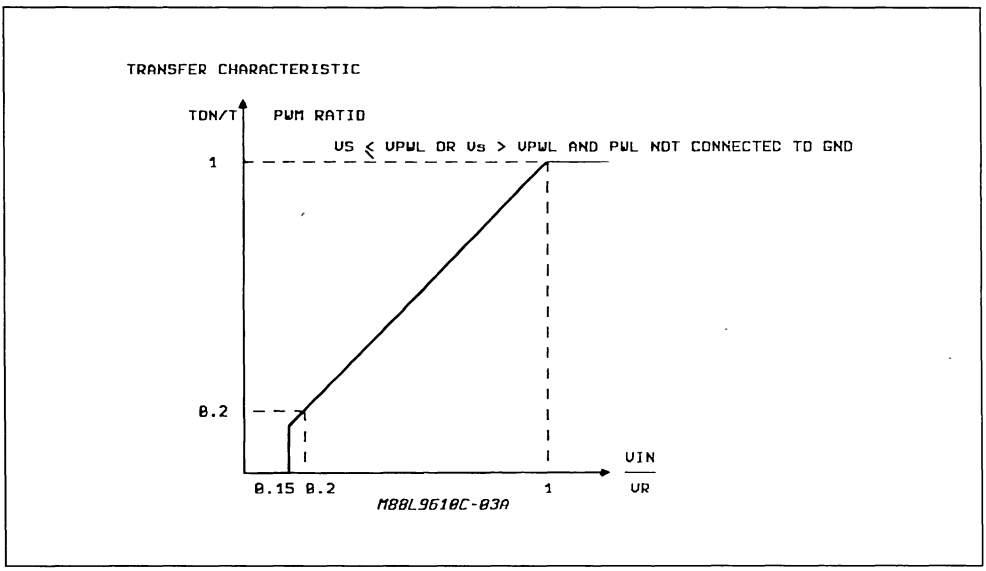
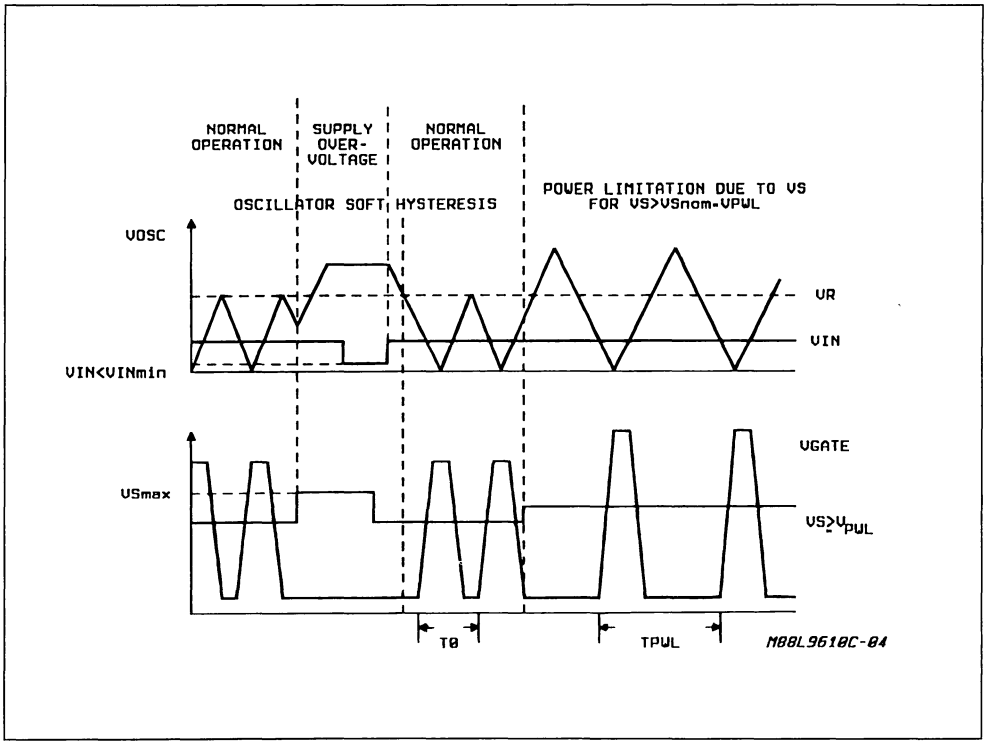


Figure 2 : The Typical Waveforms for the Power Limitation Function.



SHORT CIRCUIT CURRENT REGULATION

The maximum load current in the short circuit condition can be chosen by the value of the current sensing resistor R_S according to :

$$I_{SC} = V_{SI}/R_S$$

Two identical V_S compatible comparators are provided to realize the short circuit protection.

After reaching the lower threshold voltage (typical value V_{SI}-10 mV), the first comparator enables the timer and the gate is driven with the full continuous pump voltage : when the upper threshold voltage value is reached the second comparator maintains the chosen I_{SC} driving the NMOS gate in continuous mode.

This function - showed in fig. 3 - speeds up the switch on phase for a lamp as a load.

BANDGAP VOLTAGE REFERENCE

The circuit provides a reference voltage which may be used as control input voltage through a resistive divider. This reference is protected against the short circuit current.

CHARGE PUMP

The charge pump circuit holds the N-MOS gate above the supply voltage during the ON phase. This circuit consists of an RC astable which drives a comparator with a push-pull output stage. The external charge pump capacitor C_P must be at least equal to the NMOS parasitic input capacitance.

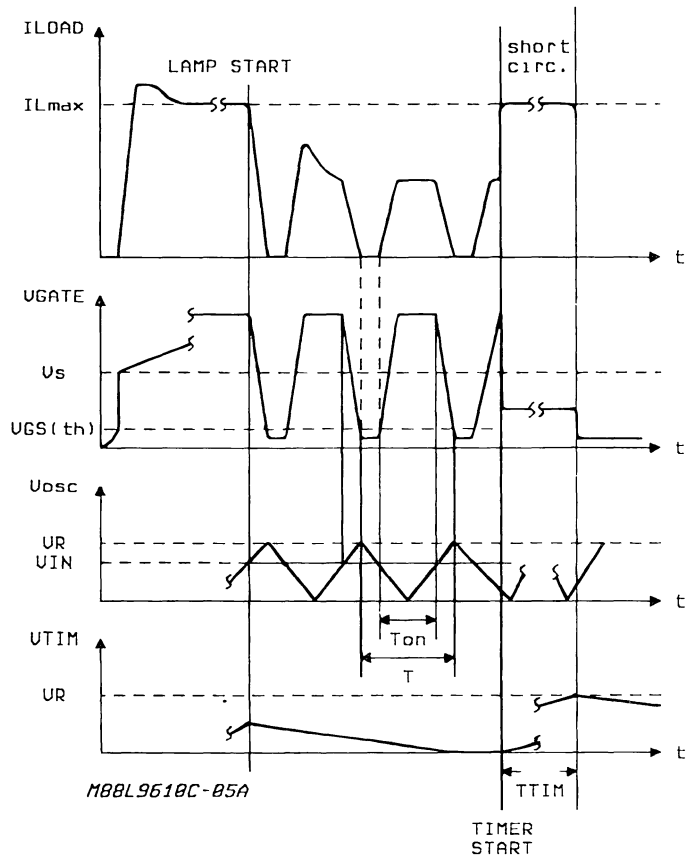
For fast gate voltage variation C_P must be increased or the bootstrap function can be used. The bootstrap capacitor should be at least 10 times greater than the powerMOS parasitic capacitance.

The charge pump voltage V_{PUMP} can reach to :

$$V_{PUMP} = 2\ V_S - V_{BE} - V_{CESAT}$$

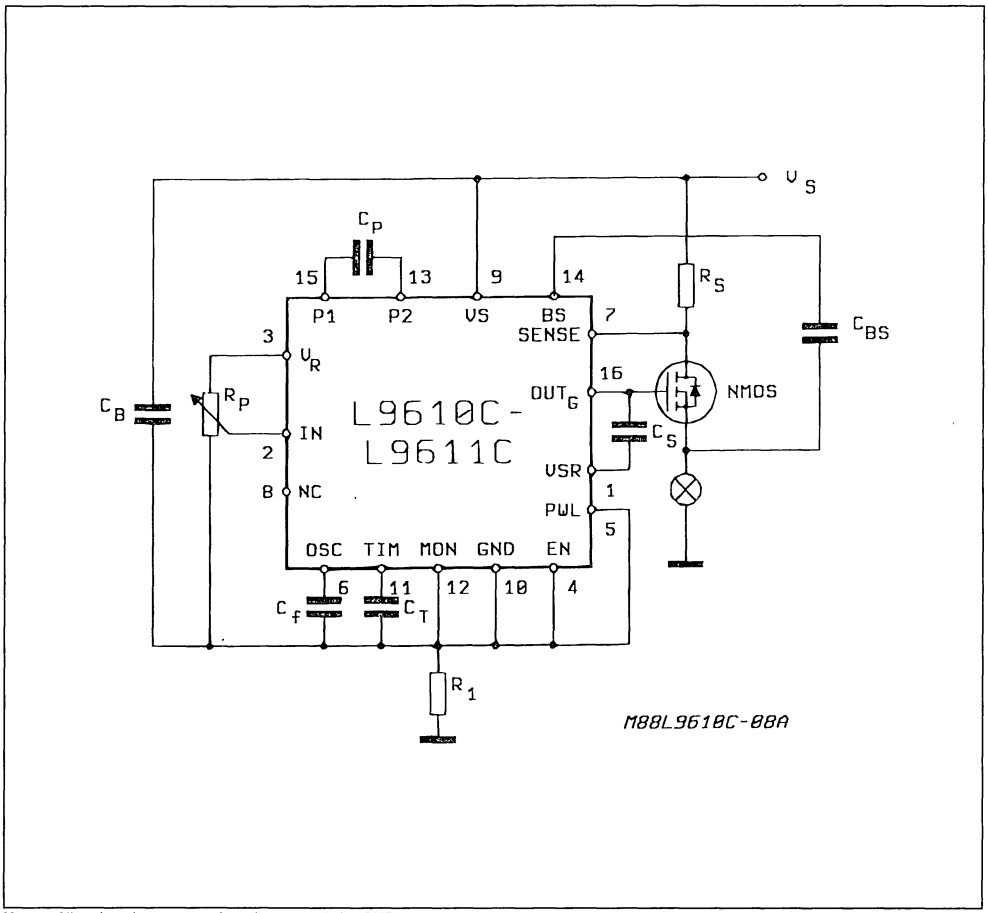
The circuit is disabled if the supply voltage is higher than V_{SH}.

Figure 3 : The Typical Waveforms for Short Circuit Current Condition.



APPLICATION CIRCUIT

Figure 4.



Note : All node voltages are referred to ground pin (GND)
The currents flowing in the arrow direction are assumed positive
without C_{BS} · C_P = 1nF
without C_{BS} . C_{BS} must be at least 10 times higher than the gate capacitance : C_P = 100 pF.

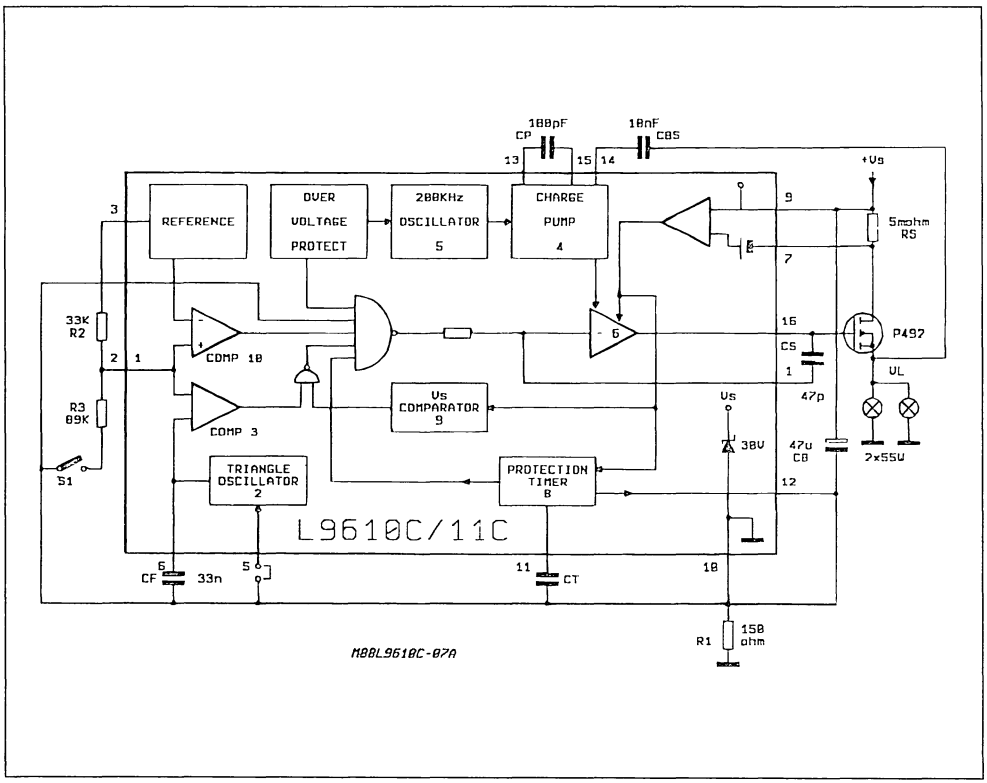
CONTROLLING A 120W HALOGEN LAMP WITH THE L9610C/11C DIMMER

The L9610C/11C Lamp Dimmer is used to control the brightness of vehicle headlamps using H4 type lamps (see fig. 5). With switch S1 open the full supply voltage is applied to the lamps : closing the switch it is a possible to reduce the average lamp voltage as desired :

$$VL = VS \frac{R3}{R2 + R3}$$

If pin 5 is connected to ground the average lamp voltage is constant, even for supply voltages in excess of 13 V.

Figure 5 : Application Circuit.



The sensing resistor R_S and timing capacitor C_t should be dimensioned according to :

$$R_S = \frac{V_{SI}}{2Inom\ (@Vs=14\ V)}$$

$$C_t = \frac{2 \times \text{limitation time}}{K_T}$$

In normal conditions (V_{CC} = 14 V, maximum brightness) the voltage drop across the sense resistor must be 50 mV. The current limiter intervenes at twice the nominal current, I_{nom}.

The timing capacitor C_t (V_{ct} = 3.5 V) must be chosen so that the delay before intervention is twice the duration of the current limitation at power-on.

The optimal value of the oscillator frequency, taking tolerances into account, must be slightly higher than the frequency at which lamp flicker is noticable (min 60 Hz).

The switching times are a compromise between possible EMI and switching power losses. The recommended value for Cs is 47pF.

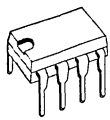
SGS-THOMSON MICROELECTRONICS

L9686

AUTOMOTIVE DIRECTION INDICATOR

ADVANCE DATA

- RELAY DRIVER IN CAR DIRECTION INDICATORS
- FLASH FREQUENCY DOUBLES TO INDICATE LAMP FAILURE
- DUMP PROTECTION (± 80 V)
- REVERSE BATTERY PROTECTION



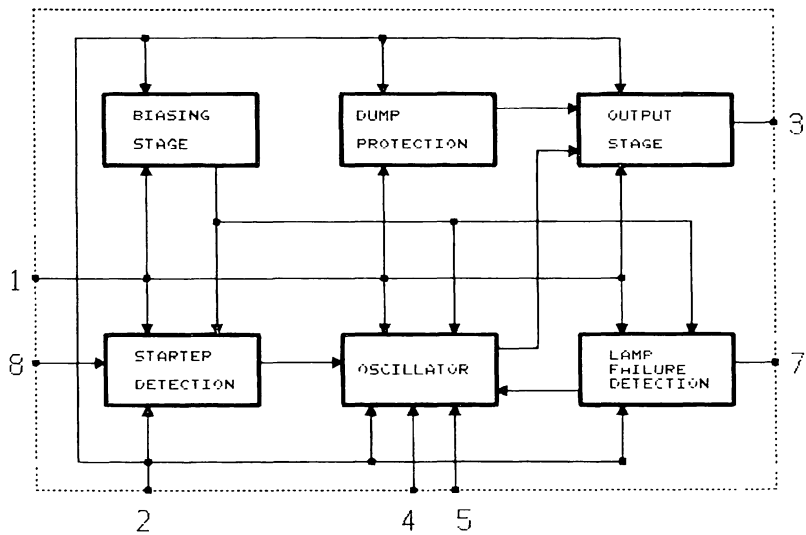
Minidip

ORDERING NUMBER: L9686

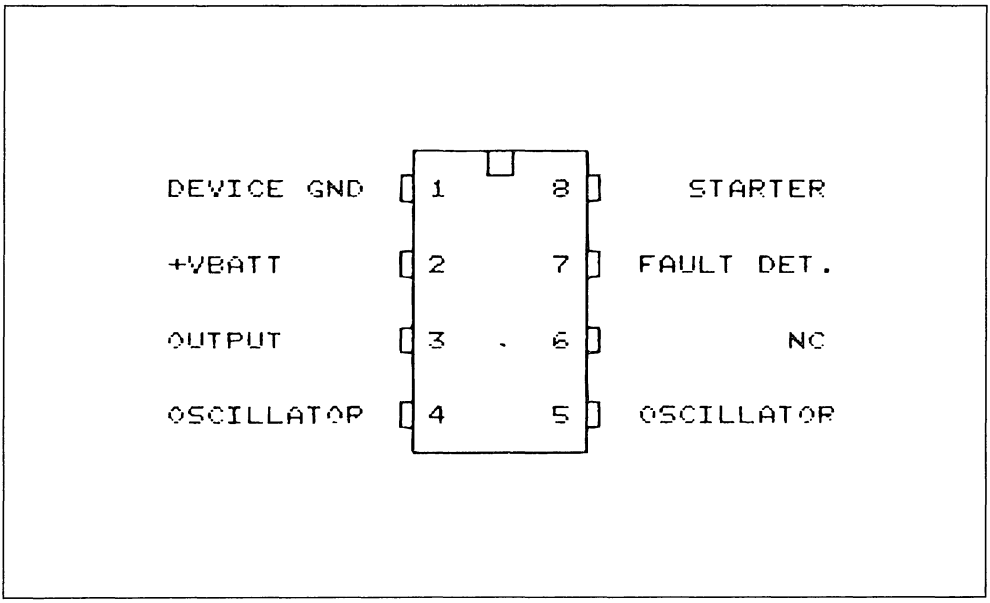
DESCRIPTION

The L9686 is a two frequency oscillator particularly suitable as relay driver for flashing light control in automotive applications. The circuit may be also used for other warning lamps like "handbrake on" etc. The lamp failure detection is given by doubling the flash repetition frequency. The L9686 is supplied in a minidip 8-lead plastic package.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Transient Peak Supply Voltage ($R_3 \geq 220\Omega$): Load Dump: $5ms \leq t_{rise} \leq 10ms$ τ_f Fall Time Constant = 100ms $R_{source} \geq 0.5\Omega$ Field Decay: $5ms \leq t_{fall} \leq 10ms$, $R_{source} \geq \Omega$ τ_r Rise Time Constant = 33ms Low Energy Spike: $t_{rise} = 1\mu s$, $t_{fall} = 2ms$, $R_{source} > 10\Omega$	 80 – 80 ± 100	 V V V
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C
P_{tot}	Total Power Dissipation at T_{amb} = 100°C	500	mW

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	100	°C/W

ELECTRICAL CHARACTERISTICS (– 20°C ≤ T_{amb} ≤, 100°C, 8V ≤ V_S ≤ 18V unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Operating Voltage		8		18	V
V2 – V1	Clamping Voltage	see note 1	27		34	V
V2 – V3	Output Saturation Voltage	I_{RL} = 250mA			1.7	V
R2	Starter Resistance	see note 2			3.6	KΩ
K_N	Oscillator Constant K_N (normal Operation)	Fn = 1/KnRoCo Osc. Frequency	1.27		1.74	
C_T	Temperature Coefficient of Kn	See Note 3		–1.5 · 10-3		1/°C
D.C.	Duty Cycle (normal operation)		45	50	55	%
K_C	Oscillator Constant K_C (lamp failure detection)	F_C = 1KcRoCo Osc. Frequency	0.53		0.74	
DC_{LF}	Duty Cicle (lamp failure detection)		35	40	45	%
I_Q	Current Consumption Relay off $I_{pin\ 1}$	V_S = 8V V_S = 13.5V V^S = 18V		2.2 2.7 3.3	3.9 4.3 4.7	mA mA mA
V_{th}	Lamp Failure Threshold (see note 4)	R_3 = 220Ω V_S = 13.5V –20 ≤ T_{amb} ≤ 100°C	65	85	95	mV

Notes : 1. This voltage is the threshold used to protect the circuit against overvoltage : if V_{bat} is > than this threshold, the relay will be on and the voltage across the circuit will maintain constant increasing the current in the protective resistor R_3

2. This is the maximum value for operation. This value must be higher than 1 K Ohms in order to limit the current in pin 8 during dumps. A recommended value for application should be 1,5 K Ohms.

3. The external leakage from the blinker unit to ground must be with an equivalent resistor higher than 5,6 K Ohms to avoid parasitic operation when the switch S_1 is off

4. This temperature coefficient is usefull to compensate the drift of the external timing network (R_1, C_1).

5. This threshold is calculated for a 20 m Ohm shunt. The threshold is dependant of V_{bat} as the bulb current.

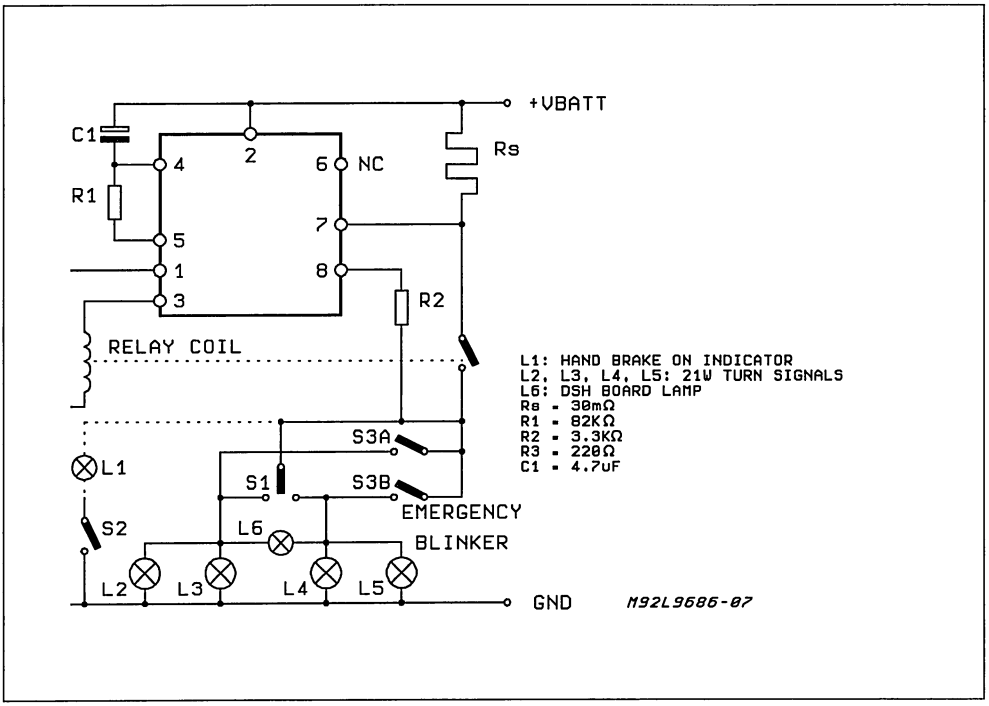
FUNCTIONAL DESCRIPTION

The circuit is designed to drive the direction indicator flasher relay. The application circuit shows the typical system configuration with the external components. Its consists of a network (R_1 C_1) to determine the oscillator frequency, shunt resistor (R_S) to detect defective bulbs and two current limiting resistors (R_2/R_3) to protect the IC against load dump transients.

The lightbulbs L_2, L_3, L_4, L_5, are the turn signal indicators with the dashboard-light L_6. The S_1 switch position is sensed across resistor R_2 and R_{lamp} by input 8. The flashing cycle is started by closing S_1 : then, after a delay time t_d typically equal to 1.5 ms, the relay is actuated and the pin 3 goes high switching on the corresponding lamps L_2, L_3, (or L_4, L_5). These lamps will flash at the oscillator frequency not depending on the battery voltage value (8 - 18 V). The flashing cycle stops and the circuit is reset to the initial position when the switch S_1 is open.

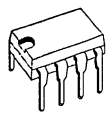
The lamp failure detection function senses the current through the shunt resistor R_S. When one of the lightbulbs is defective the voltage drop across R_S is reduced to a half and the failure is indicated by doubling the flashing frequency.

Figure 1: Application Circuit.



HEX PRECISION LIMITER

- HIGH PERFORMANCE CLAMPING AT GROUND AND POSITIVE REFERENCE VOLTAGE
- FAST ACTIVE CLAMPING
- OPERATING RANGE 4.75 - 5.25 V
- SINGLE VOLTAGE FOR SUPPLY AND POSITIVE REFERENCE
- LOW QUIESCENT CURRENT
- LOW INPUT LEAKAGE CURRENT



Minidip

ORDERING NUMBER : L9700

DESCRIPTION

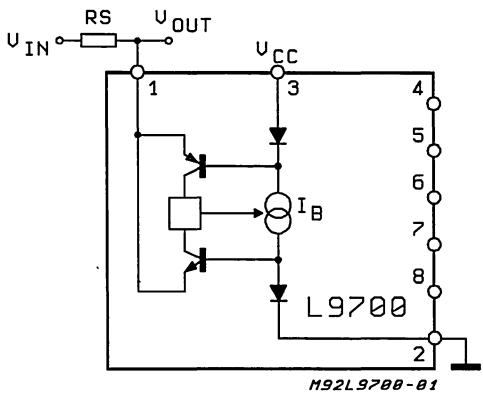
The L9700 is a monolithic circuit which is suited for input protection and voltage clamping purpose.

The limiting function is referred to ground and the positive supply voltage.

One single element contains six independent channels.

Very fast speed is achieved by internal feedback and the application of a new vertical PNP-transistor with isolated collector.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

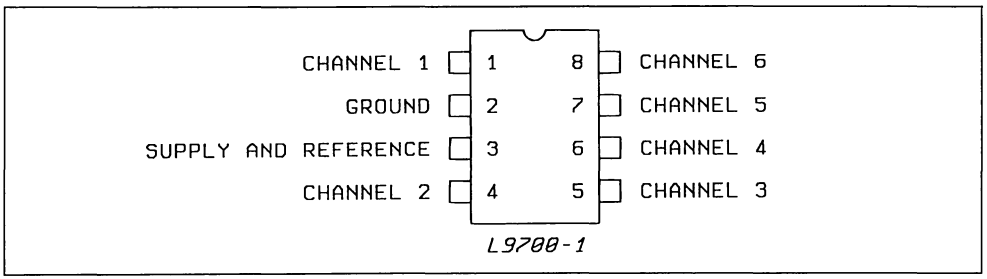
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	20	V
I_{IN}	Input Current per Channel	30	mA
T_j, T_{stg}	Junction and Storage Temperature	– 55 to 150	°C
P_D	Power Dissipation (T_A = 85°C)	650	mW

Note: The circuit is ESD protected according to MIL-STD-883C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

PIN CONNECTION



ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_j = – 40 to 125°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75		5.25	V
I_{CC}	Supply Current			1.5	3	mA
V_{cls}	Static Input Clamping Voltage Negative	I_{IN} = – 10mA	– 250		0	mV
	Positive	I_{IN} = + 10mA	V_{CC}		V_{CC} + 250	mV
I_{IN}	Input Current (static)	V_{IN} = 0 V_{IN} = V_{CC} V_{IN} = 50mV V_{IN} = V_{CC} – 50mV			15 15 5 5	µA µA µA µA
V_{cld} (*)	Dynamic Input Clamping Voltage Positive Overshoot Negative Overshoot	I_{in} = ± 10mA t_R = 5ns			 400 400	 mV mV
t_S (*)	Settling Time	See fig. 2			20	ns
R_{IN} (*)	Dynamic Input Resistance				5	Ω
C_{rtk} (*)	Crosstalk between any two Inputs	0 ≤ V_{IN} ≤ V_{CC}, f_{IN} < 1kHz		70		dB

(*) Design limits are guaranteed by statistical control on production samples over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Figure 1 : DC INPUT CHARACTERISTIC Limit Points of the Characteristic Approximation.

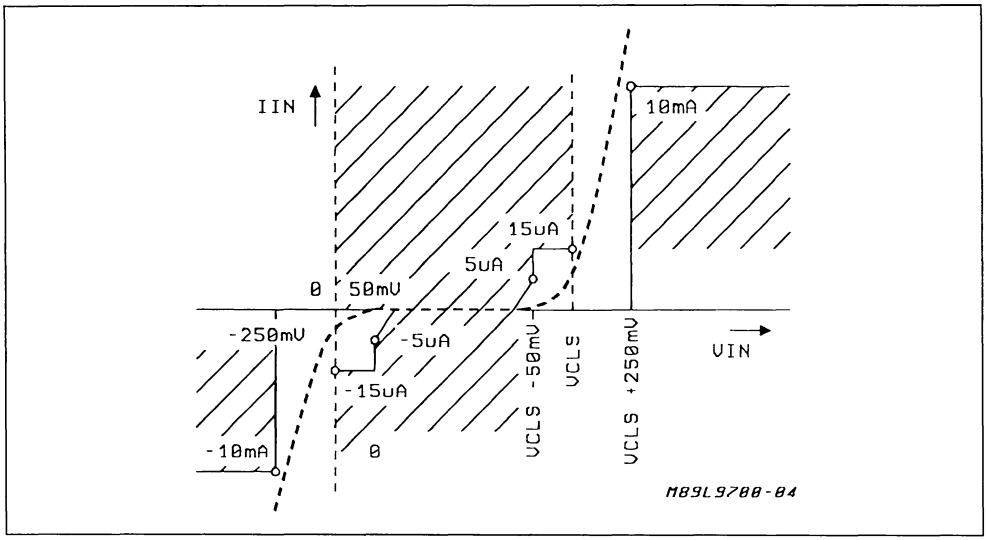


Figure 2 : Dynamical Input Characteristics.

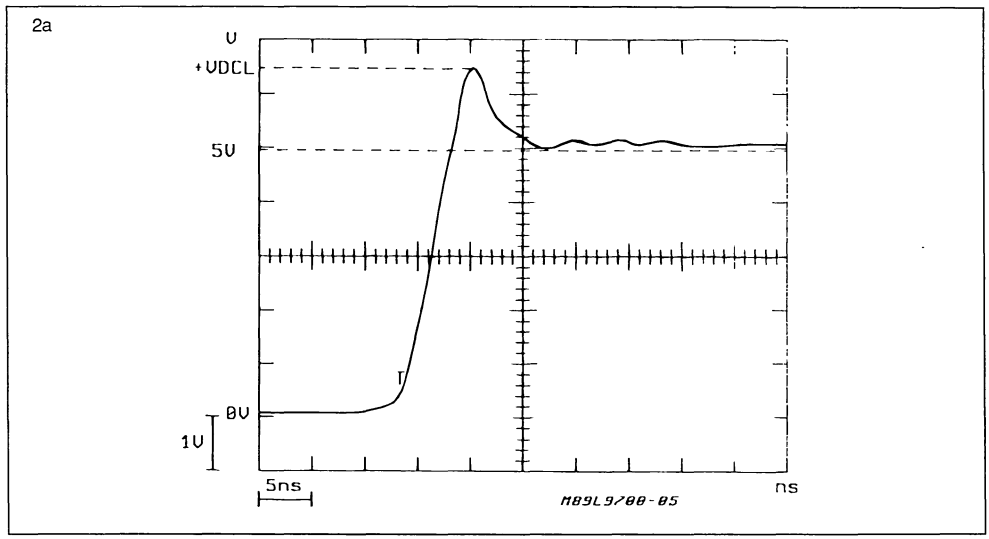
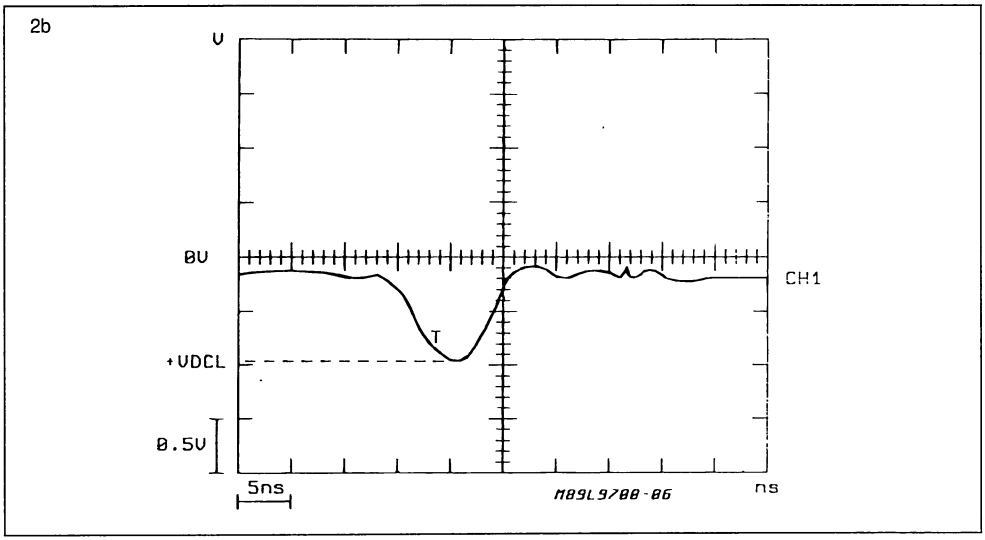


Figure 2 : Dynamical Input Characteristics (continued) .



APPLICATION INFORMATION

Most integrated circuits, both HNMOS and bipolar, are very sensitive to positive and negative overvoltages on the supply and at the inputs.

These transients occur in large numbers and with different magnitudes in the automotive environment, making adequate protection for devices aimed at it indispensible.

Overvoltages on the supply line are faced through high voltage integration technologies or through external protection (transil, varistor).

Signal inputs are generally protected using clamp diodes to the supply and ground, and a current limiter resistor. However, such solutions do not always completely satisfy the protection specifications in terms of intervention speed, negative clamping and current leakage high enough to change analog signals.

The L9700 device combines a high intervention speed with a high precision positive and negative clamp and a low current leakage providing the optimal solution to the problems of the automotive environment.

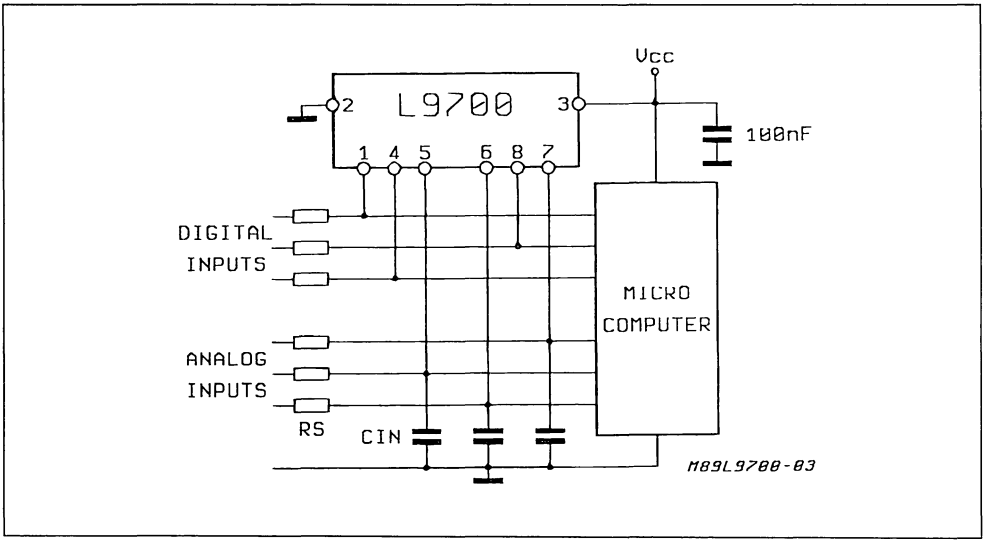
The high intervention speed, due to the pre-bias of the limiter stage and internal feedback, limits the voltage overshoot and avoid the use of external capacitors for the limitation of the transient rise times.

Figure 3 illustrates a typical automotive application scheme. The resistor R_S limits the input current of the device and is therefore dimensioned considering the characteristics of the transients to be eliminated. Consequently :

$$R_S = \frac{V_{transient\ Peak}}{I_{IN\ MAX}}$$

The C_{IN} capacitors must be used only on analog inputs because they present a low impedance during the sampling period.

Figure 3 : Typical Application.



The minimum value for C_{IN} is determined by the accuracy required, the time taken to sample the input and the input impedance during that time, while the maximum value is determined by the required frequency response and the value of R_S.

Thus for a resistive input A/D connector where :

T_S = Sample time (Seconds)

R_D = Device input resistance (Ohms)

V_{IN} = Input voltage (Volts)

k = Required accuracy (%)

Q_1 = Charge on capacitor before sampling

Q_2 = Charge on capacitor after sampling

I_D = Device input current (Amps)

Thus :

$$Q_1 - Q_2 = \frac{k \cdot Q_1}{100}$$

but $Q_1 = C_{IN} V_{IN}$

and $Q_1 - Q_2 = I_D - T_S$

so that $I_D T_S = \dfrac{k \cdot C_{IN} - V_{IN}}{100}$

and $C_{IN}(\text{min}) = \dfrac{I_D \cdot T_S}{V_{IN} \cdot k}$ Farad

so $C_{IN}(\text{min}) = \dfrac{100 \cdot T_S}{k \cdot R_D}$ Farad

The calculation for a sample and hold type convertor is even simpler :

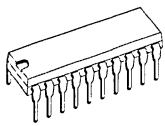
k = Required accuracy (%)

C_H = Hold capacitor (Farad)

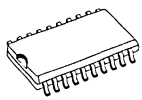
$$C_{IN}(\text{min}) = \frac{100 \cdot C_H}{k} \text{ Farad}$$

OCTAL GROUND CONTACT MONITORING CIRCUIT

- OPERATING DC SUPPLY VOLTAGE RANGE 5V TO 25V
- SUPPLY OVERVOLTAGE PULSE UP TO 40V
- VERY LOW STANDBY QUIESCENT CURRENT 0.2mA
- INTERNAL CLAMPING DIODES AT CONTACT INPUTS TO V_S AND GND
- INPUT PULSE CURRENT CAPABILITY UP TO + 50mA ; – 75mA
- NOMINAL CONTACT CURRENT OF 10mA DEFINED BY EXTERNAL CONTACT SERIES RESISTORS R_{IN1-8}
- CONTACT STATUS MONITORING BY COMPARING THE RESISTANCE AT CONTACT SENSE INPUTS WITH THE INTERNAL REFERENCE RESISTOR VALUE
- HIGH IMMUNITY DUE TO RESISTANCE COMPARISON WITH HYSTERESIS



DIP-20



SO-20L

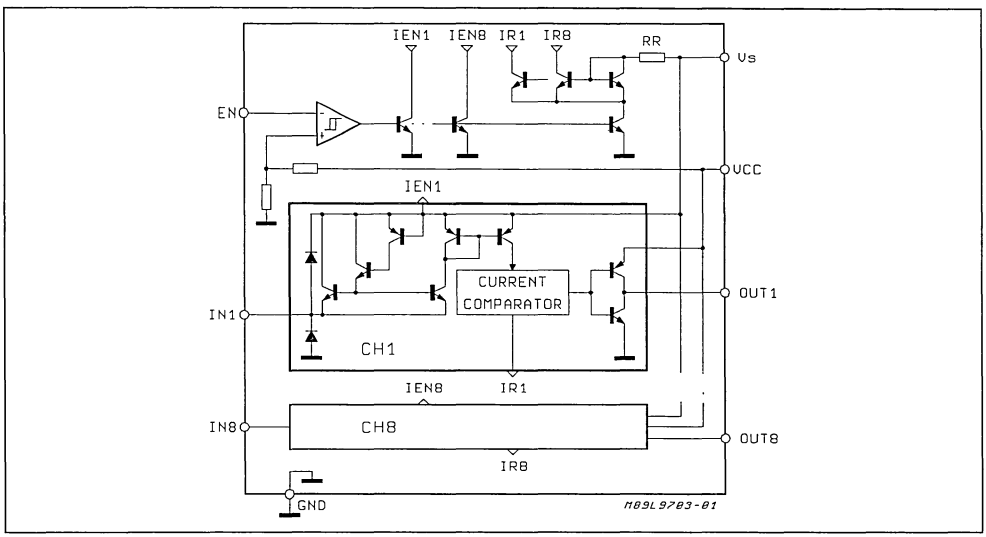
ORDERING NUMBERS : L9703 (DIP-20)
L9703D (SO-20L)

DESCRIPTION

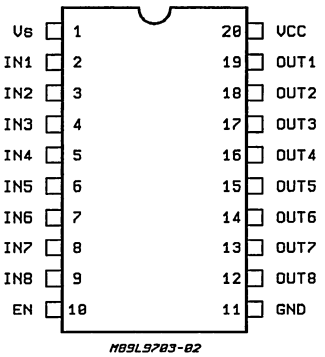
The L9703 is a bipolar monolithic integrated circuit for monitoring the status of up to eight contacts connected to GND.

It contains eight contact sense inputs and eight microcomputer compatible three-state outputs.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Transient Supply Voltage (t ≤ 1s)	+40	V
V_{CC}	Logic Supply Voltage	7	V
$I_{IN\,DC}$	Input DC Current	±40	mA
I_{INP}	Input DC Pulse (test pulse specification: 0 < tP < 2ms, f ≤ 0.2Hz, n = 25000)	50 -75	mA mA
I_O	Output Current	Internally Limited	
V_{EN}	Enable Input Voltage	V_{CC} +0.3 -0.3	V V
P_O	Power Dissipation at T_{amb} = 80°C DIP20 SO20	 875 420	 mW mW
T_{stg}, T_J	Storage and Junction Temperature Range	-55 to 150	°C

THERMAL DATA

Symbol	Parameter		DIP20	SO20	Unit
$R_{th\,j\text{-}amb}$	Thermal Resistance Junction to Ambient	MAX.	80	165	°C/W

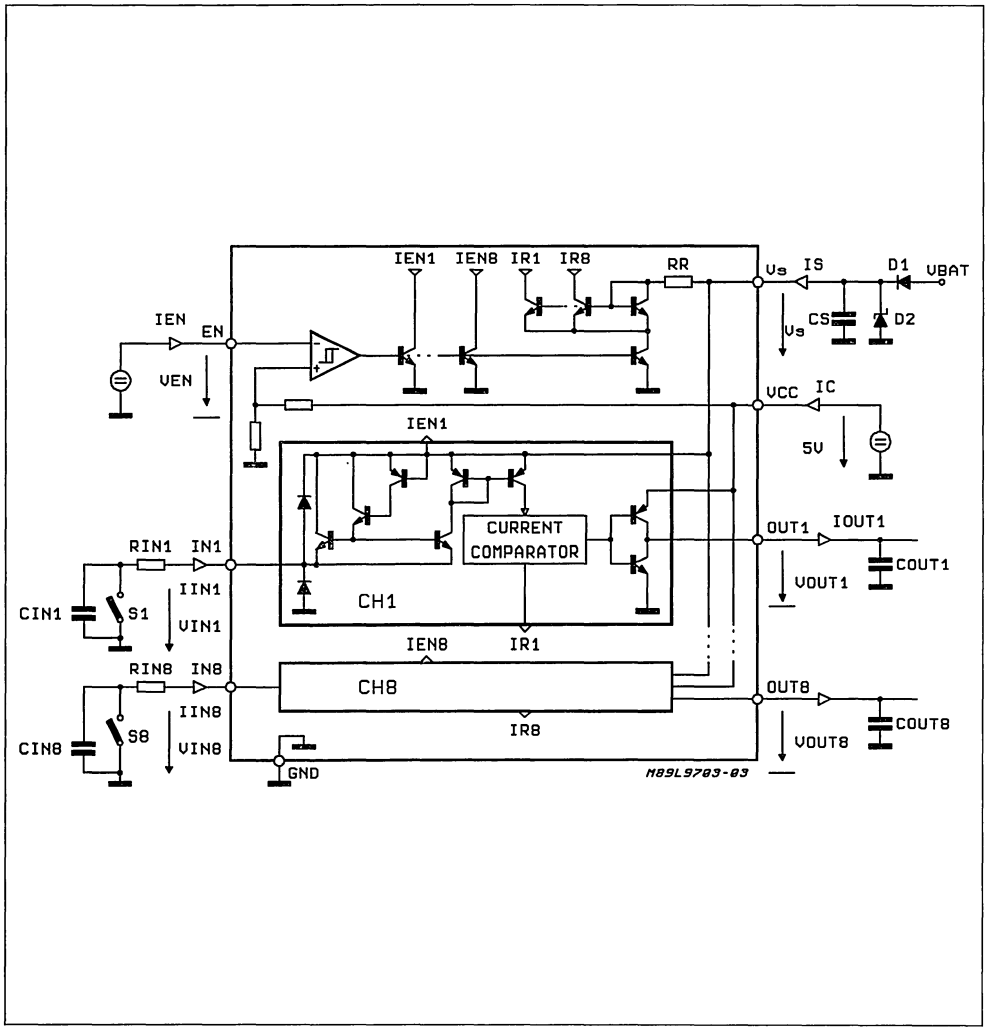
ELECTRICAL CHARACTERISTICS ($5V \le V_S \le 25V$; $-40°C \le T_j \le 125°C$; $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified; the currents flowing in the arrow direction are assumed positive as marked in the application circuit diagram, fig. 1).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ENL}	Enable Input Voltage LOW (device activated)				0.8	V
V_{ENH}	Enable Input Voltage HIGH		2.4			V
$V_{EN\,hyst}$	Enable Input Hysteresis		200	420	800	mV
I_{EN}	Enable Input Current	$2.4V < V_{EN} < V_{CC}$			5	µA
		$0V < V_{EN} < 0.8V$	-5	-1		µA
V_{OUTH}	Output Voltage HIGH	$0 < I_{OUT} < 100µA$	4.0	V_{CC} -0.1	V_{CC}	V
V_{OUTL}	Output Voltage LOW	I_{OUT} = -1mA	0.05	0.2	0.4	V
$I_{OUT\,TS}$	Output TRISTATE Current	$0 < V_{OUT} < V_{CC}$			0.5	µA
V_{IN}	Input Voltage (device active)	EN = LOW R_{IN} = 1kΩ	V_S - 2	V_S - 1.5	V_S - 0.4	V
V_{IN}	Input Clamped Voltage (device disabled)	EN = HIGH I_{IN} = 30mA I_{IN} = -30mA	V_S + 0.3 -2	V_S + 1 -1	V_S + 2 -0.3	V V
I_{OUT}	Output Current	OUT = HIGH V_{OUT} = 0			2	mA
I_{OUT}	Output Current	OUT = LOW VOUT = 5.5V			-20	mA
R_{IL}	Input Resistor (note 1) LOW Threshold	$5V < V_S < 16V$ $\lvert \Delta V_{GND} \rvert \le 0.1V_S$	1.8	4		KΩ
R_{IH}	Input Resistor (note 1) HIGH Threshold			5.3	20	KΩ
$\frac{R_{IL}}{R_{IH}}$	Input Resistor Threshold Ratio (note1)		0.65	0.75	0.85	
I_{QC}	Quiescent Current	EN = HIGH ($t_{ENH} \ge 80µs$) $5V < V_S < 16V$ $-40°C \le T_j \le 100°C$		0.12	0.16	mA
I_{QS}	Quiescent Current	All Inputs Open			0.04	mA
		All Inputs Closed			0.24	mA
I_{QC} I_{QS}	Quiescent Current	EN = LOW			6 6	mA mA
t_{do}	Delay Time/Output (EN LOW to output data ready)	$C_{OUT} \le 50pF$			15 $+3R_{IN}C_{IN}$	µs
t_{dTS}	Delay Time/Tristate (EN HIGH to output TRISTATE)	$C_{OUT} \le 50pF$			10	µs

Note · 1. The input resistor threshold value is the resistor value from the IN-pin to ground at which the corresponding output changes its status (see fig 3).

APPLICATION CIRCUIT

Figure 1 : Typical Application Diagram for the L9703 Circuit. The current flowing in the arrow direction is assumed positive. The external capacitors C_{IN} and C_{OUT} represent the total wiring capacitance at the corresponding pins.



FUNCTIONAL DESCRIPTION

The L9703 circuit monitors the status of the contacts connected to ground and through this series external resistors R_{IN} to the contact sense input pins. The contacts equivalent circuit is supposed to be as shown in fig. 2.

The L9703 circuit compares the input current with the current through the internal reference resistor. The device is designed to work with an external input series resistor of $R_{IN1\text{-}8} = 1k\Omega$. With this input resistor the contact current, when the contact is closed and the device activated (EN = LOW) is

$$I_{IN} = \frac{V_S - 2V}{1k\Omega} \quad (1)$$

For this calculation the limit value of the V_S to IN saturation voltage of 2V was considered so that the lowest limit value of I_{IN} is calculated in (1).

The function of the circuit can be demonstrated with the transfer characteristics, showing the output status as a function of the input resistor R_I, shown in figure 3. The input resistor is a sum of the R_{IN} and the contact resistance R_{CON} or R_{COFF}, for the closed contact :

$$R_I = R_{IN} + R_{CON}, \quad (2)$$

and for the open contact :

$$R_I = R_{IN} + R_{COFF}. \quad (3)$$

The output goes HIGH when the input resistance increases above 5.3kΩ (typical value) and goes LOW, when the input resistance decreases below 4kΩ (typical value). The limit values of $R_I = 1.8K\Omega$ for LOW and $R_I = 20k\Omega$ for HIGH implies that a contact with $R_{CON} = 100\Omega$ (at $I_{IN} = 10mA$) will be recognized as ON = LOW and a contact with $R_{COFF} = 19k\Omega$ will be recognized as OFF = HIGH. These limits are valid within the supply voltage range $6V \leq VS \leq 16V$ and the ground potential difference of $|\Delta VGND| = 0{,}1V$.

The internal clamping diodes at the contact monitoring inputs, together with the external contacts series resistors R_{IN}, allows the device to withstand transients at the contact connection. The contact series resistor R_{IN} limits the input current at the transient.

The dynamic behaviour of the circuit is defined by the times t_{do} and t_{dTs}. When the contact is open, the input capacitor C_{IN} must be charged through the resistor R_{IN}. In this case the total delay time may also be influenced by the time constant $R_{IN}C_{IN}$.

The delay time t_{dTs}, when disabling the device, is defined only by the internal circuitry. In both cases, an external output capacitance less than 50pF is assumed, the internal output capacitances of the three-state buffers are less than 5pF.

Figure 2 : The Contact Sense Input Connection with the Contact Equivalent Circuit.

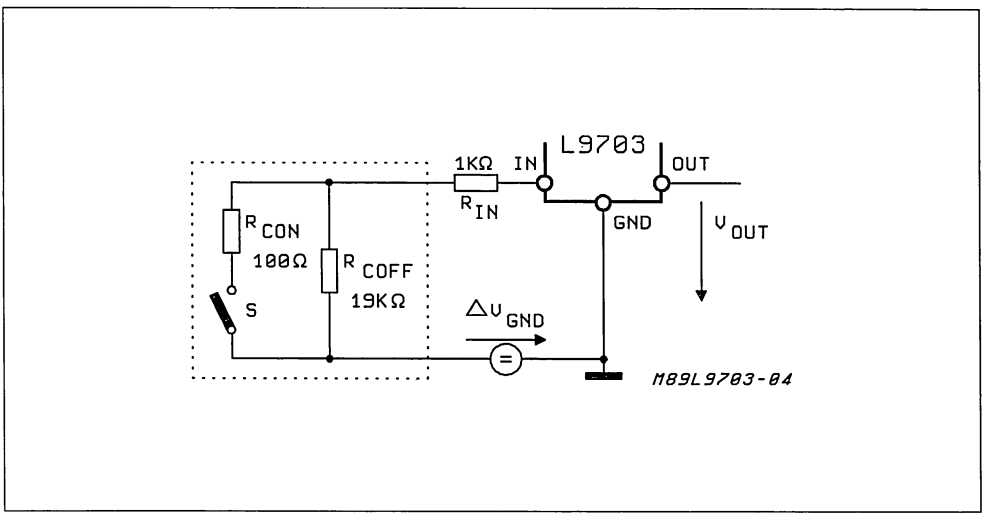
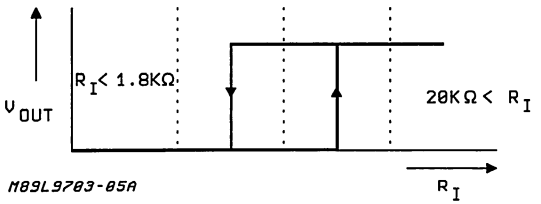
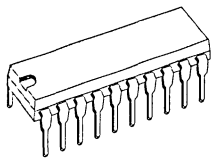


Figure 3 : The Output Voltage as a Function of the Input Resistance at the Corresponding Contact Sense Input.

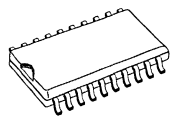


OCTAL SUPPLY CONTACT MONITORING CIRCUIT

- OPERATING DC SUPPLY VOLTAGE RANGE 5V TO 25V
- SUPPLY OVERVOLTAGE PULSE UP TO 40V
- VERY LOW STANDBY QUIESCENT CURRENT 0.2mA
- INTERNAL CLAMPING DIODES AT CONTACT INPUTS TO V_S AND GND
- INPUT PULSE CURRENT CAPABILITY UP TO + 50mA, – 75mA
- NOMINAL CONTACT CURRENTS OF 10mA DEFINED BY EXTERNAL CONTACT SERIES RESISTORS R_{IN1-8}
- CONTACT STATUS MONITORING BY COMPARING THE RESISTANCE AT CONTACT SENSE INPUTS WITH THE INTERNAL REFERENCE RESISTOR VALUE
- HIGH IMMUNITY DUE TO RESISTANCE COMPARISON WITH HYSTERESIS



DIP–20



SO–20L

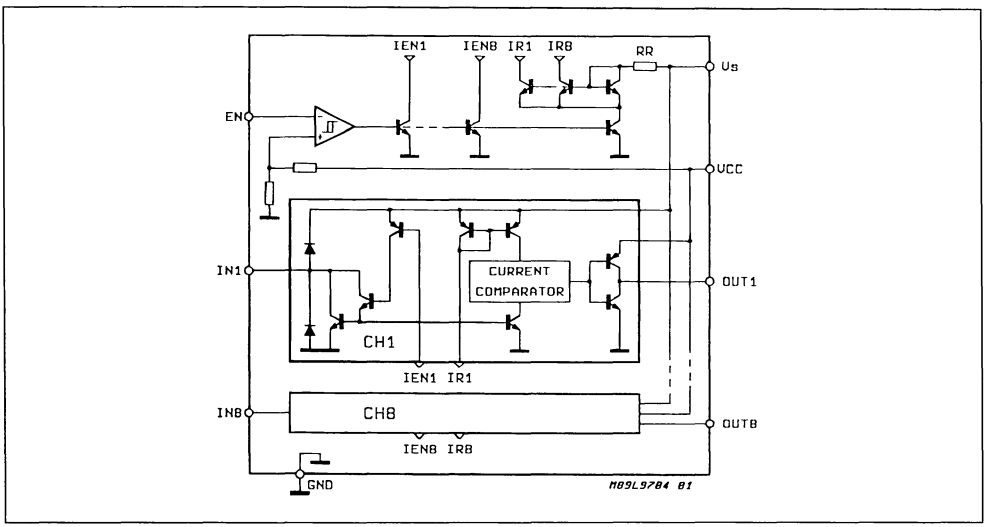
ORDERING NUMBERS: L9704 (DIP–20)
L9704D (SO–20L)

DESCRIPTION

The L9704 is a bipolar monolithic integrated circuit for monitoring the status of up to eight contacts connected to the power supply (battery).

It contains eight contact sense inputs and eight microcomputer compatible three-state outputs.

BLOCK DIAGRAM



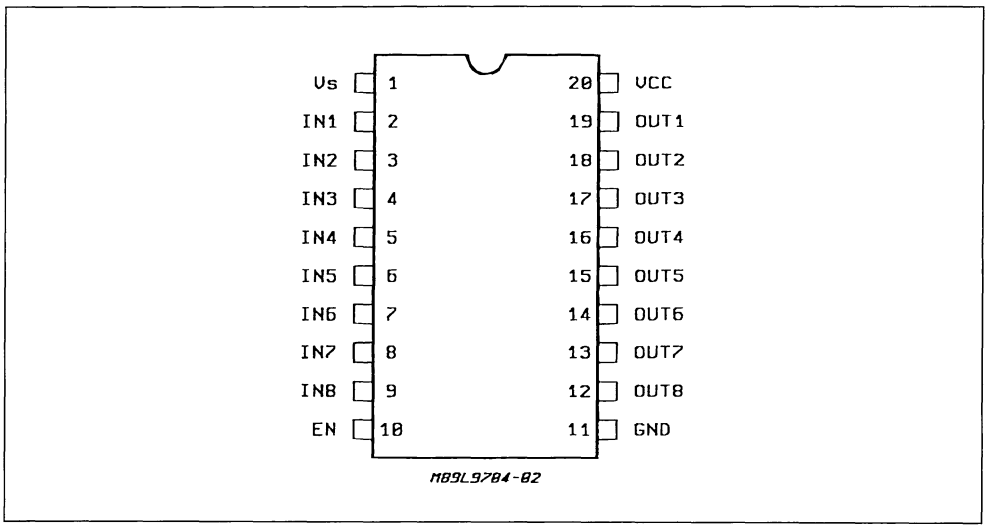
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Transient Supply Voltage ($t \leq 1s$)	+40	V
V_{CC}	Logic Supply Voltage	7	V
$I_{IN\ DC}$	Input DC Current	±40	mA
I_{INP}	Input DC Pulse (test pulse specification: $0 < tP < 2ms$, $f \leq 0.2Hz$, $n = 25000$)	50 -75	mA mA
I_O	Output Current	Internally Limited	
V_{EN}	Enable Input Voltage	V_{CC} +0.3 -0.3	V V
P_O	Power Dissipation at T_{amb} = 80°C DIP20 SO20	 875 420	 mW mW
T_{stg}, T_J	Storage and Junction Temperature Range	-55 to 150	°C

THERMAL DATA

Symbol	Parameter		DIP20	SO20	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	MAX.	80	165	°C/W

PIN CONNECTION (top view)



ELECTRICAL CHARACTERISTICS ($5V \leq V_S \leq 25V$; $-40°C \leq T_j \leq 125°C$; $4.75V \leq V_{CC} \leq 5.25V$ unless otherwise specified; the currents flowing in the arrow direction are assumed positive as marked in the application circuit diagram, fig. 1).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ENL}	Enable Input Voltage LOW (device activated)				0.8	V
V_{ENH}	Enable Input Voltage HIGH		2.4			V
$V_{EN\ hyst}$	Enable Input Hysteresis		200	300	800	mV
I_{EN}	Enable Input Current	$2.4V < V_{EN} < V_{CC}$			5	µA
		$0V < V_{EN} < 0.8V$	-5	-1		µA
V_{OUTH}	Output Voltage HIGH	$0 < I_{OUT} < 100µA$	4.0	V_{CC} -0.1	V_{CC}	V
V_{OUTL}	Output Voltage LOW	I_{OUT} = -1mA	0.05	0.2	0.4	V
$I_{OUT\ TS}$	Output TRISTATE Current	$0 < V_{OUT} < V_{CC}$			0.5	µA
V_{IN}	Input Voltage (device active)	EN = LOW R_{IN} = 1kΩ	0.4	1.5	2	V
V_{IN}	Input Voltage During Clamping (device disabled)	EN = HIGH I_{IN} = 30mA I_{IN} = -30mA	V_S + 0.3 -2	V_S + 1 -1	V_S + 2 -0.3	V V
I_{OUT}	Output Current	OUT = HIGH V_{OUT} = 0			2	mA
I_{OUT}	Output Current	OUT = LOW VOUT = 5.5V			-20	mA
R_{IL}	Input Resistor (note 1) LOW Threshold	$5V < V_S < 16V$ $\lvert \Delta V_{GND} \rvert \leq 0.1V_S$	1.1	4.8		KΩ
R_{IH} R_{IL}	Input Resistor (note 1) HIGH Threshold			6.5	29	KΩ
R_{IH}	Input Resistor Threshold Ratio (note1)		0.65	0.75	0.85	
I_{QC}	Quiescent Current	EN = HIGH ($t_{ENH} \geq 80µs$) $5V < V_S < 16V$ $-40°C \leq T_j \leq 100°C$		0.12	0 16	mA
I_{QS}		All Inputs Open			0.04	mA
SI_{IN} 2)	Input Leakage Current	All Inputs Closed $V_{BAT} \leq V_{D1}$			0.24	mA
I_{QC} I_{QS}	Quiescent Current	EN = LOW			13 2	mA mA
t_{do}	Delay Time/Output (EN LOW to output data ready)	$C_{OUT} \leq 50pF$			15 $+3R_{IN}C_{IN}$	µs
t_{dTS}	Delay Time/Tristate (EN HIGH to output TRISTATE)	$C_{OUT} \leq 50pF$			10	µs

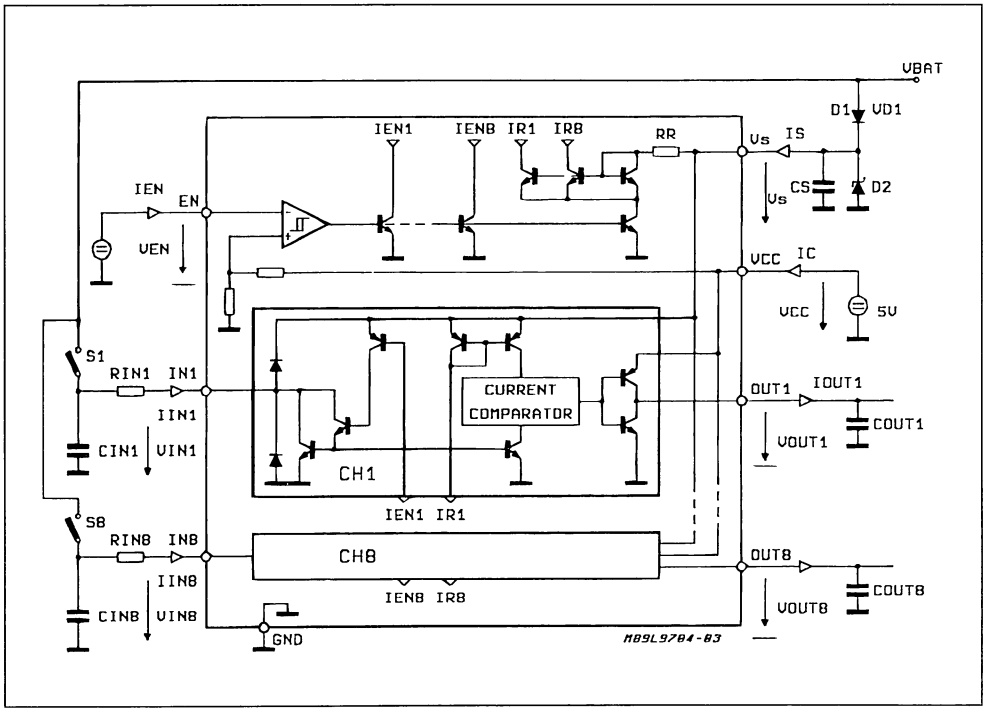
Notes :

1. The input resistor threshold value is a resistor value from the IN–pin to battery at which the corresponding output changes its status (see fig. 3)

2. SI_{IN} is the sum of the input currents $SI_{IN} = \sum_{i=1}^{8} I_{IN1}$

APPLICATION CIRCUIT DIAGRAM

Figure 1 : Typical application diagram for the L9704 circuit. The current flowing in the arrow direction is assumed positive. The external capacitors C_{IN} and C_{OUT} represent the total wiring capacitance at the corresponding pins.



FUNCTIONAL DESCRIPTION

The L9704 circuit monitors the status of the contacts connected to battery and through the series external resistors R_{IN} to the contact sense input pins. The contacts equivalent circuit is supposed to be as shown in fig. 2.

The L9704 circuit compares the input current with the current through the internal reference resistor. The device is designed to work with an external input series resistor of $R_{IN1\text{-}8} = 1k\Omega$. With this input resistor the contact current, when the contact is closed and the device activated (EN = LOW) is

$$I_{IN} = \frac{V_{BAT} + \Delta V_{BAT} - 2V}{1K\Omega} \qquad (1)$$

For this calculation the limit value of the V_{IN} (saturation voltage of 2V) was considered so that the lowest limit value of I_{IN} is calculated in (1).

The function of the circuit can be demonstrated with the transfer characteristics, showing the output status as a function of the input resistor R_I, shown in figure 3. The input resistor is a sum of the R_{IN} and the contact resistance R_{CON} or R_{COFF}, for the closed contact :

$$R_I = R_{IN} + R_{CON}, \qquad (2)$$

and for the open contact :

$$R_I = R_{IN} + R_{COFF}. \qquad (3)$$

The output goes HIGH when the input resistance increases above 6.5kΩ (typical value) and goes LOW, when the input resistance decreases below 4.8KΩ (typical value). The limit values of R_I = 1.1KΩ for LOW and R_I = 29kΩ for HIGH implies that a contact with $R_{CON} = 100\Omega$ (at I_{IN} = 10mA) will be recognized as ON = LOW and a contact with R_{COFF} = 28kΩ will be recognized as OFF = HIGH. These limits are valid within the supply voltage range $5V \le V_S \le 16V$, the battery voltage potential difference of $|\Delta VBAT| \le 0.1V_{BAT}$ and the variation of the reverse battery protection diode D1 voltage from 0.5V to 1V.

The internal clamping diodes at the contact monitoring inputs, together with the external contact series resistors R_{IN}, allows the device to withstand transients at the contact connection. The contact series resistor R_{IN} limits the input current at the transient.

The dynamic behaviour of the circuit is defined by the times t_{do} and t_{dTS}. When the contact becomes open, the input capacitor C_{IN} must be charged through the resistor R_{IN}. In this case the total delay time may also be influenced by the time constant R_{IN} C_{IN}. The delay time t_{dTS}, when disabling the device is defined only by the internal circuitry. In both cases, an external output capacitance less than 50pF is assumed, the internal output capacitances of the three-state buffers are less than 5pF.

Figure 2 : The Contact Sense Input Connection with the Contact Equivalent Circuit.

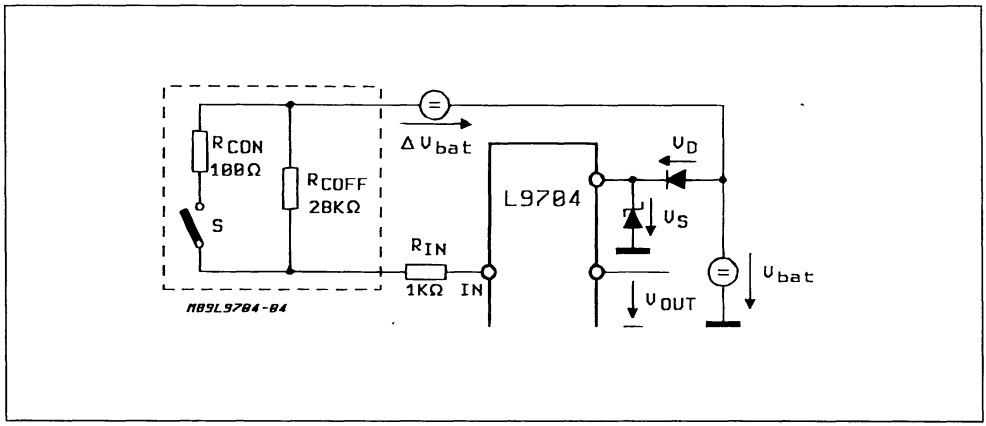
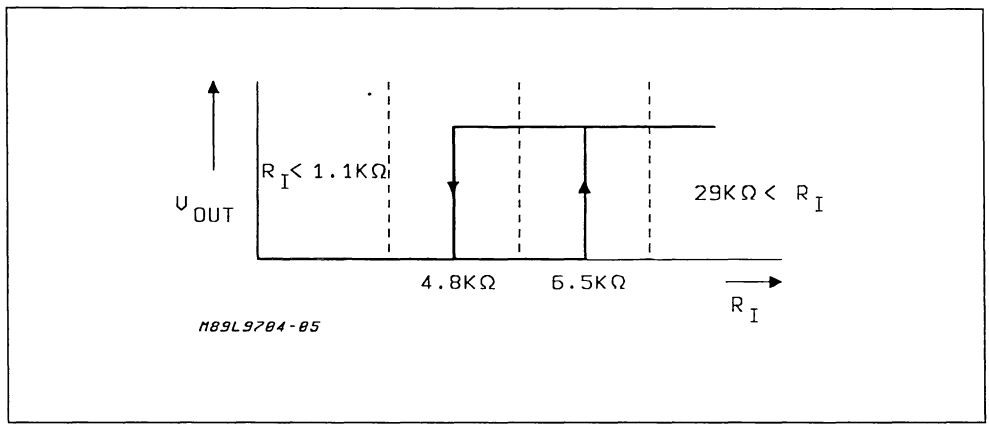


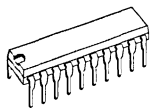
Figure 3 : The Output Voltage as a Function of the Input Resistance at the Corresponding Contact Sense Input.



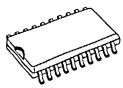
DOUBLE QUAD CONTACT INTERFACE CIRCUIT

ADVANCE DATA.

- OPERATING DC SUPPLY VOLTAGE RANGE 5V TO 25V
- SUPPLY OVERVOLTAGE PULSE UP TO 40V
- VERY LOW STAND-BY QUIESCENT CURRENT, MAX 50µA
- INTERNAL CLAMPING DIODES AT CONTACT INPUTS TO Vs AND gnd WITH PULSE CURRENT CAPABILITY UP TO +50mA, -75mA
- CHIP ENABLE FUNCTION AND TRISTATE OUTPUTS FOR PARALLEL BUS CONNECTION
- NOMINAL CONTACT CURRENTS OF 10mA DEFINED WITH EXTERNAL CONTACT SERIES RESISTORS R_{IN1-8}
- CONTACT STATUS MONITORING BY MEANS OF COMPARING THE RESISTANCE AT CONTACT SENSE INPUTS WITH THE INTERNAL REFERENCE RESISTOR VALUE
- RESISTANCE COMPARING WITH HYSTERESIS FOR HIGH NOISE IMMUNITY AND IMMUNITY TO GROUND AND BATTERY POTENTIAL DIFFERENCES



DIP 20



SO20L

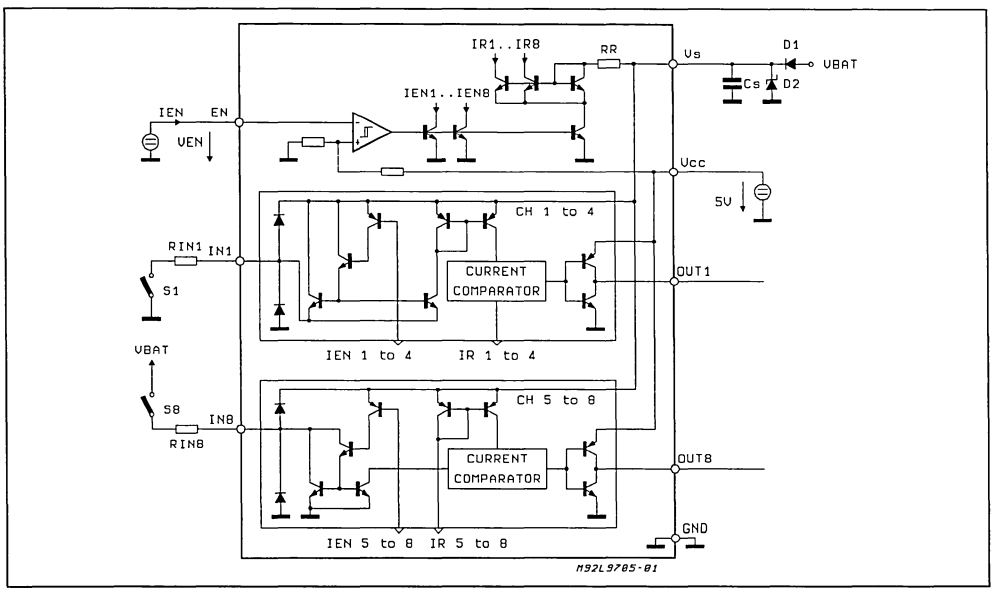
ORDERING NUMBERS : L9705

DESCRIPTION

The L9705 is a bipolar monolithic integrated circuit for monitoring the status of up to four contacts connected to GND and up to four contacts connected to the battery. The contact sense input supply the contact current and perform the contact resistance comparison function.

At the output the contact status is translated into a logical LOW level (contact closed) or logical HIGh level (contact open).

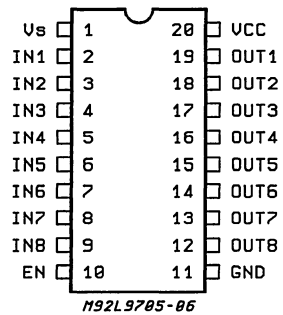
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{SDC}	DC Supply Voltage	+26	V
V_{SP}	Peak Transient Supply Voltage ($t \leq 400ms$)	+40	V
V_{CC}	Logic Supply Voltage	7	V
I_{INDC}	Input DC Current	±40	mA
I_{INP}	Input Pulse (t_p = 0 to 2ms; $f \leq 0.2Hz$; n = 25000)	-75 to 50	mA
I_{OUT}	Output Current (VO = 0 to 5.5V)	internally limited	
V_{EN}	Enable Input Voltage	V_{CC} +0.3V;-0.3V	V
P_{tot}	Total Power Dissipation (T_{amb} = 80°C) DIP 20 SO 20	875 420	mW mW
T_j	Junction Temperature Range	max150	°C

PIN CONNECTION (top view)



THERMAL DATA

Symbol	Description	DIP20	SO20L	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	80		°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient		165	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 5 to 25V, V_{CC} = 4.75 to 5.25V, V_{bat} -0.5V ≤ V_S ≤ V_{bat} -1V , Tj = –40 to 150°C unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{ENL}	Enable Input Voltage LOW (device activated)		-0.3		0.8	V
V_{ENH}	Enable Input Voltage HIGH		2.4		V_{CC}	V
V_{ENh}	Enable Input Threshold Hysteresis		200	420	800	mV
I_{EN}	Enable Input Current	2.4V < V_{EN} < V_{CC} 0V < V_{EN} < 0.8V	 -5	 -1	5	µA µA
V_{OUTH}	Output Voltage HIGH	0 < I_{OUT} < 100µA	4	V_{CC} - 0.1	V_{CC}	V
I_{OUT}	Output Current	OUT status = HIGH; V_{OUT} = 0		0.5	2	mA
V_{OUTL}	Output Voltage LOW	I_{OUT} = -1mA	0.05	0.2	0.4	V
I_{OUT}	Output Current	OUT status = LOW; V_{OUT} = 5.5V		-5	-20	mA
$I_{OUT\ TS}$	Output Tristate Current	0 < VOUT < V_{CC}			0.5	µA
$V_{IN\ 1,4}$	Input Voltage (device active)	EN = LOW; R_{IN} = 1KΩ	V_S - 2	V_S - 1.5	V_S - 0.4	V
$V_{IN\ 5,8}$	Input Voltage (device active)	EN = LOW; R_{IN} = 1KΩ	0.4	1.5	2	V
V_{IN}	Input VoltageDuring Clamp (device disabled)	EN = HIGH; I_{IN} = 30mA I_{IN} = -30mA	V_S +0.3 -2	V_S +1 -1	V_S +2 -0.3	V V
$R_{IL\ 1,4}$	Input Resistor LOW Threshold (note 1)	5V < V_S <16V; $\lvert\Delta V_{GND}\rvert \le 0.1V_S$ $\lvert\Delta V_{BAT}\rvert \le 0.1V_{BAT}$	1.8	4		KΩ
$R_{IL\ 5,8}$	Input Resistor LOW Threshold (note 1)	5V < V_S <16V; $\lvert\Delta V_{GND}\rvert \le 0.1V_S$ $\lvert\Delta V_{BAT}\rvert \le 0.1V_{BAT}$	1.8	4.8		KΩ
$R_{IH\ 1,4}$	Input Resistor HIGH Threshold (note 1)	5V < V_S < 16V; $\lvert\Delta V_{GND}\rvert \le 0.1V_S$ $\lvert\Delta V_{BAT}\rvert \le 0.1V_{BAT}$		5.3	20	KΩ
$R_{IH\ 5,8}$	Input Resistor HIGH Threshold (note 1)	5V < V_S <16V; $\lvert\Delta V_{GND}\rvert \le 0.1V_S$ $\lvert\Delta V_{BAT}\rvert \le 0.1V_{BAT}$		6.5	29	KΩ
R_{IL}	Input Resistor Threshold Ratio (note 1)	5V < V_S <16V; $\lvert\Delta V_{GND}\rvert \le 0.1V_S$ $\lvert\Delta V_{BAT}\rvert \le 0.1V_{BAT}$	0.65	0.75	0.85	
R_{IH}	Input Resistor Threshold Ratio (note 1)	5V < V_S <16V; $\lvert\Delta V_{GND}\rvert \le 0.1V_S$ $\lvert\Delta V_{BAT}\rvert \le 0.1V_{BAT}$	0.65	0.75	0.85	
I_{QC}	Quiescent Current	EN = HIGH (t_{ENH} ≥20µs) V_S = 5 to 16V; T_j = -40 to 85°C		20	40	µA
I_{QS}	Quiescent Current	all contact open			10	µA
I_{QS}	Quiescent Current	all contact closed			35	µA
ΣI_{IN} (2)	Quiescent Current	$\lvert\Delta V_{BAT}\rvert \le 0.1V_{BAT}$			25	µA
I_{QC}	Quiescent Current	EN = LOW			5	mA
I_{QS}	Quiescent Current	EN = LOW			. . 8	mA
t_{do}	Delay Time/Output (EN LOW to Output Data Ready) (note 3)	C_{OUT} ≤ 50pF			15+ $3R_{IN}$*C_{IN}	µs
t_{dTS}	Delay Time/Tristate (EN HIGH to Output Tristate) (note 3)	C_{OUT} ≤ 50pF			10	µs
t_{dIO}	Delay Time Input-Output (note 3)	EN = LOW; C_{OUT} = 50pF			6	ms

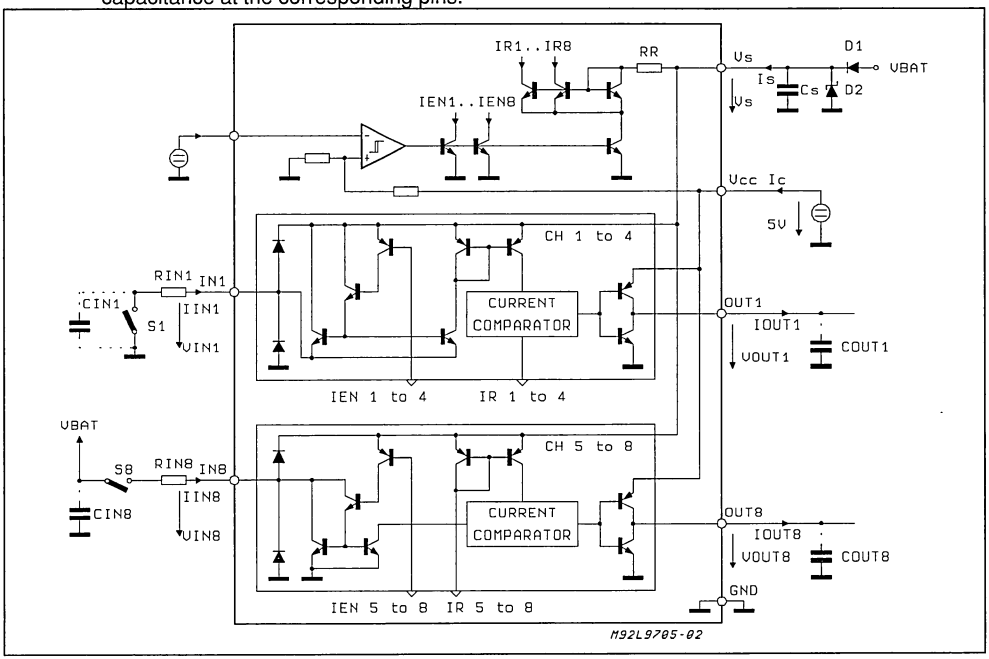
NOTES:

1) The input resistor threshold value is a resistor value from the IN-pin to ground at which the corresponding output changes its status (fig 4)

2) ΣI_{IN} is the sum of the IN5 to IN8 input currents

3) The delay times are defined from the crossing point of 50% initiating signal amplitude to the crossing point of 50% output signal amplitude

Figure 1: Typical application diagram for the L9705 circuit. The current flowing in the arrow direction is assumed positive. The external capacitors C_{IN} and C_{OUT} represent the total wiring capacitance at the corresponding pins.



FUNCTIONAL DESCRIPTION

The L9705 circuit monitors the status of the contacts which are connected through the series external resistors R_{IN} to the contact sense input pins. The contacts equivalent circuit is supposed to be as shown in fig.2 for GND connected contacts (IN 1 to 4) and as shown in fig. 3 for V_{BAT} connected contacts (IN 5 to 8).

Figure 2: The contact sense input connection with the contact equivalent circuit for GND connected contacts.

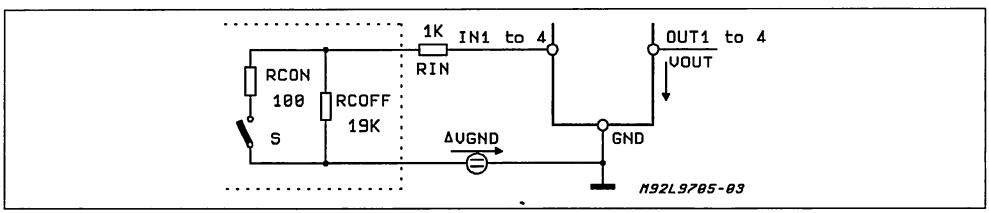
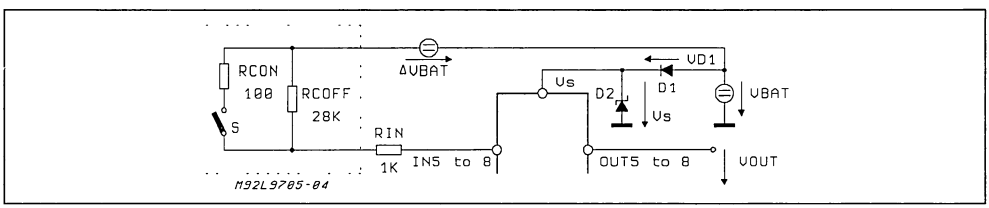


Figure 3: The contact sense input connection with the contact equivalent circuit for V_{BAT} connected contacts.



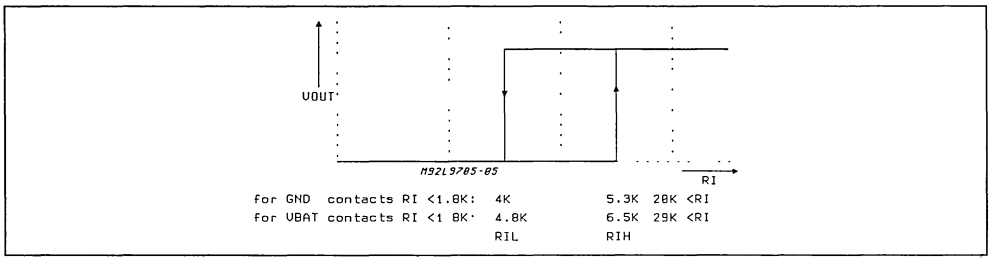
The L9705 circuit compares the input current with the current through the internal reference resistor. The device is designed to work with an external input series resistor of R_{IN1-8} = 1KΩ. With this input resistor the contact current, when the contact is closed and the device activated (EN =LOW) is:

$$I_{IN} = \frac{V_S - 2V}{1K\Omega}, \text{for GND contacts,} \quad (1)$$

$$I_{IN} = \frac{V_{BAT} + \Delta V_{BAT} - 2V}{1K\Omega}, \text{ for } V_{BAT} \text{ contacts,} \quad (2)$$

For this calculation the limit value of the V_S to V_{IN} and V_{IN} saturation voltage of 2V was considered so that the lowest limit value of I_{IN} is calculated in (1) and (2)

Figure 4: The output voltage as a function of the input resistance at the corresponding sense input.



The function of the circuit can be demonstrated with the transfer characteristics, showing the output status as a function of the input resistor R_I, shown in figure 4. The input resistor is a sum of the R_{IN} and the contact resistance R_{CON} or R_{COFF}, for the closed contact:

$R_I = R_{IN} + R_{CON}$, (3)

and for the open contact:

$R_I = R_{IN} + R_{COFF}$, (4)

The output goes HIGH when the input resistance increases above 5.3KΩ (GND contacts) or 6.5KΩ (V_{BAT} contacts) and goes LOW, when the input resistance decreases below 4KΩ (GND contacts) or 4.8KΩ (V_{BAT} contacts); these values are typical values for the switching thresholds. The limit values of R_I = 1.8KΩ (GND contacts) and R_I = 1.8KΩ (V_{BAT} contacts) for LOW and R_I = 20KΩ (GND contacts) and 29KΩ (V_{BAT} contacts) for HIGH implies that a contact with R_{CON} = 100Ω (at I_{IN} = 10mA) will be recognized as ON = LOW and a contact with R_{COFF} = 19KΩ (GND contacts) or 28KΩ (V_{BAT} contact) will be recognized as OFF = HIGH.

These limits are valid within the supply voltage range 6V ≤ V_S ≤ 16V, the ground potential difference of ΔV_{GND} = 0.1V_S, the battery voltage potential difference of ΔV_{BAT} ≤ 0.1V_{BAT} and the variation of the reverse battery protection diode D1 voltage from 0.5V to 1V.

The internal clamping diodes at the contact monitoring inputs together with the external contacts series resistors R_{IN} allows to withstand the transients at the contact connection.The contact series resistor R_{IN} limits the input current at the transient.

The dynamic behaviour of the circuit is defined with the times t_{do} and t_{dTS}. When the contact is open, the input capacitor C_{IN} must be charged through the resistor R_{IN}. In this case the total delay time t_{do} may be influenced also with the time constant $R_{IN}C_{IN}$.

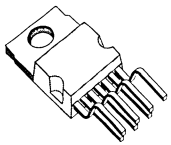
The delay time t_{dTS}, when disabling the device, is defined only with the internal circuitry. In both cases, output external capacitance less than 50pF is assumed, the internal output capacitance of the tristate buffers are less than 5pF.

HIGH SIDE DRIVER CIRCUIT

ADVANCE DATA

- OPERATING SUPPLY VOLTAGE RANGE 6 TO 45V
- 5A SHORT CIRCUIT CURRENT
- R_{ON} LESS THAN 400mΩ
- µP COMPATIBLE INPUT WITH THRESHOLD HYSTERESIS
- DC AND PWM OPERATION
- HIGH PERFORMANCE DIAGNOSTIC FUNCTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTIONS
- GROUNDED CASE
- ENABLE INPUT FOR STANDBY MODE

MULTIPOWER BCD TECHNOLOGY



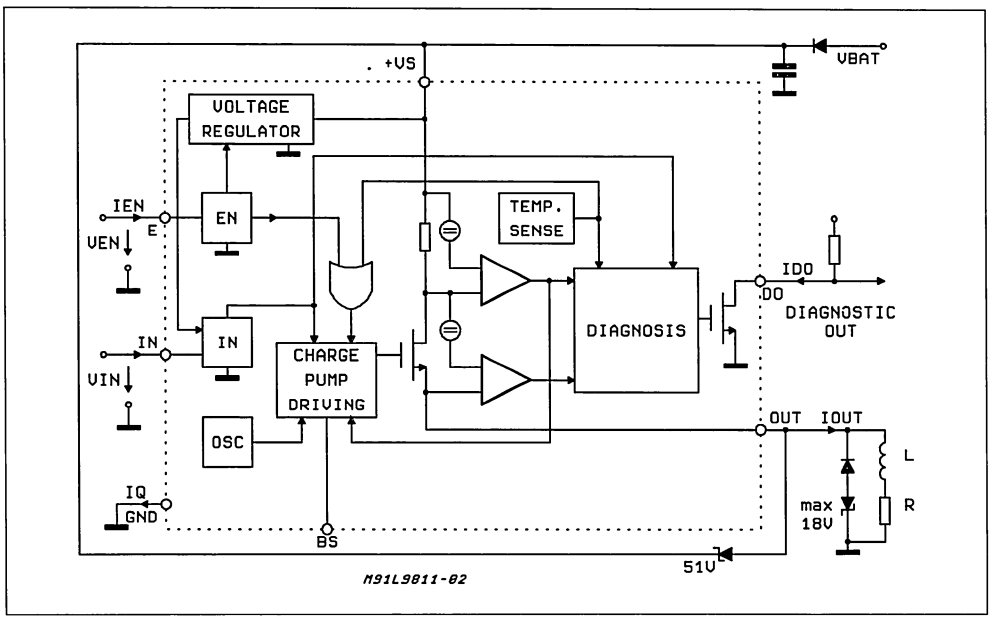
Heptawatt

ORDERING NUMBER: L9811

DESCRIPTION

The L9811 is a monolithic integrated circuit realized in Multipower BCD Technology. It is an intelligent high side driver designed especially for inductive or resistive loads. It features all functions necessary for automotive enviroment including high performance diagnostic.

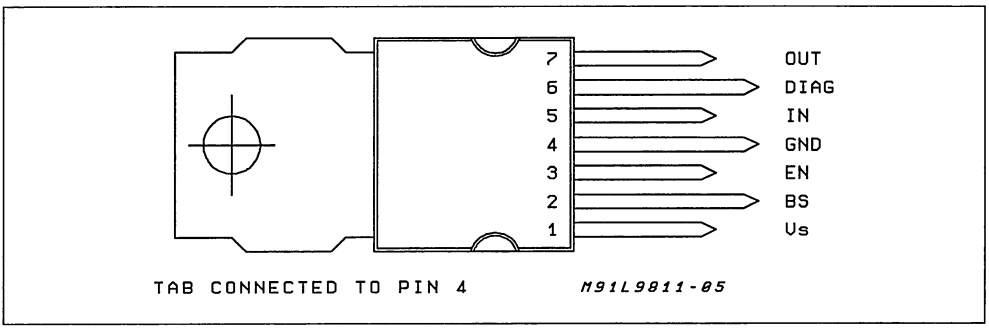
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{SDC}	Dc Supply Voltage	-0.3 to 45	V
V_S - V_O	Supply to Output Voltage	60	V
V_I, V_E	Input and Enable Input Voltage	-0.2 to 7	V
V_{BS}	Boostrap Voltage	60	V
V_O	Output Voltage	-18 to 45	V
I_O	Output Current	Internally Limited	V
V_{DF}	Diagnostic Output Voltage	-0.2 to 32	V
I_{DF}	Diagnostic Output Current	10	mA
T_{JSD}	Thermal Shutdown Threshold	min 150	°C
T_{JSDH}	Thermal shutdown Hysteresis	max 35	°C

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	max 1.5	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max 60	°C/W

DIAGNOSTIC DECISION TABLE

STATE	ENABLE	INPUT	OUTPUT		T_D	FUNCTION	DIAGNOSTIC
			V_O	I_O			
OFF	H	H	L	X	<T_{JSD}	NORMAL "OFF"	H
	H	H	L	X	>T_{JSD} *	THERMAL OVERLOAD "OFF"	L
	H	H	>V_{ODTH} *	X	<T_{JSD}	OUTPUT FAIL/"OFF"	L
ON	H	L	H	>I_{OL}	<TJSD	NORMAL "ON"	L
	H	L	X	X	>T_{JSD} *	THERMAL OVERLOAD "ON"	H
	H	L	<V_S -V_{OEXD} *	>I_{SC}	X	EXTERNAL DROP DUE TO OVERCURRENT	H
	H	L	X	>I_{OL}*	X	OPEN LOAD "ON"	H
	H	L	<V_S -V_{OEXD} *	X	<T_{JSD}	EXCESSIVE DROP "ON"	H
ST-BY	L	X	X	X	X	STANDBY MODE	H

(*)Parameter causing Diagnostic = LOW

ELECTRICAL CHARACTERISTICS (V_S = 6 to 45V (1); T_{amb} = -40 to 150°C; V_{EN} = HIGH; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{ON}	ON Resistance	V_I < 0.8V; T_{amb} < 125°C		200	400	mΩ
I_{SC}	Short Circuit Current	$V_{SDC} \leq$ 25V; V_{SPULSE} (Tp < 2ms)	2.5	5	7.5	A
I_{OL}	Open Load Detection Level	Device ON @ 25°C	30	100	160	mA
I_{OC} (2)	Output Current	V_O = -18V			100	mA
I_Q	OFF State Quiescent Current	V_I > 2V; V_S = 32V; V_I > 2V;		4.5 7.5	10 12	mA mA
I_Q	ON State Quiescent Current	V_I < 0.8V; V_S = 32V; V_I < 0.8V;		4.5 10	10 16	mA mA
V_{IL}	Input Low Level				0.8	V
V_{IH}	Input High Level		2			V
V_{ITH}	Input Threshold Hysteresis		50	100		mV
I_{IN}	Input Current	V_I = 0 to 5.5V			10	µA
I_{DFL}	Diagnostic Output Leakage Current	$T_{amb} \leq$ 125°C; V_D = 6 to 32V; Diagnostic output High			10	µA
V_{DFL}	Diagnostic Output Low	$I_{DF} \leq$ 2mA			0.4	V
V_{OEXD}	Excessive Dropout Voltage Detection Level		1	1.5	2	V
V_{ODTH}	Output Diagnostic Threshold	$V_I \geq$ 2V	4		6	V
t_{RD}	Diagnostic Delay Time				10	µs
I_{QSB}	Standby Mode Quiescent Current	V_{EN} < 0.8V; $T_{amb} \leq$ 125°C; V_S = 27V V_S = 13V			 400 200	 µA µA
V_{ENL}	Enable Level Low	Standby Mode			0.8	V
V_{ENH}	Enable Level High		2			V
V_{ENTH}	Enable Threshold Hysteresis		50	100		mV
I_{ENH}	Enable Input Current High	V_{EN} = 2 to 5.5V; V_{EN} < V_S -2 V			10	µA
I_{ENL}	Enable Input Current Low	V_{EN} = 0 to 0.8V;	-1		1	µA
t_{rON}	ON Rise Time (3)	with C_B: $V_S \leq$ 32V V_S > 8V V_S > 10V t_{OFF} > 0.3ms			 4 2 6	 µs µs µs
t_{fOFF}	OFF Fall Time	V_S = 8 to 32V			2	µs
t_{dON}	ON Delay Time	V_S = 8 to 32V		1	3	µs
t_{dOFF}	OFF Delay Time	V_S = 8 to 32V		1	3	µs
t_d	Diff. Delay Time t_{dON} - t_{dOFF}	VS = 8 to 32V			4	µs

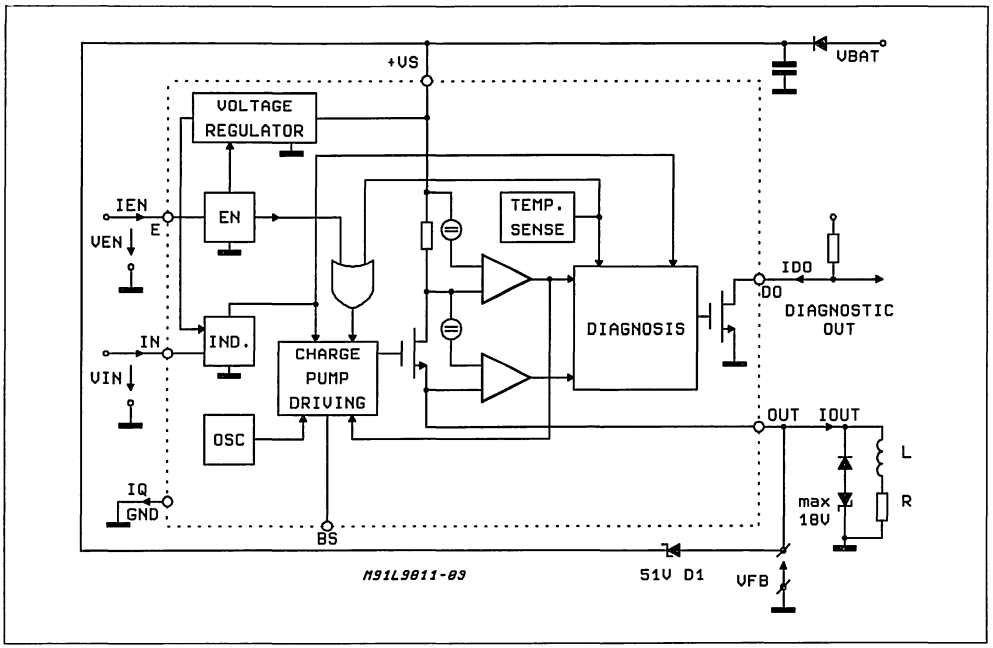
Notes:

1) For V_S < 6V the device can switch off.

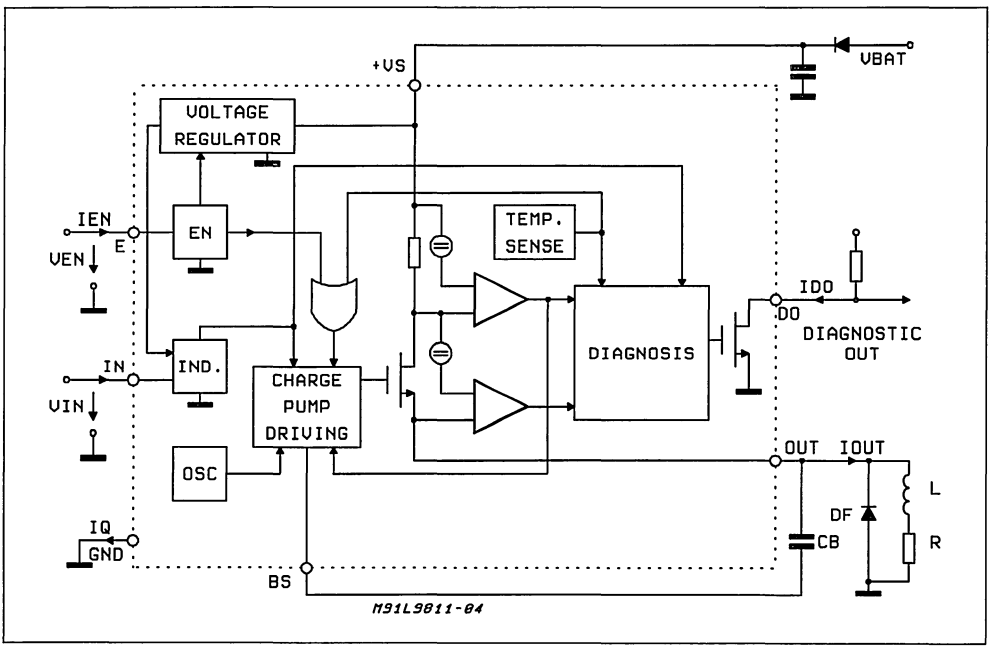
2) An external recirculation path must be assured in PWM operation to avoid excessive power dissipation

3) Measured with resistive load and I_{LOAD} = 1A from 10% to 90% of the output voltage amplitude with C_B = 33nF and after t_{OFF} < 10µs

APPLICATION DIAGRAM: DC Operation

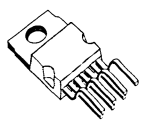


APPLICATION DIAGRAM: PWM Operation



HIGH SIDE DRIVER CIRCUIT

- OPERATING SUPPLY VOLTAGE RANGE 6 TO 45V
- TYPICAL OUTPUT CURRENT 2.7A
- R_{ON} LESS THAN 400mΩ
- µP COMPATIBLE INPUT WITH THRESHOLD HYSTERESIS
- DC AND PWM OPERATION
- HIGH PERFORMANCE DIAGNOSTIC FUNCTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTIONS
- GROUNDED CASE
- ENABLE INPUT FOR STANDBY MODE



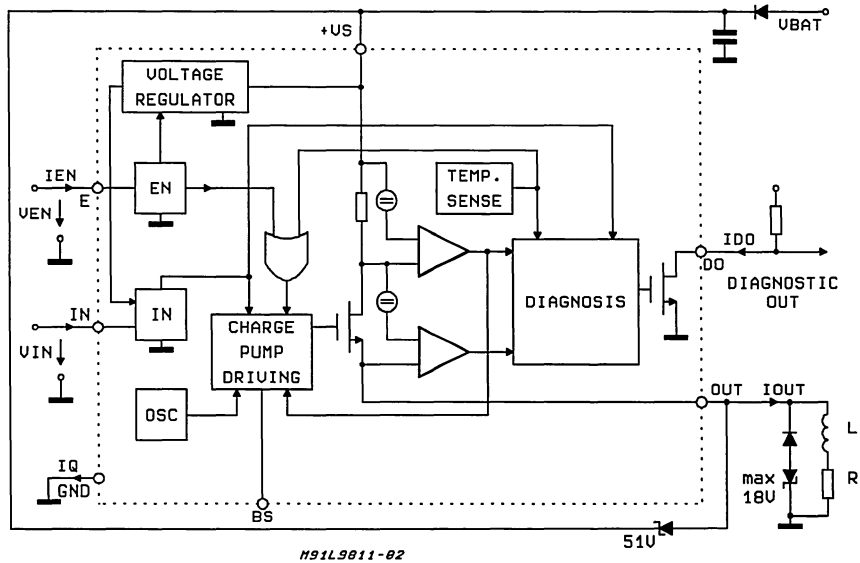
HEPTAWATT

ORDERING NUMBER: L9812R

DESCRIPTION

The L9812R is a monolithic integrated circuit realized in Multipower BCD technology. It is an intelligent high side driver designed expecially for inductive or resistive loads. It features all functions necessary for automotive environment including high performance diagnostic.

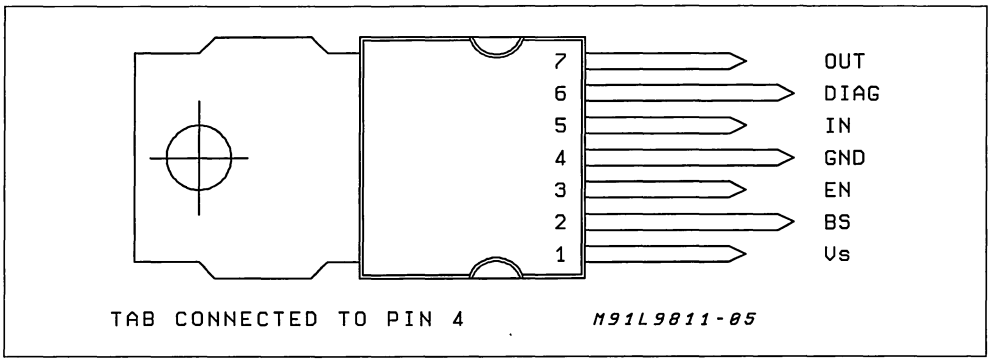
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{SDC}	DC Supply Voltage	-0.3 to 45	V
V_S - V_O	Supply to Output Voltage	60	V
V_I - V_E	Input and Enable Input Voltage	-0.2 to 7	V
V_{BS}	Bootstrap Voltage	60	V
V_O	Output Voltage	-18 to 45	V
I_O	Output Current	internally limited	V
V_{DF}	Diagnostic Output Voltage	-0.2 to 32	V
I_{DF}	Diagnostic Output Current	10	mA
T_{JSD}	Thermal Shutdown Threshold	min 150	°C
T_{JSDH}	Thermal shutdown Hysteresis	max 35	°C

PIN CONNECTION



THERMAL DATA

$R_{th\ j\ case}$	Thermal Resistance Junction-case	max 1.5	°C/W
$R_{th\ j\ camb}$	Thermal Resistance Junction-ambient	max 60	°C/W

DIAGNOSTIC DECISION TABLE

STATE	ENABLE	INPUT	OUTPUT		T_D	FUNCTION	DIAGNOSTIC
			V_O	I_O			
OFF	H	H	L	X	$<T_{JSD}$	NORMAL "OFF"	H
	H	H	L	X	$>T_{JSD}$ *	THERMAL OVERLOAD "OFF"	L
	H	H	$>V_{ODTH}$ *	X	$<T_{JSD}$	OUTPUT FAIL/"OFF"	L
ON	H	L	H	X	$<T_{JSD}$	NORMAL "ON"	H
	H	L	X	X	$>T_{JSD}$ *	THERMAL OVERLOAD "ON"	H
	H	L	$<V_S - V_{OEXD}$ *	$>I_{SC}$	X	EXTERNAL DROP DUE TO OVERCURRENT	H
	H	L	$<V_S - V_{OEXD}$ *	X	$<T_{JSD}$	XCESSIVE DROP "ON"	H
ST-BY	L	X	X	X	X	STANDBY MODE	H

(*)Parameter causing Diagnostic = LOW

ELECTRICAL CHARACTERISTICS (V_S = 6 to 45V (1); T_j = -40 to 150°C; V_{EN} = HIGH; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{ON}	ON Resistance	V_I < 0.8V; T_j < 125°C		200	400	mΩ
I_{SC}	Short Circuit Current	$V_{SDC} \leq$ 32V; V_{SPULSE} (Tp < 2ms)	1	2.7	4	A
I_{OC} (2)	Output Current	V_O = -18V			100	mA
I_Q	OFF State Quiescent Current	V_I > 2V; V_S = 32V; V_I > 2V;		4.5 7.5	10 12	mA mA
I_Q	ON State Quiescent Current	V_I < 0.8V; V_S = 32V; V_I < 0.8V;		4.5 10	10 16	mA mA
V_{IL}	Input Low Level				0.8	V
V_{IH}	Input High Level		2			V
V_{ITH}	Input Threshold Hysteresis		50	100		mV
I_{IN}	Input Current	V_I = 0 to 5.5V			10	µA
I_{DFL}	Diagnostic Output Leakage Current	$T_j \leq$ 125°C; V_D = 7V; Diagnostic output High			10	µA
V_{DFL}	Diagnostic Output Low	$I_{DF} \leq$ 2mA			0.4	V
V_{OEXD}	Excessive Dropout Voltage Detection Level		1	1.5	2	V
V_{ODTH}	Output Diagnostic Threshold	$V_I \geq$ 2V	4		6	V
t_{RD}	Diagnostic Delay Time				10	µs
I_{QSB}	Standby Mode Quiescent Current	V_{EN} < 0.8V; $T_j \leq$ 125°C; V_S= 27V V_S= 13V			400 200	µA µA
V_{ENL}	Enable Level Low	Standby Mode			0.8	V
V_{ENH}	Enable Level High		2			V
V_{ENTH}	Enable Threshold Hysteresis		50	100		mV
I_{ENH}	Enable Input Current High	V_{EN} = 2 to 5.5V; V_{EN} < V_S -2			10	µA
I_{ENL}	Enable Input Current Low	V_{EN} = 0 to 0.8V;	-1		1	µA
t_{rON}	ON Rise Time (3)	with C_B: $V_S \leq$ 32V V_S > 8V V_S > 10V t_{OFF} > 0.3ms			 4 2 6	 µs µs µs
t_{fOFF}	OFF Fall Time	V_S = 8 to 32V			2	µs
t_{dON}	ON Delay Time	V_S = 8 to 32V		1	3	µs
t_{dOFF}	OFF Delay Time	V_S = 8 to 32V		1	3	µs
t_d	Diff. Delay Time t_{dON} - t_{dOFF}	VS = 8 to 32V			4	µs

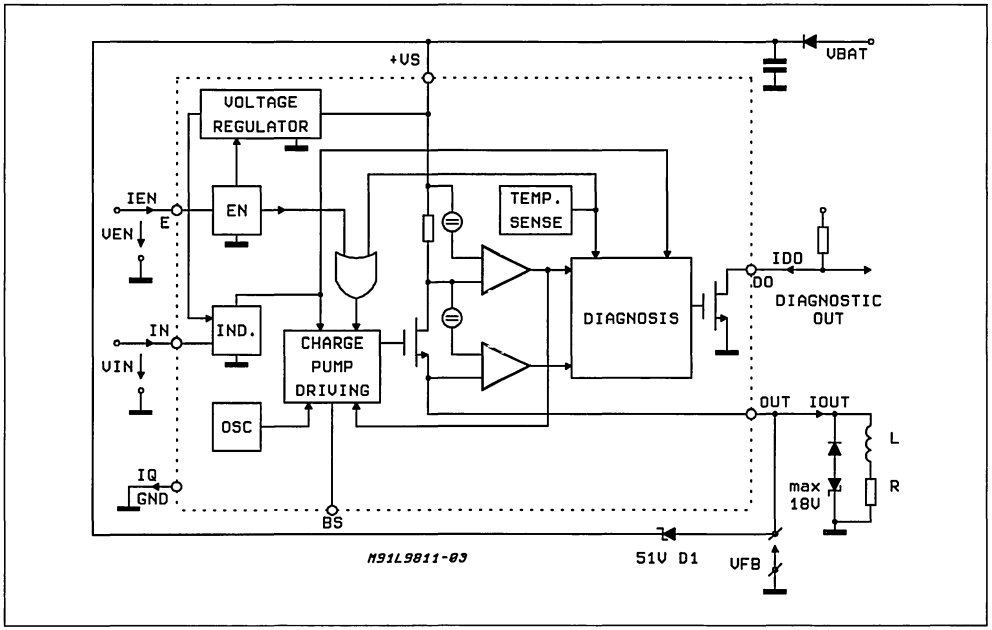
Notes:

1) For Vs < 6V the device can switch off

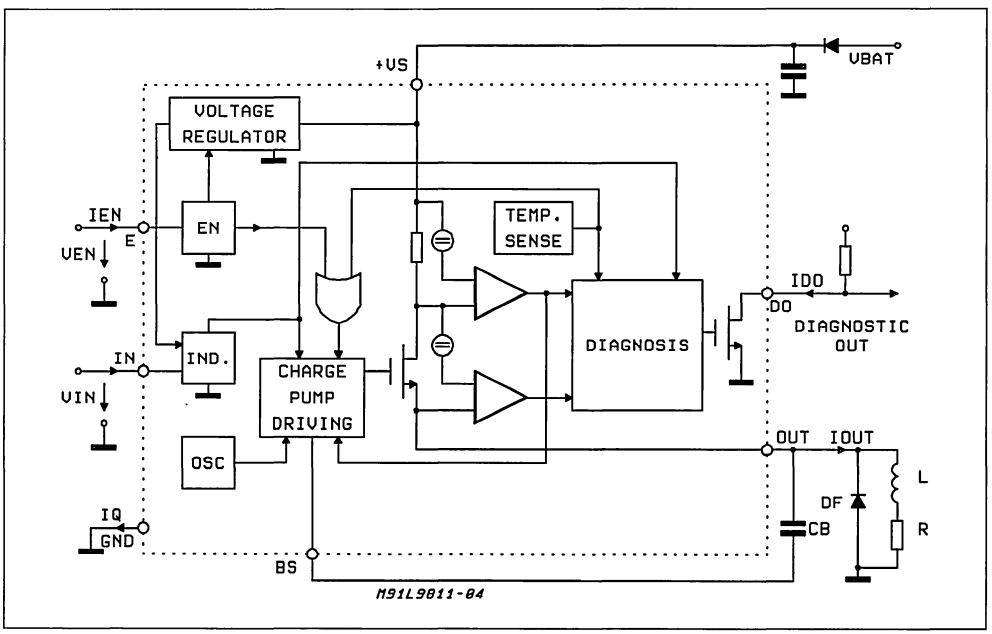
2) An external recirculation path must be assured in PWM operation to avoid excessive power dissipation

3) Measured with resistive load and I_{LOAD} = 1A from 10% to 90% of the output voltage amplitude with C_B = 33nF and after t_{OFF} < 10µs

APPLICATION DIAGRAM: DC Operation



APPLICATION DIAGRAM: PWM Operation



SGS-THOMSON MICROELECTRONICS

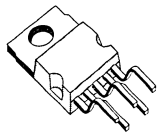
L9821

HIGH SIDE DRIVER

ADVANCE DATA

- 25A PEAK OUTPUT CURRENT
- R_{ON} = 100mΩ
- DIAGNOSTIC AND PROTECTION FUNCTIONS
- µP COMPATIBLE
- GROUNDED CASE
- INRUSH CURRENT LIMITING CIRCUIT

MULTIPOWER BCD TECHNOLOGY



Pentawatt

ORDERING NUMBER : L9821

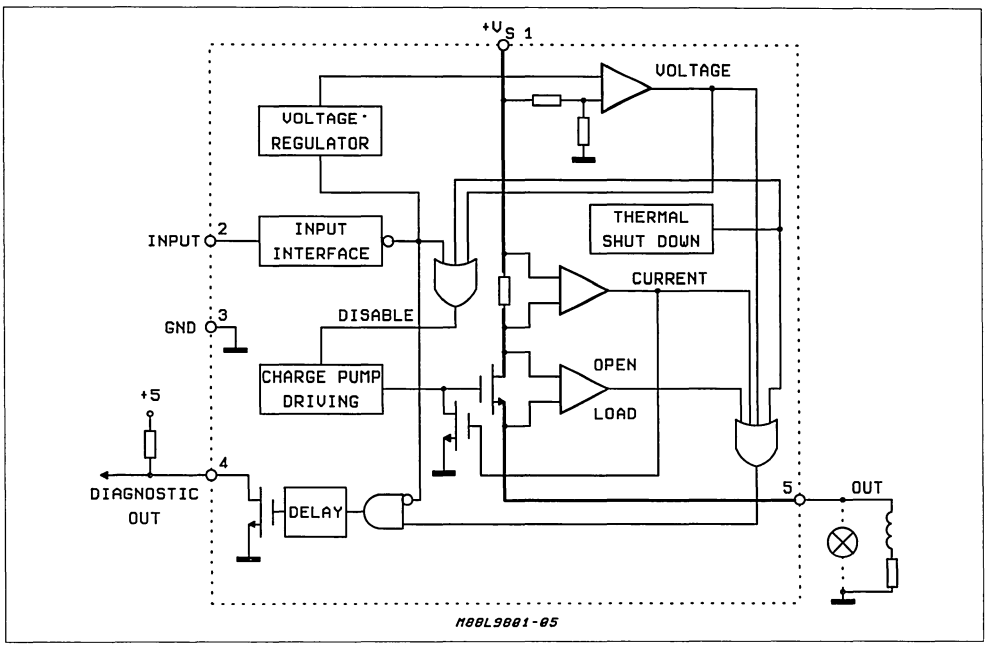
DESCRIPTION

The L9821 High Side Driver realized with Multipower - BCD mixed technology, drives resistive or inductive loads with one side connected to ground.

The input control is TTL compatible and a diagnostic output provides an indication of load (open and short) and device status (thermal and overvoltage shutdown). On chip thermal protection and short circuit protection are provided.

The device is assembled in the Pentawatt package with the tab connected to the ground terminal.

BLOCK DIAGRAM



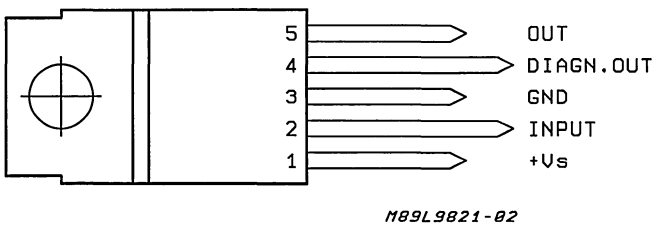
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value
V_S	Max Forward Voltage Positive Transient Peak Voltage (dump : τ_f fall time constant = 100ms, 5ms ≤ t_{rise} ≤ 10ms, R_{source} ≥ 0.5Ω) – Resistive Load – Inductive Load	50Vdc 50V 50V (*)
	Reverse Input Voltage	– 0.3Vdc
V_I V_4 V_5	Input Voltage Pin 2 (to GND) Pin 4 Voltage (to GND) Pin 5 Voltage (to GND)	– 0.3V / + V_S (V_S < 20V) – 0.3V / + V_S (V_S < 20V) – 3V / + V_S (V_S < 20V)
I_1 I_2 I_4 I_5	Pin 1 Current Pin 2 Current (forced) Pin 4 Current (sink) Pin 5 Current	Internally Limited 0.5mA 10mA Internally Limited
P_{TOT}	Power Dissipation	Internally Limited
T_J, T_{STG}	Junction and Storage Temperature Range	– 55°C to + 150°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.5	°C/W

PIN CONNECTION (top view)



M89L9821-02

PIN FUNCTIONS

1. POWER SUPPLY

Supply voltage input. When the supply reaches the maximum operating voltage (32V) the device is turned off, protecting itself and the load.
Turning off guaranteed for $V_S > 41V$.

2. INPUT

TTL compatible input. High level on this pin means output current ON. The low level voltage switches off the charge pump, the power stage and the diagnostic output reducing to the minimum value the quiescent current.

3. GROUND

This pin must be connected to ground.

4. DIAGNOSTIC FEEDBACK
The diagnostic circuit is active in input high level condition. This output detects with Tipically 45ms delay at $T_{amb} = 25°C$ the following faults :

- Overvoltage condition.
- Thermal shutdown.
- Short circuit. The power stage current is internally limited at 25A.
- Open load. The open load condition is detected with load current < 0.6A.

The diagnostic output is active low. The diagnostic delay time allows to avoid spurious diagnosys (i.e : turn ON overcurrent, overvoltage spikes etc.).

5. POWER OUTPUT

The device is provided with short circuit protection.

ELECTRICAL CHARACTERISTICS ($V_S = 14.4V$; $-40°C \leq T_j \leq 125°C$, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OP}	Operat. Voltage		6		32	V
R_{ON}	On Resistance	Input >2V:T_j = 25°C Input >2V:Full T range		0.1	 0.2	Ω
I_{SC}	Short circuit current			25		A
I_{DL}	Over Current Detection Level			20		A
I_{OPD}	Open Load Detection Level	Device ON			1.2	A
V_{clamp}	Output Under Voltage Clamping	I_{load} <6A Inductive	-12		-4	V
I_{Off}	Off State Supply Current	T_j = -40 to 35°C T_j = 35 to 85°C			100 300	µA µA
I_{ON}	ON State Supply Current	T_j = 25°C		10		mA
V_{IL}	Input Low Level				0.8	V
V_{IH}	Input High Level		2.0			V
I_I	Input Current	$V_I = V_{threshold}$			15	µA
I_{LEAKD}	Diagnostic Output Leakage Voltage	VCC = 5V Diagnostic Output			10	µA
V_{SATD}	Diagnostic Output Saturation Voltage	I_{sink} <1.6mA			0.4	V
T_{Dd}	Diagnostic Delay Time	T_j = 25°C;		45		ms
t_{dON}	Output ON Delay Time	T_j = 25°C		15		µs
t_r	Output ON Rise Time	T_j = 25°C		65		µs
t_{dOFF}	Output OFF Delay Time	T_j = 25°C		50		µs
t_f	Output OFF Fall Time	T_j = 25°C		100		µs

FUNCTIONAL DESCRIPTION

The L9821 is a high side drive monolithic switch, driven by TTL, CMOS input logic, able to supply resistive or inductive loads up to 6A DC allowing a current peak of 25A with a $R_{DS(ON)}$ = 0.1. The electronic switch, in addition to its main function, protects itself, the power network and the load against load dump (up to 60V) and overload and it detects short circuit, open load and overtemperature conditions. All these functions (logic control and power actuation) are possible on a single chip thanks to the new mixed ST Multipower BCD technology that allows to integrate isolated DMOS power transistors in combination with Bipolar and CMOS signal structures on the same chip.

The high side drive connection (series switch between the load and the positive power source) is particularly suited in automotive environment where the electrochemical corrosion withstanding has primary importance. For this connection the best solution is a Power MOS N-channel which requires for driving only a capacitive charge pump completely integrated on the switch chip.

The L9821 is based on a power DMOS series element, a driving circuit with a charge pump, an input logic interface and on some protection and fault detection circuits.

The power DMOS transistor has a $R_{DS(ON)}$ = 0.1Ω (typ. value @ T_J = 25°C, V_{GS} = 10V). The low value of $R_{DS(ON)}$ is important both to increase the power transferred to the load and to minimize the power dissipated in the device.

The charge pump is a capacitive voltage tripler starting from power supply (car battery), driven by a 500kHz oscillator.

The input interface is based on a circuitry solution able to guarantee the stability over temperature of the TTL logic levels and very low quiescent current in OFF condition.

When the supply reaches the maximum operating voltage (32V) the device is turned OFF, protecting itself and the load ; moreover local zener clamps are provided in some critical points to avoid that V_{GS} of any MOS transistor could reach dangerous values even during 60V load dump transient.

The inrush current limiting is a significant feature of the L9821. This function allows to protect the power supply network and may extend the life of the loads. For example, in the case of the lamps, the tungsten wire resistance value in cold condition is about one tenth of the nominal steady state and then the inrush current during the turn on is statistically one of the main causes of lamps failures. If the high current condition persists (e.g. load short circuit) and the junction temperature rises above 150°C, the thermal protection circuit turns off the device preventing any damage. The current limiting and the thermal shutdown are sufficient to protect the device against any overload because the power DMOS has not the second breakdown.

When the L9821 is driven and one of the protections (overtemperature, overvoltage, overload) is present, a fault detection open drain output turns on. This output is active also when I_{load} is lower than 0.6A detecting the open load (disconnected or burned out). The diagnostic output detects fault conditions with 25ms delay in order to avoid spurious diagnosys (i.e. : turn on overcurrent, overvoltage spikes etc.). In OFF conditions the fault detection circuits are not active to allow a minimum quiescent current.

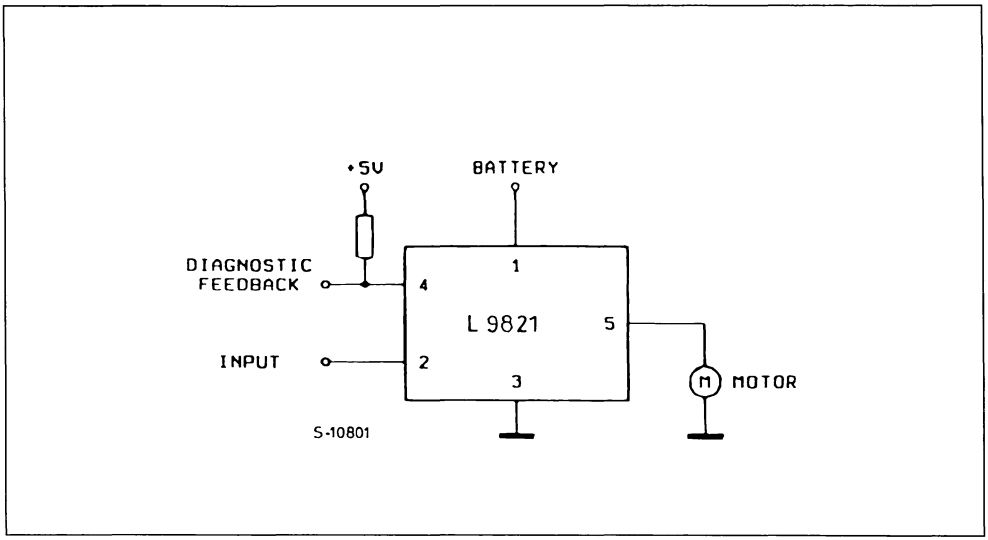
The device can drive unipolar DC motors and solenoids as well because it can recirculate an inductive current when the output voltage goes lower than V_{clamp} value (typically - 6.5V in respect to ground). The possibility to have a start up current is useful also for DC motors allowing the maximum starting torque.

TYPICAL APPLICATION OF THE L9821

The L9821 integrated high side driver can be used to replace an electromechanical relay.

Inductive load (i.e. solenoids, motors) can be driven by the L9821. No external components are required for the coil current recirculation, because the device provides this function internally.

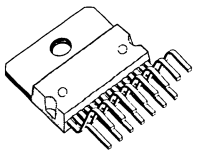
Figure 1.


+5V
BATTERY
DIAGNOSTIC
FEEDBACK
INPUT
1
2
3
4
5
L 9821
M
MOTOR
S-10801

OCTAL SERIAL SOLENOID DRIVER

ADVANCE DATA

- EIGHT HIGH CURRENT OUTPUTS CAPABLE OF DRIVING UP TO 0.75A PER OUTPUT
- 8 BIT SERIAL INPUT DATA
- 8 BIT SERIAL DIAGNOSTIC OUTPUT FOR OVERLOAD AND OPEN CIRCUIT CONDITIONS
- OUTPUT SHORT CIRCUIT PROTECTION
- CHIP ENABLE SELECT FUNCTION (active low)
- INTERNAL 34V CLAMPING FOR EACH OUTPUT
- CASCADABLE WITH ANOTHER OCTAL DRIVER



Multiwatt15

ORDERING NUMBER : L9822

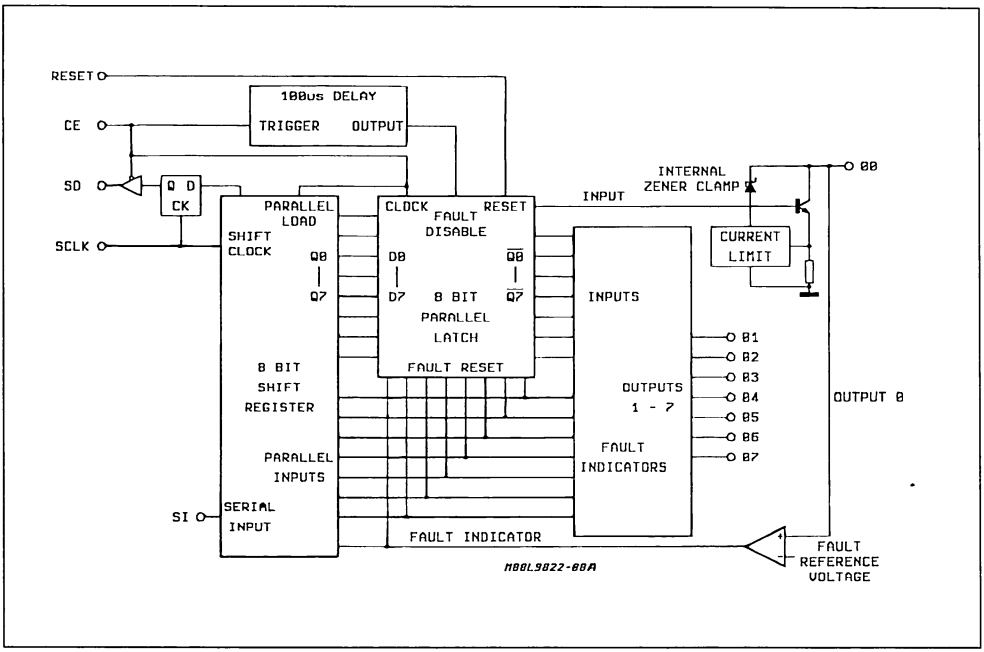
DESCRIPTION

TheL9822 is an octal low side solenoid driver rea lized in Multipower-BCD technology particularly suited for driving lamps, relays and solenoids in automotive environment.

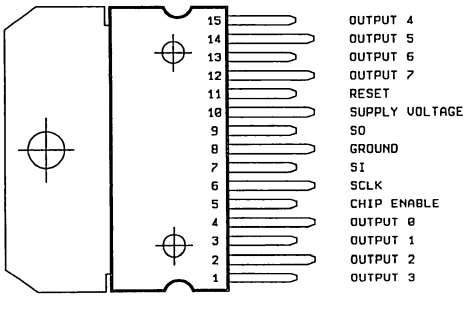
Data is transmitted serially to the device using the Serial Peripheral Interface (SPI) protocol.

The L9822 features the outputs status monitoring function.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
V_{CC}	DC Logic Supply	– 0.7	7	V
V_O	Output Voltage	– 0.7	32	V
I_I	Input Transient Current (CE, SI, SCLK, RESET, SO) : Duration Time t = 1s, $V_I < 0$ $V_I > V_{CC}$	 – 25	 + 25	 mA mA
I_{Odc}	Continous Output Current (for each output)	Int. Limited		A
T_j, T_{stg}	Junction and Storage Temperature Range	– 55	150	C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

PIN DESCRIPTION

V_{CC}

Logic supply voltage - nominally 5V

GROUND

Device Ground. This ground applies for the logic circuits as well as the power output stages.

RESET

Asynchronous reset for the output stages, the parallel latch and the shift register inside the L9822. This pin is active low and it must not be left floating. A power on clear function may be implemented connecting this pin to V_{CC} with an external resistor and to ground with an external capacitor.

CE

Chip Enable. Data is transferred from the shift registers to the outputs on the rising edge of this signal. The falling edge of this signal sets the shift register with the output voltage sense bits coming from the output stages. The output driver for the SO pin is enabled when this pin is low.

SO

Serial Output. This pin is the serial output from the shift register and it is tri-stated when CE is high. A high for a data bit on this pin indicates that the particular output is high. A low on this pin for a data bit indicates that the output is low.

Comparing the serial output bits with the previous serial input bits the external microcontroller implements the diagnostic data supplied by the L9822.

SI

Serial Input. This pin is the serial data input. A high on this pin will program a particular output to be OFF, while a low will turn it ON.

SCLK

Serial Clock. This pin clocks the shift register. New SO data will appear on every rising edge of this pin and new SI data will be latched on every SCLK's falling edge into the shift register.

OUTPUTS 00-07

Power output pins. The input and output bits corresponding to 07 are sent and received first via the SPI bus and 00 is the last. The outputs are provided with current limiting and voltage sense functions for fault indication and protection. The nominal load current for these outputs is 500mA, but the current limiting is set to a minimum of 1.2A. The outputs also have on board clamps set at about 32V for recirculation of inductive load current.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%. T_j = – 40 to 125°C ; unless otherwise speciifed)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OC}	Output Clamping Volt.	I_O = 0.5A, Output Programmed OFF	30		40	V
E_{OC}	Out. Clamping Energy	I_O = 0.5A, When ON	20			mJ
I_{Oleak}	Out. Leakage Current	V_O = 24V, Output Progr. OFF			1000	µA
V_{sat}	Output Sat. Voltage	Output Progr. ON I_O = 0.5A I_O = 0.75A I_O = 1A With Fault Reset Disabled			 0.5 1.25 2.0	 V V V
I_{OL}	Out. Current Limit	Output Progr. ON	1.0			A
t_{PHL}	Turn-on Delay	I_O = 500mA No Reactive Load			10	µs
t_{PLH}	Turn-off Delay	I_O = 500mA No Reactive Load			10	µs
V_{OREF}	Fault Refer. Voltage	Output Progr. ON Fault detected if $V_O > V_{OREF}$	1.60		2.40	V
t_{UD}	Fault Reset Delay (after CE L to H transition)	See fig. 3	65		260	µs
V_{OFF}	Output OFF Voltage	Output Progr. OFF, Output Pin Floating.			1.0	V

ELECTRICAL CHARACTERISTICS (continued)

INPUT BUFFER (SI, CE, SCLK and RESET pins)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{T-}	Threshold Voltage at Falling Edge	V_{CC} = 5V ± 10%	0.2V_{CC}			V
V_{T+}	Threshold Voltage at Rising Edge	V_{CC} = 5V ± 10%			0.8V_{CC}	V
V_H	Hysteresis Voltage	$V_{T+} - V_{T-}$	0.85		2.25	V
I_I	Input Current	V_{CC} = 5.25V, 0 < V_I < V_{CC}	– 10		+ 10	µA
C_I	Input Capacitance	0 < V_I < V_{CC}			20	pF

OUTPUT BUFFER (SO pin)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SOL}	Output LOW Voltage	I_O = 1.6mA			0.4	V
V_{SOH}	Output HIGH Voltage	I_O = 0.8mA	V_{CC} – 1.3V			V
I_{SOtl}	Output Tristate Leakage Current	0 < V_O < V_{CC}, CE Pin Held High, V_{CC} = 5.25V	– 10		10	µA
C_{SO}	Output Capacitance	0 < V_O < V_{CC} CE Pin Held High			20	pF
I_{CC}	Quiescent Supply Current at V_{CC} Pin	T_J = 125°C T_J = 25°C T_J = – 40°C All Outputs Progr. ON.			151 200 250	mA mA mA

SERIAL PERIPHERAL INTERFACE (see fig. 2, timing diagram)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{op}	Operating Frequency		D.C.		500	KHz
t_{lead}	Enable Lead Time		1000			ns
t_{lag}	Enable Lag Time		1000			ns
t_{wSCKH}	Clock HIGH Time		840			ns
t_{wSCKL}	Clock LOW Time		840			ns
t_{su}	Data Setup Time		500			ns
t_H	Data Hold Time		500			ns
t_{EN}	Enable Time				1000	ns
t_{DIS}	Disable Time				1000	ns
t_V	Data Valid Time				740	ns
t_{rSO}	Rise Time (SO output)	V_{CC} = 20 to 70% C_L = 200pF			100	ns
t_{fSO}	Fall Time (SO output)	V_{CC} = 70 to 20% C_L = 200pF			100	ns
t_{rSI}	Rise Time SPI Inputs (SCK, SI, CE)	V_{CC} = 20 to 70% C_L = 200pF			2.0	µs
t_{fSI}	Fall Time SPI Inputs (SCLK, SI, CE)	V_{CC} = 70 to 20% C_L = 200pF			2.0	µs
t_{ho}	Output Data Hold Time		0			µs

FUNCTIONAL DESCRIPTION

The L9822 is a low operating power device featuring, eight 0.75A open collector drivers with transient protection circuits in output stages. Each channel is independently controlled by an output latch and a common RESET line which disables all eight outputs. The driver has low saturation and short circuit protection and can drive inductive and resistive loads such as solenoids, lamps and relais. Data is transmitted to the device serially using the Serial Peripheral Interface (SPI) protocol. The circuit receives 8 bit serial data by means of the serial input (SI) which is stored in an internal register to control the output drivers. The serial output (SO) provides 8 bit of diagnostic data representing the voltage level at the driver output. This allows the microprocessor to diagnose the condition of the output drivers.

The output saturation voltage is monitored by a comparator for an out of saturation condition and is able to unlatch the particular driver through the fault reset line. This circuit is also cascadable with another octal driver in order to jam 8 bit multiple data. The device is selected when the chip enable (CE) line is low.

Additionally the (SO) is placed in a tri-state mode when the device is deselected. The negative edge of the (CE) transfers the voltage level of the drivers to the shift register and the positive edge of the (CE) latches the new data from the shift register to the drivers. When CE is Low, data bit contained into the shift register is transferred to SO output at every SCLK positive transition while data bit present at SI input is latched into the shift register on every SCLK negative transition.

INTERNAL BLOCKS DESCRIPTION

The internal architecture of the device is based on the three internal major blocks : the octal shift register for talking to the SPI bus, the octal latch for holding control bits written into the device and the octal load driver array.

SHIFT REGISTER

The shift register has both serial and parallel inputs and serial and parallel outputs. The serial input accepts data from the SPI bus and the serial output simultaneously sends data into the SPI bus. The parallel outputs are latched into the parallel latch inside the L9822 at the end of a data transfer. The parallel inputs jam diagnostic data into the shift register at the beginning of a data transfer cycle.

PARALLEL LATCH

The parallel latch holds the input data from the shift register. This data then actuates the output stages. Individual registers in the latch may be cleared by fault conditions in order to protect the overloaded output stages. The entire latch may also be cleared by the RESET signal.

OUTPUT STAGES

The output stages provide an active low drive signal suitable for 0.75A continuous loads. Each output has a current limit circuit which limits the maximum output current to at least 1.0A to allow for high inrush currents. Additionally, the outputs have internal zeners set to 35 volts to clamp inductive transients at turn-off. Each output also has a voltage comparator observing the output node. If the voltage exceeds 1.6V on an ON output pin, a fault condition is assumed and the latch driving this particular stage is reset, turning the output OFF to protect it. The timing of this action is described below. These comparators also provide diagnostic feedback data to the shift register. Additionally, the comparators contain an internal pulldown current which will cause the cell to indicate a low output voltage if the output is programmed OFF and the output pin is open circuited.

TIMING DATA TRANSFER

Figure #2 shows the overall timing diagram from a byte transfer to and from the L9822 using the SPI bus.

CE High to Low Transition

The action begins when the Chip Enable (CE) pin is pulled low. The tri-state Serial Output (SO) pin driver will be enabled entire time that CE is low. At the falling edge of the CE pin, the diagnostic data from the voltage comparators in the output stages will be latched into the shift register. If a particular output is high, a logic one will be jammed into that bit in the shift register. If the output is low, a logic zero will be loaded there. The most significant bit (07) should be presented at the Serial Input (SI) pin. A zero at this pin will program an output ON, while a one will program the output OFF.

SCLK Transitions

The Serial Clock (SCLK) pin should then be pulled high. At this point the diagnostic bit from the most significant output (07) will appear at the SO pin. A high here indicates that the 07 pin is higher than 1.5V. The SCLK pin should then be toggled low then high. New SO data will appear following every rising edge of SCLK and new SI data will be latched into the L9822 shift register on the falling edges. An unlimited amount of data may be shifted through the device shift register (into the SI pin and out the SO

pin), allowing the other SPI devices to be cascaded in a daisy chain with the L9822.

CE Low to High Transition

Once the last data bit has been shifted into the L9822, the CE pin should be pulled high.

At the rising edge of CE the shift register data is latched into the parallel latch and the output stages will be actuated by the new data. An internal 135 usec delay timer will also be started at this rising edge. During the 135 usec period, the outputs will be protected only by the analog current limiting circuits since the resetting of the parallel latches by faults conditions will be inhibited during this period. This allows the part to overcome any high inrush currents that may flow immediately after turn on. Once the delay period has elapsed, the output voltages are sensed by the comparators and any output with voltages higher than 1.6V are latched OFF. It should be noted that the SCLK pin should be low at both transitions of the CE pin to avoid any false clocking of the shift register. The SCLK input is gated by the CE pin, so that the SCLK pin is ignored whenever the CE pin is high.

FAULT CONDITIONS CHECK

Checking for fault conditions may be done in the following way. Clock in a new control byte. Wait 260 microseconds or so to allow the outputs to settle. Clock in the same control byte and observe the diagnostic data that comes out of the device. The diagnostic bits should be identical to the bits that were first clocked in. Any differences would point to a fault on that output. If the output was programmed ON by clocking in a zero, and a one came back as the diagnostic bit for that output, the output pin was still high and a short circuit or overload condition exists. If the output was programmed OFF by clocking in a one, and a zero came back as the diagnostic bit for that output, nothing had pulled the output pin high and it must be floating, so an open circuit condition exists for that output.

Figure 1 : Byte Timing with Asynchronous Reset.

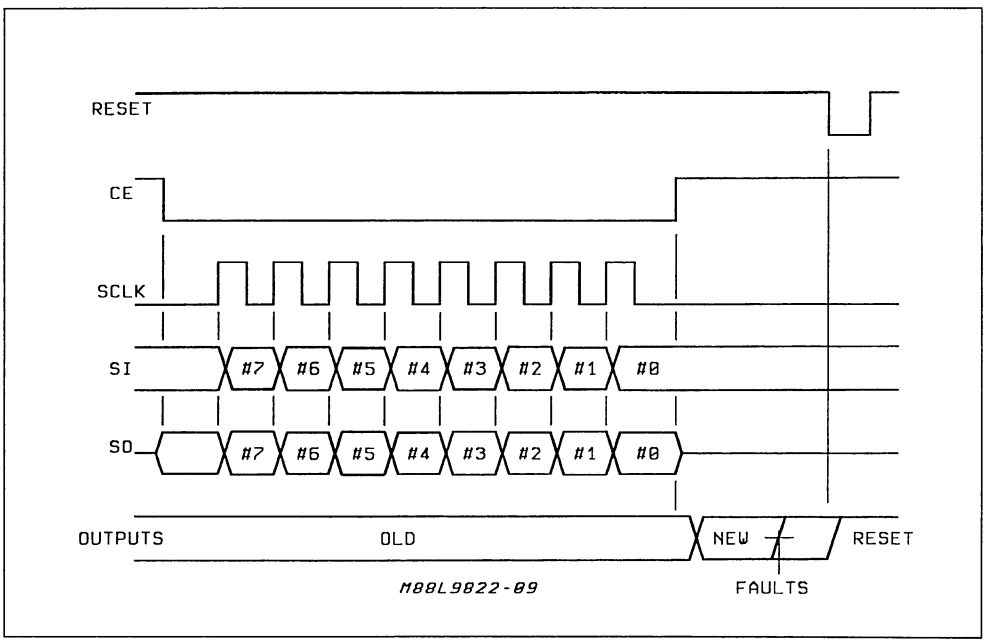


Figure 2 : Timing Diagram.

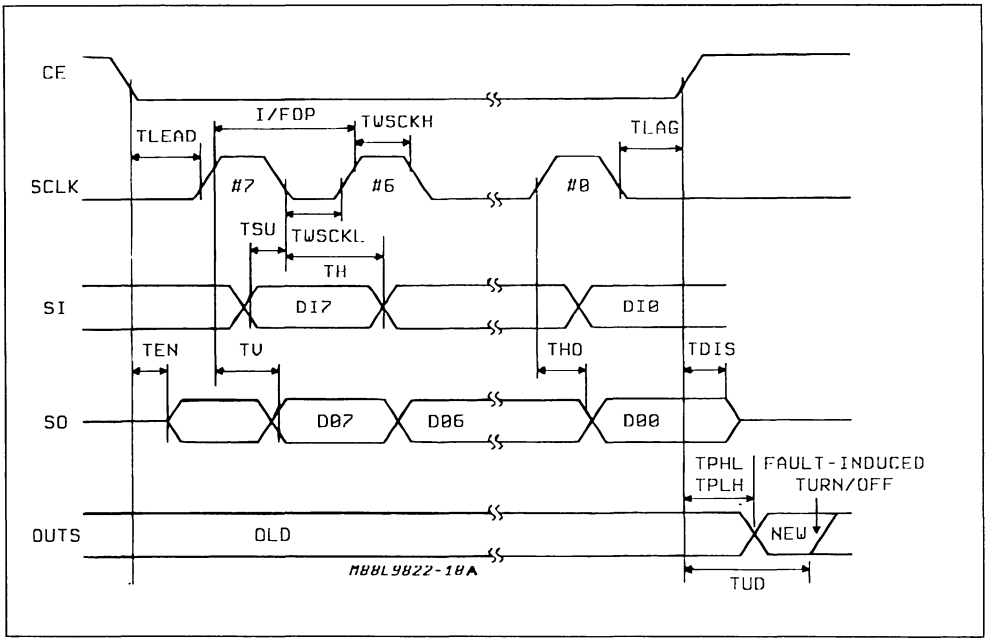
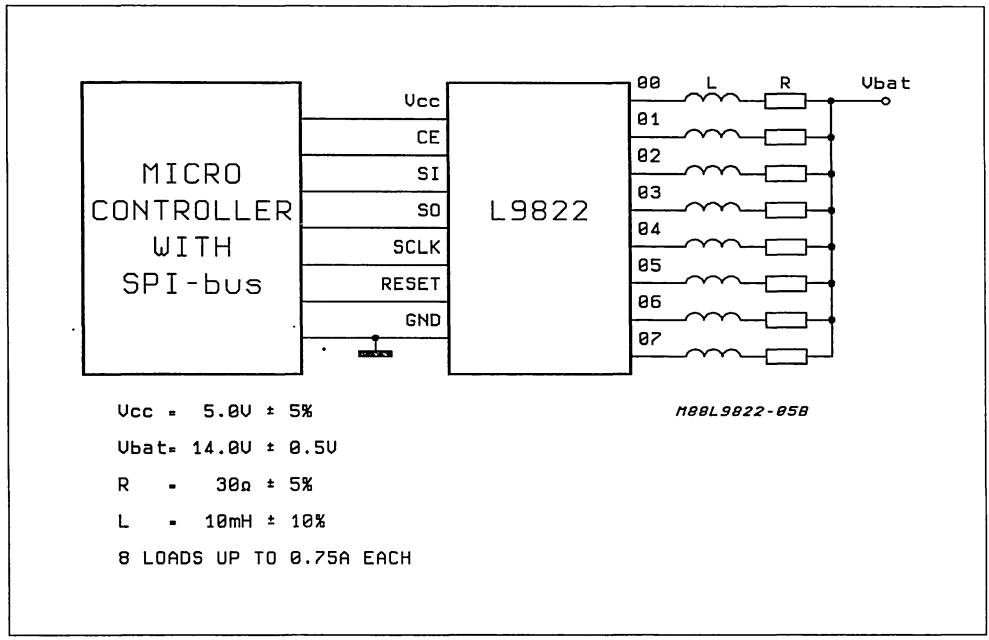


Figure 3 : Typical Application Circuit.



Vcc = 5.0V ± 5%

Vbat= 14.0V ± 0.5V

R = 30Ω ± 5%

L = 10mH ± 10%

8 LOADS UP TO 0.75A EACH

SGS-THOMSON MICROELECTRONICS

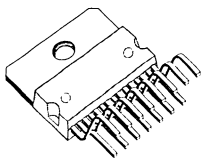
L9822E

OCTAL SERIAL SOLENOID DRIVER

PRODUCT PREVIEW

- EIGHT LOW R_{DSon} DMOS OUTPUTS (1Ω AT I_O = 1A)
- 8 BIT SERIAL INPUT DATA (SPI)
- 8 BIT SERIAL DIAGNOSTIC OUTPUT FOR OVERLOAD AND OPEN CIRCUIT CONDITIONS
- OUTPUT SHORT CIRCUIT PROTECTION
- CHIP ENABLE SELECT FUNCTION (active low)
- INTERNAL 36V CLAMPING FOR EACH OUTPUT
- CASCADABLE WITH ANOTHER OCTAL DRIVER
- LOW QUIESCENT CURRENT (10mA MAX.)
- PACKAGE MULTIWATT15

MULTIPOWER BCD TECHNOLOGY



Multiwatt15

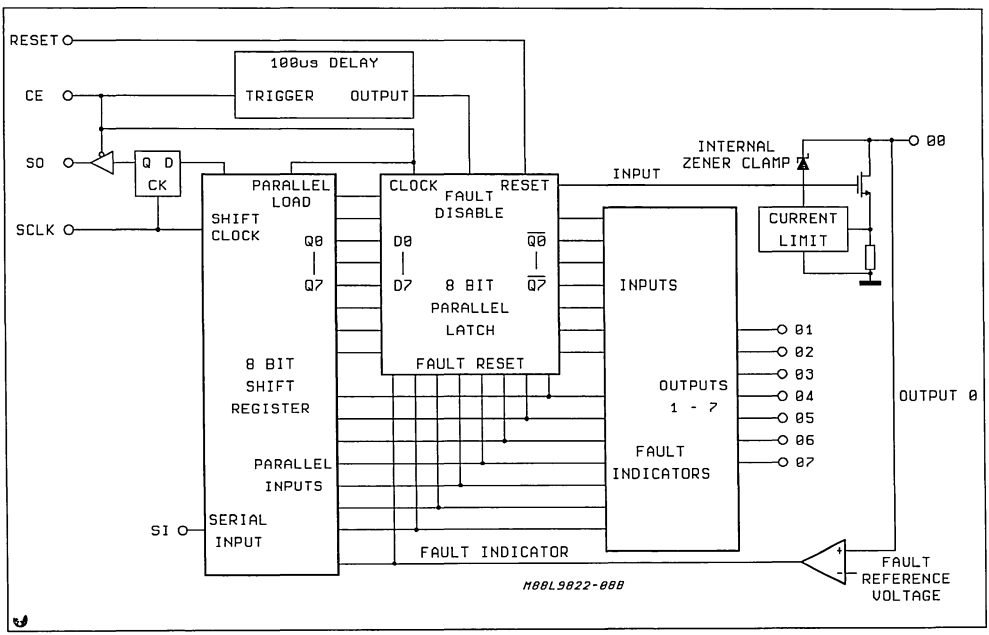
DESCRIPTION

TheL9822E is an octal low side solenoid driver rea lized in Multipower-BCD technology particularly suited for driving lamps, relays and solenoids in automotive environment. Thanks to the DMOS outputs L9822E has a very low power consumption.

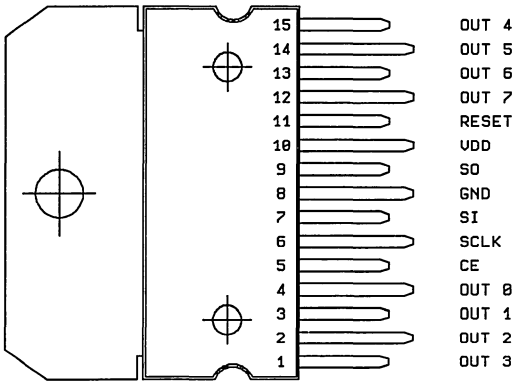
Data is transmitted serially to the device using the Serial Peripheral Interface (SPI) protocol.

The L9822E features the outputs status monitoring function.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
V_{CC}	DC Logic Supply	− 0.7	7	V
V_O	Output Voltage	− 0.7	40	V
I_I	Input Transient Current (CE, SI, SCLK, RESET, SO) : Duration Time t = 1s, $V_I < 0$ $V_I > V_{CC}$	 − 25	 + 25	 mA mA
I_{Odc}	Continous Output Current (for each output)	Int. Limited		A
T_j, T_{stg}	Junction and Storage Temperature Range	− 40	150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-Case	Max.	2	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-Ambient	Max.		°C/W

PIN DESCRIPTION

V_{CC}

Logic supply voltage - nominally 5V

GROUND

Device Ground. This ground applies for the logic circuits as well as the power output stages.

RESET

Asynchronous reset for the output stages, the parallel latch and the shift register inside the L9822E. This pin is active low and it must not be left floating. A power on clear function may be implemented connecting this pin to V_{CC} with an external resistor and to ground with an external capacitor.

CE

Chip Enable. Data is transferred from the shift registers to the outputs on the rising edge of this signal. The falling edge of this signal sets the shift register with the output voltage sense bits coming from the output stages. The output driver for the SO pin is enabled when this pin is low.

SO

Serial Output. This pin is the serial output from the shift register and it is tri-stated when CE is high. A high for a data bit on this pin indicates that the particular output is high. A low on this pin for a data bit indicates that the output is low.

Comparing the serial output bits with the previous serial input bits the external microcontroller implements the diagnostic data supplied by the L9822.

SI

Serial Input. This pin is the serial data input. A high on this pin will program a particular output to be OFF, while a low will turn it ON.

SCLK

Serial Clock. This pin clocks the shift register. New SO data will appear on every rising edge of this pin and new SI data will be latched on every SCLK's falling edge into the shift register.

OUTPUTS 00-07

Power output pins. The input and output bits corresponding to 07 are sent and received first via the SPI bus and 00 is the last. The outputs are provided with current limiting and voltage sense functions for fault indication and protection. The nominal load current for these outputs is 500mA, but the current limiting is set to a minimum of 1.05A. The outputs also have on board clamps set at about 36V for recirculation of inductive load current.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%. T_j = – 40 to 125°C ; unless otherwise speciifed)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OC}	Output Clamping Volt.	I_O = 0.5A, Output Programmed OFF	30		40	V
E_{OC}	Out. Clamping Energy	I_O = 0.5A, When ON	20			mJ
I_{Oleak}	Out. Leakage Current	V_O = 24V, Output Progr. OFF			1	mA
R_{DSon}	On Resistance	Output Progr. ON I_O = 0.5A I_O = 0.8A I_O = 1A With Fault Reset Disabled			 1 1 1	 Ω Ω Ω
I_{OL}	Out. Self Limiting Current	Output Progr. ON	1.05			A
t_{PHL}	Turn-on Delay	I_O = 500mA No Reactive Load			10	µs
t_P	Turn-off Delay	I_O = 500mA No Reactive Load			10	µs
V_{OREF}	Fault Refer. Voltage	Output Progr. ON Fault detected if $V_O > V_{OREF}$	1.6		2	V
t_{UD}	Fault Reset Delay (after CE L to H transition)	See fig. 3	75		250	µs
V_{OFF}	Output OFF Voltage	Output Pin Floating.cOutput Progr. OFF,			1.0	V

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INPUT BUFFER (SI, CE, SCLK and RESET pins)						
V_{T-}	Threshold Voltage at Falling Edge SCLK only	V_{CC} = 5V ± 10%	0.2V_{CC} 0.6			V V
V_{T+}	Threshold Voltage at Rising Edge SCLK only	V_{CC} = 5V ± 10%			0.7V_{CC} 4.15	V V
V_H	Hysteresis Voltage	$V_{T+} - V_{T-}$	0.85		2.5	V
I_I	Input Current	V_{CC} = 5.50V, 0 < V_I < V_{CC}	– 10		+ 10	µA
C_I	Input Capacitance	0 < V_I < V_{CC}			20	nF
OUTPUT BUFFER (SO pin)						
V_{SOL}	Output LOW Voltage	I_O = 1.6mA			0.4	V
V_{SOH}	Output HIGH Voltage	I_O = 0.8mA	V_{CC} – 1.3V			V
I_{SOtl}	Output Tristate Leakage Current	0 < V_O < V_{CC}, CE Pin Held High, V_{CC} = 5.25V	– 20		20	µA
C_{SO}	Output Capacitance	0 < V_O < V_{CC} CE Pin Held High			20	pF
I_{CC}	Quiescent Supply Current at V_{CC} Pin	All Outputs Progr. ON. I_O = 0.5A per Output Simultaneously			10	mA
SERIAL PERIPHERAL INTERFACE (see fig. 2, timing diagram)						
f_{op}	Operating Frequency		D.C.		2	MHz
t_{lead}	Enable Lead Time		250			ns
t_{lag}	Enable Lag Time		250			ns
t_{wSCKH}	Clock HIGH Time		200			ns
t_{wSCKL}	Clock LOW Time		200			ns
t_{su}	Data Setup Time		75			ns
t_H	Data Hold Time		75			ns
t_{EN}	Enable Time		250			ns
t_{DIS}	Disable Time		250			ns
t_V	Data Valid Time		100			ns
t_{rSO}	Rise Time (SO output)	V_{CC} = 20 to 70% C_L = 200pF			50	ns
t_{fSO}	Fall Time (SO output)	V_{CC} = 70 to 20% C_L = 200pF			50	ns
t_{rSI}	Rise Time SPI Inputs (SCK, SI, CE)	V_{CC} = 20 to 70% C_L = 200pF	200			ns
t_{fSI}	Fall Time SPI Inputs (SCLK, SI, CE)	V_{CC} = 70 to 20% C_L = 200pF	200			ns
t_{ho}	Output Data Hold Time		0			µs

FUNCTIONAL DESCRIPTION

The L9822E DMOS output is a low operating power device featu-ring, eight 1Ω R_{DSON} DMOS drivers with transient protection circuits in output stages. Each channel is independently controlled by an output latch and a common RESET line which disables all eight outputs. The driver has low saturation and short circuit protection and can drive inductive and resistive loads such as solenoids, lamps and relais. Data is transmitted to the device serially using the Serial Peripheral Interface (SPI) protocol. The circuit receives 8 bit serial data by means of the serial input (SI) which is stored in an internal register to control the output drivers. The serial output (SO) provides 8 bit of diagnostic data representing the voltage level at the driver output. This allows the microprocessor to diagnose the condition of the output drivers.

The output saturation voltage is monitored by a comparator for an out of saturation condition and is able to unlatch the particular driver through the fault reset line. This circuit is also cascadable with another octal driver in order to jam 8 bit multiple data. The device is selected when the chip enable (CE) line is low.

Additionally the (SO) is placed in a tri-state mode when the device is deselected. The negative edge of the (CE) transfers the voltage level of the drivers to the shift register and the positive edge of the (CE) latches the new data from the shift register to the drivers. When CE is Low, data bit contained into the shift register is transferred to SO output at every SCLK positive transition while data bit present at SI input is latched into the shift register on every SCLK negative transition.

Internal Blocks Description

The internal architecture of the device is based on the three internal major blocks : the octal shift register for talking to the SPI bus, the octal latch for holding control bits written into the device and the octal load driver array.

Shift Register

The shift register has both serial and parallel inputs and serial and parallel outputs. The serial input accepts data from the SPI bus and the serial output simultaneously sends data into the SPI bus. The parallel outputs are latched into the parallel latch inside the L9822E at the end of a data transfer. The parallel inputs jam diagnostic data into the shift register at the beginning of a data transfer cycle.

Parallel Latch

The parallel latch holds the input data from the shift register. This data then actuates the output stages. Individual registers in the latch may be cleared by fault conditions in order to protect the overloaded output stages. The entire latch may also be cleared by the RESET signal.

Output Stages

The output stages provide an active low drive signal suitable for 0.75A continuous loads. Each output has a current limit circuit which limits the maximum output current to at least 1.05A to allow for high inrush currents. Additionally, the outputs have internal zeners set to 36 volts to clamp inductive transients at turn-off. Each output also has a voltage comparator observing the output node. If the voltage exceeds 1.8V on an ON output pin, a fault condition is assumed and the latch driving this particular stage is reset, turning the output OFF to protect it. The timing of this action is described below. These comparators also provide diagnostic feedback data to the shift register. Additionally, the comparators contain an internal pulldown current which will cause the cell to indicate a low output voltage if the output is programmed OFF and the output pin is open circuited.

TIMING DATA TRANSFER

Figure #2 shows the overall timing diagram from a byte transfer to and from the L9822E using the SPI bus.

CE High to Low Transition

The action begins when the Chip Enable (CE) pin is pulled low. The tri-state Serial Output (SO) pin driver will be enabled entire time that CE is low. At the falling edge of the CE pin, the diagnostic data from the voltage comparators in the output stages will be latched into the shift register. If a particular output is high, a logic one will be jammed into that bit in the shift register. If the output is low, a logic zero will be loaded there. The most significant bit (07) should be presented at the Serial Input (SI) pin. A zero at this pin will program an output ON, while a one will program the output OFF.

SCLK Transitions

The Serial Clock (SCLK) pin should then be pulled high. At this point the diagnostic bit from the most significant output (07) will appear at the SO pin. A high here indicates that the 07 pin is higher than 1.8V. The SCLK pin should then be toggled low then high. New SO data will appear following every rising edge of SCLK and new SI data will be latched into the L9822E shift register on the falling edges. An unlimited amount of data may be shifted through the de-

vice shift register (into the SI pin and out the SO pin), allowing the other SPI devices to be cascaded in a daisy chain with the L9822E.

CE Low to High Transition

Once the last data bit has been shifted into the L9822E, the CE pin should be pulled high.

At the rising edge of CE the shift register data is latched into the parallel latch and the output stages will be actuated by the new data. An internal 160µs delay timer will also be started at this rising edge (see t_{UD}). During the 160µs period, the outputs will be protected only by the analog current limiting circuits since the resetting of the parallel latches by faults conditions will be inhibited during this period. This allows the part to overcome any high inrush currents that may flow immediately after turn on. Once the delay period has elapsed, the output voltages are sensed by the comparators and any output with voltages higher than 1.8V are latched OFF. It should be noted that the SCLK pin should be low at both transitions of the CE pin to avoid any false clocking of the shift register. The SCLK input is gated by the CE pin, so that the SCLK pin is ignored whenever the CE pin is high.

FAULT CONDITIONS CHECK

Checking for fault conditions may be done in the following way. Clock in a new control byte. Wait 160 microseconds or so to allow the outputs to settle. Clock in the same control byte and observe the diagnostic data that comes out of the device. The diagnostic bits should be identical to the bits that were first clocked in. Any differences would point to a fault on that output. If the output was programmed ON by clocking in a zero, and a one came back as the diagnostic bit for that output, the output pin was still high and a short circuit or overload condition exists. If the output was programmed OFF by clocking in a one, and a zero came back as the diagnostic bit for that output, nothing had pulled the output pin high and it must be floating, so an open circuit condition exists for that output.

Figure 1 : Byte Timing with Asynchronous Reset.

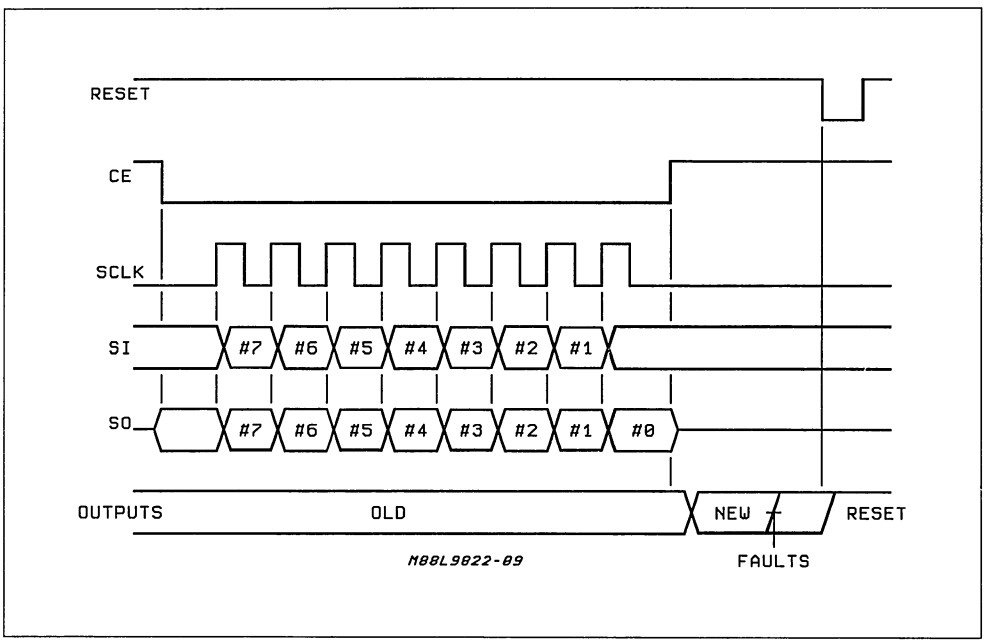


Figure 2 : Timing Diagram.

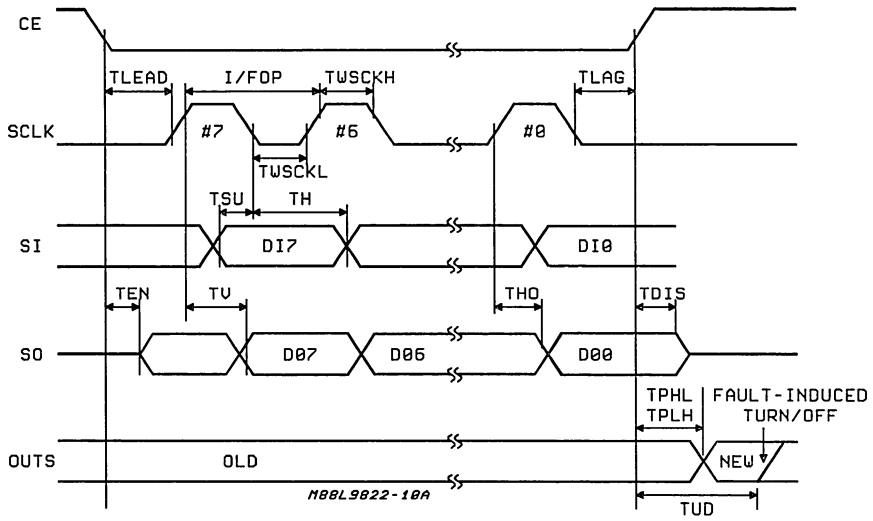
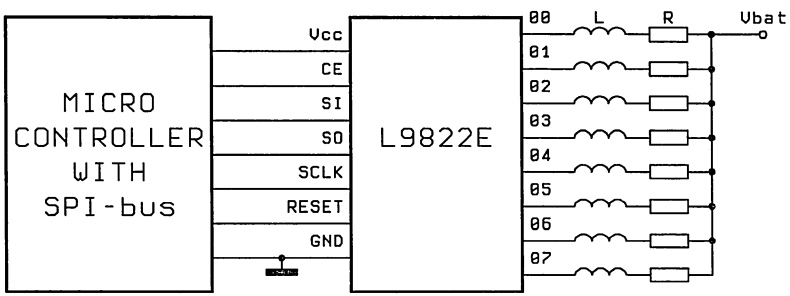


Figure 3 : Typical Application Circuit.



Vcc = 5.0V ± 5%

Vbat= 14.0V ± 0.5V

R = 30Ω ± 5%

L = 10mH ± 10%

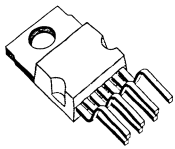
8 LOADS UP TO 0.75A EACH

M92L9822E-03

MONOLITHIC LAMP DIMMER

- HIGH EFFICIENCY DUE TO PWM CONTROL AND POWER DMOS DRIVER
- LOAD CONNECTED TO GROUND
- CURRENT LIMITATION
- OVER AND UNDERVOLTAGE PROTECTION
- ON CHIP THERMAL PROTECTION
- LIMITED AND PROGRAMMABLE OUTPUT VOLTAGE SLEW RATE
- OPEN GROUND PROTECTION
- VERY LOW STANDBY POWER CONSUMPTION
- LOAD DUMP PROTECTION
- MINIMIZED ELECTROMAGNETIC INTERFERENCE
- WIDE CHOICE IN PWM FREQUENCY RANGE
- LOAD POWER LIMITATION

MULTIPOWER BCD TECHNOLOGY

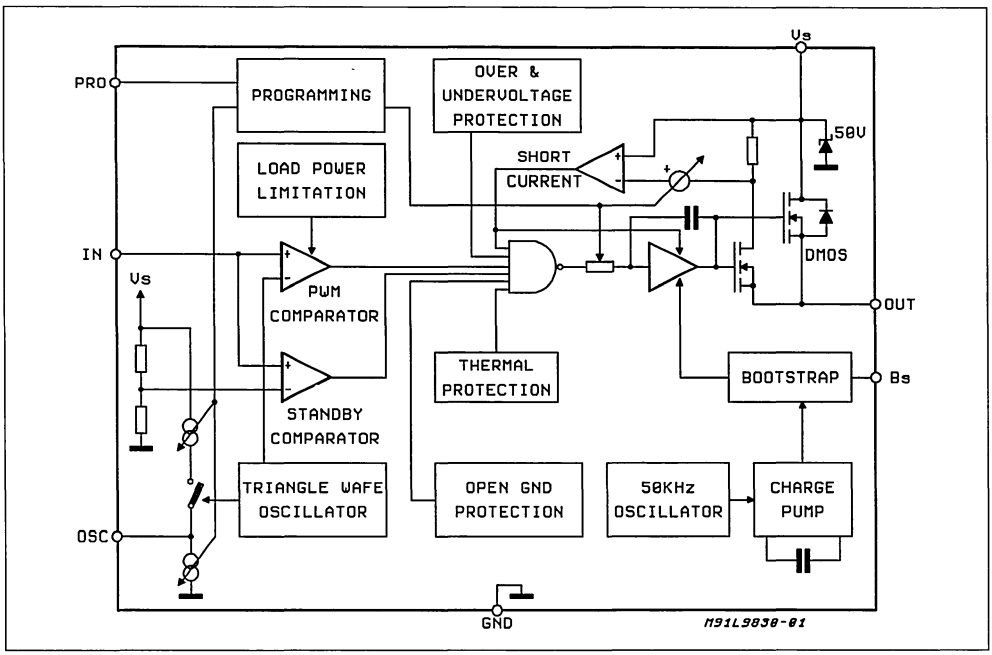


Heptawatt
ORDERING NUMBER: L9830

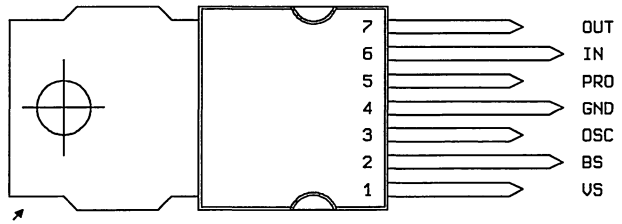
DESCRIPTION

The L9830 high side driver is a monolithic integrated circuit realized with Multipower BCD mixed technology to drive resistive loads in PWM mode with one side connected to ground.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



PIN FUNCTION

PIN	NAME	DESCRIPTION
1	V_S	Common suppy connection also Drain of the power DMOS.
2	BS	A capacitor connected between this pin and the Source of the power DMOS pin Out gives the possibility to bootstrap the gate driving voltage of the power DMOS.
3	OSC	A capacitance CT connected between GND and this terminal determines the PWM switching frequency.
4	GND	Common ground connection.
5	PRO	A resistor connected between this pin and GND provide the possibility to programming the output voltage slew rate, the PWM oscillator frequency and the short current value.
6	IN	Analog input for controlling the PWM ratio, related to V_S.
7	OUT	Source connection of the internal power DMOS.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	60	V
V_{DS}	Drain Source Voltage	60	V
V_{IN}	Input Voltage	-0.3V up to V_S +0.3V	
I_S	Supply Current	±0.2	A
I_{OR}	Output Reverse Current	-2	A
P_{tot}	Power Dissipation at $T_{case} \leq 75°C$	37.5	W
T_{amb}	Operating Ambient Temperature Range	-40 to +85	°C
T_j	Operating Junction Temperature Range	-40 to 150	°C
T_{stg}	Storage Temperature	-65 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	2	°C/W

ELECTRICAL CHARACTERISTICS ($6V \le V_S \le 16V$; $-40°C \le T_{amb} \le 85°C$, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{qo}	Operating Quiescent Current $I_{qo} = 11.3 \frac{V_S - 0.7V}{R_P} + 0.67mA$	$V_{IN} = V_S$ $R_P \rightarrow \infty$ $R_P = 30K\Omega$		2.4 8.5	6 18	mA mA
I_{qs}	Standby Current	$V_{IN} = 0$ $T_j \le 100°C$	0	200	600	µA
V_{INSB}	Input Standby High Threshold V_{IN}/V_S		0.1	0.15	0.2	
$V_{INSBhys}$	Input Standby Hysteresis		-350	-190	-50	mV
V_{INH}	Input High Threshold	$f_o \times t_{on} = 1$ $V_S \le V_{SLPL}$	0.95VS		V_S+0.3V	
I_{IN}	Input Current	$-0.3 \le V_{IN} \le V_S$+0.3V		1	5	µA
V_{SL}	Low Supply Voltage Disable High Threshold		5	5.5	6	V
V_{SLhys}	Low Supply Voltage Disable Hysteresis		-300	-100	-50	mV
V_{SLPL}	Load Power Limitation Start Supply Voltage	$V_{IN} \ge V_{INH}$, $f_{on} \cdot t_{on} = 0.96$	12	13.0	14.5	V
V_{SH}	High Supply Voltage Disable High Threshold		16	17.8	20	V
V_{SHhys}	High Supply Voltage Disable Hysteresis		-350	-190	-50	mV
V_{SLD}	Load Dump Supply Voltage Threshold	$I_q = 50mA$	45	52	55	V
I_{CLD}	Load Dump Clamping Current	VS = 60V	100	150	300	mA
T_{ST}	Thermal Shutdown Temperature		150	175	200	°C
T_{SThys}	Thermal Shutdown Temperature Hysteresis		-50	-40	-30	°C
K_{Ti}	Internal PWM Frequency Constant (without RP)	$f_o = K_{T/CT}$	1000	2000	3000	Hznf
K_{Te}	External PWM Frequency Constant	$f_o = \frac{1}{C_T R_P} K_{Te}$ $30K\Omega \le R_P \le 500K\Omega$	0.220	0.250	0.350	
I_{osi}	Internal Short Current Limitation (without R_P) (4)	$V_S = 12V$	3	6	9	A
I_{ose}	External Programmable Short Current Limit ($30K\Omega \le R_P \le 500K\Omega$) (3)	$V_S = 12V$, $R_P = 125K\Omega$	5	6	10	A
R_{DS}	Static Drain Source on Resistance	$V_S \ge 9V$, $I_O = 1A$		190	380	mΩ
S_i	Internal Fixed Output Voltage Slew Rate (without R_P) (1)	$V_S = 12V$; $5\Omega \le R_L \le 7\Omega$	50	120	230	V/ms
		$T_{amb} \le 25°C$	50	120	250	V/ms
S_e	External Programmable Output Voltage Slew Rate ($30K\Omega \le R_P \le 500K\Omega$) (2)	$V_S = 12V$, $R_P = 125K\Omega$ $R_L = 6\Omega$	50	120	200	V/ms
		$T_{amb} \le 25°C$	50	120	250	V/ms

Notes:

(1) $S_i = VS \ \ 11.16 \frac{1}{ms} - 7\ 26\ V/ms$

(2) $S_e = \frac{R_L}{R_P} \ \frac{VS - 0\ 65V}{R_L + 0\ 32\Omega} \ 1.47 \ \ 10^6 \frac{V}{msA}$

(3) $I_{OSP} = (VS - 0\ 6V) \ \frac{64260}{R_P}$

(4) $I_{OS} = (VS - 0.6V) \ \ 0\ 514 \ \frac{A}{V}$

If R_P is not present in application an internal equivalent resistor can be inserted in the calculation with a typical value of $R_P = 125K\Omega$

FUNCTIONAL DESCRIPTION

To control the power of the load with a POWERMOS transistor in the switched mode, its gate must be driven with a PWM signal. The amplitude of the gate driving pulse must guarantee that the Power DMOS transistor will be completely saturated during the ON phase. To generate the necessary gate driving voltage a charge pump circuit is required. With this circuit a gate voltage of $2 \cdot (V_S - 1.5V) \leq VS + 16V$ typically will be obtained.

The slope of the leading and trailing edge of the gate driving pulse is defined with an internal capacitor. The important criteria for the dimensioning of the output voltage slope are the electromagnetic radiation and the power dissipation of the Power DMOS. The typical value of the output pulse slope is in the range of 120V/ms to fullfill automotive radiation requirements.

The output pulse slope is directly related to the value of the supply voltage VS and in a wide range programmable through the programming resistance R_P.

$$S = \frac{dV_{out}}{dt} = R_L \cdot \frac{dI_{load}}{dt} = \frac{R_L}{R_P} \cdot \frac{VS - 0\,65V}{R_L + 0\,32\Omega} \cdot 1.47 \frac{10^6\,V}{Ams}$$

The value of the gate voltage slope due to the POWERMOS parasitic capacitors must be in a relation to the charge pump performance. For fast gate voltage variation the bootstrap option can be used. The bootstrap capacitance should have a relation greater than 50 to the DMOS parasitic capacitors and should be in the range of

$$C_{BS} \geq 100nF$$

The switching frequency "f_O" is defined with a triangle oscillator and it's programmed with the capacitor C_T, or C_T and R_P if a greater precision is required.

$$f_O = K_T/C_T \text{ (without } R_P)$$

$$f_O = \frac{1}{4C_T R_P} \text{ (with } R_P)$$

The modulation factor of the PWM driving signal of the external Power DMOS transistor is defined with the voltage level at the analog input. Fig. 1 shows the typical transfer curve giving the PWM factor as a function of the input/supply voltage ratio.

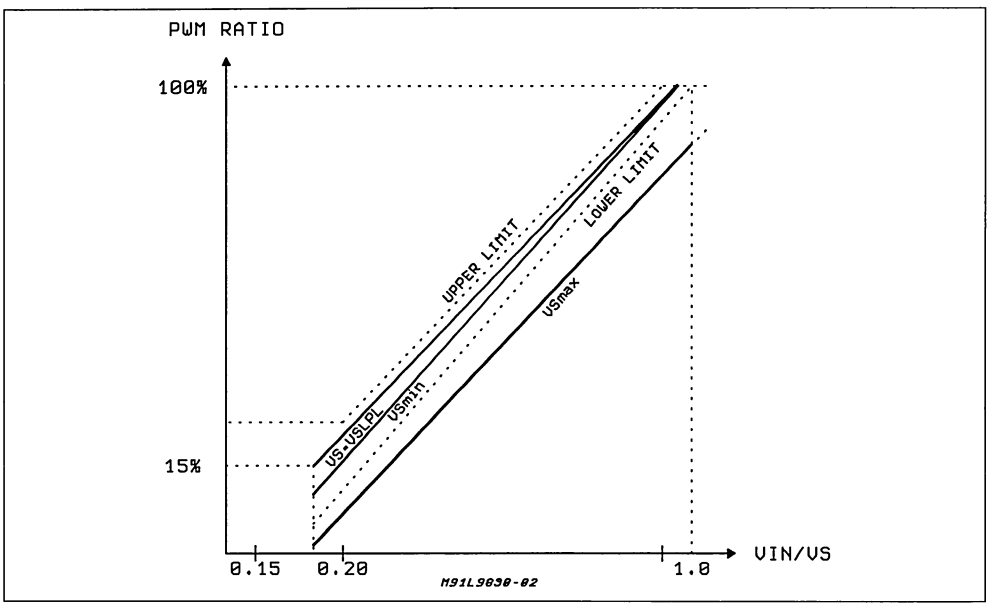
For higher supply voltage values, the power limitation circuitry will linearly reduce the PWM ratio to achive a constant load power to extend the lamps life time.

The input voltage is referred to the supply voltage. The regulation of the PWM factor can be realized with a potentiometer connected to the supply voltage and the analog input, see the typical application circuit diagram.

The maximum load current in the short circuit condition is limited internally with a sense DMOS cell.

The value of the short current is a multiple of the programming current flowing through R_P or the in-

Figure 1: Transfer Characteristc



ternal fixed resistance. Threfore this short current value is supply voltage dependent to achieve in any condition the lamp required warm up current which will be normally two or three times higher.

$$I_{OSe} = \frac{VS - 0.6V}{R_P} \cdot 64260$$

If the short current condition is detected the gate will be driven with a DC voltage which value is regulated to maintain the specified current. With this function the switch ON phase for each load will be speeded up.

The circuit features also a protection which allows to withstand high overvoltage for a limited time (load dump in automotive application). Above the VS_H threshold the gate driving of the POWERMOS transistor is switched OFF and the gate is held at the GND potential. When the V_{BAT} rises above the internal supply clamp voltage VS_{LD} the clamping diode becomes active with a serial resistance of R_{LD} and the gate voltage is floating with the GND potential. At this time the current flowing through the load is not limited. In this condition the load voltage can be calculated to

$$V_L = VS = VS_{LD} - VS_{GS} \qquad V_{GS} << VS_{LD}$$

This device is protected against temperature destruction through an internal power dissipation protection. The total power dissipation of the device can be calculated with:

for $VS_L \leq VS \leq VS_{LPL}$:

$$P_{tot} = VS^2 \cdot \left(\frac{R_{DS}}{(R_{DS} + R_L)^2} + \frac{f_O}{S} \cdot \left(1 - \frac{R_{DS}}{R_{DS} + R_L}\right) \cdot \left(1 - \frac{R_{DS}}{R_{DS} + R_L}\right) \cdot \left(1 + \frac{2VS}{R_{DS} + R_L}\right) \right)$$

and for $VS_{LPL} \leq VS \leq VS_H$:

$$P_{tot} = V^2_{SLPL} \cdot \frac{R_{DS}}{(R_{DS} + R_L)} + \frac{VS^2 \, f_O}{S} \cdot \left(1 - \frac{R_{ON}{}^2}{R_{ON} + R_L}\right)$$

Figure 2: Total Power Dissipation Characteristic

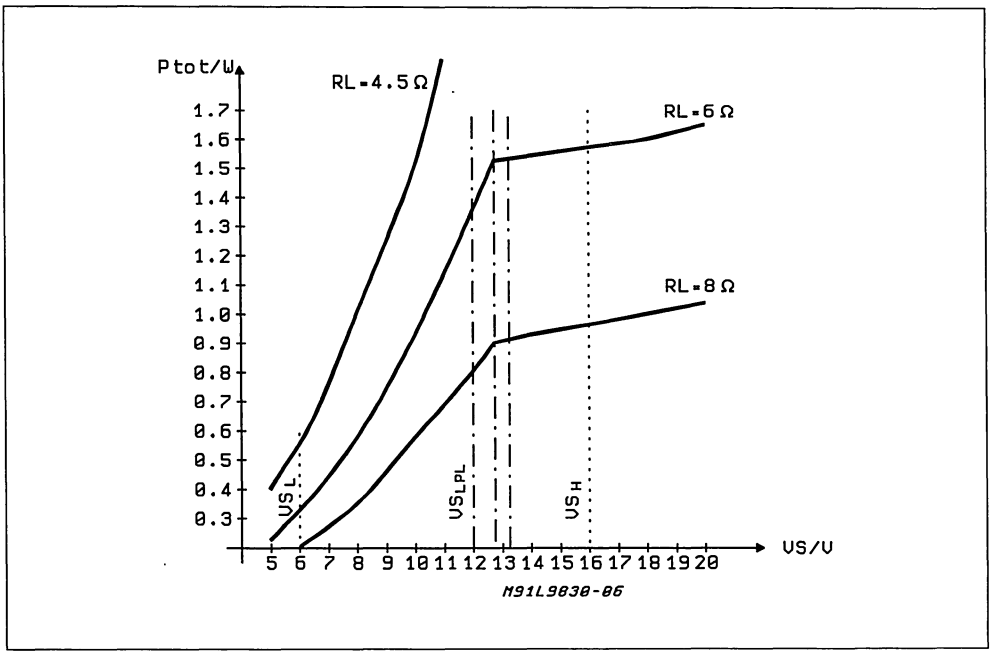
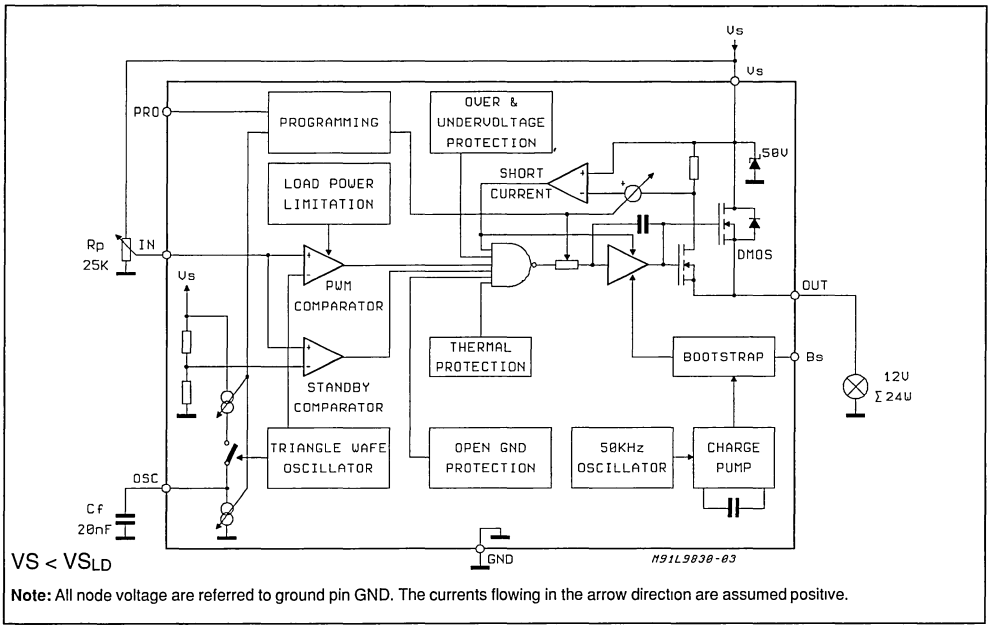
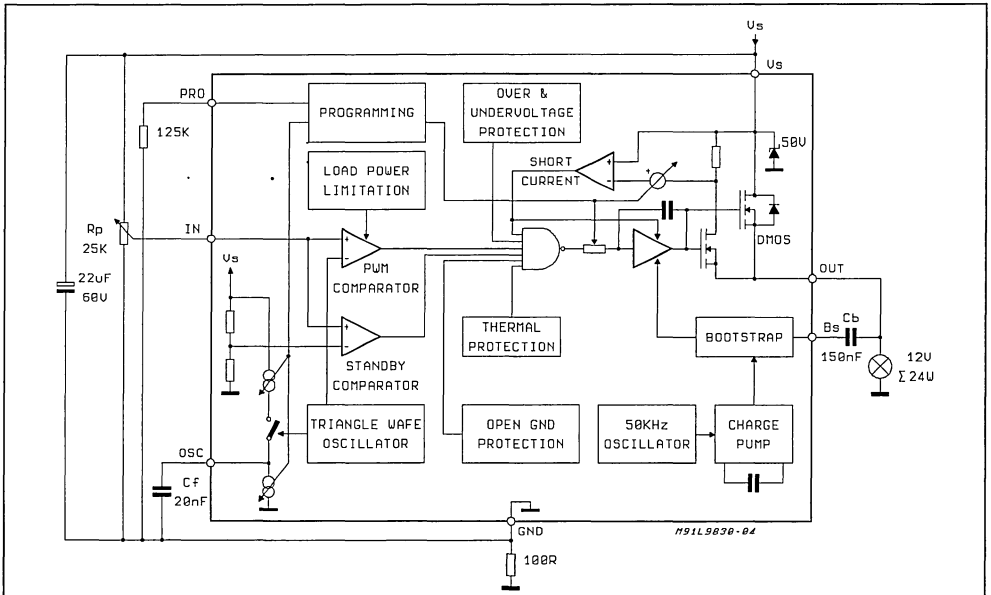


Figure 3: Application Circuit Diagram for Dashboard Dimming



Note: All node voltage are referred to ground pin GND. The currents flowing in the arrow direction are assumed positive.

Figure 4: Application Circuit Diagram for Dashboard Dimming with Optimized Device Power Dissipation



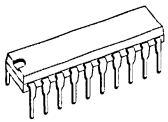
Note: All node voltage are referred to ground pin GND. The currents flowing in the arrow direction are assumed positive.

OCTAL PARALLEL LOW SIDE DRIVER

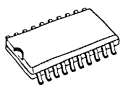
ADVANCE DATA

- OPERATING DC SUPPLY VOLTAGE RANGE 5V TO 25V
- SUPPLY OVERVOLTAGE PULSE UP TO 40V
- VERY LOW STANDBY QUIESCENT CURRENT 100µA
- EIGHT BIT PARALLEL STRUCTURE WITH MEMORY FEATURE
- BIDIRECTIONAL INPUTS-OUTPUTS
- µC COMPATIBLE INPUT LEVELS WITH THRESHOLD HYSTERESIS
- INTERNAL 4.5V REFERENCE DEFINING THE OUTPUT HIGH LEVELS
- EIGHT HIGH CURRENT OUTPUTS FOR DC CURRENTS UP TO 350mA WITH ON RESISTANCE LESS THAN 3Ω (typ. 1,5Ω)
- OUTPUT SHORT CIRCUIT PROTECTION WITH TIME DELAY CHARACTERISTICS FOR DRIVING LAMPS
- THERMAL OVERLOAD PROTECTION

MULTIPOWER BCD TECHNOLOGY



DIP-20 Plastic



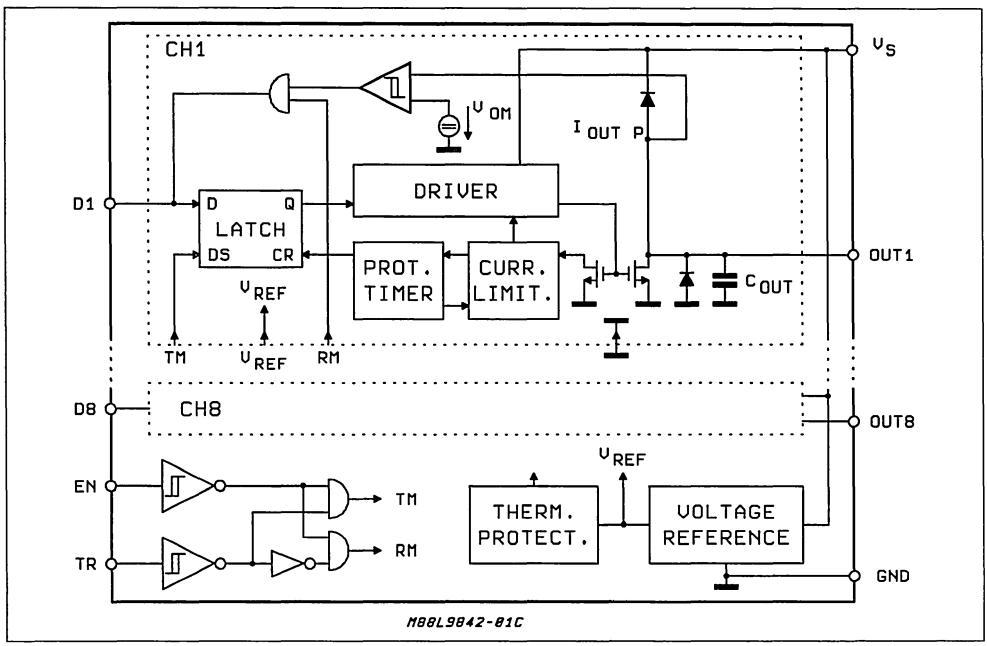
SO-20L

ORDERING NUMBERS : L9842N (DIP-20)
L9842ND (SO-20L)

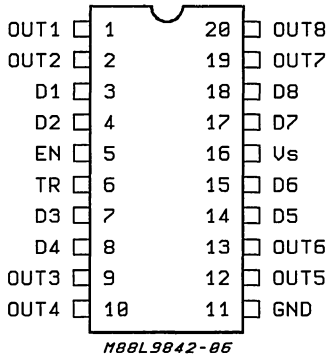
DESCRIPTION

The L9842 is an octal parallel input power interface circuit in the Multipower BCD technology with bidirectional inputs and outputs and the output status monitoring.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	40	V
V_{OUT}	Output Voltage	Int. Clamped to Vs	
dV_{OUT}/dt	Output Voltage Transient	100	V/µs
$I_{OUT\ DC}$	DC Output Current	±350	mA
$I_{OUT\ P}$ (*)	Peak Output Current ($T/t_p \geq 100$, t_p = 4ms)	±2	A
I_S	DC Current at V_S	– 1.5	A
$V_{D\ IN}$	Input Voltage	– 0.3 to 7 (**)	V
V_{EN}	Enable Input Voltage	– 0.3 to 7 (**)	V
V_{TR}	Transfer Input Voltage	– 0.3 to 7 (**)	V
T_j	Operating Junction Temperature	– 40 to 150	°C
T_{stg}	Storage Temperature	– 65 to 150	°C
P_{max}	Power Dissipation (T_{amb} = 80°C) DIP-20 SO-20	875 420	mW mW

(*) Schaffner pulses type 1 and 2
(**) For V_S < 6 7V the device can be supplied through the internal ESD diodes from inputs to V_S

THERMAL DATA

Symbol	Parameter		DIP20	SO20
Rth j-amb	Thermal Resistance Junction-ambient	Max.	80°C/W	165°C/W
$T_{j\ MAX}$	Maximum Junction Temperature		150°C/W	150°C/W

ELECTRICAL CHARACTERISTICS ($5V \le V_S \le 25V$ (40V @ $t < 400ms$), $-40°C \le T_j \le 125°C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DINL} V_{DINH}	Input Voltage LOW Input Voltage HIGH	V_E = L, V_{TR} = L (input-mode) [1] V_E = L, V_{TR} = H (output-mode) [1]	0 3.0		1.0 7.0	V V
V_{DOUTL} V_{DOUTH}	Output Voltage LOW Output Voltage HIGH	V_E = L, V_{TR} = H (output-mode) [1]	 4.0		0.4 5.0	V V
I_{DIN}	Input Current	V_E = L, V_{TR} = L (input-mode) [1]	− 10		10	µA
V_{ENL}	Enable Voltage LOW		0		1.0	V
V_{ENH}	Enable Voltage HIGH		3.0		7.0	V
V_{TRL}	Transfer Voltage LOW		0		1.0	V
V_{TRH}	Transfer Voltage HIGH		3.0		7.0	V
$I_{EN\,TR}$	Enable, Transfer Input Current	$0 < V_{E\,TR} < 5V$	− 1		1	µA
V_{EHY}	Enable Threshold Hysteresis		50			mV
V_{THY}	Transfer Threshold Hysteresis		50			mV
R_{OUT}	Output Resistance R_{OUT}-characteristic See fig. 2	Out = L $0 < I_{OUT} \le 350mA$ $V_S \ge 8V$ V_S = 6.5V V_S = 5.0V		1.5	 3.0 25 1	 Ω Ω KΩ
I_{SC}	Output Short Current I_{OUTSC}-characteristic See fig. 3	$8V \le V_S = V_{out} \le 25V$ T_{SCH} = 1.25ms T_{SCL} = 20ms	 0.8 0.36	 1.5 0.65	 2.5 1.5	 A A
V_{OUT}	Output Voltage	Out = H I_{OUT} = 0.35A (DC) I_{OUT} = 1A (pulsed)	 V_S + 0.5 V_S + 2.0		 V_S + 2 V_S + 4	 V V
ΣI_{OUTL1}	Output Leakage Current per Channel	Out = H, $-40 \le T_j \le 85°C$ V_{OUT} = 16V			100	µA
C_{OUT}	Output Capacitance	Out = H, V_{OUT} = 5V V_{OUT} = 15V	 60 30	 90 60	 120 90	 pF pF
I_Q	Quiescent Current STANDBY MODE TRANSFER-, HOLD MODE READ MODE	$5V \le V_S \le 16V$; I_{DOUT} = 0 $-40 \le T_j \le 85°C$ V_E = H, V_{TR} = H V_{TR} = L V_E = L, V_{TR} = H			 100 200 400	 µA µA µA
I_Q	Quiescent Current	V_S = 25V V_S = 40V @ $t \le 400ms$		 20	2 35	mA mA
I_{SCOP}	Additional Short Circuit Operating Current Per Channel	V_{EN} = L, V_{DIN} = L V_{TR} = L, $I_{OUT} = I_{SC}$			 I_O +500	 µA
V_{OM}	Output Monitor Threshold		2.5		3.5	V
T_{SCH} (2)	Duration of High Short Current Limiting	$I_{OUT} = I_{SCH}$	1.25	2.5	3.75	ms
T_{SCL} (2)	Duration of Low Short Current Limiting	$I_{OUT} = I_{SCL}$	20	40	60	ms

Note : 1. V_D are bidirectional data inputs or outputs depending on the V_E, V_{TR} status.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_n ON	ON-delay Time (5)	See fig. 1 R_L = 1KΩ			10	ms
t_n OFF (3)	OFF-delay Time (5)				10	µs
t_s ON	ON-delay Time (6)			20	100	µs
t_s OFF (3)	OFF-delay Time (6)			20	40	µs
t_D ON	Data ON - Delay Time (7)			2	10	µs
t_D OFF (3)	Data OFF - Delay Time (7)			2	10	µs
t_{ON}-t_{OFF}	Delay Time Difference	Except STANDBY MODE			4	µs
t_f	Filter Time (8)		0.7	2	4	µs

Notes : 2. If the output current exceeds the high short current threshold I_{SCH} an internal timer is started. If after the time period of T_{SCH} + T_{SCL} the current limiting is still active the overload condition is recognized and this output is switched off (in any case). To restart the output the transfer mode (TM) has to be chosen and the corresponding input voltage V_{DIN} must become HIGH to reset the internal overload latch

3. Because the output capacitance is the drain-source capacitance of the power switch the risetime of the outputs depends of the used supply voltage V_S, the load resistor R_L and the output capacitance C_{OUT} and can be calculated with the following equation :
$T_d = \tau$ ln 10 (reaching 90% of V_S) $\tau = R_L \times C_{OUT} \times K$ (4) K = 1.5
This additional delay time T_d must be added to t_{OFF}.

4. Because the drain source capacitance of the output transistor is voltage dependent, it is necessary to multiply C_{OUT} (specified at the maximum V_{OUT}) with a correction factor K to obtain the average output capacitance C_{OUT}.

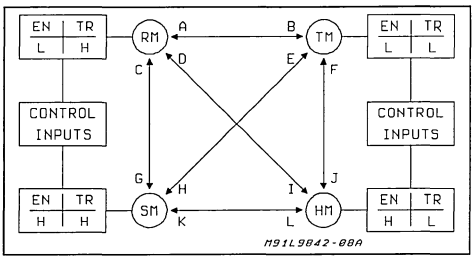
5. Delay time between all modes except STANDBY MODE.

6. Delay time between STANDBY MODE and any other mode and vice versa.

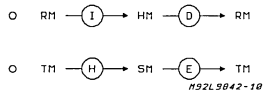
7. Data delay time when TRANSFER MODE is chosen.

8. Explanation see page 6

MODE CHANGE DIAGRAM

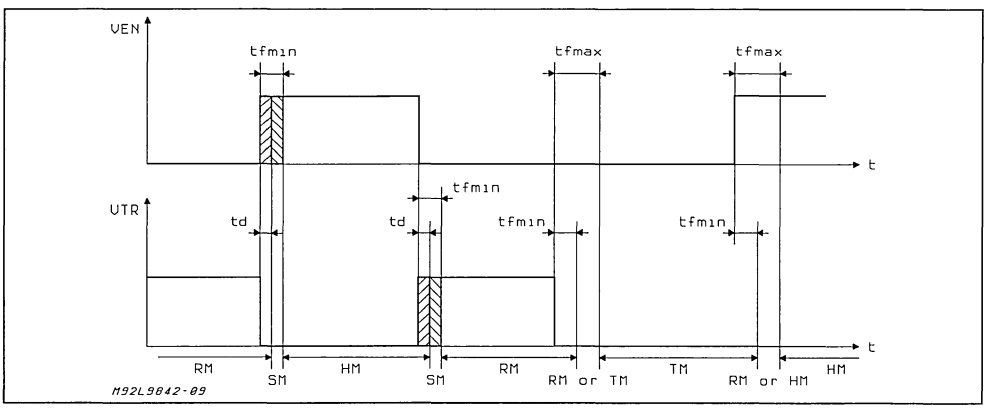


- Critical mode variations occur when both mode inputs change their state simultaneously. This is represented by the diagonal arrows in the mode change diagram.



- To avoid that a filter is implemented in the TM signal path. A suitable filter time t_f is chosen to be well beyond the mode comparator delays.

FILTERING TIMING



- As a consequence of the filter function the following features are given respectively has to be considered (refer to timing above):
- For a delay between RM and HM up to $t_d < t_{min}$ the parasitic TM will be supressed.
- To obtain the transfer function surely both mode inputs be "Low" for at least t_{TM} t_{fmax}.
- Therefore the change from TM to any other mode causes an additional delay t_f that is the internal filter time.
- The parasitic SM time is too short to influence the outputs and is hence negligible.

TRUTH TABLE FOR THE CONTROL INPUTS

Enable V_E	Transfer V_{TR}	Mode Symbol	Function Mode
L	H	RM	READ MODE (output monitoring)
L	L	TM	TRANSFER MODE (input data transferred to output)
H	L	HM	HOLD MODE (output corresponds to the data latch)
H	H	SM	STANDBY MODE (all outputs open)

Figure 1 : Timing Diagram with Function Modes.

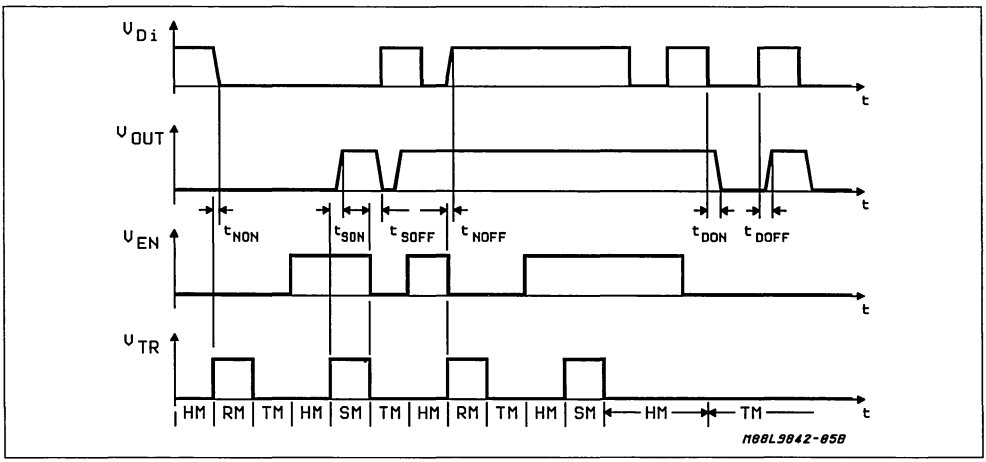


Figure 2 : Maximum R_{OUT} - Characteristics.

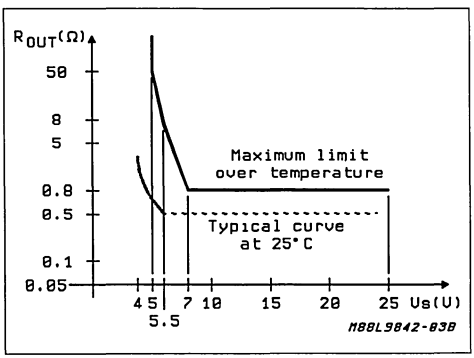


Figure 3 : Typical Short Current Characteristics.

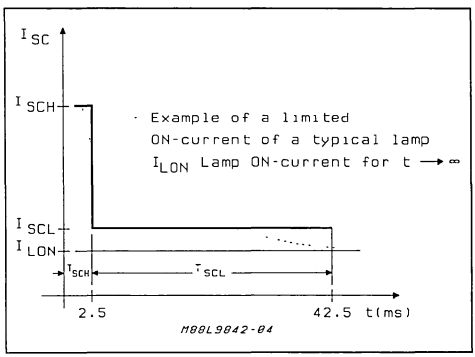
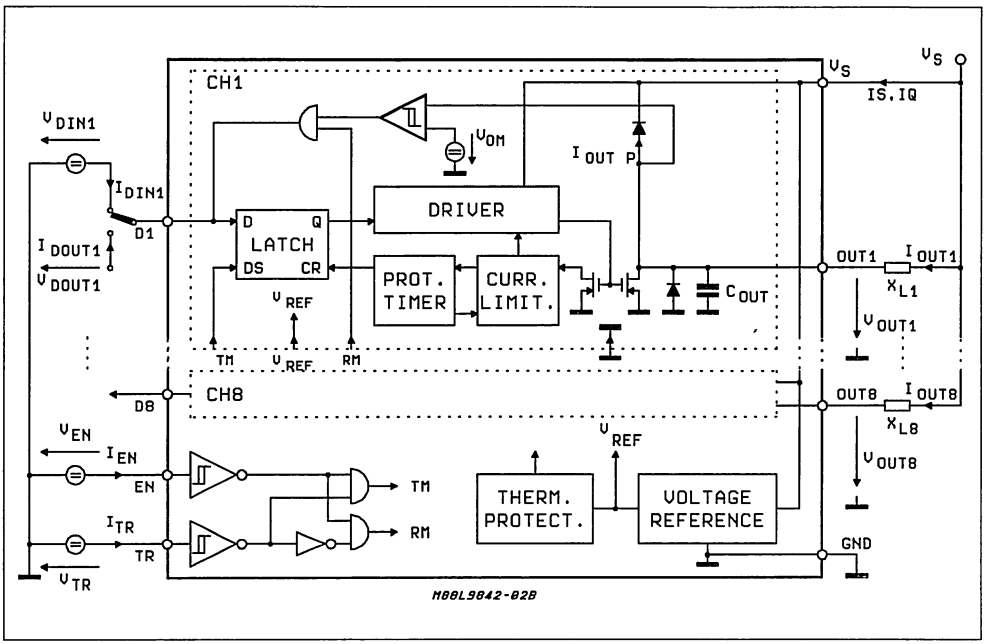


Figure 4 : Test Circuit.



FUNCTIONAL DESCRIPTIONS

This device was developed specially for automotive applications to drive different loads like relais, lamps, data buses or actuators with very low current consumption.

The L9842 contains eight identical channels each with a separate DATA input/output and the power output. In each channel the memory function, the output short circuit function and the diagnostic function is realized.

The common part determines the function modes through ENABLE and TRANSFER inputs whereas the reference part biases all current sources and generates the threshold voltages and the stabilized supply voltage for the whole CMOS-logic.

A special thermal protection, ESD-protected inputs/DATA pins and a particular output short circuit characteristic prevent a damage or the destruction of the device.

Referring to the block diagram it can be seen that each channel works independent and contains all necessary functions described in the following points.

OUTPUT BLOCK

TRANSFER FROM DATA INPUT TO POWER OUTPUT.

The DATA pins are used bidirectionally. The main path is the non inverting transfer of a digital signal from the DATA pin to the power output (TRANSFER MODE). The data pass the input latch that works also as a memory in the HOLD MODE. They remain stored until the TRANSFER MODE is selected to write in new data.

This means that in all other modes the memory content will not be changed except the output short circuit protection was active more than the check time of 42.5ms. In this case in all modes the storage flip-flop will be set to hold the output for protection into the Off-state. By activating the READ MODE in this position it is possible to detect short-circuit load.

To switch on the output again, the external control processor has to select the TRANSFER MODE and to change the input signal at the corresponding data terminal to HIGH to set the storage flip-flop and then to write in LOW. An additional reading of this channel output (selecting the READ MODE after the mentioned check time) shows whether the short-circuit is still present.

TRANSFER FROM POWER OUTPUT TO DATA OUTPUT.

The opposite signal path (READING MODE) from the output to the DATA terminals is used for the diagnostic function to monitor the output status. Output voltages greater than 3.5V lead to "HIGH" state at the DATA terminals. The HIGH level is typical 4.5V and internally stabilized. For "LOW" level the saturation voltage of N-Channel MOS transistor is relevant.

SHORT-CIRCUIT PROTECTION.

For the use of lamps a particular short-current characteristic is implemented and it is drawn in fig. 3. Because of the low resistance of lamps during the ON-phase the current limit is for typical 2.5ms about the double as for the second current limiting phase. Detecting a short circuit condition means that the channel output remains low in any condition for the check time $T_{CH} = T_{TSCH} + T_{SCL}$ independent of the status of the inputs.

These time periods are generated from two frequencies 400Hz/6.4kHz coming from the common oscillator part. If the current limiting is active after the check period an overload is recognized and the regarding channel is switched off and the DATA flip-flop is also reset as explained earlier.

In order to save supply current a special short-circuit protection is used that needs no quiescent current during the ON-state as long as no overload is present at the output. Because of this special circuit configuration the output current must exceed a given threshold to activate the current regulation loop.

This current threshold I_{TH} is determined by the ON-resistance R_{DSON} of the output DMOS and the minimum operating supply voltage V_{Smin} of the limiting circuit and can be easily calculated in the following way :

$I_{TH} = V_{Smin}/R_{DSON} = 4V/1.5\Omega = \underline{2.7A}$ (typical value at $T_j = 25°C$)

When the output is shorted for instance to V_S a maximum peak current will occur for a short duration up to the limiting circuit is switched on and the settling time is over. Under worst case conditions ($T_j = -40°C$), $V_S = 16V$, where R_{DSON} is lowest) the peak current can reach 7A with a duration of 1µs at V_{out} = 15V and 4A with a duration of 20µs at V_{out} = 5V.

COMMON PARTS

MODE CONTROL.

By the "TRANSFER" and "ENABLE" input, working modes can be selected as shown in the truthtable in the upper part of fig. 1. The control signals coming from both input comparators which determine the logic threshold and hysteresis drive the mode logic that distributes the right data to all output blocks.

TRANSFER, HOLD and READ MODE are explained before. The remaining STANDBY MODE switches the clock oscillator and all outputs off and reduce the quiescent current below 100µA. This means that only the both mode comparators and the bandgap regulator are active. The input data stored before will be not changed.

OSCILLATOR PART.

The clock oscillator contains an on-chip capacitor and requires therefore no external components. The oscillation frequency is approximately in the range of 50kHz. This oscillator signal is devided by a 7 bit-counter which creates the two frequencies for the timing of all short current control circuits in each output block.

VOLTAGE REFERENCE.

The main reference cell is a bandgap controlled very low drop voltage regulator. All threshold voltages for the input comparators, the diagnostic comparators and the thermal overload comparators as well as the reference voltage for the CMOS supply buffers are derived from one resistor devider.

Because of the low current capability of the regulator two buffers are used to supply the CMOS logic for every four channels. These voltage followers work like a current multiplier at a very low quiescent current. A clamping circuit prevents that the CMOS breakdown voltage will be reached.

CURRENT REFERENCE + POWER–ON RESET.

The two temperature compensated current lines are generated directly from the bandgap voltage and are switched off by the mode logic to save supply current. A third unswitched current line biases the input comparators and CMOS buffers.

During supply voltage rise, power-on reset circuit provides a defined status of all latches in the CMOS logic. From a supply voltage of about 4V on it enables the whole logic and the device can work. Below 4V all latches are set to hold the outputs into the OFF state.

PROTECTION CIRCUITS

ESD–PROTECTION.

Both input comparators (ENABLE, TRANSFER) are ESD protected and include zener diodes that clamp the gates of the internal MOSFETs to minimal 15V. Second diodes clamp these inputs to V_S if the supply voltage is lower than 0.6V below the zener voltage.

The eight "DATA" terminals has the same ESD protection structure as the comparator inputs.

SHORT CURRENT LIMITING.

The detailed function explanation is given in a former section where the output block is described. Generally it can be supplementary said that this kind of protection determines the limits within the safe operating area of the used DMOS structure.

The big chip area and the heat capacity of silicon allow for short durations peak currents up to five times the maximum DC current that occur under certain conditions as expounded above.

THERMAL SHUTDOWN.

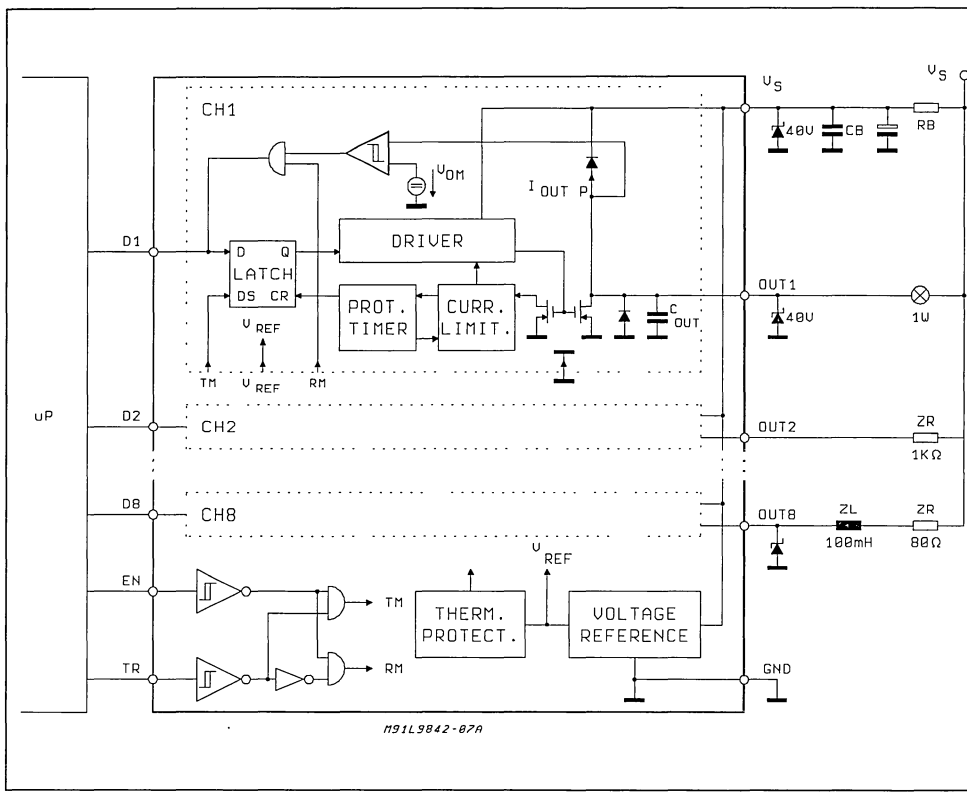
Because of the symmetry and the big size of chip two thermal overload protection circuits were placed on each side of the chip where the output structures are concentrated to ensure minimum thermal gradients to the thermal sensors.

At a chip temperature of about 160°C the device is switched OFF. This state is similar to the STANDBY MODE. After the temperature remains under approximately 135°C the element is switched ON. Thermal shut-down does not influence any logic because it switches only the gates of all output DMOS-transistors directly to ground.

APPLICATION HINTS

- Precausions by external components must be provided to avoid damage of the device (it's in any case not allowed to exceed the maximum ratings given on page 2).
- For open load detection it is recommended to use external components to fix the desired status (depending on the temperature the internal open load status can vary from "H" to "L" caused by leakage currents)

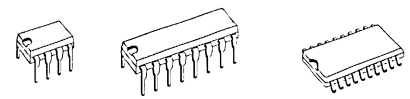
Figure 5: Application Diagram



MOTOR BRIDGE FOR HEADLIGHT ADJUSTMENT

PRODUCT PREVIEW

- FULL BRIDGE OUTPUT CONFIGURATION WITH LOW SATURATION VOLTAGE, LESS THAN 3.6V AT OUTPUT CURRENT 1A.
- OPERATING SUPPLY VOLTAGE RANGE 7V TO 18V, SUPPLY OVERVOLTAGE UP TO 50V.
- HIGH POSITIONING PRECISION AND HIGH NOISE IMMUNITY DUE TO TRANSFER CHARACTERISTIC WITH DIFFERENT POSITIONING AND NOISE IMMUNITY RANGES.
- FAST STOP THROUGH SHORT-CIRCUITING THE MOTOR.
- MOTOR STOP STATUS IN CASE OF OPEN INPUT CONDITION.
- SUPPLY OVERVOLTAGE PROTECTION FUNCTION FOR V_S MORE THAN 18V, UP TO 50V.
- INPUT PROTECTION AGAINST TRANSIENTS ON THE BATTERY LINE AND THE THE REVERSE BATTERY CONDITION.
- OUTPUT SHORT CIRCUIT PROTECTION DUE TO OUTPUT CURRENT LIMITING
- THERMAL OVERLOAD PROTECTION



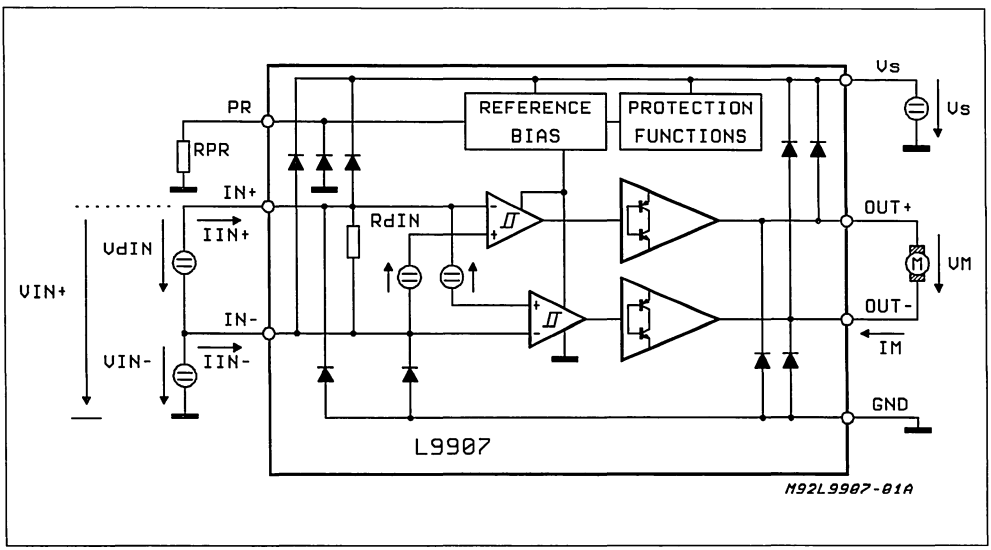
Minidip **Powerdip (12+2+2)** **SO20L(12+4+4)**

ORDERING NUMBER: L9907

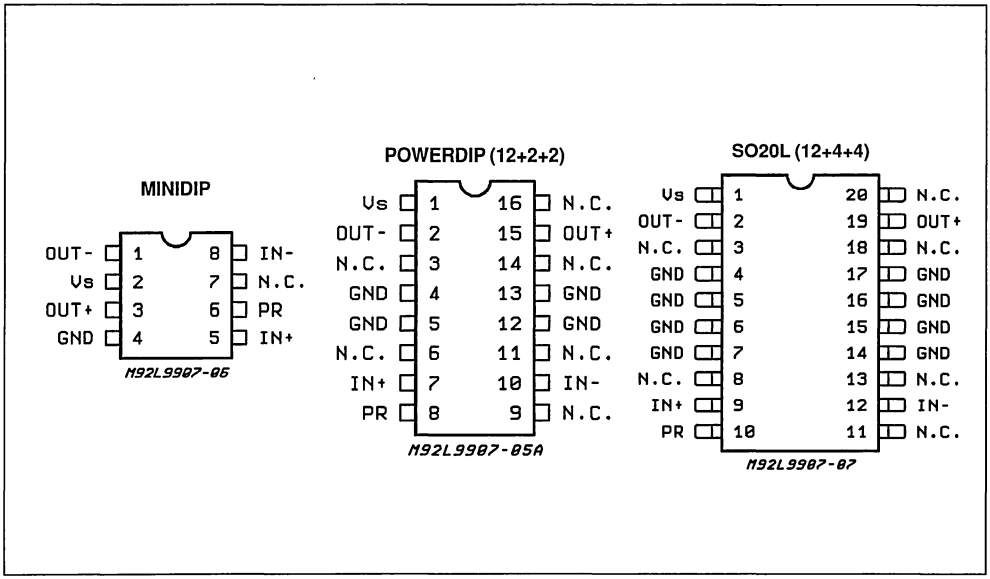
DESCRIPTION

The L9907 is a monolithic integrated power comparator with full bridge output configuration, intended for driving DC motors in positioning systems, optimized for headlight adjustment application and respecting the automotive electronics enviromental conditions.

BLOCK DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{SDC}	DC Supply Voltage	26	V
V_{SP}	Supply Voltage Pulse ($T \leq 400ms$)	50	V
I_{OUT}	DC Output Current Output Current Pulsed (100ms)	±0.5 Internally limited	A
I_{IN}	DC Input Current Input Current Pulse (2ms)	±10 ±40	mA mA

THERMAL DATA

Symbol	Parameter	SO20L (12+4+4)	Powerdip (12+2+2)	Minidip	Unit
$Rth_{j\text{-}amb}$ $Rth_{j\text{-}pins}$	Thermal resistance Junction-ambient 1) Thermal Resistance junction-pins	50 15	70 15	100 –	°C/W °C/W
T_S	Thermal Shutdown Junction Temperature		165		°C

1) with 6cm^2 on board heat sink area.

ELECTRICAL CHARACTERISTICS (7V ≤ V_S ≤ 18V, unless otherwise specified.)

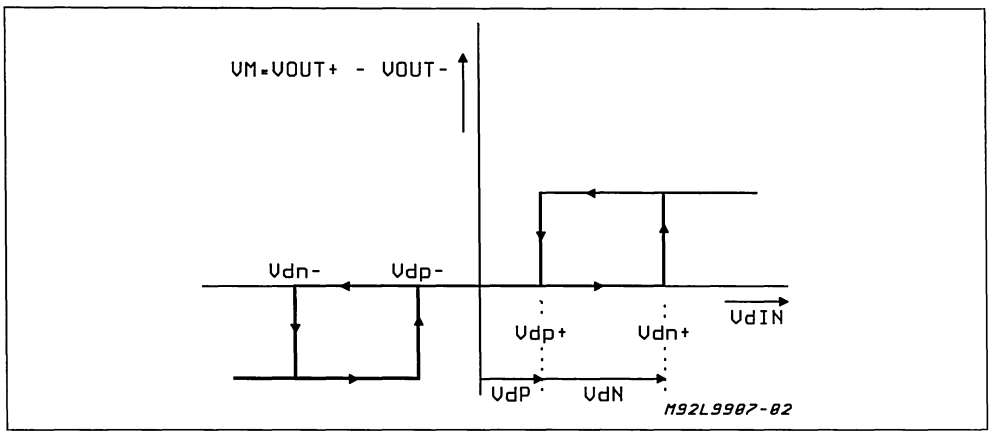
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_q	Quiescent Current	I_O = 0, (Output Open) V_{dIN} < 20mV (stop) V_{dIN} < 200mV (L or R)			 7 3	 mA mA
V_{dP-} V_{dP+}	Differential Input Voltage Positioning Thresholds (2)	0.5 < V_I < V_S -1.5V R_{PR} = ∞ R_{PR} = 0 R_{PR} = ∞ R_{PR} = 0	 – 50 – 100 20 40	 – 35 – 70 35 70	 – 20 – 40 50 50	 mV mV mV mV
V_{dN-} V_{dN+}	Differential Input Voltage Noise Immunity Thresholds	0.5 < VI < V_S -1.5V R_{PR} = ∞ R_{PR} = 0 R_{PR} = ∞ R_{PR} = 0	 $4V_{dP-}$ $4V_{dP-}$ $3V_{dP+}$ $3V_{dP+}$	 – 120 – 240 120 240	 3VdP- $3V_{dP-}$ $4V_{dP+}$ $4V_{dP+}$	 mV mV mV mV
I_{IN}	Input Bias Current	0.5 < V_I < V_S -1.5V V_{dIN} = 0 V_{dIN} = ± 200mV		 0.5 12	 2.5 40	 µA µA
R_{dIN}	Differental Input Resistance	0.5 < V_I < V_S -1.5V V_{dIN} = ± 200mV	16	25	40	kΩ
V_{OSI}	Output Saturation Voltage/ Sink Stage	I_O = 1A I_O = 0.4A		1.1 0.8	1.5 (3) 1.1	V V
V_{OSO}	Output Saturation Voltage/ Source Stage	IO = 1A I_O = 0.4A		1.6 0.9	2.1 (3) 1.4	V V

(2) With programming resistor R_{PR} between the PR pin and GND the thresholds can be adjusted from the nominal value (R_{PR} = ∞, pin PR open) up to two times the nominal value (R_{PR} = 0, pin PR shorted to GND).

The formula defining V_{dP-}, V_{dP+} typical value as a function of R_{PR} is: $-V_{dP-}(R_{PR}) = V_{dP+}(R_{PR}) = 70mV \dfrac{1+\frac{R_{PR}}{9.5K\Omega}}{1+2\frac{R_{PR}}{9.5K\Omega}}$

(3) The maximum value of the sum of the saturation voltages V_{OSI} (0.7A) + V_{OSO} (0.7A) ≤ 2.5V is the design target.

Figure 1: L9907 Differential Input to Output Transfer Charateristic.



FUNCTIONAL DESCRIPTION

The L9907 is a power comparator with full-bridge push-pull outputs, intended for driving a DC motor in the headlight adjustment system. The basical function of the device is shown in the input-output transfer characteristic, Fig. 1.

For differential input voltage VdIN lower than Vdn- the output voltage is negative (corresponds to motor direction right), for increasing input voltage, this status changes to the zero output voltage (motor is actively braked), when the differential input voltage reaches the positioning threshold V_{dp-}. The output status remains in this condition as long as the differential input voltage remains between the noise immunity range thresholds, V_{dn-} and V_{dn+}. If the input voltage increases above the similar behaviour is obtained for decreasing the input voltage and crossing the V_{dp+} and V_{dn-} thresholds. The possible output status transitions are marked with the arrows showing the corresponding direction of the output status variation.

The above described behaviour assures the positioning precision Vdp, corresponding to the Vdp- and Vdp+ thresholds and the noise immunity in the adjusted condition Vdn corresponding to the noise amplitude of Vdn - Vdp imposed on the input control or input feedback signal. Due to this feature the motor starts to move to a new position according to a new value of the input control signal first when the difference of the input control signal to the input feedback signal becomes higher than max $\pm (V_{dn+} - V_{dp-})$ and min $\pm (V_{dn+} - V_{dp+})$. These values are considered as limits of the noise immunity range.

The stop position of the motor corresponds on the input control to input feedback signal difference and can be within the range Vdp- to Vdp+. This ramnge is considered as positioning precision range.

Both the above described positioning and noise immunity ranges are defined refering to IN+, IN- pins and can be affected with the voltage drop over the input signals source resistance R_{IN+}, R_{IN-} due to the input bias currents I_{N+}, I_{N-}.

The above mentioned resistors R_{IN+}, R_{IN-} shown the application circuit diagram, Fig. 2 or the equivalent input source resistance in the application circuit diagram Fig. 3 are necessary for the input current limitation during the transients on the V_{BAT} line. The input source resistors must be dimensioned so that in case of a line transients the input current in the input pin, clamped with the internal input protection diodes do not increase over the specified absolute maximum value.

The differential inputs feature an internal input resistor R_{dIN}. This resistor assures that in the case of input control or input feedback wire interruption the input differential voltage will be within the V_{dp-} to V_{dp+} range and the motor position remains frozen.

The circuit features an overvoltage disable function referred to the supply voltage V_S. This function assures disabling the output for V_S higher than 18V, both outputs are forced to tristate in this condition.

The thermal overload function disables the output tristate when the junction temperature increases above the thermal shutdown threshold temperature of min. 150°C. For the start of a heavy loaded motor, if the motor current reaches the max. value it is necessary to respect the dynamical thermal resistance junction to ambient. The internal output current limitation threshold is rated to be higher than 1.2A. The maximum junction temperature in this phase should not increase above the thermal shutdown threshold. In the case of output disable due to thermal overload remains the output disabled till the junction temperature decreases under the thermal enable threshold. This behaviour is assured with the thermal shutdown threshold hysteresis, its minimum value is 20K.

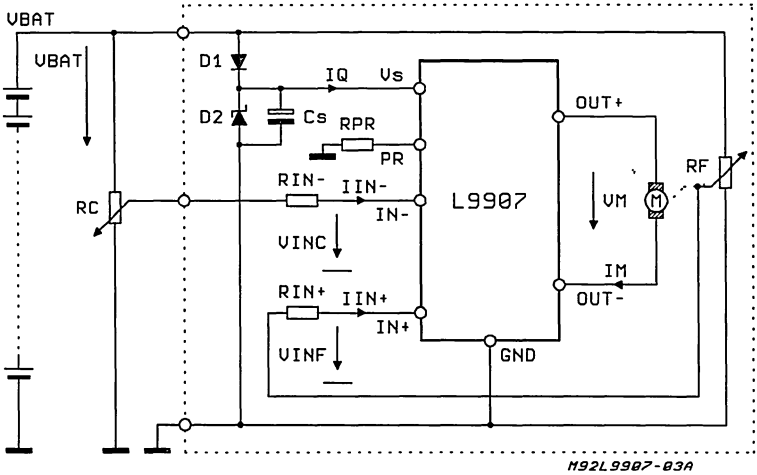
Fig. 2 and Fig. 3 shows two typical application diagrams for the headlight adjustment application. The preferable configuration is the differential input one, fig. 2 in which the optimum performance regarding the positioning precision and noise immunity is reached. To assure the safety of the circuit in the reverse battery condition a reverse protection diode D1 is necessary. The input currents in this condition are limited by the resistors R_{IN+} and R_{IN-}. The transient protection diode D2 must assure that the maximal supply voltage V_S during the transients at the V_{BAT} line will be limited to a value lower than the absolute maximum rating for V_S.

The device features an output disable function in case of input voltage overdrive. When the input voltage at one or both inputs increases above the input common mode range limit ($V_{IN} \geq V_S$ - 1.5V) both outputs will be forced to the source active condition (motor shortedx - stop). The thresholds of the described disable circuits are above and below the input common mode range, threfore a regular function is maintained until these thresholds are reached.

Proposed additional features which may be implemented (not confirmed):

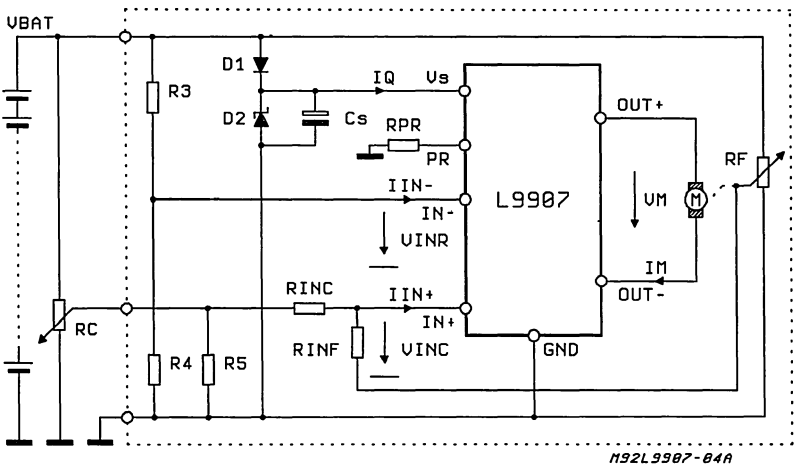
- Disable for input voltage overdrive.
  In the case of input control wire or input feedback wire short circuit to ground or the V_{BAT} line the output of the device will be disabled and therefore the previous motor position remains also in this fault condition unchanged. The input voltage threshold for the output disable function are in the range below 0.5V and above V_S-1.5V.
- V_{dp} and V_{dn} programmability with an external resistor.
- V_S dependent V_{dp} and V_{dn} or V_S independent positioning precision and noise immunity.
- Output short circuit current limitation.
- Disable/standby function.

Figure 2: Application Circuit (differential input configuration)



Note: Recommended value of R_{IN-}, R_{IN-} is 5 to 10kΩ.

Figure 3: Application Circuit (summing point configuration)



Note: R5 is necessary to define the motor low position in case of broken control wire.
Recommended value of the input source equivalent resistor value is 5 to 10kΩ.

SGS-THOMSON MICROELECTRONICS

L9930

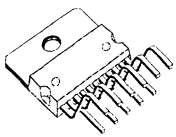
DUAL FULL BRIDGE

PRODUCT PREVIEW

- $R_{DS\ ON}$ = 2Ω
- INTERNAL CLAMPING VOLTAGE = 50V
- INTERNAL FREE WHEELING DIODES
- PARALLEL DRIVE CAPABILITY
- RESISTIVE OR INDUCTIVE LOAD

PROTECTION:
- TEMPERATURE PROTECTION
- SHORT-CIRCUIT PROTECTION (V_{bat}, LOAD, GND)

DETECTION:
- SHORTED LOAD
- OPEN LOAD



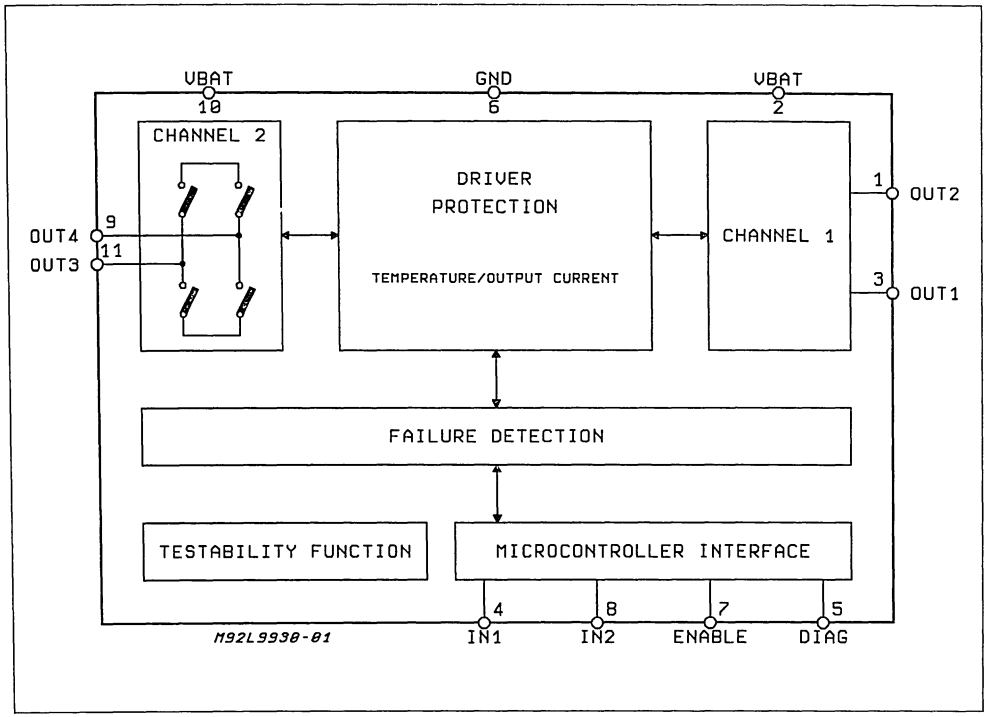
Multiwatt 11

ORDERING NUMBER: L9930

DESCRIPTION

The L9930 mounted in Multiwatt 11, is a dual full-bridge. The output stages are Power Mos switches.

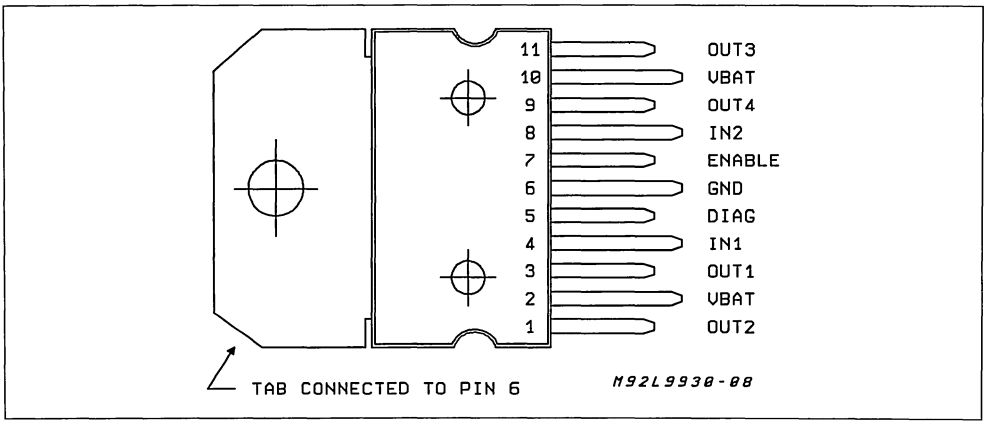
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
E	Clamped Energy at the Switching off	70	mJ
$V_{out\ DC}$	Continuous Output Voltage	24	V
$V_{out\ tr}$	Transient Output Voltage	50	V
$V_{bat\ DC}$	Continuous Battery Voltage	5 to 24	V
$V_{bat\ tr}$	Transient Battery Voltage	50	V
I_{out}	Reverse Output Current	– 3	A
f_{in}	Input Frequency	500	Hz
V_{in}	Input Voltage	– 1.5 to +7	V
V_{diag}	Diagnostic Voltage	– 1.5 to +7	V
T_s	Storage Temperature	– 55 to 150	°C
T_J	Operating Junction Tem	– 40 to 150	°C
V_{ESD}	V_{ESD} (Note MIL STD 883C)	3000	V

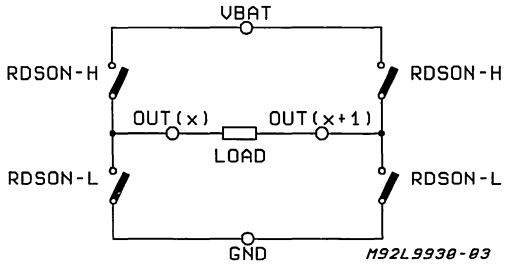
PIN CONNECTION



PIN FUNCTIONS

N.	Name	Function
1	OUT 2	Output Channel 1
2	V_{BAT}	Power Supply
3	OUT 1	Output Channel 1
4	IN 1	Input Channel 1
5	DIAG	Diagnostic Output Common for the 2 Channels
6	GND	Ground
7	ENABLE	Enable
8	IN 2	Input Channel 2
9	OUT 4	Output Channel 2
10	V_{BAT}	Power Supply
11	OUT 3	Output Channel 2

H-BRIDGE CONFIGURATION



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction to Case	max.		°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance Junction to Ambient	max.		°C/W

ELECTRICAL CHARACTERISTICS (V_{bat} = 8 to 18V tJ = – 40 to +150°C, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$R_{DSon\text{-}H}$	ON Resistance	I_{out} = 0.5A		2	4.3	Ω
$R_{DSon\text{-}L}$	ON Resistance	I_{out} = 0.5A		2	4.3	Ω
V_{OCL}	Clamping Voltage	I_{out} = 0.1A		50		V
V_F	Clamp Diode Forward Voltage	I_{out} = 0.6A (see fig. 1)		1.3		V
T_R	Output Voltyage Rise Time	V_{out}; 0.1 to 0.9 V_{out} (see fig. 1)		50	100	µs
T_F	Output Voltage Fall Time	Vout; 0.9 to 0.1 V_{out} (see fig. 1)		50	100	µs
T_{DR}	Input to Output Rising edge Delay	0.5 V_{IN} to 0.1 V_{OUT} (see fig. 1)			50	µs
T_{DF}	Input to Output Falling Edge Delay	0.5 VIN to 0.9 V_{OUT} (see fig. 1)			50	µs

OUTPUT PROTECTIONS CHARACTERISTICS

I_{SC}	Short Circuit		0.8		2.4	A
T_{SD}	Temperature		160			°C
T_{HYST}	Temperature Hysteresis			20		°C

These protections switch off the full bridge.

OUTPUT DETECTIONS CHARACTERISTICS

$R_{OPL\text{-}L}$	Open-load Threshold Resistor		100			Ω
$R_{OPL\text{-}H}$			200			Ω

SUPPLY CHARACTERISTICS

I_{QHI}	Supply Current	$I_{out1\text{-}R}$ = $I_{out2\text{-}R}$ 0.5A $I_{out1\text{-}L}$ = $I_{out2\text{-}L}$ – 0.5A V_{BAT} = 14V			15	mA
I_{QLO}		R_{load1} = R_{load2} = 50Ω V_{BAT} = 12V, ENABLE = 0			0.5	mA

ELECTRICAL CHARACTERISTICS

INPUTS CHARACTERISTICS (normal and standby mode)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IH}	High Threshold				4	V
V_{IL}	Low Threshold		1			V
I_{NHI}	Input Current 1	V_{IN} = 4V			200	µA
I_{NLO}	Input Current 2	V_{IN} = 1V			200	µA

DIAGNOSTIC CHARACTERISTICS

V_{DIAGL}	Low Level Voltage	I_{DIAG} = 2mA		0.6	0.8	V
I_{DIAGH}	Leakage Current	V_{DIAG} = 5.25V		5	10	µA

INITIALIZATION CHARACTERISTICS

T_{INIT}	Initialization Timing	V_{BAT} = 12V	10			µs
T_{STUP}	Start-Up Timing	V_{BAT} = 12V	20			µs

TRUE TABLE

ENAB	IN1	IN2	OUT1	OUT2	OUT3	OUT4	MODE	DIAG
0	0	0	HZ	HZ	HZ	HZ	STANDBY	?
0	0	1	HZ	HZ	HZ	HZ	NORMAL	?
0	1	0	HZ	HZ	HZ	HZ	NORMAL	?
0	1	1	HZ	HZ	HZ	HZ	NORMAL	?
1	0	0	HSD	LSD	HSD	LSD	NORMAL	VALID
1	0	1	HSD	LSD	LSD	HSD	NORMAL	VALID
1	1	0	LSD	HSD	HSD	LSD	NORMAL	VALID
1	1	1	LSD	HSD	LSD	HSD	NORMAL	VALID

Figure 1: Initialization.

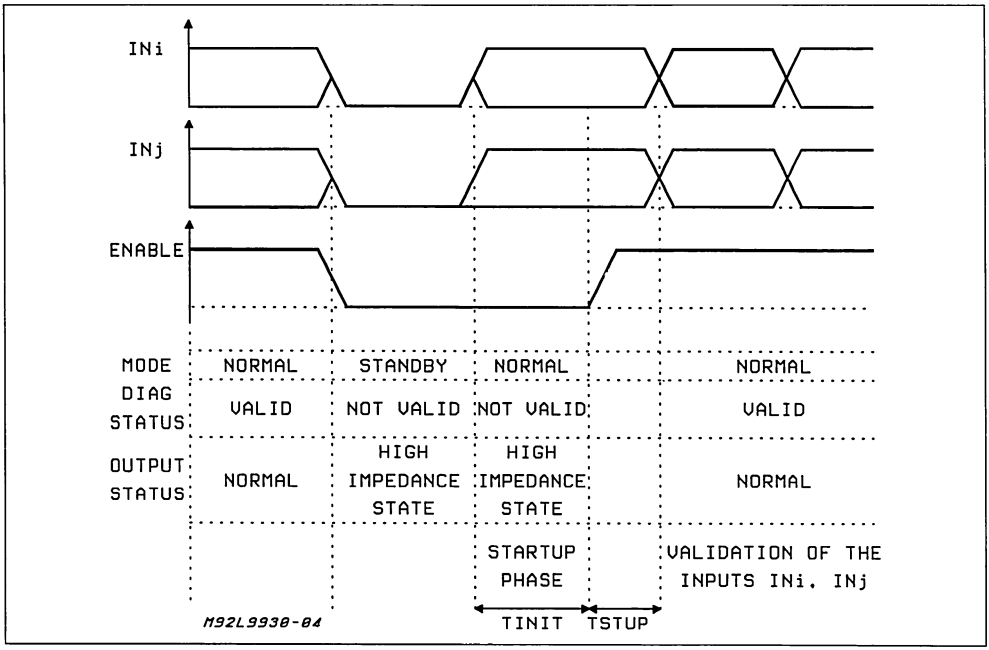


Figure 2: Normal Condition.

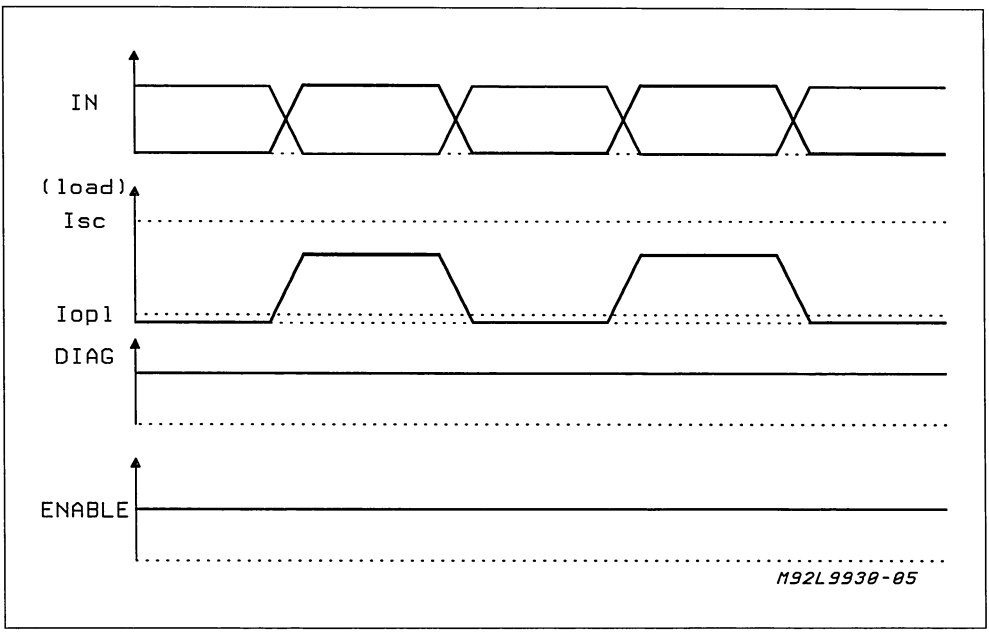


Figure 3: Short-circuit Condition.

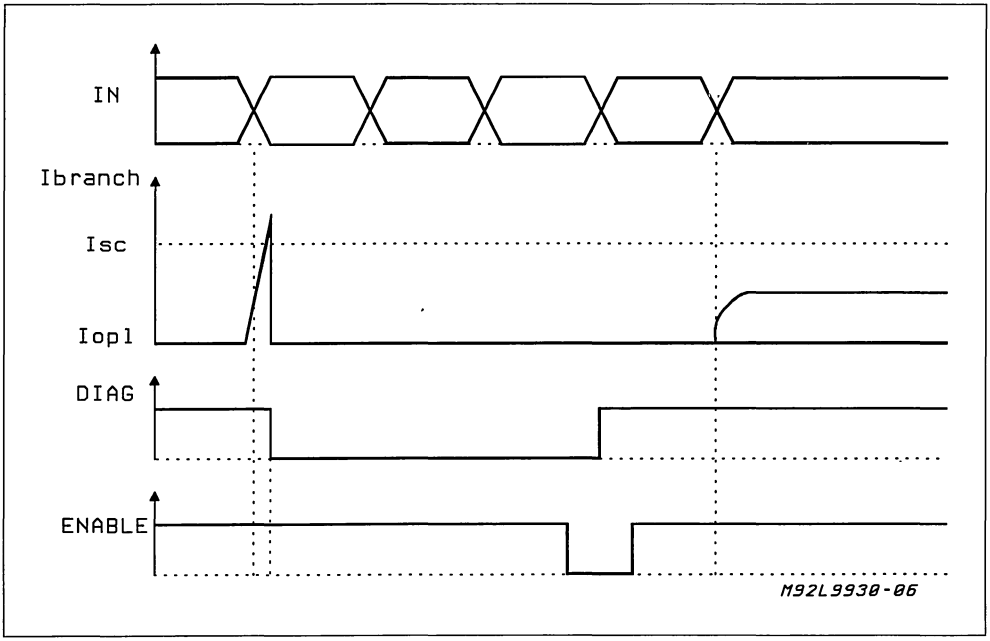
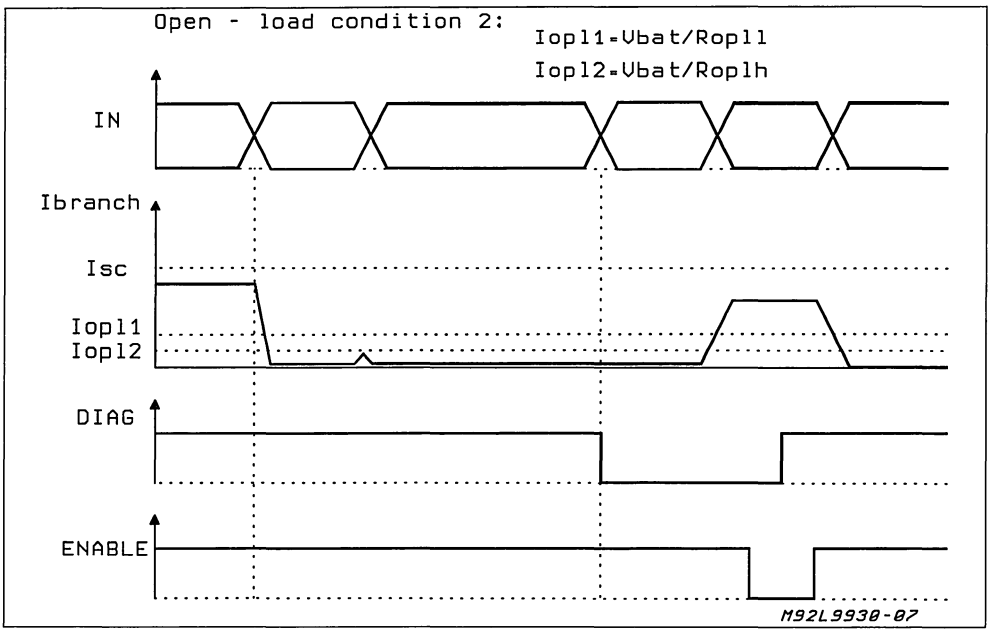
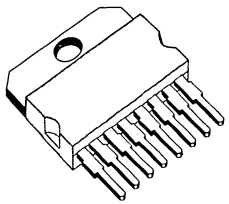


Figure 4.



HALF BRIDGE MOTOR DRIVER

- 20A OUTPUT CURRENT / DC OPERATION
- LOW SATURATION VOLTAGE
- VERY LOW CONSUMPTION IN OFF STATE
- OVERLOAD DIAGNOSTIC OUTPUT
- INTERNAL TEMPERATURE SENSOR
- GROUNDED CASE
- MULTIWATT-8 PACKAGE WITH HIGH CURRENT LEADS



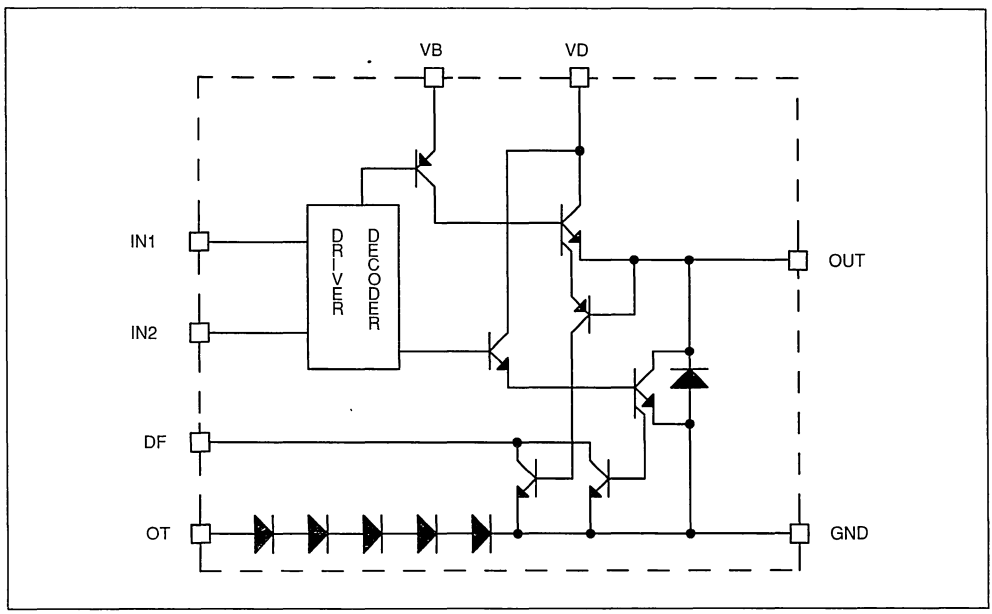
Multiwatt-8

ORDERING NUMBER: L9936

DESCRIPTION

The L9936 device is an half "H" bridge in bipolar technology particularly suited to drive up to 20A bidirectional DC motors.
The device also performs an overload diagnostic output and an internal temperature sensor.
The device is assembled in Multiwatt-8 package with the case connected to the ground terminal.

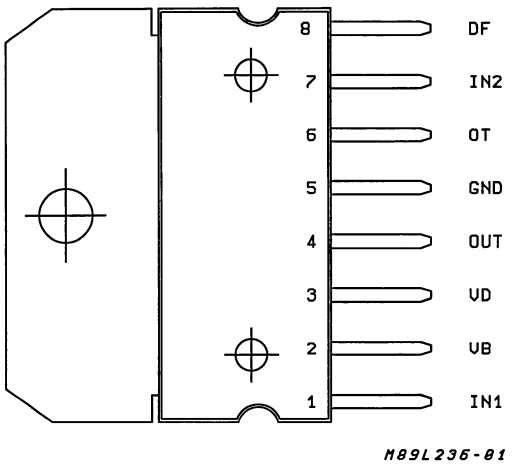
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_B	Maximum DC Voltage (non operating mode)	28	V
V_B	Maximum DC Operating Voltage	20	V
V_B	Maximum Transient Voltage tr = 5ms, td = 300ms (non operating mode)	50	V
V_I	Input Voltage	-0.3V to VB	V
V_{DF}	Diagnostic Feedback Voltage	-0.3 to 6	V
I_O	Output Current	30	A
T_j, T_{stg}	Junction and Storage Temperature Range	-40 to +150	°C

PIN CONNECTION (Top View)



PIN FUNCTIONS

N•	Name	Description
1	IN1	Command input to switch on the upper power transistor of the half bridge
2	VB	Positive supply voltage (to be connected before the reverse battery protection diode)
3	VD	Positive supply voltage (to be connected after the reverse battery protection diode)
4	OUT	Power Output
5	GND	Power ground (also connected to the case)
6	OT	Analog output to monitor the internal temperature of the device
7	IN2	Command input to switch on the lower power transistor of the half bridge
8	DF	Open collector output to monitor overload conditions

INPUT/OUTPUT TRUTH TABLE

IN1	IN2	OUT
L	L	Z
L	H	L
H	L	H

Note 1. Z means high impedance condition
Note 2 IN1 and IN2 must not be H at the same time

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	1.3	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 14.4V; -40 < Tj < 125°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_B	Operating Voltage		8.5		19	V
V_D	Operating Voltage		7.5		18	V
V_{OL}	Output to GND Saturation Voltage	I_O = 20A		650	850	mV
V_{OHB}	V_B to Out Saturation Voltage	I_O = 20A		1.5	1.75	V
V_{OHD}	VD to Out Saturation Voltage	I_O = 20A		650	850	mV
I_{SD}	Supply ON Current (V_O = L)			1		A
I_{SU}	Supply ON Current (V_O = H)			300		mA
I_{off}	Supply Off State Current	Tj = 25°C			100	µA
I_{IN}	Input ON Current	V_{IN} = 6.5V		4	6	mA

APPLICATION INFORMATIONS

L9936 is particularly suitable in full bridge configurations to drive high current bidirectional DC motors in µC based systems.
Fig. 1 shows a possible application circuit, with an analog interface between the power devices and the µC. In the following, the functions of each block of the analog interface are described.

1 - Overvoltage And Reverse Battery Protection

L9936 is particularly suitable as a full bridge to drive the window lift motors in automotive applications. Fig. 2 shows the circuit schematics; due to the hostile automotive environment, it is necessary a transil (suggested type LDP24A) between VD and GND, to protect the two L9936 against overvoltages higher than 50V. In addition, if the reverse battery protection is requested, the diode D1 between VB and VD can be used (suggested type BY239).

Figure 1

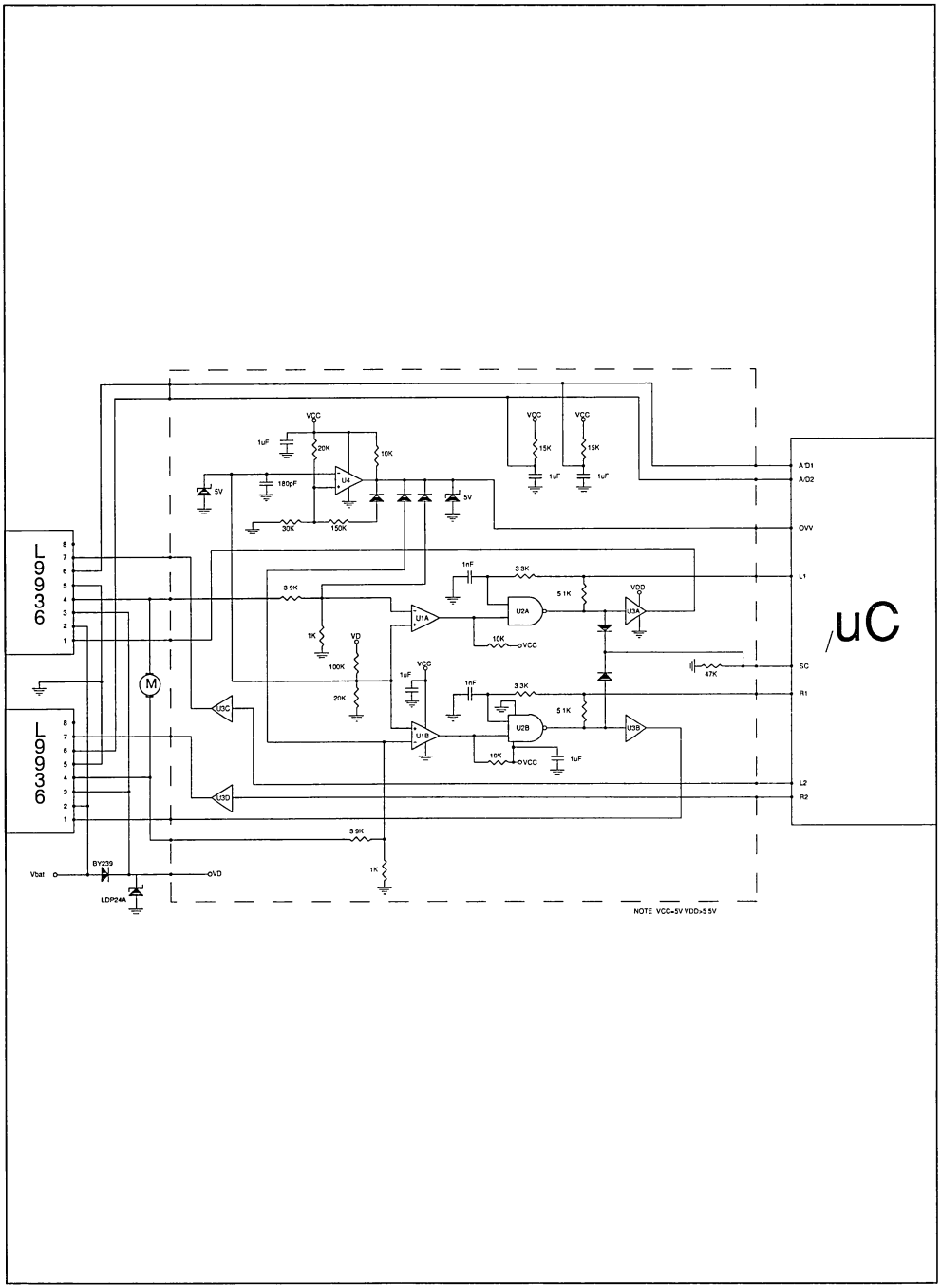
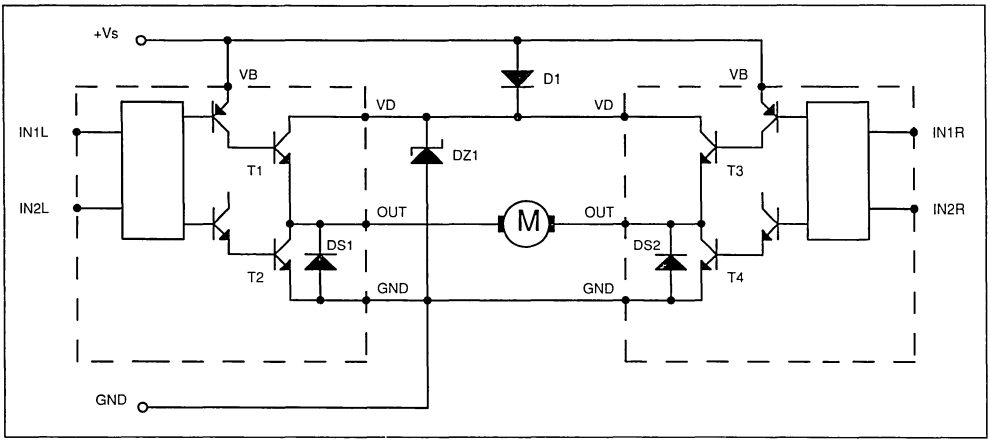

L9369
L9369
VCC
1uF
20K
10K
U4
5V
180pF
30K
150K
15K
1uF
1nF
3.3K
5.1K
U2A
U1A
U3A
VDD
3.9K
1K
VD
100K
20K
10K
VCC
47K
U2B
U1B
U3B
U3C
U3D
M
Vbat
BY239
LDP24A
OVD
NOTE VCC=5V VDD>5.5V
A/D1
A/D2
OVV
L1
SC
R1
L2
R2
uC

Figure 2



2 - Switch-off Sequence

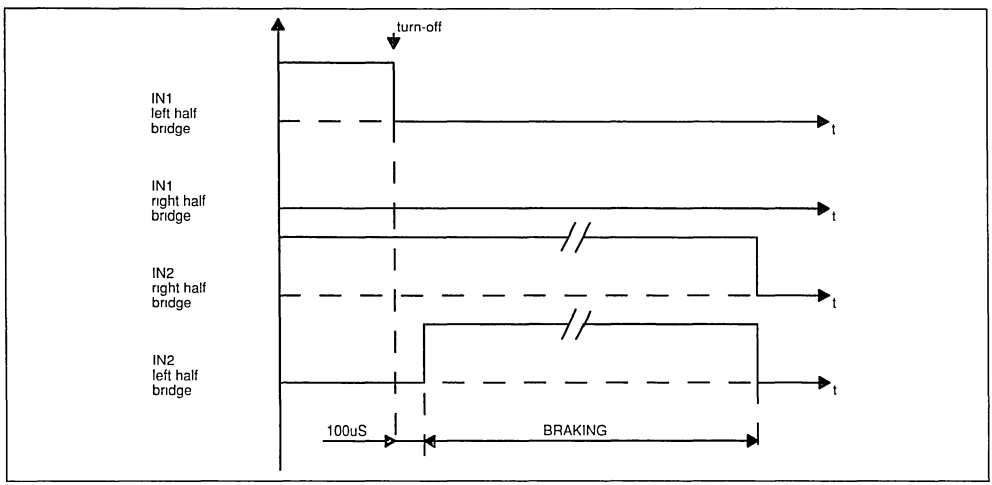
Referring to Fig. 2 and supposing i.e. T1 and T4 ON, T2 and T3 OFF (this means IN1L = IN2R = H, IN2L = IN1R = L), the following steps have to be observed to allow a correct recirculation of the current in the motor at the switch off (Ref. Fig. 3):

a) switch off T1 and wait for 100µsec about in this condition (IN1L = IN2L = IN1R = L, IN2R = H)
b) after the a.m. delay switch ON T2 (IN1L = IN1R = L, IN2L = IN2R = H)
c) switch off both T2 and T4 (IN1L = IN2L = IN1R = IN2R = L)

Step a) allows the recirculation of the motor current due to the inductive component of the motor itself between DS1 and T4; the 100µsec delay time is needed to avoid the cross-conduction in the left half bridge.

In step b) the motor is short circuited to GND (T2 and T4 ON) and this allows the dynamic braking. In step c) T1, T2, T3 and T4 are OFF to allow a very low current consumption of the two half bridges.
If the dynamic braking is not requested, step b) can be omitted. In any case the lower power transistor of an half bridge must be kept ON, after the switch off of the upper transistor of the other half bridge, for a time longer than $T = 5 \cdot R_L / L_L$, where R_L and L_L are the resistance and the inductance of the load.

Figure 3: Switch-off Sequence



3 - Input Driving Voltage

To allow a correct operation of L9936 over the full temperature range, the driving voltage at the input pins must be higher than 5.5V, with 5mA current capability.

4 - Short Circuit Protection

It is possible to protect L9936 against short circuit to ground and across the motor in the full bridge application.
The circuit schematics shown in Fig. 4 uses two voltage comparators (U1A, U1B) to detect the Vce of the upper power transistors.
U2A and U2B are open drain NAND gates (i.e. part no. HCC40107) and U3A/B/C/D are non inverting buffer to drive the two L9936 (i.e. part no. 74HC4050).
U1A and U1B sense the differential voltage VD-OUTL and VD-OUTR respectively.
Referring to Fig. 4, chosen R1=100K and R2 = 20K, the values of R3 and R4 may be calculated according to the following formula:

$$R3 = \frac{(V_D - V_{CETH}) - 0.166\ V_D)}{0.166\ V_D} * R4$$

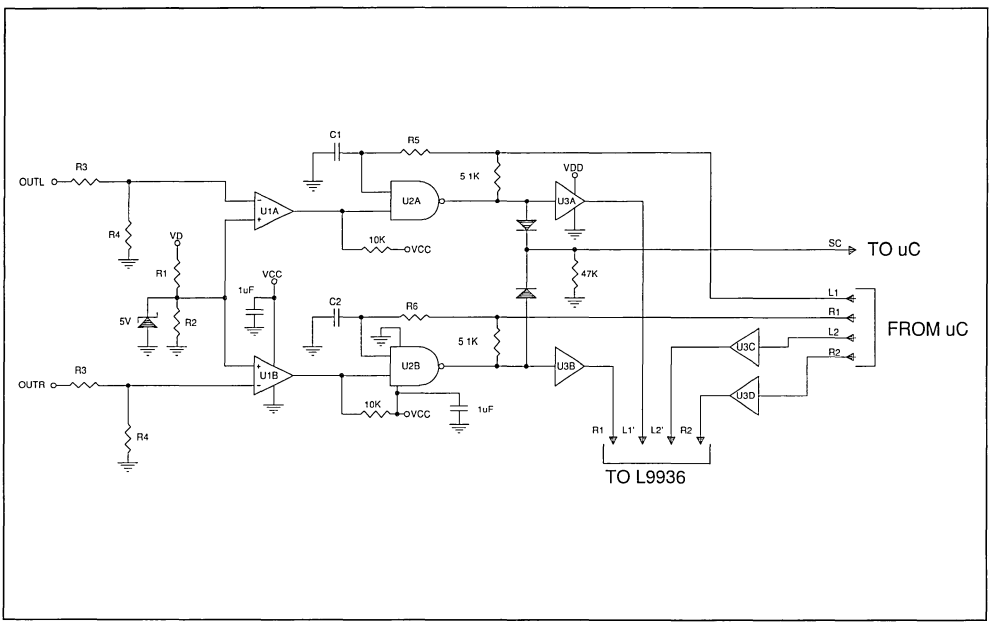
where :

V_D = bridge power supply
V_{CETH} = collector to emitter detection threshold.
Choosing V_{CETH} = 2V @ V_D = 12V and R4 = 1K, the above formula gives R3 = 4K.

When all signals from µC are at low level (motor off), the input to the two half bridges are low too; in these conditions the output voltage of the two comparators is high and therefore the outputs of U2A/U2B are free.
When the µC sends, for example, L1 and R2 high, the left half bridge output goes high and the right one goes low.
At this point the output of U1A pulls down the input of U2A before that the delay capacitor C1 is charged (through R5) up to the U2A threshold; in this way the U2A output remains free and the bridge drives the motor.
If a short circuit occurs, the Vce of the upper power transistor increases above the threshold and then the U2A output pulls down the L1 input to L9936.
Contemporary the SC signal to µC, high in normal conditions, goes low; at this point the µC executes the switch-off sequence.
We have just explained what happens when a short circuit occurs during the motor running phase.
Another faulting condition occurs switching on the bridge when a short circuit is present; in this case the bridge is driven for a time depending on the time constant R5 • C1 = R6 • C2. Choosing R5 = R6 = 3.3K and C1 = C2 = 1nF, then the time constant will be T = 3.3µsec, that is 5µsec about delay time. Longer delay time might allow the short circuit current to reach values beyond the absolute maximum ratings.

5 - Thermal Protection

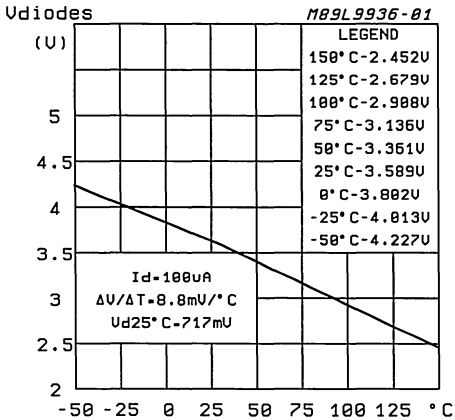
Figure 4



The L9936 has 5 built-in diodes series-connected that can be used to implement a thermal protection for the device.
Fig. 5 shows the relationship between the voltage across the diodes and the temperature at 100µA diode current.

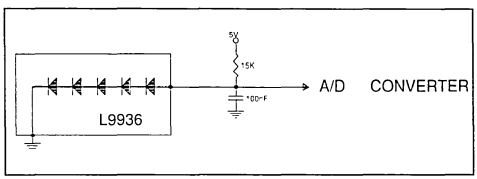
Fig. 6 shows the simplest solution to do a thermal

Figure 5



protection; an A/D converter of the µC is used to detect the voltage drop across the 5 diodes. The 15K resistor sets the current in the diodes and the 100nF capacitor acts as a filter against the noise. When the µC detects a voltage lower than the low threshold chosen according to the diagram in Fig. 5, it executes the switch-off sequence and rejects any command to the bridge until the diodes voltage increases beyond the high threshold. The recommended hysteresis value is 30°C.

Figure 6

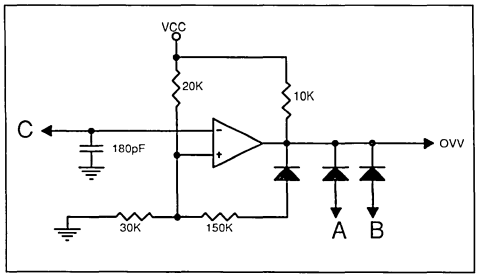


6 - Overvoltage Protection

At point 1 we suggest a way to protect the L9936 against the voltage transients. This protection allows the device to withstand overvoltages only if the bridge is not operating. To protect the device against the overvoltages in all the operating conditions it is possible to implement the circuit shown in Fig. 7.

(Note: A-B are connected to the nodes between R3 and R4 (left side and right side) in Fig. 4; C is connected to the node between R1 and R2 in Fig. 4). When V_D reaches 18V the comparator output

Figure 7



pulls down A and B, causing the intervention of the hardware protection shown in Fig. 4; at the same time the OVV signal is sent to µC, which executes the switch off sequence. The µC must reject any command to the bridge during the overvoltage conditions.
With the values showed in Fig. 7, a 1V hysteresis is provided.
It is possible to enhance the performances of the system just described avoiding the braking of the motor also for short duration voltage transients; to do this the µC, once received the overvoltage diagnostic signal (OVV), put at low level the commands to the upper transistors of the two half bridges (L1 and L2 in Fig. 4), allowing the free running of the motor.
The system holds this condition until OVV is active; when the OVV signal is released the µC restores the previous commands to the bridge.

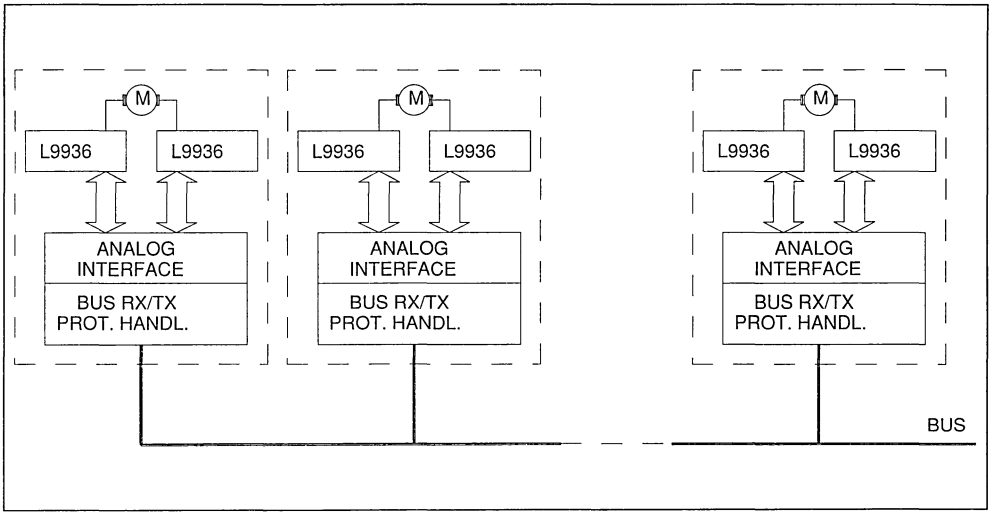
7 - Diagnostic Feedback Output

DF pin is an open drain output to monitor overcurrent and overtemperature conditions.
The overcurrent detection threshold is inversely dependent from the temperature of the chip.
Typical application of this function is to send the DF signal, with an external pull-up to Vcc, to a digital input of the µC; when the DF signal goes at low level, the µC executes the switch-off sequence.

L9936 IN A BODY MULTIPLEX ENVIRONMENT

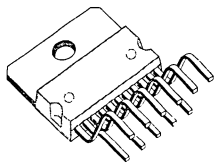
All the functions described above can be implemented in a custom integrated circuit together with a bus transceiver and a protocol handler. It is then possible to obtain a very small size module that can be integrated directly in the actuator. Fig. 8 shows a typical application of these modules as peripheral units in a "Class A" wired Multiplex System.

Figure 8: "Class A" Wired Peripheral Application



FULL BRIDGE MOTOR DRIVER

- 6A OUTPUT CURRENT
- LOW SATURATION VOLTAGE
- VERY LOW CONSUMPTION IN OFF STATE
- OVERLOAD DIAGNOSTIC OUTPUT
- INTERNAL TEMPERATURE SENSOR
- GROUNDED CASE



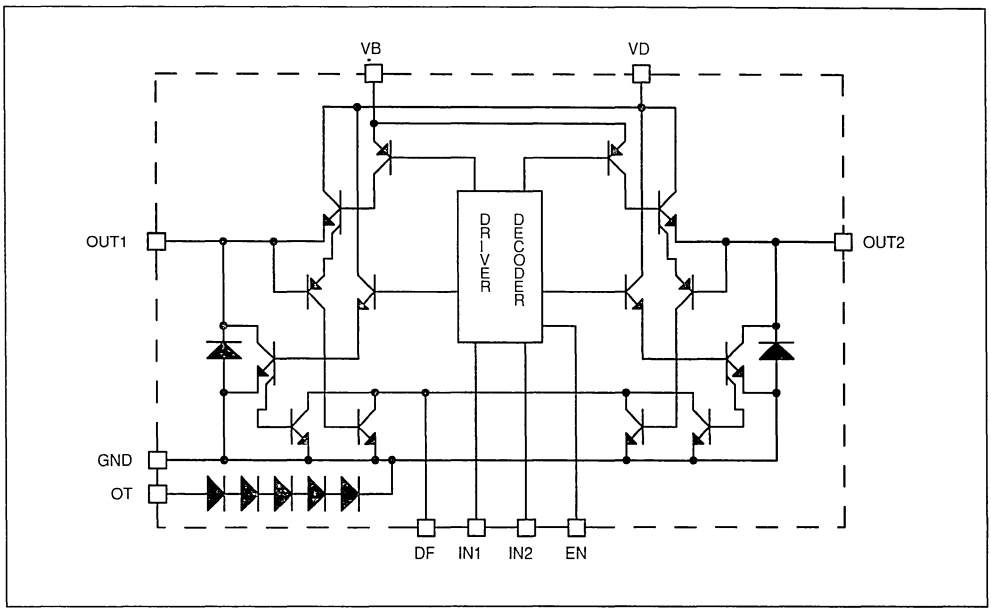
Multiwatt 11

ORDERING NUMBER: L9937

DESCRIPTION

The L9937 device is a full bridge for bidirectional motor driver applications realized in bipolar technology; it can deliver up to 6A output current with low saturation voltage.
Two diagnostic informations are provided to monitor overload conditions and the internal temperature.
The device is assembled in the MULTIWATT-11 package with the case connected to the ground terminal.

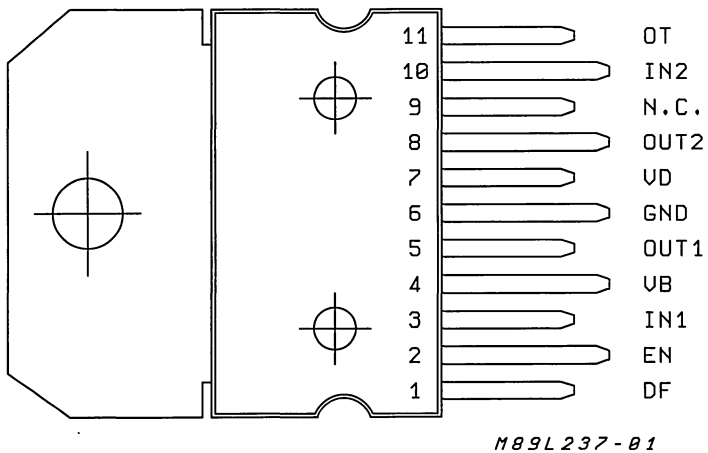
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_B	Maximum DC Voltage (non operating mode)	28	V
V_B	Maximum DC Operating Voltage	20	V
V_B	Maximum Transient Voltage tr = 5ms, td = 300ms (non operating mode)	50	V
V_I	Input Voltages	-0.3V to VB	V
V_{DF}	Diagnostic Feedback Voltage	-0.3 to 6	V
I_O	Output Current	10	A
T_j, T_{stg}	Junction and Storage Temperature Range	-40 to +150	°C

PIN CONNECTION (Top View)



PIN FUNCTIONS

N°	Name	Description
1	DF	Open collector output to monitor overload conditions
2	EN	Enable Input
3	IN1	Command input
4	VB	Positive supply voltage (to be connected before the reverse battery protection diode)
5	OUT1	Power output of the 1st half bridge
6	GND	Power ground (also connected to the case)
7	VD	Positive supply voltage (to be connected after the reverse battery protection diode)
8	OUT2	Power output of the 2nd half bridge
9	N.C.	Not connected
10	IN2	Command input
11	OT	Analog output to monitor the internal temperature of the device

INPUT/OUTPUT TRUTH TABLE

EN	IN1	IN2	OUT1	OUT2
L	L	L	Z	Z
L	H	L	Z	L
L	L	H	L	Z
L	H	H	L	L
H	L	L	Z	Z
H	H	L	H	L
H	L	H	L	H
H	H	H	L	L

Note 1: Z means high impedance condition
Note 2 All other conditions are not permitted

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th\,j\text{-}case}$	Thermal Resistance Junction-case	TBD	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 14.4V; -40 < Tj < 125°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_B	Operating Voltage		8.5		19	V
V_D	Operating Voltage		7.5		18	V
V_{OL}	Output 1/2 to GND Saturation Voltage	I_O = 6A		650		mV
V_{OHB}	V_B to Out1/2 Saturation Voltage	I_O = 6A		1.5		V
V_{OHD}	VD to Out1/2 Saturation Voltage	I_O = 6A		650		mV
I_{SD}	Supply ON Current	OUT1 = H; OUT2 = L OUT1 = L; OUT2 = H		360		mA
I_{SH}	Supply ON Current	OUT1/2 = H		600		mA
I_{off}	Supply Off State Current	Tj = 25°C			100	µA
I_{IN}	Inputs ON Current	V_{IN} = 6.5V		3.5		mA

APPLICATION INFORMATIONS

L9937 is particularly suitable to drive up to 6A bidirectional DC motors in µC based systems.
Fig. 1 shows a possible application circuit, with an analog interface between the power devices and the µC. In the following, the functions of each block of the analog interface are described.

1 - Overvoltage And Reverse Battery Protection

L9937 is particularly suitable to drive the door lock motors in automotive applications. Fig. 2 shows the circuit schematics; due to the hostile automotive environment, it is necessary a transil (suggested type 1.5KE36) between V_D and GND, to protect the L9937 against overvoltages higher than 50V. In addition, if the reverse battery protection is requested, the diode D1 between VB and VD can be used (suggested type BYW29-200A).

Figure 1

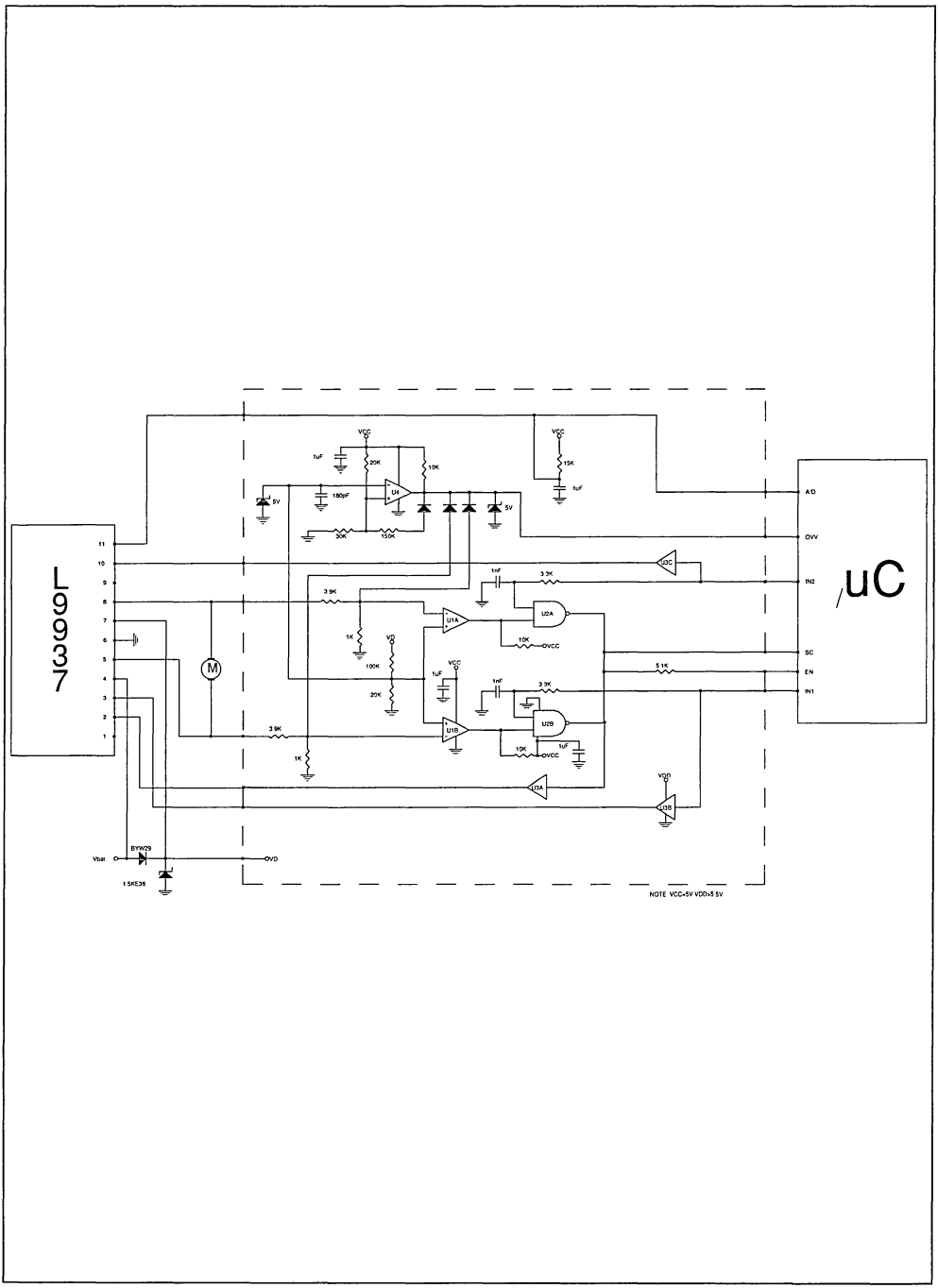
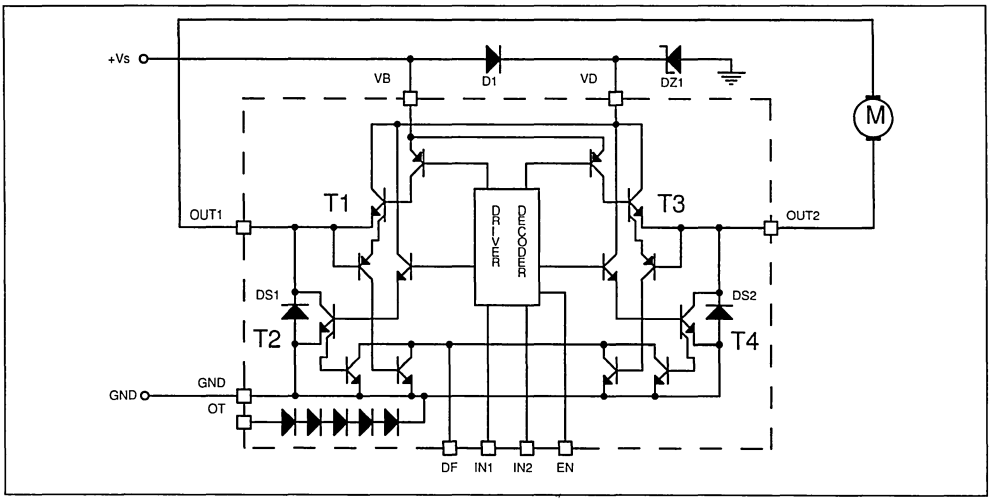

L9937
µC
A/D
OVV
IN2
SC
EN
IN1
VCC
VDD
OVCC
OVD
Vbat
BYW29
1.5KE36
NOTE VCC=5V VDD=5 5V

Figure 2



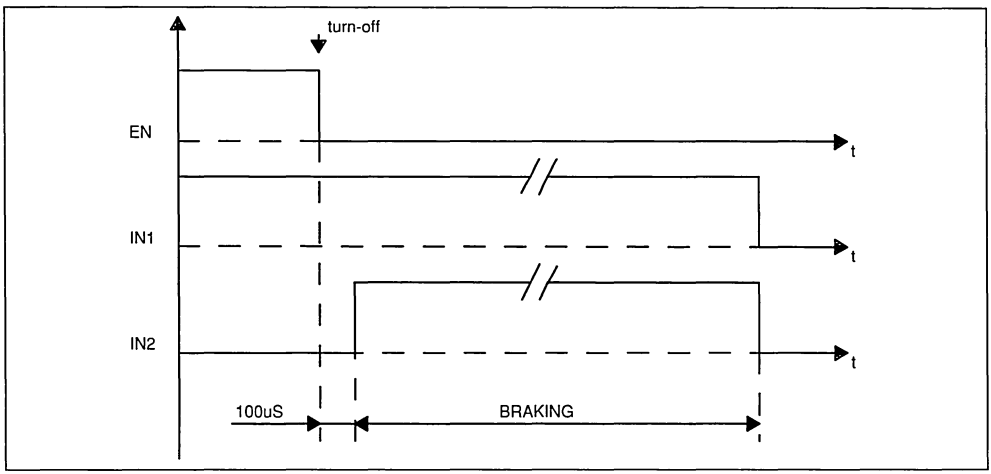
2 - Switch-off Sequence

Referring to Fig. 2 and supposing i.e. T1 and T4 ON, T2 and T3 OFF (this means EN=H IN1=H IN2=L), the following steps have to be observed to allow a correct recirculation of the current in the motor at the switch off (Ref. Fig. 3):

a)switch off T1 and wait for 100sec about in this condition (EN = L IN1 = H IN2 = L)
b)after the a.m. delay switch ON T2 (EN = L IN1 = H IN2 = H)
c)switch off both T2 and T4 after the motor stop (EN = L IN1= L IN2 = L)

Step a) allows the recirculation of the motor current due to the inductive component of the motor itself between DS1 and T4; the 100µsec delay time is needed to avoid the cross-conduction in the left half bridge.
In step b) the motor is short circuited to GND (T2 and T4 ON) and this allows the dynamic braking. In step c) T1, T2, T3 and T4 are OFF to allow a very low current consumption of the bridge. If the dynamic braking is not requested, step b) can be omitted. In any case the lower power transistor of an half bridge must be kept ON, after the switch off of the upper transistor of the other half bridge, for a time longer than $T = 5 \cdot R_L/L_L$, where RI and LI are the resistance and the inductance of the load.

Figure 3: Switch-off Sequence



3 - Input Driving Voltage

To allow a correct operation of L9937 over the full temperature range, the driving voltage at the input pins must be higher than 5.5V, with 4mA current capability.

4 - Short Circuit Protection

It is possible to protect L9937 against short circuit to ground and across the motor in the full bridge application.
The circuit schematics shown in Fig. 4 uses two voltage comparators (U1A, U1B) to detect the Vce of the upper power transistors. U2A and U2B are open drain NAND gates (i.e. part no. HCC40107) and U3A/B/C/D are non inverting buffer to drive the L9937 (i.e. part no. 74HC4050).
U1A and U1B sense the differential voltage VD-OUT2 and VD-OUT1 respectively. Referring to Fig. 4, chosen R1=100K and R2=20K, the values of R3 and R4 may be calculated according to the following formula:

$$R3 = \frac{(V_D - V_{CETH}) - 0.166\ V_D}{0.166\ V_D} * R4$$

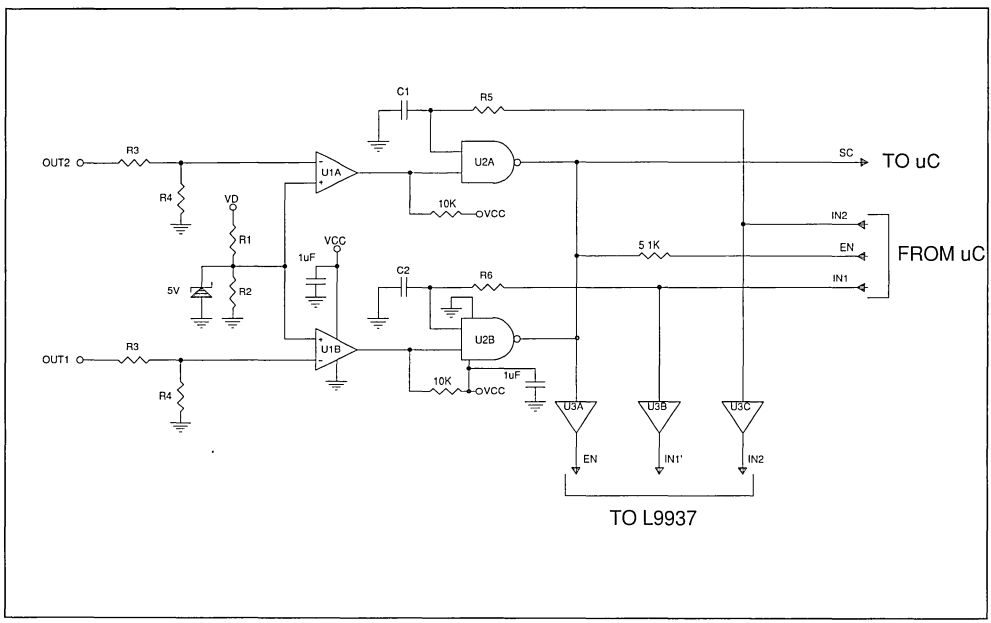
where :

V_D = bridge power supply
V_{CETH} = collector to emitter detection threshold.

Choosing:
V_{CETH} = 2V @ V_D = 12V and R4 = 1K, the above formula gives R3 = 4K.

When all signals from µC are at low level (motor off), the inputs to the bridge are low too; in these conditions the output voltage of the two comparators is high and therefore the outputs of U2A/U2B are free. When the µC sends, for example, IN2 and EN high, OUT2 of the bridge goes high and OUT1 goes low.
At this point the output of U1A pulls down the input of U2A before that the delay capacitor C1 is charged (through R5) up to The U2A threshold; in this way the U2A output remains free and the bridge drives the motor.
If a short circuit occurs, the Vce of the upper power transistor increases above the threshold and then the U2A output pulls down the enable input of L9937. Contemporary the SC signal to µC, high in normal conditions, goes low; at this point the µC executes the switch-off sequence.
We have just explained what happens when a short circuit occurs during the motor running phase. Another faulting condition occurs switching on the bridge when a short circuit is present; in this case the bridge is driven for a time depending on the time constant R5 • C1 = R6 • C2.
Choosing R5 = R6 = 3.3K and C1 = C2 = 1nF, then the time constant will be T = 3.3µsec, that is 5µsec about delay time. Longer delay time might allow the short circuit current to reach values beyond the absolute maximum ratings.

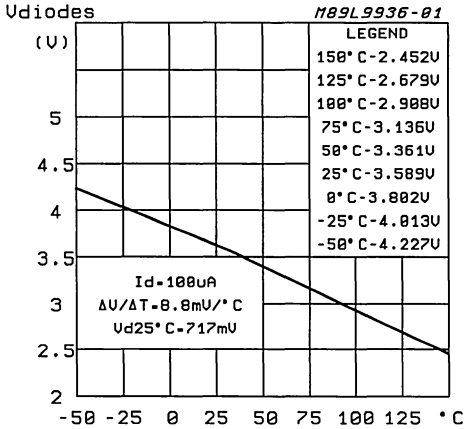
Figure 4



5 - Thermal Protection

The L9937 has 5 built-in diodes series-connected that can be used to implement a thermal protection for the device.
Fig. 5 shows the relationship between the voltage across the diodes and the temperature at 100A

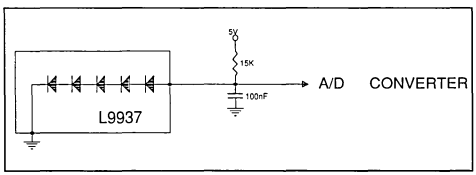
Figure 5



diode current.

Fig. 6 shows the simplest solution to do a thermal protection; an A/D converter of the µC is used to detect the voltage drop across the 5 diodes. The 15K resistor sets the current in the diodes and the 100nF capacitor acts as a filter against the noise. When the µC detects a voltage lower than the low threshold chosen according to the diagram in Fig. 5, it executes the switch-off sequence and rejects any command to the bridge until the diodes voltage increases beyond the high threshold. The recommended hysteresis value is 30°C.

Figure 6

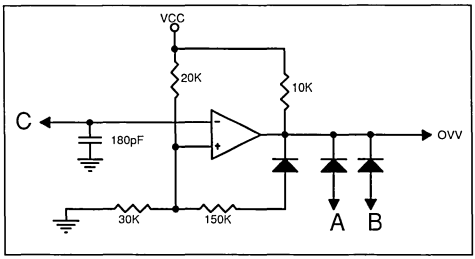


6 - Overvoltage Protection

At point 1 we suggest a way to protect the L9937 against the voltage transients. This protection allows the device to withstand overvoltages only if the bridge is not operating. To protect the device against the overvoltages in all the operating conditions it is possible to implement the circuit shown in Fig. 7.

(Note: A-B are connected to the nodes between

Figure 7



R3 and R4 (left side and right side) in Fig. 4; C is connected to the node between R1 and R2 in Fig. 4).
When V_D reaches 18V the comparator output pulls down A and B, causing the intervention of the hardware protection showed in Fig. 4; at the same time the OVV signal is sent to µC, which executes the switch off sequence. The µC must reject any command to the bridge during the overvoltage conditions.
With the values shown in Fig. 7, a 1V hysteresis is provided.
It is possible to enhance the performances of the system just described avoiding the braking of the motor also for short duration voltage transients; to do this the µC, once received the overvoltage diagnostic signal (OVV), put at low level the enable of the L9937, confirming the hardware switch-off of the motor; in this condition an output of the half bridge is in high impedance state and the other one is low, allowing the recirculation of the current and the free running of the motor.
The system holds this condition until OVV is active; when the OVV signal is released the µC resets the hardware protection, sending EN = IN1 = IN2 = L and then restore the previous command to the bridge.
It is mandatory, however, to wait for the complete current recirculation of the motor before to reset the hardware protection; in facts, when EN = IN1 = IN2 = L both the L9937 outputs are in high impedance conditions.

7 - Diagnostic Feedback Output

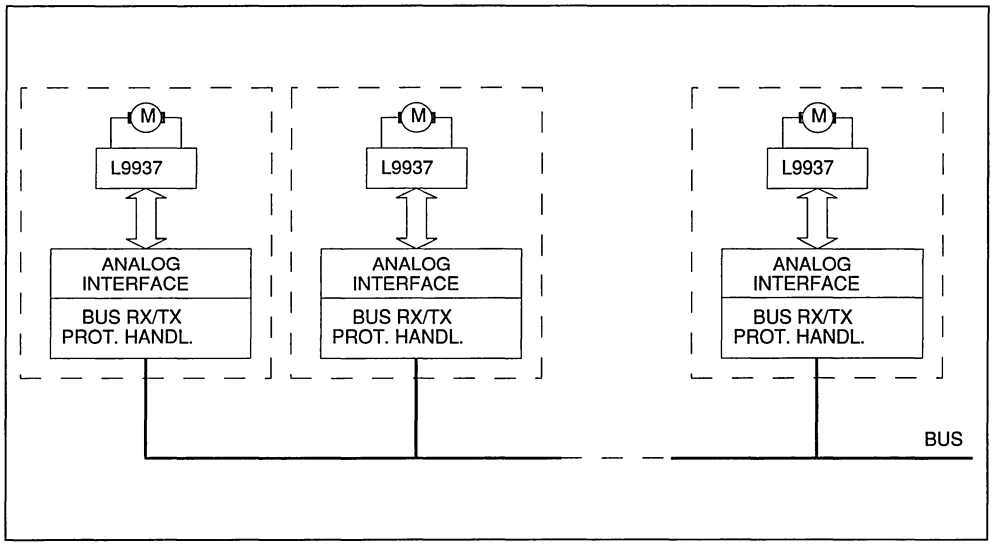
DF pin is an open drain output to monitor overcurrent and overtemperature conditions.
The overcurrent detection threshold is inversely dependent from the temperature of the chip.
Typical application of this function is to send the DF signal, with an external pull-up to Vcc, to a digital input of the µC; when the DF signal goes at low level, the µC executes the switch-off sequence.

L9937 IN A BODY MULTIPLEX ENVIRONMENT

All the functions described above can be implemented in a custom integrated circuit together with a bus transceiver and a protocol handler.

It is then possible to obtain a very small size module that can be integrated directly in the actuator. Fig. 8 shows a typical application of these modules as peripheral units in a "Class A" wired Multiplex System.

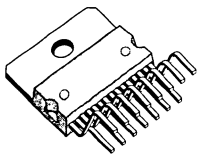
Figure 8: "Class A" Wired Peripheral Application



MULTIPLE HALF BRIDGE DRIVER

ADVANCE DATA

- 4.75A TOTAL OUTPUT CURRENT
- VERY LOW CONSUMPTION IN OFF STATE
- OVERLOAD DIAGNOSTIC
- OPEN LOAD DIAGNOSTIC
- GROUNDED CASE



Multiwatt 15

ORDERING NUMBER: L9946

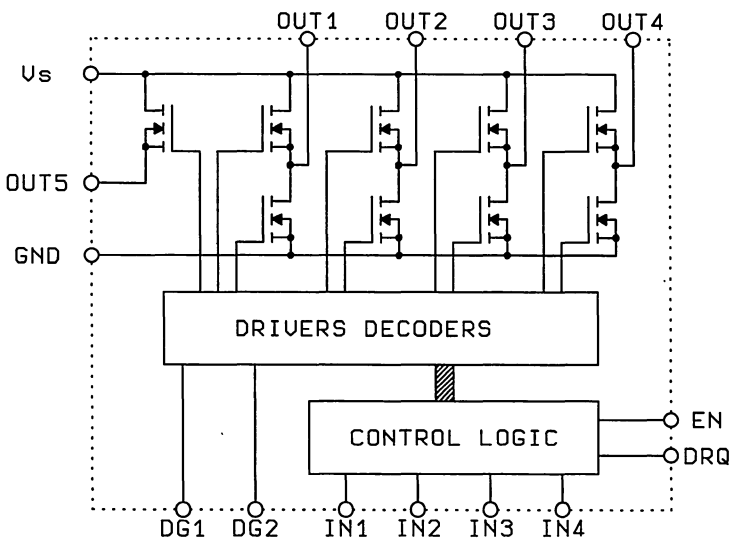
DESCRIPTION

The L9946 device is a quad half bridge plus an High Side Driver for bidirectional 3 motors and a grounded load driver applications realized in Multipower-BCD technology: it can deliver up to 4.75A output current.

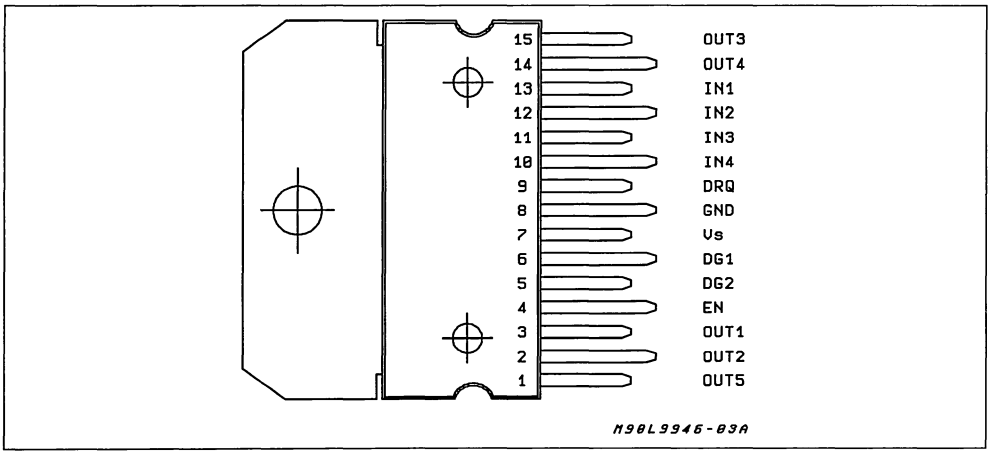
Multiple diagnostic informations are provided to monitor overload and open load conditions.

The device is assembled in the MULTIWATT-15 package with the case connected to the ground terminal.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	50	V
EN	Enable	-0.3 to 20	V
IN1 - IN4	Command Inputs	-0.3 to 20	V
DRQ	Diagnostic Request Input	-0.3 to 20	V
DG1 - DG2	Diagnostic Outputs Voltage Diagnostic Outputs Current	-0.3 to 60 10	V mA
OUT1-OUT2	Half Bridges Output Current	±2.5	A
OUT3-OUT4	Half Bridges Output Current	±5	A
OUT5	High Side Driver Output Current	-5	A
T_{stg}, T_j	Storage and Junction-Case Temperature	-40 to 150	°C
P_{tot}	Power Dissipation T_{CASE} = 85°C	26	W

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	2.5	°C/W

PIN FUNCTIONS

Pins	Description
V_S	Positive supply voltage (to be connected after the reverse battery protection diode).
EN	Enable, switches the device between the low consumption and the operating mode.
IN1, IN2, IN3	Command inputs of the four half bridges.
IN4	Command input of the high side driver.
DRQ	Diagnostic request input.
DG1, DG2	Diagnostic output (open drain).
OUT1, OUT2, OUT3, OUT4	Outputs of the four half bridges.
OUT5	Output of the high side driver.
GND	Ground

ELECTRICAL CHARACTERISTICS (V_S = 13V; -40 < T_j < 125°C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage	EN = H	8		32	V
I_{Vs}	Supply Current	EN < 0.8V T_j = 25°C			100	µA
I_{Vs}	Supply Current	EN = H; IN1 = IN2 = IN3 = IN4 = X DRQ = L	1		10	mA
I_{Vs}	Supply Current Open Load Diagnostic	EN = DRQ = H; IN1 = IN2 = IN3 = IN4 = L		50		mA
V_{en}	Enable Input Voltage High		2			V
V_{en}	Enable Input Voltage Low				0.8	V
Venth	Enable Threshold Hysteresis		50			mV
I_{en}	Enable Input Current High	0 < V_{en} < 5.5V			80	µA
V_{inH}	Input Voltage High		2			v
V_{inL}	Input Voltage Low				0.8	V
V_{inth}	Input Threshold Hysteresis		100			mV
I_{in}	Input Current	0 < V_{in} (1-4) < 5.5V			80	µA
V_{drqH}	Diagnostic Request High		2			V
V_{drqL}	Diagnostic Request Low				0.8	V
V_{drqth}	Diagnostic Req. Thr. Hysteresis		100			mV
I_{drq}	Diagnostic Req. Current	0 < V_{drq} < 5.5V			80	µA
R_{dg}	Diagnostic Output Resistance			100		Ω
Idg	Diagnostic Output leakage Current	V_{dg} (1-2) = 16V		50		µA
$R_{on\ OUT1}$ $R_{on\ OUT2}$ $R_{on\ OUT3}$ $R_{on\ OUT4}$	ON Resistance (to supply or to GND)	10V < V_S < 30V		6.5 6.5 0.32 0.32		Ω Ω Ω Ω
$I_{out1\ o\ l}$ $I_{out2\ o\ l}$ $I_{out3\ o\ l}$	Output Current in Open Load Diagnostic	IN1 = IN2 = IN3 = IN4 = L; DRQ = H EN = H		+10		mA
$I_{out3\ o\ l}$	Output Current in Open Load Diagnostic	IN1 = IN2 = IN3 = IN4 = L; DRQ = H EN = H		-100		mA
R_{on5}	High Side Driv. ON Resistance	10V < V_S <30V		0.6		Ω
$I_{out5\ o\ l}$	Output Current in Open Load Diagnostic	IN1 = IN2 = IN3 = IN4 = L; DRQ = H EN = H		-10		mA
$I_{out1/2}$ $I_{out3/4}$ I_{out5}	Output Current Threshold for Diagnostic			±1 ±4.75 ±4.75		A A A

FUNCTIONAL DESCRIPTION

EN	IN1	IN2	IN3	IN4	DRQ	OUT1	OUT2	OUT3	OUT4	OUT5	CONDITION
0	X	X	X	X	X	T	T	T	T	OFF	Low consumption
1	0	0	0	0	0	T	T	T	T	OFF	Oper. mode OFF
1	0	0	0	0	1	*snk	*snk	*snk	*src	*src	* Open Load detection
1	0	0	1	0	X	src	T	T	snk	OFF	M1 right
1	1	1	0	0	X	snk	T	T	src	OFF	M1 left
1	1	0	1	0	X	T	src	T	snk	OFF	M2 right
1	0	1	0	0	X	T	snk	T	src	OFF	M2 left
1	0	1	1	0	X	T	T	src	snk	OFF	M3 right
1	1	0	0	0	X	T	T	snk	src	OFF	M3 left
1	1	1	1	0	X	snk	snk	snk	snk	OFF	Braking
1	0	0	1	1	X	src	T	T	snk	src	M1 right + HSD
1	1	1	0	1	X	snk	T	T	src	src	M1 left + HSD
1	1	0	1	1	X	T	src	T	snk	src	M2 right + HSD
1	0	1	0	1	X	T	snk	T	src	src	M2 left + HSD
1	0	1	1	1	X	T	T	src	snk	src	M3 right + HSD
1	1	0	0	1	X	T	T	snk	src	src	M3 left + HSD
1	1	1	1	1	X	snk	snk	snk	snk	src	Braking + HSD
1	0	0	0	1	X	T	T	T	T	src	HSD only

Note 1: T means high impedance condition; **snk** means sink condition of the output; **src** means source condition of the output

***Note 2:**
In the open load diagnostic condition the sink current of OUT1, OUT2 and OUT3 is typically +10mA. In the same condition the source current of OUT4 and OUT5 are respectively -100mA and -10mA.

TRUTH TABLE OF THE DIAGNOSTIC FUNCTION

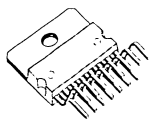
EN	IN1	IN2	IN3	IN4	DRQ	DG1	DG2	CONDITION
1	X	X	X	X	X	1	1	All ok
1	*			X	0	0	1	Overcurrent in the HB
1	X	X	X	1	0	1	0	Overcurrent in the HSD
1	0	0	0	0	1	0	1	Open Load in the HB
1	0	0	0	0	1	1	0	Open Load in the HSD
1	X	X	X	X	X	0	0	Overtemperature
1	*			1	0	0	0	Overcurrent in the HB and HSD or overtemperature
1	0	0	0	0	1	0	0	Open load in the HB and HSD or overtemperature

Notes:
*: Don't care but IN1, IN2 and IN3 must not be 0 at the same time.
HB: Half Bridges
HSD: High Side Driver

QUAD HALF-BRIDGE AND SINGLE HIGH-SIDE DRIVER

PRODUCT PREVIEW

- LOW CONSUMPTION IN STANDBY MODE (<100μA)
- TWO HALF BRIDGES FOR 3A LOAD (R_{DSON} = 0.25Ω TYP; T_j = 25°C)
- TWO HALF BRIDGES FOR 0.5A LOAD (R_{DSON} = 2.5Ω TYP; T_j = 25°C)
- HIGH SIDE DRIVER FOR 2.5A LOAD (R_{DSON} = 0.45Ω TYP; T_j = 25°C)
- DIRECT CONTROLLED BY μC (MULTIPLEX SYSTEM)
- OUTPUT HIGH/LOW LEVEL DIAGNOSTIC
- OVERCURRENT SWITCH OFF AND DIAGNOSTIC
- OVERTEMPERATURE DIAGNOSTIC BEFORE SWITCH OFF
- OPEN LOAD DIAGNOSTIC



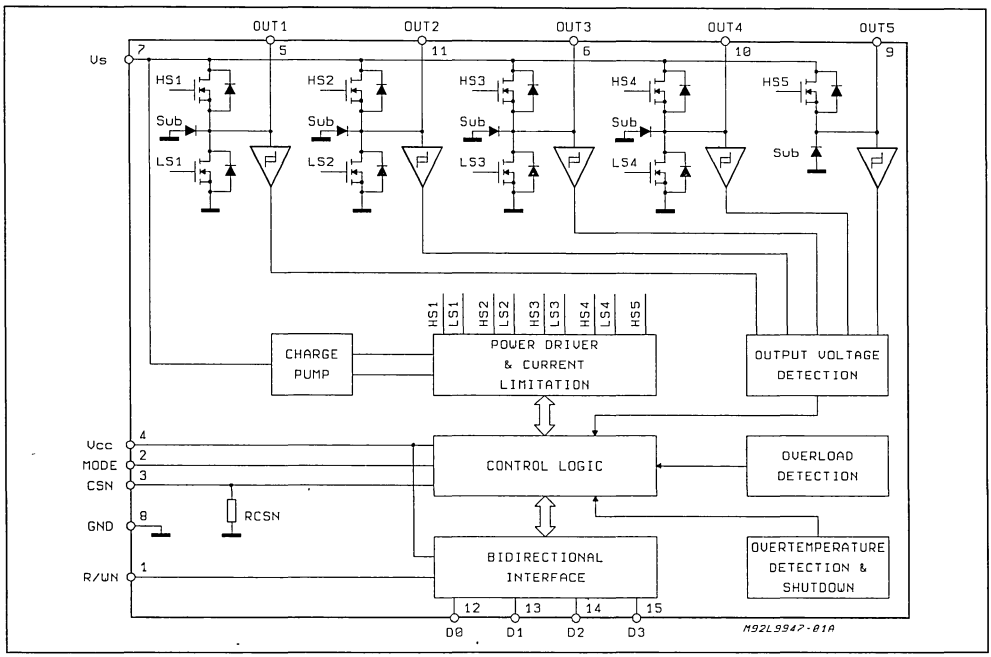
Multiwatt 15

ORDERING NUMBER: L9947

DESCRIPTION

The L9947 is a bus controlled power interface intended for automotive applications realized in multipower BCD60II technology. Up to three DC motors and one grounded resistive load can be driven with its four half-bridge and one high-side driver power outputs. The microcomputer compatible bidirectional parallel bus allows several interfaces connected on the same bus (multiplex system). The full diagnostic information is available on the bus.

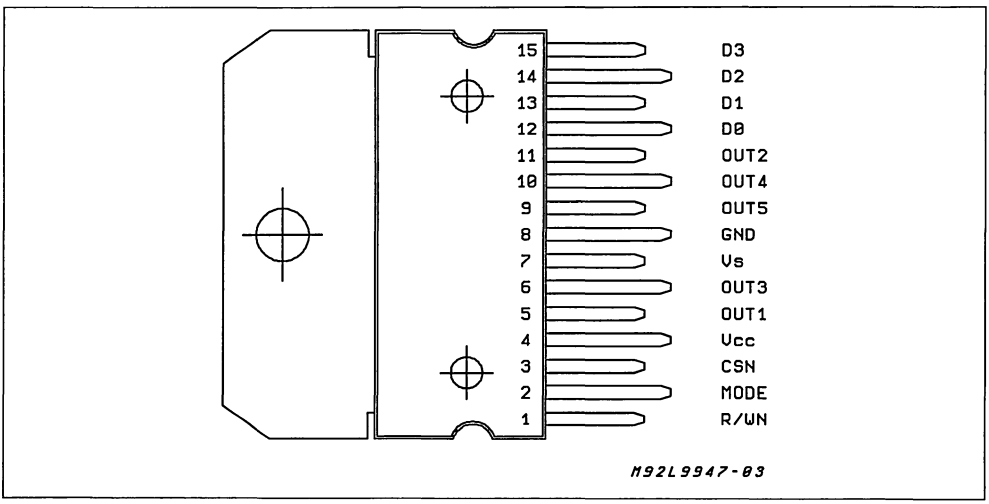
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	26	V
	Single Pulse t_{max} < 400ms	40	V
I_S	Negative Supply Current	-9	A
V_{CC}	Stabilized Supply Voltage	-0.3 to 6V	V
V_{CSN}, $V_{R/WN}$ V_{MODE}	Digital Input Voltage	-0.3 to V_{CC}+0.3	V
V_{D0-D3}	Digital Input/ Output Voltage	-0.3 to V_{CC}+0.3	V
$I_{OUT1-OUT5}$	Output Current Power	internal limited	
T_j	Operating Junction Temperature	-40 to 150	°C
T_{j-SD}	Thermal Shutdown Junction Temperature	min 150	°C
T_{j-HYS}	Thermal Junction Temperature Hysteresis	20	K

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction Ambient P_{tot} = 25W; free air; DC	38	°C/W
$Z_{th\ j-amb}$	Thermal Resistance Junction Ambient still air; single pulse tp=20s	10	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 8 to 16V; V_{CC} = 4.5 to 5.5V; T_j = -40 to 150°C;unless otherwise specified; the voltage are refered to GND and currents are assumed positive, when the current flows into the pin.)

SUPPLY:

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC}	DC Supply Current	V_S = 16V; V_{CC} = 5.5V; (status 8)		5		mA
I_S	DC Supply Current	V_S = 16V; V_{CC} = 5.5V; (status 8)		10		mA
I_{CC} + I_S	Sum Supply Current	I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0; Standby (status 2)V_S = 14V; V_{CC} = 5.5V;			100	µA
		V_S < 14V; V_{CC} = 5.5V; I_{OUT} = 0; (status 17);			1	mA
V_{SOVT}	Overvoltage Shutdown Threshold		17		25	V

CONTROL INPUTS: CNS, R/WN, MODE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{INL}	Input Low Level	V_{CC} = 5V			1.5	V
V_{INH}	Input High Level	V_{CC} = 5V	3.5			V
V_{INHyst}	Input Hysteresis	V_{CC} = 5V;	0.5			V
I_{INL}	Input Current Low	V_{CC} = 5V; V_{IN} = 0	-10		10	µA
I_{INH}	Input Current High (with exception of CSN Input)	V_{CC} = 5V; V_{IN} = 5V	-10		10	µA
R_{CSN}	Input Resistance to GND (pull down at CSN pin)		20			KΩ

DATA INPUT: D0 - D3

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DINL}	Input Low Level	V_{CC} = 5V; MODE = 0			1.5	V
V_{DINH}	Input High Level	V_{CC} = 5V; MODE = 0	3.5			V
$V_{DINHyst}$	Input Hysteresis	V_{CC} = 5V; MODE = 0	0.5			V
I_{DINL}	Input Current Low	V_{CC} = 5V; V_{IN} = 0	-10		10	µA
I_{DINH}	Input Current High	V_{CC} = 5V; V_{IN} = 5V	-10		10	µA

DATA OUTPUT: D0 - D3

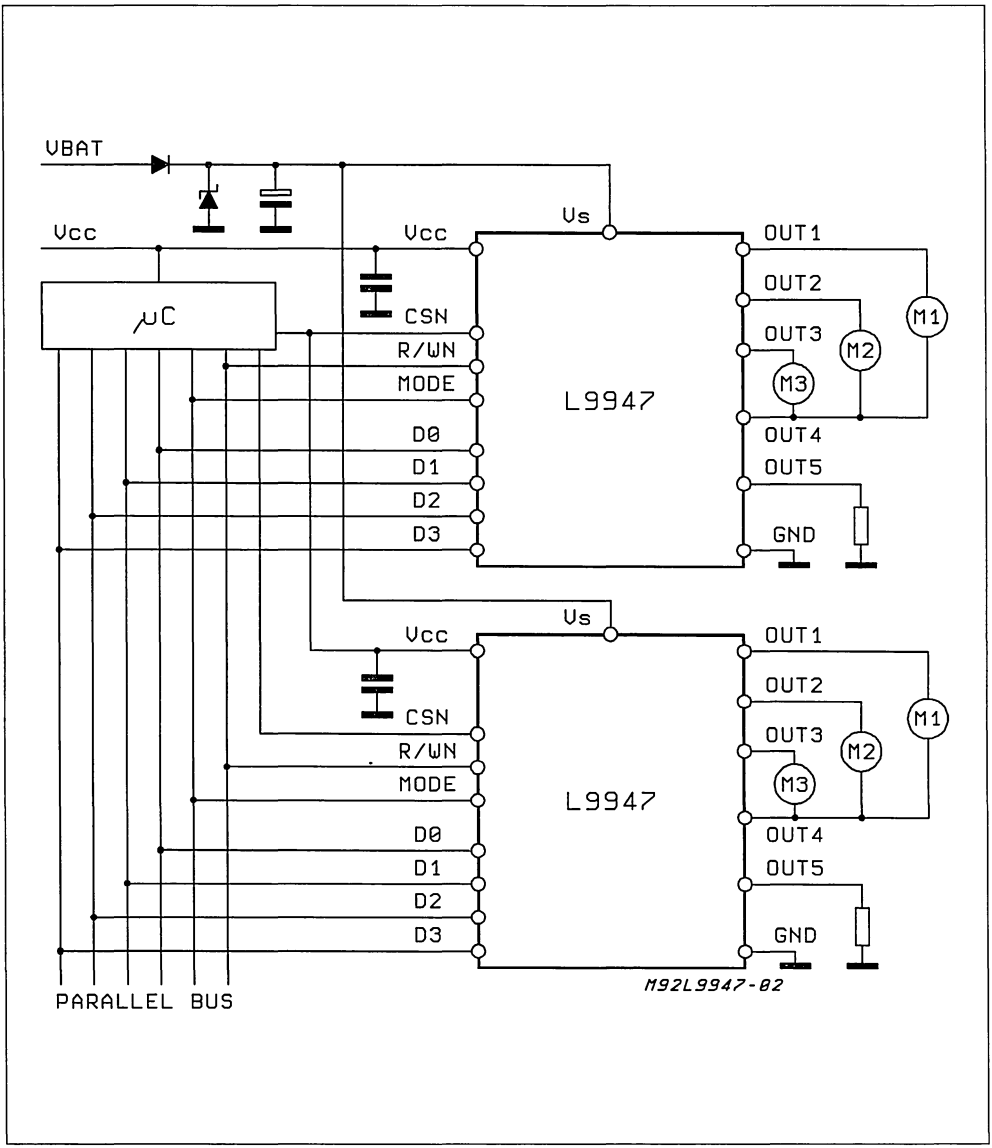
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DOL}	Output Low Level	V_{CC} = 5V; I_D = 0.5mA; MODE = 1			0.6	V
V_{DINH}	Input High Level	V_{CC} = 5V; I_D = 0.5mA; MODE = 1	4			V

ELECTRICAL CHARACTERISTICS (continued)
OUTPUTS:

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$R_{ON\ OUT1}$	On Resistance to Supply or GND	V_S = 8V; T_j = 125°C; I_{OUT} = ±0.5A			6	Ω
		V_S ≥10V; T_j = 125°C; I_{OUT} = ± 0.5A			3.95	Ω
$R_{ON\ OUT2}$	On Resistance to Supply or GND	V_S = 8V; T_j = 125°C; I_{OUT} = ±0.5A			6	Ω
		V_S ≥ 10V; T_j = 125°C; I_{OUT} = ± 0.5A			3.95	Ω
$R_{ON\ OUT3}$	On Resistance to Supply or GND	V_S = 8V; T_j = 125°C; I_{OUT} = ±2.5A			600	mΩ
		V_S ≥ 10V; T_j = 125°C; I_{OUT} = ± 2.5A			395	mΩ
$R_{ON\ OUT4}$	On Resistance to Supply or GND	V_S = 8V; T_j = 125°C; I_{OUT} = ±2.5A			600	mΩ
		V_S ≥ 10V; T_j = 125°C; I_{OUT} = ± 2.5A			395	mΩ
$R_{ON\ OUT5}$	On Resistance to Supply	V_S = 8V; T_j = 125°C; I_{OUT} = -2A			1.0	Ω
		V_S ≥ 10V; T_j = 125°C; I_{OUT} = -2A			0.7	Ω
$\|I_{OUT1}\|$	Output Current Limitation to Supply or GND	For the function of the short circuit current limitation see the functional description (pag....)	0.67		2	A
$\|I_{OUT2}\|$	Output Current Limitation to Supply or GND		0.67		2	A
$\|I_{OUT3}\|$	Output Current Limitation to Supply or GND		4		12	A
$\|I_{OUT4}\|$	Output Current Limitation to Supply or GND		4		12	A
$\|I_{OUT5}\|$	Output Current Limitation to GND		2.5		7.5	A
I_{OUT1}	Output Current	V_{OUT1} =2.5V; (status 18)	5		15	mA
I_{OUT2}	Output Current	V_{OUT2} =2.5V; (status 18)	5		15	mA
I_{OUT3}	Output Current	V_{OUT3} =2.5V; (status 18)	5		15	mA
I_{OUT4}	Output Current	V_{OUT4} =2.5V; (status 17)	80		500	mA
		V_{OUT4} =V_S -2.5V; (status 16 or 18)	-80		-500	mA
I_{OUT5}	Output Current	V_{OUT5} =V_S -2.5V; (status 18)	-5		-15	mA
V_{OUT1-5}	Output Voltage Detection Thresholds	V_S=13V; (status 11) LOW HIGH HYSTERESIS	 4.9 7.5	 0.4 V_S 0.6 V_S 0.2 V_S	 5.5 8.1	 V V V
T_{JOT}	Overtemperature Detection Thresholds	status 12 - 15		130		°C
		steady state t >20ms	125		<T_{JSD}	°C
t_{ISC}	Overcurrent Switch off Time		50			µs
f_{OSC}	Internal Oscillator Frequency			250		KHz

APPLICATION CIRCUIT DIAGRAM

Fogure 1: Recommended Application Circuit.



FUNCTIONAL DESCRIPTION

The L9947 is a power interface circuit designed for a multiplex system controlled by a parallel µC bus. The bus consists of four bidirectional data wires D0 - D3 and three control wires read/write (R/WN), mode (MODE) and chip select (CSN).

The device needs two supply voltages. The first voltage supplies the half bridges, high side driver and its driving part. The second one is a 5V stabilized supply. The function of the device in the typical operating modes is described in the following tables.

Output Activating/write Table 1

Status	CSN	R/WN	MODE	D0	D1	D2	D3	OUT1	OUT2	OUT3	OUT4	OUT5	FUNCTION
1	1	X	X	X	X	X	X	AB	AB	AB	AB	AB	Hold output behavious as programmed before
2	⊔	0	0	0	0	0	0	T	T	T	T	T	All Outputs, Standby mode
3	⊔	0	0	0	0	1	0	SRC	T	T	SNK	T	M1, right
4	⊔	0	0	1	1	0	0	SNK	T	T	SRC	T	M1, left
5	⊔	0	0	1	0	1	0	T	SRC	T	SNK	T	M2, right
6	⊔	0	0	0	1	0	0	T	SNK	T	SRC	T	M2, left
7	⊔	0	0	0	1	1	0	T	T	SRC	SNK	T	M3, right
8	⊔	0	0	1	0	0	0	T	T	SNK	SRC	T	M3, left
9	⊔	0	0	1	1	1	0	SNK	SNK	SNK	SNK	T	Braking
10	⊔	0	0	0	0	0	1	T	T	T	T	SRC	High side driver

Notes:
Where CSN = 0 the device is (for t ≤ 100µs) transparent, in this condition any change of Data D0 .... D3 will lead to the apprpriate output response.
Deselecting the circuit (CSN ⊓) the last programmed status will be stored.

Diagnostic / read. Table 2:
In readout modes the port D0 .... D3 is acting as an output showing the conditions detected before.

Status	CSN	R/WN	MODE	D0	D1	D2	D3	Function
11	⊔	1	0	OUT1	OUT2	OUT3	OUT4	OUT1, OUT2, OUT3, OUT4;
12	⊔	1	1	0	0	OT	OUT5	No failure, OT, OUT5;
13	⊔	1	1	1	0	OT	OUT5	OVC1, OT, OUT5;
14	⊔	1	1	0	1	OT	OUT5	OVC2, OT, OUT5;
15	⊔	1	1	1	1	OT	OUT5	OVV or OVV + OVC1 or OVV + OVC2 OT, OUT5;

Diagnostic / write. Table 3:
Diagnostic modes are used to check the load status for broken or shorted wires.

Status	CSN	R/WN	MODE	D0	D1	D2	D3	OUT1	OUT2	OUT3	OUT4	OUT5	Function
16	⊔	0	1	0	1	0	X	T	T	T	140mA SRC	T	
17	⊔	0	1	1	0	0	X	T	T	T	140mA SNK	T	$I_S+I_{CC} \leq 1mA$ for $I_{OUT4} = 0$
18	⊔	0	1	0	1	1	X	10mA SNK	10mA SNK	10mA SNK	140mA SRC	10mA SRC	

Standby and clear / write. Table 4:

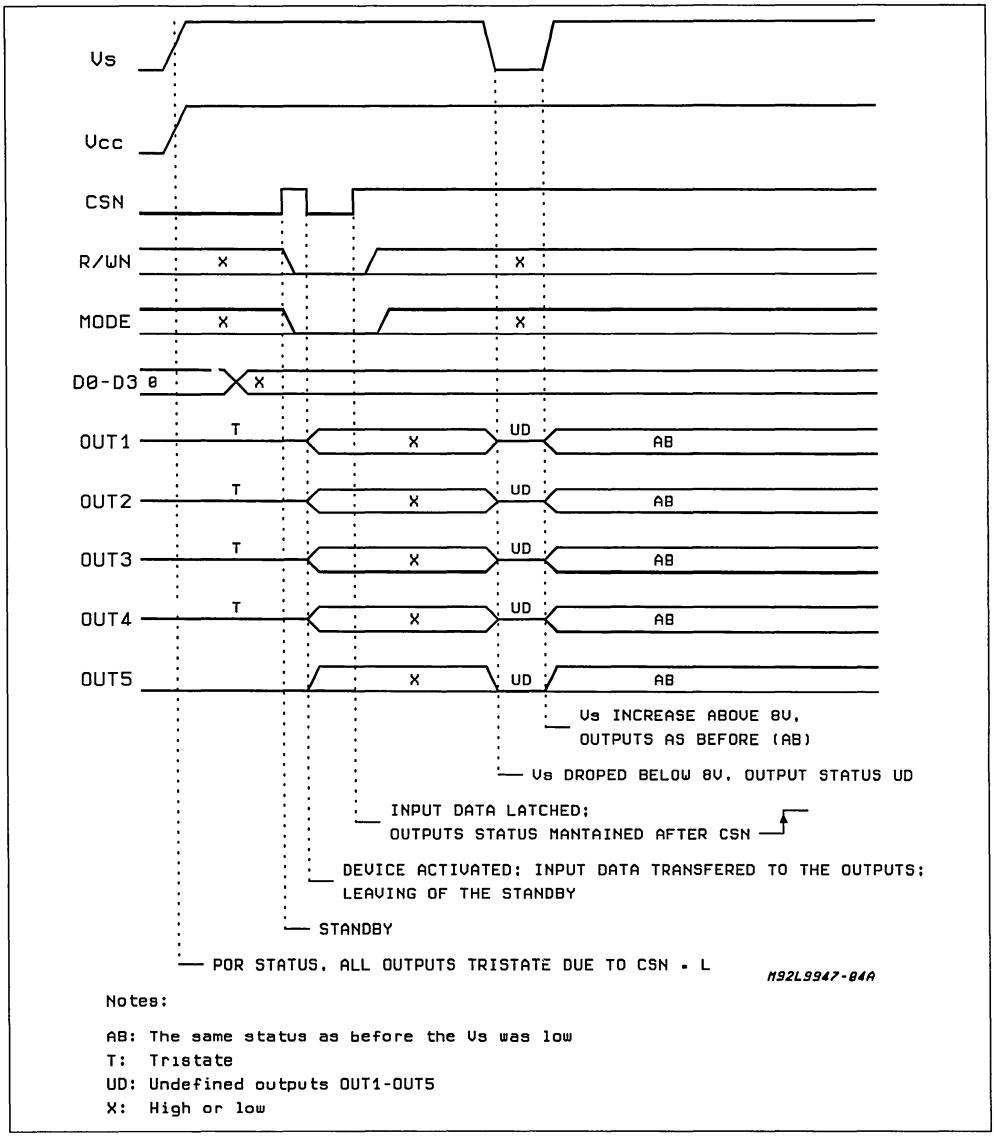
Status	CSN	R/WN	MODE	D0	D1	D2	D3	OUT1	OUT2	OUT3	OUT4	OUT5	Function
19	⊔	0	0	1	1	1	1	T	T	T	T	T	Clear
20	0	X	X	X	X	X	X	T	T	T	T	T	Clear, Static CSN = 0 will force clear status and standby after 100µs without respect of data inputs

Symbols:
1: Logic High
0: Logic Low
T: Tristate
X: Don't care

AB: As before
⊔ Low pulse t < 100µs
SRC: Source
SNK: Sink
OT: Overtemperature

OVC1: Overcurrent 1
OVC2: Overcurrent 2
OVV: Overvoltage
OUTX:
- High if output voltage was >0.6V_S during test
- Low if output voltage was < 0.4V_S during test

Figure 2: System Startup Sequence



SYSTEM STARTUP (figure 2)

It is not mandatory that Vs is present before Vcc. With the presence of the Vcc the internal logic would be reseted and the system restarts under control of the inputs. If CSN = 0 for more than 100µs after the presence of Vcc the standby mode is activated. Standby is also activated when the CSN and VCC would be high at the same time. When CSN = 0 and Vcc goes up, the device is not controlled by the bus. The outputs remain in tristate but the current consumption is larger than 100µA. A high - low - signal at the CSN - wire is mandatory to control the outputs. There is no undervoltage detection level for the supply voltage VS implemented. The VCC should be supplied from the same voltage supply as the driver of the D0 -D3 pins (eg. µC).

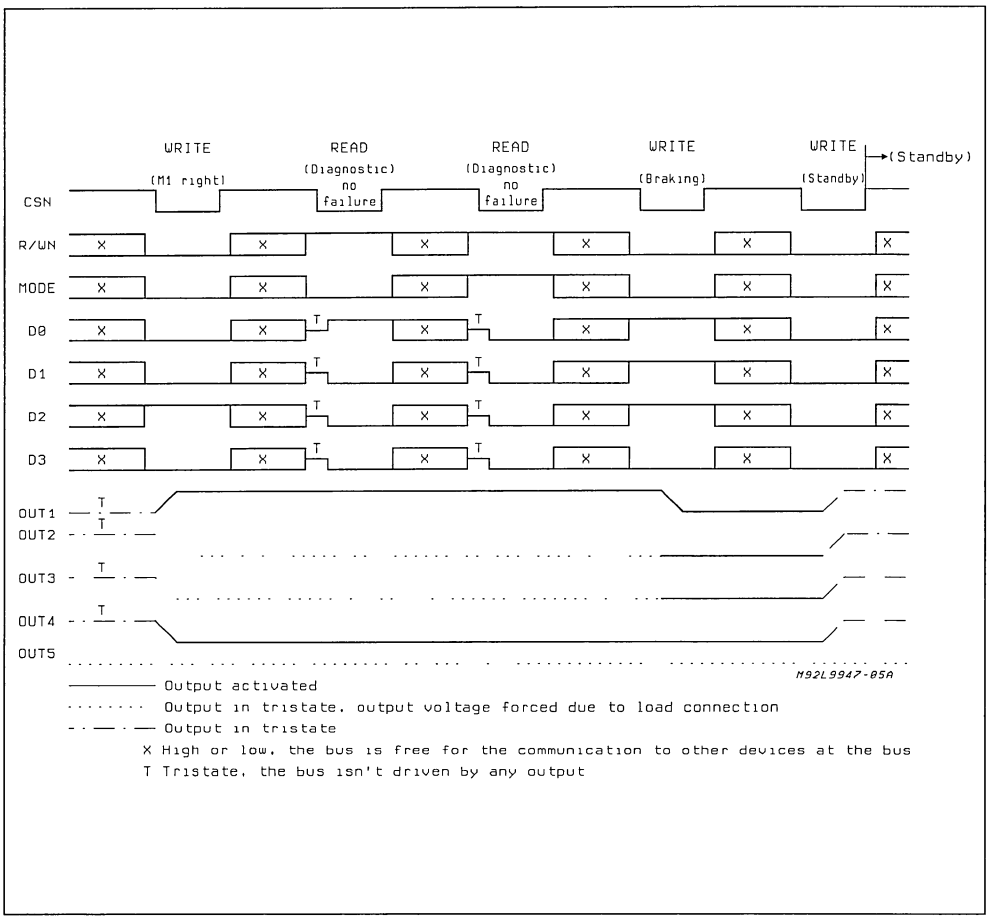
DATA TRANSFER AND OUTPUTS ACTIVATING (Figure 3)

The half bridges of OUT1, OUT2 and OUT3 can be used with OUT4 to drive three bidirectional motors in full bridge configuration as shown in fig.1 Only one motor can be driven in the same time. The µC writes the corresponding word status 1 till 10 at the bus and latch it with a low pulse in the L9947. So the motor is activated. To stop the motor it is useful to insert a braking phase (status 9). In the braking condition there are all low side DMOS of the half bridges switched-on in this case the flyback currents flows through the low side switches instead of the intrinsic diodes of the half bridges. After that, the half bridges could be switched in tristate (T). The high side driver, OUT5 can be switched only when all the half bridges are in tristate status 10.

The µC works always as master and the L9947 Power Interface as slave. That means: the µC starts the communication between the Power Interface and itself with low transition at the CSN line. CSN = 0, R/WN= 0 the L9947 reads the data at the bus and execute the command as shown in tables 1,3,4 (write mode). The high slope of the CSN stores the last command and execute it further. All inputs are disabled if CSN= 1.

So the bus can be used for another device. With CSN = 0 and R/WN = 1 the L9947 writes the status of the diagnostic at the parallel bus until CSN becomes high (table 2; status µ + 15) (read mode). The power outputs maintain the same status as before.

Figure 3: Signal sequence for data transfer to switch M1 right, read the output status, brake the motor and activate the standby mode.



BUS TIMING (figure 4)

The bus signal must be defined t_3 = 1µs before CSN goes low. It is allowed to change the level of R/WN during CSN = 0. The other signals could be changed. To store a command it is mandatory to fix the D0 - D3 and MODE signals t_9 = 1µs before the positive edge of CSN.

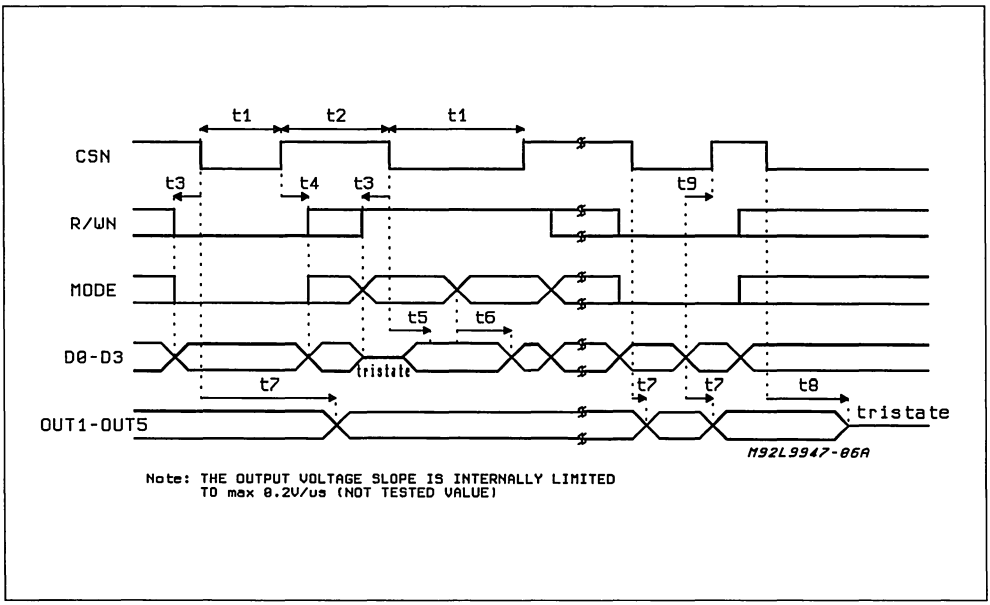
OVERCURRENT AT OUT1 - OUT5:

The output currents of OUT1 - OUT5 are internally limited. This is realized in the following way:

When the output current reaches a certain level (see pag...) the Gate - Source voltage will be clamped to a lower level. The output current is now limited and follows the output ID, UDS characteristic for this Gate - Source voltage. An internal timer starts when the output voltage drop (Drain - Source) increases above 0.4Vs.

After 100µs typ. the output is switched OFF and the corresponding overcurrent bit (OVC1 or OVC2) will be set. The outputs can be activated again with the next input data word.

Figure 4: Bus and Outputs Timing Diagram



TIMING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Width of CSN Low	20		90*	µs
t_2	Width of CSN High	10			µs
t_3	Input Signals Before Negative Cdge of CSN	1			µs
t_4	Input Signals After Positive Edge of CSN	1			µs
t_5	Valid Diagnostic Data			10	µs
t_6	Valid Diagnostic Data			10	µs
t_7	Delay Time from Input to Power Output, VS = 13V			300	µs
t_8	CSN = Low Duration (Pulse Length) for CLEAR of latched Data	100			µs
t_9	Input Data Before Positive Edge of CSN Which Should be Latched	1			µs

t_1 and t_5 are derived from the internal oscillator frequency

t_7 varies with the supply voltage V_S, relating to the output voltage slope limitation

(*) for $t_1 \geq 100\mu s$ the latched data will be reseted due to CLEAR (status 20)

DIAGNOSTIC (TABLE 2; STATUS 11 - 15):

The diagnostic delivers the information of the output voltage status (high or low) at the outputs OUT1 - OUT5, overcurrent, overvoltage shutdown and over temperature. The output voltage detection is done by hysteresis comparators with thresholds at 0.4VS and 0.6 VS. The overcurrent (OVC) information is latched till a new or repeated write command was received. The OVC1 is set to high with the overcurrent condition at any of the half-bridge outputs. OVC2 error bit will be set with the overcurrent condition at OUT5. The overvoltage (OVV) is high till the supply voltage Vs exceeds the overvoltage threshold of 20V typ.
The overtemperature (OT) is high if the junction temperature is less than typ. 30 Kevin below the thermal shutdown junction temperature (T_{JSD}).

DETECTION OF LOAD INTERRUPTION (TABLE 3):

The outputs OUT1 - OUT4 are connected by the motors in the application. The output OUT4 can be switched as current source or sink with typ. 140mA current capability (status 16 + 17). The sum of current consumption is <1mA if the output current I_{OUT4} = 0 (status 17). The diagnostic of the output voltage delivers the information if one or more of the half bridges is shorted to Vs or GND or the motor connections are interrupted. In status 18 the outputs OUT1 - OUT3 are switched as current sinks (typ. 10mA), OUt4 and OUt5 as current sources (OUT4 140mA, OUT5 10mA). With this current the influence of leakage currents and oxidized contacts is eliminated.

STANDBY (TABLE!; STATUS 2):

The L9947 is set in standby mode with the positive edge of CSN when all other inputs are low. All latched data will be cleared and the inputs and outputs are in tristate.
The total current consumption is less than 100µA. CSN=0 quits the standby. All latched data are cleared.

CLEAR (TABLE 4: STATUS 20):

If the chip select is low for ore than T_{CLR} = 100µs, the internal latched data will be cleared and the outputs become tristate. Repetitive high low edges activate the inputs again. Also a broken CSN-wire activates this clear function due to the internal pull down resistor at CSN input. After a clear, the L9947 goes in standby and can be wake up with a negative edge of CSN.

THERMAL SHUTDOWN:

When the junction temperature increases above T_{JSD} the power DMOS transistors are switched off until the junction temperature drops below the value T_{JSD} - T_{JHYST}.

CLAMP CURRENT OF THE POWER OUTPUTS:

For output voltages 10V and larger a clamp current of appr. 50µA will flow in the power outputs due to the internal gate-source voltage limitation, when the device is not in standby.

OVERVOLTAGE SHUTDOWN:

When the supply voltage VS exceeds the overvoltage threshold V_{SQVT}, typ. 20V,the outputs OUT1 - OUT5 go in tristate condition. If the supply voltage goes under the overvoltage shutdown treshold, the status is the same as before the overvoltage condition occurred.

UNDERVOLTAGE:

In the voltage range 2V <Vcc < 4V the internal logic is reseted and all outputs go in tristate. Also ground spikes on the Vcc reset the logic. After an internal reset of the logic, the L9947 is controlled again by the inputs.

GROUND INTERRUPT:

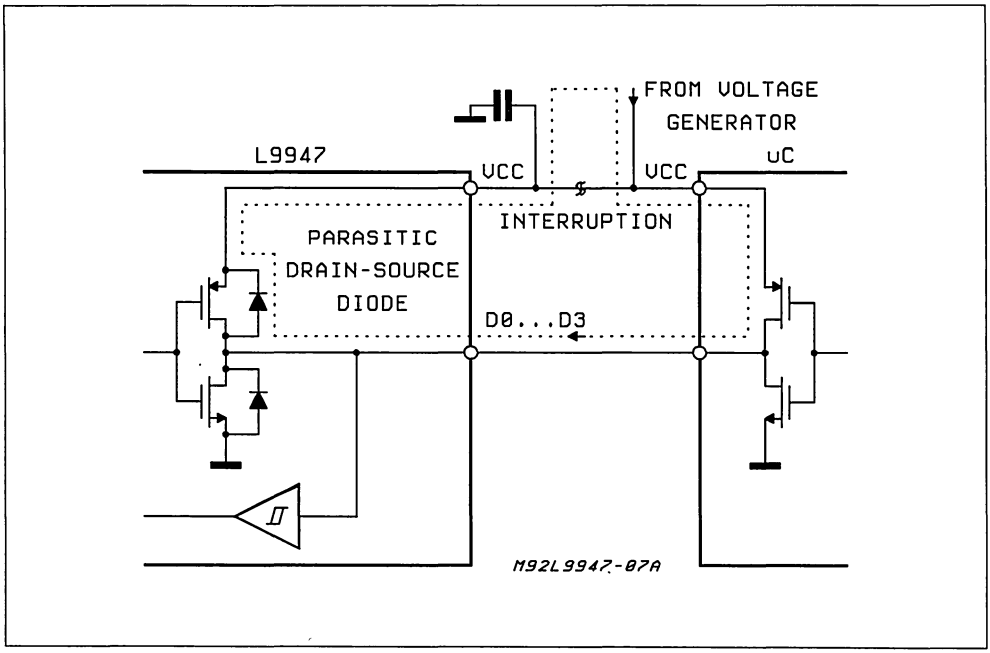
The L9947 is protected against interruption. The output OUt5 switches off at ground interruption. The outputs OUT1 - OUt4 are driven in full bridge configuration as shown in the application. There is no path through the load or direct to another ground. Thus, the device protected.

Vcc INTERRUPTION

If the supply voltage Vs is present and Vcc is interrupted or not supplied, than two cases can be distinguished:

1. The data pins D0 - D3 are not driven by the µC or they are low. So the outputs OUT1 - OUT5 and D0 - D3 are in tristate.
2. One of the pins D0 - D3 is driven high the µC. This pin supplies the VCC pin by the drain-bulk-diode of the p-channel mos (fig.5). Depending of the CSN, R/WN and MODE inputs some undesiderable functions can occur.

Figure 5: Supply Current Path at Vcc Interruption



SGS-THOMSON MICROELECTRONICS

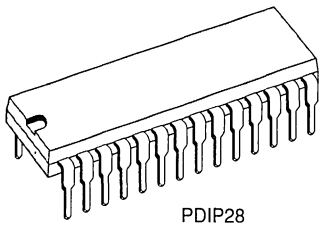
ST9560
ST9561

DATA LINK CONTROLLER FOR VEHICLE AREA NETWORK

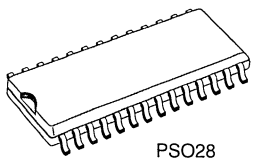
Developped with GIE PSA RENAULT

ADVANCE DATA

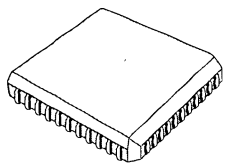
- Multimaster contention-based bus data link controller
- Fully compliant to VAN Specification ISO/TC22/SC3/WG1 Revision 4.0
- Programmable bit coding: MANCHESTER-E plus extensions to support MANCHESTER-L and pulse coding
- Supports all specified message types
- Data Field length: 0 to 30 bytes
- Programmable exchange speed up to 1.2 Mbits/s
- 16 maskable internal identifiers
- 160 bytes User RAM
- Bus access priority by message header buffer contents
- Error handling and line diagnosis
- VHDL model available
- Flexible microcontroller interface: Motorola, Intel, Z-bus, multiplexed and non-multiplexed
- Direct connection to ST9 microcontrollers
- 6 to 16 I/O lines in 44-pin version.
- 28 pin DIP and PSO (ST9560), 44 pin PLCC (ST9561) packages available



PDIP28



PSO28



PLCC44

(Ordering Information at the end of the Datasheet)

Figure 1. ST9560 Pin Configuration

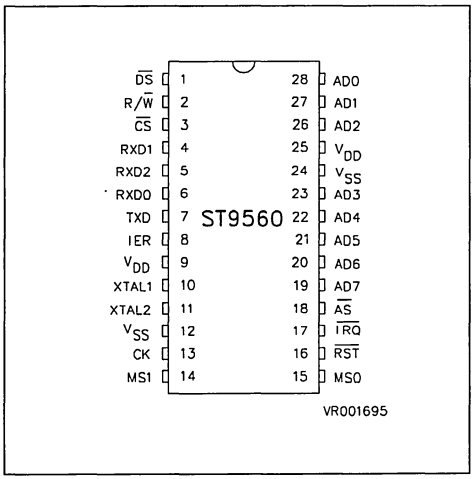


Figure 2. ST9561 Pin Configuration

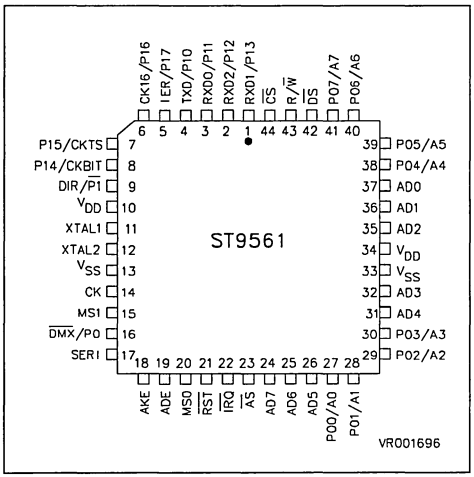
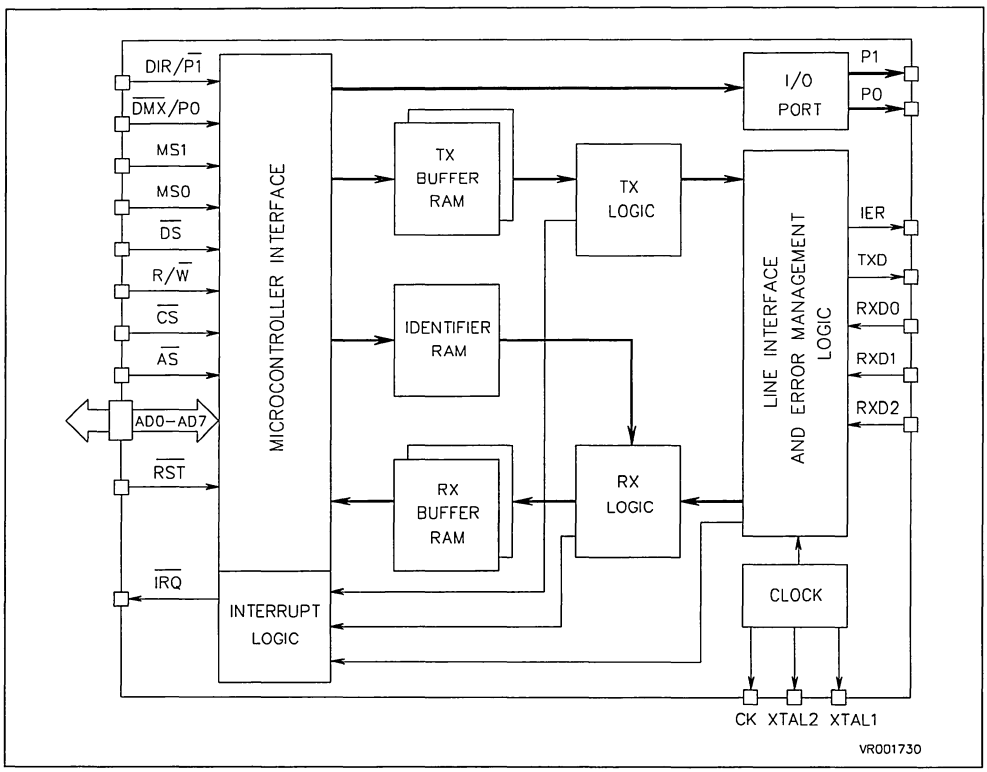


Figure 3. ST9560/ST9561 Block Diagram



GENERAL DESCRIPTION

The ST9560 and ST9561 are integrated solutions to data-link control for the Vehicle Area Network (VAN) and are fully compliant to the standard ISO/TC22/SC3/WG1 Revision 4.0. Together with a microcontroller (MCU) and the appropriate line interface circuitry, the ST9560 and ST9561 provide complete functionality for the implementation of the VAN protocol in the DATA LINK LAYER and top level of the PHYSICAL layer of the OSI communications model.

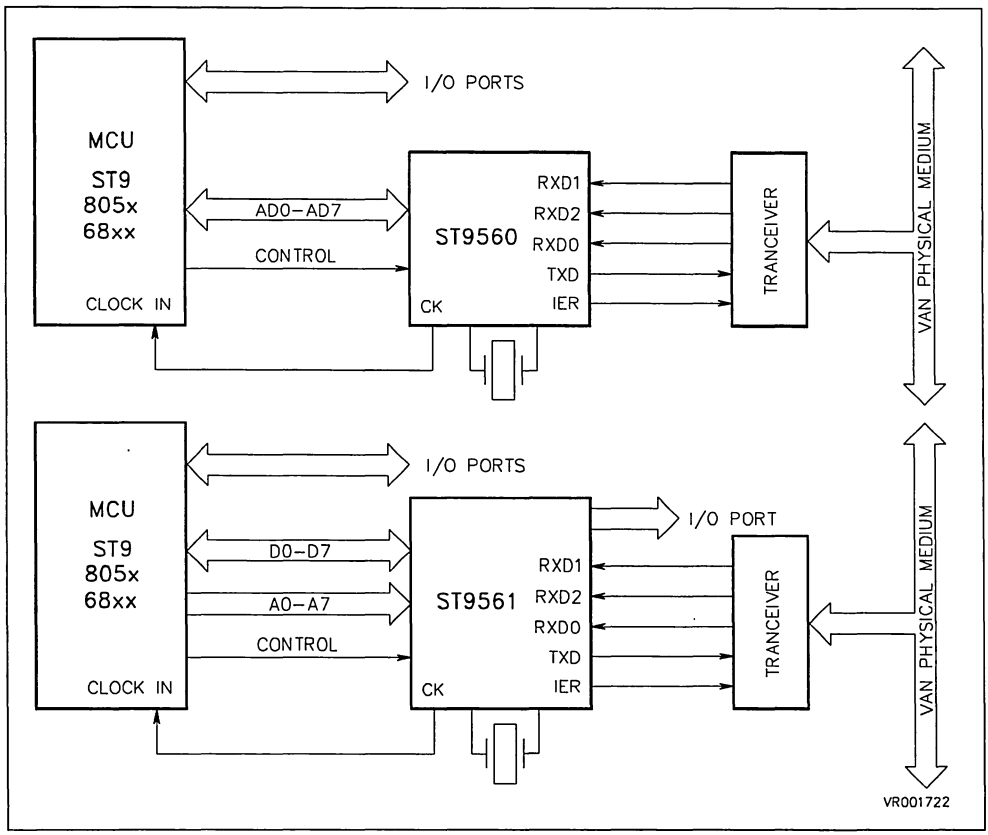
The ST9560 manages the transmission and the reception of VAN messages and also error handling (CRC, code violation detection, message frame check) and diagnosis.

The ST9560 is the 28-pin stand alone version, in Plastic Dual in Line and the Plastic SO28 Wide package, whose MCU interface is tailored for microcontrollers such as ST9, ST10 or general purpose microcontrollers using a multiplexed 8-bit address/data bus. The ST9561 is the 44-pin PLCC version with a non-multiplexed bus supplementary capability and I/O port control.

As the devices are fully compatible in their functionality, from this point on all references to the ST9560 refer to both the ST9560 and ST9561 unless otherwise noted.

The host MCU communicates with the ST9560 through 4 32-byte static RAM buffers (one or two buffers for transmit data, 2 alternate use 32-byte receive buffers).

Figure 4. ST9560 and ST9561 VAN-DLC Application Example



PIN DESCRIPTION

V_{DD}. Main Power Supply Voltage (+5V ±10%)

V_{SS}. Digital Circuit Ground

XTAL1, XTAL2. These pins connect a parallel-resonant crystal (30MHz maximum), or an external source to the on-chip clock oscillator and buffer. XTAL1 is the input of the oscillator and internal clock generator or external clock input if used; XTAL2 is the output of the oscillator.

CK. Clock output (CK is XTAL1 buffered and is not affected by the $\overline{RST}$ input).

MS1, MS0. Microcontroller Bus Mode select inputs

MS1	MS0	MCU Bus Type
0	0	Motorola like
0	1	Intel like
1	0	Z-bus like (ST9)
1	1	Reserved

$\overline{CS}$. Chip Select input (active low)

R/$\overline{W}$. In Motorola and Z-bus modes, Read/Write input low = write from MCU). In Intel mode, Write Transfer synchronisation input (active low).

$\overline{DS}$. In Motorola and Z-bus modes, Data Strobe input. In Intel mode, Read Transfer synchronisation input (active low).

$\overline{AS}$. Address Strobe input (active low in Z-bus mode, active high in Motorola and Intel modes)

$\overline{RST}$. Reset input (active low)

$\overline{IRQ}$. Interrupt output (push-pull, active low)

AD0-AD7. Multiplexed Address/Data Bus.
Data bus in non-multiplexed mode of ST9561.

The ST9560 provides the following additional pins:

RxD2, RxD1, RxD0. VAN bus Serial inputs from receiver device.

TxD. Serial output.

IER. Reset output for the VAN bus driver device.

The following pins are available on the ST9561 only.

DIR/$\overline{P1}$. Port 1 configuration
When DIR/$\overline{P1}$ = '0', Port 1 is reconstructed.
When DIR/$\overline{P1}$ = '1', Port 1 takes the Alternate VAN interface functions.
This pin includes an internal pull up.

TXD/P10. Serial output

RXD0/P11. VAN bus serial input

RXD2/P12. VAN bus serial input

RXD1/P13. VAN bus serial input

CKBIT/P14. Sample clock bit of sampled data

CKTS/P15. Time slot Clock

CK16/P16. F_{base} Clock

IER/P17. Reset output for bus driver

$\overline{DMX}$/P0. Port 0 configuration
When $\overline{DMX}$/P0 = '0', Port 0 is used as address bus (non-multiplexed micro interface)
$\overline{DMX}$/P0 = '1': Port 1 is reconstructed
This pin includes an internal pull-up.

P00-P07. General Purpose 8-bit I/O port in standard mode, Address Bus I/O in non-multiplexed mode.

SERI. Serial output decoded VAN data.
(IDEN, COM, DATA)

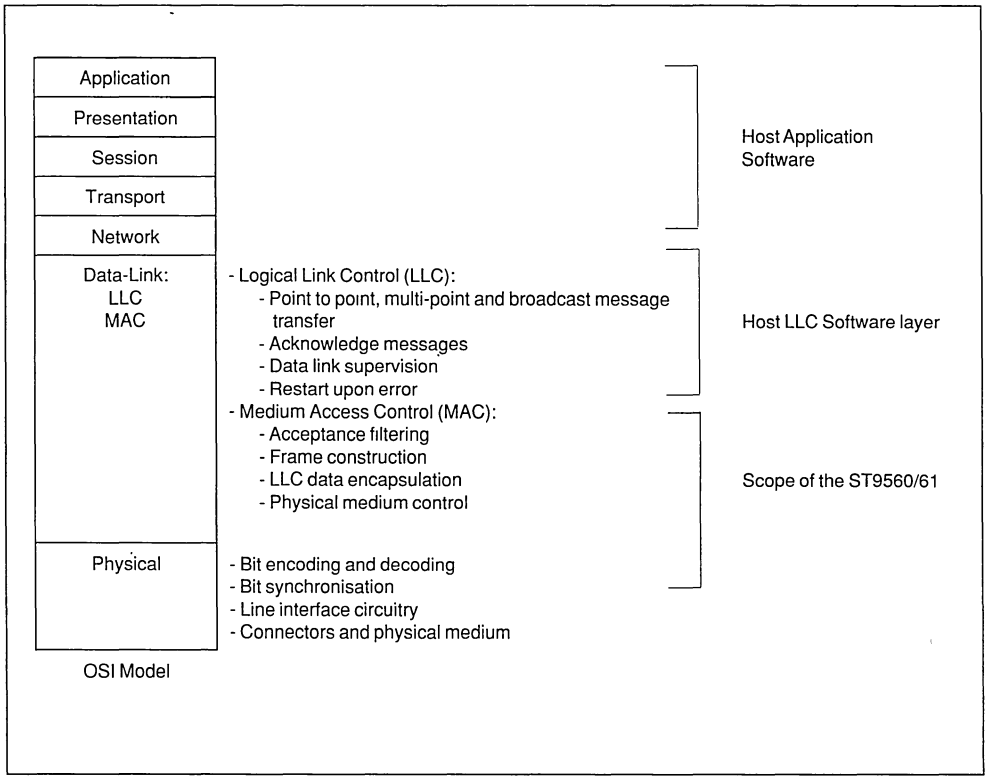
ADE. When bit MASK of register MRR is set and ADE = '1' , the frame passes the acceptance filter.

AKE. When bit MASK of register MRR is set and AKE = '1' , an acknowledge is sent.

O.S.I. MODEL AND ST9560/61

The Open System Interconnection model standardized by ISO is subdivided into 7 functionnal layers. The scope of the VAN standard, as submitted to ISO/TC22/SC3/WG1, is the Data Link and the Physical layers (see Figure 5). The Data Link layer is in turn subdivided into 2 sub-layers, the Medium Access Control (MAC) and the Logical Link Control (LLC). The ST9560/61 handles the MAC sub-layer and the upper part of the Physical layer (bit encoding/decoding). The LLC sub-layer and the upper layers of the OSI model are handled by the host processor software.

Figure 5. VAN description according to the OSI model and scope of the ST9560/61



FUNCTIONAL OVERVIEW

The ST9560

ST9560 is composed of nine major blocks: (see block diagram)

- Memories (XBF0, XBF1, RBF0, RBF1, IDEN)
- Micro interface with interrupt logic
- Interface Management Logic (transmit and receive)
- Bit Stream Processor (transmit and receive) - Transceiver Control Logic
- Error Management Logic
- Bit Timing Logic and clock circuitry
- Diagnosis circuitry
- I/O ports.

Memories

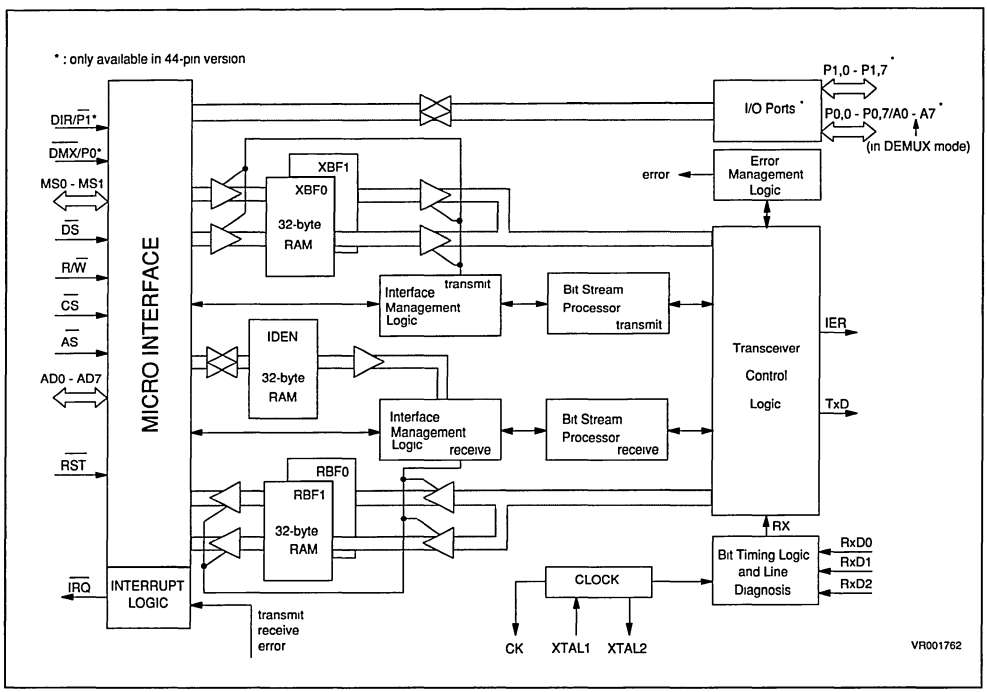
The host MCU stores the frames to transmit in a 32-byte static RAM used as a transmit buffer (XBF0 or XBF1 according to user choice). Received frames are loaded by the ST9560 in a double 32-byte static RAM (RBF0 and RBF1), transparently seen as only one buffer from the MCU interface (the user can select the first and the last transmit byte addresses, thus choosing the size of the data message).

In addition to DATA memories containing the frame buffers, a 32-byte RAM (IDEN) containing up to 16 identifiers is provided.

A set of 18 registers including status, command and identifier masks allows the host to manage the serial interface operation.

For the ST9561, another set of 6 registers allows the host the control of two 8-bit (maximum size) I/O ports.

Figure 6. Detailed Block Diagram



FUNCTIONAL OVERVIEW (Continued)

ST9560 Micro Interface

Two versions are provided:

- a 28-pin stand alone version (ST9560), whose micro interface is tailored for micro such as ST9, ST10 or general purpose microcontrollers using a multiplexed 8-bit address/data bus. The host communicates with ST9560 with 32-byte ram buffers (one or two buffers for transmit data, 2 alternate-use 32-byte receive buffers),
- a 44-pin version (ST9561) with non-multiplexed bus supplementary capability for host processors with non-multiplexed buses and I/O port control.

Direct interface to three popular MCU buses is configurable by two mode select lines, MS0 and MS1. These lines are to be hardwired to a logic one or zero in the application circuit to suit the bus configuration of the host.

Interface Management Logic

The interface management executes commands from the host and controls the data transfers on the serial bus.

Control, status and interrupt registers are used by the interface management.

Bit Stream Processor (BSP)

The bit stream processor controls the data stream between the interface (parallel data) and the serial bus.

A 32-byte identifier RAM contains up to 16 identifiers. When a message is received, the bit stream processor reads the identifiers loaded in RAM and performs the acceptance filter function. The identifier, command and data field are stored in RAM only if the message has an identifier which passes the acceptance filter.
The processor controls reception, arbitration, transmission and error signalling. The ST9560 cannot transmit in-frame responses.

Timing Logic

This block performs the synchronization functions according to the VAN specification. Each data bit is encoded and decoded according to its time slot representation. The rules of synchronization depend on the received signal.

Transceiver Control Logic

This block consists of bit coding/decoding according to the programmed type of encoding.

Error Management Logic

The different types of error (monitoring, CRC, code violation) are reported by the Bit Stream Processor and are passed to the interrupt management logic.

Diagnosis

This block monitors the states of the TXD and the three RxDi inputs (i = 0-2) and processes the sampled data in order to diagnose any potential VAN bus defects.
According to user choice (as under program control) degraded transmission modes can be chosen.

The three RxDi inputs provide different information on the VAN bus. RxD0 give the true differential logical information. RxD1 and RxD2 provide logical information from each of the two bus wires (using a threshold operation). The diagnosis logic performs the following functions.

- Digital filtering (on successive samples) in order to eliminate noise spikes.
- Transition analysis (synchronous, asynchronous protocol).
- Decision logic in order to select (automatically or not) a degraded mode (monofilar) or to detect that transmission is impossible and to go back to the normal differential mode using the TOP DIAG clock.

Control and status bits are provided to manage the operation of the diagnosis logic.

Clock Generator

The on-chip clock generator consists of an oscillator and clock divider register. The buffered output of the oscillator is passed through the CK pin. The optimum use of this signal is to drive the oscillator of the host MCU, reducing the need for a second oscillator circuit.

I/O Ports

The ST9561, 44-pin version, contains two additional standard 8-bit I/O ports.

Port 0 can be used as a standard I/O port when the multiplexed bus is used, allowing recreation of the host port used for the 9560 interface, or as the LSB byte address inputs A0-A7 if the non-multiplexed mode is selected.

Port 1 can be used as a standard 8-bit I/O port, or to output the VAN interface signals.

The ST9561 I/O ports are controlled via data registers (one per port) and configuration registers (two per port).

VAN OVERVIEW

In order to better understand the function of the ST9560, a short description of the relevant parts of the VAN protocol is provided here.

The VAN bus.

The VAN protocol implemented in the ST9560 is a superset of the standard ISO/TC22/SC3/WG1 version 4.0 and uses an access method which is multi-access based on non-destructive collision with bit-wise arbitration. All data is transferred inside frames.

Two consecutive frames are separated by an Inter-Frame Space. The ST9560 can send an in-frame request and process the in-frame response from another device, the ST9560 can not itself send an in-frame response.

VAN bus logical levels

The serial bus has two states: recessive and DOMINANT.

If two (or more) VAN modules send simultaneously, the resulting state of the bus is RECESSIVE only if all transmitters send recessive bits at the same time.

If one (or more) transmit dominant states, the resulting state of the bus will be DOMINANT.

Inside the ST9560 a dominant bit is represented by a logical '0' and a recessive bit by a logical '1'.

CODING / DECODING

Two types of encoding can be programmed by the host (Mode Control Register):

- MANCHESTER_L
- ENHANCED MANCHESTER (MANCHESTER-E)

Each of these two encoding modes can be combined with two time slot encoding modes:

- standard VAN (e.g. wire-based applications)
- pulsed (e.g. Optical based applications)

The base clock F_{base} is obtained from the local clock oscillator after user-programmable division.

The bit is encoded and decoded according to its time slot representation.

The Time Slot is the time duration of 16 F_{base} periods

TIME-SLOT in VAN STANDARD coding

In this type of coding a logical '0' is represented by a low state during the whole time-slot and a logical '1' by a high state during the whole time-slot.

TIME-SLOT in PULSE encoding:

In this type of coding, a logical '0' is represented by a low state during the first 1/8th of the time slot (2 periods of F_{base}).

A logical '1' is represented by a high state during the whole time slot.

Bit synchronisation

The synchronisation rule is based on the received signal edges and is the same for all the modules. During the sending of the preamble the synchronisation rule is disabled.

The 3 main points of time slot are:

- resynchronisation point (located at 2/16 of time slot duration in standard mode, at 4/16 of time slot duration in pulsed mode)
- sample point (located at 11/16 of time slot duration).
- transmit point.

Figure 7. Time slot reprsentation in VAN standard coding and pulse coding

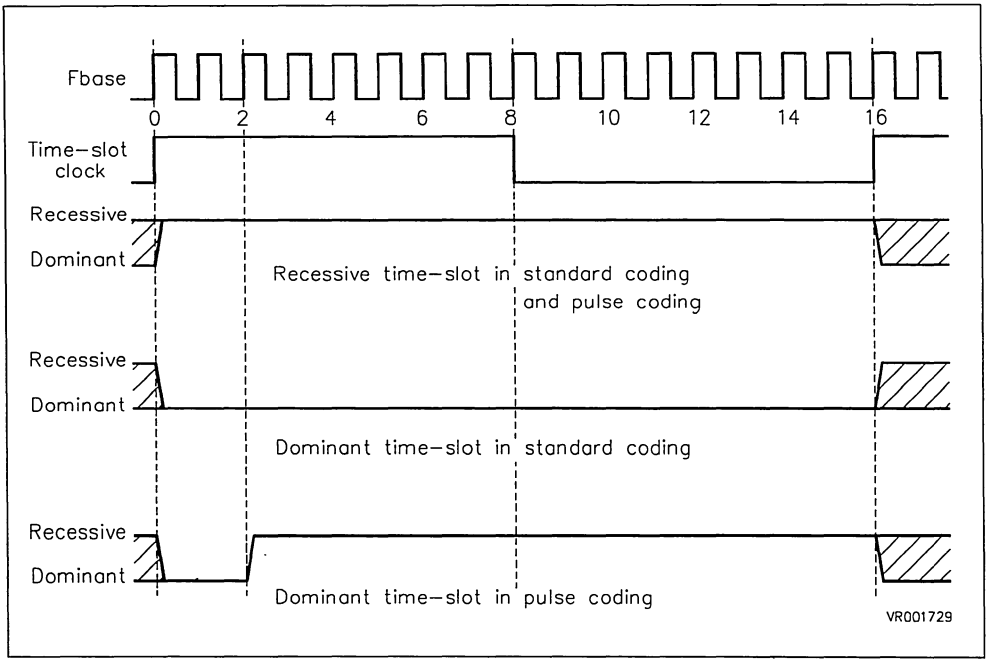
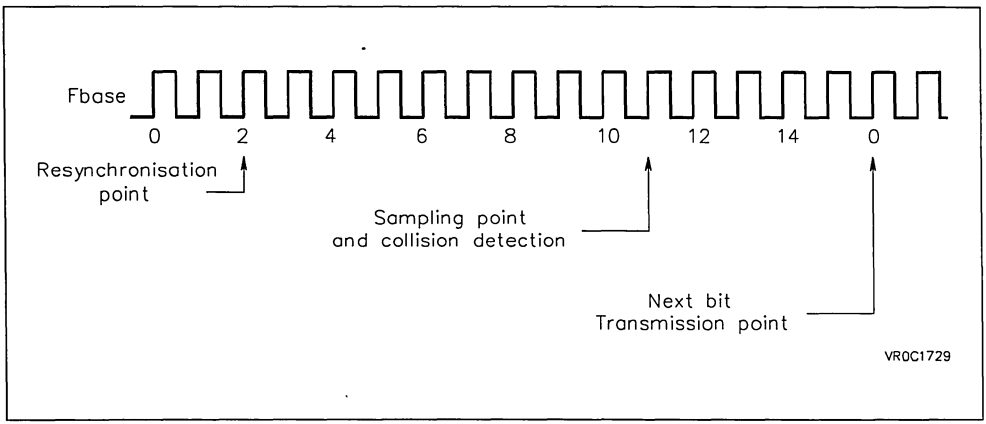


Figure 8. Time slot timing in VAN standard coding and pulse coding



VAN OVERVIEW (Continued)

Bit Representation

BIT REPRESENTATION in MANCHESTER_L:

- a logical '1' is coded as a '1' state during one time slot followed by a '0' state during one time slot.
- a logical '0' is coded as a '0' state during one time slot followed by a '1' state during one time slot.

As a consequence, 2 time slots are necessary to encode one bit.

BIT REPRESENTATION in MANCHESTER_E:

In this type of coding, bits are not coded individually but by nibble; 4 bits being encoded with 5 time slots.

- The three first bits are NRZ coded and the last bit of the nibble is MANCHESTER_L encoded.

As a consequence, a 1.25 time slot average is necessary to encode one bit.

Figure 9. Bit Representation in Manchester L

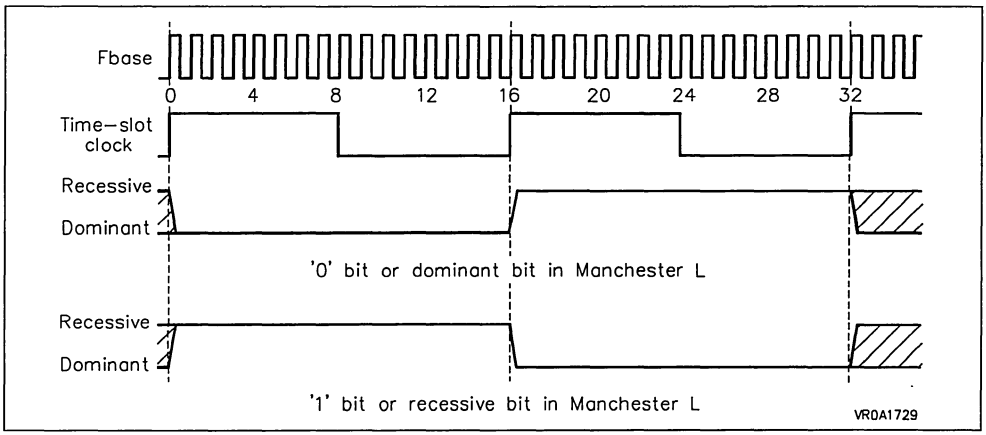
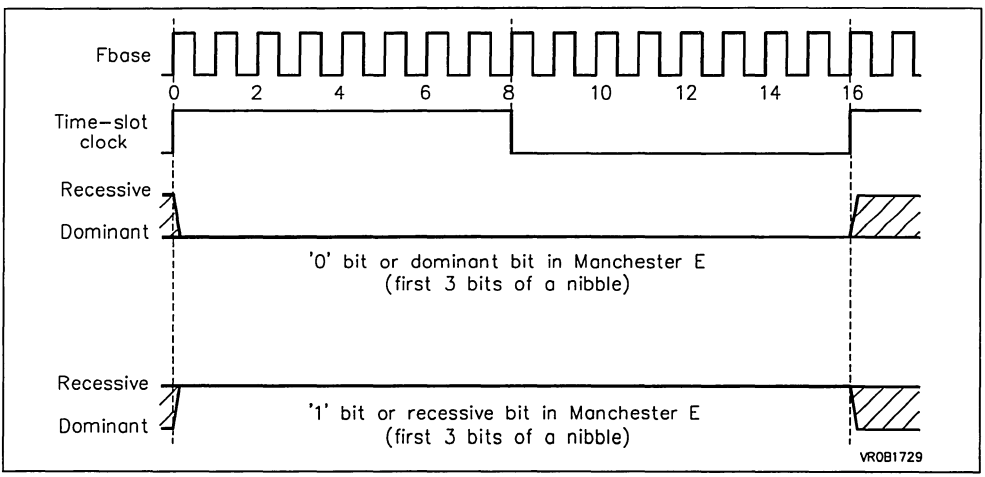


Figure 10. Bit Representation in Manchester E (NRZ Coded)



VAN OVERVIEW (Continued)

DESCRIPTION OF VAN FRAMES

Data Frames

Each frame is formed in a single format and is composed of following fields:

Start Of Message, Identifier, Command, Data, Frame Check Sequence, End Of Data, Acknowledge, End Of Message.

1) **SOF**: Start Of Frame

The Start Of Frame delimiter marks the beginning of the frame and allows synchronization for reception.

SOF is made of a preamble and a start bit. The preamble gives a common time reference for clock error confinement while the start bit initializes the frame.

SOF must be preceded by the IFS field (4 recessive time-slots).

The Preamble comprises of 4 dominant time slots followed by 4 recessive time slots.

The Start bit comprises of 1 dominant time slot followed by 1 recessive time slot.

2) **ID**: IDentifier: The identifier is a 12-bit field used to specify the frame's identification.

The identifier of a frame to be transmitted is provided by the host.

3) **COM**: COMmand:

This is a 4-bit field whose meaning is as follows:

Table 1. Command Field Description

	ML	ME	Meaning
EXT	1	1	Reserved for future extensions
RAK	1	1	acknowledge request
	0	0	acknowledge not requested
R/W	0	1	read request
	1	0	write request
RTR	0	0	data transmission
	1	1	remote transmission request

Note:
ML: MANCHESTER_L encoding
ME: MANCHESTER_Enhanced encoding

- EXTension: a reserved bit set to '1' (recessive state)
- RAK: Request AcKnowledge: this bit determines whether the sending module requests that a receiver module acknowledges successful reception of the frame.

RAK = '1': acknowledgement is requested

RAK = '0': acknowledgement is not requested

- R/W: this bit indicates whether the frame sent is a write or a read request
- RTR: Remote Transmit Request

If the bit is '0', the frame sent contains LLC-level data. If the bit is '1', the frame contains no data, and is interpreted as an in-frame request to send.

4) **DATA** field: the data field consists of a sequence having a whole number of bytes. The content of this field is provided by the LLC sublayer.

5) **FCS**: Frame Check Sequence

CRC (Cyclic Redundancy Check) is used in the receive and transmit procedures to detect any individual errors or packet errors.

The FCS field is a 15-bit field containing check bits.

The encoding is defined by the polynomial generator:

$$x^{15} + x^{11} + x^{10} + x^9 + x^8 + x^7 + x^4 + x^3 + x^2 + 1.$$

The CRC calculation includes the identification, command and data fields.

In transmit mode, the data bits are subjected to an encoding process, which is equivalent to division by the polynomial generator. The remainder obtained (ones complemented) is sent on the bus immediately after the data, in decreasing order of terms.

6) **EOD**: End Of Data

This field marks the end of the fields transmitted by the sender, i.e the following fields: identifier, command, LLC data, and FCS fields. It therefore determines the length of LLC data sent in the frame. This field is made of two consecutive dominant time slots.

7) **ACK** ACKnowledge

- positive acknowledge consists of one recessive time slot followed by a dominant time slot.
- absent acknowledge consists of two consecutive recessive time slots.

8) **EOF** End Of Frame marks the end of the frame.

It consists of eight consecutive recessive bits.

VAN OVERVIEW (Continued)

Figure 11. VAN frame structure

Note: IDEN, COM, DATA (if any) and FCS fields are transmitted MSB first

SOF	IDEN	COM	DATA (optional)	FCS	EOD	ACK	EOF

Order of Transmission

IDEN: The Identifier field is a 12-bit word used to specify the frame identification

I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0

first transmitted bit — last transmitted bit

COM: The Command field is a 4-bit word

EXT	RAK	R/W	RTR

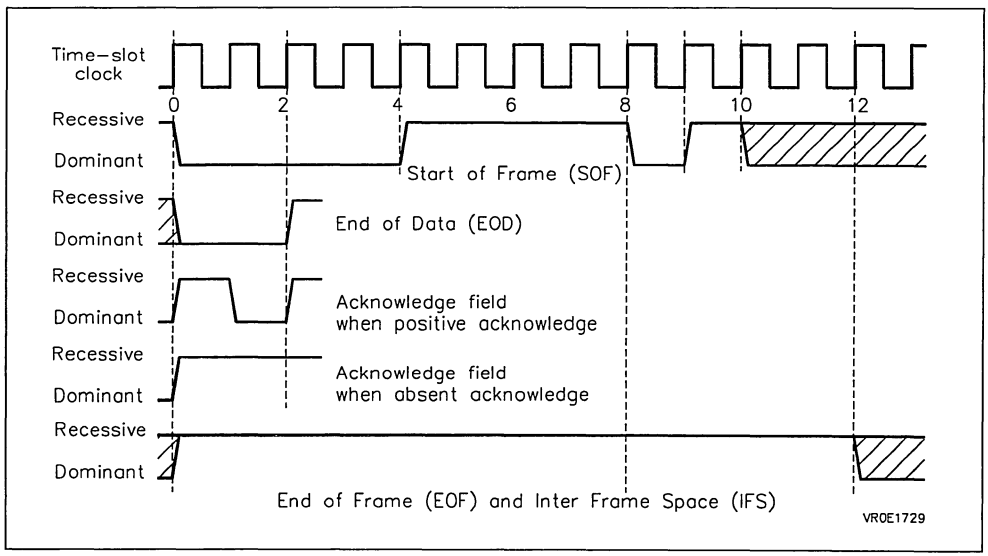
first transmitted bit — last transmitted bit

FCS: The Frame Check Sequence is a 15-bit CRC value

F_{14}	F13	F_{12}	F_{11}	F_{10}	F_9	F8	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0

first transmitted bit — last transmitted bit

Figure 12. VAN Frame field signal coding



VAN OVERVIEW (Continued)

ARBITRATION

In the case where two or more ST9560s start transmission concurrently, the bus access conflict is solved by a bit-wise arbitration method. The transmit logic compares the bit level transmitted to the bit level monitored on the bus. The transmit logic stops transmission if a recessive bit was sent and a dominant bit was monitored. This method guarantees transmission of the message with the highest priority even if there is a collision without loss of time.

As a result the identifier not only indicates the destination of the message but also its priority.

In case of loss of arbitration, the ST9560 continues to monitor the bus and when the bus is free, it tries again to send the message.

The arbitration process described above covers the fields:

- IDEN, COM, DATA, FCS

The halting of transmission in the case of a loss of arbitration does not stop the reception process, allowing the in-frame response mechanism to operate.

Request/Response Frames

ST9560 is able to send request/response frames.

Such a frame is characterized by a data field of zero length, and by a command field for which the R/W and RTR bits have the following values:

R/W designates a read mode.
RTR is specified as remote request.

In the event of an in-frame response, the initiator sends the frame part including IDENTIFIER and COMMAND fields.

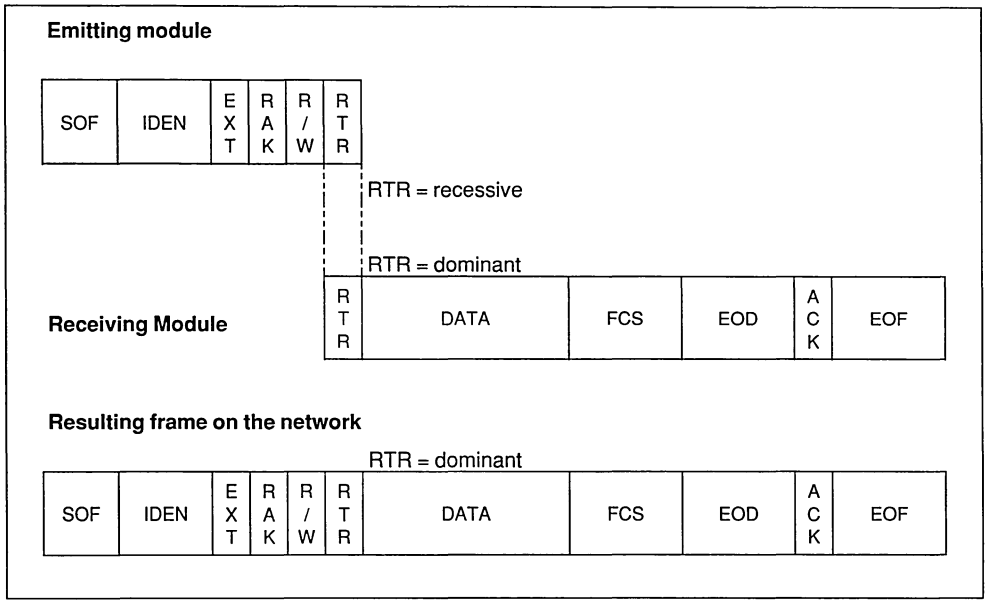
The response part of frame generated by the polled answering module, contains the following fields:

- a dominant RTR bit whose value is superimposed on the recessive bit of the request.
- a data field
- an FCS sequence

Superposition of the two parts of the frame (request and in-frame response) gives a frame on the bus which has a structure in compliance with the general frame structure.

The ST9560 cannot send in-frame responses.

Figure 13. In-frame response description



VAN OVERVIEW (Continued)

ERROR HANDLING

Error Detection

The ST9560 is equipped with several error mechanisms, implemented in hardware for efficiency

Note: Receive errors are reported only if the frame identifier is accepted.

Coherence of Reception Error

This error corresponds to the detection of an incoherence between the three receive inputs.

Code Violation Error

An error is detected on one of the bits of the binary or data fields of the frame (IDEN, COM, DAT, FCS).

This type of error occurs when the time between two transitions is less than 12/16 of time slot duration.

If such an error is detected during transmission, then bit TCVL of the Error Transmit Register is set.

If such an error is detected during reception of a message having passed the acceptance filter, bit RCVL of the Error Receive Register is set.

CRC Error

A Cyclic Redundancy Check is used in the transmit and receive procedures to detect any individual or packet errors in the messages transmitted.

The FCS is a 15-bit field, the remainder of the division by the generator polynomial:

$$x^{15} + x^{11} + x^{10} + x^9 + x^8 + x^7 + x^4 + x^3 + x^2 + 1$$

The CRC calculation is made on the fields:

- IDEN, COM, DATA

In transmit mode the FCS field is sent onto the line immediately after the data bits.

The receiver computes the CRC again. If both CRC, transmitted and computed by the receiver are different, an error has occured.

If such an error is detected during transmission, bit TCRC of the Error Transmit Register is set.

If such an error is detected during reception of a message having passed the acceptance filter, bit TCRC of the Error Receive Register is set.

DIAGNOSIS

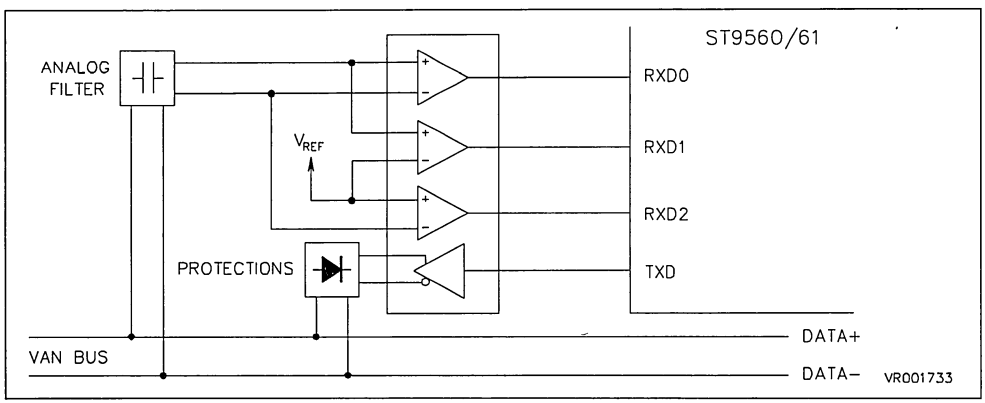
The three RxDi inputs provide three different information states on the bus. RxD0 gives the true differential logical information. RxD1 and RxD2 provide logical information from each of the two bus wires (with a threshold operation).

The diagnosis block logic performs the following functions:

- digital filtering (on 5 successive samples) in order to eliminate spikes
- transition analysis (synchronous, asynchronous, transmit, protocol)
- decision logic in order to select (automatically or not) a degraded mode (monofilar) or to detect that transmission is impossible and when to go back to the normal differential mode with the help of the TOP DIAG 'clock'.

Control and status bits are provided to manage the operation of the diagnosis logic.

Figure 14. Line-Interface Diagnosis Schematic



ST9560 MICRO INTERFACE

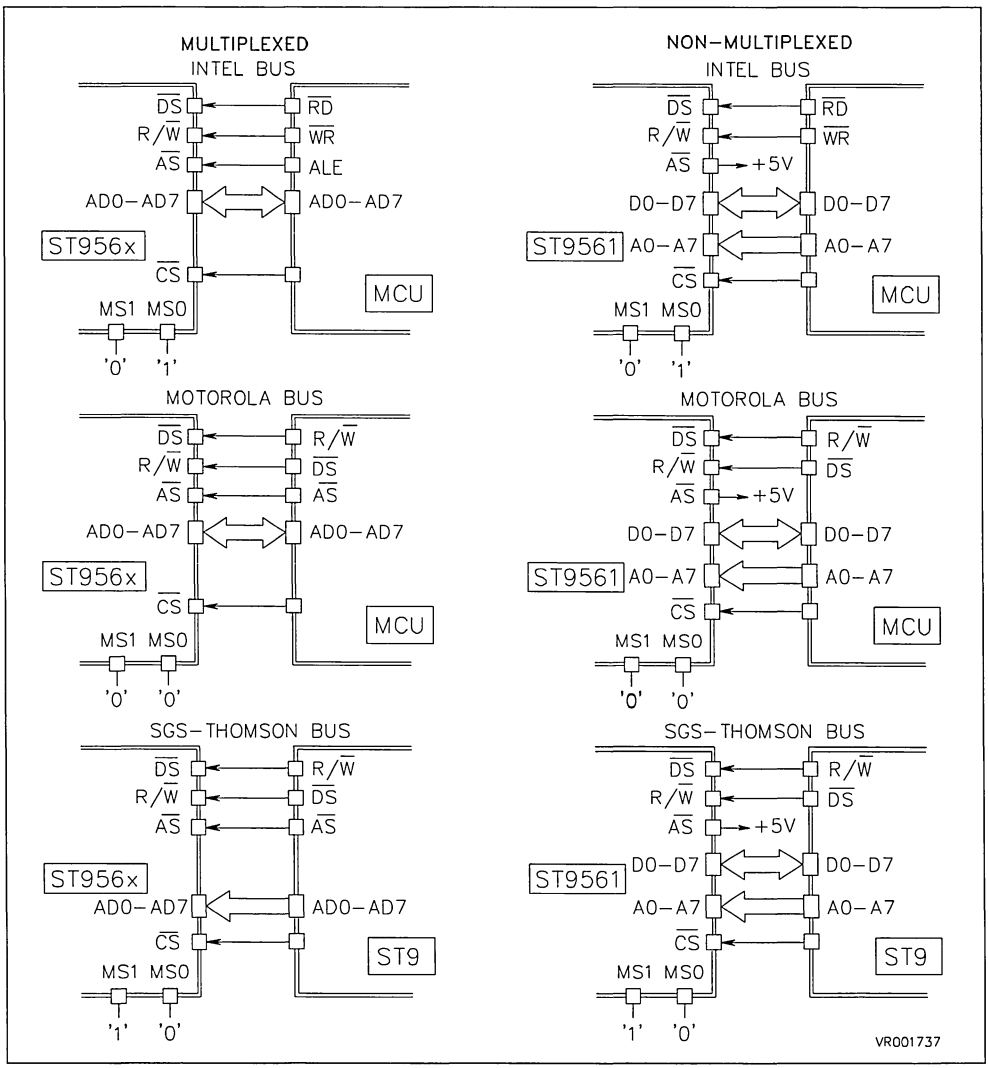
Two ST9560 versions are provided, both having the same VAN controller core and different micro interface.

A first version, a 28-pin one, is the stand alone version which is able to interface with different microprocessors such as ST9 and other general purpose microcontrollers such as Motorola 68HC11 or Intel 8051.

It uses an 8-bit address/data bus multiplexed and several control lines (ALE, $\overline{RD}$ or $\overline{DS}$, $\overline{WR}$ or $R/\overline{W}$, $\overline{CS}$) and system lines ($\overline{RST}$, $\overline{IRQ}$).

A second version, a 44-pin one, is also available offering a multiplexed/non-multiplexed bus selection. The remaining pins are used as standard I/O pins which can be configured as standard I/O's or alternate function outputs.

Figure 15. Micro Interface Schematics



FUNCTIONAL DESCRIPTION

Memory Mapping

The 160 bytes of on-chip RAM is divided into three areas:

- 2 x 32-byte receive buffers. Both of these buffers are located at the same logical addresses from address 32 (20h) to address 63 (3Fh).
- 2 x 32-byte transmit buffers. The buffers are located from address 64 (40h) to address 95 (5Fh) for transmit buffer 1 and from address 96 (60h) to 127 (7Fh) for transmit buffer 0. Only one buffer is used at any time and is user selectable. This allows the precreation of certain messages, perhaps error or warning frames, held in one transmit buffer until needed, the second buffer being used for normal transmit functions.
- 32-byte identifier buffer. This buffer is located at the same addresses as the receive buffers.

Command and status registers are located from address 0 to 19 (13h).
Locations 20 to 23 are not used (13h to 17h).

The locations 24 to 31 hold the I/O port registers of the ST9561 (14h to 1Fh). These addresses must not be used in the ST9560.

ST9560 Memory mapping

Function	Address (hex)
Transmit Buffer 0 XBF0	7F 60
Transmit Buffer 1 XBF1	5F 40
Identifiers/ Receive Buffer IBUF/RBUF0/1	3F 20
I/O Control Registers (ST9561 only)	1F 18
Reserved	17 14
Control/Status Registers	13 00

Control and Status Registers

18 registers, located at lowest addresses, both command and status, are provided for management of ST9560:

All unused address locations are reserved for future use.

Table 2. Registers

Register/Function		Address
General Purpose		
System Control Register	SCR	00h
Mode Control Register	MCR	01h
Physical Control Register	PCR	04h
Interrupt registers		
Enable Interrupt Register	EIR	05h
Status Interrupt Register	SIR	06h
Reset Interrupt Register	RIR	07h
Receive Registers		
Mode Received Register	MRR	08h
Status Received Register 1	SRR1	09h
Status Received Register 2	SRR2	0Ah
Error Received Register	ERR	0Bh
Mask Registers		
MSB of Mask 0	MSBM0	0Ch
LSB of Mask 0	LSBM0	0Dh
MSB of Mask 1	MSBM1	0Eh
LSB of Mask 1	LSBM1	0Fh
Transmit Registers		
Mode Transmit Register	MTR	10h
Command Transmit Register	CTR	11h
Status Transmit Register	STR	12h
Error Transmit Register	ETR	13h

FUNCTIONAL DECRIPTION (Continued)

SCR System Control Register
address 00h (read/write register)

7							0
ABORT	RESET	RES	RES	M3	M2	M1	M0

b7 = **ABORT**. This bit has no action when = '0', when set to '1' transmission is stopped after the end of the current transmission if transmitting a frame or immediately if not. This bit is identical in function to ABORT1 in CTR and is logically OR'ed with it.

b6 = **RESET**. Setting this level-sensitive bit to '1' generates an internal hardware reset of the ST9560, equivalent to the low state on the hardware $\overline{RST}$ pin.

All bits of control registers are set to '0', with the exception of the INIT and TI interrupts which must be cleared before starting initalisation and communication. The contents of the RAM buffers are undefined and should be initialised by the host MCU. P0C1, P1C1, P0D and P1D registers are set to "FFh".
This bit has no action when = '0'.

b5-b4 = *RESERVED*

b3-b0 = **M3,M2,M1,M0.** *Mode select* The bits in this field set the type of coding used for transmission and reception as shown in table 4.
The VAN standard coding is intended for wire transmission and the pulse coding is adapted to fibre-optic transmission.

NOTE: The reserved bits of read/write or write-only registers should be forced to 0. These bits are shown as *RESERVED* in the register descriptions.

MCR Mode Control Register
address 01h (read/write register)

7							0
PRESC	CD2	CD1	CD0	TDDIV2	TDDIV1	TDDIV0	TDIAG

b7 = **PRESC**. *Prescaler* When this bit is '0', the 1/3 prescaler is disabled, setting this bit to '1' enables the 1/3 prescaler (see Figure 21).

b6-b4 = **CD2, CD1, CD0**. *Clock Divider* These 3 bits set the division ratio of the oscillator clock divider to generate the F_{BASE} clock. They are coded as $\log_2$ (CD2-CD0) as shown in Table 3.

b3-b1 = **TDDIV2-TDDIV0**. *Top Diag Divider*. These 3 bits are written by the host to define the period of the TOP DIAG clock used in line diagnosis. The bit clock is divided in order to generate TOP DIAG clock.
The division rate depends of TDDIV2, TDDIV1, TDDIV0 value as shown in Table 5.

b0 = **TDIAG.** *Top Diag* When TOP DIAG is set to '1' by the host, a pulse is generated into the line diagnosis part. This pulse is used to generate an internal clock (FMS). In a period between 2 TOP DIAG pulses, every module able to transmit a frame should have transmitted a minimum of one frame. If no response is detected within this time, the network may have a major problem.

Table 3. Clock Divider Ratio (CDDIV)

CD2	CD1	CD0	Divider
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

FUNCTIONAL DECRIPTION (Continued)

Table 4. Line Interface Mode select

M3	M2	M1	M0	Type Of Coding	Typical Line Interface
0	0	0	0	E-MANCHESTER (standard)	Wire
0	0	0	1	L-MANCHESTER (standard)	Wire
0	0	1	0	E-MANCHESTER (pulse)	Fibre Optic
0	0	1	1	L-MANCHESTER (pulse)	Fibre Optic

Note: All other combinations are reserved for future types of communication

Table 5. Top Diagnostic Clock divider

TDDIV2	TDDIV1	TDDIV0	TOP DIAG Clock (1)	Frequency Division
0	0	0	NO CLOCK(2)	-
1	0	0	100ms	8.192k
0	1	0	200ms	16.38k
1	1	0	400ms	32.77k
0	0	1	800ms	65.54k
1	0	1	1.6s	131.1k
0	1	1	3.2s	262.1k
1	1	1	6.4s	524.3k

Notes: 1. These periods are calculated for E-MANCHESTER coding with a 100 kT/s rate
2 Direct TOP DIAG Pulse

FUNCTIONAL DECRIPTION (Continued)

PCR Physical layer Control Register
address 04h (read/write register)

7							0
TPOL	RPOL	IER	RES	RES	RES	RX1	RX0

b7 = **TPOL**. *Transmit Polarity* In order to accomodate line interfaces which change the polarity of the transmission, this bit allows the automatic inversion of the data transmitted by the TxD pin.
When TPOL = '0' TxD has standard polarity (dominant = '0', recessive = '1'), when TPOL = '1' TxD has the inverse polarity (dominant = '1', recessive = '0').

b6 = **RPOL**. *Receive Polarity* This bit controls the polarity of the three RxDi inputs.
When RPOL = '0' the RxDi inputs have direct polarity, when RPOL = '1' they have inverse polarity.

b5 = **IER**. *Line Tranceiver Reset* This bit sets the logic state of the output pin IER. It may be used as the reset signal to the external line circuitry.

b4-b2 = *RESERVED*

b1-b0 = **RX1, RX0**. *Receiver Input Select*

RX1	RX0	Function
0	0	RxD0 selected as serial input
0	1	RxD1 selected as serial input
1	0	RxD2 selected as serial input
1	1	automatic selection of serial input

EIR Enable Interrupt Register
address 05h (read/write register)

7							0
GIE	RES	FTIE	RES	TIE	FRIE	OVIE	RIE

All bits are active high to enable the interrupt.

b7 = **GIE**. Global Interrupt Enable. All interrupt enable bits are OR'ed with GIE.

b6 = *RESERVED*

b5 = **FTIE**. Failed Transmit Interrupt Enable

b4 = *RESERVED*

b3 = **TBEIE**. Transmit Interrupt Enable

b2 = **FRIE**. Failed Receive Interrupt Enable

b1 = **OVIE**. Overrun Interrupt Enable

b0 = **RIE**. Receiver Interrupt Enable

SIR Status Interrupt Register
address 06h (read-only register)

7							0
IRQ	INIT	FTI	RES	TBEI	FRI	OVI	RDAI

All bits are active high. To clear a set interrupt status bit, it is necessary to write a '1' to the corresponding bit in the Reset Interrupt Register RIR.

b7 = **IRQ**. Interrupt (logical OR of the 6 interrupt sources)

b6 = **INIT**. *Initialisation Interrupt*. This bit is set to '1' on RESET (internal or external). It must be cleared by writing to the corresponding bit in RIR at the beginning of the host initialisation of the ST9560.

b5 = **FTI**. *Failed Transmit Interrupt*. An error in a frame being transmitted will set this bit. This error can be:

- discrepancy between RxD0, RxD1 and RxD2,
- CRC error,
- code violation

as indicated in Error Transmit Register ETR.

b4 = *RESERVED*

b3 = **TBEI**. *Transmit Buffer Empty Interrupt* After a frame has been successfully transmitted, this bit is set to indicate completion and the transmit buffer selected is available for another message.
This bit is set to '1' on RESET (internal or external). It must be cleared by writing to the corresponding bit in RIR at the beginning of the host initialisation of the ST9560.

b2 = **FRI**. *Failed Receive*. An error causing a failure to make a valid reception of a frame will set this bit. The specific errors are flagged in the Error Receive Register ERR.

b1 = **OVI**. *Overrun*. This flag is set when the 2 receive buffers are filled with accepted incoming frames and a third incoming frame has passed the acceptance filter before the host has released a receive buffer.

b0 = **RDAI**. *Receive Data Available*. This bit is set when an accepted incoming frame is available in a receive buffer. To release the buffer the host has to read the message contents and to clear RDAI by setting the RDAIC bit of the Reset Interrupt Register RIR to '1'.

FUNCTIONAL DECRIPTION (Continued)

RIR Reset Interrupt Register
address 07h (write-only register)

7							0
RES	INITC	FTIC	RES	TIC	FRIC	OVIC	RDAIC

Interrupts are cleared one F_{BASE} cycle time after the corresponding bit in this register is set to '1'.

b7 = *RESERVED*

b6 = **INITC.** *Clear Init Interrupt*

b5 = **FTIC.** *Clear Failed Transmit Interrupt*

b4 = *RESERVED*

b3 = **TIC.** *Clear Transmit Interrupt*

b2 = **FRIC.** *Clear Fail Receive Interrupt*

b1 = **OVIC.** *Clear Overrun Interrupt*

b0 = **RDAIC.** *Clear Receive Data Available Interrupt*

MMR Mode Receive Register
address 08h (read/write register)

7							0
BA	RES	MF	RES	RES	RES	RES	RES

b7 = **BA.** *Buffer Access* This bit controls the host access to the two parallel 32byte RAM areas holding the identifiers and the receive buffer between addresses 20h and 2Fh as shown in Table 6.

b6 = *RESERVED*

b5 = **MF.** *Mask Filter* If an external acceptance identifier filter is used with the additional signals ADE and AKE available with the ST9561, this bit disables the internal filtering.

b5 = '0' normal mode
b5 = '1' every identifier on the VAN bus is recognized by the ST9561 when ADE = '1' (frames with RAK = '1' correctly received are acknowledged)

Note: The ADE input is not externally available for the ST9560 and the ADE input is always pulled high, thus setting the MF bit of the ST9560 will cause all incoming frames to be accepted.

b4-b0 = *RESERVED*

SRR1 Status Receive Register 1
address 09h (read-only register)

7							0
RDA	RES	RES	RES	IN3	IN2	IN1	IN0

b7 = **RDA.** *Receive Data Available* When set to '1', this bit indicates a received frame is available in the receive buffer.

b6-b4 = *RESERVED*

b3-b0 = **IN3-IN0.** *Identifier Number* (b3 = MSB) Filtered identifier index number into the Identifier RAM. This value is used by the host MCU as the index to the identifier in the RAM which has matched (after masking) the identifier field of the incoming frame. The identifier number is based upon the user allocation of the 16 identifiers in the Identifier RAM.

SRR2 Status Receive Register 2
address 0Ah (read-only register)

7							0
RDA1	RES	RES	LRBP4	LRBP3	LRBP2	LRBP1	LRBP0

b7 = **RDA1** This bit has the same meaning as RDA in SRR1.

b6-b5 = *RESERVED*

b4-b0 = **LRBP4-LRBP0.** *Last Received Byte Pointer* (b4 = MSB) This field is programmed by the ST9560 to indicate the address of the last byte received in the receive buffer. This provides the message length.

Table 6. Buffer Access Bit

BA	Host Read 20h-2Fh	Host Write 20h-2Fh
0	Receive buffers	Identifiers
1	Identifiers	Identifiers

FUNCTIONAL DECRIPTION (Continued)

ERR Error Received Register
address 0Bh (read-only register)

7							0
RF	OVR	RCVL	RES	RCRC	RDS1	RDS0	RVP

All bits of this register are active high. They are reset when clearing the Failed Receive Interrupt (FRI of SIR) by writing a '1' to FRIC of RIR.

b7 = **RF**. *Receive Failure* This bit indicates (when set) that the last reception has failed, causing a Failed Receive interrupt request.

b6 = **OVR**. *Overrun* This flag is set when the 2 receive buffers are filled with accepted incoming frames and a third incoming frame has passed the acceptance filter before the host has released a receive buffer. This is physically the same bit as OVI in SIR.

b5 = **RCVL**. *Receive Code Violation* This bit indicates (when set) that a code violation has been detected during reception. A code violation can be an incorrect SOF pattern or an incorrect Manchester bit.

b4 = *RESERVED*

b3 = **RCRC**. *Receive CRC Error* This bit indicates (when set) that a CRC error has been detected during reception.

b2-b1 = **RDS1, RDS0** *Receive Data Status*

RDS2	RDS1	Function
0	0	RxD0 selected
0	1	RxD2 selected
1	0	RxD1 selected
1	1	Major Error, No communication

b0 = **RVP** *Receive Physical Violation* This bit indicates (when set) that an incoherence has been detected between RxD0, RxD1 and RxD2 during reception.

MSBM0 MSB Mask Register 0
address 0Ch (read/write register)

7							0
MSK0.11	MSK0.10	MSK0 9	MSK0 8	MSK0 7	MSK0 6	MSK0 5	MSK0 4

b7-b0 = **MSK0.11-MSK0.4** *MSB of MASK0*

LSBM0 LSB Mask Register 0
address 0Dh (read/write register)

7							0
MSK0 3	MSK0.2	MSK0 1	MSK0.0	RES	RES	RES	RES

b7-b4 = **MSK0.3-MSK0.0** *LS Bits of MASK 0*

b3-0 = *RESERVED*

Each bit set to '1' in Mask register 0 enables the comparison of the corresponding bit of the received message identifier to the corresponding bits in the identifiers in the identifier RAM when the ST9560 performs the internal message acceptance filtering function.
Mask 0 is selected by bits RCM1 = '0' and RCM0 = '1' for each identifier.

MSBM1 MSB Mask Register 1
address 0Eh (read/write register)

7							0
MSK1 11	MSK1.10	MSK1 9	MSK1.8	MSK1 7	MSK1.6	MSK1 5	MSK1 4

b7-b0 = **MSK1.11-MSK1.4**. *MSB of MASK 1*

LSBM1 LSB Mask REGISTER 1
address 0Fh (read/write register)

7							0
MSK1 3	MSK1.2	MSK1.1	MSK1.0	RES	RES	RES	RES

b7-b4 = **MSK1.3-MSK1.0**. *LS Bits of MASK 1*

b3-b0 = *RESERVED*

Each bit set to '1' in Mask register 1 enables the comparison of the corresponding bit of the received message identifier to the corresponding bits in the identifiers in the identifier RAM when the ST9560 performs the internal message acceptance filtering function.
Mask 1 is selected by bits RCM1 = '1' and RCM0 = '0' for each identifier.

FUNCTIONAL DECRIPTION (Continued)

MTR Mode Transmit Register
address 10h (read/write register)

7							0
RANK	RES	BUF	FTB4	FTB3	FTB2	FTB1	FTB0

b7 = **RANK**. *VAN Rank Select* When the ST9560 is configured in the with RANK = '0', it is a VAN autonomous module and can transmit (if the RTS bit is set) as soon as the bus is free.
When the ST9560 is configured with RANK = '1', it is a VAN synchronous access module and can transmit only if a Start Of Frame generated by another module is detected on the network.

b6 = *RESERVED*

b5 = **BUF**. *Transmit Buffer Select* When BUF = '0', Transmit buffer 0 (XBF0) is used
When BUF = '1', Transmit buffer 1 (XBF1) is used

b4-b0 = **FTBP4-FTBP0**. *First Transmit Byte Pointer* This field is programmed by the host MCU to select the first byte to transmit in the selected Transmit buffer. Once transmission commences, the data to send will be taken from the buffer at incrementing addresses until the address is equal to the Last Transmit Byte pointer in the CTR register.

CTR Control Transmit Register
address 11h (read/write register)

7							0
RTS	ABORT1	RES	LTB4	LTB3	LTB2	LTB1	LTB0

b7 = **RTS**. *Request To Send* When RTS is set by the host, the ST9560 commences the transmission of a frame according to the setting of MTR and CTR.

b6 = **ABORT1**. *Abort Transmission* When ABORT1 is set to '1' by the host, it stops transmission after the end of the current transmission if transmitting a frame, immediately if not. This is identical in function to the ABORT bit of SCR.

b5 = *RESERVED*

b4-b0 = **LTBP4-LTBP0**. *Last Transmit Byte Pointer* b4 is MSB. This field is programmed by the host MCU to select the last byte to transmit in the selected Transmit buffer. Once transmission commences, the data to send will be taken from the buffer at incrementing addresses, starting from the address programmed into FTBR, until the address is equal to the Last Transmit Byte pointer in the CTR register.

FUNCTIONAL DECRIPTION (Continued)

STR Status Transmit Register
address 12h (read-only register)

7							0
TBA	RES	SBUF	CTB4	CTB3	CTB2	CTB1	CTB0

b7 = **TBA** *Transmit Buffer Available.* The host MCU may write into the XBF selected by the BUF bit of MTR when TBA = '1'.
When TBA = '0' the host must not write to the selected XBF as it is being used by the transmit logic.

TBA is set to '1' when the buffer has been transmitted successfully (TI interrupt) and is reset to '0' when the host starts a transmission by setting the relevant parameters in CTR and MTR.

b6 = *RESERVED*

b5 = **SBUF** *Transmit Buffer Selected* The Status information is associated to XBF selected by the BUF bit of MTR.
When SBUF = '0' the status is associated to XBF0.
When SBUF = '1' the status is associated to XBF1.

b4-b0 = **CTBP4-CTBP0**. *Current Transmit Byte Pointer* b4 is MSB. This field is programmed by the ST9560 to indicate the address within the transmit buffer of the current byte being transmitted.

ETR Error Transmit Register
address 13h (read-only register)

7							0
FTA	RES	TCVL	RES	TCRC	TDS1	TDS0	TVP

All bits in this register are active high. They are reset when clearing the Failed Transmit Interrupt (FTI of SIR) by writing a '1' to FTIC of RIR.

b7 = **FTA**. *Failed Transmission Alert* This bit indicates (when set) that last transmission has failed, causing a Failed Transmit interrupt request.

b6 = *RESERVED*

b5 = **TCVL**. *Transmit Code Violation* This bit indicates (when set) that a code violation has occured during transmission of the XBF in use. A code violation can be an incorrect SOF pattern or an incorrect Manchester bit.

b4 = *RESERVED*

bit 3 = **TCRC**. *Transmit CRC Error* This bit indicates (when set) that a CRC error has occured during transmission of the XBF in use.

b2-b1 = **TDS1, TDS0** *Transmit Data Select*

TDS1	TDS0	Function
0	0	RxD0 selected
0	1	RxD2 selected
1	0	RxD1 selected
1	1	Major Error, No communication

b0 = **TVP** *Transmit Physical Violation Error* This bit indicates (when set) that an incoherence has been detected between RxD0, RxD1 and RxD2 during transmission of the XBF in use.

RESERVED LOCATIONS

Locations from address 14h to 17h are reserved for future use.

I/O PORTS

In the ST9561 two I/O ports, Port 0 and Port 1, are available. Both ports may be configured by hardware (pin $\overline{DMX}$/P0 for Port 0 and DIR/$\overline{P1}$ for Port 1) and by software using control registers associated to ports.

I/O Port control Registers

When used in I/O Register mode, the Data Registers of the ports are mapped as following:

P0 Data Register Port 0 (P0D) Address 1Bh

P1 Data Register Port1 (P1D) Address 1Fh

The Data Registers control the logic level of the ports when configured in output mode. They are set to FFh after reset.

Two control registers per Port (PxC0 and PxC1) are used to select the output configuration. They are mapped as follows:

P0C0 Control Register 0 Port 0 Address 18h

P0C1 Control Register 1 Port 1 Address 19h

P1C0 Control Register 0 Port 0 Address 1Ch

P1C1 Control Register 1 Port 1 Address 1Dh

When $\overline{DMX}$/P0 ='1' and DIR/$\overline{P1}$ = '0', Port 0 and Port 1 are General Purpose I/O Ports. Port 0 allows the functional recreation of the MCU I/O port lost in communication with the ST9561. Each bit of the port can be individually set according to the following table.

PxC0.i	PxC1.i	I/O Bit Configuration
0	0	Input to Data Register PxD
0	1	Reserved
1	0	Output from Data Register PxD
1	1	Output Alternate Function.

where i = 0-7 and x = 0 or 1

After reset, PxC0 and PxC1 are set to 00h. It is highly recommended to refresh all data bits in these registers when using these ports in order to prevent accidental reconfiguration of non-connected port pins as inputs

Port 0 Output Alternate Functions

The PORT0 output alternate functions are as follows:

P0.7 DIN
P0.6 STAA line diagnosis signal.
P0.5 STAB line diagnosis signal.
P0.4 STAC line diagnosis signal.
P0.3 ERROR bit. This bit is set to '1' if an error has been detected in the frame.
P0.2 CVF2, encoded current state of the ST9561 internal state machine. Decoding is shown in the next table:
P0.1 CVF1
P0.0 CVF0

CVF2	CVF1	CVF0	State
0	0	0	WAIT
0	0	1	IDLER
0	1	0	IDLE
0	1	1	TBD
1	0	0	ACTIVE
1	0	1	ACKNOWLEDGE
1	1	0	ERROR

Port 1 Output Alternate Functions

When Port 1 bits 0, 4, 5, 6 and 7 are configured as output, the output alternate functions are as follows:

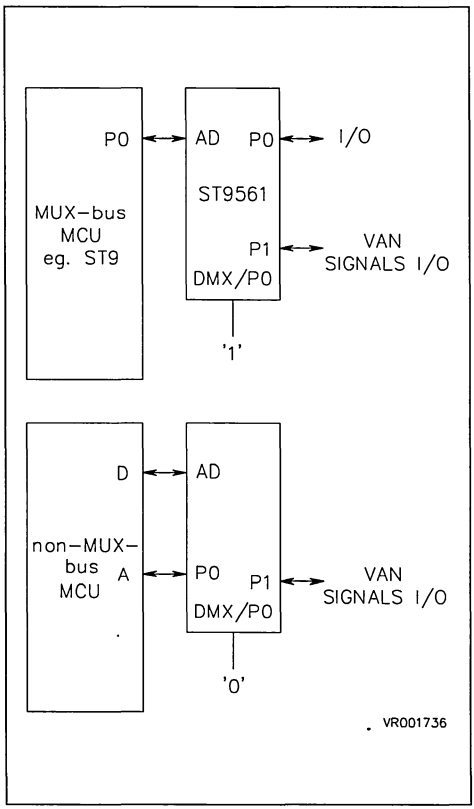
P1.0 TXD
P1.4 CKBIT
P1.5 CKTS
P1.6 CK16
P1.7 FTIP

FTIP is normally '1', it is set to '0' when the ST9561 is transmitting a frame, from the beginning of SOF to the end of EOD.

When bits 1, 2, 3 are configured as input, the input source is respectively RXD0, RXD2, RXD1.

I/O PORTS (Continued)

Figure 16. ST9561 Port Reconstruction



PORT FUNCTIONS

PORT 0

When $\overline{DMX}$/P0 ='0', Port 0 is the address input for the non-multiplexed bus interface.

7							0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
A7	A6	A5	A4	A3	A2	A1	A0

PORT 1

When DIR/$\overline{P1}$ = '1', PORT1 is in "direct mode". The pin functions are as follows:

7							0
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
IER	CK16	CKTS	CKBIT	RXD1	RXD2	RXD0	TXD

P1.7 IER reset output for bus tranceiver
P1.6 CK16 F_{BASE} clock (1)
P1.5 CKTS TIME SLOT clock (1)
P1.4 CKBIT clock bit (1)
P1.3 RXD1 serial input 1
P1.2 RXD2 serial input 2
P1.1 RXD0 serial input 0
P1.0 $\overline{TXD}$ serial output

Note 1. DIR/$\overline{P1}$ is tied to "1" internally in the ST9560. Pins P1.6, P1.5 and P1.4 are not used and are set to inputs tied to V_{DD}.

RESERVED LOCATIONS

Locations from address 1Ah to 1Eh are reserved for future use.

IDENTIFIER BUFFER

Identifiers are stored in a 32-byte RAM.

An identifier is a 12-bit field, up to sixteen identifiers may be stored on-chip.

This RAM is mapped in the ST9560 space memory from address 32 to 63 (20h to 3Fh). Bits within the Identifier are maskable with the MASK registers. This feature is controlled by the bit "MF, Mask Filter" of the Mode Receive register. When the MF bit is '1', all identifiers are accepted.

Identifier Bit Allocation

7							0
ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4

7							0
ID3	ID2	ID1	ID0	RES	AE	RCM1	RCM0

The 8 MSB bits are stored at even addresses (b7 = MSB of these 7 bits).

The 4 remaining LS bits are stored at odd addresses, bits 7 to 4 (b7 = MSB).

Bits 3 to 0 are used as following:

b3 = *RESERVED*

bit 2 = Acknowledge enable (AE)

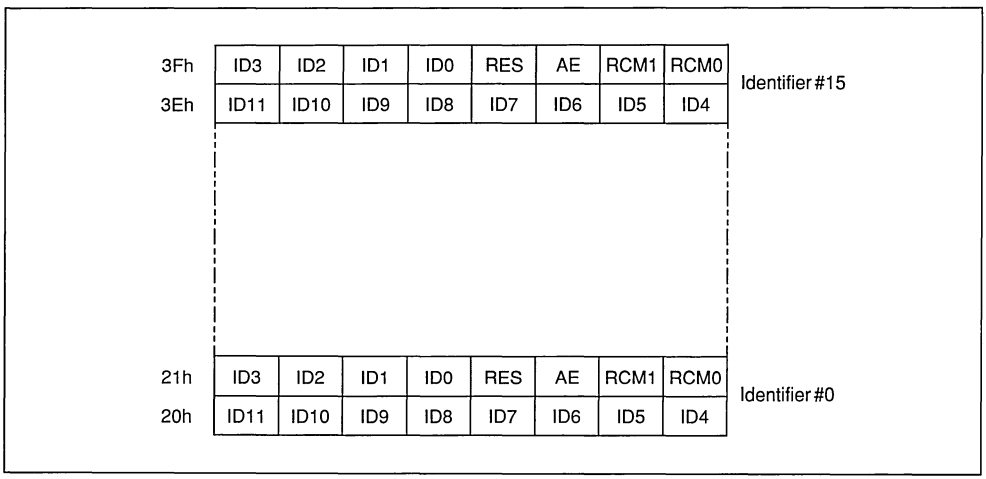
b2 = '0' acknowledge not to be generated.

b2 = '1' acknowledge generated if required.

b1-b0 = Receive control mode

RCM1	RCM0	Function
0	0	don't care identifier
0	1	mask # 1 filtered
1	0	mask # 2 filtered
1	1	no masking

Figure 17. Identifier mapping in the Identifier buffer



TRANSMIT AND RECEIVE BUFFERS

Transmit Buffer

The transmit buffer is the interface between the host CPU and the Bit Stream Processor and is able to store a whole message.

The buffer is written by the host CPU and is read by the BSP and is implemented as a 32-byte single port RAM with mutual exclusive access from the CPU and the BSP.

Two buffers are provided, XBF0 and XBF1, the user can choose either of the buffers to be written by the host.

Transmit is initiated by the host which writes in the CTR register (address 7):

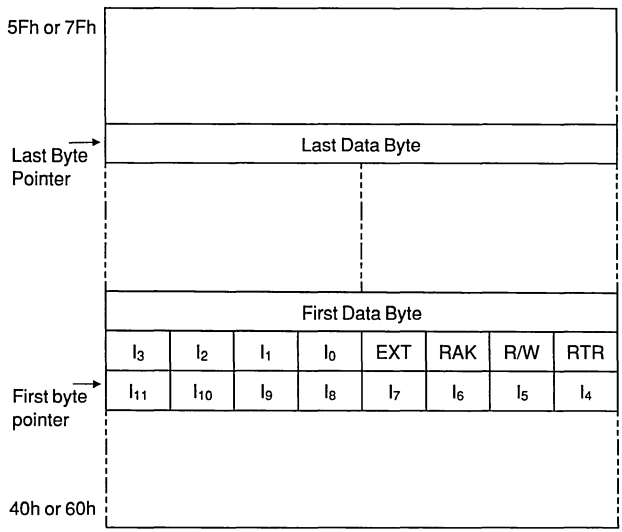
- request to send
- byte first and last address

Only one "request to send" is allowed at the same time.

An interrupt is generated at the end of transmit.

During frame transmission, the host cannot access the transmit buffer which is being used by the ST9560.

Figure 18. Transmit buffer structure



Notes:

- When there are no Data bytes (request frames), the last byte pointer is set to the 2nd Identifier command byte.
- The maximum frame length is 30 Data bytes.
- It is possible to store several frames in the same buffer.

TRANSMIT AND RECEIVE BUFFERS (Continued)

Receive Buffer

The receive buffer is the interface between the BSP and the host CPU which stores a message received from serial bus.

Once filled by the BSP and allocated to the CPU, the buffer is not available for another message. Therefore, unless the CPU releases the buffer, messages may be lost.

In order to reduce CPU requirements, two receive buffers are provided. While one buffer is allocated to the CPU, the BSP may write in the other.

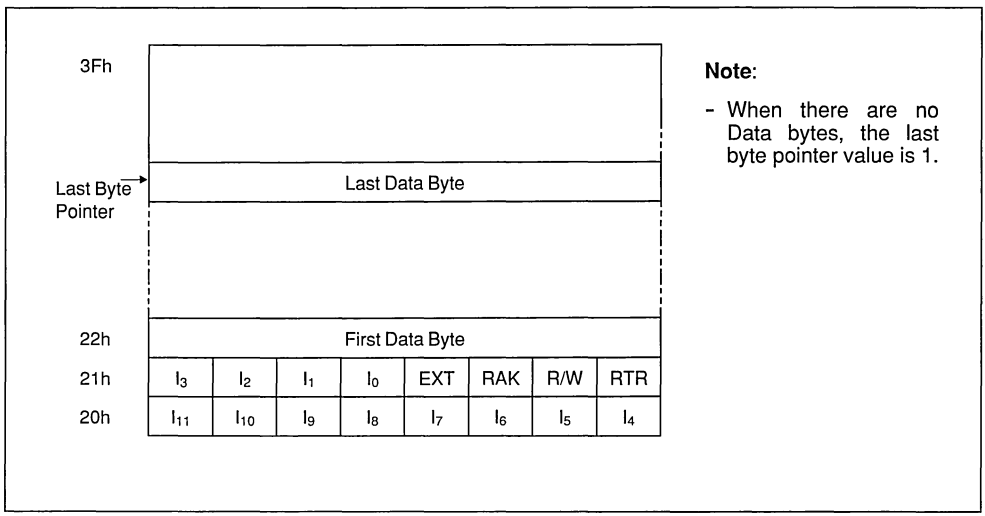
The BSP only writes into a receive buffer when the message being received passes one of the 16 acceptance filters loaded in the acceptance identifier RAM.

Both buffers are located at the same address from address 32 to address 63 (20h to 3Fh).

When a correct message is received, the Receive Status Registers 1 and 2 are updated and an interrupt is generated.

The receive buffers share the same address zone as the IDEN RAM, selection of the RAM area to be read is made under control of b7 of the MRR.

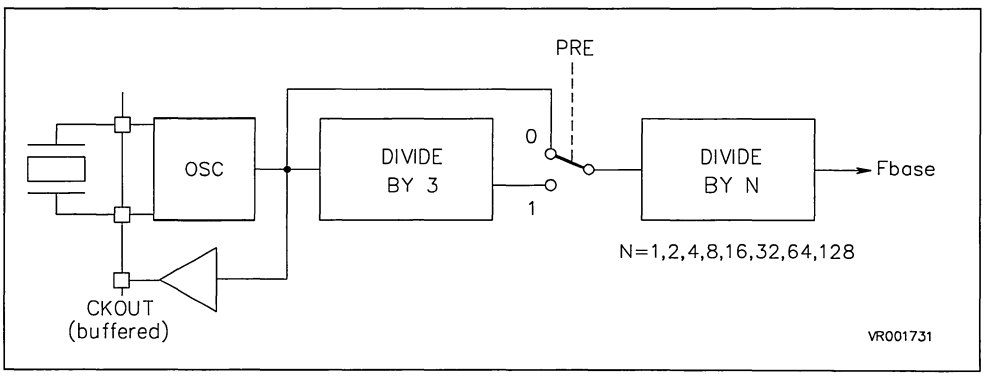
Figure 19. Receive Buffer Structure



Note:

- When there are no Data bytes, the last byte pointer value is 1.

Figure 20. F_{BASE} Clock Generator



TIMING AND SERIAL LINK RATE

ST9560 transmission rate

Time slot and bit frequencies are derived from elementary time clock called F_{BASE}.

F_{BASE} is obtained from the crystal oscillator frequency by the flow shown in figure 20, where N equals 1, 2, 4, 8, 6, 32, 64, 128 and is coded as $\log_2$ N in MCR.

According to the above flow, bit rate transmission is given by table 7, where:

- PRE designates the prescaler dividing ratio (1 or 3)
- DIV designates the coded programmed value N (F_{XTAL} or $F_{XTAL}/3$ is always divided by 2^N)
- F_{BASE} designates the elementary time frequency
- F_{TS} designates Time Slot frequency (kHz)
- M_L rate designates the rate in Manchester coding
- M_E rate designates the rate in Enhanced Manchester coding

ST9560 Oscillator

The oscillator generating the F_{BASE} timebase requires the use of an external crystal at the appropriate frequency for the transmission after division.

The circuit required is shown in the next figure:

Figure 21. ST9560 Oscillator

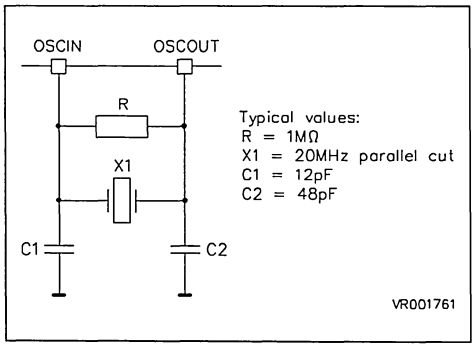


Table 7. Bit Rate Transmission (F_{XTAL} = 24MHz)

DIV	PRE	F_{BASE} (MHz)	F_{TS} (kHz)	M_L (kbits/s)	M_E (kbits/s)
1	1	24	1500	750	1200
1	3	8	500	250	400
2	1	12	750	375	600
2	3	4	250	125	200
4	1	6	375	187.5	300
4	3	2	125	62.5	100
8	1	3	187.5	93.75	150
8	3	1	62.5	31.25	37.5
16	1	1..5	93.75	46.875	75
16	3	0.500	31.25	15.625	25
32	1	0.75	46.87	23.438	37.5
32	3	0.25	15.625	7.813	12.5
64	1	0.375	23.438	11.718	18.75
64	3	0.125	7.813	3.906	6.25
128	1	0.1875	11.718	5.859	9.375
128	3	0.0625	3.906	1.953	3.125

INTERRUPT CONTROL

Interrupt Sources

The ST9560 can interrupt the micro in the five following cases, by asserting the $\overline{IRQ}$ pin low.

a) receive data available:

This occurs when an uncorrupted message, having passed the acceptance filter, is stored either in RBF0 or RBF1 buffer.

b) failed receive:

This occurs when an error is detected during reception of a message having passed the acceptance filter.

c) overrun:

A message passes the acceptance filter and neither RBF0 nor RBF1 buffers are available.

d) initialisation request:

The interrupt is generated by a low level on the $\overline{RST}$ pin or by setting bit 0 of the SCR register. No operation is allowed until this interrupt is cleared.

e) transmit data available:

The transmit buffer XBF0 or XBF1 (according to user choice) is available.

f) failed transmission:

An error has occurred during transmission of the message.

Interrupt Source Reset

Each interrupt source is cleared by setting to '1' the corresponding bit of the Reset Interrupt Register.

Enable Interrupt Register

An enable bit is associated to each interrupt source. Excepting the INIT interrupt, if the corresponding bit of an interrupt source is cleared, the source cannot interrupt the host MCU. In addition, a general interrupt enable is provided. If this bit is cleared, all interrupt sources are disabled, except the INIT interrupt.

Reset

After a reset of the ST9560 the TxD output is forced to high impedance. The ST9560 is able to transmit a level on TxD output when the INIT status interrupt is set to level 0 by the host.

ST9560 MAIN FUNCTIONS

Transmit

- acceptance of parallel data coming from the host (transmit buffer available)
- frame formatting by adding specific fields (Start Of Frame, CRC, End Of Data, End Of Frame)
- presentation to the physical layer of a serialized bit stream, starting reading from first transmit address of the transmit buffer, MSB first
- deferment of frame transmission so long as the physical medium is busy
- implementation of the arbitration mechanism
- termination of transmission upon collision detection
- in the event of loss of arbitration, scheduling a resend and continuing to receive the frame passing via the bus.
- computing the Frame Check Sequence (CRC) addition, adding it to the frame sent.
- management of the time-out to comply with the interframe spacing (IFS)
- signalling to the host that the transmit buffer is available.

Receive

- receiving a serialized bit stream from the serial bus, starting storing at address 32 (20h) of the receive buffer, MSB first.
- recompiling the complete structure of the frame (structure by field)
- checking the frame identifier and implementing the acceptance filter.
- computing the CRC of received bit stream and comparing the result with the CRC sent with the received message.
- checking the frame format
- signalling to the transmit part that an acknowledge must be sent
- removal of specific fields from the received frame
- transferring the useful parallel information (Identifier, Command and Data) to the host.

ST9560 MAIN FUNCTIONS (Continued)

Transmit Process

The ST9560 is capable of transmitting messages with variable length from 2 bytes (identifier and command fields) to lower than or equal to 30 bytes.

Transmit buffer XBF0 is used (or XBF1, according to user choice).

Host flow for transmission of a message

This flow consists in following steps:

1) check that the selected XBF buffer is available (bit 7 of Status Transmit register equals to '1')

2) write the IDENTIFIER, COMMAND and DATA fields in the TX buffer

3) write the byte count in the Command Transmit Register and set bit 7 (Request to send) of the Command Transmit Register to '1'.

4) reset interrupt source Transmit Data Available.

ST9560 flow for transmitting a message

1) check that 'Request to send' is set and TDBA (bit 3 of SIR) is cleared

2) check for 'bus idle', if not wait until the bus is free

3) send Start Of Frame

4) read the parallel data in the selected XBF buffer, serialise it and send it on the serial bus

5) monitor arbitration, if arbitration is lost, restart from step 2

6) check for errors

7) if transmission is not completed, repeat steps 4,5,6

8) send FCS field (CRC computed in parallel with step 4)

9) send EOD, ACK, EOF fields

10) set 'Transmit Buffer Available' in Status Transmit Register and assert Interrupt Transmit Request

Receive Process

As for transmit process, the ST9560 can receive frames with variable length.

Single mode is used to receive messages with length lower or equal to 32-byte.

Host flow

This flow consists in following steps:

1) check that RBF0 or RBF1 buffer is available (bit 7 of Status Receive Register equals to '1')

2) read the filtered identifier and the BYTE COUNT

3) read data from RBF0 or RBF1 buffer (BYTE COUNT is LOCATED in the Status Receive Register)

4) reset RDA and interrupt source

ST9560 flow

1) detects Start Of Frame

2) checks identifier

3) Data frame or request frame?

4) transfers IDEN, COM and DATA in the selected RBF0 or RBF1 buffer

5) checks errors

6) if not EOD, increments byte count and repeats steps 4,5

7) checks that the computed CRC result is equal to 4B15h and, if required and allowed, sends an acknowledge.

8) sets the byte count in Status Receive Register

ABSOLUTE MAXIMUM RATINGS

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

$Tj = T_A + PD \times RthJA$

Where :

T_A = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = $I_{DD} \times V_{DD}$ (chip internal power).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	-0.3 to 7.0	V
T_A	Operating Temperature Range	-40 to +125	°C
T_{STG}	Storage Temperature	-55 to 150	°C
P_{DMAX}	Maximum Power Dissipation	-	W

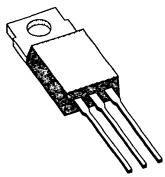
Note : Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD}	Power Supply		4.5	5.0	5.5	V
V_{IL}	Input Low Level Voltage				$0.3V_{DD}$	V
V_{IH}	Input High Level Voltage		$0.7V_{DD}$			V
I_{IL} I_{IH}	Input Leakage Current	non-I/O pins	-5		5	µA
V_{OL}	Low Level Output Voltage	I_{OL} = 4.0mA			0.4	V
V_{OH}	High Level Output Voltage	I_{OH} = -4.0mA	2.4			V
PD	Power Dissipation					W

TEA7605

LOW-DROP VOLTAGE REGULATOR

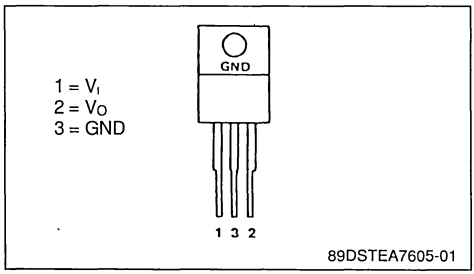
- V_O = 5V ± 4 % (I_O = 5mA)
- $I_{OS} \geq$ 500mA
- $V_I - V_O \leq$ 0.6 V (I_O = 500mA)
- $V_{I\ (surge)}$ = ± 80V
- THERMAL AND SHORT-CIRCUIT PROTECTION



TO220
(Plastic Package)

ORDER CODE : TEA7605SP

PIN CONNECTIONS



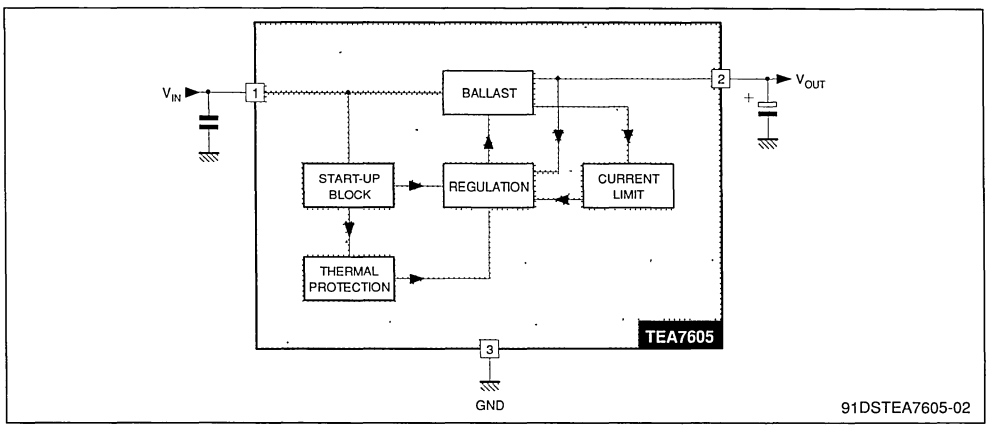
DESCRIPTION

TEA7605 is a low-drop 5V regulator well suited to supplying stabilized voltage to µPs in harsh industrial environment.

Special care was taken to keep :

- Lowest possible quiescent current (250µA).
- Lowest possible output capacitor (1µF).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input Voltage - Continuous - τ = 300 ms	 30 80	 V V
$V_{I(R)}$	Reverse Input Voltage - Continuous - τ = 120 ms	 – 18 – 80	 V V
T_J	Operating Junction Temperature	– 45, +150	°C
T_{stg}	Storage Temperature	– 55, +150	°C

TAB-01

THERMAL DATA

$R_{th\ (j\text{-}c)}$	Junction-case Thermal Resistance	Max.	3	°C/W
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	Max.	70	°C/W

TAB-02

ELECTRICAL OPERATING CHARACTERISTICS

T_j = 25°C, V_I = 14.4V (unless otherwise specified) Output Capacitor = 10µF (see note)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_O	Output Voltage (I_O = 5 to 500mA)	4.875	5	5.125	V
V_I	Input Supply Voltage (permanent)			28	V
I_{CC}	Current Consumption I_O = 0mA I_O = 150mA I_O = 500mA		0.25 10 75	0.4 20 100	mA mA mA
K_{VI}	Line Regulation (V_I = 6 to 26V ; I_O = 5mA)		5	10	mV
K_{VO}	Load Regulation (I_O = 5 to 500mA)		40	60	mV
V_I - V_O	Drop-out Voltage I_O = 150mA I_O = 500mA		0.18 0.4	 0.6	V V
SVR	Supply Voltage Rejection (I_O = 350mA, f = 120Hz, C_O = 1µF, V_I = 12 ± 5V)		60		dB
I_{OS}	Short-circuit Output Current	0.5	0.7		A

TAB-03

NOTE : Applications Hints

The output capacitor has a direct influence on output voltage stability. A 10 µF capacitor will provide satisfactory results. There is no upper limit on this capacitor value.

If necessary, this value can be reduced down to 1 µF ; however, in such case, it should be checked that output capacitor keeps sufficiently high capacitance and low equivalent series resistance in the whole temperature range.

Such low capacitor value is not recommended either, if output current is to switch abruptly from very high to very low values (for instance, 400 mA to < 1 mA).

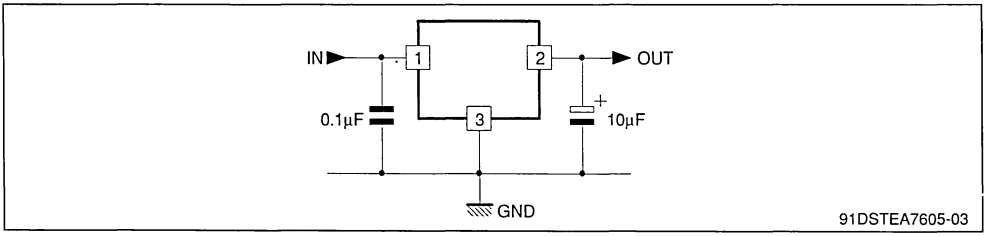
ELECTRICAL OPERATING CHARACTERISTICS

T_j = – 45°C to +125°C, V_I = 14 .4V (unless otherwise specified) Output Capacitor = 10µF

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_O	Output Voltage (I_O = 5 to 500mA)	4.8	5	5.2	V
$\frac{dv_O}{d_t}$	Output Voltage Drift T_j = – 45 to +25°C T_j = + 25 to +125°C	– 0.4 – 0.6			mV/°C
I_{CC}	Current Consumption I_O = 0mA I_O = 150mA I_O = 500mA			0.45 25 120	mA mA mA
K_{VI}	Line Regulation (V_I = 6 to 26V, I_O = 5mA)			20	mV
K_{VO}	Load Regulation (I_O = 5 to 500mA)			80	mV
V_I - V_O	Drop-out Voltage I_O = 150mA I_O = 500mA		0.2	 0.8	V V
I_{OS}	Short-circuit Output Current	0.4			A
I_{OM}	Maximum Output Current	0.5			A

TAB-04

APPLICATION DIAGRAM

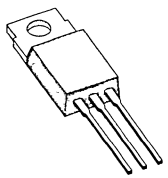


SGS-THOMSON MICROELECTRONICS

TEA7610

LOW-DROP VOLTAGE REGULATOR

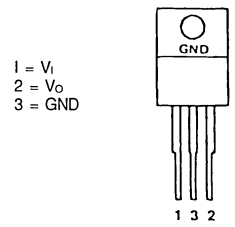
- V_O = 10V ± 4% (I_O = 5mA)
- I_O = 5 TO 500mA
- V_I - V_O = 0.6V (I_O = 500mA)
- $V_{I\ (surge)}$ = ± 80V
- THERMAL AND SHORT-CIRCUIT PROTECTION



TO220
(Plastic Package)

ORDER CODE : TEA7610SP

PIN CONNECTIONS



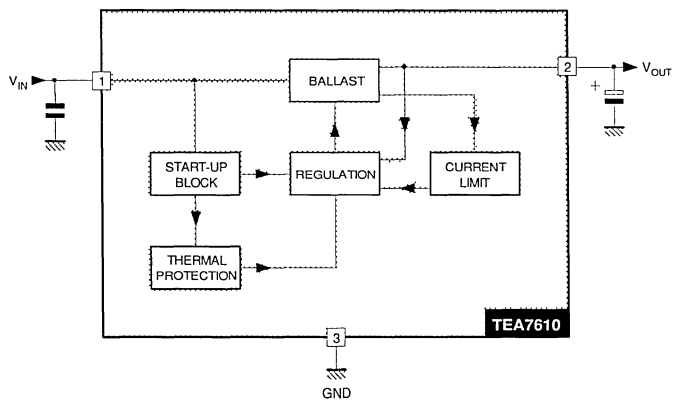
89DSTEA7610-01

DESCRIPTION

TEA7610 is a low-drop regulator well suited to supplying stabilized voltage to µPs in harsh industrial environment.

Special care was taken to keep :
- Lowest possible output capacitor (1µF).

BLOCK DIAGRAM



91DSTEA7610-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input Voltage - Continuous - τ = 300 ms	 30 80	 V V
$V_{I(R)}$	Reverse Input Voltage - Continuous - τ = 120 ms	 – 18 – 80	 V V
T_{oper}	Operating Junction Temperature	– 45, +150	°C
T_{stg}	Storage Temperature	– 55, +150	°C

TAB-01

THERMAL DATA

$R_{th(j-c)}$	Junction-case Thermal Resistance	Max.	3	°C/W
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	Max.	70	°C/W

TAB-02

ELECTRICAL OPERATING CHARACTERISTICS

T_j = 25°C, V_I = 14.4V (unless otherwise specified) Output Capacitor = 10µF (note)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_O	Output Voltage (I_O = 5 to 500mA)		9.7	10	10.3	V
V_I	Input Supply Voltage (permanent)				28	V
I_{CC}	Current Consumption	I_O = 0mA I_O = 150mA I_O = 500mA		1.5 10 75	2 20 100	mA mA mA
K_{VI}	Line Regulation (V_I = 11 to 26 V ; I_O = 5mA)			5	20	mV
K_{VO}	Load Regulation (I_O = 5 to 500mA)			40	80	mV
V_I - V_O	Drop-out Voltage	I_O = 150mA I_O = 500mA		0.18 0.4	 0.6	V V
SVR	Supply Voltage Rejection (I_O = 350mA, f = 120Hz, C_O = 1µF, V_I = 12 ± 5V)			60		dB
I_{OS}	Short-circuit Output Current		0.5	0.7		A

TAB-03

NOTE : Application Hints
The output capacitor has a direct influence on ouptut voltage stability. A 10µF capacitor will provide satisfactory results ; there is no upper limit on this capacitor value.
If necessary, this value can be reduced down to 1µF ; however, in such case, it should be checked that output capacitor keeps sufficiently high capacitance and low equivalent series resistance in the whole temperature range.
Such low capacitor value is not recommended either, if output current is to switch abruptly from very high to very low values (for instance 400mA to < 1mA).

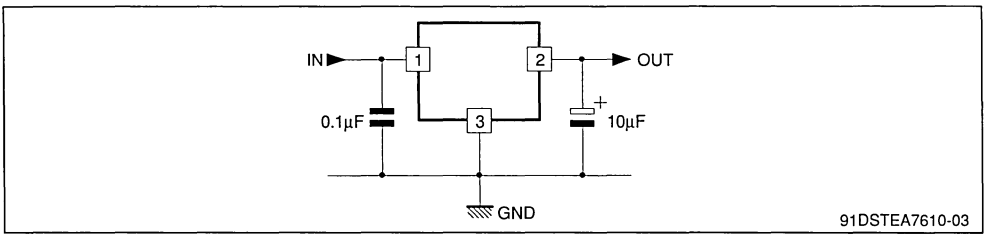
ELECTRICAL OPERATING CHARACTERISTICS

T_j = – 45°C to +125°C, V_I = 14.4V (unless otherwise specified) Output Capacitor = 10µF

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_O	Output Voltage (I_o = 5 to 500mA)		9.6	10	10.4	V
$\frac{d_{VO}}{d_t}$	utput Voltage Drift	T_j = – 45 to +25°C T_j = + 25 to +125 °C	– 1 – 1.2		0 0	mV/°C
I_{CC}	Current Consumption	I_O = 0mA I_O = 150mA I_O = 500mA			2.5 25 120	mA mA mA
K_{VI}	Line Regulation (V_I = 11 to 26V ; I_O = 5mA)				30	mV
K_{VO}	Load Regulation (I_O = 5 to 500mA)				100	mV
V_I - V_O	Drop-out Voltage	I_O = 150mA I_O = 500mA		0.20	0.8	V V
I_{OS}	Short-circuit Output Current		0.4			A
I_{OM}	Maximum Output Current		0.5			A

TAB-04

APPLICATION DIAGRAM

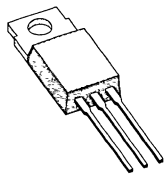


SGS-THOMSON MICROELECTRONICS

TEA7685

LOW-DROP VOLTAGE REGULATOR

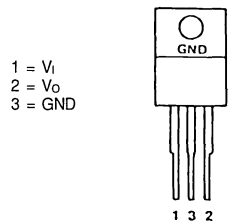
- V_O = 8.5V ± 4% (I_O = 5mA)
- I_O = 5 TO 500mA
- V_I - V_O = 0.6V (I_O = 500mA)
- $V_{I\ (surge)}$ = ± 80V
- THERMAL AND SHORT-CIRCUIT PROTECTION



TO220
(Plastic Package)

ORDER CODE : TEA7685SP

PIN CONNECTIONS



89DSTEA7685-01

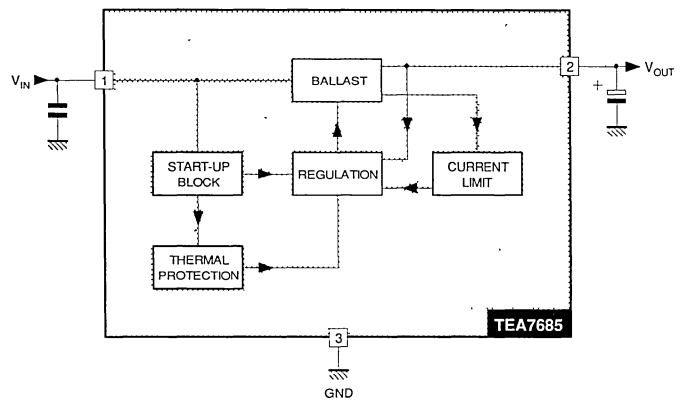
DESCRIPTION

TEA7685 is a low-drop 8.5V regulator well suited to supplying stabilized voltage to µPs in harsh industrial environment.

Special care was taken to keep :

- Lowest possible output capacitor (1µF).

BLOCK DIAGRAM



91DSTEA7685-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input Voltage - Continuous - τ = 300ms	 30 80	 V V
$V_{I(R)}$	Reverse Input Voltage - Continuous - τ = 120ms	 – 18 – 80	 V V
T_{oper}	Operating Junction Temperature	– 45, +150	°C
T_{stg}	Storage Temperature	– 55, +150	°C

TAB-01

THERMAL DATA

$R_{th(j-c)}$	Junction-case Thermal Resistance	Max.	3	°C/W
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	Max.	70	°C/W

TAB-02

ELECTRICAL OPERATING CHARACTERISTICS

T_j = 25°C, V_I = 14.4V (unless otherwise specified) Output Capacitor = 10µF (note)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_O	Output Voltage (I_O = 5 to 500mA)		8.26	8.5	8.74	V
V_I	Input Supply Voltage (permanent)				28	V
I_{CC}	Current Consumption	I_O = 0mA I_O = 150mA I_O = 500mA		1.5 10 75	2 20 100	mA mA mA
K_{VI}	Line Regulation (V_I = 9.5 to 26V ; I_O = 5mA)		– 15	5	15	mV
K_{VO}	Load Regulation (I_O = 5 to 500mA)		– 70	– 40	70	mV
V_I - V_O	Drop-out Voltage	I_O = 150mA I_O = 500mA		0.18 0.4	 0.6	V V
SVR	Supply Voltage Rejection (I_O = 350mA, f = 120Hz, C_O = 1µF, V_I = 12 ± 5V)			60		dB
I_{OS}	Short-circuit Output Current		0.5	0.7		A

TAB-03

NOTE : Application Hints
The output capacitor has a direct influence on ouptut voltage stability A 10µF capacittor will provide satisfactory results ; there is no upper limit on this capacitor value
If necessary, this value can be reduced down to 1µF ; however, in such case, it should be checked that output capacitor keeps sufficiently high capacitance and low equivalent series resistance in the whole temperature range.
Such low capacitor value is not recommended either, if output current is to switch abruptly from very high to very low values (for instance 400mA to < 1mA).

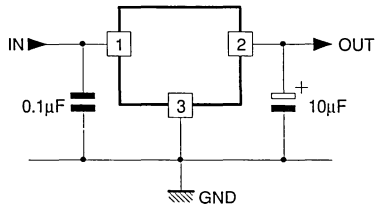
ELECTRICAL OPERATING CHARACTERISTICS

T_j = – 45°C to + 125°C, V_I = 14.4V (unless otherwise specified) Output Capacitor = 10µF

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_O	Output Voltage (I_O = 5 to 500mA)		8.16	8.5	8.84	V
$\frac{dV_O}{dt}$	Output Voltage Drift	T_j = – 45 to +25°C T_j = + 25 to +125°C	– 1 – 1.2		0 0	mV/°C
I_{CC}	Current Consumption	I_O = 0mA I_O = 150mA I_O = 500mA			2.5 25 120	mA mA mA
K_{VI}	Line Regulation (V_I = 9.5 to 26V ; I_O = 5mA)		– 25		25	mV
K_{VO}	Load Regulation (I_O = 5 to 500mA)		– 90		90	mV
V_I - V_O	Drop-out Voltage	I_O = 150mA I_O = 500mA		0.20	 0.8	V V
I_{OS}	Short-circuit Output Current		0.4			A
I_{OM}	Maximum Output Current		0.5			A

TAB-04

APPLICATION DIAGRAM



91DSTEA7685-03

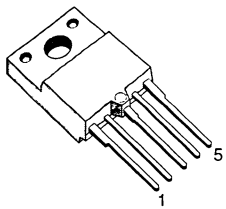
SGS-THOMSON MICROELECTRONICS

VB020

HIGH VOLTAGE IGNITION COIL DRIVER POWER IC

TYPE	V_{cl}	I_{cl}	I_d
VB020	400 V	6 A	150 mA

- PRIMARY COIL VOLTAGE INTERNALLY SET
- COIL CURRENT LIMIT INTERNALLY SET
- LOGIC LEVEL COMPATIBLE INPUT
- OVERVOLTAGE PROTECTION OF THE DRIVING AND CONTROL CIRCUIT



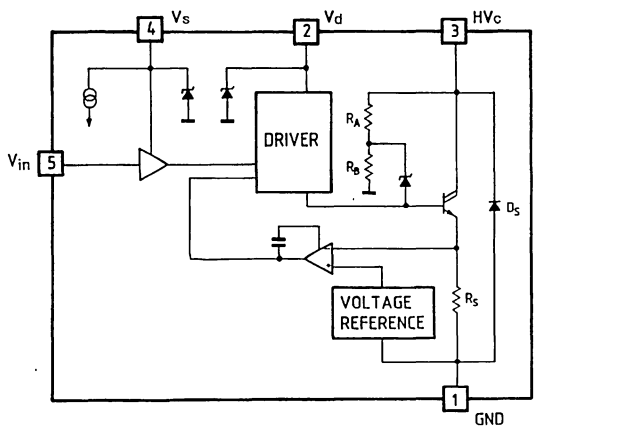
ISOWATT5

DESCRIPTION

The VB020 is a high voltage power integrated circuit made using SGS-THOMSON Microelectronics Vertical Intelligent Power Technology, with vertical current flow power darlington and logic level compatible driving circuit.

Built-in protection circuits for coil current limiting and collector voltage clamping allows the VB020 to be used as a smart, high voltage, high current interface in advanced electronic ignition systems.

BLOCK DIAGRAM



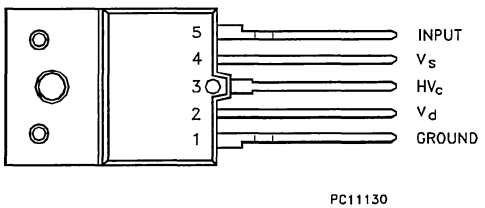
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
HV_C	Collector Voltage	Internally Limited	V
I_c	Collector Current	Internally Limited	A
V_d	Driving Stage Supply Voltage	24	V
I_d	Driving Circuitry Supply Current	350	mA
V_{in}	Maximum Input Voltage	V_s	V
V_s	Control Circuitry Supply Voltage	24	V
I_s	Control Circuitry Supply Current	200	mA
T_j	Operating Junction Temperature	-40 to 150	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction Case	(MAX)	2.5	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction Ambient	(MAX)	30	°C/W

PIN CONFIGURATION



PC11130

PIN FUNCTION

No	NAME	FUNCTION
1	GND	Emitter Power and Control Ground
2	Vd	Driver Stage Supply Voltage
3	HV_C	Output to The Primary Coil
4	Vs	Control Circuit Supply Voltage
5	INPUT	

ELECTRICAL CHARACTERISTICS ($V_b = V_{CC} = 12$ V; $T_{amb} = 25$ °C; $V_{in} = 0.4$ V; $R_S = 300\ \Omega$; $R_D = 50\ \Omega$; $R_{coil} = 500\ m\Omega$; $L_{coil} = 6$mH unless otherwise specified, see figure 1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{cl}	High Voltage Clamp	Functional Test see figs. 3 e 4	320		460	V
$V_{ce(sat)}$	Saturation Voltage of The Power Stage	$I_c = 5A$; $I_d = 40mA$; $V_{in} = 5V$ pulsed $t_{on} = 300\ \mu s$ $f_{osc} = 1$ Hz		1.5	2	V
$I_{s(on)}$	Control Circuit Supply Current	$V_{in} = 4$ V		10	25	mA
$I_{s(stand-by)}$	Control Circuit Stand-by Current	$V_{in} = 0.4$ V		5	15	mA
V_s	Control Circuit Supply Voltage		5.6		8.5	V
$I_{d(on)}$	Driver Stage Supply Current	$V_{in} = 4$ V		150	350	mA
$I_{d(stand-by)}$	Driver Stage Stand-by Current	$V_{in} = 0.4$ V			1	mA
V_d	Driver Stage Supply Voltage		5		17	V
I_{cl}	Coil Current Limit	Functional Test see figs. 3 e 4	5.5	6	6.5	A
V_{inH}	High Level Input Voltage	$I_c = 5$ A	2.4		V_s	V
V_{inL}	Low Level Input Voltage	$I_c < 2$ mA $HV_c = V_b$	0		0.8	V
I_{inH}	High Level Input Current	$V_{in} = 2.4$ V			100	µA
t_s	Storage Time	$I_c = 6$ A see figs. 1 e 2		20	30	µs
t_f	Fall Time	$I_c = 6$ A see figs. 1 e 2 & Note 1			12	µs
$E_{s/b}$	Second Breakdown Energy Clamped	$I_c = 6$ A $V_{CC} = 12$ V	300			mJ

Note 1: $V_{clamp} = 300$ V externally set

PRINCIPLE OF OPERATION

The VB020 is a high voltage, power integrated circuit with a logic level compatible input.

This part is intended for use in ignition modules or integrated into an ignition coil assembly.

The input, V_{in}, of the VB020 is fed with a logic level signal generated by an external controller or processor that determines both dwell time and ignition point. When V_{in} is high (>2.4V) the VB020 power output transistor conducts and a current controlled by the IC logic flows in the ignition coil.

The current is held constant at a level set internally by the P.I.C. until the ignition point, when Vin is driven low. During the turn-off of the transistor, the primary voltage is clamped at an internally set value, Vcl. typically 400V, in case accidental secondary open circuit conditions occur.

The transition from saturation to desaturation coil current limiting phase implies a maximum overshoot of 0.85 times the supply voltage without requiring an external RC network for frequncy compensation.

OVERVOLTAGE

The VB020 can withstand the following transient on the battery line:

-120V/2msec ($R_l = 10\ \Omega$)

100V/1msec ($R_l = 10\ \Omega$)

50V/400msec ($R_l = 2\ \Omega$, $V_{in} = 3$ V)

Figure 1 : Test Circuit.

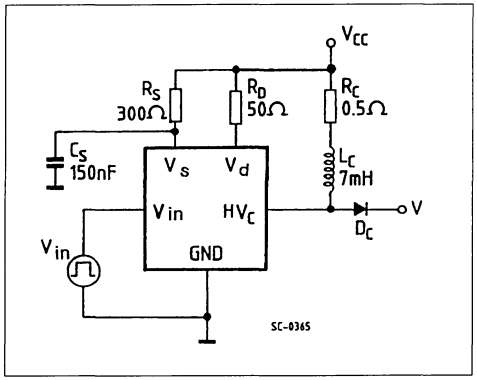


Figure 2 : Resistive Switching Waveform.

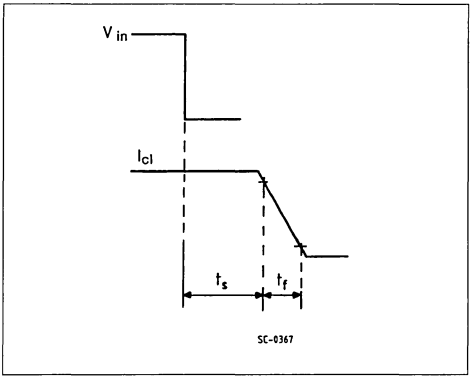
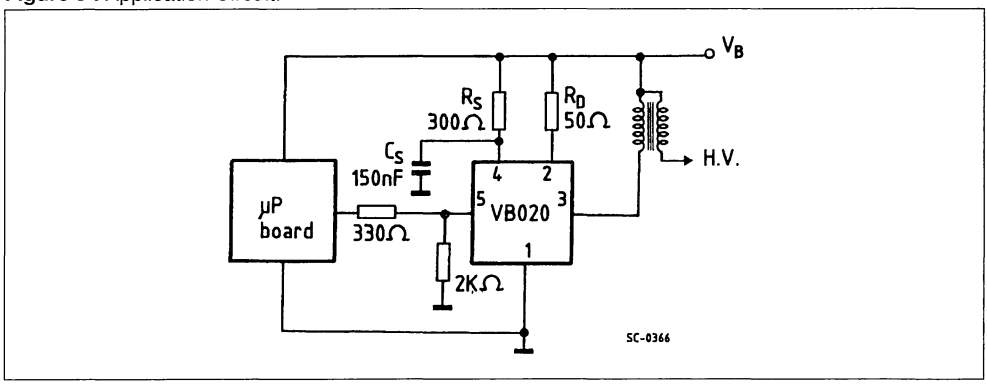
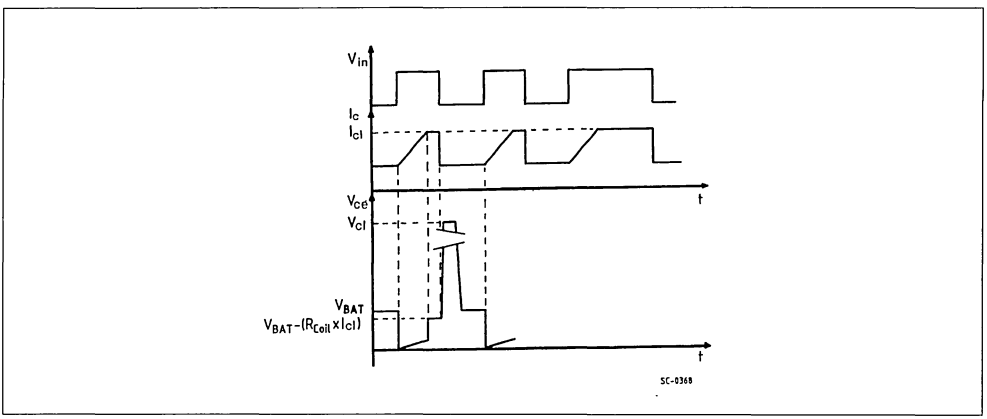


Figure 3 : Application Circuit.



Coil data: primary resistance R_C = 0.4 - 0.5 ohm.
primary inductance L_C = 6 - 8 mH.

Figure 4: Input Voltage and Output Current Waveform.



SGS-THOMSON MICROELECTRONICS

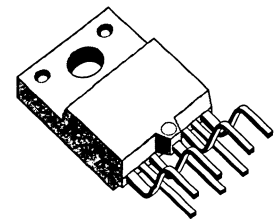
VB024

HIGH VOLTAGE IGNITION COIL DRIVER POWER IC

PRELIMINARY DATA

TYPE	V_{CL}	I_C	I_d
VB024	400 V	8 A	100 mA

- PRIMARY COIL CURRENT INTERNALLY SET
- PRIMARY COIL VOLTAGE INTERNALLY SET
- AUTOMATIC SHUT-OFF AT MAX CURRENT
- LOGIC LEVEL COMPATIBLE INPUT
- DIGITAL SIGNAL FEEDBACK TO INDICATE A PREDETERMINED CURRENT LEVEL



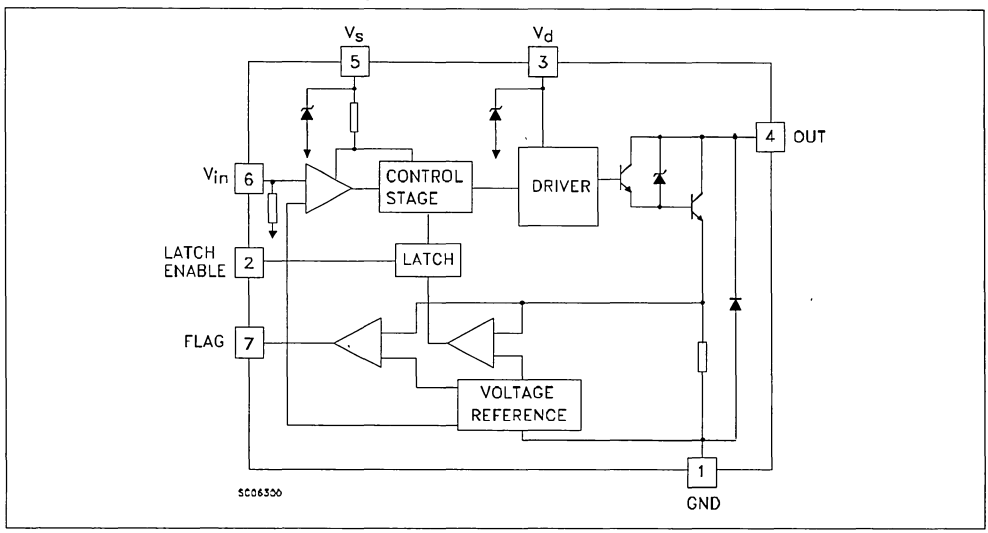
ISOWATT7

DESCRIPTION

The VB024 is a high voltage integrated circuit made using SGS-THOMSON VIPower thecnology, with vertical current flow power darlington and logic level compatible driving circuit.

The device performs the following functions: power stage for driving the primary side of the ignition coil, digital signal feedback to the control IC to indicate a predetermined current level, automatic shut-off at maximum current, self clamping for voltage flyback and logic level input.

BLOCK DIAGRAM



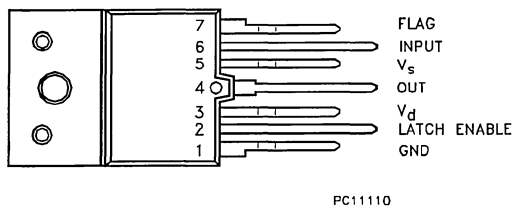
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
HV_C	Collector Voltage	Internally Limited	V
I_C	Collector Current	Internally Limited	A
V_d	Driving Stage Supply Voltage	16	V
I_d	Driving Circuitry Supply Current	600	mA
V_{in}	Maximum Input Voltage	10	V
V_s	Control Circuitry Supply Voltage	8	V
I_s	Control Circuitry Supply Current	200	mA
T_j	Operating Junction Temperature	-40 to 150	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction Case	(MAX)	2.5	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction Ambient	(MAX)	30	°C/W

CONNECTION DIAGRAM



PC11110

PIN FUNCTION

No	NAME	FUNCTION
1	GND	Emitter Power and Control Ground
2	LATCH ENABLE	Enables Of The Latch Circuitry Which Turn Off The Driver
3	Vd	Supply Voltage For The Power Stage
4	OUT	Output to The Primary Coil
5	Vs	Supply Voltage For The Control Stage
6	INPUT	
7	FLAG	Output of A Logic Signal When Ic Is Greater Than 3 A

ELECTRICAL CHARACTERISTICS (V_b = 12 V; V_s = 5 V Regulated; T_j = 25 °C; R_{coil} = 500 mΩ; L_{coil} = 6mH unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{cl}	High Voltage Clamp	V_{in} = 0.4 V -40°C ≤ T_j ≤ 125 °C	320		510	V
$V_{ce(sat)}$	Saturation Voltage of The Power Stage	I_c = 6A; I_d = 80 mA; V_{in} = 4V			2	V
$I_{s(on)}$	Control Circuit Supply Current				15	mA
V_s	Control Circuit Supply Voltage		4.5		5.5	V
$I_{d(on)}$	Driver Stage Stand-by Current	V_{in} = 4 V			180	mA
V_d	Driver Stage Supply Voltage		5.5		16	V
I_{diag}	Diagnostic Current at Wich The Flag Switches	-40°C ≤ T_j ≤ 125 °C	2.75		3.35	mA
V_{inH}	High Level Input Voltage		4		5.5	V
V_{inL}	Low Level Input Voltage		0		0.2	V
I_{inH}	High Level Input Current	V_{in} = 5.5 V	20		600	µA
V_{pos}	Positive Threshold		2.8		3.2	V
V_{neg}	Negative Threshold		1.3		1.7	V
V_{hys}	Hysteresis Voltage		1.3		1.7	V
$I_{c(max)}$	Turn-Off Current	V_{in} = 4 V -40°C ≤ T_j ≤ 125 °C	7.3		8.8	A
t_{off}	Switch-Off Time	I_c = 6 A (see note 1)	10		80	µs
V_{diagH}	High Level Diagnostic Output Voltage	R_{flag} = 20 KΩ	4		4.5	V
V_{diagL}	Low Level Diagnostic Output Volatge	R_{flag} = 100 KΩ			0.1	V

Note 1. Time fron input switching V_{neg} until V_{CL} drops to 200 V

PRINCIPLE OF OPERATION

The VB024 is designed to drive the primary side of an ignition coil and provide a logic signal output to indicate a predetermined coil current level. This output signal is used to perform dwell control. This part is intended for use in Engine Control Modules. It could also be used in an ignition module or integrated into an ignition coil assembly.

The VB024 accepts an input High signal from the control IC to start charging the primary side of the ignition coil. When the primary coil current reaches 3 amps, the VB024 outputs a logic High signal to the control IC. This flag signal is used in the calculation of the dwell time.

This device also has a maximum primary coil current $I_{c(max)}$ Shut-off feature. $I_{c(max)}$ equals aproximately 1.5 times the nominal primary coil currnet. If the Ic reaches $I_{c(max)}$, the output stage will Shut-off causing the spark to occour.

The VB024 is also internally clamped to protect it from the flyback voltage of the primary inductance as the output stage is turned off.

OVERVOLTAGE

The VB024 withstand the following transient test performed using a "Schaffner" equipment at T_A = 80 °C:

1) LOAD DUMP

Ten pulses with 10 second intervals between each transient. The device withstand load dump while fully on, fully off and during the transition between states (see figures 3 and 4).

2) NEGATIVE TRANSIENTS

Ten negative transients with 10 second intervals between each transient (see figure 5).

3) REVERSE BATTERY

Inversion of battery voltage for a time = 60 sec (see figure 5).

FIGURE1: Application Circut

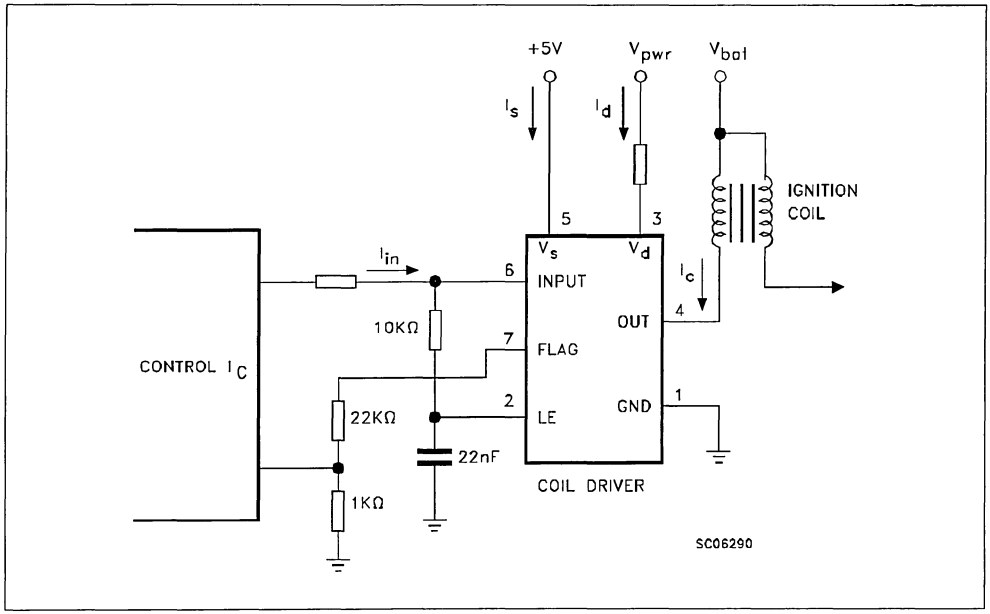


FIGURE2: Switching Waveforms

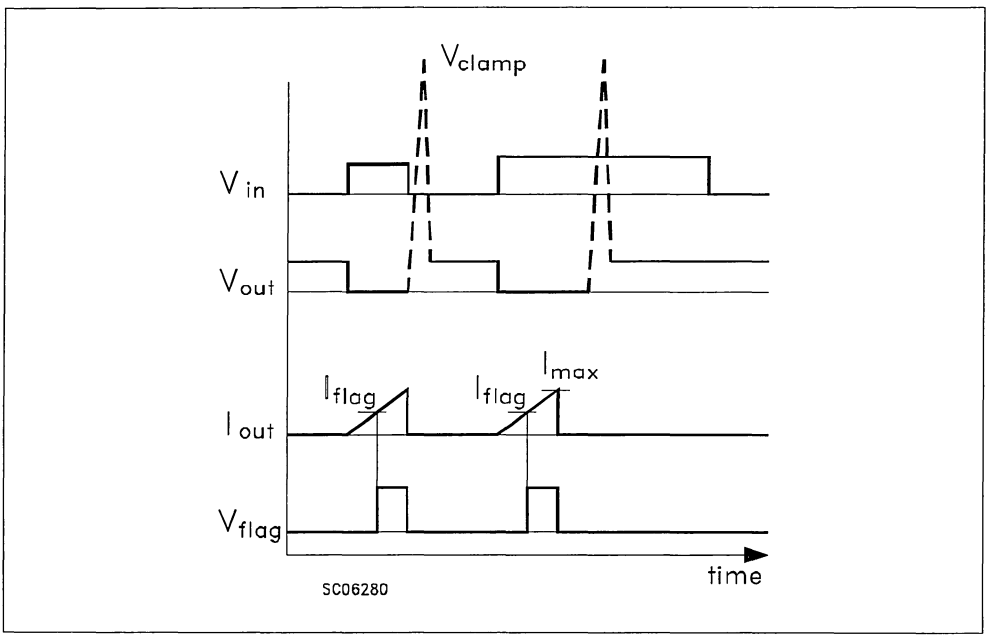


FIGURE 3: Load Dump Test Circut

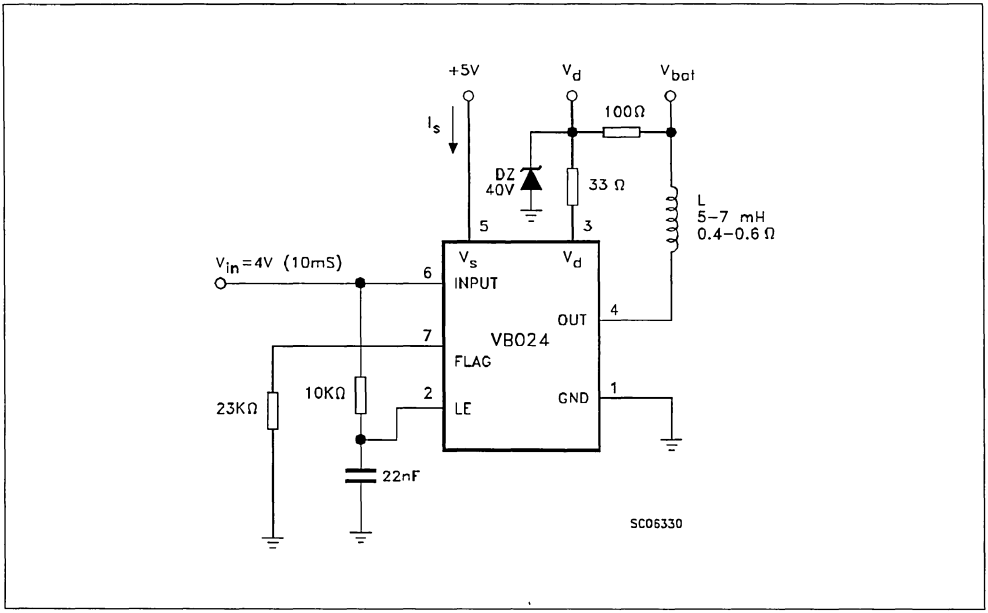


FIGURE 4: Load Dump Input Waveform

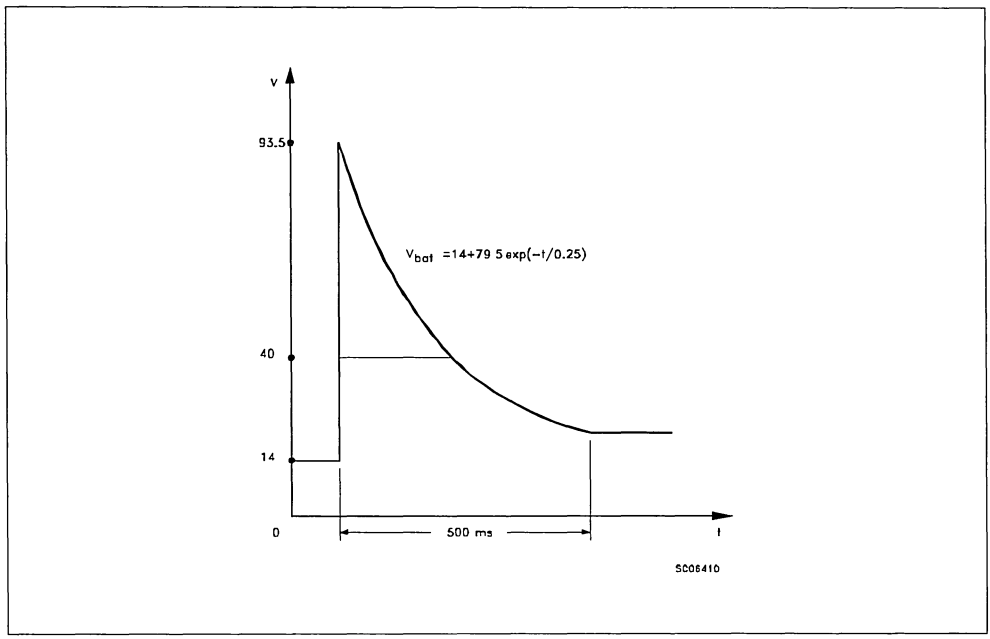


FIGURE 5: Negative Transients Test Circut

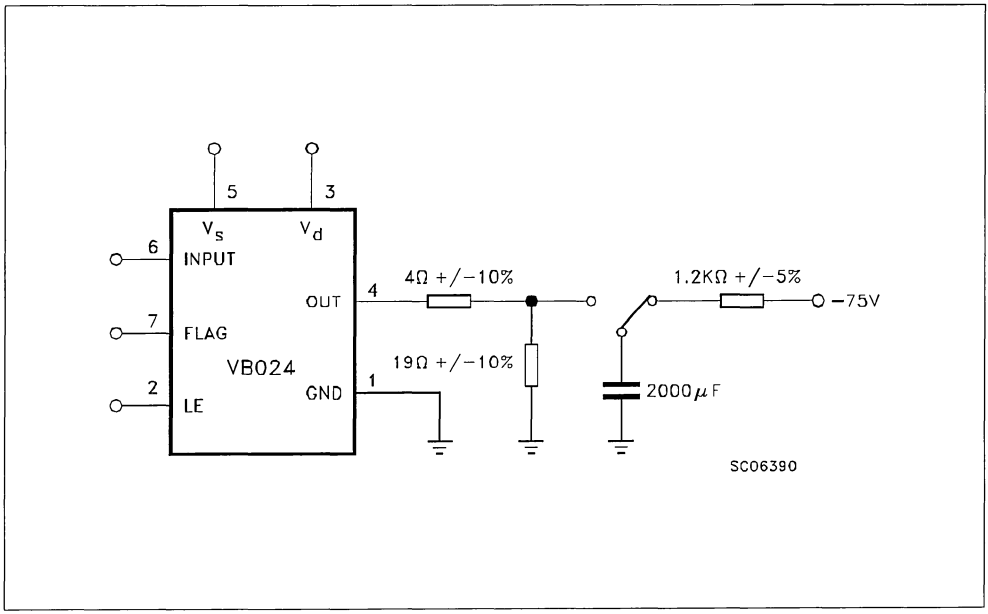
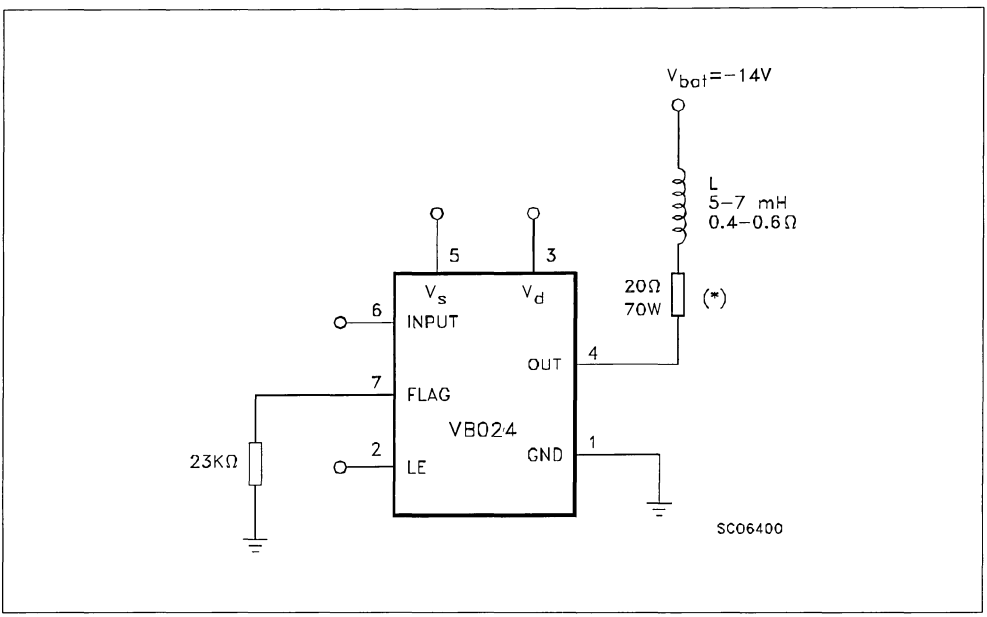


FIGURE 6: Reverse Battery Test Circuit



(*) This resistor represents vehicle wiring harness resistance

SGS-THOMSON MICROELECTRONICS

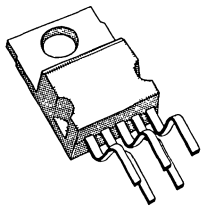
VB027

HIGH VOLTAGE IGNITION COIL DRIVER POWER IC

PRELIMINARY DATA

TYPE	V_{cl}	I_{cl}	I_d
VB027	360 V	8.5 A	80 mA

- PRIMARY COIL VOLTAGE INTERNALLY SET
- COIL CURRENT LIMIT INTERNALLY SET
- LOGIC LEVEL COMPATIBLE INPUT
- DRIVING CURRENT QUASI PROPORTIONAL TO COLLECTOR CURRENT
- DOUBLE FLAG-ON COIL CURRENT



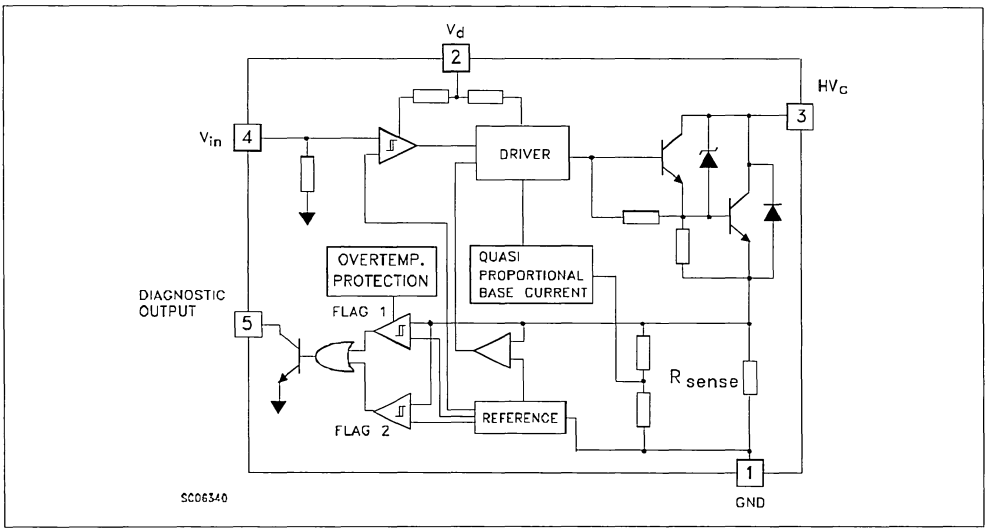
TO-220 5 LEADS

DESCRIPTION

The VB027 is a high voltage power integrated circuit made using SGS-THOMSON Microelectronics Vertical Intelligent Power Technology, with vertical current flow power darlington and logic level compatible driving circuit.

Built-in protection circuits for coil current limiting and collector voltage clamping allows the VB027 to be used as a smart, high voltage, high current interface in advanced electronic ignition systems.

BLOCK DIAGRAM



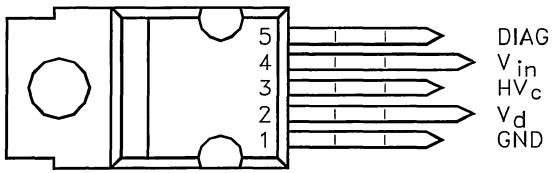
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
HV_C	Collector Voltage	Internally Limited	V
I_C	Collector Current	Internally Limited	A
V_d	Driving Stage Supply Voltage	7	V
I_d	Driving Circuitry Supply Current	200	mA
V_{in}	Maximum Input Voltage	10	V
T_j	Operating Junction Temperature	-40 to 150	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction Case	(MAX)	1.12	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction Ambient	(MAX)	62.5	°C/W

CONNECTION DIAGRAM



PC11120

PIN FUNCTION

No	NAME	FUNCTION
1	GND	Emitter Power and Control Ground
2	Vd	Supply Voltage For The Power Stage
3	HV_C	Output to The Primary Coil
4	INPUT	
5	DIAGNOSTIC	Output of a Logic Signal When Ic Is Greater Than 3 A

ELECTRICAL CHARACTERISTICS (V_b = 13.5 V; T_j = 60 °C; R_{coil} = 510 mΩ; L_{coil} = 2.85 mH; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{cl}	High Voltage Clamp	V_{in} = 0.4 V -40°C ≤ T_j ≤ 125 °C I_{coil} = 6 A	300	360	400	V
$V_{ce(sat)}$	Saturation Voltage of The Power Stage	I_c = 6A; I_d = 80 mA; V_{in} = 4V		1.6	2	V
$V_{ce(sat)dt}$	Saturation Voltage of The Power Stage Derating in Temperature	I_c = 6A; I_d = 85 mA; V_{in} = 4V -40°C ≤ T_j ≤ 125 °C			2.5	V
$I_{d(stdby)}$	Stand-by Supply Current	V_{in} = 0.4 V			10	mA
$I_{d(on)}$	Power On Supply Current	V_{in} = 4 V I_d = 6 A -40°C ≤ T_j ≤ 125 °C			130	mA
V_d	Driver Stage Supply Voltage		4.5		5.5	V
I_{cl}	Coil Current Limit	V_{in} = 4 V (see note 1)	8	8.5	9	A
$I_{cl(td)}$	Coil Current Limit Drift With Temperature	See figure 3				
V_{inH}	High Level Input Voltage	HV_c < 2 V	4		5.5	V
V_{inL}	Low Level Input Voltage	I_c < 2 mA HV_c = V_b	0		0.8	V
I_{inH}	High Level Input Current	V_{in} = 4 V	40		100	µA
V_{diagH}	High Level Diagnostic Output Voltage		3.5		V_d	V
V_{diagL}	Low Level Diagnostic Output Voltage	$I_{diagsink}$ = 2.5 mA			0.5	V
$I_{diagTH1}$	Diagnostic Current First Threshold		4.25	4.5	4.75	A
$I_{diagTD1}$	Diagnostic Current First Threshold Drift With Temperature	See figure 4				
$I_{diagTH2}$	Diagnostic Current Second Threshold		5.45	5.8	6.15	A
$I_{diagTD2}$	Diagnostic Current Second Threshold Drift With Temperature	See figure 5				
t_{dlc}	Delay Time Coil Current	I_c = 5.5 A		25		µs
t_{flc}	Fall Time Coil Current	I_c = 5.5 A		8		µs
$t_{d(diag)}$	Delay Time Diagnostic Current	R_{DIAG} = 4.7KΩ C_l = 20 pF		1		µs
$t_{r(diag)}$	Rise Time Diagnostic Current	R_{DIAG} = 4.7KΩ C_l = 20 pF		1		µs
$t_{f(diag)}$	Fall Time Diagnostic Current	R_{DIAG} = 4.7KΩ C_l = 20 pF		1		µs

Note 1. The primary coil current value Icl must be measured 1 ms afterdesaturation of the power stage

PRINCIPLE OF OPERATION

The VB027 is mainly intended as a high voltage power switch device driven by a logic level input and interfaces directly to a high energy electronic ignition coil.

The input Vin of the VB027 is fed from a low power signal generated by an external controller that determines both dwell time and ignition point.

During Vin high (≥ 4V) the VB027 increases current in the coil to the desired, internally set current level.

After reaching this level, the coil current remains constant until the ignition point, that corresponds to the transition of Vin from high to low (typ. 1.9V threshold).

During the coil current switch-off, the primary voltage HVc is clamped at an internally set value Vcl, typically 360V.

The transition from saturation to desaturation, coil current limiting phase, must have the ability to accomodate an overvoltage. A maximum overshoot of 20V is allowed.

FEEDBACK

When the collector current exceeds 4.5A, the feedback signal is turned high and it remains so, until the load current reaches 5.8A (second threshold), at that value, the feedback signal is turned low.

OVERVOLTAGE

The VB027 can withstand the following transients of the battery line:

-120V/2msec (R_i = 10 Ω)

+100V/1msec (R_i = 10 Ω)

+50V/400msec (R_i = 2 Ω, with V_{IN} = 3 V)

FIGURE1: Application Circuit

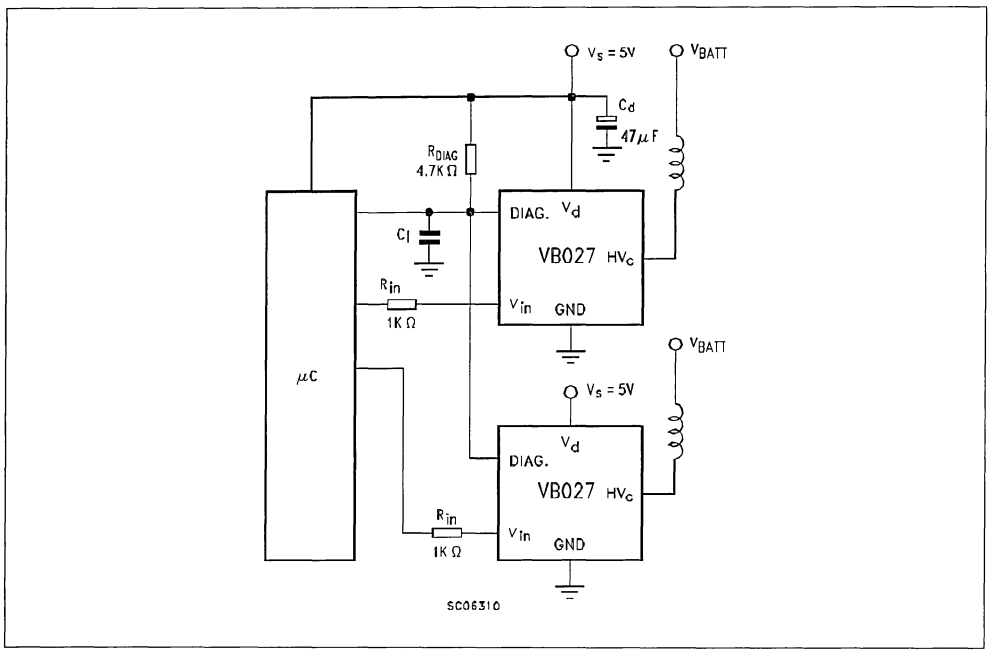


FIGURE 2: Switching Waveform

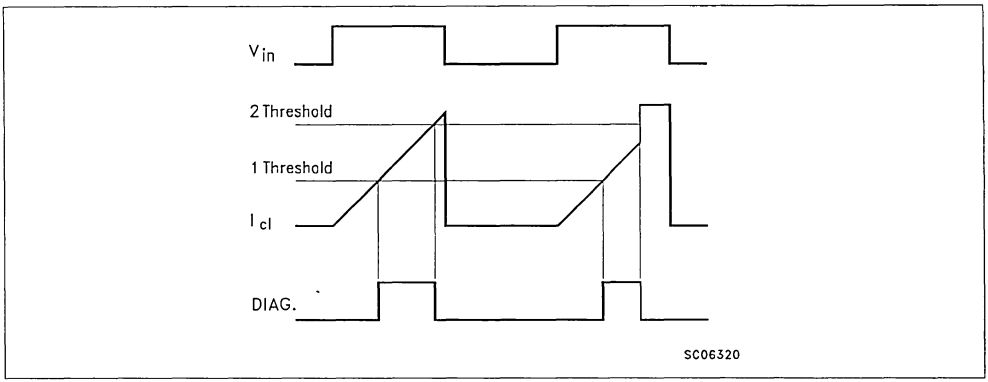


FIGURE 3: Maximum I_{cl} Versus Temperature

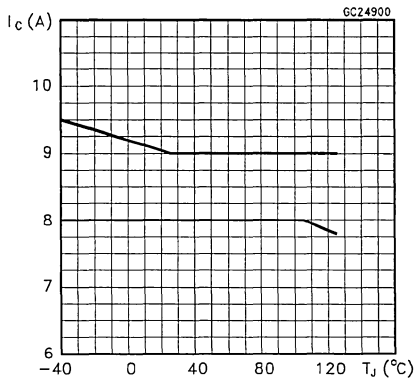


FIGURE 4: I_{flag1} Versus Temperature

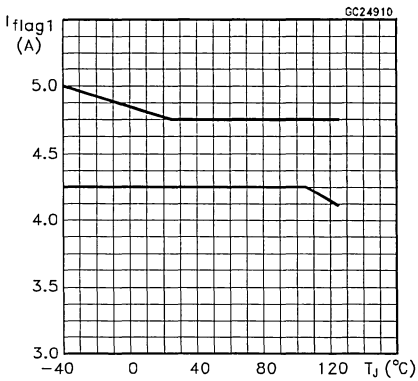
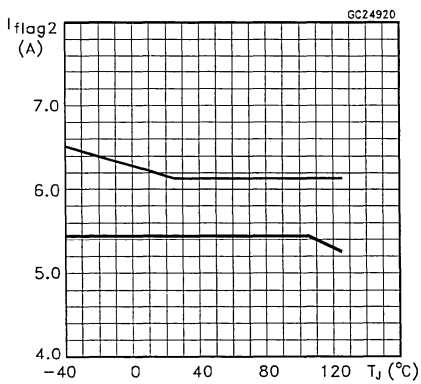


FIGURE 5: I_{flag2} Versus Temperature



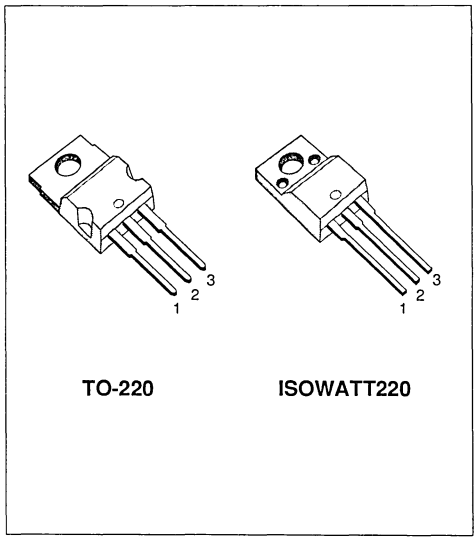
SGS-THOMSON MICROELECTRONICS

VB921Z
VB921ZFI

HIGH VOLTAGE IGNITION COIL DRIVER POWER IC

ADVANCE DATA

- NO EXTERNAL COMPONENT REQUIRED
- INTEGRATED HIGH VOLTAGE CLAMP
- COIL CURRENT LIMIT INTERNALLY SET
- HIGH RUGGEDNESS



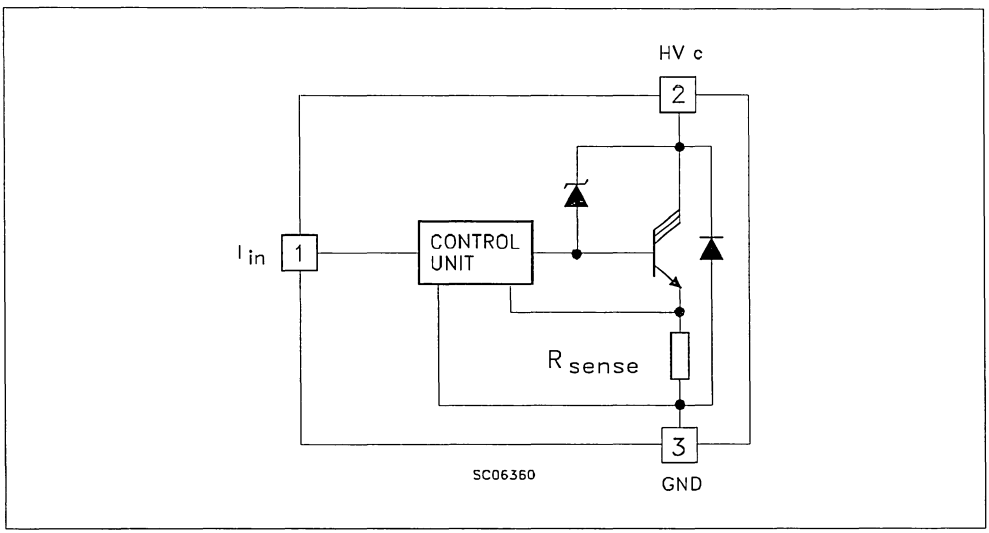
TO-220 **ISOWATT220**

DESCRIPTION

The VB921Z and VB921ZFI are monolithic high voltage integrated circuits made using SGS-THOMSON Microelectronics Vertical Intelligent Power Technology, which combines a vertical current flow power trilinton with a coil current limiting circuit and a collector voltage clamping.

The device is peculiarly suitable for application in high performance electronic car ignition, where coil current limitation and voltage clamping are required.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value		Unit
		VB921Z	VB921ZFI	
HV_c	Collector Voltage	Internally Limited		V
I_c	Collector Current	Internally Limited		A
I_{in}	Input Current	50		mA
P_{tot}	Total Dissipation at T_c = 25 °C	100	40	W
T_{stg}	Storage Temperature	-40 to 150		°C
T_j	Operating Junction Temperature	-40 to150		°C

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.25	3.12	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5		°C/W

ELECTRICAL CHARACTERISTICS (V_{batt} = 12 V, T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{cgo}	Collector Cut-off Current	V_{in} = 0 HV_c = 250 V			250	µA
V_{cl} *	Clamping Voltage	-40 < T_j < 125 °C	300		400	V
$V_{cg(sat)}$	Power Stage Saturation Voltage	I_c = 6 A I_{in} = 10 mA			2.5	V
I_{cl} *	Coil Current Limit	V_{in} = 5 V -40 ≤ T_j ≤ 125 °C	6.5	7	7.5	A
I_{in}	Input Current		10			mA
V_f **	Diode Forward Voltage	I_f = 10 A			2.5	V

* Coil data: primary resistance R_c = 0 4 - 0 8 Ω, primary inductance L_c = 6 - 8 mH

** Pulsed Pulse duration = 300 µs, duty cycle 1.5 %

SGS-THOMSON MICROELECTRONICS

VB921ZV
VB921ZVFI

HIGH VOLTAGE IGNITION COIL DRIVER POWER IC

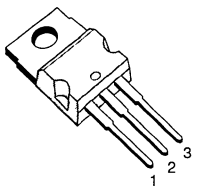
ADVANCE DATA

- NO EXTERNAL COMPONENT REQUIRED
- INTEGRATED HIGH VOLTAGE CLAMP
- COIL CURRENT LIMIT INTERNALLY SET
- HIGH RUGGEDNESS

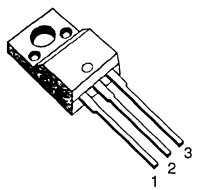
DESCRIPTION

The VB921ZV and VB921ZVFI are monolithic high voltage integrated circuits made using SGS-THOMSON Microelectronics Vertical Intelligent Power Technology, which combines a vertical current flow power trilinton with a coil current limiting circuit and a collector voltage clamping.

The device is peculiarly suitable for application in high performance electronic car ignition, where coil current limitation and voltage clamping are required.

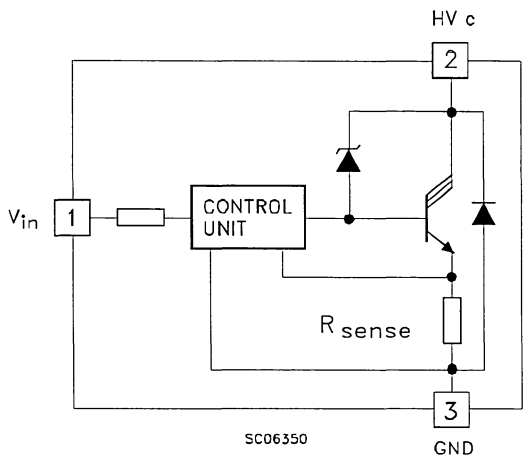


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value		Unit
		VB921Z	VB921ZFI	
HV_c	Collector Voltage	Internally Limited		V
V_{in}	Maximum Input Voltage	8		A
I_c	Collector Current	Internally Limited		A
I_{in}	Input Current	20		mA
P_{tot}	Total Dissipation at T_c = 25 °C	100	40	W
T_{stg}	Storage Temperature	-40 to 150		°C
T_j	Operating Junction Temperature	-40 to150		°C

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.25	3.12	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5		°C/W

ELECTRICAL CHARACTERISTICS (V_{batt} = 12 V, T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{cgo}	Collector Cut-off Current	V_{in} = 0 HV_c = 250 V			250	µA
V_{cl} *	Clamping Voltage	-40 < T_j < 125 °C	300		400	V
$V_{cg(sat)}$	Power Stage Saturation Voltage	I_c = 6 A I_{in} = 10 mA			2.5	V
I_{cl} *	Coil Current Limit	V_{in} = 5 V -40 ≤ T_j ≤ 125 °C see note 1	6.5	7	7.5	A
I_{in}	Input Current		8			mA
V_f **	Diode Forward Voltage	I_f = 10 A			2.5	V
V_{in}	Input Voltage		4.5		5.5	V
ΔI_{cl}	Coil Current Variation in Respect to V_{in} = 5 V	V_{in} = 4.5 - 5.5 V			200	mA

* Coil data: primary resistance R_c = 0.4 - 0.8 Ω, primary inductance L_c = 6 - 8 mH

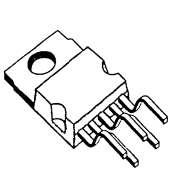
** Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

NOTE 1: I_{cl} is also controlled in respect to the variation of V_{in} between 0.5 to 5.5 V

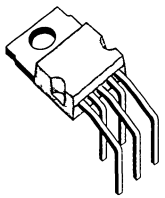
HIGH SIDE SMART POWER SOLID STATE RELAY

TYPE	V_{DSS}	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN02N	60 V	0.4 Ω	6 A	26 V

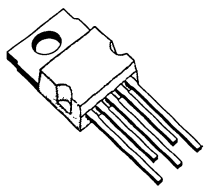
- OUTPUT CURRENT (CONTINUOUS): 6A @ T_C=25°C
- 5V LOGIC LEVEL COMPATIBLE INPUT
- THERMAL SHUT-DOWN
- UNDER VOLTAGE SHUT-DOWN
- OPEN DRAIN DIAGNOSTIC OUTPUT
- VERY LOW STAND-BY POWER DISSIPATION



PENTAWATT (vertical)



PENTAWATT (horizontal)



PENTAWATT (in-line)

ORDER CODES:

PENTAWATT vertical	VN02N
PENTAWATT horizontal	VN02N (011Y)
PENTAWATT in-line	VN02N (012Y)

DESCRIPTION

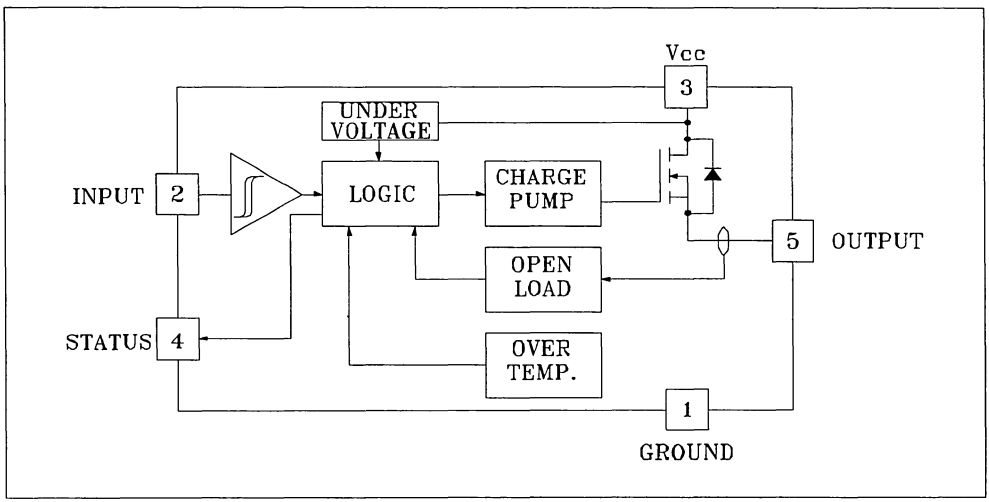
The VN02N is a monolithic device made using SGS-THOMSON Vertical Intelligent Power Technology, intended for driving resistive or inductive loads with one side grounded.

Built-in thermal shut-down protects the chip from over temperature and short circuit.

The input control is 5V logic level compatible.

The open drain diagnostic output indicates open circuit (no load) and over temperature status.

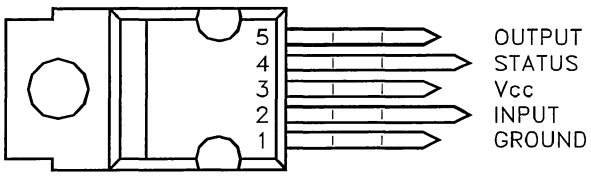
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

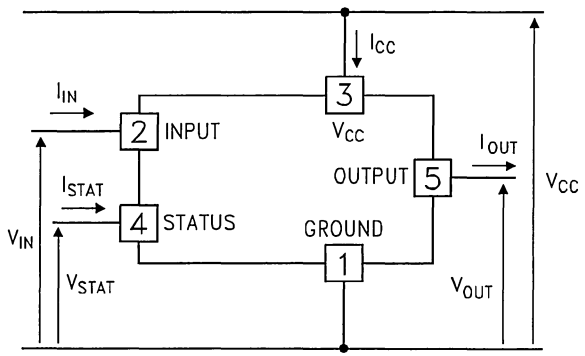
Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	V
I_{OUT}	Output Current (cont.)	6	A
I_R	Reverse Output Current	-6	A
I_{IN}	Input Current	±10	mA
$-V_{CC}$	Reverse Supply Voltage	-4	V
I_{STAT}	Status Current	±10	mA
V_{ESD}	Electrostatic Discharge (1.5 kΩ, 100 pF)	2000	V
P_{tot}	Power Dissipation at $T_c \leq 25$ °C	29	W
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

CONNECTION DIAGRAM



PC10000

CURRENT AND VOLTAGE CONVENTIONS



SC04660

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	4.35	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 13 V; -40 ≤ T_j ≤ 125 °C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		7		26	V
R_{on}	On State Resistance	I_{OUT} = 3 A I_{OUT} = 3 A T_j = 25 °C			0.8 0.4	Ω Ω
I_S	Supply Current	Off State T_j ≥ 25 °C On State			50 15	µA mA

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time Of Output Current	I_{OUT} = 3 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		10		µs
t_r	Rise Time Of Output Current	I_{OUT} = 3 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		15		µs
$t_{d(off)}$	Turn-off Delay Time Of Output Current	I_{OUT} = 3 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		15		µs
t_f	Fall Time Of Output Current	I_{OUT} = 3 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		6		µs
$(di/dt)_{on}$	Turn-on Current Slope	I_{OUT} = 3 A I_{OUT} = I_{ov}			0.5 2	A/µs A/µs
$(di/dt)_{off}$	Turn-off Current Slope	I_{OUT} = 3 A I_{OUT} = I_{ov}			2 4	A/µs A/µs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2		(*)	V
$V_{I(hyst)}$	Input Hysteresis Voltage			0.5		V
I_{IN}	Input Current	V_{IN} = 5 V		250	500	µA
V_{ICL}	Input Clamp Voltage	I_{IN} = 10 mA I_{IN} = -10 mA		6 -0.7		V V

PROTECTIONS AND DIAGNOSTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{STAT} (•)	Status Voltage Output Low	I_{STAT} = 1.6 mA			0.4	V
V_{USD}	Under Voltage Shut Down			6.5		V

ELECTRICAL CHARACTERISTICS (continued)
PROTECTION AND DIAGNOSTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SCL} (•)	Status Clamp Voltage	I_{STAT} = 10 mA I_{STAT} = -10 mA		6 -0.7		V V
t_{SC}	Switch-off Time in Short Circuit Condition at Start-Up	R_{LOAD} < 10 mΩ T_c = 25 °C		1.5	5	ms
I_{OV}	Over Current	R_{LOAD} < 10 mΩ -40 ≤ T_c ≤ 125 °C			28	A
I_{AV}	Average Current in Short Circuit	R_{LOAD} < 10 mΩ T_c = 85 °C		0.9		A
I_{OL}	Open Load Current Level		5		70	mA
T_{TSD}	Thermal Shut-down Temperature		140			°C
T_R	Reset Temperature		125			°C

(*) The V_{IH} is internally clamped at 6V about. It is possible to connect this pin to an higher voltage via an external resistor calculated to not exceed 10 mA at the input pin.
(•) Status determination > 100 µs after the switching edge.

FUNCTIONAL DESCRIPTION

The device has a diagnostic output which indicates open circuit (no load) and over temperature conditions. The output signals are processed by internal logic.

To protect the device against short circuit and over-current condition over the full range of supply voltage (V_{CC}) and temperature, the thermal protection turns the integrated Power MOS off at a minimum junction temperature of 140 °C. When the temperature returns to about 125 °C the switch is automatically turned on again.

In short circuit conditions the protection reacts with virtually no delay, the sensor being located in the region of the die where the heat is generated.

PROTECTING THE DEVICE AGAINST REVERSE BATTERY

The simplest way to protect the device against a continuous reverse battery voltage (-26V) is to insert a Schottky diode between pin 1 (GND) and ground, as shown in the typical application circuit (fig. 3).

The consequences of the voltage drop across this diode are as follows:

- If the input is pulled to power GND, a negative voltage of $-V_F$ is seen by the device. (V_{IL}, V_{IH} thresholds and V_{STAT} are increased by V_F with respect to power GND).
- The undervoltage shutdown level is increased by V_F.

If there is no need for the control unit to handle external analog signals referred to the power GND, the best approach is to connect the reference potential of the control unit to node [1] (see application circuit in fig. 4), which becomes the common signal GND for the whole control board.

In this way no shift of V_{IH}, V_{IL} and V_{STAT} takes place and no negative voltage appears on the INPUT pin; this solution allows the use of a standard diode, with a breakdown voltage able to handle any ISO normalized negative pulses that occours in the automotive environment.

TRUTH TABLE

	INPUT	OUTPUT	DIAGNOSTIC
Normal Operation	L H	L H	H H
Open Circuit (No Load)	H	H	L
Over-temperature	H	L	L
Under-voltage	X	L	H

Figure 1: Waveforms

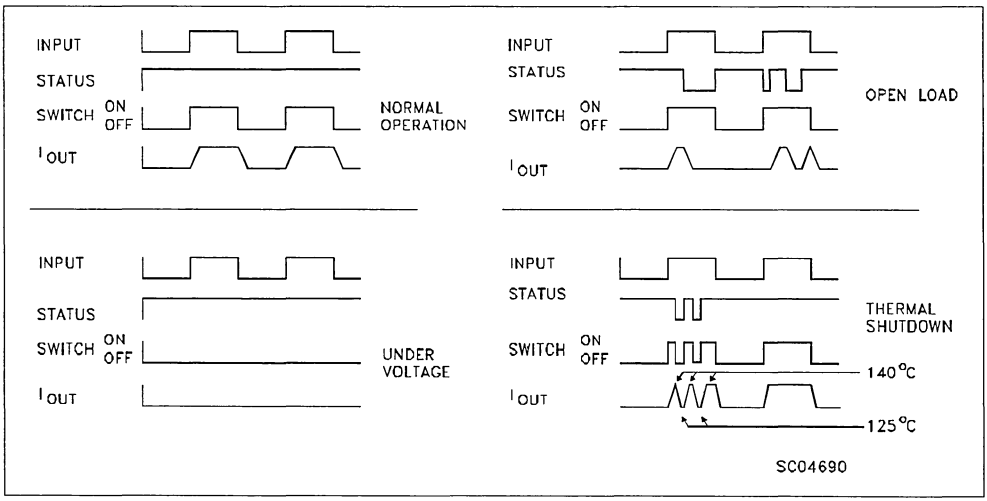


Figure 2: Over Current Test Circuit

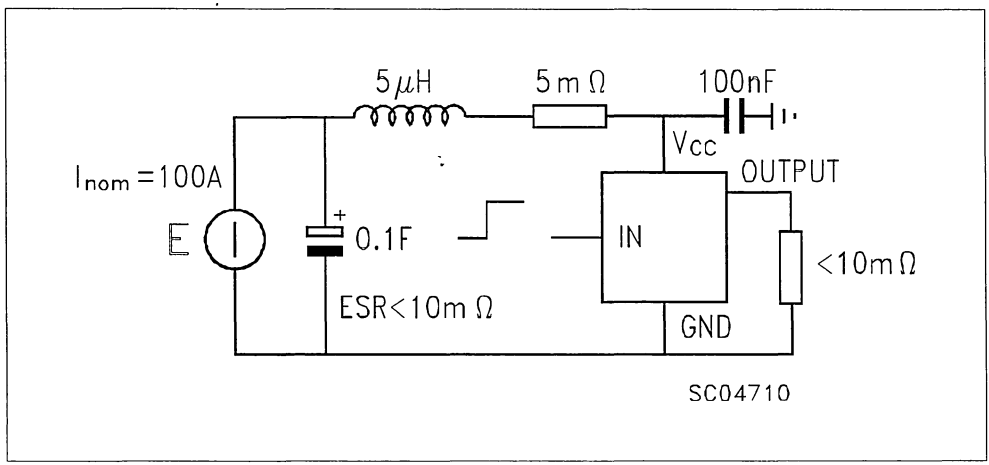


Figure 3: Typical Application Circuit With A Schottky Diode For Reverse Supply Protection

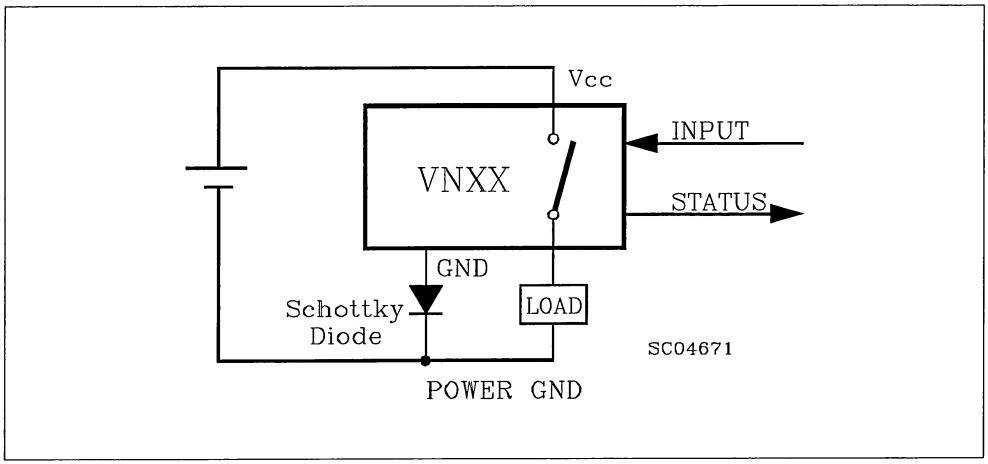
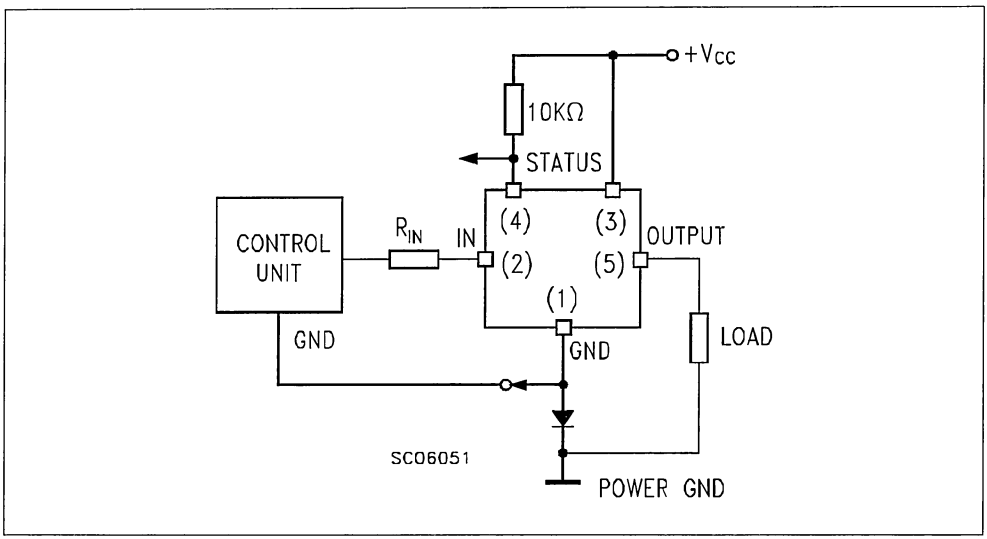
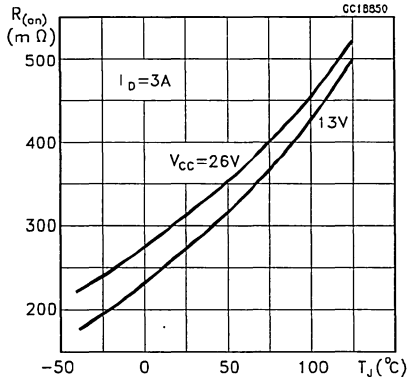


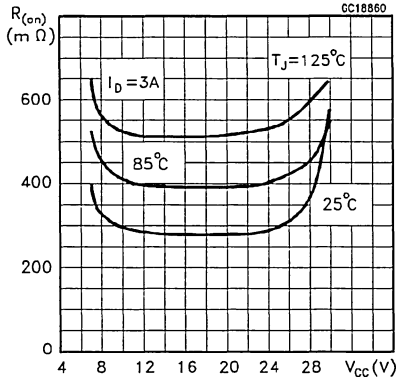
Figure 4: Typical Application Circuit With Separate Signal Ground



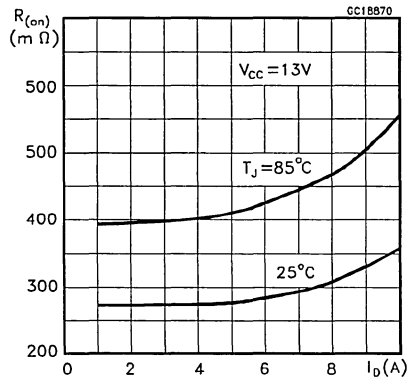
$R_{DS(on)}$ vs Junction Temperature



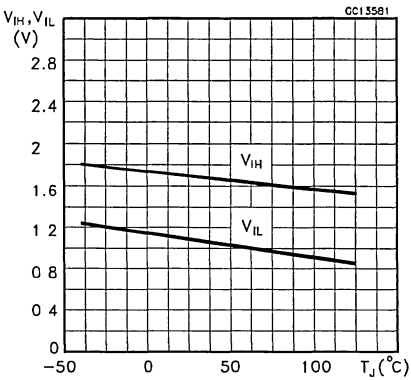
$R_{DS(on)}$ vs Supply Voltage



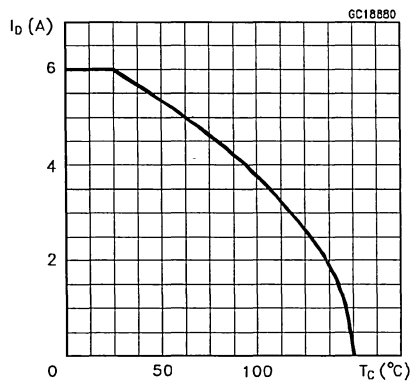
$R_{DS(on)}$ vs Output Current



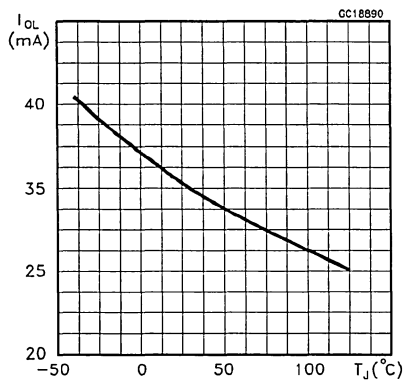
Input voltages vs Junction Temperature



Output Current Derating



Open Load vs Junction Temperature

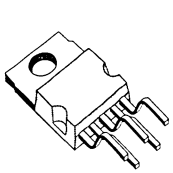


ISO HIGH SIDE SMART POWER SOLID STATE RELAY

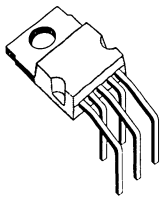
PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_n(*)	V_{CC}
VN03	60 V	0.5 Ω	0.7 A	26 V

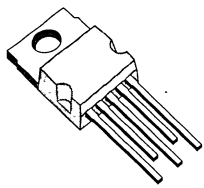
- MAXIMUM CONTINUOUS OUTPUT CURRENT (#): 4 A @ T_c= 85°C
- 5V LOGIC LEVEL COMPATIBLE INPUT
- THERMAL SHUT-DOWN
- UNDER VOLTAGE PROTECTION
- OPEN DRAIN DIAGNOSTIC OUTPUT
- INDUCTIVE LOAD FAST DEMAGNETIZATION
- VERY LOW STAND-BY POWER DISSIPATION



PENTAWATT (vertical)



PENTAWATT (horizontal)



PENTAWATT (in-line)

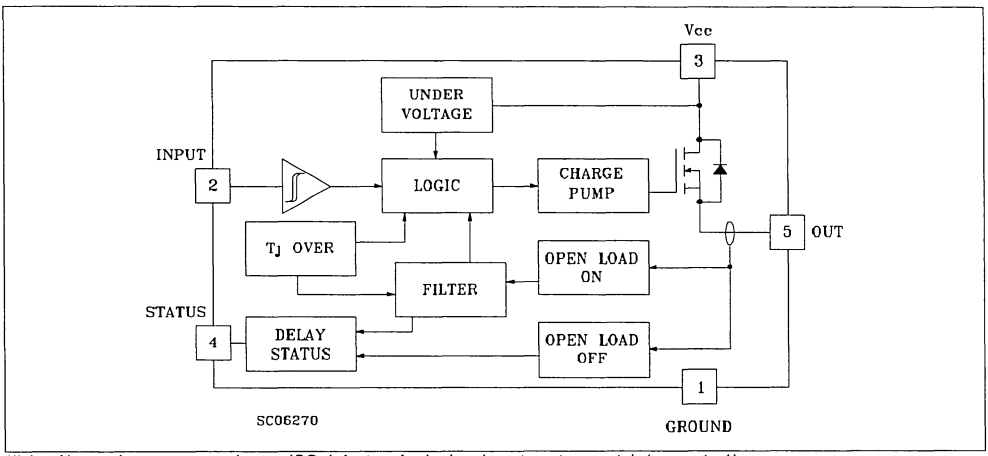
ORDER CODES:

PENTAWATT vertical	VN03
PENTAWATT horizontal	VN03 (011Y)
PENTAWATT in-line	VN03 (012Y)

DESCRIPTION

The VN03 is a monolithic device made using SGS-THOMSON Vertical Intelligent Power Technology, intended for driving resistive or inductive loads with one side grounded.
Built-in thermal shut-down protects the chip from over temperature and short circuit.
The open drain diagnostic output indicates: open load in off state and in on state, output shorted to V_{CC} and overtemperature. Fast demagnetization of inductive loads is archieved by negative (-18V) load voltage at turn-off.

BLOCK DIAGRAM

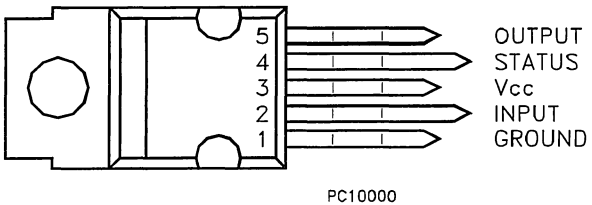


(*) In= Nominal current according to ISO definition for high side automotive switch (see note 1)
(#) The maximum continuous output current is the current at T_c = 85 °C for a battery voltage of 13 V which does not activate self protection

ABSOLUTE MAXIMUM RATING

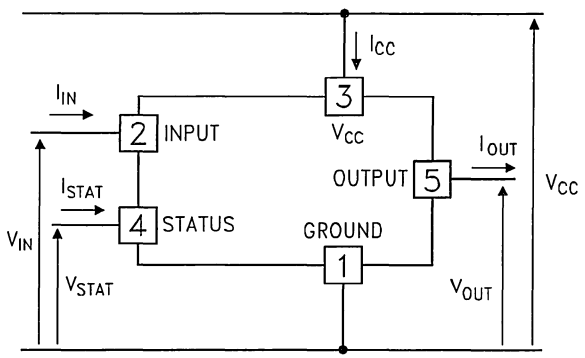
Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	V
I_{OUT}	Output Current (cont.) at T_c = 85 °C	4	A
I_R	Reverse Output Current at T_c = 85 °C	-4	A
I_{IN}	Input Current	±10	mA
$-V_{CC}$	Reverse Supply Voltage	-4	V
I_{STAT}	Status Current	±10	mA
V_{ESD}	Electrostatic Discharge (1.5 kΩ, 100 pF)	2000	V
P_{tot}	Power Dissipation at T_c = 85 °C	14	W
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

CONNECTION DIAGRAM



PC10000

CURRENT AND VOLTAGE CONVENTIONS



SC04660

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 13 V; -40 ≤ T_j ≤ 125 °C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		5.5	13	26	V
In(*)	Nominal Current	T_c = 85 °C $V_{DS(on)} \leq 0.5$ (note 1)	0.7			A
R_{on}	On State Resistance	I_{OUT} = 0.7 A I_{OUT} = 0.7 A T_j = 25 °C			1 0.5	Ω Ω
I_S	Supply Current	Off State $T_j \geq$ 25 °C On State			50 15	µA mA
$V_{DS(MAX)}$	Maximum Voltage Drop	I_{OUT} = 4 A T_c = 85 °C			3.6	V

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(^)	Turn-on Delay Time Of Output Current	I_{OUT} = 0.7 A Resistive Load Input Rise Time < 0.1 µs		15		µs
t_r(^)	Rise Time Of Output Current	I_{OUT} = 0.7 A Resistive Load Input Rise Time < 0.1 µs		10		µs
$t_{d(off)}$(^)	Turn-off Delay Time Of Output Current	I_{OUT} = 0.7 A Resistive Load Input Rise Time < 0.1 µs		15		µs
t_f(^)	Fall Time Of Output Current	I_{OUT} = 0.7 A Resistive Load Input Rise Time < 0.1 µs		4		µs
$(di/dt)_{on}$	Turn-on Current Slope	I_{OUT} = 0.7 A I_{OUT} = I_{OV}		0.05	0.5 1	A/µs A/µs
$(di/dt)_{off}$	Turn-off Current Slope	I_{OUT} = 0.7 A I_{OUT} = I_{OV}		0.14	3 3	A/µs A/µs
V_{demag}	Inductive Load Clamp Voltage	I_{OUT} = 0.7 A L = 1 mH	-24	-18	-14	V

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2		(•)	V
$V_{I(hyst)}$	Input Hysteresis Voltage			0.5		V
I_{IN}	Input Current	V_{IN} = 5 V V_{IN} = 2 V V_{IN} = 0.8 V	 25	250	500 250	µA µA µA
V_{ICL}	Input Clamp Voltage	I_{IN} = 10 mA I_{IN} = -10 mA	5.5	6 -0.7	 -0.3	V V

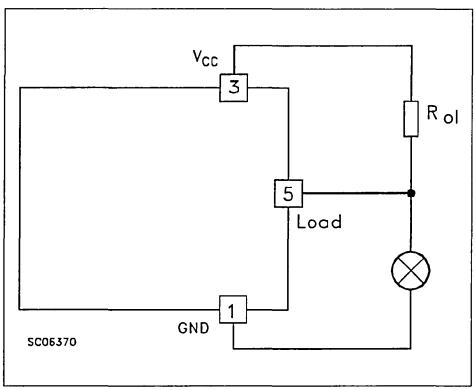
ELECTRICAL CHARACTERISTICS (continued)

PROTECTION AND DIAGNOSTICS (continued)

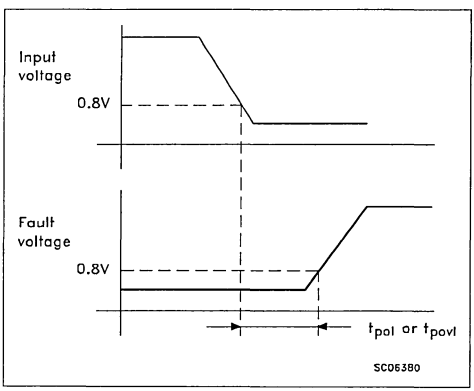
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status Voltage Output Low	I_{STAT} = 1.6 mA			0.4	V
V_{USD}	Under Voltage Shut Down			5		V
V_{SCL}	Status Clamp Voltage	I_{STAT} = 10 mA I_{STAT} = -10 mA		6 -0.7		V V
I_{OV}	Over Current	R_{LOAD} < 10 mΩ -40 ≤ T_c ≤ 125 °C			28	A
I_{AV}	Average Current in Short Circuit	R_{LOAD} < 10 mΩ T_c = 85 °C		0.9		A
I_{OL}	Open Load Current Level		5	35	70	mA
T_{TSD}	Thermal Shut-down Temperature		140			°C
T_R	Reset Temperature		125			°C
V_{OL}	Open Load Voltage Level	Off-State (note 2)	2.5	3.75	5	V
$t_{1(on)}$	Open Load Filtering Time	(note 3)	1	5	10	ms
$t_{1(off)}$	Open Load Filtering Time	(note 3)	1	5	10	ms
$t_{2(off)}$	Open Load Filtering Time	(note 3)	1	5	10	ms
t_{povl}	Status Delay	(note 3)		5	10	µs
t_{pol}	Status Delay	(note 3)	50	700		µs

(^) See Switchig Time Waveforms
(•) The V_{IH} is internally clamped at 6V about. It is possible to connect this pin to an higher voltage via an external resistor calculated to not exceed 10 mA at the input pin
note 1: The Nominal Current is the current at T_c = 85 °C for battery voltage of 13V which produces a voltage drop of 0.5 V
note 2: $I_{OL(off)} = (V_{CC} - V_{OL})/R_{OL}$ (see figure)
note 3: $t_{1(on)}$: minimum open load duration which acctivates the status output
$t_{1(off)}$: minimum load recovery time which desactivates the status output
$t_{2(off)}$: minimum on time after thermal shut down which desactivates status output
t_{povl} t_{pol}: ISO definition (see figure)

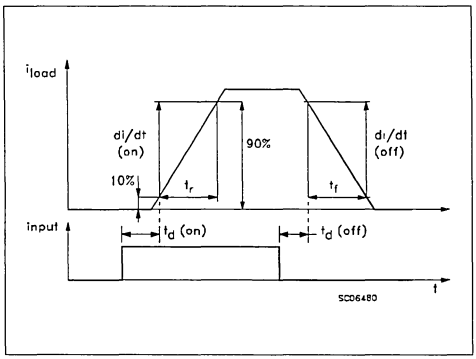
Note 2 Relevant Figure



Note 3 Relevant Figure



Switching Time Waveforms



FUNCTIONAL DESCRIPTION

The device has a diagnostic output which indicates open load conditions in off state as well as in on state, output shorted to V_{CC} and overtemperature. The truth table shows input, diagnostic and output voltage level in normal operation and in fault conditions. The output signals are processed by internal logic. The open load diagnostic output has a 5 ms filtering. The filter gives a continuous signal for the fault condition after an initial delay of about 5 ms. This means that a disconnection during normal operation, with a duration of less than 5 ms does not affect the status output. Equally, any re-connection of less than 5 ms during a disconnection duration does not affect the status output. No delay occur for the status to go low in case of overtemperature conditions. From the falling edge of the input signal the status output initially low in fault condition (over temperature or open load) will go back with a delay (t_{povl})in case of overtemperature condition and a delay (t_{pol}) in case of open load. These feature fully comply with International Standard Office (I.S.O.) requirement for automotive High Side Driver.

To protect the device against short circuit and over current conditions over the full range of supply voltage (V_{CC}) and temperature, the thermal protection turns the integrated Power MOS off at a minimum junction temperature of 140 °C. When the temperature returns to 125 °C the switch is automatically turned on again. In short circuit the protection reacts with virtually no delay, the sensor being located in the region of the die where the heat is generated. Driving inductive loads, an internal function of the device ensures the fast demagnetization with a typical voltage (V_{demag}) of -18V.

This function allows to greatly reduce the power dissipation according to the formula:

$P_{dem} = 0.5 \bullet L_{load} \bullet (I_{load})^2 \bullet [(V_{CC}+V_{demag})/V_{demag}] \bullet f$

where f = switching frequency and

V_{demag} = demagnetization voltage

Based on this formula it is possible to know the value of inductance and/or current to avoid a thermal shut-down. The maximum inductance which causes the chip temperature to reach the shut down temperature in a specific thermal environment, is infact a function of the load current for a fixed V_{CC}, V_{demag} and f.

PROTECTING THE DEVICE AGAIST LOAD DUMP - TEST PULSE 5

The device is able to withstand the test pulse No. 5 at level II (V_s = 46.5V) according to the ISO T/R 7637/1 without any external component. This means that all functions of the device are performed as designed after exposure to disturbance at level II. The VN03 is able to withstand the test pulse No.5 at level III adding an external resistor of 150 ohm between pin 1 and ground plus a filter capacitor of 1000 µF between pin 3 and ground (if $R_{LOAD} \leq 20\ \Omega$).

PROTECTING THE DEVICE AGAINST REVERSE BATTERY

The simplest way to protect the device against a continuous reverse battery voltage (-26V) is to insert a Schottky diode between pin 1(GND) and ground, as shown in the typical application circuit (fig.3).

The consequences of the voltage drop across this diode are as follows:

- If the input is pulled to power GND, a negative voltage of $-V_f$ is seen by the device. (Vil, Vih thresholds and Vstat are increased by Vf with respect to power GND).
- The undervoltage shutdown level is increased by Vf.

If there is no need for the control unit to handle external analog signals referred to the power GND, the best approach is to connect the reference potential of the control unit to node [1] (see application circuit in fig. 4), which becomes the common signal GND for the whole control board avoiding shift of V_{ih}, V_{il} and V_{stat}. This solution allows the use of a standard diode.

TRUTH TABLE

	INPUT	OUTPUT	DIAGNOSTIC
Normal Operation	L H	L H	H H
Over-temperature	H	L	L
Under-voltage	X	L	H
Short load to V_{CC}	L	H	L

Figure 1: Waveforms

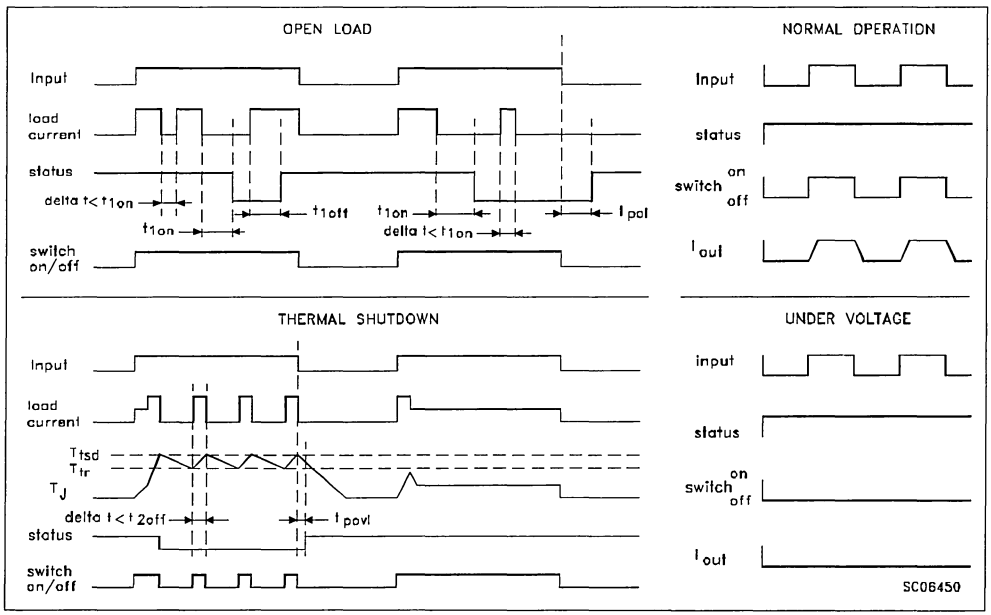


Figure 2: Over Current Test Circuit

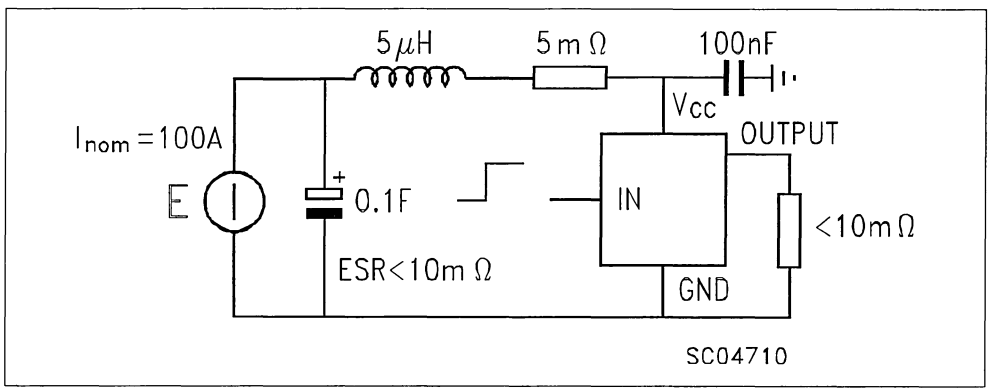


Figure 3: Typical Application Circuit With A Schottky Diode For Reverse Supply Protection

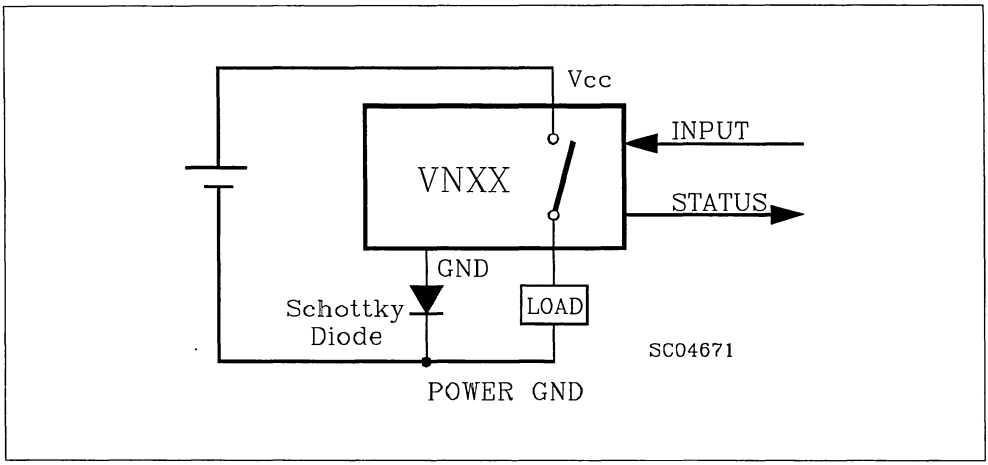
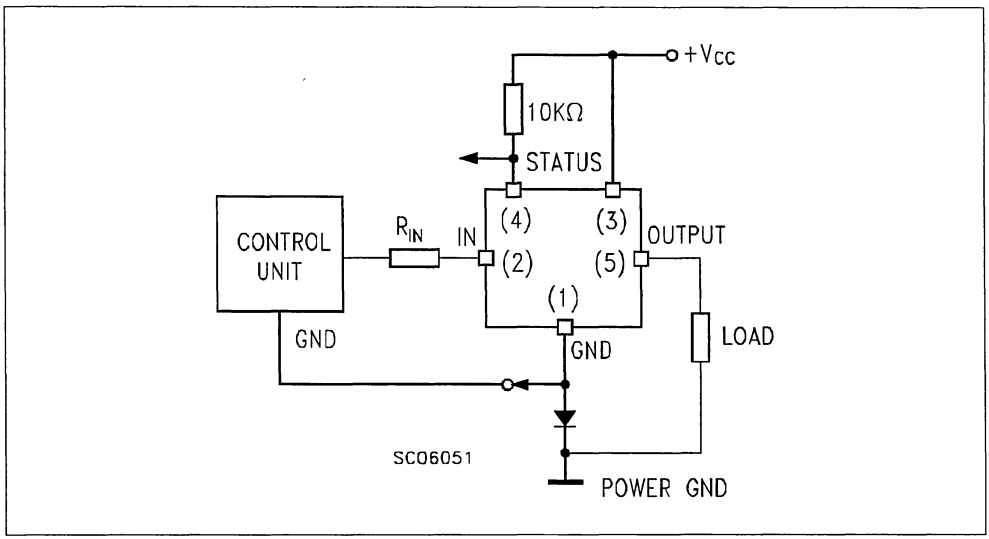


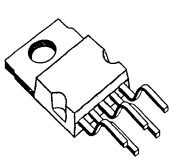
Figure 4: Typical Application Circuit With Separate Signal Ground



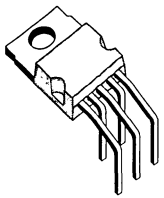
HIGH SIDE SMART POWER SOLID STATE RELAY

TYPE	V_{DSS}	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN05N	60 V	0.18 Ω	12 A	26 V

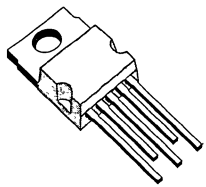
- OUTPUT CURRENT (CONTINUOUS): 12A @ T_C=25°C
- 5V LOGIC LEVEL COMPATIBLE INPUT
- THERMAL SHUT-DOWN
- UNDER VOLTAGE SHUT-DOWN
- OPEN DRAIN DIAGNOSTIC OUTPUT
- VERY LOW STAND-BY POWER DISSIPATION



PENTAWATT (vertical)



PENTAWATT (horizontal)



PENTAWATT (in-line)

ORDER CODES:

PENTAWATT vertical	VN05N
PENTAWATT horizontal	VN05N (011Y)
PENTAWATT in-line	VN05N (012Y)

DESCRIPTION

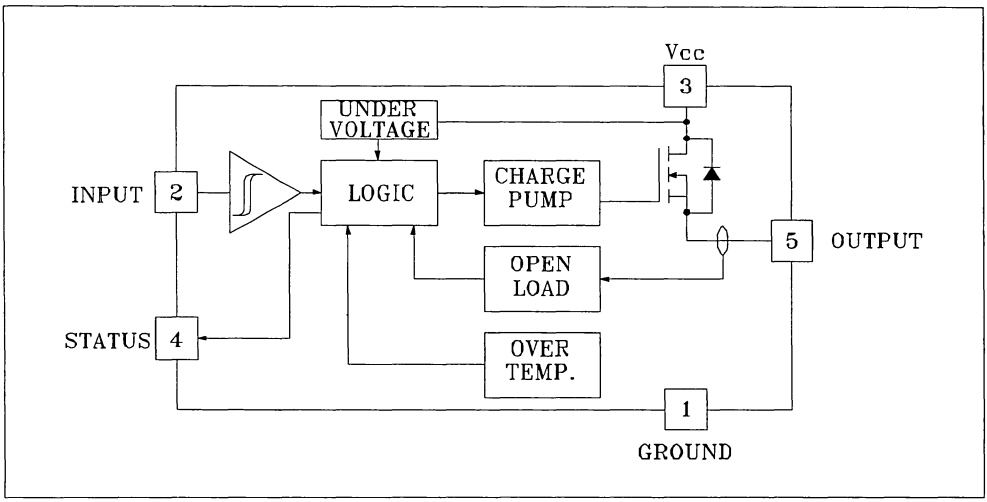
The VN05N is a monolithic device made using SGS-THOMSON Vertical Intelligent Power Technology, intended for driving resistive or inductive loads with one side grounded.

Built-in thermal shut-down protects the chip from over temperature and short circuit.

The input control is 5V logic level compatible.

The open drain diagnostic output indicates open circuit (no load) and over temperature status.

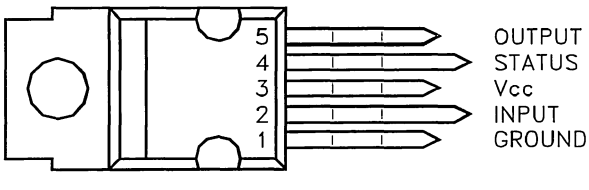
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

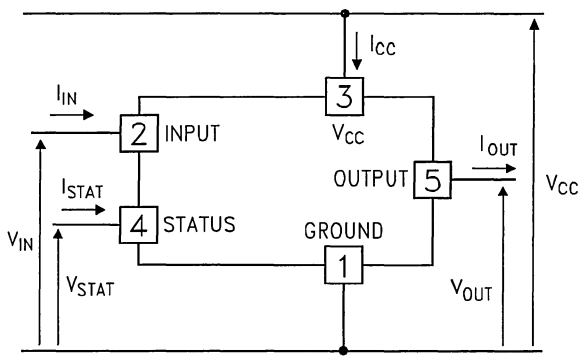
Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	V
I_{OUT}	Output Current (cont.)	12	A
I_R	Reverse Output Current	-12	A
I_{IN}	Input Current	±10	mA
$-V_{CC}$	Reverse Supply Voltage	-4	V
I_{STAT}	Status Current	±10	mA
V_{ESD}	Electrostatic Discharge (1.5 kΩ, 100 pF)	2000	V
P_{tot}	Power Dissipation at $T_c \leq 25$ °C	52	W
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

CONNECTION DIAGRAM



PC10000

CURRENT AND VOLTAGE CONVENTIONS



SC04660

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.4	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 13 V; -40 ≤ T_j ≤ 125 °C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		7		26	V
R_{on}	On State Resistance	I_{OUT} = 6 A I_{OUT} = 6 A T_j = 25 °C			0.36 0.18	Ω Ω
I_S	Supply Current	Off State T_j ≥ 25 °C On State			50 15	µA mA

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time Of Output Current	I_{OUT} = 6 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		15		µs
t_r	Rise Time Of Output Current	I_{OUT} = 6 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		30		µs
$t_{d(off)}$	Turn-off Delay Time Of Output Current	I_{OUT} = 6 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		20		µs
t_f	Fall Time Of Output Current	I_{OUT} = 6 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		10		µs
$(di/dt)_{on}$	Turn-on Current Slope	I_{OUT} = 6 A I_{OUT} = Iov			0.5 2	A/µs A/µs
$(di/dt)_{off}$	Turn-off Current Slope	I_{OUT} = 6 A I_{OUT} = Iov			2 4	A/µs A/µs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2		(*)	V
$V_{I(hyst)}$	Input Hysteresis Voltage			0.5		V
I_{IN}	Input Current	V_{IN} = 5 V		250	500	µA
V_{ICL}	Input Clamp Voltage	I_{IN} = 10 mA I_{IN} = -10 mA		6 -0.7		V V

PROTECTIONS AND DIAGNOSTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{STAT} (•)	Status Voltage Output Low	I_{STAT} = 1.6 mA			0.4	V
V_{USD}	Under Voltage Shut Down			6.5		V

ELECTRICAL CHARACTERISTICS (continued)
PROTECTION AND DIAGNOSTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SCL} (•)	Status Clamp Voltage	I_{STAT} = 10 mA I_{STAT} = -10 mA		6 -0.7		V V
t_{SC}	Switch-off Time in Short Circuit Condition at Start-Up	R_{LOAD} < 10 mΩ T_c = 25 °C		1.5	5	ms
I_{OV}	Over Current	R_{LOAD} < 10 mΩ -40 ≤ T_c ≤ 125 °C			60	A
I_{AV}	Average Current in Short Circuit	R_{LOAD} < 10 mΩ T_c = 85 °C		1.4		A
I_{OL}	Open Load Current Level		5		180	mA
T_{TSD}	Thermal Shut-down Temperature		140			°C
T_R	Reset Temperature		125			°C

(*) The V_{IH} is internally clamped at 6V about. It is possible to connect this pin to an higher voltage via an external resistor calculated to not exceed 10 mA at the input pin.
(•) Status determination > 100 µs after the switching edge

FUNCTIONAL DESCRIPTION
The device has a diagnostic output which indicates open circuit (no load) and over temperature conditions. The output signals are processed by internal logic.

To protect the device against short circuit and over-current condition over the full range of supply voltage (V_{CC}) and temperature, the thermal protection turns the integrated Power MOS off at a minimum junction temperature of 140 °C. When the temperature returns to about 125 °C the switch is automatically turned on again.

In short circuit conditions the protection reacts with virtually no delay, the sensor being located in the region of the die where the heat is generated.

PROTECTING THE DEVICE AGAINST REVERSE BATTERY
The simplest way to protect the device against a continuous reverse battery voltage (-26V) is to insert a Schottky diode between pin 1 (GND) and ground, as shown in the typical application circuit (fig. 3).

The consequences of the voltage drop across this diode are as follows:

— If the input is pulled to power GND, a negative voltage of -V_F is seen by the device. (V_{IL}, V_{IH} thresholds and V_{STAT} are increased by V_F with respect to power GND).

— The undervoltage shutdown level is increased by V_F.

If there is no need for the control unit to handle external analog signals referred to the power GND, the best approach is to connect the reference potential of the control unit to node [1] (see application circuit in fig. 4), which becomes the common signal GND for the whole control board.

In this way no shift of V_{IH}, V_{IL} and V_{STAT} takes place and no negative voltage appears on the INPUT pin; this solution allows the use of a standard diode, with a breakdown voltage able to handle any ISO normalized negative pulses that occours in the automotive environment.

TRUTH TABLE

	INPUT	OUTPUT	DIAGNOSTIC
Normal Operation	L H	L H	H H
Open Circuit (No Load)	H	H	L
Over-temperature	H	L	L
Under-voltage	X	L	H

Figure 1: Waveforms

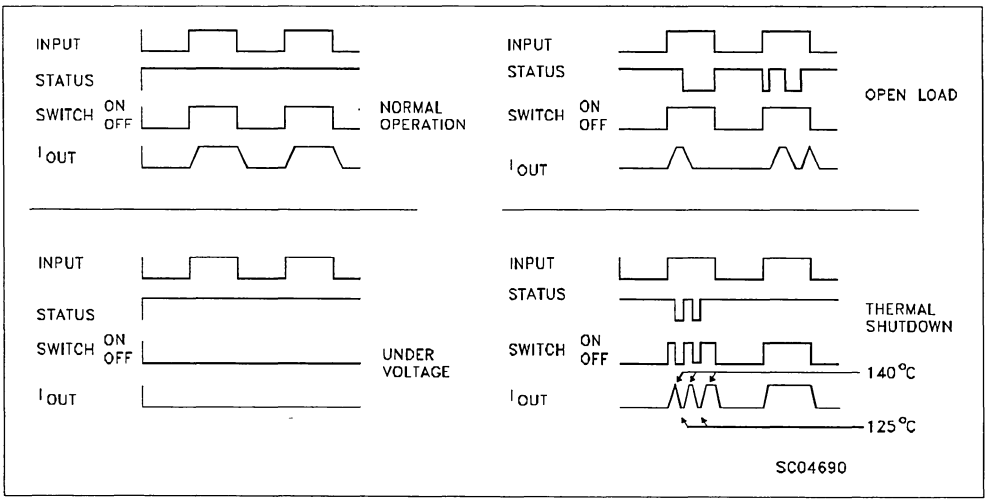


Figure 2: Over Current Test Circuit

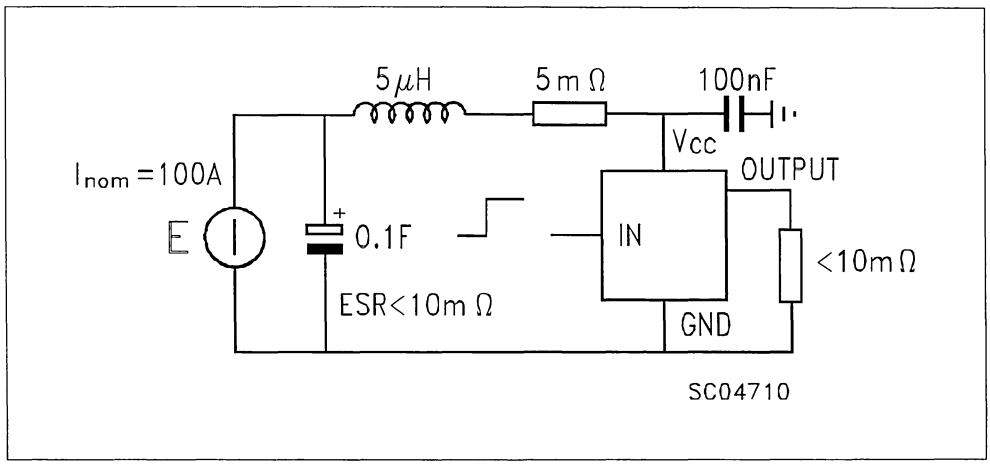


Figure 3: Typical Application Circuit With A Schottky Diode For Reverse Supply Protection

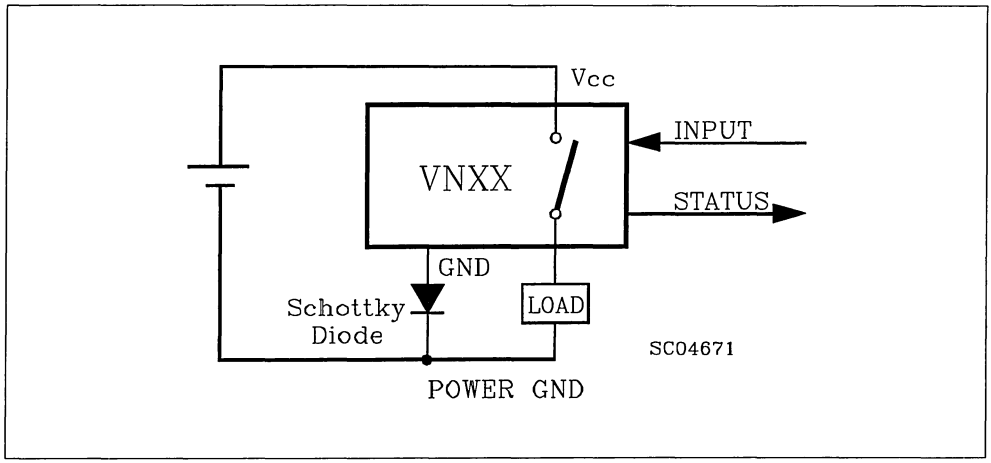
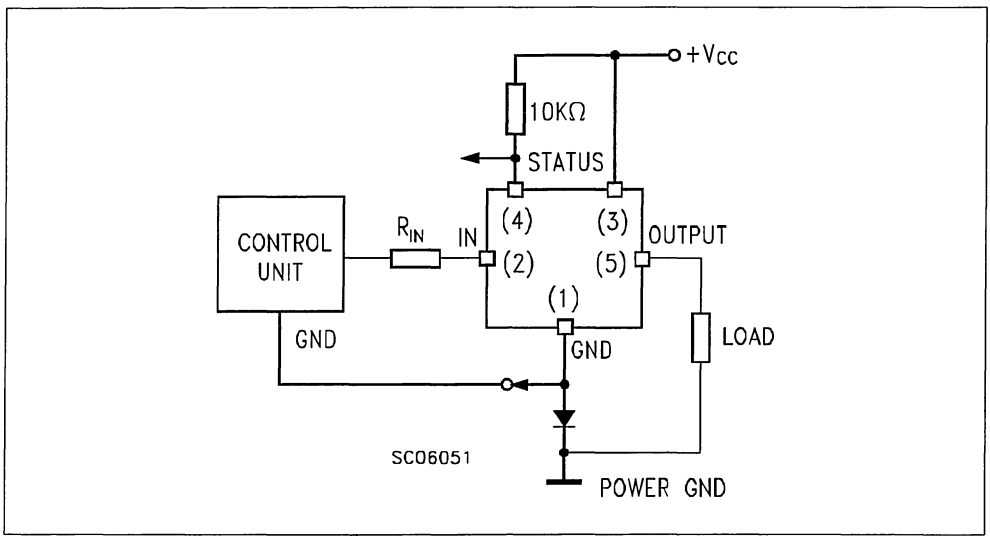
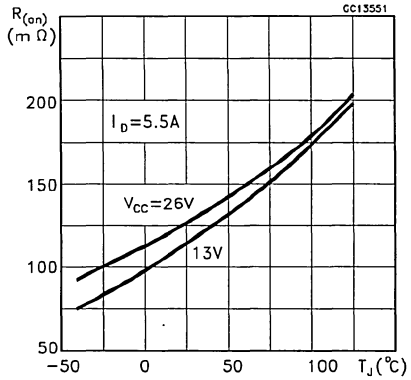


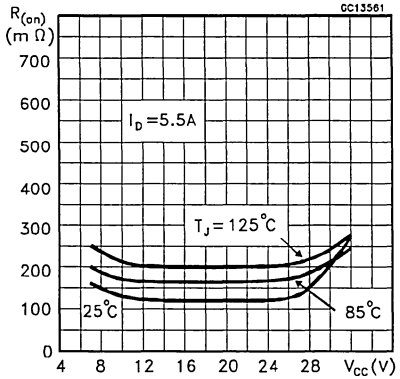
Figure 4: Typical Application Circuit With Separate Signal Ground



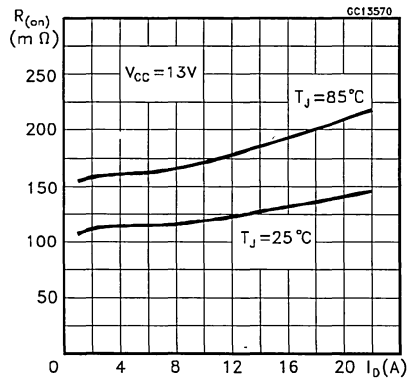
$R_{DS(on)}$ vs Junction Temperature



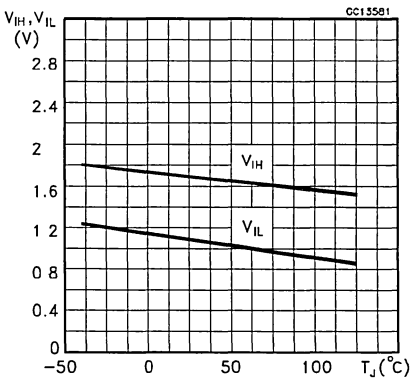
$R_{DS(on)}$ vs Supply Voltage



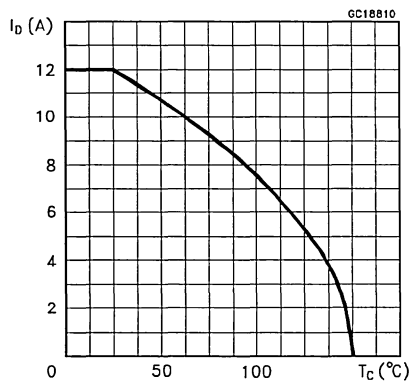
$R_{DS(on)}$ vs Output Current



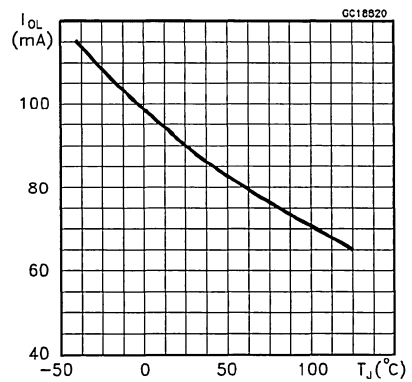
Input voltages vs Junction Temperature



Output Current Derating



Open Load vs Junction Temperature

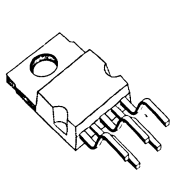


ISO HIGH SIDE SMART POWER SOLID STATE RELAY

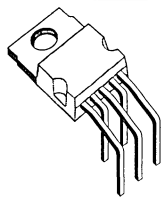
PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_n(*)	V_{CC}
VN06	60 V	0.18 Ω	1.9 A	26 V

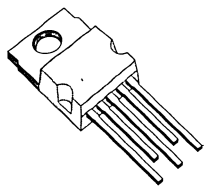
- MAXIMUM CONTINUOUS OUTPUT CURRENT (#): 8.5 A @ T_c= 85°C
- 5V LOGIC LEVEL COMPATIBLE INPUT
- THERMAL SHUT-DOWN
- UNDER VOLTAGE PROTECTION
- OPEN DRAIN DIAGNOSTIC OUTPUT
- INDUCTIVE LOAD FAST DEMAGNETIZATION
- VERY LOW STAND-BY POWER DISSIPATION



PENTAWATT (vertical)



PENTAWATT (horizontal)



PENTAWATT (in-line)

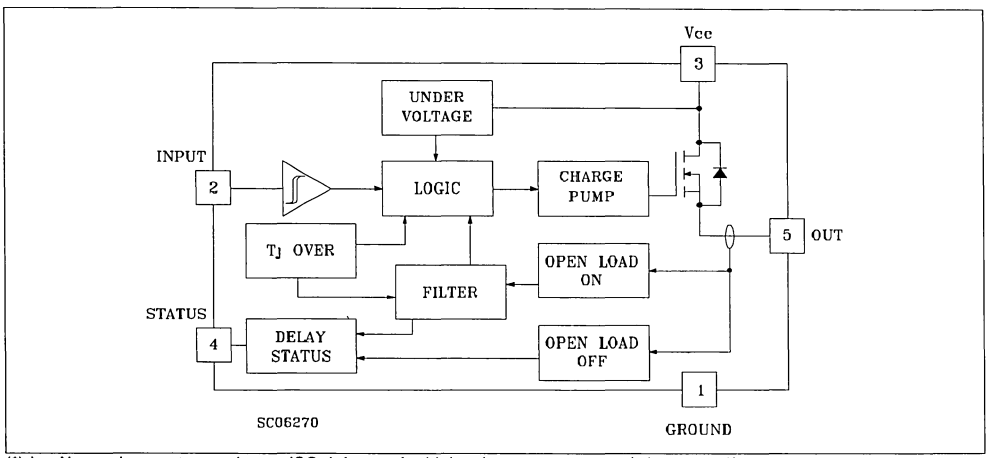
ORDER CODES:

PENTAWATT vertical	VN06
PENTAWATT horizontal	VN06 (011Y)
PENTAWATT in-line	VN06 (012Y)

DESCRIPTION

The VN06 is a monolithic device made using SGS-THOMSON Vertical Intelligent Power Technology, intended for driving resistive or inductive loads with one side grounded.
Built-in thermal shut-down protects the chip from over temperature and short circuit.
The open drain diagnostic output indicates: open load in off state and in on state, output shorted to V_{CC} and overtemperature. Fast demagnetization of inductive loads is archieved by negative (-18V) load voltage at turn-off.

BLOCK DIAGRAM

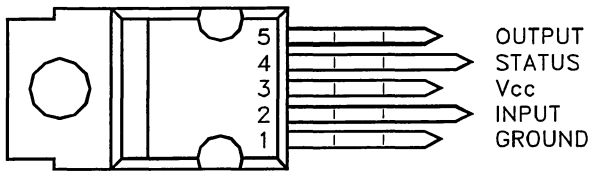


(*) In= Nominal current according to ISO definition for high side automotive switch (see note 1)
(#) The maximum continuous output current is the current at T_c = 85 °C for a battery voltage of 13 V which does not activate self protection

ABSOLUTE MAXIMUM RATING

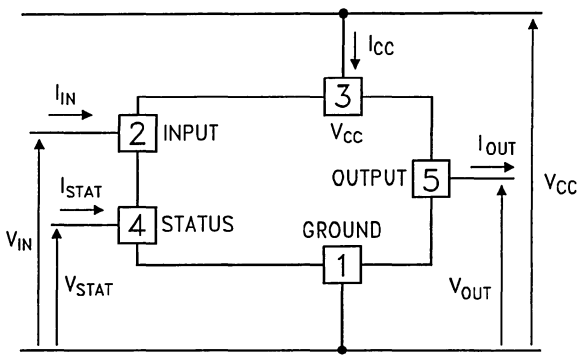
Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	V
I_{OUT}	Output Current (cont.) at T_c = 85 °C	8.5	A
I_R	Reverse Output Current at T_c = 85 °C	-8.5	A
I_{IN}	Input Current	±10	mA
$-V_{CC}$	Reverse Supply Voltage	-4	V
I_{STAT}	Status Current	±10	mA
V_{ESD}	Electrostatic Discharge (1.5 kΩ, 100 pF)	2000	V
P_{tot}	Power Dissipation at T_c = 85 °C	23	W
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

CONNECTION DIAGRAM



PC10000

CURRENT AND VOLTAGE CONVENTIONS



SC04660

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.4	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 13 V; -40 ≤ T_j ≤ 125 °C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		5.5	13	26	V
In(*)	Nominal Current	T_c = 85 °C $V_{DS(on)}$ ≤ 0.5 (note 1)	1.9			A
R_{on}	On State Resistance	I_{OUT} = 1.9 A I_{OUT} = 1.9 A T_j = 25 °C			0.36 0.18	Ω Ω
I_S	Supply Current	Off State T_j ≥ 25 °C On State			50 15	µA mA
$V_{DS(MAX)}$	Maximum Voltage Drop	I_{OUT} = 8.5 A T_c = 85 °C			2.75	V

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(^)	Turn-on Delay Time Of Output Current	I_{OUT} = 1.9 A Resistive Load Input Rise Time < 0.1 µs		20		µs
t_r(^)	Rise Time Of Output Current	I_{OUT} = 1.9 A Resistive Load Input Rise Time < 0.1 µs		20		µs
$t_{d(off)}$(^)	Turn-off Delay Time Of Output Current	I_{OUT} = 1.9 A Resistive Load Input Rise Time < 0.1 µs		25		µs
t_f(^)	Fall Time Of Output Current	I_{OUT} = 1.9 A Resistive Load Input Rise Time < 0.1 µs		6		µs
$(di/dt)_{on}$	Turn-on Current Slope	I_{OUT} = 1.9 A I_{OUT} = I_{ov}		0.08	0.5 1	A/µs A/µs
$(di/dt)_{off}$	Turn-off Current Slope	I_{OUT} = 1.9 A I_{OUT} = I_{ov}		0.2	3 3	A/µs A/µs
V_{demag}	Inductive Load Clamp Voltage	I_{OUT} = 1.9 A L = 1 mH	-24	-18	-14	V

LOGIC INPUT

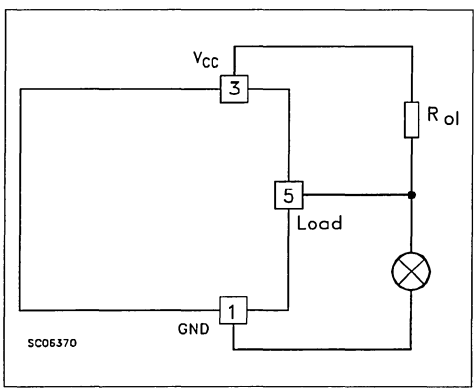
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2		(•)	V
$V_{I(hyst)}$	Input Hysteresis Voltage			0.5		V
I_{IN}	Input Current	V_{IN} = 5 V V_{IN} = 2 V V_{IN} = 0.8 V	 25	250	500 250	µA µA µA
V_{ICL}	Input Clamp Voltage	I_{IN} = 10 mA I_{IN} = -10 mA	5.5	6 -0.7	 -0.3	V V

ELECTRICAL CHARACTERISTICS (continued)
PROTECTION AND DIAGNOSTICS (continued)

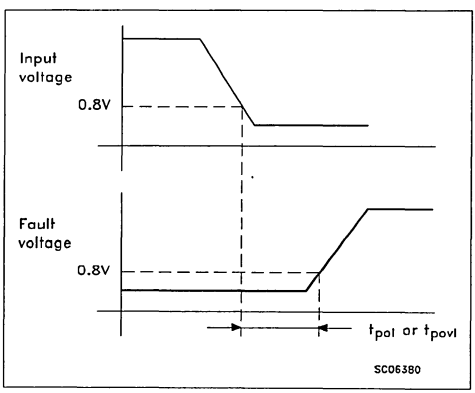
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status Voltage Output Low	I_{STAT} = 1.6 mA			0.4	V
V_{USD}	Under Voltage Shut Down			5		V
V_{SCL}	Status Clamp Voltage	I_{STAT} = 10 mA I_{STAT} = -10 mA		6 -0.7		V V
I_{OV}	Over Current	R_{LOAD} < 10 mΩ -40 ≤ T_c ≤ 125 °C			60	A
I_{AV}	Average Current in Short Circuit	R_{LOAD} < 10 mΩ T_c = 85 °C		1.4		A
I_{OL}	Open Load Current Level		5	80	180	mA
T_{TSD}	Thermal Shut-down Temperature		140			°C
T_R	Reset Temperature		125			°C
V_{OL}	Open Load Voltage Level	Off-State (note 2)	2.5	3.75	5	V
$t_{1(on)}$	Open Load Filtering Time	(note 3)	1	5	10	ms
$t_{1(off)}$	Open Load Filtering Time	(note 3)	1	5	10	ms
$t_{2(off)}$	Open Load Filtering Time	(note 3)	1	5	10	ms
t_{povl}	Status Delay	(note 3)		5	10	µs
t_{pol}	Status Delay	(note 3)	50	700		µs

(^) See Switchig Time Waveforms
(•) The V_{IH} is internally clamped at 6V about. It is possible to connect this pin to an higher voltage via an external resistor calculated to not exceed 10 mA at the input pin.
note 1: The Nominal Current is the current at T_c = 85 °C for battery voltage of 13V which produces a voltage drop of 0.5 V
note 2: $I_{OL(off)} = (V_{CC} - V_{OL})/R_{OL}$ (see figure)
note 3: $t_{1(on)}$: minimum open load duration which acctivates the status output
$t_{1(off)}$: minimum load recovery time which desactivates the status output
$t_{2(off)}$: minimum on time after thermal shut down which desactivates status output
t_{povl} t_{pol}: ISO definition (see figure)

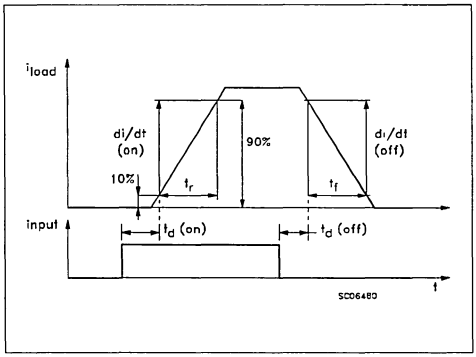
Note 2 Relevant Figure



Note 3 Relevant Figure



Switching Time Waveforms



FUNCTIONAL DESCRIPTION

The device has a diagnostic output which indicates open load conditions in off state as well as in on state, output shorted to V_{CC} and overtemperature. The truth table shows input, diagnostic and output voltage level in normal operation and in fault conditions. The output signals are processed by internal logic. The open load diagnostic output has a 5 ms filtering. The filter gives a continuous signal for the fault condition after an initial delay of about 5 ms. This means that a disconnection during normal operation, with a duration of less than 5 ms does not affect the status output. Equally, any re-connection of less than 5 ms during a disconnection duration does not affect the status output. No delay occur for the status to go low in case of overtemperature conditions. From the falling edge of the input signal the status output initially low in fault condition (over temperature or open load) will go back with a delay (t_{povl})in case of overtemperature condition and a delay (t_{pol}) in case of open load. These feature fully comply with International Standard Office (I.S.O.) requirement for automotive High Side Driver.

To protect the device against short circuit and over current conditions over the full range of supply voltage (V_{CC}) and temperature, the thermal protection turns the integrated Power MOS off at a minimum junction temperature of 140 °C. When the temperature returns to 125 °C the switch is automatically turned on again. In short circuit the protection reacts with virtually no delay, the sensor being located in the region of the die where the heat is generated. Driving inductive loads, an internal function of the device ensures the fast demagnetization with a typical voltage (V_{demag}) of -18V.

This function allows to greatly reduce the power dissipation according to the formula:

$P_{dem} = 0.5 \bullet L_{load} \bullet (I_{load})^2 \bullet [(V_{CC}+V_{demag})/V_{demag}] \bullet f$

where f = switching frequency and

V_{demag} = demagnetization voltage

Based on this formula it is possible to know the value of inductance and/or current to avoid a thermal shut-down. The maximum inductance which causes the chip temperature to reach the shut down temperature in a specific thermal environment, is infact a function of the load current for a fixed V_{CC}, V_{demag} and f.

PROTECTING THE DEVICE AGAIST LOAD DUMP - TEST PULSE 5

The device is able to withstand the test pulse No. 5 at level II (V_S = 46.5V) according to the ISO T/R 7637/1 without any external component. This means that all functions of the device are performed as designed after exposure to disturbance at level II. The VN06 is able to withstand the test pulse No.5 at level III adding an external resistor of 150 ohm between pin 1 and ground plus a filter capacitor of 1000 µF between pin 3 and ground (if $R_{LOAD} \leq 20\ \Omega$).

PROTECTING THE DEVICE AGAINST REVERSE BATTERY

The simplest way to protect the device against a continuous reverse battery voltage (-26V) is to insert a Schottky diode between pin 1(GND) and ground, as shown in the typical application circuit (fig.3).

The consequences of the voltage drop across this diode are as follows:

- If the input is pulled to power GND, a negative voltage of $-V_f$ is seen by the device. (Vil, Vih thresholds and Vstat are increased by Vf with respect to power GND).
- The undervoltage shutdown level is increased by Vf.

If there is no need for the control unit to handle external analog signals referred to the power GND, the best approach is to connect the reference potential of the control unit to node [1] (see application circuit in fig. 4), which becomes the common signal GND for the whole control board avoiding shift of V_{th}, V_{il} and V_{stat}. This solution allows the use of a standard diode.

TRUTH TABLE

	INPUT	OUTPUT	DIAGNOSTIC
Normal Operation	L H	L H	H H
Over-temperature	H	L	L
Under-voltage	X	L	H
Short load to V_{CC}	L	H	L

Figure 1: Waveforms

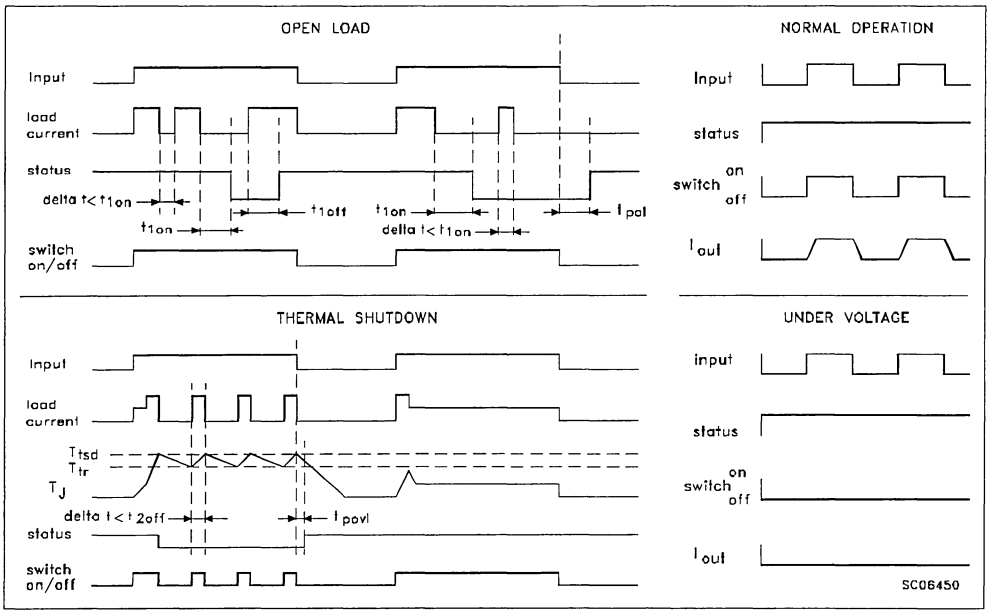


Figure 2: Over Current Test Circuit

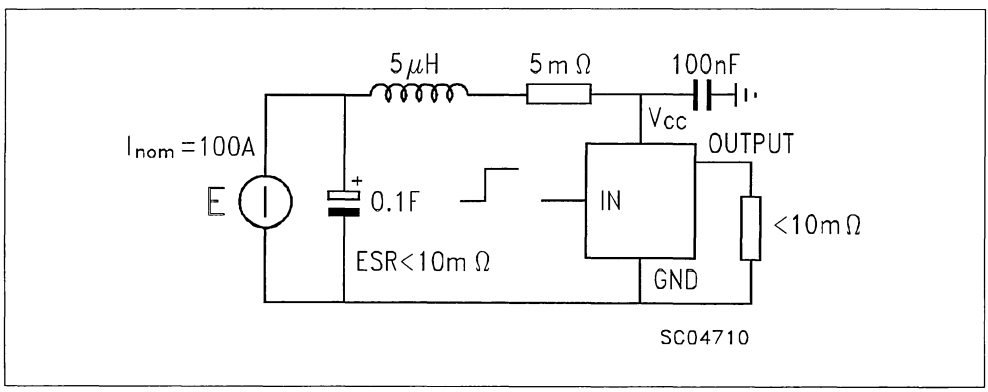


Figure 3: Typical Application Circuit With A Schottky Diode For Reverse Supply Protection

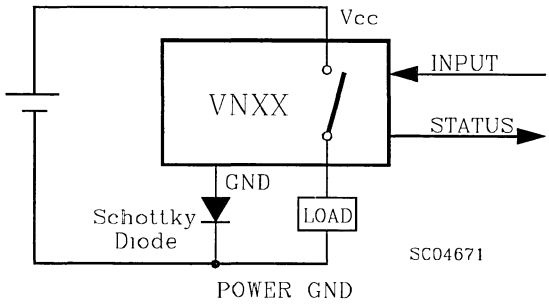
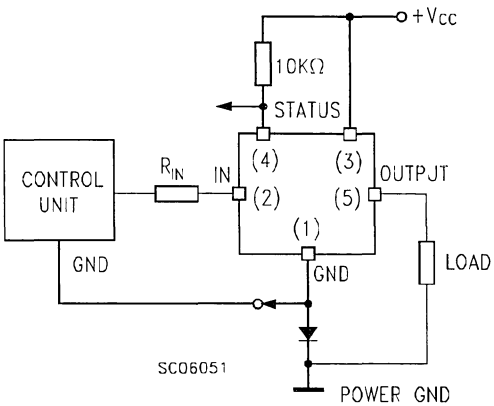
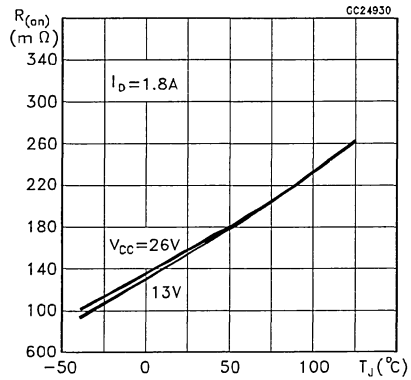


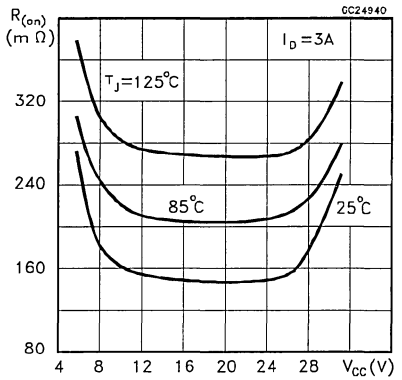
Figure 4: Typical Application Circuit With Separate Signal Ground



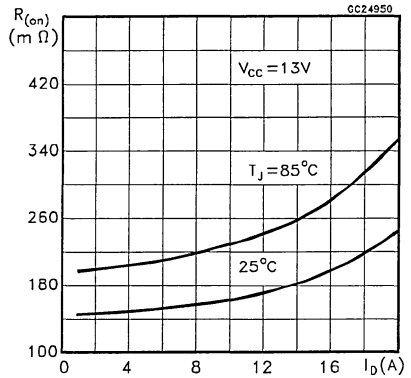
$R_{DS(on)}$ vs Junction Temperature



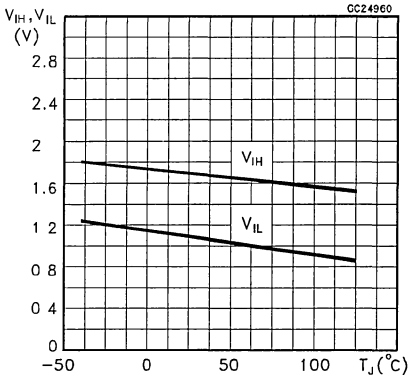
$R_{DS(on)}$ vs Supply Voltage



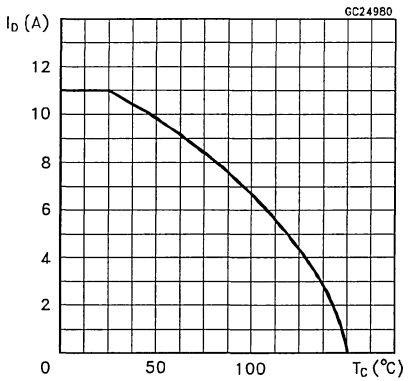
$R_{DS(on)}$ vs Output Current



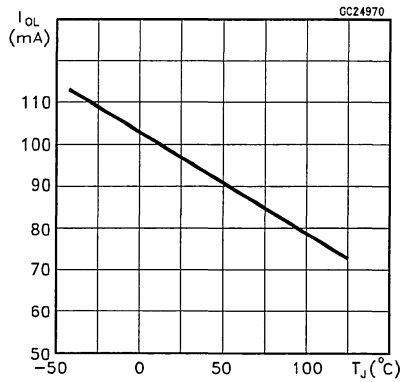
Input voltages vs Junction Temperature



Output Current Derating



Open Load vs Junction Temperature

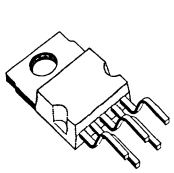


ISO HIGH SIDE SMART POWER SOLID STATE RELAY

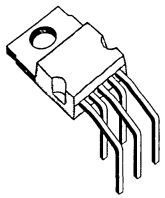
PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_n(*)	V_{CC}
VN16B	40 V	0.06 Ω	5.6 A	26 V

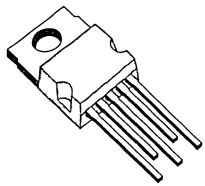
- MAXIMUM CONTINUOUS OUTPUT CURRENT (#): 20 A @ T_c= 85°C
- 5V LOGIC LEVEL COMPATIBLE INPUT
- THERMAL SHUT-DOWN
- UNDER VOLTAGE PROTECTION
- OPEN DRAIN DIAGNOSTIC OUTPUT
- INDUCTIVE LOAD FAST DEMAGNETIZATION
- VERY LOW STAND-BY POWER DISSIPATION



PENTAWATT (vertical)



PENTAWATT (horizontal)



PENTAWATT (in-line)

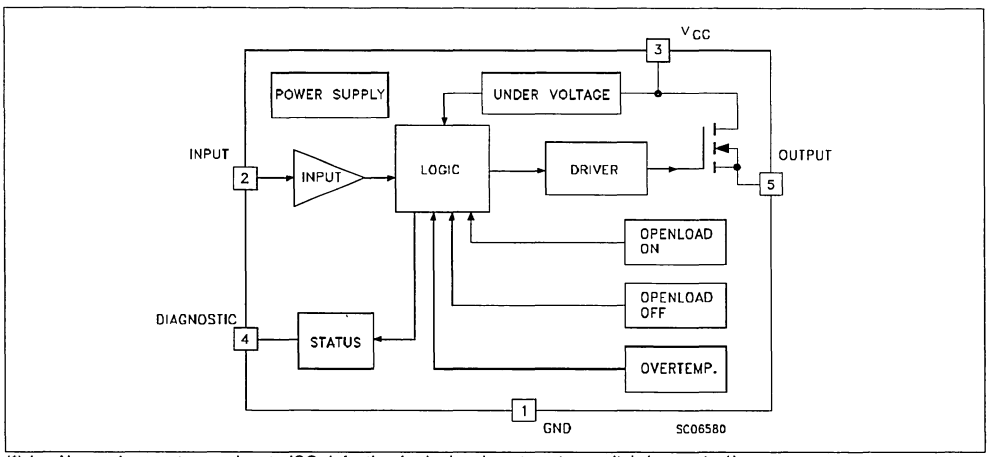
ORDER CODES:

PENTAWATT vertical	VN16B
PENTAWATT horizontal	VN16B (011Y)
PENTAWATT in-line	VN16B (012Y)

DESCRIPTION

The VN16B is a monolithic device made using SGS-THOMSON Vertical Intelligent Power Technology, intended for driving resistive or inductive loads with one side grounded.
Built-in thermal shut-down protects the chip from over temperature and short circuit.
The open drain diagnostic output indicates: open load in off state and in on state, output shorted to V_{CC} and overtemperature. Fast demagnetization of inductive loads is archieved by negative (-18V) load voltage at turn-off.

BLOCK DIAGRAM

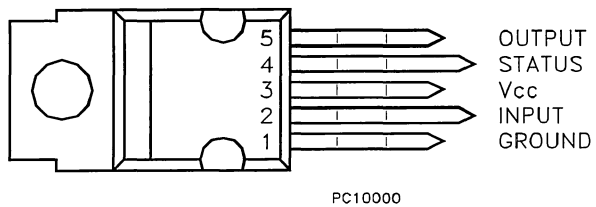


(*) In= Nominal current according to ISO definition for high side automotive switch (see note 1)
(#) The maximum continuous output current is the current at T_c = 85 °C for a battery voltage of 13 V which does not activate self protection

ABSOLUTE MAXIMUM RATING

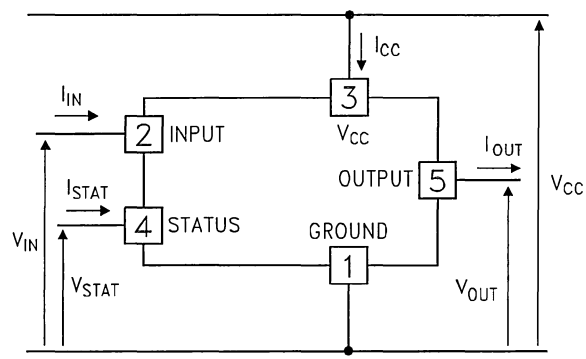
Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	40	V
I_{OUT}	Output Current (cont.) at T_c = 85 °C	20	A
$I_{OUT}(RMS)$	RMS Output Current at T_c = 85 °C	20	A
I_R	Reverse Output Current at T_c = 85 °C (f > 1Hz)	-20	A
I_{IN}	Input Current	±10	mA
$-V_{CC}$	Reverse Supply Voltage	-4	V
I_{STAT}	Status Current	±10	mA
V_{ESD}	Electrostatic Discharge (1.5 kΩ, 100 pF)	2000	V
P_{tot}	Power Dissipation at T_c = 25 °C	82	W
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

CONNECTION DIAGRAM



PC10000

CURRENT AND VOLTAGE CONVENTIONS



SC04660

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.4	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

ELECTRICAL CHARACTERISTICS ($8 < V_{CC} < 16$ V; $-40 \le T_j \le 125$ °C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		6	13	26	V
In(*)	Nominal Current	T_c = 85 °C $V_{DS(on)} \le 0.5$ V_{CC} = 13 V	5.6		8.8	A
R_{on}	On State Resistance	I_{OUT} = In V_{CC} = 13 V T_j = 25 °C	0.038		0.06	Ω
I_S	Supply Current	Off State V_{CC} = 13 V $T_j \ge$ 25 °C		25	50	µA
$V_{DS(MAX)}$	Maximum Voltage Drop	I_{OUT} = 20 A V_{CC} = 13 V T_c = 85 °C	1		1.8	V
R_i	Output to GND Internal Impedance	T_j = 25 °C	5	10	20	KΩ

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(^)	Turn-on Delay Time Of Output Current	R_{load} = 1.6 Ω	5	50	500	µs
t_r(^)	Rise Time Of Output Current	R_{load} = 1.6 Ω	40	100	680	µs
$t_{d(off)}$(^)	Turn-off Delay Time Of Output Current	R_{load} = 1.6 Ω	10	100	500	µs
t_f(^)	Fall Time Of Output Current	R_{load} = 1.6 Ω	40	100	680	µs
$(di/dt)_{on}$	Turn-on Current Slope	R_{load} = 1.6 Ω V_{CC} = 13 V	0.008		0.1	A/µs
$(di/dt)_{off}$	Turn-off Current Slope	R_{load} = 1.6 Ω V_{CC} = 13 V	0.008		0.1	A/µs
V_{demag}	Inductive Load Clamp Voltage	R_{load} = 1.6 Ω L = 1 mH	-24	-18	-14	V

LOGIC INPUT

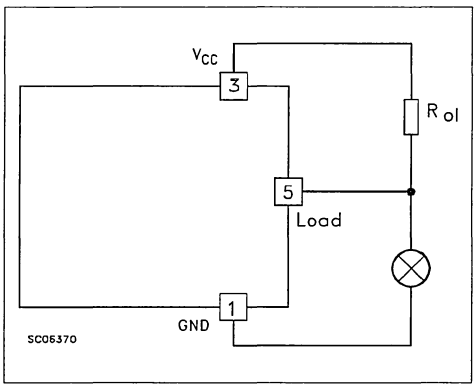
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				1.5	V
V_{IH}	Input High Level Voltage		3.5		(•)	V
$V_{I(hyst)}$	Input Hysteresis Voltage		0.2	1	1.5	V
I_{IN}	Input Current	V_{IN} = 5 V T_j = 25 °C			100	µA
V_{ICL}	Input Clamp Voltage	I_{IN} = 10 mA I_{IN} = -10 mA	5	6 -0.7	7	V V

ELECTRICAL CHARACTERISTICS (continued)
PROTECTION AND DIAGNOSTICS (continued)

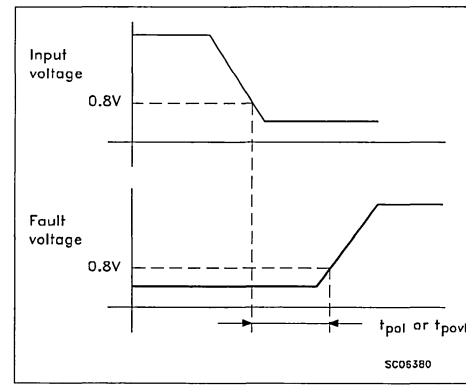
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status Voltage Output Low	I_{STAT} = 1.6 mA			0.4	V
V_{USD}	Under Voltage Shut Down		3.5	5	6	V
V_{SCL}	Status Clamp Voltage	I_{STAT} = 10 mA I_{STAT} = -10 mA	5	6 -0.7	7	V V
T_{TSD}	Thermal Shut-down Temperature		140	160	180	°C
$T_{SD(hyst)}$	Thermal Shut-down Hysteresis			15	50	°C
T_R	Reset Temperature		125			°C
V_{OL}	Open Voltage Level	Off-State (note 2)	2.5	3.8	5	V
I_{OL}	Open Load Current Level	On-State	0.15		0.85	A
t_{povl}	Status Delay	(note 3)		5	10	µs
t_{pol}	Status Delay	(note 3)	50	400	2500	µs

(*) In= Nominal current according to ISO definition for high side automotive switch (see note 1)
(^) See Switchig Time Waveforms
(•) The V_{IH} is internally clamped at 6V about. It is possible to connect this pin to an higher voltage via an external resistor calculated to not exceed 10 mA at the input pin.
note 1: The Nominal Current is the current at T_c = 85 °C for battery voltage of 13V which produces a voltage drop of 0.5 V
note 2: $I_{OL(off)} = (V_{CC} - V_{OL})/R_{OL}$ (see figure)
note 3: t_{povl} t_{pol}: ISO definition (see figure)

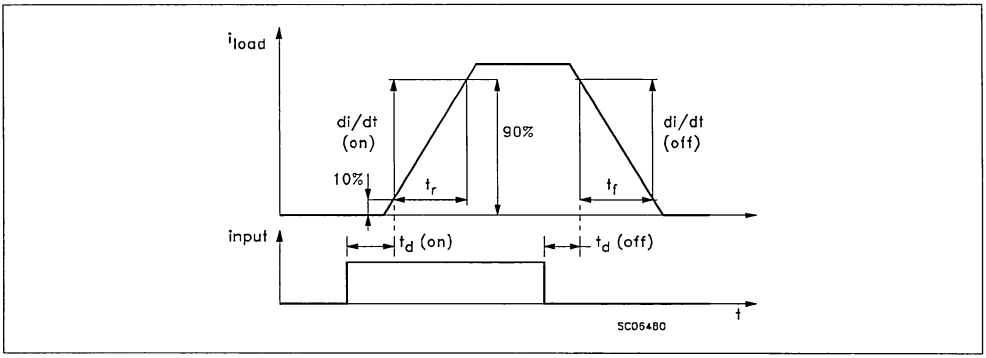
Note 2 Relevant Figure



Note 3 Relevant Figure



Switching Time Waveforms



FUNCTIONAL DESCRIPTION

The device has a diagnostic output which indicates open load in on-state, open load in off-state, over temperature conditions and stuck-on to V_{CC}.

From the falling edge of the input signal, the status output, initially low to signal a fault condition (overtemperature or open load on-state), will go back to a high state with a different delay in case of overtemperature (tpovl) and in case of open open load (tpol) respectively. This feature allows to discriminate the nature of the detected fault. To protect the device against short circuit and over current condition over the full range of supply voltage (V_{CC}) and temperature, the thermal protection turns the integrated Power MOS off at a minimum junction temperature of 140 °C. When this temperature returns to 125 °C the switch is automatically turned on again. In short circuit the protection reacts with virtually no delay, the sensor being located inside the Power MOS area. An internal function of the devices ensures the fast demagnetization of inductive loads with a typical voltage (V_{demag}) of -18V. This function allows to greatly reduces the power dissipation according to the formula:

$P_{dem} = 0.5 \bullet L_{load} \bullet (I_{load})^2 \bullet [(V_{CC}+V_{demag})/V_{demag}] \bullet f$

where f = switching frequency and
V_{demag} = demagnetization voltage.

The maximum inductance which causes the chip temperature to reach the shut-down temperature in a specified thermal environment is a function of the load current for a fixed V_{CC}, V_{demag} and f according to the above formula. In this device if the GND pin is disconnected, with V_{CC} not exceeding 16V, it will switch off.

PROTECTING THE DEVICE AGAINST REVERSE BATTERY

The simplest way to protect the device against a continuous reverse battery voltage (-26V) is to insert a Schottky diode between pin 1 (GND) and ground, as shown in the typical application circuit (fig.3).

The consequences of the voltage drop across this diode are as follows:

- If the input is pulled to power GND, a negative voltage of $-V_f$ is seen by the device. (Vil, Vih thresholds and Vstat are increased by Vf with respect to power GND).
- The undervoltage shutdown level is increased by Vf.

If there is no need for the control unit to handle external analog signals referred to the power GND, the best approach is to connect the reference potential of the control unit to node [1] (see application circuit in fig. 3), which becomes the common signal GND for the whole control board avoiding shift of V_{ih}, V_{il} and V_{stat}. This solution allows the use of a standard diode.

TRUTH TABLE

	INPUT	OUTPUT	DIAGNOSTIC
Normal Operation	L H	L H	H H
Over-temperature	X	L	L
Under-voltage	X	L	H
Short load to V_{CC}	H L	H H	L L
Open Load	H L	H L	L L (#)

(#) With an additional external resistor

Figure 1: Waveforms

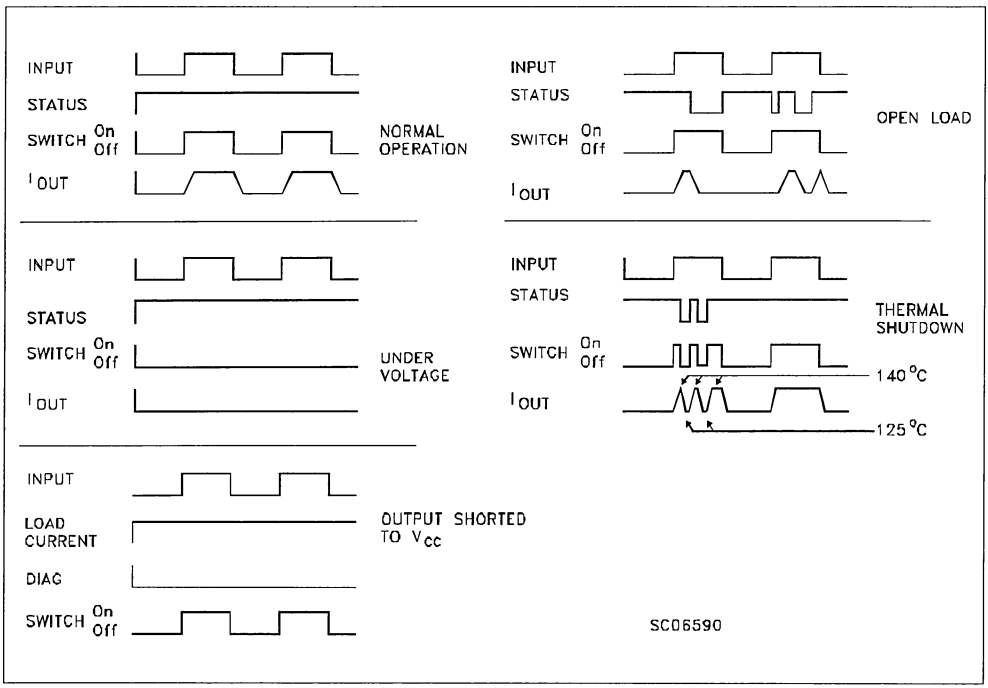


Figure 2: Over Current Test Circuit

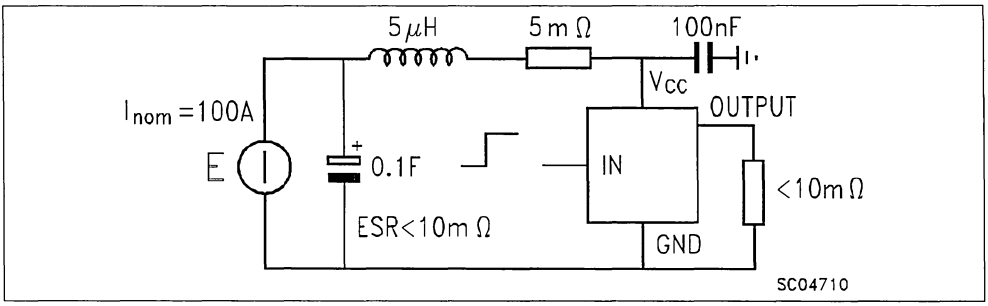


Figure 3: Typical Application Circuit With A Schottky Diode For Reverse Supply Protection

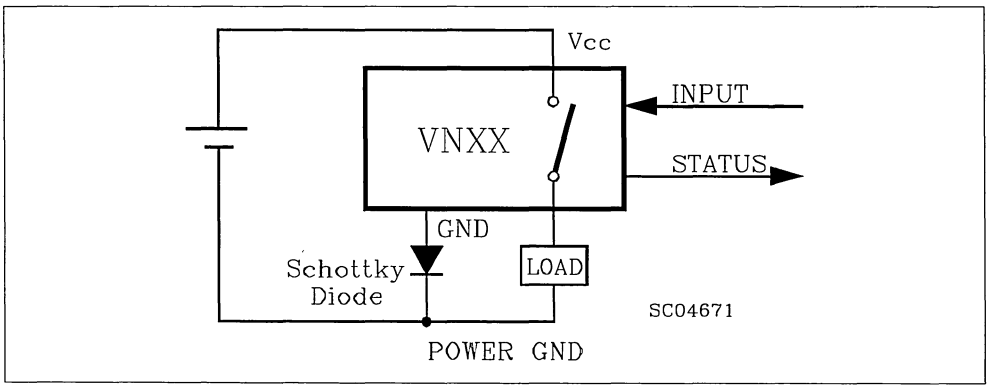
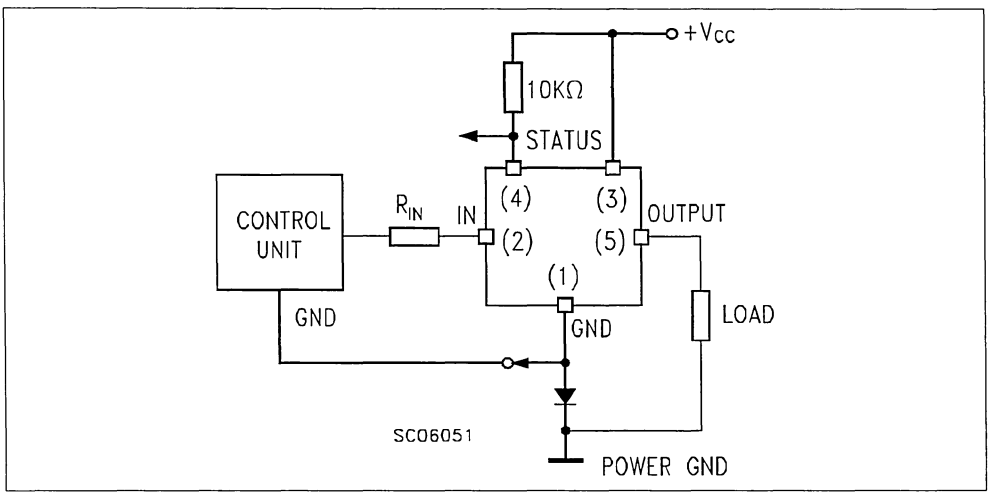


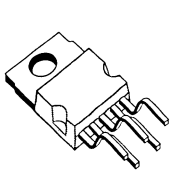
Figure 4: Typical Application Circuit With Separate Signal Ground



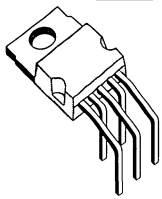
HIGH SIDE SMART POWER SOLID STATE RELAY

TYPE	V_{DSS}	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN20N	60 V	0.05 Ω	28 A	26 V

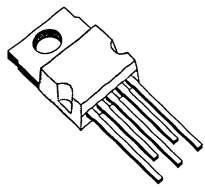
- OUTPUT CURRENT (CONTINUOUS): 28A @ T_c=25°C
- 5V LOGIC LEVEL COMPATIBLE INPUT
- THERMAL SHUT-DOWN
- UNDER VOLTAGE SHUT-DOWN
- OPEN DRAIN DIAGNOSTIC OUTPUT
- VERY LOW STAND-BY POWER DISSIPATION



PENTAWATT (vertical)



PENTAWATT (horizontal)



PENTAWATT (in-line)

ORDER CODES:

PENTAWATT vertical	VN20N
PENTAWATT horizontal	VN20N (011Y)
PENTAWATT in-line	VN20N (012Y)

DESCRIPTION

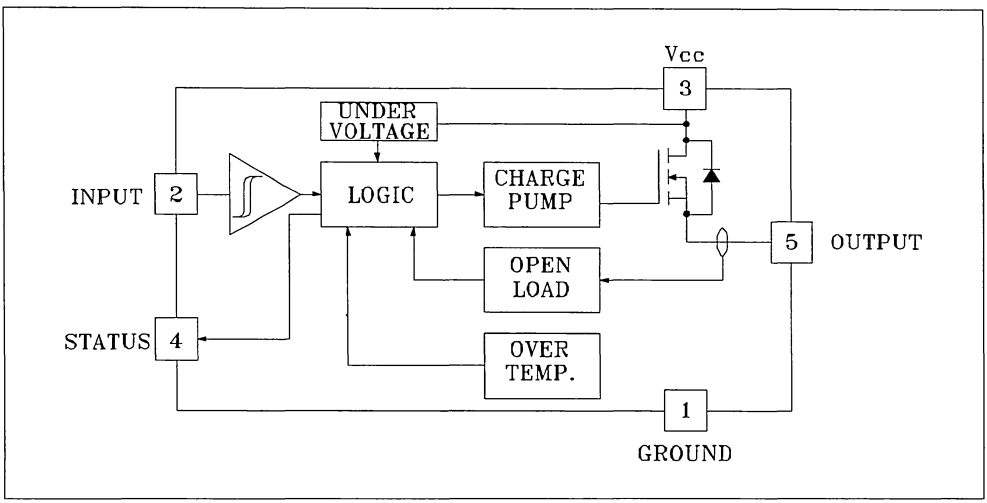
The VN20N is a monolithic device made using SGS-THOMSON Vertical Intelligent Power Technology, intended for driving resistive or inductive loads with one side grounded.

Built-in thermal shut-down protects the chip from over temperature and short circuit.

The input control is 5V logic level compatible.

The open drain diagnostic output indicates open circuit (no load) and over temperature status.

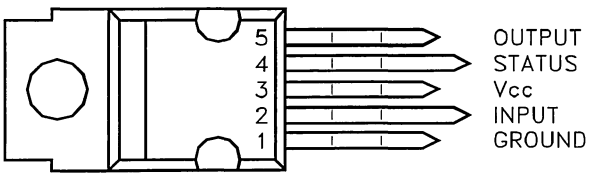
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

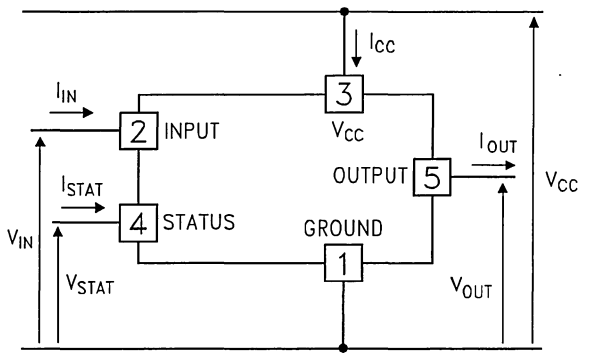
Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	V
I_{OUT}	Output Current (cont.)	28	A
I_R	Reverse Output Current	-28	A
I_{IN}	Input Current	±10	mA
$-V_{CC}$	Reverse Supply Voltage	-4	V
I_{STAT}	Status Current	±10	mA
V_{ESD}	Electrostatic Discharge (1.5 kΩ, 100 pF)	2000	V
P_{tot}	Power Dissipation at $T_c \leq 25$ °C	80	W
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

CONNECTION DIAGRAM



PC10000

CURRENT AND VOLTAGE CONVENTIONS



SC04660

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.56	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 13 V; -40 ≤ T_j ≤ 125 °C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		7		26	V
R_{on}	On State Resistance	I_{OUT} = 14 A I_{OUT} = 14 A T_j = 25 °C			0.1 0.05	Ω Ω
I_S	Supply Current	Off State T_j ≥ 25 °C On State			50 15	µA mA

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time Of Output Current	I_{OUT} = 14 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		30		µs
t_r	Rise Time Of Output Current	I_{OUT} = 14 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		70		µs
$t_{d(off)}$	Turn-off Delay Time Of Output Current	I_{OUT} = 14 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		40		µs
t_f	Fall Time Of Output Current	I_{OUT} = 14 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		30		µs
$(di/dt)_{on}$	Turn-on Current Slope	I_{OUT} = 14 A I_{OUT} = Iov			0.5 2	A/µs A/µs
$(di/dt)_{off}$	Turn-off Current Slope	I_{OUT} = 14 A I_{OUT} = Iov			2 4	A/µs A/µs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2		(*)	V
$V_{I(hyst.)}$	Input Hysteresis Voltage			0.5		V
I_{IN}	Input Current	V_{IN} = 5 V		250	500	µA
V_{ICL}	Input Clamp Voltage	I_{IN} = 10 mA I_{IN} = -10 mA		6 -0.7		V V

PROTECTIONS AND DIAGNOSTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{STAT} (•)	Status Voltage Output Low	I_{STAT} = 1.6 mA			0.4	V
V_{USD}	Under Voltage Shut Down			6.5		V

ELECTRICAL CHARACTERISTICS (continued)
PROTECTION AND DIAGNOSTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SCL} (•)	Status Clamp Voltage	I_{STAT} = 10 mA I_{STAT} = -10 mA		6 -0.7		V V
t_{SC}	Switch-off Time in Short Circuit Condition at Start-Up	R_{LOAD} < 10 mΩ T_c = 25 °C		2	5	ms
I_{OV}	Over Current	R_{LOAD} < 10 mΩ -40 ≤ T_c ≤ 125 °C			140	A
I_{AV}	Average Current in Short Circuit	R_{LOAD} < 10 mΩ T_c = 85 °C		2.5		A
I_{OL}	Open Load Current Level		5		700	mA
T_{TSD}	Thermal Shut-down Temperature		140			°C
T_R	Reset Temperature		125			°C

(*) The V_{IH} is internally clamped at 6V about. It is possible to connect this pin to an higher voltage via an external resistor calculated to not exceed 10 mA at the input pin.
(•) Status determination > 100 µs after the switching edge.

FUNCTIONAL DESCRIPTION

The device has a diagnostic output which indicates open circuit (no load) and over temperature conditions. The output signals are processed by internal logic.

To protect the device against short circuit and over-current condition over the full range of supply voltage (V_{CC}) and temperature, the thermal protection turns the integrated Power MOS off at a minimum junction temperature of 140 °C. When the temperature returns to about 125 °C the switch is automatically turned on again.

In short circuit conditions the protection reacts with virtually no delay, the sensor being located in the region of the die where the heat is generated.

PROTECTING THE DEVICE AGAINST REVERSE BATTERY

The simplest way to protect the device against a continuous reverse battery voltage (-26V) is to insert a Schottky diode between pin 1 (GND) and ground, as shown in the typical application circuit (fig. 3).

The consequences of the voltage drop across this diode are as follows:

- If the input is pulled to power GND, a negative voltage of $-V_F$ is seen by the device. (V_{IL}, V_{IH} thresholds and V_{STAT} are increased by V_F with respect to power GND).
- The undervoltage shutdown level is increased by V_F.

If there is no need for the control unit to handle external analog signals referred to the power GND, the best approach is to connect the reference potential of the control unit to node [1] (see application circuit in fig. 4), which becomes the common signal GND for the whole control board.

In this way no shift of V_{IH}, V_{IL} and V_{STAT} takes place and no negative voltage appears on the INPUT pin; this solution allows the use of a standard diode, with a breakdown voltage able to handle any ISO normalized negative pulses that occours in the automotive environment.

TRUTH TABLE

	INPUT	OUTPUT	DIAGNOSTIC
Normal Operation	L H	L H	H H
Open Circuit (No Load)	H	H	L
Over-temperature	H	L	L
Under-voltage	X	L	H

Figure 1: Waveforms

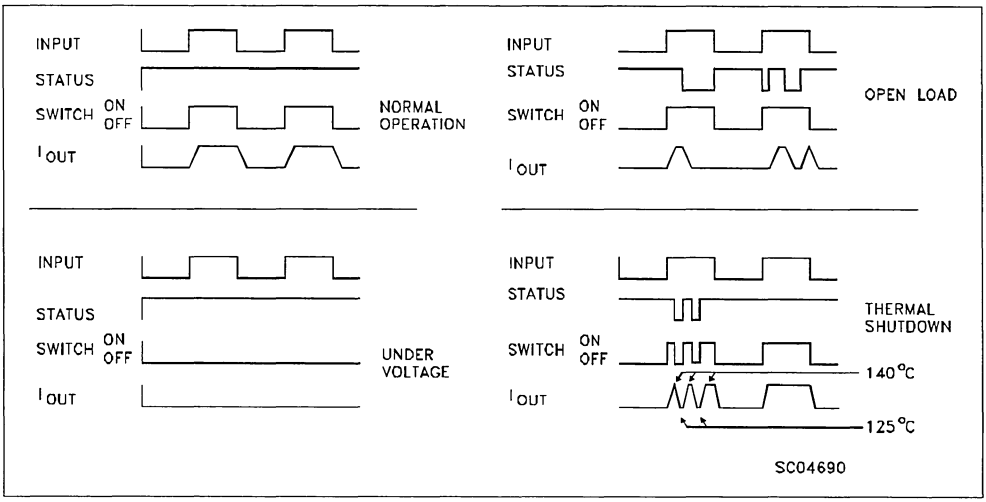


Figure 2: Over Current Test Circuit

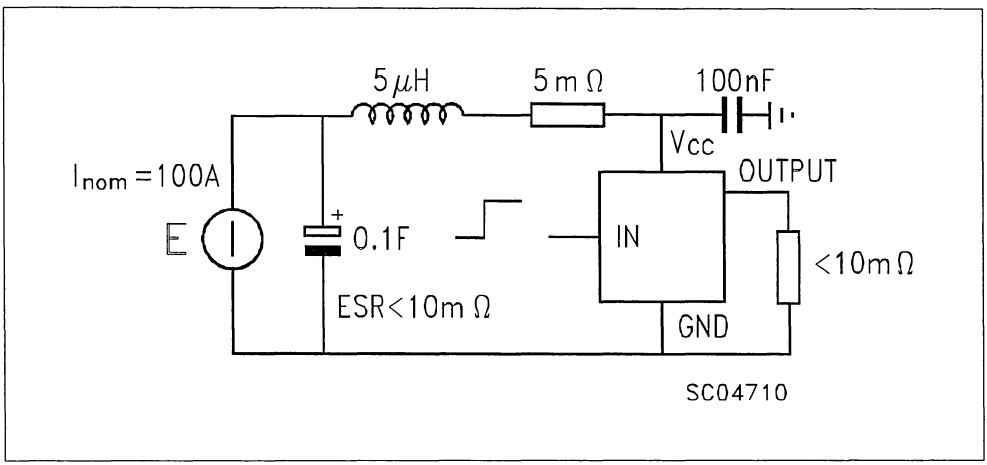


Figure 3: Typical Application Circuit With A Schottky Diode For Reverse Supply Protection

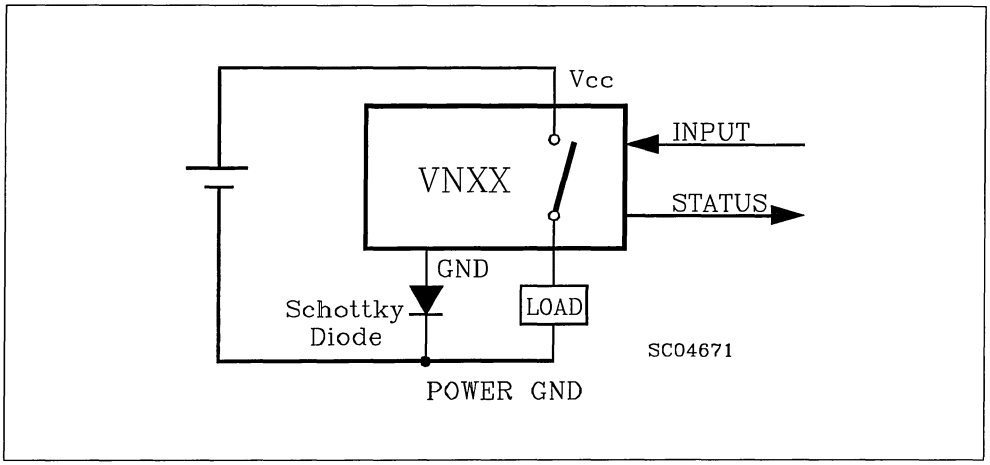
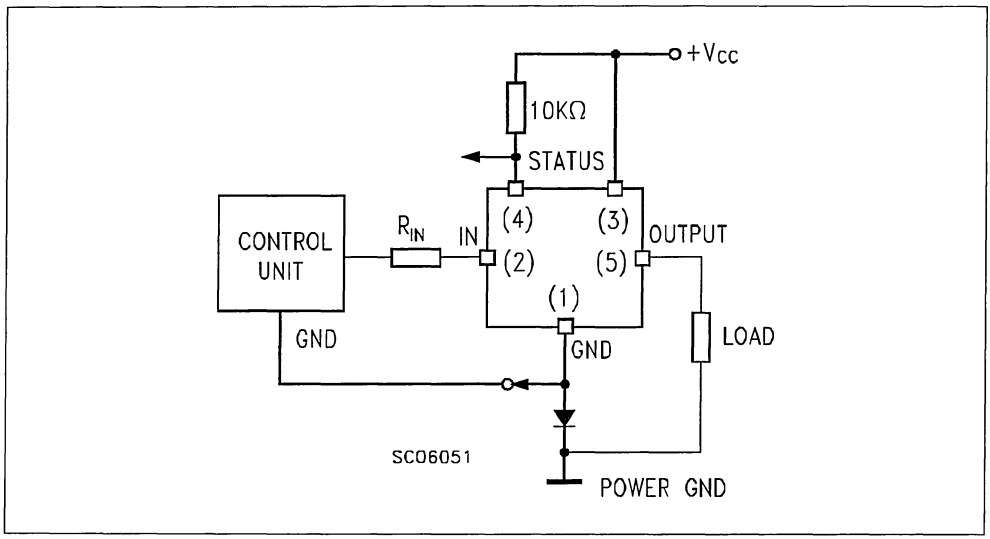
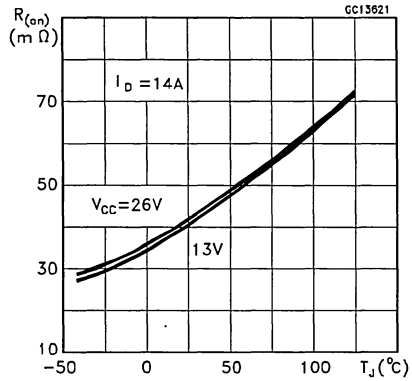


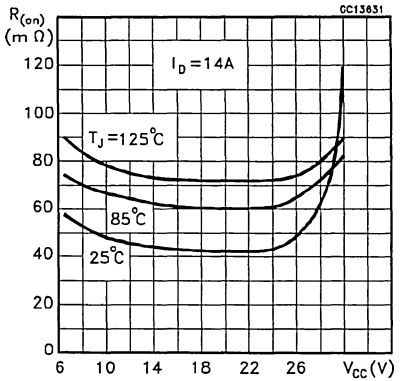
Figure 4: Typical Application Circuit With Separate Signal Ground



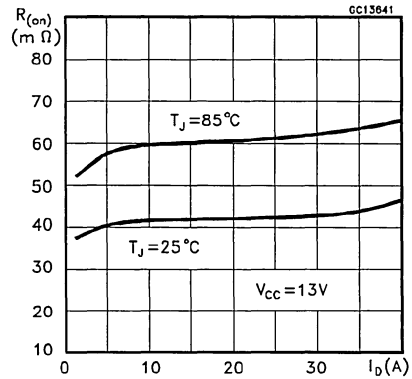
$R_{DS(on)}$ vs Junction Temperature



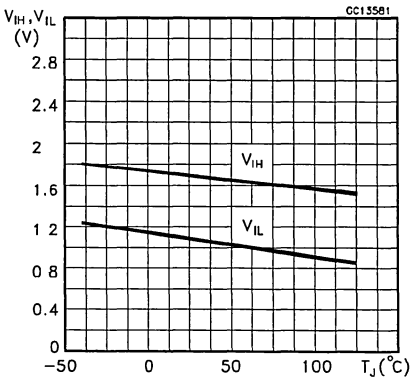
$R_{DS(on)}$ vs Supply Voltage



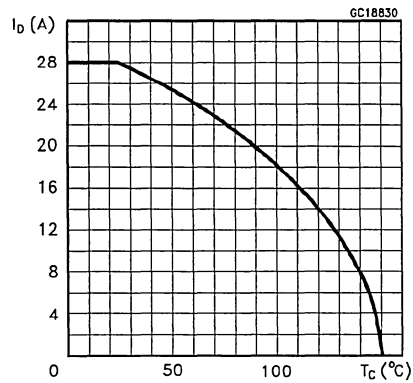
$R_{DS(on)}$ vs Output Current



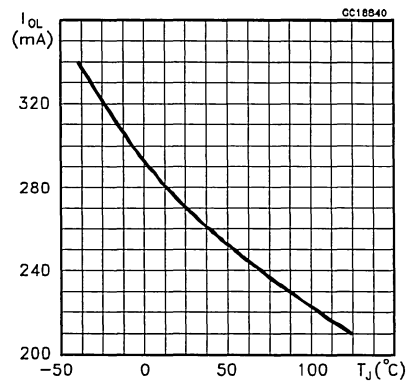
Input voltages vs Junction Temperature



Output Current Derating



Open Load vs Junction Temperature

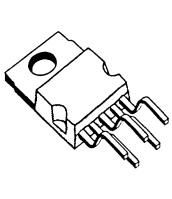


ISO HIGH SIDE SMART POWER SOLID STATE RELAY

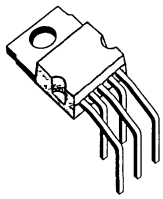
PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_n(*)	V_{CC}
VN21	60 V	0.05 Ω	7 A	26 V

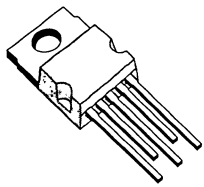
- MAXIMUM CONTINUOUS OUTPUT CURRENT (#): 20 A @ T_c= 85°C
- 5V LOGIC LEVEL COMPATIBLE INPUT
- THERMAL SHUT-DOWN
- UNDER VOLTAGE PROTECTION
- OPEN DRAIN DIAGNOSTIC OUTPUT
- INDUCTIVE LOAD FAST DEMAGNETIZATION
- VERY LOW STAND-BY POWER DISSIPATION



PENTAWATT (vertical)



PENTAWATT (horizontal)



PENTAWATT (in-line)

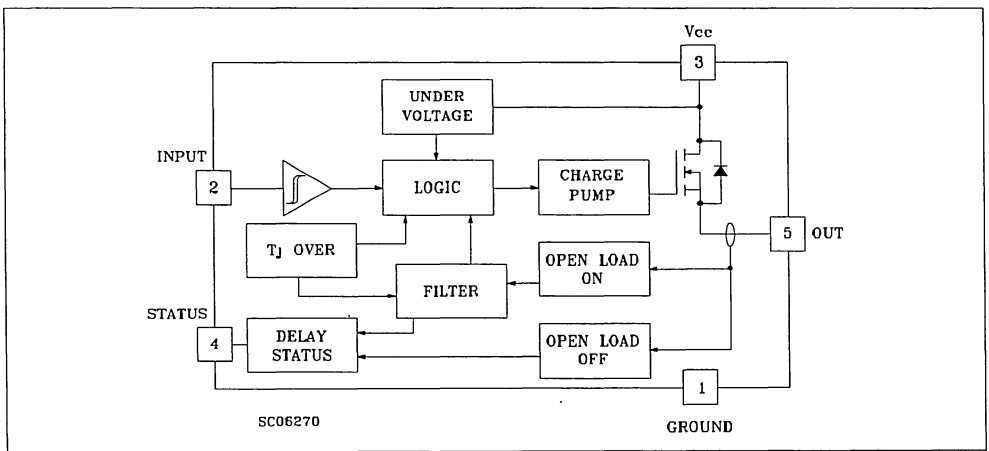
ORDER CODES:

PENTAWATT vertical	VN21
PENTAWATT horizontal	VN21 (011Y)
PENTAWATT in-line	VN21 (012Y)

DESCRIPTION

The VN21 is a monolithic device made using SGS-THOMSON Vertical Intelligent Power Technology, intended for driving resistive or inductive loads with one side grounded.
Built-in thermal shut-down protects the chip from over temperature and short circuit.
The open drain diagnostic output indicates: open load in off state and in on state, output shorted to V_{CC} and overtemperature. Fast demagnetization of inductive loads is archieved by negative (-18V) load voltage at turn-off.

BLOCK DIAGRAM

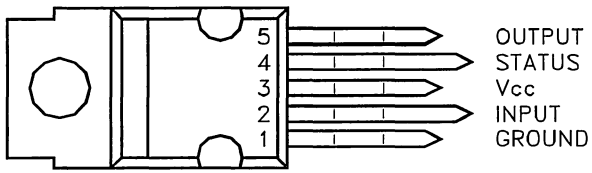


(*) In= Nominal current according to ISO definition for high side automotive switch (see note 1)
(#) The maximum continuous output current is the current at T_c = 85 °C for a battery voltage of 13 V which does not activate self protection

ABSOLUTE MAXIMUM RATING

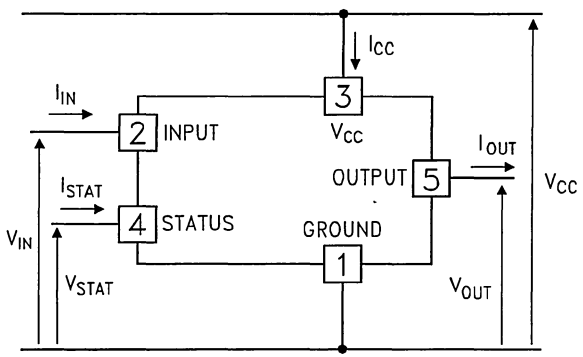
Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	V
I_{OUT}	Output Current (cont.) at T_c = 85 °C	20	A
I_R	Reverse Output Current at T_c = 85 °C	-20	A
I_{IN}	Input Current	±10	mA
$-V_{CC}$	Reverse Supply Voltage	-4	V
I_{STAT}	Status Current	±10	mA
V_{ESD}	Electrostatic Discharge (1.5 kΩ, 100 pF)	2000	V
P_{tot}	Power Dissipation at T_c = 85 °C	36	W
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

CONNECTION DIAGRAM



PC10000

CURRENT AND VOLTAGE CONVENTIONS



SC04660

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.5	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 13 V; -40 ≤ T_j ≤ 125 °C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		5.5	13	26	V
In(*)	Nominal Current	T_c = 85 °C $V_{DS(on)}$ ≤ 0.5 (note 1)	7			A
R_{on}	On State Resistance	I_{OUT} = 7 A I_{OUT} = 7 A T_j = 25 °C			0.10 0.05	Ω Ω
I_S	Supply Current	Off State T_j ≥ 25 °C On State			50 15	µA mA
$V_{DS(MAX)}$	Maximum Voltage Drop	I_{OUT} = 20 A T_c = 85 °C			1.8	V

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(^)	Turn-on Delay Time Of Output Current	I_{OUT} = 7 A Resistive Load Input Rise Time < 0.1 µs		60		µs
t_r(^)	Rise Time Of Output Current	I_{OUT} = 7 A Resistive Load Input Rise Time < 0.1 µs		70		µs
$t_{d(off)}$(^)	Turn-off Delay Time Of Output Current	I_{OUT} = 7 A Resistive Load Input Rise Time < 0.1 µs		90		µs
t_f(^)	Fall Time Of Output Current	I_{OUT} = 7 A Resistive Load Input Rise Time < 0.1 µs		25		µs
$(di/dt)_{on}$	Turn-on Current Slope	I_{OUT} = 7 A I_{OUT} = I_{ov}		0.08	0.5 1	A/µs A/µs
$(di/dt)_{off}$	Turn-off Current Slope	I_{OUT} = 7 A I_{OUT} = I_{ov}		0.2	3 3	A/µs A/µs
V_{demag}	Inductive Load Clamp Voltage	I_{OUT} = 7 A L = 1 mH	-24	-18	-14	V

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2		(•)	V
$V_{I(hyst)}$	Input Hysteresis Voltage			0.5		V
I_{IN}	Input Current	V_{IN} = 5 V V_{IN} = 2 V V_{IN} = 0.8 V	 25	250	500 250	µA µA µA
V_{ICL}	Input Clamp Voltage	I_{IN} = 10 mA I_{IN} = -10 mA	5.5	6 -0.7	 -0.3	V V

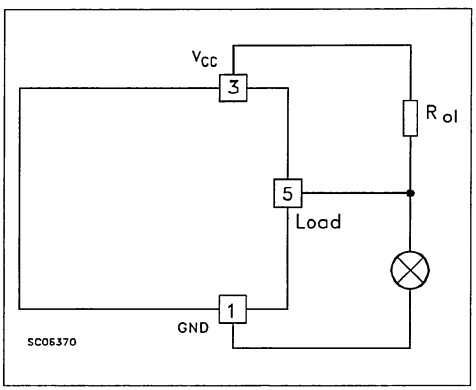
ELECTRICAL CHARACTERISTICS (continued)

PROTECTION AND DIAGNOSTICS (continued)

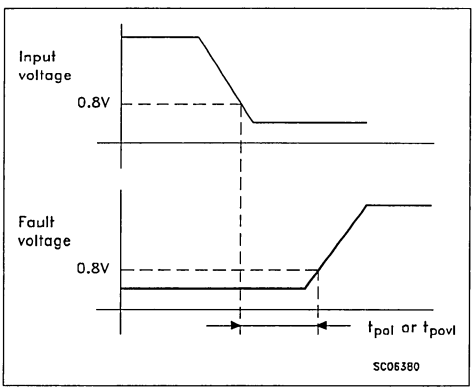
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status Voltage Output Low	I_{STAT} = 1.6 mA			0.4	V
V_{USD}	Under Voltage Shut Down			5		V
V_{SCL}	Status Clamp Voltage	I_{STAT} = 10 mA I_{STAT} = -10 mA		6 -0.7		V V
I_{OV}	Over Current	R_{LOAD} < 10 mΩ -40 ≤ T_c ≤ 125 °C			140	A
I_{AV}	Average Current in Short Circuit	R_{LOAD} < 10 mΩ T_c = 85 °C		2.5		A
I_{OL}	Open Load Current Level		5	300	700	mA
T_{TSD}	Thermal Shut-down Temperature		140			°C
T_R	Reset Temperature		125			°C
V_{OL}	Open Load Voltage Level	Off-State (note 2)	2.5	3.75	5	V
$t_{1(on)}$	Open Load Filtering Time	(note 3)	1	5	10	ms
$t_{1(off)}$	Open Load Filtering Time	(note 3)	1	5	10	ms
$t_{2(off)}$	Open Load Filtering Time	(note 3)	1	5	10	ms
t_{povl}	Status Delay	(note 3)		5	10	µs
t_{pol}	Status Delay	(note 3)	50	700		µs

(^) See Switchig Time Waveforms
(•) The V_{IH} is internally clamped at 6V about. It is possible to connect this pin to an higher voltage via an external resistor calculated to not exceed 10 mA at the input pin.
note 1: The Nominal Current is the current at T_c = 85 °C for battery voltage of 13V which produces a voltage drop of 0.5 V
note 2: $I_{OL(off)} = (V_{CC} - V_{OL})/R_{OL}$ (see figure)
note 3: $t_{1(on)}$: minimum open load duration which acctivates the status output
$t_{1(off)}$: minimum load recovery time which desactivates the status output
$t_{2(off)}$: minimum on time after thermal shut down which desactivates status output
t_{povl} t_{pol}: ISO definition (see figure)

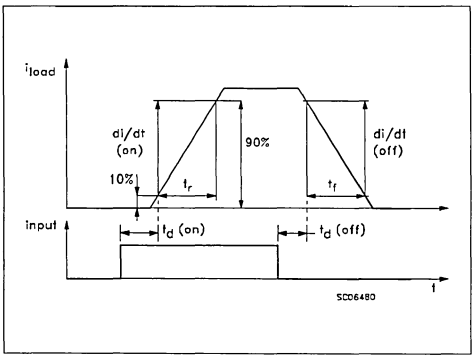
Note 2 Relevant Figure



Note 3 Relevant Figure



Switching Time Waveforms



FUNCTIONAL DESCRIPTION

The device has a diagnostic output which indicates open load conditions in off state as well as in on state, output shorted to V_{CC} and overtemperature. The truth table shows input, diagnostic and output voltage level in normal operation and in fault conditions. The output signals are processed by internal logic. The open load diagnostic output has a 5 ms filtering. The filter gives a continuous signal for the fault condition after an initial delay of about 5 ms. This means that a disconnection during normal operation, with a duration of less than 5 ms does not affect the status output. Equally, any re-connection of less than 5 ms during a disconnection duration does not affect the status output. No delay occur for the status to go low in case of overtemperature conditions. From the falling edge of the input signal the status output initially low in fault condition (over temperature or open load) will go back with a delay (t_{povl})in case of overtemperature condition and a delay (t_{pol}) in case of open load. These feature fully comply with International Standard Office (I.S.O.) requirement for automotive High Side Driver.

To protect the device against short circuit and over current conditions over the full range of supply voltage (V_{CC}) and temperature, the thermal protection turns the integrated Power MOS off at a minimum junction temperature of 140 °C. When the temperature returns to 125 °C the switch is automatically turned on again. In short circuit the protection reacts with virtually no delay, the sensor being located in the region of the die where the heat is generated. Driving inductive loads, an internal function of the device ensures the fast demagnetization with a typical voltage (V_{demag}) of -18V.

This function allows to greatly reduce the power dissipation according to the formula:

$P_{dem} = 0.5 \bullet L_{load} \bullet (I_{load})^2 \bullet [(V_{CC}+V_{demag})/V_{demag}] \bullet f$

where f = switching frequency and

V_{demag} = demagnetization voltage

Based on this formula it is possible to know the value of inductance and/or current to avoid a thermal shut-down. The maximum inductance which causes the chip temperature to reach the shut down temperature in a specific thermal environment, is infact a function of the load current for a fixed V_{CC}, V_{demag} and f.

PROTECTING THE DEVICE AGAIST LOAD DUMP - TEST PULSE 5

The device is able to withstand the test pulse No. 5 at level II (V_S = 46.5V) according to the ISO T/R 7637/1 without any external component. This means that all functions of the device are performed as designed after exposure to disturbance at level II. The VN21 is able to withstand the test pulse No.5 at level III adding an external resistor of 150 ohm between pin 1 and ground plus a filter capacitor of 1000 µF between pin 3 and ground (if $R_{LOAD} \leq 20\ \Omega$).

PROTECTING THE DEVICE AGAINST REVERSE BATTERY

The simplest way to protect the device against a continuous reverse battery voltage (-26V) is to insert a Schottky diode between pin 1(GND) and ground, as shown in the typical application circuit (fig.3).

The consequences of the voltage drop across this diode are as follows:

- If the input is pulled to power GND, a negative voltage of $-V_f$ is seen by the device. (Vil, Vih thresholds and Vstat are increased by Vf with respect to power GND).
- The undervoltage shutdown level is increased by Vf.

If there is no need for the control unit to handle external analog signals referred to the power GND, the best approach is to connect the reference potential of the control unit to node [1] (see application circuit in fig. 4), which becomes the common signal GND for the whole control board avoiding shift of V_{ih}, V_{il} and V_{stat}. This solution allows the use of a standard diode.

TRUTH TABLE

	INPUT	OUTPUT	DIAGNOSTIC
Normal Operation	L H	L H	H H
Over-temperature	H	L	L
Under-voltage	X	L	H
Short load to Vcc	L	H	L

Figure 1: Waveforms

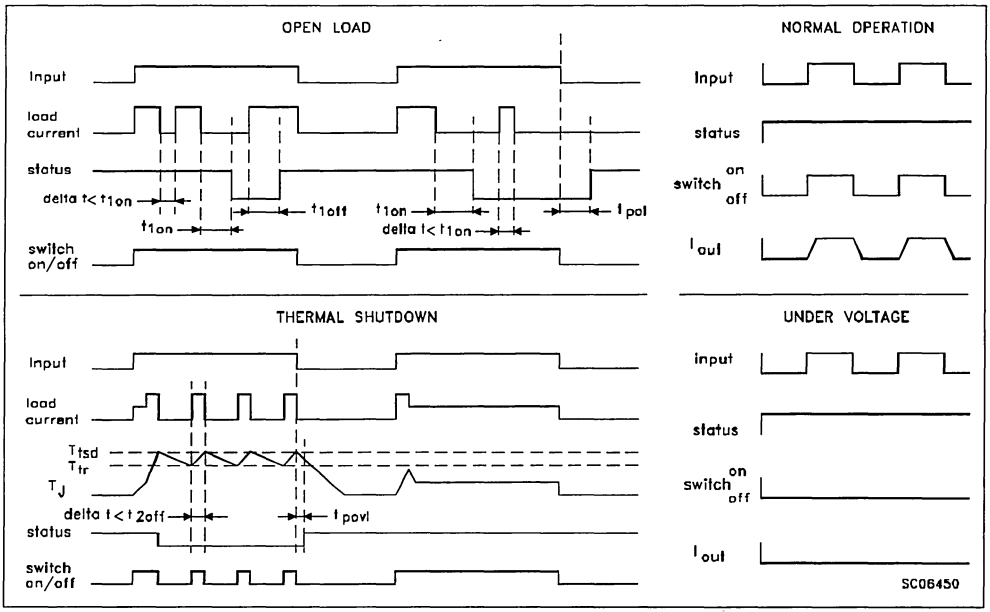


Figure 2: Over Current Test Circuit

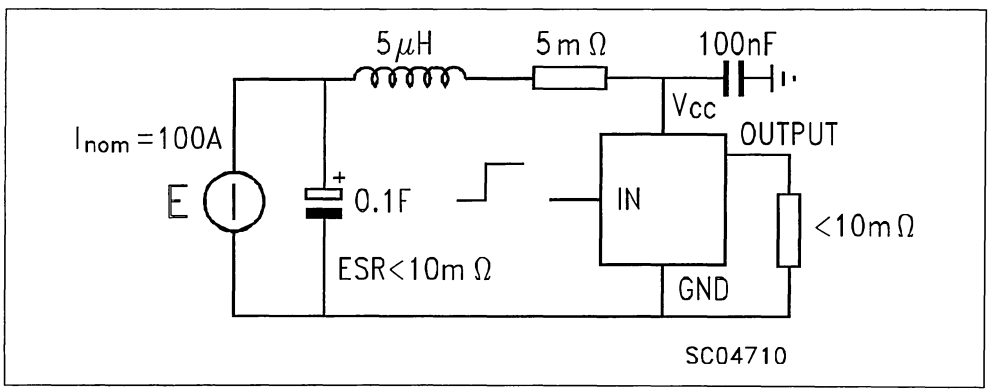


Figure 3: Typical Application Circuit With A Schottky Diode For Reverse Supply Protection

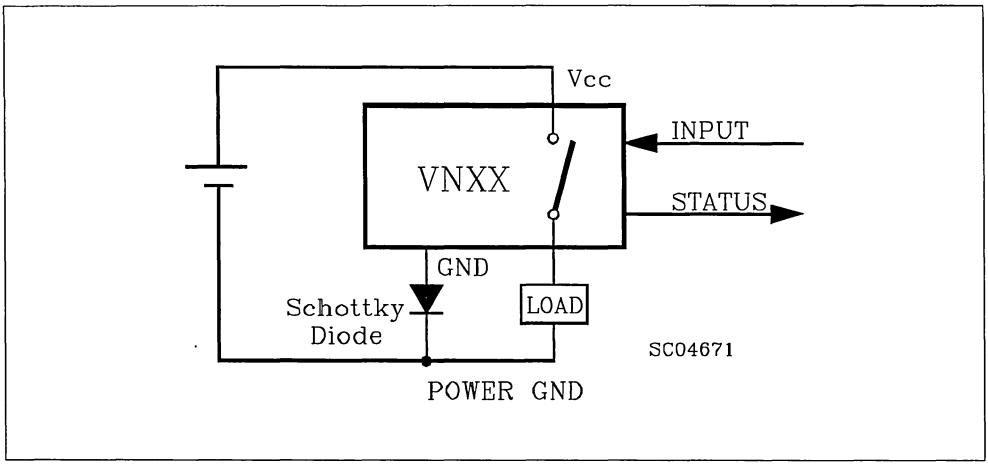
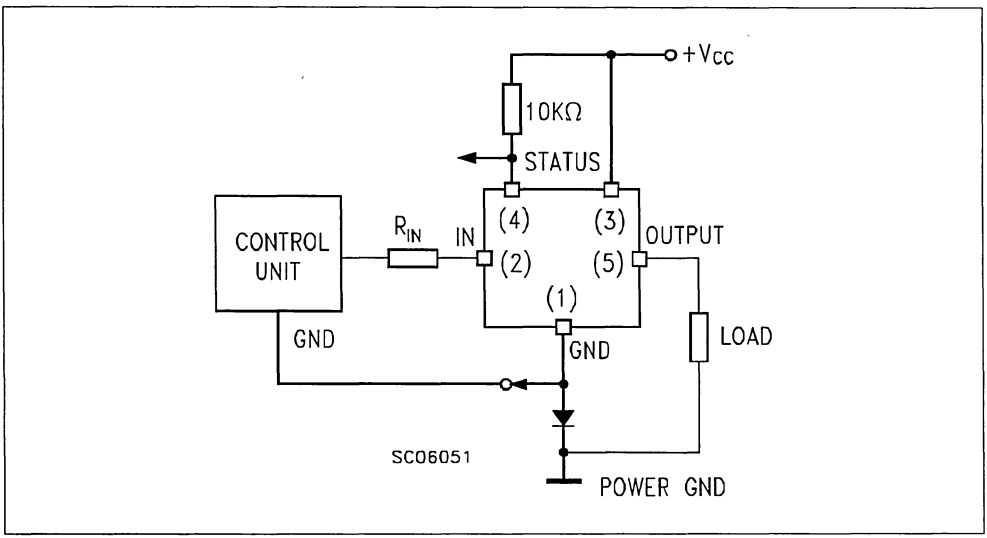


Figure 4: Typical Application Circuit With Separate Signal Ground

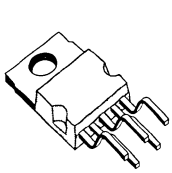


HIGH SIDE SMART POWER SOLID STATE RELAY

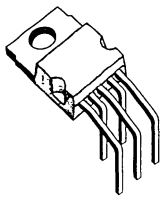
PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN30N	60 V	0.03 Ω	36 A	26 V

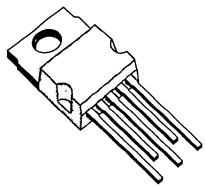
- OUTPUT CURRENT (CONTINUOUS): 36A @ T_C=25°C
- 5V LOGIC LEVEL COMPATIBLE INPUT
- THERMAL SHUT-DOWN
- UNDER VOLTAGE SHUT-DOWN
- OPEN DRAIN DIAGNOSTIC OUTPUT
- VERY LOW STAND-BY POWER DISSIPATION



PENTAWATT (vertical)



PENTAWATT (horizontal)



PENTAWATT (in-line)

ORDER CODES:

PENTAWATT vertical	VN30N
PENTAWATT horizontal	VN30N (011Y)
PENTAWATT in-line	VN30N (012Y)

DESCRIPTION

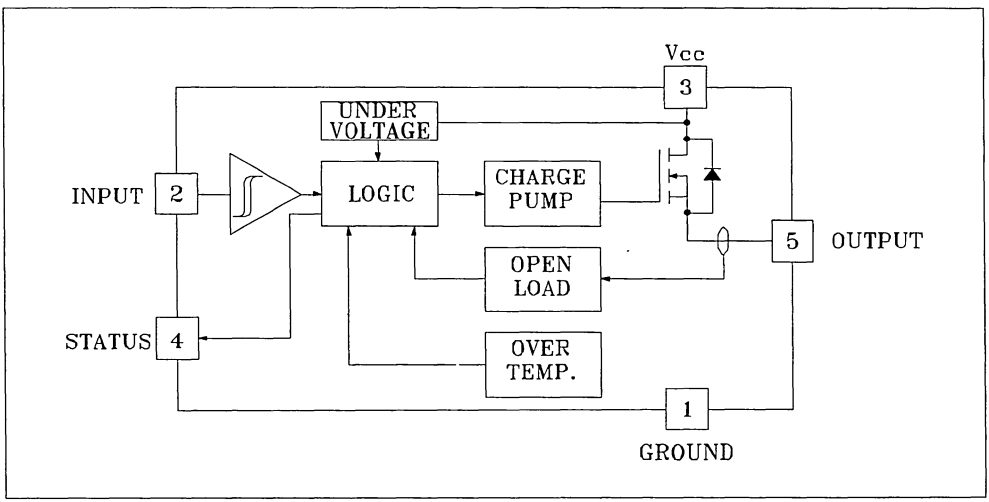
The VN30N is a monolithic device made using SGS-THOMSON Vertical Intelligent Power Technology, intended for driving resistive or inductive loads with one side grounded.

Built-in thermal shut-down protects the chip from over temperature and short circuit.

The input control is 5V logic level compatible.

The open drain diagnostic output indicates open circuit (no load) and over temperature status.

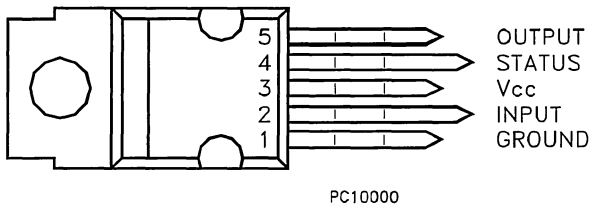
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

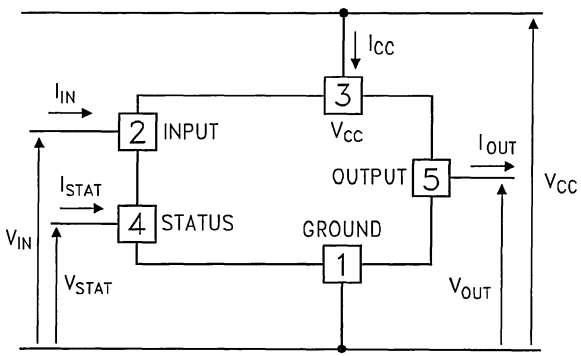
Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	V
I_{OUT}	Output Current (cont.)	36	A
I_R	Reverse Output Current	-36	A
I_{IN}	Input Current	±10	mA
$-V_{CC}$	Reverse Supply Voltage	-4	V
I_{STAT}	Status Current	±10	mA
V_{ESD}	Electrostatic Discharge (1.5 kΩ, 100 pF)	2000	V
P_{tot}	Power Dissipation at $T_c \leq 25$ °C	74	W
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

CONNECTION DIAGRAM



PC10000

CURRENT AND VOLTAGE CONVENTIONS



SC04660

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.56	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 13 V; -40 ≤ T_j ≤ 125 °C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		7		26	V
R_{on}	On State Resistance	I_{OUT} = 18 A I_{OUT} = 18 A T_j = 25 °C			0.06 0.03	Ω Ω
I_S	Supply Current	Off State T_j ≥ 25 °C On State			50 15	µA mA

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time Of Output Current	I_{OUT} = 18 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		30		µs
t_r	Rise Time Of Output Current	I_{OUT} = 18 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		100		µs
$t_{d(off)}$	Turn-off Delay Time Of Output Current	I_{OUT} = 18 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		80		µs
t_f	Fall Time Of Output Current	I_{OUT} = 18 A Resistive Load Input Rise Time < 0.1 µs T_j = 25 °C		40		µs
$(di/dt)_{on}$	Turn-on Current Slope	I_{OUT} = 18 A I_{OUT} = I_{ov}			0.5 3	A/µs A/µs
$(di/dt)_{off}$	Turn-off Current Slope	I_{OUT} = 18 A I_{OUT} = I_{ov}			3 4	A/µs A/µs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2		(*)	V
$V_{I(hyst)}$	Input Hysteresis Voltage			0.5		V
I_{IN}	Input Current	V_{IN} = 5 V		250	500	µA
V_{ICL}	Input Clamp Voltage	I_{IN} = 10 mA I_{IN} = -10 mA		6 -0.7		V V

PROTECTIONS AND DIAGNOSTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{STAT} (•)	Status Voltage Output Low	I_{STAT} = 1.6 mA			0.4	V
V_{USD}	Under Voltage Shut Down			6.5	7	V

ELECTRICAL CHARACTERISTICS (continued)
PROTECTION AND DIAGNOSTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SCL} (•)	Status Clamp Voltage	I_{STAT} = 10 mA I_{STAT} = -10 mA		6 -0.7		V V
t_{SC}	Switch-off Time in Short Circuit Condition at Start-Up	R_{LOAD} < 10 mΩ T_c = 25 °C		1		ms
I_{OV}	Over Current	R_{LOAD} < 10 mΩ -40 ≤ T_c ≤ 125 °C		140		A
I_{AV}	Average Current in Short Circuit	R_{LOAD} < 10 mΩ T_c = 85 °C		2.5		A
I_{OL}	Open Load Current Level		5		1250	mA
T_{TSD}	Thermal Shut-down Temperature		140			°C
T_R	Reset Temperature		125			°C

(*) The V_{IH} is internally clamped at 6V about. It is possible to connect this pin to an higher voltage via an external resistor calculated to not exceed 10 mA at the input pin.
(•) Status determination > 100 µs after the switching edge

FUNCTIONAL DESCRIPTION

The device has a diagnostic output which indicates open circuit (no load) and over temperature conditions. The output signals are processed by internal logic.

To protect the device against short circuit and over-current condition over the full range of supply voltage (V_{CC}) and temperature, the thermal protection turns the integrated Power MOS off at a minimum junction temperature of 140 °C. When the temperature returns to about 125 °C the switch is automatically turned on again.

In short circuit conditions the protection reacts with virtually no delay, the sensor being located in the region of the die where the heat is generated.

PROTECTING THE DEVICE AGAINST REVERSE BATTERY

The simplest way to protect the device against a continuous reverse battery voltage (-26V) is to insert a Schottky diode between pin 1 (GND) and ground, as shown in the typical application circuit (fig. 3).

The consequences of the voltage drop across this diode are as follows:

- If the input is pulled to power GND, a negative voltage of $-V_F$ is seen by the device. (V_{IL}, V_{IH} thresholds and V_{STAT} are increased by V_F with respect to power GND).
- The undervoltage shutdown level is increased by V_F.

If there is no need for the control unit to handle external analog signals referred to the power GND, the best approach is to connect the reference potential of the control unit to node [1] (see application circuit in fig. 4), which becomes the common signal GND for the whole control board.

In this way no shift of V_{IH}, V_{IL} and V_{STAT} takes place and no negative voltage appears on the INPUT pin; this solution allows the use of a standard diode, with a breakdown voltage able to handle any ISO normalized negative pulses that occours in the automotive environment.

TRUTH TABLE

	INPUT	OUTPUT	DIAGNOSTIC
Normal Operation	L H	L H	H H
Open Circuit (No Load)	H	H	L
Over-temperature	H	L	L
Under-voltage	X	L	H

Figure 1: Waveforms

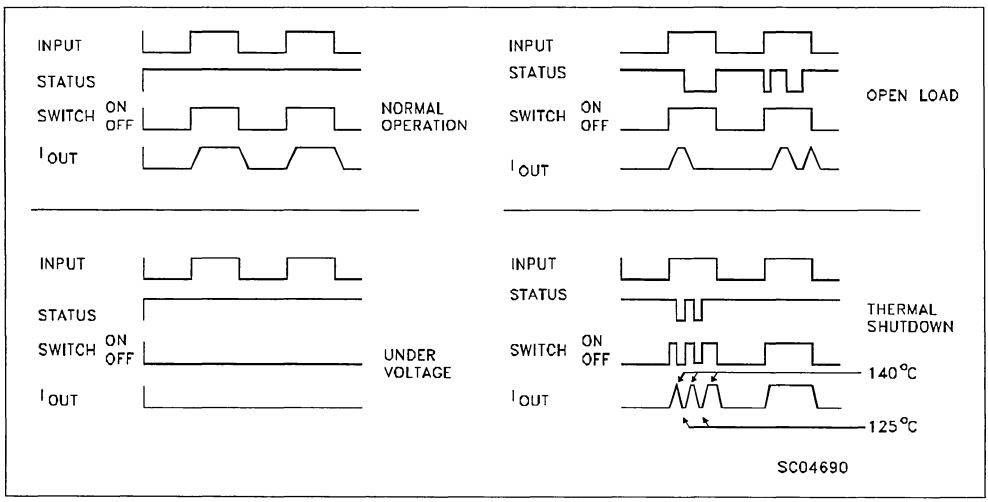


Figure 2: Over Current Test Circuit

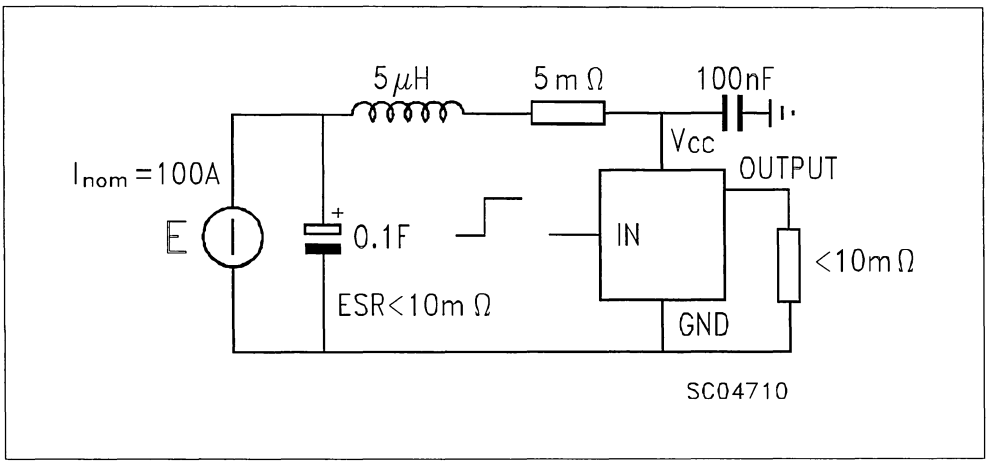


Figure 3: Typical Application Circuit With A Schottky Diode For Reverse Supply Protection

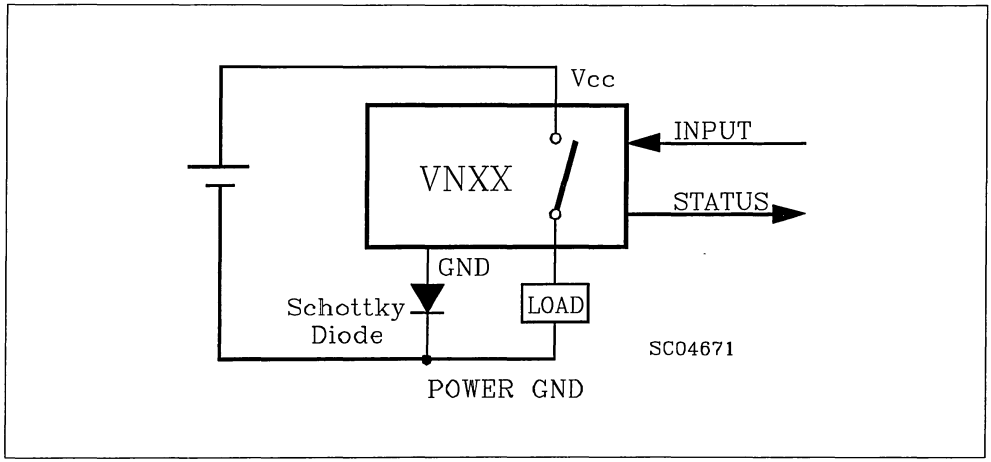
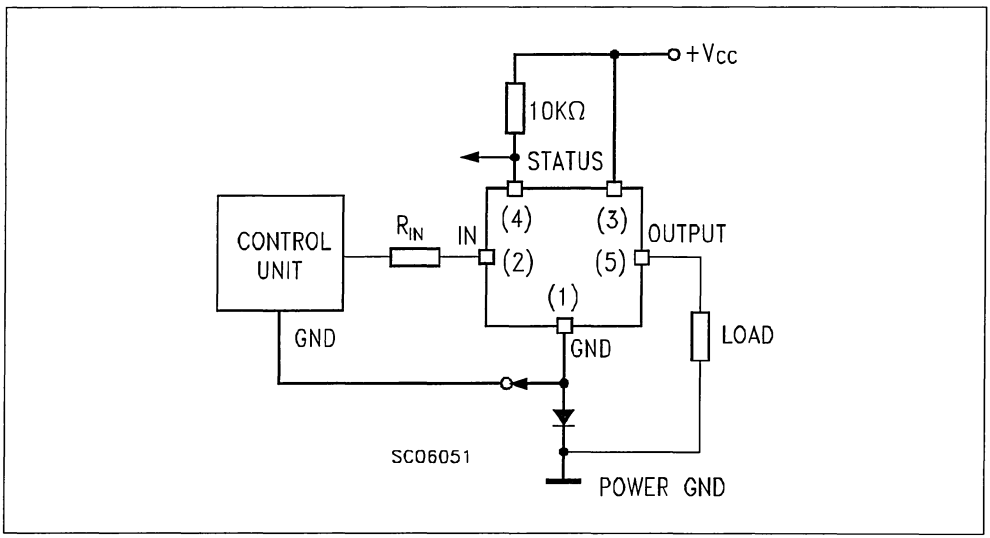


Figure 4: Typical Application Circuit With Separate Signal Ground

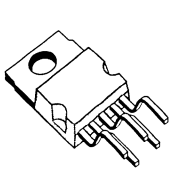


ISO HIGH SIDE SMART POWER SOLID STATE RELAY

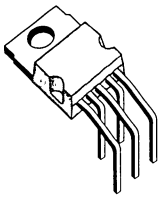
PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_n(*)	V_{CC}
VN31	60 V	0.03 Ω	11.5 A	26 V

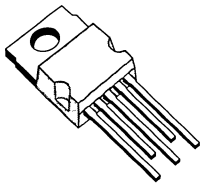
- MAXIMUM CONTINUOUS OUTPUT CURRENT (#): 25 A @ T_c= 85°C
- 5V LOGIC LEVEL COMPATIBLE INPUT
- THERMAL SHUT-DOWN
- UNDER VOLTAGE PROTECTION
- OPEN DRAIN DIAGNOSTIC OUTPUT
- INDUCTIVE LOAD FAST DEMAGNETIZATION
- VERY LOW STAND-BY POWER DISSIPATION



PENTAWATT (vertical)



PENTAWATT (horizontal)



PENTAWATT (in-line)

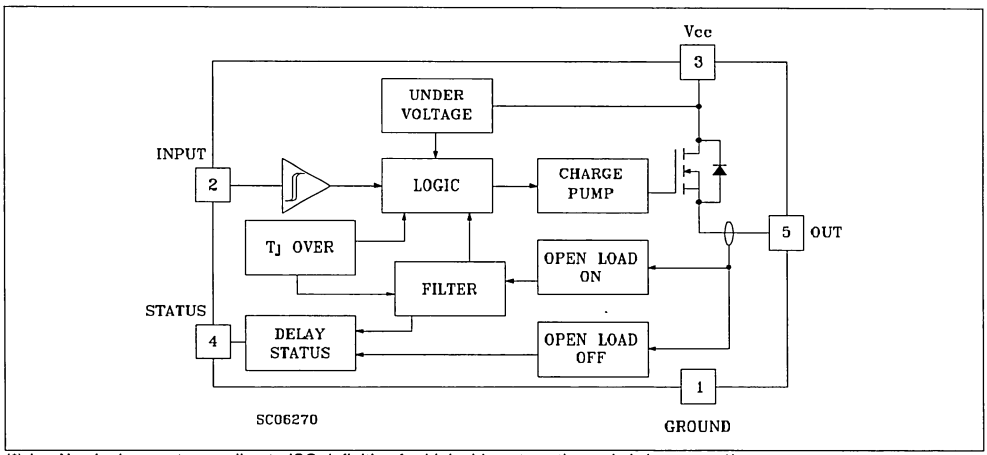
ORDER CODES:

PENTAWATT vertical	VN31
PENTAWATT horizontal	VN31 (011Y)
PENTAWATT in-line	VN31 (012Y)

DESCRIPTION

The VN31 is a monolithic device made using SGS-THOMSON Vertical Intelligent Power Technology, intended for driving resistive or inductive loads with one side grounded.
Built-in thermal shut-down protects the chip from over temperature and short circuit.
The open drain diagnostic output indicates: open load in off state and in on state, output shorted to V_{CC} and overtemperature. Fast demagnetization of inductive loads is archieved by negative (-18V) load voltage at turn-off.

BLOCK DIAGRAM

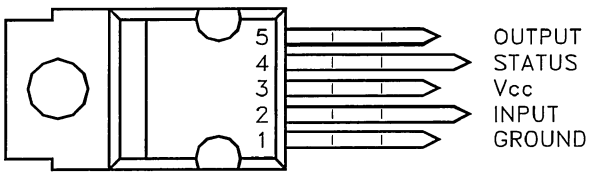


(*) In= Nominal current according to ISO definition for high side automotive switch (see note 1)
(#) The maximum continuous output current is the current at T_c = 85 °C for a battery voltage of 13 V which does not activate self protection

ABSOLUTE MAXIMUM RATING

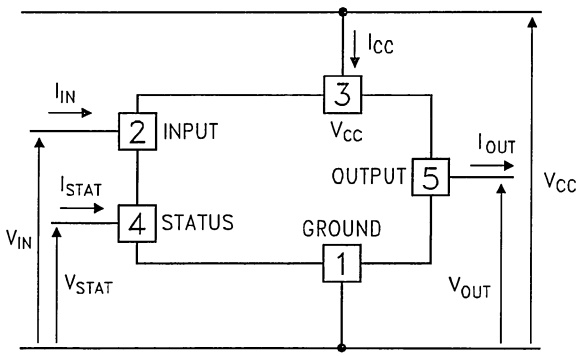
Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	V
I_{OUT}	Output Current (cont.) at T_c = 85 °C	25	A
I_R	Reverse Output Current at T_c = 85 °C	-25	A
I_{IN}	Input Current	±10	mA
$-V_{CC}$	Reverse Supply Voltage	-4	V
I_{STAT}	Status Current	±10	mA
V_{ESD}	Electrostatic Discharge (1.5 kΩ, 100 pF)	2000	V
P_{tot}	Power Dissipation at T_c = 85 °C	35	W
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

CONNECTION DIAGRAM



PC10000

CURRENT AND VOLTAGE CONVENTIONS



SC04660

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.56	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 13 V; -40 ≤ T_j ≤ 125 °C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		5.5	13	26	V
In(*)	Nominal Current	T_c = 85 °C $V_{DS(on)}$ ≤ 0.5 (note 1)	11.5			A
R_{on}	On State Resistance	I_{OUT} = 11.5 A I_{OUT} = 11.5 A T_j = 25 °C			0.06 0.03	Ω Ω
I_S	Supply Current	Off State T_j ≥ 25 °C On State			50 15	µA mA
$V_{DS(MAX)}$	Maximum Voltage Drop	I_{OUT} = 25 A T_c = 85 °C			1.5	V

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(^)	Turn-on Delay Time Of Output Current	I_{OUT} = 11.5 A Resistive Load Input Rise Time < 0.1 µs		90		µs
t_r(^)	Rise Time Of Output Current	I_{OUT} = 11.5A Resistive Load Input Rise Time < 0.1 µs		100		µs
$t_{d(off)}$(^)	Turn-off Delay Time Of Output Current	I_{OUT} = 11.5 A Resistive Load Input Rise Time < 0.1 µs		140		µs
t_f(^)	Fall Time Of Output Current	I_{OUT} = 11.5 A Resistive Load Input Rise Time < 0.1 µs		50		µs
$(di/dt)_{on}$	Turn-on Current Slope	I_{OUT} = 11.5 A I_{OUT} = I_{ov}		0.08	0.5 1	A/µs A/µs
$(di/dt)_{off}$	Turn-off Current Slope	I_{OUT} = 11.5 A I_{OUT} = I_{ov}		0.2	3 3	A/µs A/µs
V_{demag}	Inductive Load Clamp Voltage	I_{OUT} = 11.5 A L = 1 mH	-24	-18	-14	V

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				0.8	V
V_{IH}	Input High Level Voltage		2		(•)	V
$V_{I(hyst)}$	Input Hysteresis Voltage			0.5		V
I_{IN}	Input Current	V_{IN} = 5 V V_{IN} = 2 V V_{IN} = 0.8 V	 25	250	500 250 	µA µA µA
V_{ICL}	Input Clamp Voltage	I_{IN} = 10 mA I_{IN} = -10 mA	5.5	6 -0.7	 -0.3	V V

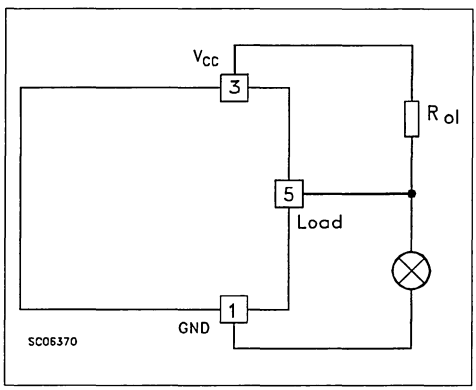
ELECTRICAL CHARACTERISTICS (continued)

PROTECTION AND DIAGNOSTICS (continued)

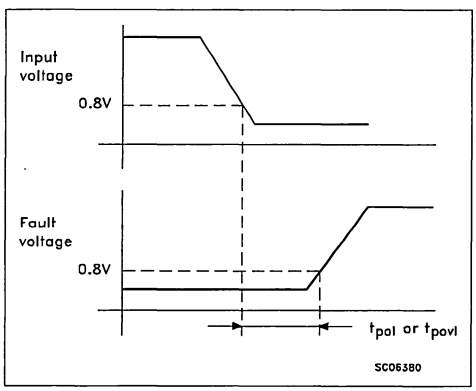
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status Voltage Output Low	I_{STAT} = 1.6 mA			0.4	V
V_{USD}	Under Voltage Shut Down			5		V
V_{SCL}	Status Clamp Voltage	I_{STAT} = 10 mA I_{STAT} = -10 mA		6 -0.7		V V
I_{OV}	Over Current	R_{LOAD} < 10 mΩ -40 ≤ T_c ≤ 125 °C		140		A
I_{AV}	Average Current in Short Circuit	R_{LOAD} < 10 mΩ T_c = 85 °C		2.5		A
I_{OL}	Open Load Current Level		5	600	1250	mA
T_{TSD}	Thermal Shut-down Temperature		140			°C
T_R	Reset Temperature		125			°C
V_{OL}	Open Load Voltage Level	Off-State (note 2)	2.5	3.75	5	V
$t_{1(on)}$	Open Load Filtering Time	(note 3)	1	5	10	ms
$t_{1(off)}$	Open Load Filtering Time	(note 3)	1	5	10	ms
$t_{2(off)}$	Open Load Filtering Time	(note 3)	1	5	10	ms
t_{povl}	Status Delay	(note 3)		5	10	µs
t_{pol}	Status Delay	(note 3)	50	700		µs

(^) See Switchig Time Waveforms
(•) The V_{IH} is internally clamped at 6V about. It is possible to connect this pin to an higher voltage via an external resistor calculated to not exceed 10 mA at the input pin.
note 1: The Nominal Current is the current at T_c = 85 °C for battery voltage of 13V which produces a voltage drop of 0.5 V
note 2: $I_{OL(off)} = (V_{CC} - V_{OL})/R_{OL}$ (see figure)
note 3: $t_{1(on)}$: minimum open load duration which acctivates the status output
$t_{1(off)}$: minimum load recovery time which desactivates the status output
$t_{2(off)}$: minimum on time after thermal shut down which desactivates status output
t_{povl} t_{pol}: ISO definition (see figure)

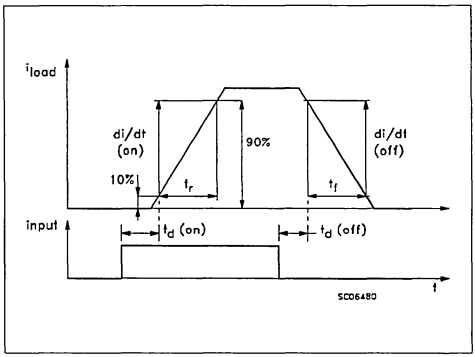
Note 2 Relevant Figure



Note 3 Relevant Figure



Switching Time Waveforms



FUNCTIONAL DESCRIPTION

The device has a diagnostic output which indicates open load conditions in off state as well as in on state, output shorted to V_{CC} and overtemperature. The truth table shows input, diagnostic and output voltage level in normal operation and in fault conditions. The output signals are processed by internal logic. The open load diagnostic output has a 5 ms filtering. The filter gives a continuous signal for the fault condition after an initial delay of about 5 ms. This means that a disconnection during normal operation, with a duration of less than 5 ms does not affect the status output. Equally, any re-connection of less than 5 ms during a disconnection duration does not affect the status output. No delay occur for the status to go low in case of overtemperature conditions. From the falling edge of the input signal the status output initially low in fault condition (over temperature or open load) will go back with a delay (t_{povl})in case of overtemperature condition and a delay (t_{pol}) in case of open load. These feature fully comply with International Standard Office (I.S.O.) requirement for automotive High Side Driver.

To protect the device against short circuit and over current conditions over the full range of supply voltage (V_{CC}) and temperature, the thermal protection turns the integrated Power MOS off at a minimum junction temperature of 140 °C. When the temperature returns to 125 °C the switch is automatically turned on again. In short circuit the protection reacts with virtually no delay, the sensor being located in the region of the die where the heat is generated. Driving inductive loads, an internal function of the device ensures the fast demagnetization with a typical voltage (V_{demag}) of -18V.

This function allows to greatly reduce the power dissipation according to the formula:

$P_{dem} = 0.5 \bullet L_{load} \bullet (I_{load})^2 \bullet [(V_{CC}+V_{demag})/V_{demag}] \bullet f$

where f = switching frequency and

V_{demag} = demagnetization voltage

Based on this formula it is possible to know the value of inductance and/or current to avoid a thermal shut-down. The maximum inductance which causes the chip temperature to reach the shut down temperature in a specific thermal environment, is infact a function of the load current for a fixed V_{CC}, V_{demag} and f.

PROTECTING THE DEVICE AGAIST LOAD DUMP - TEST PULSE 5

The device is able to withstand the test pulse No. 5 at level II (V_S = 46.5V) according to the ISO T/R 7637/1 without any external component. This means that all functions of the device are performed as designed after exposure to disturbance at level II. The VN31 is able to withstand the test pulse No.5 at level III adding an external resistor of 150 ohm between pin 1 and ground plus a filter capacitor of 1000 µF between pin 3 and ground (if $R_{LOAD} \leq 20\ \Omega$).

PROTECTING THE DEVICE AGAINST REVERSE BATTERY

The simplest way to protect the device against a continuous reverse battery voltage (-26V) is to insert a Schottky diode between pin 1(GND) and ground, as shown in the typical application circuit (fig.3).

The consequences of the voltage drop across this diode are as follows:

- If the input is pulled to power GND, a negative voltage of -V_f is seen by the device. (Vil, Vih thresholds and Vstat are increased by Vf with respect to power GND).
- The undervoltage shutdown level is increased by Vf.

If there is no need for the control unit to handle external analog signals referred to the power GND, the best approach is to connect the reference potential of the control unit to node [1] (see application circuit in fig. 4), which becomes the common signal GND for the whole control board avoiding shift of V_{ih}, V_{il} and V_{stat}. This solution allows the use of a standard diode.

TRUTH TABLE

	INPUT	OUTPUT	DIAGNOSTIC
Normal Operation	L H	L H	H H
Over-temperature	H	L	L
Under-voltage	X	L	H
Short load to V_{CC}	L	H	L

Figure 1: Waveforms

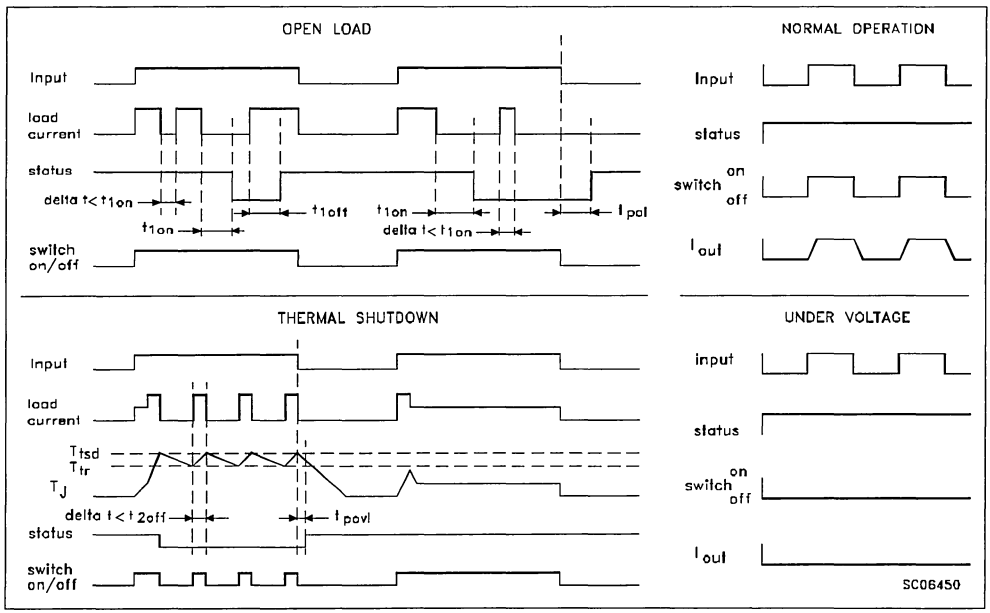


Figure 2: Over Current Test Circuit

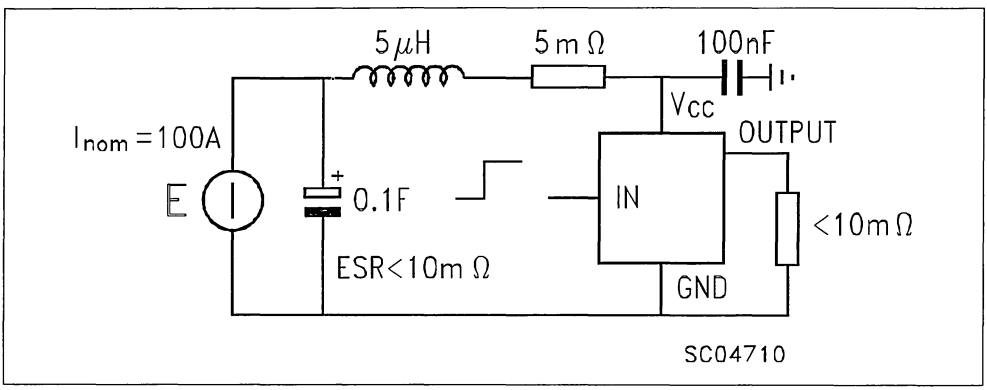


Figure 3: Typical Application Circuit With A Schottky Diode For Reverse Supply Protection

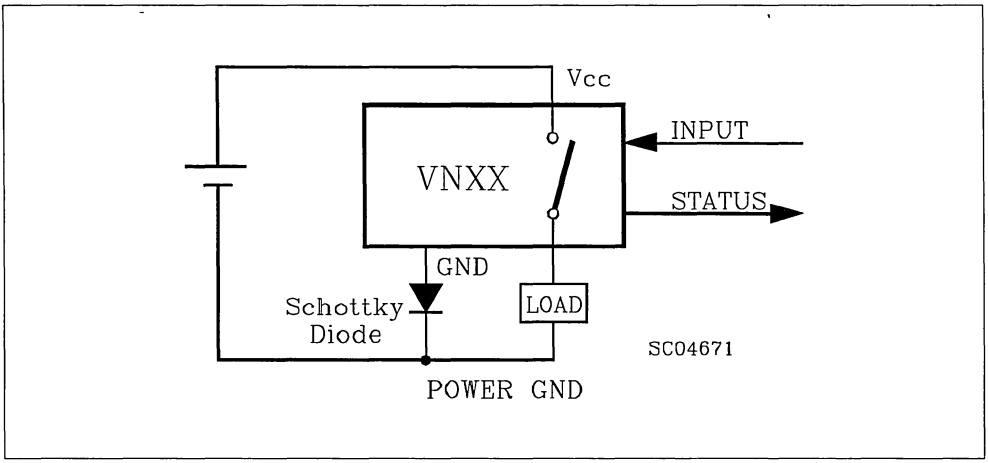
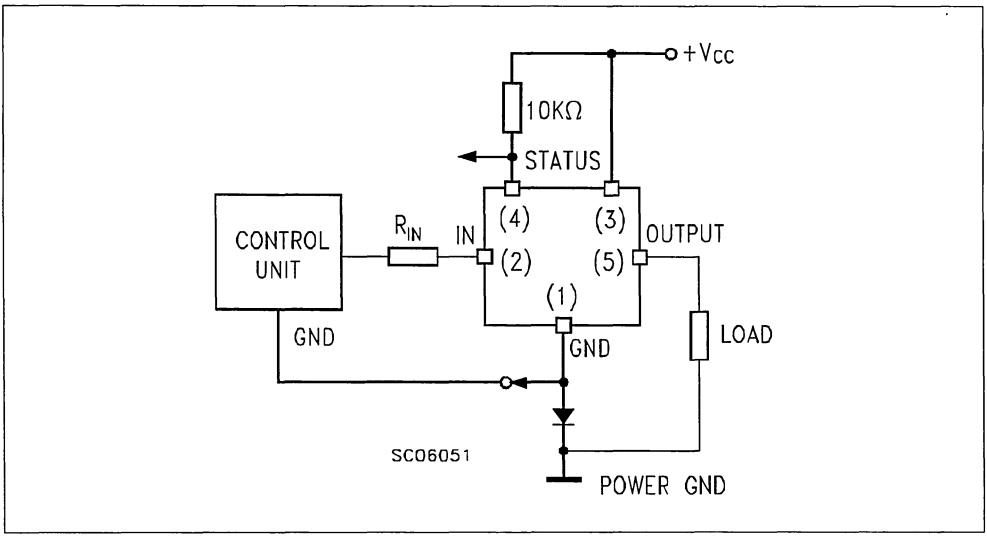


Figure 4: Typical Application Circuit With Separate Signal Ground



SGS-THOMSON MICROELECTRONICS

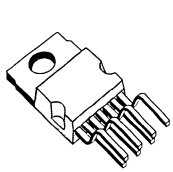
VND05B

DOUBLE CHANNEL HIGH SIDE SMART POWER SOLID STATE RELAY

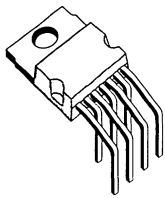
PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_n(*)	V_{CC}
VND05B	40 V	0.2 Ω	1.6 A	26 V

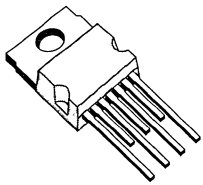
- OUTPUT CURRENT (CONTINUOUS): 7.5 A @ T_C=85°C PER CHANNEL
- 5V LOGIC LEVEL COMPATIBLE INPUT
- THERMAL SHUT-DOWN
- UNDER VOLTAGE PROTECTION
- OPEN DRAIN DIAGNOSTIC OUTPUT
- INDUCTIVE LOAD FAST DEMAGNETIZATION
- VERY LOW STAND-BY POWER DISSIPATION



HEPTAWATT (vertical)



HEPTAWATT (horizontal)



HEPTAWATT (in-line)

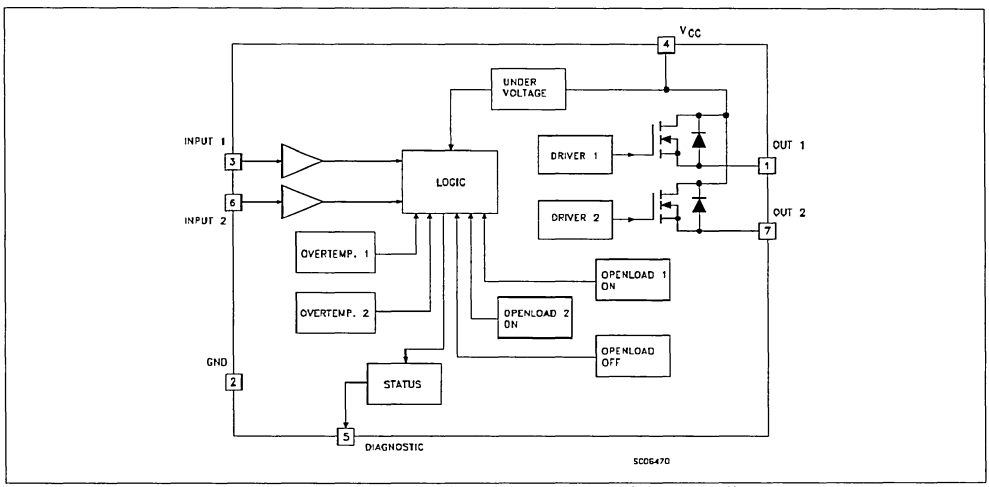
ORDER CODES:

HEPTAWATT vertical	VND05B
HEPTAWATT horizontal	VND05B (011Y)
HEPTAWATT in-line	VND05B (012Y)

DESCRIPTION

The VND05B is a monolithic device made using SGS-THOMSON Vertical Intelligent Power Technology, intended for driving resistive or inductive loads with one side grounded. This device has two channels, and a common diagnostic. Built-in thermal shut-down protects the chip from over temperature and short circuit. The status output provides an indication of open load in on state, open load in off state, overtemperature conditions and stuck-on to V_{CC}.

BLOCK DIAGRAM

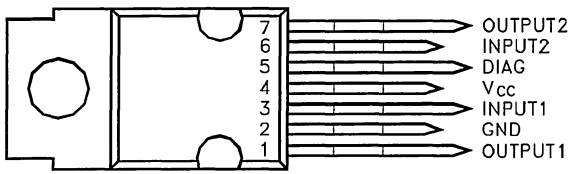


(*) In= Nominal current according to ISO definition for high side automotive switch (see note 1)

ABSOLUTE MAXIMUM RATING

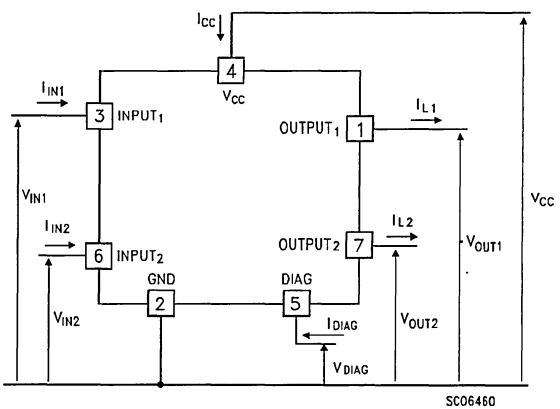
Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	40	V
I_{OUT}	Output Current (cont.) at T_c = 85 °C	7.5	A
$I_{OUT}(RMS)$	RMS Output Current at T_c = 85 °C and f > 1Hz	7.5	A
I_R	Reverse Output Current at T_c = 85 °C	-7.5	A
I_{IN}	Input Current	±10	mA
$-V_{CC}$	Reverse Supply Voltage	-4	V
I_{STAT}	Status Current	±10	mA
V_{ESD}	Electrostatic Discharge (1.5 kΩ, 100 pF)	2000	V
P_{tot}	Power Dissipation at T_c = 25 °C	50	W
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

CONNECTION DIAGRAM



PC11070

CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.5	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

ELECTRICAL CHARACTERISTICS ($8 < V_{CC} < 16$ V; $-40 \le T_j \le 125$ °C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		6	13	26	V
In(*)	Nominal Current	$T_c = 85$ °C $V_{DS(on)} \le 0.5$ $V_{CC} = 13$ V	1.6		2.6	A
R_{on}	On State Resistance	$I_{OUT} = I_n$ $V_{CC} = 13$ V $T_j = 25$ °C	0.13		0.2	Ω
I_S	Supply Current	Off State $T_j = 25$ °C $V_{CC} = 13$ V		35	100	µA
$V_{DS(MAX)}$	Maximum Voltage Drop	$I_{OUT} = 7.5$ A $T_j = 85$ °C $V_{CC} = 13$ V	1.44		2.3	V
R_i	Output to GND internal Impedance	$T_j = 25$ °C	5	10	20	KΩ

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(^)	Turn-on Delay Time Of Output Current	$R_{out} = 5.4$ Ω	5	25	200	µs
t_r(^)	Rise Time Of Output Current	$R_{out} = 5.4$ Ω	10	50	180	µs
$t_{d(off)}$(^)	Turn-off Delay Time Of Output Current	$R_{out} = 5.4$ Ω	10	75	250	µs
t_f(^)	Fall Time Of Output Current	$R_{out} = 5.4$ Ω	10	35	180	µs
$(di/dt)_{on}$	Turn-on Current Slope	$R_{out} = 5.4$ Ω	0.003		0.1	A/µs
$(di/dt)_{off}$	Turn-off Current Slope	$R_{out} = 5.4$ Ω	0.005		0.1	A/µs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				1.5	V
V_{IH}	Input High Level Voltage		3.5		(•)	V
$V_{I(hyst)}$	Input Hysteresis Voltage		0.2	0.9	1.5	V
I_{IN}	Input Current	$V_{IN} = 5$ V $T_j = 25$ °C		30	100	µA
V_{ICL}	Input Clamp Voltage	$I_{IN} = 10$ mA $I_{IN} = -10$ mA	5	6 -0.7	7	V V

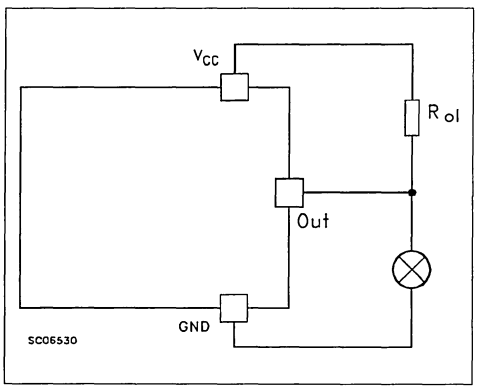
ELECTRICAL CHARACTERISTICS (continued)

PROTECTION AND DIAGNOSTICS

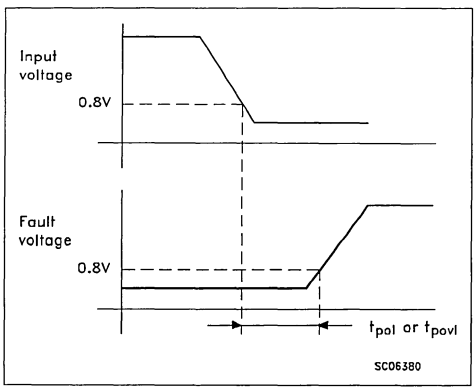
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status Voltage Output Low	I_{STAT} = 1.6 mA			0.4	V
V_{USD}	Under Voltage Shut Down		3.5	4.5	6	V
V_{SCL}	Status Clamp Voltage	I_{STAT} = 10 mA I_{STAT} = -10 mA	5	6 -0.7	7	V V
T_{TSD}	Thermal Shut-down Temperature		140	160	180	°C
$T_{SD(hyst.)}$	Thermal Shut-down Hysteresis				50	°C
T_R	Reset Temperature		125			°C
V_{OL}	Open Voltage Level	Off-State (note 2)	2.5	4	5	V
I_{OL}	Open Load Current Level	On-State	5		180	mA
t_{povl}	Status Delay	(note 3)		5	10	µs
t_{pol}	Status Delay	(note 3)	50	500	2500	µs

(*) In= Nominal current according to ISO definition for high side automotive switch (see note 1)
(^) See switching time waveform
(•) The V_{IH} is internally clamped at 6V about. It is possible to connect this pin to an higher voltage via an external resistor calculated to not exceed 10 mA at the input pin.
note 1: The Nominal Current is the current at T_c = 85 °C for battery voltage of 13V which produces a voltage drop of 0.5 V
note 2: $I_{OL(off)} = (V_{CC} - V_{OL})/R_{OL}$
note 3: t_{povl} t_{pol}: ISO definition

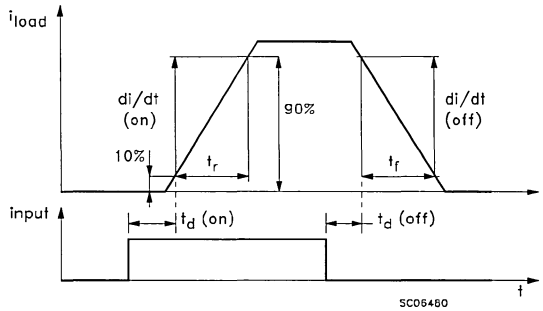
Note 2 Relevant Figure



Note 3 Relevant Figure



Switching Time Waveforms



FUNCTIONAL DESCRIPTION

The device has a common diagnostic output for both channels which indicates open load in on-state, open load in off-state, over temperature conditions and stuck-on to V_{CC}.

From the falling edge of the input signal, the status output, initially low to signal a fault condition (overtemperature or open load on-state), will go back to a high state with a different delay in case of overtemperature (tpovl) and in case of open open load (tpol) respectively. This feature allows to discriminate the nature of the detected fault. To protect the device against short circuit and over current condition over the full range of supply voltage (V_{CC}) and temperature, the thermal protection turns the integrated Power MOS off at a minimum junction temperature of 140 °C. When this temperature returns to 125 °C the switch is automatically turned on again. In short circuit the protection reacts with virtually no delay, the sensor (one for each channel) being located inside each of the two Power MOS areas. This positioning allows the device to operate with one channel in automatic thermal cycling and the other one on a normal load. An internal function of the devices ensures the fast demagnetization of inductive loads with a typical voltage (V_{demag}) of -18V. This function allows to greatly reduces the power dissipation according to the formula:

$P_{dem} = 0.5 \bullet L_{load} \bullet (I_{load})^2 \bullet [(V_{CC}+V_{demag})/V_{demag}] \bullet f$

where f = switching frequency and

V_{demag} = demagnetization voltage.

The maximum inductance which causes the chip temperature to reach the shut-down temperature in a specified thermal environment is a function of the load current for a fixed V_{CC}, Vdemag and f according to the above formula. In this device if the GND pin is disconnected, with V_{CC} not exceeding 16V, both channel will switch off.

PROTECTING THE DEVICE AGAINST REVERSE BATTERY

The simplest way to protect the device against a continuous reverse battery voltage (-26V) is to insert a Schottky diode between pin 2 (GND) and ground, as shown in the typical application circuit (fig.2).

The consequences of the voltage drop across this diode are as follows:

- If the input is pulled to power GND, a negative voltage of $-V_f$ is seen by the device. (Vil, Vih thresholds and Vstat are increased by Vf with respect to power GND).
- The undervoltage shutdown level is increased by Vf.

If there is no need for the control unit to handle external analog signals referred to the power GND, the best approach is to connect the reference potential of the control unit to the device ground (see application circuit in fig. 3), which becomes the common signal GND for the whole control board avoiding shift of V_{ih}, V_{il} and V_{stat}. This solution allows the use of a standard diode.

TRUTH TABLE

		INPUT 1	INPUT 2	OUTPUT 1	OUTPUT 2	DIAGNOSTIC
Normal Operation		L H L H	L H H L	L H L H	L H H L	H H H H
Under-voltage		X	X	L	L	H
Thermal Shutdown	Channel 1	H	X	L	X	L
	Channel 2	X	H	X	L	L
Open Load	Channel 1	H L	X L	H L	X L	L L(**)
	Channel 2	X L	H L	X L	H L	L L(**)
Output Shorted to V_{CC}	Channel 1	H L	X L	H H	X L	L L
	Channel 2	X L	H L	X L	H H	L L

Figure 1: Waveforms

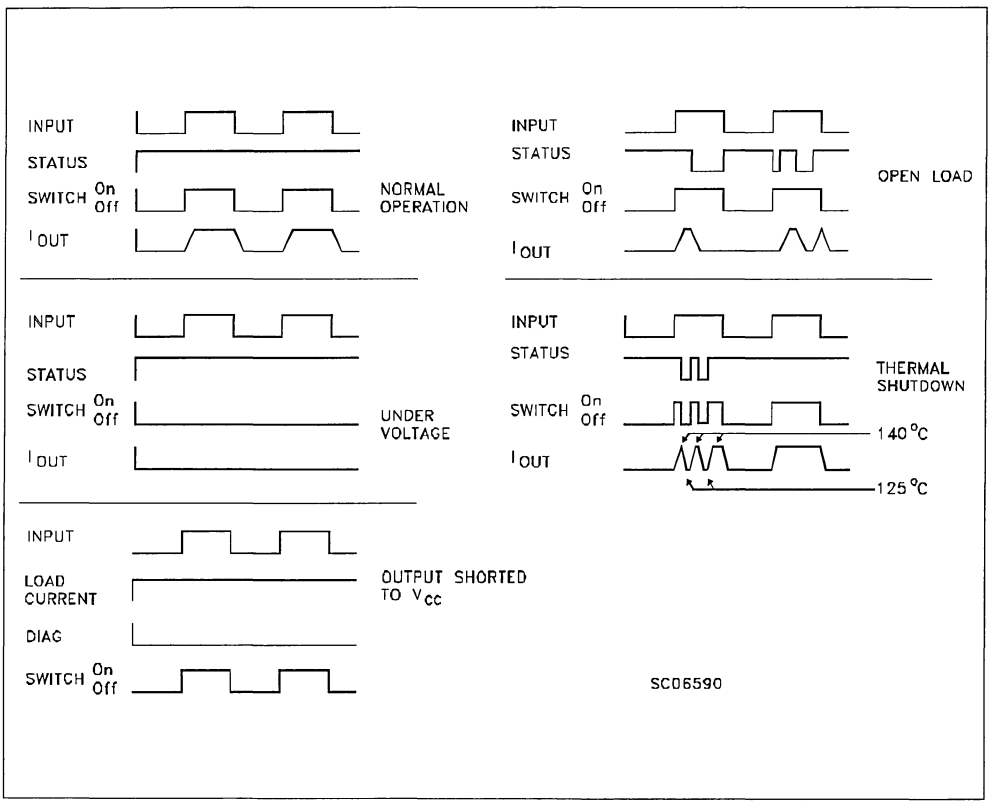


Figure 2: Typical Application Circuit With A Schottky Diode For Reverse Supply Protection

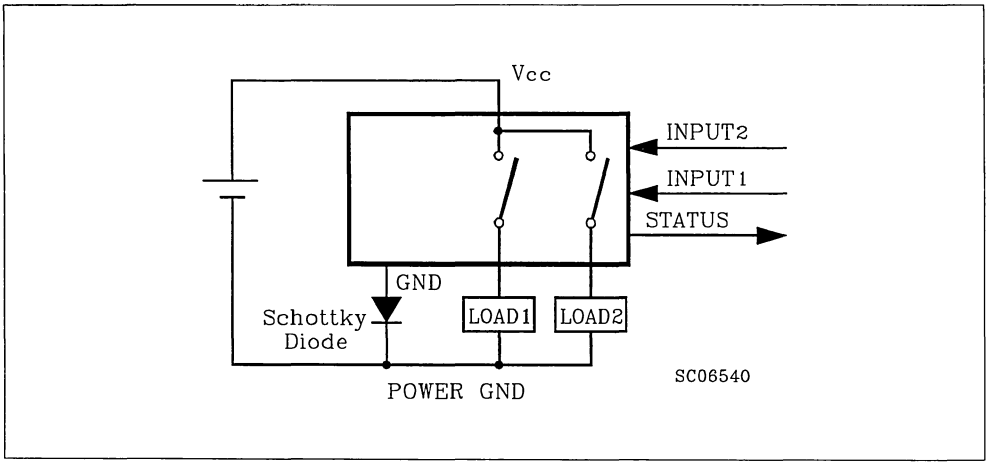
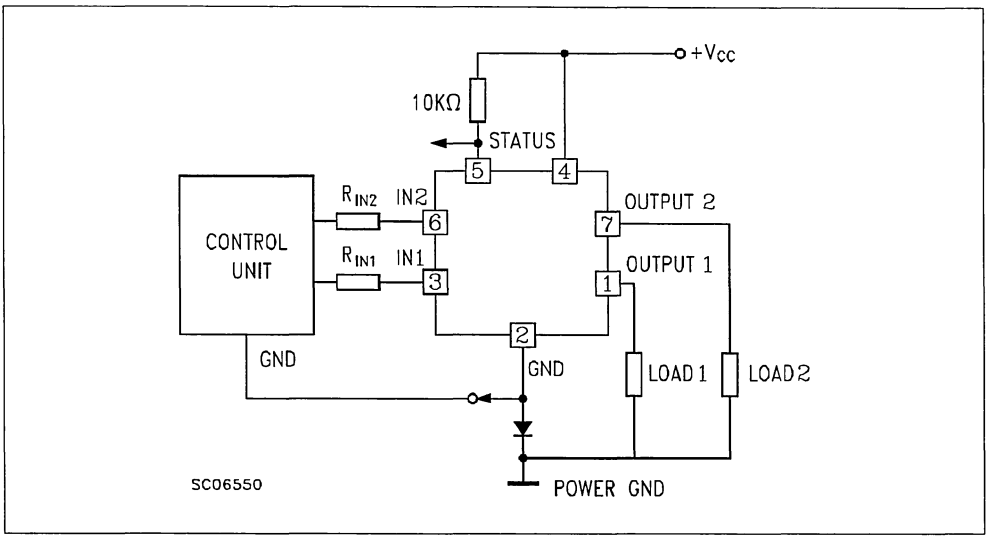


Figure 3: Typical Application Circuit With Separate Signal Ground



SGS-THOMSON MICROELECTRONICS

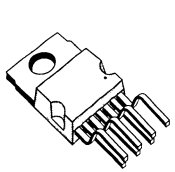
VND10B

DOUBLE CHANNEL HIGH SIDE SMART POWER SOLID STATE RELAY

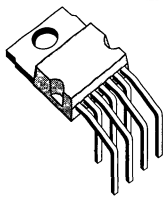
PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_n(*)	V_{CC}
VND10B	40 V	0.1 Ω	3.4 A	26 V

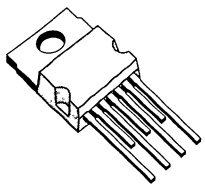
- OUTPUT CURRENT (CONTINUOUS): 13 A @ T_c=85°C PER CHANNEL
- 5V LOGIC LEVEL COMPATIBLE INPUT
- THERMAL SHUT-DOWN
- UNDER VOLTAGE PROTECTION
- OPEN DRAIN DIAGNOSTIC OUTPUT
- INDUCTIVE LOAD FAST DEMAGNETIZATION
- VERY LOW STAND-BY POWER DISSIPATION



HEPTAWATT (vertical)



HEPTAWATT (horizontal)



HEPTAWATT (in-line)

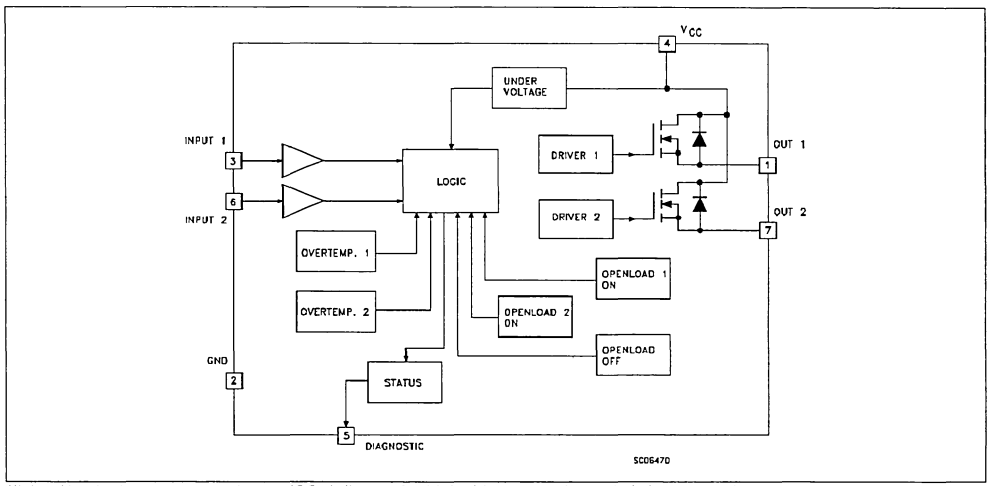
ORDER CODES:

HEPTAWATT vertical	VND10B
HEPTAWATT horizontal	VND10B (011Y)
HEPTAWATT in-line	VND10B (012Y)

DESCRIPTION

The VND10B is a monolithic device made using SGS-THOMSON Vertical Intelligent Power Technology, intended for driving resistive or inductive loads with one side grounded. This device has two channels, and a common diagnostic. Built-in thermal shut-down protects the chip from over temperature and short circuit. The status output provides an indication of open load in on state, open load in off state, overtemperature conditions and stuck-on to V_{CC}.

BLOCK DIAGRAM

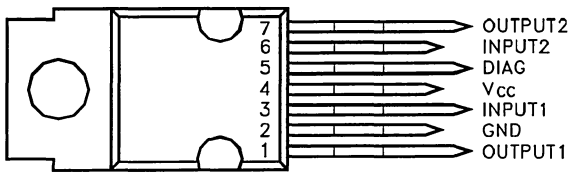


(*) In= Nominal current according to ISO definition for high side automotive switch (see note 1)

ABSOLUTE MAXIMUM RATING

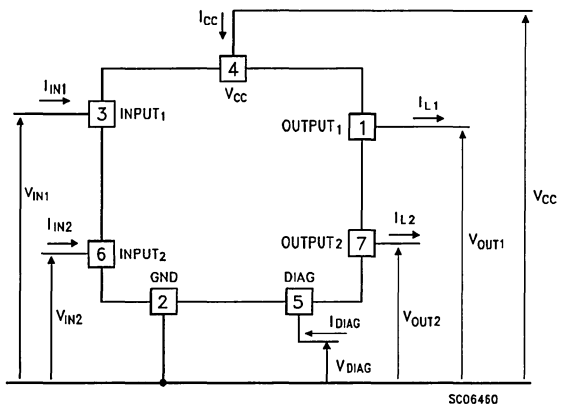
Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	40	V
I_{OUT}	Output Current (cont.) at T_c = 85 °C	13	A
$I_{OUT}(RMS)$	RMS Output Current at T_c = 85 °C and f > 1Hz	13	A
I_R	Reverse Output Current at T_c = 85 °C	-13	A
I_{IN}	Input Current	±10	mA
$-V_{CC}$	Reverse Supply Voltage	-4	V
I_{STAT}	Status Current	±10	mA
V_{ESD}	Electrostatic Discharge (1.5 kΩ, 100 pF)	2000	V
P_{tot}	Power Dissipation at T_c = 25 °C	64	W
T_j	Junction Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

CONNECTION DIAGRAM



PC11070

CURRENT AND VOLTAGE CONVENTIONS



SC06460

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.8	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

ELECTRICAL CHARACTERISTICS ($8 < V_{CC} < 16$ V; $-40 \le T_j \le 125$ °C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		6	13	26	V
In(*)	Nominal Current	$T_c = 85$ °C $V_{DS(on)} \le 0.5$ $V_{CC} = 13$ V	3.4		5.2	A
R_{on}	On State Resistance	$I_{OUT} = I_n$ $V_{CC} = 13$ V $T_j = 25$ °C	0.065		0.1	Ω
I_S	Supply Current	Off State $T_j = 25$ °C $V_{CC} = 13$ V		35	100	µA
$V_{DS(MAX)}$	Maximum Voltage Drop	$I_{OUT} = 13$ A $T_j = 85$ °C $V_{CC} = 13$ V	1.2		2	V
R_i	Output to GND internal Impedance	$T_j = 25$ °C	5	10	20	KΩ

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(^)	Turn-on Delay Time Of Output Current	$R_{out} = 2.7$ Ω	5	35	200	µs
t_r(^)	Rise Time Of Output Current	$R_{out} = 2.7$ Ω	28	110	360	µs
$t_{d(off)}$(^)	Turn-off Delay Time Of Output Current	$R_{out} = 2.7$ Ω	10	140	500	µs
t_f(^)	Fall Time Of Output Current	$R_{out} = 2.7$ Ω	28	75	360	µs
$(di/dt)_{on}$	Turn-on Current Slope	$R_{out} = 2.7$ Ω	0.003		0.1	A/µs
$(di/dt)_{off}$	Turn-off Current Slope	$R_{out} = 2.7$ Ω	0.005		0.1	A/µs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage				1.5	V
V_{IH}	Input High Level Voltage		3.5		(•)	V
$V_{I(hyst)}$	Input Hysteresis Voltage		0.2	0.9	1.5	V
I_{IN}	Input Current	$V_{IN} = 5$ V $T_j = 25$ °C		30	100	µA
V_{ICL}	Input Clamp Voltage	$I_{IN} = 10$ mA $I_{IN} = -10$ mA	5	6 -0.7	7	V V

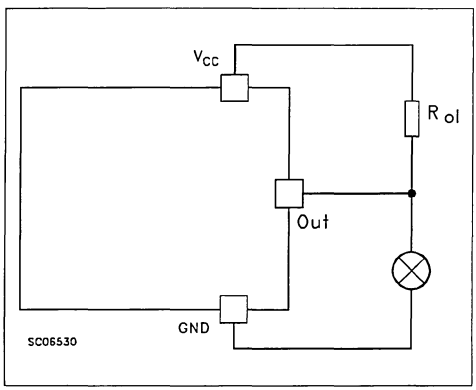
ELECTRICAL CHARACTERISTICS (continued)

PROTECTION AND DIAGNOSTICS

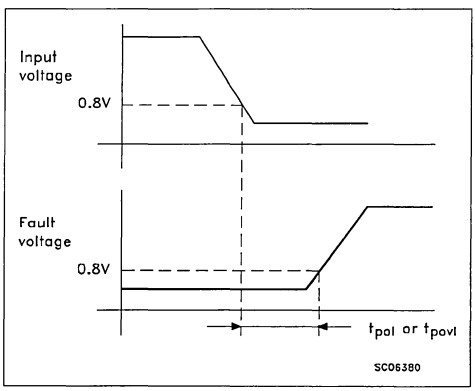
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status Voltage Output Low	I_{STAT} = 1.6 mA			0.4	V
V_{USD}	Under Voltage Shut Down		3.5	4.5	6	V
V_{SCL}	Status Clamp Voltage	I_{STAT} = 10 mA I_{STAT} = -10 mA	5	6 -0.7	7	V V
T_{TSD}	Thermal Shut-down Temperature		140	160	180	°C
$T_{SD(hyst)}$	Thermal Shut-down Hysteresis				50	°C
T_R	Reset Temperature		125			°C
V_{OL}	Open Voltage Level	Off-State (note 2)	2.5	4	5	V
I_{OL}	Open Load Current Level	On-State	0.5	0.9	1.3	A
t_{povl}	Status Delay	(note 3)		5	10	µs
t_{pol}	Status Delay	(note 3)	50	500	2500	µs

(*) In= Nominal current according to ISO definition for high side automotive switch (see note 1)
(^) See switching time waveform
(•) The V_{IH} is internally clamped at 6V about. It is possible to connect this pin to an higher voltage via an external resistor calculated to not exceed 10 mA at the input pin.
note 1: The Nominal Current is the current at T_c = 85 °C for battery voltage of 13V which produces a voltage drop of 0.5 V
note 2: $I_{OL(off)} = (V_{CC} - V_{OL})/R_{OL}$
note 3: t_{povl} t_{pol}: ISO definition

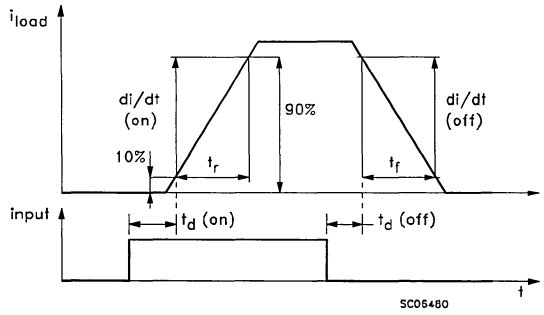
Note 2 Relevant Figure



Note 3 Relevant Figure



Switching Time Waveforms



FUNCTIONAL DESCRIPTION

The device has a common diagnostic output for both channels which indicates open load in on-state, open load in off-state, over temperature conditions and stuck-on to V_{CC}.

From the falling edge of the input signal, the status output, initially low to signal a fault condition (overtemperature or open load on-state), will go back to a high state with a different delay in case of overtemperature (tpovl) and in case of open open load (tpol) respectively. This feature allows to discriminate the nature of the detected fault. To protect the device against short circuit and over current condition over the full range of supply voltage (V_{CC}) and temperature, the thermal protection turns the integrated Power MOS off at a minimum junction temperature of 140 °C. When this temperature returns to 125 °C the switch is automatically turned on again. In short circuit the protection reacts with virtually no delay, the sensor (one for each channel) being located inside each of the two Power MOS areas. This positioning allows the device to operate with one channel in automatic thermal cycling and the other one on a normal load. An internal function of the devices ensures the fast demagnetization of inductive loads with a typical voltage (V_{demag}) of -18V. This function allows to greatly reduces the power dissipation according to the formula:

$P_{dem} = 0.5 \bullet L_{load} \bullet (I_{load})^2 \bullet [(V_{CC}+V_{demag})/V_{demag}] \bullet f$

where f = switching frequency and
V_{demag} = demagnetization voltage.

The maximum inductance which causes the chip temperature to reach the shut-down temperature in a specified thermal environment is a function of the load current for a fixed V_{CC}, Vdemag and f according to the above formula. In this device if the GND pin is disconnected, with V_{CC} not exceeding 16V, both channel will switch off.

PROTECTING THE DEVICE AGAINST REVERSE BATTERY

The simplest way to protect the device against a continuous reverse battery voltage (-26V) is to insert a Schottky diode between pin 2 (GND) and ground, as shown in the typical application circuit (fig. 2).

The consequences of the voltage drop across this diode are as follows:

- If the input is pulled to power GND, a negative voltage of $-V_f$ is seen by the device. (Vil, Vih thresholds and Vstat are increased by Vf with respect to power GND).
- The undervoltage shutdown level is increased by Vf.

If there is no need for the control unit to handle external analog signals referred to the power GND, the best approach is to connect the reference potential of the control unit to the device ground (see application circuit in fig. 3), which becomes the common signal GND for the whole control board avoiding shift of V_{ih}, V_{il} and V_{stat}. This solution allows the use of a standard diode.

TRUTH TABLE

		INPUT 1	INPUT 2	OUTPUT 1	OUTPUT 2	DIAGNOSTIC
Normal Operation		L H L H	L H H L	L H L H	L H H L	H H H H
Under-voltage		X	X	L	L	H
Thermal Shutdown	Channel 1	H	X	L	X	L
	Channel 2	X	H	X	L	L
Open Load	Channel 1	H L	X L	H L	X L	L L(**)
	Channel 2	X L	H L	X L	H L	L L(**)
Output Shorted to V_{CC}	Channel 1	H L	X L	H H	X L	L L
	Channel 2	X L	H L	X L	H H	L L

Figure 1: Waveforms

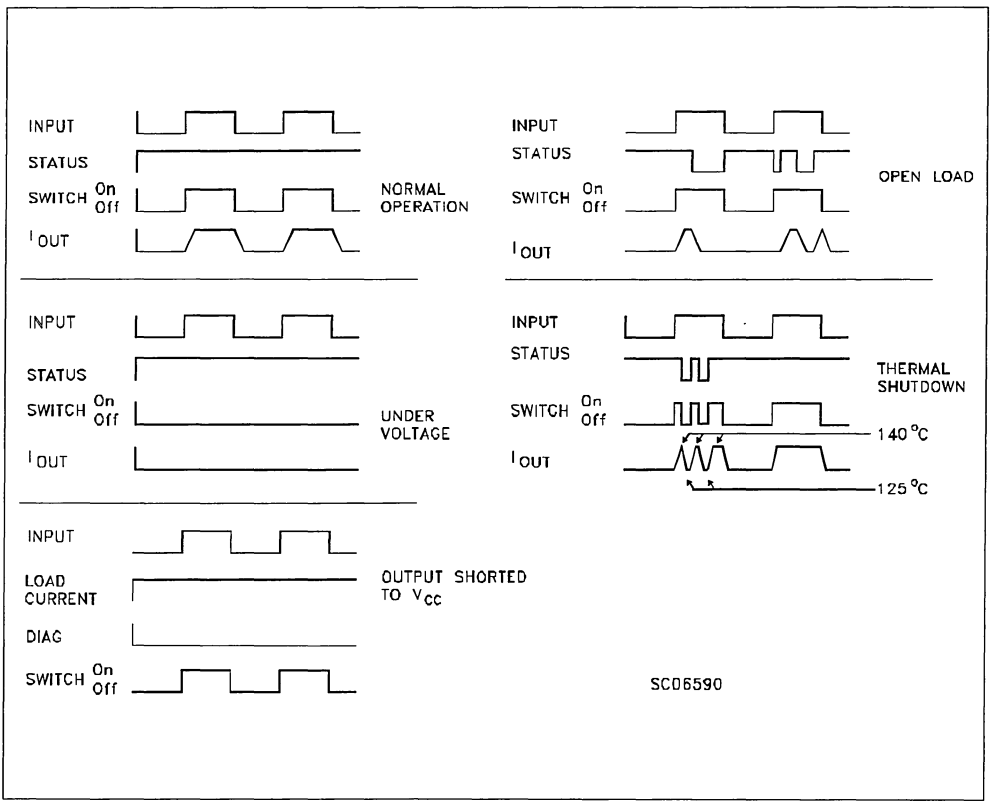


Figure 2: Typical Application Circuit With A Schottky Diode For Reverse Supply Protection

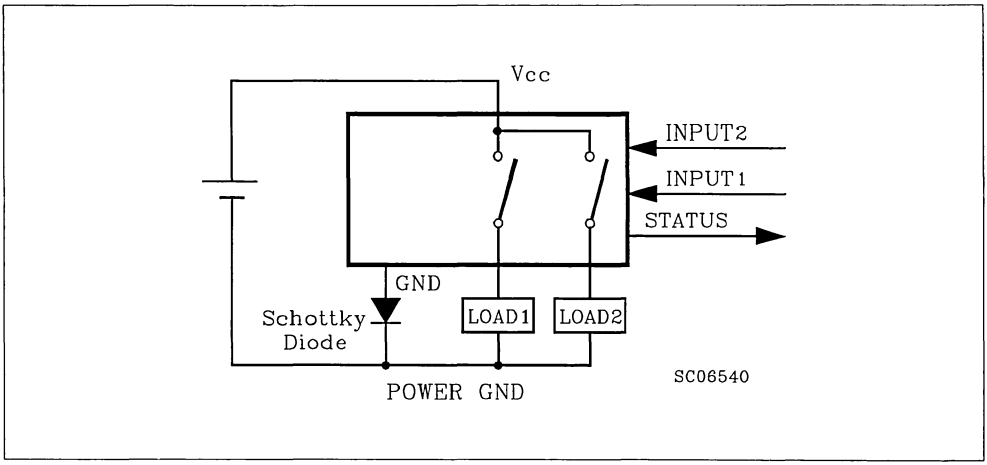
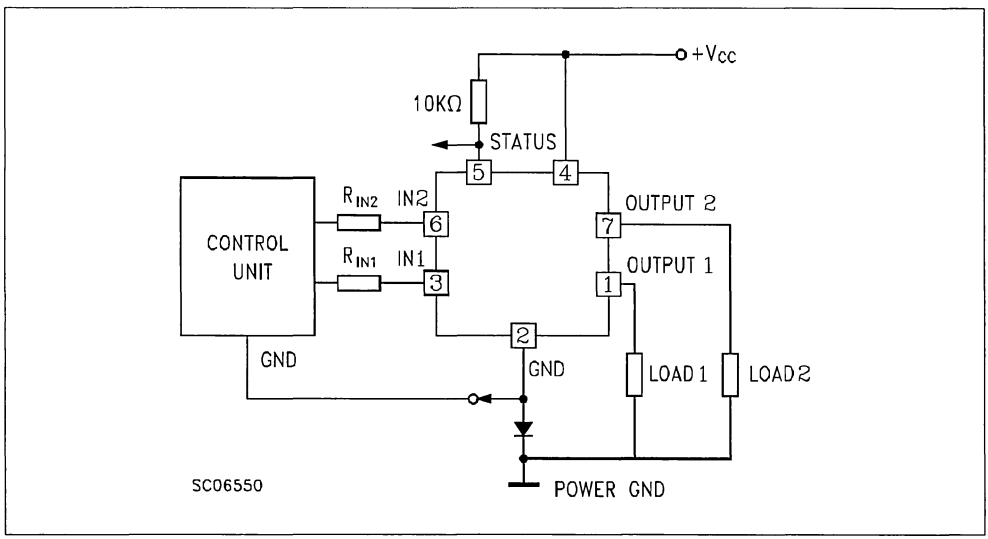


Figure 3: Typical Application Circuit With Separate Signal Ground



DISCRETE DATASHEETS

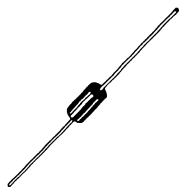
SGS-THOMSON MICROELECTRONICS

1.5KE6V8P,A/440P,A
1.5KE6V8CP,CA/440CP,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 1500 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 440 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).
- UL RECOGNIZED.



CB429
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code, and Cathode Band (for unidirectional types only).
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

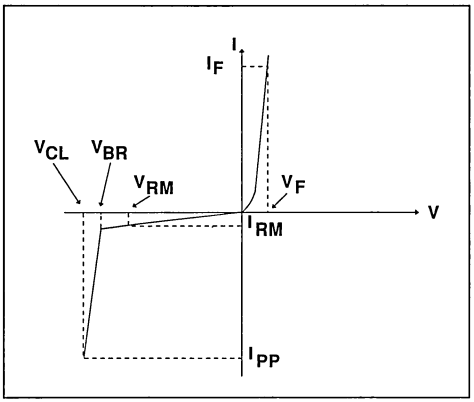
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	1500	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	5	W
I_{FSM}	Non repetitive surge peak forward current For Unidirectional types.	Tamb = 25°C t =10 ms	250	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 175	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	20	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. L_{lead} = 10 mm	75	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 100 A.



TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min	nom	max		V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
				note2									
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
P 1.5KE6V8P	P 1.5KE6V8CP	1000	5.8	6.45	6.8	7.48	10	10.5	143	13.4	746	5.7	9500
P 1.5KE6V8A	P 1.5KE6V8CA	1000	5.8	6.45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
P 1.5KE7V5P	1.5KE7V5CP	500	6.4	7.13	7.5	8.25	10	11.3	132	14.5	690	6.1	8500
1.5KE7V5A	P 1.5KE7V5CA	500	6.4	7.13	7.5	7.88	10	11.3	132	14.5	690	6.1	8500
1.5KE8V2P	1.5KE8V2CP	200	7.02	7.79	8.2	9.02	10	12.1	124	15.5	645	6.5	8000
P 1.5KE8V2A	P 1.5KE8V2CA	200	7.02	7.79	8.2	8.61	10	12.1	124	15.5	645	6.5	8000
1.5KE9V1P	1.5KE9V1CP	50	7.78	8.65	9.1	10	1	13.4	112	17.1	585	6.8	7500
1.5KE9V1A	1.5KE9V1CA	50	7.78	8.65	9.1	9.55	1	13.4	112	17.1	585	6.8	7500
1.5KE10P	1.5KE10CP	10	8.55	9.5	10	11	1	14.5	103	18.6	538	7.3	7000
P 1.5KE10A	P 1.5KE10CA	10	8.55	9.5	10	10.5	1	14.5	103	18.6	538	7.3	7000
1.5KE11P	1.5KE11CP	5	9.4	10.5	11	12.1	1	15.6	96	20.3	493	7.5	6400
1.5KE11A	1.5KE11CA	5	9.4	10.5	11	11.6	1	15.6	96	20.3	493	7.5	6400
1.5KE12P	P 1.5KE12CP	5	10.2	11.4	12	13.2	1	16.7	90	21.7	461	7.8	6000
P 1.5KE12A	P 1.5KE12CA	5	10.2	11.4	12	12.6	1	16.7	90	21.7	461	7.8	6000
1.5KE13P	1.5KE13CP	5	11.1	12.4	13	14.3	1	18.2	82	23.6	423	8.1	5500
P 1.5KE13A	P 1.5KE13CA	5	11.1	12.4	13	13.7	1	18.2	82	23.6	423	8.1	5500
P 1.5KE15P	P 1.5KE15CP	5	12.8	14.3	15	16.5	1	21.2	71	27.2	368	8.4	5000
P 1.5KE15A	P 1.5KE15CA	5	12.8	14.3	15	15.8	1	21.2	71	27.2	368	8.4	5000
1.5KE16P	1.5KE16CP	5	13.6	15.2	16	17.6	1	22.5	67	28.9	346	8.6	4700
1.5KE16A	1.5KE16CA	5	13.6	15.2	16	16.8	1	22.5	67	28.9	346	8.6	4700
P 1.5KE18P	P 1.5KE18CP	5	15.3	17.1	18	19.8	1	25.2	59.5	32.5	308	8.8	4300
P 1.5KE18A	P 1.5KE18CA	5	15.3	17.1	18	18.9	1	25.2	59.5	32.5	308	8.8	4300
P 1.5KE20P	P 1.5KE20CP	5	17.1	19	20	22	1	27.7	54	36.1	277	9.0	4000
P 1.5KE20A	1.5KE20CA	5	17.1	19	20	21	1	27.7	54	36.1	277	9.0	4000
1.5KE22P	1.5KE22CP	5	18.8	20.9	22	24.2	1	30.6	49	39.3	254	9.2	3700

P = Prefered device

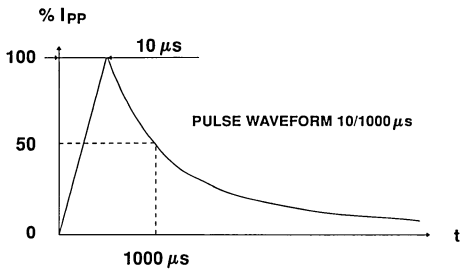
TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	Bidirectional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
1.5KE22A	1.5KE22CA	5	18.8	20.9	22	23.1	1	30.6	49	39.3	254	9.2	3700
1.5KE24P	1.5KE24CP	5	20.5	22.8	24	26.4	1	33.2	45	42.8	234	9.4	3500
P 1.5KE24A	1.5KE24CA	5	20.5	22.8	24	25.2	1	33.2	45	42.8	234	9.4	3500
P 1.5KE27P	1.5KE27CP	5	23.1	25.7	27	29.7	1	37.5	40	48.3	207	9.6	3200
1.5KE27A	1.5KE27CA	5	23.1	25.7	27	28.4	1	37.5	40	48.3	207	9.6	3200
1.5KE30P	P 1.5KE30CP	5	25.6	28.5	30	33	1	41.5	36	53.5	187	9.7	2900
P 1.5KE30A	P 1.5KE30CA	5	25.6	28.5	30	31.5	1	41.5	36	53.5	187	9.7	2900
P 1.5KE33P	P 1.5KE33CP	5	28.2	31.4	33	36.3	1	45.7	33	59.0	169	9.8	2700
P 1.5KE33A	1.5KE33CA	5	28.2	31.4	33	34.7	1	45.7	33	59.0	169	9.8	2700
P 1.5KE36P	P 1.5KE36CP	5	30.8	34.2	36	39.6	1	49.9	30	64.3	156	9.9	2500
P 1.5KE36A	P 1.5KE36CA	5	30.8	34.2	36	37.8	1	49.9	30	64.3	156	9.9	2500
P 1.5KE39P	P 1.5KE39CP	5	33.3	37.1	39	42.9	1	53.9	28	69.7	143	10.0	2400
P 1.5KE39A	P 1.5KE39CA	5	33.3	37.1	39	41.0	1	53.9	28	69.7	143	10.0	2400
1.5KE43P	1.5KE43CP	5	36.8	40.9	43	47.3	1	59.3	25.3	76.8	130	10.1	2200
P 1.5KE43A	P 1.5KE43CA	5	36.8	40.9	43	45.2	1	59.3	25.3	76.8	130	10.1	2200
1.5KE47P	1.5KE47CP	5	40.2	44.7	47	51.7	1	64.8	23.2	84	119	10.1	2050
P 1.5KE47A	P 1.5KE47CA	5	40.2	44.7	47	49.4	1	64.8	23.2	84	119	10.1	2050
1.5KE51P	1.5KE51CP	5	43.6	48.5	51	56.1	1	70.1	21.4	91	110	10.2	1950
P 1.5KE51A	1.5KE51CA	5	43.6	48.5	51	53.6	1	70.1	21.4	91	110	10.2	1950
1.5KE56P	1.5KE56CP	5	47.8	53.2	56	61.6	1	77	19.5	100	100	10.3	1800
P 1.5KE56A	1.5KE56CA	5	47.8	53.2	56	58.8	1	77	19.5	100	100	10.3	1800
1.5KE62P	1.5KE62CP	5	53.0	58.9	62	68.2	1	85	17.7	111	90	10.4	1700
P 1.5KE62A	P 1.5KE62CA	5	53.0	58.9	62	65.1	1	85	17.7	111	90	10.4	1700
P 1.5KE68P	P 1.5KE68CP	5	58.1	64.6	68	74.8	1	92	16.3	121	83	10.4	1550
P 1.5KE68A	P 1.5KE68CA	5	58.1	64.6	68	71.4	1	92	16.3	121	83	10.4	1550
1.5KE75P	1.5KE75CP	5	64.1	71.3	75	82.5	1	103	14.6	134	75	10.5	1450
P 1.5KE75A	P 1.5KE75CA	5	64.1	71.3	75	78.8	1	103	14.6	134	75	10.5	1450
P 1.5KE82P	P 1.5KE82CP	5	70.1	77.9	82	90.2	1	113	13.3	146	69	10.5	1350
P 1.5KE82A	P 1.5KE82CA	5	70.1	77.9	82	86.1	1	113	13.3	146	69	10.5	1350
1.5KE91P	1.5KE91CP	5	77.8	86.5	91	100	1	125	12	162	62	10.6	1250
P 1.5KE91A	P 1.5KE91CA	5	77.8	86.5	91	95.5	1	125	12	162	62	10.6	1250
1.5KE100P	1.5KE100CP	5	85.5	95.0	100	110	1	137	11	178	56	10.6	1150
P 1.5KE100A	1.5KE100CA	5	85.5	95.0	100	105	1	137	11	178	56	10.6	1150
1.5KE110P	P 1.5KE110CP	5	94.0	105	110	121	1	152	9.9	195	51	10.7	1050
1.5KE110A	1.5KE110CA	5	94.0	105	110	116	1	152	9.9	195	51	10.7	1050
1.5KE120P	1.5KE120CP	5	102	114	120	132	1	165	9.1	212	47	10.7	1000
P 1.5KE120A	P 1.5KE120CA	5	102	114	120	126	1	165	9.1	212	47	10.7	1000
1.5KE130P	P 1.5KE130CP	5	111	124	130	143	1	179	8.4	230	43	10.7	950
P 1.5KE130A	P 1.5KE130CA	5	111	124	130	137	1	179	8.4	230	43	10.7	950
1.5KE150P	1.5KE150CP	5	128	143	150	165	1	207	7.2	265	38	10.8	850
P 1.5KE150A	P 1.5KE150CA	5	128	143	150	158	1	207	7.2	265	38	10.8	850
P 1.5KE160P	P 1.5KE160CP	5	136	152	160	176	1	219	6.8	282	35	10.8	800
P 1.5KE160A	P 1.5KE160CA	5	136	152	160	168	1	219	6.8	282	35	10.8	800
1.5KE170P	1.5KE170CP	5	145	161	170	187	1	234	6.4	301	33	10.8	750
P 1.5KE170A	1.5KE170CA	5	145	161	170	179	1	234	6.4	301	33	10.8	750
1.5KE180P	P 1.5KE180CP	5	154	171	180	198	1	246	6.1	317	31.5	10.8	725
P 1.5KE180A	P 1.5KE180CA	5	154	171	180	189	1	246	6.1	317	31.5	10.8	725
P 1.5KE200P	P 1.5KE200CP	5	171	190	200	220	1	274	5.5	353	28	10.8	675
P 1.5KE200A	P 1.5KE200CA	5	171	190	200	210	1	274	5.5	353	28	10.8	675
1.5KE220P	P 1.5KE220CP	5	188	209	220	242	1	328	4.6	388	26	10.8	625
P 1.5KE220A	P 1.5KE220CA	5	188	209	220	231	1	328	4.6	388	26	10.8	625
P 1.5KE250P	P 1.5KE250CP	5	213	237	250	275	1	344	5.0	442	23	11	560
P 1.5KE250A	P 1.5KE250CA	5	213	237	250	263	1	344	5.0	442	23	11	560
1.5KE280P	1.5KE280CP	5	239	266	280	308	1	384	5.0	494	20	11	520
1.5KE280A	1.5KE280CA	5	239	266	280	294	1	384	5.0	494	20	11	520

P = Prefered device

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
1.5KE300P	P 1.5KE300CP	5	256	285	300	330	1	414	5.0	529	19	11	500
P 1.5KE300A	1.5KE300CA	5	256	285	300	315	1	414	5.0	529	19	11	500
1.5KE320P	1.5KE320CP	5	273	304	320	352	1	438	4.5	564	18	11	460
P 1.5KE320A	1.5KE320CA	5	273	304	320	336	1	438	4.5	564	18	11	460
P 1.5KE350P	P 1.5KE350CP	5	299	332	350	385	1	482	4.0	618	16	11	430
1.5KE350A	1.5KE350CA	5	299	332	350	368	1	482	4.0	618	16	11	430
P 1.5KE400P	P 1.5KE400CP	5	342	380	400	440	1	548	4.0	706	14	11	390
1.5KE400A	1.5KE400CA	5	342	380	400	420	1	548	4.0	706	14	11	390
P 1.5KE440P	P 1.5KE440CP	5	376	418	440	484	1	603	3.5	776	13	11	360
1.5KE440A	1.5KE440CA	5	376	418	440	462	1	603	3.5	776	13	11	360

All parameters tested at 25 °C, except where indicated.

P = Prefered device



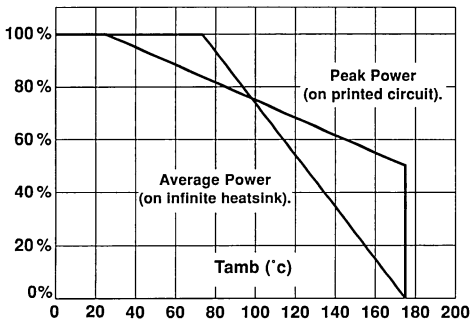


Figure 1: Power dissipation derating versus ambient temperature

Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Note 2 : Pulse test· $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.

Figure 2 : Peak pulse power versus exponential pulse duration.

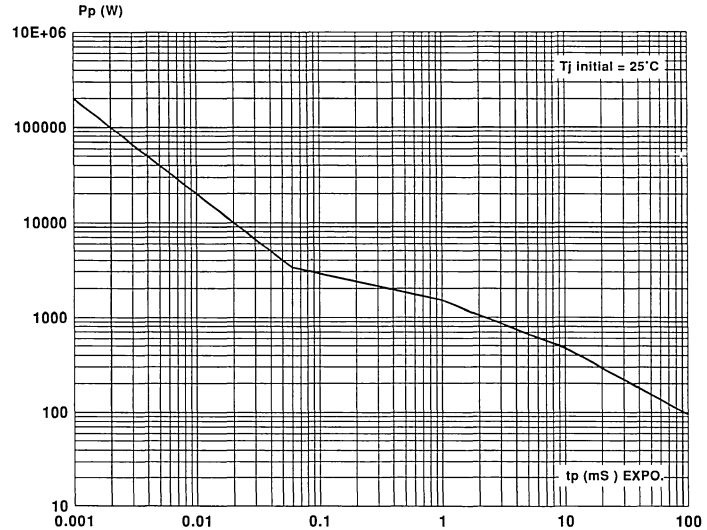
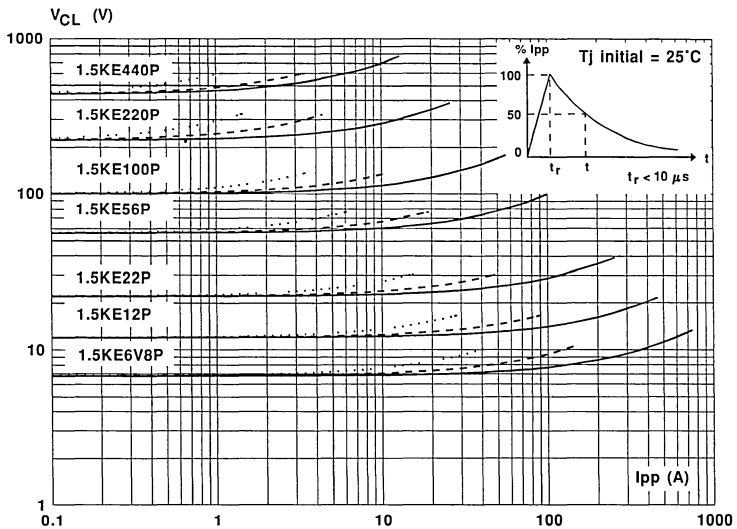


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} \cdot [T_a - 25] \cdot V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

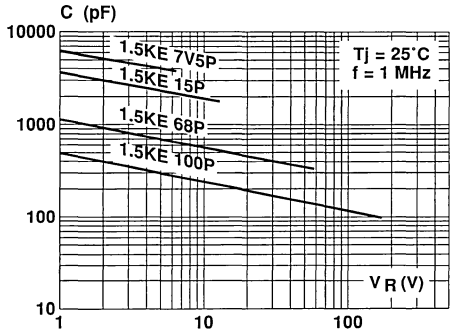


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

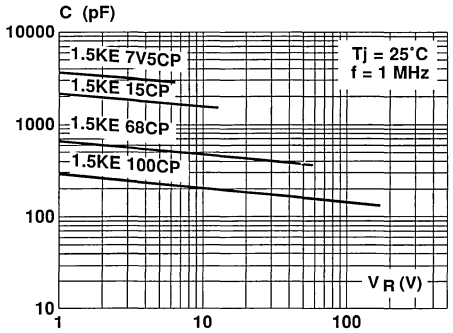


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

Note : For units with $V_{BR} > 200$ V
V_F is twice than shown.

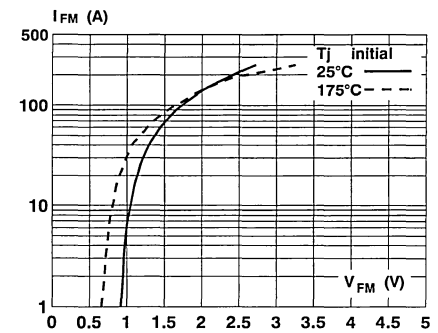
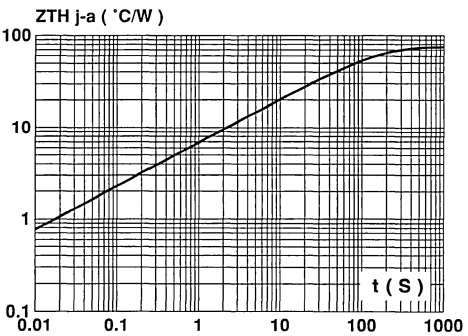
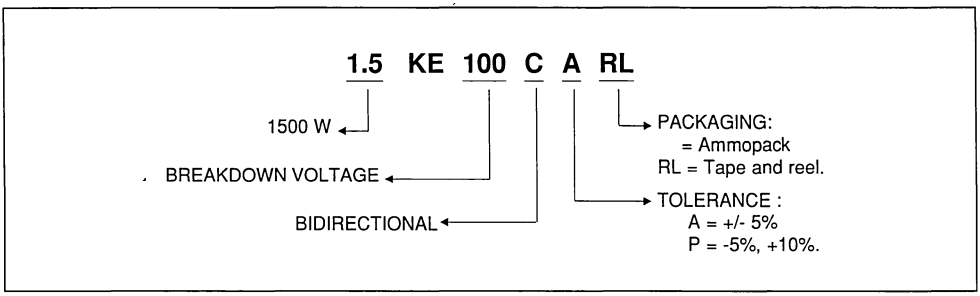


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with L_{lead} = 10mm.



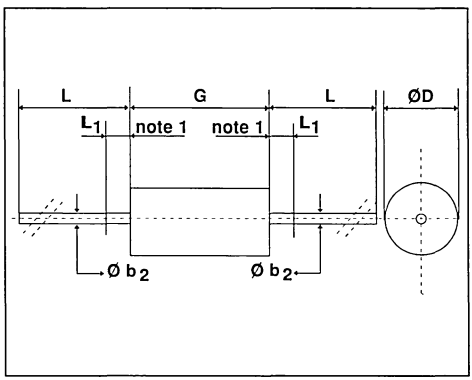
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

CB429



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	-	1.06	-	0.042
Ø D	-	5.1	-	0.20
G	-	9.8	-	0.386
L	26	-	1.024	-
L_1	-	1.27	-	0.050

note1:The diameter Ø b_2 is not controlled over zone L_1

Weight = 0.85 g.

Packaging : standard packaging is in tape and reel.

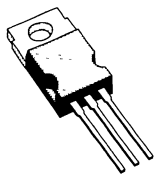
SGS-THOMSON MICROELECTRONICS

BDW93/A/B/C
BDW94/A/B/C

NPN/PNP POWER DARLINGTONS

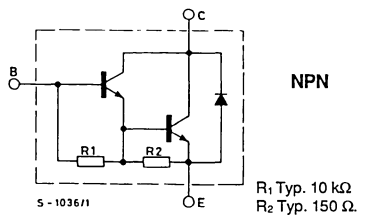
DESCRIPTION

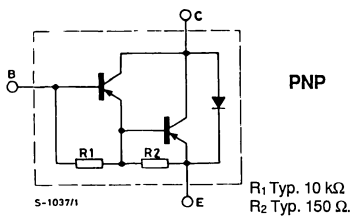
The BDW93, BDW93A, BDW93B and BDW93C are silicon epitaxial-base NPN transistors in monolithic Darlington configuration and are mounted in Jedec TO-220 plastic package. They are intended for use in power linear and switching applications. The complementary PNP types are the BDW94, BDW94A, BDW94B and BDW94C respectively.



TO-220

INTERNAL SCHEMATIC DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	NPN PNP*	Value				Unit
			BDW93 BDW94	BDW93A BDW94A	BDW93B BDW94B	BDW93C BDW94C	
V_{CBO}	Collector-base Voltage (I_E = 0)		45	60	80	100	V
V_{CEO}	Collector-emitter Voltage (I_B = 0)		45	60	80	100	V
I_C	Collector Current		12				A
I_{CM}	Collector Peak Current		15				A
I_B	Base Current		0.2				A
P_{tot}	Total Power Dissipation at $T_{case} \leq 25$ °C		80				W
T_{stg}	Storage Temperature		– 65 to 150				°C
T_j	Junction Temperature		150				°C

* For PNP types voltage and current values are negative.

THERMAL DATA

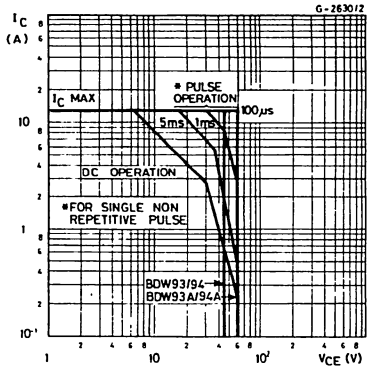
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	1.56	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

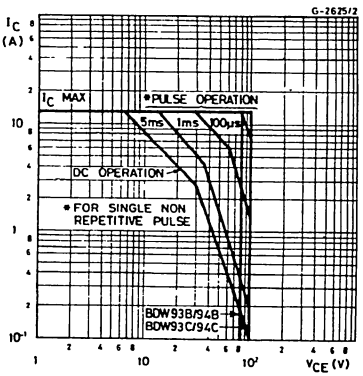
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cutoff Current (I_E = 0)	for **BDW93/94** V_{CB} = 45 V			100	µA
		for **BDW93A/94A** V_{CB} = 60 V			100	µA
		for **BDW93B/94B** V_{CB} = 80 V			100	µA
		for **BDW93C/94C** V_{CB} = 100 V			100	µA
		T_{case} = 150 °C				
		for **BDW93/94** V_{CB} = 45 V			5	mA
		for **BDW93A/94A** V_{CB} = 60 V			5	mA
		for **BDW93B/94B** V_{CB} = 80 V			5	mA
		for **BDW93C/94C** V_{CB} = 100 V			5	mA
I_{CEO}	Collector Cutoff Current (I_B = 0)	for **BDW93/94** V_{CE} = 40 V			1	mA
		for **BDW93A/94A** V_{CE} = 60 V			1	mA
		for **BDW93B/94B** V_{CE} = 80 V			1	mA
		for **BDW93C/94C** V_{CE} = 80 V			1	mA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{EB} = 5 V			2	mA
$V_{CEO(sus)}$*	Collector-emitter Sustaining Voltage (I_B = 0)	I_C = 100 mA for **BDW93/94**	45			V
		for **BDW93A/94A**	60			V
		for **BDW93B/94B**	80			V
		for **BDW93C/94C**	100			V
$V_{CE(sat)}$*	Collector-emitter Saturation Voltage	I_C = 5 A I_B = 20 mA			2	V
		I_C = 10 A I_B = 100 mA			3	V
$V_{BE(sat)}$*	Base-emitter Saturation Voltage	I_C = 5 A I_B = 20 mA			2.5	V
		I_C = 10 A I_B = 100 mA			4	V
h_{FE}*	DC Current Gain	I_C = 3 A V_{CE} = 3 V	1000			
		I_C = 5 A V_{CE} = 3 V	750		20000	
		I_C = 10 A V_{CE} = 3 V	100			
V_F*	Parallel-diode Forward Voltage	I_F = 5 A		1.3	2	V
		I_F = 10 A		1.8	4	V
h_{fe}	Small Signal Current Gain	I_C = 1 A V_{CE} = 10 V f = 1 MHz	20			

* Pulsed : pulse duration = 300 µs, duty cycle = 1.5 %.
For PNP types voltage and current values are negative.

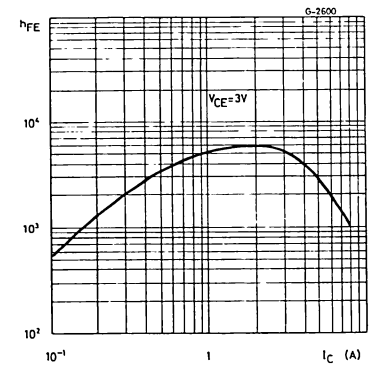
Safe Operating Areas (for **BDW93**, **BDW93A**, **BDW94**, **BDW94A**).



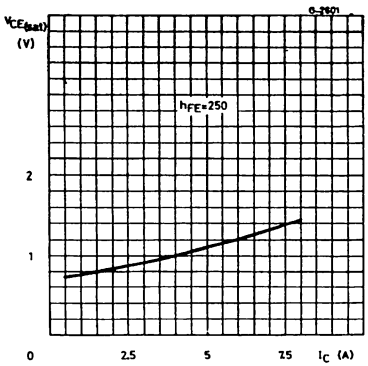
Safe Operating Areas (for **BDW93B**, **BDW93C**, **BDW94B**, **BDW94C**).



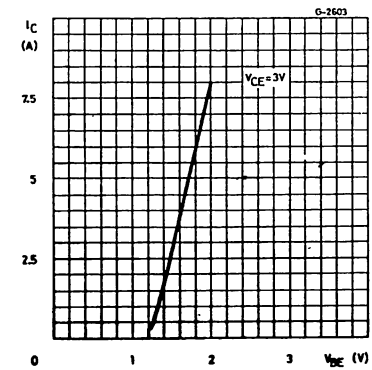
DC Current Gain (NPN types).



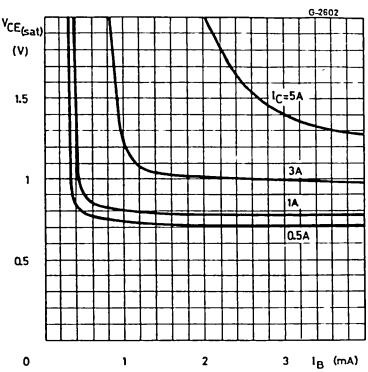
Collector-emitter Saturation Voltage (NPN types).



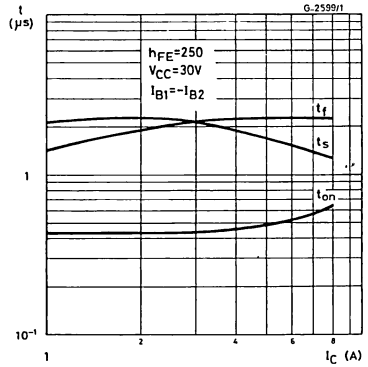
DC Transconductance (NPN types).



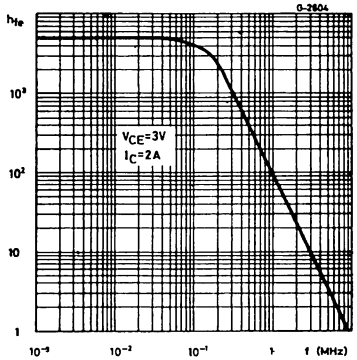
Collector-emitter Saturation Voltage (NPN types).



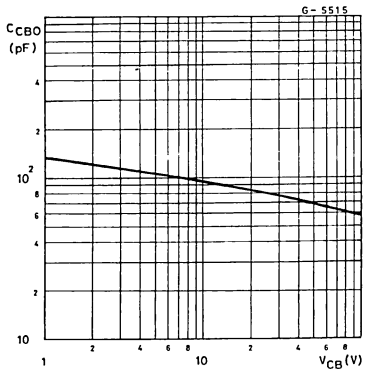
Saturated Switching Characteristics (NPN types).



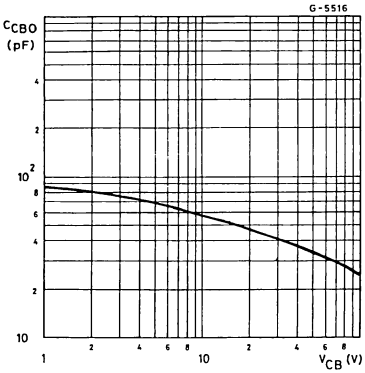
Small Signal Current Gain (NPN types).



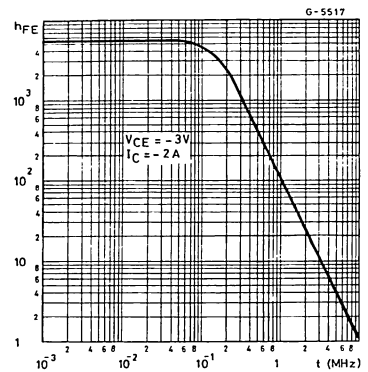
Collector-base Capacitance (PNP types).



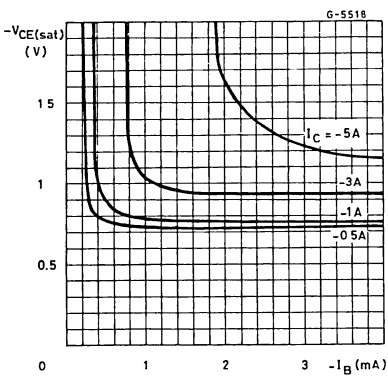
Collector-base Capacitance (NPN types).



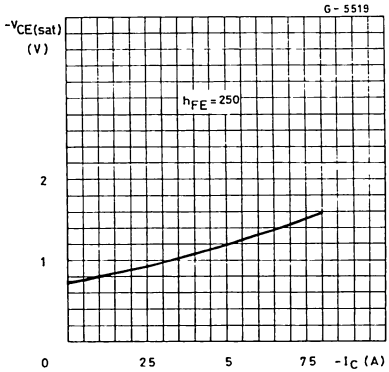
Small Signal Current Gain (PNP types).

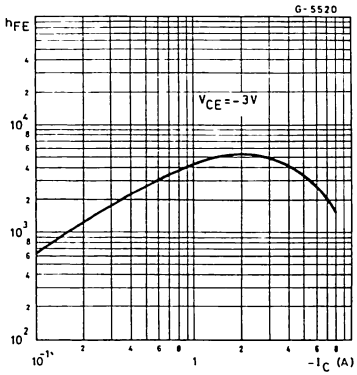


Collector-emitter Saturation Voltage (PNP types).

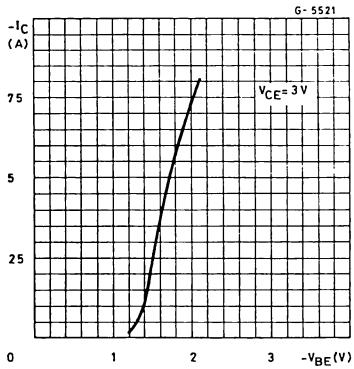


Collector-emitter Saturation Voltage (PNP types).

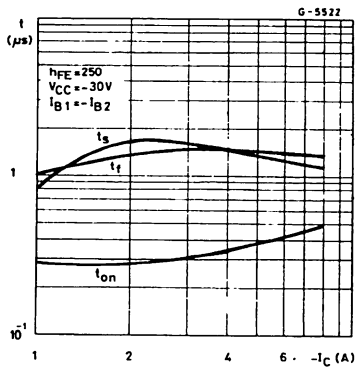




DC Transconductance (PNP types).



Saturated Switching Characteristics (PNP types).



SGS-THOMSON MICROELECTRONICS

BU931/BU931P BU931PFI

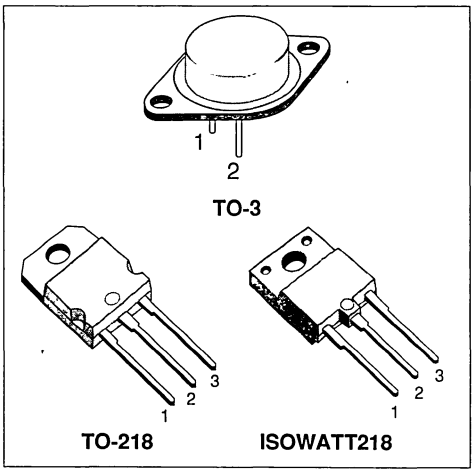
HIGH VOLTAGE IGNITION COIL DRIVER NPN POWER DARLINGTON

PRELIMINARY DATA

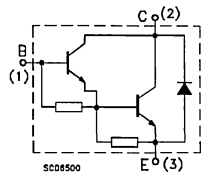
- VERY RUGGED BIPOLAR TECHNOLOGY
- HIGH OPERATING JUNCTION TEMPERATURE
- WIDE RANGE OF PACKAGES

APPLICATIONS

- HIGH RUGGEDNESS ELECTRONIC IGNITIONS



INTERNAL SCHEMATIC DIAGRAM



for **TO-3**
Emitter: pin 2
Base: pin 1
Collector: tab

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		BU931	BU931P	BU931PFI	
V_{CES}	Collector-Base Voltage (V_{BE} = 0)	450			V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	400			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	5			V
I_C	Collector Current	10			A
I_{CM}	Collector Peak Current	15			A
I_B	Base Current	1			A
I_{BM}	Base Peak Current	5			A
P_{tot}	Total Dissipation at T_c = 25 °C	175	150	55	W
T_{stg}	Storage Temperature	-65 to 200	-65 to 175	-65 to 150	°C
T_j	Max. Operating Junction Temperature	200	175	150	°C

THERMAL DATA

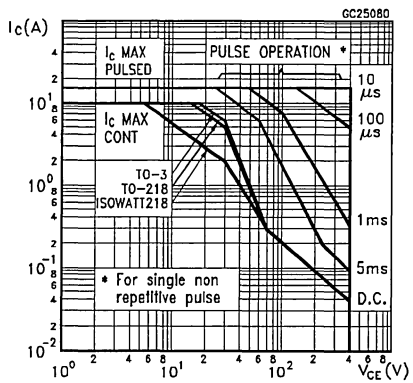
		TO-3	TO-218	ISOWATT218	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case Max	1	1	2.3	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

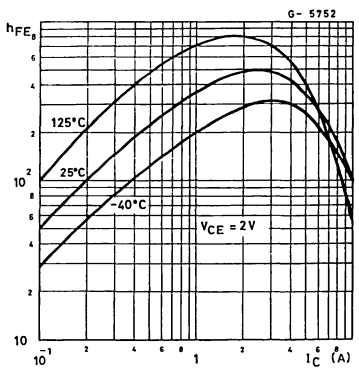
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 450 V V_{CE} = 450 V T_j = 150 °C			250 0.5	µA mA
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 400 V			250 0.5	µA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			20	mA
$V_{CEO(sus)}$*	Collector-Emitter Sustaining Voltage	I_C = 100 mA	400		500	V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 7 A I_B = 70 mA I_C = 8 A I_B = 100 mA I_C = 10 A I_B = 250 mA			1.6 1.8 1.8	V V V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 10 A I_B = 250 mA			2.5	V
h_{FE}*	DC Current Gain	I_C = 5 A V_{CE} = 10 V	300		2000	
V_F	Diode Forward Voltage	I_F = 10 A			2	V
	Functional Test (see fig. 1)	V_{CC} = 24 V V_{clamp} = 300 V L= 7 mH	8			A
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time (see fig. 3)	V_{CC} = 12 V V_{clamp} = 300 V L= 7 mH I_C = 7 A I_B = 70 mA V_{BE} = 0 R_{BE} = 47 Ω		15 0.5		µs µs

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

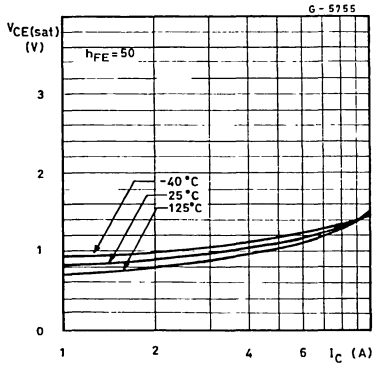
Safe Operating Areas



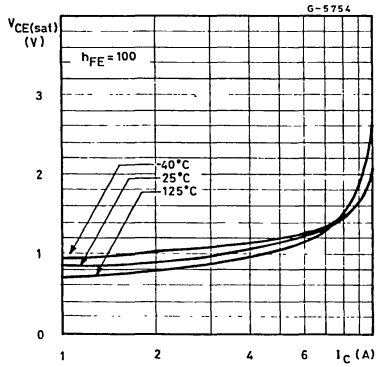
DC Current Gain



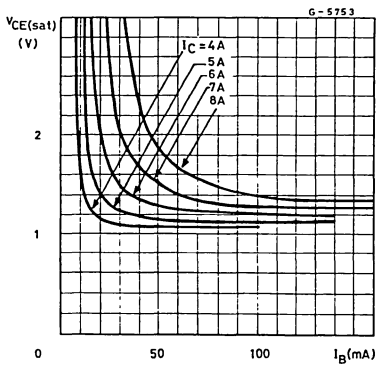
Collector-emitter Sturation Voltage



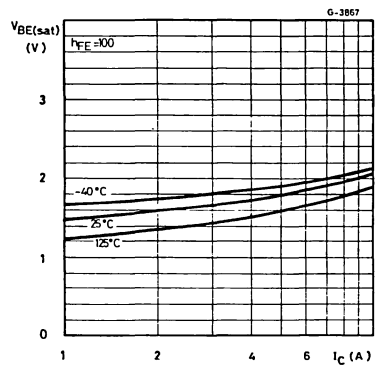
Collector-emitter Sturation Voltage



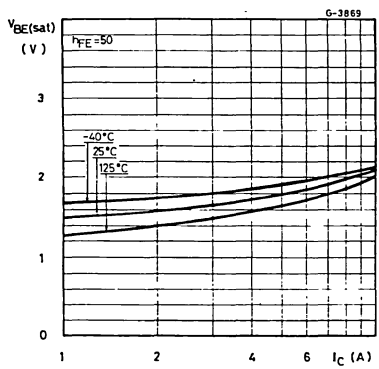
Collector-emitter Sturation Voltage



Base-emitter Sturation Voltage



Base-emitter Sturation Voltage



Switching Times Inductive Load

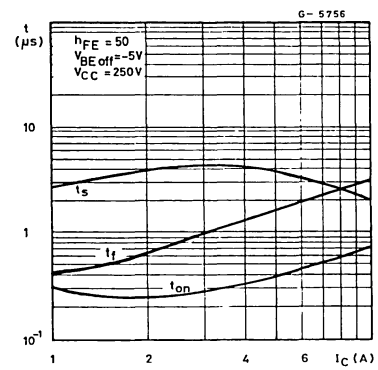


FIGURE 1: Functional Test Circuit

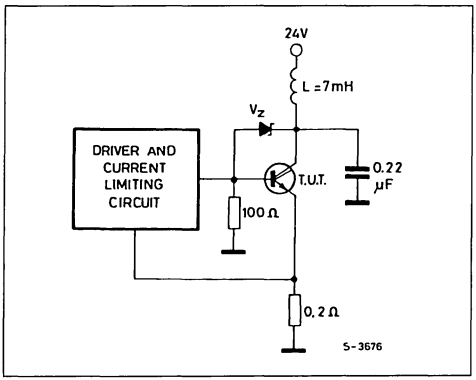


FIGURE 2: Functional Test Waveforms

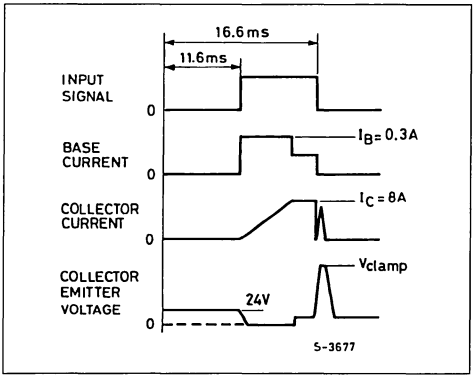
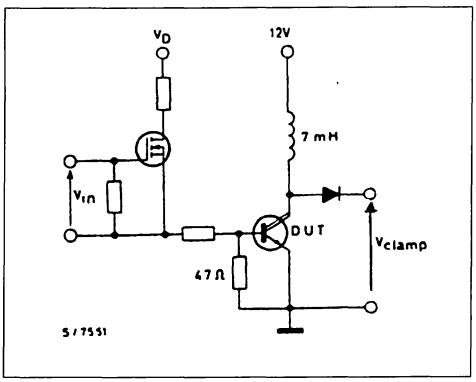


FIGURE 3: Switching Time Test Circuit



SGS-THOMSON MICROELECTRONICS

BU931T/BU931TFI BU931SM

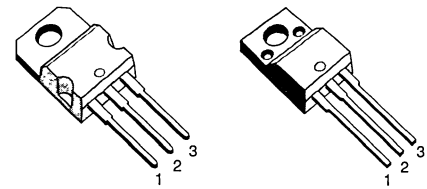
HIGH VOLTAGE IGNITION COIL DRIVER NPN POWER DARLINGTON

PRELIMINARY DATA

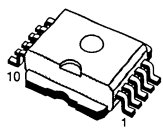
- VERY RUGGED BIPOLAR TECHNOLOGY
- HIGH OPERATING JUNCTION TEMPERATURE
- WIDE RANGE OF PACKAGES
- NEW REAL POWER SURFACE MOUNTING PACKAGE (Power SO-10)

APPLICATIONS

- HIGH RUGGEDNESS ELECTRONIC IGNITIONS

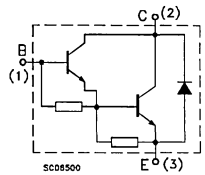


TO-220 **ISOWATT220**



Power SO-10

INTERNAL SCHEMATIC DIAGRAM



for **Power SO-10**
Emitter: pins 1 - 5
Base: pins 6 - 10
Collector: tab

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		BU931T	BU931TFI	BU931SM	
V_{CES}	Collector-Base Voltage (V_{BE} = 0)	450			V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	400			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	5			V
I_C	Collector Current	10			A
I_{CM}	Collector Peak Current	15			A
I_B	Base Current	1			A
I_{BM}	Base Peak Current	5			A
P_{tot}	Total Dissipation at T_c = 25 °C	125	40	125	W
T_{stg}	Storage Temperature	-65 to 175	-65 to 150	-65 to 175	°C
T_j	Max. Operating Junction Temperature	175	150	175	°C

THERMAL DATA

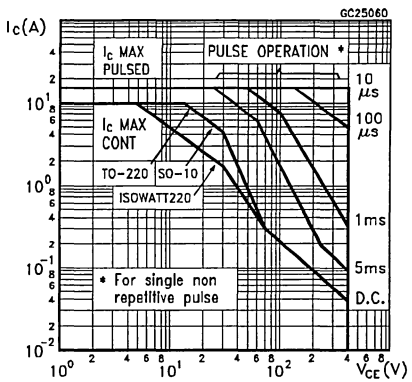
		TO-220	ISOWATT220	PowerSO-10	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case Max	1.2	3.12	1.2	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

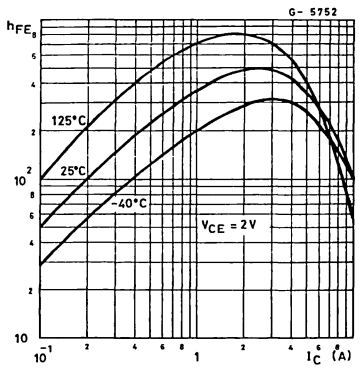
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 450 V V_{CE} = 450 V T_j = 150 °C			250 0.5	µA mA
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 400 V			250 0.5	µA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			20	mA
$V_{CEO(SUS)}$*	Collector-Emitter Saturation Voltage	I_C = 100 mA	400		500	V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 7 A I_B = 70 mA I_C = 8 A I_B = 100 mA I_C = 10 A I_B = 250 mA			1.6 1.8 1.8	V V V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 10 A I_B = 150 mA			2.5	V
h_{FE}*	DC Current Gain	I_C = 5 A V_{CE} = 10 V	300		2000	
V_F	Diode Forward Voltage	I_F = 10 A			2	V
	Functional Test (see fig. 1)	V_{CC} = 24 V V_{clamp} = 300 V L= 7 mH	8			A
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time (see fig. 3)	V_{CC} = 12 V V_{clamp} = 300 V L= 7 mH I_C = 7 A I_B = 70 mA V_{BE} = 0 R_{BE} = 47 Ω		15 0.5		µs µs

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

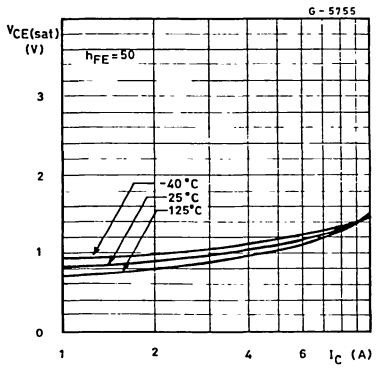
Safe Operating Areas



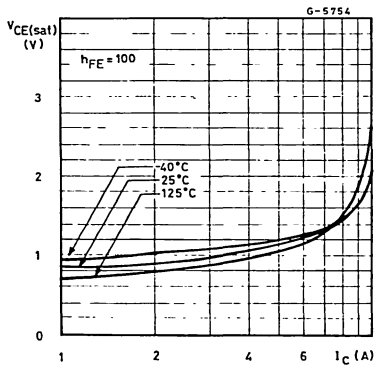
DC Current Gain



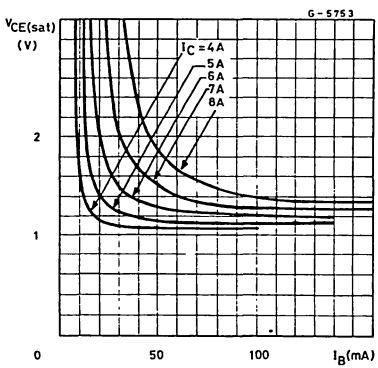
Collector-emitter Sturation Voltage



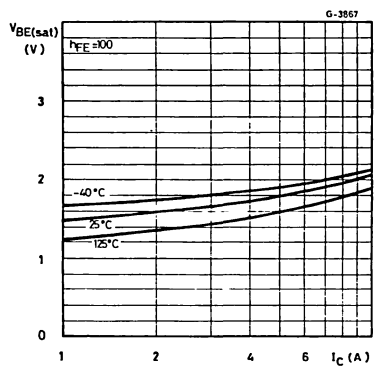
Collector-emitter Sturation Voltage



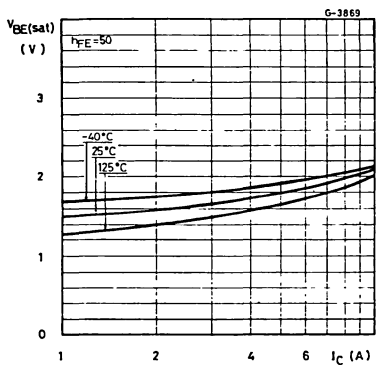
Collector-emitter Sturation Voltage



Base-emitter Sturation Voltage



Base-emitter Sturation Voltage



Switching Times Inductive Load

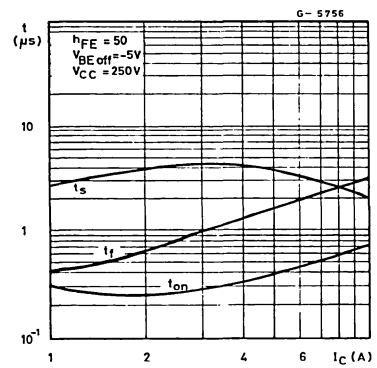


FIGURE 1: Functional Test Circuit

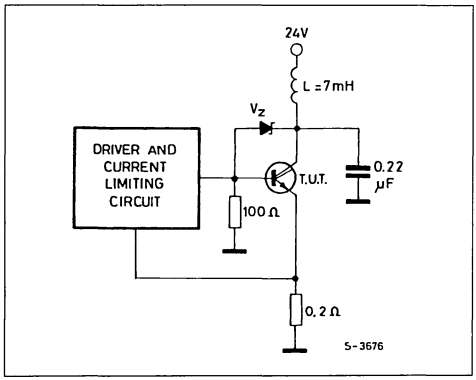


FIGURE 2: Functional Test Waveforms

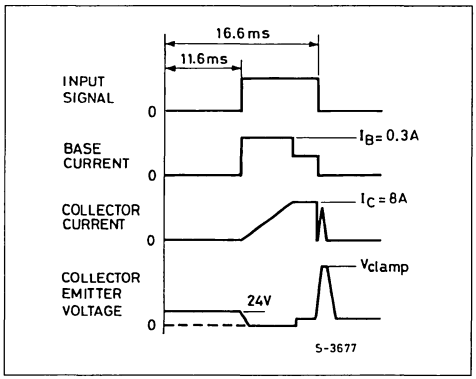
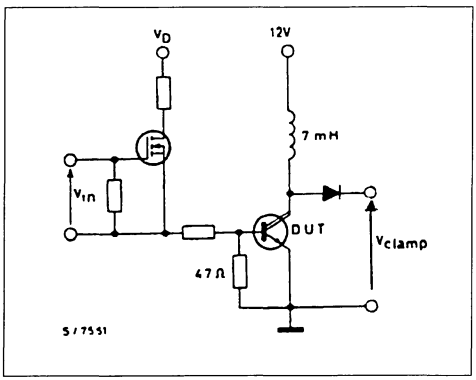


FIGURE 3: Switching Time Test Circuit



SGS-THOMSON MICROELECTRONICS

BU931Z/BU931ZP BU931ZPFI

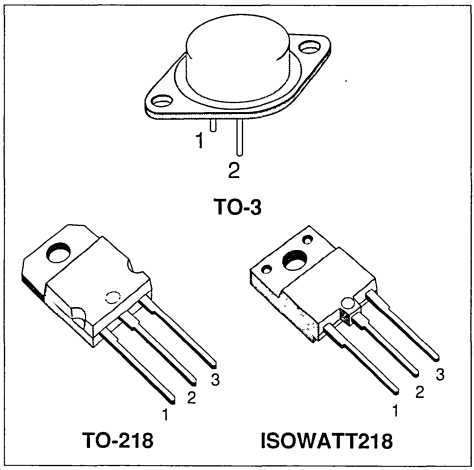
HIGH VOLTAGE IGNITION COIL DRIVER NPN POWER DARLINGTON

PRELIMINARY DATA

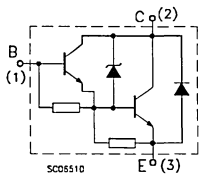
- VERY RUGGED BIPOLAR TECHNOLOGY
- BUILT IN CLAMPING ZENER
- HIGH OPERATING JUNCTION TEMPERATURE
- WIDE RANGE OF PACKAGES

APPLICATIONS

- HIGH RUGGEDNESS ELECTRONIC IGNITIONS



INTERNAL SCHEMATIC DIAGRAM



for **TO-3**
Emitter: pin 2
Base: pin 1
Collector: tab

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		BU931Z	BU931ZP	BU931ZPFI	
V_{CES}	Collector-Base Voltage (V_{BE} = 0)	350			V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	350			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	5			V
I_C	Collector Current	10			A
I_{CM}	Collector Peak Current	15			A
I_B	Base Current	1			A
I_{BM}	Base Peak Current	5			A
P_{tot}	Total Dissipation at T_c = 25 °C	175	150	60	W
T_{stg}	Storage Temperature	-65 to 200	-65 to 175	-65 to 150	°C
T_j	Max. Operating Junction Temperature	200	175	150	°C

THERMAL DATA

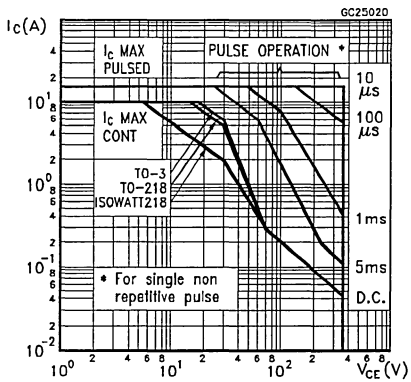
		TO-3	TO-218	ISOWATT218	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case Max	1	1	2.8	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

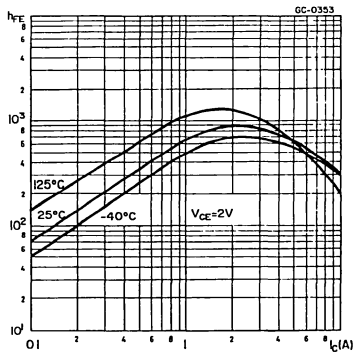
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 450 V V_{CE} = 450 V T_j = 150 °C			250 0.5	µA mA
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 400 V			250 0.5	µA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			20	mA
V_{CL}*	Clamping Voltage	I_C = 100 mA	350		500	V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 7 A I_B = 70 mA I_C = 8 A I_B = 100 mA I_C = 10 A I_B = 250 mA			1.6 1.8 1.8	V V V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 10 A I_B = 250 mA			2.5	V
h_{FE}*	DC Current Gain	I_C = 5 A V_{CE} = 10 V	300		2000	
V_F	Diode Forward Voltage	I_F = 10 A			2	V
	Functional Test (see fig. 1)	V_{CC} = 24 V L= 7 mH	8			A
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time (see fig. 3)	V_{CC} = 12 V L= 7 mH V_{clamp} = 300 V I_C = 7 A I_B = 70 mA V_{BE} = 0 R_{BE} = 47 Ω		15 0.5		µs µs

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

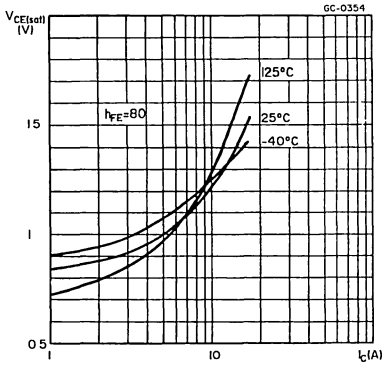
Safe Operating Areas



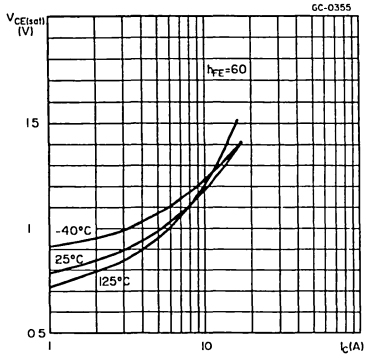
DC Current Gain



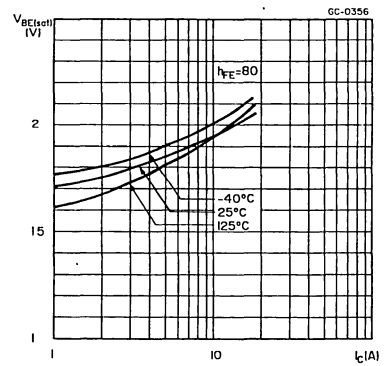
Collector-emitter Saturation Voltage



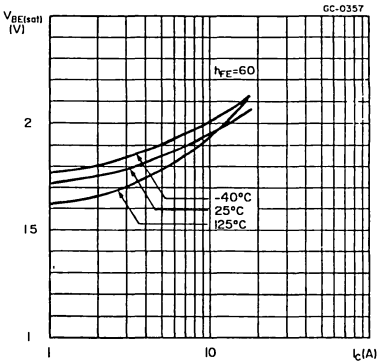
Collector-emitter Saturation Voltage



Base-emitter Saturation Voltage



Base-emitter Saturation Voltage



Collector-emitter Saturation Voltage

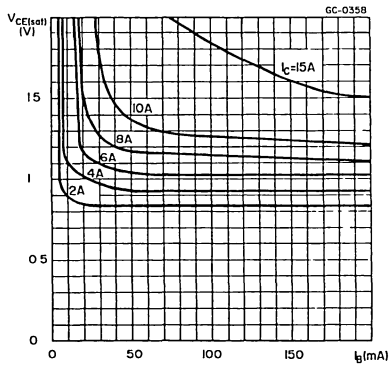


FIGURE 1: Functional Test Circuit

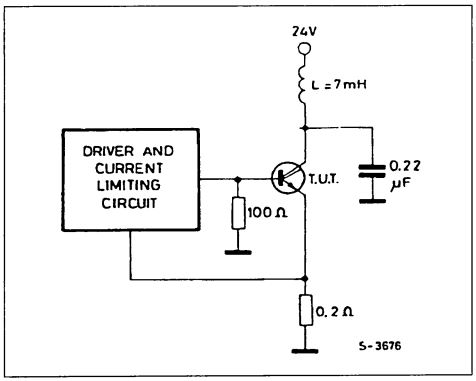


FIGURE 2: Functional Test Waveform

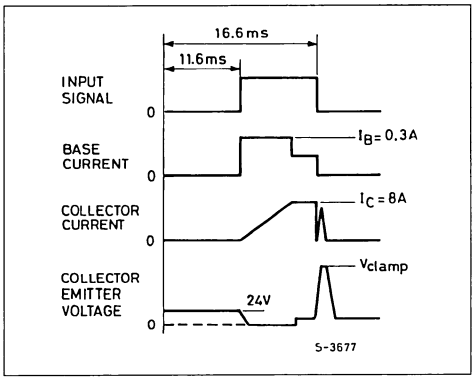
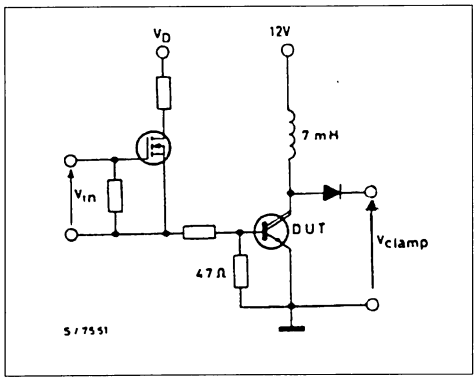


FIGURE 3: Switching Time Test Circuit



SGS-THOMSON MICROELECTRONICS

BU931ZT/BU931ZTFI BU931ZSM

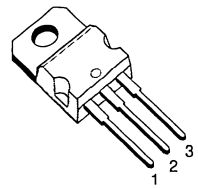
HIGH VOLTAGE IGNITION COIL DRIVER NPN POWER DARLINGTON

PRELIMINARY DATA

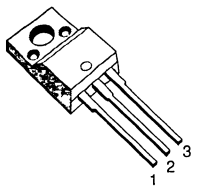
- VERY RUGGED BIPOLAR TECHNOLOGY
- BUILT IN CLAMPING ZENER
- HIGH OPERATING JUNCTION TEMPERATURE
- WIDE RANGE OF PACKAGES
- NEW REAL POWER SURFACE MOUNTING PACKAGE (Power SO-10)

APPLICATIONS

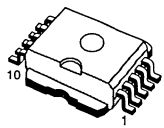
- HIGH RUGGEDNESS ELECTRONIC IGNITIONS



TO-220

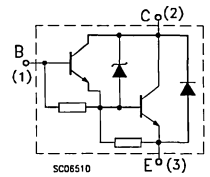


ISOWATT220



Power SO-10

INTERNAL SCHEMATIC DIAGRAM



for **Power SO-10**
Emitter: pins 1 - 5
Base: pins 6 - 10
Collector: tab

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		BU931ZT	BU931ZTFI	BU931ZSM	
V_{CES}	Collector-Base Voltage (V_{BE} = 0)	350			V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	350			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	5			V
I_C	Collector Current	10			A
I_{CM}	Collector Peak Current	15			A
I_B	Base Current	1			A
I_{BM}	Base Peak Current	5			A
P_{tot}	Total Dissipation at T_c = 25 °C	125	40	125	W
T_{stg}	Storage Temperature	-65 to 175	-65 to 150	-65 to 175	°C
T_j	Max. Operating Junction Temperature	175	150	175	°C

THERMAL DATA

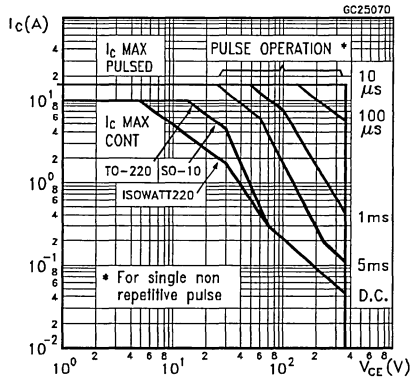
		TO-220	ISOWATT220	PowerSO-10	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case Max	1.2	3.12	1.2	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

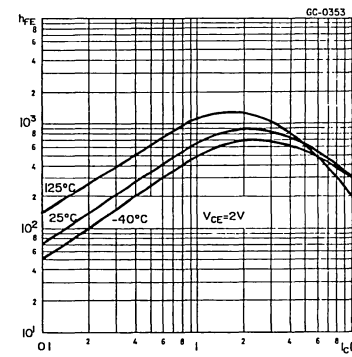
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 450 V V_{CE} = 450 V T_j = 150 °C			250 0.5	µA mA
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 400 V			250 0.5	µA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			20	mA
V_{CL}*	Clamping Voltage	I_C = 100 mA	350		500	V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 7 A I_B = 70 mA I_C = 8 A I_B = 100 mA I_C = 10 A I_B = 250 mA			1.6 1.8 1.8	V V V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 10 A I_B = 150 mA			2.5	V
h_{FE}*	DC Current Gain	I_C = 5 A V_{CE} = 10 V	300		2000	
V_F	Diode Forward Voltage	I_F = 10 A			2	V
	Functional Test (see fig. 1)	V_{CC} = 24 V L= 7 mH	8			A
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time (see fig. 3)	V_{CC} = 12 V L= 7 mH V_{clamp} = 300 V I_C = 7 A I_B = 70 mA V_{BE} = 0 R_{BE} = 47 Ω		15 0.5		µs µs

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

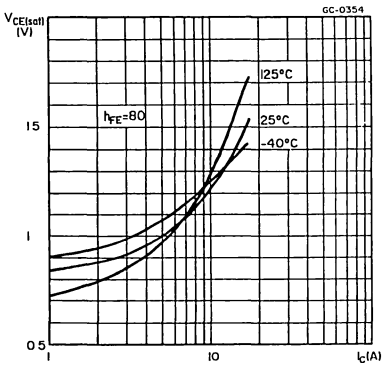
Safe Operating Areas



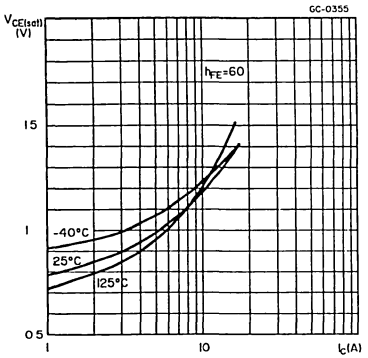
DC Current Gain



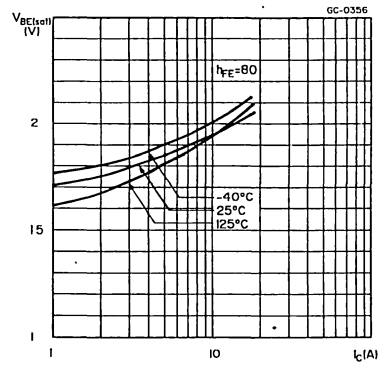
Collector-emitter Saturation Voltage



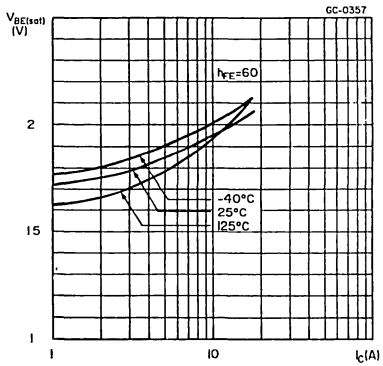
Collector-emitter Saturation Voltage



Base-emitter Saturation Voltage



Base-emitter Saturation Voltage



Collector-emitter Saturation Voltage

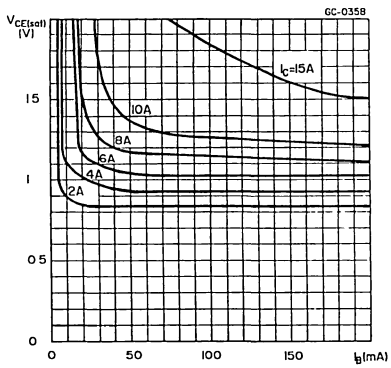


FIGURE 1: Functional Test Circuit

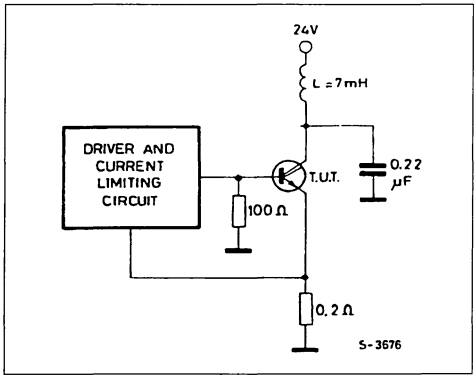


FIGURE 2: Functional Test Waveform

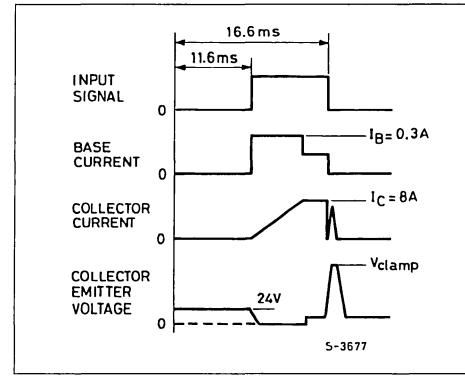
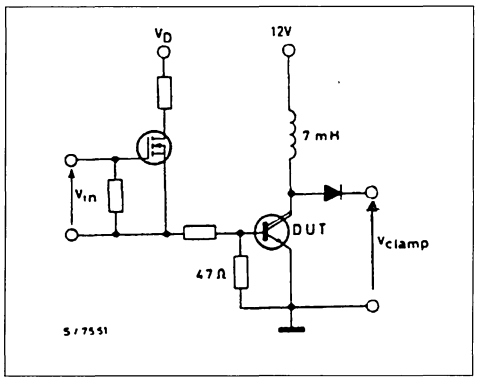


FIGURE 3: Switching Time Test Circuit



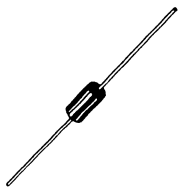
SGS-THOMSON MICROELECTRONICS

BZW04-5V8,B/376,B
BZW04P5V8,B/376,B

TRANSIL

FEATURES

- PEAK PULSE POWER= 400 W @ 1ms.
- STAND-OFF VOLTAGE RANGE : From 5V8 to 376 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).
- UL RECOGNIZED.



F126
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

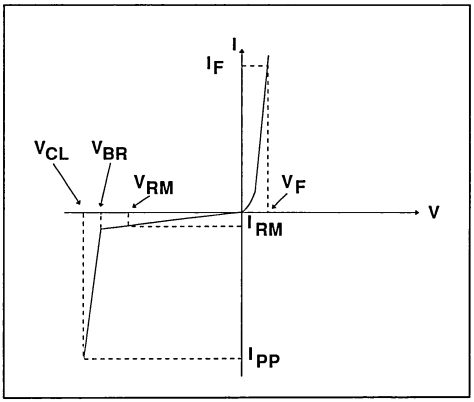
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	400	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	1.7	W
I_{FSM}	Non repetitive surge peak forward current For Unidirectional types	Tamb = 25°C t =10 ms	50	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 175	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	60	°C/W
R_{th} (j-a)	Junction to ambiant. on printed circuit. L_{lead} = 10 mm	100	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 25 A.



TYPES		I_{RM} @ V_{RM}		V_{BR} @ I_R				V_{CL} @ I_{PP}		V_{CL} @ I_{PP}		αT	C
		max		min	nom	max		max		max		max	typ
						note2		10/1000µs		8/20µs		note3	note4
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
P BZW04P5V8	P BZW04P5V8B	1000	5.8	6.45	6.8	7.48	10	10.5	38	13.4	174	5.7	3500
BZW04-5V8	BZW04-5V8B	1000	5.8	6.45	6.8	7.14	10	10.5	38	13.4	174	5.7	3500
BZW04P6V4	P BZW04P6V4B	500	6.4	7.13	7.5	8.25	10	11.3	35.4	14.5	160	6.1	3100
BZW04-6V4	BZW04-6V4B	500	6.4	7.13	7.5	7.88	10	11.3	35.4	14.5	160	6.1	3100
BZW04P7V0	BZW04P7V0B	200	7.02	7.79	8.2	9.02	10	12.1	33	15.5	148	6.5	2700
BZW04-7V0	BZW04-7V0B	200	7.02	7.79	8.2	8.61	10	12.1	33	15.5	148	6.5	2700
BZW04P7V8	BZW04P7V8B	50	7.78	8.65	9.1	10	1	13.4	30	17.1	134	6.8	2300
BZW04-7V8	BZW04-7V8B	50	7.78	8.65	9.1	9.55	1	13.4	30	17.1	134	6.8	2300
BZW04P8V5	BZW04P8V5B	10	8.55	9.5	10	11	1	14.5	27.6	18.6	124	7.3	2000
BZW04-8V5	BZW04-8V5B	10	8.55	9.5	10	10.5	1	14.5	27.6	18.6	124	7.3	2000
P BZW04P9V4	BZW04P9V4B	5	9.4	10.5	11	12.1	1	15.6	25.7	20.3	113	7.5	1750
BZW04-9V4	BZW04-9V4B	5	9.4	10.5	11	11.6	1	15.6	25.7	20.3	113	7.5	1750
P BZW04P10	P BZW04P10B	5	10.2	11.4	12	13.2	1	16.7	24	21.7	106	7.8	1550
BZW04-10	BZW04-10B	5	10.2	11.4	12	12.6	1	16.7	24	21.7	106	7.8	1550
P BZW04P11	P BZW04P11B	5	11.1	12.4	13	14.3	1	18.2	22	23.6	97	8.1	1450
BZW04-11	BZW04-11B	5	11.1	12.4	13	13.7	1	18.2	22	23.6	97	8.1	1450
P BZW04P13	P BZW04P13B	5	12.8	14.3	15	16.5	1	21.2	19	27.2	85	8.4	1200
P BZW04-13	P BZW04-13B	5	12.8	14.3	15	15.8	1	21.2	19	27.2	85	8.4	1200
P BZW04P14	BZW04P14B	5	13.6	15.2	16	17.6	1	22.5	17.8	28.9	80	8.6	1100
BZW04-14	BZW04-14B	5	13.6	15.2	16	16.8	1	22.5	17.8	28.9	80	8.6	1100
P BZW04P15	P BZW04P15B	5	15.3	17.1	18	19.8	1	25.2	16	32.5	71	8.8	975
P BZW04-15	P BZW04-15B	5	15.3	17.1	18	18.9	1	25.2	16	32.5	71	8.8	975
BZW04P17	BZW04P17B	5	17.1	19	20	22	1	27.7	14.5	36.1	64	9.0	850
BZW04-17	BZW04-17B	5	17.1	19	20	21	1	27.7	14.5	36.1	64	9.0	850
BZW04P19	P BZW04P19B	5	18.8	20.9	22	24.2	1	30.6	13	39.3	59	9.2	800

P = Prevered device

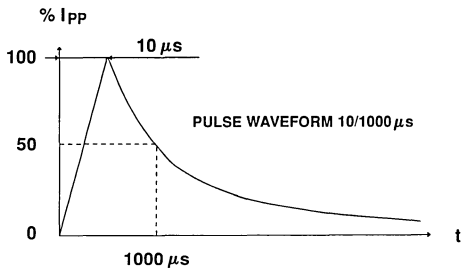
TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
BZW04-19	BZW04-19B	5	18.8	20.9	22	23.1	1	30.6	13	39.3	59	9.2	800
BZW04P20	P BZW04P20B	5	20.5	22.8	24	26.4	1	33.2	12	42.8	54	9.4	725
BZW04-20	BZW04-20B	5	20.5	22.8	24	25.2	1	33.2	12	42.8	54	9.4	725
BZW04P23	P BZW04P23B	5	23.1	25.7	27	29.7	1	37.5	10.7	48.3	48	9.6	625
BZW04-23	BZW04-23B	5	23.1	25.7	27	28.4	1	37.5	10.7	48.3	48	9.6	625
P BZW04P26	BZW04P26B	5	25.6	28.5	30	33	1	41.5	9.6	53.5	43	9.7	575
BZW04-26	BZW04-26B	5	25.6	28.5	30	31.5	1	41.5	9.6	53.5	43	9.7	575
P BZW04P28	P BZW04P28B	5	28.2	31.4	33	36.3	1	45.7	8.8	59.0	39	9.8	510
BZW04-28	BZW04-28B	5	28.2	31.4	33	34.7	1	45.7	8.8	59.0	39	9.8	510
BZW04P31	BZW04P31B	5	30.8	34.2	36	39.6	1	49.9	8	64.3	36	9.9	480
P BZW04-31	BZW04-31B	5	30.8	34.2	36	37.8	1	49.9	8	64.3	36	9.9	480
P BZW04P33	P BZW04P33B	5	33.3	37.1	39	42.9	1	53.9	7.4	69.7	33	10.0	450
P BZW04-33	BZW04-33B	5	33.3	37.1	39	41.0	1	53.9	7.4	69.7	33	10.0	450
BZW04P37	BZW04P37B	5	36.8	40.9	43	47.3	1	59.3	6.7	76.8	30	10.1	400
BZW04-37	P BZW04-37B	5	36.8	40.9	43	45.2	1	59.3	6.7	76.8	30	10.1	400
BZW04P40	BZW04P40B	5	40.2	44.7	47	51.7	1	64.8	6.2	84	27	10.1	370
BZW04-40	BZW04-40B	5	40.2	44.7	47	49.4	1	64.8	6.2	84	27	10.1	370
BZW04P44	BZW04P44B	5	43.6	48.5	51	56.1	1	70.1	5.7	91	25	10.2	350
BZW04-44	BZW04-44B	5	43.6	48.5	51	53.6	1	70.1	5.7	91	25	10.2	350
BZW04P48	P BZW04P48B	5	47.8	53.2	56	61.6	1	77	5.2	100	23	10.3	320
P BZW04-48	P BZW04-48B	5	47.8	53.2	56	58.8	1	77	5.2	100	23	10.3	320
BZW04P53	BZW04P53B	5	53.0	58.9	62	68.2	1	85	4.7	111	21	10.4	290
BZW04-53	BZW04-53B	5	53.0	58.9	62	65.1	1	85	4.7	111	21	10.4	290
P BZW04P58	P BZW04P58B	5	58.1	64.6	68	74.8	1	92	4.3	121	19	10.4	270
BZW04-58	BZW04-58B	5	58.1	64.6	68	71.4	1	92	4.3	121	19	10.4	270
BZW04P64	BZW04P64B	5	64.1	71.3	75	82.5	1	103	3.9	134	17	10.5	250
P BZW04-64	BZW04-64B	5	64.1	71.3	75	78.8	1	103	3.9	134	17	10.5	250
BZW04P70	BZW04P70B	5	70.1	77.9	82	90.2	1	113	3.5	146	16	10.5	230
BZW04-70	P BZW04-70B	5	70.1	77.9	82	86.1	1	113	3.5	146	16	10.5	230
BZW04P78	BZW04P78B	5	77.8	86.5	91	100	1	125	3.2	162	14	10.6	210
BZW04-78	BZW04-78B	5	77.8	86.5	91	95.5	1	125	3.2	162	14	10.6	210
P BZW04P85	P BZW04P85B	5	85.5	95.0	100	110	1	137	2.9	178	13	10.6	200
BZW04-85	BZW04-85B	5	85.5	95.0	100	105	1	137	2.9	178	13	10.6	200
BZW04P94	BZW04P94B	5	94.0	105	110	121	1	152	2.6	195	12	10.7	185
BZW04-94	BZW04-94B	5	94.0	105	110	116	1	152	2.6	195	12	10.7	185
BZW04P102	BZW04P102B	5	102	114	120	132	1	165	2.4	212	11	10.7	170
BZW04-102	BZW04-102B	5	102	114	120	126	1	165	2.4	212	11	10.7	170
BZW04P111	P BZW04P111B	5	111	124	130	143	1	179	2.2	230	10	10.7	165
BZW04-111	BZW04-111B	5	111	124	130	137	1	179	2.2	230	10	10.7	165
P BZW04P128	P BZW04P128B	5	128	143	150	165	1	207	2.0	265	9	10.8	145
BZW04-128	BZW04-128B	5	128	143	150	158	1	207	2.0	265	9	10.8	145
P BZW04P136	P BZW04P136B	5	136	152	160	176	1	219	1.8	282	8	10.8	140
P BZW04-136	P BZW04-136B	5	136	152	160	168	1	219	1.8	282	8	10.8	140
P BZW04P145	P BZW04P145B	5	145	161	170	187	1	234	1.7	301	7.5	10.8	135
BZW04-145	BZW04-145B	5	145	161	170	179	1	234	1.7	301	7.5	10.8	135
BZW04P154	BZW04P154B	5	154	171	180	198	1	246	1.6	317	7	10.8	125
BZW04-154	BZW04-154B	5	154	171	180	189	1	246	1.6	317	7	10.8	125
BZW04P171	BZW04P171B	5	171	190	200	220	1	274	1.5	353	6.5	10.8	120
BZW04-171	BZW04-171B	5	171	190	200	210	1	274	1.5	353	6.5	10.8	120
BZW04P188	P BZW04P188B	5	188	209	220	242	1	328	1.4	388	6	10.8	110
BZW04-188	BZW04-188B	5	188	209	220	231	1	328	1.4	388	6	10.8	110
BZW04P213	P BZW04P213B	5	213	237	250	275	1	344	1.5	442	5.2	11	100
BZW04-213	BZW04-213B	5	213	237	250	263	1	344	1.5	442	5.2	11	100
P BZW04P239	P BZW04P239B	5	239	266	280	308	1	384	1.5	494	4.6	11	95
BZW04-239	BZW04-239B	5	239	266	280	294	1	384	1.5	494	4.6	11	95

P = Prevered device

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
BZW04P256	BZW04P256B	5	256	285	300	330	1	414	1.2	529	4.3	11	90
BZW04-256	BZW04-256B	5	256	285	300	315	1	414	1.2	529	4.3	11	90
BZW04P273	BZW04P273B	5	273	304	320	352	1	438	1.2	564	4	11	85
BZW04-273	BZW04-273B	5	273	304	320	336	1	438	1.2	564	4	11	85
BZW04P299	P BZW04P299B	5	299	332	350	385	1	482	0.9	618	3.7	11	80
P BZW04-299	P BZW04-299B	5	299	332	350	368	1	482	0.9	618	3.7	11	80
BZW04P342	P BZW04P342B	5	342	380	400	440	1	548	0.9	706	3.2	11	75
BZW04-342	P BZW04-342B	5	342	380	400	420	1	548	0.9	706	3.2	11	75
P BZW04P376	P BZW04P376B	5	376	418	440	484	1	603	0.8	776	3	11	70
BZW04-376	P BZW04-376B	5	376	418	440	462	1	603	0.8	776	3	11	70

All parameters tested at 25 °C, except where indicated.

P = Prefered device



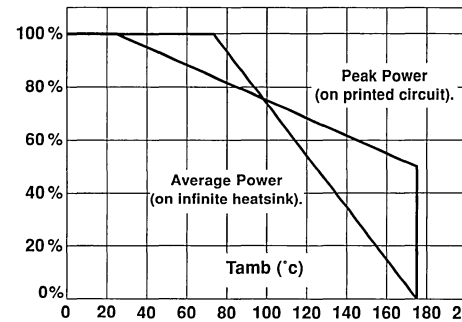


Figure 1: Power dissipation derating versus ambient temperature

Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Note 2 : Pulse test: $T_P < 50$ ms

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.

Note 4 : VR = 0 V, F = 1 MHz For bidirectional types, capacitance value is divided by 2.

Figure 2 : Peak pulse power versus exponential pulse duration.

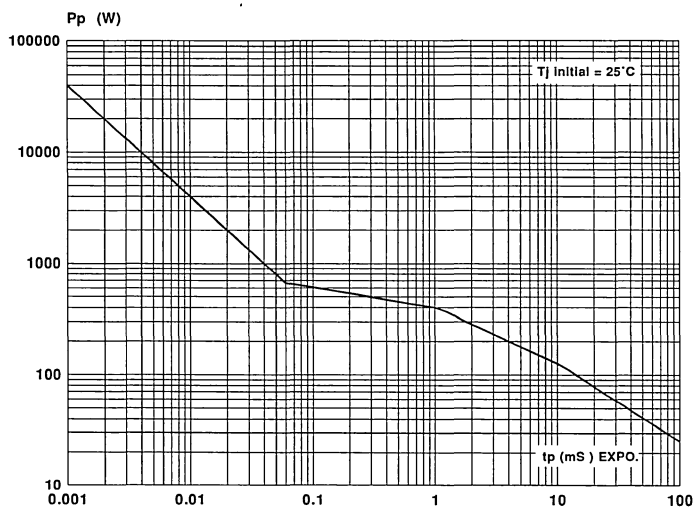
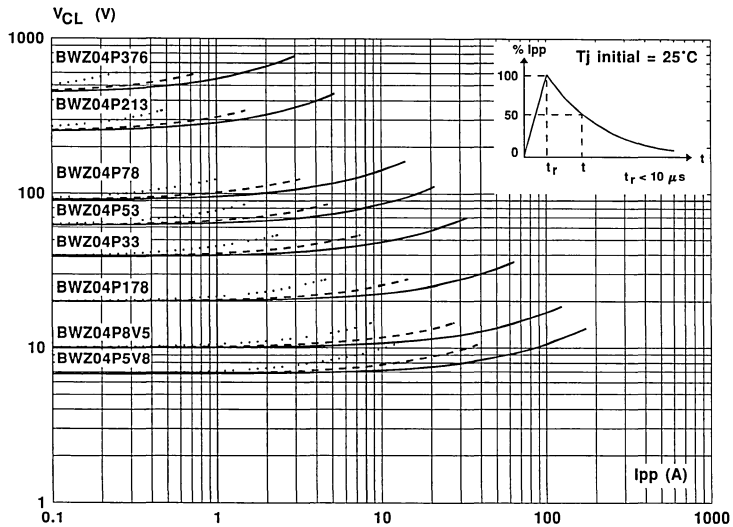


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} \cdot [T_a - 25] \cdot V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

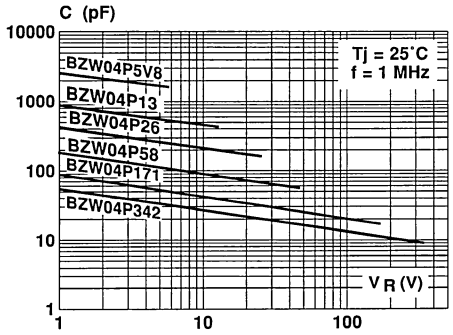


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

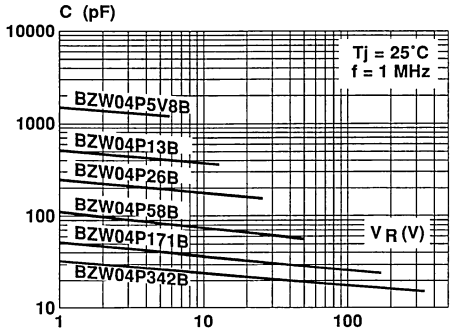


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

Note : For units with V_{BR} > 200 V
V_F is twice than shown.

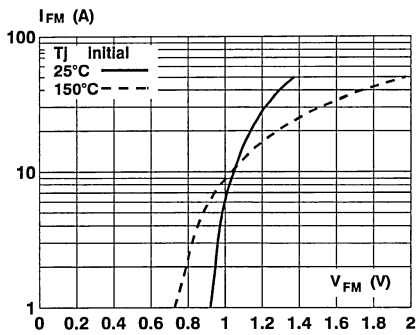
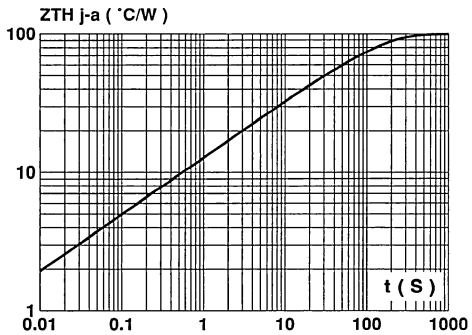
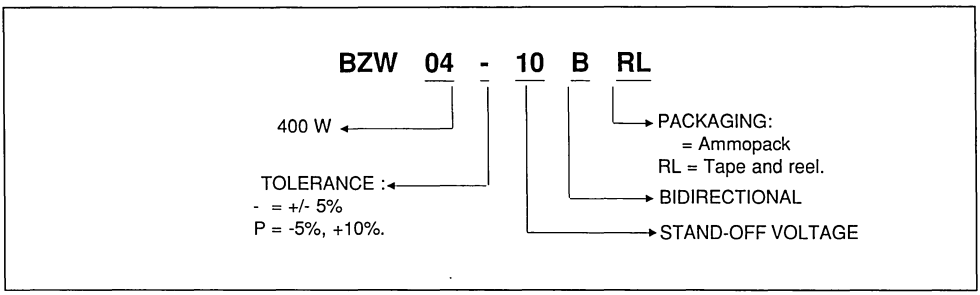


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with L_{lead} = 10mm.



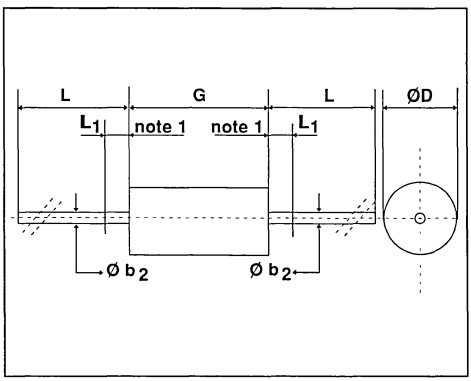
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

F 126 (Plastic).



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	0.76	0.86	0.029	0.034
Ø D	2.95	3.05	0.116	0.120
G	6.05	6.35	0.238	0.250
L	26	-	1.024	-
L_1	-	1.27	-	0.050

note1:The diameter Ø b_2 is not controlled over zone L_1

Weight = 0.4 g.

Packaging : standard packaging is in tape and reel.

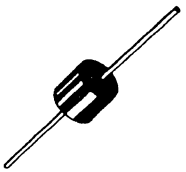
SGS-THOMSON MICROELECTRONICS

BZW50-10,B/180,B

TRANSIL

FEATURES

- PEAK PULSE POWER= 5000 W @ 1ms.
- STAND-OFF VOLTAGE RANGE : From 10V to 180 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).



AG
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

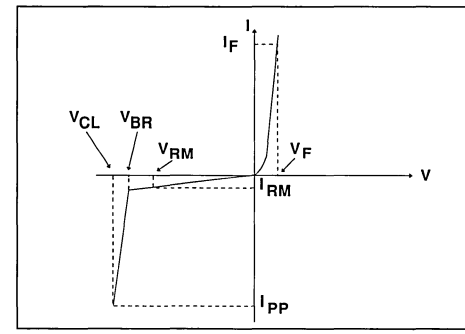
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	5000	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	6.5	W
I_{FSM}	Non repetitive surge peak forward current For Unidirectional types.	Tamb = 25°C t =10 ms	500	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 175	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	15	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. L_{lead} = 10 mm	65	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.



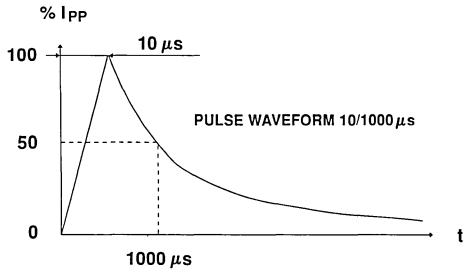
TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min	nom	max		V_{CL}@ I_{PP} max 10/1000µs		V_{CL}@ I_{PP} max 8/20µs		αT max note3	C typ note4
					note2								
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
BZW50-10	BZW50-10B	5	10	11.1	12.4	13.6	1	18.8	266	23.4	2564	7.8	24000
BZW50-12	BZW50-12B	5	12	13.3	14.8	16.3	1	22	227	28	2143	8.4	18500
BZW50-15	BZW50-15B	5	15	16.6	18.5	20.4	1	26.9	186	35	1714	8.8	13500
BZW50-18	BZW50-18B	5	18	20	22.2	24.4	1	32.2	155	41.5	1446	9.2	11500
BZW50-22	BZW50-22B	5	22	24.4	27.1	29.8	1	39.4	127	51	1177	9.6	8500
BZW50-27	BZW50-27B	5	27	30	33.3	36.6	1	48.3	103	62	968	9.8	7000
BZW50-33	BZW50-33B	5	33	36.6	40.7	44.7	1	59	85	76	789	1.0	5750
BZW50-39	BZW50-39B	5	39	43.3	48.1	53	1	69.4	72	90	667	10.1	4800
BZW50-47	BZW50-47B	5	47	52	57.8	63.6	1	83.2	60.1	108	556	10.3	4100
BZW50-56	BZW50-56B	5	56	62.2	69.1	76	1	99.6	50	129	465	10.4	3400
BZW50-68	BZW50-68B	5	68	75.6	84	92.4	1	121	41	157	382	10.5	3000
BZW50-82	BZW50-82B	5	82	91	101.2	111	1	145	34	189	317	10.6	2600
BZW50-100	BZW50-100B	5	100	111	123.5	136	1	179	28	228	263	10.7	2300
BZW50-120	BZW50-120B	5	120	133	148.1	163	1	215	23	274	219	10.8	1900
BZW50-150	BZW50-150B	5	150	166	185.2	204	1	269	19	343	175	10.8	1700
BZW50-180	BZW50-180B	5	180	200	222	244	1	322	16	410	146	10.8	1500

All parameters tested at 25 °C, except where indicated.

Note 2 : Pulse test: $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode

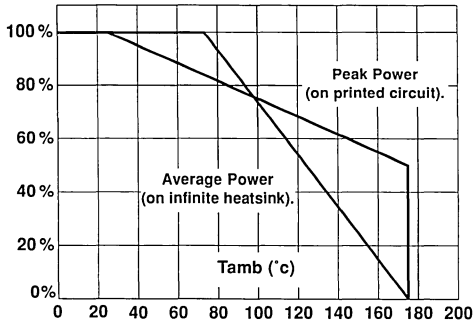


Figure 1: Power dissipation derating versus ambient temperature

Figure 2 : Peak pulse power versus exponential pulse duration.

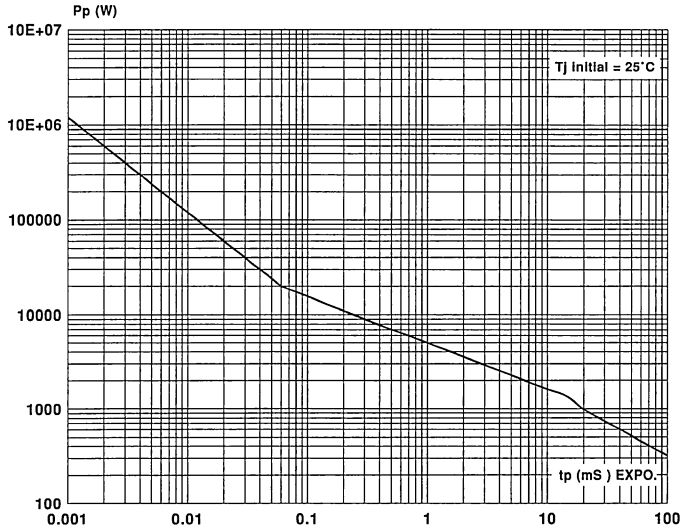
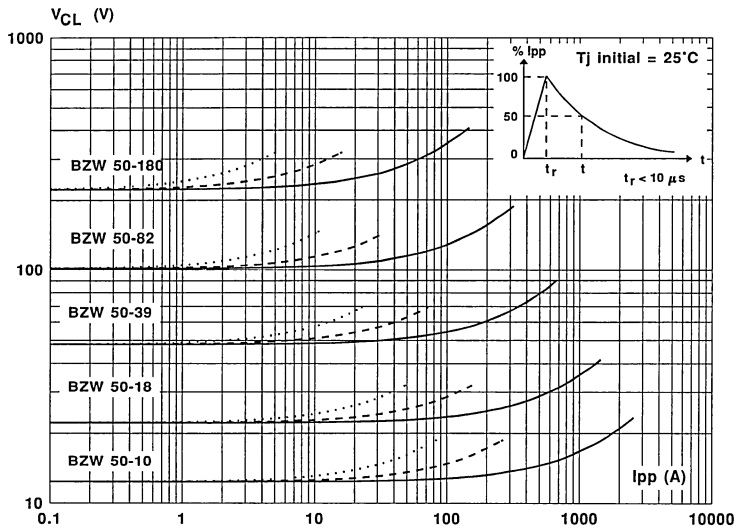


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} * [T_a - 25] * V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

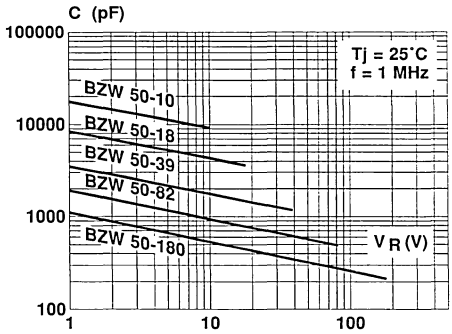


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

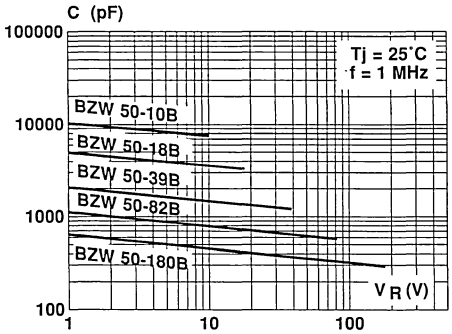


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

Note : For units with V_{BR} > 200 V
V_F is twice than shown.

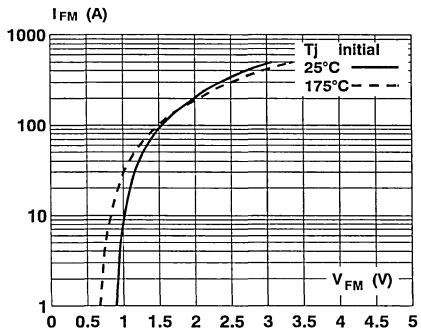
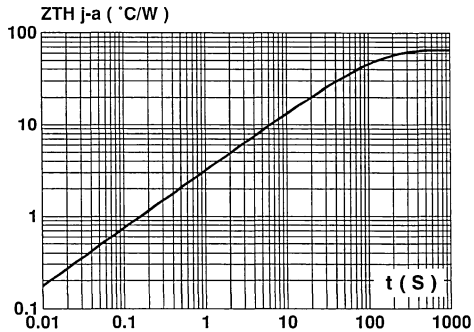
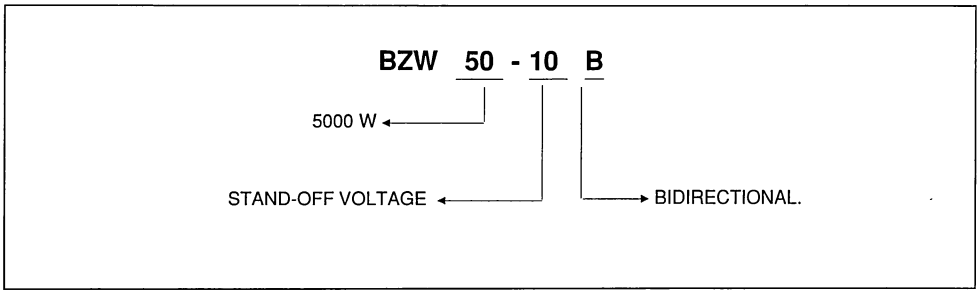


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with L_{lead} = 10mm.



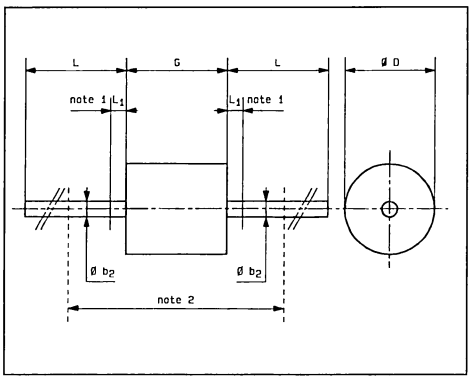
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

AG plastic.



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	1.35	1.45	0.053	0.057
Ø D	-	8	-	0.315
G	-	9.8	-	0.354
L	20	-	0.787	-
L_1	-	1.27	-	0.050

note 1 : The lead diameter Ø b_2 is not controlled over zone L_1
note 2 : 20mm minimum between bendings.

Weight = 1.6 g.

Packaging : standard packaging is in bulk.

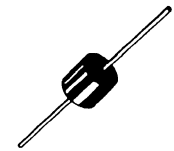
SGS-THOMSON MICROELECTRONICS

LDP24AS

TRANSIL LOAD DUMP PROTECTION

FEATURES

- TRANSIENT VOLTAGE SUPPRESSOR DIODE ESPECIALLY DESIGNED FOR LOAD DUMP EFFECT PROTECTION
- HIGH SURGE CURRENT CAPABILITY : 40 A / 40 ms EXPONENTIAL WAVE
- COMPLIANT WITH MAIN STANDARDS SUCH AS:
  -ISO / DTR 7637
  -SAEJ 1113A ...



AG
(Plastic)

DESCRIPTION

Transient voltage suppressor diode especially developed for sensitive circuit protection in automotive systems such as dash board, car radios etc.

Its high surge current capability and instantaneous response to transients provide an efficient protection against the load dump effect.

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse load dump overvoltage See note 1 - 2	T_{amb} = 85°C	120	V
P	Power dissipation on infinite heatsink	T_{amb} = 100°C	5	W
I_{FSM}	Non repetitive surge peak forward current.	T_j initial = 25°C t = 10 ms	200	A
T_{stg} T_j	Storage and junction temperature range.		- 65 to + 175 170	°C °C
T_L	Maximum lead temperature for soldering during 10 sec at 4 mm from case.		230	°C

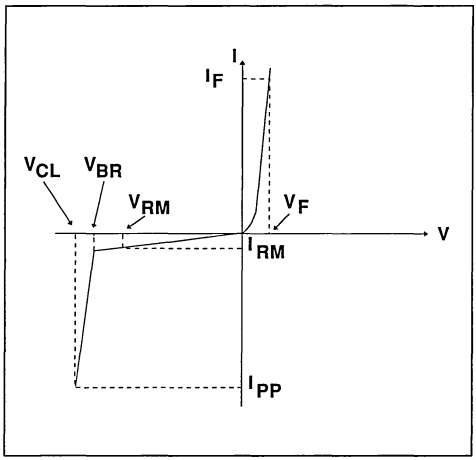
THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink		15	°C/W
R_{th} (j-a)	Junction to ambient on printed circuit.	L_{lead} = 10 mm	50	°C/W

Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{PP}	Peak pulse current.
αT	Temperature coefficient of V_{BR}.
C	Capacitance
t clamping	Clamping time (0V to V_{BR}): tp = 1ps



Symbol	Test Conditions		Min.	Typ.	Max.	Unit
I_{RM}	T_C = -40°C T_C = 25°C T_C = 85°C	V_{RM} = 24V			10 50 300	µA
V_{BR}	T_C = 25°C	I_R = 1mA	25		32	V
V_{CL}	T_C = -40°C T_C = 25°C T_C = 85°C	I_{PP} = 40A (Note 2)			36 38 40	V
αT	T_C = 25°C				9.6	10^{-4}/°C
C	F = 1MHz	V_R = 0V		8000		pF

Note 2 : Surge generator

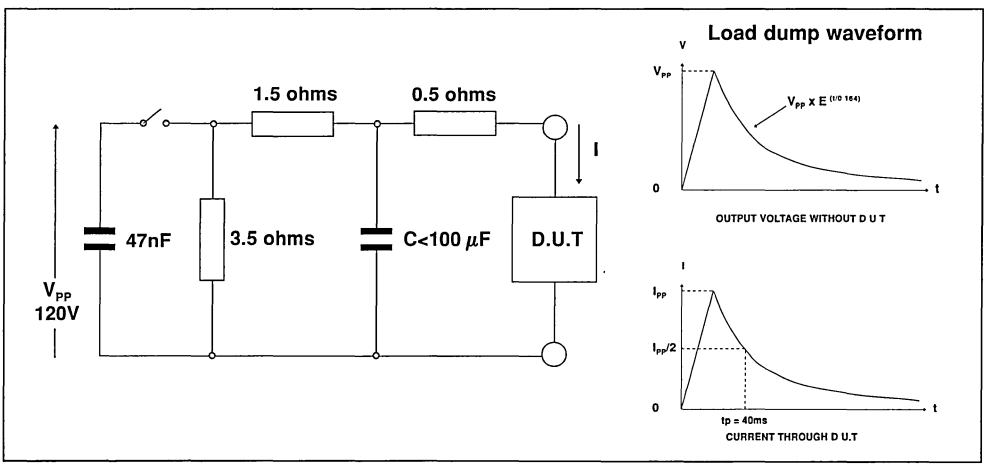


Figure 1 : Peak pulse power versus exponential pulse duration (T_j initial =85°C).

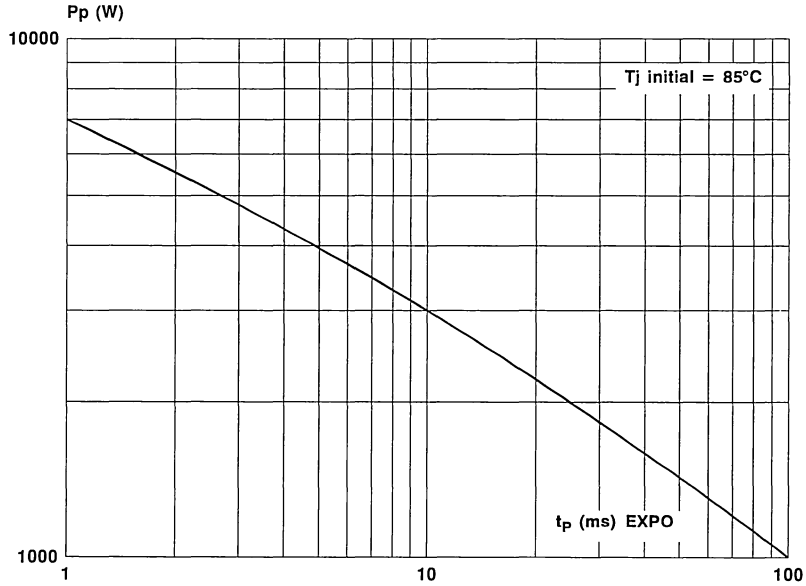


Figure 2 : Clamping voltage versus peak pulse current (T_j initial =85°C).
exponential waveform t = 40 ms ----------
t = 1 ms _____

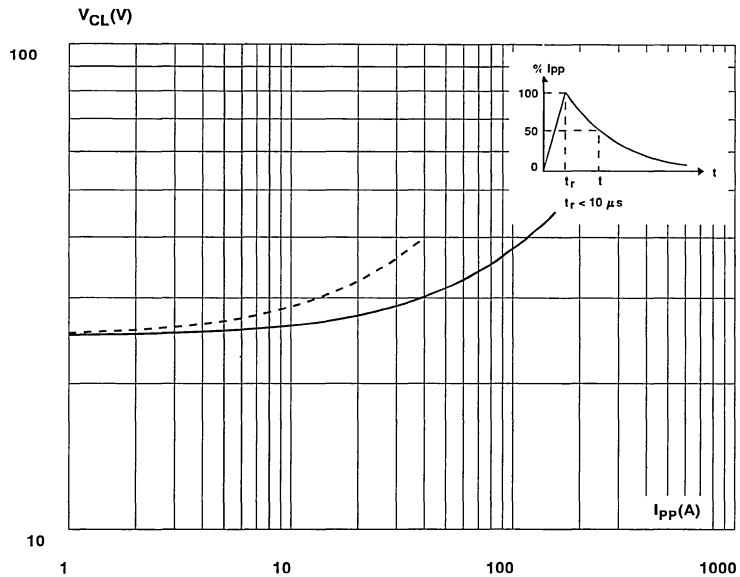


Figure 3 : Peak pulse current versus exponential pulse duration (T_j initial =85°C).

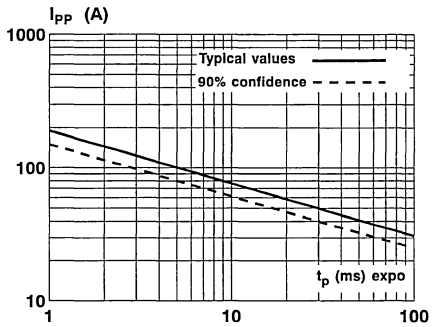


Figure 4 : Peak pulse power versus junction temperature.

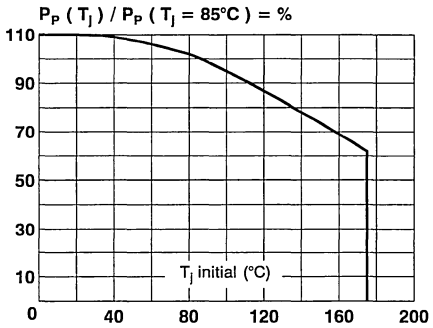


Figure 5 : Transient thermal impedance junction-ambient versus pulse duration (device mounted on PC Board with L_{lead} = 10mm).

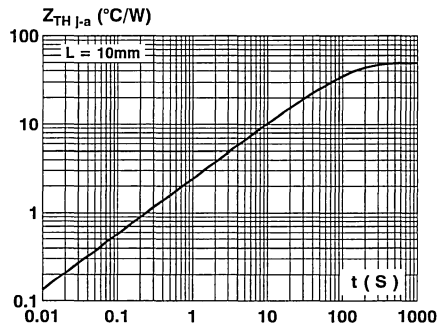
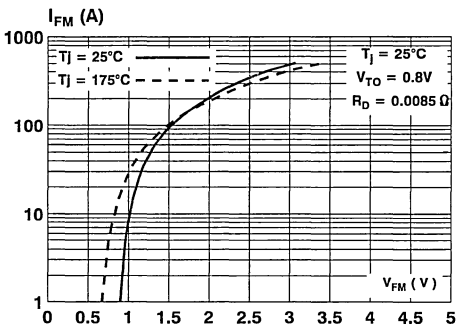
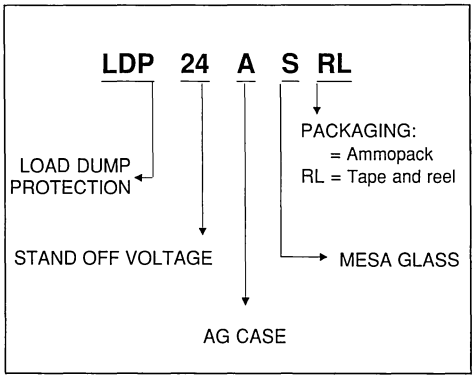


Figure 6 : Peak forward current versus peak forward voltage drop (typical values).



ORDER CODE



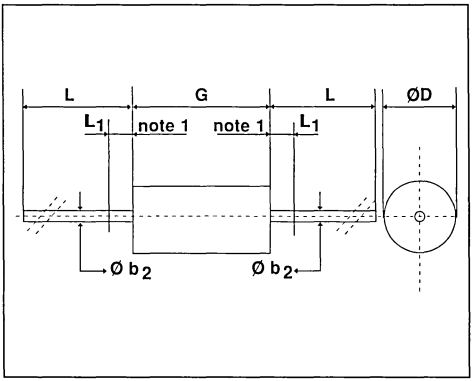
MARKING : Logo, Date Code, Type Code, Cathode Band.

Weight = 1 g.

Packaging : standard packaging is in tape and reel.

PACKAGE MECHANICAL DATA

AG (Plastic).



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	1.35	1.45	0.053	0.057
Ø D	-	8	-	0.315
G	-	9	-	0.354
L	20	-	0.787.	-
L_1	-	1.27	-	0.050

Note1: The diameter Ø b2 is not controlled over zone L1. Cooling method : by convection (method A).

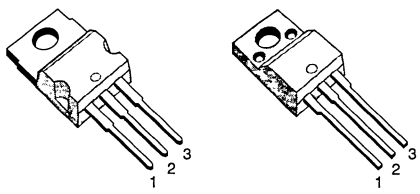
SGS-THOMSON MICROELECTRONICS

MTP3055E
MTP3055EFI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
MTP3055E	60 V	0.15 Ω	14 A
MTP3055EFI	60 V	0.15 Ω	10 A

- AVALANCHE RUGGEDNESS TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE FOR STANDARD PACKAGE
- APPLICATION ORIENTED CHARACTERIZATION
- ISOLATED PACKAGE UL RECOGNIZED, ISOLATION TO 2000V DC

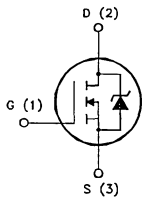


TO-220 ISOWATT220

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		MTP3055E	MTP3055EFI	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60		V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	60		V
V_{GS}	Gate-source Voltage	± 20		V
I_D	Drain Current (cont.) at T_c = 25 °C (#)	14	10	A
I_D	Drain Current (cont.) at T_c = 100 °C	10.5	6	A
I_{DM}(•)	Drain Current (pulsed)	56	56	A
P_{tot}	Total Dissipation at T_c = 25 °C	70	30	W
	Derating Factor	0.47	0.24	W/°C
T_{stg}	Storage Temperature	-65 to 175	-65 to 150	°C
T_j	Max. Operating Junction Temperature	175	150	°C

(•). Pulse width limited by safe operating area
(#) T_c = 50 °C for TO-220

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.1	4.17	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5		°C/W
$R_{thc\text{-}s}$	Thermal Resistance Case-sink	Typ	0.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	14	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25\ °C$, $I_D = I_{AR}$, $V_{DD} = 25$ V)	35	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	9	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive ($T_c = 100\ °C$, pulse width limited by T_j max, $\delta < 1\%$)	8.5	A

ELECTRICAL CHARACTERISTICS ($T_{case} = 25\ °C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu A$ $V_{GS} = 0$	60			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$) Zero Gate Voltage Drain Current ($V_{GS} = 0$)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 $T_c = 125\ °C$			50 1000	µA µA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20$ V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu A$	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10$V $I_D = 7$ A			0.15	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10$ V	14			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 7$ A	3			S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25$ V f = 1 MHz $V_{GS} = 0$			600 300 150	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING RESISTIVE LOAD

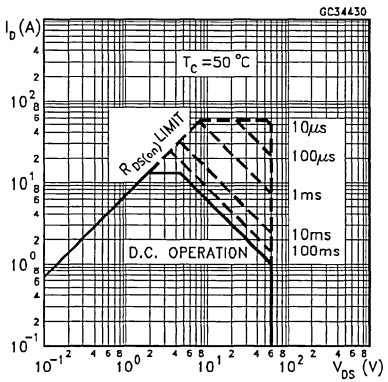
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	V_{DD} = 25 V I_D = 9 A		45	65	ns
t_r	Rise Time	R_G = 50 Ω V_{GS} = 10 V		75	100	ns
$t_{d(off)}$	Turn-off Delay Time	(see test circuit)		55	75	ns
t_f	Fall Time			50	70	ns
Q_g	Total Gate Charge	I_D = 14 A V_{GS} = 10 V V_{DD} = 40 V (see test circuit)		18	25	nC

SOURCE DRAIN DIODE

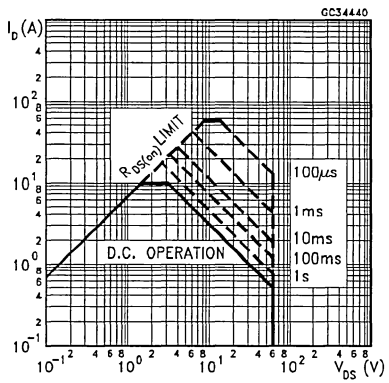
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				14	A
I_{SDM}(•)	Source-drain Current (pulsed)				56	A
V_{SD} (*)	Forward On Voltage	I_{SD} = 14 A V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 14 A di/dt = 100 A/µs V_{DD} = 30 V T_j = 150 °C		80		ns
Q_{rr}	Reverse Recovery Charge			0.15		µC

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

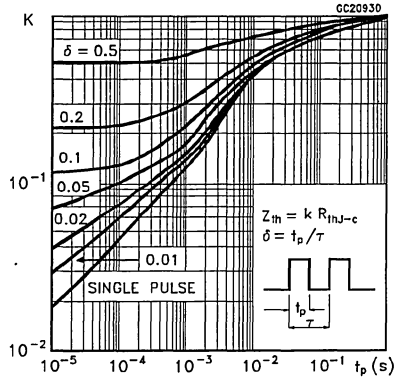
Safe Operating Area for TO-220



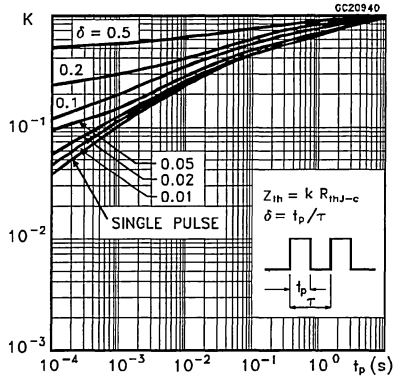
Safe Operating Area for ISOWATT220



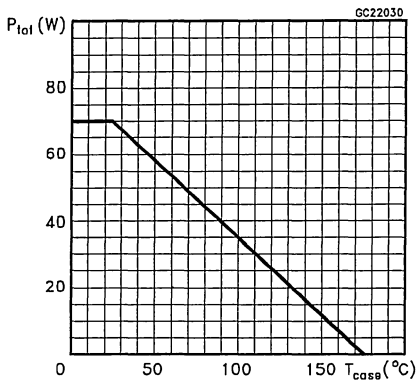
Thermal Impedance for TO-220



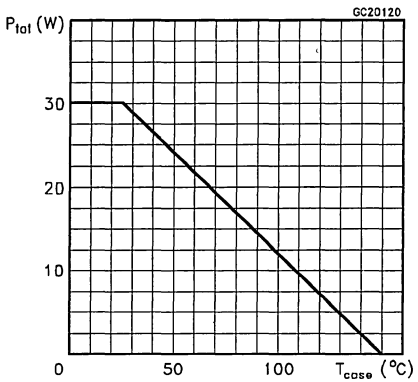
Thermal Impedance for ISOWATT220



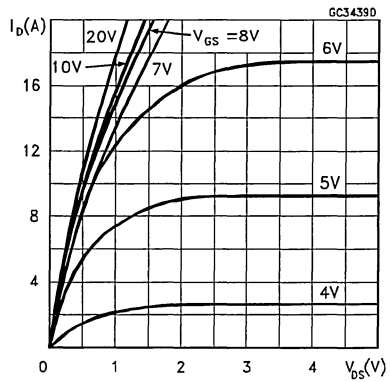
Derating Curve for TO-220



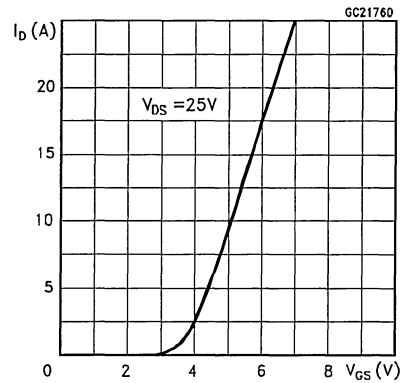
Derating Curve for ISOWATT220



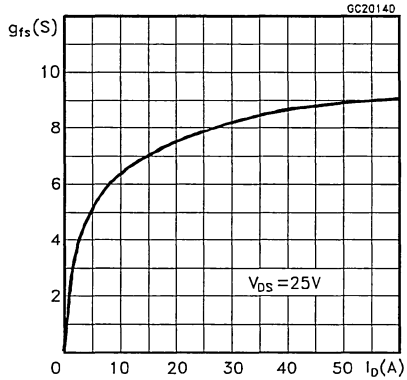
Output Characteristics



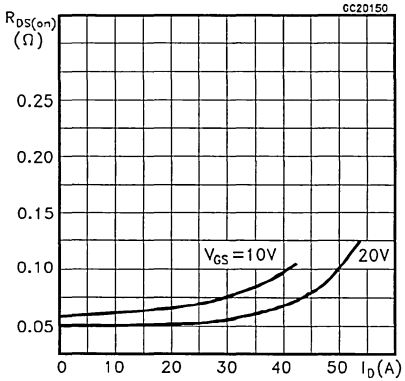
Transfer Characteristics



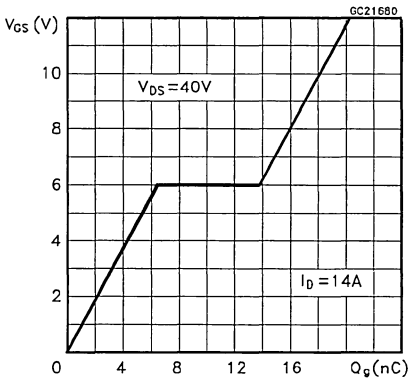
Transconductance



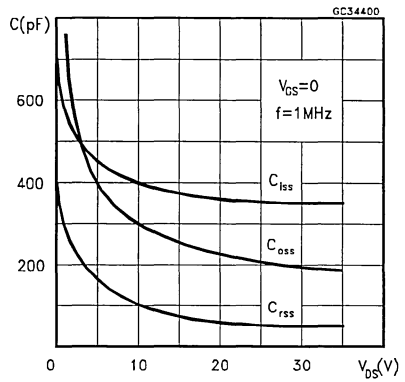
Static Drain-source On Resistance



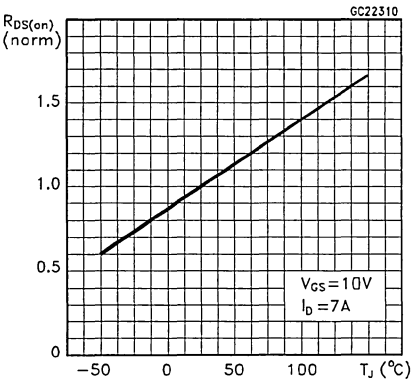
Gate Charge vs Gate-source Voltage



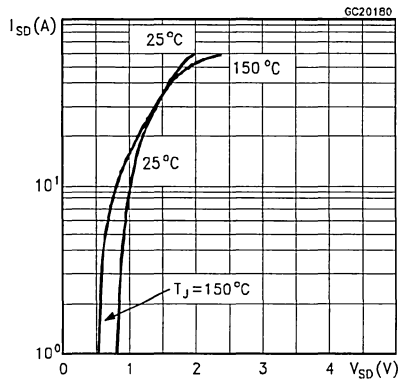
Capacitance Variations



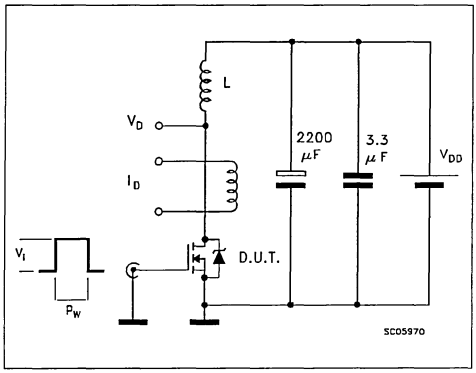
Normalized On Resistance vs Temperature



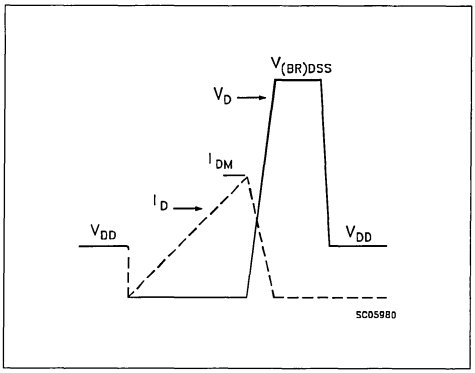
Source-drain Diode Forward Characteristics



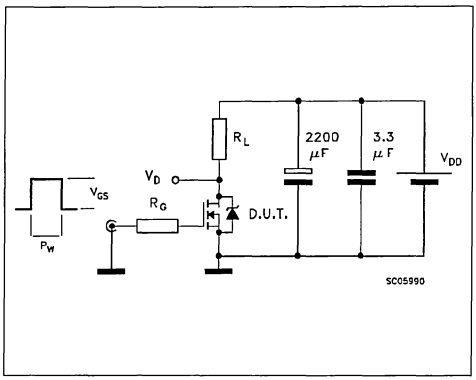
Unclamped Inductive Load Test Circuit



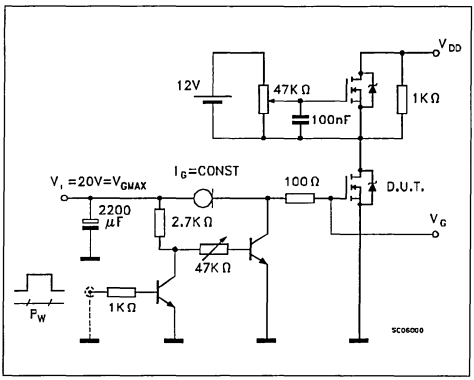
Unclamped Inductive Waveforms



Switching Time Test Circuit



Gate Charge Test Circuit



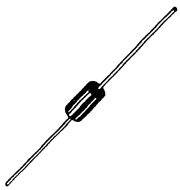
SGS-THOMSON MICROELECTRONICS

P6KE6V8P,A/440P,A
P6KE6V8CP,A/440CP,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 600 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 440 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).
- UL RECOGNIZED.



CB417
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code, and Cathode Band (for unidirectional types only).
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

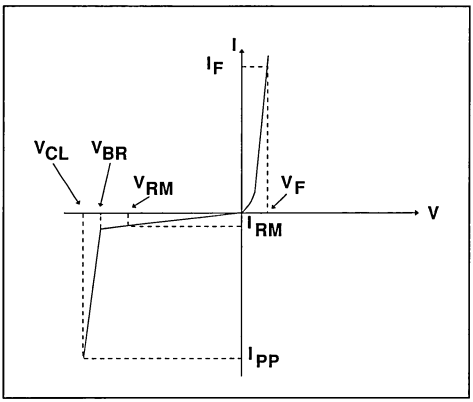
Symbol	Parameter		Value	Unit
P_{pp}	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	600	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	5	W
I_{FSM}	Non repetitive surge peak forward current For Unidirectional types.	Tamb = 25°C t =10 ms	100	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 175	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	20	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. L_{lead} = 10 mm	85	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 50 A.



TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min	nom	max		V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
				note2									
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
P6KE6V8P	P P6KE6V8CP	1000	5.8	6.45	6.8	7.48	10	10.5	57	13.4	298	5.7	4000
P P6KE6V8A	P P6KE6V8CA	1000	5.8	6.45	6.8	7.14	10	10.5	57	13.4	298	5.7	4000
P6KE7V5P	P6KE7V5CP	500	6.4	7.13	7.5	8.25	10	11.3	53	14.5	276	6.1	3700
P6KE7V5A	P P6KE7V5CA	500	6.4	7.13	7.5	7.88	10	11.3	53	14.5	276	6.1	3700
P6KE8V2P	P P6KE8V2CP	200	7.02	7.79	8.2	9.02	10	12.1	50	15.5	258	6.5	3400
P P6KE8V2A	P6KE8V2CA	200	7.02	7.79	8.2	8.61	10	12.1	50	15.5	258	6.5	3400
P6KE9V1P	P6KE9V1CP	50	7.78	8.65	9.1	10	1	13.4	45	17.1	234	6.8	3100
P6KE9V1A	P6KE9V1CA	50	7.78	8.65	9.1	9.55	1	13.4	45	17.1	234	6.8	3100
P P6KE10P	P6KE10CP	10	8.55	9.5	10	11	1	14.5	41	18.6	215	7.3	2800
P6KE10A	P6KE10CA	10	8.55	9.5	10	10.5	1	14.5	41	18.6	215	7.3	2800
P6KE11P	P6KE11CP	5	9.4	10.5	11	12.1	1	15.6	38	20.3	197	7.5	2500
P6KE11A	P6KE11CA	5	9.4	10.5	11	11.6	1	15.6	38	20.3	197	7.5	2500
P P6KE12P	P P6KE12CP	5	10.2	11.4	12	13.2	1	16.7	36	21.7	184	7.8	2300
P6KE12A	P6KE12CA	5	10.2	11.4	12	12.6	1	16.7	36	21.7	184	7.8	2300
P6KE13P	P6KE13CP	5	11.1	12.4	13	14.3	1	18.2	33	23.6	169	8.1	2150
P P6KE13A	P P6KE13CA	5	11.1	12.4	13	13.7	1	18.2	33	23.6	169	8.1	2150
P P6KE15P	P P6KE15CP	5	12.8	14.3	15	16.5	1	21.2	28	27.2	147	8.4	1900
P6KE15A	P6KE15CA	5	12.8	14.3	15	15.8	1	21.2	28	27.2	147	8.4	1900
P6KE16P	P6KE16CP	5	13.6	15.2	16	17.6	1	22.5	27	28.9	138	8.6	1800
P6KE16A	P6KE16CA	5	13.6	15.2	16	16.8	1	22.5	27	28.9	138	8.6	1800
P P6KE18P	P P6KE18CP	5	15.3	17.1	18	19.8	1	25.2	24	32.5	123	8.8	1600
P P6KE18A	P P6KE18CA	5	15.3	17.1	18	18.9	1	25.2	24	32.5	123	8.8	1600
P6KE20P	P P6KE20CP	5	17.1	19	20	22	1	27.7	22	36.1	111	9.0	1500
P P6KE20A	P P6KE20CA	5	17.1	19	20	21	1	27.7	22	36.1	111	9.0	1500
P6KE22P	P P6KE22CP	5	18.8	20.9	22	24.2	1	30.6	20	39.3	102	9.2	1350

P = Prefered device

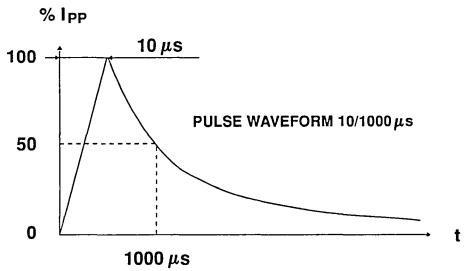
TYPES		I_{RM} @ V_{RM}		V_{BR} @ I_R				V_{CL} @ I_{PP}		V_{CL} @ I_{PP}		αT	C
		max		min	nom	max		max		max		max	typ
						note2		10/1000µs		8/20µs		note3	note4
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
P6KE22A	P6KE22CA	5	18.8	20.9	22	23.1	1	30.6	20	39.3	102	9.2	1350
P6KE24P	P6KE24CP	5	20.5	22.8	24	26.4	1	33.2	18	42.8	93	9.4	1250
P P6KE24A	P6KE24CA	5	20.5	22.8	24	25.2	1	33.2	18	42.8	93	9.4	1250
P P6KE27P	P P6KE27CP	5	23.1	25.7	27	29.7	1	37.5	16	48.3	83	9.6	1150
P6KE27A	P6KE27CA	5	23.1	25.7	27	28.4	1	37.5	16	48.3	83	9.6	1150
P P6KE30P	P P6KE30CP	5	25.6	28.5	30	33	1	41.5	14.5	53.5	75	9.7	1075
P P6KE30A	P P6KE30CA	5	25.6	28.5	30	31.5	1	41.5	14.5	53.5	75	9.7	1075
P6KE33P	P6KE33CP	5	28.2	31.4	33	36.3	1	45.7	13.1	59.0	68	9.8	1000
P P6KE33A	P P6KE33CA	5	28.2	31.4	33	34.7	1	45.7	13.1	59.0	68	9.8	1000
P P6KE36P	P P6KE36CP	5	30.8	34.2	36	39.6	1	49.9	12	64.3	62	9.9	950
P P6KE36A	P6KE36CA	5	30.8	34.2	36	37.8	1	49.9	12	64.3	62	9.9	950
P P6KE39P	P P6KE39CP	5	33.3	37.1	39	42.9	1	53.9	11.1	69.7	57	10.0	900
P P6KE39A	P P6KE39CA	5	33.3	37.1	39	41.0	1	53.9	11.1	69.7	57	10.0	900
P6KE43P	P6KE43CP	5	36.8	40.9	43	47.3	1	59.3	10.1	76.8	52	10.1	850
P6KE43A	P6KE43CA	5	36.8	40.9	43	45.2	1	59.3	10.1	76.8	52	10.1	850
P6KE47P	P P6KE47CP	5	40.2	44.7	47	51.7	1	64.8	9.3	84	48	10.1	800
P6KE47A	P P6KE47CA	5	40.2	44.7	47	49.4	1	64.8	9.3	84	48	10.1	800
P6KE51P	P P6KE51CP	5	43.6	48.5	51	56.1	1	70.1	8.6	91	44	10.2	750
P6KE51A	P P6KE51CA	5	43.6	48.5	51	53.6	1	70.1	8.6	91	44	10.2	750
P6KE56P	P P6KE56CP	5	47.8	53.2	56	61.6	1	77	7.8	100	40	10.3	700
P6KE56A	P6KE56CA	5	47.8	53.2	56	58.8	1	77	7.8	100	40	10.3	700
P6KE62P	P6KE62CP	5	53.0	58.9	62	68.2	1	85	7.1	111	36	10.4	650
P6KE62A	P6KE62CA	5	53.0	58.9	62	65.1	1	85	7.1	111	36	10.4	650
P6KE68P	P P6KE68CP	5	58.1	64.6	68	74.8	1	92	6.5	121	33	10.4	625
P6KE68A	P6KE68CA	5	58.1	64.6	68	71.4	1	92	6.5	121	33	10.4	625
P6KE75P	P6KE75CP	5	64.1	71.3	75	82.5	1	103	5.8	134	30	10.5	575
P6KE75A	P6KE75CA	5	64.1	71.3	75	78.8	1	103	5.8	134	30	10.5	575
P6KE82P	P P6KE82CP	5	70.1	77.9	82	90.2	1	113	5.3	146	27	10.5	550
P6KE82A	P6KE82CA	5	70.1	77.9	82	86.1	1	113	5.3	146	27	10.5	550
P6KE91P	P6KE91CP	5	77.8	86.5	91	100	1	125	4.8	162	25	10.6	525
P6KE91A	P6KE91CA	5	77.8	86.5	91	95.5	1	125	4.8	162	25	10.6	525
P6KE100P	P6KE100CP	5	85.5	95.0	100	110	1	137	4.4	178	22.5	10.6	500
P6KE100A	P6KE100CA	5	85.5	95.0	100	105	1	137	4.4	178	22.5	10.6	500
P6KE110P	P6KE110CP	5	94.0	105	110	121	1	152	3.9	195	20.5	10.7	470
P6KE110A	P6KE110CA	5	94.0	105	110	116	1	152	3.9	195	20.5	10.7	470
P6KE120P	P6KE120CP	5	102	114	120	132	1	165	3.6	212	19	10.7	450
P6KE120A	P6KE120CA	5	102	114	120	126	1	165	3.6	212	19	10.7	450
P6KE130P	P P6KE130CP	5	111	124	130	143	1	179	3.4	230	17.5	10.7	420
P6KE130A	P6KE130CA	5	111	124	130	137	1	179	3.4	230	17.5	10.7	420
P6KE150P	P P6KE150CP	5	128	143	150	165	1	207	2.9	265	15	10.8	400
P P6KE150A	P P6KE150CA	5	128	143	150	158	1	207	2.9	265	15	10.8	400
P6KE160P	P P6KE160CP	5	136	152	160	176	1	219	2.7	282	14	10.8	380
P6KE160A	P6KE160CA	5	136	152	160	168	1	219	2.7	282	14	10.8	380
P6KE170P	P6KE170CP	5	145	161	170	187	1	234	2.6	301	13	10.8	370
P6KE170A	P6KE170CA	5	145	161	170	179	1	234	2.6	301	13	10.8	370
P6KE180P	P P6KE180CP	5	154	171	180	198	1	246	2.4	317	12.6	10.8	360
P6KE180A	P6KE180CA	5	154	171	180	189	1	246	2.4	317	12.6	10.8	360
P6KE200P	P P6KE200CP	5	171	190	200	220	1	274	2.2	353	11.3	10.8	350
P P6KE200A	P P6KE200CA	5	171	190	200	210	1	274	2.2	353	11.3	10.8	350
P6KE220P	P6KE220CP	5	188	209	220	242	1	328	2	388	10.3	10.8	330
P6KE220A	P6KE220CA	5	188	209	220	231	1	328	2	388	10.3	10.8	330
P6KE250P	P P6KE250CP	5	213	237	250	275	1	344	2	442	9	11	310
P6KE250A	P6KE250CA	5	213	237	250	263	1	344	2	442	9	11	310
P6KE280P	P6KE280CP	5	239	266	280	308	1	384	2	494	8	11	300
P6KE280A	P6KE280CA	5	239	266	280	294	1	384	2	494	8	11	300

P = Prefered device

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
P6KE300P	P6KE300CP	5	256	285	300	330	1	414	1.6	529	7.6	11	290
P6KE300A	P6KE300CA	5	256	285	300	315	1	414	1.6	529	7.6	11	290
P6KE320P	P6KE320CP	5	273	304	320	352	1	438	1.6	564	7.1	11	280
P6KE320A	P6KE320CA	5	273	304	320	336	1	438	1.6	564	7.1	11	280
P6KE350P	P6KE350CP	5	299	332	350	385	1	482	1.6	618	6.5	11	270
P P6KE350A	P6KE350CA	5	299	332	350	368	1	482	1.6	618	6.5	11	270
P P6KE400P	P P6KE400CP	5	342	380	400	440	1	548	1.3	706	5.7	11	360
P6KE400A	P6KE400CA	5	342	380	400	420	1	548	1.3	706	5.7	11	360
P P6KE440P	P P6KE440CP	5	376	418	440	484	1	603	1.3	776	5.2	11	350
P6KE440A	P6KE440CA	5	376	418	440	462	1	603	1.3	776	5.2	11	350

All parameters tested at 25 °C, except where indicated.

P = Prefered device



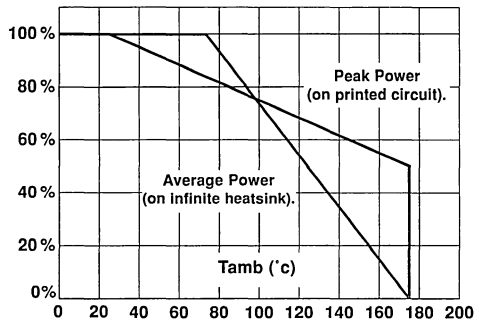


Figure 1: Power dissipation derating versus ambient temperature

Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode

Note 2 : Pulse test: $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.

Figure 2 : Peak pulse power versus exponential pulse duration.

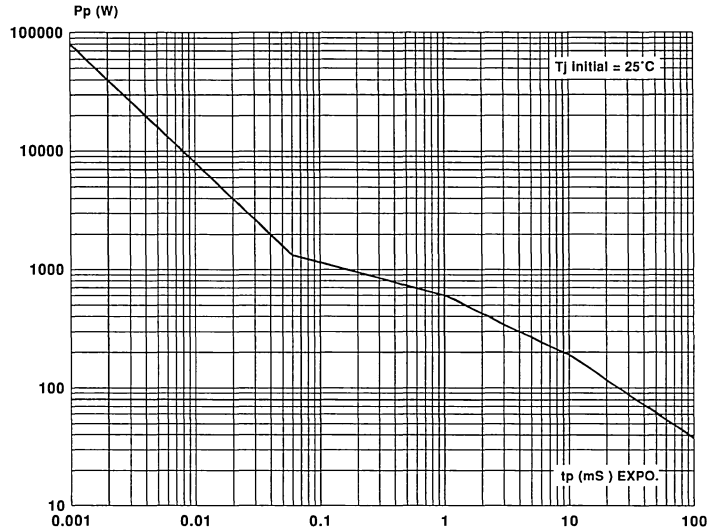
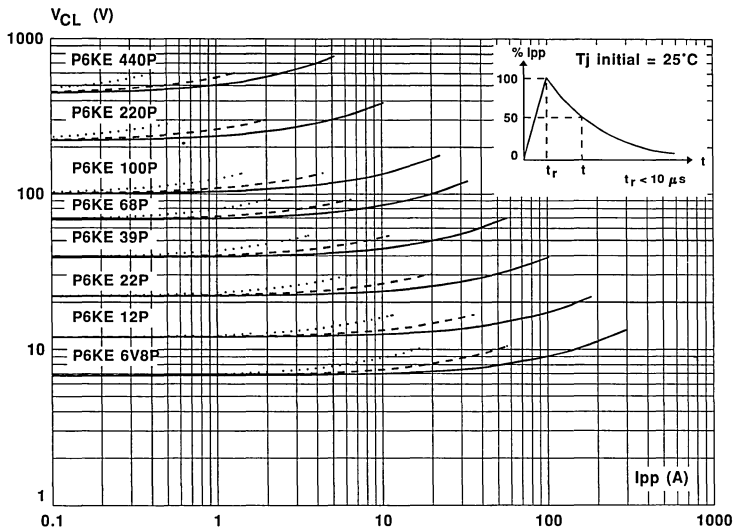


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} \cdot [T_a - 25] \cdot V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

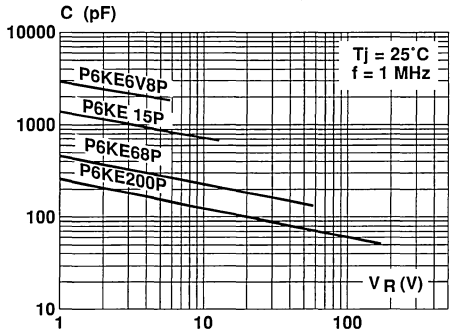


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

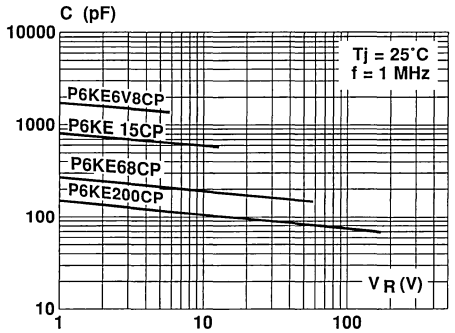


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

Note : For units with $V_{BR} > 200$ V
V_F is twice than shown.

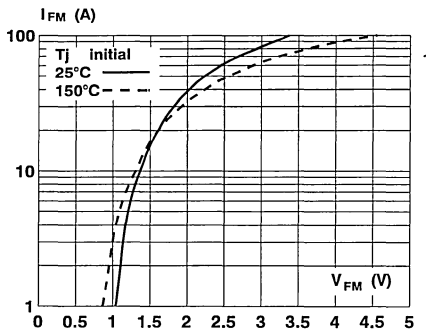
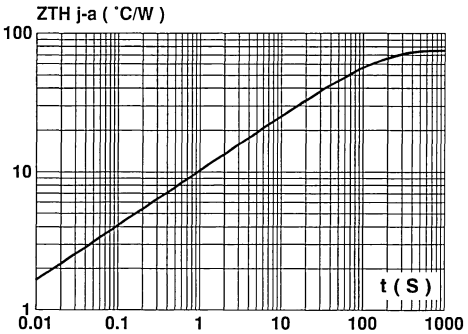
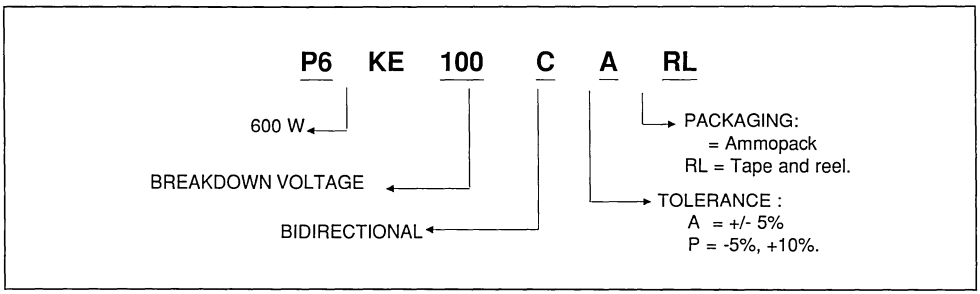


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with L_{lead} = 10mm.



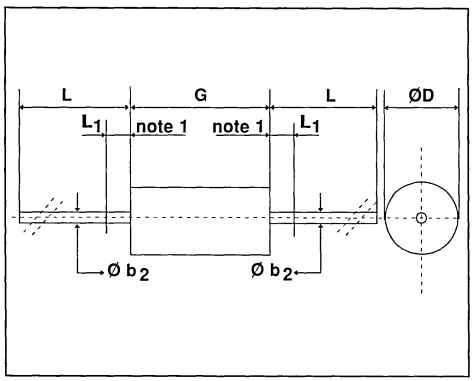
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

CB417 (Plastic).



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	-	1.092	-	0.043
Ø D	-	3.683	-	0.145
G	-	8.89	-	0.350
L	25.4	-	1.000	-
L_1	-	1.25	-	0.049

note1:The diameter Ø b_2 is not controlled over zone L_1

Weight = 0.65 g.

Packaging : standard packaging is in tape and reel.

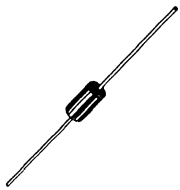
SGS-THOMSON MICROELECTRONICS

PL360D

TRANSIL

FEATURES

- PEAK PULSE POWER= 300 W @ 1ms.
- BREAKDOWN VOLTAGE = 330 V min.
- UNIDIRECTIONAL TRANSIL.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME:
  Tclamping : 1ps (0 V to VBR).



F126
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action.
The PL360D has been especially designed for transistor protection in electronic ignition circuits. Connected across collector and base, it avoids any transistor damage when a spark plug is fouled or disconnected.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band .
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

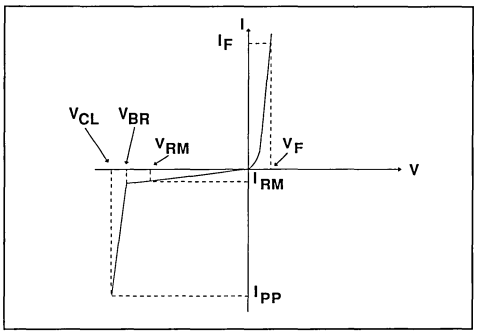
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	300	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	1.7	W
I_{ZM}	Continuous reverse current.	Tamb = 50°C	3.5	mA
T_{oper}	Operation temperature.		- 55 to 150	°C
T_{stg} T_j	Storage and junction temperature range.		- 55 to + 150 150	°C °C
T_L	Maximum lead temperature for soldering during 3 sec at 5 mm from case.		300	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	60	°C/W
R_{th} (j-a)	Junction to ambient on printed circuit. L_{lead} = 10 mm	100	°C/W

ELECTRICAL CHARACTERISTICS

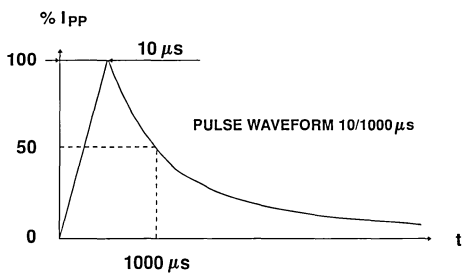
Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.



ELECTRICAL CHARACTERISTICS

Type	I_{RM} @ V_{RM}		V_{BR} @ T_j = 25 °C		V_{BR} @ T_j = 120 °C		IR	I_{ZM}	αT
	max		min	max	min	max			max
	µA	V	V		V		mA	mA	10^{-4}/°C
PL360D	0.35	270	330	370	358	416	2	3.5	11

All parameters tested at 25 °C, except where indicated.



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

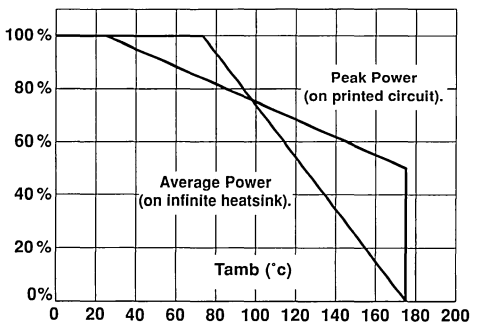


Figure 1: Power dissipation derating versus ambient temperature

Figure 2 : Peak pulse power versus exponential pulse duration.

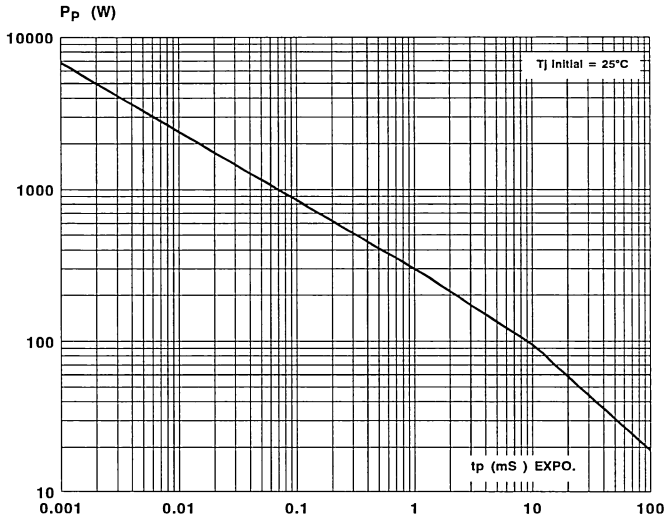
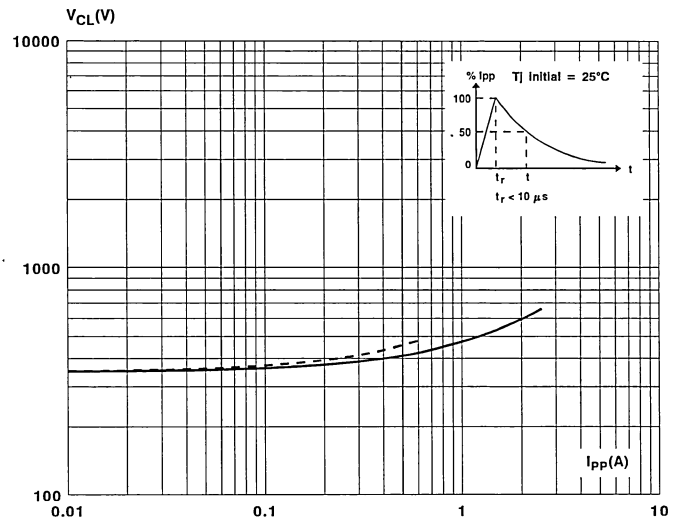


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} \cdot [T_a - 25] \cdot V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4 : Capacitance versus reverse applied voltage.

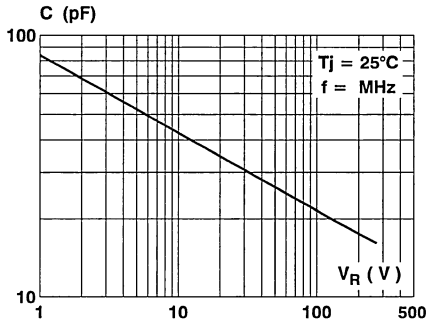
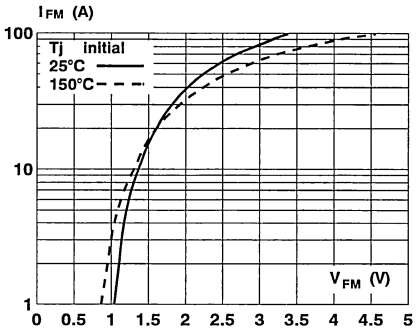
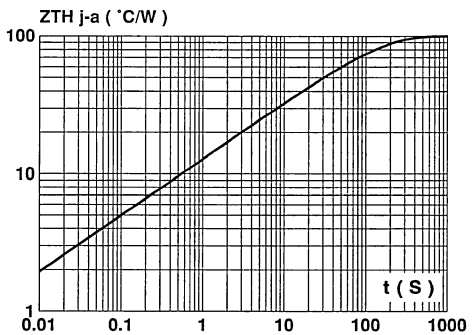


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).



Note : For units with V_{BR} > 200 V
V_F is twice than shown.

Figure 6 : Transient thermal impedance junction-ambient versus pulse duration (device mounted on PC Board with L_{lead} = 10mm).



ORDER CODE

PL360D RL

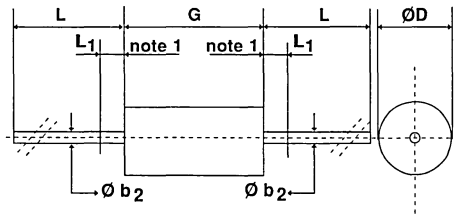
PACKAGING:
= Ammopack
RL = Tape and reel.

MARKING : Logo, Date Code, Type Code, Cathode Band.

Packaging : standard packaging is in tape and reel.

PACKAGE MECHANICAL DATA

F 126 (Plastic).



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	0.76	0.86	0.029	0.034
Ø D	2.95	3.05	0.116	0.120
G	6.05	6.35	0.238	0.250
L	26	-	1.024	-
L_1	-	1.27	-	0.050

Note1:The diameter Ø b_2 is not controlled over zone L_1

Weight = 0.4 g.

SGS-THOMSON MICROELECTRONICS

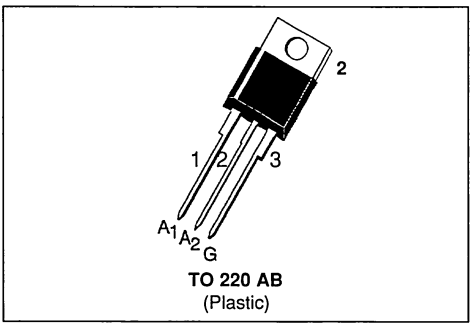
RBO08-40

REVERSED BATTERY AND OVERVOLTAGE PROTECTION CIRCUIT (RBO)

PRELIMINARY DATA

FEATURES

- DISSIPATION THROUGH PIN 2 : TAB CONNECTED TO GROUND
- MONOLITHIC SILICON CHIP
- NEGATIVE OVERVOLTAGE PROTECTION BY CLAMPING (COMPONENT T1)
- BREAKDOWN VOLTAGE : 24 V min
- CLAMPING VOLTAGE : ± 40 V max
- AVERAGE FORWARD CURRENT (COMPONENT D1) : 8 A



TO 220 AB
(Plastic)

DESCRIPTION

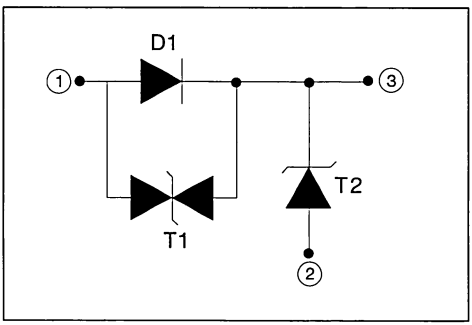
Developed especially for automotive reversed battery operation and overvoltage protection, this monolithic component chip offers multiple functions in the same package (see page 3) :

D1 : reversed battery protection

T1 : clamping function to negative overvoltage effect

T2 : Transil function to positive overvoltage effect

FUNCTIONAL DIAGRAM



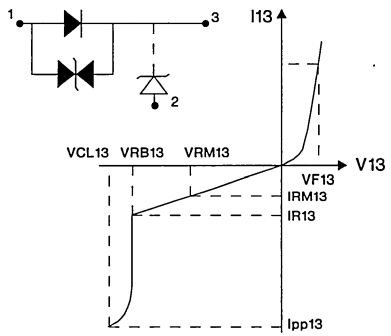
ABSOLUTE RATINGS (limiting values)

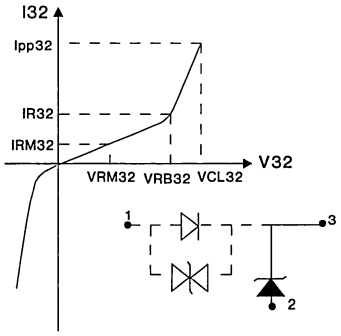
Symbol	Parameter		Value	Unit
I_{FSM}	Non repetitive surge peak forward current between Pins 1 and 3 @ T= 10 µs	Tj = 25°C	80	A
$I_{F(AV)}$	Average forward current between Pins 1 and 3	Tc = 85°C	8	A
P_P	Peak pulse between Pins 1 and 3 @ T= 1 ms (see note 1)	Tc = 85°C	600	W
P_{PP}	Peak pulse power between Pins 2 and 3 @ T= 1 ms	Tc = 85°C	1500	W
P	Total power dissipation	Tc = 85°C	25	W
Tstg Tj	Storage and junction temperature range		- 40 to + 150	°C
T_L	Maximum lead temperature for soldering during 10 s at 4.5 mm from case		230	°C

Note 1 : for a surge greater than the maximum value, the source will present a short circuit.

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
Rth (j-c)	Junction to case	2.4	°C/W



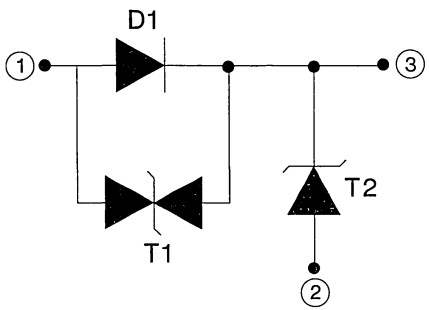


ELECTRICAL CHARACTERISTICS

Symbol	Test Conditions			Value	Unit
$V_{F\ 13}$	Maximum forward voltage @ I_F = 8 A	Tj=25°C	MAX	1.7	V
		Tj=85°C			
$V_{F\ 13}$	Maximum forward voltage @ IF = 4 A	Tj=25°C	MAX	1.35	V
		Tj=85°C			
$V_{F\ 13}$	Maximum forward voltage @ IF = 1 A	Tj=85°C	MAX	0.9	V
$V_{BR\ 31}$	Breakdown voltage @ IR = 1 mA	Tj=25°C	MIN	24	V
			MAX	32	
$I_{RM\ 31}$	Leakage current @ V_{RM} = 20 V	Tc=25°C	MAX	10	µA
		Tc=85°C		100	
$V_{CL\ 31}$	Clamping voltage @ I_{PP} = 15 A @ T= 1 ms	Tc=25°C	MAX	40	V
$V_{BR\ 32}$	Breakdown voltage @ I_R = 1 mA	Tj=25°C	MIN	24	V
			MAX	32	
$I_{RM\ 32}$	Leakage current @ V_{RM} = 20 V	Tc=25°C	MAX	10	µA
		Tc=85°C		50	
$V_{CL\ 32}$	Clamping voltage @ IPP = 37.5 A @ T= 1 ms	Tc=25°C	MAX	40	V
α t	Temperature coefficient	Tc=25°C	MAX	10^{-4}	/°C
C 13	Capacitance at 0 V	Tc=25°C	TYP	1000	pF
C 32	Capacitance at 0 V	Tc=25°C	TYP	2000	pF

Note : 13 and 32
Ex : $V_{F\ 13}$. between Pin 1 and Pin 3
$V_{BR\ 32}$. between Pin 3 and Pin 2

PRODUCT DESCRIPTION



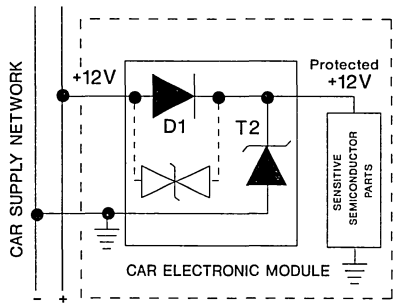
The RBO has 3 functions integrated on the same chip.

D1 : "Rectifier function" in order to protect against reversed battery operation.

T2 : "Transil function" in order to protect against positive surge generated by electric systems (ignition, relay. ...).

T1 : Protection for motor drive application (See below).

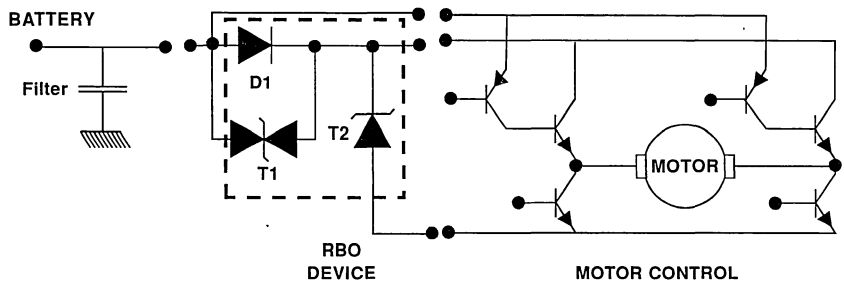
BASIC APPLICATION



*The monolithic multi function protection (RBO) has been developed to protect sensitive semiconductors in the car electronic module against both overvoltage and battery reverse.

*In addition, the RBO circuit prevents overvoltages generated by the module affecting the car supply network.

MOTOR DRIVER APPLICATION



In this application, one half of the motor drive circuit is supplied through the "RBO" and is thus protected as per its basic function application.
The second part is connected directly to the "car supply network" and is protected as follows :
- For positive surges : T2 (clamping phase) and D1 in forward-biased.
- For negative surges : T1 (clamping phase) and T2 in forward-biased.

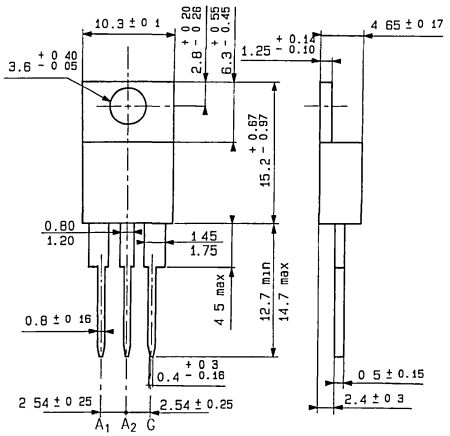
ORDERING INFORMATION

RBO 08 - 40 T

- RBO: Reversed Battery & Overvolage protection
- 08: $I_{F(AV)}$ = 8 A
- 40: V_{CL} = 40V
- T: Packages : T = TO 220 AB

PACKAGE MECHANICAL DATA (in millimeters)

TO 220 AB Plastic



Cooling method : C
Marking : type number
Weight : 2 g
Polarity : N A
Stud torque : N A

SGS-THOMSON MICROELECTRONICS

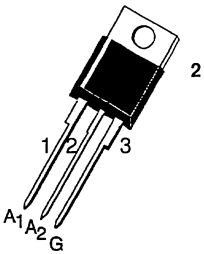
RBO40-40

REVERSED BATTERY AND OVERVOLTAGE PROTECTION CIRCUIT (RBO)

PRELIMINARY DATA

FEATURES

- DISSIPATION THROUGH PIN 2 : TAB CONNECTED TO GROUND
- MONOLITHIC SILICON CHIP
- NEGATIVE OVERVOLTAGE PROTECTION BY CLAMPING (COMPONENT T1)
- BREAKDOWN VOLTAGE : 24 V min
- CLAMPING VOLTAGE : ± 40 V max
- AVERAGE FORWARD CURRENT (COMPONENT D1) : 40 A



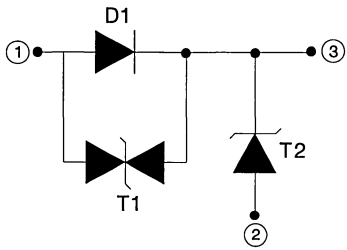
TO 220 AB
(Plastic)

DESCRIPTION

Developed especially for automotive reversed battery operation and overvoltage (load dump) protection, this monolithic component chip offers multiple functions in the same package (see page 4) :

D1 : reversed battery protection
T1 : clamping function to negative overvoltage effect
T2 : Transil function to Load Dump effect

FUNCTIONAL DIAGRAM



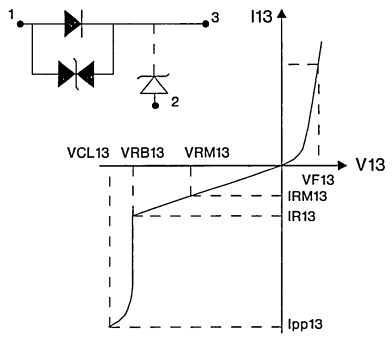
ABSOLUTE RATINGS (limiting values)

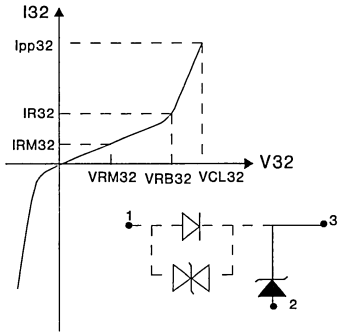
Symbol	Parameter		Value	Unit
I_{FSM}	Non repetitive surge peak forward current between Pins 1 and 3 @ T= 10 µs	Tj = 25°C	400	A
$I_{F(AV)}$	Average forward current between Pins 1 and 3	Tc = 80°C	40	A
V_{PP}	Peak load dump voltage (see note 1 and 2)	Tc = 85°C	80	V
P_{PP}	Peak pulse power between Pins 1 and 3 @ T= 1 ms	Tc = 85°C	1500	W
P	Total power dissipation	Tc = 80°C	70	W
Tstg Tj	Storage and junction temperature range		- 40 to + 150	°C
T_L	Maximum lead temperature for soldering during 10 s at 4.5 mm from case		230	°C

Notes 1 : for a surge greater than the maximum value, the source will present a short circuit.
Notes 2 : see schaffner circuit page 3

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
Rth (j-c)	Junction to case	1	°C/W



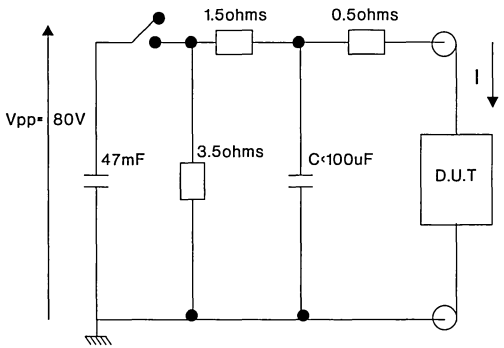


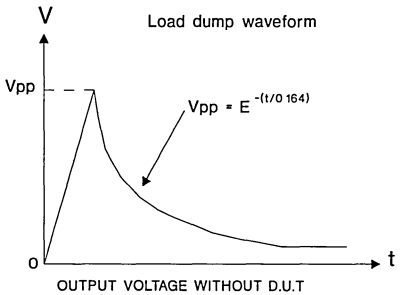
ELECTRICAL CHARACTERISTICS

Symbol	Test Conditions			Value	Unit
$V_{F\ 13}$	Maximum forward voltage @ I_F = 40 A	Tj=25°C	MAX	1.7	V
		Tj=85°C			
$V_{F\ 13}$	Maximum forward voltage @ IF = 20 A	Tj=25°C	MAX	1.35	V
		Tj=85°C			
$V_{F\ 13}$	Maximum forward voltage @ IF = 1A	Tj=85°C	MAX	0.9	V
$V_{BR\ 31}$	Breakdown voltage @ I_R = 1 mA	Tj=25°C	MIN	24	V
			MAX	32	
$I_{RM\ 31}$	Leakage current @ V_{RM} = 20 V	Tc=25°C	MAX	50	µA
		Tc=85°C		300	
$V_{CL\ 31}$	Clamping voltage @ I_{PP} = 37.5 A @ T= 1 ms	Tc=25°C	MAX	40	V
$V_{BR\ 32}$	Breakdown voltage @ I_R = 1 mA	Tj=25°C	MIN	24	V
			MAX	32	
$I_{RM\ 32}$	Leakage current @ V_{RM} = 20 V	Tc=25°C	MAX	10	µA
		Tc=85°C		100	
$V_{CL\ 32}$	Clamping voltage @ IPP = 20 A	Tc=25°C	MAX	40	V
α t	Temperature coefficient	Tc=25°C	MAX	10^{-4}	/°C
C 13	Capacitance at 0 V	Tc=25°C	TYP	3000	pF
C 32	Capacitance at 0 V	Tc=25°C	TYP	7000	pF

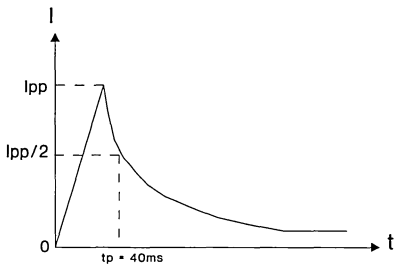
Note : 13 and 32
Ex : $V_{F\ 13}$. between Pin 1 and Pin 3
$V_{BR\ 32}$. between Pin 3 and Pin 2

SCHAFFNER CIRCUIT



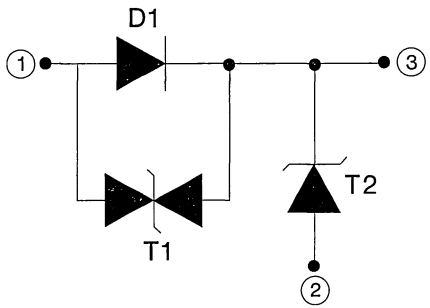


OUTPUT VOLTAGE WITHOUT D.U.T



CURRENT THROUGH D U T

PRODUCT DESCRIPTION



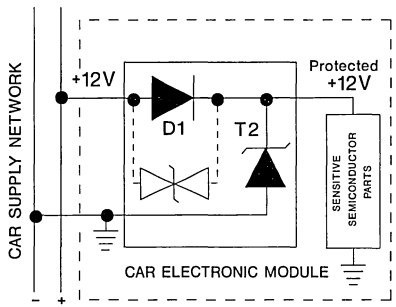
The RBO has 3 integrated functions on the same chip.

D1 : "Rectifier function" in order to protect against reversed battery operation.

T2 : "Transil function" in order to protect against Load dump generated by the alternator.

T1 : Protection for motor driver application (See below).

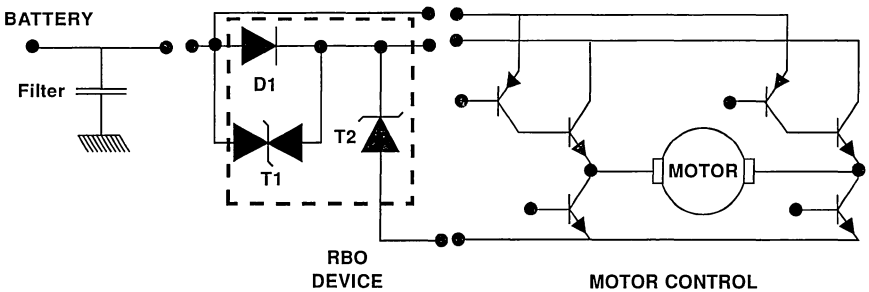
BASIC APPLICATION



*The monolithic multi function protection (RBO) has been developed to protect sensitive semiconductors in the car electronic module against both overvoltage and battery reverse.

*In addition, this RBO circuit prevents overvoltages generated by the module affecting the car supply network.

MOTOR DRIVER APPLICATION



In this application, one half of the motor drive circuit is supplied through the "RBO" and is thus protected as per its basic function application.
The second part is connected directly to the "car supply network" and is protected as follows :
- For positive surges : T2 (clamping phase) and D1 forward-biased.
- For negative surges : T1 (clamping phase) and T2 forward-biased.

ORDERING INFORMATION

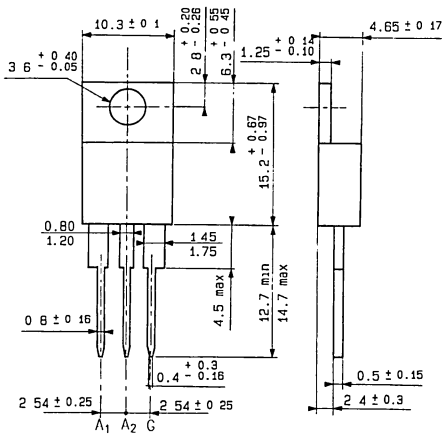
RBO **40** - **40** **T**

- **RBO**: Reversed Battery & Overvolage protection
- **40**: $I_{F(AV)}$ = 40 A
- **40**: V_{CL} = 40V
- **T**: Packages : T = TO 220 AB, M = SOP 10 (Power SO) *

* To be announced later on

PACKAGE MECHANICAL DATA (in millimeters)

TO 220 AB Plastic



Cooling method : C
Marking : type number
Weight : 2 g
Polarity : N A
Stud torque : N A

SGS-THOMSON MICROELECTRONICS

SM4T6V8,A/220,A
SM4T6V8C,CA/220C,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 400 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 220 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to V_{BR}).
- JEDEC REGISTRED.

SOD 6
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them praticularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Full compatibility with both gluing and paste soldering technologies.
- Excellent on board stability.
- Tinned copper leads.
- High temperature resistant resin.

ABSOLUTE RATINGS (limiting values)

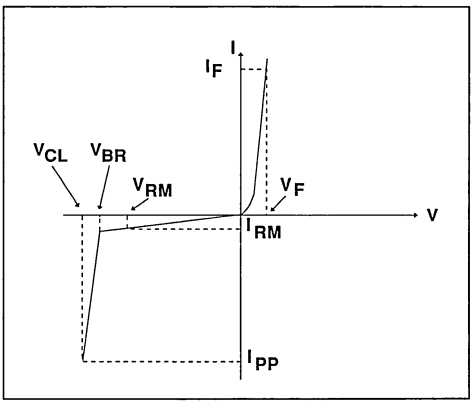
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	400	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 50°C	5	W
I_{FSM}	Non repetitive surge peak forward current. For unidirectional types.	Tamb = 25°C t =10 ms	50	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	20	°C/W
R_{th} (j-a)	Junction to ambiant. on printed circuit. With standard footprint dimensions.	100	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop $V_F < 3.5V$ @ $I_F = 25$ A.

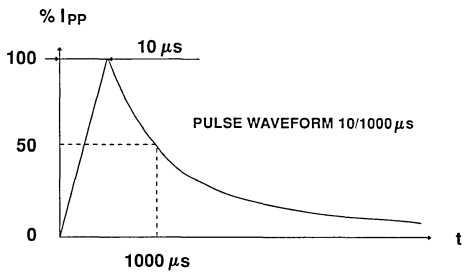


TYPES				I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Uni directional	*	Bi directional	*	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM4T6V8	QD	SM4T6V8C	VD	1000	5.8	6.45	6.8	7.48	10	10.5	38	13.4	174	5.7	3500
SM4T6V8A	QE	SM4T6V8CA	VE	1000	5.8	6.45	6.8	7.14	10	10.5	38	13.4	174	5.7	3500
SM4T7V5	QF	SM4T7V5C	VF	500	6.4	7.13	7.5	8.25	10	11.3	35.4	14.5	160	6.1	3100
SM4T7V5A	QG	SM4T7V5CA	VG	500	6.4	7.13	7.5	7.88	10	11.3	35.4	14.5	160	6.1	3100
SM4T10	QN	SM4T10C	VN	10	8.55	9.5	10	11	1	14.5	27.6	18.6	124	7.3	2000
SM4T10A	QP	SM4T10CA	VP	10	8.55	9.5	10	10.5	1	14.5	27.6	18.6	124	7.3	2000
SM4T12	QS	SM4T12C	VS	5	10.2	11.4	12	13.2	1	16.7	24	21.7	106	7.8	1550
SM4T12A	QT	SM4T12CA	VT	5	10.2	11.4	12	12.6	1	16.7	24	21.7	106	7.8	1550
SM4T15	QW	SM4T15C	VW	5	12.8	14.3	15	16.5	1	21.2	19	27.2	85	8.4	1200
SM4T15A	QX	SM4T15CA	VX	5	12.8	14.3	15	15.8	1	21.2	19	27.2	85	8.4	1200
SM4T18	RD	SM4T18C	UD	5	15.3	17.1	18	19.8	1	25.2	16	32.5	71	8.8	975
SM4T18A	RE	SM4T18CA	UE	5	15.3	17.1	18	18.9	1	25.2	16	32.5	71	8.8	975
SM4T22	RH	SM4T22C	UH	5	18.8	20.9	22	24.2	1	30.6	13	39.3	59	9.2	800
SM4T22A	RK	SM4T22CA	UK	5	18.8	20.9	22	23.1	1	30.6	13	39.3	59	9.2	800
SM4T24	RL	SM4T24C	UL	5	20.5	22.8	24	26.4	1	33.2	12	42.8	54	9.4	725
SM4T24A	RM	SM4T24CA	UM	5	20.5	22.8	24	25.2	1	33.2	12	42.8	54	9.4	725
SM4T27	RN	SM4T27C	UN	5	23.1	25.7	27	29.7	1	37.5	10.7	48.3	48	9.6	625
SM4T27A	RP	SM4T27CA	UP	5	23.1	25.7	27	28.4	1	37.5	10.7	48.3	48	9.6	625
SM4T30	RQ	SM4T30C	UQ	5	25.6	28.5	30	33	1	41.5	9.6	53.5	43	9.7	575
SM4T30A	RR	SM4T30C4	UR	5	25.6	28.5	30	31.5	1	41.5	9.6	53.5	43	9.7	575
SM4T33	RS	SM4T33C	US	5	28.2	31.4	33	36.3	1	45.7	8.8	59.0	39	9.8	510
SM4T33A	RT	SM4T33CA	UT	5	28.2	31.4	33	34.7	1	45.7	8.8	59.0	39	9.8	510
SM4T36	RU	SM4T36C	UU	5	30.8	34.2	36	39.6	1	49.9	8	64.3	36	9.9	480
SM4T36A	RV	SM4T36CA	UV	5	30.8	34.2	36	37.8	1	49.9	8	64.3	36	9.9	480
SM4T39	RW	SM4T39C	UW	5	33.3	37.1	39	42.9	1	53.9	7.4	69.7	33	10.0	450
SM4T39	RX	SM4T39	UX	5	33.3	37.1	39	41.0	1	53.9	7.4	69.7	33	10.0	450

TYPES				I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Uni directional	*	Bi directional	*	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM4T68	SN	SM4T68C	WN	5	58.1	64.6	68	74.8	1	92	4.3	121	19	10.4	270
SM4T68A	SP	SM4T68CA	WP	5	58.1	64.6	68	71.4	1	92	4.3	121	19	10.4	270
SM4T100	SW	SM4T100C	WW	5	85.5	95.0	100	110	1	137	2.9	178	13	10.6	200
SM4T100A	SX	SM4T100CA	WX	5	85.5	95.0	100	105	1	137	2.9	178	13	10.6	200
SM4T150	TH	SM4T150C	XH	5	128	143	150	165	1	207	2.0	265	9	10.8	145
SM4T150A	TK	SM4T150CA	XK	5	128	143	150	158	1	207	2.0	265	9	10.8	145
SM4T200	TS	SM4T200C	XS	5	171	190	200	220	1	274	1.5	353	6.5	10.8	120
SM4T200A	TT	SM4T200CA	XT	5	171	190	200	210	1	274	1.5	353	6.5	10.8	120
SM4T220	TU	SM4T220C	XU	5	188	209	220	242	1	328	1.4	388	6	10.8	110
SM4T220A	TV	SM4T220CA	XV	5	188	209	220	231	1	328	1.4	388	6	10.8	110

All parameters tested at 25 °C, except where indicated.

*** = Marking**



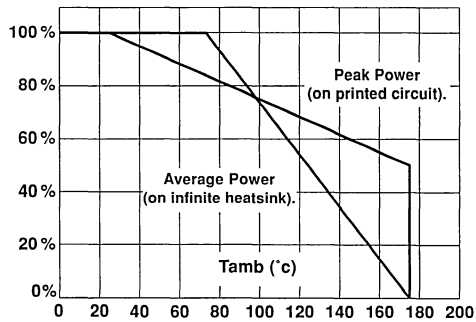


Figure 1: Power dissipation derating versus ambient temperature

Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Note 2 : Pulse test. $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.

Figure 2 : Peak pulse power versus exponential pulse duration.

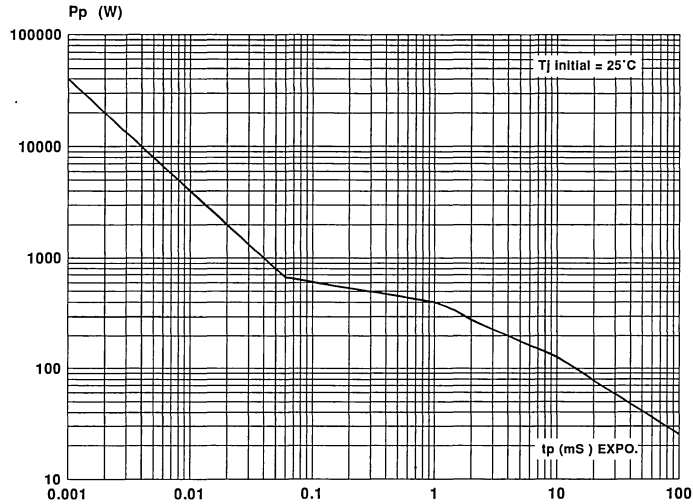
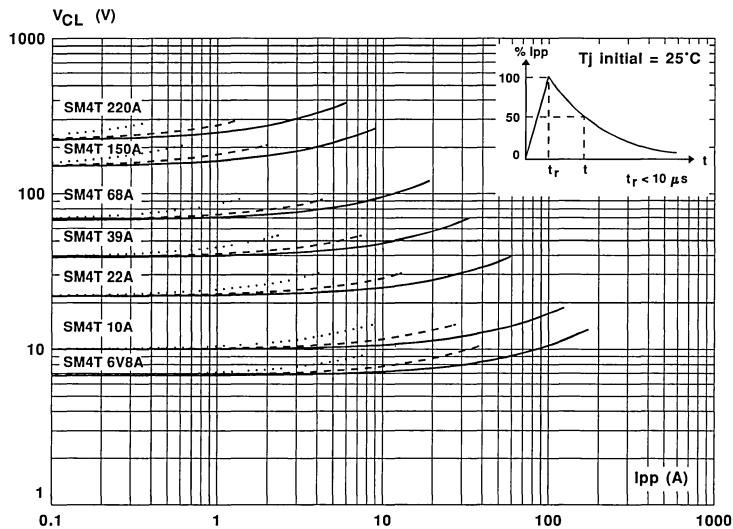


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} * [T_a - 25] * V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

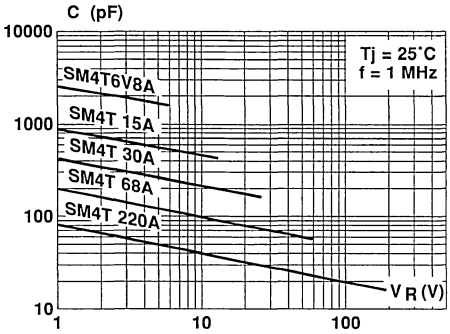


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

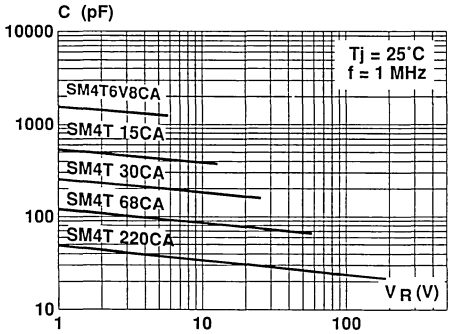


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

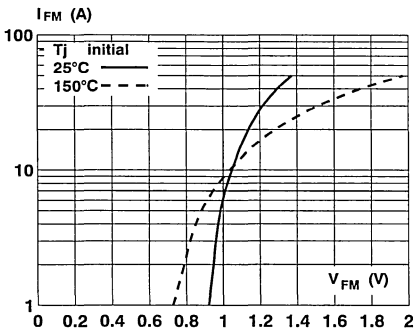
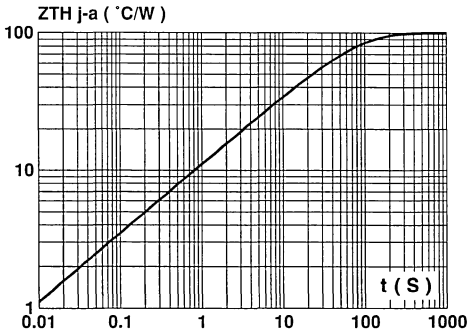
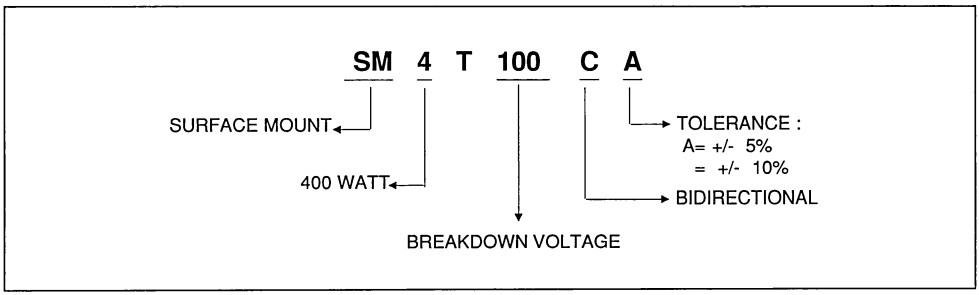


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with standard footprint dimensions.



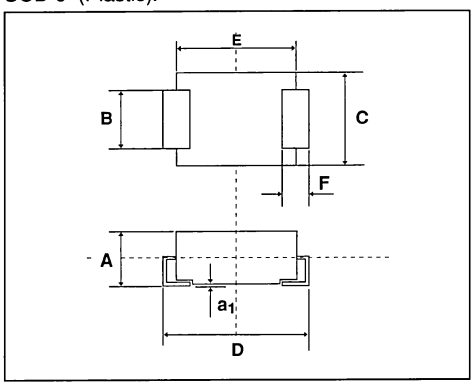
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

SOD 6 (Plastic).

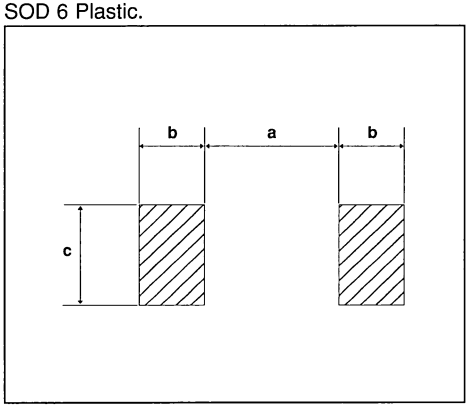


Ref	Millimeters		Inches	
	min	max	min	max
A	2.48	2.61	0.096	0.103
a1	0.10	0.20	0.004	0.008
B	1.96	2.11	0.077	0.083
C	3.65	3.93	0.143	0.155
D	5.39	5.59	0.212	0.220
E	4.15	4.30	0.163	0.170
F	1.00	1.27	0.039	0.050

Weight = 0.12 g.

FOOTPRINT DIMENSIONS (Millimeter).

SOD 6 Plastic.



Ref	Millimeters
a	2.75
b	1.52
c	2.30

Packaging : standard packaging is in film.

SGS-THOMSON MICROELECTRONICS

SM6T6V8,A/220,A
SM6T6V8C,CA/220C,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 600 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 220 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).
- JEDEC REGISTRED.

SOD 6
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Full compatibility with both gluing and paste soldering technologies.
- Excellent on board stability.
- Tinned copper leads.
- High temperature resistant resin.

ABSOLUTE RATINGS (limiting values)

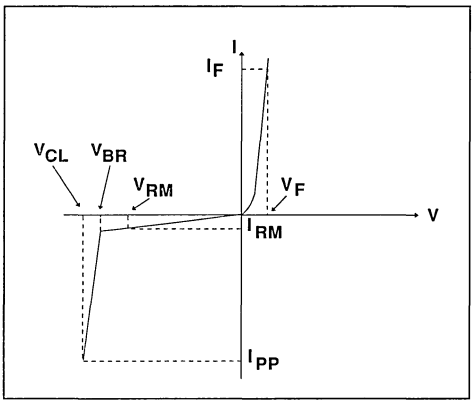
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	600	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 50°C	5	W
I_{FSM}	Non repetitive surge peak forward current. For unidirectional types.	Tamb = 25°C t =10 ms	100	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	20	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. With standard footprint dimensions.	100	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop $V_F < 3.5V$ @ $I_F = 50$ A.

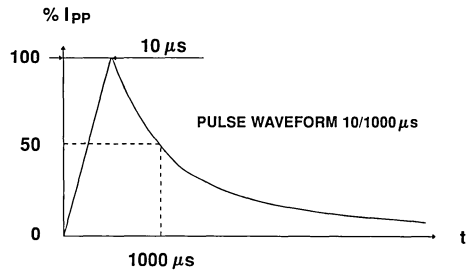


TYPES				I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Uni directional	*	Bi directional	*	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM6T6V8	DD	SM6T6V8C	LD	1000	5.8	6.45	6.8	7.48	10	10.5	57	13.4	298	5.7	4000
SM6T6V8A	DE	SM6T6V8CA	LE	1000	5.8	6.45	6.8	7.14	10	10.5	57	13.4	298	5.7	4000
SM6T7V5	DF	SM6T7V5C	LF	500	6.4	7.13	7.5	8.25	10	11.3	53	14.5	276	6.1	3700
SM6T7V5A	DG	SM6T7V5CA	LG	500	6.4	7.13	7.5	7.88	10	11.3	53	14.5	276	6.1	3700
SM6T10	DN	SM6T10C	LN	10	8.55	9.5	10	11	1	14.5	41	18.6	215	7.3	2800
SM6T10A	DP	SM6T10CA	LP	10	8.55	9.5	10	10.5	1	14.5	41	18.6	215	7.3	2800
SM6T12	DS	SM6T12C	LS	5	10.2	11.4	12	13.2	1	16.7	36	21.7	184	7.8	2300
SM6T12A	DT	SM6T12CA	LT	5	10.2	11.4	12	12.6	1	16.7	36	21.7	184	7.8	2300
SM6T15	DW	SM6T15C	LW	5	12.8	14.3	15	16.5	1	21.2	28	27.2	147	8.4	1900
SM6T15A	DX	SM6T15CA	LX	5	12.8	14.3	15	15.8	1	21.2	28	27.2	147	8.4	1900
SM6T18	ED	SM6T18C	MD	5	15.3	17.1	18	19.8	1	25.2	24	32.5	123	8.8	1600
SM6T18A	EE	SM6T18CA	ME	5	15.3	17.1	18	18.9	1	25.2	24	32.5	123	8.8	1600
SM6T22	EH	SM6T22C	MH	5	18.8	20.9	22	24.2	1	30.6	20	39.3	102	9.2	1350
SM6T22A	EK	SM6T22CA	MK	5	18.8	20.9	22	23.1	1	30.6	20	39.3	102	9.2	1350
SM6T24	EL	SM6T24C	ML	5	20.5	22.8	24	26.4	1	33.2	18	42.8	93	9.4	1250
SM6T24A	EM	SM6T24CA	MM	5	20.5	22.8	24	25.2	1	33.2	18	42.8	93	9.4	1250
SM6T27	EN	SM6T27C	MN	5	23.1	25.7	27	29.7	1	37.5	16	48.3	83	9.6	1150
SM6T27A	EP	SM6T27CA	MP	5	23.1	25.7	27	28.4	1	37.5	16	48.3	83	9.6	1150
SM6T30	EQ	SM6T30C	MQ	5	25.6	28.5	30	33	1	41.5	14.5	53.5	75	9.7	1075
SM6T30A	ER	SM6T30CA	MR	5	25.6	28.5	30	31.5	1	41.5	14.5	53.5	75	9.7	1075
SM6T33	ES	SM6T33C	MS	5	28.2	31.4	33	36.3	1	45.7	13.1	59.0	68	9.8	1000
SM6T33A	ET	SM6T33CA	MT	5	28.2	31.4	33	34.7	1	45.7	13.1	59.0	68	9.8	1000
SM6T36	EU	SM6T36C	MU	5	30.8	34.2	36	39.6	1	49.9	12	64.3	62	9.9	950
SM6T36A	EV	SM6T36CA	MV	5	30.8	34.2	36	37.8	1	49.9	12	64.3	62	9.9	950
SM6T39	EW	SM6T39C	MW	5	33.3	37.1	39	42.9	1	53.9	11.1	69.7	57	10.0	900
SM6T39	EX	SM6T39	MX	5	33.3	37.1	39	41.0	1	53.9	11.1	69.7	57	10.0	900

TYPES				I_{RM} @ V_{RM}		V_{BR} @ I_R				V_{CL} @ I_{PP}		V_{CL} @ I_{PP}		αT	C
				max		min	nom	max		max		max		max	typ
						note2				10/1000µs		8/20µs		note3	note4
Uni directional	*	Bi directional	*	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM6T68	FP	SM6T68C	NP	5	58.1	64.6	68	74.8	1	92	6.5	121	33	10.4	625
SM6T68A	FQ	SM6T68CA	NQ	5	58.1	64.6	68	71.4	1	92	6.5	121	33	10.4	625
SM6T100	FX	SM6T100C	NX	5	85.5	95.0	100	110	1	137	4.4	178	22.5	10.6	500
SM6T100A	FY	SM6T100CA	NY	5	85.5	95.0	100	105	1	137	4.4	178	22.5	10.6	500
SM6T150	GK	SM6T150C	OK	5	128	143	150	165	1	207	2.9	265	15	10.8	400
SM6T150A	GL	SM6T150CA	OL	5	128	143	150	158	1	207	2.9	265	15	10.8	400
SM6T200	GT	SM6T200C	OT	5	171	190	200	220	1	274	2.2	353	11.3	10.8	350
SM6T200A	GU	SM6T200CA	OU	5	171	190	200	210	1	274	2.2	353	11.3	10.8	350
SM6T220	GV	SM6T220C	OV	5	188	209	220	242	1	328	2	388	10.3	10.8	330
SM6T220A	GW	SM6T220CA	OW	5	188	209	220	231	1	328	2	388	10.3	10.8	330

All parameters tested at 25 °C, except where indicated.

*** = Marking**



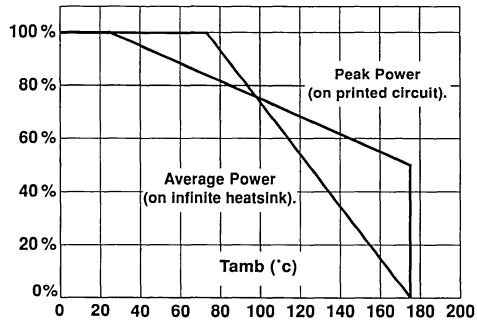


Figure 1: Power dissipation derating versus ambient temperature

Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Note 2 : Pulse test: $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.

Figure 2 : Peak pulse power versus exponential pulse duration.

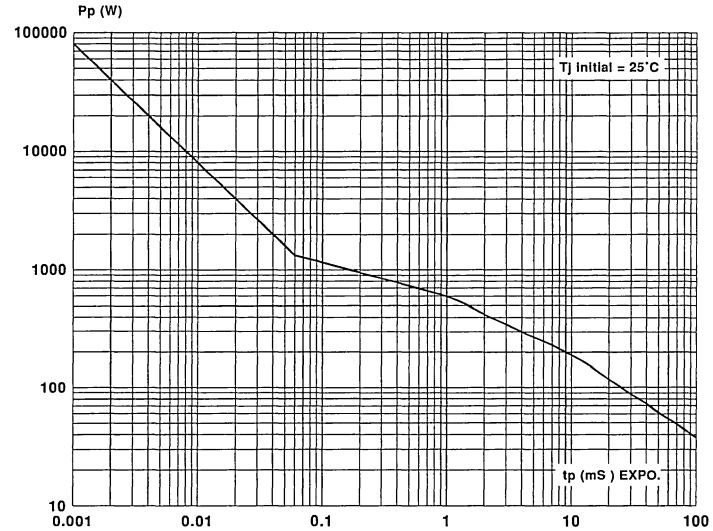
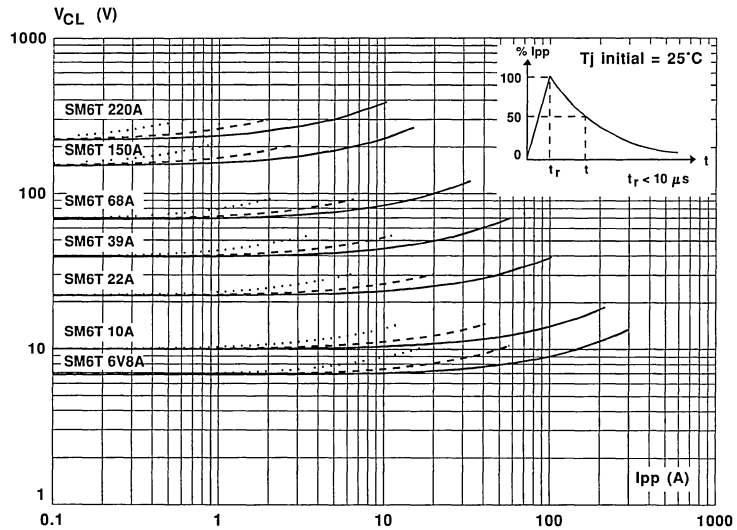


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} * [T_a - 25] * V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

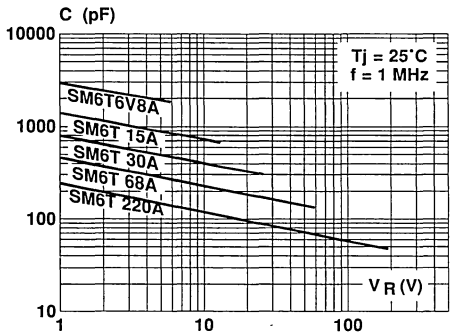


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

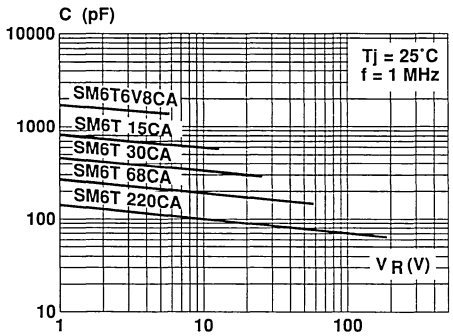


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

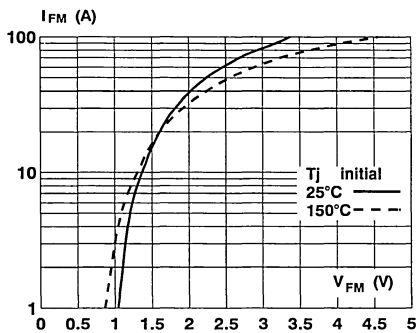
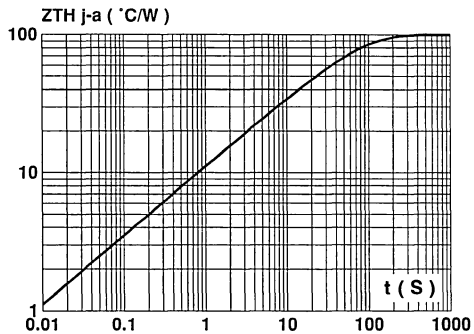
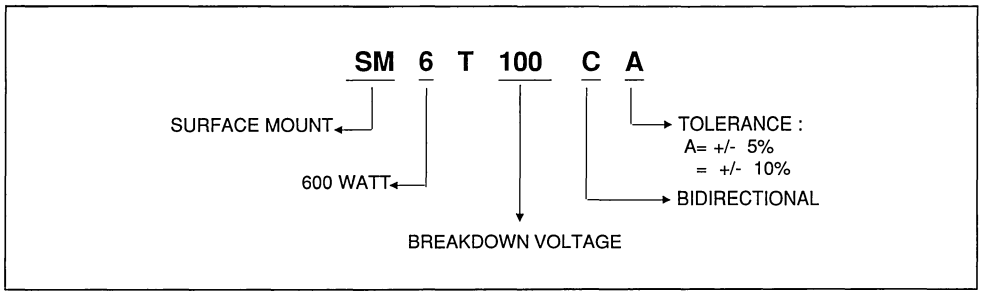


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with standard footprint dimensions.



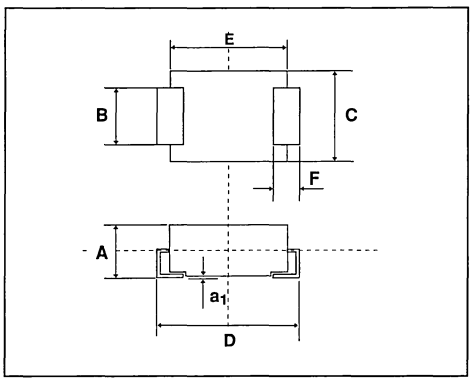
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

SOD 6 (Plastic).

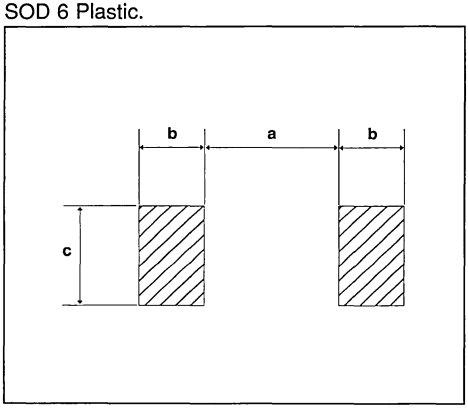


Ref	Millimeters		Inches	
	min	max	min	max
A	2.48	2.61	0.096	0.103
a1	0.10	0.20	0.004	0.008
B	1.96	2.11	0.077	0.083
C	3.65	3.93	0.143	0.155
D	5.39	5.59	0.212	0.220
E	4.15	4.30	0.163	0.170
F	1.00	1.27	0.039	0.050

Weight = 0.12 g.

FOOTPRINT DIMENSIONS (Millimeter).

SOD 6 Plastic.



Ref	Millimeters
a	2.75
b	1.52
c	2.30

Packaging : standard packaging is in film.

SGS-THOMSON MICROELECTRONICS

SM15T6V8,A/220,A
SM15T6V8C,CA/220C,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 1500 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 220 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).

SOD 15
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code, and Cathode Band (for unidirectional types only).
- Full compatibility with both gluing and paste soldering technologies.
- Excellent on board stability.
- Tinned copper leads.
- High temperature resistant resin.

ABSOLUTE RATINGS (limiting values)

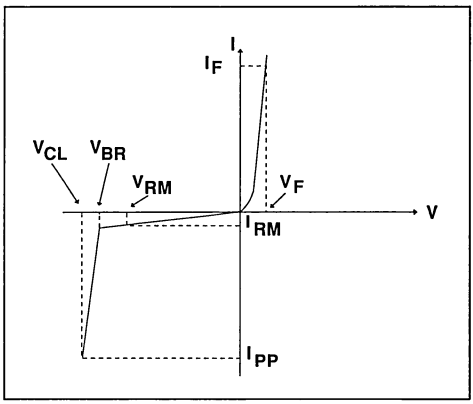
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	1500	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 50°C	10	W
I_{FSM}	Non repetitive surge peak forward current. For unidirectional types.	Tamb = 25°C t =10 ms	250	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	10	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. With standard footprint dimensions.	75	°C/W

ELECTRICAL CHARACTERISTICS

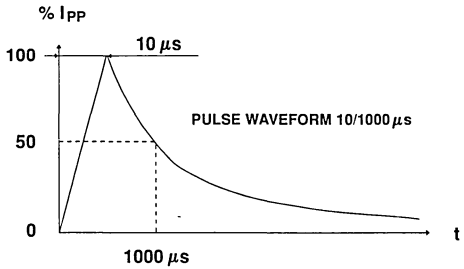
Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 100 A.



TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Uni directional	Bi directional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM15T6V8	SM15T6V8C	1000	5.8	6.45	6.8	7.48	10	10.5	143	13.4	746	5.7	9500
SM15T6V8A	SM15T6V8CA	1000	5.8	6.45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
SM15T7V5	SM15T7V5C	500	6.4	7.13	7.5	8.25	10	11.3	132	14.5	690	6.1	8500
SM15T7V5A	SM15T7V5CA	500	6.4	7.13	7.5	7.88	10	11.3	132	14.5	690	6.1	8500
SM15T10	SM15T10C	10	8.55	9.5	10	11.0	1	14.5	103	18.6	538	7.3	7000
SM15T10A	SM15T10CA	10	8.55	9.5	10	10.5	1	14.5	103	18.6	538	7.3	7000
SM15T12	SM15T12C	5	10.2	11.4	12	13.2	1	16.7	90	21.7	461	7.8	6000
SM15T12A	SM15T12CA	5	10.2	11.4	12	12.6	1	16.7	90	21.7	461	7.8	6000
SM15T15	SM15T15C	5	12.8	14.3	15	16.5	1	21.2	71	27.2	368	8.4	5000
SM15T15A	SM15T15CA	5	12.8	14.3	15	15.8	1	21.2	71	27.2	368	8.4	5000
SM15T18	SM15T18C	5	15.3	17.1	18	19.8	1	25.2	59.5	32.5	308	8.8	4300
SM15T18A	SM15T18CA	5	15.3	17.1	18	18.9	1	25.2	59.5	32.5	308	8.8	4300
SM15T22	SM15T22C	5	18.8	20.9	22	24.2	1	30.6	49	39.3	254	9.2	3700
SM15T22A	SM15T22CA	5	18.8	20.9	22	23.1	1	30.6	49	39.3	254	9.2	3700
SM15T24	SM15T24C	5	20.5	22.8	24	26.4	1	33.2	45	42.8	234	9.4	3500
SM15T24A	SM15T24CA	5	20.5	22.8	24	25.2	1	33.2	45	42.8	234	9.4	3500
SM15T27	SM15T27C	5	23.1	25.7	27	29.7	1	37.5	40	48.3	207	9.6	3200
SM15T27A	SM15T27CA	5	23.1	25.7	27	28.4	1	37.5	40	48.3	207	9.6	3200
SM15T30	SM15T30C	5	25.6	28.5	30	33.0	1	41.5	36	53.5	187	9.7	2900
SM15T30A	SM15T30CA	5	25.6	28.5	30	31.5	1	41.5	36	53.5	187	9.7	2900
SM15T33	SM15T33C	5	28.2	31.4	33	36.3	1	45.7	33	59.0	169	9.8	2700
SM15T33A	SM15T33CA	5	28.2	31.4	33	34.7	1	45.7	33	59.0	169	9.8	2700
SM15T36	SM15T36C	5	30.8	34.2	36	39.6	1	49.9	30	64.3	156	9.9	2500
SM15T36A	SM15T36CA	5	30.8	34.2	36	37.8	1	49.9	30	64.3	156	9.9	2500
SM15T39	SM15T39C	5	33.3	37.1	39	42.9	1	53.9	28	69.7	143	10.0	2400
SM15T39	SM15T39	5	33.3	37.1	39	41.0	1	53.9	28	69.7	143	10.0	2400

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Uni directional	Bi directional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM15T68	SM15T68C	5	58.1	64.6	68	74.8	1	92	16.3	121	83	10.4	1550
SM15T68A	SM15T68CA	5	58.1	64.6	68	71.4	1	92	16.3	121	83	10.4	1550
SM15T100	SM15T100C	5	85.5	95.0	100	110	1	137	11	178	56	10.6	1150
SM15T100A	SM15T100CA	5	85.5	95.0	100	105	1	137	11	178	56	10.6	1150
SM15T150	SM15T150C	5	128	143	150	165	1	207	7.2	265	38	10.8	850
SM15T150A	SM15T150CA	5	128	143	150	158	1	207	7.2	265	38	10.8	850
SM15T200	SM15T200C	5	171	190	200	220	1	274	5.5	353	28	10.8	675
SM15T200A	SM15T200CA	5	171	190	200	210	1	274	5.5	353	28	10.8	675
SM15T220	SM15T220C	5	188	209	220	242	1	328	4.6	388	26	10.8	625
SM15T220A	SM15T220CA	5	188	209	220	231	1	328	4.6	388	26	10.8	625

All parameters tested at 25 °C, except where indicated.



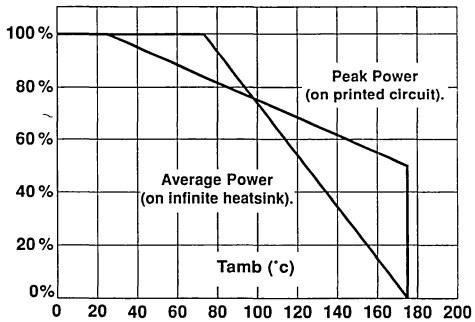


Figure 1: Power dissipation derating versus ambient temperature

Note 1 : - For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.
Note 2 : - Pulse test. $T_P < 50$ ms.
Note 3 : - $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.
Note 4 : - VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.

TYPES		TYPES		TYPES		TYPES	
Unidirectional	Marking	Bidirectional	Marking	Unidirectional	Marking	Bidirectional	Marking
SM15T6V8	MDD	SM15T6V8C	BDD	SM15T30	MEQ	SM15T30C	BEQ
SM15T6V8A	MDE	SM15T6V8CA	BDE	SM15T30A	MER	SM15T30CA	BER
SM15T7V5	MDF	SM15T7V5C	BDF	SM15T33	MES	SM15T33C	BES
SM15T7V5A	MDG	SM15T7V5CA	BDG	SM15T33A	MET	SM15T33CA	BET
SM15T10	MDN	SM15T10C	BDN	SM15T36	MEU	SM15T36C	BEU
SM15T10A	MDP	SM15T10CA	BDP	SM15T36A	MEV	SM15T36CA	BEV
SM15T12	MDS	SM15T12C	BDS	SM15T39	MEW	SM15T39C	BEW
SM15T12A	MDT	SM15T12CA	BDT	SM15T39A	MEX	SM15T39CA	BEX
SM15T15	MDW	SM15T15C	BDW	SM15T68	MFN	SM15T68C	BFN
SM15T15A	MDX	SM15T15CA	BDX	SM15T68A	MFP	SM15T68CA	BFP
SM15T18	MED	SM15T18C	BED	SM15T100	MFW	SM15T100C	BFW
SM15T18A	MEE	SM15T18CA	BEE	SM15T100A	MFX	SM15T100CA	BFX
SM15T22	MEH	SM15T22C	BEH	SM15T150	MGH	SM15T150C	BGH
SM15T22A	MEK	SM15T22CA	BEK	SM15T150A	MGK	SM15T150CA	BGK
SM15T24	MEL	SM15T24C	BEL	SM15T200	MGU	SM15T200C	BGU
SM15T24A	MEM	SM15T24CA	BEM	SM15T200A	MGV	SM15T200CA	BGV
SM15T27	MEN	SM15T27C	BEN	SM15T220	MGW	SM15T220C	BGW
SM15T27A	MEP	SM15T27CA	BEP	SM15T220A	MGVX	SM15T220CA	BGX

Figure 2 : Peak pulse power versus exponential pulse duration.

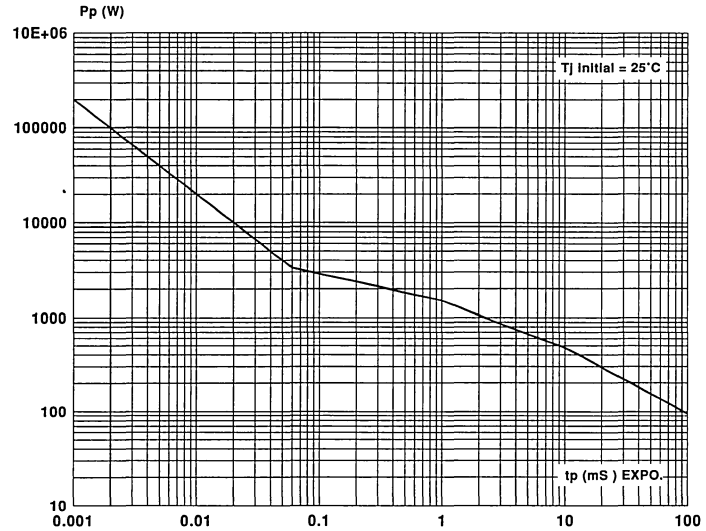
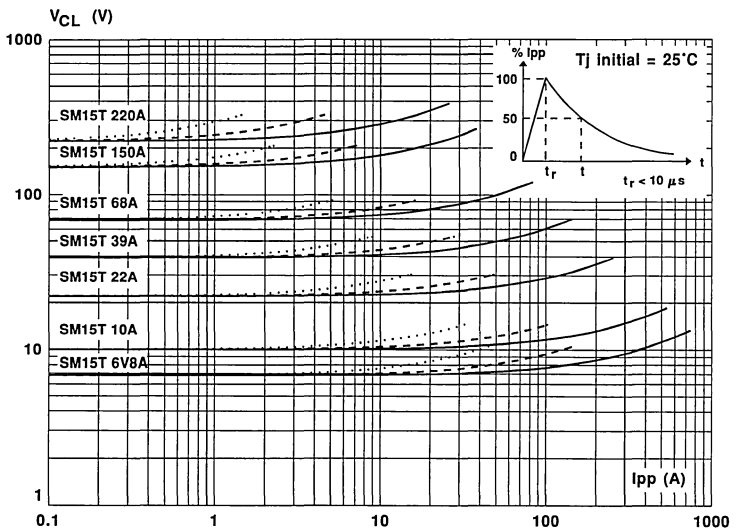


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} \cdot [T_a - 25] \cdot V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

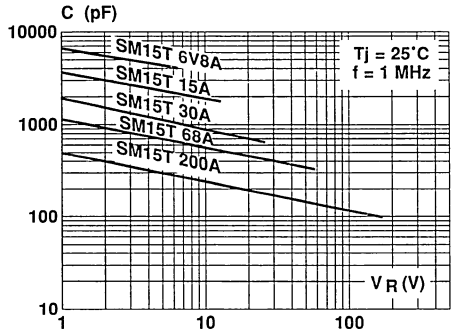


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

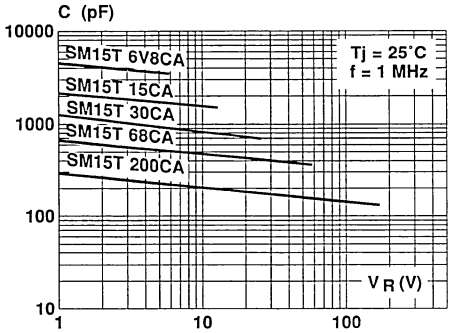


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

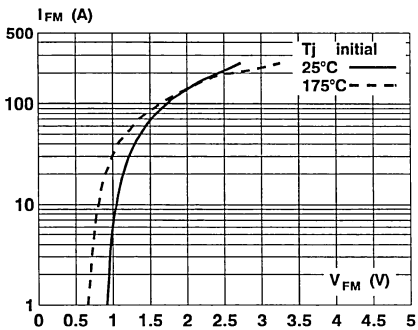
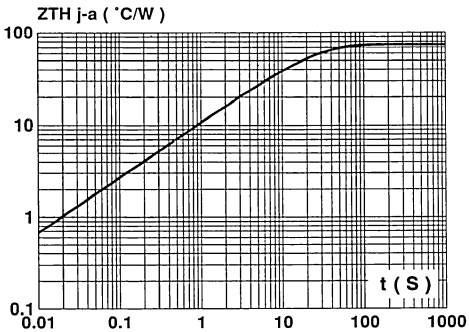
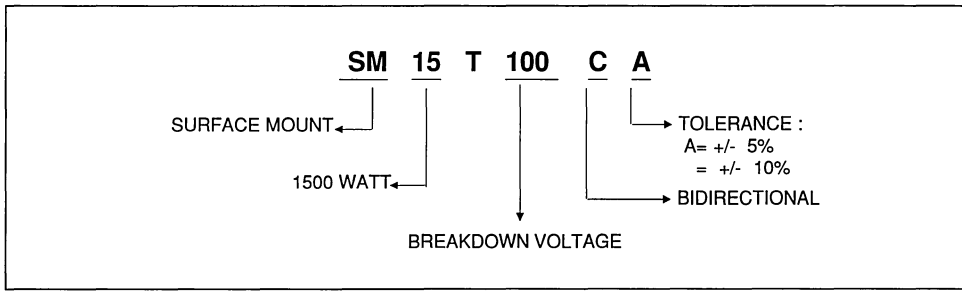


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with standard footprint dimensions.



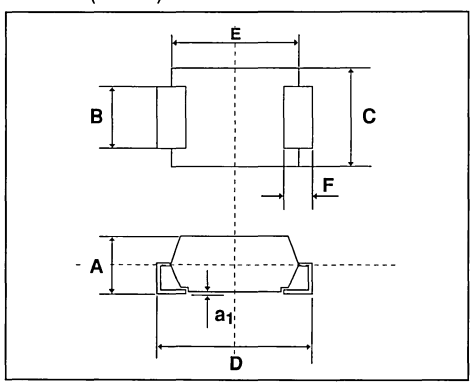
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

SOD 15 (Plastic).

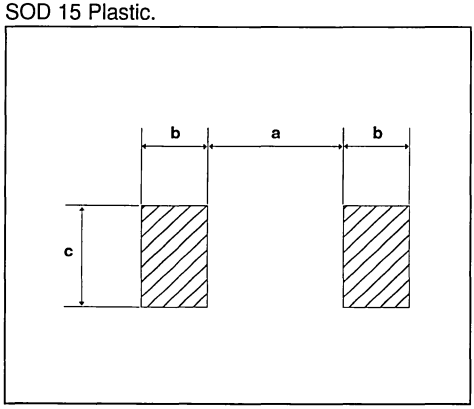


Ref	Millimeters		Inches	
	min	max	min	max
A	2.5	3.1	0.098	0.122
a1	-	0.2	-	0.008
B	2.9	3.1	0.114	0.122
C	4.8	5.2	0.190	0.200
D	7.6	8.0	0.300	0.315
E	6.3	6.6	0.248	0.259
F	1.3	1.7	0.051	0.067

Weight = 0.25 g.

FOOTPRINT DIMENSIONS (Millimeter).

SOD 15 Plastic.



Ref	Millimeters
a	4.2
b	2
c	3.3

Packaging : standard packaging is in film.

SGS-THOMSON MICROELECTRONICS

STGP10N50A

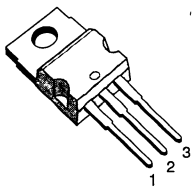
ISOLATED GATE BIPOLAR TRANSISTOR (IGBT)

PRELIMINARY DATA

- HIGH INPUT IMPEDANCE (VOLTAGE DRIVEN)
- VERY LOW ON-VOLTAGE DROP $V_{CE(SAT)}$
- HIGH RELIABILITY LEVEL
- HIGH CURRENT CAPABILITY
- OFF LOSSES INCLUDE TAIL CURRENT

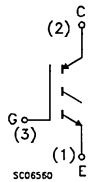
APPLICATIONS:

- AUTOMOTIVE IGNITION
- LIGHT DIMMER
- S.M.P.S. SOFT START



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CES}	Collector-Emitter Voltage (V_{GE} = 0)	500	V
V_{CER}	Collector-Emitter Voltage (R_{GE}= 20 kΩ)	500	V
V_{GE}	Gate-Emitter Voltage	± 20	V
I_C	Collector Current (continuous) at T_c = 25 °C	20	A
I_C	Collector Current (continuous) at T_c = 100 °C	10	A
I_{CM}(•)	Collector Current (pulsed)	100	A
P_{tot}	Total Dissipation at T_c = 25 °C	100	W
	Derating Factor	0.8	W/°C
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-Case	Max	1.25	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-Ambient	Max	62.5	°C/W
$R_{thc\text{-}h}$	Thermal Resistance Case-Heartsink	Max	0.1	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-Emitter Breakdown Voltage	I_C = 250 µA V_{GE} = 0	500			V
I_{CES}	Collector Cut-off Current (V_{GE} = 0)	V_{CE} = Max Rating V_{CE} = Max Rating x 0.8 T_j = 125 °C			250 1	µA mA
I_{GES}	Gate-Emitter Leakage Current (V_{CE} = 0)	V_{GE} = ± 20 V V_{CE} = 0			100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GE(th)}$	Gate Threshold Voltage	V_{CE} = V_{GE} I_C = 250 µA	2		4	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	V_{GE} = 15 V I_C = 10 A V_{GE} = 15 V I_C = 10 A T_j = 100 °C		1.85 1.75	 2.2	V V

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward Transconductance	V_{CE} = 20 V I_C = 10 A	2.5	6		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{CE} = 25 V f = 1 MHz V_{GE} = 0		900 90 30	1250 140 42	pF pF pF
Q_g	Gate Charge	V_{CE} = 400 V V_{GE} = 15 V I_C = 10 A		55		nC

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	I_C = 10 A V_{CC} = 400 V V_{GE} = 15 V R_{GE} = 100 Ω		35 100	50 150	ns ns
dI_C/dt	Turn-on Current Slope	I_C = 10 A V_{CC} = 400 V V_{GE} = 15 V R_{GE} = 100 Ω T_j = 100 °C		220		A/ms
E_{on}	Turn-on Switching Losses	I_C = 10 A V_{CC} = 400 V V_{GE} = 15 V R_{GE} = 100 Ω T_j = 100 °C		185	220	µJ
$V_{CE(350ms)}$	Collector-Emitter Dynamic Voltage	I_C = 10 A V_{CC} = 400 V V_{GE} = 15 V R_{GE} = 100 Ω T_j = 100 °C			7	V
$V_{CE(610ms)}$	Collector-Emitter Dynamic Voltage	I_C = 10 A V_{CC} = 400 V V_{GE} = 15 V R_{GE} = 100 Ω T_j = 100 °C			4	V

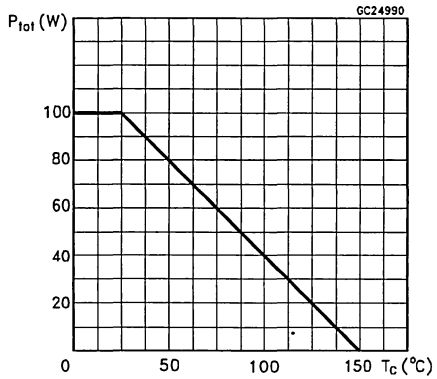
ELECTRICAL CHARACTERISTICS (continued)

SWITCHING OFF

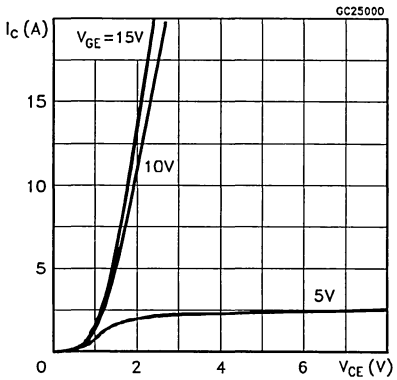
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_c	Cross-Over Time	V_{CC} = 400 V I_C = 10 A		1500		ns
$t_{r(Voff)}$	Off Voltage Rise Time	R_{GE} = 100 Ω V_{GE} = 15 V		170		ns
t_f	Fall Time			1000		ns
E_{off} (**)	Turn-off Switching Loss			2.2	3.25	mJ
t_c	Cross-Over Time	V_{CC} = 400 V I_C = 10 A		2600		ns
$t_{r(Voff)}$	Off Voltage Rise Time	R_{GE} = 100 Ω V_{GE} = 15 V		190		ns
t_f	Fall Time	T_j = 100 °C		2000		ns
E_{off} (**)	Turn-off Switching Loss			3.8	4.8	mJ

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(**) Losses include olso the tail (Jedec Standardization)

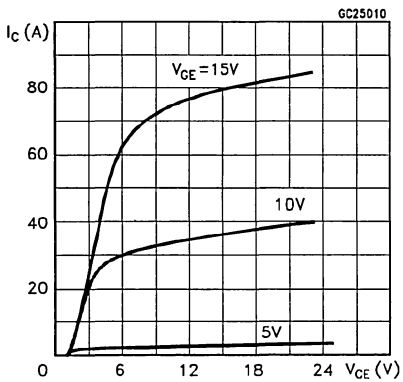
Derating Curves



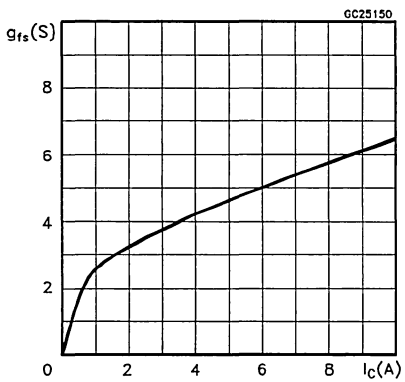
Output Characteristics



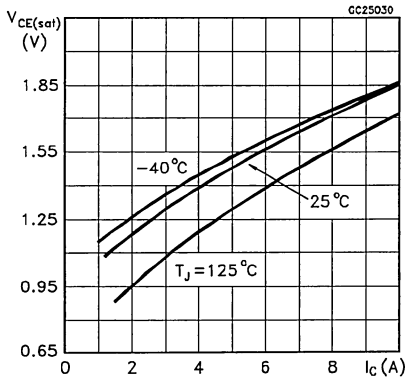
Output Characteristics



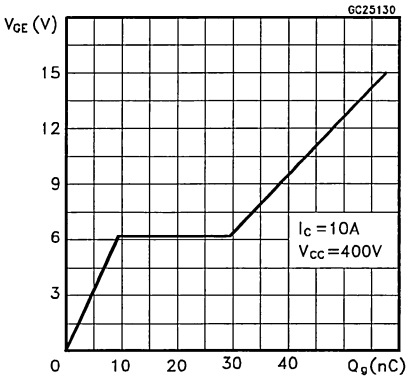
Transconductance



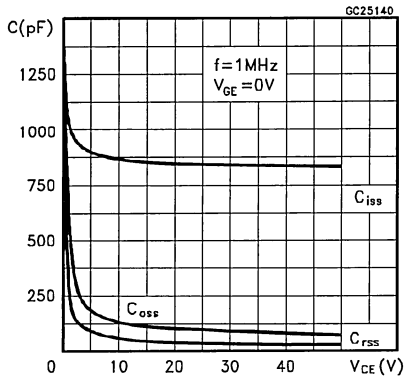
Static Collector-Emitter On Voltage



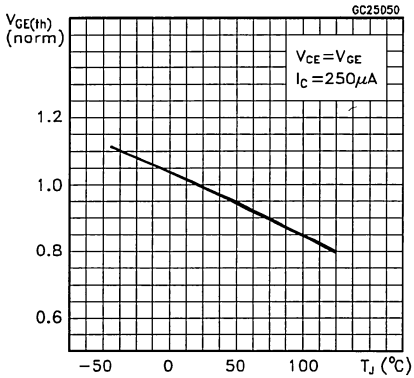
Gate Charge vs Gate-Emitter Voltage



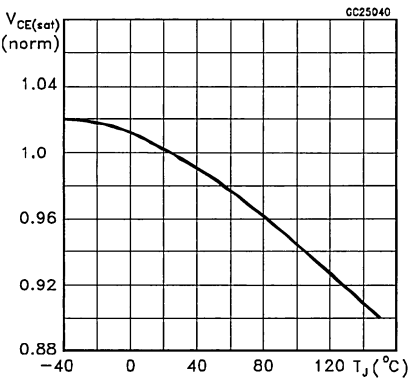
Capacitance Variation



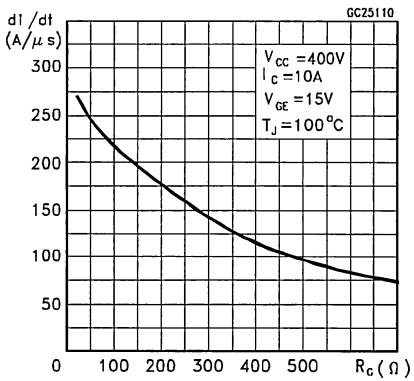
Normalized Gate Threshold Voltage vs Temperature



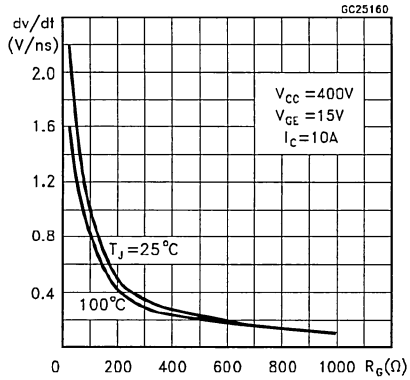
Normalized On Voltage vs Temperature



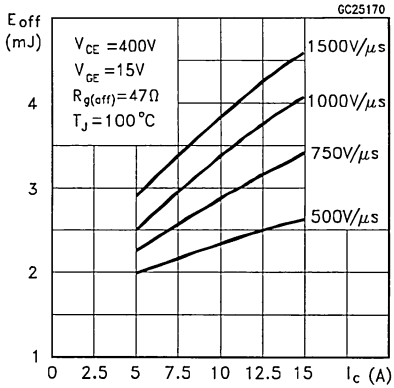
Turn On Current Slope vs Gate-Emitter Resistance



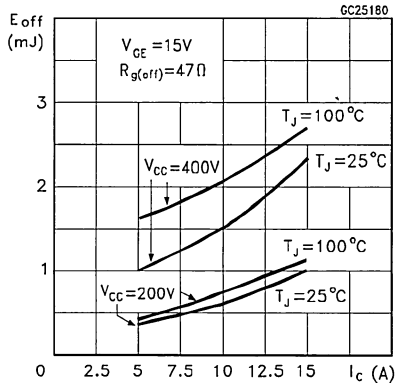
Turn Off Voltage Slope vs Gate-Emitter Resistance



Off Loses vs dv/dt



Off Loses vs Junction Temperature and Supply Voltage



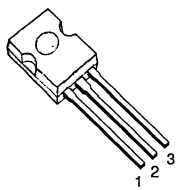
SGS-THOMSON MICROELECTRONICS

STK12N05L
STK12N06L

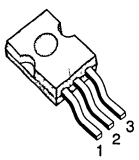
N - CHANNEL ENHANCEMENT MODE LOW THRESHOLD POWER MOS TRANSISTOR

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STK12N05L	50 V	0.15 Ω	12 A
STK12N06L	60 V	0.15 Ω	12 A

- AVALANCHE RUGGEDNESS TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- LOGIC LEVEL COMPATIBLE INPUT
- APPLICATION ORIENTED CHARACTERIZATION



SOT-82

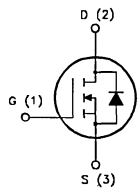


SOT-194 (option)

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STK12N05L	STK12N06L	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	50	60	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	50	60	V
V_{GS}	Gate-source Voltage	± 15		V
I_D	Drain Current (continuous) at T_c = 25 °C	12		A
I_D	Drain Current (continuous) at T_c = 100 °C	7		A
I_{DM}(•)	Drain Current (pulsed)	48		A
P_{tot}	Total Dissipation at T_c = 25 °C	50		W
	Derating Factor	0.4		W/°C
T_{stg}	Storage Temperature	-65 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.5	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.7	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0 for **STK12N05L** for **STK12N06L**	 50 60			 V V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125 °C			250 1000	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 15 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 5 V I_D = 6 A V_{GS} = 5 V I_D = 6 A T_c = 100°C			0.15 0.3	Ω Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ V_{GS} = 5 V	12			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ I_D = 6 A	4			S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			650 250 100	pF pF pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 25 V I_D = 6 A R_{GS} = 50 Ω V_{GS} = 5 V (see test circuit, figure 3)		10 50	20 80	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	V_{DD} = 40 V I_D = 12 A R_{GS} = 50 Ω V_{GS} = 5 V (see test circuit, figure 5)		150		A/µs
Q_g	Total Gate Charge	V_{DD} = 40 V I_D = 12 A V_{GS} = 5 V		9	14	nC

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING OFF

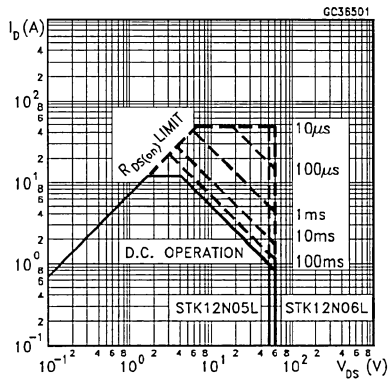
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 40 V I_D = 12 A		110	150	ns
t_f	Fall Time	R_{GS} = 50 Ω V_{GS} = 5 V		70	100	ns
t_c	Cross-over Time			180	250	ns

SOURCE DRAIN DIODE

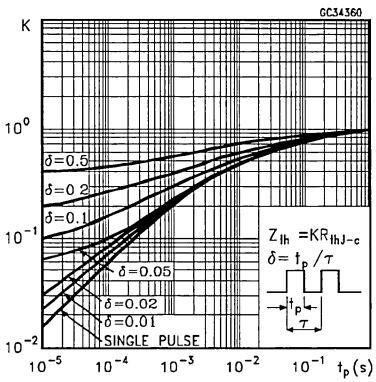
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				12	A
I_{SDM}(•)	Source-drain Current (pulsed)				48	A
V_{SD}	Forward On Voltage	I_{SD} = 12 A V_{GS} = 0			1.4	V
t_{rr}	Reverse Recovery Time	I_{SD} = 12 A di/dt = 100 A/µs V_{DD} = 15 V T_j = 150 °C		80		ns
Q_{rr}	Reverse Recovery Charge			0.15		µC
I_{RRM}	Reverse Recovery Current			3.5		A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

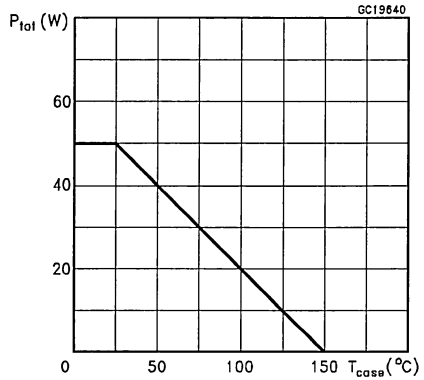
Safe Operating Areas



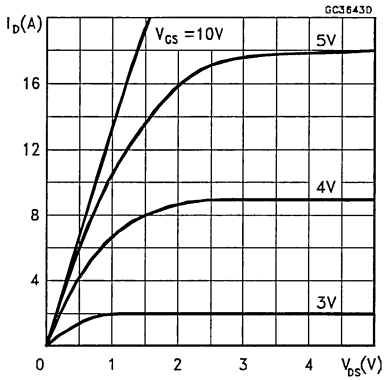
Thermal Impedance



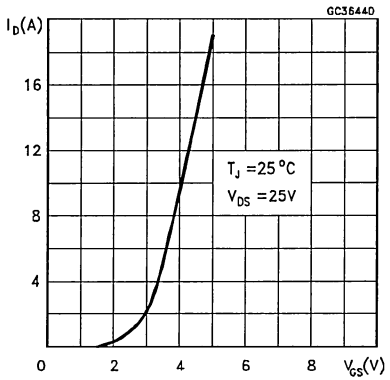
Derating Curve



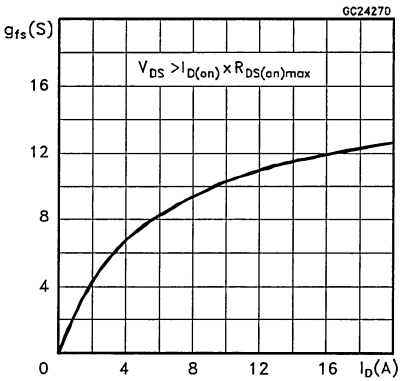
Output Characteristics



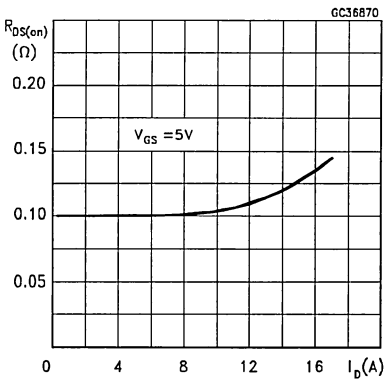
Transfer Characteristics



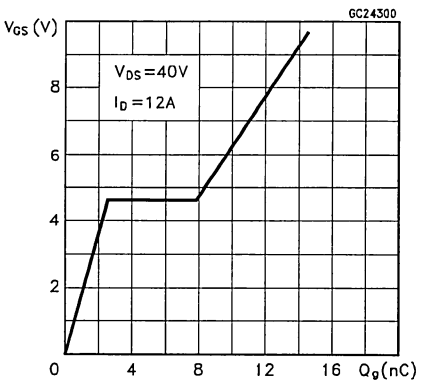
Transconductance



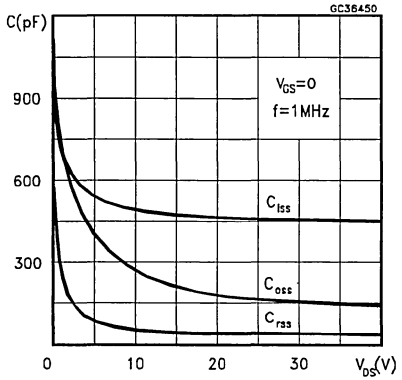
Static Drain-source On Resistance



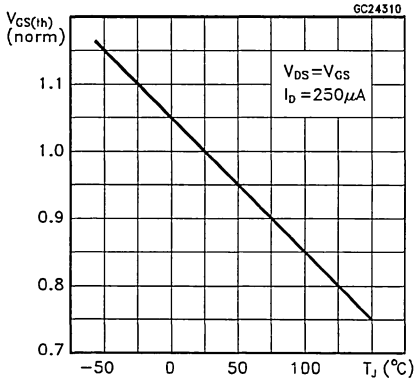
Gate Charge vs Gate-source Voltage



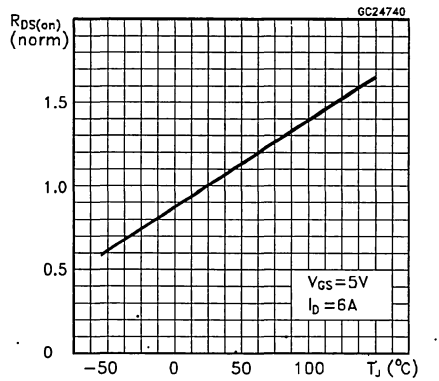
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

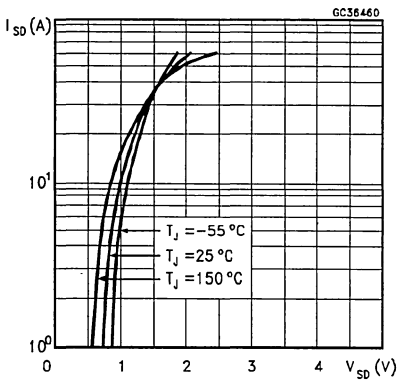


Fig. 1: Unclamped Inductive Load Test Circuits

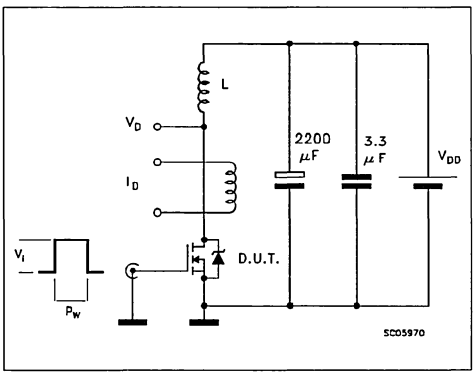


Fig. 2: Unclamped Inductive Waveforms

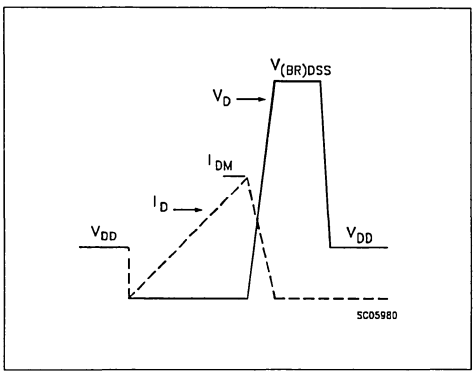


Fig. 3: Switching Times Test Circuits For Resistive Load

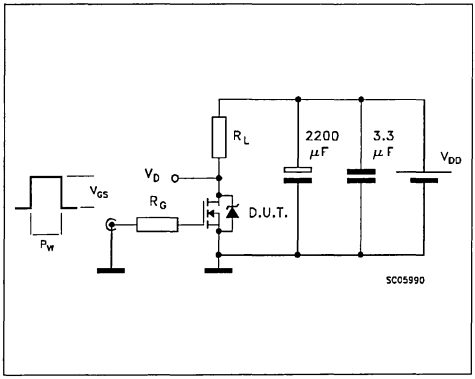


Fig. 4: Gate Charge Test Circuit

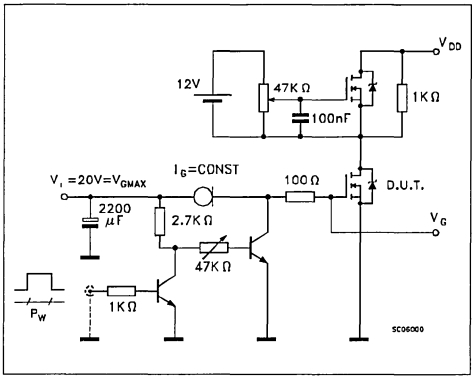
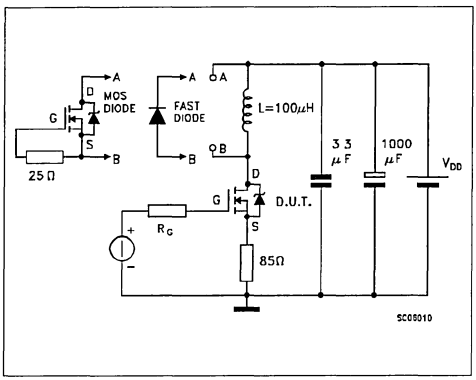


Fig. 5: Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time



SGS-THOMSON MICROELECTRONICS

STK22N05

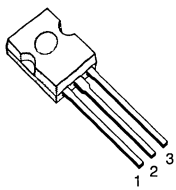
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STK22N05	50 V	0.065 Ω	22 A

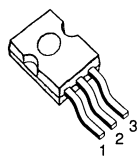
- AVALANCHE RUGGEDNESS TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- APPLICATION ORIENTED CHARACTERIZATION

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)

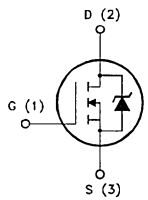


SOT-82



SOT-194 (option)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	50	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	50	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (continuous) at T_c = 25 °C	22	A
I_D	Drain Current (continuous) at T_c = 100 °C	14	A
I_{DM}(•)	Drain Current (pulsed)	88	A
P_{tot}	Total Dissipation at T_c = 25 °C	60	W
	Derating Factor	0.48	W/°C
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.08	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Case-sink	Typ	0.7	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		275	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	22	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 25$ V)	100	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	25	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive ($T_c = 100$ °C, pulse width limited by T_j max, $\delta < 1\%$)	14	A

ELECTRICAL CHARACTERISTICS ($T_{case} = 25$ °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250$ µA $V_{GS} = 0$	50			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$) Zero Gate Voltage Drain Current ($V_{GS} = 0$)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 $T_c = 125$ °C			250 1000	µA µA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20$ V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250$ µA	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance Static Drain-source On Resistance	$V_{GS} = 10$V $I_D = 11$ A $V_{GS} = 10$V $I_D = 11$ A $T_c = 100$°C			0.065 0.13	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10$ V	22			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 11$ A	6			S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25$ V f = 1 MHz $V_{GS} = 0$			1200 600 200	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 30 V I_D = 3 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 3)		30 90	45 130	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	V_{DD} = 40 V I_D = 22 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 5)		230		A/µs
Q_g	Total Gate Charge	V_{DD} = 40 V I_D = 22 A V_{GS} = 10 V		26	40	nC

SWITCHING OFF

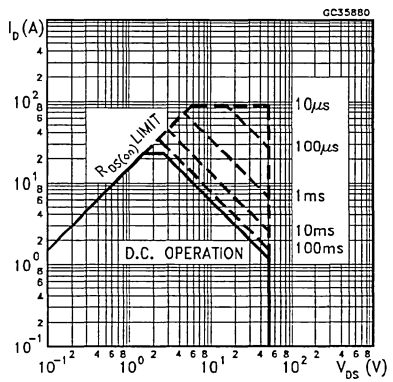
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 40 V I_D = 22 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 5)		80 80 170	120 120 250	ns ns ns

SOURCE DRAIN DIODE

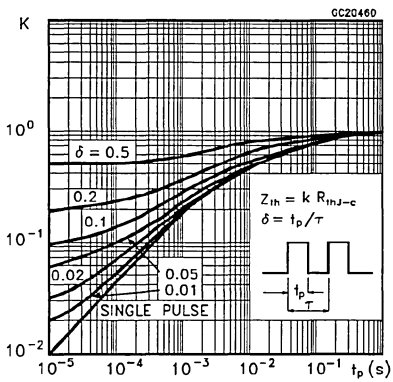
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				22 88	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 22 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 22 A di/dt = 100 A/µs V_{DD} = 30 V T_j = 150 °C (see test circuit, figure 5)		80 0.22 5.5		ns µC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

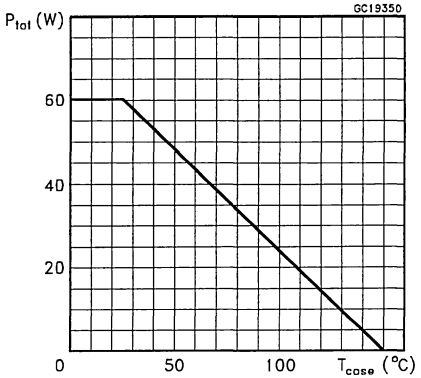
Safe Operating Area



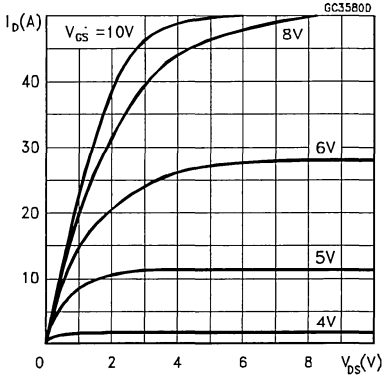
Thermal Impedance



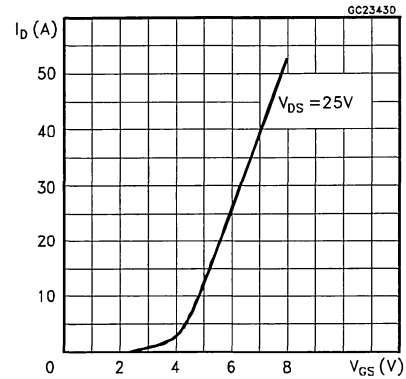
Derating Curve



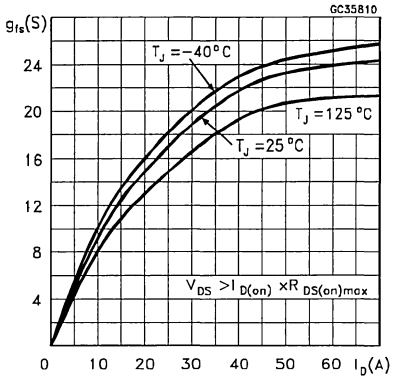
Output Characteristics



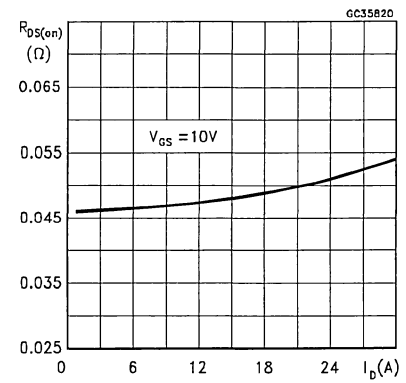
Transfer Characteristics



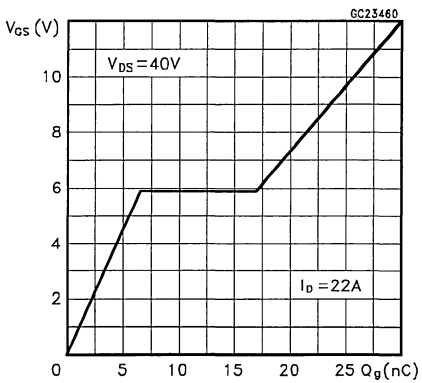
Transconductance



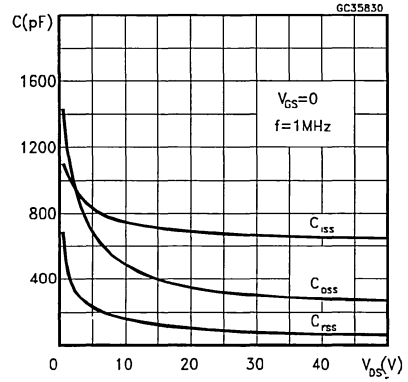
Static Drain-source On Resistance



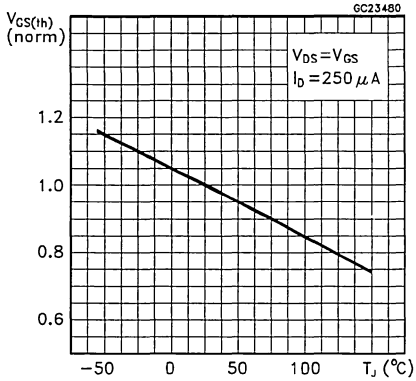
Gate Charge vs Gate-source Voltage



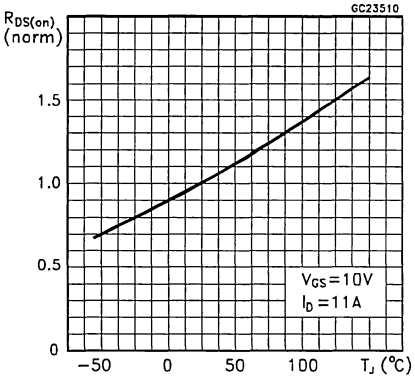
Capacitance Variations



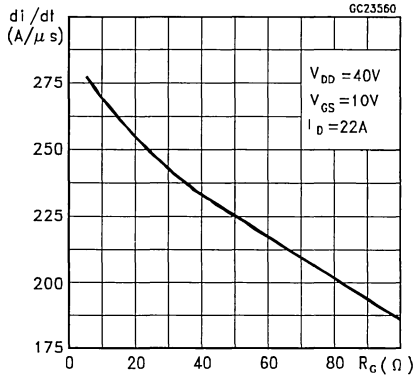
Normalized Gate Threshold Voltage vs Temperature



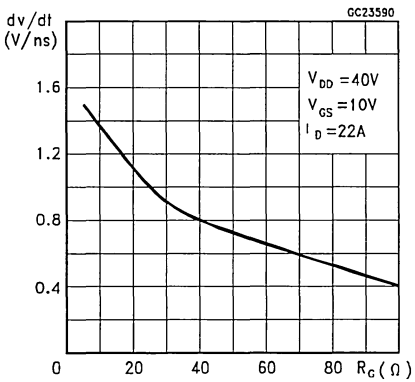
Normalized On Resistance vs Temperature



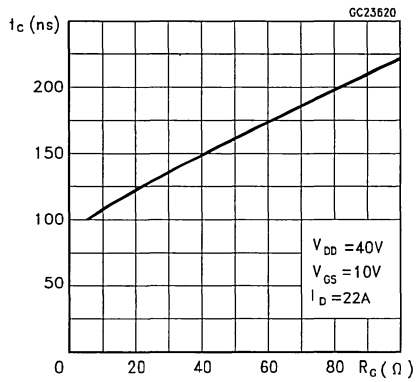
Turn-on Current Slope



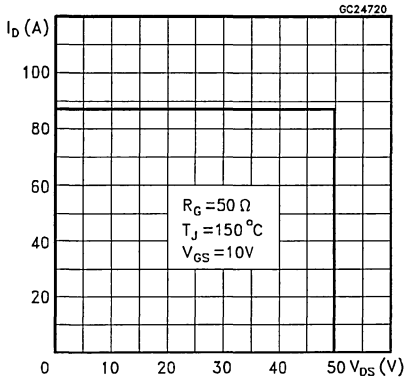
Turn-off Drain-source Voltage Slope



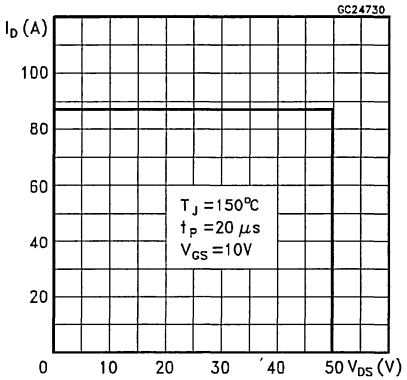
Cross-over Time



Switching Safe Operating Area



Accidental Overload Area



Source-drain Diode Forward Characteristics

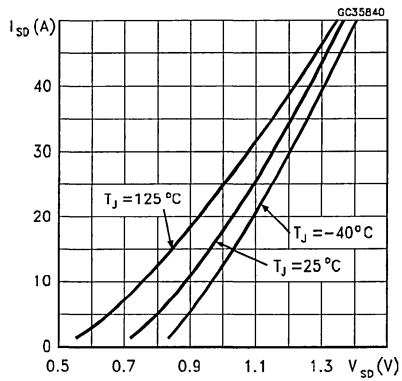


Fig. 1: Unclamped Inductive Load Test Circuits

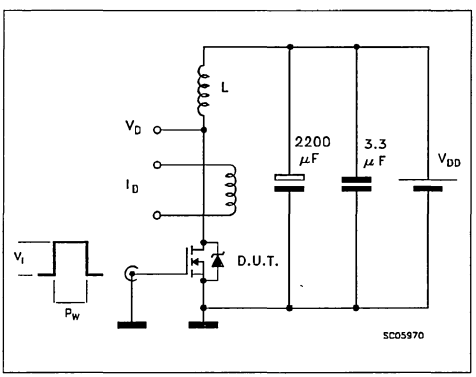


Fig. 2: Unclamped Inductive Waveforms

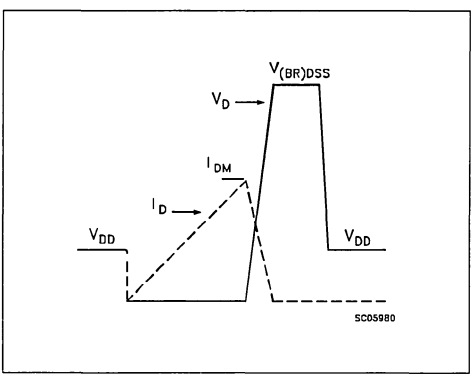


Fig. 3: Switching Times Test Circuits For Resistive Load

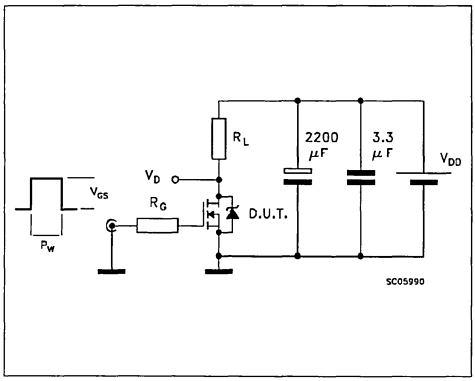


Fig. 4: Gate Charge Test Circuit

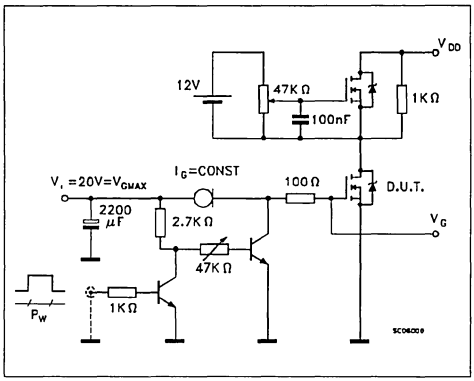
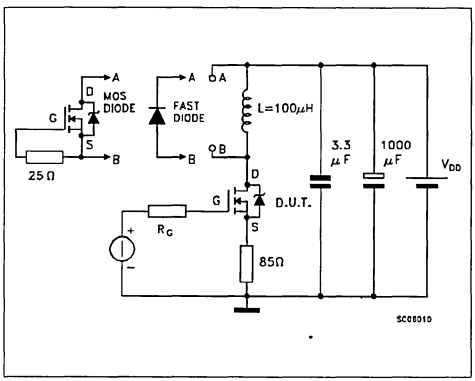


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SGS-THOMSON MICROELECTRONICS

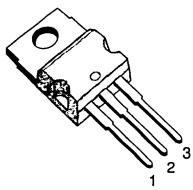
STP19N05L
STP19N06L

N - CHANNEL ENHANCEMENT MODE LOW THRESHOLD POWER MOS TRANSISTOR

TENTATIVE DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP19N05L	50 V	0.1 Ω	19 A
STP19N06L	60 V	0.1 Ω	19 A

- AVALANCHE RUGGEDNESS TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- LOGIC LEVEL COMPATIBLE INPUT
- 175°C OPERATING TEMPERATURE
- APPLICATION ORIENTED CHARACTERIZATION

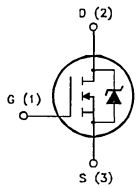


TO-220

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP19N05L	STP19N06L	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	50	60	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	50	60	V
V_{GS}	Gate-source Voltage	± 15		V
I_D	Drain Current (continuous) at T_c = 50 °C	19		A
I_D	Drain Current (continuous) at T_c = 100 °C	14		A
I_{DM}(•)	Drain Current (pulsed)	76		A
P_{tot}	Total Dissipation at T_c = 25 °C	85		W
	Derating Factor	0.57		W/°C
T_{stg}	Storage Temperature	-65 to 175		°C
T_j	Max. Operating Junction Temperature	175		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.76	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	°C/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	19	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 25$ V)	60	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	15	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive ($T_c = 100$ °C, pulse width limited by T_j max, $\delta < 1\%$)	11	A

ELECTRICAL CHARACTERISTICS ($T_{case} = 25$ °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250$ µA $V_{GS} = 0$ for **STP19N05L** for **STP19N06L**	 50 60			 V V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 $T_c = 125$ °C			250 1000	µA µA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 15$ V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250$ µA	1		2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 5$ V $I_D = 9.5$ A $V_{GS} = 5$ V $I_D = 9.5$ A $T_c = 100$°C			0.1 0.2	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 5$ V	19			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 9.5$ A		10		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25$ V $f = 1$ MHz $V_{GS} = 0$		700 200 50		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 30 V I_D = 3 A R_G = 50 Ω V_{GS} = 5 V (see test circuit, figure 3)		25 80		ns ns
$(di/dt)_{on}$	Turn-on Current Slope	V_{DD} = 40 V I_D = 19 A R_G = 50 Ω V_{GS} = 5 V (see test circuit, figure 5)		150		A/µs
Q_g	Total Gate Charge	V_{DD} = 40 V I_D = 19 A V_{GS} = 5 V		18		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 40 V I_D = 19 A R_{GS} = 50 Ω V_{GS} = 5 V (see test circuit, figure 5)		130 150 280		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				19 76	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 19 A V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 19 A di/dt = 100 A/µs V_{DD} = 25 V T_j = 150 °C (see test circuit, figure 5)		120 0.2 3.5		ns µC A

(*) Pulsed. Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

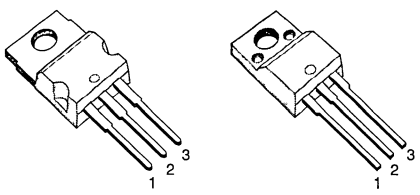
SGS-THOMSON MICROELECTRONICS

STP25N06
STP25N06FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP25N06	60 V	0.07 Ω	25 A
STP25N06FI	60 V	0.07 Ω	16 A

- AVALANCHE RUGGEDNESS TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE FOR STANDARD PACKAGE
- APPLICATION ORIENTED CHARACTERIZATION
- ISOLATED PACKAGE UL RECOGNIZED, ISOLATION TO 2000V DC

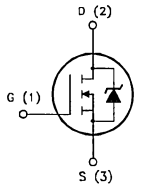


TO-220 **ISOWATT220**

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP25N06	STP25N06FI	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60		V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	60		V
V_{GS}	Gate-source Voltage	± 20		V
I_D	Drain Current (continuous) at T_c = 25 °C(#)	25	16	A
I_D	Drain Current (continuous) at T_c = 100 °C	19	10	A
I_{DM}(•)	Drain Current (pulsed)	100	100	A
P_{tot}	Total Dissipation at T_c = 25 °C	95	35	W
	Derating Factor	0.63	0.28	W/°C
T_{stg}	Storage Temperature	-65 to 175	-65 to 150	°C
T_j	Max. Operating Junction Temperature	175	150	°C

(•) Pulse width limited by safe operating area
(#) T_c = 50 °C for TO-220

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.57	3.57	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5		°C/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	25	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 25 V)	125	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	30	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (T_c = 100 °C, pulse width limited by T_j max, $\delta < 1\%$)	15	A

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	60			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125 °C			250 1000	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 12.5 A V_{GS} = 10V I_D = 12.5 A T_c = 100°C			0.07 0.14	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ V_{GS} = 10 V	25			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ I_D = 12.5 A	7			S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			1200 600 200	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 30 V I_D = 3 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 3)		30 90	45 130	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	V_{DD} = 40 V I_D = 25 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 5)		230		A/µs
Q_g	Total Gate Charge	V_{DD} = 40 V I_D = 25 A V_{GS} = 10 V		26	40	nC

SWITCHING OFF

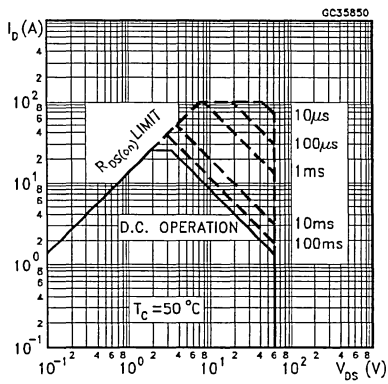
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 40 V I_D = 25 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 5)		80 80 170	120 120 250	ns ns ns

SOURCE DRAIN DIODE

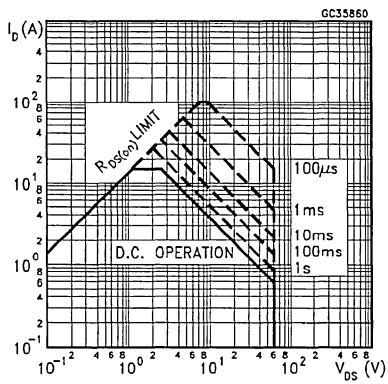
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				25 100	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 25 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 25 A di/dt = 100 A/µs V_{DD} = 30 V T_j = 150 °C (see test circuit, figure 5)		80 0.22 5.5		ns µC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

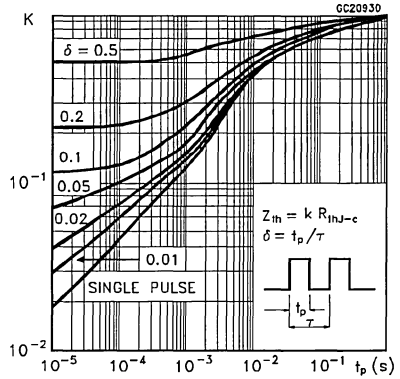
Safe Operating Areas For TO-220



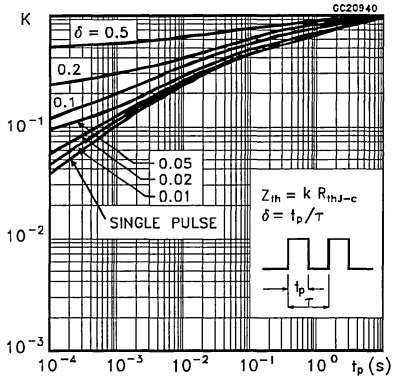
Safe Operating Areas For ISOWATT220



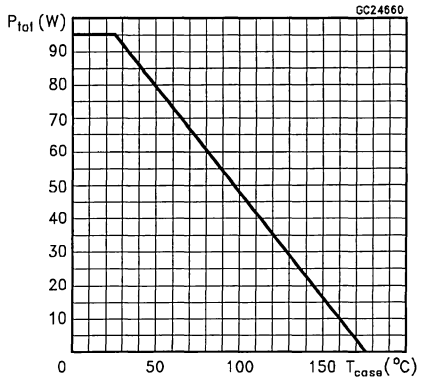
Thermal Impedeance For TO-220



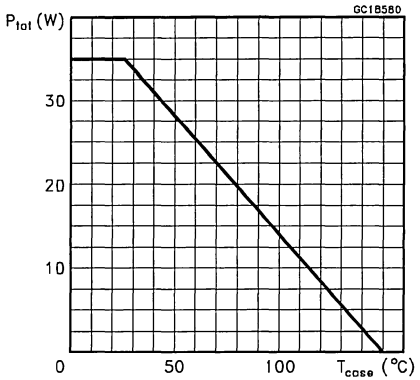
Thermal Impedance For ISOWATT220



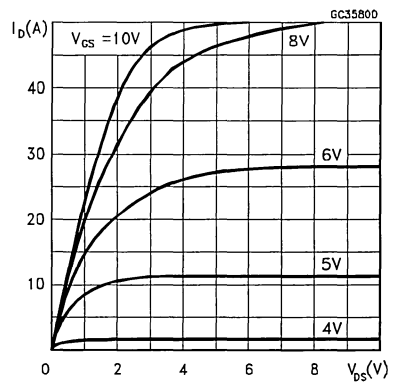
Derating Curve For TO-220



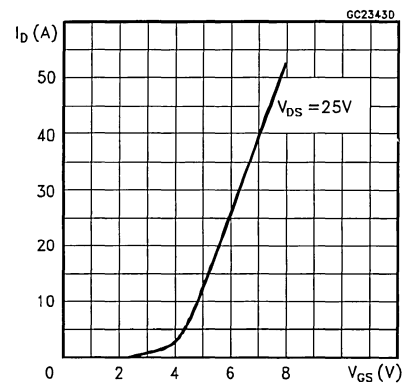
Derating Curve For ISOWATT220



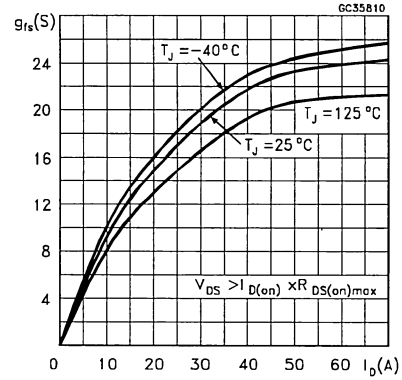
Output Characteristics



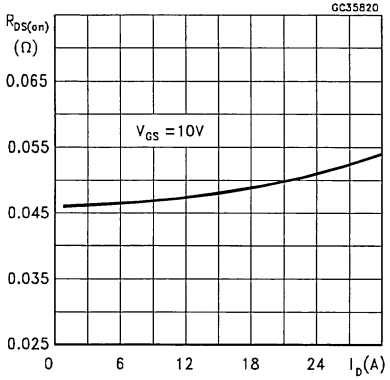
Transfer Characteristics



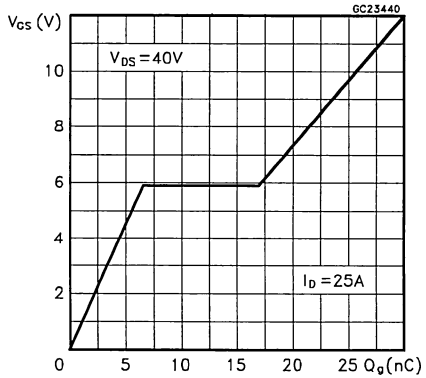
Transconductance



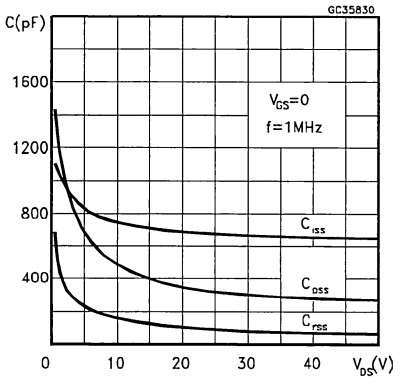
Static Drain-source On Resistance



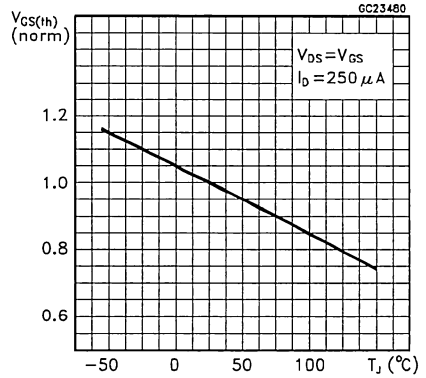
Gate Charge vs Gate-source Voltage



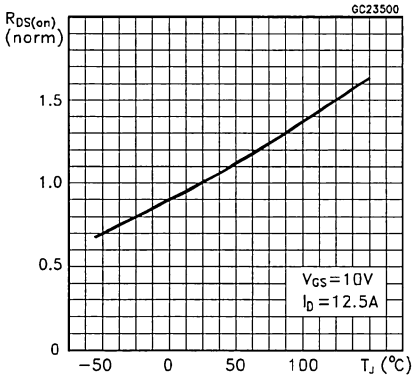
Capacitance Variations



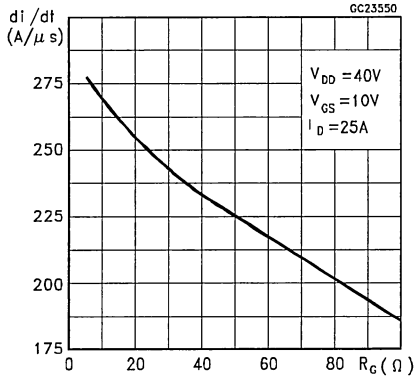
Normalized Gate Threshold Voltage vs Temperature



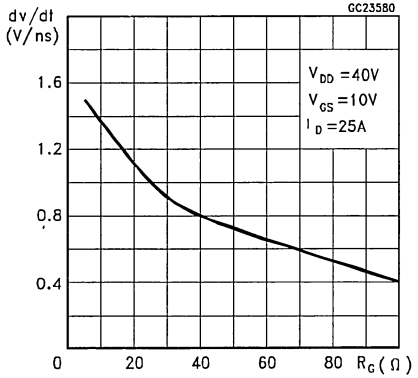
Normalized On Resistance vs Temperature



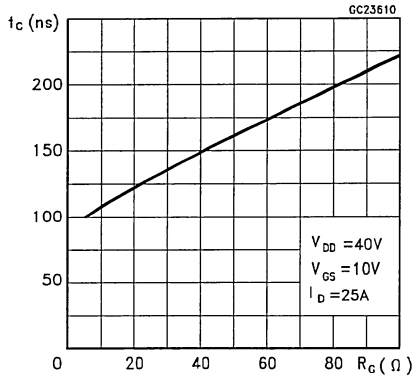
Turn-on Current Slope



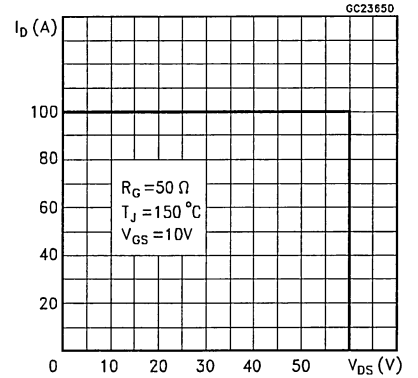
Turn-off Drain-source Voltage Slope



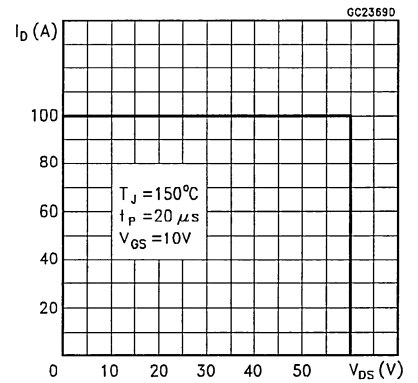
Cross-over Time



Switching Safe Operating Area



Accidental Overload Area



Source-drain Diode Forward Characteristics

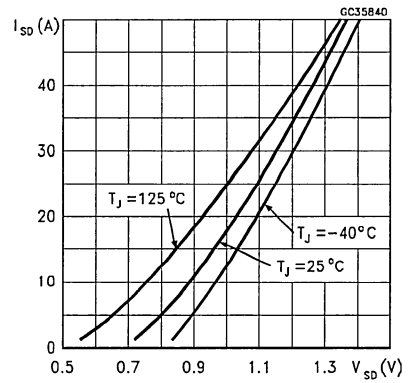


Fig. 1: Unclamped Inductive Load Test Circuits

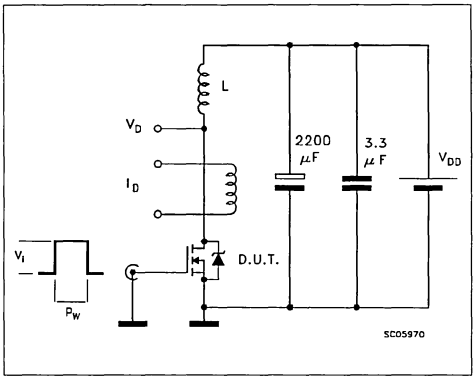


Fig. 2: Unclamped Inductive Waveforms

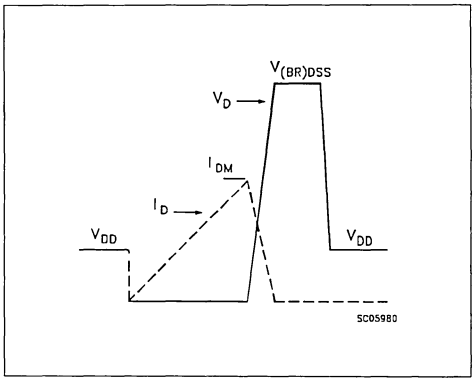


Fig. 3: Switching Times Test Circuits For Resistive Load

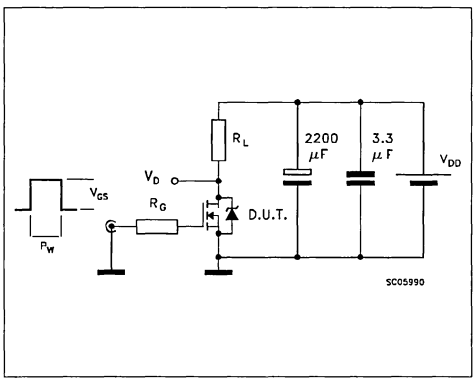


Fig. 4: Gate Charge Test Circuit

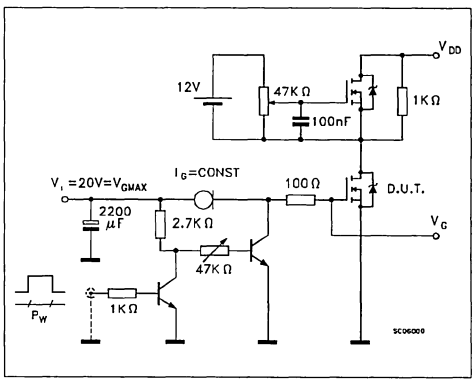
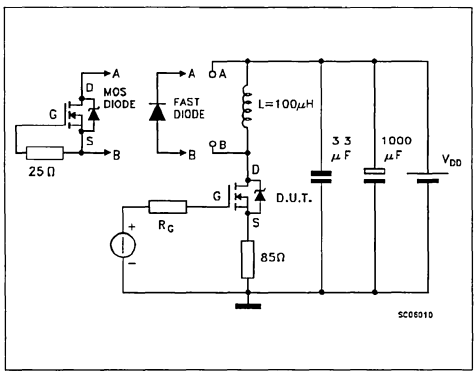


Fig. 5: Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time



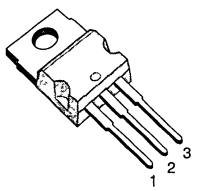
SGS-THOMSON MICROELECTRONICS

STP36N06
STP36N06FI

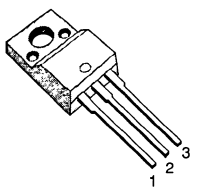
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP36N06	60 V	0.04 Ω	36 A
STP36N06FI	60 V	0.04 Ω	20 A

- AVALANCHE RUGGEDNESS TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE FOR STANDARD PACKAGE
- APPLICATION ORIENTED CHARACTERIZATION
- ISOLATED PACKAGE UL RECOGNIZED, ISOLATION TO 2000V DC



TO-220

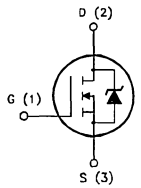


ISOWATT220

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP36N06	STP36N06FI	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60		V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	60		V
V_{GS}	Gate-source Voltage	± 20		V
I_D	Drain Current (continuous) at T_c = 25 °C(#)	36	20	A
I_D	Drain Current (continuous) at T_c = 100 °C	27	12	A
I_{DM}(•)	Drain Current (pulsed)	144	144	A
P_{tot}	Total Dissipation at T_c = 25 °C	120	35	W
	Derating Factor	0.8	0.28	W/°C
T_{stg}	Storage Temperature	-65 to 175	-65 to 150	°C
T_j	Max. Operating Junction Temperature	175	150	°C

(•) Pulse width limited by safe operating area
(#) T_c = 50 °C for TO-220

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.25	3.57	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5		°C/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	36	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25\ °C$, $I_D = I_{AR}$, $V_{DD} = 25$ V)	220	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	50	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive ($T_c = 100\ °C$, pulse width limited by T_j max, $\delta < 1\%$)	22	A

ELECTRICAL CHARACTERISTICS ($T_{case} = 25\ °C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu A$ $V_{GS} = 0$	60			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 $T_c = 125\ °C$			250 1000	µA µA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20$ V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu A$	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10$V $I_D = 18$ A $V_{GS} = 10$V $I_D = 18$ A $T_c = 100°C$			0.04 0.08	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10$ V	36			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 18$ A	12			S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25$ V f = 1 MHz $V_{GS} = 0$			2000 800 250	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 30 V I_D = 3 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 3)		45 75	65 100	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	V_{DD} = 40 V I_D = 30 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 5)		180		A/µs
Q_g	Total Gate Charge	V_{DD} = 40 V I_D = 30 A V_{GS} = 10 V		40	60	nC

SWITCHING OFF

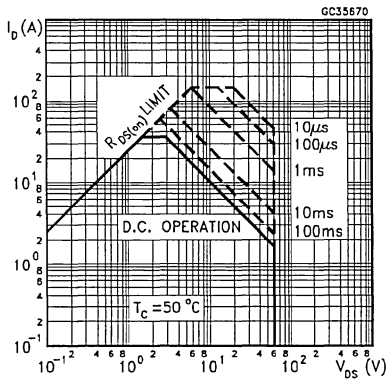
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 40 V I_D = 30 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 5)		90 65 160	130 90 220	ns ns ns

SOURCE DRAIN DIODE

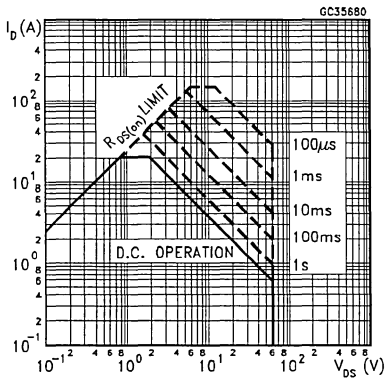
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				36 144	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 36 A V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 30 A di/dt = 100 A/µs V_{DD} = 20 V T_j = 150 °C (see test circuit, figure 5)		90 0.23 5		ns µC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

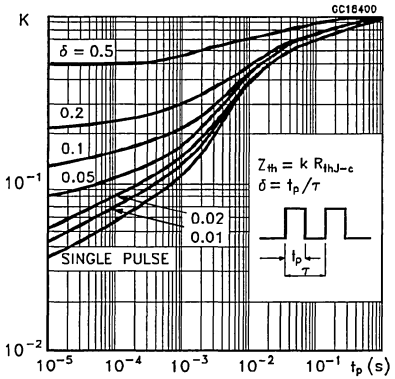
Safe Operating Areas For TO-220



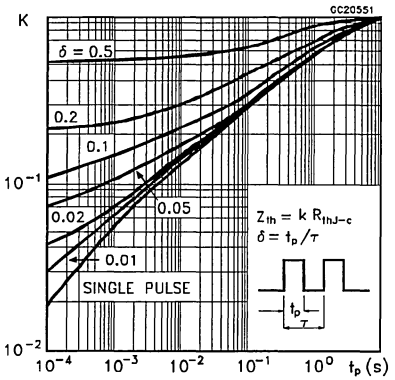
Safe Operating Areas For ISOWATT220



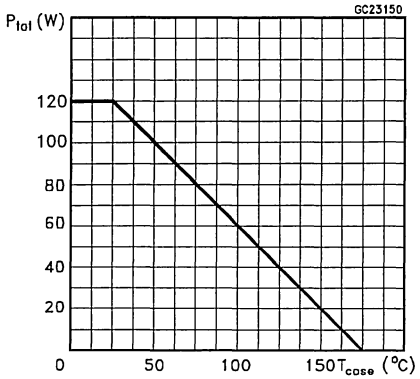
Thermal Impedance For TO-220



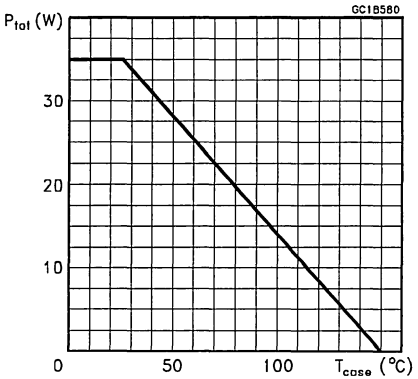
Thermal Impedance For ISOWATT220



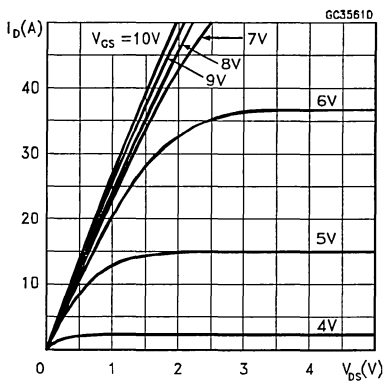
Derating Curve For TO-220



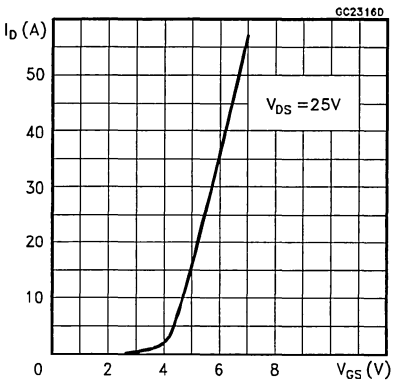
Derating Curve For ISOWATT220



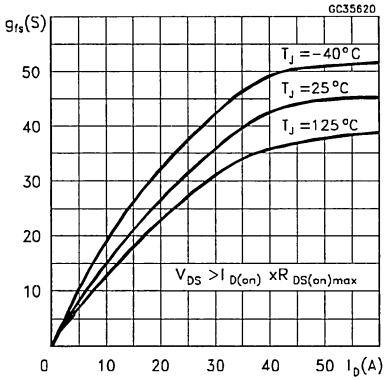
Output Characteristics



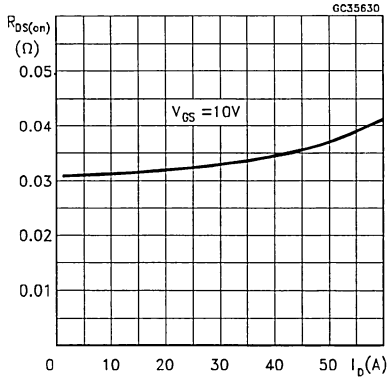
Transfer Characteristics



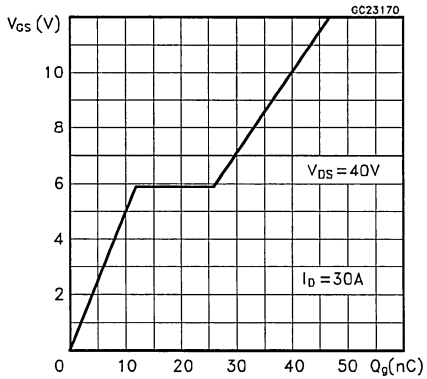
Transconductance



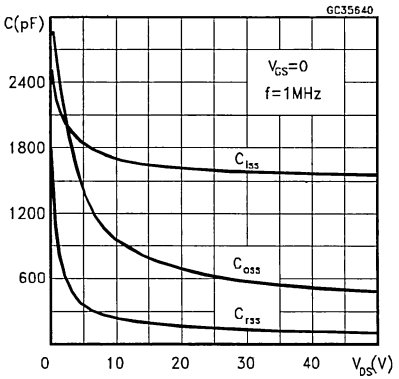
Static Drain-source On Resistance



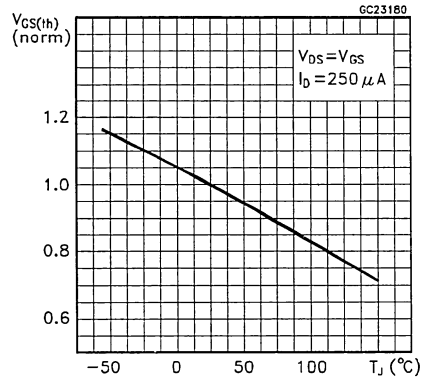
Gate Charge vs Gate-source Voltage



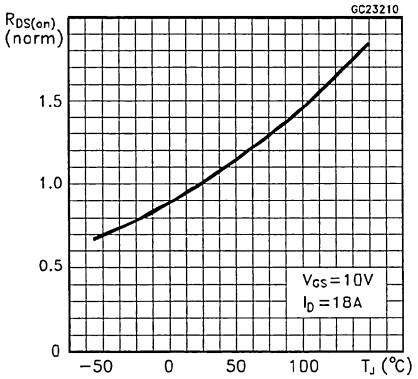
Capacitance Variations



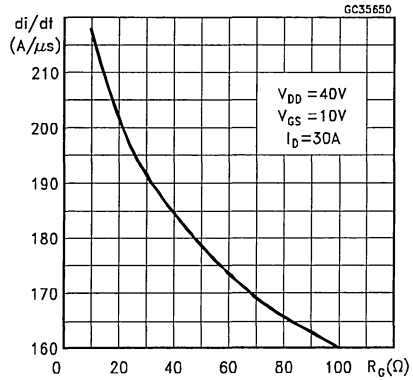
Normalized Gate Threshold Voltage vs Temperature



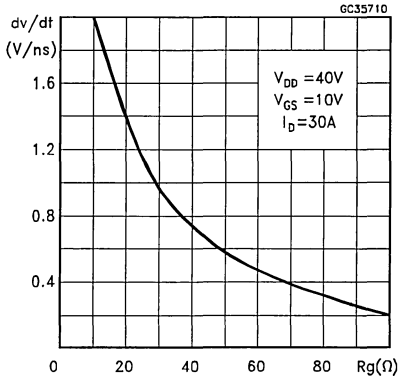
Normalized On Resistance vs Temperature



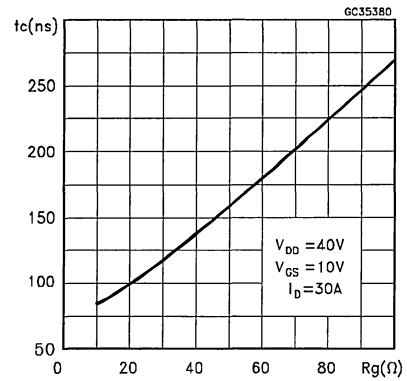
Turn-on Current Slope



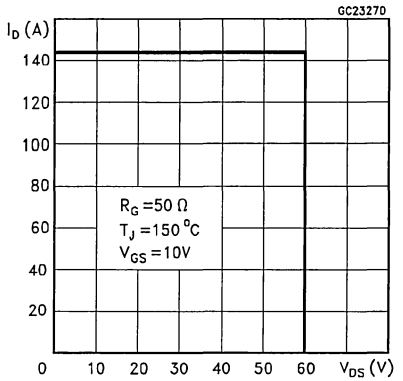
Turn-off Drain-source Voltage Slope



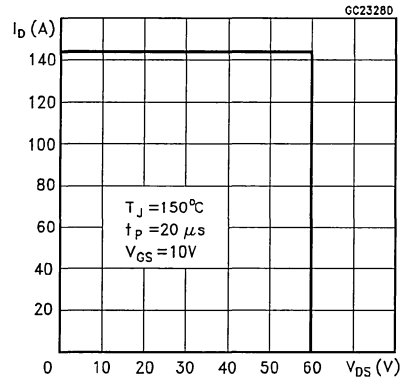
Cross-over Time



Switching Safe Operating Area



Accidental Overload Area



Source-drain Diode Forward Characteristics

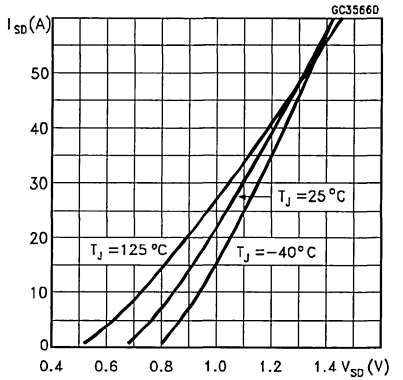


Fig. 1: Unclamped Inductive Load Test Circuits

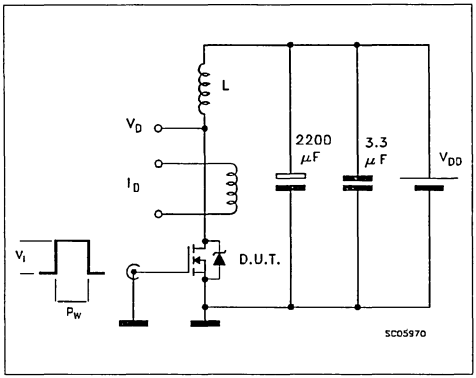


Fig. 2: Unclamped Inductive Waveforms

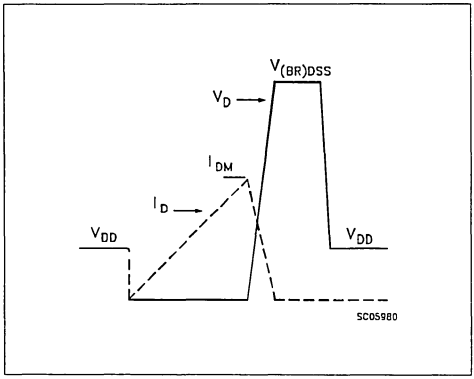


Fig. 3: Switching Times Test Circuits For Resistive Load

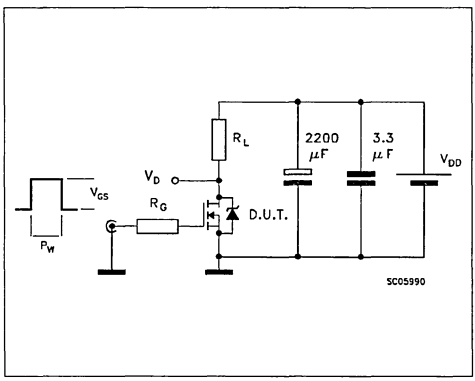


Fig. 4: Gate Charge Test Circuit

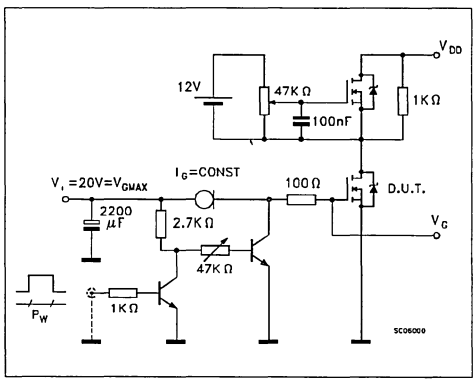
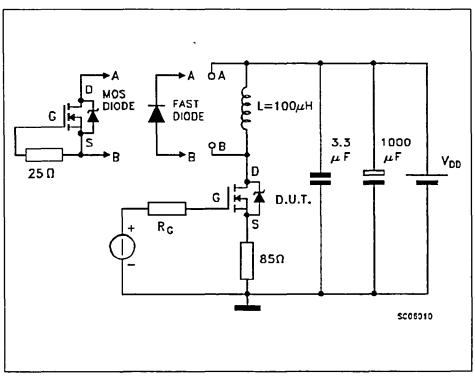


Fig. 5: Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time



SGS-THOMSON MICROELECTRONICS

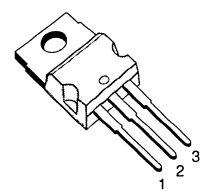
STP40N06L
STP40N06LFI

N - CHANNEL ENHANCEMENT MODE LOW THRESHOLD POWER MOS TRANSISTOR

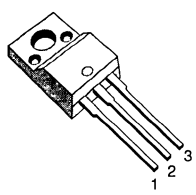
ADVANCE DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP40N06L	60 V	0.04 Ω	40 A
STP40N06LFI	60 V	0.04 Ω	22 A

- AVALANCHE RUGGEDNESS TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- LOGIC LEVEL COMPATIBLE INPUT
- 175°C OPERATING TEMPERATURE FOR STANDARD PACKAGE
- APPLICATION ORIENTED CHARACTERIZATION
- ISOLATED PACKAGE UL RECOGNIZED, ISOLATION TO 2000V DC



TO-220

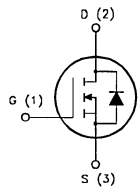


ISOWATT220

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP40N06L	STP40N06LFI	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60		V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	60		V
V_{GS}	Gate-source Voltage	± 15		V
I_D	Drain Current (continuous) at T_c = 25 °C(#)	40	22	A
I_D	Drain Current (continuous) at T_c = 100 °C	30	13	A
I_{DM}(•)	Drain Current (pulsed)	160	160	A
P_{tot}	Total Dissipation at T_c = 25 °C	150	40	W
	Derating Factor	1	0.32	W/°C
T_{stg}	Storage Temperature	-65 to 175	-65 to 150	°C
T_j	Max. Operating Junction Temperature	175	150	°C

(•) Pulse width limited by safe operating area
(#) T_c = 50 °C for TO-220

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1	3.12	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5		°C/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	60			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125 °C			250 1000	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 15 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 5 V I_D = 20 A V_{GS} = 5 V I_D = 20 A T_c = 100°C			0.04 0.08	Ω Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ V_{GS} = 5 V	40			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ I_D = 20 A	15			mho
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			2200 800 250	pF pF pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 25 V I_D = 20 A R_G = 50 Ω V_{GS} = 5 V (see test circuit, figure 3)		30 300		ns ns
$(di/dt)_{on}$	Turn-on Current Slope	V_{DD} = 40 V I_D = 40 A R_G = 50 Ω V_{GS} = 5 V (see test circuit, figure 5)		100		A/µs
Q_g	Total Gate Charge	V_{DD} = 40 V I_D = 40 A V_{GS} = 5 V		30		nC

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 40 V I_D = 40 A		180		ns
t_f	Fall Time	R_G = 50 Ω V_{GS} = 5 V		200		ns
t_c	Cross-over Time	(see test circuit, figure 5)		380		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				40	A
I_{SDM}(•)	Source-drain Current (pulsed)				160	A
V_{SD} (*)	Forward On Voltage	I_{SD} = 40 A V_{GS} = 0			2	V
t_{rr}	Reverse Recovery Time	I_{SD} = 40 A di/dt = 100 A/µs V_{DD} = 25 V T_j = 150 °C		100		ns
Q_{rr}	Reverse Recovery Charge	(see test circuit, figure 5)		0.3		µC
I_{RRM}	Reverse Recovery Current			6		A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

(•) Pulse width limited by safe operating area

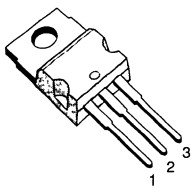
SGS-THOMSON MICROELECTRONICS

STP50N06
STP50N06FI

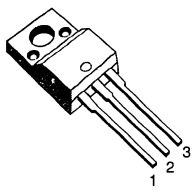
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP50N06	60 V	0.028 Ω	50 A
STP50N06FI	60 V	0.028 Ω	27 A

- AVALANCHE RUGGEDNESS TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE FOR STANDARD PACKAGE
- APPLICATION ORIENTED CHARACTERIZATION
- ISOLATED PACKAGE UL RECOGNIZED, ISOLATION TO 2000V DC



TO-220

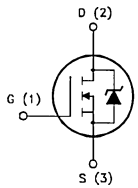


ISOWATT220

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP50N06	STP50N06FI	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60		V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	60		V
V_{GS}	Gate-source Voltage	± 20		V
I_D	Drain Current (continuous) at T_c = 25 °C(#)	50	27	A
I_D	Drain Current (continuous) at T_c = 100 °C	37	17	A
I_{DM}(•)	Drain Current (pulsed)	200	200	A
P_{tot}	Total Dissipation at T_c = 25 °C	150	40	W
	Derating Factor	1	0.32	W/°C
T_{stg}	Storage Temperature	-65 to 175	-65 to 150	°C
T_j	Max. Operating Junction Temperature	175	150	°C

(•) Pulse width limited by safe operating area
(#) T_c = 50 °C for TO-220

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1	3.12	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5		°C/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	50	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 25 V)	400	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	100	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (T_c = 100 °C, pulse width limited by T_j max, $\delta < 1\%$)	30	A

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	60			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125 °C			250 1000	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 25 A V_{GS} = 10 V I_D = 25 A T_c = 100°C			0.028 0.056	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ V_{GS} = 10 V	50			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ I_D = 25 A	17			S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			2000 1000 300	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 25 V I_D = 29 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 3)		45 90	65 130	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	V_{DD} = 40 V I_D = 50 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 5)		200		A/µs
Q_g	Total Gate Charge	V_{DD} = 40 V I_D = 50 A V_{GS} = 10 V		45	65	nC

SWITCHING OFF

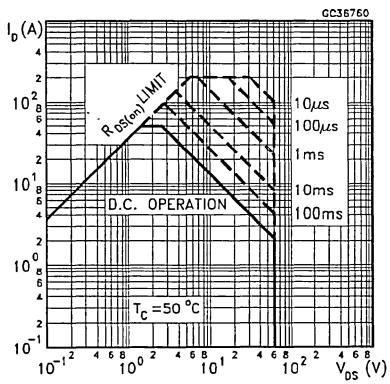
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 40 V I_D = 50 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 5)		160 90 250	220 130 350	ns ns ns

SOURCE DRAIN DIODE

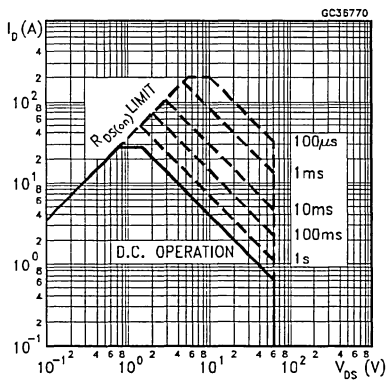
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				50 200	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 50 A V_{GS} = 0			2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 50 A di/dt = 100 A/µs V_{DD} = 30 V T_j = 150 °C (see test circuit, figure 5)		150 0.2 4		ns µC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

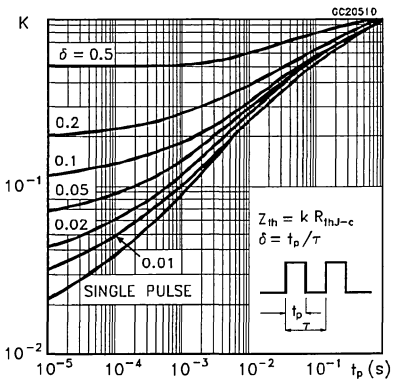
Safe Operating Areas For TO-220



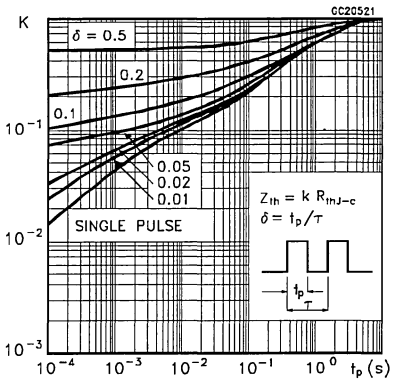
Safe Operating Areas For ISOWATT220



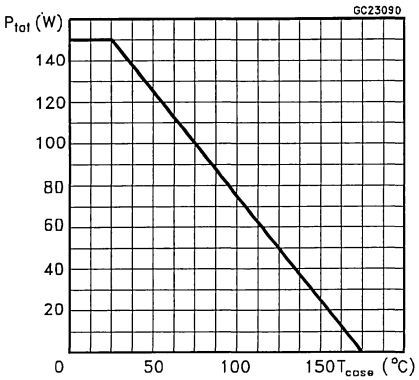
Thermal Impedeance For TO-220



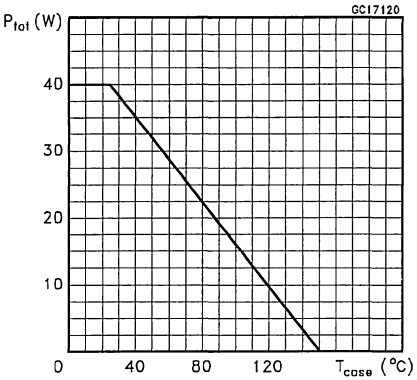
Thermal Impedance For ISOWATT220



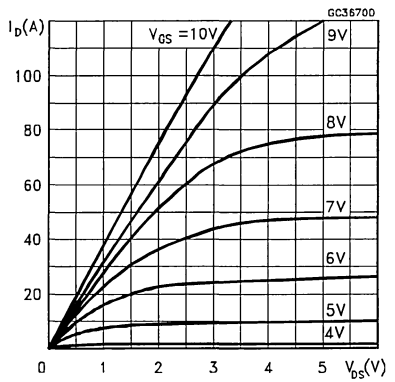
Derating Curve For TO-220



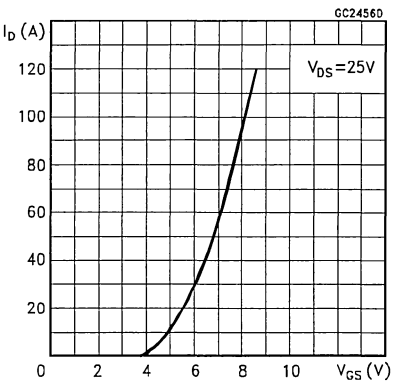
Derating Curve For ISOWATT220



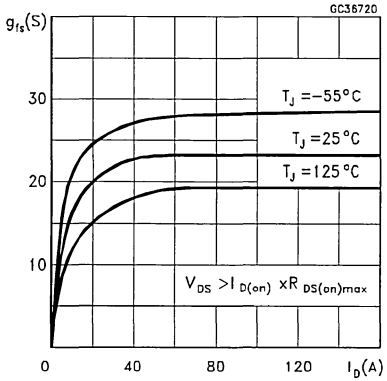
Output Characteristics



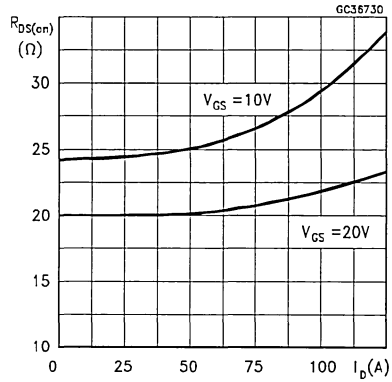
Transfer Characteristics



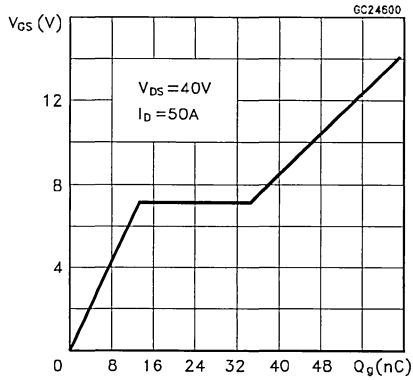
Transconductance



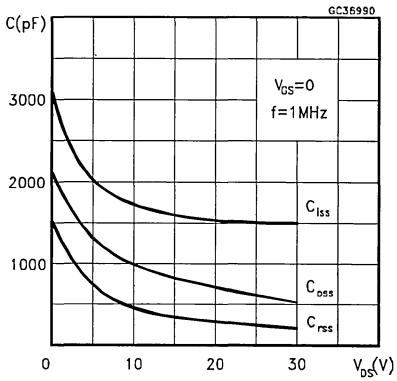
Static Drain-source On Resistance



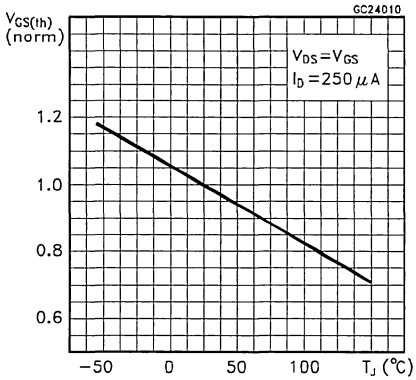
Gate Charge vs Gate-source Voltage



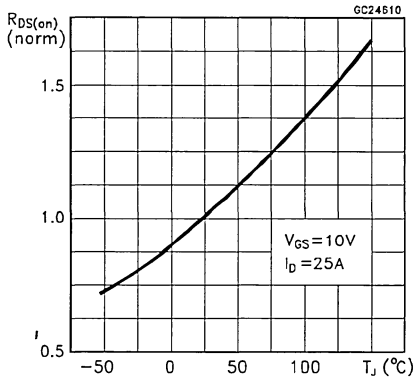
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

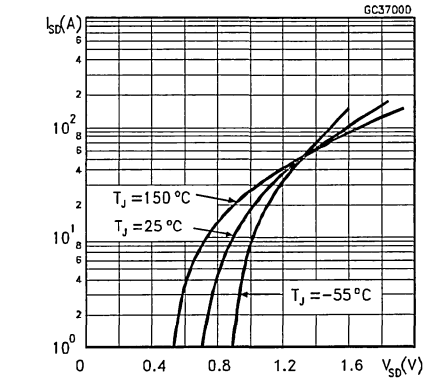


Fig. 1: Unclamped Inductive Load Test Circuits

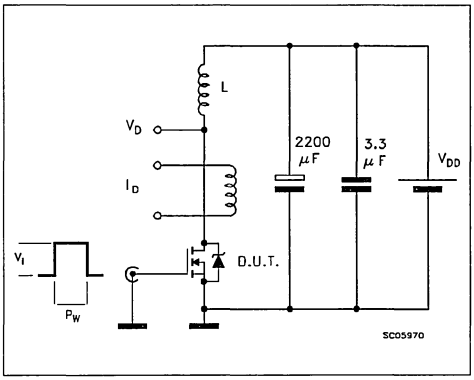


Fig. 2: Unclamped Inductive Waveforms

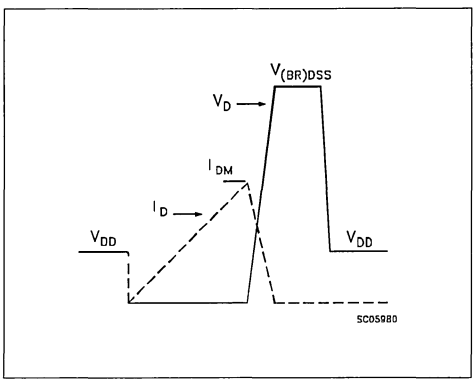


Fig. 3: Switching Times Test Circuits For Resistive Load

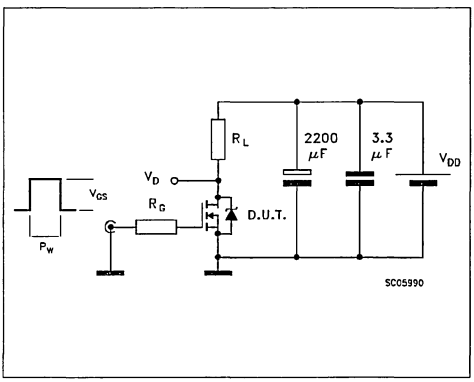


Fig. 4: Gate Charge Test Circuit

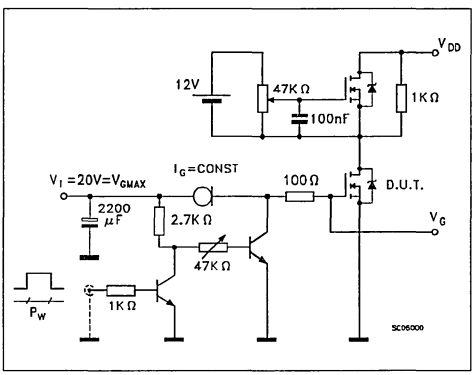
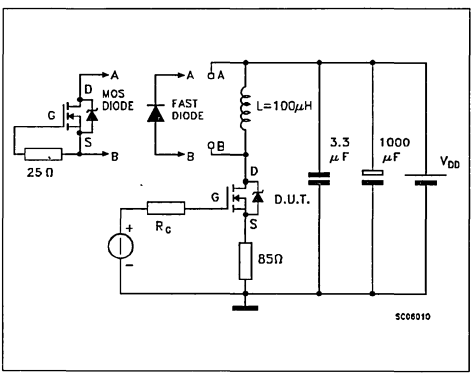


Fig. 5: Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time



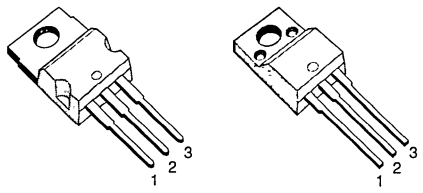
SGS-THOMSON MICROELECTRONICS

STP55N06
STP55N06FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP55N06	60 V	0.023 Ω	55 A
STP55N06FI	60 V	0.023 Ω	30 A

- AVALANCHE RUGGEDNESS TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE FOR STANDARD PACKAGE
- VERY LOW $R_{DS(on)}$
- APPLICATION ORIENTED CHARACTERIZATION
- ISOLATED PACKAGE UL RECOGNIZED, ISOLATION TO 2000V DC

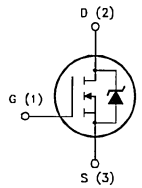


TO-220 ISOWATT220

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP55N06	STP55N06FI	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60		V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	60		V
V_{GS}	Gate-source Voltage	± 20		V
I_D	Drain Current (continuous) at T_c = 25 °C(#)	55	30	A
I_D	Drain Current (continuous) at T_c = 100 °C	41	19	A
I_{DM}(•)	Drain Current (pulsed)	220	220	A
P_{tot}	Total Dissipation at T_c = 25 °C	150	40	W
	Derating Factor	1	0.32	W/°C
T_{stg}	Storage Temperature	-65 to 175	-65 to 150	°C
T_j	Max. Operating Junction Temperature	175	150	°C

(•) Pulse width limited by safe operating area
(#) T_c = 50 °C for TO-220

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1	3.12	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5		°C/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	55	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 25$ V)	520	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	130	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive ($T_c = 100$ °C, pulse width limited by T_j max, $\delta < 1\%$)	34	A

ELECTRICAL CHARACTERISTICS ($T_{case} = 25$ °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250$ µA $V_{GS} = 0$	60			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 $T_c = 125$ °C			250 1000	µA µA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20$ V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250$ µA	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10$ V $I_D = 30$ A $V_{GS} = 10$ V $I_D = 30$ A $T_c = 100$°C			0.023 0.046	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10$ V	55			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 30$ A	16			S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25$ V f = 1 MHz $V_{GS} = 0$		2500 950 250	3000 1200 350	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 40 V I_D = 55 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 3)		110 300	150 400	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	V_{DD} = 40 V I_D = 55 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 5)		160		A/µs
Q_g	Total Gate Charge	V_{DD} = 25 V I_D = 30 A V_{GS} = 10 V		65	90	nC

SWITCHING OFF

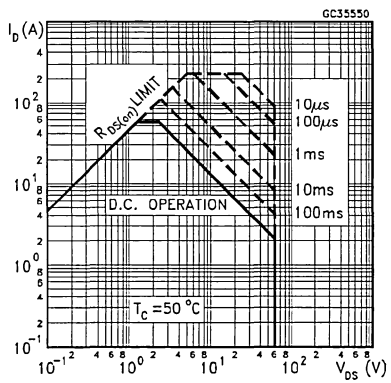
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 40 V I_D = 55 A R_G = 50 Ω V_{GS} = 10 V (see test circuit, figure 5)		160 160 320	220 220 440	ns ns ns

SOURCE DRAIN DIODE

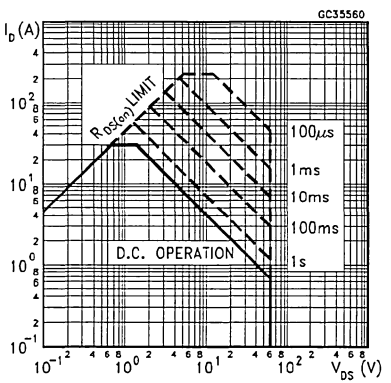
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				55 220	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 55 A V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 55 A di/dt = 100 A/µs V_{DD} = 25 V T_j = 150 °C (see test circuit, figure 5)		100 0.25 5		ns µC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

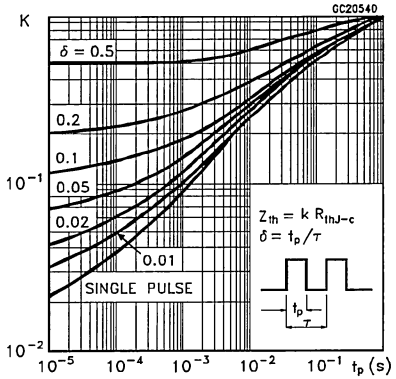
Safe Operating Areas For TO-220



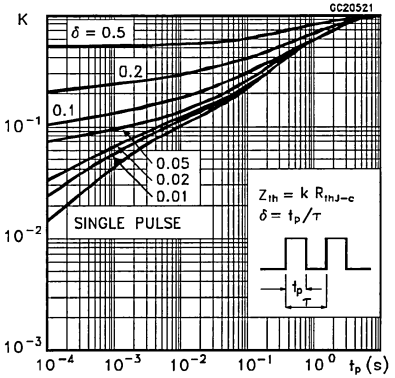
Safe Operating Areas For ISOWATT220



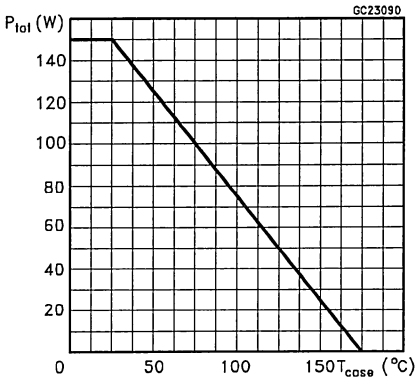
Thermal Impedance For TO-220



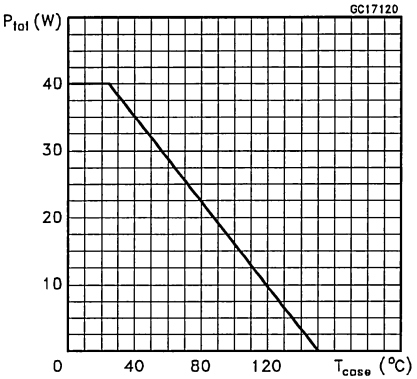
Thermal Impedance For ISOWATT220



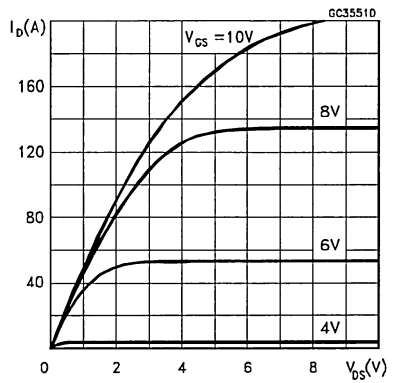
Derating Curve For TO-220



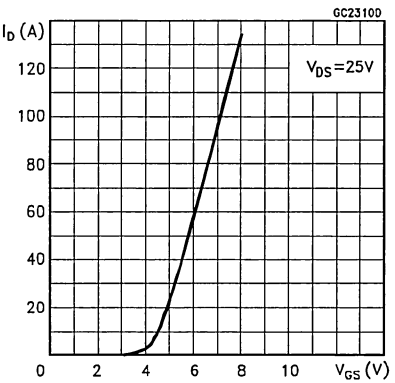
Derating Curve For ISOWATT220



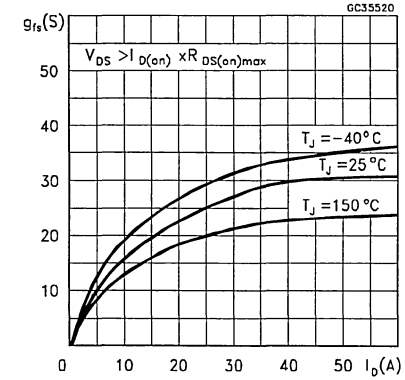
Output Characteristics



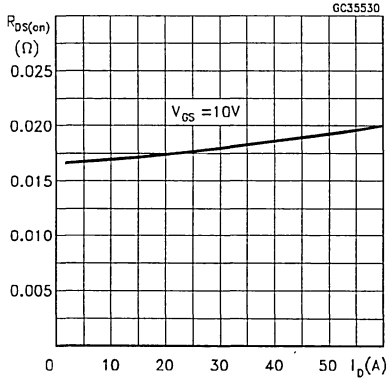
Transfer Characteristics



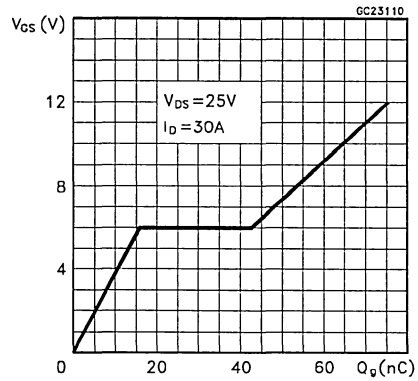
Transconductance



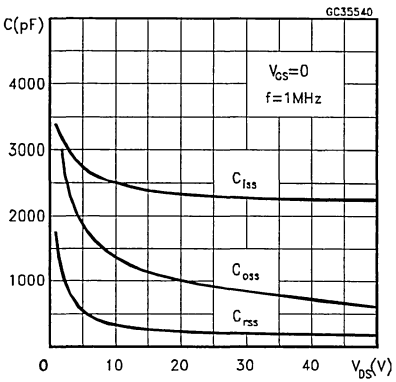
Static Drain-source On Resistance



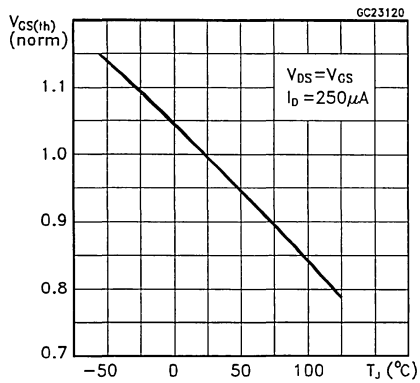
Gate Charge vs Gate-source Voltage



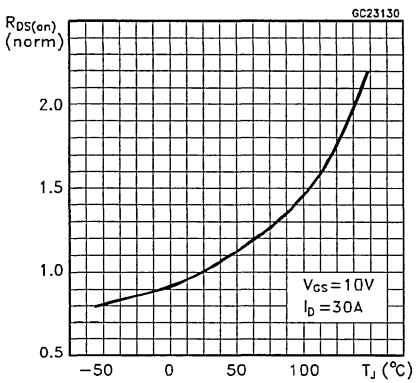
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

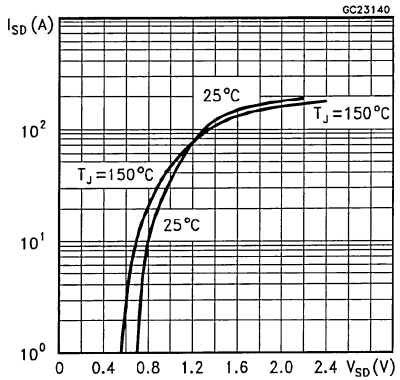


Fig. 2: Unclamped Inductive Waveforms

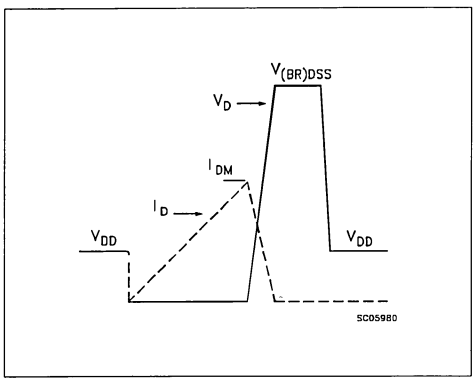


Fig. 1: Unclamped Inductive Load Test Circuits

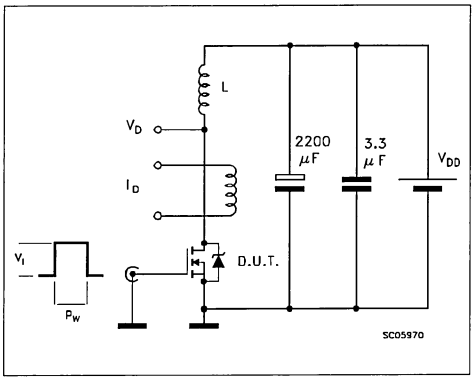


Fig. 3: Switching Times Test Circuits For Resistive Load

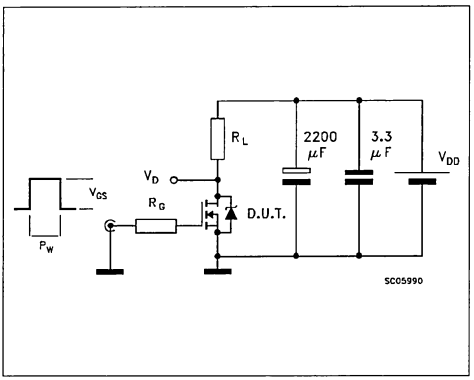


Fig. 4: Gate Charge Test Circuit

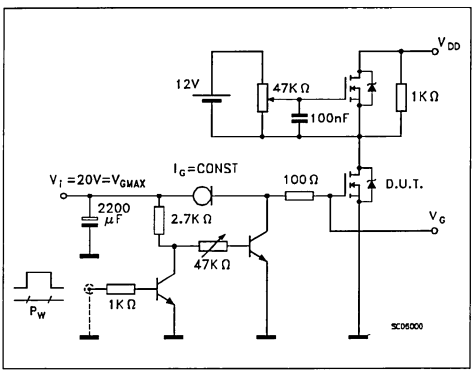
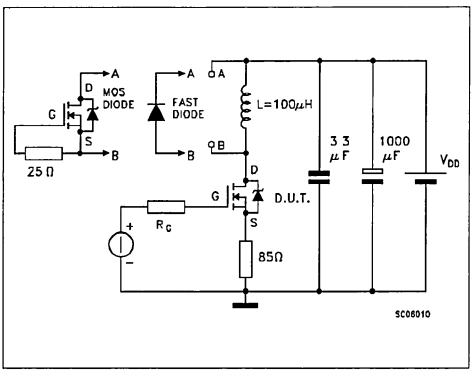


Fig. 5: Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time



APPLICATION NOTES

LOW DROP VOLTAGE REGULATORS FOR AUTOMOTIVE ELECTRONICS

By S. CISCATO

Linear voltage regulators with an input-output voltage drop of less than 2V are used to ensure continuity of the stabilized output in applications where a battery supply is used. This note describes the characteristics and operation of these devices.

Low drop linear voltage regulators are low voltage (5 to 12V) regulators which are able to provide effective stabilization of the output voltage even when the difference between input voltage and output voltage is less than 2V.

This situation can arise accidentally for a brief period when the main supply source is overloaded. It may also result from a deliberate design decision aimed at reducing the power dissipated in the supply - for example, when the device is used as a post regulator in portable instruments.

Low drop regulators are used widely in automotive applications, a field where integrated circuits have to be particularly rugged. For this reason most low drop devices include protection functions not found in standard regulators. Before describing the SGS THOMSON family of low drop regulators we will therefore begin with a brief description of the automotive electrical environment.

AUTOMOTIVE ENVIRONMENT

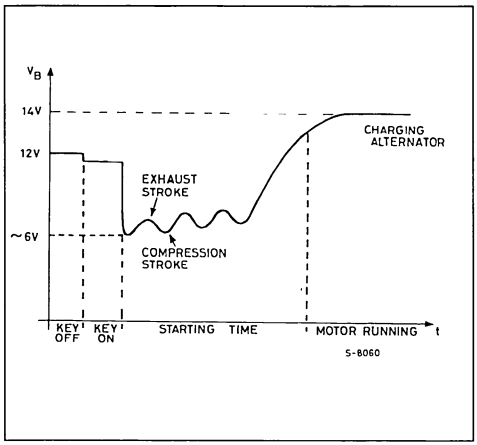
In addition to the battery voltage drop during starting, the automotive field presents a number of other serious problems concerning the regulator input voltage : positive and negative high energy / high voltage transients (load dump and field decay), positive and negative low energy/very-high-voltage spikes (switching spikes), battery reversal and battery voltage doubling.

All of these hazards must be withstood by the regulator without damage over an ambient temperature range very close to military standards (– 40 to + 125°C for underhood devices ; – 40 to + 85°C for other devices). Moreover, an output voltage precision of ± 4% to ± 2% is required over the whole temperature range and in all conditions of input voltage and load current.

BATTERY VOLTAGE DROP

During motor starting the battery is overloaded by a peak current of up to 100A drawn by the starter motor. In this condition, which persists for 20-30ms, the battery voltage drops to about 6V in very cold weather (figure 1).

Figure 1 : Cold Starting Supply Voltage Drop.



Using standard regulators with a dropout of 1.7V to 2.1V the minimum 4.75V supply necessary for essential functions such as ignition, injection and electronic engine control cannot be guaranteed. Another unfortunate consequence is the loss of RAM memory contents in car radios and trip computers.

A voltage regulator with a voltage drop of less than 1.2V is therefore necessary.

BATTERY VOLTAGE DOUBLING

To aid cold weather starting with a partially flat battery, sometimes two batteries are used in series, doubling the voltage. Regulators must therefore withstand input voltages of 24-26V without disturbing operation.

BATTERY REVERSAL

Voltage regulators must be protected internally against negative input voltages to guard against accidental battery reversal.

LOAD DUMP TRANSIENTS

Load dump transients are high voltage, high energy positive transients.

The response time of the output voltage of an alternator to load variations is very long because of the long time constant of the excitation winding and mechanical inertia.

When the load is reduced instantaneously (by turning off lights, cooling fans and so on) the output voltage of the alternator tends to present a positive peak, the amplitude of which depends on the speed of rotation and the excitation current.

During normal operation this does not cause problems because of the high capacity of the battery which, connected in parallel with the alternator output, is able to absorb the transient energy without a significant increase in voltage.

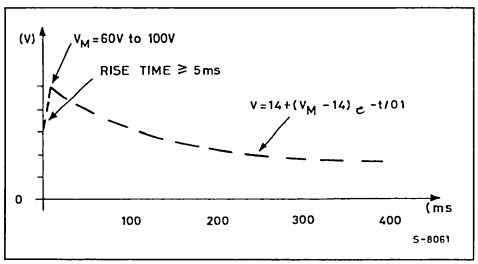
However, motor manufactures impose the standard that electronic devices must be protected against load dump transients because it is possible for the connection between battery and alternator to break.

The worst case voltage peak occurs when the battery-alternator cable is disconnected with the battery discharged and the motor running at its fastest rotation speed. In this case, the load variation is at a maximum and the voltage peak reaches a value comparable with the no-load output of the alternator running at maximum speed with the maximum excitation current.

Figure 2 shows a typical load dump waveform.

Motor manufacturers require that voltage regulators are able to protect themselves and the load against peak voltages of 60 - 100V with an equivalent series resistance of 0.1 to 1Ω , depending on the type of alternator and external protection device used.

Figure 2 : Load Drump Transient.



FIELD DECAY TRANSIENTS

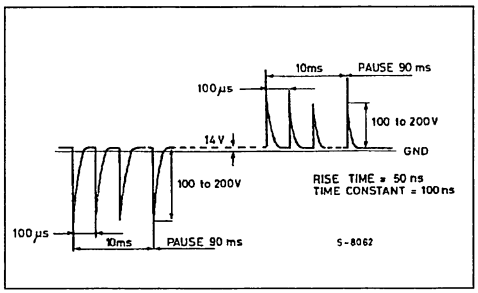
Field decay transients are high energy, high voltage negative transients.

If the ignition switch is turned off while current is flowing in inductive loads (electric motors, alternator field coil and so on) a negative voltage transient appears on the supply rail. The peak value in modulo of this transient is of the same order of magnitude as a load dump transient. In this case, too, the regulator must protect itself and the load.

SWITCHING SPIKES

Windscreen wiper motors, lamp flashers and ignition sparks behave as high frequency noise generators with an equivalent series resistance of 50 to 500 Ω. The energy associated with these transients is much lower than load dump or field decay transients but the negative and positive peaks can reach 200V. Figure 3 shows the voltage waveform which the regulators must withstand.

Figure 3 : Switching Spikes.



REGULATOR DESIGN

DROPOUT

The dropout voltage of a linear voltage regulator can be defined for a given output current, I_o, as the minimum difference between input and output voltage below which the output voltage is 100mV lower than the voltage measured at I_o with the nominal input voltage. The current I_o must be specified since the dropout voltage increases as the load current increases.

To obtain a dropout voltage of 0.05 to 1V with an output current of 10 to 50mA, the regulator types L387A, L487, L47XX, L48XX, L4920, L4921, LM2930A and LM2931A are configured with a PNP series-pass transistor as shown in figure 4. The PNP transistor is connected in the common emitter configuration and can therefore operate in saturation, yielding the low dropout voltage desired.

For higher dropout values an NPN series-pass element in emitter follower configuration may be used. This approach, shown in Figure 5, is used in the L2600 series regulators which have a maximum dropout voltage of 1.9V at 500mA.

Figure 4 : PNP Series Pass Transistor in Common Emitter Configuration for very Low Drop Out Voltage Regulators.

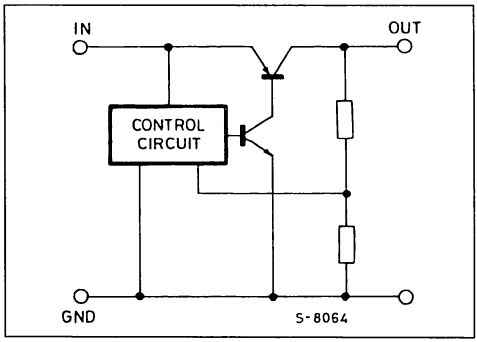
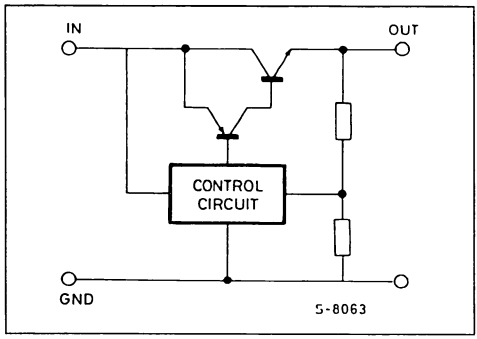


Figure 5 : NPN Series Pass Transistor in Emitter Follower Configuration.



CURRENT CONSUMPTION/QUIESCENT CURRENT

The circuit configurations shown in figures 4 and 5 behave differently as far as concerns the current consumed by the device but not delivered to the load. In the case of figure 5, this current is that necessary for the functioning of the auxiliary circuitry of the regulator (voltage reference, op amp and so on). The base current of the output transistor flows into the load.

In the Figure 4 circuit, in contrast, the base current of the output transistor does not flow through the load and, particularly in saturation, depends heavily on the load current.

Normally lateral PNP transistors are chosen for ICs because they can withstand high positive and negative overvoltages. When negative overvoltages at the input do not occur, or are eliminated by external protection devices, vertical PNP transistors can be used in place of lateral types.

Since vertical PNP transistors have higher gain the current consumed in the regulator is significantly reduced. Vertical PNP transistors will be used in future designs.

VOLTAGE REFERENCE

The wide operating range of input voltage (6 to 26V) and ambient temperature (40 to 125 °C) over which high output voltage precision is required means that a well stabilized voltage reference must be used.

All low drop regulators use bandgap type voltage references (see figure 6). In this structure the two transistors Q_2 and Q_1 have an emitter area ratio of 10 and carry equal collector currents imposed by the current mirror Q_3, Q_4, Q_5. In these conditions the base-emitter voltages of Q_1 and Q_2 differ (at 25 °C) by :

$$V_{BE} = \frac{KT}{q} 1n \frac{A(Q_2)}{A(Q_1)} = 60 \text{ mV}$$

where $\frac{A(Q_2)}{A(Q_1)} = 10$ (emitter area ratio)

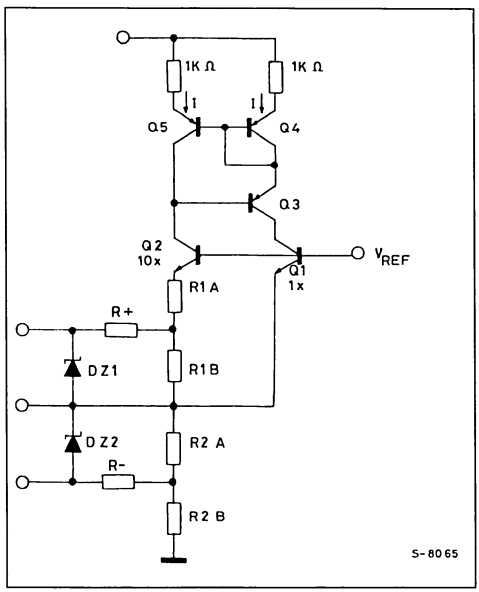
$\frac{KT}{q} = 26$ mV

K = Boltzmann's constant

T = Temperature in Kelvin

q = Charge on an electron

Figure 6 : Bandgap Voltage Reference Circuit in Low Drop Voltage Regulators.



The rejection of V_{ref} to variations in the supply voltage is improved by supplying the reference circuit from a stabilized voltage. This is achieved in the L26XX, L48XX, L4920, L4921, LM2930A and LM2931A regulators by means of a preregulator. In the L487, analysing the Figure 6 circuit gives :

$$V_{ref} = V_{BE}(Q_1) + 2\frac{R1}{R2}\Delta V_{BE}(Q_2, Q_1)$$

To maintain V_{ref} constant as temperature varies it is necessary that $\frac{d V_{ref}}{dT} = 0$ which implies choosing $\frac{R2}{R1}$ so that $\frac{2R2}{R1} \cdot \frac{60}{T(25\,^\circ)} + \frac{dV_{BE}(Q_1)}{dT} = 0$

where $T(25\,^\circ) = 298$ K

$\frac{d V_{BE}(Q1)}{dT}$ = negative temperature coefficient of the base-emitter voltage.

In L387A and L47XX regulators, in contrast, the supply to the bandgap is switched from the input to the output as soon as the nominal output voltage is reached (figures 7, 8, 9). The variation in output voltage with temperature is shown in figure 10.

Figure 7: Block Diagram of L2600 Series Regulators.

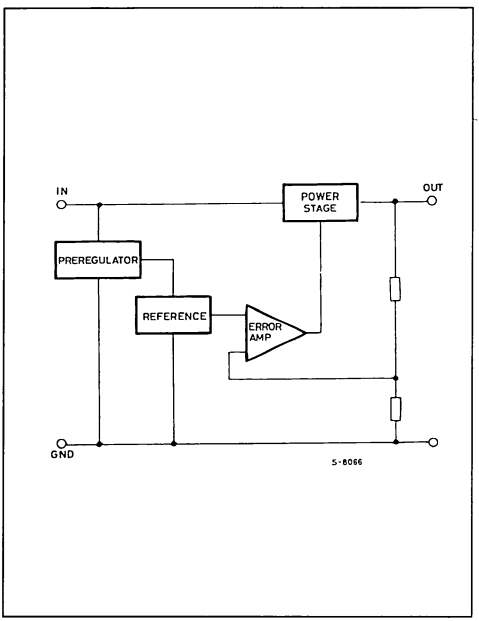


Figure 8 : Block Diagram of L387A and L487 Series Regulators.

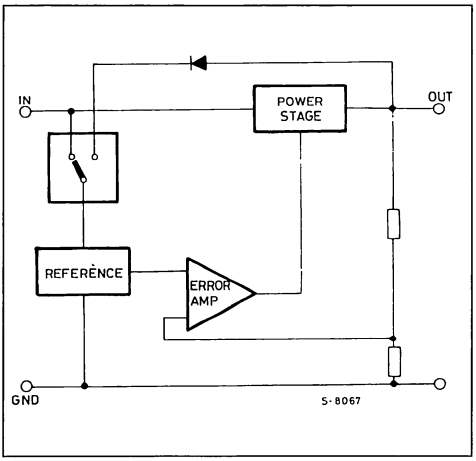


Figure 9 : Block Diagram of LM2930A, LM2931A and L4800 Series Regulators.

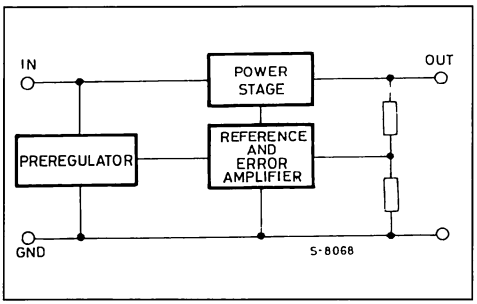
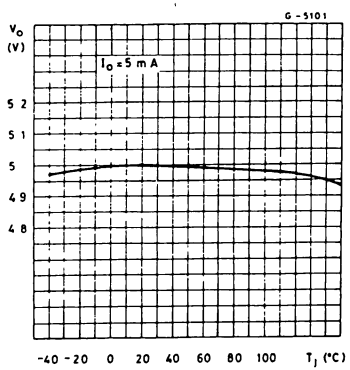


Figure 10 : Outputs Voltage vs. Temperature.



PROTECTION AGAINST HIGH ENERGY TRANSIENTS

To protect the LM2930A, LM2931A, L4920, L4921 and L48XX regulators against high-voltage, high-energy positive transients the basic circuit shown in Figure 11 is used. The zeners in this circuit limit the supply voltage to the maximum operating value and turn off the output stage. The output transistor can thus withstand voltages up to the BV_{CES} , break-down voltage.

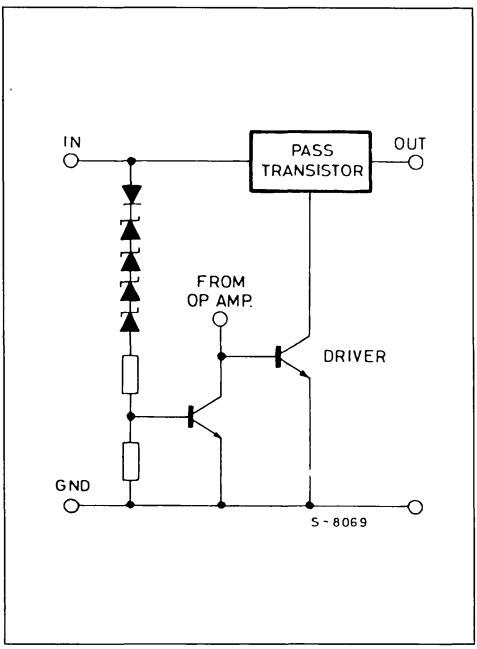
In the other regulators (L487, L387A, L47XX and L26XX) the supply to the internal circuits is also turned off.

The speed of intervention of these protection schemes is fast enough to ensure that the regulator can withstand high energy transients with a rising slope of 10V/µs without problems, interrupting normal operation only momentarily.

Protection against negative transients is provided by the high series impedance of the possible current paths and the reverse BV_{BEO} breakdown voltage of the lateral PNP transistors (BV_{CBO}).

The breakdown voltages BV_{CES} and BV_{CBO} depend on the technology therefore the transient capability is ± 60V, ± 80V or ± 100V for the various types.

Figure 11 : Overvoltage Protection Circuit.

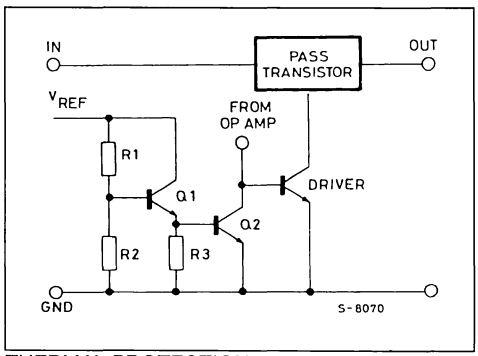


PROTECTION AGAINST LOW ENERGY OVERVOLTAGES

As shown in figure 3, the low energy overvoltages which the devices must resist have very brief rise time and can exceed the breakdown voltages. The protection schemes described above are therefore insufficient. However, since the energy associated with these transients is very low, the regulators can withstand them without problems. Nevertheless it is advisable to place a capacitor of around 100nF at the input.

All of the low drop regulators except the L26XX types need a compensation capacitor at the output. This capacitor also provides extra filtering for low energy transients because it has a low impedance at high frequencies.

Figure 12 : Thermal Protection Circuit.



THERMAL PROTECTION

When the junction temperature exceeds the safe maximum for the device a thermal protection circuit (figure 12) holds the output transistor off until the overtemperature condition has passed.

In the figure 12 circuit the resistors R1, R2 and R3 are calculated so that the base voltage of Q_1 is 600mV, thus preventing the conduction of Q_1 and Q_2.

As the junction temperature increases the minimum V_{BE} for conduction of the two transistors fall until, at about 15 °C, 2 V_{BE} = 600mV, the two transistors conduct and Q_2 turns off the output transistor driver.

CURRENT PROTECTION

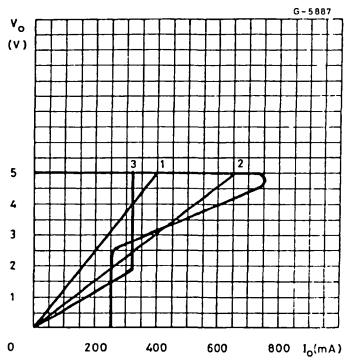
In the L487, L387A and L26XX regulators the output current is limited to its maximum value in the event of a short circuit. A special circuit acts on the base of the output transistor, preventing the output current from exceeding the limit set for the duration of the overload.

In the L4920, L4921, LM2930A, LM2931A and L48XX regulators a foldback circuit (figure 13) is used to limit the power dissipated in both the devices and the load in short circuit conditions. The current is limited to a low value (I_{sc}) of about 200 mA as soon as it exceeds the maximum value. The output voltage in this condition reaches a value corresponding to the current I_{sc} flowing through the load.

When the overload condition is removed the output voltage only returns to the nominal load value if the new static load line does not intersect the negative slope region of the curve in figure 13. If it does, the new operating point will be at the intersection.

It is important to note that when power is applied, if the load line intersects the curve in the negative slope region, the regulator will operate with a lower-than-nominal voltage. This can happen with a passive load greater than the normal load (even if it is less than the maximum load I_M) or with active loads such as a current sinker which draw more than I_{sc} even at low voltages (figure 13, curve 3).

Figure 13 : 1) Acceptable Load Line for Turn-on
2) Unacceptable Load Line for Turn-on.



EXTERNAL COMPENSATION

Since the purpose of a voltage regulator is to supply a fixed output voltage in spite of supply and load variations, the open loop gain of the regulator must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shifts due to other poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be the capacitor used to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequency too low to be compensated by a capacitor which can be integrated. For the L487, L47XX, L48XX, L387A, LM2930A and LM2931A external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The parassitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is 47 F (100 µF for L4800 series).

In the L2600, which uses an NPN power transistor, the stabilization capacitor is small enough to be integrated so no output capacitor is needed. Indeed, if an output capacitor is used it may cause oscillation unless it is greater than 100 µF, in which case it would itself be the dominant pole. If an electrolytic capacitor of more than 100 µF is used, a small capacitor must not be added in parallel or with the ESR of the electrolytic it would from another pole, worsening the stability of the system.

TURN-ON WITH CAPACITIVE LOADS

A load which presents a significant capacity between the output and ground (including the external compensation capacitor) will be seen by the regulator as a short circuit when power is applied. The regulator therefore delivers the short circuit current until the load capacitor has been charged to the nominal value.

This factor is extremely important for the dimensioning of the power source. Even a very small DC load can in such cases behave like a maximum load and the power drained from the supply is the sum of the short circuit current delivered to the load and the maximum current consumed in the regulator.

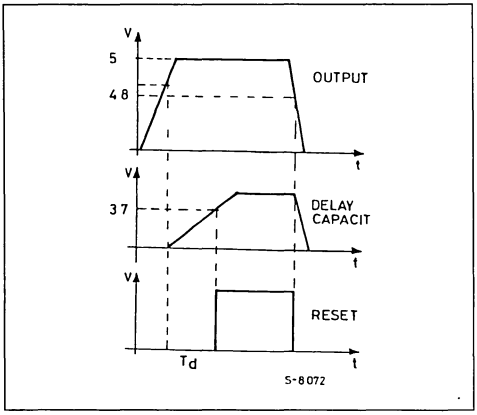
Moreover, as explained above, in regulators with foldback protection the static load line must not cross the negative slope region of figure 13 or the output voltage will not reach the nominal value when power is applied.

SPECIAL FUNCTIONS

RESET

The L387A and L487 include a power on/off reset function which inhibits the operation of circuits supplied by the regulator when the output voltage is too low (4.75V) to guarantee correct operation of logic (figure 14). To avoid malfunctions a delay is also introduced so that the enable signal is only issued some time after the safe output voltage has been reached.

Figure 14 : Reset Timing Waveforms.



The reset circuitry (figure 15) consists of :

- a comparator connected between the voltage reference and a tap of the output divider, the voltage of which is higher than the feedback voltage ;
- an SCR to memorize any brief glitches in the output voltage that can cause some trouble with the logic.
- a delay circuit with an external capacitor charged by an internal current source

This function has been integrated into the voltage regulator to exploit the basic advantage of taking information at the source. The use of double calibrations can thus be avoided.

For the correct operation of the reset function, two basic relations must be satisfied in all cases

$V_{res\ max} < V_{out\ min}$ (1)
$V_{res\ min} > 4.75\ V$ (2)

where $V_{res\ max}/V_{res\ min}$ are maximum/minimum value for the reset signal going high-low.

(1) means that the RESET signal must be high when the device is regulating

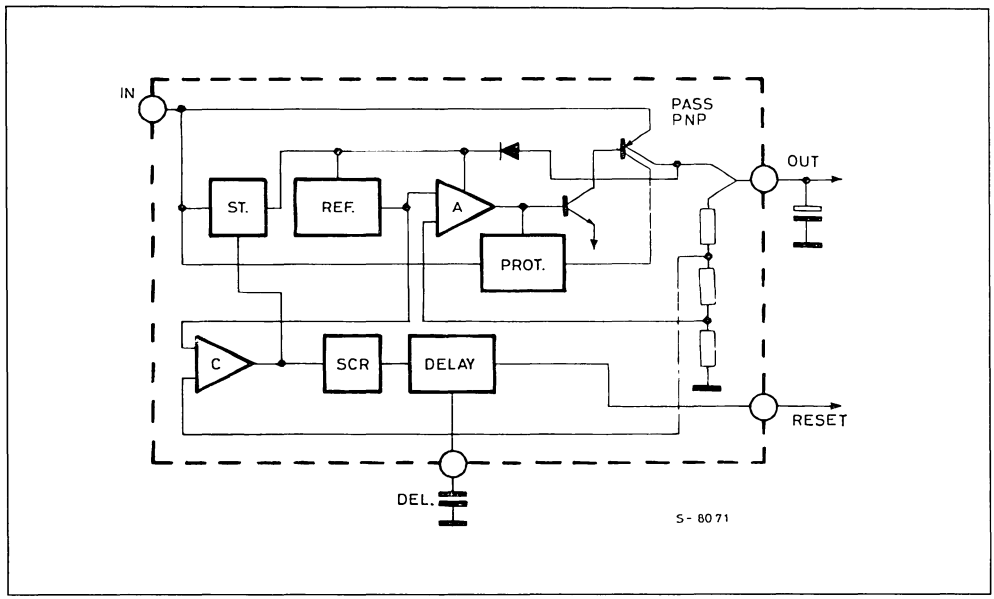
(2) means that the RESET signal must be low when the output voltage goes under 95 % of the nominal (5V). Expressions (1) and (2) can be rewritten as :

$(V_{res\ max}\ V_{res\ min}) + (V_{nom}\ V_{out\ min})$ (3)
$< V_{nom}\ 4.75V$

This means that the sum of all the errors in the worst case must be less than 5 % (250mV).

- absolute spread of the reference
- error due to the load regulation (1 % max)
- error due to the offset of the reset comparator and error amplifier (0.5 %)
- errors due to the output divider (0.5 %)
- hysteresis of the comparator to speed up the transitions (50mV that is 1 % referred to 5V output)

Figure 15 : Schematic Block Diagram of a Voltage Regulator with Reset Function.

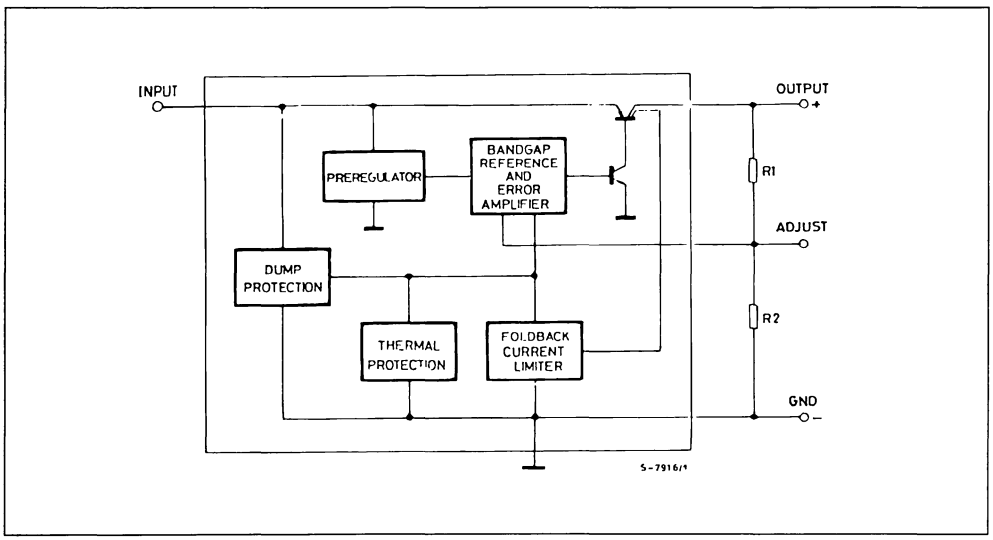


VARIABLE OUTPUT VOLTAGE

The L4920 and L4921 are structurally identical to L48XX series regulators except that the voltage divider in the feedback loop is available externally (figure 16). The output voltage can therefore be varied from 1.25V (the reference voltage) to 20V. It should be noted, however, that the minimum input voltage is 5.1V for operation with output voltages below 4.5V (otherwise the internal circuits will not work). For output voltages above 4.5V the input voltage must be at least equal to the output voltage plus the dropout voltage. The L4920 and L4921 are therefore low dropout regulators only for voltages above 4.5V.

A value of 6 KΩ is recommended for R2 to match the internal circuitry.

Figure 16 : The L4920 and L4921 are Structurally Identical to L48XX Series Regulators Except that the Voltage Divider in the Feedback Loop is Available Externally.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

THERMAL CHARACTERISTICS OF THE MULTIWATT PACKAGE

By R. TIZIANI

INTRODUCTION

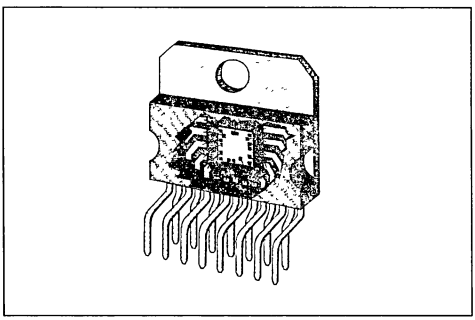
This Application Note provides a complete thermal characterization of the Multiwatt ® package (multilead double TO-220 - fig. 1).

Characterization is performed according with recomandations included in the G32-86 SEMI guideline, by means of a dedicated test pattern. It refers to :

1. Junction to case thermal resistance $R_{th(j-c)}$
2. Junction to ambient thermal resistance $R_{th(j-a)}$
3. Junction to ambient thermal impedance for single pulses and repated pulses, with different pulse width and duty cycle ;
4. Thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techniques.

Figure 1 : Multiwatt Assembly.



EXPERIMENTAL CONDITIONS

The thermal evaluation was performed by means of the test pattern P432, which is a 20K mils^2 die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 2K mils^2 with a power capability of 20W. Measurement method is described in Appendix A.

Samples with the indicated characteristics were prepared :

Package Multiwatt 15 leads

Frame Material	Copper
Slug Thickness	1.5mm
Slug Thermal Conductivity	3.9W/cm°C
Die Attach	Soft (PbSn)

Measurement of junction to case thermal resistance $R_{th(j-c)}$ is performed by holding the package against a water cooled heat sink, according with fig. 2. A thermocouple placed in contact with the slug measures the reference temperature of the case.

For junction to ambient thermal resistance $R_{th(j-a)}$ the samples are suspended horizontally in a one cubic foot box, to prevent drafts.

Both DC and pulsed conditions are used ; in the second case the contribution of package thermal capacitance is effective and transient thermal resistances much lower than the steady stata $R_{th(j-a)}$ can be found, according to pulse length and duty cycle.

The effect of the external heat sink is quantified, using as test vehicle the commercially available heat sink THM7023 especially developed by Thermalloy for the Multiwatt package, whose thermal resistance in still air is about 9°C/W.

The measurement circuit shown in fig. A3 was used for all the thermal evaluations.

JUNCTION TO CASE THERMAL RESISTANCE

The dependance of $R_{th(j-c)}$ on the dissipated power is reported in fig. 3.

It is well known that the main contribution to $R_{th(j-c)}$ of power packages in given by the silicon die.

Figure 2 : Measurement of $R_{th\ (j-c)}$.

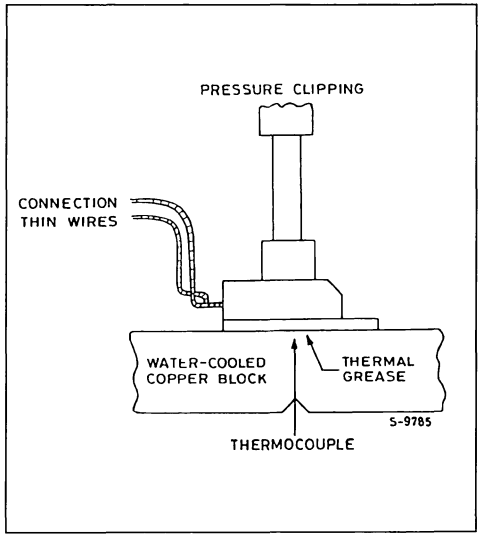
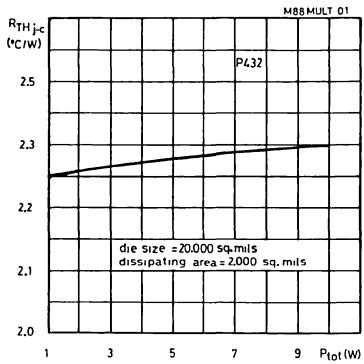


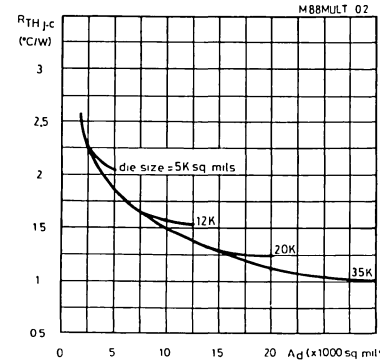
Figure 3 : $R_{th\ (j-c)}$ of Multiwatt Package vs. Power Level.



FOR DEVICES OTHER THAN THE TEST PATTERN P432 THE CALIBRATION CURVE OF FIG. 4 IS NEEDED.

It shows the relationship between $R_{th(j-c)}$ and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

Figure 4 : $R_{th(j-c)}$ Thermal Resistance vs. Die Size and on Die dissipating Area.



JUNCTION TO AMBIENT THERMAL RESISTANCE

In medium power applications (1.5-2W), the Multiwatt package can be used without external heat sink, thanks to the significant size (about 3.5cm^2) of its integrated thermal mass.

Its $R_{th(j-a)}$ has two contributions : the $R_{th(j-c)}$, mainly due to the silicon die (as shown in fig. 4) and the thermal resistance of the copper slug $R_{th\ slug}$.

Figure 5 : $R_{th(j-a)}$ of Multiwatt Package vs. dissipated Power.

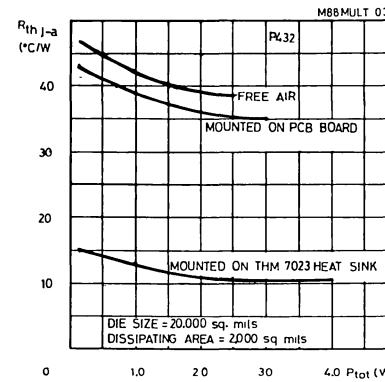


Fig. 5 gives the relationship between $R_{th(j-a)}$ and the power dissipation level for the P432 test pattern is still air, on PC board and on a commercial heat sink.

IN ORDER TO HAVE AN ACCURATE VALUE FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 5 SHOULD BE CORRECTED THROUGH THE CALIBRATION CURVE OF FIG. 4 CORRECTION TERM IS ALWAYS IN THE RANGE OF 0-2°C/W ; THEREFORE, IT AFFECTS THE $R_{th(j-a)}$ OF NO MORE THAN 5% IN STILL AIR OR WITH THE PACKAGE MOUNTED ON PC BOARD.

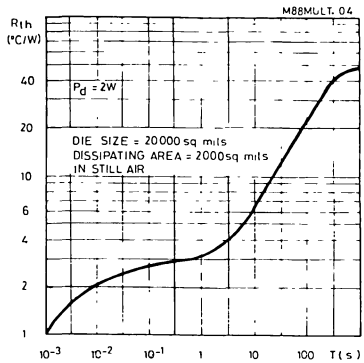
TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (without external heat sink)

The effect of single pulses of different length and height for the Multiwatt package without any external heat sink is shown in fig. 6.

This behaviour is discussed in Appendix B. Due to a significant thermal capacitance (C = 2J/°C) and correspondingly long risetime (τ = 80s), single pulses up to 30W can be delivered to the Multiwatt package for 1s with acceptable junction temperature increase.

IN ORDER TO HAVE ACCURATE R_{th} (t_0 FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 7 MUST BE CORRECTED AS DESCRIBED IN EXAMPLE 2 OF THE LAST SECTION.

Figure 6 : Transient Thermal Resistance for Single Pulse.



Repetition of pulses with defined P_d, period and duty cycle DC (ratio betwen pulse length and signal period), gives rise to oscillations in junction temperature as described in Appendix B.

The transient thermal resistance corresponding to the upper limit of the curve of fig. B4 (peak transient thermal resistance) is reported in fig. 7 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (with external heat sink)

Characterization has been repeated with a commercial heat sink (Thermalloy THM7023) in order to have an example of the effect of an external thermal mass on the impedance of the thermal module.

Relationship between transient R_{th} and pulse length is reported in fig. 8.

The effect of the increased thermal capacitance is evident in fig. 9, where thermal data of fig. 6 and 8 are compared : it can be noticed that the curves are definitely different for pulses longer than 1s, corresponding about to the rise time of the slug. The effect of the thermal mass is to keep low the heating rate of the silicon die thus allowing a better power management of long power pulses. This conclusion has general validity and can be applied to other heat sinks than the one considered in this note.

Figure 7 : Peak Transient R_{th} vs. Pulse width and Duty Cycle.

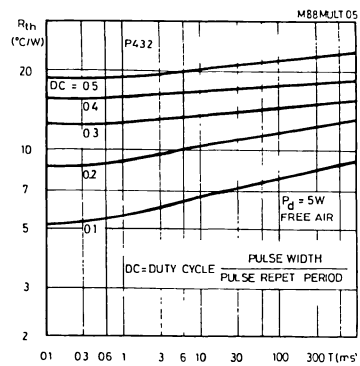


Figure 8 : Transient R_{th} for single pulses, with Heatsink.

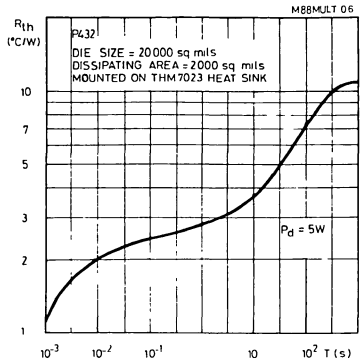
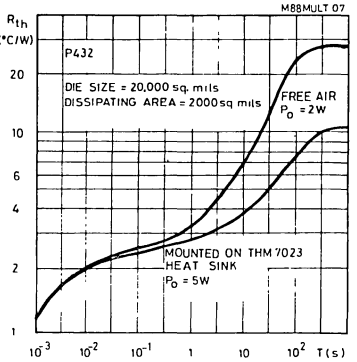


Figure 9 : Comparison of Transient R_{th} for single pulses, with and without Heat Sink.



APPENDIX A

The thermal resistance evaluation is performed with the especially designed test chip P432 which has two bipolar power transistor and one sensing diode (fig. A1). The active area is about 2000 $mils^2$ on a 35000$mils^2$ chip. Its lay-out was optimized in order to have a uniform temperature area, once the two transistor are powered ; the sensing diode is placed at the center of this area.

The relationship between the forward voltage V_f of the diode at the constant current of 100µA and the temperature is shown in fig. A2. The curve calibrates the junction temperature through the voltage drop of the diode.

The measurement circuit is shown in fig. A3. A storage oscilloscope or a fast digital voltmeter can be used for recording the V_f value.

Figure A1 : Test Pattern P432 Lay-out.

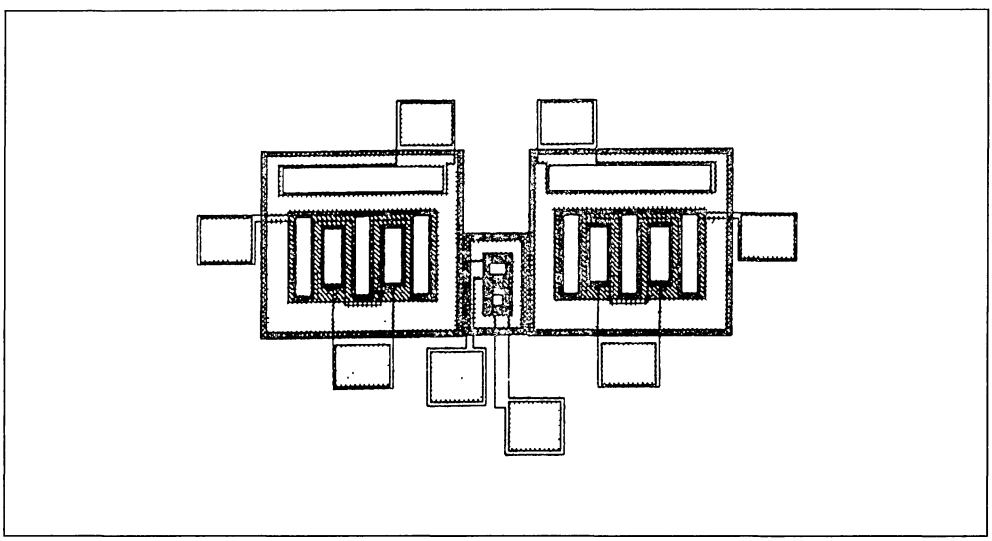


Figure A2 : Calibration Curse (sensing diode).

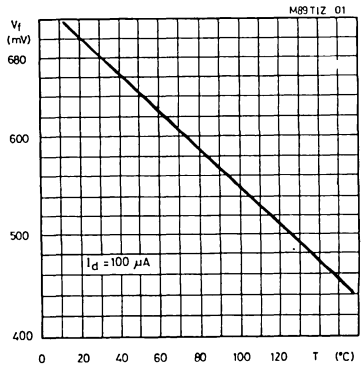
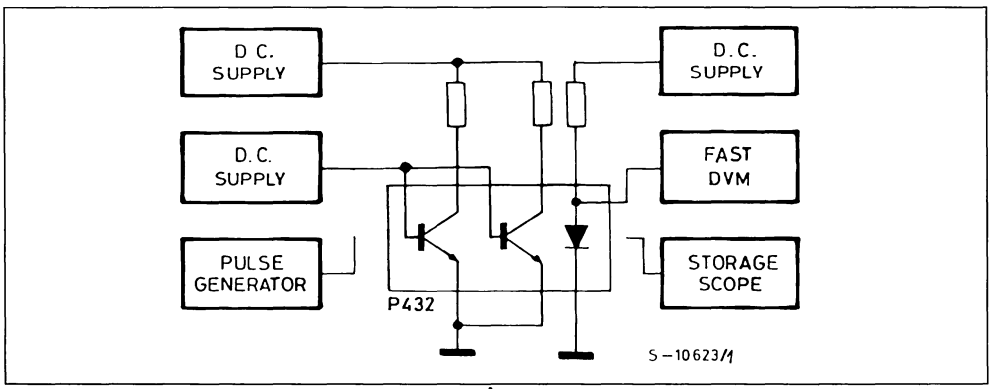


Figure A3 : Measurement Circuits.



APPENDIX B - THERMAL MANAGEMENT IN PULSED CONDITION

THERMAL RESISTANCE AND CAPACITANCE

The electrical equivalent of heat dissipation, for a thermal module formed by the active device with its package and the external heat sink is shown in fig. B1.

To each cell of the thermal chain are associated a value of thermal resistance R_{th} (°C/W) and a value of thermal capacitance C_{th} (J/°C). The former informs about temperature increase due to the element represented by the cell ; as, in the example under consideration, heat transfer is mainly based on conduction for the silicon, the copper integrated heat sink and to metallic body of the external heat sink R_{th} can be calculated from the relationship :

$$R_{th} = \frac{\gamma}{K \times S}$$

where K is the thermal conductivity of the material, the length of the conductive path and S its section.

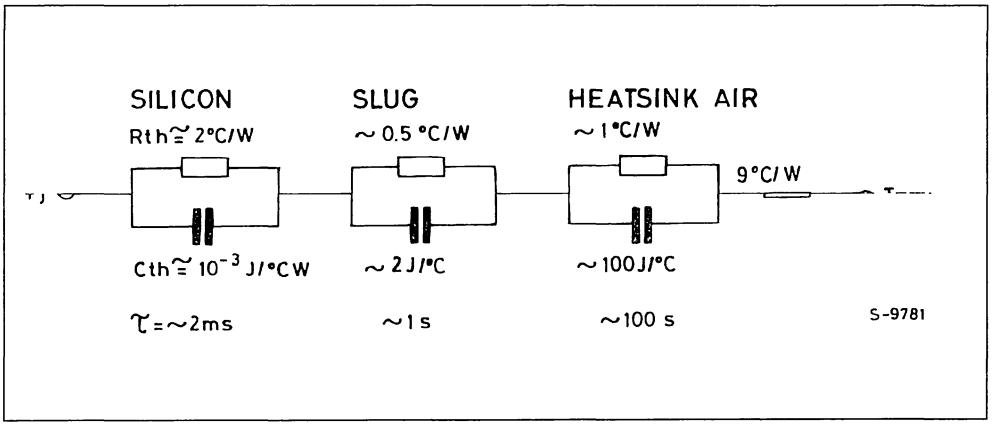
Thermal capacitance C_{th} is the capability of heat accumulation ; it depends on the specific heat of the material and on the volume effectively interested by heat exchange (this means that the parts which are not heated during heat dissipation DO NOT contribute to thermal capacitance). Thermal capacitance is given by :

$$C_{th} = d \times c_t \times V$$

where d is the density of the material, c_t its specific heat and V the volume interested to heat accumulation.

The last element of the network, assumed as purely resistive, is due to convection and radiation from the external heat sink towards the ambient.

Figure B1 : Electrical Equivalent of Multiwatt Package Mounted on the External Heatsink.



Each cell has its own risetime τ , given by the product of the thermal resistance and capacitance :

$$\tau = R_{th} \times C_{th}$$

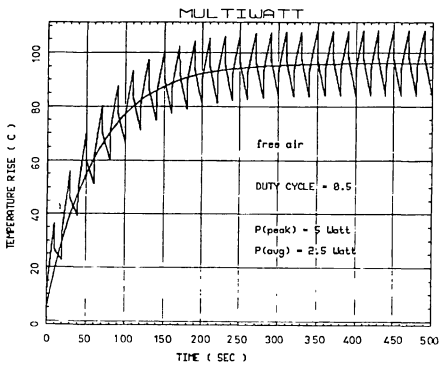
The value of the time constant determines whether a cell approaches equilibrium rapidly of slowly : if R_{th} or C_{th} increases, equilibrium is reached at a slower rate. The following relationship is valid for each cell :

$$\Delta T = R_{th} \times P_d \left[1 - e^{-t/r}\right] (1)$$

Typical values of R_{th}, C_{th} and τ for Multiwatt application are shown in fig. B1.

When power is switched on, temperature increase is ruled by subsequent charging of thermal capacitances while the value reached in the steady state depends on thermal resistances only. Qualitative behaviour of the network of fig. B1 is shown in fig. B2.

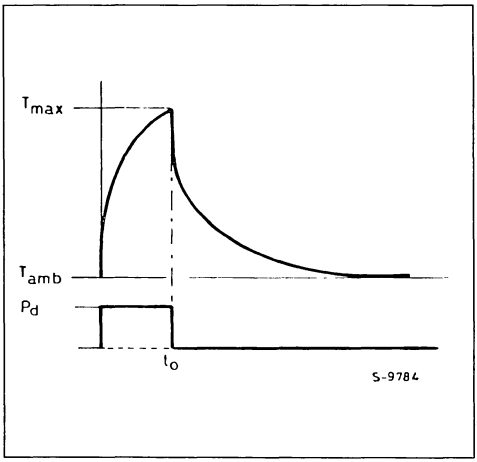
Figure B2 : Qualitative T_j increase (network of fig. B1) for repeated Power Pulse.



SINGLE POWER PULSE

When the pulse length has an assigned value, effective T_j can be significantly lower than the steady state T_j (fig. B3.).

Figure B3 : Effect of a Single Power Pulse.



For any pulse length t_o, a transient thermal resistance R_{th} (t_o) is defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power. Obviously, for shorted pulses, R_{th} (t_o) is lower and a higher power can be dissipated, without exceeding the maximum junction temperature $T_{j\text{-}max}$ allowed to the IC from reliability considerations. Fig. 7 and 9 of this Application Note give experimental values of R_{th} (t_o) for the two cases of the Multiwatt package without and with external heat sink.

REPEATED PULSES

When pulses of the same height P_d are repeated with a defined duty cycle DC and pulse length is short in comparison with the total risetime of the system (many tens of seconds) the train of pulses is seen by the system as a continuous source, at a mean power level of

$$P_{davg} = P_d \times DC$$

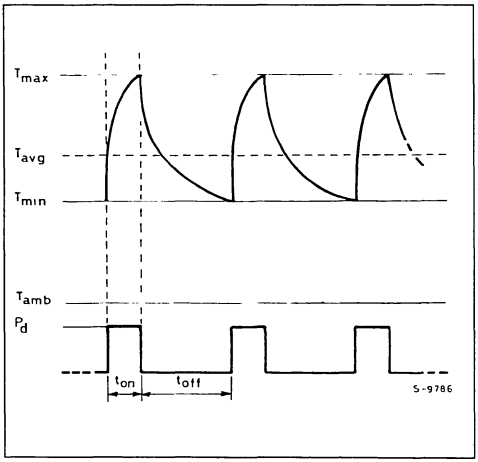
The average temperature increase is :

$$\Delta T_{avg} = R_{th} \times P_{davg} = R_{th} \times P_d \times DC$$

On the other hand, the silicon die (τ_S = 1– 3ms) is able to follow frequencies of some KHz and junction temperature oscillates about the average as qualitatively shown in fig. B4.

The thermal resistance corresponding to the peak of the oscillation at equilibrium (peak thermal resistance $R_{th\,peak}$) is now given by fig. 5, and can be obtained if pulse length and duty cycle are known ; P_{dmax} is derived from the same figure.

Figure B4 : Junction Temperature increase for repeated Pulses.



APPLICATION EXAMPLES

EXAMPLE 1 - MAXIMUM P_d FOR SINGLE PULSE OF ASSIGNED LENGTH

PROBLEM : define the maximum P_d for a single pulse with a length of 20ms in the case of Multiwatt package used without heat sink. Ambient temperature is 50°C ; maximum temperature is 130°C. Die size is 20K mils^2, with dissipating area of 2K mils^2 (as in P432 test pattern).

SOLUTION : allowed temperature increase ΔT is 80°C. Having a $R_{th(j\text{-}a)}$ of 39°C/W, Multiwatt package can dissipate about 2W in steady state. From fig. 7 the transient thermal resistance corresponding to one single pulse of 20ms is R_{th} (20ms)$_{P432}$ = 2.2°C/W. A peak of 80/2.2 = 36.3W can be applied to the circuit.

EXAMPLE 2 - CORRECTION FOR DIE SIZE AND DISSIPATING AREA

PROBLEM : correct the results obtained in example 1, for assigned die size and dissipating area. Practical case : IC having a die size of 35K mils^2 with a dissipating area of 20k mils^2.

SOLUTION : from fig. 5, thermal resistances of P432 and of the IC under consideration are $R_{th\,P432}$ = 2.3°C/W and $R_{th(j\text{-}c)IC}$ = 1.2°C/W.

As the length of the pulse is 10-15 times longer than the rise time of the silicon, the die (first cell of fig. B1) can be assumed to have reached its equilibrium condition.

R_{th} (20ms) found in previous example has to be corrected in order to take into account the new value of $R_{th(j-c)}$:

$$R_{th}\ (20ms)_{IC} = R_{th}\ (20ms)_{P432} - R_{th(j-c)P432} + R_{th(j-c)IC} =$$
$$= 2.2 - 2.3 + 1.2^{\circ}C/W = 1.1^{\circ}C/W$$

A single pulse of 80/1.1 ≅ 72W can be delivered to such device.

When the pulse has the same order of silicon rise time τ P432 is about 1ms) another type of correction is needed. In first approximation, τ increase with dissipating area with the relationship :

$$t_{IC} = \sqrt{20K_{IC}/2K_{P432} \times \tau_{P432}} \cong 3.1ms$$

Expansion of the exponential term of relationship (1) limited to the first term term, is :

$$R_{th\ IC}\ (t_o) \cong R_{th\ P432}\ (t_o)\ /3.1$$

for t_o = 1ms :

$$R_{th\ IC}\ (1ms) = 1.05/3.1^{\circ}C/W \cong 0.34^{\circ}C/W$$

A single pulse of 80/0.34 ≅ 235W can be delivered to such device.

EXAMPLE 3 – R_{th} WITH REPEATED PULSES

PROBLEM : find the peak power which can be dissipated by Multiwatt package without heatsink, when power is continuously switched on 10ms and switched off 90ms. Ambient temperature is 50°C, maximum temperature is allowed to be 125°C.

SOLUTION : a maximum ΔT = 75°C has to be considered. Fig. 5 indicated that for a pulse width of 10ms and a duty cycle of 0.1, $R_{th\ peak}$ is 6.7°C/W. Maximum P_d is 75/6.7 = 11.2W, with an average temperature increase ΔT_{peak} of 39 x 0.1 x 11.2 ≅ 43°C.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

THERMAL CHARACTERISTICS OF THE PENTAWATT-HEPTAWATT PACKAGES

By R. TIZIANI

INTRODUCTION

This Application Note is aimed to give a complete thermal characterization of the Heptawatt and Pentawatt package (fig. 1, 2).

Characterization is performed according with recomendations included in the G32-86 SEMI guideline, by means of a dedicated test pattern. It refers to :

1. Junction to case thermal resistance $R_{th(j-c)}$
2. Junction to ambient thermal resistance $R_{th(j-a)}$
3. Junction to ambient thermal impedance for single pulses and repeated pulses, with different pulse width and duty cycle ;
4. thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techniques.

Figure 1 : Pentawatt.

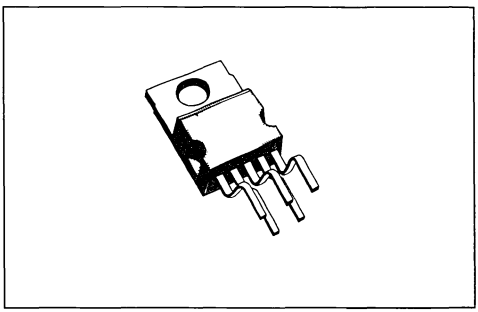
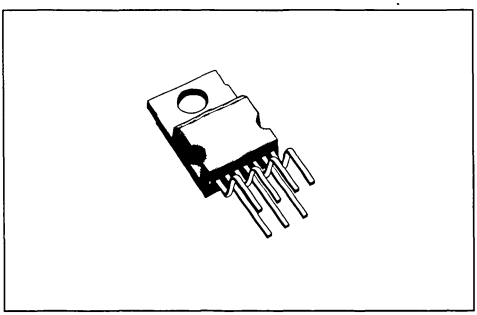


Figure 2 : Heptawatt.



EXPERIMENTAL CONDITIONS

The thermal evaluation was performed by means of the test pattern P432, which is a 15k mils^2 die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 2k mils^2 with a power capability of 20W. Measurement method is described in Appendix A.

Samples with the indicated characteristics were prepared :

Package	Pentawatt - Heptawatt
Frame Material	Copper
Slug Thickness	1.25mm Typ.
Slug Thermal Conductivity	3.9W/cm°C
Die Attach	Soft (PbSn)

Measurement of junction to case thermal resistance $R_{th(j-c)}$ is performed by holding the package against a water cooled heat sink, according with fig. 3. A thermocouple placed in contact with the slug measures the reference temperature of the case.

For junction to ambient thermal resistance $R_{th(j-a)}$ the samples are suspended horizontally in a one cubic foot box, to prevent drafts.

Both DC and pulsed conditions are used ; in the second case the contribution of package thermal capacitance is effective and transient thermal resistances much lower than the steady state $R_{th(j-a)}$ can be found, according with pulse length and duty cycle.

The effect of the external heat sink is quantified, using as test vehicle the commercially available heat sink THM7023 (Thermalloy) whose thermal resistance in still air is about 9°C/W.

The measurement circuit shown in fig. A3 was used for all of the thermal evaluations.

JUNCTION TO CASE THERMAL RESISTANCE

The dependance of $R_{th(j-c)}$ on the dissipated power is reported in fig. 4. The absolute value and the behaviour with the dissipated power are the same for

both packages as the slug thickness and the die - attach are equal.

Figure 3 : Measurement of $R_{th\ (j-c)}$.

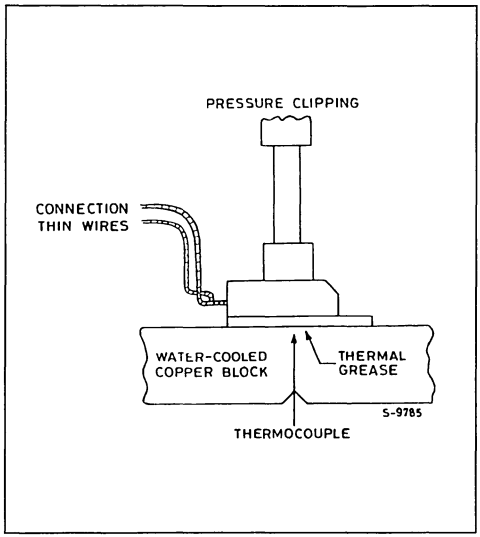
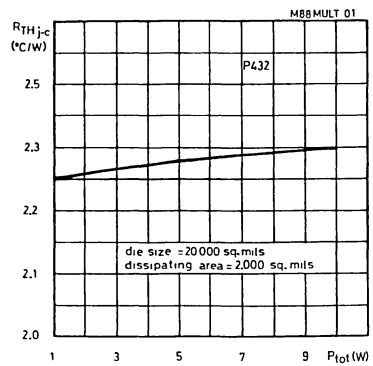


Figure 4 : $R_{th\ (j-c)}$ of Pentawatt and Heptawatt Package vs. Power Level.

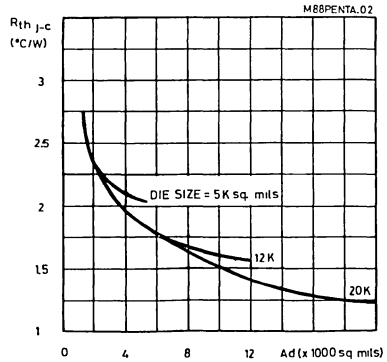


It is well known that the main contribution to $R_{th(j-c)}$ of power packages is given by the silicon die.

FOR OTHER DEVICES THAN THE TEST PATTERN P432 THE CALIBRATION CURVE OF FIG. 5 IS NEEDED.

It shows the relationship between $R_{th(j-c)}$ and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

Figure 5 : $R_{th\ (j-c)}$ Thermal Resistance vs. Die Size and on Die dissipating Area.



JUNCTION TO AMBIENT THERMAL RESISTANCE

In medium power application (1W), the Pentawatt and Heptawatt packages can be used without external heat sink thanks to the significant size (about 1.5cm^2) of its integrated thermal mass.

An effective cost solution for higher power application (1.5-2.0W) is using a copper area heat sink.

An board with the external leads bent down as shown in fig. 7.

Fig. 6 gives the relationship between $R_{th(j-a)}$ and the power dissipation level for the P432 test pattern in still air, on PC board, on integrated heat sink on board and on a commercial heat sink.

IN ORDER TO HAVE AN ACCURATE VALUE FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 6 SHOULD BE CORRECTED THROUGH THE CALIBRATION CURVE OF FIG. 5 CORRECTION TERM IS ALWAYS IN THE RANGE OF 0-2°C/W ; THEREFORE, IT AFFECTS THE $R_{th(j-a)}$ OF NO MORE THAN 5% IN STILL AIR OR WITH THE PACKAGE MOUNTED IN PC BOARD.

Figure 6 : $R_{th\ (j-a)}$ vs. dissipated Power (heptawatt).

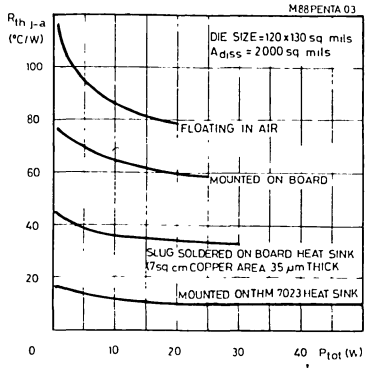
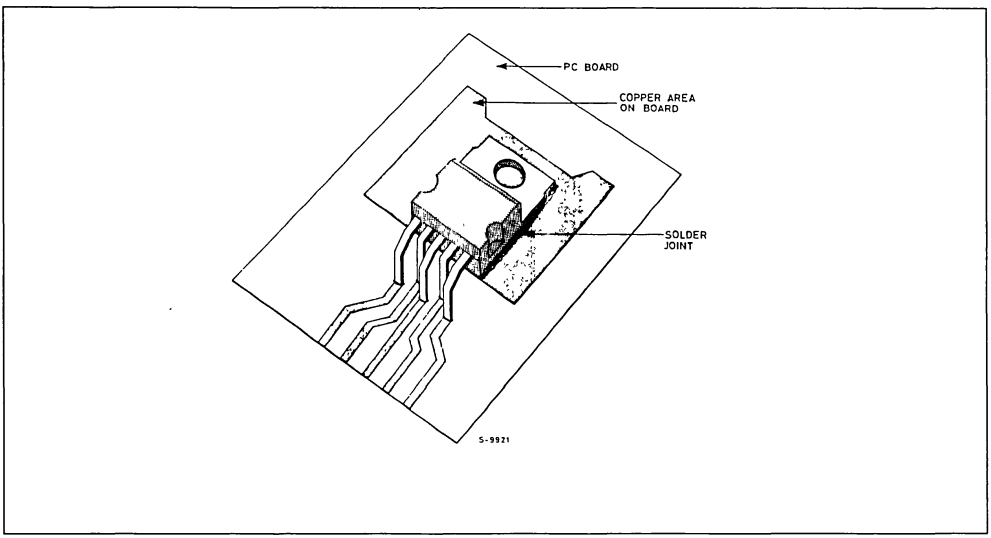


Figure 7 : Pentawatt Soldered on Copper Heatsink on P.C Board.

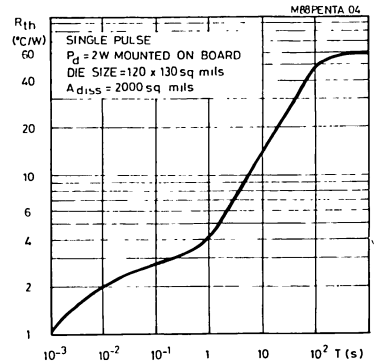


TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (without external heat sink)

The effect of single pulses of different length and height without any external heat sink is shown in fig. 8.

This behaviour is discussed in Appendix B. Due to a significant thermal capacitance (C = 1J/°C) and a correspondingly long risetime (τ = 80s), single pulses up to 20W can be delivered for 1 s with acceptable junction temperature increase.

Figure 8 : Transient Thermal Resistance for Single Pulses (heptawatt).

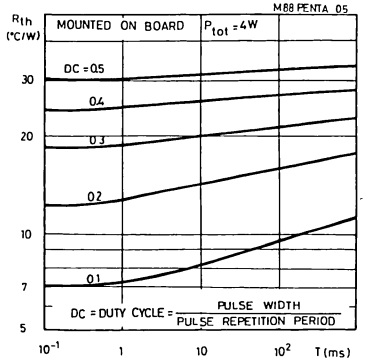


IN ORDER TO HAVE ACCURATE $R_{th}(t_o)$ FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 7 MUST BE CORRECTED AS DESCRIBED IN EXAMPLE 2 OF THE LAST SECTION.

Repetition of pulses with defined Pd, period and duty cycle DC (ratio between pulse length and signal period), gives rise to oscillations in junction temperature as described in Appendix B.

The transient thermal resistance corresponding to the upper limit of the curve of fig. B4 (peak transient thermal resistance) is reported in fig. 9 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

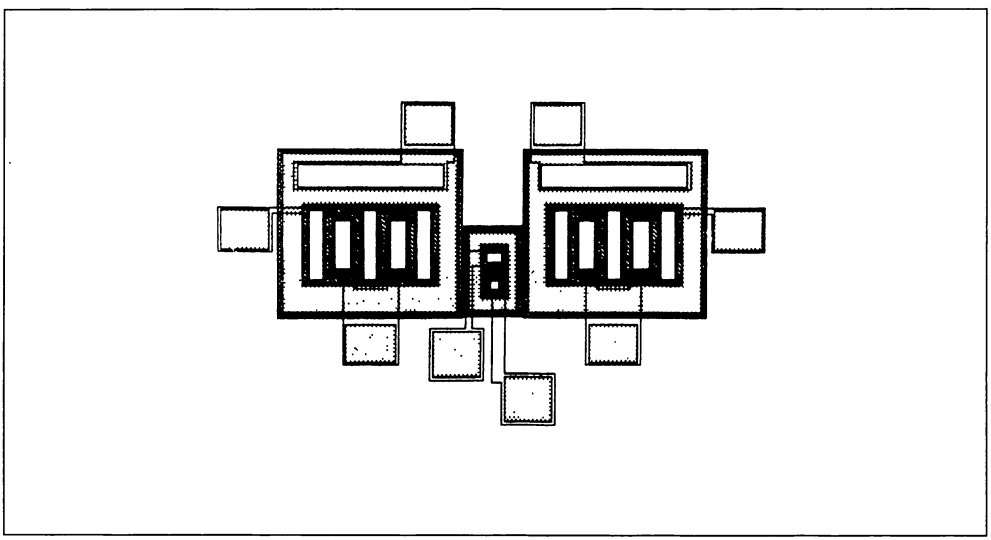
Figure 9 : Peak Transient R_{th} vs Pulse width and Duty Cycle (heptawatt).



APPENDIX A

The thermal resistance evaluation is performed with the especially designed test chip P432 which has two bipolar power transistor and one sending diode (fig. A1). The active area is about 2000 $mils^2$ on a 15000 $mils^2$ chip. Its lay-out was optimized in order to have a uniform temperature area, once the two transistor are powered ; the sensing diode is placed at the center of this area.

Figure A1 : Test Pattern P432 Lay-out.



The relationship between the forward voltage V_f of the diode at a constant current of 100µA and the temperature is shown in fig. A2. The curve calibrates the junction temperature through the voltage drop of the diode.

The measurement circuit is shown in fig. A3. A storage oscilloscope or a fast digital voltmeter can be used for recording the V_f value.

Figure A2 : Calibration Curve (sensing diode).

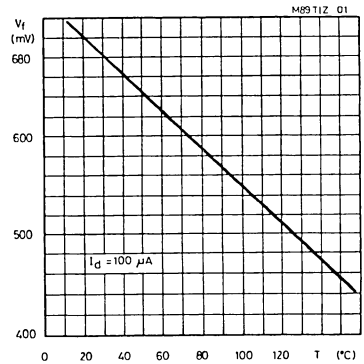
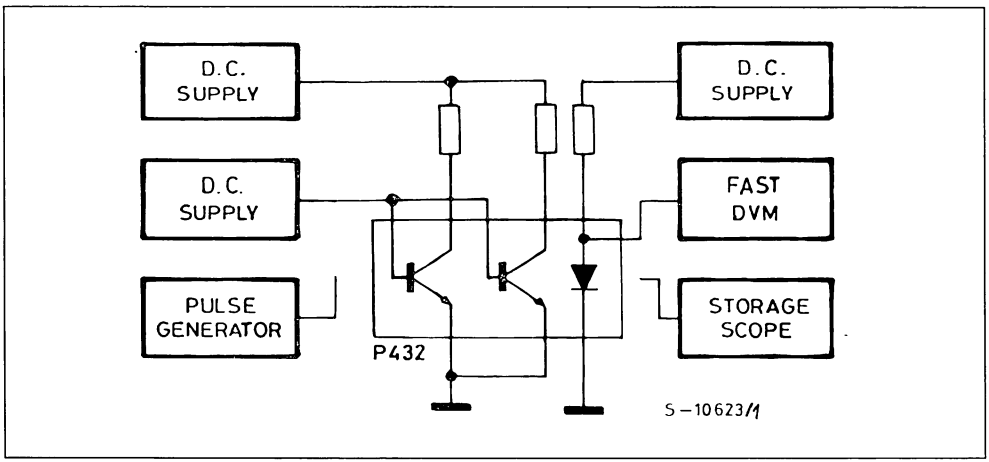


Figure A3 : Measurement Circuit.



APPENDIX B - THERMAL MANAGEMENT IN PULSED CONDITION

THERMAL RESISTANCE AND CAPACITANCE

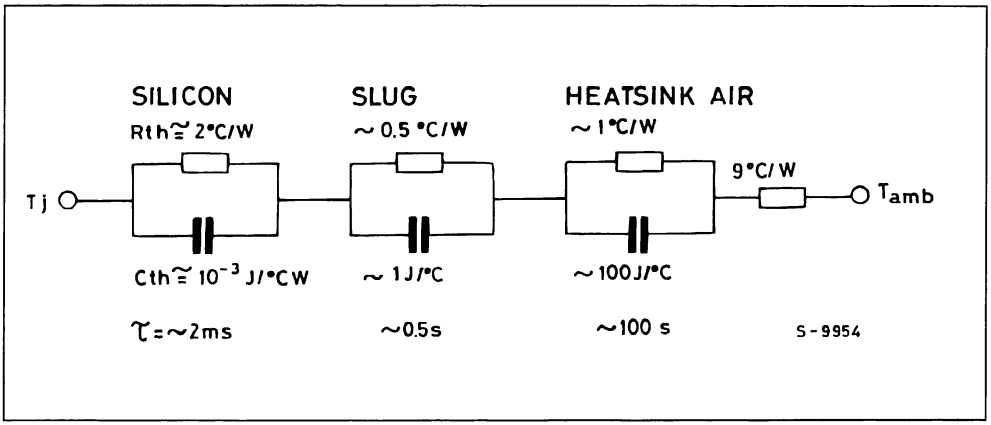
The electrical equivalent of heat dissipation, for a thermal module formed by the active device with its package and the external heat sink is shown in fig. B1.

To each cell of the thermal chain are associated a value of thermal resistance R_{th} (C/W) and a value of thermal capacitance C_{th} (J/°C). The former informs about temperature increase due to the element represented by the cell ; as, in the example under consideration, heat transfer is mainly based on conduction for the silicon, the copper integrated heat sink and to metallic body of the external heat sink Rth can be calculated from the relationship :

$$R_{th} = \frac{1}{K \times S}$$

Where K is the thermal conductivity of the material, 1 the length of the conductive path and S its section.

Figure B1 : Electrical Equivalent of Pentawatt and Heptawatt Package mounted on the External Heatsink.



Thermal capacitance C_{th} is the capability of heat accumulation ; it depends on the specific heat of the material and on the volume effectively interested by heat exchange (this means that the parts which are not heated during heat dissipation DO NOT contribute to thermal capacitance). Thermal capacitance is given by :

$$C_{th} = d \times c_t \times V$$

where d is the density of the material, c_t its specific heat and V the volume interested to heat accumulation.

The last element of the network, assumed as purely resistive, is due to convection and radiation from the external heat sink towards the ambient.

Each cell has its own risetime τ, given by the product of thermal resistance and capacitance :

$$\tau = R_{th} \times C_{th}$$

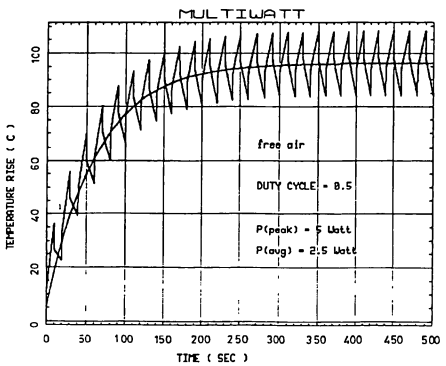
The value of the time constant determines whether a cell approaches equilibrium rapidly or slowly : if R_{th} or C_{th} increases, equilibrium is reached at a slower rate. The following relationship is valid for each cell :

$$\Delta T = R_{th} \times P_d \times [1 - e^{-t/\tau}] \quad (1)$$

Typical values of R_{th}, C_{th} and τ for Heptawatt and Pentawatt application are shown in fig. B1.

When power is switched on, temperature increase is ruled by subsequent charging of thermal capacitance while the value reached in the steady state depends on thermal resistance only. Qualitative beahaviour of the network of fig. B1 is shown in fig. B2.

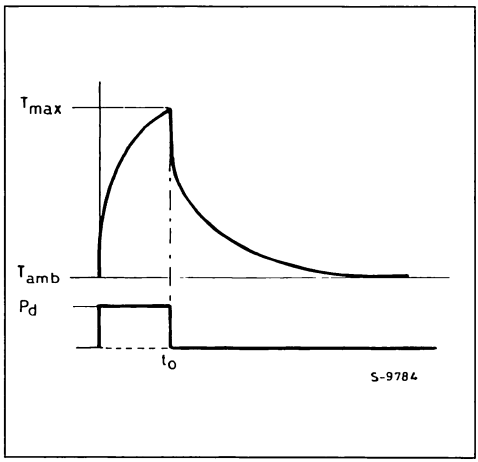
Figure B2 : Qualittative T_j increase (network of fig. B1) for repeated power pulse (heptawatt).



SINGLE POWER PULSE

When the pulse length has an assigned value, effective T_j can be significantly lower than steady state T_j (fig. B3.).

Figure B3 : Effect of a Single Power Pulse.



For any pulse length t_o, a transient thermal resistance R_{th} (t_o) is defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power. Obviously, for shorter pulses, R_{th} (t_o) is lower and a higher power can be dissipated, without exceeding the maximum junction temperature $T_{j\,max}$ allowed to the IC from reliability considerations. Fig. 7 and 9 of this Application Note give experimental values of R_{th} (t_o) for the two cases of the Heptawatt package without and with external heat sink.

REPEATED PULSES

When pulses of the same height Pd are repeated with a defined duty cycle DC and pulse length is short in comparison with the total risetime of the system (many tens of seconds) the train of pulses is seen by the system as a continuous source, at a mean power level of

$$P_{davg} = Pd \times DC$$

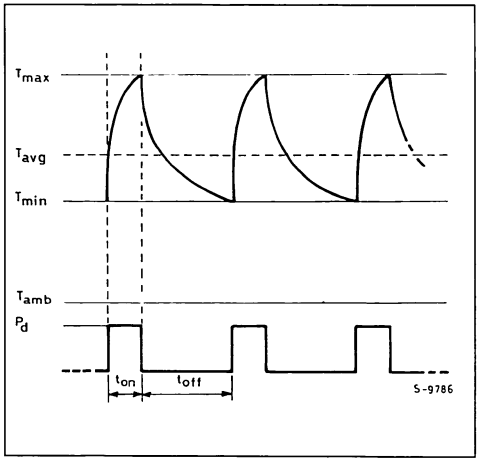
The average temperature increase is :

$$\Delta T_{avg} = R_{th} \times Pd_{avg} = R_{th} \times Pd \times DC$$

On the other hand, the silicon die ($\tau_{SI} = 1 \div 2ms$) is able to follow frequencies of some kHz and junction temperature oscillates about the average, as qualitatively shown in fig. B4.

The thermal resistance corresponding to the peak of the oscillation at equilibrium (peak thermal resistance $R_{th\,peak}$) is now given by fig. 5, and can be obtained if pulse length and duty cycle are known ; Pd_{max} is derived from the same figure.

Figure B4 : Junction Temperature increase for operated Pulses.



APPLICATION EXAMPLES

EXAMPLE 1 - MAXIMUM Pd FOR SINGLE PULSE OF ASSIGNED LENGTH

PROBLEM : define the maximum Pd for a single pulse with a length of 20ms in the case of Heptawatt package used without heat sink. Ambient temperature is 50°C ; maximum temperature is 130°C. Die size is 15k mils^2, with dissipating area of 2k mils^2 (as in P432 test pattern).

SOLUTION : allowed temperature increase ΔT is 80°C. Having a $R_{th(j\text{-}a)}$ of 60°C/W, Heptawatt package can dissipate about 1.3W in steady state From fig. 8 the transient thermal resistance corresponding to one single pulse of 20ms in R_{th} $(20ms)_{P432}$ = 2.2°C/W. A peak of 80/2.2 = 36.3W can be applied to the circuit.

EXAMPLE 2 - CORRECTION FOR DIE SIZE AND DISSIPATING AREA

PROBLEM : correct the results obtained in example 1, for assigned die size and dissipating area.

Pratical case : IC having a die size of 15k mils^2 with a dissipating area of 10k mils^2.

SOLUTION : from fig. 5, thermal resistance of P432 and of the IC under consideration are $R_{th\ P432}$ = 2.3°C/W and $R_{th(j\text{-}c)IC}$ = 1.5°C/W.

As the length of the pulse is 10-15 times longer than the risetime of the silicon, the die (first cell of fig. B1)

can be assumed to have reached its equilibrium condition.

R_{th} (20ms) found in previous example has to be corrected in order to take into account the new value of $R_{th(j-c)}$.

$$R_{th}\ (20ms)_{IC} = R_{th}\ (20ms)_{P432} - R_{th(j-c)P432} + R_{th(j-c)IC} =$$
$$= 2.2 - 2.3 + 1.5°C/W = 1.4°C/W$$

A single pulse of 80/1.4 ≡ 57W can be delivered to such a device.

EXAMPLE 3 - CORRECTION FOR SINGLE PULSES OF 1–3ms

PROBLEM : Correct the results of example 2, for pulse length of 1ms.

SOLUTION : when the pulse has the same order of magnitude of silicon rise time (τ_{P432} is about 1ms) another type of correction is needed. In first approximation it is considered that remains constant when the dissipating area gets higher and the Rth for the silicon die decreases as the reciprocal of the dissipating area. From relationship (1) :

$\Delta T = R_{th}\ (1ms)_{P432} \times 2K/10K \times Pd \times [1 - e^{-t/\tau}]$ for t_o = 1ms :

$$R_{thIC}\ (1ms) = 1.05/0.5°C/W \equiv 0.21°C/W$$

A single pulse of 80/0.21 ≡ 380W can be delivered to such a device.

EXAMPLE 4 - Rth REPEATED PULSES

PROBLEM : find the peak power which can be dissipated by Heptawatt package without heatsink, when power is continuously switched on 10ms and switched off 90ms. Ambient temperature is 50°C. maximum temperature is allowed to be 125°C.

SOLUTION : a maximum ΔT = 75°C has to be considered. Fig. 9 indicated that for a pulse width of 10ms and a duty cycle of 0.1, Rth_{peak} is 8.5°C/W. Maximum Pd is 75/8.5 = 8.8W, with an average temperature increase ΔT_{peak} of 60 x 0.1 x 8.8 ≡ 68°C.

REFERENCES

"Improved thermal evaluation, by means of a simple integrated structure" T. Hopkins, C. Cognetti, R. Tiziani - SEMI THERM (USA, 1986).

HANDLING AND MOUNTING ICs IN PLASTIC POWER PACKAGES

Integrated circuits mounted in plastic power packages can be damaged, or reliability compromised, by inappropriate handling and mounting techniques. Avoiding these problems is simple if you follow the suggestions in this section.

Advances in power package design have made it possible to replace metal packages with more economical plastic packages in many high power applications. Most of SGS-THOMSON Microelectronics power driver circuits, for example, are mounted in the innovative MULTIWATT® package, developed originally for high power audio amplifiers. Though the intrinsic reliability of these packages is now excellent the use of inappropriate techniques or unsuitable tools during mechanical handling can affect the long term reliability of the device, or even damage it. With a few simple precautions, careful designers and production engineers can eliminate these risks, saving both time and money.

BENDING AND CUTTING LEADS

The first danger area is bending and cutting the leads. In these processes it is important to avoid straining the package and particularly the area where the leads enter the encapsulating resin. If the package/lead interface is strained the resistance to humidity and thermal stress are compromised, affecting reliability.

There are five basic rules to bear in mind :

- Clamp the leads firmly between the package and the bend/cut point (figure 1).
- Bend the leads at least 3mm from the package (figure 2a).
- Never bend the leads more than 90° and never bend more than once (figure 2b).
- Never bend the leads laterally (figure 2c).
- Make sure that he bending/cutting tool does not damage the leads.

Figure 1 : Clamp the Leads between the Package and Bend/cut Point.

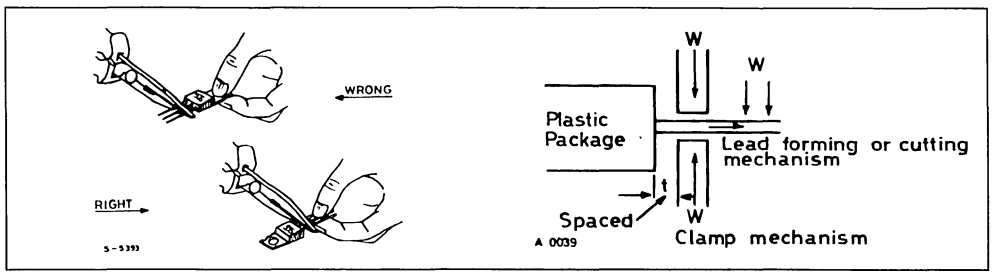
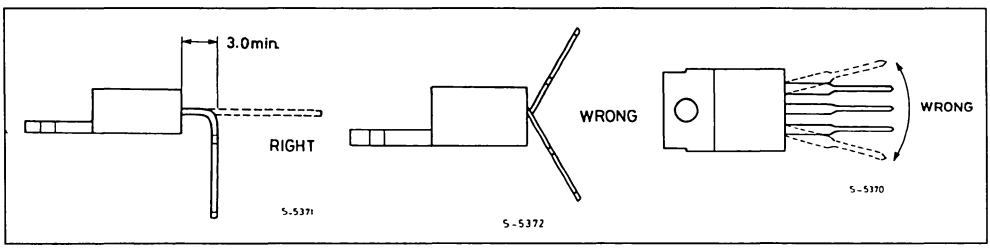


Figure 2 : Bend the Leads at Least 3mm. from the Package, never Bend Leads more than 90° and never Attempt to Splay the Leads Out.



INSERTION

When mounting the IC on a printed circuit board the golden rule is, again, to avoid stress. In particular :

- Adhere to the specified pin spacing of the device ; don't try to bend the leads to fit non-standard hole spacing.
- Leave a suitable space between the IC and the board. If necessary use a spacer.
- Take care to avoid straining the device after soldering. If a heatsink is used and it is mounted on the PC board it should be attached to the IC before soldering.

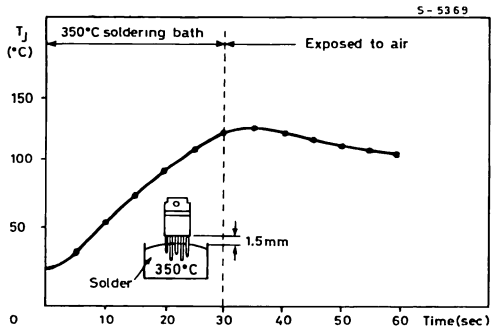
SOLDERING

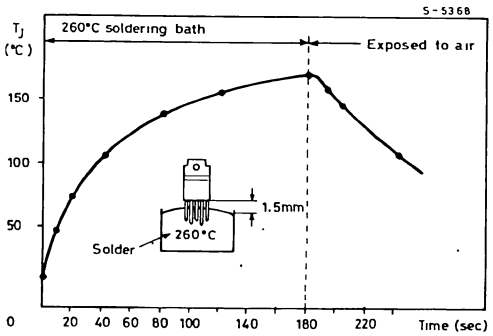
The greater danger during soldering is overheating. If an IC is exposed to high temperature for an excessive period it may be damaged or reliability reduced.

Recommended soldering conditions are 260°C for ten seconds or 350°C for three seconds. Figure 3 shows the excess junction temperature of a PENTAWATT package for both methods.

It is also important to use suitable fluxes for the soldering baths to avoid deterioration of the leads or package resin. Residual flux between the leads or in contact with the resin must be removed to guarantee long term reliability. The solvent used to remove excess flux should be chosen with care. In particular, trichloroethylene (CHCl : CCl_2) - base solvents should be avoided because the residue can corrode the encapsulant resin.

Figure 3 : The Excess Junction Temperature of a PENTAWATT Package in the suggested Soldering Conditions.





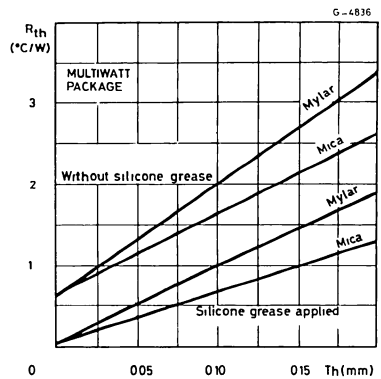
HEATSINK MOUNTING

To exploit the full capability of a power device a suitable heatsink must be used. The most important aspect from the point of view of reliability is that the heatsink is dimensioned to keep the junction temperature as low as possible. From a mechanical point of view, however, the heatsink must be designed so that it does not damage the IC. Care should also be taken in attaching the IC to the heatsink.

The contact thermal resistance between the device and the heatsink can be improved by adding a thin layer of silicon grease with sufficient fluidity to ensure uniform distribution. Figure 4 shows how the thermal resistance of a MULTIWATT package is improved by silicone grease.

An excessively thick layer or an excessively viscous silicon grease may have the opposite effect and could cause deformation of the tab.

Figure 4 : The Thermal Resistance of a MULTIWATT Package is improved by Silicon Grease. Here Thermal Resistance is plotted against Grease Thickness.



SGS-THOMSON plastic power packages - MULTIWATT, PENTAWATT and VERSAWATT - are attached to the heatsink with a single screw. A spring clip may also be used as shown in figure 5. The screw should be properly tightened to ensure that the package makes good contact with the heatsink. It should not be too tight or the tab may be deformed, breaking the die or separating the resin from the tab.

The appropriate tightening torque can be found by plotting thermal resistance against torque as shown in figure 6.

Suggested tightening torques for 3MA screws are 8Kg/cm for VERSAWATT, PENTAWATT and MULTIWATT packages. If different screws, or sping clips, are used the froce exerted by the tab must be equivalent to the force produced with these recommended torques.

Even if the screw is not overtightened the tab can be deformed, with disastrous results. If the surface of the heatsink is not sufficiently flat. The planarity of the contact surface between device and heatsink must be better than 50µm for PENTAWATT and VERSAWATT packages and less than 40µm for MULTIWATT packages.

Figure 5 : MULTIWATT, PENTAWATT and VERSAWATT Packages are attached to the Heatsink with a Single Screw or a Spring Clip.

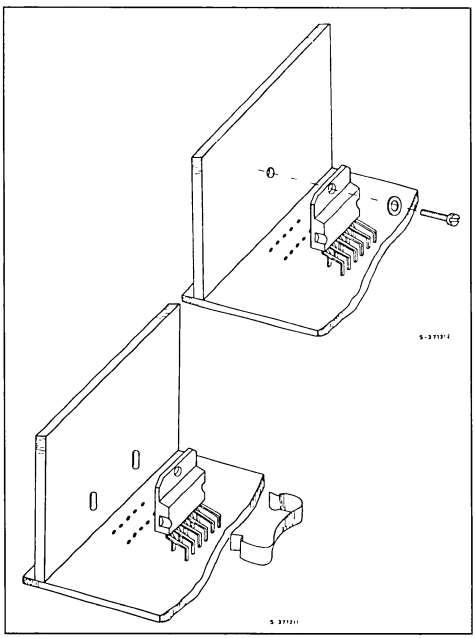


Figure 6 : Contact Thermal Resistance depends on Tightening Torque.

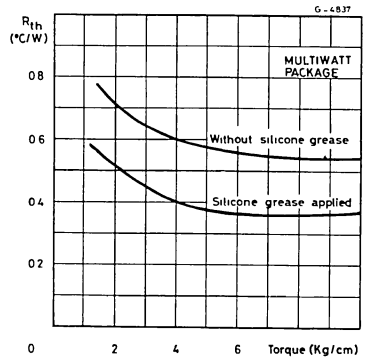
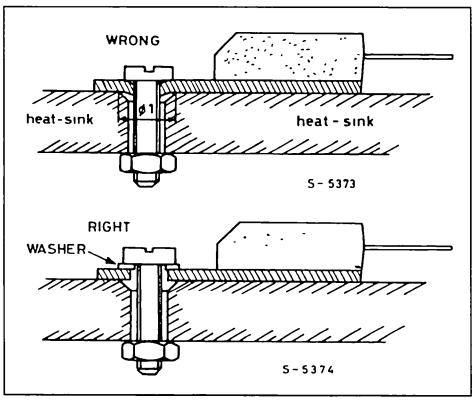


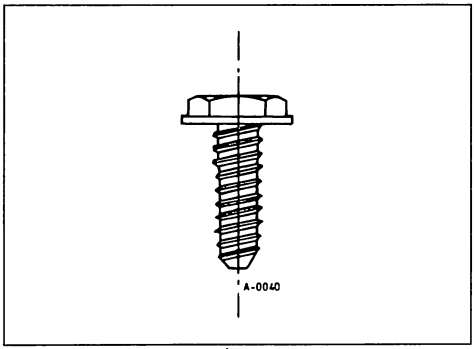
Figure 7 : The Heatsink Tab may be deformed it a Washer or a Wide-headed Screw is not used.



Similar problems may arise if the screwhead is too narrow compared to the hole in the heatsink (figure 7).

The solution here is to use a washer to distribute the pressure over a wider area. An alternative is to use screws of the type shown in figure 8 which have a wide flat head. When self-tapping screws are used it is also important to provide an outlet for the material deformed as the thread is formed. Poor contact will result if this is not done. Another possible hazard arises when the hole in the heatsink is formed with a punch : a circular depression may be formed around the hole, leading to deformation of the tab. This may be cured by using a washer or by modifying the punch.

Figure 8 : The recommended Screw Type Looks Like this.



Serious reliability problems can be encountered if the heatsink and printed circuit board are not rigidly connected. Either the heatsink must be rigidly attached to the printed circuit board or both must be securely attached to the chassis. If this is not done the stresses and strains induced by vibration will be applied to the device and in particular to the lead/resin interface. This problem is more likely to arise when large boards and large heatsinks are used or whenever the equipment is subjected to heavy vibrations.

DESIGNING WITH THERMAL IMPEDANCE

BY T.HOPKINS, C.COGNETTI, R.TIZIANI

REPRINT FROM "SEMITHERM PROCEDINGS" S.DIEGO (U.S.A.) 1988.

ABSTRACT

Power switching techniques used in many modern control systems are characterized by single or repetitive power pulses, which can reach several hundred watts each. In these applications where the pulse width is often limited to a few milleseconds, cost effective thermal design considers the effect of thermal capacitance. When this thermal capacitance is large enought, it can limit the junction temperature to within the ratings of the device even in the presence of high dissipation peaks. This paper discusses thermal impedance and the main parameters influencing it. Empirical measurements of the thermal impedance of some standard plastic packages showing the effective thermal impedance under pulsed conditions are also presented.

INTRODUCTION

Power switching applications are becoming very common in many industrial, computer and automotive ICs. In these applications, such as switching power supplies and PWM inductive load drivers, power dissipation is limited to short times, with single or repeated pulses. The normal description of the thermal performance of an IC package, Rth(j -a) (junction to ambient thermal resistance), is of little help in these pulsed applications and leads to a redundant and expensive thermal design.

This paper will discuss the thermal impedance and the main factors influencing it in plastic semiconductor packages. Experimental evaluations of the thermal performance of small signal, medium power, and high power packages wil be presented as case examples. The effects of the thermal capacitance of the packages when dealing with low duty cycle power dissipation will be presented and evaluated in each of the example cases.

THERMAL IMPEDANCE MODEL FOR PLASTIC PACKAGES

The complete thermal impedance of a device can be modeled by combining two elements, the thermal resistance and the thermal capacitance.

The thermal resistance, Rth, quantifies the capability of a given thermal path to transfer heat. The general definition of resistance of the thermal path, which includes the three different modes of heat dissipation (conduction, convection and radiation), is the ratio between the temperature increase above the reference and the heat flow, DP, and is given by the equation :

$$R_{th} = \frac{\Delta T}{\Delta P} = \frac{\Delta T}{\frac{\Delta Q}{\Delta t}}$$

Where : ΔQ = heat
Δt = time

Thermal capacitance, C_{th}, is a measure of the capability of accumulating heat, like a capacitor accumulates a charge. For a given structural element, C_{th} depends on the specific heat, c, volume V, and density d, according to the relationship :

$$C_{th} = c\ d\ V$$

The resulting temperature increase when the element has accumulated the heat Q, is given by the equation :

$$\Delta T = \Delta Q / C_{th}$$

The electrical analogy of the thermal behaviour or a given application consisting of an active device, package, printed circuit board, external heat sink and external ambient is a chain of RC cells, each having a characteristic time constant :

$$\tau = RC$$

To show how each cell contributes to the thermal impedance of the finished device consider the simplified example shown in figure 1. The example device consists of a dissipating element (integrated circuit) soldered on a copper frame surrounded by a plastic compound with no external heat sink. Its equivalent electrical circuit is shown in figure 2.

The first cell, shown in figure 2, represents the thermal characteristics of the silicon itself and is characterized by the small volume with a correspondingly low thermal capacitance, in the order of a few mJ/C. The thermal resistance between the junction and

the silicon/slug interface is of about 0.2 to 2 °C/W, depending on die size and on the size of the dissipating elements existing on the silicon. The time constant of this cell is typically in the order of a few milliseconds.

The second cell represents the good conductive path from the silicon/frame interface to the frame periphery. In power packages, where the die is often soldered directly to the external tab of the package, the thermal capacitance can be large. The time constant for this cell is in the order of seconds.

From this point, heat is transferred by conduction to the molded block of the package, with a large thermal resistance and capacitance. The time constant of the third cell is in the order of hundreds of seconds.

After the plastic has heated, convection and radiation to the ambient starts. Since a negligible capacitance is associated with this phase, it is represented by a purely resistive element.

When power is switched on, the junction temperature increase is ruled by the heat accumulation in the cells, each following its own time constant according with the equation :

$\Delta T = R_{th}\, P_d\, [1 - e^{(t/\tau)}]$

The steady state junction temperature, T_j, is a function of the $R_{th\ (j\ a)}$ of the system, but the temperature increase is dominated by thermal impedance in the transient phase, as is the case in switching applications.

A simplified example of how the time constants of each cell contribute to the temperature rise is shown in figure 3 where the contribution of the cells of figure 2 is exaggerated for a better understanding.

When working with actual packages, it is observed that the last two sections of the equivalent circuit are not as simple as in this model and possible changes will be discussed later. However, with switching times shorter than few seconds, the model is sufficient for most situations.

Figure 1 : Simplified Package Outline.

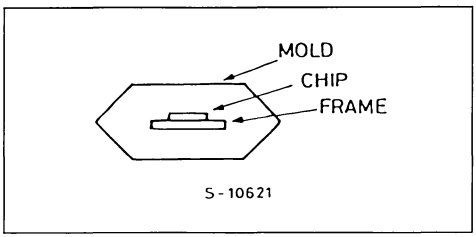


Figure 2 : Equivalent Thermal Circuit of Simplified.

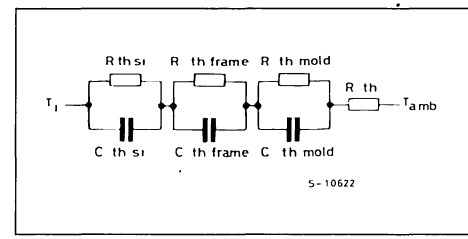
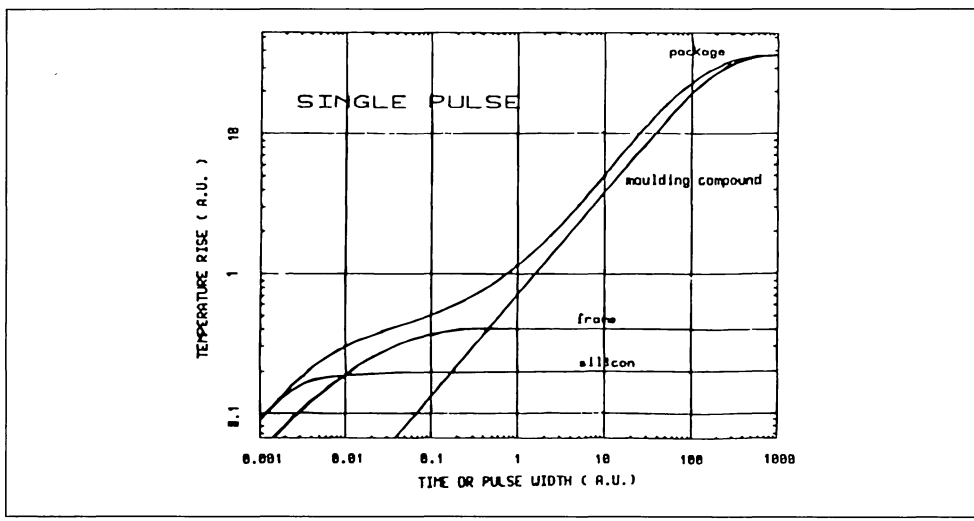


Figure 3 : Time Constant Contribution of Each Thermal Cell (qualitative example).



EXPERIMENTAL MEASUREMENTS

When thermal measurements on plastic packages are performed, the first consideration is the lack of a standard method. At present, only draft specifications exist, proposed last year and not yet standardized (1).

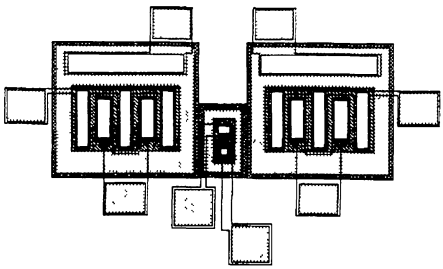
The experimental method used internally for evaluations since 1984 has anticipated these preliminary recomendations to some extent, as it is based on test patterns having, as dissipating element, two power transistors and, as measurement element, a sensing diode placed in the thermal plateau arising when the transistors are biased in parallel.

The method used has been presented elsewhere (2) for the pattern P432 (shown in figure 4), which uses two small (1000 sq mils) bipolar power transistors and has a maximum DC power capability of 40 W (limited by second breakdown of the dissipating elements).

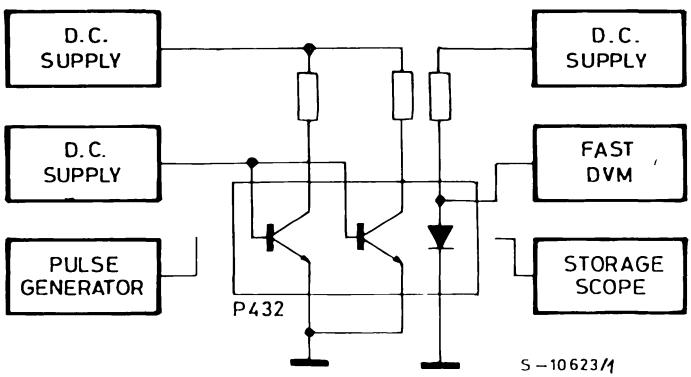
A similar methodology was followed with the new H029 pattern, based on two D-Mos transistors (3) having a total size of 17.000 sq mils and a DC power capability of 300 W on an infinite heat sink at room temperature (limited by thermal resistance and by max operating temperature of the plastics).

Figure 4.

a) P432 Test Die



b) P432 Measurement System

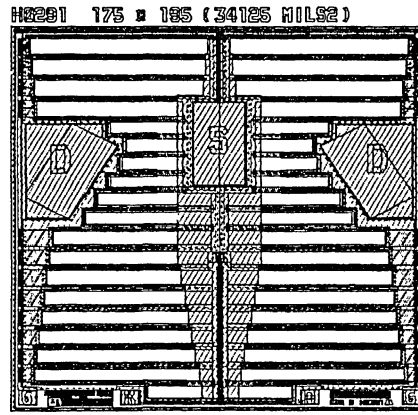


Using the thermal evaluation die, four sets of measurements were performed on an assortment of insertion and surface mount packages produced by SGS-Thomson Microelectronics. The complete characterization is available elsewhere (4). The four measurements taken were :

1) Junction to Case Thermal Resistance (Power Packages)
2) Junction to Ambient Thermal Resistance
3) Transient Thermal Impedance (Single Pulse)
4) Peak Transient Thermal Impedance (Repeated Pulses)

Figure 5.

a) H029 Test Die



b) H029 Measurement System

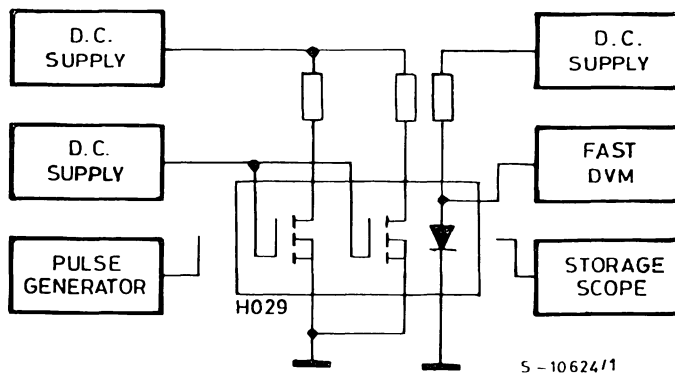
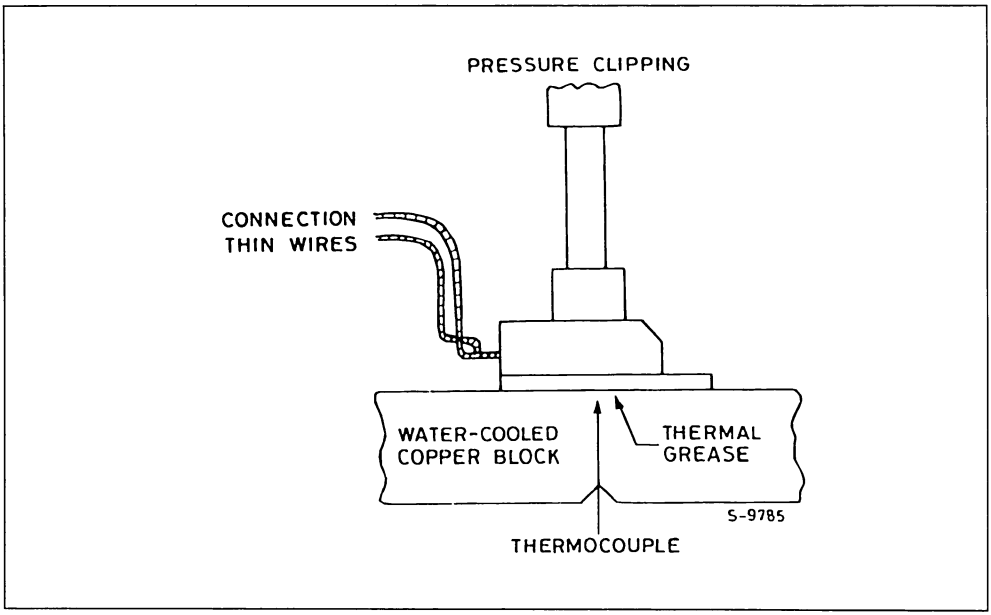


Figure 6 : Set-up for $R_{th\ (j-c)}$ Measurement.

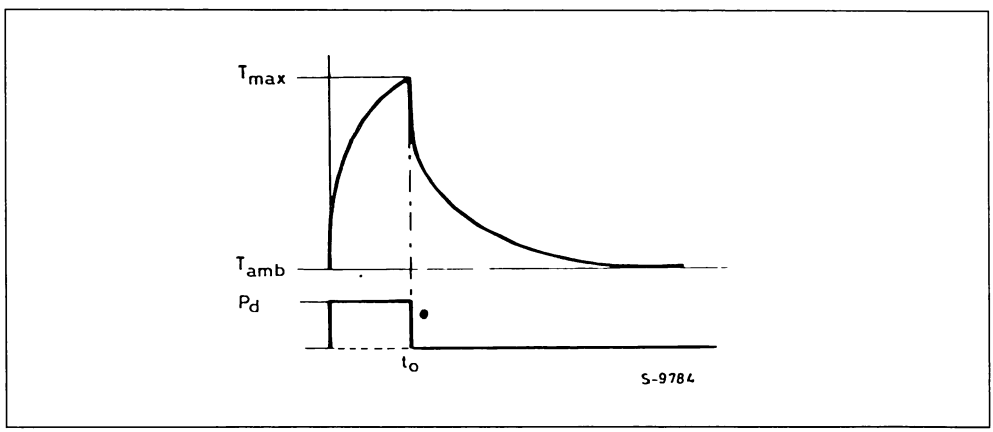


The junction to case thermal resistance measurements were taken using the well known setup shown in figure 6 where the power device is clamped against a large mass of controlled temperature.

The junction to ambient thermal resistance in still air, was measured with the package soldered on standard test boards, described later, and suspensed in 1 cubic foot box, to prevent air movement.

The single pulse transient thermal impedance was measured in still air by applying a single power pulse of duration t_o to the device. The exponential temperature rise in response to the power pulse is shown qualitetively in figure 7. In the presence of one single power pulse the temperature, ΔT_{max}, reached at time t_o, is lower than the steady state temperature calculated from the junction to ambient thermal resistance. The transient thermal impedance R_o, is obtained from the ratio $\Delta T_{max}/Pd$.

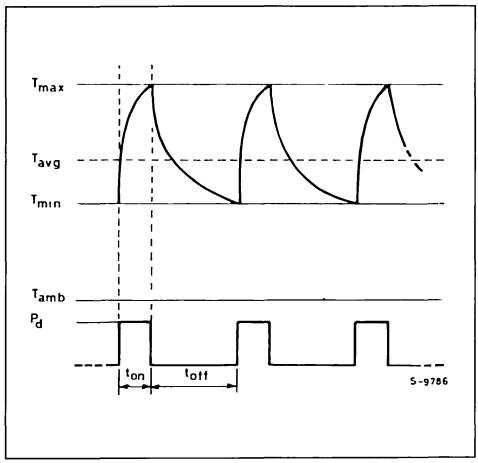
Figure 7 : Transient Thermal Response for a Single Pulse.



The peak transient thermal impedance for a series of repetitive pulses was measured by applying a string of power pulses to the device in free air. When power pulses of the same height, P_d, are repeated with a given duty cycle, DC, and the pulse length, t_p, is shorter than the total time constant of the system, the train of pulses is seen as a contiuous source with mean power level given by the equation :

$$P_{davg} = P_d \, DC$$

Figure 8 : Transient Thermal Response for Repetitive Pulses.



On the other hand, the silicon die has a thermal time constant of 1 to 2 ms and the die temperature is able to follow frequencies of some kHz. The result is that T_j oscillates about the average value :

$$\Delta T_{javg} = R_{th} \, P_{davg}$$

The resulting die temperature excursions are shown qualitatively in figure 8. The peak thermal impedance, R_{thp}, corresponding to the peak temperature, DT_{max}, at the equilibrium can be defined :

$$R_{thp} = \Delta T_{max}/P_d = F\,(t_p, DC)$$

The value of R_{thp} is a function of pulse width and duty cycle. Knowledge of R_{thp} is very important to avoid a peak temperature higher than specified values (usually 150°C).

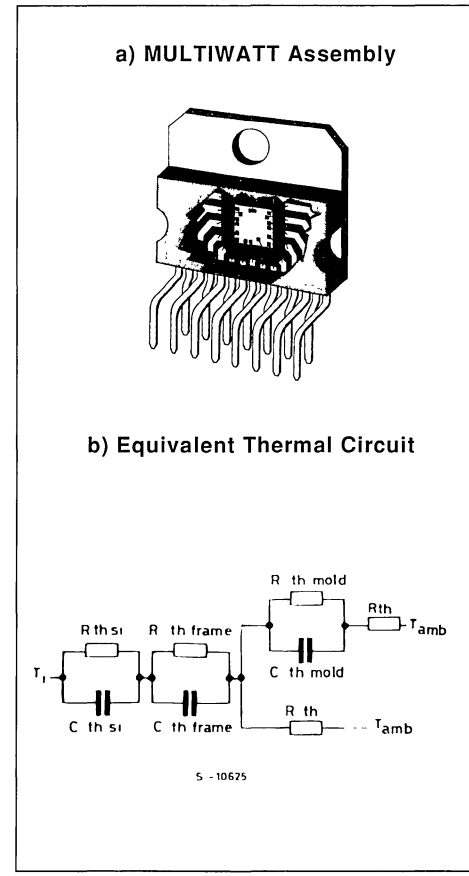
EXPERIMENTAL RESULTS

The experimental measurements taken on several of the packages tested are summarized in the following sections.

MULTIWATT PACKAGE

The MULTIWATT (R) package, shown in figure 9a, is a multileaded power package in which the die is attached directly to the tab of package using a soft solder (Pb/Sn) die attach. The tab of the package is a 1.5 mm thick copper alloy slug. The thermal model of the MULTIWATT, shown in figure 9b, is not much different from that shown in figure 2. The main difference being that when heat reaches the edge of the slug, two parallel paths are possible ; conduction towards the molding compound, and convection and radiation towards the ambient. After a given time, convection and radiation taked place from the plastic.

Figure 9.



Using the two test die, the measured junction to case thermal resistance is :

P432 $R_{th\,(j\,c)} = 2°C/W$

H029 $R_{th\,(j\,c)} = 0.4°C/W$

The measured time constant is approximately 1 ms for each of the two test patterns, but the two devices have a different steady state temperature rise.

The second cell shown in figure 9 is dominated by the large thermal mass of the slug. The thermal resistance of the slug, R_{thslug} is about 1 °C/W and the thermal time constant of the slug is in the order of 1 second.

The third RC cell in the model has a long time constant due to the mass of the plastic molding and its low thermal conductivity. For this cell the steady state is reached after hundreds of seconds.

For the MULTIWATT the DC thermal resistance of the package in free air, $R_{th\,j\,a}$, is 36 °C/W with the P432 die and 34.5°C/W with the H029 die.

Figure 10 shows the single pulse transient thermal impedance for the MULTIWATT with both the P432 and H029 test die. As can be seen on the graph, the package is capable of high dissipation for short periods of time. For a die like the H029 the power device is capable of 700 to 800 W for pulse widths in the range of 1 to 10 ms. For times up to a few seconds the effective thermal resistance for a single pulse is still in the range of 1 to 3 °C/W.

The peak transient thermal impedance for the MULTIWATT package containing the P432 die in free air is shown in figure 11.

POWER DIP PACKAGE

The power DIP package is a derivative of standard small signal DIP packages with a number of leads connected to the die pad for heat transfer to external heat sinks. With this technique low cost heat sinks can be integrated on the printed circuit board as shown in figure 12a. The thermal model of the power DIP, shown in figure 12b accounts for the external heat sink on the circuit board by adding a second RC cell in parallel with the cell corresponding to the molding compound.

In this model, the second cell has a shorter time constant than for the MULTIWATT package, due in large part to the smaller quantity of copper in the frame (the frame thickness is 0.4 mm compared to 1.5 mm). Thus the capacitance is reduced and the resistance increased.

The increased thermal impedance due to the frame can partially be compensated by a better thermal exchange to the ambient by adding copper to the heat sink on the board. The DC thermal resistance between the junction and ambient can be reduced to the same range as the MULTIWATT package in free air, as shown in figure 13.

Figure 10 : Transient Thermal Response MULTIWATT Package.

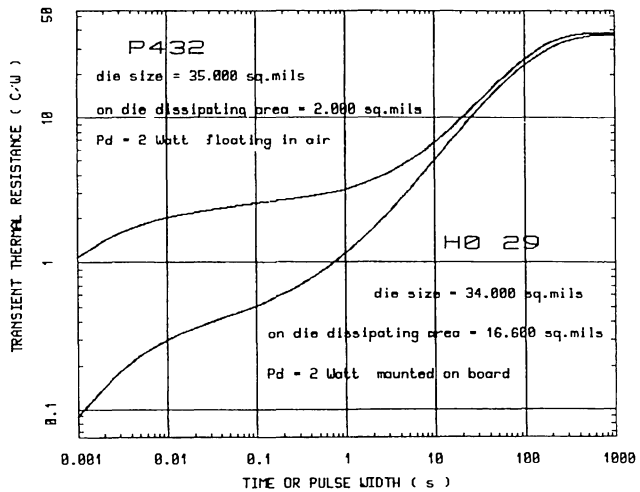


Figure 11 : Peak Thermal Resistance MULTIWATT Package.

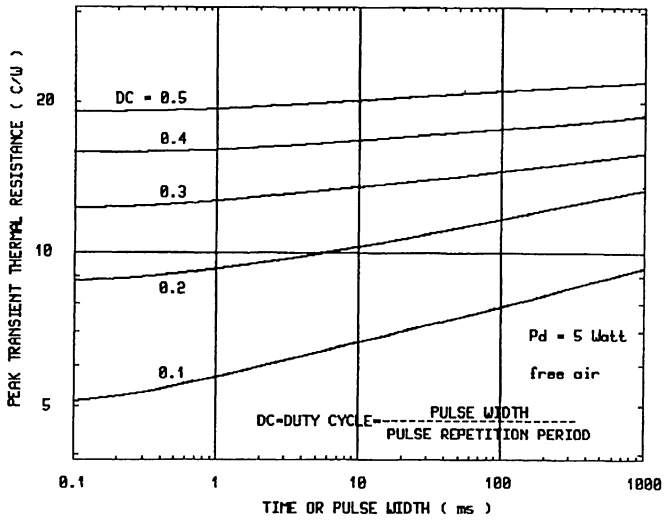
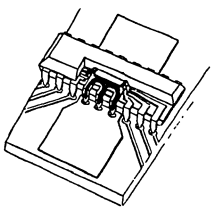
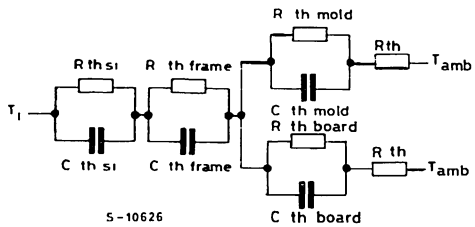


Figure 12.

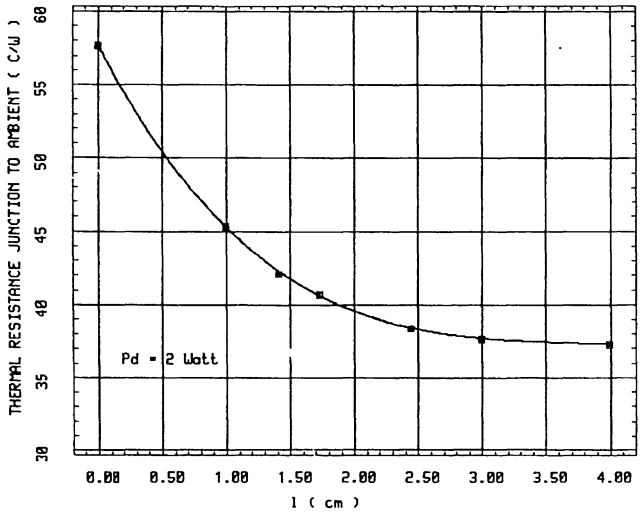


a) Power DIP Package



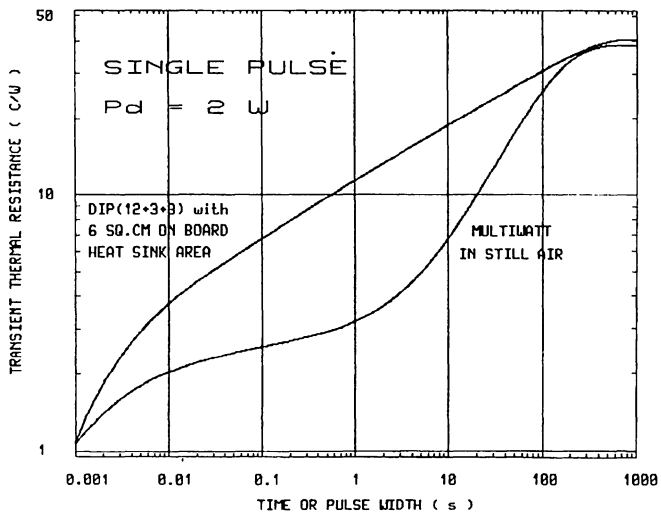
b) Equivalent Thermal Circuit

Figure 13 : Rth (j – a) vs. PCB Heat Sink Size 12 + 3 + 3 Power Dip.



As a comparison, figure 14 compares the thermal performance of the power DIP and the MULTIWATT package. It is clearly seen that even though the DC thermal resistance may be similar, the MULTIWATT is superior in its performance for pulsed applications.

Figure 14 : Transient Thermal Impedance for Single Pulses in Power DIP and MULTIWATT Packages.



STANDARD SIGNAL PACKAGES

In standard, small signal, packages the easiest thermal path is from the die to the ambient through the molding compound. However, if a high conductivity frame, like a copper lead frame, is used another path exists in parallel. Figure 15 shows the equivalent thermal model of such a package. The effectiveness of a copper frame in transferring heat to the board can be seen in the experimental results in DC conditions.

Table 1 shows the thermal resistance of some standard signal packages in two different conditions ; with the device floating in still air connected to the measurement circuit by thin wires and the same device soldered on a test board.

Table 1 : Thermal Resistance of Signal Packages

Package	Frame Thickness & Material	Rth (j-a) Floating	°C/W on Board
DIP 8	(0.4 mm Copper)	125-165	78-90
DIP 14	(0.4 mm Copper)	98-128	64-73
DIP 16	(0.4 mm Copper)	95-124	62-71
DIP 20	(0.4 mm Copper)	85-112	58-69
DIP 14	(0.25 mm Copper)	115-147	84-95
DIP 20	(0.25 mm Copper)	100-134	76-87
DIP 24	(0.25 mm Copper)	67-84	61-68
DIP 20	(0.25 mm Alloy 42)	158-184	133-145
SO 14	(0.25 mm Copper)	218-250	105-180
PLCC 44	(0.25 mm Copper)	66-83	48-72

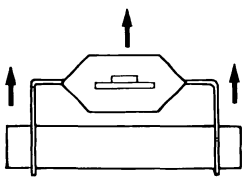
The transient thermal resistance for single pulses for the various packages are shown in figures 16 through 20.

The results of the tests, as shown in the preceding figures, show the true capabilities of the packages. For example, the DIP 20 with a Alloy 42 frame is a typical package used for signal processing applications and can dissipate only 0.5 to 0.7 W in steady state conditions. However, the transient thermal impedance for short pulses is low (11 C/W for t_p = 100 ms) and almost 7 Watts can be dissipated for 100 ms while keeping the junction temperature rise below 80°C.

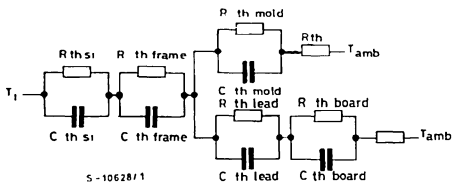
The packages using a 0.4 mm Copper frame have a low steady state thermal resistance, especially in the case of the DIP 20. The thicker lead frame increases the thermal capacitance of the die flag, which greatly improves the transient thermal impedance. In the case of the DIP 20, which has the largest die pad, the transient R_{th} for 100 ms pulses is about 4.3°C/W. This allows the device to dissipate an 18 Watt power pulse while keeping the temperature rise below 80°C.

As with the previous examples the peak transient thermal impedance for repetitive pulses depends on the pulse length and duty cycle as shown in figure 14. With the signal package, however, the effect of the duty cycle becomes much less effective for longer pulses, due primarily to the lower thermal capacitance and hence lower time constant of the frame.

Figure 15.



a) DIP Package Mounted on PCB



b) Equivalent Thermal Circuit DIP Package on PCB

Figure 16 : Transient Thermal Impedance DIP 20 (alloy 42).

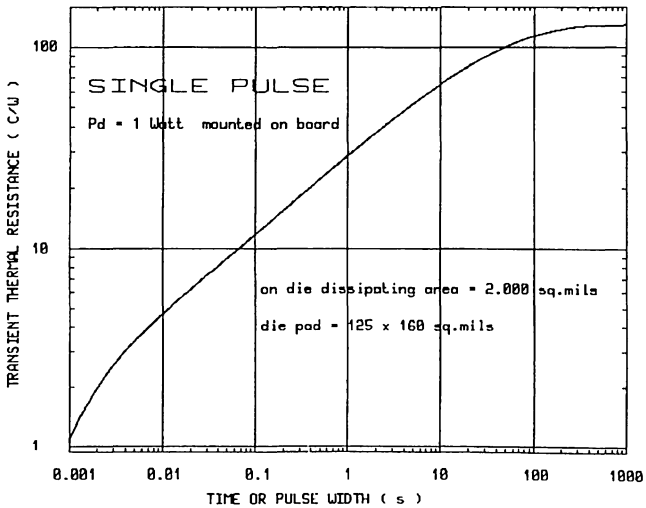


Figure 17 : Transient Thermal Impedance 0.4 mm Copper Frame DIP Packages.

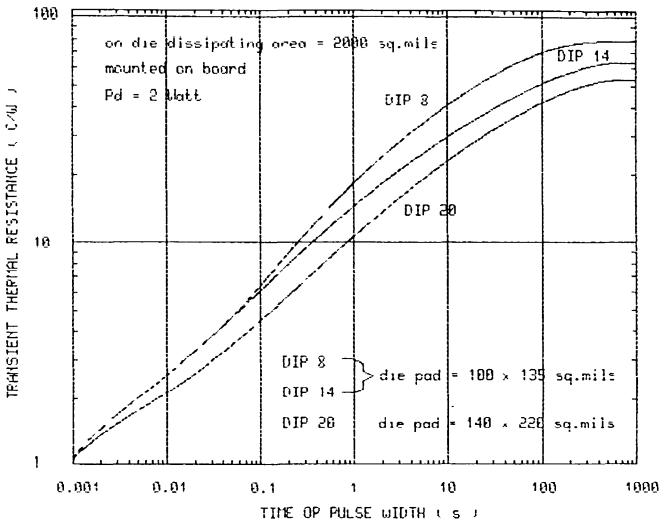


Figure 18 : Transient Thermal Impedance 0.25 mm Copper Frame DIP Packages.

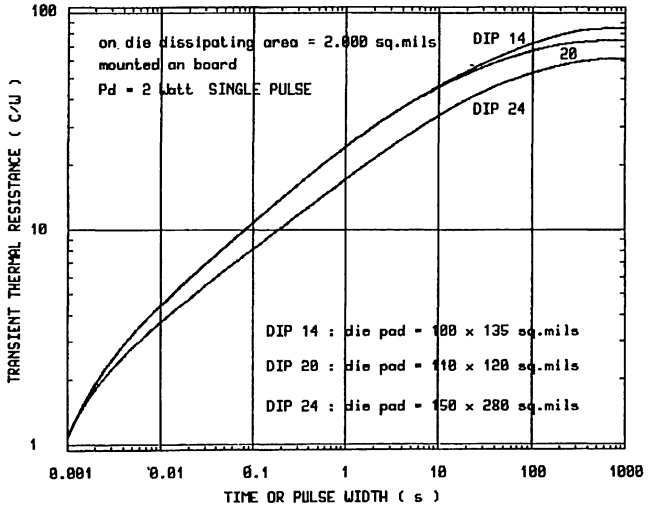


Figure 19 : Transient Thermal Impedance 0.25 mm Frame PLCC Package.

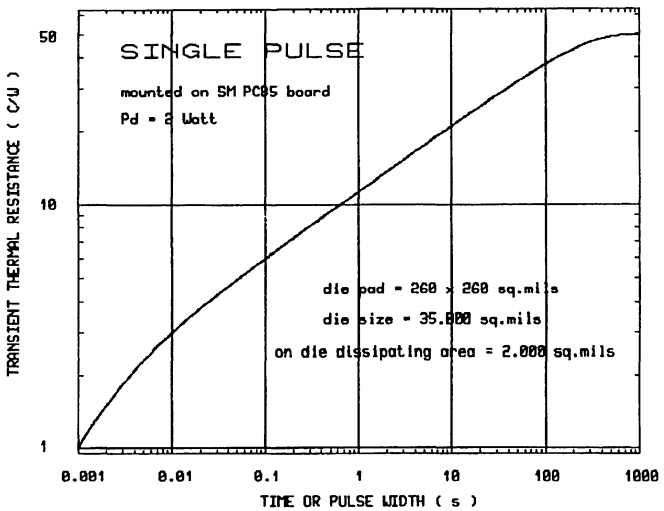


Figure 20 : Transient Thermal Impedance 0.25 mm Copper Frame SO14 Package.

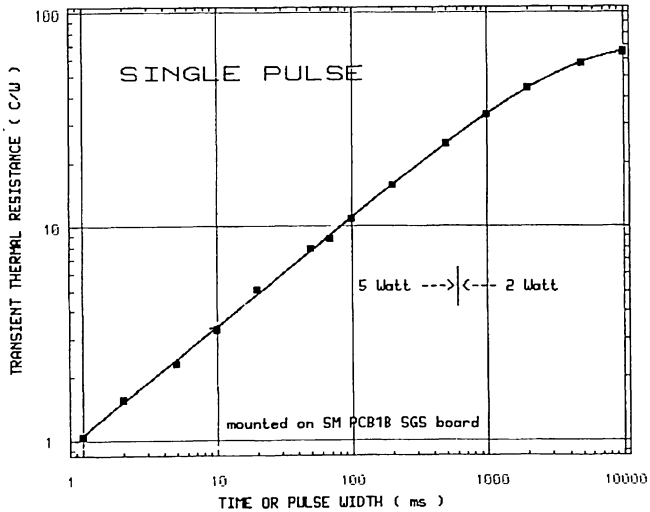
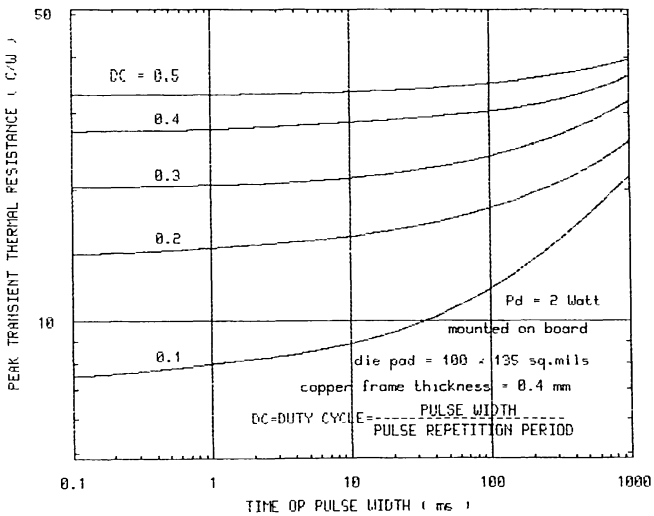


Figure 21 : Peak Thermal Impedance 0.25 mm Copper Frame 14 Lead DIP.



CONCLUSION

This paper has discussed a test procedure for measuring and quantifying the thermal characteristics of semiconductor packages. Using these test methods the thermal impedance of standard integrated circuit packages under pulsed and DC conditions were evaluated. From this evaluation two important considerations arise :

1) The true thermal impedance under repetitive pulsed conditions needs to be considered to maintain the peak junction temperature within the rating for the device. A proper evaluation will result in junction temperatures that do not exceed the specified limits under either steady state or pulsed conditions.

2) The proper evaluation of the transient thermal characteristics of an application should take into account the ability to dissipate high power pulses allowing better thermal design and possibility reducing or eliminating expensive external heat sinks when they are oversized or useless.

REFERENCES

(1) SEMI Draft Specifications 1377 and 1449, 1986

(2) T. Hopkins, R. Tiziani, and C. Cognetti, "Improved thermal impedance measurements by means of a simple integrated structure", presented at SEMITHERM 1986

(3) C. Cini, C. Diazzi, D. Rossi and S. Storti, "High side monolithic switch in Multipower-BCD technology", Proceedings of Microelectronics Conference, Munchen November 1986

(4) Application Notes 106 through 110, SGS-THOMSON Microelectronics, 1987

THERMAL MANAGEMENT IN SURFACE MOUNTING

The evolutionary trends of integrated circuits and printed circuits boards are, in both cases, towards improved performance and reduced size. From these points of view, a factor of major importance has been mutual thermal interaction between ICs, even those with low dissipation.

It follows then that thermal design of medium and high density applications has evolved to include factors such as power effects, die size, package thermal resistance, **integration level of active devices** and substrate type. Added to this a trend towards greater use of switching techniques exists.

Today, in order to design reliable application circuits, it is necessary to have complete data on package thermal response characteristics. In fact, it is a well known and long established fact that device lifetime has an exponential relationship with junction temperature.

PRELIMINARY CONSIDERATIONS

Heat dissipation for DIPs with a low thermal conductivity frame (e.g. Alloy42) is due to convection and **irradiation** from an emiting area corresponding to the silicon die and the package die pad.

Since heat transmission through the lead frame is very poor, dissipation does not depend greatly on substrate type. In fact, samples soldered on printed circuit boards, or inserted in **connectors** have nearly the same dissipation capability as samples suspended in air. The difference, in the range of just 10%, is commonly ignored and specifications for insertion ICs only give one thermal resistance value, which is more than adequate for good thermal design.

The question then arises, is the approximation valid for SO and PLCC packages ?

The answer is no ! Thermal characteristics for these devices are influenced by many factors.

1) Device Related Factors
   - size of the dissipating element
   - dissipation level
   - pulse length and duty cycle

2) Package Related Factors
   - thermal conductivity of the frame
   - frame design

3) Substrate Related Factors
   - thermal conductivity of the substrate
   - layout

Therefore a number of parameters can change the thermal characteristics. These cannot be described by a single thermal resistance, in fact a set of experimental curves gives the best presentation.

JUNCTION TO AMBIENT THERMAL RESISTANCE $R_{th(j-a)}$

$R_{th(j-a)}$ represents the thermal resistance of the system and comprises the silicon die, the package, and any thermal mass in contact with the package to dissipate heat to the ambient.

At a given dissipation level P_d, the increase in junction temperature ΔT_j over ambient temperature T_a is given by :

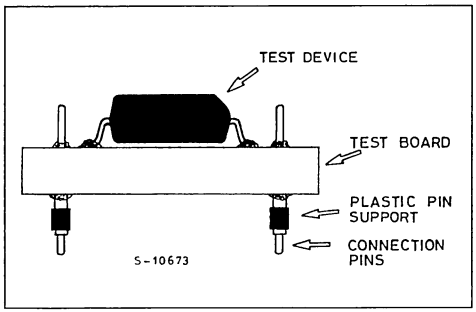
$\Delta T_j = R_{th(j-a)} \times P_d$

$R_{th(j-a)}$ is made up of many elements both within the device and external to it.

If the device is considered alone, $R_{th(j-a)}$ is given by the dissipation path from the silicon die to the leadframe, to the molding compound, to the ambient. **Experimental values are very large in this condition, especially for small packages such as Small Outline types.**

However, this situation is not met in practice and experimental data included in the present work indicates the worst case (floating samples). In most applications, Surface Mount Devices are soldered onto a substrate (commonly epoxy glass (FR4) and are in thermal contact with it through the soldered joints and the copper interconnections. In this case, the heat generated by the active circuit is transferred to the leadframe and then to the substrate. A new dissipation path thus exists in parallel with the previous one whose efficiency depends on the thermal conductivity of the frame and on the length of the printed circuit's copper tracks. Figure A shows the experimental module.

Figure A : Device Soldered to the Best Board, for Junction to Ambient Thermal Resistance Measurement.

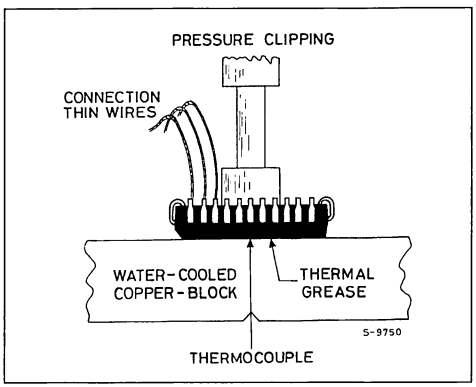


JUNCTION TO CASE THERMAL RESISTANCE $R_{th(j-c)}$

$R_{th(j-c)}$ is the thermal resistance from the junction to a given area of the peackage's external surface where a heatsink is applied.

In signal packages, a suitable area is its upper surface. **Measurements are made with the samples in good thermal contact with an infinite heatsink (fig. B).**

Figure B : Junction to Case Thermal Resistance Measurement.



When a heatsink of thermal resistance R_{hs} is attached to the package, the following relationship is valid :

$$R_{th(j-a)} = R_{th(j-c)} + \frac{R_{hs} \times R^*}{R_{hs} + R^*}$$

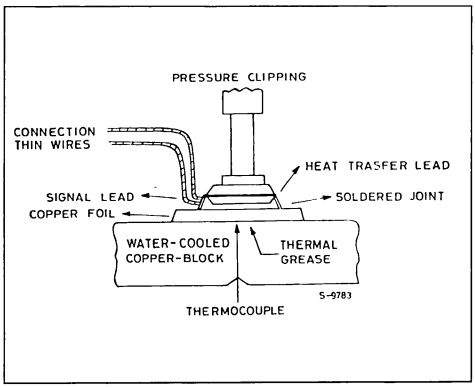
Where R^* takes into account all the other dissipation paths (i.e. junction/frame/substrate). R^* is the lowest with low thermal conductivity frames.

In high power applications $R^* \gg R_{hs}$ and $R_{th(j-a)} = R_{th(j-c)} + R_{hs}$

JUNCTION TO PIN THERMAL RESISTANCE $R_{th(j-p)}$

In medium power packages $R_{th(j-p)}$ is the thermal resistance of the heat transfer leads, from the junction to the external heatsink. In most cases the external heatsink is integrated on the board. Figure C shows the experimental setup.

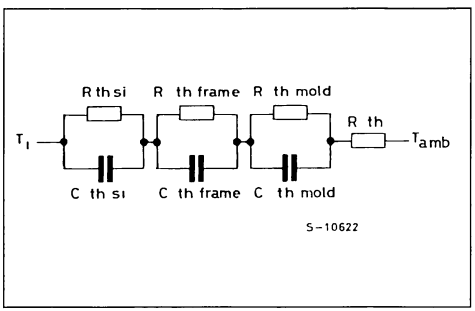
Figure C : Junction to Pin Thermal Resistance Measurement.



TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

The electrical equivalent of heat dissipation for a module formed by an active device, its package, a PCB and the ambient, is a chain of RC cells, as shown in fig. D, each with a characteristic rise time (τ) = RC.

Figure D : Equivalent Thermal Circuit Simplified Package.

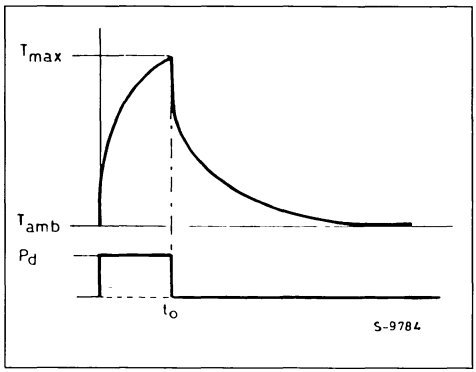


The thermal capacitance of each cell is a measure of its ability to accumulate heat and depends on the specific heat, volume and density of the constituent materials.

When power is switched on, the junction temperature after time it is governed by the heat impedance of the cells, each of which follows its own time constant - this is analogous to the exponential charge of RC cells in an electrical circuit.

For a pulse lenght t_o, the effective T_j can be significantly lower than the steady state T_j (fig. E) and the transient thermal resistance $R_{th(to)}$ can be defined from the ratio between the junction temperature at the end of the pulse and the dissipated power.

Figure E : Temperature Rise for Single Power Pulse.



Obviously, this parameter is smaller for shorter pulses and higher power can be dissipated without exceeding the maximum junction temperature defined from a reliability point of view.

The knowledge of transient thermal data is an important tool for cost effective thermal design of switching applications.

PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES

When pulses of the same height Pd are repeated with a duty cycle, DC, and a pulse width t_o, which is shorter than the overall system time constant, the train of pulses is seen as a continuous source of mean power Pd_{avg}, where :

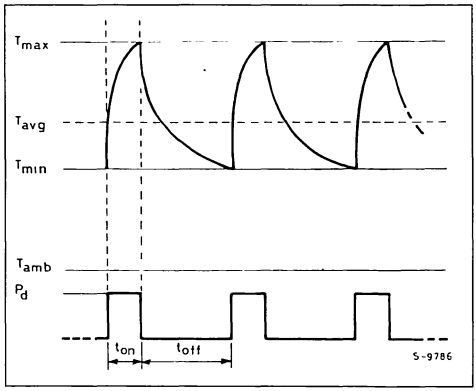
$Pd_{avg} = Pd \times DC$

However the silicon die has a time constant in the order of 1 to 2ms and is able to follow frequencies in the kHz range. Thus junction temperature oscillates about an average value given by :

$T_{javg} = R_{th} \times Pd_{avg}$

as is graphically shown in fig. F.

Figure F : Temperature Rise for Repeated Power Pulses.



The thermal resistance corresponding to the peak of the steady state oscillations (peak thermal resistance indicates the maximum temperature reached by the junction and, depending on duty cycle and pulse width, may be much lower than the DC thermal resistance.

EXPERIMENTAL METHOD

Measurements were performed by means of the especially developed thermal test pattern P432, which is designed according to the Semiconductor Equipment and Materials Institute (SEMI) G32 guideline.

Test chip P432 is based on a dissipating element formed by two npn transistors, each with 10W power capability, and one sensing diode (fig. G). The diode is placed on the temperature plateau generated when the two transistors are biased in parallel, and gives the actual junction temperature T_j of the dissipating element, through the calibration curve (fig. H) of its forward voltage Vf versus temperature at a constant current of 100µA.

Figure G : Thermal Test Pattern P432.

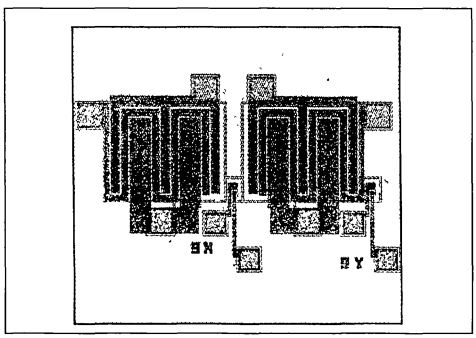
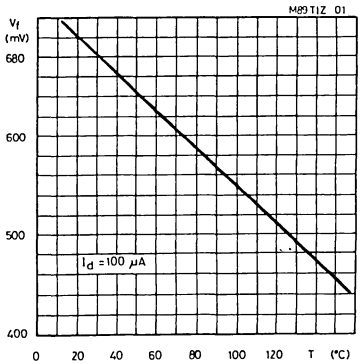


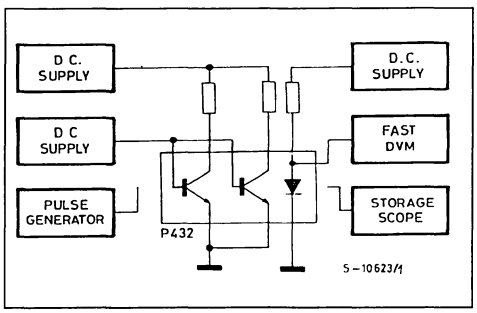
Figure H : Calibration Curve of P432 Temperature Sensing Diode.



Transistor size is intentionally limited to 1000sq. mils, in order to simulate high power density, characterizing a worst case. Die size, which is found to have little influence on thermal resistance when a copper frame is used, is slightly smaller than the die pad size and never exceeds 30k sq mils even in the largest packages such as high pin count PLCCs.

The measurement setup is shown in fig. I. it is compatible with DC and AC supplies and has an accuracy of better than 5%.

Figure I : Experimental Setup.



The advantages offered by the test pattern are :

- high power capability
- repeatable V_f and temperature coefficient (1.9mv/C) of the sensing element
- high resolution in pulsed conditions (100µs)
- better correlation from one package to another.

Both Alloy 42 and copper frames were considered for narrow SO packages (150mils body). For wide SO (300mils body) and PLCC packages only copper frames were examined. Suitable test boards were developed (figs J, K and L).

Figure J : Test Board Lay-out for SO Packages (150 mils body width)
Board size is : 23 x 42mm^2.

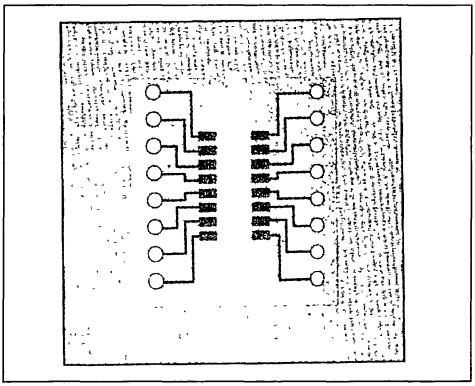


Figure K : Test Board Lay-out for SO Packages (3000 mils body width)
Board size is 38 x 43mm^2.

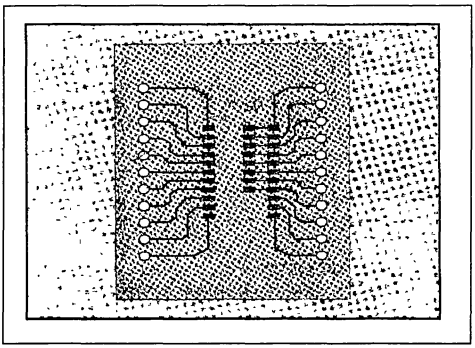
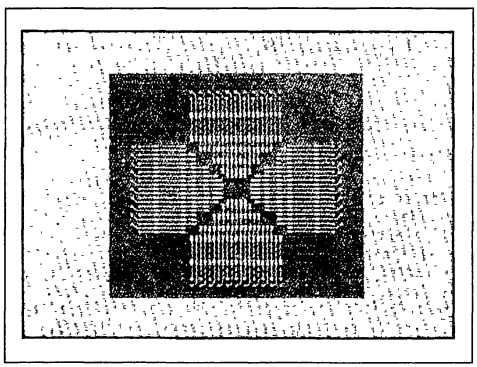


Figure K : Test Board for PLCCs
Board size is 58 x 58mm^2.



MEDIUM POWER PACKAGES

While surface mount signal ICs are readily available, almost all power ICs are still assembled in traditional insertion packages.

Medium power SM packages (Pd < 2W) can readily be derived from existing small outline and chip carrier packages by modifying the leadframe - in much the same way that Powerdip packages were derived from standard Dips.

This approach is particularly attractive because the external dimensions of the package are identical to existing low power packages, allowing the use of standard automatic assembly and test equipment. Frame modification is aimed at obtaining a low junction to pin thermal resistance path for the transfer of heat to a suitable external heatsink. A number of leads are connected to the die pad for this purpose. Two possibilities are considered here : a medium power PLCC44 with 11 heat transfer leads (fig. M) and a medium power SO20 with 8 heat transfer leads (fig. N).

A cost effective heat spreader can be obtained on the board by means of suitably dimensioned copper areas. The heat transfer leads are soldered to there areas (fig. M1, N1).

Figure M : Lead Frame for Medium Power PLCC44.

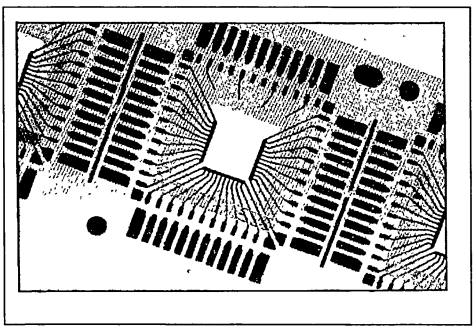


Figure N : Lead Frame for Medium Power SO20.

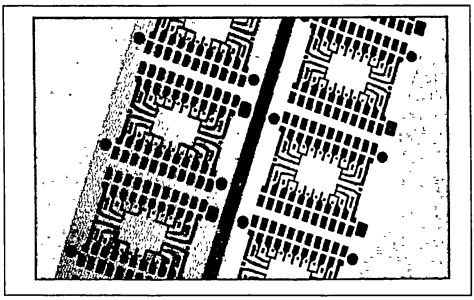


Figure M1 : Test Board for Medium Power PLCC44.

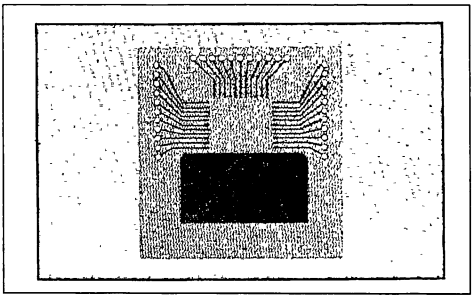
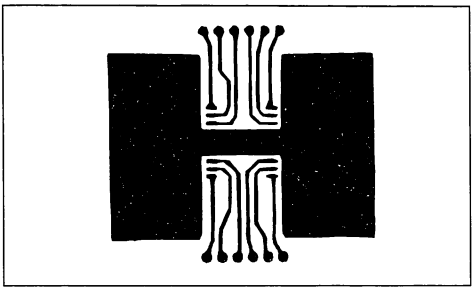


Figure N1 : Test Board for Medium Power SO20.



THERMAL DATA OF SIGNAL PACKAGES

SUMMARY OF JUNCTION TO AMBIENT THERMAL RESISTANCE IN STEADY STATE POWER DISSIPATION (SGS-THOMSON test board)

	Die Size (millinches)	**Power PD [W]**	$R_{th(j-a)}$ **[°C/W] on Board**
SO8 Alloy 42 Copper	90 x 100 94 x 125	0.2 0.2	250-310 130-180
SO14 Alloy 42 Copper Copper	98 x 100 78 x 118 98 x 125	0.3 0.5 0.7	200-240 120-160 105-145
SO16 Alloy 42 Copper	98 x 118 94 x 185	0.3 0.5	180-215 95-135
SO16W Copper	120 x 160	0.7	90-112
SO20 Copper	140 x 220	0.7	77-97
PLCC-20 Cu	180 x 180	0.7	90-110
PLCC-44 Cu	260 x 260	1.5	50-60
PLCC-68 Cu	425 x 425	1.5	40-46
PLCC-84 Cu	450 x 450	2.0	36-41
$R_{th(j-a)}$ values correspond to low and high board density			

SUMMARY OF JUNCTION TO CASE THERMAL RESISTANCE

	Die Pad Size (millinches)	$R_{th(j-a)}$ **[°C/W]**
PLCC20	140 x 140	25
PLCC44	260 x 260	13
PLCC68	425 x 425	10
PLCC84	450 x 450	9

JUNCTION TO AMBIENT THERMAL RESISTANCE IN STEADY STATE POWER DISSIPATION

Figure 1 : SO8.

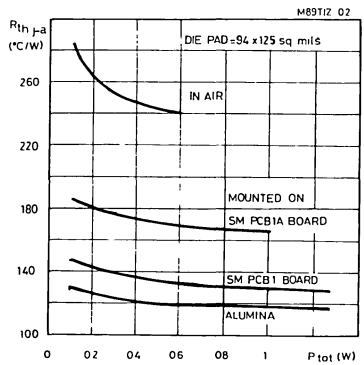


Figure 2 : SO14.

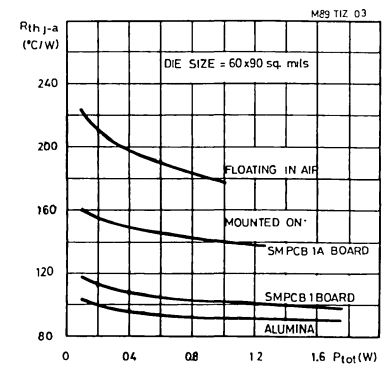


Figure 3 : SO16.

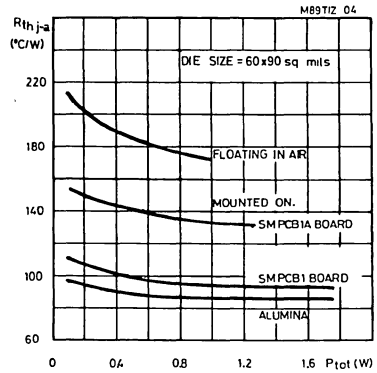


Figure 4 : SO20.

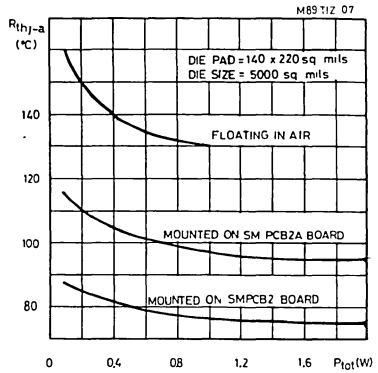


Figure 5 : PLCC20.

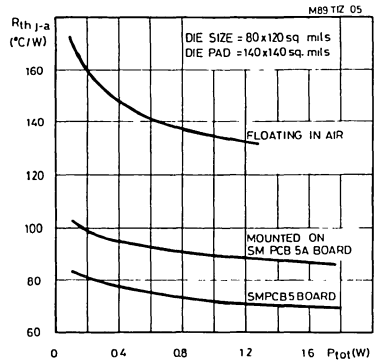


Figure 6 : PLCC44.

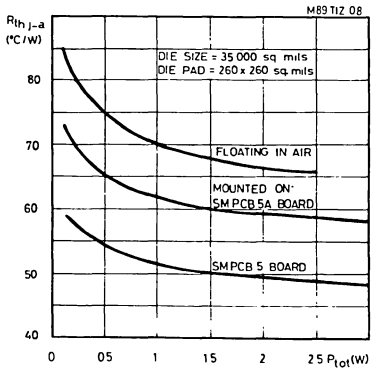


Figure 7 : PLCC68.

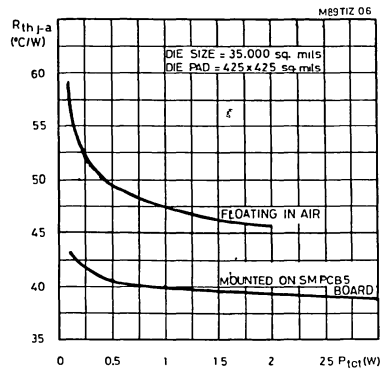
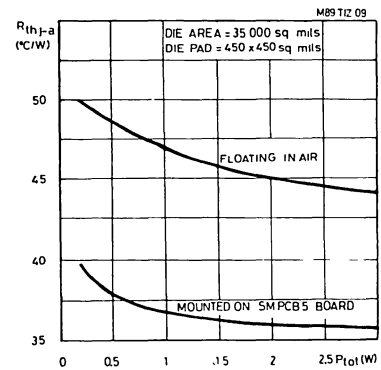


Figure 8 : PLCC84.



JUNCTION TO AMBIENT THERMAL RESISTANCE VS BOARD LAY-OUT

(area of copper tracks on the board)

Figure 9 : SO16.

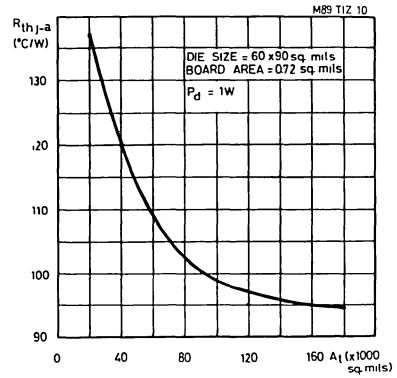


Figure 10 : SO20.

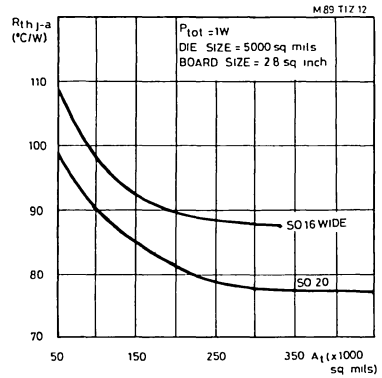


Figure 11 : PLCC44.

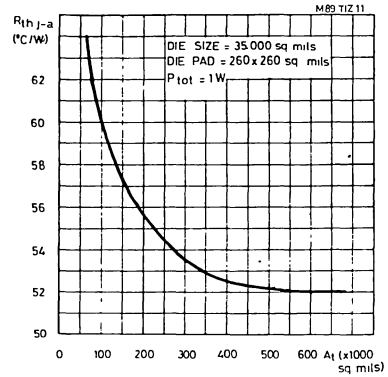
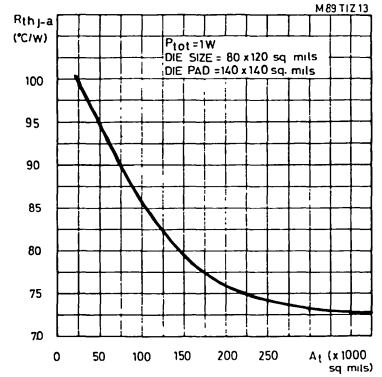


Figure 12 : PLCC20.



TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

Figure 13 : SO8.

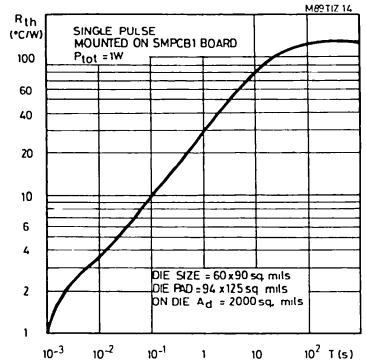


Figure 14 : SO14, 16.

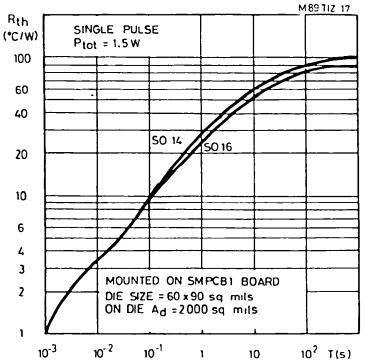


Figure 15 : SO20.

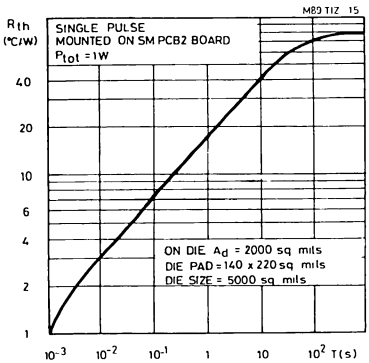


Figure 16 : PLCC44.

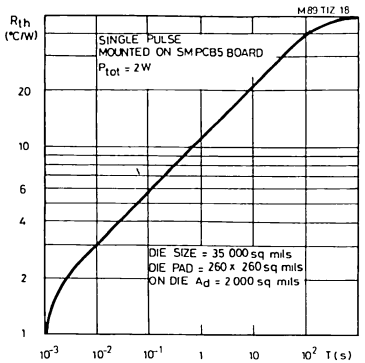


Figure 17 : PLCC68.

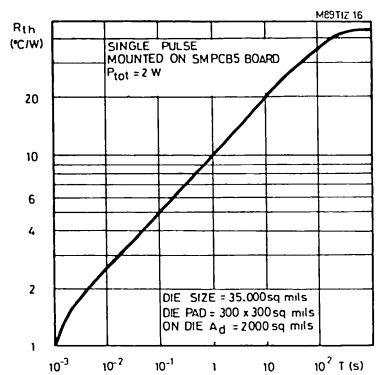
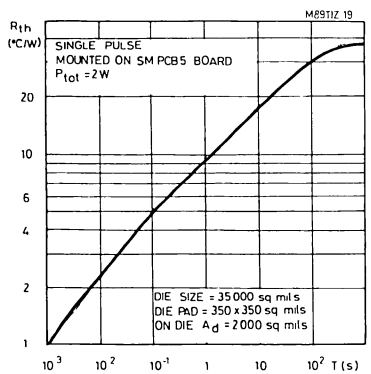


Figure 18 : PLCC84.



PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES

Figure 19 : SO14.

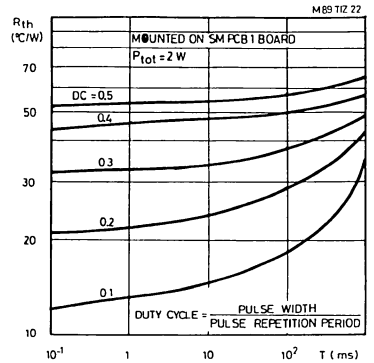


Figure 20 : SO20.

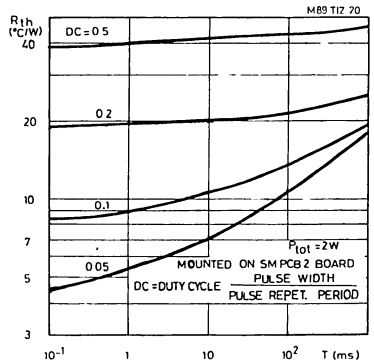


Figure 21 : PLCC44.

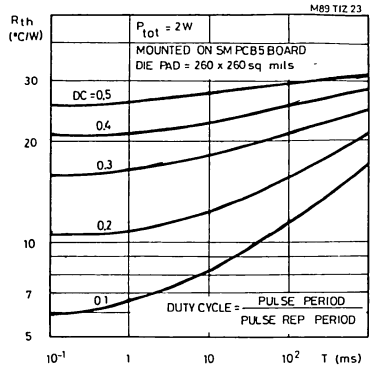


Figure 22 : PLCC68.

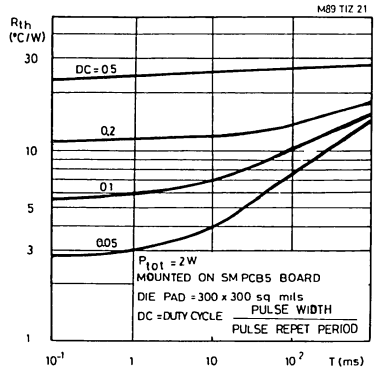
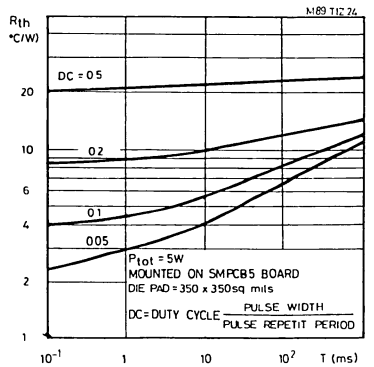


Figure 23 : PLCC84.



THERMAL DATA OF MEDIUM POWER PACKAGES

	$R_{th(j-p)}$ [°C/W] (AVERAGE)	$R_{th(j-a)}$* [°C/W]
SO (12 + 4 + 4)	14	50
PLCC (33 + 11)	12	41

* with 6 sq cm on board heat-sink

JUNCTION TO PINS THERMAL RESISTANCE VS ON DIE DISSIPATING AREA

Figure 24 : SO (12 + 4 + 4).

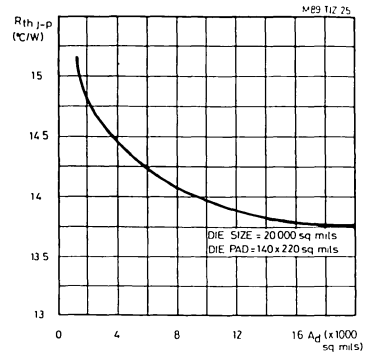
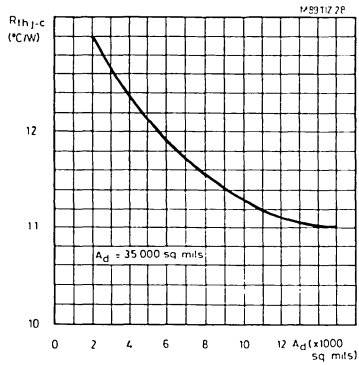
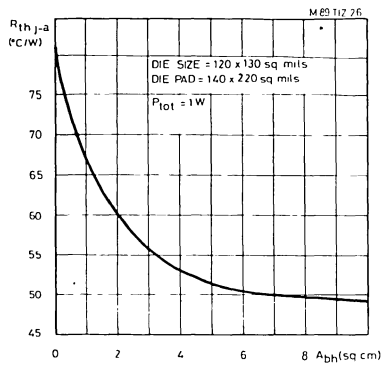


Figure 25 : PLCC (33 + 11).



JUNCTION TO AMBIENT THERMAL RESISTANCE VS AREA ON BOARD HEAT-SINK

Figure 26 : SO (12 + 4 + 4).



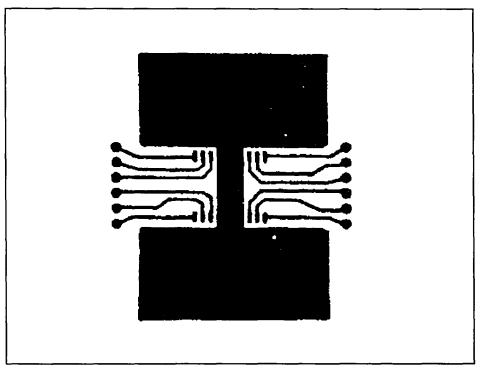
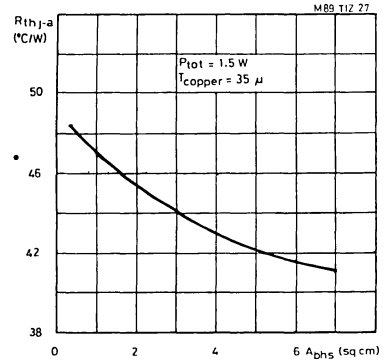
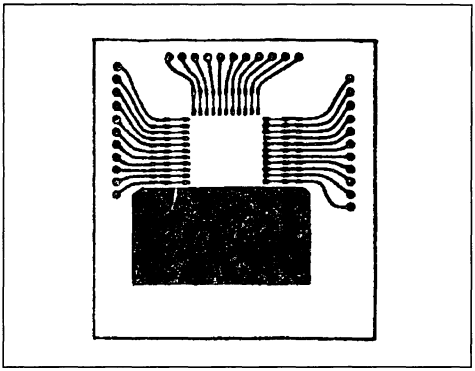


Figure 27 : PLCC (33 + 11).





TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

Figure 28 : SO (12 + 4 + 4).

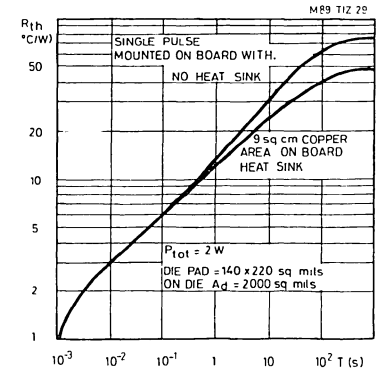
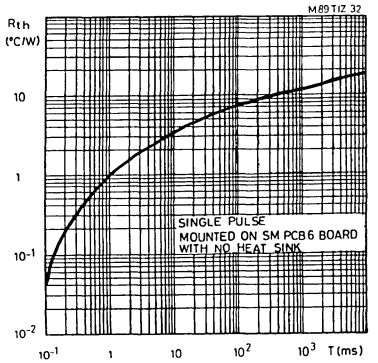
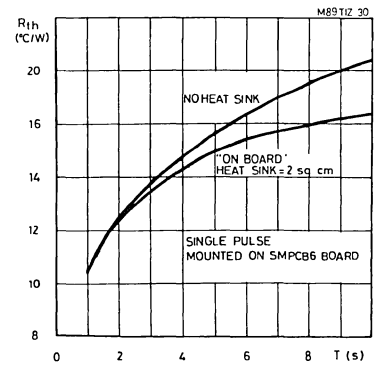


Figure 29 : PLCC (33 + 11).



pulse length = 0.1 – 10ms.

Figure 30 : PLCC (33 + 11).



pulse length = 1 – 10s

PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES.

Figure 31 : PLCC (12 + 4 + 4).

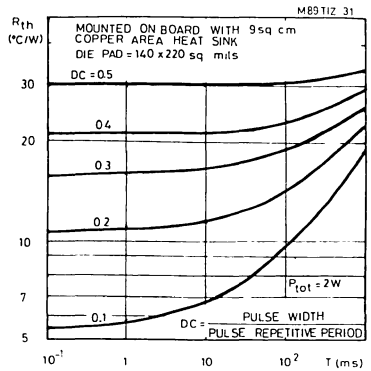
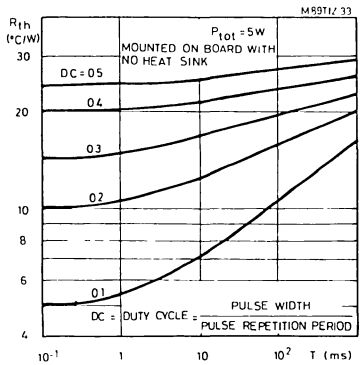


Figure 32 : PLCC (33 + 11).



APPLICATION EXAMPLES OF THERMAL DATA

Good thermal design begins with system and reliability considerations. This turn is based on correct consideration of ambient and device temperature parameters.

The ambient temperature T_a defined for applications can range from 50 to 55°C, as is common in many consumer and computer applications, through to 80°C or more in applications such as automotive systems. The ambient temperature depends on the various heat and cooling sources surrounding the device. An important factor in device lifetime is junction temperature - lifetime is approximately halved when junction temperature T_j is increased by 10°C. The maximum junction temperature commensurate with good reliability, takes into account the activation energy of the failure mechanisms which may differ for various silicon and packaging technologies.

In plastic packages the maximum T_{jmax} is 150°C, but lower values (100 to 120°C) may be specified in high rel applications such as telecoms.

When T_{jmax} and T_a are known, their difference ΔT_j indicates the permissible junction temeperature rise for a given device. For a given power dissipation Pd, the thermal design must ensure that the product Pd x Rth(j-a) is lower than ΔT_j ; where $R_{th(j-a)}$ is the thermal resistance of the device from the junction to the ambient at temperature T_a. This takes into consideration the many elements connected to the heat source and includes the leadframe, moulding compound, substrate and heatsink, if used.

EXAMPLE 1 : Maximum dissipation for SO16 packaged device soldered onto an FR4 board (1 oz copper) under the following conditions :

- Ambient temperature : T_a = 70°C
- Maximum Junction Temperature : T_{jmax} = 130°C

The average length of the 12mils wide copper line connected to each pin is 80mils, soldering pads are 30 x 40mils. The total are is thus :

A = [(80 x 12) + 1200 x 16] = 34560sq.mils

SOLUTION

From fig. 13, the value for $R_{th(j-a)}$ is 125° C/W for a copper frame package. Comparing figs. 5 and 6, a value of about 240°C/W can be assumed for Alloy 42 packages. The allowed rise in junction temperature is : ΔT_{jmax} = 130 - 70 = 60°C

Maximum dissipation is given by $\Delta Tjmax/R_{th(j-a)}$.

Therefore :

60/125 = 0.48W for Copper frame

60/240 = 0.25 for Alloy 42 frame

EXAMPLE 2 : Junction temperature for an SO20 packaged device soldered on FR4, under the following conditions :

- Ambient temperature T_a = 70°C
- Dissipated Power Pd = 0.6W

SOLUTION

A total trace-area of 200k sq.mils is assumed,this then gives, from fig. 14 :

- Thermal Resistance $R_{th(j-a)}$ = 90°C/W
- $\Delta T_j = Pd \times R_{th(j-a)}$
- $\Delta T_j = 0.6 \times 90 = 54°C$
- Junction Temperature $T_j = 54 + 70 = 124°C$

EXAMPLE 3 : To determine the size of an integrated heatsink for a medium power application using a PLCC (33 + 11) under the following conditions :

- Ambient temperature T_a = 50°C
- Max. Junction Temperature T_{jmax} = 150°C
- Dissipated Power Pd = 2.2W

SOLUTION

By calculation the application needs an $R_{th(j-a)}$ of : (150 - 50)/2.2 = 45.5°C/W

From figure 32 the on board heatspreader can thus be defined as needing an area of about 2 sq.cm.

EXAMPLE 4 : Given the application described in example 3 determine the maximum pulse width for a single 4W pulse superimposed on a continuous 1.5W dissipation

SOLUTION

The continuous steady state junction temperature at 1.5W dissipation is :

$T_{jss} = (1.5 \times 45.5) + 50 = 118.25°C$

The single pulse is allowed to cause a maximum increase of (150 - 118.25°C) = 31.75°C.

The related transient thermal resistance is (31.75/4) = 7.9°C/W

From figure 33, the corresponding pulse width can be interpreted as being in the order of 200ms.

EXAMPLE 5 : In a medium power application using an SO (12 + 4 + 4) calculate the average junction temperature and the peak temperature for repeated pulses under the following conditions :

- Ambient temperature T_a = 70°C
- On board heatsink area A = 9 sq.cm.
- Pulse length = 100ms
- Pulse height = 5W
- Duty cycle = 20%

SOLUTION

From figure 31, the thermal resistance is found to be 49°C/W. Thus the average junction temperature can be calculated :

$T_{javg} = (5 \times 49 \times 0.2) + 70 = 119°C$

From figure 36, the peak thermal resistance is given as around 15°C/W. The peak temperature can thus be calculated as :

$T_p = (5 \times 15) + 70 = 145$

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

RESISTANCE TO SOLDERING HEAT AND THERMAL CHARACTERISTICS OF PLASTIC SMDs

By C. Cognetti, E. Stroppolo and R. Tiziani

INTRODUCTION

Surface Mount Technology (SMT) has introduced a number of new technical problems, which have delayed the conversion from insertion assembly.

This is not strange : what readily available source of expertise existed a few years ago ?

Plastic SO packages were introduced in Europe in the early '70s and widely used in hybrids, but hybrid assembly has little relationship with the placement, soldering, handling tools now considered for SM PCB production. Was it surprising that even the semiconductor suppliers with sound experience in SO production could not give all of the answers needed by the PCB manufacturer ?

Japanese experience in SMT based consumer products is impressive : 87% of components used for cameras are in SM versions. However, the degree of complexity and performance of consumer products are somewhat different from the industrial, automotive and telecoms applications the Western world is interested in. On the other hand, in 1985 the percentage of SMDs (active and passive) used in industrial systems produced in Japan was 16.6% in telephones, 5.5% in automotive applications, 5.1% in cable communication, 0.7% in minicomputers[1] ; that is, a level similar to US and European production, presumably with a similar level of expertise.

In the past few years confidence in SMT has increased. More experience exists, which is the result of an expensive learning phase covered by both SMD manufacturers and users.

The reliability of plastic SMDs has an important place in this work. It needs a new approach in comparison with equivalent insertion devices, due to the completely different use.

In 14 years of production, no distinction was made in the authors' company between SO and DIP, from the point of view of reliability. They had the same reliability targets and similar evaluation methodology ; the former was often hot plate soldered on leaded ceramics for more convenient handling but no difference in long-term reliability existed.

With SMT, this is inadequate. Negative effects due to the various assembly processes, and to some thermomechanical influence of the board, can limit the device life.

The present work is focused on SMDs soldered onto a plastic substrate, by means of the most common industrial processes, and takes into account two aspects of reliability :

1. Resistance to soldering heat, i.e., the suitability to withstand the thermal shock associated with the soldering cycle, without reducing reliability. This information is obtained by performing moisture resistance tests. Data about SO packages will be presented. For PLCCs, evaluation is in progress and will be concluded in the first half of 1988.
2. Heat dissipation, which influences the failure rate. This information is obtained with test patterns and test boards designed by SGS-THOMSON Microelectronics and includes thermal impedance in pulsed conditions. A few case studies will be included in this paper but complete characterisations are available elsewhere.[2]

RESISTANCE TO SOLDERING HEAT

In through-hole technology, devices are inserted from the upper side of the board and wave soldered from its lower side.

Only the lead extremities reach the temperature (250-260°C) of the molten solder ; the maximum specified soldering time of 10s is short enough to avoid over-heating of the package body, which generally does not exceed 120-130°C during the whole process.

This temperature is lower than the moulding compound glass transition temperature (160-170°C) and the risk of permanent damage to the package structure or to the silicon die is excluded.

Device reliability is defined almost independently of the soldering time and temperature ; devices under reliability test are mounted on sockets, thus neglecting the effect of the assembly process.

On the contrary, in all industrial SMT processes, devices are soldered in a high temperature ambient (215-260°C), with high heating rate, and the plastic package is kept in glass transition conditions

(figure 1) for a relatively long time (up to 60s). This situation was never encountered before.

Concern over reduced reliability is justified and explains the trend towards defining SMD reliability *after* the soldering cycle, in order to include the effects summarised in table 1.

Figure 1 : Thermal Expansion of Moulding Compounds, Compared with the Temperature of Different Soldering Techniques.

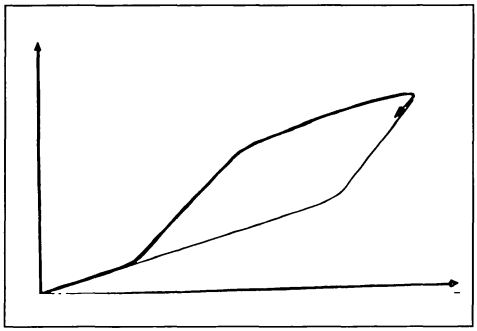


Table 1 : Factors Affecting SMD Reliability on Printed Board.

SMD Package	
Design and Structure	Volume and Thermal Inertia
Internal Contamination	Water Content
Thermomechanical Properties	Lead Solderability
Assembly Process	
Soldering Method	Contamination Level (flux)
Soldering Time/temperature	Rinsing
Substrate	
Thermomechanical Properties	Thermal Dissipation

EXPERIMENTAL

Reliability tests are performed on parts soldered onto test boards (4.5 in. x 6.5 in. FR-4 substrates).

SM PCB1 test board can accept SO-8, 14, 16. It is pre-grooved, in order to be cut in 35 positions, having the lay-out shown in figure 2 ; the SMD footprints are electrically connected to through-holes, with a pitch of 100 mils and placed in two parallel rows, 600 mils apart. Commercial pins inserted in the through-holes give the possibility of using the same equipment needed by DIPs.

The soldering processes from table 2 were used for SO packaged bipolar Operational Amplifiers and C-Mos Standard Logic. In order to simulate a rework, the soldering cycle was repeated on a number of devices. Soldering is followed by the usual rinsing in water or Freon, with or without ultrasonics.

Figure 2 : SM PCB1 Test Board.

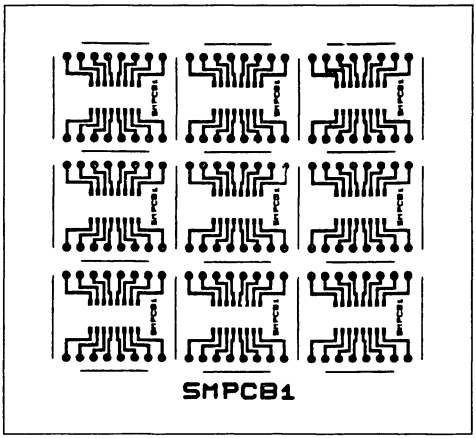


Table 2 : Soldering Processes Evaluated with SO Packaged Devices.

	Pre–heating	Soldering	Number of Cycles
Double Wave	120°C/30s	225°C/4s	1
Double Wave	120°C/30s	250°C/4s	1
Double Wave	110°C/30s	250°C/3 4s	1, 2, 3, 4
Triple Wave	110°C/30s	260°C/3s	1, 2, 3
Vapour Phase		215°C/20s	1, 2
Infra-red	160°C/30s	> 210°C/60s	1

The reliability evaluation was performed by means of the following tests :

Operating Life	150°C
Pressure Pot	121°C/2atm
THB	85°C/85% RH 15V (bips) 6V (CMos)
HAST	130°C/85% RH 15V (bips) 6V (CMos)
Thermal Cycles	– 55/+ 150°C (30/5/30 min)
Thermal Shocks	– 55/+ 150°C (5/1/5 min liquid)

130°C/85%RH Highly Accelerated Steam Test (HAST) has an acceleration factor of about 18-20 (ref. 3) in comparison with 85C/85%RH, and the concrete possibility of reaching wear-out exists with this test, after an acceptable time.

For PLCC packages a similar methodology is followed. At the time of writing, only partial data are available, which will not be included here.

EXPERIMENTAL RESULTS

Experimental results are summarised in tables 3-6.

Table 3 : Cumulative Reliability Data after Multiple Wave Soldering.

Test Vehicles : LM2904 (SO-8), LM2901 (SO-14) and M74HC74 (SO-14)		
Double Wave	225°C/4s	250°C/4s
Triple Wave		260°C/3s
Operating Life 1000h	0/154	0/32
Pressure Pot 96h	0/104	0/62
THB 85°C/85%RH 1000h 2000h	1/105*	0/32 0/32
HAST 130°C/85%RH 100h 200h		0/64 0/64
Thermal Shocks 500	0/231	0/77
* Parametric Failure		

Table 4 : Reliability Data after Vapour Phase Reflow.

Test Vehicle : LM2901 (SO-14)		
	215°C/20s	215°C/40s
Operating Life 1000h		0/32
Pressure Pot 96h		0/32
THB 85°C/85%RH 1000h 2000h		 0/32 0/32
HAST 130°C/85%RH V = 15V 100h 200h 372h 458h 635h	 0/56 0/56 0/24 2/24 5/22	 0/12 0/12 1/12 1/11 3/10
Thermal Cycles 500		0/32
All failures due to pad corrosion		

Table 5 : Cumulative Reliability Data after Infra-red Reflow.

Test Vehicles · M74HC00 and M74HC74 (SO-14)	
	> 210°C/60s
Operating Life 1300h	0/34
THB 85°C/85%RH 1300h	0/34
HAST 130°C/85%RH 100h 200h 500h 672h	 0/32 0/32 0/32 0/32
Thermal Cycles 750	0/70

Table 6 : Cumulative Reliability Data in Multiple Wave Soldering with Repetition of the Soldering Cycle.

Test Vehicles : LM2903 (SO-8), LM2901 and M74HC00 (SO-14)							
		Double Wave 250°C/3.4s			**Triple Wave 260°C/3s**		
Number of Cycles	1	2	3	4	1	2	3
Pressure Pot 96h 504h		 0/56 0/56					
100 Thermal Cycles (– 40/150°C) Followed by Pressure Pot 96h 168h 240h					 0/30 0/30 0/30	 0/30 0/30 0/30	 0/60 0/60 0/60
HAST 130°C/85%RH V = 6V 100h 500h 1000h 1150h 1300h	 0/32	 0/32	 0/32 0/18 0/18 1/18 17/17	 1/32* 0/18 0/18 1/18** 17/17**			
* Parametric Failure ** Pad Corrosion							

COMMENTS ON THE RELIABILITY RESULTS

Previous results do not reveal negative effects due to the exposure of SM devices to the soldering heat, for all of the industrial SMT soldering methods, in combination with the most common solders and cleaning solvents (Freon, water with and without ultrasonics).

Wear-out in the HAST test (130°C/85%RH) is between 1100 and 1300 hours when the soldering cycle is repeated up to 4 times with high temperature (250-260°C) multiple wave soldering, which is considered to transfer the highest thermal stress to the package body.

Pad corrosion is the final failure mechanism for all samples.

This performance is about 7-10 times better than the 2000-3000 h THB 85°C/85%RH, which is currently requested as qualification target in moisture resistance biased tests. Therefore, the reliability of surface mounted devices considered in this work is high enough to meet the most stringent requirements of the professional market.

No evidence of cracks in the plastic case was found in the previous evaluations. This effect (referred to also as 'pop corn' effect) is attributed to some anom-

alous thermal expansion of the package in the soldering phase, caused by water absorbed by the plastic encapsulation : a thermal treatment at a temperature higher than 100°C for a few hours is suggested in order to remove the absorbed water.[4]

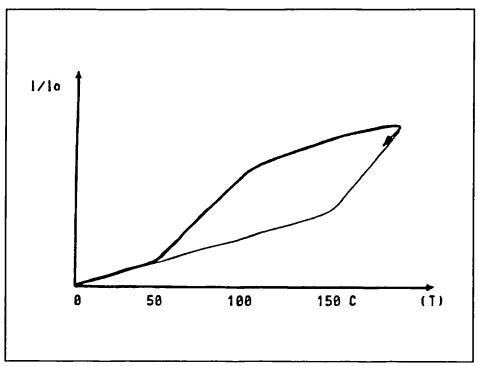
As this thermal pre-conditioning should be performed shortly before soldering, a serious problem arises in the assembly line. Such thermal annealing is not practical when the parts are supplied in plastic tapes or sticks : they should be removed from the packs by the user, heat treated, and packed again with additional costs and risks (co-planarity).

In this company's experience, the 'pop corn' effect can be completely avoided by controlling the frame-encapsulant interface, which is the easiest path for the water. Furthermore, experience has indicated that water at that interface does change the expansion characteristics of the package. About five years ago, the curve of figure 3 was found in some parts (coming from lots affected by the 'pop corn' problem) using Thermo-Mechanical Analysis (TMA). Devices under test were placed between the probes of the TMA transducer and their expansion characteristics recorded.

In the first ramp (5°C/min), package expansion was much higher than the moulding compound expansion between 50 and 100°C ; over 100°C, it returned on the curve typical of the encapsulant. Cooling down and repeating the measurement, only the lower curve of figure 3 was covered.

This behaviour was attributed to water having penetrated between the frame and the plastic body, whose expansion was responsible for the package deformation during the slow heating in TMA. When the parts were soldered on the substrate, cracks could occur due to the much faster heating rate.

Figure 3 : Thermal Expansion of SO Packages.



The problem was solved when the possibility of controlling the water content was found, by means of an improved frame design and some dedicated production steps.

Millions of parts assembled in recent years showed no evidence of the 'pop corn' effect, without any pre-conditioning before use.

The same solutions are successfully adopted for PLCC packages.

THERMAL CHARACTERISTICS

Correlation between reliability and junction temperature Tj is known :

the device lifetime is roughly halved when Tj is increased by 10°C.

Mainly due to this fact, thermal dissipation is a second factor which can influence SMD reliability : a reduced body means worse dissipation and higher power density on the board.

As careful thermal design is the key to improved reliability, a systematic characterisation of SM packages was performed, in order to study the main factors affecting thermal dissipation at both levels of package design and board design.

In the course of this work, the need for some critical revision of the way of producing and using thermal data was evident.

A point which cannot be under-evaluated is the choice of measurement method, as will be discussed later.

Another important point is the following : the common way of specifying the junction to ambient thermal resistance Rth(j-a) is to associate one value of Rth(j-a) to each device.

In the majority of data books, including this company's previous literature, little information is given on the experimental conditions used to obtain that value : the dissipated power and , above all, the kind of interconnection between the package and the measurement set-up (wires, socket or board), which in some cases can become a far from negligible heat transfer element.

Ignoring this contribution was probably justifie with packages having a low thermal conductivity frame, such as Alloy 42 or Kovar.

For those packages, heat spreading was limited to the silicon die and to the die pad ; thermal dissipation was little affected by the surroundings and the measurement assembly had little influence on the final value of Rth(j-a).

This is not the case concerning the same packages with a copper frame, introduced a few years ago to achieve a higher power capability ; due to better thermal conductivity of the leads they are much more sensitive to external dissipating media, eventually used for the measurement.

Similar statements are valid for SMDs and become more important on account of their reduced dimensions.

The concept is summarised in table 7, where the thermal resistance of some dual-in-line (DIP), Small Outline (SO) and Plastic Leaded Chip Carrier (PLCC) packages is given. The influence of the frame thermal conductibity is remarkable ; but likewise remarkable are the differences obtained for the same package, when it is connected by thin wires (and 'floating' in still air) or soldered on a PC board during the measurement.

Table 7 : Junction to Ambient Thermal Resistance (C/W) for DIP and SM Packages in Different Experimental Conditions.

	Power Pd[W]	'Floating' in Air	On SGS Test Board	Ratio
DIP 14 Leads (*)				
Alloy 42 0.25mm	0.5	156	138	1.13
Cu 0.25mm	0.6	125	90	1.39
SO-14 Leads (**)				
Alloy 42 0.25mm	0.4	280	195	1.43
Cu 0.25mm	0.6	190	105	1.80
PLCC-44 Leads (***)				
Cu 0.25mm	1.0	70	52	1.35
die size : (*) = 0.095 in. x 0.110 in. (**) = 0.060 in. x 0.090 in. (***) = 0.180 in. x 0.180 in.				

Especially for SO packages the influence of the substrate on thermal dissipation is noticeable. This fact can help to explain the following points :

1. The Rth(j-a) values published by different SMD suppliers are distributed in too wide a range (more than 70°C/W for SO packages) which handicaps a correct thermal design. Most of the difference is probably due to different test boards, and the availability of standardised measurement methodology should help to give more accurate information.
2. The board lay-out contribution should be studied, in order to quantify the effect of device density : a suitable distance between two or more dissipating elements can be an effective solution for improved reliability.
3. Specification of thermal characteristics should include more elements (power level, board density, package design) which cannot be summarised in one single thermal resistance value, as was commonly the case with Alloy 42 DIPs.

A set of experimental curves was obtained for each SM package,[2] which gives the relationship between these factors ; if used to feed back the board design, they should help to achieve a better thermal performance.

The most significant results will be discussed here.

Moreover, two other factors will be considered.

1. The thermal capacitance of the package, which is significant especially in higher pin count PLCCs ; it delays Tj increase during power transients and is important in switching applications.
2. The frame design in association with a suitable board design ; a low resistance thermal path can be obtained with modified frames ; heat is then conveyed to copper areas obtained on the board and dissipated power can be increased to 2W with SOs and PLCCs.

EXPERIMENTAL METHOD

When thermal measurements on plastic packages are performed, the first consideration is the lack of a standard method : at present, only draft specifications[5] exist, proposed in 1986 and not yet standardised.

The experimental method used in this company since 1984 has anticipated these preliminary recommendations to some extent, as it is based on the P432 thermal test pattern (figure 4) having two npn transistors, with 10W each power capability. A sensing diode is placed on the thermal plateau arising when the transistors are operating in parallel and gives the actual value of Tj, through the calibration curve of its forward voltage Vf (at constant current) vs temperature.

Transistor size, which is not fixed by the documents proposed for standardisation, was intentionally limited to 1000 mils^2, in order to simulate a high power density and characterise the worst case. Die size, which is found to have some influence on thermal resistance when copper frame is used, is slightly smaller than the die pad size and never exceeds 30000 mils^2 in larger packages, such as high pin count PLCCs.

The measurement set-up is shown in figure 5. It is compatible with DC and AC power supply and has an accuracy better than 5%.

The advantages offered by the test pattern are :

(i) high power capability (wider evaluation range) ;

(ii) repeatable electrical characteristics (Vf) and temperature coefficient (1.9mV/C) of the sensing element (accuracy) ;

(iii) high resolution in pulsed conditions (evaluation down to 100s pulses) ;

(iv) better correlation from one package to another.

Alloy 42 frames and copper frames were used for narrow SO packages (150 mils body) ; only copper frames were considered for the others : wide SO (300 mils body) and PLCC packages.

Suitable FR-4 test boards were developed, which will be described case by case.

Figure 4 : Test Pattern P432 Layout.

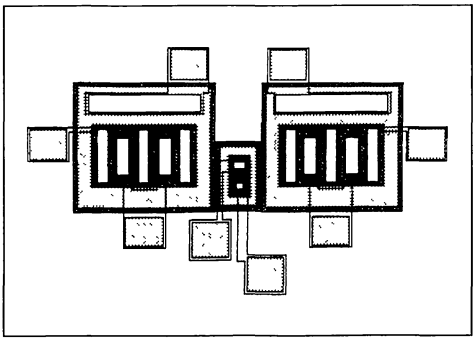
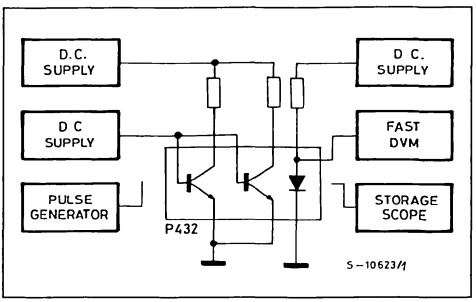


Figure 5 : Measurement System.



THERMAL CHARACTERISTICS IN DC CONDITIONS

Thermal characteristics of the SO-14 package in DC conditions are shown in figure 6.

The upper curve is related to samples floating in still air and connected to 8 thin wires needed for biasing the dissipating transistors and the sensing diode of the P432 test pattern.

Samples soldered on the FR-4 test board shown in figure 2 have an approximately halved thermal resistance ; by reducing the copper pattern length of the test board, different component densities are simulated : thermal resistance is increased by about 30% when the track length has the minimum value.

Dependence of the thermal resistance on the total area of the traces connected to the package is represented by the curve of figure 7. It quantifies the effectiveness of the board lay-out to spread the heat and dissipate it towards the ambient and can be conveniently used for determining the thermal resistance value associated with a given board design.

Figure 6 : Rth(j-a) of SO-14 Package vs. Power Level.

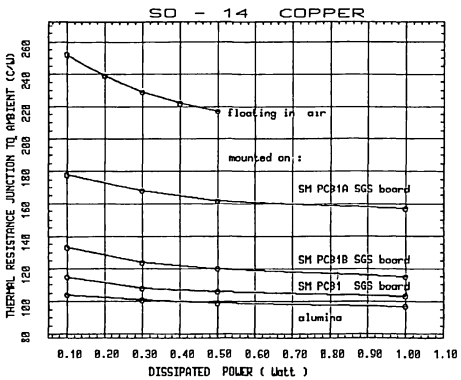


Figure 7 : Rth(j-a) of SO-14 vs. on Board Trace Area.

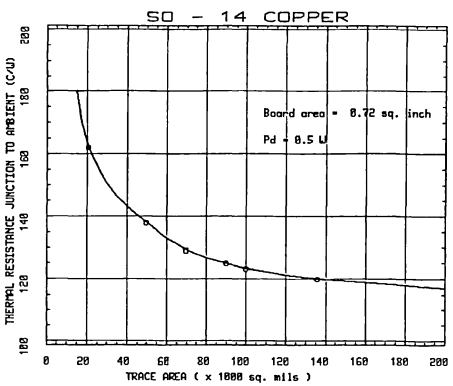
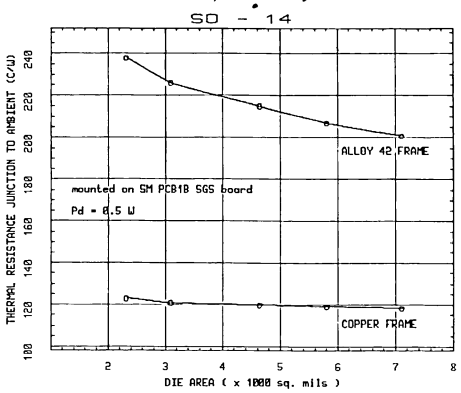


Figure 8 : Rth(j-a) of SO-14 with Copper (SGS-THOMSON) and Alloy 42 Frame.



Comparison of low conductivity (Alloy 42) and high conductivity (copper) frames is shown in figure 8.

The data obtained for the different SM packages are summarised in table 8 ; the two thermal resistance values refer to the two extreme cases of a low density and a high density board.

Table 8 : Summary of Junction to Ambient Thermal Resistance in Steady State Power Dissipation (SGS-THOMSON test boards)

	Die Pad Size (milinches)	Power Pd [W]	Rth(j-a) [°C/W] on Board
SO-8 Alloy 42	90 x 100	0 2	250-310
Copper	95 x 100	0 2	160-210
SO-14 Alloy 42	98 x 118	0 3	200-240
Copper	78 x 118	0 5	120-160
Copper	98 x 125	0 7	105-145
SO-16 Alloy 42	98 x 118	0 3	180-215
Copper	94 x 185	0 5	95-135
SO-16W Copper	120 x 160	0.7	90-112
SO-20 Copper	140 x 220	0 7	77-97
PLCC-20 Cu	180 x 180	0 7	90-110
PLCC-44 Cu	260 x 260	1 5	50-60
PLCC-68 Cu	425 x 425	1 5	40-46
PLCC-84 Cu	450 x 450	2 0	36-41
Rth(j-a) values correspond to low and high board density			

THERMAL IMPEDANCE IN PULSED CONDITIONS

The electrical equivalent of heat dissipation for a module formed by the active device, its package, the board and the external ambient is a chain of RC cells each having a characteristic risetime $\tau = RC$.

Thermal capacitance is the capability of heat accumulation and depends on the heat capacitance of the materials, their volume and their density.

When the power is switched on, the junction temperature after a time t is the result of the subsequent charge of the RC cells, according to the well known exponential relationship :

$$\Delta T_j = Rth \times Pd \times (1 - et/\tau)$$

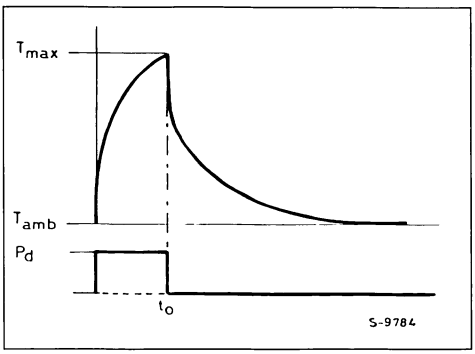
When the pulse length t_o is an assigned value, effective T_j can be significantly lower than the steady state T_j (figure 9) and a transient thermal resistance $Rth(t_o)$ can be defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power.

Obviously, for shorter pulses, transient thermal resistance is lower and a higher power can be dissipated without exceeding the maximum junction temperature defined in reliability considerations.

In a similar way, when pulses of the same height Pd are repeated with a defined duty cycle DC and the pulse is short in comparison with the total risetime of the system, the train of pulses is seen as continuous source at a mean power level :

$$Pd_{avg} = Pd \times DC$$

Figure 9 : Qualitative Tj Increase for Single Power Pulse.



On the other hand, the silicon die has a risetime of 1-2ms and is able to follow frequencies of some kHz : junction temperature oscillates about the average value :

$$\Delta Tj_{avg} = Rth \times Pd_{avg}$$

as qualitatively shown in figure 10.

The thermal resistance corresponding to the peak of the oscillation at the equilibrium (peak thermal resistance) gives information on the maximum temperature reached by the device and, depending on DC and pulse width, can be much lower than DC thermal resistance.

Figure 10 : Qualitative Tj Increase for Repeated Power Pulse.

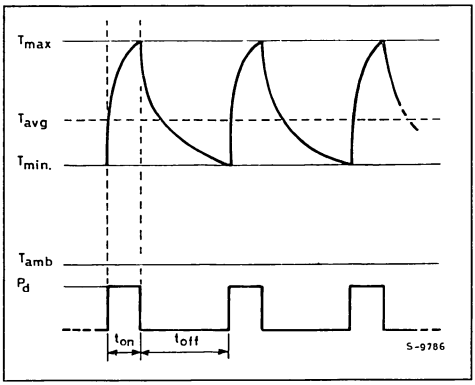
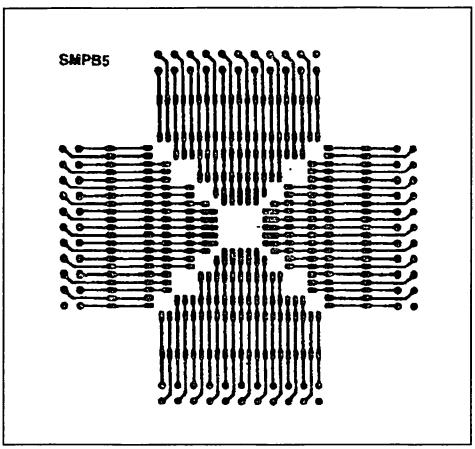
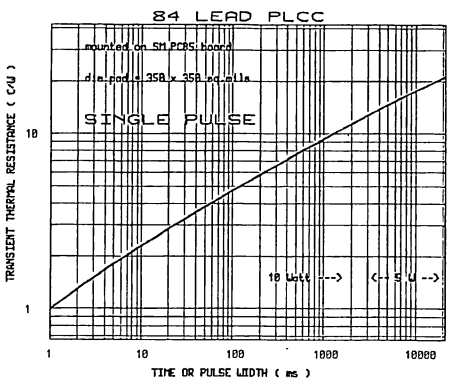


Figure 11 : Test Board for PLCC.



The knowledge of thermal characteristics in the AC condition is a valid tool to reduce redundancy (and cost) in the thermal design of pulsed applications.

Figure 12 : Transient Thermal Resistance for PLCC-84 on Board.



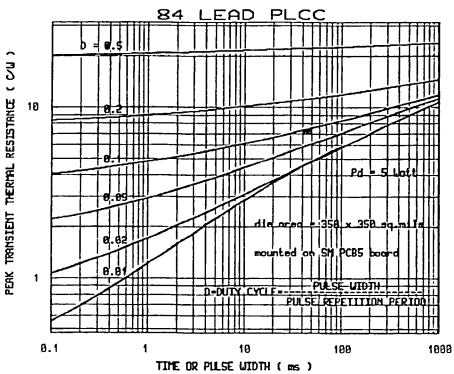
The example is now given of a high pin count PLCC, which has a large thermal capacitance, due to its volume and weight.

Temperature increase for 84 lead PLCCs soldered on the SM PCB5 test board (figure 11) for single pulses of different length is given in figure 12. A rise-time of 50-60s is typical for this package, having a thermal resistance of 38°C W in steady state (see table 8).

For single pulses, the effective thermal resistance is much reduced and acceptable junction temperature is observed even for high power pulses. 10W can be delivered for about 1s (9°C/W) and 5W for 10s (18°C/W).

Peak thermal resistance for repeated pulses, with different duty cycles, is represented in figure 13 and the above considerations are valid in this case also.

Figure 13 : Peak Transient Rth for PLCC-84 on The Board.



MEDIUM POWER APPLICATION

The lack of power packages suitable for SMT requirements (standard outline, automatic handling) is known.

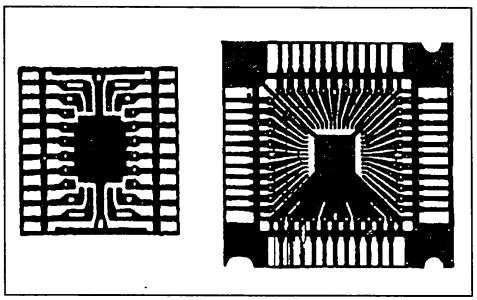
A simple way to achieve power dissipation in the medium range (1-2W) is to transform the available signal packages and modify their frame to obtain a high conduction path.

In figure 14 the frame of medium power SO and PLCC packages is shown : some leads are connected to the die pad, in order to have a low junction-to-pin thermal resistance Rth(j-p). Typical values of this parameter are in the range of 12-15°C/W, with a high conductivity lead frame.

Modification involves the internal part of the frame only, while the external dimensions of the package are not changed ; the solution offers the undoubted advantage of being compatible with existing handling and testing tools.

The heat produced by the IC, and conveyed externally by the heat transfer leads, can be cost effectively transferred to the ambient by means of dedicated copper heatsinks, integrated on the board.

Figure 14 : Medium Power SO and PLCC Frame.



In figure 15, the layout of test boards used for the thermal characterisation of medium power SO-20s (with 8 heat transfer leads) and PLCC-44s (with 11 heat transfer leads) is represented.

The area of the integrated heatsink can be optimised for cost reduction, depending on the dissipation level. In figure 16 the relationship between the Rth(j-a) of the PLCC (33 + 11) and the total dissipating area is given.

It can be noticed that, with 6-7 sq cm of substrate, the thermal resistance of PLCC-44s can be decreased from 55°C/W to 40°C/W, for 1.5-2W dissipation.

A similar performance is possible with the medium power SOs.

Figure 15 : Test Boards for Medium Power SO-20 and PLCC-44 Package.

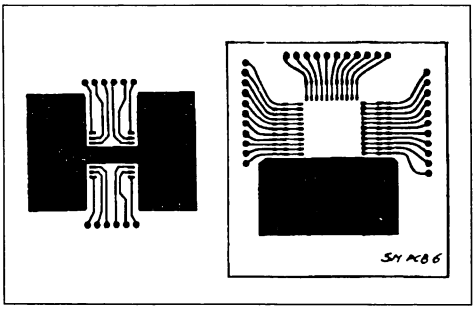
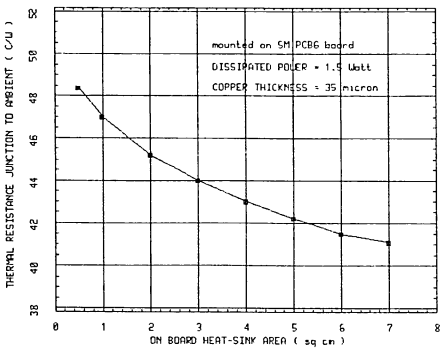


Figure 16 : Rth(j-a) of Medium Power PLCC-44 vs. Dissipating Area on Board.



CONCLUSIONS

In SMT, two main reliability related concerns are resistance to soldering heat and heat dissipation.

RESISTANCE TO SOLDERING HEAT

After extensive evaluation of devices soldered on plastic substrates by means of the three industrial soldering methods (multiple wave soldering, vapour phase and IR reflow), no reliability degradation was found.

The following soldering conditions are possible with SO packaged devices :

- Multiple Wave : T = 250 - 260°C/t = 4s (repetition allowed)
- Vapour Phase : T = 215°C/t = 20s (repetition allowed)
- Infra-red : T > 210°C/t = 60s (Tmax = 225°C)

No crack in the plastic case was evidenced during the above work or in the field, in recent years of production, and no thermal preconditioning was needed. However, this result was obtained after optimisation of the frame design and of the production process. Its extension to the totality of the products existing on the market might be too arbitrary, but it is possible to conclude that the structure of SM packages, when associated with suitable materials and processes, is able to meet the user's requirements.

A similar evaluation is running for PLCC packages and will be completed in the first half of 1988.

HEAT DISSIPATION

Some considerations have been made about the consequence of the lack of some standard evaluation methodology. To standardise test chips and test boards is very important, in order to reach a better knowledge and a better information exchange.

By means of an internally developed test pattern and suitable test boards, three points have been studied :

1. The influence of the substrate on thermal dissipation, whose effect has to be taken into account much more than for insertion packages. With a proper layout it is effective in reducing thermal resistance. For example, dissipation of copper frame SO package can become better than the equivalent Alloy 42 DIP and only 10-20% higher than the equivalent copper DIP.
2. The thermal impedance, whose value is much more suitable for the thermal design of switching applications and can contribute to reduce the cost of the system.
3. The new medium power SO and PLCC packages, which offer the possibility of cost-effective power dissipation in the range of 1.5-2W, still maintaining a standard outline.

REFERENCES

1. Nakahara, H., 'SMT Expands Options in Japan', Electronic Packaging and Production, Vol. 26, No. 1, p. 58, January (1986).
2. SGS-THOMSON Application Notes 106 to 110 on SO-8, 14, 16, 16W, 20 and PLCC-20, 44 (33 + 11), 68, 84.
3. Peck. D. S., 'Comprehensive Model for Humidity Testing Correlation', Proceedings IRPS, p. 44 (1986).
4. Fukuzawa, 1. et al, 'Moisture Resistance Degradation of Plastic LSI by Reflow Soldering', Proceedings IRPS, p. 192 (1985).
5. SEMI Draft Specifications 1377 and 1449 (1986).

HIGH SIDE MONOLITHIC SWITCH IN MULTIPOWER-BCD TECHNOLOGY

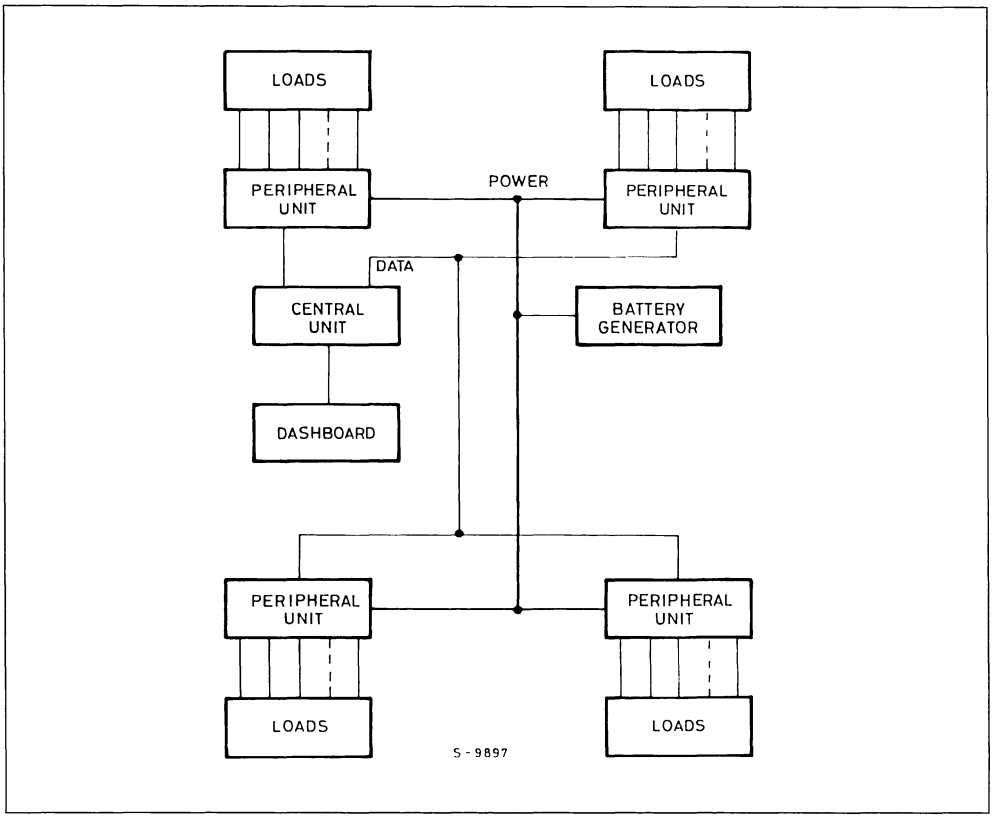
by C.Cini, C. Diazzi, D. Rossi, S. Storti

Recent advances in integrated circuit technology have allowed the realization of a new mixed process integrating isolated DMOS power transistors in combination with bipolar and CMOS signal structures on the same chip. Called Multipower-BCD, this technology has been used to realize a monolithic self-protected high-side switch mainly intended for automotive applications. Driven by TTL, CMOS input logic it can supply resistive or inductive loads up to 6A DC allowing a current peak of 25A with an $R_{DS(on)} = 0.1\Omega$. Fault conditions are signaled on a diagnostic output pin.

ELECTRONIC POWER SWITCHES IN THE CAR

The increase of the number of the electrical components in the car (today more than 50) and the increase in assembly costs shall soon make economical multiplexed power supply and control systems. These systems consist of a single line for power supply and a multiplexed signal network for control ; in this way it is not necessary to have a wire for every load, but only a common power line and a common signal line for all the loads (fig. 1).

Figure 1 : Example of a Multiplexed System.



The control system is made, for example, with a central unit near the dashboard, for the user interface, a serial data transmission line and some peripheral units near the loads (fig. 2).

The multiplexed system not only makes it possible to reduce weight and overall dimensions of the cable harness, now critical in some places (e.g. the junction between the vehicle body and the doors), but, also makes it possible to have a bidirectional signal between peripheral units and the central unit without any extra line, this is useful for fault detection and, in a future, for data transmission to make a more complex informatic system.

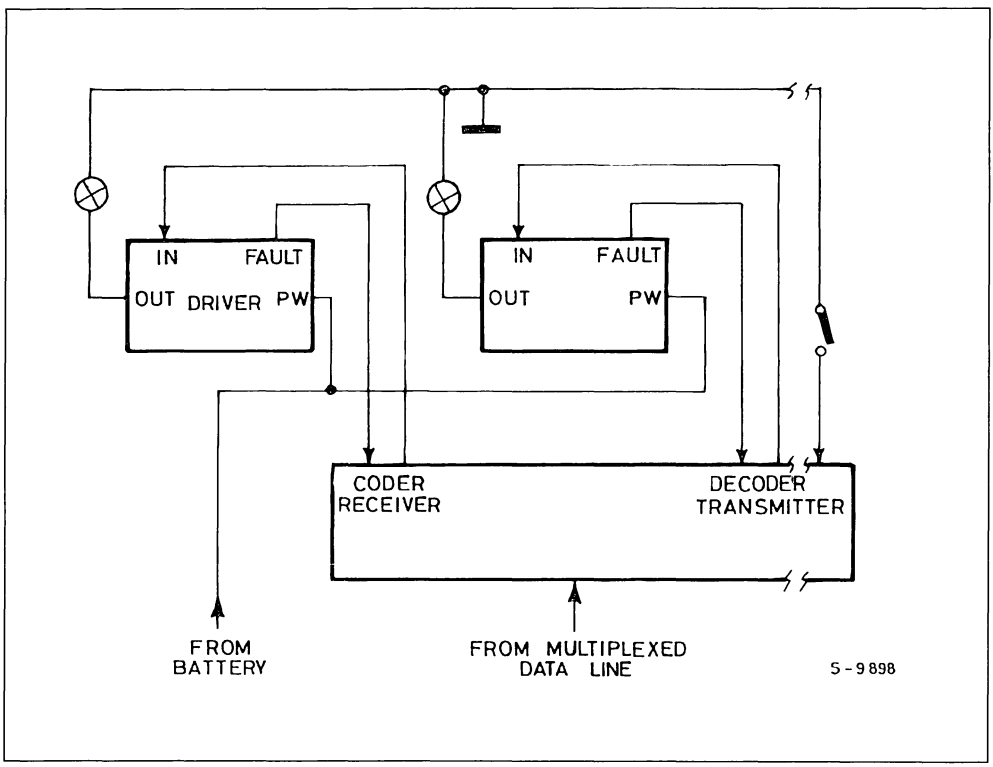
Today the key problem, from the system engineering point of view, is data transmission whereas for semiconductor technology the key problem is the electronic power switches.

The electronic switch, in addition to its main function, must be able :

1) to withstand a very high peak current (20A) with total battery voltage (≡ 14V) applied.
2) to protect itself, the power network and the load against overvoltages (load dump ≡ 60V) and overload (protection with fuses is impractical),
3) to make some fault detections e.g. detect short circuit or open load condition.

For this reasons a simple electromechanic or electronic switch standing alone is not sufficient, a more complex circuit is necessary and for this the monolithic solution is the most effective.

Figure 2 : Block Diagram of a Peripheral Unit.



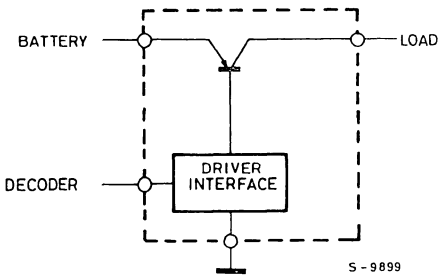
HIGH SIDE DRIVER

The problem of electrochemical corrosion is of primary importance in automotive systems because the electrical components are in an adverse environment (temperature, humidity, salt), for this reason the series switch is connected between the load and the positive power source. Therefore when the electrical component is not powered (that is for the greatest part of the lifetime of the car) it is at the lowest potential and electrochemical corrosion does not take place.

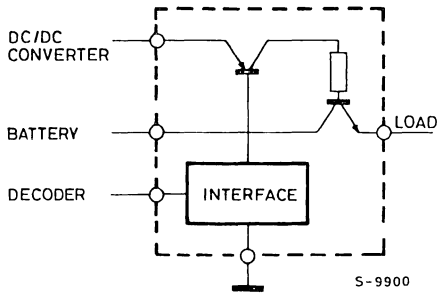
For this connection, components such as power PNP bipolar transistor or Power P-channel MOS would be integrated with low level signal circuitry (fig. 3a), but this kind of element is less efficient and more difficult to realize than their complementary one. NPN bipolar transistors or N-channel MOS, if directly driven by the supply voltage, are not a good solution because the minimum voltage drop on the switch is V_{BE} or V_T (threshold voltage) ; the best solution is to have a driving voltage for the power transistor, higher than the positive supply. Nevertheless a power junction NPN transistor (fig. 3b) needs a certain amount of base current (β = 10-60 to have deep saturation) that could be obtained with a DC-DC converter ; if centralized it complicates the power supply distribution network, if decentralized it complicates the peripheral unit always critical for size, reliability and cost.

Figure 3 : Possible High Side Drivers.

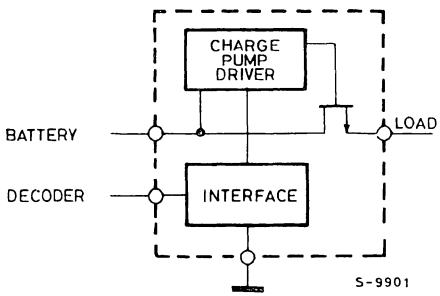
A) with PNP pass transistor



B) with NPN pass transistor (needs external DC-DC converter)



C) with N CHANNEL DMOS



On the other side a POWER MOS N-channel (fig. 3c), being a voltage driven device, requires for the driving only a capacitive charge pump which can be fully integrated on the switch chip.

Bipolar transistors moreover need driving power and principally, are limited in maximum peak power by second breakdown.

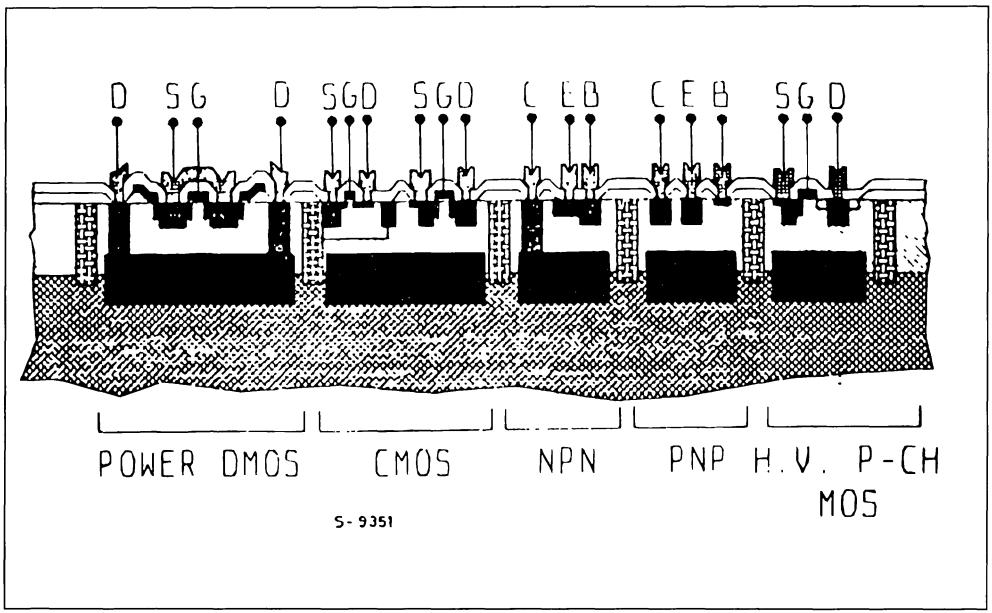
THE PROCESS TECHNOLOGY

For the realization of the device a mixed Bipolar-CMOS-DMOS process has been utilized. This process integrates the following components (tab.1) (Fig. 4) :

Table 1 : Devices in Multipower-BCD Technology.

VERTICAL D-MOS	BV_{DSS} > 60V	V_{TH} = 3V	f_T = 1GHz
P-CHANNEL DRAIN EXTENSION	BV_{DSS} > 75V	V_{TH} = 1.9V	f_T = 200MHz
C-MOS N-CHANNEL	BV_{DSS} > 15V	V_{TH} = 0.9V	
C-MOS P-CHANNEL	BV_{DSS} > 15V	V_{TH} = 1.9V	
BIPOLAR PNP	V_{CEO} > 20V	β = 30	f_T = 10MHz
BIPOLAR NPN1	V_{CEO} > 20V	β = 30	f_T = 300MHz
BIPOLAR NPN2	V_{CEO} > 20V	β = 250	f_T = 1GHz
BIPOLAR NPN3	V_{CEO} > 20V	β = 250	f_T = 140MHz

Figure 4 : A Schematic Cross Section of Bipolar, CMOS and DMOS Structures.

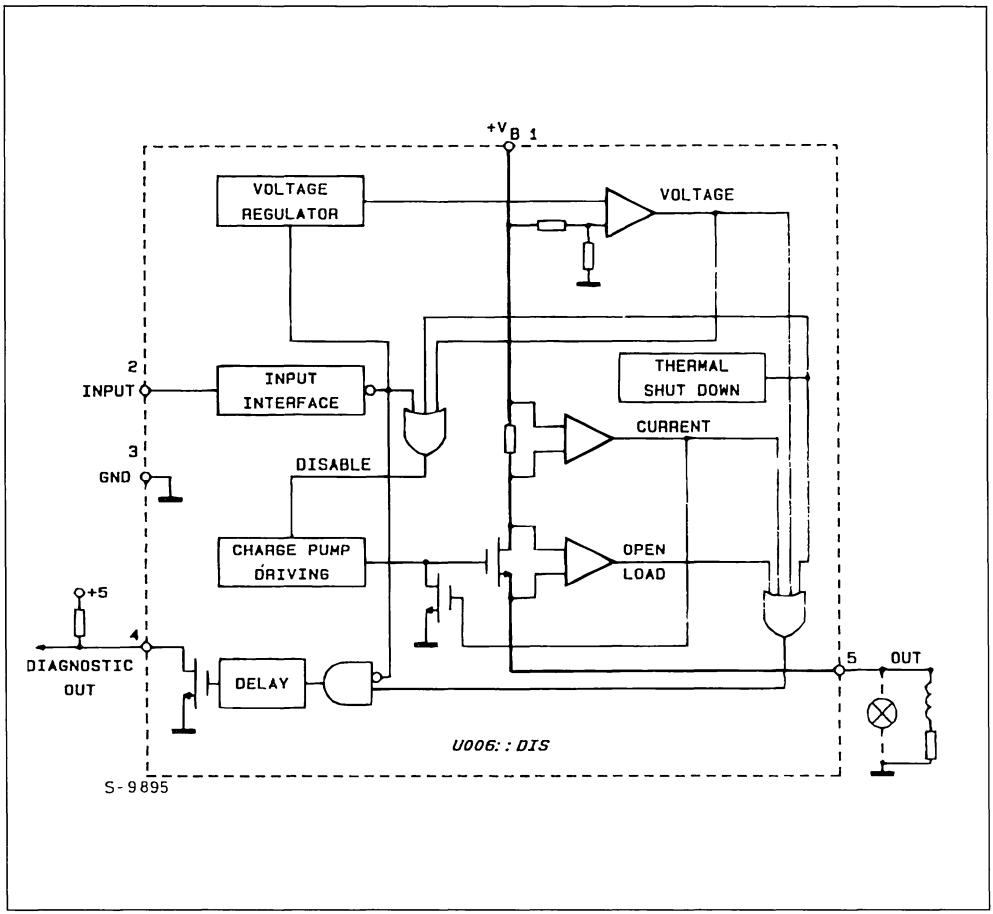


- N-CHANNEL POWER DMOS able to withstand V_{DS} = 60V for the series element.
- BIPOLAR NPN AND PNP TRANSISTORS mainly employed in analog circuitry where low offset and high gain are needed e.g. voltage comparators and references, operational amplifiers.
- CMOS TRANSISTORS to realize a dense logic network with stand by currents practically negligable.
- PASSIVE COMPONENTS as resistors with a great variety of sheet resistivity (30+8500Ω/□) to optimize both very high and very low resistive circuitry and gate oxide capacitors (e.g. to realize charge pump capacitors).

THE CIRCUIT

The circuit (fig. 5) is made by a power DMOS series element, a driving circuit with a charge pump, an input logic interface and some protection and fault detection circuits.

Figure 5 : Block Diagram of High Side Switch L9801.



THE POWER DMOS

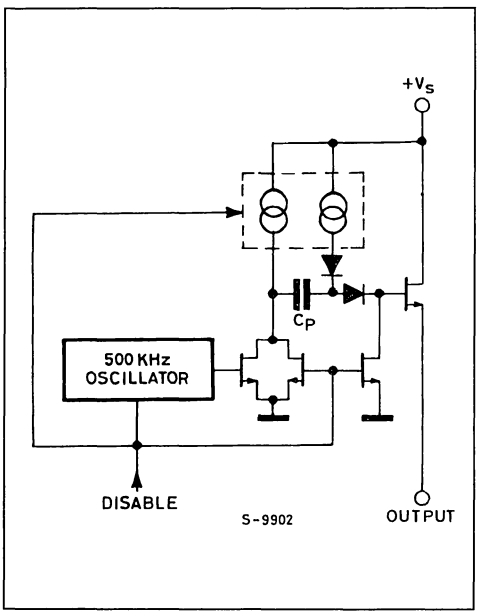
The power DMOS transistor is an array to 10,000 elementary DMOS cells that occupies an area of about 19,000 mils^2 and has a $R_{DS(on)}$ = 80mΩ with V_{GS} = 10V. The low value of $R_{DS(on)}$ is required both to increase the power transferred to the load and to minimize the power dissipated in the device. In fact the switch must be operative also at very high ambient temperature (125°C) as required in automotive applications. For example to drive a 5A (60W) load, the drop on the switch is 400 mV and the dissipated power is 2W ($R_{th\ j\text{-}case}$ 1.25°C/W).

THE CHARGE PUMP

The charge pump is a capacitive voltage doubler (fig. 6) starting from power supply (car. battery), driven by a 500 KHz oscillator.

The pump capacitor is an integrated 80 pF capacitor, the storage capacitor is the gate capacitance of the power itself (~ 500 pF).

Figure 6 : Charge Pump.



INPUT INTERFACE

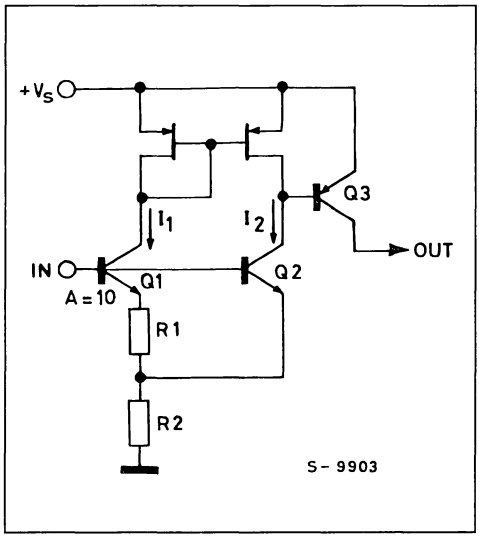
Considering the very wide operating temperature range (Tj = 40 to + 150°C) it is not possible to obtain the logic threshold from the conduction threshold of any elementary device, because of its temperature coefficient, respecting TTL input levels.

Nevertheless a solution with a voltage reference and comparator is not suitable because it needs a bias current flowing also when the device is in the OFF state.

This point is of great importance because the switches are directly connected to the car battery without the interposition of the ignition switch, thus also a little current (> 50μA) multiplied for the number of the switches (e.g. 50), causes an appreciable discharge current always flowing.

For this reason a threshold circuit has been designed derived from a well known voltage reference (fig. 7).

Figure 7 : Input Interface.



Fixed a threshold value $V_{IN} = V_{IN}^*$ for this value must be, by design $I_1 = I_2 = I_0^*$.

if α = area ratio $\quad \alpha = \dfrac{A_{Q1}}{A_{Q2}}$

must be $\quad I_1 = \dfrac{\Delta V_{BE}}{R1}$

$$(I_1 + I_2)\, R2 + V_{BE}\,(Q2) = V_{IN}$$

that is $V_{IN}^* = 2\,\dfrac{R2}{R1}\,\dfrac{KT}{q}\,1n\,\alpha + V_{BE}\ Q2$

Reasoning around the threshold point it can be noted that the transconductance of Q2 is greater than the transconductance in Q1 branch (Q1series R1). For this

if $V_{IN} > V_{IN}^*$	$I_2 > I_1$	Q3 ON
if $V_{IN} < V_{IN}^*$	$I_2 < I_1$	Q3 OFF

The choice of the values is made imposing :

1) $V_{IN}^* \equiv V_{BG} \equiv 1.250V$ band-gap voltage of silicon.

   In this case V_{IN}^* is practically stable in temperature and centered respect TTL input levels ($V_{LMAX} = 0.8V$. $V_{HMIN} = 2V$).

   The idle current I_{ABS} in the worst case, that is when $V_{IN} = V_{L\,MAX} = 0.8V$. $Tj = 150°C$, it must be $I_{ABS} = I_1 + I_2 < 50\mu A$.

The proposed circuit has also a third working region :

when $V_{IN} < V_{BE}$ $I_{ABS} = 0$ Q3 OFF

Observed that the TTL OUTPUT low level is $V_{L\,MAX}$ 0.4V with practical driving circuits the idle current of this interface is zero : only at very high junction temperature ($V_{BE} < 400mV$) or with noise margin = V_{BE} 0.4V) this performance cannot be warranted.

The output of this circuit is useful to switch off not only the power DMOS, but also all the other circuits so that the idle current only the one of the input interface.

PROTECTION AGAINST OVERVOLTAGES

When the supply reaches the maximum operative voltage (18V) the device is turned OFF, protecting itself and the load ; moreover local zener clamps are provided in some critical points to avoid that V_{GS} of any MOS transistor could reach dangerous values even during 60V load-dump transistor.

PROTECTION AGAINST OVERLOAD

If the design of this device the peculiar inrush current of incandescent lamps must be considered, in fact.

1) When the tungsten wire is cold its resistence is about one tenth of the nominal steady state value (e.g. about 300mΩ for a 12V/50V lamp)..
2) The decay time constant for the turn on extracurrent of an incandescent lamp supplied with an ideal voltage source is on the order of some milliseconds.
3) A lamp powered with a constant current slightly higher than its steady state value has a turn on time on the order of 100msec. This time comparable with human reaction time is too much long for all flash-signalling devices.

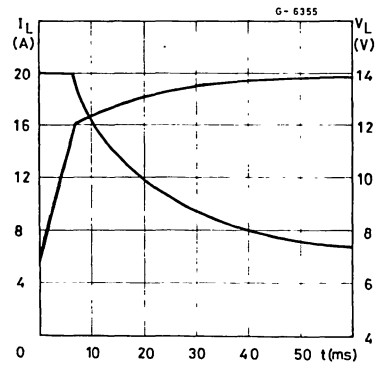
The design choice has been to put a 20A current limit (that is $I_{max} = 5\ I_{nom}$ for a 50W/12V rated lamp). This is a compromise between lamp turn on time (40msec) and electric and thermal dimensioning of the device (fig. 8).

If the high current condition persists (e.g. load short circuit) and the junction temperature rises above 155°C a thermal protection circuit turns off the device preventing any damage.

It must be noted that the power DMOS has no second breakdown, for this reason current limiting and thermal shutdown are sufficient to protect the device against any overload.

Some thermal hysteresis is provided to avoid a potentially critical condition (both current and voltage present during thermal shut down) for the POWER MOS.

Figure 8 : Lamp Current (I_L) and Voltage (V_L) vs. Time with 20A Current Limitation and 12V/50W Lamp.



FAULT DETECTION

When the device is driven and one of the protections (over temperature, overvoltage, overload) is present a fault detection open drain output turns-on. This output is active also when the drop on the POWER MOS is less than 80mV (that is $I_{load} < 1A$) detecting the open load (disconnected or burned-out).

When the device is off the fault detection circuits are not active and output transistor is turned off to allow a minimum quiescent current.

MOTOR AND INDUCTIVE DRIVING

This device can drive unipolar DC motors and solenoids as well, in fact is can recirculate an inductive current when the output voltage goes more than a threshold lower than ground. The possibility to have a high start-up current is useful also for DC motors.

CONCLUSION - FUTURE DEVELOPMENTS

A process allowing the integration of power DMOS, CMOS and BIPOLAR transistor makes possible the construction of a monolithic switch comprehending also protection and fault detection functions.

The power DMOS approach allows also the possibility to make a large range of power switches with different ON resistance and current capability only scaling proportionally the power area.

Moreover the CMOS structures can be utilized to make also the coder/decoder circuit to interface directly the transmission line.

Those features and the possibility to integrate more than one power element on the same chip makes possible, in a near future, the integration of the whole peripheral unit.

VERY LOW DROP REGULATORS ENHANCE SUPPLY PERFORMANCE

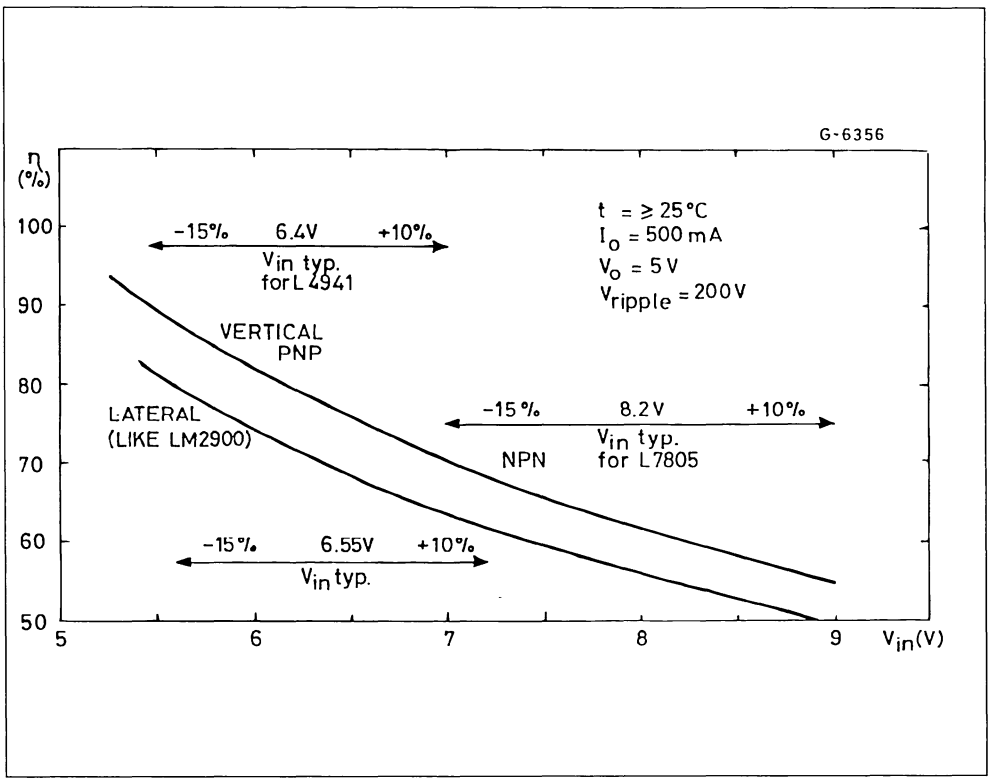
By Paolo ANTONIAZZI and Arturo WOLFSGRUBER

Standard three-terminal voltage regulator ICs use an NPN transistor as the series pass element, so the input-output voltage drop is 1.5V-2V. Low dropout regulators using lateral PNP pass transistors have been available for several years, but a lateral PNP transistor has low gain, so the base current is necessarily high, and a low f_T, so the settling time is poor. Moreover, for stability a large output capacitor is needed.

Applying a new bipolar technology (see APPENDIX : Technology Is The Key) SGS-THOMSON has developed two 5V low drop voltage regulators that use a new vertical PNP transistor structure to obtain low dropout and low quiescent current.

Type L4940 delivers up to 1.5A and offers an input-output voltage drop of 700mV at the full 1.5A output current. A 1A version, type L4941, has an input-output drop of 450mV at 1A (100mV at 0.1A). Both types have a quiescent current of 15mA at 1A (4mA with no load). Consequently these devices dissipates less power, improving the efficiency of any supply system (figure 1).

Figure 1 : A voltage regulator using vertical isolated PNP transistor is more efficient than regulators with NPN pass transistors because the drop out is lower. And it is more efficient than a regulator having a lateral PNP pass transistor because the quiescent current is lower.



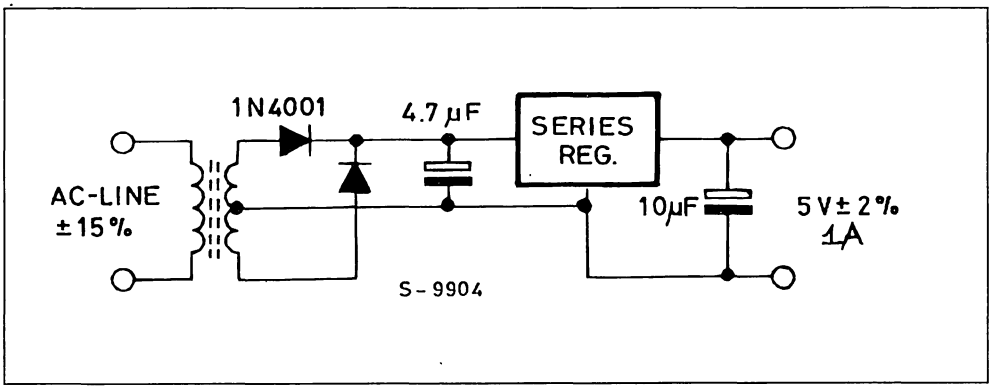
Compared to other "low drop" regulator the L4940 and L4941 have other advantages : regulation performance is guaranteed right down to the minimum input voltage and the device is stable even without an output capacitor. Additionally, a special circuit limits the quiescent current for input voltages from 3V to 5V, typically high for low drop regulators because of the saturation of the series regulator.

The two application areas which benefit the most from second generation low drop regulators like the L4940 and L4941 are post regulation and battery supplies. However, the device brings cost savings in any three-terminal regulator application.

LOW DISSIPATION REDUCES SIZE, WEIGHT & COST

In simple series regulator applications the low dissipation of the L4940/1 reduces the size and weight of the mains transformer, heatsink and printed circuit board. A comparison between equivalent 5V/1A circuits using the L4941 and a standard L7805 regulator (figure 2) shows that the L4941 solution is not only more compact and lighter, it also costs less since the difference in costs between an L4941 and an L7805 is less than the cost saving.

Figure 2 : In simple series regulator applications the L4941 can replace standard three-terminal regulators like the L7805, reducing size, weight and cost. Heat dissipation is reduced, too.



COMPARISON BETWEEN L7805 AND L4941

	L4941		L7805	
Component	**Value**	**Cost***	**Value**	**Cost***
Transformer	220V/7.5V 9.4VA	$4.8	220V/8.6V 11VA	$5.4
Diodes	2x1N4001	$0.1	2x1N4001	$0.1
Capacitors	4.7µF 10V 10µF	$0.5 $0.1	4.7µF 16V 100n	$0.75 $0.08
Heatsink	20°C/W	$0.2	10°C/W	$0.3
PC Area	20cm^2	$0.27	26cm^2	$0.35
		$5.97		$6.98

The L4941 solution, excluding the cost of the IC, is thus $1 cheaper. Moreover it is lighter, more compact and dissipates 1.6W less.

*. guide price for 1000 pieces.

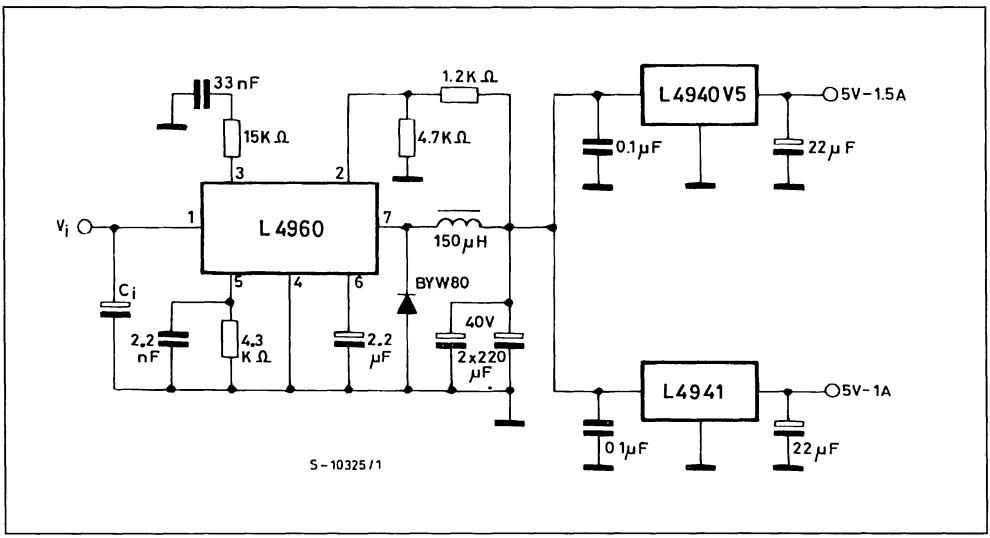
These low drop regulators also bring important benefits in supplies using post regulation, the technique where one or more linear regulators follow another regulator (often switching), to improve precision, reduce ripple and improve transient response. Though lightweight and cheap, an offline switching regulator suffers from poor load and line regulation and needs additional chokes and capacitors to reduce ripple.

Using standard regulators the efficiency of post regulation systems is low because the intermediate voltage must be high enough to allow for the post regulator's voltage drop. Moreover, a lateral PNP low drop regulator has a poor transient response so it cannot reject switching ripple effectively.

If L4940s or L4941s are used for post regulation the intermediate voltage need only be 1V above the final output voltage and 40dB SVR can be obtained at 30kHz. Consequently less power is dissipated both in the post regulators and in the pre-regulator, making post regulation much more attractive -- designers can now have the precision, low ripple and fast response without sacrificing efficiency.

Figure 3 shows a typical post-regulation power supply using a switching regulator, based on the L4960, followed by L4941 low drop regulators.

Figure 3 : Low drop regulators like the L4941 improve the efficiency of post regulation supplies because less power is dissipated and because the intermediate voltage can be lower. In this typical supply design an L4960 offline switching regulator is followed by L4941 post regulators, giving an high overall efficiency.



IMPROVING BATTERY SUPPLIES

The second application area where the L4940 and L4941 are particularly useful is in battery-powered equipment. Because of their lower dropout these devices need fewer battery cells -- five, compared to the six needed for an NPN regulator. In addition, with five NiCd cells the efficiency is 77-96% and the cells can be completely discharged.

The low quiescent current of the L4940 and L4941 reduces power consumption, prolonging battery life. Moreover, since they will continue to provide a stable 5V output with input voltages as low as 5.45V they also extend the effective battery life by allowing continued operation when the battery would previously have been discarded (figure 4).

Figure 4 : The vertical PNP pass transistor permits a minimum dropout without the penalty of higher quiescent current, giving a 30-50% longer battery life in equipment drawing a constant current two hours a day.

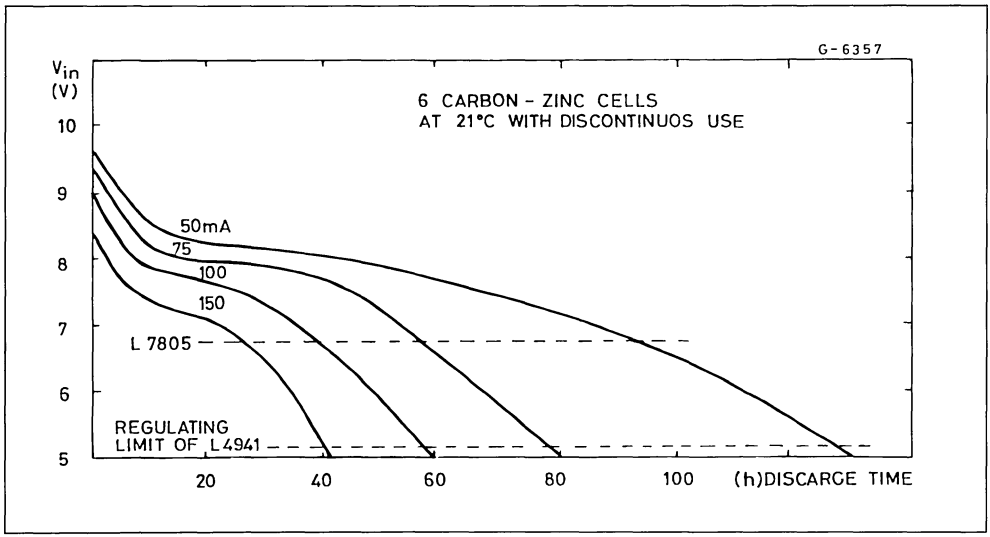
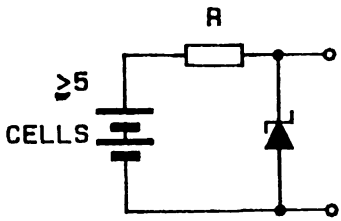
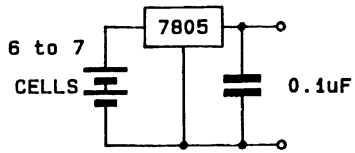


Figure 5 shows how an L4941 solution compares with five alternative 5V battery supplies.

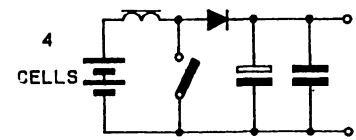
Figure 5 : The L4941 is also useful in battery-powered equipment, prolonging battery life by reducing current drain and supplying a regulated 5V output until the battery voltage has fallen to 5.45V. Here the L4941 solution is compared with five alternatives.



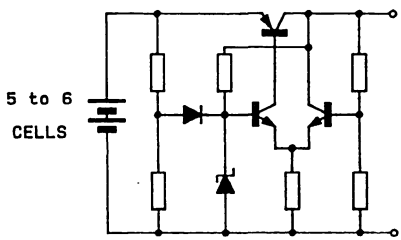
1. ZENER REGULATOR -- High current consumption when battery fully charged and high losses in Rser.



2. NPN SERIES REGULATOR -- Needs at least 7Znn/C, 6NiCd or 4Pd cells..

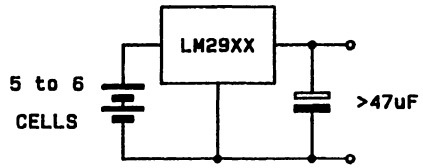


3. DC-DC CONVERTERS -- Complicated and costly. Generates EMI and average efficiency ⇐ 75%.

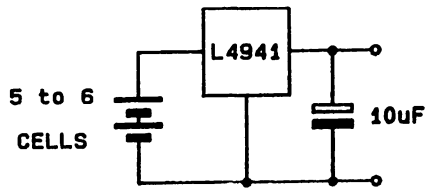


4. DISCRETE LOW DROP REGULATOR -- Bulky and performs poorly in comparison with integrated solutions.

Figure 5 (continued).



5. LATERAL PNP LOW DROP REGULATORS -- High quiescent current, limited output current and stability problems.



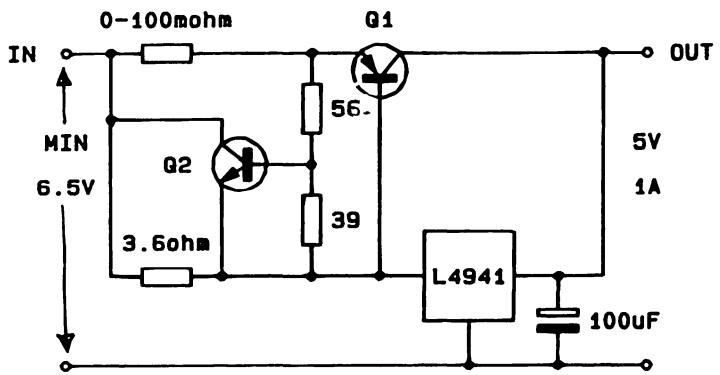
6. L494x VERTICAL PNP LOW DROP REGULATORS -- Need only 6Zn/C cells or 5NiCd cells (which are completely discharged). Quiescent current is low and average efficiency 80%.

HIGHER CURRENT

To obtain more than 1.5A output current a discrete PNP transistor can be added to the L4940 as shown in figure 6. In this circuit Q2 is a current limiter to protect the external pass transistor when the output is short circuited. An on-chip protection circuit prevents damage to the L4940.

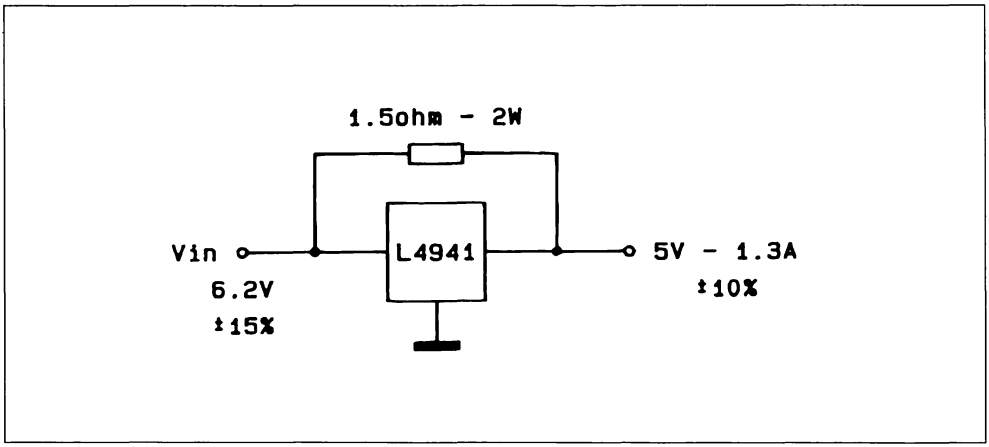
When the load current does not vary greatly higher

Figure 6 : An external PNP transistor can be added to the L4941 to obtain higher output current. Q2 is a current limiter to protect the external transistor.



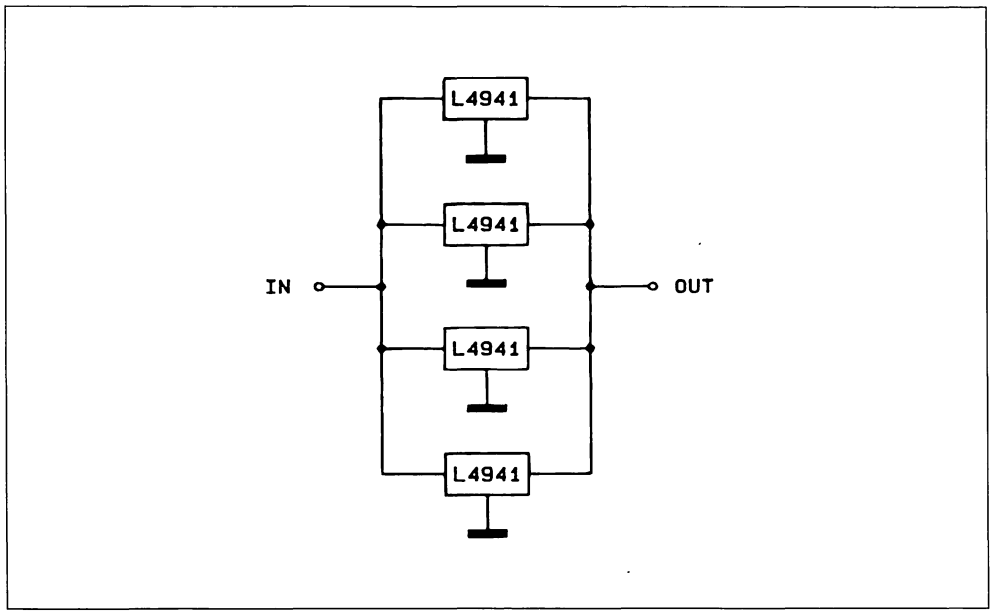
output current can also be obtained by using a shunt resistor as shown in figure 7.

Figure 7 : If the load current does not vary much a simple way to obtain higher current is to add a shunt resistor.



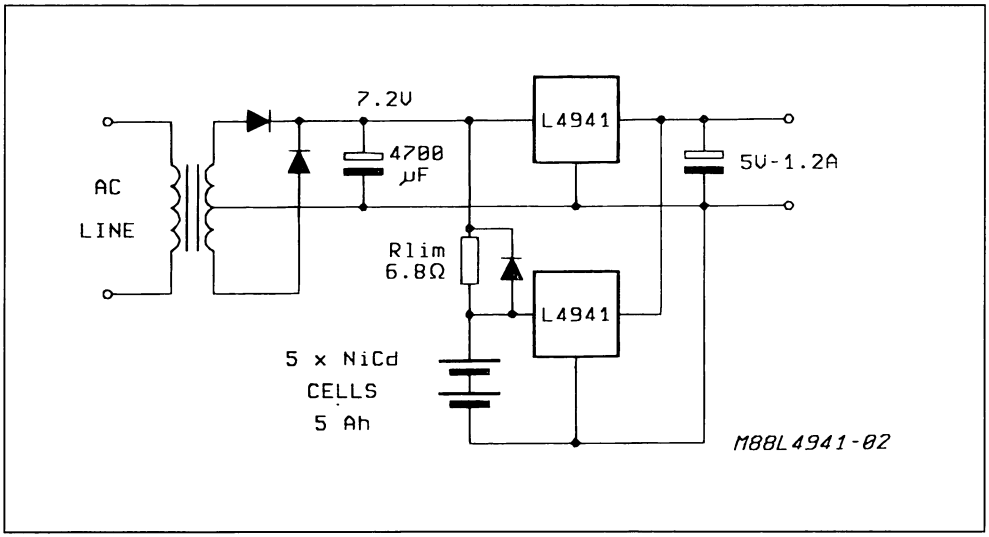
Another way to obtain higher current is simply to connect several devices in parallel as shown in figure 8. This solution also increases the overall reliability of the system and is useful also when reliability is of prime importance.

Figure 8 : Multiple L4941s can be paralleled to increase both output current and reliability.



Finally, higher current can be obtained with two devices in parallel connected to parallel sources (figure 9). This circuit provides an uninterruptable 1.2A/5V output by paralleling the normal line input with a backup battery, which is charged through Rlim when the AC input is present.

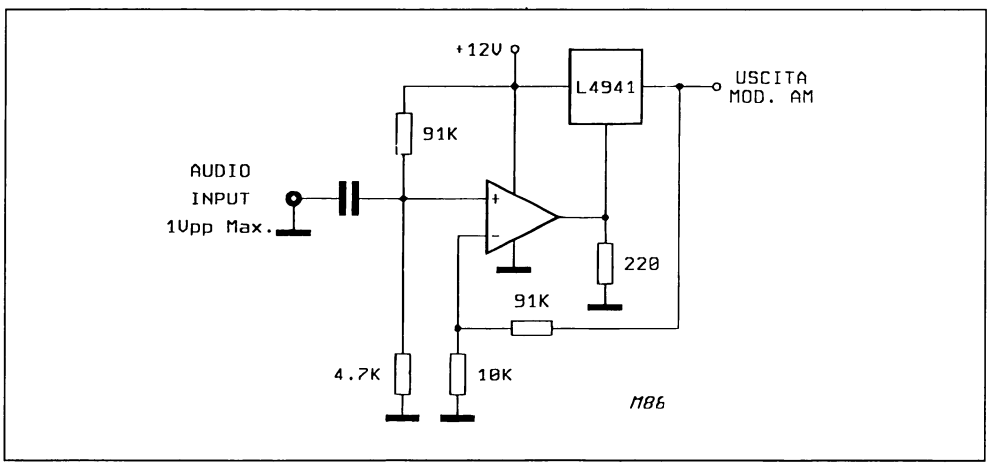
Figure 9 : Connecting two L4941s in parallel with an AC input and a battery yields an efficient 1.2A/5V uninterrutable supply.



USING THE L4941 AS A MODULATOR

Apart from power supply applications, the L4941 can be used as a modulator (figure 10). The modulator part of this circuit is also useful in the lab as a supply for SVR measurements or generally as a basic circuit for an amplifier or generator driving resistive loads. The average output voltage can be varied by adjusting the divider on the non-inverting input of the op amp.

Figure 10 : The L4941 can be used as a modulator as illustrated in this circuit.

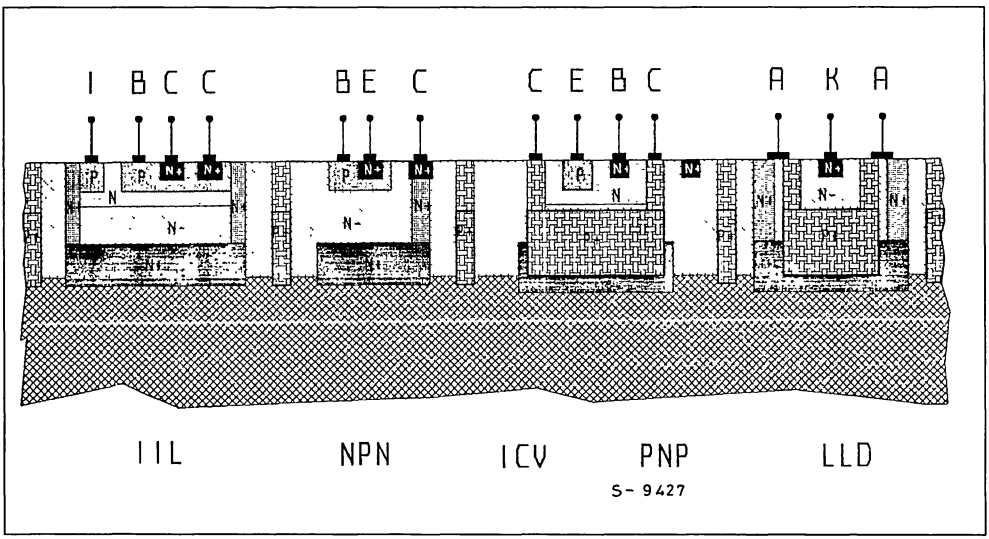


APPENDIX : TECHNOLOGY IS THE KEY

In parallel with the emergence of mixed bipolar/DMOS processes, pure bipolar technology has made significant advances, too. One of the most important of these advances ? the development of a new power PNP transistor structure -- the isolated collector vertical PNP (ICV PNP) -- which is similar in performance to NPN power transistors.

The ICV PNP is a key element in the SGS-THOMSON MICROELECTRONICS Multipower-HDS^2 P^2 (HDS^2 P^2 = High Density Super Signal/Power Process) used to design the L4940 & L4941 low drop regulators, a 20V "Multipower" process which offers NPN & ICV PNP power transistors, small signal NPN & PNP transistors, IIL logic, ECL logic and a new low leakage diode structure (see fig. 11).

Figure 11 : Multipower bipolar process with new ICV-PNP (isolated collector vertical PNP), similar in performance to NPN power transistors.



This process is characterized by an exceptionally high current density -- 6A/mm^2 for NPN transistors ; 2A/mm^2 for PNP transistors (at V_{SAT} = 1V, H_{FE} = 10) -- and very high density in the signal processing section.

Thanks to the ICV PNP power transistor structure, designers can choose any output configuration -- low side, high side, half bridge, bridge. In addition, the low voltage drop of the ICV PNP is very useful in applications where the dropout voltage is critical - in voltage regulators and automotive solenoid drivers, for example.

Another new structure offered by Multipower-HDS^2 P^2, the Low Leakage Diode (LLD) is very useful in power ICs driving inductive loads. With a parasitic PNP gain about four orders of magnitude lower than conventional diodes, the LLDs reduce dissipation in the chip -- always an important consideration in power IC design.

Multipower-HDS^2 P^2 can be applied in simple products where an ICV PNP output stage is needed such as the L4941. Moreover, because it allows the integration of very complex control circuits it is also used for power ICs which integrate a complete power subsystem such as the L6217, a single chip microstepping drive for stepper motors.

A similar process rated at 60V -- Multipower-S^2 P^2 -- has also been developed. While Multipower-HDS^2 P^2 is aimed at low voltage, high complexity applications, Multipower-S^2 P^2 is intended for higher voltage applications with medium complexity control circuits.

FULLY PROTECTED HIGH VOLTAGE INTERFACE FOR ELECTRONIC IGNITION

By S. PALARA ; M. PAPARO ; R. PELLICANO

INTRODUCTION

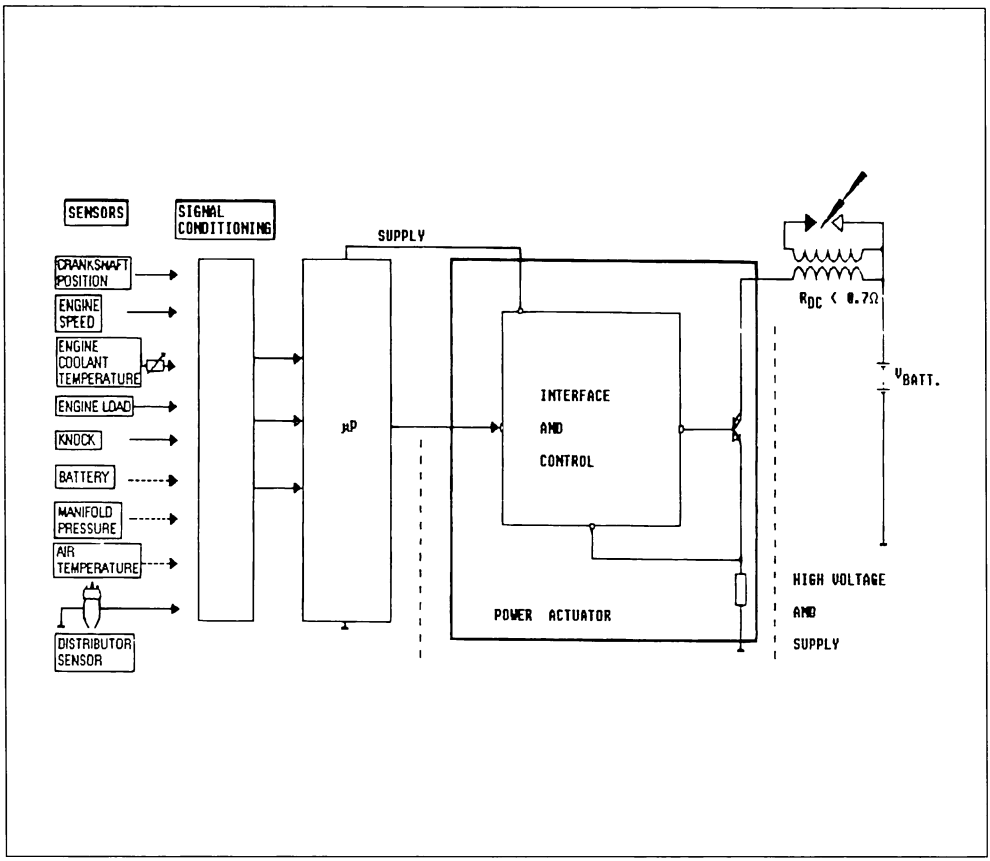
It is well known that an electronic car ignition system must be able to generate and supply the high energy discharge to the spark plugs, firing the petrol/air mixture at a precise point in each piston cycle.This job is performed by means of an high energy coil, its driver stage and the most suitable controller ; an example is shown in fig. 1.

In the most recent car ignition systems the coil current loading signal is controlled by a microprocessor that can also optimize the ignition timing. This ensures the correct spark at every speed for all environmental conditions.

The engine efficiency is so optimized ensuring the minimum toxic exhaust gas emission.

The high voltage necessary to generate the spark is obtained by charging the primary winding of the ignition coil with a controlled energy, i.e. a controlled current.

Figure 1 : Car Ignition System.



At the firing point this current is suddenly interrupted transferring the stored energy to the secondary winding and produces output voltage in excess of 20KV and therefore the spark.

The fig. 1 power actuator must also limit the current to a max of 10A and the voltage on the primary to a maximum of about 400V.

The voltage clamp avoids any damage to the power actuator : if the spark plug, for example, is disconnected, the energy stored in the coil is transferred back to the power actuator.

The device described in this paper realizes these power actuator functions with a very innovative integrated single chip solution.

THE VIPOWER M1 TECHNOLOGY

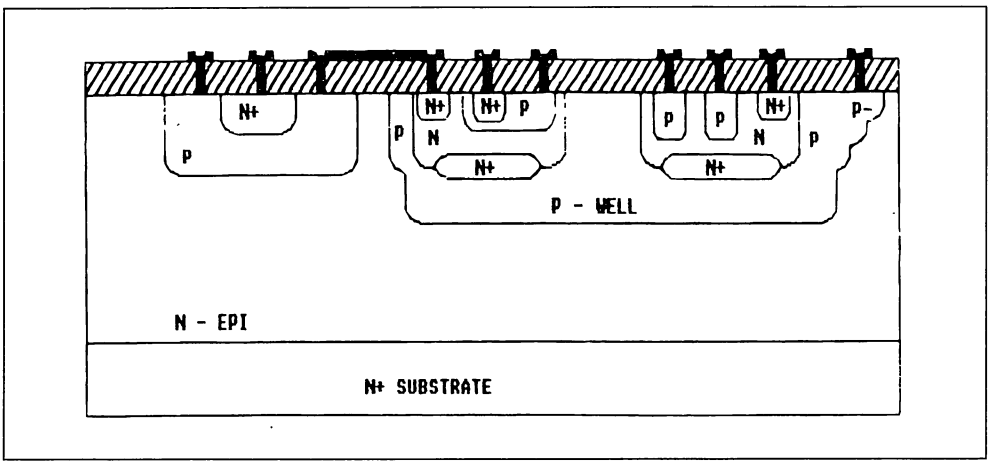
The VIPower M1 structure shown in fig. 2 combines a vertical current flow NPN power transistor and a low voltage junction isolated I.C. on the same silicon substrate.

This is realized inside a diffused p-type well that takes the place of a reverse-biased p-substrate of conventional ICs and must be connected to the most negative supply.

As in a standard discrete BJT, the first epitaxial layer thickness and resistivity set the Vceo and the ruggedness of the high voltage device, the second epi growth fixes the features of the low voltage components (up to 100V V_{CBO}).

The maximum voltage the power device can withstand is neverthless also dependent on the maximum field strentgh at the silicon surface and on the n^+/p–well parasitic diode breakdown voltage.

Figure 2 : VIPower Technology Vertical Structure.



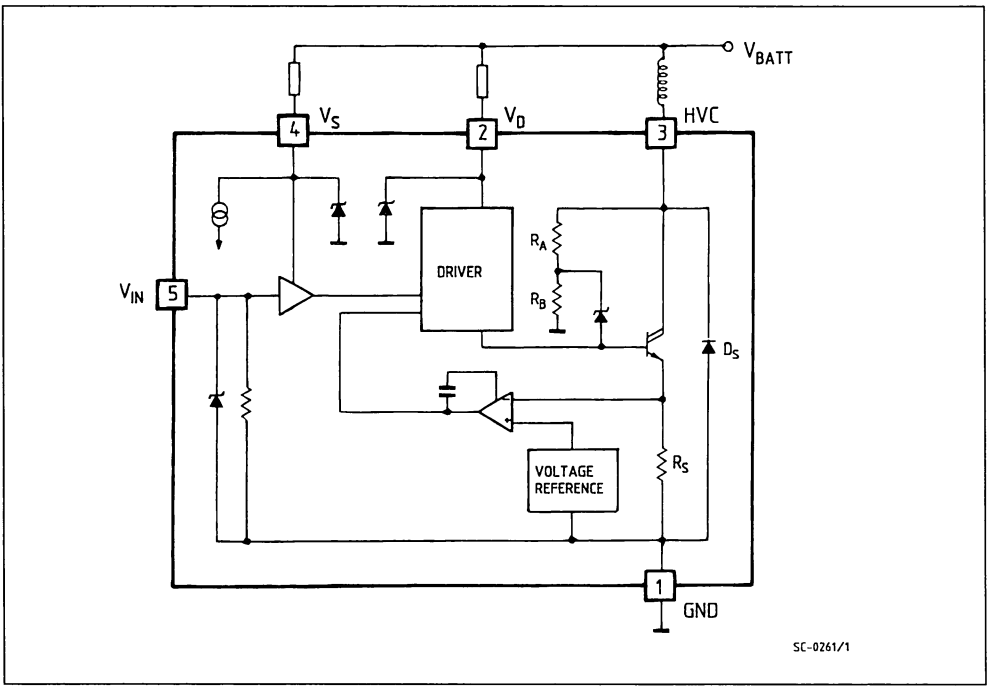
The high voltage termination of the integrated circuit is achieved by a p-diffused resistor in spiral from connected between the substrate (power darlington collector) and ground.

DEVICE CHARACTERISTICS

The device realizes the ignition, power actuator subsystem of fig. 1.

In the block diagram of fig. 3 the power Darlington with its driver and input stage, the current limit, voltage clamp circuitry and the overvoltage protection are shown.

Figure 3 : Device Block Diagram.



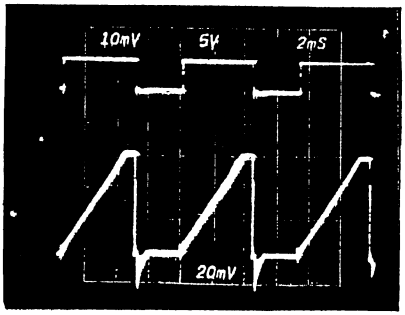
A TTL/CMOS compatible input signal coming from a logic interface, like a microprocessor, determines the turn on of the power darlington integrated in the chip.

The darlington collector current charges the coil linearly as long as a set level is reached, typically 6A ± 3%, sensed by an internal aluminium emitter resistance.

The voltage drop on this resistor is compared with an internally generated threshold (~ 200mV) and limits the current, thus controlling the Darlington base current until the input signal causes the output Darlington to switch off.

Photo 1 shows the coil current behaviour together with the corresponding input signal.

Photo 1 : Collector Current and Corresponding Input Signal.



Input signal (5V/div)

Coll. current (2A/div)

The current loop is made by compensated operational amplifier ensuring enough precision of the set value and hence of the stored energy without requiring external components.

The regulation stability is infact mandatory in the car ignition system to avoid spurious sparks on the secondary coil winding.

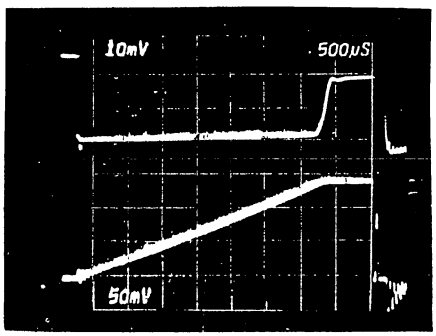
During the current limiting phase, the Darlington collector voltage reaches the battery voltage minus the voltage drop on the coil (due to the primary resistance). It causes high power dissipation in the power actuator which the microprocessor minimizes by delaying the output Darlington switch on.

The overvoltage on the power Darlington collector during the transition from the coil charging to the current limiting phase is low enough to avoid undesiderable sparks.

At the input signal switch-off the power Darlington is immediately turned off and the energy stored in the coil is transferred from the primary to the secondary winding causing the spark.

The collector voltage of the power Darlington then rises very rapidly and is detected by the spiral resistor used as the high voltage termination for the chip.

Photo 2 : Collector Voltage During Coil Charging.



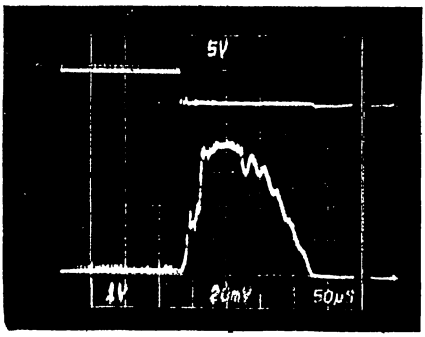
Coll. volt. (5V/div)

Coll. current (2A/div)

This resistor, used as a divider, is connected to a low voltage zener circuit that turns on the power Darlington, holding the collector voltage at a value determined in the chip (~ 400V ± 10%) which is less than the Darlington V_{CEO}.

Photo 3 shows the collector voltage during the clamp in absence of the spark plug i.e. the worst case for stress on the integrated circuit.

Photo 3 : Voltage Clamp.

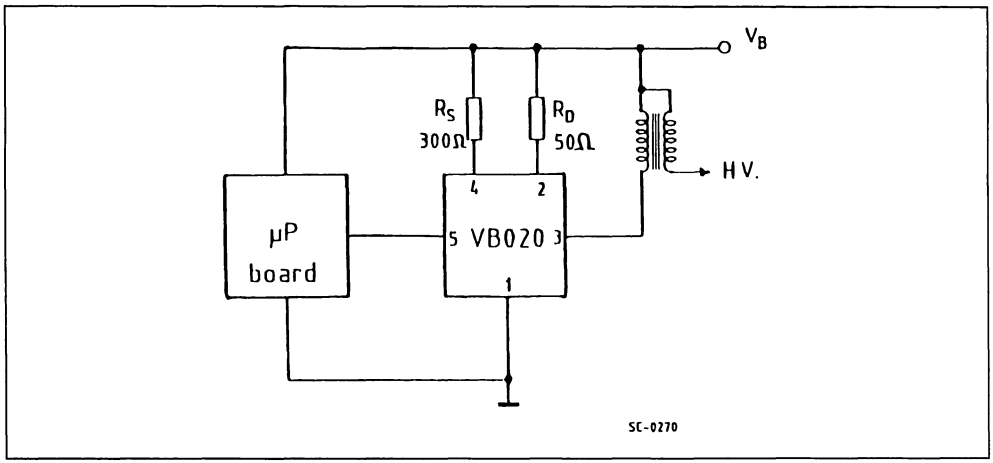


Input signal (5V/div)

Coll. volt. (100V/div)

Fig. 4 shows the application circuit for this device.

Figure 4 : Application Circuit .



Two separate pins for the supply : pin 4 and pin 2, are connected to the battery by means of two different resistors.

Pin 2 represents the supply of the driver with a current of up to 200mA.

Pin 4 is the supply for the rest of the circuit ($I_{4.1}$ ~ 3mA).

A picture of the die is shown in photograph 4.

The device is assembled in a new fully insulated five-lead plastic power package, ISOWATT 5 and shown in figure 5.

Photo 4 : The Die.

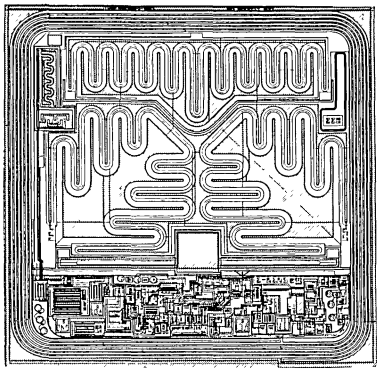
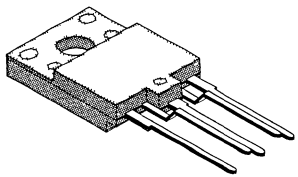


Figure 5.

ISOWATT 5



CONCLUSION

The ignition controller described in this paper completely substitutes the existing hybrid solution which requires additional components and manufacturing processes (i.e. insulating substrates, ink layers, active and special passive devices, laser trimming, encapsulation etc..). This single chip solution leads to an intrinsic increased compactness. The subsequent higher reliability is further enhanced by the known advantages of integration.

Additionally to that a cost reduction benefit through this approach is also achievable.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

NEW LEVELS OF INTEGRATION IN AUTOMOTIVE ELECTRONICS

by Riccardo Ferrari , Marco Morelli

One of the fastest growth areas today in electronics is in the automotive field. In this note the authors describe the particular needs of this field and some typical dedicated ICs developed by SGS-THOMSON.

INTRODUCTION

Since the early seventies, more and more functions have been added to our cars not only with the purpose of guaranteeing a better comfort to drivers and passengers, but also to reduce operating costs and finally to ensure compliance with new regulations concerning noise and pollution are concerned. Because of all these needs, cars have to house more and more modules designed to perform more or less complex operations (Fig. 1).

This growth makes more and more evident the need to reduce the room taken by each module, with the double target of minimizing the cost of the particular function and increasing the number of functions in a specific car; in parallel, by increasing the number of modules, it becomes mandatory to increase the reliability of each of them, otherwise the reliability of the total car would be badly affected.

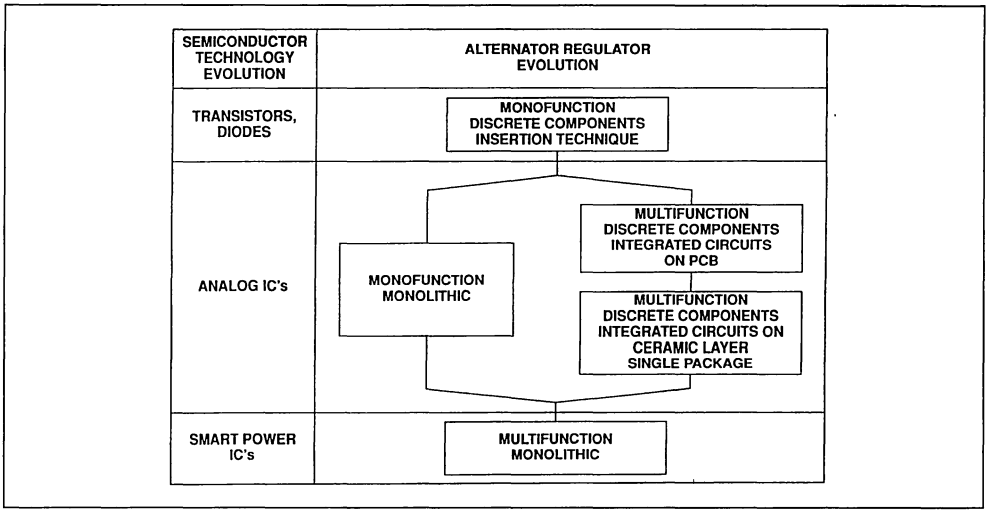
All these issues recently pushed the manufacturers of automotive systems to refer very often to producers of integrated circuits asking for the development of monolithic devices capable of replacing effectively a number of discrete components, passive parts included; anyway the trend to a total integration is not over by just designing onto a simple piece of silicon a complete function, but it carries on implementing in the same device a number of auxiliary services, that would add a substantial cost if achieved by discrete components, that can easily find place on a few extra square millimeters of silicon.

To that purpose the example given by the alternator regulator, subject of a specific description in the following pages, is particularly enlightening. Figure 2 shows briefly the evolution of the alternator regulator paralleled with the evolution of the silicon technology; it is evident that the key issue to pursue the monolithic design of very complex functions in the automotive environment is the availability of process capable to host on the same chip high density signal circuitry, together with power stages managing currents of several amperes; a process with these characteristics is usually called "smart power" process.

Figure 1: Electronics in present and future automobiles.

SAFETY & CONVENIENCE	BODY CONTROL	POWER TRAIN	DRIVER INFORMATION
Rear Window Defogger	Cruise Control	Ignition	Digital Gauges
Climate Control	Intermittent Wipar	Spark Timing	Digital Clock
Keyless Entry	Antitheft Devices	Voltage Regulator	Multitons Alarms
Automatic Door Lock	Electr. Suspension	Alternator	Engine Diagn. Results
Light Drimmer	Electr. Steering	Idle Speed control	Service Reminders
Traction Control	Multiplex Wiring	Turbo Control	Miles to Empty
Antiskid Braking	Module to Module	Emission System	Shift Indicator
Window Control	Communications	Transmiss. Control	Head-up Display
Memory Seat	Load Sensit. Braking	Diagnostics	CRT Display
Heasted Windshield	Hard/Soft Ride Control		Audio Annunciator
Voice Controlled Trunk			
Airbag Restraints			

Figure 2: Alternator regulator evolution.

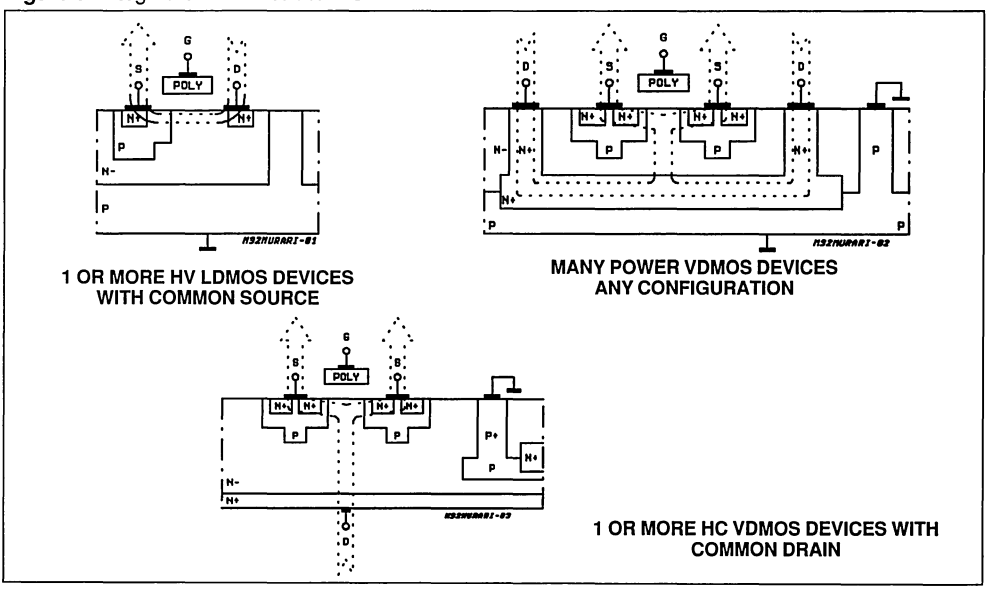


TECHNOLOGY OVERVIEW

Over the years SGS-THOMSON has developed various technologies that allow the realization of smart power circuits. The simplest way to classify these technologies is to refer to the process type, which can be purely bipolar or mixed, that is, including on a single piece of silicon both MOS structures (of control and power) and bipolar structures.

Another method (figure 3) is to examine the way in which the current flows through the power section; horizontal, with the current entering and leaving through the upper surface, or vertical, where the current enters through the upper surface and leaves through the lower surface; for this lower connection, instead of wire, the tie bar of the package is used.

Figure 3: Integrated DMOS structures.



MULTIPOWER BCD/60 vs. BCD60II

	BCD20/60	BCD60II
Junction isolation	down	up and down
Field oxide	Tapered oxide	Locos + field implant
VDMOS R on* Area (Ω*mm^2)	0.9	0.5
LDMOS R on* Area (Ω*mm^2)	0.6	0.25
CMOS tr. density (mm^{-2})	650	1500
CMOS thres. voltage (V)	1.3	1
min. NPN area (mil^2)	11	4
min. PNP area (mil^2)	15	5
Number of masks	12/14	13/15

The choice of one technology rather than another depends on various elements. By simplifying as far as possible the criteria, we can say that vertical technologies can guarantee, for a given area, lower resistances but they have the limitation of being able to include just one power device per circuit (or more than one, but always with the collectors or drains short-circuited). Horizontal technologies instead make it possible to have power structures that are completely independent. It is therefore evident that a vertical technology will give excellent results in the design of a light switch, while a horizontal technology will be equally well suited to the design of a multiple actuator.

Finally we have to underline that the continuous evolution of the silicon technologies has already made available, for the design activity, second generation processes, offering to the user both higher component density in the signal section and higher current density in the power area, so that in some cases the limit to achieve very low values of resistance does not come from the silicon, but from the bonding wires. An example of comparison between a first generation smart power technology - today in full industrial production - and a second generation one - today available for new designs - is given in Table 1: the way is open to processes that will allow the design - on the same chip-actuators - of several amperes together with microcontroller of not negligible power.

It is important at this point to underline that a smart power circuit does not consist of just silicon technology, but relies heavily on package technology. In fact it is well known that a signal device is bonded using gold wires with a diameter of 25 microns; however, gold wires can be used effectively up to diameters of 50 microns, which allows reliable operations with currents up to 2A, provided that the wire is surrounded by resin (the current capacity drops by 50% for wires in free air - that is, in the case of hermetic packages).

Figure 4: Mixed bonding technology.

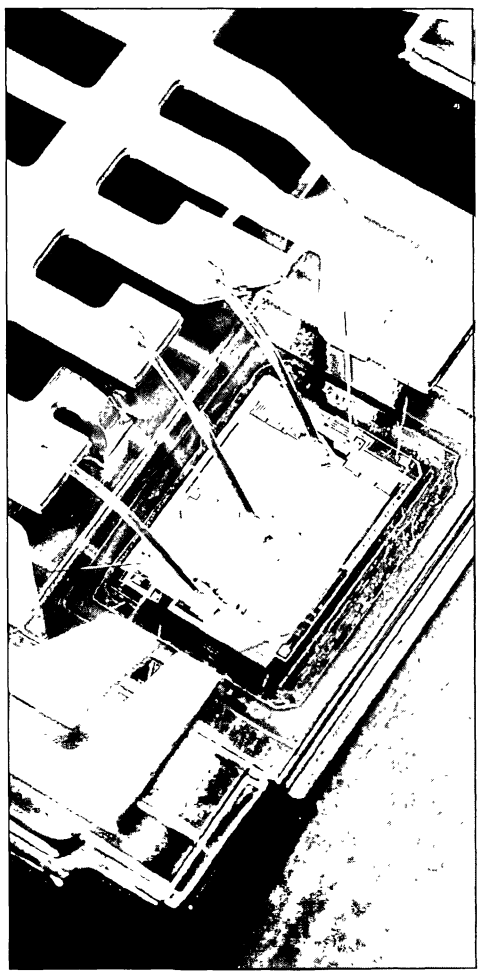
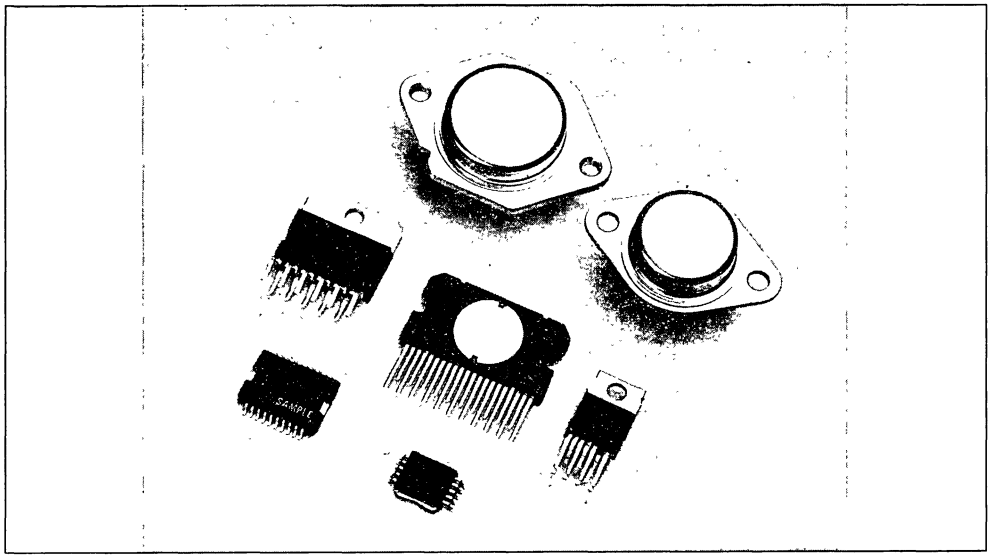


Figure 5: Power packages.



When, however, one has to deal with very high currents (more than 5A in single-point injection actuators, and more than 10A for window lift motors) gold wires are no longer suitable for obvious cost reasons so it is necessary to turn to aluminum wires with a diameter from 180 microns to 375 microns; clearly in this case it will be necessary to have adequately dimensioned bonding pads on the die, with a significant waste of silicon area.

Optimization is obtained with a mixed bonding technology where signal pads are bonded with thin gold wires and power pads with thick aluminum wires (figure 4). A further optimization is obtained by orienting the pads in the pad-to-bond-post direction.

Finally, another key area for a real industrial implementation of a smart power device is packaging; SGS-Thomson has a reputation of unparalleled excellence in the development and in the production of packaging techniques to meet power dissipation even in the presence of high pin count, and several innovative SGS-Thomson packages have been adopted as worldwide industry standards; in Figure 5 several types are displayed, including hermetic metal can, particularly suitable for components, such as the alternator regulators, that have to operate at a rather high temperature, with junction temperature that may exceed 150°C, in an extremely severe environment, since the regulator is usually exposed to any kind of dangerous element, such as grease, sand, dust, salt water and so on. A quite original power package for surface mounting, combining a low $R_{th\ j\text{-}case}$ (less than 3°C) with a small geometry, is under development in our laboratory.

THREE EXAMPLES

THE ALTERNATOR REGULATOR.

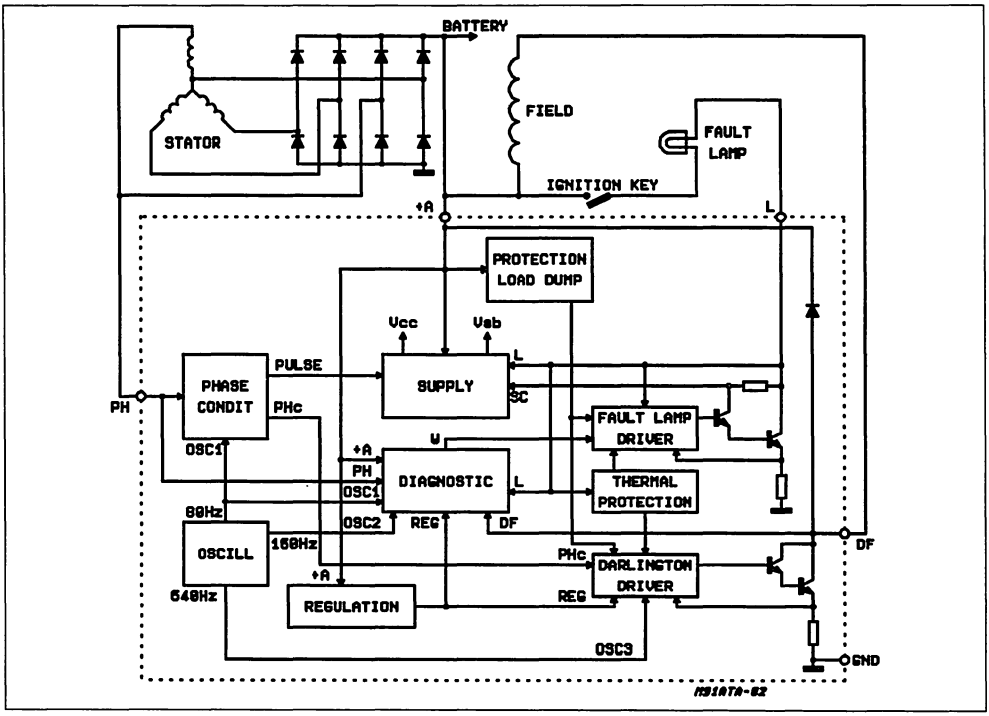
We have already briefly mentioned the evolution of the alternator regulator, but it is worth covering with some more details the history of this function.

Since the simple realization of so-called monofunction regulators by means of discrete components - diodes, transistors and resistors - the progress of the technology allowed the design of a monolithic component, still monofunction: in parallel, to provide the driver with more information about the status of the charging function, multifunction regulators were designed, but the power remained external, on a separate component.

A further improvement came with the assembly technology on a ceramic substrate, housed in a single package, but still several chips of silicon were needed.

Now SGS-Thomson has reached the maximum level of integration by designing a monolithic multifunction regulator and offering to the customer a device that minimizes the assembly operations and maximizes the reliability because of the single piece of silicon and the minimum number of connections between the silicon itself and the rest of the system: nevertheless the accuracy of the regulation and the number of possible malfunctions monitored by the circuit are well above what offered so far by the market.

Figure 6: Block diagram of alternator regulator.



The main characteristics of the device are summarized in Table 2 and the block diagram of the circuit is displayed in Figure 6.

The choice of the technology required a particular care and was driven by the following factors:

1)A circuit for the regulation of the alternator voltage, even if equipped with a complex diagnostic, is however a circuit where the power section, including the field drive in low side configuration and the free wheeling diode plus a big active zener diode, takes a significant share - about one third of the total, (see Figure7); therefore a bipolar process has been selected.

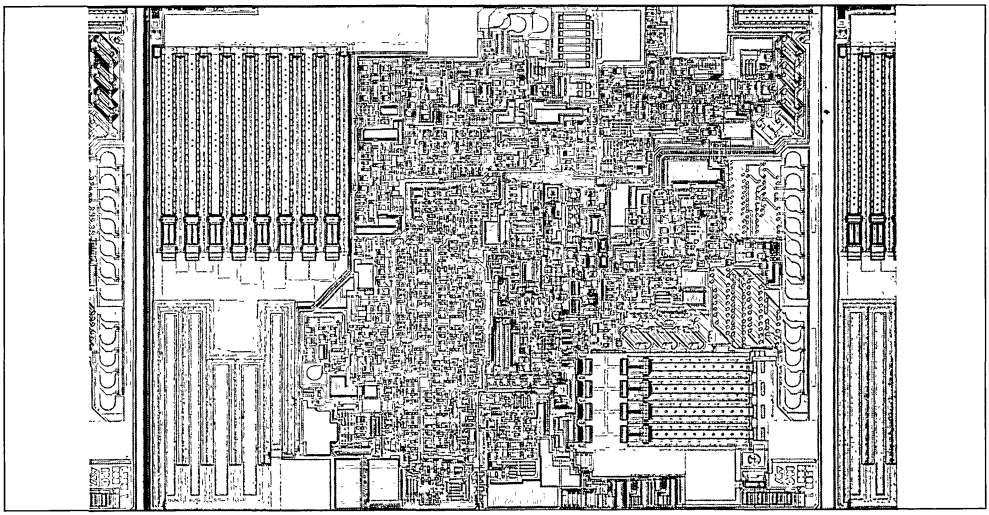
2)On the other side, about 600 small signal devices had to be integrated, and because of that a technology with a good intensity was mandatory, otherwise the total economy of the program would have been affected.

3)Finally an alternator regulator must be able to withstand very severe voltage transients, as fixed by ISO 7637/1, with voltages up to 270V and energy up to 50 joule, that arise on the car electrical network, for instance, if a sudden misconnection of the alternator occurs.

Table 2: MONOLITHIC ALTERNATOR REGULATOR

- Low side configuration
- No external component
- Accuracy on regulated voltage better than 1%
- Precise temperature coefficient
- Self-oscillating analog regulation loop
- Minimized field current at alternator stopped (500 mA max)
- Maximum field current trimmed at 5A, with 1.5V saturation voltage
- Full Diagnostic: alternator stopped
  Broken belt
  Extravoltage
  Broken wire alternator-battery
- Protected against short circuit (current limitation and thermal shutdown)
- Protected against short circuit of fault lamp driver
- Protected against extravoltages according to ISO 7637/1

Figure 7: Die of the alternator regulator.



Considering all of the above, SGS-Thomson has selected a high voltage process, internally named BSOII, fully bipolar, horizontal, with lithography of 3μm, and more than 100V of breakdown voltage in the VCBO condition.

The device is encapsulated in an hermetic package, TO-3 multileads, with bonding wires of 5 mils, able to carry continuous current up to 7 amperes (see again Figure 7).

THE PEAK & HOLD INJECTOR DRIVER

Let us now consider the U140, another component designed by SGS-Thomson to make available to the user a complex function on a simple chip; it is an actuator to drive in low side configuration the fuel injector in "single point" injection system.

As it is well known, quite essential for a good efficiency of the injection system is the capability to fix in the best way the time while the injector is opened, since that time is directly proportional to

Figure 8: Injector driver.

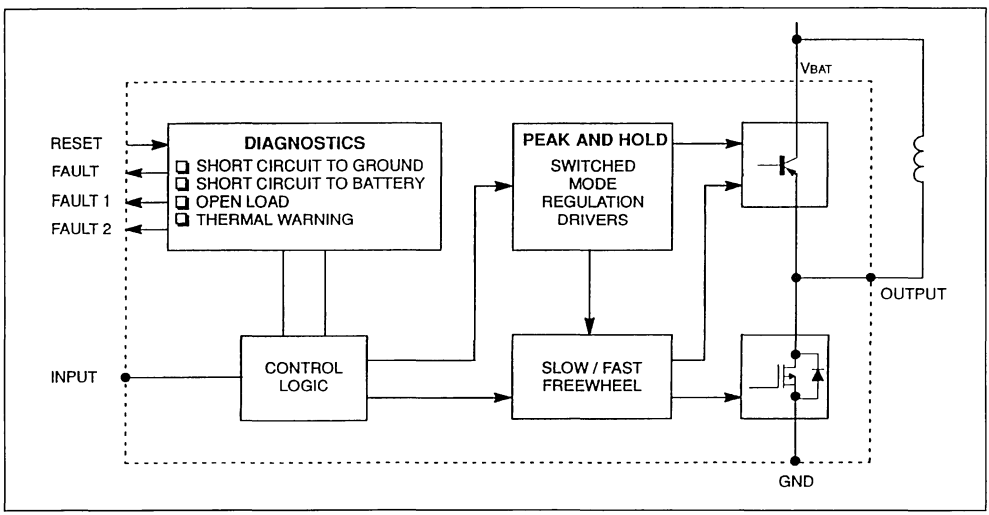
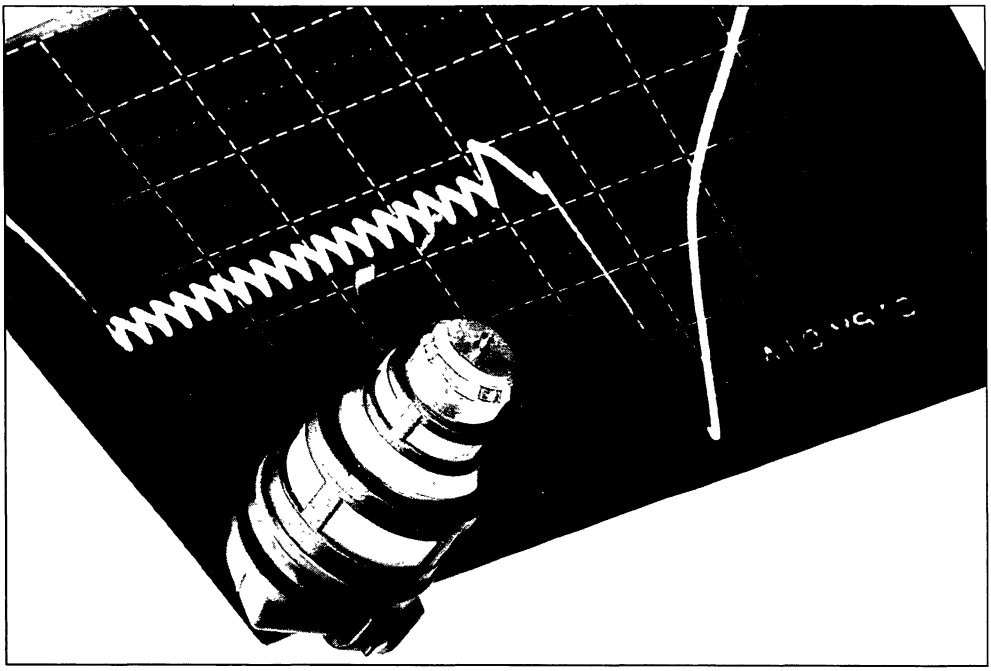


Figure 9: The injector drive is totally autonomous in fixing the current levels in the different phases, as well as the sampling of the holding current.



the quantity of fuel transferred to the intake manifold.

Particularly important to fix the fuel volume are the opening and the closing time of the nozzle, since both must be extremely fast; now, a single point injector needs a consistent current in the opening phase - up to 5A at the "PEAK" - but once opened, less current is enough to maintain the status - "HOLD" -. At the end of the cycle, finally the driving current must be switched off in a time as short as possible. The U140 meets all the above mentioned requirements: in addition, in the "HOLD" phase a further reduction of the current is achieved by switching on and off the driver stage (Figure 8), so reducing the power consumption and, as a consequence, the junction temperature.

A special mention shall be paid to the transition from "HOLD" to the "OFF" condition; as already said, it is quite important to reduce as much as possible this time; in the U140 that is achieved by discharging the inductor through an active zener set at a quite high voltage (about 70V), and that guarantees the closing of the injector in less than 50 sec. The same diode is set at 3V in the HOLD time. No external component is required by this circuit, that interfaces directly the microcontroller of the engine management system; by the way, the microntroller has just to fix the start and the end of the injection time, since the U140 is totally autonomous in fixing the current levels in the different phases, as well as the sampling of the holding current. (Figure 9).

The device incorporates a very sophisticated diagnostic (see again Figure 8), and transfers to the microcontroller all the relevant information on the status of the load.

The advantages of this monolithic devices are quite evident, if compared with existing solutions which need not less than 15 components including at least one IC and two discrete transistors, but are not limited to cost and room reduction, and to a consistent increase of the reliability: as a matter of fact the monolithic design allows to get, practically at zero cost, a very accurate value of the voltage of the recirculation diode, improving the accuracy on the ON time of the injector, and, last but not least, a diagnostic covering all the possible failure modes of the load.

The circuit is realized with SGS-Thomson's BCD technology, a mixed process including Bipolar, CMOS, and DMOS structures on the same chip; the input section is therefore able to interface directly a microcontroller, and the low side driver is designed with a DMOS having an R_{DSON} of less than 0.5 ohm. As already explained the recirculation diode is set at 70 volt in the transition from HOLD to OFF; because of that we selected the

Table 3: MONOLITHIC PEAK AND HOLD INJECTOR DRIVER

- Low side configuration
- Peak current function of battery voltage to provide a constant charging time
- Fast recirculation voltage independent from battery voltage
- Slow recirculation at max 3V
- Off time and peak current in hold condition internally fixed
- Full diagnostic: - open load
  - short circuit to ground and battery
  - thermal warning

BCD100, an option with a minimum breakdown Drain-Source voltage of 100V.

All the main features of this innovative device are listed in Table 3.

REARVIEW MIRROR DRIVING

While we are on the subject of higher levels of integration it is useful to mention the development of circuits for the multiplex wiring system, which replaces conventional cabling with a common bus and "intelligent" switches.

The intelligent switch circuits are key components for the multiplex system, and one of these is a multiple driver IC,the L9946, developed by SGS-THOMSON for rearview mirror driving applications.

This IC integrates all of the control functions and power circuits needed in the electronic external rear-view mirror unit now being adopted for high end cars and is the first chip to integrate these functions. (see Figure 10).

An important feature is that the IC is controlled directly by a microprocessor — all of the possible drive conditions are controlled by loading 4-bit commands and the L9946 generates the appropriate motor control signals.

No external power circuits are needed because the L9946 drives directly the two motors used for mirror orientation (µp/down and left/right), the motor that "folds" the mirror for maneuvering and the demister heating element. In a typical application the chip is used in multiplex door wiring system where the door is connected to the body by three wires and all door functions controlled remotely using smart chips.

Inside the chip are four DMOS half bridge power stages which drive the three bidirectional DC motors, plus a DMOS high side driver that drives the demister element. Control logic integrated on the chip decides how these transistors are to be

Figure 10: Block Diagram of the L9946.

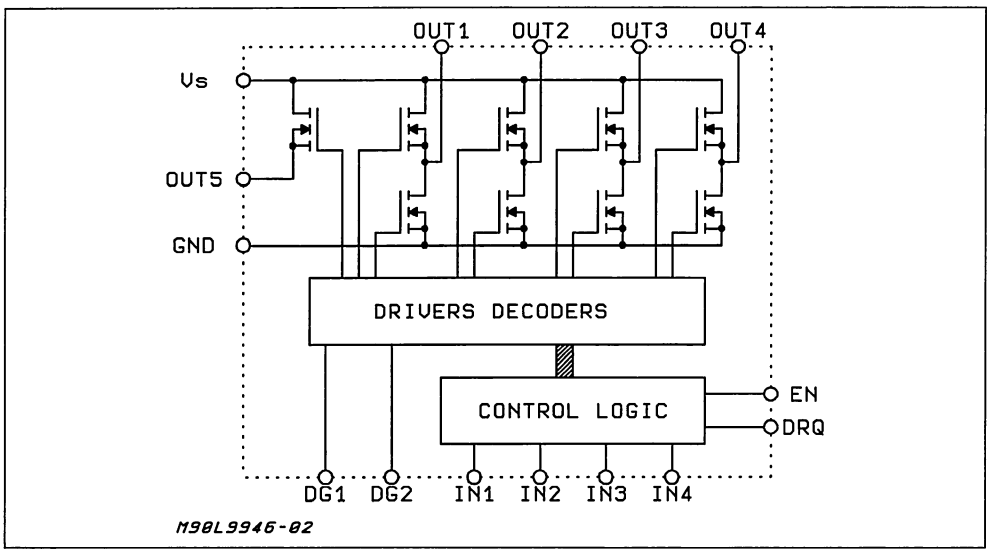


Table 4: MULTIPLE HALF-BRIDGE DRIVER

- 4.75A TOTAL OUTPUT CURRENT
- VERY LOW CONSUMPTION IN OFF STATE
- OVERLOAD DIAGNOSTIC
- OPEN LOAD DIAGNOSTIC
- GROUNDED CASE

switched to achieve the desired motion — including rapid braking. Two of the half bridges are rated at 1A output current; the other two half bridges and the high side driver are capable of delivering up to 4.75A.

In common with many other dedicated automotive ICs the L9946 incorporates diagnostic functions. Conditions such as overload and open load are signalled to the control micro so that appropriate action can be taken. In addition there is a standby pin that allows the micro to put the L9946 into a dormant state when it is not needed.

CONCLUSIONS

We think we have demonstrated that the industrial availability of processes capable to match, on the same silicon, high power and complex control functions is the key element to the integration of completed functions on a single chip of silicon. The examples described demonstrate that SGS-Thomson has developed a technology portfolio that can offer different answers for different applications, always optimizing the trade-off among the various needs.

On the other side, all the above considerations would have a merely academic interest if they were not associated with a convenient cost. It is clear that the monolithic integration of complex functions implies the use of not negligible areas of silicon, and that even in presence of high density processes.

It is therefore important to devote adequate resources to the diffusion technique, to increase the yield of each process.

Today's chips, up to 30mm^2 (and all the thee examples are below that limit) can be produced at prices competitive with an equivalent discrete solution, and in the second half of the 90's the target will be expanded up to areas of 40mm^2, giving a green light to the monolithic design of complete modules.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

HIGH CURRENT MOTOR DRIVER ICs BRING AUTOMOTIVE MULTIPLEX CLOSER

by Riccardo Ferrari & Sandro Storti

Smart power ICs delivering up to 25A complete the family of power components needed in automotive multiplex systems, making it possible to drive even a windowlift motor directly. With these ICs the large-scale adoption of partial multiplex schemes moves much closer.

One of the essential prerequisites for the large-scale introduction of multiplex wiring systems for vehicles is the availability of high power ICs capable of driving lamps, motors, solenoids and relays. These ICs must be able to survive in an exceptionally hostile environment, they must be highly reliable and — since so many are needed in each vehicle — they must be inexpensive.

Many power ICs suitable for this emerging market have already been introduced, but a gap was left at the high current end of the range, where ICs delivering 20A or more are needed to drive loads like windowlift motors.

Today SGS-THOMSON has filled this gap with new power ICs that exploit technologies that make it possible to build very high current ICs that are both reliable and economical. Two such ICs are the L9936 half-bridge motor driver and the L9937 full bridge motor driver.

The L9936 (figure 1a) contains a half-bridge circuit capable of delivering 20A dc current, which is sufficient to drive directly a windowlift motor. Since the motor is bidirectional two of these devices are used to make a complete drive stage. Designed for lighter loads, the L9937 (figure 1b) contains a full bridge delivering up to 6A continuous (12A peak for starting). A single L9937 device drives a bidirectional dc motor.

Figure 1a: Capable of delivering 25A, the L9936 half bridge driver is a smart power IC suitable for driving windowlift motors in automotive multiplex wiring systems.

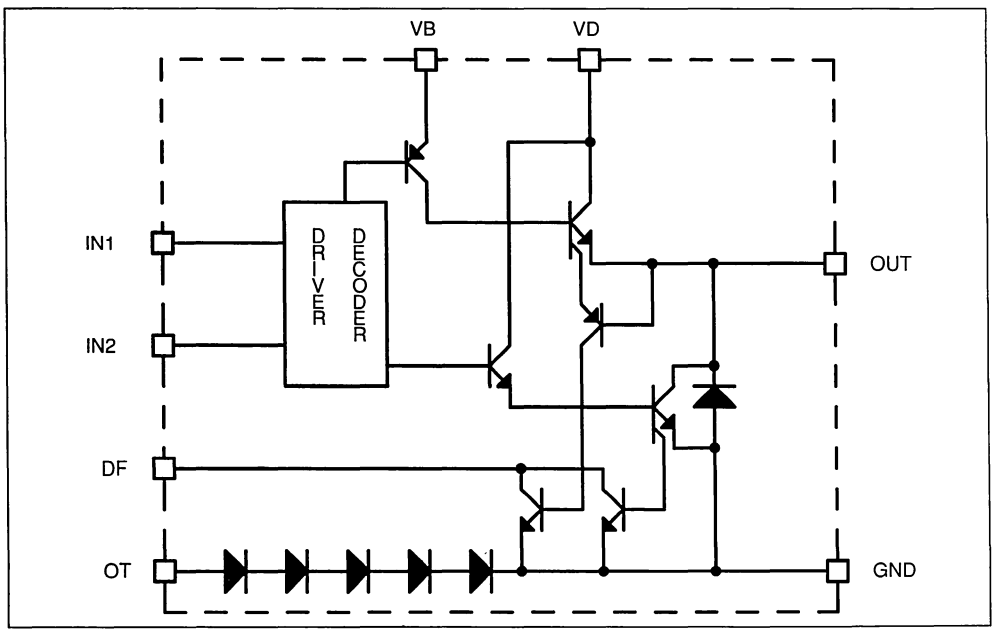
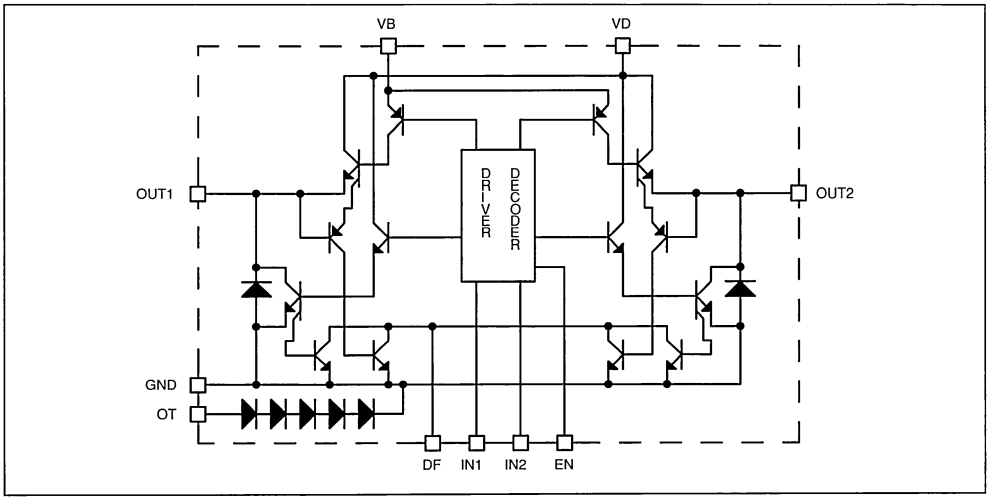


Figure 1b: A full bridge driver, the L9937 delivers 6A (10A peak) and is used in motor driving applications such as doorlock driving.



Both of these ICs are fabricated using an enhanced bipolar power process and a new mixed bonding technology. Bipolar technology has been adopted for these circuits — rather than the "BCD" mixed bipolar/CMOS/DMOS technology used for other multiplex switches — for several reasons. First of all, when very high currents are involved the resistance of the silicon is no longer dominant — half of the series resistance is caused by the metallization tracks on the surface of the chip and the bonding wires. Consequently there is nothing to be gained by using DMOS technology to further reduce the output transistor resistance. Figure 2 shows the contributions to the saturation resistance of a power NPN transistor in the BHP20 process used for these ICs. The use of thick metal (6 microns) significantly reduces voltage drop with high load currents in this technology.

Another reason for using bipolar technology is that the substrate currents generated in the substrate when 20A load current recirculates would affect low-level CMOS logic. In the L9936 and L9937 high-level bipolar logic is used in the control stages to avoid this danger, giving excellent noise immunity. Interfacing to this high-level logic

AUTOMOTIVE MULTIPLEX WIRING SYSTEMS

Multiplex wiring is the system where a conventional wiring harness is replaced partly or completely by a single, common bus which carries power and control signals throughout the vehicle. Each load is equipped with an electronic switch that recognizes commands on the control bus and returns status information.

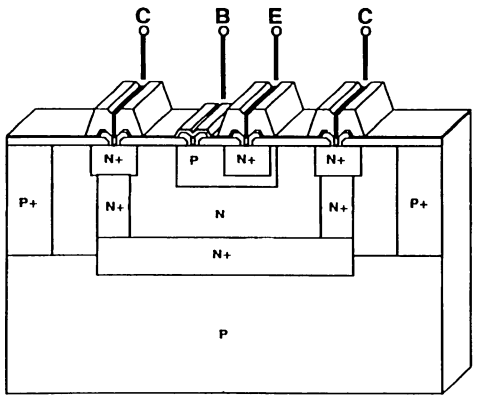
There are many different standards for the multiplex bus, of which the simplest is a three-wire scheme having one wire for the battery, one for control data and a common ground. Extra wires are sometimes added for more reliable transmission.

In a typical operation sequence, such as turning on a lamp, the control switch will cause a suitable command to be transmitted on the bus. The smart switch controlling the lamp will recognize the command and attempt to turn on the lamp. A signal indicating successful or unsuccessful completion is then returned on the bus.

Advantages of multiplex wiring are weight reduction, easier assembly, greater reliability and simpler fault diagnosis & repair. The simplicity of multiplex wiring is particularly important in critical points such as the connection between the driver's door and the rest of the body; in one case 27 wires were reduced to just three by the adoption of a multiplex subsystem.

Crucial to the success of multiplex wiring is the availability of electronic switches that can guarantee the necessary reliability and performance. Multiplex wiring is already used in small scale trials and will be adopted on volume produced vehicles in 1991.

Figure 2: In very high current ICs the voltage drop of the metallization and the bonding wires becomes significant. This example, a power transistor realized with the BHP20 process (used for the L9936 and L9937) indicates typical values. Because of this problem it is more important to optimize the metal resistances than that of the silicon.



POWER NPN
ISOLATED AREA = 5.7 mm²

MAXIMUM CURRENT = 20A
R_{SAT} = 30 mΩ

CONTRIBUTION TO R_{SAT}:
- **WIRES 6 mΩ**
- **METAL 10 mΩ**
- **SILICON 14 mΩ**

THIS IS OBTAINED BY:
- **USING DOUBLE METAL THICKNESS (0.7 + 5 μm)**

is performed in the bus interface chip which will be placed between the L9936/7 and the multiplex bus. Since these interface chips are system dependent they are always developed for a specific application, rather than being standard parts like the power ICs.

The mixed wire bonding technology used in the new ICs is clearly visible in the photo, figure 3. Because of the high current it is not possible to use the standard thin gold wires employed in

Figure 3: The mixed bonding technology used in the L9936 — shown here after bonding but before encapsulation — reconciles the conflicting requirements of current and silicon area. Thick aluminum wires are used for the power connections; thin gold wires for the signal connections.

standard ICs. Thick gold wires are out of the question, partly because of cost, but also because they are too rigid to bond to the chip without damaging it.

One alternative, widely used in simple power ICs, is to use thick aluminum wires. However, a thick aluminum bonding wire needs a large bonding pad on the die. In a simple device like a 3-terminal regulator this is not a problem because there are few such pads, but for more complex ICs with eight or more connections the wasted silicon area would be excessive.

Another alternative, still used by some companies, is to use two or more thin gold wires in parallel for each power connection. This solution, however, is costly because more gold wire is needed and it is prone to reliability problems because it is extremely difficult to verify each bond. Moreover, for the currents used in multiplex applications so many parallel wires would be needed this method would be totally impractical.

SGS-THOMSON has developed and industrialized a different solution: a mixed bonding technology where thin gold wires (50um) are used for signal connections and thick aluminum wires (250um) are used for power connections. The two bonding wire types can be clearly seen in figure 3. Note also that the bonding pads for the aluminum wires are oriented in the direction of the wire to avoid needless waste of silicon area.

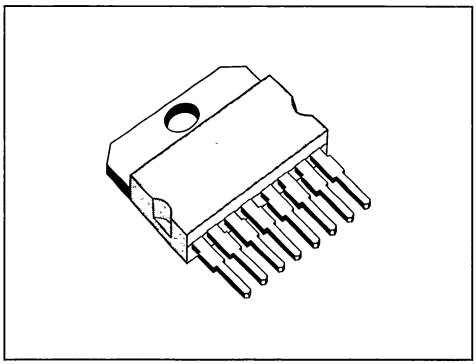
Because gold and aluminum are bonded using different techniques this has necessitated a two-step bonding operation. Moreover, because of the combination of different bonding metals the leadframe has to be plated with a special gold alloy. This plating is selective, being applied only to the bond area, partly for economy and partly to avoid gold on the external leads, which could contaminate soldering baths, causing reliability problems on PC boards.

Different bonding techniques are used to weld the two types of wire to the surface of the chip. For the thin gold wires the thermosonic method is used where an electric discharge first creates a small ball on the free end of the wire; this ball is then pressed onto the bonding pad and vibrated rapidly (in the ultrasonic range), causing the gold ball and silicon surface to weld together.

The thicker aluminum wires are bonded using the simpler ultrasonic method, where the wire is simply pressed onto the surface of the chip then vibrated rapidly to weld the wires to the pad. Because more vigorous vibrations are used in this technique the aluminum wires are bonded first, followed by the gold wires.

To guarantee automotive-level reliability the bonds are pull tested on a sample of parts. In this test the wires are pulled to determine their breaking strength. Gold wires must resist a force of at least 15g; aluminum wires must resist a pull of 130g. Moreover, the wire must break leaving the bonds intact — if a bond detaches before the wire breaks the part fails the test.

Figure 4: After molding and cropping the finished part looks like this. This eight-lead version of the Multiwatt package — first developed by SGS-THOMSON in 1979 — has wider lead spacing to suit the large high current PCB tracks.



The L9936 is housed in a new eight-lead version of the successful Multiwatt package, originally developed by SGS-THOMSON in 1979 (figure 4). This version has eight leads in line at 0.1" centers, rather than the usual two rows of leads. This makes the Multiwatt-8 package suitable for very high current devices where wide PCB tracks are needed. An 11-lead Multiwatt package is used for the L9937.

The new package also has a larger die flag — to accommodate today's large chip sizes — which has necessitated the addition of new antistress features in the frame design. These features ensure a dependable adhesion between frame and resin — essential for humidity resistance — and isolate the die flag mechanically from the external tab to ensure that the die is not damaged if the tab is deformed during mounting.

In a typical application both the L9936 and L9937 are used with a customer specific interface chip which handles bus interface and protocol handling functions. Two different approaches at the system level are used today (figure 5). In the first case each load has its own interface, connected directly to the multiplex bus. An alternative is to combines several load units into a single module; this approach is very attractive in situations like door multiplex where there is a high concentration of loads in a distinct and fairly compact assembly.

Figure 6 shows a generic door multiplex solution of the second type, illustrating the role of the new high current bipolar driver ICs. In this example an L9937 drives the door lock motor, two L9936's drive the windowlift motor, a VN02 high side

driver IC drives a hazard warning light (the light on the edge of the door that turns on whenever the door is opened) and an L9946 multiple half-bridge IC drives the three rear-view mirror motors (two for mirror adjustment and one for "folding" of the whole mirror unit for car washes and so on) and the mirror de-icing heater. All of these integrated circuits are available today.

Pure bipolar technology is used only for the very high current ICs. For all of the other parts a mixed bipolar+CMOS+DMOS technology has been chosen because of the higher efficiency of DMOS power stages and because it allows the integration of complex parts. The L9946 multiple half bridge, for example, has a four high power half bridges plus a microprocessor interface all on the

Figure 5: Two approaches are being used for multiplex systems. In the first each load has its own bus interface; in the second loads are grouped together and share a common electronics module. This approach is used in door multiplex systems, where the loads are all close together and multiplex wiring used primarily to reduce the number of wires passing from the body to the door.

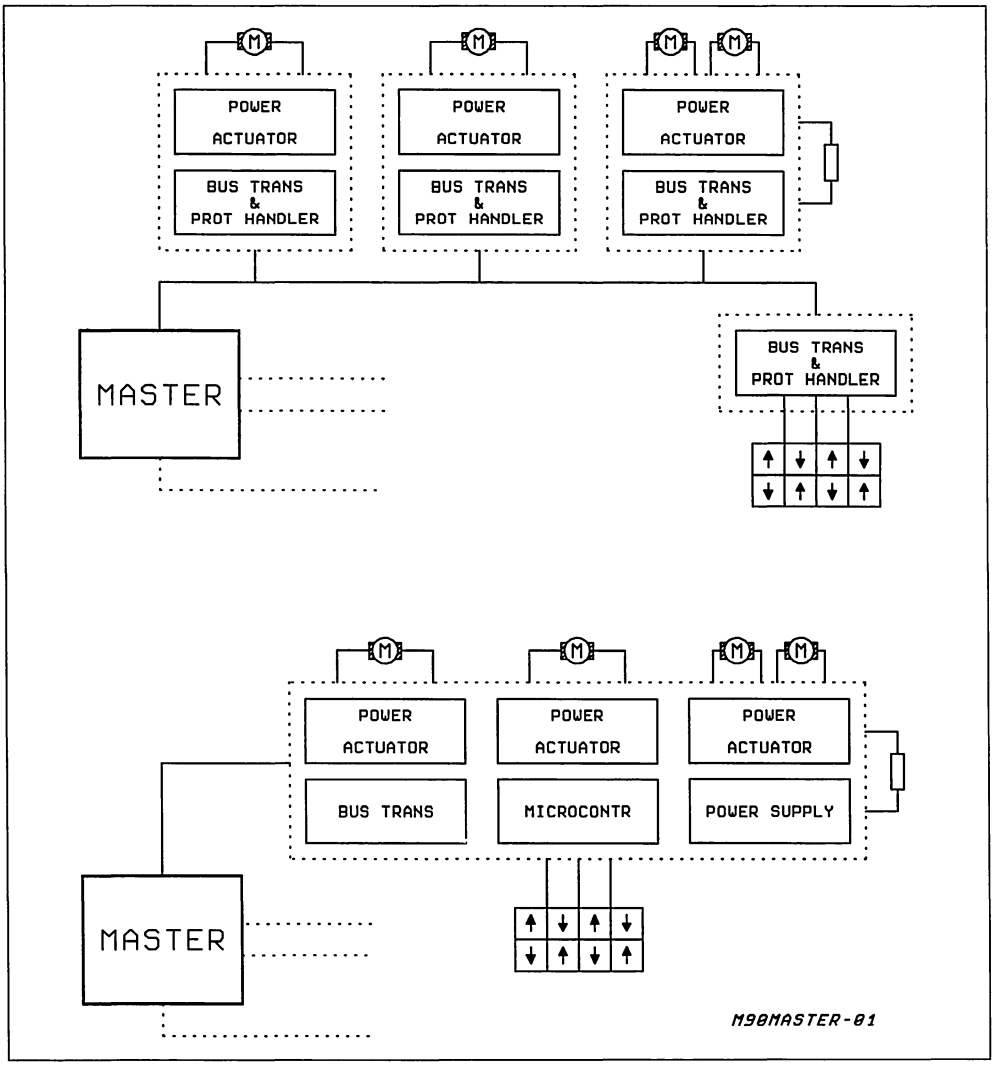
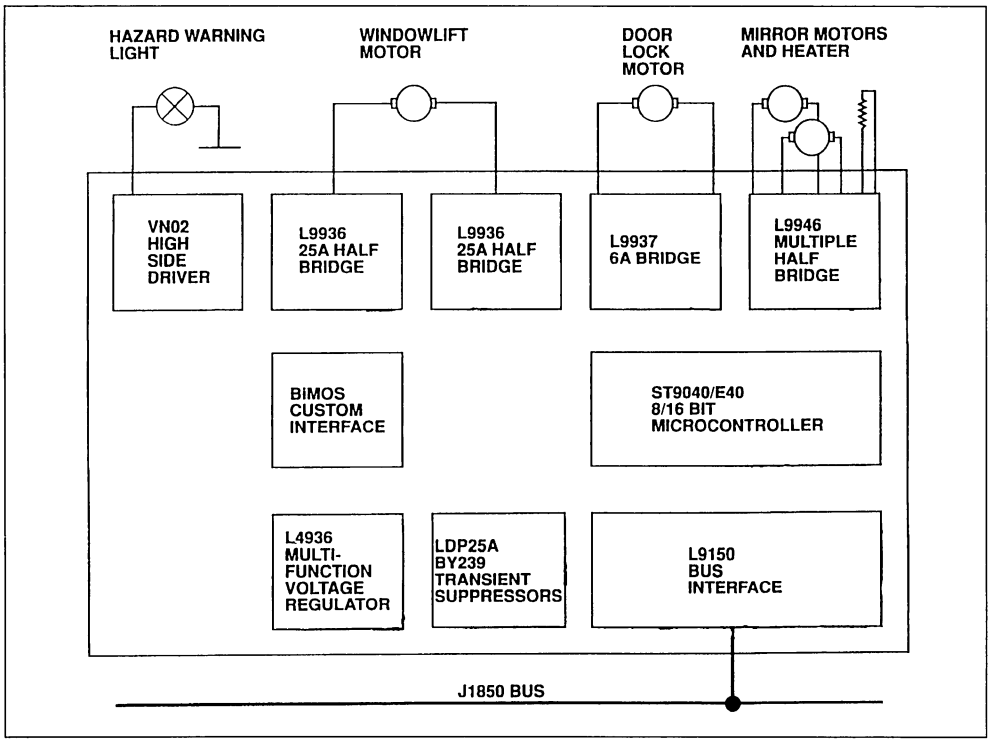


Figure 6: A typical door multiplex solution will use a mixture of high current bipolar power ICs and BCD power ICs. Solutions of this type will be on production models in 1991.



same chip.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

A SOLID STATE BLINKER FOR AUTOMOTIVE APPLICATIONS

by Sergio Ciscato

Using dedicated power ICs today it is possible to make a car blinker circuit without relays. The benefits are simpler cablinng and better reliability.

Present car direction indicator system generally use a dedicated integrated circuit as the SGS-THOMSON L9686 in conjunction with a relay to control the flashing of the lamps. A high current electromechanical switch is necessary to turn on the right or the left direction indicator lamps; to provide the emergency blinker feature a 3-pole power switch is needed too (see Fig. 1).
The first disadvantage of this system is the high number of power connections between the master module and the switches; in addition, the high currents flowing through the switches and across the relay contacts decrease their lifetime and consequently the reliability of the system.
Thanks to smart power devices is is possible to implement a solid state car direction indicator system (see Fig. 2), that solves these problems.

Figure 1: Traditional System

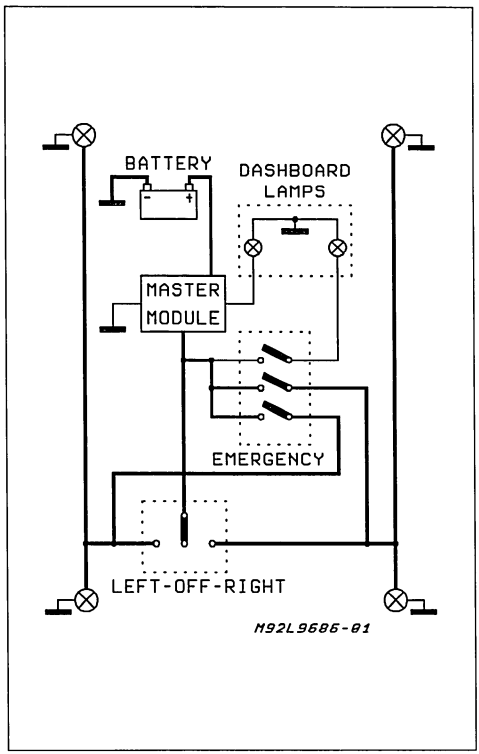
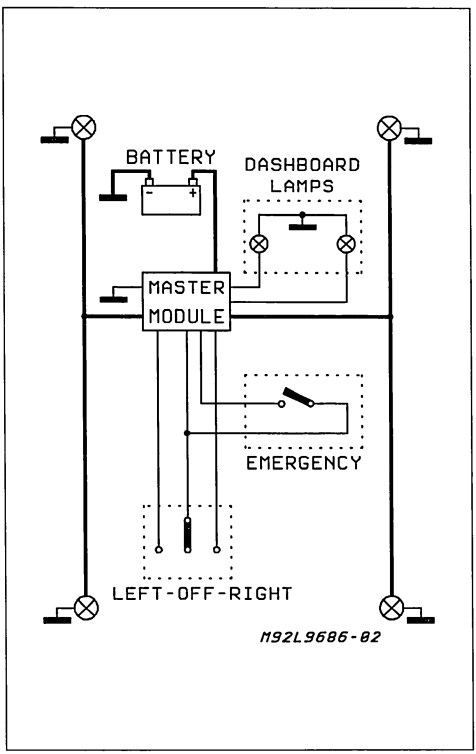


Figure 2: New Solid State System



CIRCUIT DESCRIPTION

The control device in the system described here is the L9686, but the relay is replaced by two L9821 High Side Drivers; this device delivers up to 25A peak output current with R_{ON} = 100mΩ, short circuits and thermal protection.

When a power devices is turned on, the local supply voltage can drop several volt below its nominal value because of the line inductance. This voltage drop could cause disturbances to the control logic that in some cases could produce undamped oscillations on the suplly line itself.
To avoid these oscillations and to prevent EMI disturbances, the L9821 was chosen as the power device in this applications because of a feature that limits the output current slew rate (di/dt) during the switching edges.
Fig. 3 and Fig. 4 show the rising and the falling edges of the output current of an L9821 device loaded with two 21W lamps; the current level in the first case is higher than in the second one because of the inrush current of the bulbs (see Fig. 5).

Figure 3: Rising Edge of the Output Current

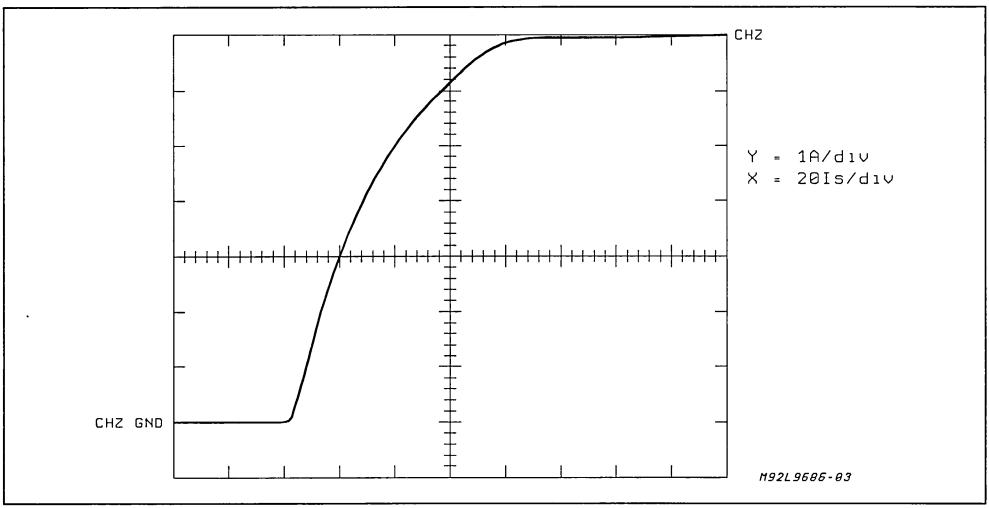


Figure 4: Falling Edge of the Output Current

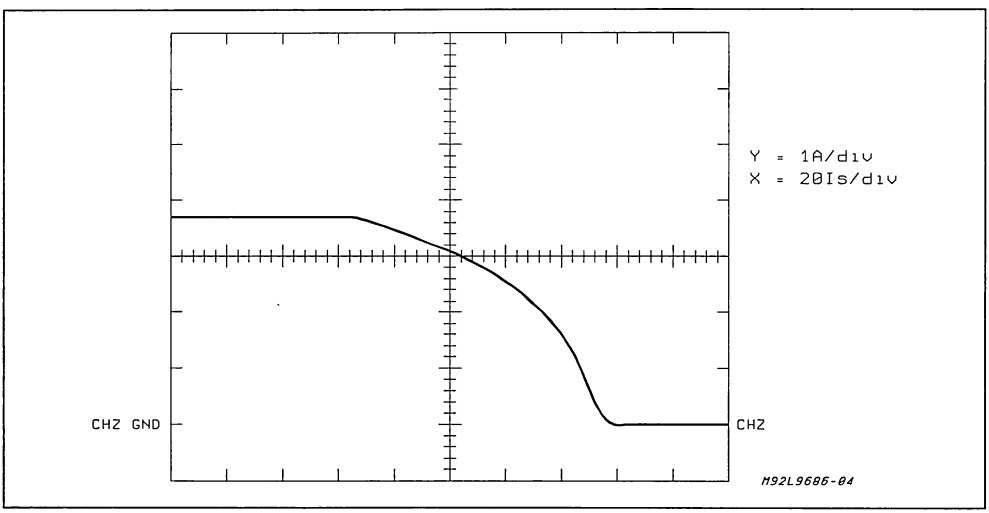


Figure 5: Output Current Waveform

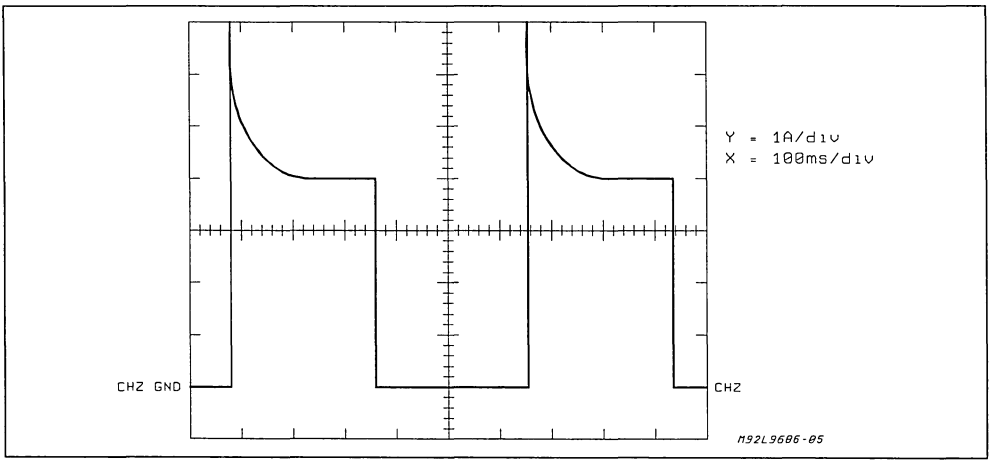


Fig. 6 shows the complete schematic diagram of the master module: when S1 is closed (left or right) the L9686's internal oscillator starts and pin 3 goes high; then the input voltage of one of the two L9821 devices goes high too, resulting in the lamps switching on. After a time equal to half of the oscillation period pin 3 of the L9686 returns low and the lamps are threfore switched off. The flashing cycle stops and the circuit is reset to the initial conditions when S1 is open.
The flashing frequency depends on the external RC networkR1 and C1 according to the following formula:

$$Fn = 1/ (1.5 \times R1 \times C1 \text{ (typ.)}$$

R3 and C2 provide hysteresis to avoid spurious switching of the oscillator comparator at every lamp turn on; this hysteresis is not necessary if the L9686 is used in conjunction with a relay, because of the relatively long delay time of this last one. Rshunt senses the current flowing in the right or the left lamps (depending on the S1 position): when one of the lamps is defective the voltage drop across R_{shunt} is reduced to a half and the failure is indicated by doubling the flashing frequency. S2 allows the emergency blinker function: when it is closed the L9686 device drives, through the diodes D1 and D2, both the L9821 smart switches and then both the right and the left lamps.

The emrgency blinker operation is monitored by the flashing of both the dashboard lamps L1 and L2 while in normal operation only L2 flashes.

OVERVOLTAGE PROTECTION

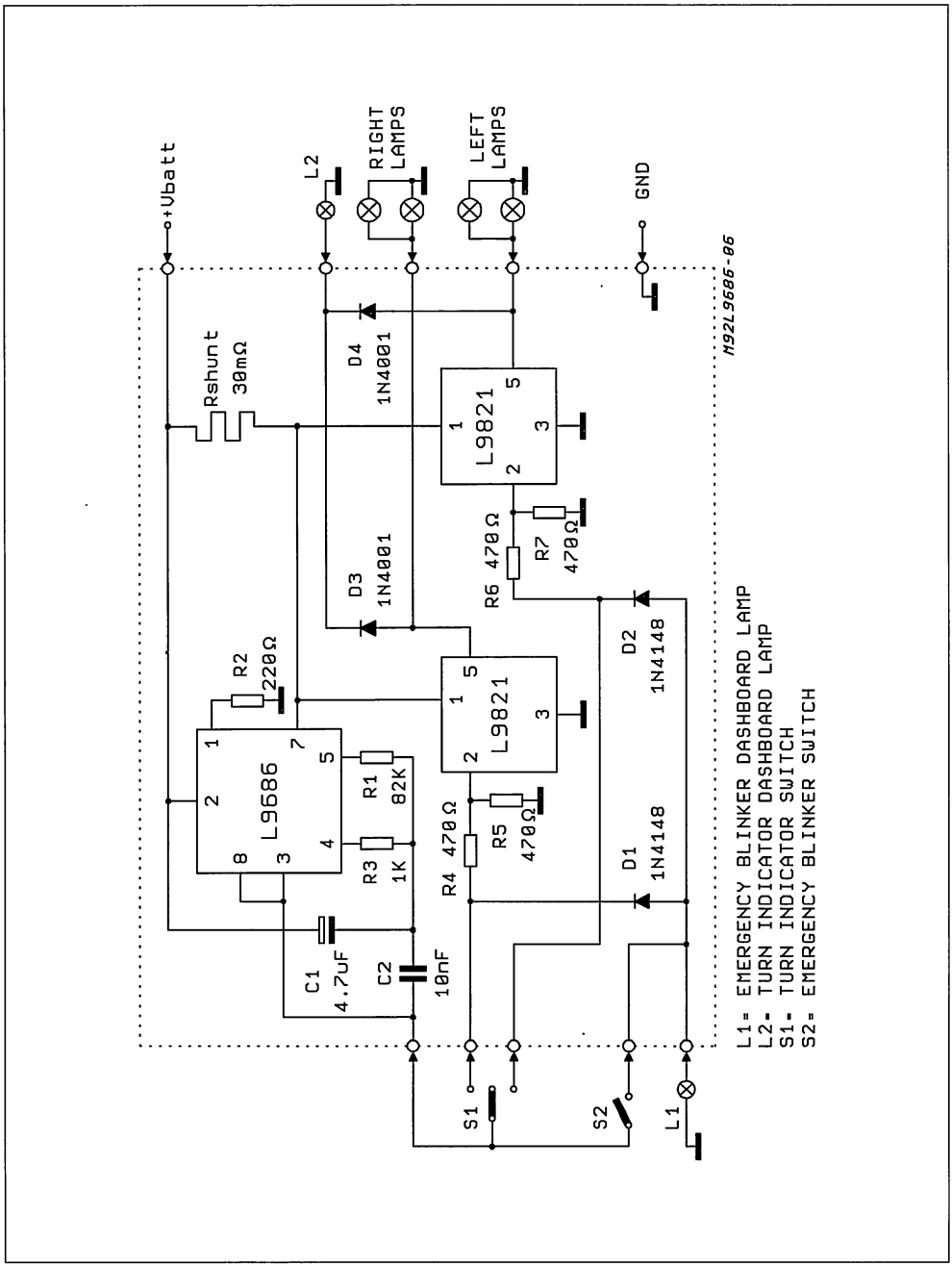
An L9821 device can withstand up to 60V load dump transient. If a centralized overvoltage protection is not provided on the alternator it is possible to increase the load dump capability of this application by placing a dedicated protection device, such as a Transil, between the supply voltage and the ground terminals. This transil must withstand the double battery, a condition often requested for the automotive equipment, so a good choice is a device with at least 26V breakdown voltage. The same protection device allows the described application to withstand all the other voltage transients. If a centralized load dump protection device is already present on the alternator a small protection zener diode is sufficient to clamp the low energy overvoltage transients due to the disconnection of the several loads in the car. In this case the breakdown voltage of the local protection device must be higher than the clamping voltage of the centralized diode.

ADVANTAGES

Fig. 2 shows a possible wiring diagram of the described system in a car; the master module has 10 connections, compared to the four of the conventional system showed in Fig. 1, but from the comparison between the two possibilities we can see some advantages:

- centralized wiring at the master module
- less power connections
- less power wire length
- no power switches
- no multipolar switch for the emergency blinker
- short circuit protection between the lamps and ground
- inrush current limiting of the smart switches increases the lamps lifetime

Figure 6: Schematic Diagram



REAR MIRRORS MULTIPLEXING USING L9946

by L. Valsecchi & S. Vergani

The application of the L9946 device in a real-world automotive multiplex system is described. After a brief introduction to the multiplex concept, the hardware and software key points are discussed. It turns out that L9946 is very well suited for this kind of relatively complex applications.

THE MULTIPLEX CONCEPT

In this section a brief introduction to the basic multiplex (MUX) concepts is given. Generally speaking, a MUX is composed by a number of units connected through a serial bus. There is a set of meaningful serial messages and each unit can recognise a subset of messages relevant to it. Once a relevant message is received, the unit performs an action according to the information contained in the message. Usually an acknowledge technique is used, so that a bidirectional information flow between units can be established. It is possible to draw a rough distinction between MUX systems based on the communication strategy. In increasing complexity order, a MUX can be classified as follows.

1) MASTER-SLAVE:

One unit is qualified as master unit, and it is the only one that can autonomously start a transmission. The other units (slaves) can transmit only after the reception of a message out of a defined set.

2) QUASI MULTI-MASTER:

As before, one unit acts like a master, but some slave units can start an autonomous transmission to the master. This happens usually when a significant event has occurred (e.g. a key has been pressed).However, the slave units cannot communicate each other directly. The messages flow is under the total control of the master unit.

3) MULTI-MASTER:

Every units can commuicate each other, and there is no more a well defined master unit.In fact, the control, at a given time, is owned by the unit currently autonomously transmitting.

The format of the serial messages, as well as the characteristics of the physical interface of the bus line are defined by a series of rules called the PROTOCOL SPECIFICATION. These rules also define in details the behaviour of the transmitting and receiving units when a situation of bus contention (i.e. when two units try to access the bus simultaneously) occurs.

The ISO (International Organization for Standardization) has standarized, at various levels, three protocols called CAN, VAN, J1850. This means that documents exist as a reference to achieve the compatibility between two systems using the same protocol.

In fact, especially for slow speed data bus, custom protocols have been developed.

There are definite advantages in using a MUX system in the automotive field. First, the number of wires required to perform the same functions is dramatically reduced. For example,with the MUX approach, to connect a keyboard unit to other units such as window lift motor control, rear mirror control etc., only three (or four if a differential bus is used) wires are required, independently of the number of keys or motors used. This leads to a reduction of costs of the harness of the vehicle.

Flexibility is another feature common to well designed multiplex systems.

The multiplex architecture allows a high degree of freedom in the choice of the physical location of the units inside the vehicle. For example, as long as the serial bus line is provided, a control keyboard can be placed indifferently in the door or on the dashboard without changing the vehicle wiring.

Furthermore, if a certain computational power (i.e. a microcontroller) is located in the peripheral units, the functional behaviour of the whole system can be defined by software so that upgrading and modification can be accomplished without changing the hardware.

Also, a sophisticated diagnostic strategy can be implemented. Usually one or more units collect diagnostic information that can be read by a tester connected to the system when a car technical assistance is required. Such a tester generally includes a menu driven diagnosis procedure, lead-

ing to easier fault detection and thus to shorter repair time.

REAR MIRRORS MULTIPLEX SYSTEM

INTRODUCTION

The application described here is an example of how the L9946 can be used as a mirror controller in a MUX system.

To explain in all the details a MUX system design is beyond the scope of this application note. However, the key points in hardware and software design will be discussed in depth.

GENERAL DESCRIPTION

This MUX is composed by a keyboard unit, a left mirror unit and a right mirror unit.

The electronics is intended to be placed inside the external rear mirror case, and inside the physical keyboard. To achieve this, when possible, devices available in small SO package have been chosen. In this way, using surface mounting technique, very compact PCB layout can be obtained.

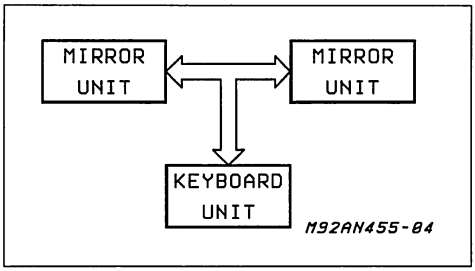
The three units are connected through a differential bus.

Including power supply line and ground return, only four connection wires are required, obtaining a substantial saving compared to the traditional solution, that requires eight wires.

The system block diagram is shown in fig. 1.

The functions implemented are:

Figure 1: System Block Diagram



- mirror plate movements
- open / fold
- wiper

The commands available are activated by 6 push buttons located in the keyboard unit.

An additional three-way selector allows to switch between the left or the right mirror. When this selector is in its central position, the only function available is a simultaneusly mirror open/fold movement.

MIRROR UNIT DESCRIPTION

The block diagram of the mirror unit is shown in fig. 2. The schematic diagram of the mirror unit is shown in fig. 3.
The only difference between the left and right mirror unit is the position of a jumper that configures the address of the unit.

Figure 2: Mirror Unit Block Diagram

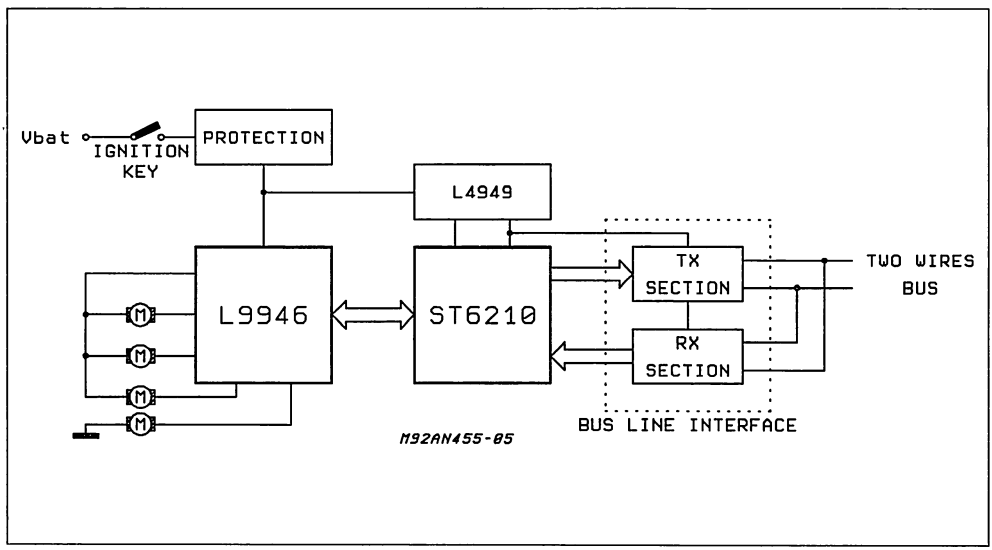
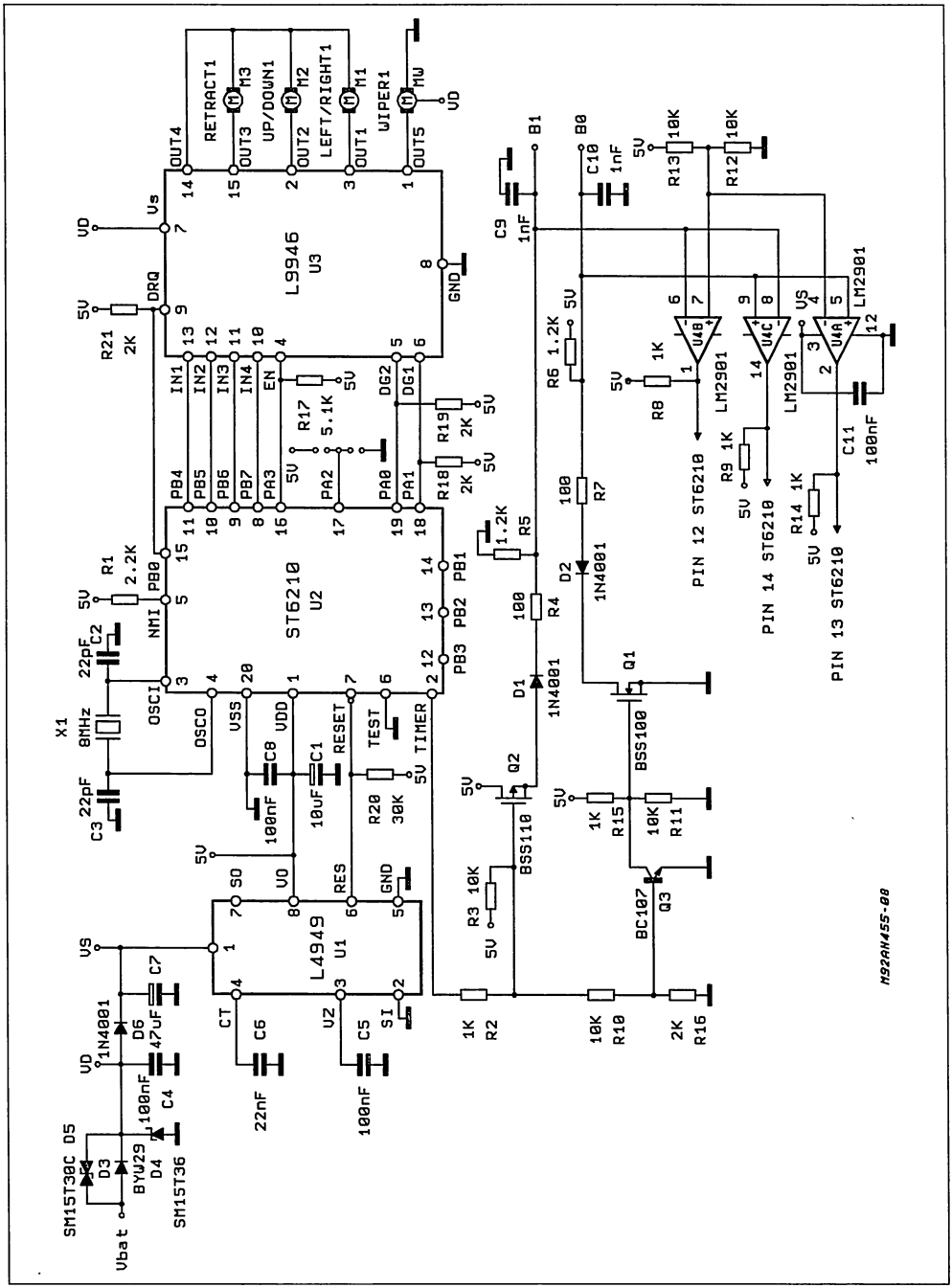


Figure 3: Mirror Unit Schematic Diagram.



In the following sections the main functional blocks are described.

Protections

The units must be protected against a number of possible anomalous voltages on the power supply line coming from the battery.

This anomalous conditions are:

1) Reverse battery

2) Load dump

3) Short negative spikes

Voltage Regulator (L4949)

This device provides the five volts necessary for the microcontroller and to the bus line interface. It also provides to the microcontroller the correct power on reset signal.

Microcontroller (ST6210)

The microcontroller (uC) choosen for this application is the ST6210 (1K8 EPRPOM, 64 bytes RAM).This is a 20 pin device, available in SO20 package. The ST6 family is intended for low-medium complexity applications.

The heaviest task for the uC in this, or similar, application is the protocol handling, i.e. the reception and the transmission of the serial messages on the bus.

Due to the low computational power and speed of this uC, the protocol was chosen to be relatively slow (3.3 kbits/sec) and the bit encoding was chosen in such a way that the decoding algorithm is tailored to optimize the hardware uC resource usage.

In this case the uC also drives the L9946 and protects it against overcurrent and/or overtemperature reading back the dignostic signals DG1 and DG2.

Mirror Actuator (L9946)

The L9946 in this application is used to drive the four mirror motors: two for the plate movements, one for the open/fold movement and one for the wiper motor. In this particular application the wiper can be driven by the high-side driver thanks to a mechanical solution built into the mirror that performs automatically the wiper alternative movement.

Bus Line Interface

This is the circuitry that realize the physical interface between the unit and the bus line. Since the functioning of the whole system relies on the correctness of the exchanged messages, the bus line interface must be designed very carefully. A complete discussion of the needed design criteria is far beyond the scope of this application note.

A list of desirable features is:

a) High noise rejection

b) Line faults (short to GND or VCC, wire cut) detection and real time recover.

c) High RF noise immunity

d) Low RF emission

The solution implemented here is a differential bus line driven by two complementary MOS devices.

The passive components around the MOS polarize and protect the devices against shorts, spikes and negative voltages applied to the bus lines.

Capacitances placed on the bus lines filter out RF noise, also reducing the bandwidth of the bus channel in order to avoid too sharp edges during bus transitions, i.e. RF emission and subsequently possible interferencies with other equipment (dashboard instrumentation, car radios etc.)

The three comparators in the RX section allow a full fault detection and recovery. This means that transmission and reception can continue also if one line is shorted to GND or V_{CC} or cut.

Figure 4: Keyboard Unit Block Diagram

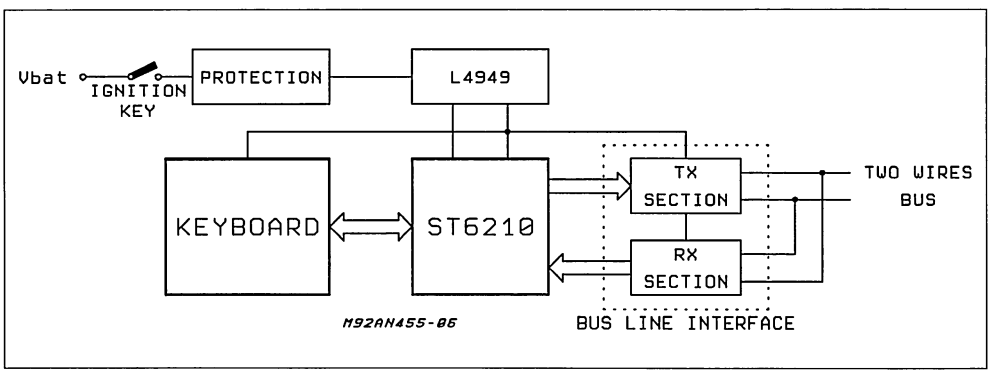
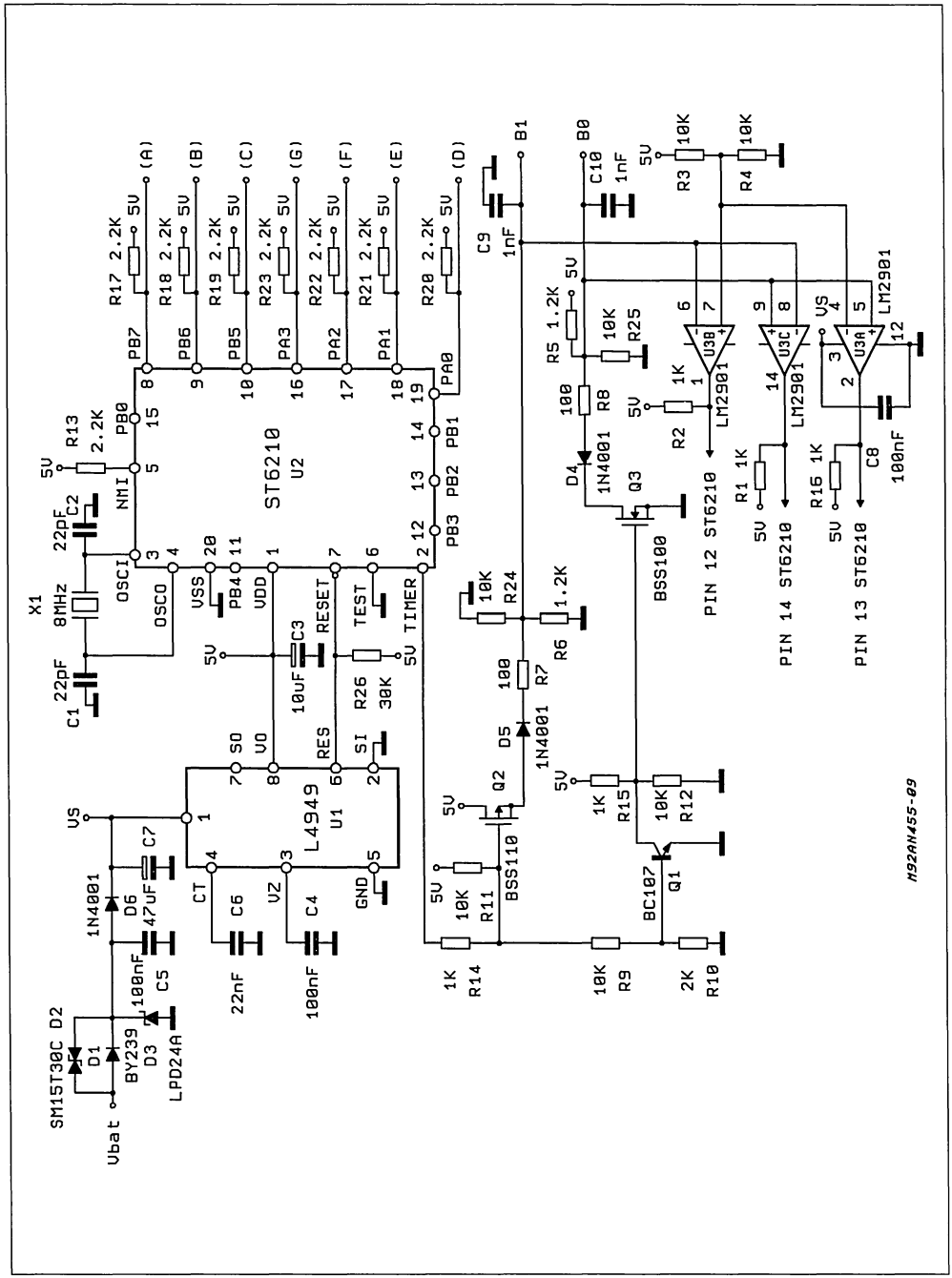


Figure 5: Keyboard Unit Schematic Diagram.



KEYBOARD UNIT DESCRIPTION

The block diagram and the schematic diagram of the keyboard unit are shown respectively in fig. 4 and fig. 5.

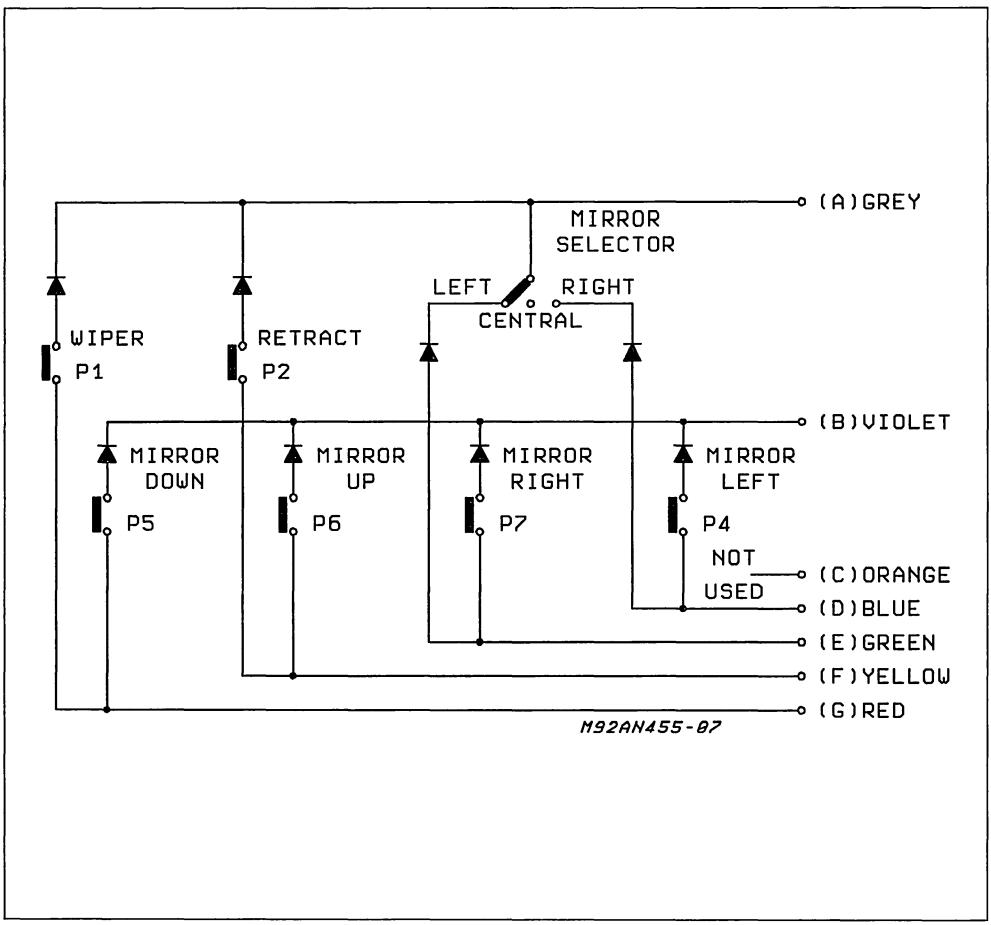
Many blocks in the architecture of this unit are very similar or identical to those used in the mirror unit.

This blocks are protections, voltage regulator and the bus line interface. The uC used is the same adopted in the mirror units.

A 4 X 2 matrix-organized keypad is connected to the unit. The schematic diagram of the physical keyboard is shown in fig. 6.

Since the physical keyboard rows and columns are directly connected to the uC pins, it must be placed very close to the electronics to avoid induced noise. A software debouncing strategy has been implemented so that a key transition is validated only if the new state has been stable for at least fifty milliseconds.

Figure 6: Keyboard Schematic Diagram.



SOFTWARE DESCRIPTION

Introduction

Two different programs have been written, one for the mirror units and one for the keyboard unit. The software was developed using the ST6 hardware emulator, and the ST6 macroassembler and linker. The mirror unit and keyboard unit programs are respectively about 1340 and 1280 bytes long. The main difficult in this software development was to overcome the uC limitations (using some software tricks) without affecting the overall program's readability.

Mirror Unit's Software Description

The software developed for this unit can be divided, at the functional level, into 3 main sections.

1) PROTOCOL HANDLER SECTION

This routines perform the serial bus message reception and transmission.

The reception procedure starts when a valid SOM (see BUS PROTOCOL DESCRIPTION paragraph) is detected. The reception ends successfully when the following conditions are obeyed:

a) Ten correct bits (i.e. with the right timing between two edges) are decoded.

b) The received checksum field matches the checksum calculated upon the preceding eight received bits.

If an error occurs, the reception is aborted and the unit starts to wait for a new valid SOM.

The transmission routine starts when the unit must send a message on the bus line. The ST6 timer is used to obtain the desired time between the edges.

2) MESSAGES DECODING AND ACTUATIONS

This section performs the message decoding and the actual driving of the L9946.

Once a correct message is received, the mirror unit compares the received address field with its own address. If they are equal, the data field of the message is decoded and the corresponding action or series of actions are undertaken.

The data fields recognized by the mirror units and their meaning are:

01110 : wiper on

10000 : wiper off

01010 : fold/open

00010 : up movement

00100 : down movement

00110 : left movement

01000 : right movement

10010 : stop motors

Immediately after the action has started, the mirror unit transmits an acknowledge message to the master unit (i.e. the keyboard unit). This message is the echo of the acknowledged reception.

3) L9946 PROTECTION

The L9946 DG1 and DG2 pins are connected to uC interrupts lines so that a fast switch off is executed when an overcurrent or an overtemperature occurs in the device.

Keyboard Unit Software Description

In the sotfware for this unit the protocol handler section is the same code used in the mirror units.

The keyboard units acts like the master of the system.

The matrix keyboard is scanned every five milliseconds. If no key status variation is detected, every fifty milliseconds a stop message is sent to the slave units as a polling. The slave units should answer to this messages. If this is not the case, the master unit knows that one or both slaves are disconnected or broken.

When a key is pressed, a debouncing procedure is started. If the pressure remains at least for fifty millisecond the corresponding command message is sent to the unit selected by the position of the three-way selector.

If this selector is in its central position, only the fold/open command is enabled, and the subsequent command is sent to both slave units.

The keyboard unit keep sending the command until the key is released. Then, the normal no-operation polling is executed.

BUS PROTOCOL DESCRIPTION

1. GENERAL

The information between the units is passed in messages transmitted serially on the bus connected to all the units.

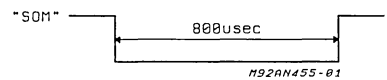
When the bus is in the idle state, i.e. no message is transmitted, its state is called "passive state". It is driven in the "active state" by a transmitting unit at the start of a message for the "start of message" time.The state is passive for the first (most significant bit) information time, active for the next bit time and so on until the message is finished (terminated) in the passive state. The value of the bit is determined by the time elapsed between two consecutive transition of the bus state. This bit encoding is called VPWM (variable pulse width modulation).

2. MESSAGE SYMBOL WAVEFORMS

The following sections show the nominal timing requirements of the VPWM message simbols generated by the software protocol handler as they appear on one wire of the bus. On the other bus wire the signal is inverted.

2.1. START OF MESSAGE

This symbol appears at the start of every message when a transmitter drives the bus in the active state to start the message.

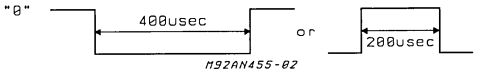


2.2. DATA BIT

Each data bit is represented by the time between two consecutive transitions. These are both passive and active bit states that are used alternately.

2.2. "0" BIT

The two "0" bit waveforms are:



2.3. "1" BIT

The two "1" bit waveforms are:

3. MESSAGE FORMAT

A message consists of a start of message (SOM) field, an address (ADR) field (3 bits), a data (DATA) field (5 bits) and a checksum (CHK) field (2 bits), for a total of 10 bits transmitted.

With the timing given in the above sections, the average transmission bit rate is 3.3 Kbps.

The SOM is the signal on wich every receiving unit starts the reception procedure.

Once a successful reception has been completed, the DATA field is decoded and the related action undertaken only if the ADR field matches with the wired address assigned to the receiving unit.

The CHK field is a way to detect some type of errors occurred during the DATA field bits transmission. During the reception procedure, a checksum value is calculated, and the reception is valid only if this value is equal to the contents of the received CHK field.

The algorithm used to calculate the checksum is the following.

a) Count the number of "1" bits in the DATA and ADR fields.

b) Take the two less significant bits of this number.

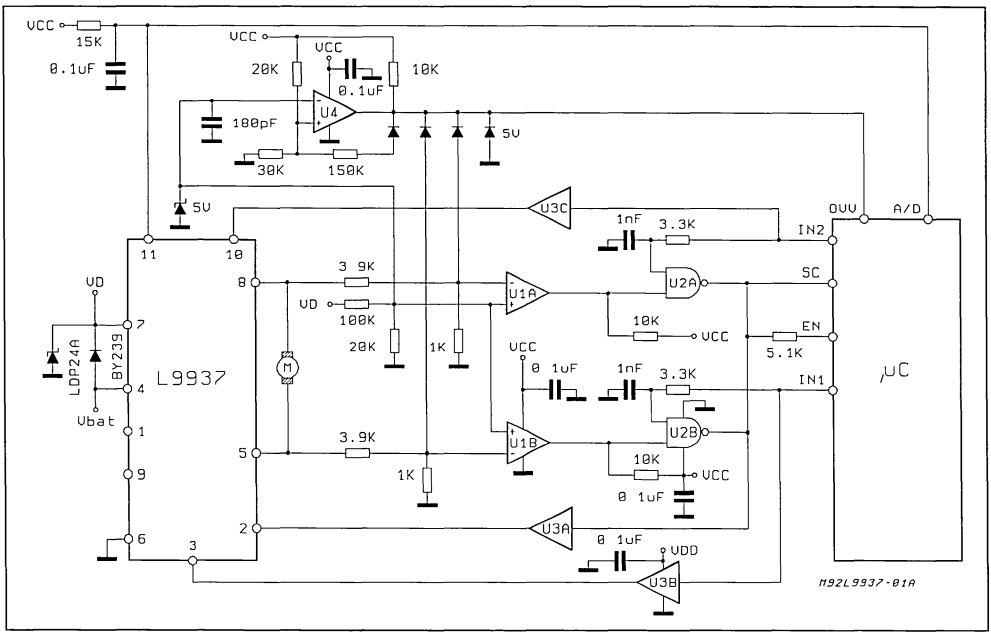
c) Complement these bits.

6A DOOR LOCK MOTOR DRIVER FOR AUTOMOTIVE

by Stefano Vergani

An application of the L9937 device (Full Bridge Motor Drive) is described. The interface between the L9937 and a µC is discussed. A complete protections circuitry description is also given.

Figure 1.



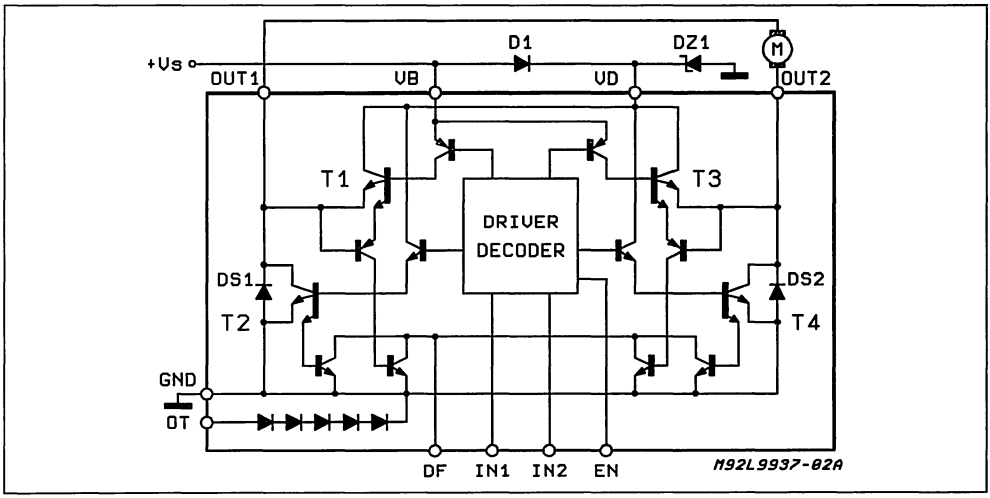
The L9937 device is a full bridge for bidirectional motor driver applications realized in bipolar technology; it can deliver up to 6A output current with low saturation voltage.
Two diagnostic informations are provided to monitor overload conditions and the internal temperature, and the device is assembled in the MULTIWATT-11 package with the case connected to the ground terminal.
The L9937 is particularly suitable to drive bidirectional DC motors in µC based systems.
Fig. 1 shows a possible application circuit, with an analog interface between the power devices and the µC.

In the following, the functions of each block of the analog interface are described.

1 - Overvoltage And Reverse Battery Protection

L9937 is particularly suitable to drive the door lock motors in automotive applications. Fig. 2 shows the circuit schematics; due to the hostile automotive environment, it is necessary a transil (suggested type LDP24A) between V_D and GND, to protect the L9937 against overvoltages higher than 50V. The diode D1 suggested type BY239-200A) supplies the voltage VD necessary for the correct device's operation at the same time it protects the device against the reverse battery.

Figure 2



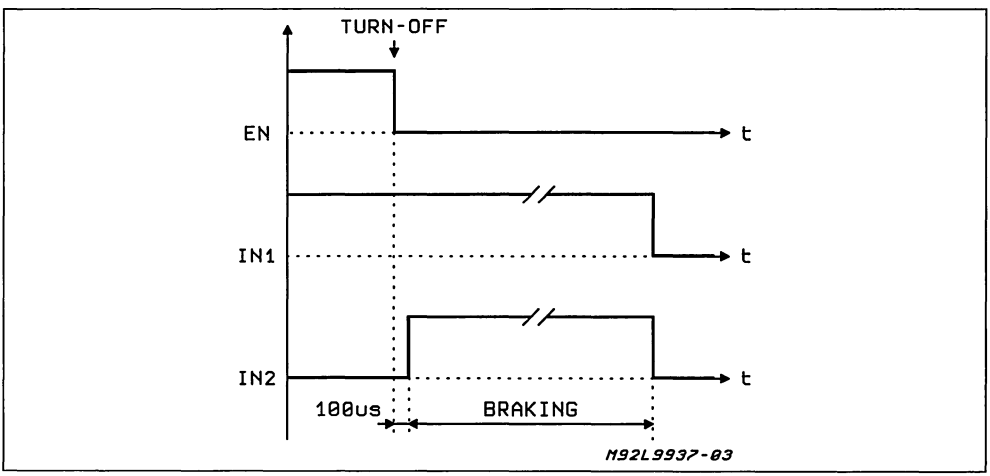
2 - Switch-off Sequence

Referring to Fig. 2 and supposing i.e. T1 and T4 ON, T2 and T3 OFF (this means EN=H IN1=H IN2=L), the following steps have to be observed to allow a correct recirculation of the current in the motor at the switch off (Ref. Fig. 3):

a)switch off T1 and wait for 100µs about in this condition (EN = L IN1 = H IN2 = L)
b)after the a.m. delay switch ON T2 (EN = L IN1 = H IN2 = H)
c)switch off both T2 and T4 after the motor stop (EN = L IN1= L IN2 = L)

Step a) allows the recirculation of the motor current due to the inductive component of the motor itself between DS1 and T4; the 100µsec delay time is needed to avoid the cross-conduction in the left half bridge.
In step b) the motor is short circuited to GND (T2 and T4 ON) and this allows the dynamic braking.
In step c) T1, T2, T3 and T4 are OFF to allow a very low current consumption of the bridge.
If the dynamic braking is not requested, step b) can be omitted. In any case the lower power transistor of an half bridge must be kept ON, after the switch off of the upper transistor of the other half bridge, for a time longer than $T = 5 \cdot R_L/L_L$, where Rl and Ll are the resistance and the inductance of the load.

Figure 3: Switch-off Sequence



3 - Input Driving Voltage

To allow a correct operation of L9937 over the full temperature range, the driving voltage at the input pins must be higher than 5.5V, with 4mA current capability.

4 - Short Circuit Protection

It is possible to protect L9937 against short circuit to ground and across the motor in the full bridge application.
The circuit schematics shown in Fig. 4 uses two voltage comparators (U1A, U1B) to detect the Vce of the upper power transistors. U2A and U2B are open drain NAND gates (i.e. part no. HCC40107) and U3A/B/C/D are non inverting buffer to drive the L9937 (i.e. part no. 74HC4050).
U1A and U1B sense the differential voltage VD-OUT2 and VD-OUT1 respectively. Referring to Fig. 4, chosen R1=100K and R2=20K, the values of R3 and R4 may be calculated according to the following formula:

$$R3 = \frac{(V_D - V_{CETH}) - 0.166\ V_D)}{0.166\ V_D} * R4$$

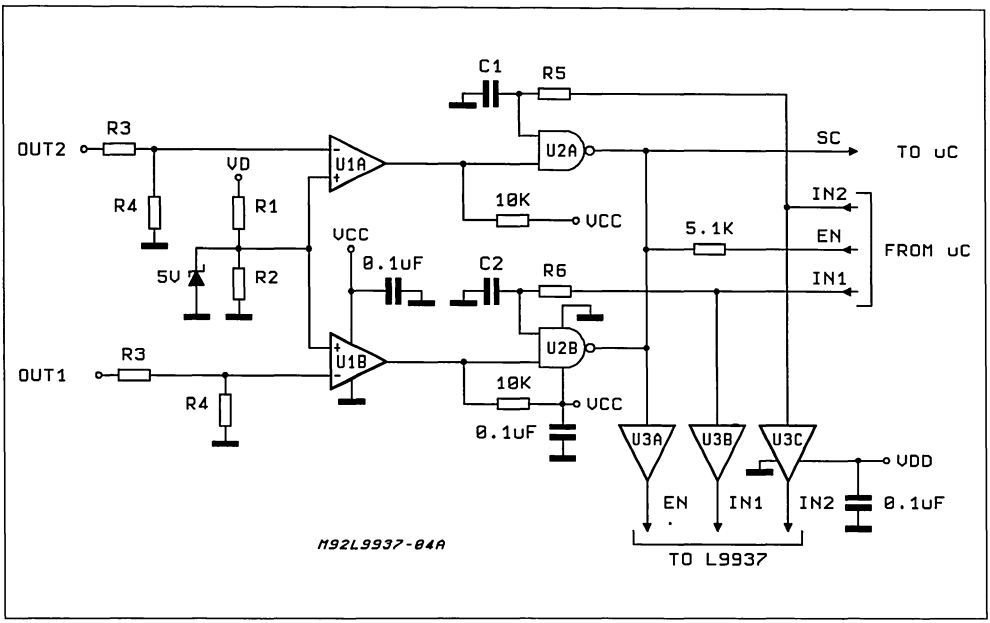
where :

V_D = bridge power supply
V_{CETH} = collector to emitter detection threshold.

Choosing:
V_{CETH} = 2V @ V_D = 12V and R4 = 1K, the above formula gives R3 = 4K.

When all signals from µC are at low level (motor off), the inputs to the bridge are low too; in these conditions the output voltage of the two comparators is high and therefore the outputs of U2A/U2B are free. When the µC sends, for example, IN2 and EN high, OUT2 of the bridge goes high and OUT1 goes low.
At this point the output of U1A pulls down the input of U2A before that the delay capacitor C1 is charged (through R5) up to the U2A threshold; in this way the U2A output remains free and the bridge drives the motor.
If a short circuit occurs, the Vce of the upper power transistor increases above the threshold and then the U2A output pulls down the enable input of L9937. At the SDME time the SC signal to µC, high in normal conditions, goes low; at this point the µC executes the switch-off sequence.
We have just explained what happens when a short circuit occurs during the motor running phase. Another faulting condition occurs switching on the bridge when a short circuit is present; in this case the bridge is driven for a time depending on the time constant R5 • C1 = R6 • C2.
Choosing R5 = R6 = 3.3K and C1 = C2 = 1nF, then the time constant will be T = 3.3µsec, that is 5µsec about delay time. Longer delay time might allow the short circuit current to reach values beyond the absolute maximum ratings.

Figure 4



5 - Thermal Protection

The L9937 has 5 built-in diodes series-connected that can be used to implement a thermal protection for the device.
Fig. 5 shows the relationship between the voltage across the diodes and the temperature at 100µA diode current.

Figure 5

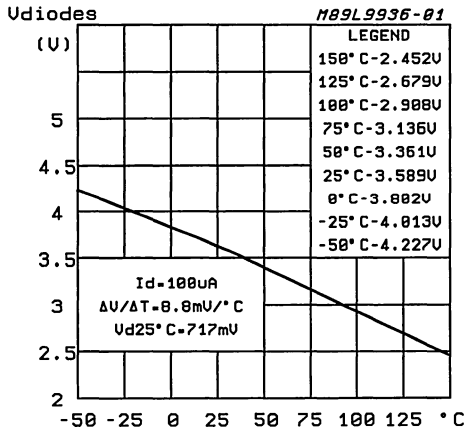
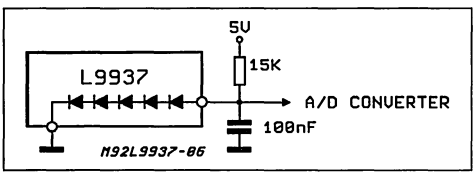


Fig. 6 shows the simplest solution to do a thermal protection; an A/D converter of the µC is used to detect the voltage drop across the 5 diodes. The 15K resistor sets the current in the diodes and the 100nF capacitor acts as a filter against the noise. When the µC detects a voltage lower than the low threshold chosen according to the diagram in Fig. 5, it executes the switch-off sequence and rejects any command to the bridge until the diodes voltage increases beyond the high threshold. The recommended hysteresis value is 30°C.

Figure 6

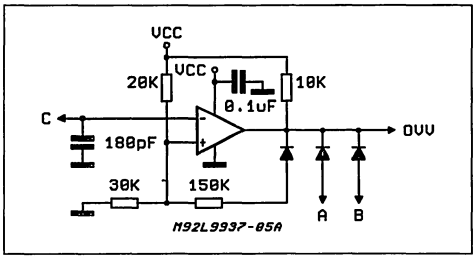


6 - Overvoltage Protection

At point 1 we suggest a way to protect the L9937 against the voltage transients. This protection allows the device to withstand overvoltages only if the bridge is not operating. To protect the device against the overvoltages in all the operating conditions it is possible to implement the circuit shown in Fig. 7.

(Note: A-B are connected to the nodes between

Figure 7



R3 and R4 (left side and right side) in Fig. 4; C is connected to the node between R1 and R2 in Fig. 4). When V_D reaches 18V the comparator output pulls down A and B, causing the intervention of the hardware protection showed in Fig. 4; at the same time the OVV signal is sent to µC, which executes the switch off sequence. The µC must reject any command to the bridge during the overvoltage conditions.
With the values shown in Fig. 7, a 1V hysteresis is provided.
It is possible to enhance the performances of the system just described avoiding the braking of the motor also for short duration voltage transients; to do this the µC, once received the overvoltage diagnostic signal (OVV), put at low level the enable of the L9937, confirming the hardware switch-off of the motor; in this condition an output of the half bridge is in high impedance state and the other one is low, allowing the recirculation of the current and the free running of the motor.
The system holds this condition until OVV is active; when the OVV signal is released the µC resets the hardware protection, sending EN = IN1 = IN2 = L and then restore the previous command to the bridge.
It is mandatory, however, to wait for the complete current recirculation of the motor before to reset the hardware protection; in facts, when EN = IN1 = IN2 = L both the L9937 outputs are in high impedance conditions.

7 - Diagnostic Feedback Output

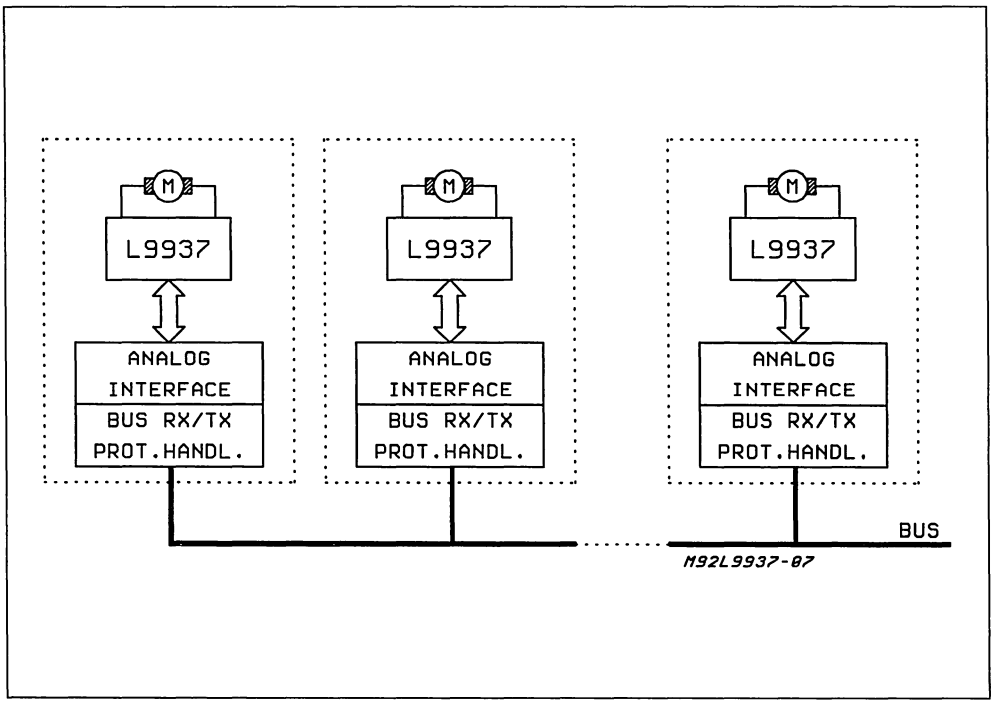
DF pin is an open drain output to monitor overcurrent and overtemperature conditions.
The overcurrent detection threshold is inversely dependent from the temperature of the chip.
Typical application of this function is to send the DF signal, with an external pull-up to Vcc, to a digital input of the µC; when the DF signal goes at low level, the µC executes the switch-off sequence.

L9937 IN A BODY MULTIPLEX ENVIRONMENT

All the functions described above can be implemented in a custom integrated circuit together with a bus transceiver and a protocol handler.

It is then possible to obtain a very small size module that can be integrated directly in the actuator. Fig. 8 shows a typical application of these modules as peripheral units in a "Class A" wired Multiplex System.

Figure 8: "Class A" Wired Peripheral Application



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SMART POWER TECHNOLOGIES FOR POWERTRAIN & BODY ELECTRONICS

by R. Ferrari

Smart power ICs are becoming increasing by common in automotive powertrain and body electronics. This note provides a general introduction to the subject.

As is well known, electronics is slowly but progressively invading every part of the automotive environment (figure 1); entering first in the car radio, it has extended progressively and is now present in all of the subsystems of an automobile. For those people who prefer a "historical" approach, the evolution of auto electronics has been divided into three main sections, each subdivided into various phases, correlated with the state of the art in general electronics at that time. Today, at the beginning of the 90's we are in the SMART POWER phase, and it is precisely that which we intend to discuss briefly here (see fig. 2).

We will look at, first of all, some definitions: smart power or intelligent power indicates those families of integrated circuits which include both logic control circuits and components capable of delivering a significant amount of power to a generic load. In numbers, a circuit can be considered smart power if it is able to deliver more than 0.5A to the load, or of withstanding more than 50V, or able to supply a power of at least 1W to the load.

Over the years SGS-THOMSON has developed various technologies that allow the realization of smart power circuits (figure 3). The simplest way to classify these technologies is to refer to the process type, which can be purely bipolar or mixed, that is, including on a single piece of silicon both MOS structures (of control and power) and bipolar structures. Another method (figure 4) is to examine the way in which the current flows through the power section; horizontal, with the current entering and leaving through the upper surface, or vertical, where the current enters through the upper surface and leaves through the lower surface; for this lower connection instead of wire the tie bar of the package is used.

The choice of one technology rather than another depends on various elements (figure 5) but simplifying as far as possible the criteria, we can say that vertical technologies can guarantee, for a given area, lower resistances but they have the limitation of being able to include just one power device per circuit (or more than one, but always with the collectors or drains short-circuited); while

Figure 1: Electronics in present and future automobiles.

SAFETY & CONVENIENCE	BODY CONTROL	POWER TRAIN	DRIVER INFORMATION
Rear Window Defogger	Cruise Control	Ignition	Digital Gauges
Climate Control	Intermittent Wipar	Spark Timing	Digital Clock
Keyless Entry	Antitheft Devices	Voltage Regulator	Multitons Alarms
Automatic Door Lock	Electr. Suspension	Alternator	Engine Diagn Results
Light Drimmer	Electr. Steering	Idle Speed control	Service Reminders
Traction Control	Multiplex Wiring	Turbo Control	Miles to Empty
Antiskid Braking	Module to Module	Emission System	Shift Indicator
Window Control	Communications	Transmiss. Control	Head-up Display
Memory Seat	Load Sensit. Braking	Diagnostics	CRT Display
Heasted Windshield	Hard/Soft Ride Control		Audio Annunciator
Voice Controlled Trunk			
Airbag Restraints			

Figure 2.

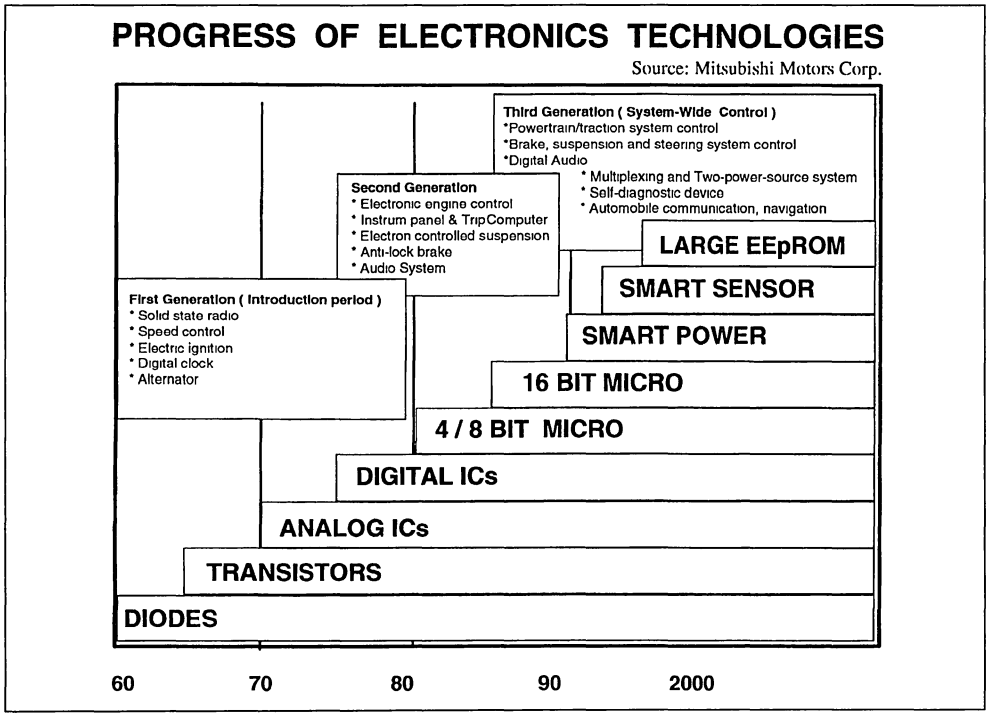


Figure 3: Smart Power Technologies Matrix.

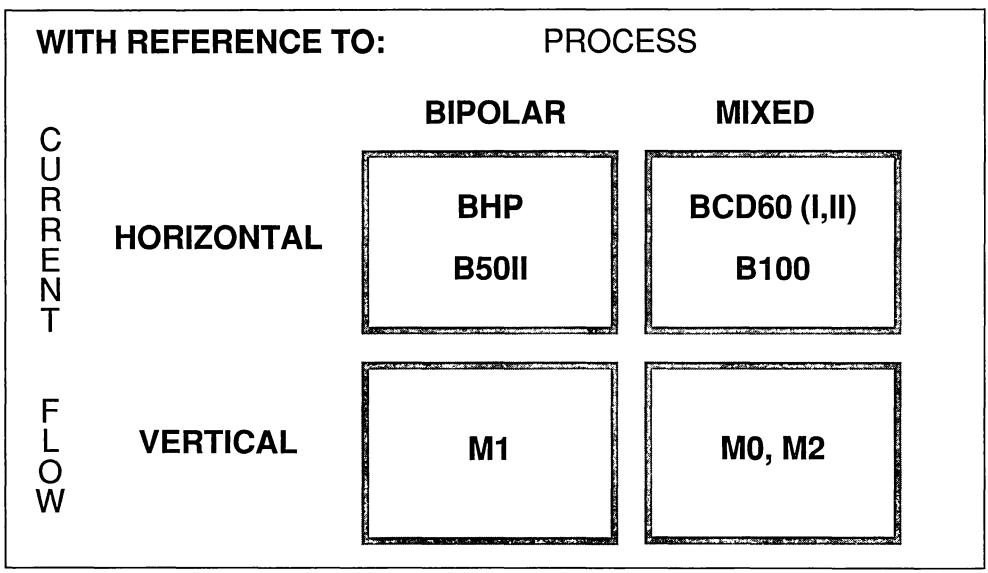
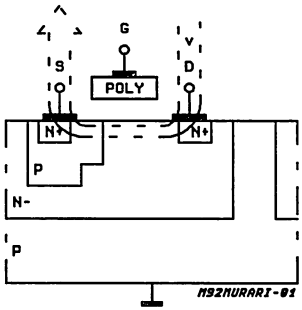
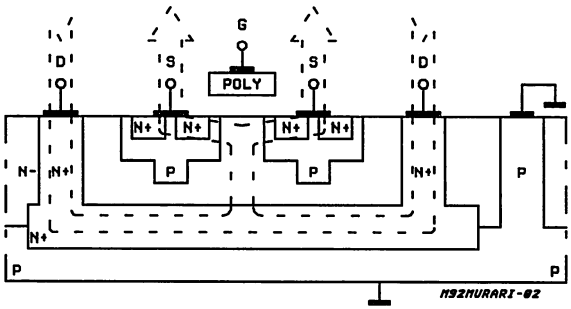


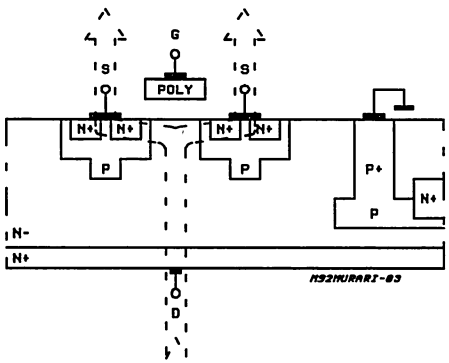
Figure 4: Integrated DMOS structures.



1OR MORE HV LDMOS DEVICES WITH COMMON SOURCE



MANY POWER VDMOS DEVICES ANY CONFIGURATION



1 OR MORE HC VDMOS DEVICES WITH COMMON DRAIN

Figure 5: Smart Power Technology Matrix selection criteria.

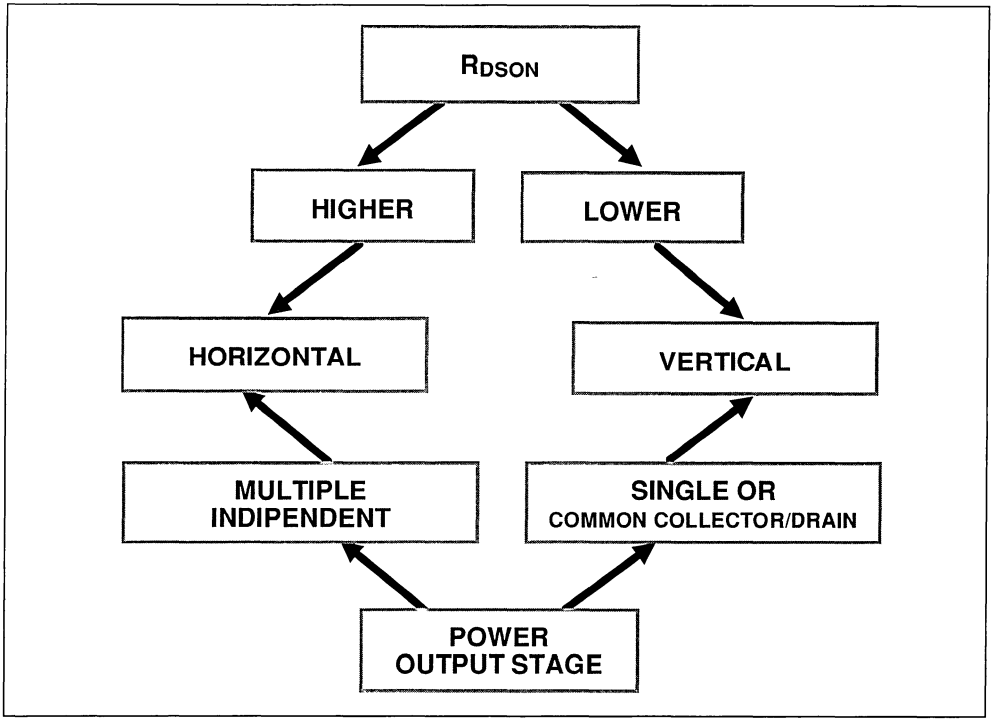


Figure 6: Multiple independent Power Structures realized with Horizontal Technology.

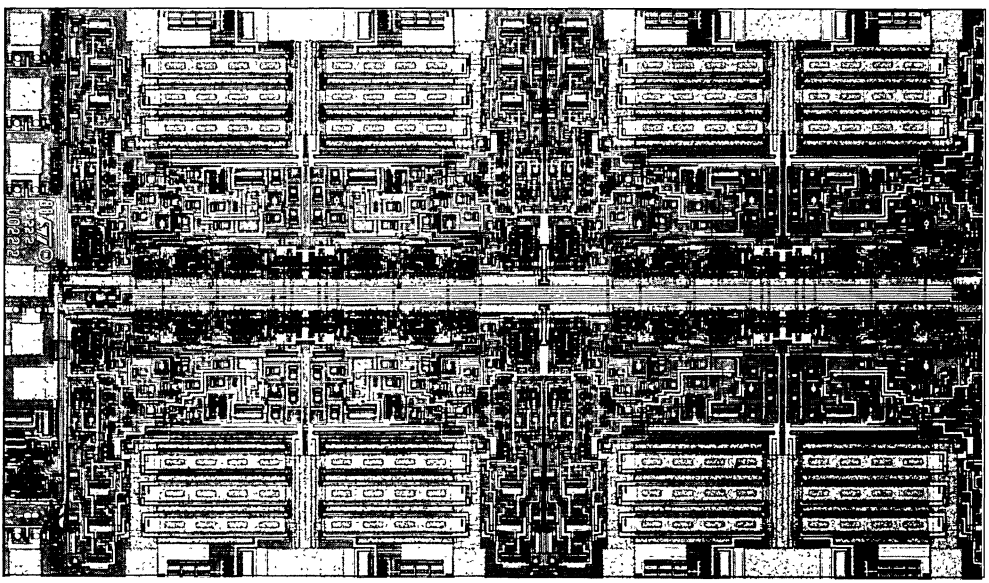


Figure 7: Bonding wire features.

WIRE	DIAMETER (micron)	RESISTANCE (mOhm/mm)	D.C. CAPABILITY (Ampere) in plastic package
GOLD	25	45	1.25
GOLD	51	11	2.50
ALUMINIUM	178	1	15
ALUMINIUM	254	0.5	28
ALUMINIUM	381	0.2	43

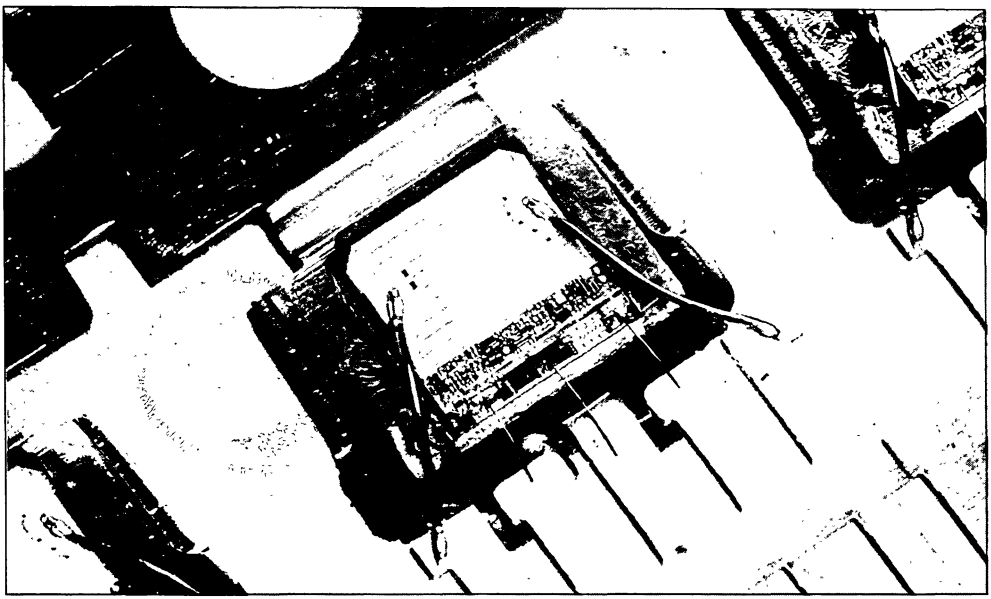
horizontal technologies make it possible to have power structures that are completely independent (figure 6). It is therefore evident that a vertical technology will give excellent results in the design of a light switch, while a horizontal technology will be equally well suited to the design of a multiple actuator.

It is important at this point to underline that a smart power circuit does not consist of just silicon technology, but relies heavily on package technology. In fact it is well known that a signal device is bonded using gold wires with a diameter of 25 microns; however, gold wire can be used effectively up to diameters of 50 microns, which allows reliable operation with currents up to 2A, provided that the wire is surrounded by resin (the current capacity drops by 50% for wires in free air -- that is, in the case of hermetic packages,

When, however, one has to deal with very high currents (more than 5A in single-point injection actuators, and more than 10A for windowlift motors) gold wires are no longer usable for obvious cost reasons so it is necessary to turn to aluminum wires (figure 7) with a diameter from 180 microns to 375 microns; clearly in this case it will be necessary to have adequately dimensioned bonding pads on the die, with a significant waste of silicon area.

Optimization is obtained with a mixed bonding technology where signal pads are bonded with thin gold wires and power pads with thick aluminum wires (figure 8). A further optimization is obtained by orienting the pads in the pad-to-bond-post direction. But while we are speaking of power it is also important to speak of packages (figure 9). These packages are part of a long tradition of TO-220 type packages (with 3, 5 and 7 pins) but recently new needs in assembly are bringing important evolutions of the classic tab

Figure 8: Mixed Bonding Technology.



packages. Devices completely encapsulated in completely isolated packages — called Isowatt — are already in production; in these devices isolation up to 1000V is obtained with a minimum reduction in the junction-to-case thermal resistance.

On the other hand, the practice of using clips, rather than screws. for mounting packages is becoming always more common, both to save space and to obtain better long-term reliability in thermal conduction. This has led to the TABLESS isolated package which accumulates the previous two needs, while for surface mounting a non-isolated package with a junction-case thermal resistance less than 3'C/W is in development in our laboratories and will be available in industrial quantities in 1991.

Now that we have examined the means that technology places at our disposition, both in diffusion and in assembly, we can now examine what typical structures smart power processes will allow us to make, and which kind of circuit will normally be driven by each structure (figure 10).

Figure 9: Power package Matrix.

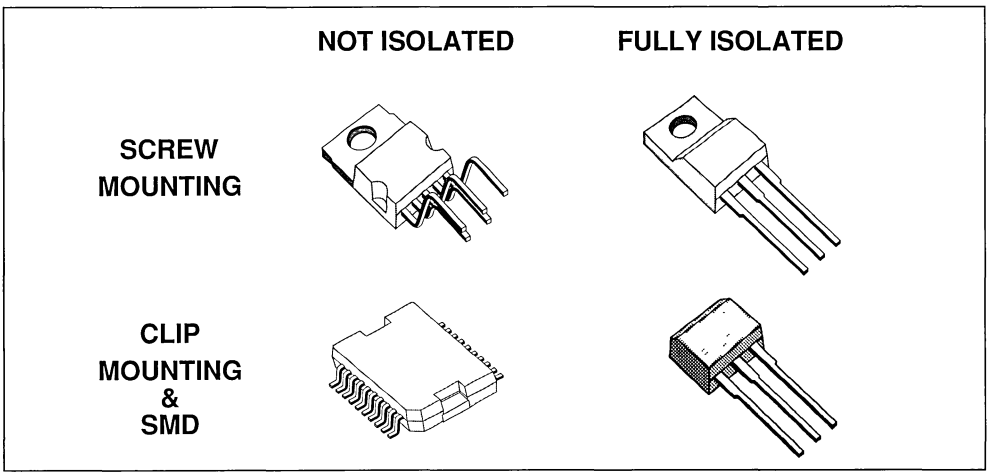


Figure 10: Intelligent power actuators basic configuration.

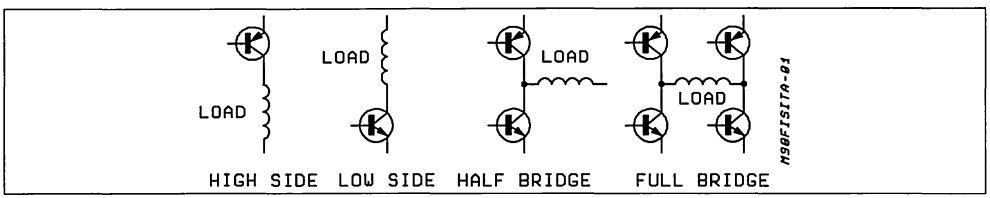
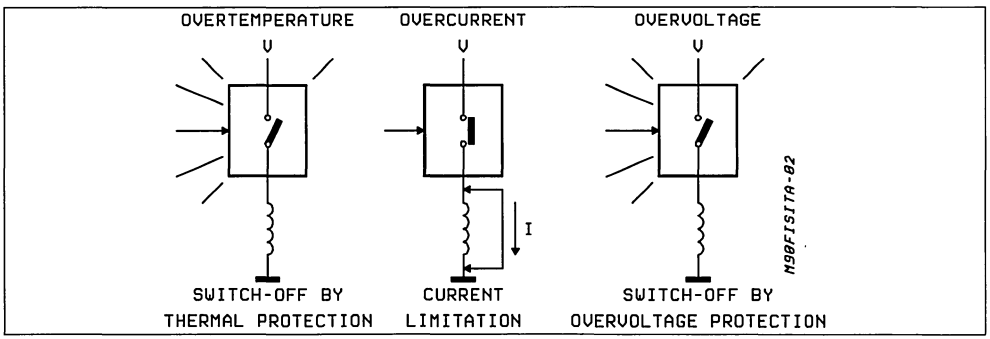


Figure 11: Intelligent power actuators basic protection.



1.The typical, so-called High Side configuration, in which the actuator is located between the supply and the load, is traditionally used in the supply of resistive loads, typically lamps, but is also suitable for mono-directional motors.

2.When the actuator is between the load and the ground of the supply system we have a "low side" configuration, very common for driving inductive loads such as, for example, the solenoids that control the opening of valves (injectors, ABS system, automatic transmission), but also ignition coils.

3.Finally, when we have to drive a motor that rotates in both directions it will be necessary to use a bridge structure; the choice between integrating the whole bridge or just half of it clearly depends on the current involved. Today's technology allows us to realize efficiently a complete bridge to drive a door lock motor, while it is necessary to use two half bridges if the load is a windowlift.

In all of these structures there will always be integrated a certain number of protection circuits, to guarantee survival of the device in the presence of possible failures in the surrounding ambient (figure 11).

These include, to name a few, the automatic shutdown when the silicon reaches a critical temperature (which can be caused not only by a short circuit in the load or its connections, but also by the degradation of thermal contact between the device and its heatsink). Today, in certain applications such as fuel injection this automatic shutdown tends to be replaced with a warning signal, which informs the control unit when a critical situation has been reached, leaving the unit itself to decide what to do (for example, reduce performance to guarantee functionality).

Another very common structure is output current limiting, even in the case of a load short circuit. Usually the intervention of the limitation circuit is accompanied by a diagnostic signal that is made available for the control system. Finally, in some devices a circuit is included that is able to detect overvoltages in the supply system, disabling the output stage and placing it in the best conditions to support the overvoltage.

Given the above, we will now describe a practical case with the aim of identifying how the design time can be optimized through a suitable interaction between the system designer and the silicon manufacturer.

The circuit shown in figure 12 is a dual low-side actuator designed to drive two independent loads with currents up to 3A each (typically injectors). The technology employed is mixed (bipo-

Figure 12: Dual 3A Low-side Actuator.

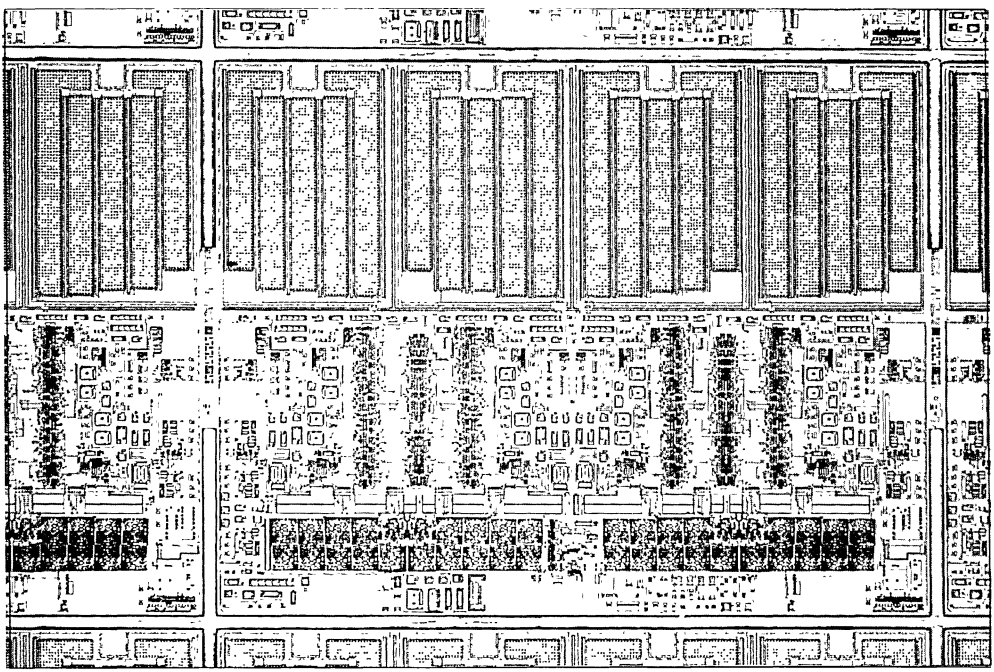
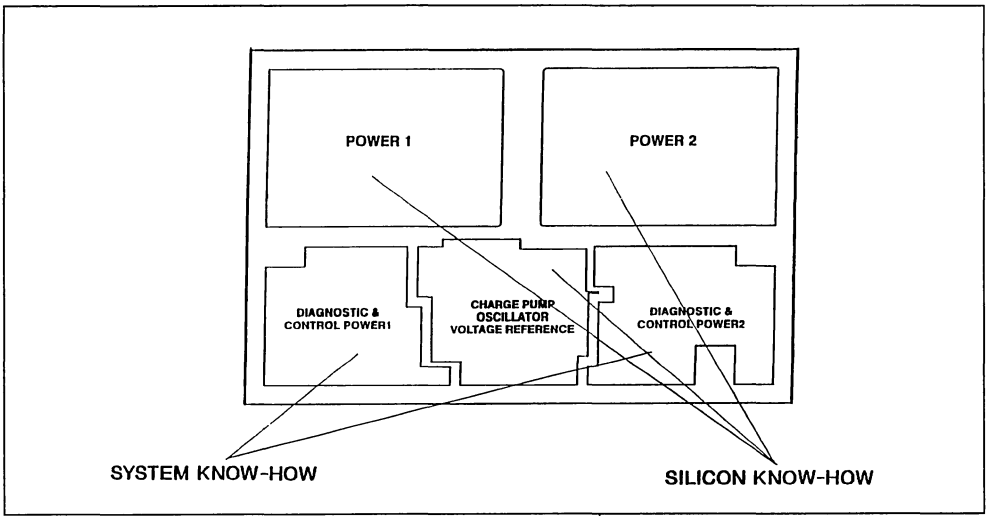


Figure 13: Expertise partitioning when designing a smart power actuator.



lar/CMOS/DMOS) with a horizontal current flow (BCD60); if we pass from the photograph to a topographical diagram of the silicon (figure 13) it becomes immediately evident that the chip is divided into a limited number of macroblocks, for each of which it is easy to attribute project leadership. In fact it will be an essential task of the system designers to define the criteria for the driving of the actuator as it is to define the malfunctions for which the activation of a diagnostic signal is necessary. On the other hand it is indisputable that only the silicon designer can optimize the design of the power section and take advantage of structures already available in his library to realize those functions which are necessary and also repeated frequently in different devices.

The system designer, too, can take considerable advantage from the use of cell libraries so the total design time can be reduced to a minimum (7-9 months from the start of the design to working silicon), reducing significantly the gap traditionally existing between a dedicated circuit (full custom) and a semicustom circuit obtained from gate arrays or standard cells.

A brief glance at another two circuits, each representative of a technology described above.

In the first we see a highly-innovative circuit for use in ignition systems. This is the VB020 (figure 14), a circuit realized in mixed vertical technology (M2) able to drive directly the primary of the ignition coil, combining a darlington with a vertical current flow with a driver circuit and TTL/CMOS compatible control circuit (figure 15). In the device are integrated circuits to limit the collector voltage (fixed at 450V max).

We conclude this series of examples with the L9937 (figure 15), a bridge circuit designed to drive a door lock motor and therefore capable of delivering continuous currents of 6A with starting peaks up to 12A. The device is realized in horizontal bipolar technology and, as appears in the photograph, is almost entirely occupied by four large power transistors that constitute the output stages of the circuit. In this case, too, you can see the mixed bonding (gold for the signal wires, aluminum for power wires) and the pads oriented to optimize silicon area. In the block diagram (figure 16) you can see a chain of diodes which has the function of monitoring the temperature of the chip.

This brief introduction to smart power technologies would not be complete if it did not dedicate a few words to the price that the customer must pay to buy circuits of this type. In fact a typical question that semiconductor companies frequently hear is "How much does a square millimeter of smart power silicon cost?". Since the price of a square millimeter of silicon depends on the total area of the chip I believe that it can be a pleasant surprise to discover that even for fairly sizable chips — that is, up to 25/6mm2 — the price of each mm2 increases very little (about 25%). The curve of figure 17 gives the trend for areas between 5 and 50mm2 and, though based on a theoretical calculation, follows closely the present commercial reality. Obviously the graph reflects the current state of the art; if only three years ago the elbow of the of the curve had been moved violently to the left without arriving at saying that the evolution will continue indefinitely with the same speed, it is however reasonable to expect in the next few years a further extension of the linear zone at least towards the 40mm2 region. As for the meaning of "1mm2 of silicon", several

Figure 14: Fully integrated high voltage darlington for electronic ignition.

- PRIMARY COIL VOLTAGE UP TO 450V
- COIL CURRENT LIMIT INTERNALLY SET TTL/CMOS COMPATIBLE INPUT
- BUILT-IN COLLECTOR-EMITTER VOLTAGE CLAMPING
- OVERVOLTAGE PROTECTION OF THE DRIVING CIRCUIT
- FULLY INSULATED FIVE LEAD POWER PACKAGE

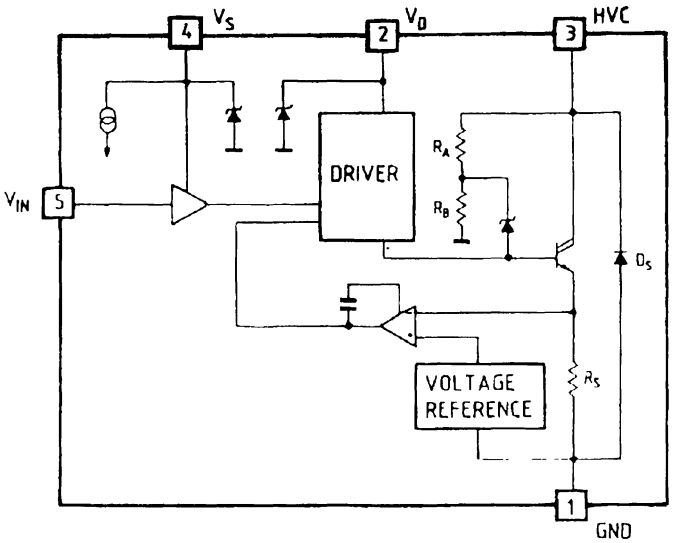


Figure 15: Die of VB020.

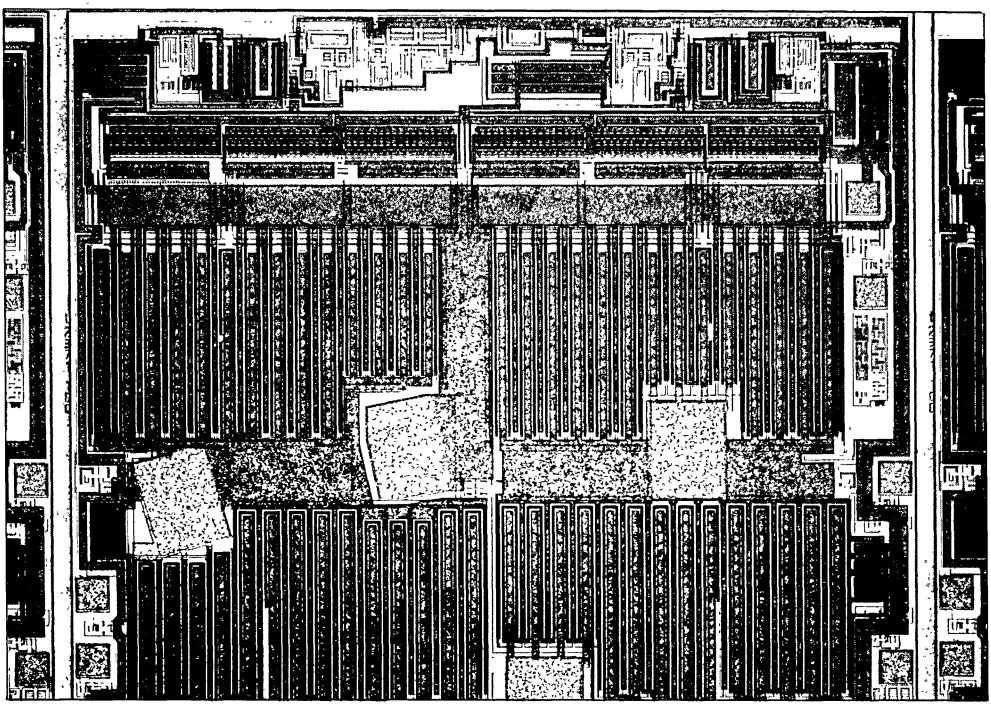


Figure 16: Full bridge motor driver.

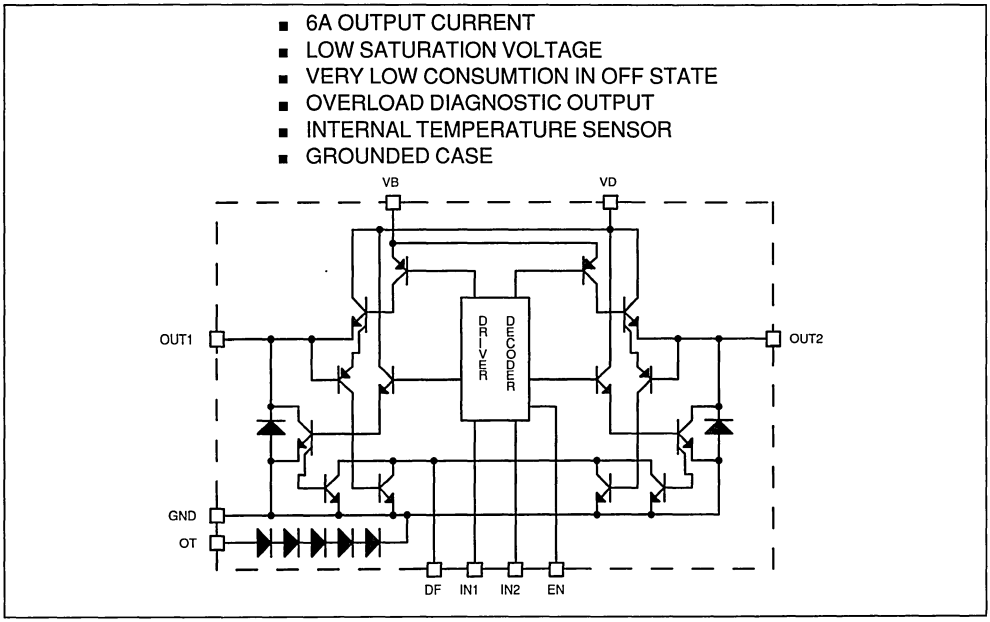


Figure 17: Smart power silicon.

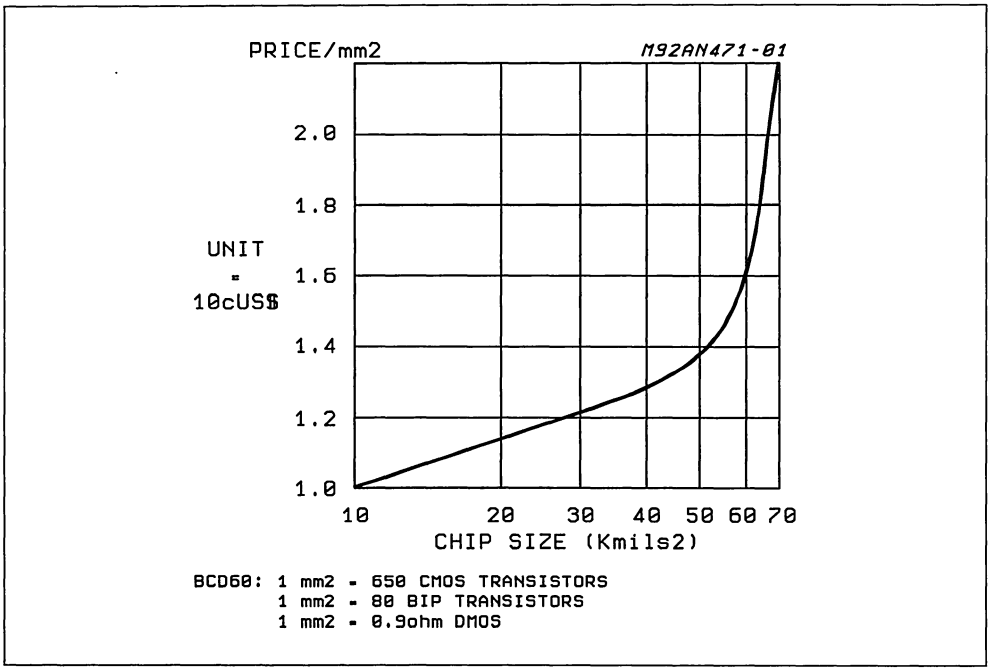
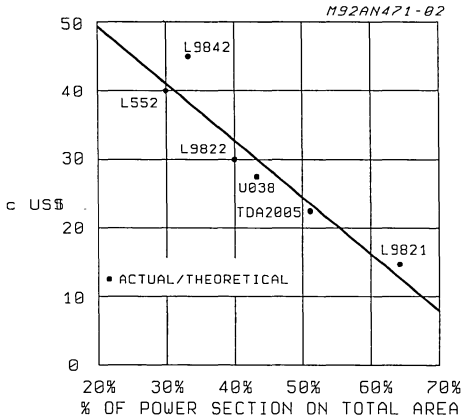


Figure 18: Smart power devices.



possibilities are given at the foot of the table.

There is another way to evaluate the price of a smart power circuit, and this is to estimate the price for each ampere delivered to the load. This method of calculation is less rigorous and can be plotted as a graph assuming as size reference the percentage of silicon dedicated to power compared to the total area of the chip. The line shown in the figure 18 graph indicates that one ampere costs approximately 30 cents but can rise to 45 cents for circuits containing particularly complex control and diagnostic logic, and it can fall to 15 cents for devices consisting essentially of only power stages. It must be underlined that two consumer devices (L552 and TDA2005 — both audio power amplifiers) for which we can assume stable specifications, mature technologies and ample markets, lie exactly on the curve. This should be indicative of the final trend for automotive devices which are as yet young devices in a young market.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

ELECTRONIC IGNITION WITH VB020 AND L497

by M. Melito

INTRODUCTION

The VB020 is a monolithic high voltage integrated circuit which combines a vertical power darlington with built-in protection circuits for coil current limiting and collector voltage clamping. The device interfaces directly with a microprocessor which controls the dwell angle.

This application note shows how it is possible to use the VB020 in an electronic ignition system not employing a microprocessor.

The IC used, the L497, is a more conventional electronic ignition controller for breakerless ignition systems using a Hall effect sensor.

OPERATING PRINCIPLE

The schematic of fig.1 shows how the two ICs are connected to control both the coil current, providing the required stored energy and the dwell angle, for low power dissipation.

The L497 was designed to drive an external Darlington and in a standard application circuit the current control is performed monitoring the coil current through a sensing resistor on the emitter of the Darlington. When the voltage drop across the sensing resistor reaches the internal comparator threshold value the dwell angle control circuit is enabled. Meanwhile the coil current is kept constant forcing the

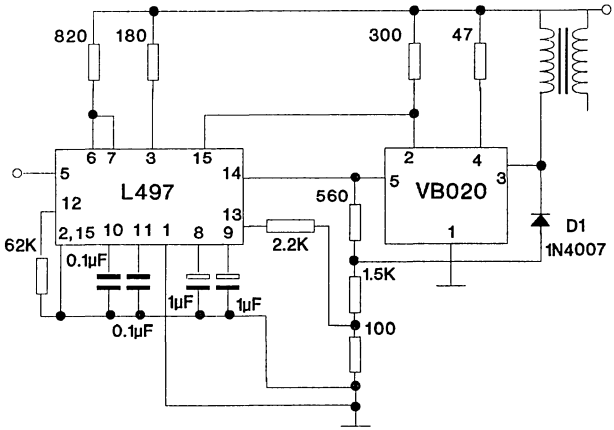


Fig. 1 - Schematic of electronic ignition with VB020 and L497.

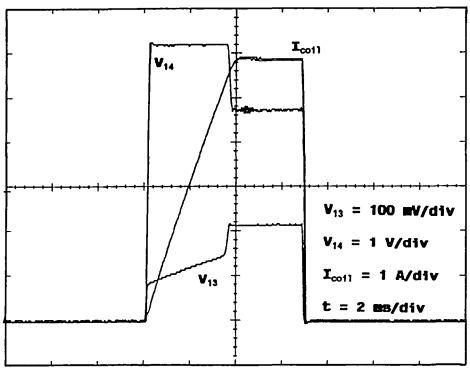


Fig. 2 - V_{13}, V_{14} and I_{coil} waveforms.

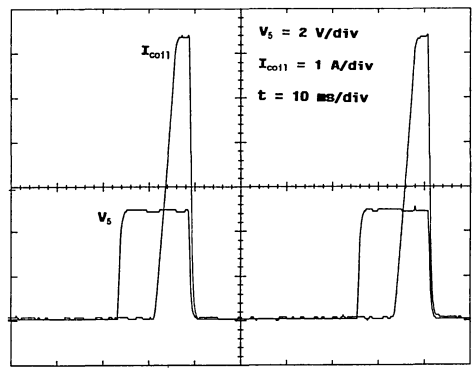


Fig. 3 - Duty-cycle = 30%; frequency = 20 Hz.

Darlington into the active region until the high-low transition of the input signal causes the spark to occur. The collector voltage is clamped to a value that is externally fixed by a resistive network. The internal dwell angle control circuit calculates the conduction time for the output Darlington in relation to the speed of rotation, to the supply voltage and to the characteristics of the coil, thus avoiding excessive power dissipation in the Darlington itself.

By linking together the L497 and the VB020 it is possible to avoid both the coil current sensing and the collector voltage clamping networks because the VB020 has internal built-in protection circuits which perform these functions. The dwell angle control is performed by supplying the L497 with the feedback signal shown in fig.2. The diode, D1, keeps the voltage at pin 13 of the L497 under the internal comparator threshold voltage until the VB020 begins to regulate the coil current. At this point

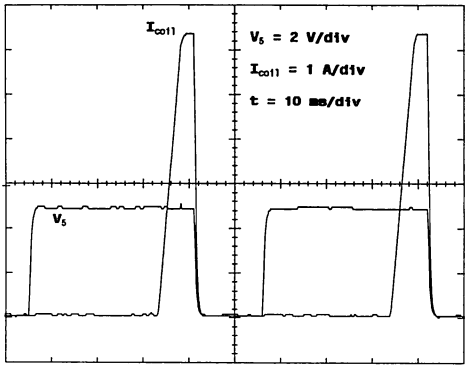


Fig. 4 - Duty-cycle = 70%; frequency = 20 Hz.

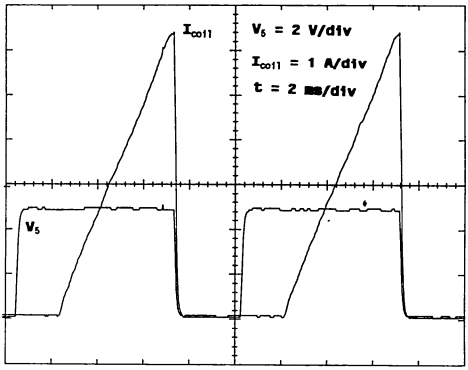


Fig. 5 - Duty-cycle = 70%; frequency = 100 Hz.

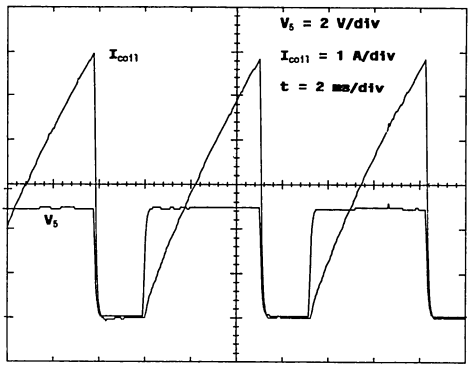


Fig. 6 - Duty-cycle = 70%; frequency = 140 Hz.

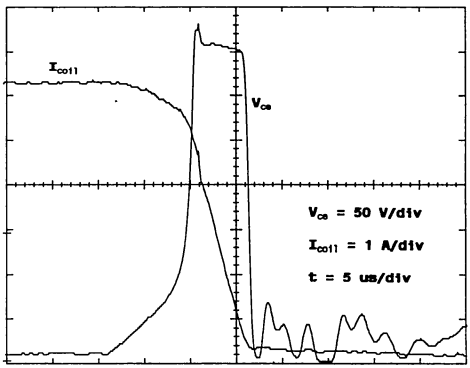


Fig. 7 - Turn-off in normal operating mode.

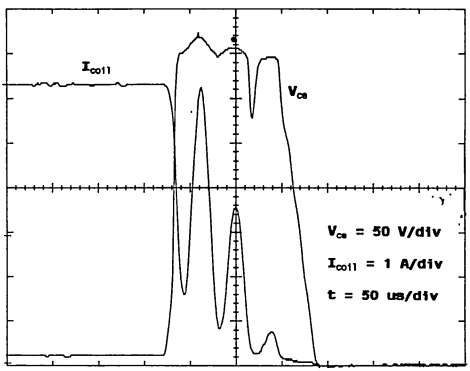


Fig. 8 - Turn-off with open gap.

D1 is turned-off and the voltage on pin 13 can reach the threshold voltage of the internal comparator enabling the dwell control circuit. Figures 3 to 8 show the system performance (V_{in}, I_{coil}) under various conditions and fig. 9 shows the conduction angle versus r.p.m. for a four cylinder engine.

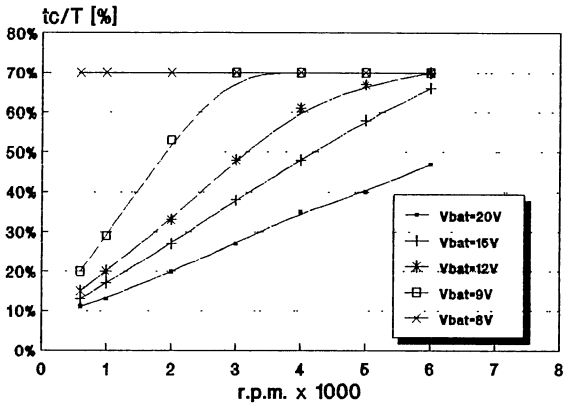


Fig. 9 - Conduction angle versus r.p.m.

CONCLUSION

The VB020 can be used in electronic ignition systems without using a microprocessor.
The overall cost of the system can be competitive with the solution using a Darlington because the current limiting and voltage clamping function performed by the VB020 are trimmed on silicon avoiding the need for additional adjustment.

REFERENCES

[1] F. Pellegrini, "L482 Development Report", SGS-THOMSON internal report, August 1982.

[2] M. Paparo, "L497 Development Report", SGS-THOMSON internal report, July 1985.

[3] "Automotive Products" Data-book, SGS-THOMSON microelectronics

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

MIXED WIRE BONDING TECHNOLOGY FOR AUTOMOTIVE SMART POWER ICs

by R. Ferrari and A. Massironi

By using a mixture of gold and aluminum bonding wires in the same IC, SGS-THOMSON has found a reliable way to correct very high current ICs that avoids wasting die area.

One of the essential prerequisites for the large-scale introduction of multiplex wiring systems for vehicles is the availability of high power integrated circuits (ICs) capable of replacing relays, driving directly lamps, motors and solenoids. These ICs must be rugged and highly reliable yet inexpensive. Many power ICs suitable for this market are already available but a gap was left at the high current — roughly 4A+ — end of the range; ICs delivering 20A or more are needed for loads like windowlift motors.

One of the main problems in high current IC design lies in the thin wires that connect the silicon chip itself to the external connections of the IC package. These bonding wires are typically fine gold wires (up to 50um thick) which cannot carry more than a few amperes of current.

Increasing the thickness of the gold wires is ruled out partly because of cost, and also because they are too rigid to weld to the surface of the chip without damaging it. It is possible in theory to use two or more gold wires in parallel for each connection but this solution is generally impractical because the large number of bonding pads waste space on the chip (the cost of a silicon chip is proportional to its area), the cost of the wire is excessive and because testing each bond is difficult.

Figure 1: Part of an almost completed strip of integrated circuits utilizing the new mixed bonding technology. The gold and aluminum wires connecting the silicon chip — the small gray rectangle — with the gold-plated external connections can be clearly seen.

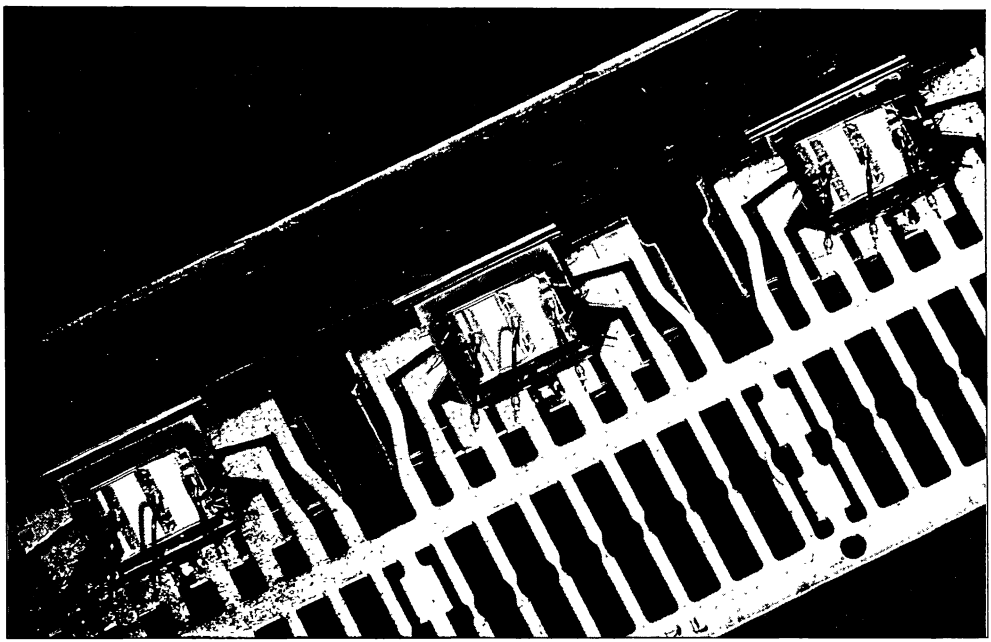
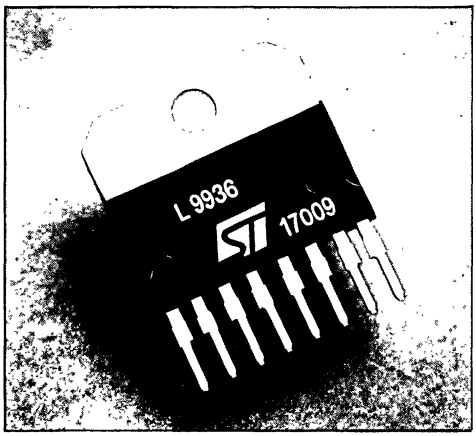


Figure 2: After the wire bonding operation the completed frame assembly is encapsulated in black plastic resin and the parts of the metal frame that served as a mechanical support are removed. The finished parts are then tested and marked with the type number and lot tracing information.



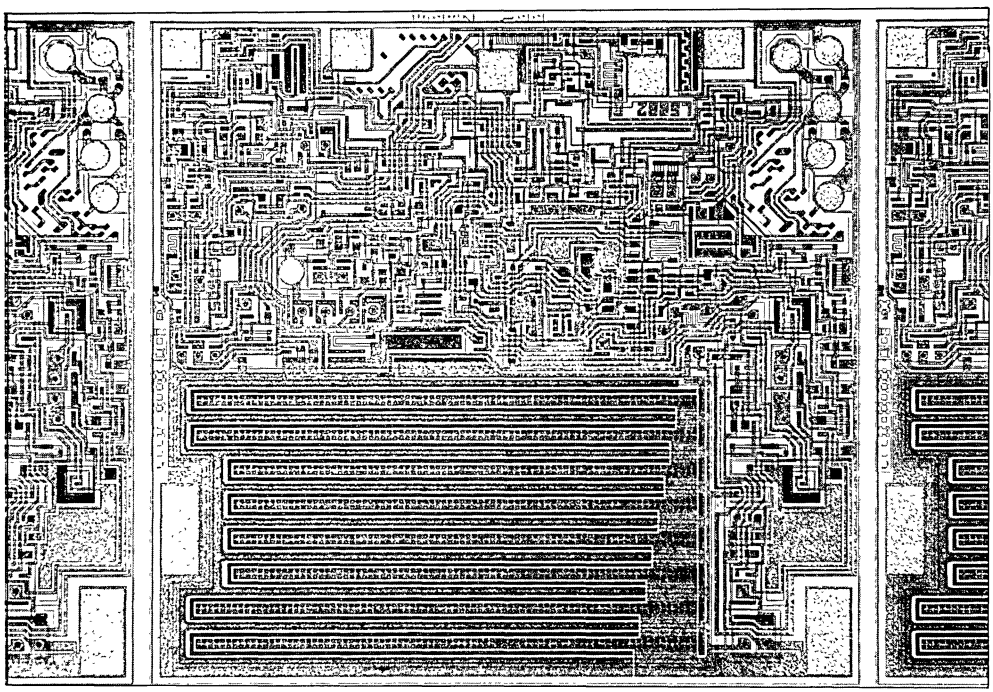
One alternative, widely used in simple power ICs, is to use thick (250um) aluminum wires. However, a thick aluminum bonding wire needs a large bonding pad on the die. In a simple device like a 3-terminal voltage regulator this is not a problem because there are few such pads, but for more complex ICs with eight or more connections the wasted silicon area would be excessive.

SGS-THOMSON has developed and industrialized an effective and efficient solution to this problem: a mixed bonding technology where thin gold wires are used for low current connections and thick aluminum wires used for power connections. Figure 1 shows a bonded frame of a 20A windowlift motor driver that uses this method; the two types of bonding wire can be clearly seen. Figure 2 shows the same IC after encapsulation with black molding resin and removal of the support elements of the frame.

Because of the use of aluminum bonding wires a selective gold alloy plating of the leadframe is necessary; gold is one of the few metals that will weld reliably to aluminum. Apart from reasons of cost, gold plating is used selectively — rather than the simpler overall plating — because of gold were used on the external lead part of the frame it would contaminate the circuit board soldering bath, leading to possible reliability problems.

Different bonding techniques are used to weld the

Figure 3.



two types of wire to the surface of the silicon chip. For the thin gold wires the thermosonic method is used where an electric discharge first creates a small ball on the free end of the wire, this ball is then pressed on to the bonding pad and vibrated rapidly (in the ultrasonic range), causing the gold ball and silicon surface to weld together.

The thicker aluminum wires are bonded using the simpler ultrasonic method, where the wire is simply pressed onto the surface of the chip then vibrated rapidly to weld the wire to the pad. Because more vigorous vibrations are used in this technique the aluminum wires are bonded first, followed by the gold wires. On the production lines two separate machines are used in tandem.

Reliability is an important consideration in automotive ICs therefore it is essential that wire bonds be secure throughout the lifetime of the circuit. To ensure that bonds are correctly executed some parts are subjected to a pull test, where the wires are pulled to determine their breaking strength. Gold wires must resist a force of at least 15g; the thicker aluminum wires must resist a pull of 130g. In both cases the wire must break; the bonds must not detach.

These pull tests are also repeated on statistical samples after accelerated life testing where parts are subjected to humidity, thermal cycling, and other stresses.

Mixed bonding technology can be used in various different power IC packages, though the photos here show the Multiwatt-8 package. This type has eight leads in line at 0.1" centers — wider than is usual — to suit high current circuits where wide circuit board tracks are used. The metal frame design of such packages reflects the care taken to ensure reliability in line with the needs of the auto market. For example, the die-mounting zone of the frame is isolated mechanically by notches and groove from the external mounting tab area. This ensures that deformation caused by overtightening the mounting screw will not subject to stress that could adversely affect reliability.

CAR IGNITION WITH IGBTs

by M. MELITO

ABSTRACT

IGBTs are now being used in a variety of switching applications due to their attractive characteristics, particularly their peak current capability, ruggedness and gate driving circuit.

Up to now their use was limited to the electrical drive sector and the IGBTs were required to be fast like the power MOSFETs and to have low conduction losses like the BJTs.

Automotive ignition switches are not required to be very fast because of low frequency at which they have to work. They must have very low $V_{CE(sat)}$ and must be very rugged. In both cases the existing technology allows us to obtain an acceptable compromise in terms of switching speed, ruggedness and power dissipation.

Moreover the structural characteristics of IGBTs lend themselves to future developments like low threshold devices for easier driving, integrated temperature and current sensing, gate to emitter and collector to gate voltage clamping, thus providing significant improvement in ruggedness, reliability, protection and system cost reduction.

This paper gives a brief explanation of the physics and of the structure of the device and highlights the characteristics which make IGBTs a very attractive competitor for the present power switches in automotive ignition.

IGBT TECHNOLOGY AND CHARACTERISTICS

Except for the p^+ substrate, the silicon cross section of an IGBT (fig. 1) is virtually identical to that of a standard power MOSFET. Both devices have the same cellular design with p^-/p^+ body, n^+ source and polysilicon gate structure. In both devices the n^- material under the p bodies is sized in thickness and resistivity to sustain the full voltage rating of the device.

Even if their structure is quite similar, the physical operation of the IGBT is different from that of the power MOSFET. In fact the IGBT is a minority carrier device and its physical operation is closer to that of a bipolar transistor than to that of a power MOSFET. This is due to the p^+ substrate which, during conduction, injects holes in the n^- region drastically reducing its resistivity.

Due to conductivity modulation, IGBTs allow power loss saving compared to power MOSFETs and have increased efficiency with respect to a bipolar transistor because the emitter covers the entire area of the die.

As for the switching speed the IGBT is in general not as fast as a power MOSFET but this is not a limiting factor because of the very low switching frequencies used in automotive ignition.

Due to the sandwiched layers of the device, the area with the extra p^+ layer forms a pnp bipolar transistor which controls the fall time of the IGBT. During turn-off the BJT portion has open base switching and switching terminates by the recombination of excess minority carriers.

Consequently the turn-off is dominated by the lifetime of the minority carriers in the n^- region.

In order to improve the fall time in IGBTs, techniques such as electron beam irradiation and doping with lifetime killers have been used to control the lifetime of minority carriers. Structural design changes, by the insertion of a n^+ buffer layer have also been introduced. The optimization of these techniques in IGBTs has allowed t_{fall} and $V_{CE(sat)}$ "tuning" (fig. 2), thus achieving the best trade-off between switching speed, power losses and ruggedness over a wide range of applications.

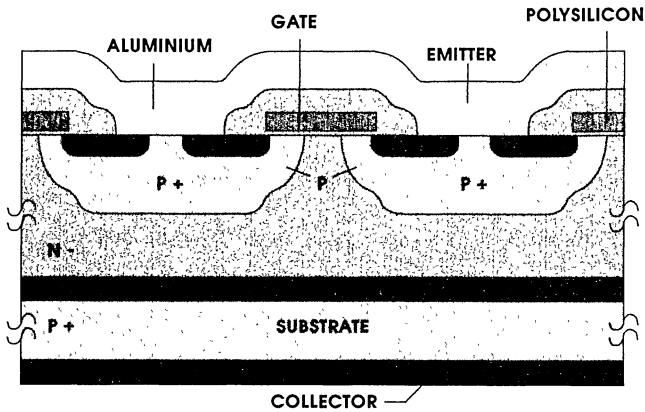


Figure 1: IGBT basic structure

Output characteristics

In a first order approximation the IGBT can be modelled as a pnp transistor driven by an n-channel power MOSFET (fig.3). This model is very simple and does not take into account second order effects, due to the common power MOSFET drain and BJT base region, but is useful to explain the IGBT characteristics.

As is apparent from the equivalent circuit, the voltage drop across the IGBT is the sum of two components: a diode drop across the p/n junction and the voltage drop across the driving Power MOSFET. Thus, like a Darlington, the on-state voltage drop across an IGBT never goes below a diode threshold voltage. As in the final stage of a pseudo-Darlington, the PNP is never in heavy saturation and its voltage drop is higher than that obtained from the same PNP in heavy saturation. It should be noted, however, that the emitter of an IGBT covers the entire area of the die, hence its injection efficiency and conduction drop are superior to that of a bipolar transistor of the same size. The typical output characteristics of an IGBT are given in fig.4.

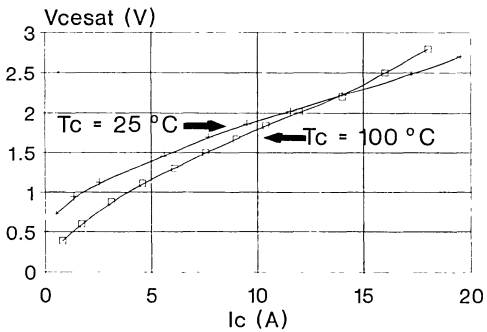


Figure 2: $V_{CE(sat)}$ versus t_{fall}

Temperature coefficient

The IGBT has a temperature coefficient of $V_{CE(sat)}$ that looks like a bipolar transistor up to approximately $I_{c\ max}$. At that point the temperature coefficient becomes zero. At collector currents greater than $I_{c,max}$, the temperature coefficient becomes positive and looks like a Power MOSFET. A typical temperature coefficient of $V_{CE(sat)}$ as a function of collector current for two junction temperatures are given in fig.5.

Switching

Due to the similar structure the switching behaviour of IGBTs for same aspects looks like the Power MOSFET one being affected by the unavoidable intrinsic capacitances of the device.

In the same way the main parameters governing switching behaviour are the gate bias, the driving impedance, the gate charge and the stray inductances.

Unlike the Power MOSFET the influence of the driving circuit on the current fall-time of IGBTs is negligible.

Turn-on

The turn-on behaviour of the IGBT is very similar to that of a Power MOSFET and in a similar way it is possible to control the turn-on time by the gate voltage and by the impedance of the driving circuit.

Turn-off

The IGBTs turn-off, shown in fig.6, can be divided into three consecutive phases:

a) the gate voltage begins to decrease until it reaches the value when the Miller effect occurs; during this phase the collector voltage increases slightly changing the output characteristics with I_c = constant.

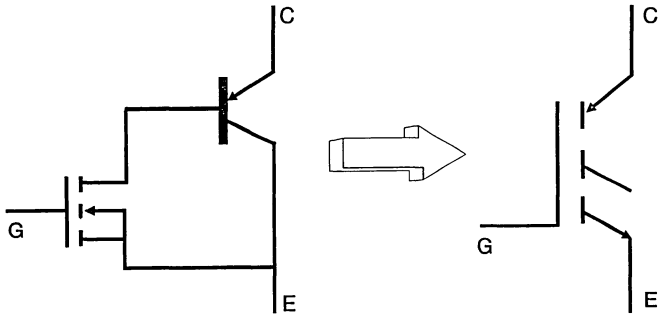


Figure 3: IGBT simplified equivalent circuit and JEDEC symbol

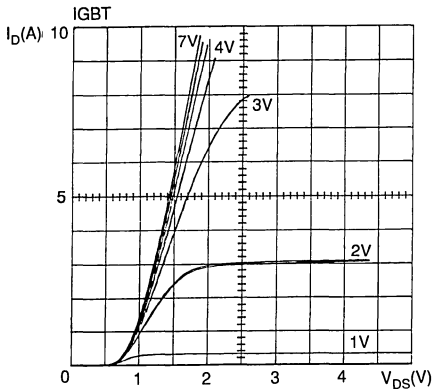


Fig. 4: IGBT Output characteristics

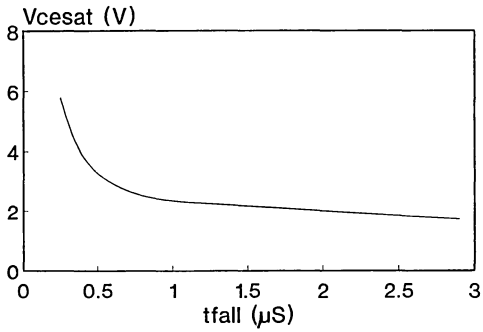


Fig. 5: $V_{CE(sat)}$ versus I_C

b) this phase is the Miller effect and the gate voltage remains constant because of modulation of the collector gate capacitance. This is due to collector voltage rapidly increasing to its maximum value.

c) the collector current begins to fall quickly then it continues with a tail which is due to recombination of minority carriers in the substrate.

The current tail, which causes the major switching losses, is strongly related to technology and its effect can not be mitigated by the driving circuit. The faster part of the collector current is due to the turn-off of the MOS portion of the IGBT structure. This part is connected to the PNP current gain which, for ignition devices, is designed to be relatively high to obtain a lower $V_{CE(sat)}$. The lower $V_{CE(sat)}$ is paid for with a longer current tail, refer to fig. 2. The price of this is acceptable because switching losses are negligible and because of the low switching frequency, compared to the losses during the on-phase and during current regulation. Moreover a very low $V_{CE(sat)}$ is imperative to allow the engine to start when the battery voltage is at its lower limit.

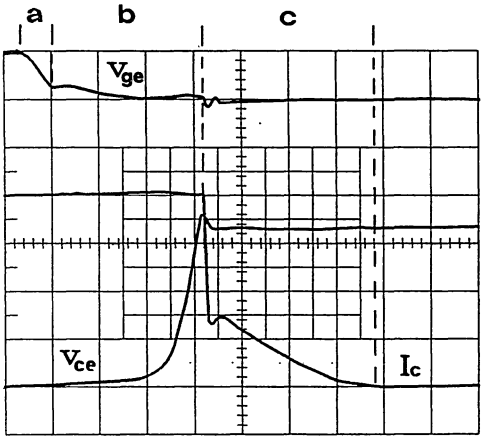


Fig. 6: IGBT turn-off

HOW AN IGNITION SWITCH MUST BE SPECIFIED

An automotive ignition switch must meet certain specifications concerning voltage and current rates, minimum energy handling capability in case of spark plug disconnection and driving requirements, over the whole operating temperature range.

The main requirements are related to:

1) breakdown voltage
2) current and saturation voltage
3) safe operating area
4) input characteristics.

Breakdown voltage

A pulse of 250V-300V on the primary side is normally more than enough to activate a spark. Of course the voltage peak on the spark plug will reach 20kV or more, because of the turns ratio, before the spark is actually ignited.

Just after that, both the primary and secondary voltages collapse and during the spark they stay significantly lower than the peak. Consequently the protecting zener can not be made to operate below 350V, to make sure that the voltage pulse will be high enough.

The switch breakdown voltage, that must never be reached, is therefore to be specified at least 50V higher than the zener breakdown to have a reasonable safety margin.

A wide range of IGBTs are actually in fully production covering BVces ranges from 400V to 1500V.

Current and saturation voltage

The current density of an IGBT rated at 500 V and 8A is up to two times greater than a bipolar transistor with comparable ratings in terms not only of breakdown and saturation voltage but also in terms of safe operating area. Consequently it is possible to achieve the same performance as a standard ignition Darlington with a smaller silicon area or alternatively to have a better thermal resistance.

Safe Operating Area

The safe operating area describes the capability of a transistor to withstand significant levels of voltage and current at the same time.

There are two main conditions that would subject an ignition switch to this combined stress:

a) In normal operating conditions the falling edge of the collector current during turn-off causes the collector voltage to rise until the spark occurs.
   During this phase the ignition switch has to withstand, at the same time, high voltage and high current levels, without

either damage or reliability degradation. This can be achieved only if the voltage and current levels are within the boundaries of the guaranteed turn-off safe operating area (RBSOA). Otherwise an network is required to shape the voltage and current waveforms.

The actual technology allows the production of IGBTs having a square RBSOA whose voltage boundary is the BVces and the current limit is at least two times the nominal current of the device thus avoiding any need for a network.

b) In case a spark plug is disconnected the ignition switch must be able to absorb the energy that the coil can not release to spark. All the stored electromagnetic energy tends to concentrate across circuit parasitic capacitances charging them up to high voltages and putting the device in avalanche with risk of going into second breakdown and failing. This problem is overcome dissipating this energy stress on the power switch by a protection zener put between the collector and the device base which turns the device on as soon as the collector voltage exceeds the nominal zener voltage. The usual way to indicate the minimum energy the switch can absorb without damage is to specify the battery voltage, the coil inductance and coil current, the clamp voltage for the zener and, if present, the collector-to-emitter capacitance.

This kind of specification is usually referred to as the "use test" and it can be easily guaranteed for the IGBTs.

Input

The ignition switch must be specified to ensure that the current and voltage available from the driving stage are enough to switch it on and off under all temperature conditions. The input characteristic of IGBTs is a MOS characteristic thus requiring a very small amount of energy for switching. The IGBTs require a driving energy that is at least two orders of magnitude lower than the Darlington's.

Moreover the recently introduced logic level IGBTs, STGP10N50L or equivalent, can be turned on with a gate voltage as little as 3V.

IMPROVEMENTS

The structural characteristics of IGBTs lend themselves to further improvements in similar ways to the developments made in power MOSFET technology.

Logic level IGBTs are available and they can be directly interfaced to CMOS, TTL, PMOS and NMOS logic circuits and microprocessors operated from 5V supplies.

Moreover temperature sensing, current sensing, gate to emitter and collector to gate voltage clamping can be designed into IGBTs at the cost of a small increase of the silicon area and the addition of only one masking layer to the process.

The functions that can be obtained provide significant improvement in ruggedness, reliability, protection and system cost reduction.

CONCLUSION

IGBTs are high voltage power switches which can work at very high current densities. They are simple to drive and are intrinsically rugged.This, coupled with the potential to integrate functions such as device protection and other reliability enhancing features, make them potentially very aggressive competitors in the automotive ignition field.

REFERENCES

[1] M. Melito, *Power Switches for Automotive Ignition*, IEE Colloquium on Power Integrated Circuit, Digest no: 1989/34, March 1989.

[2] M.W. Smith, *Applications of Insulated Gate Transistor*, PCI Proceedings , April 1984.

[3] D-S Kuo, J-Y Choi, D. Giandomenico, C Hu, S.P. Sapp, K.A. Sassaman and Bregar, *Modelling the turn-off characteristics of the bipolar-mos transistor*, IEEE Electron Device Letters, vol. EDL.6, N°5, May 1985.

[4] R. Letor, M. Melito, *Safe behaviour of IGBTs subjected to dV/dt*, PCI Proceedings, June 1990.

[5] A. Galluzzo,R. Letor, M. Melito, *Switching with IGBTs: how to obtain better performances*, PCI Proceedings, June 1991.

SGS-THOMSON MICROELECTRONICS

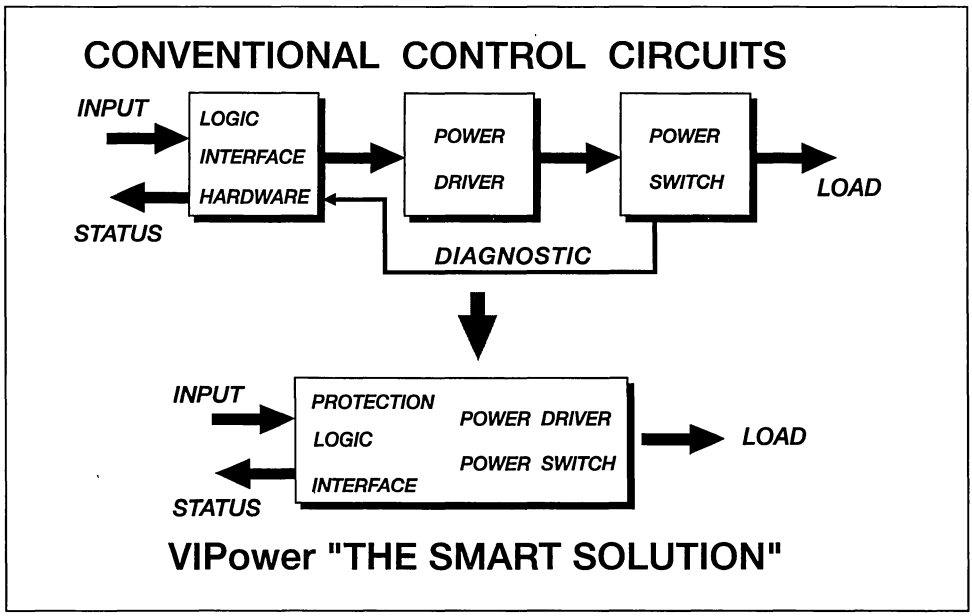
APPLICATION NOTE

HIGH SIDE DRIVERS

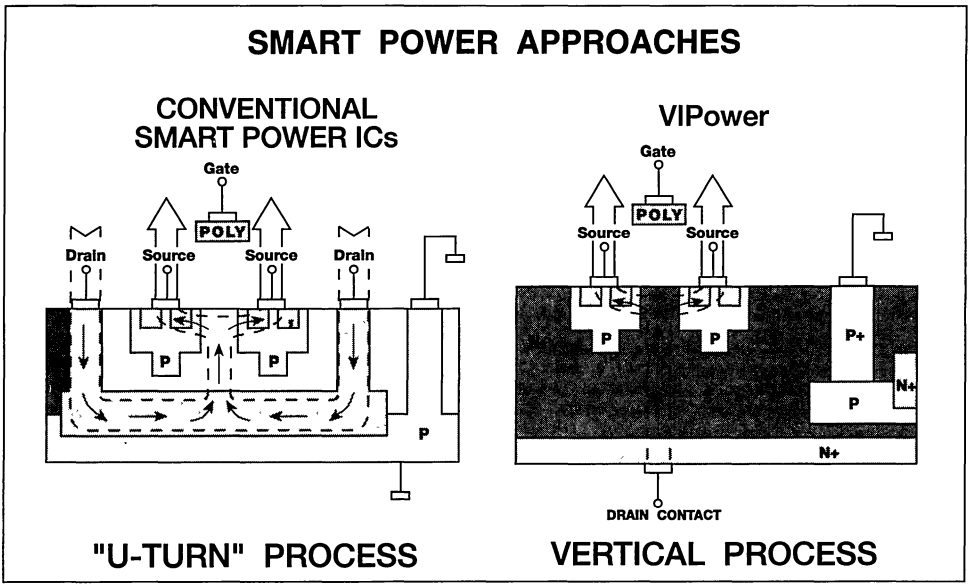
by A. Russo
B. Bancal
J. Eadie

INTRODUCTION

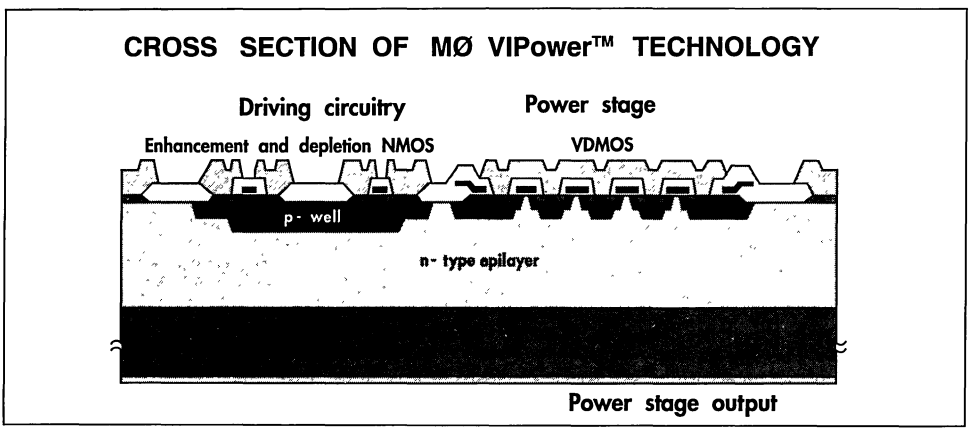
The ever increasing demand for cost reduction and higher levels of circuit complexity and reliability have directed the semiconductor manufacturer's attention towards smart power technologies which allow the production of totally integrated monolithic circuit solutions that include a power stage, control, driving and protection circuits on the same chip.



Vertical intelligent power, (VIPower ™) an SGS-THOMSON Microelectronics patented technology, established over 7 years ago, uses a fabrication process which allows the integration of complete digital and/or analog control circuits driving a vertical power transistor on the same chip. The power handling capability of this type of structure compares favourably with monolithic smart power devices of equivalent chip size which use lateral, or "U-turn" power output structures.



The VIPower technology M0 used for making these High Side Drivers produces a monolithic silicon chip which combines control and protection circuitry with a standard power MOSFET structure where the power stage current flows vertically through the silicon.



High Side Drivers, with their integrated extra features are power switches that can handle high currents and work up to about 40V supply voltage. They require only a simple TTL logic input and incorporate a fault condition status output. They can drive an inductive load without the need for a freewheeling diode. For complete protection the devices have an over-temperature sensing circuit that will shut down the chip under over-temperature conditions. They also have an under-

voltage shutdown feature. It is simple to introduce some differences in the control logic to produce devices with features which cater for different working environments.

Each application exerts an external influence over the switch. A filament lamp or DC motor, for example, have in-rush currents that any switch has to handle. Solenoids and motors have an inductive effect and must lose the residual magnetism when the current is turned off. This gives rise to induced voltages and the need to remove this stored energy. External fault conditions can also stress the drivers and their associated circuitry. The following discussion has been designed to explain the basic principles involved in using these devices and to help to understand how they react under the influence of various applications.

Almost every electronic switch used in a modern automobile application is a high side switch. This configuration is preferred for automotive use because:

a) - This configuration protects the load from continuous operation and resulting failure, if there is a short circuit to the ground. Since the body of a car is metal and 95% of the total car is ground, the short to ground is much more common than short to V_{CC}

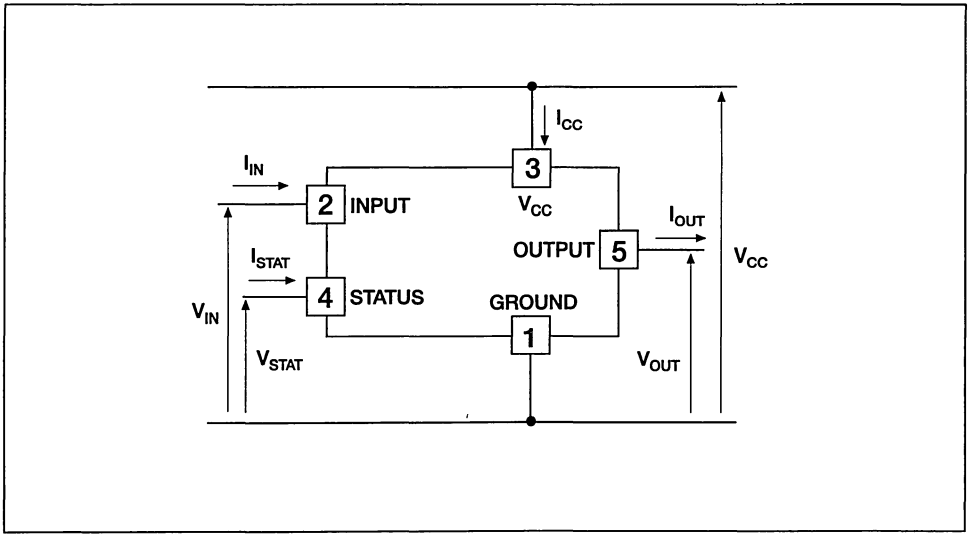
b) - High Side Drivers cause less problems with electrochemical corrosion. It is of primary importance in automotive systems because the electrical components are in an adverse environment, specifically adverse temperatures and humidity and the presence of salt. For this reason the series switch is connected between the load and the positive power source. Therefore when the electrical component is not powered (that is for the greatest part of the lifetime of the car) it is at the lowest potential and electrochemical corrosion does not take place.

Integrated High Side Drivers offer numerous advantages over the popular automotive relay used in cars today. Diagnostic information output from the High Side Driver helps the on-board microcontroller to quickly identify and isolate faults saving repair time and often improving safety. High Side Drivers can reduce the size and weight of switch modules, and where multiplexed systems are used, dramatically reduce the size of the wiring harness.

Process control applications offer another use for High Side Drivers. A considerable improvement in reliability and reduction in down time can be obtained by using them in place of relays. Process control systems, often consisting of powerful computers that control large numbers of actuators, are perfect environments for these devices. The semiconductor manufacturer has little control over the nature of the load being driven and these can vary - solenoids, motors, transducers, leds. In these situations, software process monitoring by a µP can detect a fault reported by a status output and offers the option of taking corrective action. In the unlikely event of a failure in a High Side Driver in critical processes, a second device can be programmed to operate instead.

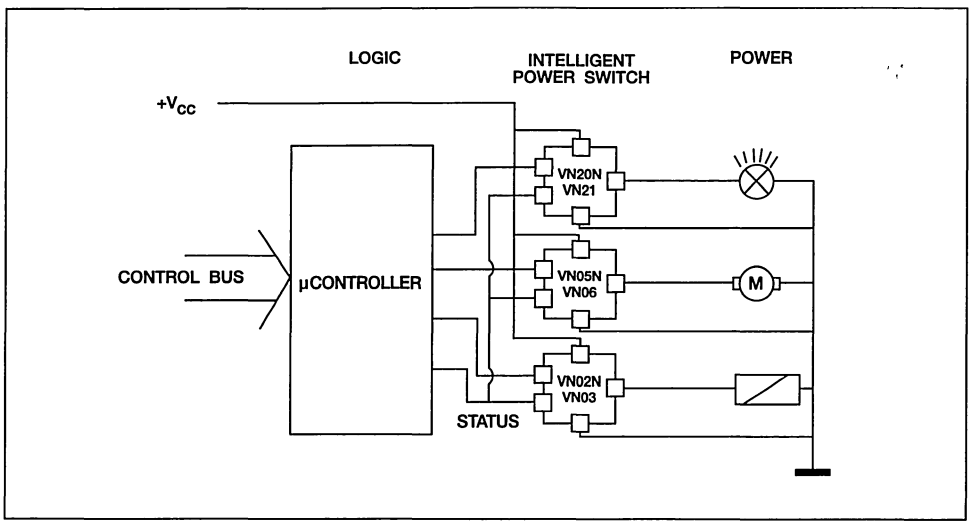
SGS-THOMSON High Side Drivers are designed to provide the user with simple, self protected, remotely controlled power switches. They have the general structure as shown in figure 1. Appendix I shows a table of the devices and summarizes their features.

Figure 1 : Standard current and voltage conventions



Some typical applications are shown in figure 2.

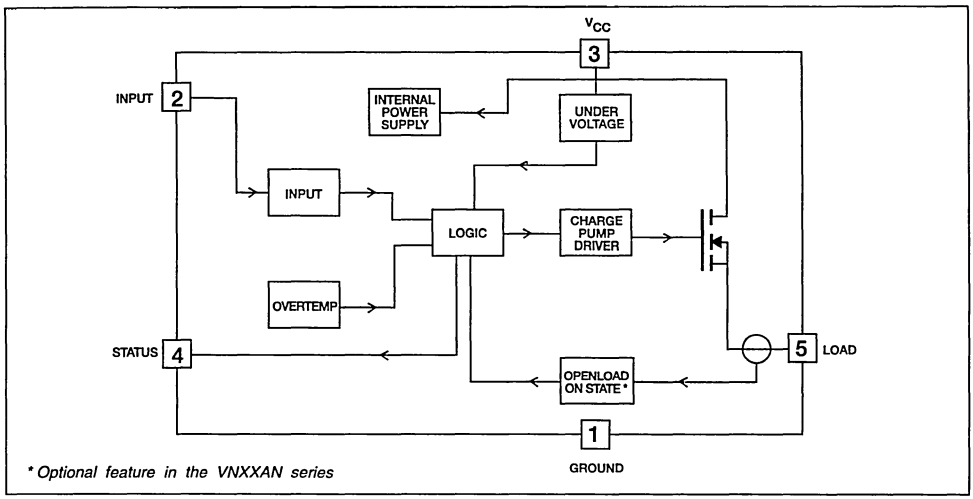
Figure 2 : High Side Drivers interfaces between control logic and power load



THE GENERAL FEATURES OF HIGH SIDE DRIVERS.

The diagram in figure 3 shows the control and protection circuit elements and the power stage of a basic device.

Figure 3 : Generic Internal Block Diagram



Input

The 5V TTL input to these High Side Drivers is protected against electrostatic discharge. General rules concerning TTL logic should be applied to the input. The input voltage is clamped internally at about 6V. It is possible to drive the input with a higher input voltage using an external resistor calculated to give a current not exceeding 10mA at the input.

Internal power supply

To accommodate the wide supply voltage range experienced by the logic and control functions, these devices have an internal power supply. Some parts of the chip are only active when the input is high, the status output and charge pump for example. This means it is possible to conserve power when the device is idle. The internal power supply has therefore been designed in two parts. One section supplies power to the basic functions of the chip all the time, even when the input is 0V. The second section supplies power only when the input is high. This ensures that the stand-by current is limited to 50µA maximum in the off-state.

THE CONTROL CIRCUIT.

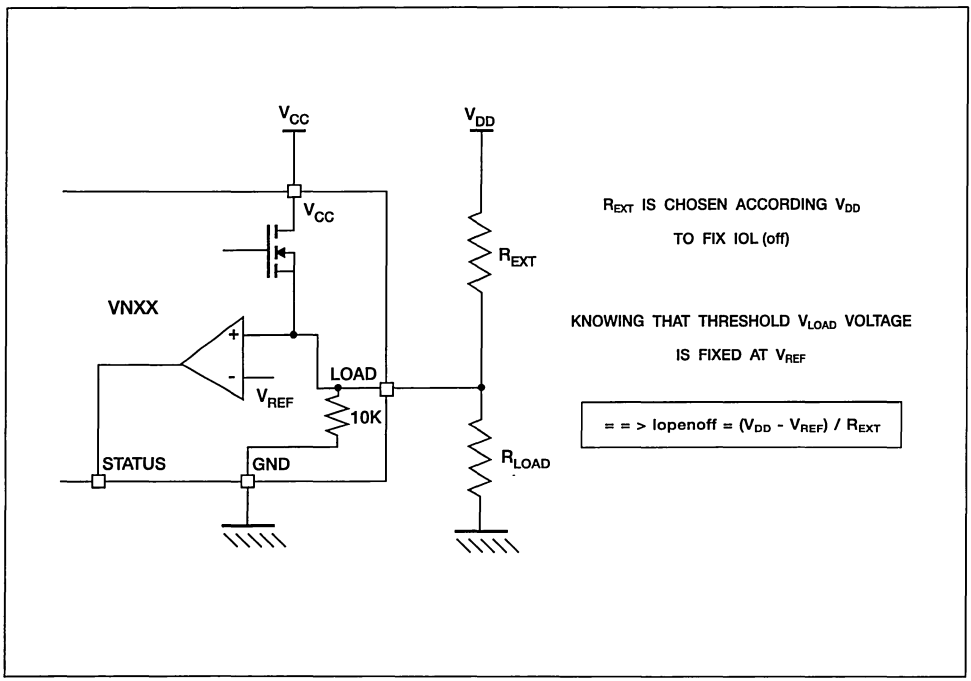
Under voltage lock-out.

Under-voltage protection occurs when the supply voltage drops to a low level specified in the datasheet as V_{USD}. The under-voltage level set at this value ensures the device functions correctly. Inductive effects must be considered in understanding the function of this feature. The di/dt is controlled by the device and not by the external circuit. The controlled value is calculated for a line inductance of 5µH(≃5mt. of wire). Typically di/dt=0.5A/µs for a normal load and 1A/µs for a short circuit. At turn on this generates an opposing voltage. If this opposing voltage is too large, the apparent supply voltage will drop below the under-voltage lock-out level and the device will turn off. Using the specified conditions, the induced voltage will not be large enough to reduce the supply voltage below 6V. This is important in the case where the load is a near short circuit when in-rush current occurs, as in the case of a car headlamp filament turning on.

Open load detection and stuck-on to V_{CC}. Open load detection occurs when the load becomes disconnected. In the VN20N family open load detection only occurs in the on-state.

An extra feature for load disconnection detection is that open load detection during the off-state as well as in the on-state can be provided. The circuit for the off-state open load detection requires an external resistor between V_{CC} and the output pin.

Figure 4 : Equivalent Schematic for the open load detection current in off-state



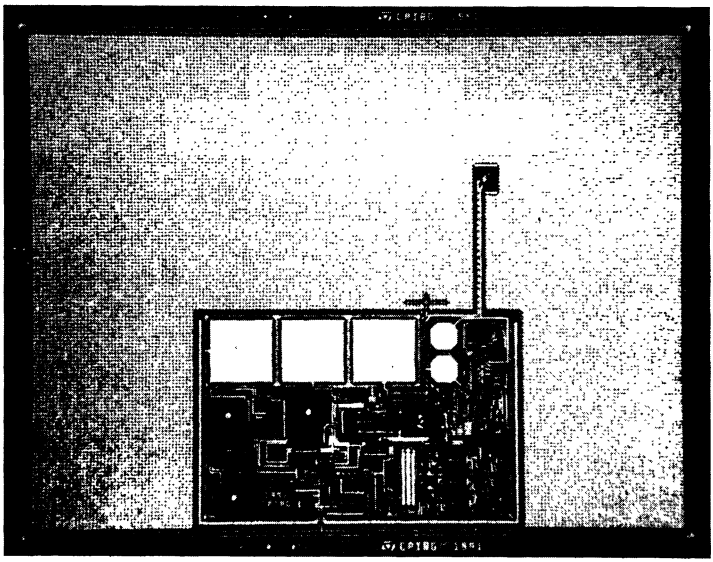
Open load detection is possible in the off-state in the VN21 family and it conforms to the I.S.O. norms for automotive applications. If an open load condition is detected the status flag goes low. Should an external supply be applied to the load (output pin) or the device is externally short circuited, the off-state open load detection can detect this "stuck-on" to V_{CC} condition.

Over-temperature protection

Over-temperature protection is based on sensing the chip temperature only. The location of the sensing element on the chip in the power stage area, ensures that accurate, very fast, temperature detection is achieved. The range within which over-temperature cutout occurs is 140°C - 180°C with 160°C being a typical level.

Over-temperature protection acts to protect the device from thermal damage and consequently also limits the average current when short circuits occur in the load.

Figure 5 : VN20N Die Layout - Note the thermal sensor inside the Power MOSFET Area

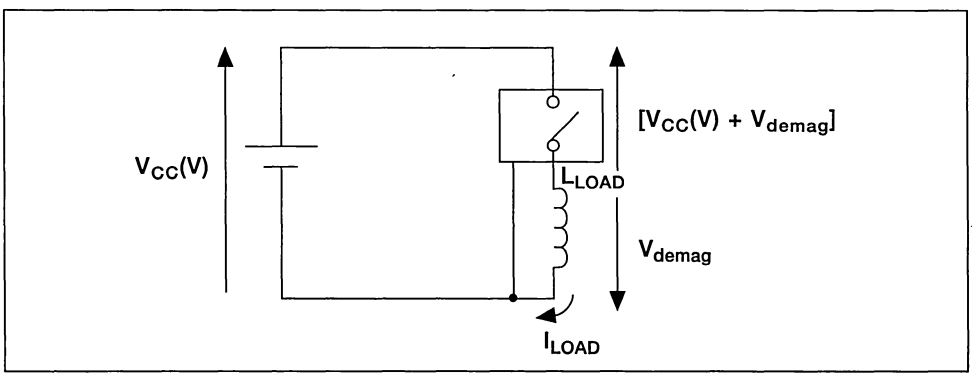


Driving the power MOSFET.
The power MOSFET output stage is driven by an internally generated gate voltage. A charge pump provides sufficient voltage to turn on the gate.

Turn-on
As previously explained, the High Side Drivers are turned-on with a controlled di/dt.

Turn-off: Normal and fast load demagnetization
When a High Side Driver turns off an inductance a reverse potential appears across the load.

Figure 6 : Inductive load demagnetization turn-off for the VN20N family



The source of the power MOSFET becomes more negative than the ground until it reaches the demagnetization voltage, $V_{demag.}$, of the specific device. In this condition the inductive load is demagnetized and its stored energy is dissipated in the power MOSFET according to the equation shown below:

$$P_{demag.} = 0.5\ L_{load}\ [I_{load}]^2 \cdot \frac{[V_{cc} + V_{demag.}]}{V_{demag.}} \cdot f$$

where f is the switching frequency and $V_{demag.}$ the demagnetization voltage.

In the basic High Side Driver family the typical value of, | Vdemag.| is = 4V.

In the I.S.O. and industrial series,to reduce the dissipated energy, an internal circuit has be added in order to have a typical | Vdemag. | = 18V.

In this condition the stored energy is removed rapidly and the power dissipation in the power MOSFET is reduced - see equation. Figure 7a/b compares the waveforms of the normal and fast demagnetization techniques.

Figure 7a/b : VN20N-VN21 Driving an Inductive Load

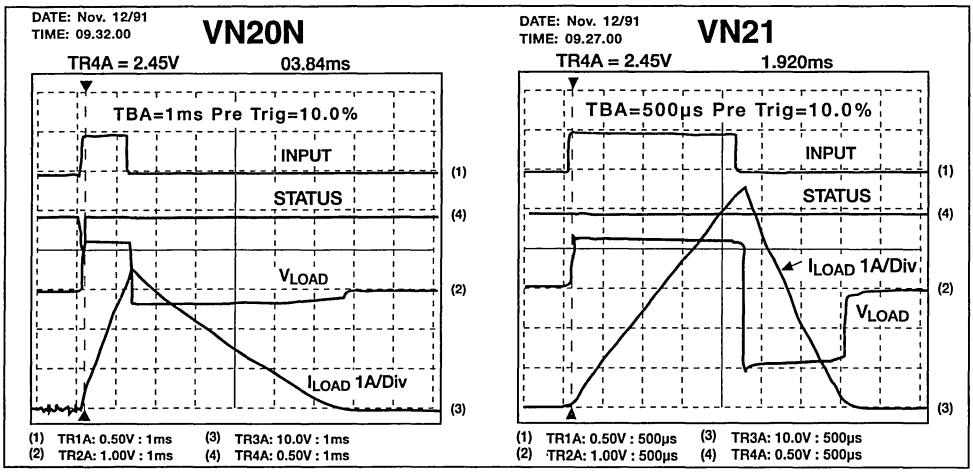
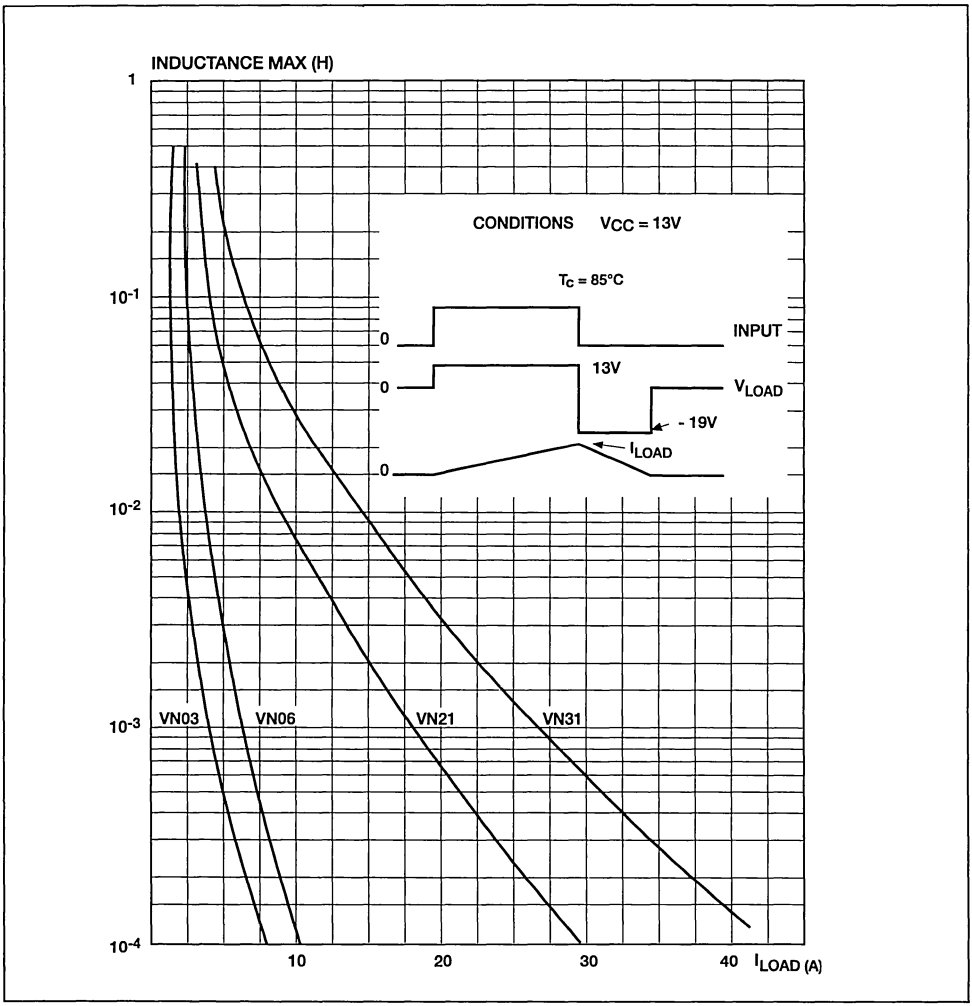


Figure 7b shows the VN21 driving an inductive load. During the on period, the current in the load rises linearly to a maximum. At turn-off the current decrease linearly, but, at a sufficiently fast rate for fast demagnetization of the load. There is no fault output from the status pin. In the VN20N, the basic High Side Driver with no special feature for fast demagnetization, the turn-off takes up to 5 times longer than the VN21. Note that the status output will pulse at turn on because the internal circuit detects a very short duration open load, see figure 7a.

The maximum inductance which causes the chip temperature to reach the shut down temperature in a specified thermal environment, is a function of the load current for a fixed V_{CC}, $V_{demag.}$ and switching frequency. This is the maximum rate at which the drivers can be demagnetized. Figure 8 shows the maximum inductance for a given load current for devices meeting I.S.O. requirements, assuming a chip temperature of 160°C at turn-off and a supply voltage of 13V. The values are for a single pulse with 85°C case temperature. Note that the devices are not protected against overtemperature during turn-off.

Figure 8 : Max inductance which produces a temperature of 160°C at turn off with Vcc = 13V. The values are for a single pulse with Tc = 85°C



Additional Features of the High Side Drivers

High Side Drivers are designed for use in various market segments, the precise requirements of the drivers varying a little with the application. There are additional features to accommodate these requirements.

To reduce the on-state quiescent current for some applications, particularly industrial ones, the open load detection circuit is not included. There will consequently also be a lower power dissipation, an important point when similar, multiple High Side Drivers are mounted on one board. It can means the difference between using or not using a heatsink.

The operating voltage range can vary e.g. 5.5V to 26V for automotive applications and 7V to 36V for process control. Some devices have fast demagnetization of the load, ground disconnection protection, on- and off- state open load detection and 5ms filtering of the status output.

Status output and status output signal filtering.

The difference in electrical behaviour between the non-filtered and the filtered High Side Drivers is that the status output filtering circuit provides a continuous signal for the fault condition after an initial delay of about 5ms in the filtered version. This means that a disconnection during normal operation, with a duration of less than 5ms does not affect the status output. Equally, any re-connection during a disconnection of less than 5ms duration does not affect the status output. No delay occours for the status to go low in case of overtemperature conditions. From the falling edge of the input signal the status output initially low in fault condition (overtemperature or open load) will go back high with no delay in case of overtemperature condition and a delay t_{POL} in case of open load. These features fully comply with International Standards Office, (I.S.O.), requirements for automotive High Side Drivers.

ABNORMAL LOAD CONDITIONS:

Load short circuits

Should a load become short circuited, various effects occur and certain steps need to be taken to deal with them, particularly choosing the correct heatsink. Two clear cases of short circuit occur:

1. The load is shorted at start-up.
2. The load becomes short during the on-state.

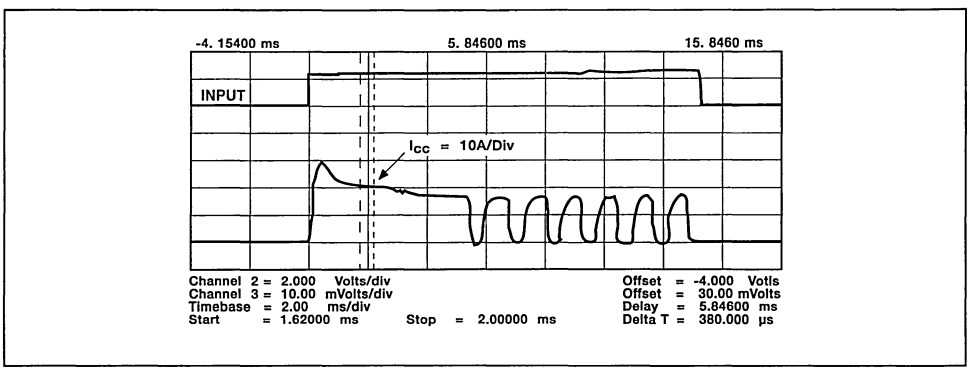
Start-up with the load short circuited.

At turn-on the gate voltage is zero and begins to increase. Short circuit current starts to flow and power is dissipated in the High Side Driver according the formula:

$$P_d = V_{DS} \times I_D$$

The effect is to cause the silicon to heat up. The power MOSFET stays in the linear region. When the silicon temperature reaches about 160°C the over temperature detection operates and the switch is turned off. Passive cooling of the device occurs until the reset temperature is reached and the device turns back on again. The cycle is repetitive and stops when the power is removed, the input taken low or the short circuit is removed.

Figure 9 : Automatic Thermal cycle at start - up with the load short - circuited.

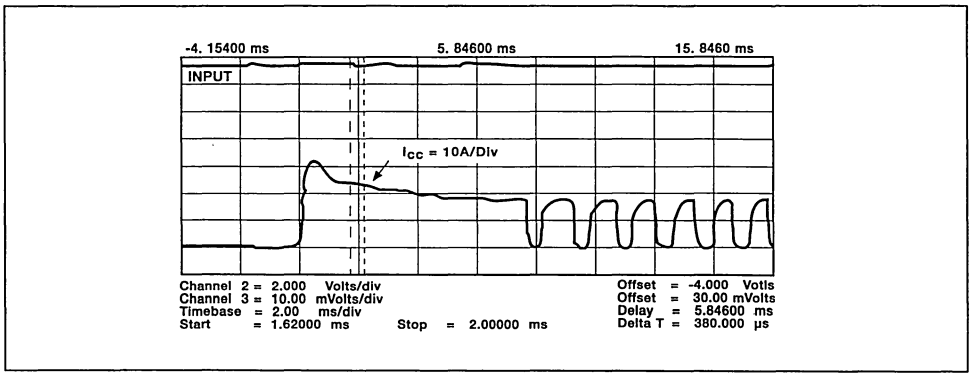


Even in this configuration, the device controls the di/dt. Figure 9 shows a start-up when there is a short circuited load driven by a VN05N. The initial peak current is 30A for this 180mΩ device.

A short circuit occurring during the on-state.

When a short circuit occurs during the on-state, the power MOSFET gate is already at a high voltage, about V_{CC}+ 8V, so the gate is hard on. Hence the short circuit di/dt is higher than in the first case, and only controlled by the load itself. After the steady state thermal condition is reached, thermal cycling is the same as in the previous case.

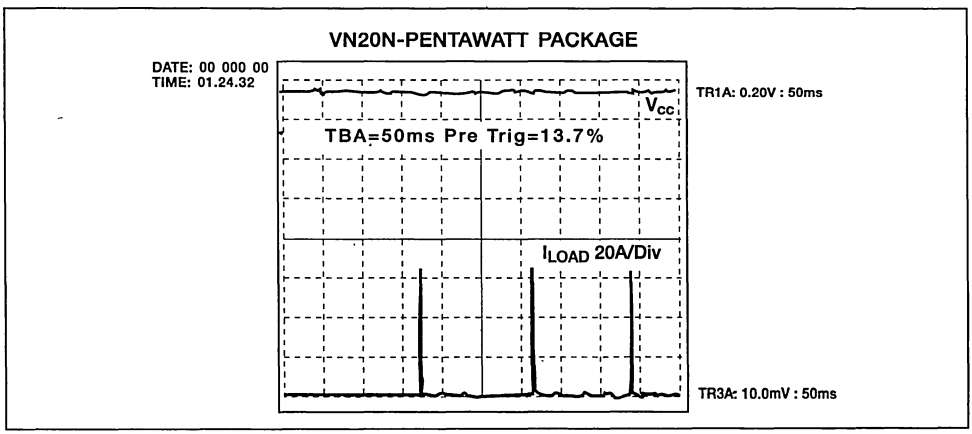
Figure 10 : Automatic thermal cycle for a short circuit occouring during the on - state



Automatic thermal cycle.

The thermal cycling in overload conditions produces repetitive current peaks. The device switches on, the silicon heats up until the over-temperature sensing acts to turn the device off. The rate of passive cooling depends on the thermal capacity of the thermal environment. This, in turn, determines the length of the off-state during thermal cycling.

Figure 11 : Automatic Thermal cycle in overload condition



It is important to evaluate the average and RMS current during short circuit conditions. This is required in order to determine the track dimensions for printed circuit boards and the correct value for any fuse used. In all practical situations there is no danger to pcb tracks from these high peak current for track designed to handle the nominal load current.

Evaluating the Average current

In steady state conditions the junction temperature oscillates between Tj (shutdown) and Tj (reset).

$Tj(av.)=(Tj(shutdown)+Tj(reset))/2 \approx 135°C$

Dissipated power:

$P_D = I_{(AV)} \times V_{CC}$

For a specific package

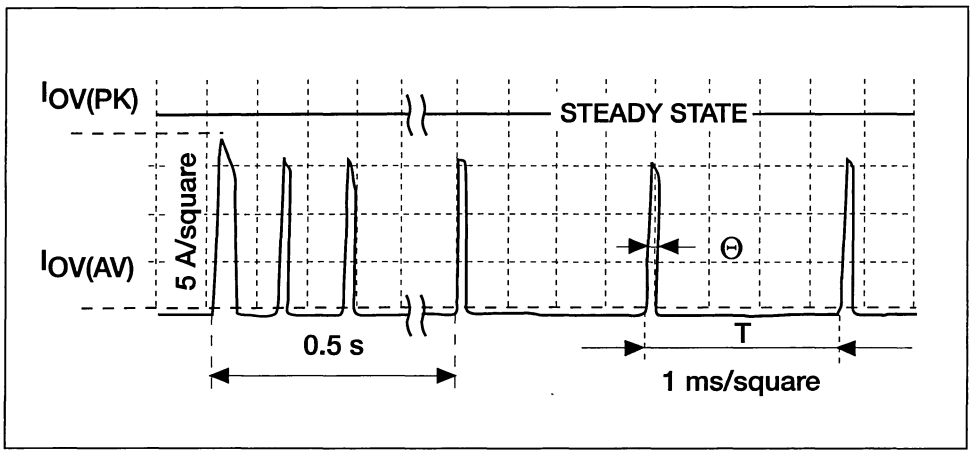
$P_D = (T_{J(AV)} - T_{case}) / R_{thj\text{-}case}$

$I_{(AV)}=(T_{J(AV)} - T_{case}) / R_{thj\text{-}case} \times V_{CC}$

Note that $I_{average}$ does not depend on the peak current $I_{(PK)}$.

Example:
VN21 with T_{case} = 85°C has an average current, $I_{(AV)}$ = 3.85A,
at $R_{thj\text{-}case}$ = 1°C/W and V_{CC} = 13V
The average current is independent of the peak current.
Generally, a current limiter does not decrease the average current.

Figure 12 : Average current during an hard short - circuit test



Evaluating the RMS current

The RMS current, I_{RMS}, generates heat in the copper track on PCBs during short circuits.

$$I_{(RMS)}^{\ 2} = 1/T\int_0^T I^2(t)dt$$

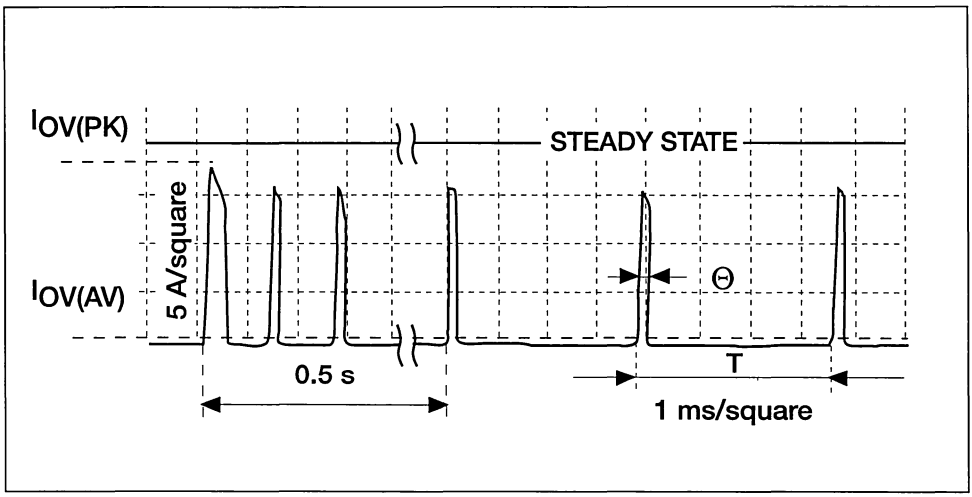
$I_{(RMS)} = I_{(PK)} \times \sqrt{\Theta/T}$, where Θ/T is the duty cycle.

with $I_{(AV)} = 1/T \int_0^T I(t)dt = I_{(PK)} \times \Theta/T$

$I_{(RMS)} = \sqrt{(I_{(PK)} \times I_{(AV)})}$

The RMS current increases proportionally to the square root of the peak current --> +40% if $I_{(PK)}$ is doubled. Schemes to limit the current do not decrease the RMS current significantly.

Figure 13 : RMS current during an hard short-circuit test



Heatsink requirements.
Overload protection is based on device heating. If you want to detect an overload, i.e a damaged load, the chip must be allowed to heat up so that the thermal sensor located on the chip is activated. This leads to the following general rules for sizing heatsinks for the VN High Side Drivers.

1. Do not use a too big heatsink.
2. Do not use a VN device which has R_{ON} much lower than that which the application requires.

This example illustrates a specific case.

Situation:
- a supply voltage of 14V,
- a load resistance of 2Ω,
- VN20N - $R_{DS(on)}$ at 25°C = 50mΩ
- load current = 7A

To detect an over current of 20A, assuming that $R_{DS(on)}$ at 150°C = 100mΩ (see datasheet) hence:

$$P_D = 20^2 \times 100^{-3} = 40W$$

$R_{thj\text{-}a}$ should be dimensioned for

$$\Theta_{\text{thermal shutdown}} - \Theta_{\text{Ambient}} < P_D \times R_{thj\text{-}a}.$$

For example 160°C - 25°C < 40W x $R_{thj\text{-}a}$

The effects of load disconnection.
When a load becomes disconnected there can be over-voltages caused by the change of load current. Figures 14a/b summarizes the likely effects. Figure 14a, shows a load driven by a VN21. The supply to the VN21 has a very low parasitic inductance. When the load becomes disconnected, the current changes at a rate determined by the time taken for the load to disconnect. This controls di/dt .

Figure 14a/b : Example of possibles situations during a load disconnection

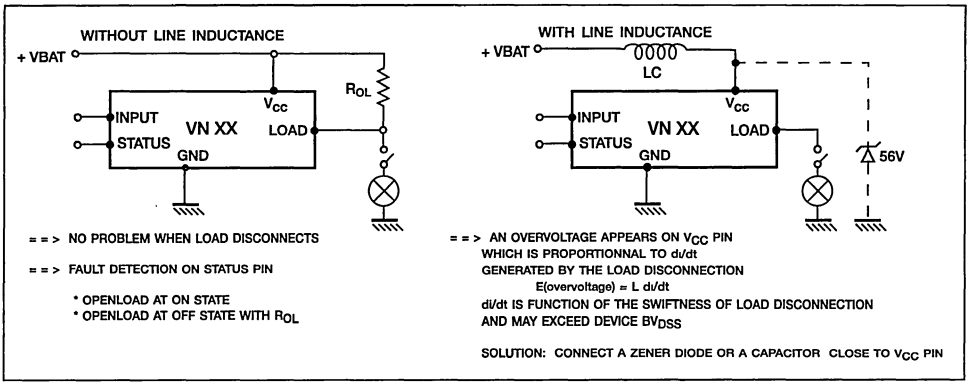
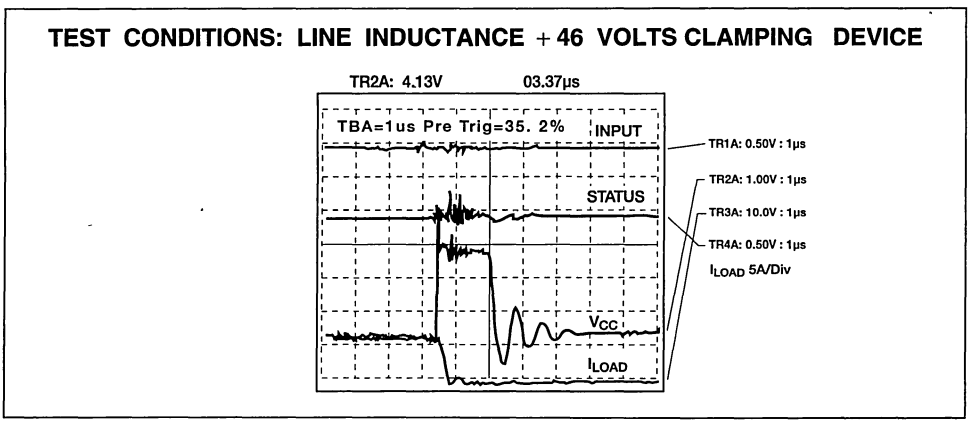


Figure 14c : Behaviour of a VN21 during a load disconnection



In this present case, there is virtually no inductance in the supply line. Hence no over-voltage is generated and V_{cc} is unaffected. The status pin goes low to indicate an open-load state

In the second case illustrated, figure 14b, the supply line has parasitic inductance and capacitance. When the load is disconnected an over-voltage is generated, ($V_{over\text{-}voltage}$ = L di/dt). The di/dt is not controlled by the device but by how fast the load is disconnected. It is possible that the over-voltage may exceed the breakdown voltage of the device. It is a wise precaution where the supply connection pins are likely to have some inductance, to use a 56V zener diode or a capacitor close to the supply pin of the switch. Figure 14c shows a test made using a zener clamp to overcome line inductance.

PROTECTION AGAINST GROUND DISCONNECTION

There are a number of distinct situations that can occur when one of the ground connections is broken in circuits using the High Side Drivers.

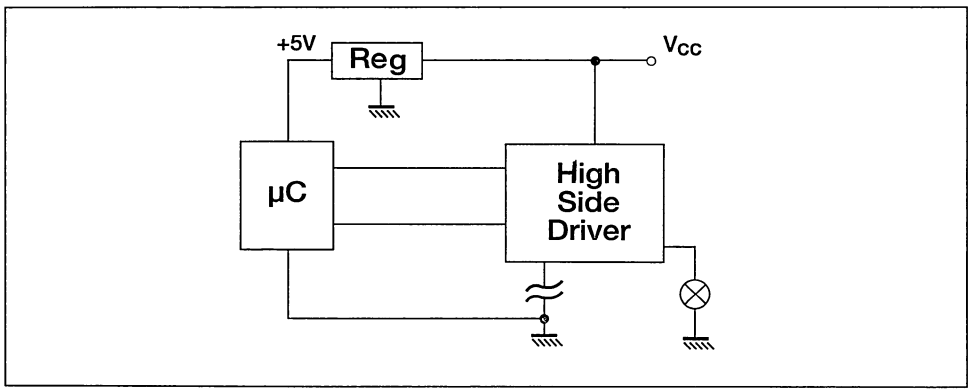
The first case, shown in fig. 15a, is when the GND pin of the High Side Driver is

disconnected while the µC and the load are connected to ground. In this case in the I.S.O. an industrial High Side Drivers nothing happens and the device remains off. In the VN20N family a voltage of about 2V appers on the load and conseguently there is a power dissipation:

$P_D = (V_{CC} - 2) \cdot I_{LOAD}$

usually very low. In these conditions the diagnostic is not functioning.

Figure 15a : Possible ground disconnection occurring when a High Side Driver is connected to a µController (case 1)

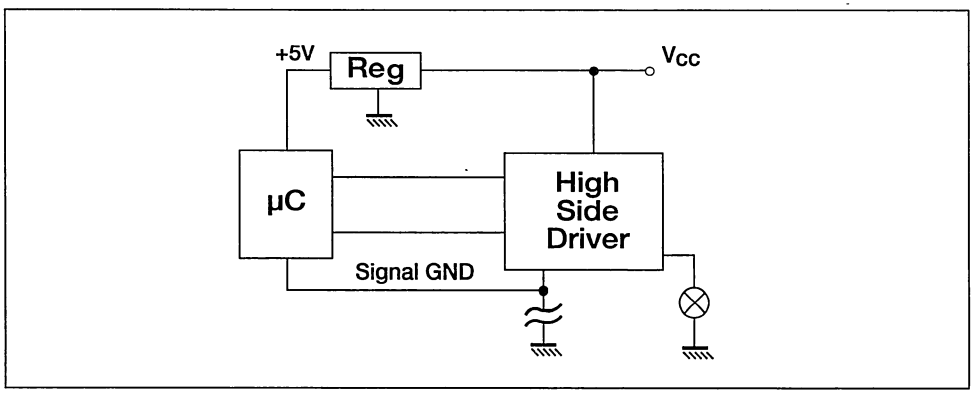


The second case, shown in fig. 15b, is when both the GND pins of the High Side Driver and of the µC are disconnected while the load is connected to ground. In this situation the signal GND rises up to V_{CC}. In the I.S.O. and industrial High Side Drivers nothing happens up to V_{CC}<18V and the diagnostic output remains in high state at V_{CC}. In the VN20N family a voltage of about 4V appears on the load and conseguently there is a power dissipation:

$P_D = (V_{CC} - 4) \cdot I_{LOAD}$

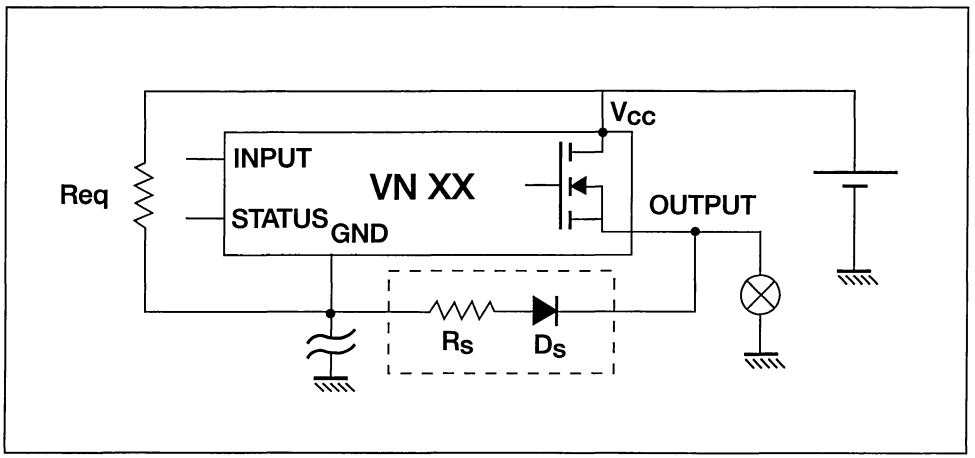
If P_D is excessive with respect to the heatsink capability, destruction may occurs since the protections are not functioning. The load is permanently activated.

Figure 15b : Possible ground disconnection occurring when a High Side Driver is connected to a µController (case 2)



Another practical case is when an external component supplies current to the High Side Driver GND pin which is disconnected from the ground. This might occur if the VN device is mounted on a local PCB with other devices and has a local ground while the load may be grounded to the frame or body of the equipment, figure 16. Also, in this case, for internally protected devices, the output remains off up to the point where the voltage on the GND pin is ≤ 18V with reference to real ground at 0V. This will reduce the maximum V_{CC} the High Side Driver is able to withstand before turning on with the control circuit in-operative. One solution to this problem is to insert a resistor and diode in between the device GND pin and the output pin. The series resistor, Rs, must be calculated so that the sum of the current, Is, of the High Side Driver chip connected to the GND node plus the current drawn by the external elements, produces a voltage drop of less than 18V across Rs + Ds + R_{load} for I.S.O. or industrial High Side Drivers and less than 2V for STD devices.

Figure 16 : Ground disconnection occuring when an equivalent resistor supplies current on the GND pin.



CONCLUSION

The VN series of High Side Drivers offers designers a highly attractive method of controlling a variety of inductive and resistive loads. The option to use a selection of extra features such as fast demagnetization or status filtering makes them equally suitable for general or specialised use, typically in the automotive environment.

VIPower

60V $B_{(BR)DSS}$ HIGH SIDE DRIVERS PRODUCT RANGE

DEVICE	$R_{DS(on)}$ @ 25°C (mohm)	V_{CC} Range (V)	PACKAGE	EXTRA FEATURES
VN02N	400	7 - 26	Pentawatt/PowerSO-10™	
VN05N	180	7 - 26	"	
VN20N	50	7 - 26	"	
VN30N	30	7 - 26	"	
VN03	500	5.5 - 26	Pentawatt/PowerSO-10	■ ○ *
VN06	180	5.5 - 26	"	■ ○ *
VN21	50	5.5 - 26	"	■ ○ *
VN31	30	5.5 - 26	"	■ ○ *
VN02AN	350	7 - 36	Pentawatt/PowerSO-10	■
VN20AN	50	7 - 36	"	■
VND05B(*)	200	6 - 26	Heptawatt/PowerSO-10	■ ○ □
VND10B(*)	100	6 - 26	"	■ ○ □
VN16B(*)	60	6 - 26	Pentawatt/PowerSO-10	■ ○
VN02H(*)	400	5 - 36	Pentawatt/PowerSO-10	

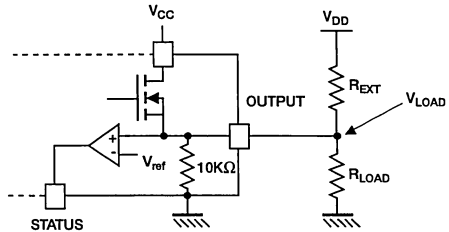
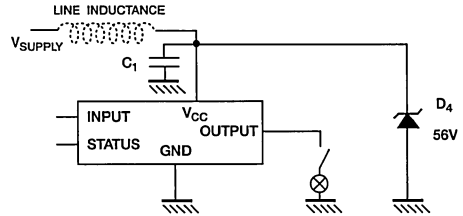
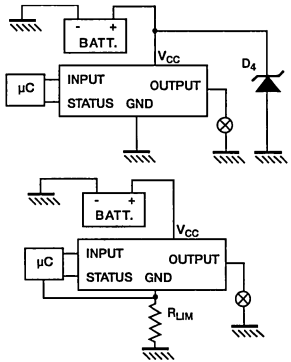
(*) Application information as described in the Note apply also to these devices

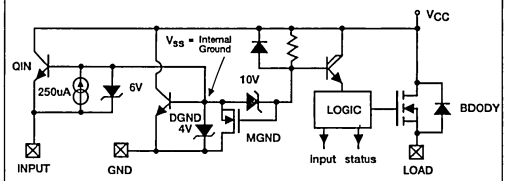
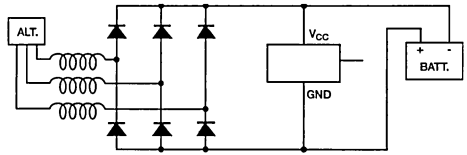
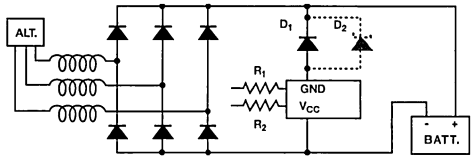
■ *Fast demagnetization & ground disconnection protection*

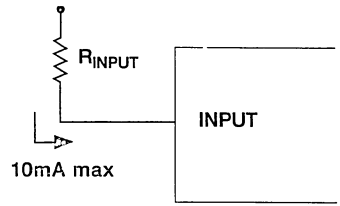
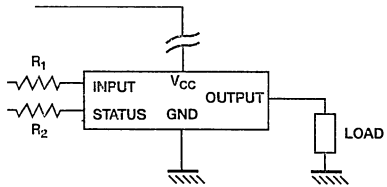
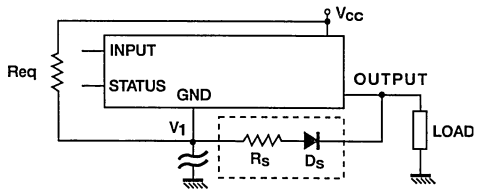
○ *Open load detection off state + stuck-on to V_{CC}*

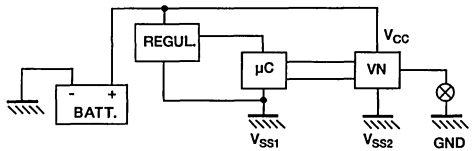
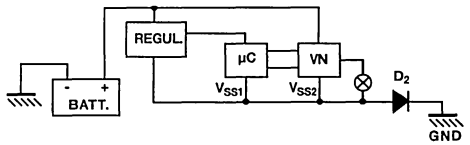
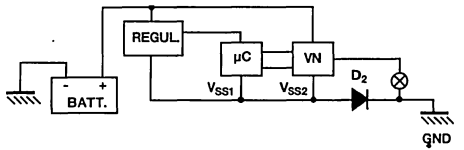
* *5msec STATUS FILTERING (ISO STANDARD)*

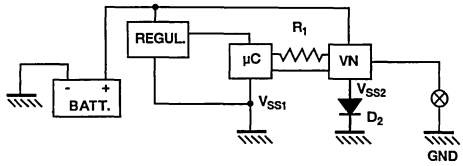
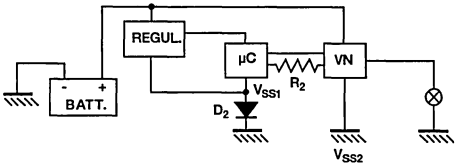
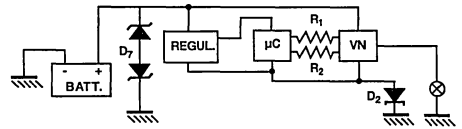
□ *Double channel*

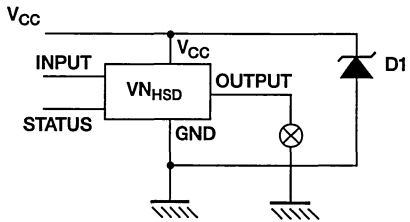
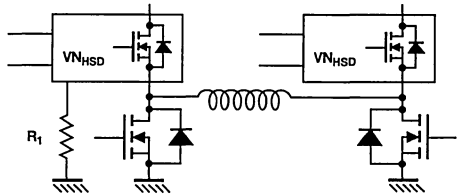
	SYMPTOM	DEVICE	COMPONENT	COMMENT	SCHEMATIC	NOTES
1	Off-state open load detection	VN03 VN06 VN21 VN31	R_{EXT}	It is necessary to set the current that fixes the voltage, V_{LOAD}, in the off state. When R_{LOAD} fails - goes open or high resistance - V_{LOAD} increases and an internal comparator triggers the status flag to go low.		Choose R_{EXT} to match V_{DD} to fix $I_{OL(off)}$. The threshold V_{LOAD} is fixed at V_{REF}. $I_{OL(off)} = (V_{DD} - V_{REF}) / R_{EXT}$. The open load detection in off-state is only possible for a nominal value of $R_{LOAD} << 10k\Omega$
2	Voltage spike on V_{CC} when load disconnects.	ALL	D4 or C1	If the line inductance is not zero and di/dt caused by disconnection of the load is high, an over voltage E =L·di/dt appears on V_{CC}, The $V_{(BR)DSS}$ of the output power MOSFET could be exceeded.		Use a 56V zener diode to clamp V_{CC} or put a capacitor, C1 (about 100nF), near V_{CC} pin.
3	Over voltage on V_{CC} from external circuit	ALL	D4 or R_{LIM}	D4 can be used as a decentralized clamp (V_{CC} clamp and energy clamp). Otherwise a resistor, R_{LIM}, can be added on the ground pin to limits the current in the signal section of the device in case it exceeds the signal path breakdown voltage.		$R_{LIM} = 150\Omega$ is a general value to protect devices from the effects of a load dump. Refer to the specific data sheet.

	SYMPTOM	DEVICE	COMPONENT	COMMENT	SCHEMATIC	NOTES
4	Supply reversal	ALL		Refer to the equivalent schematic seen by user through pins: Load, Input, GND		*V_{CC} > 1V →MGND"ON"→VSS= GND Normal case *-4 < V_{CC} < 0 →MGND OFF →No current accross input and GND pins →A DC current flows in the load and DBody WARNING : If the load is an inductance with a parallel free wheeling diode, the user sees 2 forward biased diodes between GROUND and V_{CC}. →Do not exceed imax to prevent damage.
5	Supply reversal - case 1	ALL		Battery connection reversed; correct connection of the High Side Driver devices.		If the battery is short circuited by 3 x 2 series diodes (typically an alternator diode configuration) the supply voltage, V_{CC}, is clamped to about -3V and no damage occurs to the VN device.
6	Supply reversal - case 2	ALL	D1 or D2	High Side Driver reverse connected with the battery correctly connected.		V_{CC} for the device is -13V. To prevent damage to the device use either a bipolar or Schottky diode in series with the ground pin connection. Use R1 and R2 to limit the negative current in the input and status pins because the internal ground drops to V_{CC}.

	SYMPTOM	DEVICE	COMPONENT	COMMENT	SCHEMATIC	NOTES
7	Input driving.	ALL	R_{INPUT}	Driving the input from a voltage greater than 6V		To drive the input from a line voltage > 6V insert a series resistor to limit the input current $I_{IN\ max}$ < 10mA
8	Pin disconnection - V_{CC}	ALL	R1 R2	Driving an inductive load, this kind of disconnection has the same electrical effects as V_{CC} reversal.		1) Resistive load - no problem of damage. 2) Inductive load - V_{CC} reversal occurs. If current and inductance of leads are too high the device may be damaged but the safety margin is wide - up to 100mH and 8A for the VN21 In this case, input and status pins are pulled to a negative voltage so it is recommended to insert resistors in series with these pins in order to protect the µC.
9	Pin disconnection - Ground	VN03 VN06 VN21 VN31 VN02AN VN20AN		An external component, Req, supplies current to the High Side Driver GND pin. The local ground is separate from the load ground.		The devices are internally protected (output stage off) if the voltage on the GND pin is ≤ 18V with reference to the real ground at Ø V. To avoid the High Side Driver to turn-on if GND is over 18V is possible insert Rs and Ds as shown in figure. Choose Rs so that V_1<18V

	SYMPTOM	DEVICE	COMPONENT	COMMENT	SCHEMATIC	NOTES
10	Ground potential differences	ALL		Voltage range for all High Side Drivers is defined between V_{CC} and V_{SS2} (VNxx GND). All voltages V_{IL}, V_{IH}, V_{USD} are refered to V_{SS2}.		If V_{SS1} and V_{SS2} are different, recalculate V_{IL}, V_{IH}, V_{USD} and beware of application bugs. (See points 11/12/13/14)
11	Ground potential differences - case 1	ALL	D2	Using power diode to withstand reversed battery. Case 1: $V_{SS1} = V_{SS2} =/= GND$ with $V_{SS1} > GND$		Voltage losses in power diode. Input and status levels are not effected. Under-voltage shutdown level increased by diode V_F. Off-state open load level, V_{REF}, increased by V_F. A general rule is: level shift is (V_{SS2} - GND).
12	Ground potential differences - case 2	ALL	D2	Using a diode to protect the High Side Driver against reversed battery. (See point 6 above) $V_{SS1} = V_{SS2} =/= GND$ with $V_{SS1} > GND$		The input and status are unaffected. $V_{USD} = (V_{SS2} - GND) + V_{USDo}$. Off-state open load level, V_{REF}, is increased by (V_{SS2} - GND). Not suitable if the µController uses an analog transducer referred to ground.

	SYMPTOM	DEVICE	COMPONENT	COMMENT	SCHEMATIC	NOTES
13	Ground potential differences - case 3	ALL	R1, D2	Using a diode to protect the High Side Driver against reversed battery. V_{SS1} =/= V_{SS2}. $V_{SS2} > V_{SS1}$		V_{IL} and V_{IH} shifted by (V_{SS2} - V_{SS1}). R1 limits any negative current when the µController takes I/O to ground .On the status pin the zero corresponds to the V_F of D2, V_{USD} and V_{OL} being increased by (V_{SS2} - GND).
14	Ground potential differences - case 4	ALL	R2, D2	Using a diode to protect the µC against reversed battery. V_{SS1} =/= V_{SS2}. $V_{SS2} < V_{SS1}$		In fault conditions the device pulls the status pin down to V_{SS2} and the µController sees a negative voltage - (V_{SS1} - V_{SS2}). There is a risk of latch up for the µController CMOS output. Add R2 to limit the current. Undervoltage and off-state open load levels are not shifted.
15	Summary of the influence of ground differences, pin disconnections and over voltage protection.	ALL	R1, R2, D2, D7.	Recommended scheme		* common ground for µController and VN device * Reversed battery protection - Schottky diode * Series resistor for input and status pins * Over-voltage protection - bi-directional Zener

	SYMPTOM	DEVICE	COMPONENT	COMMENT	SCHEMATIC	NOTES
16	Load dump: battery disconnection whilst the alternator is working	ALL	D1	High voltages can be generated if the battery is disconnected when the generator is running in a car. Damaging effects can be overcome by using a clamping diode with at least V_{BR} > 26V as 2 x 12V batteries are often used to jump start cars. This for overvoltage transient higher than specified in datasheets.		Protection against over-voltages are efficient if connected between pin 3 (V_{CC}) and pin 1 (ground).
17	V_{LOAD} > V_{CC} (Bridge circuit)	ALL	R1	In full bridge applications during the demagnetization phase V_{LOAD} > V_{CC}. A current will flow out of GND pin, possibly damaging the bonding.		Insert a resistance, R1 (suggested value 47Ω), in the ground pin to limit the ground current and avoid damaging the bonding.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

PROTECTION STANDARDS APPLICABLE TO AUTOMOBILES

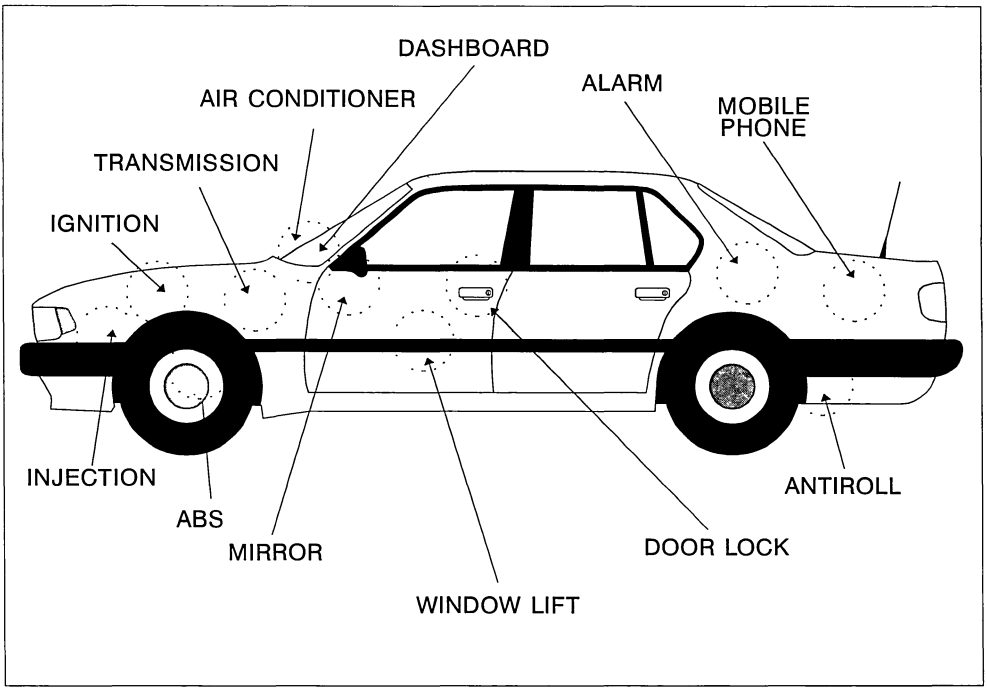
A. Bremond

1 - INTRODUCTION :

A growing number of sensitive electronic units can be found in motor vehicles. Unfortunately the presence of electrical disturbances threatens their reliability.

The objective of this paper is to list all these disruptive factors and to suggest appropriate protection devices.

Figure 1 : Electronic modules in a car



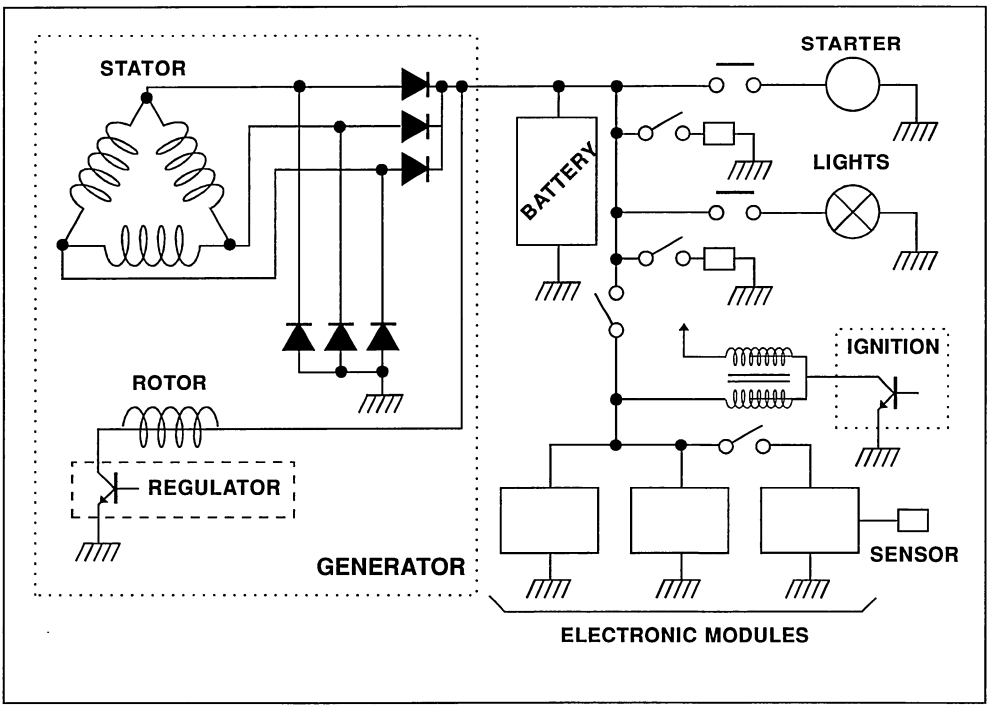
II - GENERAL INFORMATION :

II.1 Simplified diagram of an automotive electrical circuit

II.2 Coexistence of electromechanical engineering with electronics :

Fig. 2 shows that the electrical system of a motor vehicle contains some electromechanical engineering which generates disturbances (alternator, ignition system, starter, relays etc...) and some electronic equipment affected by these disturbances (instrument computer, injection unit etc...). The role of the protection devices will be to ensure the smooth coexistence of both.

Figure 2 : Automotive electrical diagram



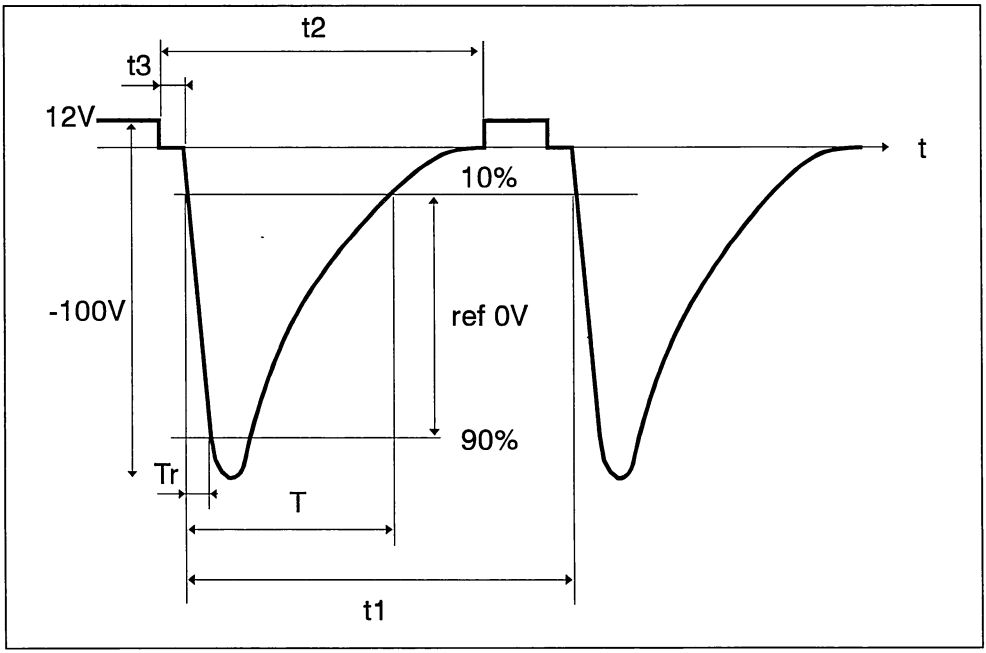
III - ORIGIN AND WAVEFORM PARAMETERS :

Electronic units receive the disturbances through the various cables which are connected to them. They are defined by the ISO/TC 22 standards and described in appropriate technical notes issued by the various motor vehicle manufacturers.

III.1 Disconnecting inductive loads :

Disconnecting an inductive element causes a high inverted overvoltage on its terminals.

Figure 3 : Shape of test pulse 1 (disconnection of Inductive Loads)



T = 2 milliseconds

Tr = 1 microsecond

Ri = 10 ohms *

t1 = 5 seconds

t2 = 0.2 second

t3 < 100 µs

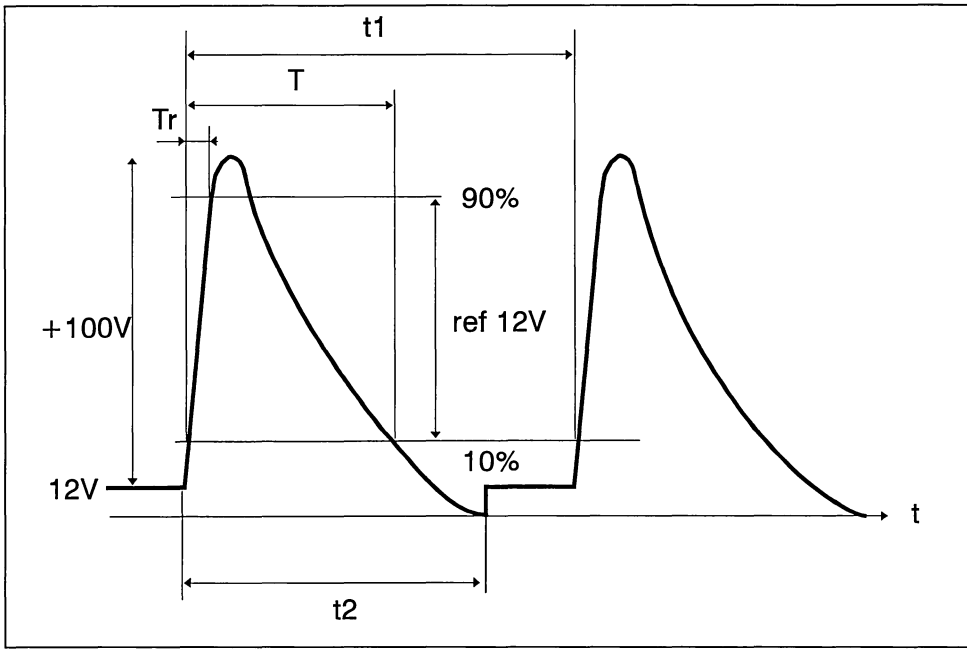
* Internal series resistor of the surge generator.

III.2 Sudden power cut off in the main circuit :

After the battery supply circuit is cut by the ignition key, the ignition circuit contines to release disturbances until the engine stops rotating.

Overvoltages are generated by switching the power supplied by electric motors acting as generators, e.g. the air conditioning fan. Their amplitude is increased by the absence of the filtering which would normally be carried out by the battery.

Figure 4 : Shape of test pulse 2 (Sudden Interruption of Series Current)



T = 2 milliseconds

Tr = 1 microsecond

Ri = 10 ohms

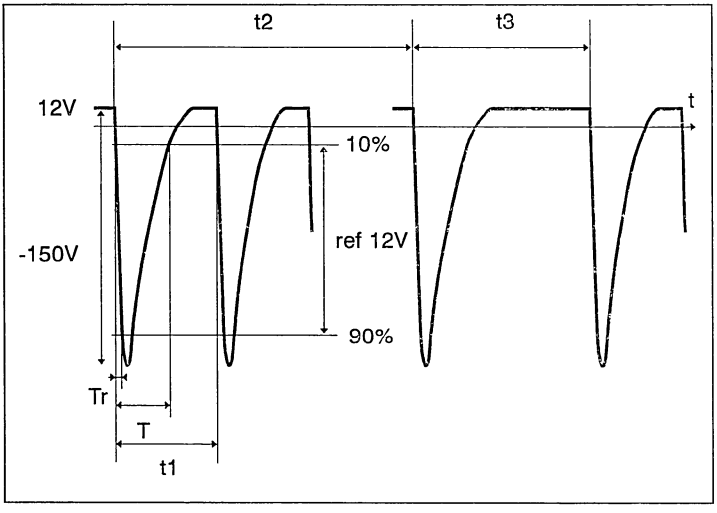
t1 = 0.5 to 5 seconds

t2 = 0.2 second

III.3. Switch bounce :

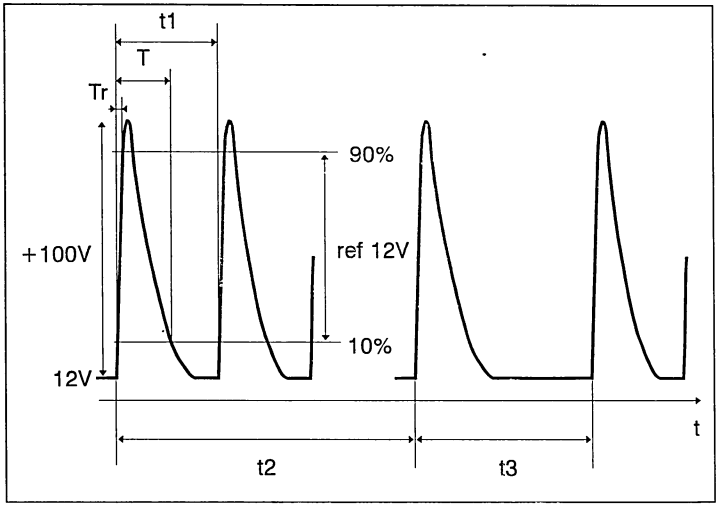
Power cut-off in the supply network capacitances and inductances, resulting from switch rebounds. generates sets of disturbances.

Figure 5A : Shape of test pulse 3A (switching spikes)



T = 0.1 microsecond
Tr = 5 nanoseconds
Ri = 50 ohms
t1 = 100 microseconds
t2 = 10 milliseconds
t3 = 90 milliseconds

Figure 5B : Shape of test pulse 3B (switching spikes)

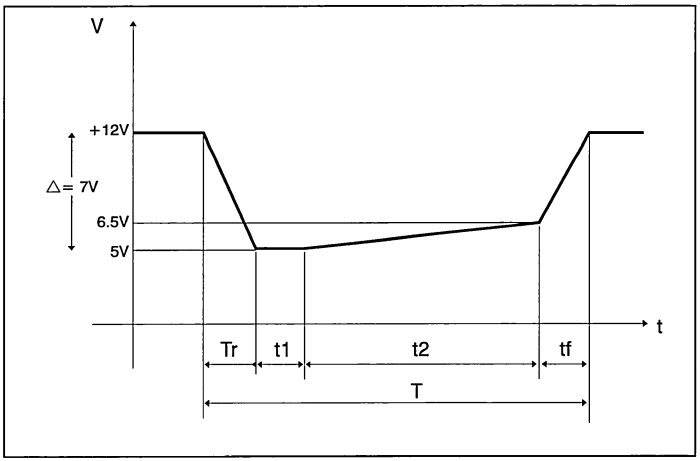


T = 0.1 microsecond
Tr = 5 nanoseconds
Ri = 50 ohms
t1 = 100 microseconds
t2 = 10 milliseconds
t3 = 90 milliseconds

III.4. Activating the starter :

When the starter circuit is activated, a voltage drop occurs in the supply source.

Figure 6 : Shape of test pulse 4 (starter motor engagement disturbance)



T = 130 milliseconds

Ri = 0.01 ohm

Tr = 10 milliseconds

t1 = 10 milliseconds

t2 = 100 milliseconds

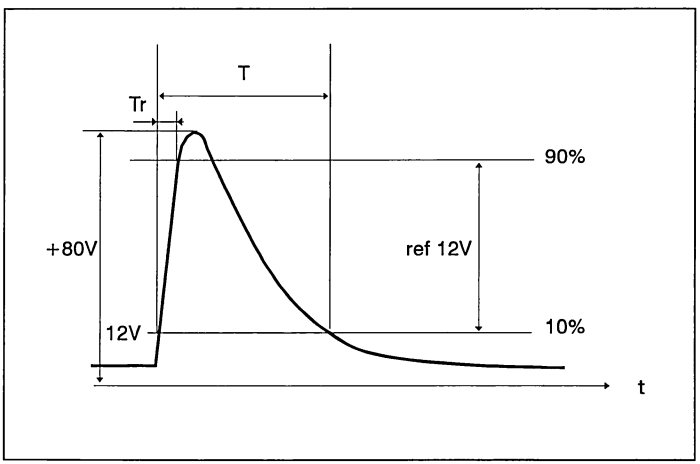
Tf = 10 milliseconds

III.5. Load dump :

This happens when the battery is disconnected whilst being charged by the alternator.

During this load dump, the voltage on the alternator terminals increases rapidly. The length of this disturbance depends on the time constant of the generator excitation circuit.

Figure 7 : Shape of test pulse 5 (load dump)



Tr < 10 milliseconds

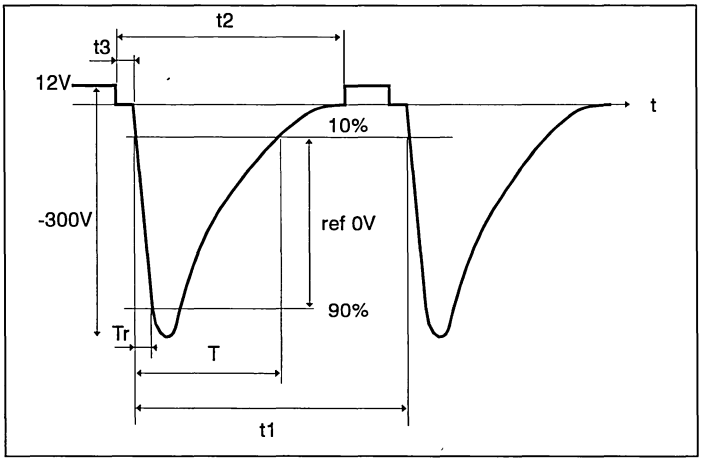
Ri = 2 ohms

T = 300 ms

III.6. Power cut off in the ignition coil :

This disturbance occurs when the ignition contact is cut off.

Figure 8 : Shape of test pulse 6 (ignition coil current interruption)

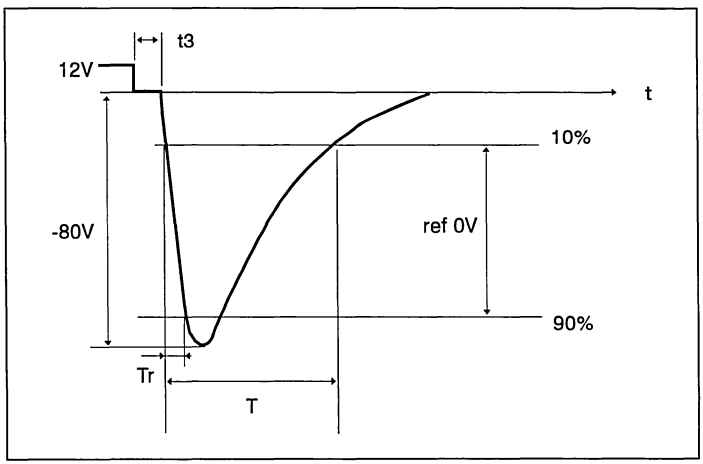


T = 300 microseconds
Tr = 60 microseconds
Ri = 30 ohms
t1 = 15 seconds
t2 = 1 second
t3 < 100 microseconds

III.7. Alternator magnetic field decay :

This negative overvoltage appears when the magnetic field of the alternator disappears (when the engine stops turning).

Figure 9 : Shape of test pulse 7 (alternator field transient at engine stop)



T = 100 milliseconds
Tr = 5 to 10 milliseconds
Ri = 10 ohms
t3 < 100 microseconds

III.8. Regulator failure :

This type of problem can cause the output generated to be permanently too high, perhaps greater than 18 V.

III.9. Starting aid :

In certain cases, when new motor vehicles have been stored over a long period (eg. sea deliveries, when starting takes place at low temperatures, etc...,) using another source of energy other than that of the vehicle becomes necessary.

The most common procedure is the use of two standard 12 Volt batteries paralleled with that of the vehicle. The overvoltage estimate is 24 Volts (or -24V in the case of an inverted connection).

III.10. Miscellaneous :

Motor vehicles can be subject to other sources of disturbances, such as :

- the connection to a diagnostic unit.
- electric soldering.
- paint electrostatic tension.
- HF rays generated by tranmission equipment.

IV - ANALYSIS OF THE VARIOUS DISTURBANCES :

ORIGIN	DURATION	VOLTAGE	ENERGY	FREQUENCY
Disconnection of inductive loads	2 ms	- 100 V	2.3 j	Frequent
Power cut-off in the main circuit	2 ms	+ 100 V	2.3 j	Frequent
Switch bounce	0.1s x 10	+ 100 V - 150 V	50j x 10	Frequent
Starter engagement	130 ms	-	-	At every start
Load dump	300 ms	+ 80 V	50 j	rare
Ignition	300 s	- 300 V	0.003j	Frequent
Alternator magnetic field decay	100 ms	- 80 V	0.2 j	At every stop
Imperfections at regulator level	Continuous	+ 18 V	-	rare
Starting aid	Several minutes	24 V	-	rare

V - CONCLUSION

Table IV shows that we are confronted with 5 types of disturbances :

a/ Positive impulsive overvoltages

b/ Negative impulsive overvoltages

c/ Positive continuous overvoltages

d/ Negative continuous overvoltages

e/ Impulsive voltage drop

The goal of protection circuits is to prevent destruction due to these disturbances.

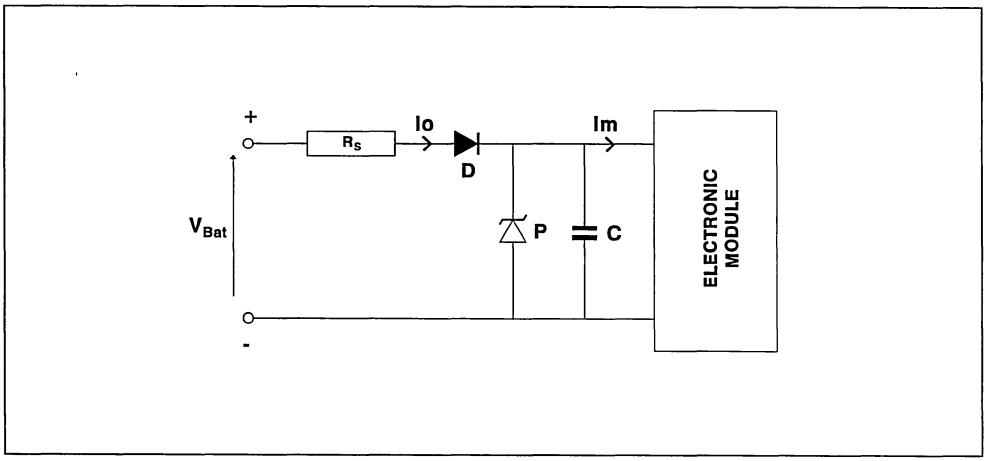
CHOICE OF PROTECTION IN AUTOMOTIVE APPLICATIONS(CLASSICAL TOPOLOGY)

A. BREMOND

1. INTRODUCTION

This paper describes a protection schematic based on discrete components, together with a general method of choosing the components to suppress the surge effects on automotive modules.

Figure 1 : General Protection Topology



2. GENERAL PROTECTION SCHEMATIC :

2.a Positive impulsive overvoltages :

This type of overvoltage is clamped by the protection component P at maximum voltage V_{CL}. Resistance R_S limits the dissipated energy in the protection component without compromising the clamping function.

2.b Negative impulsive overvoltages :

There are two ways to limit these :

- Without diode D : the protection component operates as a rectifier diode and clamps the voltage at the unit terminals to approximately 1 V.

- With diode D : the diode is reverse-biased and therefore protects the unit.

One important thing to take into account is the peak reverse voltage limit of D. V_{RRM} = 400V seems a good compromise (see curve N° 6 of the ISO/TC22 standard).

2.c Positive continuous overvoltages :

During this phase, the protection component must be in the stand- by phase (very low current passing through the component).

2.d Negative continuous overvoltages :

This protection is achieved by diode D which is reverse -biased.

2.e Impulsive voltage drop :

During this phase, the unit is fed by capacitor C while diode D prevents C from discharging into the battery circuit.

3. THE CHOICE OF COMPONENTS :

3.a Diode (D)

The following parameters will constitute the selection criteria :

- The average current used by the electronic module.

- The maximum repetitive peak reverse voltage V_{RRM}

- The maximum ambient temperature T_{amb}.

The following inequality must apply in all cases :

$$T_{amb} + R_{th}\, P < T_j \text{ max}$$

where

$$P = V_{TO}\, I_F\, (AV) + rd\, I^2_F(R_{MS})$$

R_{th} = thermal resistance (Junction - ambient) for the device and mounting in use.

3.b Resistance (R_S)

Its presence allows a "size" (and thus cost) reduction of the protection component.

Its value is a function of the following elements :

V_{bat} min : lowest battery voltage which is specified in the technical note issued by the manufacturer.

V_{CC} min : minimum voltage needed for the electronic unit in operation.

I_{CC} max : maximum supply current of the electronic module.

The maximum value of Rs will be :

$$R_S \text{ max} = (V_{bat} \text{ min} - V_{CC} \text{ min})/I_{CC} \text{ max}$$

3.c Capacitor (C)

Its role is to make sure that the voltage at the terminals of the electronic unit is greater than or equal to Vcc min while the starter circuit is active.

Its value depends on :

V_{bat} : voltage across the battery before the disturbance

V_{CC} min : see par. 5.b

T : length of the disturbance (130 ms: see application note 4.1, paragraph 111.4)

The minimum value of C will be :

$$C\text{min} = (130 * 10^{-3}/R_{eq})/\ln (V_{CC} \text{ min}/V_{bat})$$

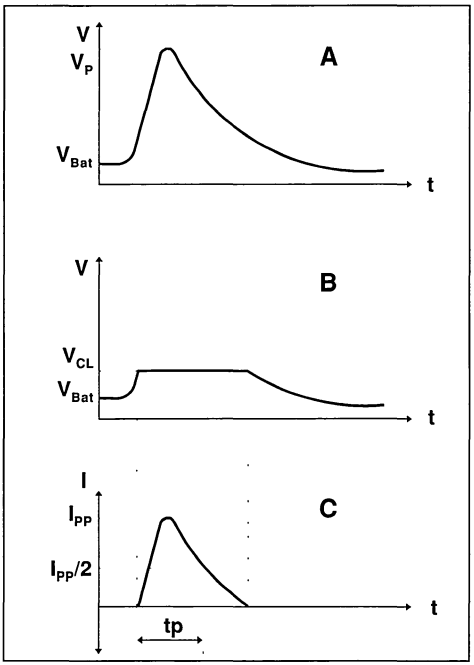
with R_{eq} = equivalent resistance of the electronic unit

$R_{eq} = V_{CC}$ min/I_{CC} max

3.d Protection component (P)

- How it works :

Figure 2 : Transil Behaviour



A : Disturbance

B : Voltage across the protection device

C : Current through the protection device

The role of the protection device is to suppress the destructive effects of the surge (Fig.2a), the most agressive being the load dump impulse.

To achieve this, the TRANSIL clamps the spike at a maximum value V_{CL} (Fig.2b). A surge current flows through the suppressor during this phase (Fig.2c).

4. THE CHOICE OF THE PROTECTION DEVICE

4.a Parameters to take into account

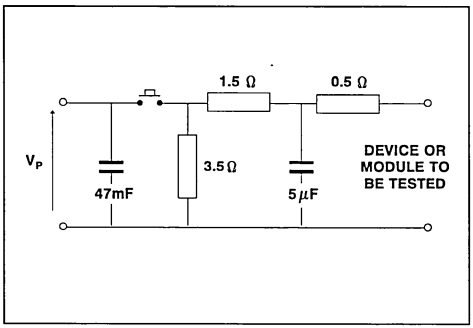
To choose the TRANSIL we have to know the surge parameters and the application requirements.

- Surge parameters

The surge is defined by the peak value Ip and the duration tp of the current wave flowing through the protection device during the clamping.

As shown in the ISO/TC22 standard the most energetic impulsive disturbance is the load dump surge. Most car manufacturers recommend the SCHAFFNER NSG 506 generator to synthesise this wave. See fig.3.

Figure 3 : Equivalent circuit of Schaffner gener-



This circuit allows us to determine the parameters of the current wave seen by the TRANSIL.

The peak current I_P is equal to :

$$I_P = (V_P - V_{CL}) / (R_G + R_S)$$

Where

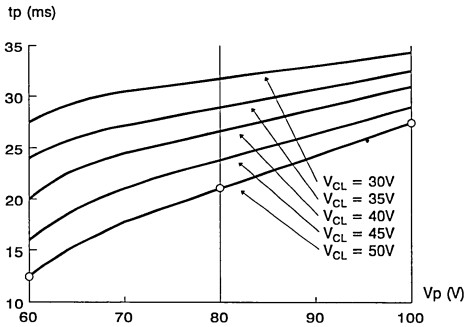
V_P = Peak voltage of the surge (+ 80V)
V_{CL} = Clamping voltage of the transil

R_G = Series resistance of the generator (2 Ohms)

R_S = Series resistance of the module to be protected (see chapter 3.b)

For example with V_P = 80V, V_{CL} = 40 V and R_S = 0 Ohm, we have I_P = 20A

Figure 4 : Current pulse duration versus V_P and V_{CL}



The curves of figure 4 give the duration tp of the current wave in the TRANSIL during clamping. This parameter depends on the peak voltage V_P of the surge and on the clamping voltage V_{CL} of the protection device. For example with V_P = 80V and V_{CL} = 40V, tp = 27.5 ms.

- Application requirements

Three values are necessary :

- The maximum operating voltage, which is the greatest battery potential. Often the car's electrical equipment has to withstand two battery voltages (due to starting aids: see ISO/TC22 standard). These parameters define the minimum stand off voltage V_{RM} of the TRANSIL.

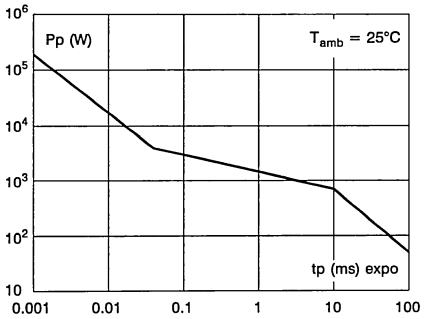
- The minimum destructive voltage, which is the voltage value over which the device will be destroyed. This limit determines the maximum clamping voltage V_{CL} of the protection device.

- The maximum ambient temperature T_{amb} that would decrease the power dissipation capability of the TRANSIL.

4.b Choice of the protection device

The choice of component is made with the help of the parameters t_P, P_P in the curve $P_P = f(t_P)$ from the "PROTECTION DEVICES" data book.

Figure 5 : Peak pulse power versus exponential pulse duration (1.5KE, 10V < V_{BR} < 250 V)

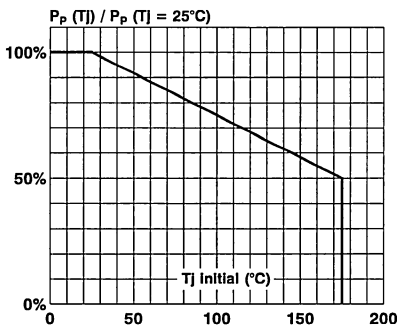


If the operating point defined by t_P and $P_P = V_{CL} * I_P$ is on or below the curve, the TRANSIL can operate in the application at 25°C of ambient temperature.

4.c The ambient temperature effect :

Component characteristics are given at an ambient temperature of 25°C (die temperature before clamping action). The following chart shows the effect of junction temperature on the power suppression capability.

Figure 6 : Allowable power dissipation versus junction temperature



This curve gives the derating to be applied to the peak power capability of the protection device according to junction temperature.

The second temperature effect is the shift of V_{BR}.

$$V_{BR} \text{ (at T)} = V_{BR} \text{ (at 25°C)} * (1 + \alpha_T \text{ (T-25)})$$

Where α_T is the temperature coefficient of V_{BR}.

4.d Calculation of clamping voltage V_{CL}

The clamping voltage V_{CL} can be estimated as follows :

$$V_{CL} = V_{BR} \text{ max} + (Rd\ IP)$$

Where Rd is the dynamic resistance of the TRANSIL

Table 1 - Typical Rd for wave of t_P = 30 ms at 25°C

	BZW04 P23	P6KE 30P	1.5KE 30P	BZW50 -22	LDP24A
Rd typ (Ω)	1.2	0.75	0.35	0.15	0.12

5 - EXAMPLE :

A / Disturbances

The load dump is the most agressive

B / Battery voltage

The electronic unit will have to function with a battery voltage of 11 V.

C / Ambient temperature

Tamb = 85°C

D/ Electrical characteristics of the module

Table 2 - Module characteristics

PARAMETERS	V_{CC}	I_{CC}
DESCRIPTION	Supply voltage	Supply current
MIN	8	-
TYP	12	400
MAX	32	600
UNIT	Volts	mA

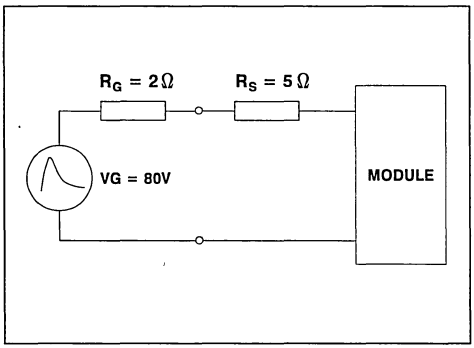
E / Analysis

E/1 Calculation of R_S max

$$R_S \text{ max} = (V_{bat} - V_{CC} \text{ min})/I_{CC} \text{ min}$$
$$R_S \text{ max} = (11\text{-}8)/0.6 = 5 \text{ Ohms}$$

E/2 Diagram

Figure 7 : Application Diagram



E/3 Peak current

$$I_{PP} = (V_G\text{-}V_{CL})/(R_G+R_S) = (80\text{-}32)/7=6.9A$$

E/4 Peak power

$$P_P = V_{CL} * I_{PP} = 32 * 6.9 = 221 \text{ W}$$

E/5 Conduction time

$$t_P = 30 \text{ ms}$$

E/6 Choice of the TRANSIL

Table 3 - Transil characteristics

TYPE	POWER CAPABILITY (tp = 30 ms)	
	at 25°C	at 85°C
BZW04	60 W	45 W
P6KE	80 W	64 W
1.5KE	200 W	160 W
BZW50	700 W	525 W
LDP24A	1980 W	1800 W

E/7 Conclusion

Diode BZW50-22 is an efficient protection device within the 85°C temperature range, and the V_{CL} max is given as follows :

$$V_{BR} (85°C) = V_{BR} (25°C) \times (1 * \alpha_T(85\text{-}25))$$
$$= 29.8 * (1 + 9.6 * 10\text{-}4 * 60)$$
$$= 31.5V$$
$$V_{CL} (85\ °C) = V_{BR} (85\ °C) + Rd\ I_P$$
$$= 31.5 + (0.15 * 6.9)$$
$$= 32.5 \text{ V}$$

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

AUTOMOTIVE PROTECTION WITH THE RBOxx SERIES

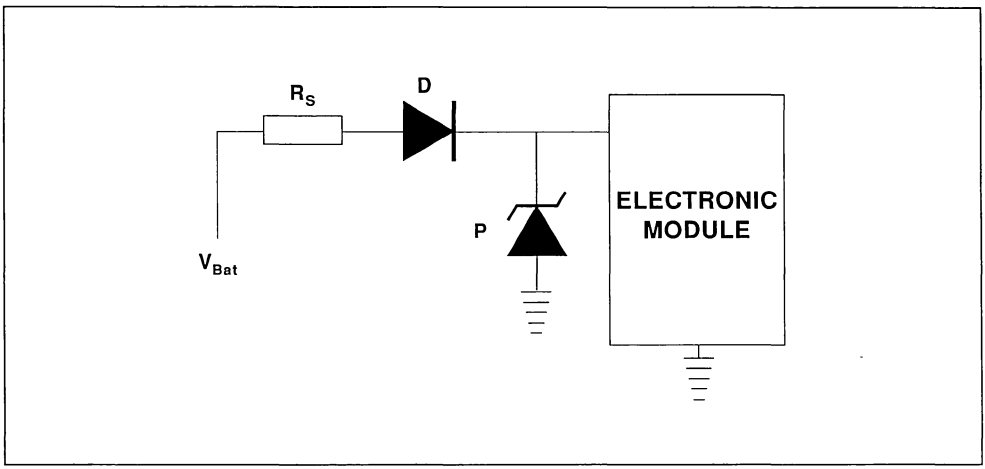
C. Cytera

1. INTRODUCTION

The harsh electrical environment in automobiles poses problems for the electronic modules present. Even in normal operation, large positive and negative overvoltages due to switch bounce, ignition coil switching and other phenomena are a potential cause of destruction. An additional hazard is the possibility of supply reversal, perhaps caused by faulty wiring. Another danger is the "load dump" effect, caused by battery disconnection while the engine is running. This causes the energy stored in the alternator coils to manifest itself as an 80 V transient lasting around 300 ms : lethal to semiconductor circuits. See application note 4.1 : "Protection standards in automotive applications" for more details.

Protection is therefore required, which can be centralized or distributed. Centralized protection attempts to suppress disturbances at their source, for example crowbar devices at the alternator to counter the load dump effect. Distributed protection aims to dissipate disturbances at their destination. Components performing this function are present in the electronic modules themselves and are thus relatively numerous. The RBOxx (Reversed Battery and Overvoltage) series of protection devices from SGS-THOMSON has been designed to reduce this distributed protection component count.

Figure 1 : Classical protection circuit

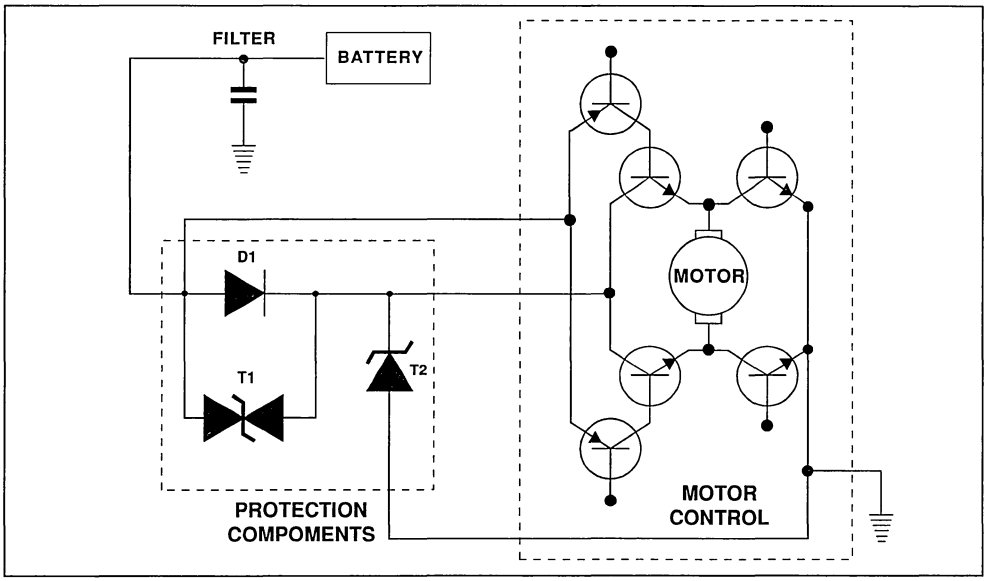


2. CLASSICAL DISTRIBUTED PROTECTION

The circuit shown in fig.1 protects the module against battery reverse as well as impulsive and continuous overvoltages, both positive and negative. In addition, overvoltages generated by the module are prevented from reaching the car supply network. Rs, in cases where it can be used, limits the power dissipated in the protection device P. Note that diode D is used in reverse-bias to block negative overvoltages, so its peak reverse voltage limit (VRRM) must be taken into account.

Motor driver protection is complicated by the presence of transistor circuits which control the direction and magnitude of current flow through the motor. A bidirectional clamping device needs to be added in order to ensure protection of both halves of this circuit. See fig.2.

Figure 2 : Motor driver protection with discrete components



The NPN transistors supplied via D1 are protected in the classical fashion already described. The PNP devices are connected directly to the car supply network and are protected as follows :

- Positive surges : overvoltage is clamped by T2 with D1 forward- biased.

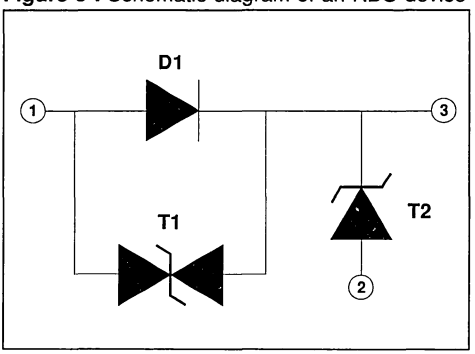
- Negative surges : These are clamped by T1 with T2 forward - biased.

Three components are thus required per motor driver, representing significant component and area cost.

3. DISTRIBUTED PROTECTION WITH THE RBOxx FAMILY

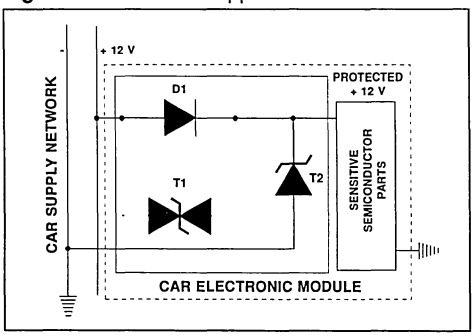
The RBOxx devices integrate all the protection functions required by car electronic modules : see fig.3.

Figure 3 : Schematic diagram of an RBO device



Diode D1 protects against a reversed battery, while the "Transil" clamping device T2 suppresses positive surges. Negative surges are blocked up to the breakdown voltage of the bidirectional clamp T1. Larger negative surges are suppressed by T1 in avalanche breakdown in series with T2 forward-biased. Fig.4 shows the basic application of the RBOxx.

Figure 4 : RBO basic application



Note that as the voltage across D1 is clamped by T1, the VRRM of the diode is no longer a concern. The clamping voltage is the same as that of T2, given by the yy digits in the part number of the form RBOxx-yy. The xx digits indicate the average forward current between pins 1 and 3.

Two devices are available at the time of writing : the RBO08-40 and the RBO40-40. The latter device is specifically designed to protect against "load dump" surges due to the greater power capability of T2, while the RBO08-40 is adequate for suppressing the other overvoltages present.

The presence of T1 makes possible an elegant solution to the motor driver protection. The RBOxx replaces the three protection components shown in fig.2 and protects the motor driver circuit in the same way.

4. CONCLUSION

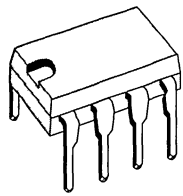
A car power supply network is often contaminated with voltage surges potentially damaging to the semiconductor circuits present. The SGS-THOMSON family of RBOxx protection devices enables full protection from these surges with the minimum component count.

PACKAGES

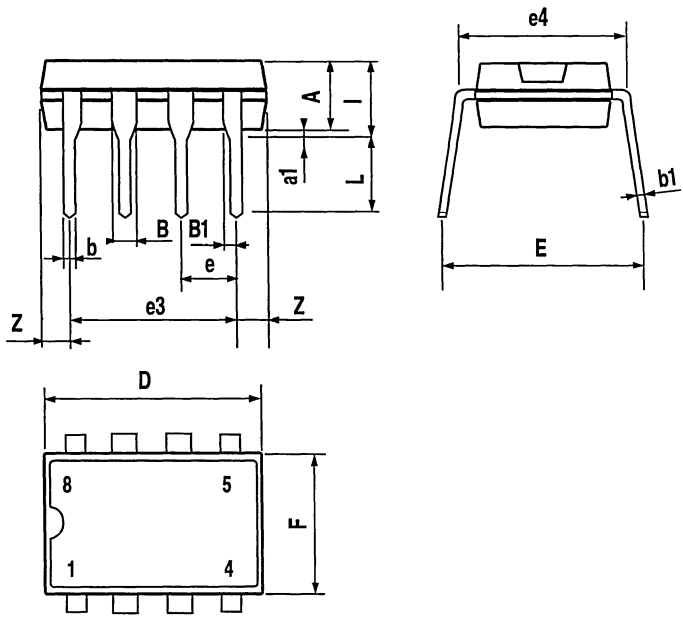
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Minidip (0.4)

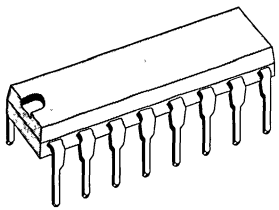


P001F

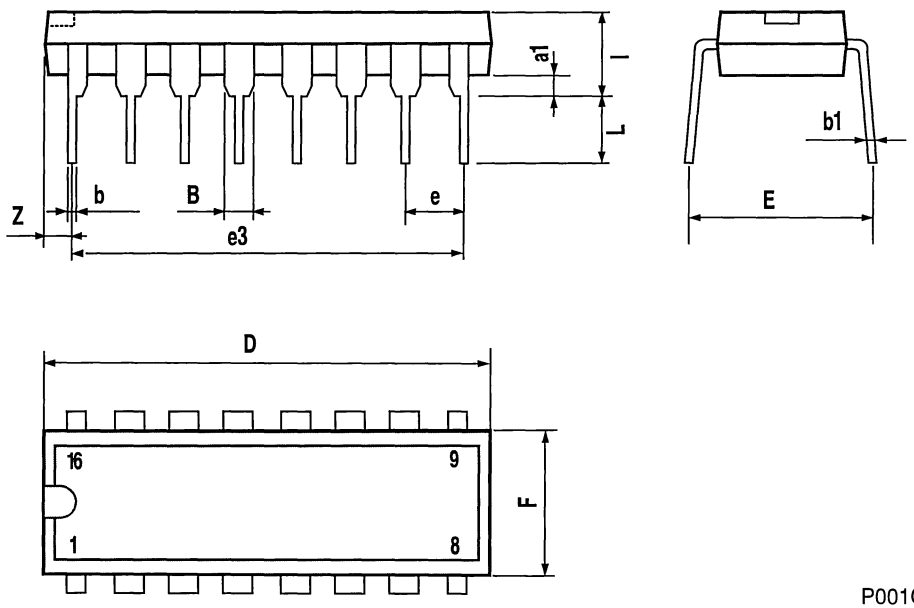
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP16 (0.25)

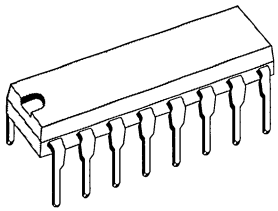


P001C

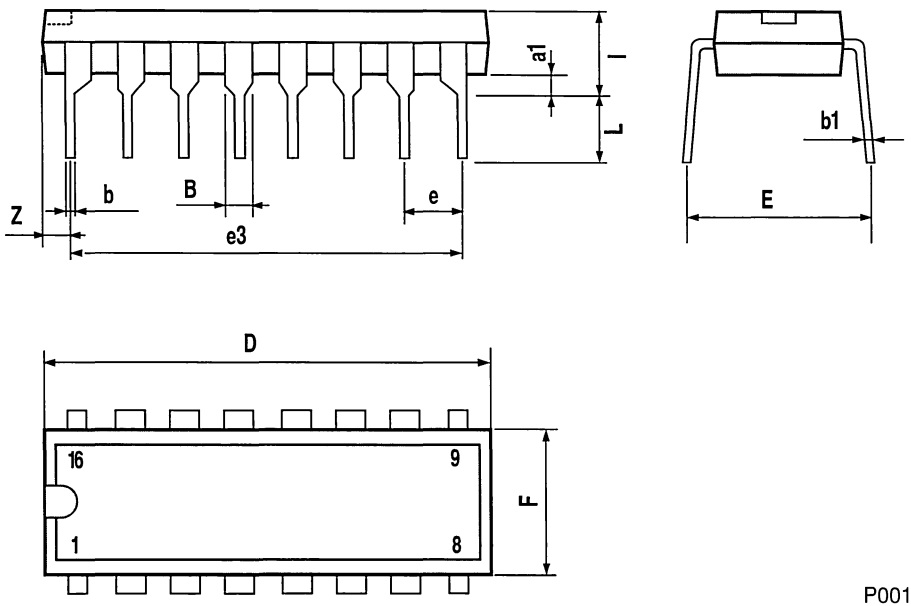
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			20			0.787
E		8.8			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP: (8+8), (12+2+2)

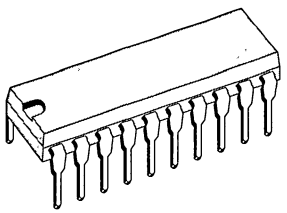


P001V

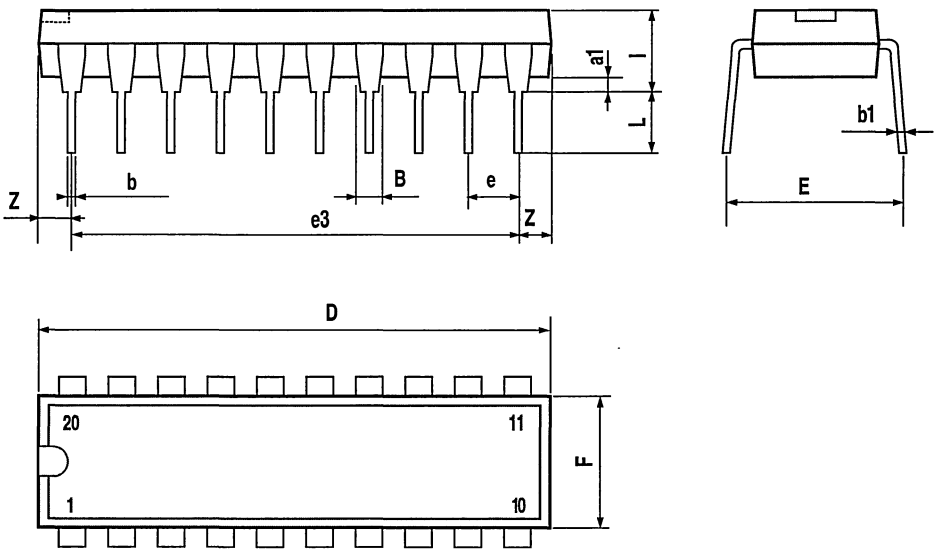
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP20 (0.25)

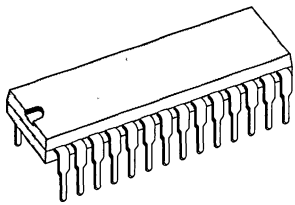


P001J

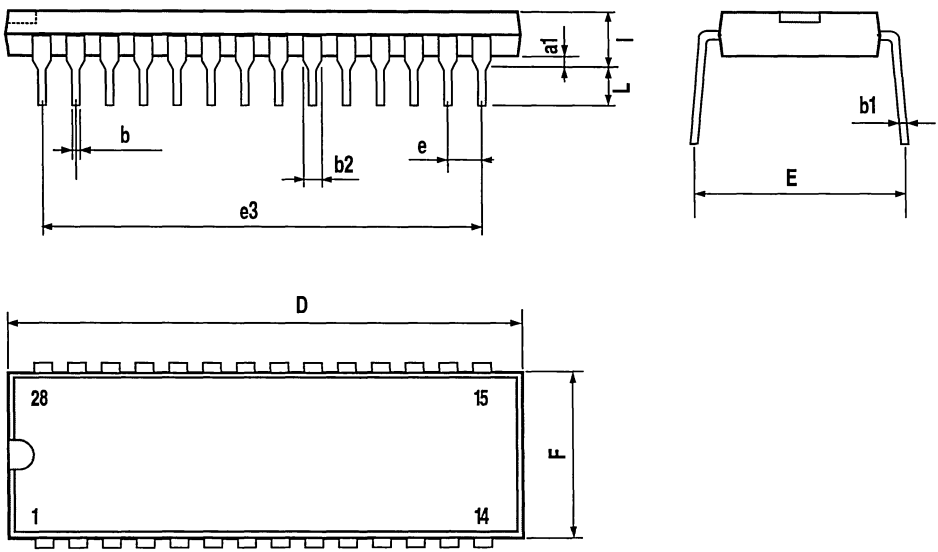
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D	35.06		36.22	1.400		1.425
E			16.3			0.641
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.30			0.130	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



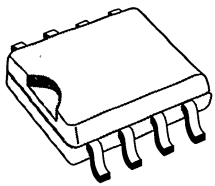
Plastic DIP28



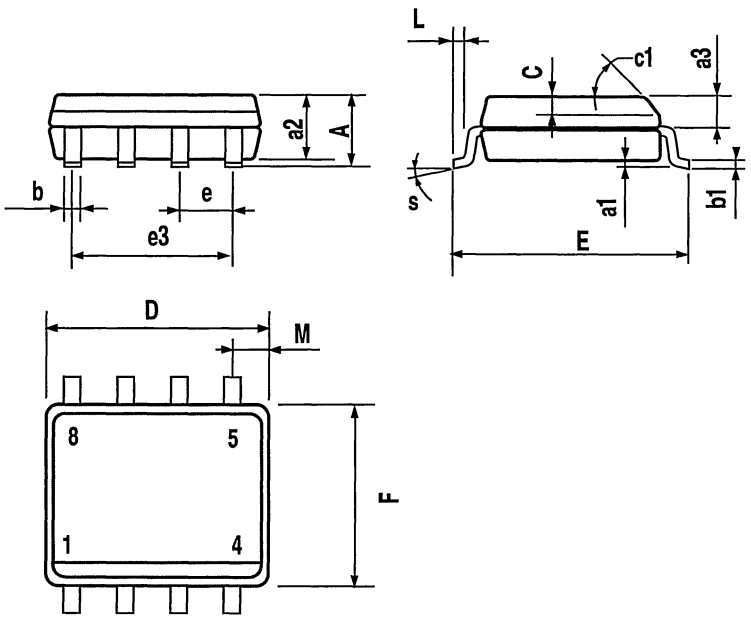
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45° (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO8

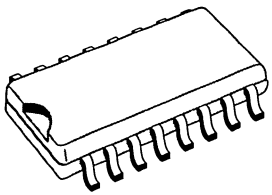


P013M

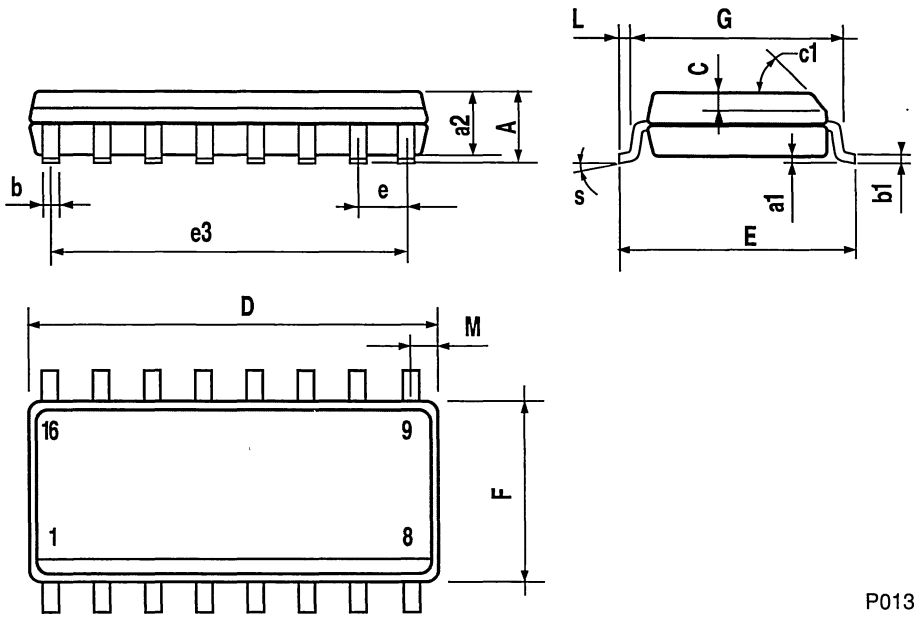
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO16

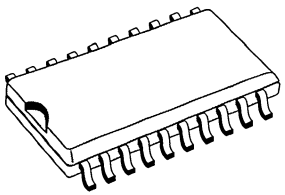


P013H

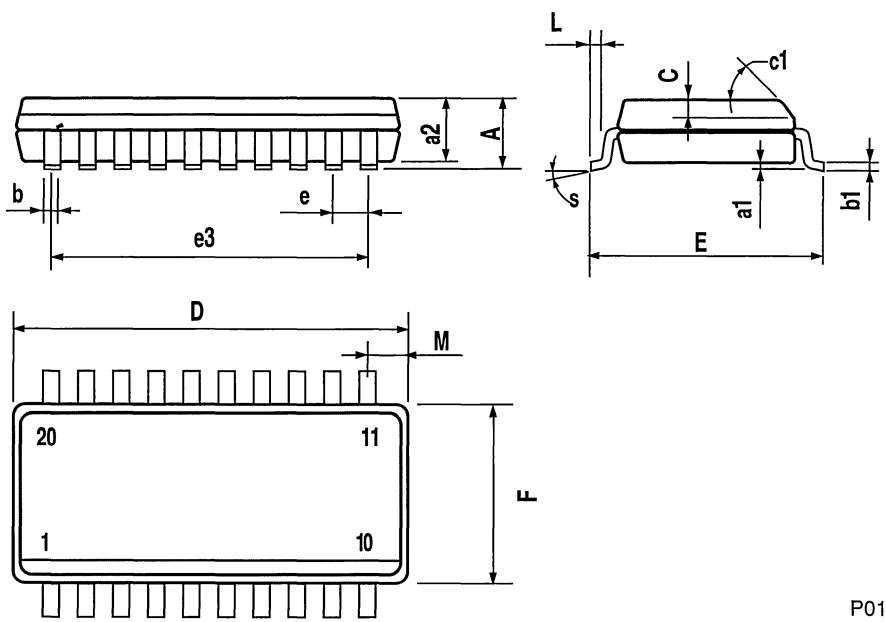
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO20L (12+4+4)

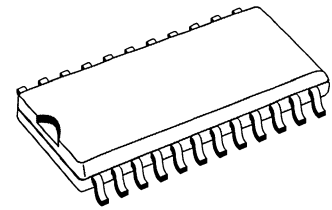


P013L

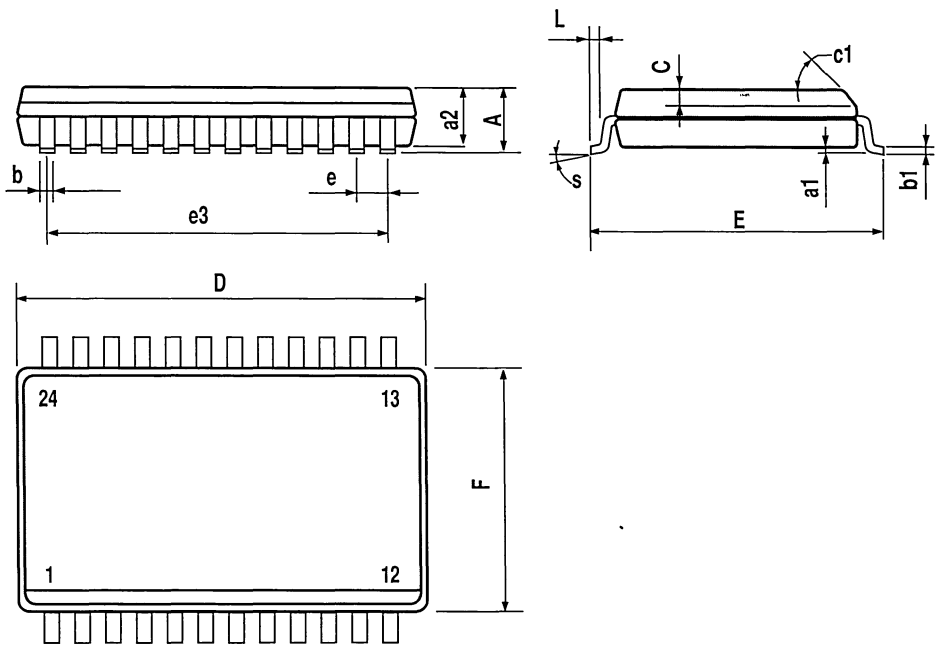
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.420
e		1.27			0.05	
e3		13.97			0.55	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



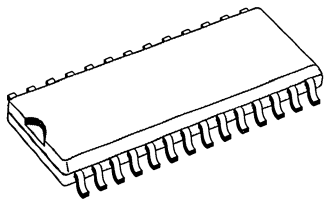
SO24 (16+4+4)



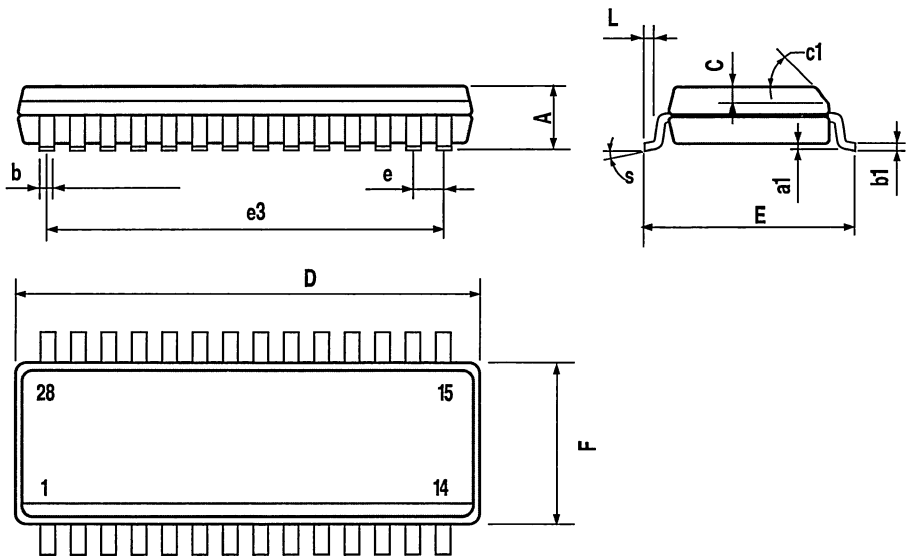
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.30	0.004		0.011
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.013
C		0.50			0.020	
c1	45° (typ.)					
D	17.70		18.10	0.696		0.712
E	10.00		10.65	0.393		0.420
e		1.27			0.05	
e3		16.51			0.65	
F	7.40		7.60	0.291		0.299
L	0.40		1.27	0.015		0.050
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO28

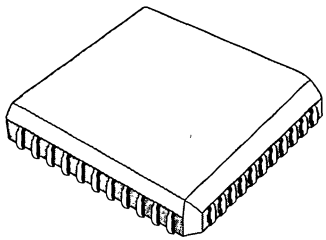


P013N

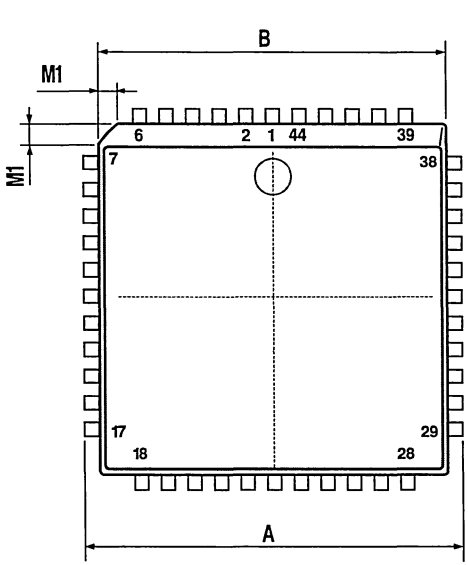
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16.0	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

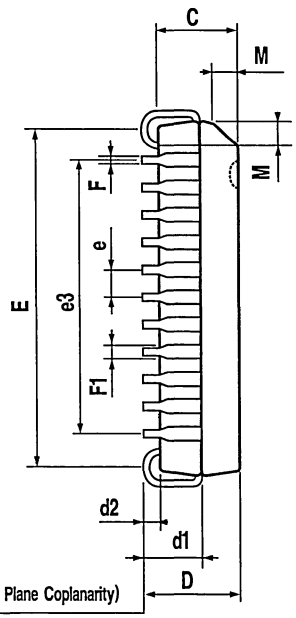
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PLCC44





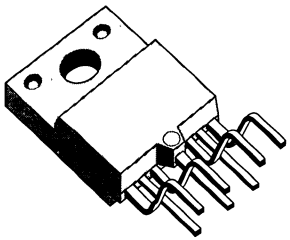
G (Seating Plane Coplanarity)

P027B

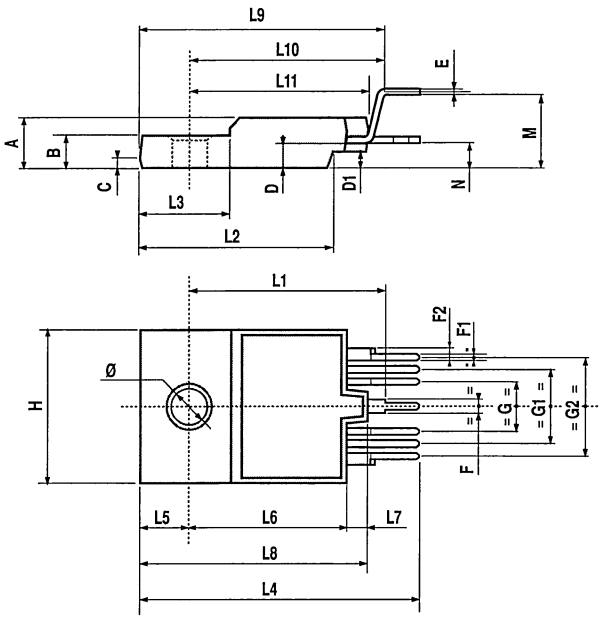
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	5.35		5.65	0.210		0.222
B	3.4		3.7	0.133		0.145
C	0.8		1.28	0.031		0.050
D	2.95		3.1	0.116		0.122
D1	1.95		2.15	0.076		0.084
E	0.5		0.6	0.019		0.023
F		1.1			0.043	
F1	0.7		0.8	0.027		0.031
F2		1.4			0.055	
G	4.88		5.28	0.192		0.207
G1	7.42		7.82	0.292		0.308
G2	9.96		10.36	0.392		0.408
H	15.9		16.1	0.626		0.634
L1	19.85		20.15	0.781		0.793
L2	19.35		19.65	0.761		0.773
L3	8.9		9.1	0.350		0.358
L4	28		29	1.102		1.141
L5	4.9		5.1	0.193		0.201
L6	15.9		16.1	0.626		0.634
L7	2.1		2.3	0.082		0.090
L8	23		23.4	0.905		0.921
L9	24.8		25.2	0.976		0.992
L10	19.8		20.2	0.779		0.795
L11	17.7		18.3	0.697		0.720
M	7.83		8.33	0.308		0.328
N	2.75		3.25	0.108		0.128
Ø	3.5		3.7	0.138		0.145

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



ISOWATT7

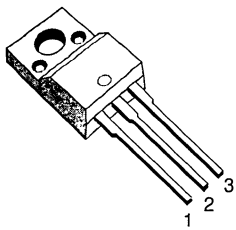


P033B

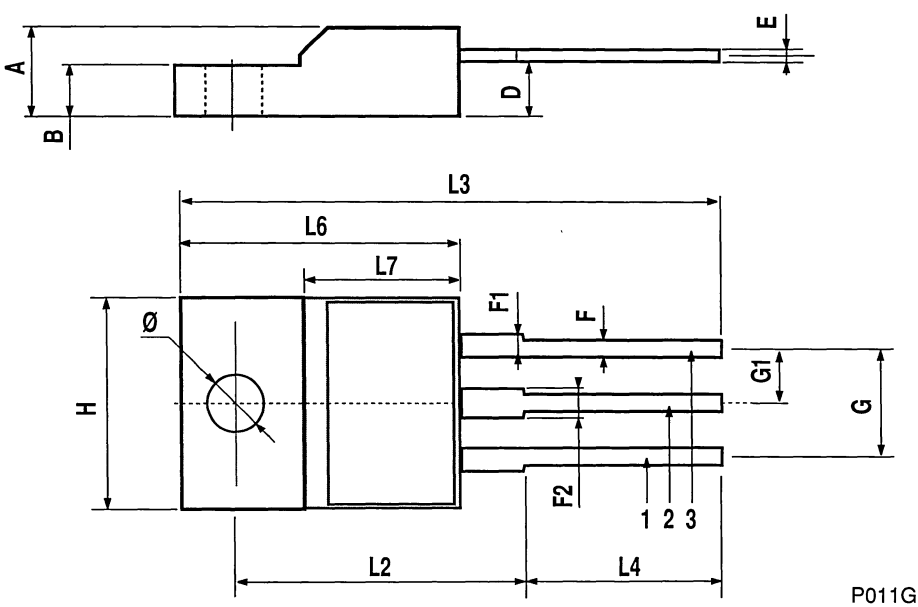
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		3.66
Ø	3		3.2	0.118		0.126

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



ISOWATT220

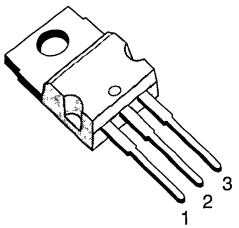


P011G

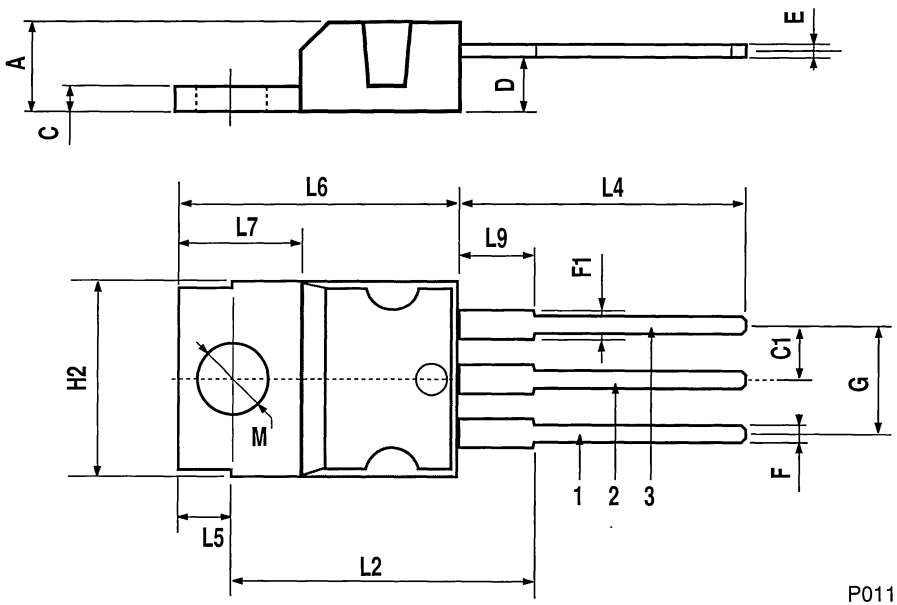
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.4		2.72	0.094		0.107
E	0.41		0.64	0.016		0.025
F	0.61		0.94	0.024		0.037
F1	1.14		1.7	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10		10.4	0.393		0.409
L2		17.6			0.692	
L4	12.7		13.7	0.500		0.539
L5	2.65		2.95	0.104		0.116
L6	15.2		15.9	0.598		0.626
L7	6.2		6.6	0.244		0260
L9	3.5		5.5	0.137		0.216
M	3.75		3.85	0.147		0.151

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



TO-220 (DSG)



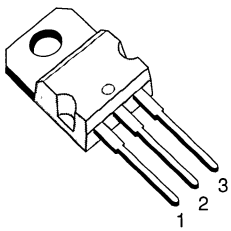
P011C

Phasing out during 1993 (see next page)

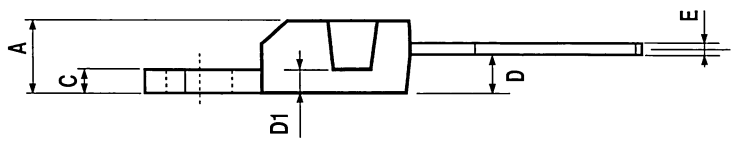
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.2		15.9	0.598		0.625
L7	6.2		6.6	0.244		0.260
L9	3.5		4.2	0.137		0.165
DIA.	3.75		3.85	0.147		0.151

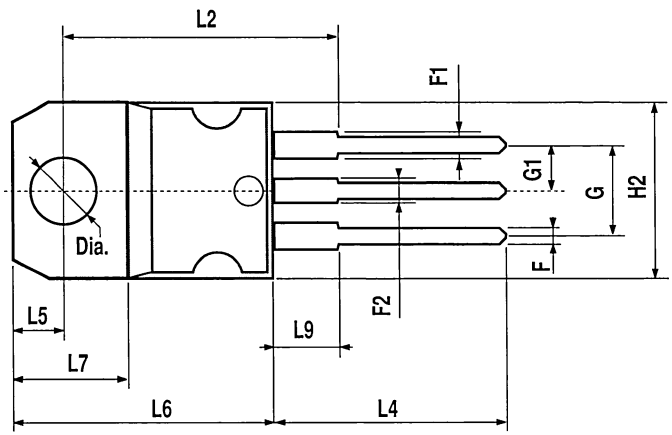
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



TO-220 (DSG new Version)



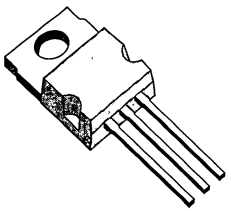


Introduced starting Q4 1992

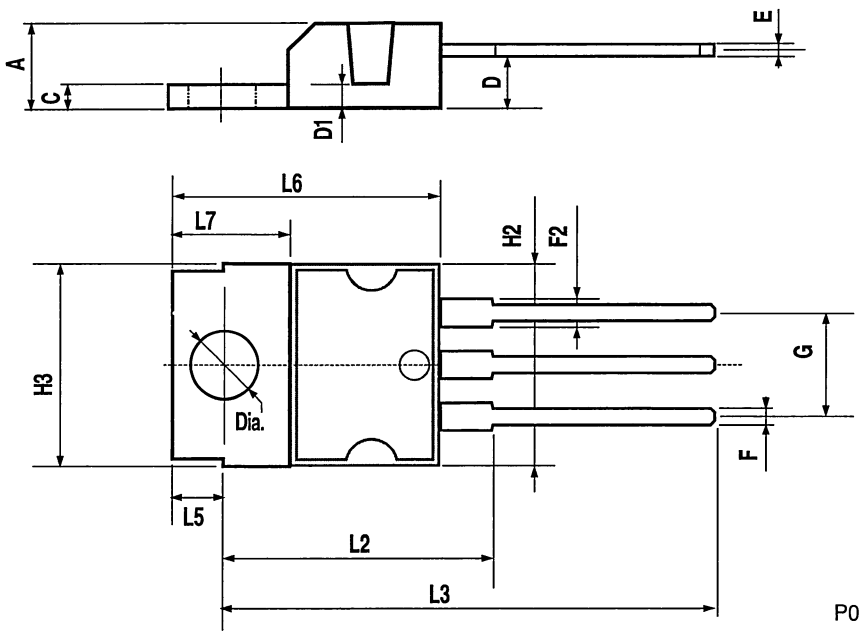
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F2	1.15		1.4	0.045		0.055
G	4.95	5.08	5.21	0.195	0.200	0.205
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L2		16.2			0.638	
L3	26.3	26.7	27.1	1.035	1.051	1.067
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



TO220

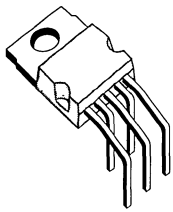


P011D

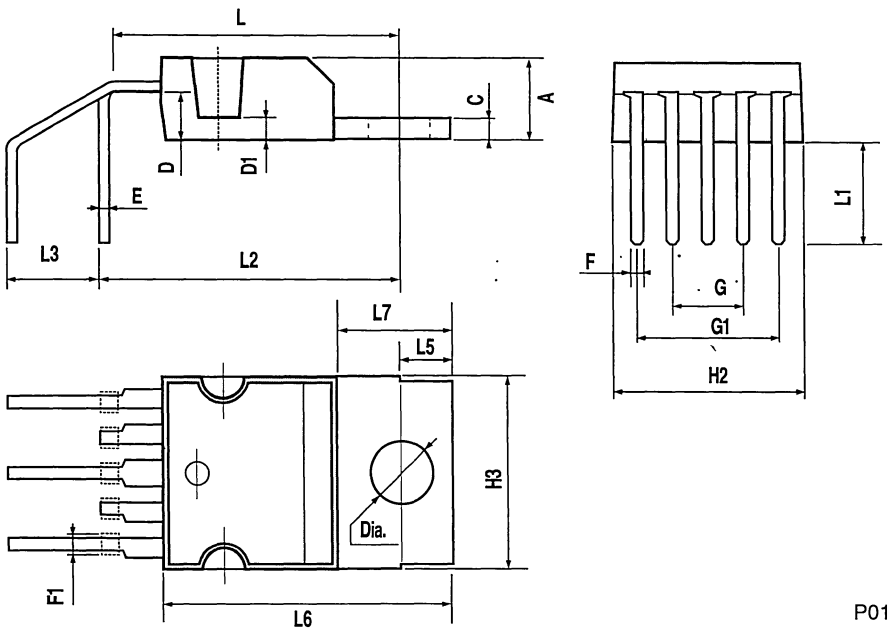
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G		3.4			0.134	
G1		6.8			0.268	
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		14.2			0.559	
L1		6			0.236	
L2		14.8			0.583	
L3		4.0			0.157	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Pentawatt H

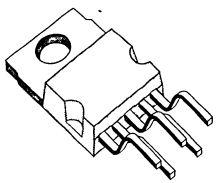


P010F

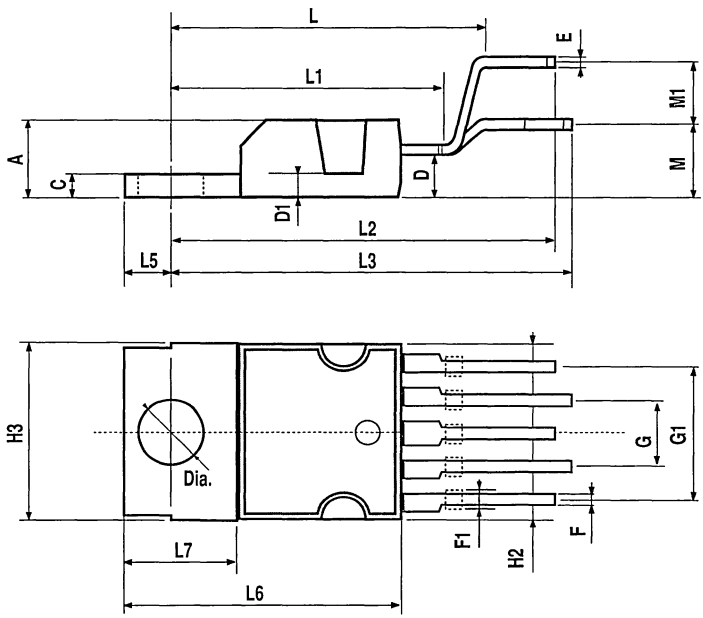
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G		3.4			0.134	
G1		6.8			0.268	
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Pentawatt V

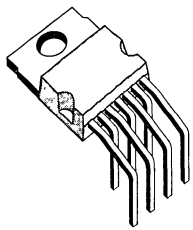


P010E

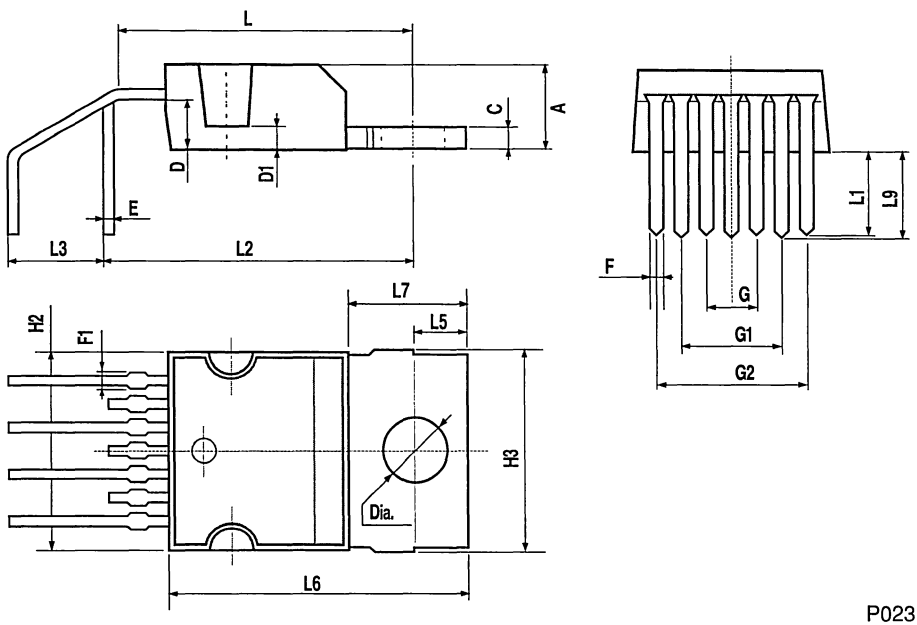
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G		2.54			0.100	
G1		5.08			0.200	
G2		7.62			0.300	
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		14.2			0.559	
L1		4.4			0.173	
L2		15.8			0.622	
L3		5.1			0.201	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
L9		4.44			0.175	
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Heptawatt H

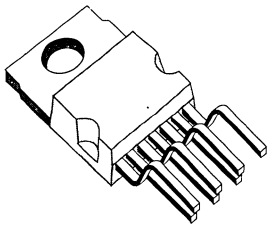


P023B

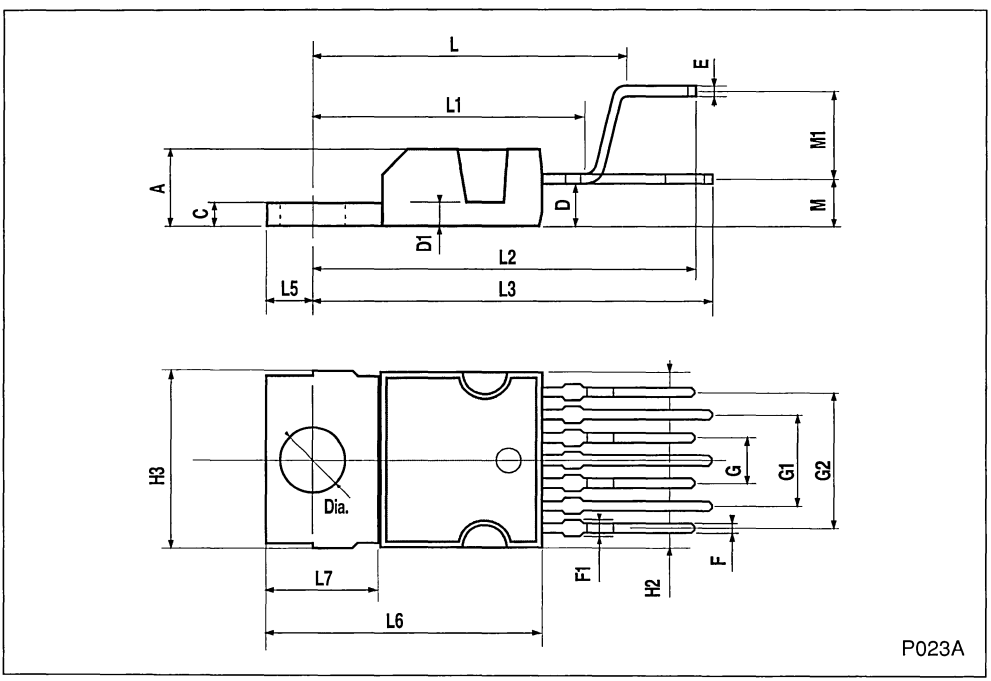
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G		2.54			0.100	
G1		5.08			0.200	
G2		7.62			0.300	
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



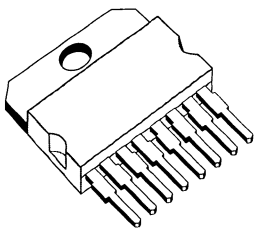
Heptawatt V



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.78		0.85	0.030		0.033
G	2.40	2.54	2.68	0.094	0.10	0.105
G1	17.64	17.78	17.92	0.69	0.70	0.71
H1	19.6			0.772		
H2			20.2			0.795
L	20.35		20.65	0.80		0.81
L1		15.7			0.62	
L2	17.05	17.20	17.35	0.67	0.68	0.68
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
U	0.40		0.55	0.015		0.022
Z	0.70		0.85	0.028		0.034
Dia1	3.65		3.85	0.144		0.152

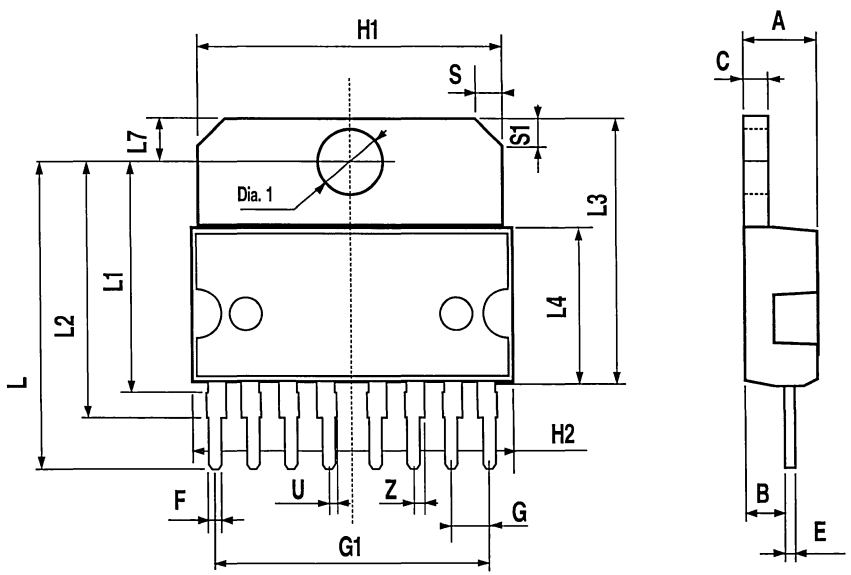
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Multiwatt8 (Pin. 5 Gnd) (*)

(*) Advanced information on a new package now in development or undergoing evaluation. Details are subject to change without notice.

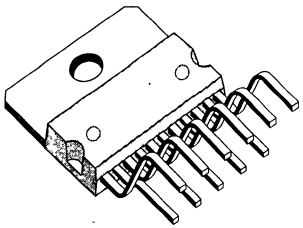


P017L

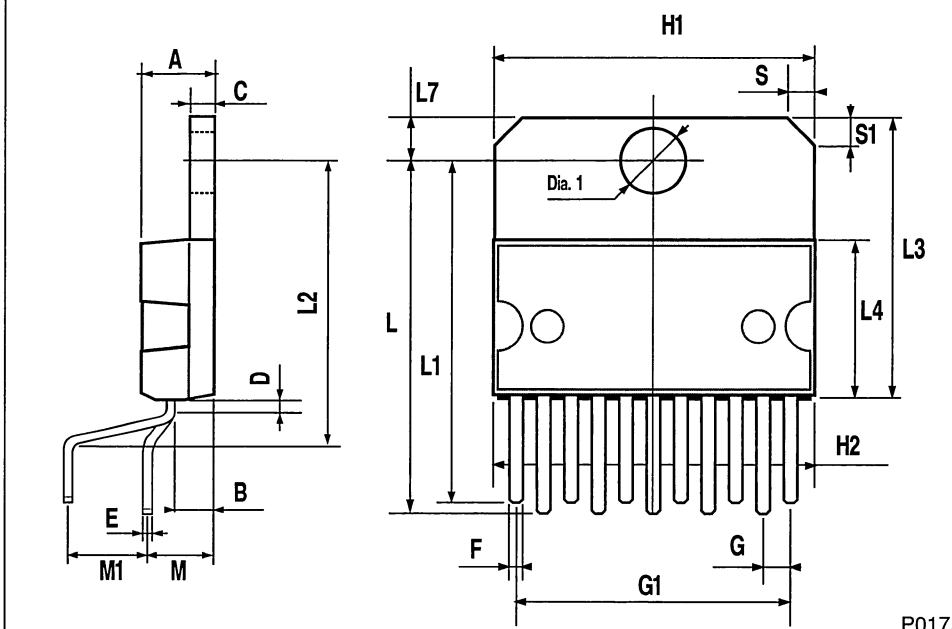
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.88		0.95	0.035		0.037
G	1.57	1.7	1.83	0.062	0.067	0.072
G1	16.87	17	17.13	0.664	0.669	0.674
H1	19.6			0.772		
H2			20.2			0.795
L	21.5		22.3	0.846		0.878
L1	21.4		22.2	0.843		0.874
L2	17.4		18.1	0.685		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.1	4.3	4.5	0.161	0.169	0.177
M1	4.88	5.08	5.3	0.192	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



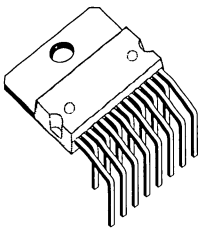
Multiwatt11 V



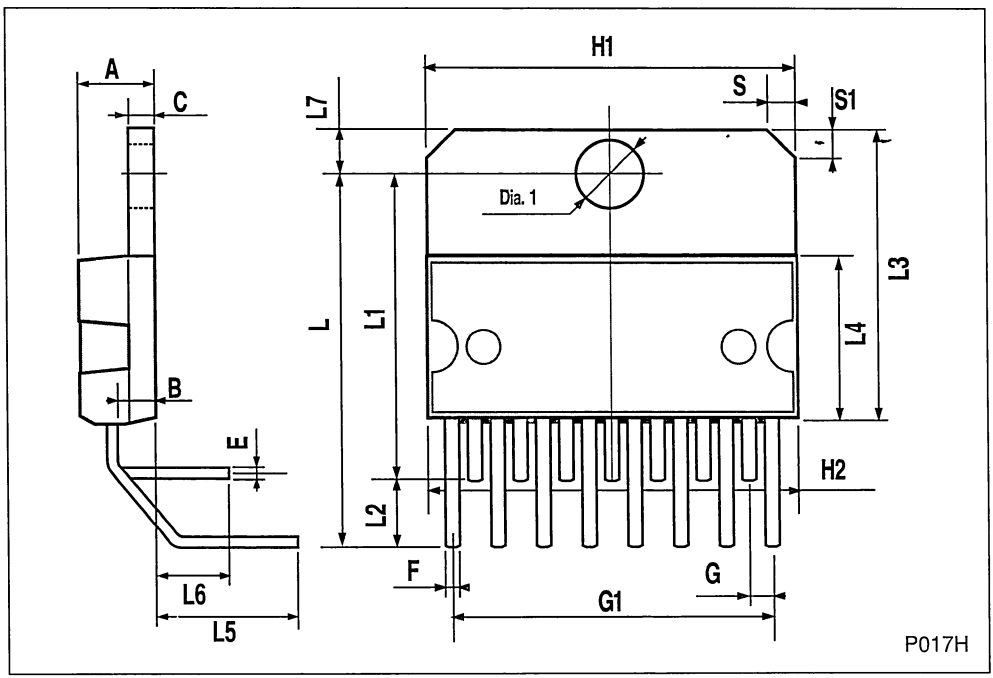
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L		20.57			0.810	
L1		18.03			0.710	
L2		2.54			0.100	
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L5		5.28			0.208	
L6		2.38			0.094	
L7	2.65		2.9	0.104		0.114
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Multiwatt15 H

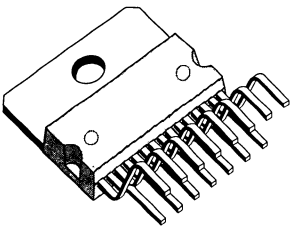


P017H

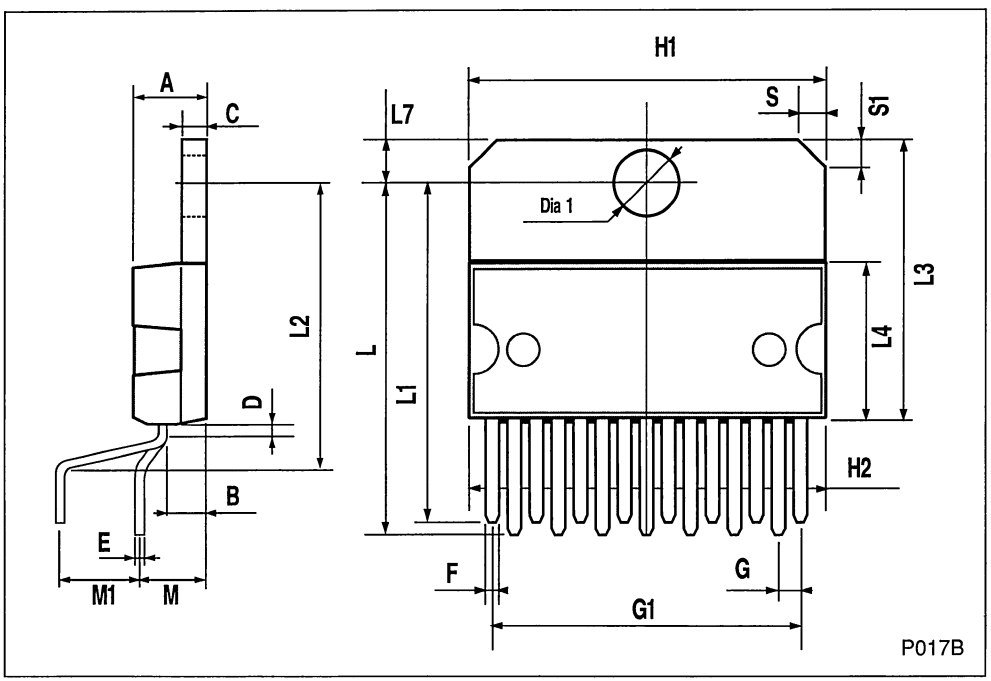
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



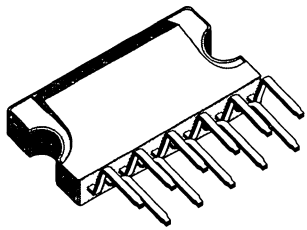
Multiwatt15 V



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.10			0.122
B			1.10			0.04
C		0.15			0.006	
D		1.50			0.059	
E		0.52			0.02	
F		0.80			0.03	
G		1.70			0.066	
G1		17.00			0.66	
H1		12.00			0.48	
H3		20.00			0.79	
L		17.90			0.70	
L1		14.40			0.57	
L2		11.00			0.43	
M		2.54			0.1	

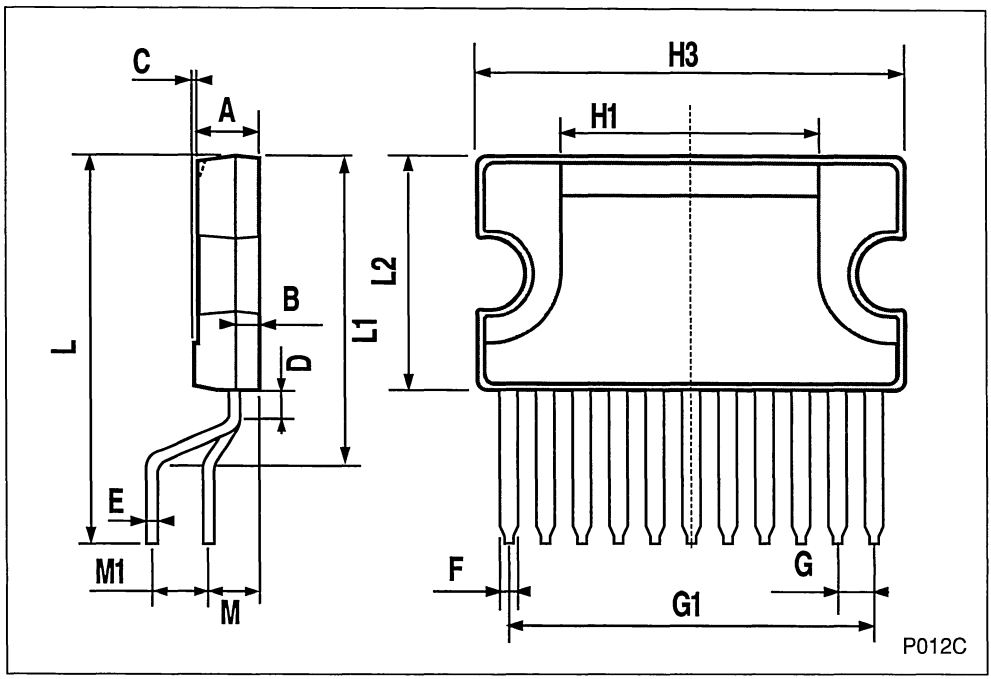
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Clipwatt11 (*)

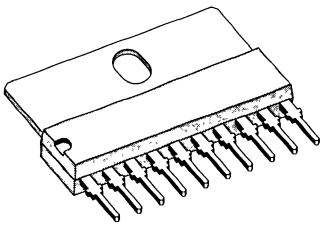
(*) Advanced information on a new package now in development or undergoing evaluation. Details are subject to change without notice.



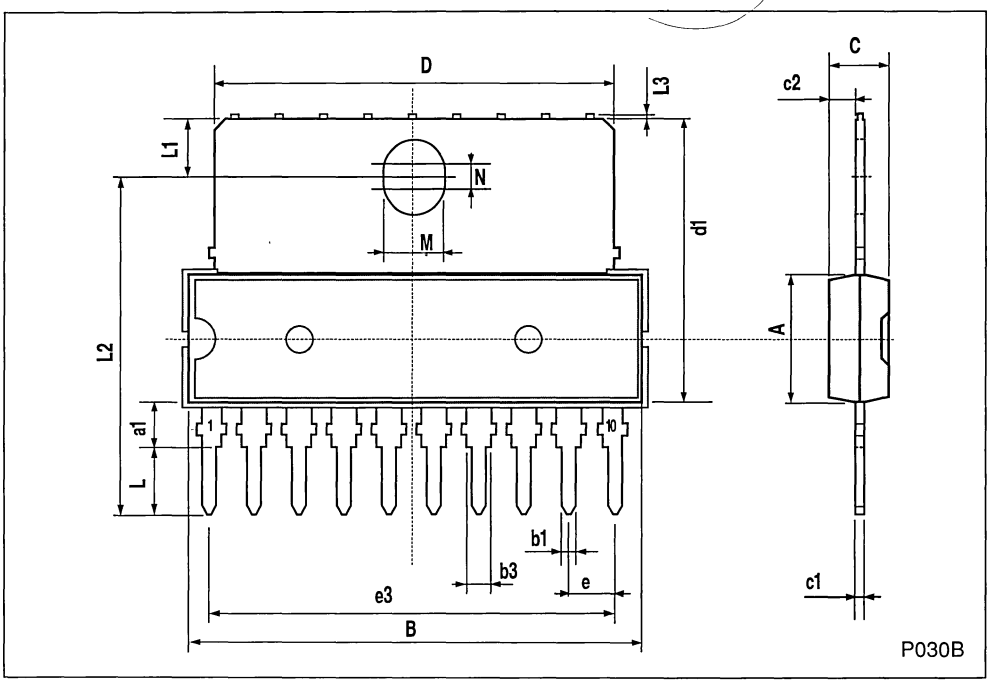
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			23.7			0.933
d1		14.5			0.571	
e		2.54			0.100	
e3		22.86			0.900	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



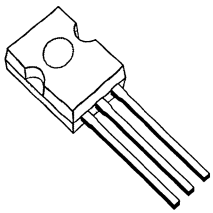
SIP10



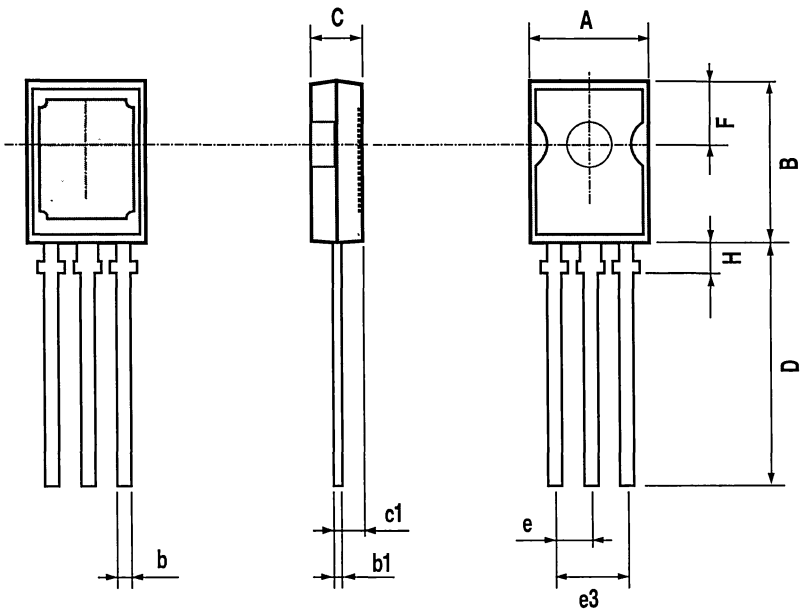
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		10.8	0.413		0.425
b	0.7		0.9	0.028		0.035
b1	0.49		0.75	0.019		0.030
C	2.4		2.7	0.094		0.106
c1		1.2			0.047	
D		15.7			0.618	
e		2.2			0.087	
e3		4.4			0.173	
F		3.8			0.150	
H			2.54		0.100	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SOT82

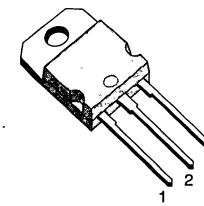


P032A

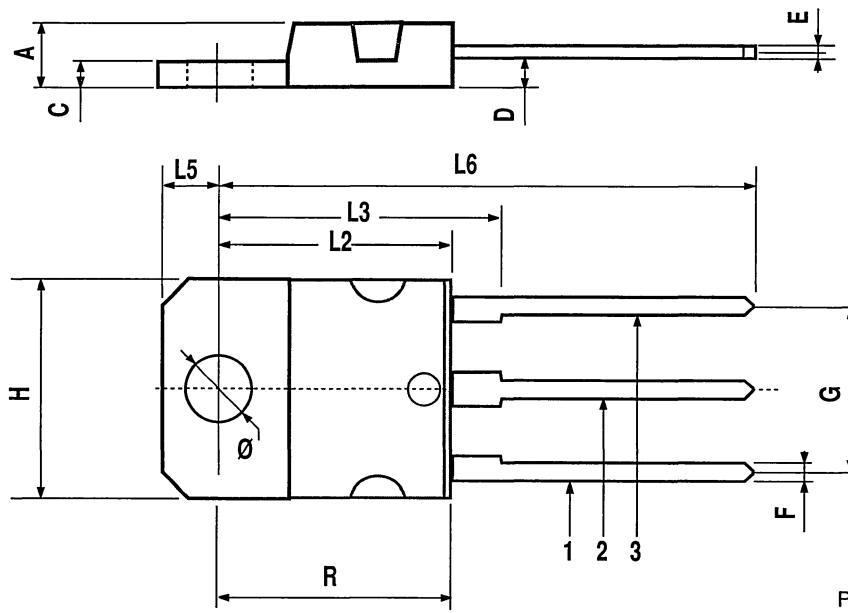
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		4.9	0.185		0.193
C	1.9		2.1	0.075		0.082
D		2.5			0.098	
E	0.5		0.78	0.019		0.030
F	1.1		1.3	0.043		0.051
G	10.8		11.1	0.425		0.437
H	14.7		15.2	0.578		0.598
L2	–		16.2	–		0.637
L3		18			0.708	
L5	3.95		4.15	0.155		0.163
L6		31			1.220	
R	–		12.2	–		0.480
Ø	4		4.1	0.157		0.161

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



TO-218 (SOT-93)



SALES OFFICES

EUROPE

DENMARK

2730 HERLEV
Herlev Torv, 4
Tel (45-44) 94 85 33
Telex 35411
Telefax (45-44) 948694

FINLAND

LOHJA SF-08150
Katakatu, 26
Tel (358-12) 155 11
Telefax (358-12) 155 66

FRANCE

94253 GENTILLY Cedex
7 - avenue Gallieni - BP 93
Tel (33-1) 47.40 75 75
Telex. 632570 STMHQ
Telefax. (33-1) 47 40 79 10

67000 STRASBOURG
20, Place des Halles
Tel (33-88) 75 50 66
Telefax (33-88) 22 29 32

GERMANY

8011 GRASBRUNN
Bretonischer Ring 4
Postfach 1122
Tel · (49-89) 460060
Telefax (49-89) 4605454
Teletex 897107=STDISTR

1000 BERLIN 37
Clay Allee 323
Tel (49-30) 8017087-89
Telefax (49-30) 8015552

6000 FRANKFURT
Gutleutstrasse 322
Tel (49-69) 237492-3
Telefax (49-69) 231957
Teletex 6997689=STVBF

3000 HANNOVER 51
Rotenburger Strasse 28A
Tel (49-511) 615960-3
Teletex 5118418 CSFBEH
Telefax (49-511) 6151243

8500 NÜRNBERG 20
Erlenstegenstrasse, 72
Tel (49-911) 59893-0
Telefax (49-911) 5980701

7000 STUTTGART 31
Mittlerer Pfad 2-4
Tel. (49-711) 13968-0
Telefax (49-711) 8661427

ITALY

20090 ASSAGO (MI)
V.le Milanofiori - Strada 4 - Palazzo A/4/A
Tel. (39-2) 89213 1 (10 linee)
Telex 330131 - 330141 SGSAGR
Telefax (39-2) 8250449

40033 CASALECCHIO DI RENO (BO)
Via R Fucini, 12
Tel (39-51) 593029
Telex· 512442
Telefax (39-51) 591305

00161 ROMA
Via A Torlonia, 15
Tel (39-6) 8443341
Telex 620653 SGSATE I
Telefax (39-6) 8444474

NETHERLANDS

5652 AR EINDHOVEN
Meerenakkerweg 1
Tel (31-40) 550015
Telex· 51186
Telefax· (31-40) 528835

SPAIN

08021 BARCELONA
Calle Platon, 6 4th Floor, 5th Door
Tel. (34-3) 4143300-4143361
Telefax. (34-3) 2021461

28027 MADRID
Calle Albacete, 5
Tel (34-1) 4051615
Telex 46033 TCCEE
Telefax (34-1) 4031134

SWEDEN

S-16421 KISTA
Borgarfjordsgatan, 13 - Box 1094
Tel · (46-8) 7939220
Telex· 12078 THSWS
Telefax (46-8) 7504950

SWITZERLAND

1218 GRAND-SACONNEX (GENEVA)
Chemin Francois-Lehmann, 18/A
Tel (41-22) 7986462
Telex· 415493 STM CH
Telefax. (41-22) 7984869

UNITED KINGDOM and EIRE

MARLOW, BUCKS
Planar House, Parkway
Globe Park
Tel (44-628) 890800
Telex 847458
Telefax (44-628) 890391

AMERICAS

BRAZIL

05413 SÃO PAULO
R Henrique Schaumann 286-CJ33
Tel (55-11) 883-5455
Telex· (391)11-37988 "UMBR BR"
Telefax · (55-11) 282-2367

CANADA

NEPEAN ONTARIO
301 Moodie Drive
Suite 307
Tel 613/829-9944

U.S.A.

NORTH & SOUTH AMERICAN
MARKETING HEADQUARTERS
1000 East Bell Road
Phoenix, AZ 85022
(1-602) 867-6100

SALES COVERAGE BY STATE

ALABAMA
Huntsville - (205) 533-5995

ARIZONA
Phoenix - (602) 867-6217

CALIFORNIA
Santa Ana - (714) 957-6018
San Jose - (408) 452-8585

COLORADO
Boulder (303) 449-9000

ILLINOIS
Schaumburg - (708) 517-1890

INDIANA
Kokomo - (317) 455-3500

MASSACHUSETTS
Lincoln - (617) 259-0300

MICHIGAN
Livonia - (313) 953-1700

NEW JERSEY
Voorhees - (609) 772-6222

NEW YORK
Poughkeepsie - (914) 454-8813

NORTH CAROLINA
Raleigh - (919) 787-6555

TEXAS
Carrollton - (214) 466-8844

FOR RF AND MICROWAVE
POWER TRANSISTORS CON-
TACT
THE FOLLOWING REGIONAL
OFFICE IN THE U.S.A.

PENNSYLVANIA
Montgomeryville - (215) 361-6400

ASIA / PACIFIC

AUSTRALIA

NSW 2220 HURTSVILLE
Suite 3, Level 7, Otis House
43 Bridge Street
Tel (61-2) 5803811
Telefax (61-2) 5806440

HONG KONG

WANCHAI
22nd Floor - Hopewell centre
183 Queen's Road East
Tel (852) 8615788
Telex 60955 ESGIES HX
Telefax (852) 8656589

INDIA

NEW DELHI 110001
LiasonOffice
62, Upper Ground Floor
World Trade Centre
Barakhamba Lane
Tel (91-11) 3715191
Telex 031-66816 STMI IN
Telefax· (91-11) 3715192

MALAYSIA

PETALING JAYA, 47400
11C, Jalan SS21/60
Damansara Utama
Tel (03) 717 3976
Telefax (03) 719 9512

PULAU PINANG 10400
4th Floor - Suite 4-03
Bangunan FOP-123D Jalan Anson
Tel (04) 379735
Telefax (04) 379816

KOREA

SEOUL 121
8th floor Shinwon Building
823-14, Yuksam-Dong
Kang-Nam-Gu
Tel (82-2) 553-0399
Telex SGSKOR K29998
Telefax (82-2) 552-1051

SINGAPORE

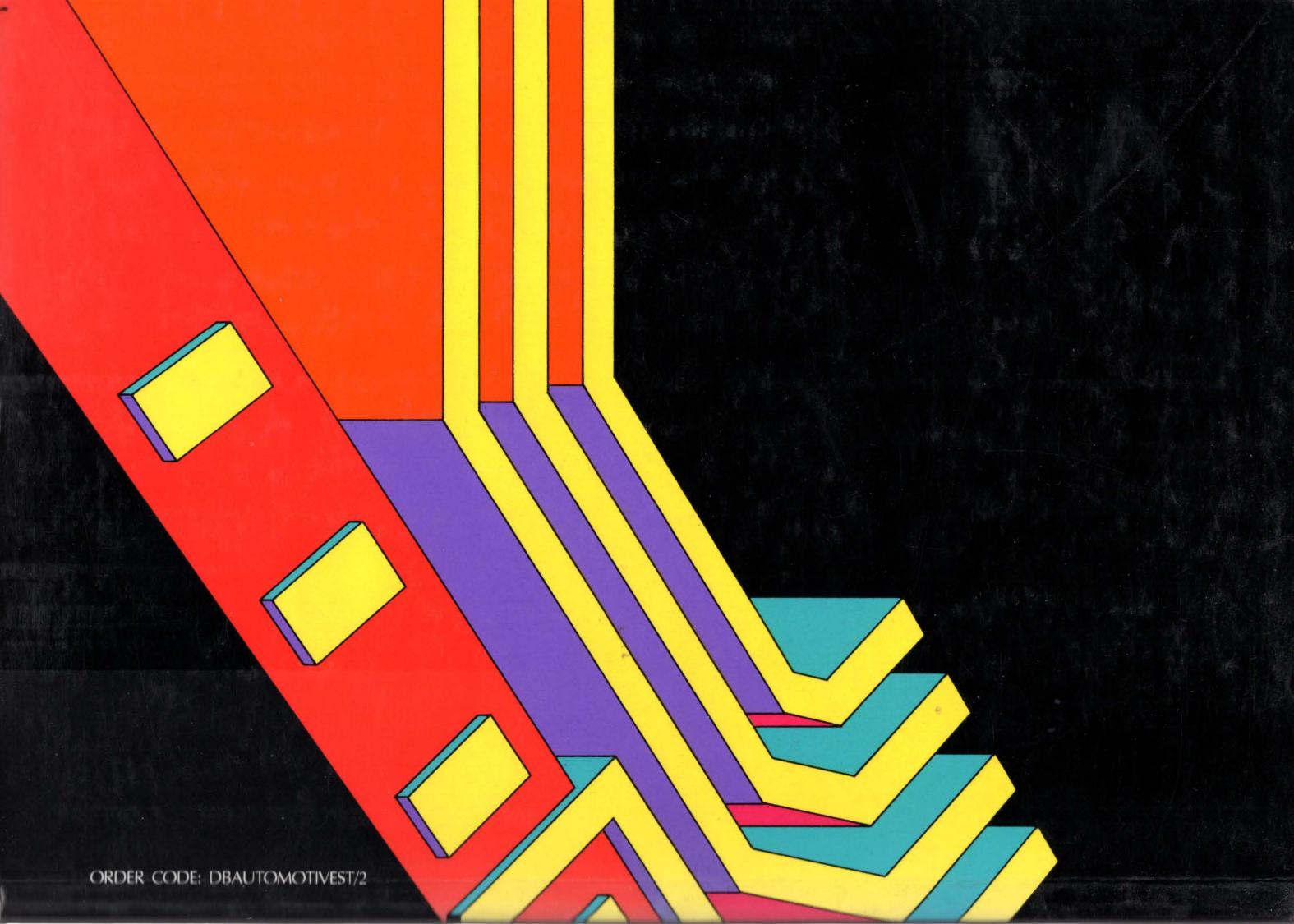
SINGAPORE 2056
28 Ang Mo Kio - Industrial Park 2
Tel (65) 4821411
Telex RS 55201 ESGIES
Telefax (65) 4820240

TAIWAN

TAIPEI
12th Floor
325, Section 1 Tun Hua South Road
Tel (886-2) 755-4111
Telex 10310 ESGIE TW
Telefax (886-2) 755-4008

JAPAN

TOKYO 108
Nisseki - Takanawa Bld 4F
2-18-10 Takanawa
Minato-Ku
Tel (81-3) 3280-4121
Telefax (81-3) 3280-4131



ORDER CODE: DBAUTOMOTIVEST/2