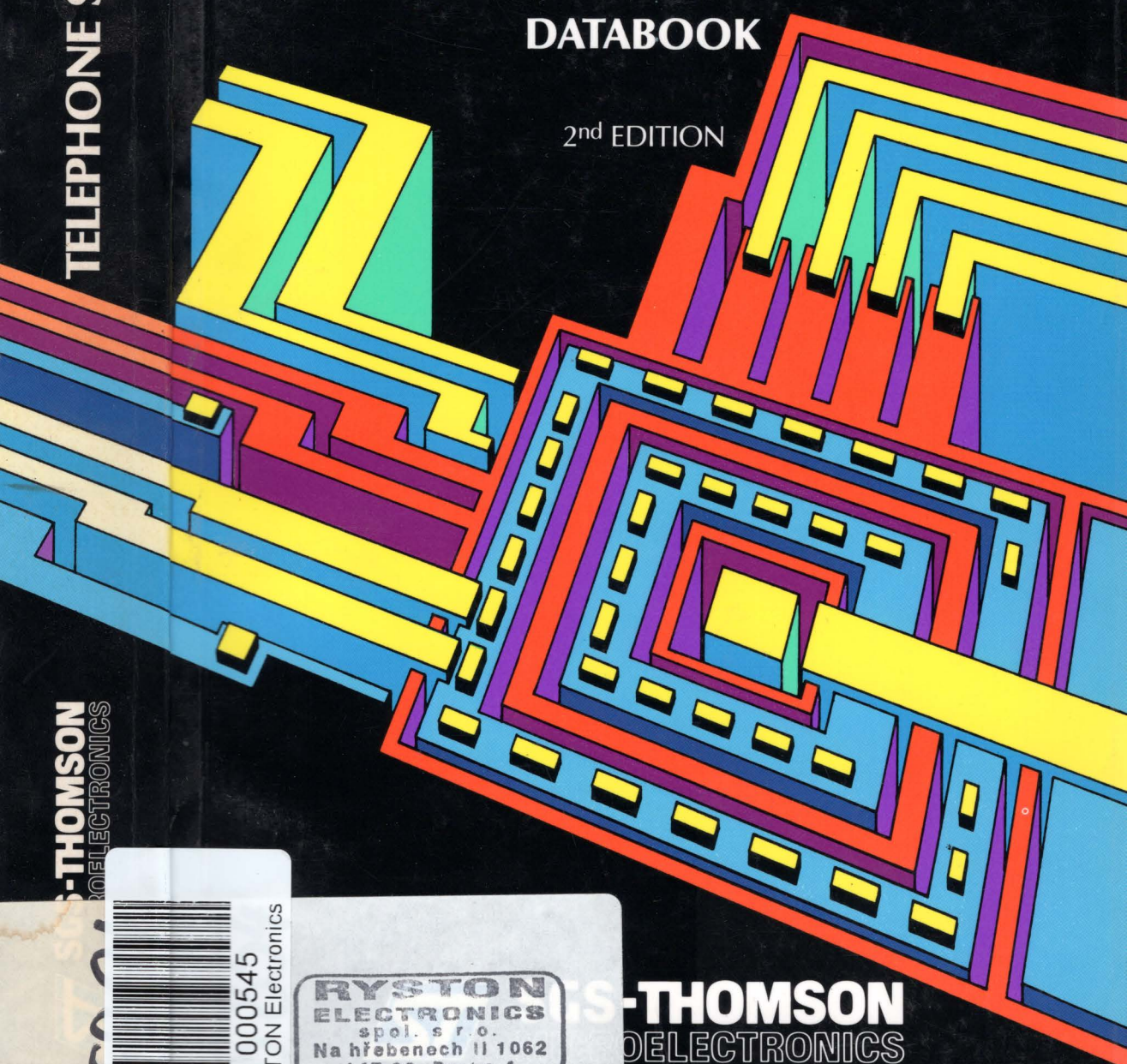
TELEPHONE SET ICs

DATABOOK

2nd EDITION



THOMSON
SEMICONDUCTORS
ELECTRONICS

TELEPHONE SET ICs

TELEPHONE SET ICs

DATABOOK

2nd EDITION

DECEMBER 1993

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED 545

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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SGS-THOMSON IN TELEPHONE SET IC MARKET: THE WORLDWIDE SUPPLIER

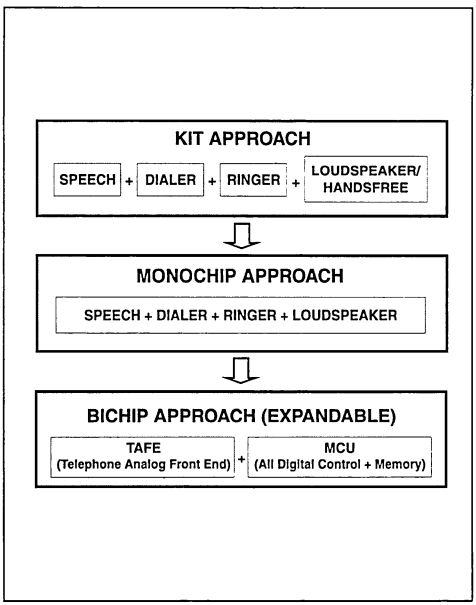
SGS-THOMSON Microelectronics has been designing and producing dedicated integrated circuits for telephone sets for two decades.

Today the company offers the widest product range and probably manufactures more telephone ICs than any other company in the world -- about 60 million ICs per year, not including protection devices and memories.

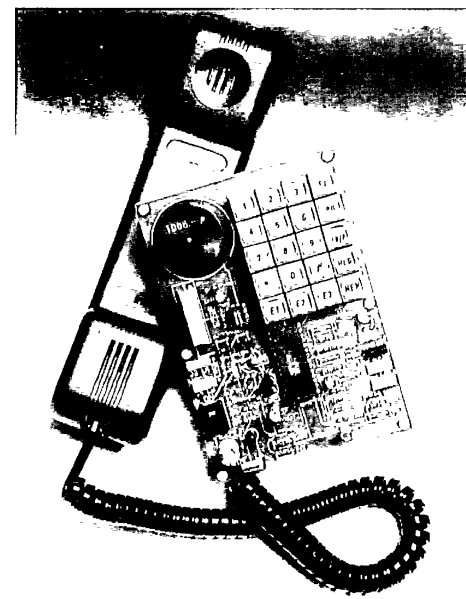
The SGS-THOMSON portfolio for analog telephone sets is moving from the traditional domain of single functions (speech, dialer, ringer, handsfree) to a more integrated approach with single chip phones, "spedials" (speech + repertory dialer) and various two-chip solutions (analog section IC + MCU).

While the individual functions still constitute the core of the current production activity, the new concept of a two-chip solution is generating the real added value in the telephones of the nineties. The idea is to combine a single analog chip, able to handle all of the Telephone Analog Front End (TAFE) functions, with a microcontroller unit (MCU), taking care of all logic activities. The two ICs can be separately upgraded in order to provide flexibility for different markets and modular growth of the functions offered.

In parallel with the consolidation of the traditional offerings in the corded analog telephone domain, new products appear in the wider scenario of digital corded, ISDN and cordless (analog and digital) telephones.



EVOLUTION OF ANALOG TELEPHONE FUNCTION



ADVANCED TECHNOLOGY. Using an advanced CMOS Technology SGS-THOMSON has produced the L3916 SPEDIAL Family (Speech + Repertory Dialer).

ALPHANUMERICAL INDEX

Type Number	Function	Page Number
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EFG71891	DTMF Generation for Binary Coded Hexadecimal Data	19
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LS204	High Performance Dual Operational Amplifier	487
LS256	Speech Circuit with Multifrequency Tone Generator Interface	87
LS285	Telephone Speech Circuit	93
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LS588	Programmable Telephone Speech Circuit	101
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ST6294	8-Bit HCMOS MCU with A/D Converter EEPROM & Auto-Reload Timer	469
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SELECTION GUIDE

SPEECH CIRCUITS

Type	Function	Package	Page
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LS285	Telephone Speech Circuit	DIP16	93
LS588	Programmable Telephone Speech Circuits	DIP16	101
LS656	Speech Circuit with Multifrequency Tone Generator Interface	DIP16/SO20L	111
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LOUDSPEAKING

Type	Function	Package	Page
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Type	Function	Package	Page
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Type	Function	Package	Page
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L3914	Low Range One Chip Phone (Speech and Dialer)	DIP28/SO28	63
L3916	Low Range One Chip Phone (Speech and Dialer)	DIP28/SO28	75
TEA7088	Low Range Phone Dedicated Analog Front End	DIP28/SO28	395
TEA7090	Low Range Phone Dedicated Analog Front End	DIP28/SO28	399
TEA7091	Telephone Analog Front End	PLCC44/PQFP44	415

(*) Replaced by TEA7532 for New Designs

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Type	Function	Package	Page
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MK53732	Tone Pulse Dialer with Last Number and Save Function	DIP18/SO20	149
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Type	Function	Package	Page
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Type	Function	Package	Page
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ST5088	Programmable ISDN Audio Front End	PLCC28	223
STH221	Muldex IC for Multimedia Teleservices	PQFP64	325
ST5421	SID-GCI: S/T Interface Device with GCI	DIP20	253
ST5451	ISDN HDLC and GCI Controller	DIP28/SO28	279

CORDLESS

Type	Function	Package	Page
ST7162	Universal Programmable Dual PLL	DIP16/SO16	311
TDA7233	1W Audio Amplifier with Mute	Minidip	355
TDA7233D	1W Audio Amplifier with Mute	SO8	355
TDA7326	AM-FM Radio Frequency Synthesizer	DIP16/SO16L	359

EEPROM, I^2C Serial Access Bus

Size	Part Number	Organis.	Vcc min (V)	Feature	Temp. Range (°C)	Package
1K	ST24C01B1	128 x 8	4.5	Byte/Page Write	0 to 70	PSDIP8
	ST24W01B1	128 x 8	4.5	Write Control	0 to 70	PSDIP8
	ST24C01CB1	128 x 8	3.0	Byte/Page Write	0 to 70	PSDIP8
	ST24W01CB1	128 x 8	3.0	Write Control	0 to 70	PSDIP8
	ST25C01B1	128 x 8	2.5	Byte/Page Write	0 to 70	PSDIP8
	ST25C01CB1	128 x 8	2.5	Byte/Page Write	0 to 70	PSDIP8
	ST25W01CB1	128 x 8	2.5	Write Control	0 to 70	PSDIP8
	ST24C01B6	128 x 8	4.5	Byte/Page Write	–40 to 85	PSDIP8
	ST24W01B6	128 x 8	4.5	Write Control	–40 to 85	PSDIP8
	ST24C01CB6	128 x 8	3.0	Byte/Page Write	–40 to 85	PSDIP8
	ST24W01CB6	128 x 8	3.0	Write Control	–40 to 85	PSDIP8
	ST25C01B6	128 x 8	2.5	Byte/Page Write	–40 to 85	PSDIP8
	ST25C01CB6	128 x 8	2.5	Byte/Page Write	–40 to 85	PSDIP8
	ST25W01CB6	128 x 8	2.5	Write Control	–40 to 85	PSDIP8
	ST24C01M1	128 x 8	4.5	Byte/Page Write	0 to 70	SO8
	ST24C01M1013TR	128 x 8	4.5	Byte/Page Write	0 to 70	SO8TR
	ST24W01M1	128 x 8	4.5	Write Control	0 to 70	SO8
	ST24W01M1013TR	128 x 8	4.5	Write Control	0 to 70	SO8TR
	ST24C01CM1	128 x 8	3.0	Byte/Page Write	0 to 70	SO8
	ST24C01CM1TR	128 x 8	3.0	Byte/Page Write	0 to 70	SO8TR
	ST24W01CM1	128 x 8	3.0	Write Control	0 to 70	SO8
	ST24W01CM1TR	128 x 8	3.0	Write Control	0 to 70	SO8TR

Size	Part Number	Organis.	Vcc min (V)	Feature	Temp. Range (°C)	Package
1K	ST25C01CM1	128 x 8	2.5	Byte/Page Write	0 to 70	SO8
	ST25C01CM1TR	128 x 8	2.5	Byte/Page Write	0 to 70	SO8TR
	ST25C01M1	128 x 8	2.5	Byte/Page Write	0 to 70	SO8
	ST25C01M1013TR	128 x 8	2.5	Byte/Page Write	0 to 70	SO8TR
	ST25W01CM1	128 x 8	2.5	Write Control	0 to 70	SO8
	ST25W01CM1TR	128 x 8	2.5	Write Control	0 to 70	SO8TR
	ST24C01M6	128 x 8	4.5	Byte/Page Write	–40 to 85	SO8
	ST24C01M6013TR	128 x 8	4.5	Byte/Page Write	–40 to 85	SO8TR
	ST24W01M6	128 x 8	4.5	Write Control	–40 to 85	SO8
	ST24W01M6013TR	128 x 8	4.5	Write Control	–40 to 85	SO8TR
	ST24C01CM6	128 x 8	3.0	Byte/Page Write	–40 to 85	SO8
	ST24C01CM6TR	128 x 8	3.0	Byte/Page Write	–40 to 85	SO8TR
	ST24W01CM6	128 x 8	3.0	Write Control	–40 to 85	SO8
	ST24W01CM6TR	128 x 8	3.0	Write Control	–40 to 85	SO8TR
	ST25C01CM6	128 x 8	2.5	Byte/Page Write	–40 to 85	SO8
	ST25C01CM6TR	128 x 8	2.5	Byte/Page Write	–40 to 85	SO8TR
	ST25C01M6	128 x 8	2.5	Byte/Page Write	–40 to 85	SO8
	ST25C01M6013TR	128 x 8	2.5	Byte/Page Write	–40 to 85	SO8TR
	ST25W01CM6	128 x 8	2.5	Write Control	–40 to 85	SO8
	ST25W01CM6TR	128 x 8	2.5	Write Control	–40 to 85	SO8TR
	ST24C01M3	128 x 8	4.5	Byte/Page Write	–40 to 125	SO8

EEPROM, I^2C Serial Access Bus (cont'd)

Size	Part Number	Organis.	V_{CC} min (V)	Feature	Temp. Range (°C)	Package
2K	ST24C02AB1	256 x 8	3.0	Byte/Page Write	0 to 70	PSDIP8
	ST24C02AB1/AAB	256 x 8	3.0	Content all 00	0 to 70	PSDIP8
	ST24C02CB1	256 x 8	3.0	Byte/Page Write	0 to 70	PSDIP8
	ST24W02CB1	256 x 8	3.0	Write Control	0 to 70	PSDIP8
	ST25C02AB1	256 x 8	2.5	Byte/Page Write	0 to 70	PSDIP8
	ST25C02CB1	256 x 8	2.5	Byte/Page Write	0 to 70	PSDIP8
	ST25W02CB1	256 x 8	2.5	Write Control	0 to 70	PSDIP8
	ST24C02AB6	256 x 8	3.0	Byte/Page Write	–40 to 85	PSDIP8
	ST24C02CB6	256 x 8	3.0	Byte/Page Write	–40 to 85	PSDIP8
	ST24W02CB6	256 x 8	3.0	Write Control	–40 to 85	PSDIP8
	ST25C02AB6	256 x 8	2.5	Byte/Page Write	–40 to 85	PSDIP8
	ST25C02CB6	256 x 8	2.5	Byte/Page Write	–40 to 85	PSDIP8
	ST25W02CB6	256 x 8	2.5	Write Control	–40 to 85	PSDIP8
	ST24C02CB3	256 x 8	3.0	Byte/Page Write	–40 to 125	PSDIP8
	ST25C02CB3	256 x 8	2.5	Byte/Page Write	–40 to 125	PSDIP8
	ST24C02AB3	256 x 8	3.0	Byte/Page Write	–40 to 125	PSDIP8
	ST24C02AM1	256 x 8	3.0	Byte/Page Write	0 to 70	SO8
	ST24C02AM1013TR	256 x 8	3.0	Byte/Page Write	0 to 70	SO8TR
	ST24C02CM1	256 x 8	3.0	Byte/Page Write	0 to 70	SO8
	ST24C02CM1TR	256 x 8	3.0	Byte/Page Write	0 to 70	SO8TR
	ST24W02CM1	256 x 8	3.0	Write Control	0 to 70	SO8
	ST24W02CM1TR	256 x 8	3.0	Write Control	0 to 70	SO8TR

Size	Part Number	Organis.	V_{CC} min (V)	Feature	Temp. Range (°C)	Package
2K	ST25C02AM1	256 x 8	2.5	Byte/Page Write	0 to 70	SO8
	ST25C02AM1013TR	256 x 8	2.5	Byte/Page Write	0 to 70	SO8TR
	ST25C02CM1	256 x 8	2.5	Byte/Page Write	0 to 70	SO8
	ST25C02CM1TR	256 x 8	2.5	Byte/Page Write	0 to 70	SO8TR
	ST25W02CM1	256 x 8	2.5	Write Control	0 to 70	SO8
	ST25W02CM1TR	256 x 8	2.5	Write Control	0 to 70	SO8TR
	ST24C02AM6	256 x 8	3.0	Byte/Page Write	–40 to 85	SO8
	ST24C02AM6013TR	256 x 8	3.0	Byte/Page Write	–40 to 85	SO8TR
	ST24C02CM6	256 x 8	3.0	Byte/Page Write	–40 to 85	SO8
	ST24C02CM6TR	256 x 8	3.0	Byte/Page Write	–40 to 85	SO8TR
	ST24W02CM6	256 x 8	3.0	Write Control	–40 to 85	SO8
	ST24W02CM6TR	256 x 8	3.0	Write Control	–40 to 85	SO8TR
	ST25C02AM6	256 x 8	2.5	Byte/Page Write	–40 to 85	SO8
	ST25C02AM6013TR	256 x 8	2.5	Byte/Page Write	–40 to 85	SO8TR
	ST25C02CM6	256 x 8	2.5	Byte/Page Write	–40 to 85	SO8
	ST25C02CM6TR	256 x 8	2.5	Byte/Page Write	–40 to 85	SO8TR
	ST25W02CM6	256 x 8	2.5	Write Control	–40 to 85	SO8
	ST25W02CM6TR	256 x 8	2.5	Write Control	–40 to 85	SO8TR
	ST24C02AM3	256 x 8	3.0	Byte/Page Write	–40 to 125	SO8
4K	ST24C04B1	512 x 8	4.5	Write Protection	0 to 70	PSDIP8
	ST24C04CB1	512 x 8	3.0	Write Protection	0 to 70	PSDIP8
	ST24W04CB1	512 x 8	3.0	Write Control	0 to 70	PSDIP8
	ST25C04B1	512 x 8	2.5	Write Protection	0 to 70	PSDIP8

EEPROM, I^2C Serial Access Bus (cont'd)

Size	Part Number	Organis.	Vcc min (V)	Feature	Temp. Range (°C)	Package
4K	ST25C04CB1	512 x 8	2.5	Write Protection	0 to 70	PSDIP8
	ST25W04CB1	512 x 8	2.5	Write Control	0 to 70	PSDIP8
	ST24C04B6	512 x 8	4.5	Write Protection	–40 to 85	PSDIP8
	ST24C04CB6	512 x 8	3.0	Write Protection	–40 to 85	PSDIP8
	ST24W04CB6	512 x 8	3.0	Write Control	–40 to 85	PSDIP8
	ST25C04B6	512 x 8	2.5	Write Protection	–40 to 85	PSDIP8
	ST25C04CB6	512 x 8	2.5	Write Protection	–40 to 85	PSDIP8
	ST25W04CB6	512 x 8	2.5	Write Control	–40 to 85	PSDIP8
	ST24C04CB3	512 x 8	3.0	Write Protection	–40 to 125	PSDIP8
	ST24C04CM1	512 x 8	3.0	Write Protection	0 to 70	SO8
	ST24C04CM1TR	512 x 8	3.0	Write Protection	0 to 70	SO8TR
	ST24W04CM1	512 x 8	3.0	Write Control	0 to 70	SO8
	ST24W04CM1TR	512 x 8	3.0	Write Control	0 to 70	SO8TR
	ST25C04CM1	512 x 8	2.5	Write Protection	0 to 70	SO8
	ST25C04CM1TR	512 x 8	2.5	Write Protection	0 to 70	SO8TR
	ST25W04CM1	512 x 8	2.5	Write Control	0 to 70	SO8
	ST25W04CM1TR	512 x 8	2.5	Write Control	0 to 70	SO8TR
	ST24C04CM6	512 x 8	3.0	Write Protection	–40 to 85	SO8
	ST24C04CM6TR	512 x 8	3.0	Write Protection	–40 to 85	SO8TR
	ST24W04CM6	512 x 8	3.0	Write Control	–40 to 85	SO8
	ST24W04CM6TR	512 x 8	3.0	Write Control	–40 to 85	SO8TR
	ST25C04CM6	512 x 8	2.5	Write Protection	–40 to 85	SO8
	ST25C04CM6TR	512 x 8	2.5	Write Protection	–40 to 85	SO8TR
4K	ST25W04CM6	512 x 8	2.5	Write Control	–40 to 85	SO8
	ST25W04CM6TR	512 x 8	2.5	Write Control	–40 to 85	SO8TR
8K	ST24C08B1	1K x 8	4 5	Write Protection	0 to 70	PSDIP8
	ST24C08CB1	1K x 8	3.0	Write Protection	0 to 70	PSDIP8
	ST25C08CB1	1K x 8	2.5	Write Protection	0 to 70	PSDIP8
	ST24C08B6	1K x 8	4.5	Write Protection	–40 to 85	PSDIP8
	ST24C08CB6	1K x 8	3.0	Write Protection	–40 to 85	PSDIP8
	ST25C08CB6	1K x 8	2.5	Write Protection	–40 to 85	PSDIP8
	ST24C08CM1	1K x 8	3.0	Write Protection	0 to 70	SO8
	ST24C08CM1TR	1Kx 8	3.0	Write Protection	0 to 70	SO8TR
	ST25C08CM1	1K x 8	2.5	Write Protection	0 to 70	SO8
	ST25C08CM1TR	1Kx 8	2.5	Write Protection	0 to 70	SO8TR
	ST24C08CM6	1K x 8	3.0	Write Protection	–40 to 85	SO8
	ST24C08CM6TR	1Kx 8	3.0	Write Protection	–40 to 85	SO8TR
	ST25C08CM6	1K x 8	2.5	Write Protection	–40 to 85	SO8
	ST25C08CM6TR	1Kx 8	2.5	Write Protection	–40 to 85	SO8TR
16K	ST24C16CB1	2K x 8	3.0	Write Protection	0 to 70	PSDIP8
	ST24E16DB1	2K x 8	3.0	XI^2C Bus & WC	0 to 70	PSDIP8
	ST25C16CB1	2K x 8	2.5	Write Protection	0 to 70	PSDIP8
	ST25E16DB1	2K x 8	2.5	XI^2C Bus & WC	0 to 70	PSDIP8
	ST24C16CB6	2K x 8	3.0	Write Protection	–40 to 85	PSDIP8
	ST24E16DB6	2K x 8	3.0	XI^2C Bus & WC	–40 to 85	PSDIP8
	ST25C16CB6	2K x 8	2.5	Write Protection	–40 to 85	PSDIP8

EEPROM, I²C Serial Access Bus (cont'd)

Size	Part Number	Organis.	Vcc min (V)	Feature	Temp. Range (°C)	Package
16K	ST25E16DB6	2K x 8	2.5	XI²C Bus & WC	–40 to 85	PSDIP8
	ST24C16CB3	2K x 8	3.0	Write Protection	–40 to 125	PSDIP8
	ST24C16CM1	2K x 8	3.0	Write Protection	0 to 70	SO8
	ST24C16CM1TR	2K x 8	3.0	Write Protection	0 to 70	SO8TR
	ST24C16DM1	2K x 8	3.0	Write Protection	0 to 70	SO8
	ST24C16DM1TR	2K x 8	3.0	Write Protection	0 to 70	SO8TR
	ST24E16DM1	2K x 8	3.0	XI²C Bus & WC	0 to 70	SO8
	ST24E16DM1TR	2K x 8	3.0	XI²C Bus & WC	0 to 70	SO8TR
	ST25C16DM1	2K x 8	2.5	Write Protection	0 to 70	SO8
	ST25C16DM1TR	2K x 8	2.5	Write Protection	0 to 70	SO8TR
	ST25E16DM1	2K x 8	2.5	XI²C Bus & WC	0 to 70	SO8
	ST25E16DM1TR	2K x 8	2.5	XI²C Bus & WC	0 to 70	SO8TR
	ST24C16DM6	2K x 8	3.0	Write Protection	–40 to 85	SO8
	ST24C16DM6TR	2K x 8	3.0	Write Protection	–40 to 85	SO8TR
	ST24E16DM6	2K x 8	3.0	XI²C Bus & WC	–40 to 85	SO8
	ST24E16DM6TR	2K x 8	3.0	XI²C Bus & WC	–40 to 85	SO8TR
	ST25C16DM6	2K x 8	2.5	Write Protection	–40 to 85	SO8
	ST25C16DM6TR	2K x 8	2.5	Write Protection	–40 to 85	SO8TR
	ST25E16DM6	2K x 8	2.5	XI²C Bus & WC	–40 to 85	SO8
	ST25E16DM6TR	2K x 8	2.5	XI²C Bus & WC	–40 to 85	SO8TR
	ST24C16CML1	2K x 8	3.0	Write Protection	0 to 70	SO14
	ST24C16CML1TR	2K x 8	3.0	Write Protection	0 to 70	SO14TR
	ST25C16CML1	2K x 8	2.5	Write Protection	0 to 70	SO14

Size	Part Number	Organis.	Vcc min (V)	Feature	Temp. Range (°C)	Package
16K	ST25C16CML1TR	2K x 8	2.5	Write Protection	0 to 70	SO14TR
	ST24C16CML6	2K x 8	3.0	Write Protection	–40 to 85	SO14
	ST24C16CML6TR	2K x 8	3.0	Write Protection	–40 to 85	SO14TR
	ST25C16CML6	2K x 8	2.5	Write Protection	–40 to 85	SO14
	ST25C16CML6TR	2K x 8	2.5	Write Protection	–40 to 85	SO14TR

TRANSIL

P_P (W)	V_{RM} (V)	Type		Case	Page
		Unidirectional	Bidirectional		
400/1 ms	5.8 to 376	BZW04../BZW04P..	BZW04..B/BZW04P..B	F126	555
400/1 ms	5.8 to 188	SM4TxxA	SM4TxxCA	SOD6	591
600/1 ms	5.8 to 376	P6KE.. P,A	P6KE.. CP, CA	CB-417	583
600/1 ms	5.8 to 188	SM6TxxA	SM6TxxCA	SOD6	597
1500/1 ms	5.8 to 376	1.5KE... P, A	1.5KE...CP, CA	CB-429	547
1550/1 ms	5.8 to 188	SM15TxxA	SM15TxxCA	SOD15	603
5000/1 ms	10 to 180	BZW50...	BZW50...B	AG	563

TRISIL

I_{PP} (A)	V_{BR} (V)	Types	Case	Page
SINGLE FUNCTION				
50/10/1000	58 to 270	TPA Series	F126	629
	58 to 270	SMTPA Series	SOD6	609
90/10/1000	58 to 270	TPB Series	CB429	635
	58 to 270	SMTPB Series	SOD15	615
100/10/1000	18 to 120	LS5018B, 5060B, 5120B	DIL8	577
TRIPLE FUNCTION				
30/10/1000	150 to 270	THBTxxx11 Series	SO8	621
	150 to 270	THBTxxx12 Series	DIL8	621
	80 to 120	TPIxx11 Series	SO8	641
	80 to 120	TPIxx12 Series	DIL8	641

GATE TRIGGERED PROTECTIONS

I_{PP} (A)	V_{BR} (V)	Types	Case	Page
30/10/1000	250	TPP25011	SO8	649
	250	TPP25012	DIL8	649
100/10/1000	250	L3100B, B1	DIL8	569

TELEPHONE SET INTERFACE: DIODE BRIDGE + PROTECTION

I_{PP} (A)	V_{BR} (V)	Types	Case	Page
30/10/1000	150 to 270	TSIxxxB5 Series	SO16	657

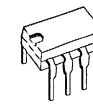
DEDICATED ICs

SGS-THOMSON MICROELECTRONICS

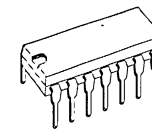
EFG7189
EFG71891

DTMF GENERATOR FOR BINARY CODED HEXADECIMAL DATA

- GENERATES 16 STANDARD DTMF TONE PAIRS
- USES LOW COST 3.579 MHz CRYSTAL
- DIRECT MICROPROCESSOR INTERFACE
- ACCEPTS 4 BIT DATA IN SERIAL OR PARALLEL FORMAT
- DATA IS STORED DURING TRANSMISSION PERIOD
- LOW HARMONIC DISTORTION
- HIGH GROUP PRE EMPHASIS
- LOW POWER CONSUMPTION IN STANDBY MODE
- PULL-UP TO V^+ ON ALL LOGIC INPUTS



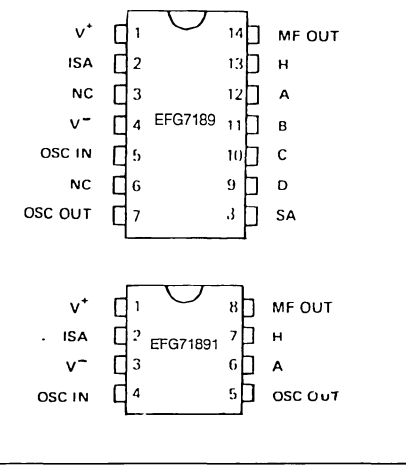
Minidip



DIP14

ORDERING NUMBERS : EFG71891PD (Minidip)
EFG7189PD (DIP14)

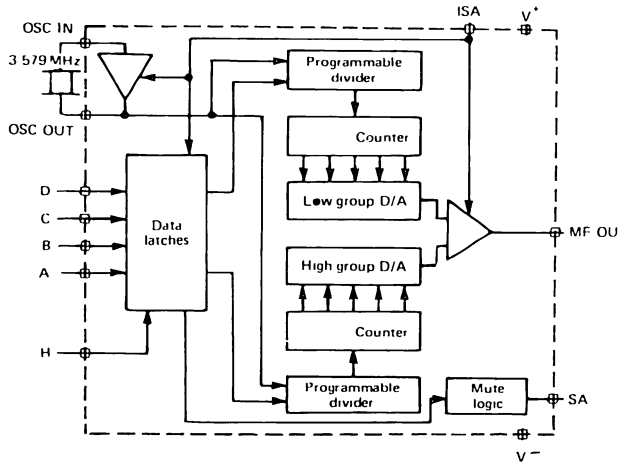
PIN CONNECTIONS (Top view)



DESCRIPTION

This CMOS circuit is designed specifically to provide, with a minimum number of external components, a low cost DTMF dialer for microprocessor controlled telephone sets operating in accordance with existing standards. The 4 bits identifying the frequency pair to be generated may be supplied via either 5 connections between the EFG7189 and the microprocessor in parallel format or in serial format through 3 connections linking the EFG7189 to the microprocessor. This feature eliminates the necessity to simulate keyboard type inputs normally required by standard DTMF generators. Input data is stored on trailing edge of ISA signal. The tone pair selected by this code is generated while ISA remains low. With ISA high, the oscillator is inhibited and the device is in standby mode. SA pin is connected to V^- while device is outputting any tone pair.

BLOCK DIAGRAM



PIN DESCRIPTION

N°	Name	Function	Description
1 4	V^+ V^-	Supply Voltage Supply Voltage	Positive Supply 0V
11 10 9	B C D	Logic Input Logic Input Logic Input	Parallel input for hexadecimal code allowing the selection of 2 frequencies constituting the DTMF signal (see attached table).
12	A	Logic Input	Serial or Parallel Input for Hexadecimal Code
13	H	Serial Input Clock	Clock Input for Hexadecimal Code Serial Input Register on Pin A Furthermore, it allows for the selection of the serial or parallel operating mode of this code. When ISA input goes low, the validated code is : • the parallel input code if input H is high. • the serial input code if input H is low.
2	ISA	Logic Input	This pin allows for the inhibition of the analog output MF OUT : • when ISA is high, output MF OUT is idle and connected to V^-. • when ISA is low, the hexadecimal code is validated and MF OUT output is activated.
8	SA	Logic Output	This pin indicates the state of the analog output : • if ISA is low, SA is a low impedance output at V^-. • if ISA is high, SA is a high impedance output.
14	MF OUT	Analog Output	This pin is the DTMF signal output.
5	OSC IN	Oscillator Input	This pin corresponds to the input of the inverter of the oscillator. The nominal frequency of the oscillator is 3.579 MHz.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V^+	Supply Voltage	– 0.3 to + 5.5	V
V_{in}	Digital Input Range	– 0.3 to V^+ + 0.3	V
T_{stg}	Storage Temperature Range	– 55 to + 125	°C

ELECTRICAL OPERATING CHARACTERISTICS
All voltages referenced to V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Supply Voltage	3	–	5.25	V
T_{oper}	Operating Temperature Range	– 25	–	70	°C
f_c	Crystal Frequency	–	3.579545	–	MHz

DC ELECTRICAL CHARACTERISTICS
T_{amb} = – 25 °C to 70 °C, V^+ = – 3 to 5.25 V, f_c = 3.579 MHz (all voltages are referenced to V^-)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{DD}	Operating Current in Transmission Mode (V^+ = 4 V, output not loaded)	–	0.6	1	mA
ISB	Standby Current (ISA, H, A, B, C, D open circuit or connected to V^+)	–	–	10	µA
V_{IL}	Input Low Voltage (ISA, H, A, B, C, D)	0	–	0.3 V^+	V
V_{IH}	Input High Voltage (ISA, H, A, B, C, D)	0.7 V^+	–	V^+	V
R_T	Pull up Resistor on Logic Inputs ISA, H, A, B, C, D	100	–	–	kΩ
I_{OLSA}	SA Output Current (V_{OLSA} = 0.5 V)	500	–	–	µA
I_{FSA}	SA Leakage Current, Open Current (V_{OHSA} = 5 V)	–	–	2	µA

A.C. ELECTRICAL CHARACTERISTICS
T_{amb} = – 25 °C to 70 °C, V^+ – 3 V to 5.25 V, f_c = 3.579 MHz

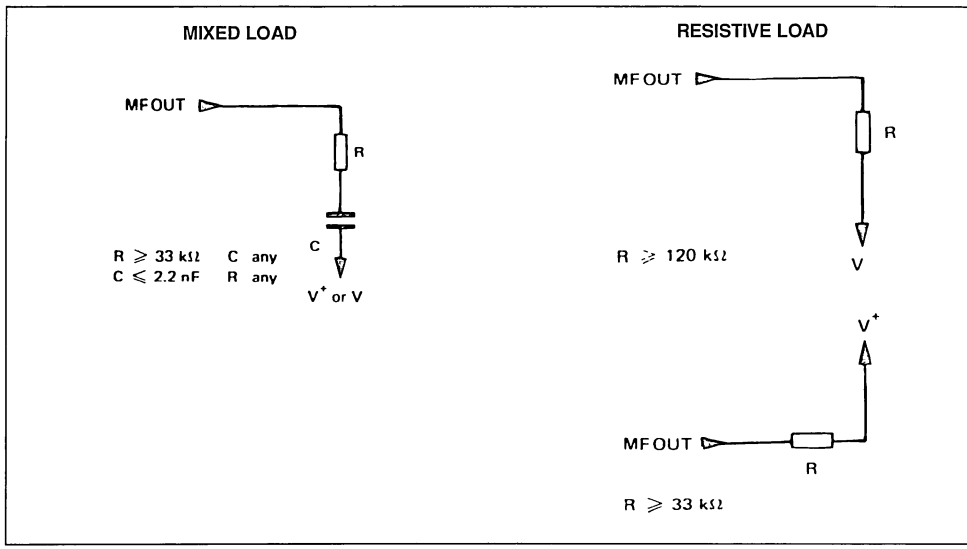
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_r t_f	Rise/Fall Time on Input Signals	–	–	50	ns
$TISA_{ON}$	Transmission Delay	–	–	5	ms
$TISA_{OFF}$	Blocking Delay	–	–	5	ms
T_H	Clock Period	10	–	–	µs
T_{HH}	High Level Clock Width	5	–	–	µs
T_{HL}	Low Level Clock Width	5	–	–	µs
T_{PH}	Set-up Time of A Related to Clock	1	–	–	µs
T_{MH}	Hold Time of A Related to Clock	7	–	–	µs
T_{PISA}	Set-up Time of the Code or Clock Related to ISA	1	–	–	µs
T_{MISA}	Hold Time of Code Related to ISA	2	–	–	µs

TRANSMISSION CHARACTERISTICS T_{amb} = – 25 °C to 70 °C, V^+ 3 V to 5.25 V, f_c = 3.579

Symbol	Parameter	Min.	Typ.	Max.	Unit
DFH DFB	High and Low Frequency Precision	–	–	1	%
AFB	Low Frequency Transmission Level (V^+ = 4 V) - Note 1	– 8	– 7	– 6	dBm
GBH	High Band Pre-emphasis	2.3	2.7	3.5	dB
D	Output Distortion	–	–	– 20	dB

Note : 1. 0 dBm = 0.775 V_{rms}
These specifications are related to the following loads.

Figure 1.



FUNCTIONAL DESCRIPTION

With ISA input at logic level "1", the device is in low power mode. The oscillator is inhibited and analog output MF OUT is at ground level. DTMF input data is detected on trailing edge of ISA. This transition enables both the oscillator and the analog output then the data is stored and corresponding DTMF pair is generated during the low state interval of the ISA signal. Any modification to H, A, B, C and D signals during this period will not have any further effect on DTMF pair generated.

The device accepts input data in two different formats :

- Parallel format : this requires 4 connections (A, B, C, D) between the microprocessor and the circuit.
- Serial format : in this case data is supplied to the circuit by the microprocessor via 2 connections A and H (see typical application diagram).

Pre-emphasis is applied to high group tone and both tones of DTMF pair are supplied through analog output pin.

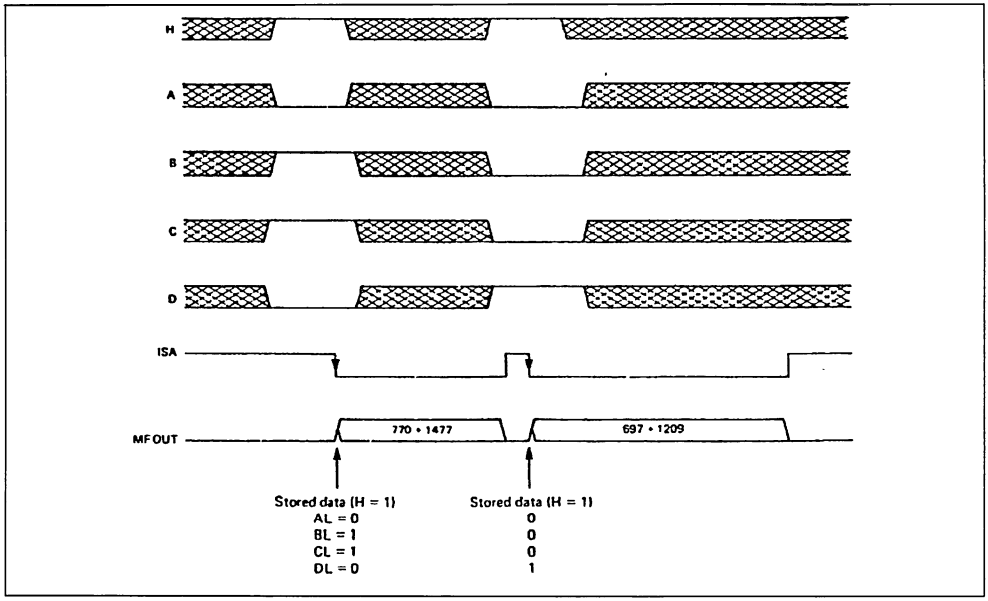
DATA ACQUISITION LOGIC

This section includes : A 4-bit shift register, an 8-line to 4-line multiplexer and a 4-bit storage register.

- The 4-bit shift register has its input connected to pin A and is enabled by the signal applied to pin H. Its outputs are AS, BS, CS and DS signals.
- The multiplexer is enabled by signal H and operates according to the following law : $AI = H.AP + \overline{H}.AS$.
- The 4-bit storage register operates on trailing edge of ISA signal. AI, BI, CI, DI and AL, BL, CL, DL are its inputs and outputs respectively.

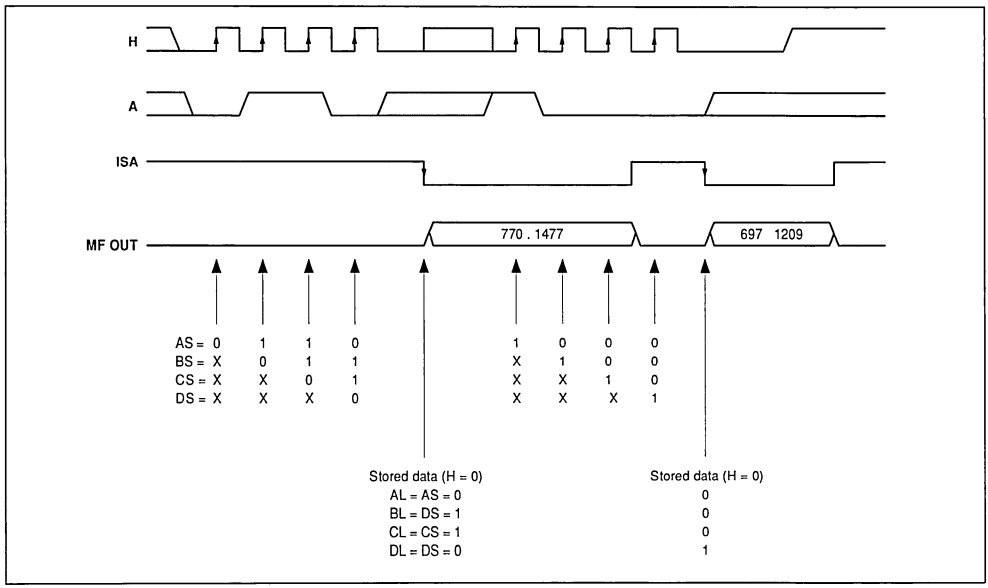
During the low state period of ISA input, AL, BL, CL and DL signals determine the DTMF pair to be generated.

Figure 2 : Example of Parallel Operating Mode.



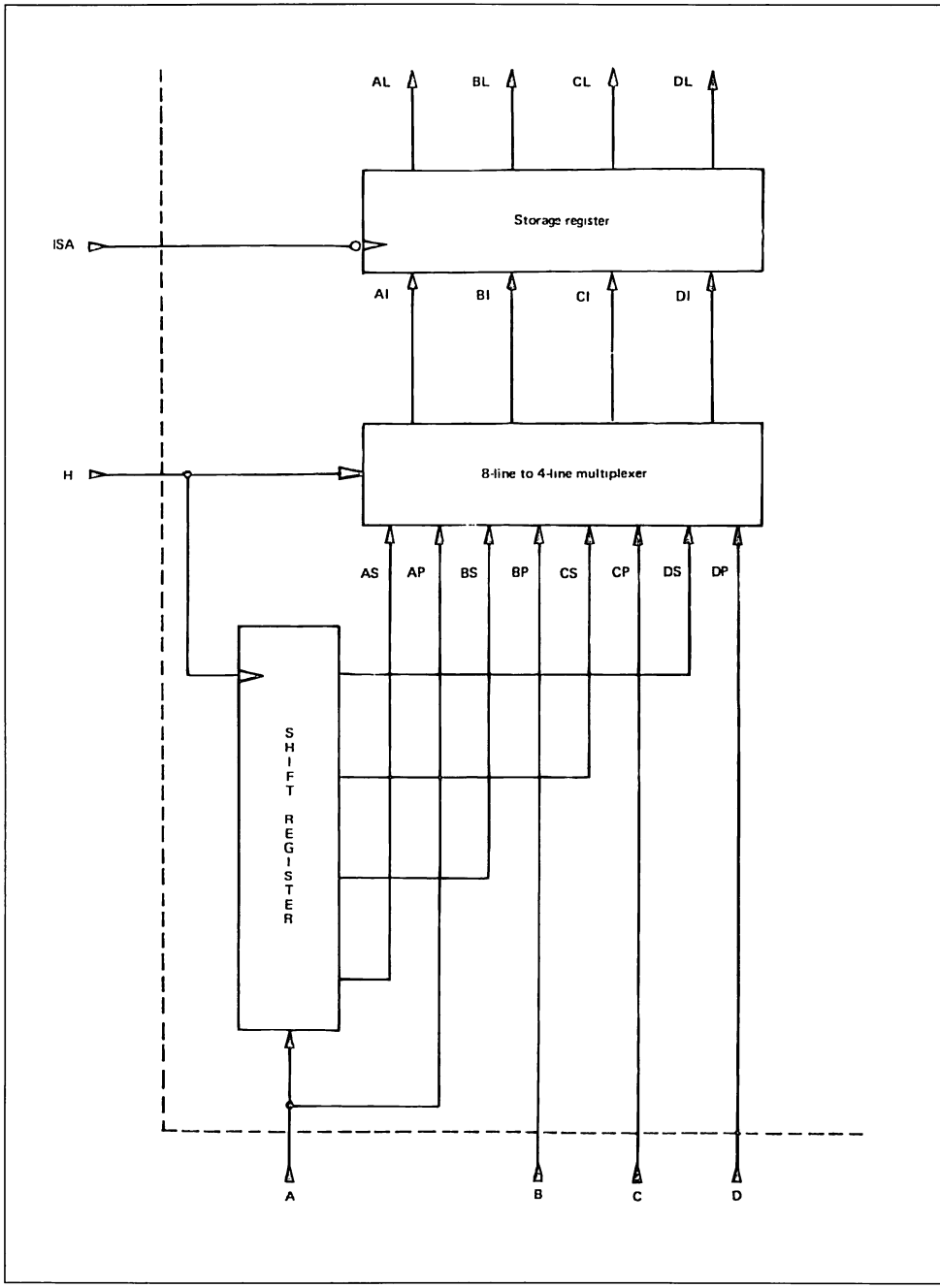
Note : If the circuit operates permanently in parallel mode, then the H input may be left floating (internally pulled-up to V+) or tied to logic 1. With ISA at logic 0, H,A,B,C, and D inputs cannot modify the generated DTMF pair.

Figure 3 : Example of Serial-Operating Mode.



Notes : 1. With ISA at logic 0, H, A, B, C and D signals cannot modify the generated DTMF pair. As a result, in serial operating mode, it is possible to enter AS, BS, CS and DS data while another DTMF pair is being generated.
2. First data to be entered is DS.

Figure 4 : Data Acquisition Logic.



TIMING DIAGRAM

Figure 5 : Rise/Fall Time on Input Signals.

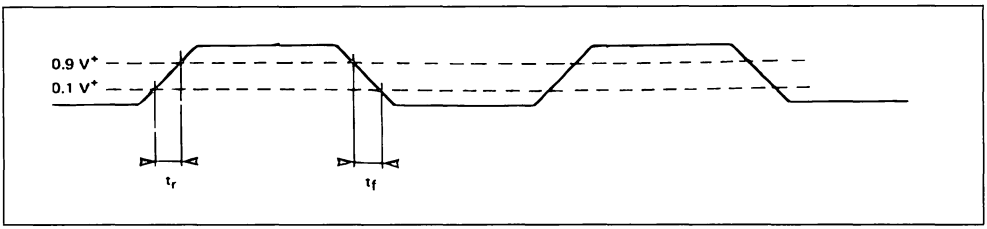


Figure 6 : Parallel Operating Mode (H = "1").

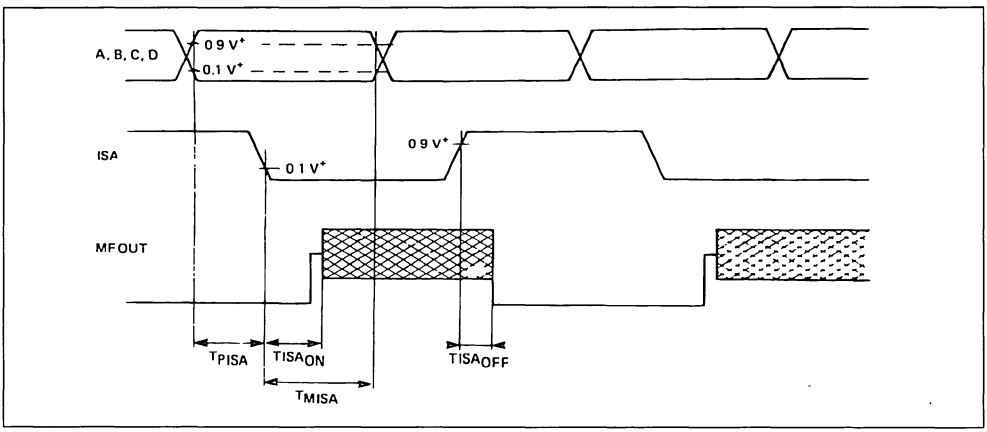


Figure 7 : Serial Operating Mode.

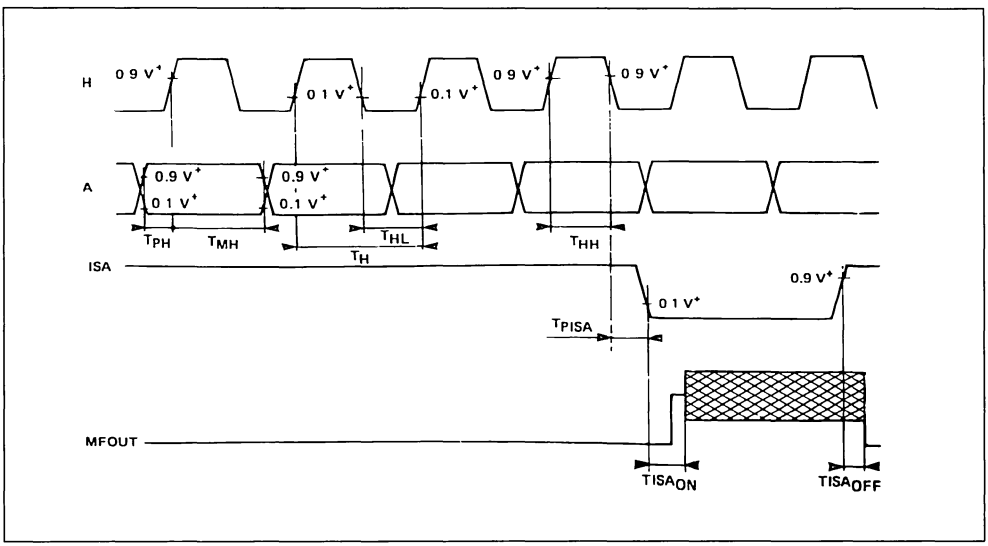


Table 1

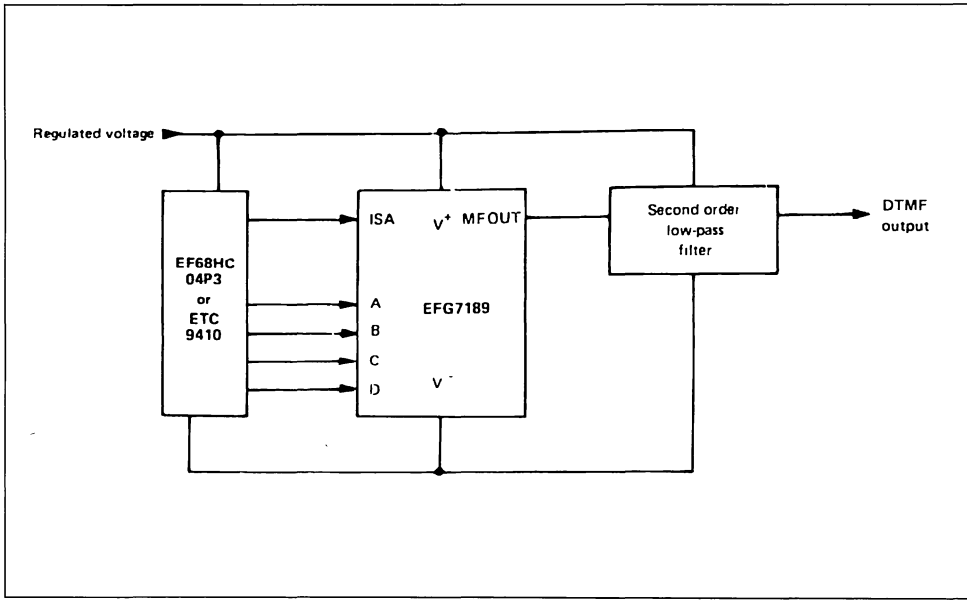
	DTMF Specification (Hz)	Frequencies Derived from a 3.579 MHz Quartz (Hz)	Division Rank	% Deviation from Standard
f1	697	701.3	5104	0.62
f2	770	771.4	4640	0.19
f3	852	857.2	4176	0.61
f4	941	935.1	3828	– 0.63
f5	1209	1215.9	2944	0.57
f6	1336	1331.7	2688	– 0.32
f7	1477	1471.9	2432	– 0.35
f8	1633	1645	2176	0.74

Table 2

Keyboard Code	Hexadecimal Code				ISA	Generated Frequencies	
	A	B	C	D		f(Hz)	f(Hz)
X	X	X	X	X	1		
1	0	0	0	1	↓	697	1209
2	0	0	1	0	↓	697	1336
3	0	0	1	1	↓	697	1477
4	0	1	0	0	↓	770	1209
5	0	1	0	1	↓	770	1336
6	0	1	1	0	↓	770	1477
7	0	1	1	1	↓	852	1209
8	1	0	0	0	↓	852	1336
9	1	0	0	1	↓	852	1477
0	1	0	1	0	↓	941	1336
•	1	0	1	1	↓	941	1209
≠	1	1	0	0	↓	941	1477
A	1	1	0	1	↓	697	1633
B	1	1	1	0	↓	770	1633
C	1	1	1	1	↓	852	1633
D	0	0	0	0	↓	941	1633

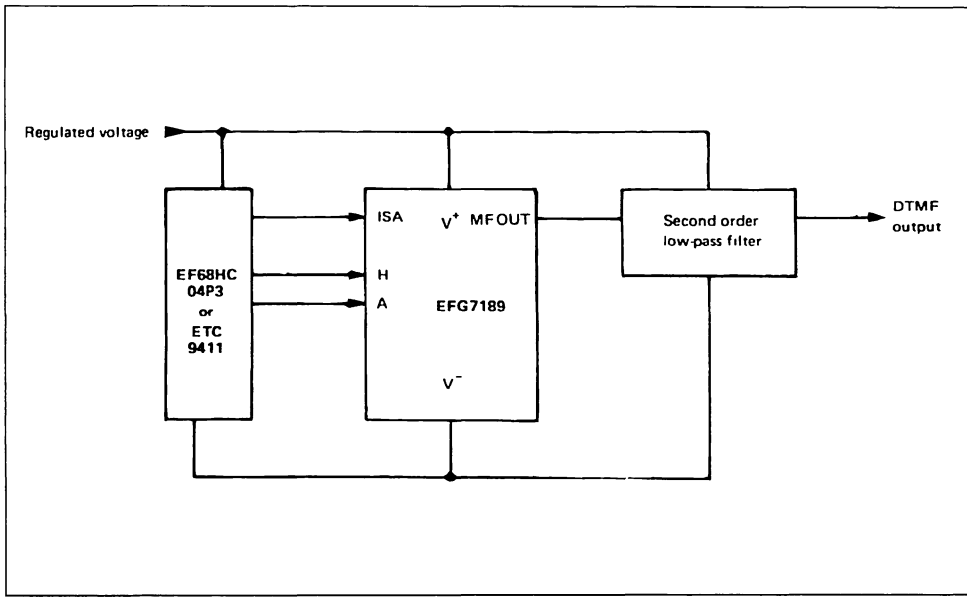
TYPICAL APPLICATION (european standards)

Figure 8 : Parallel Connection.



Note : H may be left open or connected to logic 1.

Figure 9 : Serial Connection.



Note : B, C and D may be left floating or connected to logic 1.

SECOND ORDER LOW-PASS FILTERS

Figure 10 : With Transistor (gain = 1).

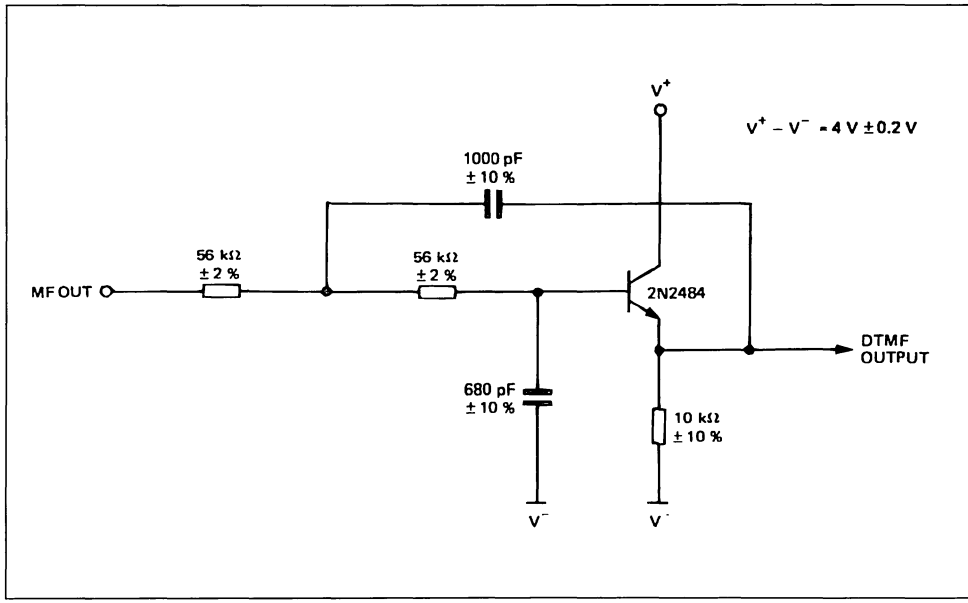
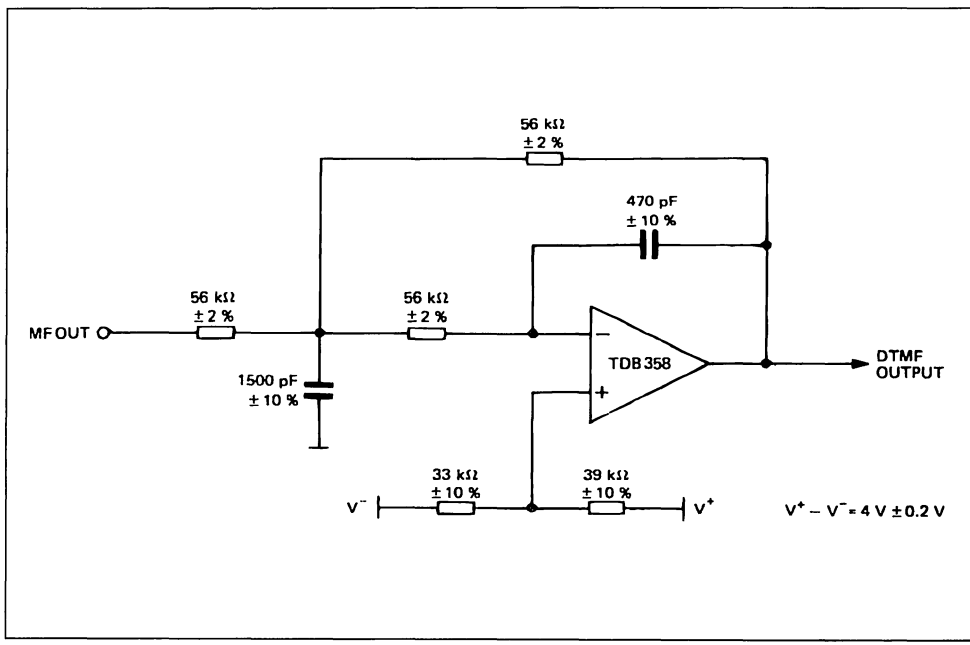
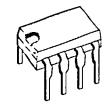


Figure 11 : With Op. Amp. (gain = 1).

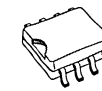


ELETRONIC TWO-TONE RINGER

- LOW CURRENT CONSUMPTION, IN ORDER TO ALLOW THE PARALLEL OPERATION OF 4 DEVICES
- INTEGRATED RECTIFIER BRIDGE WITH ZENER DIODES TO PROTECT AGAINST OVERVOLTAGES
- LITTLE EXTERNAL CIRCUITRY
- TONE AND SWITCHING FREQUENCIES ADJUSTABLE BY EXTERNAL COMPONENTS
- INTEGRATED VOLTAGE AND CURRENT HYSTERESIS
- COMPLEMENTARY OUTPUT CONFIGURATION



Minidip



SO8

ORDERING NUMBERS : L3240B1 (Minidip)
L3240D1 (SO8)

DESCRIPTION

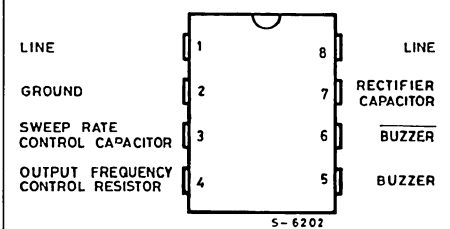
L3240 is a monolithic integrated circuit designed to replace the mechanical bell in telephone sets, in connection with an electro acoustical converter. The device can drive either directly a piezo ceramic converter (buzzer) or a small loudspeaker. In this case a transformer is needed. The two tone frequencies generated are switched by an internal oscillator in a fast sequence and made audible across output amplifiers in the transducer ; both tone frequencies and the switching frequency can be externally adjusted.

The supply voltage is obtained from the AC ring signal and the circuit is designed so that noise on the line or variations of the ringing signal cannot affect the correct operation of the devices.

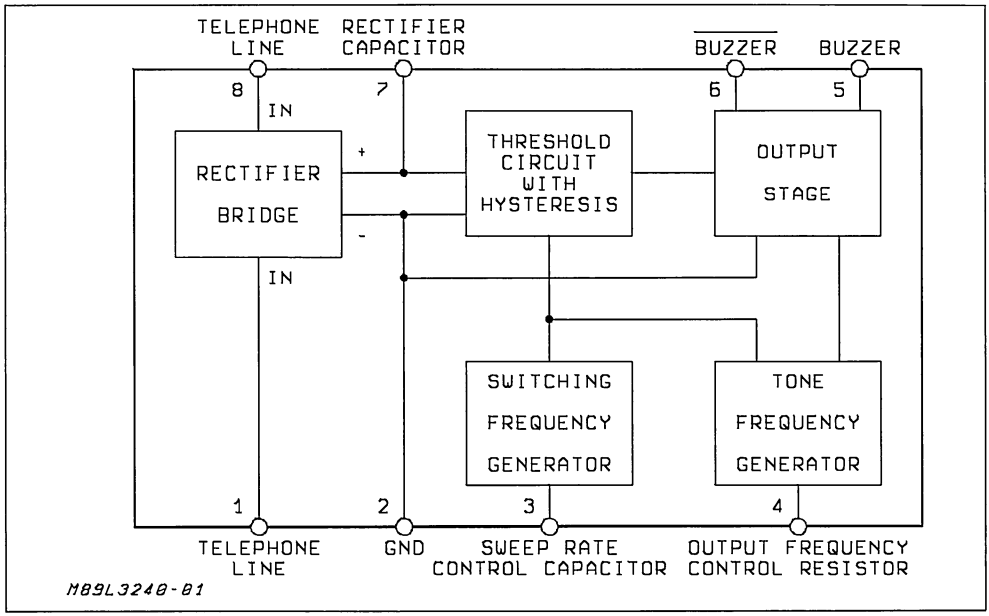
The output bridge configuration allows to use a high impedance transducer with acoustical results much better than in a single ended configuration.

The two outputs can also be connected independently to different converters or actuators (acoustical, opto, logic).

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{AB}	Calling Voltage (f = 50 Hz) Continuous	120	V_{RMS}
V_{AB}	Calling Voltage (f = 50 Hz) 5s N/10s OFF	200	V_{RMS}
DC	Supply Current	30	mA
T_{op}	Operating Temperature	– 20, + 70	°C
T_{stg}	Storage and Junction Temperature	– 65, + 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	100	°C/W

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C ; V_S = applied between pins 7-2 ;otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage				26	V
I_B	Current Consumption Without Load (Pins 8-1)	$V_{8\text{-}1}$ = 16.5 to 29.5 V		1.5	1.8	mA
V_{ON}	Activation Voltage		12		13.5	V
V_{OFF}	Sustaining Voltage		7.8		9.3	V
R_D	Differential Resistance in OFF Condition (Pins 8-1)		6.4			kΩ
V_{OUT}	Output Voltage Swing			V_S – 5		V
I_{OUT}	Short Circuit Current (pins 5-6)	V_S = 20 V		35		mA
V_S	Voltage Drop between Pins 8-1 and Pins 7-2			3		V

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C ; V_S = applied between pins 7-2 ;otherwise specified)

AC OPERATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Output Frequencies Fout 1 Fout 2	V_s = 26 V, R_1 = 14 KΩ V_s = 0 V V_s = 6 V	 2,29 1.6		 2,8 2.1	kHz
	$\frac{\text{Fout 1}}{\text{Fout 2}}$		1.33		1.43	
	Programming Resistor Range		8		56	kΩ
	Sweep Frequency	R_1 = 14kΩ, C1 =100nF	5.25	7,5	9.75	Hz

Figure 1 : Test Circuit.

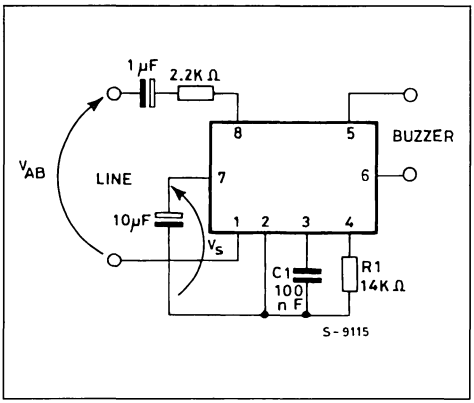


Figure 2 : Typical Application with Balanced Output.

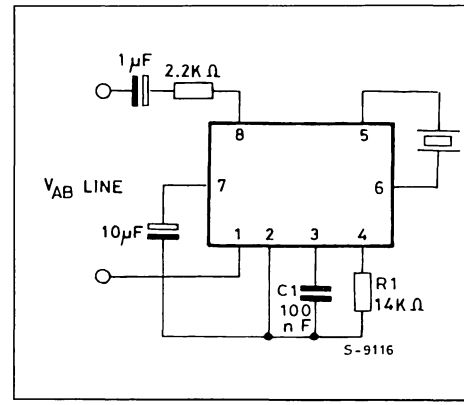


Figure 3 : Application Compatible with LS1240 (single ended output).

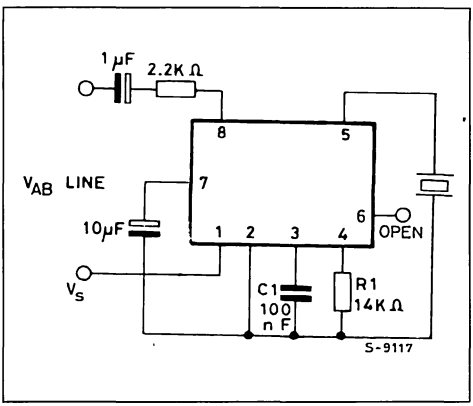
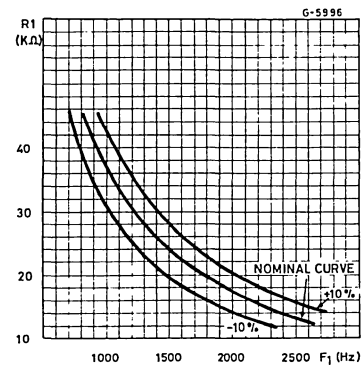


Figure 4 : F_1 Out vs. R_1.



$$R_1 \approx \frac{3.56 \times 10^4}{F_1\,(HZ)} \times \left(1 - 0.12 \times \ln \frac{F_1}{2543}\right)$$

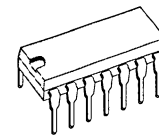
$$f_2 = 0.725\, f_1$$

$$f_{SWEEP} = \frac{750}{C1\,(nF)}$$

LOW VOLTAGE TELEPHONE SPEECH CIRCUIT

ADVANCE DATA

- OPERATION DOWN TO 1.3 V/5 mA
- DTMF & BEEP TONE INPUTS
- EXTERNAL MUTING FOR EARPHONE AND MICROPHONE
- MUTE TURNS ON BEEP TONE & DTMF INPUTS AND TURNS OFF EARPHONE & MICROPHONE
- SUITABLE FOR DYNAMIC OR PIEZO EARPHONES AND PIEZO, DYNAMIC OR ELECTRET MICROPHONES



DIP14 (0.25)

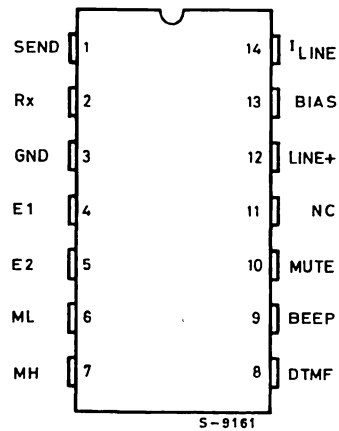
ORDERING NUMBER : L3280AB

DESCRIPTION

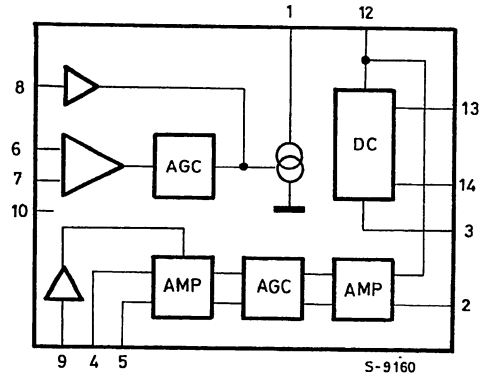
The L3280 is a brand new low voltage speech circuit designed to replace hybrid circuits in telephone sets. It is designed for sets that may be operated in parallel. It features both DTMF input and Beep tone input ; ALC on send and receive and muting input.

Various DC - characteristics can be programmed at pin 14 replacing testing resistor (43Ω) with proper network value.

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_L	Line Voltage (3 ms pulse)	20	V
I_L	Line Current	150	mA
P_{tot}	Total Power Dissipation, T_{amb} = 70 °C	1	W
T_{op}	Operating Temperature	– 20 to 55	°C
T_j	Junction Temperature	– 65 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

Figure 1 : Test Circuits.

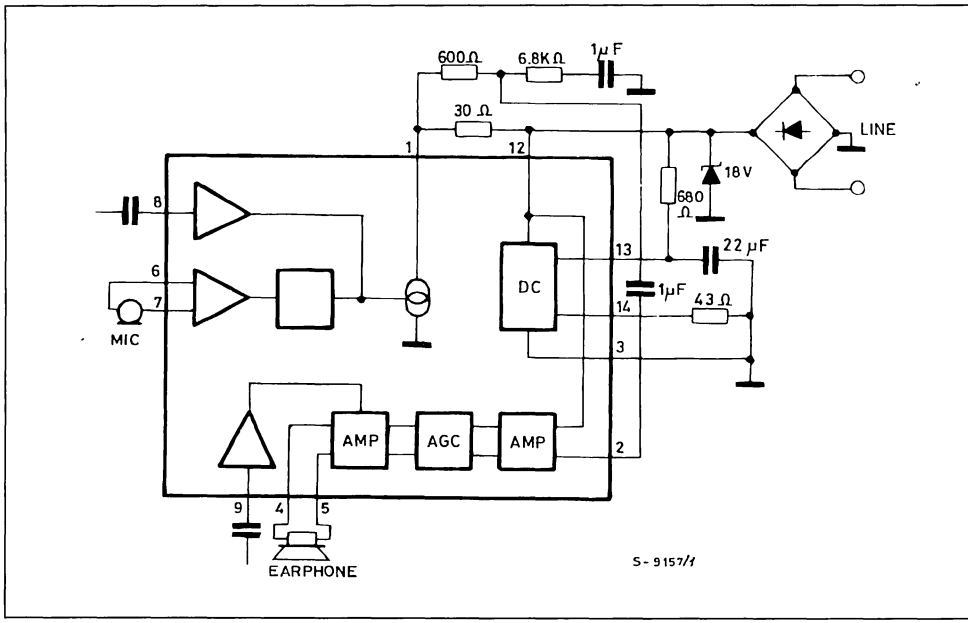
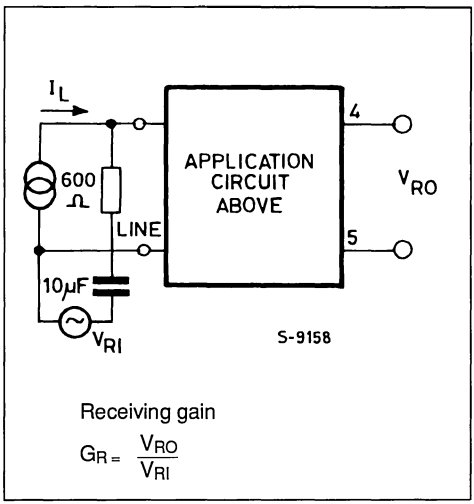


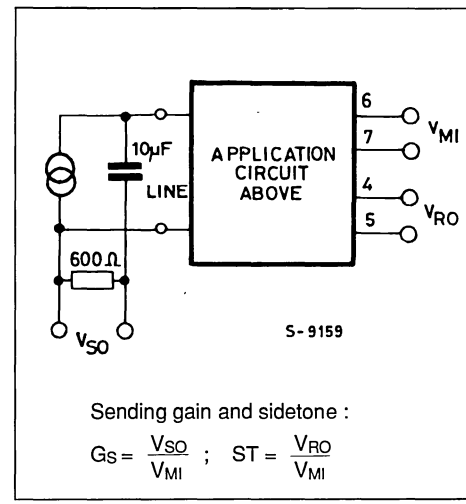
Figure 2 .



Receiving gain

$$G_R = \frac{V_{RO}}{V_{RI}}$$

Figure 3.



Sending gain and sidetone :

$$G_S = \frac{V_{SO}}{V_{MI}} \quad ; \quad ST = \frac{V_{RO}}{V_{MI}}$$

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C ; f = 1kHz ; I_L = 20mA : mute low ; R1 (pin 14) = 43Ω, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_L	Line Voltage	I_L = 20 mA		3.05	3.35	V
V_L	Line Voltage	I_L = 50 mA		5.8	6.2	V
V_L	Line Voltage	I_L = 80 mA		8.5	10	V
C_{MRR}	Common Mode Rej. Ratio		50			dB
G_S	Sending Gain	V_{MI} = 2 mV, I_L = 20 mA	47.8	49.3	50.8	dB
D_{GS}	Delta Sending Gain	I_L = 70 mA, V_{MI} = 2 mV	– 7	– 5.5	– 4	dB
T_{HDS}	Sending Distortion	V_{SO} = 700 mV			5	%
N_{TX}	Sending Noise	I_L = 50 mA, V_{MI} = 0 V		– 71		dBm
Z_{MI}	Mic. Input Impedance	V_{MI} = 2 mV	40			KΩ
G_R	Receiving Gain	I_L = 20 mA, V_{RI} = 0.2 V	7.7	9.2	10.7	dB
D_{GR}	Delta Receiving Gain	I_L = 70 mA, V_{RI} = 0.2 V	– 7	– 5.5	– 4	dB
T_{HDR}	Receiving Distortion	V_{RO} = 615 mV			5	%
N_{RX}	Receiving Noise	V_{RI} = 0 V		300		μV
Z_{RO}	Receiving Output Imped.	R_1 = 200 Ω, V_{RO} = 50 mV		10		Ω
	Sidetone	V_{MI} = 2 mV		40		dB
Z_{ML}	Line Match. Impedance	V_{RI} = 0.2 V	500	600	700	Ω
V_L	Line Voltage	I_L = 5.5 mA		1.5	1.8	V
V_{SO}	Sending Output Voltage	I_L = 5.5 mA, T_{HD} = 5 %	100			mV
I_{RO}	Rec. Output Current	I_L = 5.5 mA, T_{HD} = 5 %	0.7			mA
	OPERATION @ I_L = 16 mA					
MULO	Mute Input Low	(speaking mode)			1	V
MUHI	Mute Input High	(dialling mode)	2			V
GMF	DTMF Gain	V_{in} = 2 mV ; Mute = 2 V	25	26.5	28	dB
RMF	DTMF Input Impedance	Mute = 2 V	6	8.5		KΩ
THDMF	DTMF Distorsion	Mute = 2 V ; V_{in} = 25 mV			5	%
G_{beep}	Beeptone Gain	Mute = 2 V ; V_{in} = 25 mV		8.5		dB
R_{beep}	Beeptone Input Imped.	Mute = 2 V	12			KΩ
THD	Beeptone Distorsion	Mute = 2 V ; V_{Bt} = 100 mV			5	%
DV_L	DELTA V_{LINE}	Mute = 2 V ; I_L = 20 mA	0.5		1.2	V
G_{BACK}	Back Tone Gain		–	–	–3.0	dB

CHARACTERISTIC AT 1 KHz

Figure 4 : Receive Characteristic and Max Output at 2 % THD.

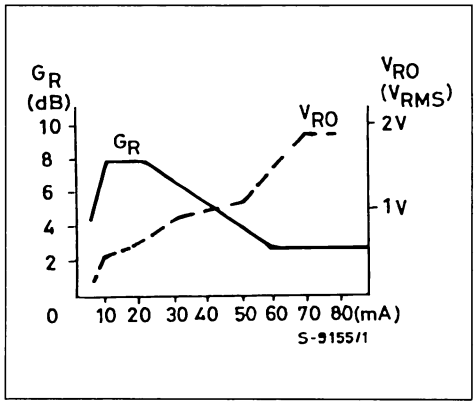


Figure 5 : Sending ALC Characteristic and Max Output at 2 % THD.

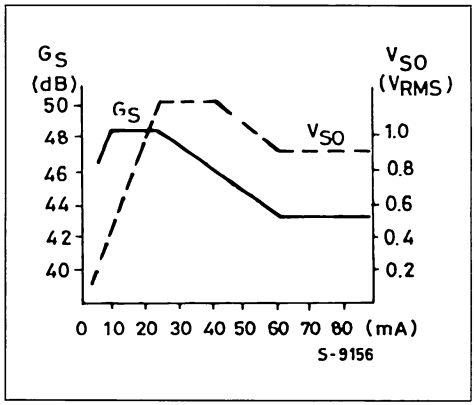
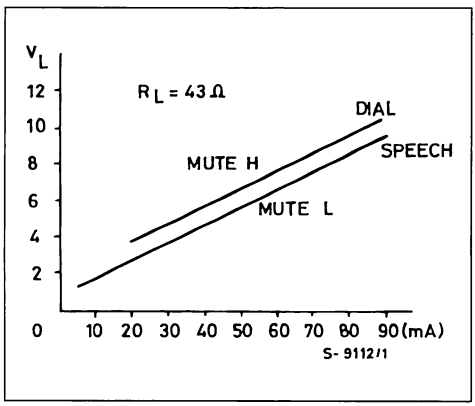


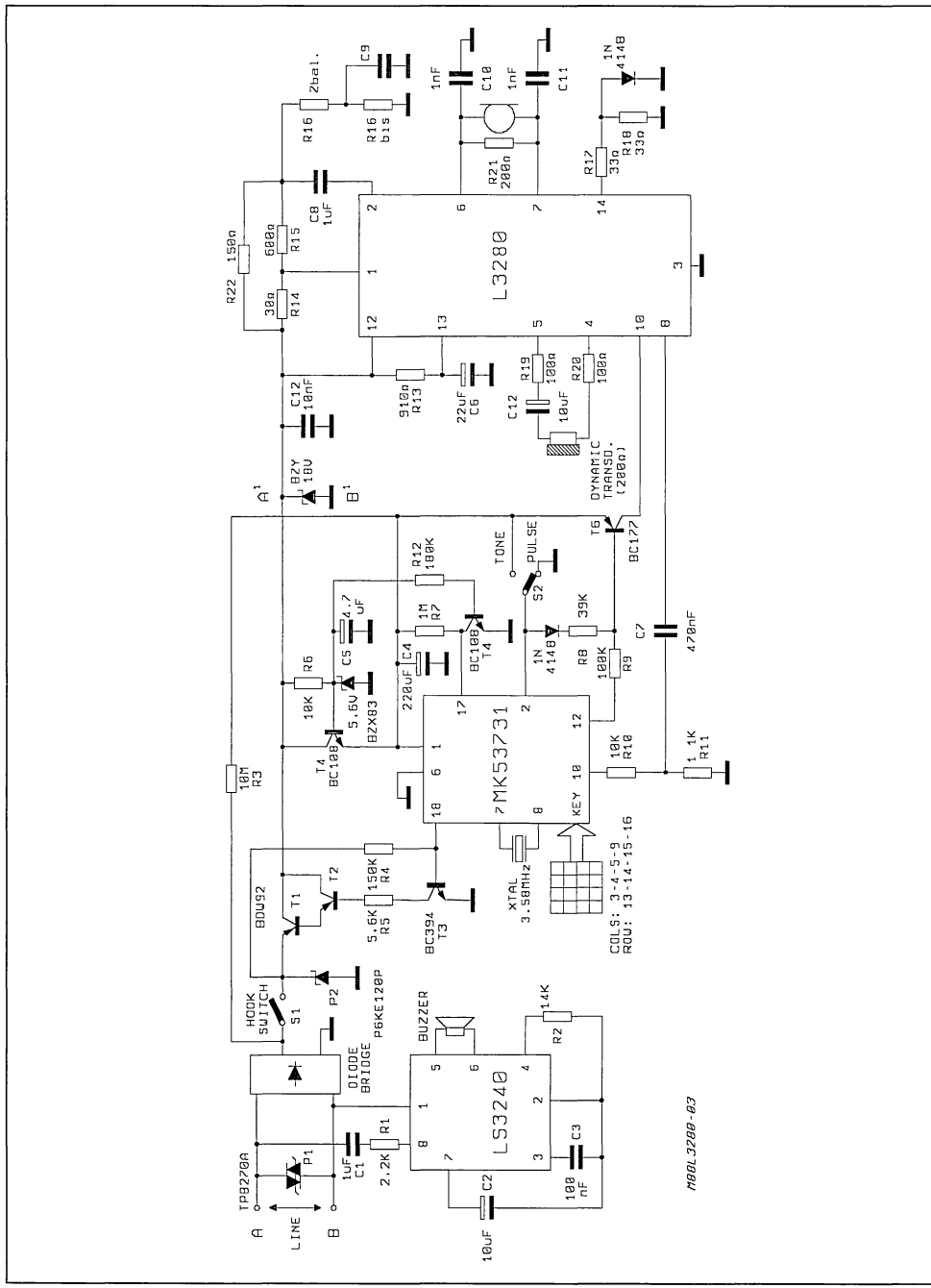
Figure 6 : DC Characteristic Measured between Line and GND.



LOGIC OF MUTE SWITCHING

	DTMF	BEEP	MIC INPUT	RECEIVE INPUT
MUTE H	ACTIVE TO LINE OUTPUT	ACTIVE TO EARPHONE OUTPUT	MUTED	MUTED
MUTE L	MUTED	MUTED	ACTIVE	ACTIVE

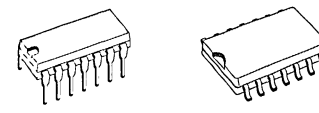
Figure 7 : Application Circuit for Dynamic Transducer.



LOW VOLTAGE TELEPHONE SPEECH CIRCUITS

PRELIMINARY DATA

- OPERATION DOWN TO 1.6V / 6.5mA
- DTMF & BEEP TONE INPUTS
- EXTERNAL MUTING FOR EARPHONE AND MICROPHONE
- SUITABLE FOR DYNAMIC EARPHONE AND DYNAMIC OR ELECTRET MICROPHONE
- AGC CONTROL ON BOTH SENDING AND RECEIVING



DIP14 SO14

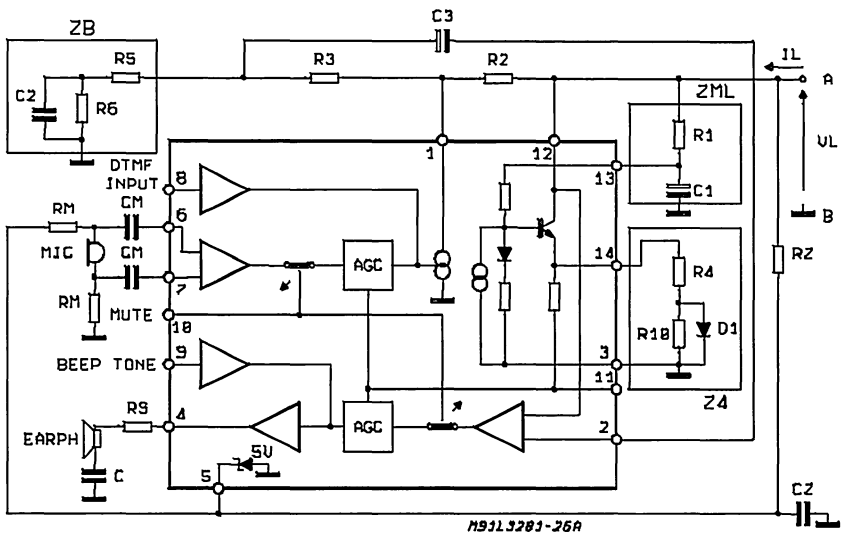
ORDERING NUMBERS:

L3281AB L3281AD1

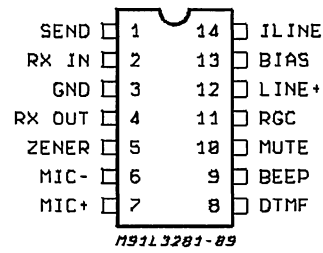
DESCRIPTION

The L3281 is an electronic speech circuit developed to replace hybrid circuits in telephone sets that can be operated in parallel with other phones.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		DIP-14	SO-14	
V_L	Line Voltage (3 ms pulse)	15		V
I_L	Line Current	150		mA
P_{tot}	Total Power Dissipation, T_{amb} = 55°C	1.0	0.6	W
T_{op}	Operating Temperature	– 20 to 55		°C
T_j	Junction Temperature	– 65 to 150		°C

THERMAL DATA

Symbol	Parameter	Value		Unit
		DIP-14	SO-14	
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient Max	90	130	°C/W

TEST CIRCUITS

Figure 1.

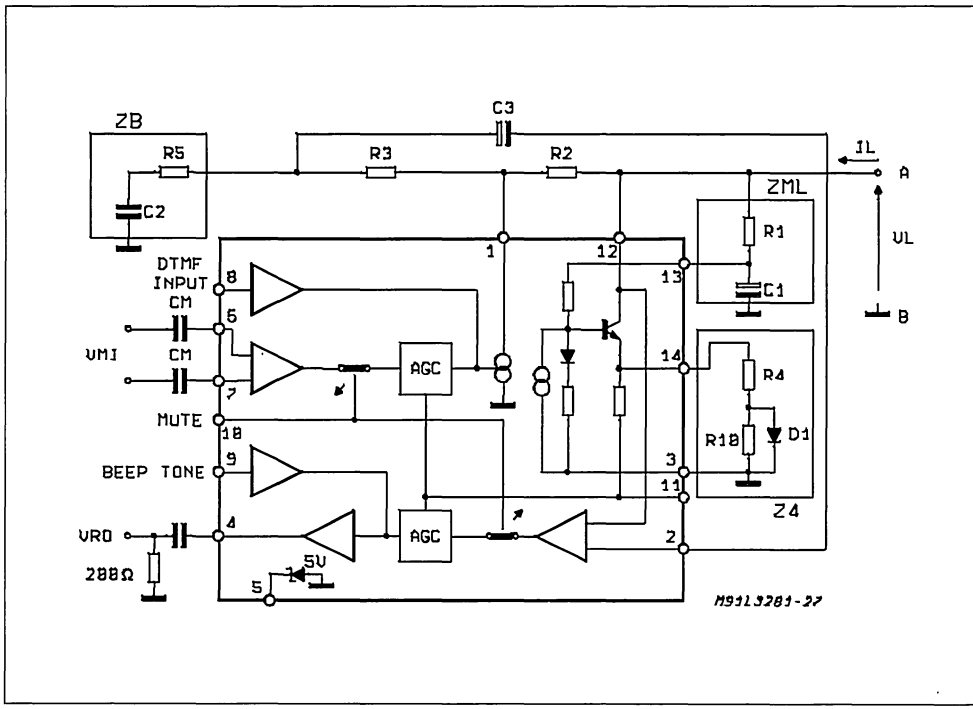


Figure 2.

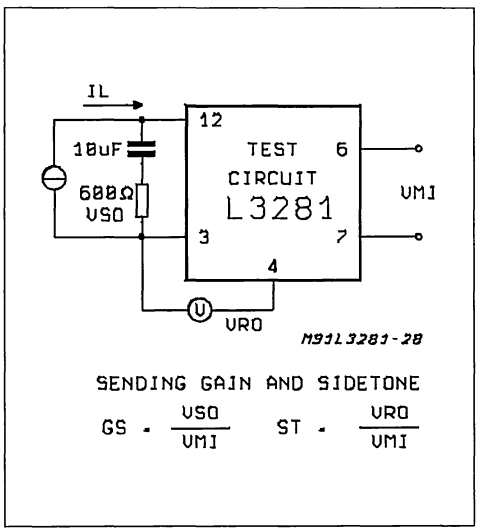
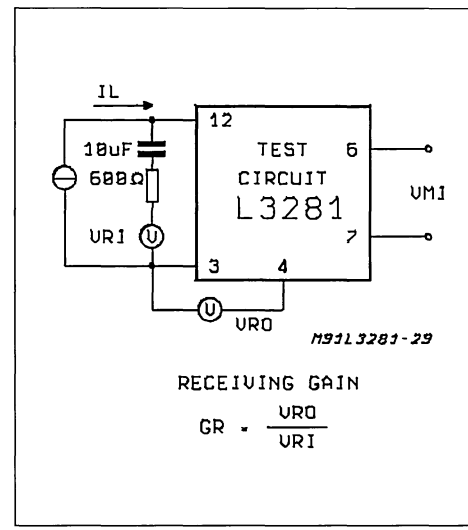


Figure 3.



ELECTRICAL CHARACTERISTICS I_L = 20 to 100mA; R4 =(51Ω // diode) + 33Ω;
T = 25°C; f = 1kHz; Unless Otherwise Specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_l	Line Voltage	I_L = 6.5mA I_L = 20mA I_L = 50mA I_L = 80mA		1.65 3.4 6.0 8	 3.7 6.5 9.5	V V V V
CMRR	Common Mode Rej. Ratio		50			dB
G_{tx}	Sending Gain	V_{ml} = 10mV; I_L = 20mA	30	31.5	33	dB
DG_{tx}	Delta Sending Gain	V_{ml} = 10mV; I_L = 70mA	– 7.2	–5.7	–4.2	dB
THD_{tx}	Sending Distortion	V_{so} = 700mV; I_L = 20mA			5	%
N_{tx}	Sending Noise	V_{ml} = 0V; I_L = 50mA		– 70		dB
Z_{ml}	Mic. Input Impedance	V_{ml} = 10mV	40			kΩ
G_{rx}	Receiving Gain	I_L = 20mA; V_{rl} = 0.2V	– 10.7	– 9.2	– 7.7	dB
DG_{rx}	Delta Receiving Gain	I_L = 70mA; V_{rl} = 0.2V	– 7.2	– 5.7	– 4.2	dB
THD_{rx}	Receiving Distortion	V_{ro} = 350mV; Load = 350Ω V_{ro} = 300mV; I_L = 10 mA			5 5	% %
N_{rx}	Receiving Noise	V_{rl} = 0V		100		µV
Z_{ro}	Rec. Output Impedance	Load = 200Ω; V_{ro} = 50V		10		Ω
	Sidetone	V_{ml} = 10mV		10	20	dB
Z_m	Line Match. Impedance	V_{rl} = 0.2V	500	600	700	Ω
V_{so}	Sending Output Voltage	I_L = 6.5mA; THD = 5%	100			mV
I_{ro}	Receiving Output Current	I_L = 6.5mA; THD = 5%	0.5			mAp
MU_{lo}	Mute Input Low	Dialing Mode		50	100	µA
MU_{hl}	Mute Input Open	Speaking Mode			1	µA
G_{mf}	DTMF Gain	$V_{mf\,IN}$ = 10mV	14.5	16	17.5	dB
R_{mf}	DTMF Input Impedance		5	10		kΩ
THD_{mf}	DTMF Distortion	$V_{mf\,LN}$ = 140mV			5	%
G_{beep}	Beeptone Gain	$V_{beep\,IN}$ = 25mV		8.5		dB
R_{beep}	Beeptone Input Impedance		5.5	8		kΩ
THD_{beep}	Beeptone Distortion	$V_{beep\,IN}$ = 100mV; I_L = 20mA		0.5	5	%
V_z	Zener Voltage (Pin 5)	I_z = 1 mA	4.2	5.1	6.2	V
I_{leak}	Leakage Current, V_{pin5} = 3V			20		µA

LOGIC OF MUTE SWITCHING

MUTE	DTMF	BEEP	MIC IMP	RX IMP
LOW (DIAL)	ACTIVE TO LINE OUTPUT	ACTIVE TO EARPHONE OUTPUT	MUTED	MUTED
OPEN (SPEECH)	ACTIVE TO LINE OUTPUT	ACTIVE TO EARPHONE OUTPUT	ACTIVE	ACTIVE

CIRCUIT DESCRIPTION

TWO TO FOUR WIRE CONVERSION

The L3281AB is based on a Wheastone bridge configuration. To balance the bridge the following relation must be satisfied:

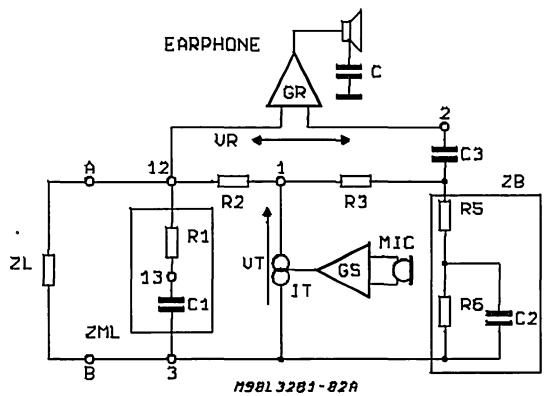
$$\frac{Zl \,//\, Zm}{Zb} = \frac{R2}{R3}$$

The AC signal from the microphone is sent to one diagonal of the bridge (pins 1 and 3). A small percentage of the signal power is lost on Zb (being Zb > (Zm//Zi)); the main part is sent to the line via R2.

In receiving mode, the AC signal coming from the LINE is sensed across the second diagonal of the bridge (pins 12 and 2).

The impedance Zm and Zb can be complex.

Figure 4: 2/4 Wire Conversion



DC CHARACTERISTIC

The fig.5 shows the equivalent simplified circuit of the DC regulator that provides to give the opportune DC impedance Zdc.

$$VL = \left[\frac{Idc \cdot Z4}{RB} \cdot (RA + RB)\right] + VD + VR1$$

$$VL = \left[(Idc \cdot Z4) \cdot \left(\frac{RA}{RB} + 1\right)\right] + VD + VR1$$

since RA = RB

$$VL = (Idc \cdot Z4 \cdot 2) + VD + VR1$$

When IL 18 mA and considering neglectible the VD + VR1 variation versus line current :

$$ZDC = \frac{\Delta VL}{\Delta Idc} = 2 \cdot Z4$$

At IL = 6.5 mA no current flows through Z4 but only in the rest of the circuit for internal biasing (Io;Ia). The bias current Io is fixed by the resistor R2. The line voltage in this case is :

$$VL = Ia\ RA + VR1 = 1.6\ V$$

The Fig.6 shows the DC characteristic (voltage between pin 12 and pin 3 versus line current). The device own an equivalent zener voltage at pin 5 that can be used as supply voltage for electret microphone (see Block Diagram).

The value of the resistor R2 and the capacitor C2 should be chosen in order to not affect the AC line inpedance. The Fig.7 shows the zener equivalent.

The zener voltage will be:

$$Vz = \left(\frac{70K}{13.6K} + 1\right) \cdot Vbe$$

It is possible to supply 1mA to the electrete voltage if VL > (1mA + Iz) · Rz + Vz

Figure 6: Low Voltage Speech Circuit.

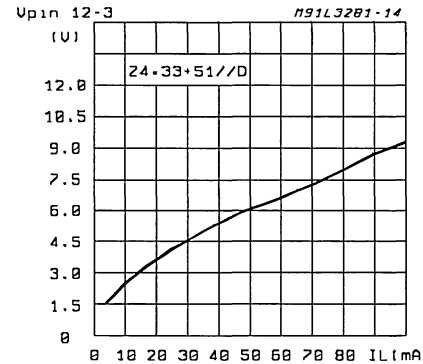


Figure 7: Zener Equivalent.

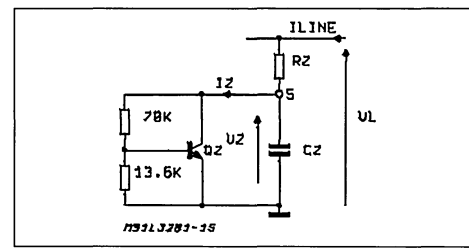
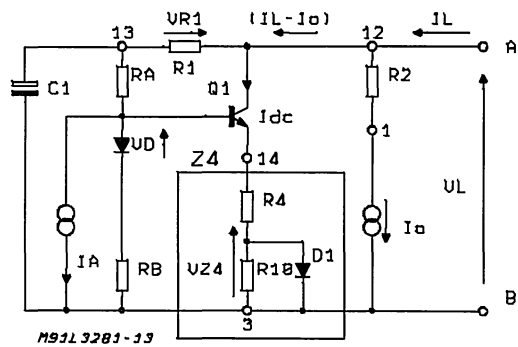


Figure 5: Equivalent Simplified Circuit



AC CHARACTERISTIC

The AC Impedance measured at line terminals is equal to:

$$Zm = (R1 + \frac{1}{jwC1}) // (R2 + R3 + Zb)$$

The value of the capacitor C1 must be In the range of 22 µF to 100 µF.

The external resistor R1 can be replaced by a resistor/capacitor network in order to realize a complex Impedance Zm.

TRANSMITTING CIRCUIT

The first block of the TX stage is basically a differential amplifier which converts voltage to current. The inputs are internally polarized at 300 mVdc. The differential Input impedance is 60 KΩ to allow a good matching to microphone. The AGC in TX is function of voltage at pin 14 in order to decrease to max gain of 5.5dB to 6.0dB when the line current increases.

Figure 8: Equivalent Transmitting Circuit.

RECEIVING CIRCUIT

Fig.9 shows the equivalent receiving circuit. The differential input of RX signal across R2+R3 is transferred to the AGC block when the mute signal (pin 10) is not active.

The AGC in RX is a function of the voltage at pin 14 and decreases the gain when the line current increases (5.5dB to 6.0dB).

The final stage is a single ended amplifier with low output impedance optimized to drive magnetic/dynamic transducers.

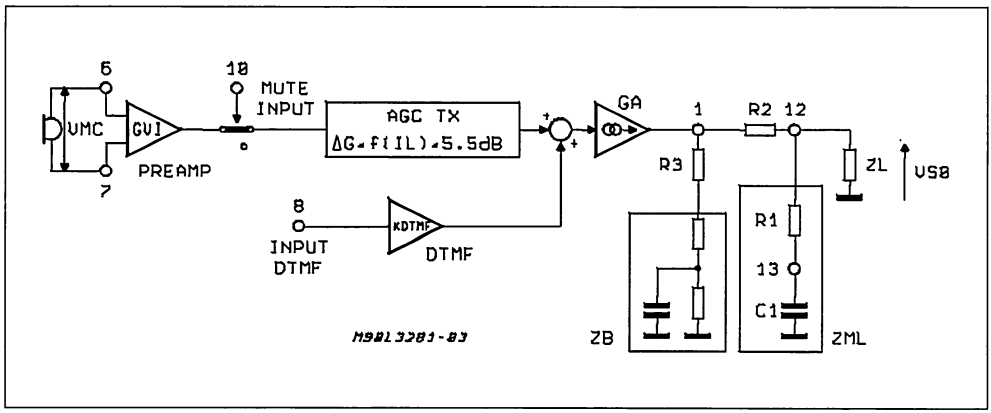
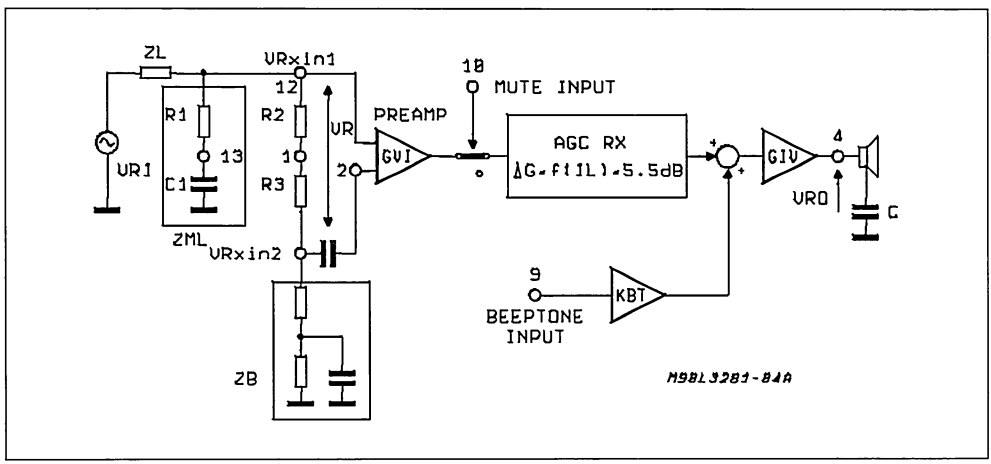
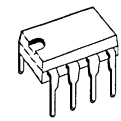


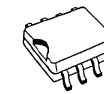
Figure 9: Equivalent Receiving Circuit.



TRUNK INTERFACE

- ON CHIP POLARITY GUARD
- MEETS DC LINE CHARACTERISTICS OF EITHER CCITT AND EIA RS 464 SPECS
- PULSE FUNCTION
- HIGH AC IMPEDANCE
- OFF HOOK-STATUS DETECTION OUTPUT
- LOW EXTERNAL COMPONENT COUNT





Minidip **SO8**

ORDERING NUMBERS:

L3845B L3845D

DESCRIPTION

The circuit provides DC loop termination for analog trunk lines.

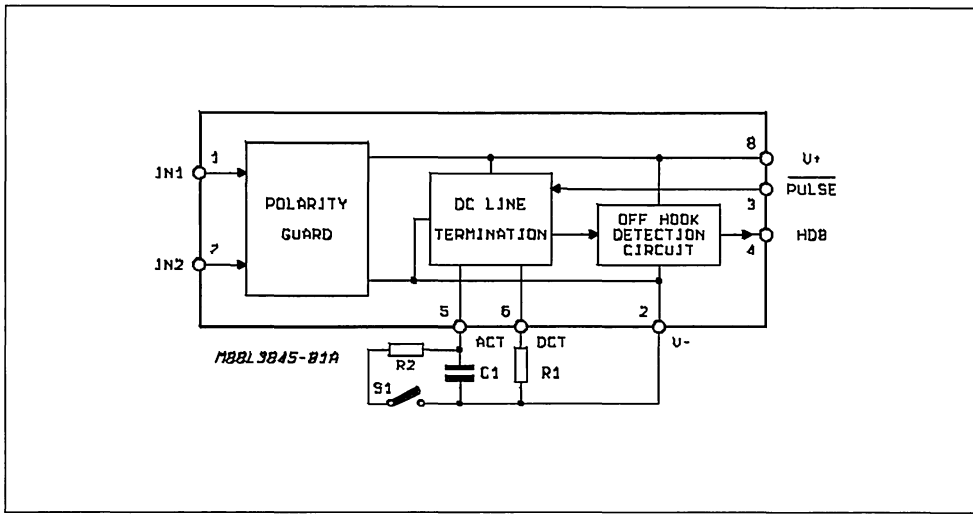
The V-I characteristics is equivalent to a fixed voltage drop (zener like characteristic) in series with an external resistance that determines the slope of the DC characteristic.

An external low voltage electrolytic capacitor causes the circuit to exhibit a very high impedance to all AC signal above a minimum frequency that is determined by the capacitor itself and by a 20 K nominal resistor integrated on the chip.

The Off-Hook status is detected all the time a typic of 8 mA is flowing into the circuit. In this condition a constant current generator is activated to supply an external device (typically an optocoupler) without affecting the AC characteristic of the circuit.

When Pulse Dialing is required the $\overline{\text{PULSE}}$ input (pin 3) connected to V- causes the device to reduce the fixed DC voltage drop and to exhibit a pure resistive impedance equal to the external resistor.

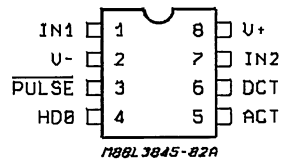
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_L	Max Line Voltage (pulse duration 10 ms max)	20	V
I_L	Max Line Current	150	mA
P_{tot}	Total Power Dissipation at Tamb = 70 °C	800	mW
T_{op}	Operating Temperature	– 40 to + 70	°C
T_{srg}, T_j	Storage and Junction Temperature	– 55 to + 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Minidip	SO8	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (*)	Max.	80	140 to 180	°C/W

(*) Mounted on FR4 Boards

DC ELECTRICAL CHARACTERISTICS (I_L = 10 mA to 100 mA, R_1 = 56 Ω, S_1 = Open, T_{amb} = + 25 °C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_L	Line Voltage (normal mode)	PULSE = Open IL = 10 mA I_L = 20 mA I_L = 100 mA			 5 6 12	 V V V
V_{LP}	Line Voltage (pulse mode)	PULSE = V^- I_L = 20 mA I_L = 35 mA I_L = 80 mA			 4 5.5 9.5	 V V V
I_{hn}	ON/OFF-Hook Line Current Detection Threshold		6.5		9.5	mA
I_{hf}	OFF/ON-Hook Line Current Detection Threshold		5		9.2	mA
I_{OUT}	OFF-Hook Output Drive Current at Pin HDO	IL = 10 mA $I_L \geq$ 20 mA	1.5 2			mA mA
V_{PM}	Pulse Input Low Voltage				0.8	V
I_{PM}	Pull-up Input Current at Pin PULSE (pulse mode)	IL = 100 mA Pulse = V^-			20	µA
I_{NM}	Imput Current at Pin Pulse (normal mode)				3	µA

AC ELECTRICAL CHARACTERISTICS (I_L = 10 mA to 100 mA, R_1 = 56 Ω, R_2 = 470 KΩ, S_1 = Open, T_{amb} = + 25 °C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_L	AC Line Impedance	C_1 = 2.2mF f = 1KHz		 20		. KΩ
	Sending/Receiving Distortion	f = 1KHz V_S = 775mVrms I_L = 15 to 100mA			 2	 %
	Sending/Receiving Distortion	S_1 = Closed; V_S = 1.3Vrms		 2		 %

APPLICATION INFORMATION

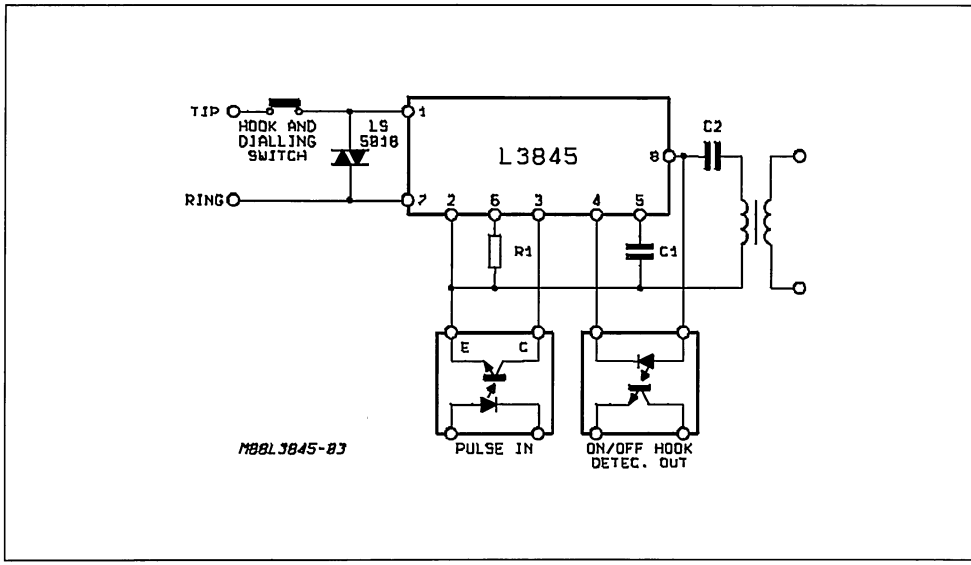
With the use of this circuit it is possible to terminate an analog trunk so that all the DC current component is flowing in the TRUNK TERMINATION CIRCUIT while the AC component is decoupled with a low voltage capacitor and can be used with a small and low cost audio coupler transformer to provide the AC balancing termination and two to four wire conversion.

Therefore it is usefull both for MODEM and PABX systems.

Figure 1 gives the typical application circuit ; it is worth to note that the TRUNK TERMINATION CIRCUIT, together with the LS5018 transient suppressor provides a compact and low cost module fully protected against lightning or overvoltages frequently present on telephone lines.

The $\overline{\text{PULSE}}$ input when connected to V- allows the device to reduce the Line Voltage and to show a resistive impedance equal to R1 to the line. When $\overline{\text{PULSE}}$ input is left open, this function is disable.

Figure 1: Typical Application.



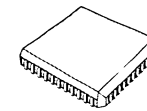
SGS-THOMSON MICROELECTRONICS

L3913

MONOCHIP TELEPHONE

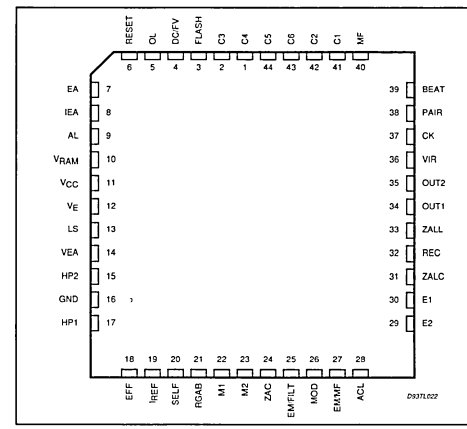
ADVANCE DATA

- ADJUSTABLE SLOPE OF DC CHARACTERISTIC
- ADJUSTABLE AUTOMATIC LINE LENGHT RECEIVING AND SENDING GAIN CONTROL (NOT USED IN DTMF), WITH POSSIBILITY OF FIXED GAIN (PABX).
- ADJUSTABLE AUTOMATIC LINE LENGHT TRACKING ANTISIDETONE SYSTEM
- ADJUSTABLE DYNAMIC IMPEDANCE
- STABILIZED POWER SUPPLY FOR PERIPHERALS
- CONFIDENCE LEVEL DURING PULSE AND DTMF DIALLING
- RECEIVING AMPLIFIER FOR DYNAMIC OR PIEZO-ELECTRIC EARPIECES
- HIGH IMPEDANCE MICROPHONE INPUTS (80KΩ MIN. IN SYMMETRICAL AND 40KΩ MIN. IN ASYMMETRICAL) SUITABLE FOR DYNAMIC, MAGNETIC, PIEZO-ELECTRIC OR ELECTRET MICROPHONE
- DYNAMIC LIMITING IN SENDING (ANTICLIPPING) PREVENTS DISTORTION OF LINE SIGNAL AND SIDETONE
- ANTISQUELCH SYSTEM IN SENDING PREVENTS "ROOM NOISE" TO BE TRANSMITTED, AND IMPROVES THE ANTI-LARSEN EFFICIENCY
- LOUDHEARING PROGRAMMABLE GAIN IN 8 STEPS OF 3 dB USING THE SERIAL BUS, OR LINEARLY USING A POTENTIOMETER
- ANTILARSEN SYSTEM WHICH DOESN'T CUT THE RECEIVING VOICE
- ANTIDISTORTION SYSTEM BY AUTOMATIC GAIN CONTROL VERSUS AVAILABLE LOUDHEARING CURRENT
- RINGING BALANCED OUTPUT IN DMOS FOR HIGHER POWER CAPABILITY
- 4 RINGING TONES ADJUSTABLE WITHOUT EXTERNAL COMPONENTS
- INTERNAL SPEED UP CIRCUIT PERMITS A FASTER CHARGE OF V_{CC} AND V_{RAM} CAPACITORS
- LOGIC BOUNCE ELIMINATION
- PULSE DIALLING 66/33 OR 60/40 OR DTMF DIALLING SELECTABLE BY PROGRAMMING PIN
- ADJUSTABLE FLASHING DURATION (90ms or 265ms)



PLCC-44

PIN CONNECTION (top view)

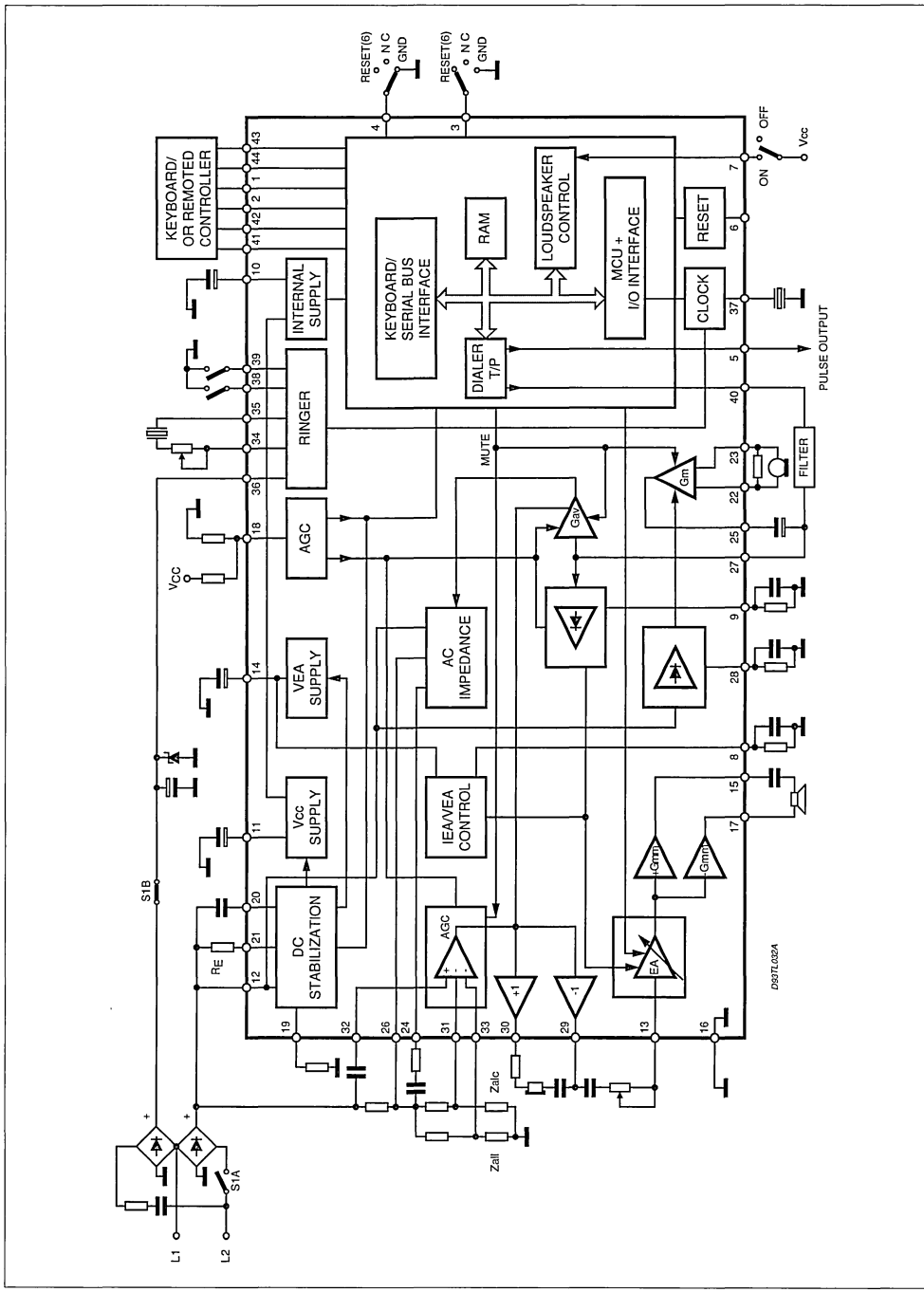


- INTERDIGITAL PAUSE
- CONFIDENCE TONE (440Hz)
- LAST NUMBER RADIAL UP TO 23 DIGITS
- STANDARD LOW COST CERAMIC 455KHz
- BINARY DATA INPUT IN SERIAL MODE
- TEST MODE CAPABILITY

DESCRIPTION

The L3913 monochip is a BIPOLAR CMOS-DMOS (BCD) integrated circuit that performs all the speech and line interface functions required in an electronic telephone set, the ringing function with 4 melodies, the pulse and DTMF dialling with redial, the loudhearing with antilarsen and antidistortion systems, a keyboard interface with the possilbility to interface with an external microcontroller using the internal serial bus, and a power supply for peripheral.

BLOCK DIAGRAM



PIN FUNCTIONS

N°	Name	Description
1	C4	Keyboards inputs
2	C3	Keyboard inputs
3	FLASH	Flashing selection (80 or 265ms)
4	DC/FV	Dialling selection (33/66 pulse, 40/60 pulse or DTMF)
5	OL	Open line output
6	RESET	Output reset in normal case, input reset in test mode
7	EA	Loudhearing ON/OFF
8	IEA	Antidistortion time constant adjustment in loudhearing
9	AL	Antilarsen time constant adjustment in loudhearing
10	V_{RAM}	RAM and internal logic supply
11	V_{CC}	Power supply for peripherals
12	V_E	Line voltage
13	LS	Loudhearing input
14	VEA	Loudhearing supply
15	HP2	Loudspeaker output
16	GND	Ground
17	HP1	Loudspeaker output
18	EFF	line lenght AGC adjustment
19	I_{REF}	Bias adjustment
20	SELF	Electronic self input
21	RGAB	DC characteristic slope adjustment
22	M1	Microphone input
23	M2	Microphone input
24	ZAC	Dynamic impedance adjustment
25	EM/FILT	First sending stage output
26	MOD	Modulator output
27	EM/MF	NSecond sending stage input and DTMF input
28	ACL	Anticlipping time constant adjustment
29	E2	Receiver output
30	E1	Receiver output
31	ZALC	Short line sidetone network
32	REC	Receiver input
33	ZALL	Long line sidetone network
34	OUT1	Buzzer output
35	OUT2	Buzzer output
36	VIR	Ringing supply
37	CK	Ceramic input (455KHz)
38	PAIR	Ajustment between 2 pairs of ringing frequencies
39	BEAT	Beat ajustment of each pair
40	MF	DTMF output
41	C1	Keyboard inputs
42	C2	Keyboard Inputs
43	C6	Keyboard inputs
44	C5	Keyboard inputs

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; f = 1kHz; R_E = 20kΩ; all resistance are specified at 1%, all capacitance at 2%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
DC CHARACTERISTICS							
V_L	Line Voltage	I_L = 15mA I_L = 25mA I_L = 60mA	- 5.75 12.75	4.4 6.15 13.15	4.9 6.55 13.55	V V V	1 1 1
V_{CC}	Stabilized Voltage Supply	ICC = 0.6mA I_L = 8.3mA	2	2.5	-	V	1
		I_{CC} = 2.1mA I_L = 25mA	3.15	3.4	3.65	V	1
I_{RAM}	Operative	VRAM = 3.5V	-	-	500	µA	
I_{RAM}	STAND-BY	VRAM = 3.5V	-	-	300	nA	
RECEPTION							
GR1	Receiving Gain	I_L = 25mA V_L = 0.3Vrms	10	11	12	dB	2
GR2	Receiving Gain	I_L = 60mA (see AGCR)	2.5	4	5.5	dB	2
AGCR	Delta Gain Receive	I_L = 60mA (to be applied only if GR2 is not respected)	6.3	7	7.7	dB	2
R_X	Distortion	I_L = 30mA; V_{out} = 5Vpp	-	0.6	3	%	2
		I_L = 60mA; V_{out} = 5Vpp	-	0.6	3	%	2
Z_{out}	Receiver	I_L = 25mA; V_{out} = 50mVrms	45	65	85	Ω	2
R_X	Offset	I_L = 25mA / 60mA	-500	-	500	mV	2
	Sidetone	I_L = 25mA V_{MI} = 2mVrms I_L = 60mA	- -	30 16	- -	dB dB	1 1
TRANSMISSION							
GS1	Sending GAIN	I_L = 25mA V_{mic} = 2mVrms	47.5	48.5	49.5	dB	1
GS2	Sending GAIN	I_L = 60mA (see SGCS)	40.4	41.9	43.4	dB	1
AGCS	Delta GAIN sending	I_L = 60mA (to be applied only if GS2 is not respected)	5.9	6.6	7.3	dB	1
CMRR	Common Mode Rejection	I_L = 25mA; V_{cm} = 50mVrms	-	75	-	dB	1
T_x	Distortion	I_L = 36mA V_{mi} = 5mVrms V_{mi} = 5mVrms + 10dB V_{mi} = 5mVrms + 20dB	- - -	- - -	3 5 7	% % %	1 1 1
AS	GAIN Attenuation	I_L = 25mA V_{mi} = 2mVrms	65	-	-	dB	1
Z_{in}	Microphone Impedance	I_L = 30mA	85	120	-	KΩ	1
T_x	Offset Pin 25 (DTMF - T_x)	I_L = 25mA / 60mA	- 100		+ 100	mV	1
$T_{x\ swing}$	Tx Output Voltage Swing	I_L = 36mA V_{mic} = 5mVrms+10dB	3.2	3.8	4.4	Vpp	1
$T_{x\ squelch}$	Dynamic Range	IL = 25mA V_{mic} = 1mVrms/0.15mVrms	7.5	9	10.5	dB	1
Z_{LINE}	Matching	I_L = 25mA I_L = 60mA	580	630	680	Ω	2
NOISE							
T_x	Noise	I_L = 25mA (psophometric)	-	- 78	-	dBmp	1
R_x	Noise	I_L = 25mA (psophometric)	-	200	-	µVp	2

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
LOUDHEARING							
V_{ea}	Loudhearing Supply	I_L = 25mA I_L = 60mA	3.5 7.8	3.8 8.2	4.1 8.9	V V	3 3
G_{ea}	Loudhearing Gain	I_L = 30 / 50mA V_{LS} = 20mVrms	19.7	20.7	21.7	dB	3
ΔG_{ea}	8 Steps Programmable Gain Using Serial Bus	IL = 25 / 60mA V_{LS} = 20mVrms	-	3	-	dB	3
Z_{ih}	Input Impedance	I_L = 30mA	24	34	44	KΩ	3
LH	Distortion LOAD = 100Ω	I_L = 50mA V_{ILINE} = 200mVrms V_{ILINE} =350mVrms	- -	1 4.5	3 7	% %	3 3
LH	Offset	I_L = 25mA	-120	-	+120	mV	3
I_{LEAK}	Leakage Pin I_{EA}	I_L = 25mA	-	-	100	nA	3
LH	Offset Pin AL	I_L = 25mA	-	-	150	mV	3
LH	Antilarsen Attenuation	I_L = 30mA Pin 9 to V_{CC}	5.75	6.25	6.75	dB	3
RINGER							
$V_{turn-on}$	Threshold on	Measured at Pin V_{IR}	14	15	17	V	4
$V_{turn-off}$	Threshold off		10.5	12	14	V	4
I_S	Supply Current	V_S = 17V no load	-	1.2	1.6	mA	4
F_{out}	Frequencies	Pin 38 = GND V_{IR} = 32V	1450 1160	1458 1166	1465 1172	Hz Hz	4 4
		Pin 38 = Open V_{IR} = 32V	544 435	547 438	550 441	Hz Hz	4 4
		Pin 39 = GND Pin 39 = Open V_{IR} = 32V	3.9 9	4 9.1	4.1 9.2	Hz Hz	4 4
V_{out}	Output Voltage Swing	V_{IR} = 32V	30	-	-	V	4
I_{IL}	Input Low	V_{IR} = 32V BEAT, PAIR (Pins 38, 39) V_{IL} = 1V	- 12	- 7	- 1.5	µA	4
DTMF GENERATION							
	DTMF Frequency Tolerances	I_L = 25mA	-0.4	-	+0.25	%	1
	DTMF Level	I_L = 25 / 60mA Low group High group Preemphasis	 -10 -8 1	 -8 -6 2	 -6 -4 3	 dBm dBm dB	 1 1 1
	DTMF Distortion	I_L = 25mA BW = 20kHz	see MASK fig. 6				
	DTMF Feedback	I_L = 60mA referred to the line voltage RX LH	 - -	 - 19 - 2.5	 - -	 dB dB	 5 5
	Flash Operating Current		8.3	-	-	mA	1
TMF	Transmission Time		80.1	81.7	83.3	ms	1
T_{IDMF}	Interdigit Time		87.4	89.2	91.5	ms	1
Tm_{MF}	Transmission Mute		167.5	170.9	174.3	ms	1
	Confidence Tone	Only by Serial Bus I_L = 25mA	-	440.9		Hz	1
	Confidence Tone Level		-	- 9	-	dBm	1

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
LEAKAGE (V_{RAM} = 3.5V)							
I_{KL}	Input Low (Keyboard current)	C1 % C6 (pins 1, 2, 41 % 44) V_{IL} = 0.5V	1.5	-	5	µA	
I_{il}	Input Low	C1 % C6 (pins 1, 2, 41 % 44) V_{IL} = 0.4V	150	450	1300	µA	
		CK (pin 37) V_{IL} = 0.5V	-	-	1	µA	
I_{ih}	Input High	EA (pin 7) V_{IH} = 3.5V	5	11.5	16	µA	
		DCFV (pin 4), Flash (3) V_{IL} = 0V	- 10	- 6	- 1.5	µA	
		C1 % C6 (pins 1, 2, 41 % 44) V_{IH} = 3.1V	- 1300	- 450	- 150	µA	
		DCFV (pin 4), Flash (3), CK(37) V_{IH} = 3.5V	- -	- -	1 1	µA µA	
I_{ol}	Output Low	Reset (pin 6) V_{OL} = 0.4V OL (pin 5)	0.2 0.7	- -	1.3 3.7	mA mA	
I_{oh}	Output High	Reset (pin 6) VOH = 2.85V OL (pin 5) V_{OH} = 0.7V	- 1.8 - 30	- 0.6 -	- 0.2 - 8	mA µA	
TIMING AND FREQUENCY							
t_r	Reset Time	In mode DTMF In mode 60/40 In mode 66/33	- - -	34.3 30 33	- - -	ms ms ms	7 7 7
t_{on}	Clock Start-up Time		-	5	-	ms	
t_{lb}	Time line Break generating a Reset	In mode 60/40 In mode 66/33 In mode DTMF	290 319 341	- - -	300 330 343	ms ms ms	7 7 7
t_e	Debounce Time	In mode 60/40 In mode 66/33 In mode DTMF	14 15.4 16	24 26.4 27.4	34 37.4 38.9	ms ms ms	
SERIAL BUS							
t_{wl}, t_{wh}	Pulse Width Clock		2	-	-	µs	8
t_{el}, t_{eh}	Pulse Width Enable Signal		2	-	-	µs	8
$t_{set\ up}$	Set-up Time Data to Clock		0	-	-	ns	8
	Hold Time Data Drom Clock		100	-	-	ns	8
t_e	Enable Time		0	-	-	ns	8
t_{RRN}	Time Between two Transmissions		900	-	-	µs	8
PULSE DIALLING (OL)							
	Dialling Pulse Frequency	In mode 60/40 (pin 4 tied to RESET)	-	10	-	Hz	
		In mode 66/33 (pin 4 not Connected)	-	10.11	-	Hz	
T_{OL}	Dialling Pulse Period	pin 4 tied to RESET pin 4 n.c.	- -	100 98.9	- -	ms ms	
t_b	Break Time	pin 4 tied to RESET pin 4 n.c.	- -	60 66	- -	ms ms	
t_m	Make Time	pin 4 tied to RESET pin 4 n.c.	- -	40 33	- -	ms ms	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
PULSE DIALLING (OL) continued.							
t_{IDOL}	Interdigit		830 813	- -	833 816.5	ms ms	
t_{mol}	Transmission Mute n Pulses Dialling	*See note below*					
t_{Fl}	Flash Pulse Duration	Pin 3 to GND, Pin 4 n.c. Pin 3 n.c., Pin 4 n.c. Pin 3 to GND, Pin 4 to Reset Pin 3 to GND, Pin 4 to GND Pin 3 n.c., Pin 4 to Reset Pin 3 n.c., Pin 4 to GND Pin 3 to Reset, Pin 4 to Reset Pin 3 to Reset, Pin 4 to GND Pin 3 to Reset, Pin 4 n.c.	99 264 90 92 240 264 110 115 121	- - - - - - - - -	101.2 266.2 92 94 242.2 266 112.2 117 123.2	ms ms ms ms ms ms ms ms ms	
t_{mfl}	Transmission Mute	In mode 60/40 In mode 66/33 In mode DTMF	830 813 860	- - -	832 815.5 880	ms ms ms	
t_p	Pause Time	In mode 60/40 In mode 66/33 In mode DTMF	3034 2994 3028	- - -	3038 2998 3032	ms ms ms	
	Clock Keyboard: Minimum time to respect, in order to take the pressed pushbutton into account	Pin 4 to pin 6 Pin 4 n.c. Pin 4 to GND	14 15.4 16	24 26.4 27.4	34 37.4 38.9	ms ms ms	
	Clock Keyboard: Minimum time to respect, in order to take the released pushbutton into account	Pin 4 to pin 6 Pin 4 n.c. Pin 4 to GND	24 26.4 27.4	24 26.4 27.4	34 37.4 38.9	ms ms ms	

Note:

Min.	Max.	Unit
n x 100 + 30	n x 100 + 32	ms
n x 98.9 + 22	n x 100 + 24.2	ms

TEST CIRCUITS

Figure 1.

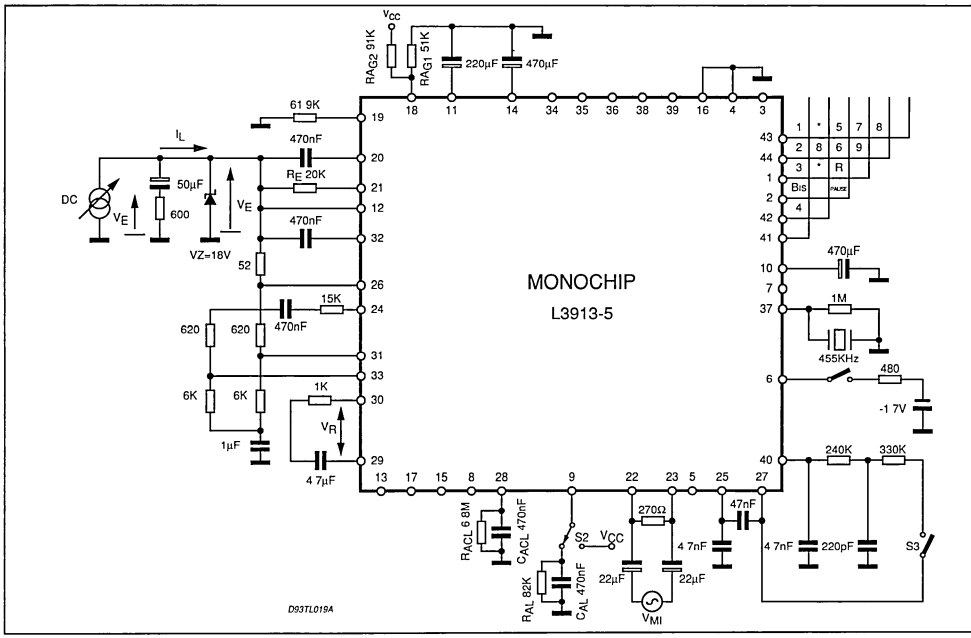


Figure 2.

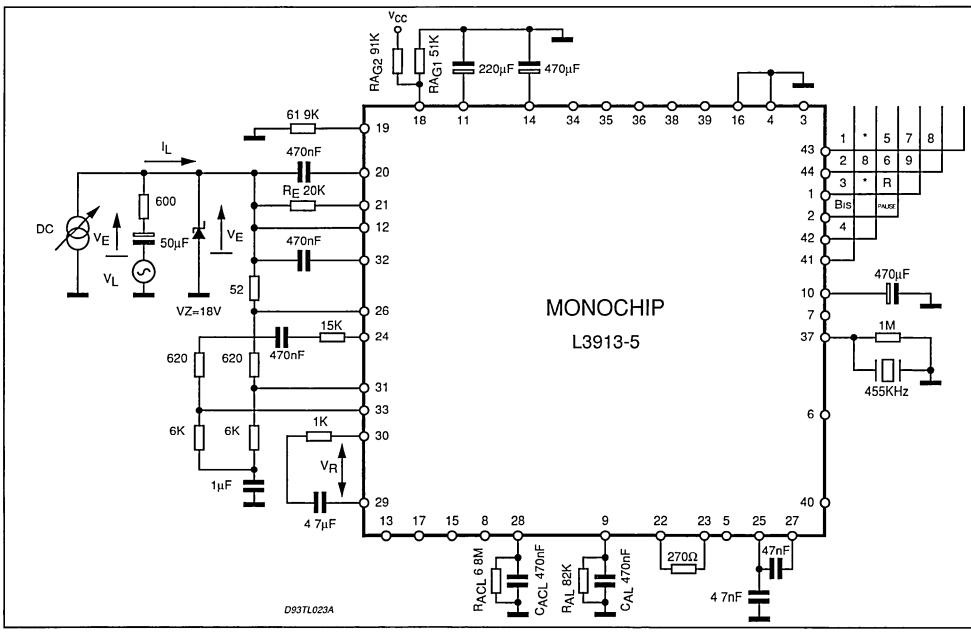


Figure 3.

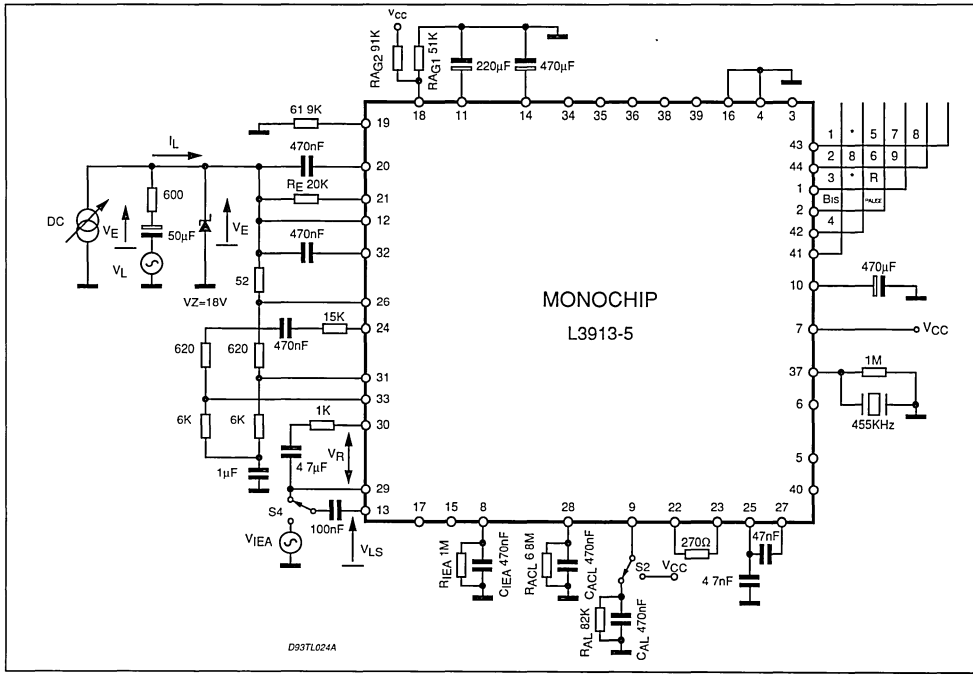
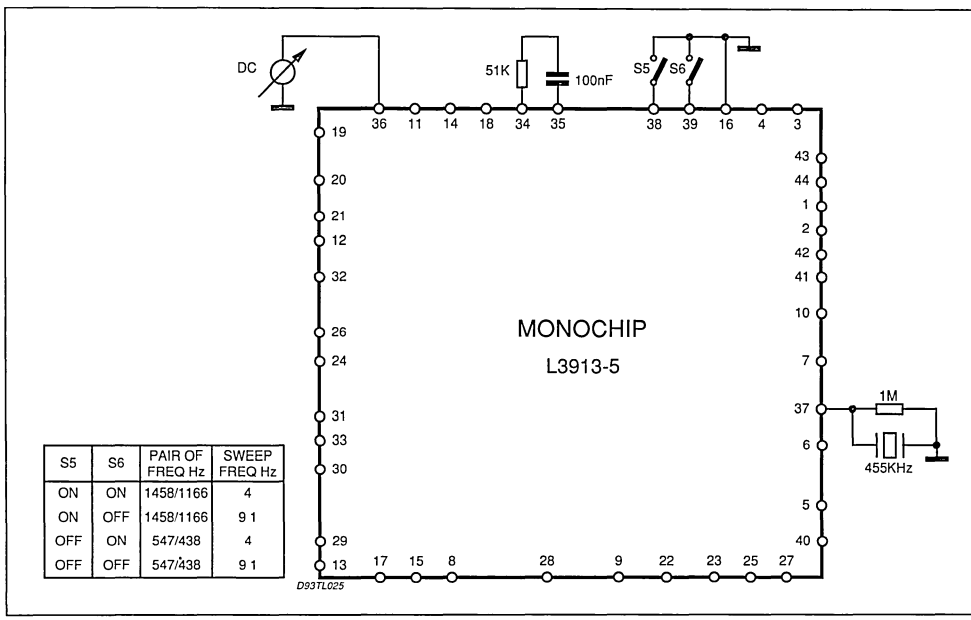


Figure 4.



S5	S6	PAIR OF FREQ Hz	SWEEP FREQ Hz
ON	ON	1458/1166	4
ON	OFF	1458/1166	9 1
OFF	ON	547/438	4
OFF	OFF	547/438	9 1

Figure 5.

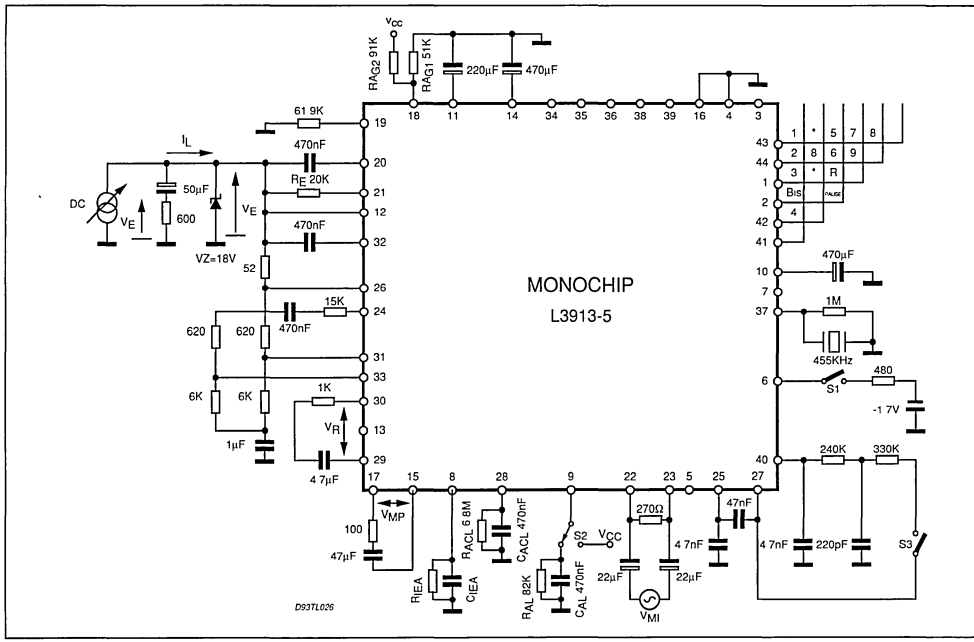
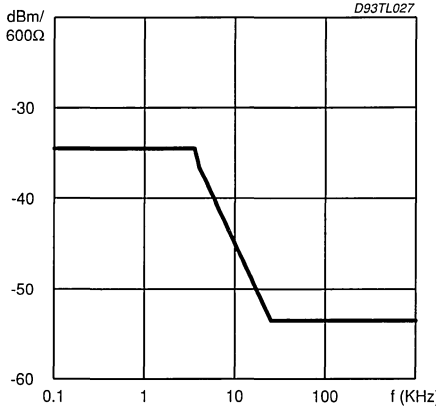


Figure 6: DTMF Distortion French Specification.



LINE BREAK DESCRIPTION

After a line break longer than a Time Line Break (tlb) an internal reset is generated. A short line break < tlb does not affect the reset.

POWER ON RESET TIMINGS (After Line Break)

Figure 7a: $V_{RAM} > V_{Son}$ at t = 0

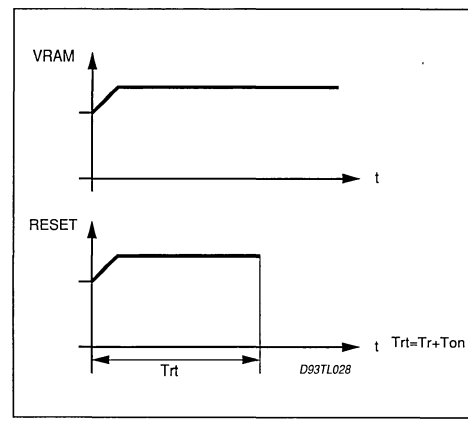
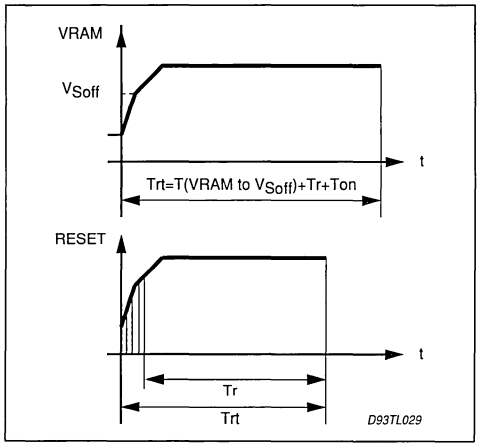
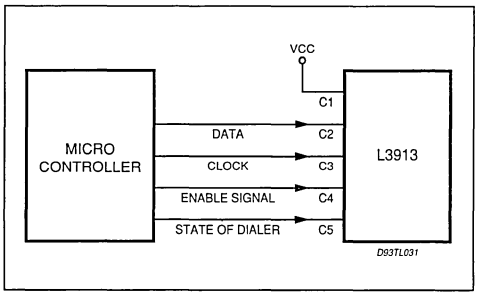


Figure 7b: $V_{RAM} < V_{Son}$ at t = 0



Pin reset: It is the power on reset output.

Figure 8.



DIALER FUNCTIONAL DESCRIPTION

The monochip includes a dialling circuit for either pulse dialling or dual tone multifrequency dialling.

The dialler transmits the codes decoded by the logic keyboard on the outputs 0L and DTMF.

DIALING MODE SELECTION

The default dialling mode is selected by the tri-level pin DC/FV (pin 4):

- DC/FV open: pulse dialling in 66/33ms
- DC/FV to pin Reset: pulse dialling in 60/40ms
- DC/FV to pin GND: DTMF dialling calibrated
- mixed mode

When the circuit is in pulse mode, it is possible to change to DTMF dialling with the " * " key. The circuit returns in pulse mode after a reset condition or after a flash pulse.

DIALLING CODES

These are the numeric keys 0 to 9, and the non numeric keys A, B, C, D, *, #. All of them are stored in RAM.

The codes A, B, C, D can be only transmitted by the serial bus, not by standard key board.

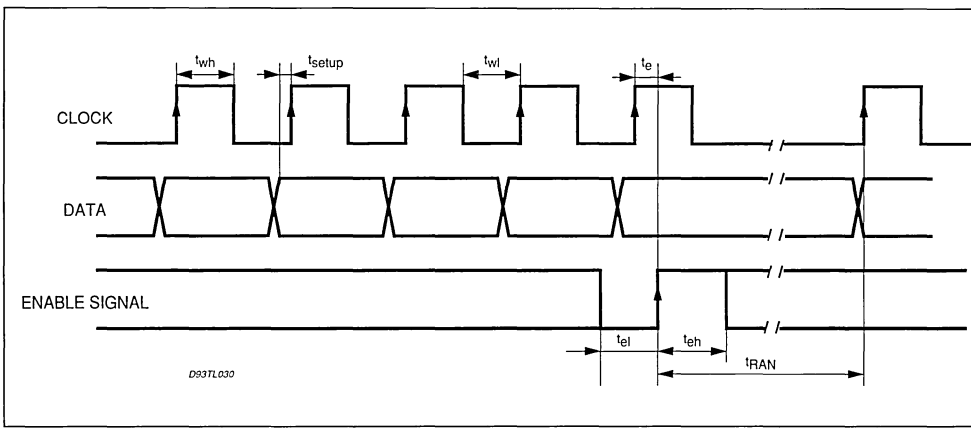
In pulse dialling, the code #, B, C, D have no effect on the dialling. The code A (in pulse mode) corresponds to 11 pulses.

SERIAL BUS DESCRIPTION

A microcontroller can be connected to the monochip by 4 pins C2, C3, C4, C5 (see fig. 8)

C1 must be connected to V_{CC} to select the serial mode operation.

Figure 9: Timing serial bus.



C2 sends the data, C3 the clock, C4 the enable signal, C5 indicates the state of the dialler (if C5 = 0 the dialler is busy, if C5 = 1 the dialler is free).

Data is a 5 bits serial word shifted in a 5 bits register during the positive transition of the clock pulse. The positive transition of the enable signal validates the acquisition of the last 5 bits.

Timings diagram in fig. 9 shows the details of serial bus synchronization.

Table 1 explains the "CODE ENTRY" in serial bus mode.

Table 1: Code Enties.

0	0	0	0	0	*
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	0
0	1	0	1	1	A
0	1	1	0	0	B
0	1	1	0	1	C
0	1	1	1	0	D
0	1	1	1	1	*
1	0	0	0	0	RESERVED
1	0	0	0	1	R: FLASH
1	0	0	1	0	REDIAL
1	0	0	1	1	LOUDSPEAKER ON
1	0	1	0	0	CONFIDENCE TONE
1	0	1	0	1	MICROPHONE MUTE
1	0	1	1	0	PAUSE
1	0	1	1	1	RESERVED
1	1	0	0	0	LOUDSPEAKER LEVEL 0dB
1	1	0	0	1	LOUDSPEAKER LEVEL 3dB
1	1	0	1	0	LOUDSPEAKER LEVEL 6dB
1	1	0	1	1	LOUDSPEAKER LEVEL 9dB
1	1	1	0	0	LOUDSPEAKER LEVEL 12dB
1	1	1	0	1	LOUDSPEAKER LEVEL 15dB
1	1	1	1	0	LOUDSPEAKER LEVEL 18dB
1	1	1	1	1	LOUDSPEAKER LEVEL 21dB

LOW RANGE ONE CHIP PHONE (SPEECH AND DIALER)

ADVANCE DATA

Speech Circuit

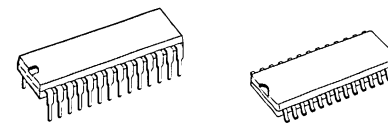
- 2 TO 4 WIRES CONVERSION
- PRESENT THE PROPER DC PATH FOR THE LINE CURRENT AND THE FLEXIBILITY TO ADJUST IT AND ALLOW PARALLEL PHONE OPERATION
- PROVIDES SUPPLY WITH LIMITED CURRENT FOR EXTERNAL CIRCUITRY
- SYMMETRICAL HIGH IMPEDANCE MICROPHONE INPUTS SUITABLE FOR DYNAMIC ELECTRET OR PIEZOELECTRIC TRANSDUCER
- ASYMMETRICAL EARPHONE OUTPUT SUITABLE FOR DYNAMIC TRANSDUCER
- LINE LOSS COMPENSATION
- INTERNAL MUTING TO DISABLE SPEECH DURING DIALING
- HOLD FUNCTION FOR PARALLEL PHONE WITH 400ms DELAY TO PREVENT FALSE RELEASE

Dialer Circuit

- 32 DIGITS FOR LAST NUMBER REDIAL BUFFER
- 18 DIGITS FOR 13 MEMORY REDIAL
- ALLOW MIXED MODE DIALING IN EITHER TONE OR PULSE MODE
- PACIFIER TONE PROVIDES AUDIBLE INDICATION OF VALID KEY PRESSED IN A BUZZER OR/AND IN THE EARPHONE
- TIMED PABX PAUSE
- FLASH INITIATES TIMED BREAK
- CONTINUOUS TONE FOR EACH DIGIT UNTIL KEY RELEASE
- USES INEXPENSIVE 3.579545MHz CERAMIC RESONATOR
- POWERED FROM TELEPHONE LINE, LOW OPERATING VOLTAGE FOR LONG LOOP APPLICATION

DESCRIPTION

The device consists of the speech and the dialer. It provides the DC line interface circuit that terminates the telephone line, analog amplifier for speech transmission and necessary signals for either DTMF or loop disconnect (pulse) dialing.

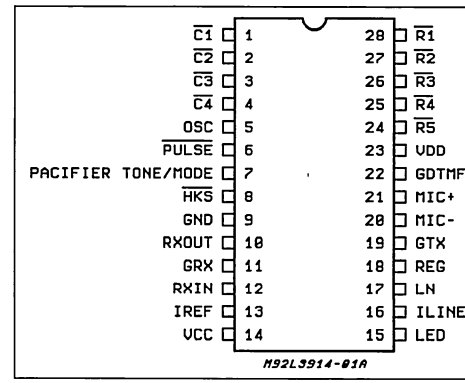


DIP28 **SO28**

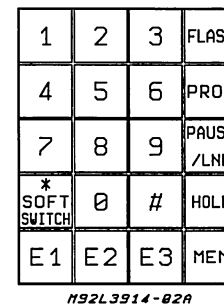
ORDERING NUMBERS:

L3914N L3914D

PIN CONNECTION (Top view)

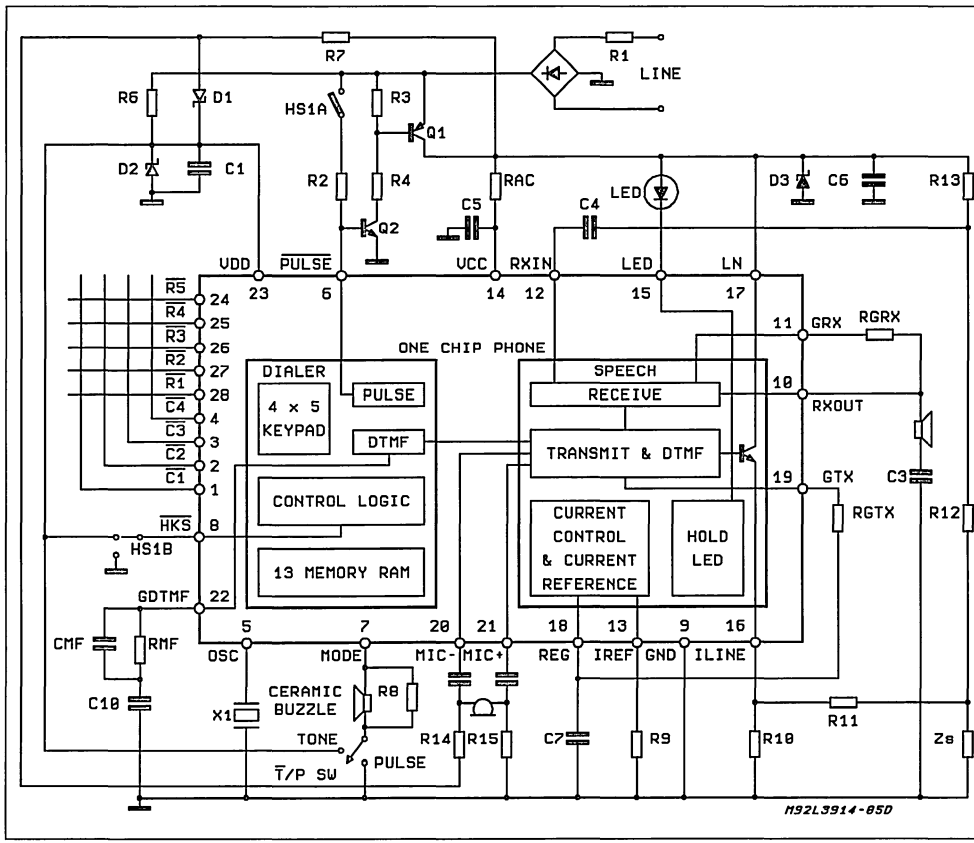


KEYPAD CONFIGURATION



Note: PAUSE/LND:
PAUSE and LND functions are sharing the same key with different sequence. Hereafter, PAUSE and LND keys are referring to the same key.

BLOCK DIAGRAM



When mated with a tone ringer, a complete telephone can be produced with just two ICs.

The DC line interface circuit develops its own line voltage across the device and it is adjustable by external resistor to suit different country's specification.

The speech network provides the two to four wires interface, electronic switching between dialing and speech and automatic gain control on transmit and receive.

The dialing network buffers up to 32 digits into the LND memory that can be later redialed with a single key input. Additionally, another 13 memories (including 3 emergency memories) of 18 digits memory is available. Users can store all 13 signalling keys and access several unique functions with single key entries. These functions include: Pause/Last Number Dialed (LND), Softswitch, Flash and Hold.

The FLASH key simulates a 585ms hook flash to transfer calls or to activate other special features provided by the PABX or central office.

The PAUSE key stores a timed pause in the number sequence. Redial is then delayed until an outside line can be accessed or some other activity occurs before normal signaling resumes.

A LND key input automatically redials the last number dialed.

The HOLD key allows the user to suspend the conversation and resume the call on either the same phone by pressing the HOLD key again or resume the conversation at a parallel phone.

FUNCTION PIN DESCRIPTION

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R5}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$

Keyboards inputs. Pins 1, 2, 3, 4, 24, 25, 26, 27, 28. The one chip phone interfaces with either the standard 2-of-9 with negative common or the single-contact (Form A) keyboard.

FUNCTION PIN DESCRIPTION (continued)

A valid keypad entry is either a single Row connected to a single Column or GND simultaneously presented to both a single Row and a single Colunm.
In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at logic level 1 (V_{DD}). Pulling one input low enables the on chip oscillator. Keyboard scanning then begins.

Scanning consists of Rows and Columns alternately switching high through on chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc) is ignored for a debounce period (TKD) of 32ms. At this time, the keyboard is sampled and if both the Row and Column information are valid, the information is buffered into the LND location. After scanning starts, the row and column inputs will assume opposite states.

In the tone mode, if two or more keys in the same row or if two or more keys in the same column are depressed a single tone will be output. The tone will corresponds to the row or column for which the two keys were pushed. This feature is for testing purposes, and single tone will not be redialed. Also in the tone mode, the output tone is continuous in the manual dialing as long as the key is pushed. The output tone duration follows the Table 1. When redialing in the tone mode, each DTMF output has 100ms duration, and the tone separation (inter signal delay) is 100ms.

Table 1: Output Tone Duration

Key-Push Time, T	Tone Output
T<= 32ms	No output, ignored by one chip phone.
32ms < = T < = 100ms + Tkd	100ms Duration
T > = 100ms + Tkd	Output Duration = T - Tkd

OSC

Output. Pin 5. Only one pin is needed to connect the ceramic resonator to the oscillator circuit. The other end of the resonator is connected to GND (pin 8). The nominal resonator frequency is 3.579545MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The ceramic resonator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ±0.25% is recommended.

$\overline{\text{PULSE}}$

Output. Pin 6. This is an output consisting of an open drain N-Channel device. During on-hook, pulse output pin is in high impedance and once off-hooked, it will be pulled high by external resistor. The pulse out will go high when the Hold key is pressed, in this way the phone will stay connected to the line untill the parallel phone is hooked-OFF or the Hold Key is pressed again.

MODE/PACIFIER TONE

Input (MODE). Pin 7. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook (V_{DD}) to off-hook (GND), the default determines the signalling mode. A V_{DD} connection defaults to tone mode operation and a GND connection defaults to pulse mode operation.

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed.. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the phone will be in pulse mode. Redial by the LND key or the MEM key will repeat the softswitch.

Output (PACIFIER TONE). Pin 7. In pulse mode, all valid key entries activate the pacifier tone. In tone mode, any non DTMF entry (FLASH, PROG, PAUSE, LND, HOLD, MEM, E1, E2 and E3), activates the pacifier tone. The pacifier tone provides audible feedback, confirming that key has been properly entered and accepted. It is a 500Hz square wave activated upon acceptance of valid key input after the 32ms debounce time. The square wave terminates after a maximum of 75ms or when the valid key is no longer present. The pacifier tone signal is simultaneously sent to earphone and the buzzer. The buzzer can be removed without affecting this function.

$\overline{\text{HKS}}$

Input. Pin 8. This is the hookswitch input to the one chip phone. This is a high impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 7. Figures 1 and 2 illustrate the timing for this pin.

GND

Pin 9 is the negative line terminal of the device. This is the voltage reference for all specifications.

RXOUT, GRX, RXIN

RXOUT (pin 10), GRX (pin 11) and RXIN (pin 12). The receive amplifier has one input RXIN and a non inverting output RXOUT. Amplification from RXIN to RXOUT is typically 31dB and it can be adjusted between 11dB and 41dB to suit the sensitivity of the earphone used. The amplification is proportional to the external resistor connected between GRX and RXOUT.

FUNCTION PIN DESCRIPTION (continued)

IREF

Pin 13. An external resistor of 3.6kOhm connected between IREF and GND will set the internal current level. Any change of this resistor value will influence the microphone gain, DTMF gain, earphone gain and sidetone.

V_{CC}

Pin 14, V_{CC} is the positive supply of the speech network. It is stabilized by a decoupling capacitor between V_{CC} and GND. The V_{CC} supply voltage may also be used to supply external peripheral circuits.

LED

Pin 15. The LED connected to this pin will start to blink when the HOLD key is pressed and will turn off if the HOLD key is pressed again. Otherwise, it will continue to blink at 1Hz frequency when the phone is on-hooked and then turn off when the parallel phone goes off-hook.

I_{LINE}

Pin 16. A recommended external resistor of 20ohm is connected between I_{LINE} and GND. Changing this resistor value will have influence on microphone gain, DTMF gain, sidetone, maximum output swing on LN and on the DC characteristics (especially in the low voltage region).

LN

Pin 17. LN is the positive line terminal of the device.

REG

Pin 18. The internal voltage regulator has to be decoupled by a capacitor from REG) to GND). The DC characteristics can be changed with an external resistor connected between LN and REG or between REG and I_{LINE} .

GTX, MIC–, MIC+

GTX (pin 19), MIC– (pin 20) and MIC+ (pin 21). The one chip phone has symmetrical microphone inputs. The amplification from microphone inputs to LN is 52dB and it can be adjusted between 44 and 52dB. The amplification is proportional to external resistor connected between GTX and REG.

GDTMF

Pin 22. When the DTMF input is enabled, the microphone inputs and the receive amplifier input will be muted and the dialing tone will be sent to the line. The voltage amplification from GDTMF to LN is 40dB. Final output level on LN can be adjusted via the external resistor connected between GDTMF and GND through a decoupling capacitor. A confidence tone is sent to the earphone during tone dialing. The attenuation of the confidence tone from LN to Vear is –32dB typically.

V_{DD}

Pin 23. V_{DD} is the positive supply for the dialing network and must meet the maximum and minimum voltage requirements.

DEVICE OPERATION

During on-hook all keypad inputs are high impedance internally and it requires very low current for memory retention. At anytime, Row and Column inputs assume opposite states at off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of approximately 40ms (measured from the initial key closure). Output tone duration is shown in Table 1.

The device allows manual dialing of an indefinite number of digits, but if more than 32 digits are dialed, it will "wrap around". That is, the extra digits beyond 32 will be stored at the beginning of LND buffer, and the first 32 digits will no longer be available for redial.

Table 2: DTMF Output Frequency

Key Input	Stadard Frequency	Actual Frequency	% Deviation
ROW 1	697	699.1	+0.31
ROW 2	770	766.2	–0.49
ROW 3	852	847.4	–0.54
ROW 4	941	948.0	+0.74
COL 1	1209	1215.9	+0.57
COL 2	1336	1331.7	–0.32
COL 3	1477	1471.9	–0.35

NORMAL DIALING

D1 D2 D3 ....etc

Normal dialing is straighforward, all keyboard entries will be stored in the buffer and signaled in succession.

PROGRAMMING AND REPORTORY DIALING

To program, enter the following:

PROG D1 D2 Dn MEM (location 0-9)

or

PROG D1 D2 Dn E1-E3

During programming, dialing is inhibited.

FUNCTION PIN DESCRIPTION (continued)

To dial a number from repertory memory ($\overline{HKS}$ must be low), enter the following:

MEM (Location 0-9) or E1-E3

To save the last number dialed, enter the following:

PROG MEM (location 0-9) or E1-E3

HOOK FLASH

D1 FLASH D2 ...etc

Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed break of 585ms. When a FLASH key is pressed, no further key inputs will be accepted until the hookflash function has been dialed. The key input following a FLASH will be stored as the initial digit of the new number, overwriting the number dialed before the FLASH, unless it is another FLASH.

FLASH key pressed immediately after hookswitch or LND will not clear the LND buffer unless digits are entered following the FLASH key.

Example:

FLASH

LND not cleared

LND FLASH

LND not cleared

LND FLASH D1 D2

LND buffer will contain D1, D2

PAUSE/LAST NUMBER DIALED

If the PAUSE/LND key is pressed right after off hook or FLASH key, it is considered as LND, if it is pressed after a digit, it will be considered as PAUSE.

LAST NUMBERED DIALED

OFF-HOOK PAUSE/LND or FLASH PAUSE/LND

Last number dialing is accomplished by entering the PAUSE/LND key.

PAUSE

OFF-HOOK D1 PAUSE/LND D2 ...etc

A pause may be entered into the dialed sequence at any point by keying in the special function key, PAUSE/LND. Pause inserts a 3.1 second delay into the dialing sequence. The total delay, including pre-digit and post-digit pauses is shown in Table 3.

Table 3: Special Function Delays

Each delay shown below represents the time required after the special function key is depressed until a new digit is dialed. The time is considered "FIRST" key if all previous inputs have been completely dialed. The time is considered "AUTO" if in redial, or if previous dialling is still in progress.

Function	First/Auto	Delay (seconds)	
		Pulse	Tone
SOFTSWITCH	FIRST AUTO	0.2 1.0	
PAUSE	FIRST AUTO	2.6 3.4	3.0 3 1

HOLD

When HOLD key is pressed during off hook, there are two options. The first option is to mute the phone (LED will blink) and the conversation can be resumed by pressing the HOLD key again. The second option is to mute the phone (LED will blink), on-hook the phone (LED will still blink at 1Hz frequency) and automatic switch off the phone when parallel phone is off-hook.

The HOLD function is disabled when the line current drops below 20mA.

SOFTSWITCH FUNCTION USING TONE/PULSE MODE SWITCH

When dialing in Pulse mode after off-hook, switching TONE/PULSE mode switch from Pulse to Tone will cause the device to change the signaling mode into tone signal and store the softswitch function in the LND memory for redial. To redial the softswitch function (mixed mode dialing) in the pulse mode after going on-hook and back to off-hook, you have to switch the TONE/PULSE mode switch back to pulse mode either before going on-hook or after off-hook or during on-hook.

Subsequent mode change from Tone to Pulse will change the signaling mode to pulse dialing sequence but this mode change will not be stored in .the LND memory.

When dialing in Tone mode after off-hook, a switching of TONE/PULSE mode Switch from Tone to Pulse will cause the device to change the signaling mode into pulse mode but this mode change will not be stored in the LND memory. When LND key is pressed in Tone mode after going off-hook, the device will output all tone signals.

A pacifier tone of 75ms is provided after 32ms debounce time when switching from Pulse to Tone mode.

Redial by the LND key will repeat the mixed dialing sequence in Pulse mode.

Figure 1: Tone Mode Timing

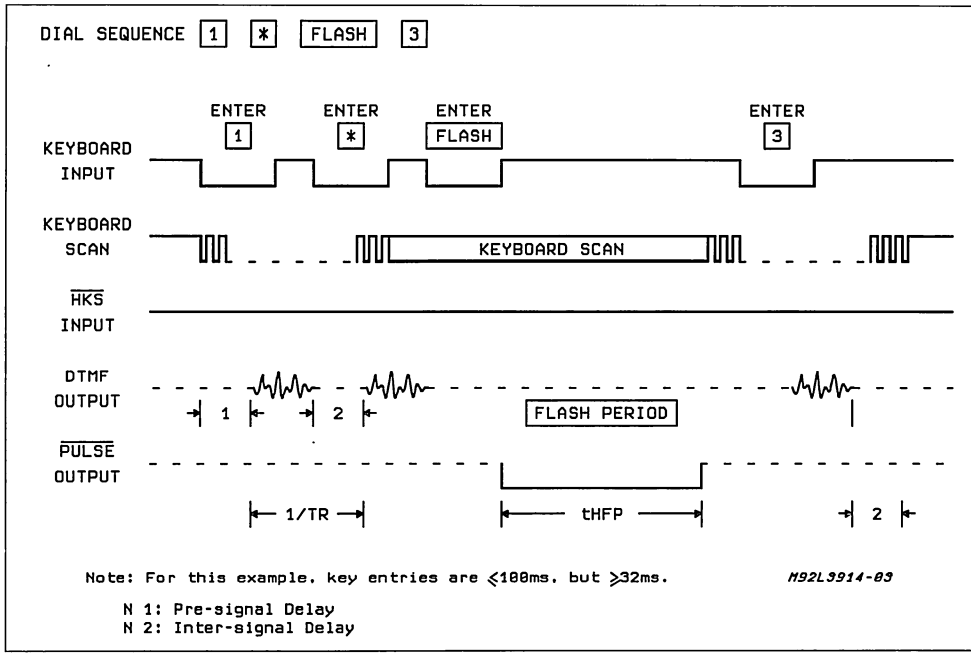
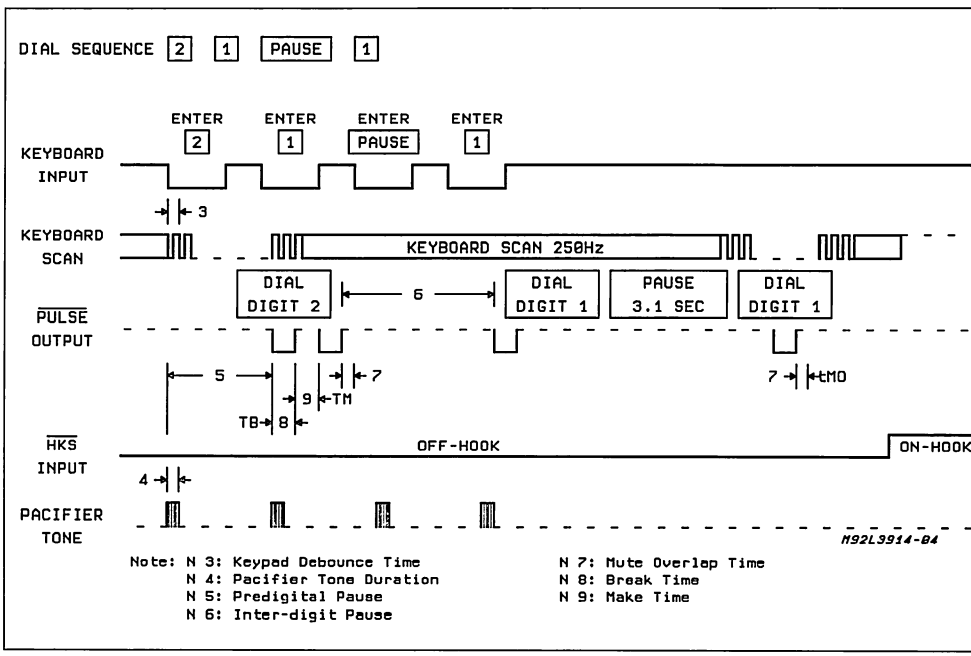


Figure 2: Pulse Mode Timing



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{LN}	Positive Line Voltage Continuous	12	V
I_{LN}	Line Current	140	mA
V_{DD}	Logic Voltage	7.0	V
V_I	Maximum Voltage on Any Pin	GND(-0.3) V_{DD}(+0.3)	V
T_{amb}	Operating Temperature Range	-40 to +125	°C
T_{stg}	Storage Temperature	-25 to 125	°C
P_{tot}	Total Power Dissipation	700	mW

ELECTRICAL CHARACTERISTICS (I_L = 10 to 140mA; V_{DD} = 4V; f = 1KHz; T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{LN}	Line Voltage	I_L = 4mA I_L = 15mA I_L = 120mA R_A = 68KΩ ; I_L = 15mA R_B = 39KΩ ; I_L = 15mA	 3.15 2.6 3.6	 3.50 3.2 4.1	2.50 3.85 7.0 3.7 4.6	V V V V V	3
V_{DD}	Logic Voltage)	TONE MODE PULSE MODE	2.50 2.20		6.00 6.00	V V	3
I_{DD}	Supply Current Into V_{DD}	TONE MODE @ V_{DD} = 4V PULSE MODE @ VDD = 4V		600 400		µA µA	3
I_{CC}	Supply Current Into V_{CC}	I_L = 15mA		1.30		mA	3
I_{LED}	Supply Current to HOLD LED	I_L = 15mA I_L = 120mA		1.5 1.5		mA mA	3
V_{MR}	Memory Retention Voltage		1.50			V	4
I_{MR}	Memory Retention Current				1.00	µA	4
I_S	Off-Hook Stand-by Current	V_{DD} = 4.0V		150	250	µA	3
I_{PL}	Pulse Output Sink Current	V_O = 0.5V	1.00	3.00		mA	3
I_{PO}	Pacifier Tone Sink/Source Current	V_O = 0.5V (Sink) V_O = 3.5V (Source)	1 0.6	3 1		mA mA	3
V_{IL}	HKS, Mode, Keyboard Inputs Low				0.3xV_{DD}	V	-
V_{IH}	HKS, Mode, Keyboard Inputs High		0.7xV_{DD}			V	-
G_{TX}	Transmit Gain	V_{mic} = 2mVrms I_L = 15mA; R_{GTX} = 68KΩ I_L = 60mA; R_{GTX} = 68KΩ	 50.0 44.5	 51.5 46.5	 53.0 48.5	 dB dB	6
A_{GTX}	Transmit Gain Variation with R_{GTX}	I_L = 15mA V_{mic} = 2mVrms R_{GTX} = 43KΩ R_{GTX} = 27KΩ	–8	 – 4 – 8	0	dB dB dB	6
D_{TX}	Transmit Distortion	I_L = 15mA; V_{LN} = 1Vrms			2	%	6
N_{TX}	Transmit Noise	I_L = 15mA; V_{mic} = 0V		–72		dBmp	6
Z_{MIC}	Microphone Input Impedance			64		KΩ	5
G_{DTMF}	DTMF Gain (Output @ LN)	I_L = 15mA ; R_{DTMF} = 2KΩ	38	40	42	dB	7
C_{DTMF}	Confidence Tone Level V_{ear}/V_{LN}		–34	–32	–30	dB	7

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{DTMF}	DTMF Level on the line High Frequency Group Low Frequency Group	R_{DTMF} = 2KΩ, C_{DTMF} = 22nF	 −8 −10	 −6 −8	 −4 −6	 dBm dBm	7
P_{EI}	Pre-emphasis		1.40	2	2.60	dB	7
DIS	DTMF Output Distortion			5	8	%	7
Z_{DTMF}	DTMF Att. pin Impedance			40		KΩ	
G_{RX}	Receive Gain	V_{inp} = 5mVrms; R_e = 300Ω R_{GRX} = 100KΩ I_L = 15mA I_L = 60mA	 29.5 24	 31.0 26	 32.5 28	 dB dB	8
A_{GRX}	Receive Gain Variation	I_L =15mA; R_e = 300Ω R_{GRX} = 10KΩ R_{GRX} = 300KΩ	−20	 −20 +10	+10	dB dB dB	8
D_{RX}	Reveive Output Distortion	I_L = 15mA; R_{GRX} = 100KΩ R_e = 150Ω; V_C = 0.25V_{rms} R_e = 300Ω; V_C = 0.45V_{rms} R_e = 450Ω; V_C = 0.55V_{rms}			 2 2 2	 % % %	8
N_{RX}	Receive Noise	$I_{L\,=\,15mA}$, R_L = 300Ω; R_{GRX} = 100KΩ; V_{INP} = 0V		200		μV	8
Z_{OUT}	Receive Output Impedance	I_L = 15mA		35		Ω	8
V_{PT}	Pacifier Tone Level on Earphone	I_L= 15mA; R_p = ∞ R_p = 430K	40 400	60 600	80 800	mVrms mVrms	8
KEYBOARD INTERFACE							
TKD	Keypad Debounce Time			32		ms	
FKS	Keypad Scan Frequency			250		Hz	
KRU	Keypad Pullup Resistance			100		KΩ	
KRD	Keypad Pulldown Resistance			500		Ω	
PULSE MODE							
TPT	Pacifier Tone Duration			75		ms	
FPT	Pacifier Tone Frequency			500		Hz	
PR	Pulse Rate			10		PPS	
TB	Break Time			60		ms	
TM	Make Time			40		ms	
IDP	Inter Digit Pause			820		ms	
PDP	Predigit Pause			50		ms	
TONE MODE							
RT	Tone Output Load			10		KΩ	
TRIS	Tone Output Rise Time				5	ms	
TR	Tone Signalling Rate			5		1/s	
TPSD	Pre Signal Delay		40			ms	
TISD	Inter Signal Delay			100		ms	
TDUR	Tone Output Duration			100		ms	
THD	Hold Mode Delay			400		ms	

Notes:
1. All inputs unloaded. Quiescent mode (oscillator off).
2. Pulse output sink current for V_{OUT} = 0.5V.
3. Pacifier tone sink current for V_{OUT} = 0.5V. Source current for V_{OUT} = 3.5V.
4 Memory retention voltage is the point where memory is guaranteed but circuit operation is not. Proper memory retention is guaranteed if either the minimum IMR is provided or the minimum VMR. The design does not have to provide both the minimum current and voltage simultaneously.

TEST CIRCUITS

Figure 3.

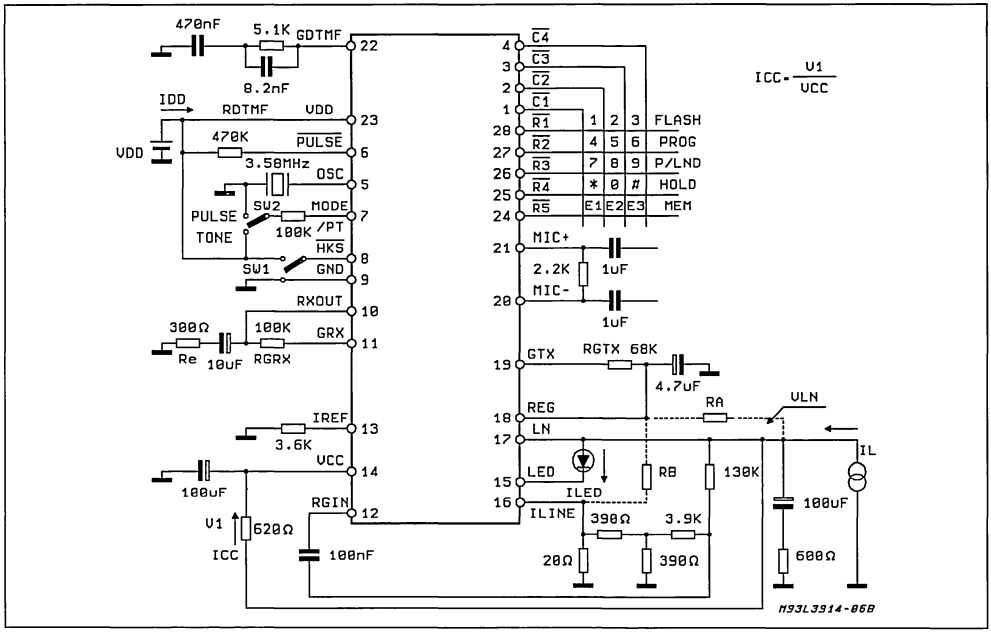
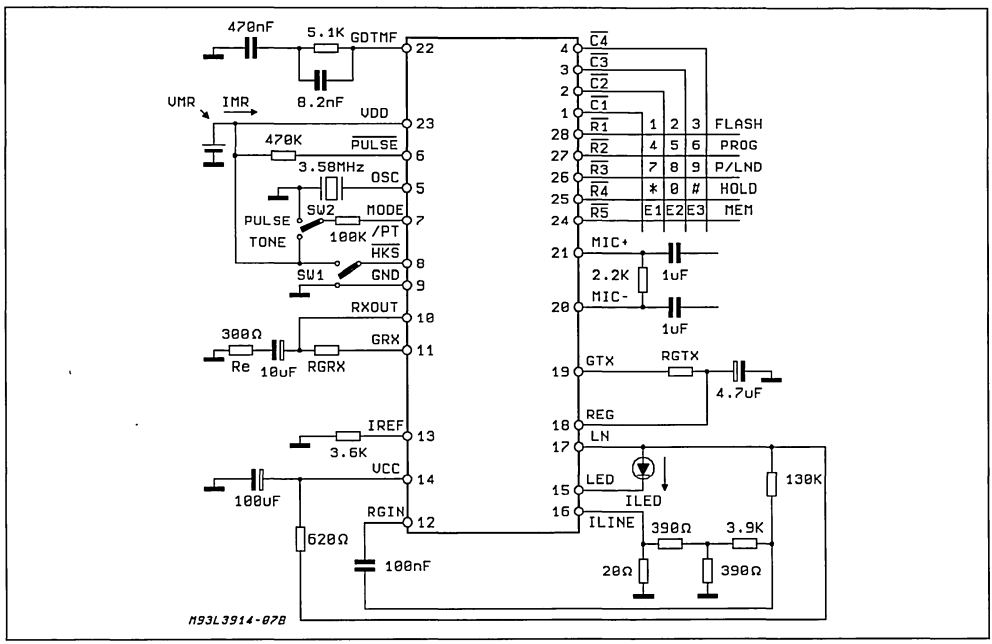


Figure 4.



TEST CIRCUITS(continued)
Figure 5.

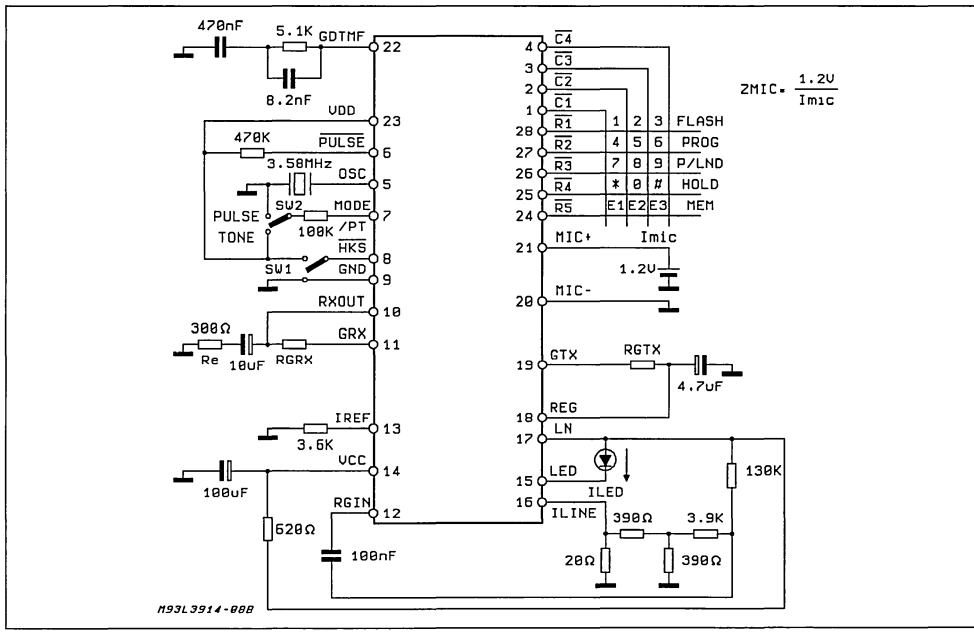
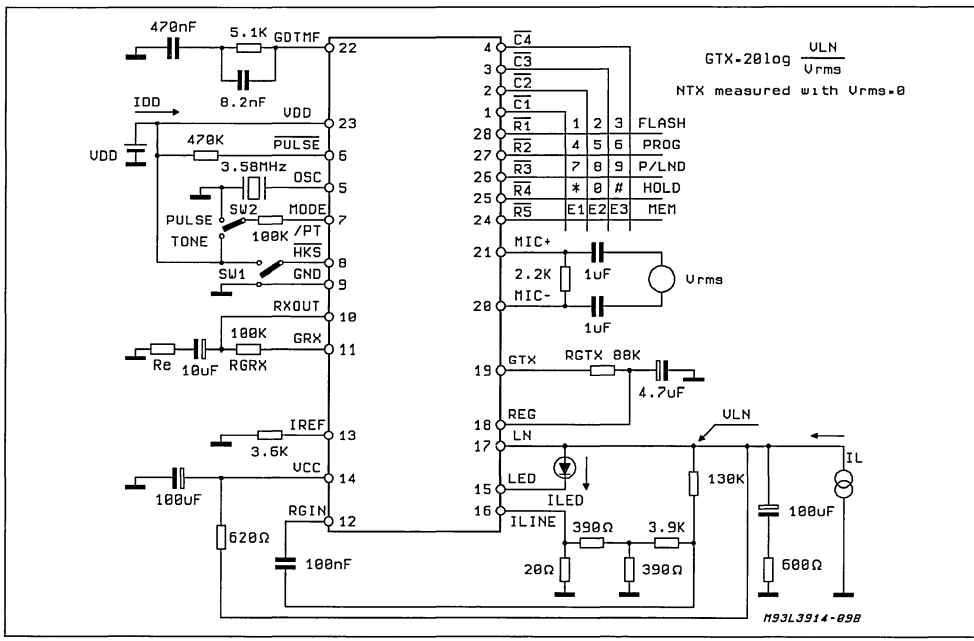


Figure 6.



TEST CIRCUITS(continued)
Figure 7.

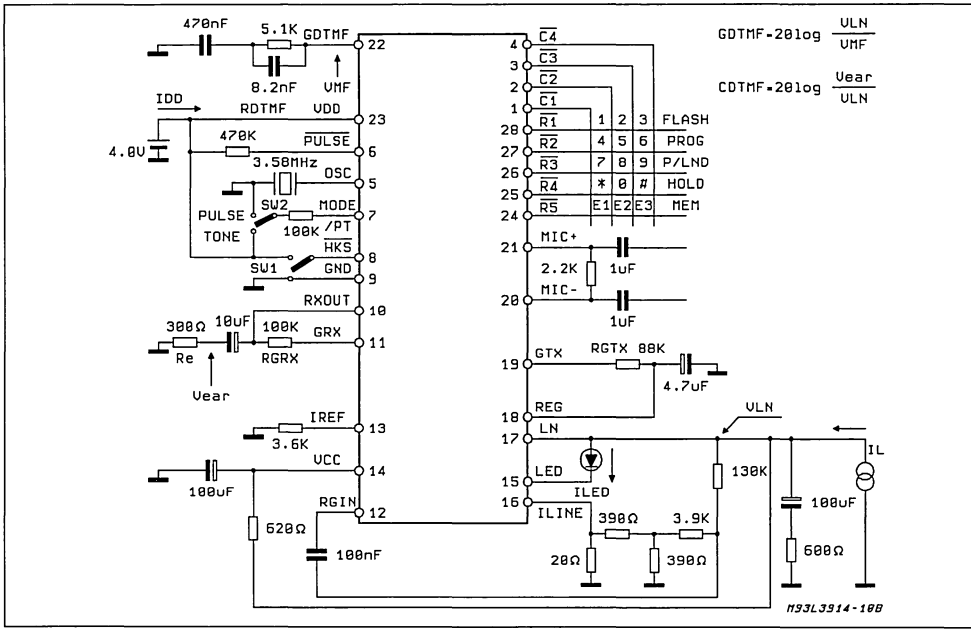


Figure 8.

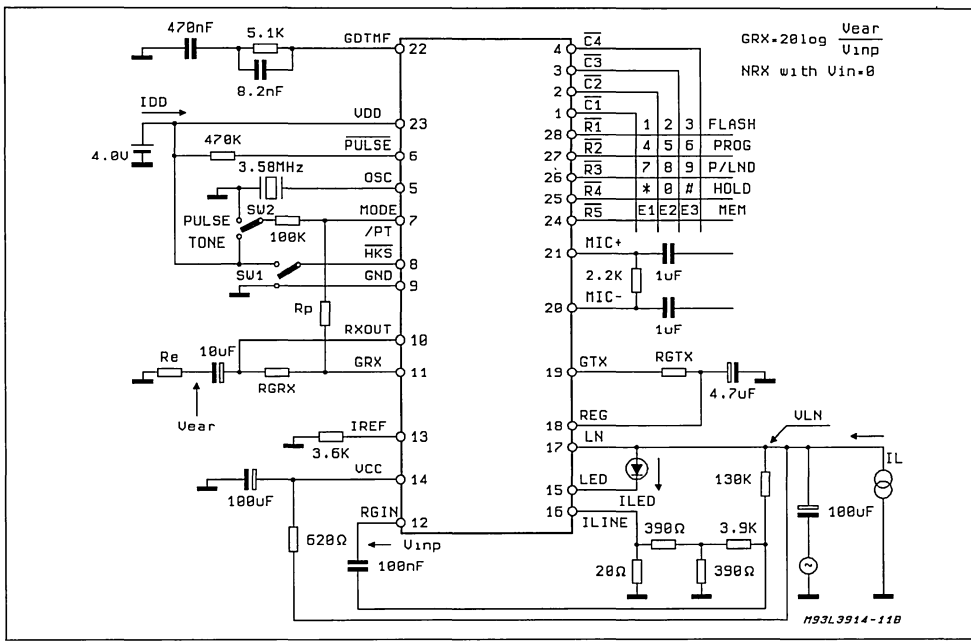
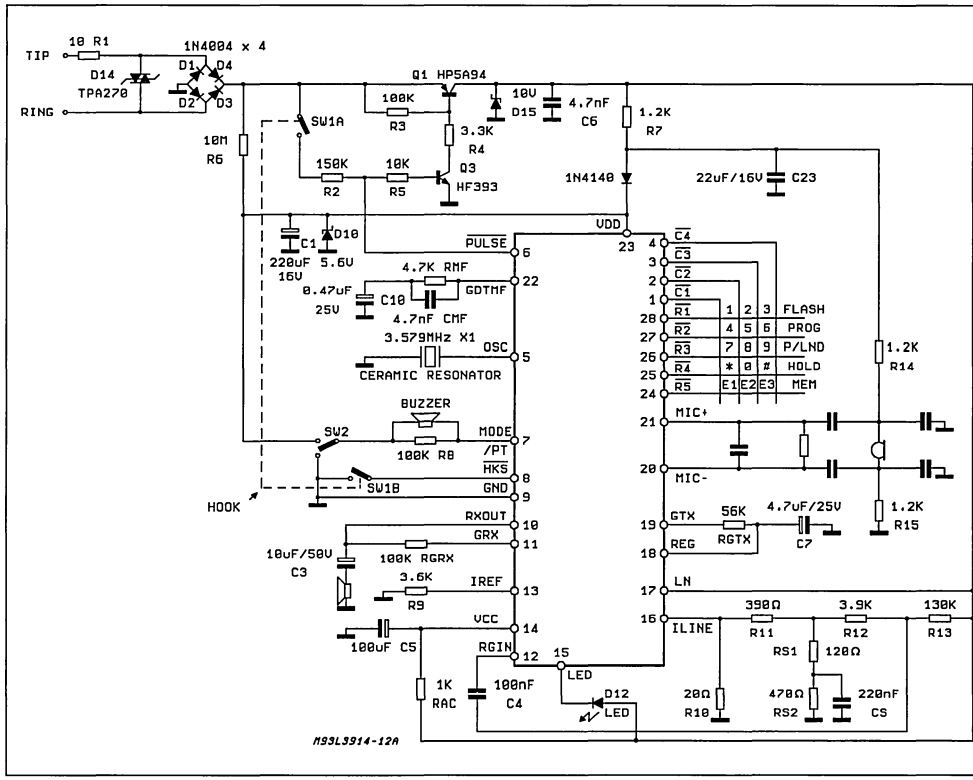


Figure 9: Typical Application Circuit.



LOW RANGE ONE CHIP PHONE (SPEECH AND DIALER)

ADVANCE DATA

Speech Circuit

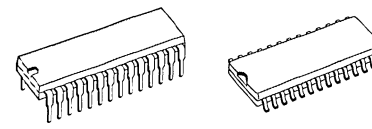
- 2 TO 4 WIRES CONVERSION
- PRESENT THE PROPER DC PATH FOR THE LINE CURRENT AND THE FLEXIBILITY TO ADJUST IT AND ALLOW PARALLEL PHONE OPERATION
- PROVIDES SUPPLY WITH LIMITED CURRENT FOR EXTERNAL CIRCUITRY
- SYMMETRICAL HIGH IMPEDANCE MICROPHONE INPUTS SUITABLE FOR DYNAMIC ELECTRET OR PIEZOELECTRIC TRANSDUCER
- ASYMMETRICAL EARPHONE OUTPUT SUITABLE FOR DYNAMIC TRANSDUCER
- LINE LOSS COMPENSATION
- INTERNAL MUTING TO DISABLE SPEECH DURING DIALING
- LIGHTED DIAL LED CONSUMING 25% OF LINE CURRENT

Dialer Circuit

- 32 DIGITS FOR LAST NUMBER REDIAL BUFFER
- 18 DIGITS FOR 13 MEMORY REDIAL
- ALLOW MIXED MODE DIALING IN EITHER TONE OR PULSE MODE
- PACIFIER TONE PROVIDES AUDIBLE INDICATION OF VALID KEY PRESSED IN A BUZZER OR/AND IN THE EARPHONE
- TIMED PABX PAUSE
- FLASH INITIATES TIMED BREAK
- CONTINUOUS TONE FOR EACH DIGIT UNTIL KEY RELEASE
- USES INEXPENSIVE 3.579545MHz CERAMIC RESONATOR
- POWERED FROM TELEPHONE LINE, LOW OPERATING VOLTAGE FOR LONG LOOP APPLICATION

DESCRIPTION

The device consists of the speech and the dialer. It provides the DC line interface circuit that terminates the telephone line, analog amplifier for speech transmission and necessary signals for either DTMF or loop disconnect (pulse) dialing.

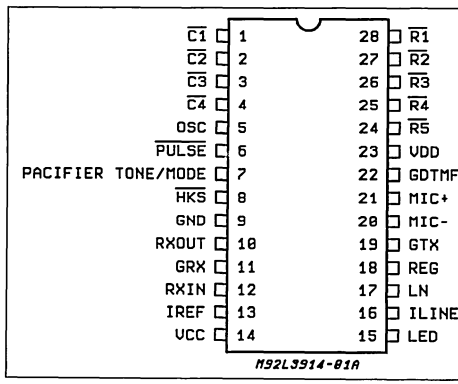


DIP28 **SO28**

ORDERING NUMBERS:

L3916N L3916D

PIN CONNECTION (Top view)



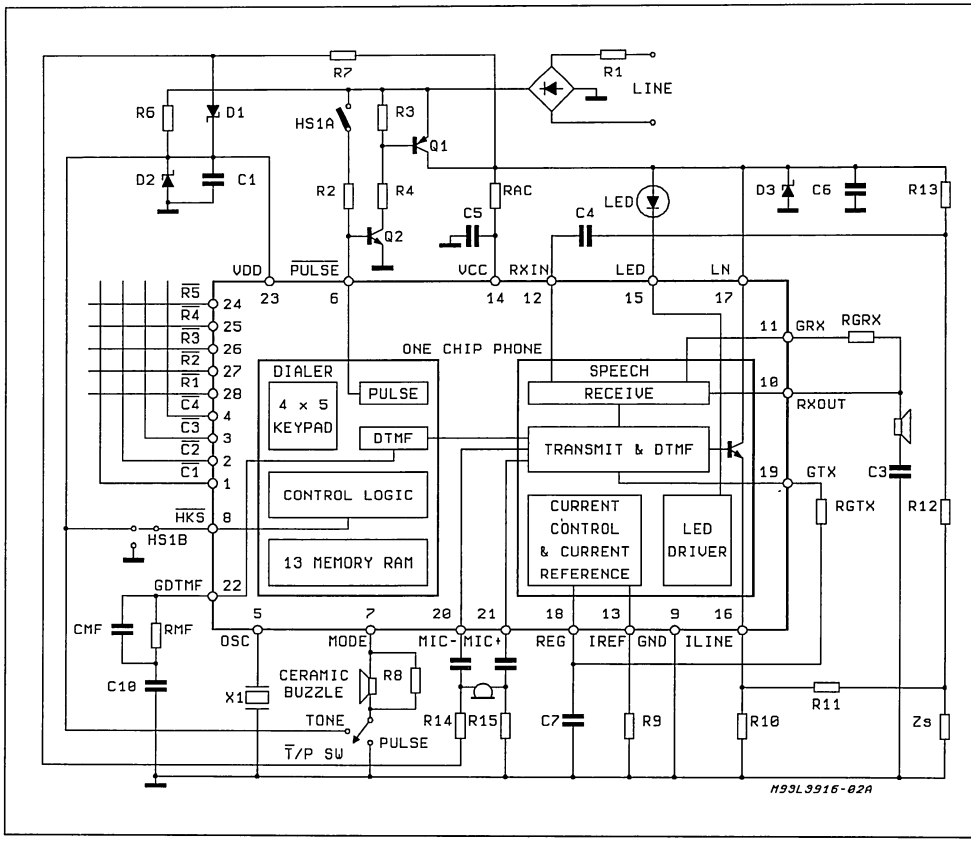
KEYPAD CONFIGURATION

1	2	3	FLASH
4	5	6	PROG
7	8	9	PAUSE /LND
* SOFT SWITCH	0	#	
E1	E2	E3	MEM

M93L3916-01

Note: PAUSE/LND:
PAUSE and LND functions are sharing the same key with different sequence. Hereafter, PAUSE and LND keys are referring to the same key.

BLOCK DIAGRAM



DESCRIPTION (continued)

When mated with a tone ringer, a complete telephone can be produced with just two ICs.

The DC line interface circuit develops its own line voltage across the device and it is adjustable by external resistor to suit different country's specification.

The speech network provides the two to four wires interface, electronic switching between dialing and speech and automatic gain control on transmit and receive.

The dialing network buffers up to 32 digits into the LND memory that can be later redialed with a single key input. Additionally, another 13 memories (including 3 emergency memories) of 18 digits memory is available. Users can store all 13 signalling keys and access several unique functions with single key entries. These functions include: Pause/Last Number Dialed (LND), Softswitch, Flash.

The FLASH key simulates a 585ms hook flash to transfer calls or to activate other special features provided by the PABX or central office.

The PAUSE key stores a timed pause in the number sequence. Redial is then delayed until an outside line can be accessed or some other activity occurs before normal signaling resumes.

A LND key input automatically redials the last number dialed.

FUNCTION PIN DESCRIPTION

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R5}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$

Keyboards inputs. Pins 1, 2, 3, 4, 24, 25, 26, 27, 28. The one chip phone interfaces with either the standard 2-of-9 with negative common or the single-contact (Form A) keyboard.

FUNCTION PIN DESCRIPTION (continued)

A valid keypad entry is either a single Row connected to a single Column or GND simultaneously presented to both a single Row and a single Colunm.
In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at logic level 1 (V_{DD}). Pulling one input low enables the on chip oscillator. Keyboard scanning then begins.

Scanning consists of Rows and Columns alternately switching high through on chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc) is ignored for a debounce period (TKD) of 32ms. At this time, the keyboard is sampled and if both the Row and Column information are valid, the information is buffered into the LND location. After scanning starts, the row and column inputs will assume opposite states.

In the tone mode, if two or more keys in the same row or if two or more keys in the same column are depressed a single tone will be output. The tone will corresponds to the row or column for which the two keys were pushed. This feature is for testing purposes, and single tone will not be redialed. Also in the tone mode, the output tone is continuous in the manual dialing as long as the key is pushed. The output tone duration follows the Table 1. When redialing in the tone mode, each DTMF output has 100ms duration, and the tone separation (inter signal delay) is 100ms.

Table 1: Output Tone Duration

Key-Push Time, T	Tone Output
T<= 32ms	No output, ignored by one chip phone.
32ms < = T < = 100ms + Tkd	100ms Duration
T > = 100ms + Tkd	Output Duration = T - Tkd

OSC

Output. Pin 5. Only one pin is needed to connect the ceramic resonator to the oscillator circuit. The other end of the resonator is connected to GND (pin 8). The nominal resonator frequency is 3.579545MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The ceramic resonator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ±0.25% is recommended

$\overline{\text{PULSE}}$

Output. Pin 6. This is an output consisting of an open drain N-Channel device. During on-hook, pulse output pin is in high impedance and once off-hooked, it will be pulled high by external resistor.

MODE/PACIFIER TONE

Input (MODE). Pin 7. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook (V_{DD}) to off-hook (GND), the default determines the signalling mode. A V_{DD} connection defaults to tone mode operation and a GND connection defaults to pulse mode operation.

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed.. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the phone will be in pulse mode. Redial by the LND key or the MEM key will repeat the softswitch.

Output (PACIFIER TONE). Pin 7. In pulse mode, all valid key entries activate the pacifier tone. In tone mode, any non DTMF entry (FLASH, PROG, PAUSE, LND, HOLD, MEM, E1, E2 and E3), activates the pacifier tone. The pacifier tone provides audible feedback, confirming. that key has been properly entered and accepted. It is a 500Hz square wave activated upon acceptance of valid key input after the 32ms debounce time. The square wave terminates after a maximum of 75ms or when the valid key is no longer present. The pacifier tone signal is simultaneously sent to earphone and the buzzer. The buzzer can be removed without affecting this function.

$\overline{\text{HKS}}$

Input. Pin 8. This is the hookswitch input to the one chip phone. This is a high impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 7. Figures 1 and 2 illustrate the timing for this pin.

GND

Pin 9 is the negative line terminal of the device. This is the voltage reference for all specifications.

RXOUT, GRX, RXIN

RXOUT (pin 10), GRX (pin 11) and RXIN (pin 12). The receive amplifier has one input RXIN and a non inverting output RXOUT. Amplification from RXIN to RXOUT is typically 31dB and it can be adjusted between 11dB and 41dB to suit the sensitivity of the earphone used. The amplification is proportional to the external resistor connected between GRX and RXOUT.

FUNCTION PIN DESCRIPTION (continued)

IREF

Pin 13. An external resistor of 3.6kOhm connected between IREF and GND will set the internal current level. Any change of this resistor value will influence the microphone gain, DTMF gain, earphone gain and sidetone.

V_{CC}

Pin 14, V_{CC} is the positive supply of the speech network. It is stabilized by a decoupling capacitor between V_{CC} and GND. The V_{CC} supply voltage may also be used to supply external peripheral circuits.

LED

Pin 15. Lighted dial indicator. The LED connected to this pin will light up when the telephone is off-hook and consuming 25% of the line current.

I_{LINE}

Pin 16. A recommended external resistor of 20ohm is connected between I_{LINE} and GND. Changing this resistor value will have influence on microphone gain, DTMF gain, sidetone, maximum output swing on LN and on the DC characteristics (especially in the low voltage region).

LN

Pin 17. LN is the positive line terminal of the device.

REG

Pin 18. The internal voltage regulator has to be decoupled by a capacitor from REG to GND. The DC characteristics can be changed with an external resistor connected between LN and REG or between REG and I_{LINE} .

GTX, MIC–, MIC+

GTX (pin 19), MIC– (pin 20) and MIC+ (pin 21). The one chip phone has symmetrical microphone inputs. The amplification from microphone inputs to LN is 52dB and it can be adjusted between 44 and 52dB. The amplification is proportional to external resistor connected between GTX and REG.

GDTMF

Pin 22. When the DTMF input is enabled, the microphone inputs and the receive amplifier input will be muted and the dialing tone will be sent to the line. The voltage amplification from GDTMF to LN is 40dB. Final ouput level on LN can be adjusted via the external resistor connected between GDTMF and GND through a decoupling capacitor. A confidence tone is sent to the earphone during tone dialing. The attenuation of the confidence tone from LN to Vear is –32dB typically.

V_{DD}

Pin 23. V_{DD} is the positive supply for the dialing network and must meet the maximum and minimum voltage requirements.

DEVICE OPERATION

During on-hook all keypad inputs are high impedance internally and it requires very low current for memory retention. At anytime, Row and Column inputs assume opposite states at off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of approximately 40ms (measured from the initial key closure). Output tone duration is shown in Table 1.

The device allows manual dialing of an indefinite number of digits, but if more than 32 digits are dialed, it will "wrap around". That is, the extra digits beyond 32 will be stored at the beginning of LND buffer, and the first 32 digits will no longer be available for redial.

Table 2: DTMF Output Frequency

Key Input	Stadard Frequency	Actual Frequency	% Deviation
ROW 1	697	699.1	+0.31
ROW 2	770	766.2	–0.49
ROW 3	852	847.4	–0.54
ROW 4	941	948.0	+0.74
COL 1	1209	1215.9	+0.57
COL 2	1336	1331.7	–0.32
COL 3	1477	1471.9	–0.35

NORMAL DIALING

D1 D2 D3 ....etc

Normal dialing is straighforward, all keyboard entries will be stored in the buffer and signaled in succession.

PROGRAMMING AND REPERTORY DIALING

To program, enter the following:

PROG D1 D2 D3. . . Dn MEM (Location 0-9)

or

PROG D1 D2. . . .Dn E1-E3

During programming, dialing is inhibited.

FUNCTION PIN DESCRIPTION (continued)

To dial a number from repertory memory ($\overline{HKS}$ must be low), enter the following:

MEM (Location 0-9) or E1-E3

To save the last number dialed, enter the following:

PROG MEM (location 0-9) or E1-E3

HOOK FLASH

D1 FLASH D2 ...etc

Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed break of 585ms. When a FLASH key is pressed, no further key inputs will be accepted until the hookflash function has been dialed. The key input following a FLASH will be stored as the initial digit of the new number, overwriting the number dialed before the FLASH, unless it is another FLASH.

FLASH key pressed immediately after hookswitch or LND will not clear the LND buffer unless digits are entered following the FLASH key.

Example:

FLASH

LND not cleared

LND FLASH

LND not cleared

LND FLASH D1 D2

LND buffer will contain D1, D2

PAUSE/LAST NUMBER DIALED

If the PAUSE/LND key is pressed right after off hook or FLASH key, it is considered as LND, if it is pressed after a digit, it will be considered as PAUSE.

LAST NUMBERED DIALED

OFF-HOOK PAUSE/LND or FLASH PAUSE/LND

Last number dialing is accomplished by entering the PAUSE/LND key.

PAUSE

OFF-HOOK D1 PAUSE/LND D2 ...etc

A pause may be entered into the dialed sequence at any point by keying in the special function key, PAUSE/LND. Pause inserts a 3.1 second delay into the dialing sequence. The total delay, including pre-digit and post-digit pauses is shown in Table 3.

Table 3: Special Function Delays

Each delay shown below represents the time required after the special function key is depressed until a new digit is dialed. The time is considered "FIRST" key if all previous inputs have been completely dialed. The time is considered "AUTO" if in redial, or if previous dialling is still in progress.

Function	First/Auto	Delay (seconds)	
		Pulse	Tone
SOFTSWITCH	FIRST	0.2	
	AUTO	1.0	
PAUSE	FIRST	2.6	3.0
	AUTO	3.4	3.1

SOFTSWITCH FUNCTION USING TONE/PULSE MODE SWITCH

When dialing in Pulse mode after off-hook, switching TONE/PULSE mode switch from Pulse to Tone will cause the device to change the signaling mode into tone signal and store the softswitch function in the LND memory for redial. To redial the softswitch function (mixed mode dialing) in the pulse mode after going on-hook and back to off-hook, you have to switch the TONE/PULSE mode switch back to pulse mode either before going on-hook or after off-hook or during on-hook.

Subsequent mode change from Tone to Pulse will change the signaling mode to pulse dialing sequence but this mode change will not be stored in .the LND memory.

When dialing in Tone mode after off-hook, a switching of TONE/PULSE mode Switch from Tone to Pulse will cause the device to change the signaling mode into pulse mode but this mode change will not be stored in the LND memory. When LND key is pressed in Tone mode after going off-hook, the device will output all tone signals.

A pacifier tone of 75ms is provided after 32ms debounce time when switching from Pulse to Tone mode.

Redial by the LND key will repeat the mixed dialing sequence in Pulse mode.

Figure 1: Tone Mode Timing

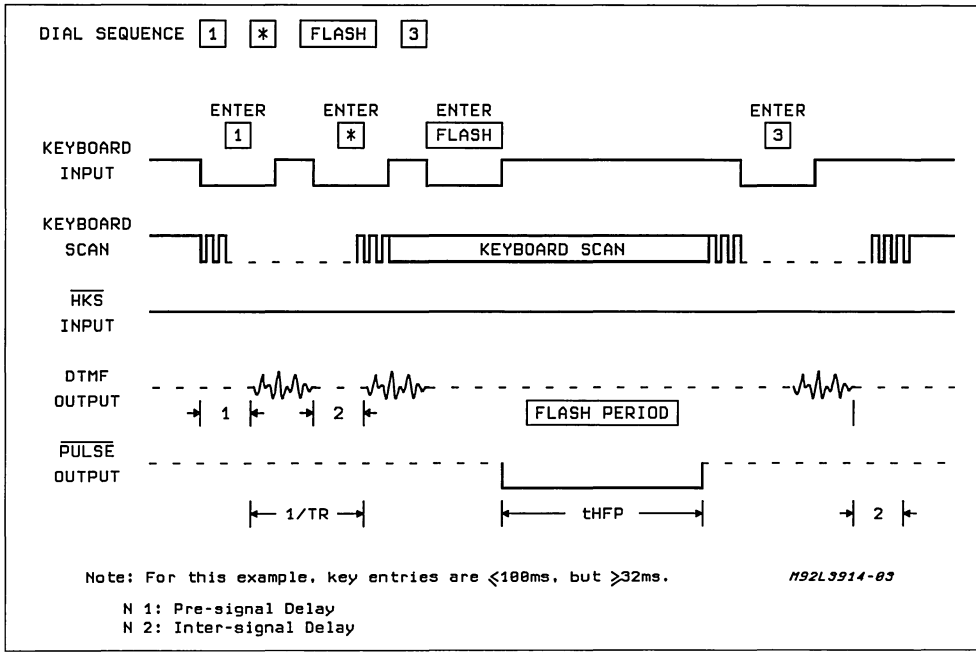
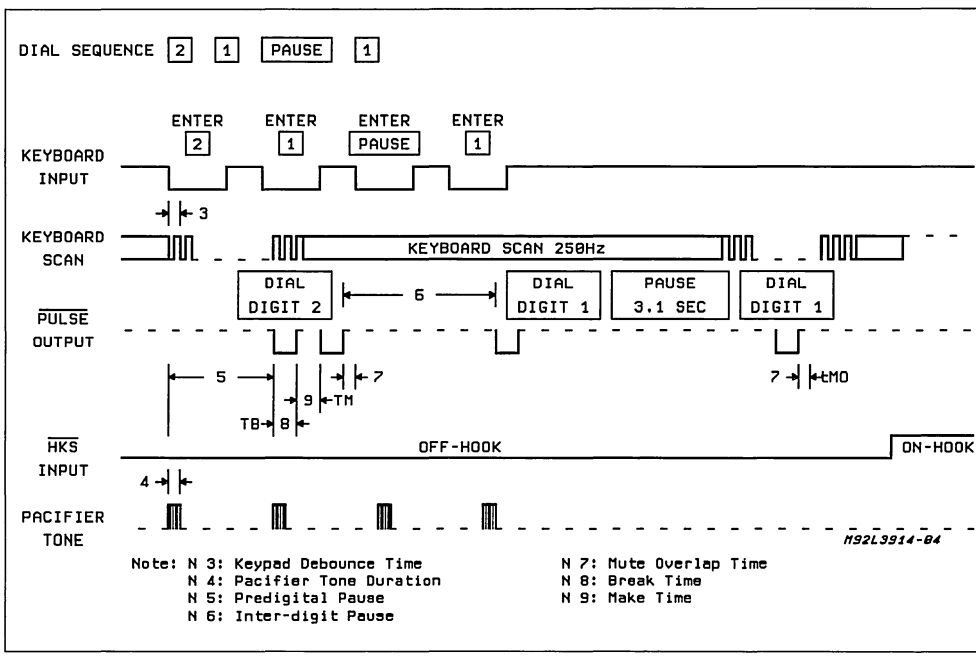


Figure 2: Pulse Mode Timing



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{LN}	Positive Line Voltage Continuous	12	V
I_{LN}	Line Current	140	mA
V_{DD}	Logic Voltage	7.0	V
V_I	Maximum Voltage on Any Pin	GND(-0.3) V_{DD}(+0.3)	V
T_{amb}	Operating Temperature Range	-40 to +125	°C
T_{stg}	Storage Temperature	-25 to 125	°C
P_{tot}	Total Power Dissipation	700	mW

ELECTRICAL CHARACTERISTICS (I_L = 10 to 140mA; f = 1KHz; T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{LN}	Line Voltage	I_L = 4mA			2.50	V	3
		I_L = 15mA	3.15	3.50	3.85	V	
		I_L = 120mA			7.0	V	
		R_A = 68KΩ I_L = 15mA	2.6	3.2	3.7	V	
		R_B = 39KΩ I_L = 15mA	3.6	4.1	4.6	V	
V_{DD}	Logic Voltage)	TONE MODE	2.50		6.00	V	3
		PULSE MODE	2.20		6.00	V	
I_{DD}	Supply Current Into V_{DD}	TONE MODE @ V_{DD} = 4V		600		µA	3
		PULSE MODE @ V_{DD} = 4V		400		µA	
I_{CC}	Supply Current Into V_{CC}	I_L = 15mA		1.30		mA	3
I_{LED}	Supply Current to LED	I_L = 15mA		4		mA	3
		I_L = 120mA		30		mA	
V_{MR}	Memory Retention Voltage		1.50			V	4
I_{MR}	Memory Retention Current				1.00	µA	4
I_S	Off-Hook Stand-by Current	V_{DD} = 4.0V		150	250	µA	3
I_{PL}	Pulse Output Sink Current	V_O = 0.5V	1.00	3.00		mA	3
I_{PO}	Pacifier Tone Sink/Source Current	V_O = 0.5V (Sink)	1	3		mA	3
		V_O = 3.5V (Source)	0.6	1.0		mA	
V_{IL}	HKS, Mode, Keyboard Inputs Low				0.3xV_{DD}	V	-
V_{IH}	HKS, Mode, Keyboard Inputs High		0.7xV_{DD}			V	-
G_{TX}	Transmit Gain	V_{mic} = 2mVrms					6
		I_L = 15mA R_{GTX} = 68KΩ	50.0	51.5	53.0	dB	
		I_L = 60mA; R_{GTX} = 68KΩ	44.5	46.5	48.5	dB	
A_{GTX}	Transmit Gain Variation with R_{GTX}	I_L = 15mA	–8		0	dB	6
		V_{mic} = 2mVrms					
		R_{GTX} = 43KΩ		– 4		dB	
		R_{GTX} = 27KΩ		– 8		dB	
D_{TX}	Transmit Distortion	I_L = 15mA V_{LN} = 1Vrms			2	%	6
N_{TX}	Transmit Noise	I_L = 15mA; V_{mic} = 0V		–72		dBmp	6
Z_{MIC}	Microphone Input Impedance			65		KΩ	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
G_{DTMF}	DTMF Gain	I_L = 15mA, R_{DTMF} = 2KΩ	38	40	42	dB	7
C_{DTMF}	Confidence Tone Level V_{ear}/V_{LN}		–34	–32	–30	dB	7
V_{DTMF}	DTMF Level on the line High Frequency Group Low Frequency Group	R_{DTMF} = 2KΩ, C_{DTMF} = 22nF	 –8 –10	 –6 –8	 –4 –6	 dBm dBm	7
P_{EI}	Pre-emphasis		1.40	2	2.60	dB	7
DIS	DTMF Output Distortion			5	8	%	7
Z_{DTMF}	DTMF Att. pin Impedance			40.0		KΩ	
G_{RX}	Receive Gain	V_{inp} = 5mVrms, R_e = 300Ω R_{GRX} = 100KΩ I_L = 15mA I_L = 60mA	 29.5 24	 31.0 26	 32.5 28	 dB dB	8
A_{GRX}	Receive Gain Variation	I_L =15mA, R_e = 300Ω R_{GRX} = 10KΩ R_{GRX} = 300KΩ	–20	 –20 +10	+10	dB dB dB	8
D_{RX}	Reveive Distortion	I_L = 15mA; R_{GRX} = 100KΩ Re = 150Ω, V_C = 0.25V_{rms} R_e = 300Ω, V_C = 0.45V_{rms} R_e = 450Ω, V_C = 0.55V_{rms}			 2 2 2	 % % %	8
N_{RX}	Receive Noise	I_L = 15mA R_L = 300Ω R_{GRX} = 100KΩ V_{inp} = 0V		200		µV	8
Z_{OUT}	Receive Output Impedance	I_L = 15mA		35		Ω	8
V_{PT}	Pacifier Tone Level on Earphone	I_L= 15mA; R_p = ∞ R_p = 430K	40 400	60 600	80 800	mVrms mVrms	8
KEYBOARD INTERFACE							
TKD	Keypad Debounce Time			32		ms	
FKS	Keypad Scan Frequency			250		Hz	
KRU	Keypad Pullup Resistance			100		KΩ	
KRD	Keypad Pulldown Resistance			500		Ω	
PULSE MODE							
TPT	Pacifier Tone Duration			75		ms	
FPT	Pacifier Tone Frequency			500		Hz	
PR	Pulse Rate			10		PPS	
TB	Break Time			60		ms	
TM	Make Time			40		ms	
IDP	Inter Digit Pause			820		ms	
PDP	Predigit Pause			50		ms	
TONE MODE							
RT	Tone Output Load			10		KΩ	
TRIS	Tone Output Rise Time				5	ms	
TR	Tone Signalling Rate			5		1/s	
TPSD	Pre Signal Delay		40			ms	
TISD	Inter Signal Delay			100		ms	
TDUR	Tone Output Duration			100		ms	

Notes:
1. All inputs unloaded. Quiescent mode (oscillator off).
2. Pulse output sink current for V_{OUT} = 0.5V.
3. Pacifier tone sink current for V_{OUT} = 0.5V. Source current for V_{OUT} = 3.5V.
4. Memory retention voltage is the point where memory is guaranteed but circuit operation is not. Proper memory retention is guaranteed if either the minimum IMR is provided or the minimum VMR. The design does not have to provide both the minimum current and voltage simultaneously.

TEST CIRCUITS

Figure 3.

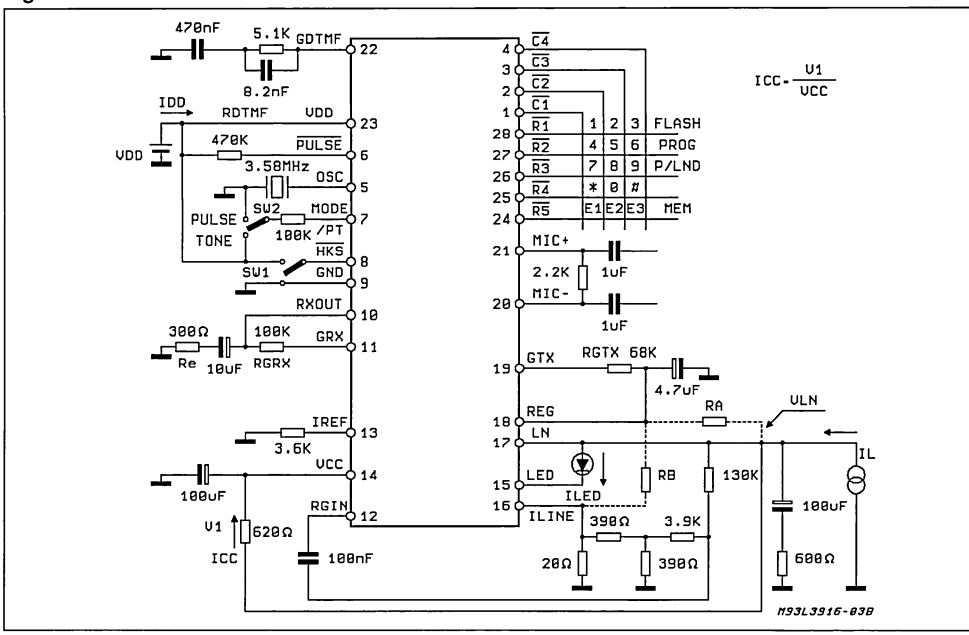
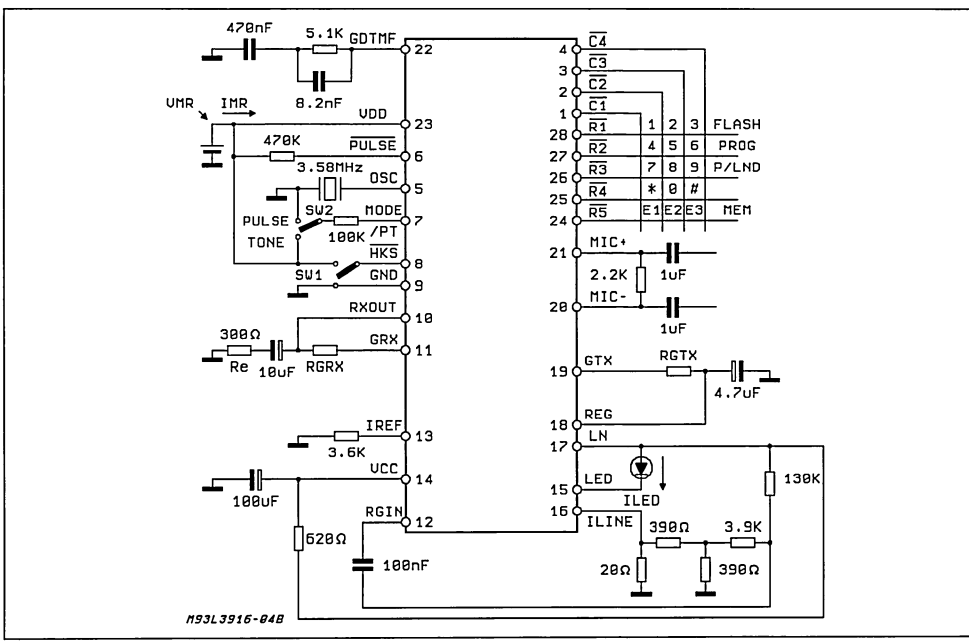


Figure 4.



TEST CIRCUITS(continued)
Figure 5.

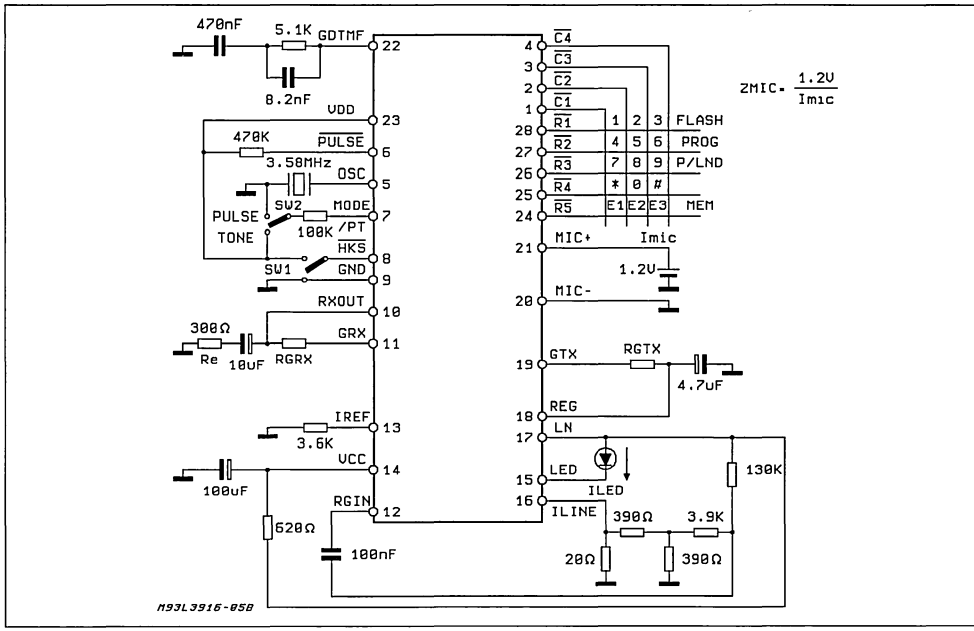
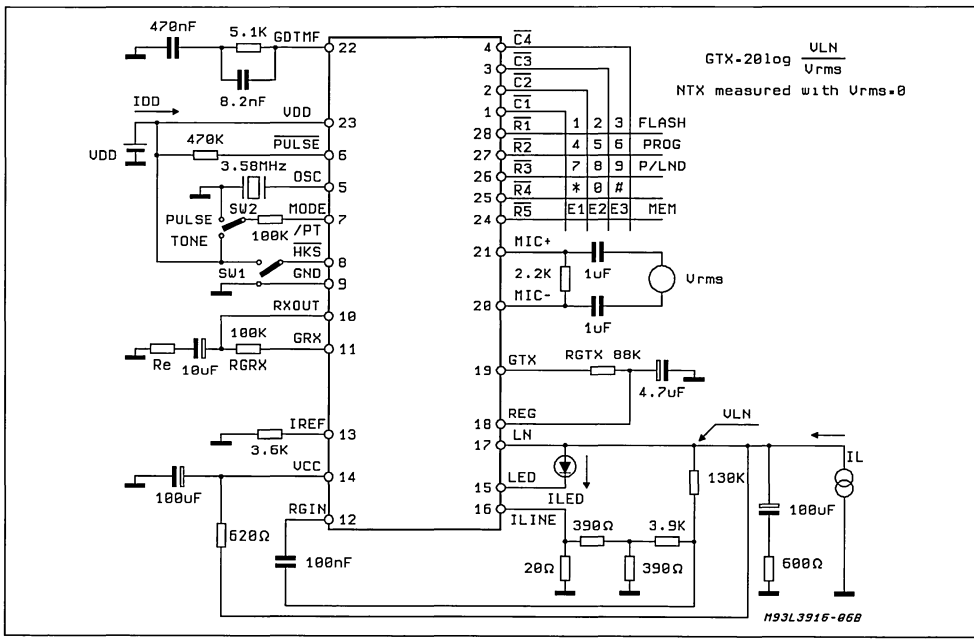


Figure 6.



TEST CIRCUITS(continued)
Figure 7.

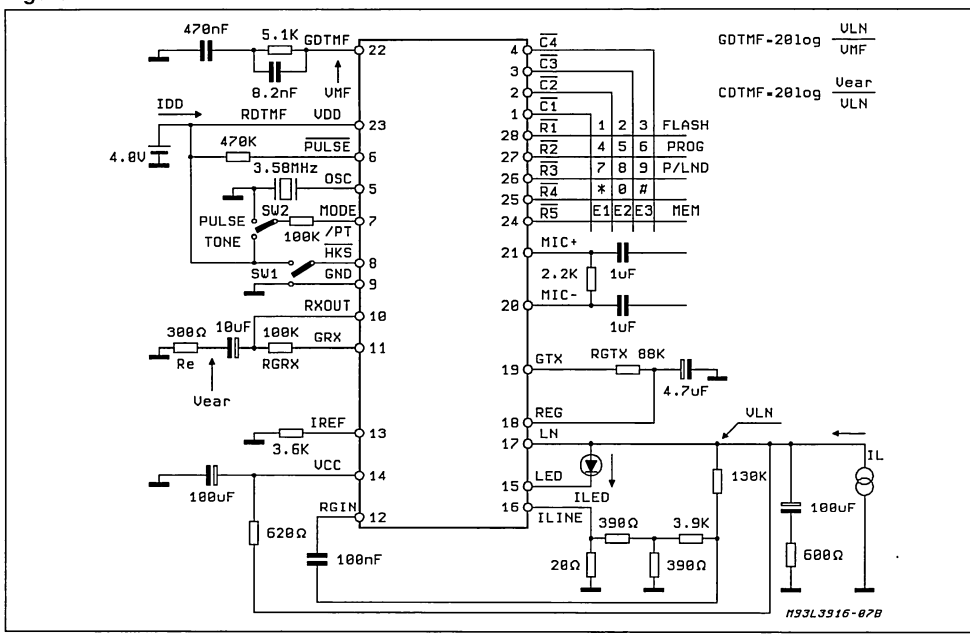


Figure 8.

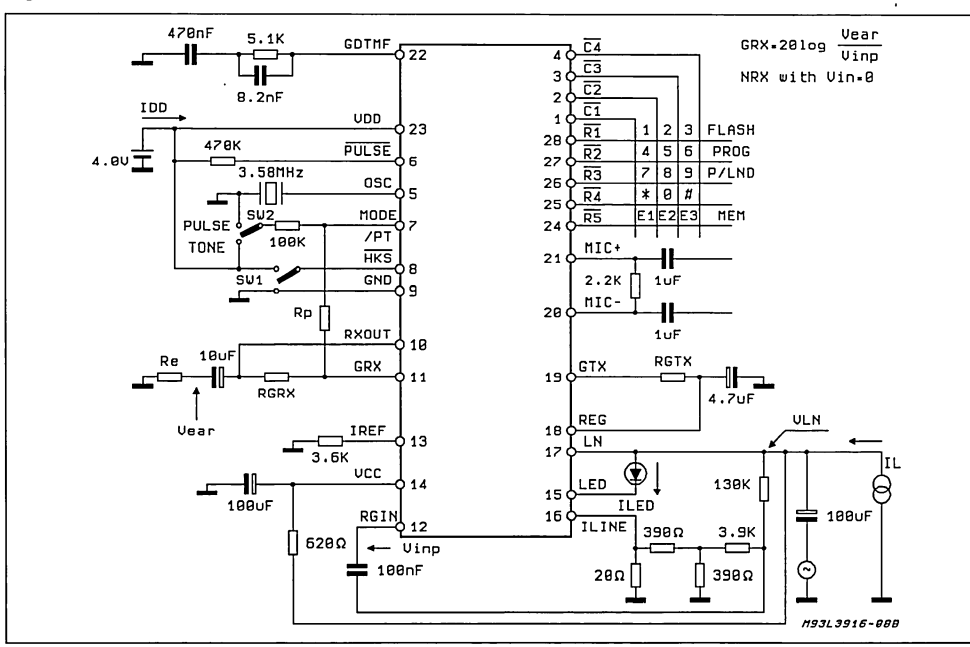
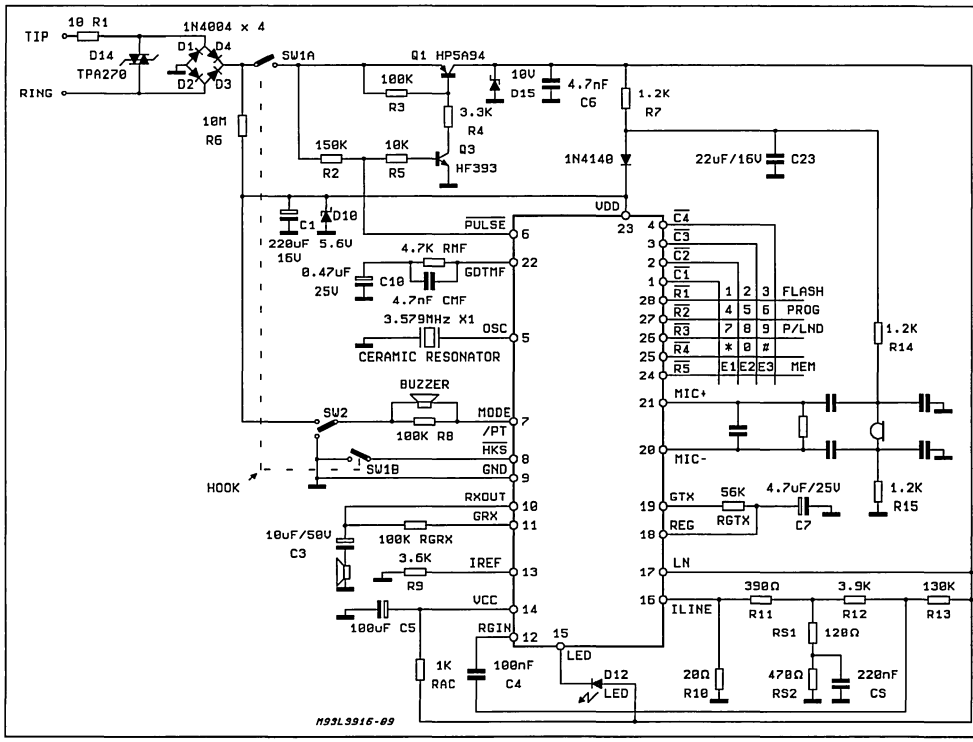
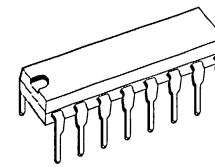


Figure 9: Typical Application Circuit.



TELEPHONE SPEECH CIRCUIT WITH MULTIFREQUENCY TONE GENERATOR INTERFACE

- PRESENTS THE PROPER DC PATH FOR THE LINE CURRENT
- HANDLES THE VOICE SIGNAL, PERFORMING THE 2/4 WIRES INTERFACE AND CHANGING THE GAIN ON BOTH SENDING AND RECEIVING AMPLIFIERS TO COMPENSATE FOR LINE ATTENUATION BY SENSING THE LINE LENGTH THROUGH THE LINE CURRENT
- ACTS AS LINEAR INTERFACE FOR MF, SUPPLYING A STABILIZED TO THE DIGITAL CHIP AND DELIVERING TO THE LINE THE MF TONE GENERATED BY THE DIALER



DIP16

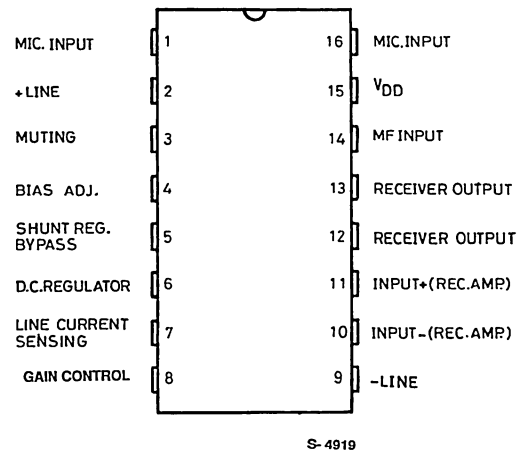
ORDERING NUMBER : LS256B

DESCRIPTION

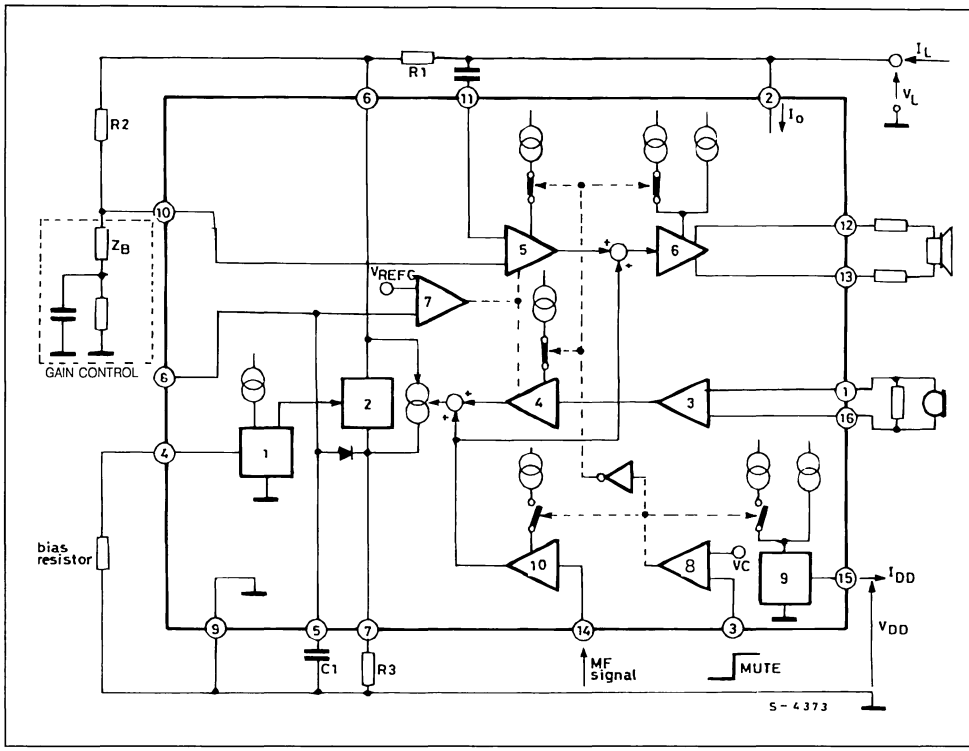
The LS256 is a monolithic integrated circuit in 16-lead dual in-line plastic package to replace the hybrid circuit in telephone set. It works with the same type of transdurcers for both transmitter and receiver (typically piezoceramic capsules, but the device can work also with dynamic ones). Many of its electrical characteristics can be controlled by means of external components to meet different specifications.

In addition to the speech operation, the LS256 acts as an interface for the MF tone signal.

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_L	Line Voltage (3ms pulse duration)	22	V
I_L	Forward Line Current	150	mA
I_L	Reverse Line Current	– 150	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70°C	1	W
T_{op}	Operating Temperature	– 45 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 65 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

TEST CIRCUITS

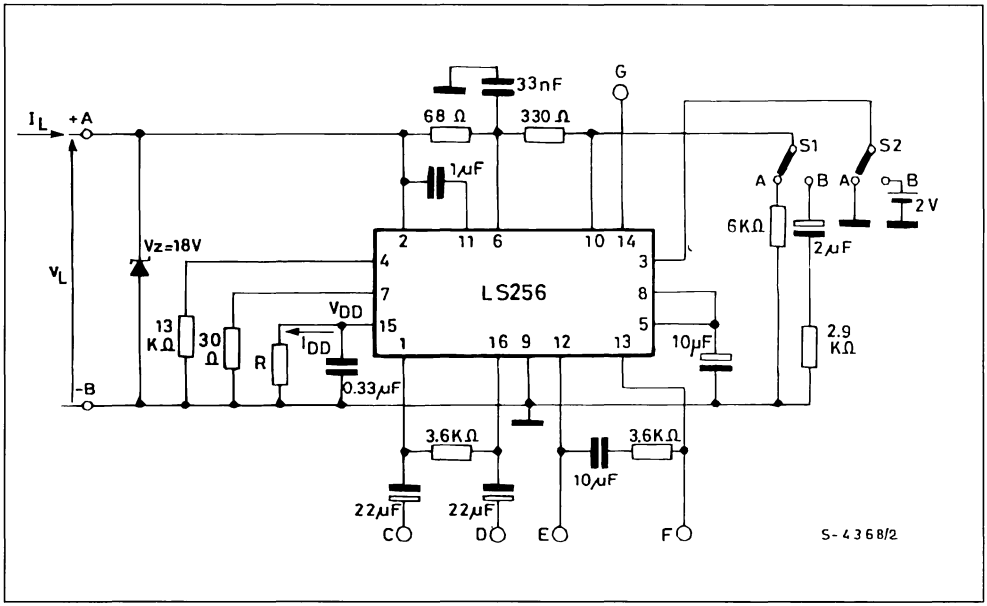
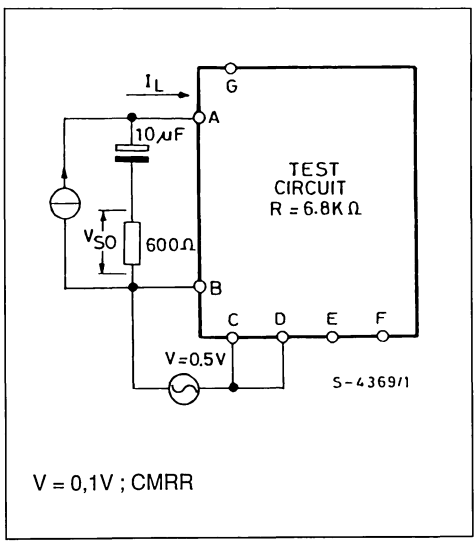
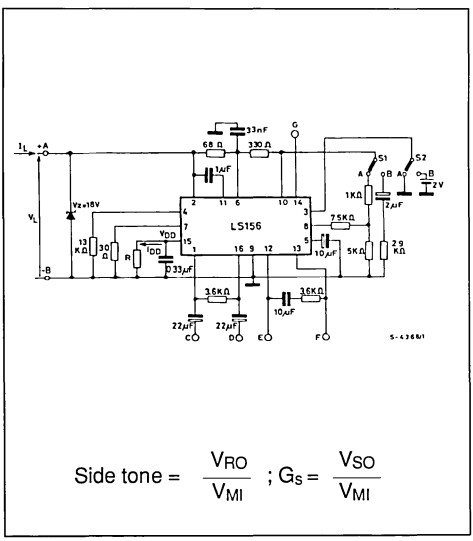


Figure 1.



V = 0,1V ; CMRR

Figure 2.



Side tone = $\frac{V_{RO}}{V_{MI}}$; $G_S = \frac{V_{SO}}{V_{MI}}$

Figure 3.

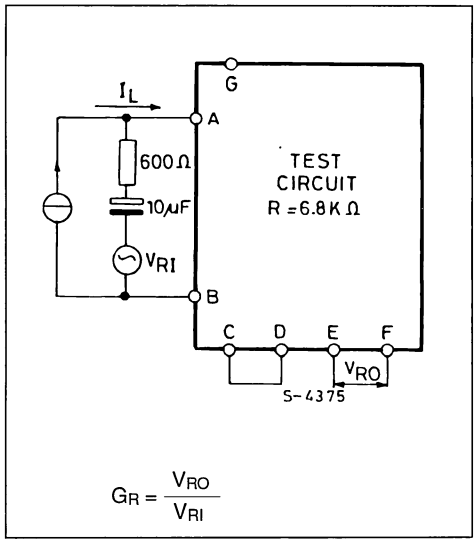
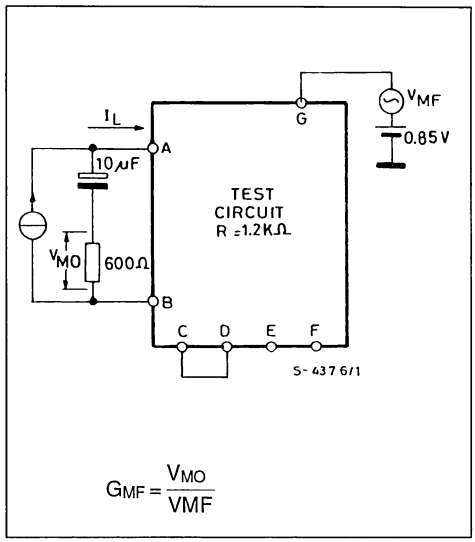


Figure 4.



ELECTRICAL CHARACTERISTICS (refer to the test circuits, S1, S2 in (a), T_{amb} = – 25 to + 50°C, f = 200 to 3400Hz, unless otherwise specified)

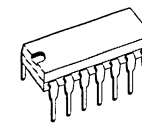
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION							
V_L	Line Voltage	T_{amb} = 25°C I_L = 12mA I_L = 20mA I_L = 80mA	3.9		4.7 5.5 12.2	V	
CMRR	Common Mode Rejection	f = 1kHz, I_L = 12 to 80mA	50			dB	1
G_S	Sending Gain	T_{amb} = 25°C, f = 1kHz I_L = 52mA V_{MI} = 2mV I_L = 25mA	44 48	45 49	46 50	dB	2
	Sending Gain Flatness	V_{MI} = 2mV, f_{ref} = 1kHz I_L = 12 to 80mA			± 1	dB	2
	Sending Distortion	f = 1kHz V_{SO} = 1V I_L = 16 to 80mA V_{SO} = 1.3V			2 10	%	2
	Sending Noise	V_{MI} = 0V; I_L = 40mA; S1 in (b)			–68.5	dBmp	2
	Microphone Input Impedance Pin 1-16	V_{MI} = 2mV, I_L = 12 to 80mA	40			kΩ	
	Sending Loss in MF Operation	V_{MI} = 2mV I_L = 52mA S_2 in (b) I_L = 25mA	– 30 – 30			dB	2
G_R	Receiving Gain	V_{RI} = 0.3V, f = 1kHz, T_{amb} = 25°C I_L = 52mA I_L = 25mA	 2.5 7	 3.5 8	 4.5 9	dB	3
	Receiving Gain Flatness	V_{RI} = 0.3V, f_{ref} = 1kHz I_L = 12 to 80mA			± 1	dB	3
	Receiving Distortion	f = 1kHz I_L = 12mA V_{RO} = 1.6V I_L = 12mA V_{RO} = 1.9V I_L = 50mA V_{RO} = 1.8V I_L = 50mA V_{RO} = 2.1V			2 10 2 10	%	3
	Receiving Noise	V_{RI} = 0V; I_L = 12 to 80mA; S1 in (b)		100		μV	3
	Receiver Output Impedance Pin 12-13	V_{RO} = 50mV, I_L = 40mA			100	Ω	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION (continued)							
G_R	Sidetone	F = 1kHz, T_{amb} = 25°C, S_1 in (b) I_L = 52mA I_L = 25mA			 36 36	dB	2
Z_{ML}	Line Matching Impedance	V_{RI} = 0.3V, f = 1kHz I_L = 12 to 80mA	500	600	700	Ω	
MULTIFREQUENCY SYNTHESIZER INTERFACE							
V_{DD}	MF Supply Voltage (standby and operation)	I_L = 12 to 80mA	2.4	2.5		V	
I_{DD}	MF Supply Current Stand by Operation	 I_L = 12 to 80mA I_L = 12 to 80mA ; S_2 in (b)	 0.5 2			 mA mA	
	MF Amplifier Gain	I_L = 12 to 80mA, f_{MF} in = 1kHz V_{MF} in = 80mV	15		17	dB	4
V_I	DC Input Voltage Level (pin 14)	$V_{M\ Fin}$ = 80mV		$3V_{DD}$		V	
R_I	Input Impedance (pin 14)	$V_{M\ Fin}$ = 80mV	40			kΩ	
d	Distortion	$V_{M\ Fin}$ = 110mV I_L = 12 to 80mA			2	%	4
	Starting Delay Time	I_L = 12 to 80mA			5	ms	
	Muting Threshold Voltage (pin 3)	Speech Operation			1	V	
		MF Operation	1.6			V	
	Muting Stand by Current (pin 3)	I_L = 12 to 80mA			− 10	µA	
	Muting Operating Current (pin 3)	I_L = 12 to 80mA, S_2 in (b)			+ 10	µA	

TELEPHONE SPEECH CIRCUITS

- 2/4 WIRE INTERFACE
- OPERATES DOWN TO 4 mA
- 3.5 V_{pp} DYNAMIC IN SENDING AT 25 mA



DIP14

ORDERING NUMBER : LS285AB1

DESCRIPTION

The LS285 is monolithic integrated circuits for replacement of the hybrid circuit (2-4 wire interface) in conventional telephones interfacing the two transducers to the line and providing a controlled amount of sidetone.

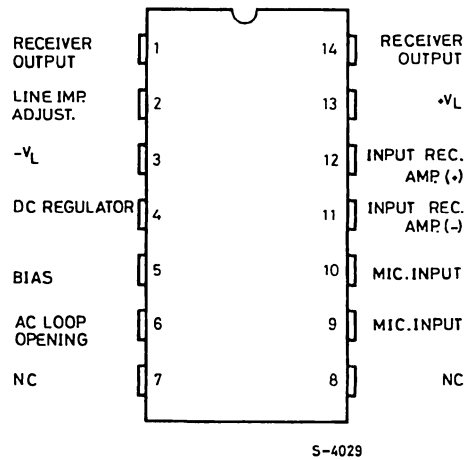
The same type of transducer can be used for both transmitter and receiver, usually a 350 Ω dynamic type.

By sensing the line current, LS285 adjusts the gain in both directions to compensate for line attenuation.

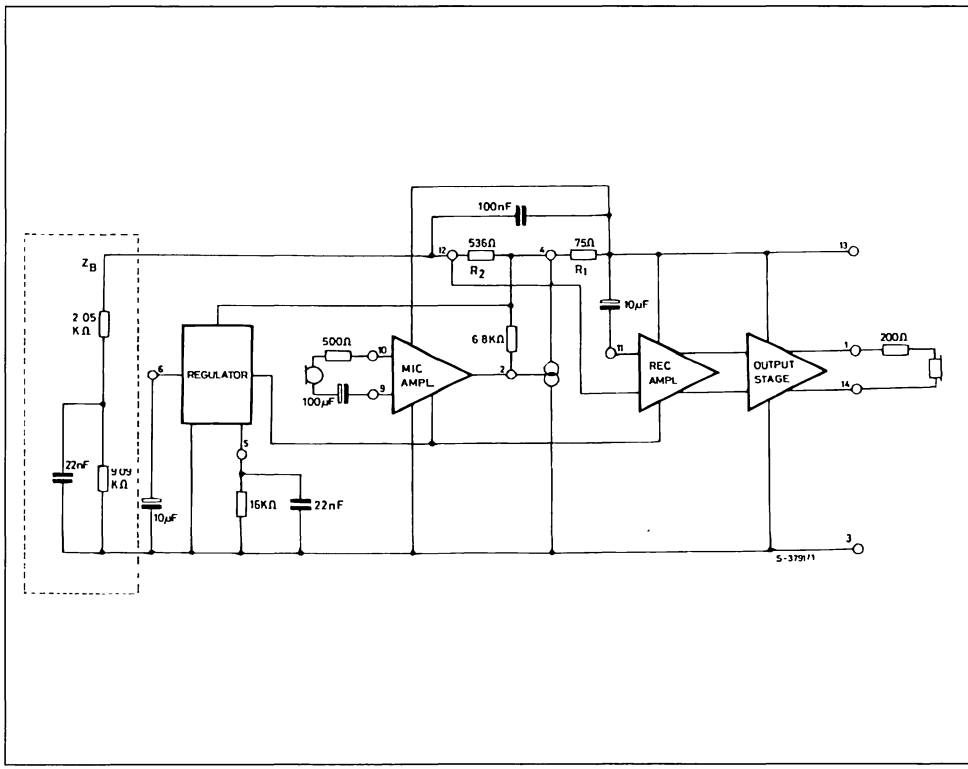
Output impedance can be matched to the line, independent of transducer impedance.

The LS285 is packaged in a 14 lead dual in–line plastic package.

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_L	Line Voltage (3 ms pulse duration)	22	V
I_L	Forward Current	120	mA
I_L	Reverse Current	– 150	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1	W
T_{stg}	Storage and Junction Temperature	– 55 to 150	°C
T_{op}	Operating Temperature	– 40 to 70	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max<0>	80	°C/W

DESCRIPTION

The LS285 is based on a bridge configuration.

They contain a regulator block, a sending amplifier and a receiver amplifier.

The regulator monitors the line current and adjusts the amplifier gain to compensate for the line length. It provides DC characteristics in line with CEPT standards.

The transmit/receiver amplifiers are connected to the line via an external bridge to provide sidetone attenuation.

The line current compensation ensures that when the subscriber is talking, the signal delivered to the line is increased in according to the line lenght. When he is hearing, the signal level on the receiver capsule is constant.

The amplifiers can also be matched to different transducers simply by varying external components. Gain variation over the operating temperature range is less than ± 1 dB.

The impedance to the line can be adjusted ; without any change in circuit parameters ; by changing an external resistor (6.8 KΩ at pin 2).

BASIC CIRCUIT CONFIGURATION.

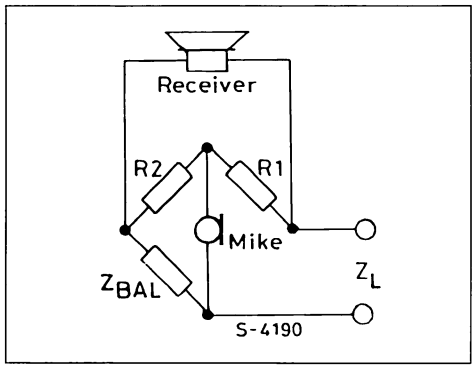


Figure 1 : Test Circuit.

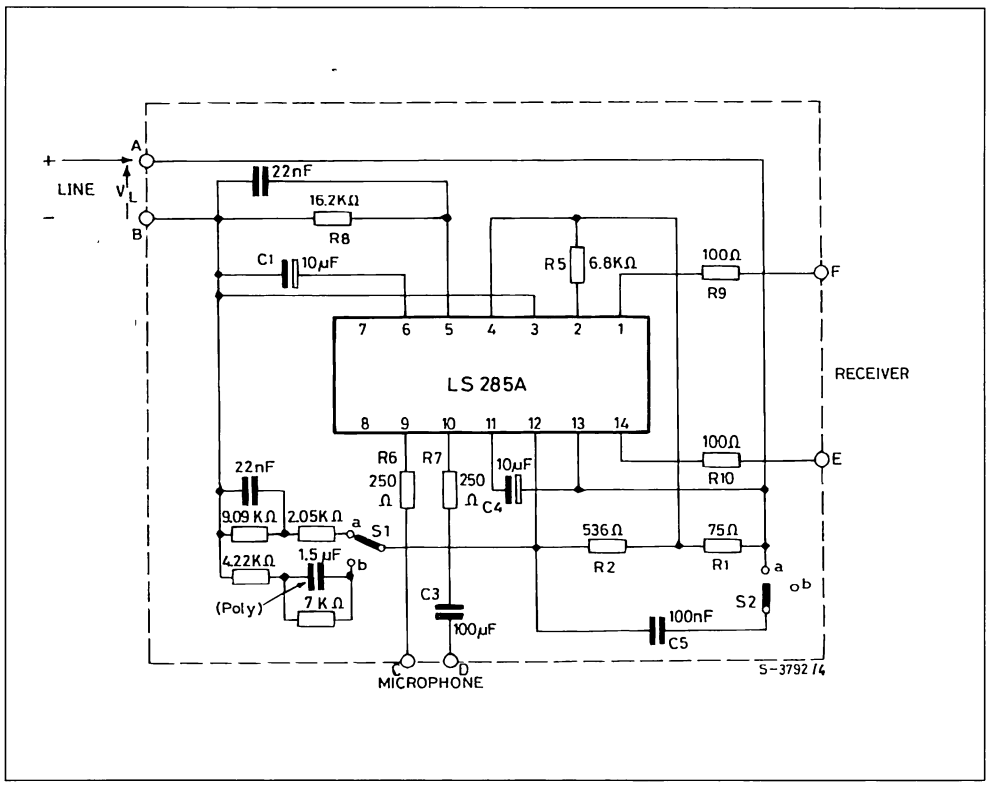
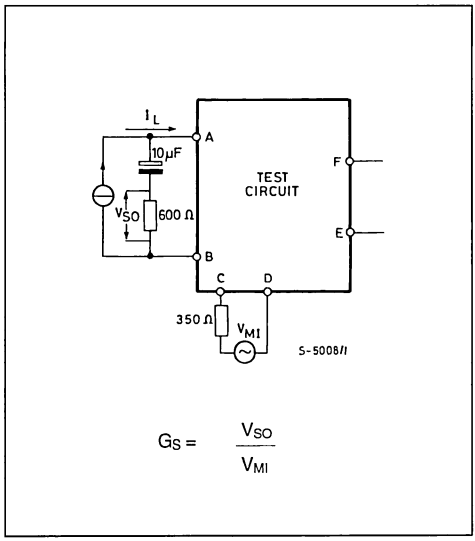
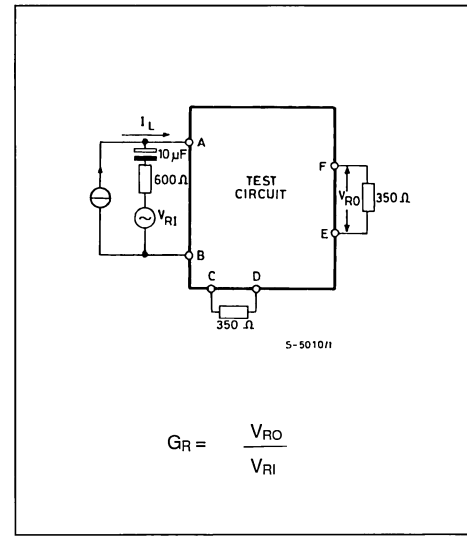


Figure 2 : Sending Gain.



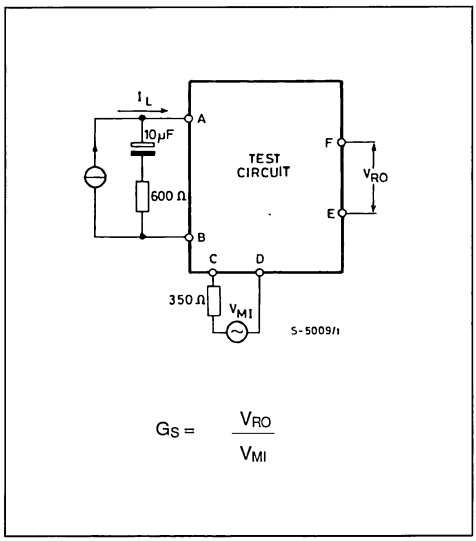
$$G_S = \frac{V_{SO}}{V_{MI}}$$

Figure 3 : Receiving Gain.



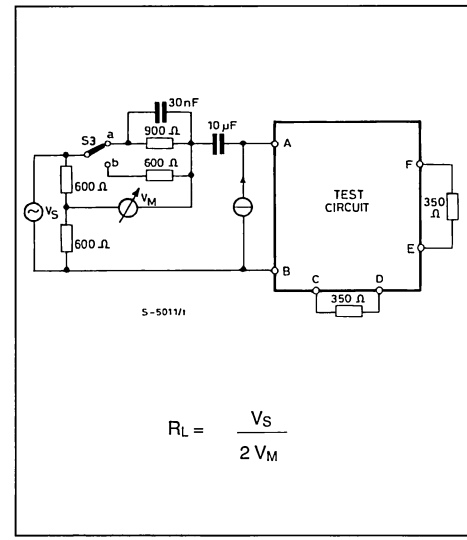
$$G_R = \frac{V_{RO}}{V_{RI}}$$

Figure 4 : Sidetone.



$$G_S = \frac{V_{RO}}{V_{MI}}$$

Figure 5 : Return Loss.



$$R_L = \frac{V_S}{2\,V_M}$$

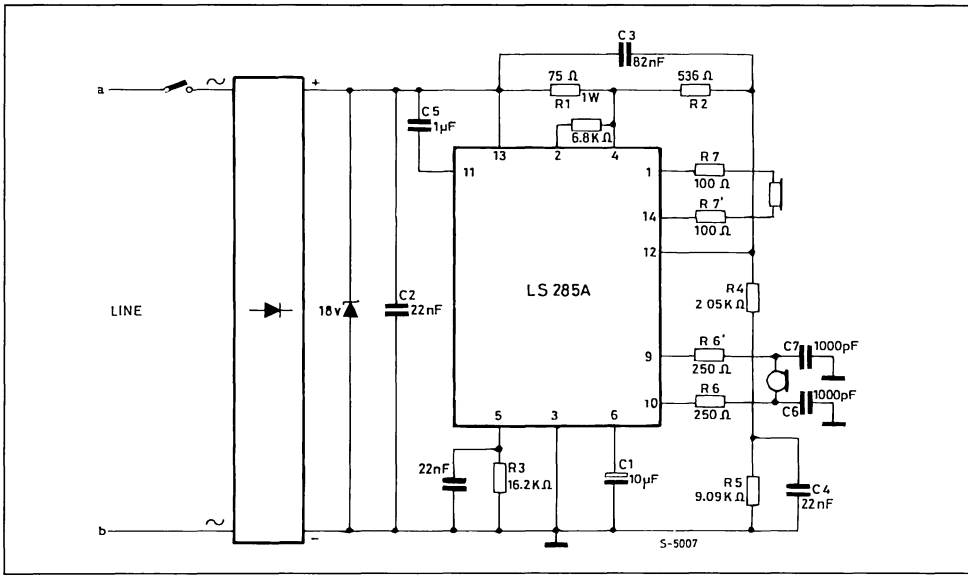
ELECTRICAL CHARACTERISTIC

(refer to the test circuit, T_{amb} = 25°C, f = 300Hz to 3400Hz, S1, S2 in "a" unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_L	Line Voltage	– 15°C < T_{amb} < + 45°C I_L = 80mA I_L = 20mA I_L = 10mA	 9.5 4.8 3.6		 11.5 5.8 1.6	V	1
G_S	Sending Gain	f = 1kHz I_L = 15mA, V_{MI} = 1.0V_{RMS} I_L = 30mA, V_{MI} = 2.5V_{RMS} I_L = 60mA, V_{MI} = 3.7V_{RMS} I_L = 80mA, V_{MI} = 4.5V_{RMS}	 48.5 47.9 42.7 42.0		 52.5 51.5 46.1 45.3	dB	2
G_S	Sending Gain Variation versus Temperature	– 15°C < T_{amb} < + 45°C		0.8		dB	2
	Sending Gain Flatness	I_L = 10 to 80mA f_{ref} = 1kHz, S1, S2 in (b)	- 0.5		+ 0.5	dB	2
	Sending Distortion	I_L = 10 to 15mA, V_{so}<0>=<0>0.7 V_p I_L = 16 to 24mA, V_{so}<0>=<0>1.3 V_p I_L = 25 to 80mA, V_{so}<0>=<0>1.75 V_p			2 2 10	% % %	2 2 2
	Sending Noise	V_{MI} = 0 V, I_L = 60 mA		– 73		dBmp	2
	Microphone Amplifier Impedance (pin 9-10)			95		Ω	1
	Max Sending Output (*)	I_L = 10 to 80mA, V_{MI} = 1V			3	V_p	2
G_R	Receiving Gain	f = 1kHz I_L = 15mA, V_{RI} = 0.8V_{RMS} I_L = 30mA, V_{RI} = 1.0V_{RMS} I_L = 60mA, V_{RI} = 1.8V_{RMS} I_L = 80mA, V_{RI} = 10V_{RMS}	 – 13.3 – 13.5 – 18 – 19		 – 9.3 – 10.5 – 14.9 – 16	dB	3
ΔG_R	Receiving Gain Variation versus Temperature	– 15°C < T_{amb} < + 45°C		0.25		dB	3
	Receiving Gain Flatness	f_{ref} = 1kHz I_L = 10 to 80mA, S1, S2 in (b)	– 0.5		+ 0.5	dB	3
	Receiving Distortion	I_L = 10 to 15mA, V_{RO} = 300mV_p I_L = 15 to 80mA, V_{RO} = 500mV_a			2 2	% %	3 3
	Receiving Amplifier Output Impedance (pin 1-14)			110		Ω	1
	Receiving Noise	V_{RI} = 0 V, I_L = 60 mA, psophometric		80		µV	3
	Max receiving Output Current	I_L = 80 mA, V_{RI} = 10 V			3.6	mAp	3
	Sidetone	f = 1kHz I_L = 20 mA I_L = 80 mA		7 0		dB dB	4 4
	Return Loss	S3 in (a) S3 in (b)		14 14		dB dB	5 5

(*) This output is limited to allow for input overvoltages.

Figure 6 : Typical Application Circuit.



APPLICATION INFORMATION

The following table shows the recommended values for the typical application circuit of fig. 6. Different values can be used and notes are added in order to help designer.

Component	Recommended Value	Purpose	Note
R1	75Ω	Bridge Resistors	The ratio R2/R1 fixes the amount of the signal delivered to the line. (see fig. 7)
R2	536Ω		
R3	16.2kΩ	Bias Resistor	Changing R3 value it is possible to shift the gain characteristics. The value can be chosen from 15kΩ to 20<0>kΩ. The recommended value assures the maximum swing (see fig. 9).
R4	2.05kΩ	Balance Network	In order to optimize the sidetone it is possible to change R4 and R5 values. In any case : $\frac{Z_B}{Z_L} = \frac{R_2}{R_1}$ where Z_B = R4 + R5//C4.
R 5	9.09kΩ		
R6 and R6'	250Ω	Microphone Impedance Matching	R6 and R6' must be equal ; 250 Ω is a typical value for dynamic capsules. Furthermore, they determine a sending gain variation according to : $\Delta G_S = 20 \log \frac{R_X}{850\Omega}$ where Rx = R6 + R6' + R_{mike}. The trend of ΔG_S as a function of Rx value is shown in fig. 8.
R7 and R7'	100Ω	Receive Impedance Matching	R7 and R7' must be equal ; 100Ω is a typical value for dynamic capsules.
C1	10 µF	AC Loop Opening	Ensures a high regulator impedance for AC signals (≈ 20kΩ). This capacitor should not be higher than 10 µF in order to have a short response time of the system.
C2	22nF	Matching to a Capacitive Line	C2 changes with the characteristics of the transmission line.
C3	82nF	High Frequency Roll-off	C3 determines the high frequency response of the circuit. it also acts as RF bypass.
C4	22nF	Balance Network	See Note for R4 and R5.
C5	1 µF	DC decoupling for Receiving Input	
C6 and C7	1000pF	RF Bypass	
C8	22nF	Filtex Capacitor	

Figure 7 : Receiving Gain Variation vs. R1 Value (with fixed R1/R2 ratio).

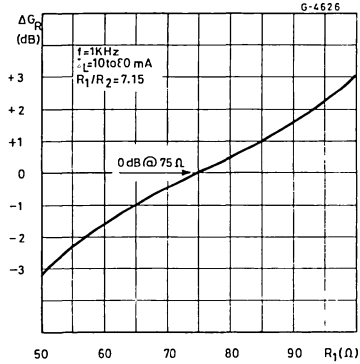


Figure 8 : Sending Gain Variation vs. Rx Value (see note for R6 and R6').

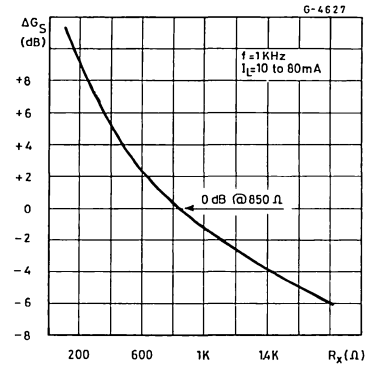
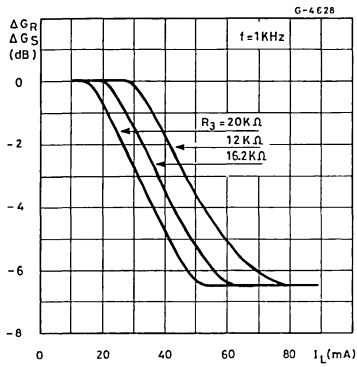


Figure 9 : Sending and receiving Gain Variation vs. Line Current.



PROGRAMMABLE TELEPHONE SPEECH CIRCUIT

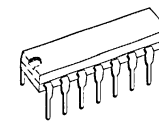
DESCRIPTION

The LS588 is a monolithic integrated circuit in 16 lead dual in-line plastic package. Designed as a replacement for the hybrid circuit in telephone sets it performs all the functions previously carried out by this circuit.

With the LS588 it is possible to select the operating mode (fixed or variable gain). The device works with both piezoceramic and dynamic transducers and therefore its gain, both in sending and receiving paths, can be present by means of two external resistors. This feature can also be obtained in AGC operating mode, when the device automatically adjusts the Rx/Tx gains to compensate for the line attenuation by sensing the line current.

The LS588 can supply the decoupling FET when working with an electret microphone. Output impedance can be matched to the line independently of transducer impedance.

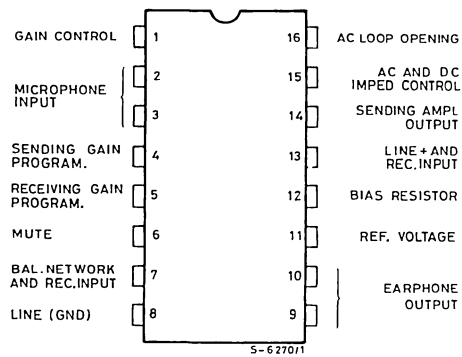
In addition, the LS588 can be set in power down state, where the device displays a strow decrease of the current consumption (about 8 mA), still maintains DC and AC impedances to the line (for parallel operation with a DTMF generator).



DIP16

ORDERING NUMBER : LS588N1

PIN CONNECTION (top view)



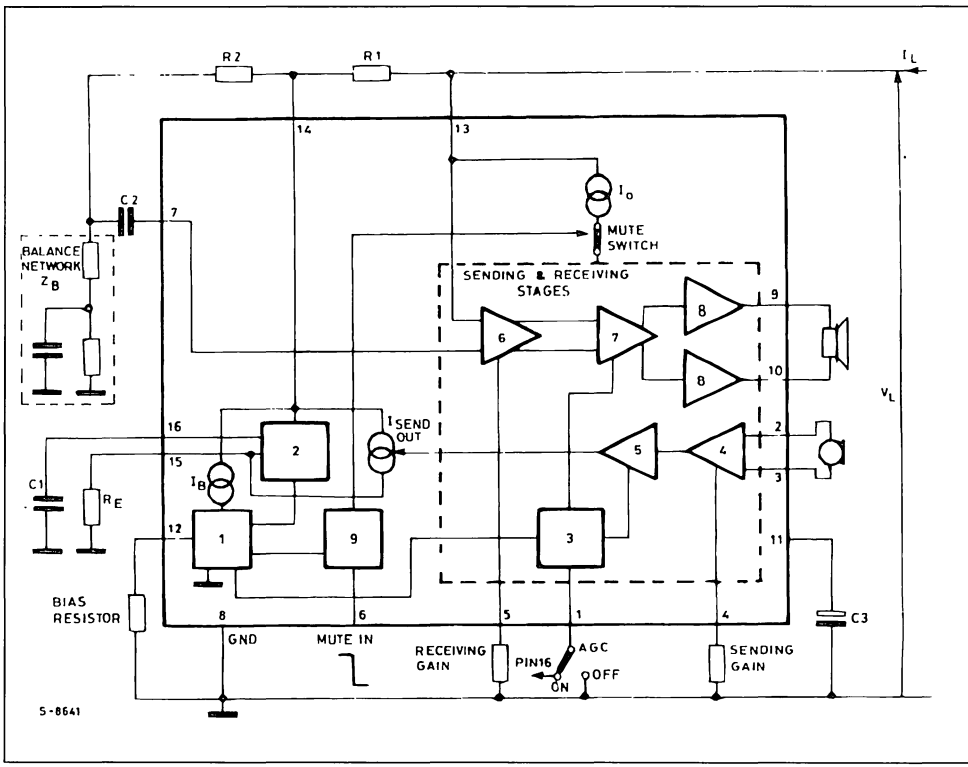
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_L	Line Voltage (3 ms pulse duration)	22	V
I_L	Forward Line Current	150	mA
I_L	Reverse Line Current	– 150	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1	W
T_{op}	Operating Temperature	– 45 to + 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 65 to + 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction–ambient	Max	80	°C/W

BLOCK DIAGRAM



TEST CIRCUITS

Figure 1.

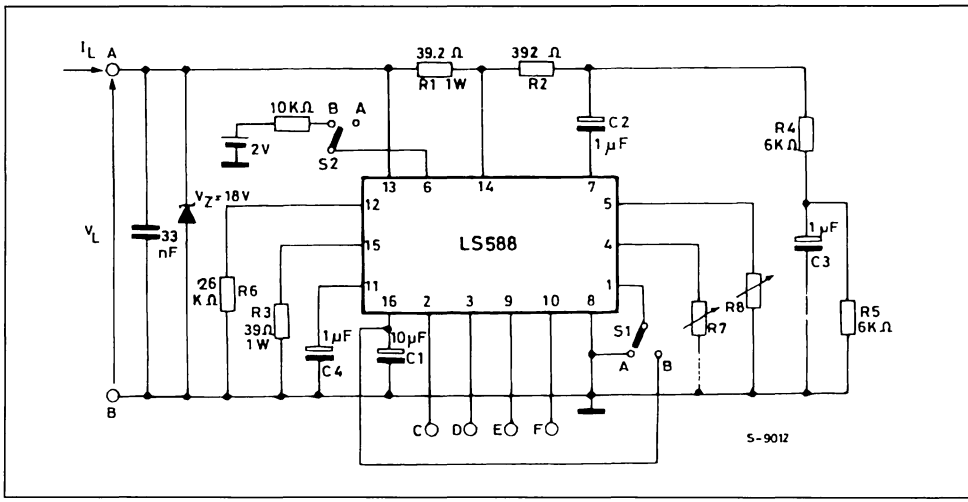


Figure 2.

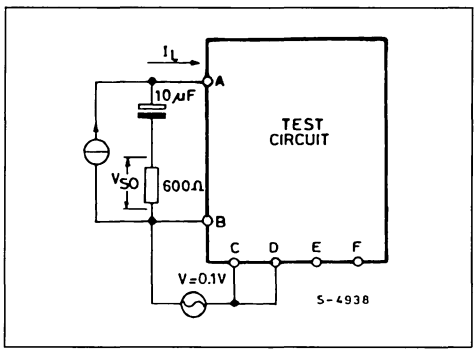


Figure 3.

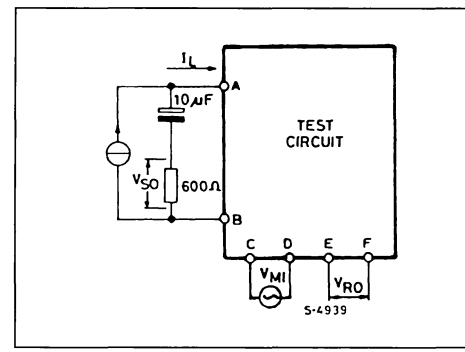
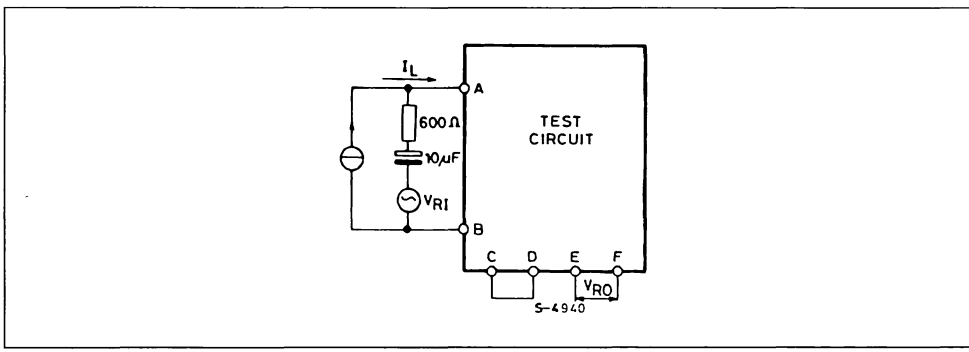


Figure 4.



ELECTRICAL CHARACTERISTICS (Refer to test circuits, T_{amb} = - 25 to + 50°C, f = 200 to 3400Hz, I_L = 15 to 100mA, R_7 = 17.3kΩ, R_8 = 17.1kΩ, S1 in A, S2 in A, unless otherwise specified)

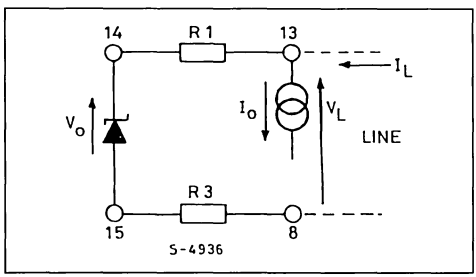
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
A.G.C. On							
V_L	Line Voltage	T_{amb} = 25°C I_L = 15mA I_L = 25mA I_L = 50mA I_L = 120mA	4.1	4.5 5.2 7	4.9 5.6 7.8 14	V	1
CMR	Common Mode Rejection	f = 1kHz	50			dB	2
G_S	Sending Gain	I_L = 50mA, f = 1kHz T_{amb} = 25°C, V_{MI} = 2mV R_7 = 17.3kΩ R_7 = 22.0kΩ	 39.0 43.8		 41.0 46.2	dB	3
ΔG_S	Sending Gain Variation versus Current	I_{ref} = 50mA, T_{amb} = 25°C	− 0.5		+ 0.5	dB	3
	Sending Gain Variation versus Current (S1 in B)	I_{ref} = 50mA, T_{amb} = 25°C I_L = 25mA I_L = 100mA	 4.0 − 2.0		 6 0	dB	3
	Sending Gain Variation versus Frequency	f_{ref} = 1kHz	− 0.5		0.5	dB	3
THD_S	Sending Distortion	f = 1kHz I_L = 15 to 25mA, V_{so} = 450mV I_L = 25 to 100mA, V_{so} = 1.6V			 2 5	%	3
N_S	Sending Noise	V_{MI} = 0mV		− 74		dBm	3
Z_{MI}	Microphone Impedance	V_{MI} = 3mV	11	15		kΩ	3
G_R	Receiving Gain	I_L = 50mA, f = 1kHz T_{amb} = 25°C, V_{RI} = 570mV R_8 = 17.1kΩ R_8 = 14.7kΩ	 2.3 − 0.1		 4.7 1.9	dB	4
ΔG_R	Receiving Gain Variation versus Current	I_{ref} = 50 mA, T_{amb} = 25 °C	− 0.5		+ 0.5	dB	4
	Receiving Gain Variation versus Current (S1 in B)	I_{ref} = 50 mA, T_{amb} = 25 °C I_L = 25mA I_L = 100mA	 4.0 − 2.0		 6 0	dB	4
	Receiving Gain Variation versus Frequency	f_{ref} = 1 kHz	− 0.5		0.5	dB	4
THD_R	Receiving Distortion	V_{RI} = 570 mV			2		
		V_{RI} = 775 mV			5	%	4
N_R	Receiving Noise	V_{RI} = 0 mV		150		µV	4
Z_{RO}	Receiving Output Impedance	V_{RO} = 50mV		50		Ω	4
	Sidetone	f = 1kHz		15		dB	3
Z_{ML}	Line Matching Impedance	V_{RI} = 0.3V, f = 1kHz	650		850	Ω	4
	Max Receiving Output (click suppression)	V_{RI} = 2V	3.9	4.4		V_{PP}	4
V_{SM}	Microphone Supply	R_{load} = 2.2 kΩ	1.9		2.2	V	1
MUTE OPERATION							
	Mute Threshold Voltage (pin 6)	Speech Condition Mute Condition	 1.5		0.8	V V	– –
	Muting Operation Current (pin 6) (S2 in B)		50			µA	–
	Line Dynamic in Mute Condition (S2 in B) THD = 2 %	I_L = 3.5 mA I_L = 4 mA	600 850			mV mV	– –
	Line Voltage in Mute Condition (S2 in B)	I_L = 3.5 mA I_L = 4 mA		3.6 4.2		V V	– –

CIRCUIT DESCRIPTION

1. DC Characteristic

In accordance with CCITT recommendations, any device connected to a telephone line must exhibit a proper DC characteristic V_L, I_L.
The DC characteristics of the LS588 is determined by the shunt regulator (block 2) together with two series resistors R_1 and R_3 (see the block diagram). The equivalent circuit is shown in fig. 5.
A fixed amount, I_o, of the total available current, I_L, is drained to allow the circuit to operate correctly. The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 12.
The recommended minimum value of I_o is 7.5mA with R pin 12 = 26kΩ.
The voltage $V_o \cong 3.8$ V of the shunt regulator is independent of the line current.
The shunt regulator (block 2) is controlled by a temperature compensated voltage reference (block 1).
Fig. 6 shows a more detailed circuit configuration of the shunt regulator.
The difference I_L-I_o flows through the shunt regulator since I_b is negligible.
I_a is an internal constant current generator ; hence $V_o = V_B + Ia \cdot R_a = 3.8V$.
The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series with a battery.
It is important to note that the DC voltage at pin 16 is proportional to the line current $V_{16} = V_{15} + V_B = (I_L - I_o) R_3 + V_B$.

Figure 5 : Equivalent DC Load to the Line.



2. Two To Four Wires Conversion

The LS588 performs the two wire (line) to four wire (microphone, earphone) conversion by means of a Wheatstone bridge configuration thus obtaining the proper decoupling between sending and receiving signals (see fig. 7).

For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$.

The AC signal from the microphone is sent to one diagonal of the bridge (pin 8 and 14). A small percentage of the signal power is lost on Z_B (since $Z_B >> Z_L$) ; the main part is sent to the line via R_1.
In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 7 and 13). After amplification it is applied to the receiving capsule.
The impedance Z_M is simulated by the shunt regulator which also acts as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{(14-8)}}{\Delta I_{(14-8)}}$

From fig. 6, considering C_1 as a short circuit to the AC signal, any variation in V_{14} generates a variation as follows :

$$V_{15} = V_A = V_{14} \frac{R_b}{R_a + R_b}$$

the corresponding current change is :

$$\Delta I = \frac{\Delta V_{15}}{R_3}$$

therefore

$$Z_M = \frac{\Delta V_{14}}{\Delta I} = R_3 \left(1 + \frac{R_a}{R_b}\right)$$

The total impedance across the line connections (pin 13 and 8) is given by

$$Z_{ML} = R_1 + Z_M // (R_2 + Z_B)$$

By choosing Z_M R_1 and Z_B Z_M

$$Z_{ML} \cong Z_M = R_3 \left(1 + \frac{R_a}{R_b}\right)$$

The amplitude of the signal received across pins 13 and 7 can be changed using different values of R_1 (of course the relationship $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$ must always be valid).

The received signal is related to the value of R_1 according to the approximated relationship :

$$V_R = V_{RI}\, 2 \frac{R_1}{R_1 + Z_M}$$

Note that if the value of R_1 is changed the transmission signal current is not changed, since the microphone amplifier is a transconductance amplifier.

3. Input and Output Amplifiers

The microphone amplifier (4) has a differential input stage with high impedance (min 11 K) so allowing a good matching to the microphone by means of an external resistor without affecting the sending gain.

The receiving output stage (8) is intended to drive both piezoceramic and dynamic capsules. It has low

output impedance, a maximum voltage swing greater than 2 V_p and a peak current of 2 mA.

With very low impedance transducers, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

4. Gain Control

It is possible to set the LS588 gain characteristics by means of one pin (pin 1).

When the pin 1 is grounded, the gains of the sending and receiving amplifiers do not depend on the line current (AGC off). When the pin 1 is connected to pin 15 the LS588 automatically changes the gain to compensate for line attenuation (AGC on).

4.1. AGC OFF

In this conditions, as already mentioned, both the sending and the receiving gain are fixed. Their values are determined, independently for the two paths, by the two external resistors R_7 (for T_x, between pin 4 and ground) and R_8 (for R_x, between pin 5 and ground), in a wide range (see fig. 8 and 9).

4.2. AGC ON

Starting from any couple of gain values, fixed by the appropriate values of R_7 and R_8, the LS588 can automatically change the sending and receiving gains depending on the line current.
The line current is sensed across R_3 (see fig. 7) and transferred to pin 16 by the regulator.

$$V_{16} = V_B + V_{15} = V_B + (I_L - I_o) \cdot R_3$$

Following comparison with an internal reference (block 1) the voltage at pin 1 is used to modify (block 3) the gain of the amplifiers (5) and (7) on both the sending and receiving paths.

The starting point of the automatic level control is obtained at I_L = 25mA when the drain current I_o = 7.5mA.

The external resistors R_7 and R_8 fix the maximum value for the gains.

Minimum gain is reached for a line current of about 100mA when the same drain current I_o of 7.5mA is used.

5. DC Shunt Regulator

The LS588 has built into the chip a DC shunt regulator intended to supply (pin 11) the coupling FET when an electret microphone is used. It delivers 1 mAp current with a voltage of 2 Volts (typ) regardless of the line current.

6. Mute Condition and Mutifrequency Interfacing

- A logical control (mute) at pin 6 allows operation in parallel with a proper DTMF generator connectable to the line.
- When pin 6 is set high (more than 1.8 Volt) the mute logic circuit (block 9) switches off both sending and receiving stages (mute switch) and reduces (1) the bias current, to sabe about 10 mA, available for the paralleled DTMF generator.

In this condition the LS588 still shows to the line the specified AC impedance (650 to 850 Ω) not provided by the DTMF generator which acts as a current generator.

7. Anticlipping Application

It is possible to avoid distortion of the sending signal limiting the sending gain with an external control at pin 4 (gain programming).

The maximum level to the line will be :

$$V_S = \frac{0.6V}{\sqrt{2}} \times \frac{R_{AC1} + R_{AC2}}{R_{AC2}}$$

The following table can be helpful to the designer when choosing different values for the external components, it refers to the typical application circuit of fig. 10.

Figure 6 : Circuit Configuration of the Shunt Regulator.

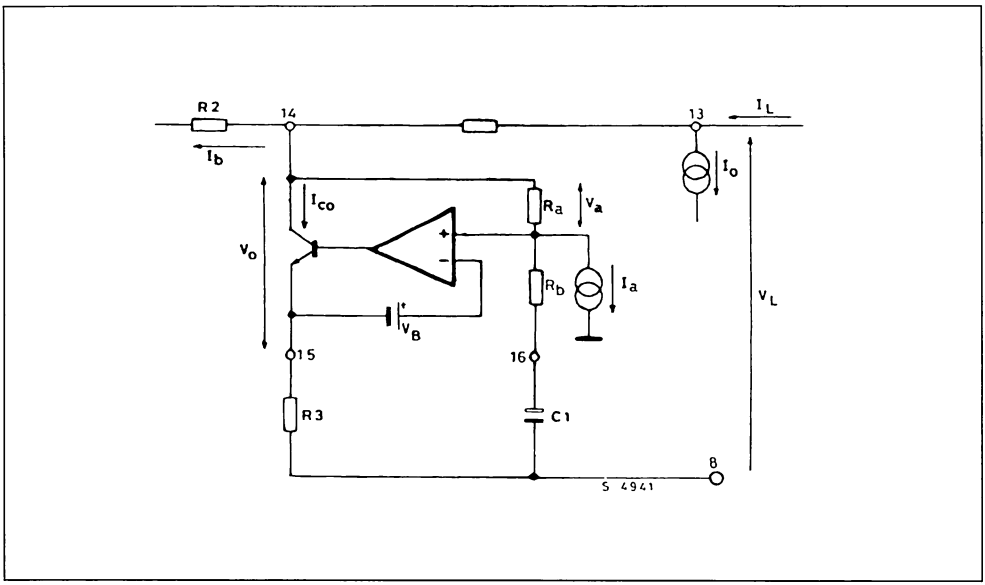


Figure 7 : Two to four Wires Conversion.

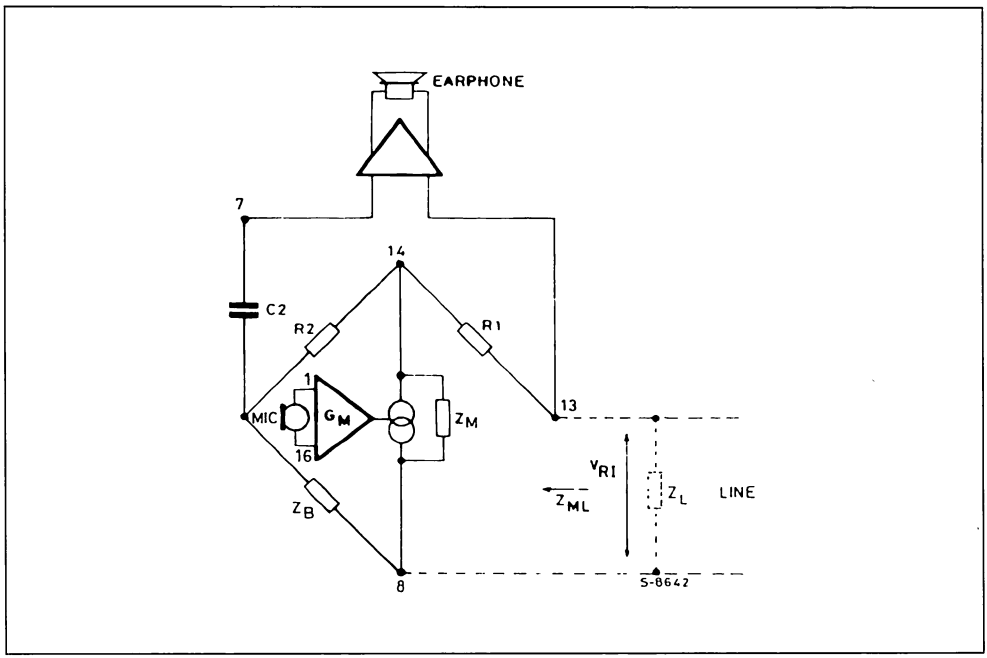


Figure 8 : Sending Gain vs. R_7 Value (AGC OFF).

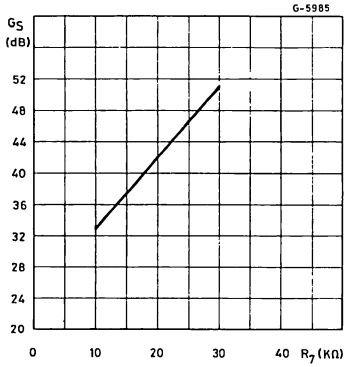


Figure 9 : Receiving Gain vs. R_8 Value (AGC OFF).

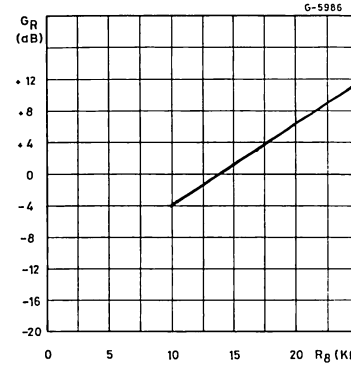


Figure 10 : Typical Application Circuit (piezoceramic transducers).

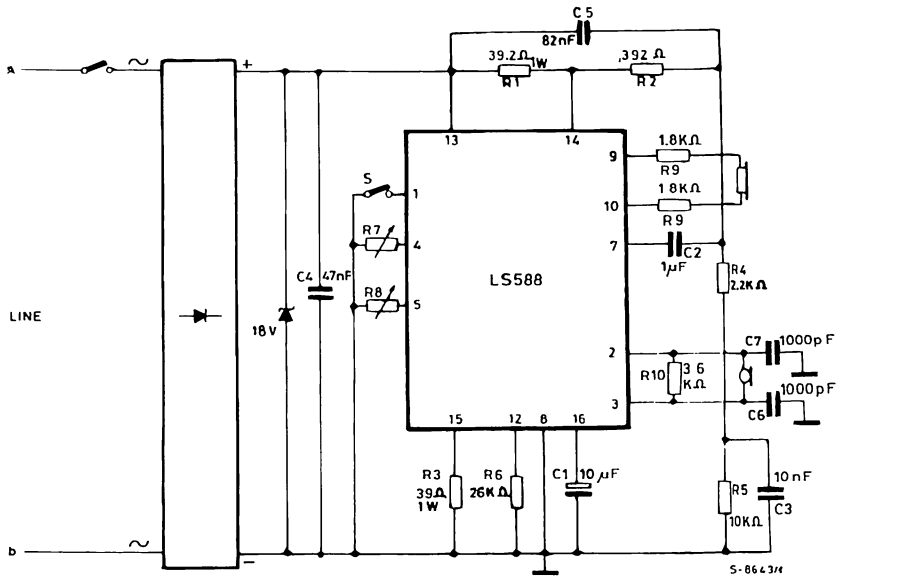
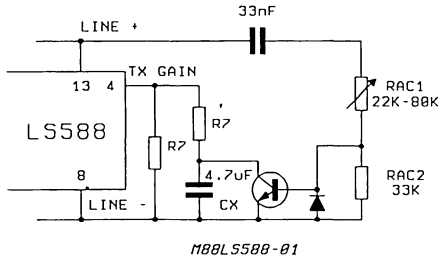
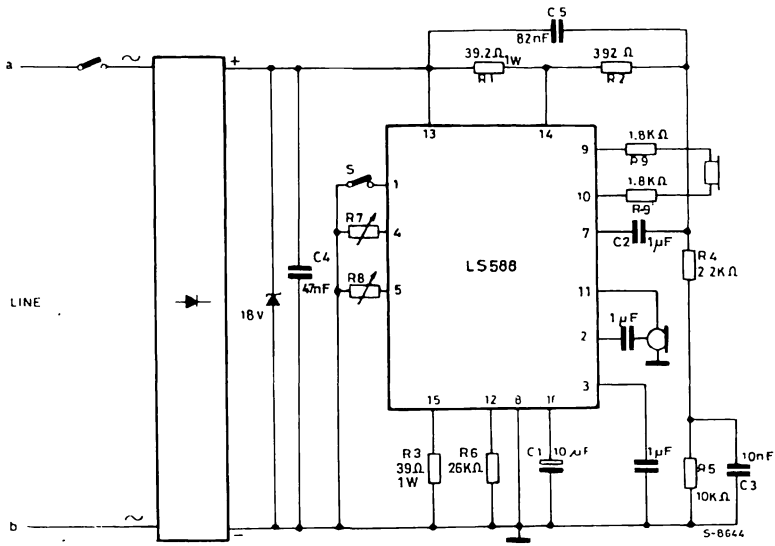


Figure 11 : Anticlipping Application.



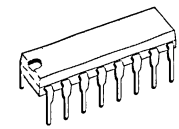
APPLICATION INFORMATION

Figure 12 : Application Circuit with Electret Microphone.

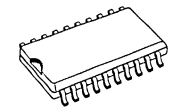


TELEPHONE SPEECH CIRCUIT WITH MULTIFREQUENCY TONE GENERATOR INTERFACE

- PRESENTS THE PROPER DC PATH FOR THE LINE CURRENT, PARTICULAR CARE BEING PAID TO HAVE LOW VOLTAGE DROP
- HANDLES THE VOICE SIGNAL, PERFORMING THE 2/4 WIRES INTERFACE AND CHANGING THE GAIN ON BOTH SENDING AND RECEIVING AMPLIFIERS TO COMPENSATE FOR LINE ATTENUATION BY SENSING EITHER THE LINE CURRENT OR THE LINE VOLTAGE. IN ADDITION, THE LS656 CAN ALSO WORK IN FIXED GAIN MODE
- ACTS AS LINEAR INTERFACE FOR MF, SUPPLYING A STABILIZED VOLTAGE TO THE DIGITAL CHIP AND DELIVERING TO THE LINE THE MF TONES GENERATED BY THE M761



DIP16



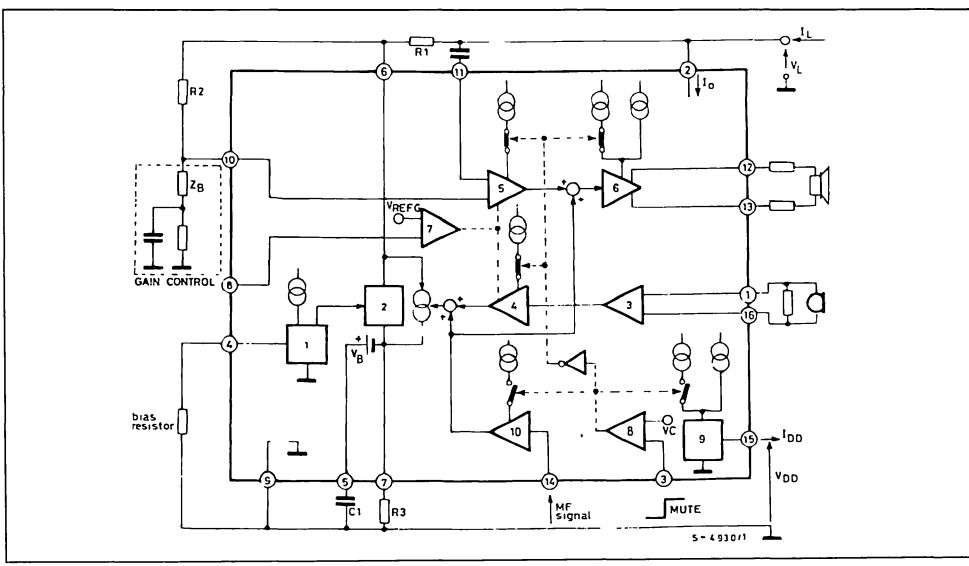
SO20L

ORDERING NUMBERS : LS656AB (DIP16)
LS656AD1 (SO20)

DESCRIPTION

The LS656 is a monolithic integrated circuit in 16-lead plastic package to replace the hybrid circuit in telephone set. It works with the same type of transducers for both transmitter and receiver (typically dynamic capsules). Many of its electrical characteristics can be controlled by means of external components to meet different specifications.
In addition to the speech operation, the LS656 acts as an interface for the MF tone signal (particularly for M761 C/MOS frequency synthesizer).

BLOCK DIAGRAM (DIP16)



ABSOLUTE MAXIMUM RATINGS

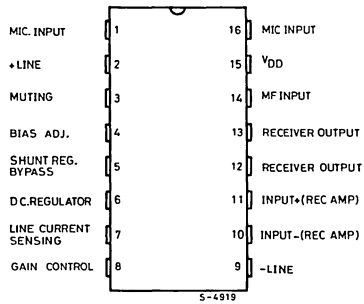
Symbol	Parameter	Value	Unit
V_L	Line Voltage (3 ms pulse duration)	22	V
I_L	Forward Line Current	150	mA
I_L	Reverse Line Current	– 150	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1	W
T_{op}	Operating Temperature	– 45 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 65 to 150	°C

THERMAL DATA

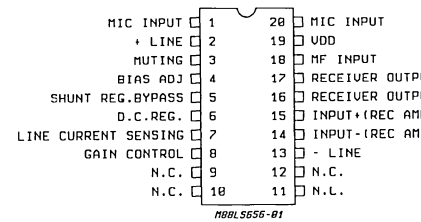
Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

PIN CONNECTIONS (top view)

DIP-16



SO-20L



TEST CIRCUITS

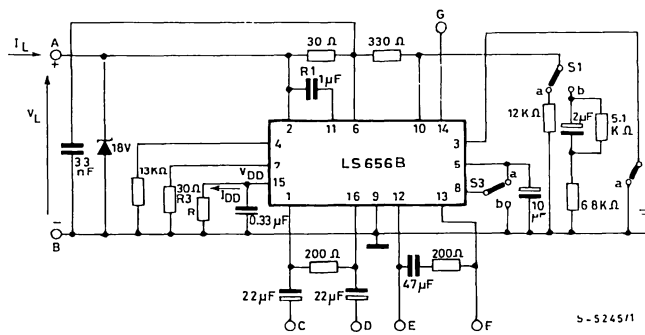
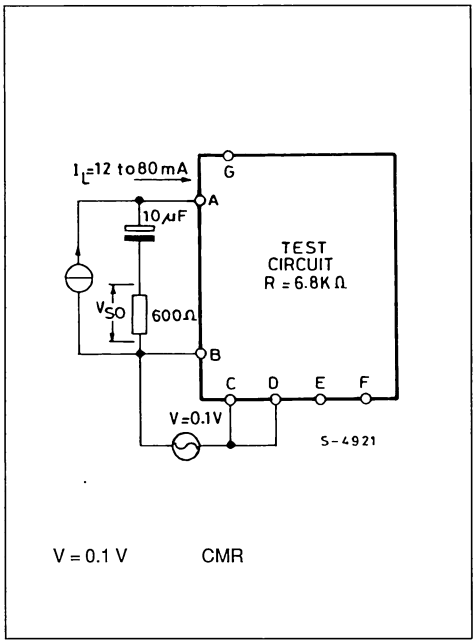
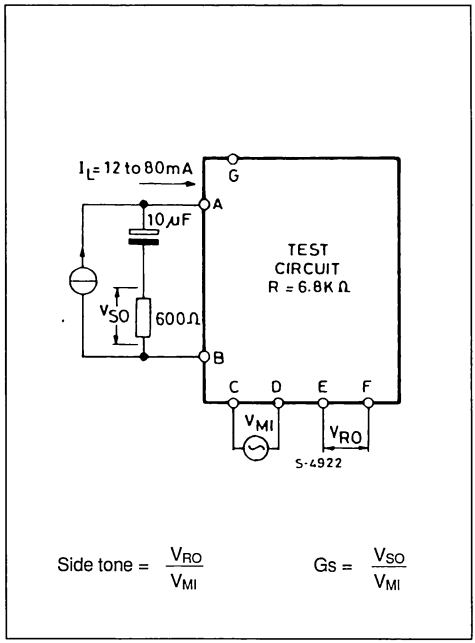


Figure 1.



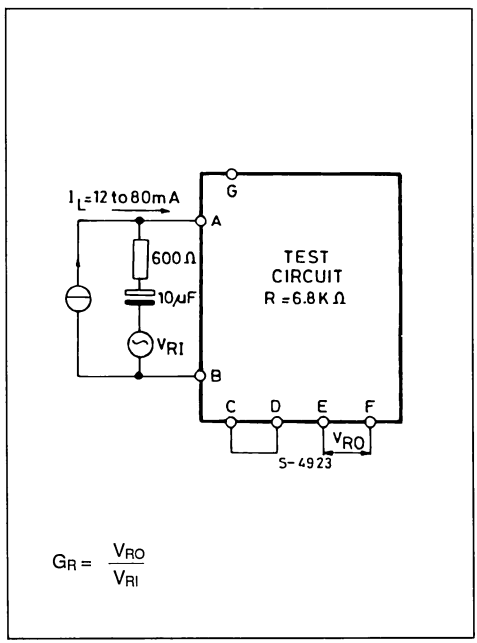
V = 0.1 V CMR

Figure 2.



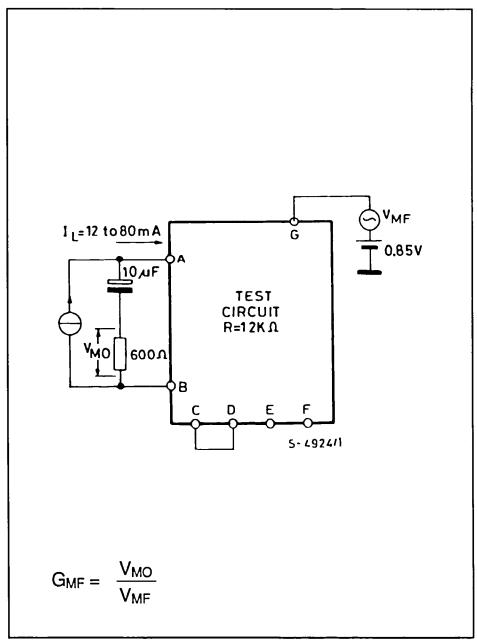
Side tone = $\frac{V_{RO}}{V_{MI}}$ Gs = $\frac{V_{SO}}{V_{MI}}$

Figure 3.



$G_R = \frac{V_{RO}}{V_{RI}}$

Figure 4.



$G_{MF} = \frac{V_{MO}}{V_{MF}}$

ELECTRICAL CHARACTERISTICS (refer to the test circuits, V_G = 1 to 2V, I_L = 12 to 80mA, S1, S2 and S3 in (a), T_{amb} = – 25 to + 50°C, f = 200 to 3400Hz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION							
V_L	Line Voltage	T_{amb} = 25°C I_L = 12mA I_L = 30mA I_L = 60mA	3.4		4.0 5.1 7.0	V	–
CMR	Common Mode Rejection	f = 1kHz	50			dB	1
G_S	Sending Gain	T_{amb} = 25°C, f = 1kHz, V_{MI} = 2mV I_L = 25mA I_L = 50mA	 48 44		 51 47	dB	2
	Sending Gain Flatness (versus frequency)	V_{MI} = 2mV, f_{ref} = 1kHz	– 1		+ 1	dB	2
	Sending Gain Flatness (versus current)	V_{MI} = 3 mV, I_{ref} = 50mA, S3 in (b)	– 1		+ 1	dB	2
	Sending Distortion	f = 1kHz, I_L = 16mA V_{so} = 775mV V_{so} = 900mV			 3 10	 % %	2
	Sending Noise	V_{MI} =0V; V_G = 1V; S1 in (b)		– 71		dBmp	2
	Microphone Input Impedance (pin 1-16)	V_{MI} = 2mV	40			kΩ	–
	Sending Gain in MF Operation	V_{MI} = 2mV, S2 in (b)	– 30			dB	2
G_R	Receiving gain	V_{RI} = 0.3V, f = 1kHz, T_{amb} = 25°C I_L = 25mA I_L = 50mA	 – 6 – 11		 – 3 – 8	dB	3
	Receiving Gain Flatness (vs. freq.)	V_{RI} = 0.3V, f_{ref} = 1kHz	– 1		+ 1	dB	3
	Receiving Gain Flatness (vs. current)	V_{RI} = 0.3V, I_{ref} = 50mA, S3 in (b)	– 1		+ 1	dB	3
	Receiving Distortion	f = 1kHz, I_L = 15mA V_{RO} = 400mV V_{RO} = 450mV			 3 10	%	3
	Receiving Noise	V_{RI} = 0V; V_G = 1V; S1 in (b)		150		µV	3
	Receiving Ouptut Impedance (pins 12-13)	V_{RO} = 50mV		30		Ω	–
	Sidetone	f = 1kHz, T_{amb} = 25°C, S1 in (b)			36	dB	2
Z_{ML}	Line Matching Impedance	V_{RI} = 0.3V, f = 1kHz	500	600	700	Ω	3
I_8	Input Current for Gain Control (pin 8)				– 10	µA	–

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
MULTIFREQUENCY SYNTHESIZER INTERFACE							
V_{DD}	MF Supply Voltage Stand by and Operation	S2 in (b)	2.4	2.5	2.7	V	–
I_{DD}	MF Supply Current Stand by Operation	S2 in (b)	0.5 2			mA mA	– –
	MF Amplifier Gain	$f_{MF\ in}$ = 1kHz, $V_{MF\ in}$ = 80mV	15		17	dB	4
V_I	DC Input Voltage Level (pin 14)	$V_{MF\ in}$ = 80mV		V_{DD} x 0.3		V	–
R_I	Input Impedance (pin 14)	$V_{MF\ in}$ = 80mV	60			kΩ	–
d	Distortion	$V_{MF\ in}$ = 150mVp, I_L > 17mA			4	%	4
	Starting Delay Time				5	ms	–
	Muting Threshold Voltage (pin3)	Speech Operation MF Operation	 1.6		1	V V	– –
	Muting Stand by Current (pin 3))				– 10	µA	–
	Muting Operating Current (pin 3)	S2 in (b)			+ 10	µA	–

CIRCUIT DESCRIPTION

1. DC Characteristic

The fig. 5 shows the DC equivalent circuit of the LS656.

A fixed amount I_o of the total available current I_L is drained for the proper operation of the circuit. The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 4 (see block diagram).

The minimum value of I_o is 7.5 mA.

The voltage V_o = 37 V of the shunt regulator is independent of the line current.
The shunt regulator (2) is controlled by a temperature compensated voltage reference (1) (see the block diagram).

Fig. 6 shows a more detailed circuit configuration of the shunt regulator.

The difference I_L-I_o flows through the shunt regulator being I_b negligible. I_a is an internal constant current generator ; hence $V_o = V_B + I_a \cdot R_a = 3.7$ V.

The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series to a battery.

It is important to note that the DC voltage at pin 5 is proportional to the line current ($V_5 = V_7 + V_B = (I_L - I_o)\ R3 + V_B$).

The DC characteristic of the LS656 is shown in fig. 7.

Figure 5 : Equivalent DC Load to the Line.

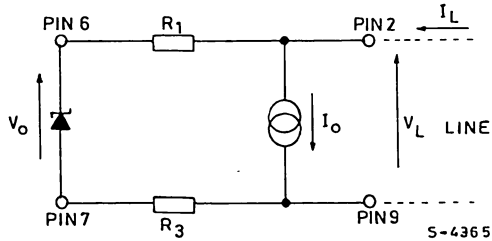


Figure 6 : Circuit Configuration of the Shunt Regulator.

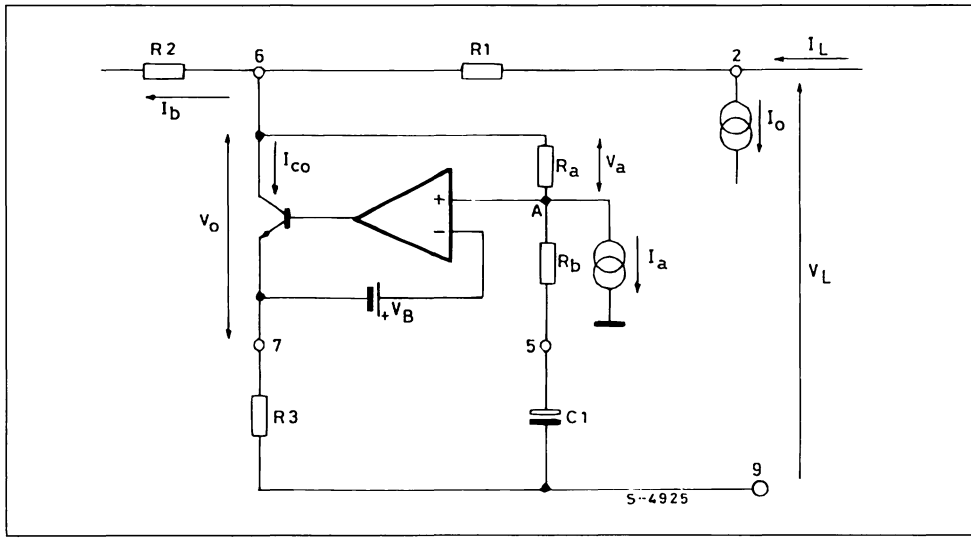
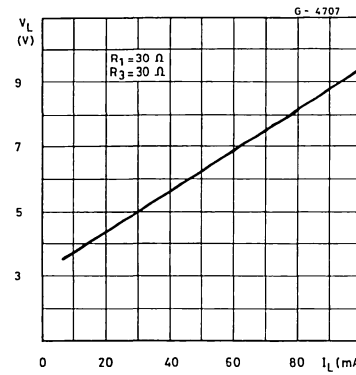


Figure 7 : DC Characteristic.



2. Two to Four Wires Conversion

The LS656 performs the two wires (line) to four wires (microphone, earphone) conversion by means of a Wheatstone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see fig. 8).

For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$

The AC signal from the microphone is sent to one diagonal of the bridge (pin 6 and 9). A small percentage of the signal power is lost on Z_B (being $Z_B >> Z_L$) ; the main part is sent to the line via R1. In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 11 and 10). After amplification it is applied to the receiving capsule.

The impedance Z_M is simulated by the shunt regulator that is also intended to work as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{6-9}}{\Delta I_{6-9}}$

From fig. 6 considering C1 as a short circuit for AC signal, any variation ΔV_6 generates a variation :

$$\Delta V_7 = \Delta V_A = \Delta V_6 \cdot \frac{R_b}{R_a + R_b}$$

The corresponding current is

$$\Delta I = \frac{\Delta V_7}{R_3}$$

Therefore

$$Z_M = \frac{\Delta V_6}{\Delta I} = R3\left(1 + \frac{R_a}{R_b}\right)$$

The total impedance across the line connections (pin 11 and 9) is given by

$$Z_{ML} = R1 + Z_M//(R2 + Z_B)$$

By choosing $Z_M \geq R1$ and $Z_B \geq Z_M$

$$Z_{ML} \cong Z_M = R3\left(1 + \frac{R_a}{R_b}\right)$$

The received signal amplitude across pin 11 and 10 can be changed using different value of R1 (of course the relationship $Z_L/Z_B = R1/R2$ must be always valid).
The received signal is related to R1 value according to the approximated relationship :

$$V_R = 2\,V_{RI}\frac{R_1}{R_1 + Z_M}$$

Note that by changing the value of R1, the transmission signal current is not changed, being the microphone amplifier a transconductance amplifier.

3. Automatic Gain Control

The LS656 automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation.

This function is performed by the circuit of fig. 9.

The differential stage is progressively unbalanced by changing V_G in the range 1 to 2 V (V_{REFG} is an internal reference voltage, temperature compensated).

It changes the current I_G, and this current is used as a control quantity for the variable gain stages (amplifier (4) and (5) in the block diagram). The voltage V_G can be taken :

a) from the LS656 itself (both in variable and in fixed mode) and.
b) from a resistive divider, directly at the end of the line.

a) In the first case, connecting V_G (pin 8) to the regulator bypass (pin 5) it is possible to obtain a gain characteristic depending on the current.
In fact (see fig. 6)

$$V_5 = V_B + V_7 \cong V_B = (I_L - I_o)\,R3$$

The starting point of the automatic level control is obtained at I_L = 25 mA when the drain current I_o = 7.5 mA.

Minimum gain is reached for a line current of about 50 mA for the same drain current I_o = 7.5 mA. When I_o is increased by means of the external resistor connected to pin 4, the two above mentioned values of the line current for the starting point and for the minimum gain increase accordingly.

It is also possible to change the starting point without changing I_o by connecting pin 8 to the centre of a resistive divider placed between pin 5 and ground (the total resistance seen by pin 5 must be at least 100 KΩ). In this case, the AGC range increases too; for example using a division 1 : 1 (50 K/50 K) the AGC starting point shifts to about I_L = 40 mA, and the minimum gain is obtained at I_L = 95 mA. In addition to this operation mode, the V_G voltage can be maintained constant thus fixing the gain value (Rx, Tx) independently of the line conditions.
For this purpose the V_{DD} voltage, available for supplying the MF generator, can be used.

b) When gains have to be related to the voltage at the line terminals of the telephone set, it is necessary to obtain V_G from a resistive divider directly connected to the end of the line.

This type of operation meets the requirements of the French standard. (See the application circuit of fig. 13).

4. Transducer Interfacing

The microphone amplifier (3) has a differential input stage with high impedance (≅ 40kΩ) so allowing a good matching to the microphone by means of external resistor without affecting the sending gain. The receiving output stage (6) is particularly intended to drive dynamic capsules. (Low output impedance (100Ω max) ; high current capability 3 mAp).

When a piezoceramic capsule is used, it is useful to increase the receiving gain by increasing R1 value (see the relationship for V_R).

Whit very low impedance transducer, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

5. Multifrequency Interfacing

The LS656 acts as a linear interface for the Multifrequency synthesizer M761 according to a logical signal (mute function) present on pin 3.

When no key of the keyboard is pressed the mute state is low and the LS656 feeds the M761 through pin 15 with low voltage and low current (standby operation of the M761). The oscillator of the M761 is not operating.

When one key is pressed, the M761 sends a "high state" mute condition to the LS656. A voltage com-

parator (8) of LS656 drives internal electronic switches ; the voltage and the current delivered by the voltage supply (9) are increased to allow the operation of the oscillator.

This extra current is diverted by the receiving and sending section of the LS656 and during this operation the receiving output stage is partially inhibited and the input stages of sending and receiving amplifiers are switched OFF.

A controlled amount of the signalling is allowed to reach the earphone to give a feedback to the subscriber ; the MF amplifier (10) delivers the dial tones to the sending paths.

The mute function can be used also when a temporary inhibition of the output signal is requested. The application circuit shown in fig. 10 fulfils the EUROPE II standard (-6, -8 dBm). If the EUROPE I levels are required (-9, -11 dBm) an external divider

Figure 8 : Two to Four Wires Conversion.

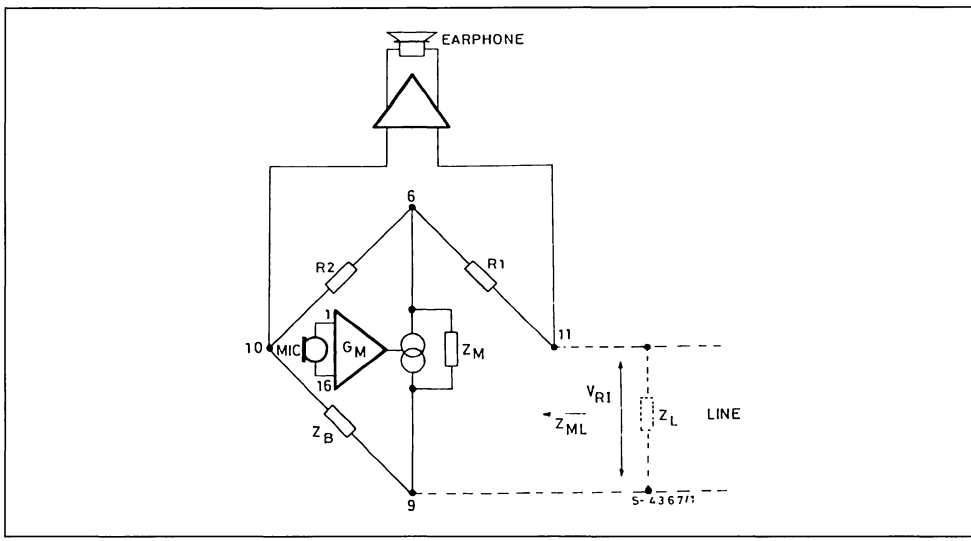
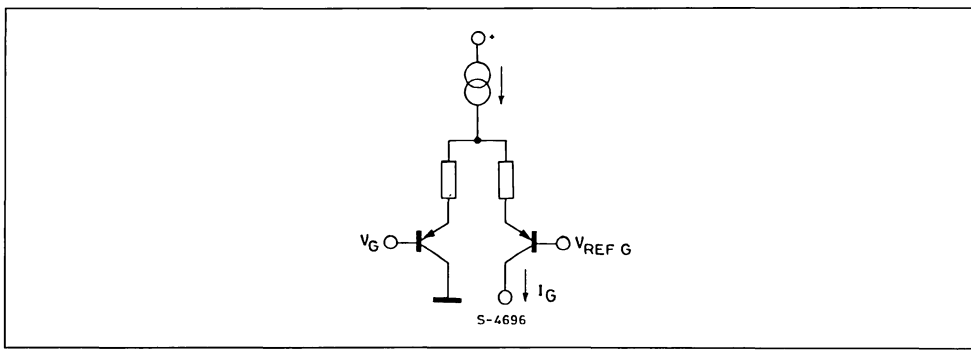


Figure 9.



APPLICATION INFORMATION

Figure 10 : Application Circuit with Multifrequency (Europe II STD).

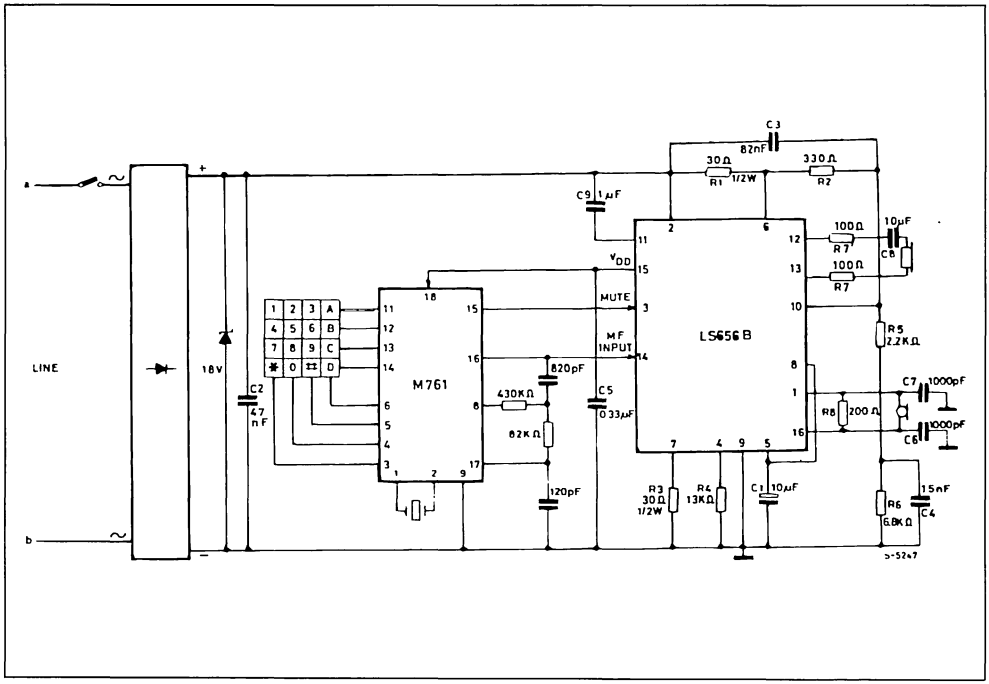


Figure 11 : Application Circuit with Multifrequency (Europe I STD).

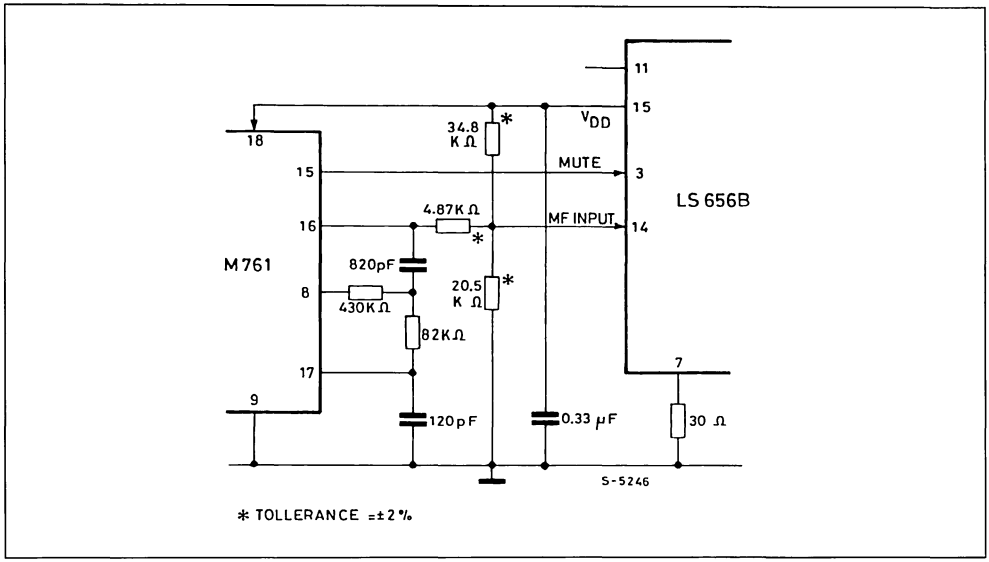


Figure 12 : Sending and Receiving Gain vs. Line Current (application circuit of fig. 10).

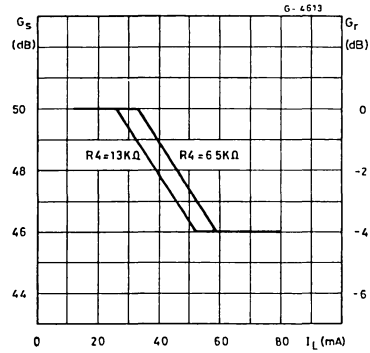


Figure 13 : Application Circuit without Multifrequency.

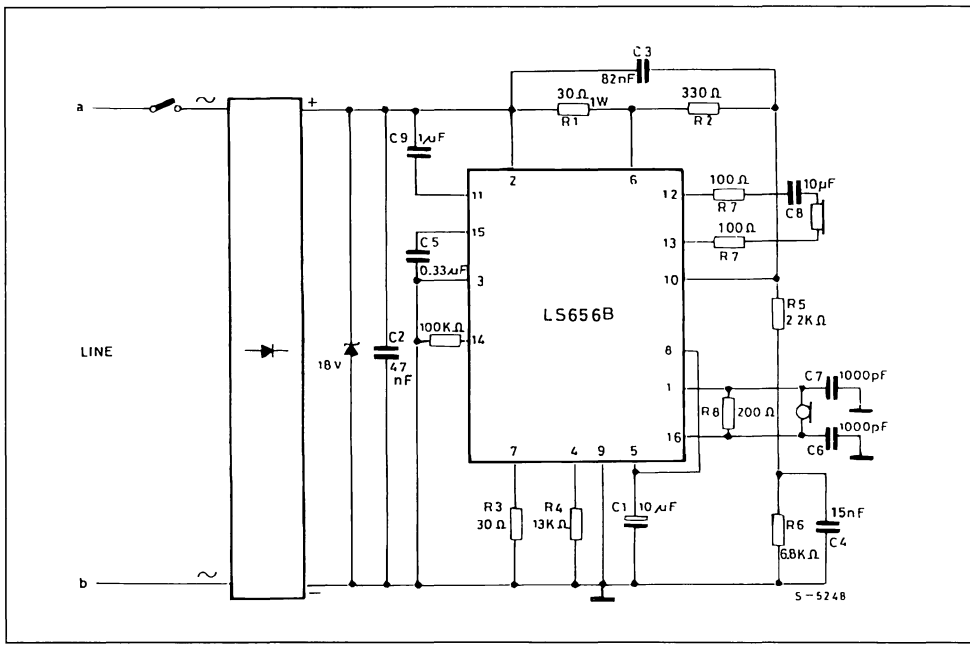


Figure 14 : Application Circuit with Gain Controlled by Line Voltage (french standard).

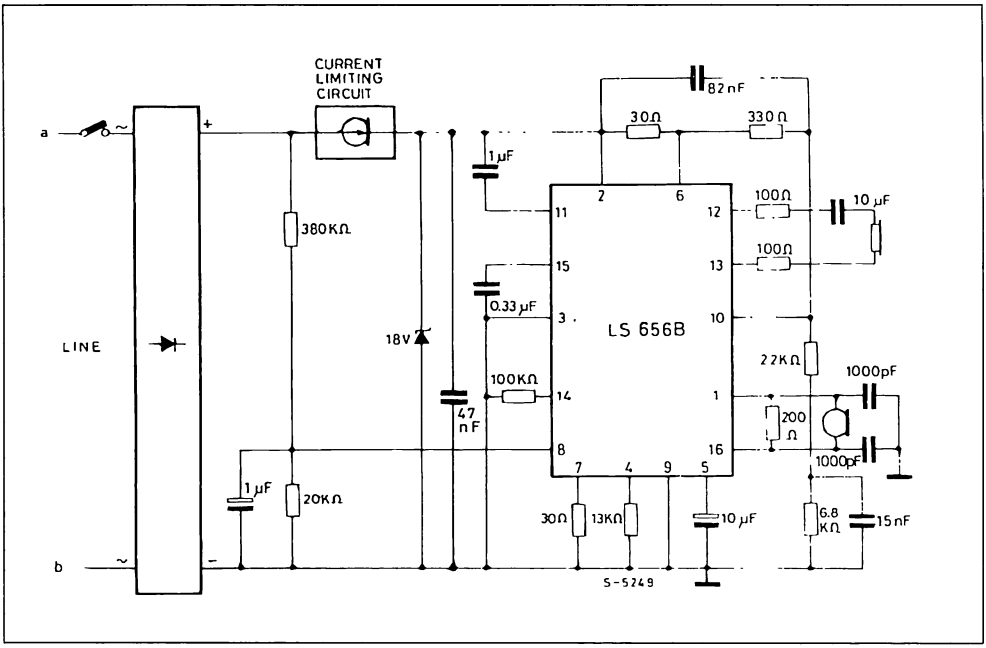
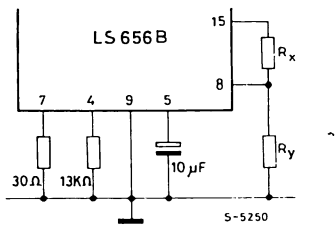
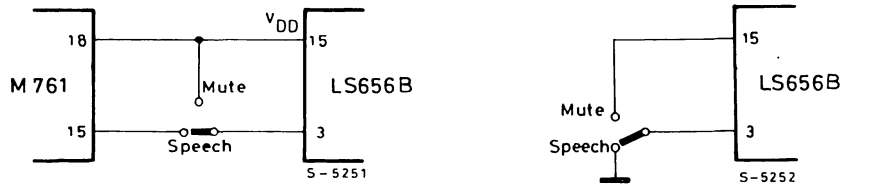


Figure 15 : Application Circuit with Fixed Gain Operation.



Ry = 0 Main gain condition
Rx = 0 Main gain condition

Figure 16 : External Mute Function.



a) with multifrequency

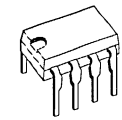
b) without multifrequency

In addition to the above mentioned applications, different values for the external components can be used in order to satisfy different requirements.
The following table (refer to the application circuit of fig. 10) can help the designers.

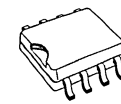
Component	Value	Purpose	Note
R1	30Ω	Bridge Resistors	R1 controls the receiving gain. When high current values are allowed, R1 must be able to dissipate up to 1 W. The Ratio R2/R1 fixes the amount of signal delivered to the line. R1 helps in fixing the DC characteristics (see R3 note).
R2	330Ω		
R3	30Ω	Line Current Sensing Fixing DC Characteristic	The relationships involving R3 are : $Z_{ML} = (20\ R3//Z_B) + R1$, $G_S = K \cdot \frac{Z_L//Z_{ML}}{R_3}$ and $V_L = (I_L - I_O)(R3 + R1) + V_O$; $V_O = 3.7V$ Without any problem it is possible to have a Z_{ML} ranging from 600 up to 900Ω. As far as the power dissipation is concerned, see R1 note.
R4	13kΩ	Bias Resistor	The suggested value assures the minimum operating current. It is possible to increase the supply current by decreasing R4 (they are inversely proportional), in order to achieve the shifting of the AGC starting point. (see fig. 16). After R4 changement, so
R5	2.2kΩ	Balance Network	It's possible to change R5 and R6 values in order to improve the matching to different lines ; in any case : $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$, $Z_B = R5 + R6//X_{C4}$
R6	6.8kΩ		
R7-R7'	100Ω	Receiver Impedance Matching	R7 and R7', must be equal ; the suggested value is good for matching to dynamic capsule ; there is no problem in increasing and decreasing (down to 0Ω) this value. A DC decoupling must be inserted when low resistance levels are used to stop
R8	200Ω	Microphone Impedance Matchin	
C1	10µF	Regulator AC byPass	A value greater than 10 µF gives a system start time too high for low current line during MF operation ; a lower value gives an alteration of the AC line impedance at low frequency.
C2	47nF	Matching to a Capacitive Line	C2 changes with the characteristics of the transmission line.
C3	82nF	Receiving Gain Flatness	C3 depends on balancing and line impedance versus frequency.
C4	15nF	Balance Network	See note for R5, R6.
C5	0.33µF	DC Filtering	The C5 range is from 0.1 µF to 0.47 µF. The lowest value is ripple limited, the higher value is starting up time limited.
C6-C7	1000pF	RF byPass	
C8	100µF	Receiving Output DC Decoupling	See note for R7, R7.
C9	1 µF	Receiving Input DC Decoupling	

ELECTRONIC TWO - TONE RINGER

- LOW CURRENT CONSUMPTION, IN ORDER TO ALLOW THE PARALLEL OPERATION OF 4 DEVICES
- INTEGRATED RECTIFIER BRIDGE WITH ZENER DIODES TO PROTECT AGAINST OVERVOLTAGES
- LITTLE EXTERNAL CIRCUITRY
- TONE AND SWITCHING FREQUENCIES ADJUSTABLE BY EXTERNAL COMPONENTS
- INTEGRATED VOLTAGE AND CURRENT HYSTERESIS



Minidip



SO8

DESCRIPTION

LS1240 and LS1240A are monolithic integrated circuits designed to replace the mechanical bell in telephone sets in connection with an electro-acoustical converter. Both devices can drive directly a piezoceramic converter (buzzer).

The output current capability of LS1240A is higher than LS1240. For driving a dynamic loudspeaker LS1240 needs a transformer, while LS1240A, needs a decoupling capacitor.

No current limitation is provided on the output stage of LS1240A, so a minimum load DC of 50 Ω is adviced.

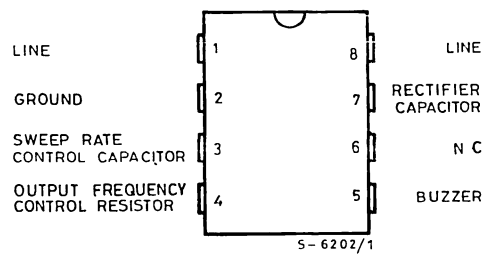
The two tone frequencies generated are switched by an internal oscillator in a fast sequence and made audible across an output amplifier in the loudspeaker, both tone frequencies and the switching frequency can be externally adjusted.

ORDERING NUMBERS

Minidip	SO8
LS1240 LS1240A	– LS1240AD1

The supply voltage is obtained from the AC ring signal and the circuit is designed so that noise on the line or variations of the ringing signal cannot affect correct operation of the device.

PIN CONNECTION (top view)



BLOCK DIAGRAM

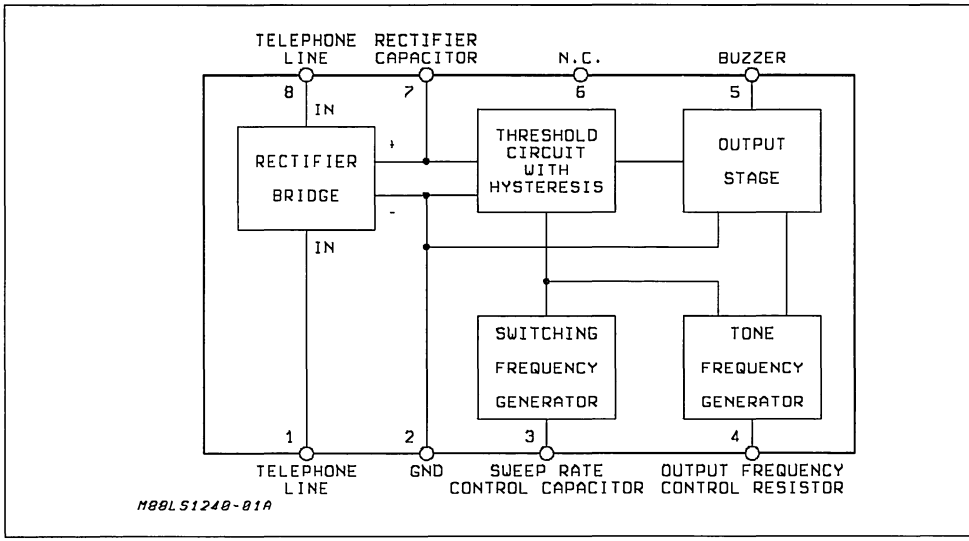
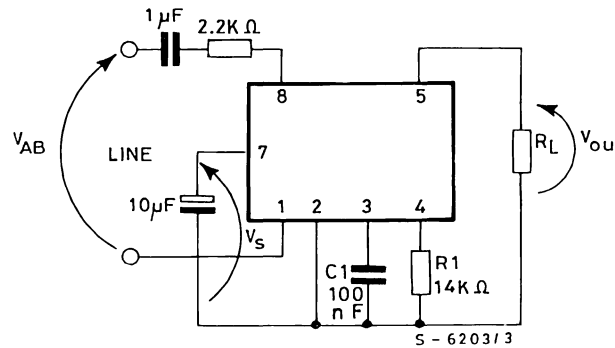


Figure 1 : Test Circuit.



$$R1 = \frac{2.72 \cdot 10^4}{f1\ (Hz)} \cdot (1 - 0.04 \ln \frac{f1}{1943}) \qquad f2 = 0.725\ f1 \qquad f_{SWEEP} = \frac{750}{C1\ (nF)}$$

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{AB}	Calling Voltage (f = 50 Hz) Continuous	120	V_{rms}
V_{AB}	Calling Voltage (f = 50 Hz) 5s ON/10s OFF	200	V_{rms}
DC	Supply Current	30	mA
T_{op}	Operating Temperature	– 20 to + 70	°C
T_{stg}	Storage and Junction Temperature	– 65 to + 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25 °C; V_S = applied between pins 7-2 unless otherwise specified)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage					26	V
I_B	Current Consumption without Load (pins 8-1)		$V_{8\text{-}1}$ = 9.3 to 25 V		1.5	1.8	mA
V_{ON}	Activation Voltage	LS1240 LS1240A		12.2 12		13.2 13.5	V V
V_{OFF}	Sustaining Voltage	LS1240 LS1240A		8 7.8		9 9.3	V V
R_D	Differential Resistance in OFF Condition (pins 8-1)			6.4			kΩ
V_{OUT}	Output Voltage Swing				V_S – 5		V
I_{OUT}	Short Circuit Current (pins 5-2)	LS1240 LS1240A	V_S = 20V R_L = 0Ω R_L = 250Ω		35 70		mA mA

AC OPERATION

f_1 f_2	Output Frequencies f_{out1} f_{out2}	V_S = 26V, R_1 = 14kΩ V_S = 0 V V_S = 6V	1.74 1.22		2.14 1.6	kHz
	$\frac{f_{OUT1}}{f_{OUT2}}$		1.33		1.43	
	Programming Resistor Range		8		56	kΩ
f_{SWEEP}	Sweep Frequency	R_1 = 14kΩ, C_1 = 100nF	5.25	7.5	9.75	Hz

Figure 2 : Typical Application for LS1240 and LS1240A

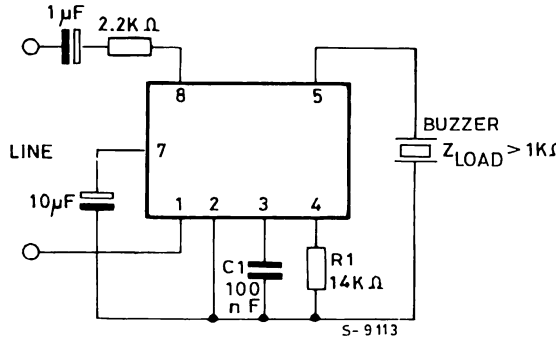
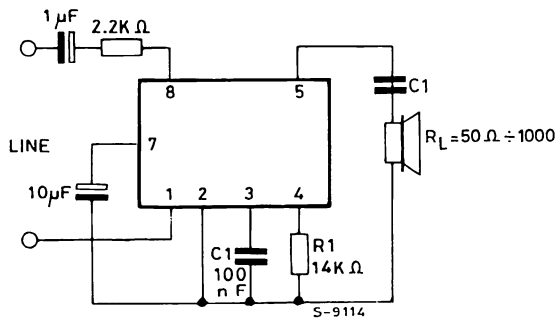


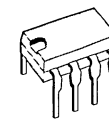
Figure 3 : Typical Application for LS1240A only.



C_1 such that $|Z_{LOAD}| > 1\ K\Omega$

ELECTRONIC TWO - TONE RINGER

- LOW CURRENT CONSUMPTION, IN ORDER TO ALLOW THE PARALLEL OPERATION OF A DEVICE
- INTEGRATED RECTIFIER BRIDGE WITH ZENER DIODES TO PROTECT AGAINST OVER VOLTAGES
- LITTLE EXTERNAL CIRCUITRY
- TONE AND SWITCHING FREQUENCIES ADJUSTABLE BY EXTERNAL COMPONENTS
- INTEGRATED VOLTAGE AND CURRENT HYSTERESIS



Minidip

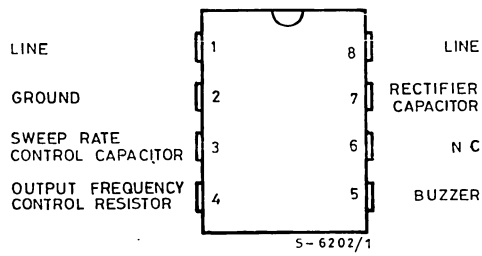
ORDERING NUMBER : LS1241

DESCRIPTION

LS1241 is a monolithic integrated circuit designed to replace the mechanical bell in telephone sets, in connection with an electro acoustical converter. The device can drive either directly a piezo ceramic converter (buzzer) or a small loudspeaker. In this case a transformer is needed. The two tone frequencies generated are switched by an output amplifier in the loudspeaker ; both tone frequencies and the switching frequency can be externally adjusted.

The supply voltage is obtained from the AC ring signal and the circuit is designed to that noise on the line or variations of the ringing signal cannot affect correct operation of the device.

PIN CONNECTION (top view)



BLOCK DIAGRAM

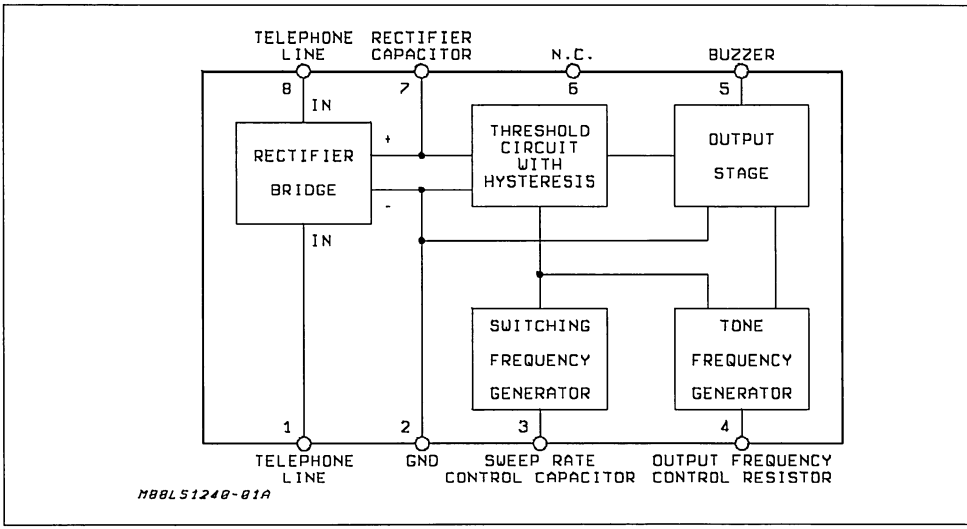
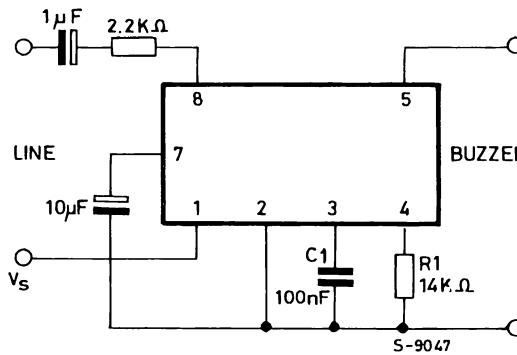


Figure 1 : Test Circuit.



$$f_1 = \frac{1.90 \cdot 10^4}{R\ (K\Omega)} \qquad f_2 = \frac{4}{5}\ f_1 \pm 4\ \% \qquad f_{SWEEP} = \frac{750}{C1\ (nF)}$$

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{AB}*	Calling Voltage (f = 50Hz) Continuous	120	V_{RMS}
V_{AB}*	Calling Voltage (f = 50Hz) 1.8s ON/3.6s OFF	200	V_{RMS}
DC	Supply Current	30	mA
T_{oper}	Operating Temperature	- 20 to + 70	°C
T_{stg}	Storage and Junction Temperature	- 65 to + 150	°C

* See test circuit of figure 1.

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C; V_S = applied between pins 7-2 unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage				26	V
I_B	Current Consumption without Load (pins 8-1)	$V_{8\text{-}1}$ = 9 to 25V		1.5	1.8	mA
V_{ON}	Activation Voltage		12.2		13.2	V
V_{OFF}	Sustaining Voltage		8		9	V
R_D	Differential Resistance in OFF Condition (pins 8-1)		6.4			kΩ
V_{OUT}	Output Voltage Swing			$V_s - 5$		V
I_{OUT}	Short Circuit Current (pins 5-2)	V_s = 20V		35		mA

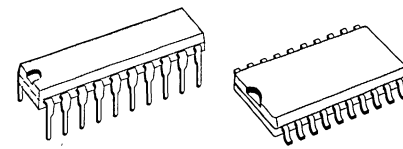
AC OPERATION

f_1 f_2	Output Frequencies f_{out1} f_{out2}	V_S = 26V, R_1 = 14kΩ V_3 = 0V V_3 = 6V	 1.21 0.93		 1.5 1.25	kHz
	$\frac{f_{OUT1}}{f_{OUT2}}$		1.2		1.3	
	Programming Resistor Range		5		50	kΩ
F_{SWEEP}	Sweep Frequency	R_1 = 14kΩ, C_1 = 100nF	5.25	7.5	9.75	Hz

SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

PRELIMINARY DATA

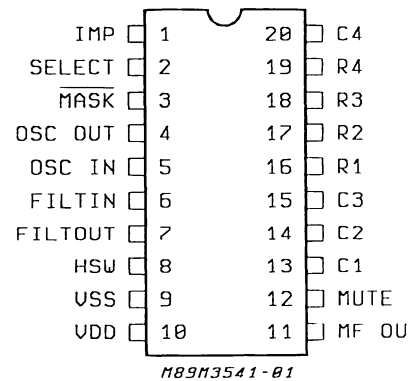
- SELECTABLE LOOP DISCONNECT OR DTMF DIALLING MODES
- ALLOWS USER TO SWITCH FROM LD TO DTMF DIALLING DURING A CALL
- LNR FACILITY ALLOWS UP TO 31 DIGITS TO BE RETAINED FOR REDIALLING
- SELECTABLE MAKE/BREAK RATIOS 2:1 AND 3:2
- SELECTABLE INTERDIGIT PAUSE 500ms OR 800ms
- USES INEXPENSIVE 560KHz RESONATOR
- TIMED BREAK RECALL (timed flash)
- OPERATES WITH INEXPENSIVE SINGLE CONTACT KEYPAD
- CAPABLE OF BATTERY-LESS OPERATION. LOW POWER CMOS PROCESS ALLOWS DIRECT OPERATION FROM TELEPHONE LINES



DIP20 **SO20**

ORDERING NUMBERS :
M3541B/1 M3541D

PIN CONNECTION (Top view)



M89M3541-01

DESCRIPTION

The M3541 is a keypad switchable LD/DTMF dialer devices designed for use in low cost, dual dialing mode telephone instruments. It is suitable for sending telephone numbers without limit and an on-chip memory allows numbers of up 31 digits to be retained for redialling later. The low power CMOS design allows the number in the memory to be maintained indefinitely (until overwritten) by a minimal current leaked from the telephone line. A particular feature of this device is the facility for the user to switch dialling mode from LD to DTMF via the keypad during the course of a call. This is intended for uses such as home banking, access to long distance trunk service, credit card verificatios and other applications which require data to be sent at low speed once a connection has been established.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Supply Voltage V_{DD} - V_{SS}	– 0.3		6.5	V
	Voltage on any Pin Except HSW Voltage on any Pin HSW (current limited to < 100µA)	V_{SS} – 0.3 V_{SS} – 0.3		V_{DD} + 0.3	V V
	Current at any Pin Except FILTOUT and FILTIN Current at Pin FILTIN Current at Pin FILTOUT	– 1 0 – 5		+ 1 0.1 0	mA mA mA
	Operating Temperature Storage Temperature	– 10 – 55		+ 55 + 125	°C °C

* Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum ratings for extended periods may affect device reliability.

D. C. ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage - Off-hook	2.4		5.7	V
I_{DD}	Supply Current - On-hook at 3.0V Supply Current - Off-hook (idle)			1 1	µA µA
	Supply Current - MF tone sending Supply Current - LD impulsing			1.0 200	mA µA
V_{HSW}	Hookswitch Input - On-hook Hookswitch Input - Off-hook	 0.8 V_{DD}		0.2 V_{DD}	
V_{OH} V_{OL}	$\overline{MASK}$, MUTE and IMP Outputs, Load – 1mA MASK, MUTE and IMP Outputs, Load + 1mA	2.2		 0.3	V V
	MF OUT D.C. Level During Tone Sending		0.9 V_{DD}		
	MF OUT Output Resistance		3		kΩ
GDP	Darlington Pair Current Gain at I_E = 100µA, V_{CE} = 2V	600			
R_{ON}	"Key not Pressed" Resistance			2	kΩ
R_{OFF}	"Key not Pressed" Resistance	500			kΩ

A. C. ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{TONE}	Tone Amplitude Low Group Tone Amplitude High Group } no Load	57	64 81	 91	mV_{RMS} mV_{RMS}
GAR	Ratio of High to Low Group Amplitude	1.5	2	2.5	dB
	Total Harmonic Distortion 0 - 4kHz 0 - 10kHz 0 - 50kHz 0 - 200kHz		 2 2.5 5 6.5	 10	 % % % %
t_{TBR}	Time Break Recall (FLASH)		100		ms

PIN FUNCTIONS

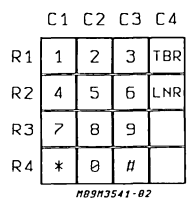
Pin Name	Function
ROW 1 ROW 2 ROW 3 ROW 4 COL 1 COL 2 COL 3 COL 4	Connections for 16 Buttons, Single Contact Keyboard
V_{DD}	Positive Supply
V_{SS}	Negative Supply
SELECT	LD/MF Selection, IDP and B/M Ratio Programming
OSCIN - OSCOUT	Oscillator Connection
HSW	Hookswitch. A logic '1' voltage at this pin is used to indidcate 'off-hook'.
$\overline{MASK}$	Output to disable speech circuit during pulse dialling and recall (see note 1).
IMP	'Loop Disconnect' Dialling Output
MF OUT	Unfiltered, Dual Tone Output
FILTOUT - FILTIN	Unity Gain Amplifier Input and Output for 2-pole Filter
MUTE	Output Active During Keying and Tone Transmission (see note 2)

Notes : 1. The $\overline{MASK}$ output may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook, during a TBR (Timed Flash) operation or for LD dialling.
2. The MUTE output is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

KEYPAD OPERATION

The device will accept keypad inputs only in the 'off-hook' condition when the key is pressed for more than 14ms. Any key pressed during the 'on-hook' condition will be ignored and the oscillator inhibited. This ensures that the current drain 'on-hook' is low and used only for memory retention.

KEYPAD FORMAT



LNR = Redial digits in "LNR"store
TBR = Timed Break Recall (timed flash)

LD/DTMF MODE SELECTION

The initial dialling mode after the telephone goes off-hook is determined as follows :

DTMF - Connect SELECT pin to V_{DD}

LD - .

Option		Connect SELECT pin to :
IDP	B/M Ratio	
800ms	2:1	V_{SS}
500ms	2:1	COL 1
500ms	3:2	COL 2
800ms	3:2	COL 3

LD dialling is at 10 i.p.s. for all options

KEYPAD LD/DTMF MODE CHANGE

If the initial dialling mode is LD, pressing either the * or # key will cause all subsequently entered digits to be dialled in DTMF. The first press of either * or # will not cause a digit to be dialled, but once in MF mode, pressing * or # will cause the appropriate tone pair to be transmitted.

If the TBR (Timed Flash) key is pressed, or an Earth Loop Recall operation is signalled to the chip, further dialling is set to the initial mode.

LAST NUMBER REDIAL

The function of the Last Number Redial store is to automatically retain the last number dialled so that it can be redialled later simply by pressing the LNR key. Either LD or MF numbers will be retained in the store. When numbers containing an LD part followed by an MF part are dialled, only the LD part will be retained in order that security codes, etc., dialled in MF are not automatically stored.

To redial a number, go off-hook and press LNR once. Alternatively, digits may be keyed manually before LNR is pressed. If the digits keyed correspond with the first digits in the LNR store, the remaining digits will be automatically redialled when LNR is pressed (this feature allows manual keying of an access code followed by a pause before dialling out the rest of the number). If, however, a digit is keyed which differs from the corresponding digit in the stored number, then redialling is inhibited.

HOOKSWITCH OPERATION

The hookswitch input is used to inform the M3541 of whether the telephone is on- or off-hook. When the telephone is on-hook the M3541 will adopt a static low power mode in which dialling functions are inhibited and only a minimal current is consumed to maintain the store contents.

The M3541 recognizes the on-hook condition when the hookswitch input (HSW) goes from logic '1' (the off-hook condition) to logic '0' for greater than 300ms. Short line voltage interruptions of less than 200ms, such as those created by the exchange during connection, will not be recognized by the M3541 as an on-hook indication.

The MASK output will go to logic '0' instantly whenever, and for as long as, the hookswitch input is at logic '0' in order to disconnect the speech circuit. This conserves current so that the store contents are not lost.

POWER-ON RESET

A Power-on Reset is internally generated when power is applied to the chip and causes the number store to be cleared.

LOOP DISCONNECT MODE

In this mode the $\overline{\text{MASK}}$ output is used to disable the speech circuit during dialling. The $\overline{\text{MASK}}$ output is logic '0' during impulsing and interdigit pauses.

The IMP output signals a break to line when at logic '0' (VSS). Make periods and I.D.P. times are signalled by logic '1' on the output. During the non-dialling period the impulsing output is at logic '0'. Timing of the output is shown below.

Figure 1 : Timing Diagram

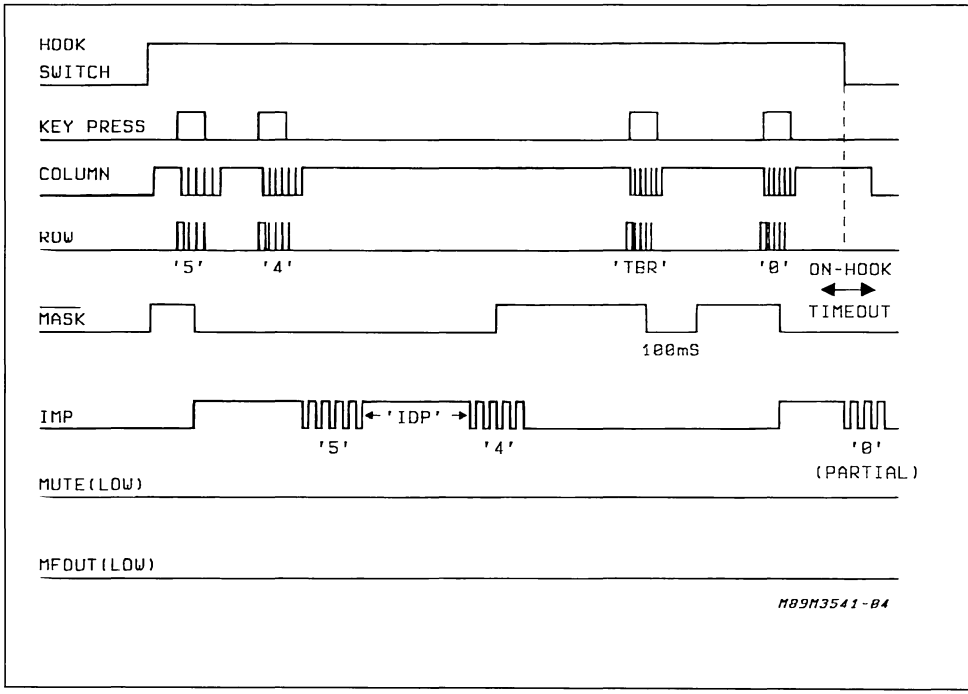
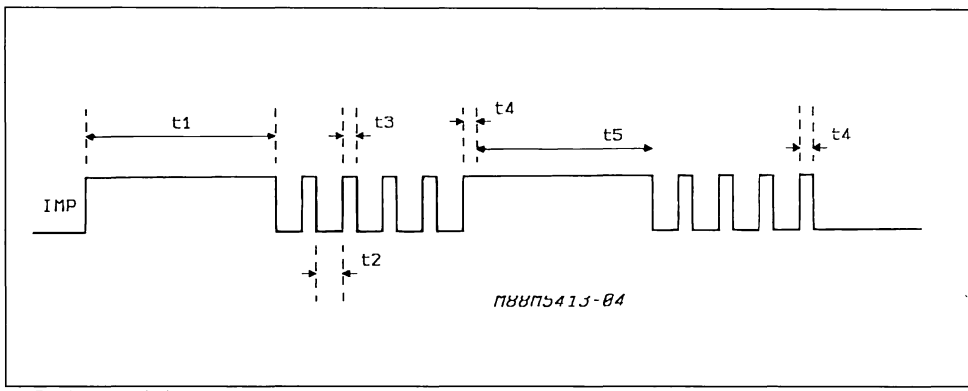


FIgure 2 : Timing Data



t_1 = Pre-digit pause (=t_5)
t_2 = Break period (60ms or 67ms)
t_3 = Make period (40ms or 33ms)
t_4 = Post-digit make (= t_3)
t_5 = Inter-digit pause (500 or 800ms)

DTMF MODE

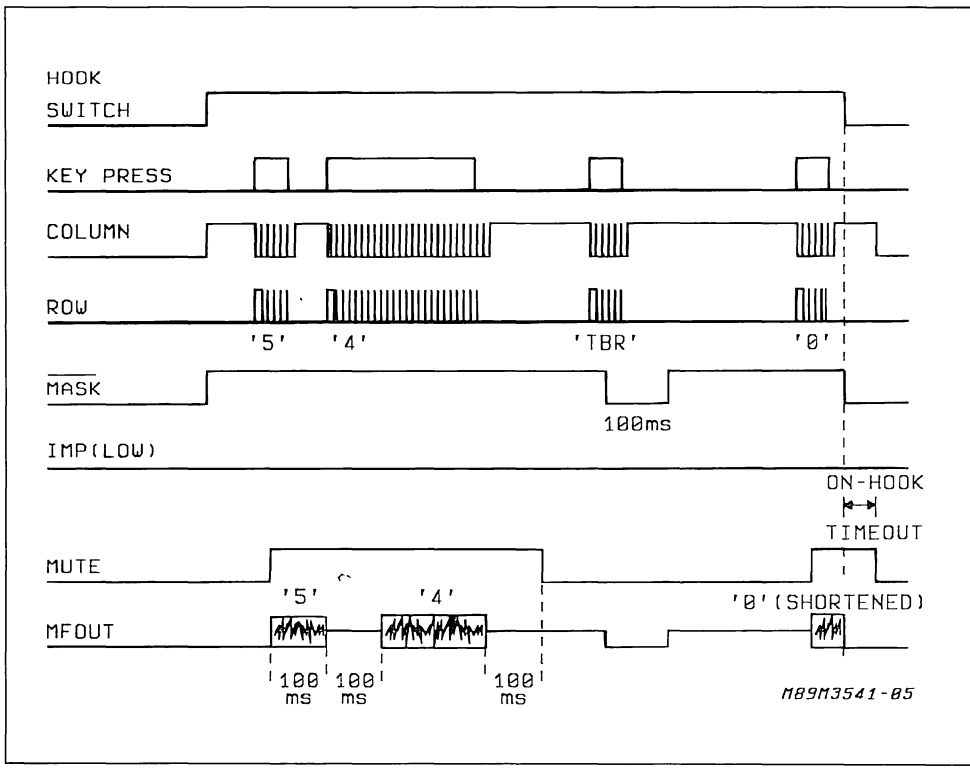
The MUTE output goes to logic '1' when a key is activated and remains active for the duration of the tone transmission.
The tone rate will be 100ms on, 100ms off minimum.

TONE FREQUENCIES

Keypad	R1	R2	R3	R4	C1	C2	C3
Nominal Frequency (Hz)	697	770	852	941	1209	1336	1477
Deviation from Nominal (%)	– 0.07	– 0.10	+0.19	– 0.15	– 0.17	– 0.20	– 0.22

There will be an additional error due to the deviation of the oscillator frequency from 560KHz.

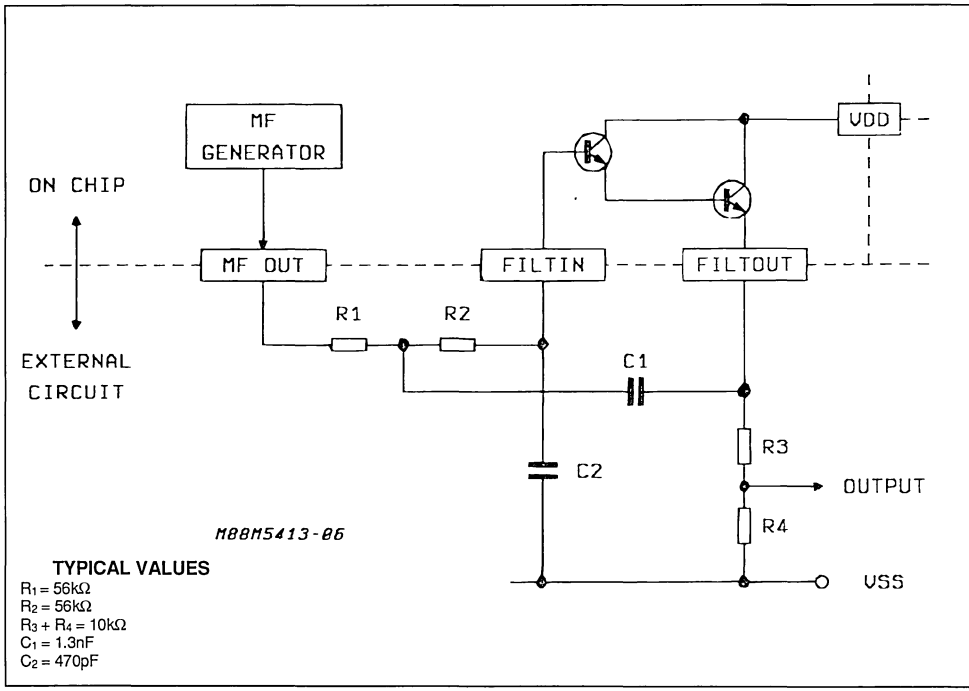
Figure 3 : Timing Diagram.



TONE OUTPUT

Facility has been made for tone filtering as shown below. This also allows the user to adjust tone amplitudes as required. The tone amplitude is proportional to the chip supply voltage, V_{DD}, and can be adjusted by changing the ratio of R3 and R4.

Figure 4.



The filter components shown have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz. The pass-band insertion loss is nominally 0.5dB.

DTMF APPLICATION CIRCUITS

The DTMF circuit in figure 5 uses a constant current supply and a 2.5V reference diode to produce the stabilised supply voltage which determines the MF tone level of the M3541. If the speech circuit provides a stabilised voltage, then figure 6 shows how it may be used to power the M3541. Diode D1 prevents the speech circuit from taking current whilst the telephone is on-hook, and D2 compensates for the voltage dropped across D1 when off-hook.

Figure 5.

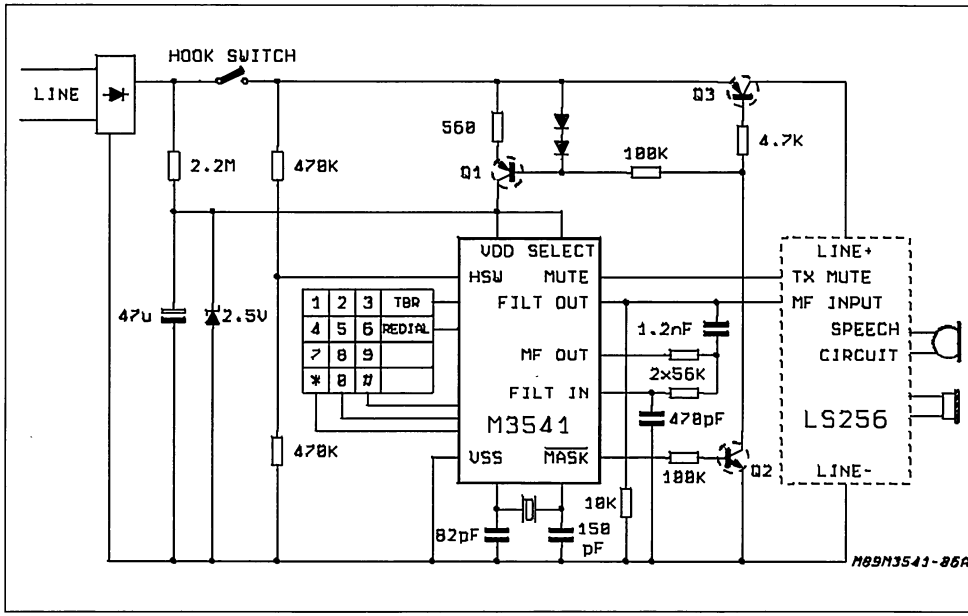
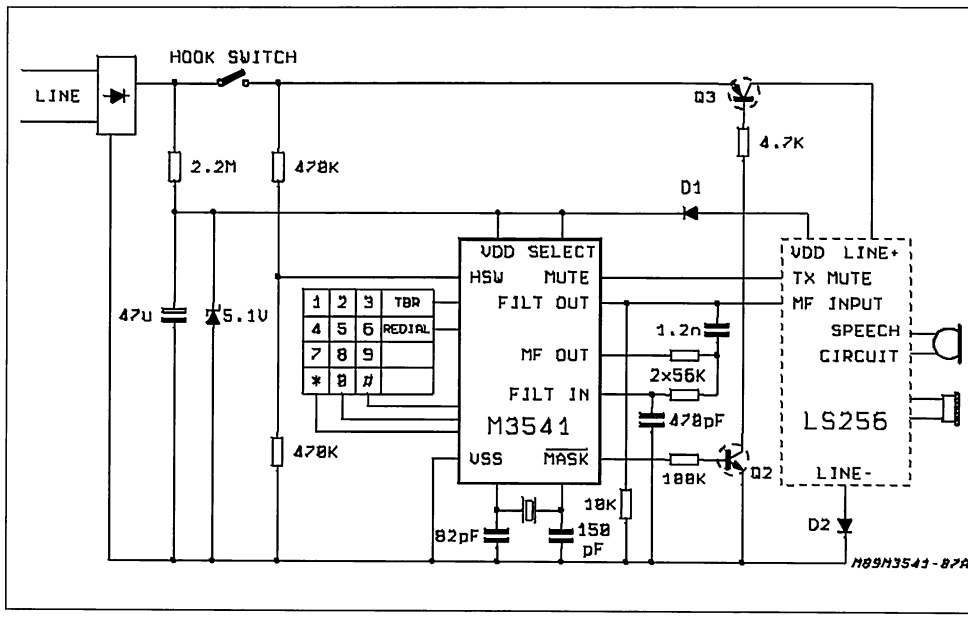


Figure 6.



SWITCHABLE LD/MF APPLICATION CIRCUITS

The circuit in figure 7 uses a constant current supply to take current from the telephone line which is used to power the M3541. The 2.5V reference diode produces a stabilised supply voltage which determines the MF tone level of the M3541.
In figure 8, a stabilising voltage from the speech is used to supply the M3541 during MF dialling to give accurate tone levels.

The M3541 is powered via the 150K resistor during TBR operations and LD dialling breaks, and via Q1 during dialling makes. This configuration minimises the component count at the expense of allowing a leakage current of about 450µA during dialling breaks. The 47µF reservoir capacitor maintains and smooths the supply to the chip.

Figure 7.

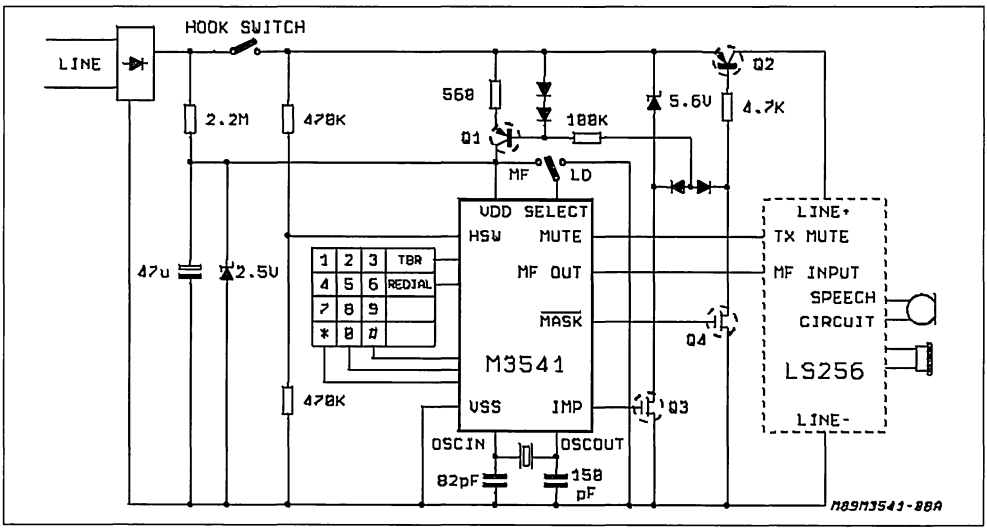
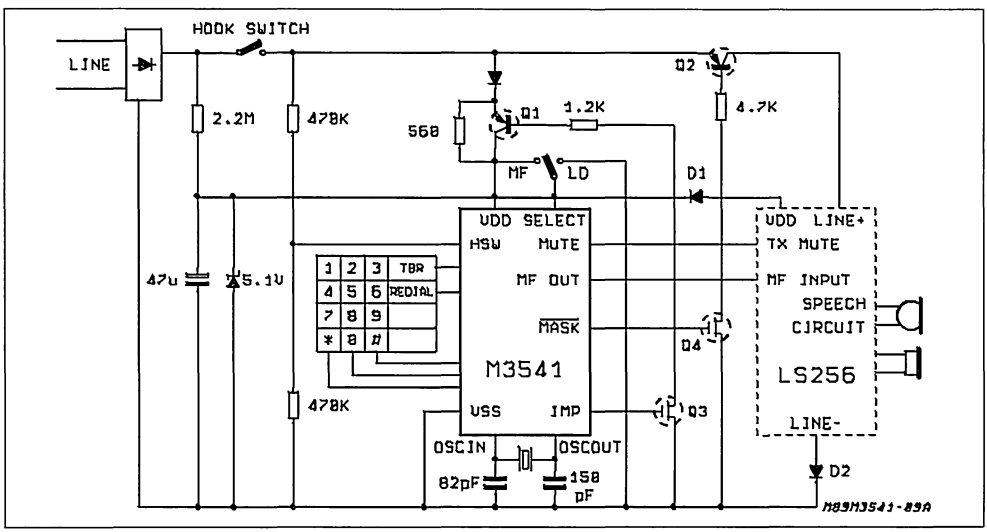


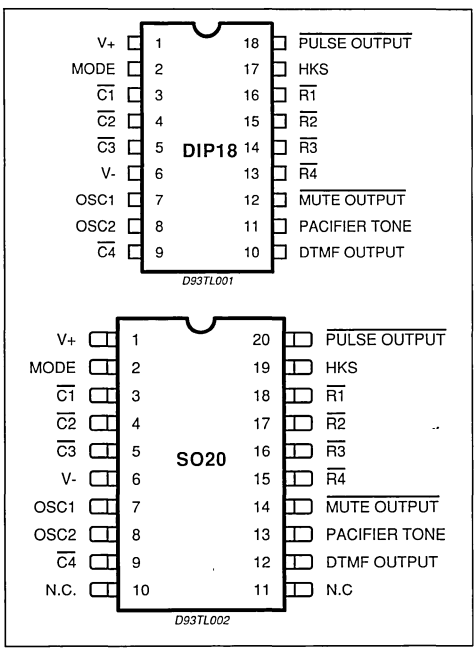
Figure 8.

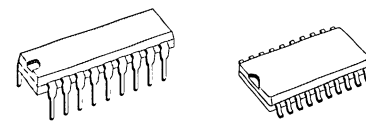


SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

- SINGLE CHIP DTMF AND PULSE DIALER
- SOFTSWITCH CHANGES SIGNALING MODE FROM PULSE TO TONE
- RECALL OF LAST NUMBER DIALED (up to 28 digits long)
- FLASH KEY INPUT INITIATES TIMED HOOK FLASH
- TIMED PABX PAUSE
- 8 TONES PER SECOND DIALING IN TONE MODE AND 10 PPS IN PULSE MODE
- DTMF ACTIVE UNTIL KEY RELEASE
- MINIMUM DTMF DURATION/SEPARATION GUARANTEED (74/54ms)
- PACIFIER TONE PROVIDES AUDIBLE INDICATION OF VALID KEY INPUT FOR NON-DTMF KEY ENTRIES
- POWERED FROM TELEPHONE LINE, LOW OPERATING VOLTAGE FOR LONG LOOP APPLICATIONS

Figure 1 : Pin Connections (top view).





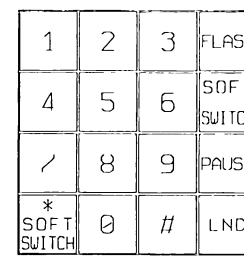
DIP18 SO20

ORDERING NUMBERS : MK53731N00 (DIP18)
MK53731D (SO20)

DESCRIPTION

The MK53731 is a Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialling. The MK53731 buffers up to 28 digits into memory that can be later redialed with a single key input. This memory capacity is sufficient for local, long distance, overseas, and even computurized long-haul networks Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include : Last Number Dialled (LND), Softswitch, Flash and Pause. Figure 2 shows the keypad configuration.
A LND key input automatically redials the last number dialled.
Two features simplify PABX dialling. The PAUSE key stores a timed pause in the number sequence. Redial is then delayed until a outside line can be accessed or some other activity occurs before normal signalling resumes. The FLASH key simulates a 560ms hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

Figure 2 : Keypad Configuration.



FUNCTIONAL PIN DESCRIPTION (DIP18 only)

V+

Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (see Electrical Specifications).

MODE

Input. Pin 2. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V–), the default determines the signaling mode. A V+ connection defaults to tone mode operation and a V– connection defaults to pulse mode operation.

When dialling in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key, or softswitch, is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$

Keyboard inputs. The MK53731 interfaces with either the standard 2-of-8 with negative common or the single-contact (Form A) keyboard.

A valid keypad entry is either a single Row connected to a single Column or V– simultaneously presented to both a single Row or Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (T_{KD}) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 17 to pin 1), the keyboard inputs are pull high through on-chip pull-up resistors.

In the tone mode, if 2 or more keys in the same row or if 2 or more keys in the same column are depressed a single tone will be output. The tone will corres-pond to the row or column for which the 2 keys were pushed. This feature is for test purposes, and single tones will not be redialed.

Also in the tone mode, the output tone is continuous in manual dialing as long as the key is pushed. The output tone duration follows the table 1.

Table 1. Output Tone Duration.

Key – Push Time, T*	Tone Output *
$T \leq 32ms$	No Output, Ignored by MK53731.
$32ms \leq T \leq 75ms + T_{DK}$	75ms Duration Output
$T \geq 75ms + T_{KD}$	Output Duration = $T - T_{KD}$

* **Note :** T_{KD} is the keypad debounce time which is typically 32 ms.

When redialing in the tone mode, each DTMF output is 75 ms duration, and the tone separation (intersignal delay) is 50 ms.

V–

Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2

Pin 7 (input), pin 8 (output). OSC1 and OSC2 are connections to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ± 0.25 % may also be used.

DTMF OUTPUT

Output. Pin 10. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 7 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK53731 is designed to operate from an unregulated supply ; the TONE LEVEL is supply independent, and the single row tone output level will be typically :

$$T_{01} = -12 \text{ dBm} \pm 1 \text{ dB}$$

The DC component of the DTMF output while active is described by the following equation :

$$V_{DC1} = 0.3 \times V+ + 0.5V$$

Figure 3 : MK53731 Block Diagram.

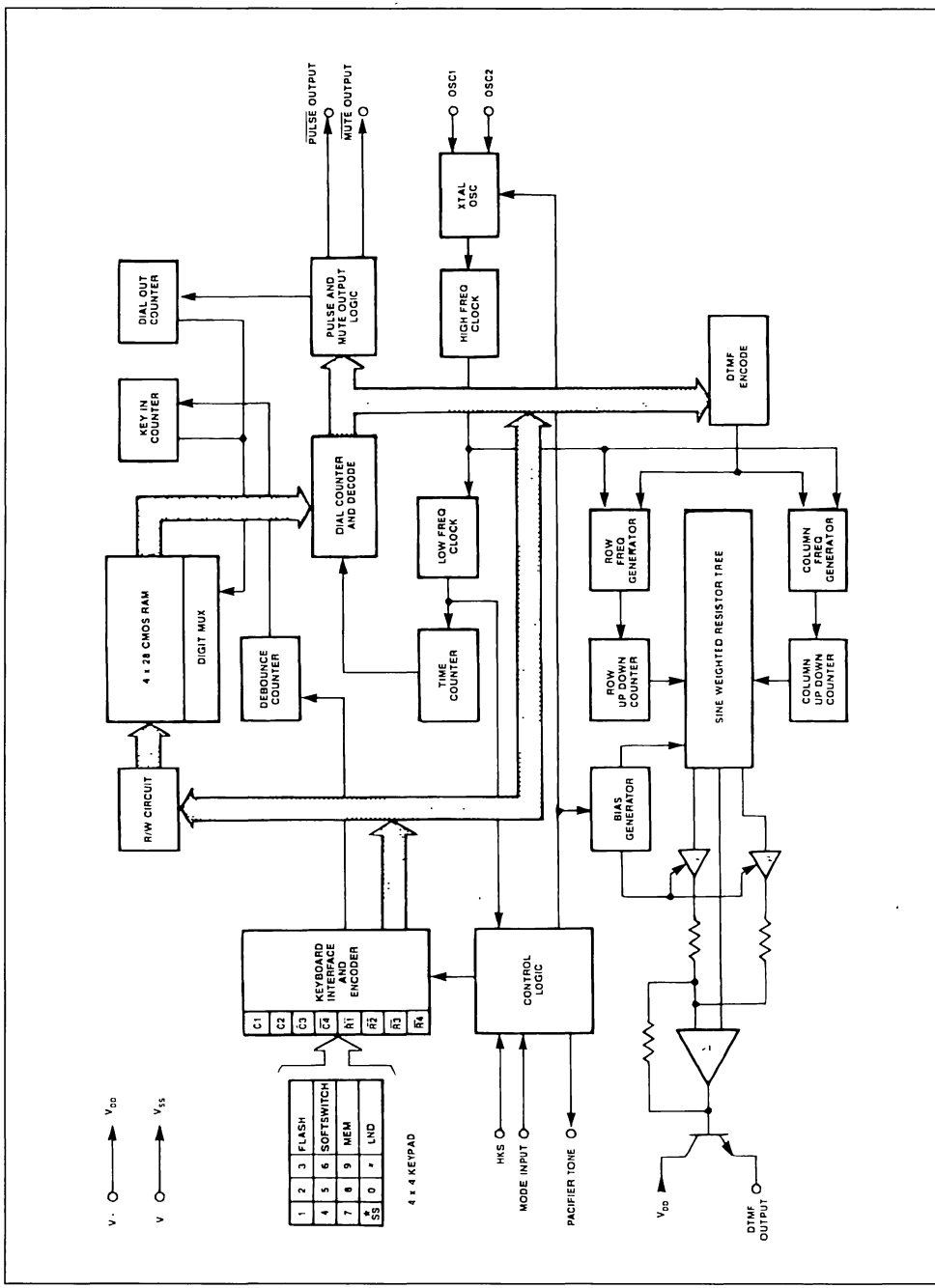


Figure 4 : Typical Single Tone.

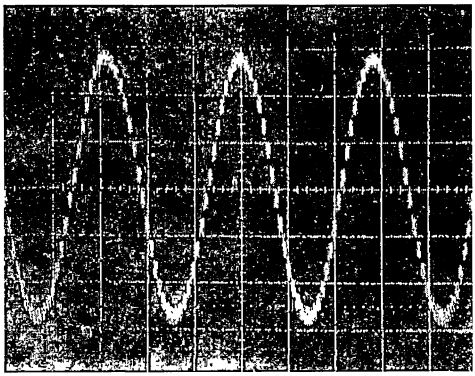


Figure 5 : Typical Dual Tone.

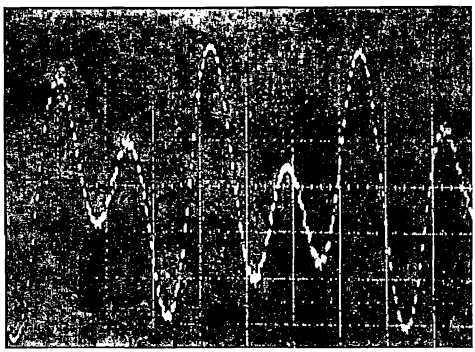
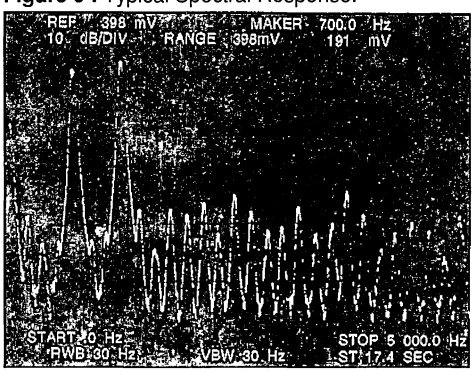


Figure 6 : Typical Spectral Response.



PACIFIER TONE

Output. Pin 11. A 500Hz square wave is activated upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all valid key entries activate the pacifier tone. In tone mode, any non-DTMF (FLASH, PAUSE, LND, SOFTSWITCH) entry activates the pacifier tone. The pacifier tone provides audible feedback, confirming that the key has been properly entered and accepted.

$\overline{\text{MUTE OUTPUT}}$

Output. Pin 12. This pin is the $\overline{\text{MUTE OUTPUT}}$ for both tone and pulse modes. Timing is dependent upon mode.

The $\overline{\text{MUTE OUTPUT}}$ consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In the tone mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE OUTPUT}}$ is active continuously until dialing is completed. $\overline{\text{MUTE OUTPUT}}$ goes active when any key is pushed.

In the pulse mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the receiver and the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE OUTPUT}}$ timing is shown in Figure 8 for pulse mode signaling and Figure 7 for tone mode signaling. $\overline{\text{MUTE OUTPUT}}$ is active during each digit, and not active during the interdigit time. In both tone and pulse modes, $\overline{\text{MUTE OUTPUT}}$ goes active 40 ms before PULSE OUTPUT for a FLASH.

HKS

Input. Pin 17. Pin 17 is the hookswitch input to the MK53731. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2. Figure 8 illustrates the timing for this pin.

$\overline{\text{PULSE OUTPUT}}$

Output. Pin 18. This is an output consisting of an open drain N-channel device. In either pulse or tone mode, the FLASH key will cause a 560 ms output pulse at pin 18.

DEVICE OPERATION (Tone Mode)

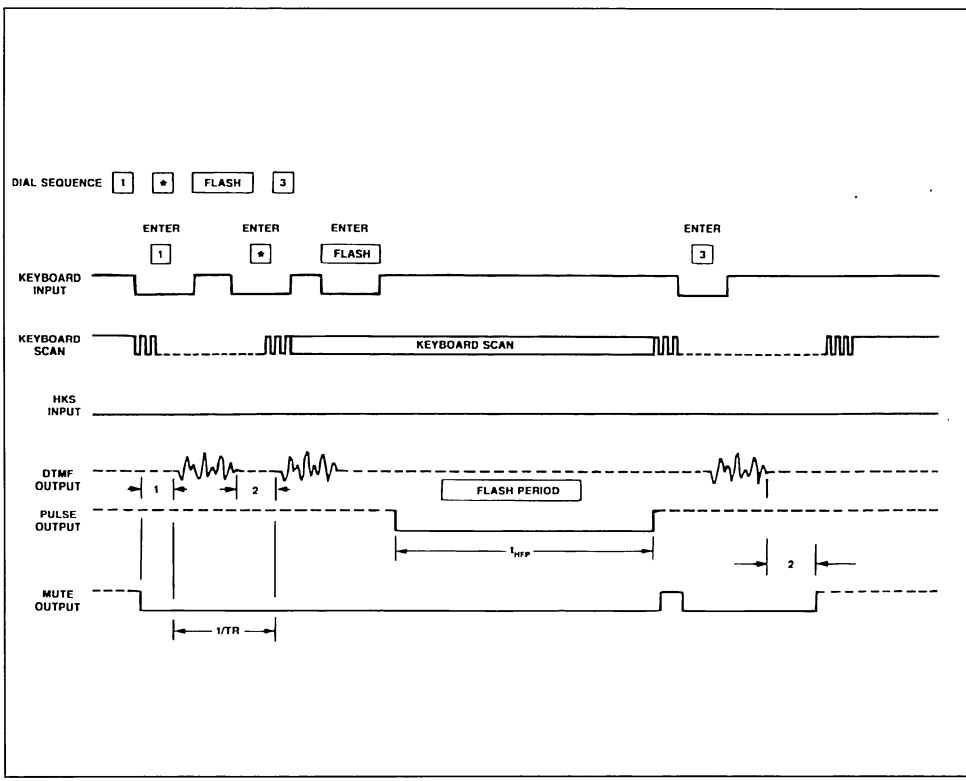
When the MK53731 is not actively dialing, it consumes very little current. While on-hook, all keypad input pins are internally pulled high. Row and Column inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of approximately 40 ms (measured from initial key closure). Output tone duration is shown in Table 2.

The MK5371 allows manual dialing of an indefinite number of digits, but if more than 28 digits are dialed, the 53731 will "wrap around". That is, the extra digits beyond 28 will be stored at the beginning of the LND buffer, and the first 28 digits will no longer be available for redial.

Table 2 : DTMF Output Frequency.

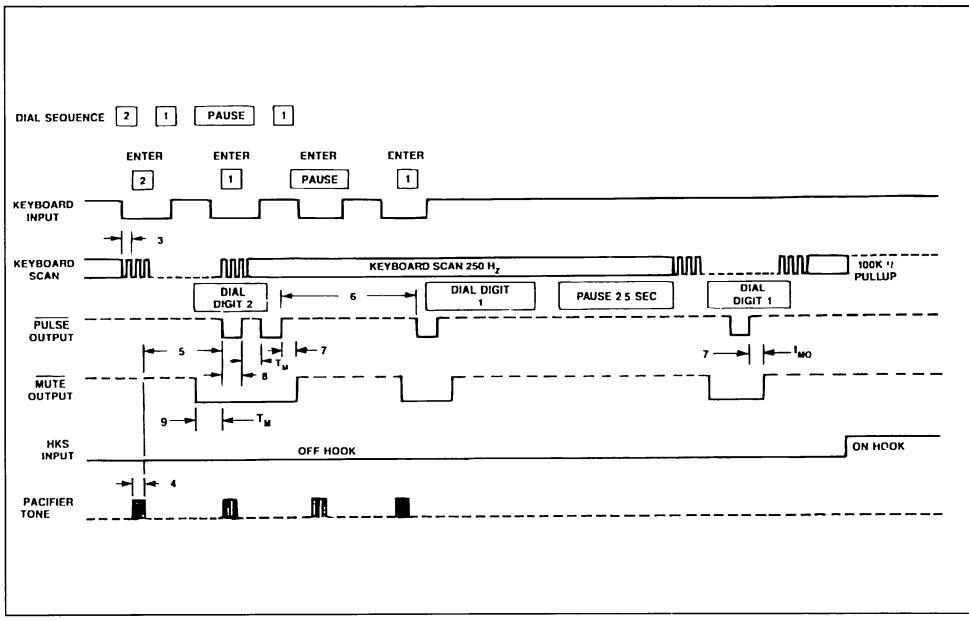
Key Input	Standard Frequency	Actual Frequency	% Deviation
ROW 1	697	699.1	+0.31
2	770	766.2	–0.49
3	852	847.4	–0.54
4	941	948.0	+0.74
COL 1	1209	1215.9	+0.57
2	1336	1331.7	–0.32
3	1477	1471.9	–0.35

Figure 7 : Tone Mode Timing.

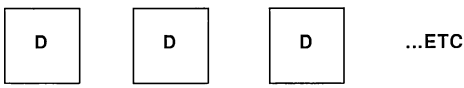


Note : For this example, key entries are ≤ 75 ms, but ≥ 32 ms.

Figure 8 : Pulse Mode Timing.



NORMAL DIALING (off-hook)

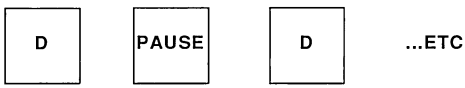


Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

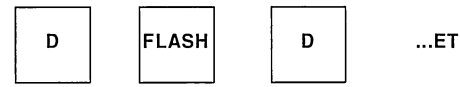
Last number dialing is accomplished by entering the LND key.

PAUSE



A pause may be entered into the dialed sequence at any point by keying in the special function key, PAUSE. Pause inserts a 1.1-second delay into the dialing sequence. The total delay, including pre-digital and post-digital pauses is shown in Table 3.

HOOK FLASH



Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed Break of 560 ms. The FLASH function is stored in memory, but it will not be redialed as such. When a FLASH key is pressed, no further key inputs will be accepted until the hookflash function (560 ms break) has been dialed. The key input following a FLASH will be stored as the initial digit of a new number (overwriting the number dialed prior to the FLASH) unless it is another FLASH. Consecutive FLASH entries after a number is dialed will be stored sequentially in the LND memory and a subsequent LND entry will cause the redial of that number with a delay, but not hookflash breaks, at the end of the redialing sequence. When redialing in tone mode, MUTE OUTPUT will remain active during the flash delay period.

SOFTSWITCH

When the dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever

the * key, or SOFTSWITCH, is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

Table 3 : Special Function Delays.

Each delay shown below represents the time required from after the special function key is depressed until a new digit can be dialed.

The time is considered "FIRST" key is all previous inputs have been completed dialed. The time is considered "AUTO" if in redial, or if previous dialing is still in progress.

Function	First/Auto	Delay (seconds)	
		Pulse	Tone
SOFTSWITCH	FIRST	1.15	
	AUTO	1.85	
PAUSE	FIRST	1.84	1.15
	AUTO	2.50	1.20

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC Supply Voltage	6.5	V
Operating Temperature	–20 to +60	°C
Storage Temperature	-55 to +125	°C
Maximum Power Dissipation @ 25°C	500	mW
Maximum Voltage on any Pin	(V+) +0.3, (V-) -0.3	V

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

DC Characteristcs

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	V+ TONE	DC Operating Voltage	2.5		6.0	V	
	V_{MR}	Memory Retention Voltage	1.5			V	1,6
	I_S	Stand-by Current		0.4	1.0	µA	1
	I_{MR}	Memory Retention Current		0.15	0.75	µA	5,6
	V_{MUTE}	Mute Output Operating Voltage	1.8			V	7
	I_T	Operating Current (Tone)		300	600	µA	2
	I_P	Operating Current (Pulse)		150	250	µA	2
	I_{ML}	Mute Output @ (2.5V)	1			mA	3
		Sink Current @ (4V)	3			mA	
	I_{PL}	Pulse Output Sink Current	1	2		mA	3
	I_{PC}	Pacifier Tone Sink/Source	250	500		µA	4
	K_{RU}	Keypad Pullup Resistance		100		KΩ	
	K_{RD}	Keypad Pulldown Resistance		500		Ω	
	V_{IL}	Keypad input Level - low	0		0.3V+	V	
	V_{IH}	Keypad Input Level - high	0.7V+		V+	V	
	V_{PULSE}	Operating Voltage (pulse mode)	1.8		6.0	V	

Notes : 1. All inputs unloaded Quiescent Mode (Oscillator off)
2. All outputs unloaded. Single key input.
3. V_{OUT} = 0.4 Volts
4. Sink Current for V_{OUT} = – 0.5 Volts. Source Current for V_{OUT} = 2.0 Volts.
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR} The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum voltage where activation of mute output with key entry is ensured

AC Characteristics – TONE MODE

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	T_{NK}	Tone Output No Key Down			80	dBm	1
	T_{OI}	Tone Output (voltage independent)	13 173	12 194	11 218	dBm mVrms	1,2 3
	P_{EI}	Pre-emphasis, High Band	1.4	2	2.6	dB	
	DC_I	Tone Output DC Bias (V+ = –2.5V) (V+ = 3.5V)		1.25 1.5		V V	
	R_E	Tone Output load		10		KΩ	4
	T_{RIS}	Tone Output Rise Time		1		ms	5
	DIS	Output DTMF Distortion		5	8	%	3
	TR	Tone Signalling Rate		5		1/sec	
1	T_{PSD}	Pre-signal Delay	40			ms	6
2	T_{ISD}	Inter-signal Delay (repertory)		54		ms	
	T_{DUR}	Tone Output Duration (repertory)		74		ms	

Notes : 1. O dBm equals 1 mW power into 600 Ω or 775 mVolts Important Note The MK53731 is designed to drive a 10 kΩ load. The 600 Ω load is only for reference.
2. Single tone (low group) as measured at pin 10 T_A = 25 °C.
3. Supply voltage = 2 5V; R_E = 10 kΩ. T_{Oi} increases typically of 10mVrms with V_{supply} = 6.0V.
4. Supply voltage = 2.5 Volts
5. Time from beginning of tone output waveform to 90 % of final magnitude of either frequency Crystal parameters suggested for proper operation are R_S < 100 Ω, L_m = 96 mH, C_m 0.02 pF, C_h = 5pF, f = 3.579545 MHz and C_L = 18 pF.
6. Time from initial key input until beginning of signaling

AC Characteristics – KEYPAD INPUTS, PACIFIER TONE
(numbers in left hand column refer to the limiting diagrams)

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
3	T_{KD}	Keypad Debounce Time		32		ms	1
	F_{KS}	Keypad Scan Frequency		250		Hz	1
	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1
	THFP	Hookflash Timing		560		ms	1

Note : 1. Crystal oscillator accuracy directly affects these times.

AC Characteristics – PULSE MODE OPERATION

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	P_R	Pulse Rate		10		PPS	1
5	P_{DP}	Pedigital Pause		48		ms	2
6	I_{DP}	Intrdigital Pause		740		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2
9	T_M	Make Time		40		ms	2

Notes : 1. 10 PPS is the nominal rate.
2. Figure 8 illustrates this relationship

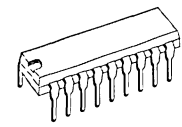
SGS-THOMSON MICROELECTRONICS

MK53732

TONE PULSE DIALER WITH LAST NUMBER AND SAVE FUNCTION

ADVANCE DATA

- SINGLE CHIP DTMF AND PULSE DIALER
- SOFTSWITCH CHANGES SIGNALING MODE FROM PULSE TO TONE
- RECALL OF LAST NUMBER DIALED (up to 28 digits long)
- SAVE ANOTHER NUMBER FUNCTION (28 digits long)
- FLASH KEY INPUT INITIATES TIMED HOOK FLASH (mask selectable)
- TIMED PABX PAUSE
- 5 TONES PER SECOND DIALING IN TONE MODE AND 10 PPS IN PULSE MODE
- DTMF ACTIVE UNTIL KEY RELEASE
- MINIMUM DTMF DURATION/SEPARATION
- PACIFIER TONE PROVIDES AUDIBLE INDICATION OF VALID KEY INPUT FOR NON-DTMF KEY ENTRIES
- POWERED FROM TELEPHONE LINE, LOW OPERATING VOLTAGE FOR LONG LOOP OPERATIONS
- MAKE/BRAK RATIO MASK SELECTABLE (40/60 or 33/67)
- PULSE RATE 10pps



DIP18 SO20

ORDERING NUMBERS :

MK53732A	MK53732AD
MK53732B	MK53732BD
MK53732E	MK53732ED
MK53732F	MK53732FD

Figure 1 : Pins Connections (top view).

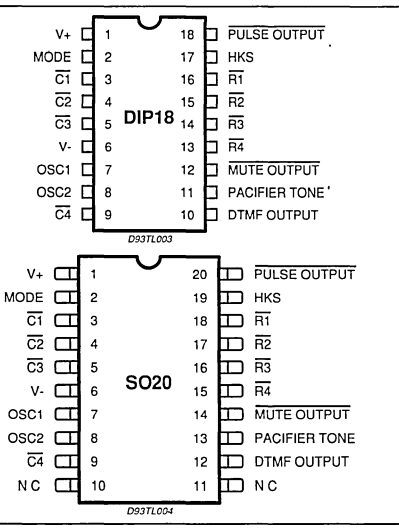
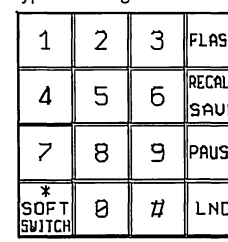


Figure 2 : Keypad Configuration.



DESCRIPTION

The device is a Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialling. The dialer buffers up to 28 digits into memory that can be later redialed with a single key input. Additionally another 28 digits memory is available for the save function.

Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include : Last Number Dialled (LND), Softswitch, Flash, Pause and Save. Figure 2 shows the keypad configuration.

A LND key input automatically redials the last number dialed.

The SAVE key serves two functions: if pressed after digits are dialled, the digits preceding will be saved into the SAVE memory. If the SAVE key is pressed just after the telephone goes off-hook, with no digits pressed prior, then the number in the SAVE memory is dialled.

Any digits entered after the SAVE key will be stored into the LND buffer.

Two features simplify PABX dialling. The PAUSE key stores a timed pause in the number sequence. Redial is then delayed until a outside line can be accessed or some other activity occurs before normal signalling resumes. The FLASH key simulates a timed break hook flash to transfer calls or to activate other special features provided by the PABX or central office.

FUNCTIONAL PIN DESCRIPTION (DIP18 only)

V+

Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (see Electrical Specifications).

MODE

Input. Pin 2. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V–), the default determines the signaling mode. A V+ connection defaults to tone mode operation and a V– connection defaults to pulse mode operation.

When dialling in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the "*" key, or softswitch, is depressed. Subsequent "*" key inputs will cause the DTMF code for an "*" to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key or the SAVE key will repeat the softswitch.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$

Keyboard inputs. The Dialer interfaces with either the standard 2-of-8 with negative common or the single-contact (Form A) keyboard.

A valid keypad entry is either a single Row connected to a single Column or V– simultaneously presented to both a single Row or Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (T_{KD}) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 17 to pin 1), the keyboard inputs become high impedance input pin.

In the tone mode, if 2 or more keys in the same row or if 2 or more keys in the same column are depressed a single tone will be output. The tone will correspond to the row or column for which the 2 keys were pushed. This feature is for test purposes, and single tones will not be redialed.

Also in the tone mode, the output tone is continuous in manual dialing as long as the key is pushed. The output tone duration follows the table 1.

Table 1. Output Tone Duration.

Key - Push Time, T	Tone Output
T ≤ 32ms	No output, ignored
32ms ≤ T ≤ 100ms + Tkd	100ms Duration
T ≥ 100ms + Tkd	Output Duration = T - Tkd

When redialing in the tone mode, each DTMF output is 100 ms duration, and the tone separation (intersignal delay) is 100 ms.

V–

Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2

Pin 7 (input), pin 8 (output). OSC1 and OSC2 are connections to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ± 0.25 % may also be used.

DTMF OUTPUT

Output. Pin 10. A NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 7 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The Dialer is designed to operate from an unregulated supply ; the TONE LEVEL is supply independent, and the single row tone output level will be typically :

$$T_{01} = 150 \text{ mVrms} \pm 1 \text{ dB}$$

The DC component of the DTMF output while active is described by the following equation :

$$V_{DCI} = 0.27 \times V^{+} + 0.44 \text{ V}$$

Figure 3 : MK53732 Block Diagram.

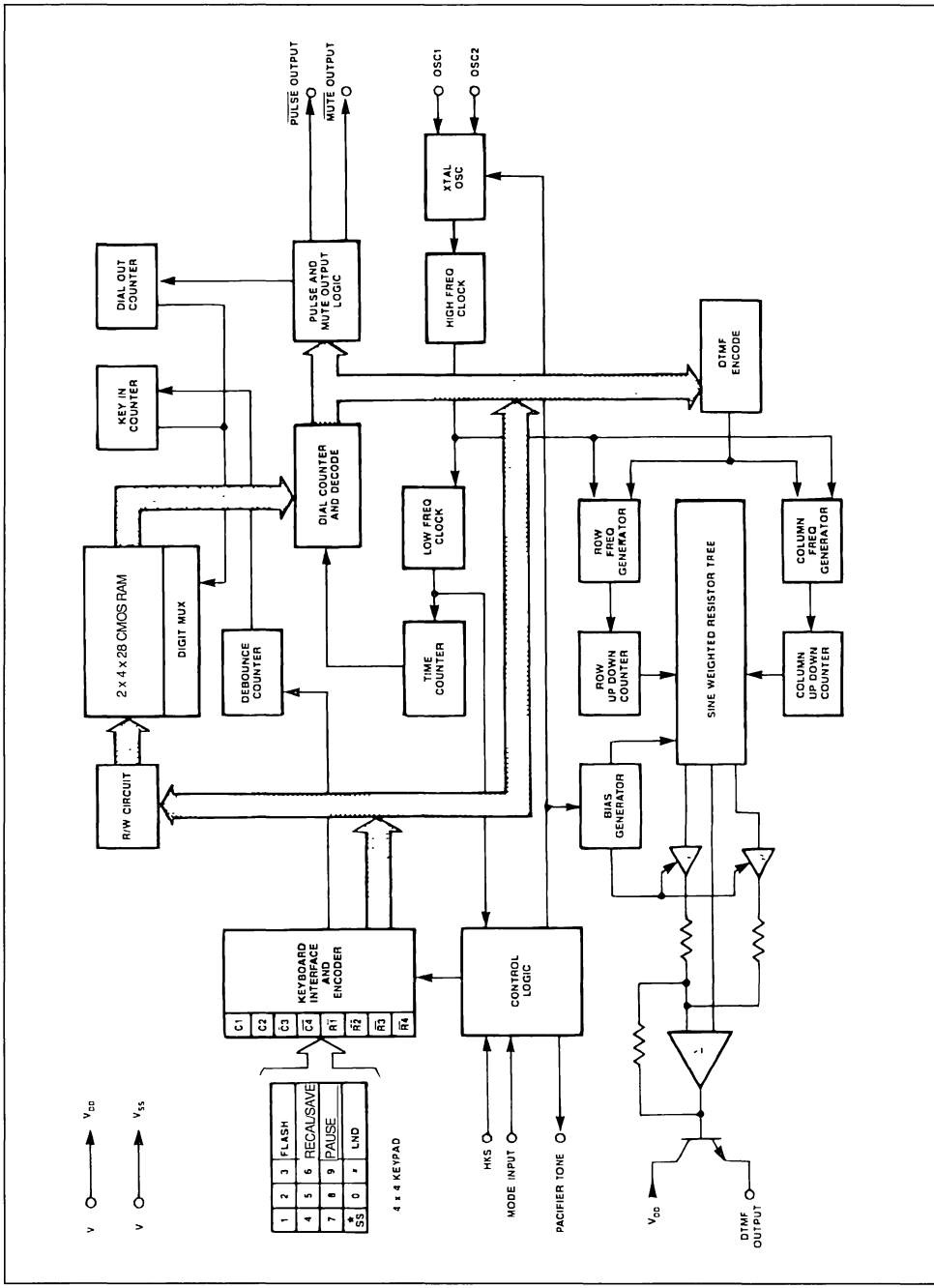


Figure 4 : Typical Single Tone.

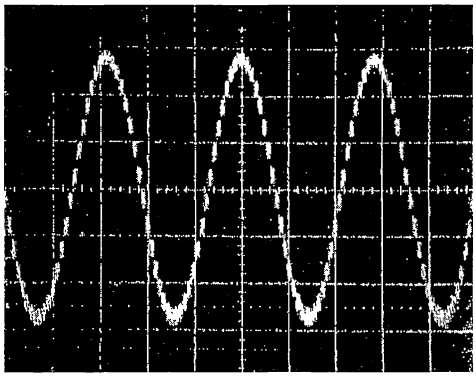


Figure 5 : Typical Dual Tone.

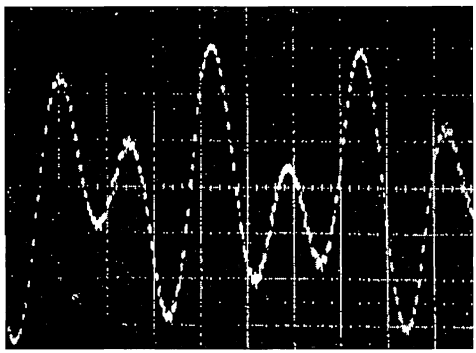
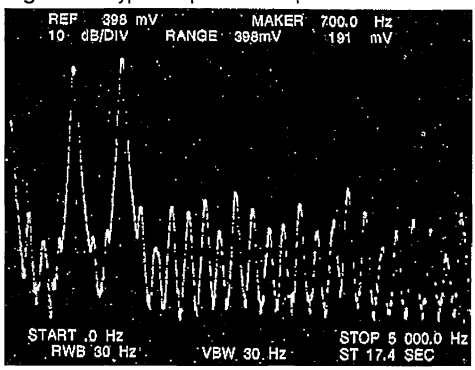


Figure 6 : Typical Spectral Response.



PACIFIER TONE

Output. Pin 11. A 500 Hz square wave is activated upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all valid key entries activate the pacifier tone. In tone mode, any non-DTMF entry (FLASH, PAUSE, SAVE, LND)activates the pacifier tone. The pacifier tone provides audible feedback, confirming that the key has been properly entered and accepted.

$\overline{\text{MUTE OUTPUT}}$

Output. Pin 12. This pin is the $\overline{\text{MUTE OUTPUT}}$ for both tone and pulse modes. Timing is dependent upon mode.

The $\overline{\text{MUTE OUTPUT}}$ consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In the tone mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the transmitter and the receiver of the speech from the line during DTMF signaling. During dialing, $\overline{\text{MUTE OUTPUT}}$ is active continuously until dialing is completed. $\overline{\text{MUTE OUTPUT}}$ goes active when any key is pushed.

In the pulse mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the receiver and the speech network from the line. $\overline{\text{MUTE OUTPUT}}$ timing is shown in Figure 8 for pulse mode signaling and Figure 7 for tone mode signaling. $\overline{\text{MUTE OUTPUT}}$ is active during each digit, and not active during the interdigit time. In pulse mode, $\overline{\text{MUTE OUTPUT}}$ goes active 70ms (MK53732A/B) and 14ms (MK53732E/F) before $\overline{\text{PULSE OUTPUT}}$ for a FLASH.

HKS

Input. Pin 17. Pin 17 is the hookswitch input to the dialer. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2. Figure 8 illustrates the timing for this pin.

$\overline{\text{PULSE OUTPUT}}$

Output. Pin 18. This is an output consisting of an open drain N-channel device. In either pulse or tone mode, the FLASH key will cause a timed break output pulse at pin 18 (see specification).

DEVICE OPERATION (Tone Mode)

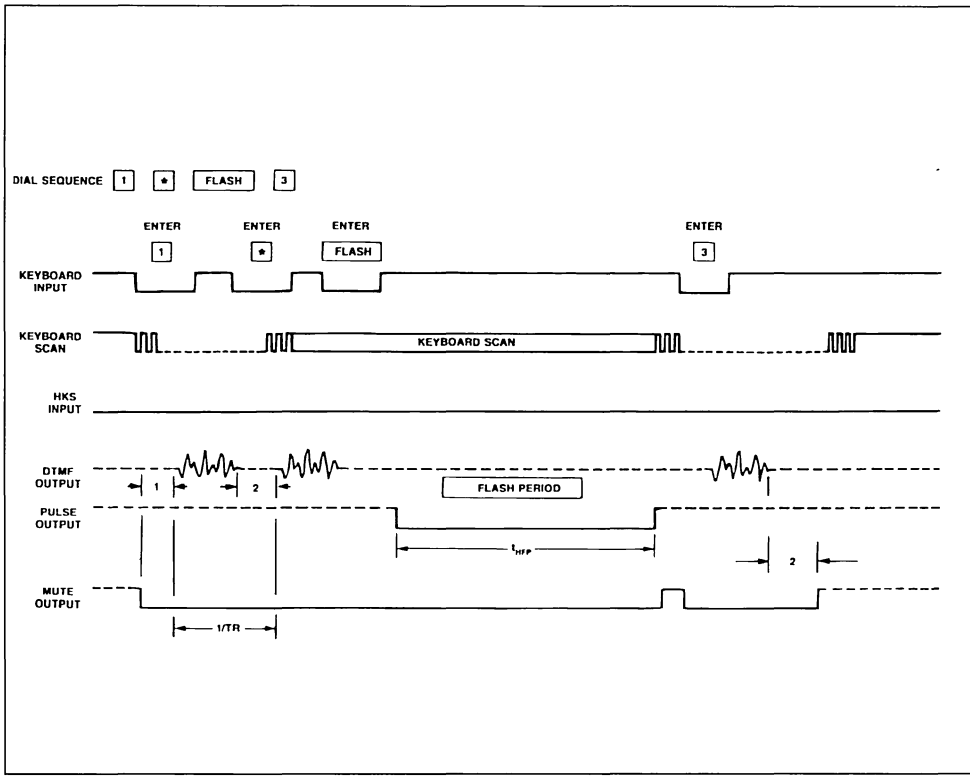
When the dialer is not actively dialing, it consumes very little current. While on-hook, all keypad input pins are high impedance. Row and Column inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of approximately 40 ms (measured from initial key closure). Output tone duration is shown in Table 1.

The device allows manual dialing of an indefinite number of digits, but if more than 28 digits are dialed, the device will "wrap around". That is, the extra digits beyond 28 will be stored at the beginning of the LND buffer, and the first 28 digits will no longer be available for redial.

Table 2 : DTMF Output Frequency.

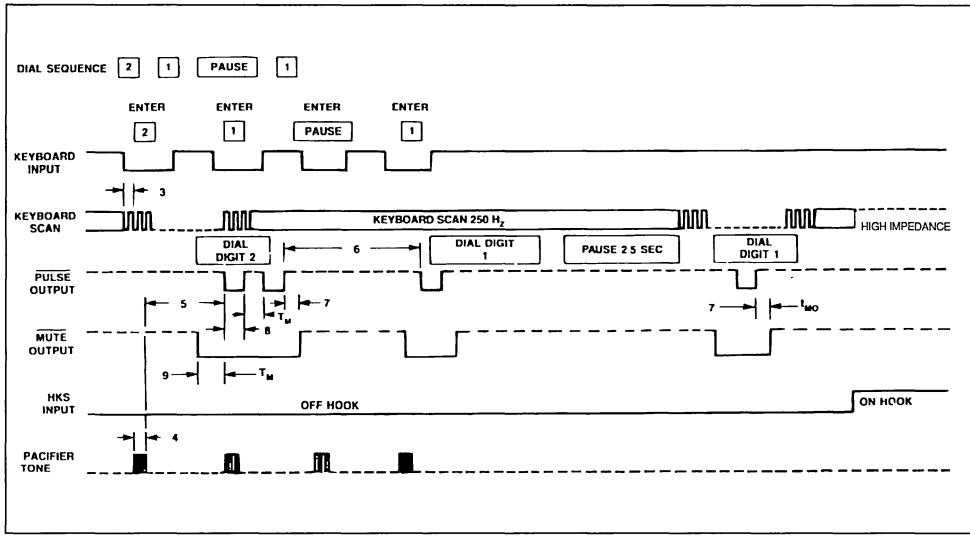
Key Input	Standard Frequency	Actual Frequency	% Deviation
ROW 1	697	699.1	+0.31
2	770	766.2	–0.49
3	852	847.4	–0.54
4	941	948.0	+0.74
COL 1	1209	1215.9	+0.57
2	1336	1331.7	–0.32
3	1477	1471.9	–0.35

Figure 7 : Tone Mode Timing.

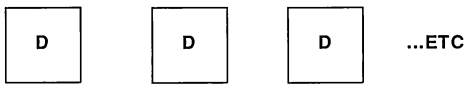


Note : For this example, key entries are ≤ 100 ms, but ≥ 32 ms.

Figure 8 : Pulse Mode Timing.



NORMAL DIALING (off-hook)



Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

Last number dialing is accomplished by entering the LND key.

SAVE

If after off-hook, SAVE is pressed after that D1, D2 and D3 have been dialed, Then D1, D2 and D3 will be entered into the SAVE buffer.

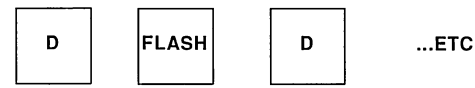
If SAVE is pressed immediately after off-hook, numbers stored in the SAVE buffer will be dialed out.

Any digits entered after the SAVE key will be entered into the LND buffer as a new number for LND.

PAUSE

A pause may be entered into the dialed sequence at any point by keying in the special function key, PAUSE. Pause inserts a 1.1-second delay into the dialing sequence. The total delay, including pre-digit and post-digit pauses is shown in Table 3.

HOOK FLASH

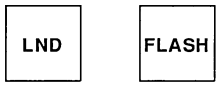


Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed Break (see specification). The FLASH function is stored in memory, but it will not be redialed as such. When a FLASH key is pressed, no further key inputs will be accepted until the hookflash function (timed break) has been dialed. The key input following a FLASH will be stored as the initial digit of a new number (overwriting the number dialed prior to the FLASH) unless it is another FLASH. Consecutive FLASH entries after a

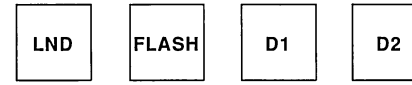
number is dialed will be stored sequentially in the LND memory and a subsequent LND entry will cause the redial of that number with a delay at the end of the redialing sequence, but not hookflash breaks. When redialing in tone mode, MUTE OUTPUT will remain active during the flash delay period.

FLASH key pressed immeditely after off-hook or LND key will not clear the LND buffer unless digits are entered following the FLASH key.

LND not cleared



LND not cleared



LND buffer will contain D1, D2

SOFTSWITCH

When dialing in the pulse mode, a Softswitch feature will allow a change to the tone mode whenever the "*" key, or SOFTSWITCH, is depressed. Subsequent "*" key inputs will cause the DTMF code for an "*" to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

Table 3 : Special Function Delays.

Each delay shown below represents the time required between the depression of the special function key and the time at which a new digit can be dialed.

The time is considered "FIRST" key is all previous inputs have been completely dialed. The time is considered "AUTO" if in redial, or if previous dialing is still in progress.

Function	First/Auto	Delay (seconds)	
		Pulse (10pps)	Tone
SOFTSWITCH	FIRST AUTO	0.2 1.0	
PAUSE	FIRST AUTO	1.9 2.7	1.2 1.3

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC Supply Voltage	6.5	V
Operating Temperature	-30 to +60	°C
Storage Temperature	-55 to +125	°C
Maximum Power Dissipation @ 25°C	500	mW
Maximum Voltage on any Pin	(V+) +0.3, (V-) -0.3	V

ELECTRICAL CHARACTERISTICS (All specifications are for $V_+ = 2.5V$ and $T_{amb} = 25°C$; unless otherwise stated).

DC Characteristcs

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	V+	DC Operating Voltage (Tone) DC Operating Voltage (Pulse)	2.5 1.8		6 6	V V	
	V_{MR}	Memory Retention Voltage	1.5			V	1,6
	I_S	Stand-by Current		0.4	1	µA	1
	I_{MR}	Memory Retention Current		0.1	0.75	µA	5,6
	V_{MUTE}	Mute Output Operating Voltage	1.8			V	7
	I_T	Operating Current (Tone)		300	600	µA	2
	I_P	Operating Current (Pulse)		150	250	µA	2
	I_{ML}	Mute Output @ (2.5V)	1			mA	3
		Sink Current @ (4V)	3			mA	
	I_{PL}	Pulse Output Sink Current	1	2		mA	3
	I_{PC}	Pacifier Tone Sink/Source	250	500		µA	4
	K_{RU}	Keypad Pullup Resistance		100		KΩ	
	K_{RD}	Keypad Pulldown Resistance		500		Ω	
	V_{IL}	Keypad input Level - low	0		0.3V+	V	
	V_{IH}	Keypad Input Level - high	0.7V+		V+	V	

Notes : 1. All inputs unloaded. Quiescent Mode (Oscillator off).
2. All outputs unloaded. Single key input.
3. V_{OUT} = 0.4 Volts.
4. Sink Current for V_{OUT} = + 0.5 Volts. Source Current for V_{OUT} = 2.0 Volts
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR} The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum voltage where activation of mute output with key entry is ensured.

AC Characteristics (numbers in left column refer to timing diagrams)

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	T_{NK}	Tone Output No Key Down			-80	dBm	1
	T_{OI}	Tone Output (voltage independent)	130	150	170	mVrms	2,3
	P_{EI}	Pre-emphasis, High Band	1.4	2	2.6	dB	
	DC_I	Tone Output DC Bias (V+ = 2.5V) (V+ = 3.5V)		1.1 1.35		V V	
	R_E	Tone Output load		10		KΩ	4
	T_{RIS}	Tone Output Rise Time		1		ms	5
	DIS	Output DTMF Distortion		5	8	%	3
	TR	Tone Signalling Rate		5		1/sec	
1	T_{PSD}	Pre-signal Delay	40			ms	6
2	T_{ISD}	Inter-signal Delay (repertory)		100		ms	
	T_{DUR}	Tone Output Duration (repertory)		100		ms	

Notes : 1. O dBm equals 1 mW power into 600 Ω or 775 mVolts Important Note. The device is designed to drive a 10 kΩ load The 600 Ω load is only for reference
2 Single tone (low group) measured at pin 10.
3 Supply voltage = 2.5 to 6 Volts R_E = 10 kΩ
4 Supply voltage = 2.5 Volts.
5 Time from beginning of tone output waveform to 90 % of final magnitude of either frequency.
6 Time from initial key input until beginning of signaling.

AC Characteristics (keypad inputs, pacifier tone)

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
3	T_{KD}	Keypad Debounce Time		32		ms	1
	F_{KS}	Keypad Scan Frequency		250		Hz	1
	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1

Note : 1. Crystal oscillator accuracy directly affects these times

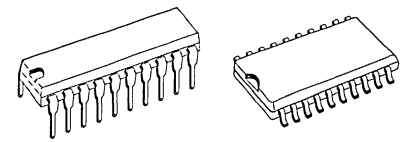
AC Characteristics (Pulse Mode Operation - specific of each version)

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VERSION A							
	P_R	Pulse Rate		10		PPS	1
5	P_{DP}	Predigit Pause		50		ms	2
6	I_{DP}	Interdigit Pause		820		ms	2
7	T_{MO}	Mute Overload Time		4		ms	2
8,9	B_M	Break/Make Ratio		60:40			2
	T_{HFP}	Hookflash Timing (Tone/Pulse)		600		ms	2
VERSION B							
	P_R	Pulse Rate		10		PPS	1
5	P_{DP}	Predigit Pause		43		ms	2
6	I_{DP}	Interdigit Pause		820		ms	2
7	T_{MO}	Mute Overload Time		4		ms	2
8,9	B_M	Break/Make Ratio		67:33			2
	T_{HFP}	Hookflash Timing (Tone/Pulse)		600		ms	2
VERSION E							
	P_R	Pulse Rate		10		PPS	1
5	P_{DP}	Predigit Pause		43		ms	2
6	I_{DP}	Interdigit Pause		820		ms	2
7	T_{MO}	Mute Overload Time		4		ms	2
8,9	B_M	Break/Make Ratio		67:33			2
	T_{HFP}	Hookflash Timing (Tone/Pulse)		104		ms	2
VERSION F							
	P_R	Pulse Rate		10		PPS	1
5	P_{DP}	Predigit Pause		50		ms	2
6	I_{DP}	Interdigit Pause		820		ms	2
7	T_{MO}	Mute Overload Time		4		ms	2
8,9	B_M	Break/Make Ratio		60:40			2
	T_{HFP}	Hookflash Timing (Tone/Pulse)		272		ms	2

Notes : 1. The Pulse Rate given is the nominal rate
2 Figure 7 and 8 illustrates this relationship.

REPERTORY DIALER

- SINGLE CHIP DTMF AND PULSE DIALER
- SOFTSWITCH CHANGES SIGNALING MODE FROM PULSE TO TONE
- NINE NUMBER REPERTORY PLUS RECALL OF LAST NUMBER DIALED (18 digits each)
- FLASH KEY INPUT INITIATES TIMED HOOK FLASH
- 8 TONE PER SECOND DIALING IN TONE MODE AND 10 PPS IN PULSE MODE
- DTMF ACTIVE UNTIL KEY RELEASE
- MINIMUM DTMF DURATION/SEPARATION GUARANTEED (74/54 ms)
- PACIFIER TONE PROVIDES AUDIBLE INDICATION OF VALID KEY INPUT FOR NON-DTMF KEY ENTRIES
- POWERED FROM TELEPHONE LINE, LOW OPERATING VOLTAGE FOR LONG LOOP APPLICATIONS

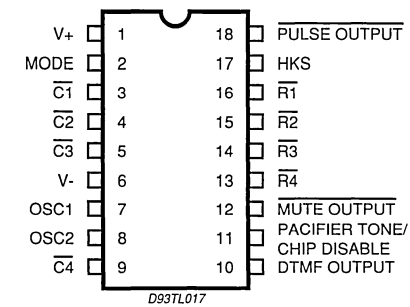


DIP18 **SO20**

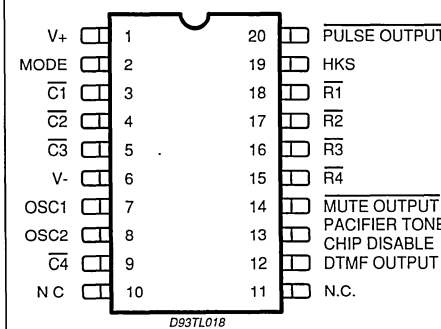
ORDERING NUMBERS :

MK53761N00 MK53761D

Figure 1 : Pin Connections.



DIP18



SO20

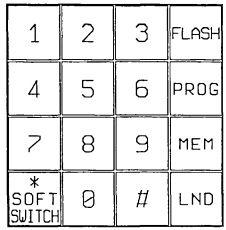
DESCRIPTION

The MK53761 is a Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53761 buffers up to 18 digits into memory that can be later redialed with a single key input. Up to nine repertory numbers may be stored. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include : Last Number Dialed (LND), Softswitch, and Flash. Figure 2 shows the keypad configuration.

A LND key input automatically redials the last number dialed. The PROG key provides an easy way to program a number into any memory location (1-9) whether on-hook on off-hook. The MEM key allows easy redialing of the number stored in memory locations (1-9).

The FLASH key simulates a 560 ms hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

Figure 2 : Keypad Configuration.



FUNCTIONAL PIN DESCRIPTION (DIP18 only)

V+

Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (see electrical specifications).

MODE

Input. Pin 2. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V–), the default determines the signaling mode. A V+ connection defaults to tone mode operation and a V– connection defaults to pulse mode operation.

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key, or softswitch, is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$

Keyboard inputs. The MK53761 interfaces with either the standard 2-of-8 with negative common or the singlecontact (Form A) keyboard.

A valid keypad entry is either a single Row connected to a single Column or V– simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (TK_D) of 32ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 17 to pin 1), the keyboard inputs all pull high through on-chip pullup resistors.

In the tone mode, if 2 or more keys in the same row or if 2 or more keys in the same column are depressed a single tone will be output. The tone will corres-pond to the row or column for which the 2 keys were pushed. This feature is for test purposes, and single tones will not be redialed.

Also in the tone mode, the output tone is continuous is manual dialing as long as the key is pushed. The output tone duration follows the table 1.

Table 1 : Output Tone Duration.

Key-Push Time, T*	Tone Output*
$T \leq 32ms$	No Output Ignored by MK53761
$32ms \leq T \leq 75ms + T_{KD}$	75ms Duration Output
$T \geq 75ms + T_{KD}$	Output Duration = $T - T_{KD}$

* TKD is the key pad debounce time which is typically 32 ms

When redialing in the tone mode, each DTMF output is 75ms duration, and the tone separation (intersignal delay) is 50ms.

V–

Input. Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2

Pin 7 (input), pin 8 (output). OSC1 and OSC2 are connections to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ± 0.25 % may also be used.

DTMF OUTPUT

Output. Pin 10. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 7 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK53761 is designed to operate from an unregulated supply ; the TONE LEVEL is supply independent, and the single row tone output level will be typically :

$$T_{oi} = -12 \text{ dBm} \pm 1 \text{ dB}$$

The DC component of the DTMF output while active is described by the following equation :

$$VDC_1 = 0.3 \text{ V+} + 0.5 \text{ Volts}$$

Figure 3 : MK53761 Functional Block Diagram.

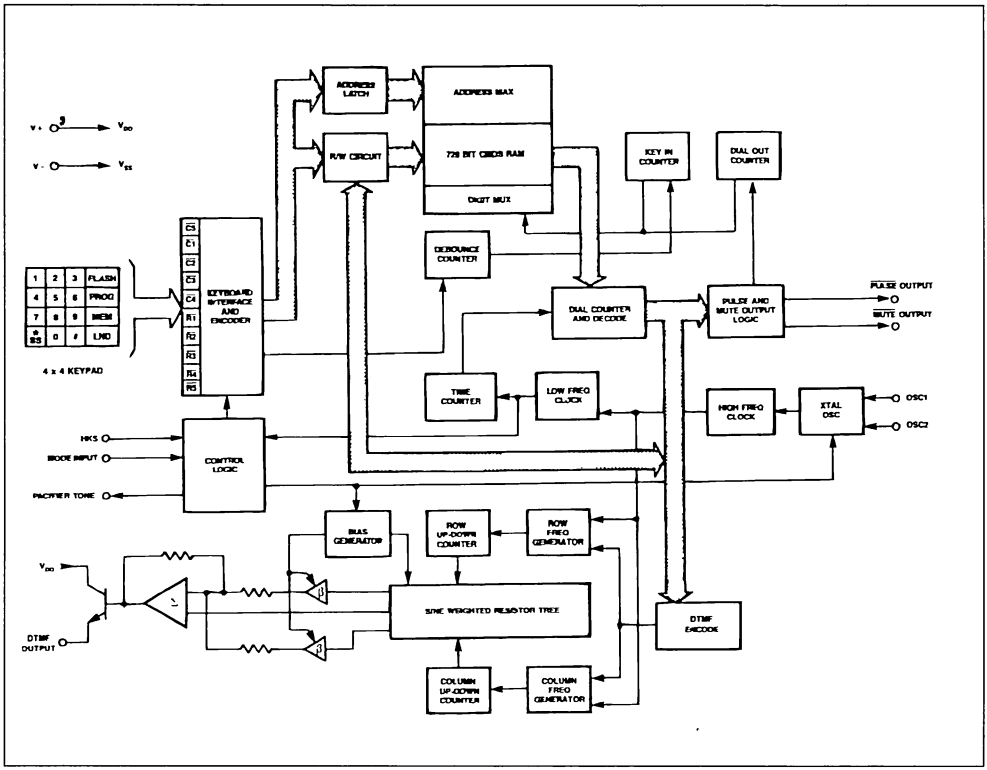


Figure 4 : Typical Single Tone.

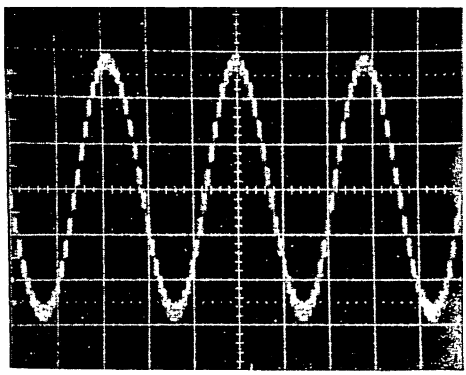


Figure 5 : Typical Dual Tone.

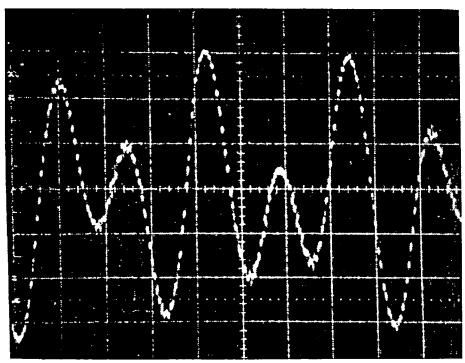
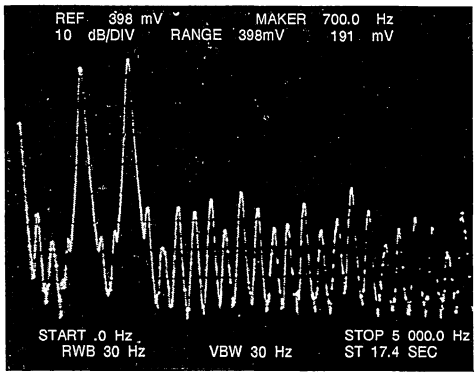


Figure 6 : Typical Spectral Response.



PACIFIER TONE OUTPUT/CHIP DISABLE INPUT

Output. Pin 11. The pacifier tone provides audible feed-back, confirming that the key has been properly entered and accepted. A 500 Hz square wave is activated upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all key entries activate the pacifier tone. In tone mode, any non-DTMF key (LND, FLASH, MEM, PROG) entry activates the pacifier tone. When programming the chip, all valid key entries activate the pacifier tone in either pulse or tone mode.

The CHIP DISABLE is an input. When pin 11 is switched low through a resistor (10 K to 100 K), the MK53761 is enabled. When pin 11 is switched to V+ through the resistor, all keypad inputs are pulled high, and the MK53761 will ignore all keypad inputs. When the chip is disabled, it will not dial, and it cannot be programmed. The chip can only be disabled when the circuit is inactive (not dialing) and Pin 12 is switched high.

Table 2 : DTMF Output Frequency.

Key Input		Standard Frequency	Actual Frequency	% Deviation
ROW	1	697	699.1	+ 0.31
	2	770	766.2	– 0.49
	3	852	847.4	– 0.54
	4	941	948.0	+ 0.74
COL	1	1209	1215.9	+ 0.57
	2	1336	1331.7	– 0.32
	3	1477	1471.9	– 0.35

MUTE OUTPUT

Output. Pin 12. This pin is the $\overline{\text{MUTE OUTPUT}}$ for both tone and pulse modes. Timing is dependent upon mode.

The $\overline{\text{MUTE OUTPUT}}$ consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In the tone mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE OUTPUT}}$ is active continuously until dialing is completed. $\overline{\text{MUTE OUTPUT}}$ goes active when any key is pushed.

In the pulse mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the receiver and the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE OUTPUT}}$ timing is shown in Figure 8 for pulse mode signaling and Figure 7 for tone mode signaling. $\overline{\text{MUTE OUTPUT}}$ is active during each digit, and not active during the interdigit time. In both tone and pulse modes, $\overline{\text{MUTE OUTPUT}}$ goes active 40 ms before $\overline{\text{PULSE OUTPUT}}$ for a FLASH. Figure 8 illustrates the timing for this pin.

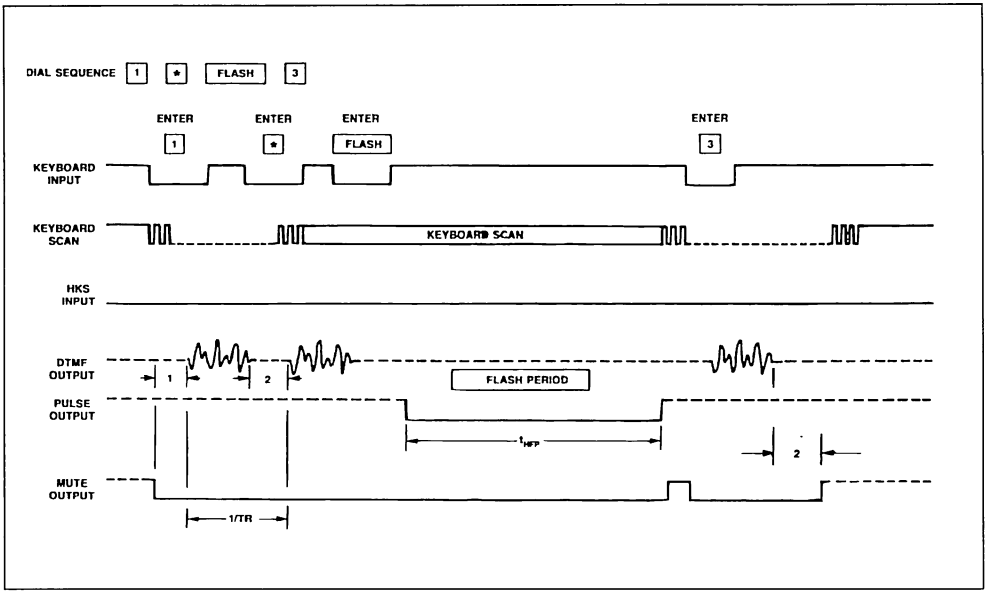
HKS

Input. Pin 17. Pin 17 is the hookswitch input to the MK53761. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2.

$\overline{\text{PULSE OUTPUT}}$

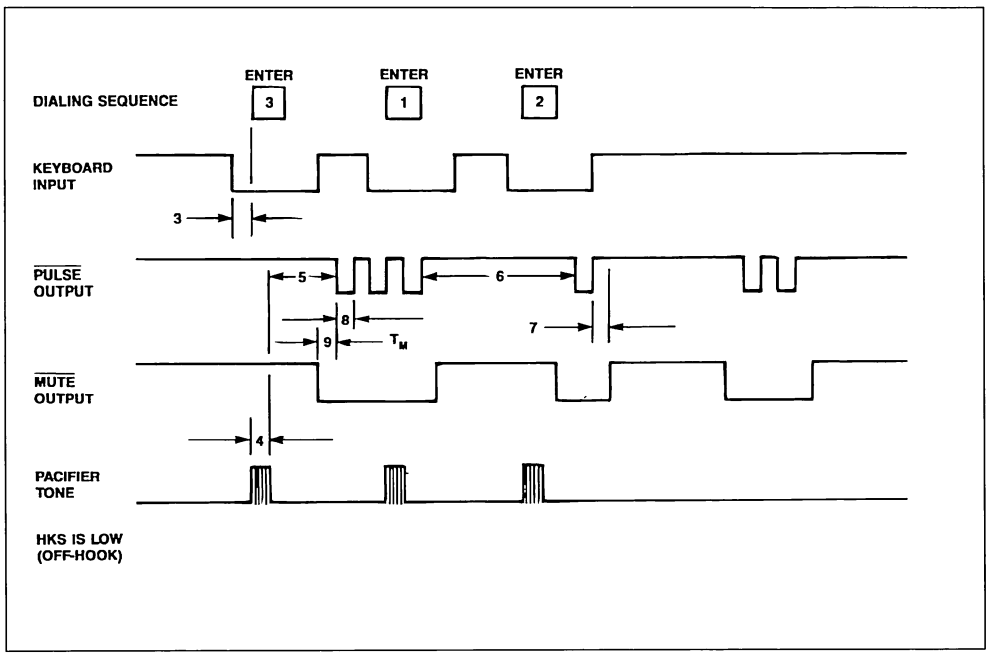
Output. Pin 18. This is an output consisting of an open drain N-channel device. In either pulse or tone mode, the FLASH key will cause a 560 ms output pulse at pin 18.

Figure 7 : Tone Mode Timing.



Notes : 1. For this example, key entries are ≤ 75 ms, but ≥ 32 ms.
2. MUTE goes active after any key is depressed

Figure 8 : Pulse Mode Timing.

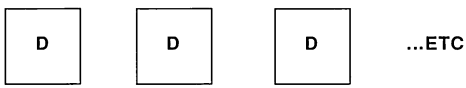


DEVICE OPERATION

When the MK53761 is not actively dialing, it consumes very little current. Row and Column inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, and dialing begins after a presignal delay of approximately 40 ms (measured from initial key closure). Output tone duration is shown in Table 1.

The MK53761 allows manual dialing of an indefinite number of digits, but if more than 18 digits are dialed per number, the 53761 will "wrap around". That is, the extra digits beyond 18 will be stored at the beginning of the LND buffer, and the first 18 digits will no longer be available for redial. During autodial from LND or any memory location, key inputs are not accepted, but they will suspend dialing until released.

NORMAL DIALING (off-hook)

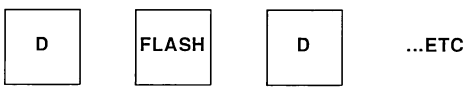


Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

Last number dialing is accomplished by entering the LND key.

HOOK FLASH



Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed Break of 560 ms. The FLASH function is stored in memory, but it will not be redialed as such. When a FLASH key is pressed, no further key inputs will be accepted until the hookflash function (560 ms break) has been dialed. The key input following a FLASH will be stored as the initial digit of a new number (overwriting the number dialed prior to the FLASH) unless it is another FLASH. Consecutive FLASH entries after a number is dialed will be stored sequentially in the LND memory and a subsequent LND entry will cause the redial of that number with a delay, but not hookflash breaks, at the end of the redialing sequence. When redialing in tone mode, $\overline{\text{MUTE OUTPUT}}$ will remain active during the flash delay period.

SOFTSWITCH

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

PROGRAMMING AND REPERTORY DIALING

Programming is independent of HKS (pin 17) and MODE (pin 2).

To program, enter the following :

PROG, Digit 1, Digit 2, ..., MEM, Location (1-9).

When programming, dialing in inhibited.

To dail a number from repertory memory (HKS must be low) enter the following :

MEM, Location (1-9).

To save the last number dialed : PROG, MEM, Location (1-9).

Table 3 : Special Function Delays.

Each delay shown below represents the time required from after the special function key is depressed until a new digit can be dialed.
The time is considered "FIRST" key is all previous inputs have been completed dialed. The time is considered "AUTO" if in redial, or previous dialing is still in progress.

Function	First/Auto	Pulse	Tone
SOFTSWITCH	FIRST AUTO	0.40 1.10	

ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
DC Supply Voltage	6.5	V
Operating Temperature	– 20 to +60	°C
Storage Temperature	– 55 to + 125	°C
Maximum Power Dissipation (25 °C)	500	mW
Maximum Voltage on any Pin	(V^+) + .3 ; (V^-) – .3	V

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V+ TONE	DC Operating Voltage (tone mode)	2.5		6.0	V	
V_{MR}	Memory Retention Voltage	1.5			V	1. 6
I_S	Standby Current		0.4	1.0	µA	1
I_{MR}	Memory Retention Current		0.15	0.75	µA	5. 6
V_{MUTE}	Mute Output Operating Voltage	1.8			V	7
I_T	Operating Current (tone)		300	600	µA	2
I_P	Operating Current (pulse)		150	250	µA	2
	Operating Current On-hook Program Mode Key Operated No-key Operated			 200 1	 µA µA	
I_{ML}	Mute Output (2.5 Volts) Sink Current (4.0 Volts)	1.0 3.0			mA mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		µA	4
K_{RU}	Keypad Pullup Resistance		100		kΩ	
K_{RD}	Keypad Pulldown Resistance		500		Ω	
V_{IL}	Keypad Input Level-low	0		0.3 V +	V	
V_{IH}	Keypad Input Level-high	0.7 V +		V +	V	
V_{PULSE}	Operating Voltage (pulse mode)	1.8		6.0	V	

Notes : 1. All inputs unloaded. Quiescent mode (oscillator off).
2. All outputs unloaded, single key input
3. V_{OUT} = 0 4 Volts.
4. Sink current for V_{OUT} = 0 5 Volts, Source Current for V_{OUT} = 2.0 Volts.
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum voltage where activation of mute output with key entry is ensured

ELECTRICAL CHARACTERISTICS (continued)

AC CHARACTERISTICS – TONE MODE

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	T_{NK}	Tone Output no Key Down			– 80	dBm	1
	T_{OI}	Tone Output (independent)	– 13 173	– 12 194	– 11 218	dBm mV_{rms}	1, 2 3
	PE_I	Pre-emphasis, High Band	1.4	2.0	2.6	dB	
	DC_I	Tone Output DC Bias V + = 2.5 V + = 3.5		 1.25 1.5		V	
	R_E	Tone Output Load		10		kΩ	4
	T_{RIS}	Tone Output Rise Time		1.0		ms	5
	DIS	Output Distortion		5.0	8.0	%	3
	TR	Tone Signaling Rate		8.0		1/sec	
1	T_{PSD}	Pre-signal Delay	40			ms	6
2	T_{ISD}	Inter-signal Delay (repertory)		54		ms	
	T_{DUR}	Tone Output Duration (repertory)		74		ms	

Notes : 1 O dBm equals 1 mW power into 600 Ω or 775 mVolts.Important note : the MK53761 is designed to drive a 10 kΩ load. The 600 Ω load is only for reference.
2. Single tone (low group), as measured at pin 10, T_A = 25°C.
3. Supply voltage = 2.5V; R_E = 10 kΩ T_{OI} increases typically of 10mVrms with V_S = 6V.
4. Supply voltage = 2 5 volts.
5 Time from beginning of tone output waveform to 90 % of final magnitude of either frequency. Crystal parameters suggested for proper operation are R_s < 100 Ω, L_m = 96 mH, C_m = 0.02 pF, C_h = 5 pF, f = 3.579545 MHz, and C_L = 18 pF
6. Time from initial key input until beginnig of signaling.

AC CHARACTERISTICS – KEYPAD INPUTS, PACIFIER TONE (numbers in left hand column refer to the timing diagrams.)

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
3	T_{KD}	Keypad Debounce Time		32		ms	1
	F_{KS}	Keypad Scan Frequency		250		Hz	1
	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1
	T_{HFP}	Hookflash Timing		560		ms	1

Note . 1. Crystal oscillator accuracy directly affects these times

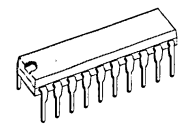
AC CHARACTERISTICS – PULSE MODE OPERATION

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	P_R	Pulse Rate		10		PPS	1
5	PDP	Predigital Pause		48		ms	2
6	IDP	Interdigital Pause		740		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2
9	T_M	Make Time		40		ms	2

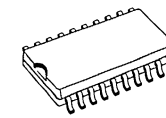
Notes : 1. 10 PPS is the nominal rate.
2. Figure 8 illustrates this relationship.

REPERTORY DIALER

- SINGLE CHIP DTMF AND PULSE DIALER
- STORES 10 18-DIGIT TELEPHONE NUMBERS, INCLUDING LAST NUMBER DIALED
- SOFTSWITCH CHANGES SIGNALING MODE FROM PULSE TO TONE
- SINGLE BUTTON REDIAL OF ALL TEN MEMORIES
- FLASH KEY INPUT INITIATES TIMED HOOK FLASH
- 8 TONES PER SECOND DIALING IN TONE MODE AND 10 PPS IN PULSE MODE
- DTMF ACTIVE UNTIL KEY RELEASE
- MINIMUM DTMF DURATION/SEPARATION GUARANTEED (74/54 ms)
- PACIFIER TONE PROVIDES AUDIBLE INDICATION OF A VALID KEY INPUT FOR NON-DTMF KEY ENTRIES
- POWERED FROM TELEPHONE LINE, LOW OPERATING VOLTAGE FOR LONG LOOP APPLICATIONS



DIP20

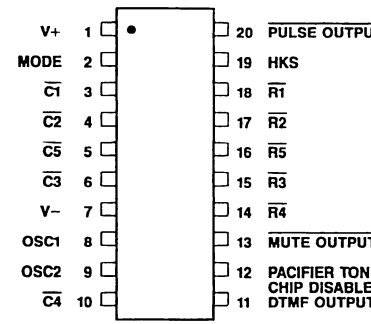


SO20

ORDERING NUMBERS :

MK53762N00 MK53762D

Figure 1 : Pin Connection.



DESCRIPTION

The MK53762 is a Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53762 buffers up to 18 digits into memory that can be later redialed with a single key input. Up to nine repertory numbers may be stored. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include : Last Number Dialed (LND), Softswitch, Flash, and 9 memories. Figure 2 shows the keypad configuration.

A LND key input automatically redials the last number dialed, and the MEM keys provide single key access to all memory locations for auto-dialing.

The FLASH key simulates a 560 ms hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

The PAUSE key allows the user to insert a delay in dialing for functions such as the pause in accessing an outside line when redialing from a PABX.

The PROG key provides an easy way to program a number into any memory location (MEM 1 - MEM 9) whether on-hook or off-hook.

Figure 2 : Keypad Configuration.

1	2	3	FLASH	MEM9
4	5	6	PROG	MEM8
7	8	9	PAUSE	MEM7
* SOFT SWITCH	0	#	LND	MEM6
MEM1	MEM2	MEM3	MEM4	MEM5

FUNCTIONAL PIN DESCRIPTION

V+
Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (see Electrical Specifications).

MODE
Input. Pin 2. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V–), the default determines the signaling mode. A V+ connection defaults to tone mode operation and a V– connection defaults to pulse mode operation.
When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key, or softswitch, is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{C5}$, $\overline{R5}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$
Keyboard inputs. The MK53762 interfaces with either the standard 2-of-10 with negative common or the single-contact (Form A) keyboard.
A valid keypad entry is either a single Row connected to a single Column or V– simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (T_{KD}) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 19 to pin 1), the keyboard inputs all pull high through on-chip pullup resistors.

In the tone mode, if 2 or more keys in the same row or column are depressed a single tone will be output. The tone will correspond to the row or column for which the 2 keys were pushed. This feature is for test purposes.
Single tones will not be redialed.
Also in the tone mode, the output tone is continuous in manual dialing as long as the key is pushed. The output tone duration follows the table below :
Table 1 : Output Tone Duration

Key-Push Time, T*	Tone Output*
$T \leq 32ms$	No Output Ignored by MK53761
$32ms \leq T \leq 75ms + T_{KD}$	75ms Duration Output
$T \geq 75ms + T_{KD}$	Output Duration = $T - T_{KD}$

* TKD is the key pad debounce time which is typically 32ms

When redialing in the tone mode, each DTMF output is 75ms duration, and the tone separation (intersignal delay) is 50ms.

V –
Input. Pin 7 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2
Pin 8 (input), pin 9 (output). OSC1 and OSC2 are connections to an on-chip inverter used as the timing reference for the circuit. It has have sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ± 0.25 % may also be used.

DTMF OUTPUT
Output. Pin 11. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 7 shows the timing at this pin.
The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.
The MK53762 is designed to operate from an unregulated supply ; the TONE LEVEL is supply independent, and the single row tone output level will be typically :

$$T_{oi} = -12 \text{ dBm} \pm 1 \text{ dB}$$

The DC component of the DTMF output while active is described by the following equation :

$$VDC_1 = 0.3\ V+ + 0.5 \text{ Volts}$$

Figure 3 : MK53762 Functional Block Diagram.

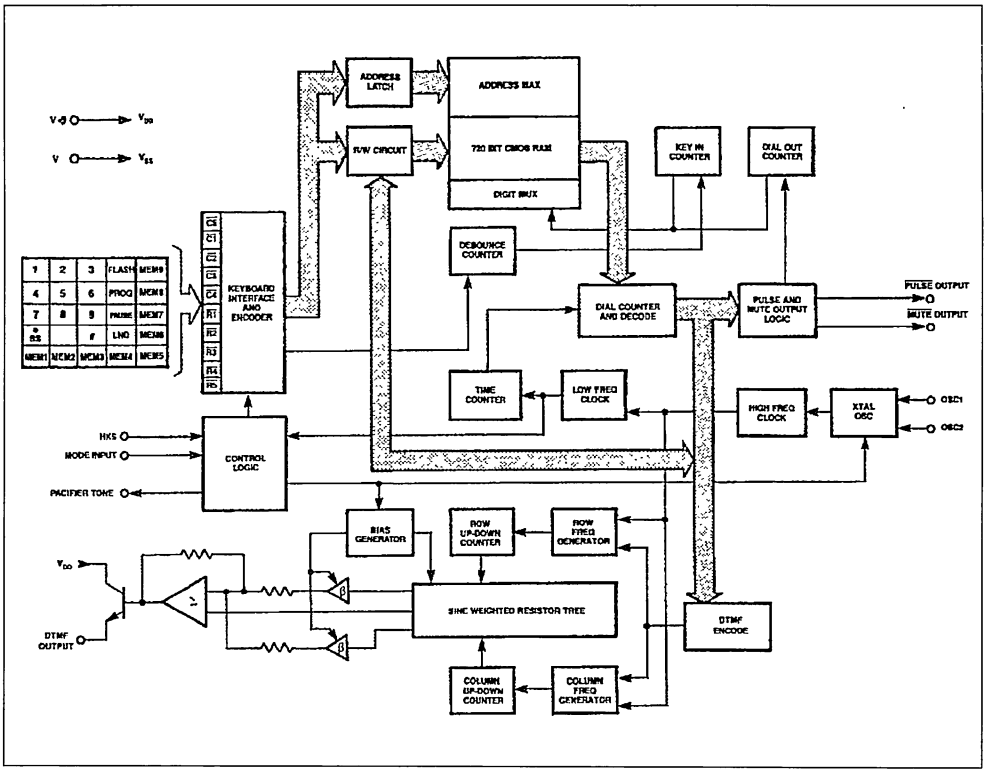


Figure 4 : Typical Single Tone.

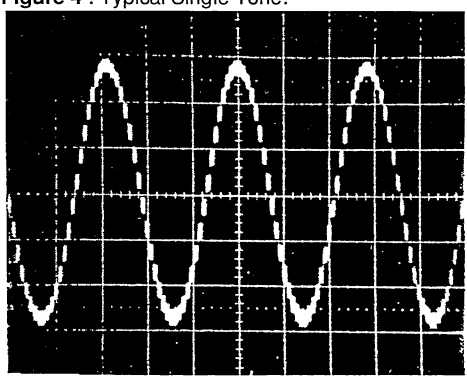
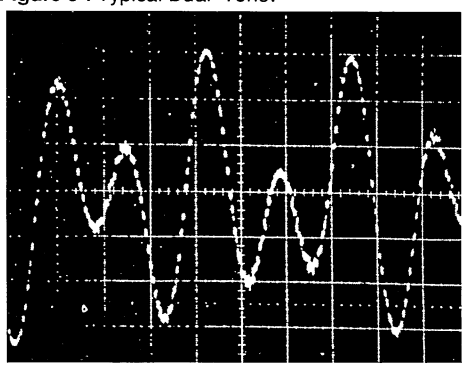


Figure 5 : Typical Dual Tone.



PACIFIER TONE OUTPUT/CHIP DISABLE INPUT

Pin 12. PAC tone is an output. The pacifier tone provides audible feedback, confirming that the key has been properly entered and accepted. A 500 Hz square wave is activated upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all key entries activate the pacifier tone. In tone mode, any non-DTMF key (LND, FLASH, MEM, PROG) entry activates the pacifier tone. When programming the chip, all valid key entries activate the pacifier tone in either pullse or tone mode.

The CHIP DISABLE is an input. When pin 12 is switched low through a resistor (10 K to 100 K), the MK53762 is enabled. When pin 12 is switched to V+ through the resistor, all keypad inputs are pulled high, and the MK53762 will ignore all keypad inputs. When the chip is disabled, it will not dial, and it cannot be programmed. The chip will only be disabled when the circuit is inactive (not dialing) and Pin 12 is switched high.

Figure 6 : Typical Spectral Response.

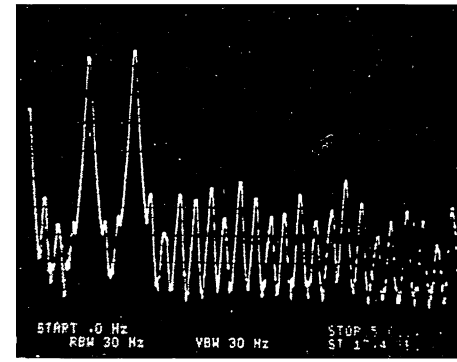
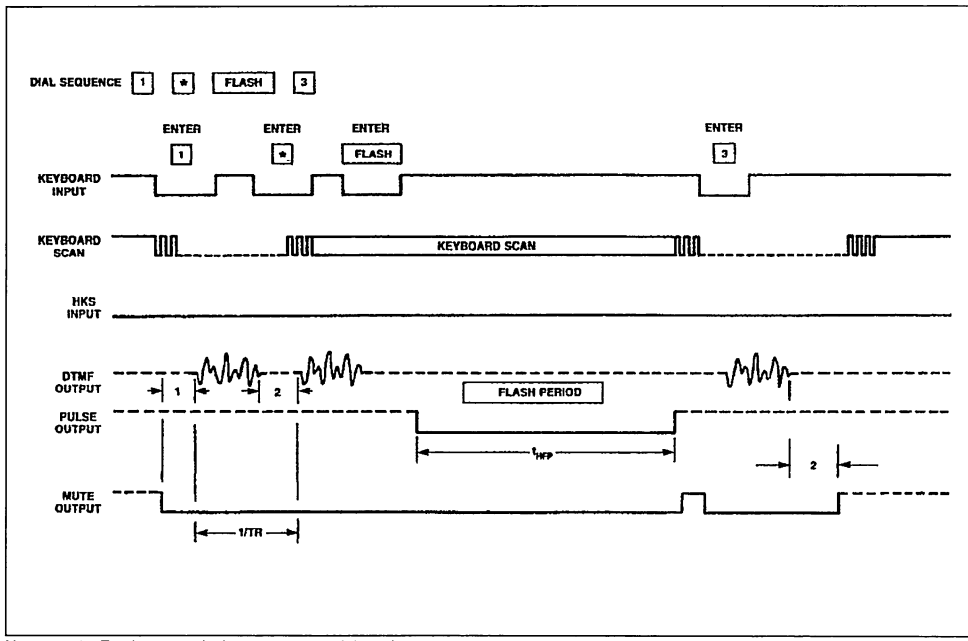


Figure 7 : Tone Mode Timing.



Notes : 1. For this example, key entries are ≤ 75 ms, but ≥ 32 ms.
2. $\overline{\text{MUTE}}$ goes active after any key is depressed.

Figure 8 : Pulse Mode Timing.

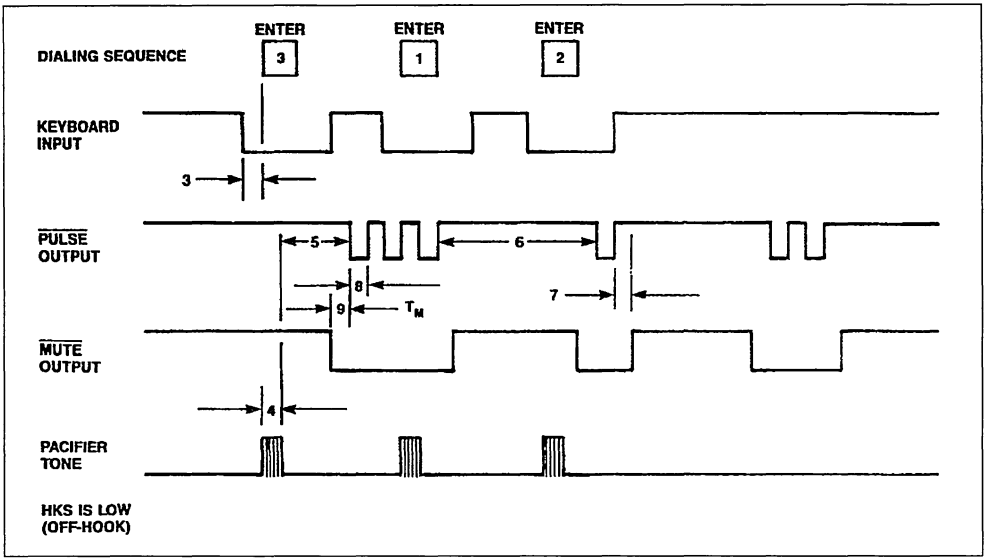


Table 2 : DTMF Output Frequency.

Key Input		Standard Frequency	Actual Frequency	% Deviation
ROW	1	697	699.1	+ 0.31
	2	770	766.2	− 0.49
	3	852	847.4	− 0.54
	4	941	948.0	+ 0.74
COL	1	1209	1215.9	+ 0.57
	2	1336	1331.7	− 0.32
	3	1477	1471.9	− 0.35

MUTE OUTPUT

Output. Pin 13. This pin is the $\overline{\text{MUTE OUTPUT}}$ for both tone and pulse modes. Timing is dependent upon mode.

The $\overline{\text{MUTE OUTPUT}}$ consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In the tone mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE OUTPUT}}$ is active continuously until dialing is completed. $\overline{\text{MUTE OUTPUT}}$ goes active when any key is pushed.

In the pulse mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the receiver and the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE OUTPUT}}$ timing is shown in Figure 8 for pulse mode signaling and Figure 7 for tone mode signaling. $\overline{\text{MUTE OUTPUT}}$ is active during each digit, and not active during the interdigit time. In both tone and pulse modes, $\overline{\text{MUTE OUTPUT}}$ goes active 40 ms before $\overline{\text{PULSE OUTPUT}}$ for a FLASH.

HKS

Input. Pin 19. Pin 19 is the hookswitch input to the MK53762. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2. Figure 8 illustrates the timing for this pin.

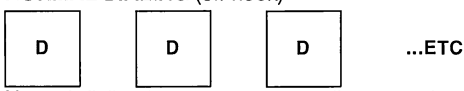
PULSE OUTPUT
Output. Pin 20. This is an output consisting of an open drain N-channel device. In either pulse or tone mode, the FLASH key will cause a 560 ms output pulse at pin 20.

DEVICE OPERATION

When the MK53762 is not actively dialing, it consumes very little current. Row and Column inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of approximately 40 ms (measured from initial key closure). Output tone duration is shown in Table 1.

The MK53762 allows manual dialing of an indefinite number of digits, but if more than 18 digits are dialed per number, the 53762 will "wrap around". That is, the extra digits beyond 18 will be stored at the beginning of the LND buffer, and the first 18 digits will no longer be available for redial. During autodial from LND or any MEM location, key inputs are not accepted, but they will suspend dialing until released.

NORMAL DIALING (off-hook)



Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

Last number dialing is accomplished by entering the LND key.

SOFTSWITCH

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key is depressed. Subsequent * inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

HOOK FLASH

Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed Break of 560 ms. The FLASH function is stored in memory, but it will not be redialed as such. When a FLASH key is pressed, no further key inputs will be accepted until the hook-flash function (560 ms break) has been dialed. The key input following a FLASH will be stored as the initial digit of a new number (overwriting the number dialed prior to the FLASH) unless it is another FLASH. Consecutive FLASH entries after a number is dialed will be stored sequentially in the LND memory and a subsequent LND entry will cause the redial of that number with a delay, but not hookflash breaks, at the end of the redialing sequence. When redialing in tone mode, MUTE OUTPUT will remain active during the flash delay period.

PAUSE

A Pause may be entered into the dialed sequence at any point by keying in the special function key, PAUSE. Pause inserts a 1.1-second delay into the dialing sequence. The total delay, including pre-digital and post-digital pauses is shown in Table 3.

PROGRAMMING AND REPERTORY DIALING

PROGRAMMING AND REPERTORY DIALING
Programming is independent of HKS (pin 19) and MODE (pin 2).

To program, enter the following :

PROG, Digit 1, Digit 2, ..., MEM (Location 1-9). When programming, dialing is inhibited.

To dial a number from repertory memory (HKS must be low) enter the single key :

MEM (Location 1-9)

To save the last number dialed : PROG, MEM (Location 1-9).

Table 3 : Special Function Delays.

Each delay shown below represents the time required from after the special function key is depressed until a new digit can be dialed.
The time is considered "FIRST" key is all previous inputs have been completed dialed. The time is considered "AUTO" if in redial, or previous dialing is still in progress.

Function	First/Auto	Pulse	Tone
SOFTSWITCH	FIRST AUTO	0.40 1.10	- -
PAUSE	FIRST AUTO	1.84 2.50	1.15 1.20

ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
DC Supply Voltage	6.5	V
Operating Temperature	– 20 to + 60	°C
Storage Temperature	– 55 to + 125	°C
Maximum Power Dissipation (25 °C)	500	mW
Maximum Voltage on any Pin	(V^+) + .3 ; (V^-) – .3	V

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V+ TONE	DC Operating Voltage (tone mode)	2.5		6.0	V	
V_{MR}	Memory Retention Voltage	1.5			V	1. 6
I_S	Standby Current		0.4	1.0	µA	1
I_{MR}	Memory Retention Current		0.15	0.75	µA	5. 6
V_{MUTE}	Mute Output Operating Voltage	1.8			V	7
I_T	Operating Current (tone)		300	600	µA	2
I_P	Operating Current (pulse)		150	250	µA	2
	Operating Current On-hook Program Mode Key Operated No-key Operated			 200 1	 µA µA	
I_{ML}	Mute Output (2.5 Volts) Sink Current (4.0 Volts)	1.0 3.0			mA mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		µA	4
K_{RU}	Keypad Pullup Resistance		100		kΩ	
K_{RD}	Keypad Pulldown Resistance		500		Ω	
V_{IL}	Keypad Input Level-low	0		0.3 V +	V	
V_{IH}	Keypad Input Level-high	0.7 V +		V +	V	
V_{PULSE}	Operating Voltage (pulse mode)	1.8		6.0	V	

Notes : 1. All inputs unloaded. Quiescent mode (oscillator off).
2. All outputs unloaded, single key input.
3. V_{OUT} = 0.4 Volts.
4. Sink current for V_{OUT} = 0.5 Volts, Source Current for V_{OUT} = 2.0 Volts.
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum voltage where activation of mute output with key entry is ensured.

ELECTRICAL CHARACTERISTICS (continued)

AC CHARACTERISTICS – TONE MODE

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	T_{NK}	Tone Output no Key Down			– 80	dBm	1
	T_{OI}	Tone Output (independent)	– 13 173	– 12 194	– 11 218	dBm mV_{rms}	1, 2 3
	PE_I	Pre-emphasis, High Band	1.4	2.0	2.6	dB	
	DC_I	Tone Output DC Bias V + = 2.5 V + = 3.5		 1.25 1.5		 V V	
	R_E	Tone Output Load		10		kΩ	4
	T_{RIS}	Tone Output Rise Time		1.0		ms	5
	DIS	Output Distortion		5.0	8.0	%	3
	TR	Tone Signaling Rate		8.0		1/sec	
1	T_{PSD}	Pre-signal Delay	40			ms	6
2	T_{ISD}	Inter-signal Delay (repertory)		54		ms	
	T_{DUR}	Tone Output Duration (repertory)		74		ms	

Notes : 1. O dBm equals 1 mW power into 600 Ω or 775 mVolts Important note : the MK53762 is designed to drive a 10 kΩ load. The 600 Ω load is only for reference.
2 Single tone (low group), as measured at pin 10, $T_A = 25°C$.
3 Supply voltage = 2.5V; R_E = 10 kΩ. T_{OI} increses typically of 10mVrms with V_S = 6V.
4. Supply voltage = 2.5 volts
5 Time from beginning of tone output waveform to 90 % of final magnitude of either frequency Crystal parameters suggested for proper operation are R_S < 100 Ω, L_m = 96 mH, C_m = 0 02 pF, C_h = 5 pF, f = 3.579545 MHz, and C_L = 18 pF.
6. Time from initial key input until beginnig of signaling.

AC CHARACTERISTICS – KEYPAD INPUTS, PACIFIER TONE (numbers in left hand column refer to the timing diagrams.)

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
3	T_{KD}	Keypad Debounce Time		32		ms	1
	F_{KS}	Keypad Scan Frequency		250		Hz	1
	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1
	T_{HFP}	Hookflash Timing		560		ms	1

Note : 1 Crystal oscillator accuracy directly affects these times

AC CHARACTERISTICS – PULSE MODE OPERATION

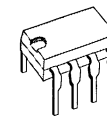
N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	P_R	Pulse Rate		10		PPS	1
5	PDP	Predigital Pause		48		ms	2
6	IDP	Interdigital Pause		740		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2
9	T_M	Make Time		40		ms	2

Notes : 1. 10 PPS is the nominal rate

ML8204
ML8205

TONE RINGER

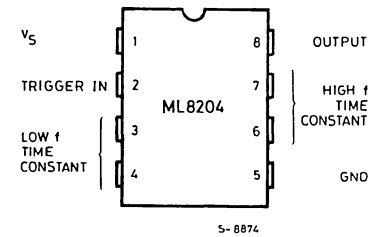
- DESIGNED FOR TELEPHONE BELL REPLACEMENT
- LOW CURRENT DRAIN
- SMALL SIZE "MINIDIP" PACKAGE
- ADJUSTABLE 2-FREQUENCY TONE
- ADJUSTABLE WARBLING RATE
- BUILT-IN HYSTERESIS PREVENTS FALSE TRIGGERING AND ROTARY DIAL "CHIRPS"
- EXTERNAL TRIGGERING OR RINGER DISABLE (ML8204)
- ADJUSTABLE FOR REDUCED SUPPLY INITIATION CURRENT (ML8205)
- TELEPHONE SET TONE RINGERS
- EXTENSION TONE RINGER MODULES
- ALARMS OR OTHER ALERTING DEVICES



Minidip

ORDERING NUMBERS : ML8204
ML8205

PIN CONNECTIONS (top view)



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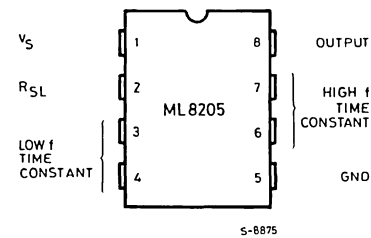
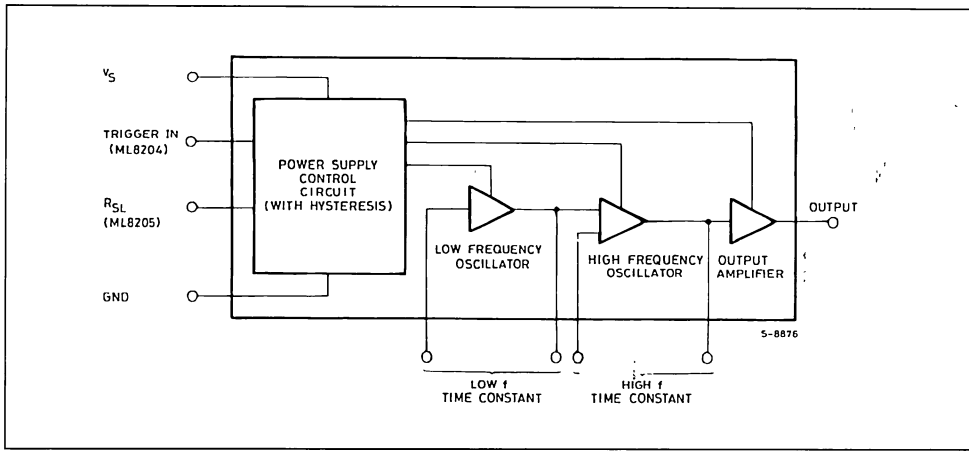


S-8875

DESCRIPTION

The ML8204/ML8205 tone ringers are monolithic devices, each incorporating two oscillators, an output amplifier and a power supply control circuit. The oscillator frequencies can be adjusted over a wide range by selection of external components. One oscillator, normally operated at a low frequency (f_L), causes the second oscillator to alternate between its nominal frequency (f_{H1}), and a related higher frequency (f_{H2}). The resulting output is a distinctive "warbling" tone. The output amplifier will drive either a transformer coupled loudspeaker or a piezo-ceramic transducer. The device can be powered from a telephone line or a fixed d.c. supply. The power supply control circuit has built-in hysteresis to prevent false triggering and rotary dial "chirps". The ML8204 can be triggered externally under logic control. The ML8205 has provision for adjustment of the power supply initiation current.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_S	Supply Voltage - GND	30	V
T_{op}	Operating Temperature	– 45 to + 65	°C
T_{stg}	Storage Temperature (E package)	– 65 to + 150	°C
P_{tot}	Total Power Dissipation (E package)*	400	mW

* Stresses in excess of thos listed unter "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	6.3	mW/°C

ELECTRICAL CHARACTERISTICS

(all voltages referenced to GND unless otherwise noted, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage				29	V
V_{SI}	Supply Initiation Voltage(1)	Trigger in Open Circuit (ML8204)	17	19	21	V
V_{SUS}	Sustaining Voltage(2)		9.7	11	12	V
I_{SI}	Supply Initiation Current	No Load $V_S = V_{SI}$, R_{SL} = 6.8kΩ (ML8205)	1.4	2.5	4.2	mA
I_{SUS}	Sustaining Current	No Load $V_S = V_{SUS}$	0.7	1.2		mA
V_{TR}	Trigger Voltage(3)		10.5			V
I_{TR}	Trigger Current(3)		40		1000(5)	µA
V_{DIS}	Disable Voltage(4)				0.8	V
I_{DIS}	Disable Current(4)		– 50			µA
V_O	Output Voltage	No Load V_S = 21V	17	19	21	V
f_o	Oscillator Frequency Tolerance	Component Tolerance Excluded			± 7	%

Notes : 1. V_{SI} is the value of supply voltage which must be exceeded to trigger oscillation
2 V_{SUS} is the value of supply voltage required to maintain oscillation
3 V_{TR} and I_{TR} are the conditions applied to Trigger In to start oscillation for $V_{SUS} \leq V_S \leq V_{SI}$
4. V_{DIS} and I_{DIS} are the conditions applied to Trigger In to inhibit oscillation for $V_{SI} < V_S$.
5. Trigger Current must be limited to this value externally.

Figure 1a : Supply Current vs. Supply Voltage (no lead).

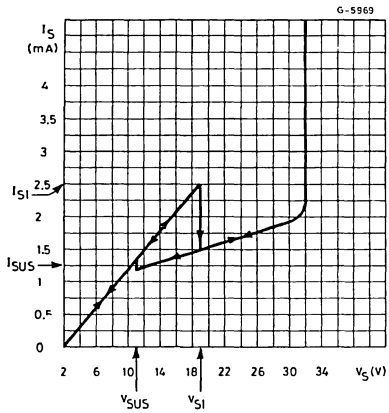
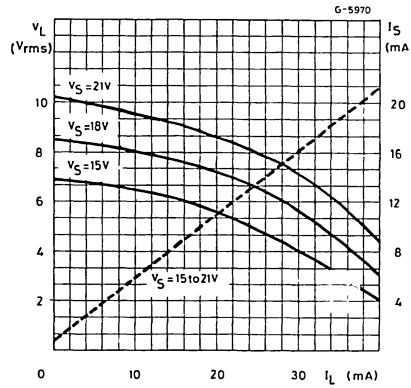


Figure 1b : Load Voltage and Supply Current vs. Load Current.



FUNCTIONAL DESCRIPTION

The M8204/ML8205 Tone Ringers are primarily intended for use as replacements for the mechanical bell in telephone sets. Each incorporates two oscillators, an output amplifier and a power supply control circuit. The devices can be powered directly from the telephone line using the a.c. ringing vol-tage, or they may be powered from a separate d.c. supply. The output amplifier is capable of driving a wide range of load impedances when powered from a low impedance supply. The power supply control circuit provides the hysteresis required to ensure positive triggering of the device and to prevent tran-sient triggering due to dial pulsing.

As the power supply voltage to the ML8204/ML8205 is increased up to the supply initiation voltage (V_{SI}), the supply current also increases up to (I_{SI}). When V_{SI} is exceeded, oscillation begins and the static power supply current decreases (see fig. 2a). The low frequency oscillator (LFO) oscillates at a rate (f_L) controlled by an external resistor and capacitor. The frequency can be determined using the relation $f_L = 1/(1.234RC)$ where R is the value of the resistor connected between pins 3 and 4, and C is the value of the capacitor connected between pin 3 and ground.

The output of the LFO is internally connected to the switching threshold circuitry of the high frequency (HFO). When the output of the LFO is high, HFO oscillates at its nominal rate (f_{H1}), described by the relation $f_{H1} = 1/(1.515RC)$ where R is the value of the resistor connected between pins 6 and 7, and C is the value of the capacitor connected between pin 6 and ground. When the output of the LFO is low, the HFO oscillates at a higher rate (f_{H2}) described by the relation $f_{H2} = 1.25\ f_{H1}$. Thus the LFO sets the warbling rate : the rate at which the HFO switches between the two tone frequencies f_{H1} and f_{H2}. Oscillation continues until the supply voltage decreases below the sustaining voltage (V_{sus}). At this point, the power supply current undergoes a step increase (from I_{sus}), and then ramps down in accoardance with the supply voltage.
In normal applications, Trigger in (pin 2) of the ML8204 is left open circuit. This pin allows external triggering of oscillation of the ML8204 at supply voltages in the range $V_{sus} \leq V_s \leq V_{SI}$. To do so, a vol-tage at least equal to the minimum trigger voltage (V_{TR}) must be applied to pin 2.

Triggering the device is accomplished by sourcing a minimum current (I_{TR}) into pin 2. This current must be limited to prevent damage to the triggering circuit. Tone ringer oscillation may also be inhibited at supply voltages in the range $V_{si} < V_s \leq V_{s(max)}$ by applying a maximum disable voltage (V_{DIS}) to pin 2. Disabling is accomplished by sinking a minimum current (I_{DIS}) out of pin 2. (See Applications Section for details on the operation and use of the Trigger in pin).

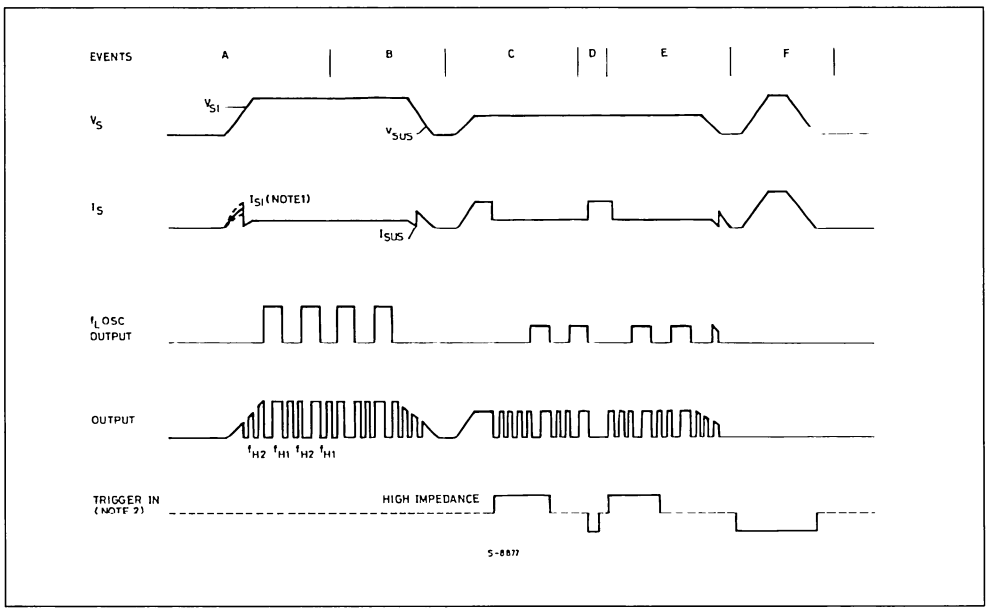
The ML8205 requires the connection of a resistor, R_{SL}, to program the slope of its supply current versus supply voltage characteristic prior to triggering ($V_s \leq V_{si}$). This in turn determines the maximum supply initiation current (I_{si} drawn at the initiation voltage (V_{si})). Programming is accomplished by connecting a slope determining resistor, R_{SL}, bet-ween pin 2 and ground. The value of I_{si} varies inversely with the value of R_{SL}. This feature can be used to control effective impedance presented to the telephone line by the ringer circuit. (See Applications section for detailed description on the operation and use of the R_{SL} pin).

The output amplifier of the ML8204/ML8205 is capable of driving a wide range of load impedances when driven from a low source impedance power supply. When the device is powered from a telephone line, load impedance should be kept fairly high (800 or greater) to prevent power supply regulation problems. A transformer is thus required for driving loudspeakers as is an output coupling capacitor. Piezo-ceramic transducers may be driven directly. However, the tone frequencies f_{H1} and f_{H2} must normally be set higher (around 2 KHz) to ensure that the transducer delivers sufficient acoustic power. (Suitable piezo-ceramic transducers typically have maximum efficiency around 2 KHz). It is also necessary to connect a zener diode in parallel with the transducer to limit voltage surges generated by the transducer during mechanical shocks.

Table 1.

N°	Pin function	Description
1	V_{SS}	Positive Power Supply
2	Trigger in	ML8204 - Oscillator External Trigger/Inhibit pin (must be connected through a current limiting resistor when used)
	R_{SL}	ML8205 - Initiation Current (I_{SI}) Programmming Pin. (must be connected)
3	Low f Time Constant	Low Frequency Time Constant Adjustement Pins. Used to Set Frequency Oscillator Switches f1 (by connection of appropriate resistor and capacitor. see fig. 3)
5	GND	Negative Power Supply
6	High f Time Constant	High Frequency Time Constant Adjustement Pins Used to Set Nominal Tone Output Frequency (f_{H1}) (by connection of appropriate resistor and capacitor. see fig. 3)
8	Output	Tone Output. (must be capacitively coupled for transformer coupled or resistive loads)

Figure 2 : ML8204/ML8205 Timing Diagram.



1. I_{SI} varies with R_{SL} on ML8205
2. Trigger in on ML8204 connected through current limiting resistor.

A) Oscillation triggered by $V_S > V_{SI}$.
B) Oscillation maintained until $V_S < V_{SUS}$.
C) Oscillation triggered by trigger in high for $V_{SUS} \leq V_S \leq V_{SI}$.
D) Oscillation stopped by trigger in low for $Vs \geq V_{SUS}$
E) Oscillation triggered by trigger in high, maintained until $V_S < V_{SUS}$.
F) Oscillation inhibited by trigger in low for $V_S > V_{SI}$

APPLICATIONS

TYPICAL TELEPHONE OR EXTENSION TONE RINGER CIRCUIT

The circuit shown in fig. 3 illustrates the use of the ML8204/8205 devices in a typical telephone or extension tone ringer application. The a.c. ringing voltage appears across the TIP and RING inputs of the circuit and is attenuated by capacitor C_1 and resistor R_1. C_1 also provides isolation from d.c. voltages on the line. After full wave rectification by the diode bridge BR_1, the waveform is filtered by capacitor C_4 to provide a d.c. supply for the tone ringer chip. As this voltage exceeds the initiation voltage, V_{SI}, oscillation starts. With the components shown, the output frequency chops between 512 Hz (f_{H1}) and 640 Hz (f_{H2}) at a 10 Hz (f_L) rate. The loudspeaker load is coupled through a 1300 Ω to 8 Ω transformer. While the output impedance of the ML8204 is quite low, the load impedance must be kept fairly high. This is to prevent d.c. power supply regulation problems due to high source impedance of the telephone line and coupling components C_1 and R_1. The output coupling capacitor C_5 is required with transformer coupled loads. The value shown (0.22 µF) presents a high enough impedance at the nominal ringing frequency to allow connection of fairly low impedance loads without upsetting the supply regulation. If the load impedance is large enough, then the value of this capacitor can be increased to couple more power to the load without upsetting the power supply to the ML8204. Potentiometer P_1, is used to adjust the audio amplitude and resistor R_4 is a current limiting resistor. Resistor R_5 is a quenching resistor used to limit back emf generated by the inductive load when ringing stops. When driving a piezo-ceramic transducer type load, the coupling capacitor C_5 is not required. However, a current limiting resistor is required as is a 29 V zener diode in parallel with the transducer. This diode limits the voltage transients than can generated by mechanical shocking of a piezo-ceramic transducer. The electrical characteristics shown in Table 2 indicate typical performance of this circuit. The incoming ringing voltage and frequency are determined by the telephone system.

Figure 3 : Typical Tone Ringer Circuit.

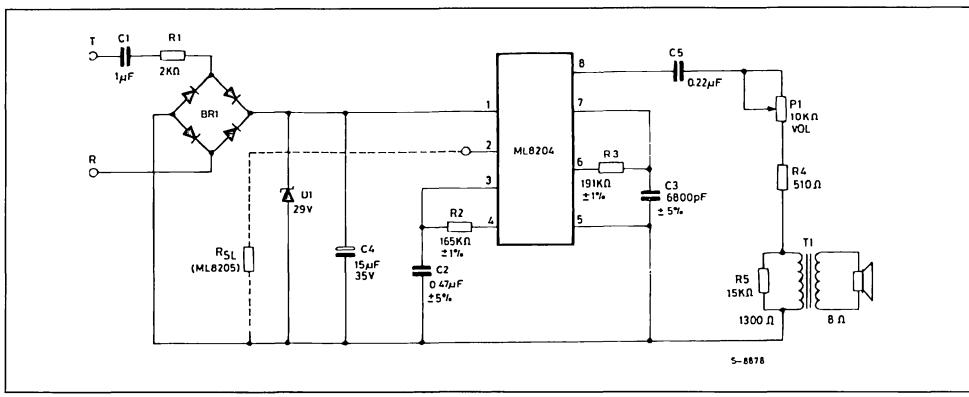


Table 2 : Typical Electrical Characteristics of Tone Ringer Circuit (fig. 3).

Parameter	Min.	Typ.	Max.	Unit	Parameter	Min.	Typ.	Max.	Unit
Input Voltage	75	88	120	V_{RMS}	Output Frequencies				
Input Frequency	16	20	60	Hz	f_L	9	10	11	Hz
					f_{H1}	461	512	563	Hz
					f_{H2}	576	640	704	Hz
Input Current (when ringing)	–	8	11	mA_{RMS}	Output Voltage (Pin 8 '0' loop)	–	25	–	V_{PP}
Output power (into 8 transformer coupled load)	–	40	–	mW	Output Sound Pressure	80	85	90	dBA

USE OF TRIGGER IN (pin 2 ML8204)

Pin 2 of the ML8204 may be used to a) externally trigger oscillation for voltages in the range $V_{sus} \leq V_s \leq V_{si}$, or b) disable ringer operation. The equivalent circuit at pin 2 is shown in Fig. 5. The ringer circuit can only oscillate when Q_1 is conducting. Normally when supply voltage V_s exceeds the supply initiation voltage (V_{si}), base current flows into Q_1, via D_2 and D_1 causing Q_1 to conduct. This continues until V_s is taken below the minimum sustaining voltage (V_{sus}).

The ML8204 can be made to oscillate when powered from supply voltages in the range $V_{sus} \leq V_s \leq V_{si}$. Oscillation is ensured by forcing a current I_{TR} (10 $\mu A \leq I_{TR} \leq 1$ mA) into pin 2 to provide base current to Q_1. This requires the voltage applied to pin 2 to exceed V_{TR} where V_{TR} is the sum of the zener voltage of D_3, the forward voltage drop of D_2 and the V_{BE} of Q_1 (typically 11 V). The required current drive can be provided by connecting a resistor R_E between pin 1 and V_S (Fig. 5a) ; where : $20\ K\Omega \leq R_E \leq (V_S - 11)/10\ M\Omega$. To operate the ML8204 from a d.c. 12 V supply, R_E should be typically 50 K. This mode of operation can also be used to reduce the effective value of the V_{si}, by inserting a zener diode in series with R_E (fig. 5b). This modifies the initiating voltage to $V_{si\ (Eff)} = V_{TR} + V_E + 10\ R_E$ (R_E is in M Ω).

Figure 4 : Pin 2 Input Equivalent Circuit.

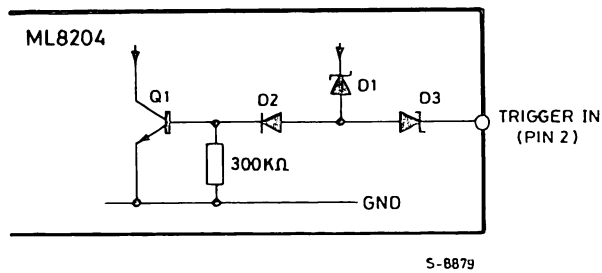
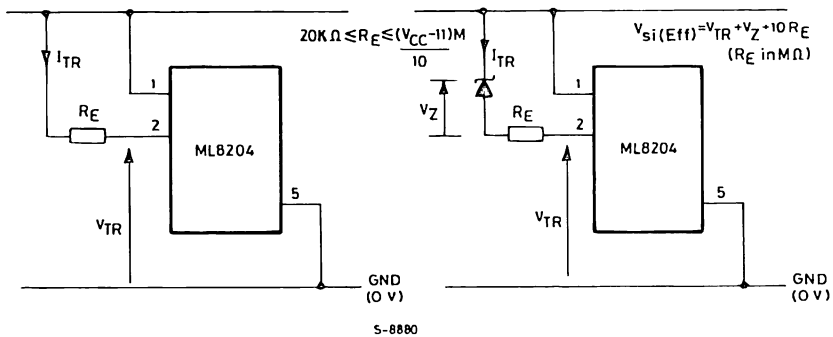


Figure 5a : Enabling Oscillation of the ML8204 for Supply Voltages less than V_{si}.

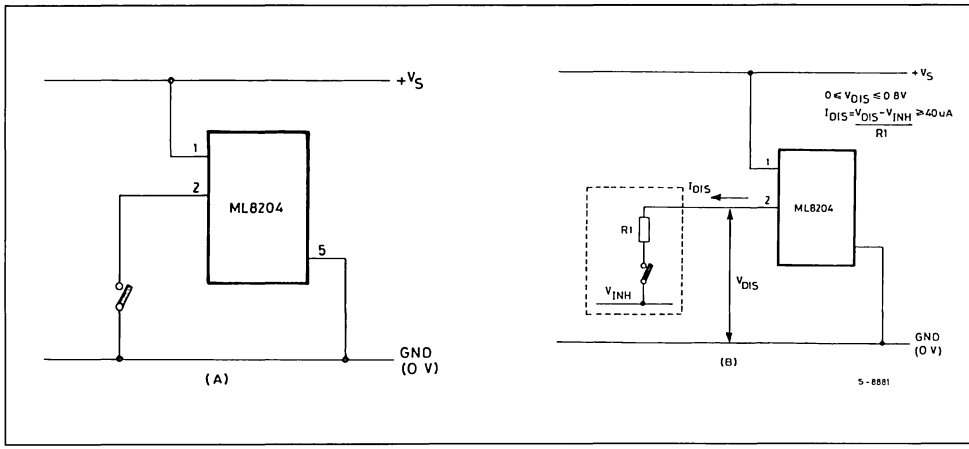
Figure 5b : Reducing the Effective Value of V_{si} for the ML8204



Oscillation of the ML8204 may be inhibited for voltages in the range $V_{si} < Vs \leq V_{s(max)}$ by sinking the current from D_1, starving Q_1 of base current. This is achieved by either a) grounding pin 2 (fig. 6a), or b) applying a voltage V_{INH} via a resistor R_1 to pin 2 (fig. 6b) to ensure that :

V_{DIS} 0.8 V, and $I_{DIS} = \frac{V_{DIS} - V_{INH}}{R_1} \geq 40\ \mu A.$

Figure 6 : Inhibiting Oscillation of the ML8204.



When driven from a fixed d.c. supply, oscillation of the ML8204 may be gated on or off by CMOS or TTL logic as shown in Fig. 7a and Fig. 7b respectively.

PROGRAMMING THE ML8205 INITIATION CURRENT

Figure 7a : Gating the ML8204 from CMOS.

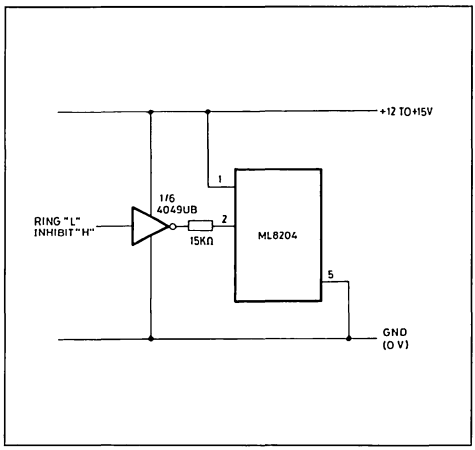
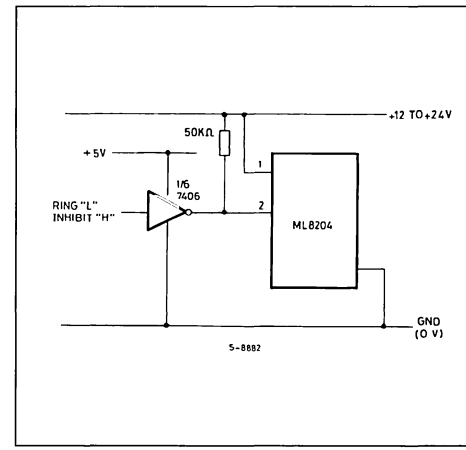


Figure 7b : Gating the ML8204 from TTL.



Pin 2 of the ML8205 requires connection of an external resistor R_{SL} (fig. 8), which is used to program the slope of the supply current vs, supply voltage characteristic, and hence the supply current up to the initiation voltage (V_{si}). This initiation voltage remains constant independent of R_{SL}. The supply initiation current (I_{si}) varies inversely with R_{SL}, decreasing for increasing values of resistance. Thus, increasing the value of R_{SL} will decrease the amount of a.c. ringing current required to trigger the device, As such, longer subscriber loops are possible since less voltage is dropped per unit length of loop wire due to the lower current level. R_{SL} can also be used to compensate for smaller a.c. line coupling capacitors (providing higher impedance) which can be used alter the ringer equivalence number of a tone ringer circuit.

The graph in fig. 9a illustrates the variation of supply current with supply voltage of the ML8205. Three curves are drawn to show the change in the slope of the I-V characteristic with R_{SL}. Curve B (R_{SL} = 6.8 KΩ) shows the I-V characteristic for the ML8204 tone ringer. Curve A is a plot with R_{SL} = 5.0 KΩ and shows an increase in the current drawn up to the initiation voltage V_{si}. The I-V characteristic after initiation remains unchanged. Curve C illustrates the effect of increasing R_{SL} to 13.0 KΩ. Initiation current decreases but again current after trigging is unchanged. The variation of I_{si}, with R_{SL} is illustrated in fig. 9b.

Figure 8 : Adjusting I_{si} by Varying R_{SL}.

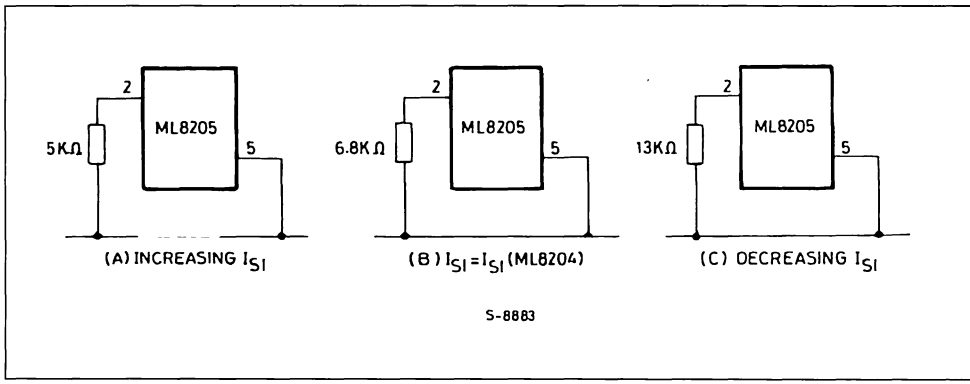


Figure 9a : I-V Slope Change Due to R_{SL}.

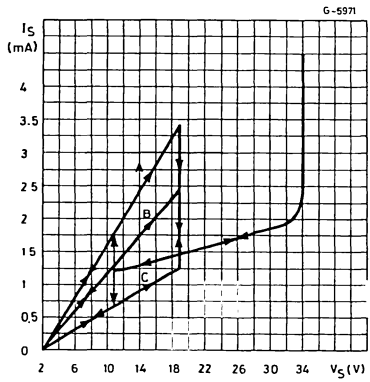
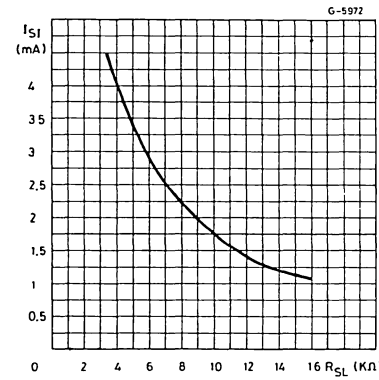


Figure 9b : Supply Initiation Current. (I_{si}) vs. R_{SL}.



MITEL F.C.C. APPROVED TONE RINGER MODULE USING ML8205

The Mitel tone ringer module (CM3215) using the Mitel ML8205 tone ringer chip in the circuit below (fig. 10) has been approved by the F.C.C. (F.C.C. reg. number BN285B673550TN). The circuit has been given a ringer equivalence of 0.7 B. This accomplished by increasing the value of R_{SL} to 13 KΩ which reduces the supply initiation current (I_{SI}). This reduction in I_{SI} allows the use of higher line coupling components (R_1 = 8.2 KΩ) while ensuring sufficient voltage drop between pins 1 and 5 of the ML8205 for triggering. The 5.1 V zener diode D_1 presents a high impedance to low level signals on the telephone line while allowing tone ringer powering from high level rigging voltages.

Figure 10 : F.C.C. Approved Tone Ringer Circuit.

TRANSIENT OVERVOLTAGE TESTING OF THE ML8204 TONE RINGER

The following tests were performed to investigate the ability of the ML8204 to withstand transients on its power supply rails. All tests were performed using the circuit shown in fig. 11 with transient voltage pulses of the form shown in fig. 12. After each application of a transient pulse, functionality of the device was checked by switching S_1, S_2, and S_3 to the configuration shown in fig. 11.

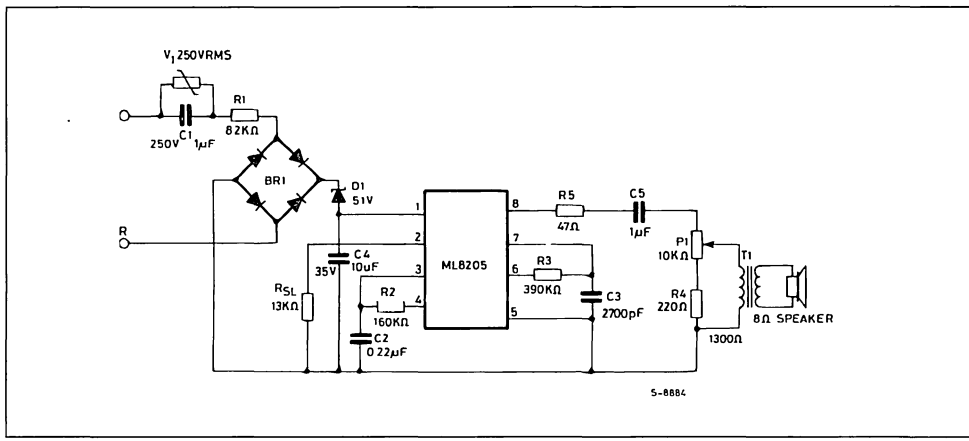
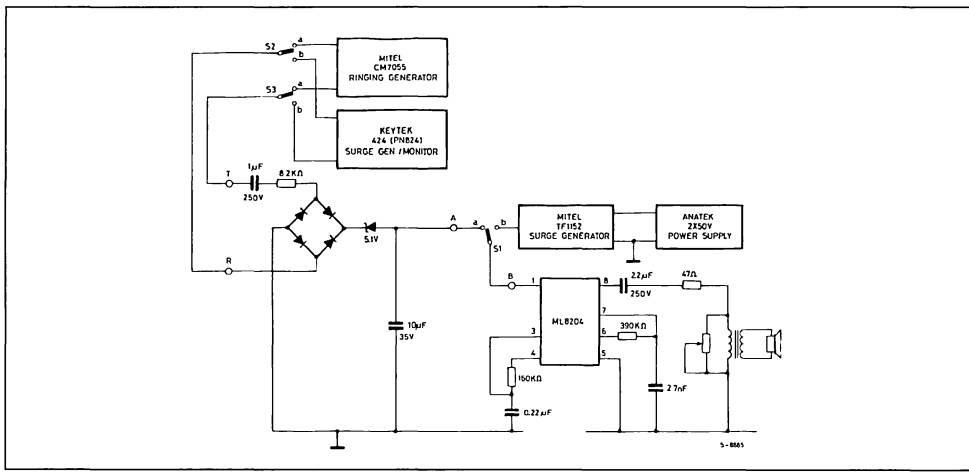


Figure 11 : ML8204 Test Circuit (power supply transient).



The device was tested in two ways by applying pulses : 1) directly into the ML8204 power supply pins, and 2) to the complete ringer circuit TIP and RING inputs. In the first case with S_1 in position "b", a series of pulses with magnitudes (V) from 30 V upwards applied from the TF152 until the ML8204 falled to operate. This was repeated for 10 devices. The unloaded value of V at which the devices ceased to operate varied from 84 to 88 V (V_{BK}). Subsequently a number of devices were tested by applying 70 V pulses to each device. Instability was noted in some devices after 100 pulse applications. All devices ceased to function after 172 to 203 pulse applications. A further set of devices were tested with 64 V pulses. All devices withstood 300 pulse applications without any sign of degradation. In the second test, with switches S_2 and S_3 in position "b" and S_1 in position "a", 800 and 1500 V pulses were repeatedly applied to the TIP and RING inputs of the circuit. No degradation of the devices' operation was observed.

SINGLE TONE OPERATION OF THE ML8204/ML8205

The ML8204/ML8205 can be made to oscillate at one or the other of its output tone frequencies f_{H1} or f_{H2}. To do so, the tone frequency determining components are connected to pins 6 and 7 as normally done. Pin 3 is used as a control input. When pin 3 is connected to V_s, the output (pin 6) will oscillate at the f_{H1} frequency. Conversely, when pin 3 is at ground, the output will oscillate at the f_{H2} frequency. The output can thus be switched between f_{H1} and f_{H2} externally by applying a control signal to pin 3. The low frequency oscillator may also be used separately by connecting the frequency determining components between pins 3 and 4 as normally done. The output is taken from pin 4. However, this is a fairly high impedance output.

Figure 12 : Typical Transient Tset Waveform.

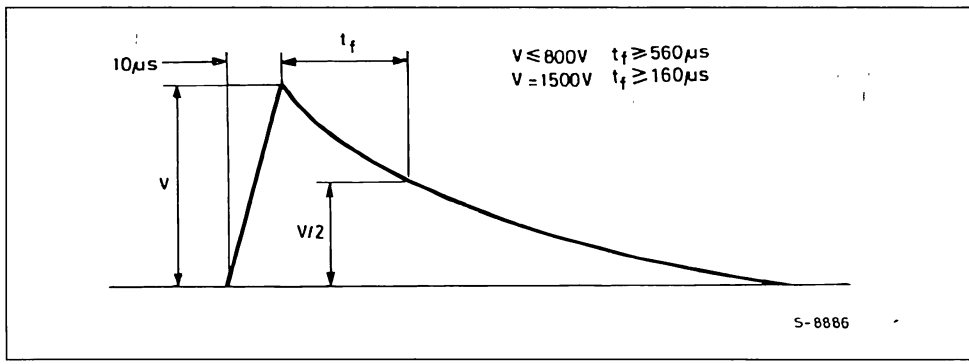
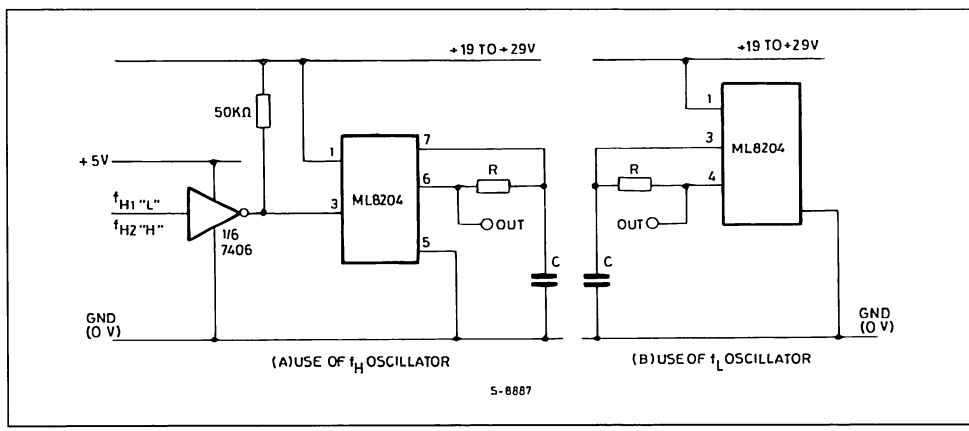


Figure 13 : Single Tone Operating of ML8204/ML8205.



TYPICAL APPLICATION CIRCUITS FOR USE WITH A PIEZO-ELECTRIC TRANSDUCER

Feedback from a piezo-electric transducer can cause spurious oscillations on the output of a ML8204/5 tone ringer. These oscillations corrupt the normal two-tone output and change as the ringer switches off.

The oscillations occur because the piezo electric transducer resonates at its characteristic frequency. If the resonant amplitude is sufficient to pull pin 8 one bipolar threshold below pin 5 then the tone ringer may give a short spurious pulse.

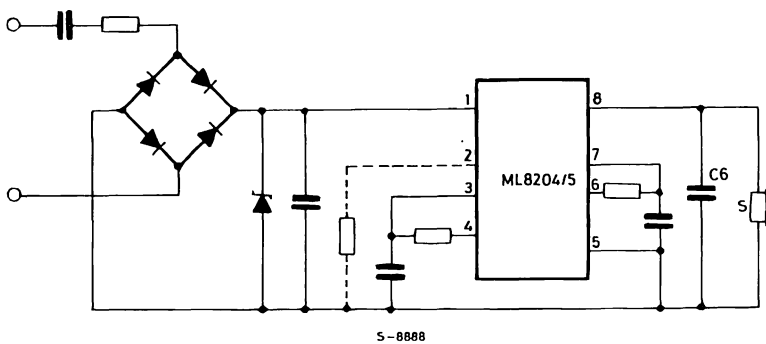
This effect can be eliminated by using a bypass capacitor across the transducer as shown in fig. 14. The size of this capacitor is obviously dependent on the piezo-electric transducer used, but a value of 0.1 µF is usually sufficient.

It is possible under specific conditions for a ML8204/5 tone ringer with a piezo-electric load to continue oscillating after the ringing voltage stops. The ringer can be powered by the smoothing capacitor which is across pins 1 and 5 (see fig. 14). This causes the device to switch off slowly and since the output frequencies shift by about a musical semitone before oscillation stops, the output can have an unpleasant tail-off.

To eliminate this, a simple monitor can be used which switches the output off when ringing stops. fig. 16 shows a circuit which works with an ML8204. When ringing voltage is applied from the line, pin 2 is held between 2 and 10 V and the device functions normally. When ringing stops, pin 2 is pulled to ground and the ML8204 switches off.

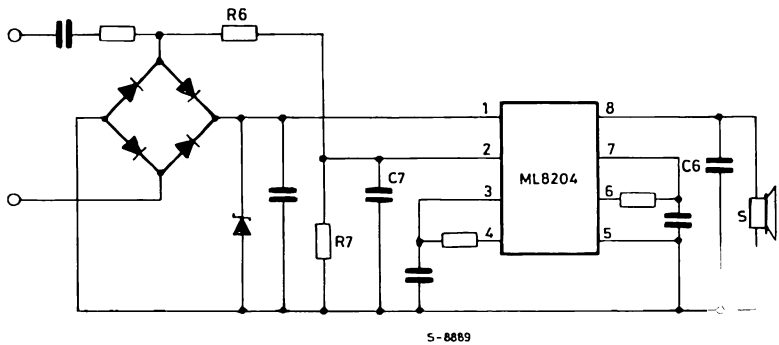
There is no enable on the ML8205 corresponding to pin 2 on the ML8204. Fig. 16 shows a circuit which does not require the enable pin. The output is switched through an NPN transistor instead. During ringing the base of the transistor is forward biased and the load is enabled. When ringing stops the transistor switches off and deactivates the load.

Figure 14 : Typical Application Circuit for Use with a Piezo-electric Transducer..



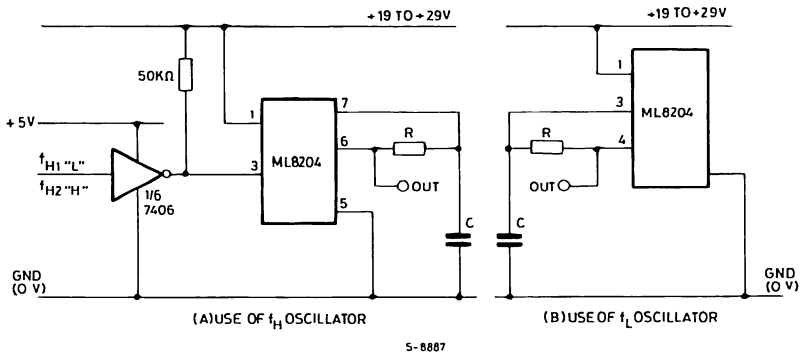
C6 = 01 µF
S = Piezo-electric transducer
Other components same as figure 3

Figure 15 : ML 8204 Circuit to Eliminate Tail-off.



C6 = 0.1 µF
C7 = 4.7 µF
R6 = 51 KΩ
R7 = 22 KΩ
S = Piezo-electric Transducer
Other Components Same as fig. 3

Figure 16 : ML8204/5 Circuit to eliminate Tail-off.



C6 = 0.1 µF
C7 = 4.7 µF
R6 = 51 KΩ
R7 = 22 KΩ
S = Piezo-electric Transducer
Other Components Same as fig. 3

SGS-THOMSON MICROELECTRONICS

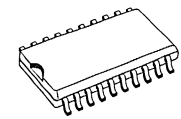
ST3854

ELECTRONIC HOOK SWITCH

PRODUCT PREVIEW

- ANALOG LINE INTERFACE
- ON HOOK DIALING AND CALL PROGRESS MONITORING FACILITIES
- PULSE DIALING INTERFACE
- CURRENT LIMITATION ON BOARD
- ANTI-TINKLE (FOR PARALLEL RINGER)
- RINGER INTERFACE (INCLUDING RECTIFIER BRIDGE)
- FRENCH D.C. CHARACTERISTIC (SELECTABLE)
- "TAKE THE LINE" COMMAND FOR SPECIAL PHONES
- LINE CURRENT INFORMATION FOR AGC LINEARIZATION PURPOSE
- LESS THAN 10µA LEAKAGE AT 50V

MULTIPOWER BCD TECHNOLOGY



SO20

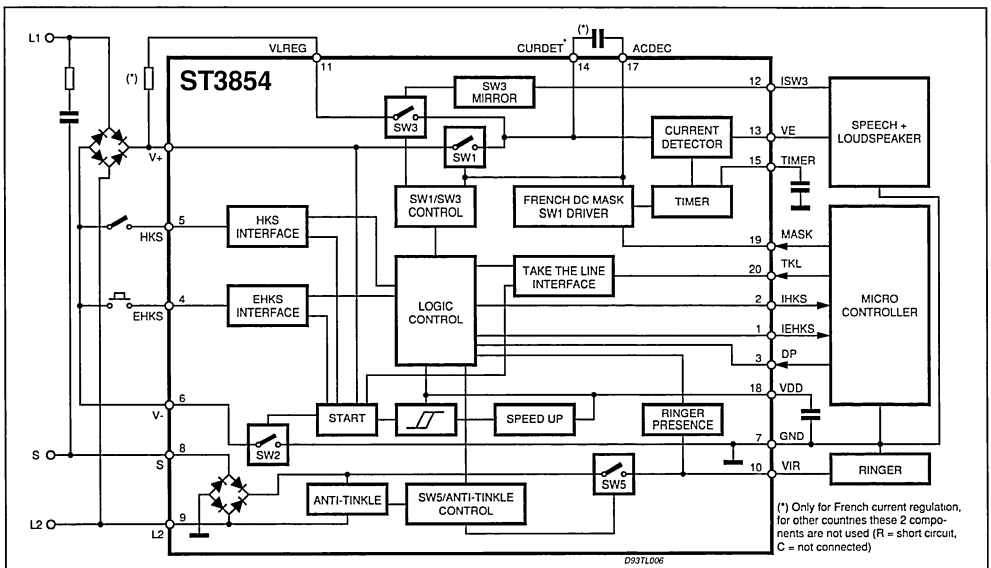
DESCRIPTION

The Electronic Hook Switch IC is designed to perform the high voltage analog interface function on corded telephones equipped with "**on-hook dialing**" or "hands-free" features, on cordless phones or on answering machines.
The device is specially intended for use in applications controlled by microcontroller.

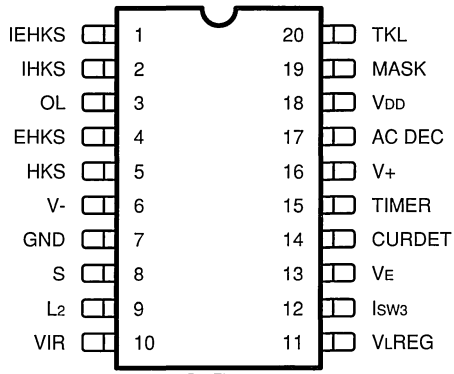
The high voltage switches are N-channel/D-MOS and P-channel/Drain Extension MOS transistors integrated in a mixed technology, Bipolar C-MOS-DMOS at 250V ratings, BCD250.

The ringer interface is provided on board. It is designed in order to avoid any circulation of current between speech and ringer sections during operation, specially in applications with common ground, like solutions based on microcontroller.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



PINS FUNCTIONS

N°	Name	Description
1	IEHKS	LOGIC OUTPUT (EHKS BUTTON INPUT STATUS) Output logic signal (open drain) following the status of PLSD key (no debounced output). EHKS button pressed IEHKS = 0 EHKS button released IEHKS = 1 (open)
2	IHKS	LOGIC OUTPUT (HKS SWITCH INPUT STATUS) Output logic signal (open drain) following the status of mechanical hook-switch (no debounced output). HKS Key closed IHKS = 0 HKS key open IHKS = 1 (open)
3	OL	PULSE DIALING INPUT Open line input signal for pulse dialing or flashing option.
4	EHKS	BUTTON INPUT (ELECTRONIC HOOK SWITCH) Input from key board, internally latched to "take the line".
5	HKS	HOOK SWITCH SENSOR Hook switch sensor operated by handset hook.
6	V⁻ Line	NEGATIVE SPEECH BRIDGE Output connection with negative path of the ringer rectifier bridge.
7	GND	SUBSTRATE Common reference point (substrate).
8	S	PARALLEL RINGER INHIBITION IN PULSE MODE Output connection to the third line wire (additional ringer/parallel telephone set).
9	L_2	LINE WIRE Output connection with the L_2 terminal.
10	V_{IR}	POSITIVE RINGER SUPPLY VOLTAGE
11	V_{LREG}	LINE CURRENT REGULATION EXTERNAL RESISTOR INPUT Output connection to external resistor for line current regulation (French characteristic).
12	I_{SW3}	AGC CURRENT LINEARITY INFORMATION Current information flowing in SW3 switch (for AGC speech correction with French regulation or for other monitor of line current).
13	V_E	POSITIVE SPEECH SUPPLY Positive power supply for speech circuits.
14	CURDET	LINE CURRENT DETECTOR Output connection with external AC decoupling capacitor and internal current detector.

PINS FUNCTIONS (continued)

N°	Name	Description
15	TIMER	FRENCH CHARACTERISTIC AND FILTER CAPACITOR Connection for external capacitor to program current limitation during Off-Hook transition time.
16	V^+ Line	POSITIVE SPEECH BRIDGE Output connection with positive path of ringer rectifier bridge.
17	AC DEC	AC DECOUPLING IN CURRENT REGULATION MODE Connection for external AC decoupling capacitor.
18	V_{DD}	INTERNAL POWER SUPPLY DC Voltage for internal logic supply.
19	MASK	CURRENT SETTING RESET –Power down reset activated by external command after line break longer than 300ms (to reset Off-Hook current limitating in French market). –Pulse dialing mask to set the current limiting (French market).
20	TKL	TAKE THE LINE / EHS COMMAND External logic command, 5V, to **"take the line"** (for cordless and answering machines).

SGS-THOMSON MICROELECTRONICS

ST5080A

PIAFE
PROGRAMMABLE ISDN AUDIO FRONT END

ADVANCE DATA

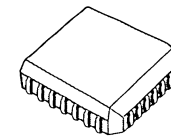
FEATURES:

Complete CODEC and FILTER system including:

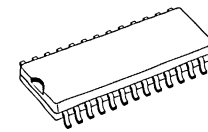
- PCM ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS
- POWERFUL ANALOG FRONT END CAPABLE TO INTERFACE DIRECTLY:
  - Microphone Dynamic, Piezo or Electrete
  - Earpiece down to 100Ω or up to 150nF
  - Loudspeaker down to 50Ω or Buzzer up to 600nF.
- TRANSMIT BAND-PASS FILTER
- ACTIVE RC NOISE FILTER
- RECEIVE LOW-PASS FILTER WITH SIN X/X CORRECTION
- MU-LAW OR A-LAW SELECTABLE COMPANDING CODER AND DECODER
- PRECISION VOLTAGE REFERENCE

Phones Features:

- DUAL SWITCHABLE MICROPHONE AMPLIFIER INPUTS. GAIN PROGRAMMABLE: 15 dB RANGE, 1 dB STEP.
- LOUDSPEAKER AMPLIFIER AUXILIARY OUTPUT. ATTENUATION PROGRAMMABLE: 30 dB RANGE, 2 dB STEP.
- SEPARATE EARPIECE AMPLIFIER OUTPUT. ATTENUATION PROGRAMMABLE: 15 dB RANGE, 1 dB STEP
- AUXILIARY SWITCHABLE EXTERNAL RING INPUT (EAIN).
- TRANSIENT SUPRESSION SIGNAL DURING POWER ON.
- INTERNAL PROGRAMMABLE SIDETONE CIRCUIT. ATTENUATION PROGRAMMABLE: 15 dB RANGE, 1 dB STEP.
- INTERNAL RING OR TONE GENERATOR INCLUDING DTMF TONES, SINEWAVE OR SQUAREWAVE WAVEFORMS. ATTENUATION PROGRAMMABLE: 27 dB RANGE, 3 dB STEP.
- COMPATIBLE WITH HANDS-FREE CIRCUIT TEA7540.
- ON CHIP SWITCHABLE ANTI-ACOUSTIC FEED-BACK CIRCUIT (ANTI-LARSEN).



PLCC28



SO28

ORDERING NUMBERS: ST5080FN (PLCC28)
ST5080D (SO28)

General Features:

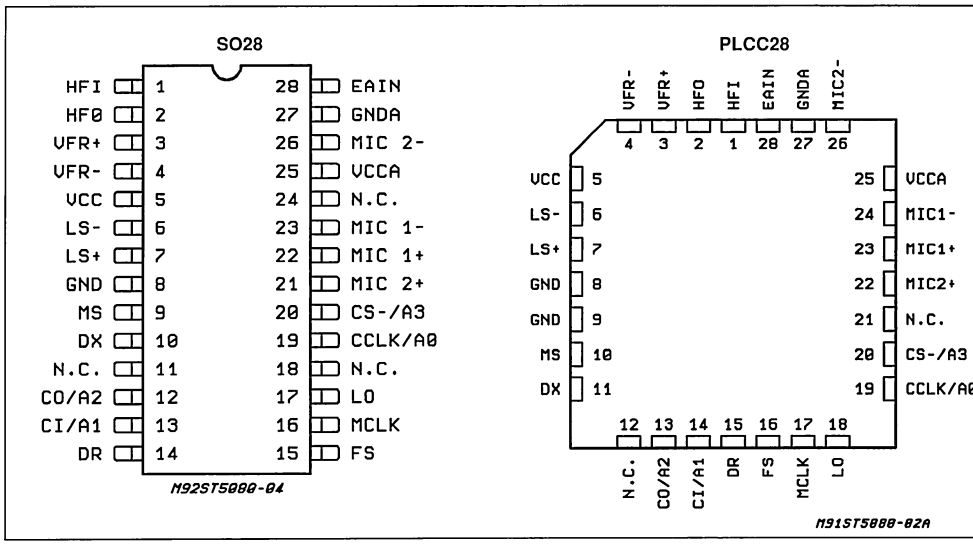
- EXTENDED TEMPERATURE RANGE OPERATION (*) – 40°C TO +85°C.
- EXTENDED POWER SUPPLY RANGE 5V±10%.
- 60 mW OPERATING POWER (TYPICAL).
- 1.0 mW STANDBY POWER (TYPICAL).
- CMOS DIGITAL INTERFACES.
- SINGLE + 5V SUPPLY.
- DIGITAL LOOPBACK TEST MODE.
- PROGRAMMABLE DIGITAL AND CONTROL INTERFACES:
  - Digital PCM Interface associated with separate serial Control Interface MICROWIRE™ compatible.
  - GCI interface compatible.

(*) Functionality guaranteed in the range – 40°C to +85°C; Timing and Electrical Specifications are guaranteed in the range – 25°C to +85°C.

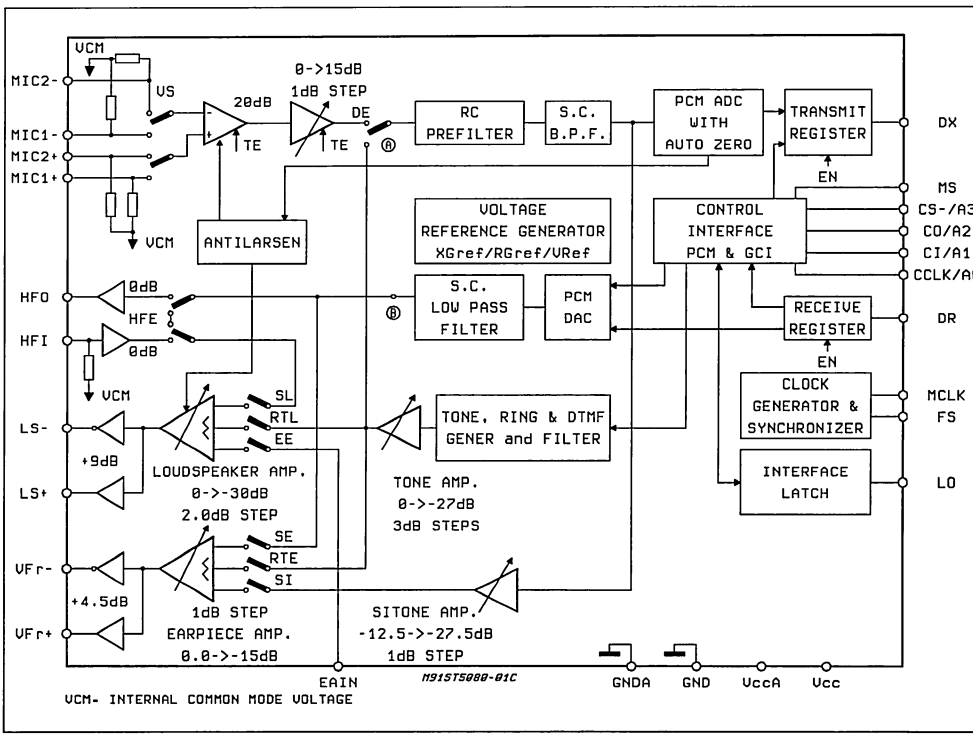
APPLICATIONS:

- ISDN TERMINALS.
- DIGITAL TELEPHONES
- CT2 AND GSM APPLICATIONS

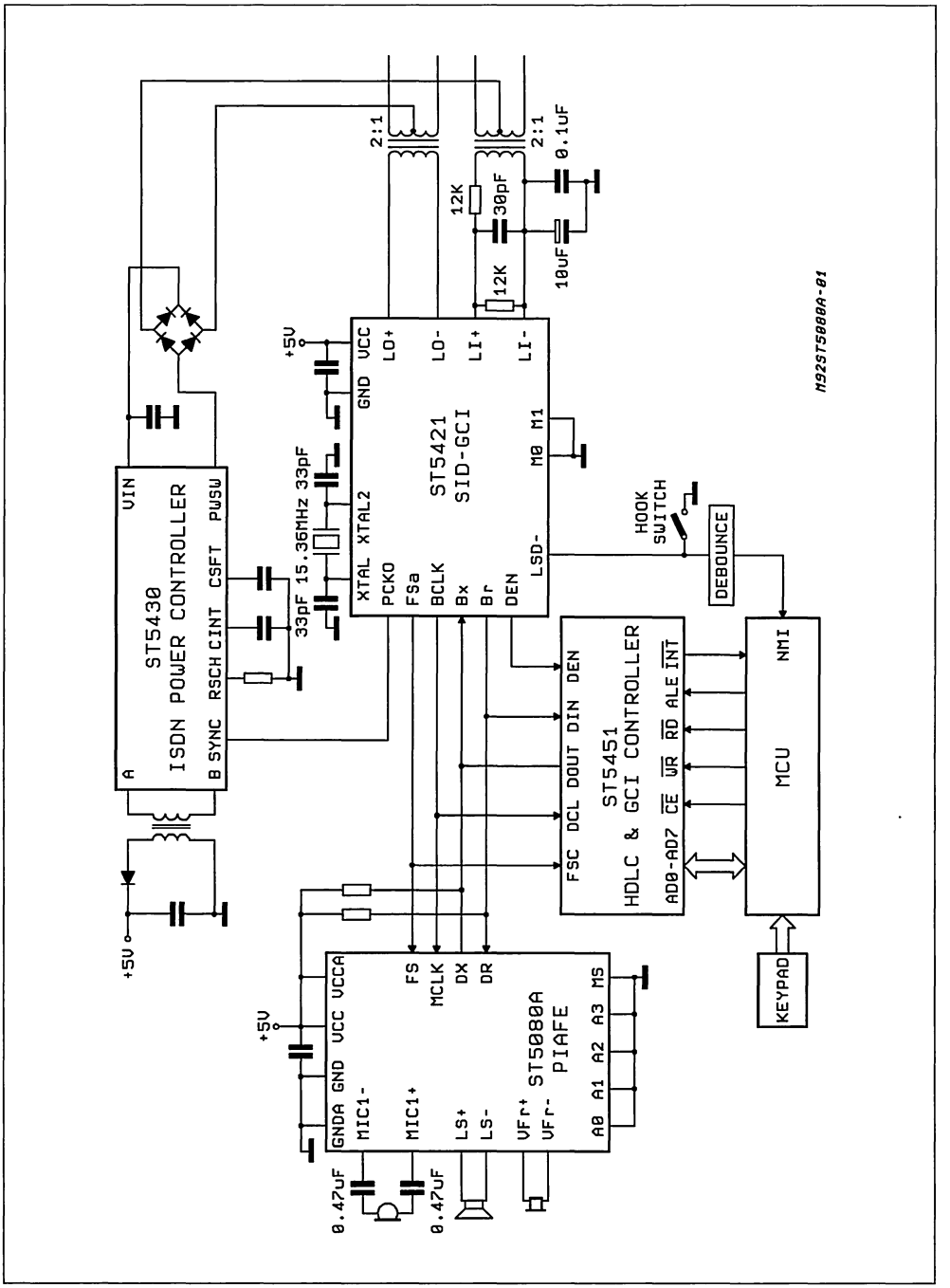
PIN CONNECTIONS (Top view)



BLOCK DIAGRAM



TYPICAL ISDN TELEPHONE SET APPLICATION



GENERAL DESCRIPTION

ST5080A PIAFE is a combined PCM CODEC/FILTER device optimized for ISDN Terminals and Digital Telephone applications. This device is A-law and Mu-law selectable and offers a number of programmable functions accessed through a serial control channel.

Depending on mode selected, channel control is provided by means of a separate serial channel control MICROWIRE compatible or multiplexed with the PCM voice data channel in a GCI compatible format requiring only 4 digital interface pins. When separate serial control interface is selected, PCM interface is compatible with Combo I and Combo II families of devices such as ETC5057/54, TS5070/71.

PIAFE is built using SGS-THOMSON's advanced HCMOS process.

Transmit section of PIAFE consists of an amplifier with switchable high impedance inputs followed by a programmable gain amplifier, an active RC antialiasing pre-filter to provide attenuation of high frequency noise, an 8th order switched capacitor band pass transmit filter and an A-law/Mu-law selectable compandig encoder.

Receive section consist of an A-law/Mu-law selectable expanding decoder which reconstructs the analog sampled data signal, a 3400 Hz low pass filter with sin X/X correction followed by two separate programmable attenuation blocks and two power amplifiers: One can be used to drive an earpiece, and the other to drive a 50 Ω loudspeaker.

Programmable functions on PIAFE include a Ring/Tone generator which provides one or two tones and can be directed to earpiece or to loudspeaker or alternatively a piezo transducer up to 600nF.

A separate programmable gain amplifier allows gain control of the signal injected. Ring/Tone generator provides sinewave or squarewave signal with precise frequencies which may be also directed to the input of the Transmit amplifier for DTMF tone generation.

An auxiliary analog input (EAIN) is also provided to enable for example the output of an external band limited Ring signal to the Loudspeaker. Transmit signal may be fed back into the receive ampifier with a programmable attenuation to provide a sidetone circuitry.

A switchable anti-accoustic feed-back system cancels the larsen effect in speech monitoring application.

Two additional pins are provided for insertion of an external Handfree function in the Loudspeaker receive path.

An output latch controlled by register programming permits external device control.

PIN FUNCTIONS: PLCC28 / **(SO28)**

Pin	Name	Description
1,2 **(1, 2)**	HFI, HFO	Hands free I/Os: These two pins can be used to insert an external Handfree circuit such as the TEA 7540 in the receive path. HFO is an output which provides the signal issued from output of the receive low pass filter while HFI is a high impendance input which is connected directly to one of the inputs of the Loudspeaker amplifier.
3,4 **(3, 4)**	V_{Fr+}, V_{Fr-}	Receive analog earpiece amplifier complementary outputs, capable of driving load impedances between 100 and 400 Ω or a piezo up to 150nF. These outputs can drive directly earpiece transductor. The signal at this output can drive be the summ of: - Receive Speech signal from D_R, - Internal Tone Generator, - Sidetone signal.
5 **(5)**	V_{CC}	Positive power supply input for the digital section. +5 V ± 10%.
6,7 **(6, 7)**	LS-,LS+	Receive analog loudspeaker amplifier complementary outputs, intended for driving a Loudspeaker: 80 mW on 50Ω load impedance can be provided at low distorsion meeting specifications. Alternatively this stage can drive a piezo transducer up to 600nF. The signal at these outputs can be the sum of: - Receive Speech signal from D_R, - Internal Tone generator, - External input signal from EAIN input.

PIN FUNCTIONS (continued)

Pin	Name	Description
10 **(9)**	MS	Mode Select: This input selects COMBO I/II interface mode with separate MICROWIRE Control interface when tied high and GCI mode when tied low.
11 **(10)**	D_X	Transmit Data ouput: Data is shifted out on this pin during the assigned transmit time slots. Elsewhere D_X output is in the high impendance state. In COMBO I/II mode, voice data byte is shifted out from TRISTATE output D_X at the MCLK frequency on the rising edge of MCLK. In GCI mode, voice data byte and control bytes are shifted out from OPEN-DRAIN output D_X at half the MCLK. An external pull up resistor is needed.
12 **(11)**	N.C.	No Connected.
15 **(14)**	D_R	Receive data input: Data is shifted in during the assigned Received time slots. In the COMBO I/II mode, voice data byte is shifted in at the MCLK frequency on the falling edges of MCLK. In the GCI mode, PCM data byte and contol byte are shifted in at half the MCLK frequency on the receive rising edges of MCLK. There is one period delay between transmit rising edge and receive rising edge of MCLK.
16 **(15)**	FS	Frame Sync input: This signal is a 8kHz clock which defines the start of the transmit and receive frames. Either of three formats may be used for this signal: non delayed timing mode, delayed timing and GCI compatible timing mode.
17 **(16)**	MCLK	Master Clock Input: This signal is used by the switched capacitor filters and the encoder/decoder sequencing logic. Values must be 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz selected by means of Control Register CR0. MCLK is used also to shift-in and out data. In GCI mode, 2.56 MHz and 512 kHz are not allowed.
18 **(17)**	LO	Open drain output: a logic 1 written into DO (CR1) appears at LO pin as a logic 0 a logic 0 written into DO puts LO pin in high impedance.
21 **(18,24)**	N.C.	No Connected.
22 **(21)**	MIC2+	Alternative positive high impedance input to transmit pre-amplifier.
23 **(22)**	MIC1+	Positive high impedance input to transmit pre-amplifier for microphone symetrical connection.
24 **(23)**	MIC1-	Negative high impedance input to transmit pre-amplifier for microphone symetrical connection.
25 **(25)**	V_{CCA}	Positive power supply input for the analog section. +5 V ± 10%. V_{CC} and V_{CCA} must be directly connected together.
26 **(26)**	MIC2-	Alternative negative high impedance input to transmit pre-amplifier.
27 **(27)**	GNDA	Analog Ground: All analog signals are referenced to this pin. GND and GNDA must be connected together close to the device.
28 **(28)**	EAIN	External Auxiliary input: This input can be used to provide alternate signals to the Loudspeaker in place of Internal Ring generator. Input signal should be voice band limited.

Following pin definitions are used only when COMBO I/II mode with separate MICROWIRE compatible serial control port is selected. (MS input set equal one)

PIN FUNCTIONS (continued)

Pin	Name	Description
13 **(12)**	CO	Control data Output: Serial control/status information is shifted out from the PIAFE on this pin when CS- is low on the falling odges of CCLK.
14 **(13)**	CI	Control data Input: Serial Control information is shifted into the PIAFE on this pin when CS- is low on the rising edges of CCLK.
19 **(19)**	CCLK	Control Clock input: This clock shifts serial control information into CI and out from CO when the CS- input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
20 **(20)**	CS-	Chip Select input: When this pin is low, control information is written into and out from the PIAFE via CI and CO pins.

Following pin definitions are used only when the GCI mode is selected. (MS input set equal zero)

PIN FUNCTIONS (continued)

Pin	Name	Description
19,14,13,20 **(19,13,12,20)**	A0,A1,A2,A3	These pins select the address of PIAFE on GCI interface and must be hardwired to either V_{CC} or GND. A0,A1,A2,A3 refer to C4,C5,C6,C7 bits of the first address byte respectively.

FUNCTIONAL DESCRIPTION

Power on initialization:
When power is first applied, power on reset circuitry initializes PIAFE and puts it into the power down state. Gain Control Registers for the various programmable gain amplifiers and programmable switches are initialized as indicated in the Control Register description section. All CODEC functions are disabled. Digital Interface is configured in GCI mode or in COMBO I/II mode depending on Mode Select pin connection.
The desired selection for all programmable functions may be intialized prior to a power up command using Monitor channel in GCI mode or MICROWIRE port in COMBO I/II mode.

Power up/down control:
Following power-on initialization, power up and power down control may be accomplished by writing any of the control instructions listed in Table 1 into PIAFE with "P" bit set to 0 for power up or 1 for power down.
Normally, it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or in a separate single byte instruction.
Any of the programmable registers may also be modified while ST5080A is powered up or down by setting "P" bit as indicated. When power up or down control is entered as a single byte instruction, bit 1 must be set to a 0.
When a power up command is given, all de-activated circuits are activated, but output D_X will remain in the high impedance state on B time slots until the second Fs pulse after power up, even if a B channel is selected.

Power down state:
Following a period of activity, power down state may be reentered by writing a power down instruction.
Control Registers remain in their current state and can be changed either by MICROWIRE control interface or GCI control channel depending on mode selected.
In addition to the power down instruction, detection of loss MCLK (no transition detected) automatically enters the device in "reset" power down state with D_X output in the high impedance state and L0 in high impedance state.

Transmit section:
Transmit analog interface is designed in two stages to enable gains up to 35 dB to be realized. Stage 1 is a low noise differential amplifier providing 20 dB gain. A microphone may be capacitevely connected to MIC1+, MIC1- inputs, while the MIC2+ MIC2– inputs may be used to capacitively connect a second microphone (for digital handsfree operation) or an auxiliary audio circuit such as TEA 7540 Hands-free circuit. MIC1 or MIC2 source is selected with bit 7 of register CR4.
Following the first stage is a programmable gain amplifier which provides from 0 to 15 dB of additional gain in 1 dB step. The total transmit gain should be adjusted so that, at reference point A, see Block Diagram description, the internal 0 dBmO voltage is 0.739 V (overload level is 1.06 Vrms). Second stage amplifier can be programmed with bits 4 to 7 of CR5. To temporarily mute the transmit input, bit TE (6 of CR4) may be set low. In this case, the analog transmit signal is grounded and the sidetone path is also disabled.
An active RC prefilter then precedes the 8th order band pass switched capacitor filter. A/D converter has a compressing characteristic according to CCITT A or mu255 coding laws, which must be selected by setting bits MA, IA in register CR0. A precision on chip voltage reference ensures accurate and highly stable transmission levels.
Any offset voltage arising in the gain-set amplifier, the filters or the comparator is cancelled by an internal autozero circuit.
Each encode cycle begins immediatly at the beginning of the selected Transmit time slot. The total signal delay referenced to the start of the time slot is approximatively 195 µs (due to the transmit filter) plus 123 µs (due to encoding delay), which totals 320 µs. Voice data is shifted out on D_X during the selected time slot on the transmit rising adges of MCLK.

Receive section:
Voice Data is shifted into the decoder's Receive voice data Register via the D_R pin during the selected time slot on the 8 receive edges of MCLK.
The decoder consists of an expanding DAC with either A or MU255 law decoding characteristic which is selected by the same control instruction used to select the Encode law during intitialization. Following the Decoder is a 3400 Hz 6th order low pass switched capacitor filter with integral Sin X/X correction for the 8 kHz sample and hold.
0 dBmO voltage at this (B) reference point (see Block Diagram description) is 0.49 Vrms. A transcient suppressing circuitry ensure interference noise suppression at power up.
The analog speech signal output can be routed either to earpiece (V_{FR+}, V_{FR-} outputs) or to loudspeaker (LS+, LS- outputs) by setting bits SL and SE (1 and 0 of CR4).
Total signal delay is approximatively 190 µs (filter plus decoding delay) plus 62.5 µs (1/2 frame) which gives approximatively 252 µs.

Differential outputs V_{FR+},V_{FR-} are intended to directly drive an earpiece. Preceding the outputs is a programmable attenuation amplifier, which must be set by writing to bits 4 to 7 in register CR6. Attenuations in the range 0 to -15 dB relative to the maximum level in 1 dB step can be programmed. The input of this programmable amplifier is the summ of several signals which can be selected by writing to register CR4.:

- Receive speech signal which has been decoded and filtered,
- Internally generated tone signal, (Tone amplitude is programmed with bits 4 to 7 of register CR7),
- Sidetone signal, the amplitude of which is programmed with bits 0 to 3 of register CR5

V_{FR+} and V_{FR-} outputs are capable of driving output power level up to 14mW into differentially connected load impedance between 100 and 400 Ω.

Differential outputs LS+,LS- are intended to directly drive a Loudspeaker. Preceding the outputs is a programmable attenuation amplifier, which must be set by writing to bits 0 to 3 in register CR6. Attenuations in the range 0 to -30 dB relative to the maximum level in 2.0 dB step can be programmed. The input of this programmable amplifier can be the summ of signals which can be selected by writing to register CR4:

- Receive speech signal which has been decoded and filtered,
- Internally generated tone signal, (Tone amplitude is programmed with bits 4 to 7 of register CR7),
- EAIN input which may be an alternate Ring signal or any voice frequency band limited signal. (An external decoupling capacitor of about 0.1µF is necessary).

Receive voice signal may be directed to output HFO by means of bit HFE in Register CR4. After processing, signal must be re-entered through input HFI to Loudspeaker amplifier input. (An external decoupling capacitor of about 0.1µF is necessary).
LS+ and LS- outputs are capable of driving output power level up to 80 mW into 50 Ω differentially connected load impedance at low distortion meeting PCM channel specifications. When the signal source is a Ring squarewave signal, power levels up to approximatively 200 mW can be delivered.

Anti-acoustic feed-back for loudspeaker to handset microphone loop with squelch effect: on chip switchable anti-larsen for loudspeaker to handset microphone feedback is implemented. A 12dB depth gain control on both transmit and receive path is provided to keep constant the loop gain. On the transmit path the 12dB gain control is provided starting from the CR5 transmit gain definition; at the same time, on the receive path the 12dB gain control is provided starting from CR6 receive gain definition.

Digital and Control Interface:
PIAFE provides a choice of either of two types of Digital Interface for both control data and PCM.
For compatibility with systems which use time slot oriented PCM busses with a separate Control Interface, as used on COMBO I/II families of devices, PIAFE functions are described in next section.
Alternatively, for systems in which PCM and control data are multiplexed together using GCI interface scheme, PIAFE functions are described in the section following the next one.
PIAFE will automatically switch to one of these two types of interface by sensing the MS pin.
Due to Line Transceiver clock recovery circuitry, a low jitter may be provided on F_S and MCLK clocks. F_S and MCLK must be always in phase. For ST5421S Transceiver, as an example, maximun value of jitter amplitude is a step of 65 ns at each GCI frame (125µs). So, the maximum jitter amplitude is 130 ns pk-pk.

COMBO I/II mode.
Digital Interface (Fig. 1)
F_S Frame Sync input determines the beginning of frame. It may have any duration from a single cycle of MCLK to a squarewave. Two different relationships may be established between the Frame Sync input and the first time slot of frame by setting bit 3 in register CR0. Non delayed data mode is similar to long frame timing on ETC5057/ TS5070 series of devices (COMBO I and COMBO II respectively): first time slot begins nominally coincident with the rising edge of F_S. Alternative is to use delayed data mode, which is similar to short frame sync timing on COMBO I or COMBO II, in which F_S input must be high at least a half cycle of MCLK earlier the frame beginning. A time slot assignment circuit on chip may be used with both timing modes, allowing connection to one of the two B1 and B2 voice data channels.
Two data formats are available: in Format 1, time slot B1 corresponds to the 8 MCLK cycles following immediately the rising edge of FS, while time slot B2 corresponds to the 8 MCLK cycles following immediately time slot B1.
In Format 2, time slot B1 is identical to Format 1. Time slot B2 appears two bit slots after time slot B1. This two bits space is left available for insertion of the D channel data.
Data format is selected by bit FF (2) in register CR0. Time slot B1 or B2 is selected by bit T0 (0) in Control Register CR1.
Bit EN (2) in control register CR1 enables or disables the voice data transfer on D_X and D_R as

Figure 1: Digital Interface Format

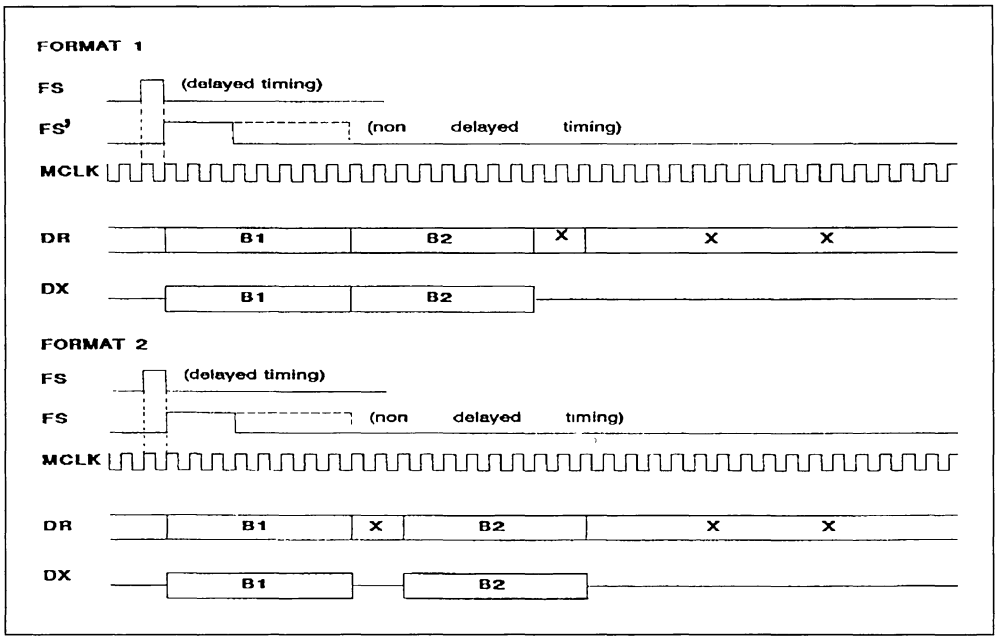
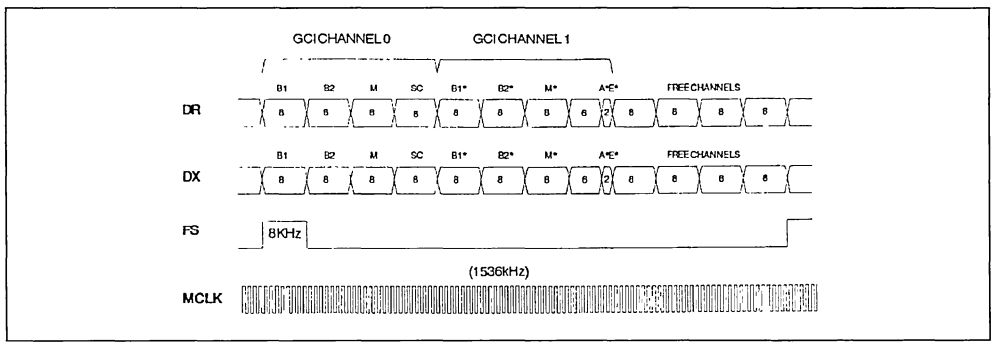


Figure 2: GCI Interface Frame Structure



appropriate. During the assigned time slot, D_X output shifts data out from the voice data register on the rising edges of MCLK. Serial voice data is shifted into D_R input during the same time slot on the falling edges of MCLK.
D_X is in the high impedance Tristate condition when in the non selected time slots.

Control Interface:
Control information or data is written into or read-back from PIAFE via the serial control port consisting of control clock CCLK, serial data input CI and output CO, and Chip Select input, CS-. All control instructions require 2 bytes as listed in Table 1, with the exception of a single byte power-up/down command.
To shift control data into ST5080A, CCLK must be pulsed high 8 times while CS- is low. Data on CI input is shifted into the serial input register on the rising edge of each CCLK pulse. After all data is shifted in, the content of the input shift register is decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide CS-pulse or may follow the first contiguously, i.e. it is not mandatory for CS- to return high in between

the first and second control bytes. At the end of the 2nd control byte, data is loaded into the appropriate programmable register. CS- must return high at the end of the 2nd byte.
To read-back status information from PIAFE, the first byte of the appropriate instruction is strobed in during the first CS- pulse, as defined in Table 1. CS- must be set low for a further 8 CCLK cycles, during which data is shifted out of the CO pin on the falling edges of CCLK.
When CS- is high, CO pin is in the high impedance Tri-state, enabling CO pins of several devices to be multiplexed together.
Thus, to summarise, 2 byte READ and WRITE instructions may use either two 8-bit wide CS- pulses or a single 16 bit wide CS- pulse.

Control channel access to PCM interface:
It is possible to access the B channel previously selected in Register CR1.
A byte written into Control Register CR3 will be automatically transmitted from D_X output in the following frame in place of the transmit PCM data.
A byte written into Control Register CR2 will be automatically sent through the receive path to the Receive amplifiers.
In order to implement a continuous data flow from the Control MICROWIRE interface to a B channel, it is necessary to send the control byte on each PCM frame.
A current byte received on D_R input can be read in the register CR2. In order to implement a continuous data flow from a B channel to MICROWIRE interface, it is necessary to read register CR2 at each PCM frame.

GCI COMPATIBLE MODE

GCI interface is an European standardized interface to connect ISDN dedicated components in the different configurations of equipment as Terminals, Network Terminations, PBX, etc...
In a Terminal equipment, this interface called SCIT for Special Circuit Interface for Terminals allows for example connection between:

- ST5421 (SID-GCI) and ST5451 (HDLC/GCI controller) used for 16 kbit/s D channel packet frames processing and SID control,
- Peripheral devices connected to a 64 kbit/s B channel and ST5451 used for GCI peripheral control.

ST5080A may be assigned to one of the B channels present on the GCI interface and is monitored via a control channel which is multiplexed with the 64 kbit/s Voice Data channels.

Figure 2 shows the frame structure at the GCI interface. Two 256 kbit/s channel are supported.

a)GCI channel 0: It is structured in four subchannels:
- B1 channel 8 bits per frame
- B2 channel 8 bits per frame
- M channel 8 bits per frame ignored by PIAFE
- SC channel 8 bits per frame ignored by PIAFE

Only B1 or B2 channel can be selected in PIAFE for PCM data transfer.

b)GCI channel 1: It is structured also in four subchannels:
- B1* channel 8 bits per frame
- B2* channel 8 bits per frame
- M* channel 8 bits per frame
- SC* which is structured as follows:

6 bits ignored by PIAFE
A* bit associated with M* channel
E* bit associated with M* channel.
B1* or B2* channel can be selected in PIAFE for PCM data transfer.
M* channel and two associated bits E* and A* are used for PIAFE control.

Thus, to summarize, B1, B2, B1* or B2* channel can be selected to transmit PCM data and M* channel is used to read/write status/command peripheral device registers. Protocol for byte exchange on the M* channel uses E* and A* bits.

Physical Interface

The interface is physically constitued with 4 wires:

Input Data wire:	D_R
Output Data wire:	D_X
Bit Clock:	MCLK
Frame Synchronization:	F_S

Data is synchronized by MCLK and F_S clock inputs.
F_S insures reinitialization of time slot counter at each frame beginning. The rising edge or FS is the reference time for the first GCI channel bit.
Data is transmitted in both directions at half the MCLK input frequency. Data is transmitted on the the rising edge of MCLK and is sampled one period after the transmit rising edge, also on a rising edge.
Note: Transmit data may be sampled by far-end device ie SID ST5421 on the falling edge 1.5 period after the transmit rising edge.
Unused channel are high impedance. Data outputs are OPEN-DRAIN and need an external pull up resistor.

COMBO activation/deactivation

ST5080A is automatically set in power down mode when GCI clocks are idle. GCI section is reactivated when GCI clocks are detected. PIAFE is completly reactivated after receiving of a power up command.

Exchange protocol on M* channel
Protocol allows a bidirectional transfer of bytes between ST5080A and GCI controller with acknowledgment at each received byte. For PIAFE, standard protocol is simplified to provide read or write register cycles almost identical to MICROWIRE serial interface.

Write cycle
Control Unit sends through the GCI controller following bytes:

- First byte is the chip select byte. The first four bits indicate the device address: (A3,A2,A1,A0). The four last bits are ignored. ST5080A compare the validated byte received internally with the address defined by pins A3, A2, A1, A0. If comparison is true, byte is acknowledged, if not, ST5080A does not acknowledge the byte.

NOTE: An internal "message in progress" flag remains active till the end of the complete message transmission to avoid irrelevant acknowledgement of any further byte.

- Second byte is structured as defined in Table 1.
- Third byte is the Data byte to write into the Register as indicated in Table 1.

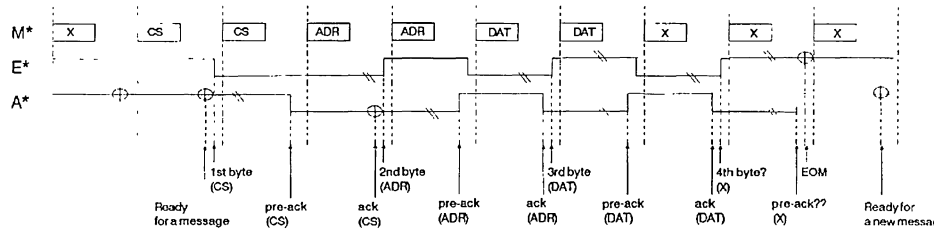
It is possible but optional to write to several different registers in a single message. In this case the Chip Select byte is sent only once at the beginning of the message, the device automatically toggles between address byte and data byte.

Read cycle
Control Unit sends two bytes. First byte is the chip select byte as defined above. Second byte is structured as defined in Table 1.
If PIAFE identifies a read-back cycle, bit 2 of byte 1 in Table 1 equal 1, it has to respond to the Control Unit by sending a single byte message which is the content of the addressed register.
It is possible but optional to request several different read-back register cycles in a single message but it is recommended to wait the answer before requesting a new read back to avoid loss of data. ST5080A responds by sending a single data byte message at each request.

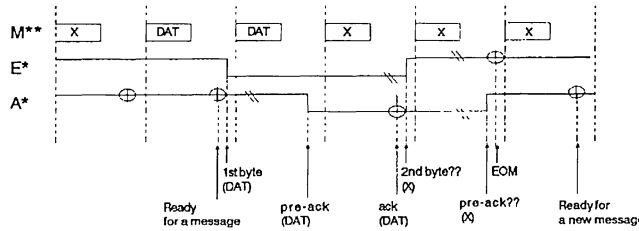
Received byte validation:
A received byte is validated if it is detected two consecutive times identical.

Exchange Protocol:
Exchange protocol is identical for both directions. Sender uses E* bit to indicate that it is sending a M* byte while receiver uses A* bit to acknowledge received byte.
When no message is transferred, E* bit and A* bit are forced to inactive state.
A transmission is initialized by sender putting E* bit from inactive state to active state and by sending first byte on M* channel in the same frame.
Transmission of a message is allowed only if A* bit from the receiver has been set inactive for at least two frames.
When receiver is ready, it validates the received byte internally when received in two consecutive frames identical. Then the receiver sets first A* bit from inactive to active state (pre-acknowlegement), and maintains A* bit active at least in the following frame (acknowledgement). If validation is not possible, (two last bytes received are not identical), receiver aborts the message setting A* bit active for only a single frame.
For the first byte received, Abort sequence is not allowed. PIAFE does not respond either if two last bytes are not identical or if the byte received does not meet the Chip Select byte defined by A0-A3 pins bias.
A second byte may be transmitted by the sender putting E* bit from active to inactive state and sending the second byte on the M* channel in the same frame. E* bit is set inactive for only one frame. If it remains inactive more than one frame, it is an end of message (i.e. not second byte available).
The second byte may be transmitted only after receiving the pre-acknowledgment of the previous byte transmitted (see Fig. 3). The same protocol is used if a third byte is transmitted. Each byte has to be transmitted at least in two consecutive frames.
The receiver validates current received byte as done on first byte and then set A* bit in the next two frames first from active to inactive state (pre-acknowledgement), and after from inactive to active state (acknowledgement). If the receiver cannot validate the received current byte (two bytes received are not identical), it pre-acknowledges normally, but let A* bit in the inactive state in the next frame which indicates an abort request.
If a message sent by ST5080A is aborted, it will stop the message and wait for a new read cycle instruction from the controller.
A message received by ST5080A is acknowledged or aborted without flow Control.
Figures 3 gives timing of a write cycle. Most significant bit (MSB) of a Monitor byte is sent first on M* channel.
E* and A* bits are active low and inactive state on DOUT is high impedance.

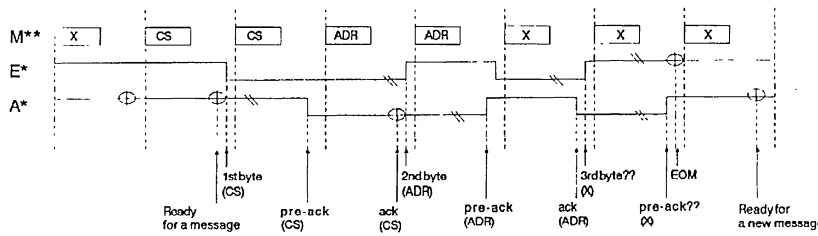
Figure 3: E and A bits Timing



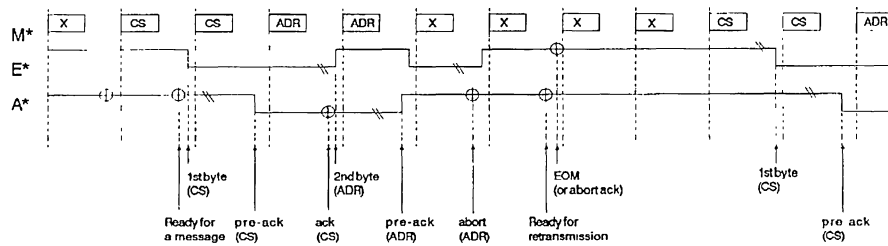
THREE BYTES MESSAGE - NORMAL TRANSMISSION



ONE BYTE MESSAGE - NORMAL TRANSMISSION



TWO BYTES MESSAGE - NORMAL TRANSMISSION



TWO BYTES MESSAGE ABORTED ON THE SECOND AND RETRANSMITTED

PROGRAMMABLE FUNCTIONS

For both formats of Digital Interface, programmable functions are configured by writing to a number of registers using a 2-byte write cycle (not including chip select byte in GCI).

Most of these registers can also be read-back for verification. Byte one is always register address, while byte two is Data.

Table 1 lists the register set and their respective adresses.

Table 1: Programmable Register Intructions

Function	Address byte								Data byte
	7	6	5	4	3	2	1	0	
Single byte Power up/down	P	X	X	X	X	X	0	X	none
Write CR0	P	0	0	0	0	0	1	X	see CR0 TABLE 2
Read-back CR0	P	0	0	0	0	1	1	X	see CR0
Write CR1	P	0	0	0	1	0	1	X	see CR1 TABLE 3
Read-back CR1	P	0	0	0	1	1	1	X	see CR1
Write Data to receive path	P	0	0	1	0	0	1	X	see CR2 TABLE 4
Read data from D_R	P	0	0	1	0	1	1	X	see CR2
Write Data to D_X	P	0	0	1	1	0	1	X	see CR3 TABLE 5
Write CR4	P	0	1	0	0	0	1	X	see CR4 TABLE 6
Read-back CR4	P	0	1	0	0	1	1	X	see CR4
Write CR5	P	0	1	0	1	0	1	X	see CR5 TABLE 7
Read-back CR5	P	0	1	0	1	1	1	X	see CR5
Write CR6	P	0	1	1	0	0	1	X	see CR6 TABLE 8
Read-back CR6	P	0	1	1	0	1	1	X	see CR6
Write CR7	P	0	1	1	1	0	1	X	see CR7 TABLE 9
Read-back CR7	P	0	1	1	1	1	1	X	see CR7
Write CR8	P	1	0	0	0	0	1	X	see CR8 TABLE 10
Read-back CR8	P	1	0	0	0	1	1	X	see CR8
Write CR9	P	1	0	0	1	0	1	X	see CR9 TABLE 11
Read-back CR9	P	1	0	0	1	1	1	X	see CR9
Write Test Register CR10	P	1	0	1	0	0	1	X	reserved

NOTE 1. bit 7 of the address byte and data byte is always the first bit clocked into or out from CI and CO pins when MICROWIRE serial port is enabled, or into and out from D_R and D_X pins when GCI mode selected.
X = reserved: write 0

NOTE 2. "P" bit is Power up/down Control bit P = 1 Means Power Down
Bit 1 indicates, if set, the presence of a second byte.

NOTE 3. Bit 2 is write/read select bit.

Table 2: Control Register CR0 Functions

7	6	5	4	3	2	1	0	Function		
F1	F0	MA	IA	DN	FF	B7	DL			
0	0							MCLK = 512 kHz		(1)
0	1							MCLK = 1.536 MHz	*	
1	0							MCLK = 2.048 MHz		
1	1							MCLK = 2.560 MHz		(1)
		0	X					Select MU-255 law	*	
		1	0					A-law including even bit inversion		
		1	1					A-law; No bit inversion		
				0				Delayed data timing	*	(1)
				1				Non delayed data timing		(1)
					0			B1 and B2 consecutive	*	(1)
					1			B1 and B2 separated		(1)
						0		8 bits time-slot	*	
						1		7 bits time-slot		
							0	Normal operation	*	
							1	Digital Loop-back		

* state at power on initialization

(1): significant in COMBO I/II mode only

Table 3: Control Register CR1 Functions

7	6	5	4	3	2	1	0	Function		
HFE	ALE	DO	MR	MX	EN	T1	T0			
0								HFO / HFI pins disabled	*	
1								HFO / HFi pins enabled		
	0							Anti-larsen disabled	*	
	1							Anti-larsen enabled		
		0						L0 latch is put in high impedance	*	
		1						L0 latch set to 0		
			0					D_R connected to rec. path	*	(1)
			1					CR2 connected to rec. path		(1)
				0				Trans path connected to D_X	*	(1)
				1				CR3 connected to D_X		(1)
					0			voice data transfer disable	*	
					1			voice data transfer enable		
						0	0	B1 channel selected	*	
						0	1	B2 channel selected		
						1	0	B1* channel selected		(2)
						1	1	B2* channel selected		(2)

* state at power on initialization

(1): significant in COMBO I / II mode only

(2): significant in GCI mode only

Table 4: Control Register CR2 Functions

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb							lsb	Data sent to Receive path or Data received from D_R input

Table 5: Control Registers CR3 Functions

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb							lsb	D_X data transmitted

Table 6: Control Register CR4 Functions

7	6	5	4	3	2	1	0	Function	
VS	TE	SI	EE	RTL	RTE	SL	SE		
0 1								MIC1 selected MIC2 selected	*
	0 1							Transmit input muted Transmit input enabled	*
		0 1						Internal sidetone disabled Internal sidetone enabled	*
			0 1					EAIN disconnected EAIN selected to Loudspeaker	*
				0 0 1 1	0 1 0 1			Ring / Tone muted Ring / Tone to Earpiece Ring / Tone to Loudspeaker Ring / Tone to Earpiece and Loudspeaker	*
						0 0 1 1	0 1 0 1	Receive signal muted Receive signal connected to earpiece amplifer Receive signal connected to loudspeaker amplifier Receive signal connected to loudspeaker and earpiece amplifier	*

* state at power on initialization

Table 7: Control Register CR5 Functions

7	6	5	4	3	2	1	0	Function
Transmit amplifier				Sidetone amplifier				
0	0	0	0					0 dB gain *
0	0	0	1					1 dB gain
-	-	-	-					in 1 dB step
1	1	1	1					15 dB gain
				0	0	0	0	-12.5 dB gain *
				0	0	0	1	-13.5 dB gain
				-	-	-	-	in 1 dB step
				1	1	1	1	-27.5 dB gain

* state at power on initialization

Table 8: Control Register CR6 Functions

7	6	5	4	3	2	1	0	Function
Earpiece ampifier				Loudspeaker				
0	0	0	0					0 dB gain *
0	0	0	1					-1 dB gain
-	-	-	-					in 1 dB step
1	1	1	1					-15 dB gain
				0	0	0	0	0 dB gain *
				0	0	0	1	-2 dB gain
				-	-	-	-	in 2 dB step
				1	1	1	1	-30 dB gain

* state at power on initialization

Table 9: Control Register CR7 Functions

7	6	5	4	3	2	1	0	Function		
Tone gain				F1	F2	SN	DE	Attenuation	f1 V_{pp}	f2 V_{pp}
0	0	0	0					0 dB *	2.4 (1)	1 9 (1)
0	0	0	1					-3 dB	1.70	1.34
0	0	1	0					-6 dB	1.20	0.95
0	0	1	1					- 9 dB	0.85	0.67
0	1	0	0					-12 dB	0.60	0.47
0	1	0	1					-15 dB	0.43	0.34
0	1	1	0					-18 dB	0.30	0.24
0	1	1	1					-21 dB	0.21	0.17
1	X	X	0					-24 dB	0.15	0.12
1	X	X	1					-27 dB	0.10	0.08
				0	0			f1 and f2 muted		*
				0	1			f2 selected		
				1	0			f1 selected		
				1	1			f1 and f2 in summed mode		
						0		Squarewave signal selected		*
						1		Sinewave signal selected		
							0	Normal operation		*
							1	Tone / Ring Generator connected to Transmit path		

* state at power on initialization

(1) value provided if f1 or f2 is selected alone
if f1 and f2 are selected in the summed mode, f1=1 34 V_{pp} while f2=1 06 V_{pp}
Output generator is 2 4 V_{pp}

X reserved write 0

Table 10: Control Register CR8 Functions

7	6	5	4	3	2	1	0	Function
f17	f16	f15	f14	f13	f12	f11	f10	
msb							lsb	Binary equivalent of the decimal number used to calculate f1

Table 11: Control Register CR9 Functions

7	6	5	4	3	2	1	0	Function
f27	f26	f25	f24	f23	f22	f21	f20	
msb							lsb	Binary equivalent of the decimal number used to calculate f2

CONTROL REGISTER CR0
First byte of a READ or a WRITE instruction to Control Register CR0 is as shown in TABLE 1. Second byte is as shown in TABLE 2.

Master Clock Frequency Selection
A master clock must be provided to PIAFE for operation of filter and coding/decoding functions.
In COMBO I/II mode, MCLK frequency can be either 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz.
Bit F1 (7) and F0 (6) must be set during initialization to select the correct internal divider.
In GCI mode, MCLK must be either 1.536MHz or 2.048MHz.
512KHz and 2.56MHz are not allowed.
Default value is 1.536 MHz for both modes.
Any clock different from the default one must be selected prior a Power-Up instruction for both modes.

Coding Law Selection
Bits MA (5) and IA (4) permit selection of Mu-255 law or A law coding with or without even bit inversion.
After power on initialization, the Mu-255 law is selected.

	Mu 255 law								True A law even bit inversion								A law without even bit inversion							
	msb							lsb	msb							lsb	msb							lsb
Vin = + full scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1
Vin = 0 V	1 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 0	1 1	0 0	1 1	0 0	1 1	0 0	1 1	1 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
Vin = - full scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1	1

MSB is always the first PCM bit shifted in or out of PIAFE.

Digital Interface timing
Bit DN=0 (3) selects digital interface in delayed timing mode while DN=1 selects non delayed data timing.
In GCI mode, bit DN is not significant.
After reset and if COMBO I/II mode is selected, delayed data timing is selected.

Digital Interface format
Bit FF=0 (2) selects digital interface in Format 1 where B1 and B2 channel are consecutive. FF=1 selects Format 2 where B1 and B2 channel are separated by two bits. (see digital interface format section).
In GCI mode, bit FF is not significant.

56+8 selection
Bit 'B7' (1) selects capability for PIAFE to take into account only the seven most significant bits of the PCM data byte selected.
When 'B7' is set, the LSB bit on D_R is ignored and LSB bit on D_X is high impedance. This function allows connection of an external "in band" data generator directly connected on the Digital Interface.

Digital loopback
Digital loopback mode is entered by setting DL bit(0) equal 1.
In Digital Loopback mode, data written into Receive PCM Data Register from the selected received time-slot is read-back from that Register in the selected transmit time-slot on D_X. Time slot is selected with Register CR1.
No PCM decoding or encoding takes place in this mode. Transmit and Receive amplifier stages are muted.

CONTROL REGISTER CR1
First byte of a READ or a WRITE instruction to Control Register CR1 is as shown in TABLE 1. Second byte is as shown in TABLE 3.

Hands-free I/Os selection
Bit HFE set to one enables HFI, HFO pins for connection of an external handfree circuit such as TEA 7540. HFO is an analog output that provides the receive voice signal. 0 dBMO level on that output is 0.491 Vrms ($1.4V_{pp}$). HFI is an analog high impedance input (10 KΩ typ.) intended to send back the processed receive signal to the Loudspeaker. 0 dBMO level on that input is 0.491Vrms.

Anti-larsen selection
Bit ALE set to one enables on-chip antilarsen and squelch effect system.

Latch output control
Bit DO controls directly logical status of latch output LO: ie, a "ZERO" written in bit DO puts output LO in high impedance, a "ONE" written in bit DO sets output LO to zero.

Microwire access to B channel on receive path
Bit MR (4) selects access from MICROWIRE Register CR2 to Receive path. When bit MR is set high, data written to register CR2 is decoded each frame, sent to the receive path and data input at D_R is ignored.
In the other direction, current PCM data input received at D_R can be read from register CR2 each frame.

Microwire access to B channel on transmit path
Bit MX (3) selects access from MICROWIRE write only Register CR3 to D_X output. When bit MX is set high, data written to CR3 is output at D_X every frame and the output of PCM encoder is ignored.

B channel selection
Bit 'EN' (2) enables or disables voice data transfer on D_X and D_R pins. When disabled, PCM data from DR is not decoded and PCM time-slots are high impedance on D_X.
In GCI mode, bits 'T1' (1) and 'T0' (0) select one of the four channels of the GCI interface.
In COMBO I/II mode, only B1 or B2 channel can be selected according to the interface format selected. Bit 'T1' is ignored.

CONTROL REGISTER CR2
Data sent to receive path or data received from D_R input. Refer to bit MR(4) in "Control Register CR1" paragraph.

CONTROL REGISTER CR3
D_X data transmitted. Refer to bit MX(3) in "Control Rgister CR1" paragraph.

CONTROL REGISTER CR4
First byte of a READ or a WRITE instruction to Control Register CR4 is as shown in TABLE 1. Second byte is as shown in TABLE 6.

Transmit Input Selection
MIC1 or MIC2 source is selected with bit VS (7).
Transmit input selected can be enabled or muted with bit TE (6).
Transmit gain can be adjusted within a 15 dB range in 1 dB step with Register CR5.

Sidetone select
Bit "SI" (5) enables or disables Sidetone circuitry. When enabled, sidetone gain can be adjusted with Register (CR5). When Transmit path is disabled, bit TE set low, sidetone circuit is also disabled.

External Auxiliary signal select
Bit "EE" (4) set to one connects EAIN input to the loudspeaker amplifier input.

Ring/Tone signal routing
Bits "RTL" (3) and RTE (2) provide select capability to connect on-chip Ring/Tone generator either to loudspeaker amplifier input or to earpiece amplifier input or both.

PCM receive data routing
Bits "SL" (1) and "SE" (0) provide select capability to connect received speech signal either to Loudspeaker amplifier input or to earpiece amplifier input or both.

CONTROL REGISTER CR5
First byte of a READ or a WRITE instuction to Control Register CR5 is as shown in TABLE 1. Second byte is as shown in TABLE 7.

Transmit gain selection
Transmit amplifier can be programmed for a gain from 0dB to 15dB in 1dB step with bits 4 to 7.
0 dBmO level at the output of the transmit amplifier (A reference point) is 0.739 Vrms (overload voltage is 1.06 Vrms).

Sidetone attenuation selection
Transmit signal picked up after the switched capacitor low pass filter may be fed back into the Receive Earpiece amplifier.
Attenuation of the signal at the output of the sidetone attenuator can be programmed from –12.5dB to -27.5dB relative to reference point A in 1 dB step with bits 0 to 3.

CONTROL REGISTER CR6
First byte of a READ or a WRITE instruction to Control Register CR6 is as shown in TABLE 1. Second byte is as shown in TABLE 8.

Earpiece amplifier gain selection:
Earpiece Receive gain can be programmed in 1 dB step from 0 dB to -15 dB relative to the maximum with bits 4 to 7.
0 dBmO voltage at the output of the amplifier on pins V_{Fr+} and V_{Fr-} is then 824.5 mVrms when 0dB gain is selected down to 146.6 mVrms when –15 dB gain is selected.

Loudspeaker amplifier gain selection:
Loudspeaker Receive amplifier gain can be programmed in 2 dB step from 0 dB to -30 dB relative to the maximum with bits 0 to 3.
0 dBmO voltage on the output of the amplifier on pins LS+ and LS- on 50 Ω is then 1.384 Vrms ($3.91V_{pp}$) when 0 dB gain is selected down to 43.7 mVrms ($123.6mV_{pp}$) when -30 dB gain is selected.

Current limitation is approximatively 150 mApk.

CONTROL REGISTER CR7:
First byte of a READ or a WRITE instruction to Control Register CR7 is as shown in TABLE 1. Second byte is as shown in TABLE 9.

Tone/Ring amplifier gain selection
Output level of Ring/Tone generator, before attenuation by programmable attenuator is 2.4 Vpk-pk when f1 generator is selected alone or summed with the f2 generator and 1.9 Vpk-pk when f2 generator is selected alone.
Selected output level can be attenuated down to -27 dB by programmable attenutator by setting bits 4 to 7.

Frequency mode selection
Bits 'F1' (3) and 'F2' (2) permit selection of f1 and/or f2 frequency generator according to TABLE 9.
When f1 (or f2) is selected, output of the Ring/Tone is a squarewave (or a sinewave) signal at the frequency selected in the CR8 (or CR9) Register.
When f1 and f2 are selected in summed mode, output of the Ring/Tone generator is a signal where f1 and f2 frequency are summed.
In order to meet DTMF specifications, f2 output level is attenuated by 2dB relative to the f1 output level.
Frequency temporization must be controlled by the microcontroller.

Waveform selection
Bit 'SN' (1) selects waveform of the output of the Ring/Tone generator. Sinewave or squarewave signal can be selected.

DTMF selection
Bit DE (0) permits connection of Ring/Tone/DTMF generator on the Transmit Data path instead of the Transmit Amplifier output. Earpiece feed-back may be provided by sidetone circuitry by setting bit SI or directly by setting bit RTE in Register CR4. Loudspeaker feed-back may be provided directly by setting bit RTL in Register CR4.

CONTROL REGISTERS CR8 AND CR9
First byte of a READ or a WRITE instruction to Control Register CR8 or CR9 is as shown in TABLE 1. Second byte is respectively as shown in TABLE 10 and 11.
Tone or Ring signal frequency value is defined by the formula:

f1 = CR8 / 0.128 Hz

and

f2 = CR9 / 0.128 Hz

where CR8 and CR9 are decimal equivalents of the binary values of the CR8 and CR9 registers respectively. Thus, any frequency between 7.8 Hz and 1992 Hz may be selected in 7.8 Hz step.
TABLE 12 gives examples for the main frequencies usual for Tone or Ring generation.

Table 12: Examples of Usual Frequency Selection

Description	f1 value (decimal)	Theoric value (Hz)	Typical value (Hz)	Error %
Tone 250 Hz	32	250	250	.00
Tone 330 Hz	42	330	328.2	–.56
Tone 425 Hz	54	425	421.9	–.73
Tone 440 Hz	56	440	437.5	–.56
Tone 800 Hz	102	800	796.9	–.39
Tone 1330 Hz	170	1330	1328.1	–.14
DTMF 697 Hz	89	697	695.3	–.24
DTMF 770 Hz	99	770	773.4	+.44
DTMF 852 Hz	109	852	851.6	–.05
DTMF 941 Hz	120	941	937.5	–.37
DTMF 1209 Hz	155	1209	1210.9	+.16
DTMF 1336 Hz	171	1336	1335.9	–.01
DTMF 1477 Hz	189	1477	1476.6	.00
DTMF 1633 Hz	209	1633	1632.8	.00
SOL	50	392	390.6	–.30
LA	56	440	437.5	–.56
SI	63	494	492.2	–.34
DO	67	523.25	523.5	+.04
RE	75	587.33	586.0	–.23
MI flat	80	622.25	625.0	+.45
MI	84	659.25	656.3	–.45
FA	89	698.5	695.3	–.45
FA sharp	95	740	742.2	+.30
SOL	100	784	781.3	–.34
SOL sharp	106	830.6	828.2	–.29
LA	113	880	882.9	+.33
SI	126	987.8	984.4	–.34
DO	134	1046.5	1046.9	+.04
RE	150	1174.66	1171.9	–.23
MI	169	1318.5	1320.4	+.14

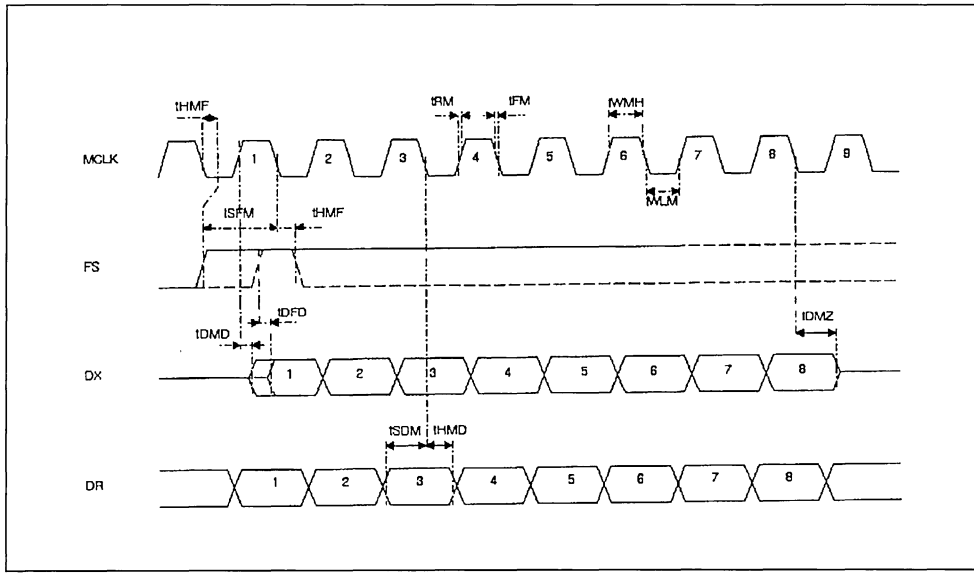
POWER SUPPLIES

While pins of PIAFE device are well protected against electrical misuse, it is recommended that the standard CMOS practise of applying GND before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

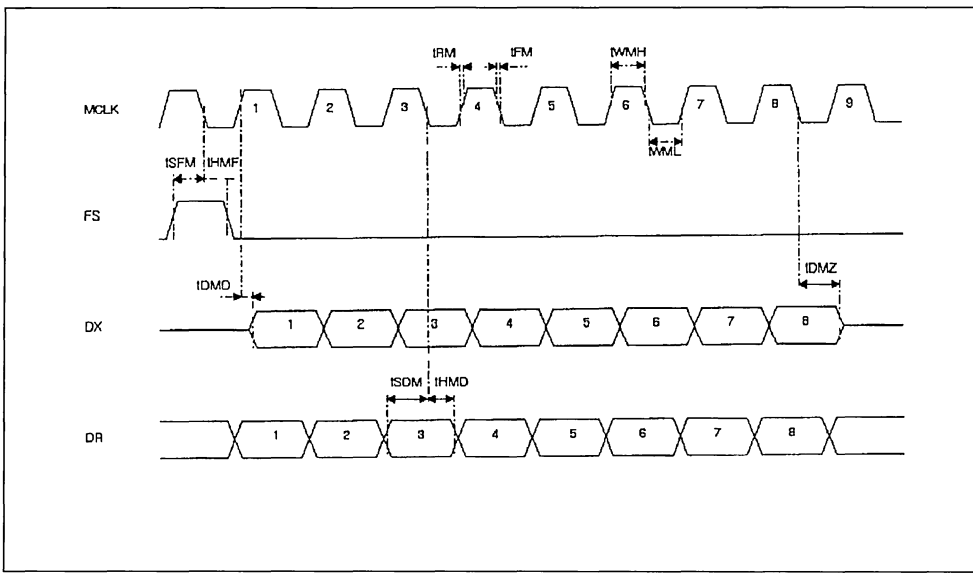
To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A power supply decoupling capacitor of 0.1 µF should be connected from this common point to V_{CC} as close as possible to the device pins.

TIMING DIAGRAM

Non Delayed Data Timing Mode

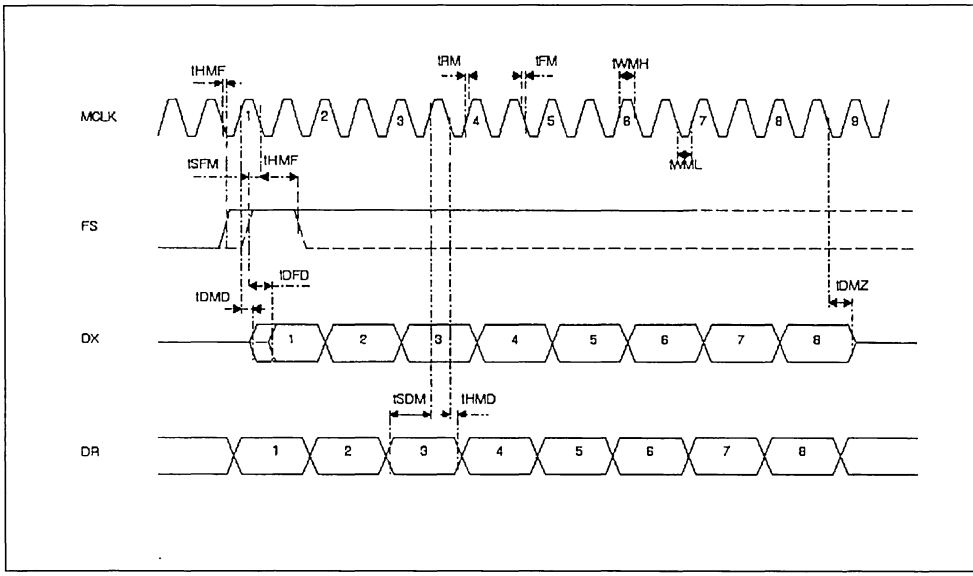


Delayed Data Timing Mode

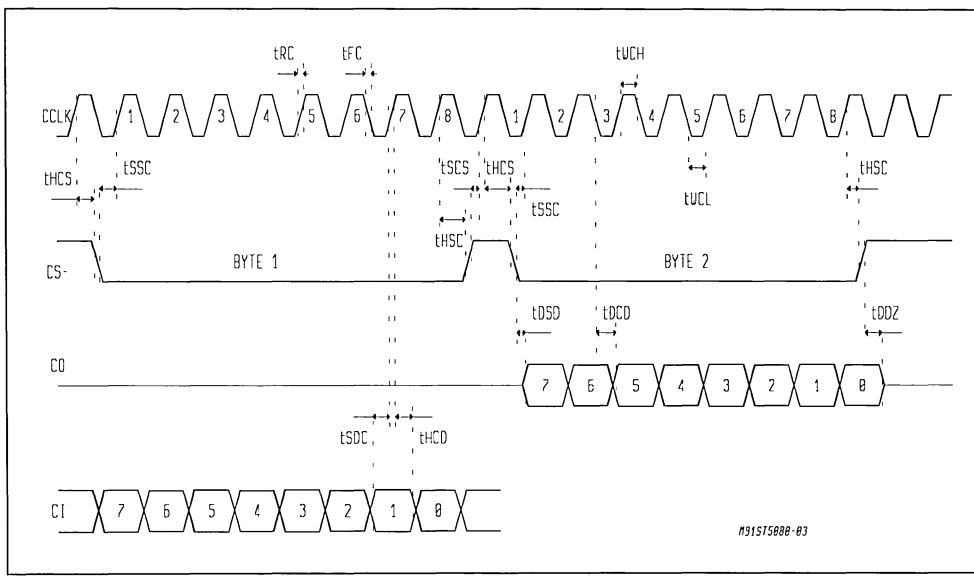


TIMING DIAGRAM (continued)

GCI Timing Mode



Serial Control Timing (MICROWIRE MODE)



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
V_{CC} to GND	7	V
Current at V_{MIC} ($V_{CC} \leq 5.5V$)	±50	mA
Current at V_{RxO} and LS	± 100	mA
Current at any digital output	± 50	mA
Voltage at any digital input ($V_{CC} \leq 5.5V$); limited at ± 50mA	V_{CC} + 1 to GND - 1	V
Storage temperature range	- 65 to + 150	°C
Lead Temperature (wave soldering, 10s)	+ 260	°C

TIMING SPECIFICATIONS (unless otherwise specified, V_{CC} = 5V ± 10%, T_A = –25°C to 85°C ; typical characteristics are specified V_{CC} = 5V, T_A = 25 °C; all signals are referenced to GND, see Note 5 for timing definitions)

MASTER CLOCK TIMING

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{MCLK}	Frequency of MCLK	Selection of frequency is programmable (see table 2)		512 1.536 2.048 2.560		kHz MHz MHz MHz
t_{WMH}	Period of MCLK high	Measured from V_{IH} to V_{IH}	80			ns
t_{WML}	Period of MCLK low	Measured from V_{IL} to V_{IL}	80			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			30	ns

PCM INTERFACE TIMING (COMBO I / II and GCI modes)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{HMF}	Hold Time MCLK low to FS low		10			ns
t_{SFM}	Setup Time, FS high to MCLK low		30			ns
t_{DMD}	Delay Time, MCLK high to data valid	Load = 100 pf			100	ns
t_{DMZ}	Delay Time, MCLK low to DX disabled		15		100	ns
t_{DFD}	Delay Time, FS high to data valid	Load = 100 pf ; Applies only if FS rises later than MCLK rising edge in Non Delayed Mode only			100	ns
t_{SDM}	Setup Time, D_R valid to MCLK receive edge		20			ns
t_{HMD}	Hold Time, MCLK low to D_R invalid		20			ns

SERIAL CONTROL PORT TIMING (Usual COMBO I / II mode only)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{CCLK}	Frequency of CCLK				2.048	MHz
t_{WCH}	Period of CCLK high	Measured from V_{IH} to V_{IH}	160			ns
t_{WCL}	Period of CCLK low	Measured from V_{IL} to V_{IL}	160			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			50	ns
t_{HCS}	Hold Time, CCLK high to CS– low		10			ns
t_{SSC}	Setup Time, CS– low to CCLK high		50			ns
t_{SDC}	Setup Time, CI valid to CCLK high		50			ns
t_{HCD}	Hold Time, CCLK high to CI invalid		50			ns
t_{DCD}	Delay Time, CCLK low to CO data valid	Load = 100 pF , plus 1 LSTTL load			80	ns
t_{DSD}	Delay Time, CS–low to CO data valid				50	ns
t_{DDZ}	Delay Time CS–high or 8th CCLK low to CO high impedance whichever comes first		15		80	ns
t_{HSC}	Hold Time, 8th CCLK high to CS– high		100			ns
t_{SCS}	Set up Time, CS– high to CCLK high		100			ns

Note 5 A signal is valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH}
For the purpoes of this specification the following conditions apply
a) All input signal are defined as V_{IL} = 0.4V, V_{IH} = 2.7V, t_R < 10ns, t_F < 10ns
b) Delay times are measured from the inputs signal valid to the output signal valid.
c) Setup times are measured from the data input valid to the clock input invalid.
d) Hold times are measured from the clock signal valid to the data input invalid.

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CC} = 5V ± 10%, T_A = –25°C to 85°C ; typical characteristic are specified at V_{CC} = 5V, T_A = 25°C ; all signals are referenced to GND)

DIGITAL INTERFACES

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All digital inputs	DC			0.7	V
			AC			0.4	V
V_{IH}	Input High Voltage	All digital inputs	DC	2.0			V
			AC	2.7			V
V_{OL}	Output Low Voltage	D_X,I_L = -2.0mA;	DC			0.4	V
		all other digital outputs, I_L = –1mA	AC			0.7	V
V_{OH}	Output High Voltage	D_X,I_L = 2.0mA;	DC	2.4			V
		all other digital outputs, I_L = 1mA	AC	2.0			V
I_{IL}	Input Low Current	Any digital input, GND < V_{IN} < V_{IL}		-10		10	µA
I_{IH}	Input High Current	Any digital input, V_{IH} < V_{IN} < V_{CC}		-10		10	µA
I_{OZ}	Output Current in High impedance (Tri-state)	D_X and CO		-10		10	µA

ANALOG INTERFACES

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{MIC}	Input Leakage	GND < V_{MIC} < V_{CC}	-100		+100	µA
R_{MIC}	Input Resistance	GND < V_{MIC} < V_{CC}	50			kΩ
R_{LVFr}	Load Resistance	V_{Fr+} to V_{Fr-}	100			Ω
C_{LVFr}	Load Capacitance	V_{Fr+} to V_{Fr-}			150	nF
R_{OVFr0}	Output Resistance	Steady zero PCM code applied to DR; I = ± 1mA		1.0		Ω
V_{OSVFr0}	Differential offset: Voltage at V_{Fr+}, V_{Fr-}	Alternating ± zero PCM code applied to DR maximum receive gain; R_L = 100Ω	-100		+100	mV
R_{LLS}	Load Resistance	L_{S+} to L_{S-}		50		Ω
C_{LLS}	Load Capacitance	L_{S+} to L_{S-}			600	nF
R_{OLS}	Output Resistance	Steady zero PCM code applied to DR; I ± 1mA		1		Ω
V_{OSLS}	Differential offset Voltage at L_{S+}, L_{S-}	Alternating ± zero PCM code applied to DR maximum receive gain; R_L = 50Ω	–100		+100	mV

POWER DISSIPATION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC0}	Power down Current	CCLK,CI = 0.4V; CS = 2.4V (µwire only) All other inputs active GCI mode only:		0.2 0.2	0.5 0.5	mA mA
I_{CC1}	Power Up Current	L_{S+}, L_{S-} and V_{Fr+}, V_{Fr-} not loaded		12.0	17.0	mA

TRANSMISSION CHARACTERISTICS (unless otherwise specified, V_{CC} = 5V ± 10%, T_A = –25°C to 85°C; typical characteristics are specified at V_{CC} = 5V, T_A = 25°C, MIC1/2 = 0dB_{m0}, D_R = 0dB_{m0} PCM code, f = 1015.625 Hz; all signal are referenced to GND)

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Transmit path - Absolute levels at MIC1 / MIC2

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Transmit Amps connected for 0dB gain		73.9		mV_{RMS}
Overload level	A law selected		106.08		mV_{RMS}
Overload level	mu law selected		106.47		mV_{RMS}
0 dBM0 level	Transmit Amps connected for 15dB gain		13.14		mV_{RMS}
Overload level	A law selected		18.86		mV_{RMS}
Overload level	mu law selected		18.93		mV_{RMS}

TRANSMISSION CHARACTERISTICS (continued)

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Receive path - Absolute levels at V_{FR} (Differentially measured)

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Receive Amp programmed for 0dB gain		824.5		mV_{RMS}
0 dBM0 level	Receive Amp programmed for - 15dB attenuation		146.6		mV_{RMS}

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Receive path - Absolute levels at L_S (Differentially measured)

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Receive Amp programmed for 0dB gain		1.384		V_{RMS}
0 dBM0 level	Receive Amp programmed for - 30dB gain		43.7		mV_{RMS}

AMPLITUDE RESPONSE
Transmit path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for maximum. Measure deviation of Digital PCM Code from ideal $0dB_{m0}$ PCM code at D_X	-0.30		0.30	dB
G_{XAG}	Transmit Gain Variation with programmed gain	Measure Transmit Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GXA, i.e. $G_{AXG} = G_{actual} - G_{prog} - G_{XA}$	-0.5		0.5	dB
G_{XAT}	Transmit Gain Variation with temperature	Measured relative to G_{XA}. min. gain < G_X < Max. gain	-0.1		0.1	dB
G_{XAV}	Transmit Gain Variation with supply	Measured relative to G_{XA} G_X = Maximum gain	-0.1		0.1	dB
G_{XAF}	Transmit Gain Variation with frequency	Relative to 1015,625 Hz, multitone test technique used. min. gain < G_X < Max. gain				
		f = 60 Hz			-26	dB
		f = 200 Hz	-1.5		-0.1	dB
		f = 300 Hz to 3000 Hz	-0.3		0.3	dB
		f = 3400 Hz	-0.8		0.0	dB
		f = 4000 Hz			-14	dB
		f = 4600 Hz (*)			-35	dB
		f = 5000 Hz to 6000 Hz			-40	dB
		f = 8000 Hz (*)			-47	dB
		f > 8000 Hz			-40	dB
G_{XAL}	Transmit Gain Variation with signal level	Sinusoidal Test method. Reference Level = $-10\ dB_{m0}$				
		V_{MIC} = $-40\ dB_{m0}$ to $+3\ dB_{m0}$	-0.25		0.25	dB
		V_{MIC} = $-50\ dB_{m0}$ to $-40\ dB_{m0}$	-0.5		0.5	dB
		V_{MIC} = $-55\ dB_{m0}$ to $-50\ dB_{m0}$	-1.2		1.2	dB

(*) The limit at frequencies between 4600Hz and 8000Hz lies on a stright line connecting the two frequencies on a linear (dB) scale versus log (Hz) scale

AMPLITUDE RESPONSE

Receive path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{RAE}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply 0 dB_{m0} PCM code to D_R Measure $V_{Fr\pm}$	-0.3		0.3	dB
G_{RAL}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply 0 dB_{m0} PCM code to D_R Measure $L_{S\pm}$	-0.6		0.6	dB
G_{RAGE}	Receive Gain Variation with programmed gain	Measure Earpiece Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GRAE, i.e. $G_{RAGE} = G_{actual} - G_{prog} - G_{RAE}$	-0.5		0.5	dB
G_{RAGL}	Receive Gain Variation with programmed gain	Measure Loudspeaker Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GRAL, i.e. $G_{RAGL} = G_{actual} - G_{prog} - G_{RAL}$	-1.0		1.0	dB
G_{RAT}	Receive Gain Variation with temperature	Measured relative to GRA. (LS and V_{Fr}) G_R = Maximum Gain	-0.1		0.1	dB
G_{RAV}	Receive Gain Variation with Supply	Measured relative to GRA. (LS and V_{Fr}) G_R = Maximum Gain	-0.1		0.1	dB
G_{RAF}	Receive Gain Variation with frequency (Earpiece or Loudspeaker)	Relative to 1015,625 Hz, multitone test technique used. min. gain < G_R < Max. gain f = 200 Hz f = 300 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz	 -0.3 -0.3 -0.8		 0.3 0.3 0.0 -14	 dB dB dB dB
$G_{RAL\,E}$	Receive Gain Variation with signal level (Earpiece)	Sinusoidal Test Method Reference Level = –10 dBm0 D_R = 0 dBm0 to +3 dBm0 D_R = -40 dBm0 to 0 dBm0 D_R = -50 dBm0 to -40 dBm0 D_R = -55 dBm0 to -50 dBm0	 -0.25 -0.25 -0.5 -1.2		 0.25 0.25 0.5 1.2	 dB dB dB dB
$G_{RAL\,L}$	Receive Gain Variation with signal level (Loudspeaker)	Sinusoidal Test Method Reference Level = –10 dBm0 D_R = 0 dBm0 to +3 dBm0 D_R = -40 dBm0 to 0 dBm0 D_R = -50 dBm0 to -40 dBm0 D_R = -55 dBm0 to -50 dBm0	 -0.25 -0.25 -0,5 -1.2		 0.25 0 25 0.5 1.2	 dB dB dB dB

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DXA	Tx Delay, Absolute	f = 1600 Hz		320		µs
DXR	Tx Delay, Relative	f = 500 - 600 Hz		225		µs
		f = 600 - 800 Hz		125		µs
		f = 800 - 1000 Hz		50		µs
		f = 1000 - 1600 Hz		20		µs
		f = 1600 - 2600 Hz		55		µs
		f = 2600 - 2800 Hz		80		µs
		f = 2800 - 3000 Hz		130		µs
DRA	Rx Delay, Absolute	f = 1600 Hz		252		µs
DRR	Rx Delay, Relative	f = 500 - 1000 Hz		10		µs
		f = 1000 - 1600 Hz		30		µs
		f = 1600 - 2600 Hz		105		µs
		f = 2600 - 2800 Hz		135		µs
		f = 2800 - 3000 Hz		185		µs

NOISE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NXC	Tx Noise, C weighted	V_{MIC} = 0V			16	dBrnC0
NXP	Tx Noise, P weighted	V_{MIC} = 0V			-70	dBm0p
NREC	Rx Noise, C weighted (Earpiece)	Receive PCM code = Alternating Positive and Negative Code			18	dBrnC0
NREP	Rx Noise, P weighted (Earpiece)	Receive PCM code = Positive Zero			-70	dBm0p
NRLC	Rx Noise, C weighted (Loudspeaker)	Receive PCM code = Alternating Positive and Negative code			21	dBrnC0
NRLP	Rx Noise, P weighted (Loudspeaker)	Receive PCM code = Positive Zero			-67	dBm0p
NRS	Noise, Single Frequency	V_{MIC} = 0V, Loop-around measurament from f = 0 Hz to 100 kHz			-50	dBm0
PPSRx	Positive PSRR, Tx	V_{MIC} = 0V, V_{CC} = 5.0 V_{DC} + 100 mV_{rms}; f = 0Hz to 50KHz	30			dB
PPSRp	Positive PSRR, Rx	PCM Code equals Positive Zero, V_{CC} = 5.0 VDC + 100 mVrms, measure $V_{Fr±}$	30			dB
		f = 0 Hz - 4 kHz	30			dB
		f = 4 kHz - 50 kHz	30			dB
SOS	Spurious Out-Band signal at the output	DR input set to 0 dBm0 PCM code 300 - 3400 Hz Input PCM Code applied at DR				
		4600 Hz - 5600 Hz			-40	dB
		5600 Hz - 7600 Hz			-50	dB
		7600 Hz - 8400 Hz			-50	dB
		8400 Hz - 100 kHz			-50	dB

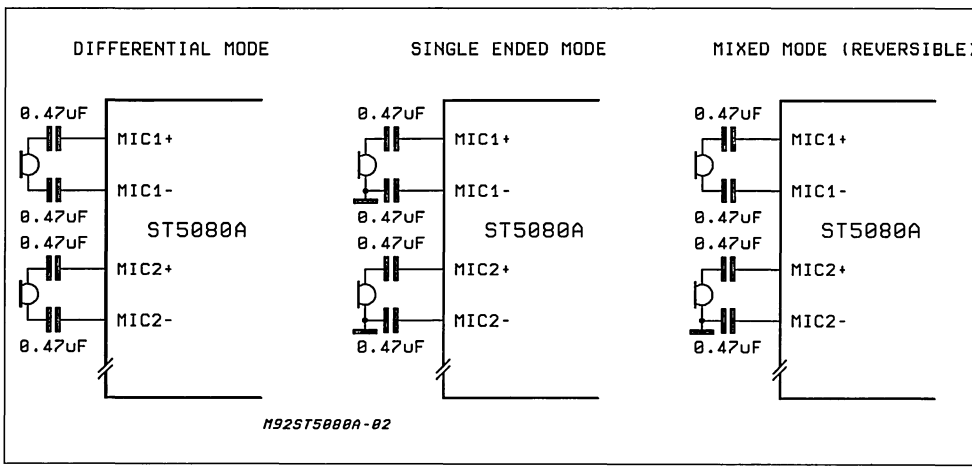
DISTORTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
S_{TDx} S_{TDr}	Signal to Total Distortion	Sinusoidal Test Methode (measured using C message weighting Filter) Level = 0 dBm0 to - 20 dBm0 Level = - 20 to -30 dBm0 Level = - 40 dBm0 Level = - 45 dBm0	 37 36 29 24			 dBC dBC dBC dBC
S_{DFx}	Single Frequency Distortion transmit	0 dBm0 input signal			-46	dB
S_{DFr}	Single Frequency Distortion receive	0 dBm0 input signal			-46	dB
IMD	Intermodulation	Loop-around measurament Voltage at V_{MIC} = -4 dBm0 to -21 dBm0, 2 Frequencies in the range 300 - 3400 Hz			-41	dB

CROSSTALK

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
C_{Tx-r}	Transmit to Receive	Transmit Level = 0 dBm0, f = 300 - 3400 Hz DR = QuietPCM Code			-65	dB
C_{Tr-x}	Receive to Transmit	Receive Level = 0 dBm0, f = 300 - 3400 Hz V_{MIC} = 0V			-65	dB

APPLICATION NOTE FOR MICROPHONE CONNECTIONS



The 4 connection modes (since the MIXED MODE is symmetrical with respect to MIC1 and MIC2) allow one microphone at a time to be selected via the V_S bit (bit 7 of Control Register CR4).

SGS-THOMSON MICROELECTRONICS

ST5088

PIAFE
PROGRAMMABLE ISDN AUDIO FRONT END

ADVANCE DATA

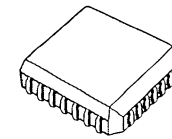
FEATURES:

Complete CODEC and FILTER system including:

- PCM ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS
- POWERFUL ANALOG FRONT END CAPABLE TO INTERFACE DIRECTLY:
  - Microphone Dynamic, Piezo or Electrete
  - Earpiece down to 100Ω or up to 150nF
  - Loudspeaker down to 50Ω or Buzzer up to 600nF.
- TRANSMIT BAND-PASS FILTER
- ACTIVE RC NOISE FILTER
- RECEIVE LOW-PASS FILTER WITH SIN X/X CORRECTION
- MU-LAW OR A-LAW SELECTABLE COMPANDING CODER AND DECODER
- PRECISION VOLTAGE REFERENCE

Phones Features:

- DUAL SWITCHABLE MICROPHONE AMPLIFIER INPUTS. GAIN PROGRAMMABLE: 15 dB RANGE, 1 dB STEP.
- LOUDSPEAKER AMPLIFIER OUTPUT. SWITCHABLE MAXIMUM GAIN: +9dB/+27dB WITH AUTOMATIC DIGITAL ANTICLIPPING SYSTEM. aTTENUATION PROGRAMMABLE: 30dB RANGE, 2dB STEP.
- SEPARATE EARPIECE AMPLIFIER OUTPUT. ATTENUATION PROGRAMMABLE: 15 dB RANGE, 1 dB STEP.
- AUXILIARY TAPE RECORDER ANALOG INTERFACE: Tx + Rx COMBINED OUTPUT.
- AUXILIARY SWITCHABLE EXTERNAL RING INPUT (EAIN).
- TRANSIENT SUPRESSION SIGNAL DURING POWER ON.
- INTERNAL PROGRAMMABLE SIDETONE CIRCUIT. ATTENUATION PROGRAMMABLE: 15 dB RANGE, 1 dB STEP, INDEPENDENT FROM Rx CONTROL.
- INTERNAL RING OR TONE GENERATOR INCLUDING DTMF TONES, SINEWAVE OR SQUAREWAVE WAVEFORMS. ATTENUATION PROGRAMMABLE: 27 dB RANGE, 3 dB STEP.
- RINGER CONTROL PROGRAMMABLE INTERNALLY (µP) OR EXTERNALLY (pin AT)
- COMPATIBLE WITH HANDS-FREE CIRCUIT TEA7540.
- ON CHIP SWITCHABLE ANTI-ACOUSTIC FEED-BACK CIRCUIT (ANTI-LARSEN).



PLCC28

ORDERING NUMBER: ST5088FN

General Features:

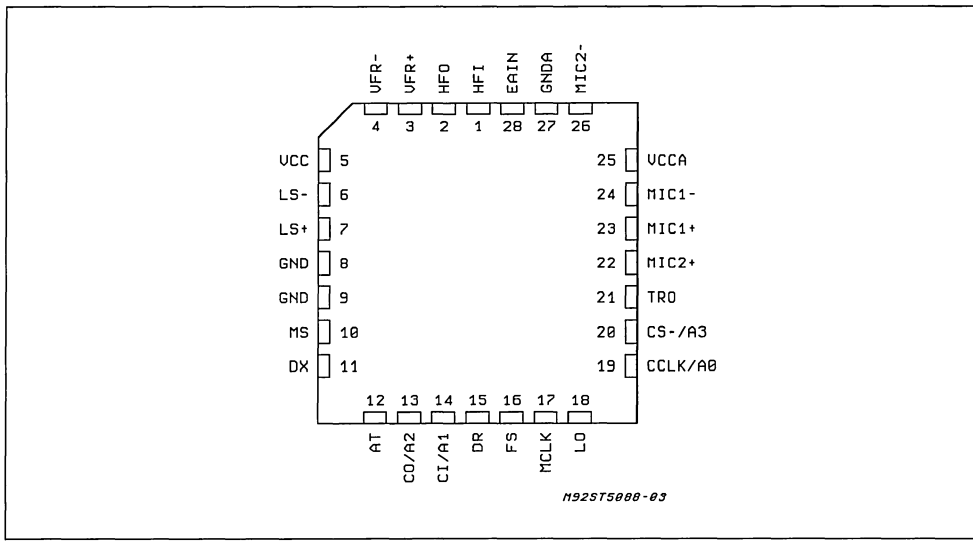
- EXTENDED TEMPERATURE RANGE OPERATION (*) – 25°C TO +85°C.
- EXTENDED POWER SUPPLY RANGE 5V±10%.
- 60 mW OPERATING POWER (TYPICAL).
- 1.0 mW STANDBY POWER (TYPICAL).
- CMOS DIGITAL INTERFACES.
- SINGLE + 5V SUPPLY.
- DIGITAL LOOPBACK TEST MODE.
- PROGRAMMABLE DIGITAL AND CONTROL INTERFACES:
  - –Digital PCM Interface associated with separate serial Control Interface MICROWIRE™ compatible.
  - –GCI interface compatible.

(*) Functionality guaranteed in the range – 25°C to +85°C; Timing and Electrical Specifications are guaranteed in the range – 5°C to +70°C.

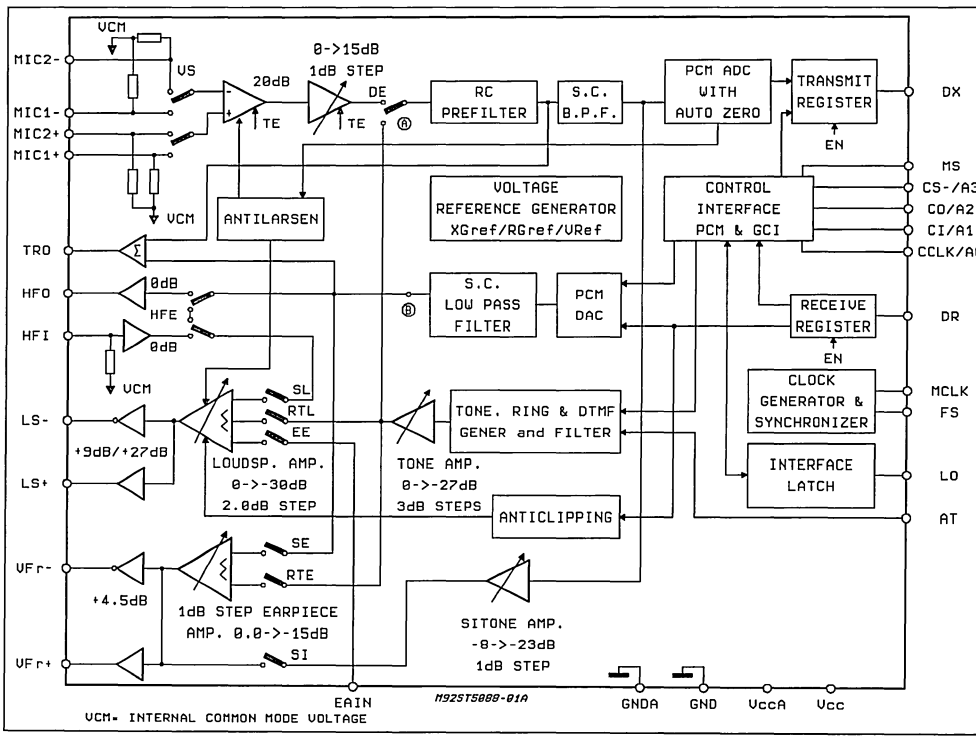
APPLICATIONS:

- ISDN TERMINALS.
- DIGITAL TELEPHONES
- CT2 AND GSM APPLICATIONS

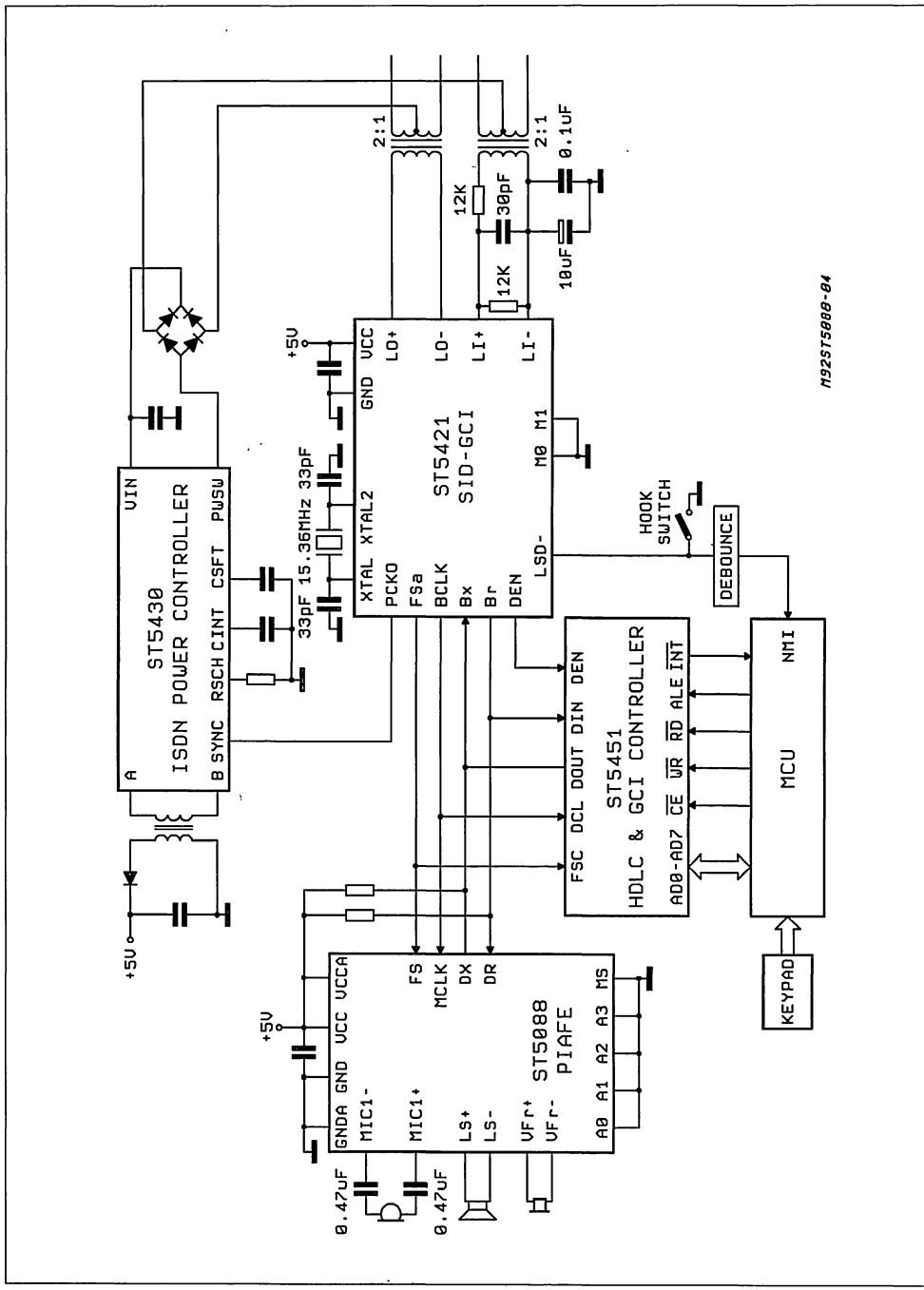
PIN CONNECTION (Top view)



BLOCK DIAGRAM



TYPICAL ISDN TELEPHONE SET APPLICATION



GENERAL DESCRIPTION

ST5088 PIAFE is a combined PCM CODEC/FILTER device optimized for ISDN Terminals and Digital Telephone applications. This device is A-law and Mu-law selectable and offers a number of programmable functions accessed through a serial control channel.
Depending on mode selected, channel control is provided by means of a separate serial channel control MICROWIRE compatible or multiplexed with the PCM voice data channel in a GCI compatible format requiring only 4 digital interface pins. When separate serial control interface is selected, PCM interface is compatible with Combo I and Combo II families of devices such as ETC5057/54, TS5070/71.
PIAFE is built using SGS-THOMSON's advanced HCMOS process.
Transmit section of PIAFE consists of an amplifier with switchable high impedance inputs followed by a programmable gain amplifier, an active RC antialiasing pre-filter to provide attenuation of high frequency noise, an 8th order switched capacitor band pass transmit filter and an A-law/Mu-law selectable compandig encoder.
Receive section consist of an A-law/Mu-law selectable expanding decoder which reconstructs the analog sampled data signal, a 3400 Hz low pass filter with sin X/X correction followed by two separate programmable attenuation blocks and two power amplifiers: one can be used to drive an earpiece, and the other to drive a 50 Ω loudspeaker or a piezo transducer up to 600nF.
When the loudspeaker section is set up with maximum gain (+27dB) the device provide internally a programmable digital anticlipping system to avoid output distortion.
Programmable functions on PIAFE include a Ring/Tone generator which provides one or two tones and can be directed to earpiece or to loudspeaker (or buzzer).
A simple ringer control interface can bypass µP control of sweep frequency and ring ON/OFF phases.
A separate programmable gain amplifier allows gain control of the signal injected. Ring/Tone generator provides sinewave or squarewave signal with precise frequencies which may be also directed to the input of the Transmit amplifier for DTMF tone generation.
An auxiliary analog input (EAIN) is also provided to enable for example the output of an external band limited Ring signal to the Loudspeaker. Transmit signal may be fed back into the receive ampifier with a programmable attenuation to provide a sidetone circuitry.
A switchable anti-accoustic feed-back system cancels the larsen effect in speech monitoring application.
Two additional pins are provided for insertion of an external Handfree function in the Loudspeaker receive path.
An output latch controlled by register programming permits external device control.

PIN FUNCTIONS

Pin	Name	Description
1,2	HFI, HFO	Hands free I/Os: These two pins can be used to insert an external Handfree circuit such as the TEA 7540 in the receive path. HFO is an output which provides the signal issued from output of the receive low pass filter while HFI is a high impendance input which is connected directly to one of the inputs of the Loudspeaker amplifier.
3,4	V_{Fr+}, V_{Fr-}	Receive analog earpiece amplifier complementary outputs, capable of driving load impedances between 100 and 400 Ω or a piezo ceramic transducer up to 150nF. These outputs can drive directly earpiece transductor. The signal at this output can drive be the summ of: - Receive Speech signal from D_R, - Internal Tone Generator, - Sidetone signal.
5	V_{CC}	Positive power supply input for the digital section. +5 V ± 10%.
6,7	LS-,LS+	Receive analog loudspeaker amplifier complementary outputs, intended for driving a Loudspeaker: 80 mW on 50Ω load impedance can be provided at low distorsion meeting specifications. Alternatively this stage can drive a piezo transducer up to 600nF. The signal at these outputs can be the sum of: - Receive Speech signal from D_R, - Internal Tone generator, - External input signal from EAIN input.

PIN FUNCTIONS (continued)

Pin	Name	Description
8,9	GND	Ground: All digital signals are referenced to this pin.
10	MS	Mode Select: This input selects COMBO I/II interface mode with separate MICROWIRE Control interface when tied high and GCI mode when tied low.
11	D_X	Transmit Data ouput: Data is shifted out on this pin during the assigned transmit time slots. Elsewhere D_X output is in the high impendance state. In COMBO I/II mode, voice data byte is shifted out from TRISTATE output D_X at the MCLK frequency on the rising edge of MCLK. In GCI mode, voice data byte and control bytes are shifted out from OPEN-DRAIN output D_X at half the MCLK. An external pull up resistor is needed.
12	AT	Alternate Tone: Ring frequency out is controlled without µP intervention. Tri-state logic controls: f1 (Vcc), f2 (GND), pause (High Impedance).
15	D_R	Receive data input: Data is shifted in during the assigned Received time slots. In the COMBO I/II mode, voice data byte is shifted in at the MCLK frequency on the falling edges of MCLK. In the GCI mode, PCM data byte and contol byte are shifted in at half the MCLK frequency on the receive rising edges of MCLK. There is one period delay between transmit rising edge and receive rising edge of MCLK.
16	FS	Frame Sync input: This signal is a 8kHz clock which defines the start of the transmit and receive frames. Either of three formats may be used for this signal: non delayed timing mode, delayed timing and GCI compatible timing mode.
17	MCLK	Master Clock Input: This signal is used by the switched capacitor filters and the encoder/decoder sequencing logic. Values must be 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz selected by means of Control Register CR0. MCLK is used also to shift-in and out data. In GCI mode, 2.56 MHz and 512 kHz are not allowed.
18	LO	Open drain output: a logic 1 written into DO (CR1) appears at LO pin as a logic 0 a logic 0 written into DO puts LO pin in high impedance.
21	TRO	Tape Recorder Output: This pin provides the analog combination of Tx voice signal and Rx voice signal.
22	MIC2+	Alternative positive high impedance input to transmit pre-amplifier.
23	MIC1+	Positive high impedance input to transmit pre-amplifier for microphone symetrical connection.
24	MIC1-	Negative high impedance input to transmit pre-amplifier for microphone symetrical connection.
25	V_{CCA}	Positive power supply input for the analog section. +5 V ± 10%. V_{CC} and V_{CCA} must be directly connected together.
26	MIC2-	Alternative negative high impedance input to transmit pre-amplifier.
27	GNDA	Analog Ground: All analog signals are referenced to this pin. GND and GNDA must be connected together close to the device.
28	EAIN	External Auxiliary input: This input can be used to provide alternate signals to the Loudspeaker in place of Internal Ring generator. Input signal should be voice band limited.

Following pin definitions are used only when COMBO I/II mode with separate MICROWIRE compatible serial control port is selected. (MS input set equal one)

PIN FUNCTIONS (continued)

Pin	Name	Description
13	CO	Control data Output: Serial control/status information is shifted out from the PIAFE on this pin when CS- is low on the falling odges of CCLK.
14	CI	Control data Input: Serial Control information is shifted into the PIAFE on this pin when CS- is low on the rising edges of CCLK.
19	CCLK	Control Clock input: This clock shifts serial control information ınto CI and out from CO when the CS- input is low, depending on the current ınstruction. CCLK may be asynchronous with the other system clocks.
20	CS-	Chip Select input: When this pin is low, control information is written into and out from the PIAFE via CI and CO pins.

Following pin definitions are used only when the GCI mode is selected. (MS input set equal zero)

PIN FUNCTIONS (continued)

Pin	Name	Description
19,14,13,20	A0,A1,A2,A3	These pins select the address of PIAFE on GCI ınterface and must be hardwired to either V_{CC} or GND. A0,A1,A2,A3 refer to C4,C5,C6,C7 bits of the first address byte respectively.

FUNCTIONAL DESCRIPTION

Power on initialization:
When power is first applied, power on reset ciıtry initializes PIAFE and puts it into the power down state. Gain Control Registers for the various programmable gain amplifiers and programmable switches are initialized as indicated in the Control Register description section. All CODEC functions are disabled. Digital Interface is configured in GCI mode or in COMBO I/II mode depending on Mode Select pin connection.
The desired selection for all programmable functions may be intialized prior to a power up command using Monitor channel in GCI mode or MICROWIRE port in COMBO I/II mode.

Power up/down control:
Following power-on initialization, power up and power down control may be accomplished by writing any of the control instructions listed in Table 1 into PIAFE with "P" bit set to 0 for power up or 1 for power down.
Normally, it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or in a separate single byte instruction.
Any of the programmable registers may also be modified while ST5088 is powered up or down by setting "P" bit as indicated. When power up or down control is entered as a single byte instruction, bit 1 must be set to a 0.

When a power up command is given, all de-activated circuits are activated, but output D_X will remain in the high impedance state on B time slots until the second Fs pulse after power up, even if a B channel is selected.

Power down state:
Following a period of activity, power down state may be reentered by writing a power down instruction.
Control Registers remain in their current state and can be changed either by MICROWIRE control interface or GCI control channel depending on mode selected.
In addition to the power down instruction, detection of loss MCLK (no transition detected) automatically enters the device in "reset" power down state with D_X output in the high impedance state and L0 in high impedance state.

Transmit section:
Transmit analog interface is designed in two stages to enable gains up to 35 dB to be realized. Stage 1 is a low noise differential amplifier providing 20 dB gain. A microphone may be capacitevely connected to MIC1+, MIC1- inputs, while the MIC2+ MIC2– inputs may be used to capacitively connect a second microphone (for digital handsfree operation) or an auxiliary audio circuit such as TEA 7540 Hands-free circuit. MIC1 or MIC2 source is selected with bit 7 of register CR4.
Following the first stage is a programmable gain

amplifier which provides from 0 to 15 dB of additional gain in 1 dB step. The total transmit gain should be adjusted so that, at reference point A, see Block Diagram description, the internal 0 dBmO voltage is 0.739 V (overload level is 1.06 Vrms). Second stage amplifier can be programmed with bits 4 to 7 of CR5. To temporarily mute the transmit input, bit TE (6 of CR4) may be set low. In this case, the analog transmit signal is grounded and the sidetone path is also disabled.
An active RC prefilter then precedes the 8th order band pass switched capacitor filter. A/D converter has a compressing characteristic according to CCITT A or mu255 coding laws, which must be selected by setting bits MA, IA in register CR0. A precision on chip voltage reference ensures accurate and highly stable transmission levels.
Any offset voltage arising in the gain-set amplifier, the filters or the comparator is cancelled by an internal autozero circuit.
Each encode cycle begins immediatly at the beginning of the selected Transmit time slot. The total signal delay referenced to the start of the time slot is approximatively 195 µs (due to the transmit filter) plus 123 µs (due to encoding delay), which totals 320 µs. Voice data is shifted out on D_X during the selected time slot on the transmit rising adges of MCLK.

Receive section:
Voice Data is shifted into the decoder's Receive voice data Register via the D_R pin during the selected time slot on the 8 receive edges of MCLK.
The decoder consists of an expanding DAC with either A or MU255 law decoding characteristic which is selected by the same control instruction used to select the Encode law during intitialization. Following the Decoder is a 3400 Hz 6th order low pass switched capacitor filter with integral Sin X/X correction for the 8 kHz sample and hold.
0 dBmO voltage at this (B) reference point (see Block Diagram description) is 0.49 Vrms. A transcient suppressing circuitry ensure interference noise suppression at power up.
The analog speech signal output can be routed either to earpiece (V_{FR+}, V_{FR-} outputs) or to loudspeaker (LS+, LS- outputs) by setting bits SL and SE (1 and 0 of CR4).
Total signal delay is approximatively 190 µs (filter plus decoding delay) plus 62.5 µs (1/2 frame) which gives approximatively 252 µs.
Differential outputs V_{FR+},V_{FR-} are intended to directly drive an earpiece. Preceding the outputs is a programmable attenuation amplifier, which must be set by writing to bits 4 to 7 in register CR6. Attenuations in the range 0 to -15 dB relative to the maximum level in 1 dB step can be programmed. The input of this programmable amplifier is the summ of several signals which can be selected by writing to register CR4.:

- Receive speech signal which has been decoded and filtered,
- Internally generated tone signal, (Tone amplitude is programmed with bits 4 to 7 of register CR7),
- Sidetone signal, the amplitude of which is programmed with bits 0 to 3 of register CR5

V_{FR+} and V_{FR-} outputs are capable of driving output power level up to 14mW into differentially connected load impedance between 100 and 400 Ω.

Differential outputs LS+,LS- are intended to directly drive a Loudspeaker. Preceding the outputs is a programmable attenuation amplifier, which must be set by writing to bits 0 to 3 in register CR6. Attenuations in the range 0 to -30 dB relative to the maximum level in 2.0 dB step can be programmed. The input of this programmable amplifier can be the summ of signals which can be selected by writing to register CR4:

- Receive speech signal which has been decoded and filtered,
- Internally generated tone signal, (Tone amplitude is programmed with bits 4 to 7 of register CR7),
- EAIN input which may be an alternate Ring signal or any voice frequency band limited signal. (An external decoupling capacitor of about 0.1µF is necessary).

Receive voice signal may be directed to output HFO by means of bit HFE in Register CR4. After processing, signal must be re-entered through input HFI to Loudspeaker amplifier input. (An external decoupling capacitor of about 0.1µF is necessary).
The output loudspeaker section has two switchable gains of +9dB and +27dB.

+9dB LS Gain
This gain mode is fully equivalent to PIAFE ST5080 behaviour.
LS+ and LS- outputs are capable of driving output power level up to 80 mW into 50 Ω differentially connected load impedance at low distortion meeting PCM channel specifications. When the signal source is a Ring squarewave signal, power levels up to approximatively 200 mW can be delivered.

+27dB LS Gain
Additional gain of 18dB has the purpose to increase the undistorted output power up to 150mW typical with digital input DR ranging from -12dBm0 to +3dBm0.
Output DC offset is limited by high pass filter with 35Hz cut frequency (with LS gain = +9dB cut frequency = 9Hz)
Anti-acoustic feed-back for loudspeaker to hand-

set microphone loop with squelch effect: on chip switchable anti-larsen for loudspeaker to handset microphone feedback is implemented. A 12dB depth gain control on both transmit and receive path is provided to keep constant the loop gain. On the transmit path the 12dB gain control is provided starting from the CR5 transmit gain definition; at the same time, on the receive path the 12dB gain control is provided starting from CR6 receive gain definition.

DIGITAL ANTICLIPPING SYSTEM (D.A.S.)

An automatic anticlipping system is necessary to avoid distortion on LS+/LS- when the output swing approaches the supply rails. (LS GAIN >> +9dB).
The digital anticlipping system calculates equivalent input signal on DR pin and compares it with a selectable anticlipping threshold. The D.A.S. is then able to reduce the overall gain in order to avoid or limit the distortion.
Four different thresholds are programmable via register:

-15dBm0	D < 1%	For safe margin
-13dBm0	D = 1%	For normal operation
-9dBm0	D ≥ 1%	For noisy ambient (*)
-7dBm0	D >> 1%	For very noisy ambient (*)

(*) When environment is noisy, power output might be more important than 1% distortion.

Gain reduction of the D.A.S. (Anticlipping Attack) has a fixed speed of 8KHz.
Gain recovery or increase (Anticlipping Release) has 4 programmable speeds of 4Hz, 8Hz, 31Hz and 62Hz.

TAPE RECORDER OUTPUT (TRO)

This section provides a combination of Tx and Rx Analog Signals to an external user like a recordering machine. The output levels relative to a signal of 0dBm0 on channel Dx and DR are:
Rx TRO = $0.245V_{RMS}$ (for 0dBm0 on DR)
Tx TRO = $0.246V_{RMS}$ (for 0dBm0 on DX)
The single ended Op Amp is able to drive an external load as low as 600Ω.

ALTERNATE TONE CONTROL (AT)

This section allows to simplify the microprocessor control of ringer operation. When pin AT is put externally at high impedance state (or left open) the control of ring frequency emission is totally through a microprocessor, which updates in real time the contents of various registers.
When pin AT is forced at GND or Vcc the ring generator emits respectively the frequencies f2 (GND) and f1 (Vcc), previously defined through registers CR9 (f2) and CR8(f1). This operative mode requires only start-up intervention of the microprocessor.

Digital and Control Interface:

PIAFE provides a choice of either of two types of Digital Interface for both control data and PCM.
For compatibility with systems which use time slot oriented PCM busses with a separate Control Interface, as used on COMBO I/II families of devices, PIAFE functions are described in next section.
Alternatively, for systems in which PCM and control data are multiplexed together using GCI interface scheme, PIAFE functions are described in the section following the next one.
PIAFE will automatically switch to one of these two types of interface by sensing the MS pin.
Due to Line Transceiver clock recovery circuitry, a low jitter may be provided on F_S and MCLK clocks. F_S and MCLK must be always in phase. For ST5421S Transceiver, as an example, maximun value of jitter amplitude is a step of 65 ns at each GCI frame (125µs). So, the maximum jitter amplitude is 130 ns pk-pk.

COMBO I/II mode.

Digital Interface (Fig. 1)

F_S Frame Sync input determines the beginning of frame. It may have any duration from a single cycle of MCLK to a squarewave. Two different relationships may be established between the Frame Sync input and the first time slot of frame by setting bit 3 in register CR0. Non delayed data mode is similar to long frame timing on ETC5057/ TS5070 series of devices (COMBO I and COMBO II respectively): first time slot begins nominally coincident with the rising edge of F_S. Alternative is to use delayed data mode, which is similar to short frame sync timing on COMBO I or COMBO II, in which F_S input must be high at least a half cycle of MCLK earlier the frame beginning. A time slot assignment circuit on chip may be used with both timing modes, allowing connection to one of the two B1 and B2 voice data channels.
Two data formats are available: in Format 1, time slot B1 corresponds to the 8 MCLK cycles following immediately the rising edge of FS, while time slot B2 corresponds to the 8 MCLK cycles following immediately time slot B1.
In Format 2, time slot B1 is identical to Format 1. Time slot B2 appears two bit slots after time slot B1. This two bits space is left available for insertion of the D channel data.
Data format is selected by bit FF (2) in register CR0. Time slot B1 or B2 is selected by bit T0 (0) in Control Register CR1.
Bit EN (2) in control register CR1 enables or disables the voice data transfer on D_X and D_R as

Figure 1: Digital Interface Format

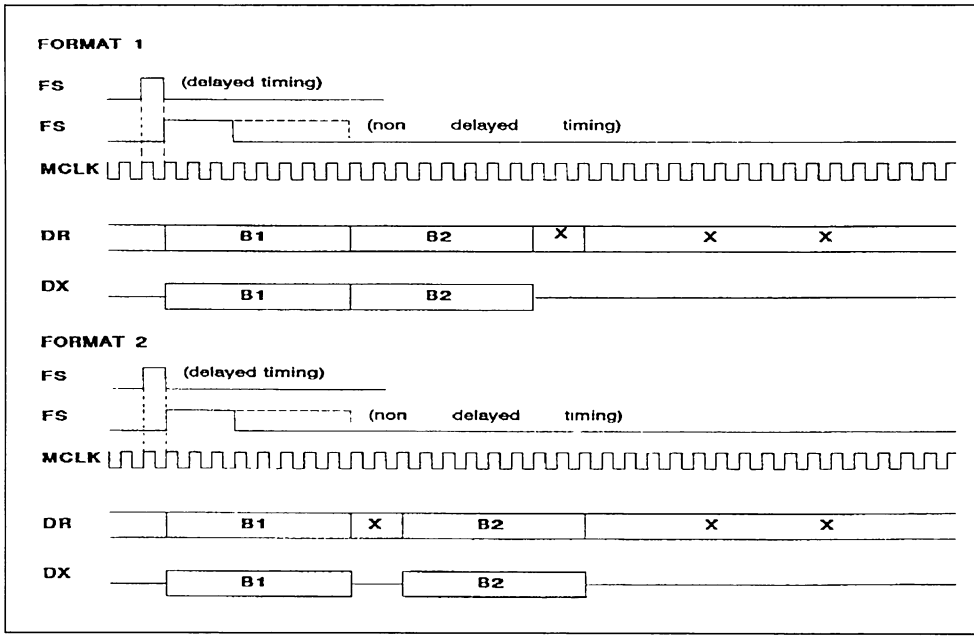
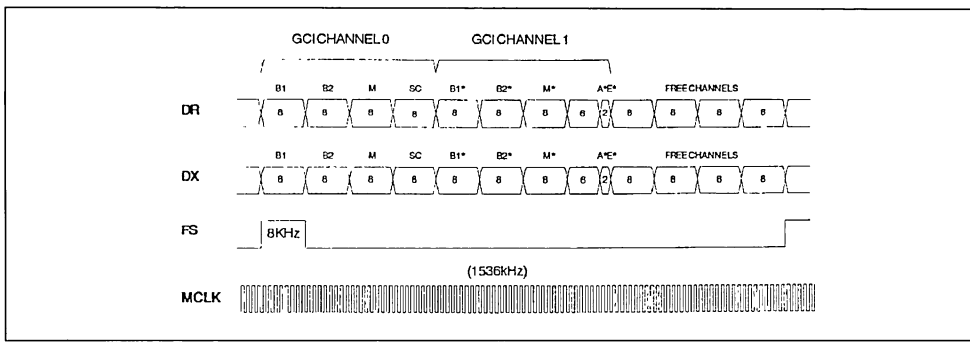


Figure 2: GCI Interface Frame Structure



appropriate. During the assigned time slot, D_X output shifts data out from the voice data register on the rising edges of MCLK. Serial voice data is shifted into D_R input during the same time slot on the falling edges of MCLK.
D_X is in the high impedance Tristate condition when in the non selected time slots.

Control Interface:
Control information or data is written into or read-back from PIAFE via the serial control port consisting of control clock CCLK, serial data input CI and output CO, and Chip Select input, CS-. All control instructions require 2 bytes as listed in Table 1, with the exception of a single byte power-up/down command.
To shift control data into ST5088, CCLK must be pulsed high 8 times while CS- is low. Data on CI input is shifted into the serial input register on the rising edge of each CCLK pulse. After all data is shifted in, the content of the input shift register is decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide CS- pulse or may follow the first contiguously, i.e. it is not mandatory for CS- to return high in between

the first and second control bytes. At the end of the 2nd control byte, data is loaded into the appropriate programmable register. CS- must return high at the end of the 2nd byte.
To read-back status information from PIAFE, the first byte of the appropriate instruction is strobed in during the first CS- pulse, as defined in Table 1. CS- must be set low for a further 8 CCLK cycles, during which data is shifted out of the CO pin on the falling edges of CCLK.
When CS- is high, CO pin is in the high impedance Tri-state, enabling CO pins of several devices to be multiplexed together.
Thus, to summarise, 2 byte READ and WRITE instructions may use either two 8-bit wide CS- pulses or a single 16 bit wide CS- pulse.

Control channel access to PCM interface:
It is possible to access the B channel previously selected in Register CR1.
A byte written into Control Register CR3 will be automatically transmitted from D_X output in the following frame in place of the transmit PCM data.
A byte written into Control Register CR2 will be automatically sent through the receive path to the Receive amplifiers.
In order to implement a continuous data flow from the Control MICROWIRE interface to a B channel, it is necessary to send the control byte on each PCM frame.
A current byte received on D_R input can be read in the register CR2. In order to implement a continuous data flow from a B channel to MICROWIRE interface, it is necessary to read register CR2 at each PCM frame.

GCI COMPATIBLE MODE

GCI interface is an European standardized interface to connect ISDN dedicated components in the different configurations of equipment as Terminals, Network Terminations, PBX, etc...
In a Terminal equipment, this interface called SCIT for Special Circuit Interface for Terminals allows for example connection between:

- ST5421 (SID-GCI) and ST5451 (HDLC/GCI controller) used for 16 kbit/s D channel packet frames processing and SID control,
- Peripheral devices connected to a 64 kbit/s B channel and ST5451 used for GCI peripheral control.

ST5088 may be assigned to one of the B channels present on the GCI interface and is monitored via a control channel which is multiplexed with the 64 kbit/s Voice Data channels.

Figure 2 shows the frame structure at the GCI interface. Two 256 kbit/s channel are supported.

a)GCI channel 0: It is structured in four subchannels:
- B1 channel 8 bits per frame
- B2 channel 8 bits per frame
- M channel 8 bits per frame ignored by PIAFE
- SC channel 8 bits per frame ignored by PIAFE

Only B1 or B2 channel can be selected in PIAFE for PCM data transfer.

b)GCI channel 1: It is structured also in four subchannels:
- B1* channel 8 bits per frame
- B2* channel 8 bits per frame
- M* channel 8 bits per frame
- SC* which is structured as follows:

6 bits ignored by PIAFE
A* bit associated with M* channel
E* bit associated with M* channel.
B1* or B2* channel can be selected in PIAFE for PCM data transfer.
M* channel and two associated bits E* and A* are used for PIAFE control.

Thus, to summarize, B1, B2, B1* or B2* channel can be selected to transmit PCM data and M* channel is used to read/write status/command peripheral device registers. Protocol for byte exchange on the M* channel uses E* and A* bits.

Physical Interface
The interface is physically constitued with 4 wires:

Input Data wire:	D_R
Output Data wire:	D_X
Bit Clock:	MCLK
Frame Synchronization:	F_S

Data is synchronized by MCLK and F_S clock inputs.
F_S insures reinitialization of time slot counter at each frame beginning. The rising edge or FS is the reference time for the first GCI channel bit.
Data is transmitted in both directions at half the MCLK input frequency. Data is transmitted on the the rising edge of MCLK and is sampled one period after the transmit rising edge, also on a rising edge.
Note: Transmit data may be sampled by far-end device ie SID ST5421 on the falling edge 1.5 period after the transmit rising edge.
Unused channel are high impedance. Data outputs are OPEN-DRAIN and need an external pull up resistor.

COMBO activation/deactivation
ST5088 is automatically set in power down mode when GCI clocks are idle. GCI section is reactivated when GCI clocks are detected. PIAFE is completly reactivated after receiving of a power up command.

Exchange protocol on M* channel
Protocol allows a bidirectional transfer of bytes between ST5088 and GCI controller with acknowledgment at each received byte. For PIAFE, standard protocol is simplified to provide read or write register cycles almost identical to MICROWIRE serial interface.

Write cycle
Control Unit sends through the GCI controller following bytes:

- First byte is the chip select byte. The first four bits indicate the device address: (A3,A2,A1,A0). The four last bits are ignored. ST5088 compare the validated byte received internally with the address defined by pins A3, A2, A1, A0. If comparison is true, byte is acknowledged, if not, ST5088 does not acknowledge the byte.

NOTE: An internal "message in progress" flag remains active till the end of the complete message transmission to avoid irrelevant acknowledgement of any further byte.

- Second byte is structured as defined in Table 1.
- Third byte is the Data byte to write into the Register as indicated in Table 1.

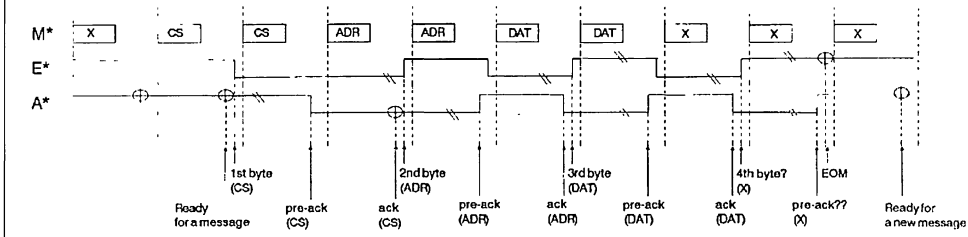
It is possible but optional to write to several different registers in a single message. In this case the Chip Select byte is sent only once at the beginning of the message, the device automatically toggles between address byte and data byte.

Read cycle
Control Unit sends two bytes. First byte is the chip select byte as defined above. Second byte is structured as defined in Table 1.
If PIAFE identifies a read-back cycle, bit 2 of byte 1 in Table 1 equal 1, it has to respond to the Control Unit by sending a single byte message which is the content of the addressed register.
It is possible but optional to request several different read-back register cycles in a single message but it is recommended to wait the answer before requesting a new read back to avoid loss of data. ST5088 responds by sending a single data byte message at each request.

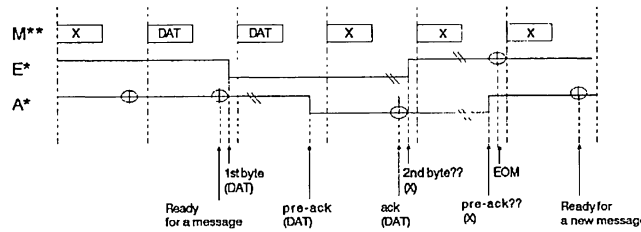
Received byte validation:
A received byte is validated if it is detected two consecutive times identical.

Exchange Protocol:
Exchange protocol is identical for both directions. Sender uses E* bit to indicate that it is sending a M* byte while receiver uses A* bit to acknowledge received byte.
When no message is transferred, E* bit and A* bit are forced to inactive state.
A transmission is initialized by sender putting E* bit from inactive state to active state and by sending first byte on M* channel in the same frame.
Transmission of a message is allowed only if A* bit from the receiver has been set inactive for at least two frames.
When receiver is ready, it validates the received byte internally when received in two consecutive frames identical. Then the receiver sets first A* bit from inactive to active state (pre-acknowlegement), and maintains A* bit active at least in the following frame (acknowledgement). If validation is not possible, (two last bytes received are not identical), receiver aborts the message setting A* bit active for only a single frame.
For the first byte received, Abort sequence is not allowed. PIAFE does not respond either if two last bytes are not identical or if the byte received does not meet the Chip Select byte defined by A0-A3 pins bias.
A second byte may be transmitted by the sender putting E* bit from active to inactive state and sending the second byte on the M* channel in the same frame. E* bit is set inactive for only one frame. If it remains inactive more than one frame, it is an end of message (i.e. not second byte available).
The second byte may be transmitted only after receiving the pre-acknowledgment of the previous byte transmitted (see Fig. 3). The same protocol is used if a third byte is transmitted. Each byte has to be transmitted at least in two consecutive frames.
The receiver validates current received byte as done on first byte and then set A* bit in the next two frames first from active to inactive state (pre-acknowledgement), and after from inactive to active state (acknowledgement). If the receiver cannot validate the received current byte (two bytes received are not identical), it pre-acknowledges normally, but let A* bit in the inactive state in the next frame which indicates an abort request.
If a message sent by ST5088 is aborted, it will stop the message and wait for a new read cycle instruction from the controller.
A message received by ST5088 is acknowledged or aborted without flow Control.
Figures 3 gives timing of a write cycle. Most significant bit (MSB) of a Monitor byte is sent first on M* channel.
E* and A* bits are active low and inactive state on DOUT is high impedance.

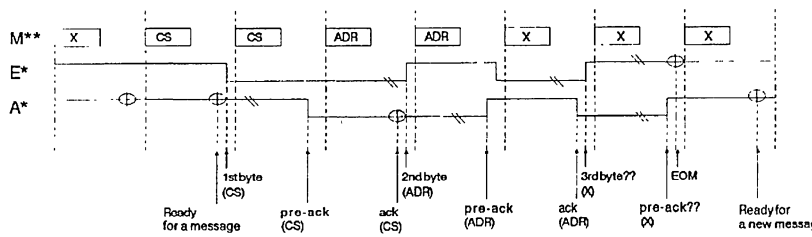
Figure 3: E and A bits Timing



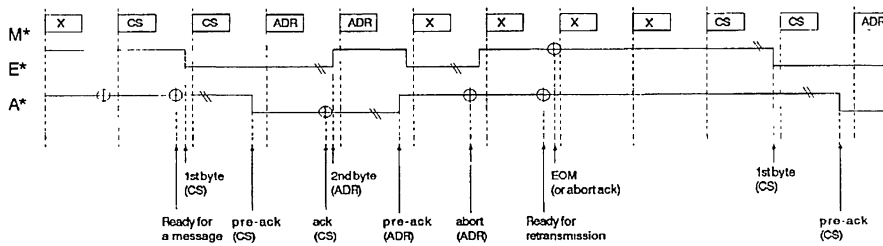
THREE BYTES MESSAGE - NORMAL TRANSMISSION



ONE BYTE MESSAGE - NORMAL TRANSMISSION



TWO BYTES MESSAGE - NORMAL TRANSMISSION



TWO BYTES MESSAGE ABORTED ON THE SECOND AND RETRANSMITTED

PROGRAMMABLE FUNCTIONS

For both formats of Digital Interface, programmable functions are configured by writing to a number of registers using a 2-byte write cycle (not including chip select byte in GCI).

Most of these registers can also be read-back for verification. Byte one is always register address, while byte two is Data.

Table 1 lists the register set and their respective adresses.

Table 1: Programmable Register Intructions

Function	Address byte								Data byte
	7	6	5	4	3	2	1	0	
Single byte Power up/down	P	X	X	X	X	X	0	X	none
Write CR0	P	0	0	0	0	0	1	X	see CR0 TABLE 2
Read-back CR0	P	0	0	0	0	1	1	X	see CR0
Write CR1	P	0	0	0	1	0	1	X	see CR1 TABLE 3
Read-back CR1	P	0	0	0	1	1	1	X	see CR1
Write Data to receive path	P	0	0	1	0	0	1	X	see CR2 TABLE 4
Read data from D_R	P	0	0	1	0	1	1	X	see CR2
Write Data to D_X	P	0	0	1	1	0	1	X	see CR3 TABLE 5
Write CR4	P	0	1	0	0	0	1	X	see CR4 TABLE 6
Read-back CR4	P	0	1	0	0	1	1	X	see CR4
Write CR5	P	0	1	0	1	0	1	X	see CR5 TABLE 7
Read-back CR5	P	0	1	0	1	1	1	X	see CR5
Write CR6	P	0	1	1	0	0	1	X	see CR6 TABLE 8
Read-back CR6	P	0	1	1	0	1	1	X	see CR6
Write CR7	P	0	1	1	1	0	1	X	see CR7 TABLE 9
Read-back CR7	P	0	1	1	1	1	1	X	see CR7
Write CR8	P	1	0	0	0	0	1	X	see CR8 TABLE 10
Read-back CR8	P	1	0	0	0	1	1	X	see CR8
Write CR9	P	1	0	0	1	0	1	X	see CR9 TABLE 11
Read-back CR9	P	1	0	0	1	1	1	X	see CR9
Write	P	1	0	1	0	0	1	X	see CR10 TABLE 12
Read-back CR10	P	1	0	1	0	1	1	X	see CR10

NOTE 1: bit 7 of the address byte and data byte is always the first bit clocked into or out from CI and CO pins when MICROWIRE serial port is enabled, or into and out from D_R and D_X pins when GCI mode selected.
X = reserved: write 0

NOTE 2: "P" bit is Power up/down Control bit. P = 1 Means Power Down.
Bit 1 indicates, if set, the presence of a second byte.

NOTE 3: Bit 2 is write/read select bit.

Table 2: Control Register CR0 Functions

7	6	5	4	3	2	1	0	Function		
F1	F0	MA	IA	DN	FF	B7	DL			
0	0							MCLK = 512 kHz		(1)
0	1							MCLK = 1.536 MHz	*	
1	0							MCLK = 2.048 MHz		
1	1							MCLK = 2.560 MHz		(1)
		0	0					MU-law; CCITT D3-D4	*	
		0	1					MU-law; Bare Coding		
		1	0					A-law including even bit inversion		
		1	1					A-law; Bare Coding		
				0				Delayed data timing	*	(1)
				1				Non delayed data timing		(1)
					0			B1 and B2 consecutive	*	(1)
					1			B1 and B2 separated		(1)
						0		8 bits time-slot	*	
						1		7 bits time-slot		
							0	Normal operation	*	
							1	Digital Loop-back		

*: state at power on initialization

(1): significant in COMBO I/II mode only

Table 3: Control Register CR1 Functions

7	6	5	4	3	2	1	0	Function		
HFE	ALE	DO	MR	MX	EN	T1	T0			
0								HFO / HFI pins disabled	*	
1								HFO / HFi pins enabled		
	0							Anti-larsen disabled	*	
	1							Anti-larsen enabled		
		0						L0 latch is put in high impedance	*	
		1						L0 latch set to 0		
			0					D_R connected to rec. path	*	(1)
			1					CR2 connected to rec. path		(1)
				0				Trans path connected to D_X	*	(1)
				1				CR3 connected to D_X		(1)
					0			voice data transfer disable	*	
					1			voice data transfer enable		
						0	0	B1 channel selected	*	
						0	1	B2 channel selected		
						1	0	B1* channel selected		(2)
						1	1	B2* channel selected		(2)

*: state at power on initialization

(1): significant in COMBO I / II mode only

(2): significant in GCI mode only.

Table 4: Control Register CR2 Functions

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb							lsb	Data sent to Receive path or Data received from D_R input

Table 5: Control Registers CR3 Functions

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb							lsb	D_X data transmitted

Table 6: Control Register CR4 Functions

7	6	5	4	3	2	1	0	Function	
VS	TE	SI	EE	RTL	RTE	SL	SE		
0 1								MIC1 selected MIC2 selected	*
	0 1							Transmit input muted Transmit input enabled	*
		0 1						Internal sidetone disabled Internal sidetone enabled	*
			0 1					EAIN disconnected EAIN selected to Loudspeaker	*
				0 0 1 1	0 1 0 1			Ring / Tone muted Ring / Tone to Earpiece Ring / Tone to Loudspeaker Ring / Tone to Earpiece and Loudspeaker	*
						0 0 1 1	0 1 0 1	Receive signal muted Receive signal connected to earpiece amplifer Receive signal connected to loudspeaker amplifier Receive signal connected to loudspeaker and earpiece amplifier	*

* state at power on initialization

Table 7: Control Register CR5 Functions

7	6	5	4	3	2	1	0	Function
Transmit amplifier				Sidetone amplifier				
0	0	0	0					0 dB gain *
0	0	0	1					1 dB gain
-	-	-	-					in 1 dB step
1	1	1	1					15 dB gain
				0	0	0	0	-8 dB gain *
				0	0	0	1	-9 dB gain
				-	-	-	-	in 1 dB step
				1	1	1	1	-23 dB gain

*: state at power on initialization

Table 8: Control Register CR6 Functions

7	6	5	4	3	2	1	0	Function
Earpiece ampifier				Loudspeaker				
0	0	0	0					0 dB gain *
0	0	0	1					-1 dB gain
-	-	-	-					in 1 dB step
1	1	1	1					-15 dB gain
				0	0	0	0	0 dB gain *
				0	0	0	1	-2 dB gain
				-	-	-	-	in 2 dB step
				1	1	1	1	-30 dB gain

*: state at power on initialization

Table 9: Control Register CR7 Functions

7	6	5	4	3	2	1	0	Function		
Tone gain				F1	F2	SN	DE	Attenuation	f1 V_{pp}	f2 V_{pp}
0	0	0	0					0 dB *	2.4 (1)	1.9 (1)
0	0	0	1					-3 dB	1.70	1.34
0	0	1	0					-6 dB	1.20	0.95
0	0	1	1					- 9 dB	0.85	0.67
0	1	0	0					-12 dB	0.60	0.47
0	1	0	1					-15 dB	0.43	0.34
0	1	1	0					-18 dB	0.30	0.24
0	1	1	1					-21 dB	0.21	0.17
1	X	X	0					-24 dB	0 15	0.12
1	X	X	1					-27 dB	0 10	0.08
				0	0			f1 and f2 muted *		
				0	1			f2 selected		
				1	0			f1 selected		
				1	1			f1 and f2 in summed mode		
						0		Squarewave signal selected *		
						1		Sinewave signal selected		
							0	Normal operation *		
							1	Tone / Ring Generator connected toTransmit path		

*: state at power on initialization

(1): value provided if f1 or f2 is selected alone.
if f1 and f2 are selected in the summed mode, f1=1.34 V_{pp} while f2=1.06 V_{pp}
Output generator is 2.4 V_{pp}

X reserved: write 0

Table 10: Control Register CR8 Functions

7	6	5	4	3	2	1	0	Function
f17	f16	f15	f14	f13	f12	f11	f10	
msb							lsb	Binary equivalent of the decimal number used to calculate f1

Table 11: Control Register CR9 Functions

7	6	5	4	3	2	1	0	Function
f27	f26	f25	f24	f23	f22	f21	f20	
msb							lsb	Binary equivalent of the decimal number used to calculate f2

Table 12: Control Register CR10 Functions

7	6	5	4	3	2	1	0	Function
GLS	ACE	VT1	VT0	FD1	FD0	DFT	HFT	
1 0								+27 dB into LH Path (*) +9dB into LH Path
	1 0							Anticlipping ON (*) Anticlipping OFF
		0 0 1 1	0 1 0 1					(*) -15dm0 Anticlipping Threshold -13dm0 Anticlipping Threshold -9dm0 Anticlipping Threshold -7dm0 Anticlipping Threshold
				0 0 1 1	0 1 0 1			(*) 256ms Gain Recovery Time Constant / (4Hz) 128ms Gain recovery Time Constant / (8Hz) 32ms Gain Recovery Time Constant / (31Hz) 16ms Gain Recovery Time Constant / (62Hz)
						0 0 1 1	0 1 0 1	(*) Standard Frequency Tone Range Halved Frequency Tone Range Doubled Frequency Tone Range Forbidden

(*) Default values inserted into the Register at Power On

CONTROL REGISTER CR0
First byte of a READ or a WRITE instruction to Control Register CR0 is as shown in TABLE 1. Second byte is as shown in TABLE 2.

Master Clock Frequency Selection
A master clock must be provided to PIAFE for operation of filter and coding/decoding functions.
In COMBO I/II mode, MCLK frequency can be either 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz.
Bit F1 (7) and F0 (6) must be set during initialization to select the correct internal divider.
In GCI mode, MCLK must be either 1.536MHz or 2.048MHz.
512KHz and 2.56MHz are not allowed.
Default value is 1.536 MHz for both modes.
Any clock different from the default one must be selected prior a Power-Up instruction for both modes.

Coding Law Selection
Bits MA (5) and IA (4) permit selection of Mu-255 law or A law coding with or without even bit inversion.
After power on initialization, the Mu-255 law is selected.

	Mu 255 law								True A law even bit inversion								A law without even bit inversion							
	msb							lsb	msb							lsb	msb							lsb
Vin = + full scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1
Vin = 0 V	1 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 0	1 1	0 0	1 1	0 0	1 1	0 0	1 1	1 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
Vin = - full scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1	1

MSB is always the first PCM bit shifted in or out of PIAFE.

Digital Interface timing
Bit DN=0 (3) selects digital interface in delayed timing mode while DN=1 selects non delayed data timing.
In GCI mode, bit DN is not significant.
After reset and if COMBO I/II mode is selected, delayed data timing is selected.

Digital Interface format
Bit FF=0 (2) selects digital interface in Format 1 where B1 and B2 channel are consecutive. FF=1 selects Format 2 where B1 and B2 channel are separated by two bits. (see digital interface format section).
In GCI mode, bit FF is not significant.

56+8 selection
Bit 'B7' (1) selects capability for PIAFE to take into account only the seven most significant bits of the PCM data byte selected.
When 'B7' is set, the LSB bit on D_R is ignored and LSB bit on D_X is high impedance. This function allows connection of an external "in band" data generator directly connected on the Digital Interface.

Digital loopback
Digital loopback mode is entered by setting DL bit(0) equal 1.
In Digital Loopback mode, data written into Receive PCM Data Register from the selected received time-slot is read-back from that Register in the selected transmit time-slot on D_X. Time slot is selected with Register CR1.
No PCM decoding or encoding takes place in this mode. Transmit and Receive amplifier stages are muted.

CONTROL REGISTER CR1
First byte of a READ or a WRITE instruction to Control Register CR1 is as shown in TABLE 1. Second byte is as shown in TABLE 3.

Hands-free I/Os selection
Bit HFE set to one enables HFI, HFO pins for connection of an external handfree circuit such as TEA 7540. HFO is an analog output that provides the receive voice signal. 0 dBMO level on that output is 0.491 Vrms ($1.4V_{pp}$). HFI is an analog high impedance input (10 KΩ typ.) intended to send back the processed receive signal to the Loudspeaker. 0 dBMO level on that input is 0.491Vrms.

Anti-larsen selection
Bit ALE set to one enables on-chip antilarsen and squelch effect system.

Latch output control
Bit DO controls directly logical status of latch output LO: ie, a "ZERO" written in bit DO puts output LO in high impedance, a "ONE" written in bit DO sets output LO to zero.

Microwire access to B channel on receive path
Bit MR (4) selects access from MICROWIRE Register CR2 to Receive path. When bit MR is set high, data written to register CR2 is decoded each frame, sent to the receive path and data input at D_R is ignored.
In the other direction, current PCM data input received at D_R can be read from register CR2 each frame.

Microwire access to B channel on transmit path
Bit MX (3) selects access from MICROWIRE write only Register CR3 to D_X output. When bit MX is set high, data written to CR3 is output at D_X every frame and the output of PCM encoder is ignored.

B channel selection
Bit 'EN' (2) enables or disables voice data transfer on D_X and D_R pins. When disabled, PCM data from DR is not decoded and PCM time-slots are high impedance on D_X.
In GCI mode, bits 'T1' (1) and 'T0' (0) select one of the four channels of the GCI interface.
In COMBO I/II mode, only B1 or B2 channel can be selected according to the interface format selected. Bit 'T1' is ignored.

CONTROL REGISTER CR2
Data sent to receive path or data received from D_R input. Refer to bit MR(4) in "Control Register CR1" paragraph.

CONTROL REGISTER CR3
D_X data transmitted. Refer to bit MX(3) in "Control Rgister CR1" paragraph.

CONTROL REGISTER CR4
First byte of a READ or a WRITE instruction to Control Register CR4 is as shown in TABLE 1. Second byte is as shown in TABLE 6.

Transmit Input Selection
MIC1 or MIC2 source is selected with bit VS (7).
Transmit input selected can be enabled or muted with bit TE (6).
Transmit gain can be adjusted within a 15 dB range in 1 dB step with Register CR5.

Sidetone select
Bit "SI" (5) enables or disables Sidetone circuitry. When enabled, sidetone gain can be adjusted with Register (CR5). When Transmit path is disabled, bit TE set low, sidetone circuit is also disabled.

External Auxiliary signal select
Bit "EE" (4) set to one connects EAIN input to the loudspeaker amplifier input.

Ring/Tone signal routing
Bits "RTL" (3) and RTE (2) provide select capability to connect on-chip Ring/Tone generator either to loudspeaker amplifier input or to earpiece amplifier input or both.

PCM receive data routing
Bits "SL" (1) and "SE" (0) provide select capability to connect received speech signal either to Loudspeaker amplifier input or to earpiece amplifier input or both.

CONTROL REGISTER CR5
First byte of a READ or a WRITE instuction to Control Register CR5 is as shown in TABLE 1. Second byte is as shown in TABLE 7.

Transmit gain selection
Transmit amplifier can be programmed for a gain from 0dB to 15dB in 1dB step with bits 4 to 7.
0 dBmO level at the output of the transmit amplifier (A reference point) is 0.739 Vrms (overload voltage is 1.06 Vrms).

Sidetone attenuation selection
Transmit signal picked up after the switched capacitor low pass filter may be fed back into the Receive Earpiece amplifier.
Attenuation of the signal at the output of the sidetone attenuator can be programmed from –8dB to –23dB relative to reference point A in 1 dB step with bits 0 to 3.

CONTROL REGISTER CR6
First byte of a READ or a WRITE instruction to Control Register CR6 is as shown in TABLE 1. Second byte is as shown in TABLE 8.

Earpiece amplifier gain selection:
Earpiece Receive gain can be programmed in 1 dB step from 0 dB to -15 dB relative to the maximum with bits 4 to 7.
0 dBmO voltage at the output of the amplifier on pins V_{Fr+} and V_{Fr-} is then 824.5 mVrms when 0dB gain is selected down to 146.6 mVrms when –15 dB gain is selected.

Loudspeaker amplifier gain selection:
Loudspeaker Receive amplifier gain can be programmed in 2 dB step from 0 dB to -30 dB relative to the maximum with bits 0 to 3.
0 dBmO voltage on the output of the amplifier on pins LS+ and LS- on 50 Ω is then 1.384 Vrms ($3.91V_{pp}$) when 0 dB gain is selected down to 43.7 mVrms ($123.6mV_{pp}$) when -30 dB gain is selected.

Current limitation is approximatively 150 mApk.

CONTROL REGISTER CR7:
First byte of a READ or a WRITE instruction to Control Register CR7 is as shown in TABLE 1. Second byte is as shown in TABLE 9.

Tone/Ring amplifier gain selection
Output level of Ring/Tone generator, before attenuation by programmable attenuator is 2.4 Vpk-pk when f1 generator is selected alone or summed with the f2 generator and 1.9 Vpk-pk when f2 generator is selected alone.
Selected output level can be attenuated down to -27 dB by programmable attenutator by setting bits 4 to 7.

Frequency mode selection
Bits 'F1' (3) and 'F2' (2) permit selection of f1 and/or f2 frequency generator according to TABLE 9.
When f1 (or f2) is selected, output of the Ring/Tone is a squarewave (or a sinewave) signal at the frequency selected in the CR8 (or CR9) Register.
When f1 and f2 are selected in summed mode, output of the Ring/Tone generator is a signal where f1 and f2 frequency are summed.
In order to meet DTMF specifications, f2 output level is attenuated by 2dB relative to the f1 output level.
Frequency temporization must be controlled by the microcontroller.
Any switching between two frequencies of the same channel (f1 or f2) is done maintaining practically the phase continuity.
The actual change in the frequency of the tone generator takes place within 1/16th of the period of the highest of the two frequencies that are switched between, plus 2µs for internal data acquisition.

Waveform selection
Bit 'SN' (1) selects waveform of the output of the Ring/Tone generator. Sinewave or squarewave signal can be selected.

DTMF selection
Bit DE (0) permits connection of Ring/Tone/DTMF generator on the Transmit Data path instead of the Transmit Amplifier output. Earpiece feed-back may be provided by sidetone circuitry by setting bit SI or directly by setting bit RTE in Register CR4. Loudspeaker feed-back may be provided directly by setting bit RTL in Register CR4.

CONTROL REGISTERS CR8 AND CR9
First byte of a READ or a WRITE instruction to Control Register CR8 or CR9 is as shown in TABLE 1. Second byte is respectively as shown in TABLE 10 and 11.
Tone or Ring signal frequency value is defined by the formula:
f1 = CR8 / 0.128 Hz and f2 = CR9 / 0.128 Hz
(with DFT = HFT = 0 in CR10)
where CR8 and CR9 are decimal equivalents of the binary values of the CR8 and CR9 registers respectively. Thus, any frequency between 7.8 Hz and 1992 Hz may be selected in 7.8 Hz step.
TABLE 13 gives examples for the main frequencies usual for Tone or Ring generation.

CONTROL REGISTER CR10
First byte of a READ or a WRITE instruction to control register CR10 is as shown in TABLE 1. Second byte is as shown in Table 12.

Extra +18dB in LS Gain
GLS = 1 sets extra 18dB Gain (total Gain = 27dB)
GLS = 0 sets standard Gain = 9dB like on ST5080

Anticlipping enable, thresholds and time constants
ACE = 1 enables the operation of the Digital anticlipping section (D.A.S.), needed to avoid distortion on sine wave when GLS = 1 (extra 18dB on LS) anticlipping thresholds of -15, -13, -9 and -7dBmo are defined by bits 4 and 5 (VT1/VT0).
Gain recovery the constants (anticlipping release) are selectable among four values, 256ms, 128ms, 32ms and 16ms by bits 2 and 3 (FD1/FD0).

Doubled Tone/Ringer Frequency Range
Double frequency range on tone & ringer generator is obtained by putting DFT = 1 (and HFT = 0).
Formula for frequency generator is:
f1 = CR8/0.064Hz and f2 = CR9/0.064Hz.
Maximum frequency is 3984.4Hz and frequency accuracy is 15.6Hz.

Halved Tone/Ringer Frequency Range
Halved frequency and double accuracy on tone & ringer generator is obtained bu putting HFT = 1 (and DFT = 0).
Formula for frequency generator is:
f1 = CR8/0.256Hz and f1 = CR9/0.256Hz
Frequency range is from 3.9Hz to 996.1Hz and step is 3.9Hz with improved accuracy for low frequencies combination.
HFT = DFT= 1 is a forbidden combination.

Table 13: Examples of Usual Frequency Selection (DFT = HFT = 0 in CR10)

Description	f1 value (decimal)	Theoric value (Hz)	Typical value (Hz)	Error %
Tone 250 Hz	32	250	250	.00
Tone 330 Hz	42	330	328.2	−.56
Tone 425 Hz	54	425	421.9	−.73
Tone 440 Hz	56	440	437.5	−.56
Tone 800 Hz	102	800	796 9	−.39
Tone 1330 Hz	170	1330	1328 1	−.14
DTMF 697 Hz	89	697	695.3	−.24
DTMF 770 Hz	99	770	773.4	+.44
DTMF 852 Hz	109	852	851.6	−.05
DTMF 941 Hz	120	941	937.5	−.37
DTMF 1209 Hz	155	1209	1210.9	+.16
DTMF 1336 Hz	171	1336	1335.9	− 01
DTMF 1477 Hz	189	1477	1476.6	.00
DTMF 1633 Hz	209	1633	1632.8	.00
SOL	50	392	390.6	−.30
LA	56	440	437.5	−.56
SI	63	494	492.2	−.34
DO	67	523.25	523.5	+.04
RE	75	587.33	586.0	−.23
MI flat	80	622.25	625.0	+.45
MI	84	659.25	656.3	−.45
FA	89	698.5	695.3	−.45
FA sharp	95	740	742.2	+.30
SOL	100	784	781.3	−.34
SOL sharp	106	830.6	828.2	−.29
LA	113	880	882.9	+.33
SI	126	987.8	984.4	−.34
DO	134	1046.5	1046.9	+.04
RE	150	1174.66	1171.9	−.23
MI	169	1318.5	1320.4	+.14

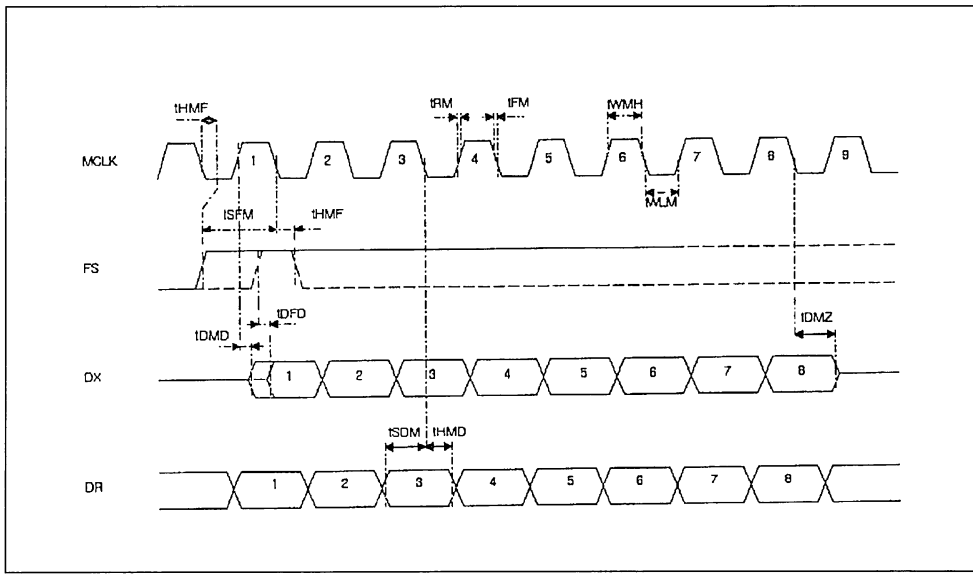
POWER SUPPLIES

While pins of PIAFE device are well protected against electrical misuse, it is recommended that the standard CMOS practise of applying GND before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

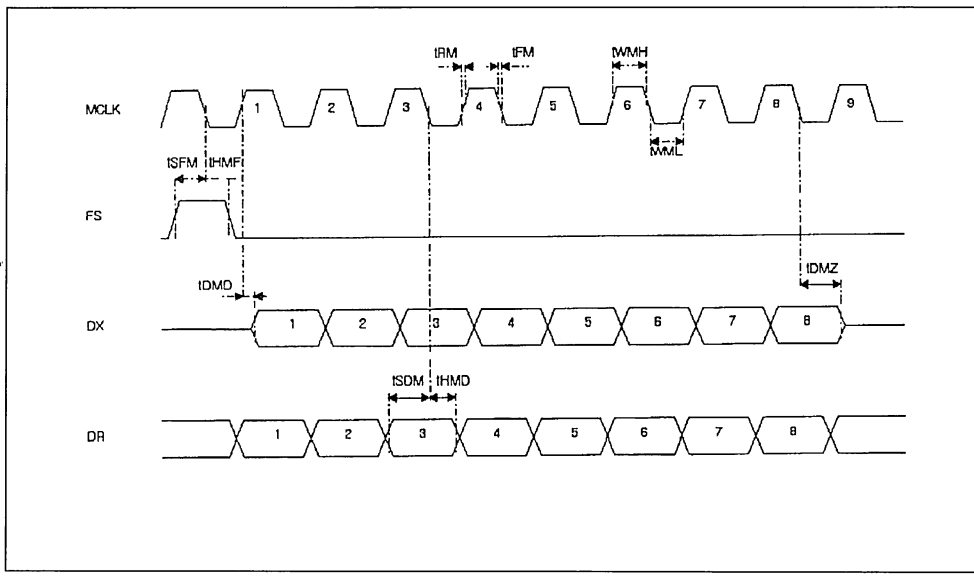
To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A power supply decoupling capacitor of 0.1 µF should be connected from this common point to V_{CC} as close as possible to the device pins.

TIMING DIAGRAM

Non Delayed Data Timing Mode

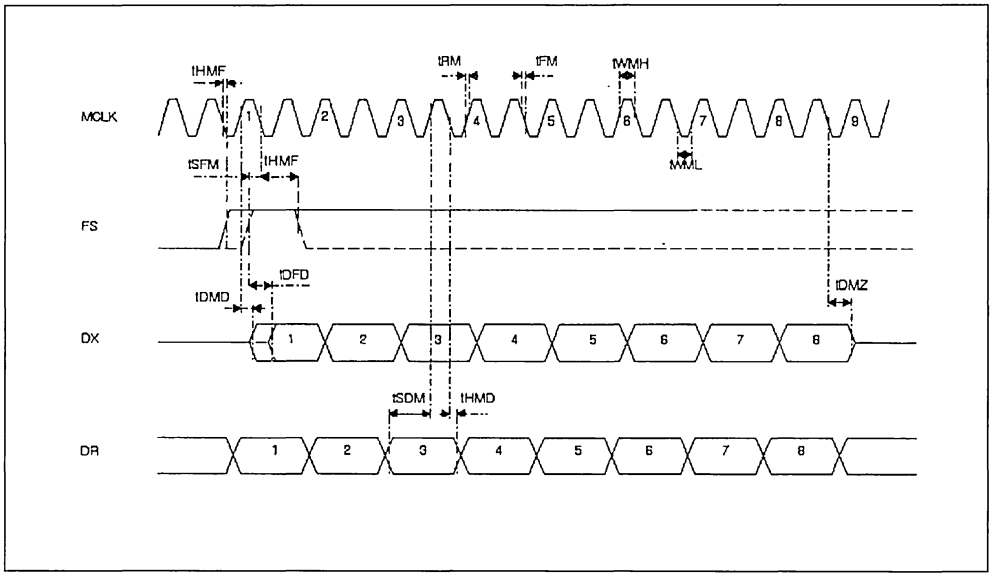


Delayed Data Timing Mode

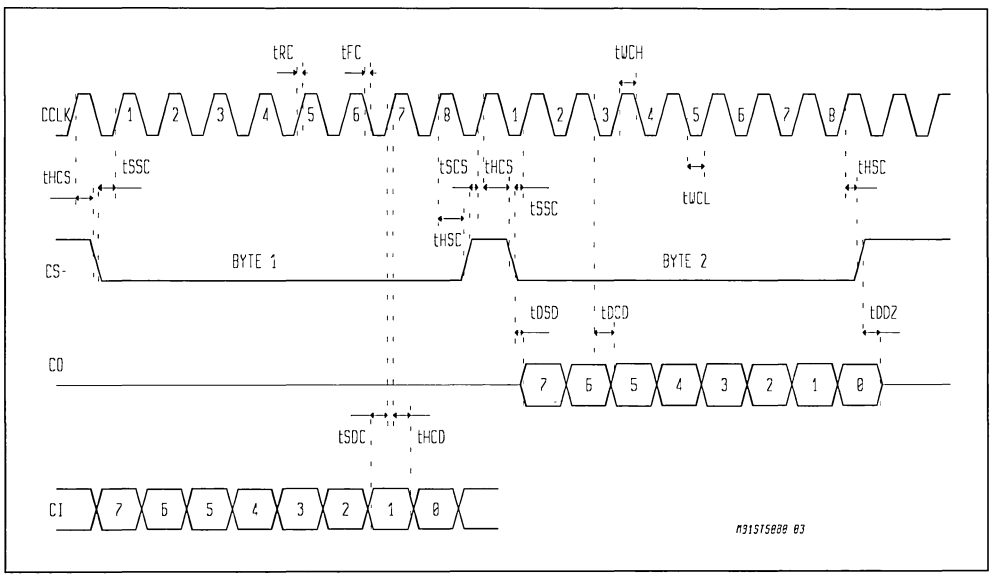


TIMING DIAGRAM (continued)

GCI Timing Mode



Serial Control Timing (MICROWIRE MODE)



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
V_{CC} to GND	7	V
Current at V_{MIC} ($V_{CC} \leq 5.5V$)	± 50	mA
Current at V_{RxO} and LS	± 100	mA
Voltage at any digital input ($V_{CC} \leq 5.5V$); limited at ±50mA	V_{CC} + 1 to GND - 1	V
Current at any digital output	± 50	mA
Storage temperature range	- 65 to + 150	°C
Lead Temperature (wave soldering, 10s)	+ 260	°C

TIMING SPECIFICATIONS (unless otherwise specified, V_{CC} = 5V ± 10%, T_A = –5°C to 70°C ; typical characteristics are specified V_{CC} = 5V, T_A = 25 °C; all signals are referenced to GND, see Note 5 for timing definitions)

MASTER CLOCK TIMING

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{MCLK}	Frequency of MCLK	Selection of frequency is programmable (see table 2)		512 1.536 2.048 2.560		kHz MHz MHz MHz
t_{WMH}	Period of MCLK high	Measured from V_{IH} to V_{IH}	80			ns
t_{WML}	Period of MCLK low	Measured from V_{IL} to V_{IL}	80			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			30	ns

PCM INTERFACE TIMING (COMBO I / II and GCI modes)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{HMF}	Hold Time MCLK low to FS low		10			ns
t_{SFM}	Setup Time, FS high to MCLK low		30			ns
t_{DMD}	Delay Time, MCLK high to data valid	Load = 100 pF			100	ns
t_{DMZ}	Delay Time, MCLK low to DX disabled		15		100	ns
t_{DFD}	Delay Time, FS high to data valid	Load = 100 pF ; Applies only if FS rises later than MCLK rising edge in Non Delayed Mode only			100	ns
t_{SDM}	Setup Time, D_R valid to MCLK receive edge		20			ns
t_{HMD}	Hold Time, MCLK low to D_R invalid		20			ns

SERIAL CONTROL PORT TIMING (Usual COMBO I / II mode only)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{CCLK}	Frequency of CCLK				2.048	MHz
t_{WCH}	Period of CCLK high	Measured from V_{IH} to V_{IH}	160			ns
t_{WCL}	Period of CCLK low	Measured from V_{IL} to V_{IL}	160			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			50	ns
t_{HCS}	Hold Time, CCLK high to CS– low		10			ns
t_{SSC}	Setup Time, CS– low to CCLK high		50			ns
t_{SDC}	Setup Time, CI valid to CCLK high		50			ns
t_{HCD}	Hold Time, CCLK high to CI invalid		50			ns
t_{DCD}	Delay Time, CCLK low to CO data valid	Load = 100 pF , plus 1 LSTTL load			80	ns
t_{DSD}	Delay Time, CS–low to CO data valid				50	ns
t_{DDZ}	Delay Time CS–high or 8th CCLK low to CO high impedance whichever comes first		15		80	ns
t_{HSC}	Hold Time, 8th CCLK high to CS– high		100			ns
t_{SCS}	Set up Time, CS– high to CCLK high		100			ns

Note 5: A signal is valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH}.
For the purpoes of this specification the following conditions apply:
a) All input signal are defined as V_{IL} = 0.4V, V_{IH} = 2.7V, t_R < 10ns, t_F < 10ns.
b) Delay times are measured from the inputs signal valid to the output signal valid.
c) Setup times are measured from the data input valid to the clock input invalid
d) Hold times are measured from the clock signal valid to the data input invalid.

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CC} = 5V ± 10%, T_A = –5°C to 70°C ; typical characteristic are specified at V_{CC} = 5V, T_A = 25°C ; all signals are referenced to GND)

DIGITAL INTERFACES

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All digital inputs except pin AT	DC			0.7	V
			AC			0.4	V
V_{IH}	Input High Voltage	All digital inputs except pin AT	DC	2.0			V
			AC	2.7			V
V_{IL}	Input Low Voltage	Input AT				0.5	V
V_{IH}	Input High Voltage	Input AT		VCC -0.5V			V
V_{OL}	Output Low Voltage	D_X,I_L = -2.0mA; all other digital outputs, I_L = –1mA	DC			0.4	V
			AC			0.7	V
V_{OH}	Output High Voltage	D_X,I_L = 2.0mA; all other digital outputs, I_L = 1mA	DC	2.4			V
			AC	2.0			V
I_{IL}	Input Low Current	Any digital input, GND < V_{IN} < V_{IL}		-10		10	µA
I_{IH}	Input High Current	Any digital input, V_{IH} < V_{IN} < V_{CC}		-10		10	µA
I_{OZ}	Output Current in High impedance (Tri-state)	D_X and CO		-10		10	µA

ANALOG INTERFACES

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{MIC}	Input Leakage	GND < V_{MIC} < V_{CC}	-100		+100	µA
R_{MIC}	Input Resistance	GND < V_{MIC} < V_{CC}	50			kΩ
R_{LVFr}	Load Resistance	V_{Fr+} to V_{Fr-}	100			Ω
C_{LVFr}	Load Capacitance	V_{Fr+} to V_{Fr-}			150	nF
R_{OVFr0}	Output Resistance	Steady zero PCM code applied to DR; I = ± 1mA		1.0		Ω
V_{OSVFr0}	Differential offset: Voltage at V_{Fr+}, V_{Fr-}	Alternating ± zero PCM code applied to DR maximum receive gain; R_L = 100Ω	-100		+100	mV
R_{LLS}	Load Resistance	L_{S+} to L_{S-}		50		Ω
C_{LLS}	Load Capacitance	L_{S+} to L_{S-}			600	nF
R_{OLS}	Output Resistance	Steady zero PCM code applied to DR; I ± 1mA		1		Ω
V_{OSLS}	Differential offset Voltage at L_{S+}, L_{S-}	Alternating ± zero PCM code applied to DR maximum receive gain; R_L = 50Ω	–100		+100	mV
R_{LTRO}	Load Resistance at TRO	TRO to GND	600			Ω

POWER DISSIPATION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC0}	Power down Current	CCLK,CI = 0.4V; CS = 2.4V (µwire only) All other inputs active GCI mode only:		0 2 0.2	0 5 0.5	mA mA
I_{CC1}	Power Up Current	L_{S+}, L_{S-} and V_{Fr+}, V_{Fr-} not loaded		12.0	17.0	mA

TRANSMISSION CHARACTERISTICS (unless otherwise specified, V_{CC} = 5V ± 10%, T_A = –5°C to 70°C; typical characteristics are specified at V_{CC} = 5V, T_A = 25°C, MIC1/2 = 0dB_{m0}, D_R = 0dB_{m0} PCM code, f = 1015.625 Hz; all signal are referenced to GND)

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Transmit path - Absolute levels at MIC1 / MIC2

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Transmit Amps connected for 0dB gain		73.9		mV_{RMS}
Overload level	A law selected		106.08		mV_{RMS}
Overload level	mu law selected		106.47		mV_{RMS}
0 dBM0 level	Transmit Amps connected for 15dB gain		13.14		mV_{RMS}
Overload level	A law selected		18.86		mV_{RMS}
Overload level	mu law selected		18.93		mV_{RMS}

TRANSMISSION CHARACTERISTICS (continued)

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Receive path - Absolute levels at V_{FR} (Differentially measured)

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Receive Amp programmed for 0dB gain		824.5		mV_{RMS}
0 dBM0 level	Receive Amp programmed for - 15dB attenuation		146.6		mV_{RMS}

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Receive path - Absolute levels at L_S (Differentially measured)

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Receive Amp programmed for 0dB gain		1.384		V_{RMS}
0 dBM0 level	Receive Amp programmed for - 30dB gain		43.7		mV_{RMS}

AMPLITUDE RESPONSE
Transmit path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for maximum. Measure deviation of Digital PCM Code from ideal $0dB_{m0}$ PCM code at D_X	-0.30		0.30	dB
G_{XAG}	Transmit Gain Variation with programmed gain	Measure Transmit Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GXA, i.e. $G_{AXG} = G_{actual} - G_{prog} - G_{XA}$	-0.5		0.5	dB
G_{XAT}	Transmit Gain Variation with temperature	Measured relative to G_{XA}. min. gain < G_X < Max. gain	-0.1		0.1	dB
G_{XAV}	Transmit Gain Variation with supply	Measured relative to G_{XA} G_X = Maximum gain	-0.1		0.1	dB
G_{XAF}	Transmit Gain Variation with frequency	Relative to 1015,625 Hz, multitone test technique used. min. gain < G_X < Max. gain f = 60 Hz f = 200 Hz f = 300 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz to 5000 Hz f = 5000 Hz and up	 -1.5 -0.3 -0.8		 -26 -0.1 0.3 0.0 -14 -32 -40	 dB dB dB dB dB dB dB
G_{XAL}	Transmit Gain Variation with signal level	Sinusoidal Test method. Reference Level = $-10\ dB_{m0}$ V_{MIC} = $-40\ dB_{m0}$ to $+3\ dB_{m0}$ V_{MIC} = $-50\ dB_{m0}$ to $-40\ dB_{m0}$ V_{MIC} = $-55\ dB_{m0}$ to $-50\ dB_{m0}$	 -0.25 -0.5 -1.5		 0.25 0.5 1.5	 dB dB dB

AMPLITUDE RESPONSE

Receive path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{RAE}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply 0 dB_{m0} PCM code to D_R Measure $V_{Fr\pm}$	-0.3		0.3	dB
G_{RAL}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply 0 dB_{m0} PCM code to D_R Measure $L_{S\pm}$	-0.6		0.6	dB
G_{RAGE}	Receive Gain Variation with programmed gain	Measure Earpiece Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GRAE, i.e. $G_{RAGE} = G_{actual} - G_{prog} - G_{RAE}$	-0.5		0.5	dB
G_{RAGL}	Receive Gain Variation with programmed gain	Measure Loudspeaker Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GRAL, i.e. $G_{RAGL} = G_{actual} - G_{prog} - G_{RAL}$	-1.0		1.0	dB
G_{RAT}	Receive Gain Variation with temperature	Measured relative to GRA. (LS and V_{Fr}) G_R = Maximum Gain	-0.1		0.1	dB
G_{RAV}	Receive Gain Variation with Supply	Measured relative to GRA. (LS and V_{Fr}) G_R = Maximum Gain	-0.1		0.1	dB
G_{RAF}	Receive Gain Variation with frequency (Earpiece or Loudspeaker)	Relative to 1015,625 Hz, multitone test technique used. min. gain < G_R < Max. gain f = 200 Hz f = 300 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz	 -0.3 -0.3 -0.8		 0.3 0.3 0.0 -14	 dB dB dB dB
$G_{RAL\,E}$	Receive Gain Variation with signal level (Earpiece)	Sinusoidal Test Method Reference Level = –10 $dBm0$ D_R = 0 dBm0 to +3 dBm0 D_R = -40 dBm0 to 0 dBm0 D_R = -50 dBm0 to -40 dBm0 D_R = -55 dBm0 to -50 dBm0	 -0.25 -0.25 -0.5 -1.5		 0.25 0.25 0.5 1.5	 dB dB dB dB
$G_{RAL\,L}$	Receive Gain Variation with signal level (Loudspeaker)	Sinusoidal Test Method Reference Level = –10 $dBm0$ D_R = 0 dBm0 to +3 dBm0 D_R = -40 dBm0 to 0 dBm0 D_R = -50 dBm0 to -40 dBm0 D_R = -55 dBm0 to -50 dBm0	 -0.25 -0.25 -0,5 -1.5		 0.25 0.25 0.5 1.5	 dB dB dB dB

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DXA	Tx Delay, Absolute	f = 1000 Hz		320	340	µs
DXR	Tx Delay, Relative	f = 500 - 600 Hz		225	245	µs
		f = 600 - 800 Hz		125	145	µs
		f = 800 - 1000 Hz		50	70	µs
		f = 1000 - 1600 Hz		20	40	µs
		f = 1600 - 2600 Hz		55	75	µs
		f = 2600 - 2800 Hz		80	100	µs
		f = 2800 - 3000 Hz		130	150	µs
DRA	Rx Delay, Absolute	f = 1600 Hz		252	270	µs
DRR	Rx Delay, Relative	f = 500 - 1000 Hz		10	30	µs
		f = 1000 - 1600 Hz		30	50	µs
		f = 1600 - 2600 Hz		105	125	µs
		f = 2600 - 2800 Hz		135	155	µs
		f = 2800 - 3000 Hz		185	205	µs

NOISE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NXC	Tx Noise, C weighted	V_{MIC} = 0V			16	dBrnC0
NXP	Tx Noise, P weighted	V_{MIC} = 0V			-70	dBm0p
NREC	Rx Noise, C weighted (Earpiece)	Receive PCM code = Alternating Positive and Negative code			18	dBrnC0
NREP	Rx Noise, P weighted (Earpiece)	Receive PCM code = Positive Zero			-70	dBm0p
NRLC	Rx Noise, C weighted (Loudspeaker)	Receive PCM code = Alternating Positive and Negative code			21	dBrnC0
NRLP	Rx Noise, P weighted (Loudspeaker)	Receive PCM code = Positive Zero			-67	dBm0p
NRS	Noise, Single Frequency	V_{MIC} = 0V, Loop-around measurament from f = 0 Hz to 100 kHz			-50	dBm0
NTRO	Recorder Noise, Pweighted	V_{MIC} = 0V Receive PCM code = Positive Zero			-60	dBmp
PPSRx	Positive PSRR, Tx	V_{MIC} = 0V, V_{CC} = 5.0 V_{DC} + 100 mV_{rms}; f = 0Hz to 50KHz	30			dB
PPSRp	Positive PSRR, Rx	PCM Code equals Positive Zero, V_{CC} = 5.0 VDC + 100 mVrms, measure $V_{Fr\pm}$	30			dB
		f = 0 Hz - 4 kHz	30			dB
		f = 4 kHz - 50 kHz	30			dB
SOS	Spurious Out-Band signal at the output	DR input set to 0 dBm0 PCM code 300 - 3400 Hz Input PCM Code applied at DR				
		4600 Hz - 5600 Hz			-40	dB
		5600 Hz - 7600 Hz			-50	dB
		7600 Hz - 8400 Hz			-50	dB
		8400 Hz - 100 kHz			-50	dB

DISTORTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
S_{TDx} S_{TDr}	Signal to Total Distortion	Sinusoidal Test Methode (measured using C message weighting Filter) Level = 0 dBm0 to - 30 dBm0 Level = - 40 dBm0 Level = - 45 dBm0	 36 29 24			 dBC dBC dBC
S_{DFx}	Single Frequency Distortion transmit	0 dBm0 input signal			-46	dB
S_{DFr}	Single Frequency Distortion receive	0 dBm0 input signal			-46	dB
IMD	Intermodulation	Loop-around measurament Voltage at V_{MIC} = -4 dBm0 to -21 dBm0, 2 Frequencies in the range 300 - 3400 Hz			-41	dB

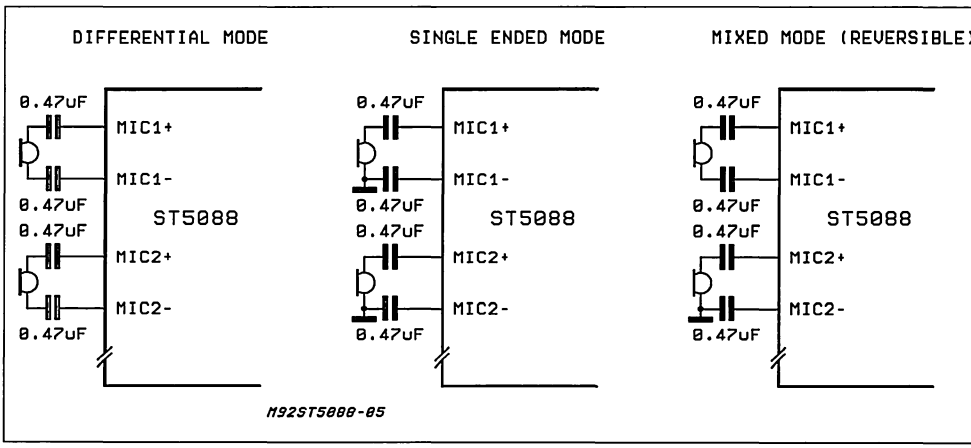
CROSSTALK

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
C_{Tx-r}	Transmit to Receive	Transmit Level = 0 dBm0, f = 300 - 3400 Hz DR = QuietPCM Code			-65	dB
C_{Tr-x}	Receive to Transmit	Receive Level = 0 dBm0, f = 300 - 3400 Hz; V_{MIC} = 0V			-65	dB

TAPE RECORDER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$G_{TRO\,RX}$	Receive TRO Output	DR = 0dBm0	220	245	275	mV_{RMS}
$G_{TRO\,TX}$	Transmit TRO Output	DX = 0dBm0	220	246	275	mVRMS

APPLICATION NOTE FOR MICROPHONE CONNECTIONS

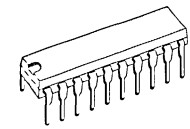


The 4 connection modes (since the MIXED MODE is symmetrical with respect to MIC1 and MIC2) allow one microphone at a time to be selected via the V_S bit (bit 7 of Control Register CR4).

SID-GCI : S/T INTERFACE DEVICE WITH GCI

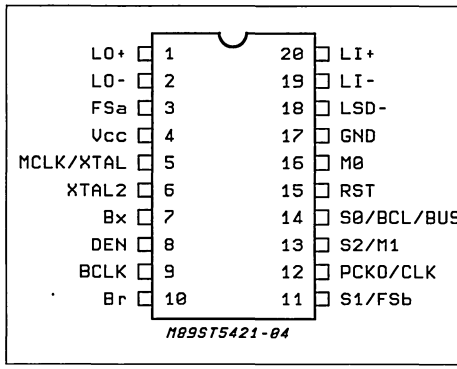
ADVANCE DATA

- SINGLE CHIP 4 WIRES 192kb/s TRANSCEIVER FULLY COMPLYING WITH CCITT I.430
- ISDN BASIC ACCESS HANDLING 144kb/s 2B + D TRANSMISSION
- GCI COMPATIBLE INTERCHIP INTERFACE
- EXCEEDS I.430 RANGE : AT LEAST 1.5KM POINT-TO-POINT AND 200M POINT-TO-MULTIPOINT
- ADAPTIVE AND FIXED TIMING OPTIONS FOR NT
- CLOCK RESYNCHRONIZER AND DATA BUFFERS FOR NT2
- PROGRAMMABLE S1 AND Q CHANNELS HANDLING ACCORDING TO US ANSI STANDARD FOR LAYER 1 MAINTENANCE
- EASILY INTERFACEABLE WITH ST5451 HDLC & GCI CONTROLLER AND ANY OTHER GCI COMPATIBLE DEVICE



DIP20

PIN CONNECTION



DESCRIPTION

The ST5421 (SID-GCI) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is bullt on SGS-THOMSON HCMOS 3A double metal advanced process, and requires only a single + 5V supply. All functions specified in CCITT reccommendation I.430 for ISDN basic access at the 'S' and 'T' interfaces are provided, and the device can be configured to operate either in TE (Terminal Equipment), in NT1 or NT2 (Network Termination) or in PABX line-card device.

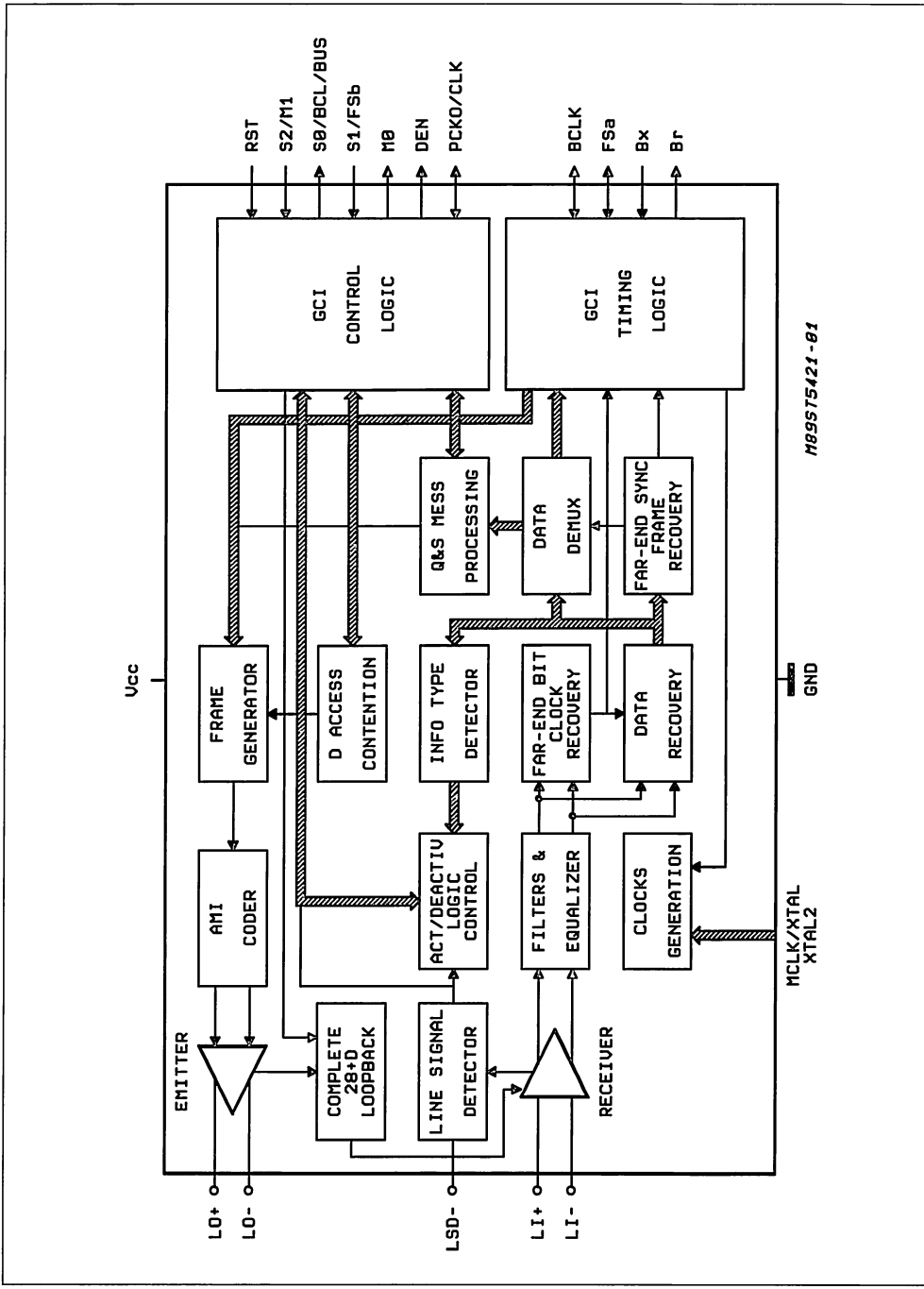
GCI interchip interface highly enhances device connection effiency by multiplexing controls and data on the same bus and requiring only 4 pins. ST5421 implements all the GCI standard functions for Monitor and Control/Indicate channels, supporting up to 8 GCI peripherals in multiplexed mode.

As specified in I.430, full-duplex transmission at 192kb/s is provided on separate transmit and receive twisted wire pairs using inverted Alternate Mark Inversion (AMI) line coding. Various channels are combined to form the 192kb/s aggregate rate, including 2 'B' channels, each of 64kb/s, and 1 'D' channel at 16kb/s. In addition, multiframe transmission is provided in a switchable processing mode based on United State ANSI standard for Layer 1 maintenance. 800 bit/s message oriented data transmission is supported by S1 and Q channels.

All I.430 wiring configurations are supported by ST5421 including passive bus for TE's distributed within 200 meters, and point-to-point and point-to-multipoint extended up to at least 1500 meters (24 AWG cables). Adaptive receive signal processing enables the device to operate with low bit error rate on any of the standard types of cable pairs commonly found in premise wiring installations when tested with the noise sources specified in I.430.

Far-end Clock Resynchronizer automatically selected, data buffer and slave-slave mode allow design of NT2 trunk-card connected to several T interfaces.

BLOCK DIAGRAM



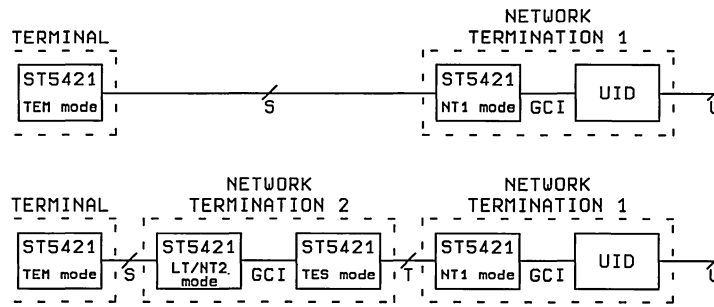
PIN DESCRIPTION

Name	Number	Description
GND	17	Ground Reference Voltage. all analog and digital signals are referenced to this pin.
V_{CC}	4	Positive Power Supply Input 5V (± 5%) relative to GND
MCLK/XTAL	5	Master Clock or Crystal Oscillator Input: this pin requires either a 15.36MHz crystal (parallel resonant with R_S < 100 Ω) to be tied between this pin and XTAL2 or a logic CMOS level 15.36MHz clock from a stable source. When using a crystal, a total of 33pF load capacitance to GND must also be connected. In NT configurations. MCLK clock input doesn't need to be synchronous with the Network Reference Clock (FSa).
XTAL2	6	Crystal Oscillator Output. This pin should be connected to one end of the 15.36MHz crystal, otherwise is not connected.
BCLK	9	Bit Clock: this signal determines the data shift rate at GCI. Data is shifted-in on Bx and shifted-out on Br at half the BCLK frequency. When NT/TES mode is selected. BCLK is an input which does not need to be synchronous with the Master Clock input (MCLK). When TEM is selected, BCLK is an output at frequency of 1536kHz. This clock is phase locked to the receive line signal and synchronous with FSa output.
FSa	3	Frame Synchronization Clock: 8kHz clock which defines the start of the frame on the GCI slave (NT/TES) Fsa is an input used as a network reference clock for S/T line. In GCI master (TEM) is an output applicable as a validation strobe for the first B channel.
S1/FSb	11	S1 if M0 = 1; is GCI channel number selection. FSb if M0 = 0 and M1 = 0 (TEM): is a data strobe indicating the active slot for the second B channel on the GCI.
Bx	7	Digital Input for GCI Channels: data to be transmitted to S line is shifted-in at half the BCLK frequency on the 2nd falling edge.
Br	10	Digital Output for GCI Channel (OPENDRAIN): data is shifted-out at half the BCLK frequency on the transmit rising edges of BCLK. An external pull-up resistor is needed.
DEN	8	DEN in TEM mode: is an output, normally low, that pulses high to indicate the active time slot for D channel data at the Bx input. It is intended to be gated with BCLK to control the D channel shifting from a layer 2 device (i.e. ST5451) to ST5421 transmit buffer. Using ST5451 HDCL/GCI controller, no external circuitry is needed.

PIN DESCRIPTION (continued)

Name	Number	Description
PCK0/CLK	12	PCK0 IN TEM, LT/NT2, NT1 mode: 32 kHz clock output synchronized to GCI clocks. It is intended to synchronize DC/DC converter in TEM mode. CLK in TES mode: is a clock signal open drain output phased-locked to the receive S line signal and applicable as far-end clock reference. Its frequency is 1536kHz compatible with 768kbit/s GCI data rate. An external pull-up resistor is needed
M0	16	M0 = 0: GCI mode selection, Time slot Assigner is selected on GCI channel 0. M0 = 1. GCI in a multiplex mode; S0, S1, S2 pins define the GCI channel number allocated to ST5421. TES/NT2 selection is done with the configuration registers.
S2/M1	13	S2 if M0 = 1: GCI channel number selection. If M0 = 0; M1 = 0: TEM selected, M1 = 1: NT1 selected.
S0/BCL/BUS	14	S0 if M0 = 1; GCI channel number selection. BCL in TEM; bit clock output at 768kHz compatible with COMBO families ETC5054/57. BUS in NT1; S Bus Configuration Selection: low for fixed timing recovery and high for adaptive timing recovery.
RST	15	Reset Pin: must be low at Power On Reset; after, a high pulse on this pin reset ST5421 in a state depending on the other configuration pins.
LSD-	18	Line Signal Detect: open drain output, normally high impedance, pulling low when SID-GCI is powered down and an S line signal is detected. It is applicable to wake up a microprocessor from a low power idle mode LSD$^-$ output goes back to high impedance when ST5421 is powered up.
LO+, LO-	1,2	Transmit AMI signal differential outputs to the S/T line transformer, when used with an appropriate 2:1 step down transformer, the line signal conforms to the output pulse masks in CCITT I.430.
LI$^-$,LI$^+$	19,20	Receive AMI signal inputs from the S/T line transformer. They should be connected to an appropriate 1:2 or 1:1 transformer through a line coupling circuit to conform I 430 recommendation. LI$^-$ pin is also the internal voltage reference pin.

Table 1: Pin configurations



	TEM	LT/NT2(1)	TES (1)	NT1
M0	i=0	i=1	i=1	i=0
DEN	o=DEN			
S2/M1	i=M1=0	i=S2	i=S2	i=M1=1
S1/FSb	o=FSb	i=S1	i=S1	Not used
S0/BCL/BUS	o=BCL	i=S0	i=S0	i=BUS
PCK0/CLK	o=PCK0	o=PCK0	o=CLK	o=PCK0

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(1) differentiation between TES and LT/NT2 is done by register programming.
Default value after reset is LT/NT2 in adaptive timing recovery configuration.

FUNCTIONAL DESCRIPTION

POWER OF INITIALIZATION

Following initial application of power, SID-GCI enters the power down de-activated state.
RST input must be tied low during power-on.

After Power on reset, all the internal I.430 circuits including the master oscillator are inactive and in a low power state except for the line signal detection circuit.

After any period of activity a high pulse on RST reset completely SID-GCI.

Configuration mode programming of SID-GCI is done by means of pins polarization and register programming.

NT1 and TEM modes are defined only by means of 2 configuration pins M0, M1 at Power On Reset.

For NT2 and TES modes (M0=1), configuration has to be completed by means of a Control Instruction on Monitor channel prior a Power Up instruction.

POWER UP/DOWN CONTROL

When TEM configuration is selected, ST5421 provides GCI Clocks needed for control channel transfer. Power Up instruction is directly provided by pulling low the Bx data input. SID-GCI then reacts sending GCI clocks. LSD- output pin can be directly connected to Bx data input for providing an automatic Power up when far-end attempts to activate.
After a period of activity, Power down state is normally re-entered by C/I control code DC (1111) while ST5421 is sending C/I indication code DP (0000); then ST5421 send twice C/I indication code DI(1111) before to power down.
It is possible to force immediately power down state by using PDN (0001) C/I control code.

When NT1 configuration is selected, ST5421 is powered up directly by receiving GCI clocks on BCLK and FSa input from the "U" device. The only way to power down ST5421 is to stop BCLK or FSa clock signal inputs.
For example PDN (0001) C/I control code has no effect.

When NT2 or TES configuration is selected, SID-GCI is powered up by the PUP code (0000) on C/I Control Channel. After a period of activity, Power down state is normally reentred by C/I control code DC (1111) while ST5421 is sending C/I indication DI(1111).
It is possible to force immediately Power down state by using PDN (0001) C/I control code. In NT1, NT2 or TES mode, loss of GCI clocks automatically forces the power down state.

POWER UP/DOWN STATE

Following a period of activity in the power up state, power down state may be re-entered as described above. Configuration Registers remain in their current state. They can be changed by the GCI Monitor channel.

The power down transition disables analog and I.430 circuitry, stops the Crystal Oscillator and all the clocks internally generated. Line Signal Detector Circuit remains active allowing LSD-pin to pull low if a receive signal is detected.

Power up transition enables all analog and I.430 circuitry, starts the Crystal oscillator and reset the state machine to the de-activated state. It also inhibits LSD-output.

LINE CODING AND FRAME FORMAT

For both directions of transmission, Alternate Mark Inversion (AMI) coding with inverted binary is used, as illustrated in figure 1.

This coding rule requires that a binary ONE is represented by a 0 current high impedance output, whereas a binary ZERO is represented by a positive or negative-going 100% duty cycle pulse. Normally, binary ZEROs alternate in polarity to maintain a d.c. balanced line signal.

The frame format used in SID-GCI follows CCITT reccommendation in I.430 and illustrated in figure 2. Each complete frame consists of 48 bits, with a line bit rate of 192kbit/s, giving a frame repetition rate of 4kHz. A violation of the AMI coding rule is used to indicate a frame boundary, by using a 0+ bit followed by a 0- balance bit to indicate the start of a frame, and by forcing the first binary zero following the balance bit to be of the same polarity as the balance bit.

In the Network Termination (NT) to Terminal Equipment (TE) transmission direction, the frame contains in addition to the 2B+D basic access data, an echo channel, the E bit, which is used to retransmit the D bits that are received from the TE (s), and three extra channels: FA, M and S bit.

In the TE to NT direction, the frame contains in addition to the 2B + D data, an extra channel, the FA bit.

FA, M and S bits are used to set up a Q multiframe channel in the TE or NT direction, and a S1 multiframe channel from NT to TE. These 800bit/s message oriented channels are structured on the base of the United States ANSI standard specification for layer 1 maintenance.

Figure 1: Inverted AMI Line-coding Rule.

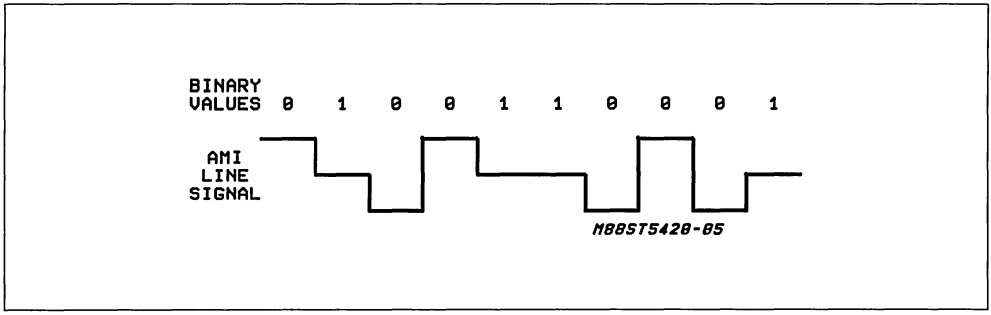
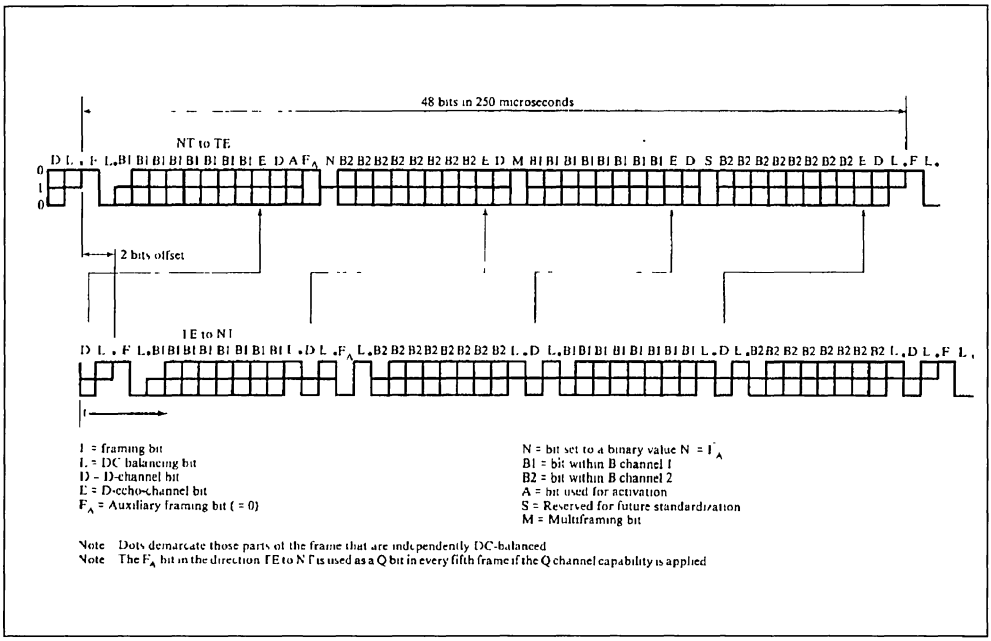


Figure 2: Frame Format



LINE TRANSMIT SECTION

The differential line driver outputs LO+ and LO- are designed to drive a suitable transformer with an external termination resistor. A 2:1 transformer, results in a signal amplitude of 750mV on the line which meets the I.430 pulse shape for all the loads specified.

When driving a binary 1 symbol, the output presents a high impedance in accordance with I.430. When driving a 0+ or 0- symbol, the voltage limited current source is turned on.

Short protection is included in the output stage.

Overvoltage protection is required externally.

Depending on TE or NT selected configuration, 192kbit/s data is transmitted on LO+,LO- by means of clocks respectively locked on the far-end received bit and frame clocks recovered from the line with two bit delay between transmit and receive frame, or locked with a fixed delay on the Frame Sync signal received from FSa input.

LINE RECEIVE SECTION

The receive input signal should be derived via a 1:1 a or 1:2 transformer of the same type used for

the transmit direction.At the front end of the receive section is a continuous filter which limits the noise bandwith. To improve the protection of the line interface and to comply with the receive input impedance spec even if power is lost, it is necessary to add 3 external resistors between the receive transformer and the LI+/LI- pins.

To correct pulse attenuation and distorsion caused by the transmission line in point-to-point and extended passive bus applications, an adaptive equalizer enhances the received pulse shape, thereby restoring a "flat" channel response with maximum eye opening over a wide spread of cable attenuation characteristics.

This equalizer is always enabled when either TE or NT mode adaptive sampling is selected, but is disabled for NT short passive bus applications, when NT mode fixed sampling is selected.

An adaptive threshold circuit maximizes Signal to Noise ratio in the eye at the detector for all loop conditions.

A DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols.

The MCLK input provides the reference clock for the DPLL at 15.36MHz.

When the device is powered down, a Line Signal Detect circuit, able to discriminate a valid line signal from noise, is enabled to detect the presence of incoming data. LSD-output pulls low to wake up the equipment.

GCI INTERFACE

General Description

GCI interface is an European standardized interface to connect ISDN dedicated components in the different configurations of equipment as Terminals, Network Terminations, PBX, etc...

In Terminal Equipments, this interface allows connection between SID-GCI and an associated ST5451 HDLC&GCI Controller used for 16kbit/s D channel processing and SID-GCI control. 64kbit/s B1 and B2 channels are transferred on GCI interface providing direct connection for B channel processing peripherals like Programmable ISDN COMBO ST5080 or extra ST5451 controllers.

In NT2 or PBX line card, GCI interface permits connection of up to 8 SID-GCI onto a common serial multiplexed bus. Each SID-GCI is assigned to one GCI channel selected by hardware configuration.

Figure 3 shows the Frame structure of a GCI channel. One GCI channel is structured in four subchannels:

- B1 channel 8 bits
- B2 channel 8 bits
- Monitor (M) channel 8 bits
- SC channel which is structured as follows:
  - D channel 2 bits
  - C/I channel 4 bits
  - A bit associated with M channel
  - E bit associated with M channel

B1,B2 and D channels are used to transfer 2B + D basic access data.

M channel is used to read and write multiframe S1 and Q channel messages and to configurate SID-GCI. Protocol for byte exchange on the M channel uses the E and A bits.

C/I (Control/Indicate) channel is used to exchange "real time" primitives between the SID-GCI and the Controller as Activation/Deactivation codes.

Physical Description

The interface consists of 4 wires:

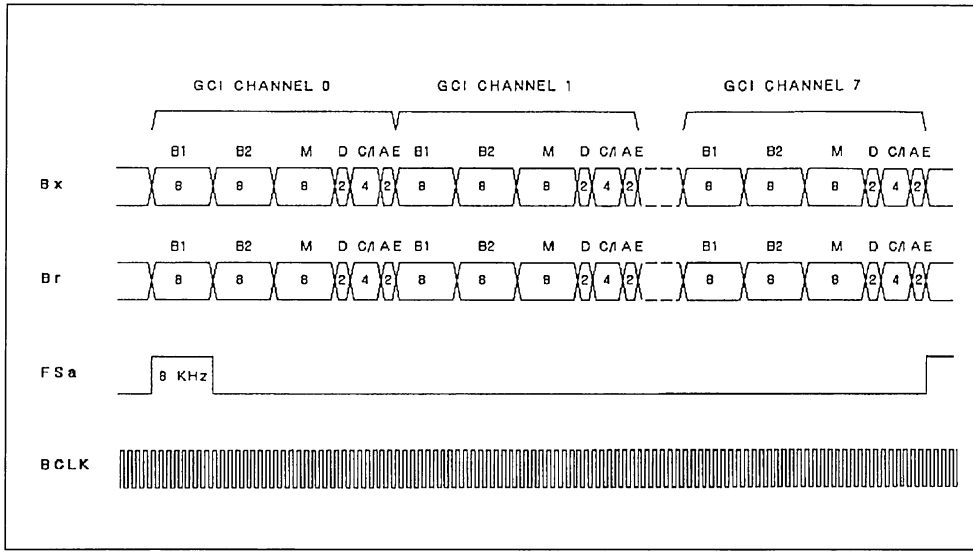
- Input Data: Bx
- Output Data: Br
- Bit Clock: BCLK
- Frame Synchronization: FSa

Data is synchronized by BCLK and FSa signals. The latter insures reinitialization of a time slot counter at each frame beginning. Its rising edge is the reference for the first bit of the first GCI channel. Data is transmitted in both directions at half the BCLK frequency, on the rising edge of BCLK and is sampled 1.5 period after the transmit rising edge. Unused channels are high impedance.

In NT2 or PABX equipments, up to 8 GCI channels (32 bits each) may be multiplexed on Bx and Br links used as a serial bus for several devices. The channel number selection is made by programming pins S0,S1 and S2 according to the following rules:

S2	S1	S0	Channel Number	Timeslots
0	0	0	0	0 -3
0	0	1	1	4 - 7
0	1	0	2	8 - 11
0	1	1	3	12 - 15
1	0	0	4	16 - 19
1	0	1	5	20 - 23
1	1	0	6	24 - 27
1	1	1	7	28 - 31

Figure 3: GCI Interface Structure



BCLK frequency may be any value between 512 and 6176kHz.

In TEM and NT1 configurations, the first GCI channels is automatically selected.

In TEM configuration, due to SID-GCI recovery circuitry, a low jitter should be provided on FSa and BCLK clocks. FSa and BCLK are always in phase. The maximum value of jitter amplitude is a step of 65ns at each GCI frame (125µs). The maximum high frequency jitter amplitude is 130ns pk-pk.

For applications such as the network side of an NT2, eg, a PABX trunk card, TES mode allows the transmission side of SID-GCI to be a slave to the received frame timing while GCI is also in slave mode Elastic buffers which allow any phase relationship between FSa and I.430 frames and a clock resynchroniser circuit absorb jitter and low frequency wander up to at least 18µs pk-pk at frequencies below 10Hz.

Exchange Protocol on the C/I channel

Exchange of information in the C/I channel runs as follows:

Two devices connected on a GCI channel send each other a permanent four bit command code in the C/I field. The same code is sent at a 8kHz frequency as long as the content of the internal C/I register remains unchanged.

When a change of C/I the command is initiated that is recognized by SID-GCI if detected in two consecutive frames.

ST5421 will interpret the new code and send the corresponding control instructions on the S line or switch a local function as long as the corresponding action is required.

An information change received from the S line or a local status change of SID-GCI set a new indication code on the C/I channel. The code is sent at least in 2 consecutive frames.

Table 2 gives the C/I codes meaning. C1 bit is first transmitted.

Here after for each mode a list of recognized Control and Indicate codes is given.

TEM mode: Control

0000 (DR) : Deactivation Request
In the Power Up state, DR instruction can be used as a Deactivation Request instruction to force transmission of INFO0 on the S line.

0001 (PDN) : Power Down Request.
PDN instruction forces the device to the Power Down state after that DI (1111) has been sent in two consecutive frames.

1000 (AR8) : Activate Request Class 8.
AR8 instruction combines an Activation Request, which initiates the Activation Sequence on the line, and a request to attempt to access the transmit D channel in the high priority class at the S interface after its complete activation. After activation of the S interface, AI8 indication is sent by ST5421. D channel access attempt is

Table 2: C/I Channel Coding

Code	TEM		LT/NT2		TES		NT1	
C1 C2 C3 C4	Ind.	Com.	Ind.	Com.	Ind.	Com.	Ind.	Com.
0000	DP	DR	TIM	PUP/DR	DP	PUP/DR	TIM	DR
0001	X	PDN	X	PDN	X	PDN	X	X
0010	X	X	X	X	X	X	X	X
0011	EOM	X	X	X	X	X	X	X
0100	EI	X	EI	X	EI	X	EI	FI2
0101	X	X	X	X	X	X	X	X
0110	X	X	X	X	X	X	X	X
0111	X	X	X	X	X	X	X	X
1000	AP	AR8	AP	AR	AP	AR	AP	AR
1001	CON	AR10	X	X	X	X	X	X
1010	X	ARL	X	ARL	X	ARL	X	ARL
1011	X	X	X	X	X	X	X	X
1100	AI8	X	AI	FI4	AI	X	AI	FI4
1101	AI10	X	X	X	X	X	X	X
1110	AIL	X	AIL	X	AIL	X	AIL	X
1111	DI	DC	DI	DC	DI	DC	DI	DC

(x) codes reserved

automatically processed for each HDLC frame to be transmitted without need for new Control Instruction.
Except for code EOM, any further indication change on C/I as CON or EI deactivates D channel access attempt at the S interface. A new AR8 instruction is needed to restart the procedure.
Note : A new AR8 instruction means that if the controller was already sending AR8, it has to change first the code sent to ie DC (1111) and after change again to AR8.

1001 (AR10) : Activate Request Class 10.
Same meaning as AR8 command but requesting access to transmit D channel with low priority class.
After activation of the S interface has been completed, AI10 indication is sent by SID-GCI.

1010 (ARL) : Activate Request Loopback.
ARL instruction operates a loopback of 2B + D channels from Bx input to Br output. It may be set when the device is either activated, in which case it is transparent (the composite signal is also transmitted to the line), or when it is deactivated in which case it is non transparent.
Any change from ARL to another C/I command clears the loopback.
When the complete loopback is activated, (AIL) code is sent by SID-GCI.

1111 (DC) : Deactivation Control.
DC instruction allows ST5421 to enter automatically the Power Down state if the S line is deactivated (DP sent by SID-GCI). When S line is not deactivated, DC has no effect.

TEM mode : Indication

0000 (DP) : Deactivation Pending Indication.
DP code indicates ST5421 is powered up and that no identified signal has been detected on the S line. DP indication is sent when one of the following events occur :
- Power Up has been completed and no signal is identified on the line,
- after a period of activity, INFO0 is detected on the S line,
- the device being in status F4, F5, F6, F7 or, F8, a DR instruction is issued.

0011 (EOM) : End of Message.
EOM indicates that the closing flag of a D channel message has been transmitted on S line indicating successfull completion of a packet sending. EOM is sent continuously until receiving of a new AR8 or AR10 command or line status change.
EOM code sending can be disabled via a Monitor channel instruction EID : (see table 3).

0100 (EI) : Error Indication.
EI indicates that a frame loss of has been detected on S line ; is sent when one of the following events occur :
- being in the F6 or F7 states, detection of a loss of frame, (jump to F8).

- being in the F7 state, receiving of INFO2, (jump to F6).

1000 (AP) : Activation Pending.
AP indicates that INFO2 (or INFO4) frames have been identified on the line.
AP indication is sent when one of the following events occur:
- being in F2 deactivated state, detection of INFO2 or INFO4.
- being in the loss framing state F8, detection of INFO2

1001 (CON) : Contention Indication
CON is sent when, during transmission of a packet in the D channel, a received E bit does not match the last transmitted D bit, indicating a lost collision.
D channel access attempt is deactivated at the S interface. A new AR8 or AR10 instruction is needed to restart the procedure.

1100 (AI8) : Activation Indication Class 8.
AI8 is sent when, following an AR8 instruction, the S line is completely activated (state F7). The D channel access procedure is set in the high priority class 8 (or 9).

1101 (AI10) : Activation Indication Class 10.
AI10 is sent when, following an AR10 instruction, the S line is completely activated. The D channel access procedure is set in the low priority class 10 (or 11).

1110 (AIL) : Activation Indication Loopback.
AIL indicates that the complete loopback requested by the instruction ARL is completed.

1111 (DI) : Deactivation Indication.
DI is sent at least in two consecutive frames when, being in the S line deactivated state (DP indication sent by SID-GCI) DC control instruction is received on C/I control channel.
After that, SID-GCI is automatically powered down.

TES mode : Control.

0000 (PUP/DR) : Power Up Request/Deactivation Request.
When in Power Down, Power Up instruction powers up the device in the configuration previously set. When in Power Up, PUP/DR can be used as a Deactivation Request instruction to force the transmission of INFO0 on the line.

0001 (PDN) : Power Down Request.
PDN instruction forces the device to the Power Down state.

1000 (AR) : Activate Request.
AR instruction initiates the Activation Sequence on the line. It is recommended that an AR be delayed at least 2ms after the PUP instruction.

1010 (ARL) : Activate Request Loopback.
Identical to TEM mode.

1111 (DC) : Deactivation Control.
DC instruction allows ST5421 to enter automatically the Power Down state if the S line is deactivated (DI sent by SID-GCI). When S line is not deactivated, DC has no effect.

TES mode : Indication.

0000 (DP) : Deactivation Pending.
DP code indicates ST5421 has been just powered up and no signal has been identified on the line.

0100 (EI) : Error Indication.
Identical to TEM mode.

1000 (AP) : Activation Pending.
Identical to TEM mode.

1100 (AI) : Activation Indication.
AI is sent when, following an AR instruction, the S line is completely activated in state F7.

1110 (AIL) : Activation Indication Loopback.
Identical to TEM mode.

1111 (DI) : Deactivation indication.
DI indication is sent when one of the following events occur:
- After a period of activity, INFO0 is detected on the S line,
- the device beeing in status F4, F5, F6, F7 or F8, DR instructions is issued.

NT1 mode : Control.

0000 (DR) : Deactivation Request.
DR command forces ST5421 through the appropriate deactivation sequence where INFO0 is sent on the line. The device remains in the Power Up state. DI indication is sent.

0100 (FI2) : Force Info 2
Being in the activated state G3, FI2 instruction forces the appropriate sequence to send INFO2 on the line. If the S line is not completely activated, FI2 instruction has no effect.

1000 (AR) : Activation Request.
Being in the inactive Power Up state, sending INFO0, AR instruction forces SID-GCI through the appropriate sequence to send INFO2 on the line. It is recommended that an AR instruction be delayed at least 2ms after setting the GCI clocks.

1010 (ARL): Activate Request Loopback.
Identical to TEM mode.

1100 (FI4) : Force Info 4.
An activation Request being in progress, FI4 instruction allows SID-GCI through the appropriate sequence to send INFO4 on the line.

1111 (DC) : Deactivation Control.
DC instruction has no effect on SID-GCI.

NT1 mode : Indication.

0000 (TIM) : Timing Requested.
Being in Power down state, the LSD- output is pulled low to indicate that the far-end is attempting to activate the S interface. The device requests GCI clock signals. Receiving of GCI clocks powers up the SID-GCI, LSD- is freed, and TIM code is sent on the C/I channel.

0100 (EI) : Error Indication.
EI code indicates that a loss of frame has been detected on the S line, ST5421 being previously activated.

1000 (AP) : Activation Pending.
AP code indicates that INFO1 frames have been identified of the line. The device is waiting for an activate request to send INFO2.

1100 (AI) : Activation Indication.
AI code indicates that the S line is activated. That means it is receiving INFO3.

1111 (DI) : Deactivation Indication.
DI code indicates S line is completely deactivated: the device can be powered down switching off GCI clocks.

1110 (AIL) : Activation Indication Loopback.
Identical to TEM mode.

NT2 mode : Control.
0000 (PUP/DR) Power Up Request/Deactivation Request.
When in Power Down state, PUP code powers up the device in the NT2 configuration previously selected. When in Power Up state DR code forces the appropriate deactivation sequence where INFO0 is sent on the line. SID-GCI remains in Power Up state.

0001 (PDN) : Power Down Request.
Identical to TES mode.

1000 (AR) : Activation Request.
After a PUP instruction, AR forces the appropriate sequence to send INFO2 on the line. It is recommended that AR instruction is sent after receiving TIM indication..

1010 (ARL) : Activation Request Loopback.
Identical to TEM mode.

1100 (FI4) : Force Info 4.
An Activation Request being in progress, FI4 instruction puts ST5421 through the appropriate sequence to send INFO4 on the line.

1111 (DC) : Deactivation Control.
The DC instruction allows to enter the power down state if the S line is deactivated.
DC control has no effect if SID-GCI not sending DI indication.

NT2 mode : Indication.

0000 (TIM) : Timing Requested.
Being in Power down state, LSD- output is pulled low to indicate that far-end is attempting to activate the interface. SID-GCI requests GCI clocks followed by a PUP instruction. After receiving, LSD- is freed and TIM is sent on C/I channel.

0100 (EI) : Error Indication.
Identical to NT1 mode.

1000 (AP) : Activation Pending.
Identical to NT1 mode.

1101 (AI) : Activation Indication.
Identical to NT1 mode.

1110 (AIL) : Activation Indication Loopback.
Identical to TEM mode.

1111 (DI) : Deactivation Indication.
The DI code indicates that the S line is completely deactivated.

EXCHANGE PROTOCOL ON M CHANNEL

Protocol allows a bidirectional transfer of bytes between SID-GCI and a Controller (for example ST5451) with an acknowledgement at each received byte.

Write cycle.
The Controller sends to ST5421 control instruction(s) coded on a single byte. It is possible but optional to write several control instructions in a single message. Control instruction bytes are structured as defined in Table 3.

Read cycle.
When a new validated S1 or Q message is received from the line, the device send a single byte message as defined in table 4. If a new message is received from the S line before the previous is acknowledged by the controller end, this new message is lost.

Exchange protocol.
The exchange protocol is identical for both directions.

The sender uses E bit to indicate that it is sending a M byte while the receiver uses A bit to acknowledge the received byte.

When no message is transferred, E bit and A bit are forced to inactive state (i.e. high impedance).

A transmission is initialized by the sender setting E bit in active state and sending the first byte on M channel in the same frame. Transmission of a message is allowed only if A bit received has been detected inactive in the last two frames.

When the receiver is ready, it validates the received byte internally when it has been detected identical in two consecutive frames. Then, the receiver set first A bit from inactive to active state; it is the pre-acknowledgement, and maintain A bit active at least in the following frame, it is the acknowledgement.
If validation is not possible, the two last bytes received not identical, the receiver abort the message by setting A bit active for one frame only.

A second M byte may be transmitted by the sender turning E bit from active to inactive state and sending the byte in the same frame. The E bit is set inactive for one frame only. If it remains inactive more than one frame, it is an end of message. The second byte may be transmitted only after receiving the pre-acknowledgement of the previous byte (see timing diagram).

The receiver validates the current received byte as for the first one and then set A bit in the next two frames first from active to inactive state (pre-acknowledgement) and from inactive to active (acknowledgement). If the receiver cannot validate (the two bytes received are not identical) it pre-acknowledges normally but let A bit in the inactive state in the next frame which indicates an abort request.

If a message is aborted, ST5421 sends again the complete message until receiving acknowledgement.
A received message is acknowledged or aborted without flow Control.
Figure 4 gives the timing of a write cycle. The most significant bit of a Monitor byte is sent first of the M channel. E & A bits are active low and inactive state on Br is high impedance.

Figure 4: Monitor messaging

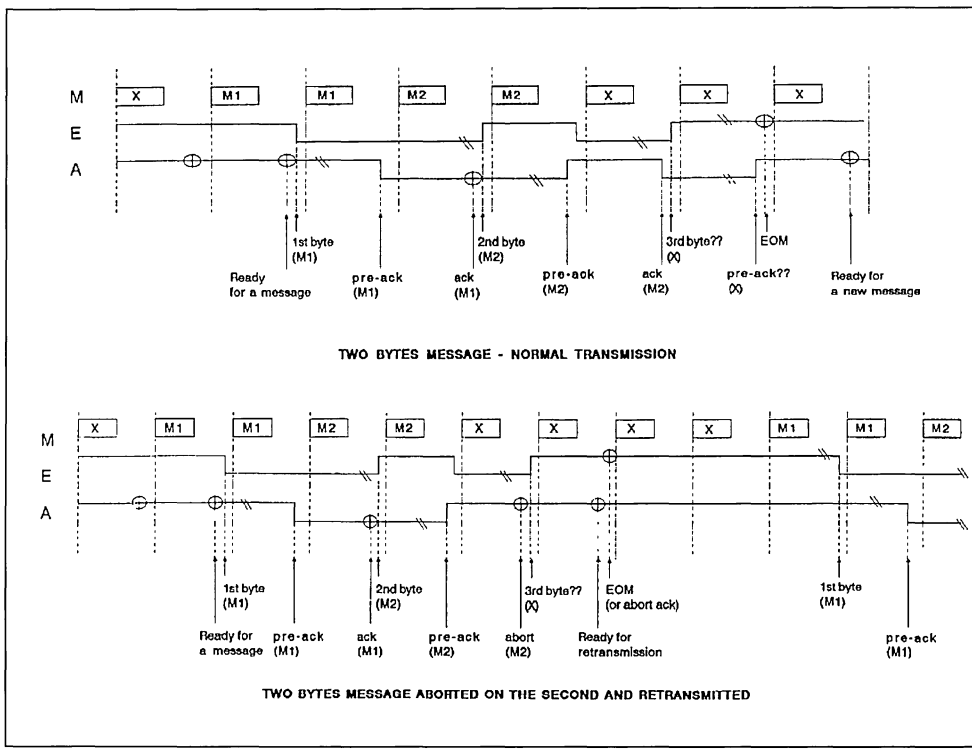


Table 3: Monitor Channel Instruction

Functions	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Device Mode:									
NT Mode Adaptive Sampling (*)	NTA	0	0	0	0	0	1	0	0
NT Mode Fixed Sampling	NTF	0	0	0	0	0	1	0	1
TE Slave Mode (slave-slave)	TES	0	0	0	0	0	1	1	0
Monitoring Mode Activation	MMA	0	0	0	1	1	1	1	1
TE Master Mode	TEM	0	0	0	0	0	1	1	1
B Channel Configuration:									
B Channel Mapped Direct (*)	BDIR	0	0	0	0	1	1	0	0
B Channel Exchanged	BEX	0	0	0	0	1	1	0	1
B1 Channel Enabled (*)	B1E	0	0	0	1	0	1	0	0
B1 Channel Disabled	B1D	0	0	0	1	0	1	0	1
B2 Channel Enabled (*)	B2E	0	0	0	1	0	1	1	0
B2 Channel Disabled	B2D	0	0	0	1	0	1	1	1
End of Messages Indication:									
EOM Indication Enabled (*)	EIE	0	0	0	1	0	0	0	1
EOM Indication Disabled	EID	0	0	0	1	0	0	0	0
Multiframe Processing:									
Multiframe Disabled (*)	MID	0	0	0	1	0	0	1	1
Multiframe Enabled	MIE	0	0	0	1	0	0	1	0
Disable Three Time Checking	DIS3X	0	0	1	0	1	0	0	1
Enable Three Time Checking (*)	EN3X	0	0	1	0	1	0	0	0
Write Multiframe Message	MFT	0	0	1	1	M1	M2	M3	M4
Loopback Test Mode:									
Clear All loopbacks (*)	CAL	0	0	0	1	1	0	1	1
Loopback B1 on Line Enabled	LB1E	0	0	0	1	1	0	0	0
Loopback B2 on Line Enabled	LB2E	0	0	0	1	1	0	0	1
Loopback 2B+D Enabled (1)	LBS	0	0	0	1	1	0	1	0
Loopback B1 on GCI Enabled	LBB1E	0	0	0	1	1	1	0	0
Loopback B2 on GCI Enabled	LBB2E	0	0	0	1	1	1	0	1

(1) alternate command instruction to ARL (C/I code), but without any status indication pending.
(*) initial state following Power on initialization

Table 4: Monitor Status Messages

Functions	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Multiframe Receive Register	MFR	0	0	1	1	M1	M2	M3	M4

Monitor channel code description:
Monitor channel code list is given in table 3 and 4.

Device mode.

NTA : NT mode Adaptive sampling.
In NT mode, adaptive sampling should be selected when the device is an NT equipment connected on any wiring configuration up to the maximum specified length for operation. Multiple Terminals, if required, must be grouped within approximately 50 meters one from each other (depending on cable capacitance as indicated in I.430). Transmit section of SID-GCI is phased locked to GCI FSa source.

NTF : NT mode fixed sampling.
In NT mode, fixed sampling should be selected when the device is in a NT equipment connected on a passive bus wiring configuration up to approximately 200 meters in length depending on cable type. In this mode the receiver DPLL is disabled and sampling of the received symbols is fixed to enable multiple Terminals (nominally up to 8) to be connected anywhere along the passive bus. Transmit and Receive section is phased locked to GCI FSa source.

TES : TE mode connected on the T interface.
This mode should be selected when the device is used on the T interface side of an NT2 equipment. I.430 circuitry operates as in TE mode but GCI interface is driven by BCLK and FSa sources providing a slave-slave configuration.

Data buffers and a clock resynchronizer enable

the GCI to function with FSa and BCLK jittering sources. No phase relationship is needed between the line recovered clocks and GCI.

A 1536kHz clock signal output phased locked to the Recevied line signal is delivered on CLK.

CLK output signal is generated only when ST5421 if fully activated (state F7) and no clock signal is detected on that pin by the device during his own selected GCI channel.
Otherwise CLK output remains high impedance.

Note: CLK output is activated immediately on the first bit of the B2 channel (GCI side) and is deactivated immediately if SID-GCI leaves F7 state

D channel access Control circuitry is disabled. i.e. D channel data at Bx input is continuously transmitted to the line; there is no monitoring of the D echo channel from the network direction.

MMA : Monitoring mode activation.
When ST5421 is configured in TE mode by means of pins M0, M1, the MMA instruction allows to receive and activate on INFO3 frames, while remaining the master of GCI. That configuration can be used for applications such as monitoring the outputs of TEs on a passive bus.
The received 2B+D can then be passively monitored (the line transmit LO+,LO- would not be connected).

TEM : TE Master Mode.
When ST5421 is in TE configuration by means of pins M0, M1, and in the Monitoring Mode Activation by means of the instruction MMA, the TEM instruction set back SID-GCI in the normal TE Master mode.

B channels configuration.

BDIR/BEX B1E/B1D B2E/B2D
BDIR and BEX instructions provide for the exchange of data between the B1 and B2 channels. (Note: when enabling a B channel in conjuction with the BEX command, channels is referenced at the CGI).
When either or both B channels are disabled by means of the B1D or B2D instruction, binary 1 are transmitted on the line regardless of Bx input while Br output is in high impedance state. When enabled by means of B1E and B2E instructions, B channel are transparently transmitted.

End of message indication.

EID/EIE
C/I channel End Of Message code sending can be enabled with instruction EIE and disabled by means of EID.

Multiframe processing.

MFT/MFR/MIE/MID
In the Transmit direction, with the device in TEM or TES mode, data entered in bit positions M1, M2, M3 and M4 of instruction MFT is transmitted to the NT in multiframe bit positions Q1, Q2, Q3 and Q4 respectively. With the device in NT mode, data entered in the M bit positions is transmitted to the TE in multiframe bit positions S11, S12, S13 and S14 respectively. In the Receive direction, when the Multiframe receive data buffer requires servicing, the MFR (see table 4) status message is autonomously sent with M1, M2, M3 and M4 bits representing Q1, Q2, Q3 and Q4 or S11, S12, S13 and S14 bits received from the multiframe respectively.

Multiframe Structure and transmission protocol on the line comply with the ANSI US Standard T1.605.1989. "Basic Access Interface for S and T Reference points - Layer 1 specification".

Multiframe message exchange can be supported by SID-GCI when the line is synchronized : states F6 & F7 in TEM or TES modes and state G3 in NT modes.

The multiframe channel processing must be enabled by an MIE instruction to use these channels.

DIS3X/EN3X

When EN3X is set, a new Multiframe message received from the line is checked and transferred on the M channel when received three times identical.
When DIS3X is set, Multiframe messages are transferred tranparently every superframe.

Loopback test modes

CAL/LBS/LB1E/LB2E/LBB1E/LBB2E
LB1E and LB2E instructions turn each individual B channel from the line receive input back to the line transmit output. They may be set separately or together.
LBB1E and LBB2E instructions turn each individual B channel from GCI input to the GCI output. They may be set separately or together.
CAL instruction clears both loopbacks.
It is not allowed to set or clear a LB1, LB2, LBB1 or LBB2 loopback while a complete loopback is set by means of the C/I instruction ARL. LBS can be used as an alternate command to ARL.

Activation/Deactivation

In NT configuration :

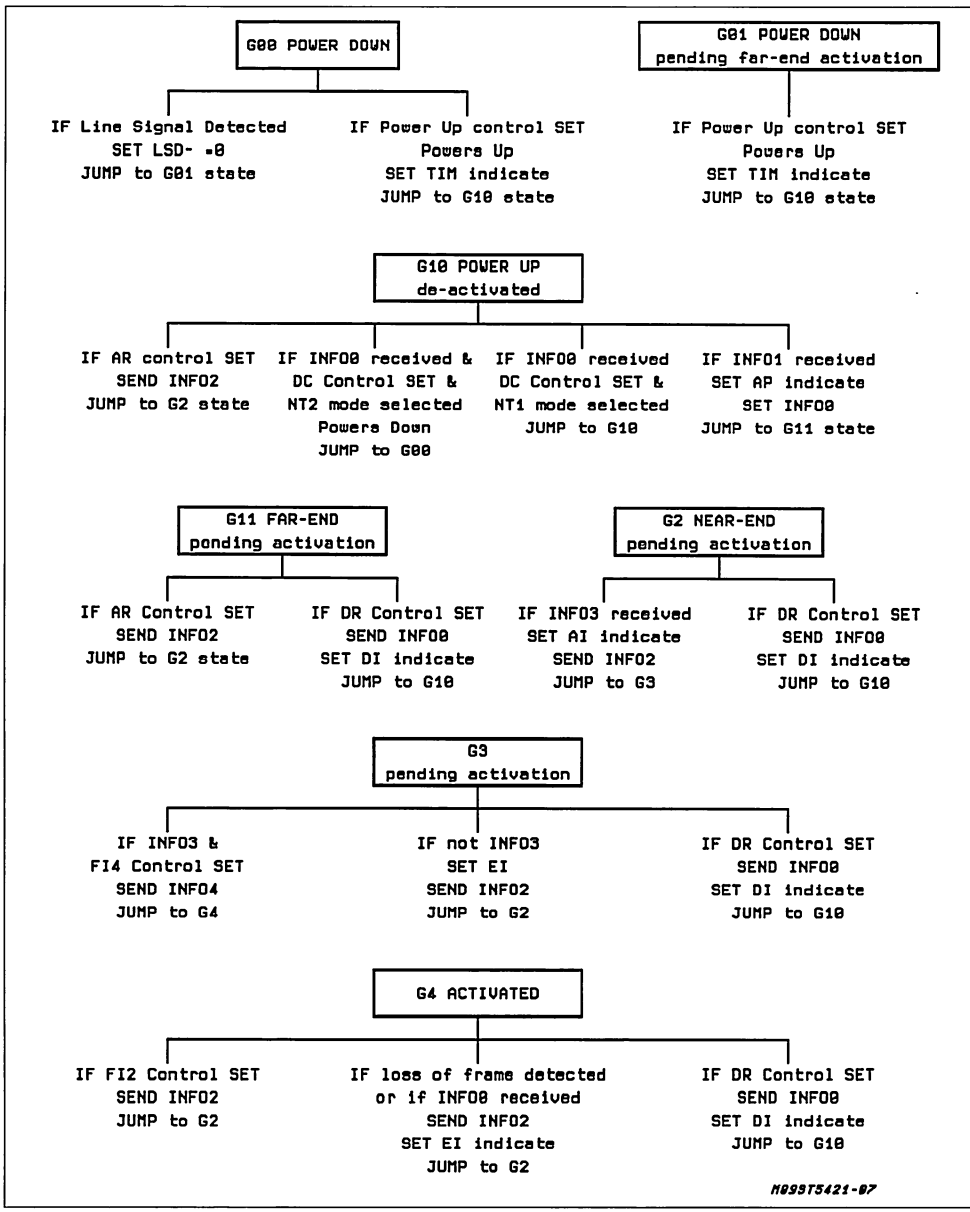
After Power on initialization, ST5421 can be con-

figured in NT1 or NT2 mode, by means of pins and register programming. In NT1, SID-GCI is powered up directly by receiving the GCI clocks on BCLK and FSa inputs. In NT2 mode, the device is powered up by means of PUP code on the C/I Control channel.

Activation may be initiated from either end of the loop.

To operate an activation from the Network, ST5421 must be first powered up by the appropriate procedure followed at least 2ms later by an AR instruction on the C/I channel. Network timing,

Figure 5: Activation Procedure in GCI mode, NT Selected.



FSa, BCLK and MCLK must be present at this time. When activation is initiated by the far-end, SID-GCI being in the Power Down state, a Line Signal Detector circuit pulls low LSD- pin, which can be used to wake up the system. A power Up procedure must be then be issued allowing identification of received signal ie, INFO1 or INFO2. The appropriate procedure is then followed according to I.430.

I.430 recommends that 2 Timers should be available in an NT. An Activation Request should be associated with the start of an external Timer 1 if required. Timer 1 should be stopped when the AI indication is generated following successful activation. If Timer 1 expires before AI is generated, however, Control instruction DR should be written to the device to force deactivation. Timer 2 which is specified to prevent unintentional re-activation, is not required since ST5421 can uniquely recognize INFO1 frames.
Two extra codes are needed for NT1 application: FI4 indicates to the SID-GCI that the U line is activated and allows completion of activation by sending INFO4. FI2 indicates to SID-GCI that the U line has lost synchronization and requests sending of INFO2.

In TEM or TES configuration :
After Power on initialization, ST5421 can be configured in TE or TES power down mode, depending on pins and register configuration setting. In TEM mode, SID-GCI is powered up by pulling low the Bx input. SID-GCI reacts by sending GCI free-running clocks. In TES mode, the SID-GCI is powered up by means of the PUP code on the C/I Control channel.

Activation may be initiated from either end of the loop. To operate an activation from the Terminal, the device must be first powered up by the appropriate procedure followed at least 2ms later by an AR instruction on the C/I channel. When activation is initiated by the far-end, SID-GCI being in the Power Down state, a Line Signal Detector Circuit pulls low the LSD- pin, which can be used to wake up the system. A Power Up procedure must then be issued allowing identification of received signal ie, INFO2. The appropriate procedure is then followed according to I.430.

Figure 6: Activation Procedure in GCI mode, TE Selected

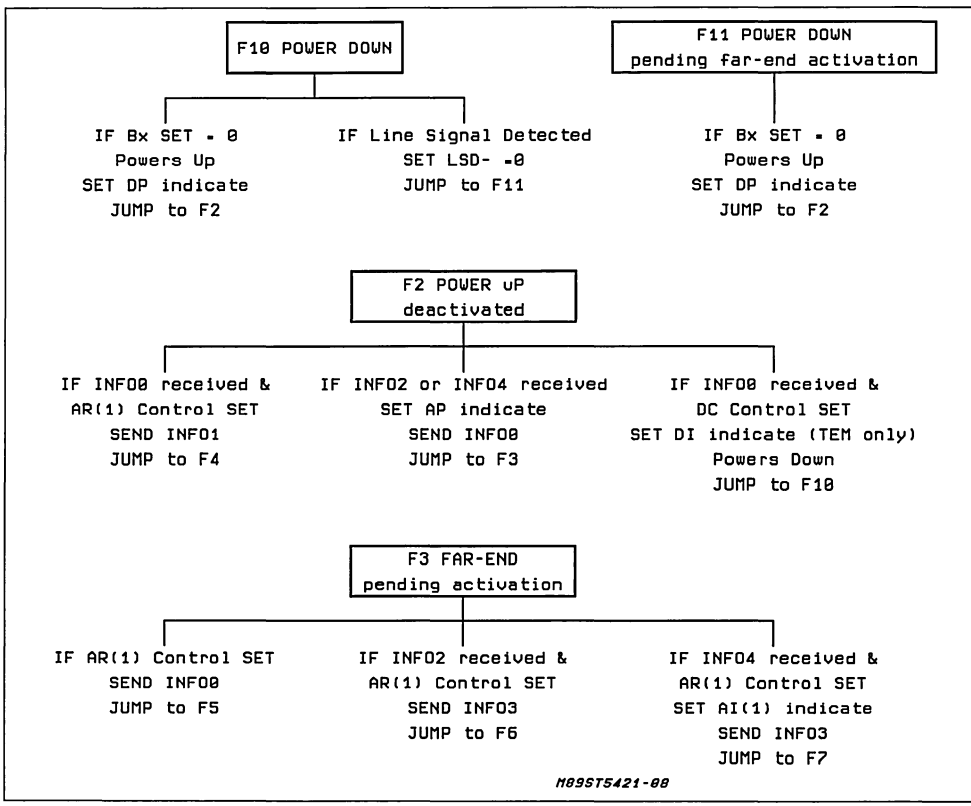
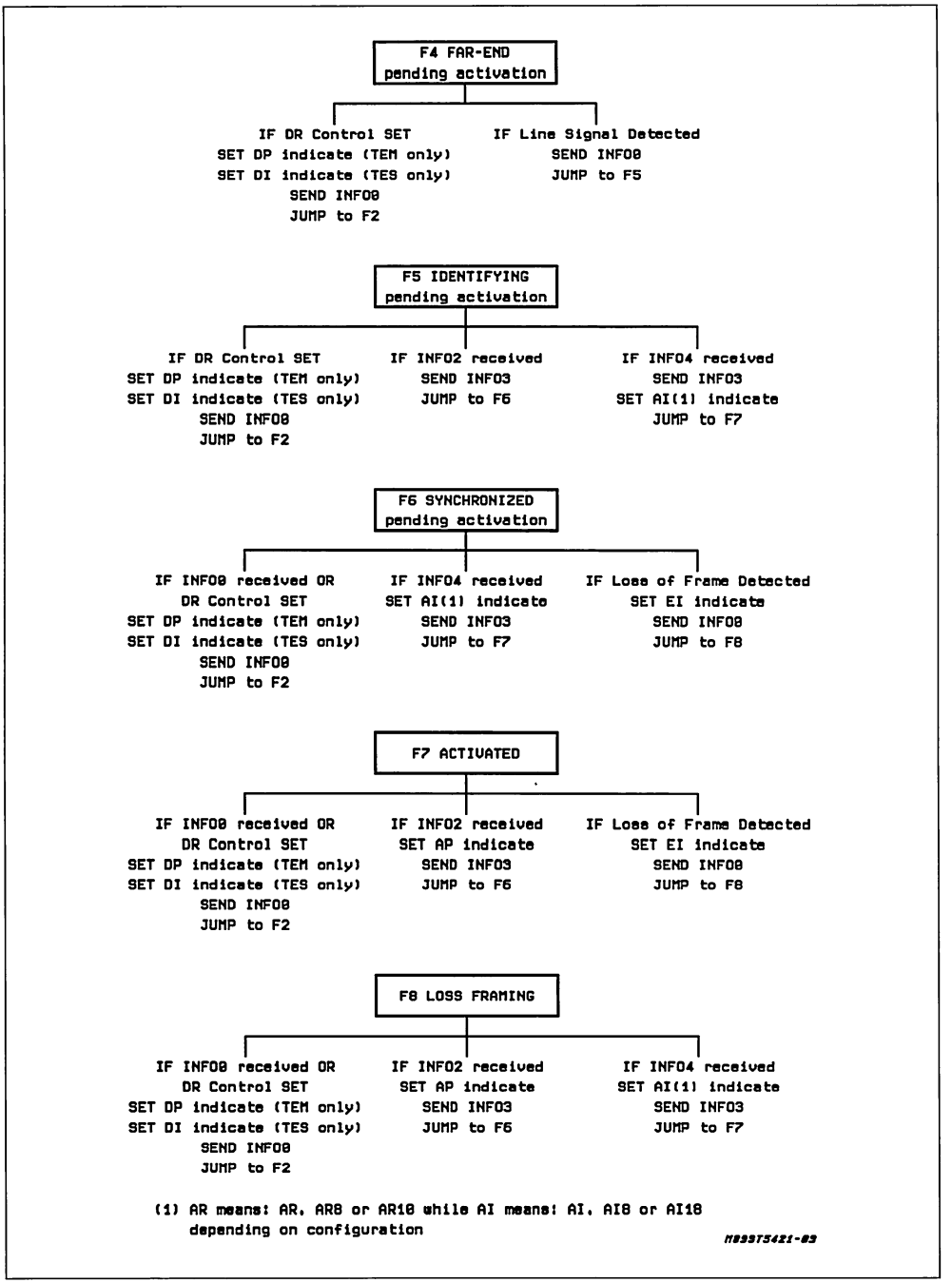


Figure 6: Continued



I.430 recommends that a Timer should be available in a TE. An Activation Request to the SID-GCI should be associated with the start of an external Timer 3 if required.Timer 3 should be stopped when the AI indication is generated following successful activation. Timer 3 expires before AI, AI8 or AI10 is generated, however, Control instruction DR should be written to the device to force de-activation.

D CHANNEL ACCESS IN TEM MODE

A controller device requiring to start transmission of a packet on the line should first prepare the complete message such that the opening Flag is ready to be shifted accross GCI. A Control Instruction AR8 or AR10 will initiate first the Activation Sequence on the line until activation has been completed and then the D channel access sequence according to Priority Class 1 (signalling) or Priority Class 2 (Data packet) respectively.

After line activation, AI8 (or AI10) indication is sent from SID-GCI. Then, DEN output immediately enables to prefetch the opening flag from the controller device into the SID-GCI D channel buffer. Meanwhile, the Priority Counter checks that no other TE connected to the S interface is transmitting in the D channel. This is assured by counting consecutive "1"s in the E bit position of frames received from the NT and comparing the value with the current priority level as specified by I.430. If another TE is active in the D channel, DEN pulses are inhibited once the Opening Flag is in the Transmit buffer to prevent further fetching of Transmit data from the Controller until D channel access is achieved.

As soon as the required number of consecutive E bit "1"s has been counted, the leading 0 of the opening flag is transmitted in the next D bit position to the NT. Then, DEN pulses are re-enabled in order to get new D channel bits. No other instructions are necessary for local flow control between controller and ST5421.

During transmission in the D channel, SID-GCI continues to compare each E bit with the D bit previously transmitted before proceeding to send the next. In case of mis-match, a contention for the previous D bit is assumed to have been won by another TE. Transmission of the current packet therefore ceases and "1"s are transmitted in all following D bit positions. Status indication CON is sent to the controller on C/I channel. DEN output pulses are again inhibited, and D channel access sequence is disabled.

In order to retransmit the lost frame, the controller must begin as before sending a new AR8 (or AR10) ; it has to change first the code sent (ie DI) and after change again to AR8. Successful sending of a transmit frame is detected when the closing Flag is transmitted in the D channel. "1"s are then transmitted in the following D bit positions.

If enabled by the Control Instruction EIE, indication EOM is sent to indicate the End of message.

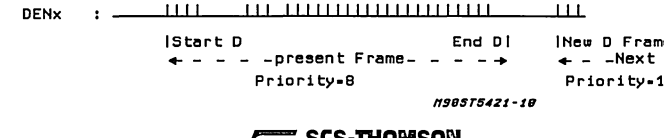
After sending of a transmit frame successfull, SID GCI will automatically perform a new D access sequence if it's still receiving AR8 or AR10 command on C/I channel, otherwise no D access sequence will be done until reception of AR8 or AR10 command.

Any indication change on the C/I channel except EOM indicates deactivation of the D channel access sequence and a new AR8 (or AR10) is needed to restart the procedure.

Note: Users willing to control the D channel access, can use this procedure:
Send AR8 or AR10 until receiving DENx, then remove ARx command code and replace it by an another command (ie DI that is equivalent to a NOP operation if the device is full_activated). At the end of a D frame EOM Indication is received (if EIE is set); when a new D message is prepared an ask for a new D channel access by AR8 or AR10 can be sent.

Users that want to discriminate consecutive D channel access with EOM Indication, are suggested to remove EOM Indication, between 2 D frames, to be able to separate the 2 messages EOM: With the following method: send AR8 (AR10) continuously, until receiving EOM Indication, then send ONCE AR8~ [0111] (AR10~ [0110]) on C/I channel and continue to send the previous code AR8 (AR10); this AR8~ (AR10~) is a kind of EOM aknowledge: the device detect a 'new' primitive AR8 (AR10), stop EOM Indication and replace it by AI8 or AI10 if ST5421 is still full activated.

For application with automatic D channel access and wanting to change the priority class (8 or 10) for D channel, they can use the following procedure:
Assuming that the present D frame is priority class 8 and that the next D frame will be priority class 10, users can change AR8 code to AR10 as soon as they are sure that the present D frame is started, by controlling DENx, anticipating the next D messages before the closing flag of the present D frame. When the automatic D channel access will be performed for next D message, the D channel request will be done with the desired priority class. (see figure below).



MULTIFRAME MAINTENANCE CHANNELS (S1 AND Q WORDS)

Each direction of transmission across the S interface includes a low-speed (800 b/s) channel for loop maintenance accessed via the monitor channel of ST5421. A multiframe structure, consisting of 20 frames on the S interface, is used to synchronize these channels and convey messages coded into 4-bit words, see Table 5. One word is transmitted downstream (NT-to-TE) in the S1 channel, and one word is transmitted upstream (TE-to-NT) in the Q channel every multiframe.

When the device is in NT mode, the MIE command enables both the transmission of the multiframe identification algorithm (reversal of the FA/N bits every 5th frame and M bit set = 1 every 20th frame) and enables the MFR message. The algorithm is present during INFO2 and INFO4 frames. In TE modes this command only enables the MFR message since the device will always search for and synchronize to the multiframing identification bits if NT is sending them. In all modes, at the end of each multiframe the received 4-bit word is decoded to determine if it should generate an MFR interrupt immediately, or be stored until 3 consecutive multiframes have contained the same 4-bit word before a MFR message is generated. Table 5 lists the codes which are 3-times checked. Note, however, that no other action is taken by the ST5421 in response to received codes (e.g. loop-backs are not automotically implemented); the external controller must take the necessary action. This provides the freedom to implement maintenance functions without constrains from the device, and to utilise the unassigned codes for other functions.
It is possible to disable the checking algorithm by setting DIS3X instruction on M channel. There, Multiframe words are transferred transparently on M channel.

The MID command disables the transmission of the Multiframe identification algorithm in NT mode and disables the MFR message in both NT and TE modes. Both the MIE and MID commands can only be written to the device when it is deactivated (either powered-up or powered-down). The Multiframe Transmit Register should also be loaded with the appropriate "idle" messages, by means of an MFT instruction, prior to activation.

Table 5: Codes for Q and S1 channel messages

Message (1)	NT to TE					TE to NT				
	Received at TE				Number of Repetitions Before MFR message (EN3X set)	Received at NT				Number of Repetitions Before MFR message (EN3X set)
	S11	S12	S13	S14		Q1	Q2	Q3	Q4	
Idle (Normal)	0	0	0	0	3	1	1	1	1	3
Loss-of-Power Indication	1	1	1	1	1	0	0	0	0	1
STP Pass	0	0	1	0	3	--	--	--	--	--
STF Fail	0	0	0	1	3	--	--	--	--	--
ST Request (3)	--	--	--	--	--	0	0	0	1	3
STI Indication	0	1	1	1	3	--	--	--	--	--
DTSE-IN	1	0	0	0	1	--	--	--	--	--
DTSE-OUT	0	1	0	0	1	--	--	--	--	--
DTSE-IN & OUT	1	1	0	0	1	--	--	--	--	--
LB1 Request	--	--	--	--	--	0	1	1	1	3
LB1/Indication	1	1	0	1	3	--	--	--	--	--
LB2 Request	--	--	--	--	--	1	0	1	1	3
LB2/Indication	1	0	1	1	3	--	--	--	--	--
LB1/2Request (2)	--	--	--	--	--	0	0	1	1	3
LB1/2Indication	1	0	0	1	3	--	--	--	--	--
Loss-of-Received Signal Indication	1	0	1	0	3	--	--	--	--	--
Unassigned	All other codes				1	All other codes				1

Notes:
(1) No autonomous action is taken by ST5421 in response to received messages. Where appropriate, the external controller must respond with a command or other action.
(2) The code "0011" will be received by an NT1 when the LB1 and LB2 requests are transmitted by two different TEs (NT2s) on a Passive Bus.
(3) The code "0001" will be received by an NT1 when ST Request and any other code (except LP) is sent simultaneously by two or more TEs on a Passive Bus

Figure 7: ISDN Telephone Set Application (non isolated)

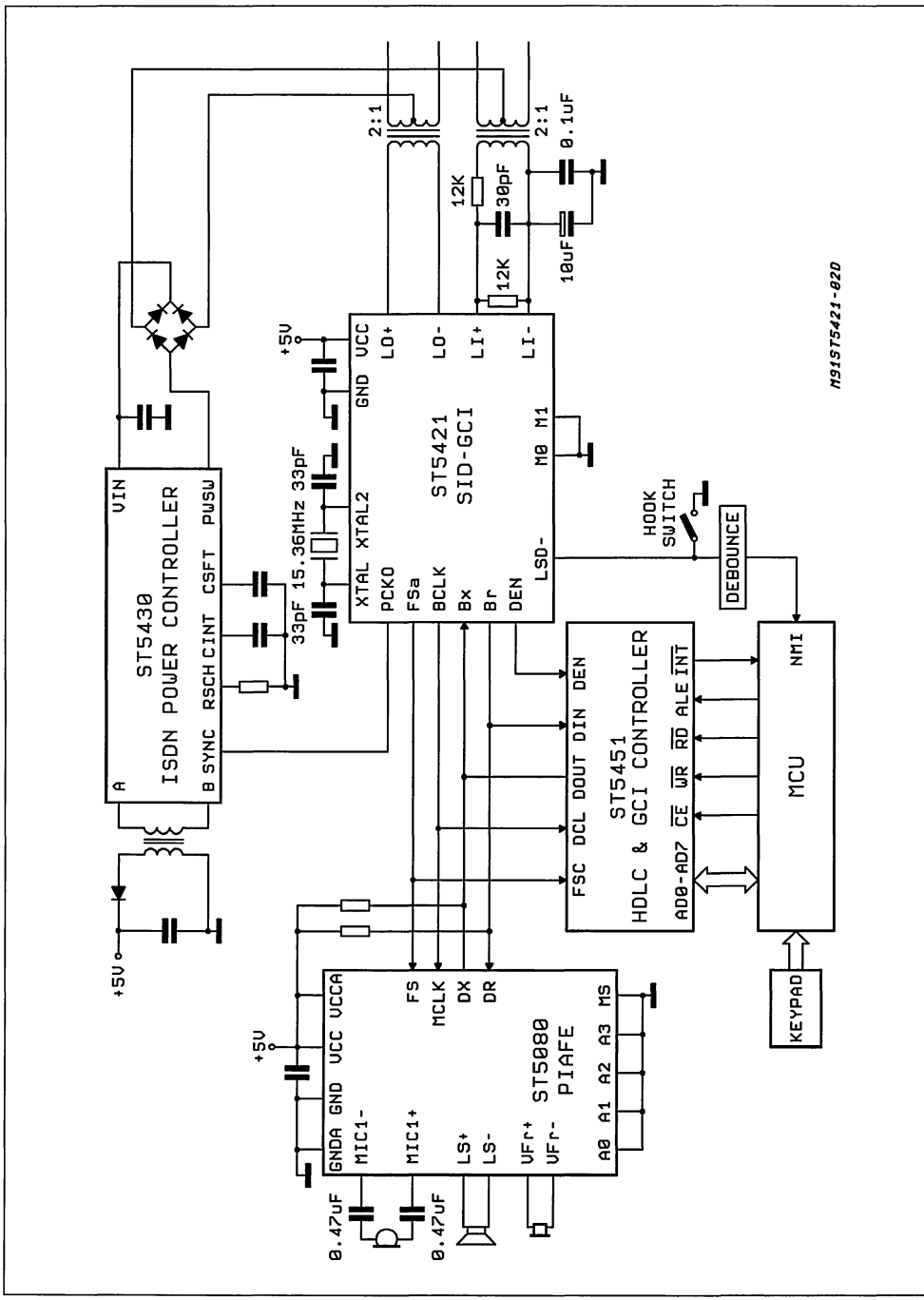
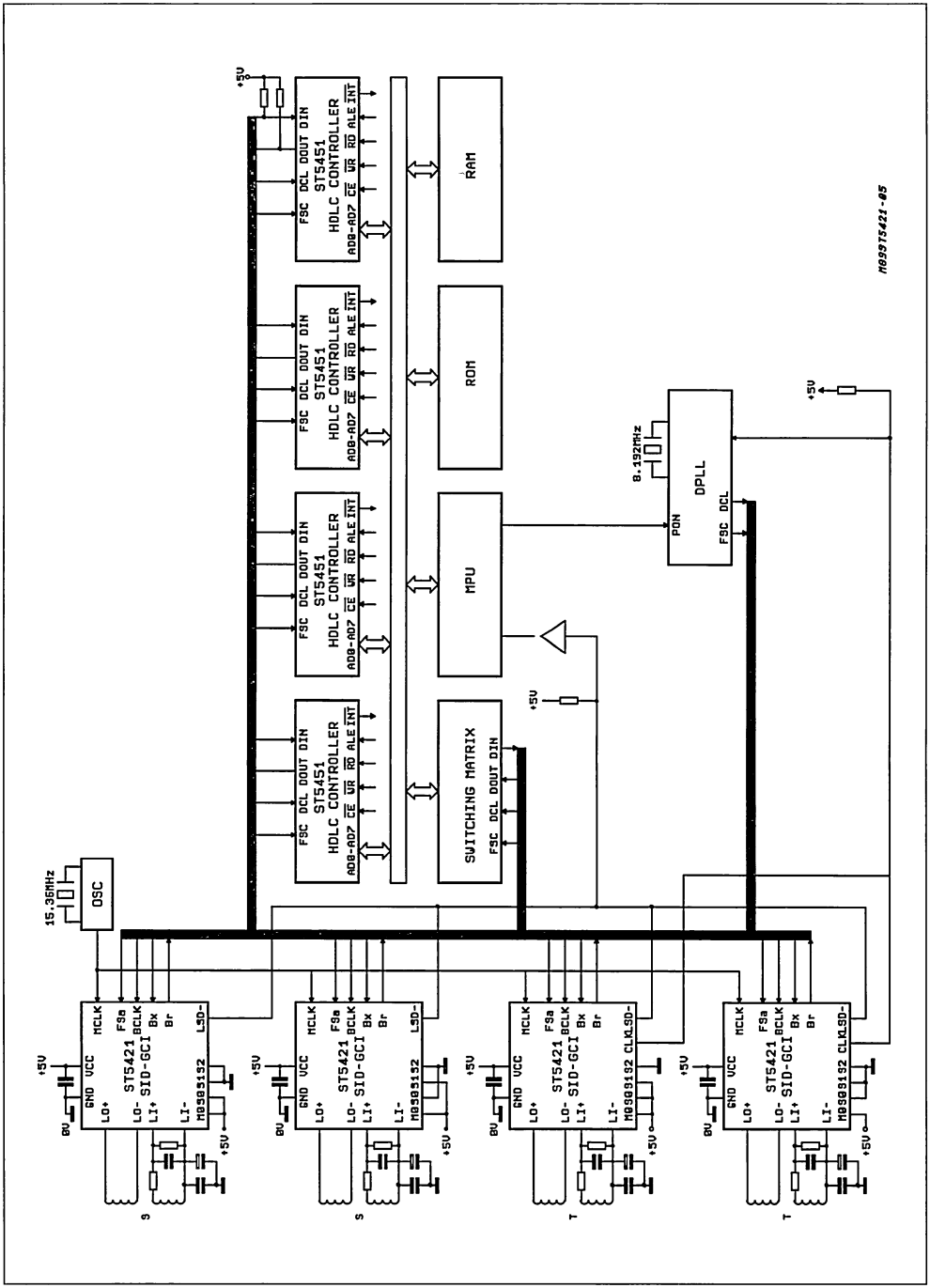


Figure 8: NT2 Application GCI Compatible



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
V_{CC} to GND	7	V
Voltage at Bx, Br	V_{CC} + 1 to GND - 1	V
Voltage at any Digital Input (except Bx)	V_{CC} + 1 to GND - 1	V
Current at any Digital Input (except Br)	± 50	mA
Current at Lo	± 100	mA
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering 10s)	300	°C

ELECTRICAL CHARACTERISTICS (unless specified otherwise: V_{CC} = 5V ±5%, T_A = 0 °C to 70°C; typical characteristics are specified at V_{CC} = 5V, T_A = 25°C. All signals are referenced to GND).

DIGITAL INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All Digital Inputs			0.7	V
V_{IH}	Input High Voltage	All Digital Inputs	2.2			V
V_{ILX}	Input Low Voltage	MCLK/XTAL input			0.5	V
V_{IHX}	Input High Voltage	MCLK/XTAL input	V_{CC}-0.5			V
V_{OL}	Output Low Voltage	Br: I_L = 3.2 mA All other Digital Outputs: I_L = ±1mA			0.4	V
V_{OH}	Output High Voltage	Br: I_L = 3.2 mA All other Digital Outputs: I_L = ±1mA All outputs, I_L = 100µA	2.4 2.4 V_{CC}-0.5			V V V
I_{IL}	Input Low Current	Any Digital Input, GND < VIN < V_{IL}	-10		+10	µA
I_{IH}	Input High Current	Any Digital Input, VIH < V_{IN} < V_{CC}	-10		+10	µA
I_{OZ}	Output Current in HIGH Impedance (tri-state)	All Digital Tri-state I/Os	-10		+10	µA

LINE INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{LI}	Differential Input Resistance	GND < LI_+, LI- < V_{CC}	200			kΩ
C_{LLO}	Load Capacitance	From LO+ to LO-			200	pF
V_{OS}	Differential Offset Voltage at L_{O+}, L_{O-}	Driving Binary 1s, 220Ω between LO+ and LO-	-20		20	mV

POWER DISSIPATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power Down Current	All Outputs Open-circuit			850	µA
$I_{CC}1$	Power Up Current	Device Deactivated (Note1)			16	mA

Note1: when the device is activated and driving a correct terminated line, ICC1 increases by several mA. A worst case data pattarn, consisting of all binary O'S increases ICC1 by apprximately 8mA.

ELECTRICAL CHARACTERISTICS (continued)

TRANSMISSION PERFORMANCE •

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Transmit Pulse Amplitude	Conform to all CCITT I430 requirenents using the specified transformer. (see transformer model)				
		R_L 220Ω between L_{O+} and L_{O-}	±1.4		±1.6	Vpk
	Transmit Pulse unbalance	0^+ reletive to 0^-			±5	%
	Input Pulse Amplitude	Differential between L_{I+} &L_{I-}	±175			mVpk

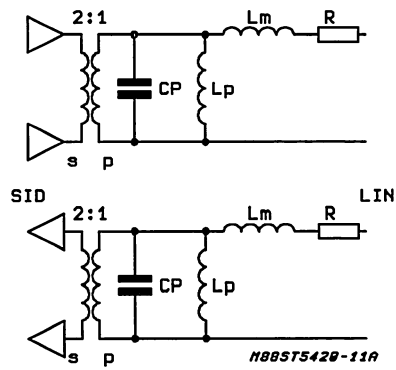
MASTERCLOCK

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	MCLK Frequency			15.36		MHz
	MCLK Frequency Tolerance		-100		100	ppm
	MCLK Input Clock Jitter				50	ns pk-pk
	Timing Recovery Jitter	BCLK Output Relative to MCLK at TE	-130		130	ns
t_{MH}, t_{ML}	Clock Pulse width High and Low of MCLK	$V_{IH} = V_{CC}$-0.5V, V_{IL} = 0.5V	20			ns
t_{MR}, t_{MF}	Rise Time and Fall Time of MCLK	Used as a logical input			10	ns

TRANSFORMER MODEL (all values are to be measured at 10kHz)

		Min.	Typ.	Max.	Unit
1:N	Primary to Secondary Turn Ratio	-1%	2	1%	
R	Primary Total DC Resistance		12		Ohm
Lp	Primary Inductance	22	30	37.5	mH
Lm	Primary Inductance with Secondary Shorted		16	20	mH
Cp	Primary Capacitance with Secondary Open			25	pF

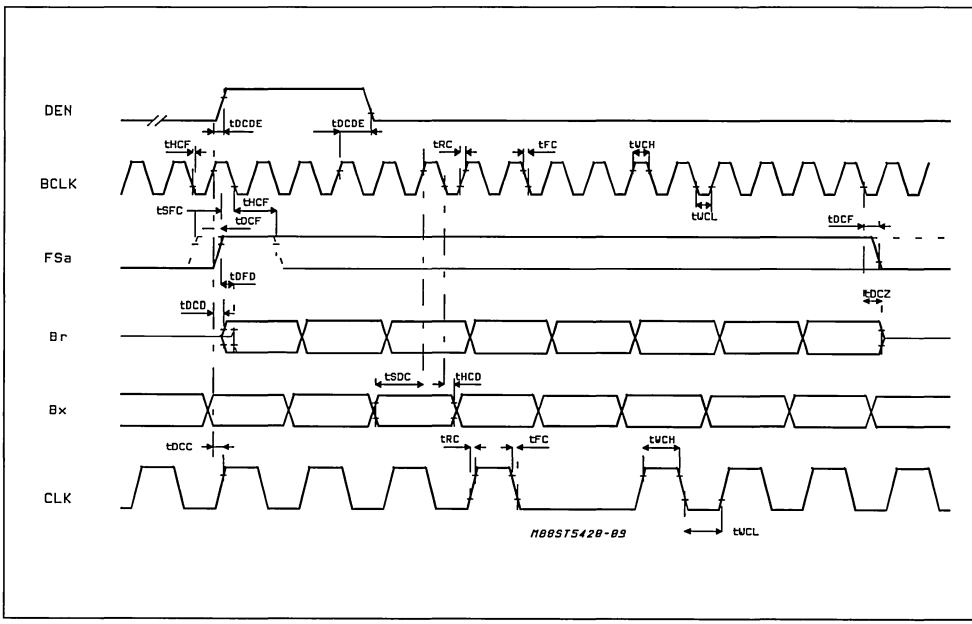
Figure 9: Transmit & Receive Transformer Model



TIMING SPECIFICATIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DCDE}	Delay Time BCLK High to DEN Transition	TE Mode only			30	ns
t_{HCF}	Hold Time BCLK Trans. to FSa Transition		0			ns
t_{RC}, t_{FC}	Rise & Fall Time BCLK				15	ns
t_{WCH}, t_{WCL}	BCLK width High & Low		60			ns
t_{SFC}	Setup Time FSa High to BCLK Low		70		BCLK -50	ns
t_{DCF}	Delay Time BCLK High to FSa HIGH	TE Mode only			30	ns
t_{DCD}	Delay Time BCLK High to DATA Valid		20		80	ns
t_{DFD}	Delay Time FSa High to Data Valid	Load 100pF. Apply only if FSa rises later than BCLK rising edge			80	ns
t_{DCZ}	Delay Time BCLK Low Data Invalid		50		120	ns
t_{SDC}	Setup Time Data Valid to BCLK Low		30			ns
t_{HDC}	Hold Time BCLK Low to Data Invalid		20			ns
t_{DCC}	Delay Time BCLK High to CLK High	TE and TES side modes only	0		30	ns

Figure 10: GCI Mode



APPLICATIONS INFORMATION

While the pins of ST5421 SID-GCI device are well protected against electrical misuse, it is recommended that the standard CMOS practise of applying GND to the device before any other connections, should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A power supply decoupling capacitor of 0.15F should be connected from this common point to V_{CC} as close as possible to the device pins.

CRYSTAL OSCILLATOR

The clock source for ST5421 may be provided with a commercially available crystal or an external clock source meeting the frequency requirements as explained in the following sections.

CRYSTAL SPECIFICATION

ST5421 SID-GCI clock source may be either a quartz crystal operating in parallel mode or an external signal source at 15.36MHz. The complete oscillator (crystal plus the oscillator circuit) must meet a frequency tolerance specification of 1 100ppm total to comply with the CCITT I.430 specification for TE applications.The frequency tolerance limits span the conditions of full operating temeprature range (commercial or industrial) and effects due to aging and part parameter variations.

The crystal is connected between pin 5 (MCLK/XTAL) and pin 6 (XTAL2), with a 33pF total capacitance from each pin to ground. The external capacitors must be mica or high-Q ceramic type. The use of NPO (Negative Positive Zero coefficient) capacitors is highly recommended to ensure tight tolerance over the operating temperature range. The 33pF capacitance includes the external capacitor plus any trace and lead capacitance on the board. Nominal frequency of 15.360MHz, frequency tolerance (accuracy, temperature and aging) less than 1.60ppm, with Rs = 150, CL= 20pF, parallel mode, C0 (shunt capacitance) 7pF.An external circuit may be driven directly from the pin XTAL2 (pin 6) provided that the load presented is greater than 50K shunted by a total of 33pF of capacitance. Crystal oscillator board layout is critical and should be designed with short traces that do not run parallel when in close proximity (to minimize coupling between adjacent pins). On multi-layered boards a ground layer should be used to prevent coupling from signals on adjacent board layers. Ground traces on either side of the high frequency trace also helps isolate the noise pickup.

EXTERNAL OSCILLATOR CONFIGURATION

An external 5V drive clock sourcxed may be connected to the MCLK (pin 5) input pin of ST5421. The nominal frequency should be 15.36MHz with a tolerance of 1 80ppm. The ST5421 SID provides a load of about 7pF at the MCLK input pin.

LINE TRANSFORMER REQUIREMENTS

The electrical characteristics of the pulse transformer for the ISDN "S" interface are defined to meet the output and input signal and the line isolation and characteristics as defined in CCITT reccommednation I.430. The transformer provides isolation for the line card or terminal from the line it lasi provides a means to transfer power to the terminalb over the S-loop via the "phantom" circuit created by center-tapping the line side windings. A transformer is used both at the transmit and the receive end of the loop. These notes specify the tolerances of a transformer that is employed with ST5421 to meet the CCITT recommendation on output pulse mask and impedance requirements.

LINE TRANSFORMER RATIO

The transmit and th receive transformers can be the same (with a winding ratio of 1:2) or optionally, the receive transformer could have a transformer ratio of 1:1. The primary of the transformer is connected to the S loop while the secondary is connected to the device.

EXTERNAL PROTECTION CIRCUITRY

Precautions are to be taken to ensure that ST5421 SID-GCI is protected against electrical surges and other interferences due to electromagnetic fields, power line faults and lightening discharge that may occur in the transmission medium. Protection circuits that are external to the device are recommended on both the primary and secondary sides of the line transformer.

DC BIAS CAPACITORS FOR ANALOG REFERENCE

Two decoupling capacitors (0.1µF mica) and 10µF (electrolytic) are connected between pin 19 of the device and its ground connection. These capacitors decouple the midpoint of a two-resistor potential divider (inside the device) and provide an internally buffered reference for the analog circuitry.

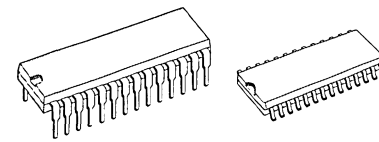
ST5421 EXCEEDING I.430 TRANSMISSION REQUIREMENTS

This ST5421 is designed with the goal of substantially exceeding the transmission performance requirements as specified in the I.430. This is made possible in the ST5421 SID design by employing superior analog front end designs. For example, in the receive path, an analog prefiter removes <200kHz noise signals, which is then followed by an adaptive line equalizer to accomodate varying line conditions with superior performance. A continuously tracking adaptive threshold circuit provides the slicing levels for the detection circuits for correct interpretation of transmission bits even on long lossy loops. This implementation results in longer ranges of S interface cables compared to I.430 requirements.

ISDN HDLC AND GCI CONTROLLER

ADVANCE DATA

- MONOLITHIC ISDN ORIENTED HDLC AND GCI CONTROLLER.
- GCI AND µW/DSI COMPATIBLE.
- FULLY CONTROLLING GCI AND GCI-SCIT M & C/I CHANNELS MANAGEMENT.
- FULLY SUPPORTING LAPB AND LAPD PROTOCOL ON B OR D CHANNEL.
- EASILY INTERFACEABLE WITH ANY KIND OF STANDARD NON MULTIPLEXED OR MULTIPLEXED BUS MICROPROCESSOR.
- DMA ACCESS WITH MULTIPLEXED BUS µP
- CAN HANDLE AND STORE AT THE SAME TIME TWO FRAMES IN TRANSMISSION (64bytes FIFO Tx) AND EIGHT FRAMES IN RECEPTION (64bytes FIFO Rx)
- COMPATIBLE WITH ALL THE SGS-THOMSON ISDN PRODUCT FAMILY.



DIP28 SO28

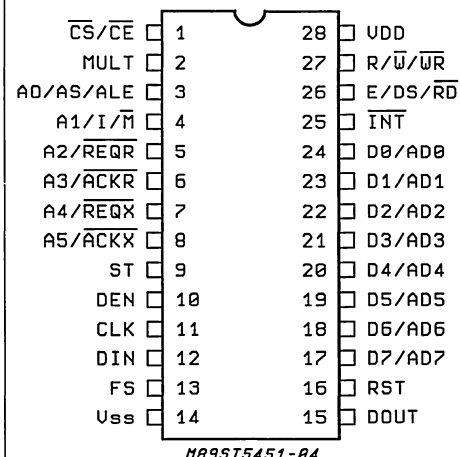
ORDERING NUMBERS:

ST5451N ST5451D

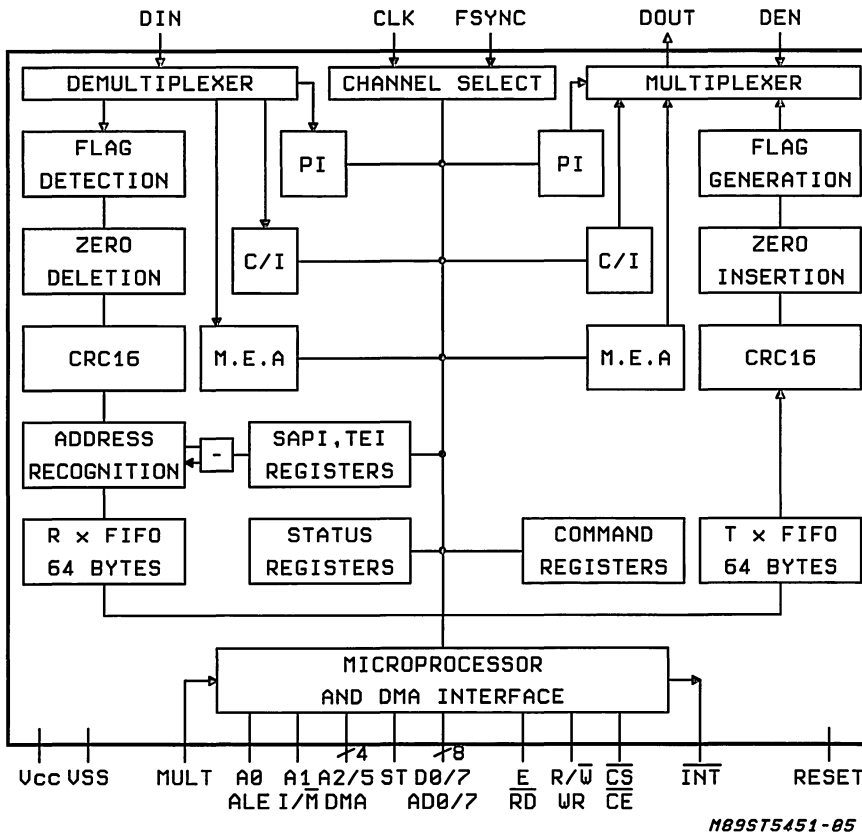
GENERAL DESCRIPTION

ST5451 HDLC and GCI controller is a CMOS circuit fully developed by SGS-THOMSON and diffused in advanced 1.2 µm HCMOS3 technology.
The device is intended to be used mainly in ISDN applications, in Terminal (TE) and in Line Terminations (LT).
ST5451 can handle HDLC packets either on 16Kbit/s D channel or 64 Kbit/s B channel; it can work with a wide range of PCM signals going from GCI (General Circuit Interface) to DSI (Digital System Interface) to any PCM-like stream.
ST5451 is a complete GCI controller designed to comply with the GCI and GCI-SCIT (Special Circuit Interface for Terminal) completely handling Monitor (M) and Command/Indicate (C/I) channels.
ST5451 can be easily controlled by many different kind of microprocessors or microcontrollers having either non-multiplexed or multiplexed bus structure.
ST5451 can be used in connection with ST5420/1 S Interface Devices (SID-µW and SID-GCI) and ST5080 Programmable ISDN Combo (PIC) in Terminals and with ST5410 U Interface Device (UID) in Line Terminations.

PIN CONNECTION (Top view)



BLOCK DIAGRAM



PIN DESCRIPTION

NAME	PIN	TYPE	FUNCTION
$\overline{CS}$	1	I	Chip Select. A low level enables ST5451 for read/write operations.
$\overline{INT}$	25	O	Interrupt request is asserted by ST5451 when it request a service. Open drain output.
MULT	2	I	Multiplexed Bus. Indicates the µP bus interface selected. MULT = 1: multiplexed bus and DMA available. MULT = 0: address and data bus separated.
I/$\overline{M}$	4	I	Intel/Motorola. When MULT = 1 this pin selects either Intel or Motorola 6805 bus.

DEMULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 0)

NAME	PIN	TYPE	FUNCTION
A0/A5	3-8	I	Address Bus. To transfer addresses from µP to ST5451.
D0/D7	17-24	I/O	Data Bus. To transfer data between µP and ST5451.
R/$\overline{W}$	27	I	Read/Write. "1" indicates a read operation; "0" a write operation.
E	26	I	Enable. Read/write operations are synchronized with this signal; its falling edge marks the end of an operation.

MULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 1 I/$\overline{M}$ = 1)

NAME	PIN	TYPE	FUNCTION
AD0/AD7	17-24	I/O	Address Data Bus. To transfer addresses and data between µP and ST5451.
$\overline{WR}$	27	I	Write. This signal indicates a write operation.
$\overline{RD}$	26	I	Read. This signal indicates a read operation.
ALE	3	I	Falling edge latches the address from the external A/D Bus.

MULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 1; I/$\overline{M}$ = 0)

NAME	PIN	TYPE	FUNCTION
AD0/AD7	17-24	I/O	Address Data Bus. To transfer addresses and data between µP and ST5451.
R/$\overline{W}$	27	I	Read/Write. "1" Indicates a write operation; "0" a write operation.
DS	26	I	Data Strobe. Read/Write operations are synchronized with this signal: its falling edge marks the end of an operation.
AS	3	I	Address Strobe. Falling edge latches the address from the external A/D Bus.

DMA (direct memory access): only when MULT = 1

NAME	PIN	TYPE	FUNCTION
$\overline{\text{DMA REQ X}}$ DMA REQ R	7 5	O O	Direct Memory Access Requests: these outputs are asserted by the device to request an exchange of byte from the memory.
$\overline{\text{DMA ACK X}}$ DMA ACK R	8 6	I I	Direct Memory Access Acknowledge: these inputs are asserted by the DMA controller to signal to the HDLC controller that a byte is being transferred in response to a previous transfer request.

GCI INTERFACE

NAME	PIN	TYPE	FUNCTION
D_{OUT}	15	I/O	Data output for B and D channels. In GCI mode it outputs B1, B2, M and C/I channels. In TE mode (GCI-SCIT) it can invert to input data for M' and C/I' channels (See Table 2).
D_{IN}	12	I/O	Data input for B and D channels. In GCI mode it inputs B1, B2, M and C/I channels In TE mode (GCI-SCIT) it can invert to output data for M' and C/I' channels (See Table 2).
C_{LK}	11	I	Data Clock It determines the data shift rate for GCI channels on the module interface.
FS	13	I	Frame synchronization. This signal is a 8 kHz signal for frame synchronization. The front edge gives the time reference of the first bit in the frame.
DEN	10	I	Data Enable. In TE mode, this pin is a normally low input pulsing high to indicate the active bit times for D channel transmit at DOUT pin. It is intended to be gated with CLK to control the shifting of data from HDLC controller to S interface device.

NON GCI INTERFACE

NAME	PIN	TYPE	FUNCTION
D_{OUT}	15	O	Data output. Digital output for serial data. Three modes: - HDLC Protocol multiplexed link - HDLC Protocol non multiplexed link - Non HDLC protocol (transparent Mode).
D_{IN}	12	I	Data input. Digital input for serial data. Three modes (See D_{OUT}).
C_{LK}	11	I	Data Clock. It determines the data shift rate. Two modes: Single or double bit rate.
FS	13	I	Frame synchronization. Used in mode HDCL protocol multiplexed link. Don't care in other modes. The rising edge gives the time reference of the first bit of the frame.
DEN	10	I	Data Enable. When high, enable the data transfer. on D_{OUT}

OTHERS

NAME	PIN	TYPE	FUNCTION
V_{DD}	28	I	Positive power supply = 5V ±5%
V_{SS}	14	I	Signal ground
R_{ST}	16	I	Reset
ST	9	I	Special Test. (Reserved) must be tied to V_{SS}

2 - FUNCTIONS

2 - 1 - Basic HDLC Functions

2 - 1 - 1 - In Receive Direction:

- Channel selection
  In GCI channel B1 or B2 or D may be selected. B1 or B2 may be selected without M and C/I channels
- Flag detection
  A zero followed by six consecutive ones and another zero is recognized as a flag
- Zero delete
  A zero, after five consecutive ones within an HDLC frame, is deleted
- CRC checking
  The CRC field is checked according to the generator polynomial

$$X^{16} + X^{12} + X^5 + 1$$

- Check for abort
  Seven or more consecutive ones are interpreted as an abort flag
- Check for idle
  Fifteen or more consecutive ones are interpreted as "idle"
- Minimum lenght checking
  HDLC frames with less than n bytes between start and end flag are ignored: allowed values are $3 \leq n \leq 6$.

This value is set by a programmable register

- Address Field recognition
  4 SAPI and/or 3 TEI may be recognized. Several programmable registers indicate the recognized address types.

2 - 1 - 2 - In Transmit Direction:

- Shift control in TE mode
  D channel data are signalled by DEN pin.
- Flag generation
  A flag is generated at the beginning and at the end of every frame.
- Zero insert
  A zero is inserted after five consecutive ones within an HDLC frame
- CRC generation
  The CRC field of the transmitted frame is generated according to the generator polynomial

$$X^{16} + X^{12} + X^5 + 1$$

- Abort sequence generation
  An HDLC frame may be terminated with an abort sequence under microprocessor control

- Interframe time fill
  Flags or idle (consecutive ones) may be transmitted during the interframe time. A programmable bit selects the mode.

2 - 2 - FIFO Structure
2 - 2 - 1 - Receive FIFO Structure
In receive direction, a 64 byte FIFO memory is used. It is divided in 8 blocks of 8 bytes automatically chained.

In case of a frame length of 64 bytes or less, the whole frame can be stored in the FIFO. After the first 32 bytes have been received µP is interrupted and may read the available data.

In case of frames longer than 64 bytes, the µP is interrupted to read out the FIFO by 32 byte block.

In case of several short frames, up to eight may be stored inside the FIFO. After an interrupt, one frame is available for the µP. The eventual other seven frames are queued and transferred one by one.

2 - 2 - 2 - Transmit FIFO Structure
In transmit direction, a 64 byte FIFO memory is used, structured in 2 blocks of 32 bytes. ST5451 is requested to transmit after 32 bytes have been written into the FIFO.

If a transmission request does not include a message end, the HDLC controller will request the next data block by an interrupt.

2 - 3 - Microprocessor Interface
Three types of microprocessor interfaces are available (MULT and I/$\overline{M}$ control pins set the desired interface).
- Motorola non multiplexed families.
- Motorola multiplexed family (6805 type)
- Intel family.

You can connect ST5451 to a Direct Memory Access Controller as MC68440 or MC6450 (dual or quad channels).
A programmable register indicates DMA Interface enabling.

TABLE 1 - ST5451 Internal Registers

Address Hexa	Read	Write
00	Receive FIFO	Transmit FIFO
1F	-	-
20	ISTA0	ISTA0
21	ISTA1	ISTA1
22	ISTA2	ISTA2
23	STAR	CMDR
24	MODE	MODE
25	RFBC	TSR
26	CA	CA
27	CB	CB
28	CC	CC
29	CD	CD
2A	CE	CE
2B	CF	CF
2C	CIR1	CIX1
2D	CIR2	CIX2
2E	MONR1	MONX1/0
2F	-	MONX1/1
30	MONR2	MONX2/0
31	-	MONX2/1
32	-	MASK0
33	-	MASK1
34	-	MASK2
3E	CCR	CCR

TABLE 2 - CHANNEL ASSIGNMENT SELECT

CF REGISTER								C/I		M		8KB/s		16KB/s		56KB/s		64KB/s		C/I'		M'		CI*	
TE	MAS /SSC	CCS	CMS /SC	PI	VZ DOUT	MSD1	MSD0	RX	TX	RX	TX	RX	TX	DR	DX	RX	TX	RX	TX	RX	TX	RX	TX	TX	
X	X	X	X	X	X	X	0	RX ON DIN TX ON DOUT																	CONTINUOUS MODE
X	X	0	0	X	X	0	1							DIN	DOUT										
X	0	0	1	X	X	0	1					DIN (1)	DOUT (1)												MULTIPLEXED NON GCI MODE
X	1	0	1	X	X	0	1					DIN (2)	DOUT (2)												
X	X	1	0	X	X	0	1											DIN	DOUT						
X	0	1	1	X	X	0	1					DIN (3)	DOUT (3)												
X	1	1	1	X	X	0	1									DIN (4)	DOUT (4)								
1	1	0	0	0	0/1	1	1	DIN	DOUT	DIN	DOUT			DIN	DOUT										TERMINAL GCI MODE (D MASTER)
1	1	0	1	0	0/1	1	1	DIN	DOUT (6)	DIN	DOUT			DIN	DOUT (6)									DOUT (6)	
1	1	0	0	1	0/1	1	1	DIN	DOUT	DIN	DOUT			DIN	DOUT					DOUT (5)	DIN (5)	DOUT (5)	DIN (5)		
1	1	0	1	1	0/1	1	1	DIN	DOUT (6)	DIN	DOUT			DIN	DOUT (6)					DOUT (5)	DIN (5)	DOUT (5)	DIN (5)	DOUT (6)	
1	0	0	0	0	0/1	1	1	DIN	DOUT					DIN	DOUT										TERMINAL GCI MODE (D SLAVE)
1	0	0	1	0	0/1	1	1	DIN	DOUT (6)					DIN	DOUT (6)									DOUT (6)	
1	0	0	0	1	0/1	1	1	DIN	DOUT					DIN	DOUT					DIN	DOUT	DIN	DOUT		
1	0	0	1	1	0/1	1	1	DIN	DOUT (6)					DIN	DOUT (6)					DIN	DOUT	DIN	DOUT	DOUT (6)	
1	X	1	0	0	0/1	1	1	DIN	DOUT									DIN	DOUT						TERMINAL GCI MODE (B1 or B2)
1	0	1	1	0	0/1	1	1	DIN	DOUT			DIN (3)	DOUT (3)												
1	1	1	1	0	0/1	1	1	DIN	DOUT							DIN (4)	DOUT (4)								
1	X	1	0	1	0/1	1	1	DIN	DOUT									DIN	DOUT	DIN	DOUT	DIN	DOUT		
1	0	1	1	1	0/1	1	1	DIN	DOUT			DIN (3)	DOUT (3)							DIN	DOUT	DIN	DOUT		
1	1	1	1	1	0/1	1	1	DIN	DOUT							DIN (4)	DOUT (4)			DIN	DOUT	DIN	DOUT		
0	X	0	X	X	0/1	1	1	DIN	DOUT	DIN	DOUT			DIN	DOUT										REGULAR GCI MODE

(1) FIRST BIT OF 16KB/S CHANNEL SELECTED
(2) SECOND BIT OF THE 16KB/S CHANNEL SELECTED
(3) LAST BIT OF THE 64KB/S CHANNEL SELECTED
(4) SEVEN FIRST BITS OF THE 64KB/S CHANNEL SELECTED
(5) TO INSURE THE EXCHANGING OF MESSAGES WITH THE OTHERS
ST5451 PERIPHERAL DEVICES THE MASTER DEVICE USES THE C/I' AND M' CHANNELS ON
DIN PIN FOR THE OUTPUT SERIAL DATA DOUT PIN FOR THE INPUT SERIAL DATA
(6) ONLY THROUGH THE ACCESS PROCEDURE

THIS TABLE SHOWS THE USED CHANNELS ACCORDING TO THE CONFIGURATION OF THE CF REGISTER AND THE PINS USED (DIN, DOUT) WHERE THE RECEIVERS RX AND THE TRANSMITTERS TX GET OR PUT THE DATA

H96ST5451-31

3 - REGISTER DESCRIPTION

For all the register pictures MSB is on the left and LSB on the right
If not otherwise stated bit are considered active at 1.

FIFOS

RFIFO (read), XFIFO (write).

The address range of the two FIFOs are identical. All the 32 addresses give access to the "current" FIFO location.

When the closing Flag of a receive frame is detected, a status byte is available in the RFIFO. This byte has the following format:

RBC	RDO	CRC	RAB	0	0	0	0

RBC Receive Byte Count.
The length of the received frame is n time 8 bits (n=3,4,5,...)

RDO Receive Data Overflow
A part of the frame has not been lost because the receive FIFO was full

CRC CRC Check
The received CRC bytes were not correct

RAB Receive Abort
The received frame was not aborted

A status byte equal to D0H indicates a correctly received frame

ISTA0 Interrupt Status Register 0
After RESET 10H

RME	RPF	RFO	XPR	XDU	EXI2	EXI1	0

RME Receive Message End
One complete frame of length less than or equal to 32 bytes, or the last part of a frame of length greater than 32 bytes is stored in the RFIFO.

RPF Receive Pool Full
32 bytes of a frame are in RFIFO. The frame is not yet completely received.

RFO Receive Frame Overflow
A complete frame was lost because no storage space was available in the RFIFO.

XPR Transmit Pool Ready
One data block (32 bytes max) may be entered into the XFIFO.

XDU Transmit Data Underrun
A transmitted frame was terminated with an abort sequence because no data were available for transmission in XFIFO and no XME command was issued. It is not possible to transmit frame when that interrupt remains unacknowledged and XRES has not been set.

EXI2 Extended Interrupt 2
The interrupt reason is indicated in register ISTA2

EXI1 Extented Interrupt1
The interrupt reason is indicated in register ISTA1.

ISTA1 Interrupt Status Register 1
After RESET 01H
(GCI mode only)

0	0	CIC1	EOM1	XAB1	RMR1	RAB1	XMR1

CIC1 Comman/Indicate Change
A change in the value of CIR1 is detected

EOM1 End of Message 1 (monitor channel)
MON1 has received an end of message.

XAB1 Monitor Transmit ABORT
The received byte has not been detected in two successive frames.
MON1 has sent an ABORT (A bit) to the remote transmitter.

RMR1 Receive Monitor Register 1 ready
A byte has been received in register MONR1.

RAB1 Receive Abort
MON1 received an ABORT from the remote receiver.

XMR1 Transmit Monitor Register 1 ready
A byte can be stored in register MONX1

ISTA2 Interrupt Status Register 2
After RESET 01H
(GCI and TE mode only)

0	0	CIC2	EOM2	XAB2	RMR2	RAB2	XMR2

CIC2 Command/Indicate Change
A change in the value of CIR2 is detected.

EOM2 End of Message 2 (monitor channel)
MON2 has received an end of message.

XAB2 Monitor Transmit ABORT
The received byte has not been detected in two successive frames.
MON2 has sent an ABORT (A bit) to the remote transmitter.

RMR2 Receive Monitor Register 2 ready
A byte has been received in register MONR2.

RAB2 Receive ABORT
MON2 received an ABORT from the remote receiver.

XMR2 Transmit Monitor Register 2 ready
A byte can be stored in register MONX2.

MASK0, MASK1, MASK2
After Reset FF; the three mask registers MASK0, MASK1, MASK2 are associated respectively to the three interrupt registers ISTA0, ISTA1,and ISTA2.
Each interrupt source in ISTA registers can be selectively masked by setting to "1" the corresponding bit in MASK1. Interrupt sources (masked or not) are indicated when ISTA is read by the microprocessor. When an interrupt source is not masked, $\overline{INT}$ goes low.

STAR Status Register
After Reset 48H

XDOV	XFW	IDLE	RLA	DCIO	0	0	0

XDOV Transmit Data Overflow
More than 32 bytes have been written into the XFIFO.

XFW XFIFO Write enable
Data can be entered into the XFIFO.

IDLE IDLE State
15 or more consecutive ones have been detected on the input data line.

RLA Receive Line Active
Frames or interframe flags are being received

DCIO D and C/I Channels are occupied

CMDR Command Register
After Reset 00

XHF	XME	RMC	RMD	RHR	XRES	M2RES	M1RES

XHF HDLC frame transmission can start.

XME Transmit Message End
The last part of the frame was entered in XFIFO and can be sent.

RMC Receive Message Complete
Reaction to RPF or RME interrupt. The received frame (or one pool of data) has been read and the corresponding RFIFO is free.

RMD Receive Message Delete
Reaction to RPF or RME interrupt. The entire frame will be ignored. The part of frame already stored is deleted.

RHR Reset HDLC receiver

XRES Reset HDLC transmitter
XFIFO is cleared and the transmitted frame (if any) is aborted.

M2RES Monitor 2 Reset
Reset MONITOR and C/I channels (TX and RX).

M1RES Monitor 1 Reset
Reset MONITOR and C/I channels (TX and RX).

* For the four first bits (XHF, XME, RMC, RMD), the reset is done by the device; the other bits level sensitive

MODE HDLC Mode Register
After Reset 00

DMA	FL1	FL0	ITF	RAC	CAC	NHF	FLA

DMA DMA Interface activation

FL1/0 Frame Length
Minimum frame length accepted

	FL1	**FL0**
3 bytes	0	0
4 bytes	0	1
5 bytes	1	0
6 bytes	1	1

ITF InterframeTime Fill
ITF= 1 : Flags are transmitted
ITF= 0 : IDLE is transmitted

RAC RAC= 1 : Activate RX
RAC= 0 : deactivate RX

CAC Channel Activation
CAC = 1 : Activate RX and TX
CAC = 0 : deactivate RX and TX

NHF HDLC Function Select
NHF = 1 : disable HDLC function

FLA Flag
FLA = 1 : transmit shared flags
FLA = 0 : transmit two flags between consecutive frames.

RFBC Receive Frame Byte Counter
After reset 00

RDC7	RDC6	RDC5	RDC4	RDC3	RDC2	RDC1	RDC0

RDC 0/7 Receive Data Count

Total number of bytes of received frame without CRC.

RDC 0/4 Indicate the number of bytes in the current block available in RFIFO.

RDC 5/7 Indicate the number of 32 bytes blocks received. If the frame exceeds 223 bytes, RDC 5/7 hold the value "111", only RDC 4/0 continue to count modulo 32.

See Table 3.

The contents of the register are valid after an RME interrupt. The µP must read N+1 bytes to transfer the number of bytes received and the status byte into the memory.

CIX1 Command/Indicate Transmit Register 1
After reset FFH
(GCI only)

1	1	1	1	C1	C2	C3	C4

C1, C2, C3, C4:

Code to be transmitted permanently in the outgoing GCI C/I channel.

CIR1 Command/Indicate Receive Register 1
After reset FFH
(GCI only)

1	1	1	1	C1	C2	C3	C4

C1, C2, C3, C4:

Incoming GCI C/I channel.

MONX1 Monitor Transmit Register 1
After reset FFH
(GCI only)

M1	M2	M3	M4	M5	M6	M7	M8

The value written in MONX1 is transmitted in the outgoing Monitor channel according to GCI transfer protocol. XMR1 interrupt indicates when MONX1 is again available.

MONR1 Monitor Receive Register 1
After reset FFH
(GCI only)

M1	M2	M3	M4	M5	M6	M7	M8

The value read from MONR1 gives the value of the byte received in the monitor channel according to GCI transfer protocol. RMR1 interrupt indicates when a new byte is available in MONR1 register.

CIX2 Command/Indicate Transmit Register 2
After Reset FFH
(GCI and TE mode only)

1	1	P1	P2	P3	P4	P5	P6

P1/P6 Code transmitted permanently in the 2nd GCI C/I channel.

CIR2 Command/Indicate Receive Register 2
After reset FFH
(GCI and TE mode selected only)

1	1	P1	P2	P3	P4	P5	P6

P1/P6 The contents of the 2nd C/I channel; they are the different requests received from TE peripheral devices to µP.
Six peripherals can make a simultaneous request.

MONX2 Monitor Transmit Register 2
After reset FFH
(GCI and TE mode only)
The value written in MONX2 is transmitted in the 2nd GCI M channel to a peripheral (if PI= 1; register CF).

TABLE 3

N (number of bytes in the frame received without CRC)	Counter 765	Counter 43210	n (number of 32 bytes blocks received)
N	n	m	n
1 Min	000	00001	0
2	000	00010	0
3	000	00011	0
30	000	11110	0
31	000	11111	0
32	001	00000	1
33	001	00001	1
62	001	11110	1
63	001	11111	1
64	010	00000	2
222	110	11110	6
223	110	11111	6
224	111	11111	7
256	111	00000	7
257	111	00001	7
-	111	-	7

MONR2 Monitor Receive Register 2
After reset FFH
(GCI and TE mode only)
The value read from MONR2 gives the value of the byte received from M channel in 2nd GCI channel.

TSR Time Slot Register
After reset 00

TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0

In GCI mode (MDS1= 1 in CF Register)
a) CCS=1 in CF Reg. (64 Kbit/s)
Then: TSR2 indicates B1 or B2 TSR4/7 indicate position of GCI channel
b) CCS=0 in CF Reg. (16 Kbit/s)
Then: TSR4/7 indicate position of GCI and its D channel

In Multiplexed Mode
(MDS1=0 in CF Register)
a) CCS=1 in CF Reg. (64 Kbit/s)
Then: TSR2/7 indicate channel position in the 64 time slots multiplex
b) CCS=0 in CF Reg. (16 Kbit/s)
Then: TSR0/7 indicate channel position in the 256 time slots multiplex.

CA Configurationn Register A
After reset 00

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0

CA0	SAPI 0 is recognized	CA0 = 1
CA1	SAPI 63	CA1 = 1
CA2	SAPI x	CA2 = 1
CA3	SAPI y	CA3 = 1
CA4	TEI 127	CA4 = 1
CA5	TEI z	CA5 = 1
CA6	TEI t	CA6 = 1
CA7	Address filter active	CA7 = 1

CB Configuration register B
After reset 00
Content of CB indicate SAPI x value
High Order 6 Bits

SAPI	0	0

CC Configuration Register C
After reset 00
Content of CC indicate SAPI y value
High Order 6 Bits

SAPI	0	0

CD Configuration Register D
After reset 00
Content of CD indicate TEI z value.

7 High Order Bits

TEI	0

CE Configuration Register E
After reset 00
Content of CE indicate TEI t value.

7 High Order Bits

TEI	0

CF Configuration Register F
After 00

TE	MAS/SSC	CCS	CMS/SC	PI	VZDOUT	MDS1	MDS0

TE TE mode
TE = 1 : the frame is constitued by three GCI channels (GCI-SCIT)

MAS/SSC If CCS = 0, TE = 1, MDS0 and MDS1 = 1 (i.e. GCI mode, TE mode, 16 Kbit/s)
MAS/SSc is MAS and:
MAS = 0 means "Slave device"
MAS = 1 means "Master device"

If SC = 1 (i.e. a sub-channel is selected) MAS/SSC is SSC; if 16Kb is selected SSC chooses between first on second bit of the stream while, if 64Kb is selected SSC chooses between first or last seven bits of the stream (see TABLE 2 and CMS/SC)

CCS Channel Capacity Selection
CCS = 1: 64 Kb/s
CCS = 0: 16 Kb/s.

CMS/SC If CCS = 0, TE = 1, MDS0 and MDS1 = 1 (i.e. GCI mode, TE mode, 16Kbit/s)
CMS/SC is CMS (Contention mode selection) and:
CMS = 1 means "D and C/I channel access procedure active"
CMS = 0 means "D and C/Z channel access procedure active"

If CCS = 1 and TE = 1 CMS/SC is SC (Subchannel) and:
SC = 0 means "16Kbit/s or 64Kbit/s is used"
SC = 1 means "an 8Kbit/s or 56Kbit/s subchannel inside a 16Kbit/s or 64kbit/s is used" (see MAS/SSC)

PI Peripheral Interface (only if TE=1)
PI = 1: CIX2, CIR2, MONX2, MONR2, active

VZDOUT When level 1 device is inactive (i.e. CIR1 = DI = 1111) and GCI has to be waken up (i.e. TIM = 0000 in CIX1), DOUT is set to zero requiring FS and CLK if VZ DOUT=1.

MDS1 Mode Bit 1
MDS1 = 1:GCI mode
MDS1 = 0: Multiplexed mode

MDS0 Mode Bit 0
MDS0 = 1: Multiplexer and Demultiplexer are active.
MDS=0 No multiplexer.

CCR Configuration Register 00
After reset 00

TLP	ADDR	AD3	AD2	AD1	AD0	CRS	TRI

TLP Test Loop
TLP = 1: The transmitter is internally connected to the receiver; the transmit output is not activated. The digital interface must be activated to provide the bit clock and frame Synchro.

ADDR Address Recognized
If TE = 1 and PI = 1
ADDR = 1: The first byte received in MONR2 is compared with AD0/3. If equal the message is accepted, otherwise is ignored.
ADDR = 0: The message is always accepted.

AD0/3 When PI = 1, is the component address.

AD0/2 Address bit used to access D and C/I channels (TE = CMS =1, CCS = 0).

CRS Clock Rate Selection
CRS = 1: Clock frequency is twice the data rate (GCI).
CRS = 0: Clock frequency and data rate are identical.

TRI Tristate
TRI = 1: DOUT in tristate
TRI = 0: DOUT in open drain.

4 - WORKING PROCEDURES

4 - 1 - RECEIVE FRAME

Recognized frame (by means of SAPI and/or TEI identification), having a minimum length is stored in the RFIFO with all bytes between the opening flag and CRC field.

When the frame is less than or equal to 32 bytes, is transferred in one block, and just after the receiving completion interrupt (RME), a status byte is appended at the end. The frame and its status byte remain stored until µP acknowledgement (RMC).

When the frame is longer than 32 bytes, blocks of 32 bytes plus one remainder block of lenght 1 to 32 are transferred to the microprocessor. The receiving 32 byte block generates a RPF interrupt and the data in RFIFO remains valid until µP acknowledgement (RMC).

The µP can ignore a received frame by meaning RMD (Receive Memory Delete), reaction to RPF or RME. The part of frame already stored is deleted and the remainder frame is ignored by the HDLC Controller.

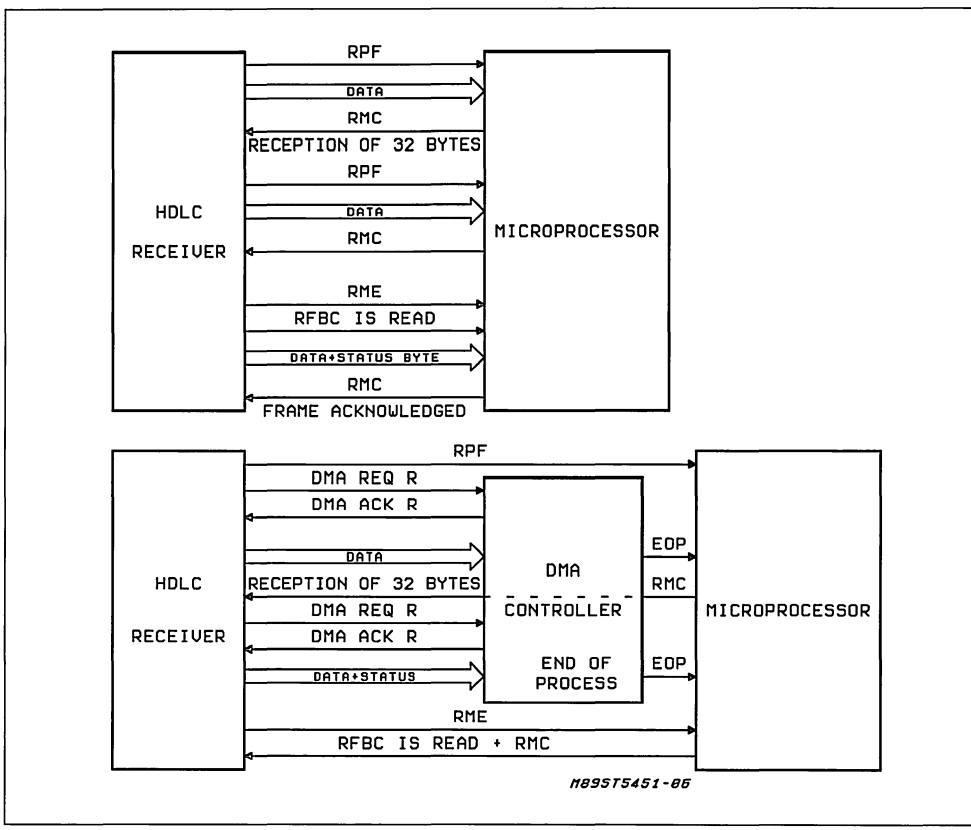
The last block of the frame generates the RME interrupt.

RFBC register bits 0 to 4 indicate the number of bytes currently stored in the RFIFO. Bits 5 to 7 indicate the total number of 32 byte blocks already received. Bits 5 to 7 do not overflow. When the counter status 7 has been reached, it indicates a frame length greater than 223 bytes (see Table 3).

RFBC register is valid only after the RME interrupt and remains valid until RMC acknowledgement by µP.
At each read access by the µP, RFBC 5/7 bits remain unchanged, RFBC 0/4 bits are decreased to reach value 0 when the whole block is read.

Interrupts are queued inside the device. They are sent one by one to the microprocessor after each acknowledgement RMC. If a frame is lost because the RFIFO was full, a RFO interrupt is generated.

Figure 1: Receiving of an HDCL frame



4- 2 - TRANSMIT FRAME

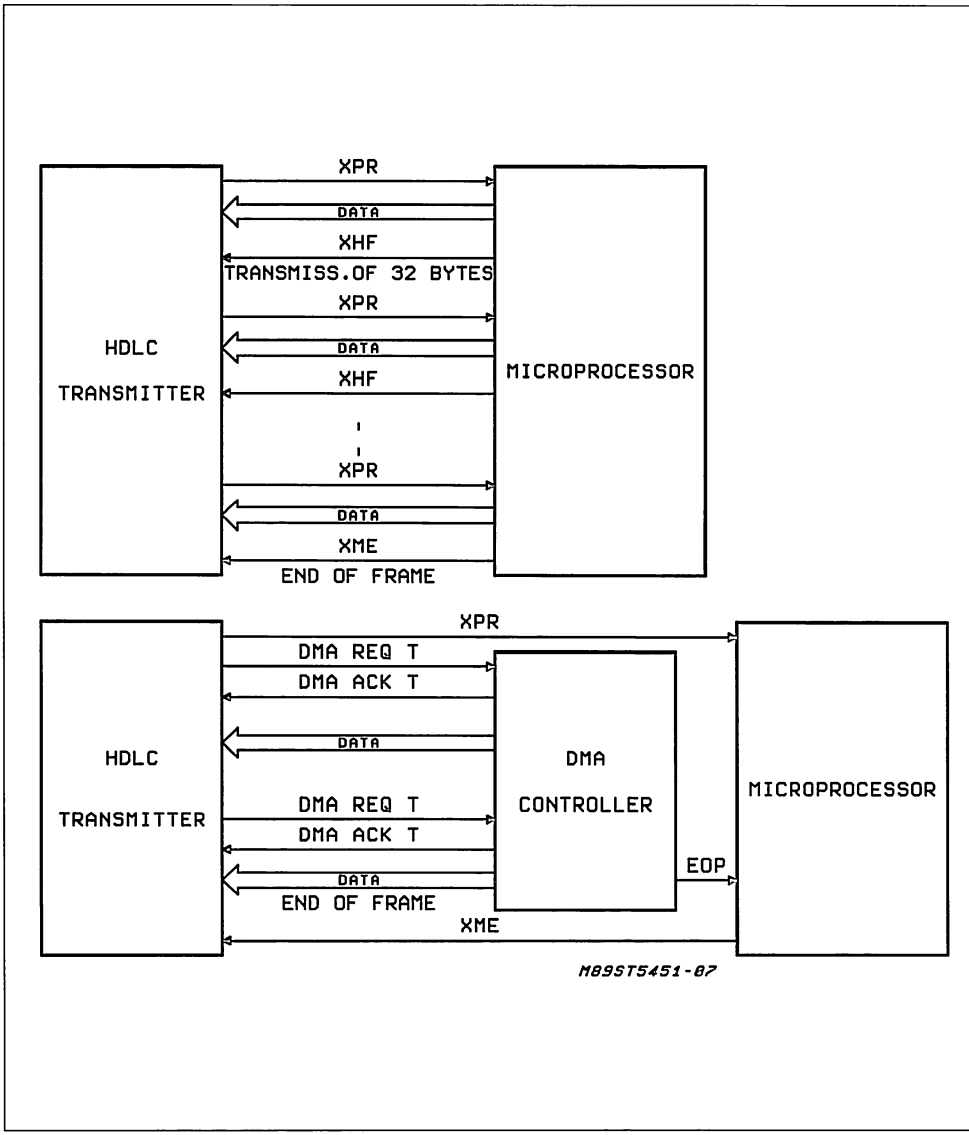
After polling bit XFW or after a XPR interrupt, up to 32 bytes may be stored in XFIFO. Transmission begins after that XHF command is issued by µP. ST5451 will request another data block by an XPR interrupt if the XFIFO contains less than 32 bytes.

When XME is set, all remaining XFIFO bytes are transmitted, the CRC field and the closing flag are added. The HDLC controller then generates a new XPR interrupt.

If the XFIFO becomes empty while XME command has not been set, an abort sequence is generated, followed by interframe time fill and XDU interrupt is generated.

A frame may be aborted by XRES command as well.

Figure 2: Transmission of an HDCL frame



4 - 3 - COMMAND/INDICATE PROCEDURE

The exchange of information in the C/I channel runs as follows:
The two circuits (i.e. ST5421 and ST5451) connected on the GCI interface send one each other a permanent four bit command code in C/I field.

RECEIVE C/I

The ST5451 stores on every frame the four bits of C/I channel coming from level 1 circuit in a first register CIR. This value is compared with the previous one. If a one new appears during two consecutive frames, this new value is loaded in register CIR1 and a CIC1 interrupt is generated.

TRANSMIT C/I

The transmit register CIX1 can be written at any time by the µP. Its content is continuously sent in the C/I channel.

Note: The TIM command (0000) forces a low level on DOUT, if CIR1 = DI (1111) when VZ DOUT = 1 to require FS and CLK.

4 - 4 - MONITOR CHANNEL

The GCI Monitor channel procedure allows full duplex data transmission with acknowledgement using A bit.

MESSAGE RECEIVING

An interrupt (bit RMR1 in ISTA1 register) is generated when a new byte is available in register MONR1.
ST5451 generates an interrupt bit (XAB1 in ISTA1) if it does not read twice the same bytes meanwhile sending an ABORT to the remote transmitter.
It performs an interrupt (EOM in ISTA1) also when it has received an End Of Message. Acknowledgement to remote transmitter is sent if:
- the byte was received twice with the same value
- the microprocessor reads the previous byte stored in register MONR1.
This procedure performs flow control between S interface device and µP.

MESSAGE TRANSMISSION

ST5451generates an interrupt (XMR1 in ISTA1) when register MONX1 is available.
Writing register MONX1/0 generates a message transmission. When the last byte is stored in the register MONX1/1, ST5451 sends the End of Message to remote receiver. If an Abort is received, one interrupt (RAB1) is generated.

4 - 5 - M' and C/I' CHANNELS

The procedure allows a full duplex data transmission between microprocessor and the peripheral devices connected on C/I' local and M' channel through GCI-SCIT channel 1.
Receive Interrupt on C/I' (DOUT is an input).
A new value on C/I' indicates to ST5451 master that one device in the terminal wants to send a message. Up to six peripherals may generate such an interrupt to the microprocessor.
ST5451 writes at every frame the six bits of C/I' channel coming from peripherals in register CIR'.
This value is compared with the previous one and if a new one appears during two consecutive frames, is loaded in register CIR2 and CIC2 interrupt (ISTA2 register) is generated.
µP may send a message on M' channel (DIN becomes an output) to allow the peripheral device to transmit.

MESSAGE TRANSMISSION ON M' CHANNEL

ST5451 sets interrupt XMR2 (ISTA2 register) if register MONX2/0 is available. Writing MONX2/0 generates a message transmission. When the last byte is stored in register MONX2/1, ST5451sends End of Message to remote peripheral.
If an ABORT is received, interrupt RAB2 (ISTA2 register) is issued. Then microprocessor may send its message again.

MESSAGE RECEPTION ON M' CHANNEL

Interrupt bit RMR2 (ISTA2 register) is generated when a new byte is available in MONR2 register.
ST5451 sets interrupt bit XAB2 (ISTA2 register) if it does not read twice the same byte; in this case, it sends an ABORT to remote peripheral.
The controller generates interrupt bit EOM2 (ISTA2 register) when End Of Message is received.

4 - 6 - ACCESS PROCEDURE TO D AND C/I CHANNELS (GCI and TE mode selected only)

Up to eight HDLC controllers may be connected to D channel and C/I channel. A contention resolution mechanism is used if bit CMS (Contention Mode Selection) is set.
The mechanism allows to give an access without losing data.
An access request may be generated, if CIX1 (Command/Indicate Register 1) contains a different code from DI (1111). During the procedure, M channel (with A and E bits) may be used. On input DIN, the GCI controller checks the CMS4 bit (CMS channel - Third GCI channel) (see Fig. 4).
CMS4 indicates the status of C/I and D channels CMS4= 1 "channels free"; CMS4= 0 channels occupied.
If the channels are free, the HDLC controller starts transmitting its individual address AD2 on CMS1, AD1 on CMS2, AD0 on CMS3. If an erroneous address is detected, the procedure is terminated immediately. If the complete address can be read without error, the D and C/I channels are occupied: the ST5451 transmits CMS4 = 0: The HDLC controller which has the lowest address has priority over the others.
The access request is withdrawn if the HDLC controller transmits code DI = 1111. the CMS4 bit (CMS field) is set.

Figure 3: GCI-SCIT Frame Timing

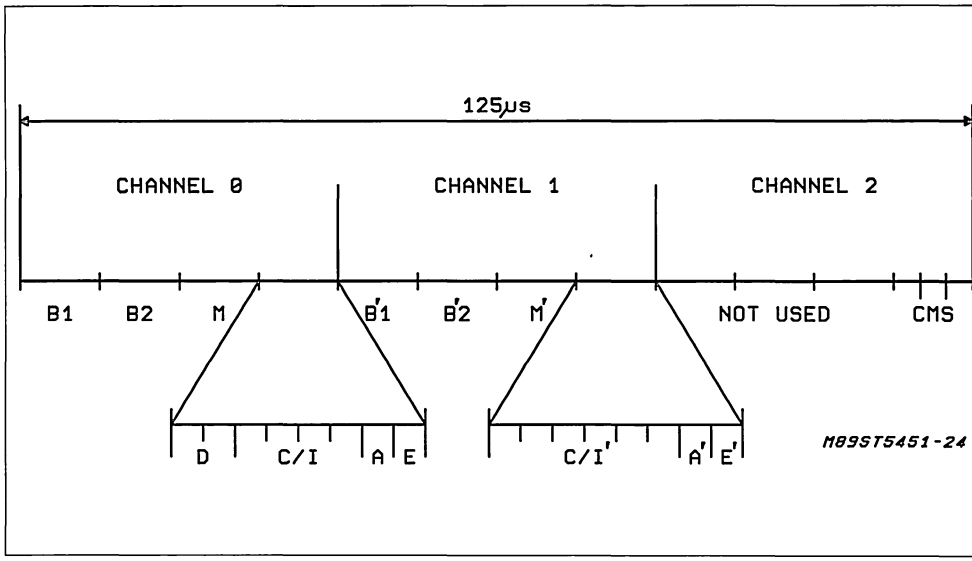
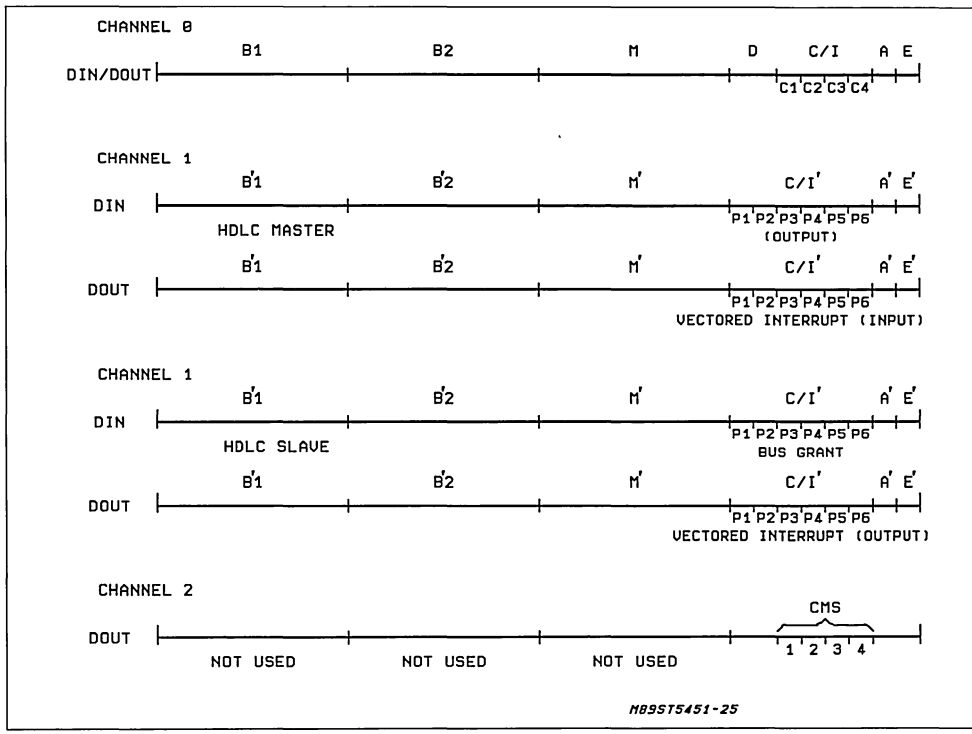


Figure 4: GCI-SCIT Channels Timing



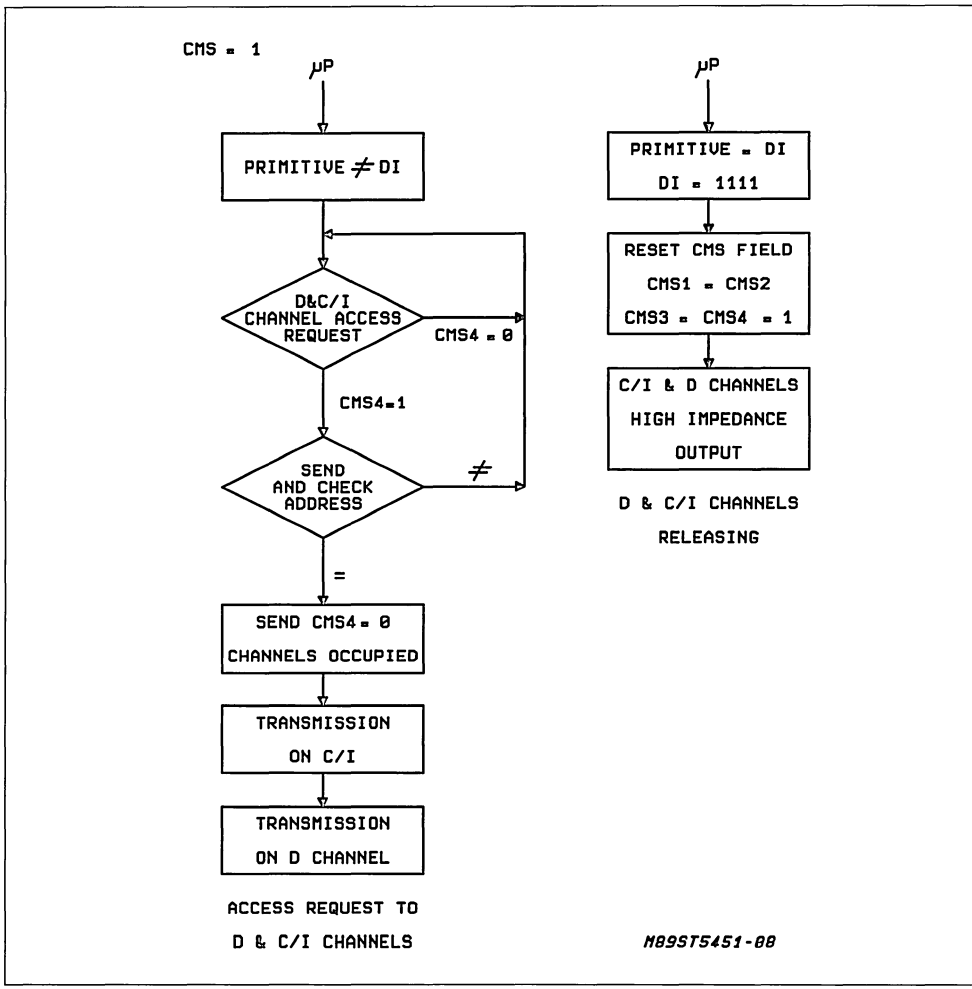
4 - 7 - DMA ACCESS

The HDLC controller has a DMA interface which is activated by DMA bit in MODE register.The DMA interface is available only when multiplexed bus is selected.
ST 5451 asserts DMA REQR or DMA REQX to request an exchange of bytes between the FIFOS and the external memory.
The external DMA controller asserts DMA ACKR or DMA ACKX to access the FIFOS.
These signals are equivalent to E/DS/RD functions.
During DMA access, CS/CE pin must be inactive; AS and E/DS/RD signals can be present.
Outside DMA Access, all registers are accessible by the µP except the FIFOS.

FRAME RECEPTION:
When one block has been stored in RFIFO, DMA REQ R pin goes low and RPF (or RME) interrupts the µP. The DMA controller reads the RFIFO. After the RME interrupt, the frame length will be available in RFBC register. The block is acknowledged by RMC command.

FRAME TRANSMISSION:
When a 32 byte block is free in XFIFO, DMA request goes low and XPR interrupts the µP. The DMA controller can write data in the XFIFO. At the end of the frame, the µP send XME to HDLC controller; CRC and closing flag will be sent by the HDLC controller.

Figure 5: D and C/I channels Access Procedure



4 - 8 - INTERRUPT PROCEDURE

4 - 8 - 1 - HDLC CHANNELS

4 - 8 - 1 - 1 - RECEIVE DIRECTION

RRE and RPF interrupts

RPF bit (register ISTA0) set high to indicate the HDLC controller has received a block of 32 bytes which is not a complete message.

This bit remains high until it is erased by the microprocessor.

As for each bit of ISTA0 register, except the extension bits of ISTA1 and ISTA2 (EXI1, EXI2), the way to erase RPF is to write a "0" at its location and to write a "1" at the location of the others (for example 7FH into ISTA0 to erase RME). The processing order is:

- put Mask0 on ISTA0 (if Mask Off)
- (Read FIFOR) X 32
- Write ISTA0 to erase RPF (BFH)
- Write RMC to "1" for asking for another block of the frame
  (NB: RMC, RMD are automatically erased by the controller)
- Remove Mask0

RME bit (register ISTA0) set high to indicate the HDLC controller has received a short frame or the last block of a large frame. The message is now complete, the bit remains high until it is erased by the microprocessor. The processing order is:

- put Mask0 on ISTA0 (if upper level Mask Off)
- Read RFBC with a mask on the 3 most significant bits, to know the number "N" of transfers to do
- (Read FIFOR) x N for data
- Read FIFOR for status on the frame
- Write ISTA0 to erase RME (7FH)
- Write RMC or RMD to "1" for asking for another frame.

RF0 interrupts

RF0 is a bit of the interrupt register ISTA0 set high to indicate an overflow of the receive FIFO has been detected, either because more than 8 frames cannot be stored or because more than 64 bytes can't be stored. This information is also stored into the status of the concerned frame (RDO).

The processing order of the microprocessor is:

- Looking for RPF and RME bits and pop - up the frames. Then look for the status and throw down the frame concerned. In general case, only one frame is lost.

4 - 8 - 1 - 2 - TRANSMIT DIRECTION

XPR Interrupt

XPR is a bit of the interrupt register ISTA0 coming high to indicate HDLC controller has a free block of 32 bytes. This bit remains high until the microprocessor write a byte into the block and erase this bit into ISTA0; if another block is free, XPR get high again immediately.

The processing order of the microprocessor is in non DMA Mode:

- Put Mask0 on ISTA0 (if upper level Mask Off)
- Write at least one byte into FIFOX
- Write ISTA0 to erase XPR
- Write XHF to "1" for launching the transmit operation of block (a block is not necessarily 32 bytes)
  or write XME to "1" for launching the transmit of a short frame or of the last part of a frame
- Remove masks

In DMA Mode two general cases are possible:

1) The external DMA controller works by "pages" less or equal to 32 bytes. The "process" of the DMAC is a short frame transmission and the processor must give an XME at the end of the DMAC process (refer to figure 2).

2) The DMA controller works by "pages" of more than 32 bytes. It's process is the transfer of the whole frame.
The circuit doesn't need an XHF at the end of an intermediate 32 byte block; since it has reached 32 bytes written into the current fifo, it begins the transfer and toggles on the second fifo as soon as the first is full. (At this moment an XME is possible if the 32nd byte was the end of the frame - case 1) and then, a 33rd write operation into the fifo generates an internal XHF and the frame following blocks are expected.

- In the two cases the flow control is done between DMAC and ST5451 by the way of REQX and ACKX signals

The processing order is:

- Put Mask0
- Give order to DMAC to begin transfer
- Wait for DMAC end of process
- Write ISTA to erase on XPR
- Write XME to signal the end of the frame to the ST5451 (otherwise the ST5451 will put "underrun" interrupt, as soon as its two blocks are free).

XDU Interrupt

XDU is a bit of the interrupt register ISTA0 coming high to indicate HDLC controller has detected an underrun (a frame is being transmitted and no more bytes are available into the FIFO).

The HDLC controller finish the frame by transmitting an "Abort" and no more data can be transmitted even in NHF mode. To be sure XDU is seen by the MIcroprocessor, XDU interrupt bit must be erased in ISTA0 in addition of XRES security procedure

The transmit control is frozen and the only way to reinitialize a transmit session is to write an XRES, after erasing XDU.

4 - 8 - 2 - M CHANNELS INTERRUPTS EOM, RMR, XMR, RAB

Receive Direction

RMR 1/2 is a bit of interrupt register ISTA 1/2 coming high to indicate the M (or M') channel controller has received a valid byte on receiving channel (two identical consecutive bytes).

The microprocessor processing order is;

1. Erasing RMR 1/2 interrupt into ISTA 1/2
2. Read MONR 1/2 register.

This order can't be inverted because, as long as MONR isn't read, the receive state machine is locked in wait state, a new byte can't be acknowledged and so, a new interrupt can't be done.

More, if MONR is read first, the receive state machine is ready for receiving a new byte and create another interrupt. So, if the interrupt bit corresponding to the previous frame isn't erased before a new byte arrives, this byte won't be seen (the microprocessor won't be informed) and the controller will be locked waiting for MONR read.

XAB 1/2 is a bit of the interrupt register coming high to indicate the receive controller has detected an abort (two conscutive bytes not identical) as long as this interrupt isn't erased, the receiver is locked in wait state.

EOM 1/2 is a bit of the interrupt register coming high to indicate the receive controller has detected an end of message. As long as the interrupt isn't erased, the receiver is locked in wait state.

Transmit Direction

XMR 1/2 is a bit of the interrupt register coming high to indicate a byte can be written into MONX. The processing order is:

1. Erasing XMR bit
2. Writing a new byte into MONX.

If this order is inverted, the new byte will be transmitted and a new XMR may be erased before being seen by the microprocessor.

RAB 1/2 is a bit of the interrupt register coming high to indicate the remote receiver has reported an abort detection. The processing order is:

1. Erasing RAB bit
2. Erasing XMR bit
3. Writing a new byte into MONX.

If a write operation of the new byte is done before the RAB erasing, the byte will be lost and the transmitter will stay waiting for it.

4 - 8 - 3 - CI CHANNEL INTERRUPTS

CIC 1/2 is a bit of ISTA 1/2 interrupt register coming high to indicate a valid byte has been detected by the command indicate receive controller, and readable into CIR 1/2 register. The processing order is:

1. Erasing CIC bit
2. Reading CIR register.

If this order is inverted, a next byte may be unseen by the microprocessor. It is recommended to work with "Ping Pong" protocol on CI channels, as non flow control is done.

4 - 9 - SOFTWARE RESET PROCEDURES

4 - 9 - 1 - XRES (Transmit Direction)

XRES is a level sensitive command of CMDR which initialize the transmit process.

- XPR interrupt bit is erased
- XDU interrupt bit is not erased (security procedure)
- All data in FIFOs are lost
- After an XRES, the microprocessor must wait for an XPR before writing new data.

The processing order is:

- Writing a "1" into XRES (CMDR)
- Writing a "0" into XRES (CMDR)
- Read ISTA0 waiting XPR or enable XPR interrupt

4 - 9 - 2 - RHR (Receive Direction)

RHR is a level sensitive command of CMDR, which reinitialize the receive process.

- RME, RPF bits are erased
- RFO bit is erased
- All frames in FIFO R are lost
- If RHR is released (got down) at the time a frame is on line, the HDLC controller waits for a flag.

4 - 9 - 3 - M1RES, M2RES M/CI channels

MRES is a level sensitive command of CMDR which initialize the M/CI channel protocole in both directions.

XMR, RAB, RMR, CIC, XAB, EOM bits are erased by MRES.

After a clock programming (bit CRS), it's necessary to put MRES bit to initialize properly the M protocol.

TYPICAL APPLICATIONS

ST5451 HDLC controller may be used in TE, NT2, NT12 or LT.

Figures 6 to 8 illustrate three typical applications in multifunctional TE.

The D channel containing only signalling is processed by the LAPD controller and routed via a parallel µP interface to the terminal processor. The support of the LAPD protocol which is implemented by the HDLC controller device allows in cost senstive applications the use of a low cost microprocessor. See fig. 6.

Fig. 7 illustrates a configuration in which the D channel containing signalling data (SAPI s) as well as packet switched data (SAPI p) is processed by two controllers and two independent microprocessors.

Fig. 8 illustrates a configuration in which one microprocessor is connected to two controllers via a DMA controller.
D channel with LAPD signalling data and B channel LAPB packet data are processed by the same µP. A DMA controller performs device to memory transfers. It is a typical work station application.

Fig. 9 and 10 illustrate 2 typical applications in NT2 or exchange.

An NT2 or LT in fig.9 with eight D channel controllers connected to the GCI interface handle subscriber 0 to 7. Any GCI compatible transceiver (S or U) may be used to do the subscriber line interface; a GCI compatible exchange circuit may implement the system interface. This is one decentralized application.

Fig. 10 illustrates a centralized application. Using a switching net work, it is possible to connect:

up to thirty two 64 Kbit/s channels on a 2 Mb/s PCM highway to 32 B channel controllers

up to sixty four 64 Kbit/s channels on a 4 Mb/s PCM highway to 64 B channel controllers

up to two hundred fifty six D channels on a 4 Mb/s highway to 256 D channel controllers.

Figure 6: Low cost GCI terminal application

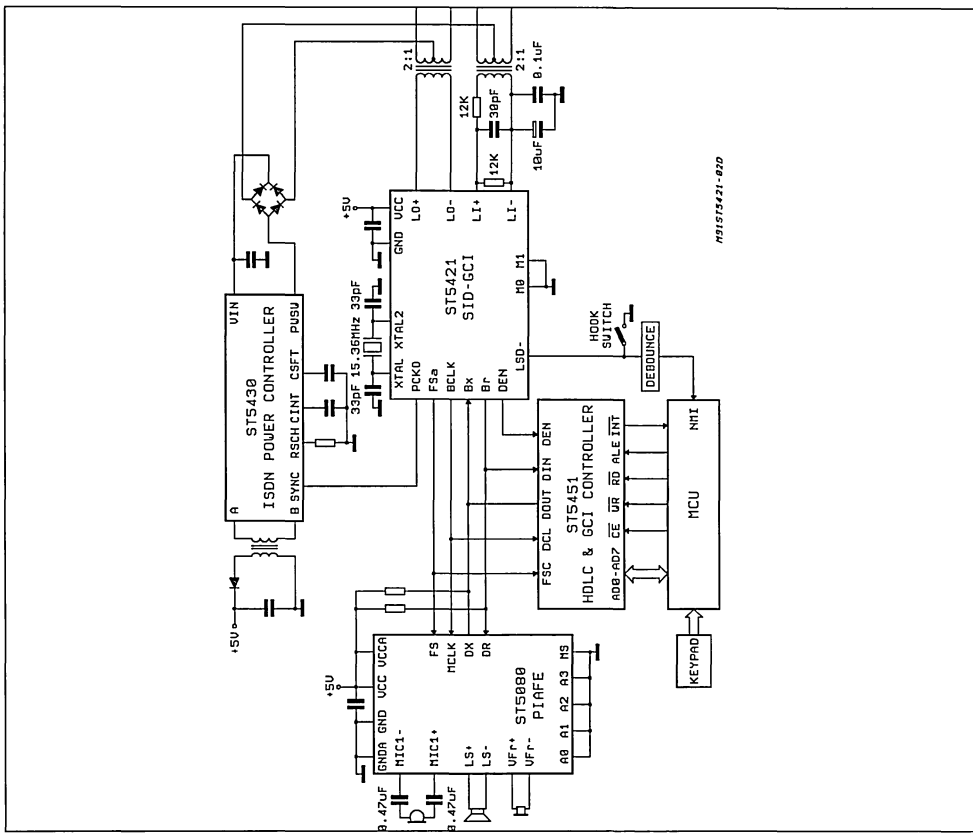


Figure 7: LAPB and LAPD protocol on the same D channel handlended with 2 different µPs

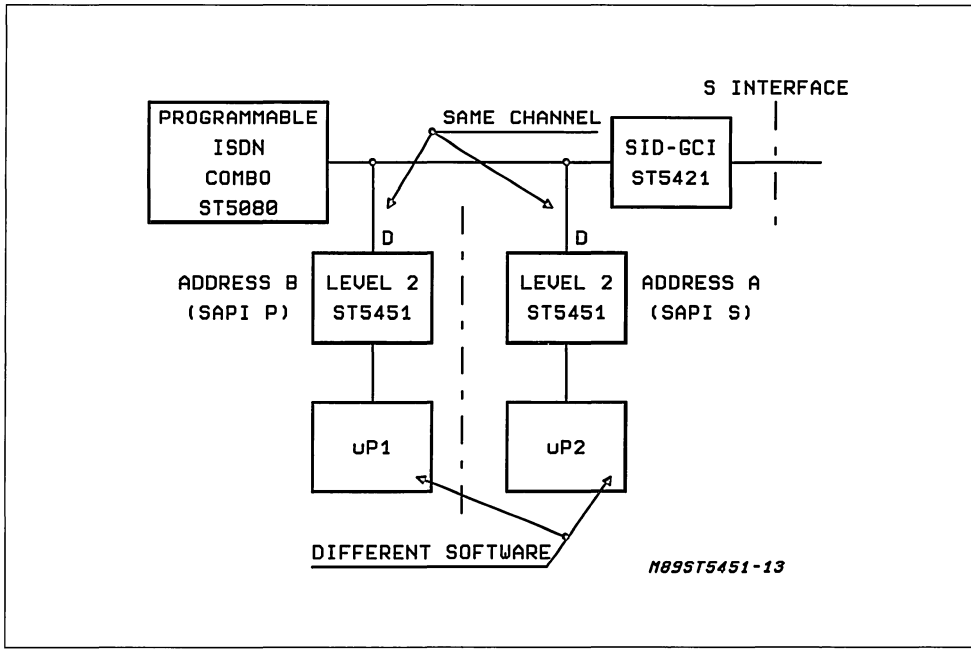


Figure 8: LAPB and LAPD protocol handling an B and D channel

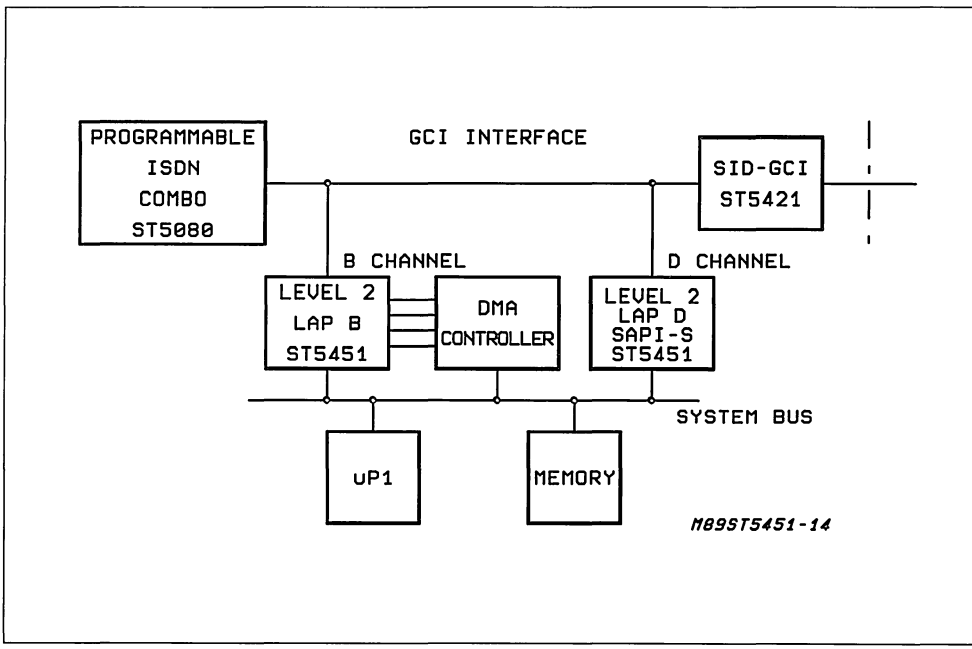


Figure 9: Decentralized D channel handling in NT2 or LT

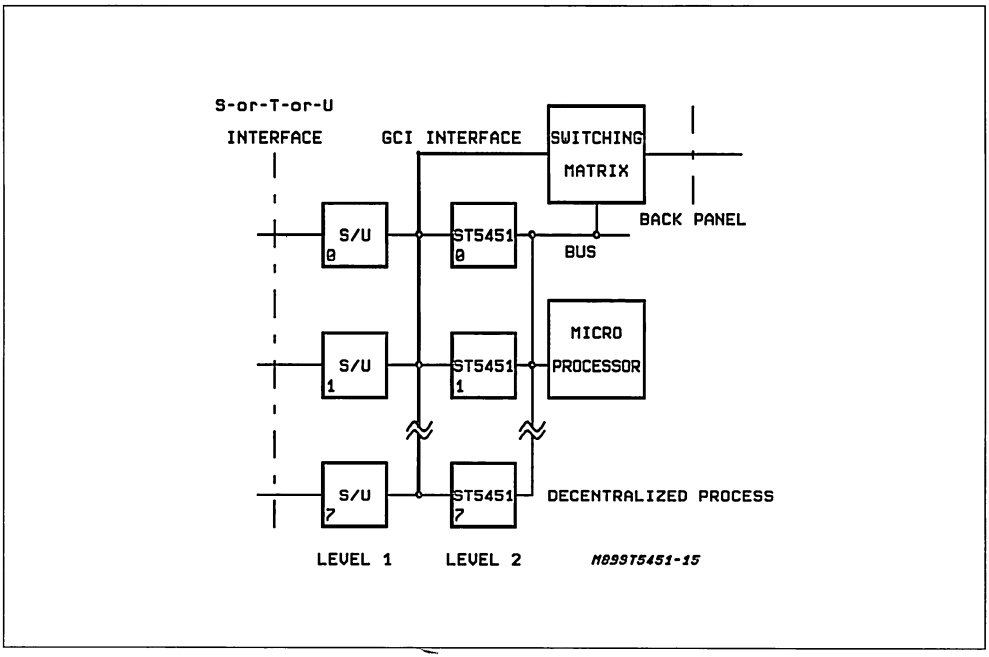


Figure 10: Centralized D channel handling in NT2 or LT

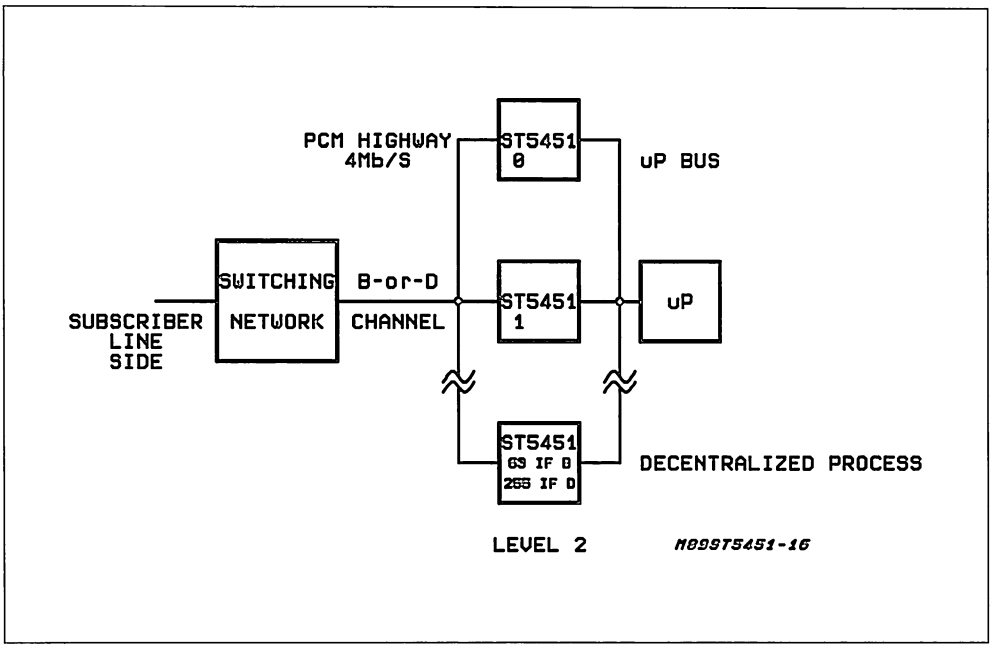


Figure 11: HDCL Frame Transmission Procedure

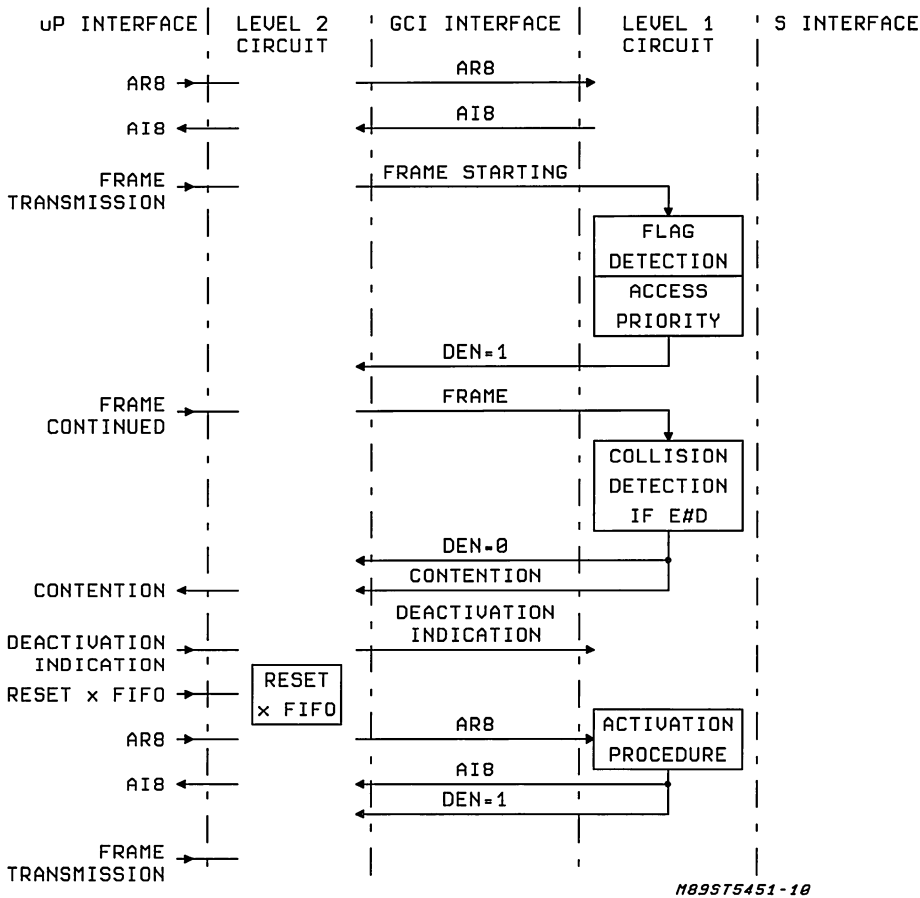


Figure 12: HDCL Frame Transmission Procedure in D Channel

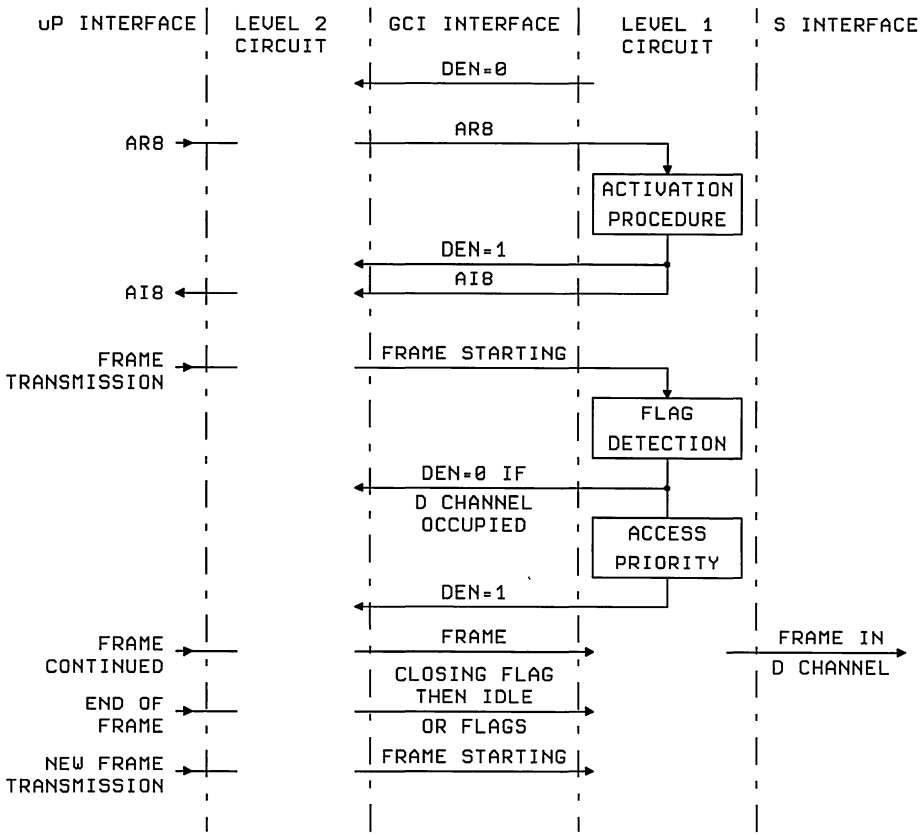
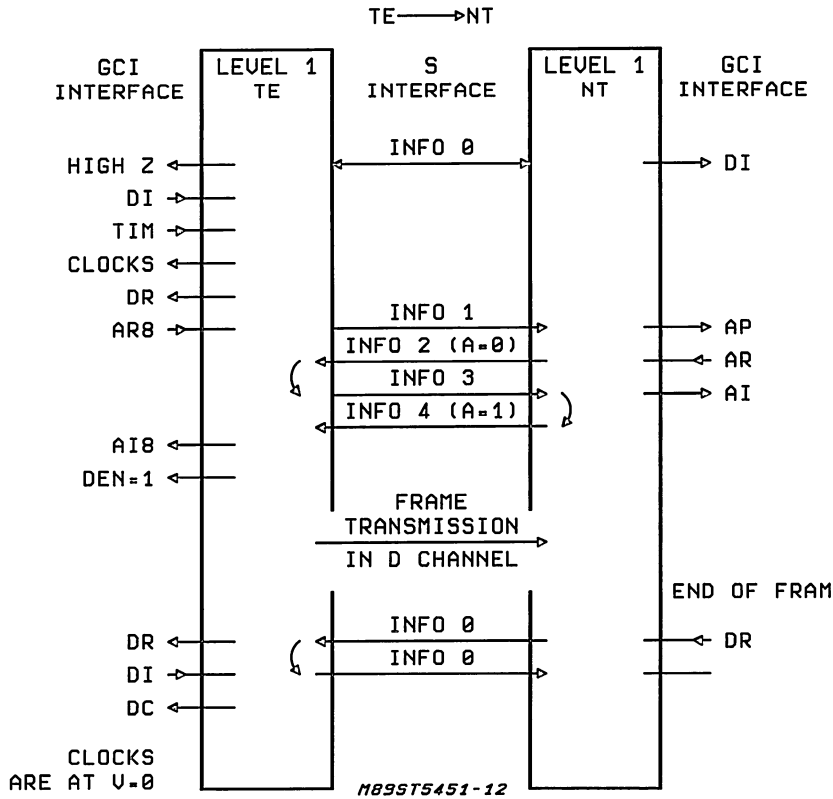


Figure 13: S Activation and Deactivation procedure



ELECTRICAL CHARACTERISTICS (T from 0 to 70°C, V_{DD} = 5 ± 0.25V).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_S	Supply Current	CLK Freq. = 4MHz	–	4	–	mA
		CLK Freq. = 2MHz	–	2	4	mA
		NO CLK Freq.	–	20	300	µA

STATIC CHARACTERISTICS - GCI INTERFACE (T from 0 to 70°C, V_{DD} = 5 ± 0.25V).

Symbol	Parameter	Condition	Min.	Max.	Unit
VIH	High Level Input Voltage	Maximum leakage current : ± 10 µA	2.4	VDD+0,4	V
VIL	Low Level Input Voltage	Maximum leakage current : ± 10 µA	VSS-0,4	0,8	V
VOH	High Level Output Voltage	IOH = -0,4 µA	2,4		V
VOL	Low Level Output Voltage	IOL = 2mA		0,45	V
VOL	Low Level Output Voltage D_{OUT} . D_{in} . INT	IOL = 7mA		0,45	V
C	Input/Output Capacity			10	pF
C_{OUT}	Load Capacity DIN/DOUT			150	pF
	Load Capacity $\overline{INT}$			150	pF
	Load Capacity AD0/7			100	pF

DYNAMIC ELECTRICAL CHARACTERISTICS - GCI Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
FSync	8 KHz		8		KHz
F_{CLK}	64 x n x FSync $1 \leq n \leq 8$	512		4096	KHz
t_{WCH}	Period of CLK High	80			ns
t_{WCL}	Period of CLK Low	80			ns
t_{RC}	Rise Time of CLK			10	ns
t_{FC}	Full Time of CLK			10	ns
t_{HCF}	Hold Time: CLK - FS	0			ns
t_{SFC}	Set-up Time: FS - CLK	30			ns
t_{DCD}	Delay Time: CLK High to data valid. out: 150 pF			80	ns
t_{DCZ}	Delay Time: to Data Disabled	0		80	ns
t_{DFD}	Delay Time: FSync. High to data valid. count: 150 pF. Applies only if Sync rises later than CLK raising edge.			80	ns
t_{SDC}	Set-up Time: Data valid to CLK receive edge.	30			ns
t_{HDC}	Hold Time: CLK low to data invalid.	30			ns

DYNAMIC ELECTRICAL CHARACTERISTICS - Double Clock Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
FSync	8 KHz		8		KHz
F_{CLK}	16 x n x FSync $1 \leq n \leq 64$	128		8192	KHz
t_{WCH}	Period of CLK High	50			ns
t_{WCL}	Period of CLK Low	50			ns
t_{RC}	Rise Time of CLK			10	ns
t_{FC}	Full Time of CLK			10	ns
t_{HCF}	Hold Time: CLK - FS	0			ns
t_{SFC}	Set-up Time: FS - CLK	30			ns
t_{DCD}	Delay Time: CLK High to data valid. out: 150 pF			80	ns
t_{DCZ}	Delay Time: to Data Disabled	0		80	ns
t_{DFD}	Delay Time: FSync High to data valid. count: 150 pF. Applies only if Sync rises later than CLK raising edge.			80	ns
t_{SDC}	Set-up Time: Data valid to CLK receive edge.	30			ns
t_{HDC}	Hold Time: CLK low to data invalid.	30			ns

ELECTRICAL CHARACTERISTICS - Single Clock Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
FSync	8 KHz		8		KHz
F_{CLK}	8 x n x FSync $1 \leq n \leq 64$	64		4096	KHz
t_{WCH}	Period of CLK High	80			ns
t_{WCL}	Period of CLK Low	80			ns
t_{RC}	Rise Time of CLK			10	ns
t_{FC}	Full Time of CLK			10	ns
t_{HCF}	Hold Time: CLK - FS	0			ns
t_{SFC}	Set-up Time: FS - CLK	100			ns
t_{DCD}	Delay Time: CLK High to data valid. out: 150 pF			80	ns
t_{DCZ}	Delay Time: to Data Disabled	0		80	ns
t_{DFD}	Delay Time: FSync. High to data valid. count: 150 pF. Applies only if Sync rises later than CLK raising edge.			80	ns
t_{SDC}	Set-up Time: Data valid to CLK receive edge.	30			ns
t_{HDC}	Hold Time: CLK low to data invalid.	30			ns

Figure 14: GCI Timing

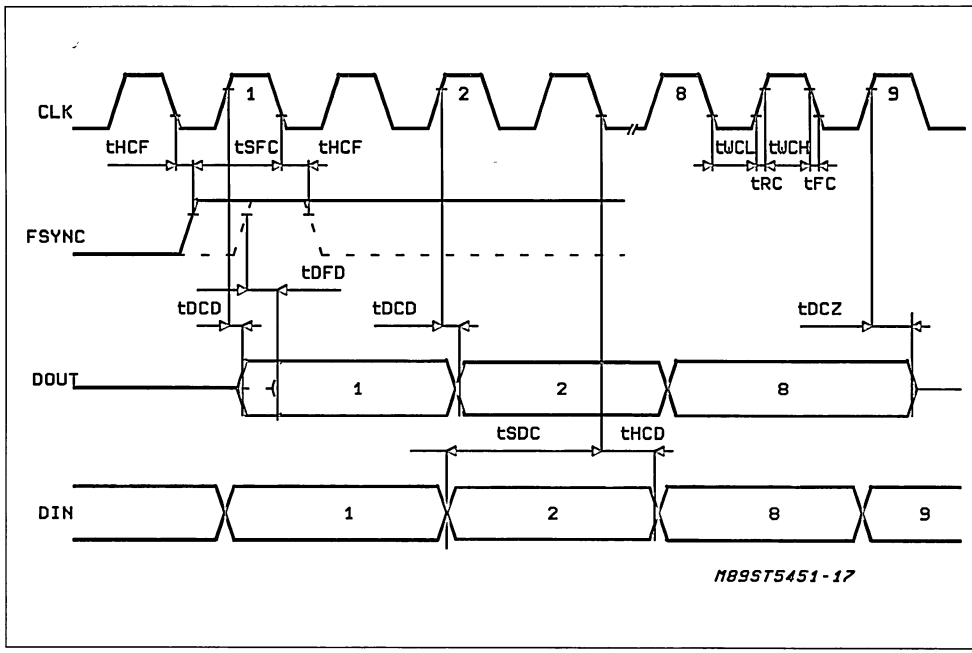


Figure 15: Single Clock Diagram

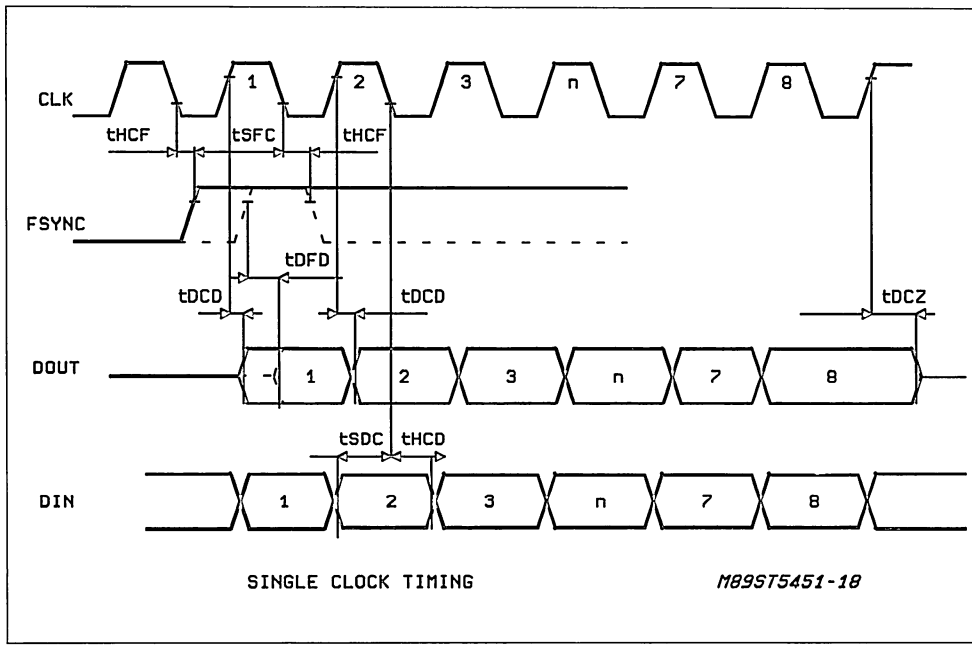
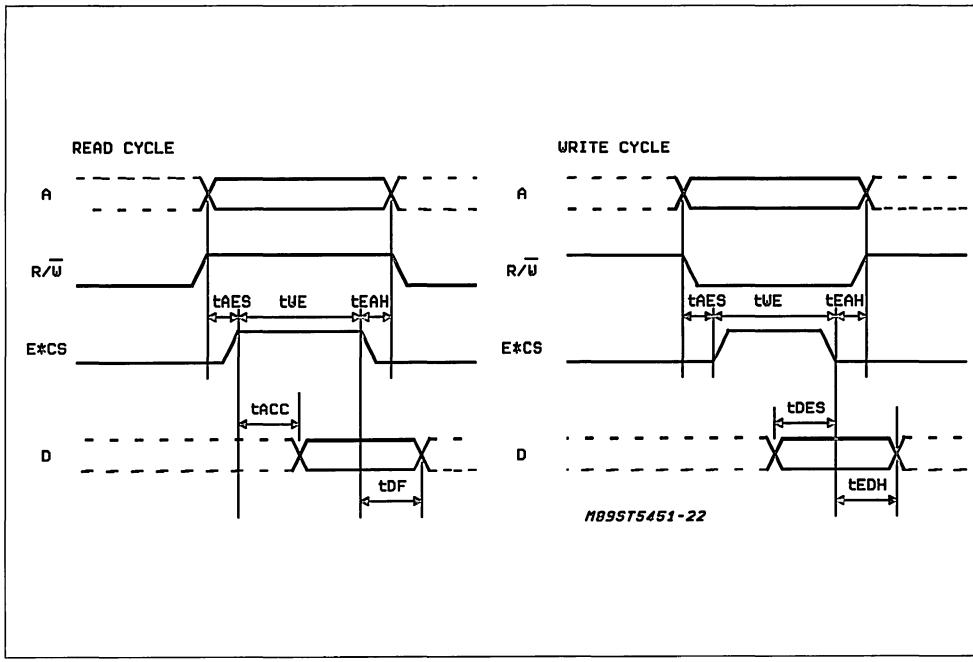


Figure 16: Non-multiplexed µP bus timing



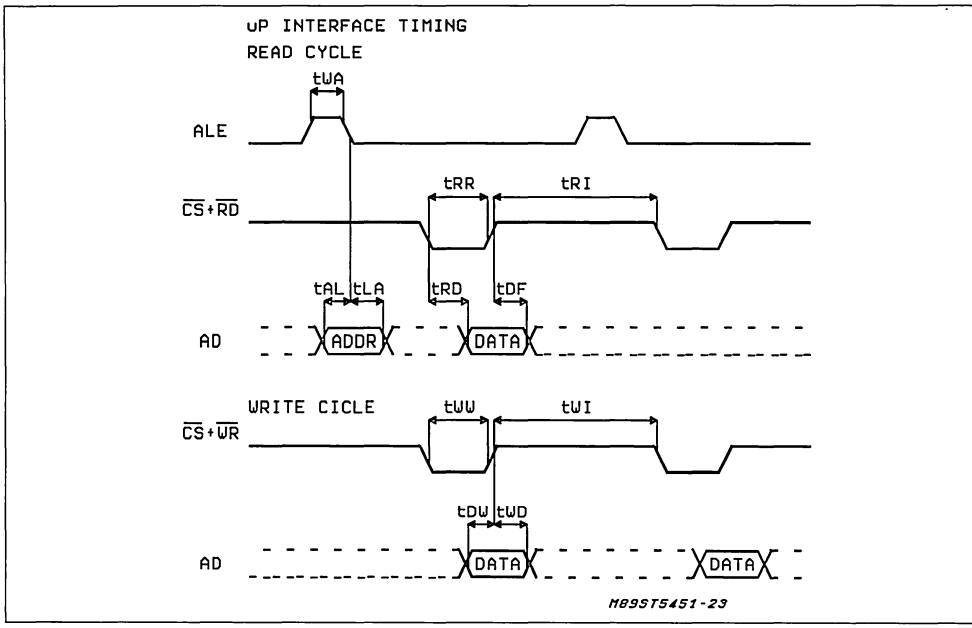
READ CYCLE (Non-multiplexed mode)

Symbol	Parameter	Min.	Max.	Unit
t_{EAH}	Address Hold After E	10		ns
t_{EAH}	R/$\overline{W}$ Hold After E	10		ns
t_{AES}	Address to E Setup	20		ns
t_{AES}	R/$\overline{W}$ to E. Setup	20		ns
t_{ACC}	Data Delay from E		110	ns
t_{DF}	Output Float Delay		25	ns
t_{WE}	Minimum Width of E	110		ns

WRITE CYCLE (Non-multiplexed mode)

Symbol	Parameter	Min.	Max.	Unit
t_{EAH}	Address Hold After	10		ns
t_{EAH}	R/$\overline{W}$ Hold After E	10		ns
t_{AES}	Address to E Setup	20		ns
t_{AES}	R/$\overline{W}$ to E.CS Setup	20		ns
t_{DES}	Data to End of E Setup	35		ns
t_{EDH}	End of E.CS to Data hold	10		ns
t_{WE}	Minimum Width of E	60		ns
t_{RW}	Minimum Width of RESET	100		ns

Figure 17: Multiplexed Intel-like µP bus timing



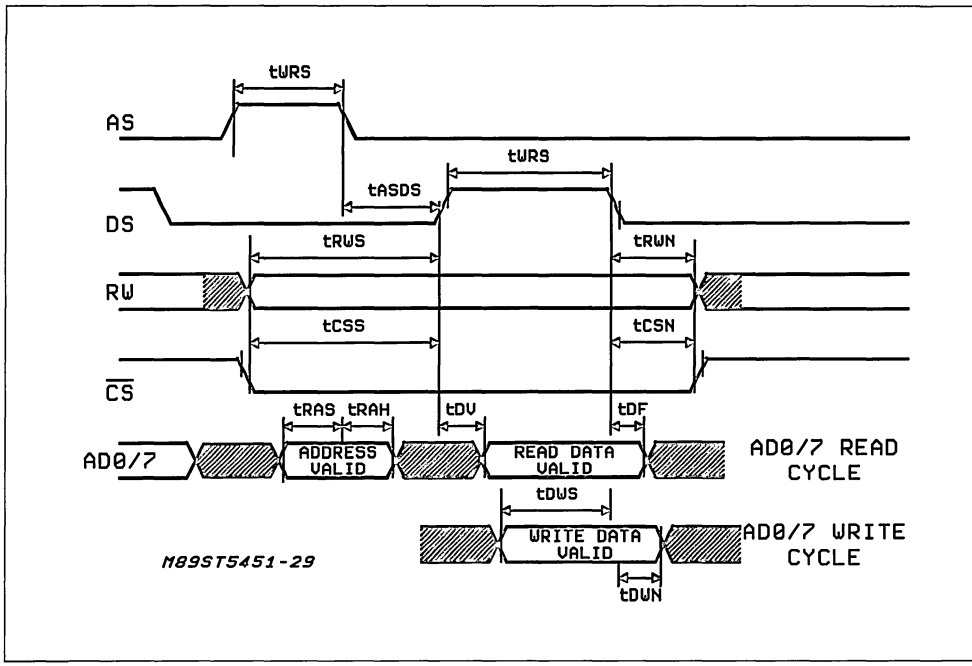
READ CYCLE (Multiplexed Intel Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{LA}	Address Hold After ALE	10		ns
t_{AL}	Address to ALE Setup	20		ns
t_{RD}	Data Delay from $\overline{RD}$		110	ns
t_{RR}	$\overline{RD}$ Pulse Width	110		ns
t_{DF}	Output Float Delay		25	ns
t_{RI}	$\overline{RD}$ Control Interval	70		ns
t_{WA}	ALE Pulse Width	30		ns
t_{CSS}	$\overline{CE}$ to $\overline{RD}$ or $\overline{WR}$ set-up t_{CSS}	20		ns
t_{CSH}	$\overline{CE}$ hold after $\overline{RD}$ to $\overline{WR}$ t_{CSH}	10		ns

WRITE CYCLE (Multiplexed Intel Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{WW}	$\overline{WR}$ Pulse Width	60		ns
t_{DW}	Data Setup to $\overline{WR}$	35		ns
t_{WD}	Data Hold after $\overline{WR}$	10		ns
t_{WI}	$\overline{WR}$ Control Interval	70		ns

Figure 18: Multiplexed Motorola-like µP bus timing



Symbol	Parameter	Min.	Max.	Unit
t_{WAS}	AS Pulse Width	30		ns
t_{WDS}	DS Pulse Width	110		ns
t_{ASDS}	AS low to DS high	10		ns
t_{RWS}	RW to DS setup	20		ns
t_{RWH}	RW hold after DS	10		ns
t_{CSS}	CS to DS setup	20		ns
t_{CSH}	CS hold after DS	10		ns
t_{AAS}	Address to AS setup	20		ns
t_{AAH}	Address hold after AS	10		ns

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit
t_{DV}	Data Valid after DS		110	ns
t_{DF}	Output Flat Delay		25	ns

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit
t_{DWS}	Data to DS setup	35		ns
t_{DWH}	Data Hold after DS	10		ns

DMA BUS TIMING (Reception Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{ACC}	Data Delay from ACKR		110	ns
t_{DF}	Output Float Delay		25	ns
$t_{W\overline{AR}}$	Minimum width $\overline{ACKR}$	110		ns
t_{WAR}	Minimum width ACKR	70		ns
t_{DRAR}	REQR Delay from ACKR		80	ns

Figure 19: DMA frame reception timing

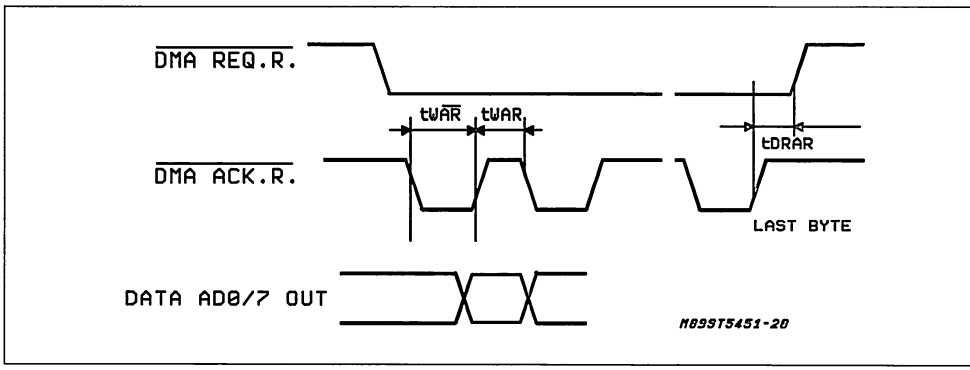
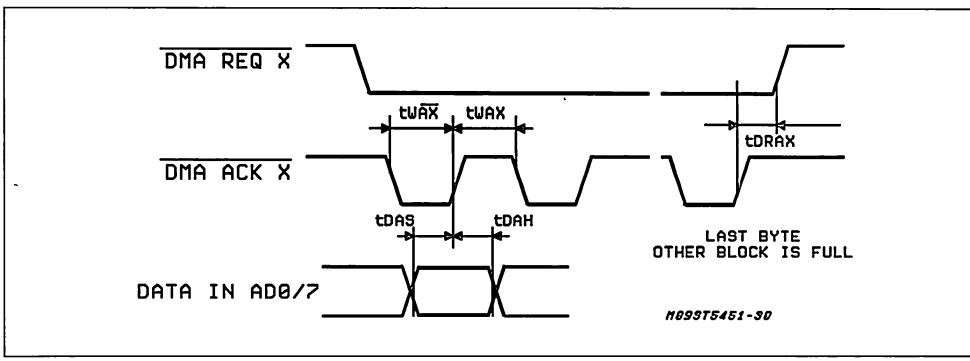


Figure 20: DMA frame transmission timing



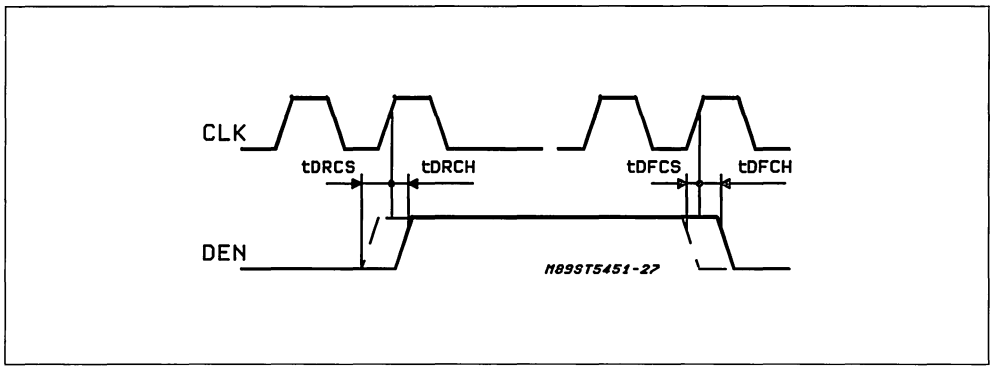
DMA BUS TIMING (Transmission Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{DAS}	Data Setup to ACKX	35		ns
t_{DAH}	Data Hold from ACKX	10		ns
$t_{W\overline{AX}}$	Minimum width $\overline{ACKX}$	60		ns
t_{WAX}	Minimum width ACKX	70		ns
t_{DRAX}	REQX Delay from ACKX	80		ns

DEN TIMING

Symbol	Parameter	Min.	Max.	Unit
t_{DRCS}	DEN setup to CLK		30	ns
t_{DRCH}	DEN Hold from CLK		30	ns
t_{DFCS}	DEN Setup to CLK		30	ns
t_{DRCH}	DEN Hold from CLK		30	ns

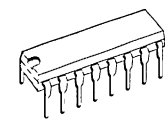
Figure 21: DEN Timing



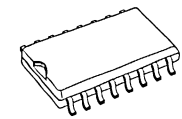
UNIVERSAL PROGRAMMABLE DUAL PLL

PRODUCT PREVIEW

- TWO INDEPENDENT PLL WITH 16 BITS PROGRAMMABLE DIVIDERS FROM 13 TO 65535 FOR TRANSMIT AND RECEIVE LOOPS
- ON CHIP REFERENCE OSCILLATOR COMMON FOR THE TWO LOOPS UP TO 16MHz WITH EXTERNAL CRYSTAL
- TWO INDEPENDENT PROGRAMMABLE REFERENCE COUNTERS:
  - 12 bits programmable counter from 13 to 4095 followed by selectable dividers by 1, 4 and 25
  - 14 bits auxiliary programmable counter from 13 to 16383
- A MCU CLOCK DERIVED FROM REFERENCE OSCILLATOR WITH A SELECTABLE DIVISION FACTOR OF 3 OR 4
- TWO INDEPENDENT PFD (PHASE FREQUENCY DISCRIMINATOR) WITH 3 STATE OUTPUTS
- LOCK DETECT SIGNAL OUTPUT FOR THE TRANSMIT LOOP
- 3 & 4 WIRES SELECTABLE MCU SERIAL INTERFACE, FOR SIMULTANEOUS PROGRAMMING OF 2 COUNTERS
- STAND-BY MODE

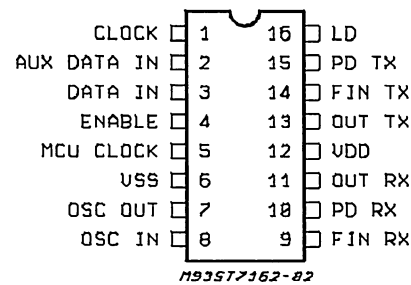


DIP16
ORDERING NUMBER: ST7162N



SO16
ORDERING NUMBER: ST7162D

PIN CONNECTION (Top view)



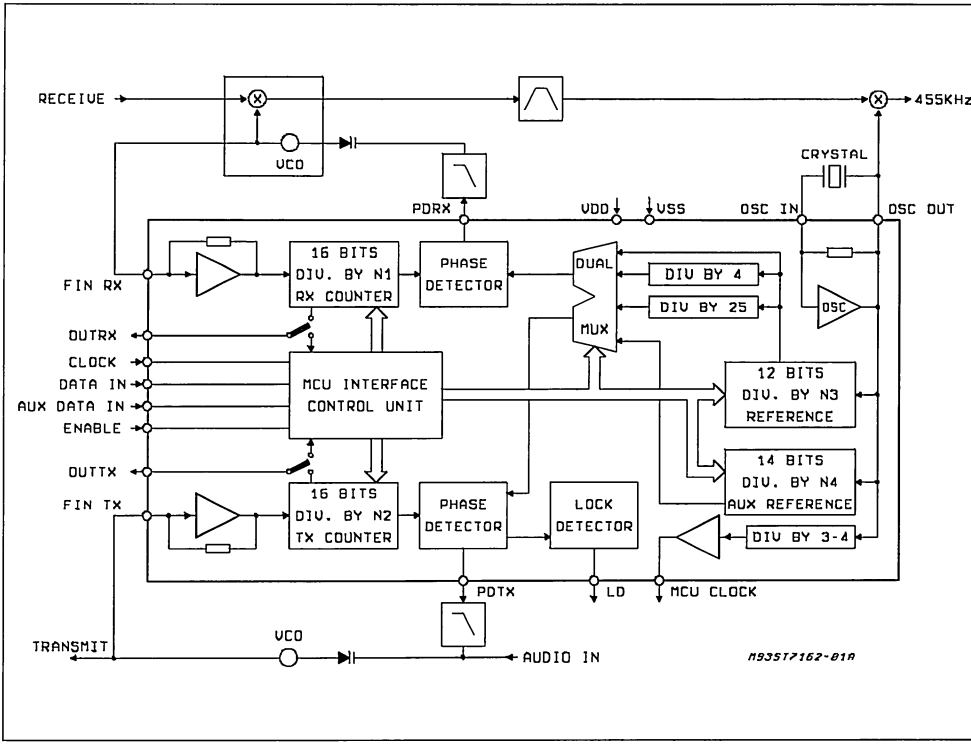
MAIN CHARACTERISTICS

- High input sensitivity: 200mVpkpk @ 60MHz
- Low consumption: 3.5mA @ 3V for the two loops
- Power supply voltage: 3V to 5V
- Operating temperature range: –25°C to +70°C

DESCRIPTION

The ST7162 is a dual frequency synthesizer in High Speed CMOS technology for radio applications with a frequency up to 60MHz. The low power consumption and high flexibility make it well suitable for cordless CT0 applications in various countries.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD} - V_{SS}	Supply Voltage	– 0.5 to +6	V
V_{IN}	Input Voltage	V_{SS} –0.5 to V_{DD} +0.5	V
V_{OUT}	Output Voltage	V_{SS} –0.5 to V_{DD} +0.5	V
I_{IN}, I_{OUT}	DC Current per pin	– 10 to 10	mA
I_{DD}, I_{SS}	DC Current for pin V_{DD} or V_{SS}	– 30 to 30	mA
T_{stg}	Storage Temperature	– 55 to +125	°C

PIN FUNCTIONS

N.	Name	Function
1	CLOCK	MCU Interface
2	AUX DATA IN	MCU Interface
3	DATA IN	MCU Interface
4	ENABLE	MCU Interface
5	MCU CLOCK	Scaled down reference frequency for clocking the MCU
6	V_{SS}	Negative Power Supply
7	OSC OUT	Oscillator Output
8	OSC IN	Oscillator Input
9	FIN R_X	Input to the 16 bits Receive Counter
10	PD R_X	Phase detector output of the Receive loop
11	Out R_X	Power saving output bit for the RX loop and FIN R_X divided by N1 for testing the R_X input sensitivity.
12	V_{DD}	Positive power supply
13	OUT T_X	Power saving output bit for the T_X loop and FIN T_X divided by N2 for testing the T_X input sensitivity.
14	FIN T_X	Input to the 16 bits Transmit counter.
15	PD T_X	Phase detector output of the transmit loop
16	LD	Lock detect output of the transmit loop.

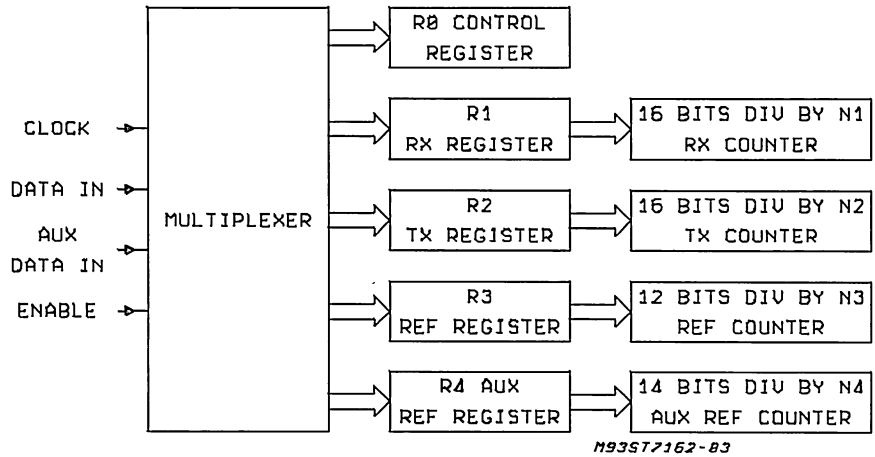
ELECTRICAL CHARACTERISTICS (Tamb = 25°C, voltage reference = V_{SS})

Symbol	Parameter	Test Condition	V_{DD}	Min.	Typ.	Max.	Unit
SUPPLY							
V_{DD}	Supply Voltage			3		5.5	V
I_{DD} up	Supply Current	200mVpkpk sinus at input; FIN RX = 36MHz, FIN TX =49MHz; loop in lock condition; f_{osc} = 10.24MHz; no output load	3V 5V			3.7 7.7	mA mA
I_{DDRX}	Supply Current	200mVpkpk sinus at input; FIN RX = 36MHz; TX Loop in Power down; f_{osc} = 10.24MHz; no output load	3V 5V			2.5 5.3	mA mA
I_{DD} down	Supply Current	Stand-by mode for all counters; OSCIN pin Grounded; MCU interface disabled	3V 5V			150 300	µA µA
T_X and R_X INPUTS							
C_{IN}	Input Capacitance					8	pF
I_{IN} up	Input Current	$0 < V_{IN} < V_{DD}$	3V 5V	– 60 – 100		60 100	µA µA
Fmax	Input Frequency	Input = sinus 200mVpkpk AC coupled	3-5V			60	MHz
OSCILLATOR							
C_{IN}	Input Capacitance					8	pF
C_{OUT}	Output Capacitance					8	pF
I_{IN} up	Input Current	$0 < V_{IN} < V_{DD}$ DC measured	3V 5V	– 60 – 100		60 100	µA µA
Fmax	Input Frequency		3-5V			16	MHz

ELECTRICAL CHARACTERISTICS (Tamb = 25°C, voltage reference = V_{SS})

Symbol	Parameter	Test Condition	V_{DD}	Min.	Typ.	Max.	Unit
PHASE FREQUENCY DISCRIMINATOR							
C_{OUT}	Output Capacitance					8	pF
$I_{OUT\ HI}$	Output Current	Source V_{OUT} = 2.7V V_{OUT} = 4.5V	 3V 5V	 – 200 – 500			 µA µA
$I_{OUT\ LO}$	Output Current	Sink V_{OUT} = 0.3V V_{OUT} = 0.5V	 3V 5V	 200 500			 µA µA
I_{LEAK}	Leakage Current	Three state output $VPDT_X$, $VPDR_X$ = 0 or 5V	5V	– 50		50	nA
MCU INTERFACE INPUTS							
C_{IN}	Input Capacitance					8	pF
I_{IN}	Input Current	DC measured $V_{IN} = V_{DD}$ or V_{SS}	3-5V	– 10		10	µA
V_{IH}	Input Voltage	High level "1"	3V 5V	2.3 3.8			V V
V_{IL}	Input Voltage	Low level "0"	3V 5V			0.7 1.2	V V
Fmax	Input Frequency	Maximum frequency at clock input	3-5V			500	KHz
T_W	Pulse width	Clock and Enable inputs	3V 5V	80 60			ns ns
T_{SU}	Set-up Time	Data to clock Enable to clock	3-5V 3-5V	100 200			ns ns
T_{HOLD}	Hold Time	Clock to data	3V 5V	80 40			ns ns
T_{REC}	Recovery Time	Enable to Clock	3V 5V	80 40			ns ns
DIGITAL OUTPUTS: $OUTT_X$, $OUTR_X$, MCU_{CLOCK}, LD							
C_{LOAD}	Output Load Capacitance					25	pF
$V_{OUT\ IH}$	Output Voltage	I_{OUT} = 0, High level "1"	3V 5V	2.95 4.95			V V
$V_{OUT\ LO}$	Output Voltage	I_{OUT} = 0, Low level "0"	3V 5V			0.05 0.05	V V
I_{OUTHI}	Output Current	Source V_{OUT} = 2.7V V_{OUT} = 4.5V	 3V 5V	 – 200 – 500			 µA µA
I_{OUTLO}	Output Current	Sink V_{OUT} = 0.3V V_{OUT} = 0.5V	 3V 5V	 200 500			 µA µA
THI	Output rise Time	C_{LOAD} = 25pF	3V 5V			200 100	ns ns
TLO	Output Fall Time	C_{LOAD} = 25pF	3V 5V			200 100	ns ns

Figure 1: Control Unit Block Diagram



Sumary of Internal Registers

Register	Adress			Number of Data Bits	Function
	A2	A1	A0		
R0	0	0	0	13	CIRCUIT CONTROL
R1	0	0	1	16	BINARY VALUE OF N1 = RX RATIO
R2	0	1	0	16	BINARY VALUE OF N2 = TX RATIO
R3	0	1	1	12	BINARY VALUE OF N3 = REF RATIO
R4	1	0	0	14	BINARY VALUE OF N4 = AUX REF RATIO

Description of Control Register

Bit	Name	Function
D12	TEST 1	Test Mode: See Table 1.
D11	TEST 2	
D10	TEST 3	
D9	AUXILIARY DATA SELECT	Set to 0 to select 3 wires serial data bus mode at the next pattern Set to 1 to select 4 wires serial data bus mode at the next pattern
D8	REFOUT/3	Set to 0, MCUCLOCK frequency = OSC.OUT frequency / 4 Set to 1, MCUCLOCK frequency = OSC.OUT frequency / 3
D7	TXCE	TX Counter Enable bit: if set to 0, TX amplifier, counter and PFD will be in power down mode and OUTTX pin will be set to 1.
D6	RXCE	RX Counter Enable bit: if set to 0, RX amplifier, counter and PFD will be in power down mode and OUTRX pin will be set to 1.
D5	RCE	Reference Counter Enable bit: if set to 0, ref counter will be in power down mode.
D4	ARCE	Auxiliary Reference Counter Enable bit: if set to 0, AUX Ref counter will be in power down mode
D3	MUX SELECT 1	Used to connect internally PFD inputs REFTX and REFRX to the chosen Ref frequency output: see Table 2.
D2	MUX SELECT 2	
D1	MUX SELECT 3	
D0	MUX SELECT 4	

Table 1.

TEST1	TEST2	TEST3	Status of output pin OUTTX	Status of output pin OUTRX	Status of TX and RX PFD
0	0	0	CONTROL BIT $\overline{TXCE}$	CONTROL BIT $\overline{RXCE}$	NORMAL OPERATION
0	0	1	INTERNAL POINT REFTX	INTERNAL POINT REFRX	TEST MODE NORMAL IUP
0	1	0	INTERNAL POINT FINTX/N2	INTERNAL POINT FINRX/N1	TEST MODE NORMAL IDOWN
0	1	1	INTERNAL POINT FINTX/N2	INTERNAL POINT FINRX/N1	TEST MODE I LEAKAGE
1	0	0	CONTROL BIT $\overline{TXCE}$	CONTROL BIT $\overline{RXCE}$	OPERATION WITH INCREASED IUP AND IDOWN
1	0	1	INTERNAL POINT REFTX	INTERNAL POINT REFRX	TEST MODE INCREASED IUP
1	1	0	INTERNAL POINT FINTX/N2	INTERNAL POINT FINRX/N1	TEST MODE INCREASED IDOWN
1	1	1	INTERNAL POINT FINTX/N2	INTERNAL POINT FINRX/N1	TEST MODE I LEAKAGE

Figure 2: Reference Frequency Diagram.

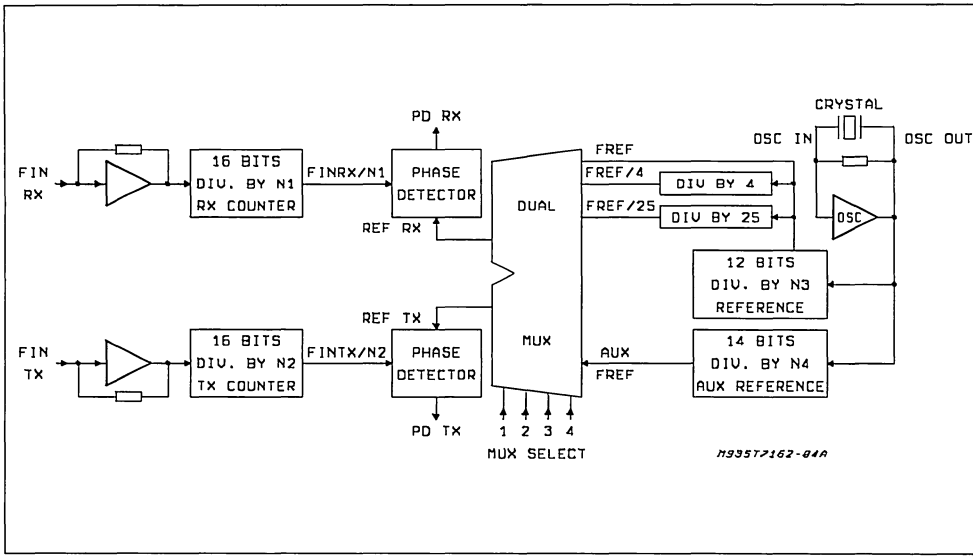


Table 2.

MUX SELECT 1	MUX SELECT 2	MUX SELECT 3	MUX SELECT 4	INPUT OF TX PFD REFTX CONNECTED TO INTERNAL POINT (see Note 1)	INPUT OF RX PFD REFRX CONNECTED TO INTERNAL POINT (see Note 2)
0	0	0	0	FREF	FREF
0	0	0	1	FREF	FREF/4
0	0	1	0	FREF	FREF/25
0	0	1	1	FREF	AUXFREF
0	1	0	0	FREF/4	FREF
0	1	0	1	FREF/4	FREF/4
0	1	1	0	FREF/4	FREF/25
0	1	1	1	FREF/4	AUXFREF
1	0	0	0	FREF/25	FREF
1	0	0	1	FREF/25	FREF/4
1	0	1	0	FREF/25	FREF/25
1	0	1	1	FREF/25	AUXFREF
1	1	0	0	AUXFREF	FREF
1	1	0	1	AUXFREF	FREF/4
1	1	1	0	AUXFREF	FREF/25
1	1	1	1	AUXFREF	AUXFREF

Note (1):
If the 12 bits REF. counter is disabled (R_{CE} control bit = 0) then the inputs of RX and TX PFD (REF TX and REF RX) are connected to internal point AUX REF.

Note (2):
If the 14 bits auxiliary reference counter is disabled (ARCE control bit = 0) then the internal point AUXFREF is replaced by FREF/ 25

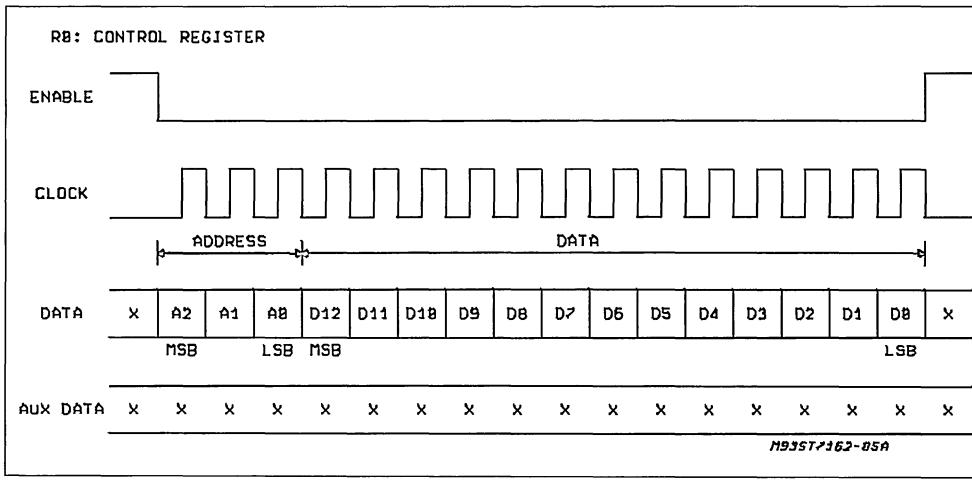
PROGRAMMING THE REGISTER (Figs 3 to 8)

When a Low level is present on the ENABLE input, information on the DATA and AUX DATA inputs are used to program the internal registers. Data are shifted at the rising edge of the clock input. First the 3 address bits of a register are sent, followed by 12 to 16 data bits, depending on the lenght of the register. The address is latched at the 3rd clock impulse following a falling edge at ENABLE input. This configuration allows to send various lenght patterns. Moreover, fixed patterns of 24 or 32 bits can be sent if dummy bits are inserted between the address bits and the first data bit. After the last data bit, a rising edge of the ENABLE input latches the information. When the V_{DD} supply is switched on, an internal circuit provides a reset of the control register bits. When the serial bus is not used, a Low level at clock input and a HIGH level at ENABLE inputs are applied.

PROGRAMMING THE 3/4 WIRES MODE

When the Auxiliary Data select bit of the control register is set to 1, the serial bus is switched in 4 wires mode at the next pattern. Then one or other of the 5 registers may be serially loaded by one or other of the DATA or AUX DATA inputs. When loading simultaneously 2 registers with different lenght, dummy bits are inserted between the address bits and the data bits of the shorter register (see fig. 8).

Figure 3: 3 Wires Serial Data Transmission Timing



X = DON'T CARE

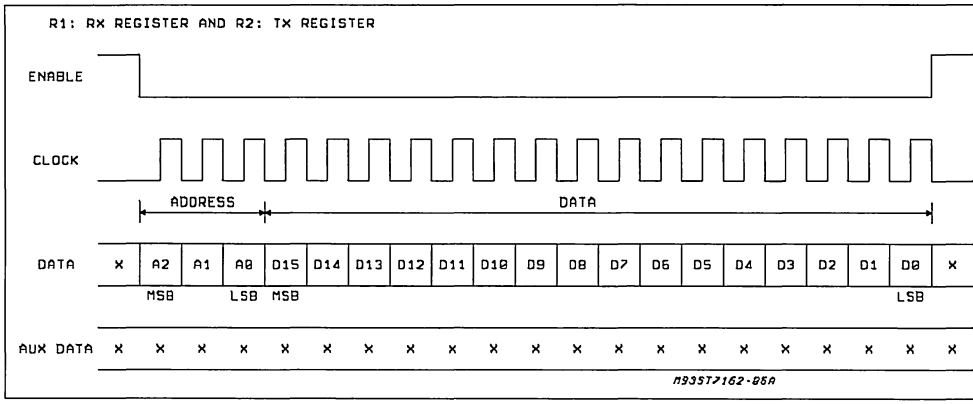
ADDRESS

A2	A1	A0
0	0	0

DATA

D12	TEST 1
D11	TEST 2
D10	TEST 3
D9	AUX. DATA SELECT
D8	REF OUT/3
D7	TX COUNTER ENABLE
D6	RX COUNTER ENABLE
D5	REF. COUNTER ENABLE
D4	AUX. REF. COUNTER ENABLE
D3	MUX SELECT 1
D2	MUX SELECT 2
D1	MUX SELECT 3
D0	MUX SELECT 4

Figure 4: 3 Wires Serial Data Transmission Timing



X = DON'T CARE

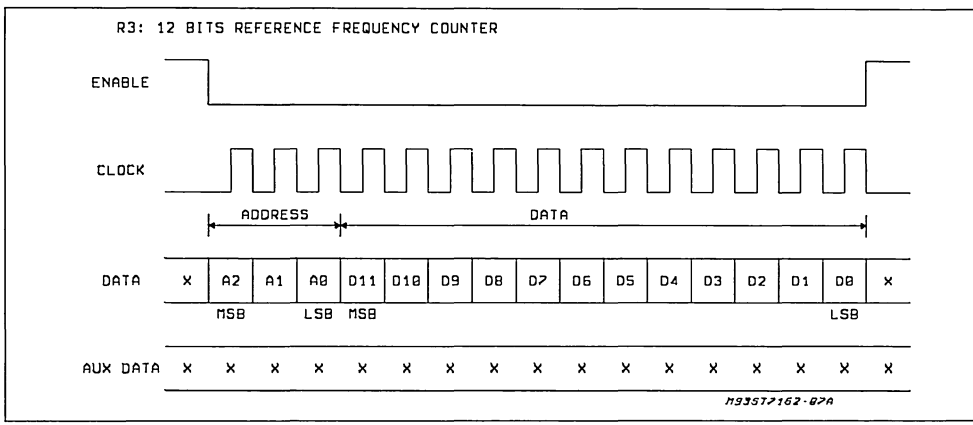
ADDRESS

A2	A1	A0	REGISTER
0	0	1	R1 : RX COUNTER
0	1	0	R2 : TX COUNTER

DATA

D15	MSB = 32768
:	
:	
:	
D0	LSB = 1

Figure 5: 3 Wires Serial Data Transmission Timing



X = DON'T CARE

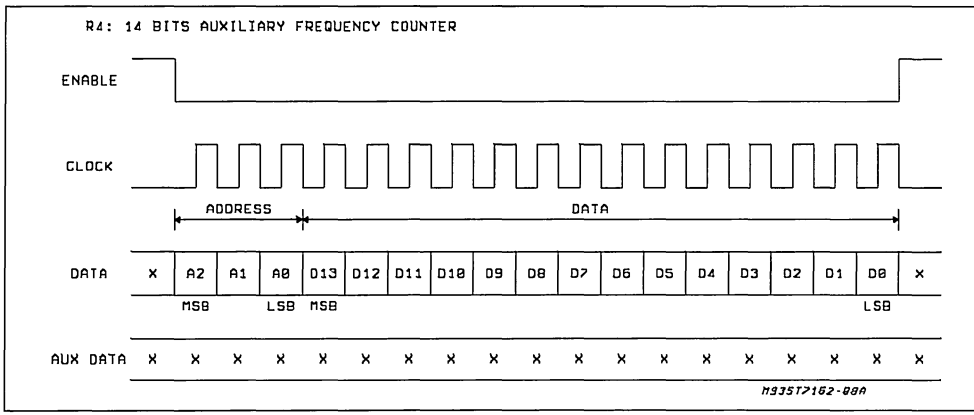
ADDRESS

A2	A1	A0	REGISTER
0	1	1	R3 : REF. COUNTER

DATA

D11	MSB = 2048
:	
:	
:	
D0	LSB = 1

Figure 6: 3 Wires Serial Data Transmission Timing



X = DON'T CARE

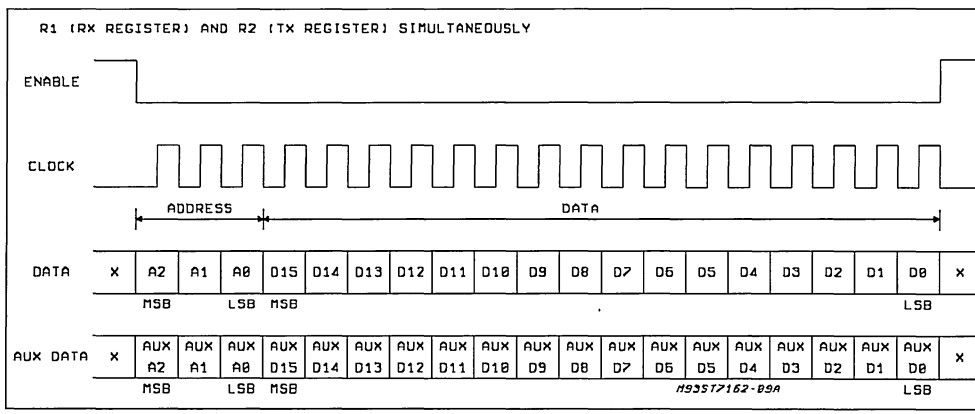
ADDRESS

A2	A1	A0	REGISTER
1	0	0	R4 : AUX REF. COUNTER

DATA

D13	MSB = 8192
:	
:	
:	
D0	LSB = 1

Figure 7: 4 Wires Serial Data Transmission Timing



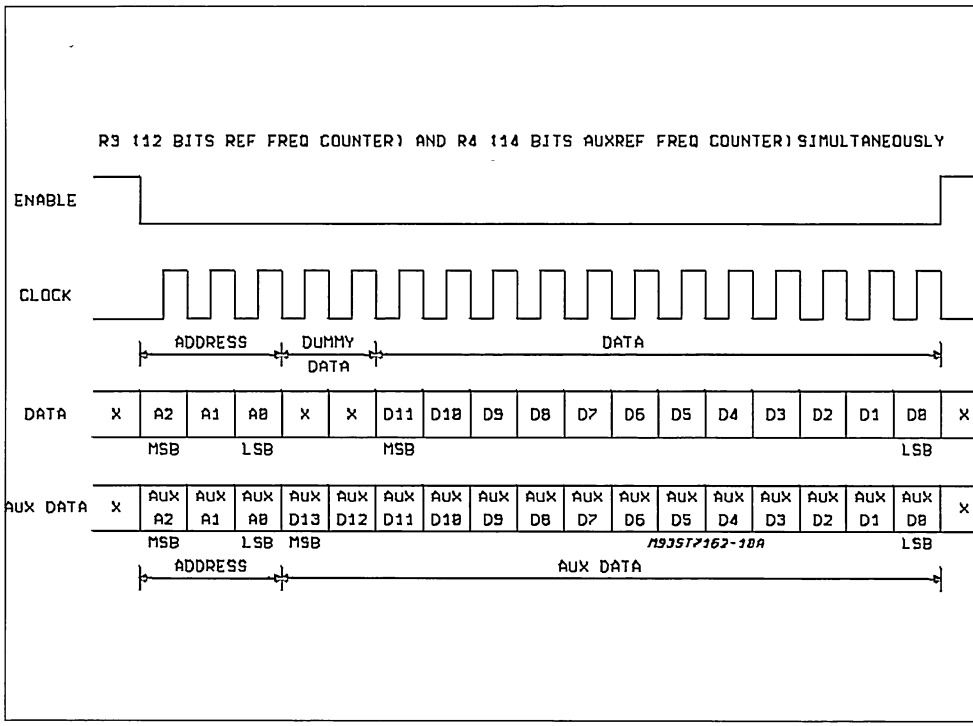
ADDRESS

A2 AUX A2	A1 AUX A1	A0 AUX A0	REGISTER
0	0	1	R1 : RX COUNTER
0	1	0	R2 : TX COUNTER

DATA

D15, AUX D15	MSB = 32768
:	
:	
:	
D0, AUX D0	LSB = 1

Figure 8: 4 Wires Serial Data Transmission Timing



X = DON'T CARE

ADDRESS

A2 AUX A2	A1 AUX A1	A0 AUX A0	REGISTER
0	1	1	R3 : REF COUNTER
1	0	0	R4 : AUX REF. COUNTER

DATA		AUX DATA	
D11	MSB = 2048	AUX D13	MSB = 8192
:		:	
:		:	
:		:	
D0	LSB = 1	AUX D0	LSB = 1

PFD DESCRIPTION (pin 10 & 15)

Outputs PDTX or PDRX produce an output pulse current, sourcing or sinking, whose width depends on the delay between falling edges of reference frequency and RF frequency divided. Simplified schematic of both PFD is described in figure 10. When the current output is off, PFD is in high impedance state. The voltage at PFD outputs pins depends on the loop filter and V_{CO} characteristics (Fig. 9)

Figure 9: PD Output Current vs. FIN / REF. Frequencies.

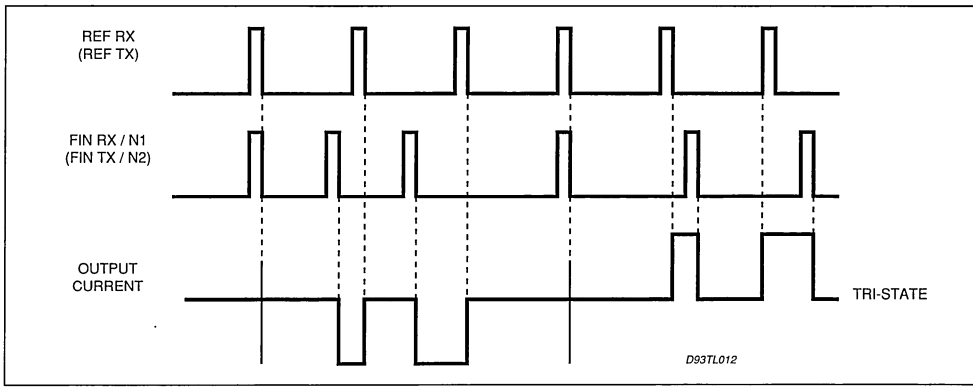
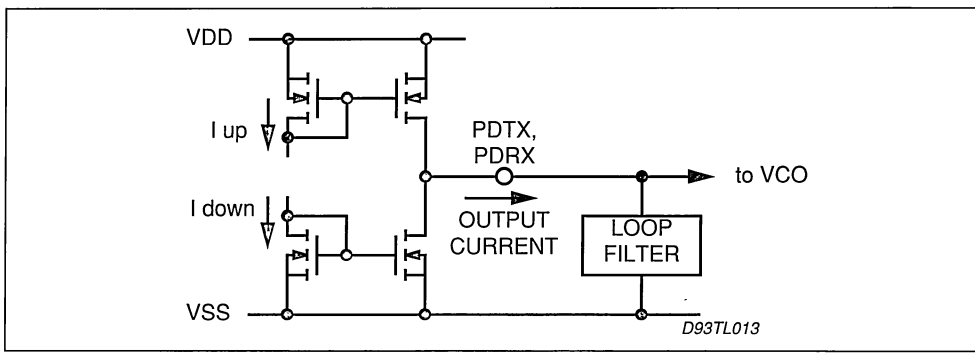


Figure 10: Simplified schematic of PFD outputs.



When the loop is locked, to prevent a dead area in the PFD gain due to switching delays, a very short phase offset is introduced in the loop, so the PFD output current show the following waveform Fig. 11.

Figure 11: PD output current in locked condition.

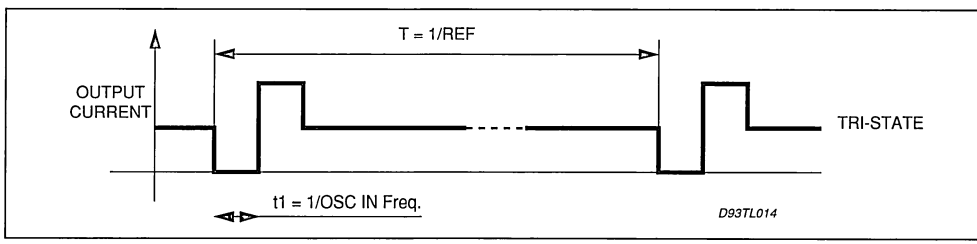


Figure 12: Switching diagrams.

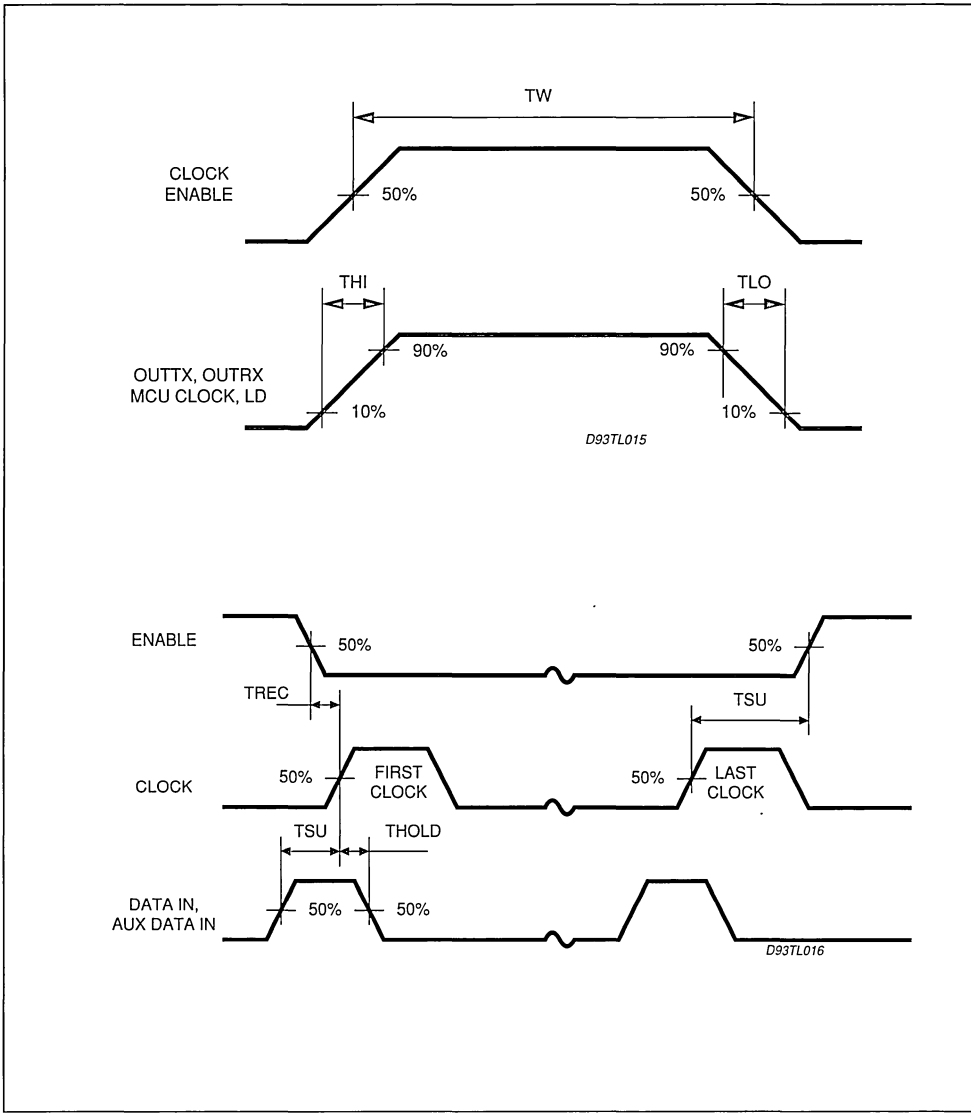
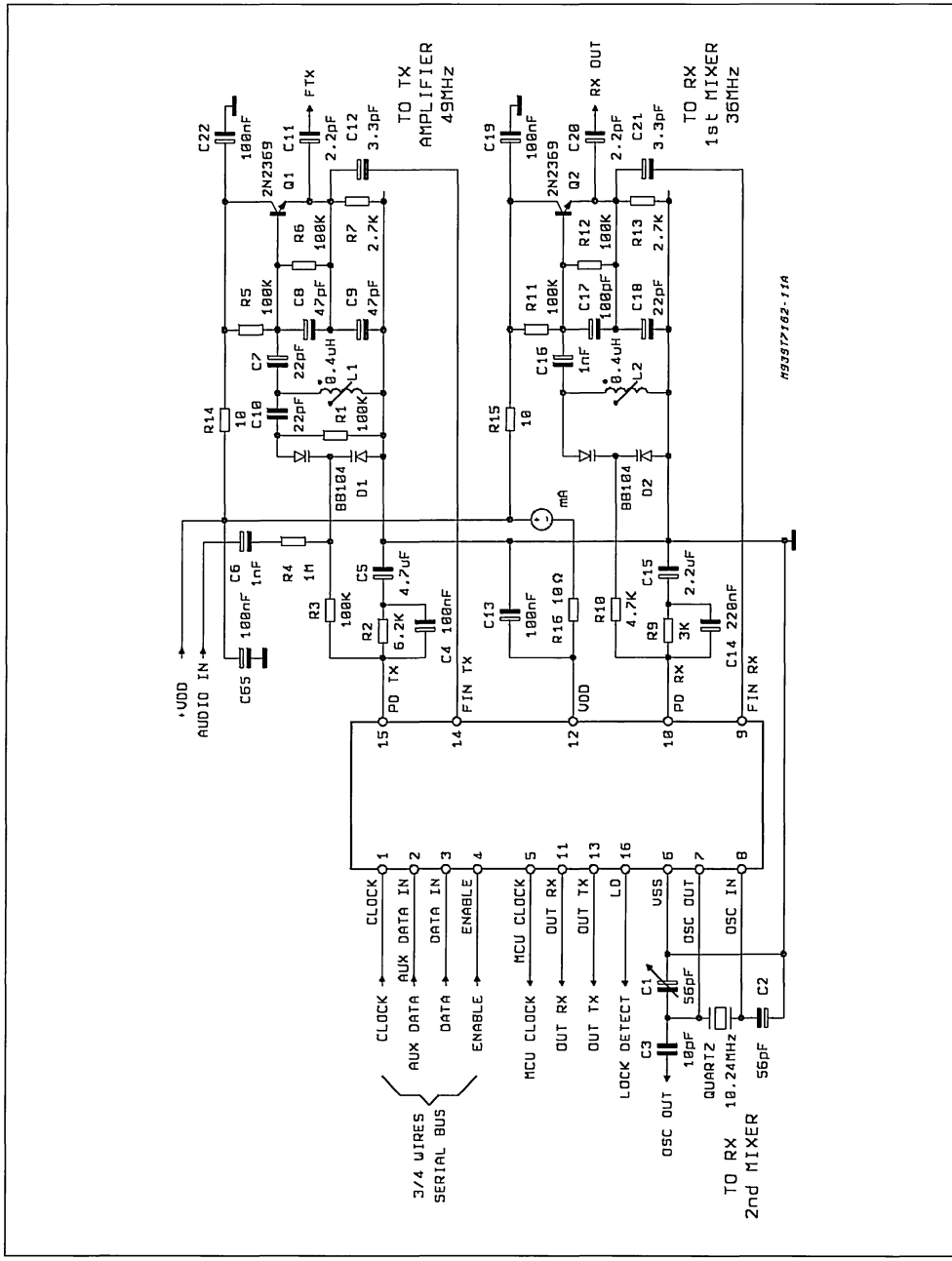
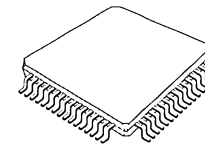


Figure 13: Test Circuit.



MULDEX IC FOR MULTIMEDIA TELESERVICES

- HCMOS SEA OF GATE TECHNOLOGY
- 64 PINS QUAD FLAT PACKAGE
- TWO MODES OF OPERATION: STAND-ALONE, MICROPROCESSOR
- INTERFACE FOR 8/16/32 BIT MICROPROCESSORS
- TRANSMITTER FUNCTIONS:
  Implementation of two electrical interfaces:
  - 64kbit/s only
  - to 4 up to 32 Time Slot Multiplex.
  Allocation of the multimedia frame structure in B channel for 32B channels.
  3 input internal multiplexer can multiplex up to 3 sources within the 64kbit/s output stream.
  Serial/Parallel input to the AC data:
  - Serial: using the 8th bit of the input stream.
  - Parallel: using bytes provided by microprocessor.
  Serial/parallel input for the seven sub-channels.
- RECEIVER FUNCTIONS:
  Implementation of two electrical interfaces:
  - 64kbit/s only
  - to 4 up to 32 Time Slot Multiplex
  Allocation of the multimedia frame structure in Bchannel of 32 channels.
  3 Output internal demultiplexer can demultiplex up 3 signals provided by the 64kbit/s input stream.
  Serial/parallel output for AC data:
  - Serial: using the 8th bit of the output stream.
  - Parallel: using bytes provided by microprocessor.
  Serial/parallel output for the seven subchannels.
- OTHER GENERAL ASPECTS:
  Interrupt procedures to access 16 input registers and 10 output registers.
  Working with/without external byte synchronization depending on Protocol Select Pin and bit programmation.
  The emitter and receiver provide superframe synchronization.
  Error correction on BAS (up to two consecutive errors can be corrected, three are detected).
  Fast receiver synchronization (parallel method).



PQFP64

ORDERING NUMBER: STH221

DESCRIPTION

The ·H221/Muldex integrated circuit is a multiplex/demultiplex for a frame structure with 8-bit data channel. Manufactured using HCMOS "Sea of gates" technology, the device requires a single 5 V supply and is available in a 64 pin Quad Flat Package. The H221/Muldex implements the frame structure for a 64 kbit/s channel in audiovisual teleservices as defined by CCITT in the H.221 recommendation with automatic generation/decoding of FAW and error correction detection on BAS. It also implements the CRC4 algorithm for error detection on the sub-multiframe structure and allows the possibility of serial and/or parallel input/output of data channels (including the AC channel). In addition the multiframe structure is supported with automatic generation/decoding of the Multiframe Alignment Word and enabling of multiframe count. The H221/Muldex is controlled by a microprocessor using an 8-bit data bus or can function in a stand-alone mode; standard 64 kbit/s or time division multiplex interface are implemented.

PIN CONNECTION (Top view)

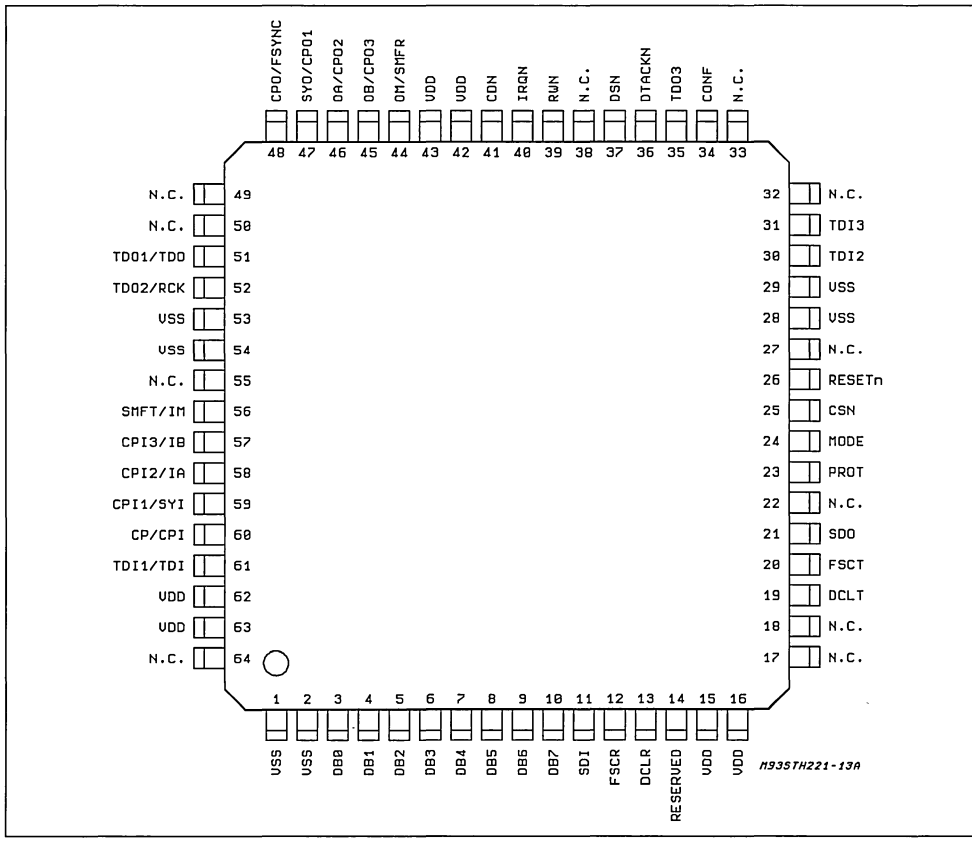


Table 1: Alphabetical Listing of Symbols.

Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin
CDN	41	DB0	3	SMFR/OM	44	VSS	1,2,28,29,53, 54
CONF	34	DB1	4	FSCR	12	SMFT/IM	56
CP/CPI	60	DB2	5	FSCT	20	TDI1/TDI	61
CPI1/SYI	59	DB3	6	FSYN/CPO	48	TDI2	30
CPI2/IA	58	DB4	7	IRQN	40	TDI3	31
CPI3/IB	57	DB5	8	MODE/TEST	24	TDO1/TDO	51
CPO1/SYO	47	DB6	9	PROT	23	TDO2/RCK	52
CP02/OA	46	DB7	10	RESETN	26	TD03	35
CP03/OB	45	DCLR	13	RWN	39	VDD	15,16,42,43, 62,63
DSN	37	DCLT	19	SDI	11	CSN	25
DTACKN	36	SDO	21				

Pin 16 must not be connected.

Table 2: Pin Description.

Pin	Symbol	Mode	Type	Function
3-10	DB0-DB7	I/O	CPU	**I/O Data µP Interface.**
11	SDI	I	Rx	**Serial Data Input**. Input of serial stream from line into the receiver. 64 kbit/s or 256 kbit/s up to 2048kb/sec (GCI).
12	FSCR	I	Rx	**Frame Syncro Rx.** Octet synchronization (if present) for the receiver.
13	DCLR	I	Rx	**Data Clock Rx.** Clock of input data for receiver. 64 khz or 512 up to 4096 khz (GCI)
19	DCLT	I	Tx	**Data Clock Tx.** Clock of output data from transmitter. 64 khz or 512 up to 4096 khz (GCI)
20	FSCT	I	Tx	**Frame Syncro Tx.** Octet syncronization (if present) for the transmitter.
21	SDO	O*	Tx	**Serial Data Output**. Output of serial stream from transmitter into B channel selected. Open drain in GCI mode.
23	PROT	I		**Protocol select**. Select of protocol implementation: 0 = 64 kbit/s 1 = Multiplex at 512 up to 2048kb/s.
24	MODE/ TEST	I		CONF = 1 Test is given by this pin. Specific test mode of the component. In normal operation, must be 0. CONF = 0. Selection of working mode. MODE = 0. Controlled by CPU (CPU mode) MODE = 1. Stand Alone (S-A Mode). mode). Test is given by Bit 3 of Command Register.
25	CSN	I	CPU	**Chip Select.** In CPU mode allows the selection of the component by the CPU: 0 = The CPU can access internal registers using RWN, CDN, DSN signals. 1 = The H221 is disabled. In S-A mode this pin represents the N5 bit of the H221 protocol (Enable/disable of the multiframe count).
26	RESETN	I		**Reset component**. Reset the H221 and initializes default conditions. Low Signal = active Minimum duration = 1µs.
30	TDI 2	I	Tx	**Terminal Data Input 2.** Serial input of data for the transmitter, clocked by CP. Data is shifted on the falling edge of CP. Usable only if CONF = 1 otherwise ignored.
31	TDI 3	I	Tx	**Terminal Data Input 3.** Serial input of data for the transmitter. Data is shifted on the falling edge of CP. Usable only if CONF = 1 otherwise ignored.
34	CONF	I		**Configuration.** CONF = 0. CPI, TDI, SYI, IA, IB, IM, OM, TDO, CPO, SYO, OA, OB, RCK, Mode pins are validated. CONF = 1. CP, TDI 1/3, CPI 1/3, TDO 1/3, CPO 1/3, SMFT, SMFR, TEST, FSYN pins are validated.
35	TDO 3	O	Tx	**Terminal Data Output 3.** Serial Output of data received. Data is shifted on the rising edge of CP. If CONF = 1: Open Drain else TDO3 = 0.
36	DTCAKN	O	CPU	**Data Acknowledge**. Data acknowledge for writing from CPU and data ready for reading. 1 = Data not yet ready or acknowledged. 0 = Data ready or acknowledged. In S-A mode it represents the Aloc signal.
37	DSN	I	CPU	**Data Strobe**. Strobe signal for data I/O from/to CPU. 0 = Data Valid on data bus. In S-A mode it is used to strobe the BAS data on the data bus.

Table 2: Pin Description.

Pin	Symbol	Mode	Type	Function
39	RWN	I	CPU	**Read or Write**. Indicates whether the next data transfer performed is a read or a write. 0 = Write operation. 1 = Read operation. In S-A mode it indicates the direction of the BAS data on data bus.
40	IRQN	OD	CPU	**Interrupt Request.** When low indicates that the H221 is requesting interrupt service. This lead goes high when the CPU performs the interrupt acknowledge. It is an open drain so pull-up resistor is needed. In S-A mode it represents the Eloc signal.
41	CDN	I	CPU	**Command or Data** Selection between the command register or the data registers set. 0 = The CPU accesses a data register. 1 = The CPU accesses the command register. In S-A mode it enables the computing of the CRC4 value by the transmitter. 0 = Tx computers CRC4 value. 1 = All 1's are transmitted on the CRC4 position (CRC4 disabled).
44	SMFR/ OM	O	Rx	CONF = 1. Submultiframe received. This signal goes high at the beginning of first bit of octet 1 of every submultiframe. It returns low at the beginning of first bit of octet 83 of every submultiframe. CONF = 0 Out Mask. Frame synchronization; it goes high before the beginning of first bit of octet 1 of every frame. It returns low between the 16th and the 72nd octet, depending on the programmed conditions. Valid only when the receiver is frame aligned.
45	CP03/ OB	O	Rx	CONF = 1. Clock pulse for data output 3. This signal is configurated by CPS and WIN bits. It is associated to TDO3 data CONF = 0. Out multiplex addr. B. LSB of the channel number of the bit on the TDO output.
46	CP02/ OA	O	Rx	CONF = 1. Clock pulse for data output 2. This signal is configurated by CPS and WIN bits. It is associated to TDO2 data. CONF = 0. Out multiplex addr. A. Together with OA and SYO indicates the channel number of the bit on the TDO output. These signals can be used to address an external demultiplexer separating 8 sub-channels.
47	SYO/ CPO1	O	Rx	CONF = 1. Clock pulse for data output 1. This signal is configurated by CPS and WIN bits. It is associated to TD01 data. CONF = 0. Synchro Output MSB of the channel number of the bit on the TDO output. It also represents the synchronization octet; SYO is low at the beginning of the octet.
48	FSYN/ CPO	I	-	CONF = 1. Frame Synchronization. This 8kHz signal indicates the first bit of the first time slot for TDO1, TDO2, TDO3, TDI1, TDI2, TDI3 multiplex. CONF = 0 Clock Pulse Output; Clock for the output of data from receiver. The clock input must have a mimimum frequency of 64 KHz and a maximum frequency of 2 MHz. Signals OA, OB and SYO have meaning only whne CPO has a 64 KHz frequency.

Table 2: Pin Description.

Pin	Symbol	Mode	Type	Function
51	TDO1/ TDO	TS/O	Rx	CONF = 1. Terminal Output 1. Serial output of data received. Data is shifted on the rising edge of CP. OPEN DRAIN CONF = 0. Terminal Data Output. Serial output of data received, clocked by CPO. Data is shifted on the leading edge of CPO.
52	TDO2/ RCK	TS/O	Rx	CONF = 1. Terminal Output 2. Serial output of data received. Data is shifted on the rising edge of CP. OPEN DRAIN CONF = 0. Rx Clock. A 64 KHz clock recovered by the receiver from the incoming stream.
56	SMFT/ IM	0	Tx	CONF = 1. Submultiframe transmitted. This signal goes high at the beginning of first bit of octet 1 of every submultiframe. It returns low at the beginning of first bit of octet 8 of every submultiframe. CONF = 0. Input Mask. Input Mas. Frame synch; it goes high before the transmission of the first bit of octet # 1 of every frame. It returns low between the 16th and the 72nd octet, depending on the programmed conditions.
57	CPI3/ IB	0	Tx	CONF = 1. Clock Pulse for data input 3. This signal is configurated by CPS and WIN bits. It is associated to TDI3 data. CONF = 0. Input Mask. In multiplex addr. B. LSB of the channel number of the bit on the TDI input.
58	CPI2/ IA	0	Tx	CONF = 1. Clock Pulse for data Input 2. This signal is configurated by CPS and WIN bits. It is associated to TDI2 data. CONF = 0. In Multiplex Addr. A In multiplex addr. A. Together with IA and SYI indicates the channel number of the bit on the TDI input. These signals can be used to address the multiplexing of 8 sub-channels.
59	CPI/ SYI	O	Tx	CONF = 1. Clock Pulse for data input 1. This signal is configurated by CPS and WIN bits. It is associated to TDI1 data. CONF = 0. Input Synchronization .Input Sync. MSB of the channel number of the bit on the TDI input. It also represents the sync of the outgoing octet i.e. SYI is low at the beginning of the octet.
60	CP/CPI	I	Tx-Rx/ Tx	CONF = 1. Clock Pulse. This signal is used to generate six clock pulses: CPI1, CPI2, CPI3 and CPO1, CPO2, CPO3. Its frequency is twice binary data rate of TDI1, TDI2, TDB and TDO1, TDO2, TDO3 multiplex. Minimum frequency 128kHz. Maximum frequency 4096kHz. CONF = 0. Clock Pulse input. Clock for the input of data into transmitter. The clock input must have a minimum frequency of 64kHz and a maximum frequency of 2 MHz. Signals IA, IB and SYI have meaning only when CPI has a 64kHz frequency.
61	TDI1/ TDI	I	Tx	CONF = 1. Terminal Data Input 1. Serial input of data for the transmitter. Data is shifted on the falling edge of CP. CONF = 0. Terminal Data Input. Serial input of data for the transmitter, clocked by CPI. Data is shifted on the leading edge of CPI.

OVERVIEW

The H221/Muldex performs complete multiplexing/demultiplexing according to the CCITT H.221 recommendation. It generates and decodes frame and multiframe structure automatically without intervention by the host CPU. The host CPU must initialize the H221 registers and supply or read BAS and AC information upon request. The CPU is notified of important events via interrupt. The H221/Muldex contains a receiver, a transmitter and an interface unit (fig. 1).

ARCHITECTURE

Transmitter

The transmitter can work in two main modes: unframed or framed. In the first mode, octets to be transmitted are shifted out on the serial data output (SDO) without any data insertion or control; in framed mode, the transmitter constructs the frame, submultiframe and multiframe structure. Data is shifted on the rising edge of the data clock signal (DCLT).

In framed mode the transmitter handles bit # 8 of the octets: it puts into octets 1 to 16 information that identifies the frame structure (FAW, BAS, Parity, CRC4, A, E, according to the submultiframe); into octets 17 to 80 the transmitter puts the AC channel information.
This data can be sent to the AC register of the transmitter by the host CPU or can be the 8th bit of the incoming bit stream, depending on the configuration set by CPU. A request for AC data is made by the CPU via interrupt; the transmitter generates an interrupt request 1mS before it needs the data. After this time it transfers the AC data into internal register and starts the transmission of the next 8 octets. Then the cycle restarts with another interrupt request.

The same mechanism is applied to the BAS data request; SMFT pin generates a signal every 20ms.

This submultiframe transmit signal is at "1"during FAS transmitting. CPU can update if necessary BAS data and configuration registers TDI1R, TDI2R, TDI3R, when SMT is low. BAS data will be emitted during the next submultiframe and the new configuration of TDI1, TDI2, TDI3 multiplex will be actual after this next submultiframe. If not updated, old data is emitted.

The transmitter puts into the first bit of every information that identifies the multiframe structure; some are fixed and generated by the transmitter (MAW), others are variable (multiframe counter, L1, L2, L3, R bits and TEA). When enabled, the multiframe count is generated automatically by the transmitter, if disabled, all zeroes are transmitted; other bits are sent by the host CPU into the TFAS register. This data is transferred into internal register for transmission at the beginning of a multiframe (i.e. on the first bit of the frame # 0); if necessary data can be updated by the CPU before the end of a multiframe; no interrupt request is generated for this data.

The transmitter also computes the CRC4 value of a submultiframe and puts this value on the next odd frame according to the CCITT H221 recommendation; at reset, for the first two frames a zero value is transmitted; if the CRC4 computing is not enabled, the transmitter sends all ones in the CRC4 position.

Receiver

The receiver, like the transmitter, has two working modes: unframed and framed. In the first mode, octets received into the serial input (SDI) are shifted out on the terminal data (TDO) without any control or synchronism search; in framed mode, the receiver detects frame and multiframe alignment words (FAW and MAW) following procedures specified in CCITT H221 recommendation. When frame alignment is obtained, the receiver computes parity for BAS data; it uses this data for correcting up to two errors on BAS; 3 errors are detected.

If aligned, the receiver also decodes AC data; the availability of the data is signalled to the host CPU via interrupt; the CPU has 1ms to remove the data before the AC register is updated with the new value. The AC data is also available as the 8th bit of octets on terminal data output (TDO) when the component is receiving octets 17 to 80. The number of interrupt generated for the AC channel depends on the configuration set by CPU.

BAS register (RBAS) is updated every submultiframe when receiving octet 17 of the odd frame (i.e. after the parity has been verified); CPU can read BAS data when SMFR is low. SMFR pin generates a signal every 20ms. This Submultiframe Receive Signal is at "1"during an even frame and FAS and BAS receiving of odd frame. After reading BAS data, CPU can load immediately into TDO1R, TDO2R, TDO3R register when SMFR is yet low to change the configuration of TDO1, TDO2, TDO3 multiplex if necessary. Errors detected on BAS data (corrected or not) are signalled to the host CPU via interrupt; reading the receiver status register the CPU can determine the type of error.

The data on the BAS register is not valid if errors on BAS are not recoverable. In the first bit of every frame the receiver reads information concerning multiframe structure; registers that hold this information (multiframe counter (RC), L1, L2, L3, R bits and TEA (RFAS)) are updated at the beginning of a multiframe; the CPU can read multiframe data at any time except on the first octet of the first frame of a multiframe.

The receiver also computes the CRC4 value of a submultiframe and compares it with the received value of CRC4; if discrepancies are found, bit Eloc is set and an interrupt is generated; error interrupts are generated at the beginning of a frame only when some error condition are present.

Interface

The interface unit provides interface between the host CPU and the H221 Muldex transmitter and receiver via data bus and some control signals. The interface holds general purpose register and decoding logic for the addressing of transmitter and receiver registers. Using data-strobe/data-acknowledge protocol, the H221/Muldex can interface CPU that use synchronous or asynchronous read/write cycles.

PRINCIPLES OF OPERATION

CPU Interface

The CPU has direct access into two register, command or data, using the CDN signal. The data register is split in 16 registers; the address of the data register is specified in the command register. The CPU configures the H221/Muldex by writing the command and data registers. Status information can be accessed by reading one of the status registers and is used to monitor the H221/Muldex operation. The most useful information is coded in the command/status register for fast access by the CPU.

H221 Registers

The H221/Muldex registers are divided into four classes: command/status, receiver, transmitter, test.

Command/Status Register. Direct access by CPU when CDN signal is high; contains interrupt and error flags, controls the addressing of data registers, the clearing of interrupt flags, the test mode and the start of the transmitter.

Receiver Registers. These registers contain information received: multiframe data, BAS data, AC data, octet. Other registers contain status information of the receiver: frame and multiframe counters, AC counter, status bit indicating level of synchronization achieved (octet, frame, multiframe).

Transmitter Registers. These registers contain information to be transmitted: multiframe data, BAS data, AC data, octect. Other registers contain status information of the transmitter: frame and multiframe counters, AC counter, bits programming the operating mode of the transmitter.

Test Register. These registers contain data used for the testing of the component; not used in normal operation.

Table 3: Common/Status Register Definition.

Bit	7	6	5	4	3	2	1	0
(Write) Field	IR	IT	IE	S	W3/T	W2	W1	W0

Bit	Symbol	Name/Description
0	W0	**Data Register Address** (bit 0). Interpreted with W1 (bit 1) and W2 (bit 2) and W3 [(bit 3) + if CONF = 1] as the address of the data register as indicated by the following table:

W3	W2	W1	W0	Write	Read
0	0	0	0	TFAS	RFAS
0	0	0	1	TBAS	RBAS
0	0	1	0	TAC	RAC
0	0	1	1	TEST	TC
0	1	0	0	TEST	RC
0	1	0	1	COND	RXST
0	1	1	0	ACS/TEST	RTACC
0	1	1	1	TPD	RPD
		Available only if CONF = 1			
1	0	0	0	TSAA	TBCR
1	0	0	1	TDO1R	-
1	0	1	0	TDO2R	-
1	0	1	1	TDO3R	-
1	1	0	0	TSAN	RBCR
1	1	0	1	TDI1R	-
1	1	1	0	TDI2R	-
1	1	1	1	TDI3R	-

Forced to 1 if MODE pin is high and CONF = 0.

Bit	Symbol	Name/Description
1	W1	**Data Register Address** (bit 1). Forced to 0 when MODE pin is high and CONF = 0.
2	W2	**Data Register Address** (bit 2). Forced to 0 when MODE pin is high and CONF = 0.
3	W3/T	**Data Register Address** (bit 3) if CONF = 1. **CR Test if CONF = 0.** Specifies test mode of the component. In normal operation must be 0. T is cleared by hardware reset or by software reset (bit RSN of COND register). If CONF = 1, this function is performed through pin MODE/TEST
4	S	**Start/Interrupt Enable**. When this bit goes high, the transmitter starts transmitting the first bit of the first frame of a multiframe. If it remains high, generation of all interrupts is enabled. If it returns low interrupts are disabled. Two consecutive writes to this bit (1-0) are sufficient to start the transmitter. The transmitter starts on the second falling edge of SYI signal (fig. 5). S is cleared by hardware reset or by software reset (bit RSN of COND register).
5	IE	**Error Interrupt Acknowledge**. Writing 1 on this bit clears the corresponding interrupt flag.
6	IT	**Transmitter Interrupt Acknowledge**. Writing 1 on this bit clears the corresponding interrupt flag.
7	IR	**Receiver Interrupt Acknowledge**. Writing 1 on this bit clears the corresponding interrupt flag.

Table 3: Common/Status Register Definition. (Continued)

Bit	7	6	5	4	3	2	1	0
(Read) Field	IR	IT	IE	ELOC	ALOC	EBC	EB	0

Bit	Symbol	Name/Description
0	–	**Unused bit**. Read always as zero.
1	EB	**BAS Data Error** When 1 indicates an unrecoverable error on the BAS data. This bit is updated on a submultiframe basis.
2	EBC	**BAS Data Error Recovered** When 1 indicates that BAS data has been received with an or 2 errors and that error has been corrected by the error correction logic.
3	ALOC	**Local Alignment**. When 0 indicates that the receiver is aligned on frame and multiframe. The same bit is transmitted as bit A of the frame if ASEL bit of ACS/TEST register allows it.
4	ELOC	**Local Error**. When 1 indicates a difference between the CRC4 value calculated by the receiver and the CRC4 received. The same bit can be transmitted as bit E of the frame
5	IE	**Error Interrupt Flag.** When 1 indicates that an error interrupt has been generated by the component. It returns 0 on error interrupt acknowledge.
6	IT	**Transmitter Interrupt Flag**. When 1 indicates that a transmitter interrupt has been generated by the component. It returns 0 on transmitter interrupts acknowledge.
7	IR	**Receiver Interrupt Flag.** When 1 indicates that a receiver interrupt has been generated by the component. It returns 0 on receiver interrupt acknowledge.

Table 4: TFAS Register Definition (Address 0000).

Bit	7	6	5	4	3	2	1	0
(Write) Field	EPI	SYNEXT	N5	TEA	R	L3	L2	L1
Hardware RESET configuration	0	1	X	0	0	0	0	0

Bit	Symbol	Name/Description
0-3	L1-L3, R	**L1-L3, R bits.** L1-L3 and R bits of H221 multiframe structure. Cleared by hardware or software reset.
4	TEA	**TEA bit**. Terminal Equipment Alarm bit to be transmitted. Cleared by hardware or software reset.
5	N5	**N5 bit**. Multiframe count enable. When 1 the transmitter counts multiframe sending multiframe number in descending order on bit N1N4 (N1 = LSB). No default on reset.
6	SYNEXT	**Transmitter Octet Syncro Valid.** Specifies if external octet synchro is valid. If 1, the external octect syncro is present and valid; if 0, the octet synchro may be present but it is not taken into account by transmitter. Hardware or software reset forces this bit to 1.
7	EPI	**Enable Parallel Input**. When 1 enables parallel input of data to be transmitted using TPD register. If this bit is 0 data enters serially through the TDI input. Cleared by hardware or software reset.

Table 5: RFAS Register Definition (Address 0000).

Bit	7	6	5	4	3	2	1	0
(Read) Field	0	0	N5	TEA	R	L3	L2	L1

Bit	Symbol	Name/Description
0-3	L1-L3, R	**L1-L3, R bits.** L1-L3 and R bits of H221 multiframe structure.
4	TEA	**TEA bit**. Terminal Equipment Alarm bit received.
5	N5	**N5 bit**. Enable multiframe count bit received. If 1 the remote transmitter has multiframe numbering enabled.
6-7	–	**Unused bits**. Read as zero.

Table 6: TBAS and RBAS Register Definition (Address 0001).

Bit	7	6	5	4	3	2	1	0
Field	b_0	b_1	b_2	b_3	b_4	b_5	b_6	b_7

Bit	Symbol	Name/Description
0-7	b_0b_7	**BAS Data.** BAS data to be transmitted (TBAS Register write) or received (RBAS Register read). b_0 is the MSB and b_7 the LSB as defined by CCITT.

Rem: Hardware RESET is inactive on configuration.

Table 7: TAC and RAC Register Definition (Address 0010).

Bit	7	6	5	4	3	2	1	0
Field	AC_7	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0

Bit	Symbol	Name/Description
0-7	AC_0AC_7	**AC Data.** AC data to be transmitted (TAC Register write) or received (RAC Register read). In TAC register AC_0 is the first bit transmitted while in RAC register AC_0 represents the last bit received.

Rem: Hardware RESET is inactive on configuration.

Table 8: TC Register Definition (Address 0011).

Bit	7	6	5	4	3	2	1	0
(Read) Field	TN_4	TN_3	TN_2	TN_1	TF_3	TF_2	TF_1	TF_0

Bit	Symbol	Name/Description
0-3	TF_0TF_3	**Transmitter Frame Counter.** Indicates the frame number in transmission (i.e. the frame position within the multiframe structure). TF_0 is the LSB.
4-7	TN_1TN_4	**Transmitter Multiframe Counter.** Indicates multiframe number in transmission and represents bit N1N4 of the multiframe structure. TN_1 is the LSB.

Rem: Write register used for TEST only '
: No access to user

Table 9: RC Register Definition (Address 0100).

Bit	7	6	5	4	3	2	1	0
(Read) Field	RN_4	RN_3	RN_2	RN_1	RF_3	RF_2	RF_1	RF_0

Bit	Symbol	Name/Description
0-3	RF_0RF_3	**Receiver Frame Counter.** Indicates the receiving frame number (i.e. the frame position within the multiframe structure). RF_0 is the LSB.
4-7	RN_1RN_4	**Receiver Multiframe Counter.** Indicates bit N1 N4 of the received multiframe structure. RN_1 is the LSB.

Rem: WRITE register used for TEST only
: No access to user.

Table 10: COND Register Definition (Address 0101).

Bit	7	6	5	4	3	2	1	0
(Write) Field	ENEL	ENCRC	SYNEXR	RSN	ACS	N5IEN	B1B2N	FUN
Hardware RESET Configuration	1	0	0	1	1	1	1	1

Bit	Symbol	Name/Description
0	FUN	**Framed or Unframed Mode.** Specifies if the transmitter generates frame and multiframe structure. If 1 the transmitter sends FAS, BAS, AC, CRC4, A, E and multiframe information on bit 8 of transmitting data. If 0 the 8th bit is passed as is from TDI input to SDO output. Hardware reset forces this bit to 1.
1	B1B2N	**B1 or B2 Position.** When GCI mode active and CONF set to 0, specifies the position of the octet on the input or output data stream. If 1 the octet is placed on B1 position; if 0 on B2 position. In 64 kbit/s mode or CONF set to 1, B1B2N has no meaning. Hardware reset forces this bit to 1. When CONF is set to 1, the desired position is defined through bits 4 to 0 of TSAN register (TSN4, TSN3, TSN2, TSN1, TSN0).
2	N5IEN	**N5 Internal or External.** Specifies the source of N5 bit (multiframe count enable). If 1 the N5 bit of the transmitter is the complement of the Aloc bit of the receiver. In this case the transmitter starts multiframe count automatically when the receiver is aligned. If N5IEN = 0, the N5 bit of the transmitter is the bit contained in the TFAS register. In this case the transmitter starts multiframe count when the CPU writes 1 on N5 bit of TFAS register. Hardware reset forces this bit to 1.
3	ACS	**AC Mode Select.** Specifies the way AC data is exchanged with the terminal: parallel or mixed mode (serial/parallel). If 0, AC data are sent to H221/Muldex by CPU through data bus 8 bits at a time (parallel mode) upon interrupt request. Eight interrupt requests are generated by the transmitter at the beginning of octets 9, 17, 25, 33, 41, 49, 57, 65; the CPU has 1mS to update the AC register (TAC), then the 8 bits of AC are transmitted (for data requested on octet 9 the transmission starts at octet 16 and ends at octect 24, AC0 bit first). Eight interrupt requests are generated by the receiver at the beginning of octets 25, 33, 41, 49, 57, 65, 73, 1; the CPU has 1ms to remove data from AC register (RAC), then the AC register is updated with the new received data (in octet 25 is presented data received in octets 16 to 24, AC0 bit first). If the ACS bit is 1, AC data are sent to H221/Muldex in a mixed mode (parallel/serie). Parallel data are requested first; the number of parallel AC data is specified on bits $ACSE_0$ $ACSE_2$ of ACS/TEST register. The remaining part of the AC data is sent to the transmitter as the 8th bit of the stream coming into the TDI pin. Interrupt request is generated only for parallel data. The receiver gives AC data simultaneously in both ways but generates interrupt request only for parallel data. Hardware reset forces this bit to 1.

Table 10: COND Register Definition (Continued).

Bit	Symbol	Name/Description
4	RSN	**Reset Software**. When 0, this bit forces reset state of the component and initializes default conditions in all registers except the COND register itself. Hardware reset forces this bit to 1.
5	SYNEXR	**Receiver Octet Syncro Valid**. Specifies if external octet synchro is valid. If 1, the external octet synchro is present and valid; if 0, the octet synchro may be present but it is not taken into consideration by the receiver. Hardware reset forces this bit to 0.
6	ENCRC	**Enable CRC4 Calculation**. Specifies whether the transmitter has to calculate and transmit the value of CRC4. If 1, the transmitter calculates and transmits the CRC4 value; if 0, the value of CRC4 is not calculated and all ones are transmitted on the CRC4 position. Hardware reset forces this bit to 0.
7	ENEL	**Enable transmission of Eloc.** Specifies is the Eloc signal is passed from the receiver to the transmitter. If 1, the receiver passes the Eloc bit (the result of comparison between CRC4 received and calculated) to the transmitter. If 0, no value is transferred and the transmitter always sends 0 on the E bit position. Hardware reset forces this bit to 1.

Table 11: RXST Register Definition (Address 0101).

Bit	7	6	5	4	3	2	1	0
(Read) Field	CRCA1	–	–	SM	SF	SO	E	A

Bit	Symbol	Name/Description
0	A	**Alignment Loss**. When 1 indicates a loss of alignment in the remote receiver. It represents the A bit received in odd frames.
1	E	**CRC4 Error**. When 1 indicates an error on the CRC4 computing by the remote receiver. It re presents the E bit received in odd frames.
2	SO	**Octet Synchronization**. When 1 indicates that the receiver has achieved octet synchronization by recognizing the FAS position on the frame structure.
3	SF	**Frame Synchronization**. This bit goes high when the receiver validates the received frame as specified by CCITT H221 rec. It remains high until a loss of frame alignment is recognized.
4	SM	**Multiframe Synchronization**. This bit goes high when multiframe alignment is achieved by the receiver that recognizes the multiframe alignment signal. It returns low when three consecutive multiframe alignment signals have been received with an error.
5-6	–	**Unused bits**. Read undefined.
7	CRCA1	**CRC4 All Ones**. When 1 indicates that the received CRC4 data contains all ones. This can be a symptom that indicates the disabling of the CRC4 calculation by the remote transmitter.

Table 12: ACS/TEST Register Definition (Address 0110).

Bit	7	6	5	4	3	2	1	0
(Write) Field	$ACSE_2$	$ACSE_1$	$ACSE_0$	RRES	ASEL	AEXT	RSBT	RCL
Hardware RESET Configuration	0	0	0	0	0	X	0	X

Bit	Symbol	Name/Description
0	RCL	**Recirculate Control** Specifies recirculating of the output stream into the receiver for local testing purposes. If 1, the output of the transmitter is internally recirculated into the receiver. The output pin (SDO) is forced to 1 when in 64 kbit/s mode (3-state when in GCI mode), the data on the input pin (SDI) is ignored. This bit has meaning only when bit T of command register is 1.
1	RSBT	**Reset bit timing**. When this bit goes high, the bit timing of the transmitter is initialized. This function may be used to synchronize two or more transmitters (fig. 6). Hardware or software reset force this bit to 0. Valid only when T bit of command register is 0; if bit T = 1 the RSBT bit should be 0.
2	AEXT	**External A bit**. Represents the value of the transmitted A bit when ASEL bit is 1. No default on hardware or software reset. Valid only when T bit of command register is 0; if bit T = 1 the AEXT bit should be 0.
3	ASEL	**A bit select**. This bit specifies the source of the A bit transmitted on odd frames. If 1 the value of A is that of the AEXT bit of this register (see below). If 0 the A bit is generated internally by the receiver and indicates the frame and multiframe alignment. Hardware or software reset force this bit to 0. Valid only when bit T of command register is 0; if bit T = 1 the ASEL bit should be 0.
4	RRES	**Receiver Restart**. Controls the restart of the receiver alignment. If 1, the receiver restarts octet, frame and multiframe alignment, regardless of the current level of alignment. Hardware reset forces this bit to 0.
5	$ACSE_0$	**AC Select**. (bit 0) Interpreted with $ACSE_1$ and $ACSE_2$ as the number of serial AC channels as indicated by the following table: $ACSE_2$ $ACSE_1$ $ACSE_0$ | IM/OM | AC# 0 0 0 | 16 | 8 0 0 1 | 72 | 1 0 1 0 | 64 | 2 0 1 1 | 56 | 3 1 0 0 | 48 | 4 1 0 1 | 40 | 5 1 1 0 | 32 | 6 1 1 1 | 24 | 7 The IM and OM signals go high at the beginning of the first octet of the frame and return low at the end of the octet indicated by the 4th column of the table. The 5th column indicates how many serial octets are input to the transmitter. When signals IM and OM are high, interrupt are generated respectively by the transmitter and the receiver; when signals return low no more interrupts are generated; in this way IM and OM signals indicate the switching between parallel and serial mode of AC channel. ACSE bits have meaning only when ACS bit of COND register is high; otherwise ACSE bit must be zero. Hardware reset forces this bit to 0.
6	$ACSE_1$	**AC Select**. (bit 1). Hardware reset forces this bit to 0.
7	$ACSE_2$	**AC Select**. (bit 2). Hardware reset forces this bit to 0.

Table 13: RTACC Register Definition (Address 0110).

Bit	7	6	5	4	3	2	1	0
(Read) Field	–	–	ACT_2	ACT_1	ACT_0	ACR_2	ACR_1	ACR_0

Bit	Symbol	Name/Description
0-2	ACR_0ACR_2	**Receiver AC Counter.** Indicates the byte number of the AC in the RAC register. E. g. when 0 indicates that RAC contains 8 bit of AC channel received in octets 17 to 24.
3-5	ACT_0ACT_2	**Transmitter AC Counter.** Indicates the byte number of the AC in the TAC register. E. g. when 0 indicates that CPU must write into TAC register AC data that will be transmitted in octets 17 to 24.
6-7	–	**Unused bits.** Read undefined.

Table 14: TPD and RPD Register Definition (Address 0111).

Bit	7	6	5	4	3	2	1	0
Field	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d0

Bit	Symbol	Name/Description
0-7	d_0d_7	**Parallel Data.** This register contains parallel data to be transmitted (TPD) or received (RPD). The TPD register is used by the transmitter only when the EPI bit of COND register is 1 and it must be updated by CPU every octet; its content is transferred on the output register on the rising edge of the clock (DCLT) that marks the beginning of the octet. THe RPD register is updated by the receiver on the first bit of the octet; CPU can read the register at any time but during the first bit of every octet. The bit d_7 is the first bit of the octet entered into the receiver and the first bit of the octet shifted out from the transmitter.

Rem: Hardware RESET is inactive on configuration.

Table 15: TSAA Register Definition (Address 1000).

Bit	7	6	5	4	3	2	1	0
(Write) Field	NM8	WIN	CPS	TSA4	TSA3	TSA2	TSA1	TSA0
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0-4	TSA0 - TSA4	Time Slot Side Application. These 5 bits indicate the time Slot selected of 32 Time Slots corresponding to 64kb/s channel for transmitting and receiving. The receiver delivers eight bits onto TD01, TD02, TD03 pins with clock pulses CP01, CP02, CP03 during the Time Slot selected.. The transmitter receives eight bits from TDI1, TDI2, TDI3 pins and delivers clock pulses CPI1 and CPI2 and CPI3 during the same Time Slot. Pulse relating to FAS and BAS is delivered if bit NM8 = 1.
5	CPS	Clock Pulse Simple. The Frequency of CPI1-3, CPO1-3 clocks and Data rate of TDI1-3, TDO1-3 are the same. CPS = 0 and WIN = 0. The frequencies of CPI1-3, CPO1-3 is twice Data rate of TDI-3, TDO1-3.
6	WIN	Window. WIN = 1. CPI 1-3 and CP0 1-3 pins deliver windows. WIN = 0. CPI 1-3 and CPO1-3 pins deliver clock pulses.
7	NM8	Non Masked bit 8. NM8 = 1. Clock pulse (or window) relating to FAS and BAS is delivered. NM8 = 0. Clock pulse (or window) relating to FAS and BAS is not delivered.

Table 16: TBCR Register Definition (Address 1000).

Bit	7	6	5	4	3	2	1	0
(Read) Field	TF0	TB6	TB5	TB4	TB3	TB2	TB1	TB0

Bit	Symbol	Name/Description
0-6	TB0-6	Transmit Byte. This counter indicates the number of octet which is being transmitted (Modulo 80).
7	TF0	Transmit frame. TF0 = 0 Even frame. TF0 = 1 Odd frame

Table 17: TDO1 Register Definition (Address 1001).

Bit	7	6	5	4	3	2	1	0
(Write) Field	R81	R71	R61	R51	R41	R31	R21	R11
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0	R11	Subchannel 1 Received is switched on TDO1 pin.
1	R21	Subchannel 2 Received is switched on TDO1 pin.
2	R31	Subchannel 3 Received is switched on TDO1 pin.
3	R41	Subchannel 4 Received is switched on TDO1 pin.
4	R51	Subchannel 5 Received is switched on TDO1 pin.
5	R61	Subchannel 6 Received is switched on TDO1 pin.
6	R71	Subchannel 7 Received is switched on TDO1 pin.
7	R81	Subchannel 8 Received is switched on TDO1 pin.

Table 18: TD02 Register Definition (Address 1010).

Bit	7	6	5	4	3	2	1	0
(Write) Field	R82	R72	R62	R52	R42	R32	R22	R12
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0	R12	Subchannel 1 Received is switched on TDO2 pin.
1	R22	Subchannel 2 Received is switched on TDO2 pin.
2	R32	Subchannel 3 Received is switched on TDO2 pin.
3	R42	Subchannel 4 Received is switched on TDO2 pin.
4	R52	Subchannel 5 Received is switched on TDO2 pin.
5	R62	Subchannel 6 Received is switched on TDO2 pin.
6	R72	Subchannel 7 Received is switched on TDO2 pin.
7	R82	Subchannel 8 Received is switched on TDO2 pin.

Table 19: TDO3 Register Definition (Address 1011).

Bit	7	6	5	4	3	2	1	0
(Write) Field	R83	R73	R63	R53	R43	R33	R23	R13
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0	R13	Subchannel 1 Received is switched on TDO3 pin.
1	R23	Subchannel 2 Received is switched on TDO3 pin.
2	R33	Subchannel 3 Received is switched on TDO3 pin.
3	R43	Subchannel 4 Received is switched on TDO3 pin.
4	R53	Subchannel 5 Received is switched on TDO3 pin.
5	R63	Subchannel 6 Received is switched on TDO3 pin.
6	R73	Subchannel 7 Received is switched on TDO3 pin.
7	R83	Subchannel 8 Received is switched on TDO3 pin.

Table 20: TSAN Register Definition (Address 1100).

Bit	7	6	5	4	3	2	1	0
(Write) Field	MGN2	MGN1	MGN0	TSN4	TSN3	TSN2	TSN1	TSN0
Hardware RESET Configuration	0	1	1	0	0	0	0	0

Bit	Symbol	Name/Description
0-4	TSN04	Time Slot Side Network. These 5 bits indicate the time slot selected of 32 time slots corresponding to 64kb/s channel for transmitting and receiving. The H221 frame is transmitted and received in this channel.
5-7	MGN0-2	Maximum channel group side network. These 3 bits indicate the number of group of 4 B channels which constituites the multiplexes side network. **MGN2 MGN1 MGN0** 0 0 1 1 group of 4 Time Slots 0 1 0 2 group of 4 Time Slots 0 1 1 3 group of 4 Time Slots 1 0 0 4 group of 4 Time Slots 1 0 1 5 group of 4 Time Slots 1 1 0 6 group of 4 Time Slots 1 1 1 7 group of 4 Time Slots 0 0 0 8 group of 4 Time Slots Example TSAN is 61(h); TSN = 1, MGN = 3. The emitter and the receiver are connected onto the Time Slot 1 of multiplex which is constituited by 12 Time Slots.

Table 21: RBCR Register Definition (Address 1100).

Bit	7	6	5	4	3	2	1	0
(Read) Field	RF0	RB6	RB5	RB4	RB3	RB2	RB1	RB0

Bit	Symbol	Name/Description
0-6	RB0-6	Byte received. These 7 bits indicate the number of octet received (Modulo 80).
7	RF0	Frame Received. RF0 = Even frame RF0 = 1 Odd Frame.

Table 22: TDI1 Register Definition (Address 1101).

Bit	7	6	5	4	3	2	1	0
(Write) Field	T81	T71	T61	T51	T41	T31	T21	T11
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0	T11	Subchannel 1 to be emitted comes from TDI1 pin.
1	T21	Subchannel 2 to be emitted comes from TDI1 pin.
2	T31	Subchannel 3 to be emitted comes from TDI1 pin.
3	T41	Subchannel 4 to be emitted comes from TDI1 pin.
4	T51	Subchannel 5 to be emitted comes from TDI1 pin.
5	T61	Subchannel 6 to be emitted comes from TDI1 pin.
6	T71	Subchannel 7 to be emitted comes from TDI1 pin.
7	T81	Subchannel 8 to be emitted comes from TDI1 pin.

Table 23: TDI2 Register Definition (Address 1110).

Bit	7	6	5	4	3	2	1	0
(Write) Field	T82	T72	T62	T52	T42	T32	T22	T12
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0	T12	Subchannel 1 to be emitted comes from TDI2 pin.
1	T22	Subchannel 2 to be emitted comes from TDI2 pin.
2	T32	Subchannel 3 to be emitted comes from TDI2 pin.
3	T42	Subchannel 4 to be emitted comes from TDI2 pin.
4	T52	Subchannel 5 to be emitted comes from TDI2 pin.
5	T62	Subchannel 6 to be emitted comes from TDI2 pin.
6	T72	Subchannel 7 to be emitted comes from TDI2 pin.
7	T82	Subchannel 8 to be emitted comes from TDI2 pin.

Table 24: TDI3 Register Definition (Address 1111).

Bit	7	6	5	4	3	2	1	0
(Write) Field	T83	T73	T63	T53	T43	T33	T23	T13
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0	T13	Subchannel 1 to be emitted comes from TDI3 pin.
1	T23	Subchannel 2 to be emitted comes from TDI3 pin.
2	T33	Subchannel 3 to be emitted comes from TDI3 pin.
3	T43	Subchannel 4 to be emitted comes from TDI3 pin.
4	T53	Subchannel 5 to be emitted comes from TDI3 pin.
5	T63	Subchannel 6 to be emitted comes from TDI3 pin.
6	T73	Subchannel 7 to be emitted comes from TDI3 pin.
7	T83	Subchannel 8 to be emitted comes from TDI3 pin.

Table 25: Circuit Configuration.

	Input/Output	PROT = 0	PROT = 1
CONF = 0	Side Network	DCLR = 64kHz DCLT = 64kHz	One GCI channel: Data rate 256kb/s DCLR = DCLT = 512kHz
	Side Application	13 signals for external multiplexer	
CONF = 1	Side Network	DCLR = 64kHz DCLT = 64KHz FSCR = FSCT must be supplied	1 to 8 GCI channels Data Rate n x 256kb/s DCLR = DCLT = n x 512kHz ($1 \leq n \leq 8$) FSR = FSCT 1 B channel selected of 32
	Side Application	3 Input Multiplex 3 Output Multiplex 1 64kb/s selected of 32	

Figure 1: Circuit Interfaces.

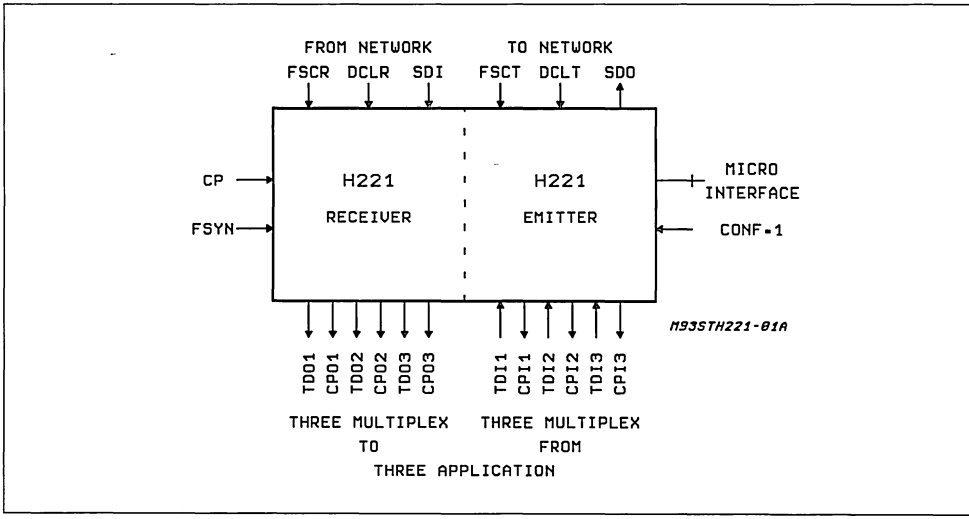


Figure 2: Video and Audio Terminal.

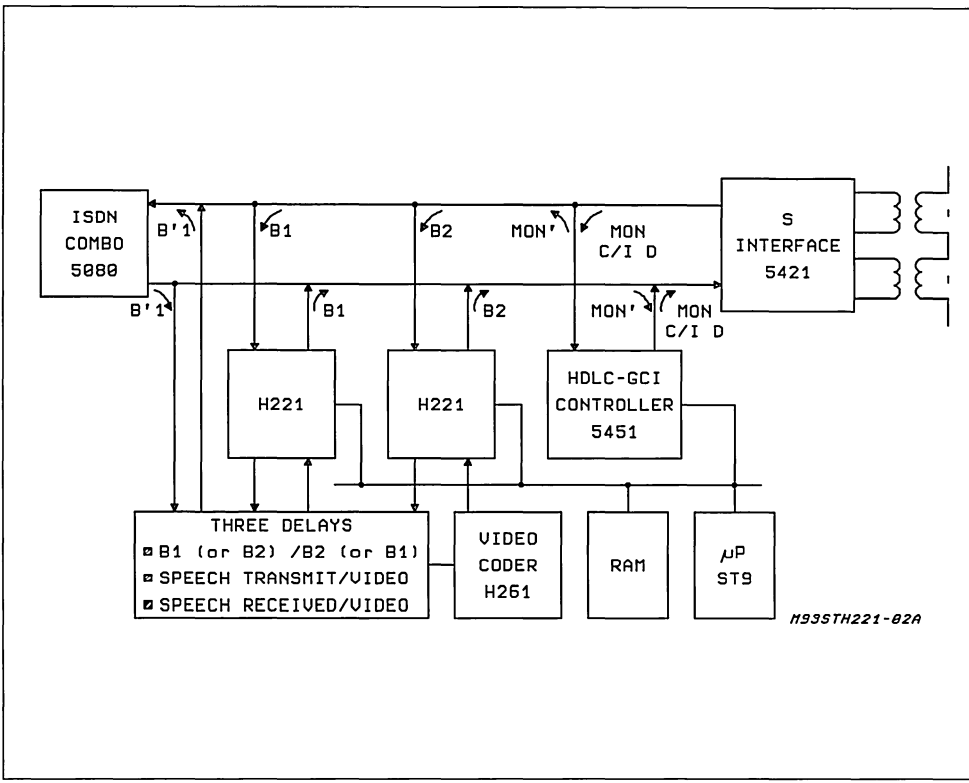


Table 24: Multiframe Structure.

	Submultiframe	Frame	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
MULTIFRAME	0	0	N1							
		1	0							
	1	2	N2							
		3	0							
	2	4	N3							
		5	1							
	3	6	N4	0	0	1	1	0	1	1
		7	0	1	A	E	C1	C2	C3	C4
	4	8	N5							
		9	1							
	5	10	L1							
		11	1							
	6	12	L2							
		13	L3							
	7	14	TEA							
		15	R							

Multiframe Synchronization: Bit 1 of frames 1, 3, 5, 7, 9, 11.
Multiframe number: N1, N2, N3, N4, N5.
Channel number: L1, L2, L3.
Terminal Equipment Alarm TEA, Bit reserved R.

Figure 3: H221 Multiframe.

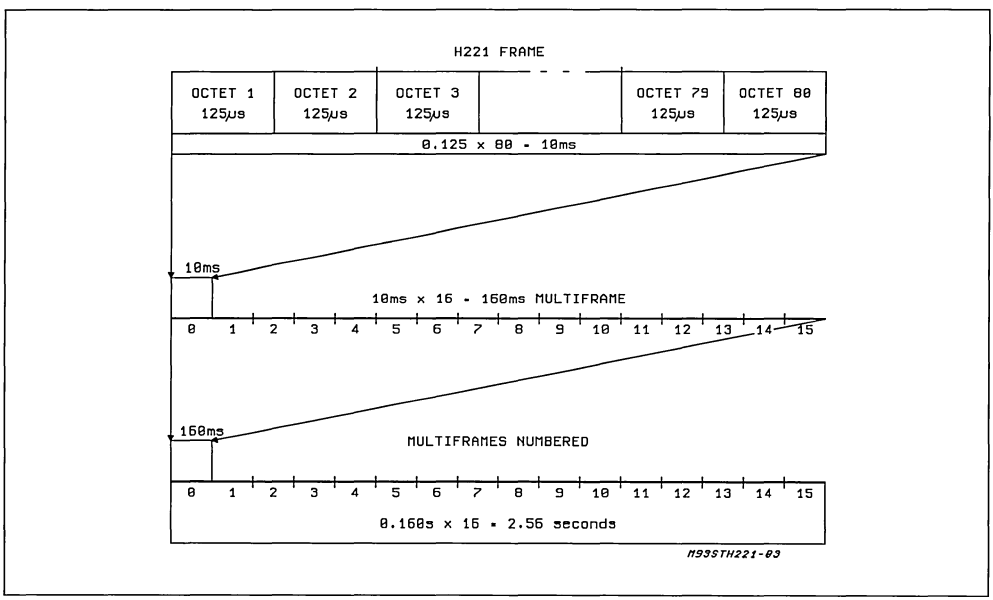
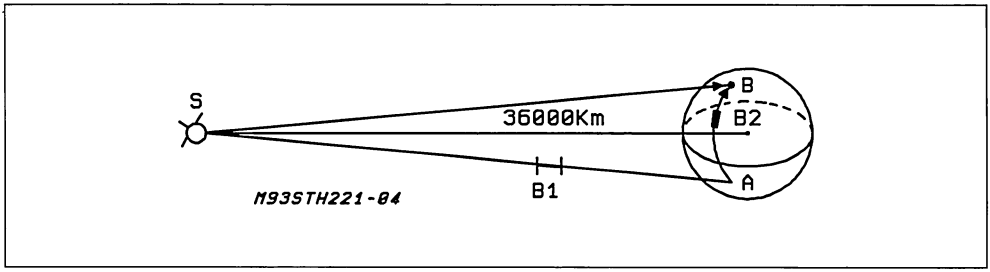


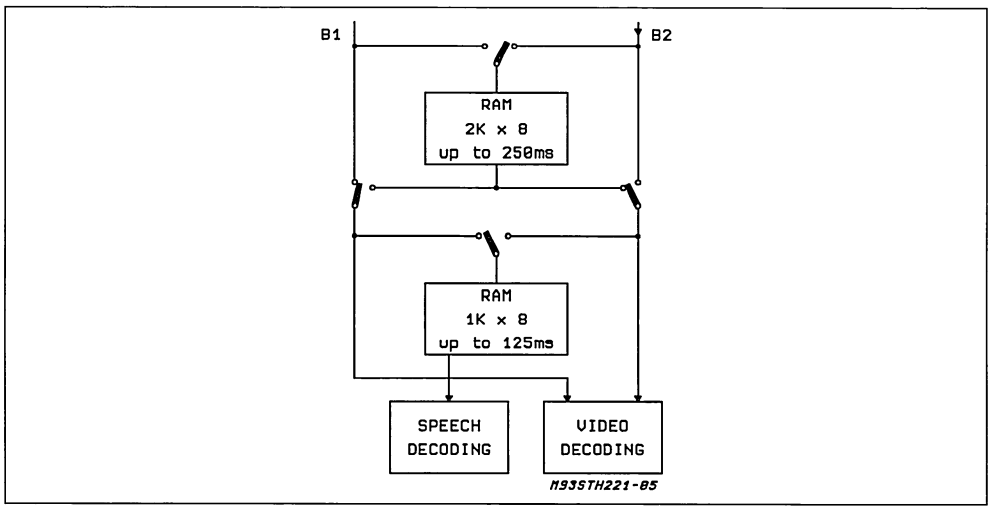
Figure 4: Possible Delays of B1 and B2 Channels.



B1 channel path ASB 300000Km/s Delay $\frac{3600 \cdot 2}{300000} = 0.240s.$

B2 channel path (AB) 5ms/Km (AB) = 6000Km Delay $6000 \cdot 5 = 30000\mu s$
Difference between B1 and B2: 240 - 30ms = 210ms

Figure 5: Terminal Receiving.



Assumptions for videophone terminal.

– The delay of B1 channel is greater than the delay of B2 channel (mp to 250 µs); B2 channel must be delayed.
– Video decoder is slower than the speech decoding up to 100ms.
– B1 is reserved to speech.
– B2 is reserved to video.

Figure 6: Two H.221 Frames Transmetting.

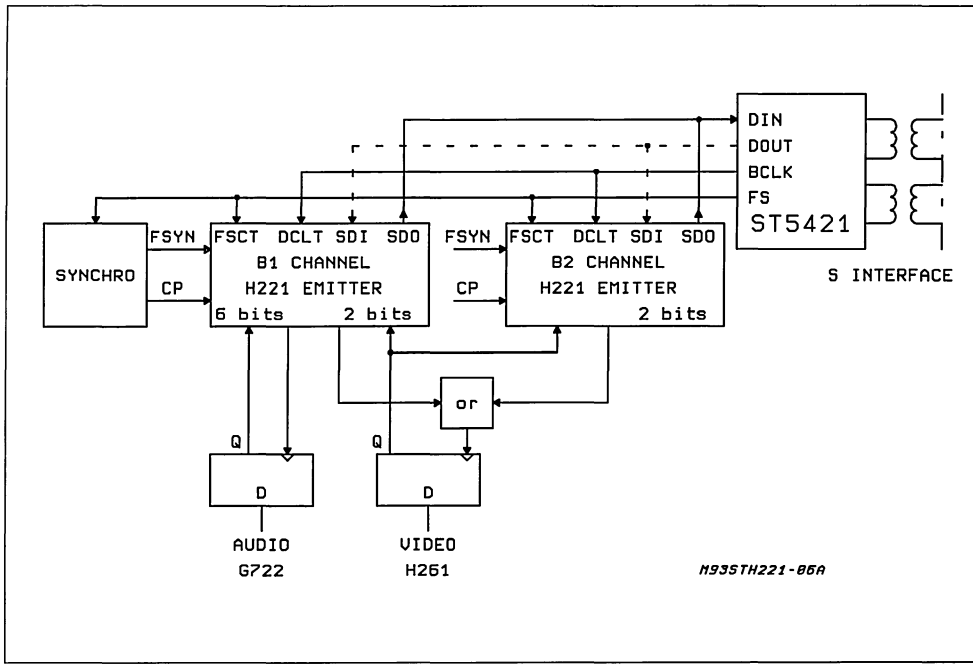


Figure 7: B1 channel is slower than B2 channel.

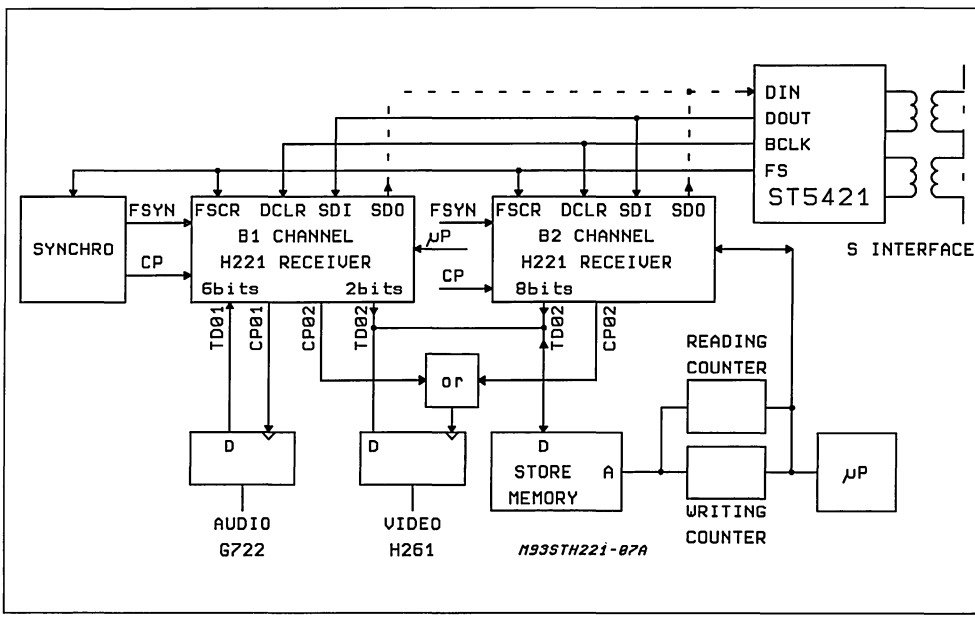


Figure 8: Application Interface Configuration can change every 20ms.

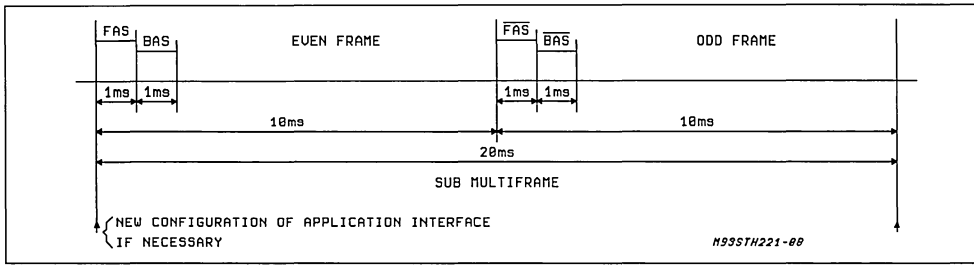


Figure 9: Sub multiframe received.

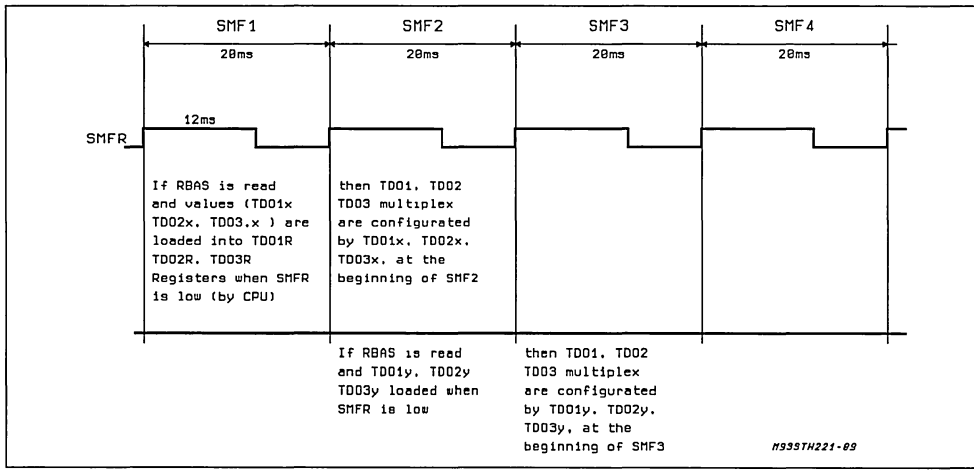


Figure 10: Sub multiframe emitted.

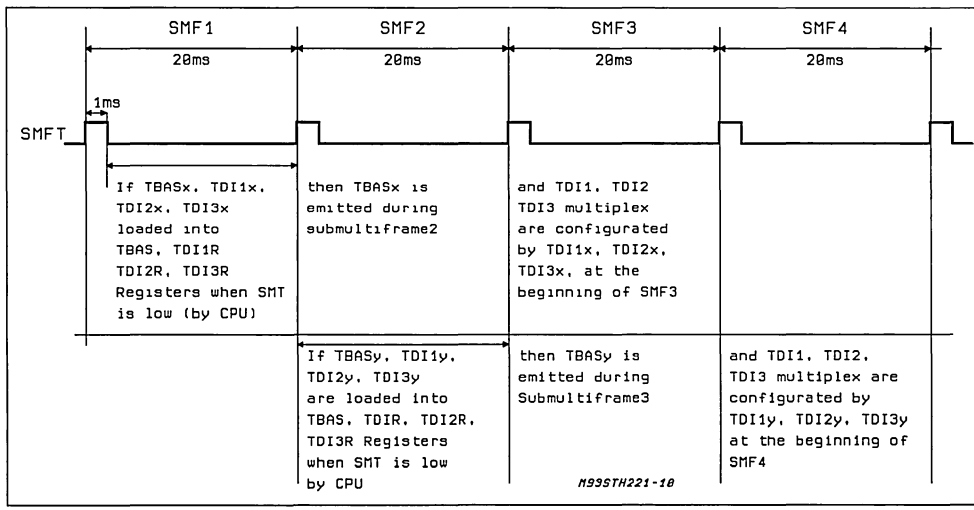


Figure 11: FSYN in comparison with FS when FSYN is different from FS.

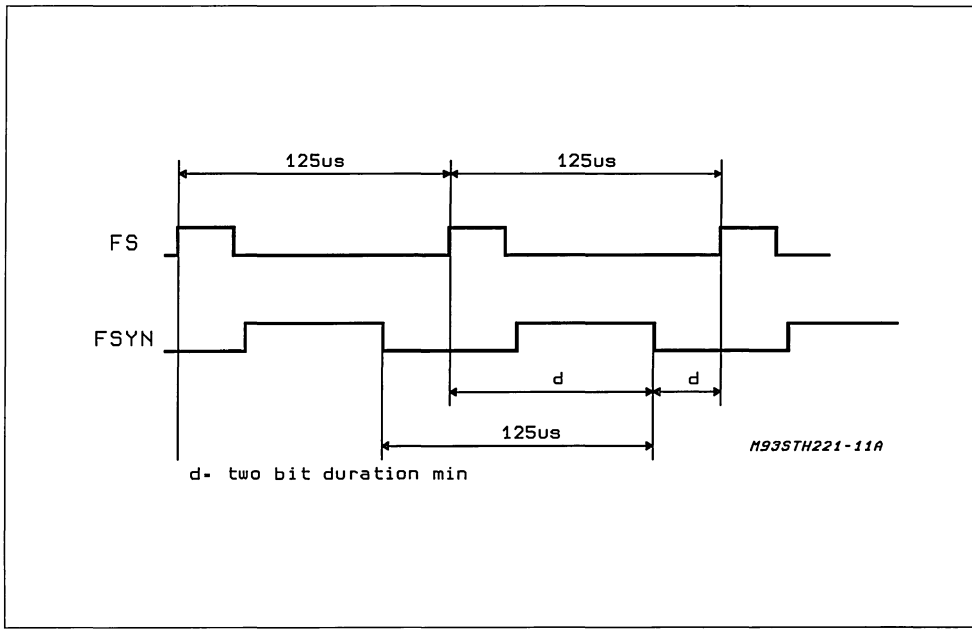
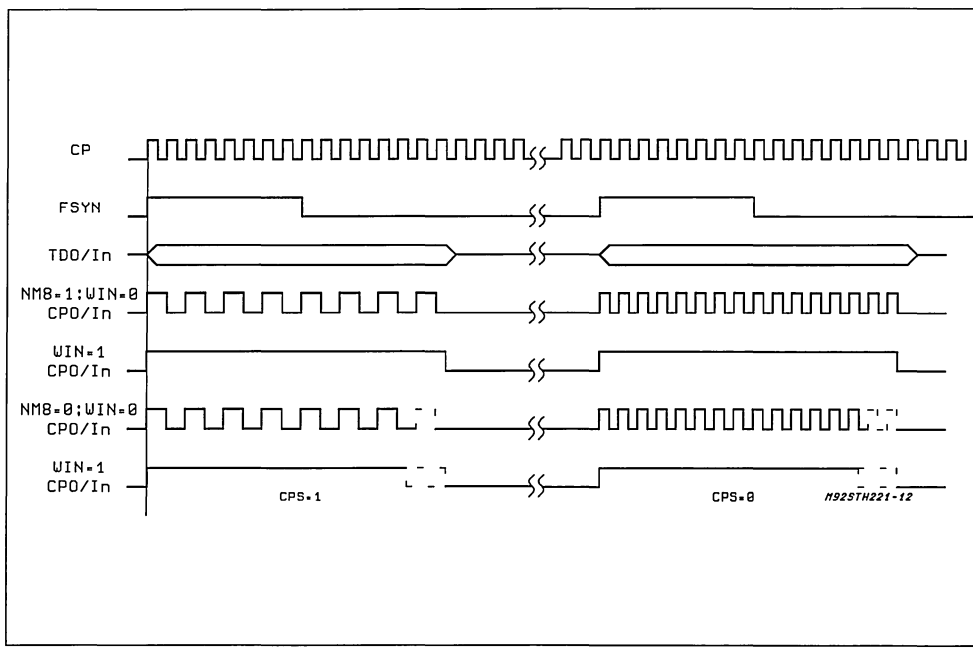


Figure 12: Application Interface.



TIMING CHARACTERISTICS (Preliminary)

Table 25: CPU Read and Write Timing.

Symbol	Description	Min.	Max.	Unit
t_{CTS}	CSN, CDN, RWN, BUS Set-Up Time	40	–	ns
t_{CTH}	CSN, CDN, RWN, BUS Hold Time	10	–	ns
t_{DTS}	DTACKN Valid Offset	–	20	ns
t_{DTH}	DTACKN Release	–	20	ns
t_{DSW}	DSN Width	40	–	ns
t_{DSS}	Data Valid Offset	–	20	ns
t_{DSH}	Data Release	–	20	ns

TIMING DIAGRAMS.

Figure 13: CPU Write Cycle

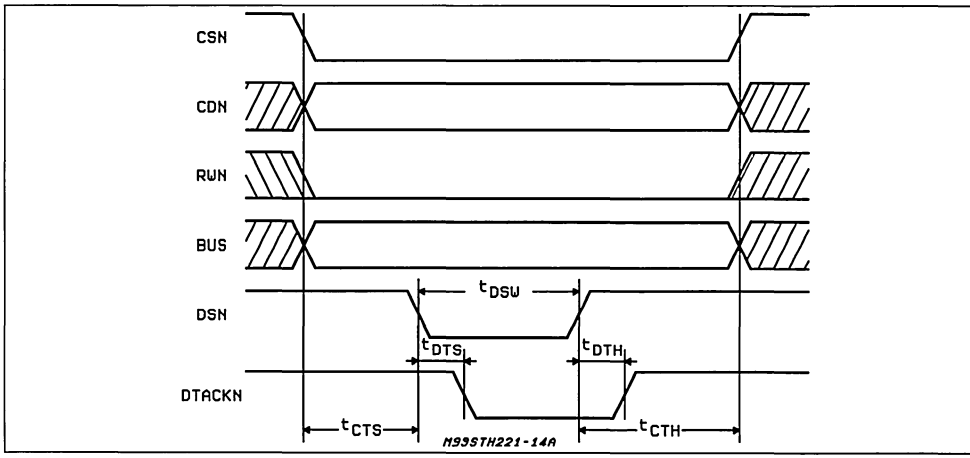


Figure 14: CPU Read Cycle

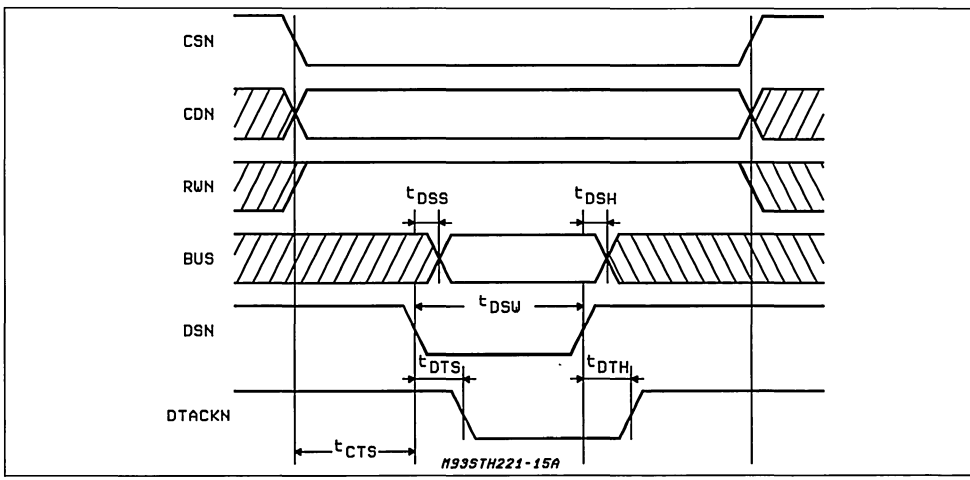


Figure 15: Transmitter Start Timing.

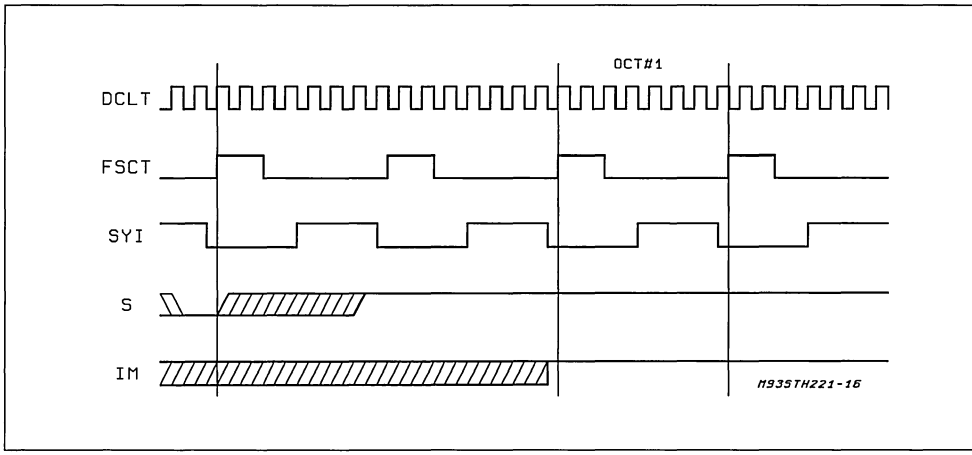


Table 26: Network Side Timing Specifications

Symbol	Test Conditions	Parameters	Min.	Max.	Unit
t_{HCF}	Hold Time DCLR/DCLT Transition to FSCR/FSCT Transition		0		ns
t_{RC}, t_{FC}	Rise and Fall Time: DCLR/DCLT			15	ns
t_{WCH}, t_{WCL}	DCL Width High and Low		60		ns
t_{SFC}	Set up Time FS High to DCL Low		70	DCL –50	ns
t_{DCD}	Delay Time DCL High to Data Valid	Load 150pF		80	ns
t_{DFD}	Delay Time FS High to Data Valid	Load 150pF		80	ns
t_{DCZ}	Delay Time DCL Low Data Invalid			120	ns
t_{SDC}	Set up Time Data Valid to DCL Low		30		ns
t_{HDC}	Hold Time DCL Low to Data Invalid		20		ns

Table 27: Application Side Timing Specifications

Symbol	Test Conditions	Parameters	Min.	Max.	Unit
t_{WCH}, t_{WCL}	CP width High and Low	CP = m · 128kHz 1 ≤ m ≤ 32	60	–	ns
t_{RC}, t_{FC}	Rise and Fall Time CP		–	15	ns
t_{SFC}	Set Up Time FSYN High to CP Low		70	CP –50	ns
t_{DCDa}	Delay Time CP High to Data Valid	Load 150pF	–	70	ns
t_{DFDa}	Delay Time FSYN High to Data Valid	Load 150pF	–	90	ns
t_{DCZ}	Delay Time CP Low to Data Invalid		–	120	ns
t_{SDC}	Set Up Time Data Valid to CP Low		30	–	ns
t_{HDC}	Hold Time CP Low to Data Invalid		20	–	ns

Table 27: Application Side Timing Specifications (continued)

Symbol	Test Conditions	Parameters	Min.	Max.	Unit
t_{DCC}	Delay Time CP High to CPO1/3, CPI1/3 High		–	60	ns
t_{DCW}	Delay Time CP Low to window High and Low		–	80	ns
t_{DFC}	Delay Time FSYN High to CPO 1/3, CPI 1/3 High	First Clock Pulse of First Time Slot	–	80	ns
t_{DFW}	Delay Time FSYN High to window High	First Clock Pulse of First Time Slot	–	80	ns
t_{DDT}	Delay Time DCLT High to SFMT High and Low		–	80	ns
t_{DDR}	Delay Time DCLR High to SFMR High and Low		–	80	ns
t_{DDO}	Delay Time DCLR Low OB, OA, SYO, OM valid	CONF = 0	–	60	ns
t_{DDI}	Delay Time DCLT Low to IB, IA, SYI IM valid	CONF = 0	–	60	ns
t_{SDC}	Set Up Time Data Valid to CPI Low	CONF = 0	30	–	ns
t_{HDC}	Hold Time CPI Low to Data Invalid	CONF = 0	20	–	ns

Figure 16: Network Side Signals.

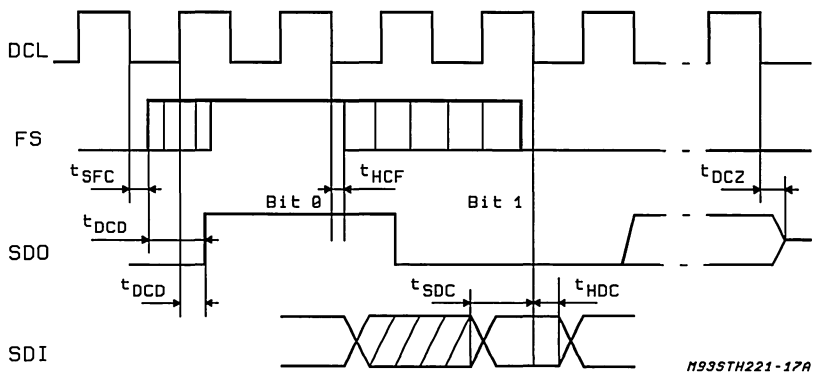
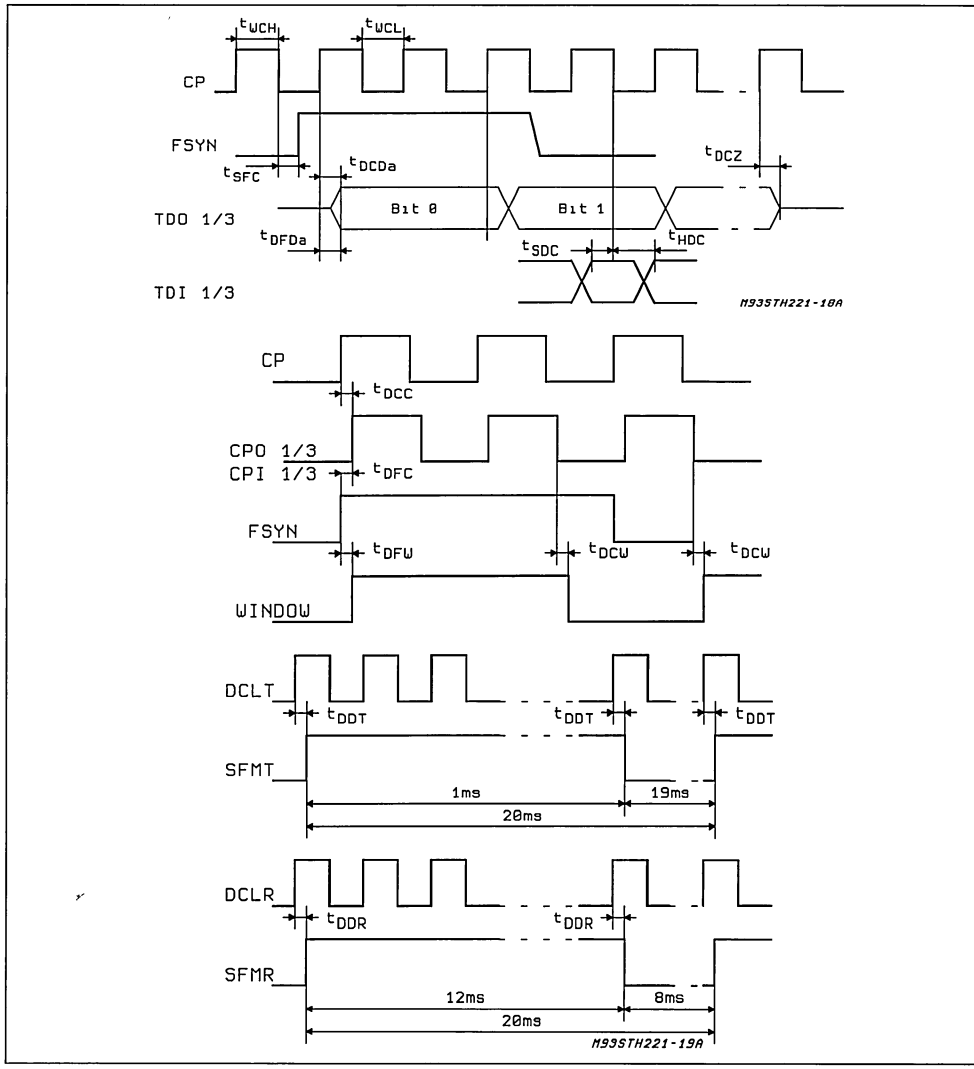
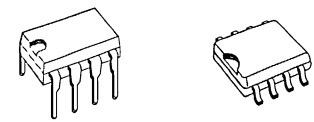


Figure 17: Application Side Signals.



1W AUDIO AMPLIFIER WITH MUTE

- OPERATING VOLTAGE 1.8 TO 15V
- EXTERNAL MUTE OR POWER DOWN FUNCTION
- IMPROVED SUPPLY VOLTAGE REJECTION
- LOW QUIESCENT CURRENT
- HIGH POWER CAPABILITY
- LOW CROSSOVER DISTORTION



Minidip **SO8**

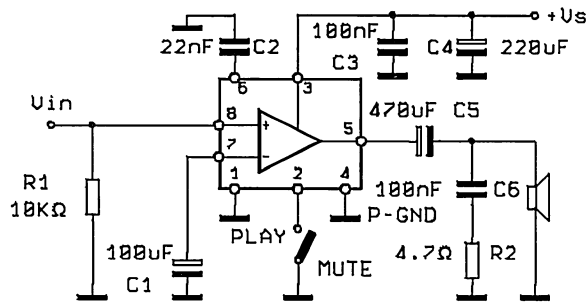
ORDERING NUMBERS:

TDA7233 TDA7233D

DESCRIPTION

The TDA7233/D is a monolithic integrated circuit in 8 pin Minidip or SO8 package, intended for use as class AB power amplifier with a wide range of supply voltage from 1.8V to 15V in portable players, cordless telephones and Cellular Radios.

TEST AND APPLICATION CIRCUIT



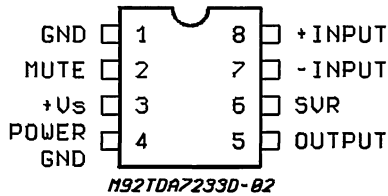
M92TDA7233D-01

Note: Switch Open = Mute
Switch Closed = Play

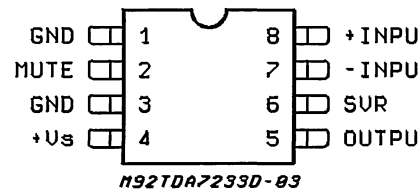
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	16	V
I_O	Output Peak Current	1	A
P_{tot}	Total Power Dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and Junction Temperature	–40 to 150	°C

PIN CONNECTIONS (Top views)



Minidip



SO8

THERMAL DATA

Symbol	Parameter		SO8	Minidip	Unit
Rth j-amb	Thermal Resistance Junction-ambient	max.	200	100	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 6 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		1.8		15	V
V_o	Quiescent Out Voltage			2.7		V
		V_S = 3 V V_S = 9 V		1.2 4.2		V V
I_d	Quiescent Drain Current	MUTE HIGH		3.6	9	mA
		MUTE LOW		0.4		
I_b	Input Bias Current			100		nA
P_o	Output Power	d = 10 % f = 1 KHz V_S = 12 V R_L = 8 Ω V_S = 9 V R_L = 4 Ω V_S = 9 V R_L = 8 Ω V_S = 6 V R_L = 8 Ω V_S = 6 V R_L = 4 Ω V_S = 3 V R_L = 4 Ω V_S = 3 V R_L = 8 Ω		 1.9 1.6 1 0.4 0.7 110 70		 W W W W W mW mW
d	Distortion	P_o = 0.5 W f = 1 kHz R_L = 8 Ω V_S = 9 V		0.3		%
G_v	Closed Loop Voltage Gain	f = 1 kHz		39		dB
R_{IN}	Input Resistance	f = 1 kHz	100			KΩ
e_N	Total Input Noise (R_S = 10 kΩ)	B = Curve A		2		μV
		B = 22 Hz to 22 kHz		3		
SVR	Supply Voltage Rejection	f = 100 Hz, R_g = 10 KΩ		45		dB
	MUTE Attenuation	V_o = 1 V f = 100 Hz to 10 kHz		70		dB
	MUTE Threshold			0.6		V
I_M	MUTE Current			0.4		mA

Figure 1: Output Power vs. Supply Voltage

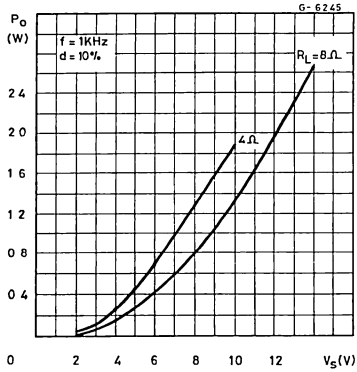


Figure 2: Supply Voltage Rejection vs. Frequency

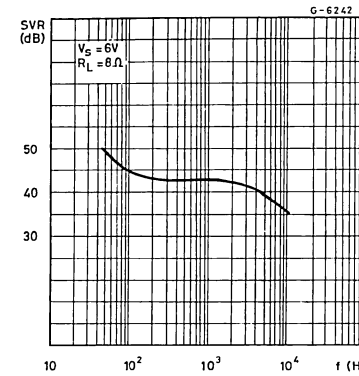


Figure 3: DC Output Voltage vs. Supply Voltage

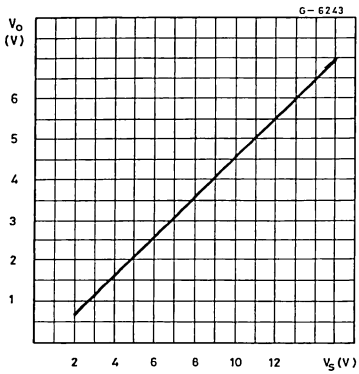


Figure 4: Quiescent Current vs. Supply Voltage

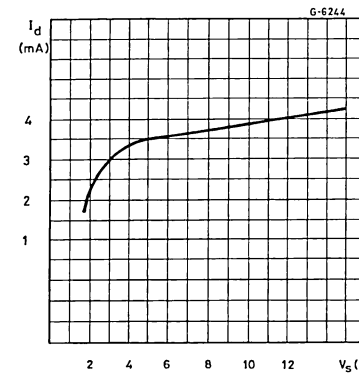
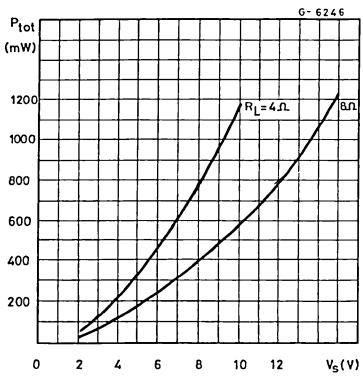


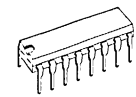
Figure 5: Total Dissipated Power vs. Supply Voltage



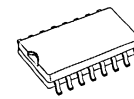
AM-FM RADIO FREQUENCY SYNTHESIZER

ADVANCE DATA

- FM INPUT AND PRECOUNTER FOR UP TO 140MHz
- AM INPUT FOR UP TO 40MHz
- 6-BIT SWALLOW COUNTER, 8-BIT PROGRAMMABLE COUNTER FOR FM AND SW
- 14-BIT PROGRAMMABLE COUNTER FOR LW AND MW
- ASYNCHRONOUS 8-BIT SERIAL INTERFACE
- ON-CHIP REFERENCE OSCILLATOR AND COUNTER
- PROGRAMMABLE SCANNING STEPS FOR AM AND FM
- DIGITAL PHASE DETECTOR AND LOOP FILTER
- TWO SEPARATE FREE PROGRAMMABLE FILTER APPLICATIONS AVAILABLE
- TUNING VOLTAGE OUTPUT 0.5 TO 9.5V
- PROGRAMMABLE CURRENT SOURCES TO SET THE LOOP GAIN
- ON-CHIP POWER ON RESET
- STANDBY MODE



DIP 16



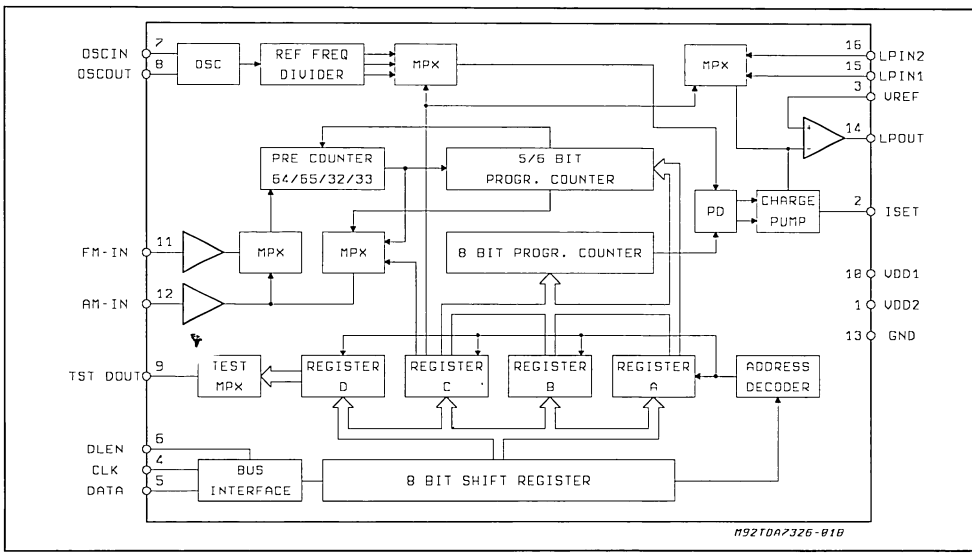
SO16L

ORDERING NUMBER: TDA7326 (DIP 16)
TDA7326D (SO16L)

DESCRIPTION

The TDA7326 is a PLL frequency synthesizer in CMOS technology that performs all the function of a PLL radio tuning system for FM and AM (LW, MW, SW)

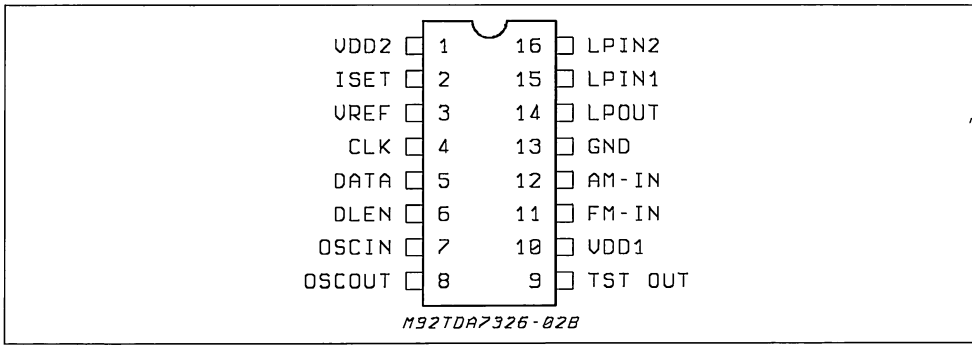
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD1} - V_{SS}	Supply Voltage	- 0.3 to + 7	V
V_{DD2} - V_{SS}	Supply Voltage	- 0.3 to + 12	V
V_{IN}	Input Voltage	VSS - 0.3 to V_{DD} + 0.3	V
V_{OUT}	Output Voltage	VSS - 0.3 to V_{DD} + 0.3	V
I_{IN}	Input Current	- 10 to + 10	mA
I_{OUT}	Output Current	- 10 to + 10	mA
T_{stg}	Storage Temperature	- 55 to + 125	°C
T_A	Ambient Temperature	-20 to + 85	°C

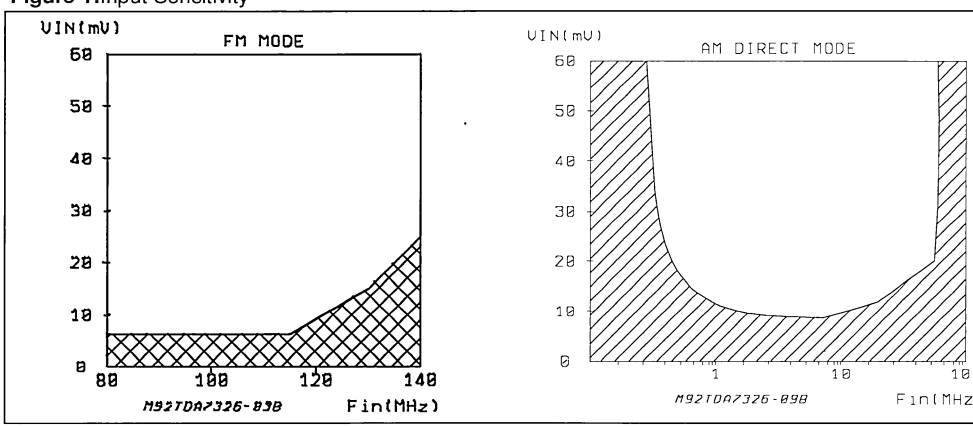
PIN CONNECTION



THERMAL DATA

Symbol	Parameter	DIP 16	SO 16L	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	100	200	

Figure 1: Input Sensitivity



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C ; V_{DD1} - V_{SS} = 5V; V_{DD2} - V_{SS} = 9V f_{OSC} = 4MHz; R_{ISET} = 68KΩ; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD1}	Supply Voltage		4.5	5.0	5.5	V
V_{DD2}	Supply Voltage			9.0	10.0	V
$I_{DD1\ FM}$	Supply Current	no output load, FM mode, f_{in} = 100MHz		15	20	mA
$I_{DD1\ AM}$	Supply Current	no output load, AM mode, fin = 1MHz		6	10	mA
$I_{DD1\ STB}$	Supply Current	Standby mode			20	µA
I_{DD2}	Supply Current			2	3	mA
V_{REF}	Voltage at pin 3			3.5		V
V_{ISET}	Voltage at pin 2	RiSET = 68KΩ		8.0		V

RF INPUT (AMIN FMIN)

f_{IMIN}	Min Input Frequency AM	Direct Mode			0.5	MHz
		Swallow Mode			16	MHz
f_{IMAX}	Max Input Frequency AM	Direct Mode	20			MHz
		Swallow Mode	40			MHz
f_{IMIN}	Min Input Frequency FM	Sinus			30	MHz
f_{IMAX}	Max Input Frequency FM	Sinus	140			MHz
V_{IMIN}	Min Input Voltage AM	Direct Mode 0.6 to 16MHz (Sinus)			40	mV/rms
		Swallow Mode 16 to 40MHz (Sinus)			40	mV/rms
V_{IMAX}	Max Input Voltage AM	0.6 to 40MHz (Sinus)	600			mV/rms
V_{IMIN}	Min Input Voltage FM	70 to 120MHz (Sinus)			30	mV/rms
V_{IMAX}	Max Input Voltage FM	70 to 120MHz (Sinus)	600			mV/rms
Z_{in}	Input Impedance FM	fin = 120MHz		200		Ω
Z_{in}	Input Impedance AM	fin = 12MHz		1400		Ω

OSCILLATOR

f_{OSC}	Oscillator Frequency			4		MHz
t_{bu}	Built Up Time	Euro-Quartz ITT			100	ms
C_{in}	Internal Capacitance			9		pF
C_{OUT}	Internal Capacitance			9		pF
Z_{in}	Input Impedance			4	15	KΩ
V_{in}	Input Voltage				VDD1	mVpp

PLL CHARACTERISTICS

f_{step}	Step Width AM			1/2.5		KHz
f_{step}	Step Width FM			1.25/25		KHz
f_{ref}	Ref Frequency AM			1/2.5		KHz
f_{ref}	Ref Frequency FM			12.5/25		KHz

LOOP FILTER INPUT (LP_{IN1}, LP_{IN2} = PIN 15,16)

$-I_{in}$	Input Leakage Current	VIN = V_{SS}; Phase Detector Output = Tristate		-0.1		µA
I_{in}	Input Leakage Current	VIN = V_{DD}; Phase Detector Output = Tristate		0.1		µA

ELECTRICAL CHARACTERISTICS (continued)

LOOP FILTER OUTPUT (LP_{OUT} = PIN 14)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OL}	Output Voltage Low	ILOAD = 0.2mA V_{DD2}; = 10V			0.6	V
V_{OH}	Output Voltage High	-ILOAD = 0.2mA V_{DD2}; = 10V	9			V

CHARGE PUMP CURRENT GENERATION (LP_{IN1}, LP_{IN2} = PIN 15, 16)

I_{SI}	Sink Current LPIN1,2	CURR1 = 0, CURR2 = 0		5		µA
		CURR1 = 0, CURR2 = 1		200		µA
		CURR1 = 1, CURR2 = 1		300		µA
		CURR1 = 1, CURR2 = 0		500		µA
$-I_{SO}$	Source Current LPIN1,2	CURR1 = 0, CURR2 = 0		5		µA
		CURR1 = 0, CURR2 = 1		200		µA
		CURR1 = 1, CURR2 = 1		300		µA
		CURR1 = 1, CURR2 = 0		500		µA

DOUT1 OPENDRAIN OUTPUT(PIN 9)

V_{OL}	Output Voltage Low	ILOAD = 1mA			0.5	V

BUS INTERFACE

$-I_{IL}$	Input Leakage Current	VIN = Vss	-1		1	µA
I_{IH}	Input Leakage Current	VIN = Vss	-1		1	µA
V_{IH}	Input Voltage High	Leading edge	3.4			V
V_{IL}	Input Voltage Low	Leading edge			1.6	V

BUS INTERFACE, WAITING TIME (see fig. 5)

t_1	DLEN to CLK		0.2			µs
t_3	CLK to DATA		0.1			µs
t_5	CLK to DATA		0.4			µs

BUS INTERFACE, DATA REPETITION TIME (see fig. 5)

t_{r1}	Release Time Between 2 bytes, exept byte 4		5			µs
t_{r2}	Release Time after the transmission of byte 4	FM mode	180			µs
		AM mode	2			ms

BUS INTERFACE, SETUP TIME (see fig. 5)

t_2	DLEN to CLK		1			µs

BUS INTERFACE, HOLD TIME (see fig. 5)

t_4	DATA to CKL		0			µs
t_6	DLEN to CLK		0.4			µs
f_{CLK}	CLK Frequency				500	KHz
	Duty Cycle			50		%
t_{pl}		see fig. 5	1			µs
t_{ph}		see fig. 5	1			µs

2.0 GENERAL DESCRIPTION

This circuit contains a frequency synthesizer and a loop filter for an FM and AM radio tuning system. Only a V_{CO} is required to build a complete PLL system.
A small signal of the AM and FM V_{CO} can be accepted by the circuit.
For FM and SW application, the counter works in a two stages configuration.
The first stage is a swallow counter with a four modulus (:32/33/64/65) precounter.
The second stage is an 8-bit programmable counter.
For LW and MW application, a 14-bit programmable counter is available.
The circuit receives the scalling factors for the programmable counters and the values of the reference frequencies via a three line serial bus interface.
The reference frequency is generated by a 4MHz XTAL oscillator followed by the reference divider.
An external oscillator (f = 4MHz) can be used instead of the internal one; it must be connected to OSCIN (pin 7)
The reference- and step-frequency is 1 or 2.5kHz for AM.
For FM mode a step frequency of 12.5 and 25kHz can be selected.
The circuit checks the format of the received data words.
Valid data in the interface shift register are stored automatically in buffer registers at the end of transmission.
The output signals of the phase detector are switching the programmable current sources.
Their currents are integrated in the loop filter to a DC voltage.The values of the current sources are programmable by two bits also received via the serial bus.
The loop filter amplifier is supplied by a separate positive power supply, to minimize the noise in reduced by the digital part of the system.
The loop gain can be set for different conditions.
After a power on reset, all registers are reset to zero and the standby mode is activated.
In standby mode, oscillator, reference counter, AM input and FM input are stopped. The power consumption is reduced to a minimum.

3.0 DETAILED DESCRIPTION OF THE PLL FREQUENCY SYNTHESIZER

3.1 INPUT AMPLIFIERS

The signals applied on AM and FM input are amplified to get a logic level in order to drive the frequency dividers.

3.1.1 Input Impedance

The typical input impedance: for the FM input is 200Ω and for AM input is 1.4kΩ.

3.1.2 Input sensitivity

(see Figures 1a and 1b).

3.2 DATA AND CONTROL REGISTER

3.2.1 Register Location

The data registers (bit2...bit7) for the control register and the data registers PC0...PC7, SW0...SW5 for the counters are organized in four words, identified by two address bits (bit0 and bit1), bit0 is the first bit to be send by the controller, bit7 is the last one. The order and the number of the bytes to be transmitted is free of choice. The modification of the PC0...PC7 registers is valid for the internal counters only after transmission of bite4 (SC0...SC5).
Standby mode is activated during the registers AM/FM and SWM/DIR are set to zero.

3.3 DIVIDER FROM V_{CO} FREQUENCY TO REFERENCE FREQUENCY

	ADDRESS BITS		DATA BITS					
BYTE	**MSB-BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**LSB BIT 0**
Function	adr 0	adr 1	data 0	data 1	data 2	data 3	data 4	data 5
byte 1	0	0	test 0	test 1	test 2	SOUT	CURR2	f_{REF}
byte 2	0	1	PC7	PC6	LPF1/2	CURR 1	SWM/DIR	AM/FM
byte 3	1	0	PC5	PC4	PC3	PC2	PC1	PC0
byte 4	1	1	SC5	SC4	SC3	SC2	SC1	SC0

3.2.2 CONTROL AND STATUS REGISTERS

REGISTER NAME	FUNCTION
SWM/DIR	Swallow direct-mode switch 1 = SWM, 0 = DIR
AM/FM	AM - FM band switch 1=AM, 0 = FM
f_{REF}	Selection of reference frequency (see table 3.4)
CURR1	Current select of change pump
CURR2	Current select of change pump
LPF1/LPF2	Loop filter input select 1= I_{PF1}, 0 = I_{PF2}
SOUT	Switch output condition 1=output high, 0 = output low

This divider provides a low frequency f_{SYN} which is phase compared with the reference frequency f_{REF}.

3.4 OPERATING MODE

Four operating modes are available:
- FM mode,
- AM swallow mode,
- AM direct mode,
- Standby mode

They are user programmable with the SWR/DIR and AM/FM registers.
Standby mode: all functions are stopped. This allows low current consumption without lost of information in all register

3.4.1 FM and AM (SW) Operation (Swallow Mode)

The FM or AM signal is applied to a four modulus: 32/33/64/65 high speed prescaler, which is controlled by a 6 bit divider 'A'.This divider is controlled by the 6 bit SC register. In parallel the output of the prescaler is connected to a 8 bit divider 'B'. This divider is controlled by the 8 bit PC register. For FM mode with 25kHz reference frequency operation, the divider A is a 5 bit divider. The high speed prescaler is working in : 32/33 dividing mode. Bit 6 of the SC register has to kept to "0".
Dividing range calculation :
For FM mode with 12.5kHz reference frequency and SW swallow mode operation :
$f_{VCO} = [\,65 \cdot A_1 + (B_1 + 1 - A_1) \cdot 64\,] \cdot f_{REF}$ or
$f_{VCO} = (64 \cdot B_1 + A_1 + 64) \cdot f_{REF}$
Important : For correct operation $B \geq 64$ and $B \geq A$.
At FM mode with 25kHz reference frequency :
$f_{VCO} = [\,33 \cdot A_2 + (B_2 + 1 - A_2) \cdot 32\,] \cdot f_{REF}$
$f_{VCO} = (32 \cdot B_2 + A_2 + 32) \cdot f_{REF}$
Important: For correct operation $B \geq 32$ and $B \geq A$.
A and B are variable values of the dividers.
To keep the actual tuning frequency after a modification of the reference frequency, the values of the dividers have to be modified in the following way.
Switching from 25kHz to 12.5kHz reference frequency : $B_1 = B_2$, $A_1 = A_2 \cdot 2$
Switching from 12.5kHz to 25kHz reference frequency:

$$B_2 = B_1,\ A_2 = \frac{A_1}{2} \text{ and } A_2 = \frac{(A_1 + 1)}{2}$$

for odd values A_1.

Figure 2: FM and AM (SW) operation (swallow mode)

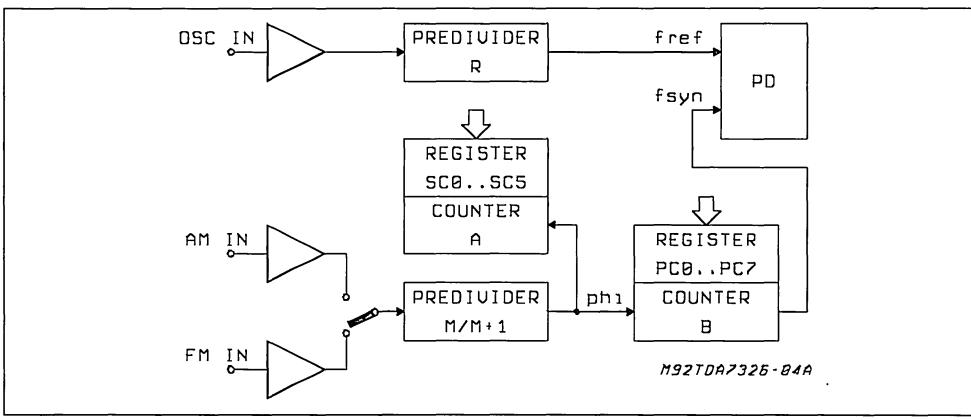
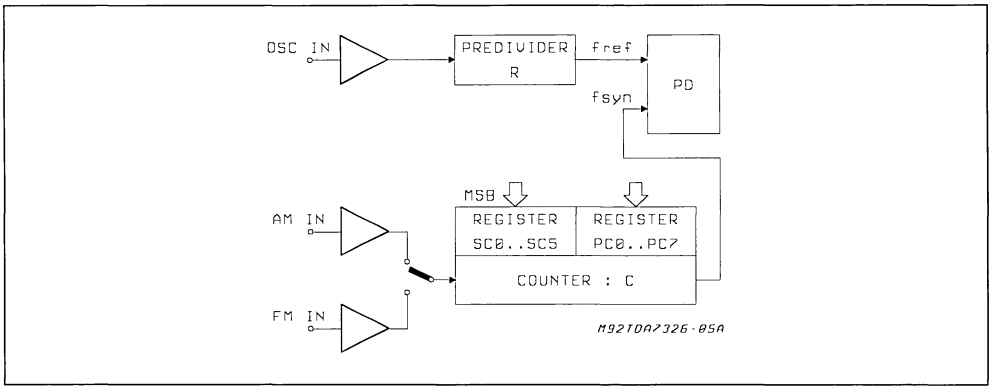


Figure 3: AM direct mode operation for SW, MW and LW



The AM signal is directly applied to the 14 bit static divider 'C'. This divider is controlled by both SC and PC registers.
Dividing range: $f_{VCO} = (C + 1) \cdot f_{REF}$

3.4 REFERENCE FREQUENCY GENERATOR

The crystal oscillator clock is divided by the reference frequency divider to provide the reference frequency to the phase comparator. Reference frequency divider range is selectable by the programming bit 'f_{REF}'.
Available reference frequency are shown in

TABLE 3.4

AM/FM	f_{REF}	f_{REF} (kHz)
0	0	12.5
0	1	25
1	0	1
1	1	2.5

Figure 4: Phase comparator

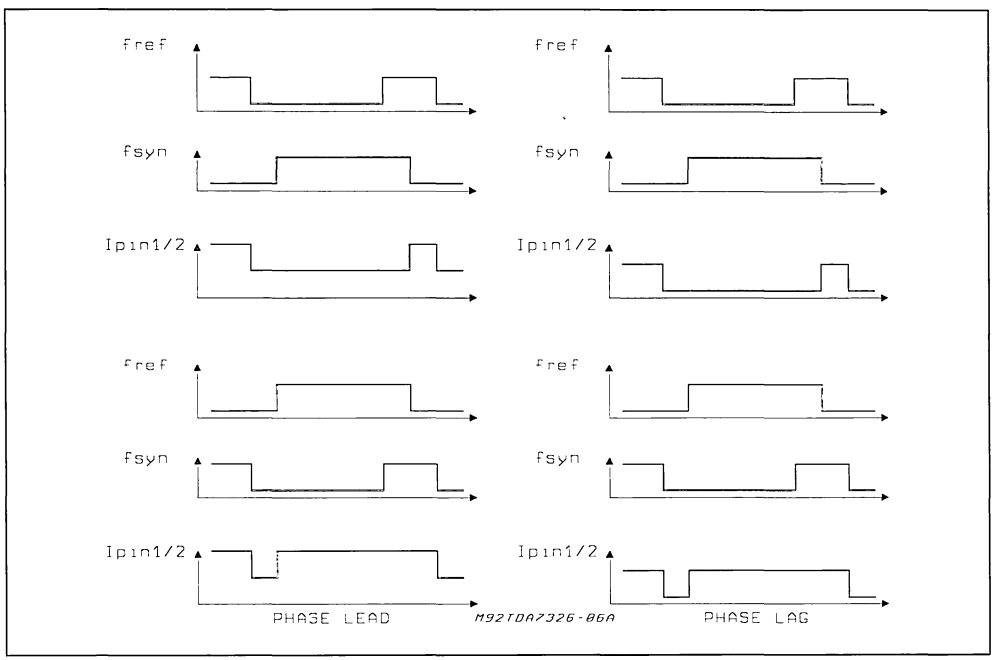
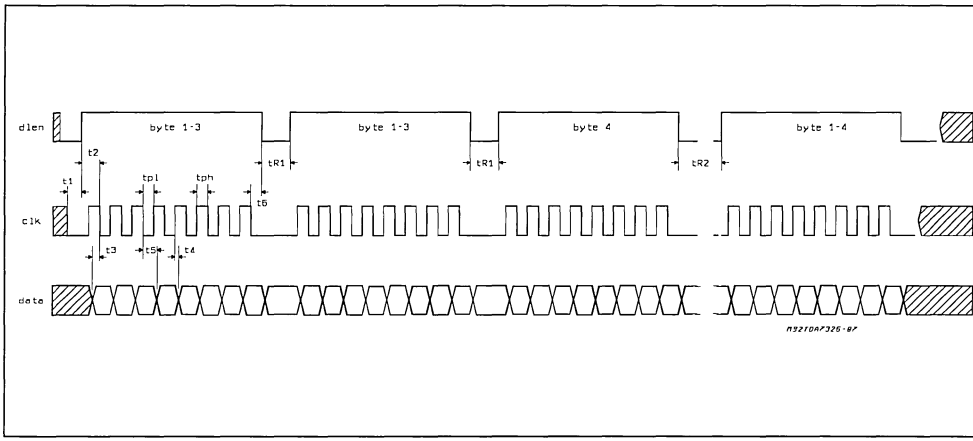


Figure 5



following table.

3.5 THREE STATE PHASE COMPARATOR

The phase comparator generates a phase error signal according to phase difference between f_{SYN} and f_{REF}. This phase error signal drives the charge pump current generator

3.6 CHARGE PUMP CURRENT GENERATOR

This system generates signed pulses of current. Duration and polarity of those pulses are determined by the phase error signal. The absolute current values are programmable by 'CURR1' and 'CURR2' register and controlled by an external resistor R_{ISET} connected to Pin 2 and GND.

3.7 LOW NOISE CMOS OP-AMP

A low noise Op-Amp is available on chip. The positive input of this Op-Amp is connected to an internal voltage divider and to Pin 3 'V_{REF}'. The negative input is connected to the charge pump output.

In cooperation with this internal amplifier and external components, a active filter can be provided. To increase the flexibility in application the negative input can be switched to two input pins (Pins 15 and 16). This switch is controlled by 'LPF' register with 'LPF' low Pin 15 is active and 'LPF' high Pin 16 is active. This feature allows two separate active filters with different performance.

Test Register Status			Test Function	
test 0	test 1	test 2	PIN9 (TEST/OUT)	PIN 7 (OSCIN)
0	0	0	S_{out} (appl. mode)	O_{scin} (appl. mode)
1	0	0	f_{ref} Output	O_{scin} (appl. mode)
0	1	0	P_{hi} Output	f_{ref} Input
1	1	0	f_{syn} Output	fref Input
0	0	1	P_{hi} input	O_{scin} (appl. mode)

3.8 SWITCH OUTPUT AND TEST FUNCTION

3.9 C-BUS INTERFACE

This interface allows communication between the PLL device and µp systems. A bus control system check the format of transmission, only eight bit word transmission is allowed. Four registers with 6 bit are user programmable. The selection of this four registers is controlled by two address bits.

4.0 BIT ORGANIZATION OF THE BUS TRANSFER OPERATION

Loading registers for all bytes of the programmable counters and all control registers

0	1	PC7	PC6	LPF1/ LPF2	CURR1	SWM DIR	AM FM	1	0	PC5	PC4	PC3	PC2	PC1	PCO	⇒

⇒	1	1	SC5 (0)*	SC4	SC3	SC2	SC1	SC0	0	0	0	0	0	S_{OUT}	CURR2	f_{ref}

Loading registers for all bytes of the programmable counters and all control registers

0	1	PC7	PC6	LPF2/ LPF1	CURR1	SWM DIR	AM FM	1	0	PC5	PC4	PC3	PC2	PC1	PCO	⇒

⇒	1	1	SC5 (0)*	SC4	SC3	SC2	SC1	SC0

Loading registers for 11 or 12 bits of the programmable counters

1	0	PC5	PC4	PC3	PC2	PC1	PC0	1	1	SC5 (0)*	SC4	SC3	SC2	SC1	SC0

Loading registers for 5 or 6 bits of the programmable counters

1	1	SC5 (0)*	SC4	SC3	SC2	SC1	SC0

Setting control register for loop filter select charge pump current mode select

0	1	X	X	LPF2/ LPF1	CURR1	SWM/ DIR	AM FM

Setting control register for switch output pin 9, charge pump current bit 2, reference frequency select

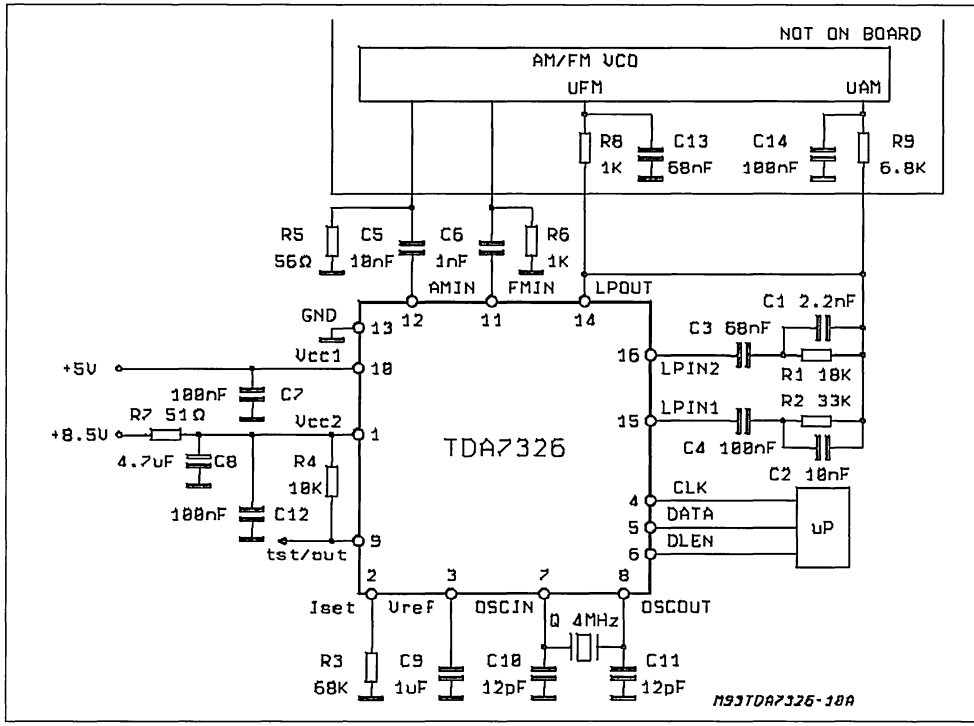
0	0	0	0	0	S_{OUT}	CURR2	f_{REF}

Test mode inizialization

0	0	TST0	TST1	TST2	S_{OUT}	CURR2	f_{REF}

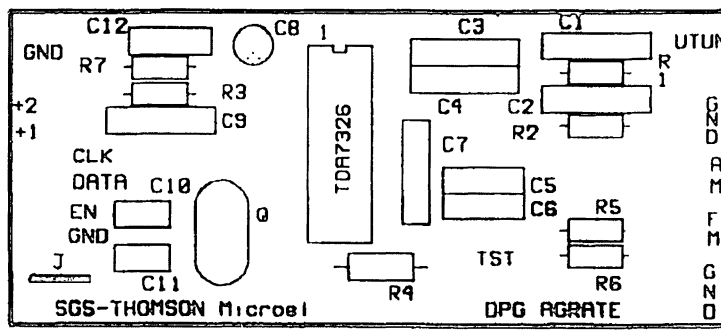
(*) This bit has to be "0" for f_{REF} = "1" (f_{REF} = 25kHz in FM mode)

Figure 5: Application with two loop-filters



*) C7 must be connected as closed as possible between pin 10 and pin 13

Figure 6: PC Board and Component Layout of fig. 5



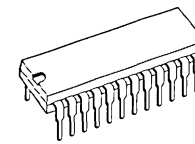
SGS-THOMSON MICROELECTRONICS

TEA7052

SPEECH CIRCUIT WITH POWER MANAGEMENT

ADVANCE DATA

- 2/4 WIRES INTERFACE WITH
  - Double antisidetone network
  - Rx gain and AC impedance externally programmable
- DTMF INTERFACE
- PULSE DIAL INTERFACE
- 4.0 VOLTS SUPPLY FOR MICROPROCESSOR OR DIALER
- RESET TO MICROPROCESSOR
- CURRENT SUPPLY FOR LOUDSPEAKER
- HANDS-FREE INTERFACE
- DC CHARACTERISTIC AND ON/OFF HOOK FOR FRANCE
- CONTROL AGAINST HIGH VOLTAGE TRANSIENTS



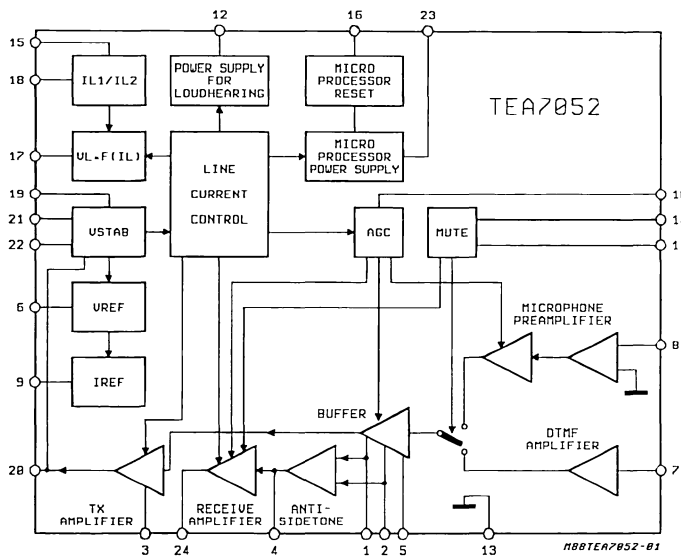
DIP24

ORDERING NUMBER : TEA7052DP

DESCRIPTION

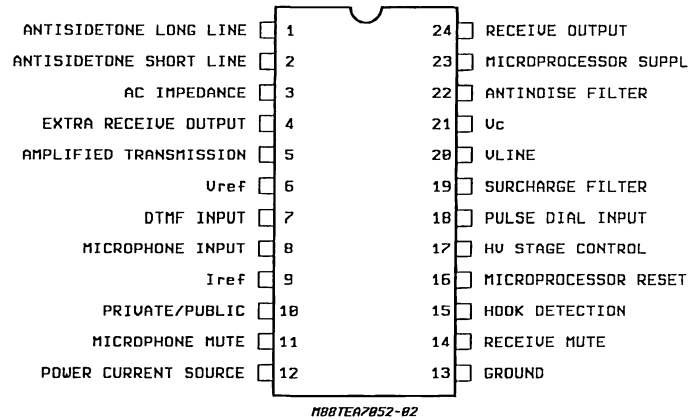
The TEA7052 is expressely designed to meet the french specification for telephone set in medium and high range equipments.

BLOCK DIAGRAM



PIN CONNECTIONS (top view)

DIP24



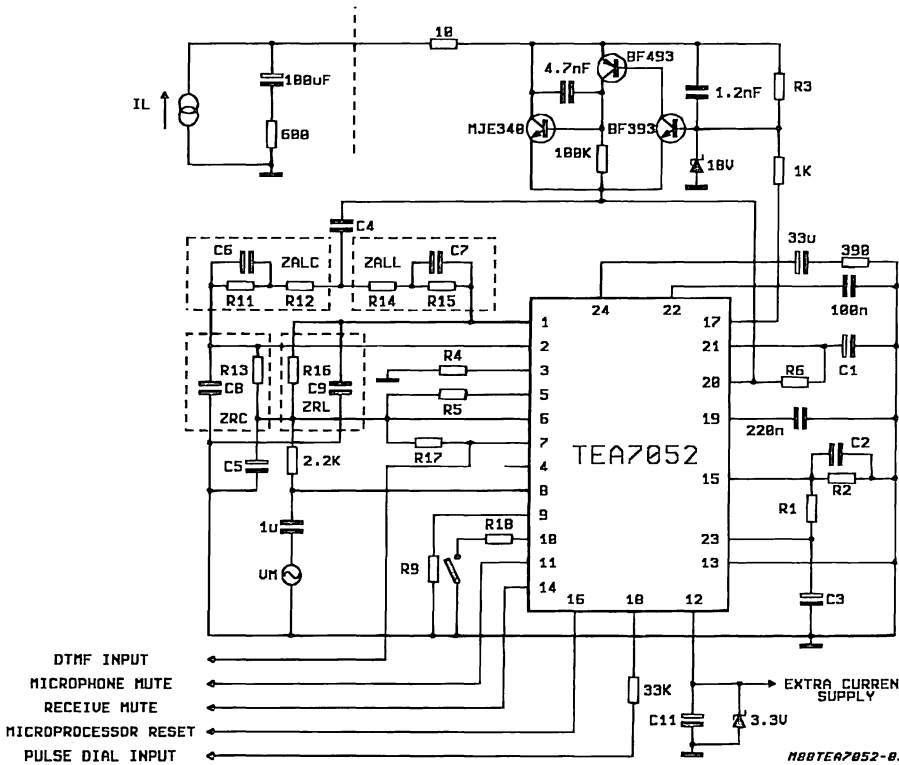
ELECTRICAL CHARACTERISTICS ($T_a = 25^oC$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
V_C	Stabilized Voltage (pin 21)	I_L = 27mA	2.35	2.6	2.85	V
Idem	Charging Current (pin 21)	I_L = 27mA		2.6		mA
I_R	Line Current Regulation for HV Control (pin17)	Pin 15 = Pin 21 = GND I_L = 150mA I_L = 100mA	150		 5	µA
		Pin 15 ON ; Pin 21 = GND I_L = 75mA	150			µA
   I_R/I_L		Pins 15 and 21 ON I_L = 60mA I_L = 16mA 27mA < I_L < 50mA	 150 0.8	 0.9	 100 1.0	 µA nA µA/mA
Iint	Internal Bias Current (pin 21)	I_L = 27mA, R_9 = 26.7kΩ, ($V_{20} = R_6$ x Iint + V_C)	250	280	310	µA
V_{REF}	Reference Voltage	I_L = 27mA	1.32	1.38	1.47	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
I_{REF}	Current at V_{REF}		– 10		100	µA
Vmp	Stabilized Supply at Pin 23		3.7	4.0		V
Icmp	Charging Current at Pin 23	Pin 15 = Pin 21 = GND $I_{L1} = I_L - Idem$	0.7 x x I_{L1}			mA
Ispm	Static Current at Pin 23	I_L = 6mA I_L > 25mA	0.5 2.5	 2.8		mA
Iimp	Internal Consumption		90	120	160	µA
Iea	Supply Current for Parallel Circuits (pin 12)	R_9 = 26.7kΩ I_L = 10mA I_L = 27mA I_L = 42mA	 8 21	 3 9.5 23.5		 mA mA mA
 Vrh Vrb Vrsh Vrsb	Microprocessor Reset High Treshold Low Treshold Output High Output Low	 Reset = 1 Reset = 0	 0.845 0.76 0.9	 0.89 0.8	 0.84 0.1	 Vmp (pin 23)
Vmh Vmb	Mute Microphone (pin 11)	ON OFF	1.6 0.25		 0.8	V V
Vmh Vmb	Mute Earphone (pin 14)	ON OFF	2.7 0.25		 2.1	V V
Gel Gec	Tx Gain Long Line Tx Gain Short Line	I_L = 27mA I_L = 42mA	41 34	42 36	43 38	dB
Gmf	DTMF Gain	I_L = 27mA, Pin 11 > 1.6V	41	42	43	dB
De	Tx Distorsion	I_L = 27 to 42mA V_L = 0dBm V_L = 3dBm			 3 10	 % %
Ze	Microphone Impedance		20			kΩ
Bep	Tx Noise (psophometric)	I_L > 27mA, 2k at Pins 6-8		– 73		dBmp
Re	Tx Attenuation in Mute Mode	I_L = 27mA, Pin 11 > 1.6V	60			dB
Grl Grc	Rx Gain Long Line Rx Gain Short Line	I_L = 27mA I_L = 42mA	29 22	30 24	31 26	dB
Dr	Rx Distorsion	I_L = 27 to 42mA Vec = 500mV Vec = 700mV			 3 10	 % %
Brp	Rx Noise	I_L > 27mA		– 74		dBmp
Rc	Rx Attenuation in Mute Mode	I_L = 27mA, Pin 14 > 2.7V	60			dB
Gal	Antisidetone	I_L = 27 to 42mA	– 22			dB
Zac	AC Impedance	I_L > 27mA	500	650	800	Ω
Grs	Confidence Level Vrec/Vmf	Pin 11 > 1.6V, Pin 14 > 2.7V	35.5	38.5	41.5	dB

TEST CIRCUIT



R1 = 920KΩ
R2 = 820KΩ
R3 = 1.5MΩ
R4 = 75Ω
R5 = 5.1KΩ
R8 = 13KΩ
R9 = 26.7KΩ
R11 = 140KΩ
R12 = 0Ω
R13 = 2.7KΩ
R14 = 0Ω
R15 = 140KΩ
R16 = 2.7KΩ
R17 = 1.2 KΩ
R18 = 680KΩ for private complex

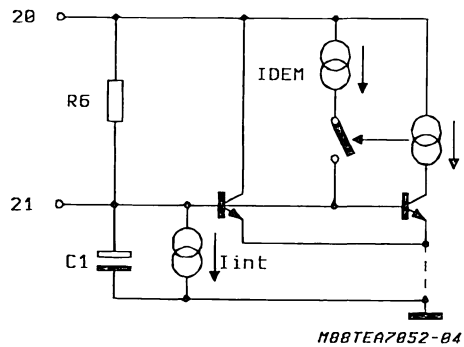
C1 = 100µF
C2 = 4.7µF
C3 = 10µF
C4 = 1µF
C5 = 100µF
C6 = 27pF
C7 = 27pF
C8 = 2.2nF
C9 = 2 2nF
C11 = 220µF

CIRCUIT DESCRIPTION

1. DC-CHARACTERISTICS

1.1. VC (pin 21). The stabilized voltage Vc is connected to Vline (pin 20) through an internal shunt regulator which presents to the line a high AC impedance at frequencies higher than 200Hz. At this purpose the value of C1 (at pin 21) must be not lower than 47 microFarad.

Figure 1.



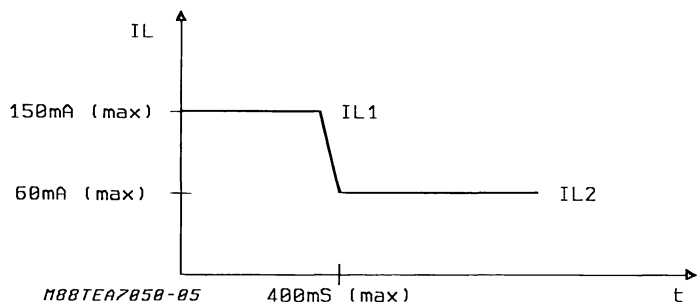
At "Off-hook", with only DC voltage applied to the line terminals, C1 fixes the timing of the line current profile at :

- 150mA max for a time shorter than 400msec (T-charge)
- 60mA max in steady state (conversation)

T-charge of 240msec (typ) is obtained with C1= 220µF.

$$\text{T-charge} = \frac{Vc \times C1}{Idem} \text{ typically.}$$

Figure 2.



1.2. HOOK DETECTION (in ring mode) (pin 15). The DC-characteristic requested to allow off-hook detection by the exchange during ring call may be accomplished :
a) through an analog control (R-C) or
b) by a microprocessor.

a) Application with standard dialer (analog control)

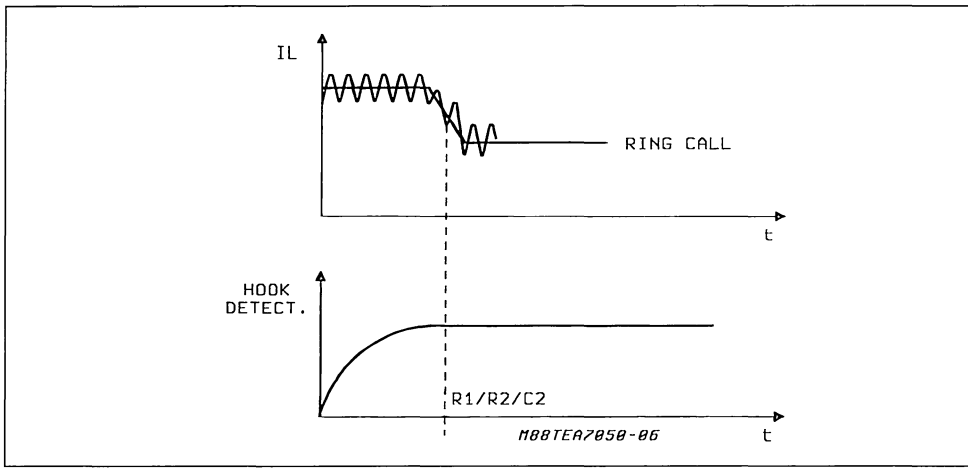
The components R1, R2 and C2 define the timing of the DC characteristic and also limit at 75mA-peak the line current during decadic dialing.

Optimum values are : - R1 x C2 = 1.8 sec ;

R2 x C2 = 0.8 sec.

To reduce the minimum time between a "on-hook / off-hook" sequence, R2 may be replaced by a switch to ground.

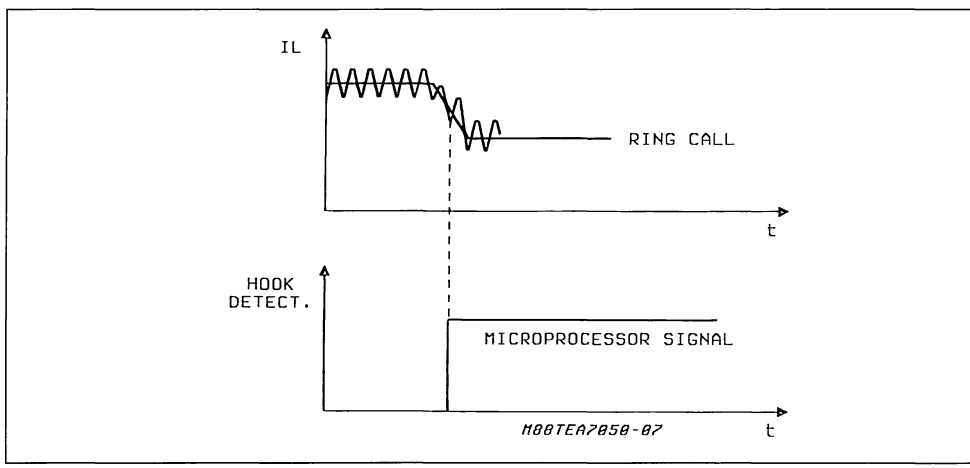
Figure 3.



b) Application with a microprocessor

Pin 15 may be controlled directly by the micro-controller, through a resistor R1b which replaces R1, R2 and C2.

Figure 4.



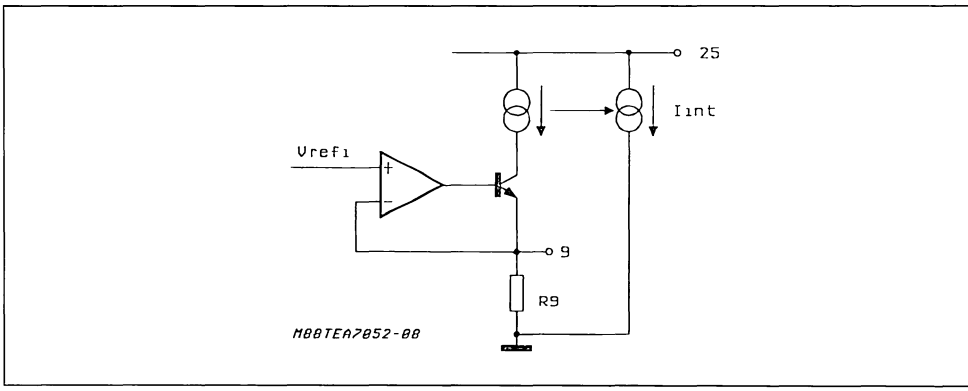
1.3. VLINE (pin 20). The line voltage (pin 20) is determined by the value of the external resistor R6 and by the internal current, Iint, flowing between Vc (pin 21) and Ground (see also paragr. 1.1.) :

Vline = Vc + R6 x Iint.

Vc is fixed by design at about 2.6 volts.

Iint is reversely related to R9 (Iint = 7.5V/R9 at Iline = 27mA).

Figure 5.



Vline must be externally adjusted (with R6) to guarantee both DC and AC characteristic in accordance to the french standards. At this purpose it is suggested that Vline equals 5.6 volts at Iline = 16mA. This typical value is obtained with R6 = 13Kohm.

1.4. HIGH VOLTAGE CONTROL STAGE (pin 17). The behaviour of "HV control" is determined by several conditions, both internal (Iline sensor) and external (pins 15 and 21) with the purpose to accomplish the different DC characteristics and transitory conditions imposed by the French specification :

a) steady DC-characteristic and lightnings (pins 15 and 21 ON)

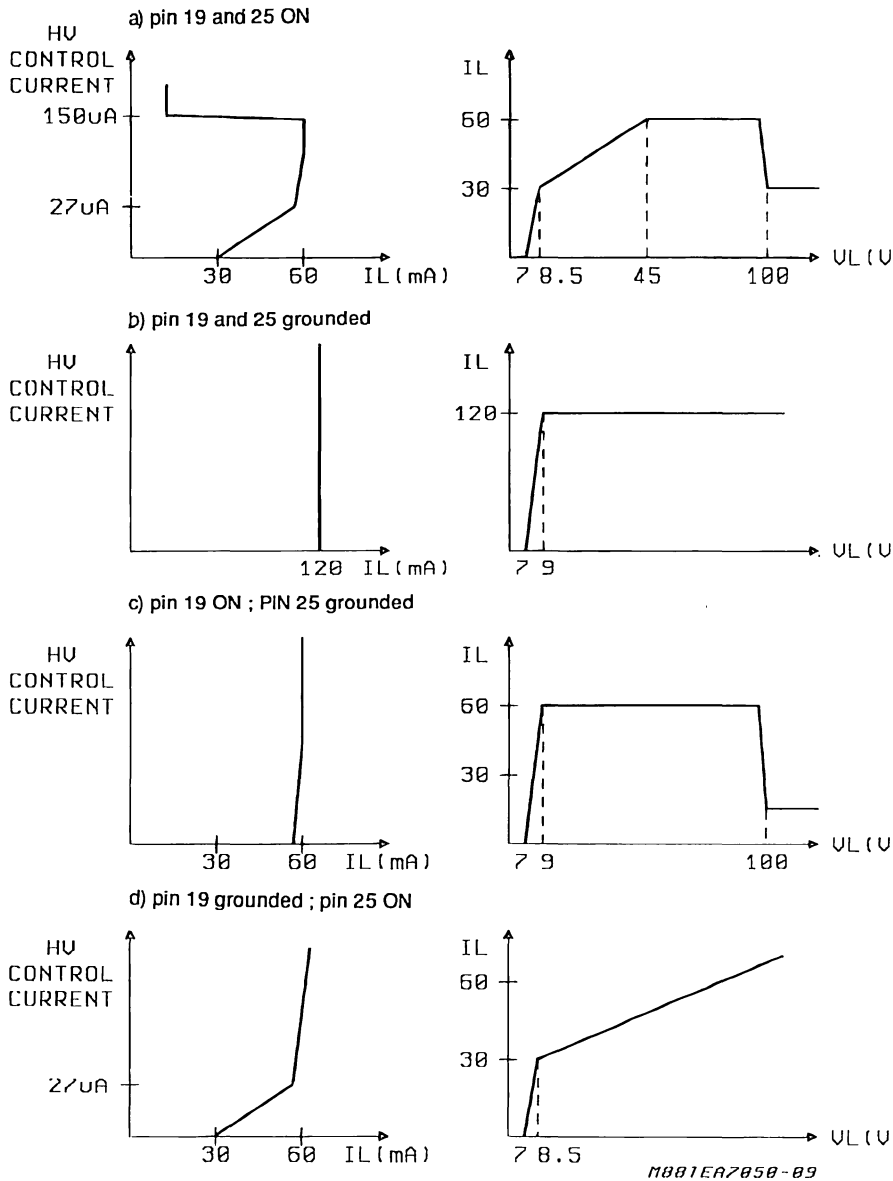
b) DC-characteristic at off-hook (pin 15 and 21 grounded)

c) DC-characteristic during decadic dialing (pin 21 grounded)

d) DC-characteristic after off-hook in ringing (pin 15 grounded)

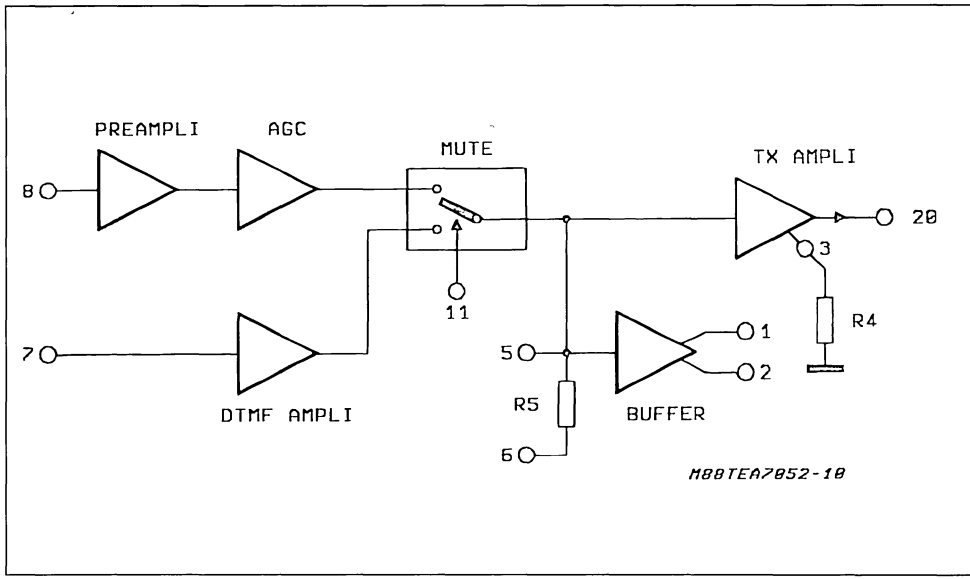
To do that, HV control pin regulates the current injected into the external high voltage transistor stage, requested by the French specification.

Figure 6.


a) pin 19 and 25 ON
HV CONTROL CURRENT
150uA
27uA
30
60
IL(mA)
IL
60
30
7
8.5
45
100
VL(V)
b) pin 19 and 25 grounded
HV CONTROL CURRENT
120 IL(mA)
IL
120
7
9
VL(V)
c) pin 19 ON ; PIN 25 grounded
HV CONTROL CURRENT
30
60
IL(mA)
IL
60
30
7
9
100
VL(V)
d) pin 19 grounded ; pin 25 ON
HV CONTROL CURRENT
27uA
30
60
IL(mA)
IL
60
30
7
8.5
VL(V)
M001EA7050-09

2. TRANSMISSION CHAIN

Figure 7.



2.1. A.G.C. IN TRANSMISSION. The transmission gain between Microphone Input (pin 8) and Vline (pin 20) is internally decreased of 6dB when the line current varies from 27mA to 42mA with a constant AC load of 600 ohms.

2.2. SENDING IMPEDANCE. The impedance of the Output Stage Amplifier, Zout, is determined by the impedance Z4 (at pin 3).

$$Zout = 10.65 \times Z4.$$

The total AC impedance shown to the line is the parallel

$$Zpar = Zout//Zint//Zext$$

where :

- Zint = 10kohm // 8.5nF (internal)
- Zext = R6 // C4 (at pin 20)

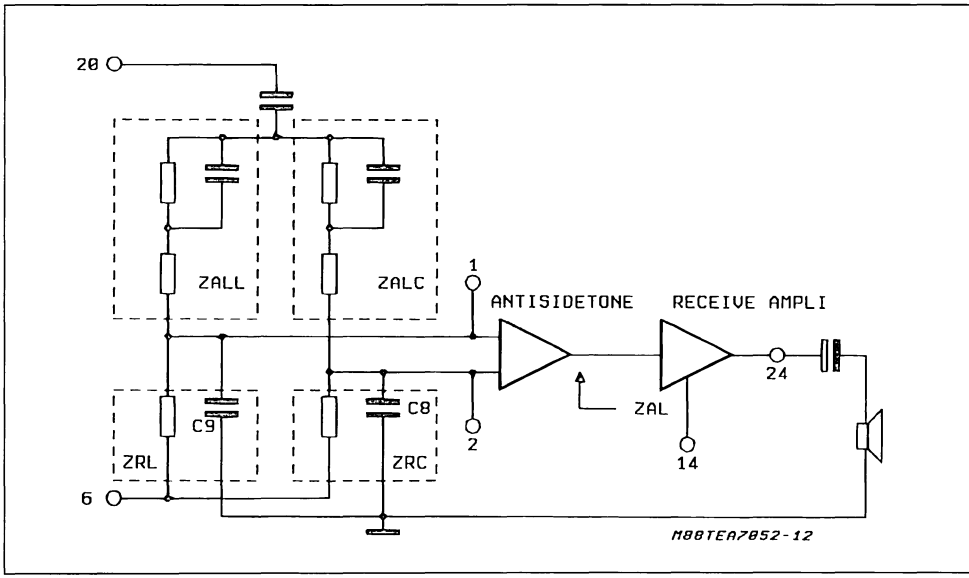
2.3. SENDING MUTE. In normal speech operation (Vmute < 0.8V), the signal at Microphone Input (pin 8) is amplified to Vline (pin 20) with the gains Gec (short line), Gel (long line) or intermediate, depending on Iline.

In sending mute condition (Vmute > 1.6V) these gains are reduced of at least 60dB. In the same condition DTMF input (pin 7) is activated, with gain Gmf to the line independent from Iline.

2.4. ANTISIDETONE BUFFER. The signal coming from the sending preamplifier is internally presented at pin 5 and than buffered to pins 1 and 2 for sidetone cancellation (see paragraph 3.2.).

3. RECEIVE CHAIN

Figure 8.



3.1. A.G.C. IN RECEIVE. As described for the transmission chain, also the receiving gains Gr, from pins 1 and 2 to pin 24, have a reduction of 6dB when Iline moves from 27mA to 42mA.

3.2. SIDETONE COMPENSATION. The circuit is provided with a double anti-sidetone network to optimize sidetone both at long and short lines.

Before entering pins 1 and 2, the received signal is attenuated by two attenuating networks :

- Zall / Zrl to pin 1 for long lines sidetone compensation,
- Zalc / Zrc to pin 2 for short lines sidetone compensation.

Zrl and Zrc define the total receive gains :

a) $\frac{V\,24}{V\,20} = Grl \times \frac{Zrc}{Zrl + Zall}$ for long lines

b) $\frac{V\,20}{V\,24} = Grc \times \frac{Zrc}{Zrc + Zalc}$ for short lines

Zall and Zalc define the sidetone compensation of the circuit.

The equivalent balancing impedance is given by the formula :

$$Zal = K \times Zalc + (1 - K) \times Zall$$

where K = 0 at Iline = 27mA or lower (long line)

K varies from 0 to 1 with Iline between 27mA and 42mA,

K = 1 at Iline = 42mA or higher (short line).

Calculations to define Zall and Zalc are :

a) $Zall = 70 \times R5 \times \frac{Zline(long) \,//\, Zext \,//\, Zint \,//\, Zout}{Zout}$

b) $Zalc = 70 \times R5 \times \frac{Zline(short) \,//\, Zext \,//\, Zint \,//\, Zout}{Zout}$

where :

- Zext = R6 // C4 // (Zelectret) (at pin 20)
- Zint = 10Kohms // 8.5nF (internal impedance)
- Zout = 10.65 x Z4 (at pin 3 ; see paragr. 2.2.)
- Zline (short) and (long) are the impedances of the line at 0Km and 3.5Km.
- R5 = 5.1Kohm ± 1 %

3.3. AC Impedance. The total AC impedance of the circuit to the line is :

Zpar = Zout//Zint//Zext//Zalc//Zall (see par. 2.2. and 3.2.)
= Zout//Zint//Zext (Zalc, Zall Zpar)

3.4. RECEIVE MUTE (and confidence level). When the receive channel is muted (Vpin 14 > 2.7V) the receive gain is reduced of 60dB minimum.

In this condition an internal connection is activated from DTMF input (pin 7) to Receive Output (pin 24) with a gain Gmf = 38.5dB to provide acoustic feedback of the DTMF transmission.

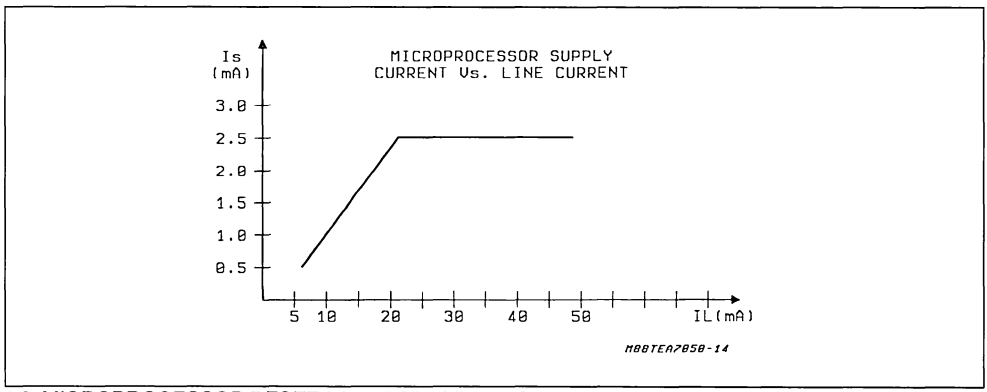
4. MICROPROCESSOR INTERFACE

4.1. MICROPROCESSOR SUPPLY (pin 23). At "off-hook" the first priority of the circuit is to make some current available at the Microprocessor Supply (pin 23) to charge quickly the external capacitor C3.

This charging current is : Icpm = 0.7 x (Iline - Idem), where Idem = 2.6mA is the current charging C1.

Vmp = 3.95V in normal operation and current increases linearly from 0.5mA min, at Iline=6mA, to 2.5mA min, at Iline = 27mA, remaining stable for higher values of Iline.

Figure 9 : Microprocessor Supply Current vs. Line Current.

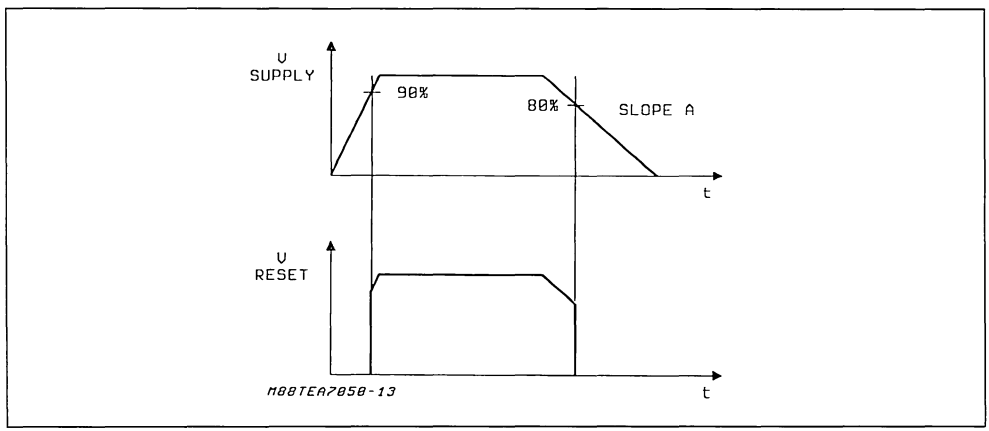


4.2. MICROPROCESSOR RESET (pin 16). The Microprocessor Reset becomes active when Vmp overcomes 85 % of its nominal level.

It becomes low when Vmp undergoes 84 %.

Slope A is related to C3, I1mp (internal consumption) and to the external load (microprocessor or dialer).

Figure 10.

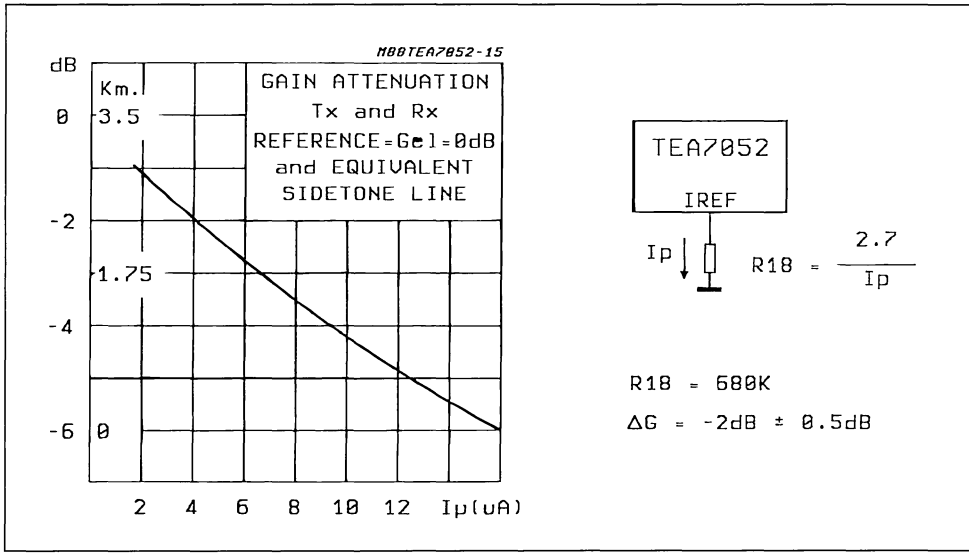


5. PUBLIC / PRIVATE

5.1. A.G.C. OFF (pin 10). An external resistor, R18, applied between pin 10 and ground disconnects the AGC control.

Sending, receiving gain and sidetone compensation are now independent of the line length and the value of the current Ip, flowing through R18, defines the length of the line for which sidetone is optimized (Ip = 2.7V / R18).

Figure 11.



5.2. SECRET FUNCTION FOR PRIVATE (pins 11 & 14). The two separate Mute pins allow "Secret Function" (only microphone muted).

As the two controls have different threshold levels, they can be operated :

a) separately through two different control logic,

b) connected in short circuit with a three levels logic (Vm = 0V speech mode ; Vm = 1.8V microph mute ;
Vm = 3V all mute).

6. POWER MANAGEMEN AND HANDS-FREE INTERFACE

6.1. Power Management (pin 12). Most of the DC current available from the line will be delivered by the speech circuit at the output Isource (pin 12) through an internal current generator.

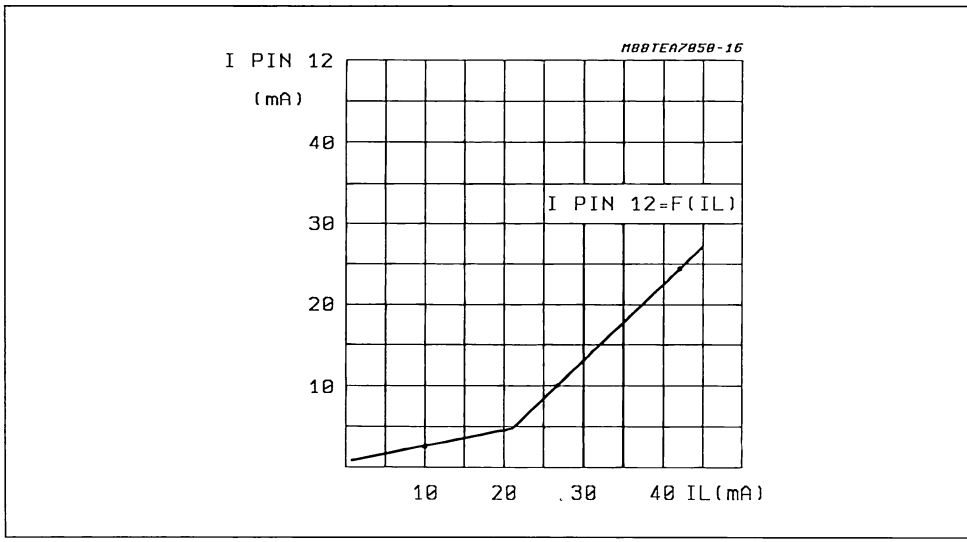
Typical values of this current, Iea, are :
- Iea = (0.3 x Iline) for Iline < 22mA
- Iea = (0.9 x Iline 13mA) for Iline > 22mA

(ex : Iline = 16mA then Iea = 4.8mA
Iline = 30mA then Iea = 14.0mA
Iline = 60mA then Iea = 41.0mA

The voltage level at pin 12 must be defined by an external regulator (i.e. : zener) and, if necessary, filtered with a capacitor (47 to 220 microF).

In case Vline (at pin 20) approaches V at pin 12, then the internal current source switches off and its DC current is shunt to ground through an internal complementary generator, thus avoiding and negative effect on the AC and DC impedances of the telephone set application.

Figure 12.



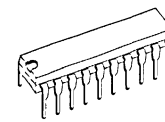
6.2. EXTRA RECEIVE OUTPUT (pin 4). The Extra Receive Signal is active also in Receive Mute condition, so allowing the transit of the receive signal from the speech circuit to an external hands-free system even when the earpiece is muted.

The gain at this pin is 30dB lower than standard Receive Output (pin 24).

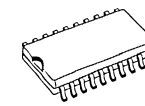
SPEECH CIRCUIT WITH POWER MANAGEMENT

PRELIMINARY DATA

- 2/4 WIRES INTERFACE WITH
  - double antisidetone network
  - AC impedance externally programmable
  - Rx output dynamic programmable
  - AGC attack-disconnect points programmable
- ANTI-CLIPPING/ANTI DISTORTION CIRCUIT PROGRAMMABLE
- DTMF INTERFACE
- 3.3 VOLTS SUPPLY FOR MICROPROCESSOR OR DIALER
- EXTRA CURRENT SUPPLY PROGRAMMABLE FOR LOUD SPEAKER
- DC CHARACTERISTIC PROGRAMMABLE FOR ALL SPECIFICATION
- LOW CURRENT OPERATION



DIP-20



SO-20L

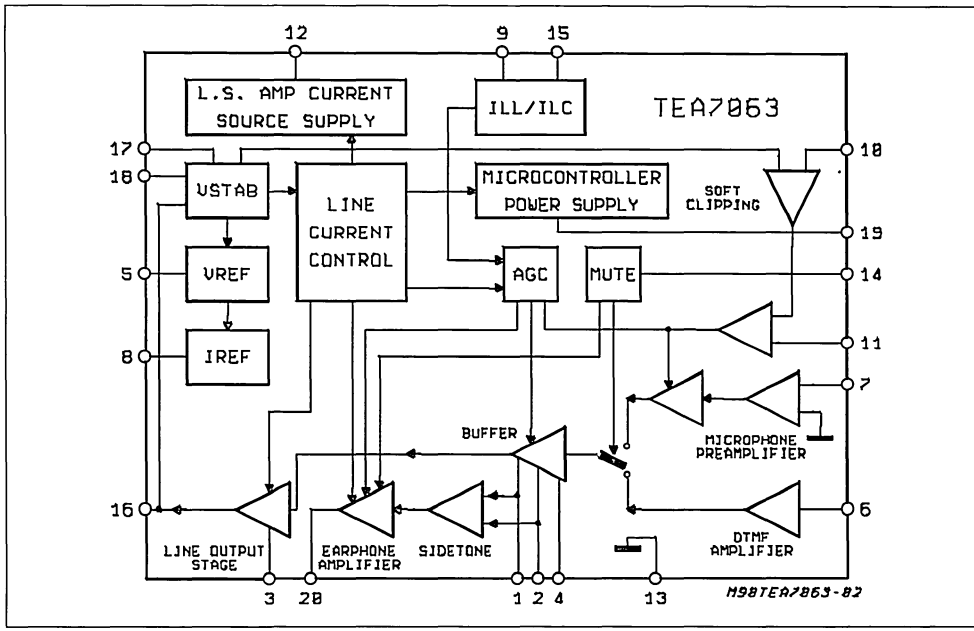
ORDERING NUMBERS:

TEA7063DP TEA7063FP

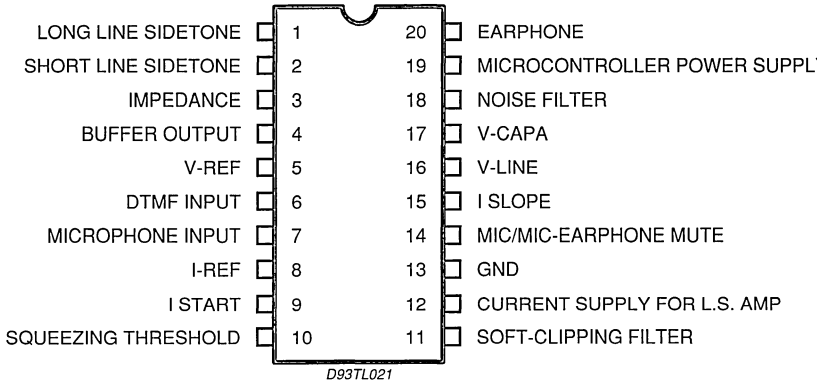
DESCRIPTION

The TEA7063 is designed to meet the different worldwide specifications for telephone set in medium and high range equipments.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



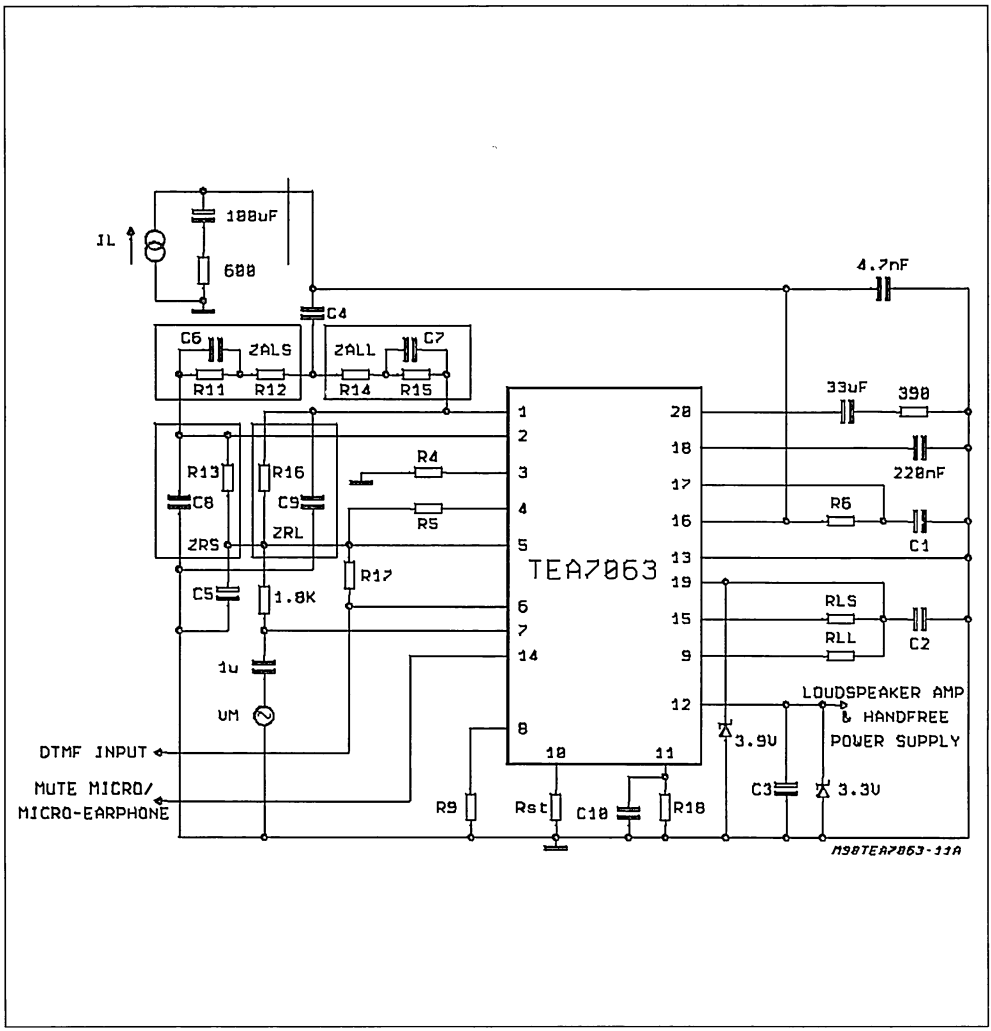
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Max. Current DC (steady)	150	mA
	Max. Voltage AC (steady)	7.5	V
	Max. Voltage AC + DC (steady)	9	V
	Max. Current (20ms) ONE SHOT	1	A
	Max. Voltage (20ms) ONE SHOT current < 1A	12	V
P_{tot}	Total Power Dissipation	1	W
T_J	Junction Temperature	130	°C

MAXIMUM OPERATING CONDITION

Symbol	Parameter	Value	Unit
V_{DC}	DC Voltage	7	V
V_{AC}	AC Voltage	2.2	Vp
I_{DC}	DC Current	110	mA
T_{OP}	Temperature Range	-20 to 70	°C

TEST CIRCUIT



R4 = 75
R5 = 5.1K
R6 = 22K
R9 = 100K
R11 = 140K
R12 = 0

R13 = 2.7K
R14 = 0
R15 = 140K
R16 = 2.7K
R17 = 1.8K
R18 = 560K

C1 = 47µF
C2 = 4.7µF
C3 = 47µF
C4 = 470nF
C5 = 100µF
C6 = 47pF

C7 = 47pF
C8 = 2.2nF
C9 = 2.2nF
C10 = 150nF

RLL = 150K
RLS = 100K
RST = 330K

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; f = 1KHz; R9 = 100KΩ; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_C	Stabilized Voltage (pin 17)	I_L = 25mA; R9 = 100KΩ	2.25	2.5	2.75	V
Iint	Internal Bias Current (pin 17)	I_L = 25mA I_L = 25mA; R9 = 180K (V16 - R6*Iint +V_C)	120	140 105	160	µA µA
V_{ref}	Reference Voltage	I_L = 25mA	1.05	1.2	1.35	V
I_{ref}	Current at V_{ref}		-100		+10	µA
V_{mp}	Stabilized Supply at pin 19		3.1	3.3	3.5	V
I_{cmp}	Charging Current at Pin 19	Pin 17 = GND	0.6 X I_{line}			mA
I_{spm}	Static Current at Pin 19	I_L = 25mA; R9 = 100KΩ	1.1	1.5		mA
		I_L = 25mA; R9 = 180KΩ		0.85		mA
I_{imp}	Internal Consumption		80	110	150	µA
I_{ea}	Supply Current for Parallel Circuits (pin 12)	I_L = 25mA I_L = 75mA	10 50	12 57		mA mA
V_{mh} V_{mb}	Mute Microphone (pin 14)	ON OFF	1.6 0.25		 0.8	V V
V_{mh} V_{mb}	Mute Earphone (pin 14)	ON OFF	2.7 0.25		 2.1	V V
I_{mleak}	Mute Leakage Current (pin 14)	V_{14} = 5V			20	µA
G_S AGC_S	Tx Gain Long Line	I_L = 25mA	41.5 -7	42.5 -6	43.5 -5	dB dB
G_mf	DTMF Gain	Pin 14 > 1.6V	41.5	42.5	43.5	dB
THD_S	Tx Distortion	I_L = 25mA V_{mic} = -3dBm -GS V_{mic} = -3dBm -GS + 15dB			 3 10	 % %
Z_e	Microphone Impedance		20			KΩ
N_{Tx}	Tx Noise (psometric)	I_L = 25mA 2KΩ at Pins 5-7		-74		dBm psoph
R_S	Tx Attenuation in Mute Mode	I_L = 25mA Pin 14 > 1.6V	60			dB
G_r AGC_r	Rx Gain Long Line Line Lenght	I_L = 25mA	29 -7	30 -6	31 -5	dB dB
THD_r	Rx Distortion	I_L = 25mA Vro = 500mV Vro = 630mV			 3 10	 % %
N_{Rx}	Rx Noise	I_L = 25mA		-74		dBmp
R_r	Rx Attenuation in Mute Mode	I_L = 25mA Pin = 14 > 2.7V	50			dB
G_{as}	Antisidetone	I_L = 25mA	22			dB
Z_{ac}	AC Impedance	I_L = 25mA	500	650	800	Ω
G_{rs}	Confidence Level = V_{LINE}/V_{REC} (in DTMF)	Pin 14 > 2.7V	35.5	38.5	41.5	dB
I_{ST}	Soft Clipping Current Level Control (pin 10)	I_L = 25mA; R9 = 100KΩ I_L = 25mA; R9 = 180KΩ	2.30	2.55 1.4	2.80	mA µA
V_{ST}	Control Voltage Range (Pin 10)	V_{ST} = R_{ST} x I_{ST}	0		1	V

CIRCUIT DESCRIPTION

1. DC CHARACTERISTICS

1.1 V_C (pin 17)

The stabilized voltage VC is connected to Vline (pin 16) through an internal shunt regulator T1, T2, which presents to the line a high AC impedance at frequecncies higher than 200Hz. At this purpose the value of C1 (at pin 17) must be not lower than 47µF (suggested value is 100µF).

The shunt regulator, T1 and T2, also controls the extra current source, or power management, at pin 12 (see also paragraph 6).

1.2 V_{LINE} (pin 16)

The line voltage (pin 16) is determined by the value of the external resistor R6 and by the internal current, I_{int}, flowing between V_C (pin 17) and Ground (see also paragr.: 1.1):

$V_{LINE} = V_C + R6 \times I_{int}$

V_C is fixed by design at about 2.5V.

I_{int} is reversely related to R9:

I_{int} = 8 Volt/R9 + 60µA at I_L > 25mA

I_{int} = 4 Volt/R9 + 60µA at I_L = 6mA

where I_L depends on I_{LB} (see supply management)

V_{LINE} must be externally adjusted (with R6) to guarantee both DC and AC characteristic in accordance to the specific standard of the different adminastrations.

Another adjustment of the DC characteristic is possible with R9. Increasing the value of R9 causes a decrease of I_{int} and consequently a reduction of the product I_{int} x R9. (see also Paragraph 7)

Figure 1

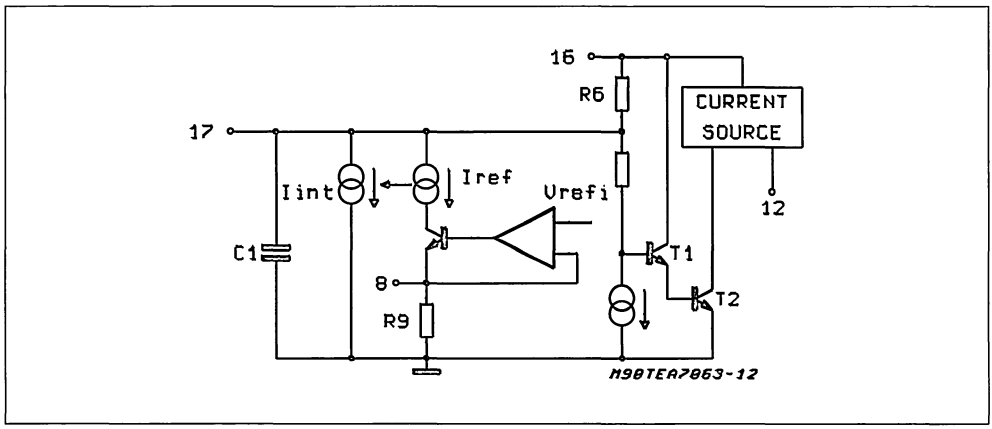
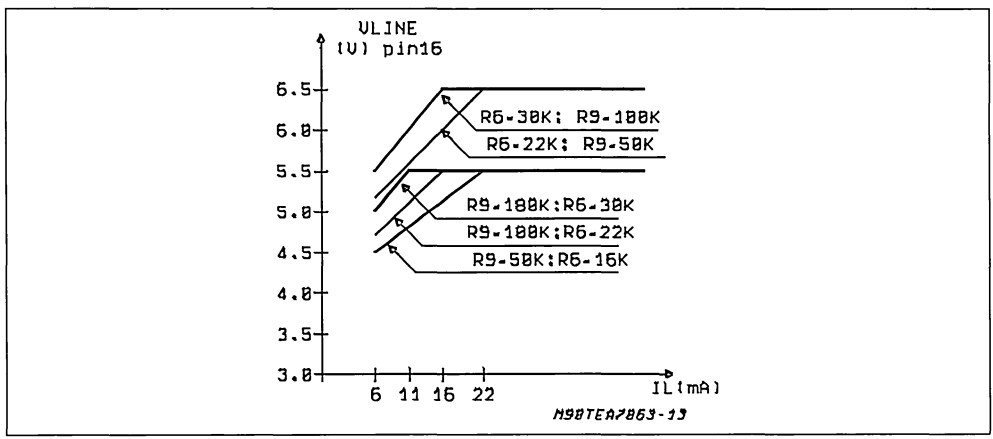


Figure 2



2. TRANSMISSION CHAIN

2.1 A.G.C. In Transmission

The transmission gain between Microphone Input (pin 7) and Vline (pin 16) is internally decreased of 6dB when the line current varies from ILL to ILS with a constant AC load of 600Ω.

The values of ILL (long line current) and ILS (short line current) are programmable through I-start (pin 9) and I-slope (pin 15) (see also paragr. 4).

2.2 Sending Impedance

The impedance of the Output Stage Amplifier, Z_{out}, is determined by the impedance Z4 (at pin 3).

$$Z_{out} = 10.65 \times Z4$$

The total AC impedance shown to the line is the parallel

$Z_{par} = Z_{out}//Z_{int}//Z_{ext}$

where:

- Z_{int} = 10KΩ//8.5 nF (internal)
- Z_{ext} = R6//C4 (at pin 16)

2.3 Sending Mute

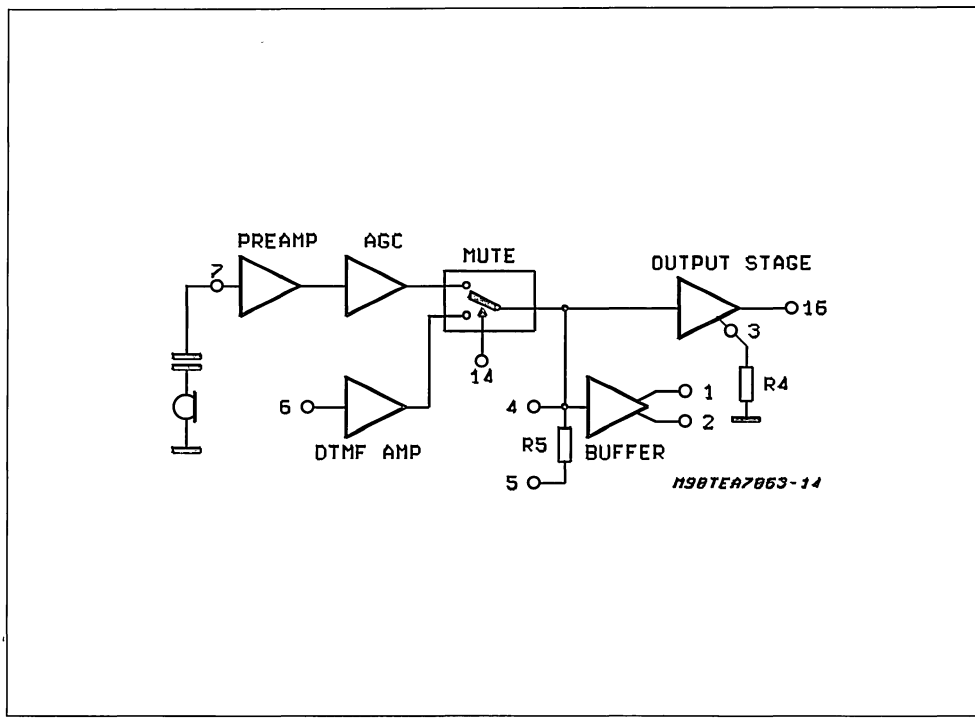
In normal speech operation (V_{mute} at pin 14 < 0.8V), the signal at Microphone Input (pin 7) is amplified to V_{line} (pin 16) with the gain Gs (long line) or 6dB lower (shorter lines) depending on AGC control (see paragr. 4).

In sending mute condition (V 14 > 1.6V) these gains are reduced of at least 60dB. In the same condition, DTMF input (pin 6) is activated, with gain Gmf to the line independent from I_{line} lenght.

2.4 Antisidetone Buffer

The signal coming from the sending preamplifier is internally presented at pin 4 and than buffered to pins 1 and 2 for sidetone cancellation (see paragraph 3.2).

Figure 3



2.5 Soft Clipping

To avoid distortion on line, the TEA7063 has a "soft clipping" on transmit channel.

The resistor (Rsoft) on pin 10 fixes the maximum AC peak dynamic on the line: V_{STL}

$$V_{STL}(Vp) = Vpin16(DC) - 1.44 \cdot \frac{R_{soft}\ (\text{pin } 10)}{R9\ (\text{pin } 8)}$$

where $R_{soft} \leq \frac{1V}{I_{ST}}$ $I_{ST} = \frac{470mV}{2 \cdot R9\ (pin8)}$

The capacitor (C10) and the resistor (R10) connected on pin 11 fixe the constant time of the soft clipping.

Recommended values: C10 = 150nF;
R10 = 560KΩ

Figure 4

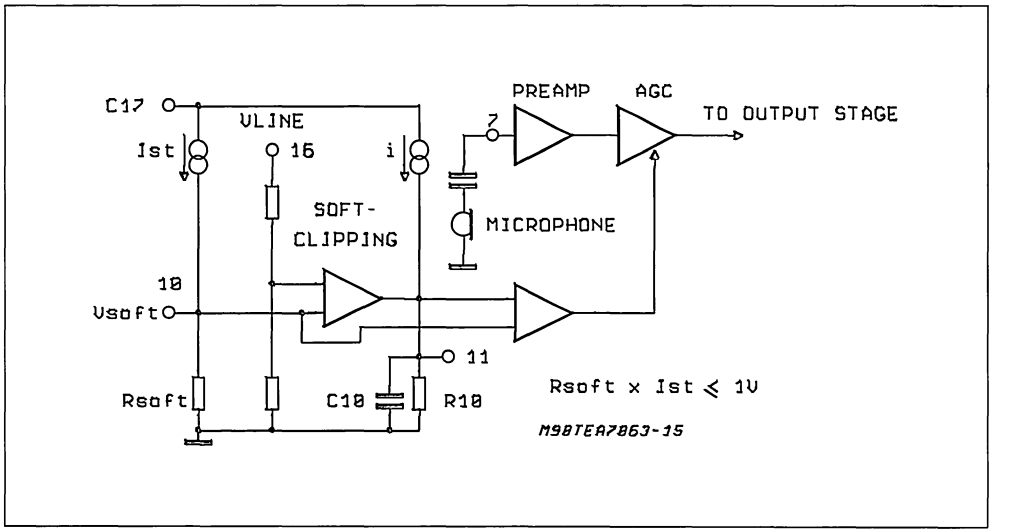
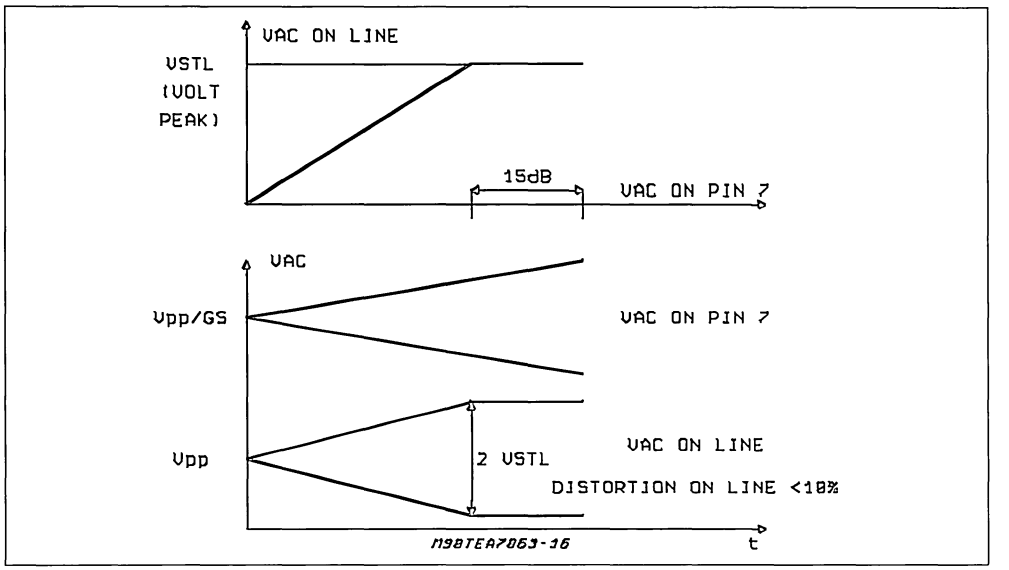


Figure 5: Transmit Curves



3. RECEIVE CHAIN

3.1 A.G.C. In Receive

As described for the transmission chain, also the receiving gains Gr, from pins 1 and 2 to pin 20, have a reduction of 6dB when Iline moves from ILL to ILS (see also paragr. 4).

3.2 Sidetone Compensation

The circuit is provided with a double anti-sidetone network to optimize both at long and short lines.

In case double antisidetone network is not requested by the application needs, pins 1 and 2 can be connected to each other and 5 external passive components can be saved (ZALL and ZRL).

Before entering pins 1 and 2, the received signal is areduced by the two attenating networks:

- ZALL/ZRL to pin 1 for long lines sidetone compensation,

- ZALS/ZRS to pin 2 for short lines sidetone compensation.

ZRL and ZRS define the total receive gains:

a) $\frac{V20}{V16} = G_r \bullet \frac{ZRL}{ZRL + ZALL}$ for long lines

b)

$\frac{V20}{V16} = (G_r - 6dB) \bullet \frac{ZRS}{ZRS + ZALS}$ for short lines

ZALL and ZALS define the sidetone compensation of the circuit.

The equivalent balancing impedance is given by the formula:

$ZAL = K \bullet ZALS + (1 - K) \bullet ZALL$

where:

-K = 0 at I_{LINE} = ILL or lower (long line)

-K varies linearly from 0 to 1 with Iline between ILL and ILS

-K = 1 at I_{LINE} = ILS or higher (short line)..

Calculations to define ZALL and ZALS are:

a)

$ZALL = 70 \bullet R5 \bullet \frac{Z_{line\ (\ long\ )} // Z_{ext} // Z_{int} // Z_{out}}{Z_{out}}$

b)

$ZALL = 70 \bullet R5 \bullet \frac{Z_{line\ (\ short\ )} // Z_{ext} // Z_{int} // Z_{out}}{Z_{out}}$

where:

- Z_{ext} = R6//C4//(Zelectret) (at pin 13)
- Z_{int} = 10KΩ//8.5nF (internal impedance)
- Z_{out} = 10.65 • Z4 (at pin 3; see paragr. 2.2)
- Zline (short) and (long) are the impedances of the line at minimum and naximum line lenght
- R5 = 5.1KΩ ±1% (typically)

3.3 AC Impedance

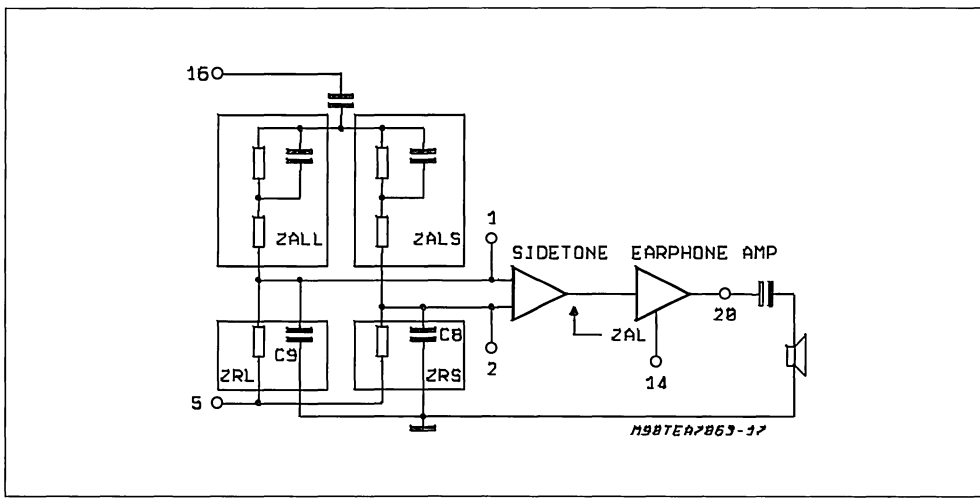
The total AC impedance of the circuit to the line is:

ZAC = Zout//Zint//Zext (ZALS, ZALL >>ZAC)

3.4 Receive Mute (and confidence level)

When the receive channel is muted (Vpin 14 > 2.7V) the receive gain is reduced of 60dB minimum.

Figure 6



In this condition an internal connection is activated from line DTMF output (pin 16) to Receive Output (pin 20) with an attenuation GRS = 38.5dB to provide acoustic feedback of the DTMF emission.

4. A.G.C AND SIDETONE PROGRAMMING

4.1 Programmable Controls

AGC and sidetone attack and disonnect points (or currents) are programmable externally through two independents pins, I-start (pin 9) and I-slope (pin 15).

4.2 I-Start (pin 9)

An external resistor RLL connected between I-start (pin 9) and Microprocessor Supply (pin 19) controls the attack point of AGC and ZAL (antisidetone Z).

ILL is the line current at which the control starts. Formulas for ILL and RLL with R9 = 100K are:

$$ILL = \frac{2880}{RLL} + 11mA$$

$$RLL = \frac{2880}{(ILL - 11mA)}$$

4.3 I-Slope (pin 15)

An external resistor RLS connected between I-slope (pin 15) and Microprocessor Supply (pin 19) controls the disconnected point of AGC and ZAS (antisidetone Z). ILS is the line current at which the control stops. Formulas for ILS and RLS with R9 = 100K are:

$$ILS = \frac{4680}{RLS} + ILL;$$

$$RLS = \frac{4680}{(ILS - ILL)}$$

4.4 A.G.C. OFF (pin 9 and 15)

Programming ILL and ILS respectively higher than 70mA and 450mA is forcing the IC in AGC OFF Condition.

Suggested external components are:
RLL = 51KΩ and RLS = 10KΩ

In this case sending, receiving gain and sidetone compensation are independent of the line lenght. Pins 1 and 2 can be connected to each other saving 5 passive external components at pin 2.

4.5 Secret Function for Private (pin 14)

The two separate thresholds for sending and Receiving Mute (pin 14) allow "Secret Function" (only microphone muted).

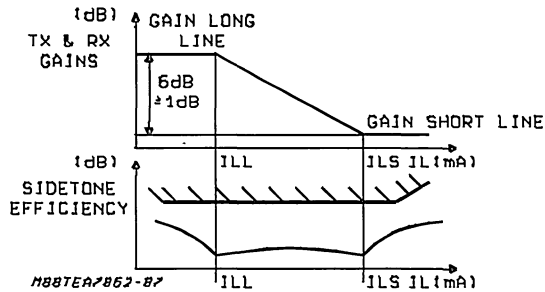
Pin 14 can be set:

a) between 0.25V and 0.8V for speech mode,

b) between 1.6V and 2.1V for "secret" mode (microphone muted),

c) between 2.7V and 3.3V for "all muted" mode

Figure 7



5. MICROPROCESSOR INTERFACE

5.1 Microprocessor Supply (pin 19)

At "off-hook" the first priority of the circuit is to make some current available at the Microprocessor Supply (pin 19) to charge quickly the external capacitor C2.

This charging current is $I_{cpm} = 0.6 \bullet I_{LINE}$

T-charge of about 10ms is necessary, with C2 = 47/µF. to charge pin 19 at the specified value of 3.3V typical at I_{LINE} = 25mA:

$$\text{T-charge} = \frac{3.3V \circ C2}{0.6 \circ I_{LINE}} \text{ typically}$$

V_{mp} = 3.3V in normal operation and current increases linearly from 0.5mA min, at I_{LINE} = 6mA, to1.5mA, at I_{LINE} = 25mA, remaining stable for higher values of I_{LINE}. (with R9 = 100K)

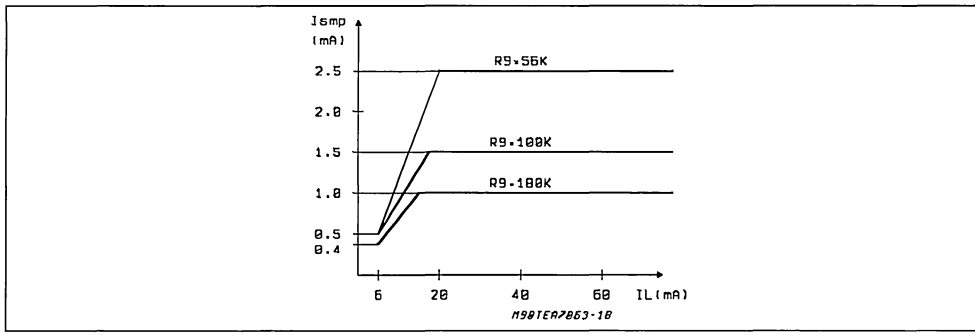
In general:

$$I_{mp} = \frac{130Volt}{R9} + 0.3mA \text{ at } I_L > 25mA$$

$$I_{mp} = \frac{11Volt}{R9} + 0.3mA \text{ at } I_L > 6mA$$

A zener of 3.9V typical is generally suggested to

Figure 8



6. CURRENT SOURCE FOR SPEAKERPHONE

6.1 Current Source (pin 12)

Most of the DC current available from the line is delivered by the speech circuit at the output I_{source} (pin 12) through an internal current generator.

Typical values of this current, I_{LS} with R9 = 100K, are:

$I_{LS} = (0.3 \bullet I_{LINE})$ for $I_{LINE} < 16.5mA$
$I_{LS} = (0.9 \bullet I_{LINE} - 10mA)$ for $I_{LINE} > 16.5mA$

(ex: I_{LINE} = 16mA then I_{LS} = 5mA

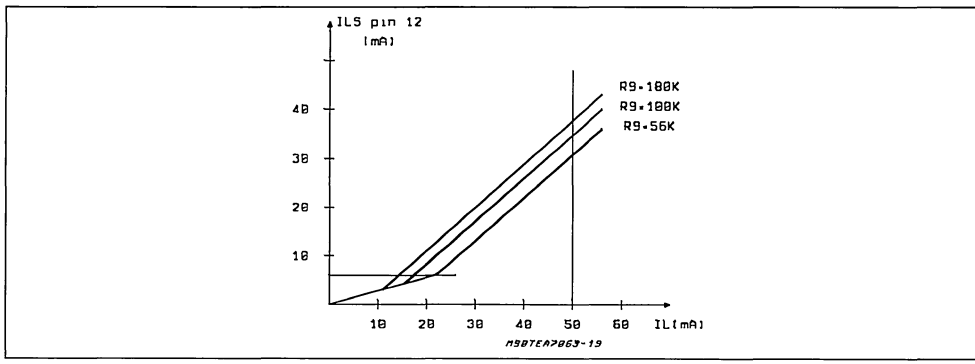
I_{LINE} = 30mA then I_{LS} = 17mA

I_{LINE} = 60mA then I_{LS} = 44mA).

The voltage level at pin 12 must be defined by an external regulator (i.e.: zener) and, if necessary, filtered with a capacitor (47 to 220µF).

In case V_{LINE} (at pin 16) approaches voltage at pin 12, then the internal current source switches off and its DC current is shunt to ground through and internal complementary generator, thus avoiding any negative effect on the AC and DC impedances of the telephone set application.

Figure 9



7. INTERNAL DESCRIPTION OF CURRENT MANAGEMENT

7.1 Internal Power Supply Management

R9 fixes the line power supply management.
R9 fixes the values of: I_{ear}, I_{up}, I_{ref} and ILS.

A current line information is used to modifie the values of I_{ear}, I_{up}, I_{ref} and ILS between a minimum and a maximum values.

On Fig 10:
The transmit output stage is represented by a current source (I_{tr}). The I_{tr} value depends of the DC voltage on V_{LINE} (pin 16) and R_{ZAC} value.

The other internal stages connected to V_{LINE} (pin 16) are represented by a constant 1.3mA current source.

7.2 DC Characteristics (internal)

The DC characteristic is equals to:

$$V_{LINE} \text{ (pin 16)} = V_C \text{ (pin 17)} + R6 \bullet I_{int}$$

Iint is the sum of all the current sources connected on VC (pin 17):
$[I_p + I_{ref} + Vpin17 / (r7 + r8)]$

- I_p is the bias internal operational amplifiers power supply.
- $I_{ref} = 1 / 3 \bullet (V_{ref1} / R9)$; with $V_{ref1} = 470mV$
- $I_{ref} = 156 / R9$ mA

The current line information changes Iint value;

at low line current (6mA): $I_{int} = 4V / R9 + 60\mu A$

at low line current (IL = ILb): $I_{int} = 8V / R9 + 60\mu A$

7.3 Microcontroller Supply (internal)

$I_{up} = [(p2 / r2) \bullet I_{ref} + 0.3]$ mA $= [(p2 / r2) \bullet 156 / R9) + 0.3]$ mA

The current line information changes p2/r2 value;

at low line current (6mA): p2 / r2 = 70
at a line current (IL = ILb): p2 / r2 = 820

7.4 Earphone Current Supply (internal)

$I_{ear} = (p1 / r1) \bullet I_{ref}$ mA $= (p1 / r1) \bullet (156 / R9)$ mA

The current line information changes p1/r1 value;

at low line current (6mA): (p1 / r1) = 200
at a line current (IL = ILb): p1 / r1 = 2700

The maximum peak dynamic on the earphone is:
$V_{pear} = Z_{ear} \bullet I_{ear}$

7.5 Transmit Output Stage (internal)

The output stage bias current depends of the DC voltage on pin 16 and on R_{ZAC} impedance.

$$I_{tr} = \frac{0.1425 \bullet V_{LINE} - 0.517}{R_Z}$$ (R_Z is the resistor connected betwee pin3 and the ground)

7.6 Loudspeaker Current Source (internal)

The current source for external peripherals has two slopes:

- First slope; before I_{ear}, I_{up}, I_{tr} and I_{int} are stabilized at their maximum values: (IL = ILb)

$$ILS = 0.285 \bullet IL$$

- Second slope; after I_{ear}, I_{up}, I_{tr} and I_{int} are stabilized at their maximum values: (for IL > ILb)

$$\Delta (ILS) = 0.91 \bullet \Delta(I_{LINE}$$

I_{ear}, I_{up}, I_{tr} and I_{int} are stabilized at their maximum values between 16 and 26mA, the absolute IL value depends of R9 value. The line current (ILb) where I_{ear}, I_{up}, I_{tr}, I_{int} are stabilized at their maximum values and where the slope of ILS change is:

$$ILb = \frac{I_{ear} + I_{up} + I_{tr} + I_{int} + 1.3}{0.715}$$

7.7 Numerical Example

1) R9 = 100KΩ; R6 = 25KΩ

♦ DC characteristic = 6V for I_{int} max:
= 5V for I_{int} min:

I_{int} min (IL = 6mA) = 4 /100K + 60 = 100µA
I_{int} min (IL = ILb) = 8 /100K + 60 = 140µA

Vpin17 = 2.5V ⇒ R6 = 25KΩ ⇒
Vpin16 min (IL = 6mA) = 2.5 + 25 • 100E - 3 = 5V
Vpin16 max (IL = ILb) = 2.5 + 25 • 140E - 3 = 6V

♦ Current Sources

I_{up} min (IL = 6mA) = 0.4mA
I_{up} max (IL = ILb) = 1.6mA

I_{ear} min (IL = 6mA) = 0.3mA
I_{ear} max (IL = ILb) = 4.2mA

with R_Z = 75Ω

I_{tr} min (IL = 6mA) = 2.6mA
I_{tr} max (IL = ILb) = 4.5mA

ILS min (IL = 6mA) = 1.3mA

♦ ILb
$$ILb = \frac{1.6 + 4.2 + 4.5 + 0.14 + 1.3}{0.715} \text{ mA}$$

ILb = 16.5mA

ILS (for IL = ILb) = 0.285 • ILb = 4.7mA

♦ at IL = 100mA:

Δ(ILS) = 0.91 • Δ(IL) = 0.91 • (100 - 16.5) = 76mA
ILS = 4.7 + 76 = 80.7mA

2) R9 = 56KΩ; R6 = 18KΩ

♦ DC characteristic = 6.1V for I_{int} max:
= 4.8V for I_{int} min:

I_{int} min (IL = 6mA) = 4 /56K + 60 = 130µA
I_{int} min (IL = ILb) = 8 /56K + 60 = 200µA

Vpin17 = 2.5V ⇒ R6 = 18KΩ ⇒
Vpin16 min (IL = 6mA) = 2.5 + 18 • 130E - 3 = 4.85V
Vpin16 max (IL = ILb) = 2.5 + 18 • 200E - 3 = 6.1V

♦ Current Sources

I_{up} min (IL = 6mA) = 0.5mA
I_{up} max (IL = ILb) = 2.5mA

I_{ear} min (IL = 6mA) = 0.55mA
I_{ear} max (IL = ILb) = 7.5mA

with R_Z = 75Ω

I_{tr} min (IL = 6mA) = 2.35mA
I_{tr} max (IL = ILb) = 4.5mA

ILS min (IL = 6mA) = 1.17mA

♦ $ILb = \frac{2.5 + 7.5 + 4.5 + 0.2 + 1.3}{0.715}$ mA

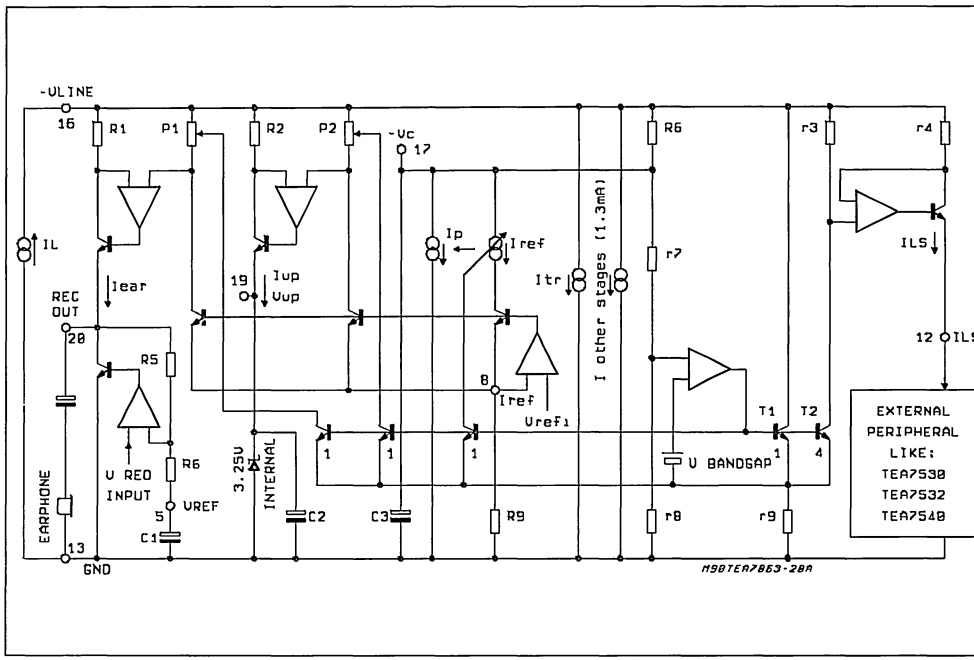
ILb = 22.4mA

ILS (for IL = ILb) = 0.285 • ILb = 6.4mA

♦ at IL = 100mA:

Δ(ILS) = 0.91 • Δ(IL) = 0.91 • (100 - 22.6) = 64mA
ILS = 6.4 + 64 = 70.4mA

Figure 10: Line Power Supply Management



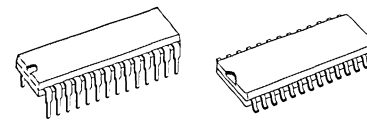
SGS-THOMSON MICROELECTRONICS

TEA7088

LOW RANGE PHONE DEDICATED CHIP

PRODUCT PREVIEW

- RING
  - GENERATION OF 8 MELODY TONES (including the 3 German melody tones)
  - 4 STEP DIGITAL CONTROL ON THE AMPLIFIER OUTPUT LEVEL
- SPEECH
  - SOFTCLIPPING ON SENDING CHANNEL
  - RECEIVE AMPLIFIER FOR PIEZO OR ELECTRODYNAMIC TRANSDUCER
  - +6 dB MODE ON RECEIVE CHANNEL
  - AGC SLOPE LINE LOSS COMPENSATION PROGRAMMABLE
  - LINE POWER MANAGEMENT
- DIALLING
  - PULSE DIALLING INTERFACE
  - DTMF GENERATOR
- MICROCONTROLLER POWER SUPPLY
- MICROCONTROLLER CONTROL INTERFACE INCLUDING SERIAL BUS
- LINE CURRENT SOURCE SUPPLY FOR EXTERNAL PERIPHERALS



DIP28 **SO28**

ORDERING NUMBERS:

TEA7088DP TEA7088FP

DESCRIPTION

This TEA7088 is a single chip device which integrates the three basic functions of a low range telephone set:
- Speech network
- DTMF generator
- Ringer on buzzer

A complete low-end telephone set can be designed with a TEA7088 associated with a microcontroller.

SPEECH

The speech network includes:

- a low noise transmit channel suitable for any kind of microphone transducer. Softclipping on transmit line signal is provided by the chip.
- a low noise receive channel with symmetrical outputs to be compatible with both piezoceramic and electrodynamic earpiece. An additional 6dB gain can be inserted in the receive channel.
- a line length depending gain control. Starting point of gain decreases is fixed @ 25mA line current; slope of gain decrease is externally adjustable for a constant gain over line current, the pin AGC must be left open.

The phone impedance and sidetone can be tuned through external networks.

DTMF GENERATOR

The onboard DTMF generator fullfils the CEPT requirements with an external single pole filter. A single quartz is used on the microcontroller (ST629X) to drive the TEA7088. If more tones are requested the input RM/MSK allows to inject tones generated by the microcontroller.

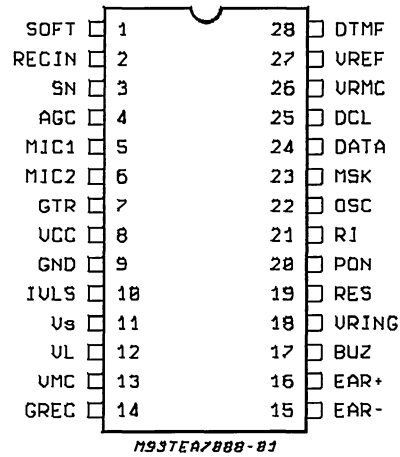
RINGER

Up to 8 different tones can be generated by the TEA7088 ringer. The digital volume control of the ringer can be performed through a specific command (4 steps). A ring indication signal is provided to the microcontroller by the TEA7088.

FURTHER ADVANTAGES

- The microcontroller power supply is provided by the TEA7088. The power supply is specifically designed to cope with a long flash or a long ground key duration.
- The TEA7088 is able to supply the necessary current to an external speakerphone circuit TEA7540 or loudspeaker amplifier TEA7530 and TEA7532 without any additional circuitry.
- Line current and reset indications are provided to the microcontroller by the chip.
- The microcontroller drives the TEA7088 through a 2 wires serial interface.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{OP}	Operating Temperature	-25 to +70	°C
T_{stg}	Storage Temperature	-55 to +150	°C
I_{LINE}	Line Current	120	mA
I_{RING}	Ring Current	50	mA
Authorized voltage on Pin	2 - RECIN	13	V
	3 - SN	12	V
	8 - VCC	12	V
	10 - IVLS	6	V
	12 - VL	12	V
	13 - VMC	6	V
	17 - BUZ	V_{RING} +0.3/GND -0.3	V
	19 - RES	V_{RMC} +0.3/GND -0.3	V
	20 - PON	V_{RMC} +0.3/GND -0.3	V
	21 - RI	V_{RMC} +0.3/GND -0.3	V
	22 - OSC	V_{RMC} +0.3/GND -0.3	V
	23 - MSK	V_{RMC} +0.3/GND -0.3	V
	24 - DATA	V_{RMC} +0.3/GND -0.3	V
	25 - DCL	V_{RMC} +0.3/GND -0.3	V
	26 - VRMC	5	V
T_j	Junction Temperature	-25 to 110	°C

Figure 1: Block Diagram

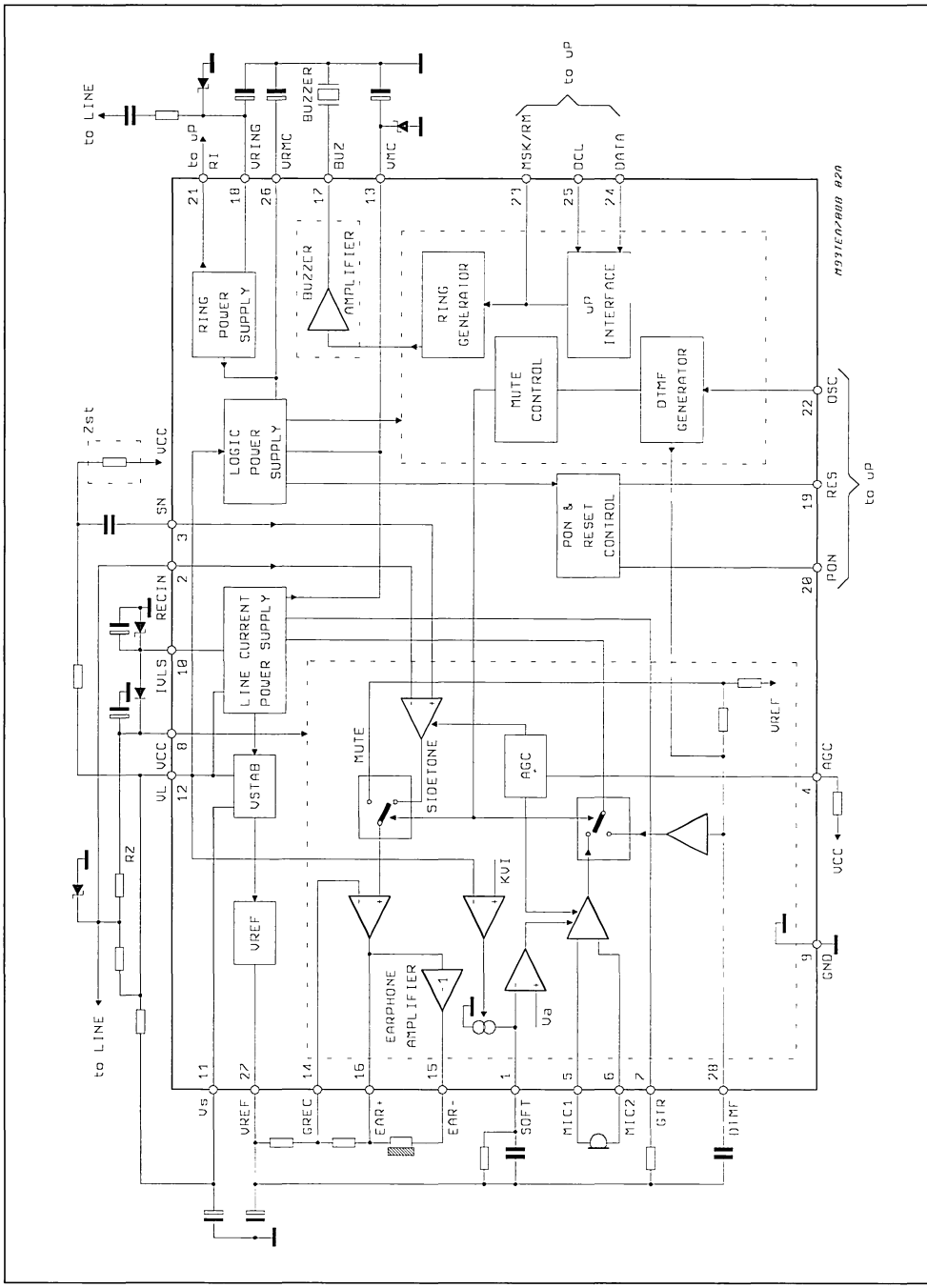
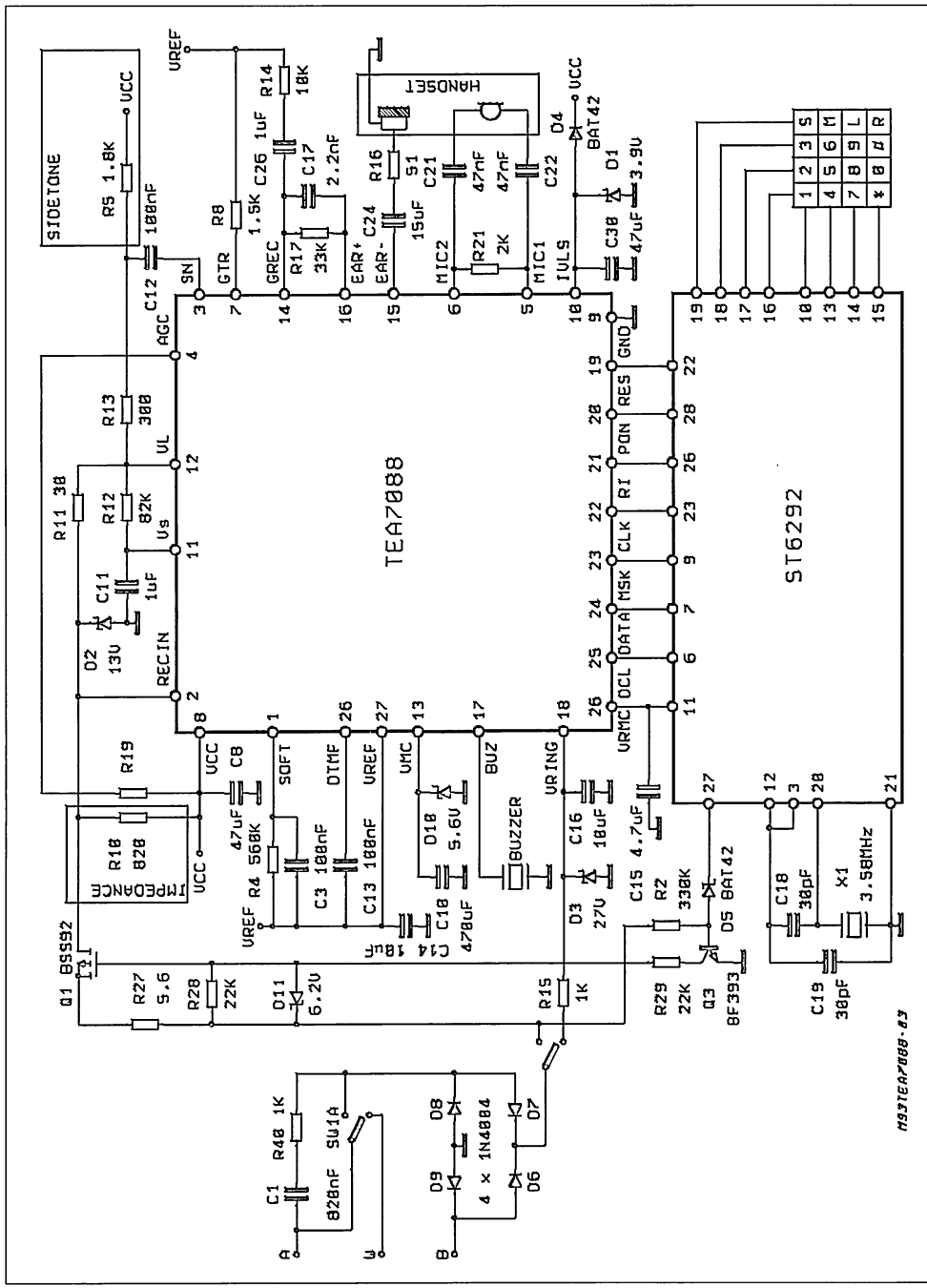


Figure 2: Typical Application



LOW RANGE PHONE DEDICATED CHIP

PRELIMINARY DATA

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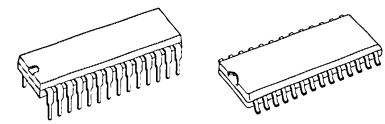


DIP28 **SO28**

ORDERING NUMBERS:

TEA7090DP TEA7090FP

DESCRIPTION

This TEA7090 is a single chip device which integrates the three basic functions of a low range telephone set:
- Speech network
- DTMF generator
- Ringer on buzzer

A complete low-end telephone set can be designed with a TEA7090 associated with a microcontroller. The electrical characteristics of the device suit the German telephone set public and private market.

SPEECH

The speech network includes:

- a low noise transmit channel suitable for any kind of microphone transducer. Softclipping on transmit line signal is provided by the chip.
- a low noise receive channel with symmetrical outputs to be compatible with both piezoceramic and electrodynamic earpiece. An additional 6dB gain can be inserted in the receive channel.

The phone impedance and sidetone can be tuned through external networks.

DTMF GENERATOR

The onboard DTMF generator fullfils the CEPT requirements with an external single pole filter. A single quartz is used on the microcontroller (ST629X) to drive the TEA7090.

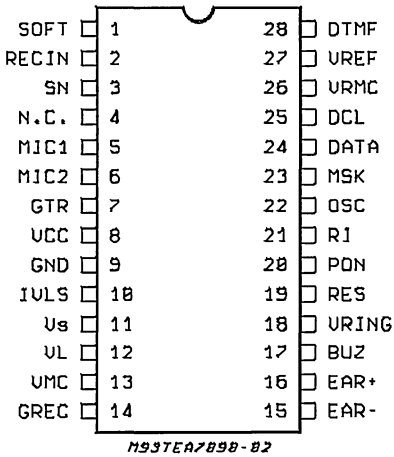
RINGER

Up to 8 different tones can be generated by the TEA7090 ringer. The digital volume control of the ringer can be performed through a specific command (4 steps). A ring indication signal is provided to the microcontroller by the TEA7090.

FURTHER ADVANTAGES

- The microcontroller power supply is provided by the TEA7090. The power supply is specifically designed to cope with a long flash or a long ground key duration.
- The TEA7090 is able to supply the necessary current to an external speakerphone circuit or loudspeaker amplifier without any additional circuitry.
- Line current and reset indications are provided to the microcontroller by the chip.
- The microcontroller drives the TEA7090 through a 2 wires serial interface.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{OP}	Operating Temperature	-25 to +70	°C
T_{stg}	Storage Temperature	-55 to +150	°C
I_{LINE}	Line Current	120	mA
I_{RING}	Ring Current	50	mA
Authorized voltage on Pin	2 - RECIN	13	V
	3 - SN	12	V
	8 - VCC	12	V
	10 - IVLS	6	V
	12 - VL	12	V
	13 - VMC	6	V
	17 - BUZ	V_{RING} +0.3/GND -0.3	V
	19 - RES	V_{RMC} +0.3/GND -0.3	V
	20 - PON	V_{RMC} +0.3/GND -0.3	V
	21 - RI	V_{RMC} +0.3/GND -0.3	V
	22 - OSC	V_{RMC} +0.3/GND -0.3	V
	23 - MSK	V_{RMC} +0.3/GND -0.3	V
	24 - DATA	V_{RMC} +0.3/GND -0.3	V
	25 - DCL	V_{RMC} +0.3/GND -0.3	V
	26 - VRMC	5	V
T_j	Junction Temperature	-25 to 110	°C

Figure 1: Block Diagram

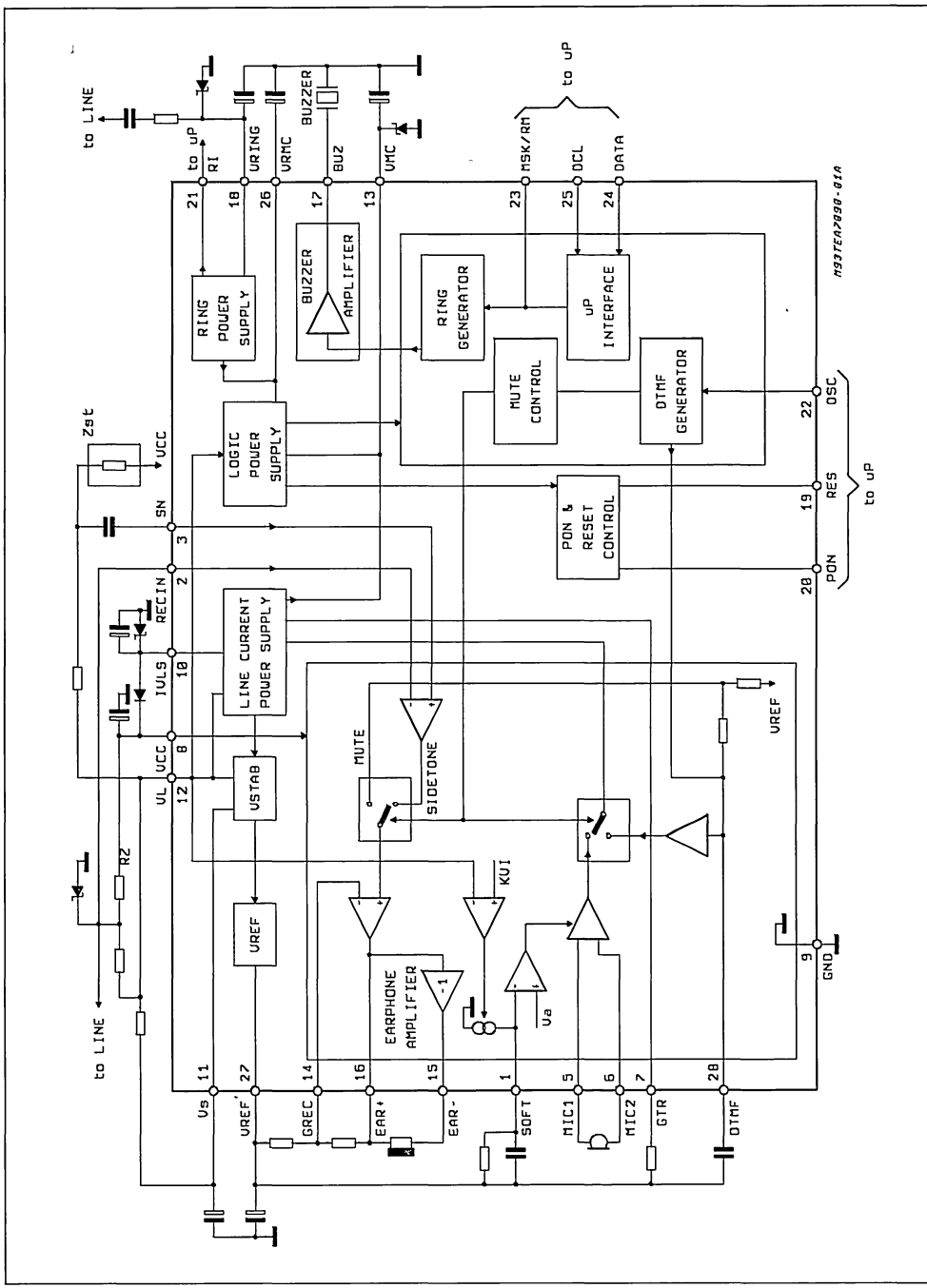
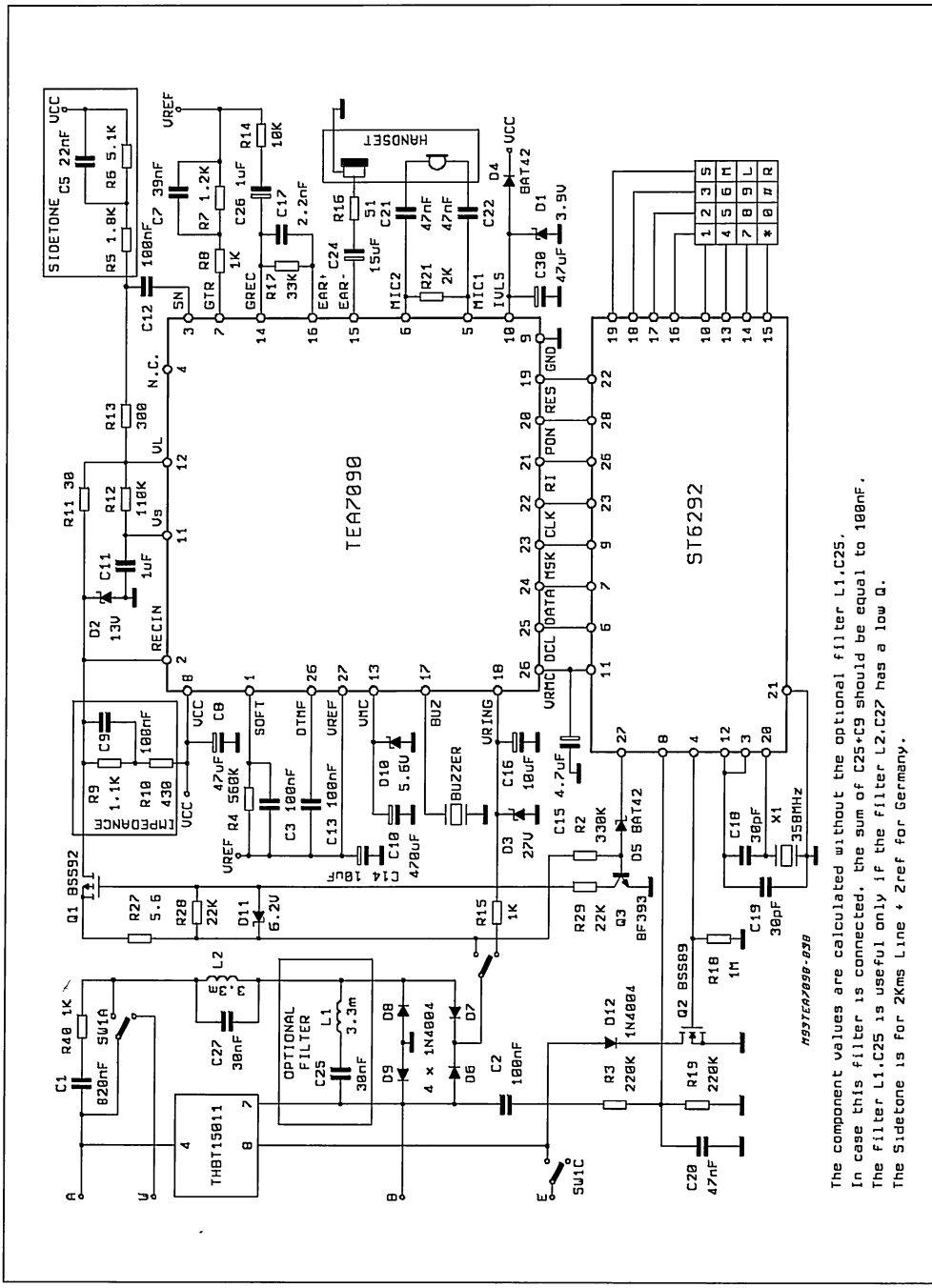


Figure 2: Typical Application for Germany.



TYPICAL DIAGRAM and GENERAL CHARACTERISTICS

A typical diagram is given on Fig 1.
The values of the different networks used in this datasheet are defined as followed:

- The Return loss is adjusted by RZ on the German complex impedance (220 + 820//115nF).
- The transmit adjust gain network (ZGTR) is calculated in order to have a steady gain on a 600Ω load on line (44dB typical).
- The sidetone network (ZST) is set to be Lower than 20dB (Vear/Vmic) on a 600Ω load on line.
- The DC characteristics are set by a resistor of 110k between VL and VS

DC CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_L	Line Voltage (Pin 12) - In speech and DTMF mode - In Mask mode	Test 1 I_L = 20mA I_L = 50mA I_L = 20mA	 5.4 6.5 	 6 7.2 	 6.6 7.9 3.5	 V V V
I_{VRMC} V_{RMC}	Stabilized Voltage (Pin 26) - Output current - Output Voltage	Test 1 I_L = 12mA I_L = 20mA I_L = 20mA	 1 1.5 3.2	 3.4	 3.6	 mA mA V
I_{VMC}	Unstabilized Voltage (Pin 13) - Start up Current - Output Current	Test 1 V_{RMC} = 2V I_L = 20mA I_L = 20mA	 12 4.5	 15 5	 	 mA mA
I_{LS}	Line Current Source Supply (Pin 10)	Test 1 I_L = 20mA I_L = 50mA	 	 11.4 39	 	 mA mA

The line current source supply depends of I_L;
- For I_L < 18mA: **I_{LS} (mA) = 0.61 x I_L(mA) - 0.8mA**
- For I_L > 18mA: **I_{LS} (mA) = 0.92 x I_L(mA) - 7mA**

On this pin the maximum output level is;
Vpin10 = Vpin12 - (1.2 + 10 x I_{LS})
and **Vpin10 < 6V**

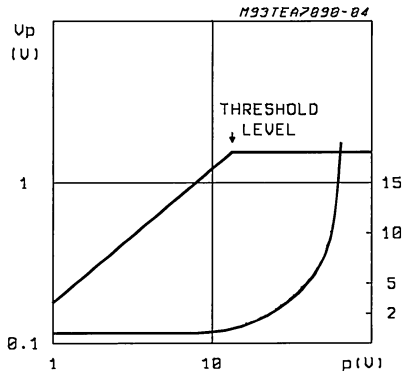
AC CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R1	RETURN LOSS	Test 2 RL = 220 + 820 // 115nF F = 300/3400Hz	17			dB

TRANSMIT CHARACTERISTICS (T_{amb} = 25°C; F = 1KHz)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Gtr	Gain	Test 4 V_{em} = -55dBV R_{tg} = 910 + 1.1K // 39nF I_L = 20mA	43	44	45	dB
ΔGtr	Gain Variation	Test 4 –75dBV < V_{em} < –55dBV R_{tg} = 910 + 1.1K // 39nF 20mA < I_L < 50mA	-0.5		0.5	dB
Zmic	Microphone Input Impedance		32	40	48	KΩ
Nt	Noise	Test 4 2KΩ on microphone inputs I_L = 20mA		-76		dBmp
Mmic	Microphone Mute	Test 4 Vem = -55dBV	60			dB
Dt VLmax	Soft Clipping - Maximum Level on Line	Test 4 See Fig. 3 d < 2% I_L = 20mA		 1.9		 Vp

Figure 3.



The maximum gain is adjustable between 42 and 54dB with Rgt value:

$$Gtl = 20\log\left(820 \cdot \frac{RZ\,//\,RL}{Rgt\,//\,50K}\right)$$

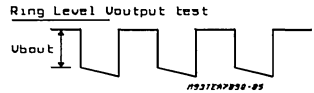
RL = line load impedance

RECEIVE CHARACTERISTICS (T_{amb} = 25°C; f = 1KHz)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
E_{ff}	Sidetone - Efficiency	Test 4 Vmic = -55dBV I_L = 20mA Rrg1 = 11K Rrg2 = 20K			20	dB
Grec	Gain in Symmetric Mode	Test 6 Rrg1 = 11K Rrg2 = 20K I_L = 20mA Vpin12 = -12dBV	1	2	3	dB
ΔGrec	Gain Variation	Test 6 Rrg1 = 11K Rrg2 = 20K 20mA < I_L < 50mA -32dBV < Vpin12 < -12dBV	-0.5		0.5	dB
Dr	Distortion	Test 7 Asymmetric output use Rear = 300 Vear = -16dBV Vear = -12dBV I_L = 20mA Test 6 Symmetric output use Rear = 300 Vear = -10dBV Vear = -6dBV I_L = 20mA		 1 2 1 2	 2 5 2 5	 % % % %
Nr	Noise	Test 6 Rear = 300 I_L = 20mA		 -75		 dBmp
Mear	Earphone Mute	Test 6 Vpin12 = -12dBV	60			dB
Zout	Output Impedance				40	Ω

RING CHARACTERISTICS (T_{amb} = 25°C; f = 1KHz)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Ringer	Test 8				
$V_{Thri\ ON}$	- Ringing Threshold Voltage	RI active	15		20	V
$V_{Thri\ OFF}$		Ri inactive		8	9	V
I_{Ring}	Internal Consumption in Ring Mode	VRING = 10V		1	1.2	mA
V_{RMC}	Microprocessor Supply Voltage		3.7	4	4.3	V
t_{ron}	- Rise time	I_{ring} = 10mA			100	ms
V_{Ring}	- Internal Zener Voltage		24	26	29	V
Vbout	- Buzzer V_{out}	Level Code (011111)	23	25	28	Vpp
		Level Code (011110)	9	11	13	Vpp
	Freq = 1312Hz	Level Code (011101)	3	4.5	6	Vpp
	Freq. Code 001111	Level Code (011100)	0.5	1	2	Vpp
F1	-3 tone ring melody	Freq. Code (000000)		822		Hz
F2		Freq. Code (001101)		1074		Hz
F3		Freq. Code (001111)		1312		Hz
	- Ring Frequency Accuracy		-0.4		0.4	%

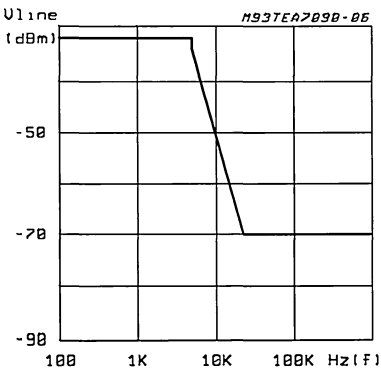


DTMF GENERATOR (T = 5 to 55°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Amf	- Tone Frequency Accuracy	Test 5 For all parameters H = 1.79MHz I_L = 20mA	- 0.4		0.4	%
Llf	- LF Group line level		-12	-10.5	-9	dBm
Lhf	- HF Group line level		-10	-8.5	-7	dBm
Pmf	- Preemphasis HF/LF		+1	+2	+3	dB
Cmf	- DTMF Confidence tone:					
	Earphone level (low freq.)		13	17	21	mV
	Earphone level (high freq.)		17	22	27	mV
–	- Unwanted frequency level (see Fig 4)		–	–	–	–

Note: LF = Low Frequency
HF = High Frequency

Figure 4: Unwanted Frequency level in DTMF



MICROCONTROLLER INTERFACE WITH TEA7090

All inputs can be driven by a Low level max. of 0.1 x VRMC and a high level min. of 0.9 x VRMC.

All inputs except OSC (pin 22) have an internal pull-up resistor (120K).

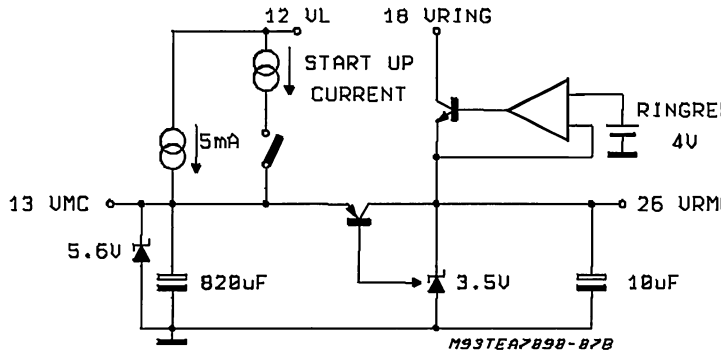
Steady state for OSC at low level is forbidden.
All outputs can drive a ± 1mA typical.

Power Supply

The microcontroller is power supplied by a 3.5V regulated supply **(VRMC)** and by an unregulated power supply (VMC).

The two supplies are connected through a serial regulator. The unregulated power supply (VMC) has a DC voltage equal to: **Vpin12 – 0.6V** and must be lower than 6V.

Figure 4.



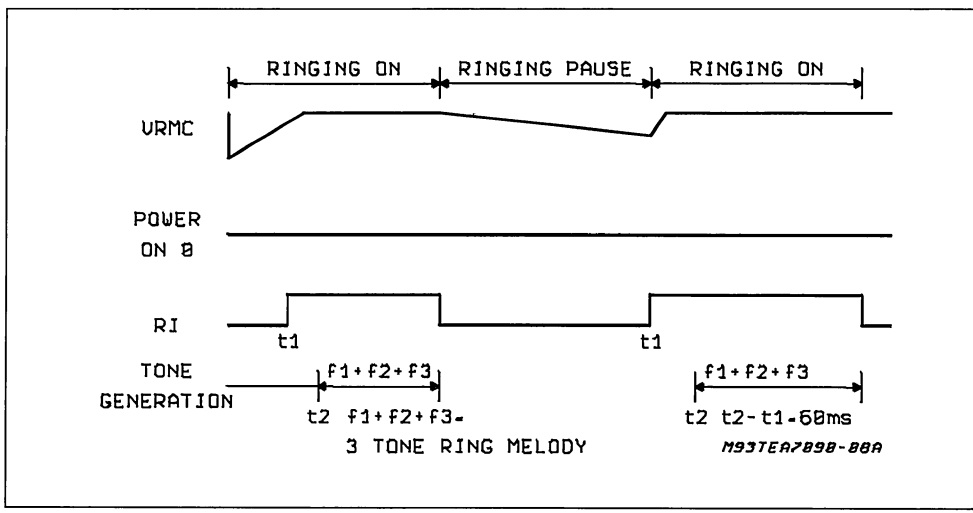
In ring mode, only the 10µF connected on pin VRMC is power supplied.

Ring Indicator Output (RI)

Ri is active with more than 18V on VRING (with internal Hysteresis of 10V) and when VRMC is higher than 3.15V. (0.9 x Final value).

As soon as the microcontroller receives this signal, it can send the digital code for the output level and the ringing melody on the ring signal output.

Figure 5: Timing.



During the delay t2-t1, the microcontroller can analyse the line ring frequency and then sends to the serial data input the code corresponding to the chosen ringing output level.

Power on

P_{ON} is active when the line current is present and the voltage is higher than 3.15V on V_{RMC}. (0.9 x Final Value).

NOTE:
During the break period in the pulse and Flash mode and during the exchange line break, the Power on signal is going to low level. Maximum delay for Pon decay edge after I_{Line} goes to zero is 50ms (with Cpin8 = 47µF, Cpin11 = 1µF, Cpin27 = 10µF).

Figure 6: Timing HOOK OFF/HOOK ON

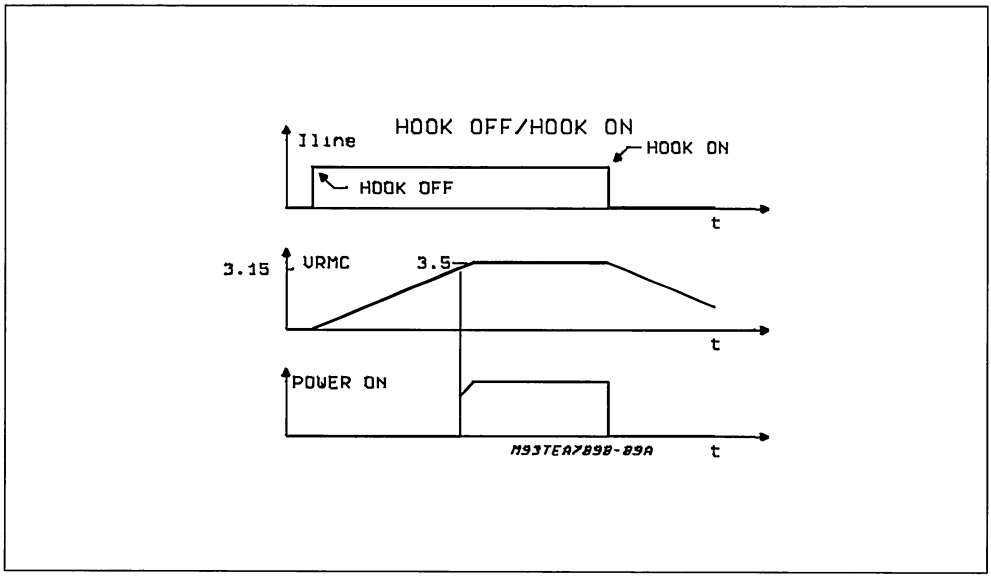
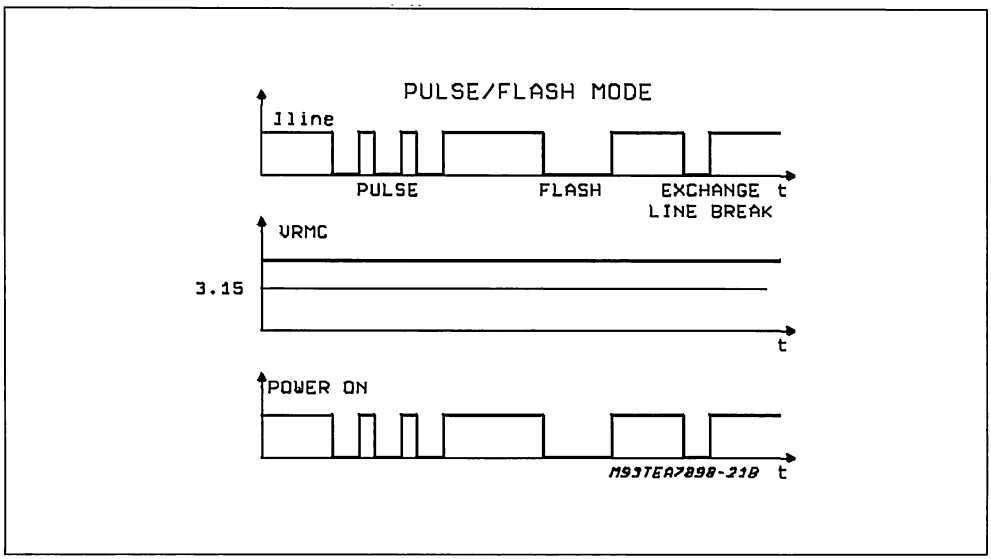


Figure 7: Timing PULSE/FLASH MODE



Reset

RESET is active in speech on the first positive edge of PON and then remains high until VRMC decreases below 3.15V (0.9 x final value) or the RESET code is received. In Ring, RESET is identical to RI output.

NOTE: For complete timing information on reset code use, see TEA7090+ST6292 App. Note.

Figure 8: Timing PULSE/FLASH MODE

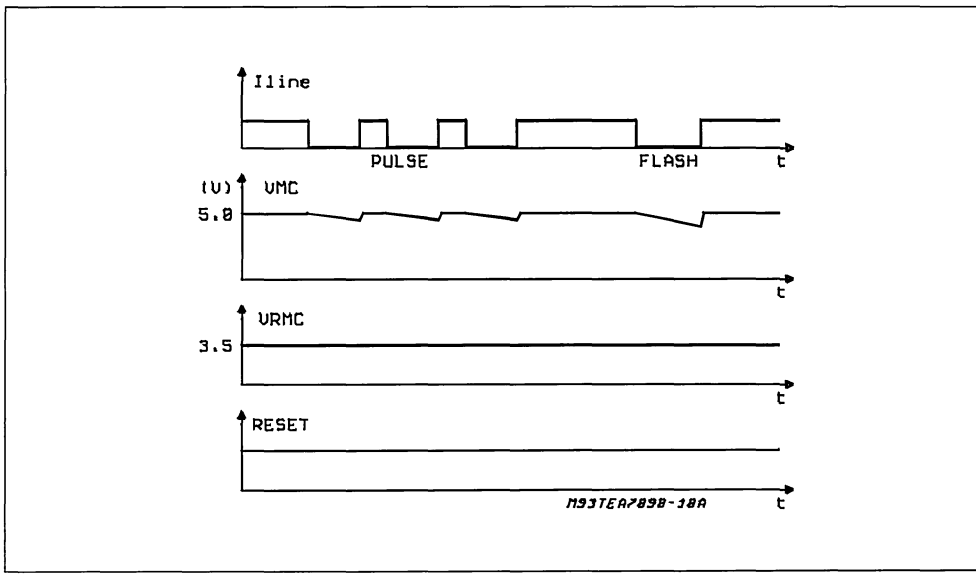
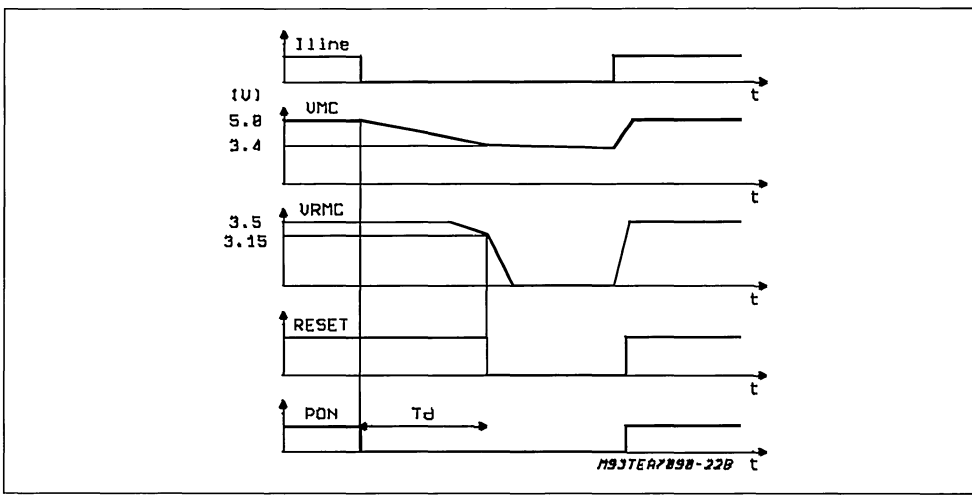


Figure 9: Timing Without Use Microcontroller Reset Code Control



TD is fixed by the VMC value, C10 on VMC, and the ST6 current consumption.
Example: V_{MC} = 5V, C_{10} = 470µF, $I_{ST6+\ TEA7090}$ = 450µA ⇒ T_D = 1.67s by this way the TEA7090+ ST6 drive a long ground key duration.

Figure 10: Timing Exchange Line Break with the Microcontroller

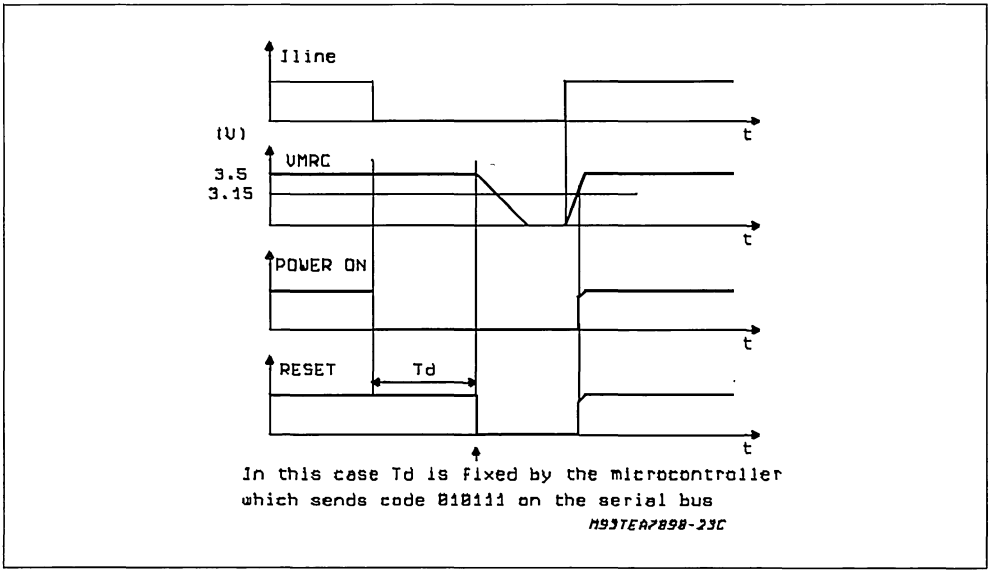
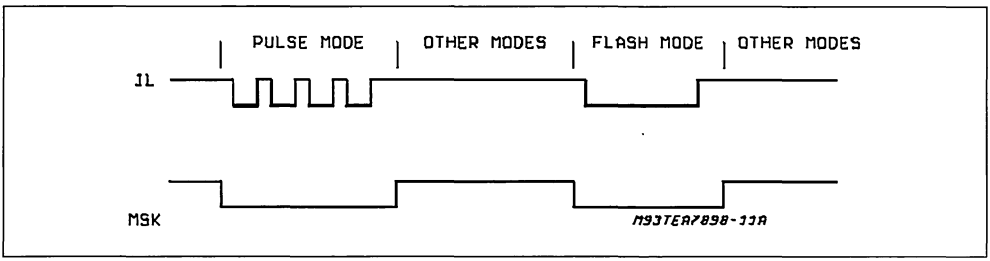


Figure 11: Timing.



Mask input (MSK)

MSK input must be high by default (fig 11).
In speech configuration forcing MSK input to low level will have same functionality than the MASK code.

For Ring mode when it is necessary to send other frequencies than the 8 basic ones, this input allows to drive the buzzer output.

Serial byte interface (Data and clock)

This two wires bus is a 6 bit one. The TEA7090 is only using the 5 last bits. In other SGS-THOMSON integrated circuits the 6 bits codes are used. The common codes are compatible between the different circuits.

There are different kind of codes on the serial bus

– The DTMF and ring frequency codes

– The mode codes:
  - Dialling
  - Speech
  - Mute
  - Ring

– The configuration codes:
  - Mask/No Mask
  - Normal gain/Normal gain +6dB, on receive channel

– The 4 ring levels codes

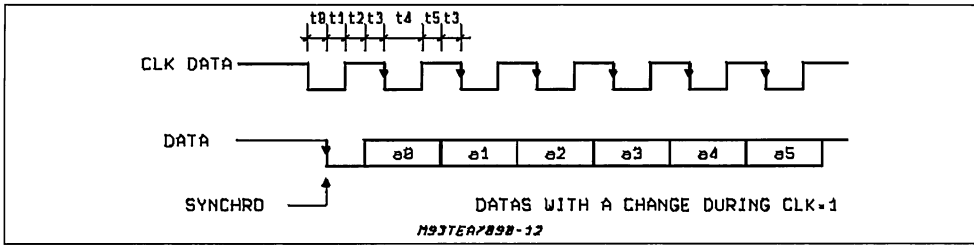
– The Reset code

6 bit codes (fig 12)

t0, t1, t2, t3, t4, t5 must be greater than 1µs.

During interbyte, clock and data line have to be at a high level. The byte must be considered active on the last (seventh) positive edge on **DCL (pin 25)**. The data transition has to occur only when DCL = 1.

Figure 12: Timing.



FUNCTIONALITY DESCRIPTION

Each part of the serial interface can be separated in blocks of functionalities.

There are three kind of blocks.

- The single code blocks (MASK, +6dB) are toggle codes. Their default configurations are **NoMask** and **Normal** on Receive Channel.
- The Reset control can be sent only once. Only positive edge Pon, derived on opening and closing the line, is forcing the default mode again.

NOTE: This code is only active in speech configuration.

- The multi-codes blocks (DTMF + Ring frequencies, Mode, Ring level) have exclusive codes. That means at one time inside a block, only one code is active. As one new code is sent, the previous code is cancelled. The default configuration for DTMF (or Ring) is 000000. For Mode block it is speech (010000) and for Ring level block it is the minimum level (011100).
- Between two DTMF/RING frequencies, introducing a Mute or speech code implies to wait 1ms to end the sinwave or square period.

Note: For Ring it's allowed to send two frequency codes without a Mute one.

Codes						Keyboard	Remarks	
a5	a4	a3	a2	a1	a0			
0	0	0	0	0	0	"2"	1336 Hz + 697 Hz	IN DTMF DIALLING
0	0	0	0	0	1	"1"	1209 Hz + 697 Hz	
0	0	0	0	1	0	"A"	1633 Hz + 697 Hz	
0	0	0	0	1	1	"3"	1477 Hz + 697 Hz	
0	0	0	1	0	0	"8"	1336 Hz + 852 Hz	
0	0	0	1	0	1	"7"	1209 Hz + 852 Hz	
0	0	0	1	1	0	"C"	1633 Hz + 852 Hz	
0	0	0	1	1	1	"9"	1477 Hz + 852 Hz	
0	0	1	0	0	0	"5"	1336 Hz + 770 Hz	
0	0	1	0	0	1	"4"	1209 Hz + 770 Hz	
0	0	1	0	1	0	"B"	1633 Hz + 770 Hz	
0	0	1	0	1	1	"6"	1477 Hz + 770 Hz	
0	0	1	1	0	0	"0"	1336 Hz + 941 Hz	
0	0	1	1	0	1	"*"	1209 Hz + 941 Hz	
0	0	1	1	1	0	"D"	1633 Hz + 941 Hz	
0	0	1	1	1	1	"#"	1477 Hz + 941 Hz	
0	0	0	0	0	0		822 Hz ring signal	IN RING MODE
0	0	0	0	0	1		744 Hz ring signal	
0	0	0	0	1	0		1005 Hz ring signal	
0	0	0	0	1	1		909 Hz ring signal	
0	0	1	1	0	0		1187 Hz ring signal	
0	0	1	1	0	1		1074 Hz ring signal	
0	0	1	1	1	0		1451 Hz ring signal	
0	0	1	1	1	1		1312 Hz ring signal	
0	1	0	0	0	0		Speech mode	
0	1	0	0	0	1		Dialling mode or ring start	
0	1	0	0	1	0		Earphone & Microphone mute	
0	1	0	0	1	1		Microphone mute	
0	1	0	1	0	1		Mask/No Mask	
0	1	0	1	1	0	"+6dB"	Normal/+6dB on Receive channel	
0	1	0	1	1	1		Reset control	
0	1	1	1	0	0		Minimum ring level (level 1)	
0	1	1	1	0	1		Intermediate ring level (level 2)	
0	1	1	1	1	0		Intermediate ring level (level 3)	
0	1	1	1	1	1		Maximum ring level (level 4)	

Figure 13: Test1 Circuit (VL/IVRMC/VRMC/IVMC/ILS)

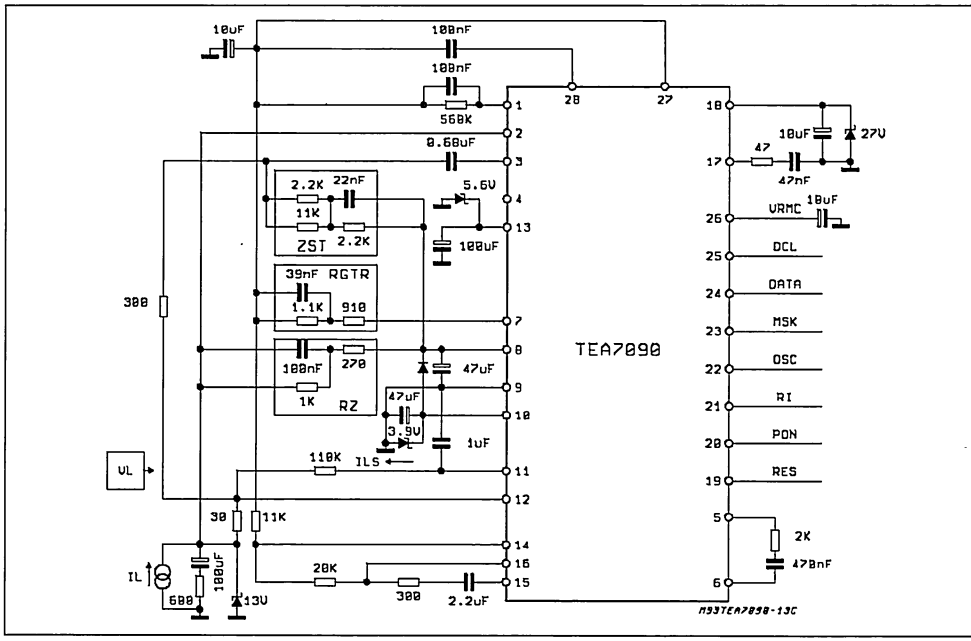


Figure 14: Test2 Circuit RL

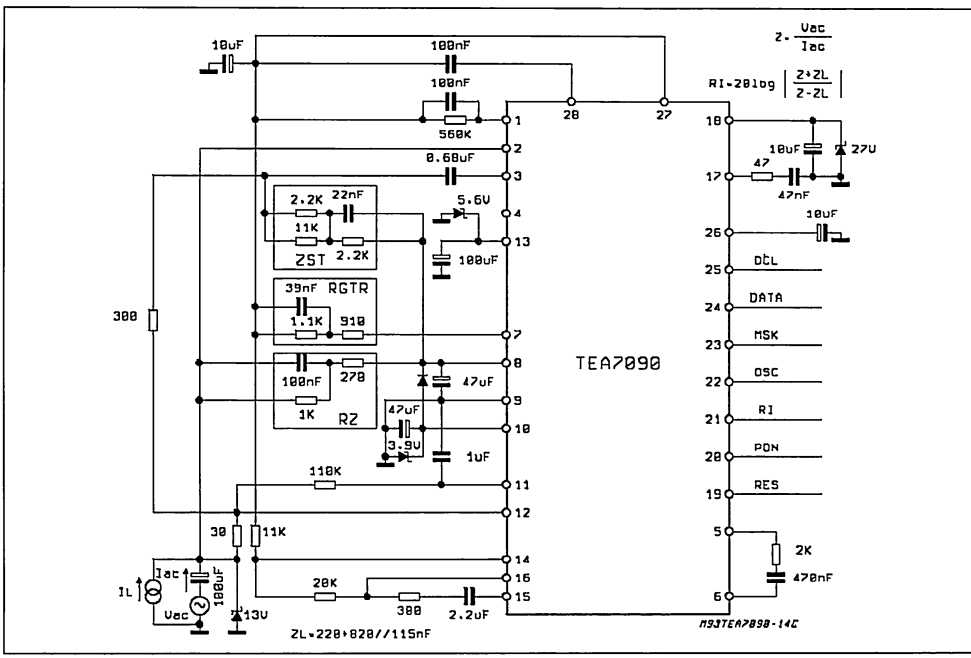


Figure 15: Test 4 (Gtr/Zmic/Nt/Mmic/Dt/Vlmax/Eff)

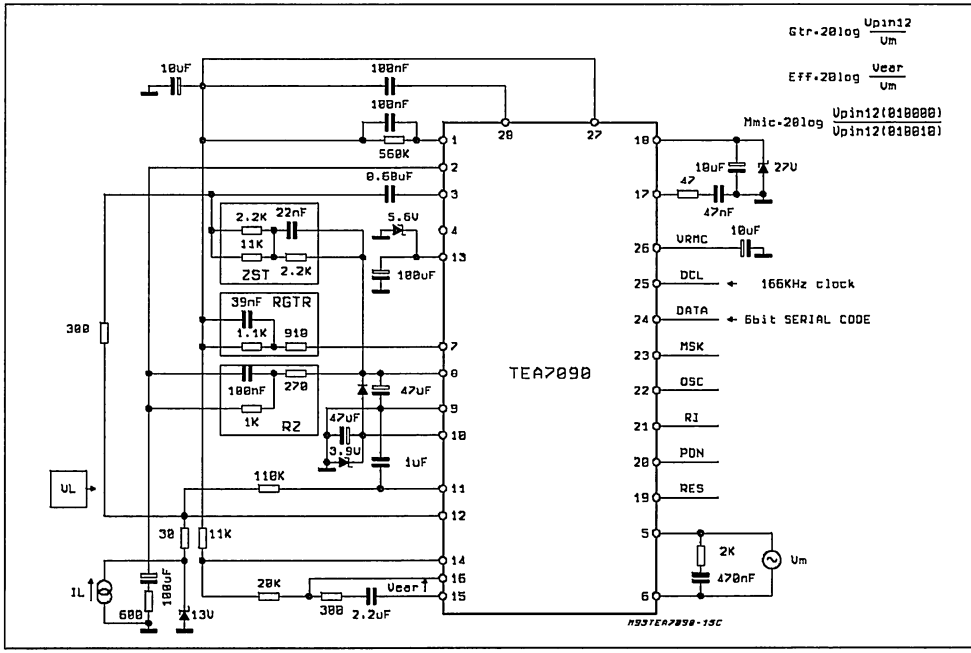


Figure 16: Test5 Circuit DTMF

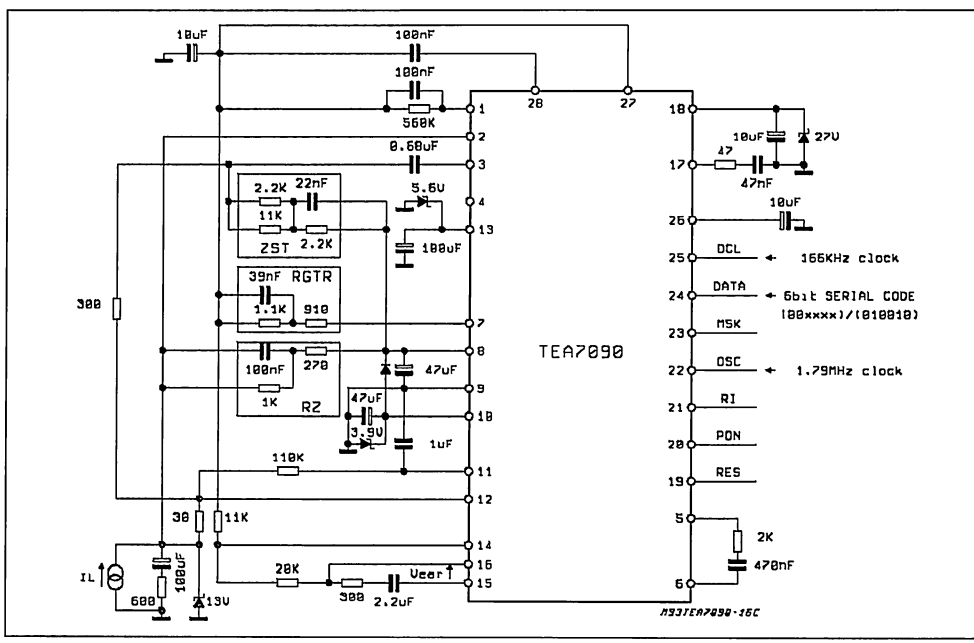


Figure 17: Test6 Crcuit(Grec/Dr/Mear)

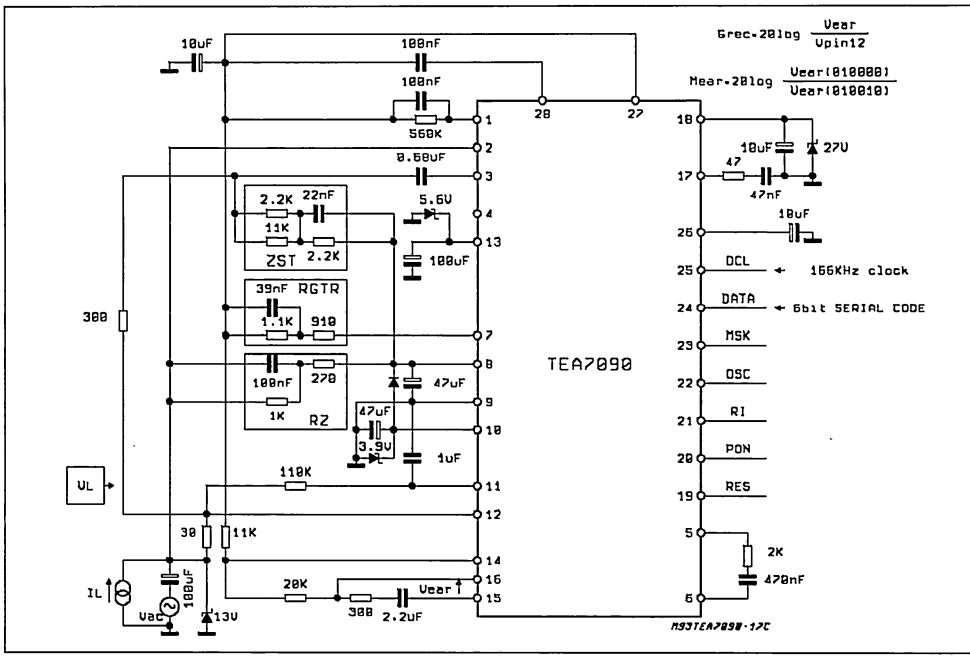


Figure 18: Test7 Crcuit(Dr/Nr)

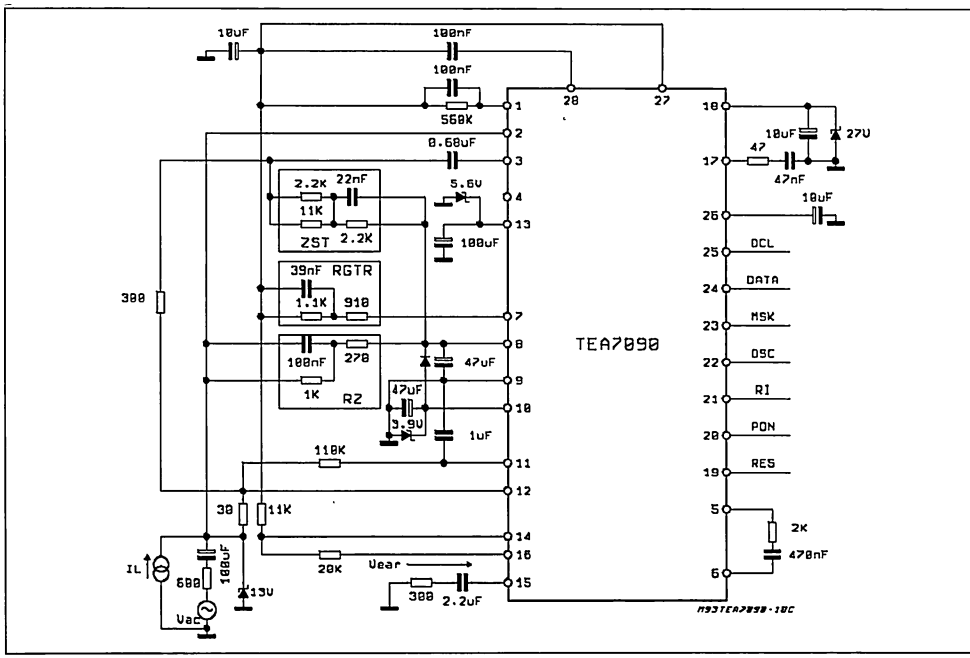


Figure 19: Test 8a Circuit Vthri

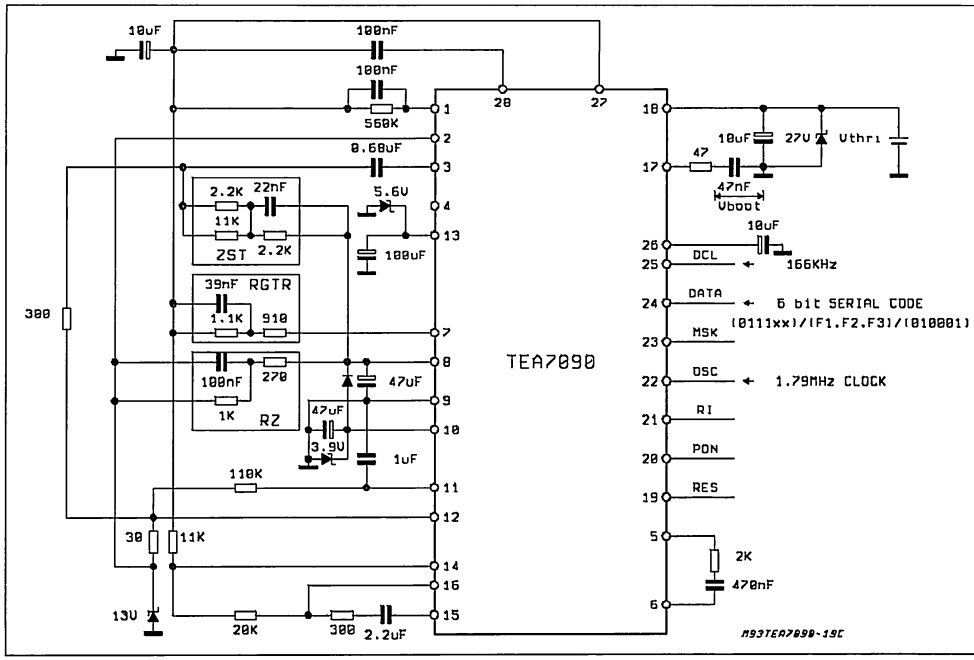
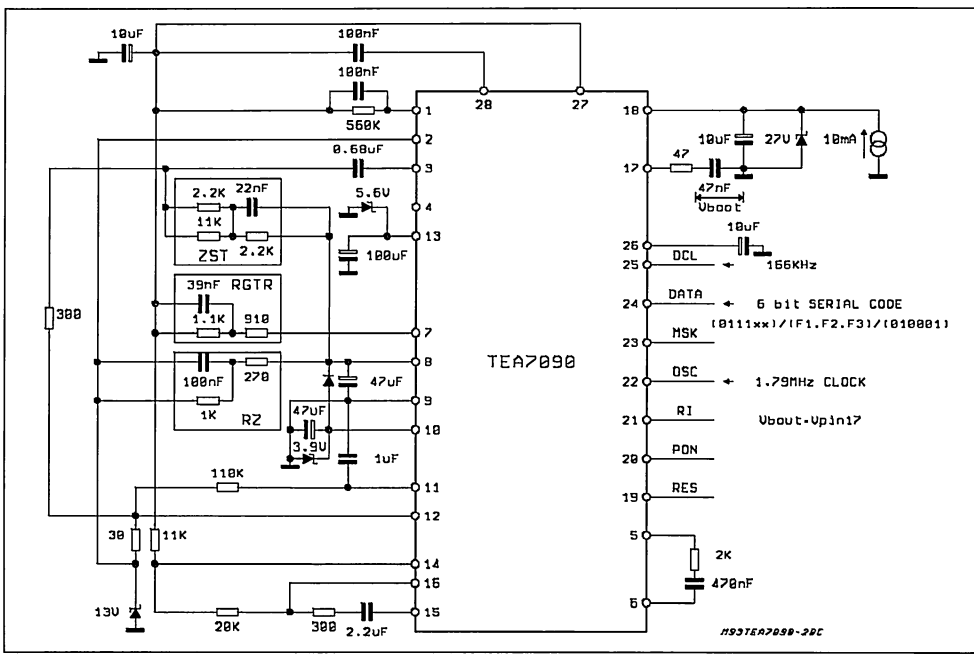


Figure 20: Test 8b Vbout



SGS-THOMSON MICROELECTRONICS

TEA7091

TELEPHONE ANALOG FRONT END

PRODUCT PREVIEW

FEATURES:

SPEECH

- DC LINE CURRENT RANGE FROM 6 TO 110mA
- Tx AND Rx GAIN EXTERNALLY ADJUSTABLE
- AGC IN Tx AND Rx EXTERNALLY PROGRAMMABLE
- AGC DISABLEABLE THROUGH MICROCONTROLLER BUS
- SINGLE/DOUBLE SIDETONE NETWORK SOFTWARE PROGRAMMABLE
- SOFTCLIPPING ON Tx CHANNEL
- SQUELCH TO REDUCE Tx NOISE ENVIROMENT AND TO IMPROVE HOWLING IMMUNITY IN LOUDHEARING MODE
- RECEIVING AMPLIFIER FOR PIEZO OR ELECTRODYNAMIC TRANSDUCERS
- +6dB MODE ON Rx CHANNEL (SELECTABLE THROUGH MICROCONTROLLER BUS)
- –6dB MODE ON Tx CHANNEL (SELECTABLE THROUGH MICROCONTROLLER BUS)
- FREQUENCY GENERATOR FOR WAITING MELODY
- ERROR BEEP GENERATOR
- HOLD LINE CURRENT DETECTOR FOR TRANSFER/ AUTO RELEASE

GROUP LISTENING / ON-HOOK DIALING

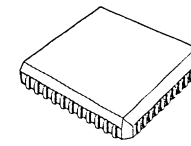
- ANTI HOWLING WITH ACOUSTIC FEEDBACK SYSTEM COUPLED WITH SQUELCH
- DIGITAL VOLUME CONTROL (8 STEPS OF 4dB EACH) THROUGH MICROCONTROLLER BUS
- ANTILARSEN ATTENUATION (4 DIFFERENT LEVELS) PROGRAMMABLE THROUGH MICROCONTROLLER BUS

HANDSFREE INTERFACE

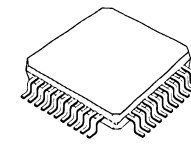
- PIN AND SOFTWARE FACILITY FOR EASY INTERCONNECTION WITH HANDSFREE CONTROLLER IC.

RING ON LOUDSPEAKER

- EMBEDDED SWITCH MODE POWER SUPPLY TO FEED THE LOUDSPEAKER AMPLIFIER DURING RING MODE
- DIGITAL VOLUME CONTROL (8 STEPS OF 4dB EACH) THROUGH MICROCONTROLLER BUS
- RING FREQUENCY GENERATOR PROGRAMMED THROUGH MICROCONTROLLER BUS



PLCC44



PQFP44

DIALLING

- DTMF GENERATOR (CONTROLLED BY MCU BUS)
- DC MASK VALUE DURING MAKE PERIOD PROGRAMMABLE THROUGH MICROCONTROLLER BUS

MICROCONTROLLER INTERFACE

- STABILIZED VOLTAGE FOR MICROCONTROLLER
- 2 WIRE SERIAL BUS
- RING INDICATOR
- POWER-ON SIGNAL
- RESET SIGNAL
- LINE CURRENT VARIATION INDICATOR

SELF BIASED LOUDSPEAKER AMPLIFIER FOR ANSWERING MACHINE

DESCRIPTION

The TEA7091 is a Telephone set Analog Front End (TAFE) interface intended for use in conjunction with a microcontroller.
In this configuration the TEA7091 provides a worldwide mid-range telephone set with loudhearing on board and melody ringer on loudspeaker.
Repertory dialer (memory on MCU) and various features (HOLD, Tone/Pulse, Flash, MUTE, adjustable Ringer and Loudhearing levels..) are programmable by MCU.

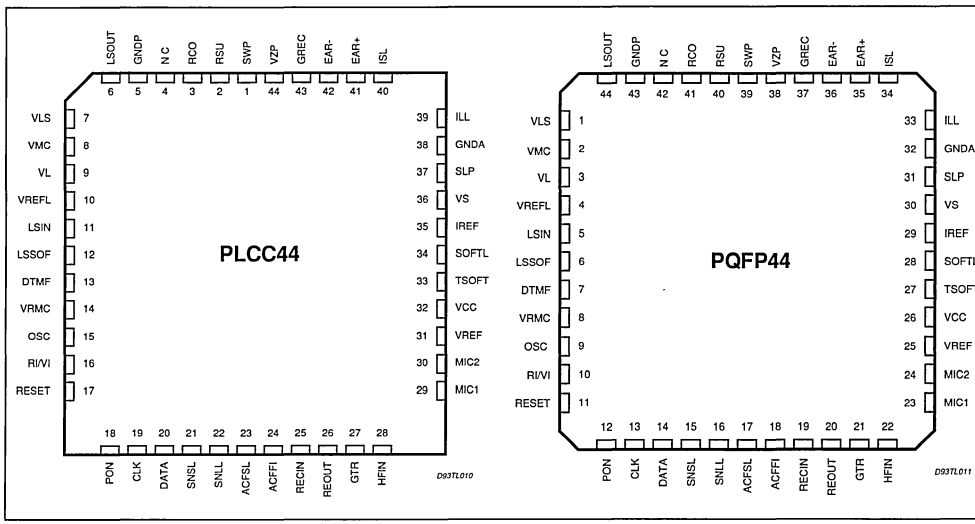
Also high-range telephone set can be built around TEA7091 by adding Handsfree controller (TEA7540), Electronic Hook Switch and upgraded MCU (ST family) with LCD driver.

The concept using TAFE + Microcontroller is called BICHIP approach.
The benefits of this concept are:

- Saving of external components.
- Easy upgrade of the features (extra memories, LCD driver, Answering machine or Cordless interface..) through microcontroller.
- Replacement of configuration switches (PABX /Public, Tone/Pulse...) by EEPROM settings.

This also induces reliability and cost improvement.

PINS CONNECTION (Top views)



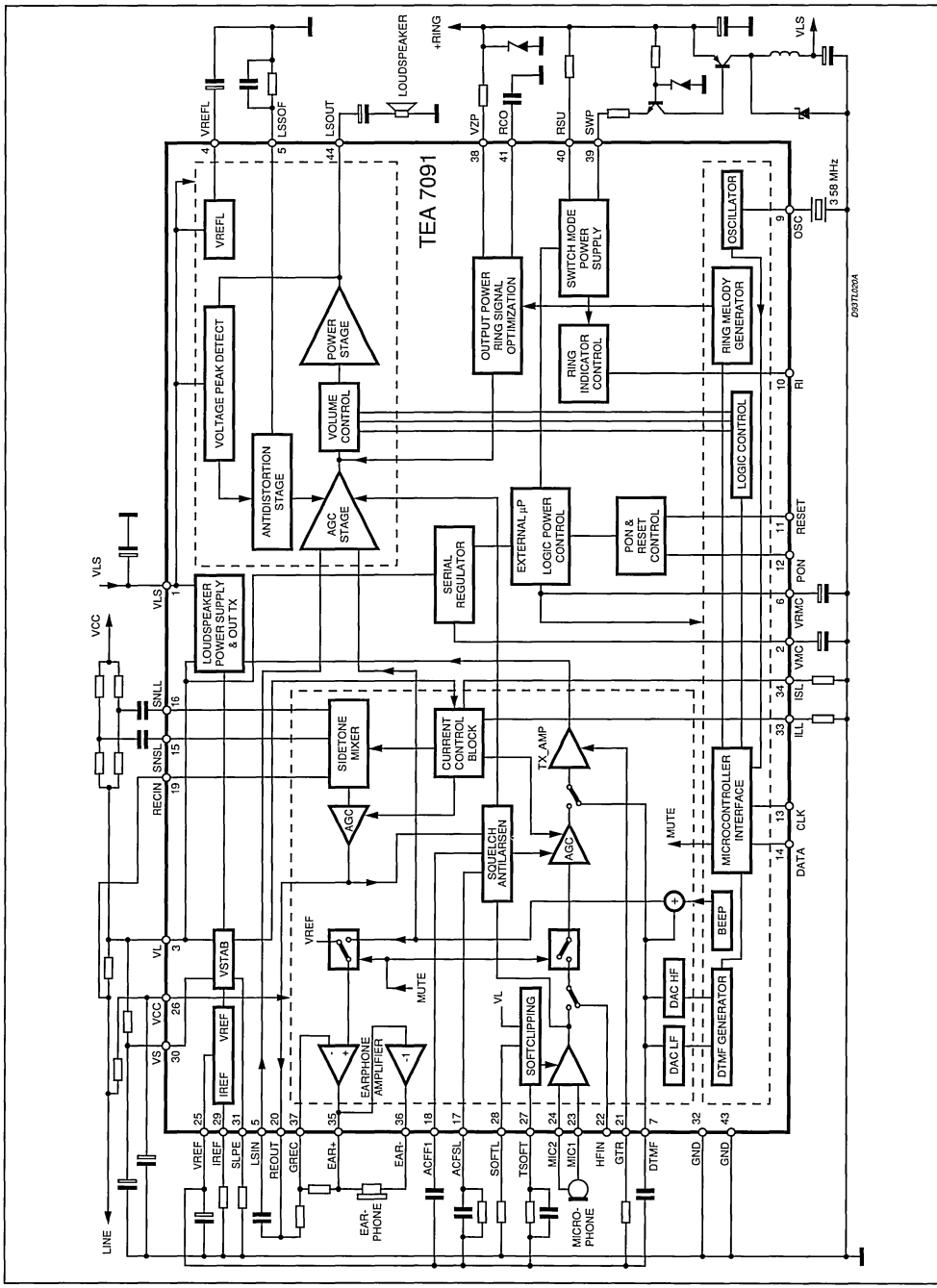
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{op}	Operating Temperature	– 25 to +70	°C
T_{stg}	Storage Temperature	– 55 to +150	°C
V_{LM}	Supply Voltage (pin 3)	12	V
I_{LM}	Supply Current	150	mA
V_{REGM}	CMOS part supply (Pin 8)	6	V
T_j	Junction Temperature	– 25 to +150	°C

PIN DESCRIPTIONS

PQFP44 N° Pins	PLCC44 N° Pins	Names	Functions
1	7	VLS	Loudspeaker power supply.
2	8	VMC	Unregulated microcontroller supply.
3	9	VL	Line voltage.
4	10	VREFL	Loudspeaker reference voltage.
5	11	LSIN	Loudspeaker input.
6	12	LSSOF	Loudspeaker softclipping time constatnt.
7	13	DTMF	DTMF filter.
8	14	VRMC	Stabilized microcontroller supply.
9	15	OSC	Oscillator input.
10	16	RI/VI	Ring indicator / Line current variation indicator.
11	17	RESET	Microcontroller reset.
12	18	PON	Power on output.
13	19	CLK	Clock data input.
14	20	DATA	Data Input.
15	21	SNSL	Short line sidetone input.
16	22	SNLL	Long line sidetone input.
17	23	ACFSL	Anti-acoustic feedback and squelch peak voltage.
18	24	ACFFI	Anti-acoustic feedback and squelch filter.
19	25	RECIN	Receiving Input.
20	26	REOUT	Receive output.
21	27	GTR	Transmit gain adjustment.
22	28	HFIN	Handsfree microphone input.
23	29	MIC1	Microphone input.
24	30	MIC2	Microphone input.
25	31	VREF	Transmit and receive reference voltage (VCC/2).
26	32	VCC	Transmit and receive power supply.
27	33	TSOFT	Transmit soft-clipping time constant.
28	34	SOFTL	Maximum AC signal (Softclipping threshold).
29	35	IREF	Internal reference current.
30	36	VS	Shunt regulator capacitor.
31	37	SLP	DC mask slope.
32	38	GNDA	Analog Ground (signal).
33	39	ILL	Line current regulation start up.
34	40	ISL	Line current regulation stop.
35	41	EAR+	Positive earphone output.
36	42	EAR–	Negative earphone output.
37	43	GREC	Receive gain adjustment.
38	44	VZP	Switch mode power supply internal zener.
39	1	SWP	Switch mode power supply output.
40	2	RSU	Ring start up level.
41	3	RCO	Ring capacitor optimization (output power).
42	4	N.C.	Not Connected.
43	5	GNDP	Power Ground.
44	6	LSOUT	Loudspeaker Output.

Figure 1: Block Diagram.



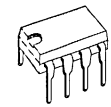
SGS-THOMSON MICROELECTRONICS

TEA7530

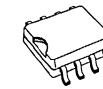
MONITOR AMPLIFIER

PRELIMINARY DATA

- LOW VOLTAGE
- POWER: 100mW AT 5V
- ANTIDISTORTION SYSTEM FOR LOW CURRENT LINES



MINIDIP



SO-8

ORDERING NUMBERS:

TEA7530DP TEA7530FP

DESCRIPTION

This 8 pins IC is designed for monitor telephone set and provides:

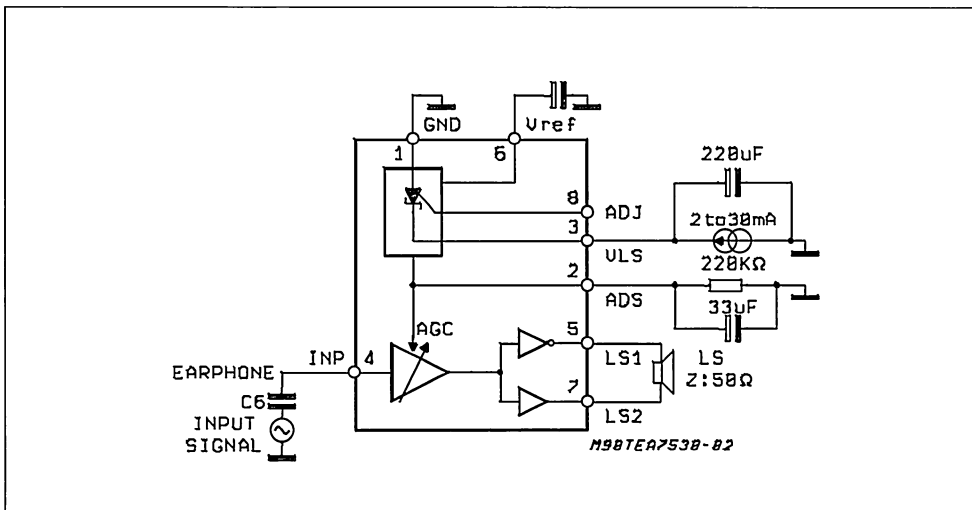
a) Signal amplification for monitoring

b) Antidistortion by automatic gain adaptation.

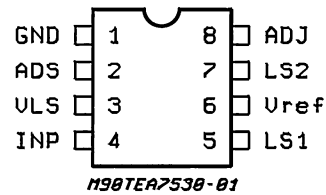
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		Minidip	SO	
T_{op}	Temperature Range	-20 to +70	-20 to +70	°C
V_{LS}	Supply Voltage	6	6	V
I_{LS}	Supply Current for T > 300ms for T ≤ 300ms	90 150	75 120	mA mA

BLOCK DIAGRAM



PIN CONNECTION (top view)



PIN FUNCTION

N°	Symbol	Description
1	GND	Ground
2	ADS	Antidistortion
3	V_{LS}	Supply
4	INP	Input Signal
5	LS1	Output Loudspeaker 1
6	V_{REF}	Internal Reference Voltage
7	LS2	Output Loudspeaker 2
8	ADJ	Adjust Internal Reference V_{LS}

FUNCTIONAL DESCRIPTION

TEA7530 performs the following functions:

The circuit amplifies the incoming signal and feeds it to the loudspeaker.

- The Antidistortion system is incorporated for low current available from line.
- The maximum power available on a 50Ω impedance loudspeaker is 25mW at 3V and 100mW at 5V.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, I_{LS} = 30mA unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{LS1}	V_{LS1} Supply	ILS = 2mA (fig. 5) I_{LS} = 30mA (fig. 5)	2.7	3 3.15	3.3 3.4	V V
V_{LSM}	V_{LS} Maximum	I_{pin8} = 40µA (fig. 5; So = closed)			5.7	V
V_{ADJ}	Voltage Pin 8	I_{LS} = 2 to 30mA (fig. 5	1.0	1.25	1.5	V
G	Loudspeaker Amplifier Gain = $\frac{V_{(5)} - V_{(7)}}{V_{(4)}}$	I_{LS} = 30mA (fig. 6)	30	32	34	dB
THD	Distortion	f = 300Hz to 2KHz $V_{(5)} - V_{(7)}$ = 0.8Vrms; (fig. 6)			2	%
Z_{INPIN}	Earphone Input	(fig. 7)	2.1	2.8	3.5	KΩ
V_{OFFS}	Output Offset [$V_{(5)} - V_{(7)}$]	(fig. 6)	-80		80	mV
GATT	Loudspeaker Attenuated Gain = [$V_{(5)} - V_{(7)}$] / $V_{(4)}$	$V_{(2)}$ = 0.7V; (fig. 8) $V_{(2)}$ = 0.4V; (fig. 8)	 20	-30 30	-20	dB dB

Figure 1: Loudspeaker Gain vs. Voltage on Pin 2

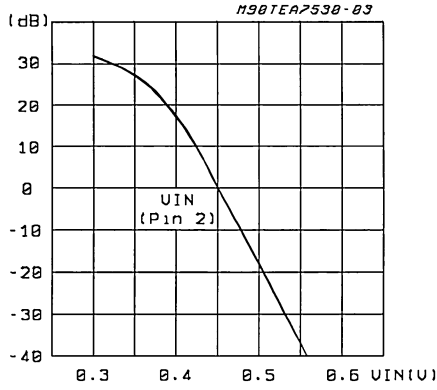


Figure 2: Power Available on Loudspeaker vs. V_{LS} Typical Curve. (Voltage Mode

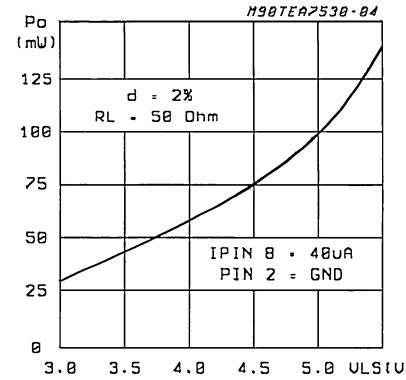


Figure 3: Distortion vs. Output Power

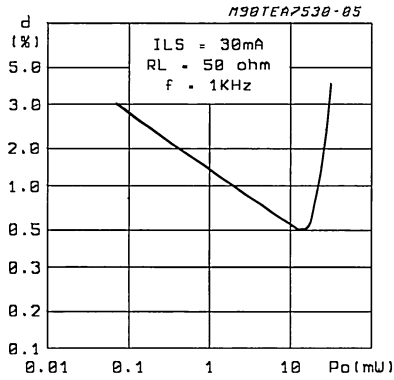
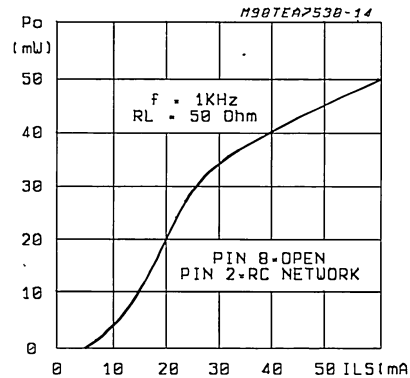


Figure 4: Output Power vs. Supply Current (Current Mode Supply)



TEST CIRCUITS

Figure 5: Shuntvoltage Regulator / Reference Voltage at Pin 8.

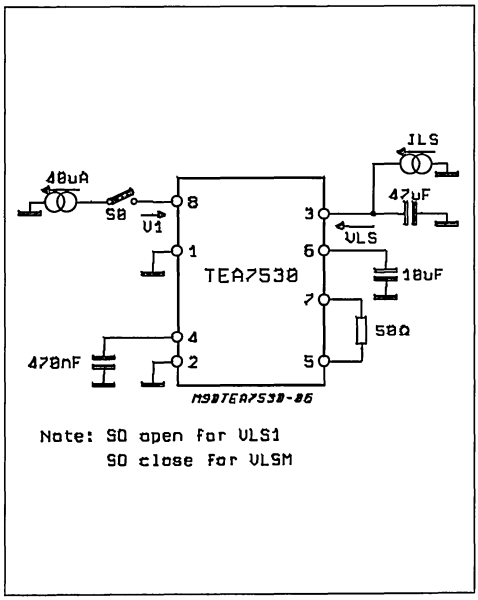


Figure 6: Loudspeaker Amplifier: Gain/Distortion/Output Offset

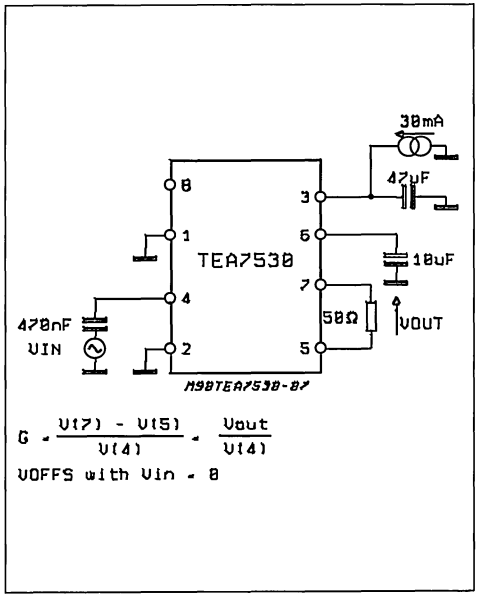


Figure 7: Impedance, ZINP

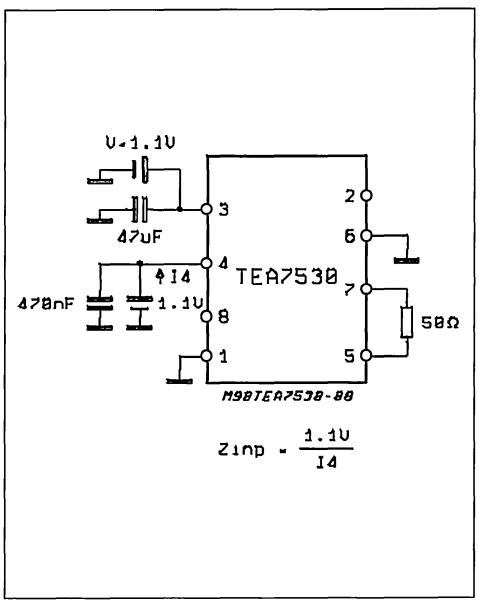
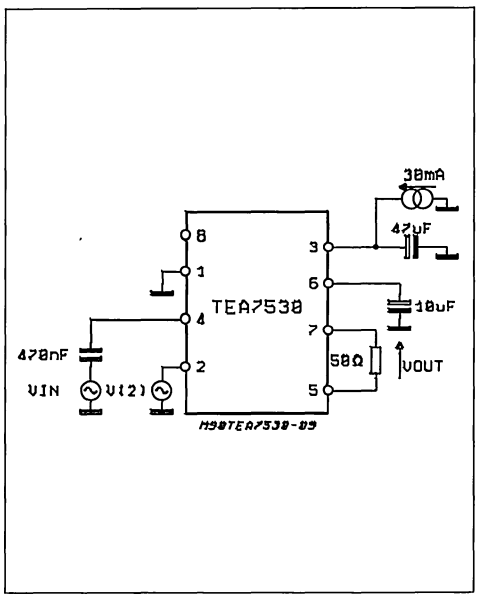


Figure 8: Anti-loading Feedback System at G = GATT



CIRCUIT DESCRIPTION

TEA7530 is a 8 pin DIP integrated circuit providing the following facilities:

- ♦ Loudspeaker amplifier
- ♦ Antidistortion feed-back system (limited line current compensation)

1.1. LOUDSPEAKER AMPLIFIER

The amplifier is divided into 2 main sections.

- Automatic Gain Control (AGC)
- Push-pull amplifier (bridge structure)

a) The AGC section is used for the antidistortion system.

- ♦ When used in a telephone set to avoid larsen effect the AGC automatically decreases loudspeaker amplifier gain.
- ♦ When the required output level exceeds the capabilities of the available current, the AGC decreases the loudspeaker amplifier gain to avoids distortion.

b) The output amplifier uses a double push-pull configuration (H bridge) to get maximum dynamic range under limited supply conditions.

Figure 9

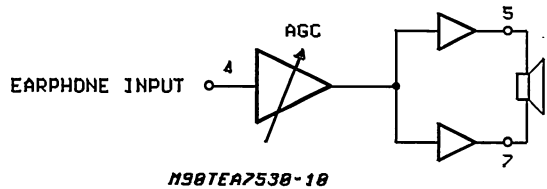
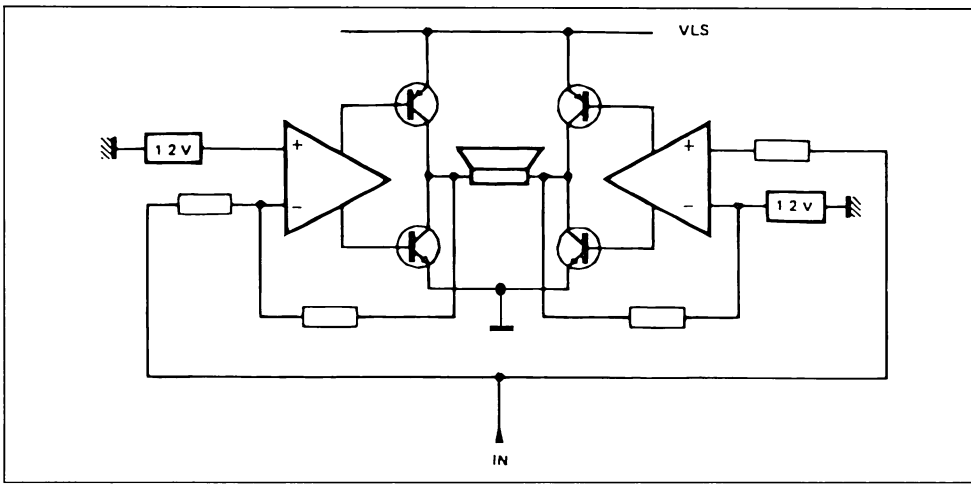


Figure 10



Amplifier DC Supply

In transmission mode, the supply voltage is controlled by the internal shunt DC regulator. For this reason, the TEA7530 should be supplied from a current source (see: supply considerations).
An antidistortion system is embodied which provides AGC control to avoid loudspeaker distortion under current-limited conditions.

AGC Circuit action

When the supply V_{LS} is insufficient, the voltage at pin 8, falls below the reference voltage 1.2V, resulting in transistor (TR) being switched off, resulting zero current flow in resistor R. This state enables the gain control system. Under these conditions, the shunt DC supply will switch at a rate determined by the time constant of the RC network on pin 2.
This switching action accomodates normal speech characteristic under low supply conditions.
The AGC will be switched ON when the level on Pin 2 is greater than a reference voltage of 0.4V.

Supply Considerations

a) Current MODE - Pin 8 is open ($V_{LS} = V_{LS1}$) or connected to ground with an external resistor (R_{ext}) higher than 16KΩ. The typical value of V_{LS} is :

$$V_{LS} = 1.2V \frac{40.5K\Omega + (27K\Omega // R_{EXT})}{(27K\Omega // R_{EXT})}.$$

The AGC section is working as described in the previous paragraph.

b) Voltage MODE - Pin 8 is shorted or connected to GND with a resistor (R_{EXT}) lower than 16KΩ. In this condition the circuit must be supplied with a DC voltage of 3 to 5.5V. In this case the AGC section is permanently ON. Pin 2 must be shorted to GND (in voltage mode only) to avoid permanent attenuation of the signal at audio input

PIN FUNCTIONS

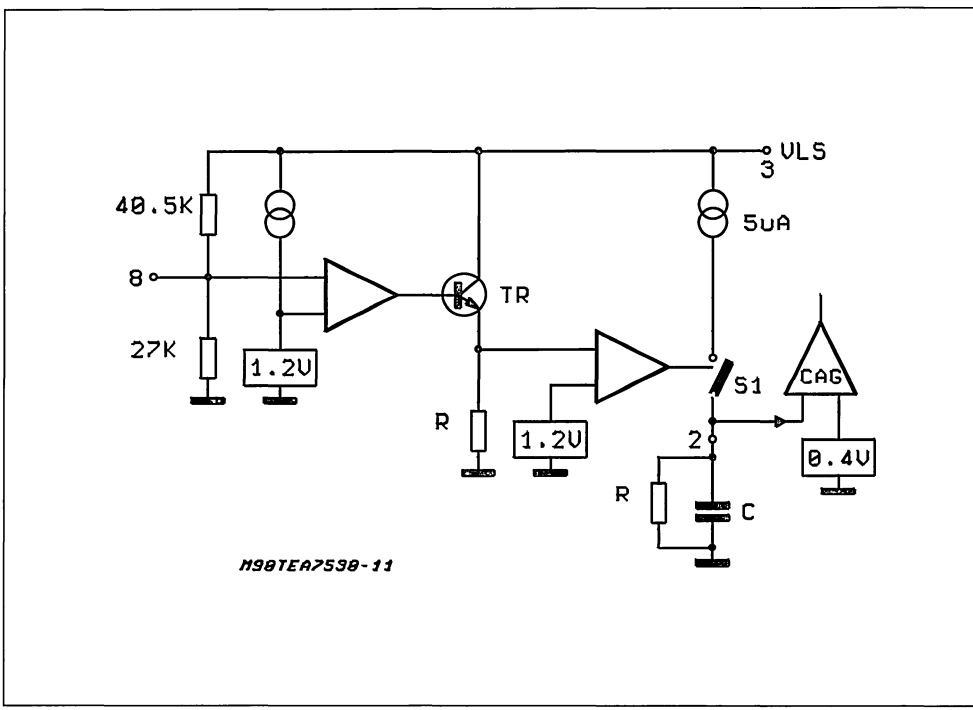
PIN 1: GND.

PIN 2: AUTOMATIC GAIN CONTROL FILTER

The antidistortion system response is adjusted by the R-C network on this pin.

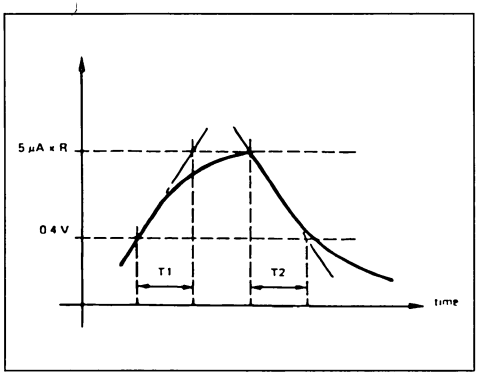
The AGC will be switched ON when the level on pin 2 is greater than a reference voltage of 0.4V, the RC-network charges (current source ON) or discharges (current source OFF) according to supply voltage.

Figure 11



THEORETICAL VOLTAGE ON PIN 2

Figure 12

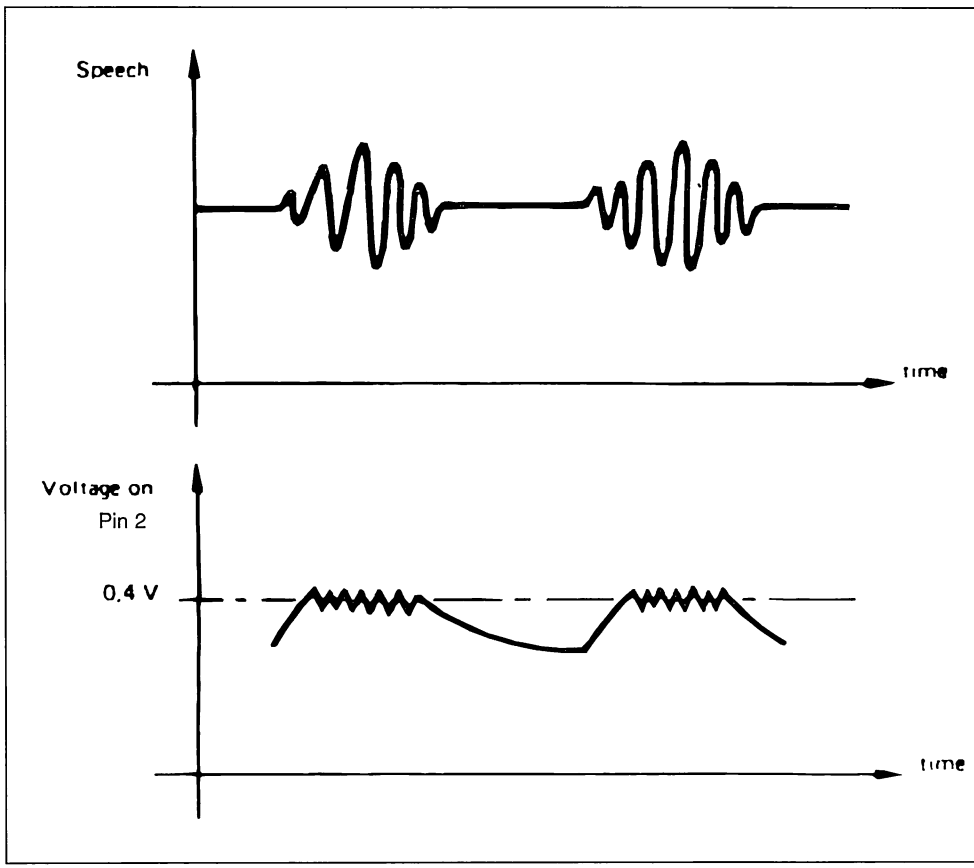


- The value of R affects the system time constant and the charge/discharge duty cycle.
- The value of C only affects the system time constant.
- R should be greater or equal to 150KΩ for correct AGC operation.

PIN 3: CIRCUIT SUPPLY VOLTAGE
With pin 8 open circuit, V_{LS} is internally stabilized at 3V.
When the TEA7530 is under AGC control, the voltage on this pin varies slightly (due to AGC action).

PIN 4: EARPHONE INPUT
Input for loudspeaker signal

Figure 13

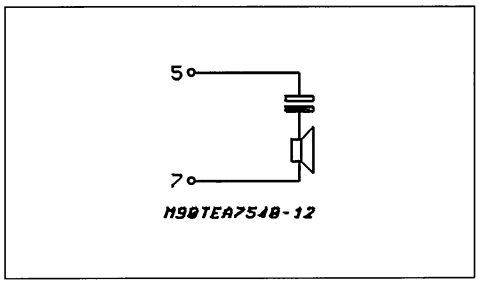


PIN 5-7: LOUDSPEAKER OUTPUTS

Maximum outpt voltage: $V_{pp} = 2V_{LS}$ - 2.5V (with a gain of 32dB).

Maximum output current: depending of the supply current.

Figure 14



Two loudspeaker connection methods are possible, using the amplifier in either symmetrical or asymmetrical mode.

Note:

It is advisable to connect a 47nF capacitor in parallel with the loudspeaker (between pins 5 and 7).

- "Symmetrical" mode

This is for low voltage working, but at a higher supply current. The highest output power is available in this mode, due to the 5.7V maximum supply voltage restriction, imposed by the TEA7530

Loudspeaker impedance recommended value: 50Ω.

Nominal gain available between earphone input and loudspeaker outputs: 32dB.

- "Asymmetrical" Mode

This allows higher voltage operation, but at a lower supply current.

Loudspeaker impedance recommended value: 25Ω.

Nominal gain available between earphone input and loudspeaker output: 32 - 6 = 26dB.

Pin 6: V_{ref}: INTERNAL REFERENCE

Output which provides an internally regulated reference voltage.

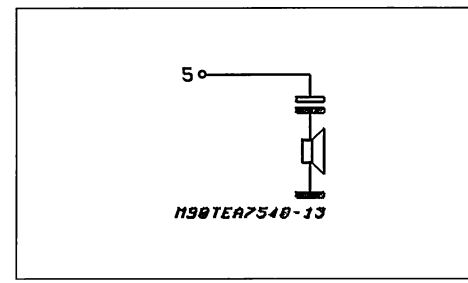
V_{ref} = 1.2V typical

MAXIMUM AVAILABLE CURRENT: 5µA

Pin 8: ADJUST V_{LS}

This pin is used to adjust the IC supply voltage.

Figure 15

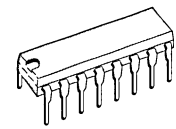


TEA7531

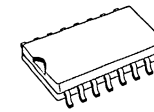
MONITOR AMPLIFIER

REPLACED BY TEA7532 FOR NEW DESIGNS

- PROGRAMMABLE GAIN IN STEPS OF 6dB OR LINEARLY
- ON/OFF POSITION
- LOW VOLTAGE
- POWER: 100mW AT 5V



DIP16



SO16

ORDERING NUMBERS: TEA7531DP (DIP16)
TEA7531FP (SO16)

DESCRIPTION

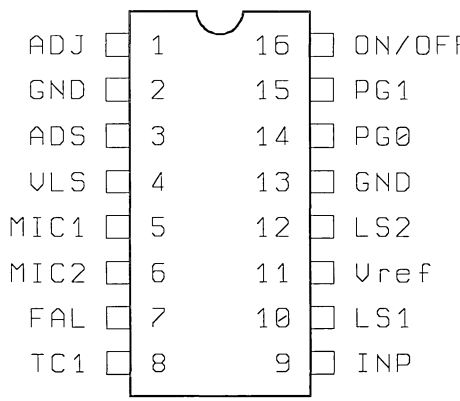
This 16 pins IC is designed for monitor (loudspeaker) telephone set and provides:

a) Signal amplification for monitoring (loudspeaker)

b) Antiacoustic feedback (antilarsen)

c) Antidistortion by automatic gain adaption

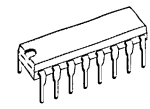
PIN CONNECTION (Top view)



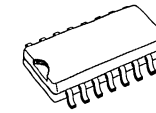
M89TEA7531-01

MONITOR AMPLIFIER

- PROGRAMMABLE GAIN IN STEPS OF 6 dB
- ON/OFF POSITION
- LOW VOLTAGE
- POWER : 100 mW AT 5 V



DIP16



SO16

ORDERING NUMBERS : TEA7532DP (DIP16)
TEA7532FP (SO16)

DESCRIPTION

This 16 pins IC is designed for monitor (loudspeaker) telephone set and provides :

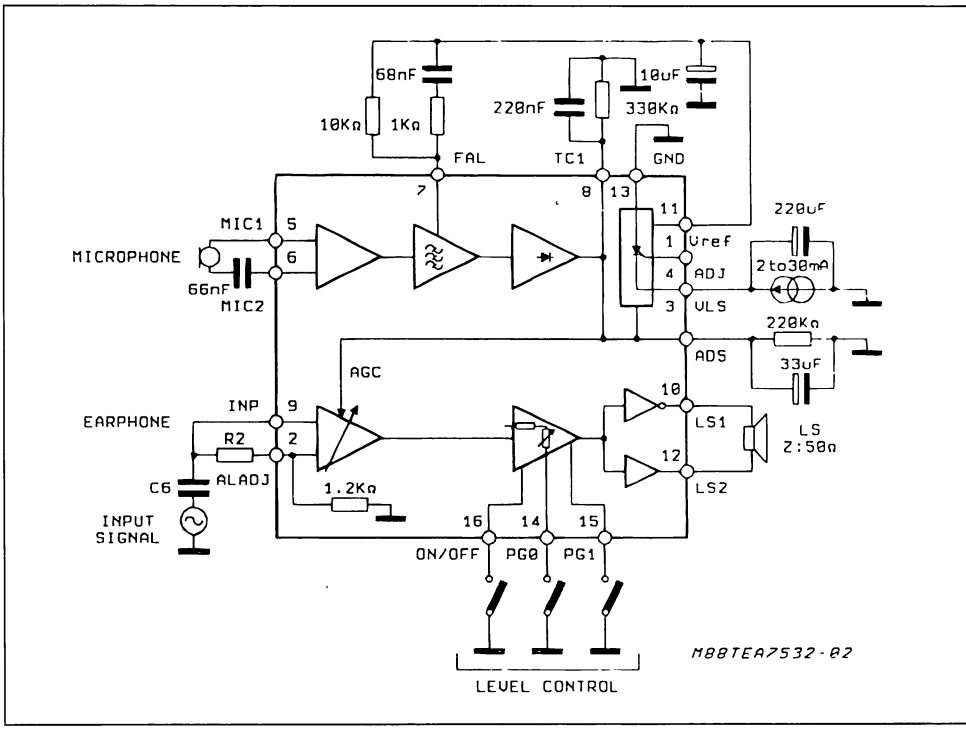
a) Signal amplification for monitoring (loudspeaker)

b) Antiacoustic feedback (antilarsen)

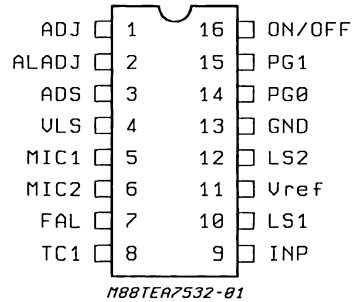
c) Antidistortion by automatic gain adaptation

d) Antilarsen adjustment (full duplex)

BLOCK DIAGRAM



PIN CONNECTION (Top view)



PIN DESCRIPTION

N°	Symbol	Description
1	ADJ	Adjust Internal Reference V_{LS}
2	ALADJ	Antilarsen Adjustement
3	ADS	Antidistortion
4	V_{LS}	Supply
5	MIC1	Microphone Input
6	MIC2	Microphone input
7	FAL	Antilarsen Filter
8	TC1	Antilarsen Time Constant
9	INP	Input Signal
10	LS1	Output Loudspeaker 1
11	V_{REF}	Internal Resistance
12	LS2	Output Loudspeaker 2
13	GND	Ground
14 15 16	PG0 PG1 ON/OFF	Inputs Program Level to Loudspeaker

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{op}	Temperature Range	–5 to + 45	°C
V_{LS}	Supply Voltage	6	V
I_{LS}	Supply Current for T > 300ms for T ≤ 300ms	90 150	mA mA
V_L	Voltage Level (pins, PG0, PG1, on/off)	0.6 > to V_S + 0.6	V

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, I_{LS} = 30mA unless otherwise specified)

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
V_{LS1}	V_{LS} Supply	I_{LS} = 2mA (fig. 7) I_{LS} = 30mA (fig. 7)			2.6	3.0 3.15	3.4 3.4	V V
V_{LSM}	V_{LS} Maximum	$I_{pin\ 1}$ = 50µA (fig. 7 ; So = closed)					5.5	V
V_{ADJ}	Voltage Pin 1	I_{LS} = 2mA to 30mA (fig. 7)			1.1	1.25	1.4	V
G	Loudspeaker Amplifier Gain = $\frac{V_{10} - V_{12}}{V_9}$	ON/OFF	PG0	PG1				
G000		GND	GND	GND	12	14	16	dB
G001		GND	GND	V_{LS}	18	20	22	dB
G010		GND	V_{LS}	GND	24	26	28	dB
G011		GND	V_{LS}	V_{LS}	30	32	34	dB
G100		V_{LS}	X	X		– 30	– 20	dB
THD	Distortion	f = 300Hz to 2kHz, $V_{10} - V_{12}$ = 0.8V_{RMS}, G = G011, (fig. 8)					2	%
G2	[V(10) – V(12)]/V2	P_{G0} = P_{G1} = V_{LS}, V_8 = 0.8V (fig. 8)			30	32	34	dB
Z_{MICIN}	Microphone Input	Symetrical at (pins 5-6) Asymetrical at (pin 6) fig. 9				4.5		kΩ
Z_{INPIN}	Earphone Input	(fig. 9)			2.2	2.8	3.4	kΩ
Z_{IN2}	Antilarsen Adjustment Input				1	1.2	1.45	kΩ
V_{OFFS}	Ouput Offset $[V_{(10)} - V_{(12)}]$	G011 ; (fig. 8)			– 50		50	mV
$I_{ON/OFF}$ I_{PG0} I_{PG1}	Input Current ON State	V_{PG1} = 0V ; (fig. 8)			– 10 – 10 – 10	– 5 – 5 – 5		µA µA µA
$I_{ON/OFF}$ I_{PG0} I_{PG1}	Input Current OFF State	V_{PG1} = V_{LS} ; (fig. 8)					1 1 1	µA µA µA
$V_{IL\ ON/OFF}$ $V_{IL\ PG0}$ $V_{IL\ PG1}$	Input Voltage ON State						0.45 0.45 0.45	V V V
$V_{IH\ ON/OFF}$ $V_{IH\ PG0}$ $V_{IH\ PG1}$	Input Voltage OFF State				1.5 1.5 1.5			V V V
G_{MIC}	Microphone Gain = $V_{(7)}/[V_{(5)} - V_{(6)}]$	V_{MIC} = 10mV_{RMS}, f = 2kHz (fig. 10)			22.5	23.5	24.5	dB
Vg	Voltage Pin 8				0.48	0.67	0.75	V
G_{ATT}	Loudspeaker Attenuated Gain = $[V_{(10)} - V_{(12)}]/V_{(9)}$	G011 ; V_8 = 0.6V ; (fig. 10) G011 ; V_8 = 0.4V ; (fig. 10)			20	– 30 30	– 20	dB dB

FUNCTIONAL DESCRIPTION

TEA7532 performs the following functions :
The circuit amplifies the incoming signal and feeds it to the loudspeaker. PG0 and PG1 inputs are used to set the loudspeaker gain in a range of 32dB to 14dB in 6dB steps.
The TEA7532 inputs (PG0, PG1, ON/OFF) permit the loudspeaker to be cut-off thus ensuring privacy of communication.

- The antilarsen (antiacoustic feedback) system is incorporated.
- The maximum power available on a 50Ω impedance loudspeaker is 25mW at 3 volts and 100mW at 5V.

Limit values for external components :
R3 min = 5 kΩ (R3 adjust VLS), R7 max = 390 kΩ,
R6 min = R7/35
R max between pin 5 and 6 = 10kΩ + C min = 10nF.

Figure 1 : Loudspeaker Gain Versus Voltage on Pin (3) - (8) with Pin 2 Open.

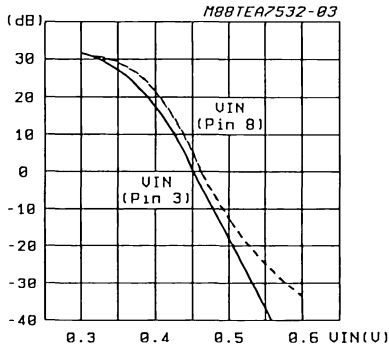
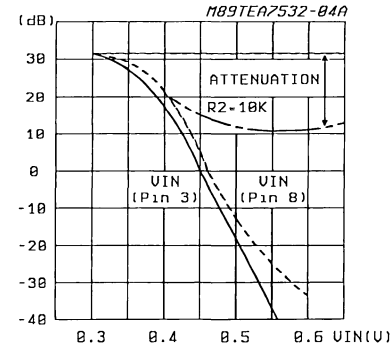


Figure 2 : Loudspeaker Gain Versus Voltage on Pin (3) - (8) and Versus R_2. (*)



(*) ATTENUATION = $\frac{Z_{in2}\ (1.2\ K)}{Z_{in2}\ (1\ 2\ K) + R_2\ (E\ X\ T)}$

$R_2 = 10\ K \Rightarrow ATT = 20\ dB$

$R_2 = 3\ \ K \Rightarrow ATT \approx 10\ dB$

Figure 3 : AC Output Voltage Versus Amplifier Gain.

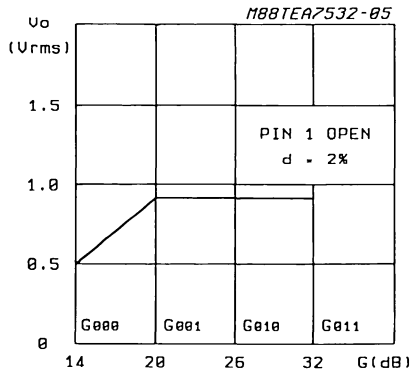


Figure 4 : Power Available on Loudspeaker Versus V_{LS} Typical Curve.

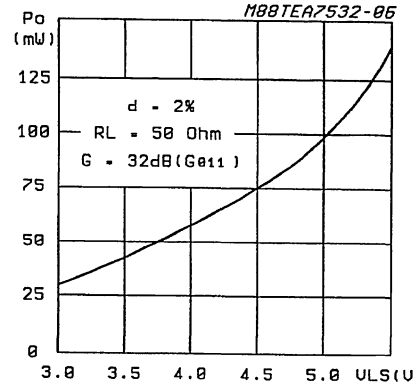


Figure 5 : Distortion Versus Output Power.

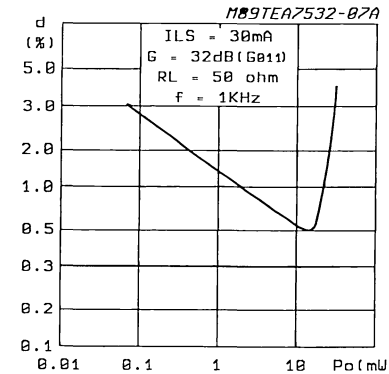
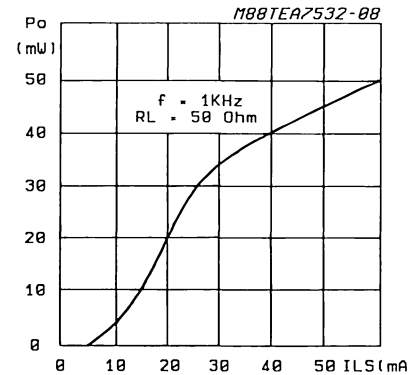
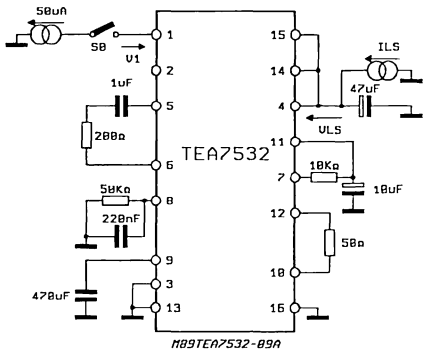


Figure 6 : Output Power Versus Supply Current.



TEST CIRCUITS

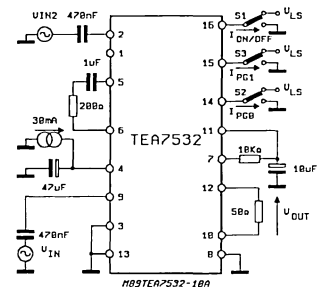
Figure 7 : Shuntvoltage Regulator/ Reference Voltage at Pin 1.



Note : S0 open for VLS 1
S0 close for VLSM.

Figure 8 : Loudspeaker Amplifier : Gain/Distor tion/Output Offset.

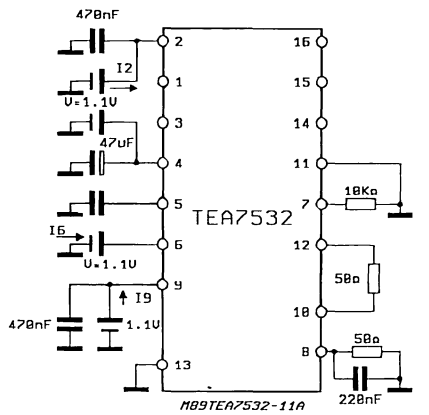
	S1	S2	S3
G1XX	1	X	X
G000	0	0	0
G010	0	1	0
G001	0	0	1



- $G = \frac{V(10) - V(12)}{V(9)} = \frac{Vout}{V(9)}$
- VOFFS with Vin = 0.

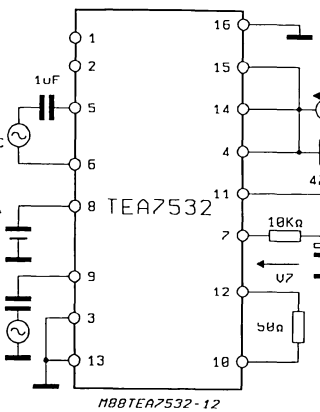
V_{LS} = 1
G_{ND} = 0

Figure 9 : Impedance ZMIC, ZINP and Zin2.



$Zmic = \frac{1.1\ V}{I6}$; $Zinp = \frac{1.1\ V}{I9}$; $Zin2 = \frac{1.1\ V}{I2}$

Figure 10 : Antiacoustic Feedback System at G011.



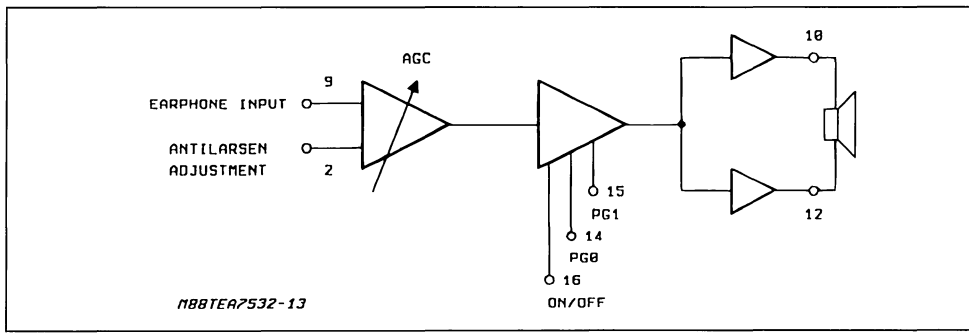
CIRCUIT DESCRIPTION

TEA7532 is a 16 pin DIL integrated circuit providing the following facilities :

- Loudspeaker amplifier
- Antiacoustic feed-back system (antilarsen system)

1.1. LOUDSPEAKER AMPLIFIER

Figure 11.



The amplifier is divided into 3 main sections.

- Automatic Gain Control (AGC)
- Preamplifier
- Push-pull amplifier (bridge structure)

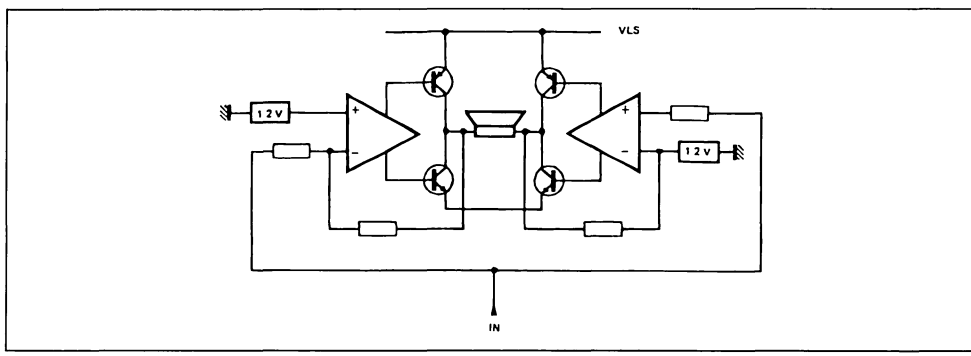
a) The AGC section is used for the antilarsen and antidistortion system.

- When used in a telephone set to avoid larsen effect the AGC automatically decreases loudspeaker amplifier gain.
- When the required output level exceeds the capabilities of the available current, the AGC decreases the loudspeaker amplifier gain to avoid distortion.

b) The preamplifier permits step control of amplifier gain in steps of 6 dB, using pins PG0 and PG1, which may be controlled using switches or by a microprocessor. The amplifier may be muted using the ON/OFF control signal (pin 16).

c) The output amplifier uses a double push-pull configuration (H bridge) to get maximum dynamic range under limited supply conditions.

Figure 12.

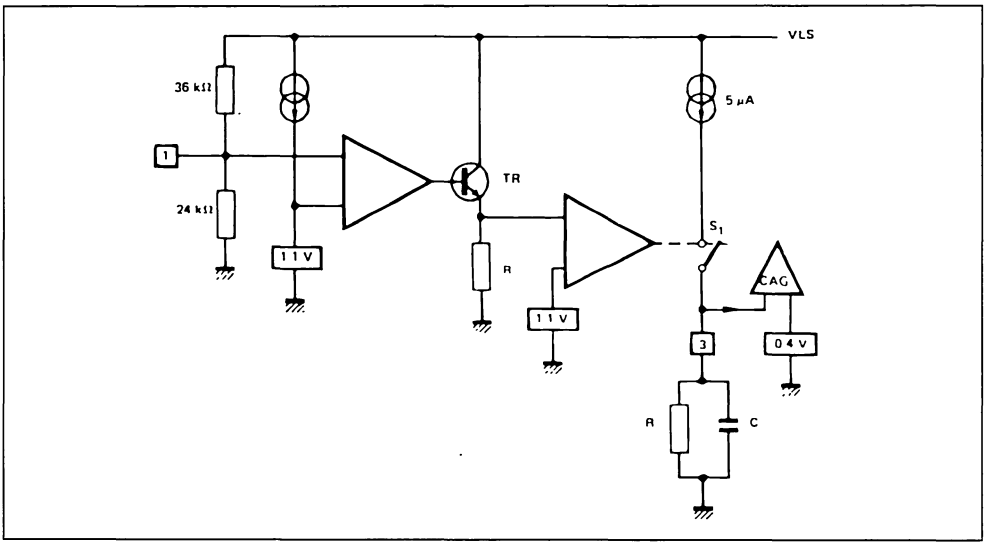


Amplifier dc supply.

In transmission mode, the supply voltage is controlled by the internal shunt DC regulator. For this reason, the TEA7532 should be supplied from a current source (see : supply considerations).

An antidistortion system is embodied which provides AGC control to avoid loudspeaker distortion under current-limited conditions.

Figure 13.



Circuit action.

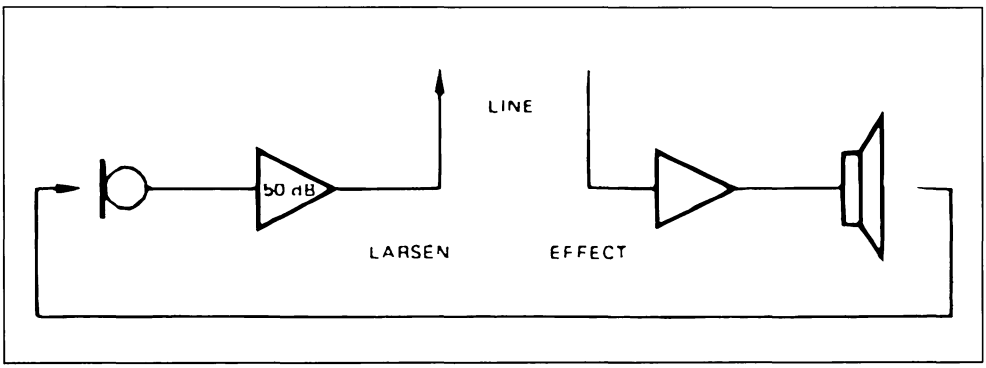
When the supply voltage is insufficient, the voltage at pin 1, falls below the reference voltage 1.1 V, resulting in transistor (TR) being switched off, resulting in zero current flow in resistor R. This state enables the gain control system. Under these conditions, the shunt DC supply will switch at a rate determined by the time constant of the RC network on pin 3.

This switching action accomodates normal speech characteristics under low supply conditions.

1.2. ANTIACOUSTIC FEED-BACK SYSTEM (ANTILARSEN SYSTEM)

The purpose of this system is to control AGC action in order to avoid acoustic feed-back between the loudspeaker and the microphone, when used in a telephone set.

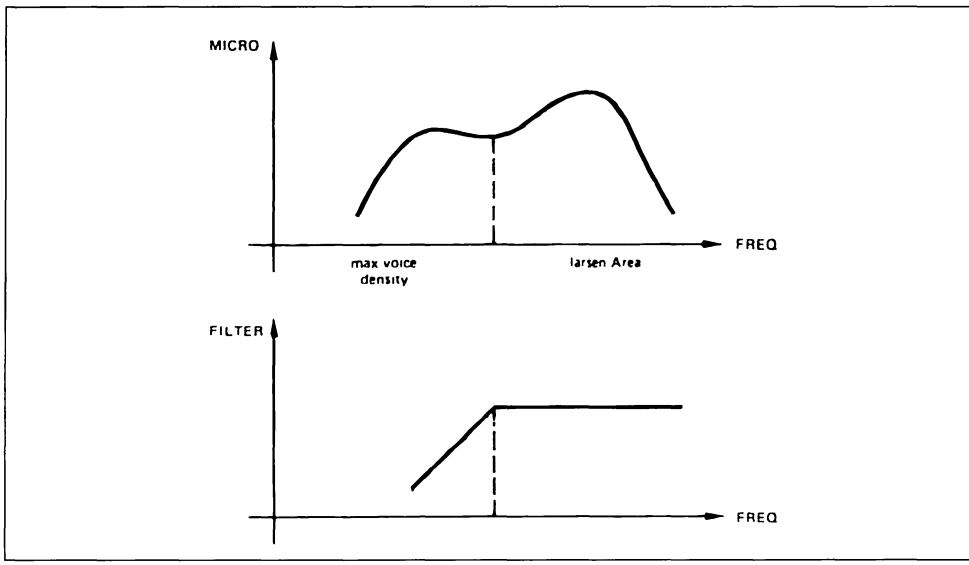
Figure 14 .



Principle of operation.

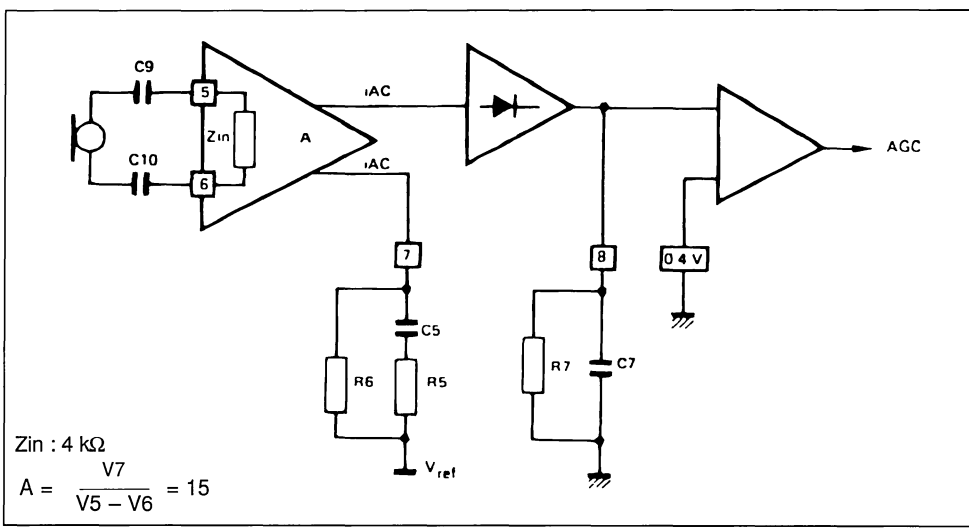
When examining the spectral density of the voice area and the larsen area, it can be seen that the dominant features of each exist in different frequency bands.

Figure 15.



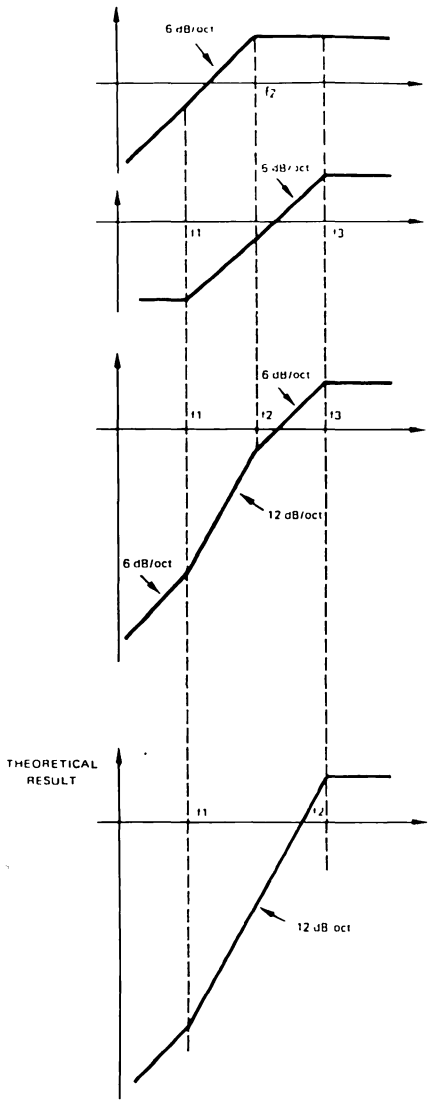
To extract the larsen component, the microphone signal is first filtered by a second order filter (formed by two first order filters), then amplified and rectified in order to produce the AGC control signal.

Figure 16.



The first filter is generated by the capacitors on pins 5 and 6 ; the second filter by the R-C network on pin 7.

Figure 17 : Antilarsen System Filter Response.



Filter on pins 5 & 6

$$f2 = \frac{C9 + C10}{2\pi \, Zin \, C9 \, C10}$$

Filter on pin 7

$$f1 = \frac{1}{2\pi \, (R5 + R6) \, C5}$$

$$f3 = \frac{1}{2\pi \, R5 \, C5}$$

Antilarsen system
Filter response

If f2 = f3 the Antilarsen system filter is equivalent to a second order filter.

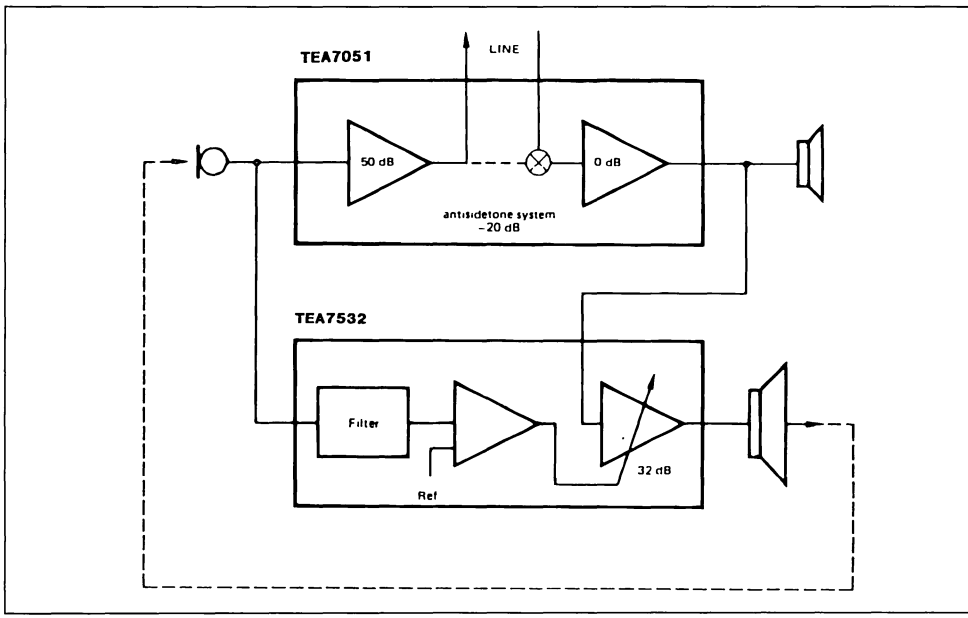
$$\frac{C9 + C10}{2\pi \, Zin \, C9 \, C10} = \frac{1}{2\pi \, R5 \, C5}$$

A complete telephone set has two antilarsen systems :

- one in the transmission circuit (for example : TEA7051) antisidetone network ;
- one in the loudspeaker amplifier (for example : TEA7532).

Together these form a high efficiency antilarsen system.

Figure 18.



PIN FUNCTIONS

PIN 1 : ADJUST V_{LS}

This pin is used to adjust the IC supply voltage.

PIN 2 : ANTILARSEN ADJUSTMENT

The AC signal at this pin is amplified to the loudspeaker without AGC attenuation.

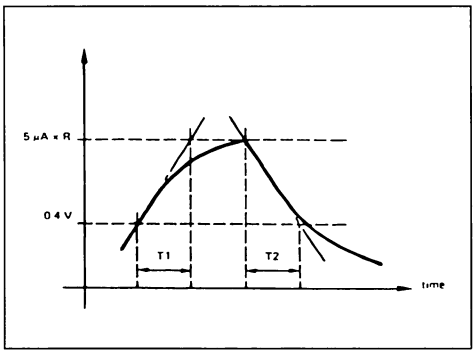
PIN 3 : AUTOMATIC GAIN CONTROL FILTER

The antidistortion system response is adjusted by the R-C network on this pin.

The AGC will be switched ON when the level on pin 3 is greater than the reference voltage (0.4 V), the RC-network charges (current source ON) or discharges (current source OFF) according to the supply voltage.

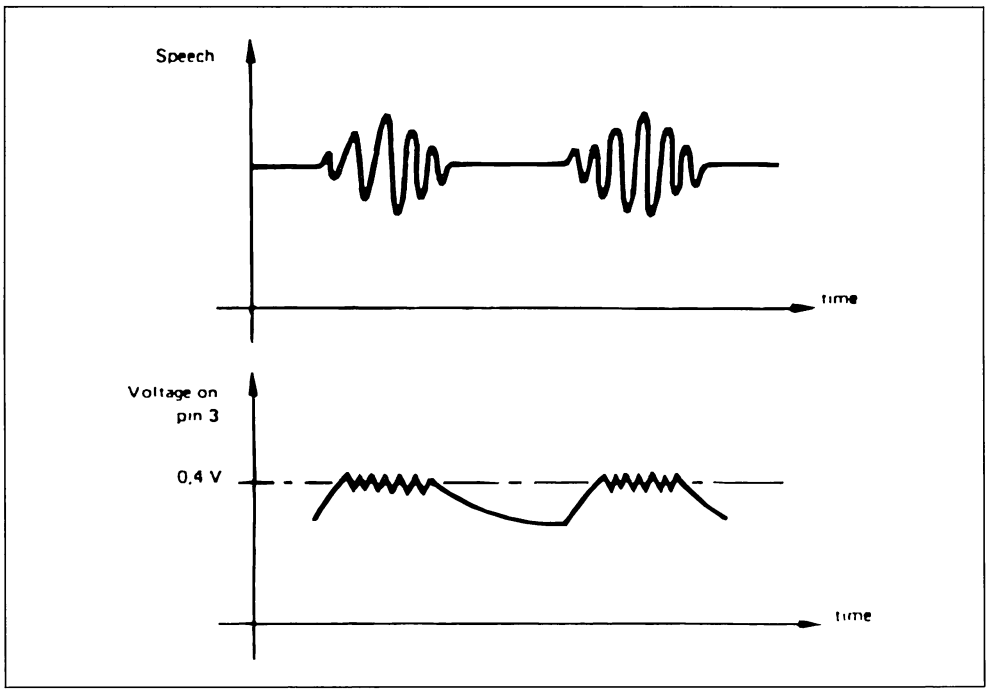
THEORETICAL VOLTAGE ON PIN 3

Figure 19 :



- The value of R affects the system time constant and the charge/discharge duty cycle.
- The value of C only affects the system time constant.
- R should be greater or equal than 150 kΩ for correct AGC operation.

Figure 20.



PIN 4 : CIRCUIT SUPPLY VOLTAGE
With pin 1 open circuit, VLS is internally stabilized at 2.8 V.

When the TEA7532 is under AGC control, the voltage on this pin varies slightly (due to AGC action).

PIN 5/6 : MICROPHONE INPUTS

These are used for antilarsen control.

PIN 7 : ANTILARSEN FILTER 1

The second filter of the antilarsen system (1 st filter : pins 5-6) is formed by the RC network R5C5.
In order to obtain a second order filter for the antilarsen system, the cut-off frequency defined at this pin, should be the same as that chosen for the first filter.

For correct TEA7532 operation R6 and R5 should be fixed at 10 kΩ and 1 kΩ respectively.

PIN 8 : ANTILARSEN FILTER 2

The gain and the response of the antilarsen system can be adjusted respectively by the resistor and the capacitor on this pin, according to the acoustic characteristics of the telephone set.

The value of the resistor should not exceed 390 kΩ. When the voltage on this pin exceeds the threshold voltage of 0.4 V, the AGC system is enabled.

PIN 9 : EARPHONE INPUT

Input for loudspeaker signal.

PIN 10-12 : LOUDSPEAKER OUTPUTS

Maximum output voltage : $V_{pp} = 2\ V_{LS} - 2.5$ V (with a gain of 32 dB).

Maximum output current : depending of the supply current.

Two loudspeaker connection methods are possible, using the amplifier in either "H" mode or "B" mode.

Note : It is advisable to connect a 47 nF capacitor in parallel with the loudspeaker (between pins 10 and 12).

- "H" Mode

This is for low voltage working, but at a higher supply current. The highest output power is available in this mode, due to the 5.5 V maximum supply voltage restriction, imposed by the TEA7532.
Loudspeaker impedance recommended value : 50 Ω.
Maximum gain available between earphone input and loudspeaker output : 32 dB.

Figure 21.

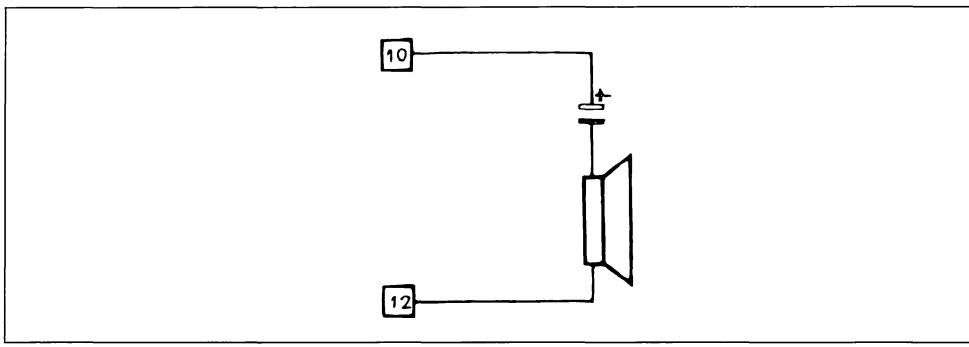
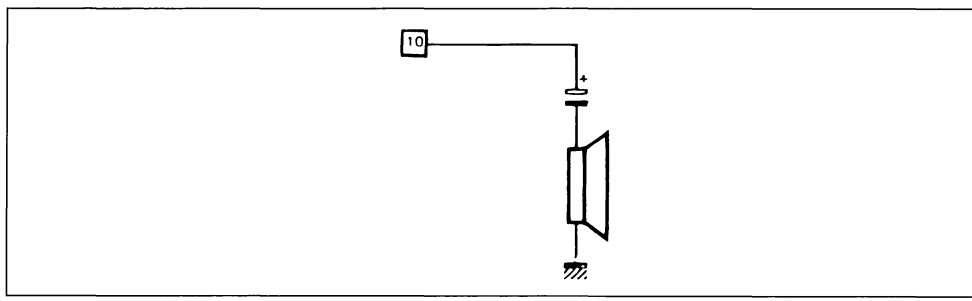


Figure 22.



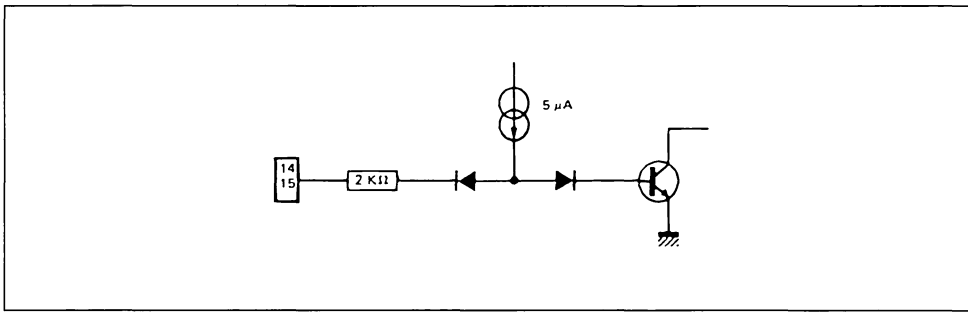
- "B" Mode
This allows higher voltage operation, but at a lower supply current.
Loudspeaker impedance recommended value : 25 Ω.
Maximum gain available between earphone input and loudspeaker output : 32 - 6 = 26 dB.

PIN 11 : Vref : INTERNAL REFERENCE
Output which provides an internally regulated reference voltage.

Vref = 1.1 V typical

MAXIMUM AVAILABLE CURRENT : 5 µA

Figure 23.



PIN 13 : GROUND

PIN 14-15 : GAIN ADJUSTMENT INPUTS

These pins are used to adjust the loudspeaker amplifier gain. Four steps of 6 dB/step are available (pin open circuit = high level).

PG0	PG1	
1	1	Gmax
1	0	Gmax - <0> 6 dB
0	1	Gmax - 12 dB
0	0	Gmax - 18 dB

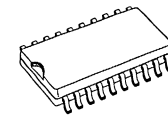
PIN 16 : LOUDSPEAKER MUTING.

This pin is used to mute the loudspeaker. Pin open-circuit : high level = loudspeaker muted.

Pin low level : louspeaker enabled (see connection of pins 14 and 15).

MONITOR AMPLIFIER

- 7 DIGITALLY PROGRAMMABLE GAINS IN STEPS OF 4.5dB
- ON/OFF POSITION
- LOW VOLTAGE (3.5V to 6.5V)
- POWER: >140mW at 5V; >250mW at 6.5V



SO-20

ORDERING NUMBER: TEA7533FP

DESCRIPTION

This 20 pins IC is designed for monitoring and loudspeaker telephone set and provides:

a) signal amplification for monitoring (loudspeaker).
b) antiacoustic feedback (antilarsen).
c) antidistortion by automatic level adaptation.
d) antilarsen adjustment (full duplex).
e) antidistortion by automatic gain adaptation in current supply mode.
f) service audio inputs with internal dedicated switches.

FUNCTIONAL DESCRIPTION

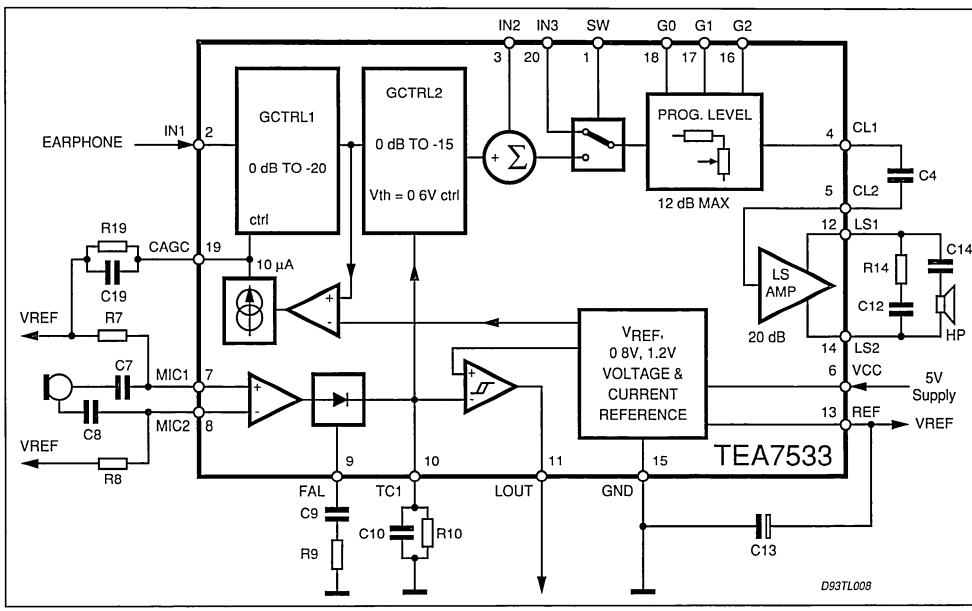
TEA7533 performs the following functions:

The circuit amplifies the incoming signal and feeds it to the loudspeaker. PG0, PG1 and PG2 inputs are used to set the loudspeaker gain in a range of 32dB to 5dB in 7 steps of 4.5dB.

The TEA7533 inputs (PG0, PG1, PG2) allows also the loudspeaker to be cut-off, thus ensuring privacy of communication.

- The antilarsen (antiacoustic feedback) system is incorporated.
- The maximum power available on a 50Ω impedance loudspeaker is 140mW at 5V and 250mW at 6.5V.

BLOCK DIAGRAM



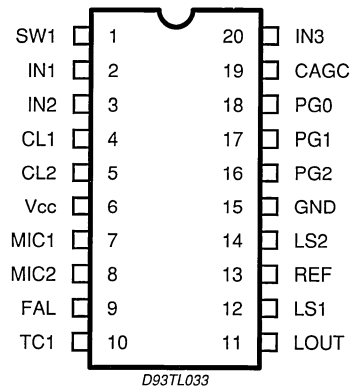
PIN DESCRIPTION

N°	Symbol	Description
1	SW	Switch control: IN2 or IN3
2	IN1	Audio Input AVG Controlled
3	IN2	2nd Audio input; No Anti-distortion Control
4	CL1	Intermediate Receive Output (Decoupling capacitor)
5	CL2	Intermediate Receive Input (Decoupling capacitor)
6	V_{CC}	Supply Voltage
7	MIC1	Microphone input 1
8	MIC2	Microphone input 2
9	FAL	Antilarsen Filter
10	TC1	Antilarsen Gain Set up
11	LOUT	Status Output, Digital Output.
12	LS1	Loudspeaker Output1
13	REF	Reference Voltage; (V_{CC} - 0.7V/2)
14	LS2	Loudspeaker Output2
15	GND	Ground
16	PG2	Digital Input; Loudspeaker Level Control
17	PG1	Digital Input; Loudspeaker Level Control
18	PG0	Digital Input; Loudspeaker Level Control
19	CAGC	Gain Control Filter Capacitor
20	IN3	3rd Audio Input

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_{CC}	Max. Supply Voltage	7	V
I_{CC}	Max Supply Current at t > 300ms at t ≤ 300ms	100 150	mA mA
V_{LOGIC}	Voltage Level (logic pins)	-0.6/V_{CC}+0.6	V
T_{op}	Operative Temperature Range	-20 to +70	°C
T_{stg}	Storage Temperature Range	-55 to +125	°C

PIN CONNECTION (Top view)



D93TL033

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, R_{BIAS} = 60KΩ; V_{G0} = V_{G1} = V_{G2} = H; V_{in} = 0Vrms; V_{TG1} = 0V; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.5	5	6.5	V
I_{CC}	Supply Current	V_{CC} = 5V; PG0 = PG1 = PG2 = L V_{CC} = 5V; PG0 = PG1 = PG2 = H	– –	0.75 1.6	1 2.1	mA mA
V_{ref}	Voltage Reference	 V_{CC} = 5V	– 1.72	(V_{CC} - 0.7)/2 2.15	– 2.6	V
I_{ref}	Current Available at V_{ref}	Source Sink	– –	30 400	– –	µA µA
IN2 & IN3 AMPLIFIER SECTIONS						
G_O	Final Stage Gain (V_{LS1} - V_{LS2})/V_{CL2}		19	20	21	dB
G	Loudspeaker Amplifier Gain (V_{LS1} - V_{LS2})/IN3 (or IN2)	V_{TC1} = 0V; V_{IN} = 60mVrms V_{CAGL} = 0V				
		PG2, PG1, PG0				
G111	Gain max	H H H	30	31.5	33	dB
G110	Gain 1st step	H H L	25.5	27	28.5	dB
G101	Gain 2nd step	H L H	21	22.5	24	dB
G100	Gain 3rd step	H L L	16.5	18	19.5	dB
G011	Gain 4th step	L H H	12.0	13.5	15	dB
G010	Gain 5th step	L H L	7.5	9	10.5	dB
G001	Gain 6th step	L L H	3	4.5	6	dB
G000	Off step	L L L	-	-40	-30	dB
V_{OFF}	Output Offset	G = G111; R_{LOAD} = 50Ω	-50	-	50	mV
LS DIN	Loudspeaker Dinamic (V_{LS1}- V_{LS2})	R_{LOAD} = 50Ω V_{CC} = 3.5V; THD = 4% V_{CC} = 5V; THD = 4%	 4.5 6.5	 5 6.7	 - -	 Vpp Vpp
THD	Output Distortion	V_{CC} = 5V G = G111(32dB) SW = L; V_{OUT} = 2Vrms SW = H; V_{OUT} = 2Vrms	 - -	 - -	 2 2	 % %
IN1 AMPLIFIER SECTION						
G_1	Loudspeaker Amplifier Gain (V_{LS1} - V_{LS2}) / IN1	V_{CAG} (19) = V_{REF}; V_{TC1} = 0V V_{IN1} = 45mVrms	29.5	31.5	34.5	dB
THD1	Distortion	V_{IN} = 45mVrms	–	1	2	%
IN1 ANTIDISTORTION SECTION						
ALG1	Antilarsen Attenuation on IN1 Chain	V_{CAGC} = V_{REF}; V_{TC1} = 0.8V	–17	–15	–13	dB
ALTHD	Distortion with Antilarsen Active		–	4.5	6.0	%
CAGC THD	Distortion with AGC Control Active	V_{IN1} = 80mV V_{IN1} = 560mV	– –	– –	3 10	% %
PG	Logic Interface PG0, PG1, PG2, SW= L, IN3 = ON					
PGH	Logical Input High		0	-	0.4 x (V_{CC} - 0.7)	V
PGL	Logical Input Low		0.6 x (V_{CC} - 0.7)	-	V_{CC}	V
I_{PGL}	Input Current Low state	V_{IN} = 0V	-1	-	+1	µA
I_{PGH}	Input Current High State	V_{IN} = V_{CC}	-1	-	+1	µA
ANALOG INTERFACE						
I_{BIAS}	Biasing Current Analog Inputs	IN1, IN2, IN3, MIC1,MIC2	–	17	100	mA

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ANTILARSEN SECTION						
G_{MIC}	Microphone Amplifier Gain = $V_{FAL}/(V_{MIC1} - V_{MIC2})$	V_{IN} = 4.5mVrms; f = 5KHz	19.5	21	22.5	dB
$V_{TC1\ TH}$	TC1 Threshold for –3dB attenuation on IN1 chain		0.55	0.68	0.75	V
$V_{TC1\ LOW}$	TC1 Level with V_{mic} = 0 Vrms		0	0.07	0.2	V
TC1 H	High Thereshold of LOUT Comparator	V_{LOUT} < 0.4V	1.1	1.2	–	V
TC1 L	Low Thereshold of LOUT Comparator	V_{LOUT} > 4.1V	–	0.8	0.9	V
$I_{LOUT\ L}$	Output Current of Comparator LOUT	V_{TC1} = 1.5V; V_{LOUT} = 0.5V	5	20	–	µA
$I_{LOUT\ H}$		VTC1 = 0.6V; V_{LOUT} = 3.5V	–	–1	–0.5	µA
$V_{LOUT\ L}$	Output Voltage of Comparator LOUT	VTC1 = 1.5V	–	0.08	0.4	V
$V_{LOUT\ H}$		VTC1 = 0.6V	4.1	4.33	–	V

TEST CIRCUIT

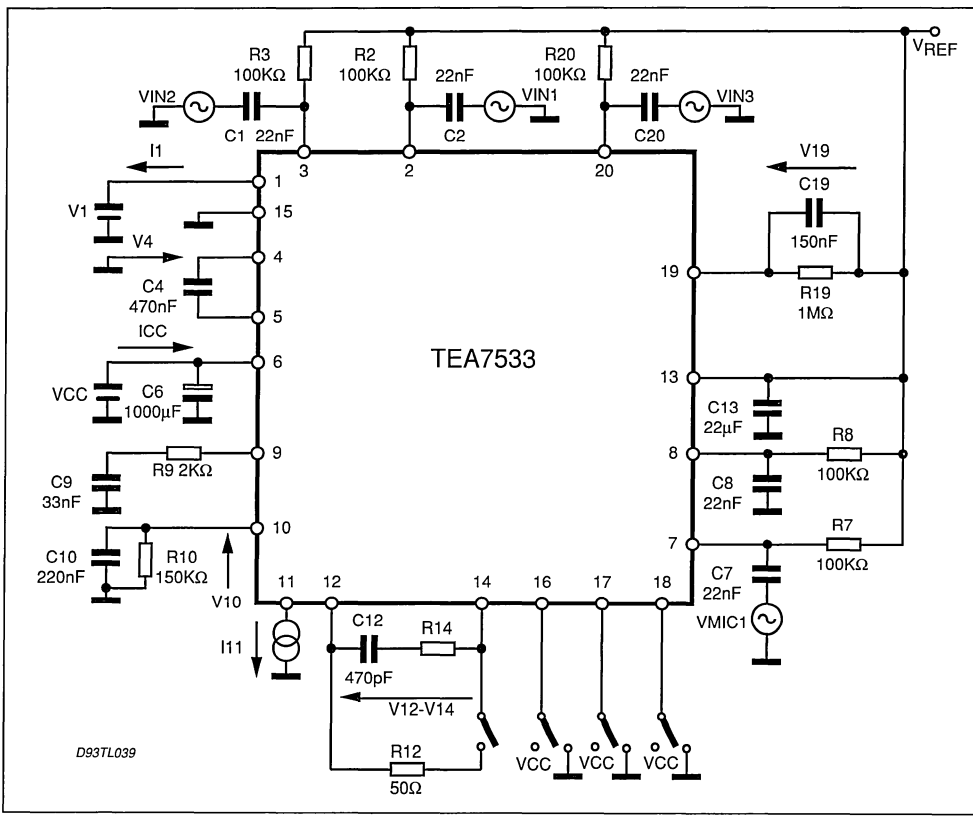


Figure 1: IN1 Channel - AGC Gain (Typical)

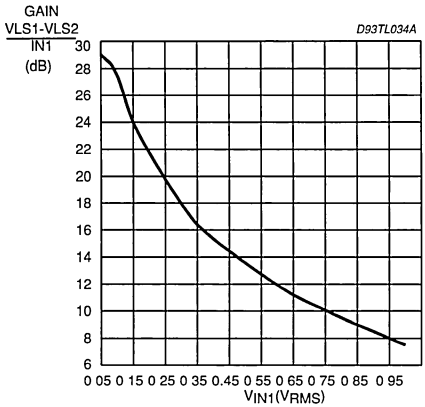


Figure 2: IN1 Channel ($V_{CAGC} - V_{REF}$)

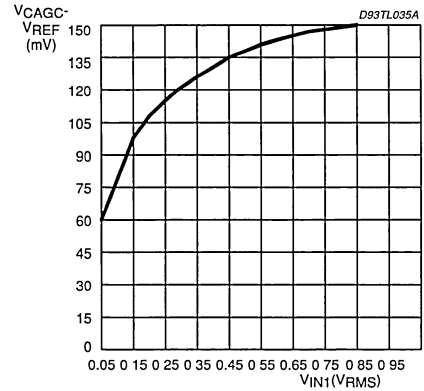


Figure 3: IN1 Channel – Distortion (Typical)

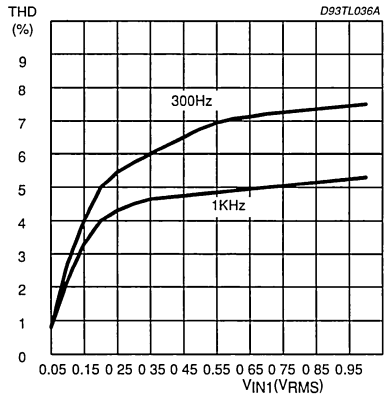


Figure 4: IN3 and IN2 Channels – Distortion

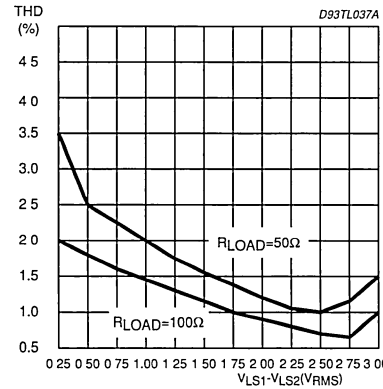
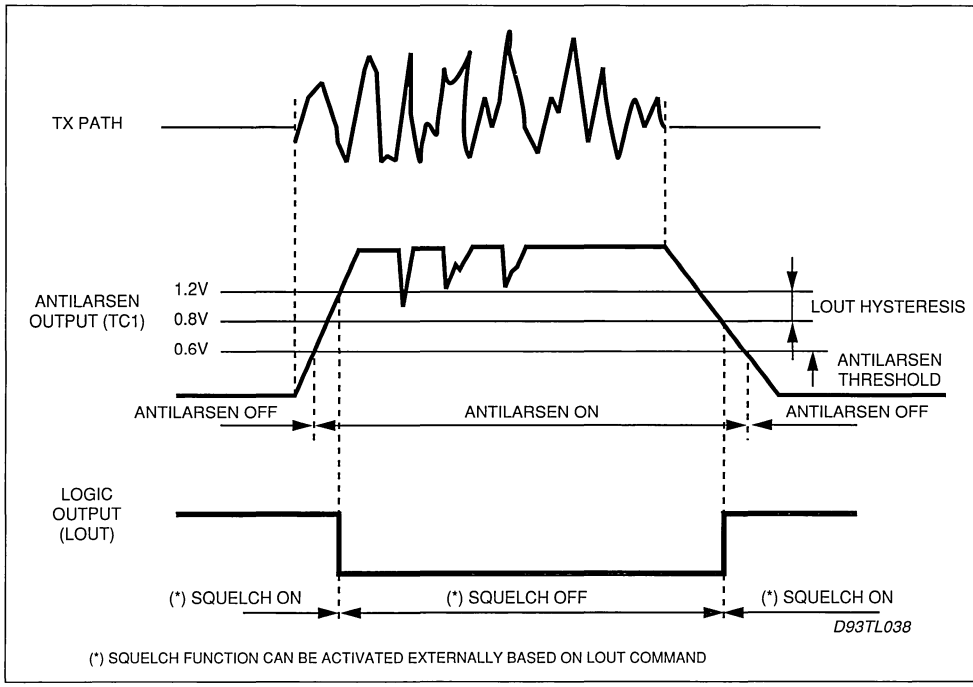


Figure 5: Time Diagram for TC1 (Antilarsen) and LOUT.



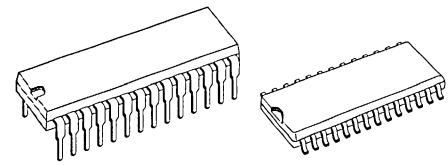
SGS-THOMSON MICROELECTRONICS

TEA7540

HANDSFREE CONTROLLER

PRELIMINARY DATA

- NOISE/SPEECH DISCRIMINATION IN EMISSION AND RECEPTION
- INTEGRATED SIGNAL GAIN COMPRESSOR IN BOTH MODES
- PROGRAMMABLE ATTENUATORS IN BOTH MODES
- ADAPTED TO ACOUSTIC PARAMETERS OF ALL CABINETS
- LOW OPERATING VOLTAGE 2.5V
- LOW OPERATING CURRENT 2.1mA
- CHIP SELECT BETWEEN HANDSFREE AND MONITORING MODES



DIP28 **SO28**

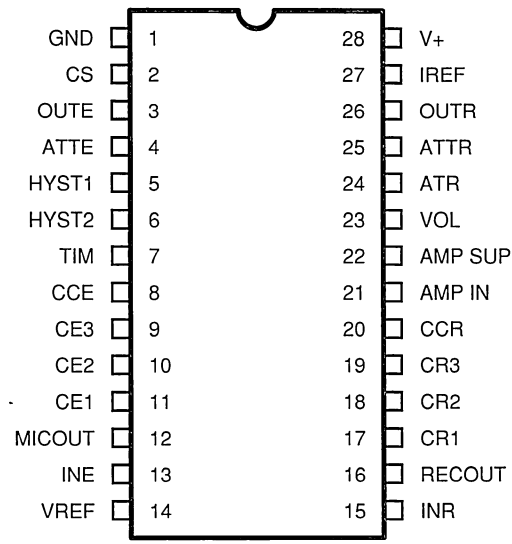
ORDERING NUMBERS:

TEA7540DP TEA7540FP

DESCRIPTION

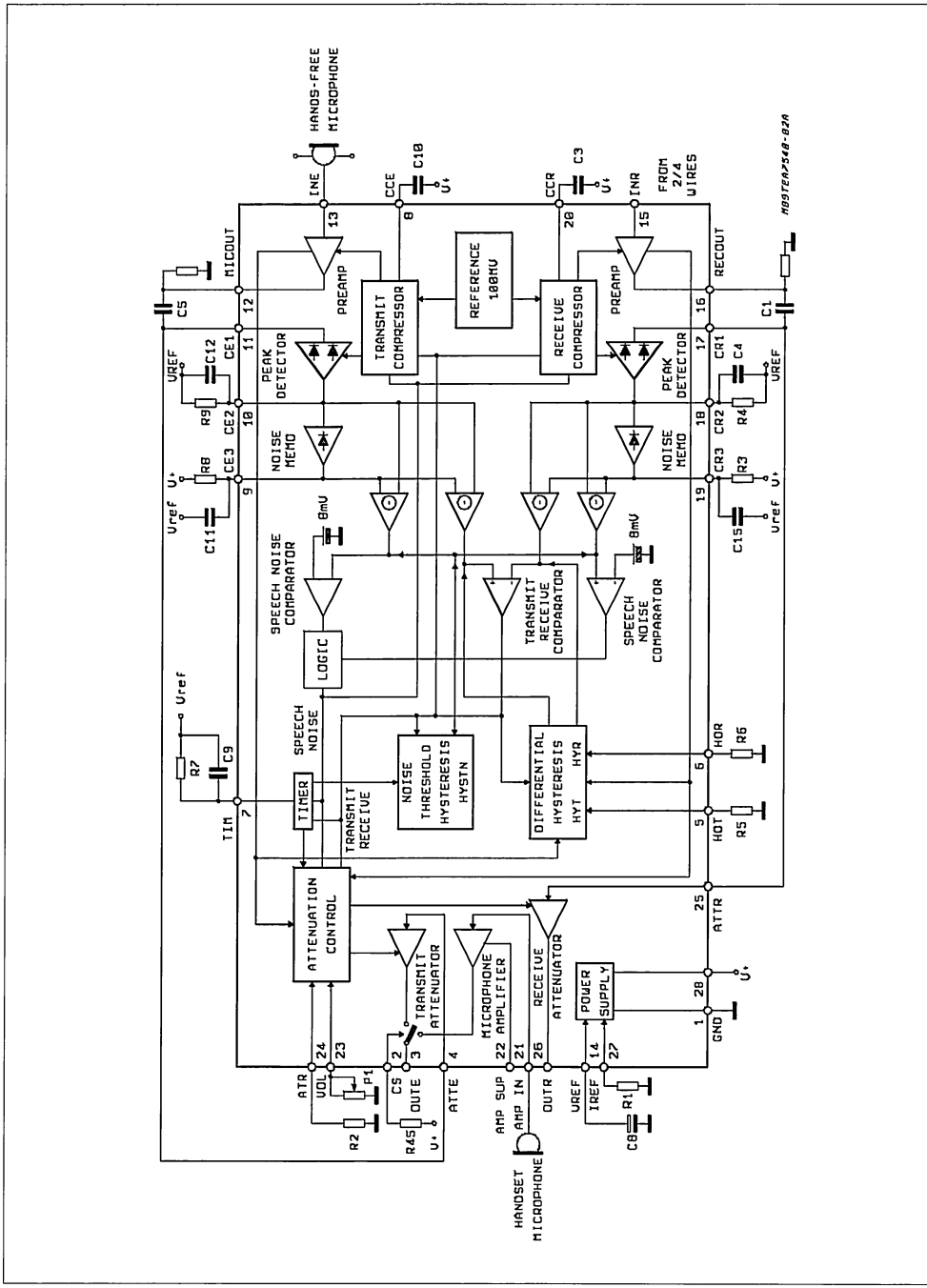
This 28 pins IC is an innovative approach to quality handsfree telephone sets. It results from an extensive research on speech signal.

PIN CONNECTION (top view)



D93TL005

BLOCK DIAGRAM



PIN FUNCTION

N°	Name	Function
1	GND	Ground
2	CS	Chip Select
3	OUTE	Transmit Attenuator Output
4	ATTE	Transmit Attenuator Input
5	HYST1	Transmit Channel Hysteresis
6	HYST2	Receive Channel Hysteresis
7	TIM	RC Timer
8	CCE	Time Constant of the Transmit Signal Compressor
9	CE3	Transmit Background Noise Memorization Output
10	CE2	Transmit Peak Detector Output
11	CE1	Transmit Rectifier Input
12	MICOUT	Transmit Signal Compressor Output
13	INE	Transmit Signal Compressor Input
14	V_{ref}	V+/2 - Reference Voltage
15	INR	Receive Signal Compressor Input
16	RECOUT	Receive Signal Compressor Output
17	CR1	Receive Rectifier Input
18	CR2	Receive Peak Detector Output
19	CR3	Receive Background Noise Memorization Output
20	CCR	Time Constant of the Receive Signal Compressor
21	AMP IN	Handset Preamplifier Input
22	AMP SUP	Handset Preamplifier Power Supply
23	VOL	Volume Control
24	ATR	Attenuation Value
25	ATTR	Receive Attenuator Input
26	OUTR	Receive Attenuator Output
27	I_{ref}	Reference Current Source
28	V+	

FUNCTIONAL DESCRIPTION

SWITCHED ATTENUATORS

Figure 1 represents a block diagram of a handsfree subset with attenuators in signal mode. To prevent the system from howling, the total loop gain, including acoustic feedback through the housing and sidetone coupling, must be less than 0dB. For this purpose, two switched attenuators are inserted in each mode (emission and reception). The attenuation is shifted from one mode to the other, resulting from the speech level comparison between each way.

To prevent the circuit to switch continuously in one way, the operation of the IC must be fully symetrical in both ways. This involves signal comparison, attenuation value.

GAIN COMPRESSOR

In TEA7540, two signal compressors are inserted in each mode before the signal comparison, so the signal coming from each end has the same level (100mV peak), the losses in each way (for instance losses resulting from the line length in receiving mode) are compensated and the signal comparison is fully symetrical. The time constant of each signal compressor decreases 80 times more quickly than it increases to prevent from noise increasing between words. The compressing depth is 38dB.

BACKGROUND NOISE DISCRIMINATION

An additional feature provided in TEA7540 is background noise level discrimination in each way. The IC stores the background sound level with a long time constant (3 to 5 seconds depending on an external RC) and compares it with the incoming signal in order to distinguish a useful signal (speech) from the background noise. This background noise memorization is also used to compensate the noise in each mode before signal comparison: the noise level in each mode is sub-

stracted from the incoming signal before the comparison. So very high noise level in one mode cannot trouble the comparison between the useful signals.
The result of the comparison manages the attenuators in the following way:

- The maximum attenuation is switched on the mode where the speech signal is the lowest. The maximum attenuation is fixed by two external resistor (maximum 52dB). The time constant of the switch is fixed by the timer via an external capacitor.

- When neither party is talking both attenuators are set to a medium attenuation. Thus each mode is in idle mode. The time constant of the switch from active mode to idle mode must be long enough to prevent from switching to idle mode between two words (see fig.2). This time constant is fixed by an external RC.

Figure 1

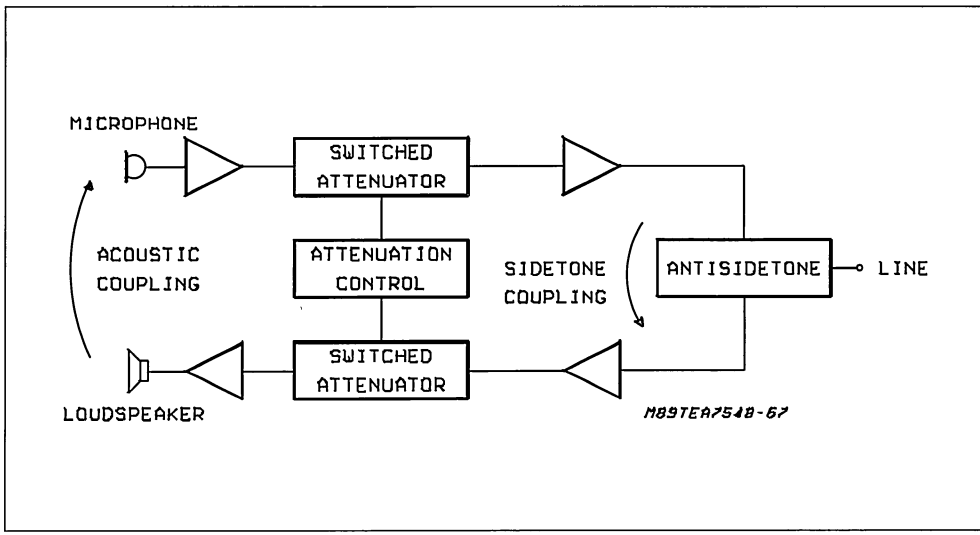
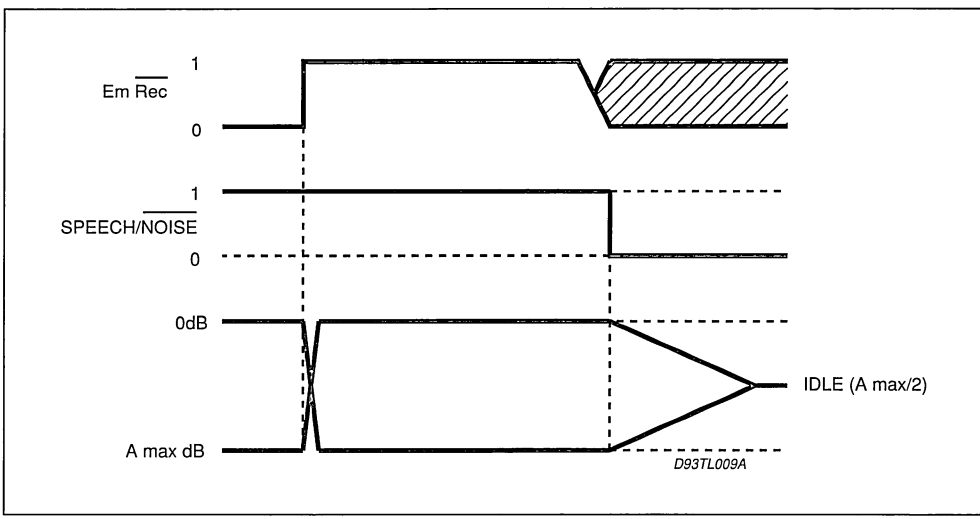


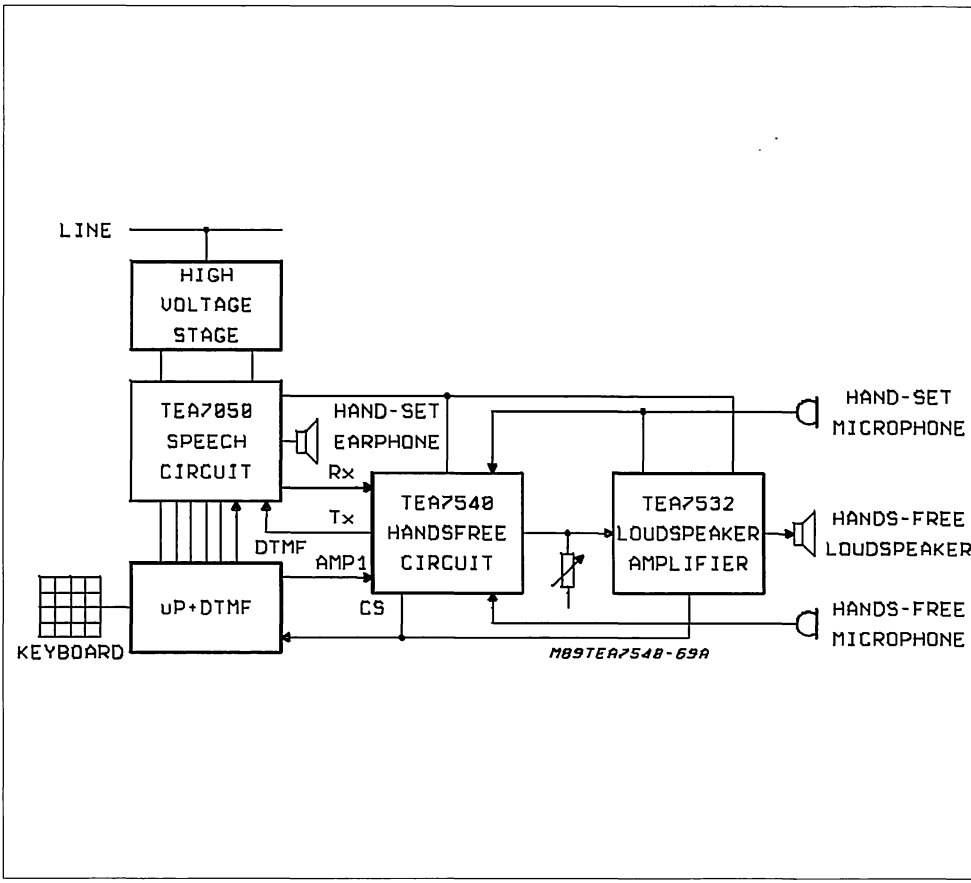
Figure 2



TEA7540 OPERATION

TEA7540 is powered through an external shunt regulator (for instance the shunt regulator of the monitor amplifier TEA7532) or an external zener diode.
It can work at a very low voltage (2.5V) over the circuit and it has a low current consumption (2.1mA).
It's also possible via the chip select pin (CS) to put the handsfree function in standby to use the circuit in monitoring mode with the handset microphone.
TEA7540 is designed to work with all kind of microphone, including Electret.
TEA7540 also handles the handset microphone signal (AMP IN) when the system is set to normal conversation mode.

Figure 3: Application Diagram (Example of high range telephone set using TEA7540).



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V^+	Supply Voltage	12	V
Top	Operating Temperature	-20 to 70	°C
T_{stg}	Storage Temperature Range	-65 to 125	°C

ELECTRICAL CHARACTERISTICS (Refer to test circuits, T_{amb} = 25°C; V^+ = 3V; f = 1KHz unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
SUPPLY SECTION							
V^+	Supply Voltage		2.5		7.0	V	1
I_C	Current Consumption	Vcs = 0 Handsfree mode Vcs= N.C. Monitoring mode		2.1 1.1	3.0 1.5	mA mA	1
TRANSMIT SECTION							
COMPRESSOR							
Rine	Compressor input impedance	PIN13	7.5	10.0	14.5	KΩ	1
C_R	Compressor Range			16.5		dB	
G_{1max}	Maximum Gain		40.5	41.5	42.5	dB	2
G_{1min}	Minimum Gain		24.0	25.0	26.0	dB	3
V_O	Output Voltage	PIN12 compressing range	160	200	240	mVpp	4
T_{dh}	Transmit Distortion				3.0	%	4
I_{cce1}	Compressor dacay time current	Increasing gain	1.0	1.25	1.5	µA	5
I_{cce2}	Compressor rise time current	Decreasing gain	65	85	105	µA	6
V_{cce1}	Voltage drop PIN8 V_{cce} = Vref - Vpin8	G1max		0	20	mV	2
V_{cce2}		G1min	175	225	275	mV	3
PEAK DETECTOR							
R_{inpd}	Input impedance PIN11		7.5	10.0	14.5	KΩ	1
I_{ce2}	Rise time current		16	20	24	µA	7
NOISE MEMORIZATION							
V1	Max voltage drop on pin 9		33	36	45	mV	8
ATTENUATOR							
R_{ina}	Input impedance PIN4		7.5	10	14.5	KΩ	1
ATE-	Attenuation= 20log(Voute/Vatte) Mode: Inactive Tx, Rx Comp. Max Gain	Rpin24 = 11KΩ Rpin24 = 15KΩ		46 58		dB dB	9
ATE-active	Mode: Active	Rpin24 = 11KΩ	0	1.5	3	dB	10
ATE-IDLE	Mode: Noise Tx, Rx Comp. Max Gain	Rpin24 = 11KΩ		23		dB	11
RECEIVE SECTION							
COMPRESSOR							
R_{inr}	Input impedance	PIN15	7.5	10.0	14.5	KΩ	1
C_R	Compressor Range			20.5		dB	
G_{2max}	Maximum Gain		35.5	36.5	37.5	dB	2
G_{2min}	Minimum Gain		15.0	16.0	17.0	dB	3
V_{micout}	Compressor output voltage	PIN16 compressing range	160	200	240	mVpp	4
R_{dh}	Receive Distortion				3.0	%	4
I_{ccr1}	Compressor decay time current	Increasing gain	1.0	1.25	1.5	µA	5
I_{ccr2}	Compressor rise time current	Decreasing gain	65	85	105	µA	6
V_{ccr1}	Voltage drop PIN20 Vccr = Vref - Vpin20	G2max		0	20	mV	2
V_{ccr2}		G2min	175	225	275	mV	3

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
PEAK DETECTOR							
R_{inpd}	Input impedance	PIN17	7.5	10	14.5	KΩ	1
I_{cr2}	Rise time current		16	20	24	µA	7
NOISE MEMORIZATION							
V1	Max voltage drop on PIN 19		33	36	45	mV	8
ATTENUATOR							
Rina	Input impedance	PIN25	7.5	10	14.5	KΩ	1
ATR-	Attenuation= 20lg(Voutr/Vatte) Mode: Inactive RX, TX Comp. Max Gain	Rpin24 = 11KΩ Rpin24 = 15KΩ		46 58		dB dB	9
ATR-active	Mode: Active	Rpin24 = 11KΩ	0	1.5	3	dB	10
ATR-IDLE	Mode: Noise RX, TX Comp. Max Gain	Rpin24 = 11KΩ		23		dB	11
ATTENUATION CONTROL SECTION							
V_{TIME}	Tx Mode Att.Voltage		190	250	325	mV	12
I_{TIME}	TX Mode Att.Current		40	50	70	µA	12
V_{TIMR}	RX Mode Att.Voltage		-325	-250	-190	mV	13
I_{TIMR}	RX Mode Att.Current		40	50	70	µA	13
ATRVOL	Volume Control		29	32	35	dB	14
MICROPHONE PREAMPLIFIER							
R_{amp}	Imput impedance	PIN21	35	50	70	KΩ	
G_{mic}	V_{mic} = Voute-Vamp in	V_{cs} open	19	20	21	dB	
G_{2off}	Compressor Gain Monitoring Mode G2 = V_{recout}/V_{inr}	Rext between PINs 2 - 28 Rext = open Rext = 40KΩ		36.5 16		dB dB	

Figure 1: Basic Configuration

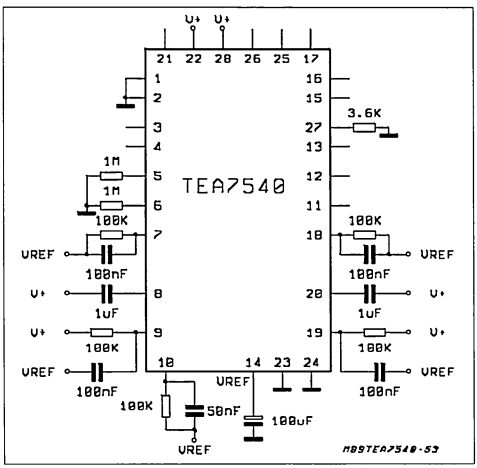
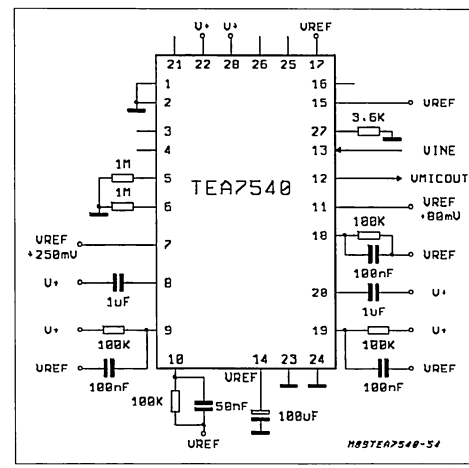


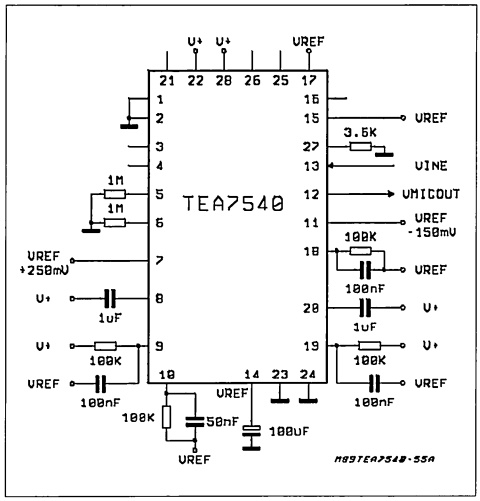
Figure 2: Test Configuration



V^+ = 3V
pin 7 is forced to transmit mode
pin 11 is forced to max gain
Input signal on pin 13 VINE = 1.5mVpp
output voltage VMICOUT measured on pin 12

G1max = 20log (VMICOUT / VINE)

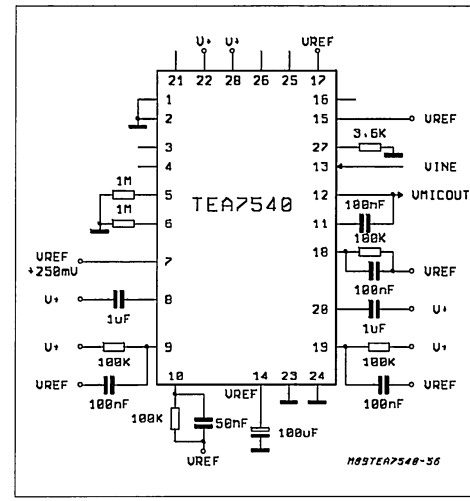
Figure 3: Test Configuration



$V^+ = 3V$
pin 7 is forced to transmit mode
pin 11 is forced to minimum gain
Input signal on pin 13 VINE = 1.5mVpp
output voltage VMICOUT measured on pin 12

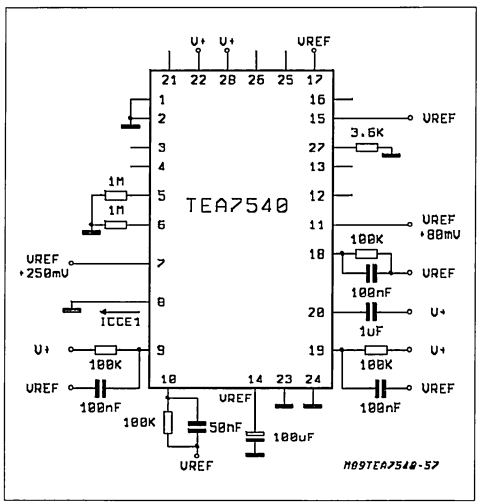
G1min = 20log (VMICOUT / VINE)

Figure 4: Test Configuration



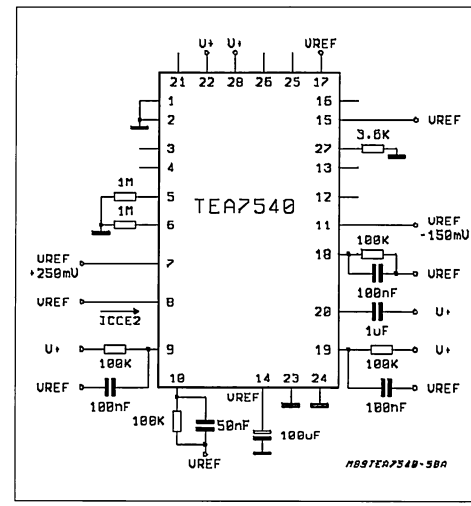
$V^+ = 3V$
pin 7 is forced to transmit mode
Input signal on pin 13 VINE in the compressing range (5mVpp for example)
output voltage VMICOUT measured on pin 12

Figure 5: Test Configuration



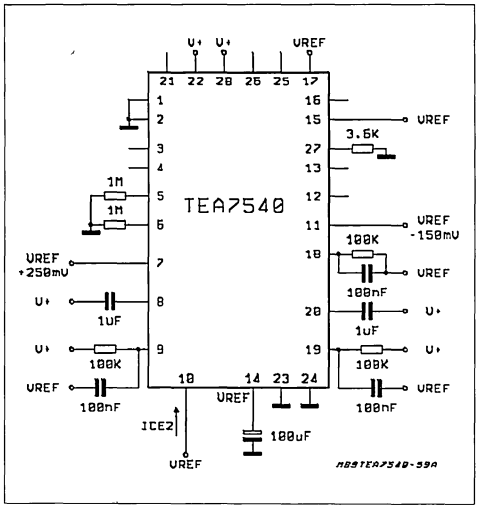
$V^+ = 3V$
pin 7 is forced to transmit mode
pin 11 is forced to maximum gain

Figure 6: Test Configuration



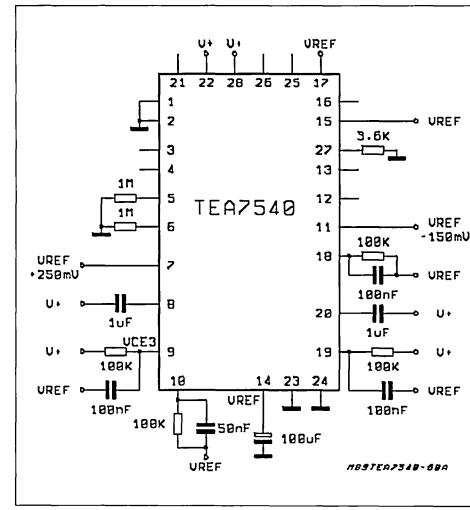
$V^+ = 3V$
pin 7 is forced to transmit mode
pin 11 is forced to minimum gain

Figure 7: Test Configuration



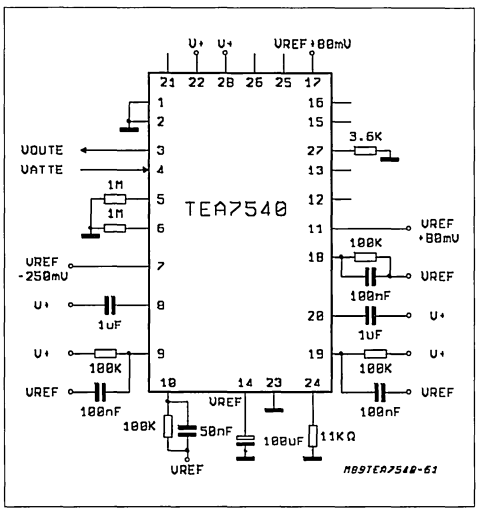
V^+ = 3V
pin 7 is forced to transmit mode
pin 11 is forced to minimum gain

Figure 8: Test Configuration



V^+ = 3V
pin 7 is forced to transmit mode
pin 11 is forced to minimum gain

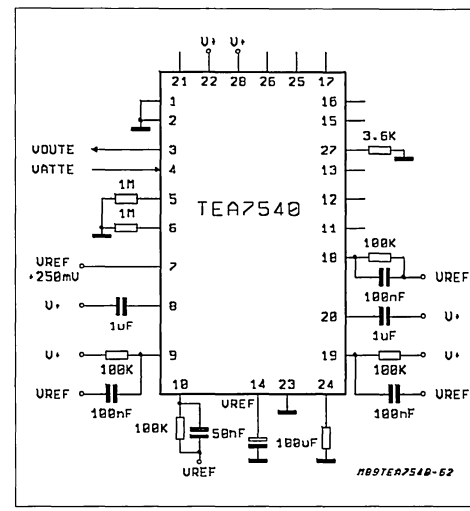
Figure 9: Test Configuration



V^+ = 3V
pin 7 is forced to receive mode
pin 11 and pin 17 are forced to maximum gain
Input signal on pin 4 VATTE = 200mVpp

ATE2 = 20log (VOUTE / VATTE) with Rpin24 = 11KΩ

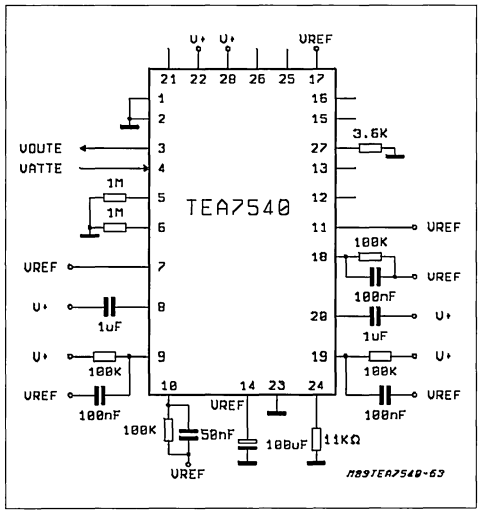
Figure 10: Test Configuration



V^+ = 3V
pin 7 is forced to transmit mode
Input signal on pin 4 VATTE = 200mVpp

ATE = 20log(VOUTE / VATTE)

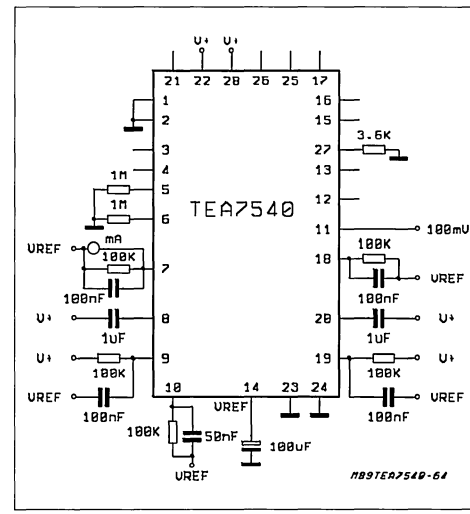
Figure 11: Test Configuration



$V^+ = 3V$
pin 7 is forced to idle mode after that the two compressor have been forced at maximum gain by V11 and V17
Input signal on pin 4 VATTE = 200mVpp
Rpin24 = 11KΩ

ATE6 = 20log(VOUTE / VATTE)

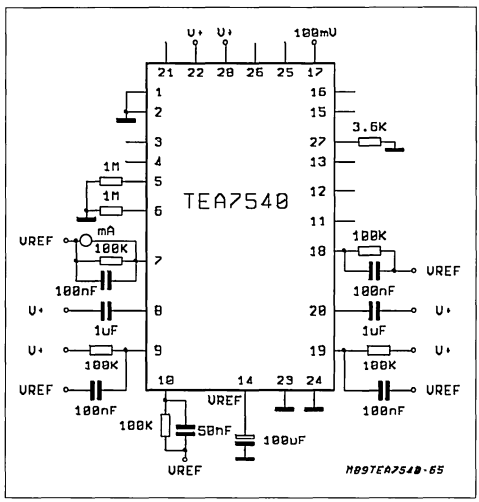
Figure 12: Test Configuration



$V^+ = 3V$
pin 11 is forced to 100mV to force the transmit mode

VTIM_E voltage on pin 7
ITIM_E current through the mA

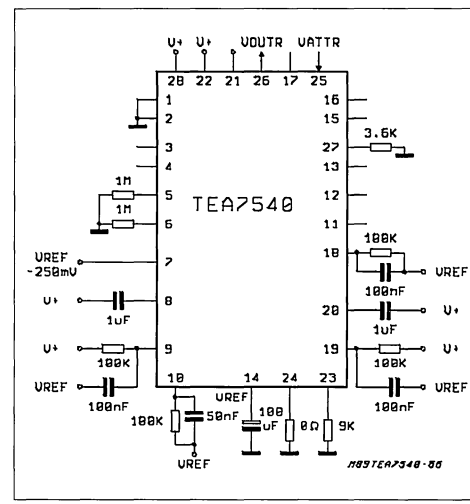
Figure 13: Test Configuration



$V^+ = 3V$
pin 17 is forced to 100mV to force the receive mode

VTIM_R voltage on pin 7
ITIM_R current through the mA

Figure 14: Test Configuration



$V^+ = 3V$
pin 7 is forced to receive mode
Input signal pin 25: VATTR = 200mVpp
Rpin23 = 9KΩ

ATRVOL = 20log(VOUTR / VATTR)

LINE INTERFARCE

DESIGNED TO INTERFACE AN EQUIPMENT WITH THE TELEPHONE LINE, THIS 8 PINS IC PROVIDES :

- LINE ADAPTATION
- RING DETECTION

IT IS PARTICULARLY CONVENIENT FOR MODEM APPLICATIONS AND FULFILLS A WIDE RANGE OF INTERNATIONAL SPECIFICATIONS.

LINE ADAPTATION : (DC CHARACTERISTIC)

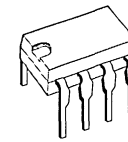
- ZENER CHARACTERISTIC WITH ADJUSTABLE SLOPE
- ADJUSTABLE DYNAMIC IMPEDANCE
- ADJUSTABLE MAXIMUM AMPLITUDE OF THE SIGNAL
- USE ONLY A LOW COST DRY TRANSFORMER
- NEED NO DIALLING RELAY

RING DETECTION :

- ADJUSTABLE DETECTION LEVEL
- ADJUSTABLE AC IMPEDANCE
- VERY LOW LINE DISTORTION
- LOGIC SIGNAL OUTPUT

OTHER :

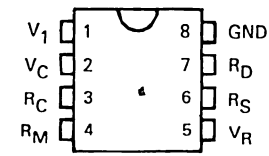
- LOW WORKING VOLTAGE
- WIDE OPERATING CURRENT RANGE



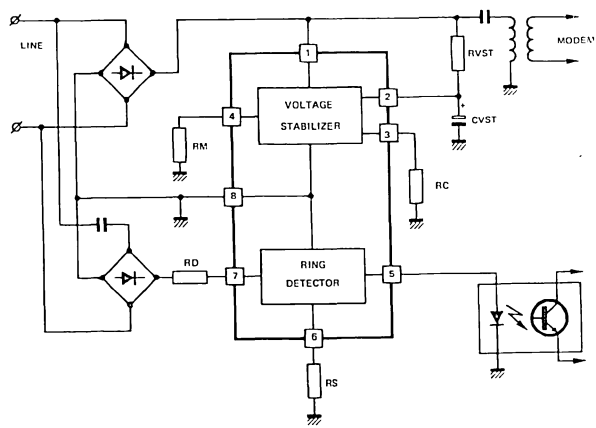
MINIDIP

ORDERING NUMBER : TEA7868DP

PIN CONNECTION (top view)



BLOCK DIAGRAM



VOLTAGE STABILIZER

Name	N°	Description
V_1	1	Voltage over the IC
V_C	2	C_{VST} decouples the voltage stabilizer and R_{VST} fixes the impedance
R_C	3	R_C fixes the voltage through R_{VST}
R_M	4	R_C fixes the slope of DC characteristic
GND	8	Ground

RING DETECTOR

Name	N°	Description
V_R	5	Ring detection output connected to an optocoupling device
R_S	6	R_S fixes the ring detection level
RD	7	Ring Detection Input, R_D fixes the impedance of the ring detector

Outlines

Specially designed for the modem applications, this 8 pins IC provides line adaptation, ring detection and easy pulse dialling. It is a Direct Connect Circuit (DCC) which has been designed to fulfill a wide range of AC and DC specifications for various countries.

Ring Detection

This circuit detects the incoming ringing signal and generates a logic signal to the microcomputer via an optocoupling device. The detection level can be fixed by an external resistor. The dynamic impedance of the ring detector is also fixed by an external resistor. The line distortion of the ringing signal is very low compared to the distortion introduced by a zener detector.

Line Adaptation

The DC characteristic can fulfill a wide range of DC specifications :

- zener characteristic with adjustable slope fixed by an external resistor
- line current limitation using an external CTP.

The dynamic impedance is fixed by an external resistor R_{VST} so as to match with different line impedances.
The maximum amplitude of the signal is fixed by two external resistors R_{VST} and R_C.
This circuit has been designed to be connected to a low cost dry transformer.
The application has been studied to avoid the use of dialling relay.
With its possibility of ring detection, off-hook are dialling this circuit is adapted to the application smart modems. Is also satisfies the FCC Rules Part 68.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_1, V_7	Supply Voltage	16	V
P_{tot}	Power Dissipation	600	mW
T_{oper}	Operating Temperature	-25 to 65	°C
T_{stg}	Storage Temperature	-55 to 150	°C

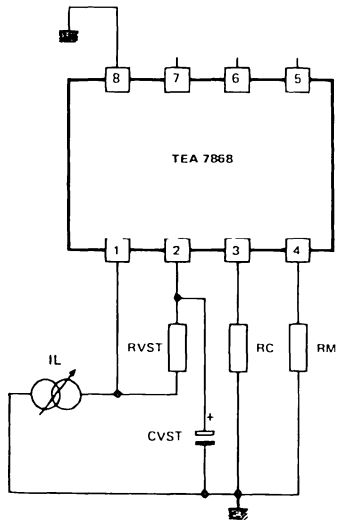
STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_L	Line Current (Pin 1)	10		120	mA
V_1	Voltage over the IC (Pin 1) (see Figure 1)				V
	I_L = 10mA	3.0	3.2	3.4	
	I_L = 100mA	4.3	4.5	4.7	
V_C	Voltage Stabilizer (Pin 2) (see Figure 1)				V
	I_L = 10mA	1.9	2.1	2.3	
	I_L = 100mA	3.2	3.4	3.6	

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

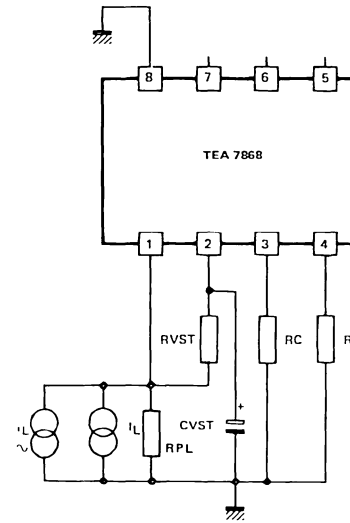
Symbol	Parameter	Min.	Typ.	Max.	Unit
R.L.	Impedance of the Transmission Part. (see Figure 2) Return loss compared to 60Ω : 300Hz < f < 5kHz, I_L = 20mA	15			dB
V_R	Ring Detection Level (see Figure 3) for a Low Level on Pin 5 (< 0.3V) : no Detection for a High Level on Pin 5 (> 0.8V) : Ring Detection	19	20 20	24	V_{PP}
Z_R	Impedance of the Ring Detection Part : Typically $R_S + R_D/13$ (see Figure 3)	9.5	10.5	11.5	kΩ
	Distortion in Ring Mode : f_{RING} = 50Hz (see note 4)				

Figure 1 : Static Electrical Characteristic Test Diagram.



External components :
C_{VST} = 100µF
R_C = 2.7kΩ
R_{VST} = 1.2kΩ
R_M = 12Ω

Figure 2 : Impedance Measurement.



External components :
C_{VST} = 100µF
R_C = 2.7kΩ
RPL = 1200Ω
R_{VST} = 1.2kΩ
R_M = 12Ω

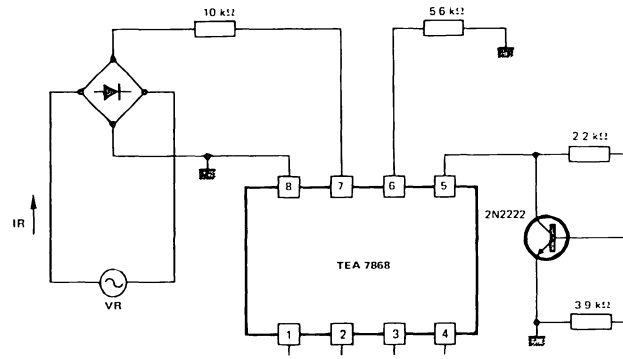
Test conditions :
I_L = 20mA

Return loss defined by :

$$R_L = 20 \log \left(\frac{|Z_{OUT} + 600|}{|Z_{OUT} - 600|} \right)$$

$$Z_{OUT} = \frac{V_1}{I_L}$$

Figure 3 : Ring Detection Level and Impedance.



Test Conditions :

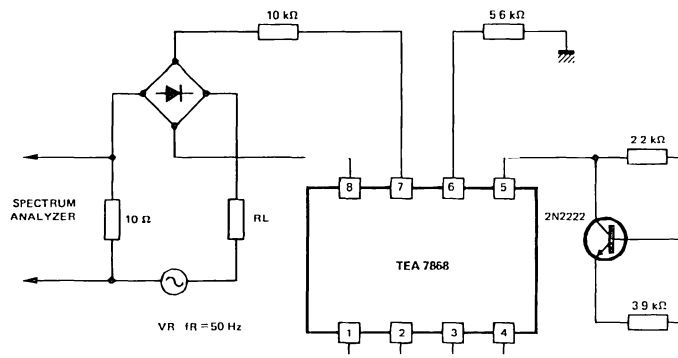
Ring detection level
for : V_R = 18V_{PP} V(5) < 0 3V
for : V_R = 22V_{PP} V(5) > 0 8V

Impedance of the ring detection part

$$ZR = \frac{V_R}{I_R}$$

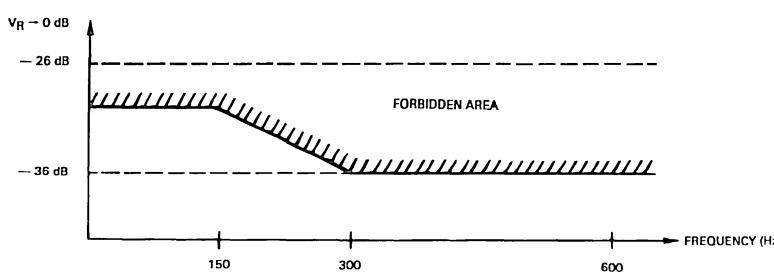
Figure 4 : Ring Detection Distortion.

a)



Test conditions : V_R = 90V_{RMS}, 300Ω < R_L < 1400Ω
No distortion peaks appear in the forbidden area of the following shape :

b)



APPLICATIONS INFORMATION

Rin Detection (see Figure 5)

The ringing signal coming from the line is rectified by the diode bridge ; the circuit compares the peak amplitude of the signal to a predeterminated detection level fixed by R_S. On the output transistor of the optocoupling device a logic signal is generated which frequency is twice the frequency of the ringing signal.

"0" = the amplitude of the ringing signal is greater than the detection level.
"1" = the amplitude of the ringing signal is lower than the detection level.

The ring detection circuit is fully linear ; so the distortion on the line is very low compared to the distorsion introduced by a zener detector as usually used.

Three external components affect the characteristic of the ring detection circuit. The capacitor C_R provides the DC solation from the line.

The AC impedance of the circuit at the ringing frequency is given by the formula :

$$Z_{AC} = Z_{CR}(f) + R_D + R_S/13$$

Z_{CR} is the impedance of the capacitor C_R at the ringing frequency.

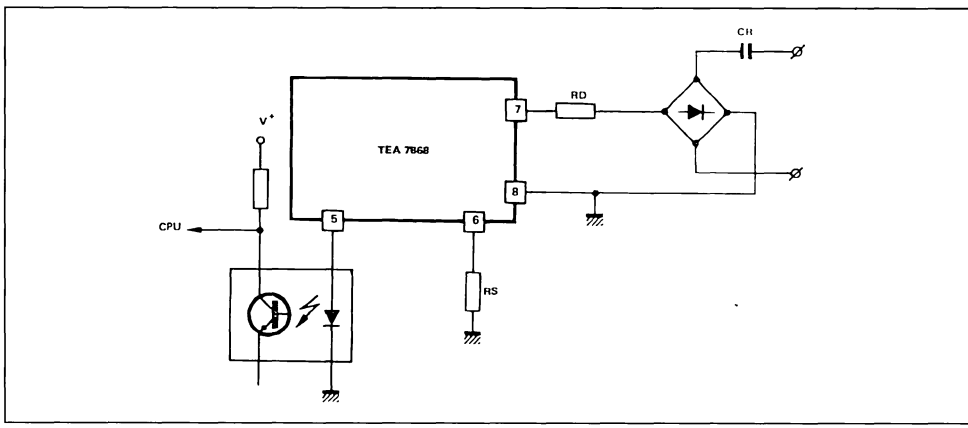
The ring detection level is fixed by the external resistor R_S with the following formula :

$$R_S = \frac{11 \text{ volts}}{V_R - V_D - 3 \text{ volts}} R_D$$

V_R is the peak amplitude of the ringing signal at the detection level.

V_D is the voltage over the diode bridge and the capacitor C_R at the ringing frequency.

Figure 5



AC/DC Line Adaptation (see Figure 6)

This part of the TEA7868 is used for line adaptation
An Equivalent Diagram of the Circuit is given at Figure 7.

Figure 6

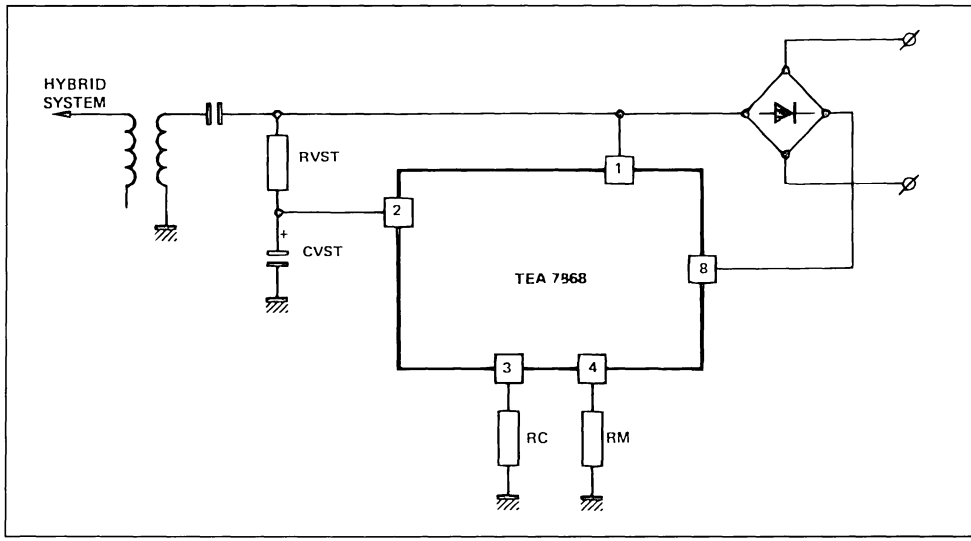
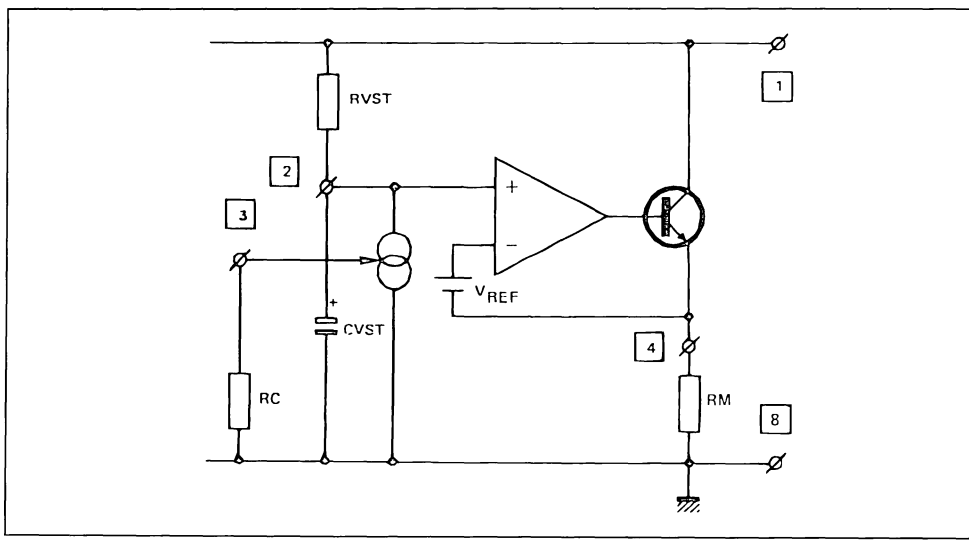


Figure 7

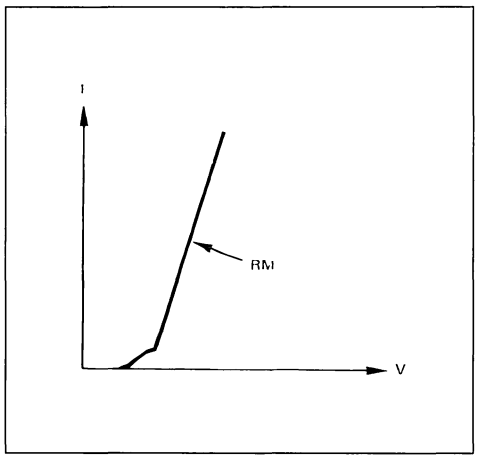


The DC characteristic is a zener characteristic which slope is fixed by R_M (see Figure 8). The voltage over the circuit (pin 1) is fixed via a current source driven through R_{VST}. The value of this current source is fixed by the external resistor R_C with the formula :

$$V(R_{SVST}) = V_1 - V_2 = \frac{R_{VST}}{R_C} \times 2.45 \text{ volts}$$

Note that the voltage through R_{VST} also limits the amplitude of the emitted signal.

Figure 8



The external resistor R_{VST} also defines the AC impedance of the circuit : Z_{AC} = R_{VST} / / impedance seen from the transformer (see hybrid system)

* When a current limitation is required for the DC characteristic (as for the French specification), an external TPE is connected between the telephone line and the circuit (see application diagram).

Pulse Dialling

Pulse dialling is easily done using a high voltage optocoupling device and a high voltage PNP transistor as shown on the typical application diagram.

Hybrid System

This system uses an operational amplifier to prevent from injecting the emitted signal in the receiving path of the modem IC. A typical diagram is given at Figure 9.

R_L represents the impedance of the telephone line Z_L in parallel with R_{VST}. Typically we take $Z_L = 600\Omega$.

The hybrid gain of the system is given by :

$$G_D = \frac{V_S}{V_E} = 1 - \frac{R_2 + R_3}{R_2} \frac{R_1}{R_1 + R_L}$$

For a maximum efficiency you must have $G_D = 0$ and this gives :

$$\frac{R_3}{R_2} = \frac{R_L}{R_1}$$

The impedance seen from the line must be 600 ohms, this impedance is given by :

$$Z_{out} = R_1 \,//\, R_{VST}$$

So, if R_{VST} is fixed, R_1 is also fixed by $Z_{out} = 600\Omega$.

The gain between the online signal and the modem input is :

$$G_E = \frac{R_L}{R_1 + R_L}$$

The gain between the line and the modem input is :

$$G_R = 1 + \frac{R_3}{R_2}$$

Those calculations are purely theoretical ; really the line impedance has a complex component, so there will be little changes in the value of R_1, R_2, R_3 to adapt the hybrid system.

Figure 9

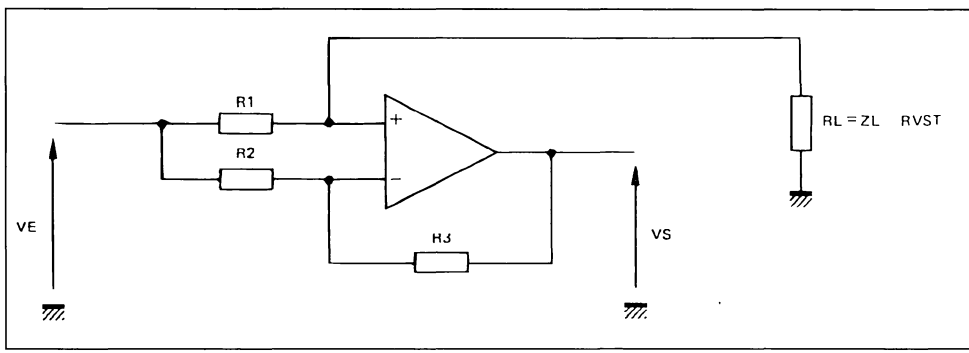
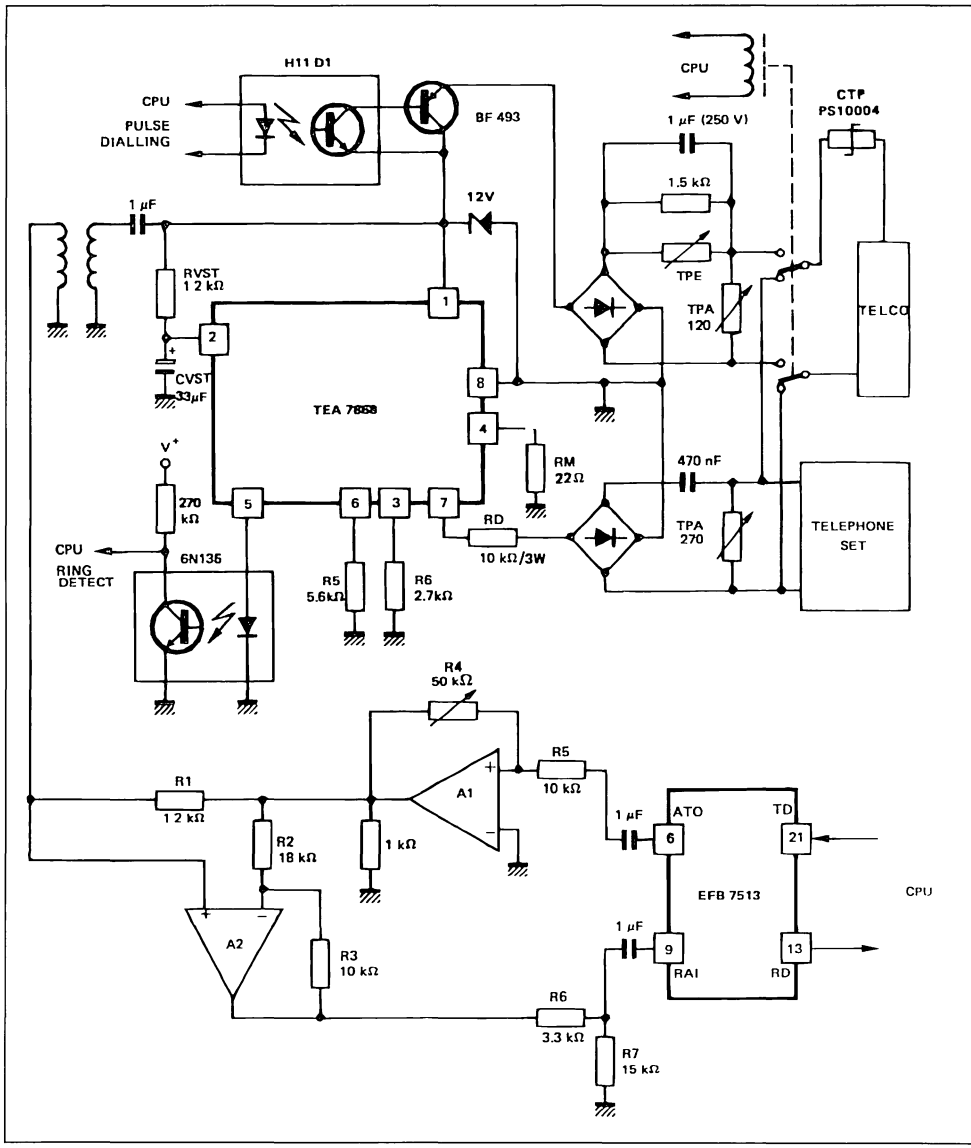


Figure 10 : Complete DAA Interface Circuit with TEA7868.



DEDICATED MCUs

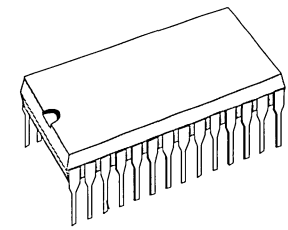
SGS-THOMSON MICROELECTRONICS

ST6294

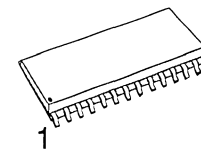
8-BIT HCMOS MCU WITH A/D CONVERTER, EEPROM & AUTO-RELOAD TIMER

For complete specifications refer to "DEDICATED MCU FAMILY for Telephone Set App." (1Q'94)

- 3 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -25 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User ROM: 3868 bytes
- Data ROM: User selectable size (in program ROM)
- Data RAM: 128 bytes
- EEPROM: 128 bytes
- PDIP28, PSO28 packages
- 21 fully software programmable I/O as:
  - Input with pull-up resistor
  - Input without pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull outputs
  - Analog Inputs
- 8 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (Timer1)
- 8 bit auto-reload timer with 7-bit programmable prescaler (AR Timer)
- Digital Watchdog
- 8 bit A/D Converter with up to 13 analog inputs
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator (Quartz Crystal or Ceramic)
- Power-on Reset
- Clock output
- 9 powerful addressing modes
- The development tool of the ST6294 microcontrollers consists of the ST626x-EMU emulation and development system connected via a standard RS232 serial line to an MS-DOS Personal Computer



PDIP28



PSO28

October 1993

Figure 1. ST6294 Pin Configuration

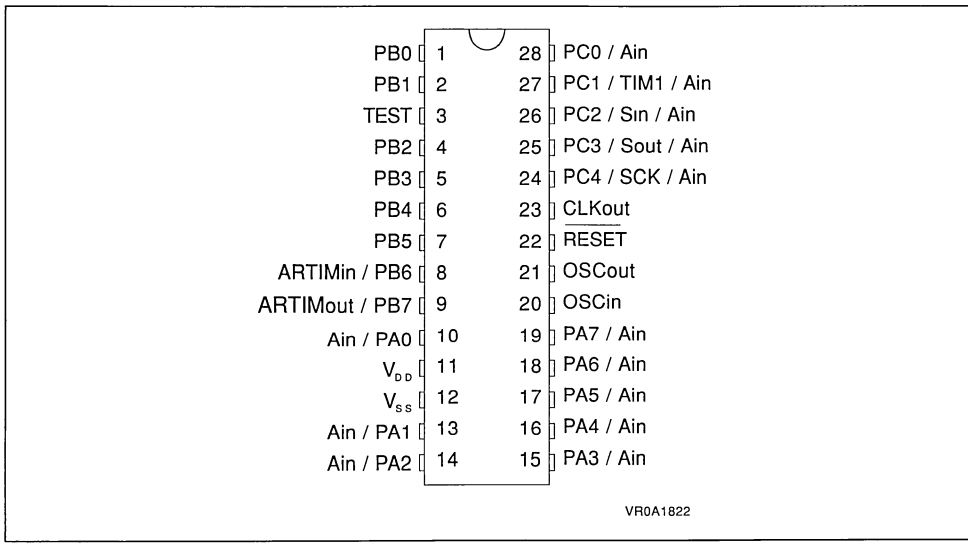
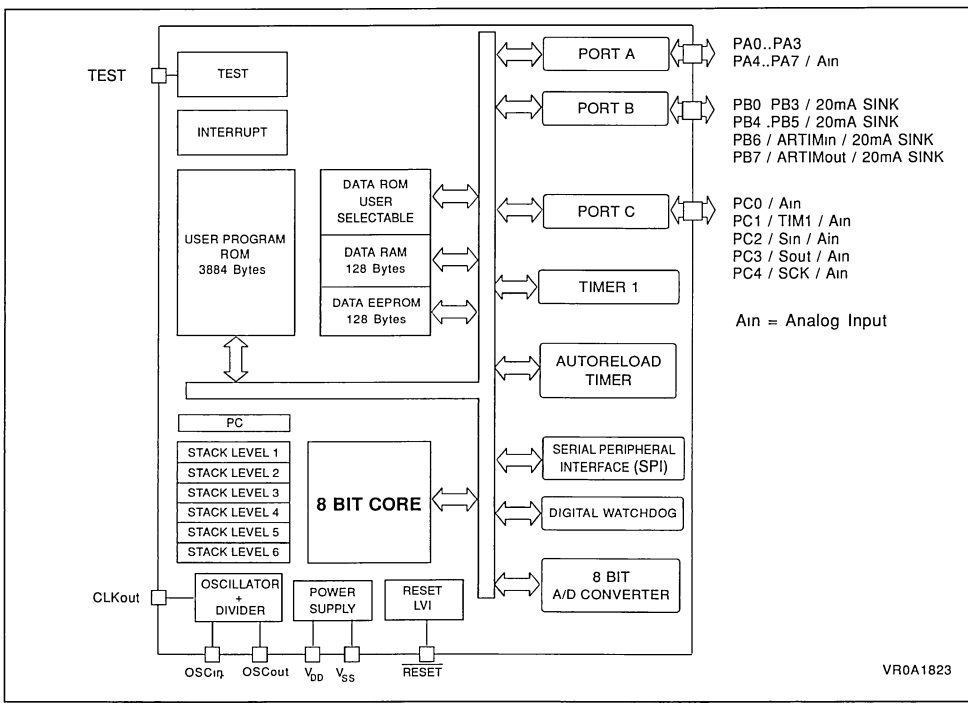


Figure 2. ST6294 Block Diagram



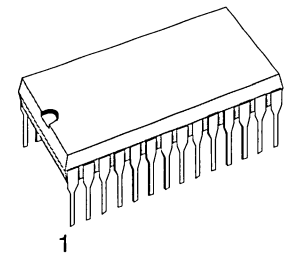
SGS-THOMSON MICROELECTRONICS

ST62E94, T94

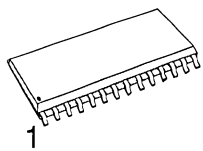
8-BIT EPROM HCMOS MCUs WITH A/D CONVERTER, EEPROM & AUTORELOAD TIMER

For complete specifications refer to "DEDICATED MCU FAMILY for Telephone Set App." (1Q'94)

- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -25 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User EPROM: 3868 bytes
  Data ROM: User selectable size (in program EPROM)
  Data RAM: 128 bytes
  EEPROM: 128 bytes
- PDIP28, PSO28 (ST62T94) packages
- CDIP28W (ST62E94) packages
- 21 fully software programmable I/O as:
  – Input with pull-up resistor
  – Input without Pull-up resistor
  – Input with interrupt generation
  – Open-drain or push-pull outputs
  – Analog Inputs
- 8 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (Timer1)
- 8 bit Autoreload timer with 7-bit programmable prescaler (AR Timer)
- Digital Watchdog
- 8 bit A/D Converter with up to analog inputs
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator (Quartz or Ceramic)
- Power-on Reset
- Clock output
- 9 powerful addressing modes

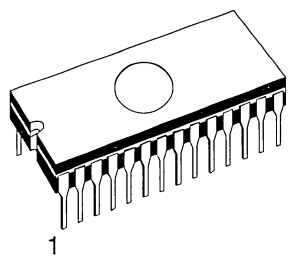


PDIP28



PSO28

EPROM PACKAGES



CDIP28W

The ST62E94 is the EPROM version; ST62T94 is the OTP version; both are fully compatible with ST6294 ROM version.

October 1993

Figure 1. ST62E94/T94 Pin Configuration

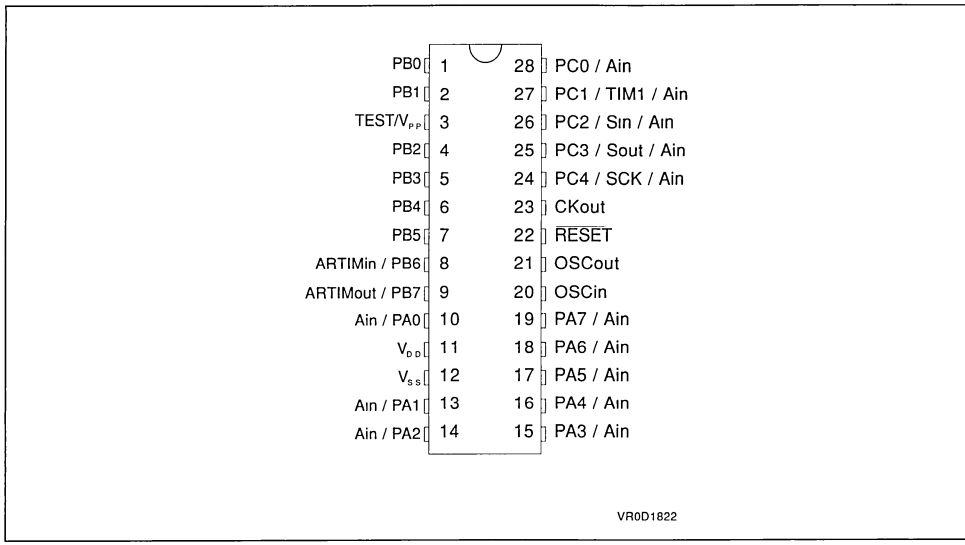
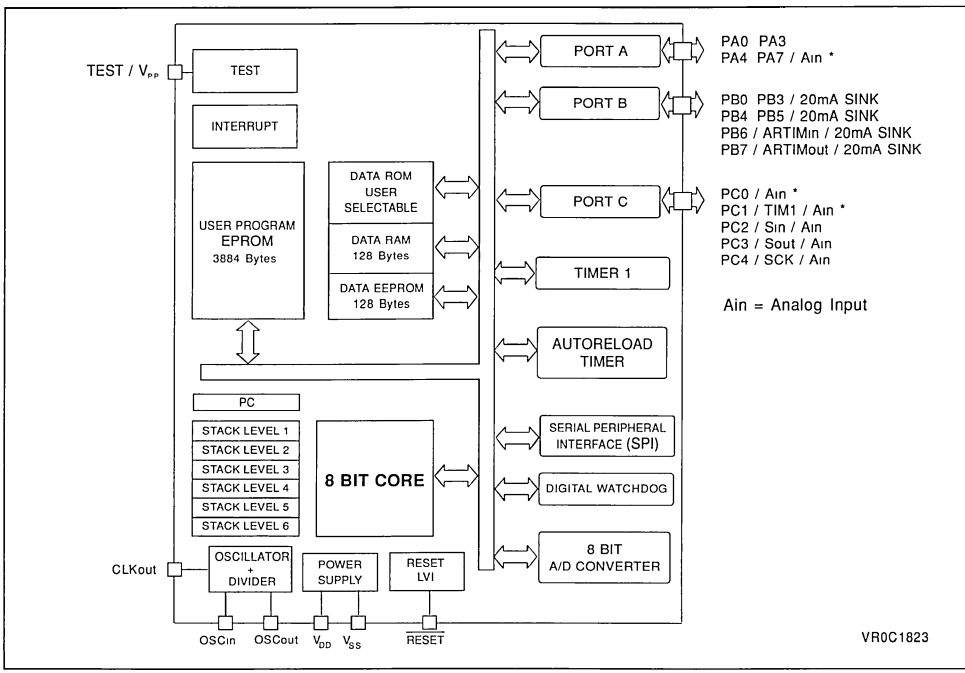


Figure 2. ST62E94 Block Diagram



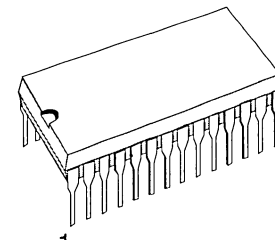
SGS-THOMSON MICROELECTRONICS

ST7291

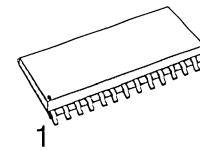
8-BIT HCMOS MCUs WITH 16K ROM AND WAKE-UP FUNCTION

For complete specifications refer to "DEDICATED MCU FAMILY for Telephone Set App." (1Q'94)

- 3 to 5.5V supply operating range
- 8MHz Maximum Clock Frequency
- Fully static operation
- 0 to +70°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention Modes
- User ROM: 16K bytes
- Data RAM: 256 bytes
- 28 pin Dual In Line and SO plastic packages
- 19 bidirectional I/O lines
- 8 lines programmable as interrupt wake-up inputs
- 16-bit timer with one output compare (without output pin).
- Interrupt Wake-up function
- Low voltage detector
- Master Reset and power on reset
- Full Hardware Emulator
- 8-bit data manipulation
- 74 basic instructions
- 10 main addressing modes
- 8x8 unsigned multiply instruction
- True bit manipulation
- Complete development support on real time emulator with PC/DOS
- Full software package (Cross Assembler, debugger)

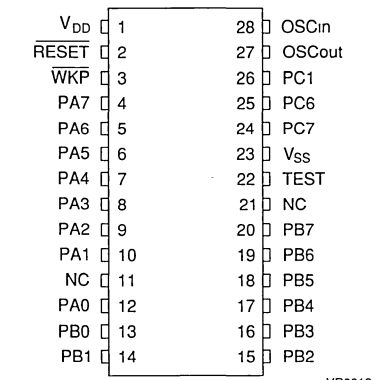


PDIP28



PSO28

PIN DESCRIPTION

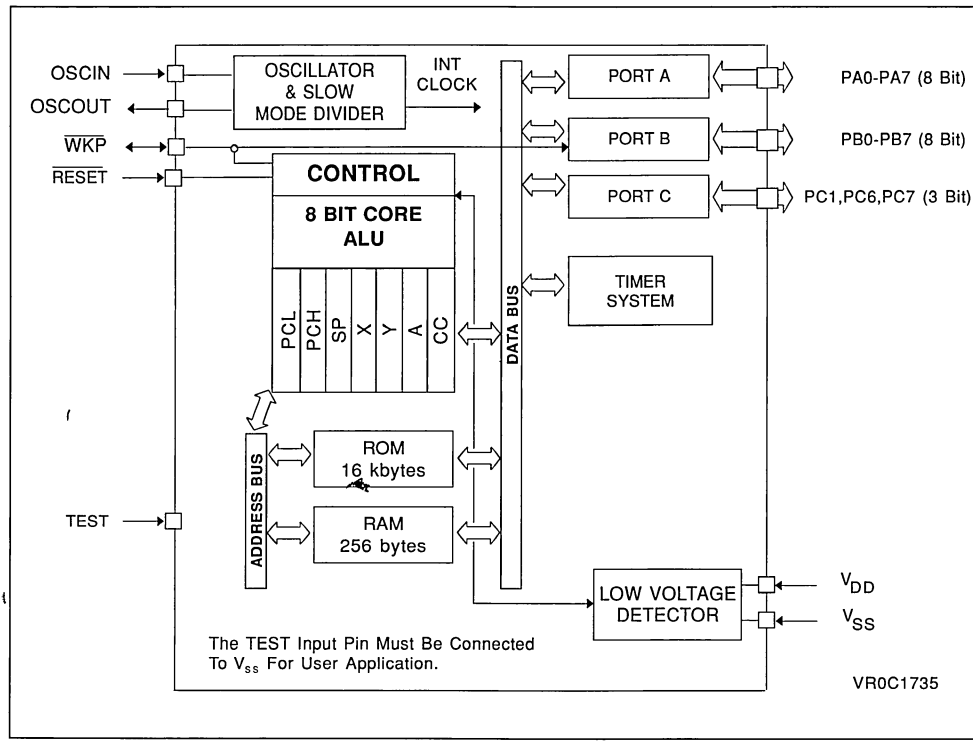


November 1993

INTRODUCTION

The ST7291 is a HCMOS microcontroller unit (MCU) from the ST72 family. It is based around an industry standard 8 bit core and offers an enhanced instruction set. The processor runs with an external clock at 8 MHz with a 5V supply and 4MHz with a 3.3V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST7291 can be placed in WAIT or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8 bit data management the ST7291 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes an on-chip oscillator, CPU, ROM, RAM, I/O, one timer with one output compare system, and a low voltage detector.

Figure 1. ST7291 Block Diagram



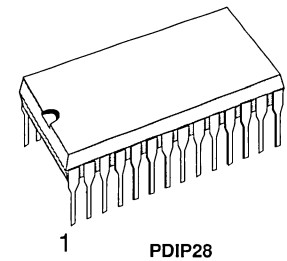
SGS-THOMSON MICROELECTRONICS

ST7293

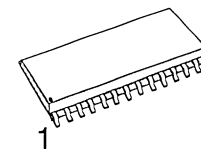
8-BIT HCMOS MCUs WITH EEPROM

For complete specifications refer to "DEDICATED MCU FAMILY for Telephone Set App." (1Q'94)

- 2.5 to 5.5V supply operating range
- 4MHz Maximum Clock Frequency
- Fully static operation
- -25 to +85°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention Modes
- User ROM: 3328 bytes
- Data RAM: 128 bytes
- EEPROM: 128 bytes
- 28 pin Dual In Line and SO plastic packages
- 22 bidirectional I/O lines
- 6 lines programmable as interrupt wake-up inputs
- 16-bit timer with 1 input capture and 2 output compares
- Master Reset and power on reset
- Full Hardware Emulator
- User mask options:
  - internal clock for timer (÷ 2,÷ 4,÷ 8)
  - pinout for ICAP and OCMP1 signals
  - enable wake-up function on PORT C
  - open drain on PORT A
  - Watchdog enable/disable after Reset
  - Watchdog state during WAIT mode
- 8-bit data manipulation
- 74 basic instructions
- 9 main addressing modes
- 8x8 unsigned multiply instruction
- true bit manipulation
- Complete development support on real time emulator with PC/DOS
- Full software package (Cross Assembler, debugger)

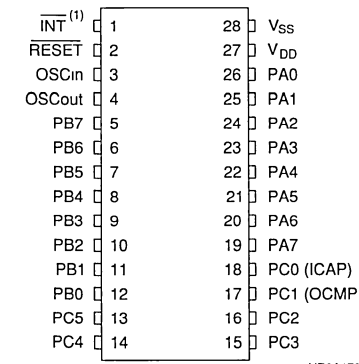


PDIP28



PSO28

PIN DESCRIPTION



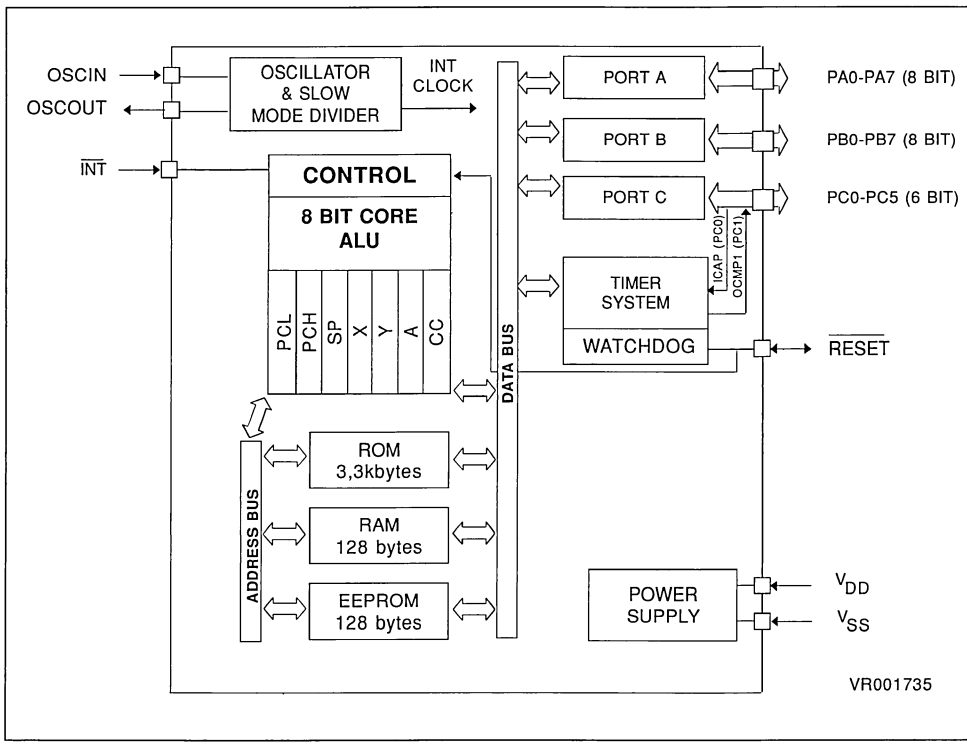
Note 1. This pin is also the VPP input for EPROM based devices

November 1993

INTRODUCTION

The ST7293 is a HCMOS microcontroller unit (MCU) from the ST72 family. It is based around an industry standard 8 bit core and offers an enhanced instruction set. The processor runs with an external clock at 4 MHz with a 5V supply and 2MHz with a 3V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST7293 can be placed in WAIT or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8 bit data management the ST7293 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes an on-chip oscillator, CPU, ROM, RAM, EEPROM, I/O, and one timer with 1 input capture and 2 output compare systems.

Figure 1. ST7293 Block Diagram



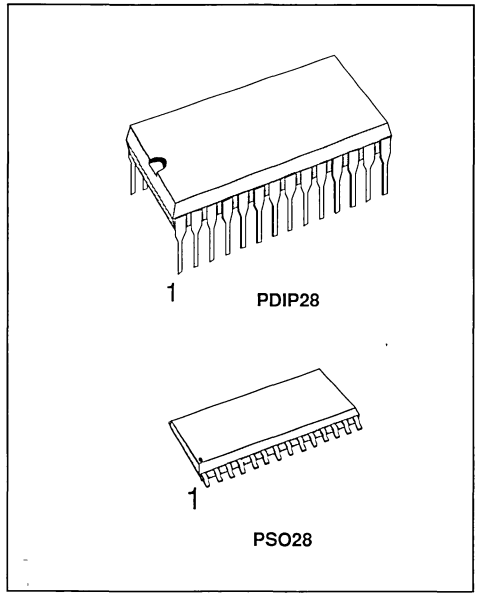
SGS-THOMSON MICROELECTRONICS

ST7294

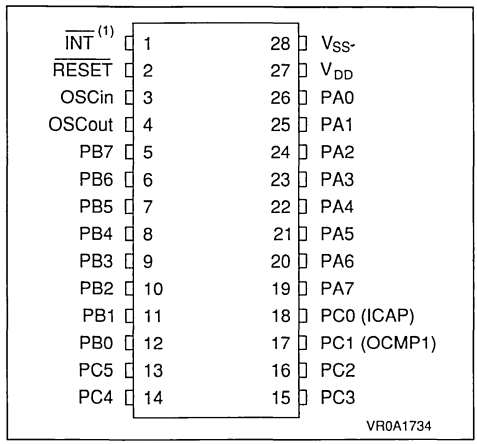
8-BIT HCMOS MCUs WITH EEPROM

For complete specifications refer to "DEDICATED MCU FAMILY for Telephone Set App." (1Q'94)

- 2.5 to 5.5V supply operating range
- 4MHz Maximum Clock Frequency
- Fully static operation
- -25 to +85°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention Modes
- User ROM: 6144 bytes
  Data RAM: 224 bytes
  EEPROM: 256 bytes
- 28 pin Dual In Line and SO plastic packages
- 22 bidirectional I/O lines
- 6 lines programmable as interrupt wake-up inputs
- 16-bit timer with 1 input capture and 2 output compares
- 2V RAM retention mode
- Master Reset and power on reset
- Full Hardware Emulator
- User mask options:
  - internal clock for timer (÷ 2,÷ 4,÷ 8)
  - pinout for ICAP and OCMP1 signals
  - enable wake-up function on PORT C
  - open drain on PORT A
  - pull-up on PORT A and PORT B
  - Watchdog enable/disable after Reset
  - Watchdog enable during WAIT mode
- 8-bit data manipulation
- 74 basic instructions
- 10 main addressing modes
- 8x8 unsigned multiply instruction
- true bit manipulation
- Complete development support on real time emulator with PC/DOS
- Full software package (Cross Assembler, debugger)



Pin Configuration



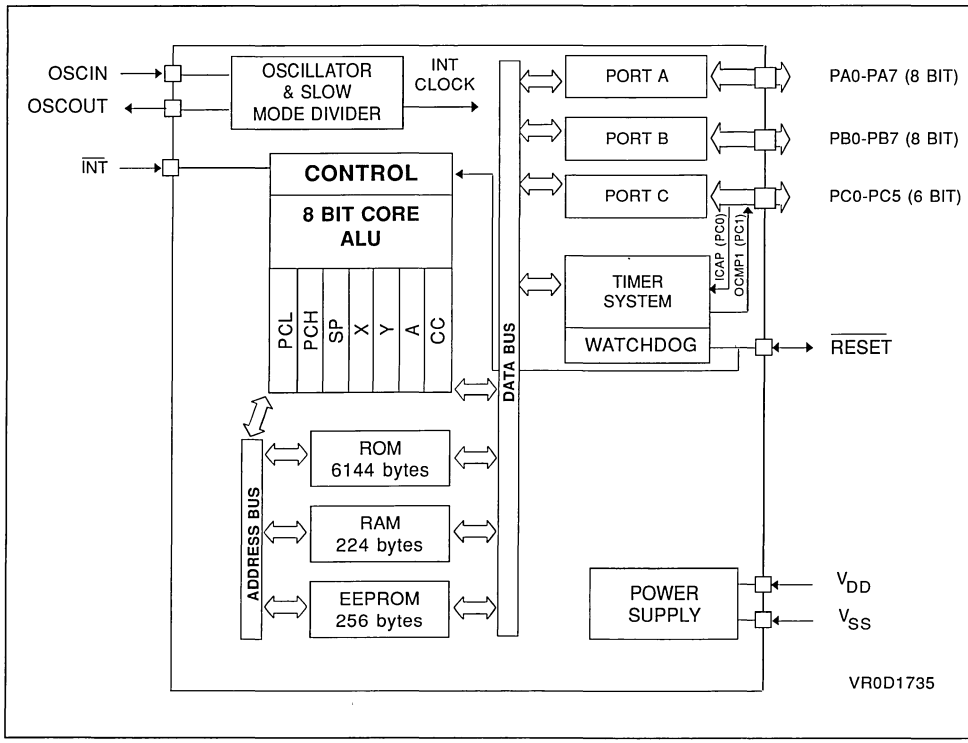
Note 1. This pin is also the VPP input for EPROM based devices

October 1993

INTRODUCTION

The ST7294 is a HCMOS microcontroller unit (MCU) from the ST72 family. It is based around an industry standard 8 bit core and offers an enhanced instruction set. The processor runs with an external clock at 4 MHz with a 5V supply and 2MHz with a 3V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST7294 can be placed in WAIT or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8 bit data management the ST7294 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes an on-chip oscillator, CPU, ROM, RAM, EEPROM, I/O, and one timer with 1 input capture and 2 output compare systems.

Figure 1. ST7294 Block Diagram



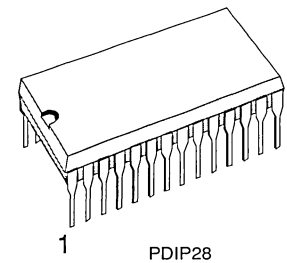
SGS-THOMSON MICROELECTRONICS

ST72E94
ST72T94

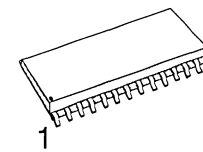
8-BIT EPROM HCMOS MCUs WITH EEPROM

For complete specifications refer to "DEDICATED MCU FAMILY for Telephone Set App." (1Q'94)

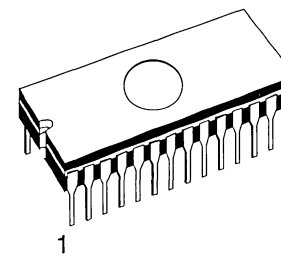
- 3V to 5.5V supply operating range
- 4MHz Maximum Clock Frequency
- Fully static operation
- -25 to +85°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention Modes
- User EPROM: 7168 bytes
  Data RAM: 224 bytes
  EEPROM: 256 bytes
- 28-pin Plastic Dual In Line and SO package for ST72T94 OTP version
- 28-pin Ceramic Dual In Line package for ST72E94 EPROM version
- 22 bidirectional I/O lines
- 6 lines programmable as interrupt wake-up inputs
- 16-bit timer with 1 input capture and 2 output compares
- 2V RAM retention mode
- Master Reset and power on reset
- Full Hardware Emulator
- Compatible with ST7294 (6K) and ST7293 (3.3K) ROM devices
- 8-bit data manipulation
- 74 basic instructions
- 10 main addressing modes
- 8x8 unsigned multiply instruction
- true bit manipulation
- Complete development support on real time emulator with PC/DOS
- Full software package (Cross Assembler, debugger)



PDIP28



PSO28



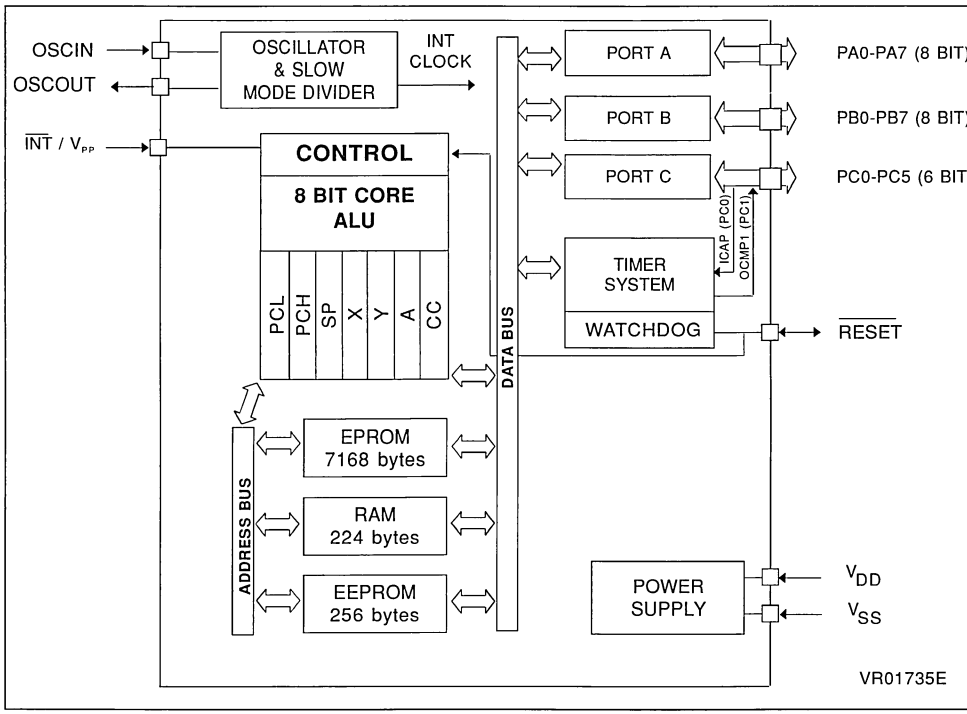
CDIP28

October 1993

INTRODUCTION

The ST72E94 and ST72T94 (following mentioned as ST72E94) are EPROM members with EEPROM of the ST72 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developped and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process.The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices. **THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST7294 ROM-BASED DEVICE FOR FURTHER DETAILS.**

Figure 1. ST72E94 Block Diagram



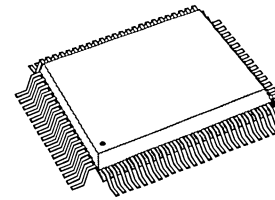
The EPROM ST72E94 may be used for the prototyping and the pre-production phases of development, can be configured as either a standalone microcontroller with 7K bytes of on-chip ROM, either as a microcontroller able to manage external memory.

The ST72E94 is a HCMOS microcontroller unit (MCU) from the ST72 family. It is based around an industry standard 8 bit core and offers an enhanced instruction set. The processor runs with an external clock at 4 MHz with a 5V supply and 2MHz with a 3V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST72E94 can be placed in WAIT or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8 bit data management the ST72E94 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes an on-chip oscillator, CPU, EPROM, RAM, EEPROM, I/O, and one timer with 1 input capture and 2 output compare systems.

STATIC ANSWERING AND RECORDING CHIP

For complete specifications refer to "DEDICATED MCU FAMILY for Telephone Set App." (1Q'94)

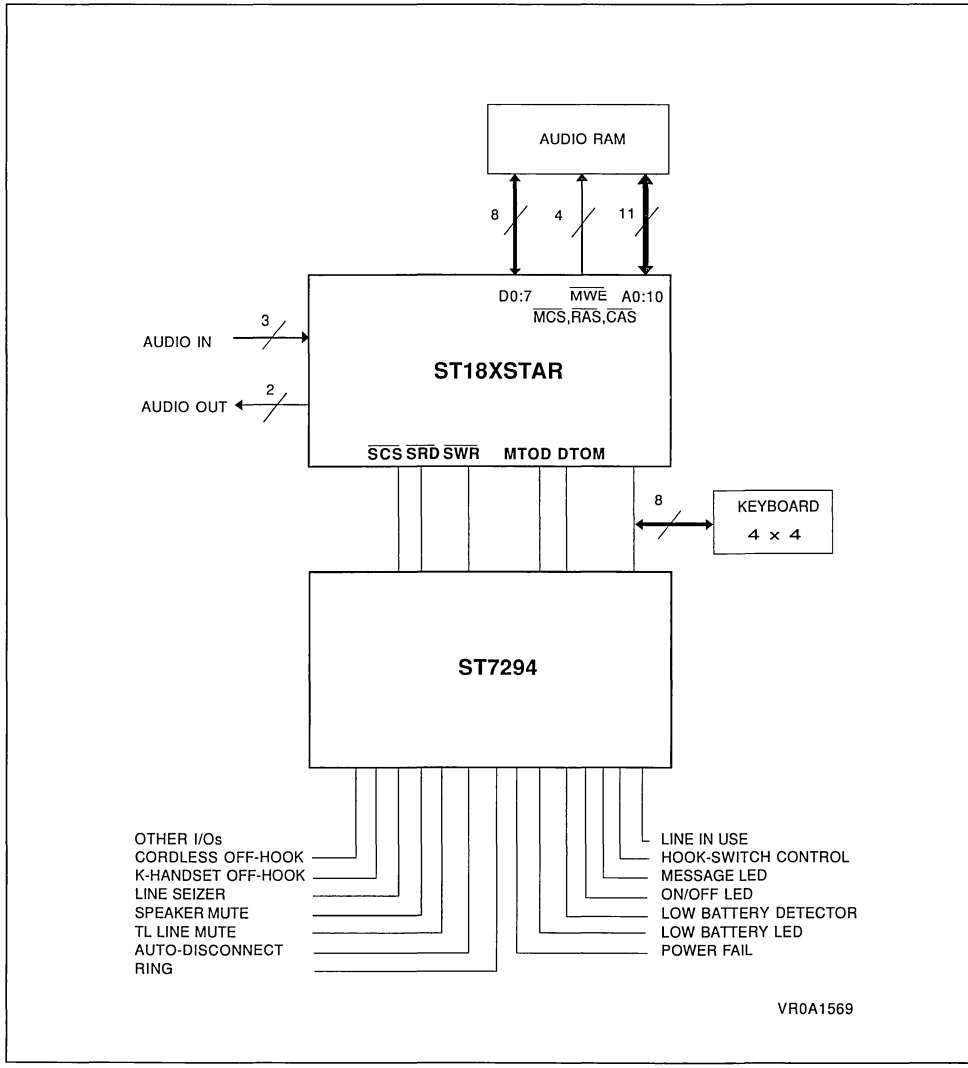
The ST18XSTAR is a high quality low bit rate speech synthesis and recording system. Using ACELP type algorithms for voice compression at 4800bps, it offers the most competitive compromise between speech quality and memory size. It also includes voice synthesis capability, generated from a non volatile memory to produce predefined messages. Including tone and DTMF detectors for remote control operation, it is suitable for use in answering machines, answering telephone sets, cordless answering telephone sets,voice mail systems and memo recorders.



PQFP100

- Low bit rate (4.8kbps) speech coding and decoding system.
- Ultra low bit variable rate (<1.5kbps) speech synthesis message capability.
- Voice storage memory capability up to 32Mbits.
- Integrated implementation on one **D**igital **S**ignal **P**rocessor (DSP) chip.
- Low power design:
  - Single 5V power supply,
  - Maximum active power consumption 500mW,
  - Sleep power Mode 1.5mA for ARAM refresh.
- Reduced size and power consumption suitable for standard voice answering and recording machines, cordless phones with voice recording capability, memo recorders.
- Maximum flexibility provided with emulation ROMless version ST18RXSTAR.
- Extended modes of operations and features :
  - Fast and slow read/skip modes. Messages monitoring.
  - Voice messages for remote operation through telephone line.
  - Possible use of SRAMs, DRAMs, ROMs or EPROMs.
  - Advanced error correction algorithms allowing use of ARAMs.
  - Programmable call progress and call waiting tone generators/detectors including DTMF,comply with PAA/TPA/AGH/1764 specifications.
  - Programmable voice activity detection for silence compression.
  - Programmable output attenuation level (for remote call screening).
  - Wide dynamic range (48dB).
  - PCM 64Kbps coding mode for high-quality incoming/outgoing messages.
- Versatile Interfaces
  - 3 to 1 muxed single-ended A/D input.
  - 2 D/A independently programmable output drivers.
  - On-chip converters.
  - Host processor parallel interface.

Microcontroller Interface typical application example.

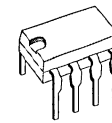


STANDARD LINEAR ICs

LOW NOISE DUAL OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- LOW VOLTAGE NOISE : **4.5nV/√Hz**
- HIGH GAIN BANDWIDTH PRODUCT : **15MHz**
- HIGH SLEW RATE : **7V/µs**
- LOW DISTORTION : 0.002%
- EXCELLENT FREQUENCY STABILITY
- ESD PROTECTION 2kV



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

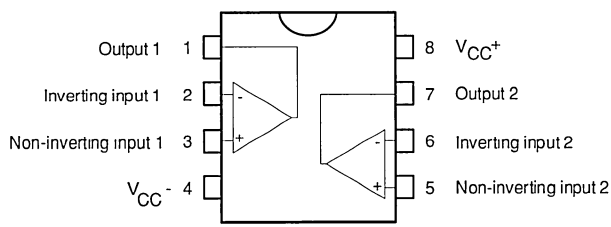
The LM833 is a monolithic dual operational amplifier dedicated to audio applications. The LM833 offers low voltage noise (4.5nV/√Hz) and high frequency performances (15MHz gain bandwidth product, 7V/µs slew rate).
In addition the LM833 has also a very low distortion (0.002%) and excellent phase/gain margins.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
LM833	-40, +105°C	•	•

833-01.TBL

PIN CONNECTIONS (top view)

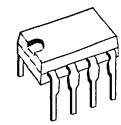


833-01.EPS

HIGH PERFORMANCE DUAL OPERATIONAL AMPLIFIERS

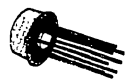
For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)



H
TO99
(Metal Can)

DESCRIPTION

The LS204 is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products.

The circuit presents very stable electrical characteristics over the entire supply voltage range, and is particularly intended for professional and telecom applications (active filters, etc).

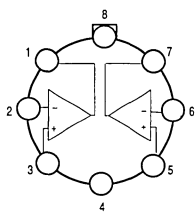
ORDER CODES

Part Number	Temperature Range	Package		
		H	N	D
LS204C	0°C, +70°C	•	•	•
LS204I	-40°C, +105°C	•	•	•
LS204M	-55°C, +125°C	•	•	•

204-01 TBL

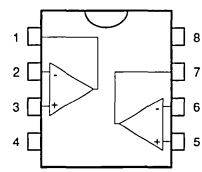
PIN CONNECTIONS (top views)

TO99



204-01.EPS

DIP8/SO8



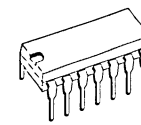
204-02.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output
8 - V_{CC}^+

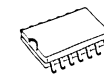
HIGH PERFORMANCE QUAD OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

The LS404 is a high performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products.

The circuit presents very stable electrical characteristics over the entire supply voltage range, and it particularly intended for professional and telecom applications (active filters, etc).

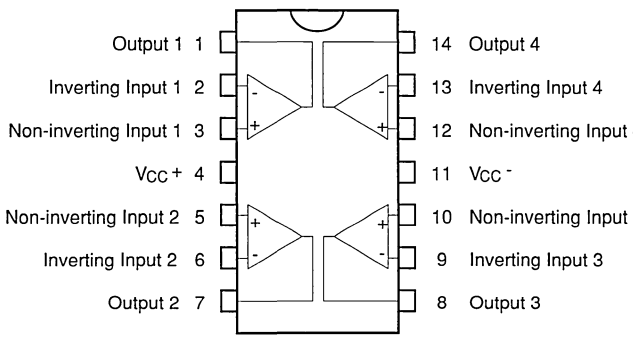
The patented input stage circuit allows small input signal swings below the negative supply voltage and prevents phase inversion when the inputs is over driver.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
LS404C	0°C, +70°C	•	•
LS404I	-40°C, +105°C	•	•
LS404M	-55°C, +125°C	•	•

404-01.TBL

PIN CONNECTIONS (top view)



404-01.EPS

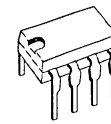
SGS-THOMSON MICROELECTRONICS

MC33078

LOW NOISE DUAL OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- LOW VOLTAGE NOISE : **4.5nV/√Hz**
- HIGH GAIN BANDWIDTH PRODUCT : **15MHz**
- HIGH SLEW RATE : **7V/µs**
- LOW DISTORTION : 0.002%
- LARGE OUTPUT VOLTAGE SWING +14.3V/-14.6V
- LOW INPUT OFFSET VOLTAGE
- EXCELLENT FREQUENCY STABILITY
- ESD PROTECTION 2kV



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

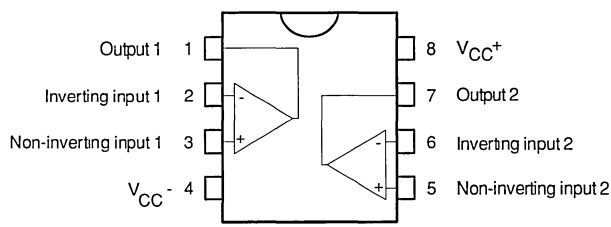
The MC33078 is a monolithic dual operational amplifier dedicated to audio applications. The MC33078 offers low voltage noise (4.5nV/√Hz) and high frequency performances (15MHz gain bandwidth product, 7V/µs slew rate).
In addition the MC33078 has a very low distortion (0.002%) and excellent phase/gain margins.
The output stage allows a large output voltage swing and symmetrical source and sink currents.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
MC33078	-40, +105°C	•	•

33078-01.TBL

PIN CONNECTIONS (top view)



33078-01.EPS

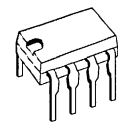
SGS-THOMSON MICROELECTRONICS

MC33171 - MC35171

LOW POWER SINGLE BIPOLAR OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- GOOD CONSUMPTION/SPEED RATIO : ONLY 200µA FOR 2.1MHz, 2V/µs
- SINGLE (OR DUAL) SUPPLY OPERATION FROM +4V TO +44V (±2V TO ±22V)
- WIDE INPUT COMMON MODE VOLTAGE RANGE INCLUDING V_{CC}^-
- LOW LEVEL OUTPUT VOLTAGE CLOSE TO V_{CC}^-: 100mV TYPICAL
- PIN TO PIN COMPATIBLE WITH STANDARD SINGLE OP AMPs



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The MC33171 series are single bipolar operational amplifiers offering both low consumption (200µA) and good speed (2.1MHz, 2V/µs).

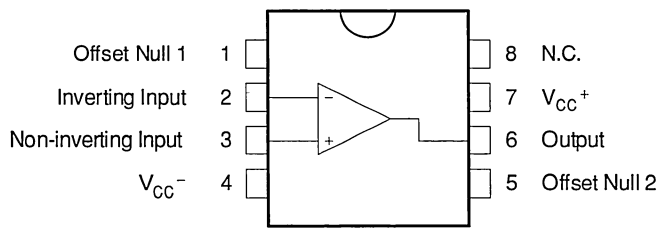
Moreover the Input Common Mode Range extends down to the lower supply rail, allowing single supply operation from +4V to +44V.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
MC33171	-40°C, +105°C	•	•
MC35171	-55°C, +125°C	•	•
Example: MC33171N			

33171-01.TBL

PIN CONNECTIONS (top view)



33171-01.EPS

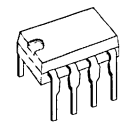
SGS-THOMSON MICROELECTRONICS

MC33172 - MC35172

LOW POWER DUAL BIPOLAR OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- GOOD CONSUMPTION/SPEED RATIO : ONLY 200µA/Amp FOR 2.1MHz, 2V/µs
- SINGLE (OR DUAL) SUPPLY OPERATION FROM +4V TO +44V (±2V TO ±22V)
- WIDE INPUT COMMON MODE VOLTAGE RANGE INCLUDING V_{CC}^-
- LOW LEVEL OUTPUT VOLTAGE CLOSE TO V_{CC}^- : 100mV TYPICAL
- PIN TO PIN COMPATIBLE WITH STANDARD DUAL OP AMPs



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The MC33172 series are dual bipolar operational amplifiers offering both low consumption (200µA/Amp) and good speed (2.1MHz, 2V/µs).

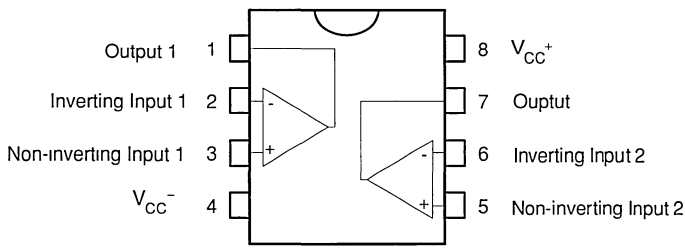
Moreover the Input Common Mode Range extends down to the lower supply rail, allowing single supply operation from +4V to +44V.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
MC33172	-40°C, +105°C	•	•
MC35172	-55°C, +125°C	•	•
Example: MC33172N			

33172-01.TBL

PIN CONNECTIONS (top view)



33172-01.EPS

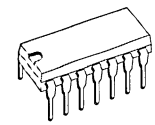
SGS-THOMSON MICROELECTRONICS

MC33174 - MC35174

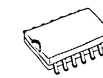
LOW POWER QUAD BIPOLAR OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- GOOD CONSUMPTION/SPEED RATIO : ONLY 200µA/Amp FOR 2.1MHz, 2V/µs
- SINGLE (OR DUAL) SUPPLY OPERATION FROM +4V TO +44V (±2V TO ±22V)
- WIDE INPUT COMMON MODE VOLTAGE RANGE INCLUDING V_{CC}^-
- LOW LEVEL OUTPUT VOLTAGE CLOSE TO V_{CC}^-: 100mV TYPICAL
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP AMPs
- ESD PROTECTION



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

The MC33174 series are quad bipolar operational amplifiers offering both low consumption (200µA/Amp) and good speed (2.1MHz, 2V/µs).

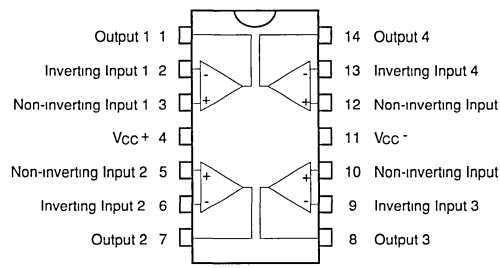
Moreover the Input Common Mode Range extends down to the lower supply rail, allowing single supply operation from +4V to +44V.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
MC33174	-40°C, +105°C	•	•
MC35174	-55°C, +125°C	•	•
Example: MC33174N			

33174-01.TBL

PIN CONNECTIONS (top view)

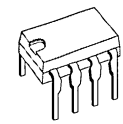


33174-01.EPS

DUAL BIPOLAR OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

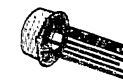
- LOW DISTORTION RATIO
- LOW NOISE
- VERY LOW SUPPLY CURRENT
- LOW INPUT OFFSET CURRENT
- VERY LOW INPUT OFFSET VOLTAGE
- LARGE COMMON-MODE RANGE
- HIGH GAIN
- HIGH OUTPUT CURRENT
- GAIN-BANDWIDTH PRODUCT : 2.5MHz
- TEMPERATURE DRIFT : 2μV/°C
- LONG TERM STABILITY : 8μV/YEAR (for $T_{amb} \leq 50°C$)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

J
CERDIP8
(Cerdip Package)



H
TO99
(Metal Can)

DESCRIPTION

The TEB1033, TEF1033 and TEC1033 are high performance dual-operational amplifiers intended for active filter applications. The internal phase compensation allows stable operation as voltage follower in spite of their high gain-bandwidth products.

The circuits present very stable electrical characteristics over the entire supply voltage range.

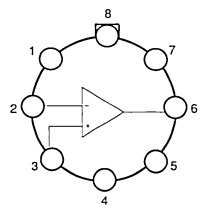
ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
TEB1033	0°C, +70°C	•	•	•	•
TEF1033	–40°C, +105°C	•	•	•	•
TEC1033	–55°C, +125°C	•	•	•	•
Example : TEB1033N					

1033-01 TBL

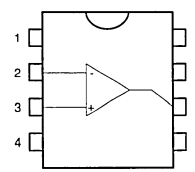
PIN CONNECTIONS (top views)

TO99



1033-01.EPS

DIP8/SO8
CERDIP8



1033-02.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

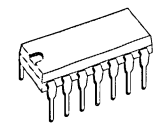
SGS-THOMSON MICROELECTRONICS

TEB4033
TEF4033-TEC4033

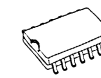
QUAD BIPOLAR OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- LOW DISTORTION RATIO
- LOW NOISE
- VERY LOW SUPPLY CURRENT
- LOW INPUT OFFSET CURRENT
- VERY LOW INPUT OFFSET VOLTAGE
- LARGE COMMON-MODE RANGE
- HIGH GAIN
- HIGH OUTPUT CURRENT
- GAIN-BANDWIDTH PRODUCT : 2.5MHz
- TEMPERATURE DRIFT : 2µV/°C
- LONG TERM STABILITY : 8µV/YEAR (for $T_{amb} \leq 50°C$)



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

DESCRIPTION

The TEB4033, TEF4033 and TEC4033 are high performance quad-operational amplifiers intended for active filter applications. The internal phase compensation allows stable operation as voltage follower in spite of their high gain-bandwidth products.

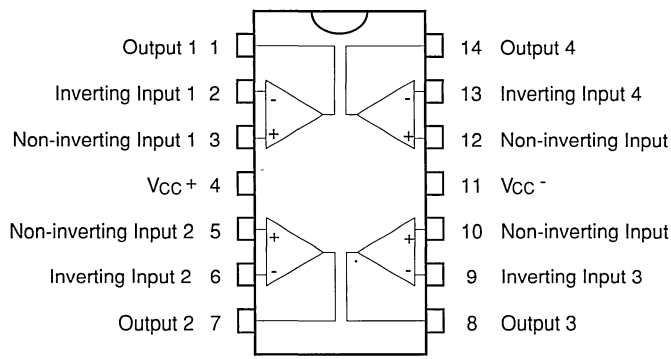
The circuits present very stable electrical characteristics over the entire supply voltage range.

ORDER CODES

Part Number	Temperature Range	Package		
		N	J	D
TEB4033	0°C, +70°C	•	•	•
TEF4033	–40°C, +105°C	•	•	•
TEC4033	–55°C, +125°C	•	•	•
Example : TEB4033N				

4033-01 TBL

PIN CONNECTIONS (top view)



4033-01 EPS

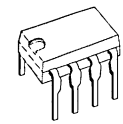
SGS-THOMSON MICROELECTRONICS

TS27L2C,I,M

VERY LOW POWER DUAL CMOS OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD DUAL OP-AMPs (TL082 -LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS27L2C/AC/BC	0°C, +70°C	•	•
TS27L2I/AI/BI	-40°C, +105°C	•	•
TS27L2M/AM/BM	-55°C, +125°C	•	•
Example : TS27L2ACN			

27L2-01.TBL

DESCRIPTION

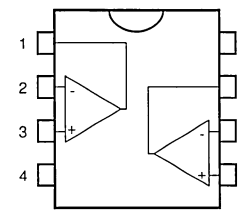
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L2 (very low power)
- I_{CC}= 150µA/amp. : TS27M2 (low power)
- I_{CC}= 1mA/amp. : TS272 (high speed)

These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

PIN CONNECTIONS (top view)



1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{cc}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{cc}^+

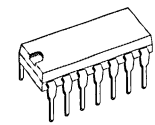
27L2-01 EPS

TS27L4C,I,M

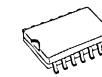
VERY LOW POWER QUAD CMOS OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS27L4C/AC/BC	0°C, +70°C	•	•
TS27L4I/AI/BI	-40°C, +105°C	•	•
TS27L4M/AM/BM	-55°C, +125°C	•	•
Example : TS27L4ACN			

27L4-01.TBL

DESCRIPTION

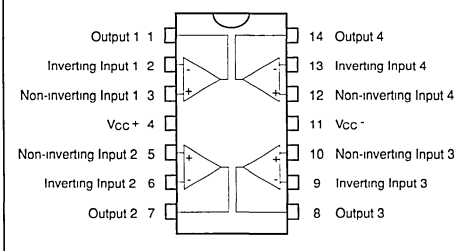
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L4 (very low power)
- I_{CC}= 150µA/amp. : TS27M4 (low power)
- I_{CC}= 1mA/amp. : TS274 (high speed)

These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

PIN CONNECTIONS (top view)



27L4-01.EPS

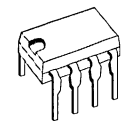
SGS-THOMSON MICROELECTRONICS

TS27M2C,I,M

LOW POWER DUAL CMOS OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD DUAL OP-AMPs (TL082 -LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS27M2C/AC/BC	0°C, +70°C	•	•
TS27M2I/AI/BI	-40°C, +105°C	•	•
TS27M2M/AM/BM	-55°C, +125°C	•	•
Example : TS27M2ACN			

27M2-01.TBL

DESCRIPTION

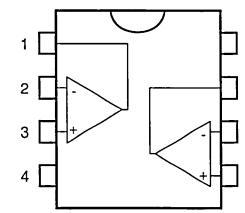
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon-gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L2 (very low power)
- I_{CC}= 150µA/amp. : TS27M2 (low power)
- I_{CC}= 1mA/amp. : TS272 (high speed)

These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

PIN CONNECTIONS (top view)



1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

27M2-01.EPS

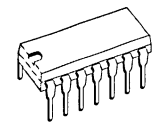
SGS-THOMSON MICROELECTRONICS

TS27M4C,I,M

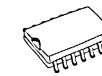
LOW POWER QUAD CMOS OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS27M4C/AC/BC	0°C, +70°C	●	●
TS27M4I/AI/BI	-40°C, +105°C	●	●
TS27M4M/AM/BM	-55°C, +125°C	●	●
Example : TS27M4ACN			

27M4-01.TBL

DESCRIPTION

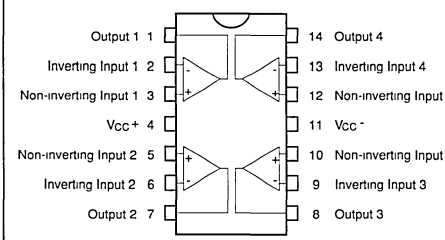
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L4 (very low power)
- I_{CC}= 150µA/amp. : TS27M4 (low power)
- I_{CC}= 1mA/amp. : TS274 (high speed)

These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

PIN CONNECTIONS (top view)



27M4-01.EPS

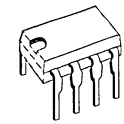
SGS-THOMSON MICROELECTRONICS

TS271C,I,M

PROGRAMMABLE SINGLE CMOS OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- OFFSET NULL CAPABILITY (by external compensation)
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- THE TRANSFER FUNCTION IS LINEAR
- CONSUMPTION CURRENT AND DYNAMIC PARAMETERS ARE STABLE REGARDING THE VOLTAGE POWER SUPPLY VARIATIONS
- DYNAMIC CHARACTERISTICS ADJUSTABLE BY I_{SET}
- VERY LARGE I_{SET} RANGE
- PIN TO PIN COMPATIBLE WITH SINGLE OPERATIONAL AMPLIFIER UA776
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS271C/AC/BC	0°C, +70°C	•	•
TS271I/AI/BI	-40°C, +105°C	•	•
TS271M/AM/BM	-55°C, +125°C	•	•
Example : TS271ACN			

271-01.TBL

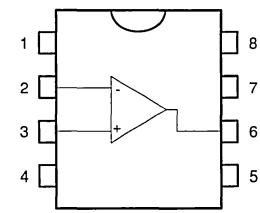
DESCRIPTION

The TS271 is a low cost, low power single operational amplifier designed to operate with single or dual supplies. This operational amplifier uses the SGS-THOMSON silicon gate LIN MOS process giving it an excellent consumption-speed ratio. This amplifier is ideally suited for low consumption applications.

The power supply is externally programmable with a resistor connected between pins 8 and 4. It allows to choose the best consumption-speed ratio and supply current can be minimized according to the required speed. This device is specified for the following I_{SET} current values : 1.5µA, 25µA, 130µA.

This CMOS amplifier offers very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 3).

PIN CONNECTIONS (top view)



1 - Offset Null 1
2 - Inverting Input
3 - Non-inverting Input
4 - V_{CC}^-
5 - Offset Null 2
6 - Output
7 - V_{CC}^+
8 - I_{SET}

271-01.EPS

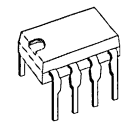
SGS-THOMSON MICROELECTRONICS

TS272C,I,M

HIGH SPEED DUAL CMOS OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD DUAL OP-AMPs (TL082 -LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS272C/AC/BC	0°C, +70°C	•	•
TS272I/AI/BI	-40°C, +105°C	•	•
TS272M/AM/BM	-55°C, +125°C	•	•
Example : TS272ACN			

272-01.TBL

DESCRIPTION

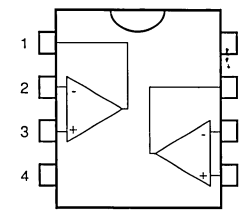
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L2 (very low power)
- I_{CC}= 150µA/amp. : TS27M2 (low power)
- I_{CC}= 1mA/amp. : TS272 (high speed)

These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

PIN CONNECTIONS (top view)



1 - Output 1
2 - Inverting Input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

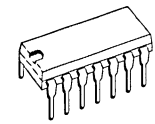
272-01.EPS

TS274C,I,M

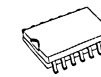
HIGH SPEED QUAD CMOS OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS274C/AC/BC	0°C, +70°C	•	•
TS274I/AI/BI	-40°C, +105°C	•	•
TS274M/AM/BM	-55°C, +125°C	•	•
Example : TS274ACN			

274-01.TBL

DESCRIPTION

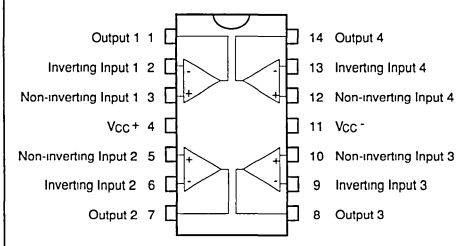
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

- I_{CC}= 10µA/amp. : TS27L4 (very low power)
- I_{CC}= 150µA/amp. : TS27M4 (low power)
- I_{CC}= 1mA/amp. : TS274 (high speed)

These CMOS amplifiers offer very high input impedance and extremely low input currents.
The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

PIN CONNECTIONS (top view)

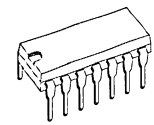


274-01.EPS

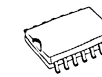
MICROPOWER QUAD CMOS VOLTAGE COMPARATORS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- EXTREMELY LOW SUPPLY CURRENT : 9µA TYP / COMPARATOR
- WIDE SINGLE SUPPLY RANGE (3V TO 16V) OR DUAL SUPPLIES (±1.5V TO ±8V)
- EXTREMELY LOW INPUT BIAS CURRENT : 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1pA TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 1.5µs TYP FOR 5mV OVERDRIVE
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM339



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

The TS339 is a micropower CMOS quad voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM339). Similar performances are offered by the quad micropower comparator TS3704 with a push-pull CMOS output.

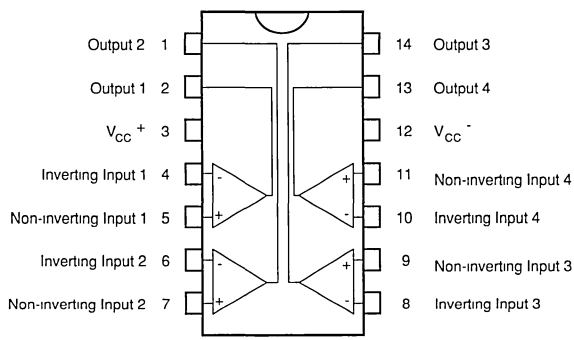
Thus response times remain similar to the LM339.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS393C	0°C, +70°C	•	•
TS393I	-40°C, +105°C	•	•
TS393M	-55°C, +125°C	•	•
Example : TS393CN			

339-01.TBL

PIN CONNECTIONS (top view)

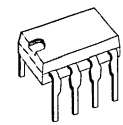


339-01.EPS

MICROPOWER DUAL CMOS VOLTAGE COMPARATORS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- EXTREMELY LOW SUPPLY CURRENT : 9µA TYP/COMPARATOR
- WIDE SINGLE SUPPLY RANGE (3V to 16V) OR DUAL SUPPLIES (±1.5V to ±8V)
- EXTREMELY LOW INPUT BIAS CURRENT : 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1pA TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 2.5µs TYP FOR 5mV OVERDRIVE
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM393



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The TS393 is a micropower CMOS dual voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM393). Similar performances are offered by the dual micropower comparator TS3702 with a push-pull CMOS output.

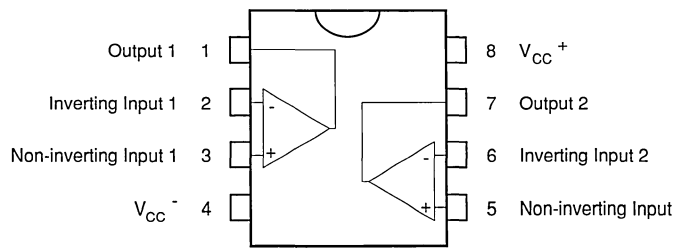
Thus response times remain similar to the LM393.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS393C	0°C, +70°C	•	•
TS393I	-40°C, +105°C	•	•
TS393M	-55°C, +125°C	•	•
Example : TS393CN			

393-01.TBL

PIN CONNECTIONS (top view)



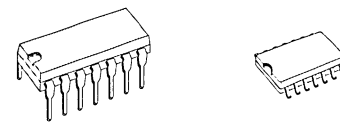
393-01.EPS

INPUT/OUTPUT **RAIL TO RAIL** DUAL CMOS OPERATIONAL AMPLIFIER (WITH **STANDBY** POSITION)

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- **RAIL TO RAIL** INPUT AND OUTPUT VOLTAGE RANGES
- **STANDBY** POSITION : REDUCED **CONSUMPTION (1µA)** AND **HIGH IMPEDANCE OUTPUTS**
- SINGLE (OR DUAL) SUPPLY OPERATION FROM **2.7V TO 16V** (±1.35V to ±8V)
- EXTREMELY LOW INPUT BIAS CURRENT : **1pA** TYP
- LOW INPUT OFFSET VOLTAGE : **5mV max.**
- SPECIFIED FOR **600Ω** AND **100Ω** LOADS
- LOW SUPPLY CURRENT : 400µA/Ampli
- SPEED : 1.3MHz - 1.3V/µs

- SPICE MACROMODEL INCLUDED IN THIS SPECIFICATION



N
DIP14
(Plastic Package)

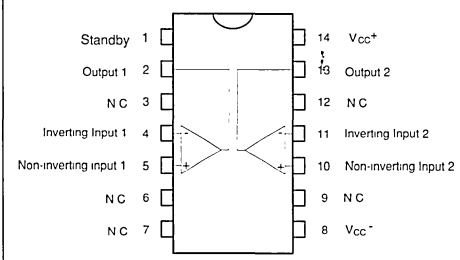
D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS902I/AI	-40, +105°C	•	•

902 01 TDL

PIN CONNECTIONS (top view)



902-01 EPS

DESCRIPTION

The TS902 is a RAIL TO RAIL dual CMOS operational amplifier designed to operate with single or dual supply voltage.

The input voltage range V_{Icm} includes the two supply rails V_{CC}^+ and V_{CC}^-.

The output reaches :

- V_{CC}^- +50mV V_{CC}^+ -50mV with $R_L = 10k\Omega$
- V_{CC}^- +650mV V_{CC}^+ -650mV with $R_L = 600\Omega$

This product offers a broad supply voltage operating range from 2.7V to 16V and a supply current of only 400µA/amp. (V_{CC} = 10V).

Source and sink output current capability is typically 50mA (at V_{CC} = 10V), fixed by an internal limitation circuit.

The TS902 can be put on STANDBY position by connecting the pin 1 to V_{CC}^- (only 1µA and high impedance outputs).

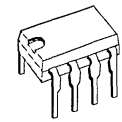
SGS-THOMSON MICROELECTRONICS

TS912

INPUT/OUTPUT **RAIL TO RAIL** DUAL CMOS OPERATIONAL AMPLIFIER

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- **RAIL TO RAIL** INPUT AND OUTPUT VOLTAGE RANGES
- SINGLE (OR DUAL) SUPPLY OPERATION FROM **2.7V TO 16V** (±1.35V to ±8V)
- EXTREMELY LOW INPUT BIAS CURRENT : **1pA** TYP
- LOW INPUT OFFSET VOLTAGE : **5mV max.**
- SPECIFIED FOR **600Ω** AND **100Ω** LOADS
- LOW SUPPLY CURRENT : 400µA/Ampli
- SPEED : 1.3MHz - 1.3V/µs
- SPICE MACROMODEL INCLUDED IN THIS SPECIFICATION



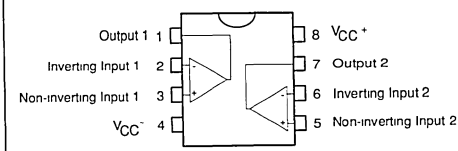
N
DIP8
(Plastic Package)

ORDER CODES

Part Number	Temperature Range	Package
		N
TS912I/AI	-40, +105°C	•

912-01 TBL

PIN CONNECTIONS (top view)



912-01 EPS

DESCRIPTION

The TS912 is a RAIL TO RAIL dual CMOS operational amplifier designed to operate with single or dual supply voltage.
The input voltage range V_{icm} includes the two supply rails V_{CC}^+ and V_{CC}^-.
The output reaches :

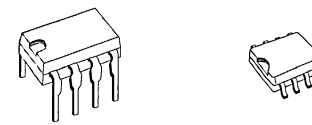
- V_{CC}^- +50mV V_{CC}^+ -50mV with R_L = 10kΩ
- V_{CC}^- +650mV V_{CC}^+ -650mV with R_L = 600Ω

This product offers a broad supply voltage operating range from 2.7V to 16V and a supply current of only 400µA/amp. (V_{CC} = 10V).
Source and sink output current capability is typically 50mA (at V_{CC} = 10V), fixed by an internal limitation circuit.

MICROPOWER DUAL CMOS VOLTAGE COMPARATORS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- PUSH-PULL CMOS OUTPUT (NO EXTERNAL PULL-UP RESISTOR REQUIRED)
- EXTREMELY LOW SUPPLY CURRENT : 9µA TYP / COMPARATOR
- WIDE SINGLE SUPPLY RANGE (3V TO 16V) OR DUAL SUPPLIES (± 1.5V TO ± 8V)
- EXTREMELY LOW INPUT BIAS CURRENT : 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1pA TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 2µs TYP FOR 5mV OVERDRIVE
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM393



N
DIP8
(Plastic Package)

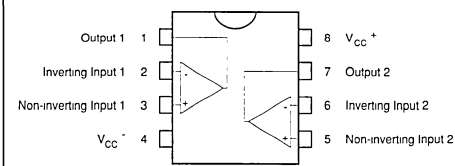
D
SO8
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3702C	0°C, +70°C	●	●
TS3702I	-40°C, +105°C	○	○
TS3702M	-55°C, +125°C	●	○
Example : TS3702CN			

3702-01.TBL

PIN CONNECTIONS (top view)



3702-01.EPS

DESCRIPTION

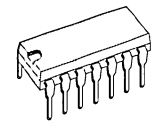
The TS3702 is a micropower CMOS dual voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM393). The push-pull CMOS output stage allows power and space saving by eliminating the external pull-up resistor required by usual open-collector output comparators.

Thus response times remain similar to the LM393.

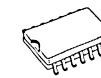
MICROPOWER QUAD CMOS VOLTAGE COMPARATORS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- PUSH-PULL CMOS OUTPUT (NO EXTERNAL PULL-UP RESISTOR REQUIRED)
- EXTREMELY LOW SUPPLY CURRENT : 9µA TYP / COMPARATOR
- WIDE SINGLE SUPPLY RANGE (3V TO 16V) OR DUAL SUPPLIES (± 1.5V TO ± 8V)
- EXTREMELY LOW INPUT BIAS CURRENT : 1pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1pA TYP
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE : $10^{12}\Omega$ TYP
- FAST RESPONSE TIME : 2µs TYP FOR 5mV OVERDRIVE
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM339



N
DIP14
(Plastic Package)



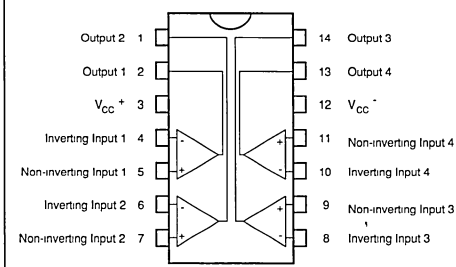
D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3704C	0°C, +70°C	•	•
TS3704I	-40°C, +105°C	•	•
TS3704M	-55°C, +125°C	•	•
Example : TS3704CN			

374-01.TBL

PIN CONNECTIONS (top view)



3704-01 EPS

DESCRIPTION

The TS3704 is a micropower CMOS quad voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM339). The push-pull CMOS output stage allows power and space saving by eliminating the external pull-up resistor required by usual open-collector output comparators.

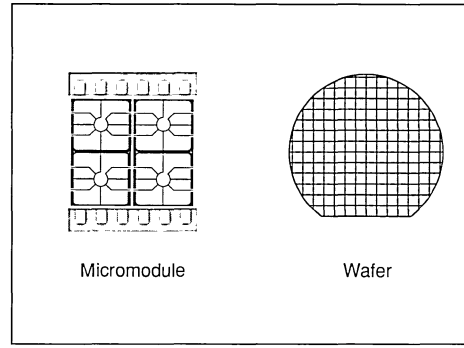
Thus response times remain similar to the LM339.

MEMORIES

HIGH ENDURANCE CMOS 192 bit EEPROM WITH SECURE LOGIC ACCESS CONTROL

ADVANCE DATA

- SINGLE 5V SUPPLY VOLTAGE
- PROGRAMMING TIME: 5 ms
- MEMORY DIVIDED INTO:
  - 24 bits of Chip Data
  - 40 bits of Application Data
  - 48 bits of Count Data
  - 12 extra-bits of Transport Code
  - 64 bits of Issuer Data
- COUNTING CAPABILITY up to 262,144 UNITS
- CIRCUIT PROTECTED by TRANSPORT CODE for DELIVERY from SGS-THOMSON to the CUSTOMER
- 5 EXTERNAL CONTACTS ONLY (ISO 7816 COMPATIBLE)
- ANSWER to RESET FULLY COMPATIBLE with ISO 7816-3
- E.S.D. GREATER THAN 4000V
- POWER-ON and LOW V_{CC} RESET



DESCRIPTION

The ST1305 is a 192 bits EEPROM memory with associated security logic to control memory access. The circuit includes counting capabilities and thus is very well adapted to prepaid card applications.

The ST1305 is protected by hardwired security logic and special fuses. The memory is a matrix of 24 x 8 cells accessed bit by bit for reading and programming, and by byte for internal erasing in final application.

Figure 1. Logic Diagram

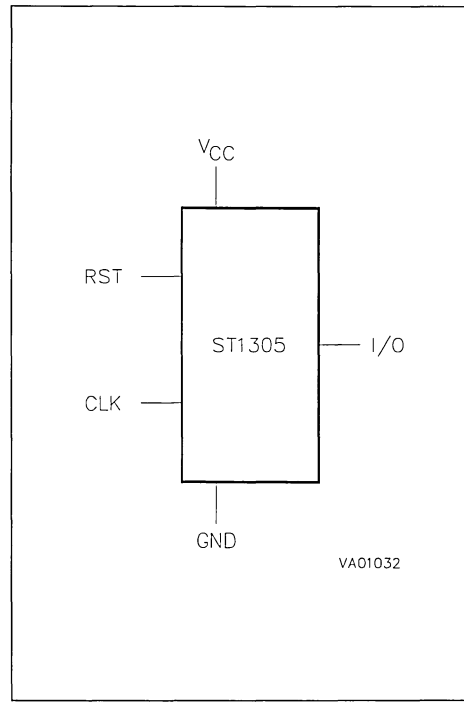


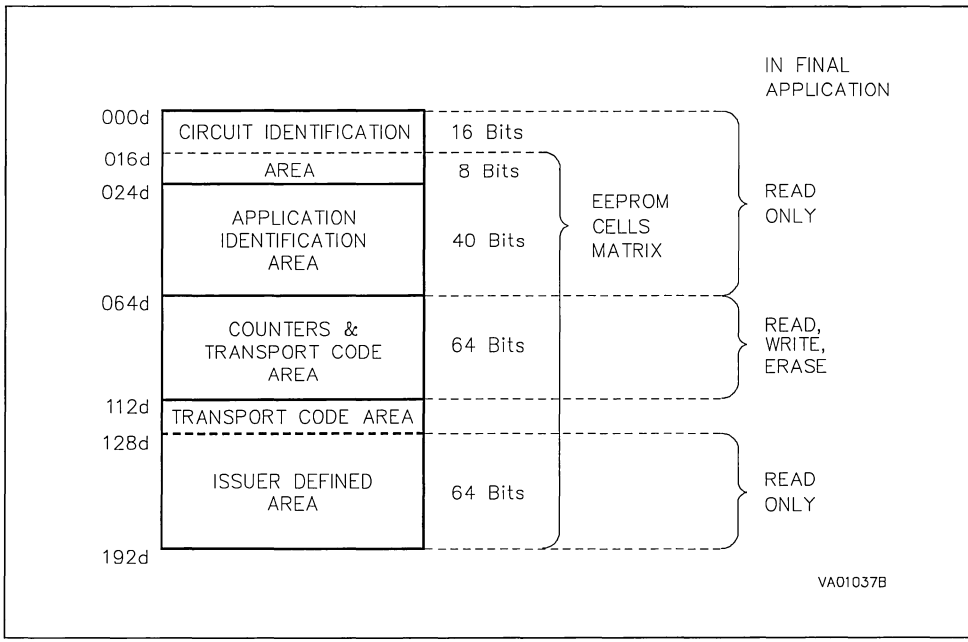
Table 1. Signal Names

CLK	Clock
RST	Reset
I/O	Data Input / Output
V_{CC}	Supply Voltage
GND	Ground

INTERNAL ADDRESS MAPPING

The internal address space of the ST1305 is divided into five zones as shown in Figure 2. These zones are the actual EEPROM memory array. The Transport Code or Counter area is used in two configurations: In the ISSUER configuration it is used to store the Transport Code loaded by SGS-THOMSON for security during delivery to the card issuer; in the USER configuration it is used as a serie of counters.

Figure 2. Memory Map



SERIAL ACCESS CMOS 1K (128 x 8) EEPROMs

ABBREVIATED DATA

- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24C01 version
  - 3V to 5.5V for ST24x01C versions
  - 2.5V to 5.5V for ST25C01, ST25x01C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W01C and ST25W01C
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES FOR "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGN: ST24/25C01C and ST24/25W01C

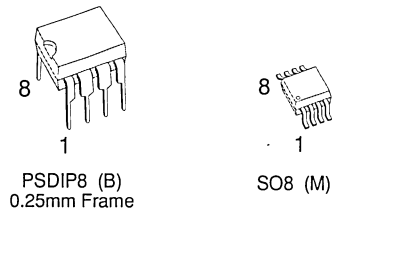
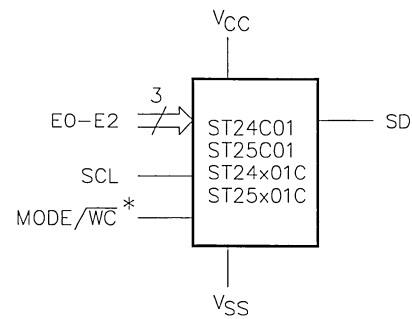


Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W01C products.

DESCRIPTION

This specification covers a range of 1K bits I^2C bus EEPROM products, the ST24/25C01, the ST24/25C01C and the ST24/25W01C. In the text, products are referred to as ST24/25x01C, where

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

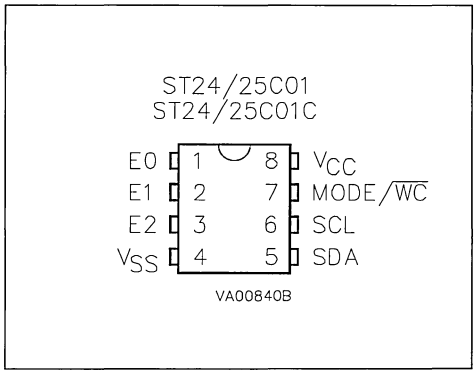


Figure 2B. SO Pin Connections

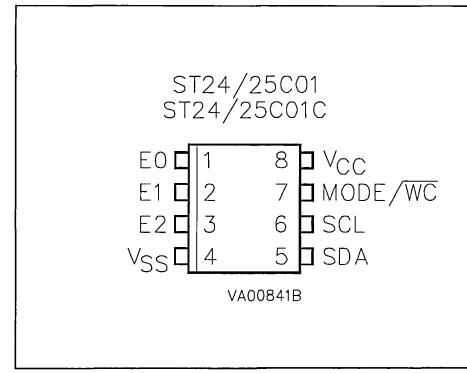


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage	ST24/25C01 ST24/25x01C		–0.3 to V_{CC} +0.6 –0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST24/25C01 ST24/25x01C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST24/25C01 ST24/25x01C	500 500	V

Notes: 1 Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω)

DESCRIPTION (cont'd)

"x" is: "C" for Standard version and "W" for hardware Write Control version.

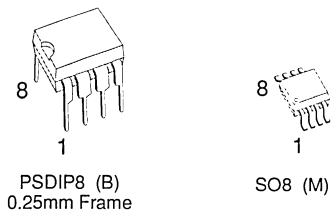
The ST24/25x01C are 1K bit electrically erasable programmable memories (EEPROM), organized as 128 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

SERIAL ACCESS CMOS 2K (256 x 8) EEPROMs

ABBREVIATED DATA

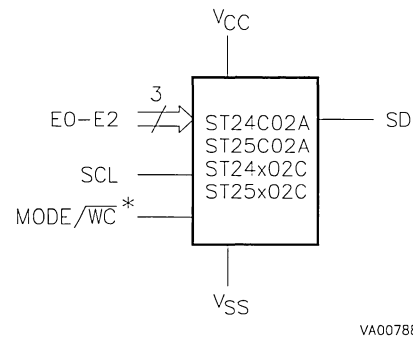
- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24C02A version
  - 3V to 5.5V for ST24x02C versions
  - 2.5V to 5.5V for ST25C02A, ST25x02C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W02C and ST25W02C
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES for "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGNS: ST24/25C02C and ST24/25W02C



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W02C products

DESCRIPTION

This specification covers a range of 2K bits I^2C bus EEPROM products, the ST24/25C02A, the ST24/25C02C and the ST24/25W02C. In the text, products are referred to as ST24/25x02C, where

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

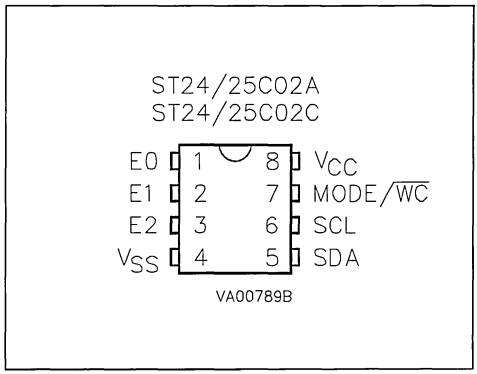


Figure 2B. SO Pin Connections

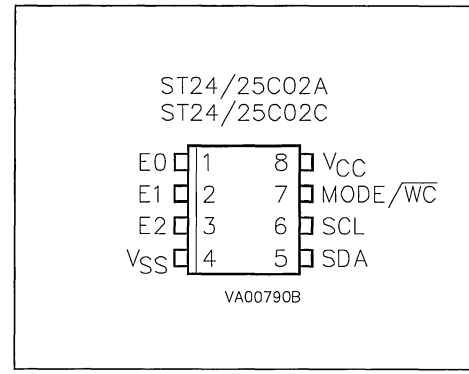


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage	ST24/25C02A ST24/25x02C		–0.3 to V_{CC} +0.6 –0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST24/25C02A ST24/25x02C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST24/25C02A ST24/25x02C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

"x" is: "C" for Standard version and "W" for hardware Write Control version.

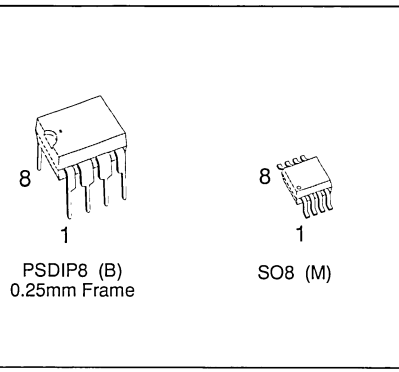
The ST24/25x02C are 2K bit electrically erasable programmable memories (EEPROM), organized as 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

SERIAL ACCESS CMOS 4K (512 x 8) EEPROMs

ABBREVIATED DATA

- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24C04 version
  - 3V to 5.5V for ST24x04C versions
  - 2.5V to 5.5V for ST25C04, ST25x04C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W04C and ST25W04C
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES for "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGNS: ST24/25C04C and ST24/25W04C



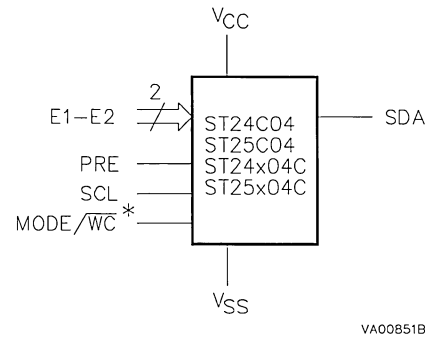
DESCRIPTION

This specification covers a range of 4K bits I^2C bus EEPROM products, the ST24/25C04, the ST24/25C04C and the ST24/25W04C. In the text, products are referred to as ST24/25x04C, where

Table 1. Signal Names

PRE	Write Protect Enable
E1 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W04C products.

This is an abbreviated version of the complete document. The full document is available separately

Figure 2A. DIP Pin Connections

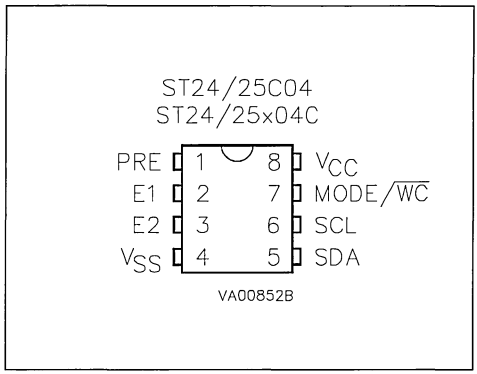


Figure 2B. SO Pin Connections

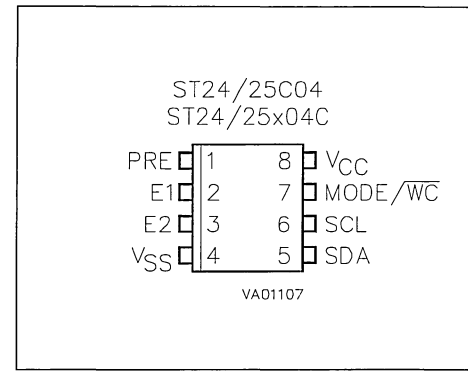


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage	ST24/25C04 ST24/25x04C		–0.3 to V_{CC} +0.6 –0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST24/25C04 ST24/25x04C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST24/25C04 ST24/25x04C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

"x" is: "C" for Standard version and "W" for hardware Write Control version.

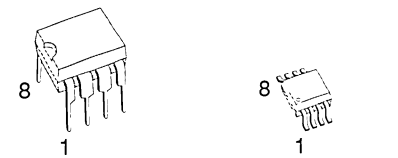
The ST24/25x04C are 4K bit electrically erasable programmable memories (EEPROM), organized as 2 blocks of 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

ST24C08, ST25C08
ST24x08C, ST25x08C

SERIAL ACCESS CMOS 8K (1024 x 8) EEPROMs

ABBREVIATED DATA

- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24C08 version
  - 3V to 5.5V for ST24x08C versions
  - 2.5V to 5.5V for ST25C08, ST25x08C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W08C and ST25W08C
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES)
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES for "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGN: ST24/25C08C and ST24/25W08C



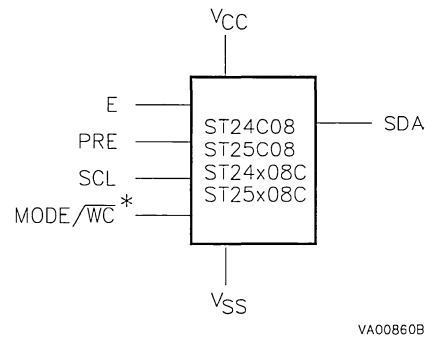
DESCRIPTION

This specification covers a range of 8K bits I^2C bus EEPROM products, the ST24/25C08, the ST24/25C08C and the ST24/25W08C. In the text,

Table 1. Signal Names

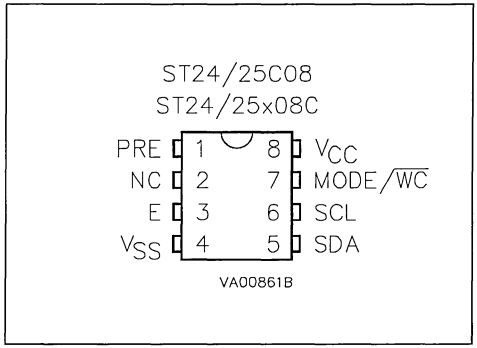
PRE	Write Protect Enable
E	Chip Enable Input
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



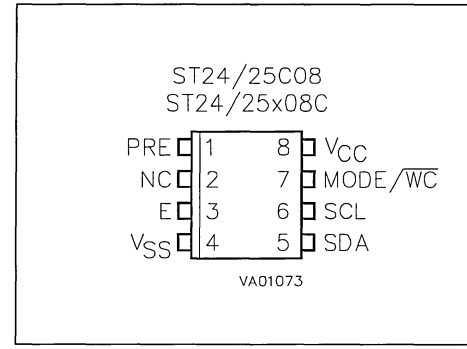
Note: $\overline{WC}$ signal is only available for ST24/25W08C products.

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage	ST24/25C08 ST24/25x08C		–0.3 to V_{CC} +0.6 –0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST24/25C08 ST24/25x08C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST24/25C08 ST24/25x08C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω)
3 EIAJ IC-121 (Condition C) (200pF, 0 Ω)

DESCRIPTION (cont'd)

products are referred to as ST24/25x08C, where "x" is: "C" for Standard version and "W" for Hardware Write Control version.

The ST24/25x08C are 8K bit electrically erasable programmable memories (EEPROM), organized as 4 blocks of 256 x 8 bits.

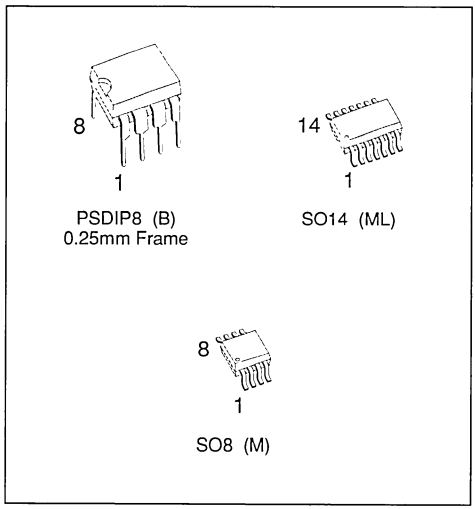
They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years.

The memories operate with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

SERIAL ACCESS CMOS 16K (2048 x 8) EEPROMs

ABBREVIATED DATA

- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x16 versions
  - 2.5V to 5.5V for ST25x16 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W16 and ST25W16
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES)
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

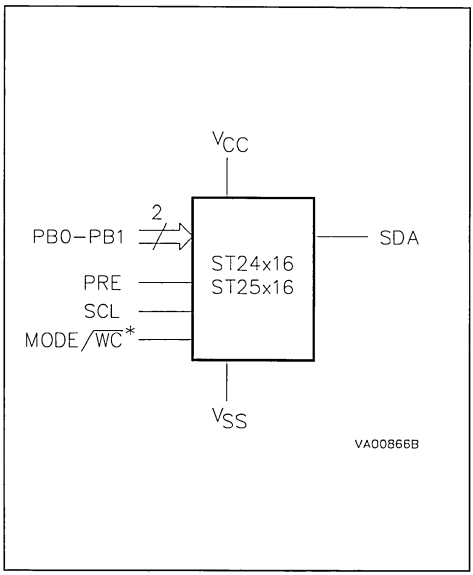


DESCRIPTION

This specification covers a range of 16K bits I^2C bus EEPROM products, the ST24/25C16 and the ST24/25W16. In the text, products are referred to as ST24/25x16 where "x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x16 are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x 8 bits. These are manufactured

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W16 products

Table 1. Signal Names

PRE	Write Protect Enable
PB0, PB1	Protect Block Select
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multybyte/Page Write Mode (C version)
$\overline{W}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

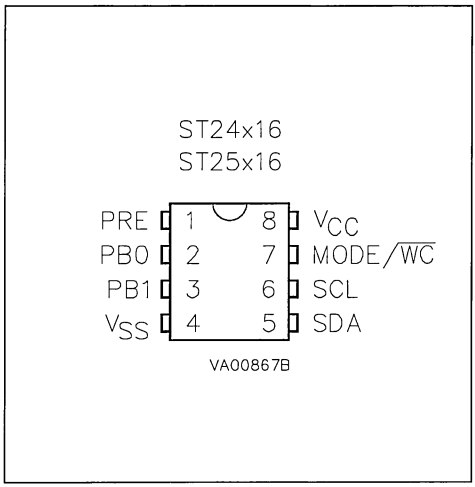
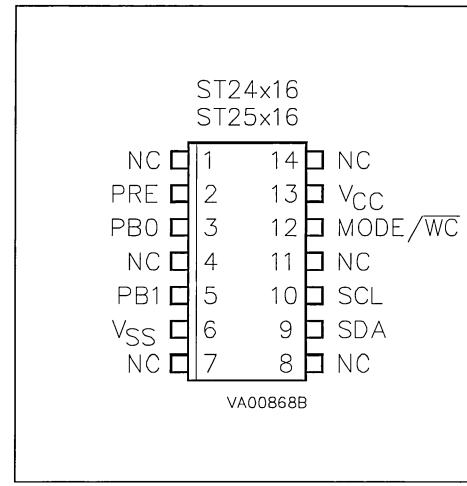
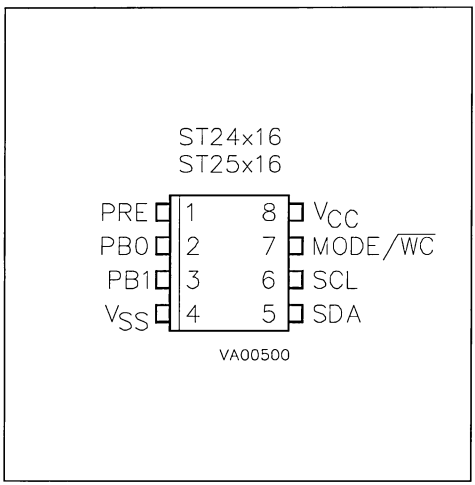


Figure 2B. SO14 Pin Connections



Warning: NC = No Connection

Figure 2C. SO8 Pin Connections



DESCRIPTION (cont'd)

in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years.

The ST25x16 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The memories behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the 4 upper blocks of the memory may be write protected. The protected area is programmable to start on any 16 byte boundary. The block in which the protection starts is selected by the input pins PB0, PB1. Protection is enabled by setting a Protect Flag bit when the PRE input pin is driven High.

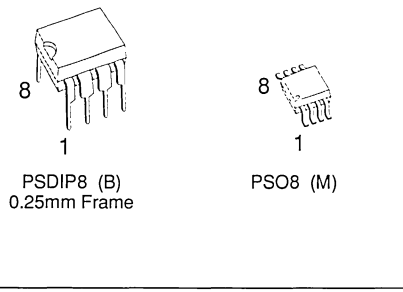
SGS-THOMSON MICROELECTRONICS

ST24E16D
ST25E16D

SERIAL ACCESS CMOS 16K (2048 x 8) EEPROMs EXTENDED ADDRESSING COMPATIBLE WITH I²C BUS

ABBREVIATED DATA

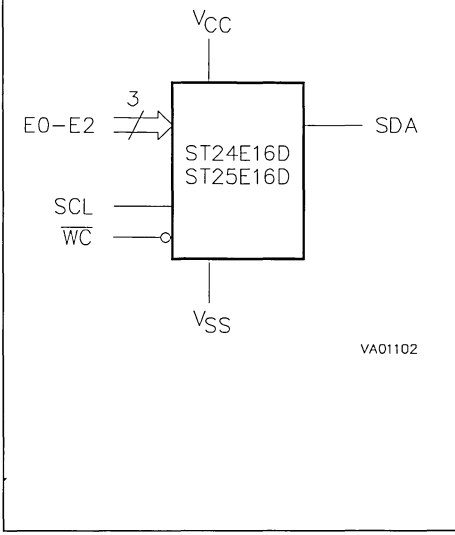
- COMPATIBLE with I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24E16D version
  - 2V to 5.5V for ST25E16D version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

PSO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST24/25E16D are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The ST25E16D operates with a power supply value as

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

This is an abbreviated version of the complete document The full document is available separately

Figure 2A. DIP Pin Connections

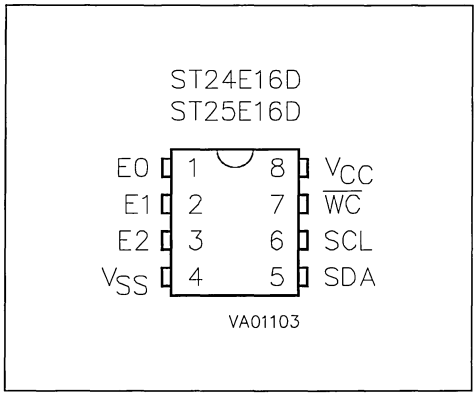


Figure 2B. SO Pin Connections

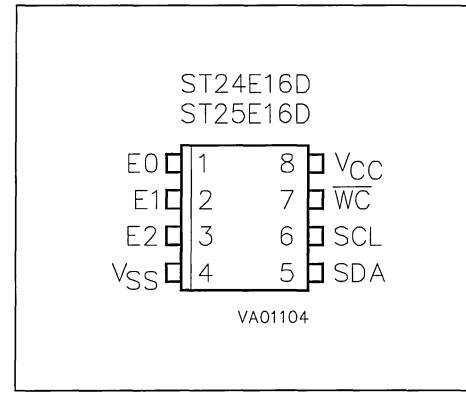


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2 100pF through 1500Ω; MIL-STD-883C, 3015.7
3 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

low as 2.0V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E16D carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E16D behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master.

The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way.

PROTECTION CIRCUITS

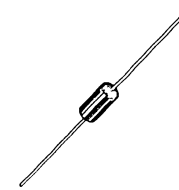
SGS-THOMSON MICROELECTRONICS

1.5KE6V8P,A/440P,A
1.5KE6V8CP,CA/440CP,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 1500 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 440 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to V_{BR}).
- UL RECOGNIZED.



CB429
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code, and Cathode Band (for unidirectional types only).
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

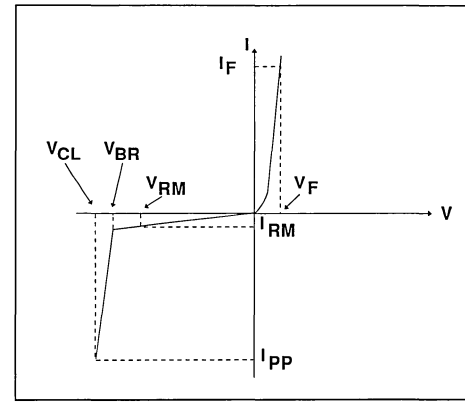
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	1500	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	5	W
I_{FSM}	Non repetitive surge peak forward current For Unidirectional types.	Tamb = 25°C t =10 ms	250	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 175	°C °C
T_L	Maximum lead temperature for soldering during 10 s		230	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	20	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. L_{lead} = 10 mm	75	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 100 A.



TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
P 1.5KE6V8P	P 1.5KE6V8CP	1000	5.8	6.45	6.8	7.48	10	10.5	143	13.4	746	5.7	9500
P 1.5KE6V8A	P 1.5KE6V8CA	1000	5.8	6.45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
P 1.5KE7V5P	1.5KE7V5CP	500	6.4	7.13	7.5	8.25	10	11.3	132	14.5	690	6.1	8500
1.5KE7V5A	P 1.5KE7V5CA	500	6.4	7.13	7.5	7.88	10	11.3	132	14.5	690	6.1	8500
1.5KE8V2P	1.5KE8V2CP	200	7.02	7.79	8.2	9.02	10	12.1	124	15.5	645	6.5	8000
P 1.5KE8V2A	P 1.5KE8V2CA	200	7.02	7.79	8.2	8.61	10	12.1	124	15.5	645	6.5	8000
1.5KE9V1P	1.5KE9V1CP	50	7.78	8.65	9.1	10	1	13.4	112	17.1	585	6.8	7500
1.5KE9V1A	1.5KE9V1CA	50	7.78	8.65	9.1	9.55	1	13.4	112	17.1	585	6.8	7500
1.5KE10P	1.5KE10CP	10	8.55	9.5	10	11	1	14.5	103	18.6	538	7.3	7000
P 1.5KE10A	P 1.5KE10CA	10	8.55	9.5	10	10.5	1	14.5	103	18.6	538	7.3	7000
1.5KE11P	1.5KE11CP	5	9.4	10.5	11	12.1	1	15.6	96	20.3	493	7.5	6400
1.5KE11A	1.5KE11CA	5	9.4	10.5	11	11.6	1	15.6	96	20.3	493	7.5	6400
1.5KE12P	P 1.5KE12CP	5	10.2	11.4	12	13.2	1	16.7	90	21.7	461	7.8	6000
P 1.5KE12A	P 1.5KE12CA	5	10.2	11.4	12	12.6	1	16.7	90	21.7	461	7.8	6000
1.5KE13P	1.5KE13CP	5	11.1	12.4	13	14.3	1	18.2	82	23.6	423	8.1	5500
P 1.5KE13A	P 1.5KE13CA	5	11.1	12.4	13	13.7	1	18.2	82	23.6	423	8.1	5500
P 1.5KE15P	P 1.5KE15CP	5	12.8	14.3	15	16.5	1	21.2	71	27.2	368	8.4	5000
P 1.5KE15A	P 1.5KE15CA	5	12.8	14.3	15	15.8	1	21.2	71	27.2	368	8.4	5000
1.5KE16P	1.5KE16CP	5	13.6	15.2	16	17.6	1	22.5	67	28.9	346	8.6	4700
1.5KE16A	1.5KE16CA	5	13.6	15.2	16	16.8	1	22.5	67	28.9	346	8.6	4700
P 1.5KE18P	P 1.5KE18CP	5	15.3	17.1	18	19.8	1	25.2	59.5	32.5	308	8.8	4300
P 1.5KE18A	P 1.5KE18CA	5	15.3	17.1	18	18.9	1	25.2	59.5	32.5	308	8.8	4300
P 1.5KE20P	P 1.5KE20CP	5	17.1	19	20	22	1	27.7	54	36.1	277	9.0	4000
P 1.5KE20A	1.5KE20CA	5	17.1	19	20	21	1	27.7	54	36.1	277	9.0	4000
1.5KE22P	1.5KE22CP	5	18.8	20.9	22	24.2	1	30.6	49	39.3	254	9.2	3700

P = Prefered device

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
1.5KE22A	1.5KE22CA	5	18.8	20.9	22	23.1	1	30.6	49	39.3	254	9.2	3700
1.5KE24P	1.5KE24CP	5	20.5	22.8	24	26.4	1	33.2	45	42.8	234	9.4	3500
P 1.5KE24A	1.5KE24CA	5	20.5	22.8	24	25.2	1	33.2	45	42.8	234	9.4	3500
P 1.5KE27P	1.5KE27CP	5	23.1	25.7	27	29.7	1	37.5	40	48.3	207	9.6	3200
1.5KE27A	1.5KE27CA	5	23.1	25.7	27	28.4	1	37.5	40	48.3	207	9.6	3200
1.5KE30P	P 1.5KE30CP	5	25.6	28.5	30	33	1	41.5	36	53.5	187	9.7	2900
P 1.5KE30A	P 1.5KE30CA	5	25.6	28.5	30	31.5	1	41.5	36	53.5	187	9.7	2900
P 1.5KE33P	P 1.5KE33CP	5	28.2	31.4	33	36.3	1	45.7	33	59.0	169	9.8	2700
P 1.5KE33A	1.5KE33CA	5	28.2	31.4	33	34.7	1	45.7	33	59.0	169	9.8	2700
P 1.5KE36P	P 1.5KE36CP	5	30.8	34.2	36	39.6	1	49.9	30	64.3	156	9.9	2500
P 1.5KE36A	P 1.5KE36CA	5	30.8	34.2	36	37.8	1	49.9	30	64.3	156	9.9	2500
P 1.5KE39P	P 1.5KE39CP	5	33.3	37.1	39	42.9	1	53.9	28	69.7	143	10.0	2400
P 1.5KE39A	P 1.5KE39CA	5	33.3	37.1	39	41.0	1	53.9	28	69.7	143	10.0	2400
1.5KE43P	1.5KE43CP	5	36.8	40.9	43	47.3	1	59.3	25.3	76.8	130	10.1	2200
P 1.5KE43A	P 1.5KE43CA	5	36.8	40.9	43	45.2	1	59.3	25.3	76.8	130	10.1	2200
1.5KE47P	1.5KE47CP	5	40.2	44.7	47	51.7	1	64.8	23.2	84	119	10.1	2050
P 1.5KE47A	P 1.5KE47CA	5	40.2	44.7	47	49.4	1	64.8	23.2	84	119	10.1	2050
1.5KE51P	1.5KE51CP	5	43.6	48.5	51	56.1	1	70.1	21.4	91	110	10.2	1950
P 1.5KE51A	1.5KE51CA	5	43.6	48.5	51	53.6	1	70.1	21.4	91	110	10.2	1950
1.5KE56P	1.5KE56CP	5	47.8	53.2	56	61.6	1	77	19.5	100	100	10.3	1800
P 1.5KE56A	1.5KE56CA	5	47.8	53.2	56	58.8	1	77	19.5	100	100	10.3	1800
1.5KE62P	1.5KE62CP	5	53.0	58.9	62	68.2	1	85	17.7	111	90	10.4	1700
P 1.5KE62A	P 1.5KE62CA	5	53.0	58.9	62	65.1	1	85	17.7	111	90	10.4	1700
P 1.5KE68P	P 1.5KE68CP	5	58.1	64.6	68	74.8	1	92	16.3	121	83	10.4	1550
P 1.5KE68A	P 1.5KE68CA	5	58.1	64.6	68	71.4	1	92	16.3	121	83	10.4	1550
1.5KE75P	1.5KE75CP	5	64.1	71.3	75	82.5	1	103	14.6	134	75	10.5	1450
P 1.5KE75A	P 1.5KE75CA	5	64.1	71.3	75	78.8	1	103	14.6	134	75	10.5	1450
P 1.5KE82P	P 1.5KE82CP	5	70.1	77.9	82	90.2	1	113	13.3	146	69	10.5	1350
P 1.5KE82A	P 1.5KE82CA	5	70.1	77.9	82	86.1	1	113	13.3	146	69	10.5	1350
1.5KE91P	1.5KE91CP	5	77.8	86.5	91	100	1	125	12	162	62	10.6	1250
P 1.5KE91A	P 1.5KE91CA	5	77.8	86.5	91	95.5	1	125	12	162	62	10.6	1250
1.5KE100P	1.5KE100CP	5	85.5	95.0	100	110	1	137	11	178	56	10.6	1150
P 1.5KE100A	1.5KE100CA	5	85.5	95.0	100	105	1	137	11	178	56	10.6	1150
1.5KE110P	P 1.5KE110CP	5	94.0	105	110	121	1	152	9.9	195	51	10.7	1050
1.5KE110A	1.5KE110CA	5	94.0	105	110	116	1	152	9.9	195	51	10.7	1050
1.5KE120P	1.5KE120CP	5	102	114	120	132	1	165	9.1	212	47	10.7	1000
P 1.5KE120A	P 1.5KE120CA	5	102	114	120	126	1	165	9.1	212	47	10.7	1000
1.5KE130P	P 1.5KE130CP	5	111	124	130	143	1	179	8.4	230	43	10.7	950
P 1.5KE130A	P 1.5KE130CA	5	111	124	130	137	1	179	8.4	230	43	10.7	950
1.5KE150P	1.5KE150CP	5	128	143	150	165	1	207	7.2	265	38	10.8	850
P 1.5KE150A	P 1.5KE150CA	5	128	143	150	158	1	207	7.2	265	38	10.8	850
P 1.5KE160P	P 1.5KE160CP	5	136	152	160	176	1	219	6.8	282	35	10.8	800
P 1.5KE160A	P 1.5KE160CA	5	136	152	160	168	1	219	6.8	282	35	10.8	800
1.5KE170P	1.5KE170CP	5	145	161	170	187	1	234	6.4	301	33	10.8	750
P 1.5KE170A	1.5KE170CA	5	145	161	170	179	1	234	6.4	301	33	10.8	750
1.5KE180P	P 1.5KE180CP	5	154	171	180	198	1	246	6.1	317	31.5	10.8	725
P 1.5KE180A	P 1.5KE180CA	5	154	171	180	189	1	246	6.1	317	31.5	10.8	725
P 1.5KE200P	P 1.5KE200CP	5	171	190	200	220	1	274	5.5	353	28	10.8	675
P 1.5KE200A	P 1.5KE200CA	5	171	190	200	210	1	274	5.5	353	28	10.8	675
1.5KE220P	P 1.5KE220CP	5	188	209	220	242	1	328	4.6	388	26	10.8	625
P 1.5KE220A	P 1.5KE220CA	5	188	209	220	231	1	328	4.6	388	26	10.8	625
P 1.5KE250P	P 1.5KE250CP	5	213	237	250	275	1	344	5.0	442	23	11	560
P 1.5KE250A	P 1.5KE250CA	5	213	237	250	263	1	344	5.0	442	23	11	560
1.5KE280P	1.5KE280CP	5	239	266	280	308	1	384	5.0	494	20	11	520
1.5KE280A	1.5KE280CA	5	239	266	280	294	1	384	5.0	494	20	11	520

P = Prefered device

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
1.5KE300P	P 1.5KE300CP	5	256	285	300	330	1	414	5.0	529	19	11	500
P 1.5KE300A	1.5KE300CA	5	256	285	300	315	1	414	5.0	529	19	11	500
1.5KE320P	1.5KE320CP	5	273	304	320	352	1	438	4.5	564	18	11	460
P 1.5KE320A	1.5KE320CA	5	273	304	320	336	1	438	4.5	564	18	11	460
P 1.5KE350P	P 1.5KE350CP	5	299	332	350	385	1	482	4.0	618	16	11	430
1.5KE350A	1.5KE350CA	5	299	332	350	368	1	482	4.0	618	16	11	430
P 1.5KE400P	P 1.5KE400CP	5	342	380	400	440	1	548	4.0	706	14	11	390
1.5KE400A	1.5KE400CA	5	342	380	400	420	1	548	4.0	706	14	11	390
P 1.5KE440P	P 1.5KE440CP	5	376	418	440	484	1	603	3.5	776	13	11	360
1.5KE440A	1.5KE440CA	5	376	418	440	462	1	603	3.5	776	13	11	360

All parameters tested at 25 °C, except where indicated.

P = Prefered device

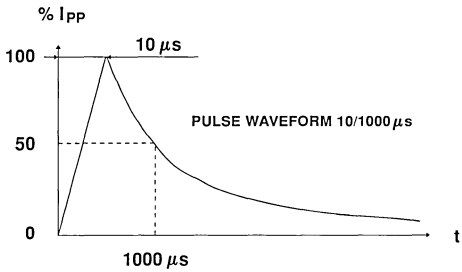
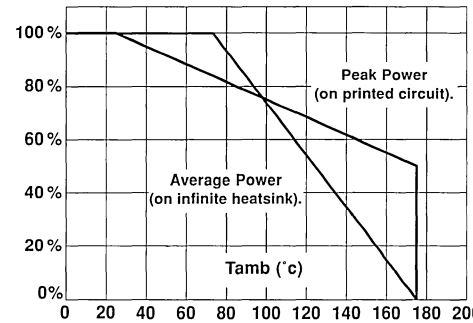


Figure 1: Power dissipation derating versus ambient temperature



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Note 2 : Pulse test $T_P < 50$ ms

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$

Note 4 : VR = 0 V, F = 1 MHz For bidirectional types, capacitance value is divided by 2

Figure 2 : Peak pulse power versus exponential pulse duration.

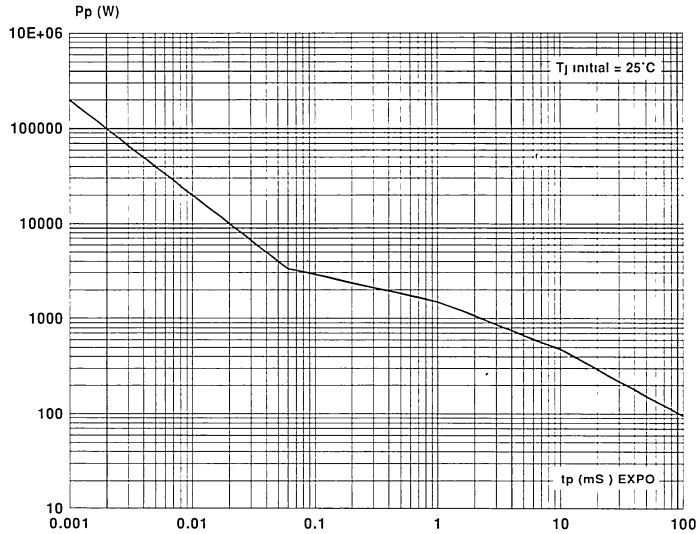
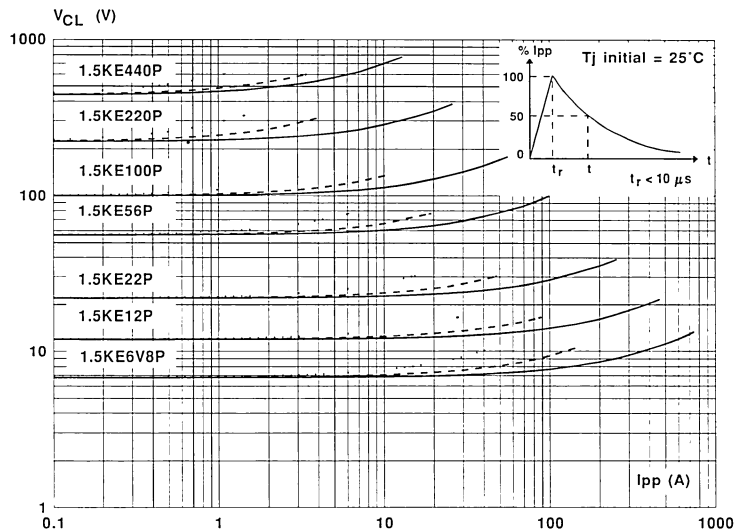


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} \cdot [T_a - 25] \cdot V_{(BR)}$
For intermediate voltages, extrapolate the given results

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

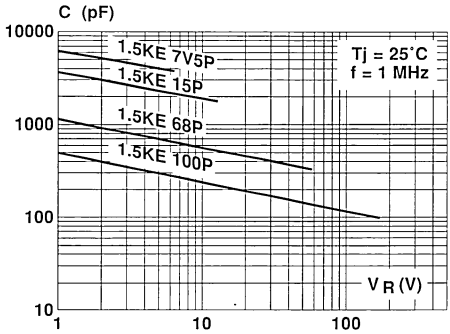


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

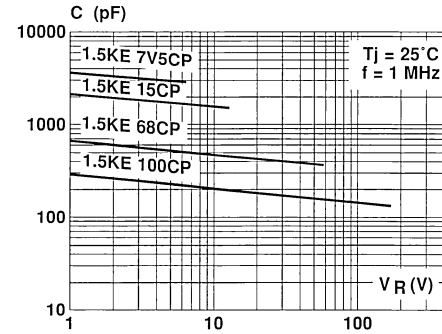


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

Note : For units with V_{BR} > 200 V
V_F is twice than shown

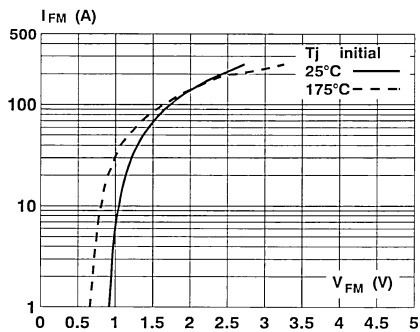
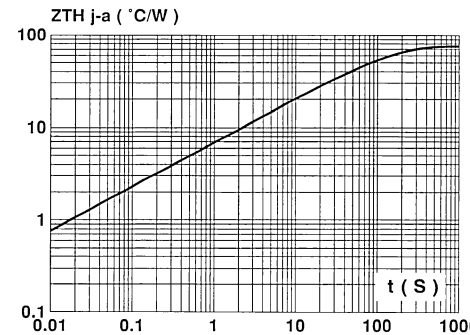
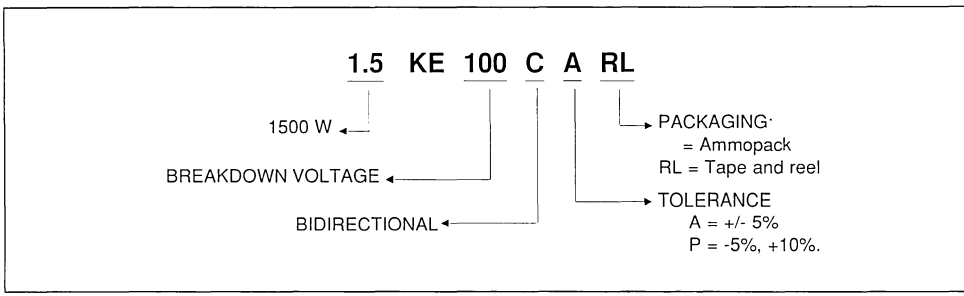


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with L_{lead} = 10mm.



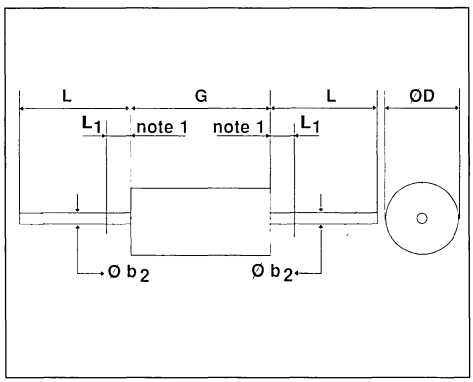
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

CB429



Ref.	Millimeters		Inches	
	min	max	min	max
∅ b_2	-	1.06	-	0.042
∅ D	-	5 1	-	0 20
G	-	9 8	-	0.386
L	26	-	1 024	-
L_1	-	1.27	-	0.050
note1:The diameter ∅ b_2 is not controlled over zone L_1				

Weight = 0 85 g.

Packaging : standard packaging is in tape and reel

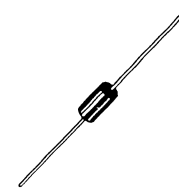
SGS-THOMSON MICROELECTRONICS

BZW04-5V8,B/376,B
BZW04P5V8,B/376,B

TRANSIL

FEATURES

- PEAK PULSE POWER= 400 W @ 1ms.
- STAND-OFF VOLTAGE RANGE : From 5V8 to 376 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).
- UL RECOGNIZED



F126
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

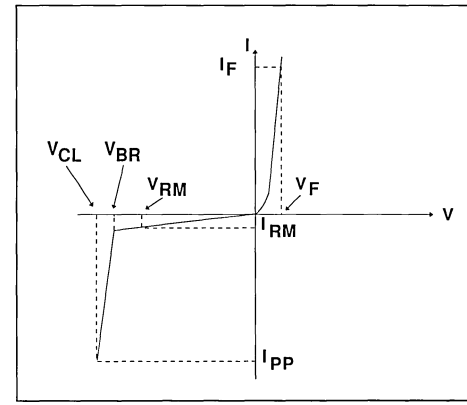
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	400	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	1.7	W
I_{FSM}	Non repetitive surge peak forward current For Unidirectional types	Tamb = 25°C t =10 ms	50	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 175	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	60	°C/W
R_{th} (j-a)	Junction to ambiant. on printed circuit. L_{lead} = 10 mm	100	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 25 A.



TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	Bidirectional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
P BZW04P5V8	P BZW04P5V8B	1000	5.8	6.45	6 8	7.48	10	10.5	38	13.4	174	5.7	3500
BZW04-5V8	BZW04-5V8B	1000	5.8	6.45	6.8	7.14	10	10.5	38	13.4	174	5.7	3500
BZW04P6V4	P BZW04P6V4B	500	6.4	7.13	7.5	8.25	10	11.3	35.4	14.5	160	6.1	3100
BZW04-6V4	BZW04-6V4B	500	6.4	7.13	7.5	7.88	10	11.3	35.4	14.5	160	6.1	3100
BZW04P7V0	BZW04P7V0B	200	7.02	7.79	8.2	9.02	10	12.1	33	15.5	148	6.5	2700
BZW04-7V0	BZW04-7V0B	200	7.02	7.79	8.2	8.61	10	12.1	33	15.5	148	6.5	2700
BZW04P7V8	BZW04P7V8B	50	7.78	8.65	9.1	10	1	13.4	30	17.1	134	6.8	2300
BZW04-7V8	BZW04-7V8B	50	7.78	8.65	9.1	9.55	1	13.4	30	17.1	134	6.8	2300
BZW04P8V5	BZW04P8V5B	10	8.55	9.5	10	11	1	14.5	27.6	18.6	124	7.3	2000
BZW04-8V5	BZW04-8V5B	10	8.55	9.5	10	10.5	1	14.5	27.6	18.6	124	7.3	2000
P BZW04P9V4	BZW04P9V4B	5	9.4	10.5	11	12.1	1	15.6	25.7	20.3	113	7.5	1750
BZW04-9V4	BZW04-9V4B	5	9.4	10.5	11	11.6	1	15.6	25.7	20.3	113	7.5	1750
P BZW04P10	P BZW04P10B	5	10.2	11.4	12	13.2	1	16.7	24	21.7	106	7.8	1550
BZW04-10	BZW04-10B	5	10.2	11.4	12	12.6	1	16.7	24	21.7	106	7.8	1550
P BZW04P11	P BZW04P11B	5	11.1	12.4	13	14.3	1	18.2	22	23.6	97	8.1	1450
BZW04-11	BZW04-11B	5	11.1	12.4	13	13.7	1	18.2	22	23.6	97	8.1	1450
P BZW04P13	P BZW04P13B	5	12.8	14.3	15	16.5	1	21.2	19	27.2	85	8.4	1200
P BZW04-13	P BZW04-13B	5	12.8	14.3	15	15.8	1	21.2	19	27.2	85	8.4	1200
P BZW04P14	BZW04P14B	5	13.6	15.2	16	17.6	1	22.5	17.8	28.9	80	8.6	1100
BZW04-14	BZW04-14B	5	13.6	15.2	16	16.8	1	22.5	17.8	28.9	80	8.6	1100
P BZW04P15	P BZW04P15B	5	15.3	17.1	18	19.8	1	25.2	16	32.5	71	8.8	975
P BZW04-15	P BZW04-15B	5	15.3	17.1	18	18.9	1	25.2	16	32.5	71	8.8	975
BZW04P17	BZW04P17B	5	17.1	19	20	22	1	27.7	14.5	36.1	64	9.0	850
BZW04-17	BZW04-17B	5	17.1	19	20	21	1	27.7	14.5	36.1	64	9.0	850
BZW04P19	P BZW04P19B	5	18.8	20.9	22	24.2	1	30.6	13	39.3	59	9.2	800

P = Prevered device

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	Bidirectional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
BZW04-19	BZW04-19B	5	18.8	20.9	22	23.1	1	30.6	13	39.3	59	9.2	800
BZW04P20	P BZW04P20B	5	20.5	22.8	24	26.4	1	33.2	12	42.8	54	9.4	725
BZW04-20	BZW04-20B	5	20.5	22.8	24	25.2	1	33.2	12	42.8	54	9.4	725
BZW04P23	P BZW04P23B	5	23.1	25.7	27	29.7	1	37.5	10.7	48.3	48	9.6	625
BZW04-23	BZW04-23B	5	23.1	25.7	27	28.4	1	37.5	10.7	48.3	48	9.6	625
P BZW04P26	BZW04P26B	5	25.6	28.5	30	33	1	41.5	9.6	53.5	43	9.7	575
BZW04-26	BZW04-26B	5	25.6	28.5	30	31.5	1	41.5	9.6	53.5	43	9.7	575
P BZW04P28	P BZW04P28B	5	28.2	31.4	33	36.3	1	45 7	8.8	59.0	39	9.8	510
BZW04-28	BZW04-28B	5	28.2	31.4	33	34 7	1	45.7	8.8	59.0	39	9.8	510
BZW04P31	BZW04P31B	5	30.8	34.2	36	39.6	1	49.9	8	64.3	36	9.9	480
P BZW04-31	BZW04-31B	5	30.8	34.2	36	37.8	1	49.9	8	64.3	36	9.9	480
P BZW04P33	P BZW04P33B	5	33.3	37.1	39	42.9	1	53.9	7.4	69 7	33	10.0	450
P BZW04-33	BZW04-33B	5	33.3	37.1	39	41.0	1	53.9	7.4	69.7	33	10.0	450
BZW04P37	BZW04P37B	5	36.8	40.9	43	47.3	1	59.3	6.7	76.8	30	10.1	400
BZW04-37	P BZW04-37B	5	36.8	40.9	43	45.2	1	59.3	6.7	76 8	30	10.1	400
BZW04P40	BZW04P40B	5	40.2	44.7	47	51.7	1	64.8	6.2	84	27	10.1	370
BZW04-40	BZW04-40B	5	40.2	44.7	47	49.4	1	64.8	6.2	84	27	10.1	370
BZW04P44	BZW04P44B	5	43.6	48.5	51	56.1	1	70.1	5.7	91	25	10.2	350
BZW04-44	BZW04-44B	5	43.6	48.5	51	53 6	1	70.1	5.7	91	25	10.2	350
BZW04P48	P BZW04P48B	5	47.8	53.2	56	61.6	1	77	5.2	100	23	10.3	320
P BZW04-48	P BZW04-48B	5	47.8	53.2	56	58.8	1	77	5.2	100	23	10.3	320
BZW04P53	BZW04P53B	5	53.0	58.9	62	68.2	1	85	4.7	111	21	10.4	290
BZW04-53	BZW04-53B	5	53.0	58.9	62	65.1	1	85	4.7	111	21	10.4	290
P BZW04P58	P BZW04P58B	5	58.1	64.6	68	74.8	1	92	4.3	121	19	10.4	270
BZW04-58	BZW04-58B	5	58.1	64.6	68	71.4	1	92	4.3	121	19	10.4	270
BZW04P64	BZW04P64B	5	64.1	71.3	75	82.5	1	103	3.9	134	17	10.5	250
P BZW04-64	BZW04-64B	5	64.1	71.3	75	78.8	1	103	3.9	134	17	10.5	250
BZW04P70	BZW04P70B	5	70.1	77.9	82	90 2	1	113	3.5	146	16	10.5	230
BZW04-70	P BZW04-70B	5	70.1	77.9	82	86.1	1	113	3.5	146	16	10.5	230
BZW04P78	BZW04P78B	5	77.8	86.5	91	100	1	125	3.2	162	14	10.6	210
BZW04-78	BZW04-78B	5	77.8	86.5	91	95.5	1	125	3.2	162	14	10.6	210
P BZW04P85	P BZW04P85B	5	85.5	95.0	100	110	1	137	2.9	178	13	10.6	200
BZW04-85	BZW04-85B	5	85.5	95.0	100	105	1	137	2.9	178	13	10 6	200
BZW04P94	BZW04P94B	5	94.0	105	110	121	1	152	2.6	195	12	10.7	185
BZW04-94	BZW04-94B	5	94.0	105	110	116	1	152	2.6	195	12	10.7	185
BZW04P102	BZW04P102B	5	102	114	120	132	1	165	2.4	212	11	10.7	170
BZW04-102	BZW04-102B	5	102	114	120	126	1	165	2.4	212	11	10.7	170
BZW04P111	P BZW04P111B	5	111	124	130	143	1	179	2 2	230	10	10.7	165
BZW04-111	BZW04-111B	5	111	124	130	137	1	179	2 2	230	10	10.7	165
P BZW04P128	P BZW04P128B	5	128	143	150	165	1	207	2 0	265	9	10.8	145
BZW04-128	BZW04-128B	5	128	143	150	158	1	207	2.0	265	9	10.8	145
P BZW04P136	P BZW04P136B	5	136	152	160	176	1	219	1.8	282	8	10.8	140
P BZW04-136	P BZW04-136B	5	136	152	160	168	1	219	1.8	282	8	10.8	140
P BZW04P145	P BZW04P145B	5	145	161	170	187	1	234	1.7	301	7.5	10.8	135
BZW04-145	BZW04-145B	5	145	161	170	179	1	234	1.7	301	7 5	10.8	135
BZW04P154	BZW04P154B	5	154	171	180	198	1	246	1.6	317	7	10.8	125
BZW04-154	BZW04-154B	5	154	171	180	189	1	246	1.6	317	7	10 8	125
BZW04P171	BZW04P171B	5	171	190	200	220	1	274	1.5	353	6.5	10.8	120
BZW04-171	BZW04-171B	5	171	190	200	210	1	274	1.5	353	6.5	10.8	120
BZW04P188	P BZW04P188B	5	188	209	220	242	1	328	1.4	388	6	10.8	110
BZW04-188	BZW04-188B	5	188	209	220	231	1	328	1.4	388	6	10.8	110
BZW04P213	P BZW04P213B	5	213	237	250	275	1	344	1.5	442	5.2	11	100
BZW04-213	BZW04-213B	5	213	237	250	263	1	344	1.5	442	5.2	11	100
P BZW04P239	P BZW04P239B	5	239	266	280	308	1	384	1.5	494	4.6	11	95
BZW04-239	BZW04-239B	5	239	266	280	294	1	384	1.5	494	4.6	11	95

P = Prevered device

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
BZW04P256	BZW04P256B	5	256	285	300	330	1	414	1.2	529	4.3	11	90
BZW04-256	BZW04-256B	5	256	285	300	315	1	414	1.2	529	4.3	11	90
BZW04P273	BZW04P273B	5	273	304	320	352	1	438	1.2	564	4	11	85
BZW04-273	BZW04-273B	5	273	304	320	336	1	438	1.2	564	4	11	85
BZW04P299	P BZW04P299B	5	299	332	350	385	1	482	0.9	618	3.7	11	80
P BZW04-299	P BZW04-299B	5	299	332	350	368	1	482	0.9	618	3.7	11	80
BZW04P342	P BZW04P342B	5	342	380	400	440	1	548	0.9	706	3.2	11	75
BZW04-342	P BZW04-342B	5	342	380	400	420	1	548	0.9	706	3.2	11	75
P BZW04P376	P BZW04P376B	5	376	418	440	484	1	603	0.8	776	3	11	70
BZW04-376	P BZW04-376B	5	376	418	440	462	1	603	0.8	776	3	11	70

All parameters tested at 25 °C, except where indicated.

P = Prefered device

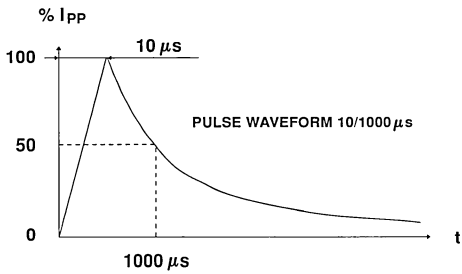
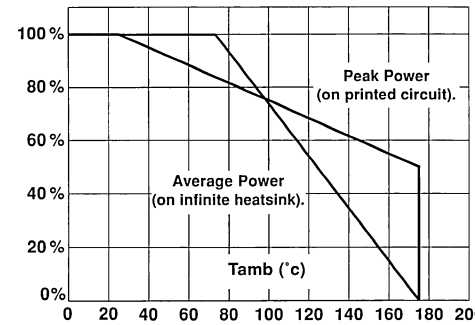


Figure 1: Power dissipation derating versus ambient temperature



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode

Note 2 : Pulse test. $T_P < 50$ ms

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2

Figure 2 : Peak pulse power versus exponential pulse duration.

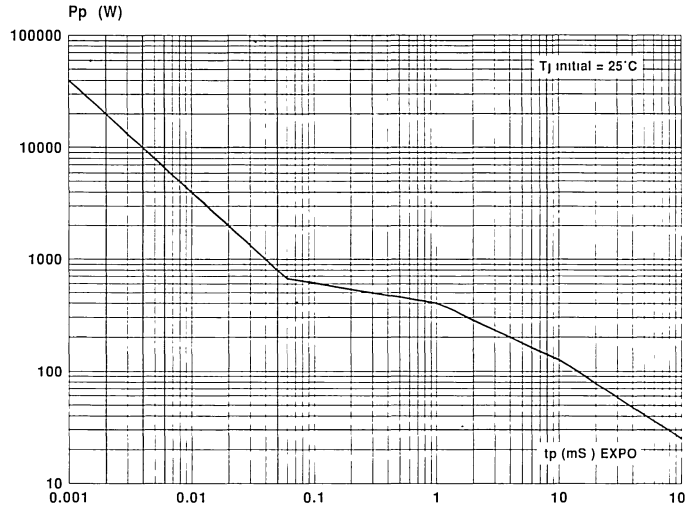
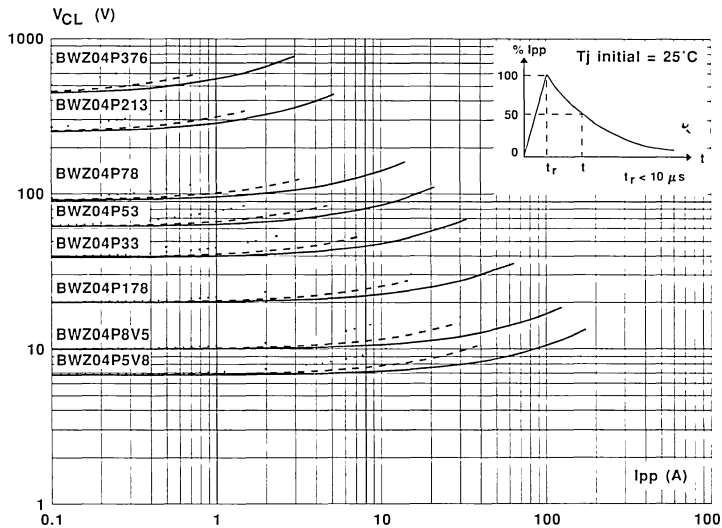


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} \cdot [T_a - 25] \cdot V_{(BR)}$.
For intermediate voltages, extrapolate the given results

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

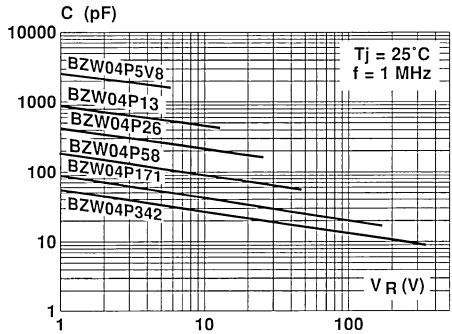


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

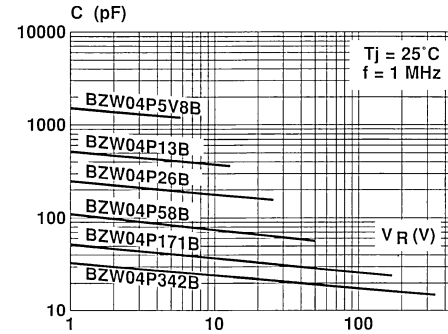


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

Note : For units with V_{BR} > 200 V
V_F is twice than shown

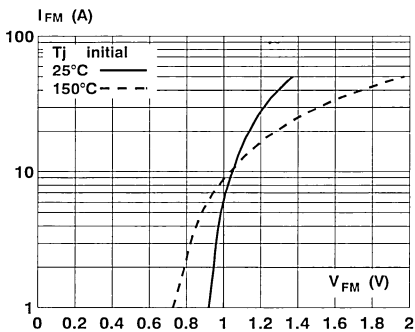
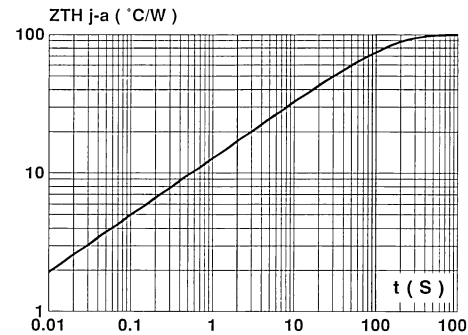
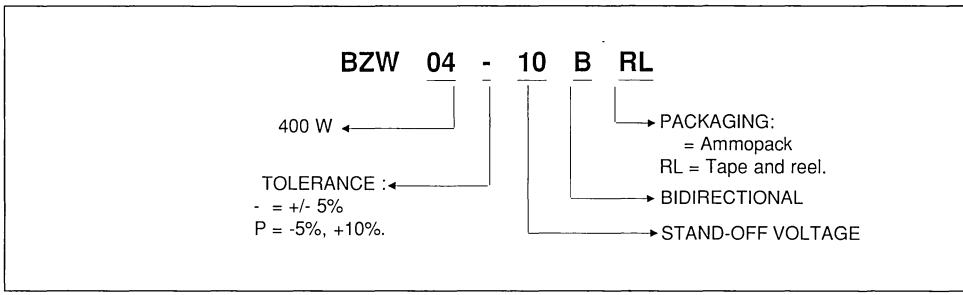


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with L_{lead} = 10mm.



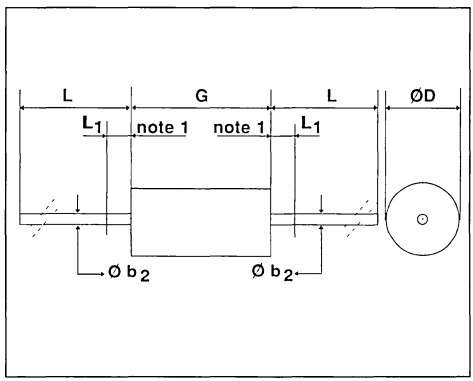
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

F 126 (Plastic).



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	0.76	0.86	0.029	0.034
Ø D	2.95	3.05	0.116	0.120
G	6.05	6.35	0.238	0.250
L	26	-	1.024	-
L_1	-	1.27	-	0.050

note1:The diameter Ø b_2 is not controlled over zone L_1

Weight = 0.4 g.

Packaging : standard packaging is in tape and reel.

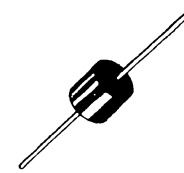
SGS-THOMSON MICROELECTRONICS

BZW50-10,B/180,B

TRANSIL

FEATURES

- PEAK PULSE POWER= 5000 W @ 1ms.
- STAND-OFF VOLTAGE RANGE : From 10V to 180 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).



AG
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

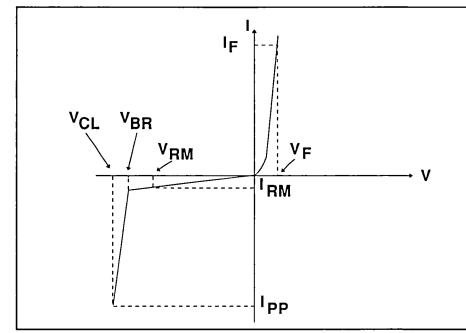
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	5000	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	6.5	W
I_{FSM}	Non repetitive surge peak forward current For Unidirectional types.	Tamb = 25°C t =10 ms	500	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 175	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	15	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. L_{lead} = 10 mm	65	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.



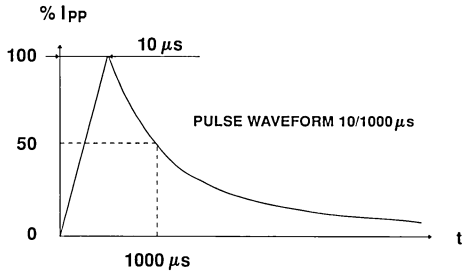
TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min	nom	max note2		V_{CL}@ I_{PP} max 10/1000µs		V_{CL}@ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	Bidirectional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
BZW50-10	BZW50-10B	5	10	11.1	12.4	13.6	1	18.8	266	23.4	2564	7.8	24000
BZW50-12	BZW50-12B	5	12	13.3	14.8	16.3	1	22	227	28	2143	8.4	18500
BZW50-15	BZW50-15B	5	15	16.6	18.5	20.4	1	26.9	186	35	1714	8.8	13500
BZW50-18	BZW50-18B	5	18	20	22.2	24.4	1	32.2	155	41.5	1446	9.2	11500
BZW50-22	BZW50-22B	5	22	24.4	27.1	29.8	1	39.4	127	51	1177	9.6	8500
BZW50-27	BZW50-27B	5	27	30	33.3	36.6	1	48.3	103	62	968	9.8	7000
BZW50-33	BZW50-33B	5	33	36.6	40.7	44.7	1	59	85	76	789	1.0	5750
BZW50-39	BZW50-39B	5	39	43.3	48.1	53	1	69.4	72	90	667	10.1	4800
BZW50-47	BZW50-47B	5	47	52	57.8	63.6	1	83.2	60.1	108	556	10.3	4100
BZW50-56	BZW50-56B	5	56	62.2	69.1	76	1	99.6	50	129	465	10.4	3400
BZW50-68	BZW50-68B	5	68	75.6	84	92.4	1	121	41	157	382	10.5	3000
BZW50-82	BZW50-82B	5	82	91	101.2	111	1	145	34	189	317	10.6	2600
BZW50-100	BZW50-100B	5	100	111	123.5	136	1	179	28	228	263	10.7	2300
BZW50-120	BZW50-120B	5	120	133	148.1	163	1	215	23	274	219	10.8	1900
BZW50-150	BZW50-150B	5	150	166	185.2	204	1	269	19	343	175	10.8	1700
BZW50-180	BZW50-180B	5	180	200	222	244	1	322	16	410	146	10.8	1500

All parameters tested at 25 °C, except where indicated.

Note 2 : Pulse test: $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Figure 1: Power dissipation derating versus ambient temperature

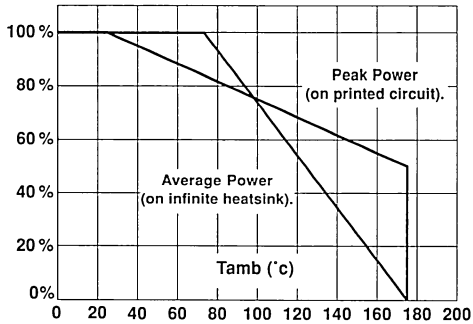


Figure 2 : Peak pulse power versus exponential pulse duration.

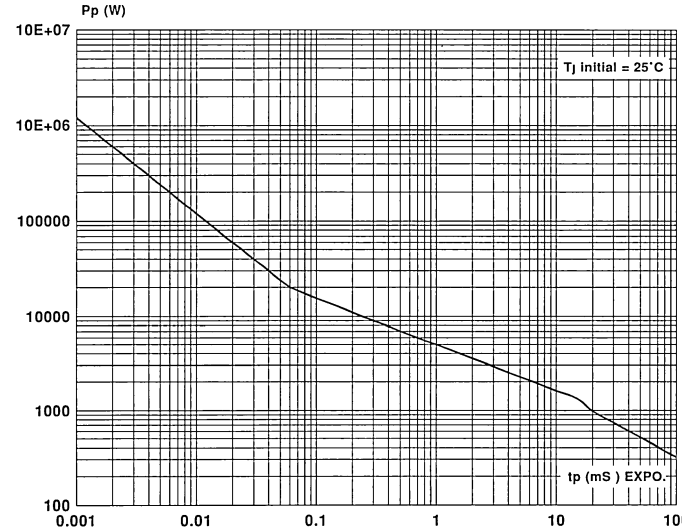
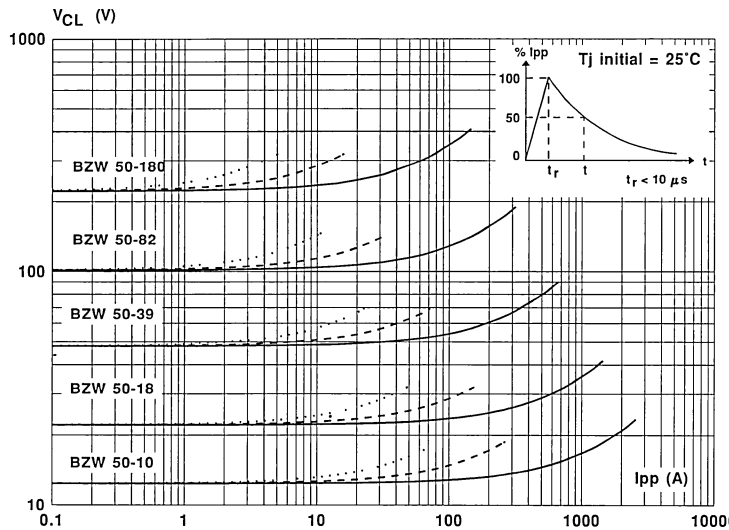


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} * [T_a - 25] * V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

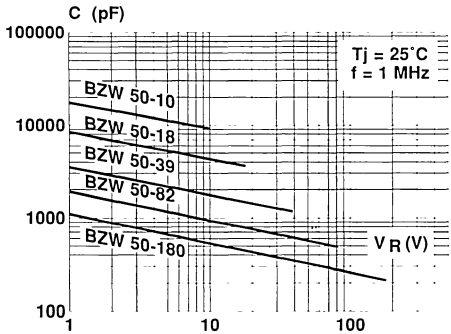


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

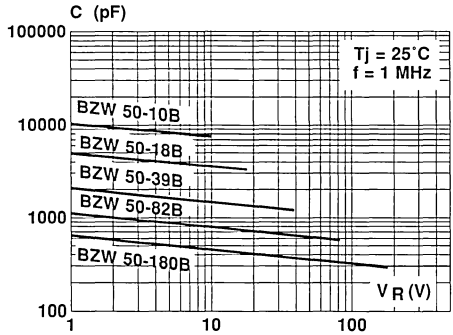


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

Note : For units with V_{BR} > 200 V
V_F is twice than shown.

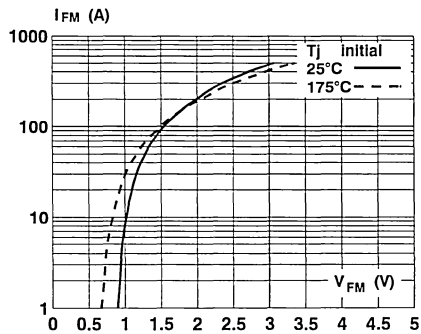
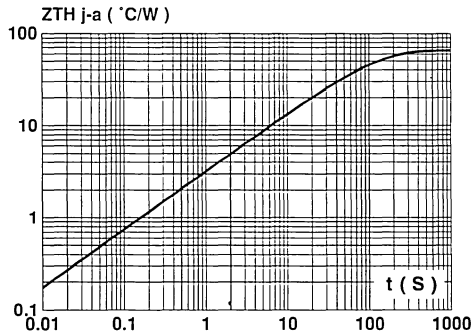
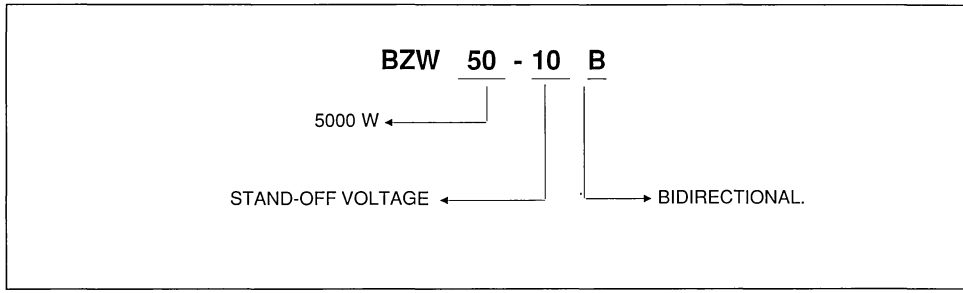


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with L_{lead} = 10mm.



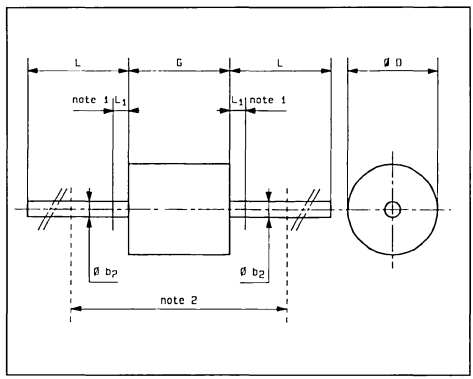
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

AG plastic.



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	1.35	1.45	0.053	0.057
Ø D	-	8	-	0.315
G	-	9.8	-	0.354
L	20	-	0.787	-
L_1	-	1.27	-	0.050

note 1 : The lead diameter Ø b_2 is not controlled over zone L_1
note 2 : 20mm minimum between bendings

Weight = 1.6 g.

Packaging : standard packaging is in bulk.

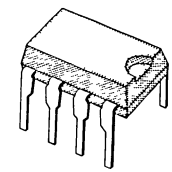
SGS-THOMSON MICROELECTRONICS

L3100B
L3100B1

PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR AND CURRENT LIMITER

FEATURES

- UNIDIRECTIONAL FUNCTION
- PROGRAMMABLE BREAKDOWN VOLTAGE UP TO 265 V
- PROGRAMMABLE CURRENT LIMITATION FROM 50 mA TO 550 mA
- HIGH SURGE CURRENT CAPABILITY
  I_{PP} = 100A 10/1000 µs



DIL 8
(Plastic)

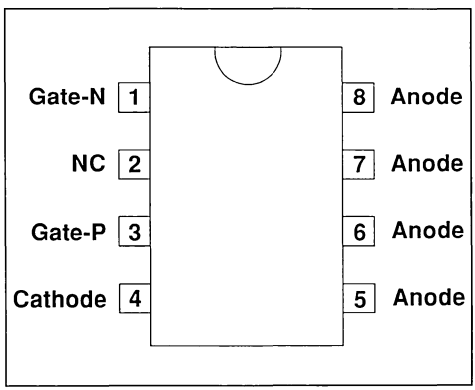
DESCRIPTION

Dedicated to sensitive telecom equipment protection, this device can provide both voltage protection and current limitation with a very tight tolerance.
Its high surge current capability makes the L3100B a reliable protection device for very exposed equipment, or when series resistors are very low.
The breakdown voltage can be easily programmed by using an external zener diode.
A multiple protection mode can also be performed when using several zener diodes, providing each line interface with an optimized protection level.
The current limiting function is achieved with the use of a resistor between the gate and the cathode. The value of the resistor will determine the level of the desired current.

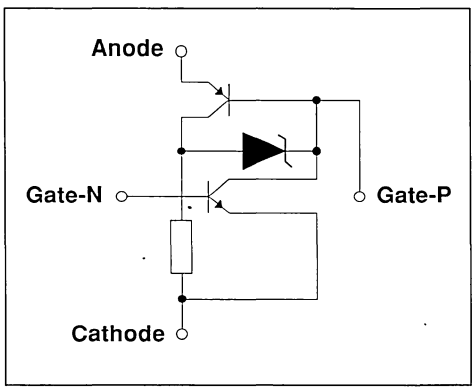
IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

CONNECTION DIAGRAM

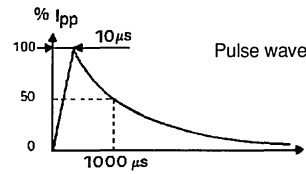


SCHEMATIC DIAGRAM



ABSOLUTE RATINGS (limiting values) (- 40°C ≤ T_{amb} ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs	100 250	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 10 ms	50	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C



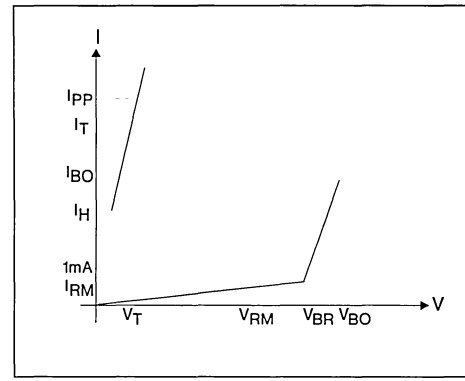
Pulse waveform 10/1000µs

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
R_{th} (j-a)	Junction-to-ambient	80	°C/W

ELECTRICAL CHARACTERISTICS.

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage @ I_T
I_{BO}	Breakover current
I_{PP}	Peak pulse current
V_G	Gate voltage
I_G	Firing gate current



OPERATION WITHOUT GATE.

Type	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} max	@ min note 1	I_{BO} max	I_H min note 1	V_T max note 2	C max note 3
	µA	V	V	mA	V	mA	mA	mA	V	pF
L3100B	6 40	60 250	265	1	350	200	500	280	2	100
L3100B1	6 40	60 250	255	1	350	200	500	210	2	100

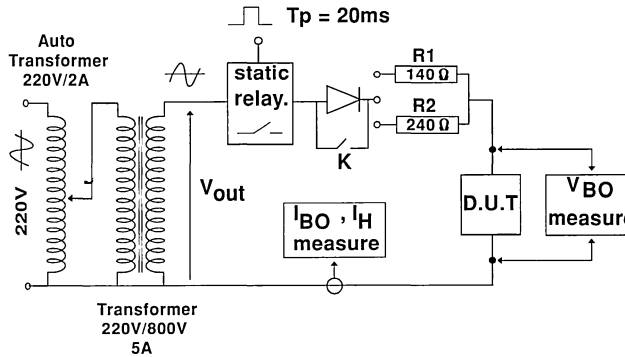
OPERATION WITH GATES.

Type	V_{GN} @ I_{GN} = 200 mA		IGN @ V_{AC} = 100V		V_{RGN} @ I_G = 1mA	I_{GP} @ V_{AC} = 100V
	min	max	min	max	min	max
	V	V	mA	mA	V	mA
L3100B/B1	0.6	1.8	30	200	0.7	150

All parameters tested at 25°C, except where indicated otherwise.

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters
Note 2 : Square pulse T_P= 500µs - I_T = 1A.
Note 3 : V_R = 5 V, f = 1MHz.

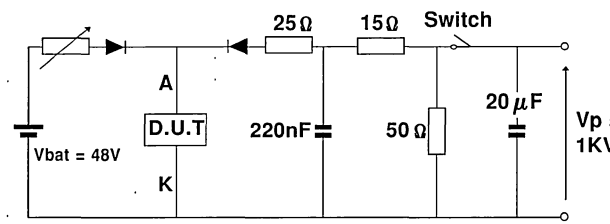
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

Figure 1 : Non-repetitive surge peak on state current versus number of cycles. (with sinusoïdal pulse: F = 50 Hz).

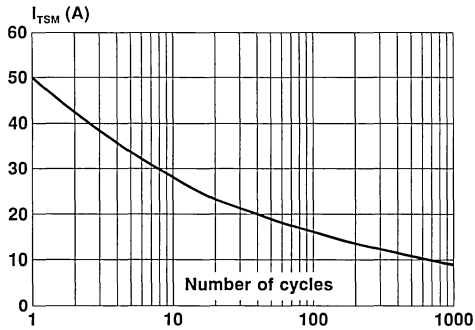


Figure 2 : Relative variation of holding current versus junction temperature.

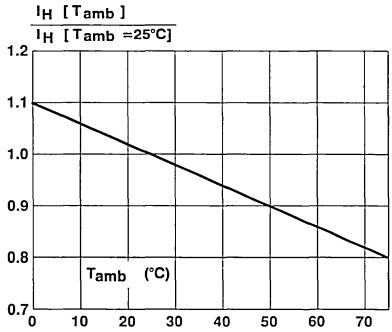


Figure 3 : Relative variation of breakdown voltage versus ambient temperature.

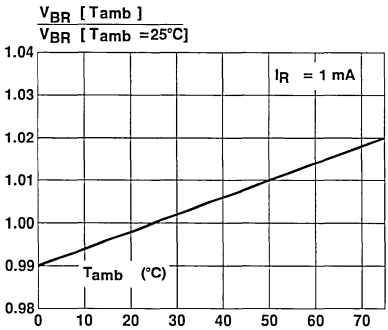
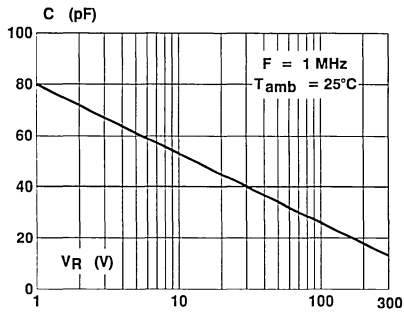


Figure 4 : Junction capacitance versus reverse applied voltage.



APPLICATION CIRCUIT

Overvoltage Protection and Current limitation

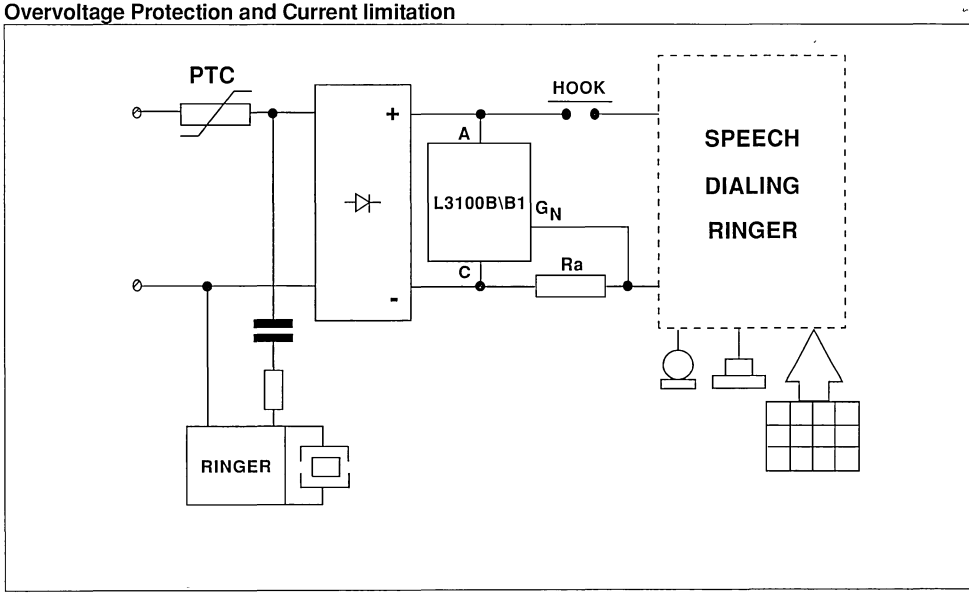
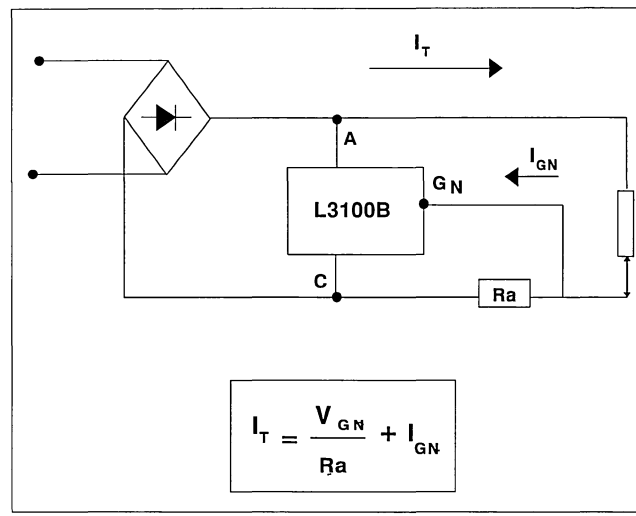


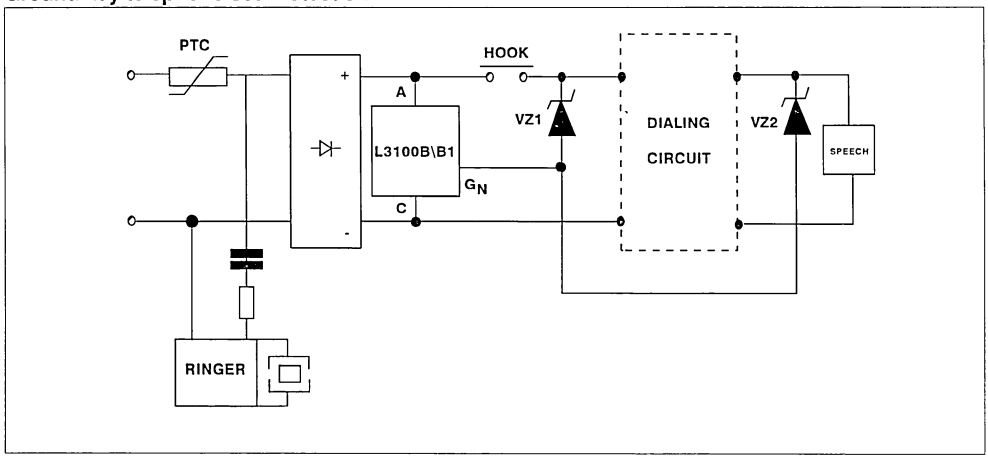
Table below gives the tolerance of the limited current I_T for each standardized resistor value. The formula (1) has been used with V_{GN} values specified at the typical gate current level I_{GN}.

CURRENT TOLERANCE		
R Ω (± 5%)	I_T mA min	I_T mA max
3.00	268	533
3.30	246	503
3.60	228	478
3.90	213	456
4.30	196	433
4.70	181	413
5.10	170	396
5.60	158	379
6.20	145	361
6.80	135	347
7.50	152	333
8.20	117	322
9.10	108	310
10.10	101	299
11.00	95	291
12.00	90	283
13.00	85	277
15.00	78	266
16.00	75	263
18.00	70	256
20.00	66	250
22.00	62	245
24.00	60	242
27.00	56	237
30.00	54	233



V_{GN} @ I_{GN}		
Min	Max	Typ.
V	V	mA
0.75	0.95	100

Ground key telephone set Protection



PROTECTION MODES :

OFF HOOK = Ringer circuit protection is ensured with breakdown voltage at 265 V.

ON HOOK = In dialing mode and in conversation mode, the breakdown voltage of L3100B can be adapted to different levels with two zener diodes.

ORDER CODE

L3100 B 1

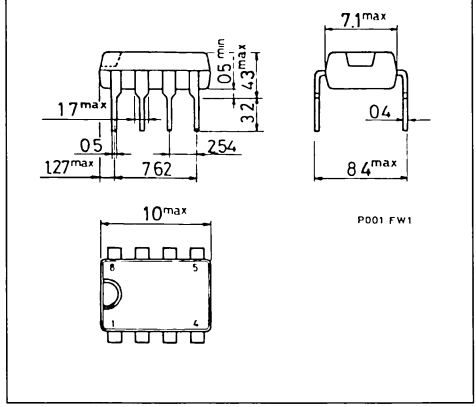
VERSION.
= VBR = 265 V
1 = VBR = 255 V

MARKING : Logo, Date Code,part Number.

PACKAGING : Products supplied in antistatic tubes.

PACKAGE MECHANICAL DATA (in millimeters).

DIL 8 Plastic



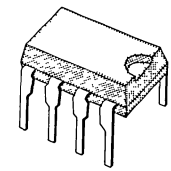
SGS-THOMSON MICROELECTRONICS

LS5018B
LS5060B/LS5120B

TRISIL

FEATURES

- BIDIRECTIONAL CROWBAR PROTECTION.
- BREAKDOWN VOLTAGE RANGE: FROM 18 V To 120 V.
- HOLDING CURRENT = 200 mA min.
- HIGH SURGE CURRENT CAPABILITY I_{PP} = 100A 10/1000 µs

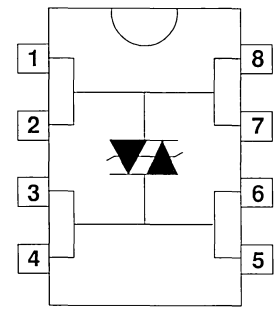


DIL 8
(Plastic)

DESCRIPTION

The LS50xxB series has been designed to protect telecommunication equipment against lightning and transients induced by AC power lines.
Its high surge current capability makes the LS50xxB a reliable protection device for very exposed equipment, or when series resistors are very low.

SCHEMATIC DIAGRAM



IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (- 40°C ≤ T_{amb} ≤ +85°C)

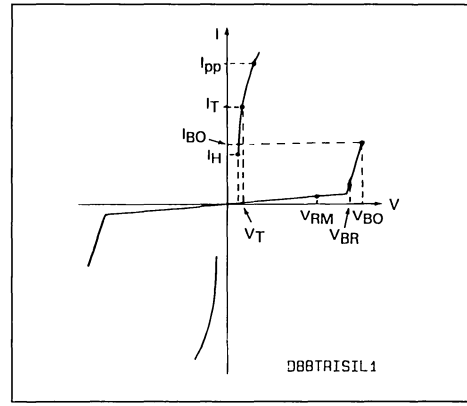
Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs	100 250	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	50	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 150	°C °C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
R_{th} (j-a)	Junction-to-ambient	80	°C/W

ELECTRICAL CHARACTERISTICS.

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage @ I_T
I_{BO}	Breakover current
I_{PP}	Peak pulse current

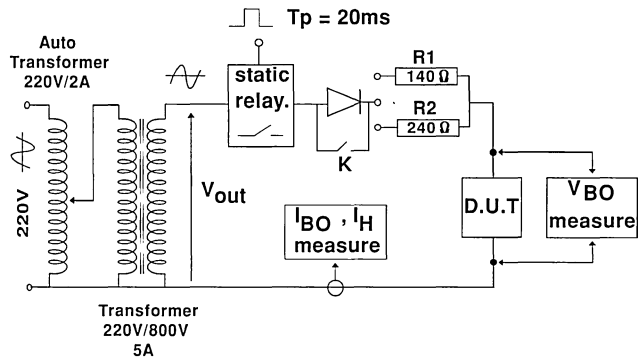


Type	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} max	@ min note 1	I_{BO} max	I_H min note 1	V_T max note 2	C max note 3
	µA	V	V	mA	V	mA	mA	mA	V	pF
LS5018B	5	16	17	1	22		1300	200	3	150
LS5060B	10	50	60	1	85		1000	200	3	150
LS5120B	20	100	120	1	180	500	1250	250	3	150

All parameters tested at 25°C, except where indicated.

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 2 : Square pulse T_P= 500µs - I_T = 1A.
Note 3 : V_R = 5 V, F = 1MHz.

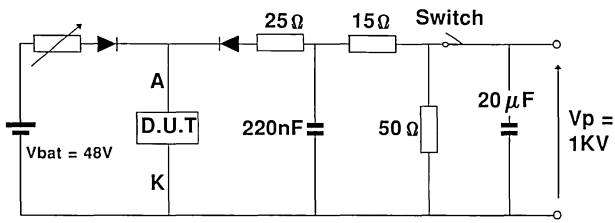
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on state current versus number of cycles. (with sinusoïdal pluse: F = 50 Hz).

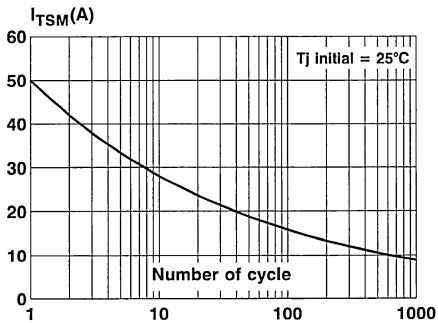


Figure 2 : Relative variation of holding current versus ambient temperature.

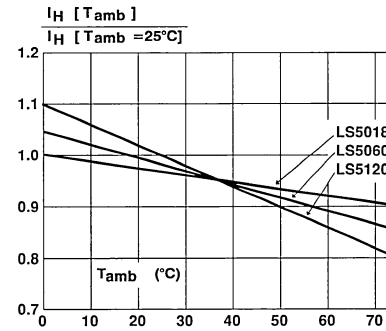


Figure 3 : Relative variation of breakdown voltage versus ambient temperature.

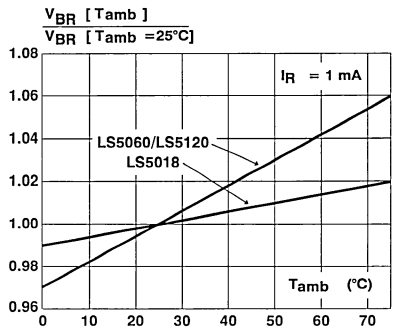
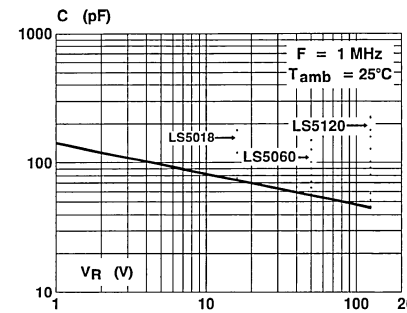
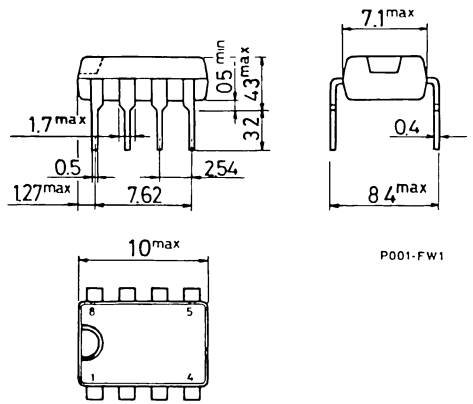


Figure 4 : Junction capacitance versus reverse applied voltage.



PACKAGE MECHANICAL DATA (in millimeters).

DIL 8 Plastic



MARKING : Logo, Date Code,part Number.

PACKAGING : Products supplied in antistatic tubes.

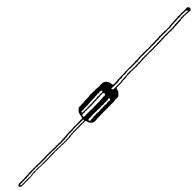
SGS-THOMSON MICROELECTRONICS

P6KE6V8P,A/440P,A
P6KE6V8CP,A/440CP,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 600 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 440 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).
- UL RECOGNIZED.



CB417
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code, and Cathode Band (for unidirectional types only).
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

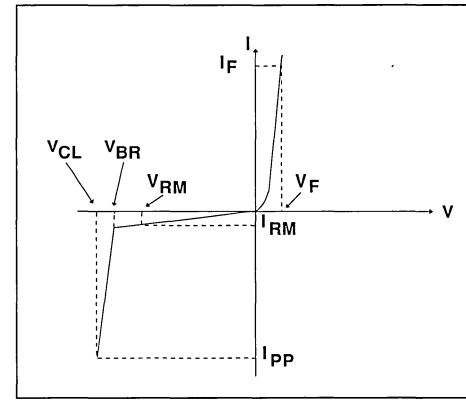
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	600	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	5	W
I_{FSM}	Non repetitive surge peak forward current For Unidirectional types.	Tamb = 25°C t =10 ms	100	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 175	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	20	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. L_{lead} = 10 mm	85	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 50 A.



TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
P6KE6V8P	P6KE6V8CP	1000	5.8	6.45	6.8	7.48	10	10.5	57	13.4	298	5.7	4000
P6KE6V8A	P6KE6V8CA	1000	5.8	6.45	6.8	7.14	10	10.5	57	13.4	298	5.7	4000
P6KE7V5P	P6KE7V5CP	500	6.4	7.13	7.5	8.25	10	11.3	53	14.5	276	6.1	3700
P6KE7V5A	P6KE7V5CA	500	6.4	7.13	7.5	7.88	10	11.3	53	14.5	276	6.1	3700
P6KE8V2P	P6KE8V2CP	200	7.02	7.79	8.2	9.02	10	12.1	50	15.5	258	6.5	3400
P6KE8V2A	P6KE8V2CA	200	7.02	7.79	8.2	8.61	10	12.1	50	15.5	258	6.5	3400
P6KE9V1P	P6KE9V1CP	50	7.78	8.65	9.1	10	1	13.4	45	17.1	234	6.8	3100
P6KE9V1A	P6KE9V1CA	50	7.78	8.65	9.1	9.55	1	13.4	45	17.1	234	6.8	3100
P6KE10P	P6KE10CP	10	8.55	9.5	10	11	1	14.5	41	18.6	215	7.3	2800
P6KE10A	P6KE10CA	10	8.55	9.5	10	10.5	1	14.5	41	18.6	215	7.3	2800
P6KE11P	P6KE11CP	5	9.4	10.5	11	12.1	1	15.6	38	20.3	197	7.5	2500
P6KE11A	P6KE11CA	5	9.4	10.5	11	11.6	1	15.6	38	20.3	197	7.5	2500
P6KE12P	P6KE12CP	5	10.2	11.4	12	13.2	1	16.7	36	21.7	184	7.8	2300
P6KE12A	P6KE12CA	5	10.2	11.4	12	12.6	1	16.7	36	21.7	184	7.8	2300
P6KE13P	P6KE13CP	5	11.1	12.4	13	14.3	1	18.2	33	23.6	169	8.1	2150
P6KE13A	P6KE13CA	5	11.1	12.4	13	13.7	1	18.2	33	23.6	169	8.1	2150
P6KE15P	P6KE15CP	5	12.8	14.3	15	16.5	1	21.2	28	27.2	147	8.4	1900
P6KE15A	P6KE15CA	5	12.8	14.3	15	15.8	1	21.2	28	27.2	147	8.4	1900
P6KE16P	P6KE16CP	5	13.6	15.2	16	17.6	1	22.5	27	28.9	138	8.6	1800
P6KE16A	P6KE16CA	5	13.6	15.2	16	16.8	1	22.5	27	28.9	138	8.6	1800
P6KE18P	P6KE18CP	5	15.3	17.1	18	19.8	1	25.2	24	32.5	123	8.8	1600
P6KE18A	P6KE18CA	5	15.3	17.1	18	18.9	1	25.2	24	32.5	123	8.8	1600
P6KE20P	P6KE20CP	5	17.1	19	20	22	1	27.7	22	36.1	111	9.0	1500
P6KE20A	P6KE20CA	5	17.1	19	20	21	1	27.7	22	36.1	111	9.0	1500
P6KE22P	P6KE22CP	5	18.8	20.9	22	24.2	1	30.6	20	39.3	102	9.2	1350

P = Prefered device

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	Bidirectional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
P6KE22A	P6KE22CA	5	18.8	20.9	22	23.1	1	30.6	20	39.3	102	9.2	1350
P6KE24P	P6KE24CP	5	20.5	22.8	24	26.4	1	33.2	18	42.8	93	9.4	1250
P P6KE24A	P6KE24CA	5	20.5	22.8	24	25.2	1	33.2	18	42.8	93	9.4	1250
P P6KE27P	P P6KE27CP	5	23.1	25.7	27	29.7	1	37.5	16	48.3	83	9.6	1150
P6KE27A	P6KE27CA	5	23.1	25.7	27	28.4	1	37.5	16	48.3	83	9 6	1150
P P6KE30P	P P6KE30CP	5	25.6	28.5	30	33	1	41.5	14.5	53.5	75	9.7	1075
P P6KE30A	P P6KE30CA	5	25.6	28.5	30	31.5	1	41.5	14.5	53.5	75	9.7	1075
P6KE33P	P6KE33CP	5	28.2	31.4	33	36.3	1	45.7	13.1	59.0	68	9.8	1000
P P6KE33A	P P6KE33CA	5	28.2	31.4	33	34.7	1	45.7	13.1	59.0	68	9.8	1000
P P6KE36P	P P6KE36CP	5	30.8	34.2	36	39.6	1	49.9	12	64.3	62	9.9	950
P P6KE36A	P6KE36CA	5	30.8	34.2	36	37.8	1	49.9	12	64.3	62	9.9	950
P P6KE39P	P P6KE39CP	5	33.3	37.1	39	42.9	1	53.9	11.1	69.7	57	10.0	900
P P6KE39A	P P6KE39CA	5	33.3	37.1	39	41.0	1	53.9	11.1	69.7	57	10.0	900
P6KE43P	P6KE43CP	5	36.8	40.9	43	47.3	1	59.3	10.1	76.8	52	10.1	850
P6KE43A	P6KE43CA	5	36.8	40.9	43	45.2	1	59.3	10.1	76.8	52	10.1	850
P6KE47P	P P6KE47CP	5	40.2	44.7	47	51.7	1	64.8	9.3	84	48	10.1	800
P6KE47A	P P6KE47CA	5	40.2	44.7	47	49.4	1	64.8	9.3	84	48	10.1	800
P6KE51P	P P6KE51CP	5	43.6	48.5	51	56.1	1	70.1	8.6	91	44	10.2	750
P6KE51A	P P6KE51CA	5	43.6	48.5	51	53.6	1	70.1	8.6	91	44	10.2	750
P6KE56P	P P6KE56CP	5	47.8	53.2	56	61.6	1	77	7.8	100	40	10.3	700
P6KE56A	P6KE56CA	5	47.8	53.2	56	58.8	1	77	7.8	100	40	10.3	700
P6KE62P	P6KE62CP	5	53.0	58.9	62	68.2	1	85	7.1	111	36	10.4	650
P6KE62A	P6KE62CA	5	53.0	58.9	62	65.1	1	85	7.1	111	36	10.4	650
P6KE68P	P P6KE68CP	5	58.1	64.6	68	74.8	1	92	6.5	121	33	10.4	625
P6KE68A	P6KE68CA	5	58.1	64.6	68	71.4	1	92	6.5	121	33	10.4	625
P6KE75P	P6KE75CP	5	64.1	71.3	75	82.5	1	103	5.8	134	30	10.5	575
P6KE75A	P6KE75CA	5	64.1	71.3	75	78.8	1	103	5.8	134	30	10.5	575
P6KE82P	P P6KE82CP	5	70.1	77.9	82	90.2	1	113	5.3	146	27	10.5	550
P6KE82A	P6KE82CA	5	70.1	77.9	82	86.1	1	113	5.3	146	27	10 5	550
P6KE91P	P6KE91CP	5	77.8	86.5	91	100	1	125	4.8	162	25	10.6	525
P6KE91A	P6KE91CA	5	77.8	86.5	91	95.5	1	125	4.8	162	25	10.6	525
P6KE100P	P6KE100CP	5	85.5	95.0	100	110	1	137	4.4	178	22.5	10.6	500
P6KE100A	P6KE100CA	5	85.5	95.0	100	105	1	137	4.4	178	22.5	10.6	500
P6KE110P	P6KE110CP	5	94.0	105	110	121	1	152	3.9	195	20.5	10.7	470
P6KE110A	P6KE110CA	5	94.0	105	110	116	1	152	3.9	195	20.5	10.7	470
P6KE120P	P6KE120CP	5	102	114	120	132	1	165	3.6	212	19	10.7	450
P6KE120A	P6KE120CA	5	102	114	120	126	1	165	3.6	212	19	10.7	450
P6KE130P	P P6KE130CP	5	111	124	130	143	1	179	3.4	230	17.5	10.7	420
P6KE130A	P6KE130CA	5	111	124	130	137	1	179	3.4	230	17.5	10.7	420
P6KE150P	P P6KE150CP	5	128	143	150	165	1	207	2.9	265	15	10.8	400
P P6KE150A	P P6KE150CA	5	128	143	150	158	1	207	2.9	265	15	10.8	400
P6KE160P	P P6KE160CP	5	136	152	160	176	1	219	2.7	282	14	10.8	380
P6KE160A	P6KE160CA	5	136	152	160	168	1	219	2.7	282	14	10 8	380
P6KE170P	P6KE170CP	5	145	161	170	187	1	234	2.6	301	13	10.8	370
P6KE170A	P6KE170CA	5	145	161	170	179	1	234	2.6	301	13	10.8	370
P6KE180P	P P6KE180CP	5	154	171	180	198	1	246	2.4	317	12.6	10.8	360
P6KE180A	P6KE180CA	5	154	171	180	189	1	246	2.4	317	12.6	10.8	360
P6KE200P	P P6KE200CP	5	171	190	200	220	1	274	2.2	353	11.3	10.8	350
P P6KE200A	P P6KE200CA	5	171	190	200	210	1	274	2.2	353	11.3	10.8	350
P6KE220P	P6KE220CP	5	188	209	220	242	1	328	2	388	10.3	10.8	330
P6KE220A	P6KE220CA	5	188	209	220	231	1	328	2	388	10.3	10.8	330
P6KE250P	P P6KE250CP	5	213	237	250	275	1	344	2	442	9	11	310
P6KE250A	P6KE250CA	5	213	237	250	263	1	344	2	442	9	11	310
P6KE280P	P6KE280CP	5	239	266	280	308	1	384	2	494	8	11	300
P6KE280A	P6KE280CA	5	239	266	280	294	1	384	2	494	8	11	300

P = Prefered device

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
P6KE300P	P6KE300CP	5	256	285	300	330	1	414	1.6	529	7.6	11	290
P6KE300A	P6KE300CA	5	256	285	300	315	1	414	1.6	529	7.6	11	290
P6KE320P	P6KE320CP	5	273	304	320	352	1	438	1.6	564	7.1	11	280
P6KE320A	P6KE320CA	5	273	304	320	336	1	438	1.6	564	7.1	11	280
P6KE350P	P6KE350CP	5	299	332	350	385	1	482	1.6	618	6.5	11	270
P P6KE350A	P6KE350CA	5	299	332	350	368	1	482	1.6	618	6.5	11	270
P P6KE400P	P P6KE400CP	5	342	380	400	440	1	548	1.3	706	5.7	11	360
P6KE400A	P6KE400CA	5	342	380	400	420	1	548	1.3	706	5.7	11	360
P P6KE440P	P P6KE440CP	5	376	418	440	484	1	603	1.3	776	5.2	11	350
P6KE440A	P6KE440CA	5	376	418	440	462	1	603	1.3	776	5.2	11	350

All parameters tested at 25 °C, except where indicated.

P = Prefered device

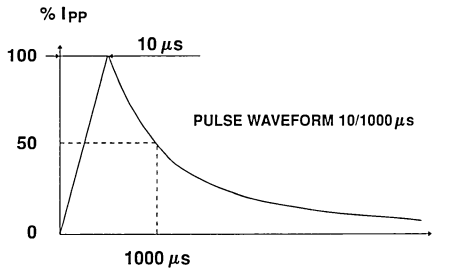
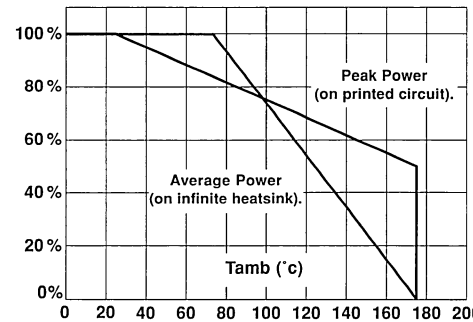


Figure 1: Power dissipation derating versus ambient temperature



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Note 2 : Pulse test: $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.

Figure 2 : Peak pulse power versus exponential pulse duration.

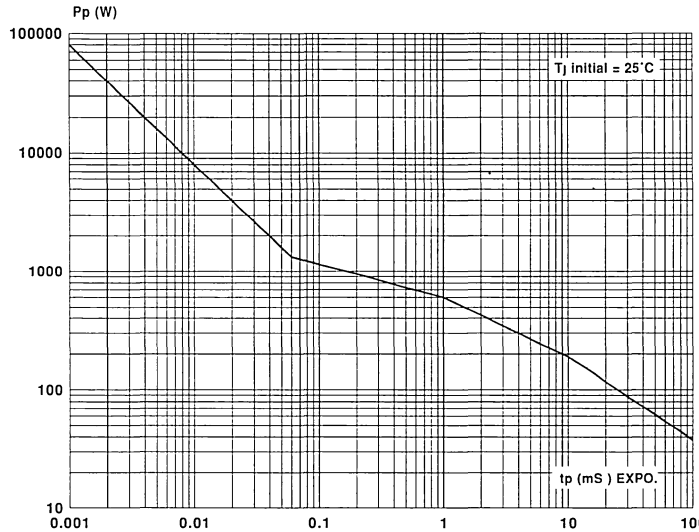
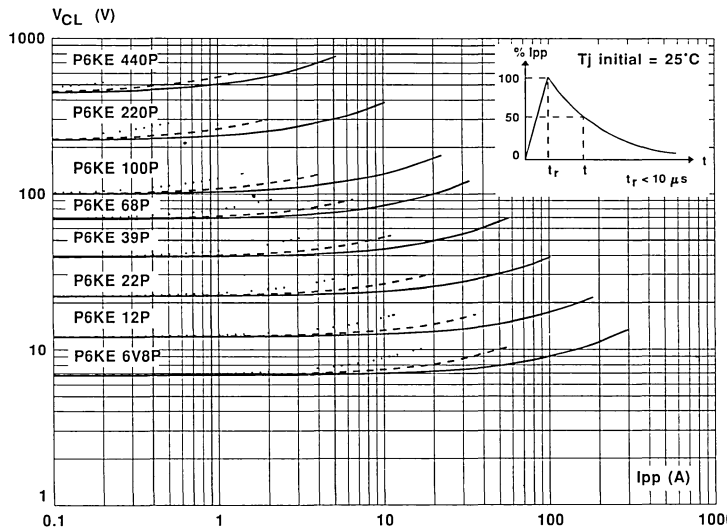


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} \cdot [T_a - 25] \cdot V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

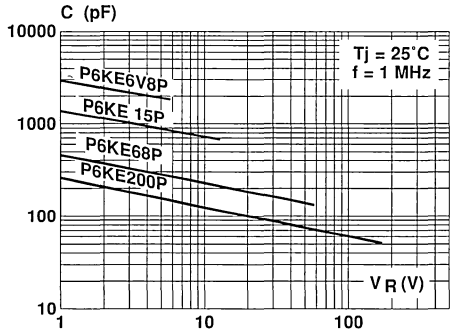


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

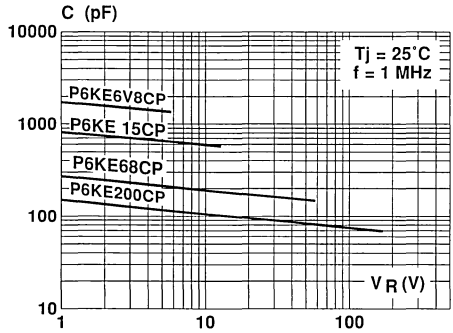


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

Note : For units with $V_{BR} > 200$ V
V_F is twice than shown.

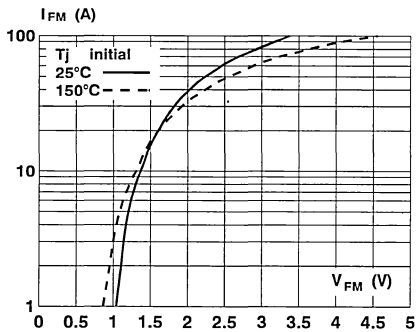
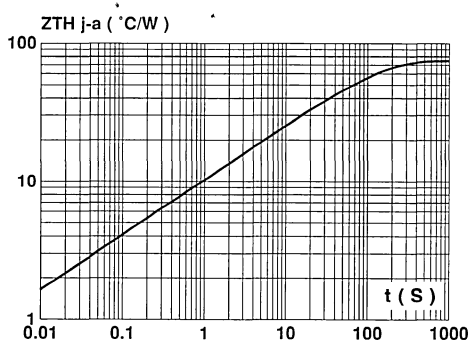
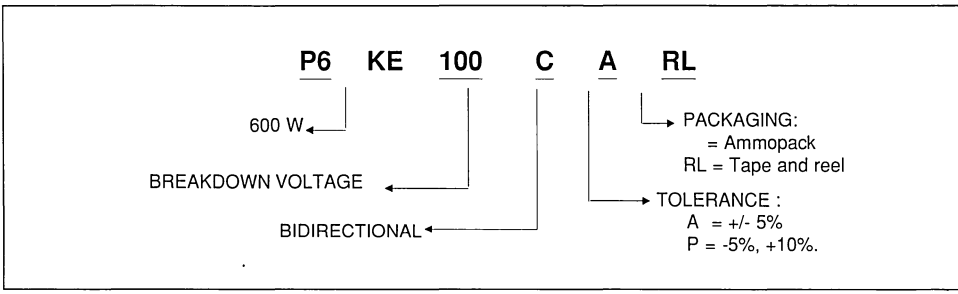


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting with L_{lead} = 10mm.



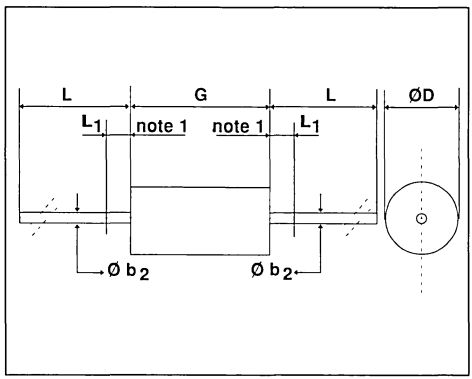
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

CB417 (Plastic).



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	-	1.092	-	0.043
Ø D	-	3.683	-	0.145
G	-	8.89	-	0.350
L	25.4	-	1.000	-
L_1	-	1.25	-	0.049

note1:The diameter Ø b_2 is not controlled over zone L_1

Weight = 0.65 g.

Packaging : standard packaging is in tape and reel.

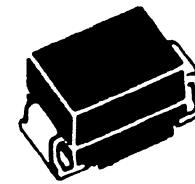
SGS-THOMSON MICROELECTRONICS

SM4T6V8,A/220,A
SM4T6V8C,CA/220C,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 400 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 220 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).
- JEDEC REGISTRED.



SOD 6
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them praticularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Full compatibility with both gluing and paste soldering technologies.
- Excellent on board stability.
- Tinned copper leads.
- High temperature resistant resin.

ABSOLUTE RATINGS (limiting values)

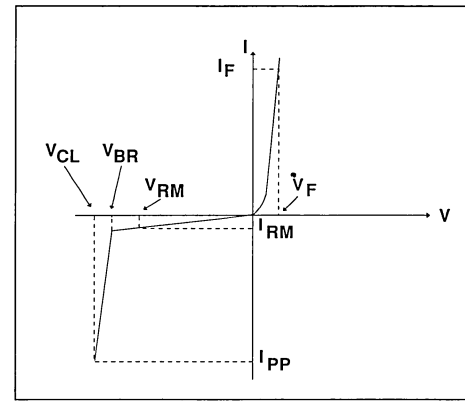
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	400	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 50°C	5	W
I_{FSM}	Non repetitive surge peak forward current. For unidirectional types.	Tamb = 25°C t =10 ms	50	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	20	°C/W
R_{th} (j-a)	Junction to ambiant. on printed circuit. With standard footprint dimensions.	100	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop $V_F < 3.5V$ @ $I_F = 25$ A.



TYPES				I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Uni directional	*	Bi directional	*	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM4T6V8	QD	SM4T6V8C	VD	1000	5.8	6.45	6.8	7.48	10	10.5	38	13.4	174	5.7	3500
SM4T6V8A	QE	SM4T6V8CA	VE	1000	5.8	6.45	6.8	7.14	10	10.5	38	13.4	174	5.7	3500
SM4T7V5	QF	SM4T7V5C	VF	500	6.4	7.13	7.5	8.25	10	11.3	35.4	14.5	160	6.1	3100
SM4T7V5A	QG	SM4T7V5CA	VG	500	6.4	7.13	7.5	7.88	10	11.3	35.4	14.5	160	6.1	3100
SM4T10	QN	SM4T10C	VN	10	8.55	9.5	10	11	1	14.5	27.6	18.6	124	7.3	2000
SM4T10A	QP	SM4T10CA	VP	10	8.55	9.5	10	10.5	1	14.5	27.6	18.6	124	7.3	2000
SM4T12	QS	SM4T12C	VS	5	10.2	11.4	12	13.2	1	16.7	24	21.7	106	7.8	1550
SM4T12A	QT	SM4T12CA	VT	5	10.2	11.4	12	12.6	1	16.7	24	21.7	106	7.8	1550
SM4T15	QW	SM4T15C	VW	5	12.8	14.3	15	16.5	1	21.2	19	27.2	85	8.4	1200
SM4T15A	QX	SM4T15CA	VX	5	12.8	14.3	15	15.8	1	21.2	19	27.2	85	8.4	1200
SM4T18	RD	SM4T18C	UD	5	15.3	17.1	18	19.8	1	25.2	16	32.5	71	8.8	975
SM4T18A	RE	SM4T18CA	UE	5	15.3	17.1	18	18.9	1	25.2	16	32.5	71	8.8	975
SM4T22	RH	SM4T22C	UH	5	18.8	20.9	22	24.2	1	30.6	13	39.3	59	9.2	800
SM4T22A	RK	SM4T22CA	UK	5	18.8	20.9	22	23.1	1	30.6	13	39.3	59	9.2	800
SM4T24	RL	SM4T24C	UL	5	20.5	22.8	24	26.4	1	33.2	12	42.8	54	9.4	725
SM4T24A	RM	SM4T24CA	UM	5	20.5	22.8	24	25.2	1	33.2	12	42.8	54	9.4	725
SM4T27	RN	SM4T27C	UN	5	23.1	25.7	27	29.7	1	37.5	10.7	48.3	48	9.6	625
SM4T27A	RP	SM4T27CA	UP	5	23.1	25.7	27	28.4	1	37.5	10.7	48.3	48	9.6	625
SM4T30	RQ	SM4T30C	UQ	5	25.6	28.5	30	33	1	41.5	9.6	53.5	43	9.7	575
SM4T30A	RR	SM4T30C4	UR	5	25.6	28.5	30	31.5	1	41.5	9.6	53.5	43	9.7	575
SM4T33	RS	SM4T33C	US	5	28.2	31.4	33	36.3	1	45.7	8.8	59.0	39	9.8	510
SM4T33A	RT	SM4T33CA	UT	5	28.2	31.4	33	34.7	1	45.7	8.8	59.0	39	9.8	510
SM4T36	RU	SM4T36C	UU	5	30.8	34.2	36	39.6	1	49.9	8	64.3	36	9.9	480
SM4T36A	RV	SM4T36CA	UV	5	30.8	34.2	36	37.8	1	49.9	8	64.3	36	9.9	480
SM4T39	RW	SM4T39C	UW	5	33.3	37.1	39	42.9	1	53.9	7.4	69.7	33	10.0	450
SM4T39	RX	SM4T39	UX	5	33.3	37.1	39	41.0	1	53.9	7.4	69.7	33	10.0	450

TYPES				I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Uni directional	*	Bi directional	*	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM4T68	SN	SM4T68C	WN	5	58.1	64.6	68	74.8	1	92	4.3	121	19	10.4	270
SM4T68A	SP	SM4T68CA	WP	5	58.1	64.6	68	71.4	1	92	4.3	121	19	10.4	270
SM4T100	SW	SM4T100C	WW	5	85.5	95.0	100	110	1	137	2.9	178	13	10.6	200
SM4T100A	SX	SM4T100CA	WX	5	85.5	95.0	100	105	1	137	2.9	178	13	10.6	200
SM4T150	TH	SM4T150C	XH	5	128	143	150	165	1	207	2.0	265	9	10.8	145
SM4T150A	TK	SM4T150CA	XK	5	128	143	150	158	1	207	2.0	265	9	10.8	145
SM4T200	TS	SM4T200C	XS	5	171	190	200	220	1	274	1.5	353	6.5	10.8	120
SM4T200A	TT	SM4T200CA	XT	5	171	190	200	210	1	274	1.5	353	6.5	10.8	120
SM4T220	TU	SM4T220C	XU	5	188	209	220	242	1	328	1.4	388	6	10.8	110
SM4T220A	TV	SM4T220CA	XV	5	188	209	220	231	1	328	1.4	388	6	10.8	110

All parameters tested at 25 °C, except where indicated.

*** = Marking**

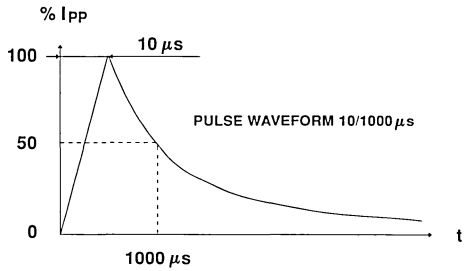
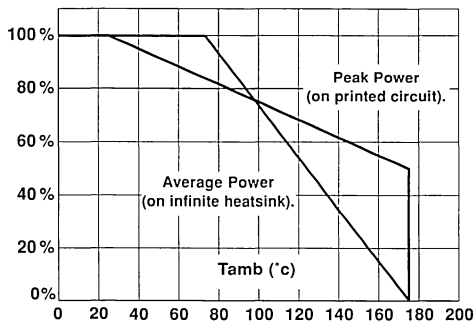


Figure 1: Power dissipation derating versus ambient temperature



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Note 2 : Pulse test. $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$

Note 4 : VR = 0 V, F = 1 MHz For bidirectional types, capacitance value is divided by 2

Figure 2 : Peak pulse power versus exponential pulse duration.

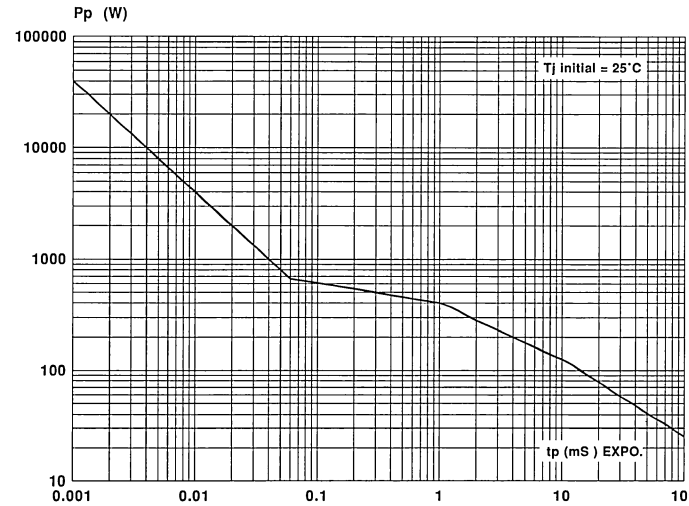
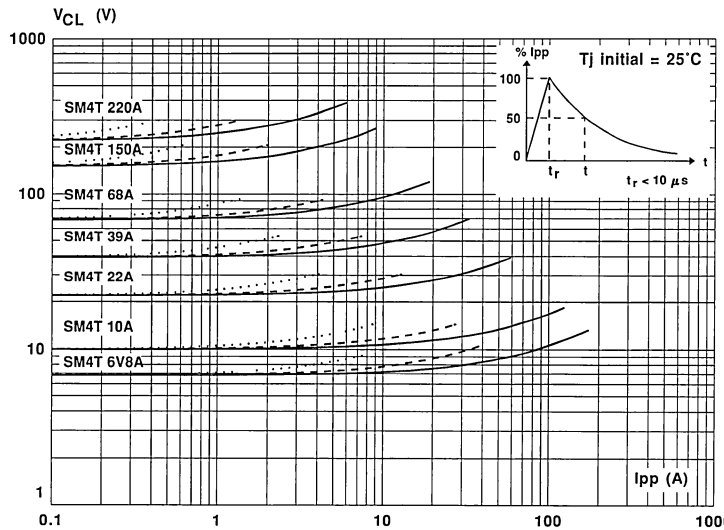


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} \cdot [T_a - 25] \cdot V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

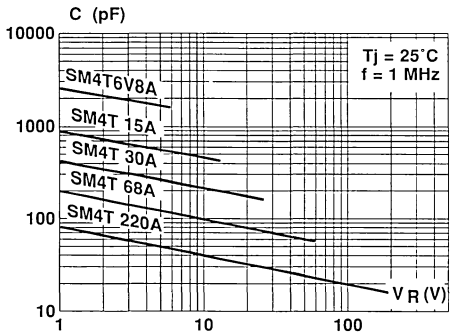


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

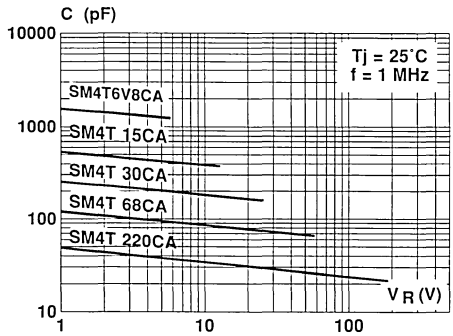


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

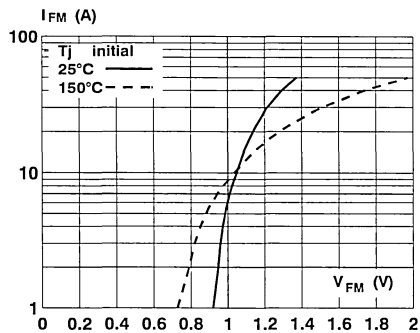
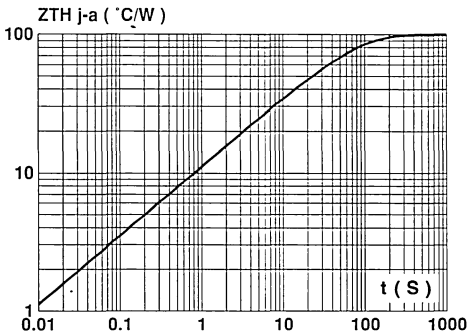
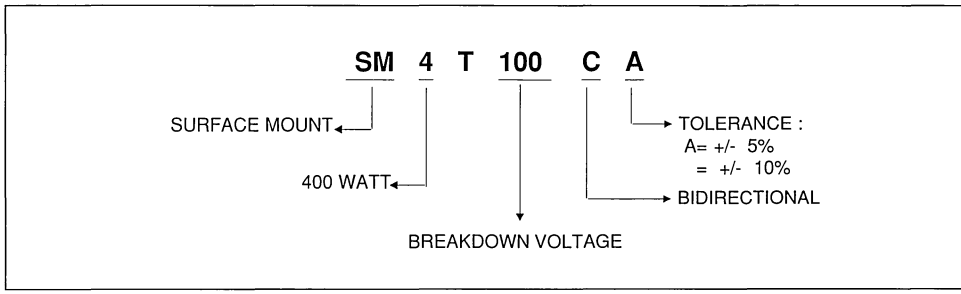


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with standard footprint dimensions.



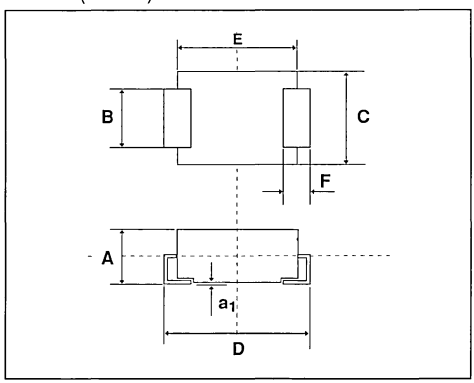
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

SOD 6 (Plastic).

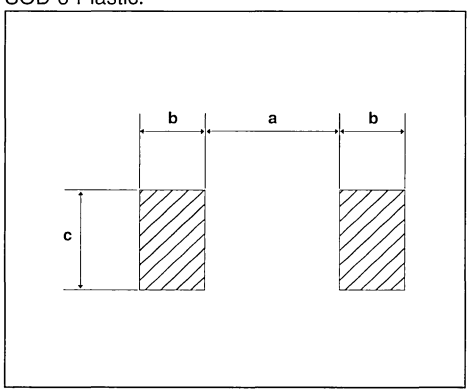


Ref	Millimeters		Inches	
	min	max	min	max
A	2.48	2.61	0.096	0.103
a1	0.10	0.20	0.004	0.008
B	1.96	2.11	0.077	0.083
C	3.65	3.93	0.143	0.155
D	5.39	5.59	0.212	0.220
E	4.15	4.30	0.163	0.170
F	1.00	1.27	0.039	0.050

Weight = 0.12 g.

FOOTPRINT DIMENSIONS (Millimeter).

SOD 6 Plastic.



Ref	Millimeters
a	2.75
b	1.52
c	2.30

Packaging : standard packaging is in film.

SGS-THOMSON MICROELECTRONICS

SM6T6V8,A/220,A
SM6T6V8C,CA/220C,CA

TRANSIL

FEATURES

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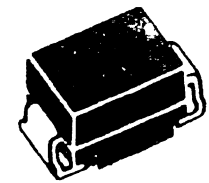

SOD 6
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ELECTRICAL CHARACTERISTICS

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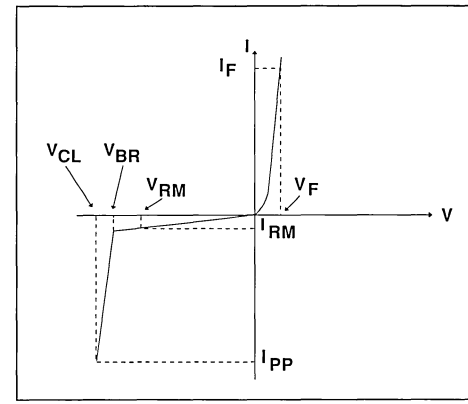
V_F	Forward Voltage drop $V_F < 3.5V$ @ $I_F = 50$ A.

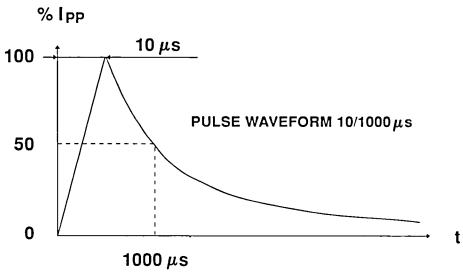


TYPES				I_{RM} @ V_{RM} max		V_{BR} @ I_R min	nom	max		V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Uni directional	*	Bi directional	*	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM6T6V8	DD	SM6T6V8C	LD	1000	5.8	6 45	6.8	7.48	10	10.5	57	13.4	298	5.7	4000
SM6T6V8A	DE	SM6T6V8CA	LE	1000	5.8	6.45	6.8	7.14	10	10.5	57	13.4	298	5.7	4000
SM6T7V5	DF	SM6T7V5C	LF	500	6.4	7.13	7.5	8.25	10	11.3	53	14.5	276	6.1	3700
SM6T7V5A	DG	SM6T7V5CA	LG	500	6.4	7.13	7.5	7.88	10	11.3	53	14.5	276	6.1	3700
SM6T10	DN	SM6T10C	LN	10	8.55	9.5	10	11	1	14.5	41	18.6	215	7.3	2800
SM6T10A	DP	SM6T10CA	LP	10	8.55	9.5	10	10.5	1	14.5	41	18.6	215	7.3	2800
SM6T12	DS	SM6T12C	LS	5	10.2	11.4	12	13.2	1	16.7	36	21.7	184	7.8	2300
SM6T12A	DT	SM6T12CA	LT	5	10.2	11.4	12	12.6	1	16.7	36	21.7	184	7.8	2300
SM6T15	DW	SM6T15C	LW	5	12.8	14.3	15	16.5	1	21.2	28	27.2	147	8.4	1900
SM6T15A	DX	SM6T15CA	LX	5	12.8	14.3	15	15.8	1	21.2	28	27.2	147	8.4	1900
SM6T18	ED	SM6T18C	MD	5	15.3	17.1	18	19.8	1	25.2	24	32.5	123	8.8	1600
SM6T18A	EE	SM6T18CA	ME	5	15.3	17.1	18	18.9	1	25.2	24	32.5	123	8.8	1600
SM6T22	EH	SM6T22C	MH	5	18.8	20.9	22	24.2	1	30.6	20	39.3	102	9.2	1350
SM6T22A	EK	SM6T22CA	MK	5	18.8	20.9	22	23.1	1	30.6	20	39.3	102	9.2	1350
SM6T24	EL	SM6T24C	ML	5	20.5	22.8	24	26.4	1	33.2	18	42.8	93	9.4	1250
SM6T24A	EM	SM6T24CA	MM	5	20.5	22.8	24	25.2	1	33.2	18	42.8	93	9.4	1250
SM6T27	EN	SM6T27C	MN	5	23.1	25.7	27	29.7	1	37.5	16	48.3	83	9.6	1150
SM6T27A	EP	SM6T27CA	MP	5	23.1	25.7	27	28.4	1	37.5	16	48.3	83	9.6	1150
SM6T30	EQ	SM6T30C	MQ	5	25.6	28.5	30	33	1	41.5	14.5	53.5	75	9.7	1075
SM6T30A	ER	SM6T30CA	MR	5	25.6	28.5	30	31.5	1	41.5	14.5	53.5	75	9.7	1075
SM6T33	ES	SM6T33C	MS	5	28.2	31.4	33	36.3	1	45.7	13.1	59.0	68	9.8	1000
SM6T33A	ET	SM6T33CA	MT	5	28.2	31.4	33	34.7	1	45.7	13.1	59.0	68	9.8	1000
SM6T36	EU	SM6T36C	MU	5	30.8	34.2	36	39.6	1	49.9	12	64.3	62	9.9	950
SM6T36A	EV	SM6T36CA	MV	5	30.8	34.2	36	37.8	1	49.9	12	64.3	62	9.9	950
SM6T39	EW	SM6T39C	MW	5	33.3	37.1	39	42.9	1	53.9	11.1	69.7	57	10.0	900
SM6T39	EX	SM6T39	MX	5	33.3	37.1	39	41.0	1	53.9	11.1	69.7	57	10.0	900

TYPES				I_{RM} @ V_{RM}		V_{BR} @ I_R				V_{CL} @ I_{PP}		V_{CL} @ I_{PP}		αT	C
				max		min	nom	max		max		max		max	typ
								note2		10/1000µs		8/20µs		note3	note4
Uni directional	*	Bi directional	*	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM6T68	FP	SM6T68C	NP	5	58.1	64.6	68	74.8	1	92	6.5	121	33	10.4	625
SM6T68A	FQ	SM6T68CA	NQ	5	58.1	64.6	68	71.4	1	92	6.5	121	33	10.4	625
SM6T100	FX	SM6T100C	NX	5	85.5	95.0	100	110	1	137	4.4	178	22.5	10.6	500
SM6T100A	FY	SM6T100CA	NY	5	85.5	95.0	100	105	1	137	4.4	178	22.5	10.6	500
SM6T150	GK	SM6T150C	OK	5	128	143	150	165	1	207	2.9	265	15	10.8	400
SM6T150A	GL	SM6T150CA	OL	5	128	143	150	158	1	207	2.9	265	15	10.8	400
SM6T200	GT	SM6T200C	OT	5	171	190	200	220	1	274	2.2	353	11.3	10.8	350
SM6T200A	GU	SM6T200CA	OU	5	171	190	200	210	1	274	2.2	353	11.3	10.8	350
SM6T220	GV	SM6T220C	OV	5	188	209	220	242	1	328	2	388	10.3	10.8	330
SM6T220A	GW	SM6T220CA	OW	5	188	209	220	231	1	328	2	388	10.3	10.8	330

All parameters tested at 25 °C, except where indicated.

*** = Marking**



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode

Note 2 : Pulse test· $T_P < 50$ ms

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25\,C)}$

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2

Figure 1: Power dissipation derating versus ambient temperature

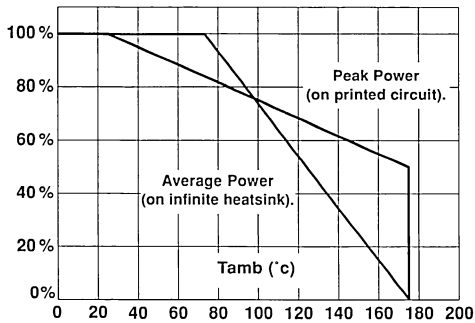


Figure 2 : Peak pulse power versus exponential pulse duration.

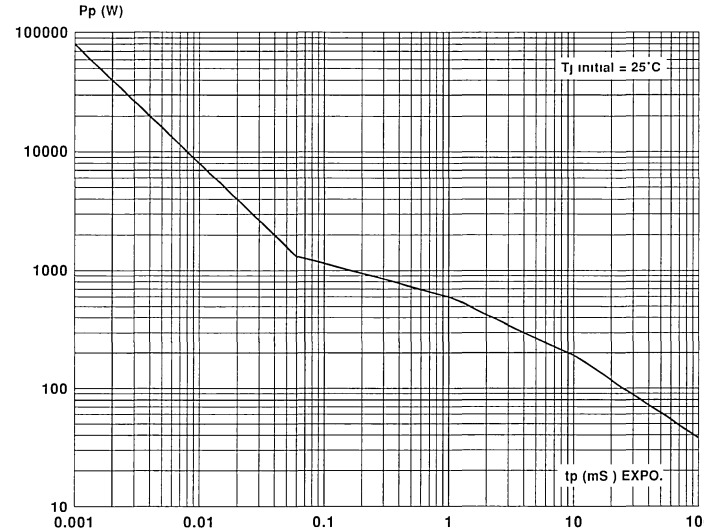
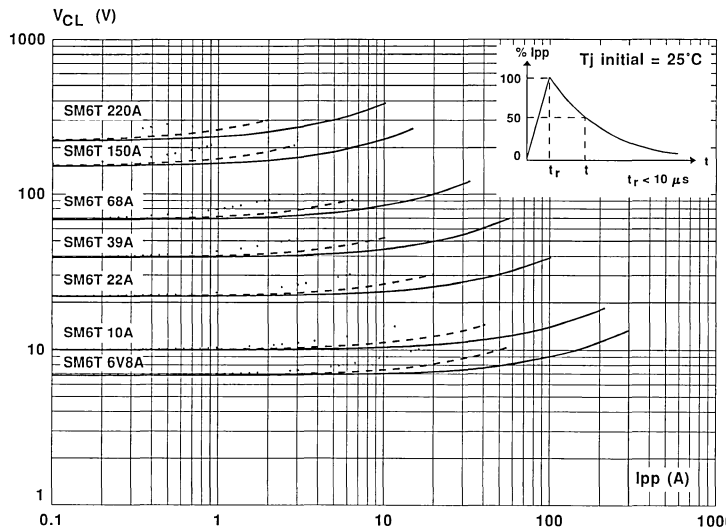


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} * [T_a - 25] * V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

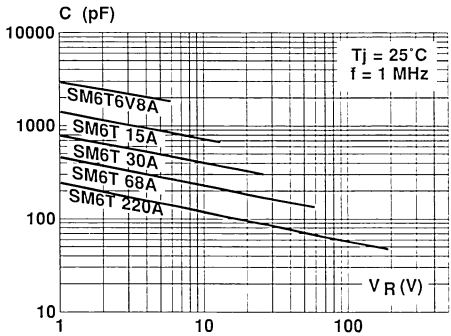


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

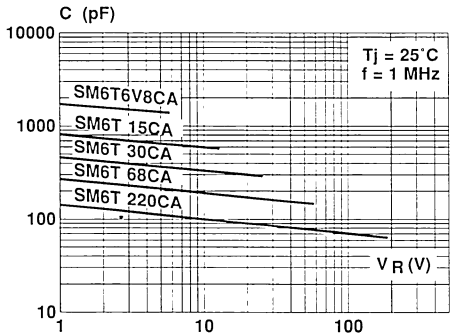


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

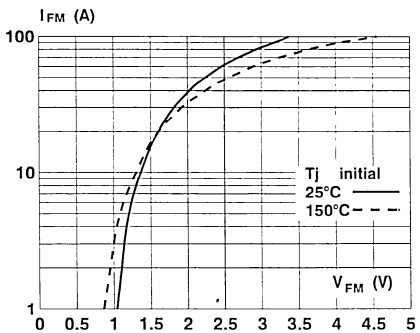
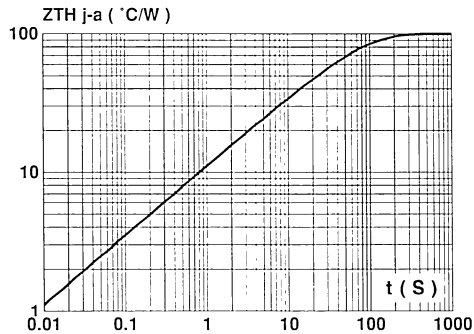
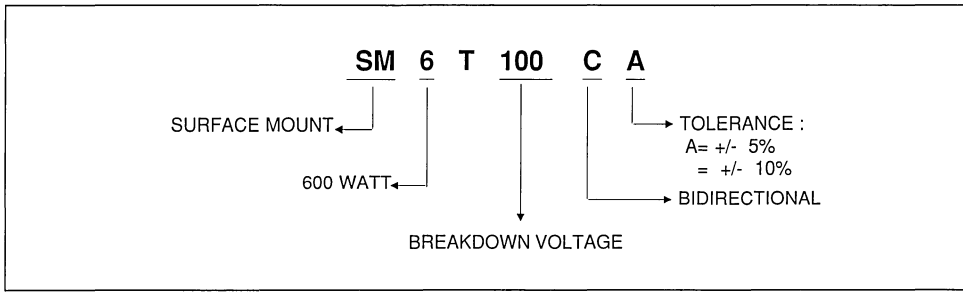


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with standard footprint dimensions.



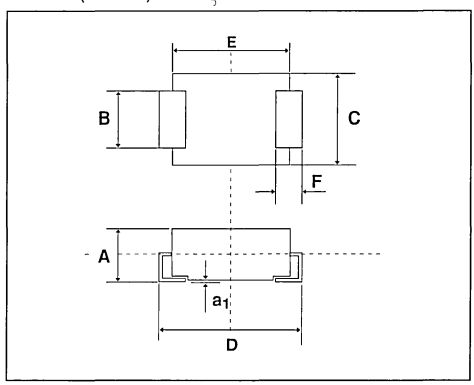
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

SOD 6 (Plastic).

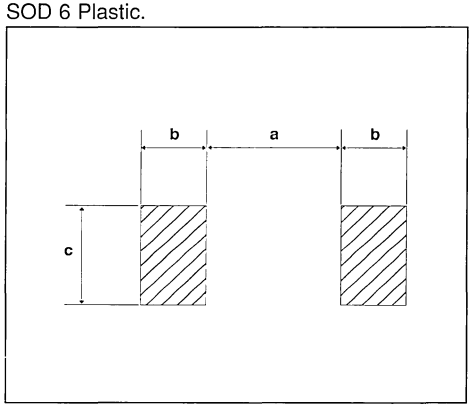


Ref	Millimeters		Inches	
	min	max	min	max
A	2.48	2.61	0.096	0.103
a1	0.10	0.20	0 004	0.008
B	1.96	2.11	0.077	0.083
C	3.65	3.93	0.143	0.155
D	5.39	5.59	0.212	0.220
E	4.15	4.30	0.163	0.170
F	1.00	1.27	0.039	0.050

Weight = 0.12 g.

FOOTPRINT DIMENSIONS (Millimeter).

SOD 6 Plastic.



Ref	Millimeters
a	2.75
b	1.52
c	2.30

Packaging : standard packaging is in film.

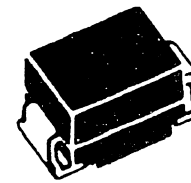
SGS-THOMSON MICROELECTRONICS

SM15T6V8,A/220,A
SM15T6V8C,CA/220C,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 1500 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 220 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).



SOD 15
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code, and Cathode Band (for unidirectional types only).
- Full compatibility with both gluing and paste soldering technologies.
- Excellent on board stability.
- Tinned copper leads.
- High temperature resistant resin.

ABSOLUTE RATINGS (limiting values)

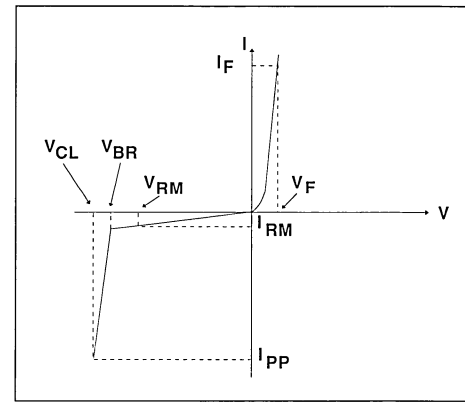
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	1500	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1	Tlead = 50°C	10	W
I_{FSM}	Non repetitive surge peak forward current. For unidirectional types.	Tamb = 25°C t =10 ms	250	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	10	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. With standard footprint dimensions.	75	°C/W

ELECTRICAL CHARACTERISTICS

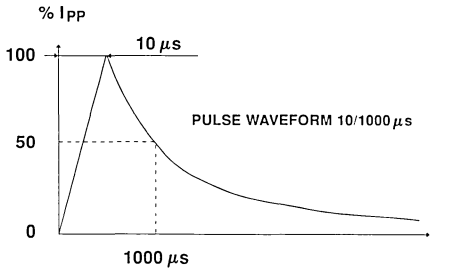
Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 100 A.



TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Uni directional	Bi directional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM15T6V8	SM15T6V8C	1000	5.8	6.45	6.8	7.48	10	10.5	143	13.4	746	5.7	9500
SM15T6V8A	SM15T6V8CA	1000	5.8	6.45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
SM15T7V5	SM15T7V5C	500	6.4	7.13	7 5	8 25	10	11.3	132	14.5	690	6.1	8500
SM15T7V5A	SM15T7V5CA	500	6.4	7 13	7.5	7.88	10	11.3	132	14.5	690	6 1	8500
SM15T10	SM15T10C	10	8 55	9.5	10	11.0	1	14.5	103	18.6	538	7.3	7000
SM15T10A	SM15T10CA	10	8 55	9.5	10	10.5	1	14.5	103	18.6	538	7.3	7000
SM15T12	SM15T12C	5	10.2	11.4	12	13.2	1	16.7	90	21.7	461	7.8	6000
SM15T12A	SM15T12CA	5	10.2	11.4	12	12.6	1	16 7	90	21.7	461	7.8	6000
SM15T15	SM15T15C	5	12.8	14.3	15	16 5	1	21.2	71	27.2	368	8.4	5000
SM15T15A	SM15T15CA	5	12.8	14.3	15	15 8	1	21.2	71	27.2	368	8.4	5000
SM15T18	SM15T18C	5	15.3	17.1	18	19.8	1	25.2	59.5	32.5	308	8.8	4300
SM15T18A	SM15T18CA	5	15.3	17 1	18	18.9	1	25 2	59.5	32.5	308	8.8	4300
SM15T22	SM15T22C	5	18.8	20.9	22	24.2	1	30.6	49	39.3	254	9.2	3700
SM15T22A	SM15T22CA	5	18.8	20.9	22	23.1	1	30.6	49	39.3	254	9 2	3700
SM15T24	SM15T24C	5	20.5	22.8	24	26.4	1	33.2	45	42.8	234	9.4	3500
SM15T24A	SM15T24CA	5	20.5	22.8	24	25.2	1	33.2	45	42.8	234	9.4	3500
SM15T27	SM15T27C	5	23.1	25.7	27	29 7	1	37.5	40	48.3	207	9.6	3200
SM15T27A	SM15T27CA	5	23.1	25.7	27	28.4	1	37 5	40	48.3	207	9 6	3200
SM15T30	SM15T30C	5	25.6	28.5	30	33.0	1	41.5	36	53.5	187	9.7	2900
SM15T30A	SM15T30CA	5	25.6	28.5	30	31.5	1	41.5	36	53.5	187	9.7	2900
SM15T33	SM15T33C	5	28.2	31.4	33	36.3	1	45.7	33	59.0	169	9.8	2700
SM15T33A	SM15T33CA	5	28.2	31.4	33	34.7	1	45.7	33	59.0	169	9.8	2700
SM15T36	SM15T36C	5	30.8	34.2	36	39.6	1	49.9	30	64.3	156	9 9	2500
SM15T36A	SM15T36CA	5	30.8	34.2	36	37 8	1	49.9	30	64.3	156	9 9	2500
SM15T39	SM15T39C	5	33 3	37.1	39	42 9	1	53.9	28	69.7	143	10.0	2400
SM15T39	SM15T39	5	33.3	37.1	39	41.0	1	53.9	28	69.7	143	10.0	2400

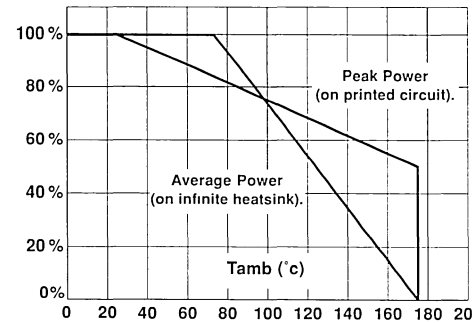
TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min	nom	max	note2	V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Uni directional	Bi directional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM15T68	SM15T68C	5	58.1	64.6	68	74.8	1	92	16.3	121	83	10 4	1550
SM15T68A	SM15T68CA	5	58.1	64.6	68	71.4	1	92	16.3	121	83	10.4	1550
SM15T100	SM15T100C	5	85.5	95.0	100	110	1	137	11	178	56	10.6	1150
SM15T100A	SM15T100CA	5	85 5	95.0	100	105	1	137	11	178	56	10.6	1150
SM15T150	SM15T150C	5	128	143	150	165	1	207	7.2	265	38	10.8	850
SM15T150A	SM15T150CA	5	128	143	150	158	1	207	7.2	265	38	10.8	850
SM15T200	SM15T200C	5	171	190	200	220	1	274	5.5	353	28	10.8	675
SM15T200A	SM15T200CA	5	171	190	200	210	1	274	5.5	353	28	10.8	675
SM15T220	SM15T220C	5	188	209	220	242	1	328	4.6	388	26	10.8	625
SM15T220A	SM15T220CA	5	188	209	220	231	1	328	4.6	388	26	10.8	625

All parameters tested at 25 °C, except where indicated.



Note 1 : - For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode
Note 2 : - Pulse test: $T_P < 50$ ms
Note 3 : - $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25\,C)}$
Note 4 : - VR = 0 V, F = 1 MHz For bidirectional types, capacitance value is divided by 2

Figure 1: Power dissipation derating versus ambient temperature



TYPES		TYPES		TYPES		TYPES	
Unidirectional	Marking	Bidirectional	Marking	Unidirectional	Marking	Bidirectional	Marking
SM15T6V8	MDD	SM15T6V8C	BDD	SM15T30	MEQ	SM15T30C	BEQ
SM15T6V8A	MDE	SM15T6V8CA	BDE	SM15T30A	MER	SM15T30CA	BER
SM15T7V5	MDF	SM15T7V5C	BDF	SM15T33	MES	SM15T33C	BES
SM15T7V5A	MDG	SM15T7V5CA	BDG	SM15T33A	MET	SM15T33CA	BET
SM15T10	MDN	SM15T10C	BDN	SM15T36	MEU	SM15T36C	BEU
SM15T10A	MDP	SM15T10CA	BDP	SM15T36A	MEV	SM15T36CA	BEV
SM15T12	MDS	SM15T12C	BDS	SM15T39	MEW	SM15T39C	BEW
SM15T12A	MDT	SM15T12CA	BDT	SM15T39A	MEX	SM15T39CA	BEX
SM15T15	MDW	SM15T15C	BDW	SM15T68	MFN	SM15T68C	BFN
SM15T15A	MDX	SM15T15CA	BDX	SM15T68A	MFP	SM15T68CA	BFP
SM15T18	MED	SM15T18C	BED	SM15T100	MFW	SM15T100C	BFW
SM15T18A	MEE	SM15T18CA	BEE	SM15T100A	MFX	SM15T100CA	BFX
SM15T22	MEH	SM15T22C	BEH	SM15T150	MGH	SM15T150C	BGH
SM15T22A	MEK	SM15T22CA	BEK	SM15T150A	MGK	SM15T150CA	BGK
SM15T24	MEL	SM15T24C	BEL	SM15T200	MGU	SM15T200C	BGU
SM15T24A	MEM	SM15T24CA	BEM	SM15T200A	MGV	SM15T200CA	BGV
SM15T27	MEN	SM15T27C	BEN	SM15T220	MGW	SM15T220C	BGW
SM15T27A	MEP	SM15T27CA	BEP	SM15T220A	MGVX	SM15T220CA	BGX

Figure 2 : Peak pulse power versus exponential pulse duration.

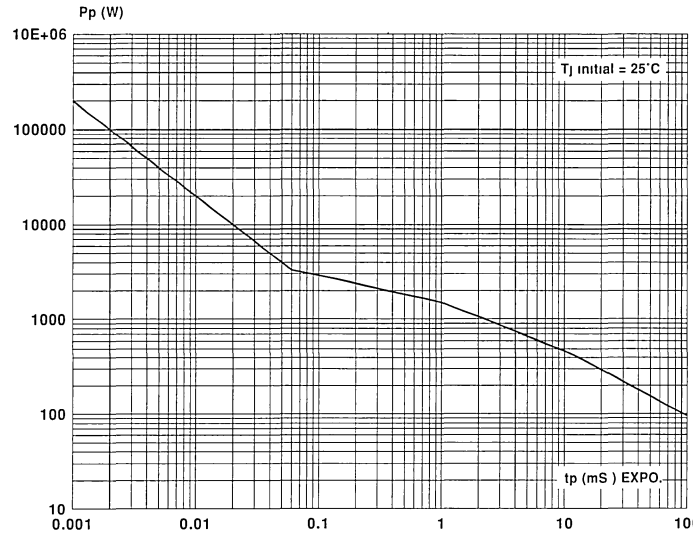
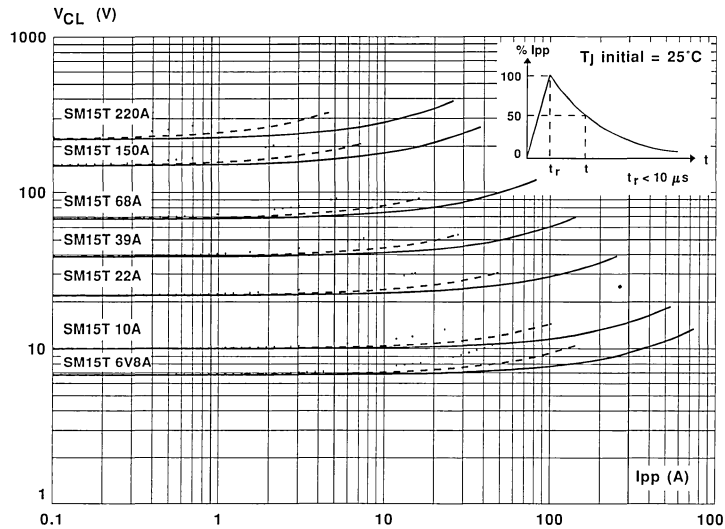


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} * [T_a - 25] * V_{(BR)}$.
For intermediate voltages, extrapolate the given results

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

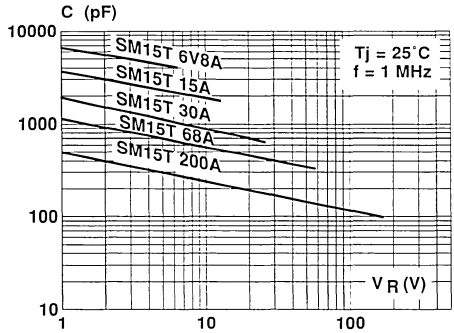


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

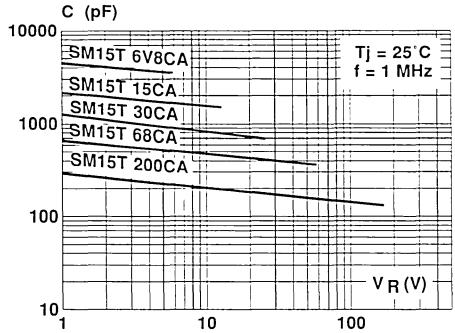


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

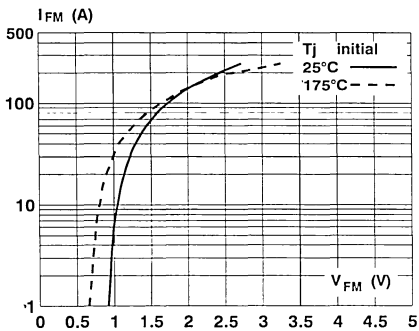
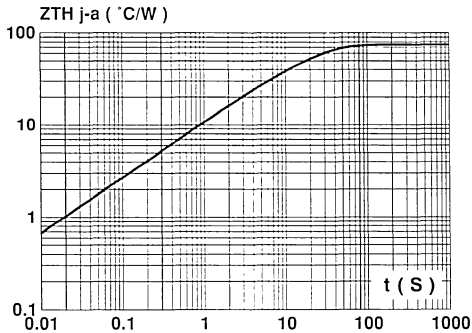
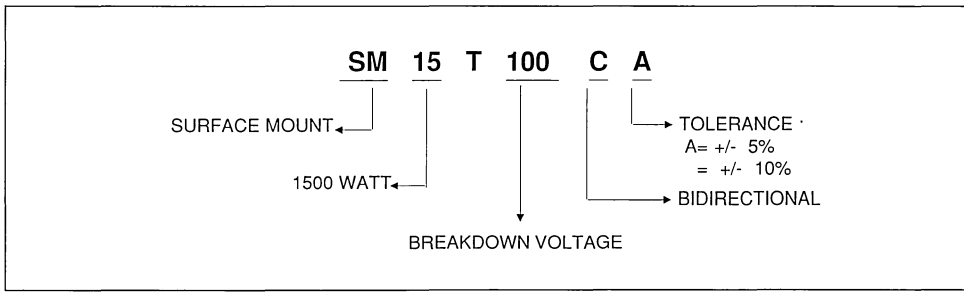


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with standard footprint dimensions.



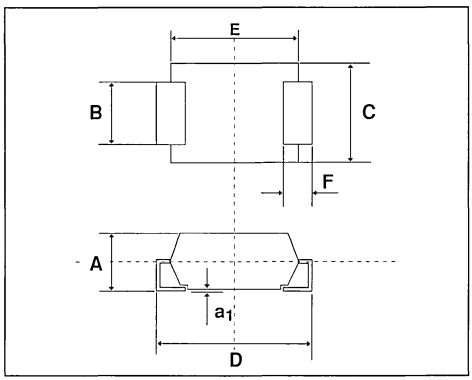
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

SOD 15 (Plastic).

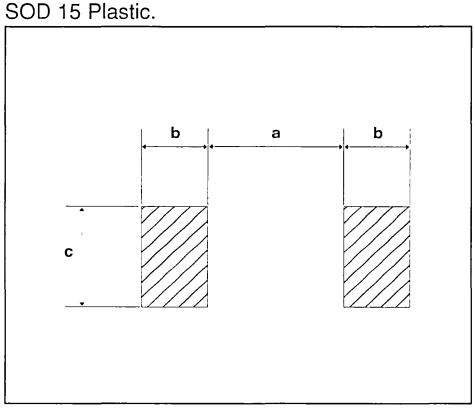


Ref	Millimeters		Inches	
	min	max	min	max
A	2.5	3.1	0.098	0.122
a1	-	0.2	-	0 008
B	2.9	3.1	0 114	0.122
C	4.8	5.2	0.190	0.200
D	7.6	8.0	0.300	0.315
E	6.3	6.6	0 248	0 259
F	1.3	1.7	0.051	0.067

Weight = 0.25 g.

FOOTPRINT DIMENSIONS (Millimeter).

SOD 15 Plastic.



Ref	Millimeters
a	4.2
b	2
c	3 3

Packaging : standard packaging is in film.

SGS-THOMSON MICROELECTRONICS

SMTPA SERIES

TRISIL

FEATURES

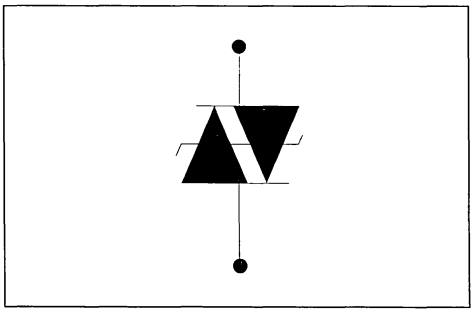
- BIDIRECTIONAL CROWBAR PROTECTION.
- BREAKDOWN VOLTAGE RANGE: From 62 V To 270 V.
- HOLDING CURRENT = 150 mA min
- PEAK PULSE CURRENT : I_{PP} = 50 A, 10/1000 µs.

SOD 6
(Plastic)

DESCRIPTION

The SMTPAxx series has been designed to protect telecommunication equipments against lightning and transient induced by AC power lines.

SCHEMATIC DIAGRAM



IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ T_{amb} ≤ + 85°C)

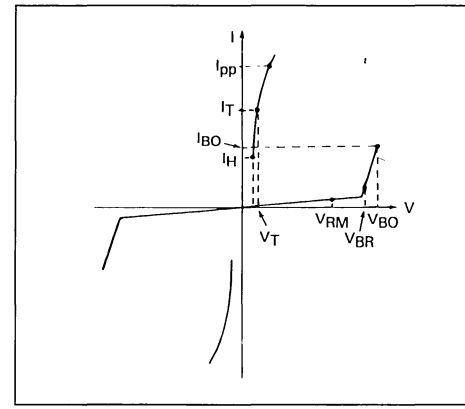
Symbol	Parameter		Value	Unit
P	Power dissipation on infinite heatsink	T_{lead} = 50 °C	5	W
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs	50 100	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	30	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction to leads. on infinite heatsink.	20	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit with standard footprint dimensions.	100	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current

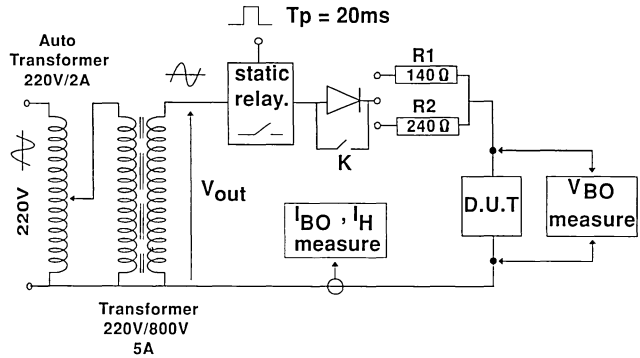


Type	Marking	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} @ I_{BO} max note1		I_H min note1	V_T max note2	C max note3
	Laser	µA	V	V	mA	V	mA	mA	V	pF
SMTPA62	U01	2	56	62	1	82	800	150	2	150
SMTPA68	U05	2	61	68	1	90	800	150	2	150
SMTPA100	U13	2	90	100	1	133	800	150	2	100
SMTPA120	U17	2	108	120	1	160	800	150	2	100
SMTPA130	U19	2	117	130	1	173	800	150	2	100
SMTPA180	U25	2	162	180	1	240	800	150	2	100
SMTPA200	U27	2	180	200	1	267	800	150	2	100
SMTPA220	U31	2	198	220	1	293	800	150	2	100
SMTPA240	U35	2	216	240	1	320	800	150	2	100
SMTPA270	U39	2	243	270	1	360	800	150	2	100

All parameters tested at 25°C, except where indicated

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 2 : Square pulse Tp = 1 ms - I_T = 3A.
Note 3 : V_R = 1V, F = 1MHz.

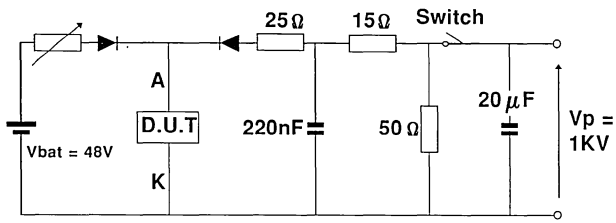
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 μsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 μs.
3) The D.U.T will come back to the OFF-State withing a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on state current versus number of cycles. (with sinusoidal pulse: F= 50 Hz).

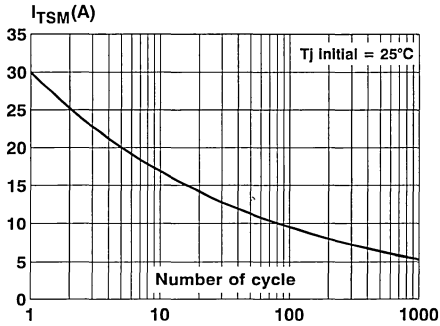


Figure 2 : On state characteristics (typical values).

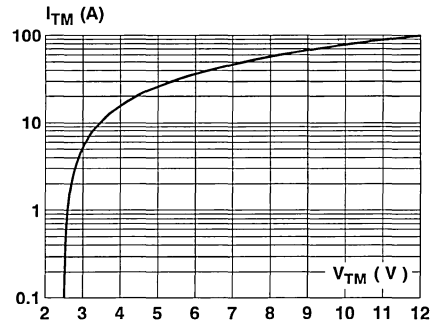
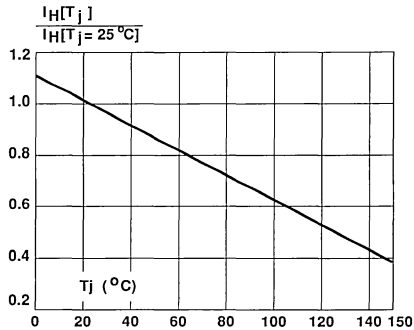
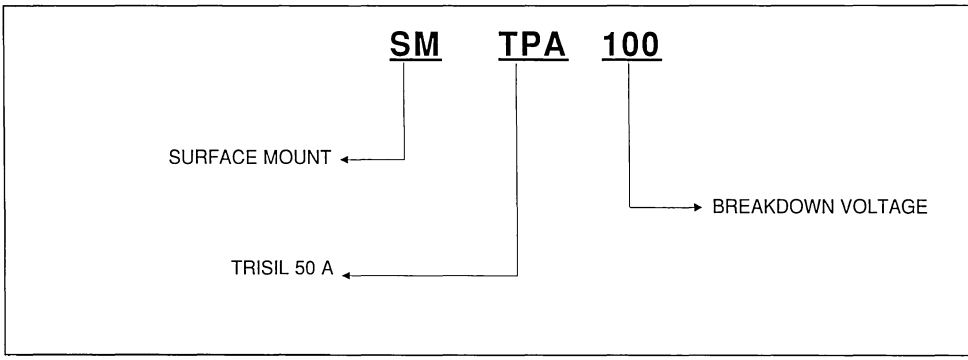


Figure 3 : Relative variation of holding current versus junction temperature.



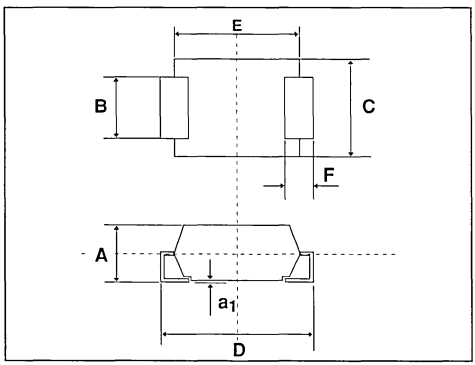
ORDER CODE



MARKING : Logo, date code, type code.

PACKAGE MECHANICAL DATA.

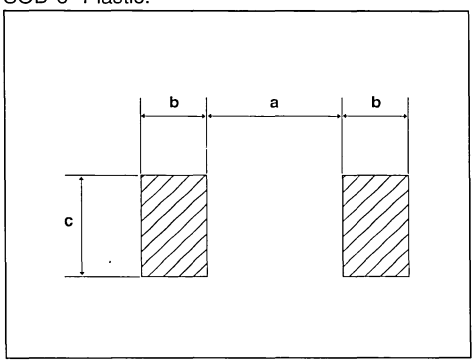
SOD 6 Plastic.



Ref	Millimeters		Inches	
	min	max	min	max
A	2.48	2.61	0.096	0.103
a_1	0.10	0.20	0.004	0.008
B	1.96	2.11	0.077	0.083
C	3.65	3.93	0.143	0.155
D	5.39	5.59	0.212	0.220
E	4.15	4.30	0.163	0.170
F	1.00	1.27	0.039	0.050

FOOTPRINT DIMENSIONS (Millimeters)

SOD 6 Plastic.



Ref	Millimeters
a	2.75
b	1.52
c	2.30

Packaging : Standard packaging is in film.

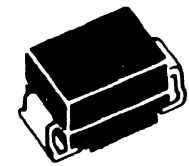
SGS-THOMSON MICROELECTRONICS

SMTPB SERIES

TRISIL

FEATURES

- BIDIRECTIONAL CROWBAR PROTECTION.
- BREAKDOWN VOLTAGE RANGE:
  From 62 V To 270 V.
- HOLDING CURRENT = 150 mA min
- PEAK PULSE CURRENT :
  I_{PP} = 90 A, 10/1000 µs.

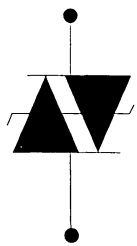


SOD 15
(Plastic)

DESCRIPTION

The SMTPBxx series has been designed to protect telecommunication equipment against lightning and transient induced by AC power lines.

SCHEMATIC DIAGRAM



IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ T_{amb} ≤ + 85°C)

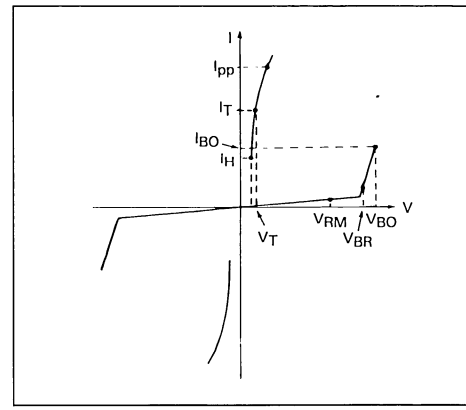
Symbol	Parameter		Value	Unit
P	Power dissipation on infinite heatsink	T_{lead} = 50 °C	10	W
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs	90 150	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	50	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		+ 260	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction to leads. On infinite heatsink.	10	°C/W
R_{th} (j-a)	Junction to ambient. On printed circuit with standard footprint dimensions.	75	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current

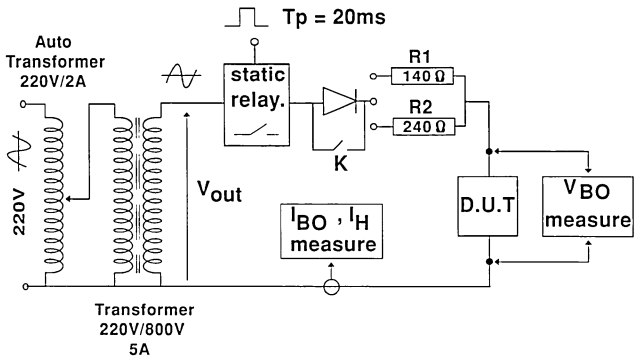


Type	Marcking	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} @ I_{BO} max note1	max	I_H min note1	V_T max note2	C max note3
	Laser	µA	V	V	mA	V	mA	mA	V	pF
SMTPB62	W07	2	56	62	1	82	800	150	3.5	350
SMTPB68	W11	2	61	68	1	90	800	150	3.5	350
SMTPB100	W17	2	90	100	1	133	800	150	3.5	200
SMTPB120	W21	2	108	120	1	160	800	150	3.5	200
SMTPB130	W23	2	117	130	1	173	800	150	3.5	200
SMTPB180	W29	2	162	180	1	240	800	150	3.5	200
SMTPB200	W31	2	180	200	1	267	800	150	3.5	200
SMTPB220	W35	2	198	220	1	293	800	150	3.5	200
SMTPB240	W39	2	216	240	1	320	800	150	3.5	200
SMTPB270	W43	2	243	270	1	360	800	150	3.5	200

All parameters tested at 25°C, except where indicated.

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 2 : Square pulse Tp = 1 ms - I_T = 5A.
Note 3 : V_R = 1V, F = 1MHz.

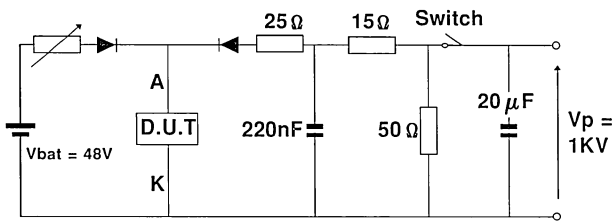
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State withing a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on state current versus number of cycles. (with sinusoïdal pluse: F= 50 Hz).

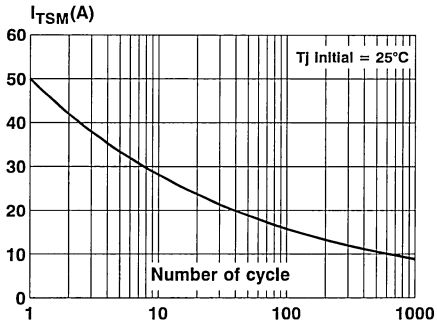


Figure 2 : On - state characteristics (typical values).

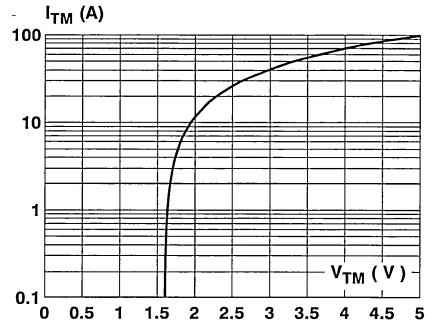
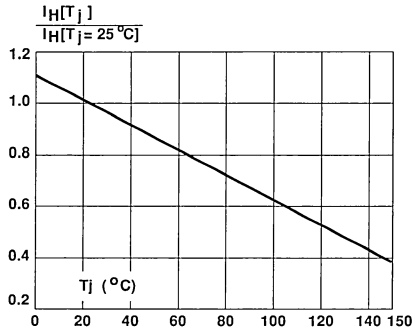
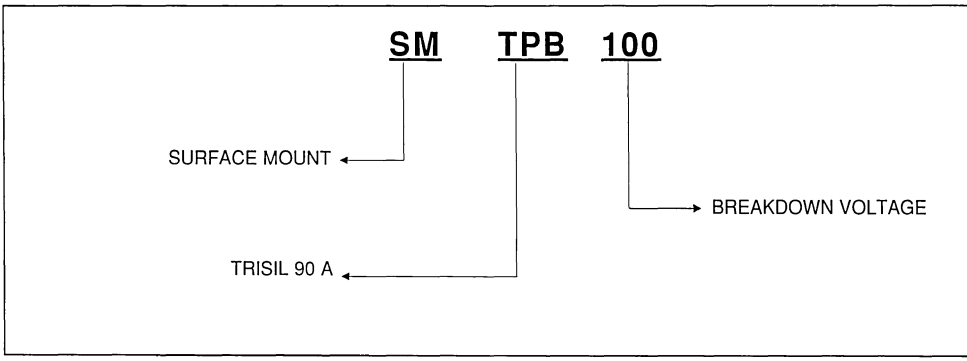


Figure 3 : Relative variation of holding current versus junction temperature.



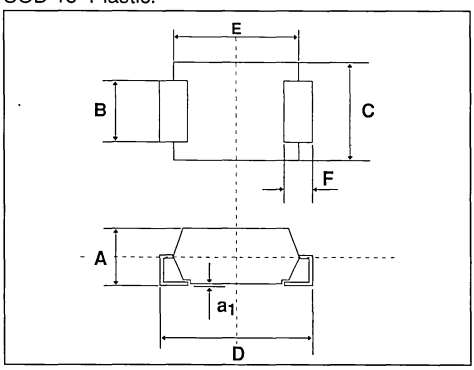
ORDER CODE



MARKING : Logo, date code, type code.

PACKAGE MECHANICAL DATA.

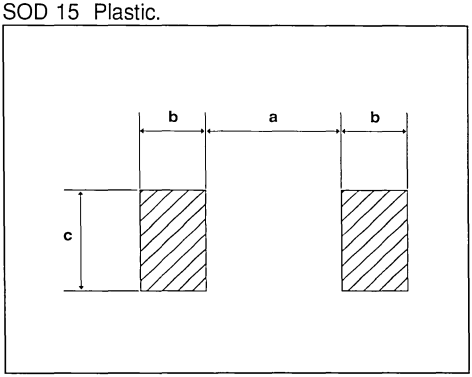
SOD 15 Plastic.



Ref	Millimeters		Inches	
	min	max	min	max
A	2.5	3.1	0.098	0.122
a_1	-	0.2	-	0.008
B	2.9	3.1	0.114	0.122
C	4.8	5.2	0.190	0.200
D	7.6	8.0	0.300	0.315
E	6.3	6.6	0.248	0.259
F	1.3	1.7	0.051	0.067

FOOTPRINT DIMENSIONS.

SOD 15 Plastic.



Ref	Millimeters
a	4.2
b	2
c	3.3

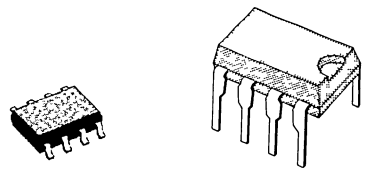
Packaging : Standard packaging is in film.

THBT150
THBT200 / THBT270

TRISIL

FEATURES

- BIDIRECTIONAL TRIPLE PROTECTION
- CROWBAR PROTECTION
- PEAK PULSE CURRENT :
  I_{PP} = 30 A , 10/1000 µs
- HOLDING CURRENT = 150 mA min
- AVAILABLE IN DIP 8 AND SO 8 PACKAGES



SO 8
(Plastic)

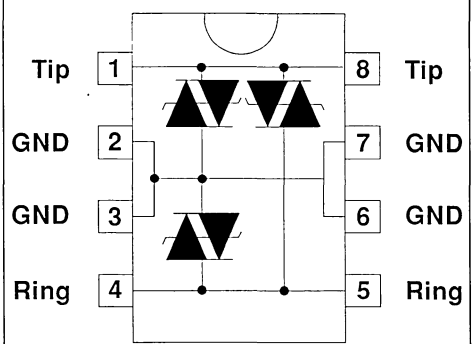
DIL 8
(Plastic)

DESCRIPTION

Dedicated to telecommunication equipment protection, these devices provide a triple bidirectional protection function.
They ensure the same protection capability with the same breakdown voltage both in common mode and in differential mode.

Particular attention has been given to the internal wire bonding . A 4-point configuration ensures reliable protection, eliminating the overvoltage introduced by the parasitic inductances of the wiring (Ldi/dt) especially for very fast transients.

SCHEMATIC DIAGRAM

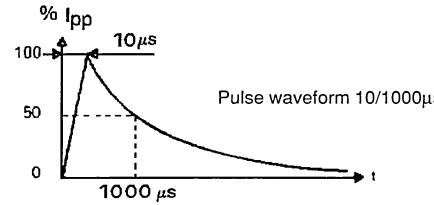


IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ T_{amb} ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 5/320 µs 2/10 µs	30 40 75	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 10 ms tp = 1 s	5 3.5	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C



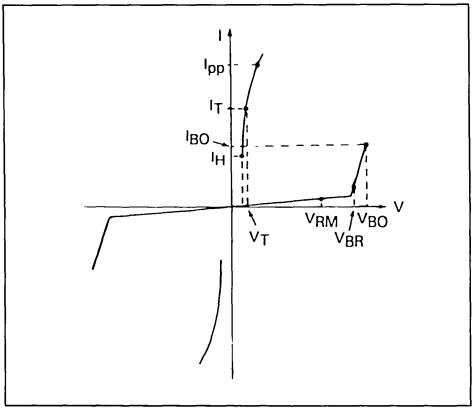
Pulse waveform 10/1000µs

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
R_{th} (j-a)	Junction-to-ambient	DIL 8 SO 8	125 171	°C/W °C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current



STATIC PARAMETERS

Types	I_R @ V_{RM} max		VBR @ I_R min		V_{BO} @ I_{BO} max	min note1	max	IH min note1	VT max note2	C max note3
	µA	V	V	mA	V	mA	mA	mA	V	pF
THBT150	5	135	150	1	210	50	400	150	8	200
THBT200	5	180	200	1	290	50	400	150	8	200
THBT270	5	240	270	1	380	50	400	150	8	200

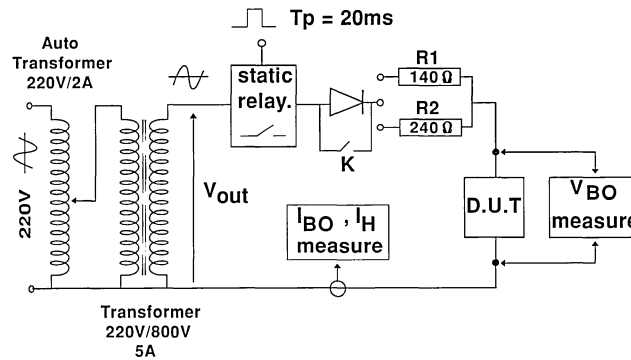
DYNAMIC PARAMETERS

Types	V_{BO} dyn Typical Value note 4
	(V)
THBT150	290
THBT200	380
THBT270	420

All parameters tested at 25°C, except where indicated

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters
Note 2 : Square pulse Tp = 500 µs - I_T = 5A
Note 3 : V_R = 1V, F = 1MHz
Note 4 : The dynamic breakover voltage is meassured with following surge test : CCITT - 1 5 KV 10/700 µs

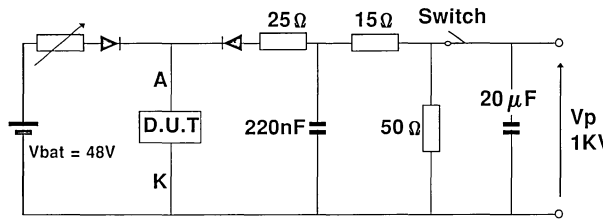
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST



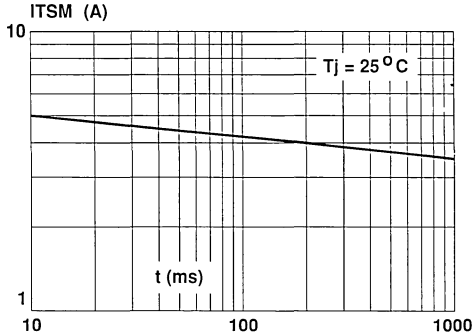
Surge Generator
10/700 μsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

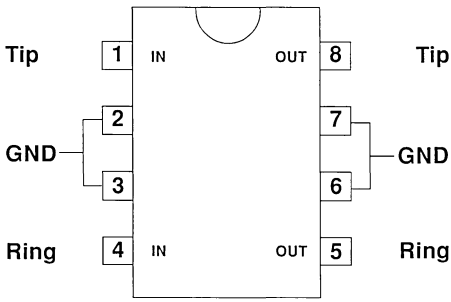
TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 μs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on-state current. (with sinusoidal pulse : F =50Hz)



APPLICATION NOTE



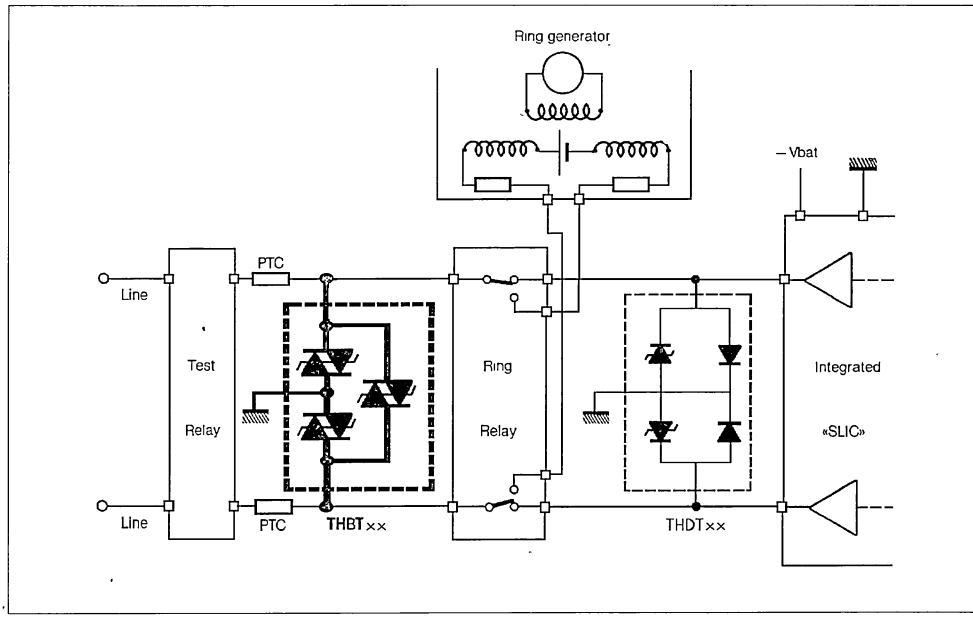
4- points structure lay-out.

1) Connect pins 2, 3, 6 and 7 to ground in order to guarantee a good surge current capability for long duration disturbances.

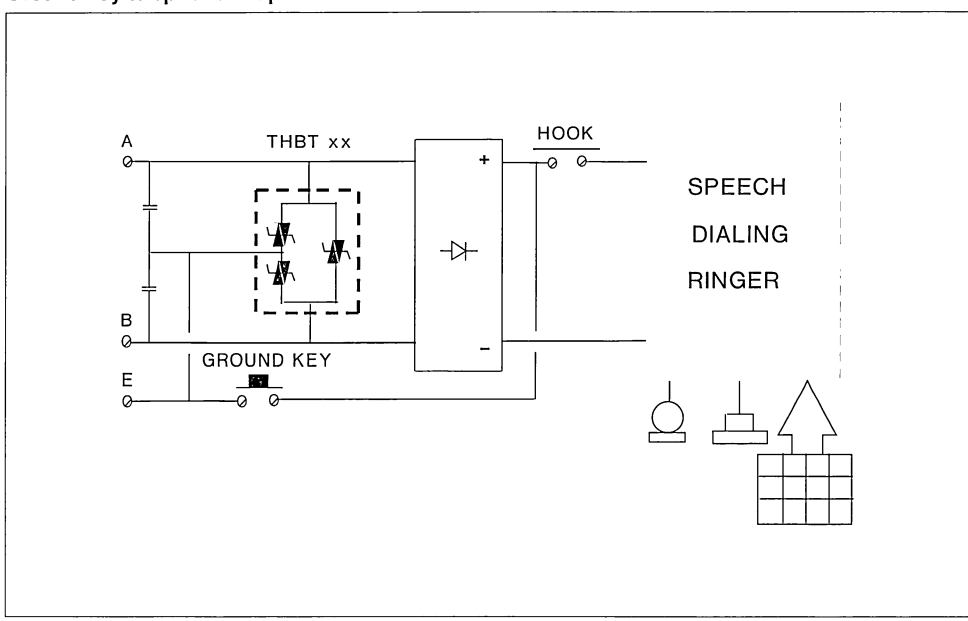
2) In order to take advantage of the "4-points structure" of the THBTxxx, the tip and Ring lines have to cross through the device. In this case, the device will eliminate the overvoltages generated by the parasitic inductances of the wiring (Ldi/dt), especially for very fast Transients.

APPLICATION CIRCUIT

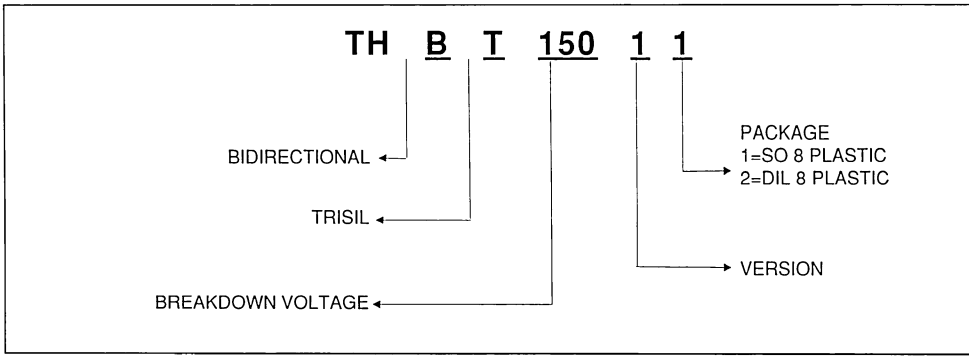
Line card protection



Ground key telephone set protection



ORDER CODE



MARKING

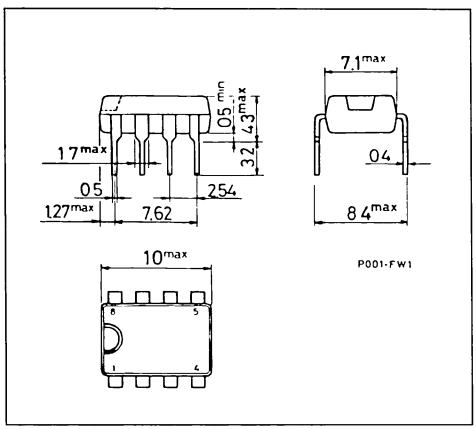
Package	Type	Marking
SO8	THBT15011	BT1511
	THBT20011	BT2011
	THBT27011	BT2711

Package	Type	Marking
DIL8	THBT15012	BT1512
	THBT20012	BT2012
	THBT27012	BT2712

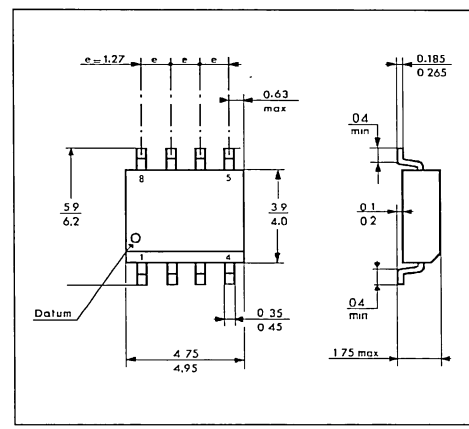
Packaging : Products supplied in antistatic tubes.

PACKAGE MECHANICAL DATA (in millimeters)

DIL 8 Plastic

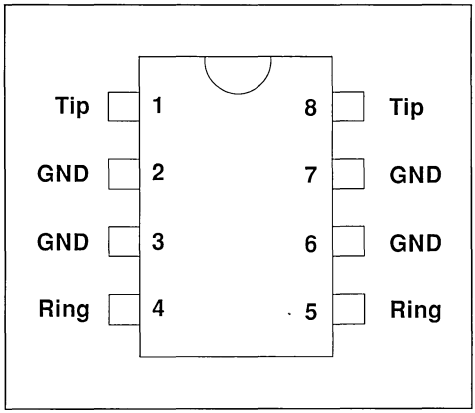


SO 8 Plastic

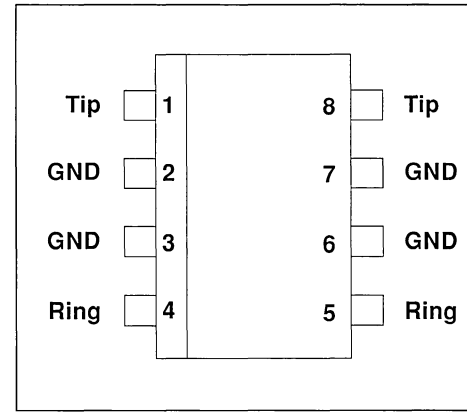


CONNECTION DIAGRAM

DIL 8 Plastic



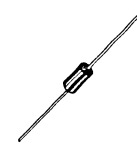
SO 8 Plastic



TRISIL

FEATURES

- BIDIRECTIONAL CROWBAR PROTECTION.
- BREAKDOWN VOLTAGE RANGE:
  From 62 V To 270 V.
- HOLDING CURRENT = I_H
  Suffix 12 = 120mA min.
  Suffix 18 = 180mA min.
- PEAK PULSE CURRENT :
  I_{PP} = 50 A, 10/1000 µs.



F 126
(Plastic)

DESCRIPTION

The TPAxx series has been designed to protect telecommunication equipments against lightning and transient induced by AC power lines.

SCHEMATIC DIAGRAM

IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

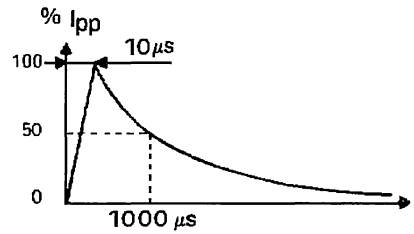
ABSOLUTE RATINGS (limiting values) ($-40°C \leq T_{amb} \leq +85°C$)

Symbol	Parameter		Value	Unit
P	Power dissipation on infinite heatsink	T_{amb} = 50 °C	1.7	W
I_{PP}	Peak pulse current See note1	10/1000 µs 8/20 µs	50 100	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	30	A
dI/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

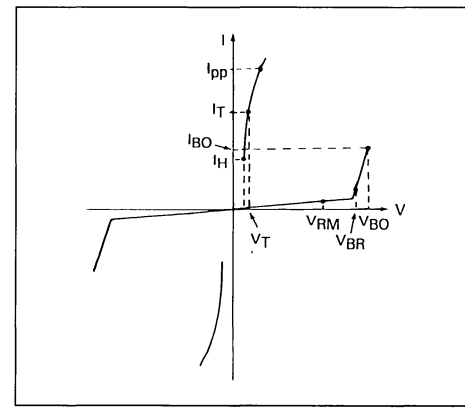
Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction to leads on infinite heatsink.	60	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. Llead = 10 mm	100	°C/W

Note 1: 10/1000 µs wave form



ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current



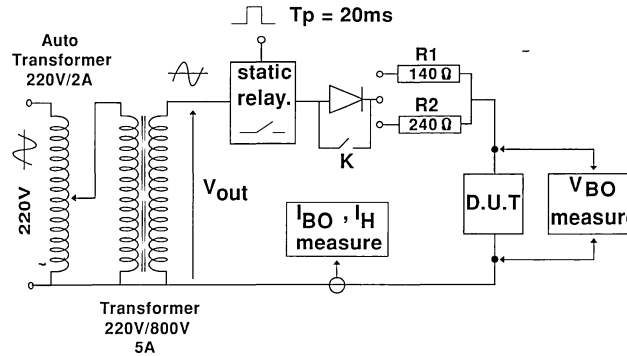
ELECTRICAL CHARACTERISTICS

Type	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} @ I_{BO} max note2	max	V_T max note3	C max note4	I_H min note2
	µA	V	V	mA	V	mA	V	pF	mA
P TPA62A - 12 or 18	2	56	62	1	82	300	2	150	
TPA62B - 12 or 18	2	56	62	1	75	300	2	150	
P TPA68A - 12 or 18	2	61	68	1	90	300	2	150	
TPA68B - 12 or 18	2	61	68	1	82	300	2	150	
(1) TPA75A - 12 or 18	2	67	75	1	100	300	2	150	
(1) TPA75B - 12 or 18	2	67	75	1	91	300	2	150	
(1) TPA82A - 12 or 18	2	74	82	1	109	300	2	150	
(1) TPA82B - 12 or 18	2	74	82	1	99	300	2	150	Suffix 12
(1) TPA91A - 12 or 18	2	82	91	1	121	300	2	150	for 120 mA.
(1) TPA91B - 12 or 18	2	82	91	1	110	300	2	150	
P TPA100A - 12 or 18	2	90	100	1	133	300	2	100	
TPA100B - 12 or 18	2	90	100	1	121	300	2	100	
P TPA110A - 12 or 18	2	99	110	1	147	300	2	100	
TPA110B - 12 or 18	2	99	110	1	133	300	2	100	
P TPA120A - 12 or 18	2	108	120	1	160	300	2	100	Suffix 18
TPA120B - 12 or 18	2	108	120	1	145	300	2	100	for 180 mA.
P TPA130A - 12 or 18	2	117	130	1	173	300	2	100	
TPA130B - 12 or 18	2	117	130	1	157	300	2	100	
(1) TPA150A - 12 or 18	2	135	150	1	200	300	4	75	
(1) TPA150B - 12 or 18	2	135	150	1	181	300	4	75	
(1) TPA160A - 12 or 18	2	144	160	1	213	300	4	75	
(1) TPA160B - 12 or 18	2	144	160	1	193	300	4	75	
P TPA180A - 12 or 18	2	162	180	1	240	300	4	75	
TPA180B - 12 or 18	2	162	180	1	217	300	4	75	
P TPA200A - 12 or 18	2	180	200	1	267	300	4	75	
TPA200B - 12 or 18	2	180	200	1	241	300	4	75	
P TPA220A - 12 or 18	2	198	220	1	293	300	4	75	
TPA220B - 12 or 18	2	198	220	1	265	300	4	75	
P TPA240A - 12 or 18	2	216	240	1	320	300	4	75	
TPA240B - 12 or 18	2	216	240	1	289	300	4	75	
P TPA270A - 12 or 18	2	243	270	1	360	300	4	75	
TPA270B - 12 or 18	2	243	270	1	325	300	4	75	

All parameters tested at 25°C, except where indicated

P : Preferred device.
(1): These voltages are on request
Note 2 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 3 : Square pulse Tp = 1 ms - I_T = 3A
Note 4 : V_R = 1V, F = 1MHz

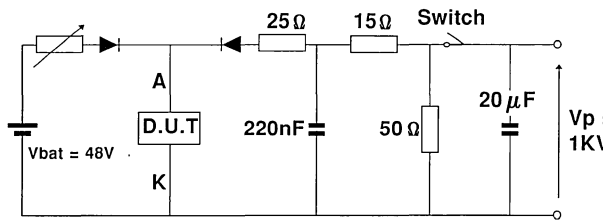
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State withing a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on state current versus number of cycles. (with sinusoidal

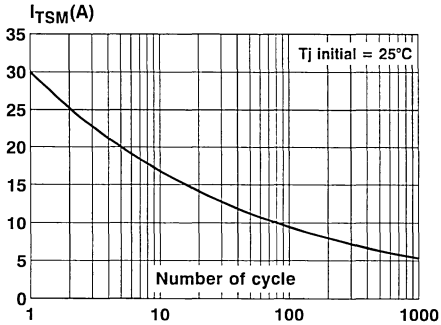
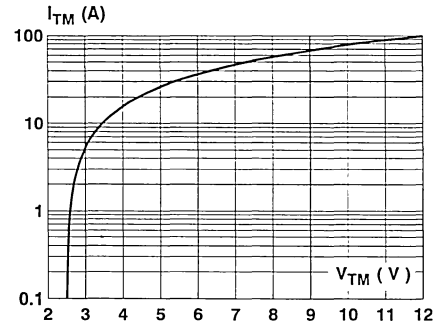
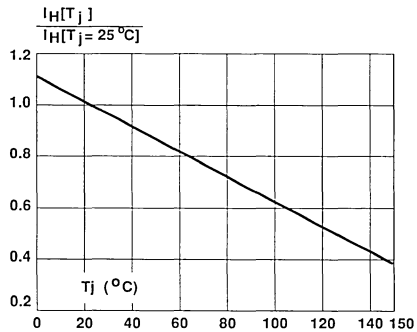


Figure 2 : On - state characteristics (typical values).

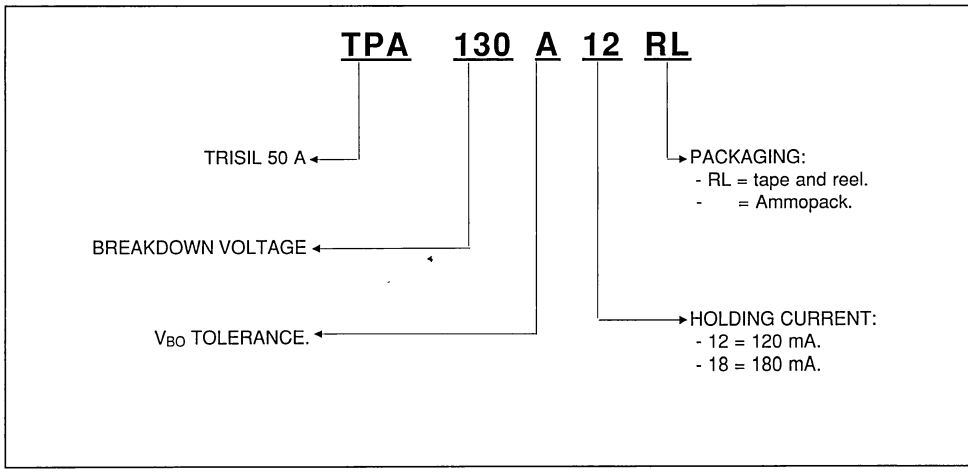


Note : For device with V_{BR} > 150 Volt
The V_T value is twice that shown

Figure 3 : Relative variation of holding current versus junction temperature.



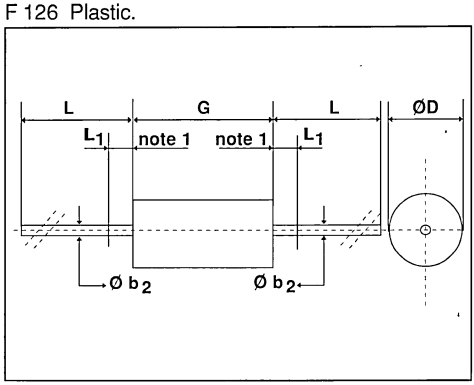
ORDER CODE



MARKING : Logo, Date Code, Part Number.

PACKAGE MECHANICAL DATA.

F 126 Plastic.



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	0.76	0.86	0.03	0.034
Ø D	-	3.05	-	0.12
G	-	6.35	-	0.25
L	26	-	1.02	-
L_1	-	1.27	-	0.05

note 1:The diameter Ø b_2 is not controlled over zone L_1.

Packaging : Standard packaging is in tape and reel.

SGS-THOMSON MICROELECTRONICS

TPB SERIES

TRISIL

FEATURES

- BIDIRECTIONAL CROWBAR PROTECTION.
- BREAKDOWN VOLTAGE RANGE:
  From 62 V To 270 V.
- HOLDING CURRENT = I_H
  Suffix 12 = 120mA min.
  Suffix 18 = 180mA min.
- PEAK PULSE CURRENT :
  I_{PP} = 90 A, 10/1000 µs.

CB 429
(Plastic)

DESCRIPTION

The TPBxx series has been designed to protect telecommunication equipments against lightning and transient induced by AC power lines.

SCHEMATIC DIAGRAM

IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

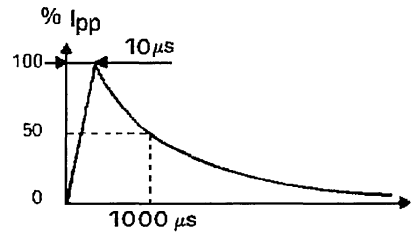
ABSOLUTE RATINGS (limiting values) ($-40°C \leq T_{amb} \leq +85°C$)

Symbol	Parameter		Value	Unit
P	Power dissipation on infinite heatsink	T_{amb} = 50 °C	5	W
I_{PP}	Peak pulse current See note1	10/1000 µs 8/20 µs	90 150	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	50	A
dI/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_J	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

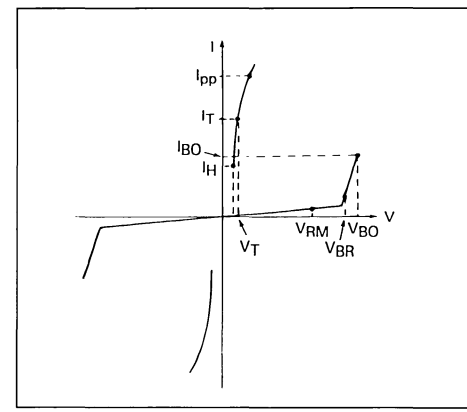
Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction to leads. On infinite heatsink.	20	°C/W
R_{th} (j-a)	Junction to ambient. On printed circuit. L_{lead} = 10 mm	75	°C/W

Note 1: 10/1000 µs wave form.



ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current



ELECTRICAL CHARACTERISTICS

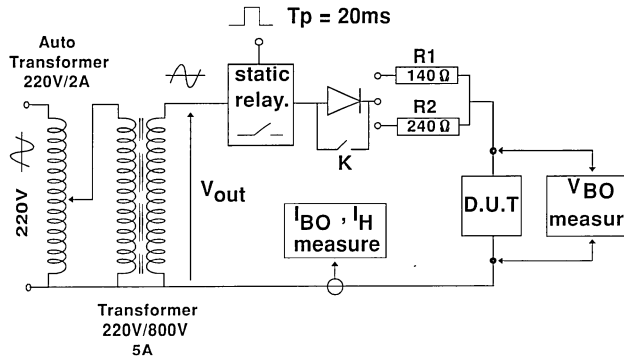
Type	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} @ I_{BO} max note2	max	V_T max note3	C max note4	I_H min note2
	µA	V	V	mA	V	mA	V	pF	mA
P TPB62A - 12 or 18	2	56	62	1	82	300	3.5	300	
TPB62B - 12 or 18	2	56	62	1	75	300	3.5	300	
P TPB68A - 12 or 18	2	61	68	1	90	300	3.5	300	
TPB68B - 12 or 18	2	61	68	1	82	300	3.5	300	
(1) TPB75A - 12 or 18	2	67	75	1	100	300	3.5	300	
(1) TPB75B - 12 or 18	2	67	75	1	91	300	3.5	300	
(1) TPB82A - 12 or 18	2	74	82	1	109	300	3.5	300	
(1) TPB82B - 12 or 18	2	74	82	1	99	300	3.5	300	Suffix 12
(1) TPB91A - 12 or 18	2	82	91	1	121	300	3.5	300	for 120 mA.
(1) TPB91B - 12 or 18	2	82	91	1	110	300	3.5	300	
P TPB100A - 12 or 18	2	90	100	1	133	300	3.5	200	
TPB100B - 12 or 18	2	90	100	1	121	300	3.5	200	
P TPB110A - 12 or 18	2	99	110	1	147	300	3.5	200	
TPB110B - 12 or 18	2	99	110	1	133	300	3.5	200	
P TPB120A - 12 or 18	2	108	120	1	160	300	3.5	200	Suffix 18
TPB120B - 12 or 18	2	108	120	1	145	300	3.5	200	for 180 mA.
P TPB130A - 12 or 18	2	117	130	1	173	300	3.5	200	
TPB130B - 12 or 18	2	117	130	1	157	300	3.5	200	
(1) TPB150A - 12 or 18	2	135	150	1	200	300	7	150	
(1) TPB150B - 12 or 18	2	135	150	1	181	300	7	150	
(1) TPB160A - 12 or 18	2	144	160	1	213	300	7	150	
(1) TPB160B - 12 or 18	2	144	160	1	193	300	7	150	
P TPB180A - 12 or 18	2	162	180	1	240	300	7	150	
TPB180B - 12 or 18	2	162	180	1	217	300	7	150	
P TPB200A - 12 or 18	2	180	200	1	267	300	7	150	
TPB200B - 12 or 18	2	180	200	1	241	300	7	150	
P TPB220A - 12 or 18	2	198	220	1	293	300	7	150	
TPB220B - 12 or 18	2	198	220	1	265	300	7	150	
P TPB240A - 12 or 18	2	216	240	1	320	300	7	150	
TPB240B - 12 or 18	2	216	240	1	289	300	7	150	
P TPB270A - 12 or 18	2	243	270	1	360	300	7	150	
TPB270B - 12 or 18	2	243	270	1	325	300	7	150	

All parameters tested at 25°C, except where indicated

P : Preferred device
(1): These voltages are on request

Note 2 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters
Note 3 : Square pulse Tp = 1 ms - I_T = 5A
Note 4 : V_R = 1V, F = 1MHz

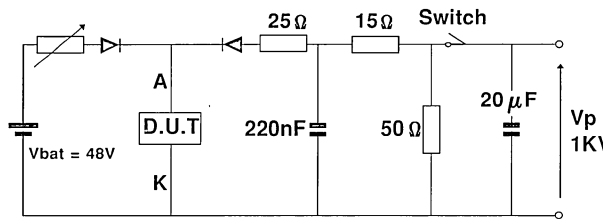
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State withing a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on state current versus number of cycles. (with sinusoïdal

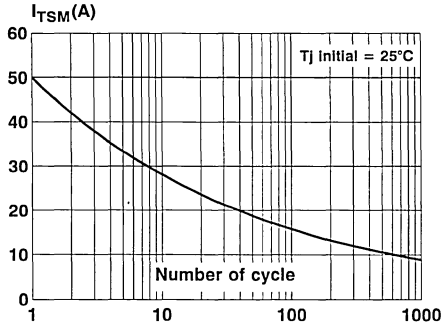
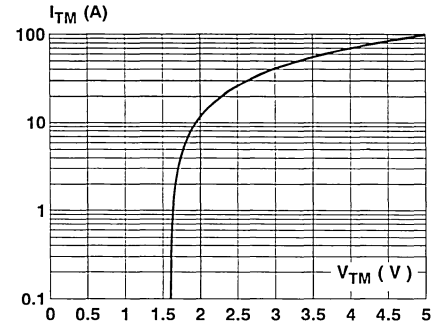
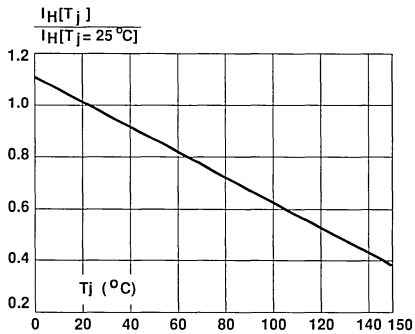


Figure 2 : On - state characteristics (typical values).

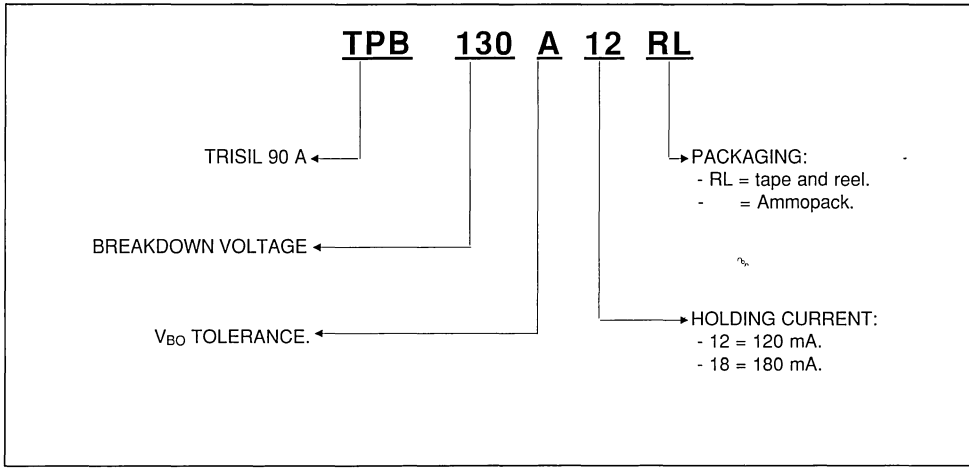


Note : For devices with V_{BR} > 150 V
The V_T value is twice that shown

Figure 3 : Relative variation of holding current versus junction temperature.



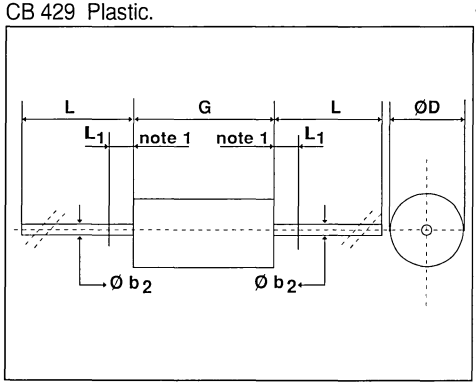
ORDER CODE



MARKING : Logo, Date Code, Part Number.

PACKAGE MECHANICAL DATA.

CB 429 Plastic.



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	-	1.06	-	0.042
Ø D	-	5.1	-	0.20
G	-	9.8	-	0.386
L	26	-	1.024	-
L_1	-	1.27	-	0.050

note 1:The diameter Ø b_2 is not controlled over zone L_1.

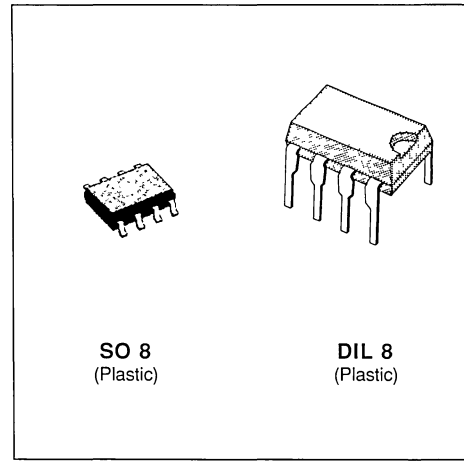
Packaging : Standard packaging is in tape and reel.

TPI80xxP/TPI120xxP

TRIBALANCED PROTECTION FOR ISDN INTERFACES

FEATURES

- BIDIRECTIONAL TRIPOLE PROTECTION.
- CROWBAR PROTECTION.
- PEAK PULSE CURRENT :
  I_{PP} = 30 A , 10/1000 µs.
- BREAKDOWN VOLTAGE:
  TPI80 = 80V
  TPI120 = 120V.
- AVAILABLE IN DIL8 AND SO8 PACKAGES.



SO 8
(Plastic)

DIL 8
(Plastic)

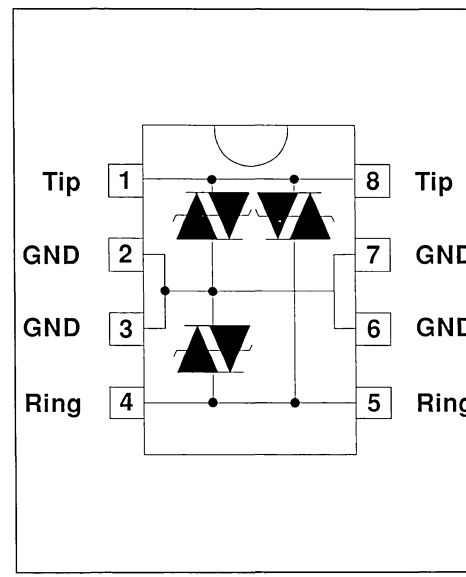
DESCRIPTION: TRIBALANCED PROTECTION

Dedicated devices for ISDN interface and high speed data telecom lines protection.

It's a tripole TRISIL with low capacitance providing:

- Low capacitances from lines to ground : allowing high speed transmission without signal attenuation.
- Good capacitance balance (Line A/Line B) in order to insure the longitudinal balance of the line.
- Fixed breakdown voltage in both common and differential modes.
- The same surge current capability in both common and differential modes.

SCHEMATIC DIAGRAM

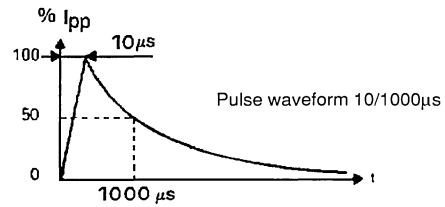


IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ T_{amb} ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 5/320 µs 2/10 µs	30 40 90	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 10 ms tp = 1 s	5 3.5	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C

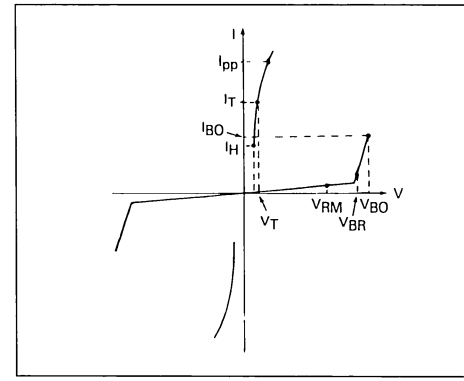


THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
R_{th} (j-a)	Junction-to-ambient	DIL 8 SO 8	125 171	°C/W °C/W

ELECTRICAL CHARACTERISTICS

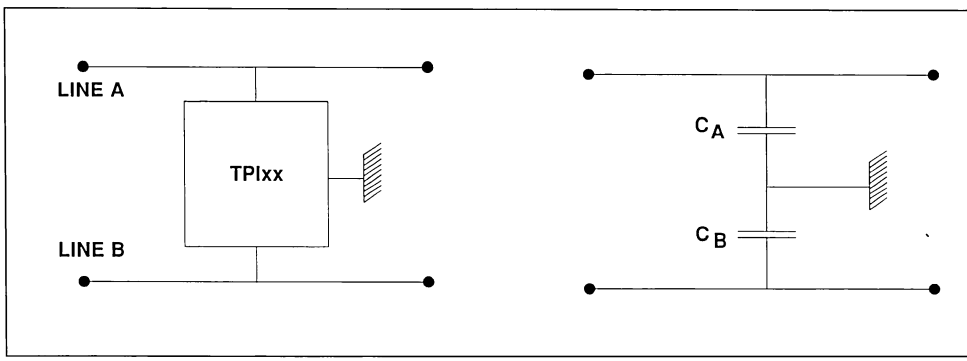
Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current



Types	I_R @ V_{RM} max		VBR @ I_R min		V_{BO} max note1	IBO max note1	IH min note1	VT max note2
	µA	V	V	mA	V	mA	mA	V
TPI80xxP	10	70	80	1	120	800	150	8
TPI120xxP	10	105	120	1	180	800	150	8

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters
Note 2 : Square pulse Tp = 500 µs - I_T = 5A

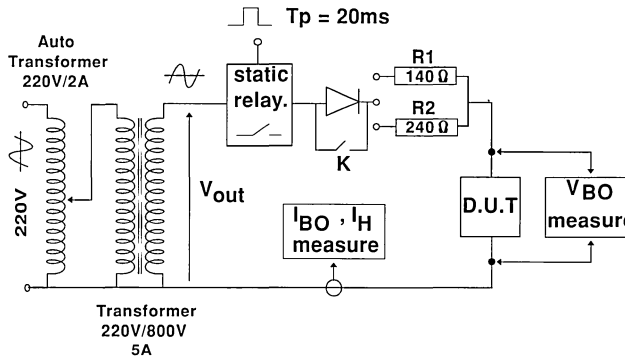
CAPACITANCES CHARACTERISTICS



CONFIGURATION	C_A (pf) max	C_B (pf) max	C_A - C_B (pf) max
V_A =1V V_B =56V	70	50	30
V_A = 56V V_B= 1V	50	70	30

All parameters tested at 25°C, except where indicated

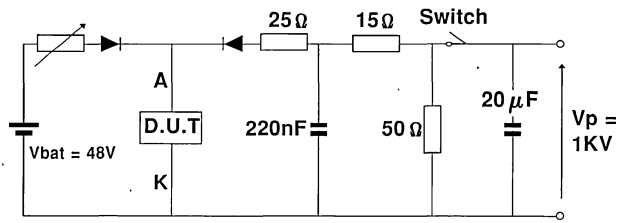
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



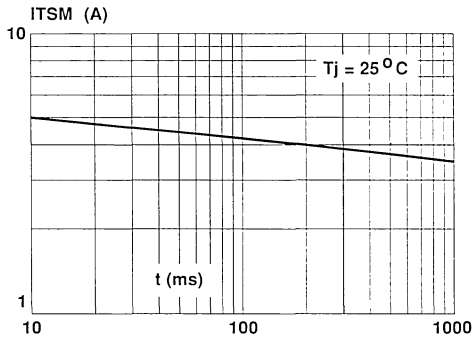
Surge Generator
10/700 μsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

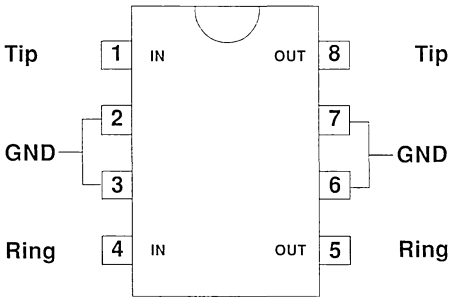
TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on-state current. (with sinusoidal pulse : F =50Hz)



APPLICATION NOTE.



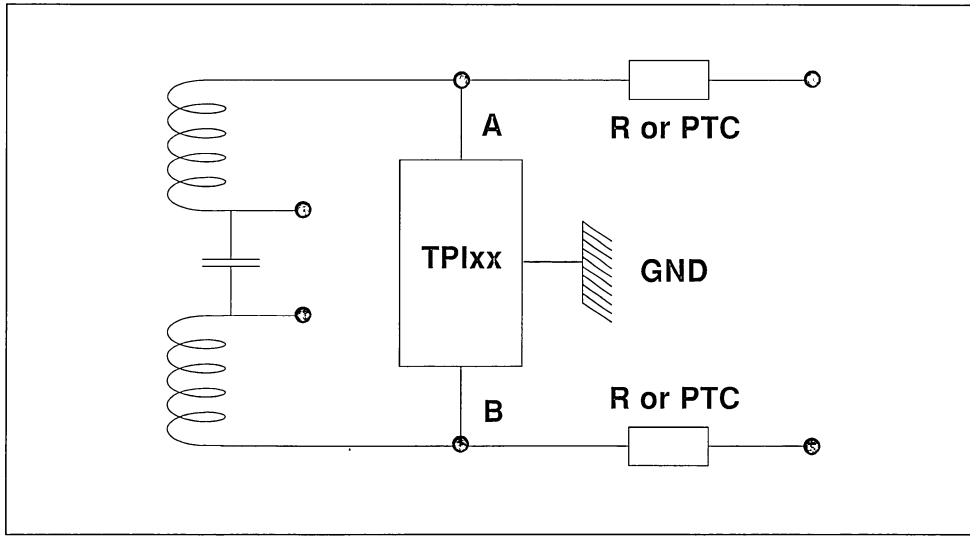
4- points structure lay-out

1) Connect pins 2, 3, 6 and 7 to ground in order to guarantee a good surge current capability for long duration disturbances.

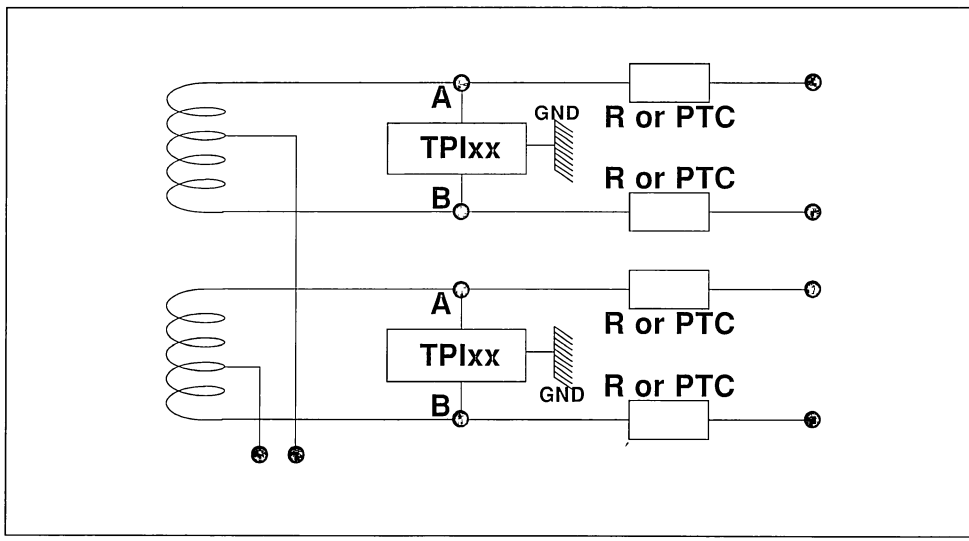
2) In order to take advantage of the "4-points structure" of the TPIxxxP, the tip and Ring lines have to cross through the device. in this case, the device will eliminate the overvoltages generated by the parasitic inductances of the wiring (Ldi/dt), especially for very fast Transients.

APPLICATION NOTE

U Interface Protection

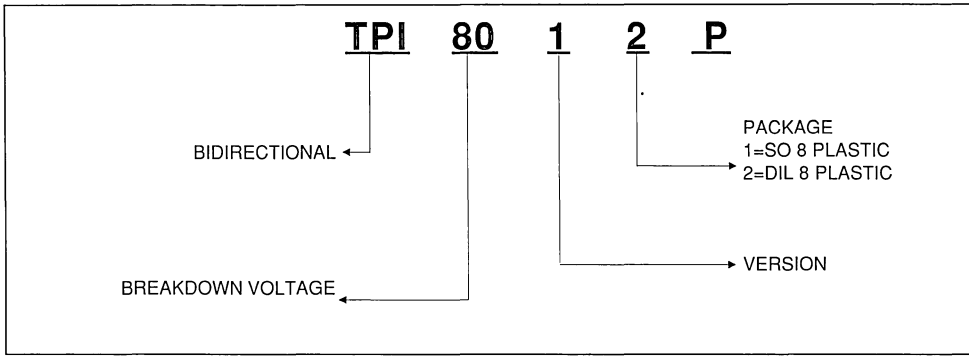


S Interface Protection



This component use an intemal diagram which allows to have symetrical characteristics with a good balanced behaviour.
This topology insures the same breakdown voltage level in positive and negative for differential or common mode surge.

ORDER CODE



MARKING

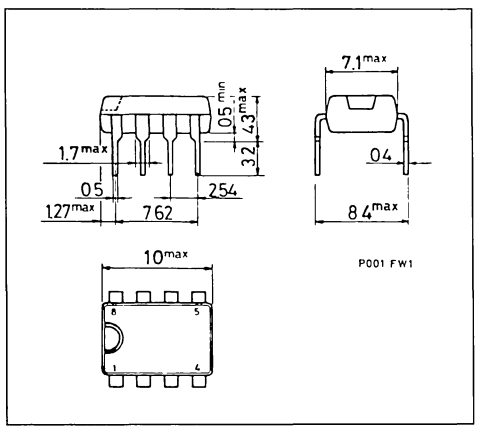
Package	Type	Marking
SO8	TPI8011 TPI12011	TPI80 TPI120

Package	Type	Marking
DIL8	TPI8012 TPI12012	TPI80 TPI120

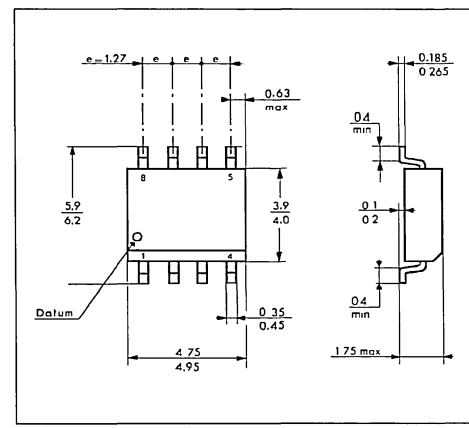
Packaging : Products supplied in antistatic tubes.

PACKAGE MECHANICAL DATA (in millimeters)

DIL 8 Plastic

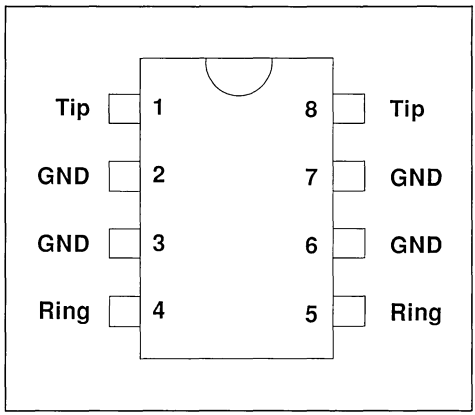


SO 8 Plastic

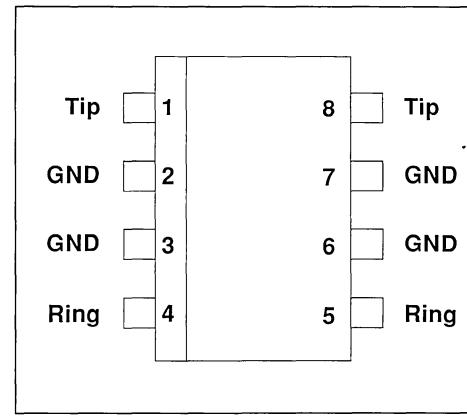


CONNECTION DIAGRAM

DIL 8 Plastic



SO 8 Plastic



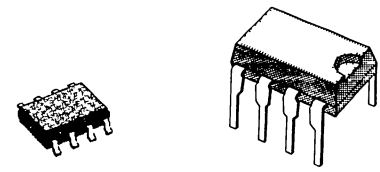
SGS-THOMSON MICROELECTRONICS

TPP25011
TPP25012

PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR AND CURRENT REGULATION

FEATURES

- UNIDIRECTIONAL FUNCTION
- PROGRAMMABLE BREAKDOWN VOLTAGE UP TO 250 V
- PROGRAMMABLE CURRENT LIMITATION FROM 40 mA TO 500 mA
- HIGH SURGE CURRENT CAPABILITY I_{PP} = 30A 10/1000 µs
- AVAILABLE IN DIL 8 AND SO 8 PACKAGES.



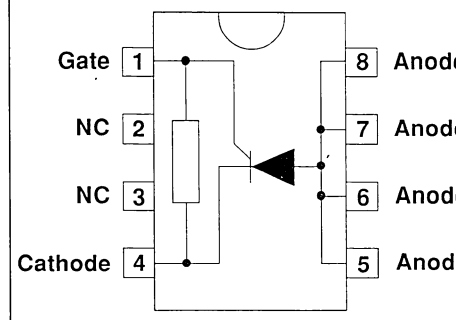
SO 8
(Plastic)

DIL 8
(Plastic)

DESCRIPTION

Dedicated to sensitive telecom equipment protection, this device can provide both voltage protection and current limitation with a very tight tolerance.
The breakdown voltage can be easily programmed by using an external zener diode.
A multiple protection mode can be also performed when using several zener diodes, providing to each line interface an optimized protection level.
The current limiting function is achieved with the use of a resistor between the gate and the cathode. The value of the resistor will determine the level of the desired current.

SCHEMATIC DIAGRAM

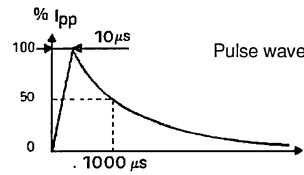


IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (- 40°C ≤ T_{amb} ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 5/320 µs 2/10 µs	30 40 75	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 10 ms tp = 1 s	5 3.5	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C



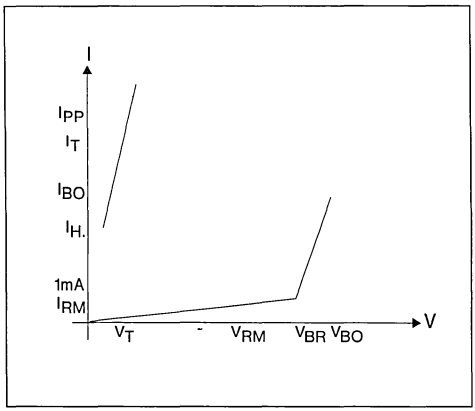
Pulse waveform 10/1000µs

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
R_{th} (j-a)	Junction-to-ambient	DIL 8 SO 8	125 171	°C/W °C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage @ I_T
I_{BO}	Breakover current
I_{PP}	Peak pulse current
V_G	Gate voltage
I_G	Firing gate current



OPERATION WITHOUT GATE (0°C ≤ T_{amb} ≤ 70°C)

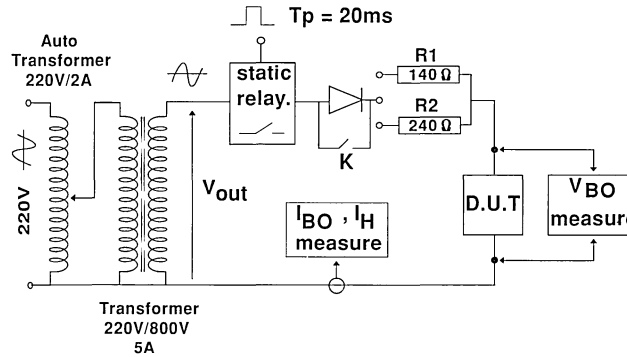
TYPE	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} max	@ min note 1	I_{BO} max	I_H min note 1	V_T max note 2	C max note 3
	µA	V	V	mA	V	mA	mA	mA	V	pF
TPP250	6	60	250	1	340	15	200	180	5	100

OPERATION WITH GATE (T_{amb} = 25°C)

Types	V_{GN} @ I_{GN} =30 mA min note 4	max	IG min V_A - C = 100 V	max
	V	V	mA	mA
TPP250	1.05	1.35	5	40

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters
Note 2 : Square pulse T_P= 500µs - I_T = 1A.
Note 3 : V_R = 5 V, F = 1MHz.
Note 4 : V_{GN} limits are given at the typical I_{GN} value

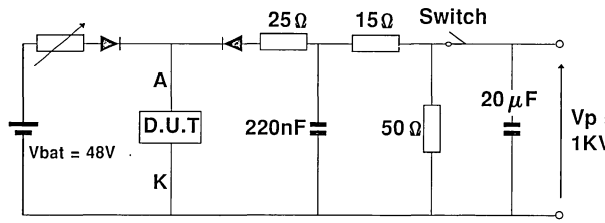
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

APPLICATION CIRCUIT

Overvoltage protection and current limitation

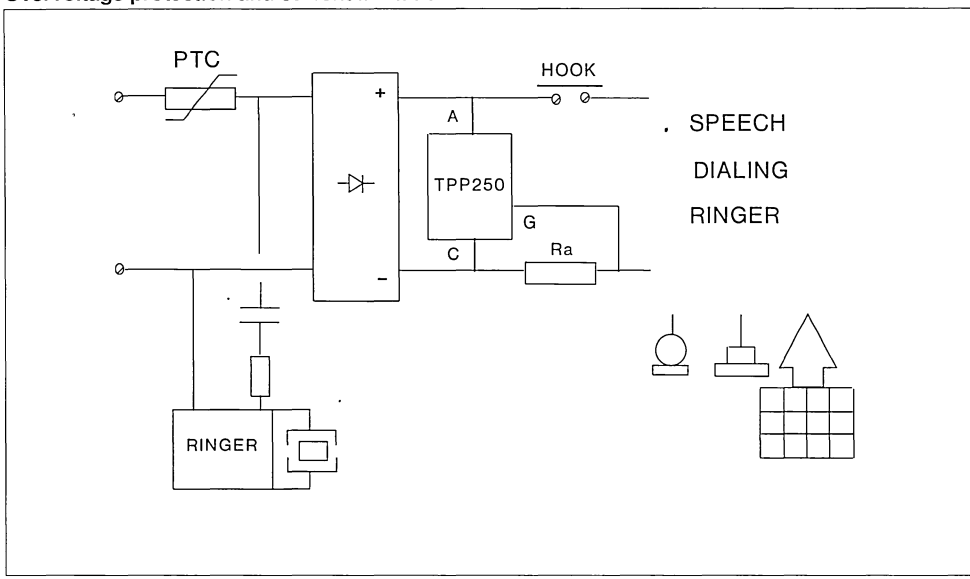
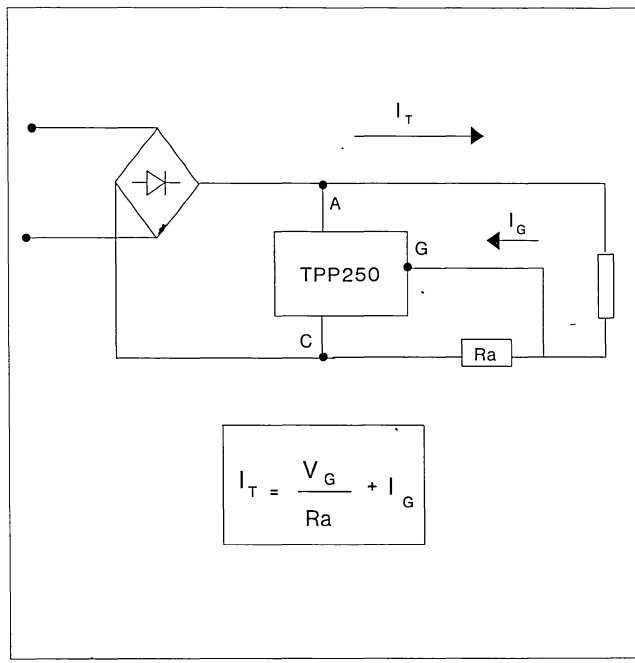
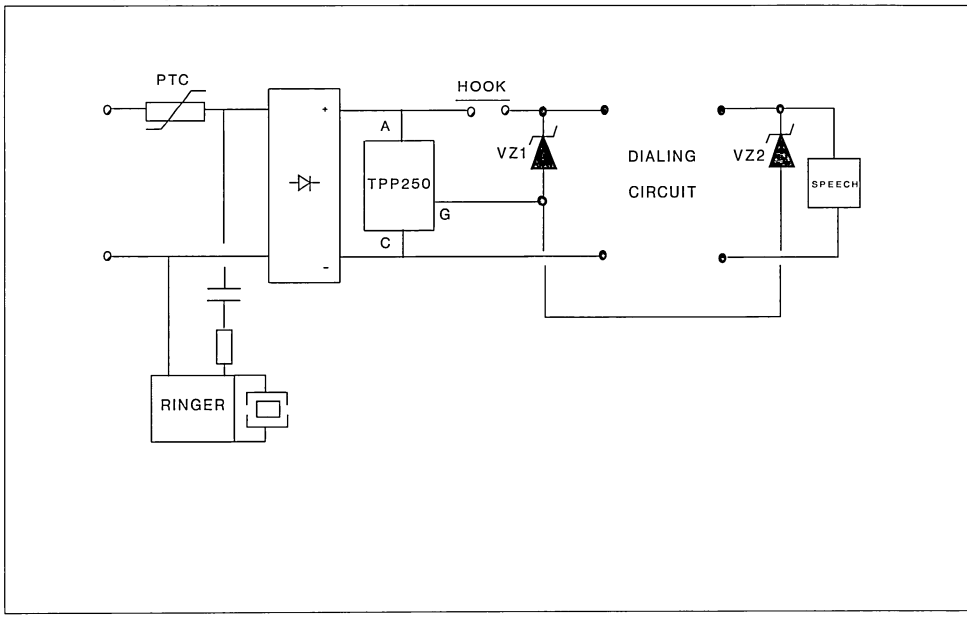


Table below gives the tolerance of the limited current I_T for each standardized resistor value.

CURRENT TOLERANCE		
R Ω (± 5%)	I_T mA min	I_T mA max
3.00	338	514
3.30	308	471
3.60	283	435
3.90	261	404
4.30	238	370
4.70	218	342
5.10	201	319
5.60	184	294
6.20	166	269
6.80	152	249
7.50	138	229
8.20	127	213
9.10	115	196
10.10	104	181
11.00	96	169
12.00	88	158
13.00	82	149
15.00	72	135
16.00	68	129
18.00	61	119
20.00	55	111
22.00	50	105
24.00	47	99
27.00	42	93
30.00	38	87



Ground key telephone set protection

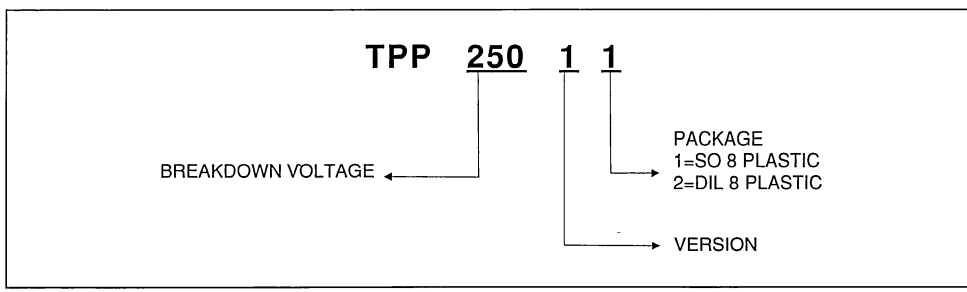


PROTECTION MODES :

OFF HOOK = Ringer circuit protection is insured with breakdown voltage at 250 V.

ON HOOK = In dialing mode and in conversation mode, the breakdown voltage of TPP250 can be adapted at different levels with two zener diodes.

ORDER CODE

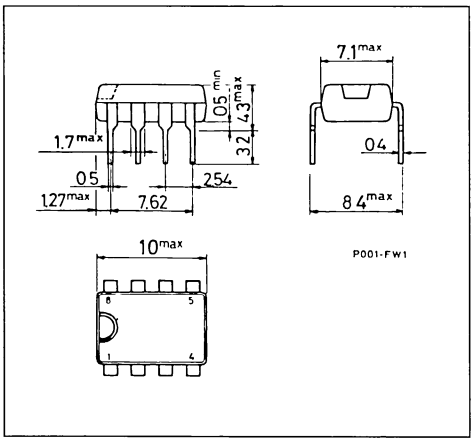


MARKING

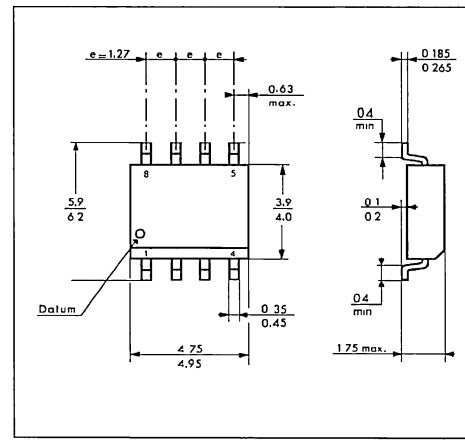
Package	Type	Marking
SO 8 DIL 8	TPP25011 TPP25012	TPP250 TPP250

PACKAGE MECHANICAL DATA (in millimeters)

DIL 8 Plastic

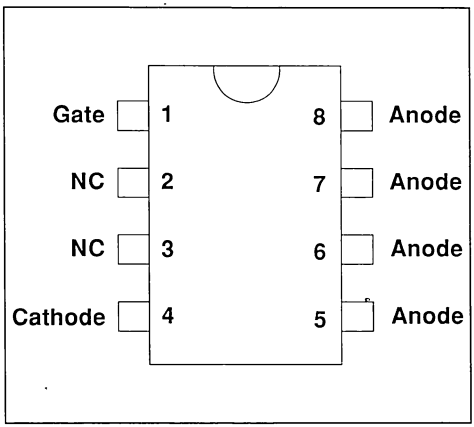


SO 8 Plastic

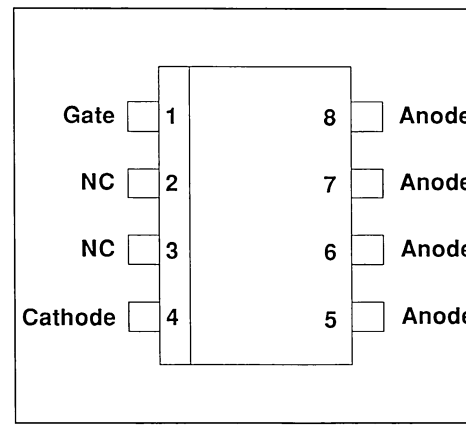


CONNECTION DIAGRAM

DIL 8 Plastic



SO 8 Plastic



Packaging : Products supplied in antistatic tubes.

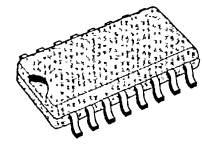
SGS-THOMSON MICROELECTRONICS

TSIxxxB5

TELEPHONE SET INTERFACE

FEATURES

- SINGLE DEVICE PROVIDING :
  DIODE BRIDGE
  BIDIRECTIONAL PROTECTION
- CROWBAR PROTECTION
- PEAK PULSE CURRENT :
  I_{PP} = 30A, 10/1000 µs
- VOLTAGE RANGE FROM 120V to 270V
- Maximum current : Io = 0.5

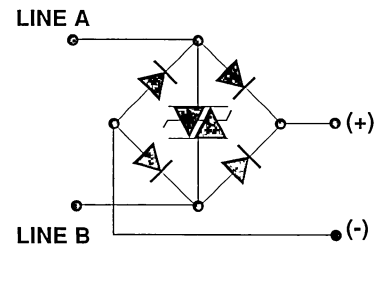


SO16
(Plastic)

IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

FUNCTIONAL DIAGRAM



ABSOLUTE RATINGS (limiting values) (-40°C ≤ Tamb ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 5/310 µs 2/10 µs	30 40 75	A
Io	Maximum current		0.5	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 10 ms tp = 1 s	5 3.5	A
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 150	°C °C

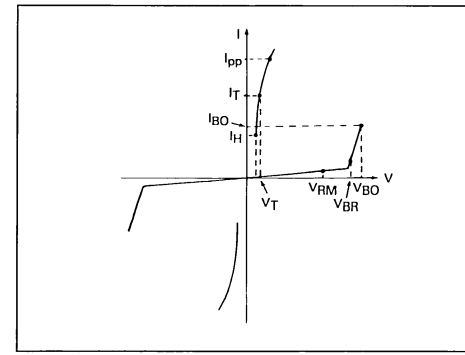
THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-a)	Junction-ambient thermal resistance - mounting on FR4	80	°C/W

ELECTRICAL CHARACTERISTICS

Tamb = 25°C

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
V_F	Forward Voltage Drop
I_{BO}	Breakover current
I_{PP}	Peak pulse current



PARAMETERS RELATED TO THE PROTECTION DEVICE

Types	I_R @ V_{RM} max		V_{BO} @ I_{BO} max note1	IH min note1	I_{BO} min note1	I_{BO} max	V_T max note2
	µA	V	V	mA	mA	mA	V
TSI120B5	1 5	50 120	180	150	50	400	8
TSI150B5	1 5	50 150	230	150	50	400	8
TSI180B5	1 5	50 180	250	150	50	400	8
TSI200B5	1 5	50 200	290	150	50	400	8
TSI270B5	1 5	50 270	380	150	50	400	8

PARAMETERS RELATED TO THE DIODE BRIDGE

Symbol	Test conditions	Value	Unit
V_F	I_F = 20mA note 3 i_F = 100mA note 3	0.9 1.0	V
C	note 4	200	pF

All parameters are tested at 25°C, except where indicated

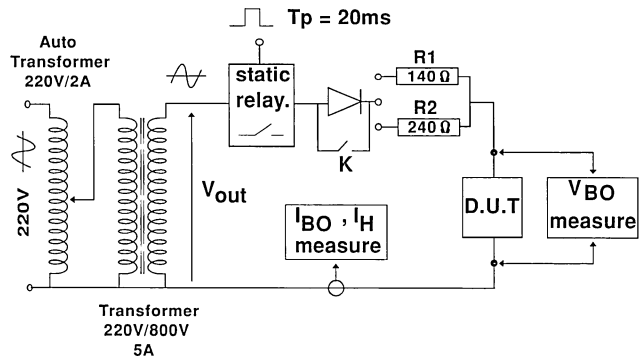
Note 1 : See test conditions for V_{BO}, I_{BO}, I_H parameters

Note 2 : Square pulse tp = 500 µs - I_T = 5A.

Note 3 : V_F is given for one diode

Note 4 : V_R = 0V, F = 1MHz.

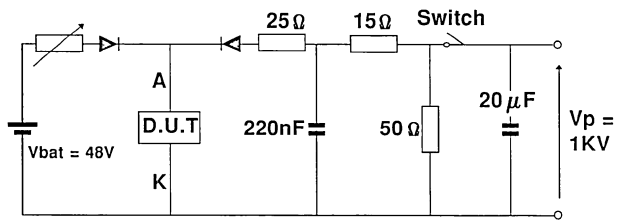
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

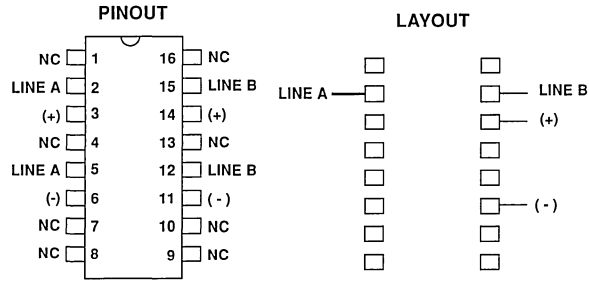
TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.

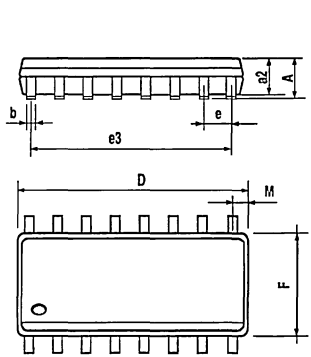
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.

3) The D.U.T will come back to the OFF-State withing a duration of 50 ms max.

PINOUT CONFIGURATION AND LAYOUT RECOMMENDATIONS :



PACKAGE MECHANICAL DATA



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0 35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° max					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.5		1.27	0.020		0.050
M			0.62			0.024
S	8° max					

MARKING : LOGO, DATE CODE, DEVICE CODE.

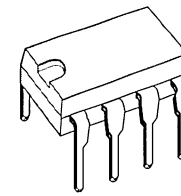
DEVICE	TSI120B5	TSI150B5	TSI180B5	TSI200B5	TSI270B5
MARKING	TSI120	TSI150	TSI180	TSI200	TSI270

PACKAGES

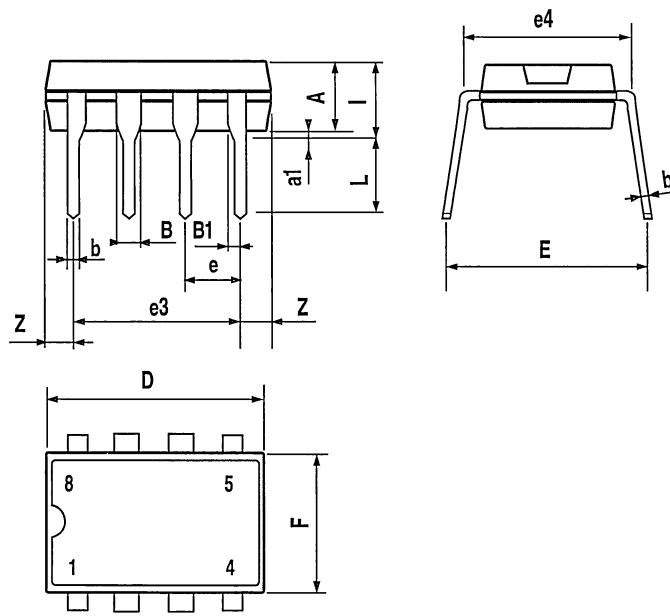
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
`e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Minidip (0.25)

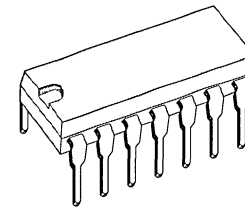


P001W

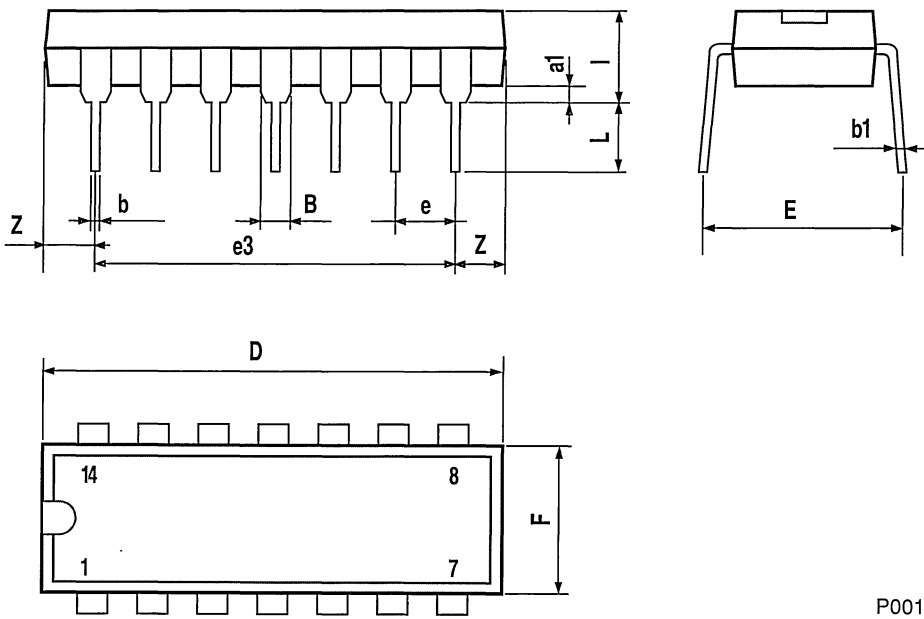
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP14

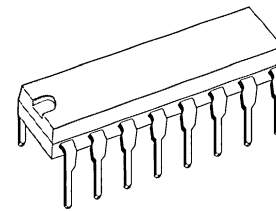


P001A

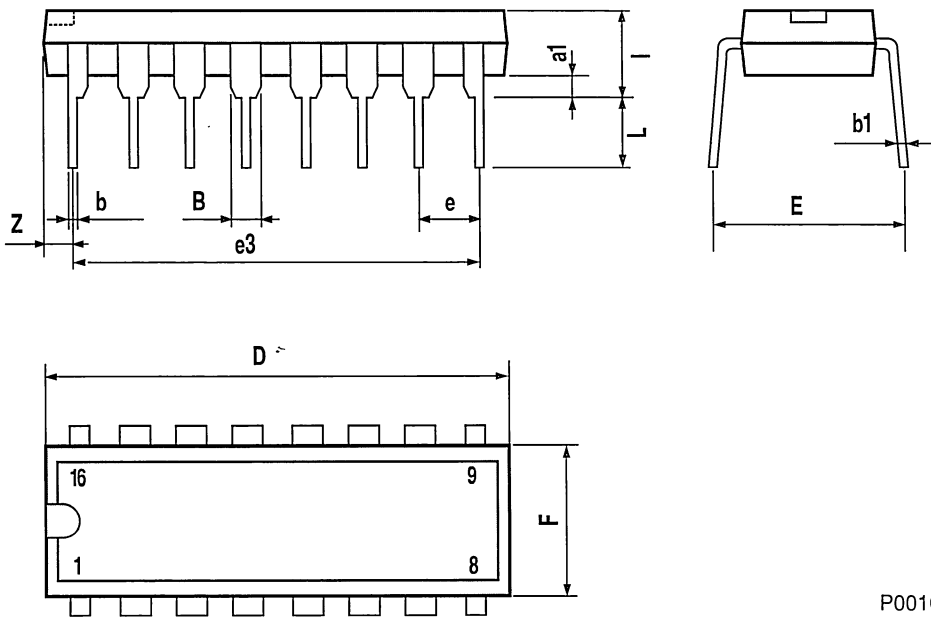
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP16 (0.25)

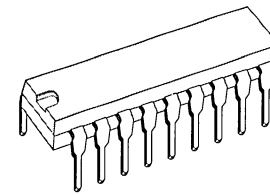


P001C

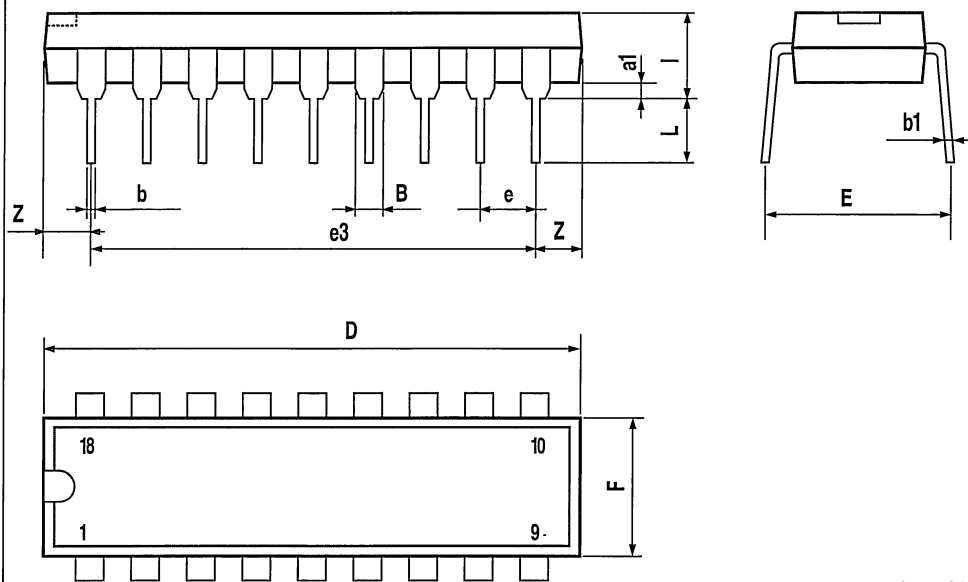
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.064
b		0.46			0.018	
b1		0.25			0.010	
D			23.24			0.914
E		8.5			0.335	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z		1.27	1.59		0.050	0.062

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP18 (0.25)

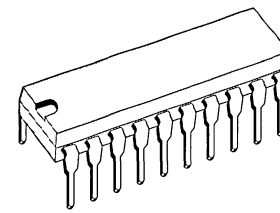


P001T

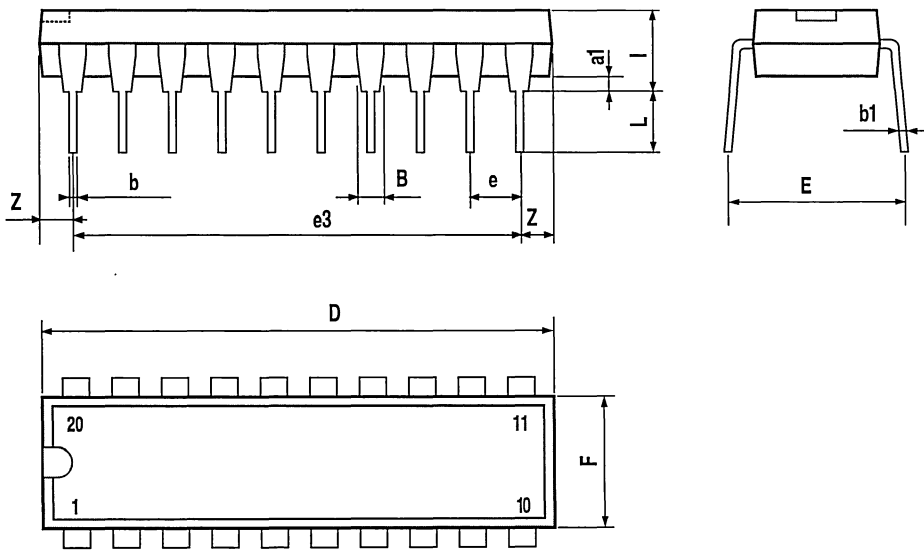
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP20 (0.25)

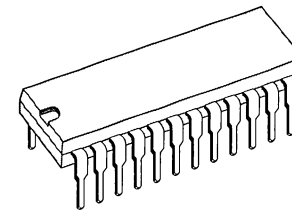


P001J

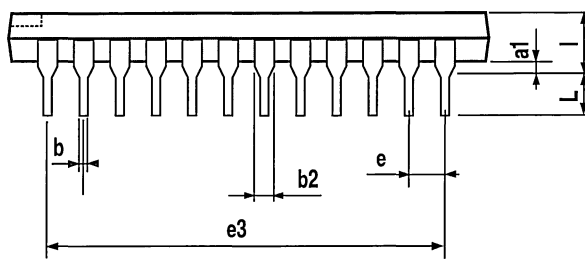
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

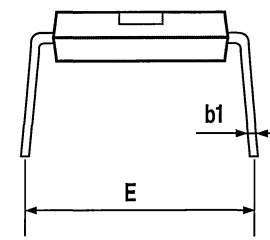
SGS-THOMSON MICROELECTRONICS

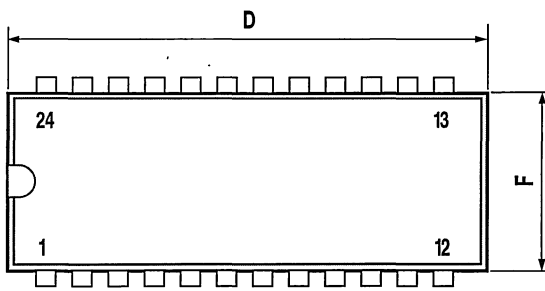
OUTLINE AND MECHANICAL DATA



DIP24 (0.25)





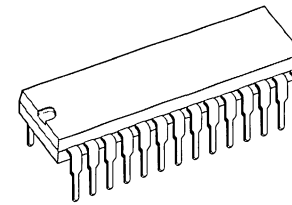


P043A

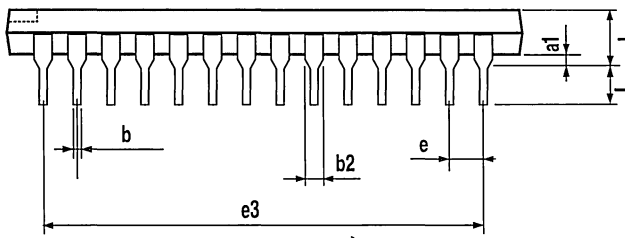
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

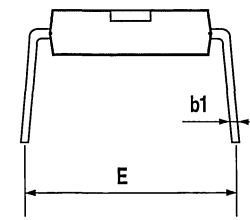
SGS-THOMSON MICROELECTRONICS

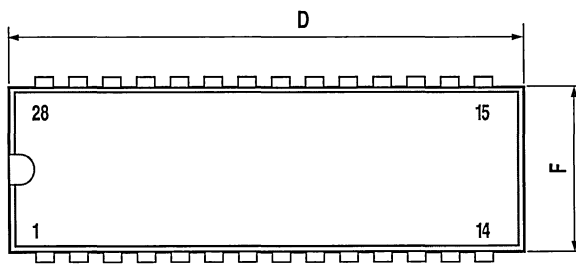
OUTLINE AND MECHANICAL DATA



DIP28





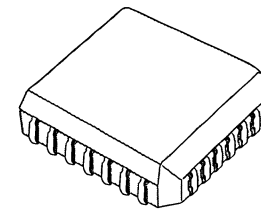


P043D

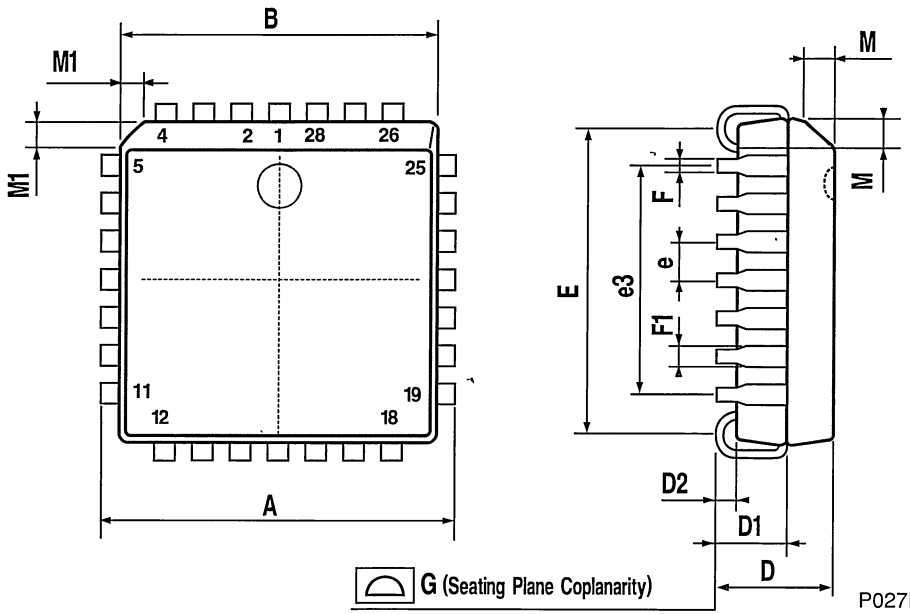
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



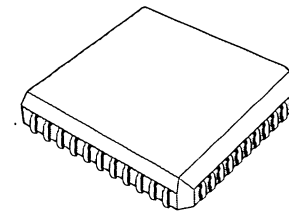
PLCC28



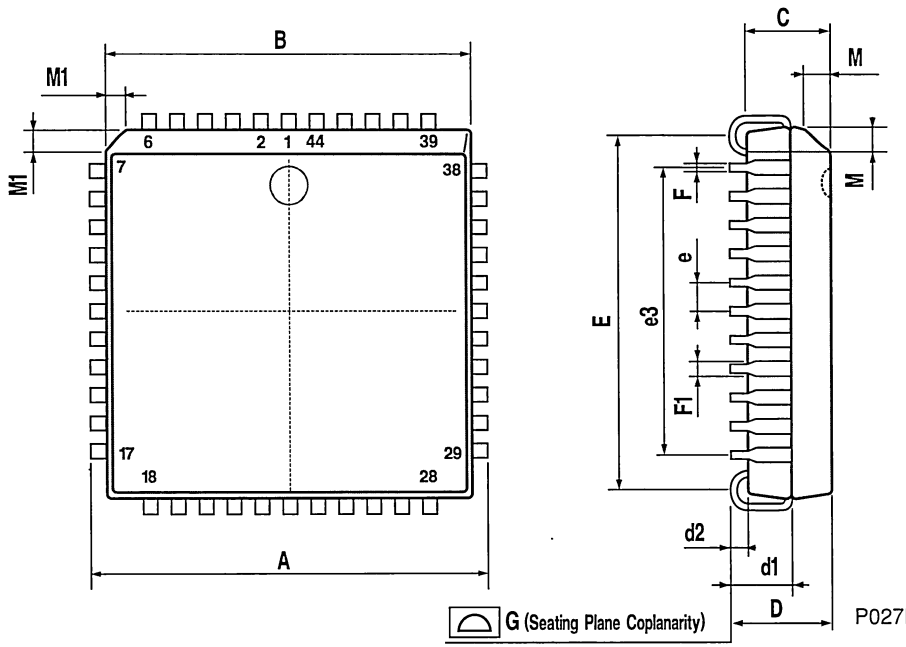
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



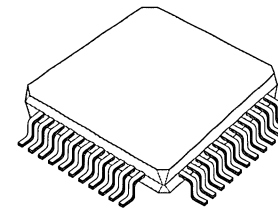
PLCC44



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.40			0.134
A1	0.25			0.01		
A2	2.55	2.80	3.05	0.10	0.11	0.12
B	0.35		0.50	0.014		0.020
C	0.13		0.23	0.005		0.009
D	16.95	17.20	17.45	0.667	0.677	0.687
D1	13.90	14.00	14.10	0.547	0.551	0.555
D2		10.00			0.394	
e		1.00			0.039	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E2		10.00			0.394	
F		1.60			0.063	
K	0°(min.), 7°(max.)					
L	0.65	0.80	0.95	0.025	0.031	0.037

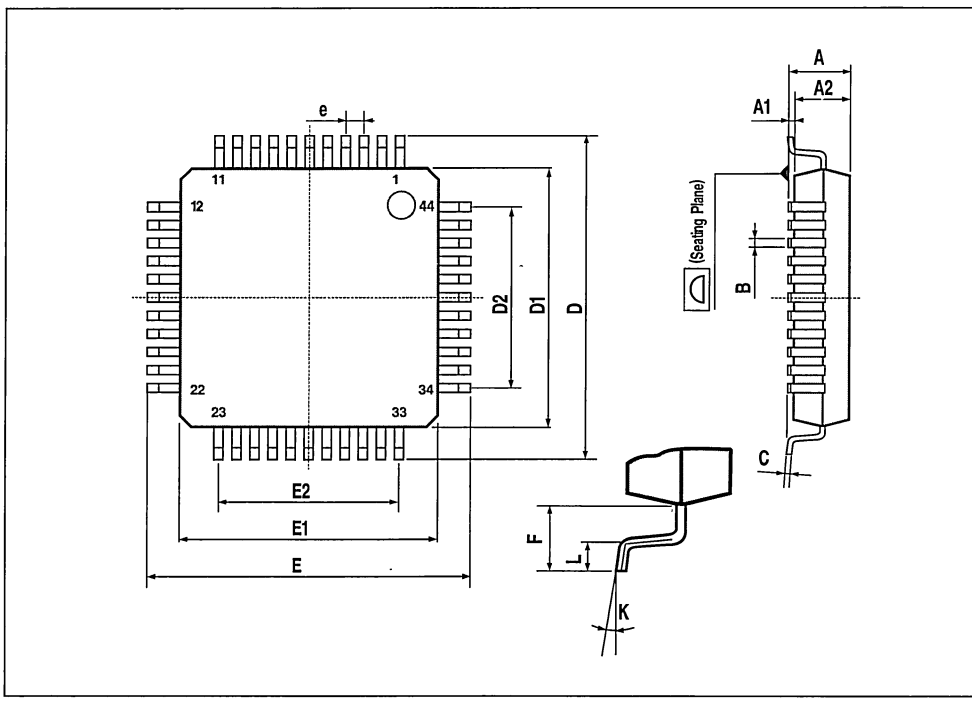
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PQFP44 (*)

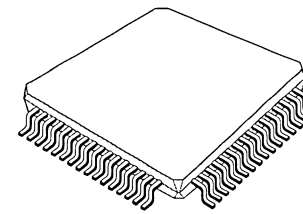
(*) Advanced information on a new package now in development or undergoing evaluation. Details are subject to change without notice.



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.40			0.134
A1	0.25			0.01		
A2	2.55	2.80	3.05	0.10	0.11	0.12
B	0.30		0.45	0.012		0.018
C	0.13		0.23	0.005		0.009
D	16.95	17.20	17.45	0.667	0.677	0.687
D1	13.90	14.00	14.10	0.547	0.551	0.555
D2		12.00			0.472	
e		0.80			0.031	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E2		12.00			0.472	
F		1.60			0.063	
K	0°(min.), 7°(max.)					
L	0.65	0.80	0.95	0.025	0.031	0.037

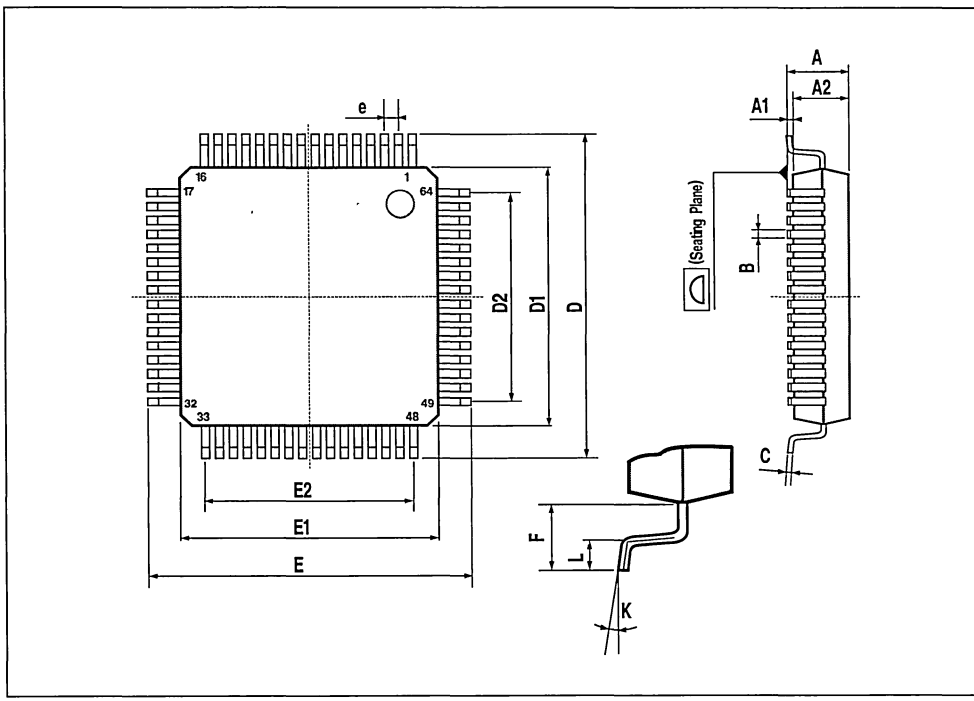
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PQFP64 (*)

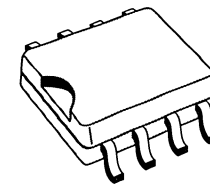
(*) Advanced information on a new package now in development or undergoing evaluation. Details are subject to change without notice.



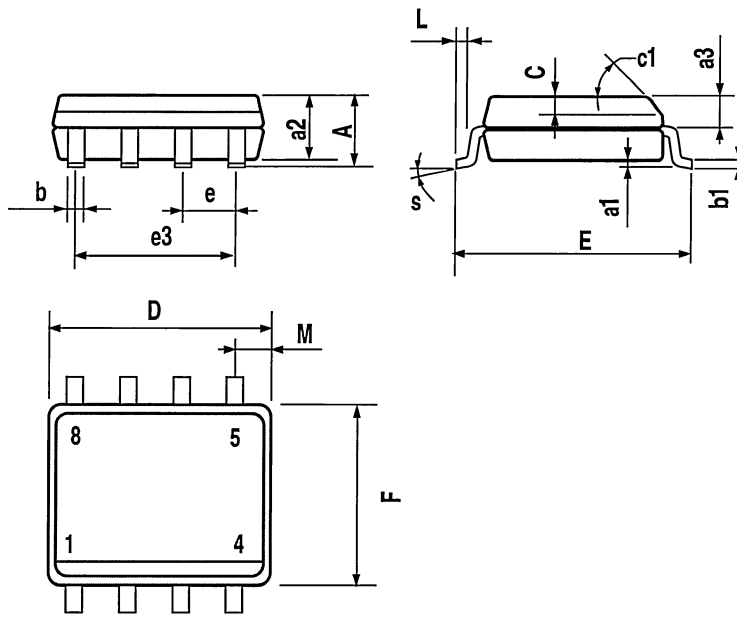
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO8

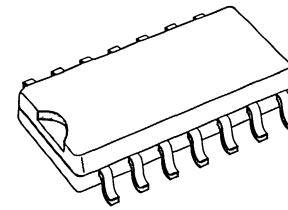


P013M

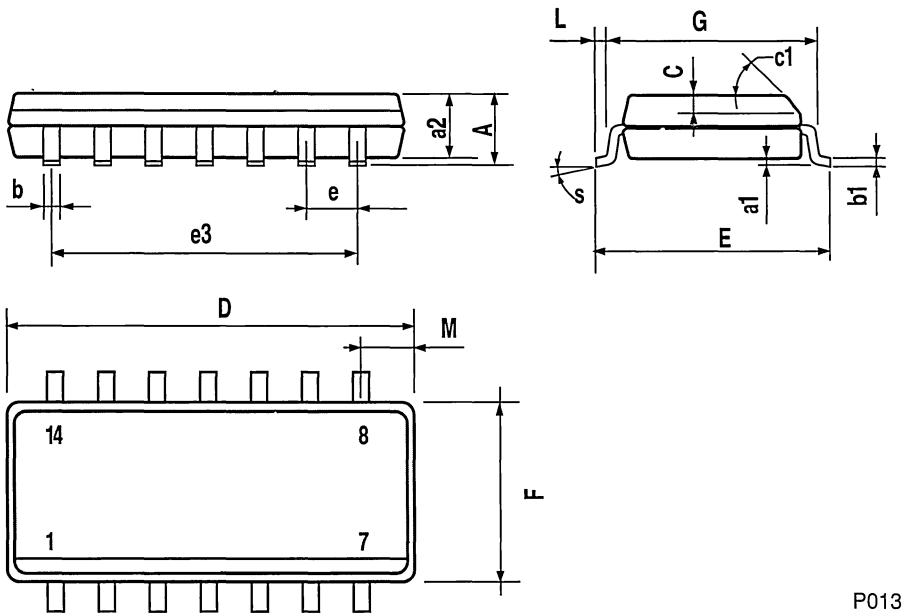
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.15		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO14

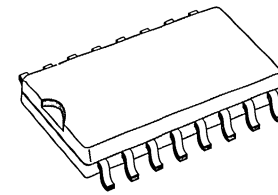


P013G

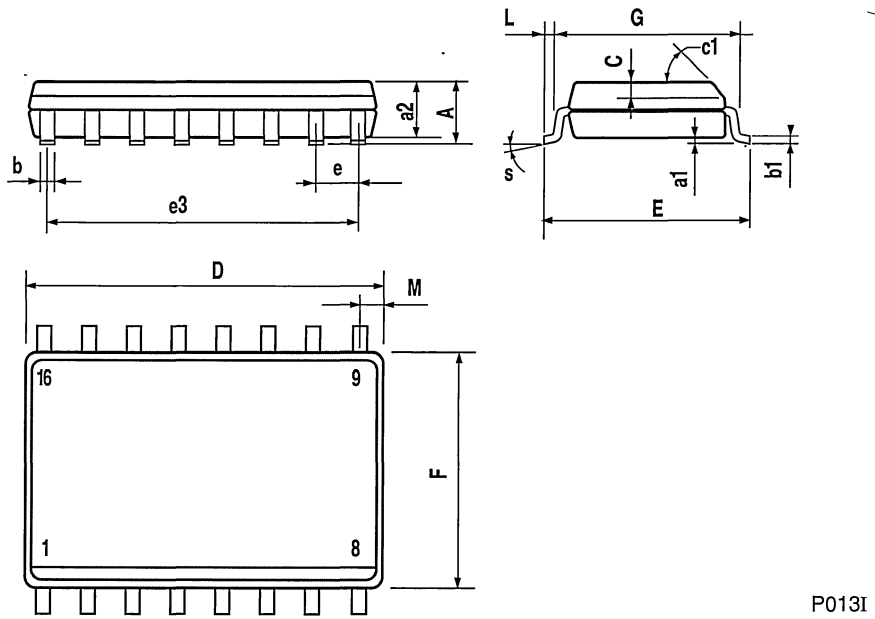
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.397		0.413
E	10.0		10.65	0.393		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.300
G	8.8		9.15	0.346		0.360
L	0.5		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO16L

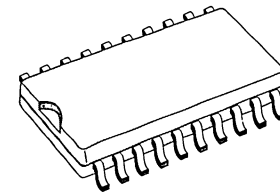


P013I

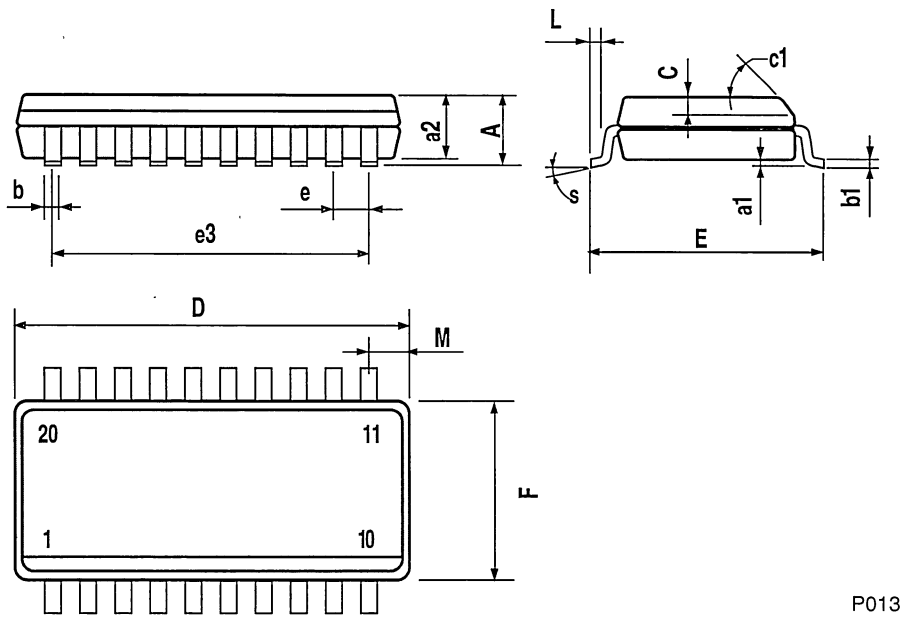
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	-
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO20

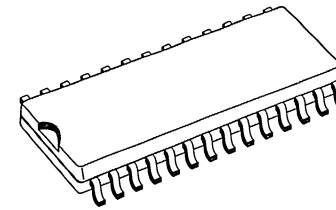


P013L

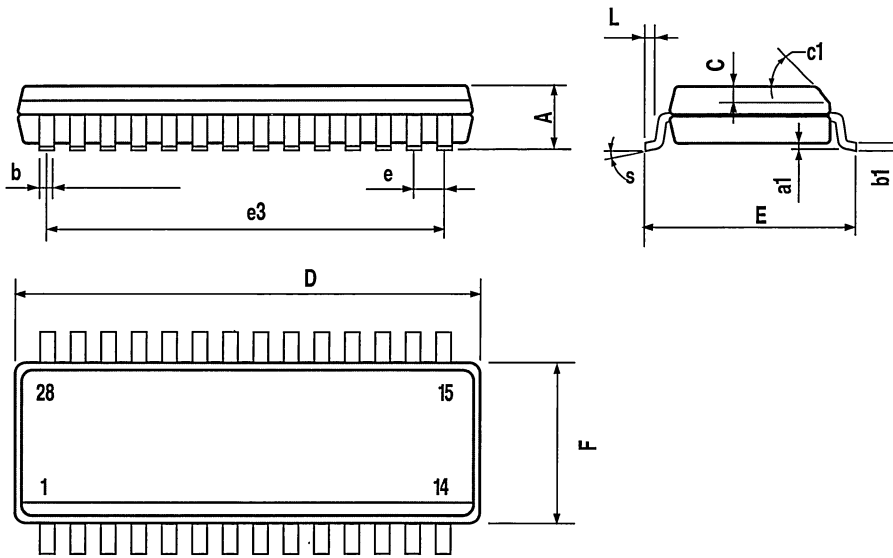
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO28



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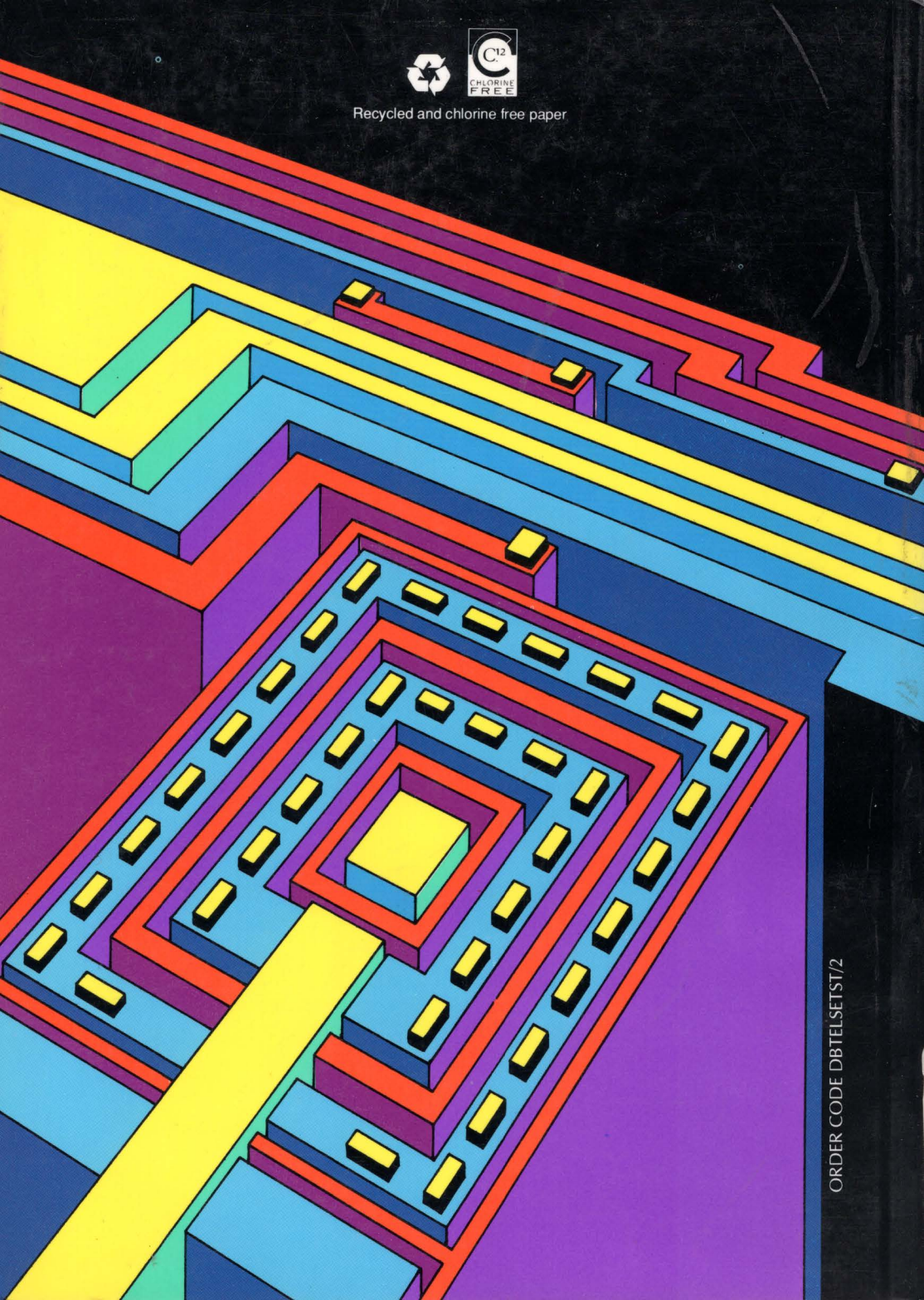

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