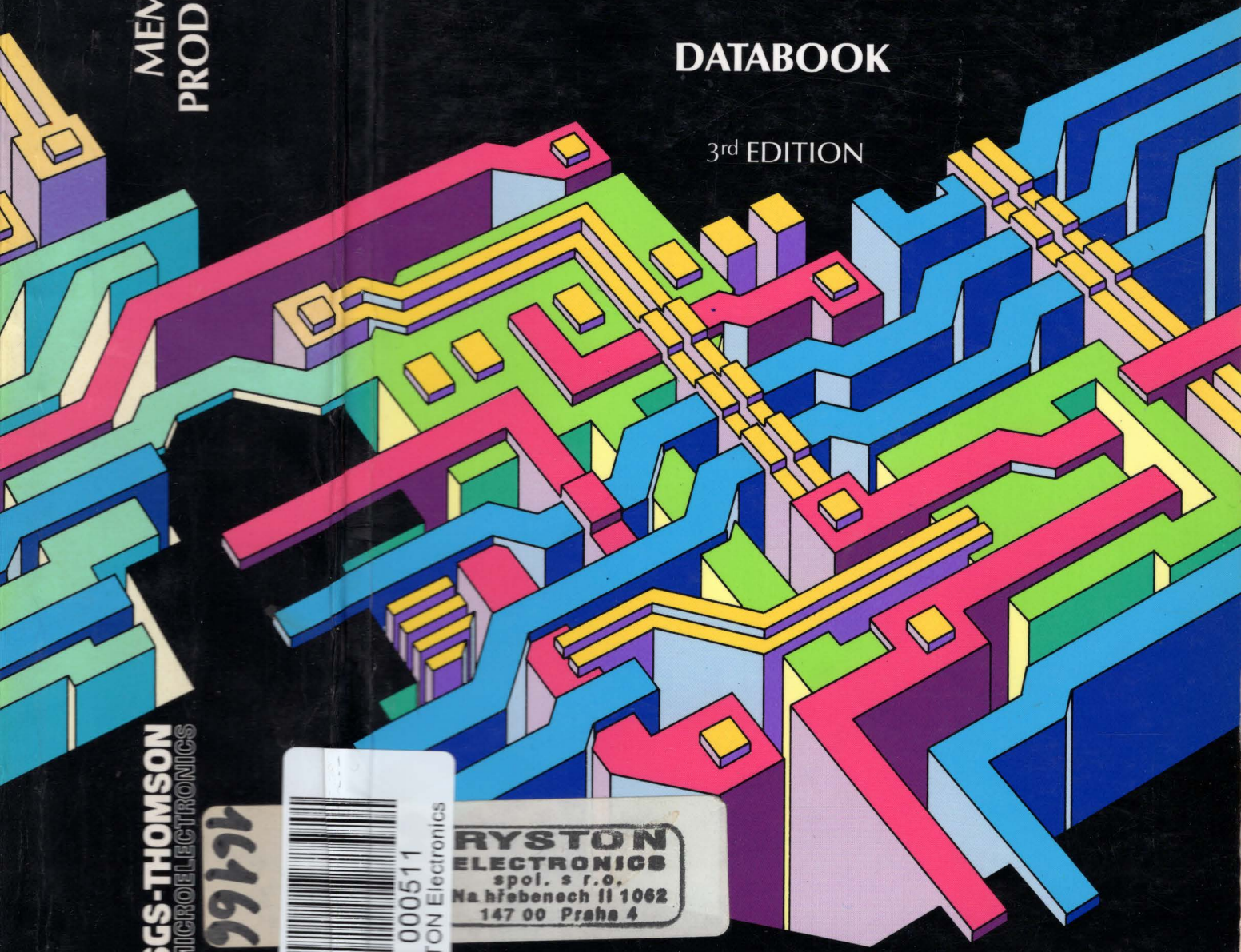
MEMORY PRODUCTS

DATABOOK

3rd EDITION



SGS-THOMSON MICROELECTRONICS

MEMORY PRODUCTS

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MEMORY PRODUCTS

DATABOOK

3rd EDITION

JUNE 1994

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

SGS-THOMSON Microelectronics manufactures an extensive range of memory products which can satisfy the needs of many applications. The products include,

Non-Volatile Memories: UV EPROM, OTP Memory, FLASH Memory, EEPROM and SMARTCARD PRODUCTS.

Static RAMs: Fast SRAM, Cache TAGRAM and burst RAM (BRAM), BiPORT FIFO, ZEROPOWER and TIMEKEEPER battery backed SRAMs.

This data book provides comprehensive, technical information on each family of memory products to aid selection and design for a specific use.

UV EPROMs (UV Eraseable Electrically Programmable Read Only Memories). This family consists of EPROMs which can be erased by exposure to Ultra Violet light through a quartz window in the package. The range of EPROMs is from 16K bit up to 16 Megabit and they are manufactured in two technologies, NMOS for 16K up to 512K densities and CMOS from 64K up to 16 Megabit densities. Memory access times are as fast as 60ns. Programming times have been reduced through the use of specially designed 'margin mode verify' circuits and the new PRESTO programming algorithms. Many of the CMOS types are able to be programed in the application board rather than in a separate programmer. For portable equipment needing low power consumption some sizes of EPROM are specified for operation in the read mode at down to 3V supply voltage.

OTP Memories (One Time Programmable Memories). These products are similar to UV EPROMs but are packaged in plastic packages, both Dual-In-Line and surface mounting types. They are not eraseable, but may be programed one time only by the customer.

FLASH Memories (Electrically Programmable and Eraseable Memories). FLASH Memories provide an extra degree of flexibility for the system designer by implementing both electrical programming and erasure in the application. This gives the memories additional functionality and enables customers to both load the contents at a late stage in the manufacturing line, or field upgrade the equipment. New applications such as Mass Storage for computers are also foreseen for FLASH memories. The manufacturing process, although more demanding in terms of process control, is basically similar to the EPROM, thus ensuring a similar evolution of memory density, performance and reliability.

EEPROMs (Electrically Eraseable and Programmable Memories). Different from the FLASH Memory which may be erased only by chip or large sector, the EEPROM may be erased and written byte-by- byte. Two types of EEPROM are included in our range: serial bus and parallel access types. EEPROMs are widely used for storing equipment set-up parameters or data tables. The special CMOS process and cell designs used by SGS-THOMSON allows us to offer products with a very high endurance against wear-out that occurs after many erase/write cycles in this type of memory. Our EEPROMs are able to typically withstand 5 to 10 million cycles together with over 10 years data retention.

SMARTCARD PRODUCTS. Three families of Smartcard Product are included. All are based on EEPROM technology and in addition include logic, microcomputer cores and/or cryptographic mathematical processors. The logic and microcomputers provide both secure memory access and serial I/O operation. Applications include telephone cards, banking cards, health cards, transportation and many other uses.

INTRODUCTION

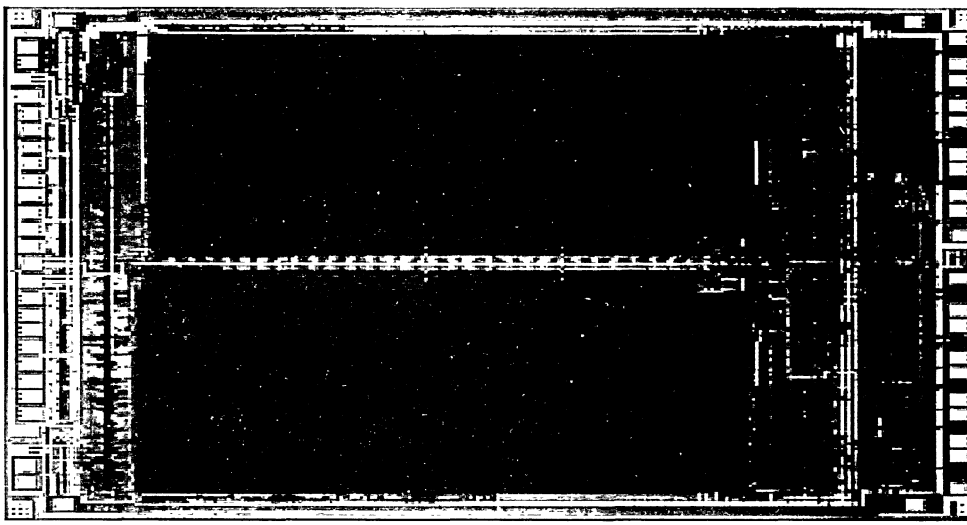
Fast SRAM and BRAM. Using an innovative submicron CMOS technology SGS-THOMSON offers a range of standard Fast SRAM and specialty SRAMs (BRAMs) for data cache applications.

Cache TAGRAM. Computer cache systems are made using a combination of memory to store cache data addresses (the TAGRAM) and the cache data itself (either a standard Fast SRAM or a BRAM). The TAGRAM family allows customers to design very flexible and high performance cache subsystems.

BiPORT FIFOs. The BiPORT FIFO family is a series of fast FIFO memories based on SRAM technology, with built-in address registers for read and write pointers. Sizes range from 512 bit to 8K bit and the architecture allows both depth and width expansion.

ZEROPOWER and TIMEKEEPER. This range of products satisfies a very important sector of applications: they provide fast read/write non-volatile memory for use as back-up storage, for example for data protection at power failure. The basic ZEROPOWER products consist of an ultra low power SRAM with an integrated supply voltage detector and a switch-over circuit to a battery to sustain the contents at power down. The package includes an integrated lithium battery which has the capacity to maintain the memory contents for up to 10 years. TIMEKEEPER products are similar but include also a quartz controlled clock/calendar which is also powered by the back-up battery.

SGS-THOMSON has an extensive program of both process and product development which results in many new and upgraded product introductions every year. Please contact your nearest sales office to learn about new products that have been introduced since this book was published.



The 4 Megabit FLASH Memory developed in 0.6 micron CMOS Technology.

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CMOS UV EPROM and OTP ROM

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
64K	M27C64A-15F1	8K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C64A-20F1	8K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C64A-25F1	8K x 8	250	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C64A-30F1	8K x 8	300	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C64A-20F6	8K x 8	200	5V ± 10%	30mA / 100µA	–40 to 85	FDIP28W
	M27C64A-25F6	8K x 8	250	5V ± 10%	30mA / 100µA	–40 to 85	FDIP28W
	M27C64A-30F6	8K x 8	300	5V ± 10%	30mA / 100µA	–40 to 85	FDIP28W
256K	M27C256B-70XF1	32K x 8	70	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C256B-80XF1	32K x 8	80	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C256B-10XF1	32K x 8	100	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C256B-12XF1	32K x 8	120	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C256B-15XF1	32K x 8	150	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C256B-20XF1	32K x 8	200	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C256B-25XF1	32K x 8	250	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C256B-10F1	32K x 8	100	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C256B-12F1	32K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C256B-15F1	32K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C256B-20F1	32K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C256B-25F1	32K x 8	250	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C256B-15XF6	32K x 8	150	5V ± 5%	30mA / 100µA	–40 to 85	FDIP28W
	M27C256B-20XF6	32K x 8	200	5V ± 5%	30mA / 100µA	–40 to 85	FDIP28W
	M27C256B-90F6	32K x 8	90	5V ± 10%	30mA / 100µA	–40 to 85	FDIP28W
	M27C256B-12F6	32K x 8	120	5V ± 10%	30mA / 100µA	–40 to 85	FDIP28W

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
256K	M27C256B-15F6	32K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	FDIP28W
	M27C256B-20F6	32K x 8	200	5V ± 10%	30mA / 100µA	–40 to 85	FDIP28W
	M27C256B-25F6	32K x 8	250	5V ± 10%	30mA / 100µA	–40 to 85	FDIP28W
	M27C256B-15XF3	32K x 8	150	5V ± 5%	30mA / 100µA	–40 to 125	FDIP28W
	M27C256B-20F3	32K x 8	200	5V ± 10%	30mA / 100µA	–40 to 125	FDIP28W
	M27C256B-90B1	32K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	PDIP28
	M27C256B-12B1	32K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PDIP28
	M27C256B-15B1	32K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PDIP28
	M27C256B-20B1	32K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PDIP28
	M27C256B-15B6	32K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	PDIP28
	M27C256B-20B7	32K x 8	200	5V ± 10%	30mA / 100µA	–40 to 105	PDIP28
	M27C256B-20B3	32K x 8	200	5V ± 10%	30mA / 100µA	–40 to 125	PDIP28
	M27C256B-90C1	32K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C256B-12C1	32K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C256B-15C1	32K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C256B-20C1	32K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C256B-12C6	32K x 8	120	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32
	M27C256B-15C6	32K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32
	M27C256B-20C6	32K x 8	200	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32
	M27C256B-90N1	32K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	TSOP28
	M87C257-12XF1	32K x 8	120	5V ± 5%	30mA / 200µA	0 to 70	FDIP28W
	M87C257-20XF1	32K x 8	200	5V ± 5%	30mA / 200µA	0 to 70	FDIP28W
	M87C257-12F1	32K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	FDIP28W

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
256K	M87C257-20F1	32K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	FDIP28W
	M87C257-15F6	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	FDIP28W
	M87C257-15C1	32K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PLCC32
	M87C257-15C6	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PLCC32
	M87C257-20C6	32K x 8	200	5V ± 10%	30mA / 200µA	–40 to 85	PLCC32
	M87C257-15C3	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PLCC32
512K	M27C512-70XF1	64K x 8	70	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C512-80XF1	64K x 8	80	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C512-12XF1	64K x 8	120	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C512-15XF1	64K x 8	150	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C512-20XF1	64K x 8	200	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C512-25XF1	64K x 8	250	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W
	M27C512-10F1	64K x 8	100	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C512-12F1	64K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C512-15F1	64K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C512-20F1	64K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C512-25F1	64K x 8	250	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W
	M27C512-15XF6	64K x 8	150	5V ± 5%	30mA / 100µA	–40 to 85	FDIP28W
	M27C512-15F6	64K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	FDIP28W
	M27C512-20F6	64K x 8	200	5V ± 10%	30mA / 100µA	–40 to 85	FDIP28W
	M27C512-12F3	64K x 8	120	5V ± 10%	30mA / 100µA	–40 to 125	FDIP28W
	M27C512-20F3	64K x 8	200	5V ± 10%	30mA / 100µA	–40 to 125	FDIP28W

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
512K	M27C512-90B1	64K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	PDIP28
	M27C512-12B1	64K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PDIP28
	M27C512-15B1	64K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PDIP28
	M27C512-20B1	64K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PDIP28
	M27C512-15B6	64K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	PDIP28
	M27C512-20B6	64K x 8	200	5V ± 10%	30mA / 100µA	–40 to 85	PDIP28
	M27C512-12B3	64K x 8	120	5V ± 10%	30mA / 100µA	–40 to 125	PDIP28
	M27C512-20B3	64K x 8	200	5V ± 10%	30mA / 100µA	–40 to 125	PDIP28
	M27C512-90C1	64K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C512-12C1	64K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C512-15C1	64K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C512-20C1	64K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27V512-200K1	64K x 8	200	3 to 5.5V	10mA / 100µA	0 to 70	PLCC32
	M27C512-12C6	64K x 8	120	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32
	M27C512-20C6	64K x 8	200	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32
	M27C512-12C3	64K x 8	120	5V ± 10%	30mA / 100µA	–40 to 125	PLCC32
	M27C512-90N1	64K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	TSOP28
	M27C512-12N1	64K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	TSOP28
	M27V512-200N1	64K x 8	200	3 to 5.5V	10mA / 100µA	0 to 70	TSOP28
1M	M27C1001-70XF1	128K x 8	70	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W
	M27C1001-80XF1	128K x 8	80	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W
	M27C1001-12F1	128K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W
	M27C1001-12XF1	128K x 8	120	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
1M	M27C1001-15XF1	128K x 8	150	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W
	M27C1001-20XF1	128K x 8	200	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W
	M27C1001-25XF1	128K x 8	250	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W
	M27C1001-10F1	128K x 8	100	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W
	M27C1001-15F1	128K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W
	M27C1001-20F1	128K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W
	M27C1001-25F1	128K x 8	250	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W
	M27C1001-20XF6	128K x 8	200	5V ± 5%	30mA / 100µA	–40 to 85	FDIP32W
	M27C1001-12F6	128K x 8	120	5V ± 10%	30mA / 100µA	–40 to 85	FDIP32W
	M27C1001-15F6	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	FDIP32W
	M27C1001-20F6	128K x 8	200	5V ± 10%	30mA / 100µA	–40 to 85	FDIP32W
	M27C1001-10XF3	128K x 8	100	5V ± 5%	30mA / 100µA	–40 to 125	FDIP32W
	M27C1001-10L1	Use M27V101-200L6					LCCC32W
	M27C1001-15B1	128K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PDIP32
	M27C1001-12B3	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 125	PDIP32
	M27C1001-90C1	128K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C1001-10C1	128K x 8	100	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C1001-12C1	128K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C1001-15C1	128K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C1001-20C1	128K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27V101-200K1	128K x 8	200	3 to 5.5V	30mA / 100µA	0 to 70	PLCC32
	M27C1001-90C6	128K x 8	90	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32
	M27C1001-12C6	128K x 8	120	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
1M	M27C1001-15C6	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32
	M27V101-200L6	128K x 8	200	3.2 to 5.5V	30mA / 100µA	–40 to 85	LCCC32W
	M27C1024-80XF1	64K x 16	80	5V ± 5%	35mA / 100µA	0 to 70	FDIP40W
	M27C1024-12XF1	64K x 16	120	5V ± 5%	35mA / 100µA	0 to 70	FDIP40W
	M27C1024-15XF1	64K x 16	150	5V ± 5%	35mA / 100µA	0 to 70	FDIP40W
	M27C1024-20XF1	64K x 16	200	5V ± 5%	35mA / 100µA	0 to 70	FDIP40W
	M27C1024-10F1	64K x 16	100	5V ± 10%	35mA / 100µA	0 to 70	FDIP40W
	M27C1024-12F1	64K x 16	120	5V ± 10%	35mA / 100µA	0 to 70	FDIP40W
	M27C1024-15F1	64K x 16	150	5V ± 10%	35mA / 100µA	0 to 70	FDIP40W
	M27C1024-20F1	64K x 16	200	5V ± 10%	35mA / 100µA	0 to 70	FDIP40W
	M27C1024-25F1	64K x 16	250	5V ± 10%	35mA / 100µA	0 to 70	FDIP40W
	M27C1024-12XF6	64K x 16	120	5V ± 5%	35mA / 100µA	–40 to 85	FDIP40W
	M27C1024-10C1	64K x 16	100	5V ± 10%	35mA / 100µA	0 to 70	PLCC44
	M27C1024-12C1	64K x 16	120	5V ± 10%	35mA / 100µA	0 to 70	PLCC44
	M27C1024-15C1	64K x 16	150	5V ± 10%	35mA / 100µA	0 to 70	PLCC44
	M27C1024-12C6	64K x 16	120	5V ± 10%	35mA / 100µA	–40 to 85	PLCC44
2M	M27C2001-80XF1	256K x 8	80	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W
	M27C2001-15XF1	256K x 8	150	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W
	M27C2001-10F1	256K x 8	100	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W
	M27C2001-12F1	256K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W
	M27C2001-15F1	256K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W
	M27C2001-20F1	256K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W
	M27C2001-12F6	256K x 8	120	5V ± 10%	30mA / 100µA	–40 to 85	FDIP32W

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
2M	M27C2001-10L1	Use M27V201-200L6					LCCC32W
	M27C2001-10C1	256K x 8	100	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C2001-12C1	256K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27C2001-15C1	256K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M27V201-200K1	256K x 8	200	3 to 5.5V	30mA / 100µA	0 to 70	PLCC32
	M27C2001-12C6	256K x 8	120	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32
	M27C2001-15C6	256K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32
	M27V201-200L6	256K x 8	200	3.2 to 5.5V	30mA / 100µA	–40 to 85	LCCC32W
4M	M27C4001-80XF1	512K x 8	80	5V ± 5%	50mA / 100µA	0 to 70	FDIP32W
	M27C4001-10XF1	512K x 8	100	5V ± 5%	50mA / 100µA	0 to 70	FDIP32W
	M27C4001-10F1	512K x 8	100	5V ± 10%	50mA / 100µA	0 to 70	FDIP32W
	M27C4001-12F1	512K x 8	120	5V ± 10%	50mA / 100µA	0 to 70	FDIP32W
	M27C4001-15F1	512K x 8	150	5V ± 10%	50mA / 100µA	0 to 70	FDIP32W
	M27C4001-12F6	512K x 8	120	5V ± 10%	50mA / 100µA	–40 to 85	FDIP32W
	M27C4001-95XL6	512K x 8	95	5V ± 5%	50mA / 100µA	–40 to 85	LCCC32W
	M27C4001-10C1	512K x 8	100	5V ± 10%	50mA / 100µA	0 to 70	PLCC32
	M27C4001-12C1	512K x 8	120	5V ± 10%	50mA / 100µA	0 to 70	PLCC32
	M27C4001-15C1	512K x 8	150	5V ± 10%	50mA / 100µA	0 to 70	PLCC32
	M27V401-200K1	512K x 8	200	3 to 5.5V	50mA / 100µA	0 to 70	PLCC32
	M27C4001-12C6	512K x 8	120	5V ± 10%	50mA / 100µA	–40 to 85	PLCC32
	M27V401-200L6	512K x 8	200	3.2 to 5.5V	50mA / 100µA	–40 to 85	LCCC32W
	M27C4002-80XF1	256K x 16	80	5V ± 5%	50mA / 100µA	0 to 70	FDIP40W
	M27C4002-10XF1	256K x 16	100	5V ± 5%	50mA / 100µA	0 to 70	FDIP40W

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
4M	M27C4002-10F1	256K x 16	100	5V ± 10%	50mA / 100µA	0 to 70	FDIP40W
	M27C4002-12F1	256K x 16	120	5V ± 10%	50mA / 100µA	0 to 70	FDIP40W
	M27C4002-15F1	256K x 16	150	5V ± 10%	50mA / 100µA	0 to 70	FDIP40W
	M27C4002-12F6	256K x 16	120	5V ± 10%	50mA / 100µA	–40 to 85	FDIP40W
	M27C4002-15F6	256K x 16	150	5V ± 10%	50mA / 100µA	–40 to 85	FDIP40W
	M27C4002-12J6	256K x 16	120	5V ± 10%	50mA / 100µA	–40 to 85	JLCC44W
	M27C4002-12C1	256K x 16	120	5V ± 10%	50mA / 100µA	0 to 70	PLCC44
	M27C4002-15C1	256K x 16	150	5V ± 10%	50mA / 100µA	0 to 70	PLCC44
	M27C4002-12C6	256K x 16	120	5V ± 10%	50mA / 100µA	0 to 70	PLCC44
	M27C4002-15C6	256K x 16	150	5V ± 10%	50mA / 100µA	0 to 70	PLCC44
16M	M27C160-200F1	x8 / x16	200	5V ± 10%	50mA / 100µA	0 to 70	FDIP42W

NMOS UV EPROM

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
16K	M2716F1	2K x 8	450	5V ± 5%	100mA / 25mA	0 to 70	FDIP24W
	M2716-1F1	2K x 8	350	5V ± 10%	100mA / 25mA	0 to 70	FDIP24W
	M2716F6	2K x 8	450	5V ± 5%	100mA / 25mA	–40 to 85	FDIP24W
	M2716-1F6	2K x 8	350	5V ± 10%	100mA / 25mA	–40 to 85	FDIP24W
32K	M2732A-2F1	4K x 8	200	5V ± 5%	125mA / 35mA	0 to 70	FDIP24W
	M2732AF1	4K x 8	250	5V ± 5%	125mA / 35mA	0 to 70	FDIP24W
	M2732A-3F1	4K x 8	300	5V ± 5%	125mA / 35mA	0 to 70	FDIP24W
	M2732A-4F1	4K x 8	450	5V ± 5%	125mA / 35mA	0 to 70	FDIP24W
	M2732A-20F1	4K x 8	200	5V ± 10%	125mA / 35mA	0 to 70	FDIP24W
	M2732A-25F1	4K x 8	250	5V ± 10%	125mA / 35mA	0 to 70	FDIP24W
	M2732AF6	4K x 8	250	5V ± 5%	125mA / 35mA	–40 to 85	FDIP24W
	M2732A-4F6	4K x 8	450	5V ± 5%	125mA / 35mA	–40 to 85	FDIP24W
64K	M2764A-1F1	8K x 8	180	5V ± 5%	75mA / 35mA	0 to 70	FDIP28W
	M2764A-2F1	8K x 8	200	5V ± 5%	75mA / 35mA	0 to 70	FDIP28W
	M2764AF1	8K x 8	250	5V ± 5%	75mA / 35mA	0 to 70	FDIP28W
	M2764A-3F1	8K x 8	300	5V ± 5%	75mA / 35mA	0 to 70	FDIP28W
	M2764A-4F1	8K x 8	450	5V ± 5%	75mA / 35mA	0 to 70	FDIP28W
	M2764A-20F1	8K x 8	200	5V ± 10%	75mA / 35mA	0 to 70	FDIP28W
	M2764A-25F1	8K x 8	250	5V ± 10%	75mA / 35mA	0 to 70	FDIP28W
	M2764A-2F6	8K x 8	200	5V ± 5%	75mA / 35mA	–40 to 85	FDIP28W
	M2764AF6	8K x 8	250	5V ± 5%	75mA / 35mA	–40 to 85	FDIP28W
	M2764A-4F6	8K x 8	450	5V ± 5%	75mA / 35mA	–40 to 85	FDIP28W

NMOS UV EPROM (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
128K	M27128AF1	16K x 8	250	5V ± 5%	85mA / 40mA	0 to 70	FDIP28W
	M27128A-3F1	16K x 8	300	5V ± 5%	85mA / 40mA	0 to 70	FDIP28W
	M27128A-4F1	16K x 8	450	5V ± 5%	85mA / 40mA	0 to 70	FDIP28W
	M27128A-2F1	16K x 8	200	5V ± 5%	85mA / 40mA	0 to 70	FDIP28W
	M27128A-25F1	16K x 8	250	5V ± 10%	85mA / 40mA	0 to 70	FDIP28W
	M27128AF6	16K x 8	250	5V ± 5%	85mA / 40mA	–40 to 85	FDIP28W
256K	M27256-1F1	32K x 8	170	5V ± 5%	100mA / 40mA	0 to 70	FDIP28W
	M27256-2F1	32K x 8	200	5V ± 5%	100mA / 40mA	0 to 70	FDIP28W
	M27256F1	32K x 8	250	5V ± 5%	100mA / 40mA	0 to 70	FDIP28W
	M27256-3F1	32K x 8	300	5V ± 5%	100mA / 40mA	0 to 70	FDIP28W
	M27256-4F1	32K x 8	450	5V ± 5%	100mA / 40mA	0 to 70	FDIP28W
	M27256-20F1	32K x 8	200	5V ± 10%	100mA / 40mA	0 to 70	FDIP28W
	M27256-25F1	32K x 8	250	5V ± 10%	100mA / 40mA	0 to 70	FDIP28W
	M27256F6	32K x 8	250	5V ± 5%	100mA / 40mA	–40 to 85	FDIP28W
512K	M27512-2F1	32K x 8	200	5V ± 5%	125mA / 40mA	0 to 70	FDIP28W
	M27512F1	32K x 8	250	5V ± 5%	125mA / 40mA	0 to 70	FDIP28W
	M27512-3F1	32K x 8	300	5V ± 5%	125mA / 40mA	0 to 70	FDIP28W
	M27512-20F1	32K x 8	200	5V ± 10%	125mA / 40mA	0 to 70	FDIP28W
	M27512-25F1	32K x 8	250	5V ± 10%	125mA / 40mA	0 to 70	FDIP28W
	M27512-2F6	32K x 8	200	5V ± 5%	125mA / 40mA	–40 to 85	FDIP28W
	M27512F6	32K x 8	250	5V ± 5%	125mA / 40mA	–40 to 85	FDIP28W

FLASH MEMORIES

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
256K	M28F256A-12B1	32K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	PDIP32
	M28F256-12B1	32K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	PDIP32
	M28F256A-15B1	32K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PDIP32
	M28F256-15B1	32K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PDIP32
	M28F256A-20B1	32K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	PDIP32
	M28F256-20B1	32K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	PDIP32
	M28F256A-15B6	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PDIP32
	M28F256-15B6	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PDIP32
	M28F256A-15B3	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PDIP32
	M28F256-15B3	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PDIP32
	M28F256A-12C1	32K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	PLCC32
	M28F256-12C1	32K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	PLCC32
	M28F256A-15C1	32K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PLCC32
	M28F256-15C1	32K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PLCC32
	M28F256A-20C1	32K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	PLCC32
	M28F256-20C1	32K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	PLCC32
	M28F256A-15C6	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PLCC32
	M28F256-15C6	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PLCC32
	M28F256A-15C3	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PLCC32
	M28F256-15C3	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PLCC32
512K	M28F512-12B1	64K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	PDIP32
	M28F512-15B1	64K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PDIP32
	M28F512-20B1	64K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	PDIP32

FLASH MEMORIES (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
512K	M28F512-15B6	64K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PDIP32
	M28F512-15B3	64K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PDIP32
	M28F512-12C1	64K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	PLCC32
	M28F512-15C1	64K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PLCC32
	M28F512-20C1	64K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	PLCC32
	M28F512-15C6	64K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PLCC32
	M28F512-15C3	64K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PLCC32
1M	M28F101-120P1	128K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PDIP32
	M28F101-150P1	128K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PDIP32
	M28F101-200P1	128K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PDIP32
	M28F101-150P6	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	PDIP32
	M28F101-150P3	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 125	PDIP32
	M28F101-120K1	128K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M28F101-150K1	128K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M28F101-200K1	128K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PLCC32
	M28F101-150K6	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32
	M28F101-150K3	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 125	PLCC32
	M28F101-120N1	128K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	TSOP32
	M28F101-150N1	128K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	TSOP32
	M28F101A-60N1	128K x 8	60	5V ± 10%	30mA / 100µA	0 to 70	TSOP32
	M28V101A-100N1	128K x 8	100	3.3V ± 0.3V	30mA / 100µA	0 to 70	TSOP32
	M28F101B-60N1	128K x 8	60	5V ± 10%	30mA / 100µA	0 to 70	TSOP32
	M28V101B-150N1	128K x 8	150	3.3V ± 0.3V	30mA / 100µA	0 to 70	TSOP32

FLASH MEMORIES (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stby	Temperature Range (°C)	Package
1M	M28F102-150K1	64K x 16	150	5V ± 10%	50mA / 100µA	0 to 70	PLCC44
	M28F102-150K6	64K x 16	150	5V ± 10%	50mA / 100µA	–40 to 85	PLCC44
	M28F102-150K3	64K x 16	150	5V ± 10%	50mA / 100µA	–40 to 125	PLCC44
2M	M28F201-60N1	256K x 8	60	5V ± 10%	30mA / 100µA	0 to 70	TSOP32
	M28V201-100N1	256K x 8	100	3.3V ± 0.3V	30mA / 100µA	0 to 70	TSOP32
	M28F201A-60N1	256K x 8	60	5V ± 10%	30mA / 100µA	0 to 70	TSOP32
	M28V201A-150N1	256K x 8	150	3.3V ± 0.3V	30mA / 100µA	0 to 70	TSOP32
4M	M28F410-60N1	x8 / x16, Block Er.	60	5V ± 10%	30mA / 80µA	0 to 70	TSOP56
	M28V410-150N1	x8 / x16, Block Er.	150	3V to 5.5V	30mA / 50µA	0 to 70	TSOP56
	M28F411-60N1	512K x 8, Block Er.	60	5V ± 10%	30mA / 80µA	0 to 70	TSOP40
	M28V411-150N1	512K x 8, Block Er.	150	3V to 5.5V	30mA / 50µA	0 to 70	TSOP40
8M	M28F841-85N1	1M x 8, Sector Er.	85	5V ± 10%	30mA / 30µA	0 to 70	TSOP40
	M28V841-200N1	1M x 8, Sector Er.	200	3V to 5.5V	30mA / 30µA	0 to 70	TSOP40
16M	M28F161-100N1	2M x 8, Sector Er.	100	3.3V ± 0.3V	30mA / 30µA	0 to 70	TSOP48

EEPROM, I²C and MICROWIRE Serial Access Bus

Size	Part Number	Organisation	V_{CC} min (V)	Feature	Temperature Range (°C)	Package
1K	ST24C01B1	128 x 8	4.5	Byte/Page Write	0 to 70	PSDIP8
	ST24W01B1	128 x 8	4.5	Write Control	0 to 70	PSDIP8
	ST24C01CB1	128 x 8	3.0	Byte/Page Write	0 to 70	PSDIP8
	ST24W01CB1	128 x 8	3.0	Write Control	0 to 70	PSDIP8
	ST25C01B1	128 x 8	2.5	Byte/Page Write	0 to 70	PSDIP8
	ST25C01CB1	128 x 8	2.5	Byte/Page Write	0 to 70	PSDIP8
	ST25W01CB1	128 x 8	2.5	Write Control	0 to 70	PSDIP8
	ST24C01B6	128 x 8	4.5	Byte/Page Write	–40 to 85	PSDIP8
	ST24W01B6	128 x 8	4.5	Write Control	–40 to 85	PSDIP8
	ST24C01CB6	128 x 8	3.0	Byte/Page Write	–40 to 85	PSDIP8
	ST24W01CB6	128 x 8	3.0	Write Control	–40 to 85	PSDIP8
	ST25C01B6	128 x 8	2.5	Byte/Page Write	–40 to 85	PSDIP8
	ST25C01CB6	128 x 8	2.5	Byte/Page Write	–40 to 85	PSDIP8
	ST25W01CB6	128 x 8	2.5	Write Control	–40 to 85	PSDIP8
	ST24C01M1	128 x 8	4.5	Byte/Page Write	0 to 70	SO8
	ST24C01M1013TR	128 x 8	4.5	Byte/Page Write	0 to 70	SO8TR
	ST24W01M1	128 x 8	4.5	Write Control	0 to 70	SO8
	ST24W01M1013TR	128 x 8	4.5	Write Control	0 to 70	SO8TR
	ST24C01CM1	128 x 8	3.0	Byte/Page Write	0 to 70	SO8
	ST24C01CM1TR	128 x 8	3.0	Byte/Page Write	0 to 70	SO8TR
	ST24W01CM1	128 x 8	3.0	Write Control	0 to 70	SO8
	ST24W01CM1TR	128 x 8	3.0	Write Control	0 to 70	SO8TR

EEPROM, I²C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	V_{CC} min (V)	Feature	Temperature Range (°C)	Package
1K	ST25C01CM1	128 x 8	2.5	Byte/Page Write	0 to 70	SO8
	ST25C01CM1TR	128 x 8	2.5	Byte/Page Write	0 to 70	SO8TR
	ST25C01M1	128 x 8	2.5	Byte/Page Write	0 to 70	SO8
	ST25C01M1013TR	128 x 8	2.5	Byte/Page Write	0 to 70	SO8TR
	ST25W01CM1	128 x 8	2.5	Write Control	0 to 70	SO8
	ST25W01CM1TR	128 x 8	2.5	Write Control	0 to 70	SO8TR
	ST24C01M6	128 x 8	4.5	Byte/Page Write	–40 to 85	SO8
	ST24C01M6013TR	128 x 8	4.5	Byte/Page Write	–40 to 85	SO8TR
	ST24W01M6	128 x 8	4.5	Write Control	–40 to 85	SO8
	ST24W01M6013TR	128 x 8	4.5	Write Control	–40 to 85	SO8TR
	ST24C01CM6	128 x 8	3.0	Byte/Page Write	–40 to 85	SO8
	ST24C01CM6TR	128 x 8	3.0	Byte/Page Write	–40 to 85	SO8TR
	ST24W01CM6	128 x 8	3.0	Write Control	–40 to 85	SO8
	ST24W01CM6TR	128 x 8	3.0	Write Control	–40 to 85	SO8TR
	ST25C01CM6	128 x 8	2.5	Byte/Page Write	–40 to 85	SO8
	ST25C01CM6TR	128 x 8	2.5	Byte/Page Write	–40 to 85	SO8TR
	ST25C01M6	128 x 8	2.5	Byte/Page Write	–40 to 85	SO8
	ST25C01M6013TR	128 x 8	2.5	Byte/Page Write	–40 to 85	SO8TR
	ST25W01CM6	128 x 8	2.5	Write Control	–40 to 85	SO8
	ST25W01CM6TR	128 x 8	2.5	Write Control	–40 to 85	SO8TR
	ST24C01M3	128 x 8	4.5	Byte/Page Write	–40 to 125	SO8

EEPROM, I²C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	V_{CC} min (V)	Feature	Temperature Range (°C)	Package
2K	ST24C02AB1	256 x 8	3.0	Byte/Page Write	0 to 70	PSDIP8
	ST24C02AB1/AAB	256 x 8	3.0	Content all 00	0 to 70	PSDIP8
	ST24C02CB1	256 x 8	3.0	Byte/Page Write	0 to 70	PSDIP8
	ST24W02CB1	256 x 8	3.0	Write Control	0 to 70	PSDIP8
	ST25C02AB1	256 x 8	2.5	Byte/Page Write	0 to 70	PSDIP8
	ST25C02CB1	256 x 8	2.5	Byte/Page Write	0 to 70	PSDIP8
	ST25W02CB1	256 x 8	2.5	Write Control	0 to 70	PSDIP8
	ST24C02AB6	256 x 8	3.0	Byte/Page Write	–40 to 85	PSDIP8
	ST24C02CB6	256 x 8	3.0	Byte/Page Write	–40 to 85	PSDIP8
	ST24W02CB6	256 x 8	3.0	Write Control	–40 to 85	PSDIP8
	ST25C02AB6	256 x 8	2.5	Byte/Page Write	–40 to 85	PSDIP8
	ST25C02CB6	256 x 8	2.5	Byte/Page Write	–40 to 85	PSDIP8
	ST25W02CB6	256 x 8	2.5	Write Control	–40 to 85	PSDIP8
	ST24C02CB3	256 x 8	3.0	Byte/Page Write	–40 to 125	PSDIP8
	ST25C02CB3	256 x 8	2.5	Byte/Page Write	–40 to 125	PSDIP8
	ST24C02AB3	256 x 8	3.0	Byte/Page Write	–40 to 125	PSDIP8
	ST24C02AM1	256 x 8	3.0	Byte/Page Write	0 to 70	SO8
	ST24C02AM1013TR	256 x 8	3.0	Byte/Page Write	0 to 70	SO8TR
	ST24C02CM1	256 x 8	3.0	Byte/Page Write	0 to 70	SO8
	ST24C02CM1TR	256 x 8	3.0	Byte/Page Write	0 to 70	SO8TR
	ST24W02CM1	256 x 8	3.0	Write Control	0 to 70	SO8
	ST24W02CM1TR	256 x 8	3.0	Write Control	0 to 70	SO8TR

EEPROM, I²C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	V_{CC} min (V)	Feature	Temperature Range (°C)	Package
2K	ST25C02AM1	256 x 8	2.5	Byte/Page Write	0 to 70	SO8
	ST25C02AM1013TR	256 x 8	2.5	Byte/Page Write	0 to 70	SO8TR
	ST25C02CM1	256 x 8	2.5	Byte/Page Write	0 to 70	SO8
	ST25C02CM1TR	256 x 8	2.5	Byte/Page Write	0 to 70	SO8TR
	ST25W02CM1	256 x 8	2.5	Write Control	0 to 70	SO8
	ST25W02CM1TR	256 x 8	2.5	Write Control	0 to 70	SO8TR
	ST24C02AM6	256 x 8	3.0	Byte/Page Write	–40 to 85	SO8
	ST24C02AM6013TR	256 x 8	3.0	Byte/Page Write	–40 to 85	SO8TR
	ST24C02CM6	256 x 8	3.0	Byte/Page Write	–40 to 85	SO8
	ST24C02CM6TR	256 x 8	3.0	Byte/Page Write	–40 to 85	SO8TR
	ST24W02CM6	256 x 8	3.0	Write Control	–40 to 85	SO8
	ST24W02CM6TR	256 x 8	3.0	Write Control	–40 to 85	SO8TR
	ST25C02AM6	256 x 8	2.5	Byte/Page Write	–40 to 85	SO8
	ST25C02AM6013TR	256 x 8	2.5	Byte/Page Write	–40 to 85	SO8TR
	ST25C02CM6	256 x 8	2.5	Byte/Page Write	–40 to 85	SO8
	ST25C02CM6TR	256 x 8	2.5	Byte/Page Write	–40 to 85	SO8TR
	ST25W02CM6	256 x 8	2.5	Write Control	–40 to 85	SO8
	ST25W02CM6TR	256 x 8	2.5	Write Control	–40 to 85	SO8TR
	ST24C02AM3	256 x 8	3.0	Byte/Page Write	–40 to 125	SO8
4K	ST24C04B1	512 x 8	4.5	Write Protection	0 to 70	PSDIP8
	ST24C04CB1	512 x 8	3.0	Write Protection	0 to 70	PSDIP8
	ST24W04CB1	512 x 8	3.0	Write Control	0 to 70	PSDIP8
	ST25C04B1	512 x 8	2.5	Write Protection	0 to 70	PSDIP8

EEPROM, I²C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	V_{CC} min (V)	Feature	Temperature Range (°C)	Package
4K	ST25C04CB1	512 x 8	2.5	Write Protection	0 to 70	PSDIP8
	ST25W04CB1	512 x 8	2.5	Write Control	0 to 70	PSDIP8
	ST24C04B6	512 x 8	4.5	Write Protection	–40 to 85	PSDIP8
	ST24C04CB6	512 x 8	3.0	Write Protection	–40 to 85	PSDIP8
	ST24W04CB6	512 x 8	3.0	Write Control	–40 to 85	PSDIP8
	ST25C04B6	512 x 8	2.5	Write Protection	–40 to 85	PSDIP8
	ST25C04CB6	512 x 8	2.5	Write Protection	–40 to 85	PSDIP8
	ST25W04CB6	512 x 8	2.5	Write Control	–40 to 85	PSDIP8
	ST24C04CB3	512 x 8	3.0	Write Protection	–40 to 125	PSDIP8
	ST24C04CM1	512 x 8	3.0	Write Protection	0 to 70	SO8
	ST24C04CM1TR	512 x 8	3.0	Write Protection	0 to 70	SO8TR
	ST24W04CM1	512 x 8	3.0	Write Control	0 to 70	SO8
	ST24W04CM1TR	512 x 8	3.0	Write Control	0 to 70	SO8TR
	ST25C04CM1	512 x 8	2.5	Write Protection	0 to 70	SO8
	ST25C04CM1TR	512 x 8	2.5	Write Protection	0 to 70	SO8TR
	ST25W04CM1	512 x 8	2.5	Write Control	0 to 70	SO8
	ST25W04CM1TR	512 x 8	2.5	Write Control	0 to 70	SO8TR
	ST24C04CM6	512 x 8	3.0	Write Protection	–40 to 85	SO8
	ST24C04CM6TR	512 x 8	3.0	Write Protection	–40 to 85	SO8TR
	ST24W04CM6	512 x 8	3.0	Write Control	–40 to 85	SO8
	ST24W04CM6TR	512 x 8	3.0	Write Control	–40 to 85	SO8TR
	ST25C04CM6	512 x 8	2.5	Write Protection	–40 to 85	SO8
	ST25C04CM6TR	512 x 8	2.5	Write Protection	–40 to 85	SO8TR

EEPROM, I²C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	V_{CC} min (V)	Feature	Temperature Range (°C)	Package
4K	ST25W04CM6	512 x 8	2.5	Write Control	–40 to 85	SO8
	ST25W04CM6TR	512 x 8	2.5	Write Control	–40 to 85	SO8TR
8K	ST24C08B1	1K x 8	4.5	Write Protection	0 to 70	PSDIP8
	ST24C08CB1	1K x 8	3.0	Write Protection	0 to 70	PSDIP8
	ST25C08CB1	1K x 8	2.5	Write Protection	0 to 70	PSDIP8
	ST24C08B6	1K x 8	4.5	Write Protection	–40 to 85	PSDIP8
	ST24C08CB6	1K x 8	3.0	Write Protection	–40 to 85	PSDIP8
	ST25C08CB6	1K x 8	2.5	Write Protection	–40 to 85	PSDIP8
	ST24C08CM1	1K x 8	3.0	Write Protection	0 to 70	SO8
	ST24C08CM1TR	1Kx 8	3.0	Write Protection	0 to 70	SO8TR
	ST25C08CM1	1K x 8	2.5	Write Protection	0 to 70	SO8
	ST25C08CM1TR	1Kx 8	2.5	Write Protection	0 to 70	SO8TR
	ST24C08CM6	1K x 8	3.0	Write Protection	–40 to 85	SO8
	ST24C08CM6TR	1Kx 8	3.0	Write Protection	–40 to 85	SO8TR
	ST25C08CM6	1K x 8	2.5	Write Protection	–40 to 85	SO8
	ST25C08CM6TR	1Kx 8	2.5	Write Protection	–40 to 85	SO8TR
16K	ST24C16CB1	2K x 8	3.0	Write Protection	0 to 70	PSDIP8
	ST24E16DB1	2K x 8	3.0	XI²C Bus & WC	0 to 70	PSDIP8
	ST25C16CB1	2K x 8	2.5	Write Protection	0 to 70	PSDIP8
	ST25E16DB1	2K x 8	2.5	XI²C Bus & WC	0 to 70	PSDIP8
	ST24C16CB6	2K x 8	3.0	Write Protection	–40 to 85	PSDIP8
	ST24E16DB6	2K x 8	3.0	XI²C Bus & WC	–40 to 85	PSDIP8
	ST25C16CB6	2K x 8	2.5	Write Protection	–40 to 85	PSDIP8

EEPROM, I²C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	V_{CC} min (V)	Feature	Temperature Range (°C)	Package
16K	ST25E16DB6	2K x 8	2.5	XI²C Bus & WC	–40 to 85	PSDIP8
	ST24C16CB3	2K x 8	3.0	Write Protection	–40 to 125	PSDIP8
	ST24C16CM1	2K x 8	3.0	Write Protection	0 to 70	SO8
	ST24C16CM1TR	2K x 8	3.0	Write Protection	0 to 70	SO8TR
	ST24C16DM1	2K x 8	3.0	Write Protection	0 to 70	SO8
	ST24C16DM1TR	2K x 8	3.0	Write Protection	0 to 70	SO8TR
	ST24E16DM1	2K x 8	3.0	XI²C Bus & WC	0 to 70	SO8
	ST24E16DM1TR	2K x 8	3.0	XI²C Bus & WC	0 to 70	SO8TR
	ST25C16DM1	2K x 8	2.5	Write Protection	0 to 70	SO8
	ST25C16DM1TR	2K x 8	2.5	Write Protection	0 to 70	SO8TR
	ST25E16DM1	2K x 8	2.5	XI²C Bus & WC	0 to 70	SO8
	ST25E16DM1TR	2K x 8	2.5	XI²C Bus & WC	0 to 70	SO8TR
	ST24C16DM6	2K x 8	3.0	Write Protection	–40 to 85	SO8
	ST24C16DM6TR	2K x 8	3.0	Write Protection	–40 to 85	SO8TR
	ST24E16DM6	2K x 8	3.0	XI²C Bus & WC	–40 to 85	SO8
	ST24E16DM6TR	2K x 8	3.0	XI²C Bus & WC	–40 to 85	SO8TR
	ST25C16DM6	2K x 8	2.5	Write Protection	–40 to 85	SO8
	ST25C16DM6TR	2K x 8	2.5	Write Protection	–40 to 85	SO8TR
	ST25E16DM6	2K x 8	2.5	XI²C Bus & WC	–40 to 85	SO8
	ST25E16DM6TR	2K x 8	2.5	XI²C Bus & WC	–40 to 85	SO8TR
	ST24C16CML1	2K x 8	3.0	Write Protection	0 to 70	SO14
	ST24C16CML1TR	2K x 8	3.0	Write Protection	0 to 70	SO14TR
	ST25C16CML1	2K x 8	2.5	Write Protection	0 to 70	SO14

EEPROM, I²C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	V_{CC} min (V)	Feature	Temperature Range (°C)	Package
16K	ST25C16CML1TR	2K x 8	2.5	Write Protection	0 to 70	SO14TR
	ST24C16CML6	2K x 8	3.0	Write Protection	–40 to 85	SO14
	ST24C16CML6TR	2K x 8	3.0	Write Protection	–40 to 85	SO14TR
	ST25C16CML6	2K x 8	2.5	Write Protection	–40 to 85	SO14
	ST25C16CML6TR	2K x 8	2.5	Write Protection	–40 to 85	SO14TR
256	ST93C06CB1	32x8 or 16x16	3.0	Dual Org, 1MHz	0 to 70	PSDIP8
	ST93C06B1	32x8 or 16x16	4.5	Dual Org, 1MHz	0 to 70	PSDIP8
	ST93C06CB6	32x8 or 16x16	3.0	Dual Org, 1MHz	–40 to 85	PSDIP8
	ST93C06B6	32x8 or 16x16	4.5	Dual Org, 1MHz	–40 to 85	PSDIP8
	ST93C06CB3	32x8 or 16x16	3.0	Dual Org, 1MHz	–40 to 125	PSDIP8
	ST93C06B3	32x8 or 16x16	4.5	Dual Org, 1MHz	–40 to 125	PSDIP8
	ST93C06CM1	32x8 or 16x16	3.0	Dual Org, 1MHz	0 to 70	SO8
	ST93C06CM1TR	32x8 or 16x16	3.0	Dual Org, 1MHz	0 to 70	SO8TR
	ST93C06M1	32x8 or 16x16	4.5	Dual Org, 1MHz	0 to 70	SO8
	ST93C06M1013TR	32x8 or 16x16	4.5	Dual Org, 1MHz	0 to 70	SO8TR
	ST93C06CM6	32x8 or 16x16	3.0	Dual Org, 1MHz	–40 to 85	SO8
	ST93C06CM6TR	32x8 or 16x16	3.0	Dual Org, 1MHz	–40 to 85	SO8TR
	ST93C06M6	32x8 or 16x16	4.5	Dual Org, 1MHz	–40 to 85	SO8
	ST93C06M6013TR	32x8 or 16x16	4.5	Dual Org, 1MHz	–40 to 85	SO8TR
	ST93C06CM3	32x8 or 16x16	3.0	Dual Org, 1MHz	–40 to 125	SO8
	ST93C06CM3TR	32x8 or 16x16	3.0	Dual Org, 1MHz	–40 to 125	SO8TR
	ST93C06M3	32x8 or 16x16	4.5	Dual Org, 1MHz	–40 to 125	SO8

EEPROM, I²C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	V_{CC} min (V)	Feature	Temperature Range (°C)	Package
1K	ST93CS46B1	64 x 16	4.5	Write Protection	0 to 70	PSDIP8
	ST93CS47B1	64 x 16	2.5	Write Protection	0 to 70	PSDIP8
	ST93CS46B6	64 x 16	4.5	Write Protection	–40 to 85	PSDIP8
	ST93CS47B6	64 x 16	2.5	Write Protection	–40 to 85	PSDIP8
	ST93CS46B3	64 x 16	4.5	Write Protection	–40 to 125	PSDIP8
	ST93CS46M1	64 x 16	4.5	Write Protection	0 to 70	SO8
	ST93CS47M1	64 x 16	2.5	Write Protection	0 to 70	SO8
	ST93CS46M6	64 x 16	4.5	Write Protection	–40 to 85	SO8
	ST93CS47M6	64 x 16	2.5	Write Protection	–40 to 85	SO8
	ST93CS46M3	64 x 16	4.5	Write Protection	–40 to 125	SO8
	ST93C46AB1	128x8 or 64x16	4.5	Dual Org, 1MHz	0 to 70	PSDIP8
	ST93C46CB1	128x8 or 64x16	3.0	Dual Org, 1MHz	0 to 70	PSDIP8
	ST93C46AB6	128x8 or 64x16	4.5	Dual Org, 1MHz	–40 to 85	PSDIP8
	ST93C46CB6	128x8 or 64x16	3.0	Dual Org, 1MHz	–40 to 85	PSDIP8
	ST93C46AB3	128x8 or 64x16	4.5	Dual Org, 1MHz	–40 to 125	PSDIP8
	ST93C46CB3	128x8 or 64x16	3.0	Dual Org, 1MHz	–40 to 125	PSDIP8
	ST93C46AM1	128x8 or 64x16	4.5	Dual Org, 1MHz	0 to 70	SO8
	ST93C46AM1013TR	128x8 or 64x16	4.5	Dual Org, 1MHz	0 to 70	SO8TR
	ST93C46TM1	128x8 or 64x16	4.5	90 Turn Pinout	0 to 70	SO8
	ST93C46TM1013TR	128x8 or 64x16	4.5	90 Turn Pinout	0 to 70	SO8TR
	ST93C46CM1	128x8 or 64x16	3.0	Dual Org, 1MHz	0 to 70	SO8
	ST93C46CM1TR	128x8 or 64x16	3.0	Dual Org, 1MHz	0 to 70	SO8TR
	ST93C46AM6	128x8 or 64x16	4.5	Dual Org, 1MHz	–40 to 85	SO8

EEPROM, I²C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	V_{CC} min (V)	Feature	Temperature Range (°C)	Package
1K	ST93C46AM6013TR	128x8 or 64x16	4.5	Dual Org, 1MHz	–40 to 85	SO8TR
	ST93C46TM6	128x8 or 64x16	4.5	90 Turn Pinout	–40 to 85	SO8
	ST93C46TM6013TR	128x8 or 64x16	4.5	90 Turn Pinout	–40 to 85	SO8TR
	ST93C46CM6	128x8 or 64x16	3.0	Dual Org, 1MHz	–40 to 85	SO8
	ST93C46CM6TR	128x8 or 64x16	3.0	Dual Org, 1MHz	–40 to 85	SO8TR
	ST93C46AM3	128x8 or 64x16	4.5	Dual Org, 1MHz	–40 to 125	SO8
	ST93C46AM3013TR	128x8 or 64x16	4.5	Dual Org, 1MHz	–40 to 125	SO8TR
	ST93C46TM3	128x8 or 64x16	4.5	90 Turn Pinout	–40 to 125	SO8
	ST93C46TM3013TR	128x8 or 64x16	4.5	90 Turn Pinout	–40 to 125	SO8TR
	ST93C46CM3	128x8 or 64x16	3.0	Dual Org, 1MHz	–40 to 125	SO8
	ST93C46CM3TR	128x8 or 64x16	3.0	Dual Org, 1MHz	–40 to 125	SO8TR
2K	ST93CS56B1	128 x 16	4.5	Write Protection	0 to 70	PSDIP8
	ST93CS57B1	128 x 16	2.5	Write Protection	0 to 70	PSDIP8
	ST93CS56B6	128 x 16	4.5	Write Protection	–40 to 85	PSDIP8
	ST93CS57B6	128 x 16	2.5	Write Protection	–40 to 85	PSDIP8
	ST93CS56B3	128 x 16	4.5	Write Protection	–40 to 125	PSDIP8
	ST93CS56M1	128 x 16	4.5	Write Protection	0 to 70	SO8
	ST93CS56M1013TR	128 x 16	4.5	Write Protection	0 to 70	SO8TR
	ST93CS57M1	128 x 16	2.5	Write Protection	0 to 70	SO8
	ST93CS57M1013TR	128 x 16	2.5	Write Protection	0 to 70	SO8TR
	ST93CS56M6	128 x 16	4.5	Write Protection	–40 to 85	SO8
	ST93CS56M6013TR	128 x 16	4.5	Write Protection	–40 to 85	SO8TR

EEPROM, I²C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	V_{CC} min (V)	Feature	Temperature Range (°C)	Package
2K	ST93CS57M6	128 x 16	2.5	Write Protection	–40 to 85	SO8
	ST93CS57M6013TR	128 x 16	2.5	Write Protection	–40 to 85	SO8TR
	ST93CS56M3	128 x 16	4.5	Write Protection	–40 to 125	SO8
	ST93C56B1	256x8 or 128x16	4.5	Dual Org, 1MHz	0 to 70	PSDIP8
	ST93C56B6	256x8 or 128x16	4.5	Dual Org, 1MHz	–40 to 85	PSDIP8
	ST93C56B3	256x8 or 128x16	4.5	Dual Org, 1MHz	–40 to 125	PSDIP8
	ST93C56M1	256x8 or 128x16	4.5	Dual Org, 1MHz	0 to 70	SO8
	ST93C56M1013TR	256x8 or 128x16	4.5	Dual Org, 1MHz	0 to 70	SO8TR
	ST93C56M6	256x8 or 128x16	4.5	Dual Org, 1MHz	–40 to 85	SO8
	ST93C56M3	256x8 or 128x16	4.5	Dual Org, 1MHz	–40 to 125	SO8
4K	ST93CS66B1	256 x 16	4.5	Write Protection	0 to 70	PSDIP8
	ST93CS67B1	256 x 16	2.5	Write Protection	0 to 70	PSDIP8
	ST93CS66B6	256 x 16	4.5	Write Protection	–40 to 85	PSDIP8
	ST93CS67B6	256 x 16	2.5	Write Protection	–40 to 85	PSDIP8
	ST93CS66B3	256 x 16	4.5	Write Protection	–40 to 125	PSDIP8
	ST93CS66ML1	256 x 16	4.5	Write Protection	0 to 70	SO14
	ST93CS67ML1	256 x 16	2.5	Write Protection	0 to 70	SO14
	ST93CS66ML1013TR	256 x 16	4.5	Write Protection	0 to 70	SO14TR
	ST93CS66ML6	256 x 16	4.5	Write Protection	–40 to 85	SO14
	ST93CS67ML6	256 x 16	2.5	Write Protection	–40 to 85	SO14
	ST93CS66ML6TR	256 x 16	4.5	Write Protection	–40 to 85	SO14TR
	ST93CS66ML3	256 x 16	4.5	Write Protection	–40 to 125	SO14
	ST93CS66ML3TR	256 x 16	4.5	Write Protection	–40 to 125	SO14TR

EEPROM, Parallel Access Bus

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} min (V)	I_{CC} / Stby	Temperature Range (°C)	Package
64K	M28C64C-150P1	8K x 8	150	4.5	30mA / 100µA	0 to 70	PDIP28
	M28C64C-200P1	8K x 8	200	4.5	30mA / 100µA	0 to 70	PDIP28
	M28C64C-150P6	8K x 8	150	4.5	30mA / 100µA	–40 to 85	PDIP28
	M28C64C-200P6	8K x 8	200	4.5	30mA / 100µA	–40 to 85	PDIP28
	M28C64C-150K1	8K x 8	150	4.5	30mA / 100µA	0 to 70	PLCC32
	M28C64C-200K1	8K x 8	200	4.5	30mA / 100µA	0 to 70	PLCC32
	M28C64C-150K6	8K x 8	150	4.5	30mA / 100µA	–40 to 85	PLCC32
	M28C64C-200K6	8K x 8	200	4.5	30mA / 100µA	–40 to 85	PLCC32
	M28C64C-150M1	8K x 8	150	4.5	30mA / 100µA	0 to 70	SO28
	M28C64C-200M1	8K x 8	200	4.5	30mA / 100µA	0 to 70	SO28
	M28C64C-150M6	8K x 8	150	4.5	30mA / 100µA	–40 to 85	SO28
	M28C64C-200M6	8K x 8	200	4.5	30mA / 100µA	–40 to 85	SO28

FAST SRAM

Size	Part Number	Organisation	t_{ACC} (ns)	I_{CC} / Stby	Features	Package
256K	M624064-12PS1	64K x 4	12	160mA / 1mA	Common I/O	PSDIP24
	M624064-15PS1	64K x 4	15	160mA / 1mA	Common I/O	PSDIP24
	M624064-20PS1	64K x 4	20	160mA / 1mA	Common I/O	PSDIP24
	M624065-12PS1	64K x 4	12	160mA / 1mA	With Output Enable	PSDIP28
	M624065-15PS1	64K x 4	15	160mA / 1mA	With Output Enable	PSDIP28
	M624065-20PS1	64K x 4	20	160mA / 1mA	With Output Enable	PSDIP28
	M624064-12E1	64K x 4	12	160mA / 1mA	Common I/O	SOJ24
	M624064-12E1TR	64K x 4	12	160mA / 1mA	Common I/O	SOJ24TR
	M624064-15E1	64K x 4	15	160mA / 1mA	Common I/O	SOJ24
	M624064-15E1TR	64K x 4	15	160mA / 1mA	Common I/O	SOJ24TR
	M624064-20E1	64K x 4	20	160mA / 1mA	Common I/O	SOJ24
	M624064-20E1TR	64K x 4	20	160mA / 1mA	Common I/O	SOJ24TR
	M624065-12E1	64K x 4	12	160mA / 1mA	With Output Enable	SOJ28
	M624065-12E1TR	64K x 4	12	160mA / 1mA	With Output Enable	SOJ28TR
	M624065-15E1	64K x 4	15	160mA / 1mA	With Output Enable	SOJ28
	M624065-15E1TR	64K x 4	15	160mA / 1mA	With Output Enable	SOJ28TR
	M624065-20E1	64K x 4	20	160mA / 1mA	With Output Enable	SOJ28
	M624065-20E1TR	64K x 4	20	160mA / 1mA	With Output Enable	SOJ28TR
	M628032-12PS1	32K x 8	12	160mA / 1mA	With Output Enable	PSDIP28
	M628032-15PS1	32K x 8	15	160mA / 1mA	With Output Enable	PSDIP28
	M628032-20PS1	32K x 8	20	160mA / 1mA	With Output Enable	PSDIP28
	M628032-12E1	32K x 8	12	160mA / 1mA	With Output Enable	SOJ28
	M628032-12E1TR	32K x 8	12	160mA / 1mA	With Output Enable	SOJ28TR

FAST SRAM (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	I_{CC} / Stby	Features	Package
256K	M628032-15E1	32K x 8	15	160mA / 1mA	With Output Enable	SOJ28
	M628032-15E1TR	32K x 8	15	160mA / 1mA	With Output Enable	SOJ28TR
	M628032-20E1	32K x 8	20	160mA / 1mA	With Output Enable	SOJ28
	M628032-20E1TR	32K x 8	20	160mA / 1mA	With Output Enable	SOJ28TR
1M	M624256-15E1	256K x 4	15	175mA / 1mA	With Output Enable	SOJ28
	M624256-15E1TR	256K x 4	15	175mA / 1mA	With Output Enable	SOJ28TR
	M624256-17E1	256K x 4	17	175mA / 1mA	With Output Enable	SOJ28
	M624256-17E1TR	256K x 4	17	175mA / 1mA	With Output Enable	SOJ28TR
	M624256-20E1	256K x 4	20	140mA / 1mA	With Output Enable	SOJ28
	M624256-20E1TR	256K x 4	20	140mA / 1mA	With Output Enable	SOJ28TR
	M624256-25E1	256K x 4	25	130mA / 1mA	With Output Enable	SOJ28
	M624256-25E1TR	256K x 4	25	130mA / 1mA	With Output Enable	SOJ28TR
	M628128-15E1	128K x 8	15	175mA / 1mA	With Output Enable	SOJ32
	M628128-15E1TR	128K x 8	15	175mA / 1mA	With Output Enable	SOJ32TR
	M628128-17E1	128K x 8	17	175mA / 1mA	With Output Enable	SOJ32
	M628128-17E1TR	128K x 8	17	175mA / 1mA	With Output Enable	SOJ32TR
	M628128-20E1	128K x 8	20	140mA / 4mA	With Output Enable	SOJ32
	M628128-20E1TR	128K x 8	20	140mA / 4mA	With Output Enable	SOJ32TR
	M628128-25E1	128K x 8	25	130mA / 4mA	With Output Enable	SOJ32
	M628128-25E1TR	128K x 8	25	130mA / 4mA	With Output Enable	SOJ32TR

CACHE MEMORIES

Part Number	Organisation	t_{ACC} (ns)	Description	Package
MK41S80X10	4K x 4	10	Very Fast TAGRAM	SOJ24
MK41S80X10TR	4K x 4	10	Very Fast TAGRAM	SOJ24TR
MK41S80N12	4K x 4	12	Very Fast TAGRAM	PSDIP22
MK41S80X12	4K x 4	12	Very Fast TAGRAM	SOJ24
MK41S80X12TR	4K x 4	12	Very Fast TAGRAM	SOJ24TR
MK41S80N15	4K x 4	15	Very Fast TAGRAM	PSDIP22
MK41S80X15	4K x 4	15	Very Fast TAGRAM	SOJ24
MK41S80X15TR	4K x 4	15	Very Fast TAGRAM	SOJ24TR
MK41S80N20	4K x 4	20	Very Fast TAGRAM	PSDIP22
MK41S80X20	4K x 4	20	Very Fast TAGRAM	SOJ24
MK41S80X20TR	4K x 4	20	Very Fast TAGRAM	SOJ24TR
MK41S80N25	4K x 4	25	Very Fast TAGRAM	PSDIP22
MK41S80X25	4K x 4	25	Very Fast TAGRAM	SOJ24
MK41S80X25TR	4K x 4	25	Very Fast TAGRAM	SOJ24TR
MK48S80N17	8K x 8	17	Very Fast TAGRAM	PSDIP28
MK48S80X17	8K x 8	17	Very Fast TAGRAM	SOJ28
MK48S80X17TR	8K x 8	17	Very Fast TAGRAM	SOJ28TR
MK48S74N20	8K x 8	20	Very Fast TAGRAM	PSDIP28
MK48S80N20	8K x 8	20	Very Fast TAGRAM	PSDIP28
MK48S74X20	8K x 8	20	Very Fast TAGRAM	SOJ28
MK48S74X20TR	8K x 8	20	Very Fast TAGRAM	SOJ28TR
MK48S80X20	8K x 8	20	Very Fast TAGRAM	SOJ28
MK48S80X20TR	8K x 8	20	Very Fast TAGRAM	SOJ28TR

CACHE MEMORIES (cont'd)

Part Number	Organisation	t_{ACC} (ns)	Description	Package
MK48S74N25	8K x 8	25	Very Fast TAGRAM	PSDIP28
MK48S80N25	8K x 8	25	Very Fast TAGRAM	PSDIP28
MK48S74X25	8K x 8	25	Very Fast TAGRAM	SOJ28
MK48S74X25TR	8K x 8	25	Very Fast TAGRAM	SOJ28TR
MK48S80X25	8K x 8	25	Very Fast TAGRAM	SOJ28
MK48S80X25TR	8K x 8	25	Very Fast TAGRAM	SOJ28TR
M62486ARQ8TR	32K x 9	8	Burst SRAM	PLCC44TR
M62486ARQ9TR	32K x 9	9	Burst SRAM	PLCC44TR
M62486RQ8	32K x 9	8	Burst SRAM	PLCC44
M62486RQ9	32K x 9	9	Burst SRAM	PLCC44
M62486AQ11	32K x 9	11	Burst SRAM	PLCC44
M62486AQ11TR	32K x 9	11	Burst SRAM	PLCC44TR
M62486AQ12	32K x 9	12	Burst SRAM	PLCC44
M62486AQ12TR	32K x 9	12	Burst SRAM	PLCC44TR
M62486AQ14	32K x 9	14	Burst SRAM	PLCC44
M62486AQ14TR	32K x 9	14	Burst SRAM	PLCC44TR
MK62486Q19	32K x 9	19	Burst SRAM	PLCC44
MK62486Q19TR	32K x 9	19	Burst SRAM	PLCC44TR
MK62486Q24	32K x 9	24	Burst SRAM	PLCC44
MK62486Q24TR	32K x 9	24	Burst SRAM	PLCC44TR
MK4202Q17	2K x 20	17	Very Fast TAGRAM	PLCC68
MK4202Q20	2K x 20	20	Very Fast TAGRAM	PLCC68
MK4202Q25	2K x 20	25	Very Fast TAGRAM	PLCC68

BiPORT FIFO

Part Number	Organisation	t_{ACC} (ns)	Description	Package
MK4505MN25	1K x 5	25	Master FIFO	PSDIP24
MK4505MN33	1K x 5	33	Master FIFO	PSDIP24
MK4505MN50	1K x 5	50	Master FIFO	PSDIP24
MK4505SN25	1K x 5	25	Slave FIFO	PSDIP20
MK4505SN33	1K x 5	33	Slave FIFO	PSDIP20
MK4505SN50	1K x 5	50	Slave FIFO	PSDIP20
MK45H01N25	512 x 9	25	Very Fast FIFO	PDIP28
MK45H01N35	512 x 9	35	Very Fast FIFO	PDIP28
MK45H01N50	512 x 9	50	Very Fast FIFO	PDIP28
MK45H01N12	512 x 9	120	Very Fast FIFO	PDIP28
MK45H11N25	512 x 9	25	Very Fast FIFO	PSDIP28
MK45H11N35	512 x 9	35	Very Fast FIFO	PSDIP28
MK45H11N50	512 x 9	50	Very Fast FIFO	PSDIP28
MK45H11N12	512 x 9	120	Very Fast FIFO	PSDIP28
MK45H01K25	512 x 9	25	Very Fast FIFO	PLCC32
MK45H01K25TR	512 x 9	25	Very Fast FIFO	PLCC32TR
MK45H01K35	512 x 9	35	Very Fast FIFO	PLCC32
MK45H01K35TR	512 x 9	35	Very Fast FIFO	PLCC32TR
MK45H01K50	512 x 9	50	Very Fast FIFO	PLCC32
MK45H01K50TR	512 x 9	50	Very Fast FIFO	PLCC32TR
MK45H01K12	512 x 9	120	Very Fast FIFO	PLCC32
MK45H01K12TR	512 x 9	120	Very Fast FIFO	PLCC32TR

BiPORT FIFO (cont'd)

Part Number	Organisation	t_{ACC} (ns)	Description	Package
MK4501N80	512 x 9	80	Fast FIFO	PDIP28
MK4501N10	512 x 9	100	Fast FIFO	PDIP28
MK4501N12	512 x 9	120	Fast FIFO	PDIP28
MK4501N15	512 x 9	150	Fast FIFO	PDIP28
MK4501N20	512 x 9	200	Fast FIFO	PDIP28
MK4501K80	512 x 9	80	Fast FIFO	PLCC32
MK4501K80TR	512 x 9	80	Fast FIFO	PLCC32TR
MK4501K10	512 x 9	100	Fast FIFO	PLCC32
MK4501K10TR	512 x 9	100	Fast FIFO	PLCC32TR
MK4501K12	512 x 9	120	Fast FIFO	PLCC32
MK4501K12TR	512 x 9	120	Fast FIFO	PLCC32TR
MK4501K15	512 x 9	150	Fast FIFO	PLCC32
MK4501K15TR	512 x 9	150	Fast FIFO	PLCC32TR
MK4501K20	512 x 9	200	Fast FIFO	PLCC32
MK4501K20TR	512 x 9	200	Fast FIFO	PLCC32TR
MK45H02N25	1K x 9	25	Very Fast FIFO	PDIP28
MK45H02N35	1K x 9	35	Very Fast FIFO	PDIP28
MK45H02N50	1K x 9	50	Very Fast FIFO	PDIP28
MK45H02N12	1K x 9	120	Very Fast FIFO	PDIP28
MK45H12N25	1K x 9	25	Very Fast FIFO	PSDIP28
MK45H12N35	1K x 9	35	Very Fast FIFO	PSDIP28
MK45H12N50	1K x 9	50	Very Fast FIFO	PSDIP28
MK45H12N12	1K x 9	120	Very Fast FIFO	PSDIP28

BiPORT FIFO (cont'd)

Part Number	Organisation	t_{ACC} (ns)	Description	Package
MK45H02K25	1K x 9	25	Very Fast FIFO	PLCC32
MK45H02K25TR	1K x 9	25	Very Fast FIFO	PLCC32TR
MK45H02K35	1K x 9	35	Very Fast FIFO	PLCC32
MK45H02K35TR	1K x 9	35	Very Fast FIFO	PLCC32TR
MK45H02K50	1K x 9	50	Very Fast FIFO	PLCC32
MK45H02K50TR	1K x 9	50	Very Fast FIFO	PLCC32TR
MK45H02K12	1K x 9	120	Very Fast FIFO	PLCC32
MK45H02K12TR	1K x 9	120	Very Fast FIFO	PLCC32TR
MK45H03N25	2K x 9	25	Very Fast FIFO	PDIP28
MK45H03N35	2K x 9	35	Very Fast FIFO	PDIP28
MK45H03N50	2K x 9	50	Very Fast FIFO	PDIP28
MK45H03N12	2K x 9	120	Very Fast FIFO	PDIP28
MK45H13N25	2K x 9	25	Very Fast FIFO	PSDIP28
MK45H13N35	2K x 9	35	Very Fast FIFO	PSDIP28
MK45H13N50	2K x 9	50	Very Fast FIFO	PSDIP28
MK45H13N12	2K x 9	120	Very Fast FIFO	PSDIP28
MK45H03K25	2K x 9	25	Very Fast FIFO	PLCC32
MK45H03K25TR	2K x 9	25	Very Fast FIFO	PLCC32TR
MK45H03K35	2K x 9	35	Very Fast FIFO	PLCC32
MK45H03K35TR	2K x 9	35	Very Fast FIFO	PLCC32TR
MK45H03K50	2K x 9	50	Very Fast FIFO	PLCC32
MK45H03K50TR	2K x 9	50	Very Fast FIFO	PLCC32TR
MK45H03K12	2K x 9	120	Very Fast FIFO	PLCC32

BiPORT FIFO (cont'd)

Part Number	Organisation	t_{ACC} (ns)	Description	Package
MK45H03K12TR	2K x 9	120	Very Fast FIFO	PLCC32TR
MK4503N80	2K x 9	80	Fast FIFO	PDIP28
MK4503N10	2K x 9	100	Fast FIFO	PDIP28
MK4503N12	2K x 9	120	Fast FIFO	PDIP28
MK4503N15	2K x 9	150	Fast FIFO	PDIP28
MK4503N20	2K x 9	200	Fast FIFO	PDIP28
MK45H04N25	4K x 9	25	Very Fast FIFO	PDIP28
MK45H04N35	4K x 9	35	Very Fast FIFO	PDIP28
MK45H04N50	4K x 9	50	Very Fast FIFO	PDIP28
MK45H04N12	4K x 9	120	Very Fast FIFO	PDIP28
MK45H14N25	4K x 9	25	Very Fast FIFO	PSDIP28
MK45H14N35	4K x 9	35	Very Fast FIFO	PSDIP28
MK45H14N50	4K x 9	50	Very Fast FIFO	PSDIP28
MK45H14N12	4K x 9	120	Very Fast FIFO	PSDIP28
MK45H04K25	4K x 9	25	Very Fast FIFO	PLCC32
MK45H04K25TR	4K x 9	25	Very Fast FIFO	PLCC32TR
MK45H04K35	4K x 9	35	Very Fast FIFO	PLCC32
MK45H04K35TR	4K x 9	35	Very Fast FIFO	PLCC32TR
MK45H04K50	4K x 9	50	Very Fast FIFO	PLCC32
MK45H04K50TR	4K x 9	50	Very Fast FIFO	PLCC32TR
MK45H04K12	4K x 9	120	Very Fast FIFO	PLCC32
MK45H04K12TR	4K x 9	120	Very Fast FIFO	PLCC32TR

BiPORT FIFO (cont'd)

Part Number	Organisation	t_{ACC} (ns)	Description	Package
MK45H08N25	8K x 9	25	Very Fast FIFO	PDIP28
MK45H08N35	8K x 9	35	Very Fast FIFO	PDIP28
MK45H08N50	8K x 9	50	Very Fast FIFO	PDIP28
MK45H08N12	8K x 9	120	Very Fast FIFO	PDIP28

ZEROPOWER and TIMEKEEPER

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	Temperature Range (°C)	Package
16K	MK48C02AN15	2K x 8	150	5V +10/-5%	0 to 70	PDIP28
	MK48C02AK15	2K x 8	150	5V +10/-5%	0 to 70	PLCC32
	MK48Z02B12	2K x 8	120	5V +10/-5%	0 to 70	PHDIP24
	MK48Z02B15	2K x 8	150	5V +10/-5%	0 to 70	PHDIP24
	MK48Z02B20	2K x 8	200	5V +10/-5%	0 to 70	PHDIP24
	MK48Z02B25	2K x 8	250	5V +10/-5%	0 to 70	PHDIP24
	MK48Z12B15	2K x 8	150	5V ± 10%	0 to 70	PHDIP24
	MK48Z12B20	2K x 8	200	5V ± 10%	0 to 70	PHDIP24
	MK48Z12B25	2K x 8	250	5V ± 10%	0 to 70	PHDIP24
	MKI48Z02B15	2K x 8	150	5V +10/-5%	–40 to 85	PHDIP24
	MKI48Z02B20	2K x 8	200	5V +10/-5%	–40 to 85	PHDIP24

ZEROPOWER and TIMEKEEPER (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	Temperature Range (°C)	Package
16K	MKI48Z02B25	2K x 8	250	5V +10/-5%	–40 to 85	PHDIP24
	MKI48Z12B15	2K x 8	150	5V ± 10%	–40 to 85	PHDIP24
	MKI48Z12B20	2K x 8	200	5V ± 10%	–40 to 85	PHDIP24
	MKI48Z12B25	2K x 8	250	5V ± 10%	–40 to 85	PHDIP24
	M48Z02-150PC1	2K x 8	150	5V +10/-5%	0 to 70	PCDIP24
	M48Z12-150PC1	2K x 8	150	5V ± 10%	0 to 70	PCDIP24
64K	MK48Z08B10	8K x 8	100	5V +10/-5%	0 to 70	PHDIP28
	MK48Z09B10	8K x 8	100	5V +10/-5%	0 to 70	PHDIP28
	MK48Z18B10	8K x 8	100	5V ± 10%	0 to 70	PHDIP28
	MK48Z19B10	8K x 8	100	5V ± 10%	0 to 70	PHDIP28
	MKI48Z18B10	8K x 8	100	5V ± 10%	–40 to 85	PHDIP28
	M48Z08-100PC1	8K x 8	100	5V +10/-5%	0 to 70	PCDIP28
	M48Z09-100PC1	8K x 8	100	5V +10/-5%	0 to 70	PCDIP28
	M48Z18-100PC1	8K x 8	100	5V ± 10%	0 to 70	PCDIP28
	M48Z19-100PC1	8K x 8	100	5V ± 10%	0 to 70	PCDIP28
	M48Z18-100MH1	8K x 8	100	5V ± 10%	0 to 70	SOH28
256K	M48Z30Y-85PM1	32K x 8	85	5V ± 10%	0 to 70	PMDIP28
	M48Z30Y-100PM1	32K x 8	100	5V ± 10%	0 to 70	PMDIP28
	M48Z30-85PM1	32K x 8	85	5V +10/-5%	0 to 70	PMDIP28
	M48Z30-100PM1	32K x 8	100	5V +10/-5%	0 to 70	PMDIP28
	M48Z32-85PC1	32K x 8	85	5V +10/-5%	0 to 70	PCDIP28
	M48Z32-100PC1	32K x 8	100	5V +10/-5%	0 to 70	PCDIP28

ZEROPOWER and TIMEKEEPER (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	Temperature Range (°C)	Package
256K	M48Z32Y-85PC1	32K x 8	85	5V ± 10%	0 to 70	PCDIP28
	M48Z32Y-100PC1	32K x 8	100	5V ± 10%	0 to 70	PCDIP28
1M	M48Z128Y-85PM1	128K x 8	85	5V ± 10%	0 to 70	PMDIP32
	M48Z128Y-120PM1	128K x 8	120	5V ± 10%	0 to 70	PMDIP32
	M48Z128-85PM1	128K x 8	85	5V +10/-5%	0 to 70	PMDIP32
	M48Z128-120PM1	128K x 8	120	5V +10/-5%	0 to 70	PMDIP32
2M	M46Z128Y-85PM1	128K x 16	85	5V ± 10%	0 to 70	PMDIP40
	M46Z128Y-120PM1	128K x 16	120	5V ± 10%	0 to 70	PMDIP40
	M46Z128-85PM1	128K x 16	85	5V +10/-5%	0 to 70	PMDIP40
	M46Z128-120PM1	128K x 16	120	5V +10/-5%	0 to 70	PMDIP40
	M48Z256Y-85PL1	256K x 8	85	5V ± 10%	0 to 70	PMLDIP32
	M48Z256Y-120PL1	256K x 8	120	5V ± 10%	0 to 70	PMLDIP32
	M48Z256-85PL1	256K x 8	85	5V +10/-5%	0 to 70	PMLDIP32
	M48Z256-120PL1	256K x 8	120	5V +10/-5%	0 to 70	PMLDIP32
4M	M46Z256Y-85PM1	256K x 16	85	5V ± 10%	0 to 70	PMDIP40
	M46Z256Y-120PM1	256K x 16	120	5V ± 10%	0 to 70	PMDIP40
	M46Z256-85PM1	256K x 16	85	5V +10/-5%	0 to 70	PMDIP40
	M46Z256-120PM1	256K x 16	120	5V +10/-5%	0 to 70	PMDIP40
	M48Z512Y-85PL1	512K x 8	85	5V ± 10%	0 to 70	PMLDIP32
	M48Z512Y-120PL1	512K x 8	120	5V ± 10%	0 to 70	PMLDIP32
	M48Z512-85PL1	512K x 8	85	5V +10/-5%	0 to 70	PMLDIP32
	M48Z512-120PL1	512K x 8	120	5V +10/-5%	0 to 70	PMLDIP32

ZEROPOWER and TIMEKEEPER (cont'd)

Size	Part Number	Organisation	t_{ACC} (ns)	V_{CC} Range	Temperature Range (°C)	Package
512	MK41T56N00	64 x 8	-	5V ± 10%	0 to 70	PSDIP8
	MK41T56S00	64 x 8	-	5V ± 10%	0 to 70	SO8
	MKI41T56S00	64 x 8	-	5V ± 10%	–40 to 85	SO8
	MKI41T56S00TR	64 x 8	-	5V ± 10%	–40 to 85	SO8TR
	MK48T87B24	64 x 8	-	5V ± 10%	0 to 70	PHDIP24
16K	MK48T02B12	2K x 8	120	5V +10/-5%	0 to 70	PHDIP24
	MK48T02B15	2K x 8	150	5V +10/-5%	0 to 70	PHDIP24
	MK48T02B20	2K x 8	200	5V +10/-5%	0 to 70	PHDIP24
	MK48T02B25	2K x 8	250	5V +10/-5%	0 to 70	PHDIP24
	MK48T12B15	2K x 8	150	5V ± 10%	0 to 70	PHDIP24
	MK48T12B20	2K x 8	200	5V ± 10%	0 to 70	PHDIP24
	MK48T12B25	2K x 8	250	5V ± 10%	0 to 70	PHDIP24
	M48T02-150PC1	2K x 8	150	5V +10/-5%	0 to 70	PCDIP24
	M48T12-150PC1	2K x 8	150	5V ± 10%	0 to 70	PCDIP24
64K	MK48T08B10	8K x 8	100	5V +10/-5%	0 to 70	PHDIP28
	MK48T08B15	8K x 8	150	5V +10/-5%	0 to 70	PHDIP28
	MK48T18B10	8K x 8	100	5V ± 10%	0 to 70	PHDIP28
	MK48T18B15	8K x 8	150	5V ± 10%	0 to 70	PHDIP28
	M48T08-100PC1	8K x 8	100	5V +10/-5%	0 to 70	PCDIP28
	M48T18-100PC1	8K x 8	100	5V ± 10%	0 to 70	PCDIP28
	M48T18-100MH1	8K x 8	100	5V ± 10%	0 to 70	SOH28

SNAPHAT Housing

Family	Part Number	Description	Temperature Range (°C)	Package
ZEROPOWER	M4Z28-BR00SH1	Battery	0 to 70	SH28
TIMEKEEPER	M4T28-BR12SH1	Battery and Crystal	0 to 70	SH28

MEMORY BASED [1]

Product	Process	Memory	Feature/Application
ST1305	CMOS	192 bit EEPROM	Low Cost, TRANSPORT code
ST1331	CMOS	208 bit EEPROM	Anti-Tearing
ST1333	CMOS	288 bit EEPROM	Anti-Tearing & Authentication
ST1335	CMOS	272 bit EEPROM	Anti-Tearing & Authentication
ST1336	CMOS	208 bit EEPROM	Anti-Tearing
ST14C02C	CMOS	2K bit EEPROM	I^2C Serial Access EEPROMs, General Purpose (Health Card, Industry)
ST14C04C	CMOS	4K bit EEPROM	I^2C Serial Access EEPROMs, General Purpose (Health Card, Industry)

Note:1.Trend is larger memory, programmable functions, TRANSPORT and PIN code security.

MICROCOMPUTER BASED

Product	Process	User ROM	RAM	EP/EEPROM	Feature	Application
ST16601	CMOS	1K	128	1088	Firmware security algorithm	Banking
ST16F48	CMOS	16K	288	8K	High EEPROM capacity	Multiservice
ST16SF48	CMOS	16K	288	8K	3V, Firmware security features	Multiservice
ST16CF54	CMOS	16K	352	4K	MAP, RSA in 66ms for 512bit	Cards (Public Key Algorithms)
ST16KF74	CMOS	20K	608	4K	MAP , DES, RSA in 17ms for 512bit	Terminals (Public Key Algorithms)
ST16LF74	CMOS	20K	608	4K	MAP, RSA in 17ms for 512bit	Terminals (Public Key Algorithms)

Note: MAP = Modular Arithmetic Processor

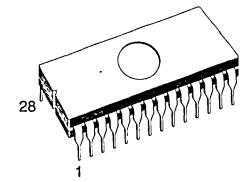
HARDWARE DEVELOPMENT SYSTEM

Part Number	Description	Supply Voltage
ST16XYZ-EMU	ST16XYZ Full Family Emulator	Mixed (110 V and 220V)

CMOS UV EPROM & OTP MEMORIES

CMOS 64K (8K x 8) UV EPROM

- VERY FAST ACCESS TIME: 150ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.5V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- HIGH SPEED PROGRAMMING (less than 1 minute)



FDIP28W (F)

DESCRIPTION

The M27C64A is a high speed 65,536 bit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems requiring large programs. It is organized as 8,192 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Figure 1. Logic Diagram

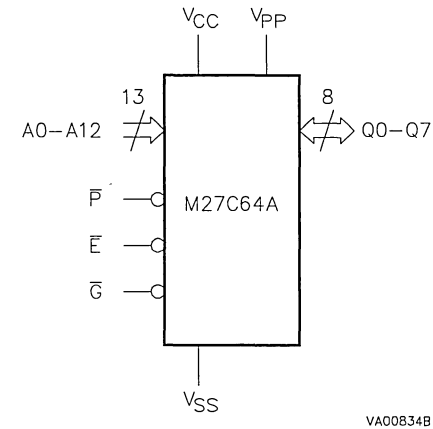


Table 1. Signal Names

A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

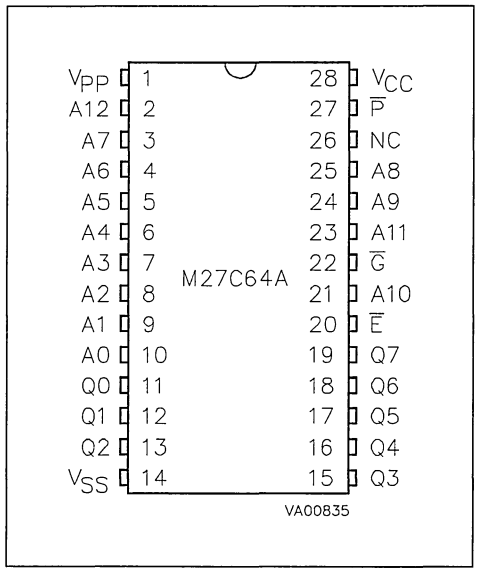
Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2 0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0 5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Figure 2. DIP Pin Connections



Warning: NC = No Connection

DEVICE OPERATION

The modes of operation of the M27C64A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C64A has a standby mode which reduces the active current from 30mA to 100µA. The M27C64A is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made

DEVICE OPERATION (cont'd)

a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C64A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C64A is in the programming mode when V_{pp} input is at 12.5V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6V ± 0.25V.

High Speed Programming

The high speed programming algorithm, described in the flowchart, rapidly programs the M27C64A using an efficient and reliable method, particularly suited to the production programming environment. An individual device will take around 1 minute to program.

Program Inhibit

Programming of multiple M27C64A in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C64A may be common. A TTL low level pulse applied to a M27C64A $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.5V, will program that M27C64A. A high level $\overline{E}$ input inhibits the other M27C64A from being programmed.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	1	0	0	1	1	0	1	1	9Bh
Device Code	V_{IH}	0	0	0	0	1	0	0	0	08h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

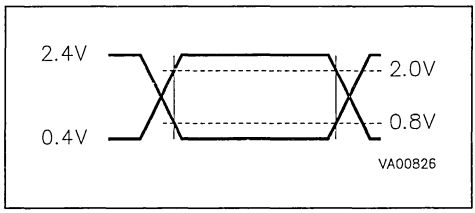


Figure 4. AC Testing Load Circuit

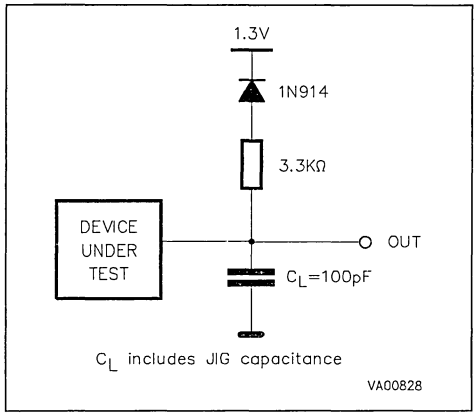


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1 Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

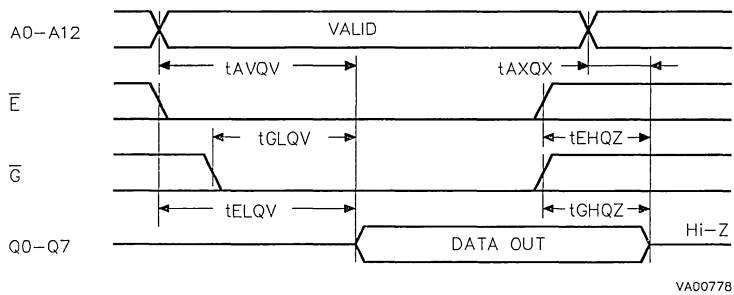


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C: V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C: V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C64A								Unit
				-15		-20		-25		-30		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200		250		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200		250		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		75		80		100		120	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	50	0	60	0	105	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	50	0	60	0	105	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			30	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		30	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width (Initial)		0.95	1.05	ms
		Program Pulse Width (Over Program)		2.85	78.75	ms
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

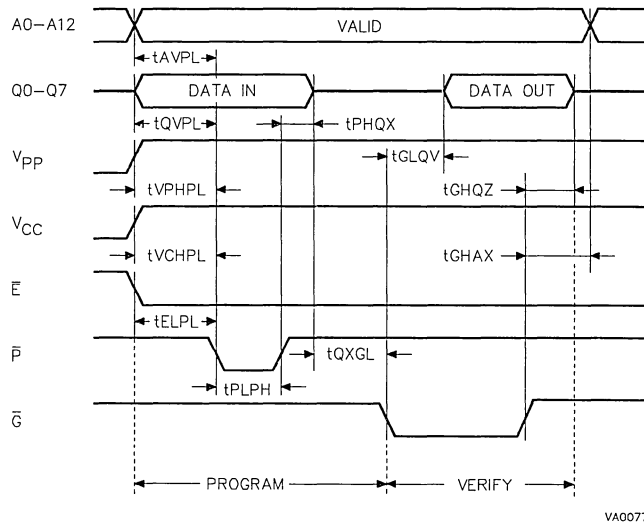
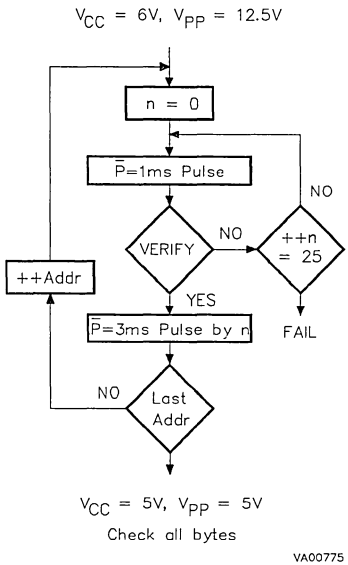


Figure 7. Programming Flowchart



Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.5V and V_{CC} at 6V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C64A. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C64A, with V_{PP}=V_{CC}=5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C64A, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C64A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C64A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C64A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C64A window to prevent unintentional erasure. The recommended erasure procedure for the M27C64A is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27C64A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C64A -15 F 1 X

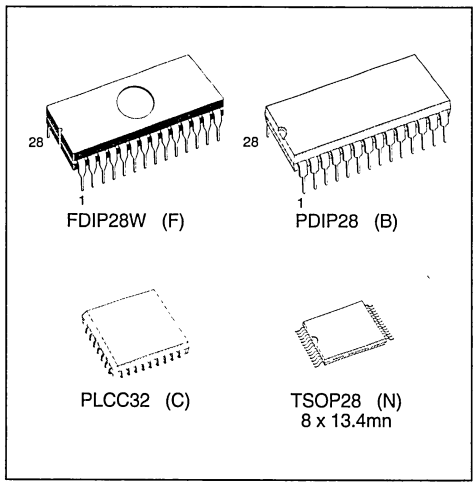
Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-15	150 ns	blank	± 10%	F	FDIP28W	1	0 to 70 °C	X	Additional Burn-in
-20	200 ns					6	–40 to 85 °C		
-25	250 ns								
-30	300 ns								

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 256K (32K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 3sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C256B is a high speed 262,144 bit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems. It is organized as 32,768 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C256B is offered in Plastic Dual-in-Line, Plastic Leaded Chip Carrier, and Plastic Thin Small Outline packages.

Figure 1. Logic Diagram

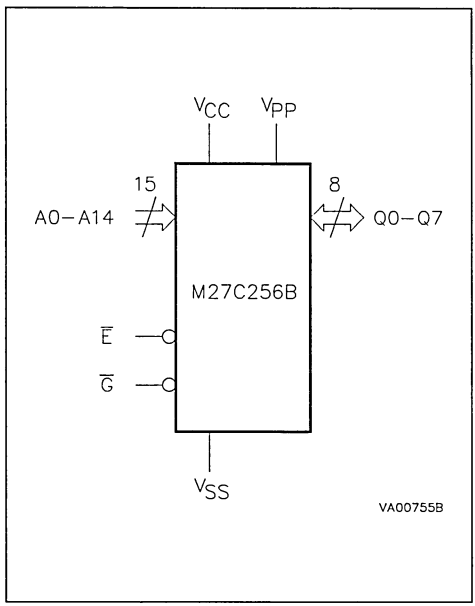


Table 1. Signal Names

A0 - A14	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Figure 2A. DIP Pin Connections

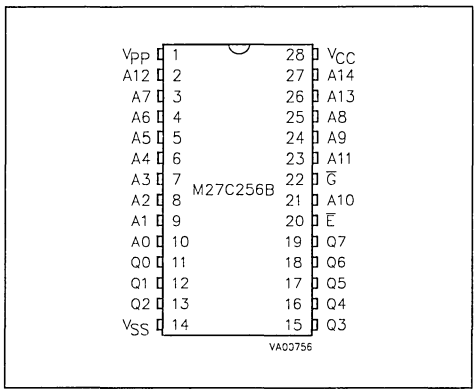
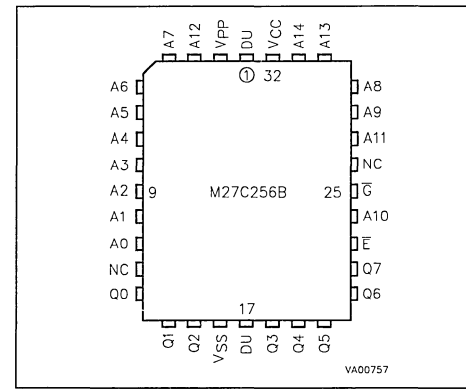
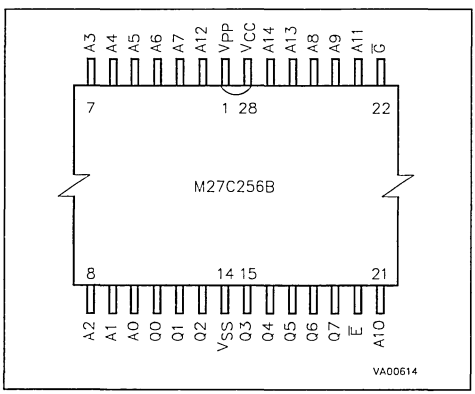


Figure 2B. LCC Pin Connections



Warning: NC = No Connection, DU = Dont't Use.

Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operation of the M27C256B are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C256B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time

DEVICE OPERATION (cont'd)

is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C256B has a standby mode which reduces the active current from 30 mA to 100µA. The M27C256B is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Considerations

The power switching characteristics of Advance CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	1	1	0	1	8Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

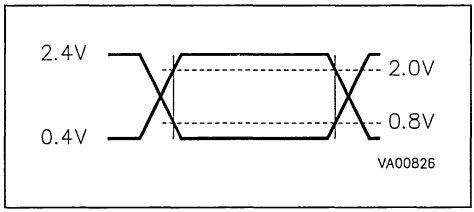


Figure 4. AC Testing Load Circuit

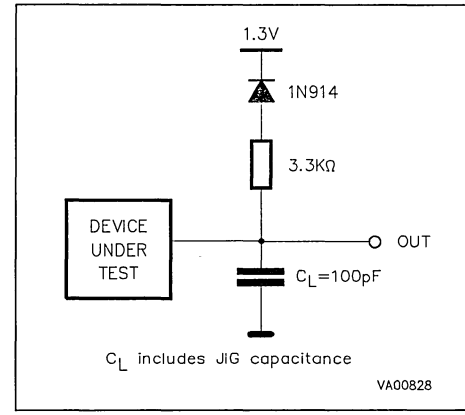


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C256B						Unit
				-70		-80		-90		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		80		90	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		80		90	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		40	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C256B						Unit
				-10		-12		-15/-20/-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		60		65	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

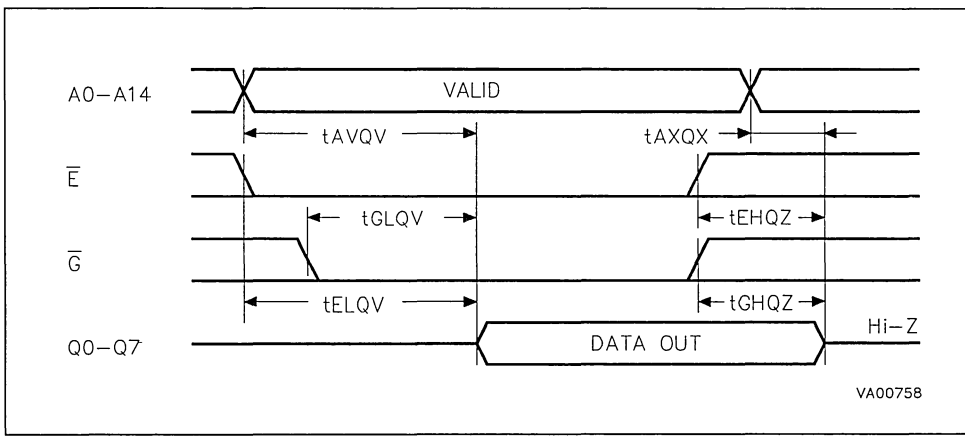


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

DEVICE OPERATION (cont'd)

4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C256B are in the '1' state. Data is introduced by selectively programming '0' into the desired bit locations. Although only '0' will be programmed, both '1' and '0' can be present in the data word. The only way to change a '0' to a '1' is by die exposition to ultraviolet light (UV EPROM). The M27C256B is in the programming mode when V_{PP} input is at 12.75 V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

Figure 6. Programming and Verify Modes AC Waveforms

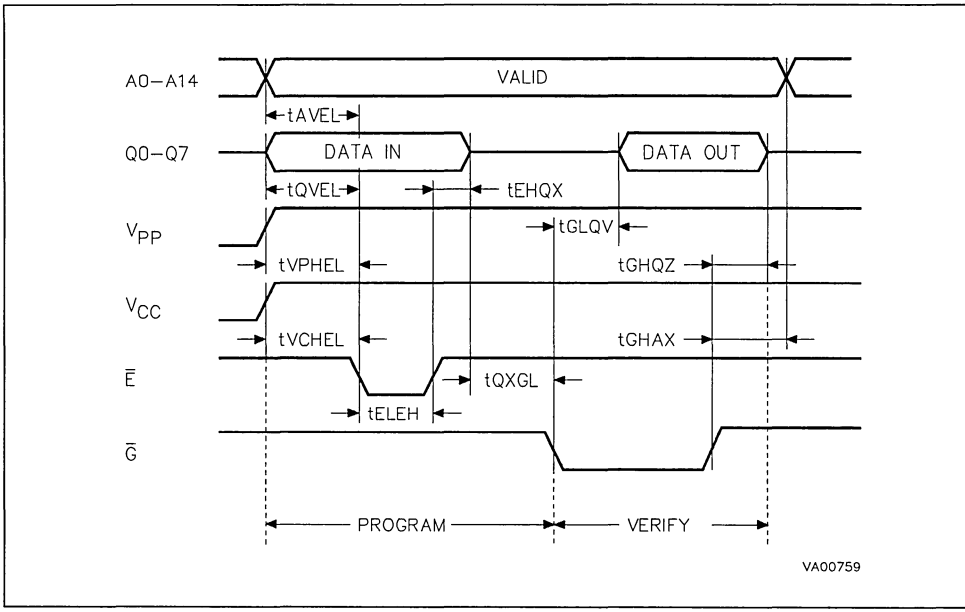
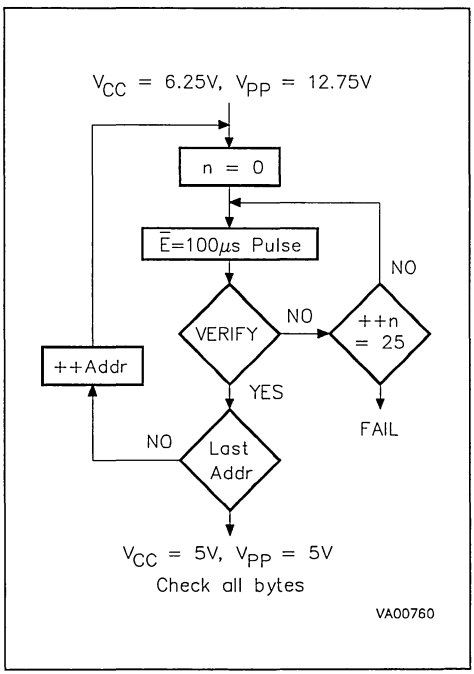


Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in a typical time of less than 3 seconds. Programming with PRESTO II involves the application of a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C256Bs in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C256B may be common. A TTL low level pulse applied to a M27C256B's $\overline{E}$ input, with V_{PP} at 12.75 V, will program that M27C256B. A high level $\overline{E}$ input inhibits the other M27C256Bs from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C256B. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C256B, with V_{CC} = V_{PP} = 5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C256B, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C256B is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C256B in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C256B is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C256B window to prevent unintentional erasure. The recommended erasure procedure for the M27C256B is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C256B should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C256B -70 X C 1 TR

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-70	70 ns	X	± 5%	F	FDIP28W	1	0 to 70 °C	X	Additional Burn-in
-80	80 ns	blank	± 10%	B	PDIP28	3	–40 to 125 °C	TR	Tape & Reel Packing
-90	90 ns			C	PLCC32	6	–40 to 85 °C		
-10	100 ns			N	TSOP28 8 x 13.4mm	7	–40 to 105 °C		
-12	120 ns								
-15	150 ns								
-20	200 ns								
-25	250 ns								

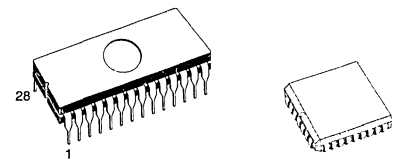
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

M87C257

ADDRESS LATCHED CMOS 256K (32K x 8) UV EPROM and OTP ROM

- INTEGRATED ADDRESS LATCH
- VERY FAST ACCESS TIME: 100ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 3sec. (PRESTO II ALGORITHM)



FDIP28W (F)

PLCC32 (C)

DESCRIPTION

The M87C257 is a high speed 262,144 bit UV erasable and electrically programmable memory EPROM. The M87C257 incorporates latches for all address inputs to minimize chip count, reduce cost, and simplify the design of multiplexed bus systems.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M87C257 is offered in Plastic Leaded Chip Carrier, package.

Table 1. Signal Names

A0 - A14	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{AS}V_{PP}$	Address Strobe / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

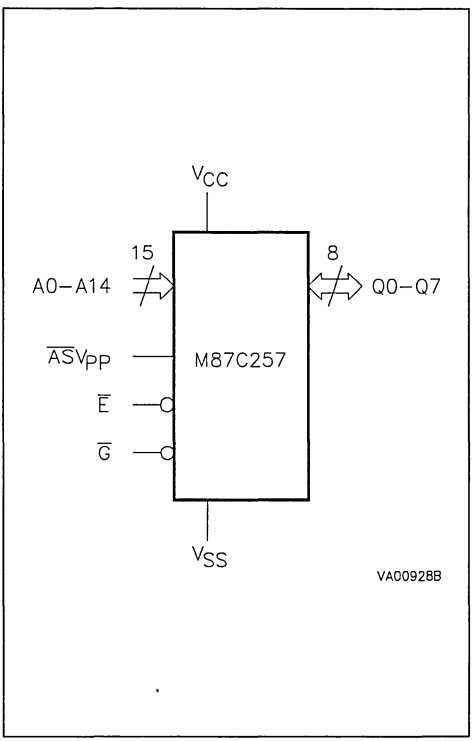


Figure 2A. DIP Pin Connections

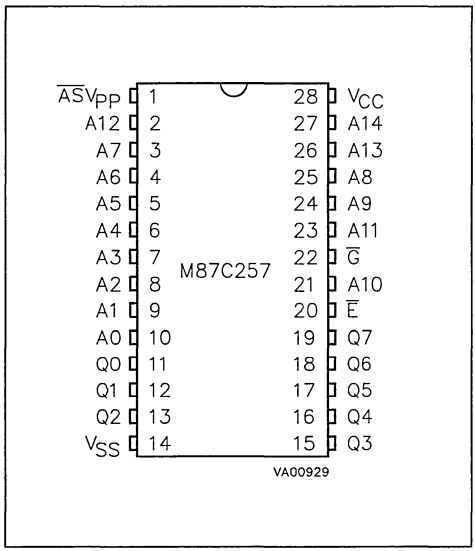
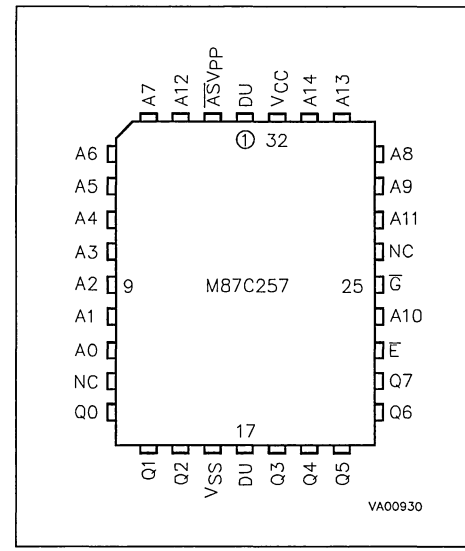


Figure 2C. LCC Pin Connections



Warning: NC = No Connection, DU = Dont't Use.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operation of the M87C257 are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M87C257 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should

DEVICE OPERATION (cont'd)

be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable ($\overline{AS}$ = V_{IH}) or latched ($\overline{AS}$ = V_{IL}), the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

The M87C257 reduces the hardware interface in multiplexed address-data bus systems. The processor multiplexed bus (AD0-AD7) may be tied to the M87C257's address and data pins. No separate address latch is needed because the M87C257 latches all address inputs when $\overline{AS}$ is low.

Standby Mode

The M87C257 has a standby mode which reduces the active current from 30mA to 100µA (Address Stable). The M87C257 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Considerations

The power switching characteristics of Advance CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	$\overline{AS}/V_{PP}$	Q0 - Q7
Read (Latched Address)	V_{IL}	V_{IL}	X	V_{IL}	Data Out
Read (Applied Address)	V_{IL}	V_{IL}	X	V_{IH}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{IL}	Codes

Note. X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	0	0	0	0	80h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

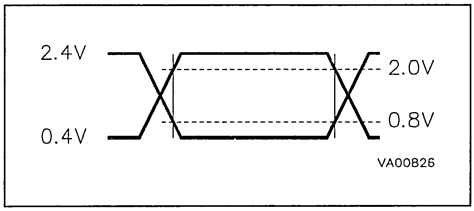


Figure 4. AC Testing Load Circuit

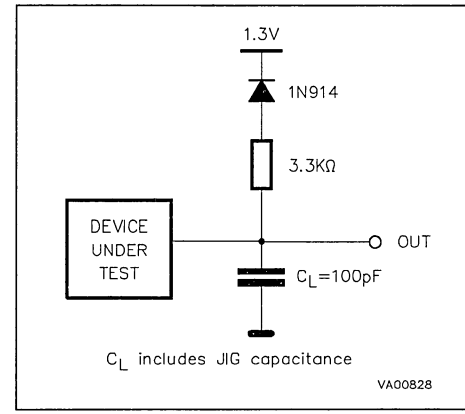


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

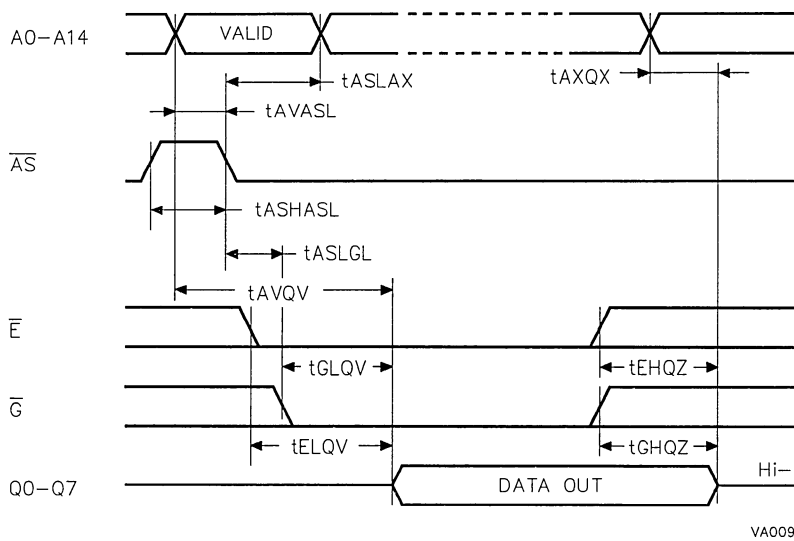


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{ASV}_{PP} = V_{IH}$, Address Switching		10	mA
		$\overline{E} = V_{IH}$, $\overline{ASV}_{PP} = V_{IL}$, Address Stable		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} \ge V_{CC} - 0.2V$, $\overline{ASV}_{PP} \ge V_{CC} - 0.2V$, Address Switching		6	mA
		$\overline{E} \ge V_{CC} - 0.2V$, $\overline{ASV}_{PP} = V_{SS}$, Address Stable		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	V_{CC} – 0.8V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M87C257								Unit
				-10		-12		-15		-20		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100		120		150		200	ns
t_{AVASL}	t_{AL}	Address Valid to Address Strobe Low		7		7		7		15		ns
t_{ASHASL}	t_{LL}	Address Strobe High to Address Strobe Low		35		35		35		50		ns
t_{ASLAX}	t_{LA}	Address Strobe Low to Address Transition		20		20		20		30		ns
t_{ASLGL}	t_{LOE}	Address Strobe Low to Output Enable Low		20		20		20		30		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		40		50		60		70	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	40	0	40	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	40	0	40	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	V_{CC} -0.8V		V
V_{ID}	A9 Voltage		11.5	12.5	V

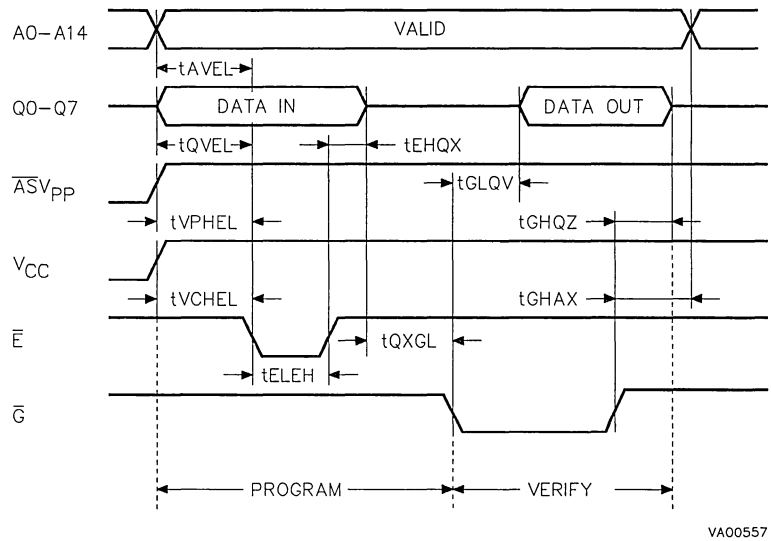
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Figure 6. Programming and Verify Modes AC Waveforms



DEVICE OPERATION (cont'd)

capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M87C257 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M87C257 is in the programming mode when V_{PP} input is at 12.75 V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

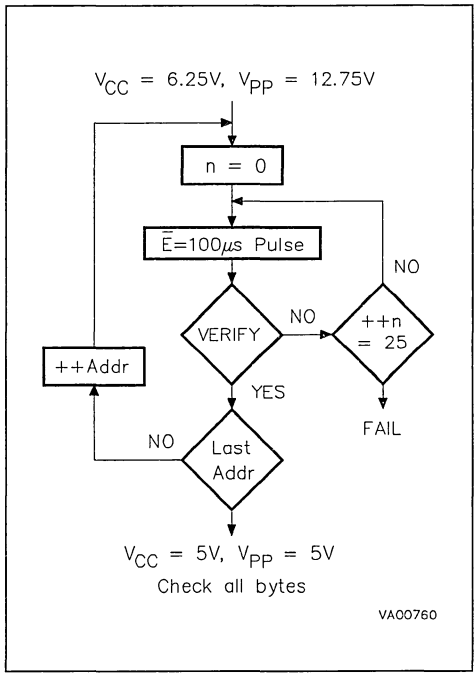
PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in a typical time of less than 3 seconds. Programming with PRESTO II involves the application of a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M87C257s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M87C257 may be common. A TTL low level pulse applied to a M87C257's $\overline{E}$ input, with V_{PP} at 12.75 V, will program that M87C257. A high level $\overline{E}$ input inhibits the other M87C257s from being programmed.

Figure 7. Programming Flowchart



Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M87C257. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M87C257, with $V_{CC} = V_{PP} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. When A9 = V_{ID}, $\overline{AS}$ need not be toggled to latch each identifier address. For the SGS-THOMSON M87C257, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M87C257 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M87C257 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M87C257 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M87C257 window to prevent unintentional erasure. The recommended erasure procedure for the M87C257 is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M87C257 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M87C257 -10 X F 1 X

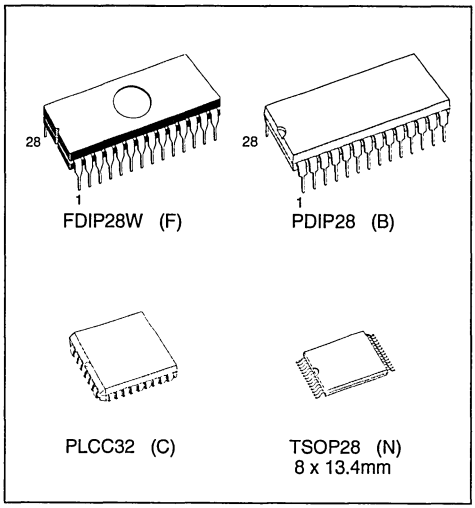
Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-10	100 ns	X	± 5%	F	FDIP28W	1	0 to 70 °C	X	Additional Burn-in
-12	120 ns	blank	± 10%	C	PLCC32	3	–40 to 125 °C	TR	Tape & Reel Packing
-15	150 ns					6	–40 to 85 °C		
-20	200 ns					7	–40 to 105 °C		

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 512K (64K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 60ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 6sec. (PRESTO IIB ALGORITHM)



DESCRIPTION

The M27C512 is a high speed 524,288 bit UV erasable and electrically programmable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements. Its is organized as 65,536 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C512 is offered in Plastic Dual-in-Line, Plastic Thin Small Outline and Plastic Leaded Chip Carrier packages.

Figure 1. Logic Diagram

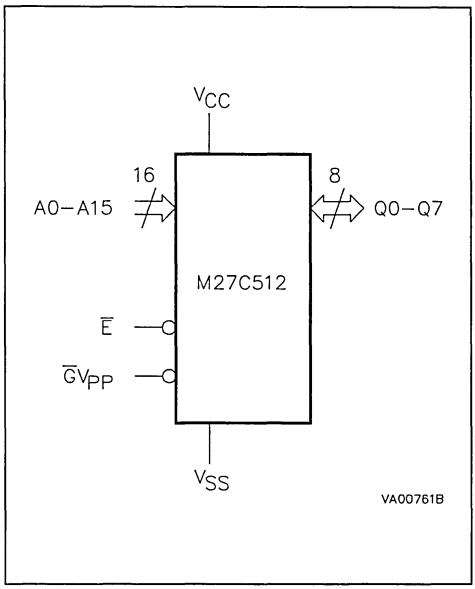


Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Figure 2A. DIP Pin Connections

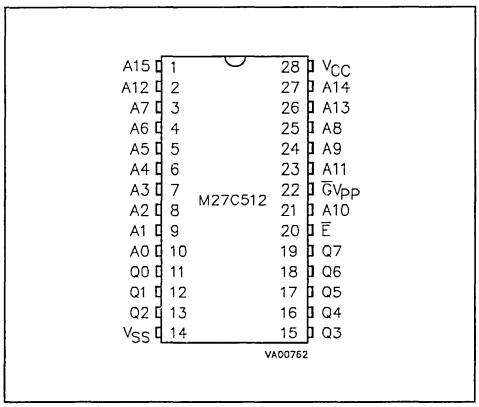
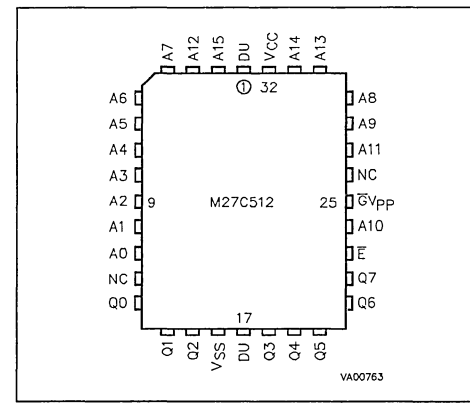
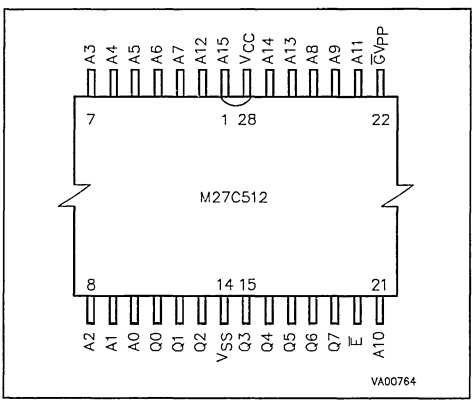


Figure 2B. LCC Pin Connections



Warning: NC = No Connection, DU = Don't Use

Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operations of the M27C512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}/V_{PP}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data

DEVICE OPERATION (cont'd)

is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C512 has a standby mode which reduces the active current from 30mA to 100µA The M27C512 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supplyconnection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C512 are in the '1' state. Data is introduced by selectively programming '0' into the desired bit locations. Although only '0' will be programmed, both '1' and '0' can be present in the data word. The only way to change a '0' to a '1' is by die exposure to ultraviolet light (UV EPROM). The M27C512 is in the programming mode when V_{PP} input is at 12.75V and $\overline{E}$ is at

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q0 - Q7
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	1	1	1	1	0	1	3Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

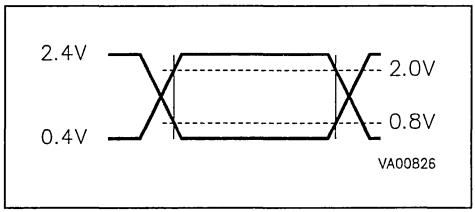


Figure 4. AC Testing Load Circuit

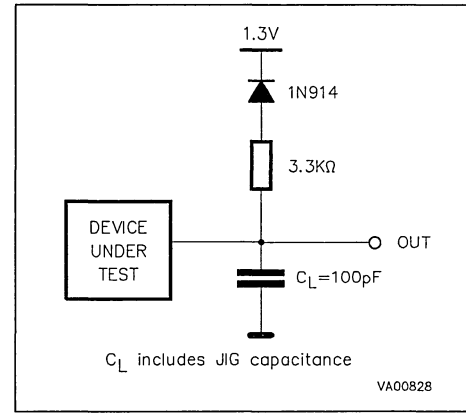


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note. 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C512								Unit
				-60		-70		-80		-90		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		60		70		80		90	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		60		70		80		90	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		30		35		40		40	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	25	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	25	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C512						Unit
				-10		-12		-15/-20/-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

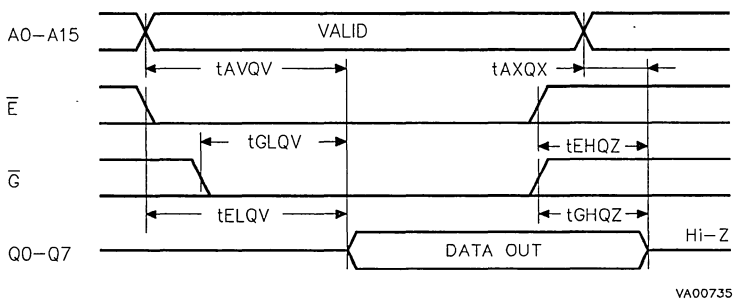


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. MARGIN MODE AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	VA9 High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	VA10 High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	VA10 Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to VA10 Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to VA9 Transition		2		µs

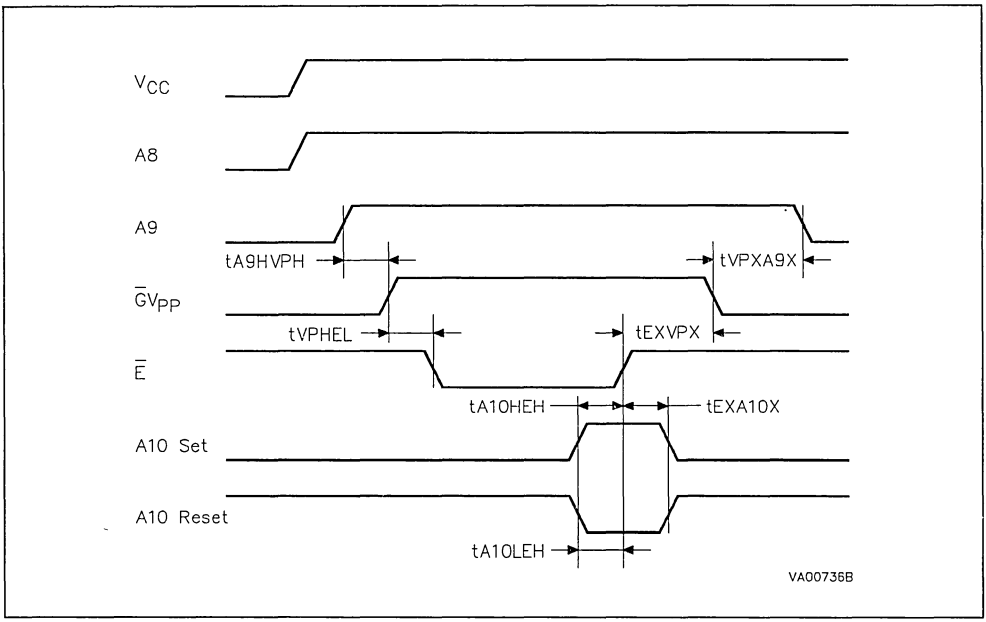
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} (2)	t_{DFP}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. MARGIN MODE AC Waveforms



Note: A8 High level = 5V; A9 High level = 12V.

Figure 7. Programming and Verify Modes AC Waveforms

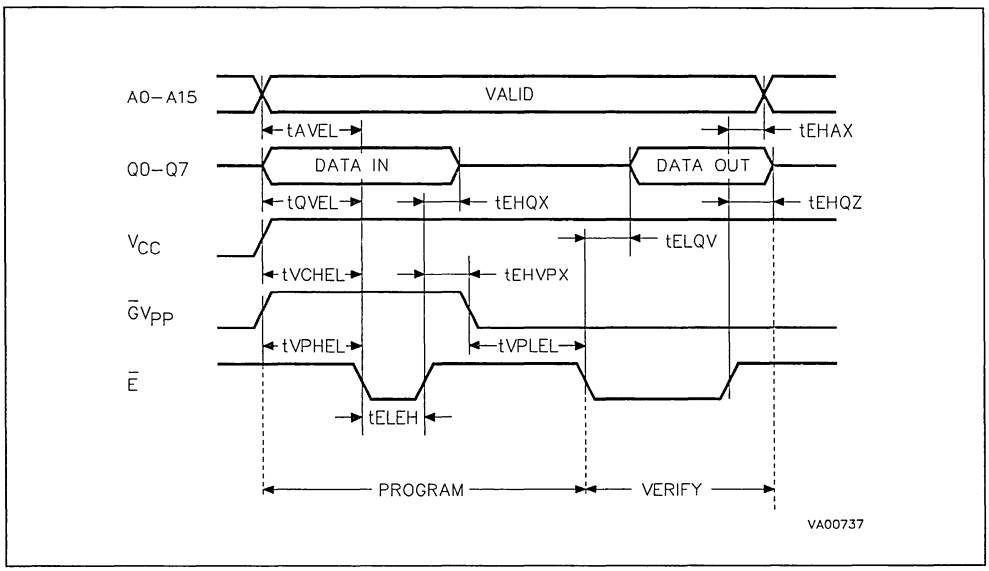
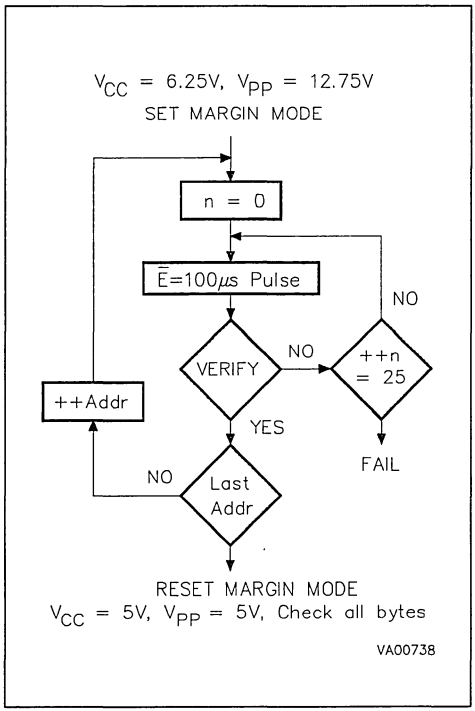


Figure 8. Programming Flowchart



DEVICE OPERATION (cont'd)

TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

The M27C512 can use PRESTO IIB Programming Algorithm that drastically reduces the programming time (typically less than 6 seconds). Nevertheless to achieve compatibility with all programming equipments, PRESTO Programming Algorithm can be used as well.

PRESTO IIB Programming Algorithm

PRESTO IIB Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 7 seconds. This can be achieved with SGS-THOMSON M27C512 due to several design innovations described in the M27C512 datasheet to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 100µs program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin.

Program Inhibit

Programming of multiple M27C512s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ V_{PP} of the parallel M27C512 may be common. A TTL low level pulse applied to a M27C512's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27C512. A high level $\overline{E}$ input inhibits the other M27C512s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}. Data should be verified with t_{ELQV} after the falling edge of $\overline{E}$.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C512, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range.

Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C512 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C512 window to prevent unintentional erasure. The recommended erasure procedure for the M27C512 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C512 -70 X C 1 TR

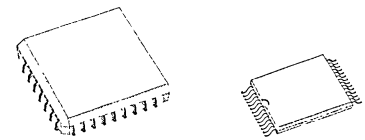
Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-60	60 ns	X	± 5%	F	FDIP28W	1	0 to 70 °C	X	Additional Burn-in
-70	70 ns	blank	± 10%	B	PDIP28	3	–40 to 125 °C	TR	Tape & Reel Packing
-80	80 ns			C	PLCC32	6	–40 to 85 °C		
-90	90 ns			N	TSOP28 8 x 13.4mm				
-10	100 ns								
-12	120 ns								
-15	150 ns								
-20	200 ns								
-25	250 ns								

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

LOW VOLTAGE CMOS 512K (64K x 8) OTP ROM

- LOW VOLTAGE READ OPERATION
  - V_{CC} Range: 3V to 5.5V (T_A = 0 to 70°C)
  - V_{CC} Range: 3.2V to 5.5V (T_A = –40 to 85°C)
- ACCESS TIME: 120, 150 and 200ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 10mA
  - Standby Current 10µA
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 6sec. (PRESTO IIB ALGORITHM)
- M27V512 is PROGRAMMABLE as M27C512 with IDENTICAL SIGNATURE



PLCC32 (K)

TSOP28 (N)
8 x 13.4mm

DESCRIPTION

The M27V512 is a low voltage, low power 512K One Time Programmable ROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements. Its is organized as 524,288 by 8 bits.

The M27V512 operates in the read mode with a supply voltage as low as 3V (3.2V between –40 to 85°C). The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges. The M27V512 can also be operated as a standard 512 EPROM (similar to M27C512) with a 5V power supply .

For equipment requiring a surface monted, low profile package, theM27V512 is offered in Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

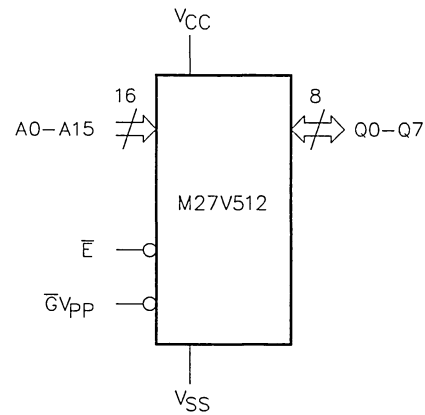


Figure 2A. LCC Pin Connections

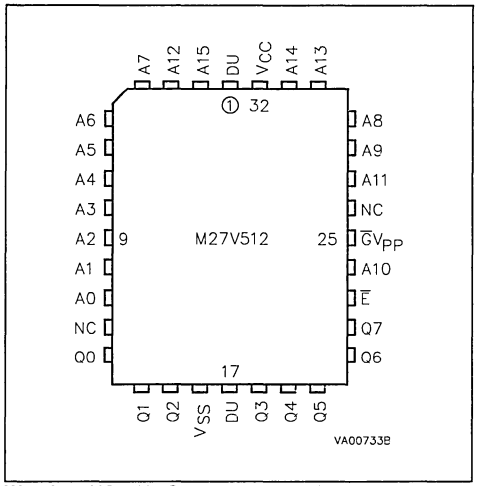
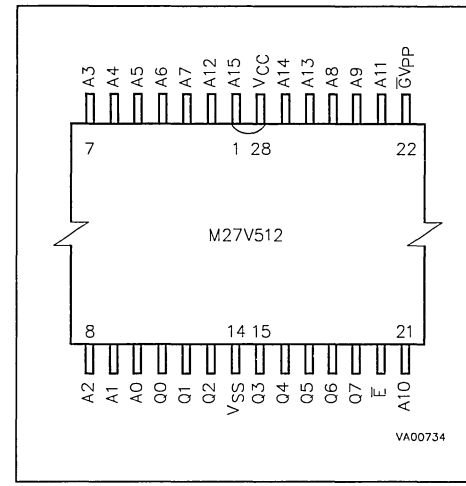


Figure 2B. TSOP Pin Connections



Warning: NC = No Connection, DU = Don't Use.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operations of the M27V512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27V512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, inde-

DEVICE OPERATION (Cont'd)

pendent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V512 has a standby mode which reduces the active current from 10mA to 10µA with low voltage operation $V_{CC} \leq 3.2V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V512 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because OTP ROMs are often used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS OTP ROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supplyconnection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q0 - Q7
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	1	1	1	1	0	1	3Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

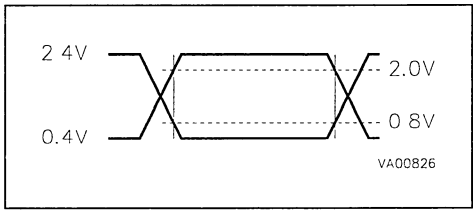


Figure 4. AC Testing Load Circuit

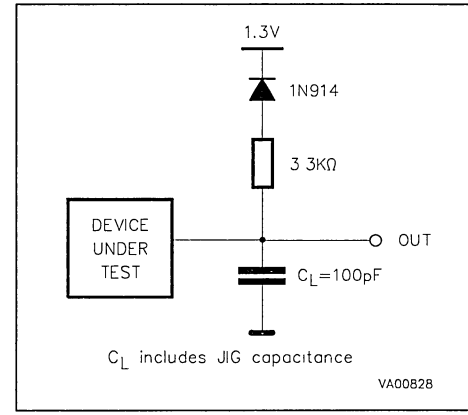


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} ≤ 3.2V		10	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 3.2V		10	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27V512						Unit
				-120		-150		-200		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		65		70		80	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	60	0	60	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	60	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

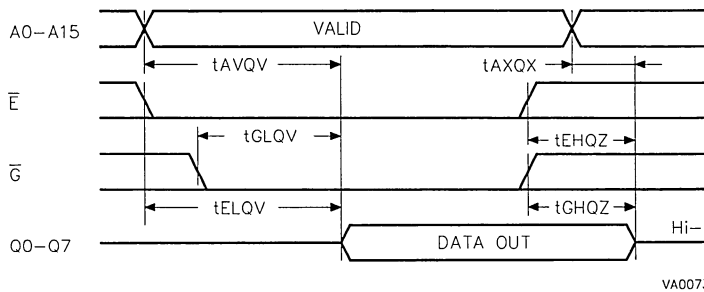


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Table 9. MARGIN MODE AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

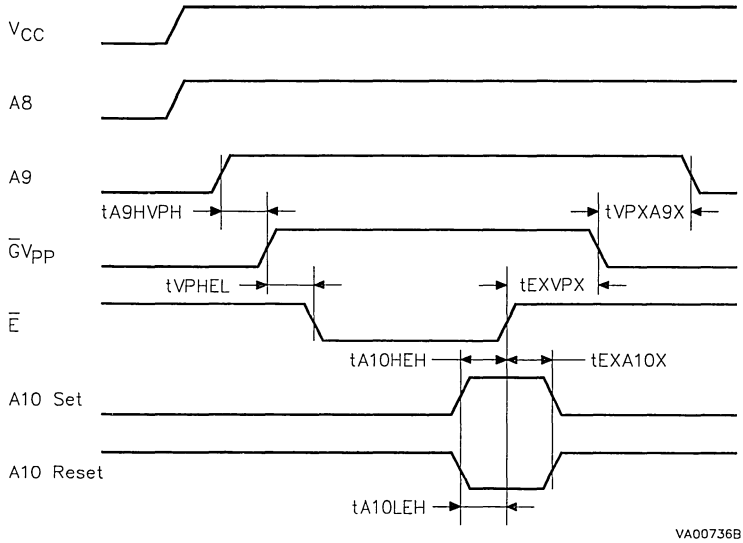
Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	VA9 High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	VA10 High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	VA10 Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to VA10 Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to VA9 Transition		2		µs

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		0		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} (2)	t_{DFP}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. MARGIN MODE AC Waveforms



Note: A8 High level = 5V; A9 High level = 12V.

Figure 7. Programming and Verify Modes AC Waveforms

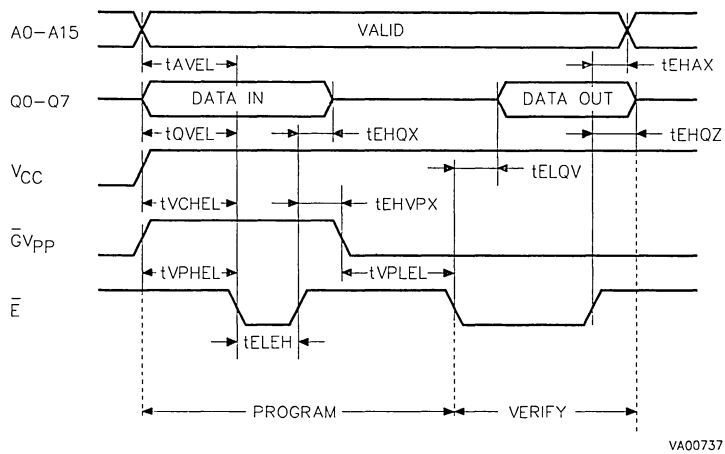
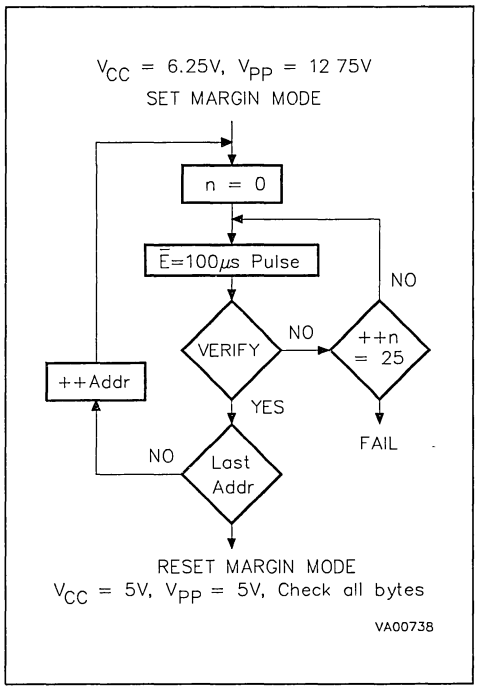


Figure 8. Programming Flowchart



Programming

The M27V512 has been designed to be fully compatible with the M27C512. As a result the M27V512 can be programmed as the M27C512 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27V512 has the same electronic signature and uses the same PRESTO IIB algorithm.

When delivered, all bits of the M27V512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The M27V512 is in the programming mode when V_{PP} input is at 12.75V and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

The M27V512 uses the PRESTO IIB Programming Algorithm that drastically reduces the programming time (typically less than 6 seconds). Nevertheless to achieve compatibility with all programming equipments, PRESTO Programming Algorithm can be used as well.

PRESTO IIB Programming Algorithm

PRESTO IIB Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in around 6 seconds. This can be achieved with SGS-THOMSON M27V512 due to several design innovations to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 100µs program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin.

Program Inhibit

Programming of multiple M27V512s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}V_{PP}$ of the parallel M27V512 may be common. A TTL low level pulse applied to a M27V512's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27V512. A high level $\overline{E}$ input inhibits the other M27V512s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}. Data should be verified with t_{ELQV} after the falling edge of $\overline{E}$.

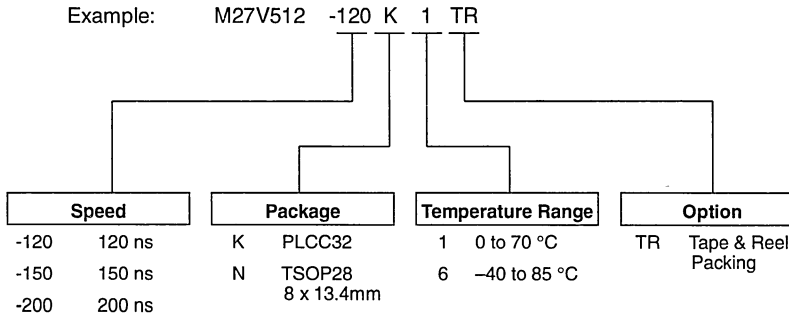
Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V512. To activate this mode, the programming equipment must apply a Supply Voltage V_{CC} of 5V and force 11.5V to 12.5V on address line A9 of the M27V512.

Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27V512, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

Note that the M27V512 and the M27C512 have the same identifier bytes.

ORDERING INFORMATION SCHEME

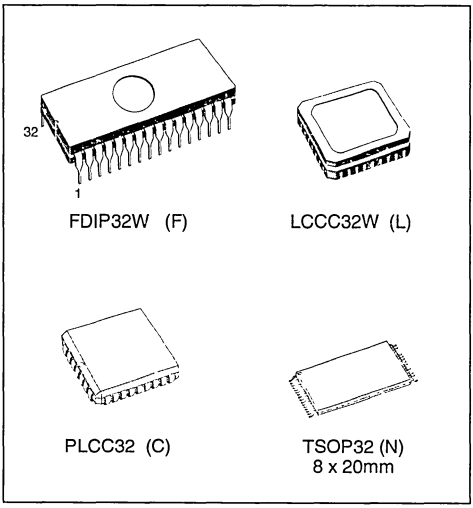


For a list of available options (Speed, Package, Temperature Range, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 1 Megabit (128K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 60ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 12sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C1001 is a high speed 1 Megabit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems requiring large programs. It is organized as 131,072 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure. For applications where the content is programmed only one time and erasure is not required, the M27C1001 is offered in both Plastic Dual-in-Line, Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Table 1. Signal Names

A0 - A16	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

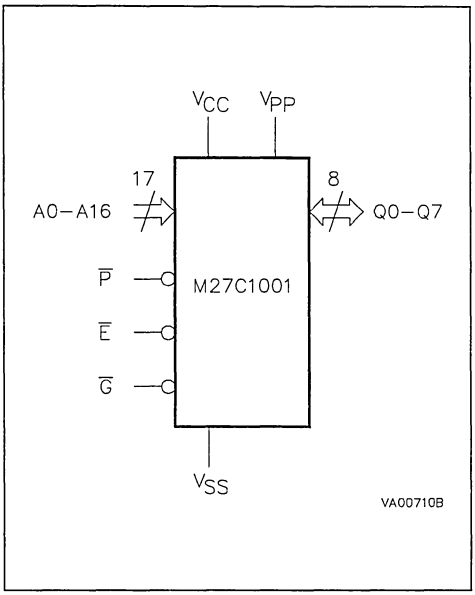
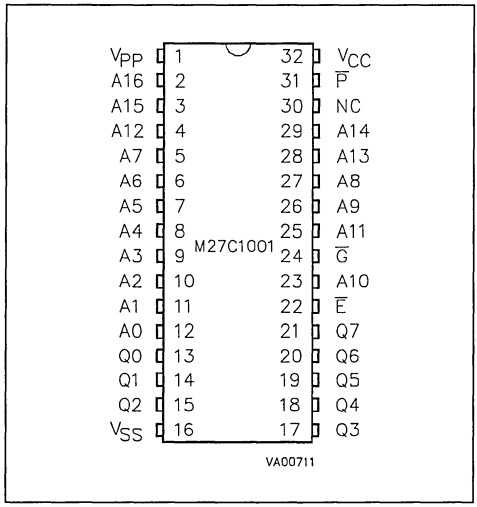
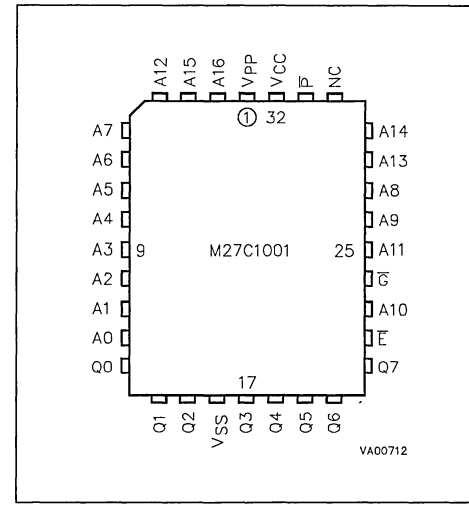


Figure 2A. DIP Pin Connections



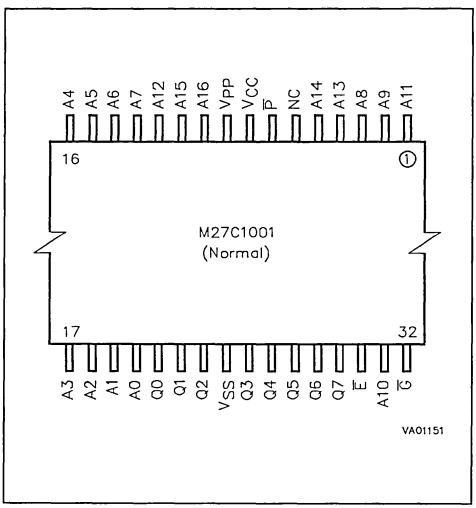
Warning: NC = No Connection.

Figure 2B. LCC Pin Connections



Warning: NC = No Connection.

Figure 2C. TSOP Pin Connections



Note: This is advance information on a new product now in development Details are subject to change without notice.

DEVICE OPERATION

The modes of operation of the M27C1001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C1001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C1001 has a standby mode which reduces the active current from 30mA to 100µA. The M27C1001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	0	1	05h

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

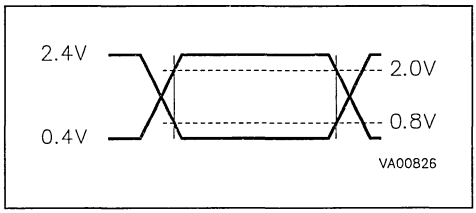


Figure 4. AC Testing Load Circuit

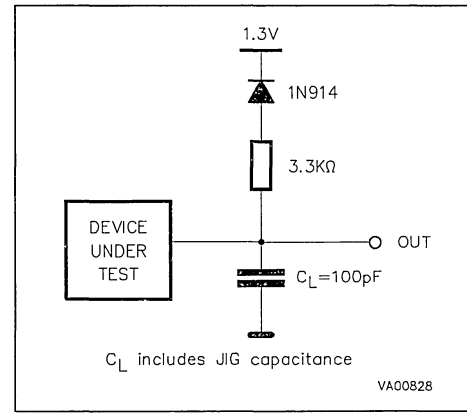


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0 5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1001								Unit
				-60		-70		-80		-90		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		60		70		80		90	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		60		70		80		90	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		35		40		45	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1001						Unit
				-10		-12		-15/-20/-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		60		65	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

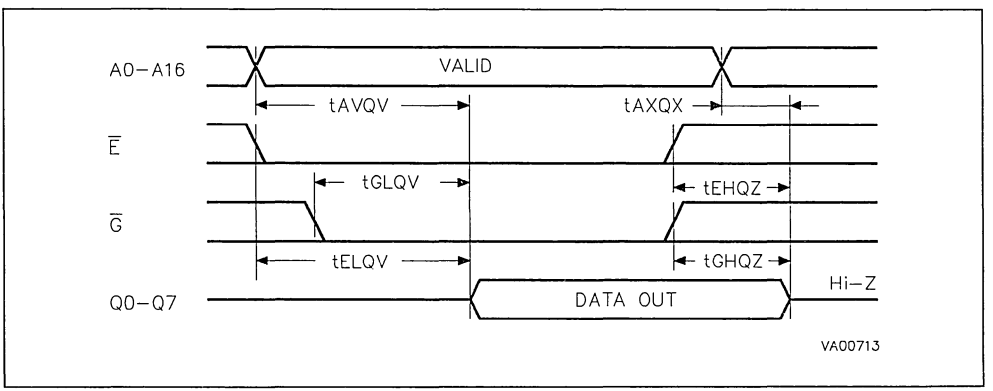


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

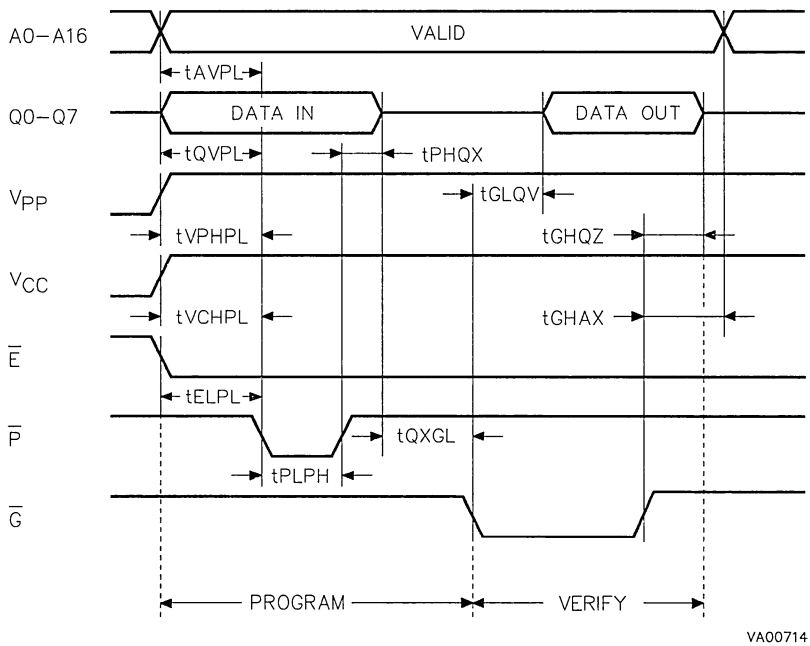
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



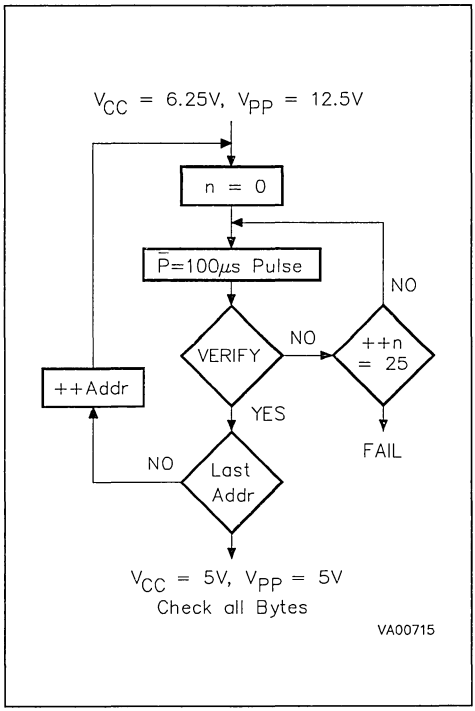
DEVICE OPERATION (cont'd)

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C1001 are in the '1' state. Data is introduced by selectively programming '0' into the desired bit locations. Although only '0' will be programmed, both '1' and '0' can be present in the data word. The only way to change a '0' to a '1' is by die exposition to ultraviolet light (UV EPROM). The M27C1001 is in the programming mode when V_{pp} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in around 12 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C1001s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C1001 may be common. A TTL low level pulse applied to a M27C1001's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C1001. A high level $\overline{E}$ input inhibits the other M27C1001s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C1001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C1001, with V_{PP}=V_{CC}=5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C1001, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C1001 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C1001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C1001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1001 is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27C1001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C1001 -70 X C 1 TR

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-60	60 ns	X	± 5%	F	FDIP32W	1	0 to 70 °C	X	Additional Burn-in
-70	70 ns	blank	± 10%	B	PDIP32	3	–40 to 125 °C	TR	Tape & Reel Packing
-80	80 ns			C	PLCC32	6	–40 to 85 °C		
-90	90 ns			L	LCCC32W				
-10	100 ns			N	TSOP32 8 x 20mm				
-12	120 ns								
-15	150 ns								
-20	200 ns								
-25	250 ns								

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

M27V101

LOW VOLTAGE CMOS 1 Megabit (128K x 8) UV EPROM and OTP ROM

- LOW VOLTAGE READ OPERATION
  - V_{CC} Range: 3V to 5.5V (T_A = 0 to 70°C)
  - V_{CC} Range: 3.2V to 5.5V (T_A = –40 to 85°C)
- ACCESS TIME: 120, 150 and 200ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES for SURFACE MOUNTING:
  - Ceramic: LCCC32W, ultra-thin 2.8mm (max) height
  - Plastic: PLCC32 and TSOP32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 12sec. (PRESTO II ALGORITHM)
- M27V101 is PROGRAMMABLE as M27C1001 with IDENTICAL SIGNATURE

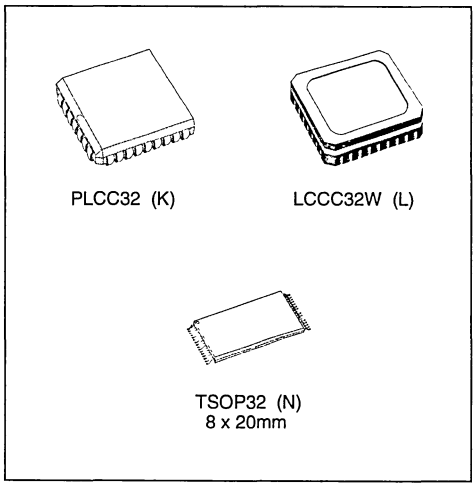
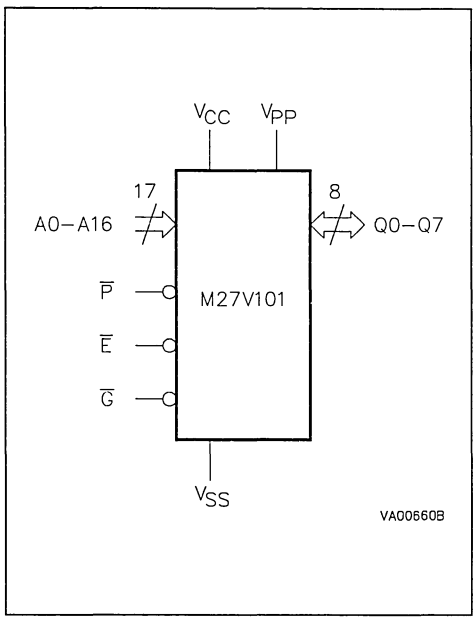


Figure 1. Logic Diagram



DESCRIPTION

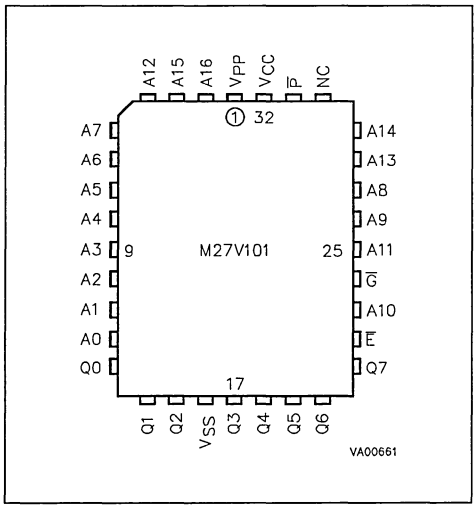
The M27V101 is a low voltage, low power 1 Megabit electrically programmable memory (EPROM), ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 131,072 by 8 bits.

The M27V101 operates in the read mode with a supply voltage as low as 3V (3.2V between –40 to 85°C). The decrease in operating power allows

Table 1. Signal Names

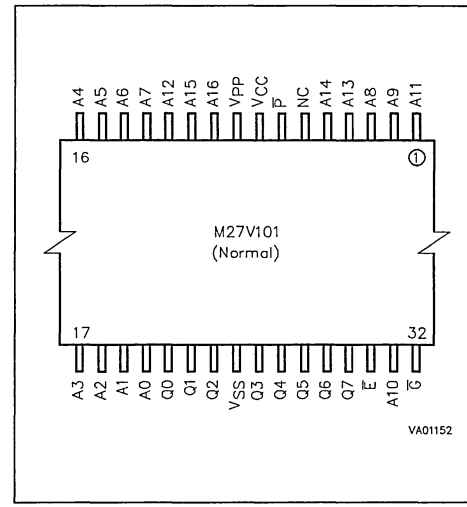
A0 - A16	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. LCC Pin Connections



Warning: NC = No Connection.

Figure 2B. TSOP Pin Connections



Note: This is advance information on a new product now in development. Details are subject to change without notice.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DESCRIPTION (cont'd)

either a reduction of the size of the battery or an increase in the time between battery recharges. The M27V101 can also be operated as a standard 1 Megabit EPROM (similar to M27C1001) with a 5V power supply .

The 32 pin Window, Leadless Chip Carrier package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure. For applications where the content is programmed only one time and erasure is not required, the M27V101 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

DEVICE OPERATION

The modes of operation of the M27V101 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27V101 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V101 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation $V_{CC} \leq 3.2V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V101 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer:

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: $X = V_{IH}$ or V_{IL}, $V_{ID} = 12V \pm 0.5V$

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	0	1	05h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

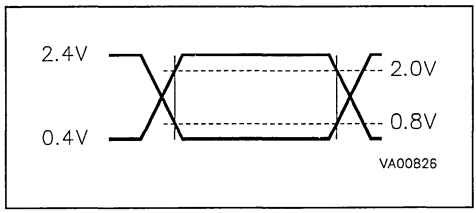


Figure 4. AC Testing Load Circuit

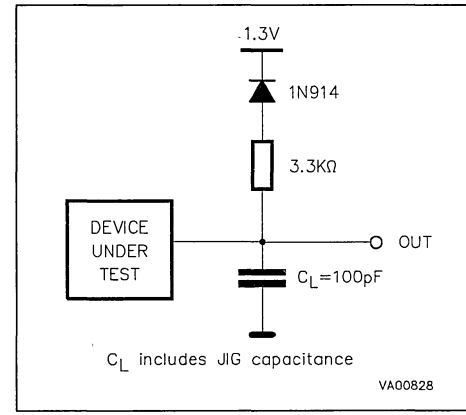


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} ≤ 3.2V		15	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 3.2V		20	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27V101						Unit
				-120		-150		-200		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		80		85		90	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	70	0	70	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	70	0	70	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

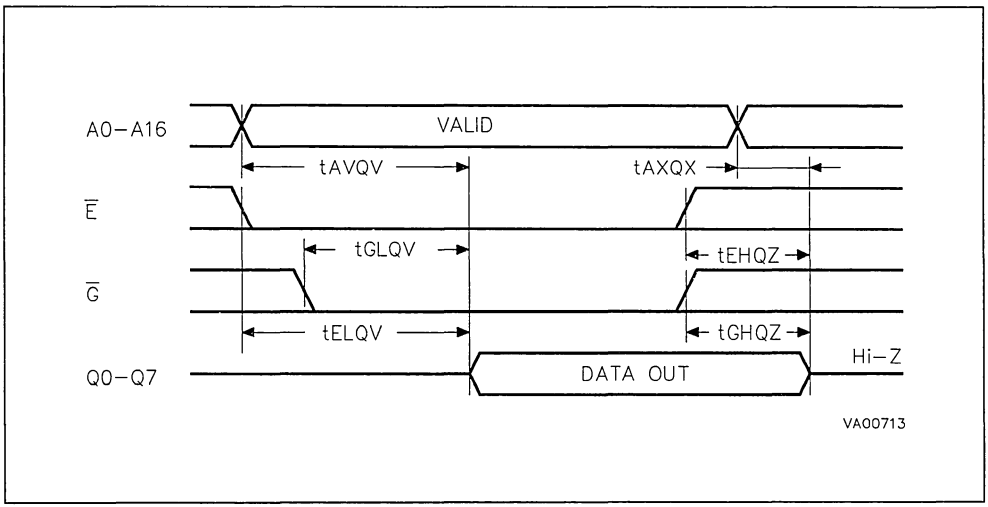


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

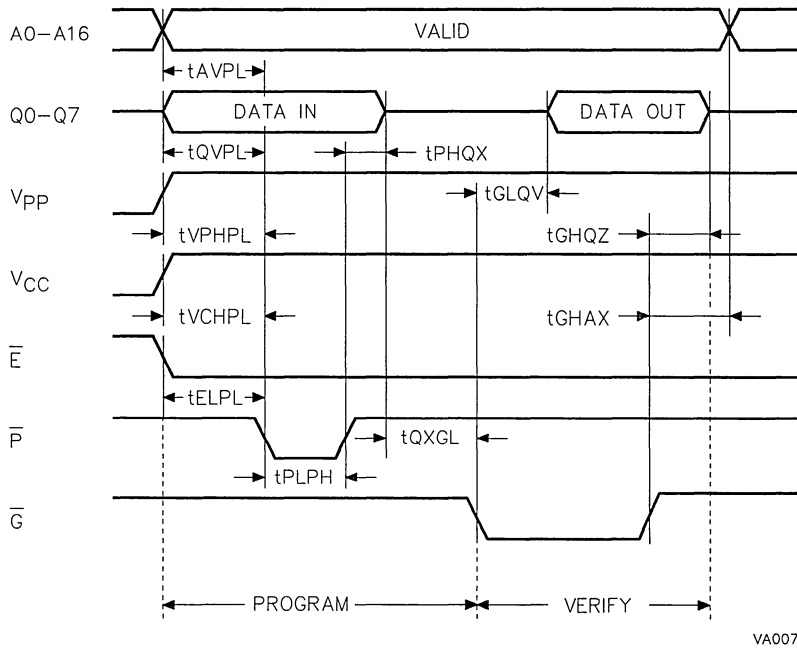
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



DEVICE OPERATION (cont'd)

the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

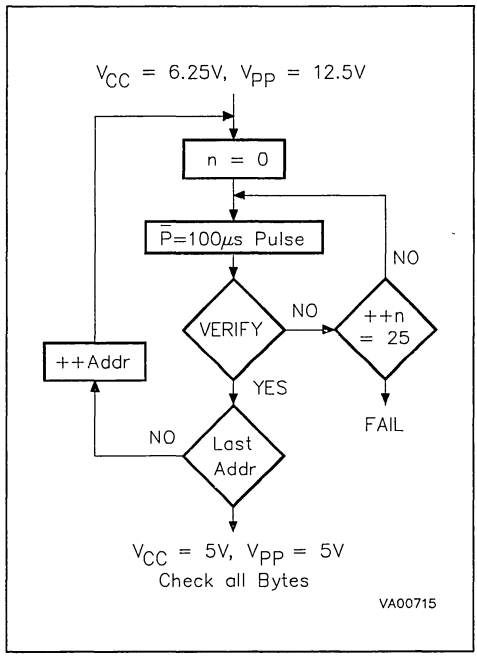
The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

The M27V101 has been designed to be fully compatible with the M27C1001. As a result the M27V101 can be programmed as the M27C1001 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27V101 has the same electronic signature and uses the same PRESTO II algorithm .

When delivered (and after each erasure for UV EPROM), all bits of the M27V101 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27V101 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in around 12 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V101s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27V101 may be common. A TTL low level pulse applied to a M27V101's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27V101. A high level $\overline{E}$ input inhibits the other M27V101s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V101. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V101, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

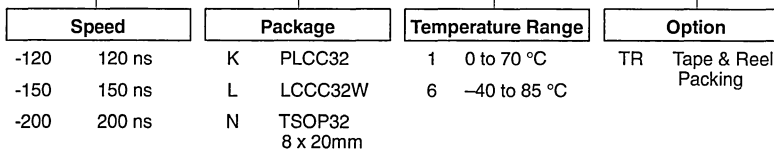
Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27V101, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7. Note that the M27V101 and M27C1001 have the same identifier bytes .

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27V101 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V101 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V101 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V101 window to prevent unintentional erasure. The recommended erasure procedure for the M27V101 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27V101 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27V101 -200 K 6 TR



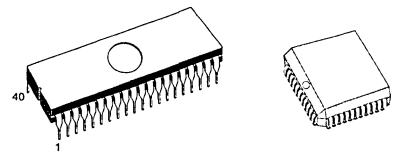
Speed		Package		Temperature Range		Option	
-120	120 ns	K	PLCC32	1	0 to 70 °C	TR	Tape & Reel Packing
-150	150 ns	L	LCCC32W	6	–40 to 85 °C		
-200	200 ns	N	TSOP32 8 x 20mm				

For a list of available options (Speed, Package, Temperature Range, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 1Megabit (64K x16) UV EPROM and OTP ROM

- FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 35mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIME of AROUND 6 sec. (PRESTO II ALGORITHM)



FDIP40W (F)

PLCC44 (C)

DESCRIPTION

The M27C1024 is a 1 Megabit UV erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 16 bits.

The 40 pin Ceramic Frit Seal Window package has a transparent lid whide allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For application where the content is programmed only one time and erasure is not required, the M27C1024 is offered in a Plastic Leaded Chip Carrier package.

Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q15	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

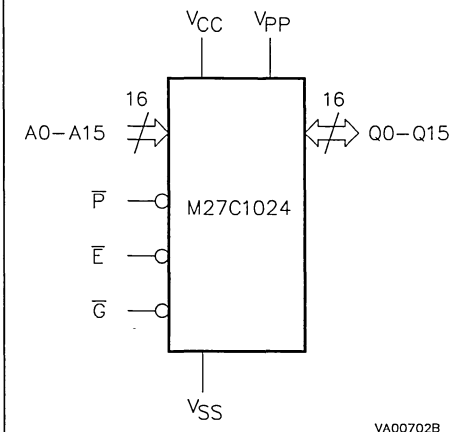
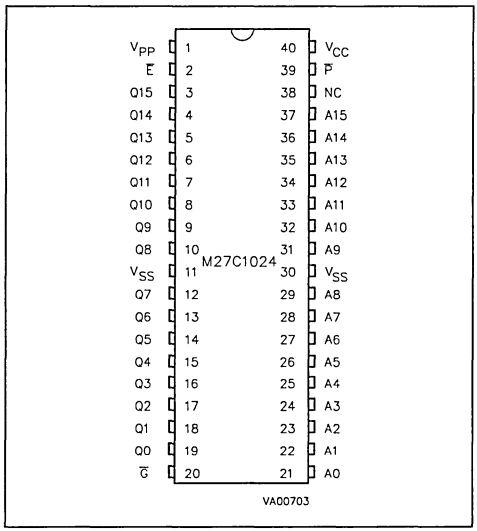
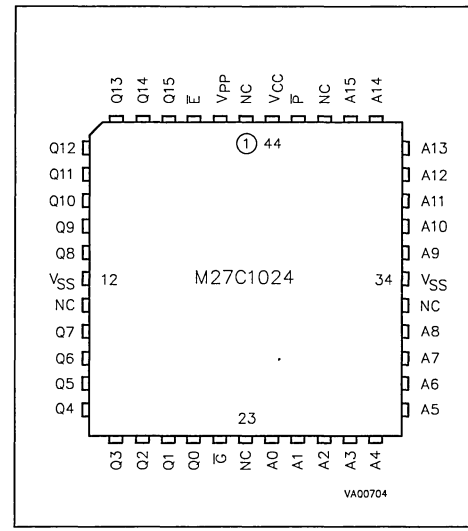


Figure 2A. DIP Pin Connections



Warning: NC = No Connection.

Figure 2B. LCC Pin Connections



Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operations of the M27C1024 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for Vpp and 12V on A9 for Electronic Signature.

Read Mode

The M27C1024 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{OE} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C1024 has a standby mode which reduces the active current from 35 mA to 100 µA.

DEVICE OPERATION (cont'd)

The M27C1024 is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between Vcc and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C1024 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C1024 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied, 16 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q15
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Data Output
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	X	V_{IL} Pulse	X	V_{PP}	Data Input
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Output
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ±0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	1	1	0	0	8Ch

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

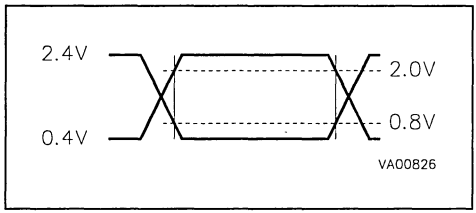


Figure 4. AC Testing Load Circuit

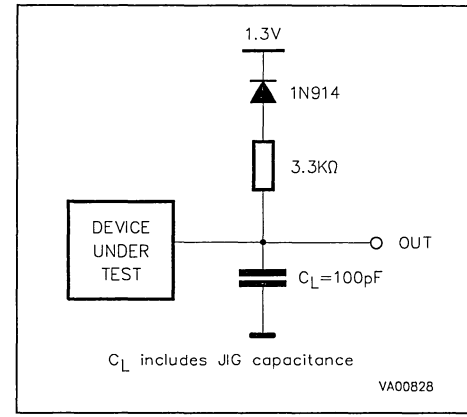


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

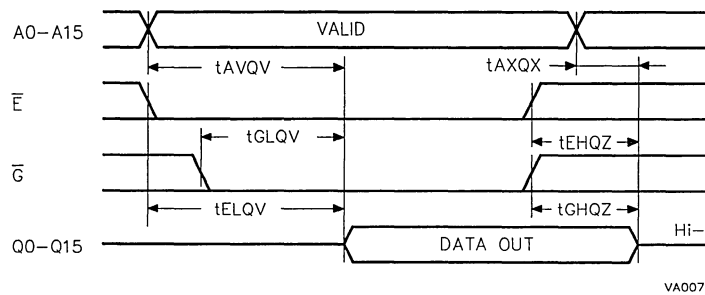


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz		35	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1024						Unit
				-80		-90		-10		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		80		90		100	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		80		90		100	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		40		45		50	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1024						Unit
				-12		-15		-20/-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		60		60		70	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	40	0	50	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	40	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

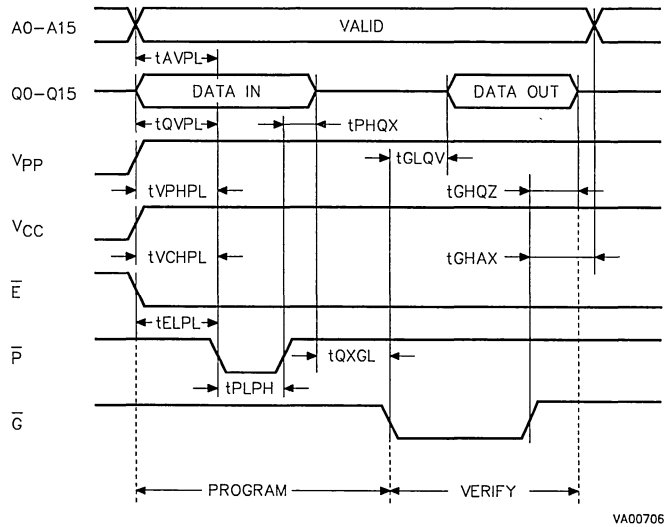
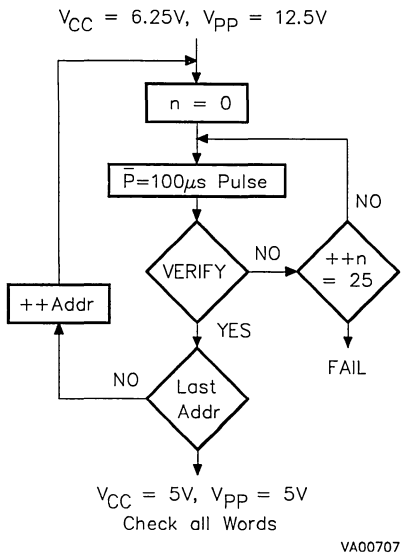


Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows programming of the whole array with a guaranteed margin, in a typical time of less than 6 seconds. Programming with PRESTO II consists of applying a sequence of 100 µs program pulses to each word until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C1024s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C1024 may be common. A TTL low level pulse applied to a M27C1024's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C1024. A high level $\overline{E}$ input inhibits the other M27C1024s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C1024. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C1024 with V_{PP} = V_{CC} = 5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C1024, these two iden-tifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C1024 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C1024 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C1024 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1024 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1024 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C1024 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C1024 -12 X F 1 X

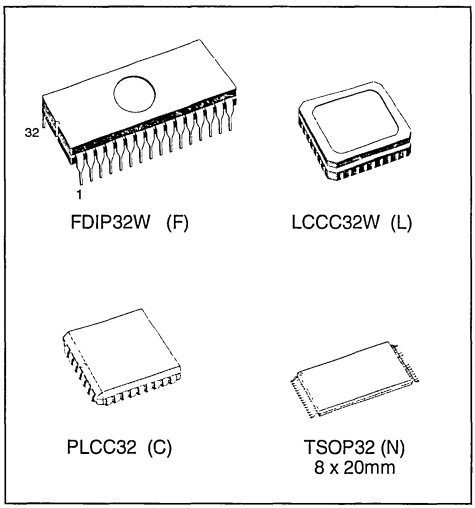
Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-80	80ns	X	± 5%	F	FDIP40W	1	0 to 70 °C	X	Additional Burn-in
-90	90ns	blank	± 10%	C	PLCC44	6	–40 to 85 °C	TR	Tape & Reel Packing
-10	100ns								
-12	120ns								
-15	150ns								
-20	200ns								
-25	250ns								

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 2 Megabit (256K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 24sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C2001 is a high speed 2 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 262,144 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C2001 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

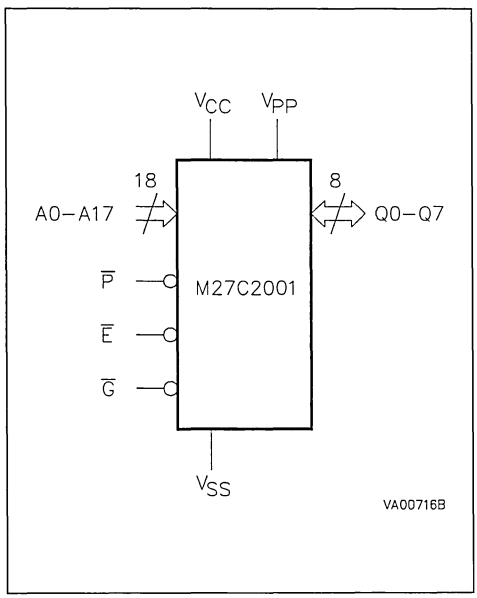


Figure 2A. DIP Pin Connections

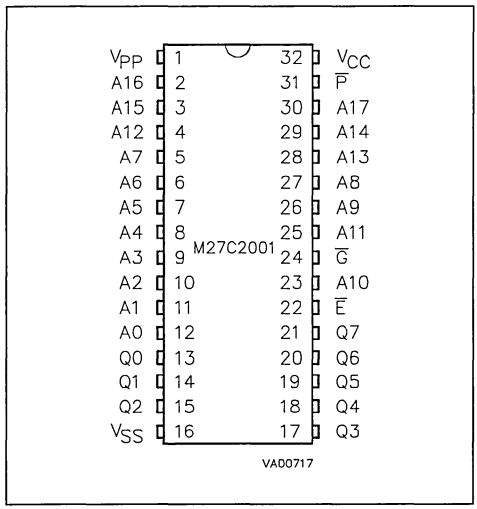


Figure 2B. LCC Pin Connections

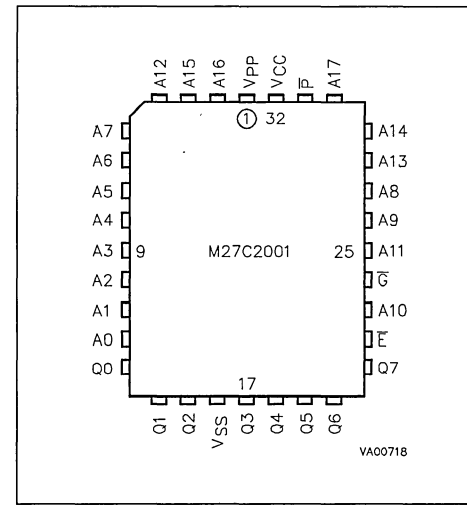
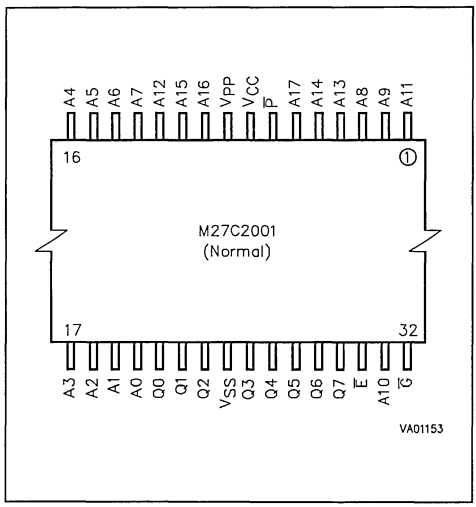


Figure 2C. TSOP Pin Connections



Note: This is advance information on a new product now in development. Details are subject to change without notice.

DEVICE OPERATION

The modes of operations of the M27C2001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

Read Mode

The M27C2001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C2001 has a standby mode which reduces the active current from 30mA to 100µA. The M27C2001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,
b. complete assurance that output bus contention will not occur.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	1	0	0	0	0	1	61h

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

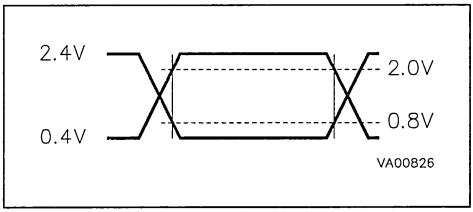


Figure 4. AC Testing Load Circuit

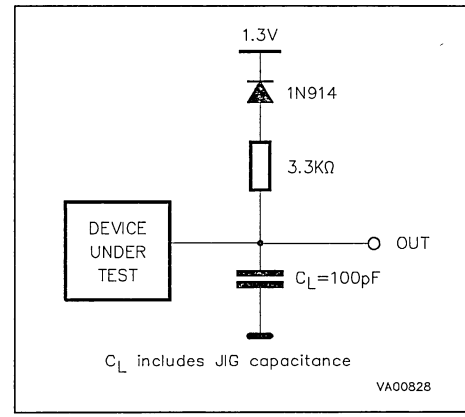


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C2001						Unit
				-80		-10		-12		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		80		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		80		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		50		50	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	30	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C2001						Unit
				-15		-20		-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		60		70		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	50	0	60	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

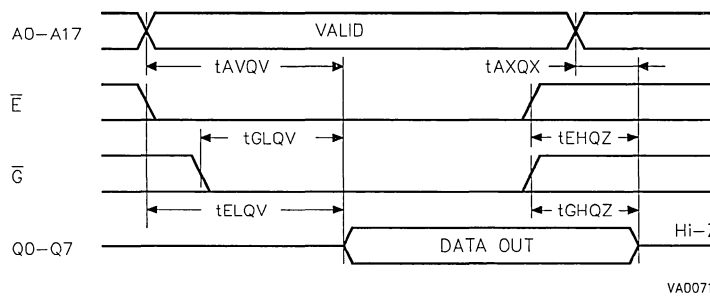


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

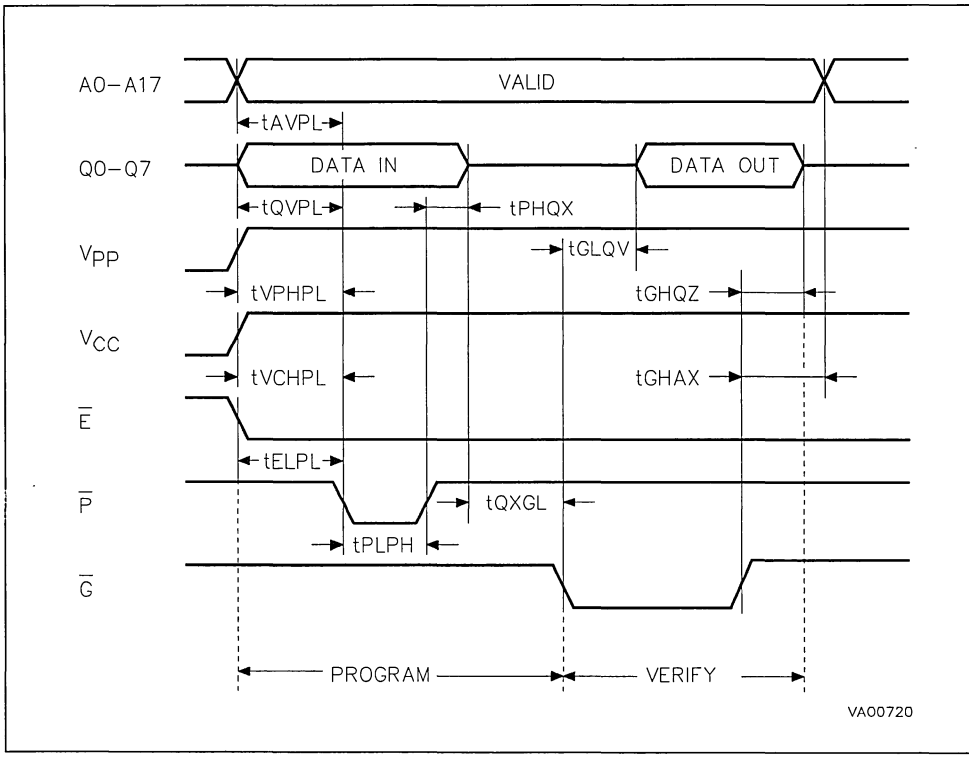
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



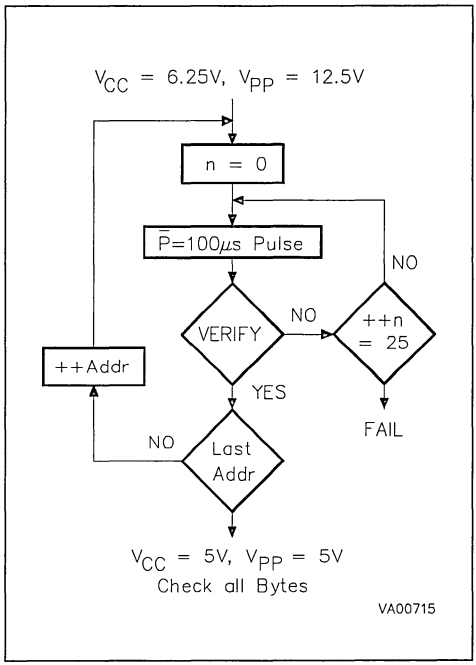
DEVICE OPERATION (cont'd)

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C2001 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C2001 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 24 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C2001s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C2001 may be common. A TTL low level pulse applied to a M27C2001's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C2001. A high level $\overline{E}$ input inhibits the other M27C2001s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C2001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C2001 with $V_{PP}=V_{CC}=5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C2001, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C2001 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C2001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C2001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C2001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C2001 is exposure to short wave ultraviolet light which has wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C2001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C2001 -80 X F 1 X

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-80	80 ns	X	± 5%	F	FDIP32W	1	0 to 70 °C	X	Additional Burn-in
-10	100 ns	blank	± 10%	C	PLCC32	6	–40 to 85 °C	TR	Tape & Reel Packing
-12	120 ns			L	LCCC32W				
-15	150 ns			N	TSOP32 8 x 20mm				
-20	200 ns								
-25	250 ns								

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

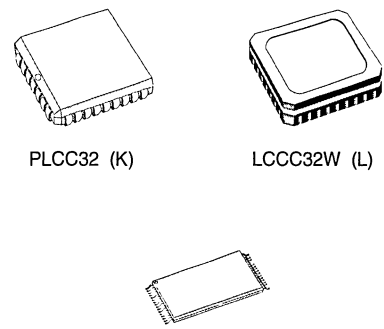
For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SGS-THOMSON MICROELECTRONICS

M27V201

LOW VOLTAGE CMOS 2 Megabit (256K x 8) UV EPROM and OTP ROM

- LOW VOLTAGE READ OPERATION
  - V_{CC} Range: 3V to 5.5V (T_A = 0 to 70°C)
  - V_{CC} Range: 3.2V to 5.5V (T_A = –40 to 85°C)
- ACCESS TIME: 200 and 250ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES for SURFACE MOUNTING:
  - Ceramic: LCCC32W, ultra-thin 2.8mm (max) height
  - Plastic: PLCC32 and TSOP32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 24sec. (PRESTO II ALGORITHM)
- M27V201 is PROGRAMMABLE as M27C2001 with IDENTICAL SIGNATURE



PLCC32 (K)

LCCC32W (L)

TSOP32 (N)
8 x 20mm

DESCRIPTION

The M27V201 is a low voltage, low power 2 Megabit electrically programmable memory (EPROM), ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 262,144 by 8 bits.

The M27V201 operates in the read mode with a supply voltage as low as 3V (3.2V between –40 to 85°C). The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

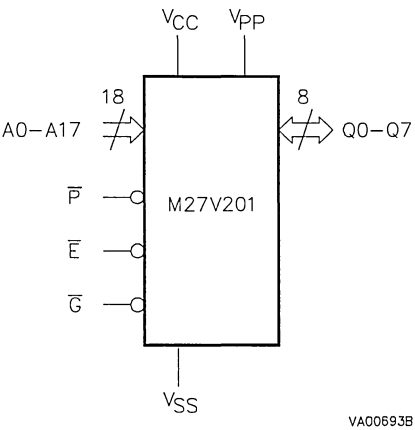


Figure 2A. LCC Pin Connections

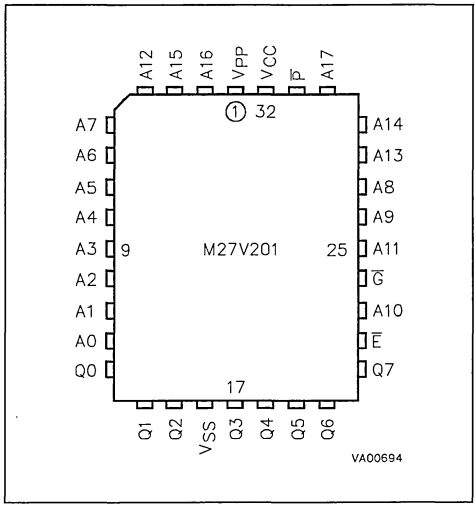
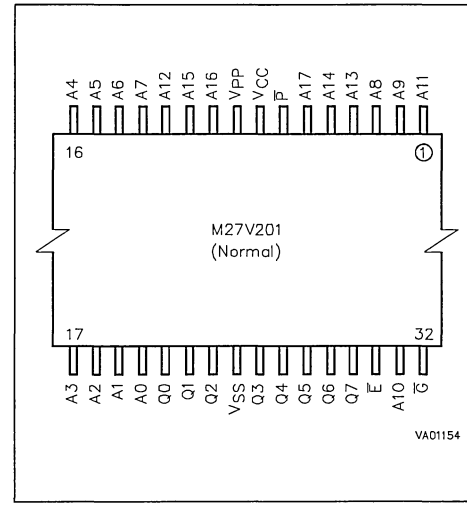


Figure 2B. TSOP Pin Connections



Note: This is advance information on a new product now in development. Details are subject to change without notice.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DESCRIPTION (cont'd)

The M27V201 can also be operated as a standard 2 Megabit EPROM (similar to M27C2001) with a 5V power supply .

The 32 pin Window, Leadless Chip Carrier package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure. For applications where the content is programmed only one time and erasure is not required, the M27V201 is offered in both Plastic Leaded Chip Carrier and Plastic thin Small Outline packages.

DEVICE OPERATION

The modes of operation of the M27V201 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27V201 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V201 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation $V_{CC} \leq 3.2V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V201 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer:

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: $X = V_{IH}$ or V_{IL}, $V_{ID} = 12V \pm 0.5V$

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	1	0	0	0	0	1	61h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

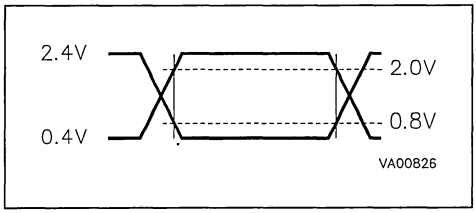


Figure 4. AC Testing Load Circuit

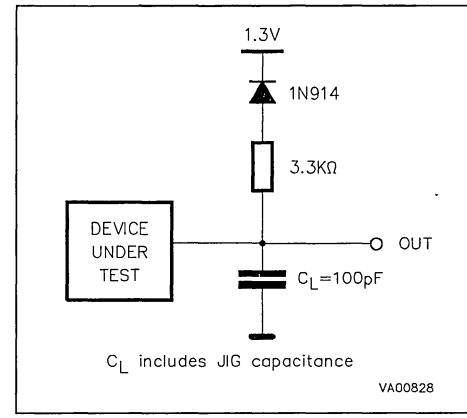


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} ≤ 3.2V		15	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 3.2V		20	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27V201				Unit
				-200		-250		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		100		120	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	80	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	80	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

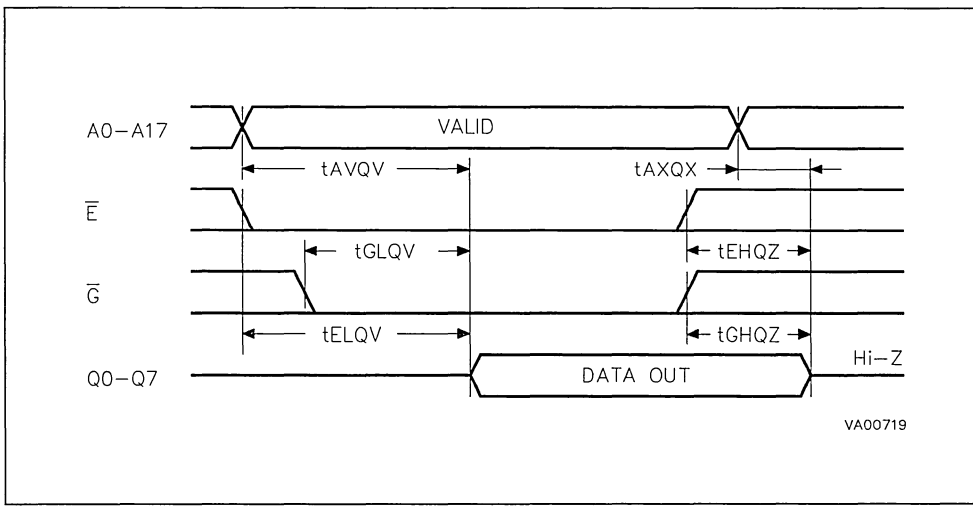


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

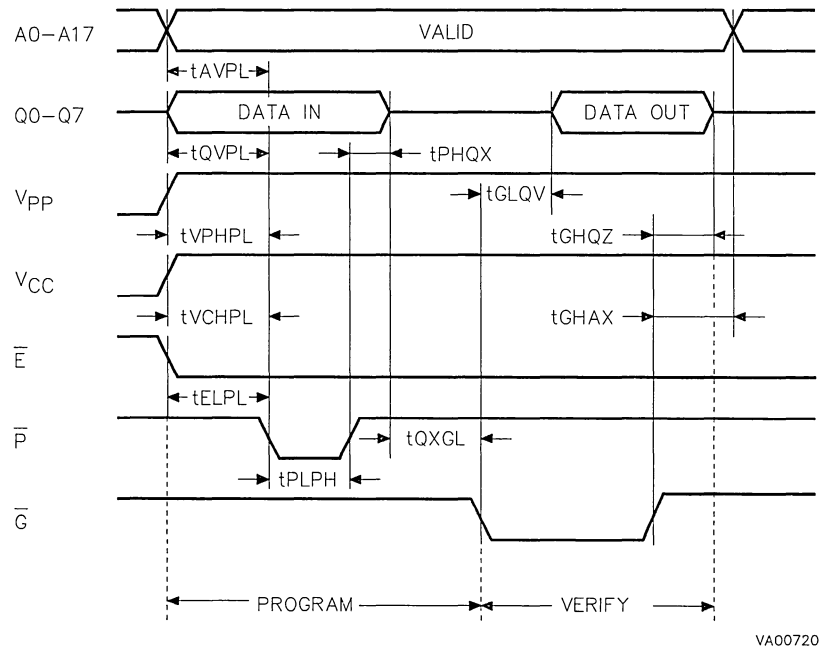
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



DEVICE OPERATION (cont'd)

the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

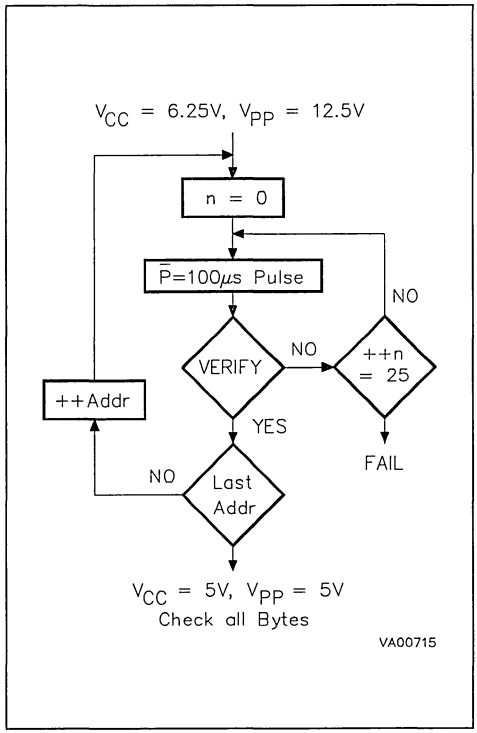
The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

The M27V201 has been designed to be fully compatible with the M27C2001. As a result the M27V201 can be programmed as the M27C2001 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27V201 has the same electronic signature and uses the same PRESTO II algorithm .

When delivered (and after each erasure for UV EPROM), all bits of the M27V201 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27V201 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in around 26 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V201s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27V201 may be common. A TTL low level pulse applied to a M27V201's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27V201. A high level $\overline{E}$ input inhibits the other M27V201s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

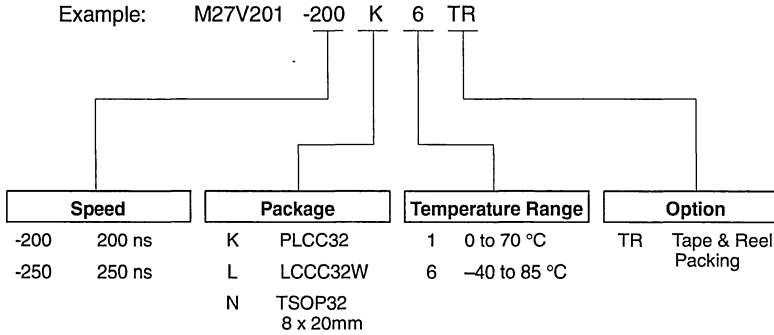
The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V201. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V201, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27V201, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7. Note that the M27V201 and M27C2001 have the same identifier bytes .

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27V201 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V201 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V201 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V201 window to prevent unintentional erasure. The recommended erasure procedure for the M27V201 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27V201 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

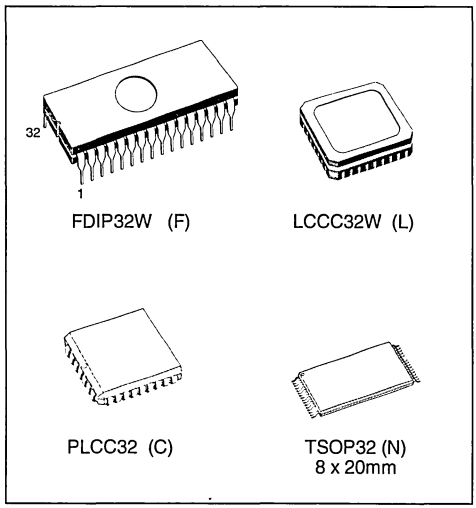


For a list of available options (Speed, Package, Temperature Range, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 4 Megabit (512K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA at 5MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 48sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C4001 is a high speed 4 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 524,288 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C4001 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Table 1. Signal Names

A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

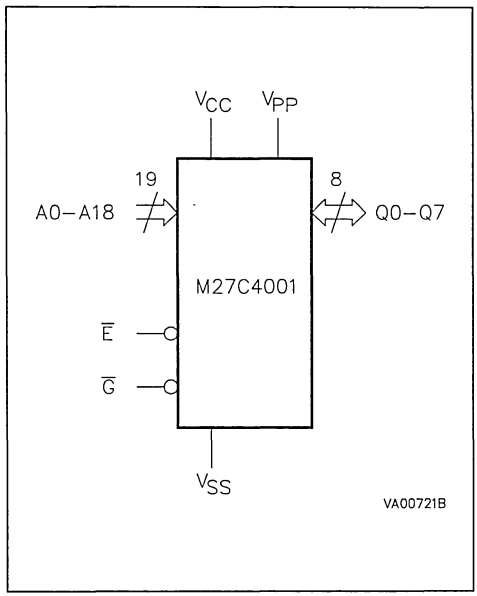


Figure 2A. DIP Pin Connections

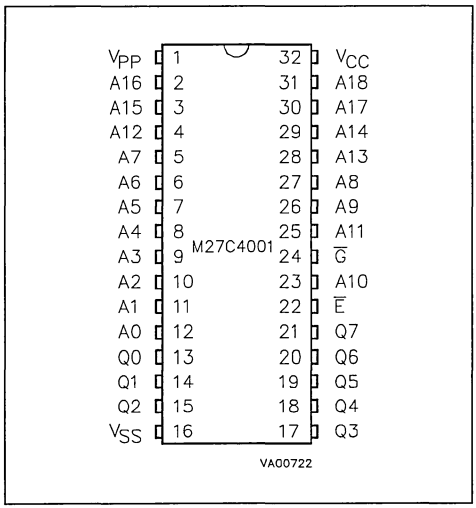


Figure 2B. LCC Pin Connections

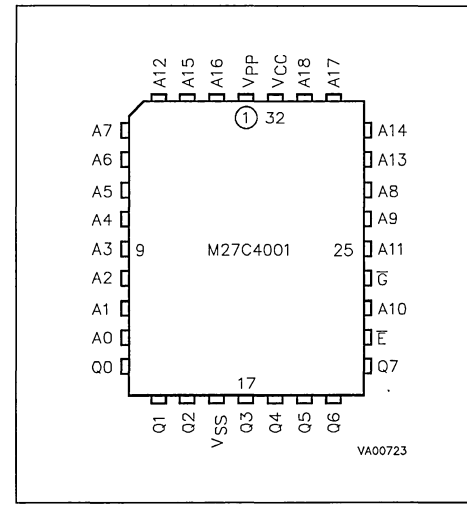
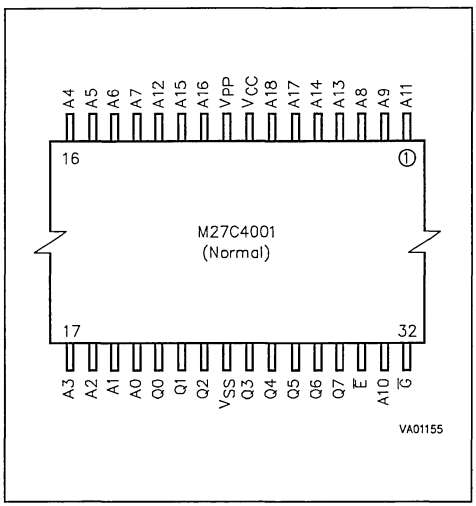


Figure 2C. TSOP Pin Connections



Note: This is advance information on a new product now in development. Details are subject to change without notice.

DEVICE OPERATION

The modes of operations of the M27C4001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

Read Mode

The M27C4001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C4001 has a standby mode which reduces the active current from 50mA to 100µA. The M27C4001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,
b. complete assurance that output bus contention will not occur.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	0	0	1	41h

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

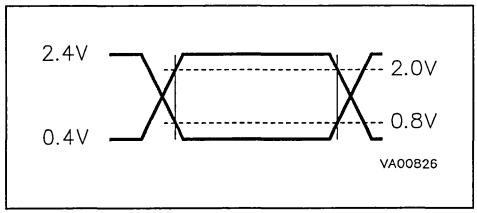


Figure 4. AC Testing Load Circuit

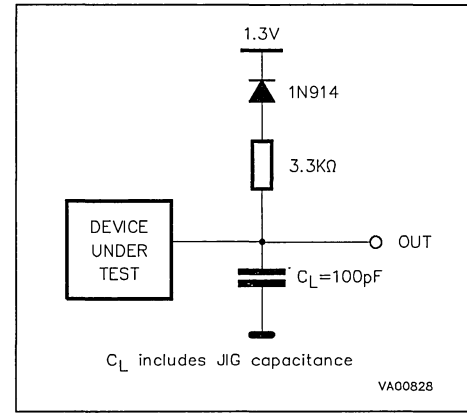


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

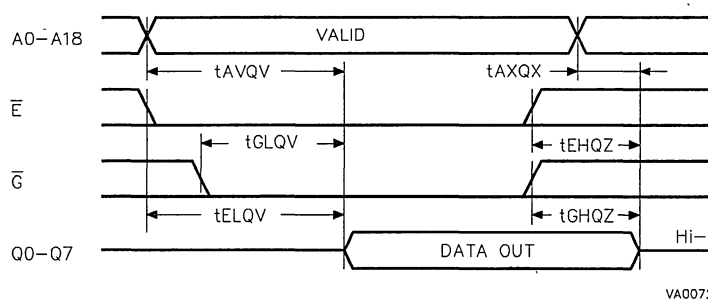


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4001						Unit
				-80		-10		-12		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		80		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		80		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		40		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4001				Unis
				-15		-20		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		60		70	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

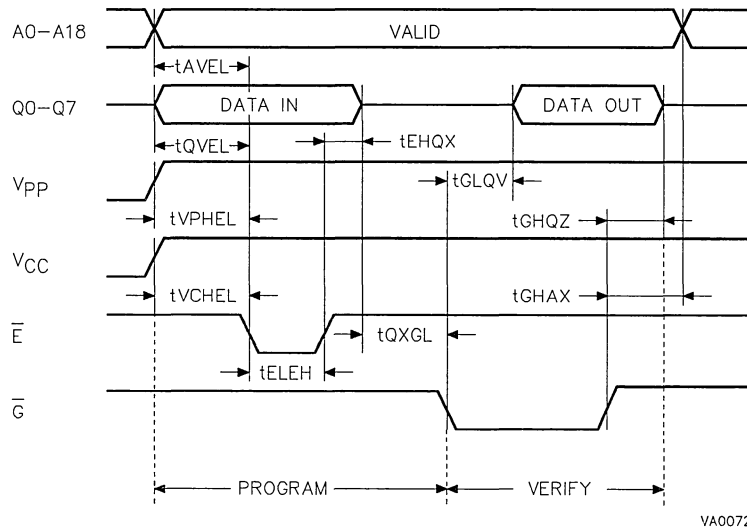
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



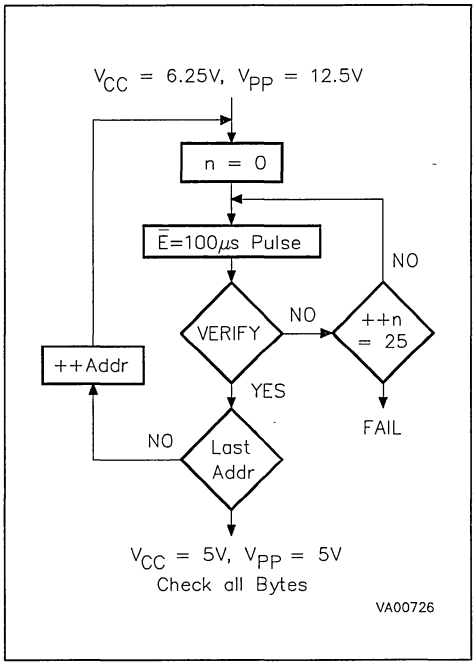
DEVICE OPERATION (cont'd)

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C4001 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C4001 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 52 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C4001s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C4001 may be common. A TTL low level pulse applied to a M27C4001's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27C4001. A high level $\overline{E}$ input inhibits the other M27C4001s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C4001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C4001 with V_{PP}=V_{CC}=5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C4001, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C4001 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C4001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C4001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C4001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C4001 is exposure to short wave ultraviolet light which has wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C4001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C4001 -80 X F 1 X

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-80	80 ns	X	± 5%	F	FDIP32W	1	0 to 70 °C	X	Additional Burn-in
-10	100 ns	blank	± 10%	C	PLCC32	6	–40 to 85 °C	TR	Tape & Reel Packing
-12	120 ns			L	LCCC32W				
-15	150 ns			N	TSOP32 8 x 20mm				
-20	200 ns								

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

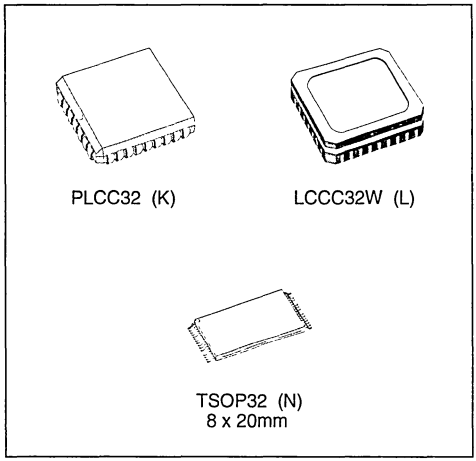
For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SGS-THOMSON MICROELECTRONICS

M27V401

LOW VOLTAGE CMOS 4 Megabit (512K x 8) UV EPROM and OTP ROM

- LOW VOLTAGE READ OPERATION
  - V_{CC} Range: 3V to 5.5V (T_A = 0 to 70°C)
  - V_{CC} Range: 3.2V to 5.5V (T_A = –40 to 85°C)
- ACCESS TIME: 200 and 250ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES for SURFACE MOUNTING:
  - Ceramic: LCCC32W, ultra-thin 2.8mm (max) height
  - Plastic: PLCC32 and TSOP32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 48sec. (PRESTO II ALGORITHM)
- M27V401 is PROGRAMMABLE as M27C4001 with IDENTICAL SIGNATURE



DESCRIPTION

The M27V401 is a low voltage, low power 4 Megabit electrically programmable memory (EPROM), ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 524,288 by 8 bits.

The M27V401 operates in the read mode with a supply voltage as low as 3V (3.2V between –40 to 85°C). The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

Table 1. Signal Names

A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

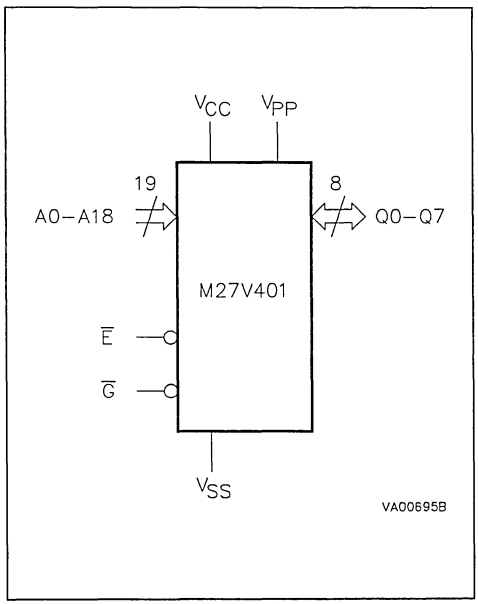


Figure 2A. LCC Pin Connections

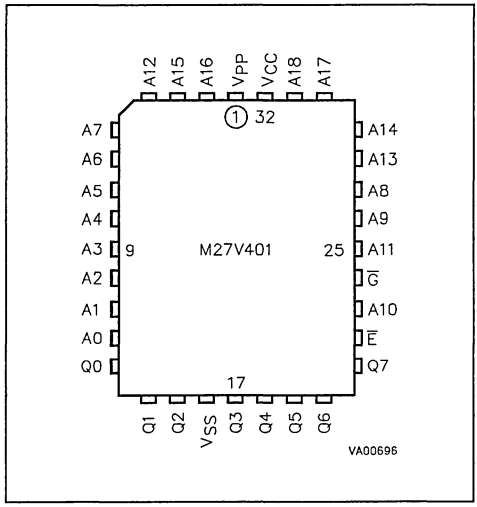
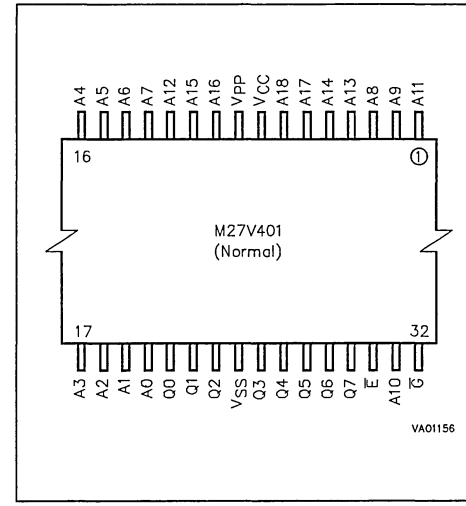


Figure 2B. TSOP Pin Connections



Note: This is advance information on a new product now in development. Details are subject to change without notice.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DESCRIPTION (cont'd)

The M27V401 can also be operated as a standard 4 Megabit EPROM (similar to M27C4001) with a 5V power supply .

The 32 pin Window, Leadless Chip Carrier package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure. For applications where the content is programmed only one time and erasure is not required, the M27V401 is offered in both Plastic Leaded Chip Carrier and Plastic thin Small Outline packages.

DEVICE OPERATION

The modes of operation of the M27V401 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27V401 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V401 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation $V_{CC} \leq 3.2V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V401 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	0	0	1	41h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

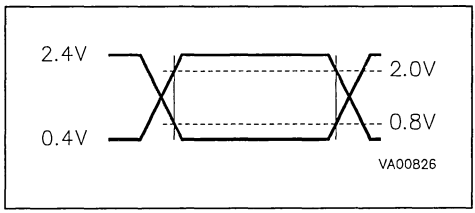


Figure 4. AC Testing Load Circuit

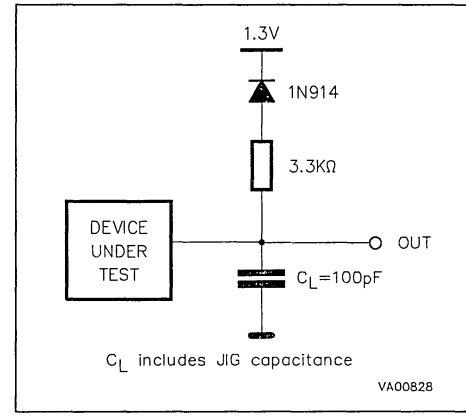


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} ≤ 3.2V		15	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 3.2V		20	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27V401				Unit
				-200		-250		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		130		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	80	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	80	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested..

Figure 5. Read Mode AC Waveforms

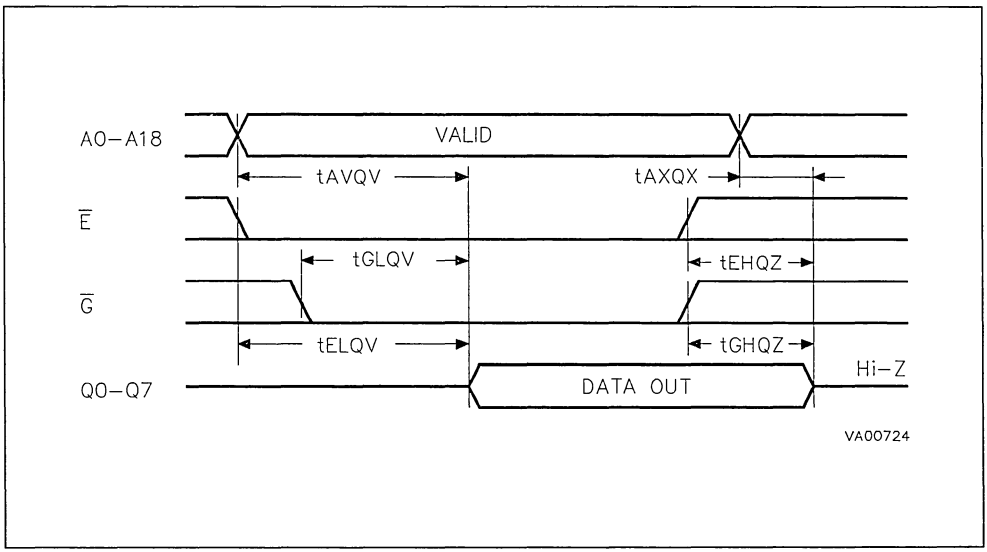


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

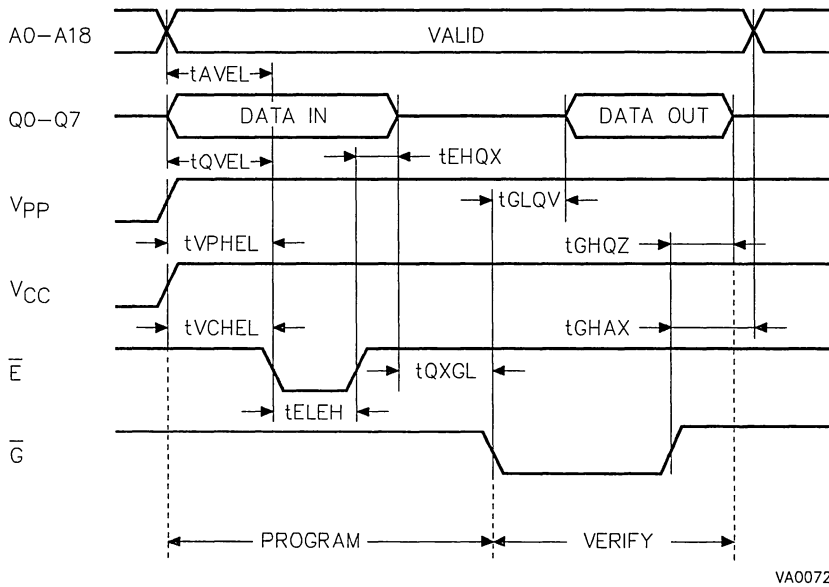
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested..

Figure 6. Programming and Verify Modes AC Waveforms



DEVICE OPERATION (cont'd)

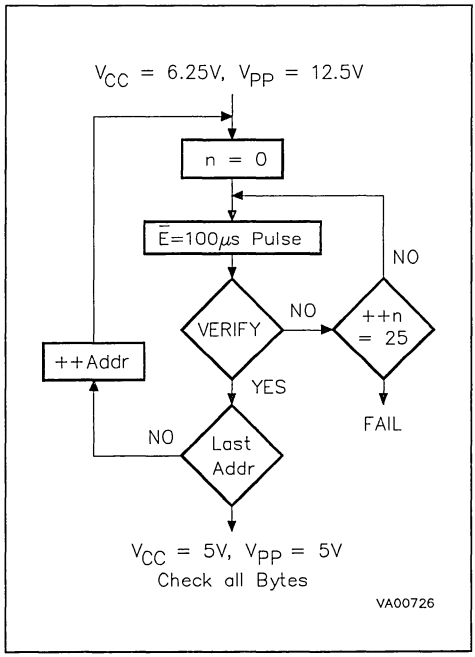
The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

The M27V401 has been designed to be fully compatible with the M27C4001. As a result the M27V401 can be programmed as the M27C4001 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27V401 has the same electronic signature and uses the same PRESTO II algorithm .

When delivered (and after each erasure for UV EPROM), all bits of the M27V401 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27V401 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in around 52 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V401s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27V401 may be common. A TTL low level pulse applied to a M27V401's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27V401. A high level $\overline{E}$ input inhibits the other M27V401s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH},, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

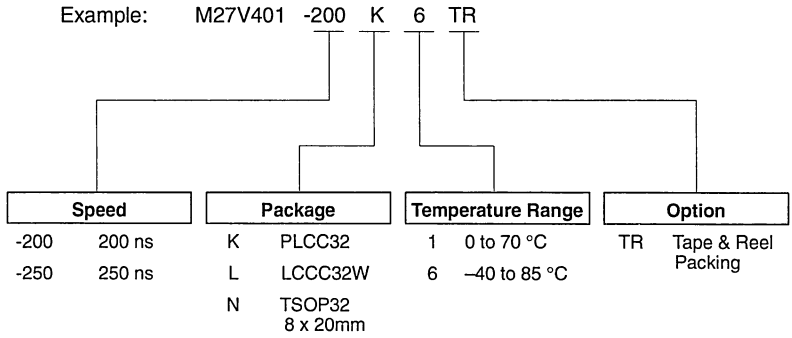
The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V401. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V401, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27V401, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7. Note that the M27V401 and M27C4001 have the same identifier bytes .

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27V401 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V401 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V401 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V401 window to prevent unintentional erasure. The recommended erasure procedure for the M27V401 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27V401 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

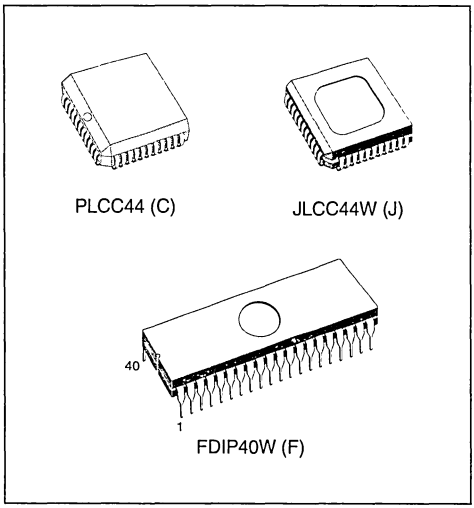


For a list of available options (Speed, Package, Temperature Range, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 4 Megabit (256K x 16) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 50mA at 5MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 24sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C4002 is a high speed 4 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 262,144 by 16 bits.

The Window Ceramic Frit-Seal Dual-in-Line and J-Lead Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C4002 is offered in Plastic Leaded Chip Carrier package.

Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q15	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

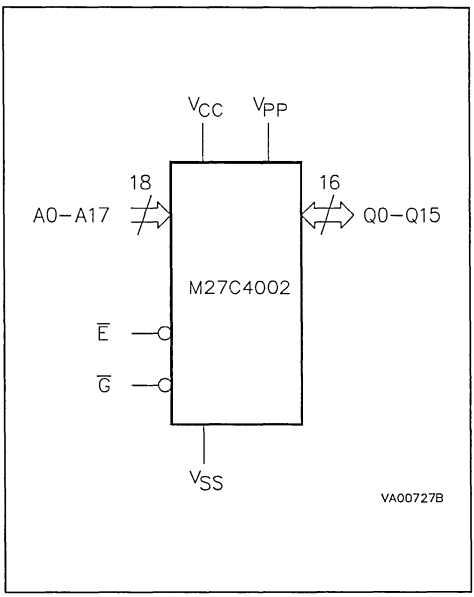


Figure 2A. DIP Pin Connections

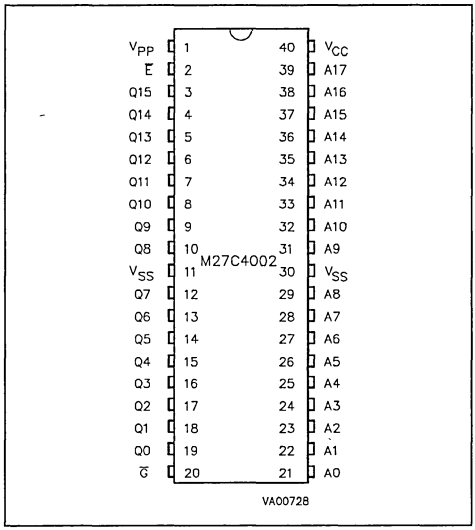
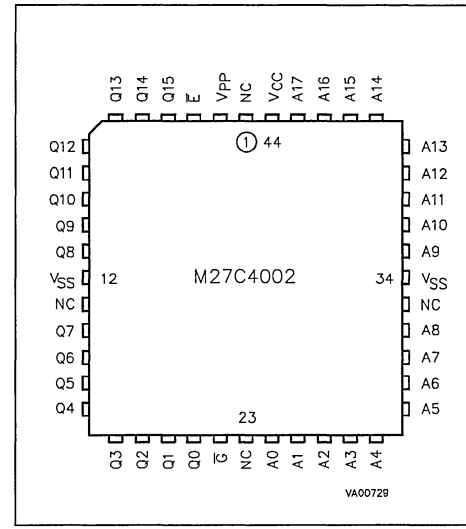


Figure 2B. LCC Pin Connections



Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operations of the M27C4002 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C4002 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C4002 has a standby mode which reduces the active current from 50mA to 100µA. The

DEVICE OPERATION (cont'd)

M27C4002 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the output capacitive and inductive loading of the device.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C4002 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C4002 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q15
Read	V_{IL}	V_{IL}	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	1	0	0	44h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

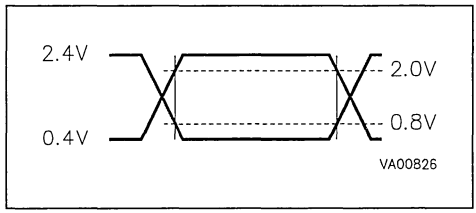


Figure 4. AC Testing Load Circuit

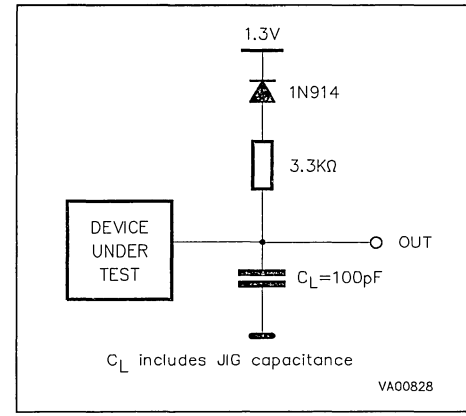


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

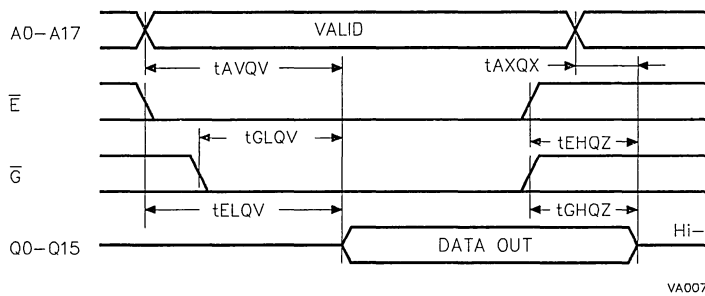


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 10MHz		70	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Maximum DC voltage on Output is V_{CC} +0 5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4002						Unit
				-80		-10		-12		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		80		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		80		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		40		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4002				Unit
				-15		-20		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		60		70	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

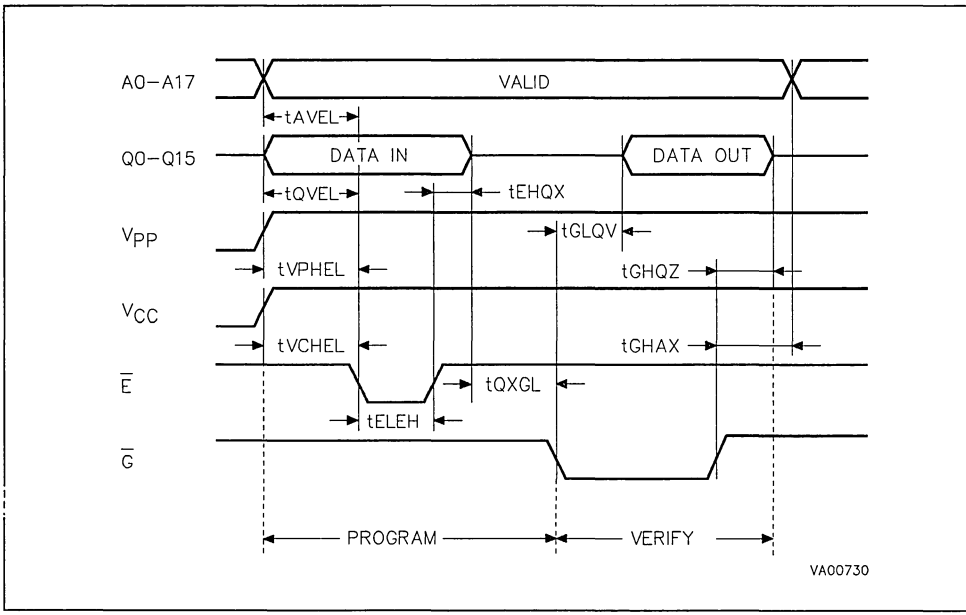
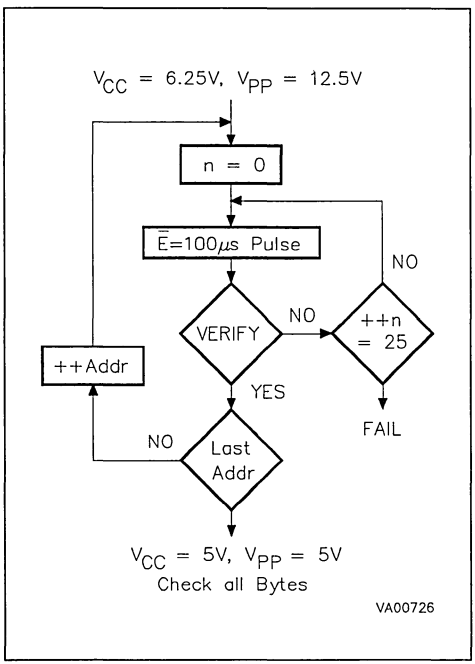


Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 24 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C4002s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C4002 may be common. A TTL low level pulse applied to a M27C4002's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27C4002. A high level $\overline{E}$ input inhibits the other M27C4002s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C4002. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C4002 with $V_{PP}=V_{CC}=5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C4002, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C4002 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C4002 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C4002 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C4002 window to prevent unintentional erasure. The recommended erasure procedure for the M27C4002 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 $\mu W/cm^2$ power rating. The M27C4002 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C4002 -10 X F 1 X

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-80	80 ns	X	± 5%	F	FDIP40W	1	0 to 70 °C	X	Additional Burn-in
-10	100 ns	blank	± 10%	C	PLCC44	6	–40 to 85 °C	TR	Tape & Reel Packing
-12	120 ns			J	JLCC44W				
-15	150 ns								
-20	200 ns								

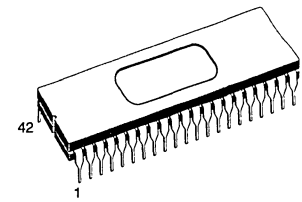
For a list of available options (Speed, V_{CC} Tolerance, Package etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 16 Megabit (2M x 8 or 1M x 16) UV EPROM

ADVANCE DATA

- FAST ACCESS TIME: 150ns
- WORD-WIDE or BYTE-WIDE CONFIGURABLE
- 16 Megabit, 42 Pin, MASK ROM COMPATIBLE
- LOW POWER CONSUMPTION
  - Active Current 70mA at 8MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE 12.5V ± 0.3V
- PROGRAMMING TIME of AROUND 10sec. (PRESTO III ALGORITHM)



FDIP42W (F)

DESCRIPTION

The M27C160 is a 16 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large data or program storage. It is organised as either 2M words of 8 bit or 1M words of 16 bit. The pin-out is compatible with a 16 Megabit Mask ROM.

The 42 pin Window Ceramic Frit-Seal package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written rapidly to the device by following the programming procedure.

Table 1. Signal Names

A0 - A19	Address Inputs
Q0 - Q7	Data Outputs
Q8 - Q14	Data Outputs
Q15A-1	Data Output / Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{BYTE}V_{PP}$	Byte Mode / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

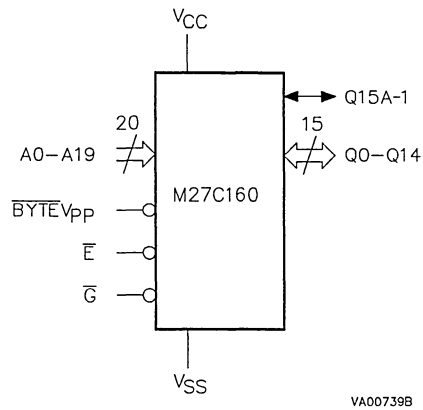


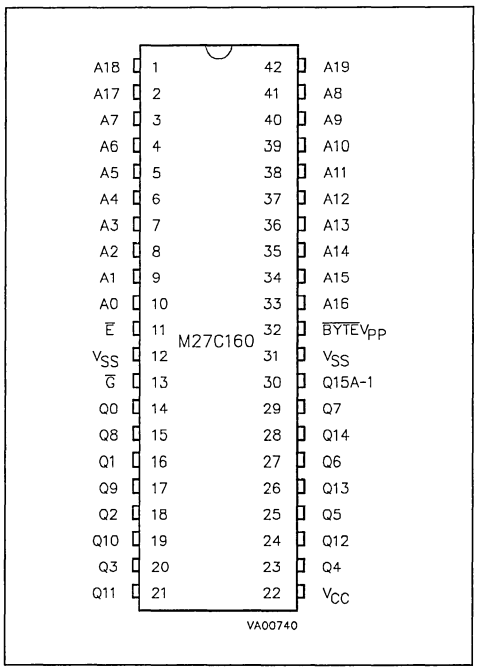
Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The operating modes of the M27C160 are listed in the Operating Modes Table. A single 5V supply is required in the read mode. All inputs are TTL compatible except for V_{PP} and 12V on A9 for the Electronic Signature.

Read Mode

The M27C160 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the $\overline{BYTE}V_{PP}$ pin. When $\overline{BYTE}V_{PP}$ is at V_{IH} the Word-wide organisation is selected and the Q15A-1 pin is used for Q15 Data Output. When the $\overline{BYTE}V_{PP}$ pin is at V_{IL} the Byte-wide organisation is selected and the Q15A-1 pin is used for the Address Input A-1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A-1 at V_{IL} the lower 8 bits of the 16 bit data are selected and with A-1 at V_{IH} the upper 8 bits of the 16 bit data are selected.

The M27C160 has two control inputs, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte-wide organisation must be selected. The $\overline{E}$ signal is the power control and should be used for device selection. The $\overline{G}$ signal is the output control and should be used to gate data to the output pins. With $\overline{E}=V_{IL}$ and $\overline{G}=V_{IL}$ the output data will be valid in a time t_{AVQV} after the all address lines are valid and stable. The Chip Enable to Output Valid time t_{ELQV} is equal to the Address Valid to output Valid time t_{AVQV}. When the Addresses are valid and $\overline{E}=V_{IL}$, the output data is valid after a time of t_{GLQV} from the falling edge of the Output Enable signal.

Standby Mode

The M27C160 has a standby mode which reduces the active current from 50mA (f = 5MHz) to 100µA. The standby mode is entered by applying a CMOS high level V_{CC} –0.2V to $\overline{E}$. When in the standby mode the outputs are in an high impedance state, independant of the $\overline{G}$ input level.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{BYTEV}_{PP}$	A9	Q0 - Q7	Q8 - Q14	Q15A-1
Read Word-wide	V_{IL}	V_{IL}	V_{IH}	X	Data Out	Data Out	Data Out
Read Byte-wide Upper	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IH}
Read Byte-wide Lower	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IL}
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z	Hi-Z	Hi-Z
Program	V_{IL} Pulse	V_{IH}	V_{PP}	X	Data In	Data In	Data In
Verify	X	V_{IL}	V_{PP}	X	Data Out	Data Out	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes	Codes	Code

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7 or Q15	Q6 or Q14	Q5 or Q13	Q4 or Q12	Q3 or Q11	Q2 or Q10	Q1 or Q9	Q0 or Q8	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	1	0	0	0	1	B1h

Table 5. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 8Mhz		70	mA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
I_{OS}	Output Short Circuit Current	Note 2 and 3		100	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (4)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V

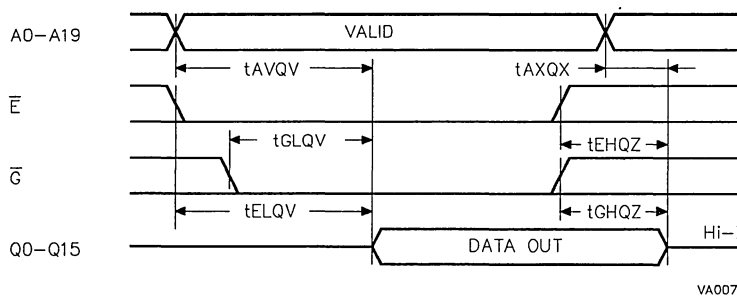
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. Sampled only, not 100% tested.
3. Output shortcircuited for no more than one second. No more than one output shorted at a time.
4. Maximum DC voltage on Output is V_{CC} +0.5V

Table 6. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C160				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{BHQV}	t_{ST}	BYTE High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		60		70	ns
t_{BLQZ} (2)	t_{STD}	BYTE Low to Output Hi-Z	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	50	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	5		5		ns
t_{BLQX}	t_{OH}	BYTE Low to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	5		5		ns

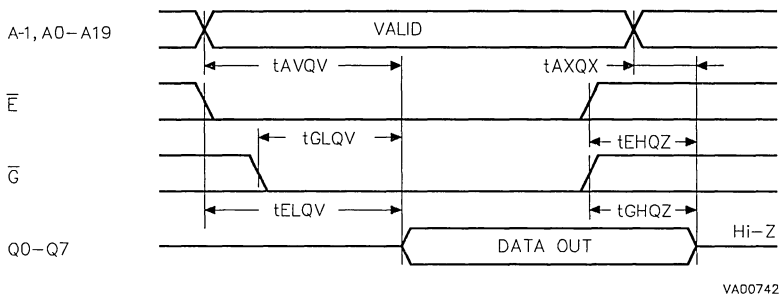
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Figure 3. Word-Wide Read Mode AC Waveforms



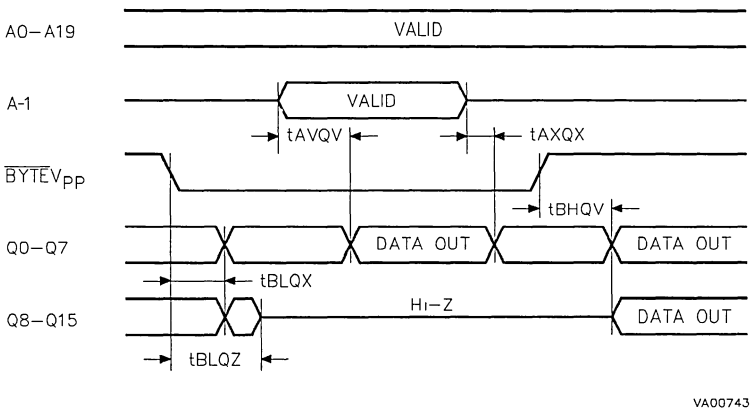
Note: $\overline{BYTE}/V_{PP}$ = V_{IH}

Figure 4. Byte-Wide Read Mode AC Waveforms



Note: $\overline{BYTE}V_{PP} = V_{IL}$

Figure 5. $\overline{BYTE}$ Transition AC Waveforms



Note: $\overline{E}$ and $\overline{G} = V_{IL}$

AC Measurement Conditions

Input Rise and Fall Times	< 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 6. AC Testing Input Output Waveforms

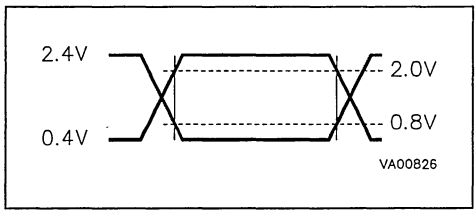


Figure 7. AC Testing Load Circuit

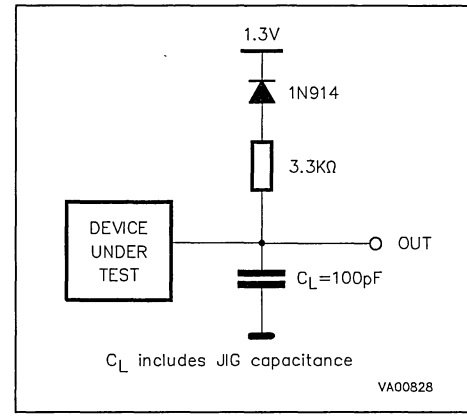


Table 7. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (except $\overline{BYTE}/V_{PP}$)	V_{IN} = 0V		10	pF
	Input Capacitance ($\overline{BYTE}/V_{PP}$)	V_{IN} = 0V		120	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±1	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.4	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	3.5		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHAV}	t_{VPS}	V_{PP} High to Address Valid		2		µs
t_{VCHAV}	t_{VCS}	V_{CC} High to Address Valid		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		9.5	10.5	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			120	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 8. Programming and Verify Modes AC Waveforms

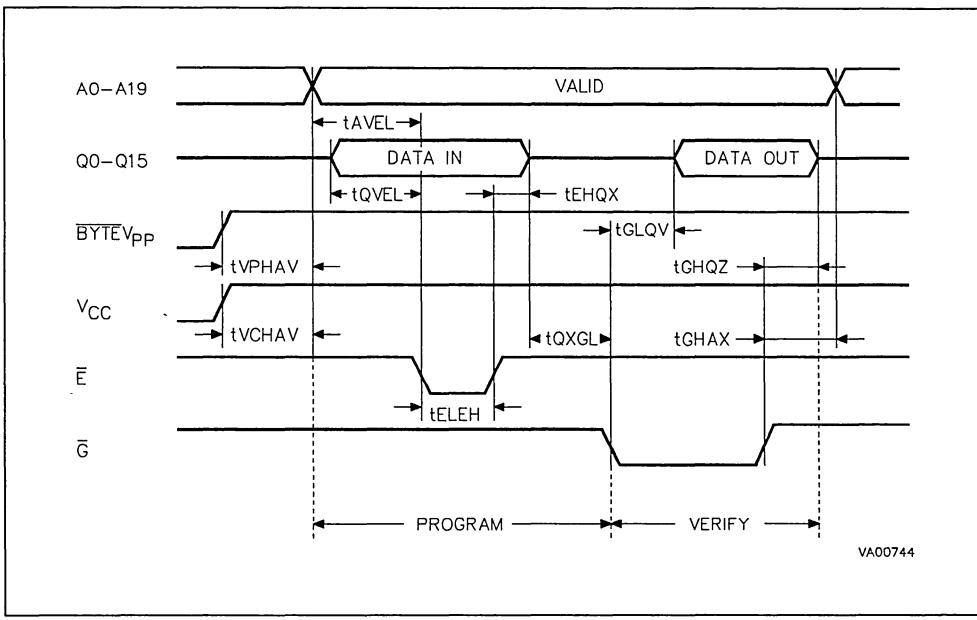
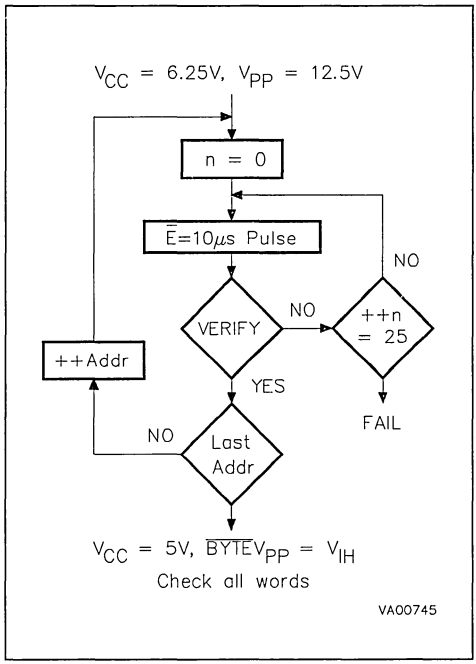


Figure 9. Programming Flowchart



Output Disable Mode

When EPROMs are used in memory arrays two line output control should be used. This function uses the output disable mode which allows:

a. the lowest possible power consumption

b. complete assurance that output bus contention will not occur

For the best use of the two control lines $\overline{E}$ and $\overline{G}$, the input $\overline{E}$ should be decoded and used as the primary selection, while $\overline{G}$ should be made a common connection to all memories in the array. $\overline{G}$ should be connected to the $\overline{READ}$ signal of the system bus. This will ensure that all deselected devices are in the low power standby mode and that the output lines are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require carefull decoupliing of the supplies to the devices. The supply current I_{CC} has three segments of importance to the system designer: the standby current, the active current and the transient peaks that are produced by the falling and rising edges of $\overline{E}$.

The magnitude of the transient current peaks is dependant on the capacititive and inductive loading of the device outputs. The associated transient voltage peaks can be supressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor is used on every device between V_{CC} and V_{SS}. This should be a high frequency type of low inherent inductance and should be placed as close as possible to the device. In addition, a 4.7µF electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. This capacitor should be mounted near the power supply connection point. The purpose of this capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programing

When first delivered, and after erasure for UV EPROMs, all bits are in the "1" logic state (Output High). Data with both "1's" and "0's" is applied and the "0s'" are programed into the memory array. For programing V_{CC} is raised to 6.25V. The M27C160 is in the Program Mode when V_{PP} is at 12.75V, $\overline{G}$ is at V_{IH} and $\overline{E}$ is pulsed to V_{IL}. Data to be programed is applied 16 bits in parallel to the data output pins Q0 - Q15.

PRESTO III Algorithm

The PRESTO III Algorithm allows the whole 16 Megabit array to be programed with a guaranteed margin in a typical time of less than 10 seconds. The algorithm applies a series of 10µs program pulses to each word until a correct verify is made. During programing and verify a MARGIN MODE circuit is automatically activated to guarantee that each cell is programed with an adequate margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the neccessary threshold margin for each cell.

Program Inhibit

Multiple M27C160s may be programed in parallel with different data. This is done by putting in parallel all inputs except $\overline{E}$ and $\overline{G}$. With V_{CC} at 6.25V and V_{PP} at 12.5V, data should be applied to all devices and $\overline{G}$ placed at V_{IH}. Low level pulses on the $\overline{E}$ of one device will program that device.

Program Verify

After each program pulse a verify read is made by reading the data output with V_{CC} at 6.25V, V_{PP} at 12.5V and $\overline{G}$ placed at V_{IL}.

Electronic Signature

The Electronic Signature Mode allows a binary code to be read from the EPROM which identifies the Manufacturer and Device Type. These codes are intended to be used to match the programing

equipment to the device being programed and its corresponding algorithm.

The Electronic Signature Mode is activated by applying a voltage V_{ID} of 12V to the Address line A9 and V_{IL} to all other Address lines, with $\overline{E}$ and $\overline{G}$ at V_{IL} and $\overline{BYTE}$ at V_{IH}. The identifier bytes may be read from either Q0-Q7 or Q8-Q15. With Address line A0 at V_{IL} the byte output is the Manufacture's code, with A0 at V_{IH} the byte identifies the Device Type. The codes for the SGS-THOMSON M27C160 are given in Table 4.

Erasure

The erasure of the M27C160 begins when the cells are exposed to light of wavelengths shorter than approximately 4000 Å. Sunlight and some types of fluorescent lamps have wavelengths in the 3000 - 4000 Å range. Constant exposure to room level fluorescent lighting could erase a typical EPROM in about 3 years, while it takes approximately 170 hours to cause erasure when exposed to direct sunlight. To prevent accidental erasure it is recommended that opaque labels be placed over the M27C160 window.

The erase procedure for the M27C160 is exposure to UV light with a wavelength of 2537 Å. The integrated dose (UV intensity x time) for erasure should be a minimum of 15 W-sec/cm^2. The erase time with this dosage is 15 to 20 minutes using an UV lamp with 12,000 µW/cm^2 rating. The M27C160 should be placed within 2.5cm of the lamp tube during erasure. No filter should be used on the lamp.

ORDERING INFORMATION SCHEME

Example: M27C160 -200 X F 1

Speed		V_{CC} Tolerance		Package		Temperature Range	
-150	150 ns	X	± 5%	F	FDIP42W	1	0 to 70 °C
-200	200 ns	blank	± 10%				

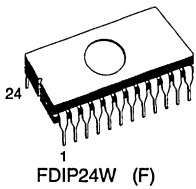
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

NMOS UV EPROM

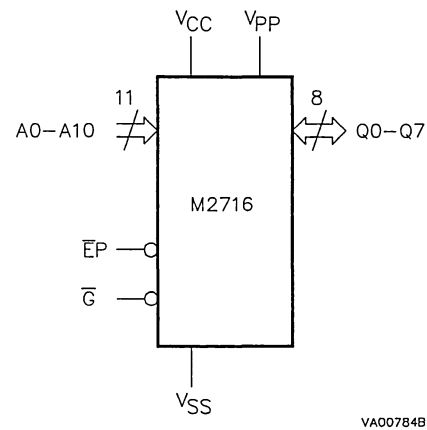
NMOS 16K (2K x 8) UV EPROM

- 2048 x 8 ORGANIZATION
- 525mW Max ACTIVE POWER, 132mW Max STANDBY POWER
- ACCESS TIME:
  - M2716-1 is 350ns
  - M2716 is 450ns
- SINGLE 5V SUPPLY VOLTAGE
- STATIC-NO CLOCKS REQUIRED
- INPUTS and OUTPUTS TTL COMPATIBLE DURING BOTH READ and PROGRAM MODES
- THREE-STATE OUTPUT with TIED-OR- CAPABILITY
- EXTENDED TEMPERATURE RANGE
- PROGRAMMING VOLTAGE: 25V



FDIP24W (F)

Figure 1. Logic Diagram



DESCRIPTION

The M2716 is a 16,384 bit UV erasable and electrically programmable memory EPROM, ideally suited for applications where fast turn around and pattern experimentation are important requirements.

The M2716 is housed in a 24 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Table 1. Signal Names

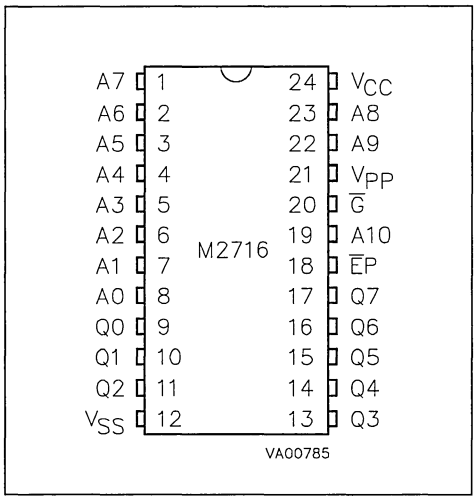
A0 - A10	Address Inputs
Q0 - Q7	Data Outputs
$\overline{EP}$	Chip Enable / Program
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{CC}	Supply Voltage		–0.3 to 6	V
V_{IO}	Input or Output Voltages		–0.3 to 6	V
V_{PP}	Program Supply		–0.3 to 26.5	V
P_D	Power Dissipation		1.5	W

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The M2716 has 3 modes of operation in the normal system environment. These are shown in Table 3.

Read Mode. The M2716 read operation requires that $\overline{G} = V_{IL}$, $\overline{EP} = V_{IL}$ and that addresses A0-A10 have been stabilized. Valid data will appear on the output pins after time t_{AVQV}, t_{GLQV} or t_{ELQV} (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode. The M2716 is deselected by making $\overline{G} = V_{IH}$. This mode is independent of $\overline{EP}$ and the condition of the addresses. The outputs are Hi-Z when $\overline{G} = V_{IH}$. This allows tied-OR of 2 or more M2716's for memory expansion.

Standby Mode (Power Down). The M2716 may be powered down to the standby mode by making $\overline{EP} = V_{IH}$. This is independent of $\overline{G}$ and automatically puts the outputs in the Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. V_{CC} and V_{PP} must be maintained at 5V. Access time at power up remains either t_{AVQV} or t_{ELQV} (see Switching Time Waveforms).

Programming

The M2716 is shipped from SGS-THOMSON completely erased. All bits will be at "1" level (output high) in this initial state and after any full erasure. Table 3 shows the 3 programming modes.

Program Mode. The M2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, sequential addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the $\overline{EP}$ pin. All input voltage levels including the program pulse on chip enable are TTL compatible.

The programming sequence is: with $V_{PP} = 25V$, $V_{CC} = 5V$, $\overline{G} = V_{IH}$ and $\overline{EP} = V_{IL}$, an address is selected and the desired data word is applied to the output pins (V_{IL} = "0" and V_{IH} = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a

DEVICE OPERATION (cont'd)

pulse width between 45ms and 55ms. Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or higher) must not be maintained longer than t_{PHPL} (max) on the program pin during programming. M2716's may be programmed in parallel in this mode.

Program Verify Mode. The programming of the M2716 may be verified either one byte at a time during the programming (as shown in Figure 6) or by reading all of the bytes out at the end of the programming sequence. This can be done with V_{PP} = 25V or 5V in either case. V_{PP} must be at 5V for all operating modes and can be maintained at 25V for all programming modes.

Program Inhibit Mode. The program inhibit mode allows several M2716's to be programmed simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the M2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{G}$ = V_{IH} will put its outputs in the Hi-Z state.

ERASURE OPERATION

The M2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the M2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

An ultraviolet source of 2537 Å yielding a total integrated dosage of 15 watt-seconds/cm^2 power rating is used. The M2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age, it is therefore important to periodically check that the UV system is in good order.

This will ensure that the EPROMs are being completely erased. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

Table 3. Operating Modes

Mode	$\overline{EP}$	$\overline{G}$	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{CC}	Data Out
Program	V_{IH} Pulse	V_{IH}	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{PP} or V_{CC}	Data Out
Program Inhibit	V_{IL}	V_{IH}	V_{PP}	Hi-Z
Deselect	X	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Note: X = V_{IH} or V_{IL}.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

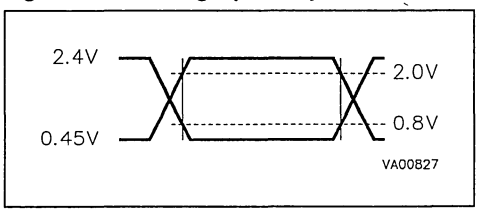


Figure 4. AC Testing Load Circuit

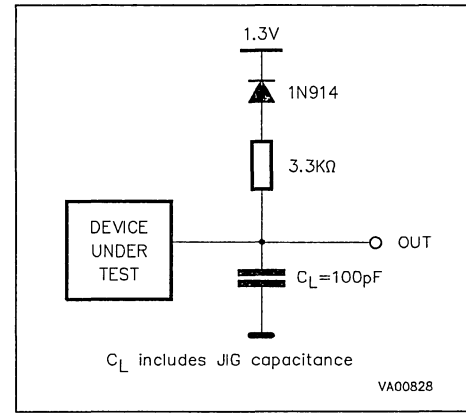


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$, $\overline{E}P = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E}P = V_{IL}$, $\overline{G} = V_{IL}$		100	mA
I_{CC1}	Supply Current (Standby)	$\overline{E}P = V_{IH}$, $\overline{G} = V_{IL}$		25	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 6. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M2716				Unit
				-1		blank		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}P = V_{IL}$, $\overline{G} = V_{IL}$		350		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		350		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}P = V_{IL}$		120		120	ns
t_{EHQZ} (2)	t_{OD}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	100	0	100	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}P = V_{IL}$	0	100	0	100	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}P = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

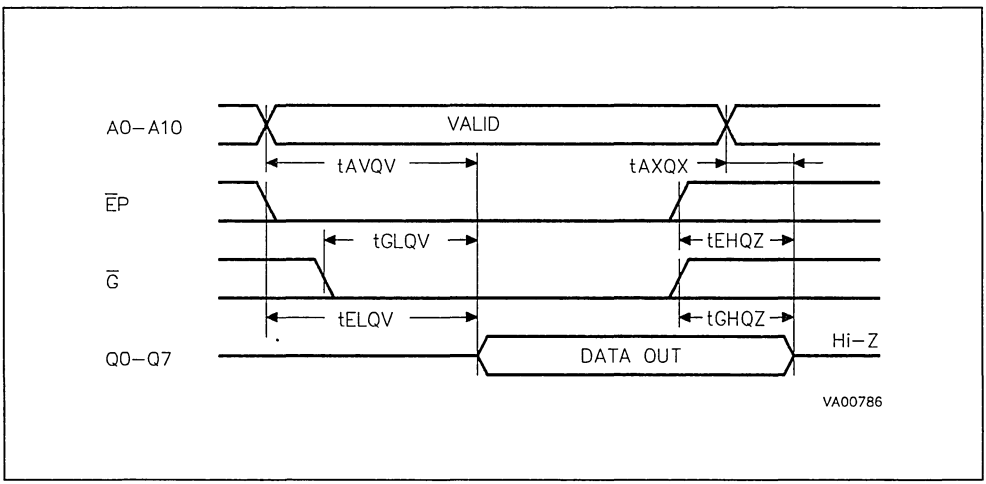


Table 7. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 25V ± 1V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			100	mA
I_{PP}	Program Current			5	mA
I_{PP1}	Program Current Pulse	$\overline{E}P = V_{IH}$ Pulse		30	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V

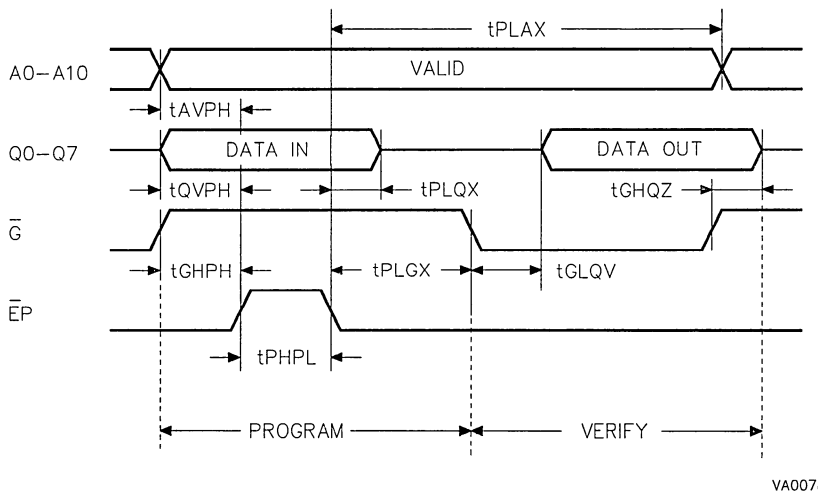
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 8. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 25V ± 1V)

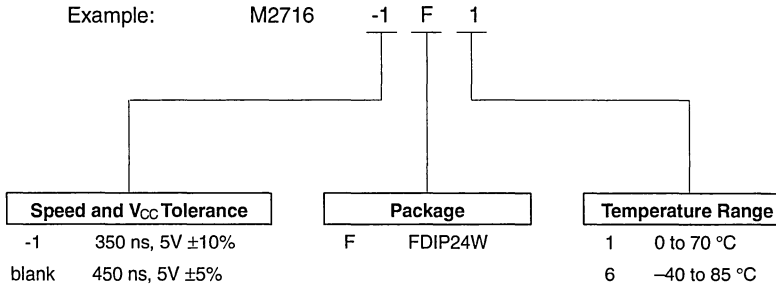
Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVPH}	t_{AS}	Address Valid to Program High	$\overline{G} = V_{IH}$	2		µs
t_{QVPH}	t_{DS}	Input Valid to Program High	$\overline{G} = V_{IH}$	2		µs
t_{GHPH}	t_{OS}	Output Enable High to Program High		2		µs
t_{PL1PL2}	t_{PR}	Program Pulse Rise Time		5		ns
t_{PH1PH2}	t_{PF}	Program Pulse Fall Time		5		ns
t_{PHPL}	t_{PW}	Program Pulse Width		45	55	ms
t_{PLQX}	t_{DH}	Program Low to Input Transition		2		µs
t_{PLGX}	t_{OH}	Program Low to Output Enable Transition		2		µs
t_{GLQV}	t_{OE}	Output Enable to Output Valid	$\overline{EP} = V_{IL}$		120	ns
t_{GHQZ}	t_{DF}	Output Enable High to Output Hi-Z		0	100	ns
t_{PLAX}	t_{AH}	Program Low to Address Transition		2		µs

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



ORDERING INFORMATION SCHEME

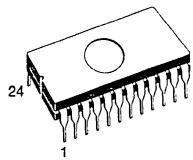


For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

NMOS 32K (4K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- INPUTS and OUTPUTS TTL COMPATIBLE DURING READ and PROGRAM
- COMPLETELY STATIC



FDIP24W (F)

DESCRIPTION

The M2732A is a 32,768 bit UV erasable and electrically programmable memory EPROM. It is organized as 4,096 words by 8 bits. The M2732A with its single 5V power supply and with an access time of 200 ns, is ideal suited for applications where fast turn around and pattern experimentation one important requirements.

The M2732A is honsed in a 24 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can be then written to the clerice by following the programming procedure.

Figure 1. Logic Diagram

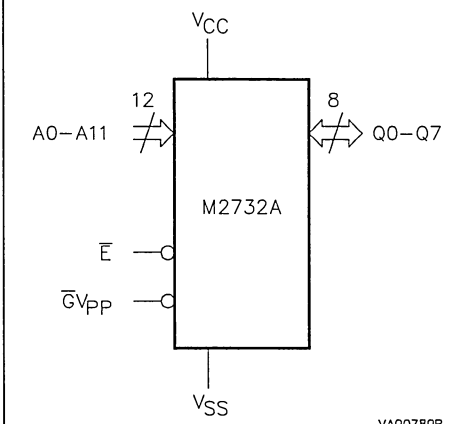


Table 1. Signal Names

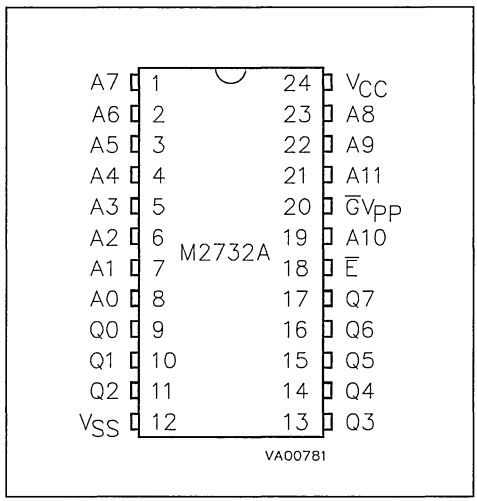
A0 - A11	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6	V
V_{CC}	Supply Voltage		–0.6 to 6	V
V_{PP}	Program Supply Voltage		–0.6 to 22	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The six modes of operation for the M2732A are listed in the Operating Modes Table. A single 5V power supply is required in the read mode. All inputs are TTL level except for V_{PP}.

Read Mode

The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVAQ}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M2732A has a standby mode which reduces the active power current by 70 %, from 125 mA to 35 mA. The M2732A is placed in the standby mode by applying a TTL high signal to $\overline{E}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because M2732A's are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{E}$ be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

Programming

When delivered, and after each erasure, all bits of the M2732A are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2732A is in the programming mode when the $\overline{G}V_{PP}$ input is at 21V. A 0.1µF capacitor must be placed across $\overline{G}V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied, 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50ms, active low, TTL program pulse is applied to the $\overline{E}$ input. A program pulse must be applied at each address location to be programmed. Any location can be programmed at any time - either individually, sequentially, or at random. The program pulse has a maximum width of 55ms. The M2732A must not be programmed with a DC signal applied to the $\overline{E}$ input.

Programming of multiple M2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Inputs of the paralleled M2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{E}$ input programs the paralleled 2732As.

Program Inhibit

Programming of multiple M2732As in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}V_{PP}$) of the parallel M2732As may be common. A TTL level program pulse applied to a M2732A's $\overline{E}$ input with $\overline{G}V_{PP}$ at 21V will program that M2732A. A high level $\overline{E}$ input inhibits the other M2732As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is carried out with $\overline{G}V_{PP}$ and $\overline{E}$ at V_{IL}.

ERASURE OPERATION

The erasure characteristics of the M2732A are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to the direct sunlight. If the M2732A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2732A window to prevent unintentional erasure.

The recommended erasure procedure for the M2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M2732A should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	V_{CC}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{CC}	Data Out
Program	V_{IL} Pulse	V_{PP}	V_{CC}	Data In
Verify	V_{IL}	V_{IL}	V_{CC}	Data Out
Program Inhibit	V_{IH}	V_{PP}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Note: X = V_{IH} or V_{IL}.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

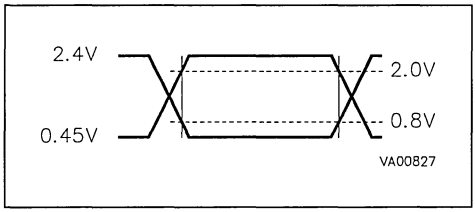


Figure 4. AC Testing Load Circuit

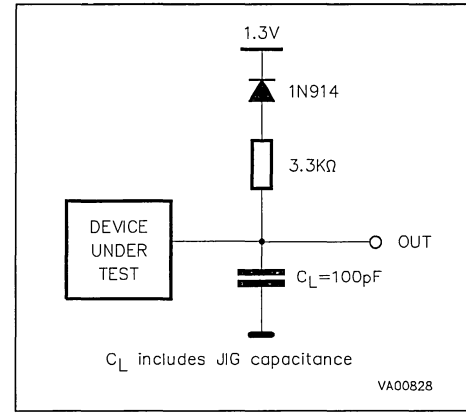


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (except $\overline{G}V_{PP}$)	V_{IN} = 0V		6	pF
C_{IN1}	Input Capacitance ($\overline{G}V_{PP}$)	V_{IN} = 0V		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

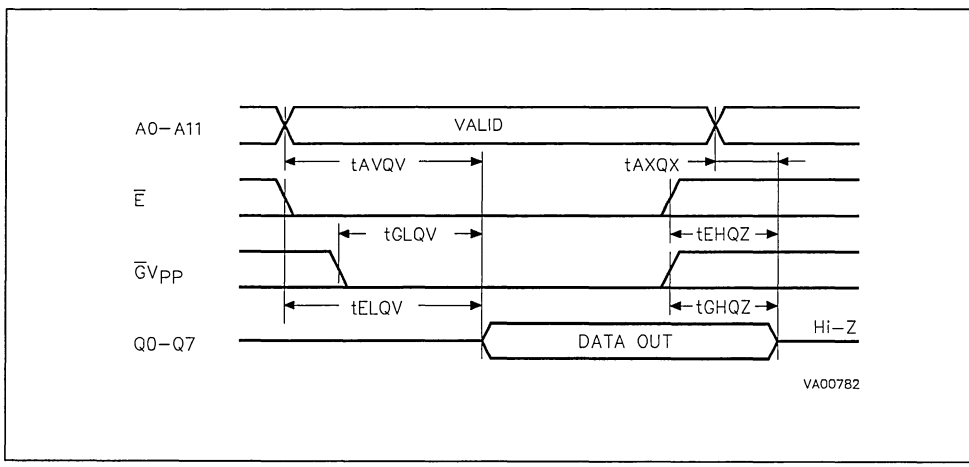


Table 5. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Value		Unit
			Min	Max	
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		125	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$, $\overline{G} = V_{IL}$		35	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 6. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M2732A								Unit
				-2, -20		blank, -25		-3		-4		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		100		100		150		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	60	0	60	0	130	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	60	0	60	0	130	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Table 7. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 21V ± 0.5V)

Symbol	Parameter	Test Condition	Min	Max	Units
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		125	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{PP}$		30	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

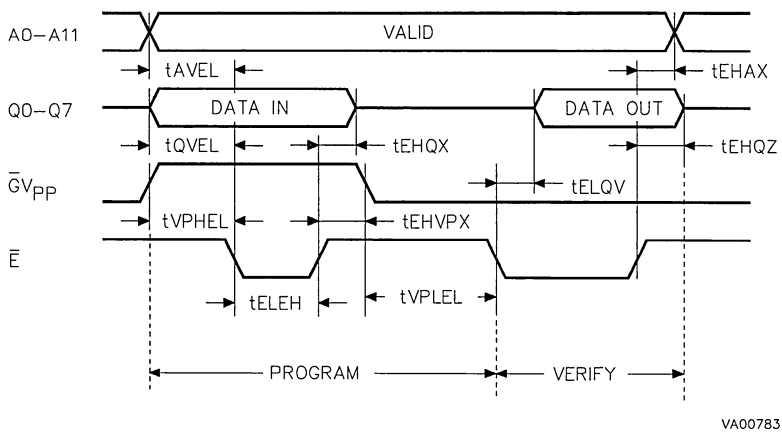
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

Table 8. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 21V ± 0.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
$t_{VPL1VPL2}$	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		45	55	ms
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		1	µs
t_{EHQZ}	t_{DF}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Figure 6. Programming and Verify Modes AC Waveforms



ORDERING INFORMATION SCHEME

Example: M2732A -2 F 1

Speed and V_{CC} Tolerance		Package		Temperature Range	
-2	200 ns, 5V ±5%	F	FDIP24W	1	0 to 70 °C
blank	250 ns, 5V ±5%			6	–40 to 85 °C
-3	300 ns, 5V ±5%				
-4	450 ns, 5V ±5%				
-20	200 ns, 5V ±10%				
-25	250 ns, 5V ±10%				

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

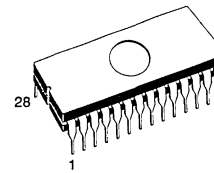
For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SGS-THOMSON MICROELECTRONICS

M2764A

NMOS 64K (8K x 8) UV EPROM

- FAST ACCESS TIME: 180ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M2764A is a 65,536 bit UV erasable and electrically programmable memory EPROM. It is organized as 8,192 words by 8 bits.

The M27C64A is housed in a 28 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Figure 1. Logic Diagram

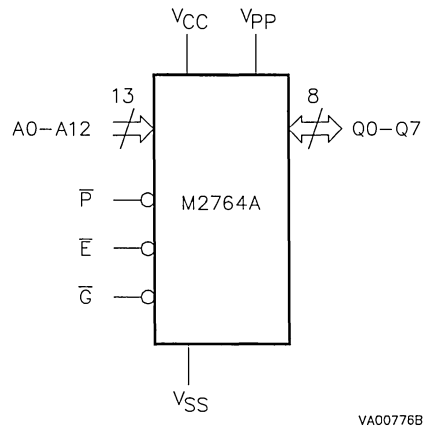


Table 1. Signal Names

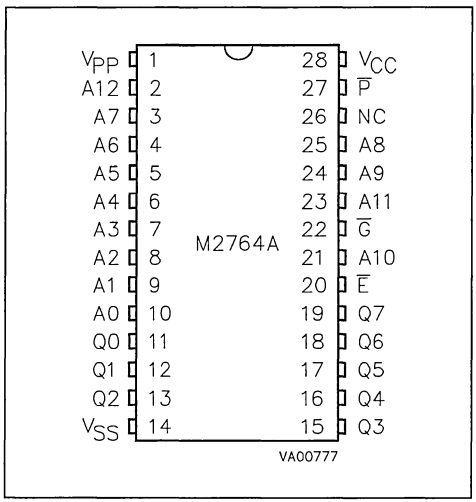
A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.6 to 6.5	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



Warning: NC = No Connection.

DEVICE OPERATION

The seven modes of operations of the M2764A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M2764A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M2764A has a standby mode which reduces the maximum active power current from 75mA to 35mA. The M2764A is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M2764A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2764A is in the programming mode when V_{PP} input is at 12.5V and $\overline{E}$ and $\overline{P}$ are at TTL low. The data to be programmed is applied, 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M2764A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes Out

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5%.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	1	0	0	0	08h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

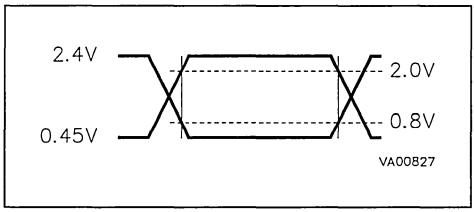


Figure 4. AC Testing Load Circuit

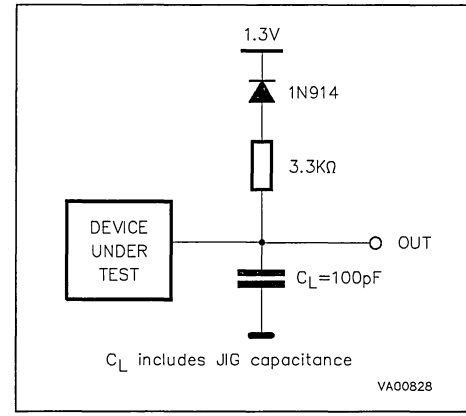


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

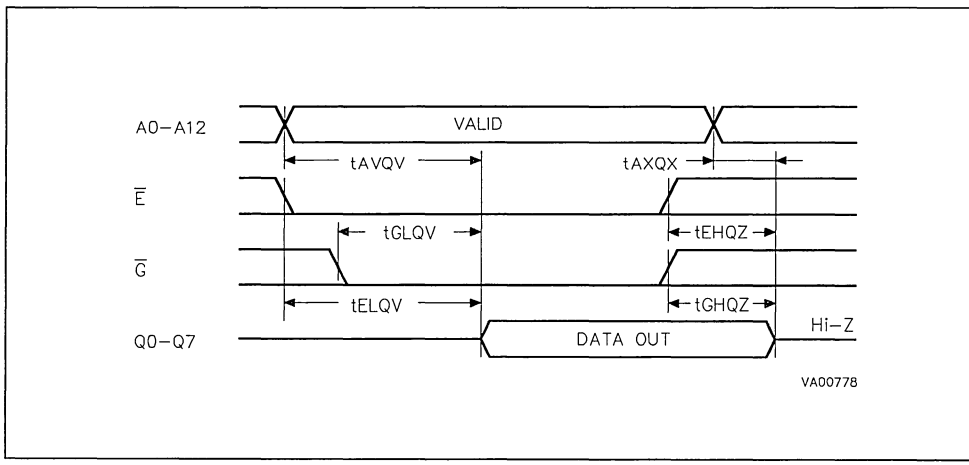


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		75	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		35	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M2764A						Unit
				-1		-2, -20		blank, -25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		180		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		180		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		65		75		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	55	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	55	0	55	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M2764A				Unit
				-3		-4		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$,		120		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	105	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	105	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Units
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			75	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
VA9	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t_{PLPH}	t_{OPW}	Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			150	ns
t_{GHQZ} (4)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. The Initial Program Pulse width tolerance is 1 ms ± 5%.
3. The length of the Over-program Pulse varies from 2.85 ms to 78.95 ms, depending of the multiplication value of the iteration counter.
4. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

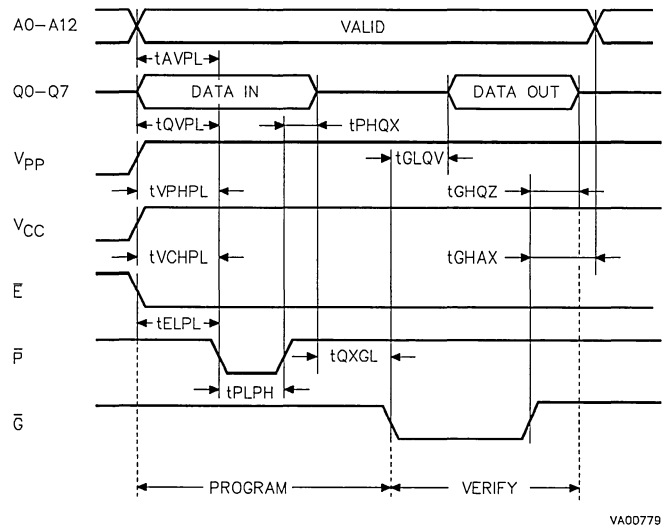
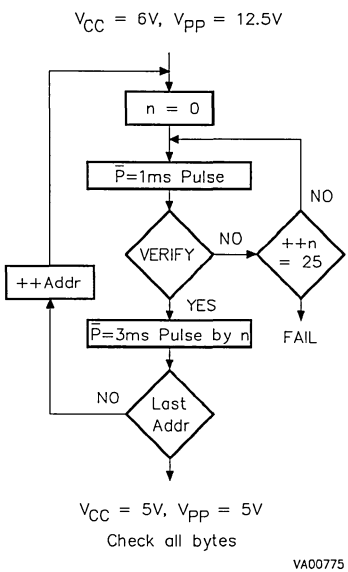


Figure 7. Fast Programming Flowchart



DEVICE OPERATION (cont'd)

been successfully programmed. A flowchart of the M2764A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and over-program.

The duration of the initial $\overline{P}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3ms by n (n is equal to the number of the initial one millisecond pulses applied to a particular M2764A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5V and V_{PP} = 5V.

Program Inhibit

Programming of multiple M2764A in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}$) of the parallel M2764A may be common. A TTL low pulse applied to a M2764A's $\overline{E}$ input, with V_{PP} at 12.5V, will program that M2764A. A high level $\overline{E}$ input inhibits the other M2764As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, $\overline{P} = V_{IH}$ and $V_{PP} = 12.5V$.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M2764A.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M2764A. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the SGS-THOMSON M2764A, these two identifier bytes are given below.

ERASURE OPERATION (applies to UV EPPROM)

The erasure characteristic of the M2764A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M2764A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M2764A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2764A window to prevent unintentional erasure. The recommended erasure procedure for the M2764A is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M2764A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M2764A -1 F 1

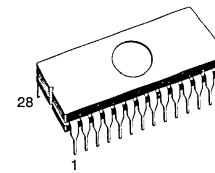
Speed and V_{CC} Tolerance		Package		Temperature Range	
-1	180 ns, 5V ±5%	F	FDIP28W	1	0 to 70 °
-2	200 ns, 5V ±5%			6	–40 to 85 °C
blank	250 ns, 5V ±5%				
-3	300 ns, 5V ±5%				
-4	450 ns, 5V ±5%				
-20	200 ns, 5V ±10%				
-25	250 ns, 5V ±10%				

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

NMOS 128K (16K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5 V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 40mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M27128A is a 131,072 bit UV erasable and electrically programmable memory EPROM. It is organized as 16,384 words by 8 bits.

The M27128A is housed in a 28 Pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Table 1. Signal Names

A0 - A13	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

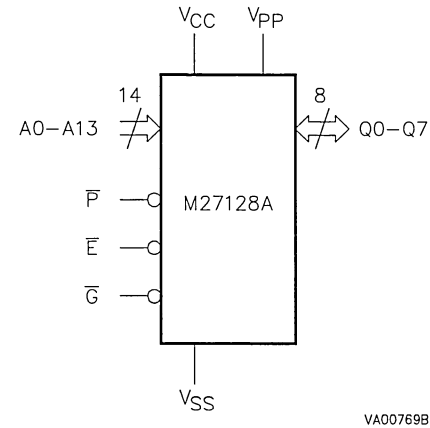
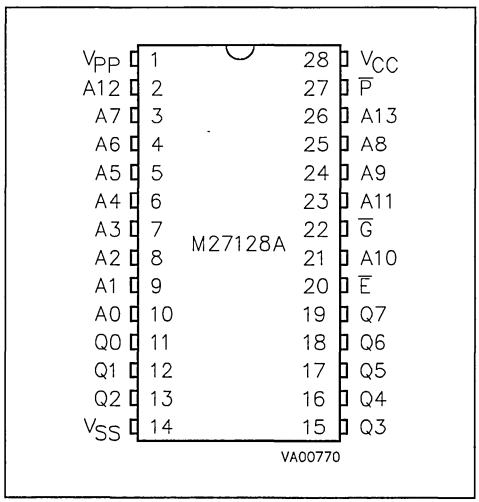


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.25	V
V_{CC}	Supply Voltage		–0.6 to 6.25	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



Warning: NC = No Connection.

DEVICE OPERATION

The seven modes of operation of the M27128A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27128A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27128A has a standby mode which reduces the maximum active power current from 85mA to 40mA. The M27128A is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPPROM), all bits of the M27128A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M27128A is in the programming mode when V_{PP} input is at 12.5V and $\overline{E}$ and $\overline{P}$ are at TTL low. The data to be programmed is applied 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M27128A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes Out

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5%.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	1	0	0	1	89h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

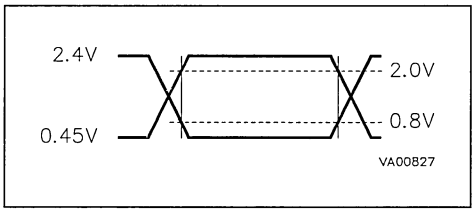


Figure 4. AC Testing Load Circuit

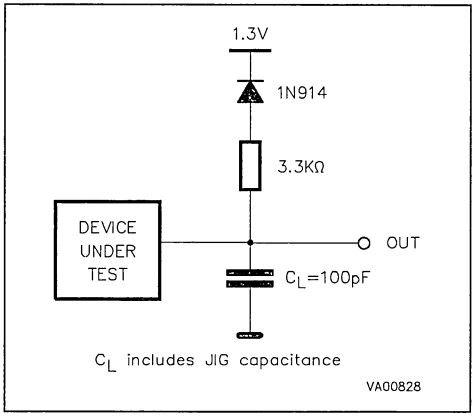


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	=	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	=	12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

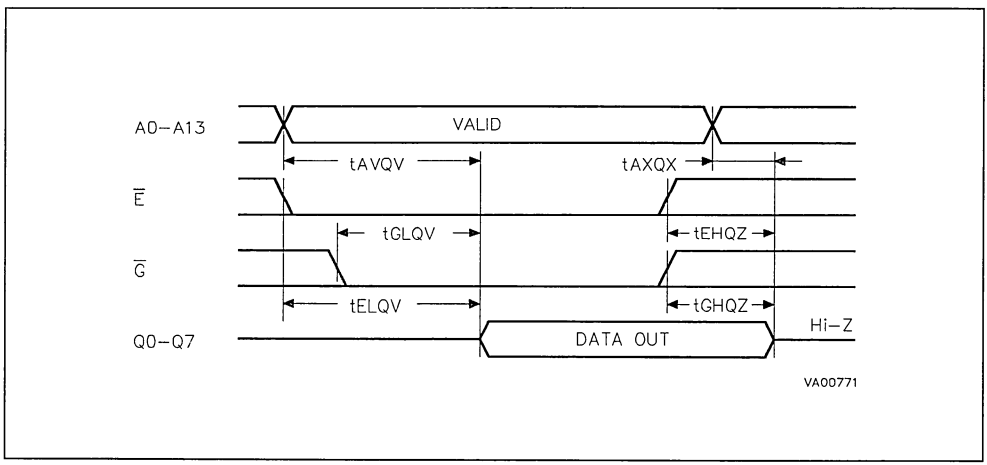


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		75	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		35	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	=	0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27128A								Unit
				-2, -20		blank, -25		-3, -30		-4		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		75		100		120		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	60	0	105	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	55	0	60	0	105	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics [1]
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			100	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics [1]
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t_{PLPH}	t_{OPW}	Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			150	ns
t_{GHQZ} [4]	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. The Initial Program Pulse width tolerance is 1 ms ± 5%.
3. The length of the Over-program Pulse varies from 2.85 ms to 78.95 ms, depending on the multiplication value of the iteration counter.
4. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

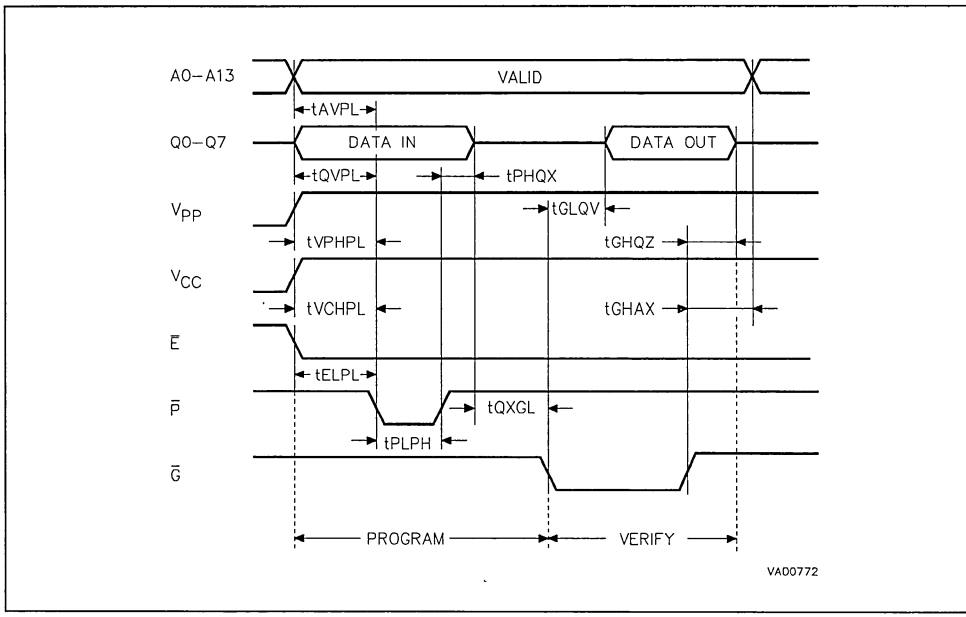
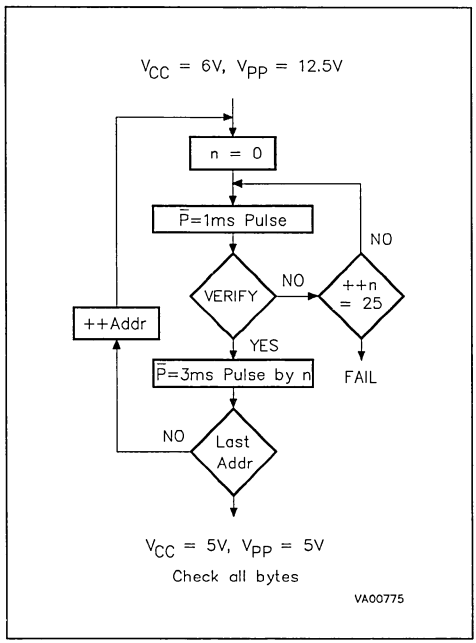


Figure 7. Programming Flowchart



DEVICE OPERATION (cont'd)

continually monitored to determine when it has been successfully programmed. A flowchart of the M27128A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and over-program.

The duration of the initial $\overline{P}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3ms by n (n is equal to the number of the initial one millisecond pulses applied to a particular M27128A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5 and V_{PP} = 5V.

Program Inhibit

Programming of multiple M27128A's in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}$) of the parallel M27128A may be common. A TTL low pulse applied to a M27128A's $\overline{E}$ input, with V_{PP} = 12.5V, will program that M27128A. A high level $\overline{E}$ input inhibits the other M27128As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, $\overline{P} = V_{IH}$ and V_{PP} at 12.5V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the25°C ± 5°C ambient temperature range that is required when programming the M27128A.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27128A. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS-THOMSON M27128A, these two identifier bytes are given below.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristic of the M27128A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27128A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27128A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27128A window to prevent unintentional erasure. The recommended erasure procedure for the M27128A is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27128A should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27128A -2 F 1

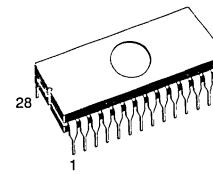
Speed and V_{CC} Tolerance		Package		Temperature Range	
-2	200 ns, 5V ±5%	F	FDIP28W	1	0 to 70 °C
blank	250 ns, 5V ± 5%			6	–40 to 85 °C
-3	300 ns, 5V ± 5%				
-4	450 ns, 5V ± 5%				
-20	200 ns, 5V ± 10%				
-25	250 ns, 5V ± 10%				
-30	300 ns, 5V ± 10%				

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

NMOS 256K (32K x 8) UV EPROM

- FAST ACCESS TIME: 170ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 40mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M27256 is a 262,144 bit UV erasable and electrically programmable memory EPROM. It is organized as 32.768 words by 8 bits.

The M27256 is housed in a 28 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user toexpose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure

Figure 1. Logic Diagram

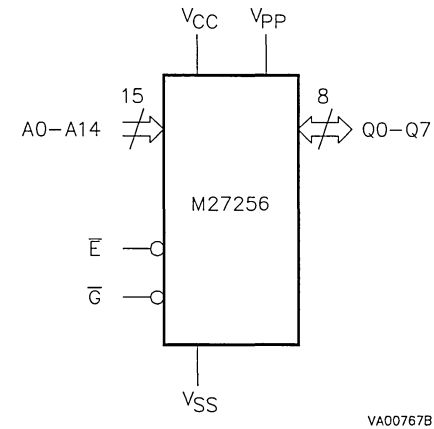


Table 1. Signal Names

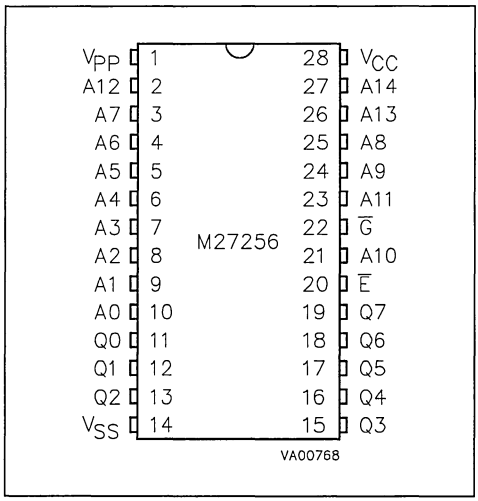
A0 - A14	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.25	V
V_{CC}	Supply Voltage		–0.6 to 6.25	V
V_{A9}	VA9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The eight modes of operations of the M27256 are listed in the Operating Modes Table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27256 has a standby mode which reduces the maximum active power current from 100mA to 40mA. The M27256 is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitors should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programmain

When delivered, (and after each erasure for UV EPROM), all bits of the M27256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27256 is in the programming mode when V_{PP} input is at 12.5V and $\overline{E}$ is at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M27256 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27256 Fast Programming Algorithm is shown on the Flowchart. The Fast Programming Algorithm utilizes two different pulse types : initial and over-program. The duration of the initial $\overline{E}$ pulse(s) is 1ms, which will then be followed by a longer over-program pulse of length 3ns by n (n is equal to the number of the initial one millisecond pulses applied

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Optional Verify	V_{IL}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5%.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

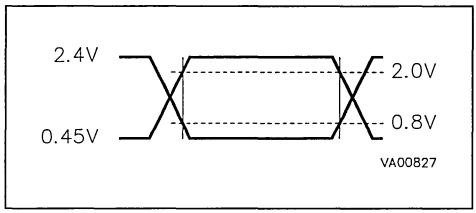


Figure 4. AC Testing Load Circuit

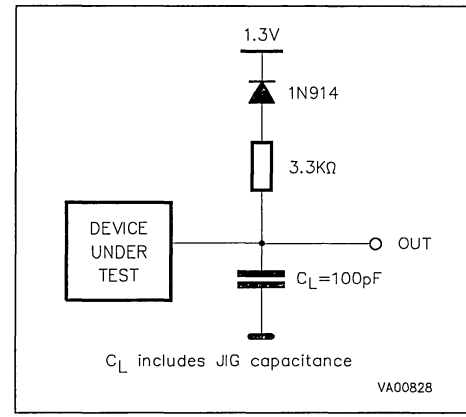


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

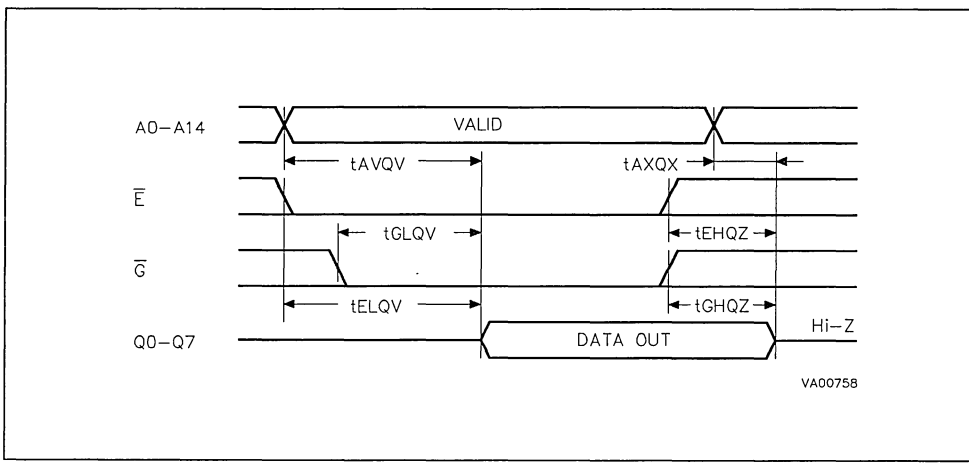


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		40	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27256						Unit
				-1		-2, -20		blank, -25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		170		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		170		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		70		75		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	35	0	55	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	35	0	55	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27256				Unit
				-3		-4		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$,		120		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	105	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	105	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			100	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t_{ELEH}	t_{OPW}	Chip Enable Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			150	ns
t_{GHQZ} (4)	t_{DFP}	Output Enable Low to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. The Initial Program Pulse width tolerance is 1 ms ± 5%.
3 The length of the Over-program Pulse varies from 2.85 ms to 78.95 ms, depending on the multiplication value of the iteration counter.
4. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

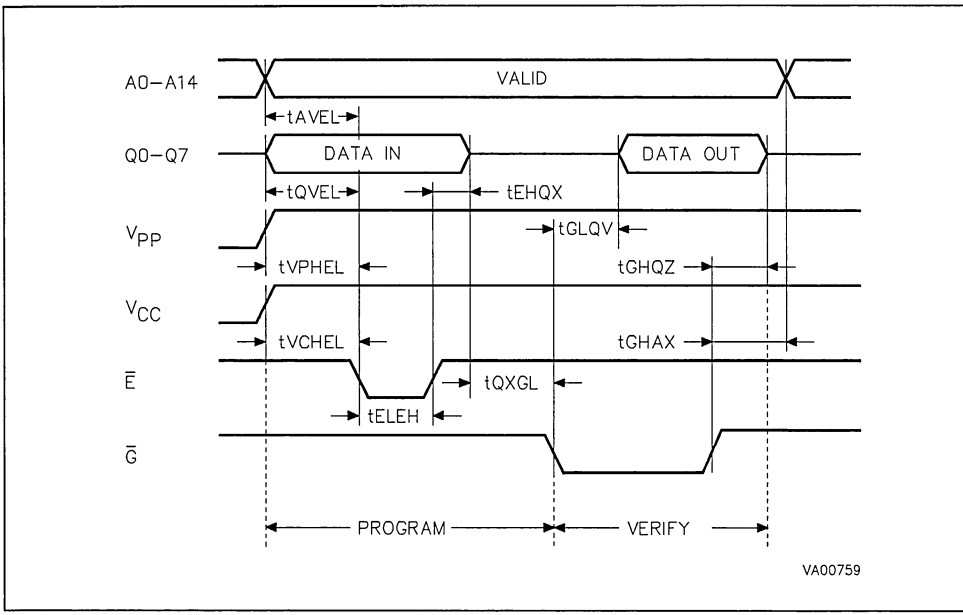
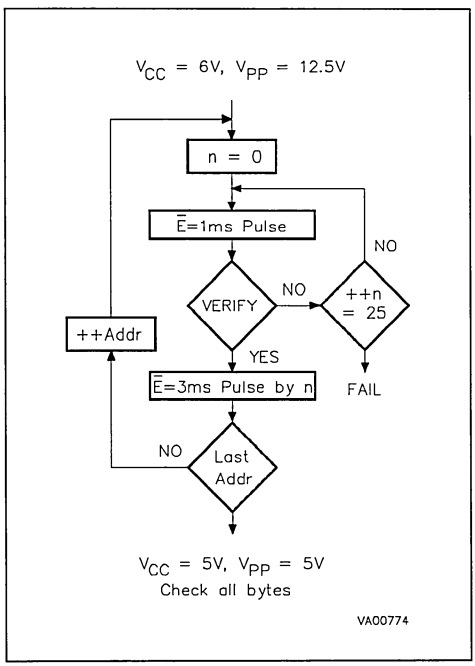


Figure 7. Programming Flowchart



DEVICE OPERATION (cont'd)

to a particular M27256 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V.

When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5V and V_{PP} = 5V.

Program Inhibit

Programming of multiple M27256s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}$) of the parallel M27256 may be common. A TTL low pulse applied to a M27256's $\overline{E}$ input, with V_{PP} = 12.5V, will program that M27256. A high level $\overline{E}$ input inhibits the other M27256s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$ and V_{PP} = 12.5V.

Optional Verify

The optional verify may be performed instead of the verify mode. It is performed with $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$ (as opposed to the standard verify which has $\overline{E}$ =

DEVICE OPERATION (cont'd)

V_{IH}), and V_{PP} = 12.5V. The outputs will be in a Hi-z state according to the signal presented to $\overline{G}$. Therefore, all devices with V_{PP} = 12.5V and $\overline{G} = V_{IL}$ will present data on the bus independent of the $\overline{E}$ state. When parallel programming several devices which share the common bus, V_{PP} should be lowered to V_{CC} (6V) and the normal read mode used to execute a program verify.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27256. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS-THOMSON M27256, these two identifier bytes are given below.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristic of the M27256 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27256 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27256 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque lables be put over the M27256 window to prevent unintentional erasure. The recommended erasure procedure for the M27256 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27256 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27256 -1 F 1

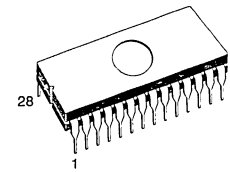
Speed and V_{CC} Tolerance		Package		Temperature Range	
-1	170 ns, 5V ±5%	F	FDIP28W	1	0 to 70 °C
-2	200 ns, 5V ±5%			6	–40 to 85 °C
blank	250 ns, 5V ±5%				
-3	300 ns, 5V ±5%				
-4	400 ns, 5V ±5%				
-20	200 ns, 5V ±10%				
-25	250 ns, 5V ±10%				

For a list of available options (Speed, V_{CC} Tolerance, Package, etc) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

NMOS 512K (64K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 40mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAM MING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M27512 is a 524,288 bit UV erasable and electrically programmable memory EPROM. It is organized as 65,536 words by 8 bits.

The M27512 is housed in a 28 Pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Figure 1. Logic Diagram

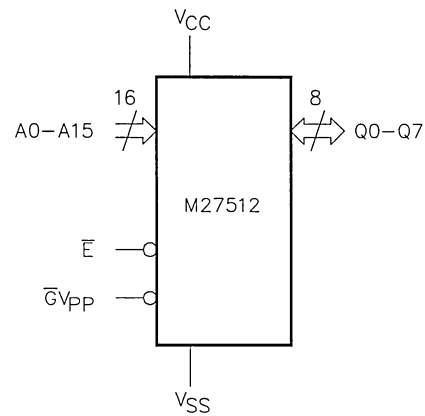


Table 1. Signal Names

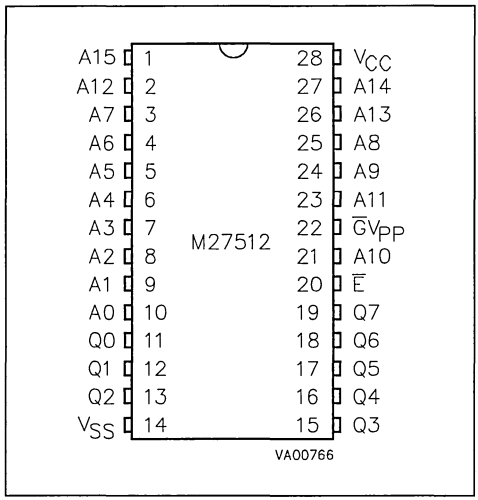
A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	Grade 1 Grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	Grade 1 Grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.6 to 6.5	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The six modes of operations of the M27512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27512 has a standby mode which reduces the maximum active power current from 125mA to 40mA. The M27512 is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices.

The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommenced that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered, and after each erasure, all bits of the M27512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27512 is in the programming mode when $\overline{G}V_{PP}$ input is at 12.5V and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. The M27512 can use PRESTO Programming Algorithm that drastically reduces the programming time (typically less than 50 seconds). Nevertheless to achieve compatibility with all programming equipment, the standard Fast Programming Algorithm may also be used.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M27512 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27512 Fast Programming Algorithm is shown in Figure 8.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q0 - Q7
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Verify	V_{IH}	V_{IL}	X	Data Out
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5%.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	1	1	0	1	0Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

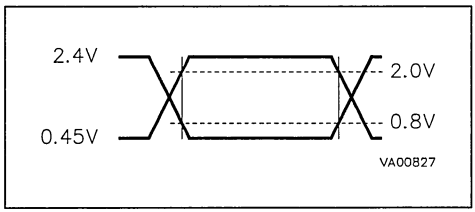


Figure 4. AC Testing Load Circuit

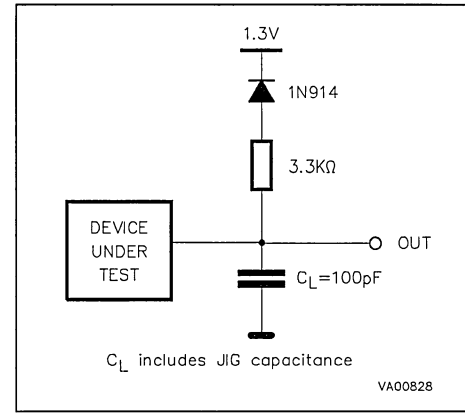


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

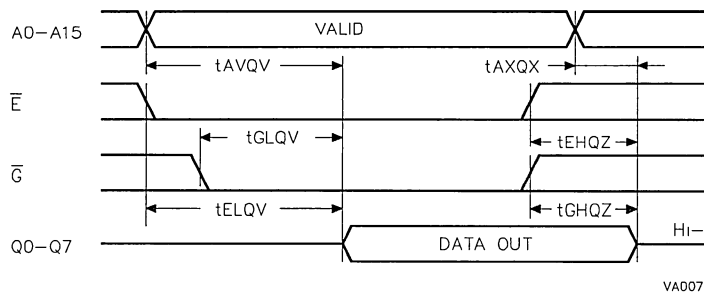


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		125	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		40	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27512						Unit
				-2, -20		blank, -25		-3		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		200		250		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		75		100		120	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	60	0	105	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	55	0	60	0	105	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			150	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. MARGIN MODE AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	VA9 High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	VA10 High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	VA10 Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to VA10 Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to VA9 Transition		2		µs

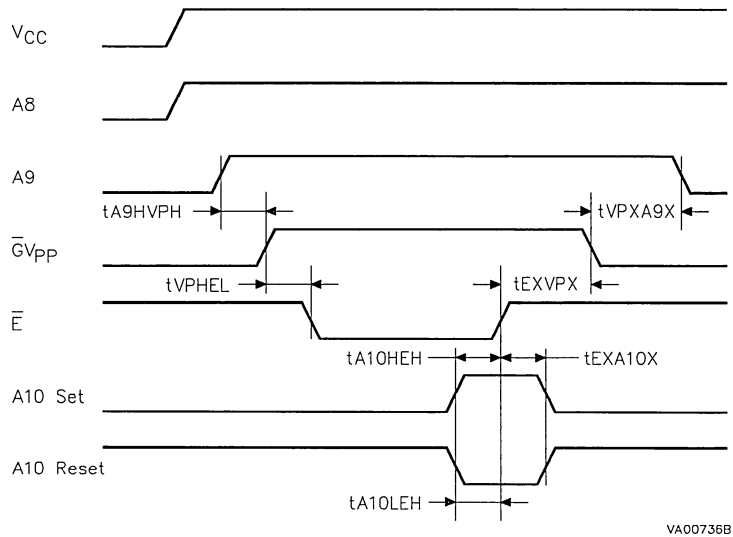
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t_{ELEH}	t_{OPW}	Chip Enable Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} (4)	t_{DF}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. The Initial Program Pulse width tolerance is 1 ms ± 5%.
3. The length of the Over-program Pulse varies from 2.85 ms to 78.95 ms, depending on the multiplication value of the iteration counter.
4. Sampled only, not 100% tested.

Figure 6. MARGIN MODE AC Waveform



Note: A8 High level = 5V; A9 High level = 12V.

Figure 7. Programming and Verify Modes AC Waveforms

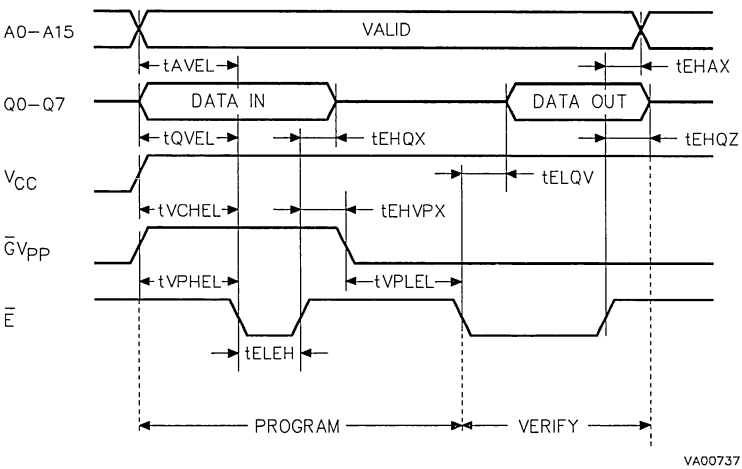


Figure 8. Fast Programming Flowchart

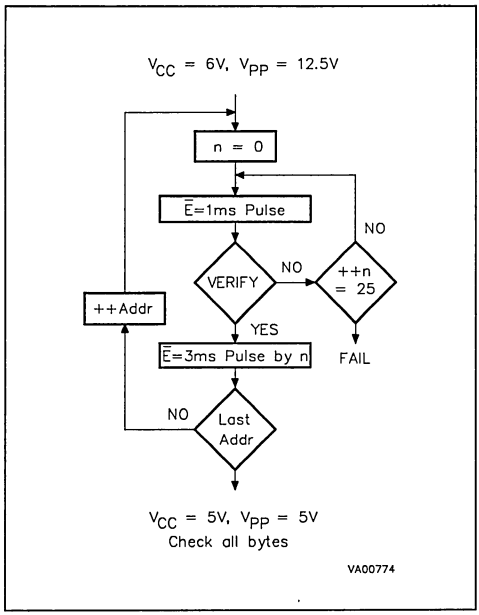
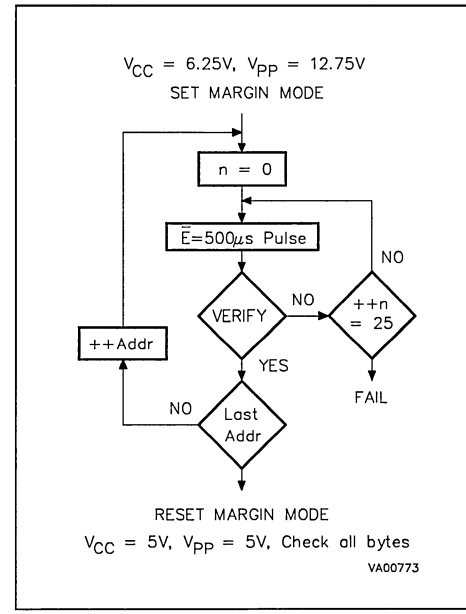


Figure 9. PRESTO Programming Flowchart



DEVICE OPERATION (cont'd)

The Fast Programming Algorithm utilizes two different pulse types : initial and overprogram. The duration of the initial $\overline{E}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3ns by n (n is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27512 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.
The entire sequence of program pulses is performed at V_{CC} = 6V and $\overline{G}V_{PP}$ = 12.5V (byte verifications at V_{CC} = 6V and $\overline{G}V_{PP} = V_{IL}$). When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5V.

PRESTO Programming Algorithm

PRESTO Programming Algorithm allows to program the whole array with a guaranted margin, in a typical time of less than 50 seconds (to be compared with 283 seconds for the Fast algorithm). This can be achieved with the SGS-THOMSON M27512 due to several design innovations described in the next paragraph that improves programming efficiency and brings adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin.
Then a sequence of 500µs program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27512s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}V_{PP}$) of the parallel M27512 may be common. A TTL low level pulse applied to a M27512's $\overline{E}$ input, with $\overline{G}V_{pp}$ at 12.5V, will program that M27512. A high level $\overline{E}$ input inhibits the other M27512s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}V_{pp}$ and $\overline{E}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{E}$.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25 °C ± 5 °C ambient temperature range that is required when programming the M27512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode, except for A14 and A15 which should be high. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristic of the M27512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27512 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27512 window to prevent unintentional erasure. The recommended erasure procedure for the M27512 is exposure to short wave ultraviolet light which has wavelength 2537 Å.

The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27512 -2 F 1

Speed and V_{CC} Tolerance		Package		Temperature Range	
-2	200 ns, 5V ±5%	F	FDIP28W	1	0 to 70 °C
blank	250 ns, 5V ±5%			6	–40 to 85 °C
-3	300 ns, 5V ±5%				
-20	200 ns, 5V ±10%				
-25	250 ns, 5V ±10%				

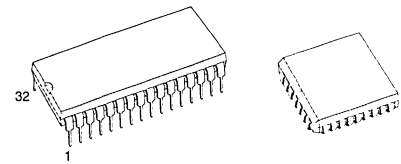
For a list of available options (Speed, V_{CC} Tolerance, Package, etc) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FLASH MEMORIES

CMOS 256K (32K x 8, Chip Erase) FLASH MEMORY

- FAST ACCESS TIME: 120ns
- 1,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 100µs (PRESTO F PROGRAMMING)
- ELECTRICAL CHIP ERASE IN 1s RANGE



PDIP32 (P)

PLCC32 (K)

DESCRIPTION

The M28F256 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 32K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F256 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

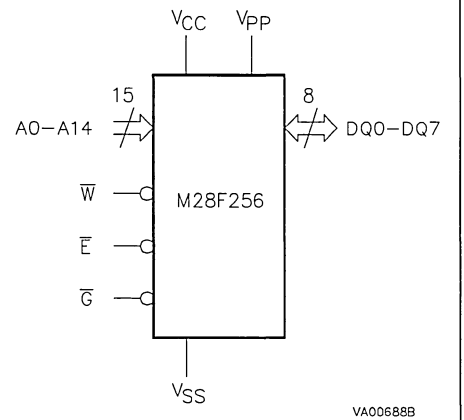
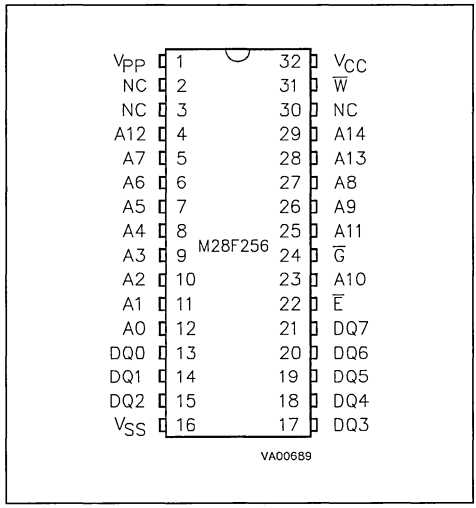
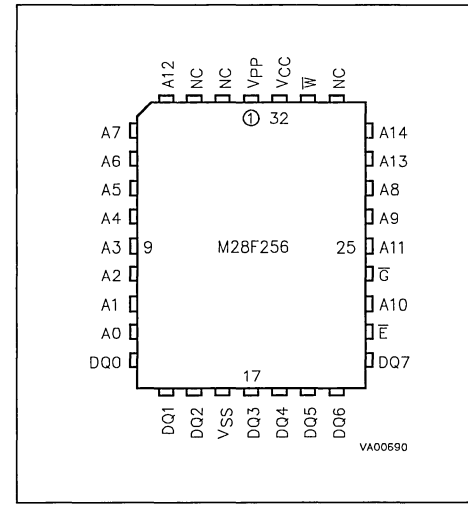


Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F256 FLASH MEMORY employs a technology similar to a 256K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F256 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

Read Mode. The M28F256 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 200µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when V_{PP} is $\leq$ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory.

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	0	1	0	0	0	0A8h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A14	DQ0-DQ7	Operation	A0-A14	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	0000h	20h
					Read	0001h	0A8h
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A14	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A14	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

READ/WRITE MODES (cont'd)

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this second cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

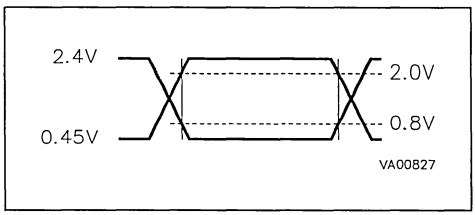


Figure 4. AC Testing Load Circuit

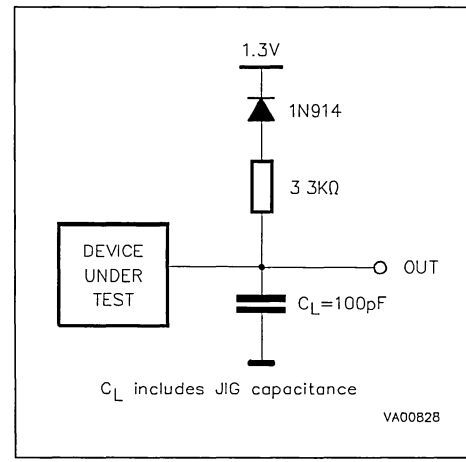


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		200	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±100	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±100	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage TTL	IOH = –2.5mA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	4.1		V
		I_{OH} = –1mA	V_{CC} –0.8		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA

Note: 1. Not 100% Tested. Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F256 -12		Unit
				Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics
((T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F256 -15		-20		Unit
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		55		60	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

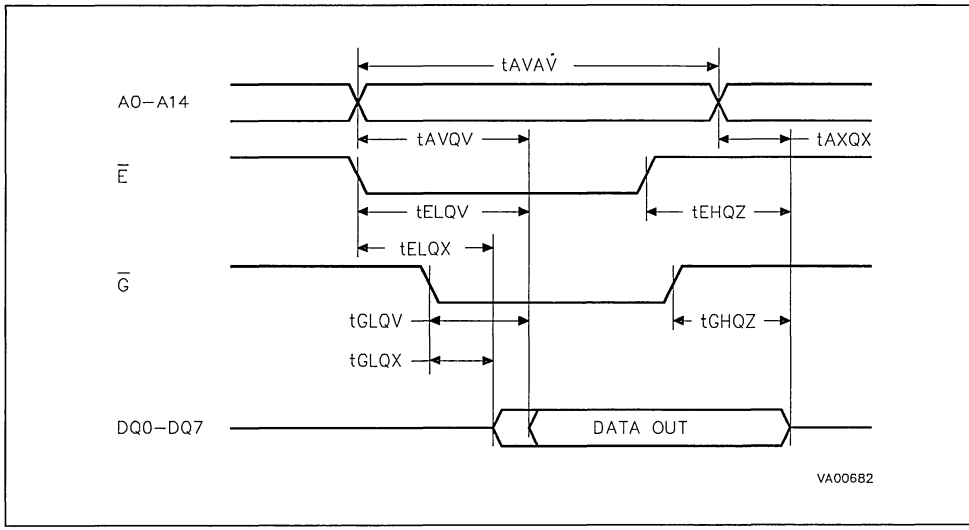


Figure 6. Read Command Waveforms

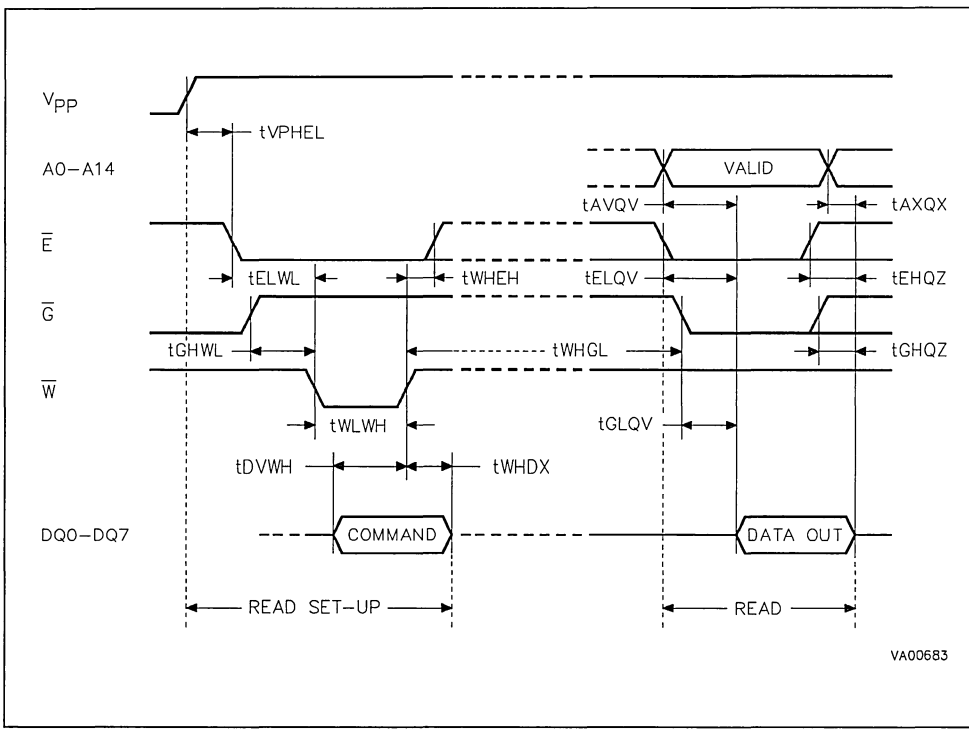


Figure 7. Electronic Signature Command Waveforms

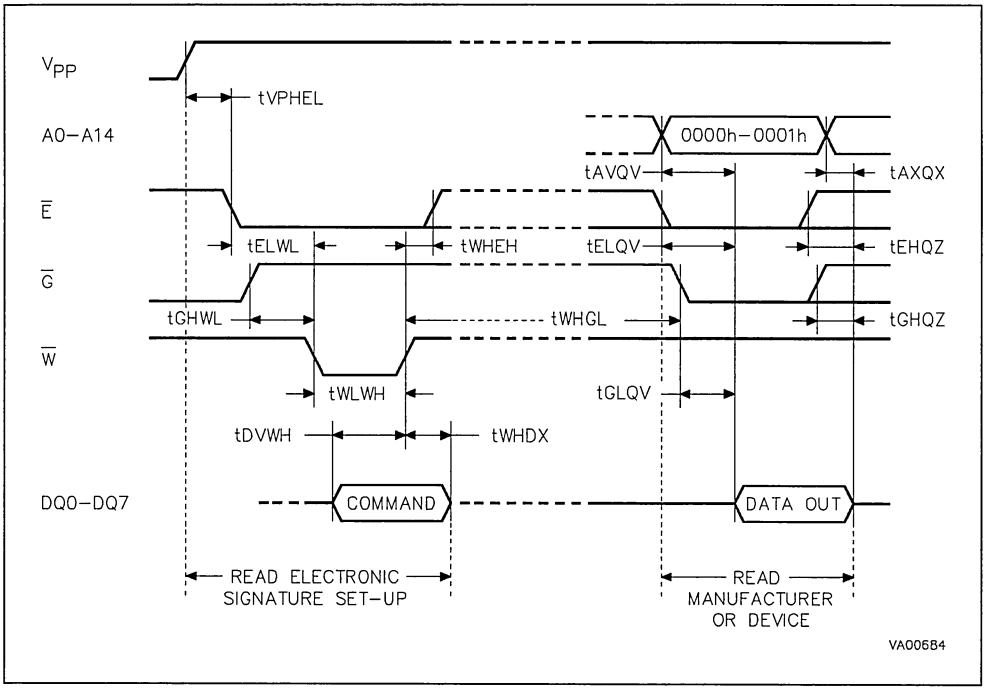


Table 9A. Read/Write Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = 12V)

Symbol	Alt	Parameter	M28F256 -12		Unit
			Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	100		ns
t_{WHWH3}	t_{WC}	Write Cycle Time	120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		ns
t_{ELEH} (2)		Chip Enable Low to Chip Enable High (Write Pulse)	60		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		ns
t_{WHWH1}		Duration of Program Operation	95	105	µs
t_{WHWH2}		Duration of Erase Operation	9.5	10.5	ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		120	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		120	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		50	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z		40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		ns

Notes: 1. Sampled only, not 100% tested
2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Table 9B. Read/Write Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = 12V)

Symbol	Alt	Parameter	M28F256				Unit
			-15		-20		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	100		100		ns
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH} (2)		Chip Enable Low to Chip Enable High (Write Pulse)	60		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	95	105	95	105	µs
t_{WHWH2}		Duration of Erase Operation	9.5	10.5	9.5	10.5	ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested
2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

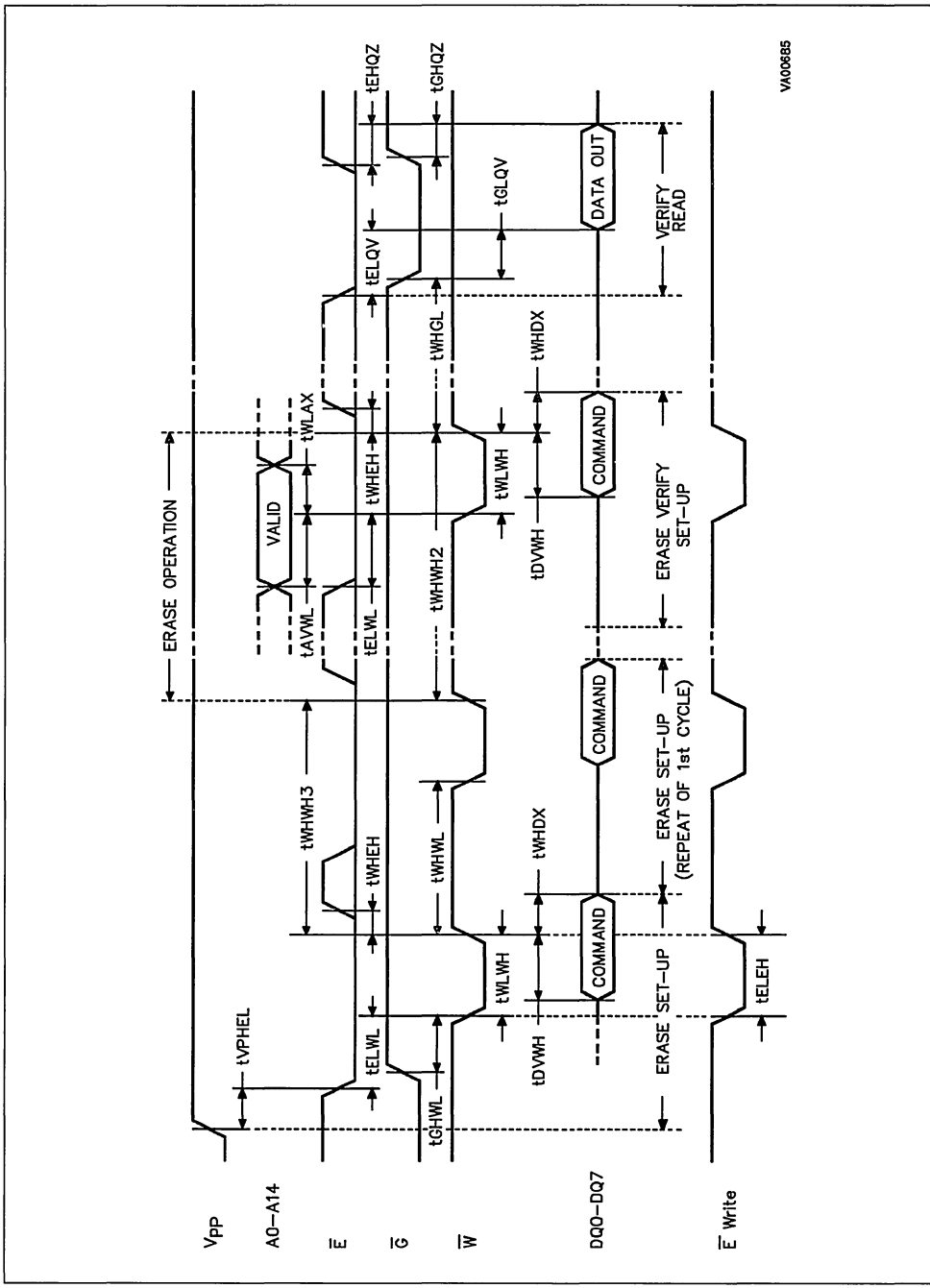


Figure 9. Program Set-up and Program Verify Commands Waveforms

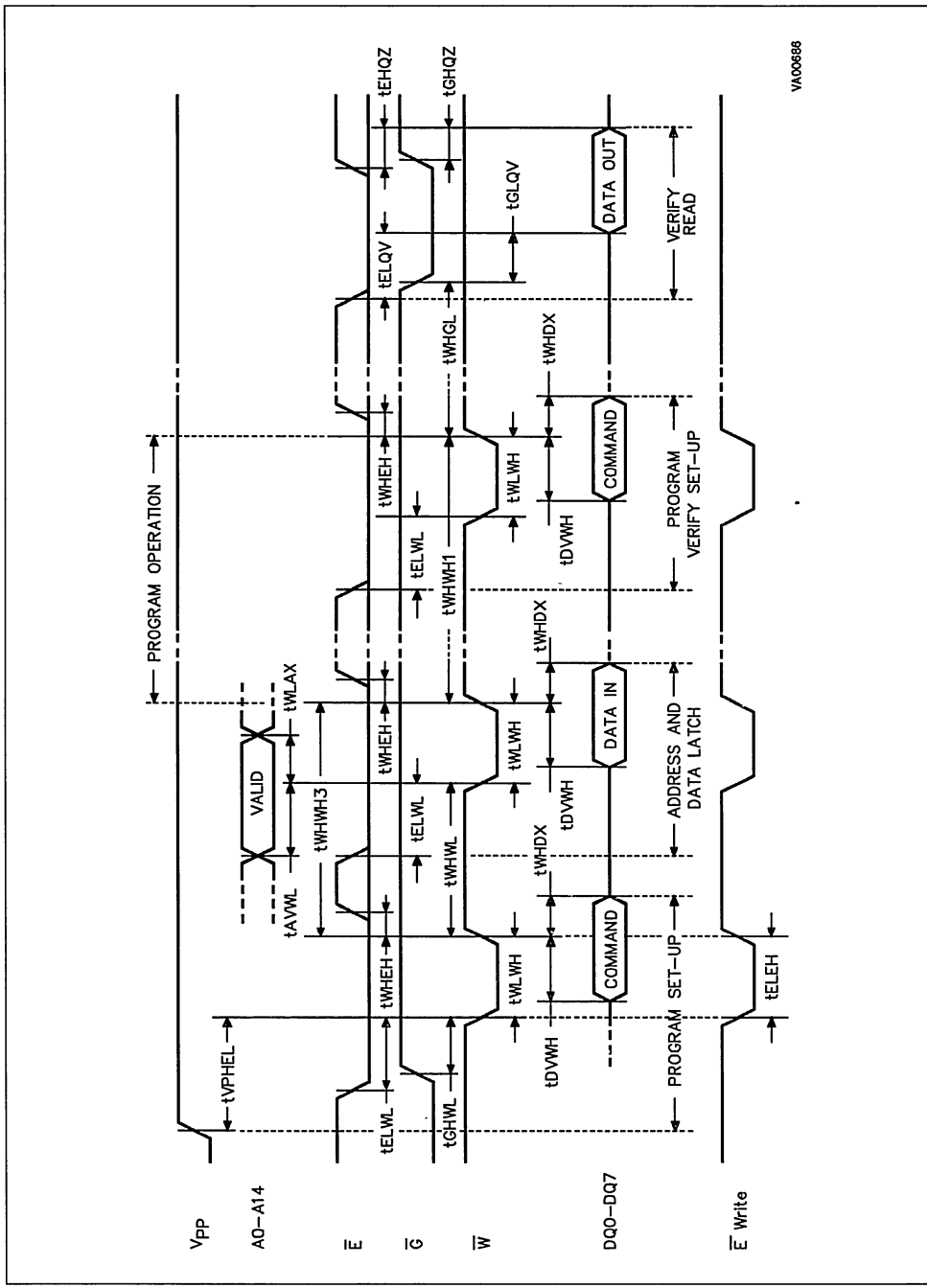


Figure 10. Erasing Flowchart

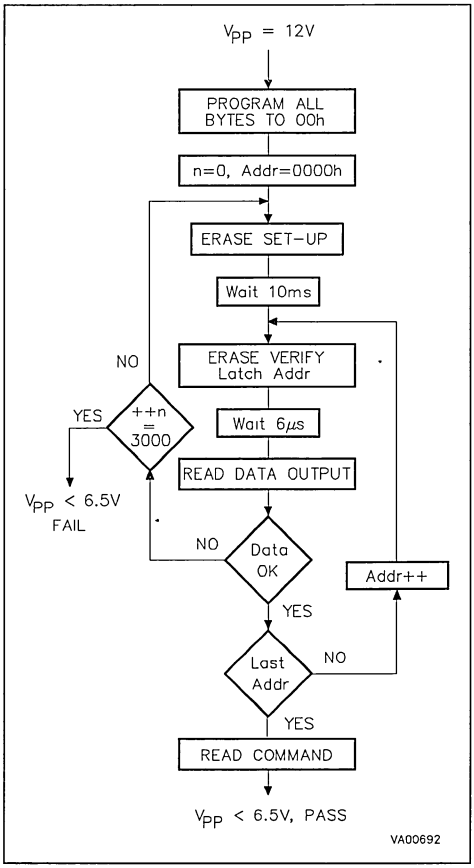
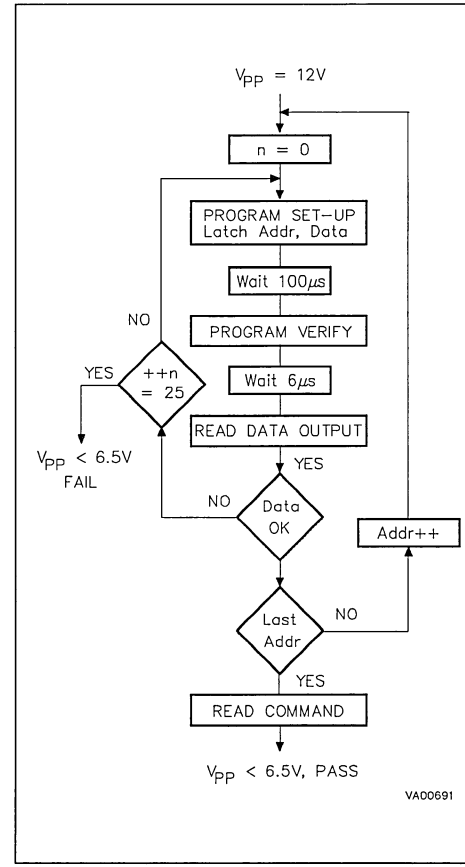


Figure 11. Programming Flowchart



PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programs all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 100µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME

Example: M28F256 -12 X B 1 TR

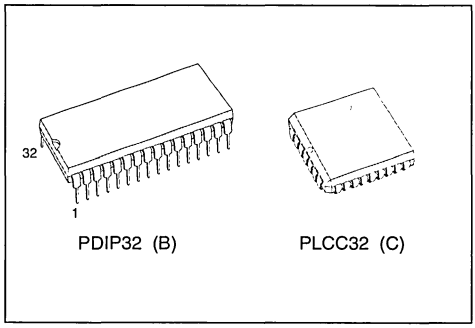
Speed		V_{CC} Tolerance		Package		Temp. Range		Option	
-12	120 ns	blank	± 10%	B	PDIP32	1	0 to 70 °C	TR	Tape & Reel Packing
-15	150 ns	X	± 5%	C	PLCC32	3	–40 to 125 °C		
-20	200 ns					6	–40 to 85 °C		

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

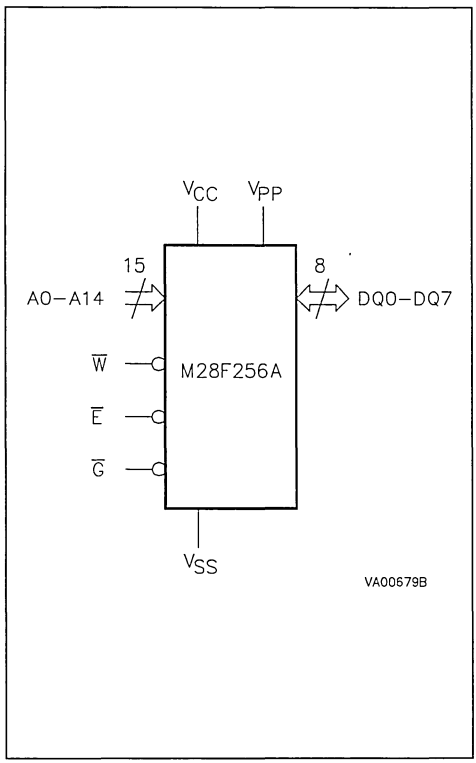
CMOS 256K (32K x 8, Chip Erase) FLASH MEMORY

- FAST ACCESS TIME: 120ns
- LOW POWER CONSUMPTION
  - Standby Current: 200µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE IN 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



PDIP32 (B) PLCC32 (C)

Figure 1. Logic Diagram



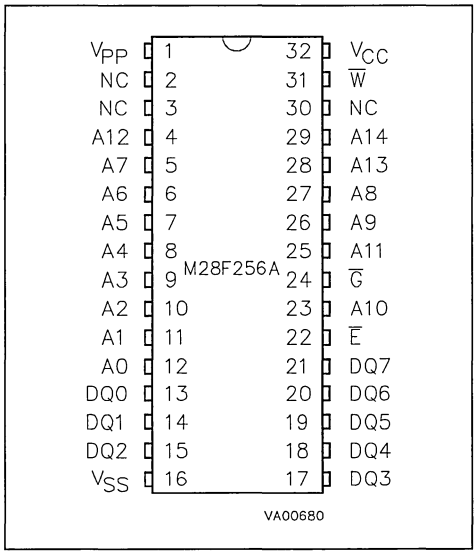
DESCRIPTION

The M28F256A FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 32K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F256A FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

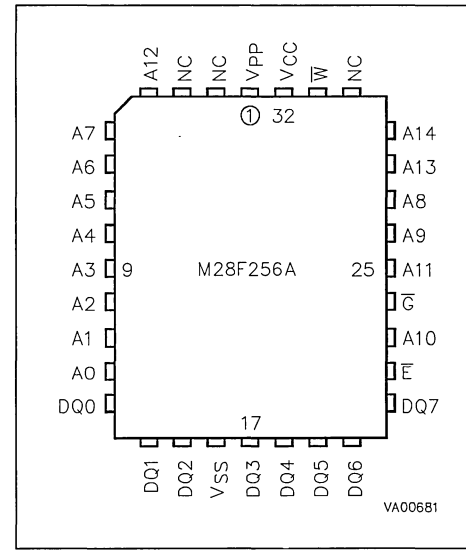
A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F256A FLASH MEMORY employs a technology similar to a 256K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F256A functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is don't care.

Read Mode. The M28F256A has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 200µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when $V_{PP} \leq 6.5V$ the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	0	1	0	1	0	0AAh

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A14	DQ0-DQ7	Operation	A0-A14	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	0000h	20h
					Read	0001h	0AAh
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A14	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A14	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising

READ/WRITE MODES (cont'd)

edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

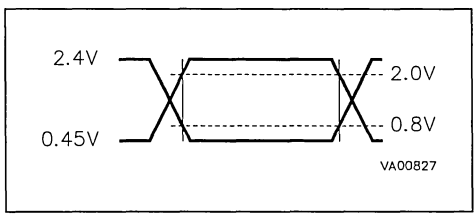


Figure 4. AC Testing Load Circuit

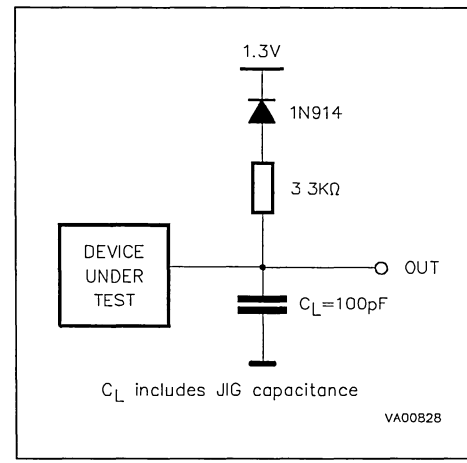


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 6MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		200	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±100	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±100	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grade 6)		0.45	V
V_{OH}	Output High Voltage CMOS	$I_{OH} = -100\mu A$	4.1		V
		I_{OH} = –1mA	V_{CC} –0.8		V
		I_{OH} = –2.5mA (grade 1)	V_{CC} –0.8		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID} (grade 1)		200	µA
		A9 = V_{ID} (grade 6)		500	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% Tested. Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F256A -12		Unit
				Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics
(((T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F256A -15		M28F256A -20		Unit
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0	=	0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

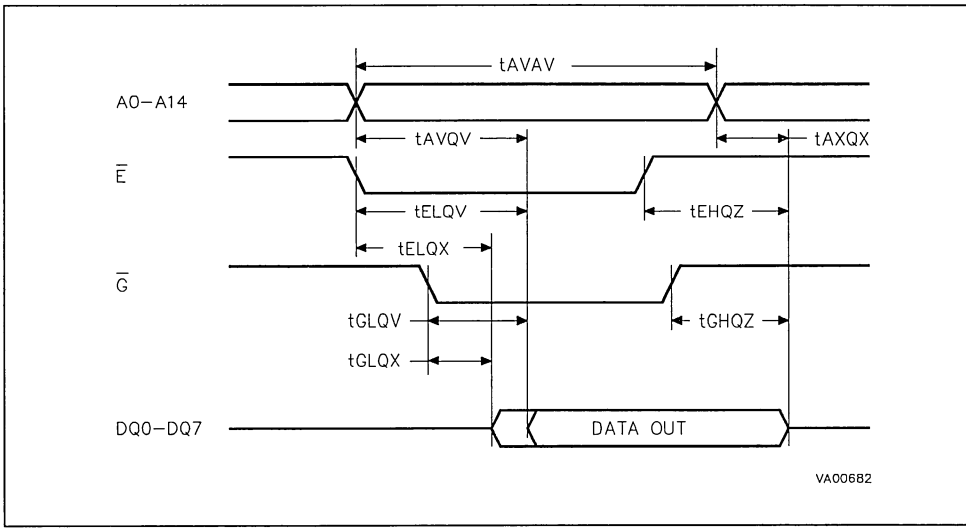


Figure 6. Read Command Waveforms

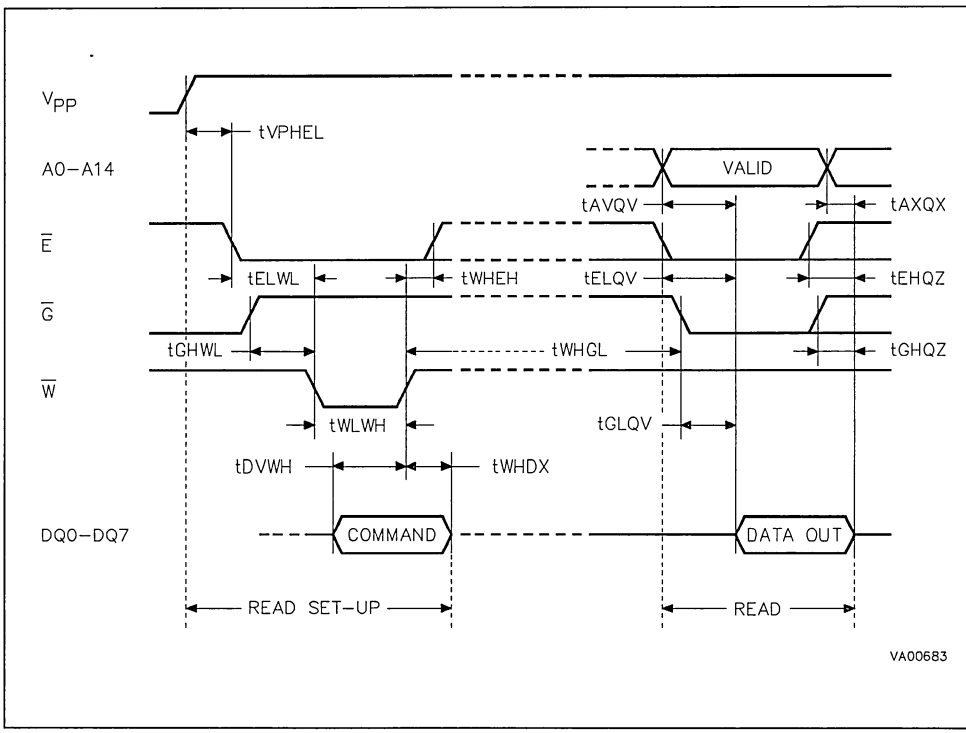


Figure 7. Electronic Signature Command Waveforms

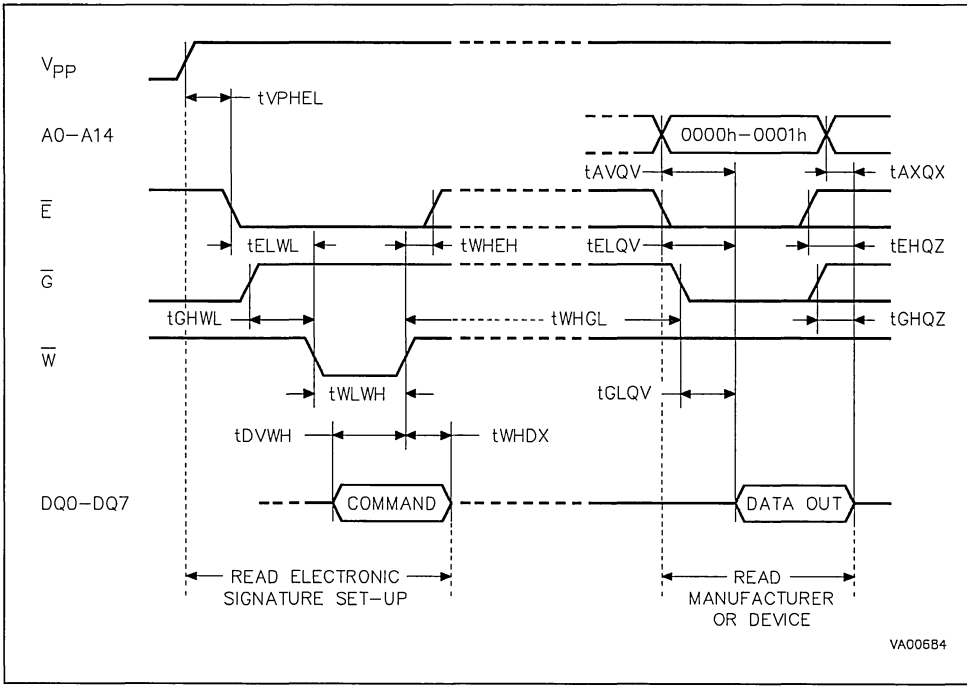


Table 9A. Read/Write Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or V_{CC} = 5V ± 10%: V_{PP} = 12V)

Symbol	Alt	Parameter	M28F256A -12		Unit
			Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	100		ns
t_{WHWH3}	t_{WC}	Write Cycle Time	120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		ns
t_{ELEH} (2)		Chip Enable Low to Chip Enable High (Write Pulse)	70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		ns
t_{WHWH1}		Duration of Program Operation	10		µs
t_{WHWH2}		Duration of Erase Operation	9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		120	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		120	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		50	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z		40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		ns

Notes: 1. Sampled only, not 100% tested
2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Table 9B. Read/Write Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or V_{CC} = 5V ± 10%: V_{PP} = 12V)

Symbol	Alt	Parameter	M28F256A				Unit
			-15		-20		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	100		100		ns
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH} (2)		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	10		10		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested
2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

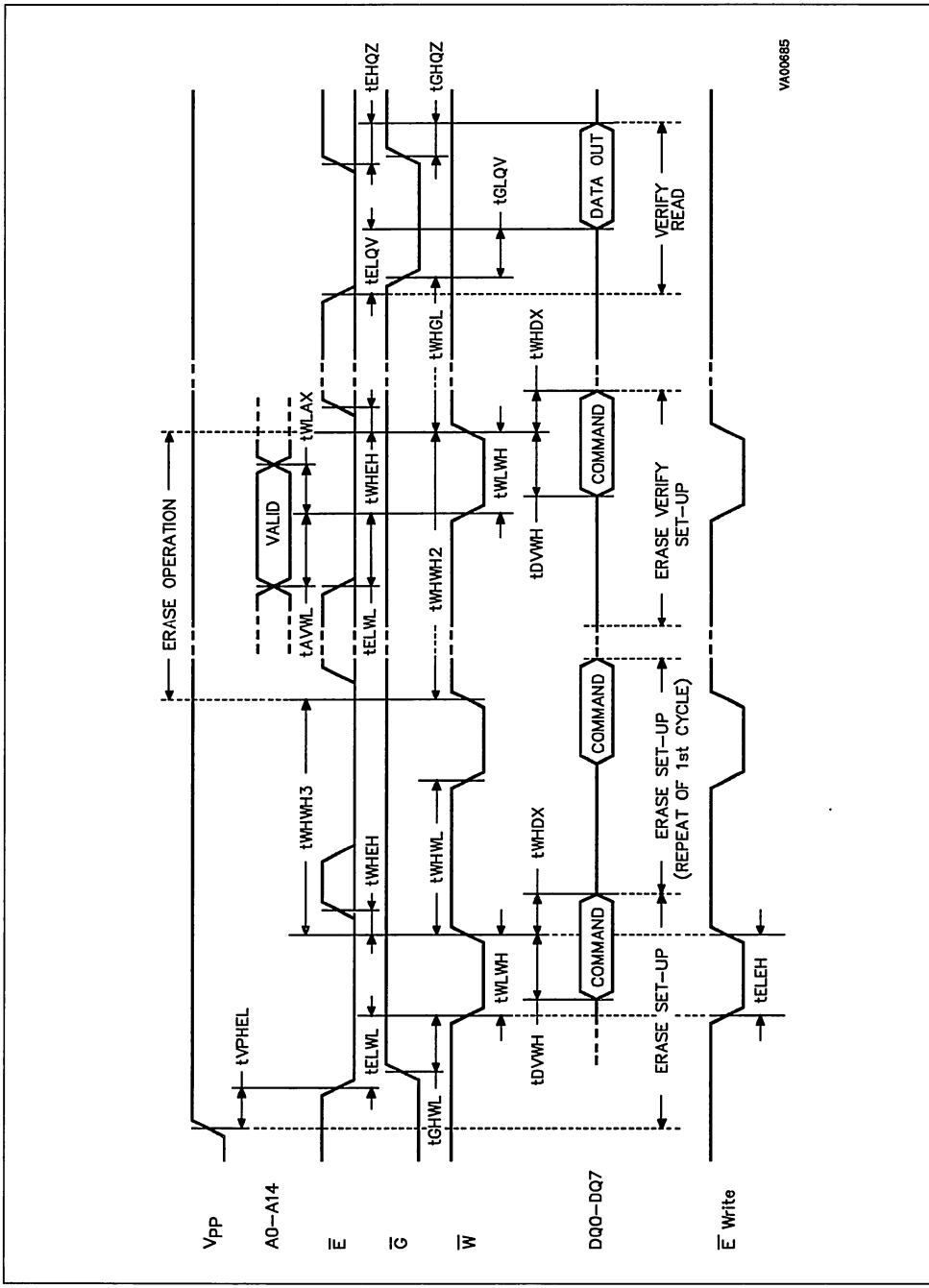


Figure 9. Program Set-up and Program Verify Commands Waveforms

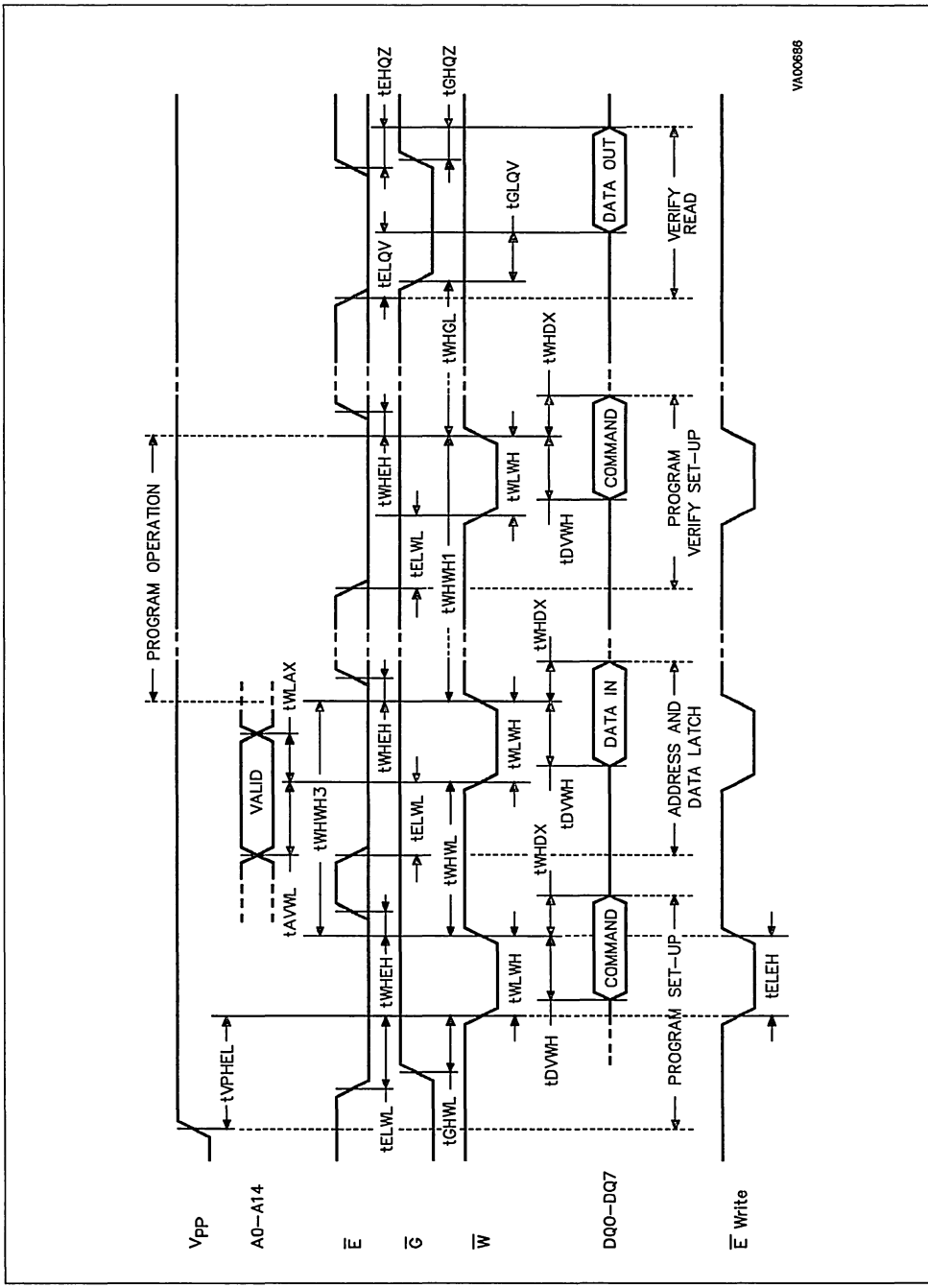


Figure 10. Erasing Flowchart

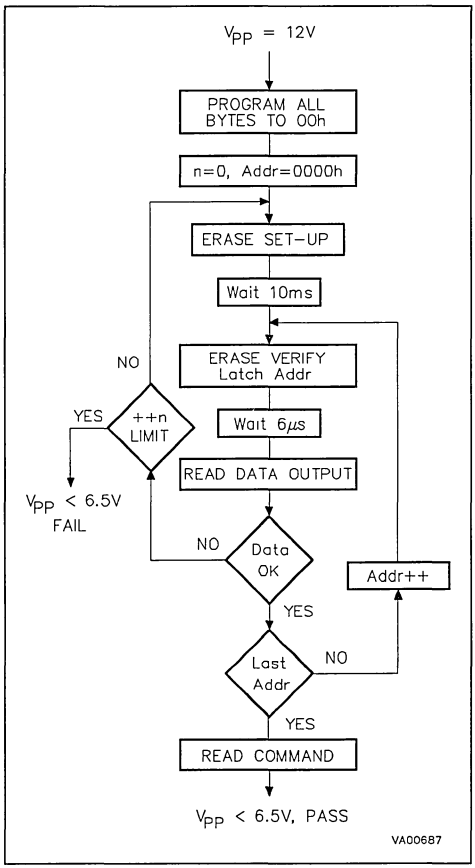
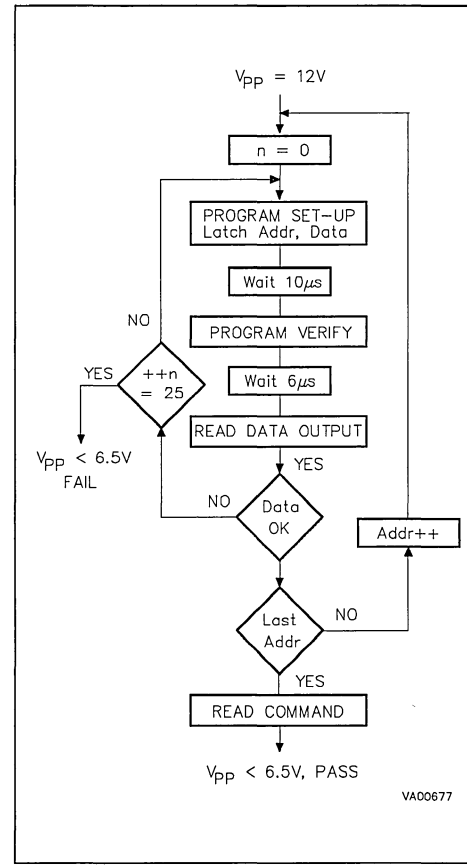


Figure 11. Programming Flowchart



Limit: 1000 at grades 1 & 6; 6000 at grade 3.

PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME

Example: M28F256A -12 X B 1 TR

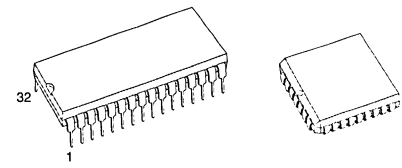
Speed		V_{CC} Tolerance		Package		Temp. Range		Option	
-12	120 ns	blank	± 10%	B	PDIP32	1	0 to 70 °C	Y3	1,000 Cycles
-15	150 ns	X	± 5%	C	PLCC32	3	–40 to 125 °C	TR	Tape & Reel Packing
-20	200 ns					6	–40 to 85 °C		

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

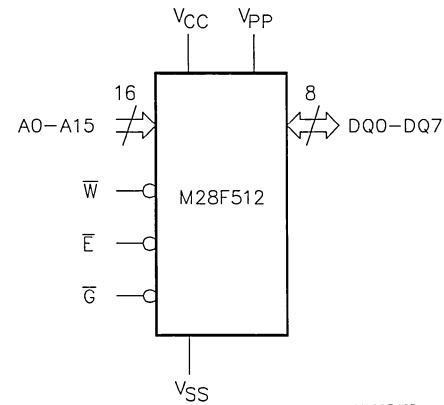
CMOS 512K (64K x 8, Chip Erase) FLASH MEMORY

- FAST ACCESS TIME: 120ns
- LOW POWER CONSUMPTION
  - Standby Current: 200µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE IN 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



PDIP32 (B) PLCC32 (C)

Figure 1. Logic Diagram



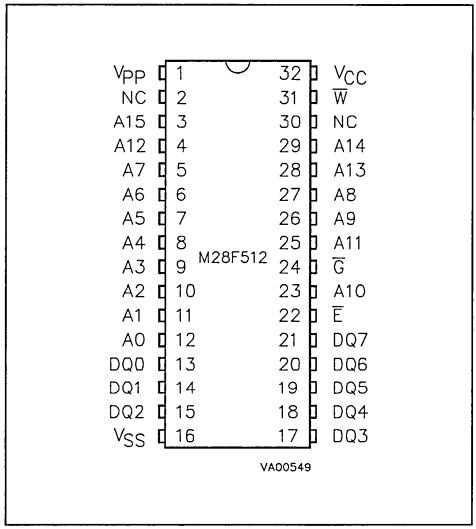
DESCRIPTION

The M28F512 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 64K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F512 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

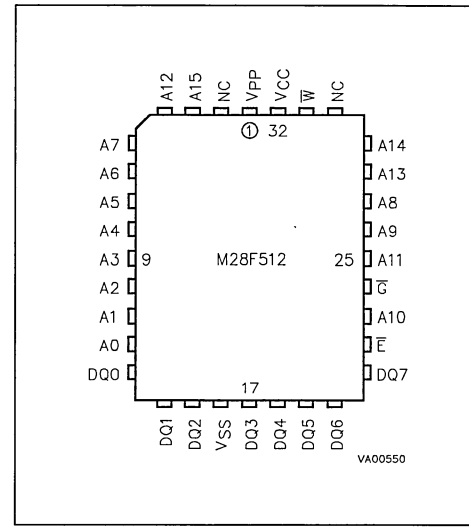
A0 - A15	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F512 FLASH MEMORY employs a technology similar to a 512K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F512 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

Read Mode. The M28F512 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 200µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when V_{PP} is $\leq$ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	0	1	0	02h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A15	DQ0-DQ7	Operation	A0-A15	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	0000h	20h
					Read	0001h	02h
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A15	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A15	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is

READ/WRITE MODES (cont'd)

followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

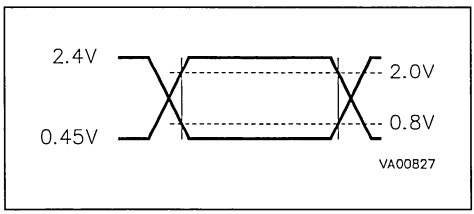


Figure 4. AC Testing Load Circuit

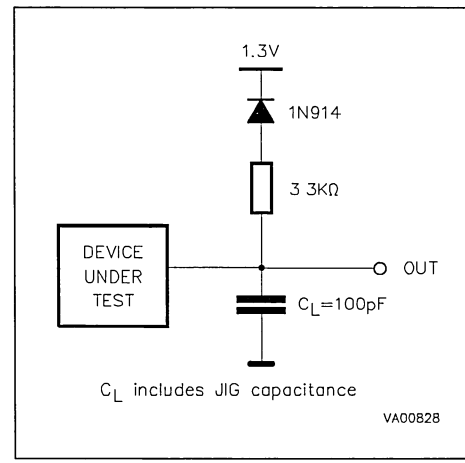


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 6MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		200	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±100	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±100	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grade 6)		0.45	V
V_{OH}	Output High Voltage CMOS	$I_{OH} = -100\mu A$	4.1		V
		I_{OH} = –1mA	V_{CC} –0.8		V
		I_{OH} = –2.5mA (grade 1)	V_{CC} –0.8		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	$A9 = V_{ID}$		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% tested. Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F512 -12		Unit
				Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics
((T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F512 -15		-20		Unit
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0	=	0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

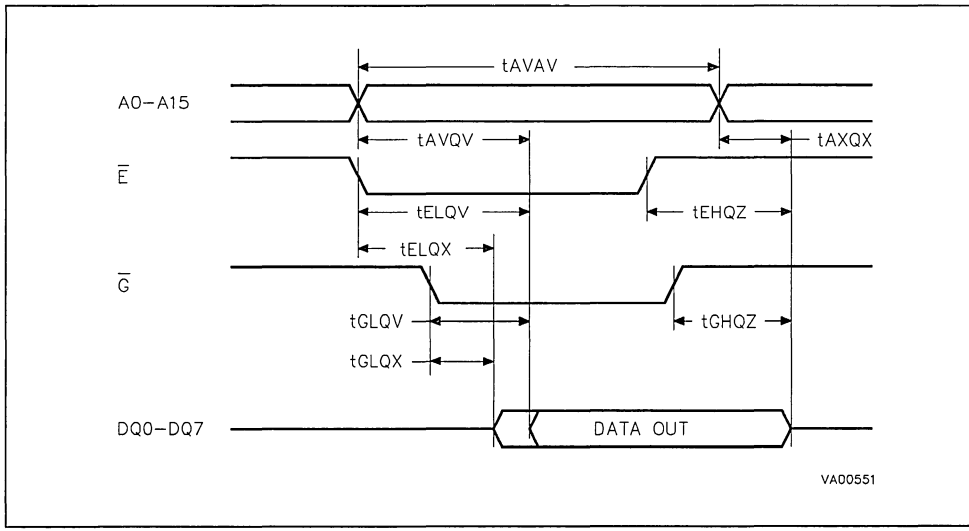


Figure 6. Read Command Waveforms

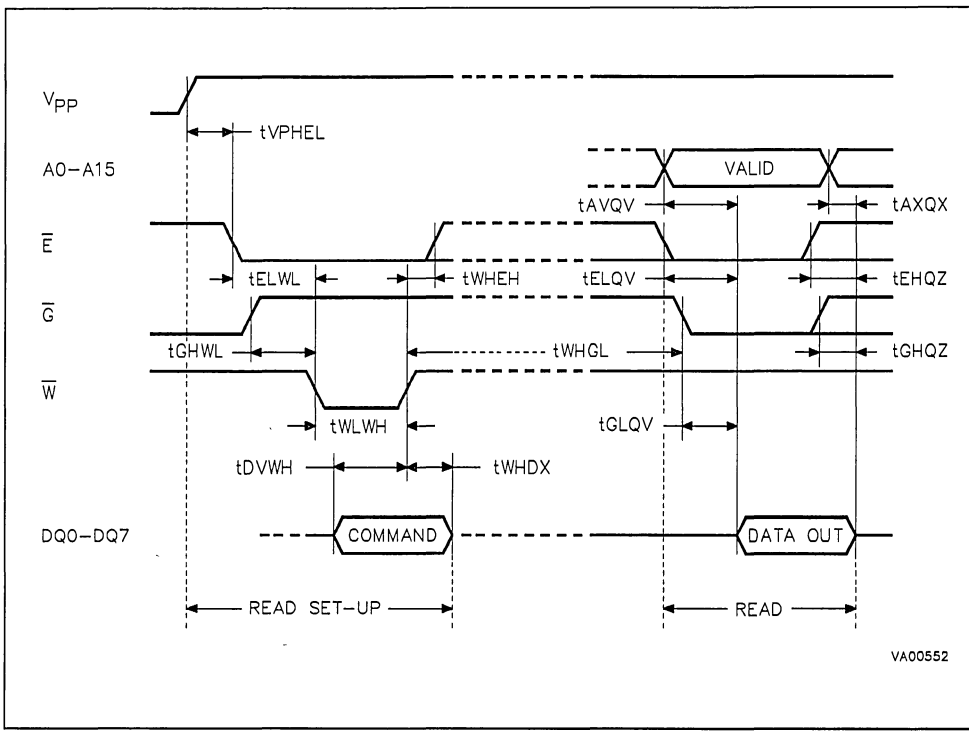


Figure 7. Electronic Signature Command Waveforms

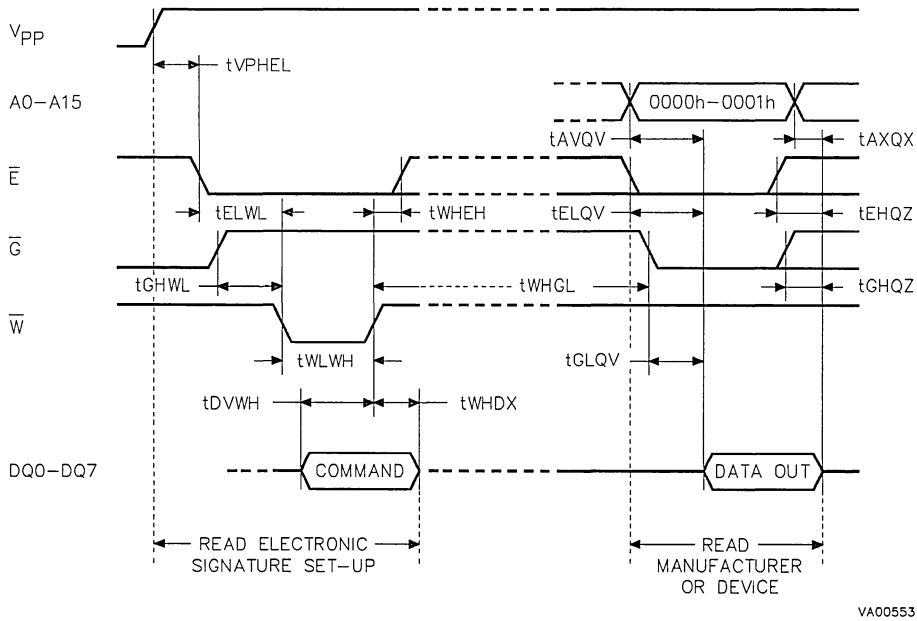


Table 9A. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Alt	Parameter	M28F512 -12		Unit
			Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		ns
t_{WHWH1}		Duration of Program Operation	9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		50	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		ns

Notes: 1. Sampled only, not 100% tested
2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Table 9B. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Alt	Parameter	M28F512				Unit
			-15		-20		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		60		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested
2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

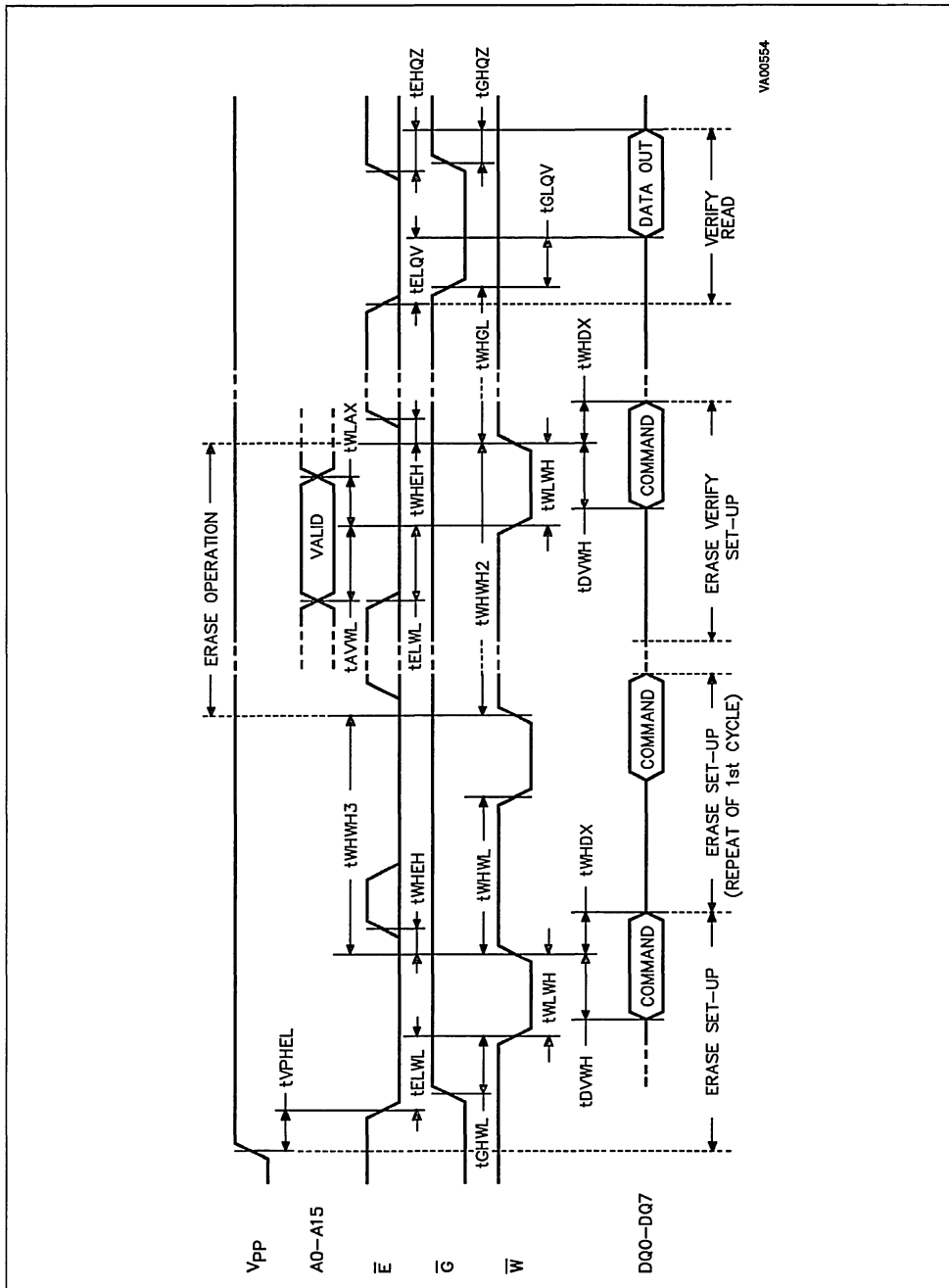


Figure 9. Program Set-up and Program Verify Commands Waveforms - $\overline{W}$ Controlled

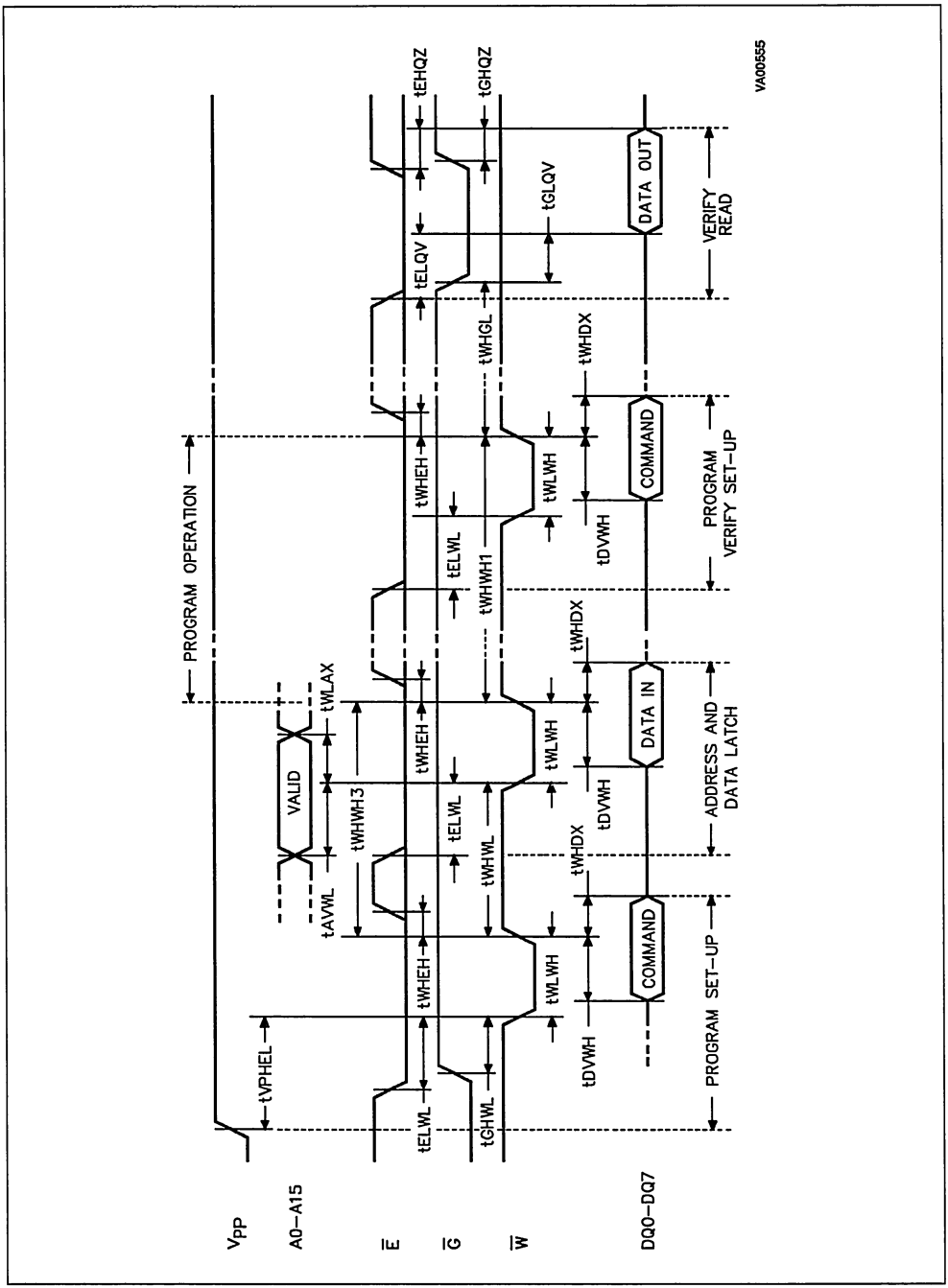


Figure 10. Program Set-up and Program Verify Commands Waveforms - $\overline{E}$ Controlled

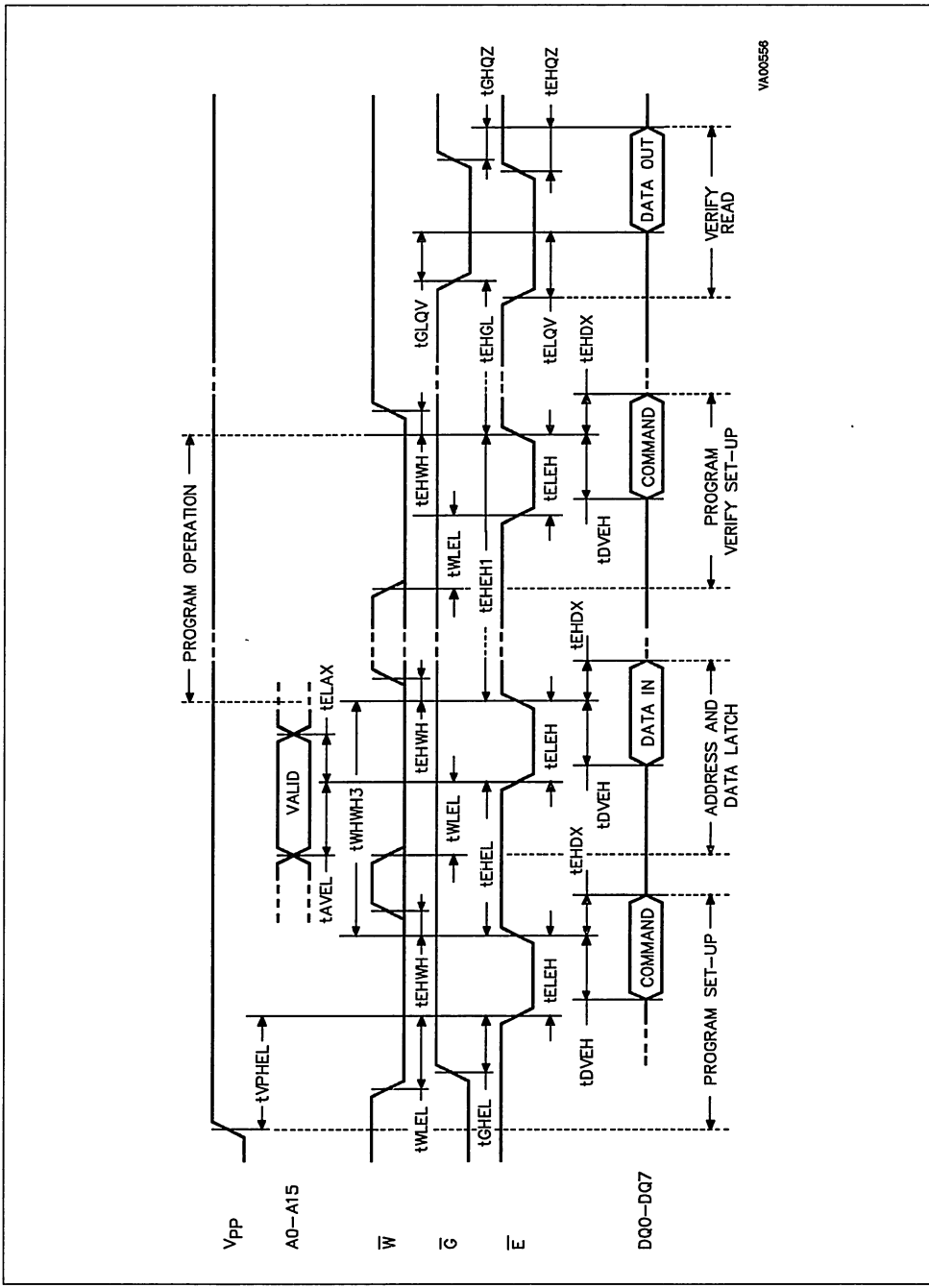


Figure 11. Erasing Flowchart

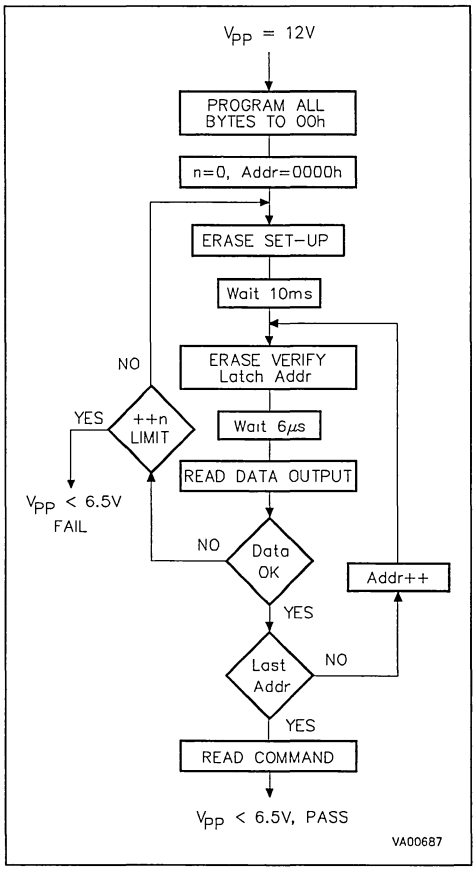
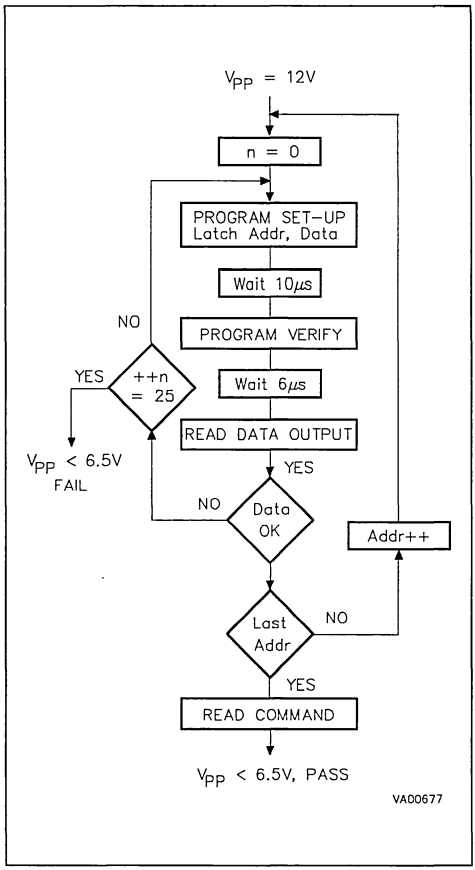


Figure 12. Programming Flowchart



Limit: 1000 at grades 1 & 6; 6000 at grade 3.

PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME

Example: M28F512 -12 X C 1 TR

Speed		V_{CC} Tolerance		Package		Temp. Range		Option	
-12	120 ns	blank	± 10%	B	PDIP32	1	0 to 70 °C	Y3	1,000 Cycles
-15	150 ns	X	± 5%	C	PLCC32	3	–40 to 125 °C	TR	Tape & Reel Packing
-20	200 ns					6	–40 to 85 °C		

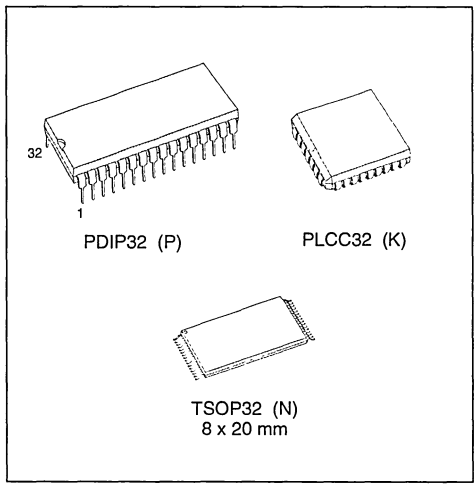
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 1 Megabit (128K x 8, Chip Erase) FLASH MEMORY

ADVANCE DATA

- FAST ACCESS TIME: 100ns
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE in 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



DESCRIPTION

The M28F101 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 128K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F101 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Figure 1. Logic Diagram

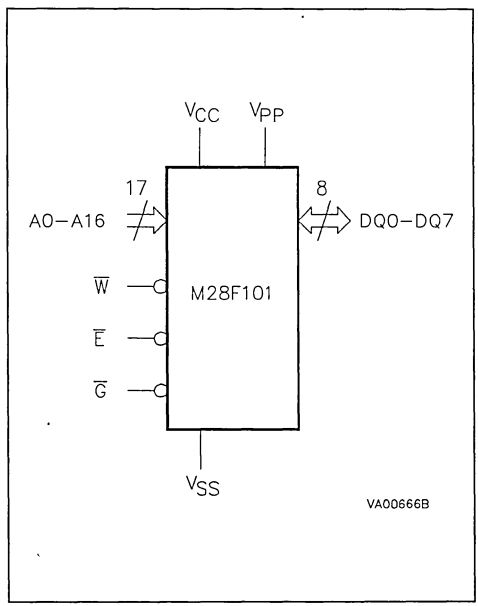
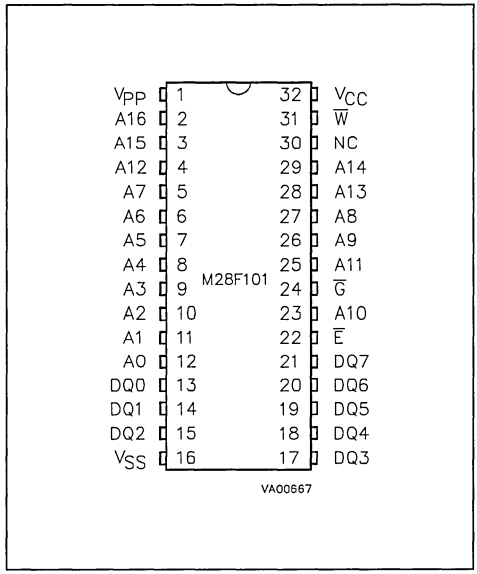


Table 1. Signal Names

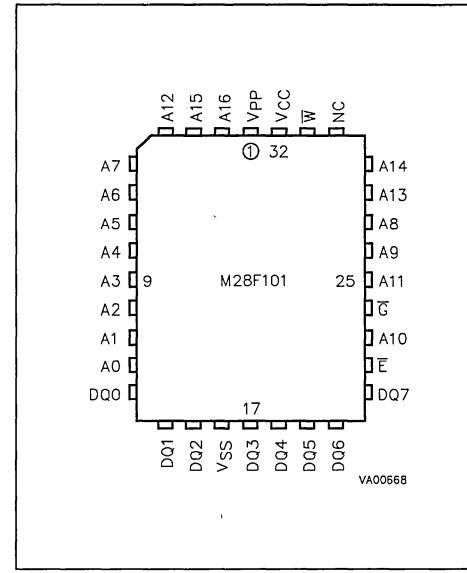
A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



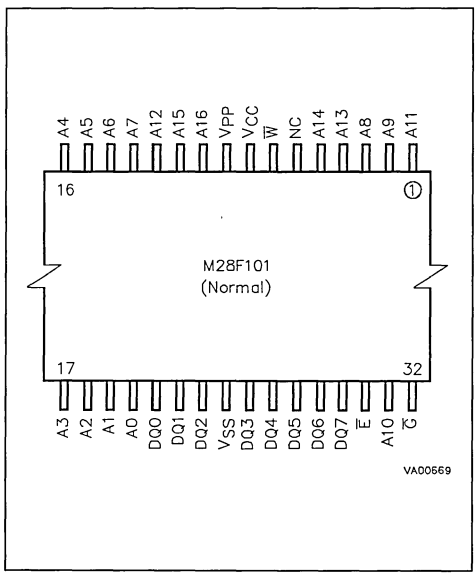
Warning: NC = No Connection

Figure 2B. LCC Pin Connections



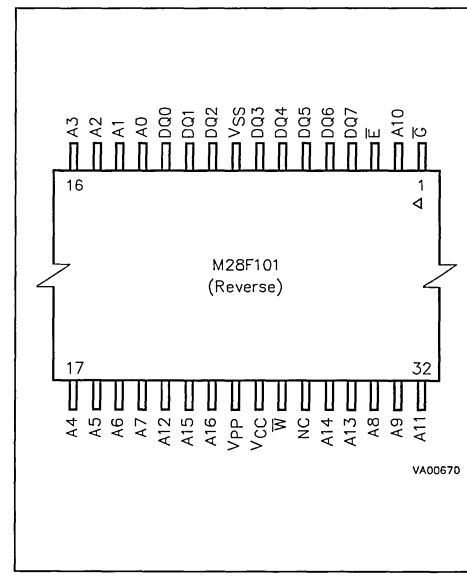
Warning: NC = No Connection

Figure 2C. TSOP Pin Connections



Warning: NC = No Connection

Figure 2D. TSOP Reverse Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F101 FLASH MEMORY employs a technology similar to a 1 Megabit EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F101 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command regsiter is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is don't care.

Read Mode. The M28F101 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 100µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	1	1	07h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A16	DQ0-DQ7	Operation	A0-A16	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	00000h	20h
					Read	00001h	07h
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A16	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A16	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when V_{PP} is ≤ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 00000h or 00001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

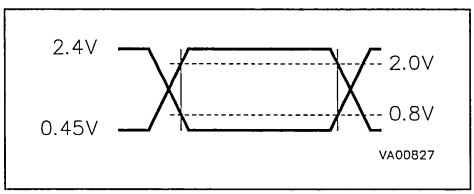


Figure 4. AC Testing Load Circuit

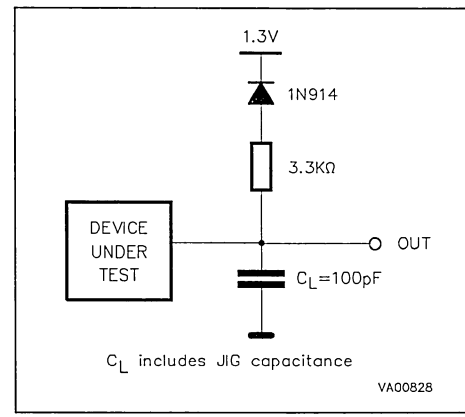


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 6MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		15	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		15	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±10	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±10	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grade 6)		0.45	V
V_{OH}	Output High Voltage CMOS	$I_{OH} = -100\mu A$	4.1		V
		I_{OH} = –2.5mA	0.85 V_{CC}		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	$A9 = V_{ID}$		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% tested. Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F101				Unit
				-100		-120		
				Min	Max	Min	Max	
t_{WHGL}		Write Enable High to Output Enable Low		6		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	45	0	55	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics
(((T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F101				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{WHGL}		Write Enable High to Output Enable Low		6		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0	=	0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

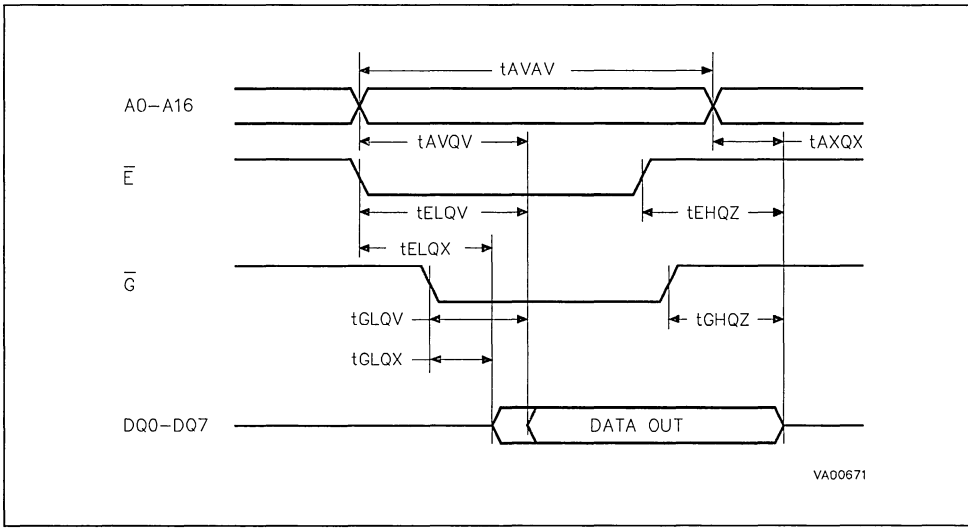


Figure 6. Read Command Waveforms

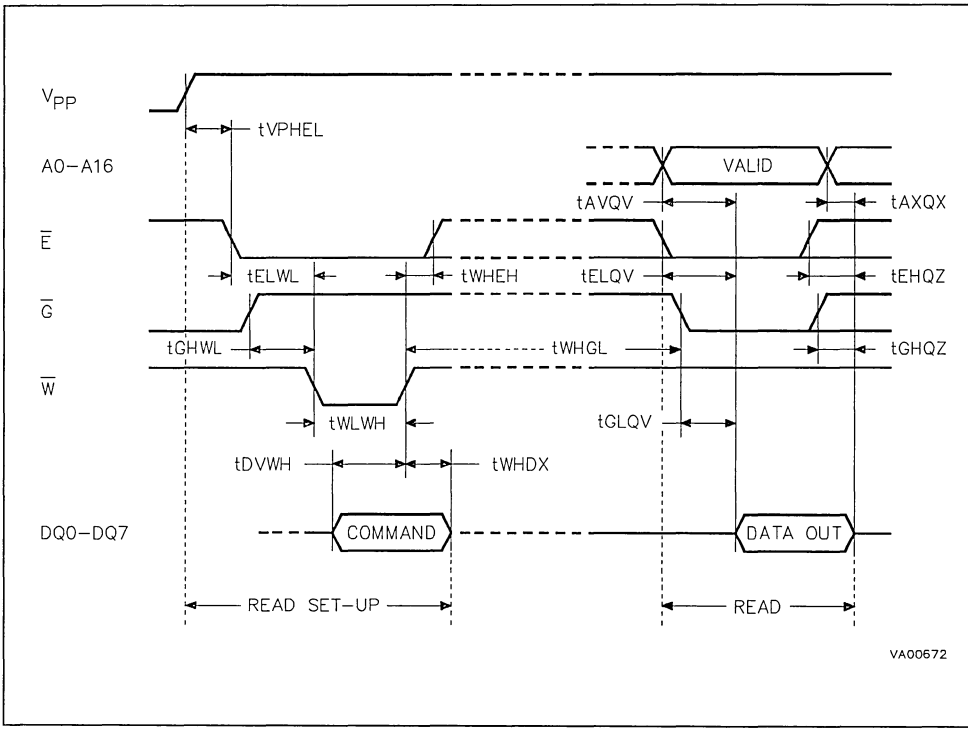
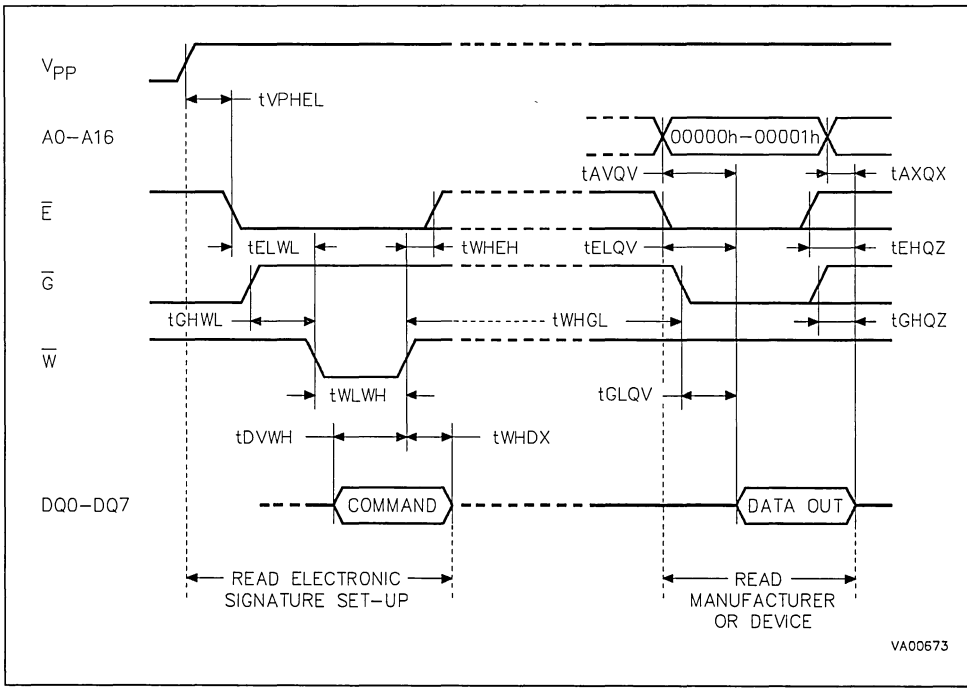


Figure 7. Electronic Signature Command Waveforms



READ/WRITE MODES (cont'd)

to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

Table 9A. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Alt	Parameter	M28F101				Unit
			-100		-120		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		60		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		40		50	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Note: 1. Sampled only, not 100% tested

Table 9B. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Alt	Parameter	M28F101				Unit
			-150		-200		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

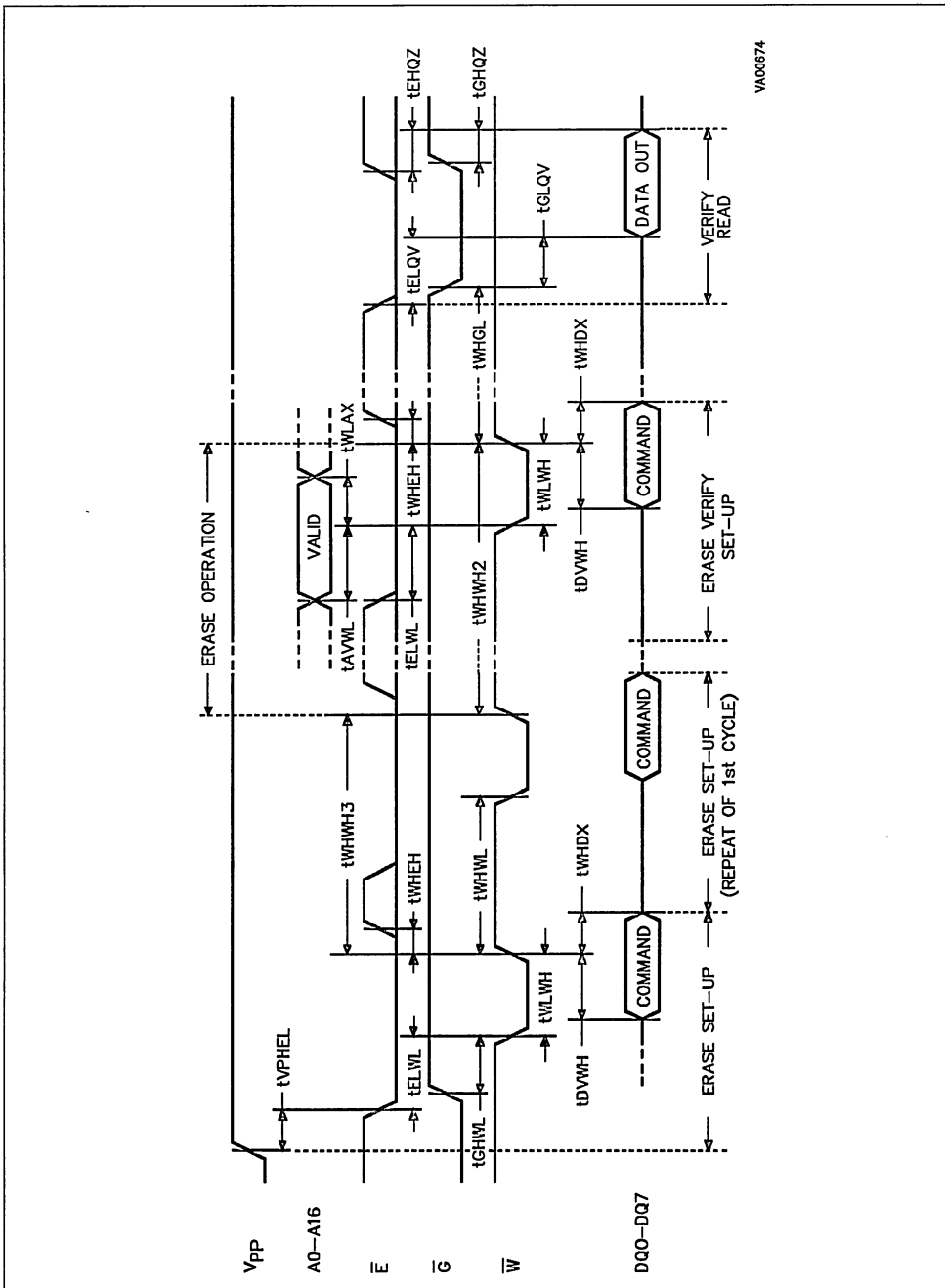


Figure 9. Program Set-up and Program Verify Commands Waveforms - $\overline{W}$ Controlled

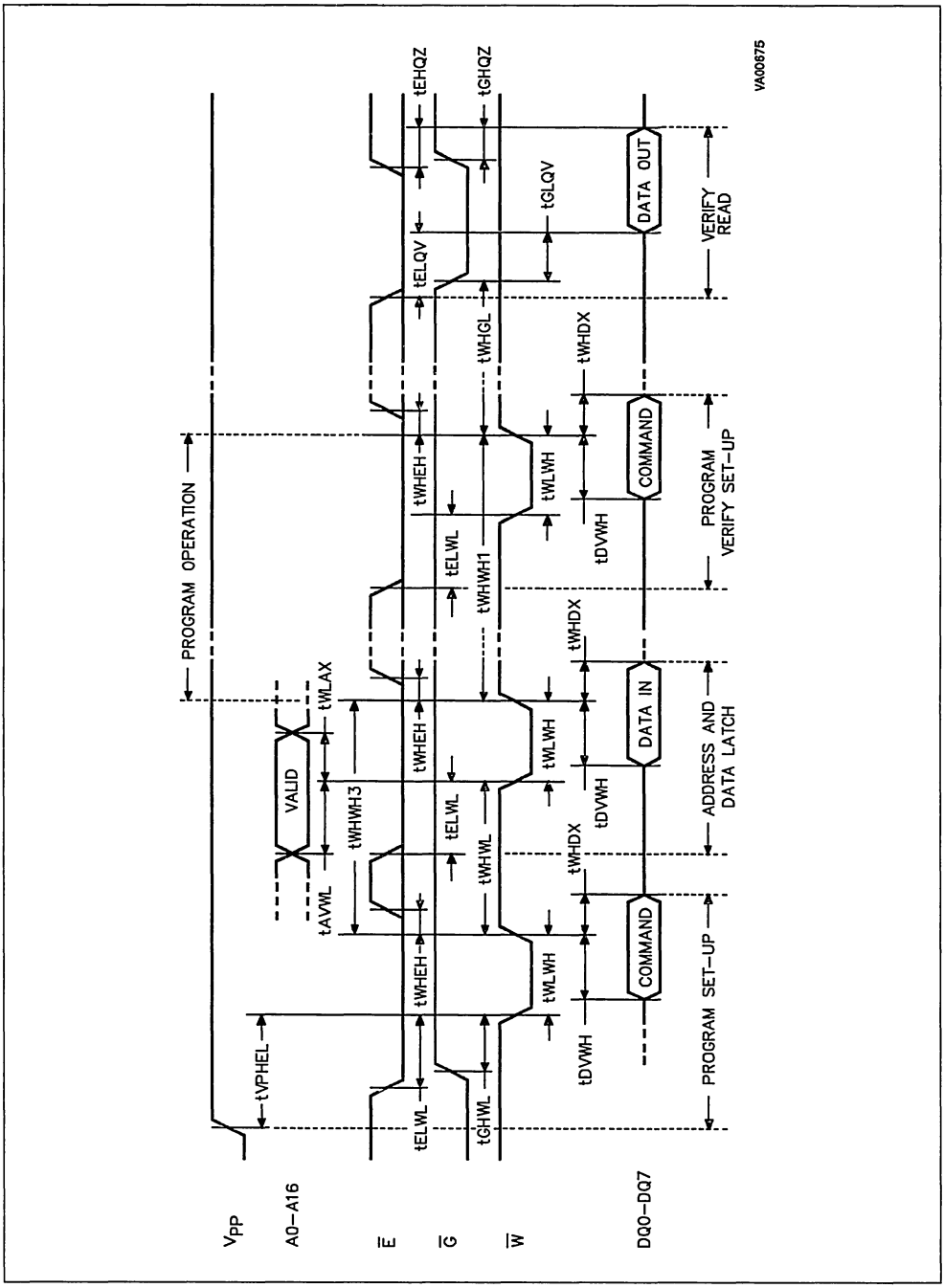


Figure 10. Program Set-up and Program Verify Commands Waveforms - $\overline{E}$ Controlled

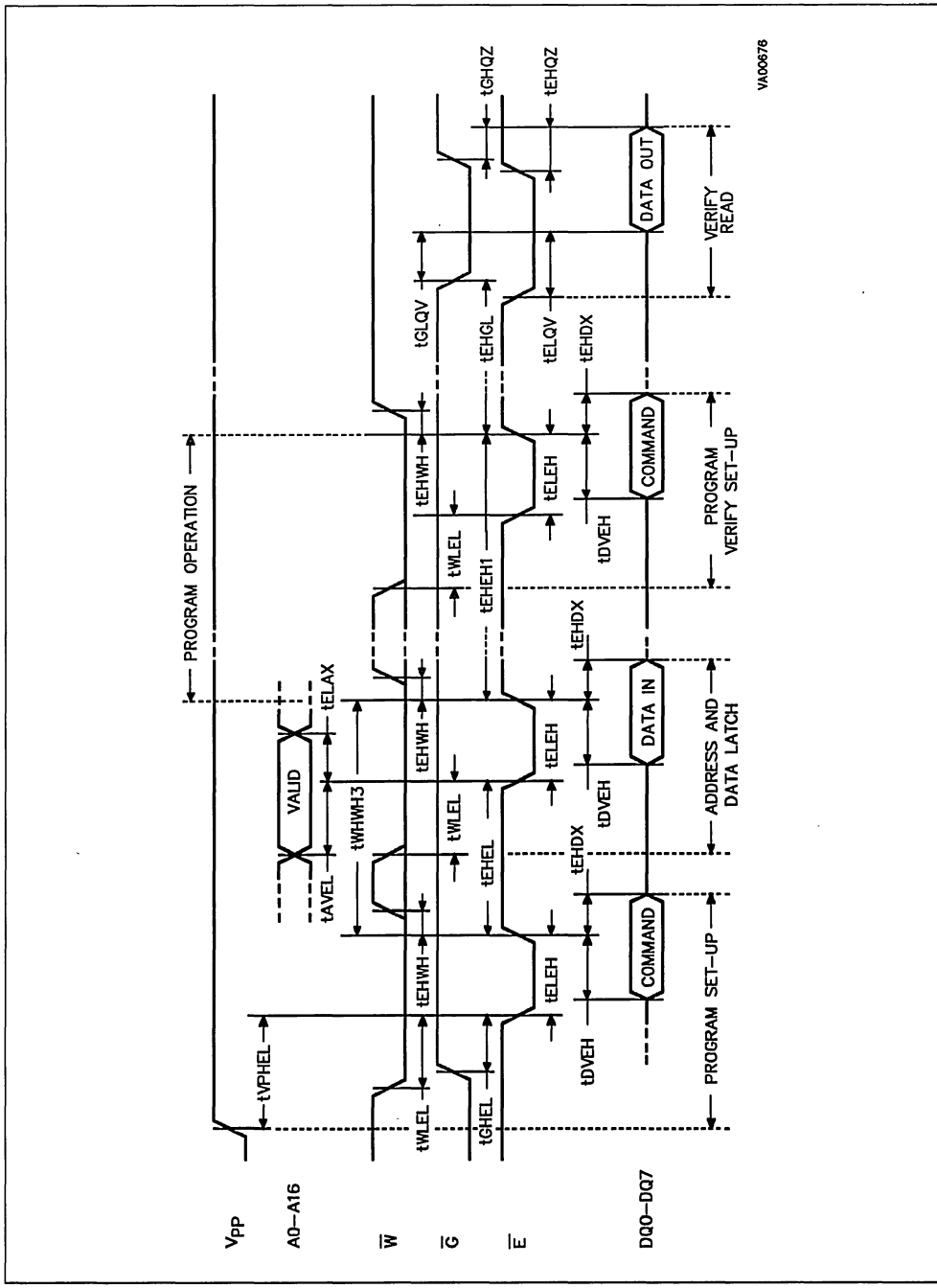


Figure 11. Erasing Flowchart

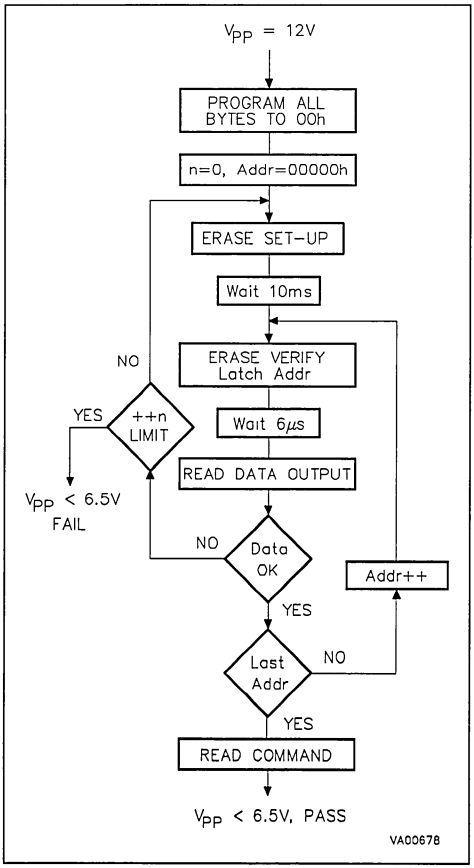
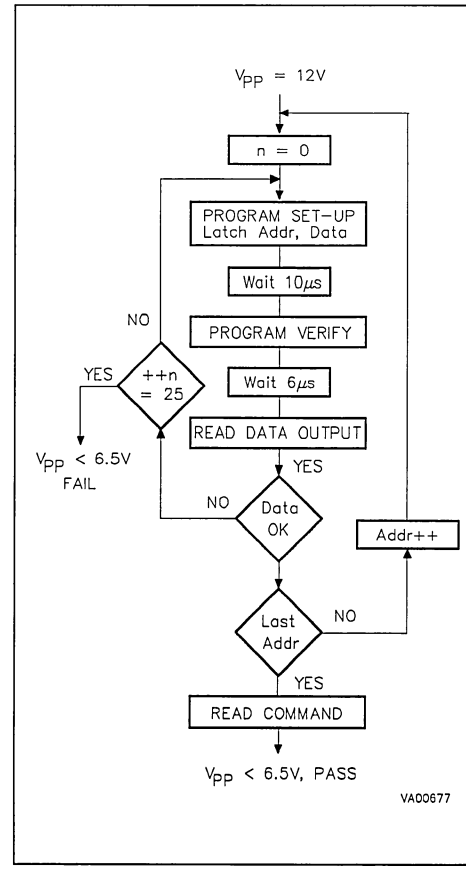


Figure 12. Programming Flowchart



Limit: 1000 at grade 1; 6000 at grades 3 & 6.

PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME

Example: M28F101 -100 X N 1 R

Speed		V_{CC} Tolerance		Package		Temp. Range		Option	
-100	100 ns	blank	± 10%	P	PDIP32	1	0 to 70 °C	R	Reverse Pin-Out
-120	120 ns	X	± 5%	K	PLCC32	3	–40 to 125 °C	Y3	1,000 Cycles
-150	150 ns			N	TSOP32 8 x 20 mm	6	–40 to 85 °C	TR	Tape & Reel Packing
-200	200 ns								

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

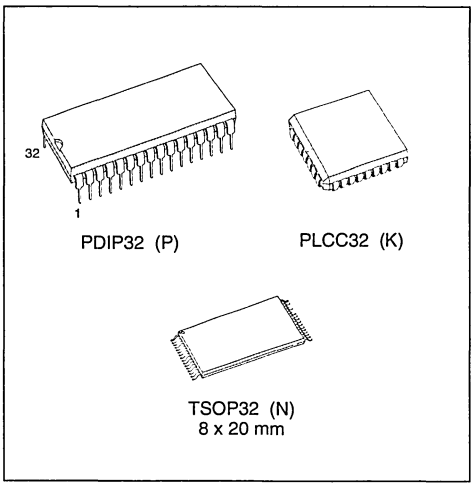
SGS-THOMSON MICROELECTRONICS

M28F101A
M28V101A

CMOS 1 Megabit (128K x 8, Chip Erase) FLASH MEMORY

PRODUCT CONCEPT

- MEMORY CHIP ERASE
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F101A version
  - 3.3V ± 0.3V for M28V101A version
- 12V PROGRAMMING VOLTAGE
- PROGRAM/ERASE CYCLES
  - 100,000 for M28F101A
  - 10,000 for M28V101A
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Data Polling and Toggle Protocol for P/E. C. Status
- LOW POWER CONSUMPTION
  - 30µA Typical in Standby
- FAST ACCESS TIMES
  - 60ns for M28F101A version
  - 150ns for M28V101A version



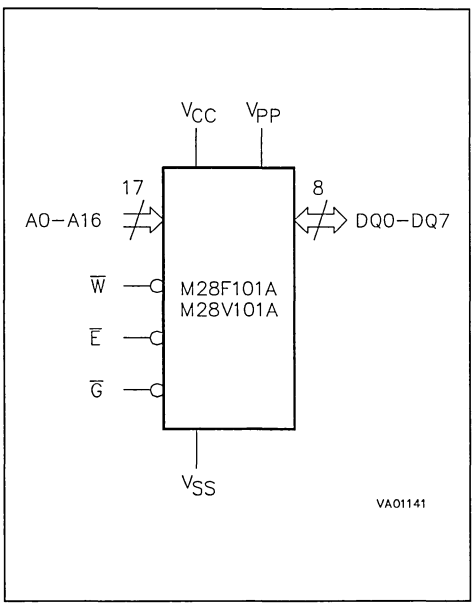
DESCRIPTION

The M28F101A, M28V101A FLASH MEMORY products are non-volatile memories that may be erased electrically in bulk and programmed byte-by-byte. The interface is directly compatible with most microprocessors. The device is available in PDIP32, PLCC32 and TSOP32 (8 x 20mm). Both normal and reverse pin outs are available for the TSOP32 package.

Table 1. Signal Names

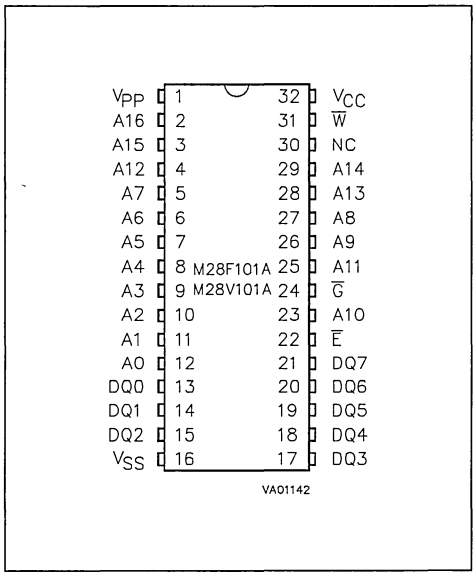
A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



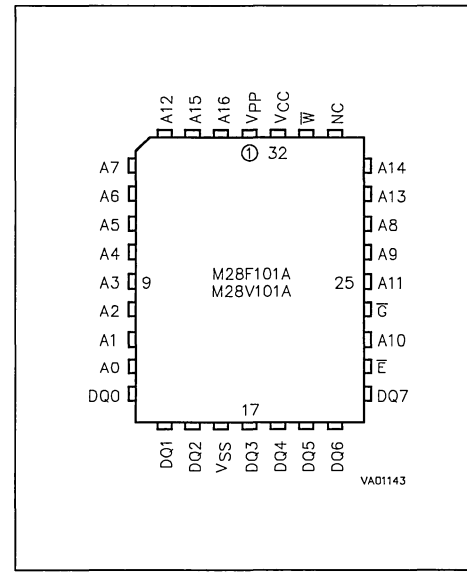
This is advance information on a new product now undergoing evaluation. Details are subject to change without notice.

Figure 2A. DIP Pin Connections



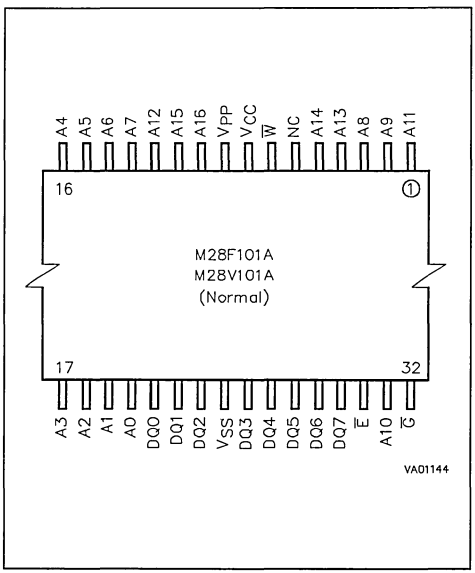
Warning: NC = No Connection

Figure 2B. LCC Pin Connections



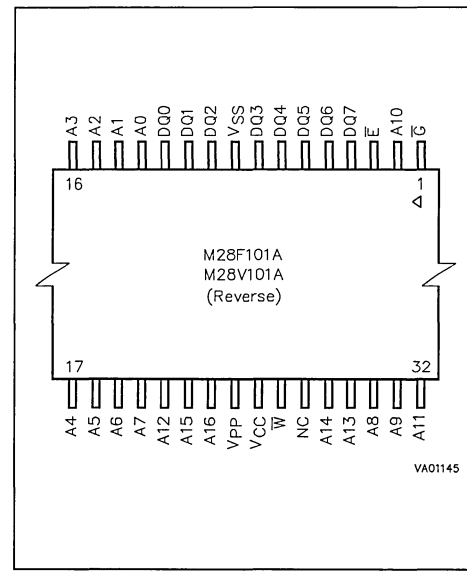
Warning: NC = No Connection

Figure 2C. TSOP Pin Connections



Warning: NC = No Connection

Figure 2D. TSOP Reverse Pin Connections



Warning: NC = No Connection

Organisation

The organisation is 128K x 8 with Address lines A0-A16 and Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs.

Erase and Program are performed under control of the internal Program/Erase Controller (P/E.C.).

Data Output bits DQ7 and DQ6 provide polling or toggle signals during Automatic Program or Erase to indicate the Busy/Ready state of the internal Program/Erase Controller.

Command Interface

The memory is interfaced by 5 operation cycles for reading the array, reading the Electronic Signature, output disable, standby or writing.

Command bytes can be written to a Command Interface latch to perform instructions for reading (array or Electronic Signature), erasure, programing or reset. When power is first applied, or if V_{CC} falls below V_{LKO}, the command interface is reset to read the array.

Instructions

Five instructions are defined to perform Read Memory Array, Read Electronic Signature, Auto Erase, Auto Program and Reset. Instructions are composed of a first command write operation followed by either a second command write, to confirm the commands for programing and erase, or read operations to read data from the memory or to read the Electronic Signature.

For added data protection, the intructions for byte program and erase consist of two commands that are written to the memory. These instructions can be aborted after the first command has been given using the Reset instruction. Byte programing takes typically 6µs. Erasure of the entire memory takes typically 2.4sec when performed by the internal Automatic P/E.C. algorithm.

During an Automatic Program or Erase operation reads to the memory return a byte of which two data bits, DQ7 and DQ6, reflect the Busy/Ready status of the P/E.C.

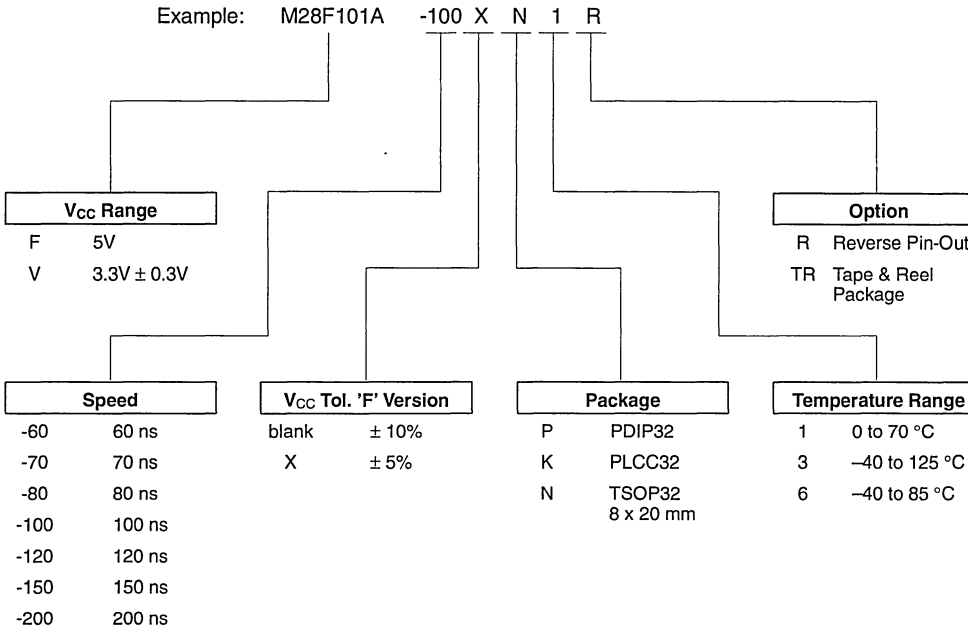
After a Program or Erase command the interface is reset to read the memory array.

Table 2. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address	Data Output
RD	Read Array	1+	Write	X	00h	Read	Address	Array Output
RSIG	Read Electronic Signature	1+	Write	X	80h or 90h	Read	A0 = '0' or '1'	Code Output
EE	Erase Auto	2	Write	X	30h	Write	X	30h
PG	Program Auto	2	Write	X	10h or 50h	Write	Address	Data Input
RST (2)	Reset	1-2	Write	X	0FFh	Write	X	0FFh

Notes: 1. X = Don't Care
2. 1 or 2 cycles may be required, see Instruction descriptions.

ORDERING INFORMATION SCHEME



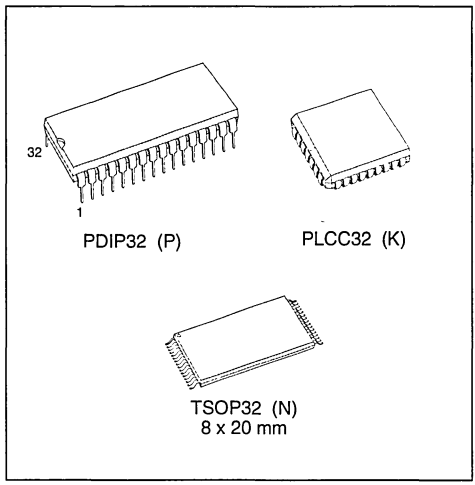
For a list of available options (V_{CC} Range, Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 1 Megabit (128K x 8, Chip Erase) FLASH MEMORY

ADVANCE DATA

- FAST ACCESS TIMES
  - 60ns for M28F101B version
  - 150ns for M28V101B version
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 PROGRAM/ERASE CYCLES
- 12V PROGRAMMING VOLTAGE
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F101B version
  - 3.3V ± 0.3V for M28V101B version
- TYPICAL BYTE PROGRAMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE in 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



DESCRIPTION

The M28F101B, M28V101B FLASH MEMORY products are non-volatile memories which may be erased electrically at the chip level and programmed byte-by-byte. They are organised as 128K bytes of 8 bits. They use a command register architecture to select the operating modes and thus provide a simple microprocessor interface. The M28F101B, M28V101B FLASH MEMORY products are suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 60ns makes the device suitable for

Table 1. Signal Names

A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

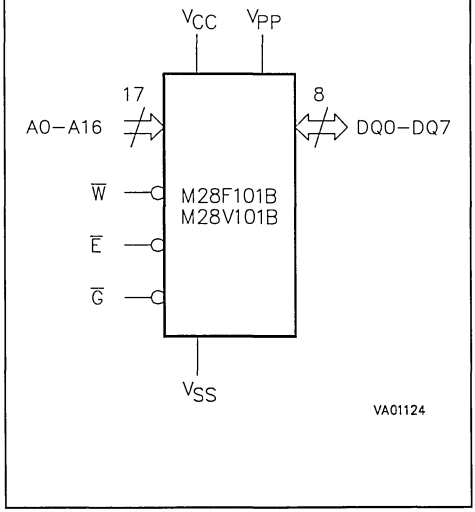
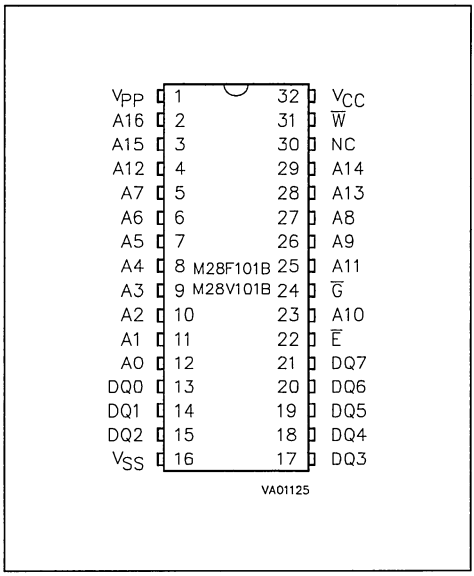
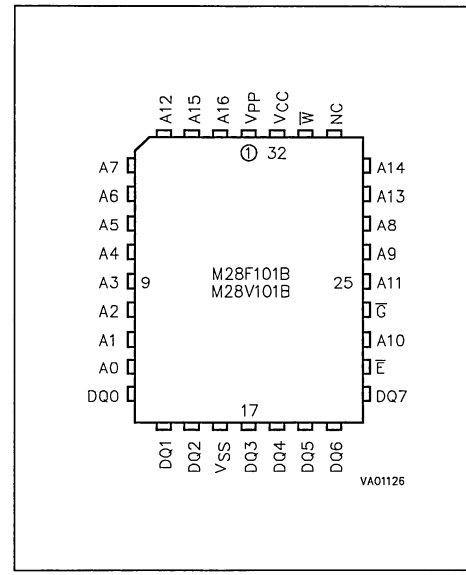


Figure 2A. DIP Pin Connections



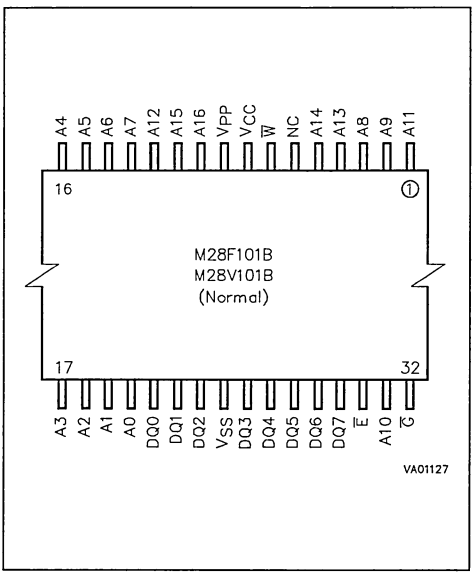
Warning: NC = No Connection

Figure 2B. LCC Pin Connections



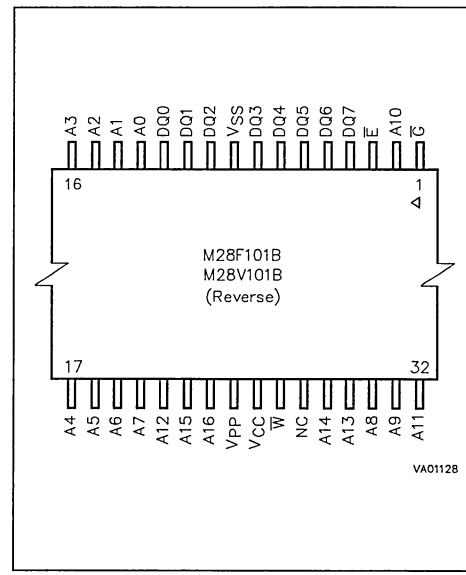
Warning: NC = No Connection

Figure 2C. TSOP Pin Connections



Warning: NC = No Connection

Figure 2D. TSOP Reverse Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

use in high speed microprocessor systems, while the low supply voltage capability makes it ideal for portable applications.

DEVICE OPERATION

The M28F101B, M28V101B FLASH MEMORY products employ a technology similar to a 1 Megabit EPROM but add to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F101 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command regsiter is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is don't care.

Read Mode. The M28F101B, M28V101B have two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 100µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code: M28F101B	V_{IH}	1	1	1	0	1	1	1	0	0EEh
Device Code: M28V101B	V_{IH}	1	1	1	0	1	1	1	1	0EFh

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A16	DQ0-DQ7	Operation	A0-A16	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature (2)	2	Write	X	80h or 90h	Read	00000h	20h
					Read	00001h	0EEh or 0EFh
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A16	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A16	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Electronic Signature Table

READ/WRITE MODES (cont'd)

set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when V_{PP} is ≤ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

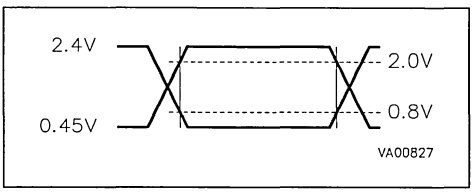


Figure 4. AC Testing Load Circuit

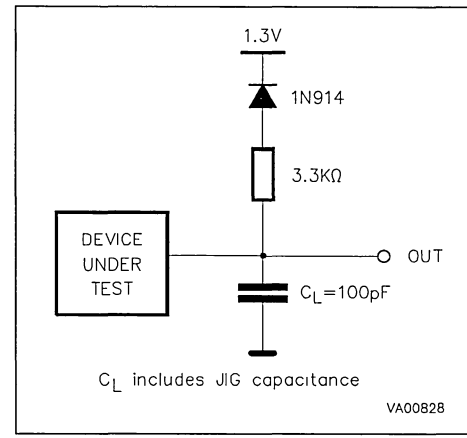


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 10MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		20	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		20	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		20	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±10	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±10	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4		V
		I_{OH} = –2.5mA	0.85 V_{CC}		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	$A9 = V_{ID}$		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out	M28F101B	2.2		V
		M28V101B	2.0		V

Note: 1. Not 100% tested. Characterisation Data available.

Table 8. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F101B -80		Unit
				Min	Max	
t_{WHGL}		Write Enable High to Output Enable Low		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	80		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		80	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		80	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		ns

Note: 1. Sampled only, not 100% tested

READ/WRITE MODES (cont'd)

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 80h or 90h to the command register. The following read cycle, with address inputs 00000h or 00001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

Figure 5. Read Mode AC Waveforms

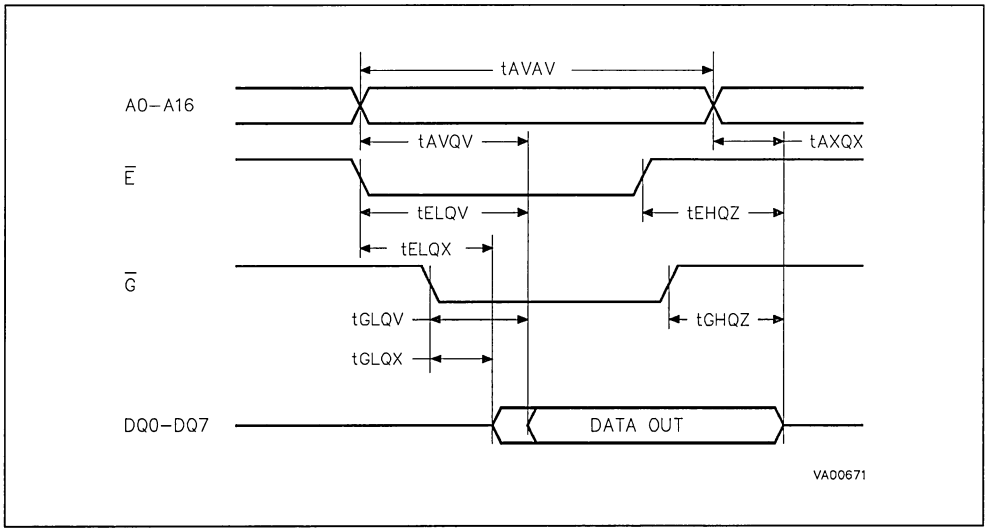


Figure 6. Read Command Waveforms

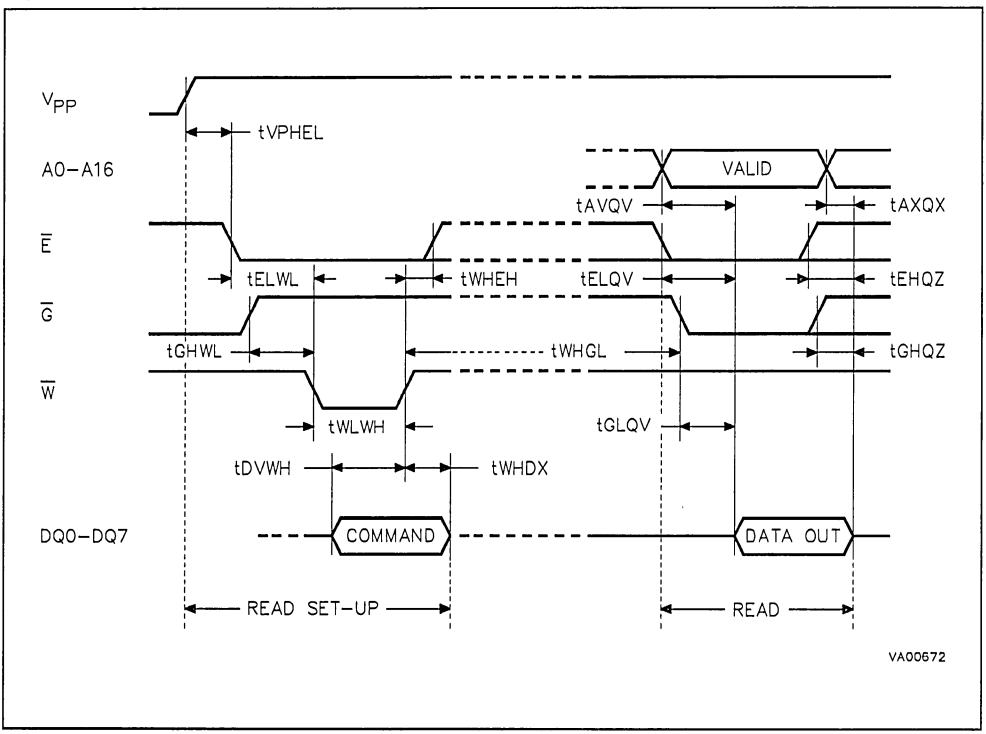
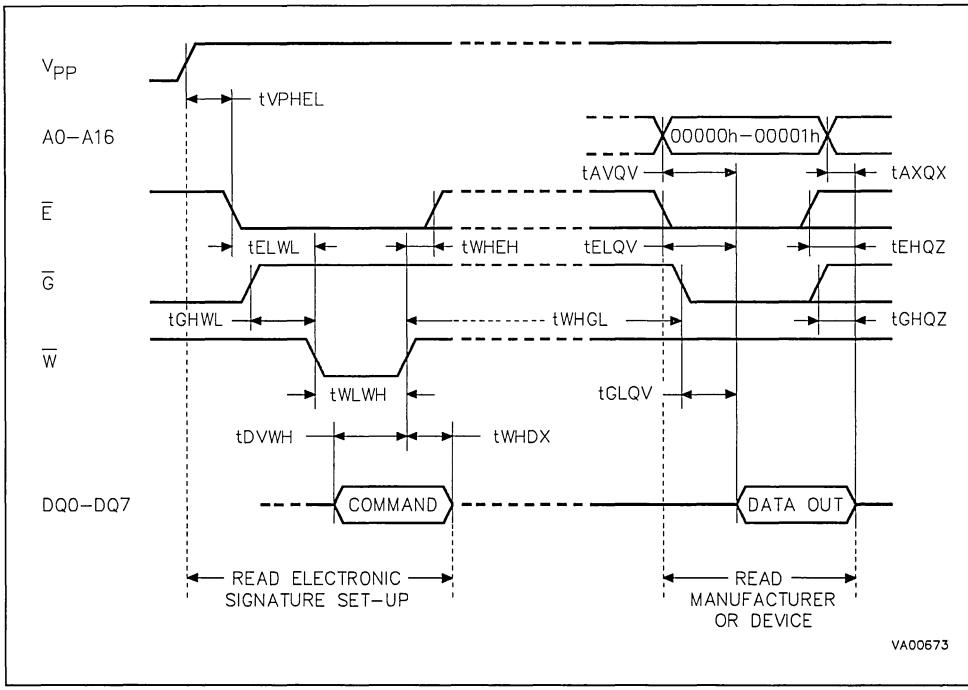


Figure 7. Electronic Signature Command Waveforms



READ/WRITE MODES (cont'd)

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

Table 9. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	M28F101B		Unit
			-80		
			Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	80		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		ns
t_{ELAX}		Chip Enable Low to Address Transition	60		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	45		ns
t_{DVEH}		Input Valid to Chip Enable High	50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	45		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	60		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		ns
t_{EHDX}		Chip Enable High to Input Transition	0		ns
t_{WHWH1}		Duration of Program Operation	10		µs
t_{EHEH1}		Duration of Program Operation	10		µs
t_{WHWH2}		Duration of Erase Operation	9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		80	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		80	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		35	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		35	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		ns

Note: 1. Sampled only, not 100% tested

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

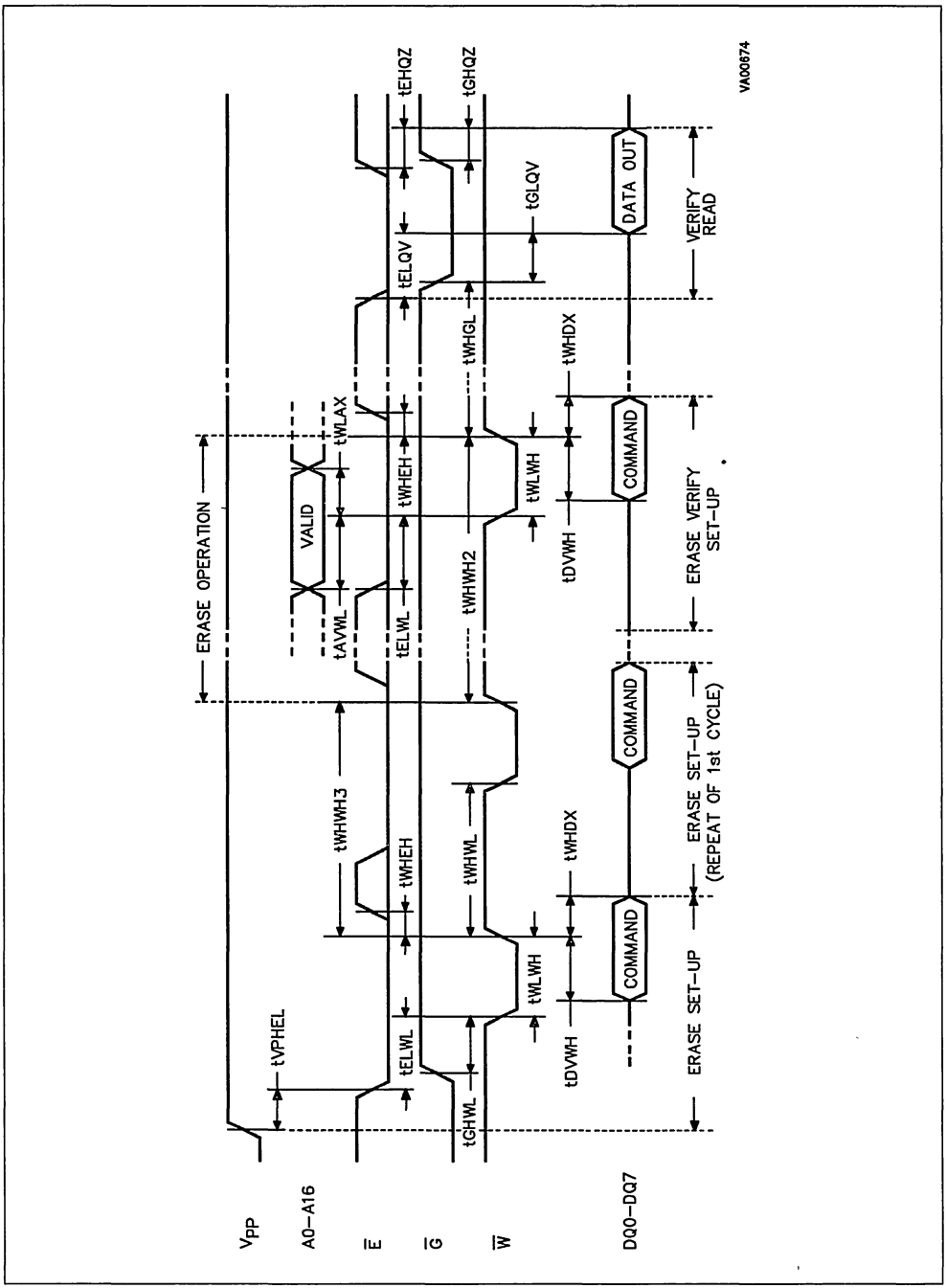


Figure 9. Program Set-up and Program Verify Commands Waveforms - $\overline{W}$ Controlled

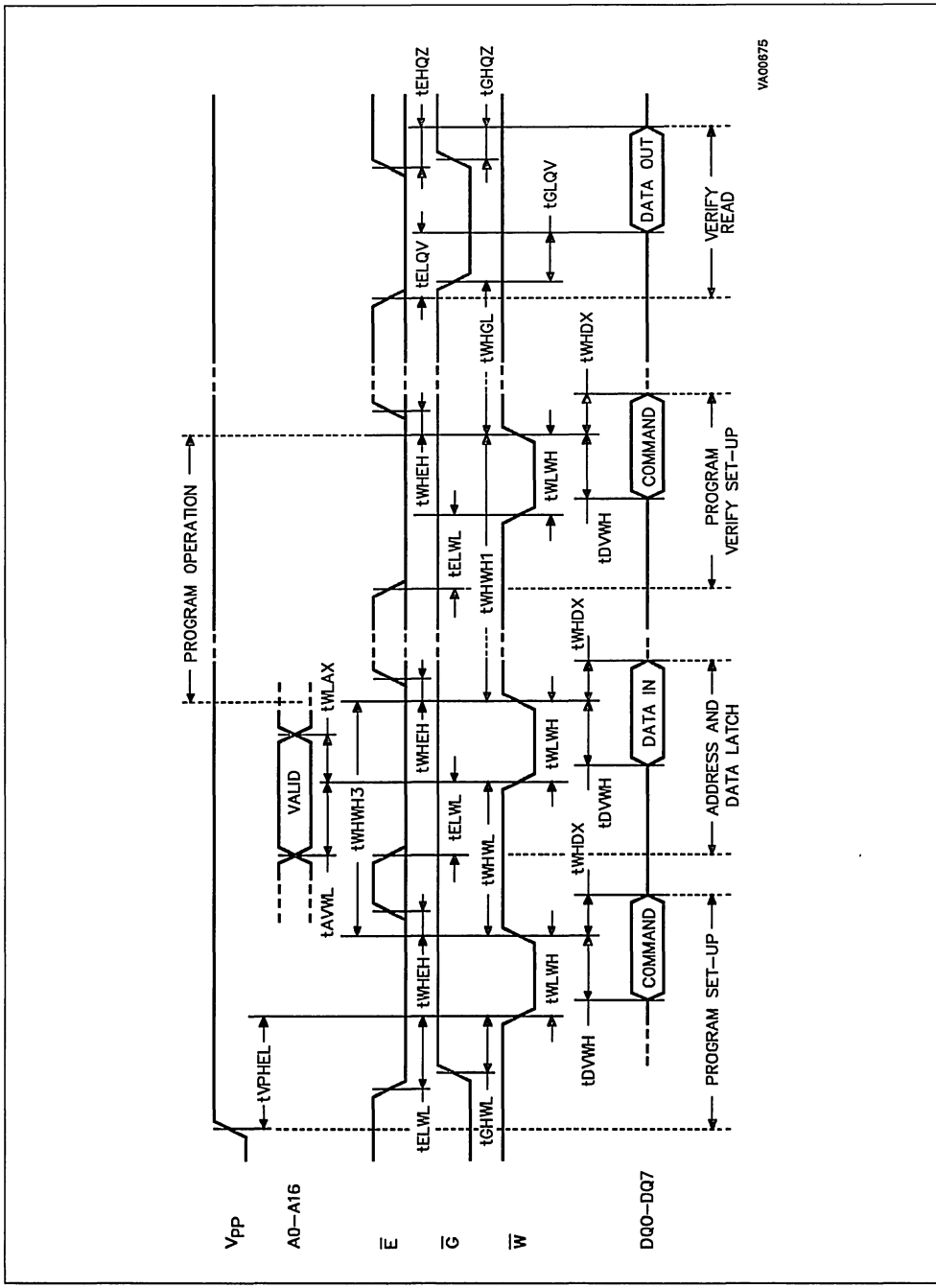


Figure 10. Program Set-up and Program Verify Commands Waveforms - $\overline{E}$ Controlled

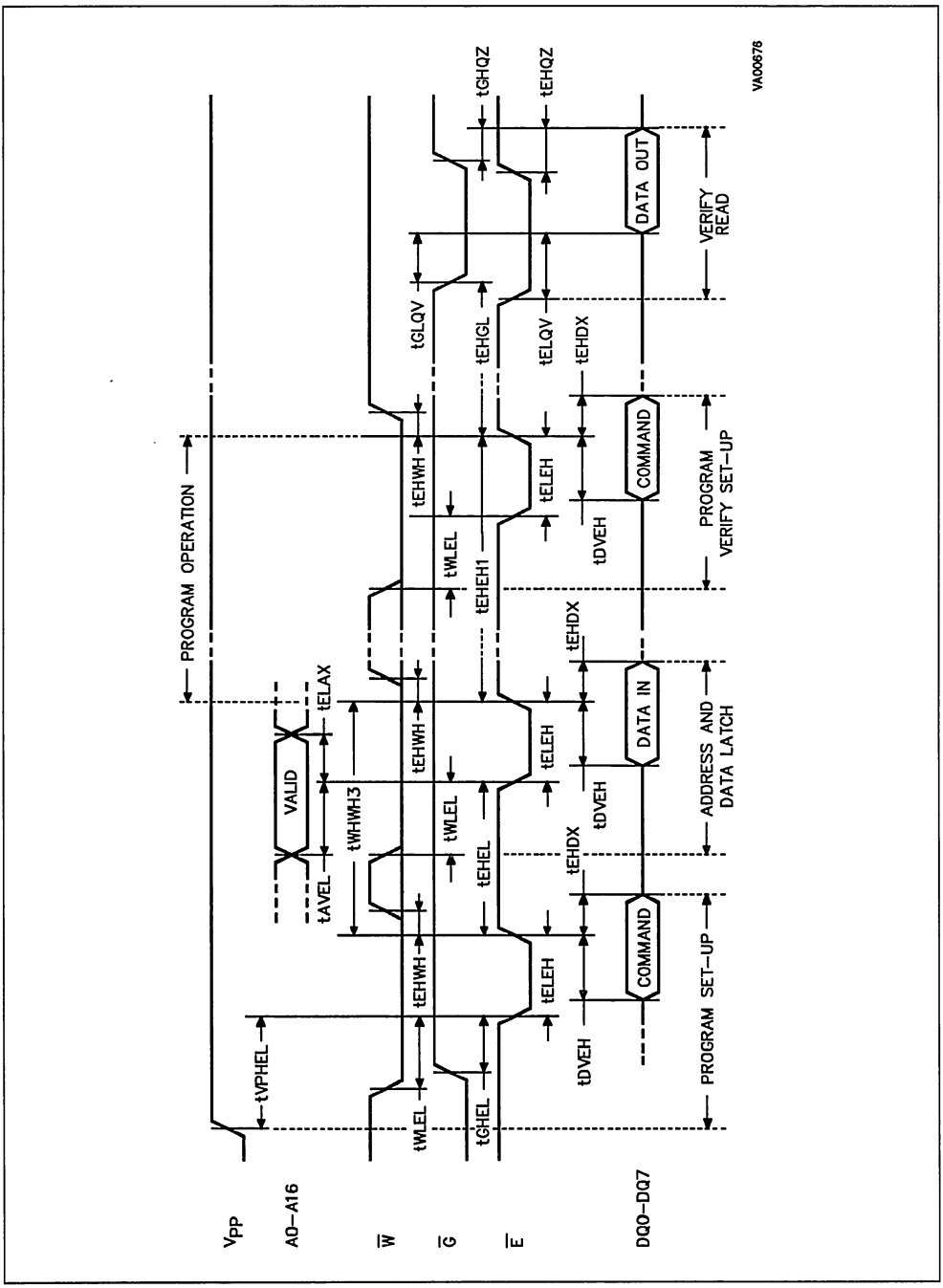


Figure 11. Erasing Flowchart

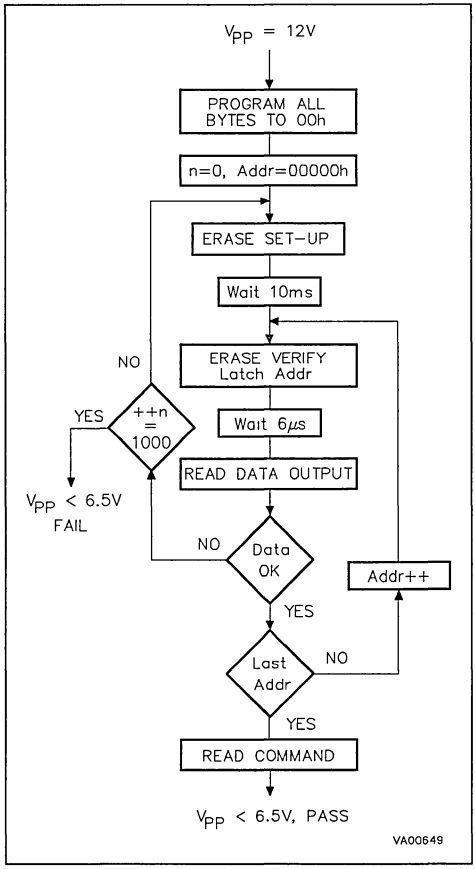
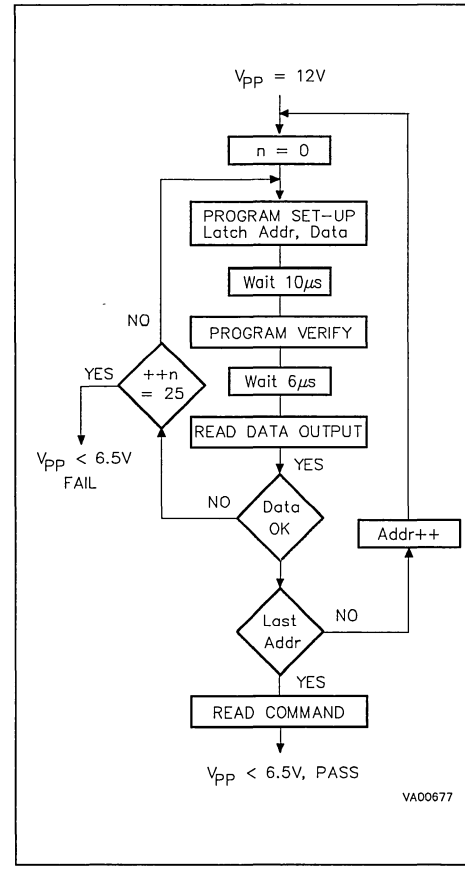


Figure 12. Programming Flowchart



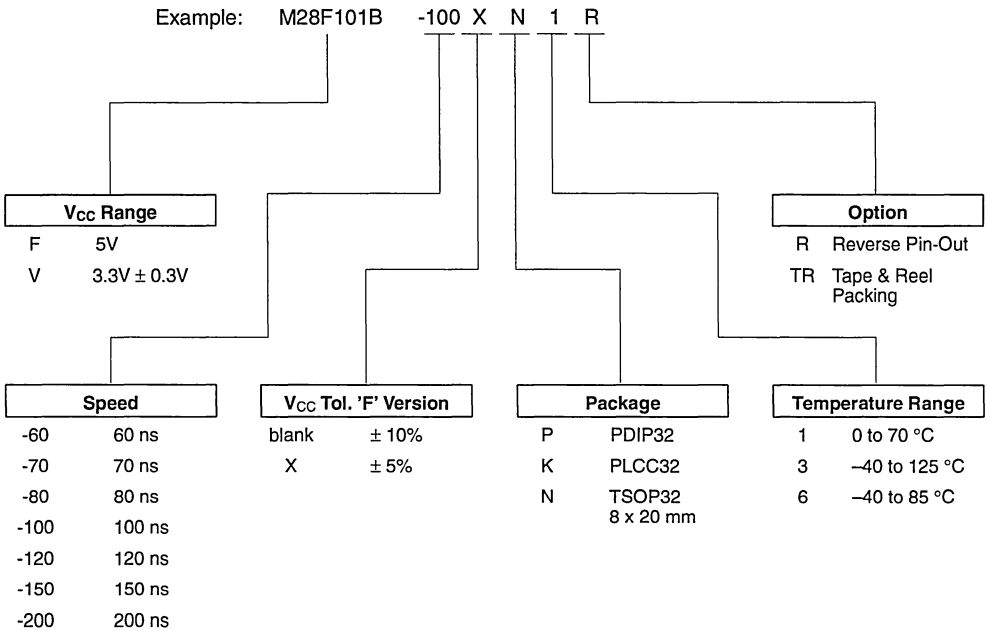
PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME



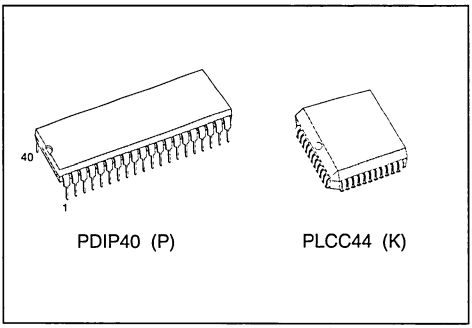
For a list of available options (V_{CC} Range, Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 1 Megabit (64K x 16, Chip Erase) FLASH MEMORY

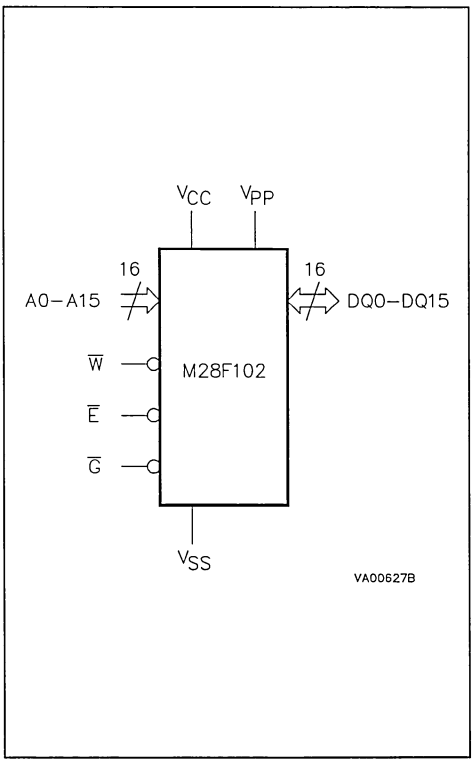
ADVANCE DATA

- FAST ACCESS TIME: 100ns
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE in 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



PDIP40 (P) PLCC44 (K)

Figure 1. Logic Diagram



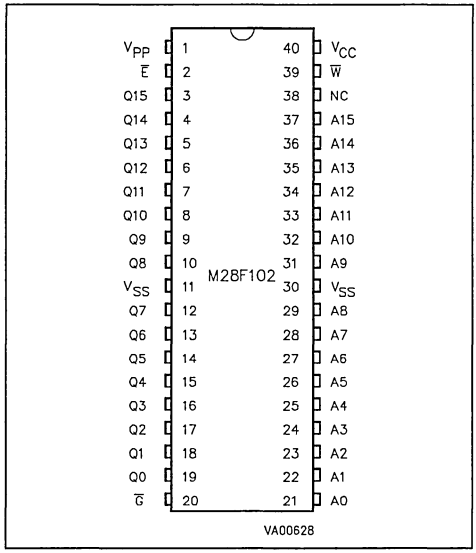
DESCRIPTION

The M28F102 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed word-by-word. It is organised as 64K words of 16 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F102 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

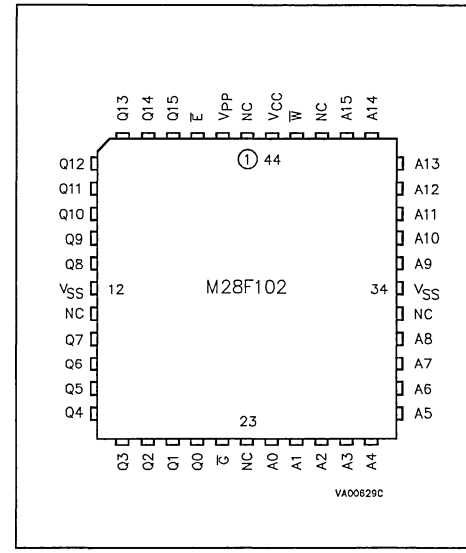
A0 - A15	Address Inputs
DQ0 - DQ15	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F102 FLASH MEMORY employs a technology similar to a 1 Megabit EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F102 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command regsiter is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

Read Mode. The M28F102 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 50mA to 100µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when V_{PP} is $\leq$ 6.5V the contents of the command register default to 0000h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 0000h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ15
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ15-DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	0	1	0	0	0	0	0	0020h
Device Code	V_{IH}	0	0	1	0	1	0	0	0	0	0050h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A15	DQ0-DQ15	Operation	A0-A15	DQ0-DQ15
Read	1	Write	X	0000h			
Electronic Signature	2	Write	X	0090h	Read	0000h	0020h
					Read	0001h	0050h
Setup Erase/ Erase	2	Write	X	0020h			
					Write	X	0020h
Erase Verify	2	Write	A0-A15	00A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	0040h			
					Write	A0-A15	Data Input
Program Verify	2	Write	X	00C0h	Read	X	Data Output
Reset	2	Write	X	0FFFFh	Write	X	0FFFFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 0000h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 0090h to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 0000h, the Erase command then erases them to 0FFFFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFFFh.

The Erase Mode is set-up by writing 0020h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is

READ/WRITE MODES (cont'd)

followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 00A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFFFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 00A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFFFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 00C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFFFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

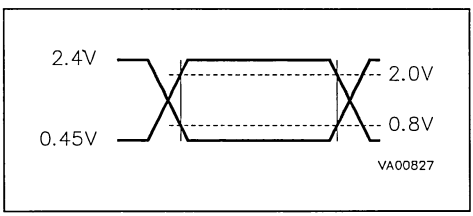


Figure 4. AC Testing Load Circuit

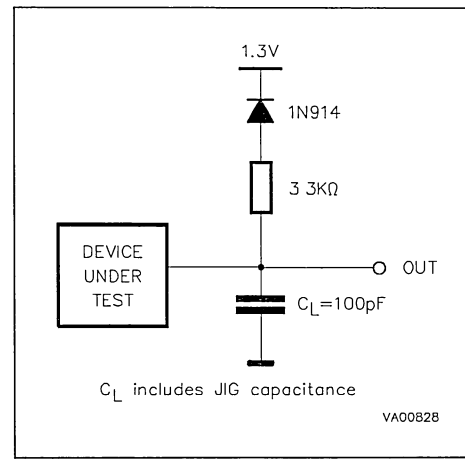


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 5MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±10	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±10	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		50	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		50	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grade 6)		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4		V
		I_{OH} = –2.5mA	0.85 V_{CC}		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID}		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% tested. Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F102				Unit
				-100		-120		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics
(((T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F102				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	45	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

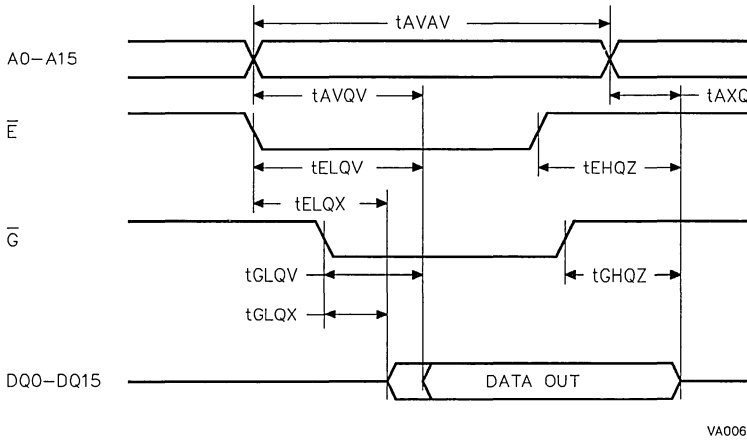


Figure 6. Read Command Waveforms

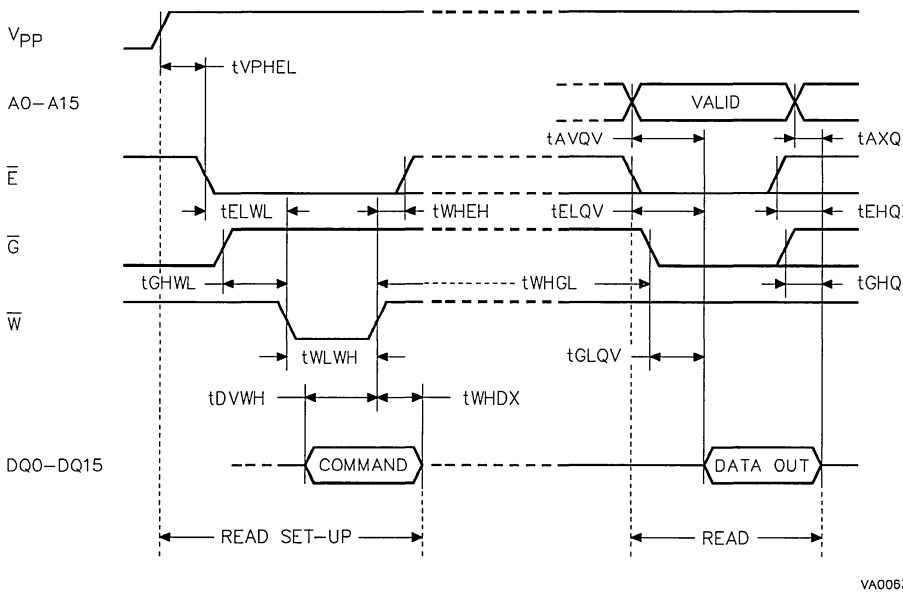


Figure 7. Electronic Signature Command Waveforms

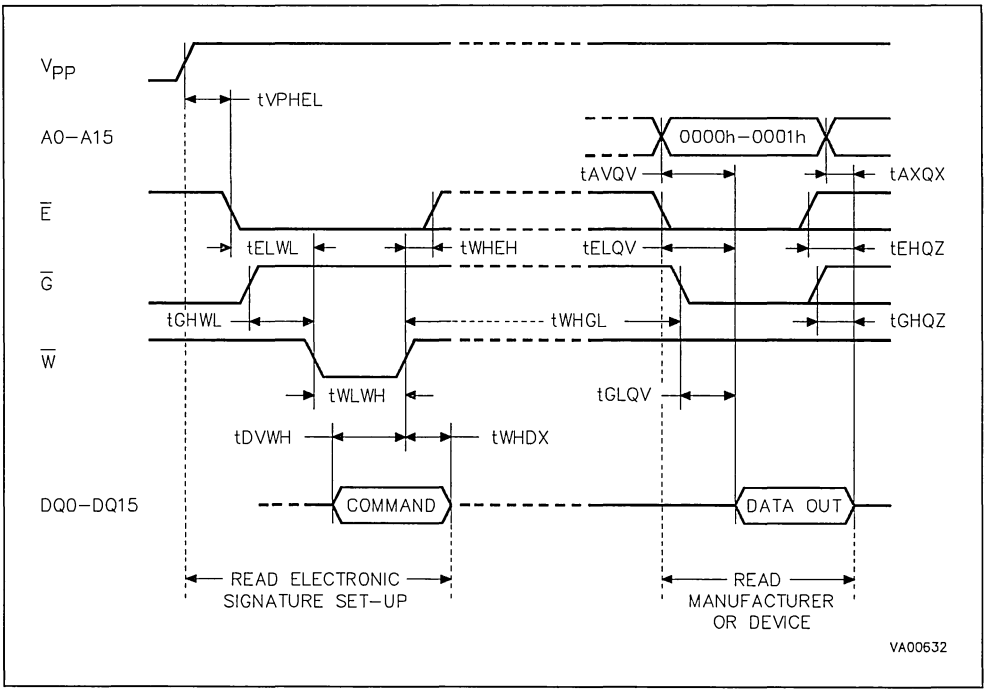


Table 9A. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	M28F102				Unit
			-100		-120		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		60		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		40		40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested

Table 9B. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	M28F102				Unit
			-150		-200		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		80		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		45	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

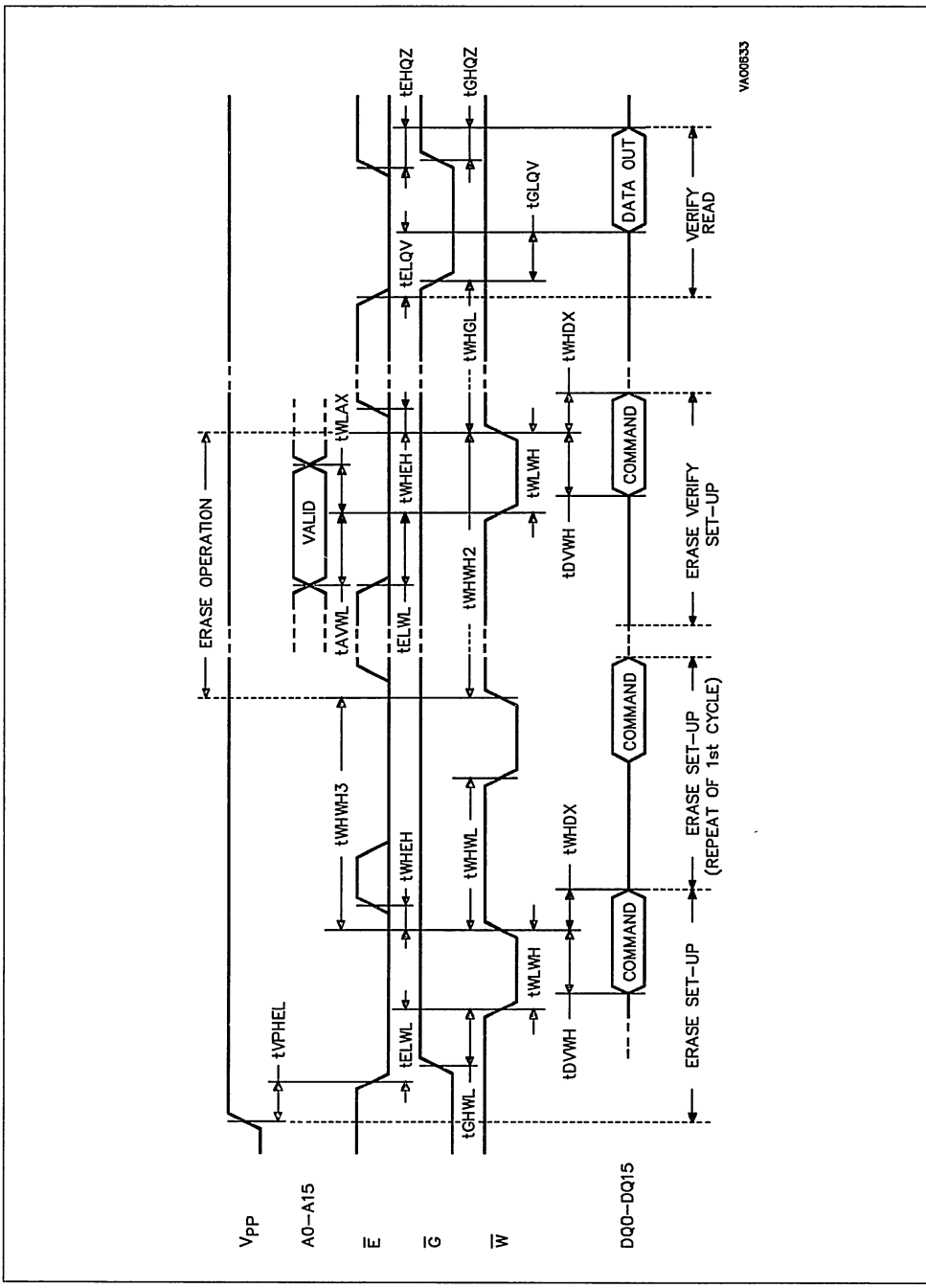


Figure 9. Program Set-up and Program Verify Commands Waveforms - $\overline{W}$ Controlled

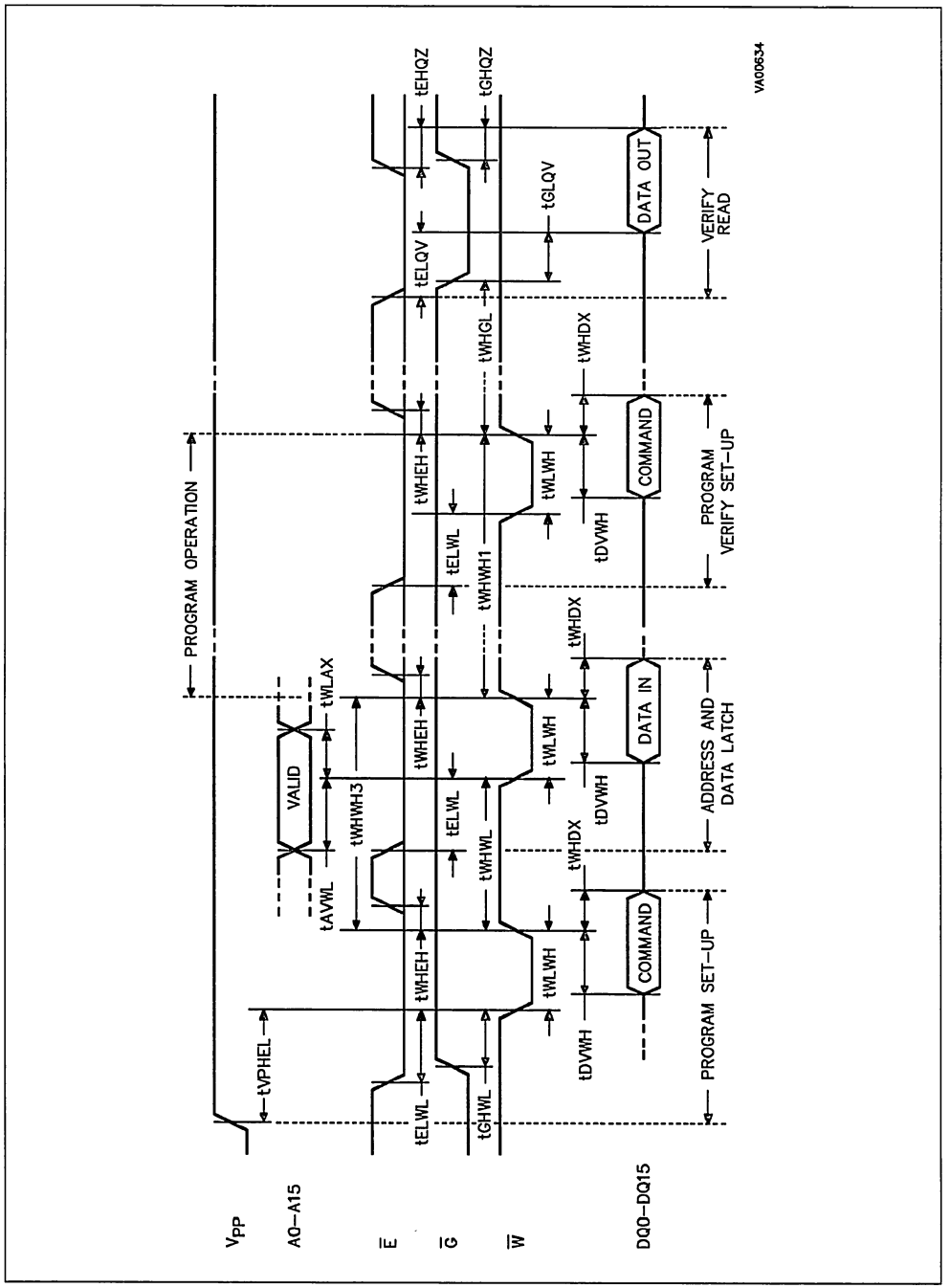


Figure 10. Program Set-up and Program Verify Commands Waveforms - $\overline{E}$ Controlled

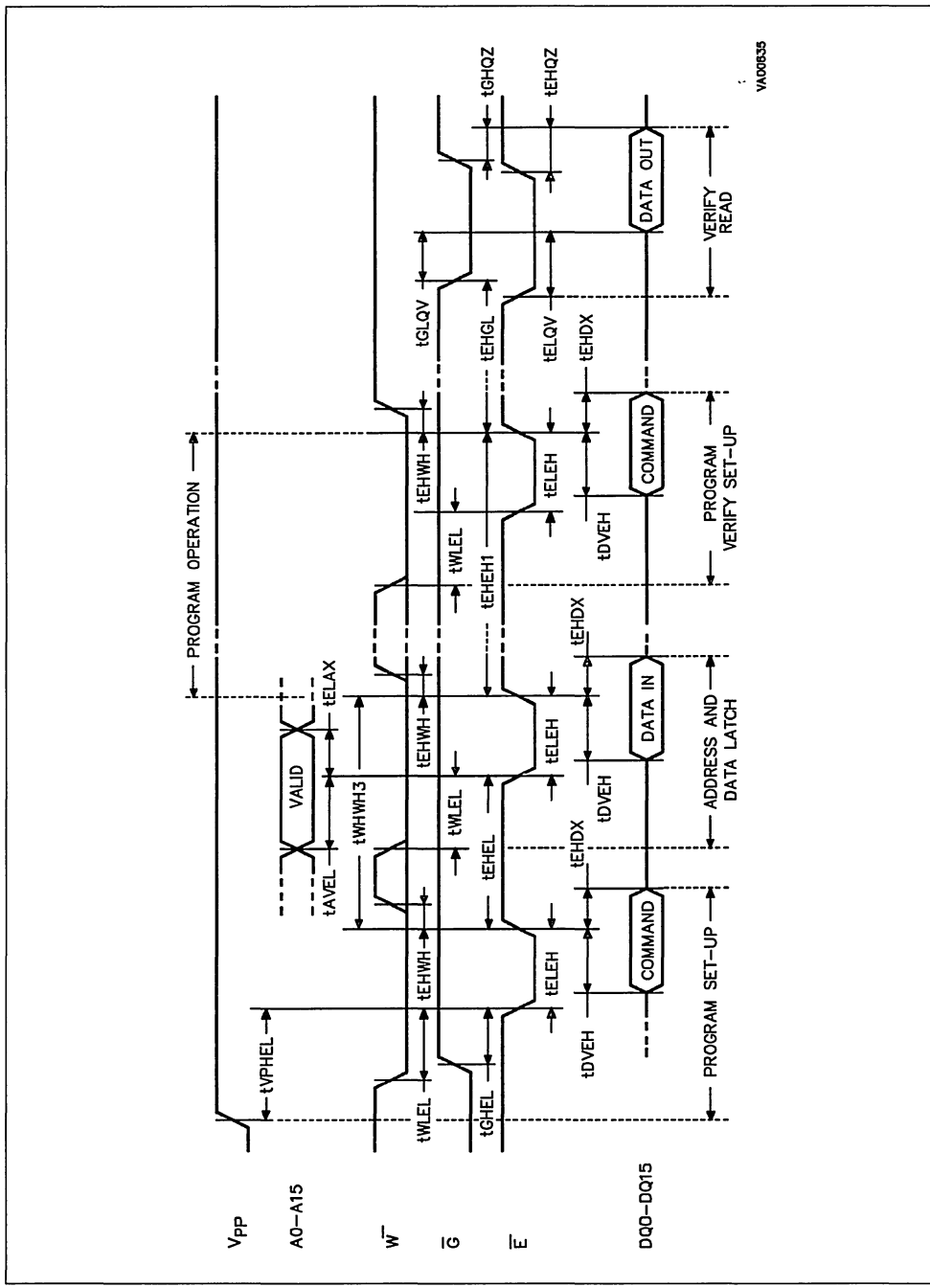


Figure 11. Erasing Flowchart

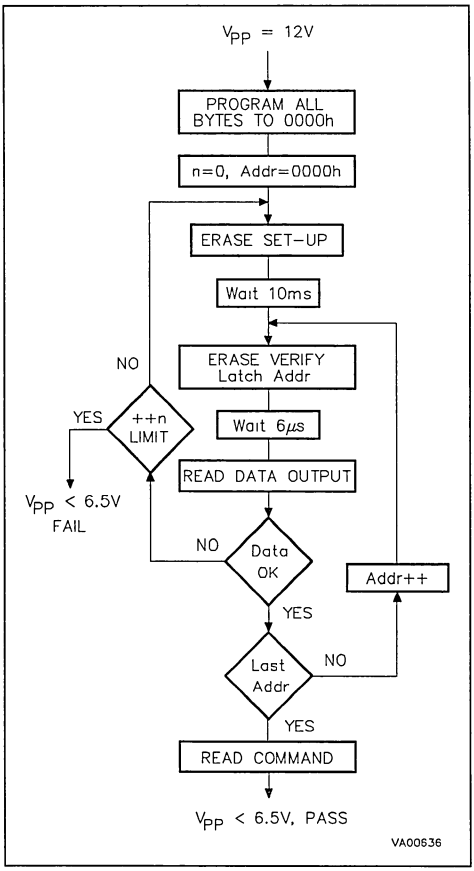
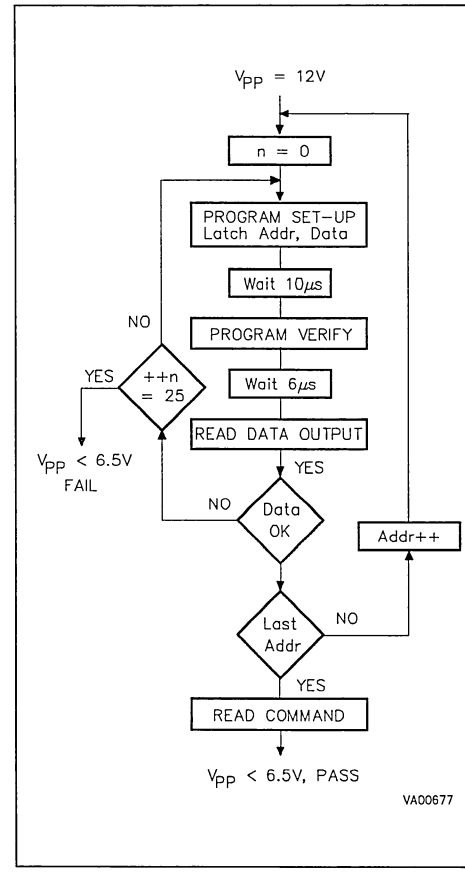


Figure 12. Programming Flowchart



Limit: 1000 at grade 1; 6000 at grades 3 & 6.

PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all words to 0000h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 0020h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 00A0h to the command register together with the address of the word to be verified. The subsequent read cycle reads the data which is compared to 0FFFFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFFFh fails. If this occurs, the address of the last word checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a word until a correct verify occurs. Up to 25 programming operations are allowed for one word. Program is set-up by writing 0040h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 00C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME

Example: M28F102 -100 X P 1 TR

Speed		V_{CC} Tolerance		Package		Temp. Range		Option	
-100	100 ns	blank	± 10%	P	PDIP40	1	0 to 70 °C	Y3	1,000 Cycles
-120	120 ns	X	± 5%	K	PLCC44	3	–40 to 125 °C	TR	Tape & Reel Packing
-150	150 ns					6	–40 to 85 °C		
-200	200 ns								

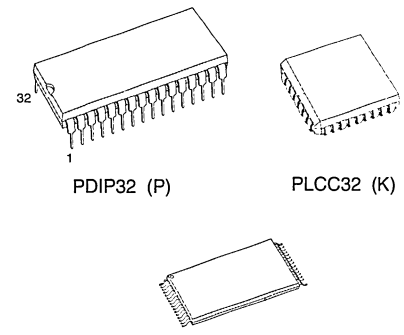
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 2 Megabit (256K x 8, Chip Erase) FLASH MEMORY

ADVANCE DATA

- FAST ACCESS TIMES
  - 60ns for M28F201 version
  - 150ns for M28V201 version
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 PROGRAM/ERASE CYCLES
- 12V PROGRAMMING VOLTAGE
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M20F201 version
  - 3.3V ± 0.3V for M20V201 version
- TYPICAL BYTE PROGRAMMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE in 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



DESCRIPTION

The M28F201, M28V201 FLASH MEMORY products are non-volatile memories which may be erased electrically at the chip level and programmed byte-by-byte. They are organised as 256K bytes of 8 bits. They use a command register architecture to select the operating modes and thus provide a simple microprocessor interface. The M28F201, M28V201 FLASH MEMORY products are suitable for applications where the memory has to be reprogrammed in the equipment.

Table 1. Signal Names

A0 - A17	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

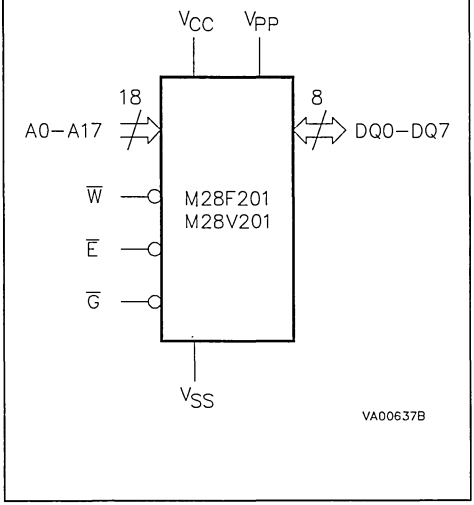


Figure 2A. DIP Pin Connections

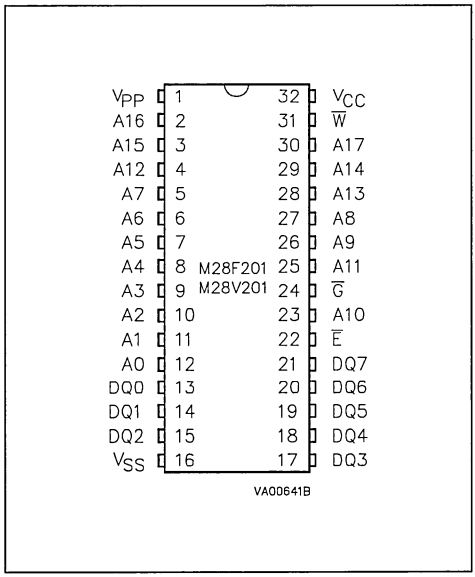


Figure 2B. LCC Pin Connections

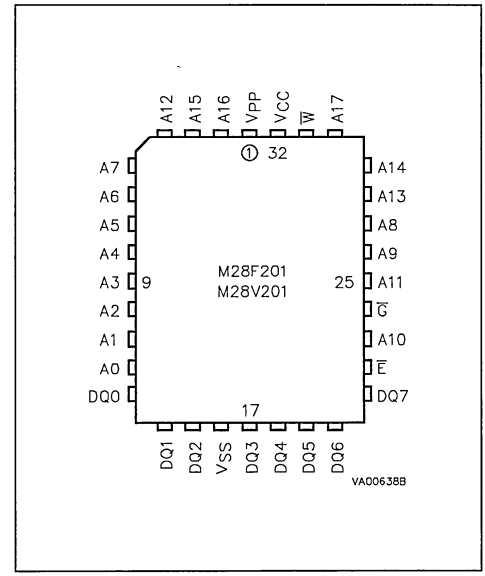


Figure 2C. TSOP Pin Connections

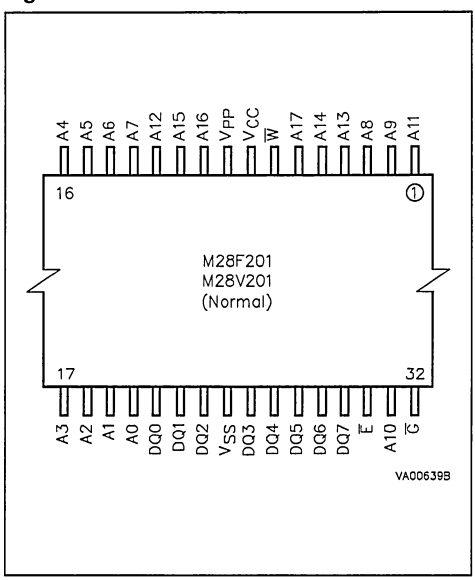


Figure 2D. TSOP Reverse Pin Connections

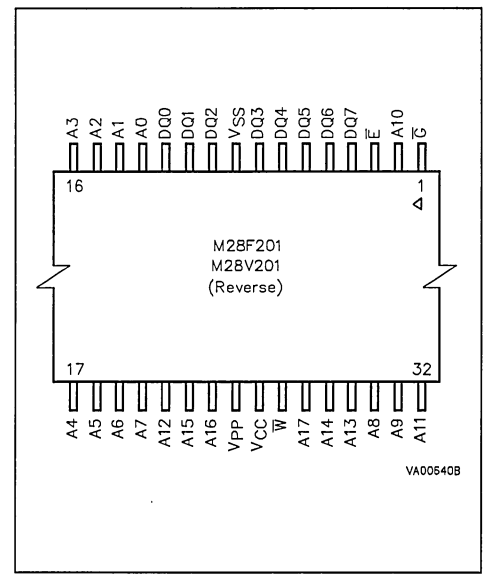


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

The access time of 60ns makes the device suitable for use in high speed microprocessor systems, while the low supply voltage capability makes it ideal for portable applications.

DEVICE OPERATION

The M28F201, M28V201 FLASH MEMORY products employ a technology similar to a 1 Megabit EPROM but add to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and the M28F201 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

Read Mode. The M28F201, M28V201 have two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 100µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code: M28F201	V_{IH}	1	1	1	1	0	1	0	0	0F4h
Device Code: M28V201	V_{IH}	1	1	1	1	0	1	0	1	0F5h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A17	DQ0-DQ7	Operation	A0-A17	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature (2)	2	Write	X	80h or 90h	Read	00000h	20h
					Read	00001h	0EEh or 0EFh
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A17	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A17	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Electronic Signature Table

READ/WRITE MODES (cont'd)

set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when V_{PP} is ≤ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

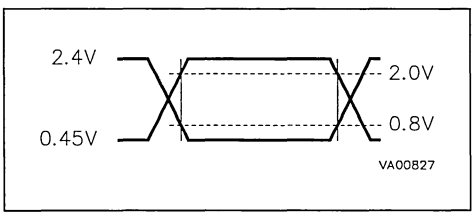


Figure 4. AC Testing Load Circuit

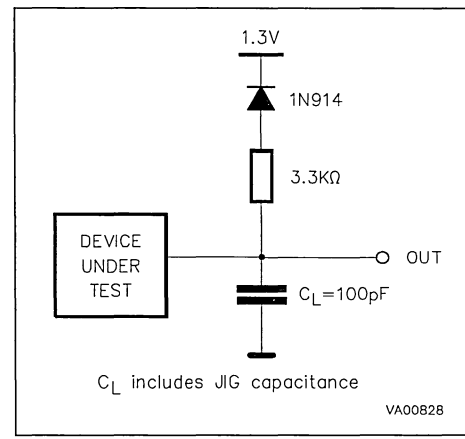


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 10MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		20	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		20	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify)		20	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±10	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±10	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.4		V
		I_{OH} = –2.5mA	0.85 V_{CC}		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	$A9 = V_{ID}$		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out	M28F201	2.2		V
		M28V201	2.0		V

Note: 1. Not 100% tested. Characterisation Data available.

Table 8. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F201		Unit
				-80		
				Min	Max	
t_{WHGL}		Write Enable High to Output Enable Low		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	80		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		80	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		80	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		ns

Note: 1. Sampled only, not 100% tested

READ/WRITE MODES (cont'd)

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 80h or 90h to the command register. The following read cycle, with address inputs 00000h or 00001h, output the manufacturer or device codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

Figure 5. Read Mode AC Waveforms

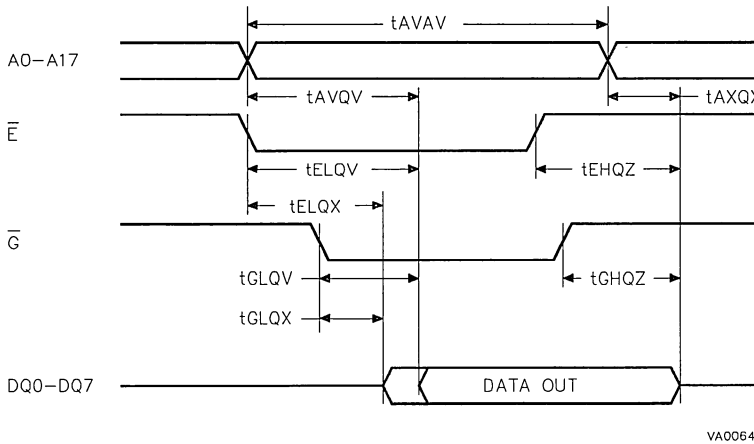


Figure 6. Read Command Waveforms

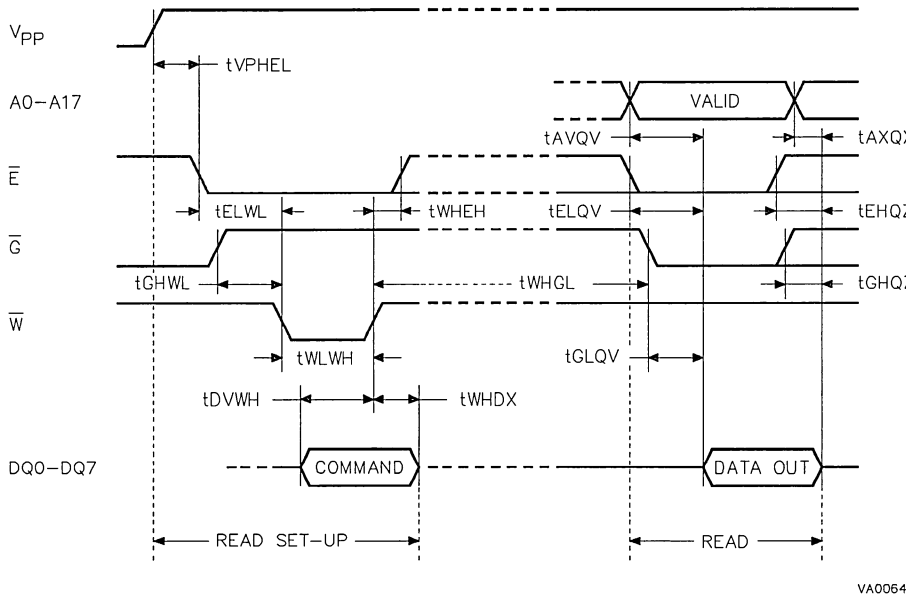
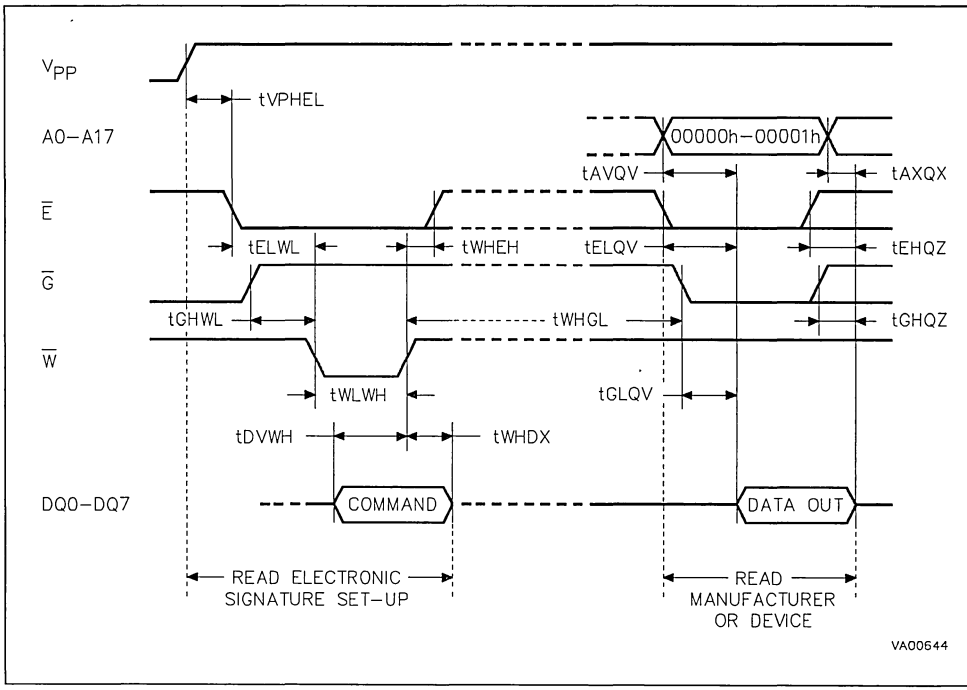


Figure 7. Electronic Signature Command Waveforms



READ/WRITE MODES (cont'd)

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this second cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

Table 9. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	M28F201		Unit
			-80		
			Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		µs
t_{AVAV}	t_{WC}	Write Cycle Time	80		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		ns
t_{ELAX}		Chip Enable Low to Address Transition	60		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	45		ns
t_{DVEH}		Input Valid to Chip Enable High	50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	45		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	60		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		ns
t_{EHDX}		Chip Enable High to Input Transition	0		ns
t_{WHWH1}		Duration of Program Operation	10		µs
t_{EHEH1}		Duration of Program Operation	10		µs
t_{WHWH2}		Duration of Erase Operation	9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		80	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		80	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		35	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		35	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		ns

Note: 1. Sampled only, not 100% tested

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

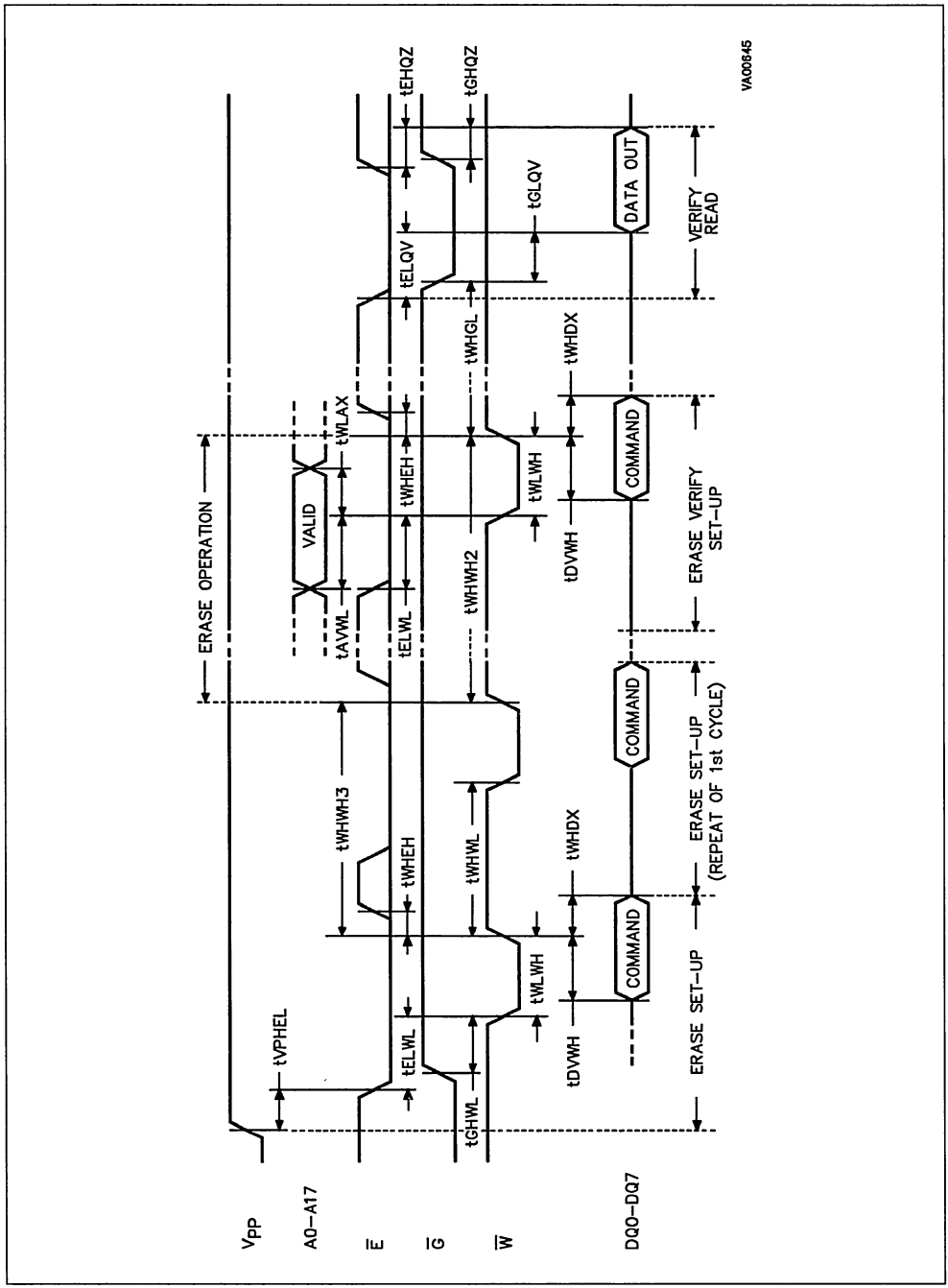


Figure 9. Program Set-up and Program Verify Commands Waveforms - $\overline{W}$ Controlled

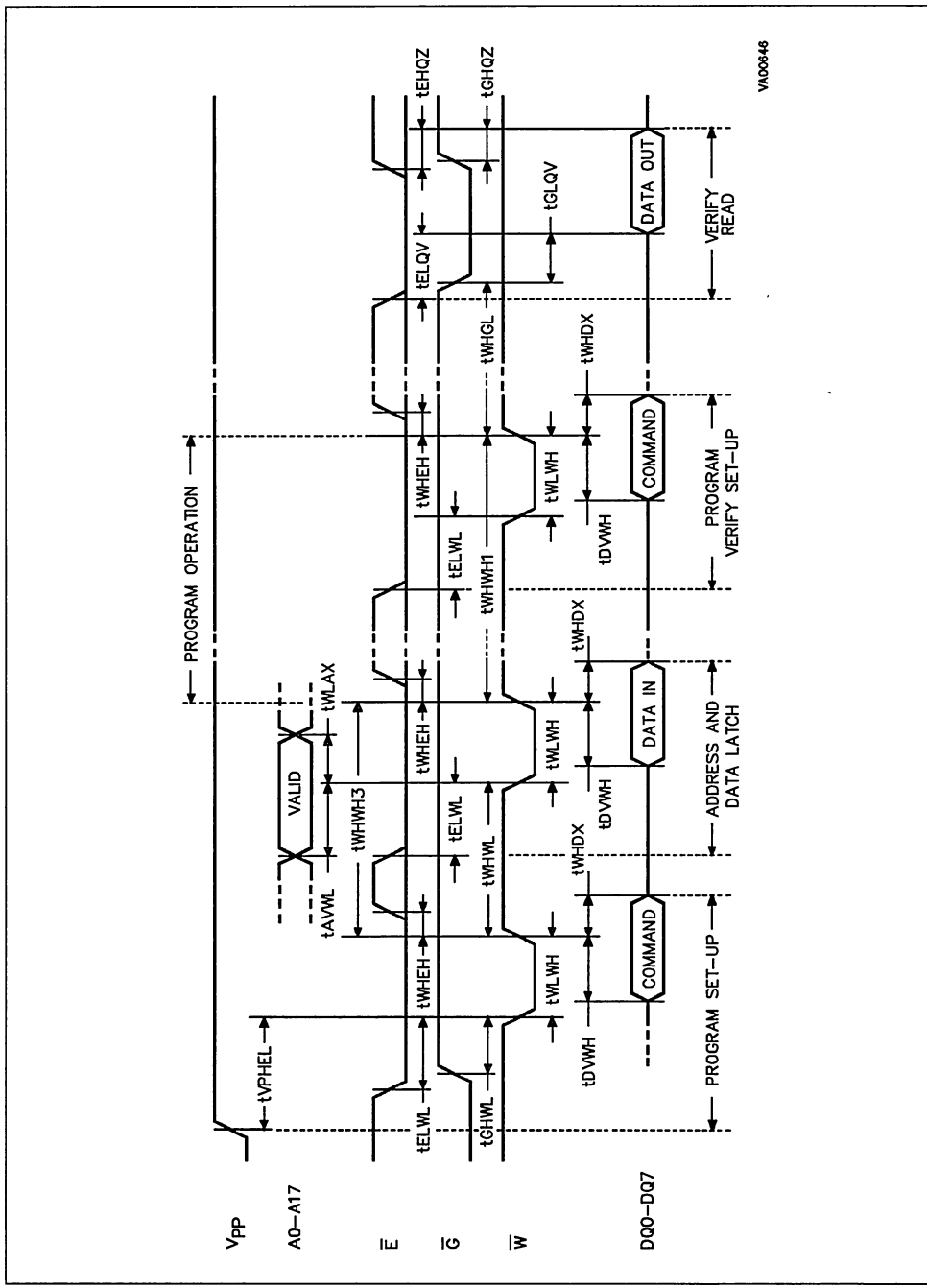


Figure 10. Program Set-up and Program Verify Commands Waveforms - $\overline{E}$ Controlled

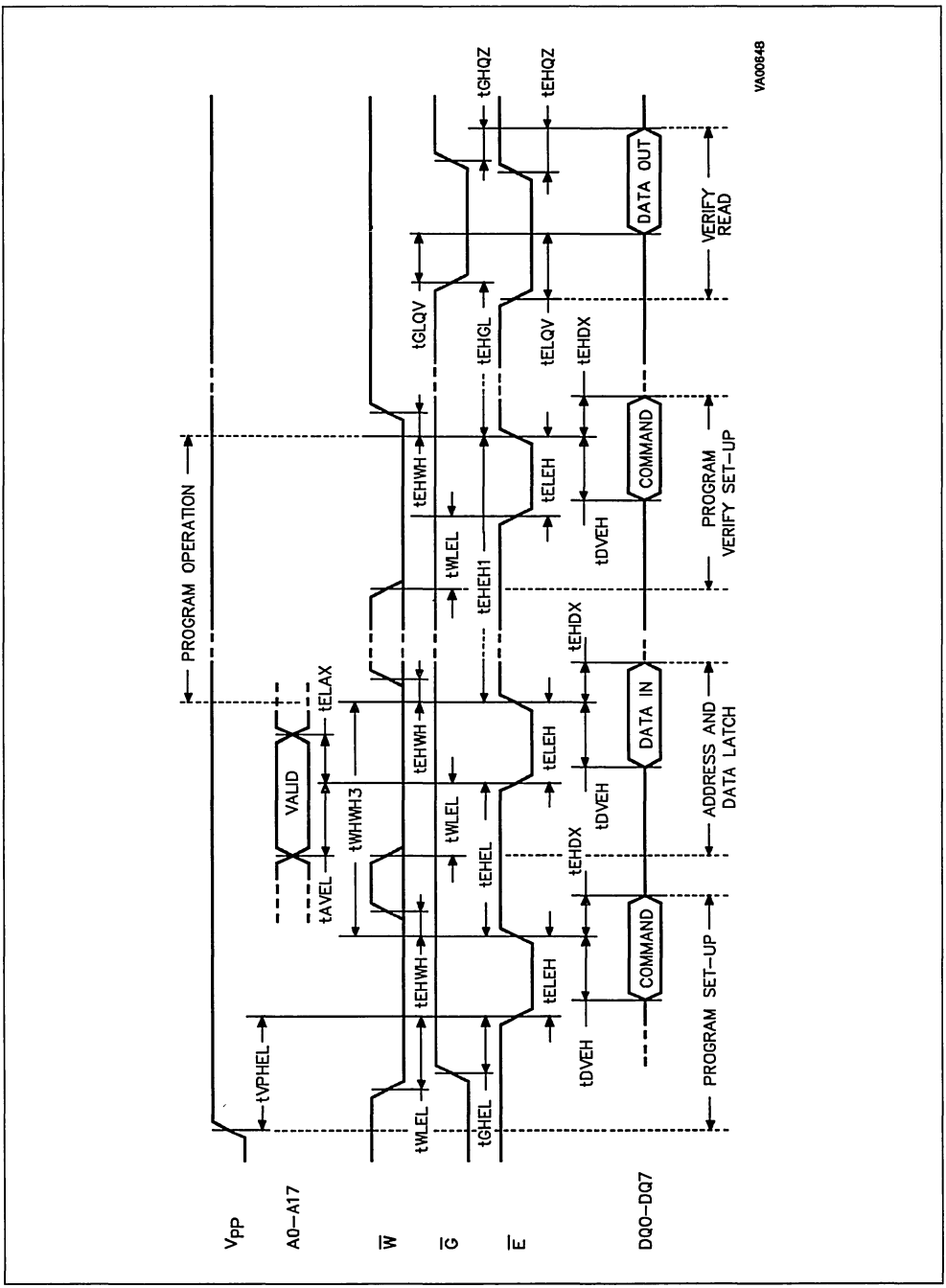


Figure 11. Erasing Flowchart

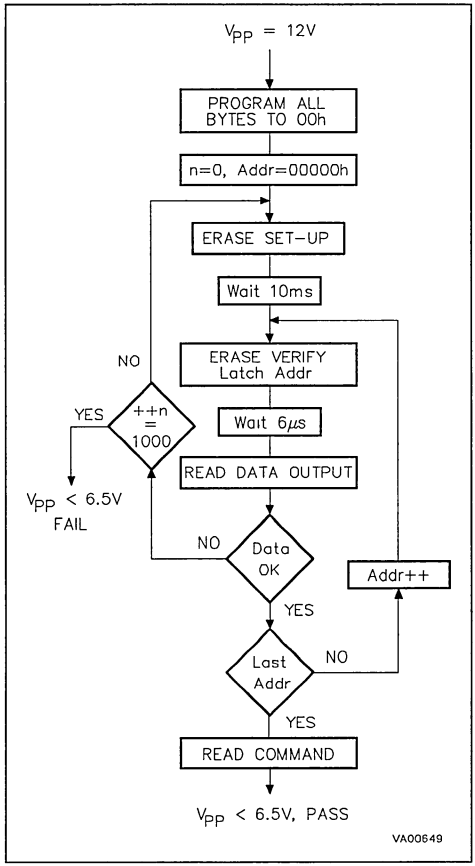
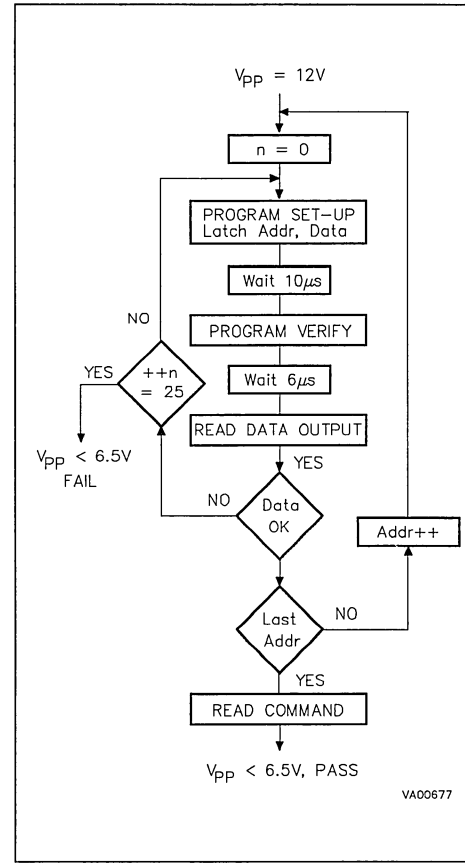


Figure 12. Programming Flowchart



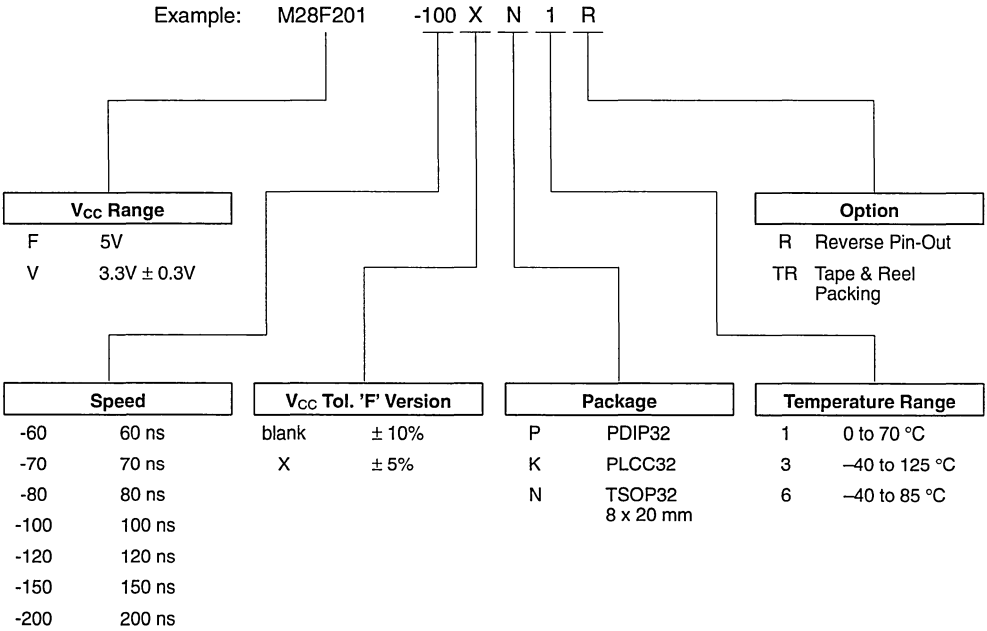
PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME



For a list of available options (V_{CC} Range, Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

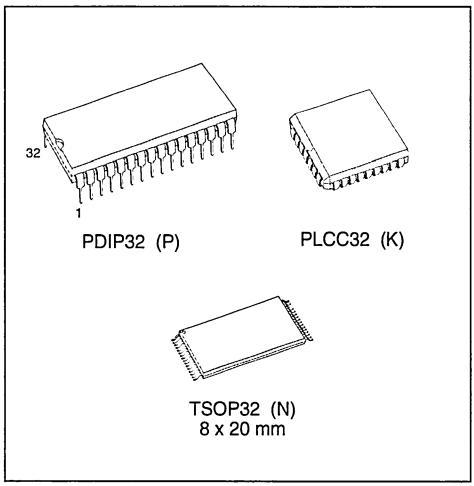
SGS-THOMSON MICROELECTRONICS

M28F201A
M28V201A

CMOS 2 Megabit (256K x 8, Chip Erase) FLASH MEMORY

PRODUCT CONCEPT

- MEMORY CHIP ERASE
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F201A version
  - 3.3V ± 0.3V for M28V201A version
- 12V PROGRAMMING VOLTAGE
- PROGRAM/ERASE CYCLES
  - 100,000 for M28F201A
  - 10,000 for M28V201A
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Data Polling and Toggle Protocol for P/E. C. Status
- LOW POWER CONSUMPTION
  - 30µA Typical in Standby
- FAST ACCESS TIMES
  - 60ns for M28F201A version
  - 150ns for M28V201A version



DESCRIPTION

The M28F201A, M28V201A FLASH MEMORY products are non-volatile memories that may be erased electrically in bulk and programmed byte-by-byte. The interface is directly compatible with most microprocessors. The device is available in PDIP32, PLCC32 and TSOP32 (8 x 20mm). Both normal and reverse pin outs are available for the TSOP32 package.

Table 1. Signal Names

A0 - A17	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

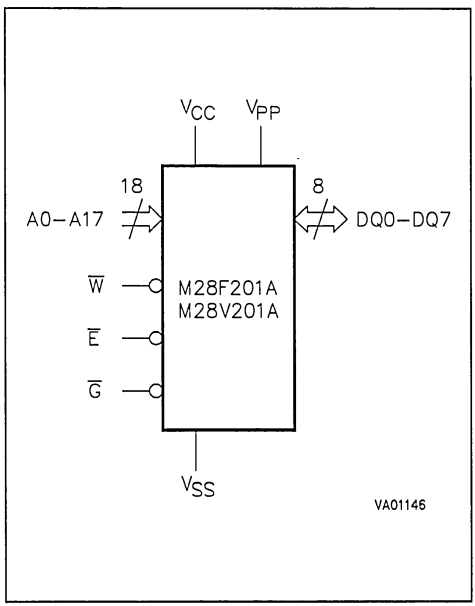


Figure 2A. DIP Pin Connections

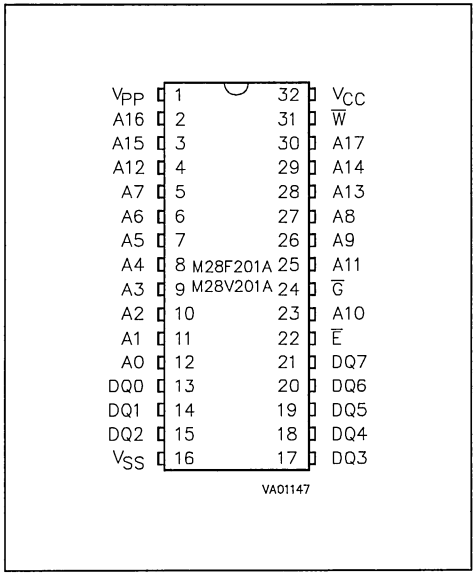


Figure 2B. LCC Pin Connections

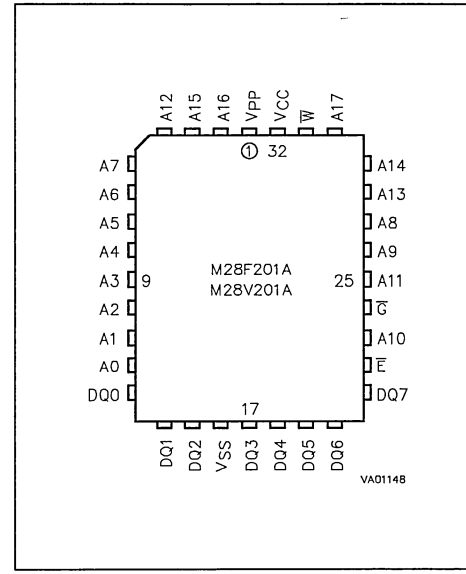


Figure 2C. TSOP Pin Connections

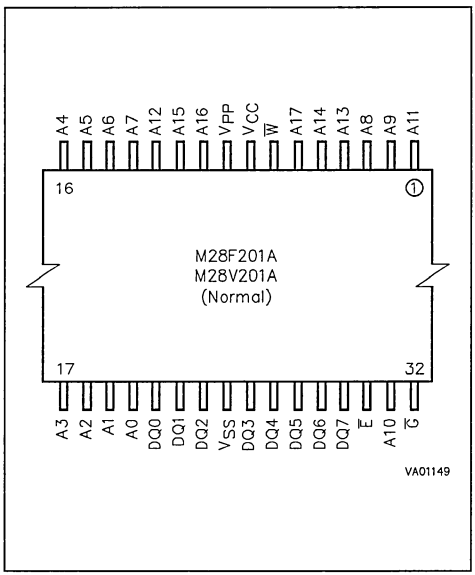
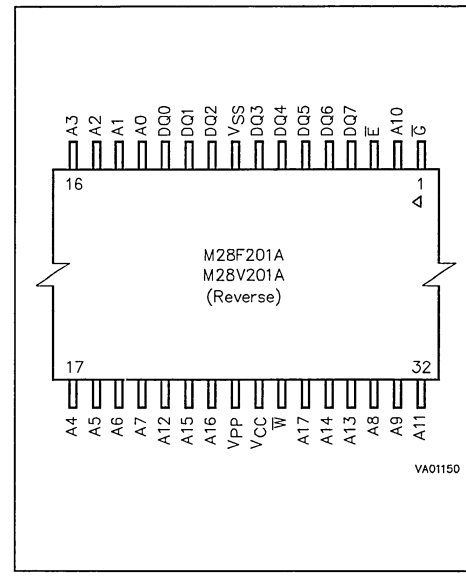


Figure 2D. TSOP Reverse Pin Connections



Organisation

The organisation is 256K x 8 with Address lines A0-A17 and Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs.

Erase and Program are performed under control of the internal Program/Erase Controller (P/E.C.).

Data Output bits DQ7 and DQ6 provide polling or toggle signals during Automatic Program or Erase to indicate the Busy/Ready state of the internal Program/Erase Controller.

Command Interface

The memory is interfaced by 5 operation cycles for reading the array, reading the Electronic Signature, output disable, standby or writing.

Command bytes can be written to a Command Interface latch to perform instructions for reading (array or Electronic Signature), erasure, programing or reset. When power is first applied, or if V_{CC} falls below V_{LKO}, the command interface is reset to read the array.

Instructions

Five instructions are defined to perform Read Memory Array, Read Electronic Signature, Auto Erase, Auto Program and Reset. Instructions are composed of a first command write operation followed by either a second command write, to confirm the commands for programing and erase, or read operations to read data from the memory or to read the Electronic Signature.

For added data protection, the intructions for byte program and erase consist of two commands that are written to the memory. These instructions can be aborted after the first command has been given using the Reset instruction. Byte programing takes typically 6µs. Erasure of the entire memory takes typically 2.4sec when performed by the internal Automatic P/E.C. algorithm.

During an Automatic Program or Erase operation reads to the memory return a byte of which two data bits, DQ7 and DQ6, reflect the Busy/Ready status of the P/E.C.

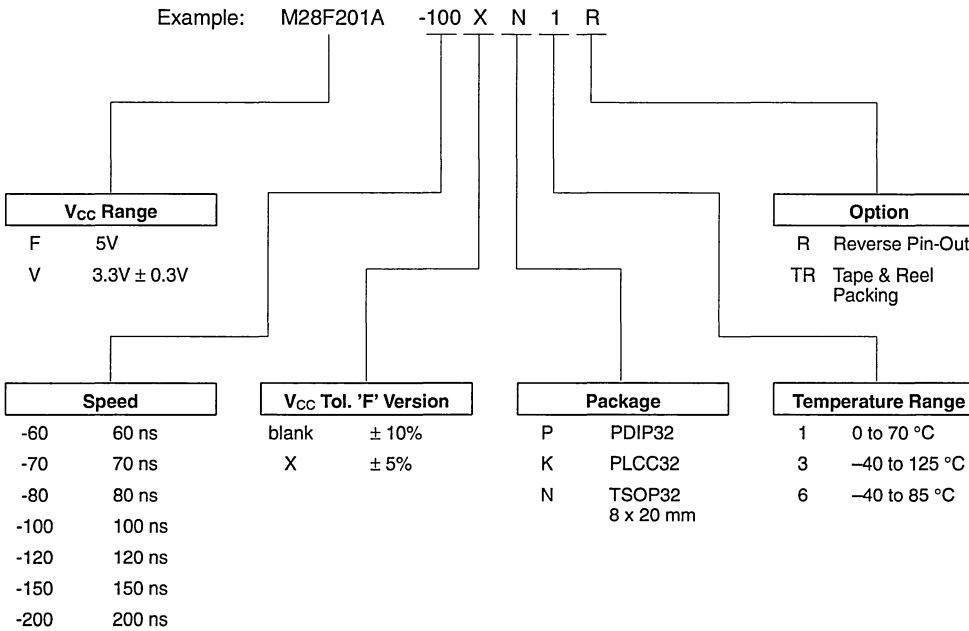
After a Program or Erase command the interface is reset to read the memory array.

Table 2. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address	Data Output
RD	Read Array	1+	Write	X	00h	Read	Address	Array Output
RSIG	Read Electronic Signature	1+	Write	X	80h or 90h	Read	A0 = '0' or '1'	Code Output
EE	Erase Auto	2	Write	X	30h	Write	X	30h
PG	Program Auto	2	Write	X	10h or 50h	Write	Address	Data Input
RST (2)	Reset	1-2	Write	X	0FFh	Write	X	0FFh

Notes: 1. X = Don't Care
2. 1 or 2 cycles may be required, see Instruction descriptions.

ORDERING INFORMATION SCHEME



For a list of available options (V_{CC} Range, Speed, V_{CC} Tolerance, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SGS-THOMSON MICROELECTRONICS

M28F410, F420
M28V410, V420

CMOS 4 Megabit (x8 or x16, 7 Block Erase) FLASH MEMORY

ADVANCE DATA

- SMALL SIZE TSOP56 and SO44 PLASTIC PACKAGES
  - Normal and Reverse Pinout for TSOP version
- DUAL x8 and x16 ORGANISATION
- MEMORY ERASE in BLOCKS
  - One 16K Boot Block (top or bottom location) with hardware write protection
  - Two 8K bytes Key Parameter Blocks
  - One 96K bytes Main Block
  - Three 128K bytes Main Blocks
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F410, F420 versions
  - 3V to 5.5V for M28V410, V420 versions
- PROGRAM/ERASE CYCLES
  - 100,000 for M28F410, F420 versions
  - 10,000 for M28V410, V420 versions
- PROGRAM/ERASE CONTROLLER
- LOW POWER CONSUMPTION
  - 80µA Typical in Standby for M28F410, F420
  - 50µA Typical in Standby for M28V410, V420
  - 0.2µA Typical in Deep Power Down for all versions
- FAST ACCESS TIMES
  - 60-80ns for M28F410, F420
  - 150-200ns for M28V410, V420

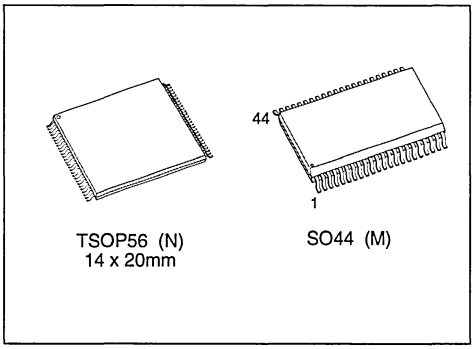


Table 1. Signal Names

A0-A17	Address Inputs
DQ0-DQ7	Data Input / Outputs
DQ8-DQ14	Data Input / Outputs
DQ15A-1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{BYTE}$	Byte/Word Organisation
$\overline{PWD}$	Power Down/Boot Block Lock
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

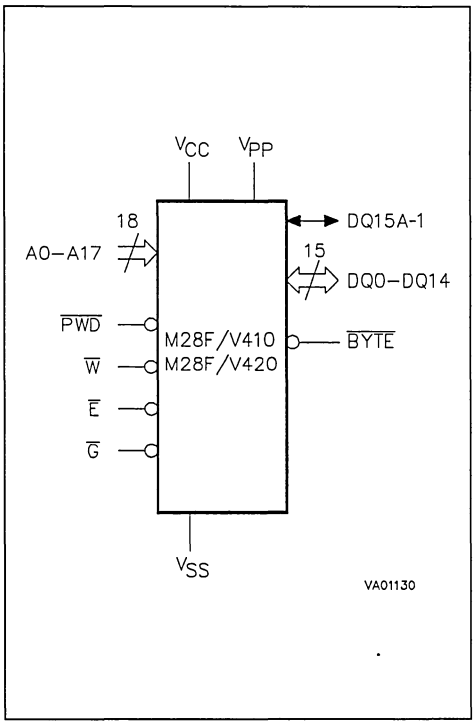
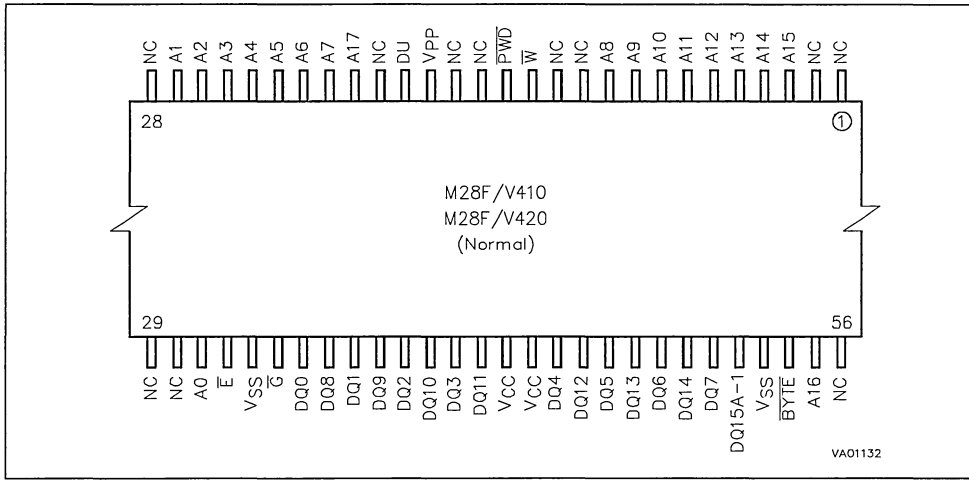
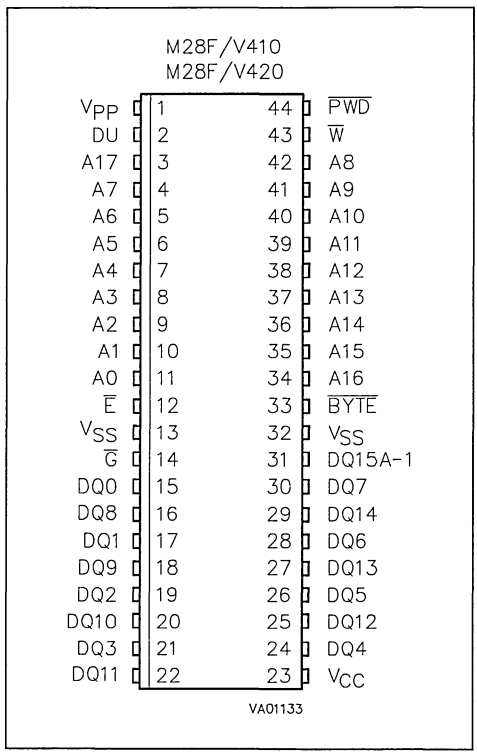


Figure 2A. TSOP Pin Connections



Warning: NC = No Connections, DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

DESCRIPTION

The M28F410, F420 and M28V410, V420 FLASH MEMORY products are non- volatile memories that may be erased electrically at the block level and programed by byte or word. The interface is directly compatible with most microprocessors. Plastic PTSO56 (Normal and Reverse pinout) and PSO44 packages are used.

Organisation

The organisation, as 512K x 8 or 256K x 16, is selectable by an external $\overline{BYTE}$ signal. When $\overline{BYTE}$ is Low and the x8 organisation is selected, the Data Input/Output signal DQ15 acts as Address line A-1 and selects the lower or upper byte of the memory word for output on DQ0-DQ7, DQ8-DQ15 remain high impedance. When $\overline{BYTE}$ is High the memory uses the Address inputs A0-A18 and the Data Input/Outputs DQ0-DQ15. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Power Down/Boot block unlock, tri-state, input places the memory in deep power down, normal operation or enables programing and erasure of the Boot block.

Blocks

Erasure of the memories is in blocks. There are 7 blocks in the memory address space, one 'Boot' block of 16K, two 'Key Parameter' blocks of 8K, one 'Main' block of 96K and three 'Main' blocks of 128K. The M28F410, V410 memories have the Boot block at the top of the memory address space and the M28F420, V420 locate the Boot block starting at the bottom. Erasure of each block takes typically

DESCRIPTION (cont'd)

1-2 seconds and each block may be programed and erased over 100,000 cycles (10,000 cycles for M28V410, V420). The Boot block is protected from accidental programing or erasure by a hardware protection depending on the Power Down $\overline{PWD}$ signal. Program/Erase commands in the Boot block are executed only when $\overline{PWD}$ is at 12V. Block erasure may be suspended while data is read from other blocks of the memory, then resumed.

Command Interface

Commands can be written to a Command Interface latch to perform read, programming, erasure and to monitor the memory's status. When power is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array. Five operations can be performed by the appropriate bus cycles, Read Byte or Word from the Array, Read Electronic Signature, Output Disable, Standby and Write a Command of an Instruction.

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte or word program and block erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation, byte or word programming takes typically 9µs, block erase typically 1- 2.4 seconds. Erasure of a memory block may be suspended in order to read data from another block and then resumed. A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation.

Power Saving

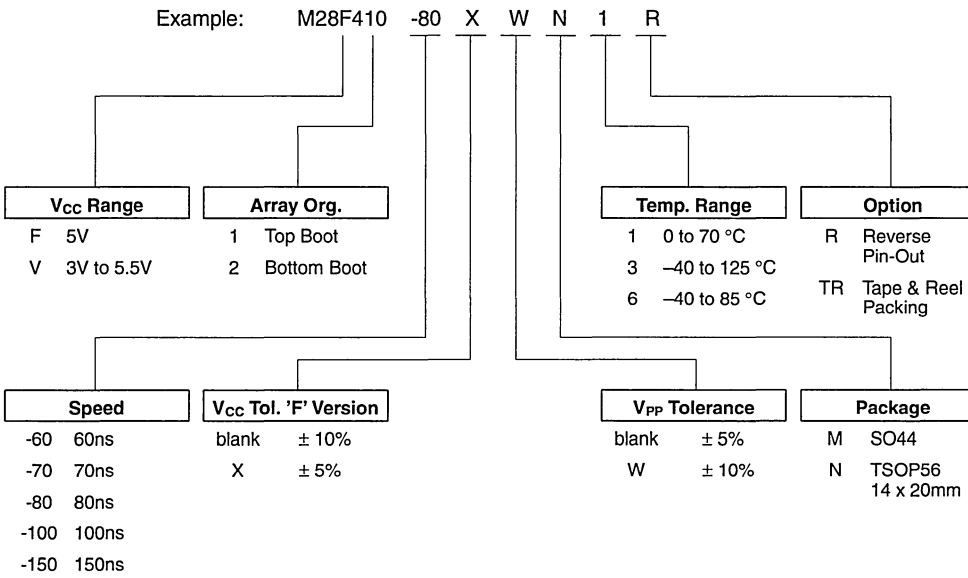
The M28F410, F420 and M28V410, V420 memories have a number of power saving features. Following a Read access the memory enters a static mode in which the supply current is typically 1.0mA (0.8mA for M28V410, V420). A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Power Down $\overline{PWD}$ signals are at V_{CC}, when the supply current drops to typically 45µA. A deep power down mode is enabled when the Power Down $\overline{PWD}$ signal is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 600ns maximum (700ns for M28V410, V420), with instructions to the C.I. recognised after only 480ns (1µs for M28V410, V420).

Table 2. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address	Data Output
RD	Read	1+	Write	X	0FFh	Note 2		
RSR	Read Status Register	1+	Write	X	70h	Note 2		
RSIG	Read Electronic Signature	3	Write	X	90h	Note 2		
EE	Erase	2	Write	X	20h	Write	Block Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care
2. The first cycle of the RD, RSR or RSIG instuction is followed by read operations to read the Array, Status Register or Electronic Signature code.

ORDERING INFORMATION SCHEME



For a list of available options (V_{CC} Range, Array Organisation, Speed, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

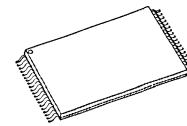
SGS-THOMSON MICROELECTRONICS

M28F411, F421
M28V411, V421

CMOS 4 Megabit (512K x 8, 7 Block Erase) FLASH MEMORY

ADVANCE DATA

- SMALL SIZE TSOP40 PLASTIC PACKAGE
  - Normal and Reverse Pinout
- MEMORY ERASE in BLOCKS
  - One 16K Boot Block (top or bottom location) with hardware write protection
  - Two 8K Key Parameter Blocks
  - One 96K Main Block
  - Three 128K Main Blocks
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F411, F421 versions
  - 3V to 5.5V for M28V411, V421 versions
- PROGRAM/ERASE CYCLES
  - 100,000 for M28F411, F421 versions
  - 10,000 for M28V411, V421 versions
- PROGRAM/ERASE CONTROLLER
- LOW POWER CONSUMPTION
  - 80µA Typical in Standby for M28F411, F421
  - 50µA Typical in Standby for M28V411, V421
  - 0.2µA Typical in Deep Power Down for all versions
- FAST ACCESS TIMES
  - 60-80ns for M28F411, F421
  - 150-200ns for M28V411, V421



TSOP40 (N)
10 x 20mm

Figure 1. Logic Diagram

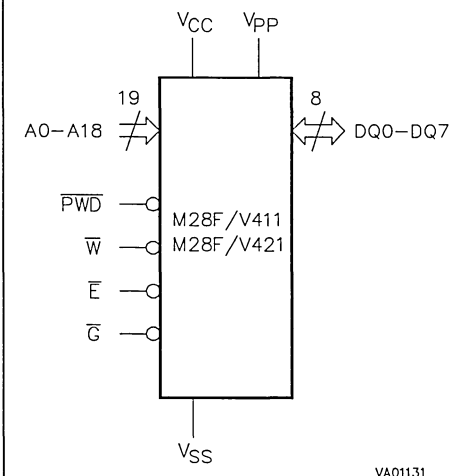
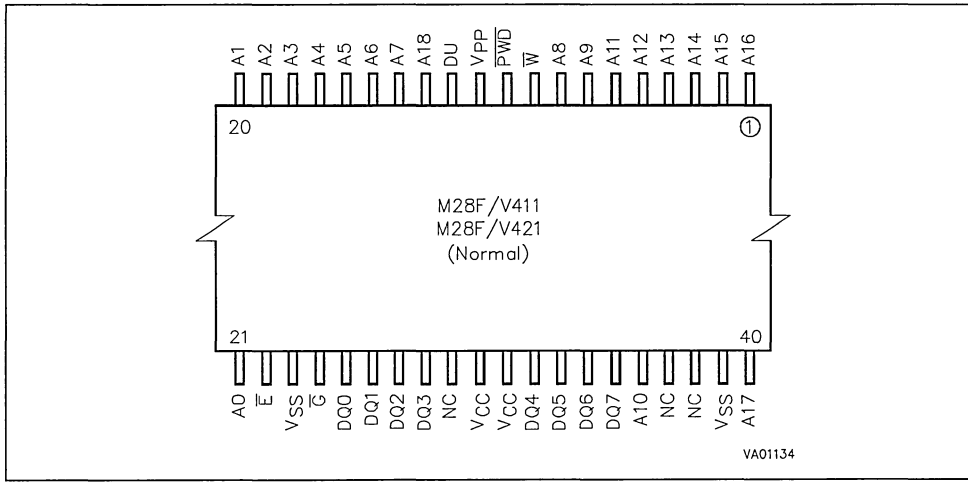


Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{PWD}$	Power Down/Boot Block Lock
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2. TSOP Pin Connections



Warning: NC = No Connection, DU = Don't Use

DESCRIPTION

The M28F411, F421 and M28V411, V421 FLASH MEMORY products are non- volatile memories that may be erased electrically at the block level and programed byte-by-byte. The interface is directly compatible with most microprocessors. Plastic TSOP40 (Normal and Reverse pinout) package is used.

Organisation

The organisation is 512K x 8 with Address lines A0-A18 and Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Power Down/Boot block unlock, tri-state, input places the memory in deep power down, normal operation or enables programing and erasure of the Boot block.

Blocks

Erasure of the memories is in blocks. There are 7 blocks in the memory address space, one 'Boot' block of 16K, two 'Key Parameter' blocks of 8K, one 'Main' block of 96K and three 'Main' blocks of 128K. The M28F411, V411 memories have the Boot block at the top of the memory address space and the M28F421, V421 locate the Boot block starting at the bottom. Erasure of each block takes typically 1-2 seconds and each block may be programed and erased over 100,000 cycles (10,000 for M28V411, V421). The Boot block is protected from accidental programing or erasure by a hardware protection depending on the $\overline{PWD}$ signal. Program/Erase commands in the Boot block are executed only when $\overline{PWD}$ is at 12V. Block erasure may be suspended while data is read from other blocks of the memory, then resumed.

Command Interface

Commands can be written to a Command Interface latch to perform read, programming, erasure and to monitor the memory's status. When power is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array. Five operations can be performed by the appropriate bus cycles, Read Byte from the Array, Read Electronic Signature, Output Disable, Standby and Write a Command of an Instruction.

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status.

Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the

DESCRIPTION (cont'd)

array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte program and block erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation, byte programming takes typically 9µs, block erase typically 1-2.4 seconds. Erasure of a memory block may be suspended in order to read data from another block and then resumed. A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation.

Power Saving

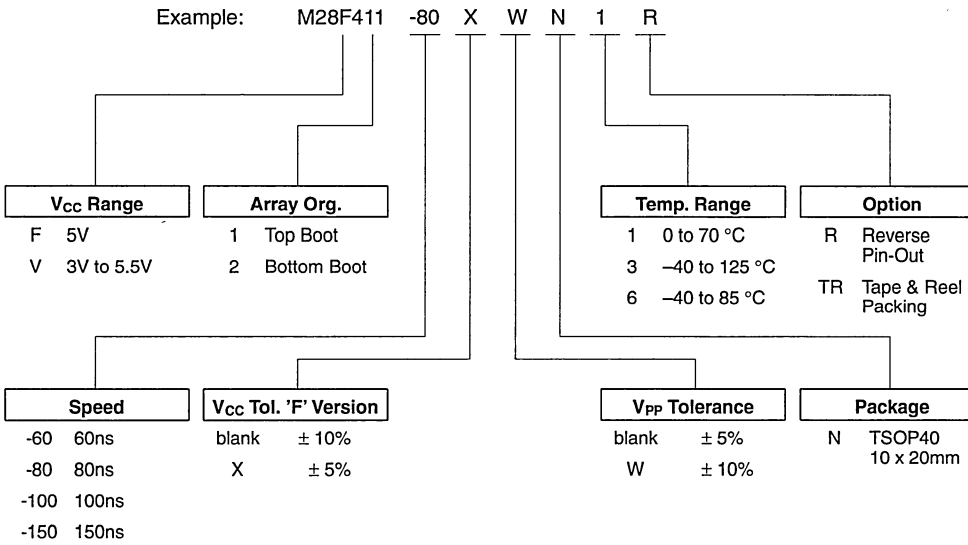
The M28F411, F421 and M28V411, V421 memories have a number of power saving features. Following a Read access the memory enters a static mode in which the supply current is typically 1.0mA (0.8mA for M28V411, V421). A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Power Down $\overline{PWD}$ signals are at V_{CC}, when the supply current drops to typically 45µA. A deep power down mode is enabled when the Power Down $\overline{PWD}$ signal is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 600ns maximum (700ns for M28V411, V421), with instructions to the C.I. recognised after only 480ns (1µs for M28V411, V421).

Table 2. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address	Data Output
RD	Read	1+	Write	X	0FFh	Note 2		
RSR	Read Status Register	1+	Write	X	70h	Note 2		
RSIG	Read Electronic Signature	3	Write	X	90h	Note 2		
EE	Erase	2	Write	X	20h	Write	Block Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care
2. The first cycle of the RD, RSR or RSIG instuction is followed by read operations to read the Array, Status Register or Electronic Signature code

ORDERING INFORMATION SCHEME



For a list of available options (V_{CC} Range, Array Organisation, Speed, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

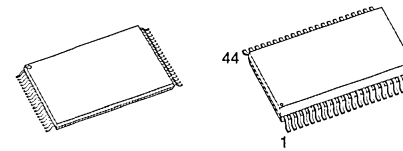
SGS-THOMSON MICROELECTRONICS

M28F841
M28V841

CMOS 8 Megabit (1Meg x 8, 16 x 64K Sector Erase) FLASH MEMORY

ADVANCE DATA

- SMALL SIZE TSOP40 and SO44 PLASTIC PACKAGES
  - Normal and Reverse Pinout for TSOP versions
- MEMORY ERASE in SECTORS, 16 x 64K
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F841 version
  - 3V to 5.5V for M28V841 version
- PROGRAM/ERASE CYCLES per SECTOR
  - 100,000 for M28F841 version
  - 10,000 for M28V841 version
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Erase by Sector, Erase Suspend/Resume
  - Ready/Busy Output
- LOW POWER CONSUMPTION
  - 30µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
- FAST ACCESS TIMES
  - 85-120ns for M28F841
  - 200ns for M28V841



TSOP40 (N)
10 x 20mm

SO44 (M)

Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{PWD}$	Power Down
$R\overline{B}$	Ready Busy Output
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

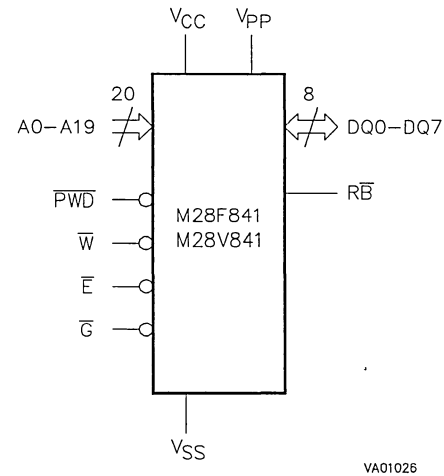
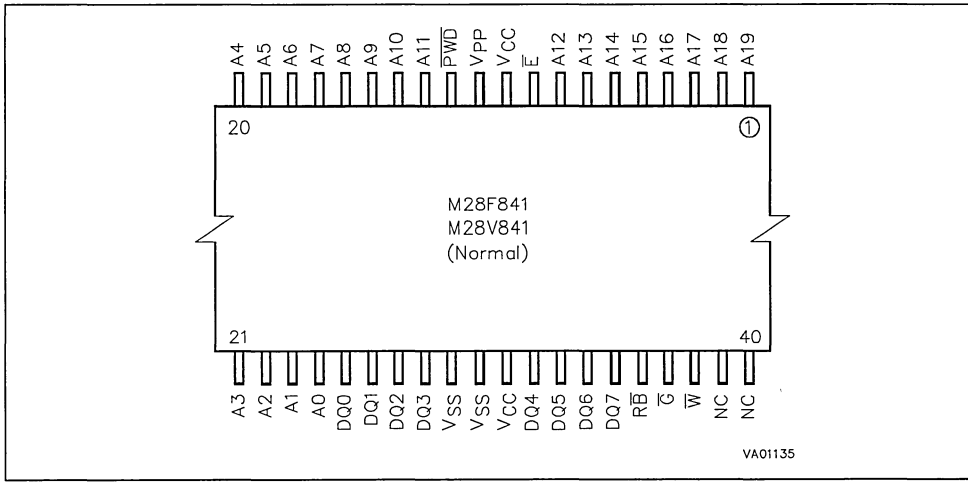
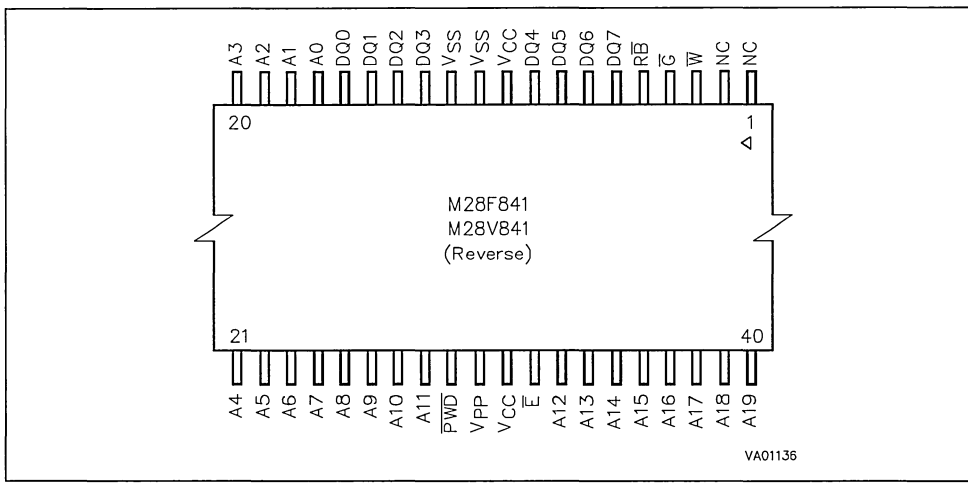


Figure 2A. TSOP Pin Connections



Warning: NC = No Connection

Figure 2B. TSOP Reverse Pin Connections



Warning: NC = No Connection

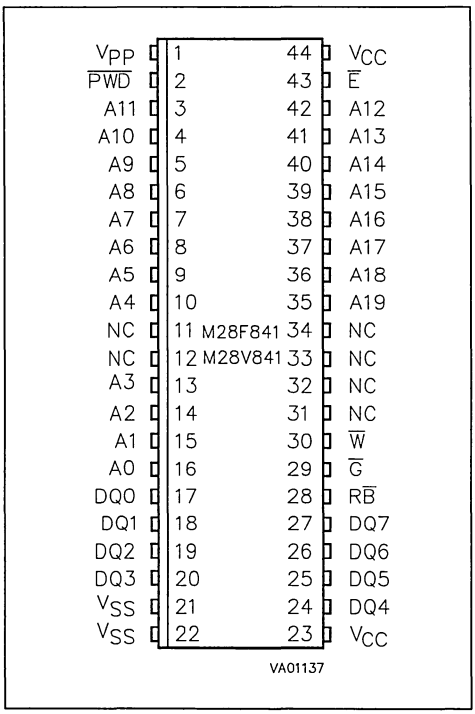
DESCRIPTION

The M28F841, M28V841 FLASH MEMORY products are non-volatile memories that may be erased electrically at the sector level and programed byte-by-byte. The interface is directly compatible with most microprocessors. They are intended for computer file systems applications. Plastic TSOP40 (Normal and Reverse pinout) and SO44 packages are used.

Organisation

The organisation is 1 Meg x 8 with Address lines A0-A19 and Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Power Down input places the memory in deep power down. A Ready/Busy output indicates the status of the internal Program/Erase Controller (P/E.C.).

Figure 2C. SO Pin Connections



Warning: NC = No Connection

Sectors

Erasure of the memories is in sectors. There are 16 sectors in the memory address space, each of 64K bytes. Programing of each sector takes typically 0.6 seconds and erasure 1.6 seconds, each sector may be programed and erased over 100,000 cycles (10,000 for M28V841). All sectors are protected from programming or erasure when the Power Down $\overline{PWD}$ signal is Low. Sector erase may be suspended while data is read from other sectors of the memory, then resumed.

Command Interface

Commands can be written to a Command Interface latch to perform read, programing, erasure and to monitor the memory's status. When power is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array. Four operations can be performed by the appropriate bus cycles, Read a Byte from the Array, Output Disable, Standby and Write a Command of an Instruction.

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the Array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte program and sector erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation. Byte programming takes typically 9µs, sector erase typically 1.6 seconds. Erasure of a memory sector may be suspended in order to read data from another sector and then resumed. A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation. In addition a Ready/Busy output indicates the status of the P/E.C. After Programing or Erasure the command interface must be reset by giving the Read Memory Array instruction before the memory contents can be accessed.

Power Saving

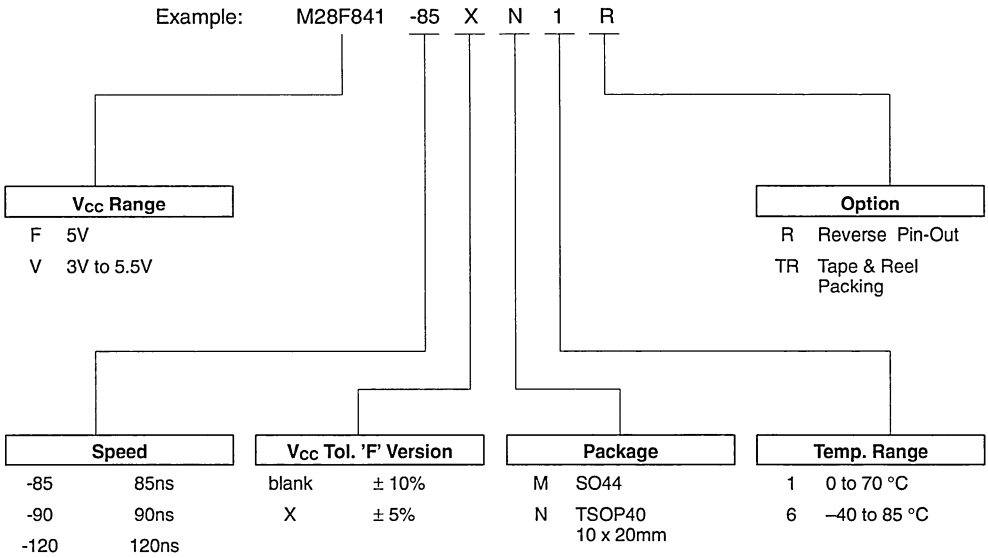
The M28F841, M28V841 memories have a number of power saving features. Following a Read access the memory enters a static mode in which the supply current is typically 1.0mA. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Power Down $\overline{PWD}$ signals are at V_{CC}, when the supply current drops to typically 30µA. A deep power down mode is enabled when the Power Down $\overline{PWD}$ signal is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 400ns maximum, with instructions to the C.I. recognised after 1µs.

Table 2. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address	Data Output
RD	Read	1+	Write	X	0FFh	Note 2		
RSR	Read Status Register	1+	Write	X	70h	Note 2		
RSIG	Read Electronic Signature	3	Write	X	90h	Note 2		
EE	Erase	2	Write	Sector Address	20h	Write	Sector Address	0D0h
PG	Program	2	Write	Byte Address	40h or 10h	Write	Byte Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care
2. The first cycle of the RD, RSR or RSIG instuction is followed by read operations to read the Array, Status Register or Electronic Signature code.

ORDERING INFORMATION SCHEME



For a list of available options (V_{CC} Range, Speed, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

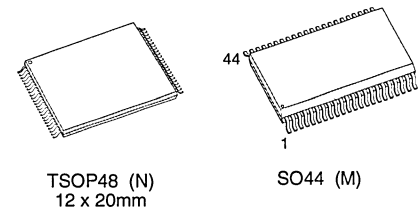
SGS-THOMSON MICROELECTRONICS

M28F161

CMOS 16 Megabit (2Meg x 8, 32 x 64K Sector Erase) FLASH MEMORY

PRODUCT CONCEPT

- SMALL SIZE TSOP48 and SO44 PLASTIC PACKAGES
  - Normal and Reverse Pinout for TSOP versions
- MEMORY ERASE in SECTORS, 32 x 64K
- SUPPLY VOLTAGE in READ OPERATION
  - 3.3V ± 0.3V
- 12V PROGRAMMING VOLTAGE
- 10,000 PROGRAM/ERASE CYCLES per SECTOR
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Erase by Sector, Erase Suspend/Resume
  - Ready/Busy Output
- LOW POWER CONSUMPTION
  - 30µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
- FAST ACCESS TIMES: 100ns Max



TSOP48 (N)
12 x 20mm

SO44 (M)

Figure 1. Logic Diagram

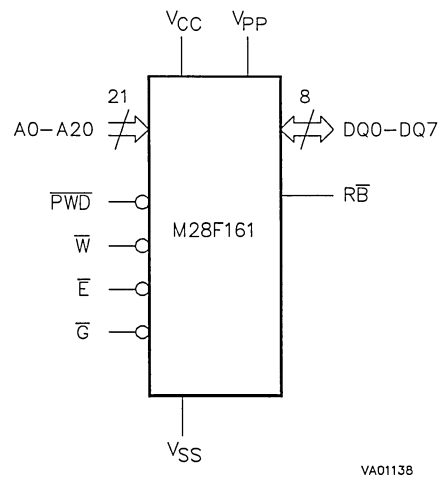
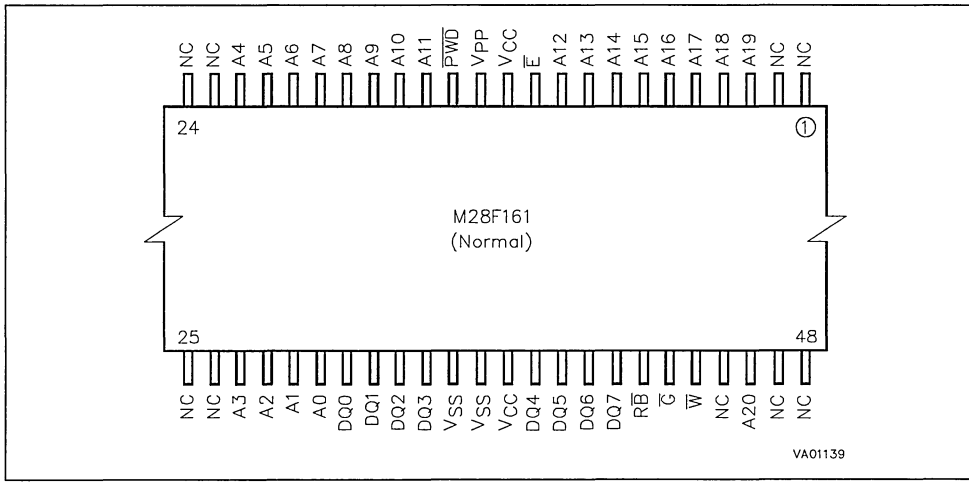


Table 1. Signal Names

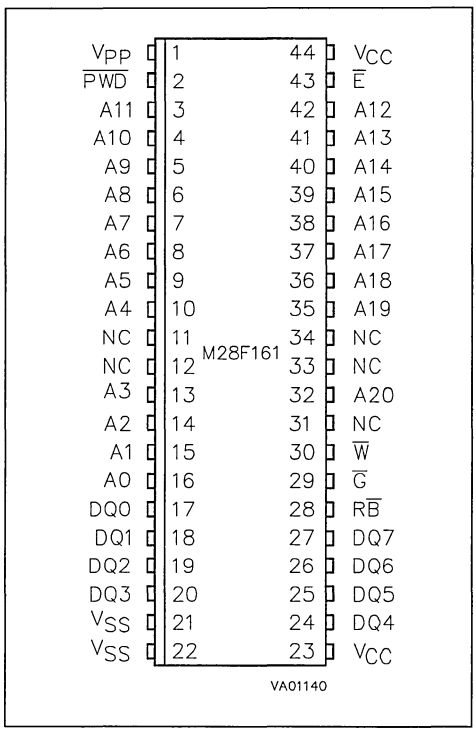
A0-A20	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{PWD}$	Power Down
$R\overline{B}$	Ready Busy Output
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. TSOP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

DESCRIPTION

The M28F161 FLASH MEMORY is a non-volatile memory that may be erased electrically at the sector level and programed byte-by-byte. The interface is directly compatible with most microprocessors. It is intended for computer file systems applications. Plastic TSOP48 (Normal and Reverse pinout) and SO44 packages are used.

Organisation

The organisation is 2 Meg x 8 with Address lines A0-A20 and Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Power Down input places the memory in deep power down. A Ready/Busy output indicates the status of the internal Program/Erase Controller (P/E.C.).

Sectors

Erasure of the memory is in sectors. There are 32 sectors in the memory address space, each of 64K bytes. Programing of each sector takes typically 0.6 seconds and erasure 1.6 seconds, each sector may be programed and erased over 10,000 cycles. All sectors are protected from programming or erasure when the Power Down PWD signal is Low. Sector erase may be suspended while data is read from other sectors of the memory, then resumed.

Command Interface

Commands can be written to a Command Interface latch to perform read, programing, erasure and to monitor the memory's status. When power is first applied, on exit from power down or if V_{CC} falls

below V_{LKO}, the command interface is reset to Read Memory Array. Four operations can be performed by the appropriate bus cycles, Read a Byte from the Array, Output Disable, Standby and Write a Command of an Instruction.

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the Array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte program and sector erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation.

Byte programming takes typically 9µs, sector erase typically 1.6 seconds. Erasure of a memory sector may be suspended in order to read data from another sector and then resumed. A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation. In addition a Ready/Busy output indicates the status of the P/E.C. After Programing or Erasure the command interface must be reset by giving the Read Memory Array instruction before the memory contents can be accessed.

Power Saving

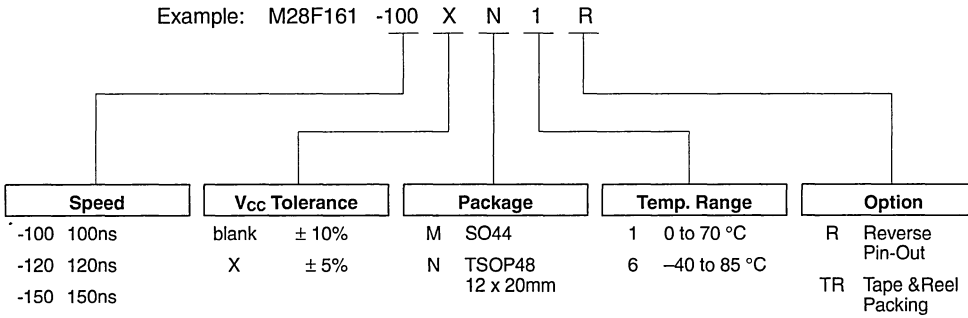
The M28F161 memory has a number of power saving features. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Power Down $\overline{PWD}$ signals are at V_{CC}, when the supply current drops to typically 30µA. A deep power down mode is enabled when the Power Down $\overline{PWD}$ signal is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 400ns maximum, with instructions to the C.I. recognised after 1µs.

Table 2. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address	Data Output
RD	Read	1	Write	X	FFh	Note 2		
RSR	Read Status Register	1	Write	X	70h	Note 2		
RSIG	Read Electronic Signature	3	Write	X	90h	Note 2		
EE	Erase	2	Write	Sector Address	20h	Write	Sector Address	D0h
PG	Program	2	Write	Byte Address	40h or 10h	Write	Byte Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	B0h			
ER	Erase Resume	1	Write	X	D0h			

Notes: 1. X = Don't Care
2. The first cycle of the RD, RSR or RSIG instuction is followed by read operations to read the Array, Status Register or Electronic Signature code.

ORDERING INFORMATION SCHEME



For a list of available options (Speed, V_{CC} Tolerance, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

I^2C BUS EEPROM

SERIAL ACCESS CMOS 1K (128 x 8) EEPROMs

- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24C01 version
  - 3V to 5.5V for ST24x01C versions
  - 2.5V to 5.5V for ST25C01, ST25x01C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W01C and ST25W01C
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES FOR "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGN: ST24/25C01C and ST24/25W01C

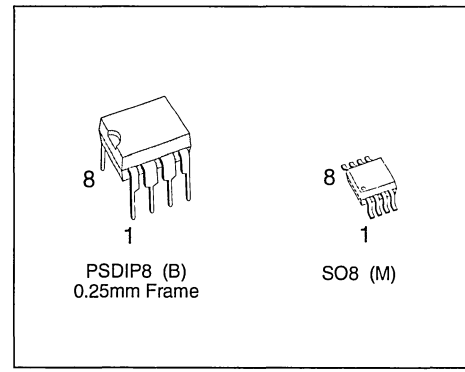
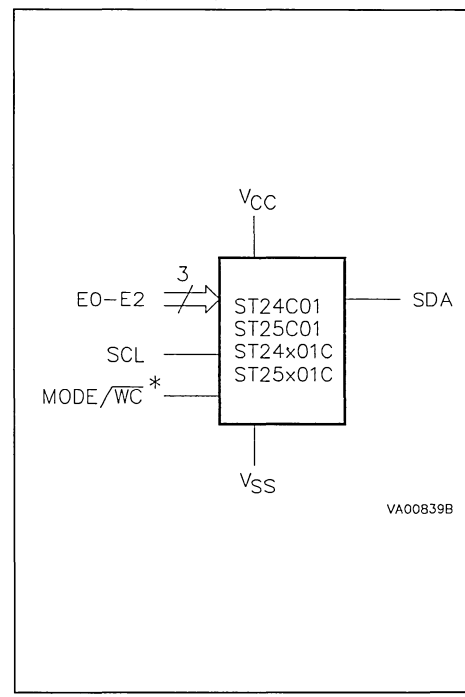


Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W01C products.

DESCRIPTION

This specification covers a range of 1K bits I^2C bus EEPROM products, the ST24/25C01, the ST24/25C01C and the ST24/25W01C. In the text, products are referred to as ST24/25x01C, where

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Wnte Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

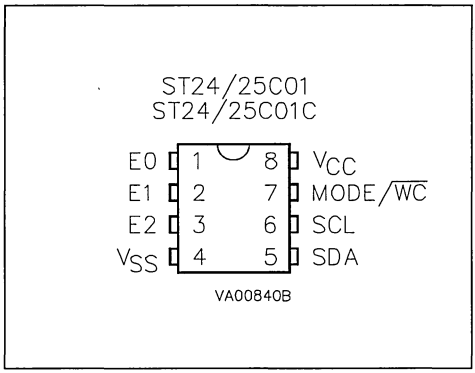


Figure 2B. SO Pin Connections

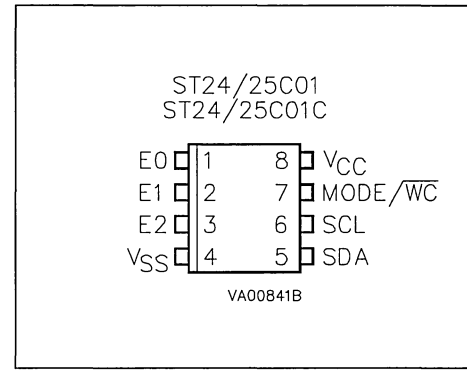


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage	ST24/25C01 ST24/25x01C		–0.3 to V_{CC} +0.6 –0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST24/25C01 ST24/25x01C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST24/25C01 ST24/25x01C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

"x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x01C are 1K bit electrically erasable programmable memories (EEPROM), organized as 128 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 3 chip enable inputs (E2, E1, E0) so that up to 8 x 1K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol with all memory operations synchronized

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	RW bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X		START, Device Select, RW = '0', Address
	'1'	X	1	reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	1 to 128	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, RW = '0'
Multibyte Write (2)	'0'	V_{IH}	4	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, RW = '0'

Notes: 1. X = V_{IH} or V_{IL}
2. Multibyte Write not available in ST24/25W01C versions.

Table 5. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST24C01, ST25C01	1,000,000	10
ST24C01C, ST25C01C ST24W01C, ST25W01C	1,000,000	10

by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

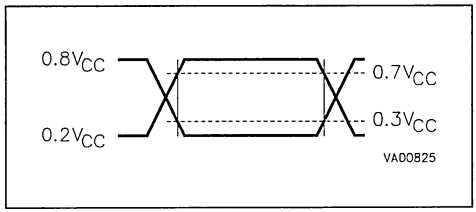
When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 3. AC Testing Input Output Waveforms



SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 4).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 4).

Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits (b3, b2, b1) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as V_{IH} (Multibyte Write mode).

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered only for ST24W01C and ST25W01C versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. When unconnected, the $\overline{WC}$ input is internally read as V_{IL}. The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

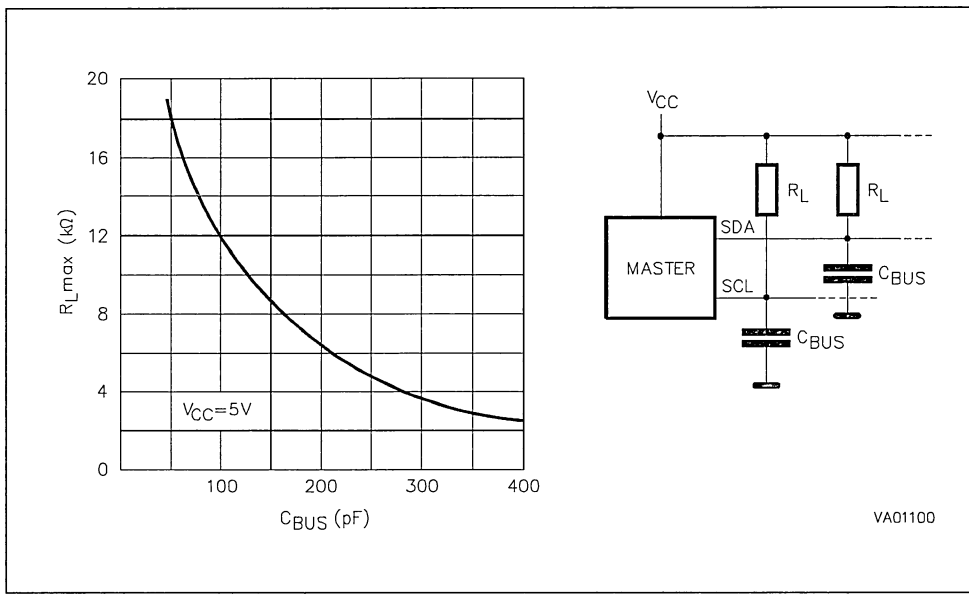


Table 6. Capacitance (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ

Note: 1. Sampled only, not 100% tested.

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0 - E2, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0 - E2, MODE, $\overline{WC}$)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
V_{POR} (1)	Power On Reset Threshold (ST25 series)		1.5	2.4	V
V_{CC} Read (1)	V_{CC} Range for Read Operations (ST25 series)		2.5	5.5	V
V_{CC} Write	V_{CC} Range for Write Operations		2.5	5.5	V

Note: 1. At the time of publication of this data sheet, the statistical history, for the ST25x01C, was not yet sufficient to guarantee a V_{CC} Read = 2V. For the lastest information contact your local SGS-THOMSON Sales Office.

Table 8. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD.STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD.DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU.DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU.STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	T_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms.

DEVICE OPERATION

I²C Bus Background

The ST24/25x01C support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x01C are always slave devices in all communications.

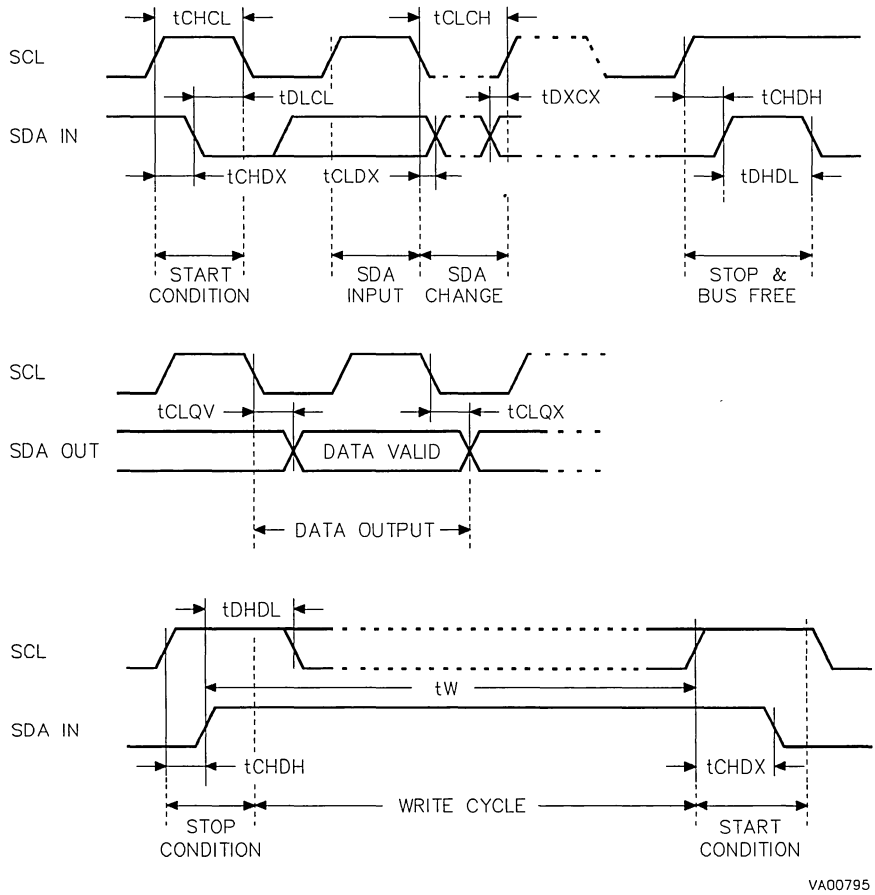
Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x01C continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x01C and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x01C sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Figure 5. AC Waveforms



DEVICE OPERATION (cont'd)

Memory Addressing. To start communication between the bus master and the slave ST24/25x01C, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following 3 bits identify the specific memory on the bus. They are matched to the chip enable signals E2, E1, E0. Thus up to 8 x 1K memories can be connected on the same bus giving a memory capacity total of 8K bits. After a START condition any memory on the bus will identify the device code and compare the following 3 bits to its chip enable inputs E2, E1, E0.

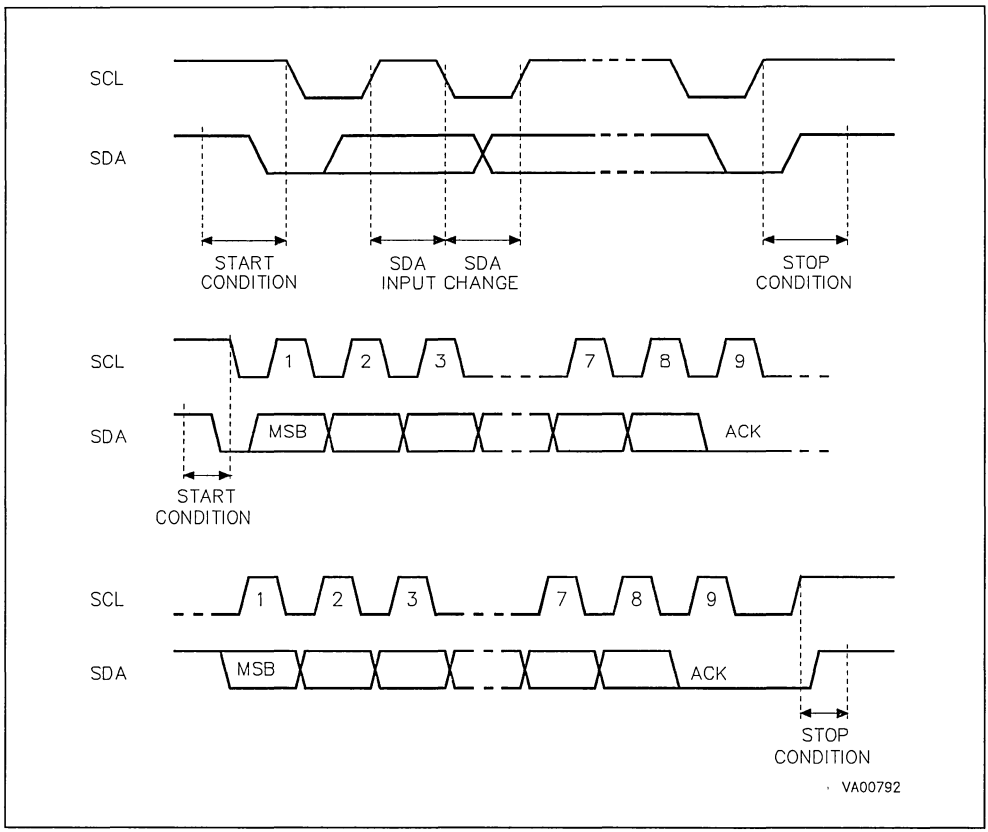
The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Write Operations

The Multibyte Write mode (only available on the ST24/25C01 and ST24/25C01C versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 7 bits (the Most Significant Bit is ignored) provides access to any of the 128 bytes of the memory. After receipt of the

Figure 6. I^2C Bus Protocol



byte address the device again responds with an acknowledge.

For the ST24/25W01C versions, any write command with $\overline{WC}$ = 1 (during a period of time from the START condition untill the end of the Byte Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 5 most significant address bits A6-A2), the programming time is then doubled to a maximum of 20ms. Writing more than 4 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 8 bytes long). However, the Multibyte Write can properly write up to 8 consecutive bytes only if the first address of these 8 bytes is the first address of the row, the 7 following bytes being written in the 7 following bytes of this same row.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (tW) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the

DEVICE OPERATION (cont'd)

memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25x01C wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the St24/25x01C terminate the data transfer and switches to a standby state.

Figure 7. Write Cycle Polling using ACK

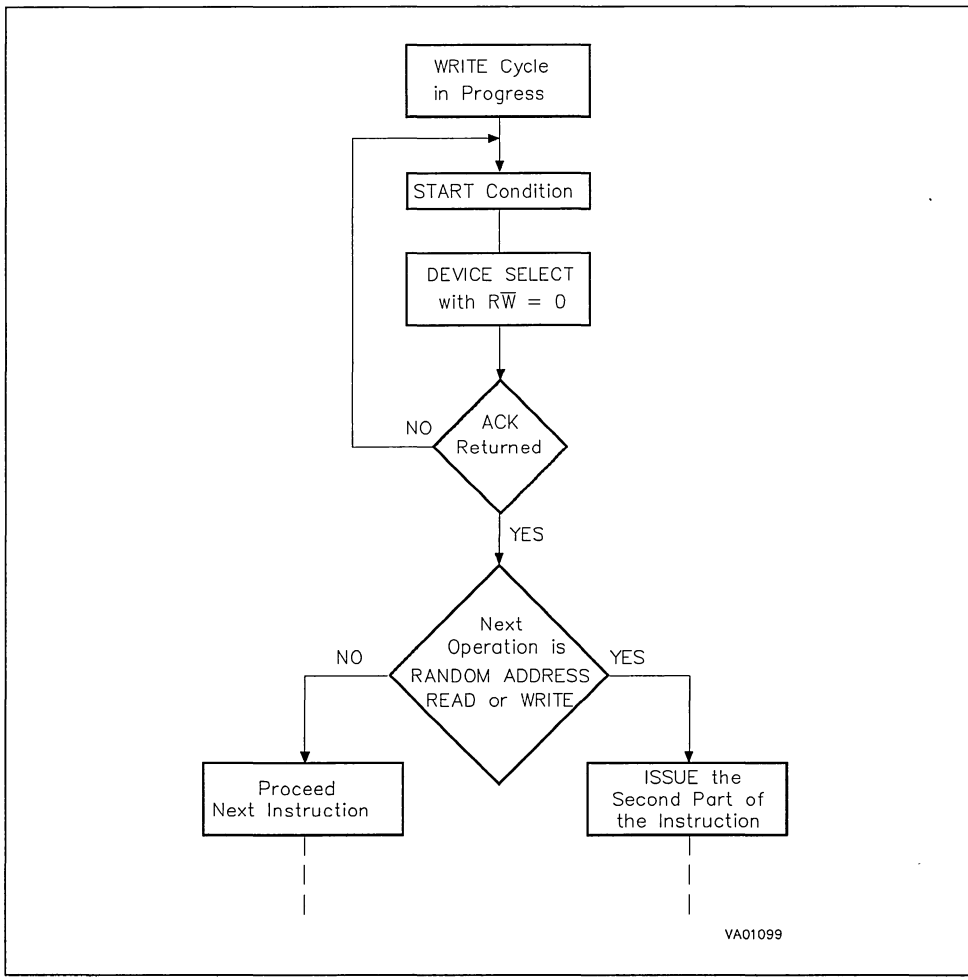


Figure 8. Write Modes Sequence (ST24/25C01, ST24/25C01C)

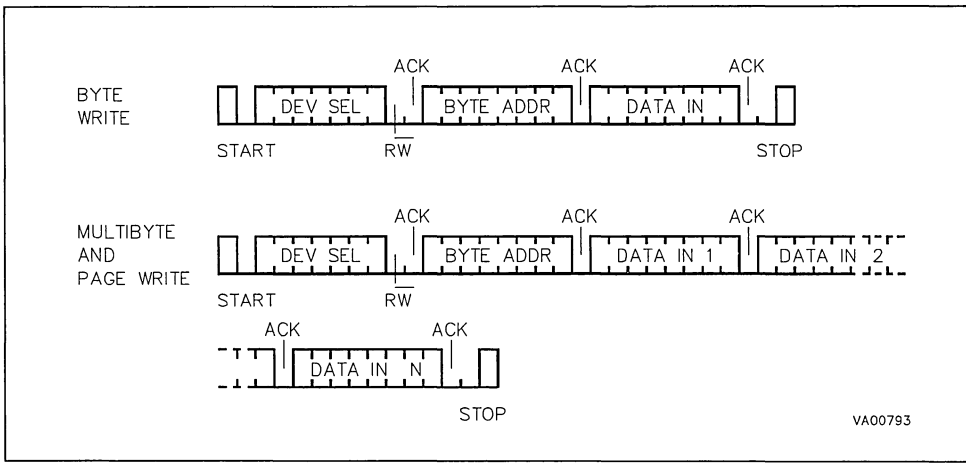


Figure 9. Write Modes Sequence with Write Control = 1 (ST24/25W01C)

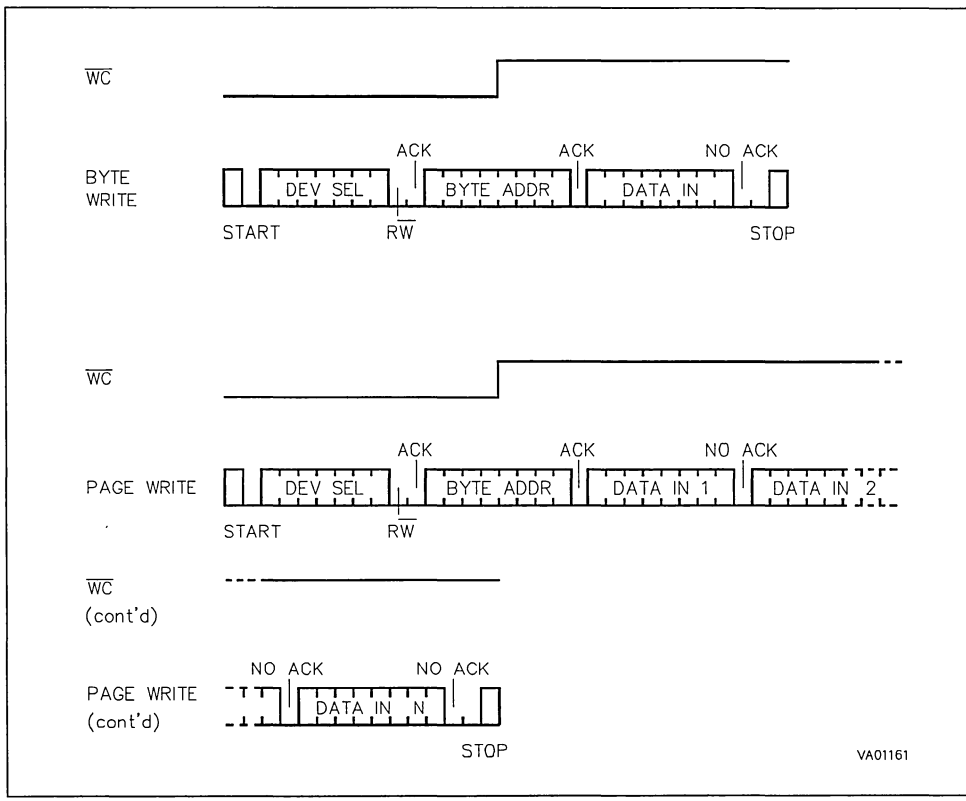
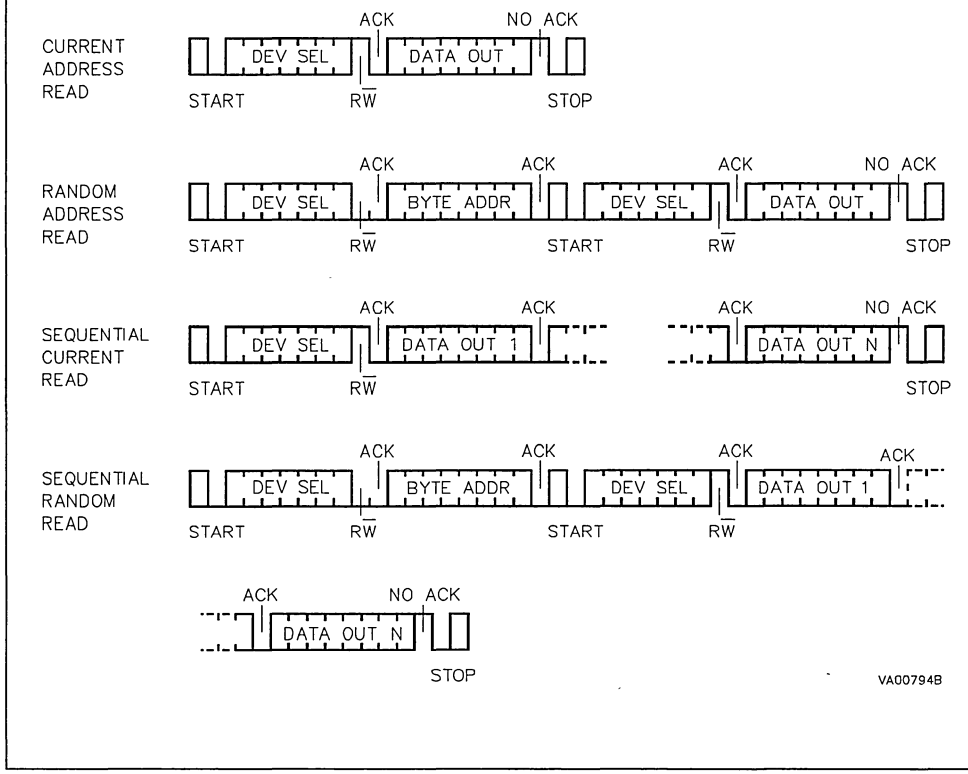
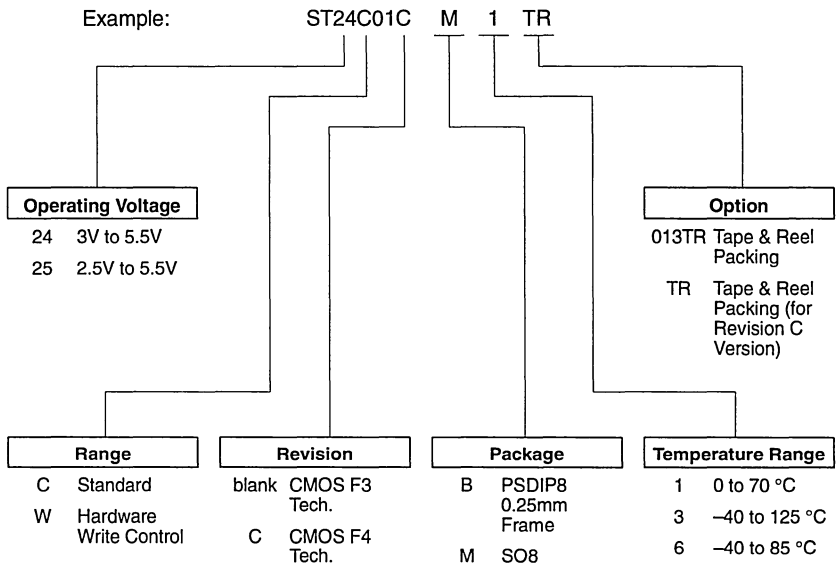


Figure 10. Read Modes Sequence



ORDERING INFORMATION SCHEME



Parts are shipped with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Range, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SERIAL ACCESS CMOS 2K (256 x 8) EEPROMs

- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24C02A version
  - 3V to 5.5V for ST24x02C versions
  - 2.5V to 5.5V for ST25C02A, ST25x02C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W02C and ST25W02C
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES for "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGNS: ST24/25C02C and ST24/25W02C

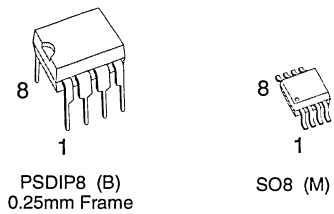
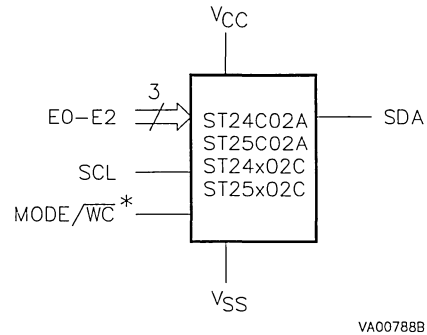


Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W02C products.

DESCRIPTION

This specification covers a range of 2K bits I^2C bus EEPROM products, the ST24/25C02A, the ST24/25C02C and the ST24/25W02C. In the text, products are referred to as ST24/25x02C, where

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

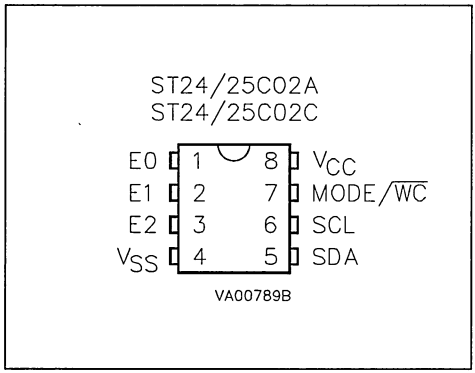


Figure 2B. SO Pin Connections

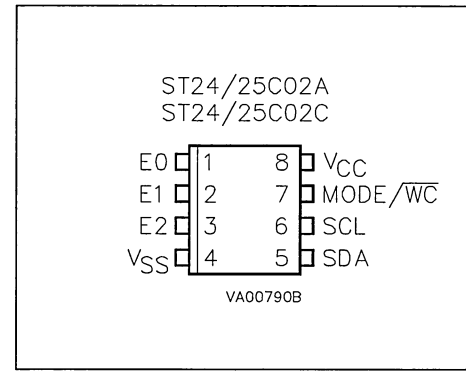


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage	ST24/25C02A ST24/25x02C		–0.3 to V_{CC} +0.6 –0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST24/25C02A ST24/25x02C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST24/25C02A ST24/25x02C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

"x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x02C are 2K bit electrically erasable programmable memories (EEPROM), organized as 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 3 chip enable inputs (E2, E1, E0) so that up to 8 x 2K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol with all memory operations synchronized

Table 3. Device Select Code

	Device Code				Chip Enable			$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	$R\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	$R\overline{W}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, $R\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 256	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, $R\overline{W}$ = '0'
Multibyte Write (2)	'0'	V_{IH}	4	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, $R\overline{W}$ = '0'

Notes: 1. X = V_{IH} or V_{IL}
2. Multibyte Write not available in ST24/25W02C versions.

Table 5. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST24C02A, ST25C02A	1,000,000	10
ST24C02C, ST25C02C ST24W02C, ST25W02C	1,000,000	10

by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

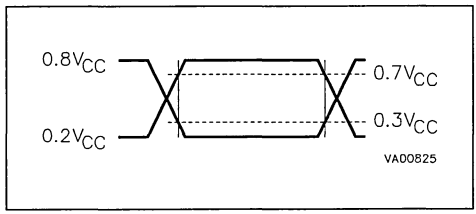
When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 3. AC Testing Input Output Waveforms



SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 4).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 4).

Chip Enable (E2 - E0). These chip enable inputs are used to set the 3 least significant bits (b3, b2, b1) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as a V_{IH} (Multibyte Write mode).

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered only for ST24W02C and ST25W02C versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle.

The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

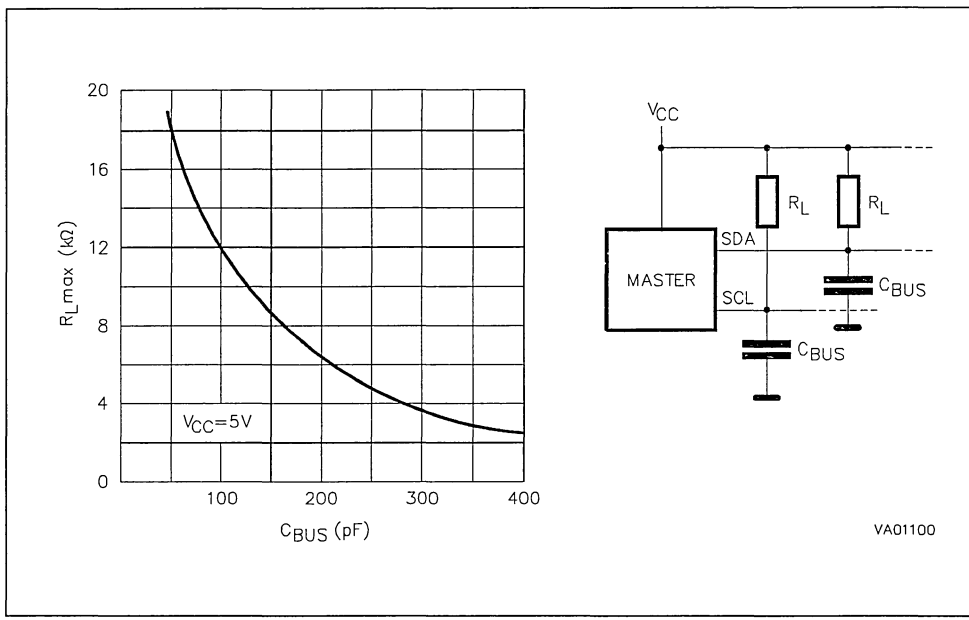


Table 6. Capacitance (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		100	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		5	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, MODE, $\overline{WC}$)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
V_{POR} (1)	Power On Reset Threshold (ST25 series)		1.5	2.4	V
V_{CC} Read (1)	V_{CC} Range for Read Operations (ST25 series)		2.5	5.5	V
V_{CC} Write	V_{CC} Range for Write Operations		2.5	5.5	V

Note: 1. At the time of publication of this data sheet, the statistical history, for the ST25x02C, was not yet sufficient to guarantee a V_{CC} Read = 2V. For the lastest information contact your local SGS-THOMSON Sales Office.

Table 8. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD.STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU.DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	T_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms.

DEVICE OPERATION

I²C Bus Background

The ST24/25x02C support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x02C are always slave devices in all communications.

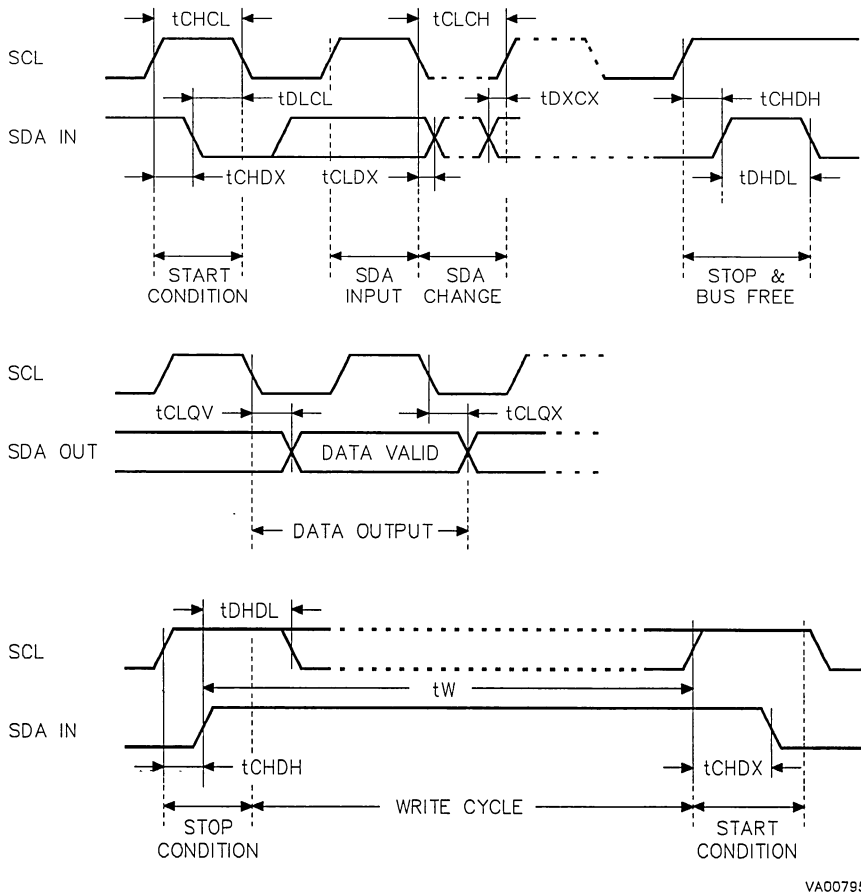
Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x02C continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x02C and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x02C sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock

Figure 5. AC Waveforms



DEVICE OPERATION (cont'd)

low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x02C, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following 3 bits identify the specific memory on the bus. They are matched to the chip enable signals E2, E1, E0. Thus up to 8 x 2K memories can be connected on the same bus giving a memory capacity total of 16K bits. After a START condition any memory on the bus will identify the device code and compare the following 3 bits to its chip enable inputs E2, E1, E0.

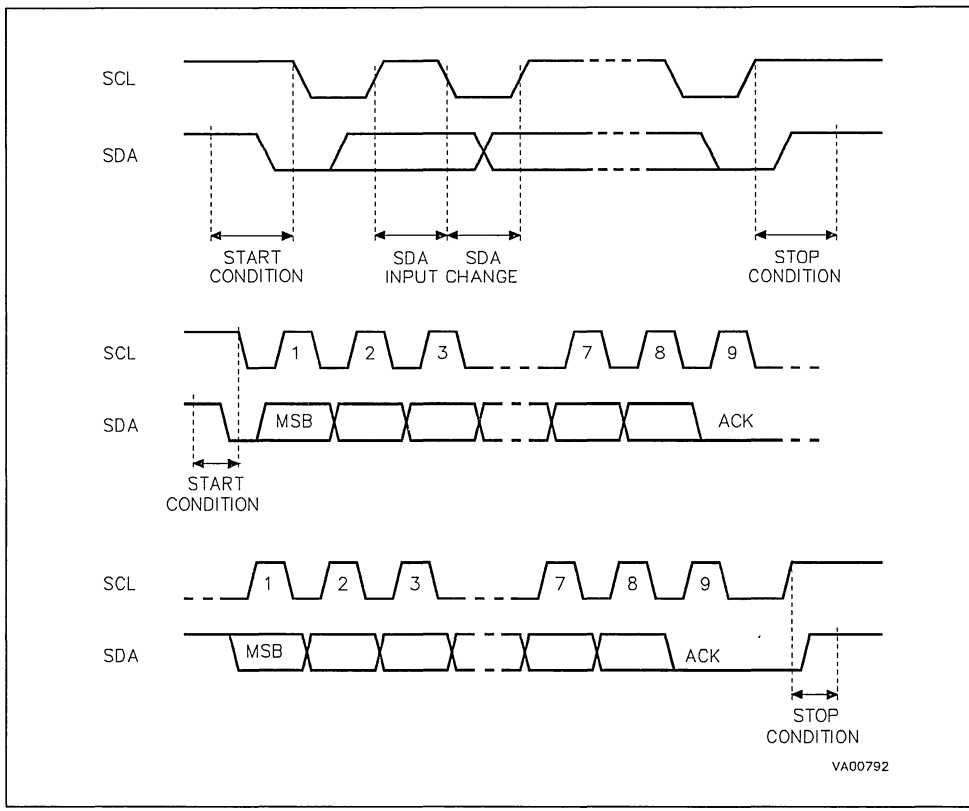
The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Write Operations

The Multibyte Write mode (only available on the ST24/25C02A AND ST24/25C02C versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

Figure 6. I^2C Bus Protocol



For the ST24/25W02C versions, any write command with $\overline{WC}$ = 1 will not modify the memory content.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 6 most significant address bits A7-A2), the programming time is then doubled to a maximum of 20ms. Writing more than 4 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 8 bytes long). However, the Multibyte Write can properly write up to 8 consecutive bytes only if the first address of these 8 bytes is the first address of the row, the 7 following bytes being written in the 7 following bytes of this same row.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the master issues a START condition followed by a device select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses,

DEVICE OPERATION (cont'd)

with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25x02C wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x02C terminate the data transfer and switches to a standby state.

Figure 7. Write Cycle Polling using ACK

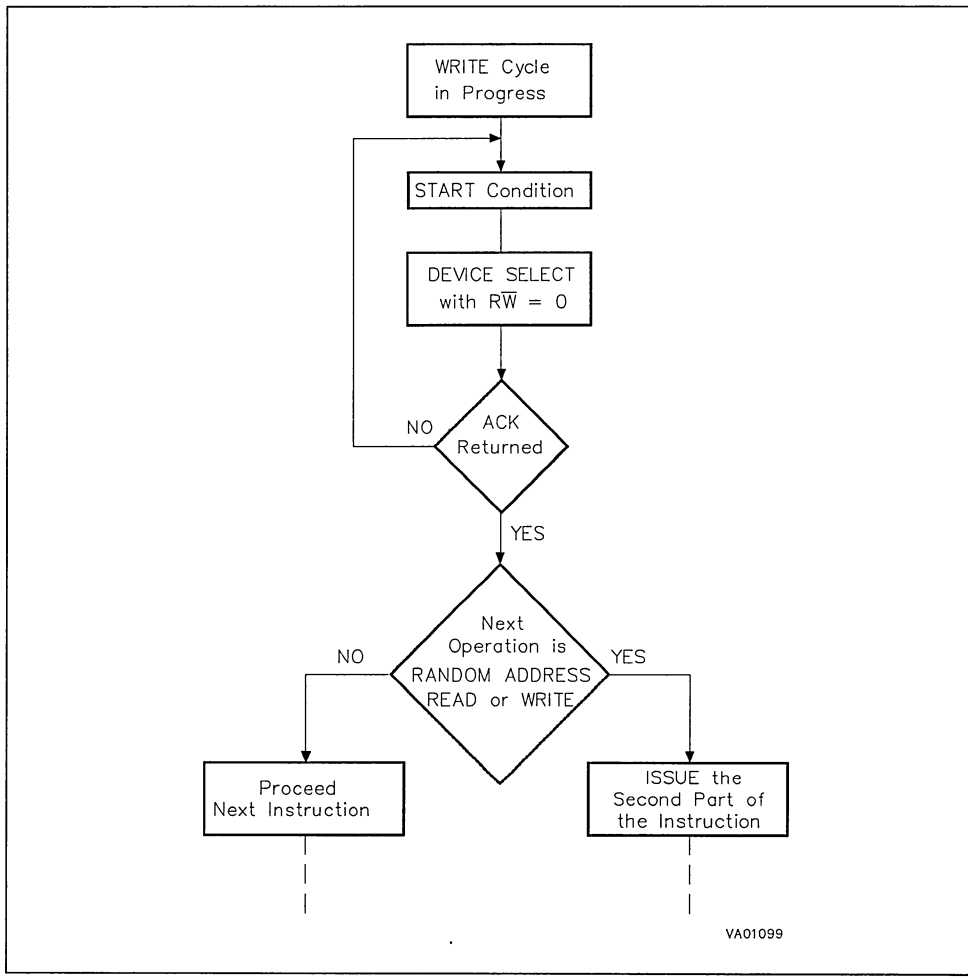


Figure 8. Write Modes Sequence (ST24/25C02A, ST24/25C02C)

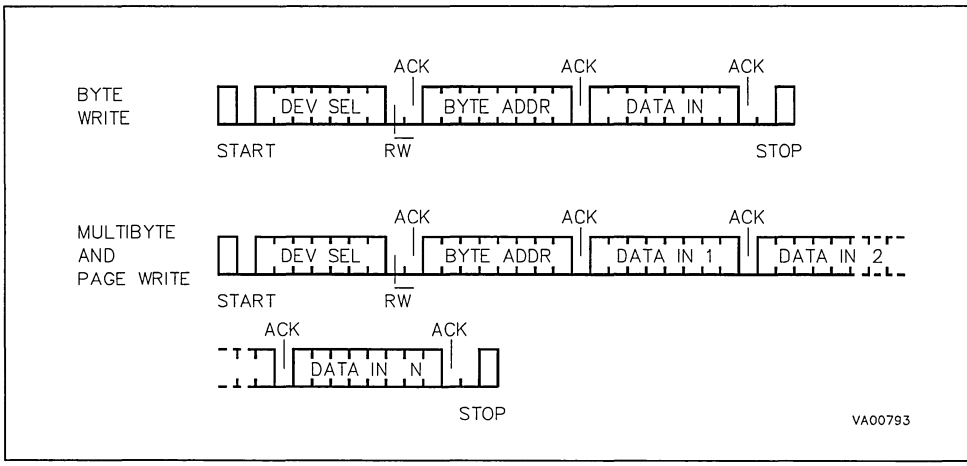


Figure 9. Write Modes Sequence with Write Control = 1 (ST24/25W02C)

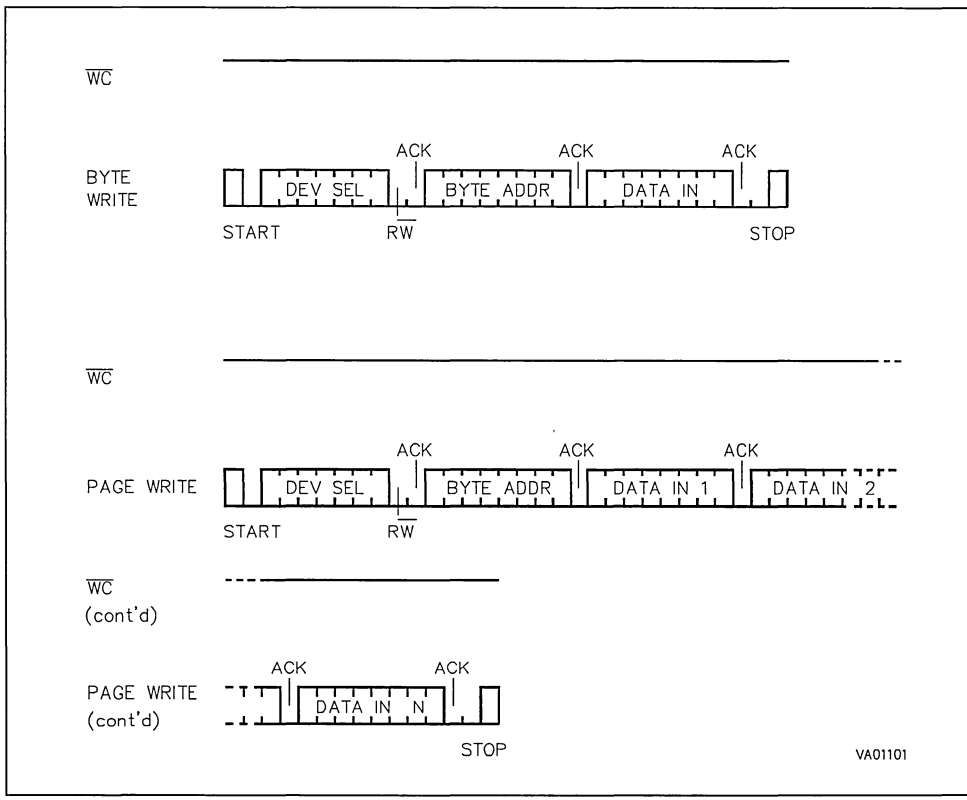
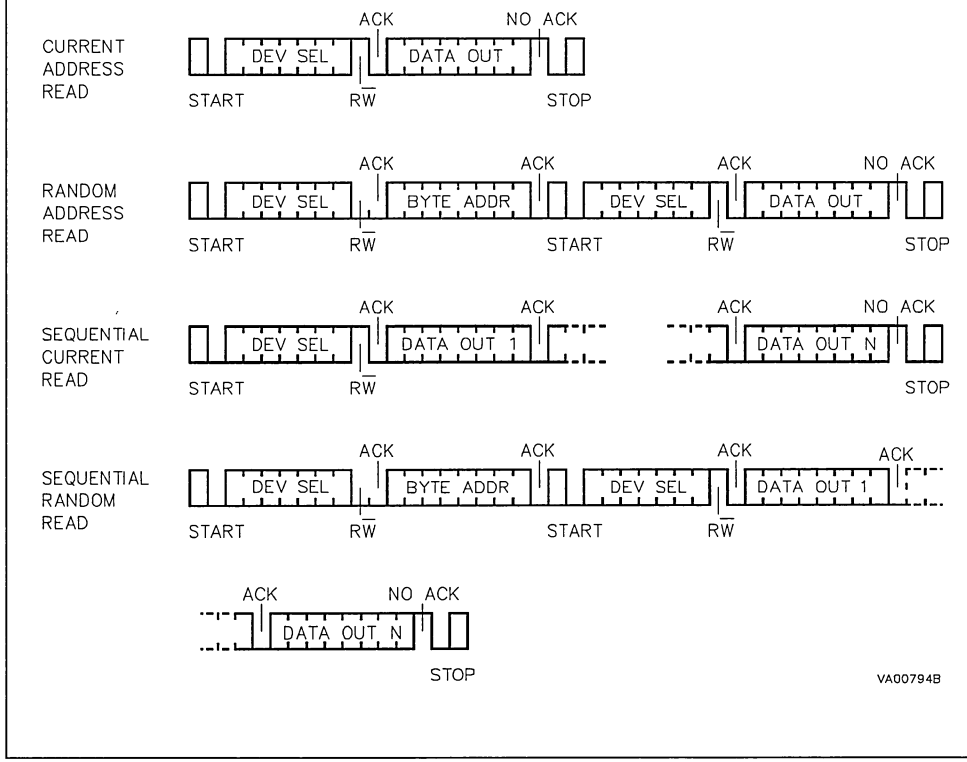
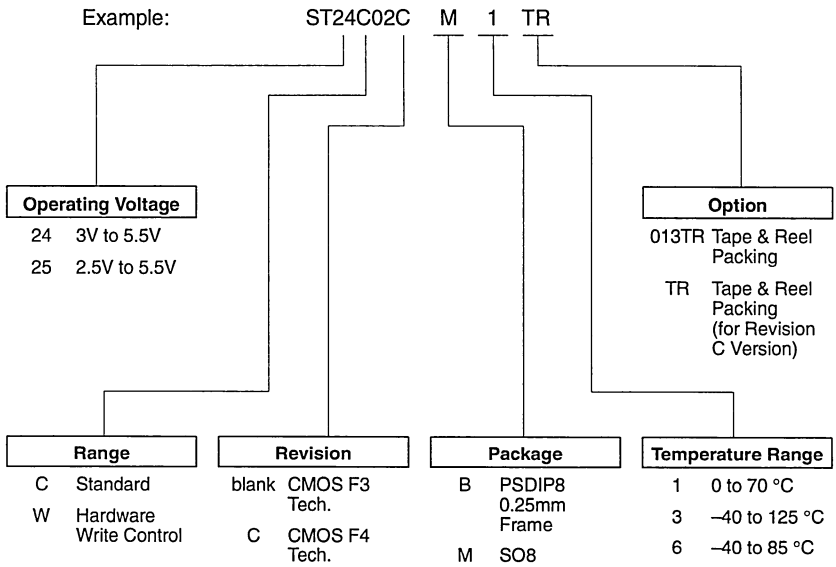


Figure 10. Read Modes Sequence



ORDERING INFORMATION SCHEME



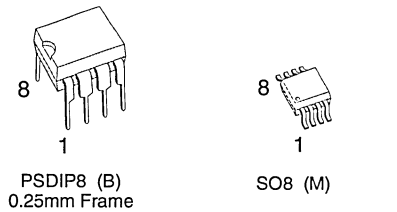
Parts are shipped with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Range, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SERIAL ACCESS CMOS 4K (512 x 8) EEPROMs

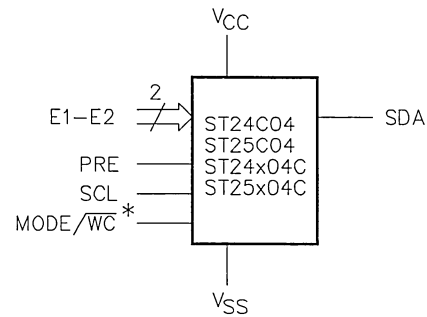
- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24C04 version
  - 3V to 5.5V for ST24x04C versions
  - 2.5V to 5.5V for ST25C04, ST25x04C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W04C and ST25W04C
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES for "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGNS: ST24/25C04C and ST24/25W04C



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W04C products.

DESCRIPTION

This specification covers a range of 4K bits I^2C bus EEPROM products, the ST24/25C04, the ST24/25C04C and the ST24/25W04C. In the text, products are referred to as ST24/25x04C, where

Table 1. Signal Names

PRE	Write Protect Enable
E1 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

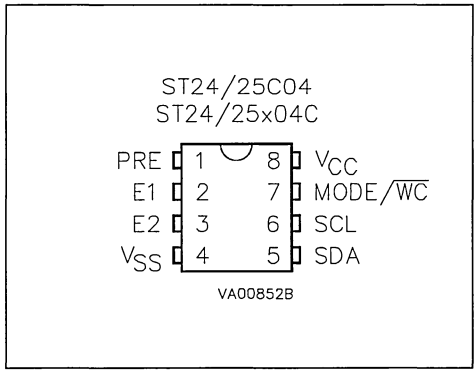


Figure 2B. SO Pin Connections

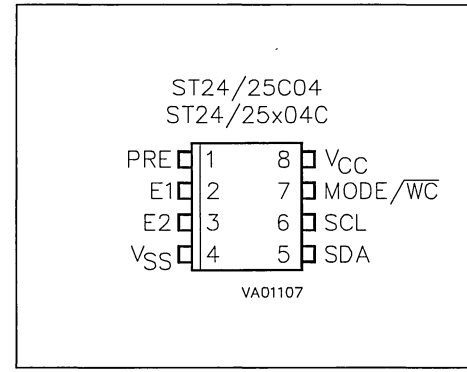


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage	ST24/25C04 ST24/25x04C		–0.3 to V_{CC} +0.6 –0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST24/25C04 ST24/25x04C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST24/25C04 ST24/25x04C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

"x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x04C are 4K bit electrically erasable programmable memories (EEPROM), organized as 2 blocks of 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available. The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 2 chip enable inputs (E2, E1) so that up to 4 x 4K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol with all memory operations synchronized by the serial

Table 3. Device Select Code

	Device Code				Chip Enable		Block Select	RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	A8	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	RW bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X		START, Device Select, RW = '0', Address
	'1'	X	1	reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	1 to 512	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, RW = '0'
Multibyte Write (2)	'0'	V_{IH}	4	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, RW = '0'

Notes: 1. X = V_{IH} or V_{IL}
2. Multibyte Write not available in ST24/25W04C versions.

Table 5. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST24C04, ST25C04	1,000,000	10
ST24C04C, ST25C04C ST24W04C, ST25W04C	1,000,000	10

clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

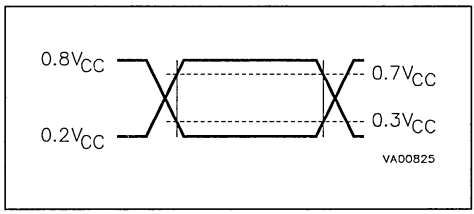
When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 3. AC Testing Input Output Waveforms



SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 4).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 4).

Chip Enable (E1 - E2). These chip enable inputs are used to set the 2 least significant bits (b2, b3) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Protect Enable (PRE). The PRE input pin, in addition to the status of the Block Address Pointer bit (b2, location 1FFh as in Figure 7), sets the PRE write protection active.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as V_{IH} (Multibyte Write mode).

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered only for ST24W04C and ST25W04C versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. . The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

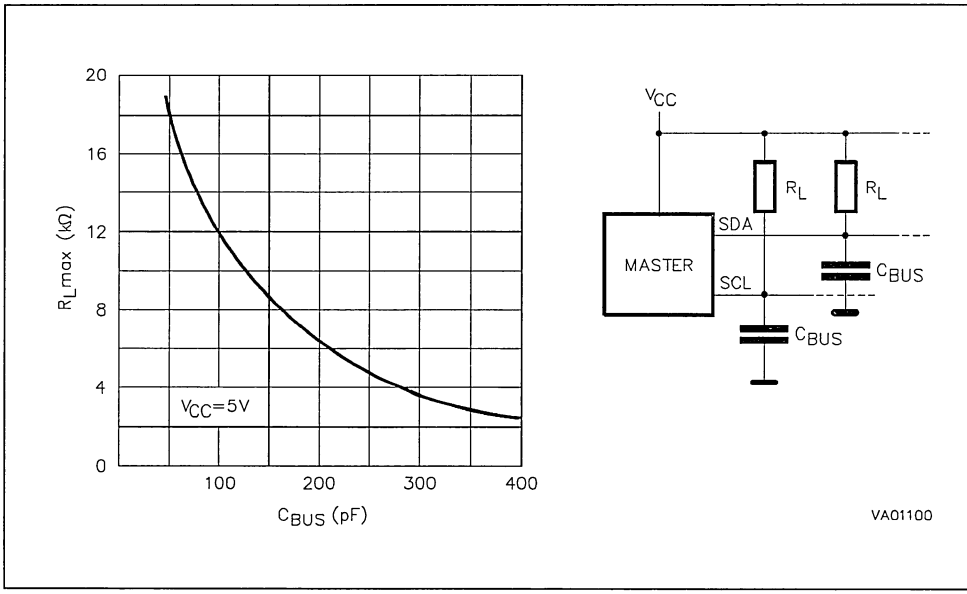


Table 6. Capacitance (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		100	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		5	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E1 - E2, PRE, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E1 - E2, PRE, MODE, $\overline{WC}$)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
V_{POR} (1)	Power On Reset Threshold (ST25 series)		1.5	2.4	V
V_{CC} Read (1)	V_{CC} Range for Read Operations (ST25 series)		2.5	5.5	V
V_{CC} Write	V_{CC} Range for Write Operations		2.5	5.5	V

Note: 1. At the time of publication of this data sheet, the statistical history, for the ST25x04C, was not yet sufficient to guarantee a V_{CC} Read = 2V. For the lastest information contact your local SGS-THOMSON Sales Office.

Table 8. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU.STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD.STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	T_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms.

DEVICE OPERATION

I²C Bus Background

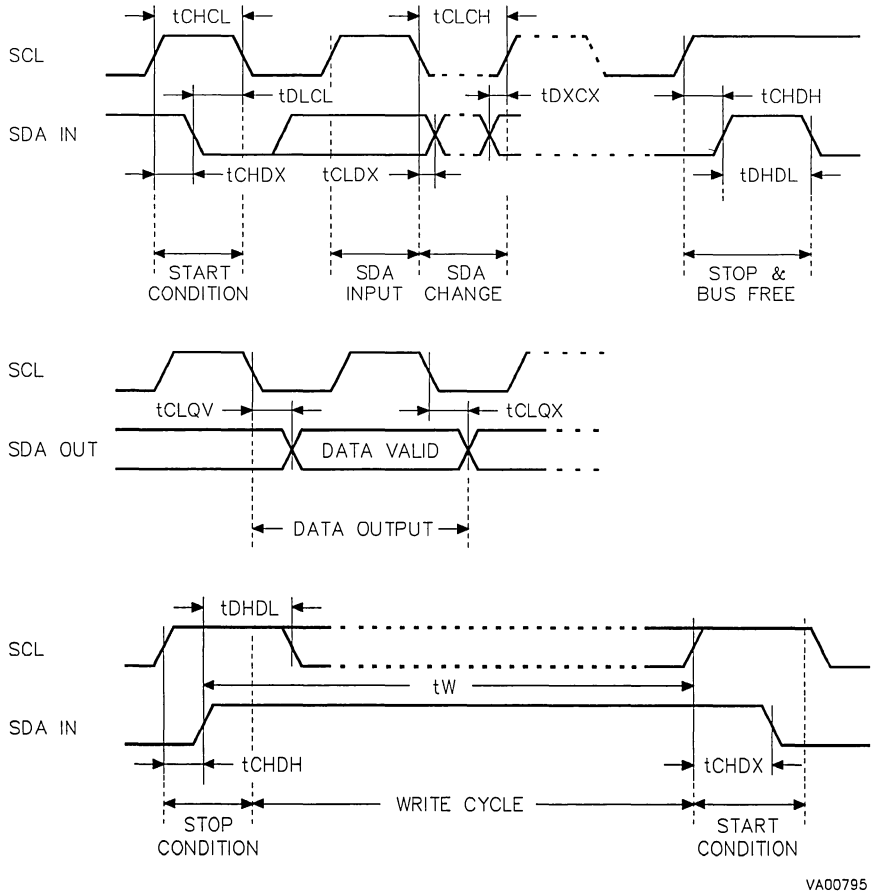
The ST24/25x04C support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x04C are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x04C continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x04C and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Figure 5. AC Waveforms



DEVICE OPERATION (cont'd)

Data Input. During data input the ST24/25x04C sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x04C, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following 2 bits identify the specific memory on the bus. They are matched to the chip enable signals E2, E1. Thus up to 4 x 4K memories can be connected on the same bus giving a memory capacity total of 16K bits. After a START condition any memory on the bus will identify the device code and compare the following 2 bits to its chip enable inputs E2, E1.

The 7th bit sent is the block number (one block = 256 bytes). The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Write Operations

The Multibyte Write mode (only available on the ST24/25C04 and ST24/25C04C versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The memory acknowledges this and waits for a byte

Figure 6. I^2C Bus Protocol

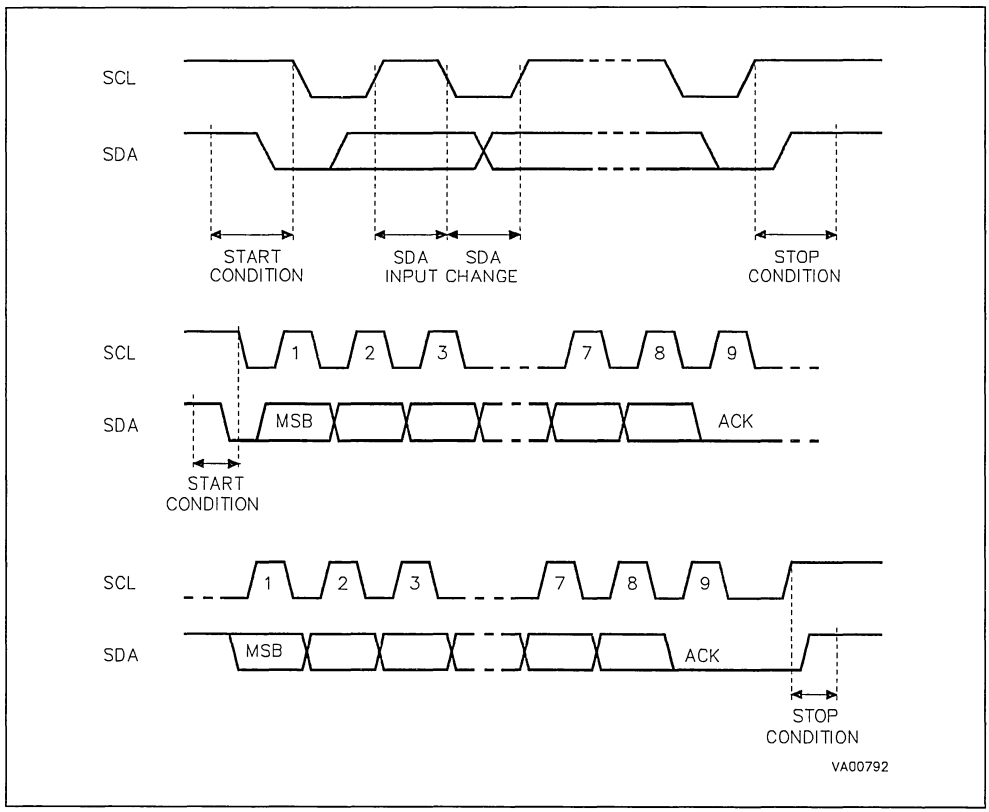
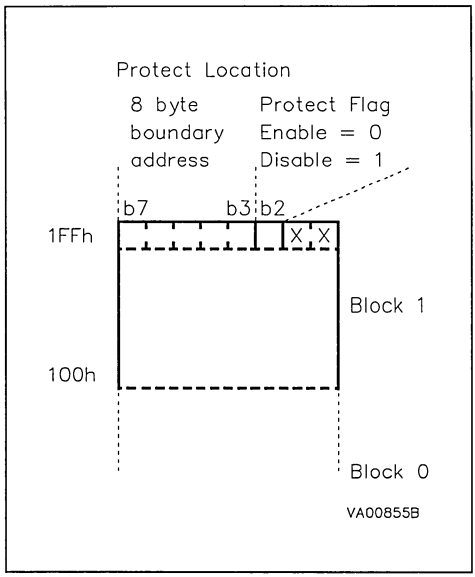


Figure 7. Memory Protection



address. The byte address of 8 bits provides access to one block of 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W04C versions, any write command with $\overline{WC}$ = 1 will not modify the memory content.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 6 most significant address bits A7-A2), the programming time is then doubled to a maximum of 20ms. Writing more than 4 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 8 bytes long). However, the Multibyte Write can properly write up to 8 consecutive bytes as soon as the first address of these 8 bytes is the first address of the row, the 7 following bytes being written in the 7 following bytes of this same row.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same inside one block. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 8).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Write Protection. Data in the upper block of 256 bytes of the memory may be write protected. The memory is write protected between a boundary address and the top of memory (address 1FFh) when the PRE input pin is taken high and when the Protect Flag (bit b2 in location 1FFh) is set to '0'. The boundary address is user defined by writing a value in the Block Address Pointer (location 1FFh).

This Block Address Pointer defines an 8 bit address composed of the 5 MSBs of location 1FFh and 3

DEVICE OPERATION (cont'd)

LSBs which are read as '0'. This address pointer can therefore address a boundary in steps of 8 bytes.

The sequence to follow to use the Write Protected feature is:

- write the data to be protected into the top of the memory, up to, but not including, location 1FFh;
- set the protection by writing the correct bottom boundary address, into location 1FFh, with bit b2 (Protect flag) set to '0'.

The area will now be protected when the PRE input is taken High.

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input pin High). If the Multibyte Write starts at the location right below the first byte of the Write Protected area, then the instruction will write over the first 3 bytes of the Write Protected area. The area protected is therefore smaller than the content defined in the location 1FFh, by 3 bytes. This does not apply to the Page Write mode as the address counter 'roll-over' and thus cannot go above the 8 bytes lower boundary of the protected area.

Figure 8. Write Cycle Polling using ACK

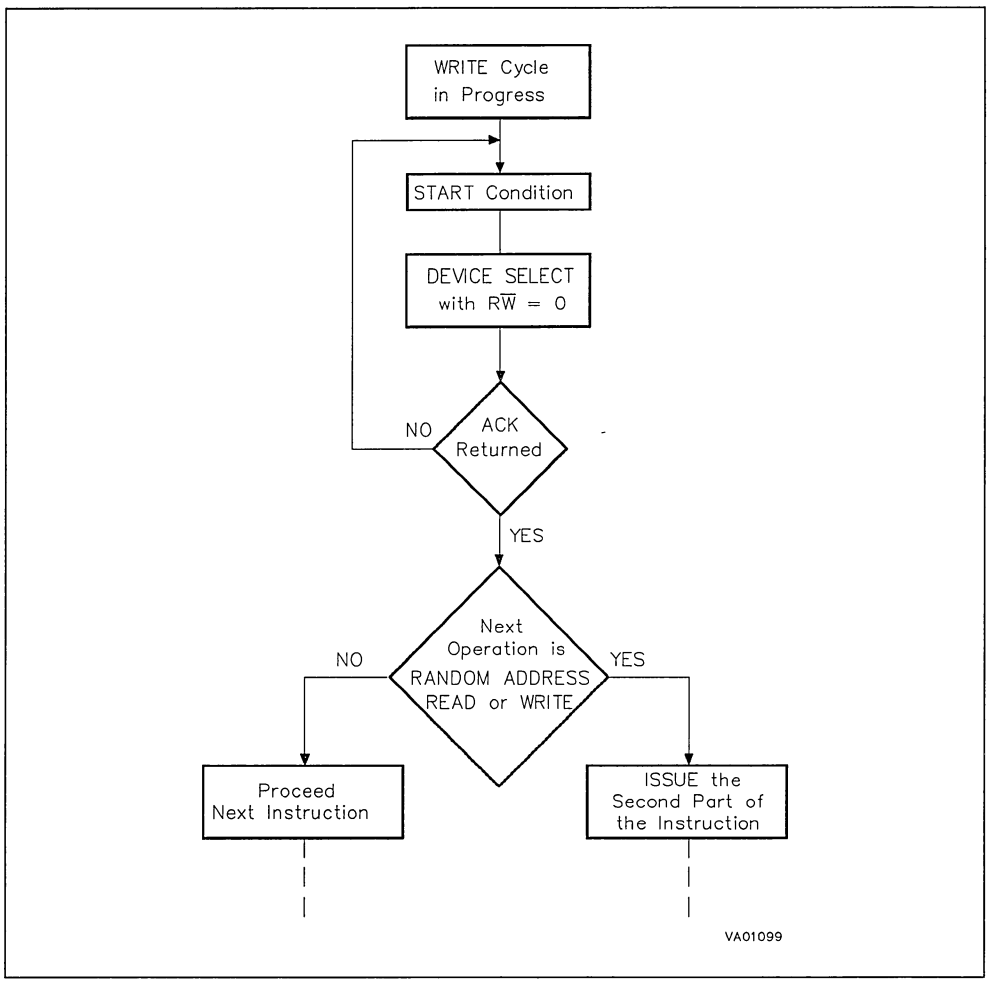


Figure 9. Write Modes Sequence (ST24/25C04, ST24/25C04C)

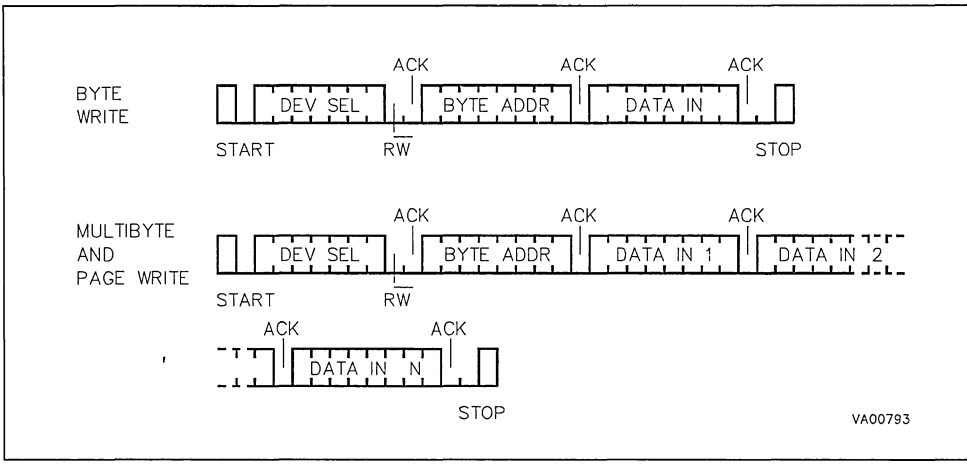
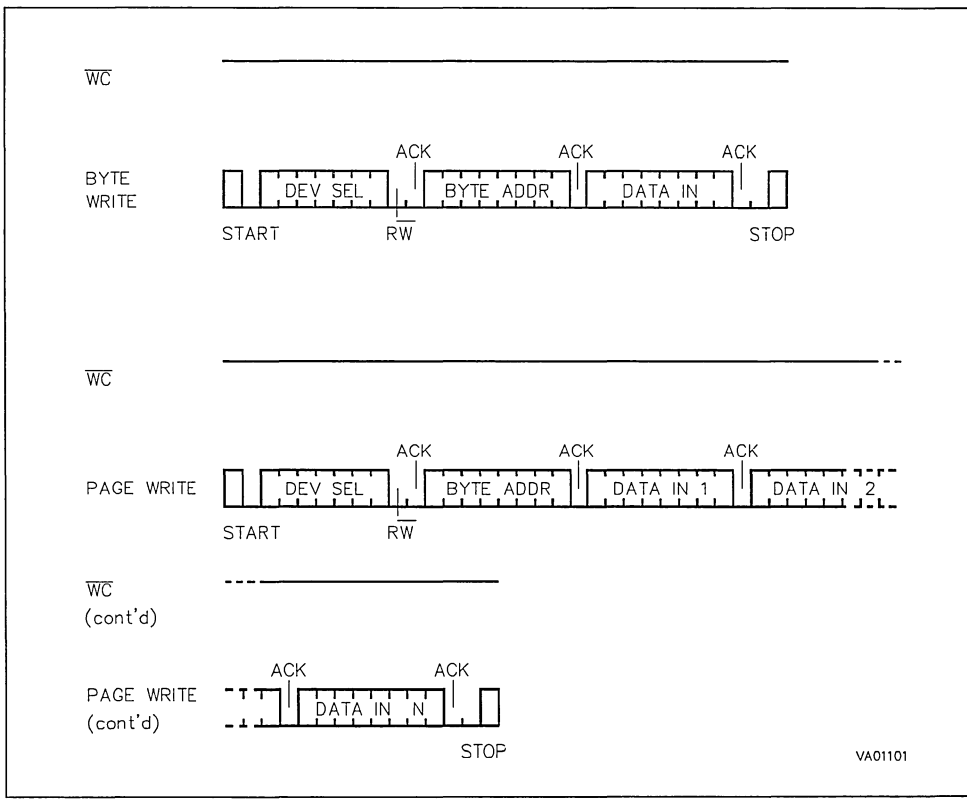


Figure 10. Write Modes Sequence with Write Control = 1 (ST24/25W04C)



Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

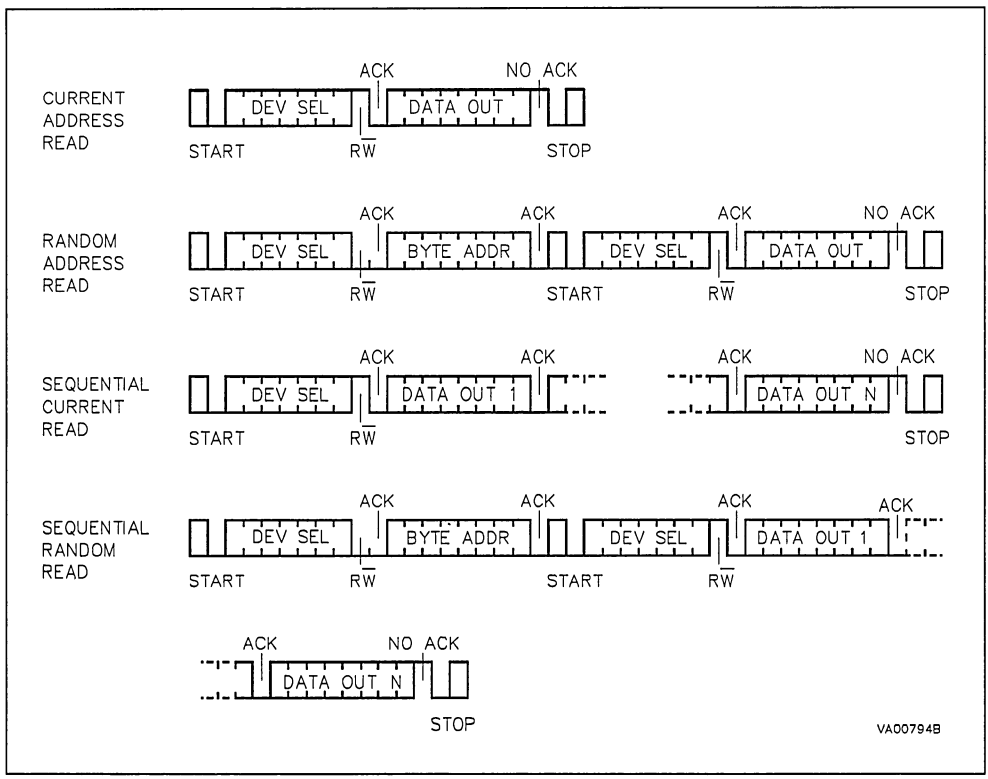
Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 11. This is followed by another START condition from the master and the byte address is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

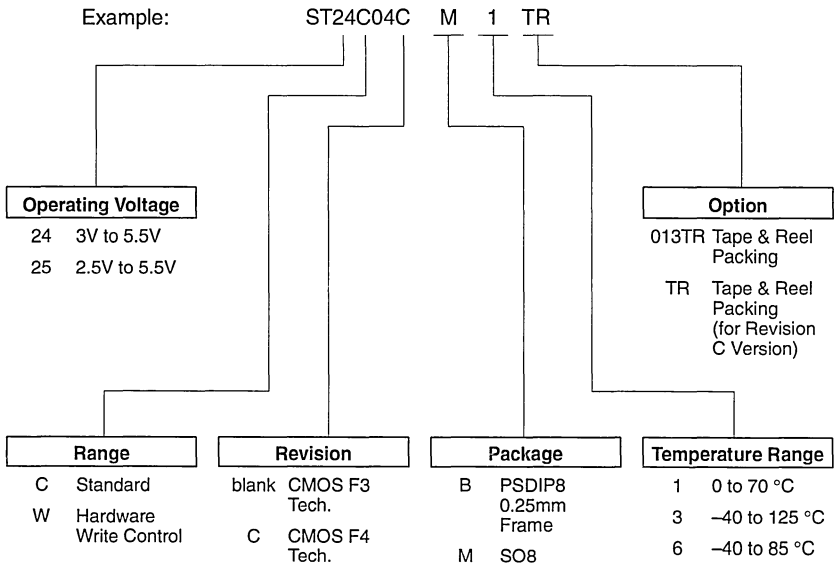
Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25x04C wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x04C terminate the data transfer and switches to a standby state.

Figure 11. Read Modes Sequence



ORDERING INFORMATION SCHEME



Parts are shipped with the memory content set at all "1's" (FFh).

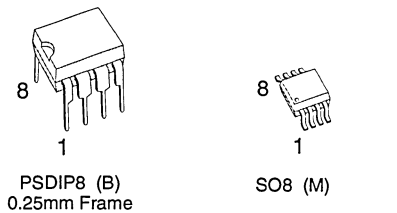
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

ST24C08, ST25C08
ST24x08C, ST25x08C

SERIAL ACCESS CMOS 8K (1024 x 8) EEPROMs

- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24C08 version
  - 3V to 5.5V for ST24x08C versions
  - 2.5V to 5.5V for ST25C08, ST25x08C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W08C and ST25W08C
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES)
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES for "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGN: ST24/25C08C and ST24/25W08C



PSDIP8 (B)
0.25mm Frame

SO8 (M)

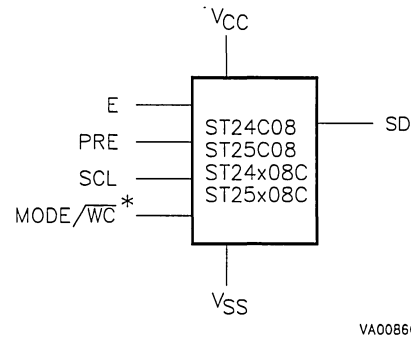
DESCRIPTION

This specification covers a range of 8K bits I^2C bus EEPROM products, the ST24/25C08, the ST24/25C08C and the ST24/25W08C. In the text,

Table 1. Signal Names

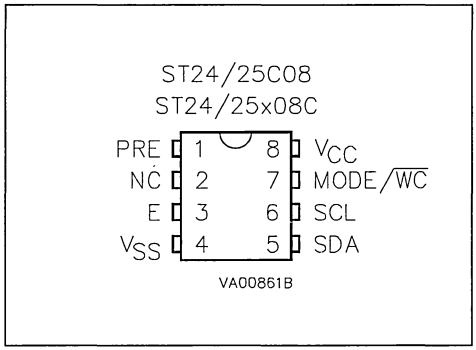
PRE	Write Protect Enable
E	Chip Enable Input
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



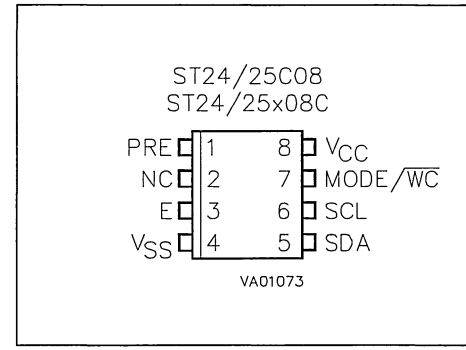
Note: $\overline{WC}$ signal is only available for ST24/25W08C products.

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage	ST24/25C08 ST24/25x08C		–0.3 to V_{CC} +0.6 –0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST24/25C08 ST24/25x08C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST24/25C08 ST24/25x08C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2 MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3 EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

products are referred to as ST24/25x08C, where "x" is: "C" for Standard version and "W" for Hardware Write Control version.

The ST24/25x08C are 8K bit electrically erasable programmable memories (EEPROM), organized as 4 blocks of 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 1 chip enable input (E) so that up to 2 x 8K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol

Table 3. Device Select Code

	Device Code				Chip Enable	Block Select		$\overline{RW}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E	A9	A8	$\overline{RW}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	$\overline{RW}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $\overline{RW}$ = '1'
Random Address Read	'0'	X		START, Device Select, $\overline{RW}$ = '0', Address
	'1'	X	1	reSTART, Device Select, $\overline{RW}$ = '1'
Sequential Read	'1'	X	1 to 1024	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, $\overline{RW}$ = '0'
Multibyte Write (2)	'0'	V_{IH}	8	START, Device Select, $\overline{RW}$ = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, $\overline{RW}$ = '0'

Notes: 1. X = V_{IH} or V_{IL}
2. Multibyte Write not available in ST24/25W08C versions.

Table 5. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST24C08, ST25C08	1,000,000	10
ST24C08C, ST25C08C ST24W08C, ST25W08C	1,000,000	10

with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

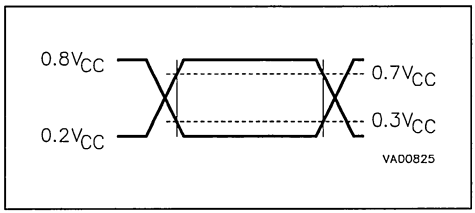
When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, ali operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 3. AC Testing Input Output Waveforms



SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 4).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 4).

Chip Enable (E). This chip enable input is used to set one least significant bit (b3) of the device select byte code. This input may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Protect Enable (PRE). The PRE input pin, in addition to the status of the Block Address Pointer bit (b2, location 3FFh as in Figure 7), sets the PRE write protection active.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as a V_{IH} (Multibyte Write mode).

Write Control ($\overline{WC}$). An hardware Write Control ($\overline{WC}$) feature is offered only for ST24W08C and ST25W08C versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. When unconnected the $\overline{WC}$ input is internally read as V_{IL}. The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

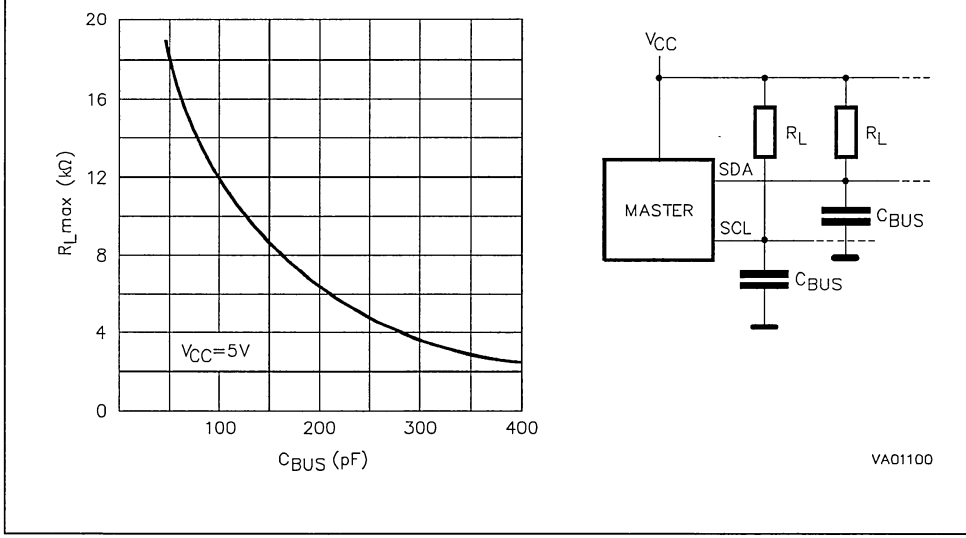


Table 6. Capacitance (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.7\ V_{CC}$	500		kΩ

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E, PRE, MODE, WC)		–0.3	0.5	V
V_{IH}	Input High Voltage (E, PRE, MODE, WC)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
V_{POR} (1)	Power On Reset Threshold (ST25 series)		1.5	2.4	V
V_{CC} Read (1)	V_{CC} Range for Read Operations (ST25 series)		2.5	5.5	V
V_{CC} Write	V_{CC} Range for Write Operations		2.5	5.5	V

Note: 1. At the time of publication of this data sheet, the statistical history, for the ST25x08C, was not yet sufficient to guarantee a V_{CC} Read = 2V. For the lastest information contact your local SGS-THOMSON Sales Office.

Table 8. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU.DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	T_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms.

DEVICE OPERATION

I²C Bus Background

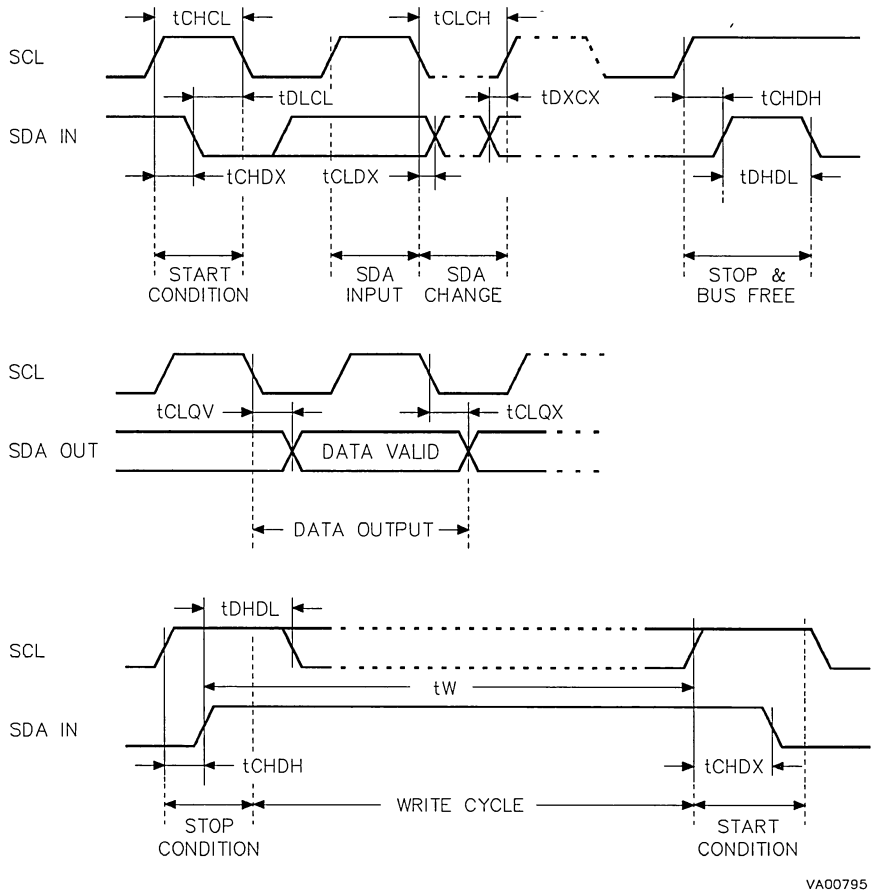
The ST24/25x08C support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x08C are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x08C continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x08C and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Figure 5. AC Waveforms



DEVICE OPERATION (cont'd)

Data Input. During data input the ST24/25x08C sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x08C, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following bit identifies the specific memory on the bus. It is matched to the chip enable signal E. Thus up to 2 x 8K memories can be connected on the same bus giving a memory capacity total of 16K bits. After a START condition any memory on the bus will identify the device code and compare the following bit to its chip enable input E.

The 6th and 7th bits sent, select the block number (one block = 256 bytes). The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Write Operations

The Multibyte Write mode (only available on the ST24/25C08 and ST24/25C08C versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The memory acknowledges this and waits for a byte

Figure 6. I^2C Bus Protocol

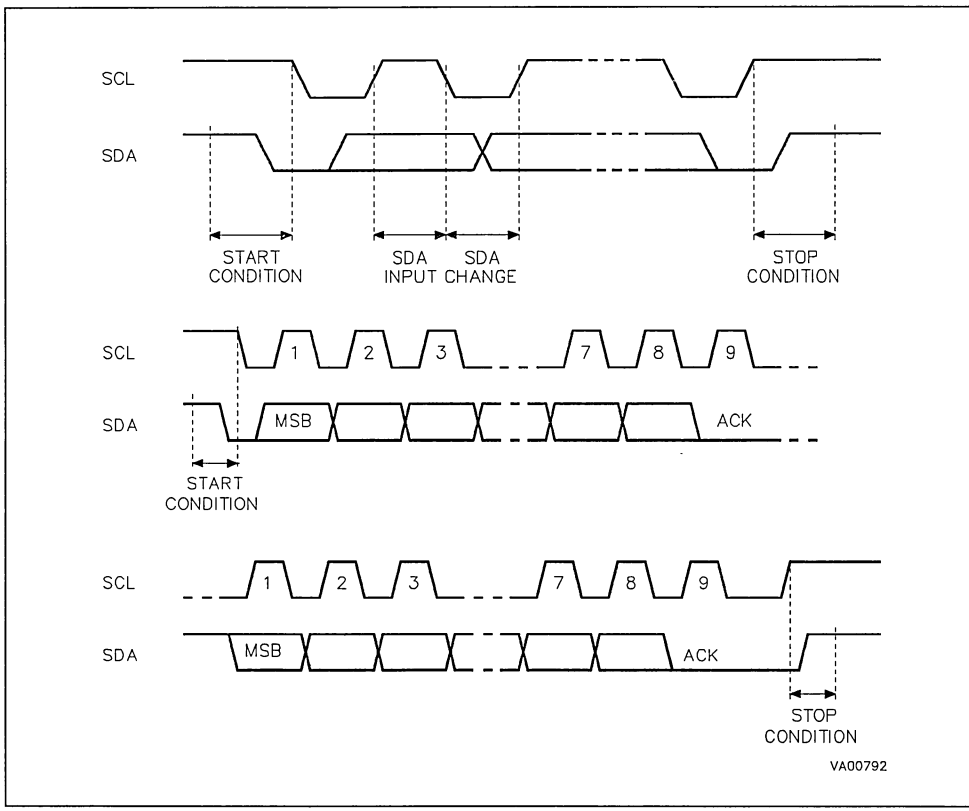
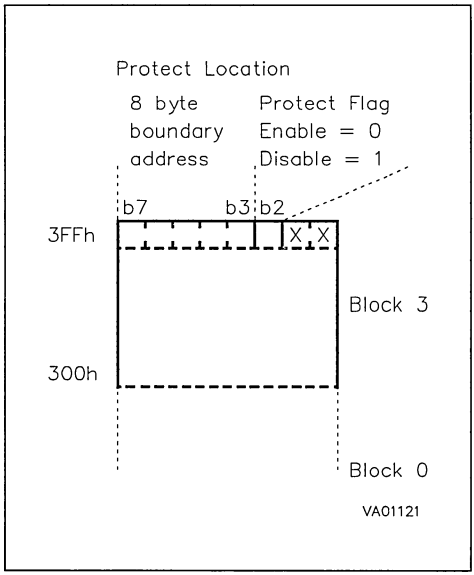


Figure 7. Memory Protection



address. The byte address of 8 bits provides access to one block of 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W08C versions, any write command with $\overline{WC}$ = 1 will not modify the memory content.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the standby current.

Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 5 most significant address bits A7-A3), the programming time is then doubled to a maximum of 20ms. Writing more than 8 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 16 bytes long). However, the Multibyte Write can properly write up to 16 consecutive bytes only if the first address of these 16 bytes is the first address of the row, the 15 following bytes being written in the 15 following bytes of this same row.

Page Write. For the Page Write mode the MODE pin must be at V_{IL}. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 4 most significant memory address bits (A7-A4) are the same inside one block. The master sends from one up to 16 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 8).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Write Protection. Data in the upper block of 256 bytes of the memory may be write protected. The memory is write protected between a boundary address and the top of memory (address 3FFh) when the PRE input pin is taken high and when the Protect Flag (bit b2 in location 3FFh) is set to '0'. The boundary address is user defined by writing a value in the Block Address Pointer (location 3FFh).

This Block Address Pointer defines an 8 bit address composed of the 5 MSBs of location 3FFh and 3

DEVICE OPERATION (cont'd)

LSBs which are read as '0'. This address pointer can therefore address a boundary in steps of 8 bytes.

The sequence to follow to use the Write Protected feature is:

- write the data to be protected into the top of the memory, up to, but not including, location 3FFh;
- set the protection by writing the correct bottom boundary address, into location 3FFh, with bit b2 (Protect flag) set to '0'.

The area will now be protected when the PRE input is taken High.

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input pin High). If the Multibyte Write starts at the location right below the first byte of the Write Protected area, then the instruction will write over the first 7 bytes of the Write Protected area. The area protected is therefore smaller than the content defined in the location 3FFh, by 7 bytes. This does not apply to the Page Write mode as the address counter 'roll-over' and thus cannot go above the 16 bytes lower boundary of the protected area.

Figure 8. Write Cycle Polling using ACK

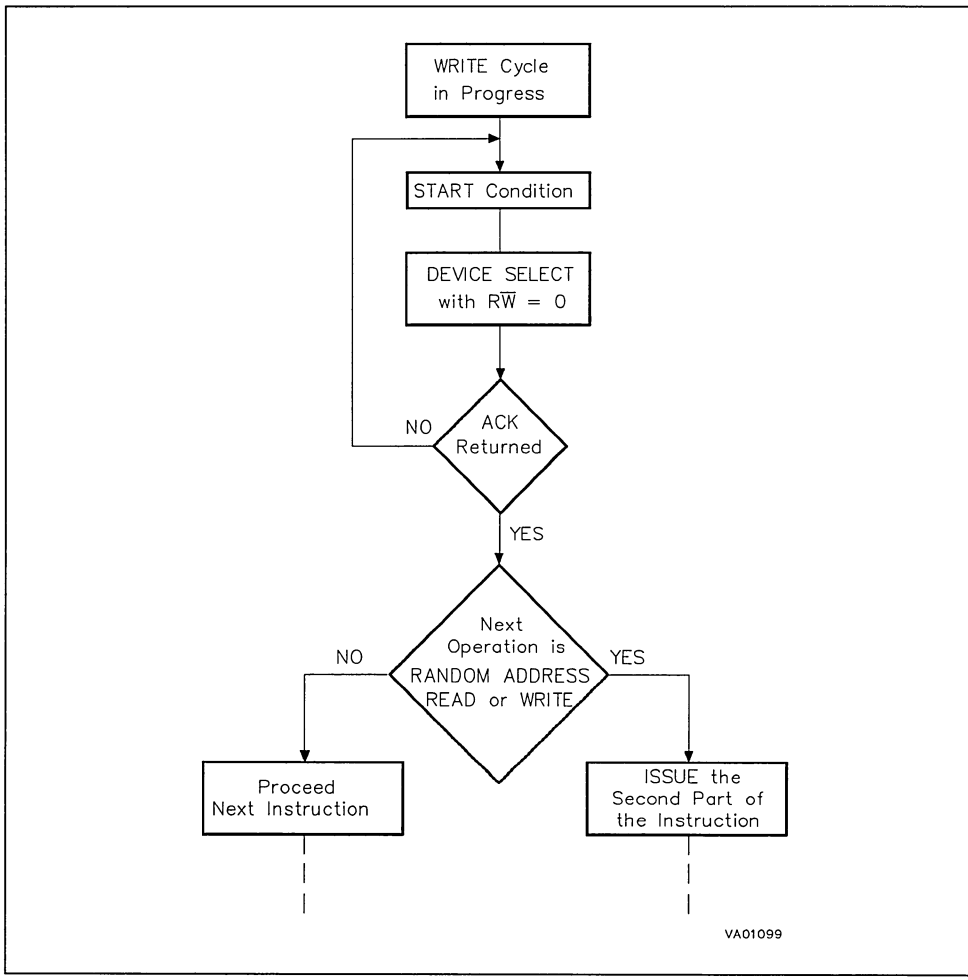


Figure 9. Write Modes Sequence (ST24/25C08, ST24/25C08C)

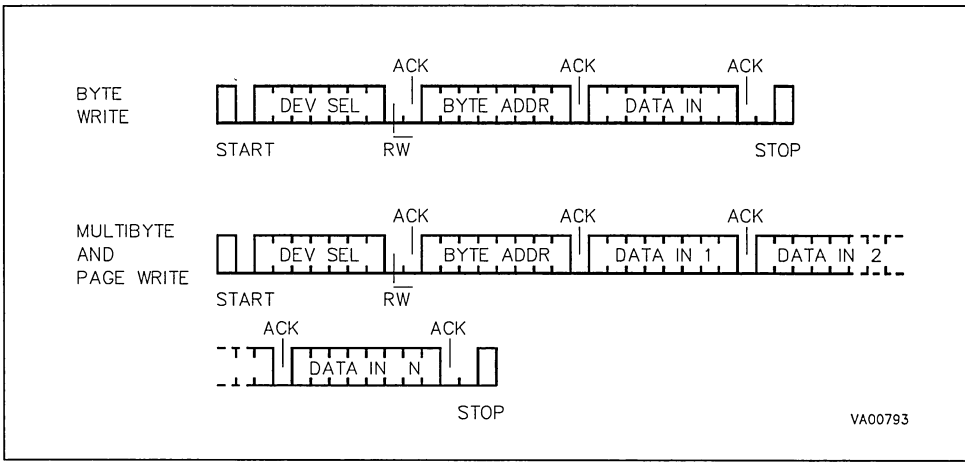
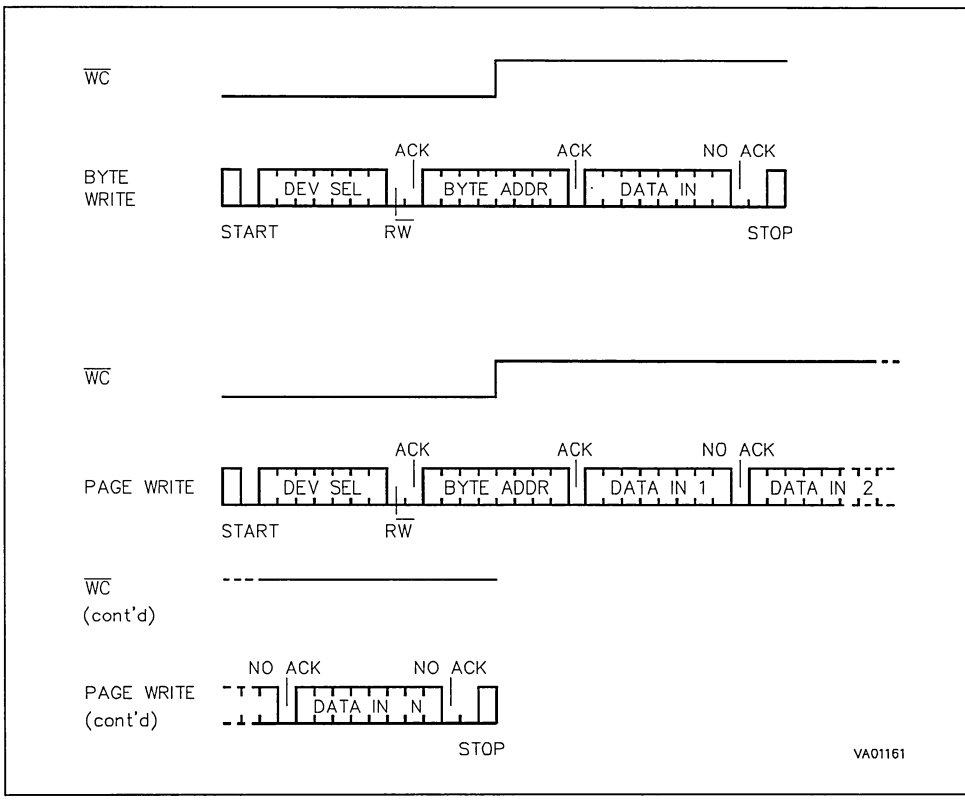


Figure 10. Write Modes Sequence with Write Control = 1 (ST24/25W08C)



Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

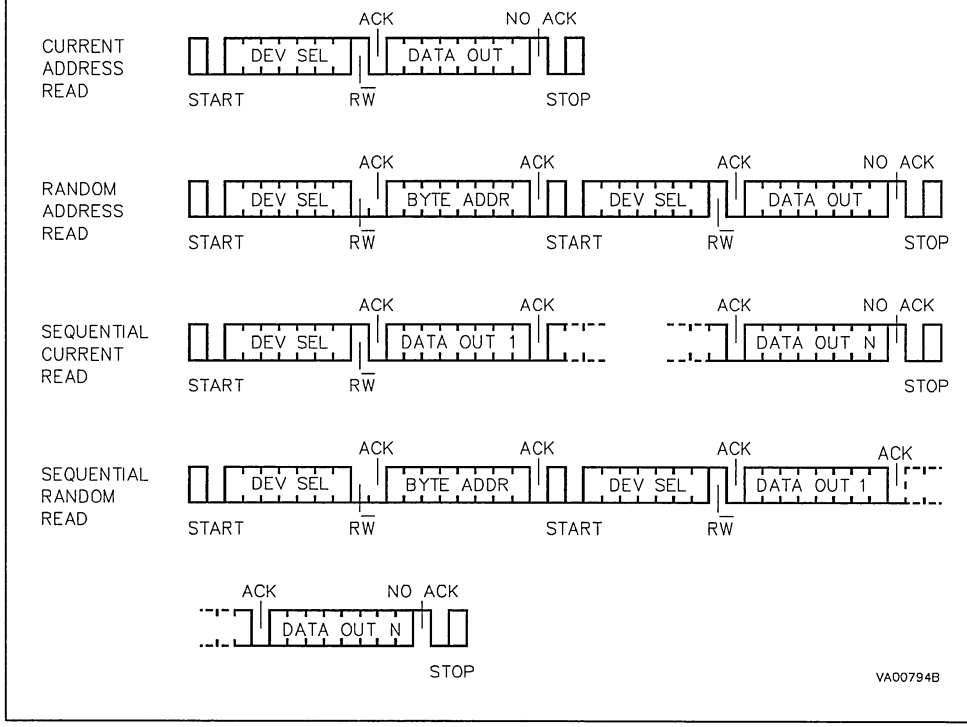
Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter (see Figure 11). This is followed by another START condition from the master and the byte address is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

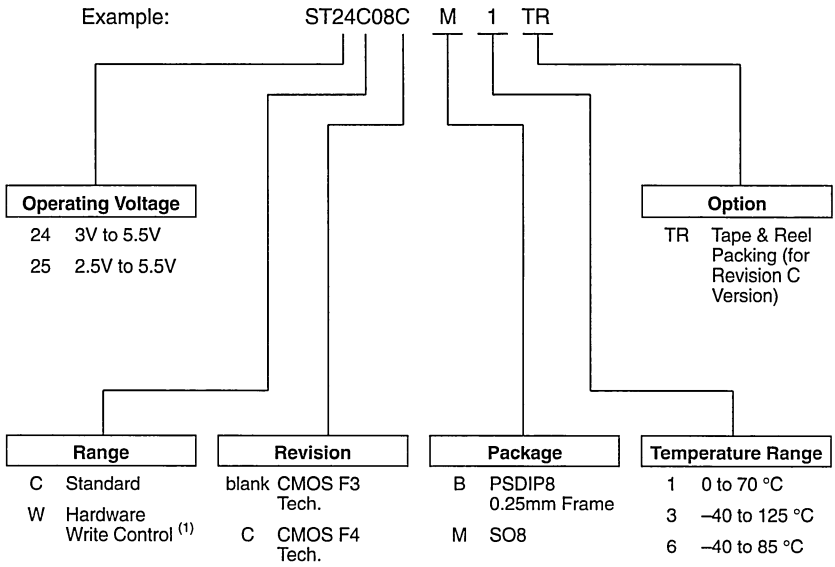
Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25x08C wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x08C terminate the data transfer and switches to a standby state.

Figure 11. Read Modes Sequence



ORDERING INFORMATION SCHEME



Note: 1. At the time of publication of this document the "W" type was not available for the lastest information. Please contact your local SGS-THOMSON sales office.

Parts are shipped with the memory content set at all "1's" (FFh).

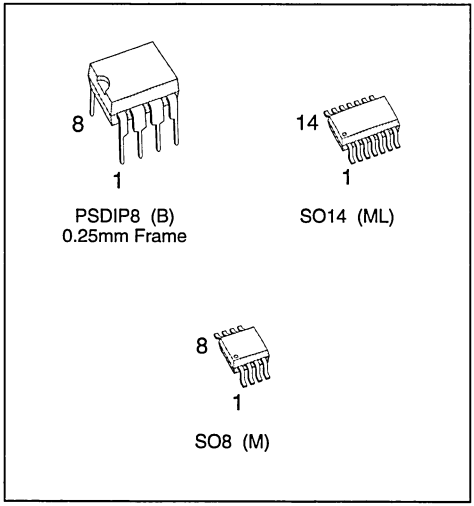
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

ST24C16, ST25C16 ST24W16, ST25W16

SERIAL ACCESS CMOS 16K (2048 x 8) EEPROMs

- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x16 versions
  - 2.5V to 5.5V for ST25x16 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W16 and ST25W16
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES)
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



DESCRIPTION

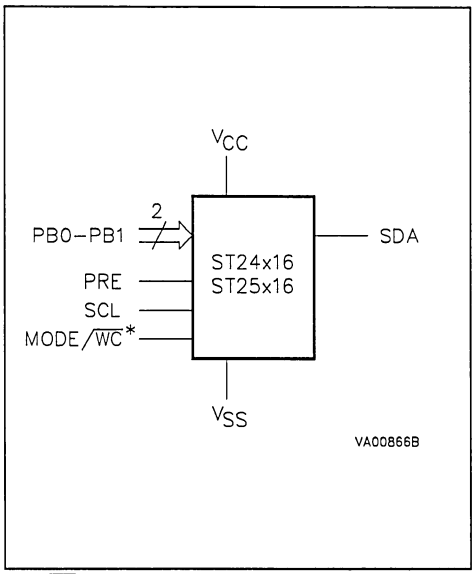
This specification covers a range of 16K bits I^2C bus EEPROM products, the ST24/25C16 and the ST24/25W16. In the text, products are referred to as ST24/25x16 where "x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x16 are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x 8 bits. These are manufactured

Table 1. Signal Names

PRE	Write Protect Enable
PB0, PB1	Protect Block Select
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multybyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W16 products.

Figure 2A. DIP Pin Connections

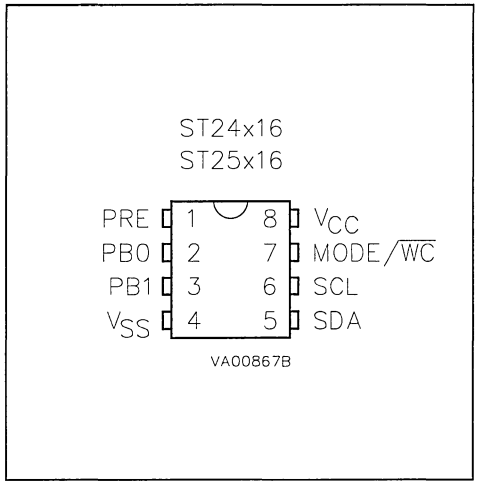
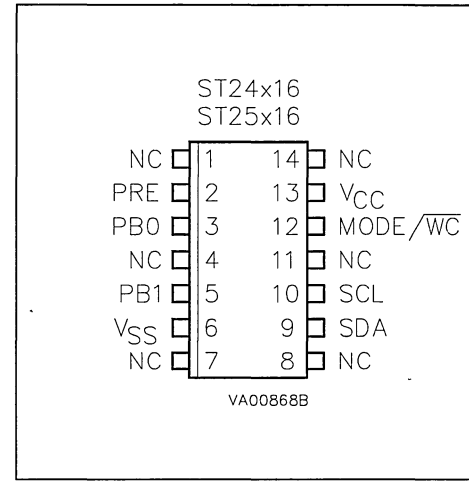
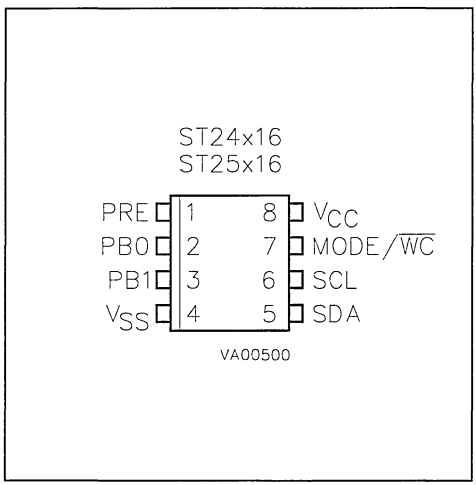


Figure 2B. SO14 Pin Connections



Warning: NC = No Connection

Figure 2C. SO8 Pin Connections



DESCRIPTION (cont'd)

in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The ST25x16 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The memories behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the 4 upper blocks of the memory may be write protected. The protected area is programmable to start on any 16 byte boundary. The block in which the protection starts is selected by the input pins PB0, PB1. Protection is enabled by setting a Protect Flag bit when the PRE input pin is driven High.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 and SO14) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

Table 3. Device Select Code

	Device Code				Memory MSB Addresses			$\overline{RW}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	A10	A9	A8	$\overline{RW}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	$\overline{RW}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $\overline{RW}$ = '1'
Random Address Read	'0'	X		START, Device Select, $\overline{RW}$ = '0', Address
	'1'	X	1	reSTART, Device Select, $\overline{RW}$ = '1'
Sequential Read	'1'	X	1 to 2048	As CURRENT or RANDOM Mode
Byte Write	'0'	X	1	START, Device Select, $\overline{RW}$ = '0'
Multibyte Write	'0'	V_{IH}	8	START, Device Select, $\overline{RW}$ = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, $\overline{RW}$ = '0'

Note: X = V_{IH} or V_{IL}.

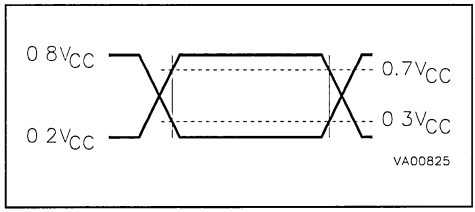
Table 5. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST24C16, ST25C16 ST24W16, ST25W16	1,000,000	10

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 3. AC Testing Input Output Waveforms



DESCRIPTION (cont'd)

and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input signal is used to synchronise all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 4).

Serial Data (SDA). The SDA signal is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 4).

Protected Block Select (PB0, PB1). PB0 and PB1 input signals select the block in the upper part of the memory where write protection starts. These inputs have a CMOS compatible input level.

Protect Enable (PRE). The PRE input signal, in addition to the status of the Block Address Pointer bit (b2, location 7FFh as in Figure 7), sets the PRE write protection active.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as V_{IH} (Multibyte Write mode).

Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

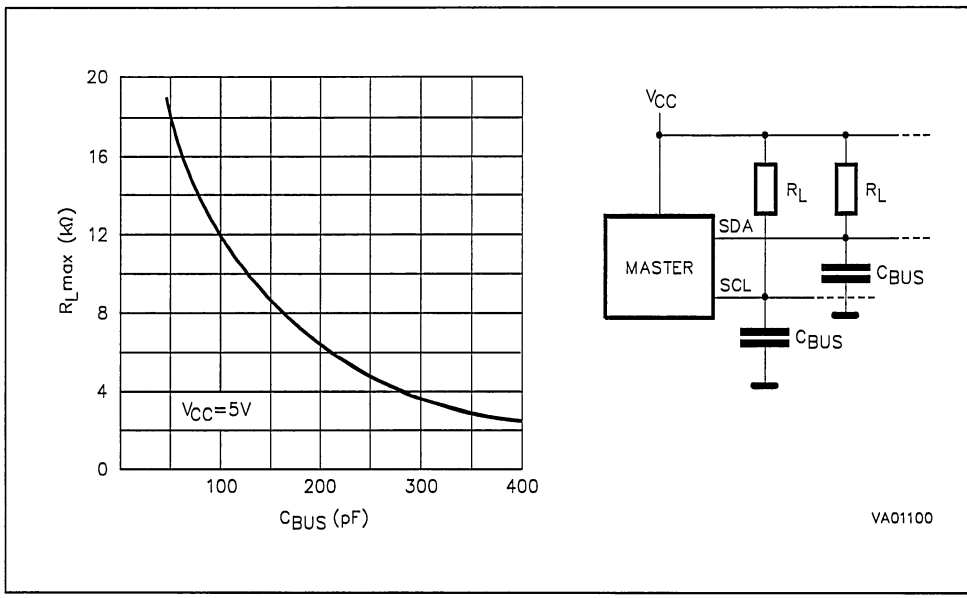


Table 6. Capacitance (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ

Note: 1. Sampled only, not 100% tested.

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		100	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		5	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (PB0 - PB1, PRE, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (PB0 - PB1, PRE, MODE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
V_{POR} (1)	Power On Reset Threshold (ST25 series)		1.5	2.4	V
V_{CC} Read (1)	V_{CC} Range for Read Operations (ST25 series)		2.5	5.5	V
V_{CC} Write	V_{CC} Range for Write Operations		2.5	5.5	V

Note: 1. At the time of publication of this data sheet, the statistical history, for the ST25x16, was not yet sufficient to guarantee a V_{CC} Read = 2V. For the lastest information contact your local SGS-THOMSON Sales Office.

Table 8. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	t_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (5 address MSB are not constant) the maximum programming time is doubled to 20ms.

SIGNAL DESCRIPTIONS (cont'd)

Write Control (WC). An hardware Write Control feature is offered only for ST24W16 and ST25W16 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH}) or disable ($\overline{WC}$ at V_{IL}) the internal write protection. When unconnected, the $\overline{WC}$ input is internally read as V_{IL}. The devices with this Write Control feature no longer supports the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

DEVICE OPERATION

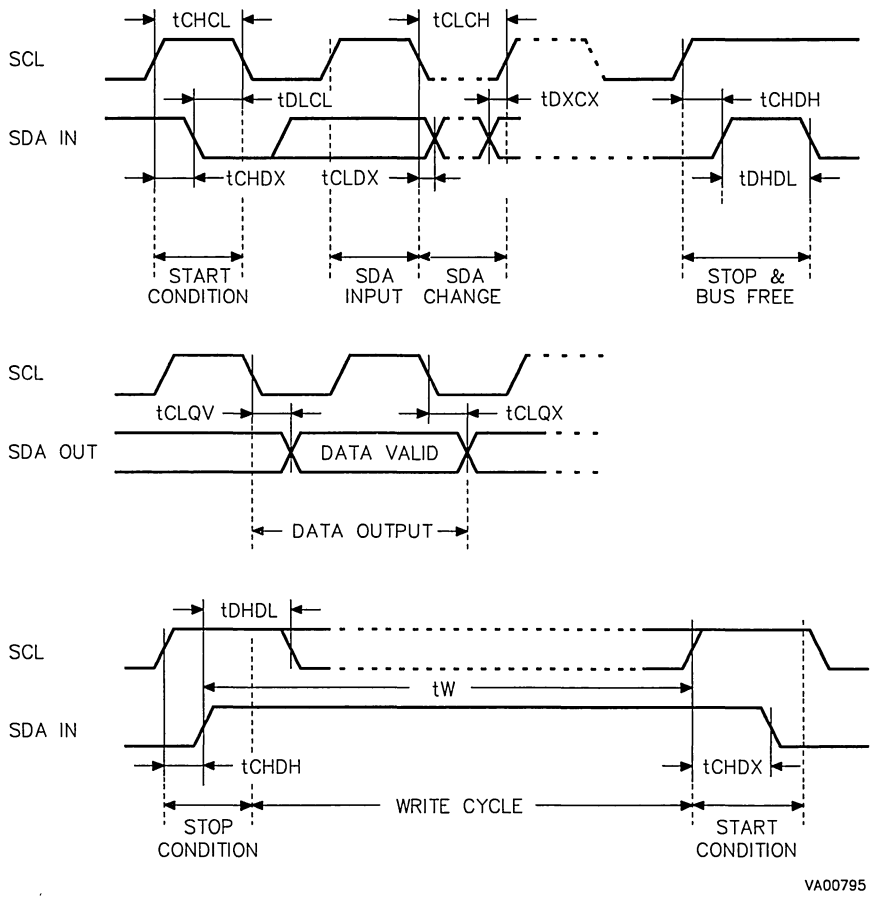
I²C Bus Background

The ST24/25x16 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x16 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x16 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x16 and the bus master. A STOP condition at the end of a Read command forces the standby state. A

Figure 5. AC Waveforms



DEVICE OPERATION (cont'd)

STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x16 samples the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x16, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifie the device type (1010), 3 Block select bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Write Operations

The Multibyte Write mode (only available on the ST24/25C16 versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides ac-

Figure 6. I^2C Bus Protocol

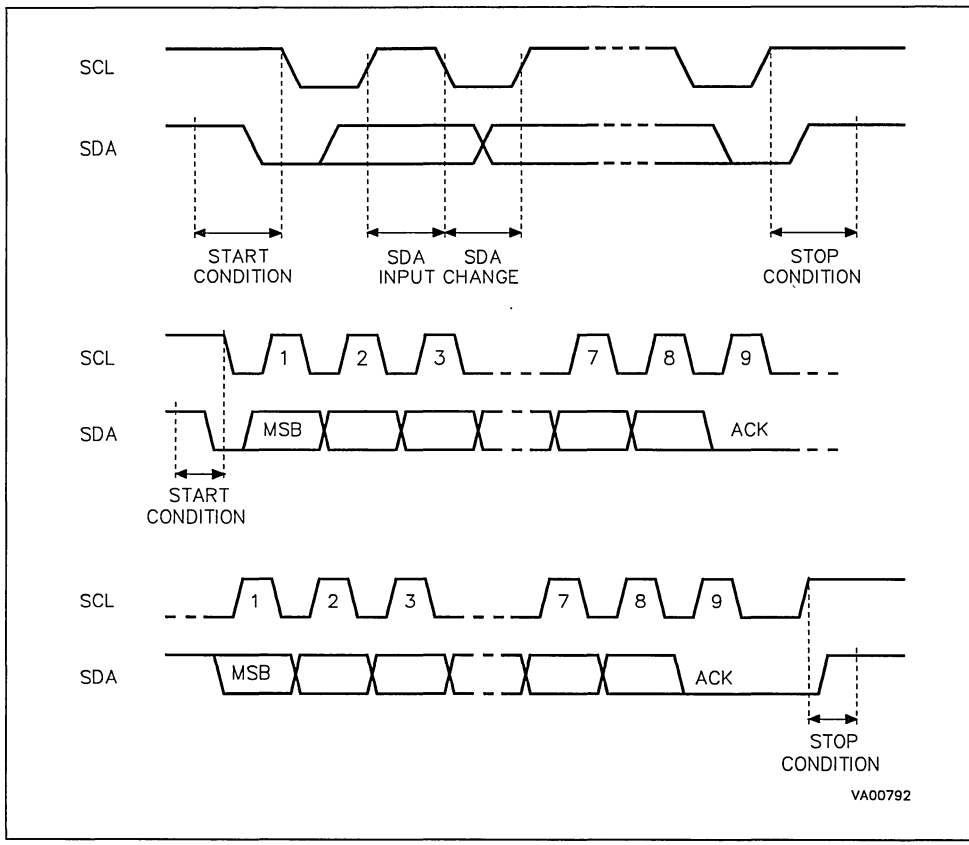
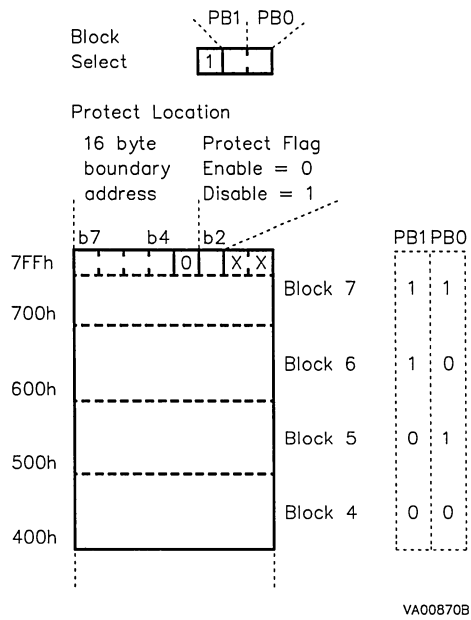


Figure 7. Memory Protection



cess to any of the 256 bytes of one memory block. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W16 versions, any write command with $\overline{WC}$ = 1 (during a period of time from the START condition untill the end of the Byte Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 10.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 contiguous rows (one row is 16 bytes), the programming time is then doubled to a maximum of 20ms. Writing more than 8 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 16 bytes long). However, the Multibyte Write can properly write up to 16 consecutive bytes only if the first address of these 16 bytes is the first address of the row, the 15 following bytes being written in the 15 following bytes of this same row.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the same Block Address bits (b3, b2, b1 of Device Select code in Table 3) and the same 4 MSBs in the Byte Address. The master sends one up to 16 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (4

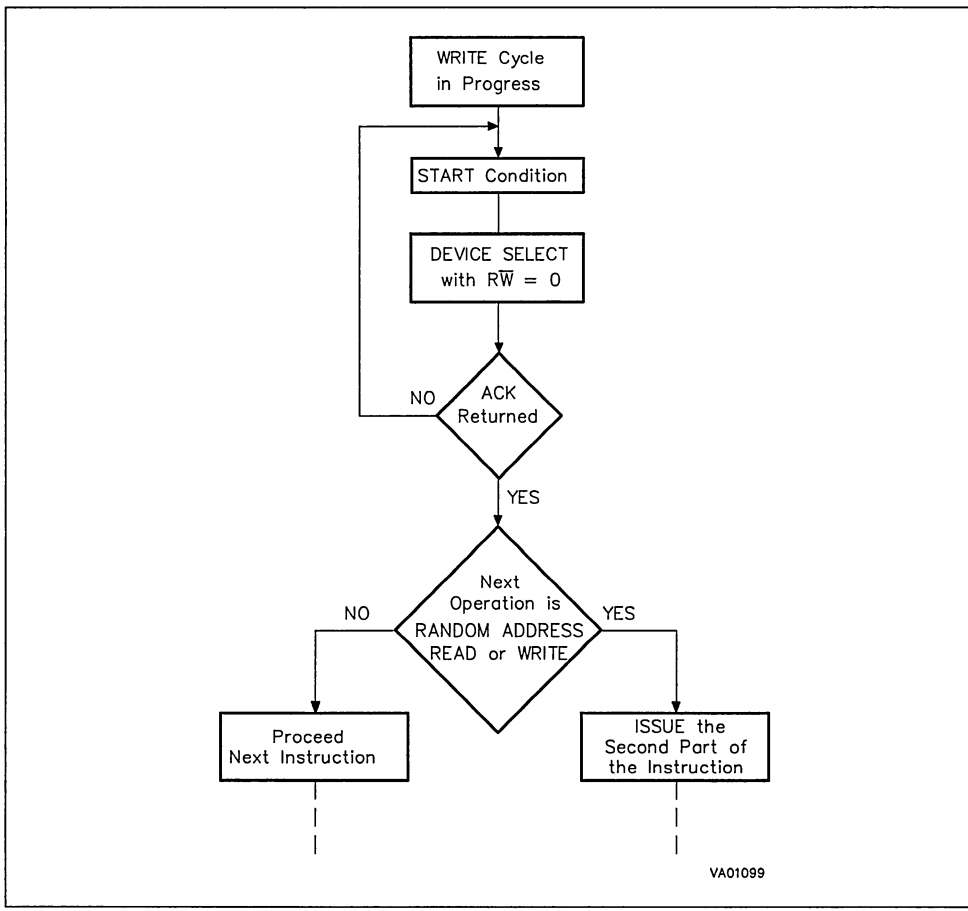
DEVICE OPERATION (cont'd)

Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master. The sequence is:

- Initial condition: a Write is in progress (see Figure 8).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is internally writing, no ACK will be returned. The Master goes back to Step1. If the memory has terminated the internal writing, it will issue an ACK indicating that the memory is ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step 1).

Figure 8. Write Cycle Polling using ACK



Write Protection. Data in the upper four blocks of 256 bytes of the memory may be write protected. The memory is write protected between a boundary address and the top of memory (address 7FFh). The boundary address is user defined by writing a value in the Block Address Pointer (location 7FFh).

This Block Address Pointer defines an 8 bit address composed of the 4 MSBs of location 7FFh and 4 LSBs which are forced to '0'. This address pointer can therefore address a boundary in steps of 16 bytes.

The block in which the Block Address Pointer defines the boundary of the write protected memory is defined by the logic level on the PB1 and PB0 inputs:

- PB1 = '0' and PB0 = '0' select block 4
- PB1 = '0' and PB0 = '1' select block 5
- PB1 = '1' and PB0 = '0' select block 6
- PB1 = '1' and PB0 = '1' select block 7

To use the Write Protected feature follow this sequence:

- write the data to be protected into the top of the memory, up to, but not including, location 7FFh;
- select the block by hardwiring the signals PB0 & PB1;
- and set the protection by writing the correct bottom boundary address into location 7FFh.

The area will now be protected when the PRE input is taken High.

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input pin High). If the Multibyte Write starts at the location right below the first byte of the Write Protected area, then the instruction will write over the first 7 bytes of the Write Protected area. The area protected is therefore smaller than the content defined in the location 7FFh, by 7 bytes. This does not apply to the Page Write mode as the address counter 'roll-over' and thus cannot go above the 16 bytes lower boundary of the protected area.

Read Operation

Read operations are independent of the state of the MODE signal. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter (see Figure 11). This is followed by another START condition from the master and the byte address repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the

Figure 9. Write Modes Sequence (ST24/25C16)

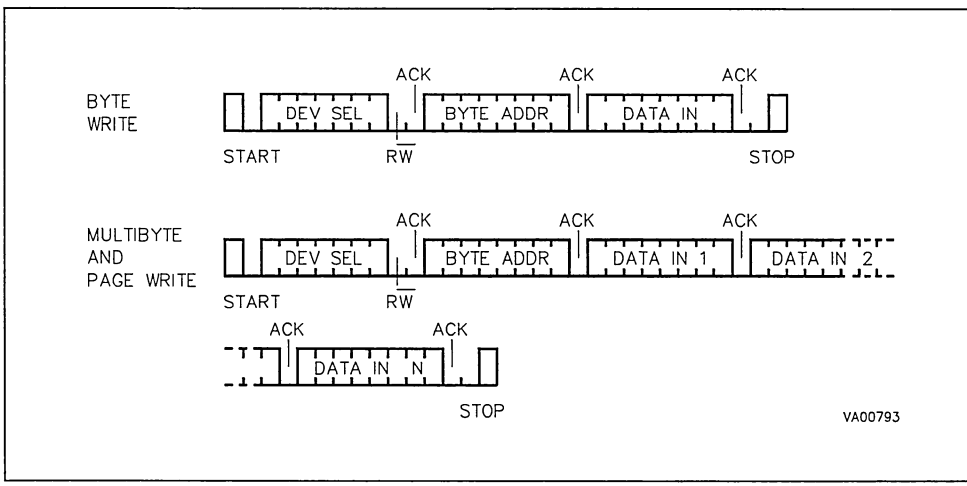
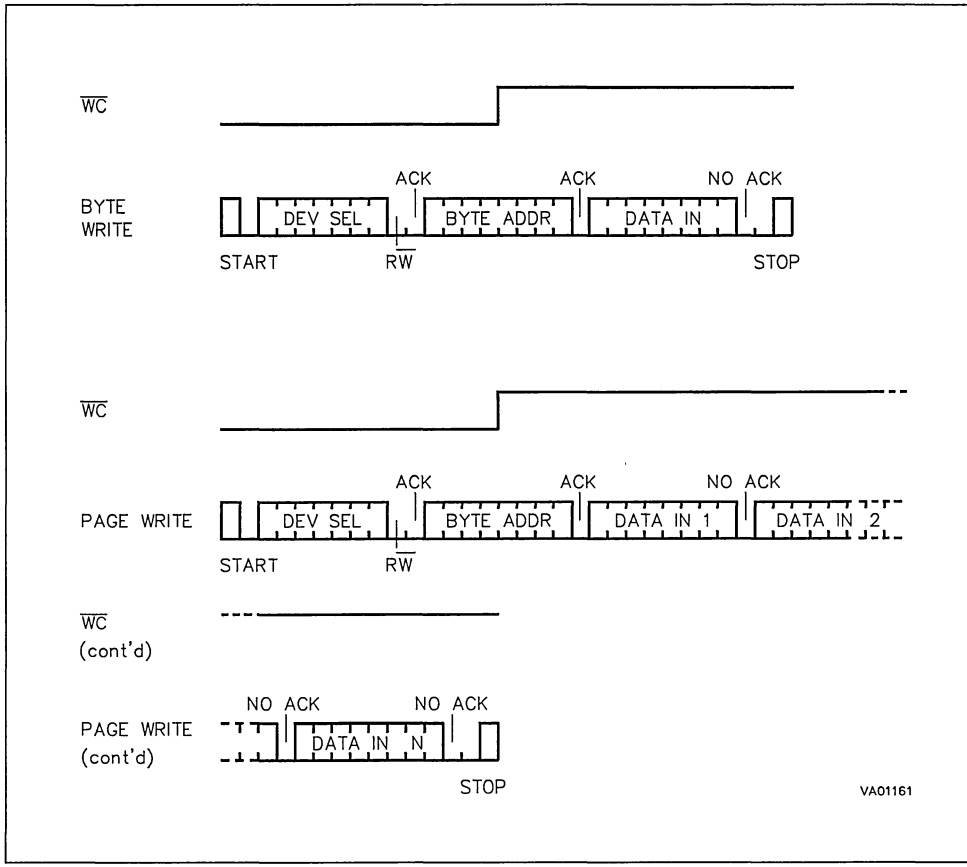


Figure 10. Write Modes Sequence with Write Control = 1 (ST24/25W16)



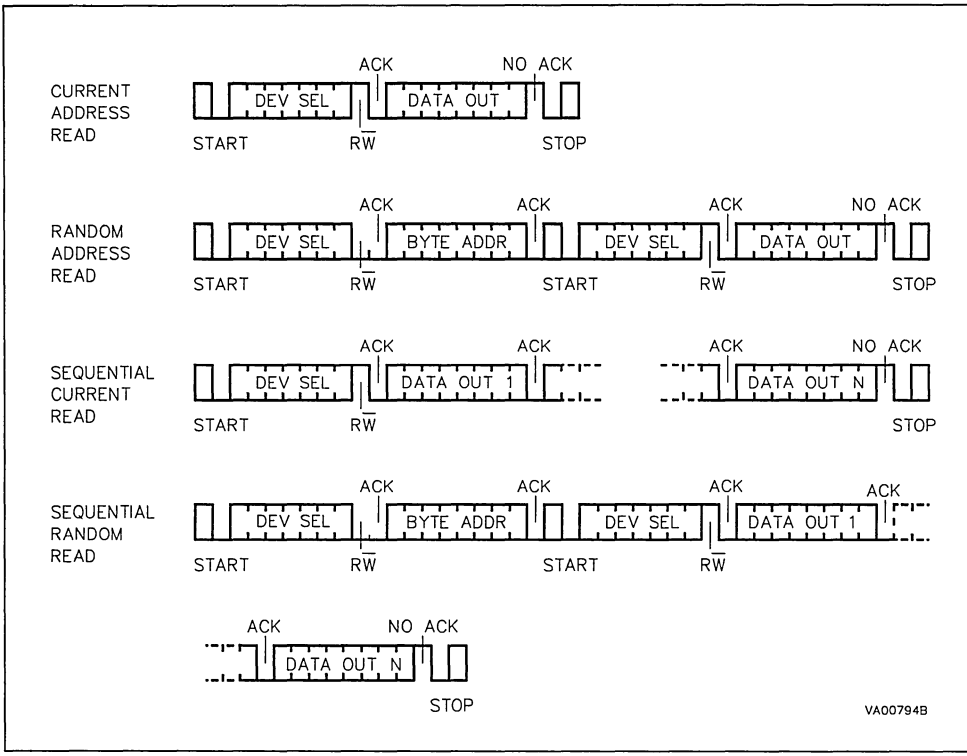
DEVICE OPERATION (cont'd)

byte output, but terminates the transfer with a STOP condition.

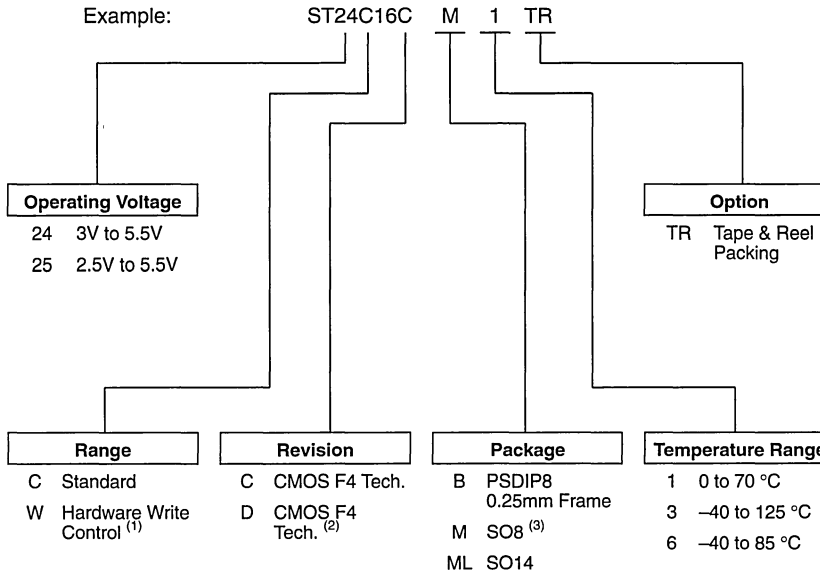
Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25x16 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x16 terminate the data transfer and switches to a standby state.

Figure 11. Read Modes Sequence



ORDERING INFORMATION SCHEME



Notes: 1. Available on Revision D only.
2. Revision D is an upgrade of Revision C with optimized chip lay-out fits SO8 package.
3. Available only for Revision D devices.

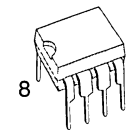
Parts are shipped with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Range, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SERIAL ACCESS CMOS 16K (2048 x 8) EEPROMs

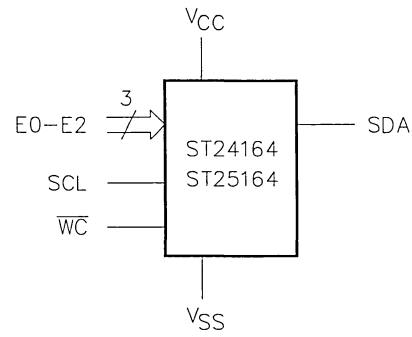
- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24164 version
  - 2.5V to 5.5V for ST25164 version
- HARDWARE WRITE CONTROL PIN
- TWO WIRE SERIAL INTERFACE
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST24/25164 are 16K bit electrically erasable programmable memories (EEPROM), organized as 2048 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V.

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

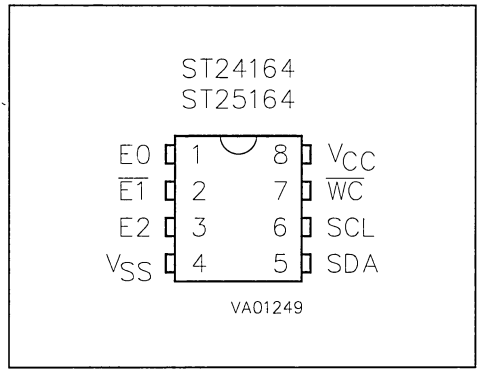


Figure 2B. SO Pin Connections

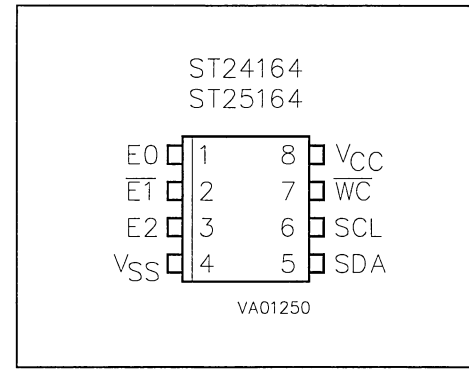


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 3 grade 6	–40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the two wire serial interface which uses a bi-directional data bus and serial clock. The memories offer 3 chip enable inputs (E2, $\overline{E1}$, E0) so that up to 8 x 16K devices may be attached to the bus and selected individually. The memories behave as a slave device with all memory operations synchronized by the serial clock.

Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits, plus one read/write bit and terminated by an acknowledge bit (see Table 3).

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Table 3. Device Select Code

		Chip Enable			MSB Address			R/$\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	E2	E1	E0	A10	A9	A8	R/$\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	R$\overline{W}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, R/$\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, R/$\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, R/$\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 2048	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, R/$\overline{W}$ = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, R/$\overline{W}$ = '0'

Notes: 1. X = V_{IH} or V_{IL}

Table 5. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST24164, ST25164	1,000,000	10

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

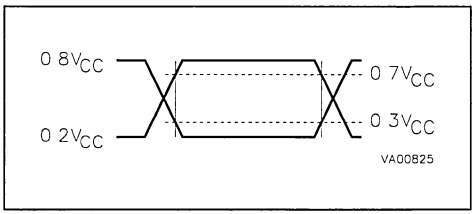
Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 4).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 4).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 3. AC Testing Input Output Waveforms



Chip Enable (E2 - E0). These chip enable inputs are used to set 3 bits (b6, b5, b4) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. $\overline{WC}$ pin can be direcly connected to V_{SS} pin, in order to run the ST24/25164 without the Write Control protection.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

DEVICE OPERATION

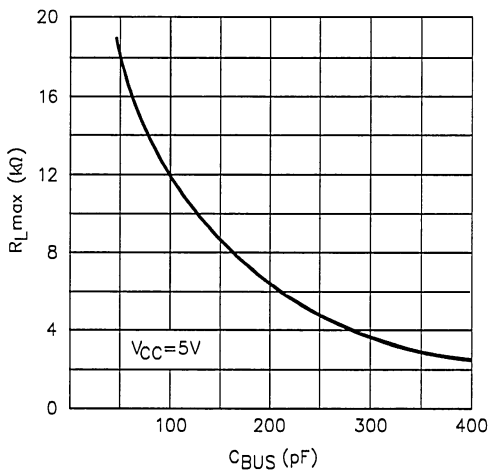
Bus Background

The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25164 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25164 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25164

Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for a Serial Bus



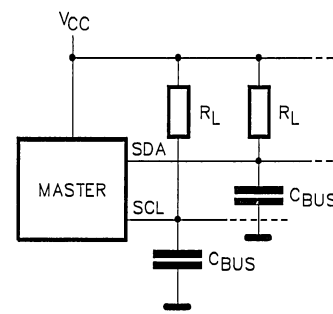


Table 6. Capacitance (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		100	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		5	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, WC)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, WC)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
V_{POR} (1)	Power On Reset Threshold (ST25 series)		1.5	2.0	V
V_{CC} Read (1)	V_{CC} Range for Read Operations (ST25 series)		2.5	5.5	V
V_{CC} Write	V_{CC} Range for Write Operations		2.5	5.5	V

Note: 1. At the time of publication of this data sheet, the statistical history, for the ST25164, was not yet sufficient to guarantee a V_{CC} Read = 2V. For the lastest information contact your local SGS-THOMSON Sales Office.

Table 8. AC Characteristics
(T_A = –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU.DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	T_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W	t_{WR}	Write Time		10	ms

Note: 1. For a reSTART condition, or following a write cycle.

DEVICE OPERATION (cont'd)

and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

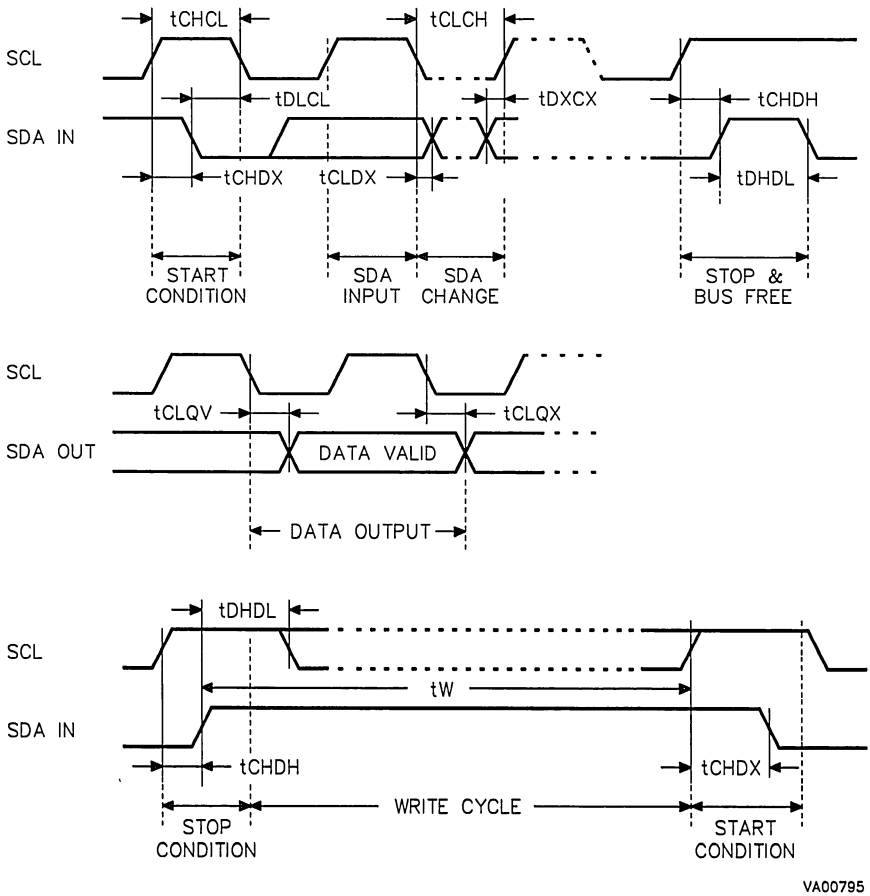
Data Input. During data input the ST24/25164 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25164, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a Read or Write bit (R/$\overline{W}$).

Three out of the four most significant bits of the Device Select code are the Device Select bits (b6, b5, b4). They are matched to the chip enable signals applied on pins E2, $\overline{E1}$, E0. Thus up to 8 x 16K memories can be connected on the same bus giving a memory capacity total of 128K bits. After a START condition any memory on the bus will identify the device code and compare the 3 bits to its chip enable inputs E2, $\overline{E1}$, E0.

The 8th bit sent is the Read or Write bit (R/$\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Figure 5. AC Waveforms



DEVICE OPERATION (cont'd)

Write Operations

The Write Operations is only possible when the Write Control pin is low ($\overline{WC}$ to ground).

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for the lower byte address. After receipt of the byte address the device again responds with an acknowledge.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 4 most significant Byte Address bits (A7-A4) are the same. The master sends from one up to 16 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is

Figure 6. I^2C Bus Protocol

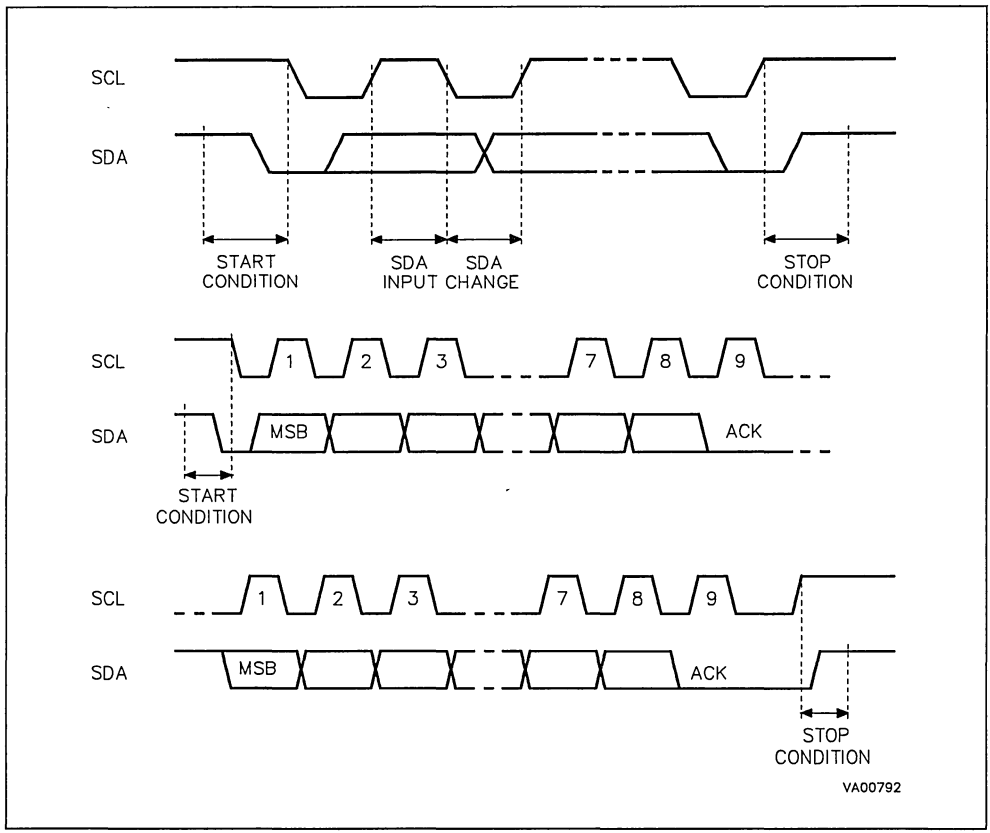
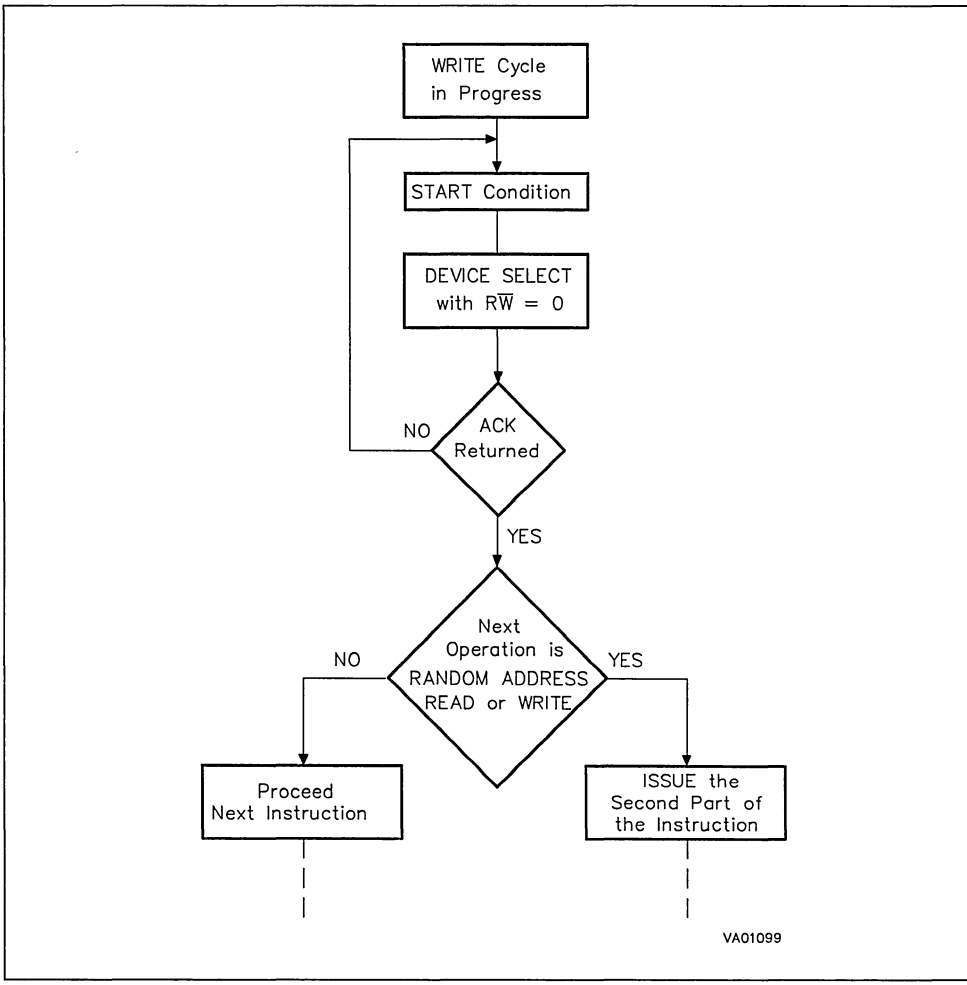


Figure 7. Write Cycle Polling using ACK



shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the master issues a START condition followed by a device select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Read Operations

Read operations are independent of the state of the $\overline{WC}$ pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read,

Figure 8. Write Modes Sequence

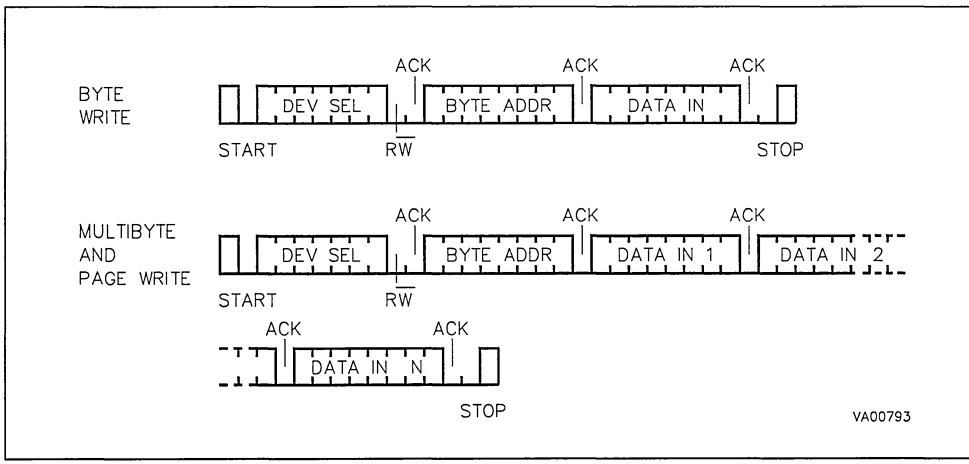


Figure 9. Write Modes Sequence with Write Control = 1

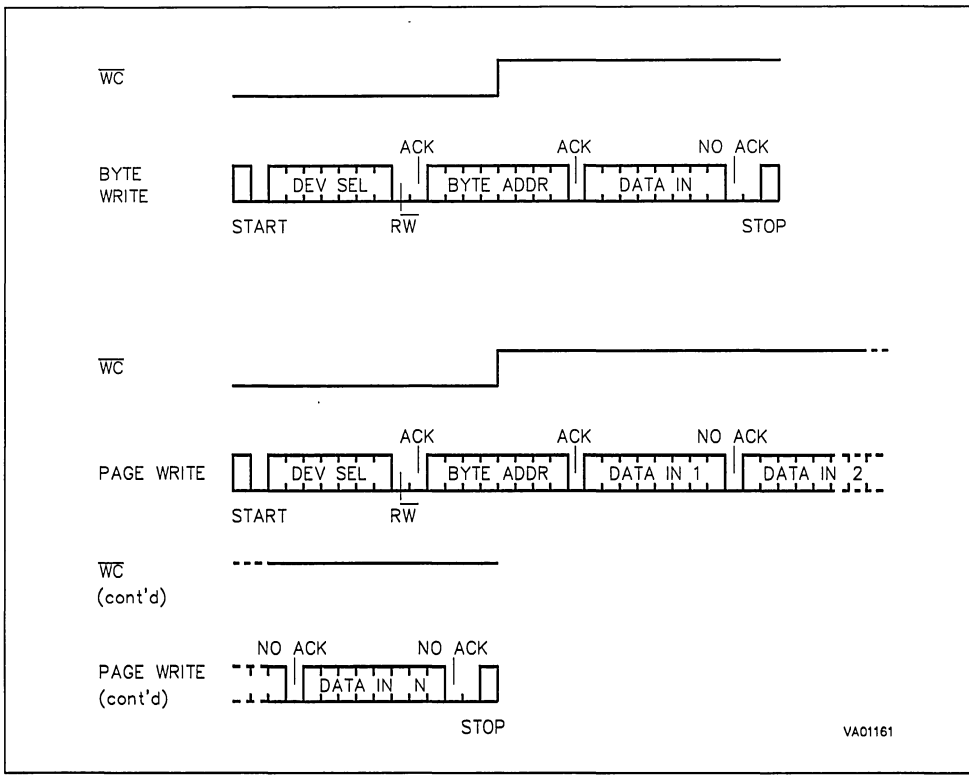
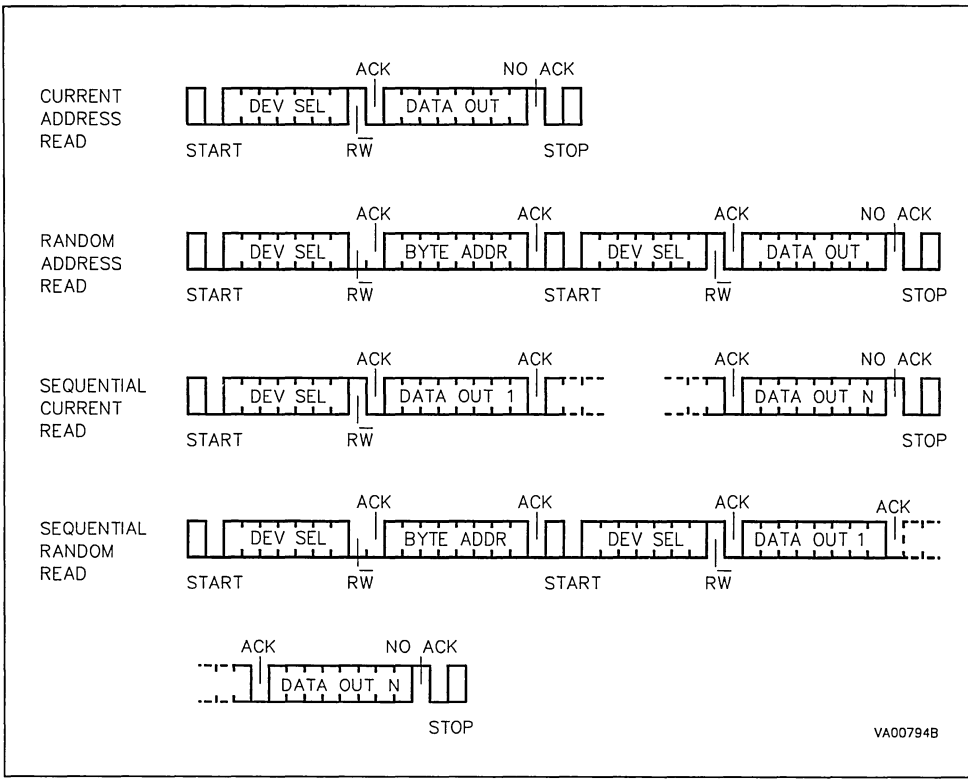


Figure 10. Read Modes Sequence



DEVICE OPERATION (cont'd)

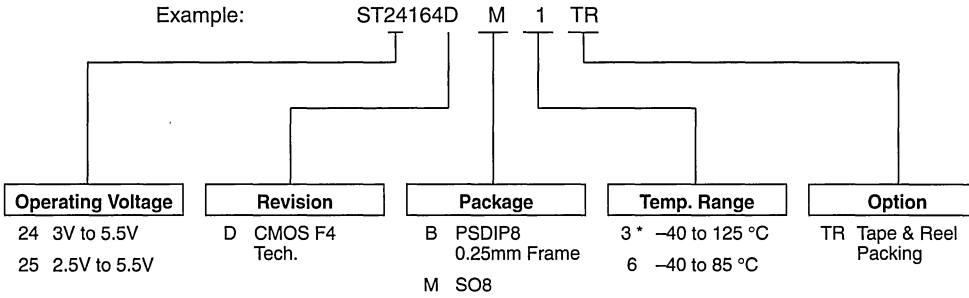
this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R/$\overline{W}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address is repeated with the R/$\overline{W}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25164 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25164 terminate the data transfer and switches to a standby state.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on request only.

Parts are shipped with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

XI^{2}C BUS EEPROM

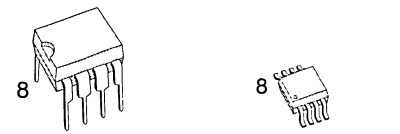
SGS-THOMSON MICROELECTRONICS

ST24E16D
ST25E16D

SERIAL ACCESS CMOS 16K (2048 x 8) EEPROMs EXTENDED ADDRESSING COMPATIBLE WITH I²C BUS

PRODUCT CONCEPT

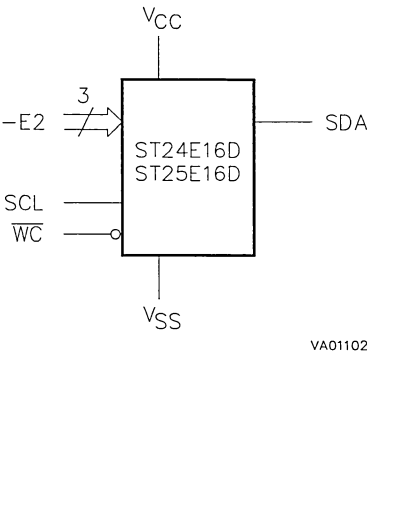
- COMPATIBLE with I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24E16D version
  - 2V to 5.5V for ST25E16D version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST24/25E16D are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The ST25E16D operates with a power supply value as

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

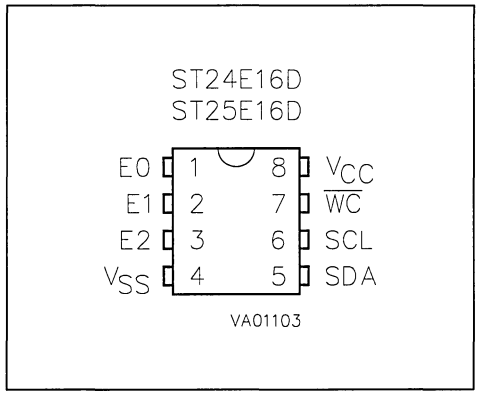


Figure 2B. SO Pin Connections

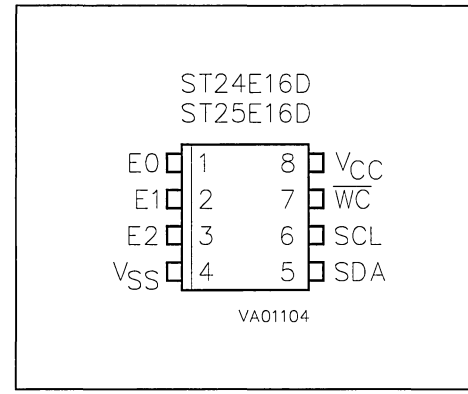


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

low as 2.0V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E16D carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E16D behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknow-

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	RW bit	Bytes	Initial Sequence
Current Address Read	'1'	1	START, Device Select, RW = '1'
Random Address Read	'0'		START, Device Select, RW = '0', Address
	'1'	1	reSTART, Device Select, RW = '1'
Sequential Read	'1'	1 to 2048	As CURRENT or RANDOM Mode
Byte Write	'0'	1	START, Device Select, RW = '0'
Page Write	'0'	16	START, Device Select, RW = '0'

Note: X = V_{IH} or V_{IL}.

ledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way.

Data transfers are terminated with a STOP condition. In this way, up to 8 ST24/25E16D may be connected to the same I^2C bus and selected individually, allowing a total addressing field of 128 Kbit.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3)

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL compatible.

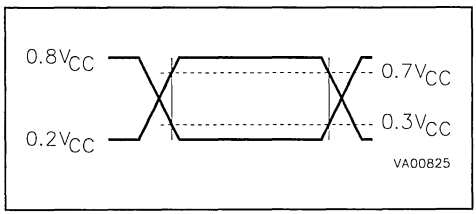
Write Control ($\overline{WC}$). The Write Control feature $\overline{WC}$ is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH}) or disable ($\overline{WC}$ at V_{IL}) the internal write protection. The devices with this Write Control feature no longer supports the multibyte mode of operation. When unconnected, the $\overline{WC}$ input is internally read as V_{IL}.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION

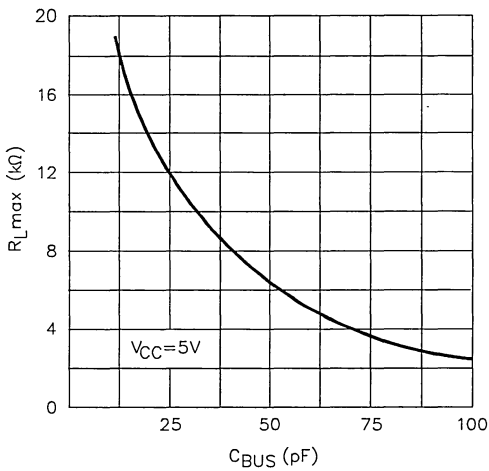
I²C Bus Background

The ST24/25E16D support the extended addressing I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25E16D are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25E16D continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25E16D and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus, f_C = 400kHz



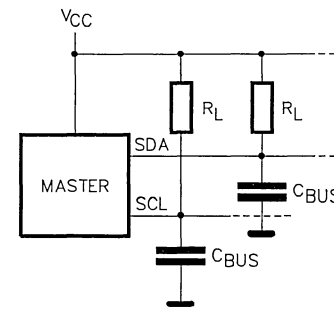


Table 5. Capacitance (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter		Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
R_{IN}	$\overline{WC}$ Input Resistor	$0V \leq V_{IN} \leq 0.3V_{CC}$	8	25	kΩ
		$0.7\ V_{CC} \leq V_{IN} \leq V_{CC}$	1		kΩ
I_{LI}	Input Leakage Current (SCL, SDA, E0-E2)	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2V, f_C = 400kHz		1	mA
I_{CC1}	Supply Current (Standby)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2V, f_C = 400kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2V		0.4	V
V_{POR} (1)	Power On Reset Threshold (ST25 series)		1.5	2	V
V_{CC} Read (1)	V_{CC} Range for Read Operations (ST25 series)		2.5	5.5	V
V_{CC} Write	V_{CC} Range for Write Operations		2.5	5.5	V

Note: 1. At the time of publication of this data sheet, the statistical history, for the ST25E16D, was not yet sufficient to guarantee a V_{CC} Read = 2V. For the lastest information contact your local SGS-THOMSON Sales Office.

Table 7. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		300	ns
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD.STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD.DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU.DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	200	800	ns
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_{NS}	t_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		5	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (5 address MSB are not constant) the maximum programming time is doubled to 20ms.

DEVICE OPERATION (cont'd)

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25E16D sample the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave ST24/25E16D, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, 3 Chip Enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation. There are two modes both for read and write. These are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Memory Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. The Least Significant Byte addresses a block of 256 bytes, bits b10,b9,b8 of the Most Significant Byte select one block among 8 blocks (one block is 256 bytes).

Most Significant Byte

0	0	0	0	0	b10	b9	b8

Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Figure 5. AC Waveforms

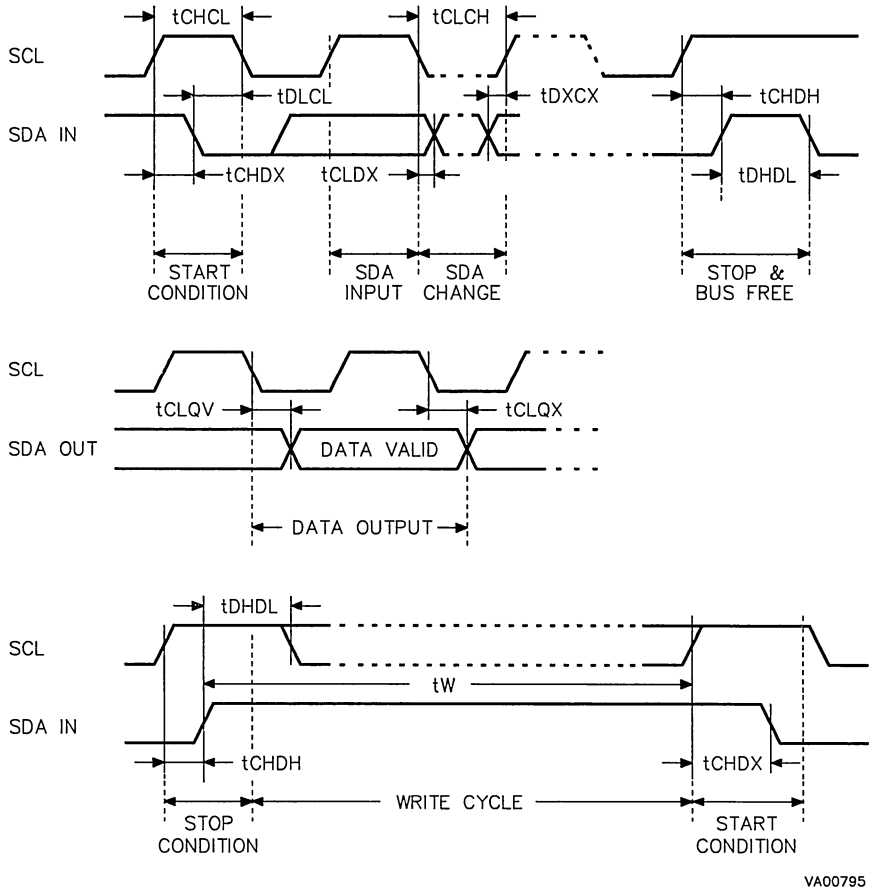
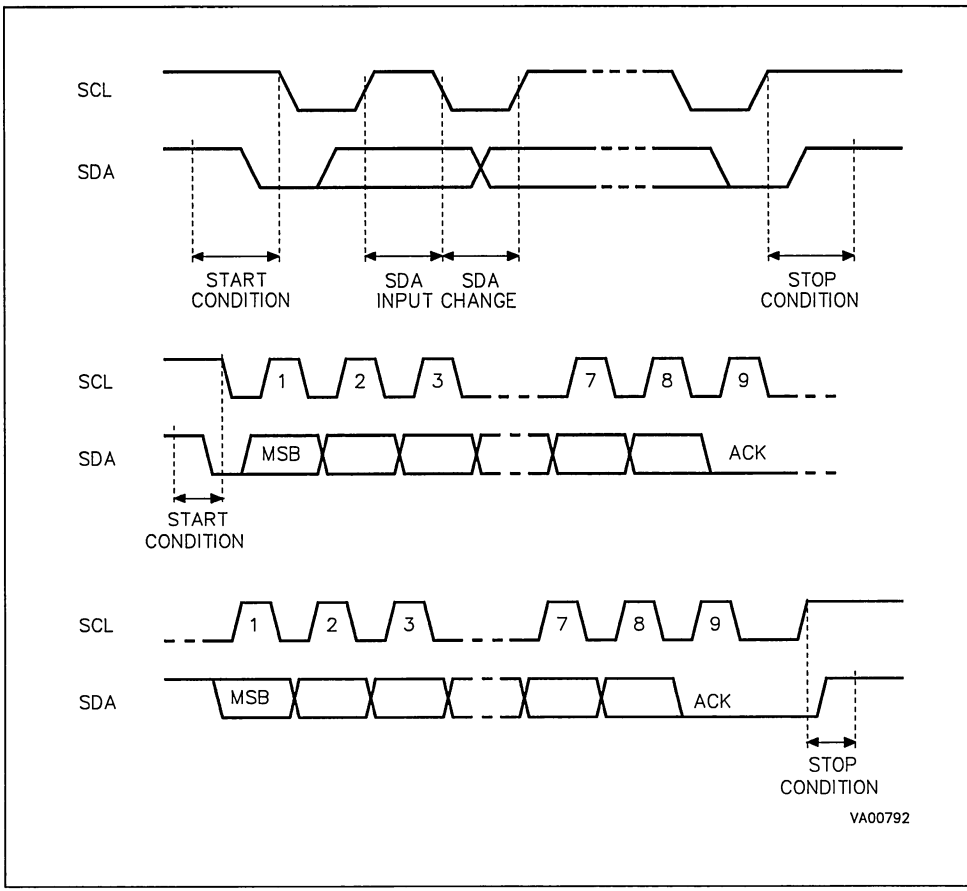


Figure 6. I²C Bus Protocol



Write Operations

Following a START condition the master sends a device select code with the RW bit reset to '0'. The ST24/25E16D acknowledge this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the 8 blocks of 256 bytes each. Writing in the ST24/25E16D may be inhibited if input pin WC is taken high.

For the ST24/25E16D versions, any write command with WC = 1 (during a period of time from the START condition untill the end of the 2 Bytes Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the ST24/25E16D. The master then terminates the transfer by generating a STOP condition.

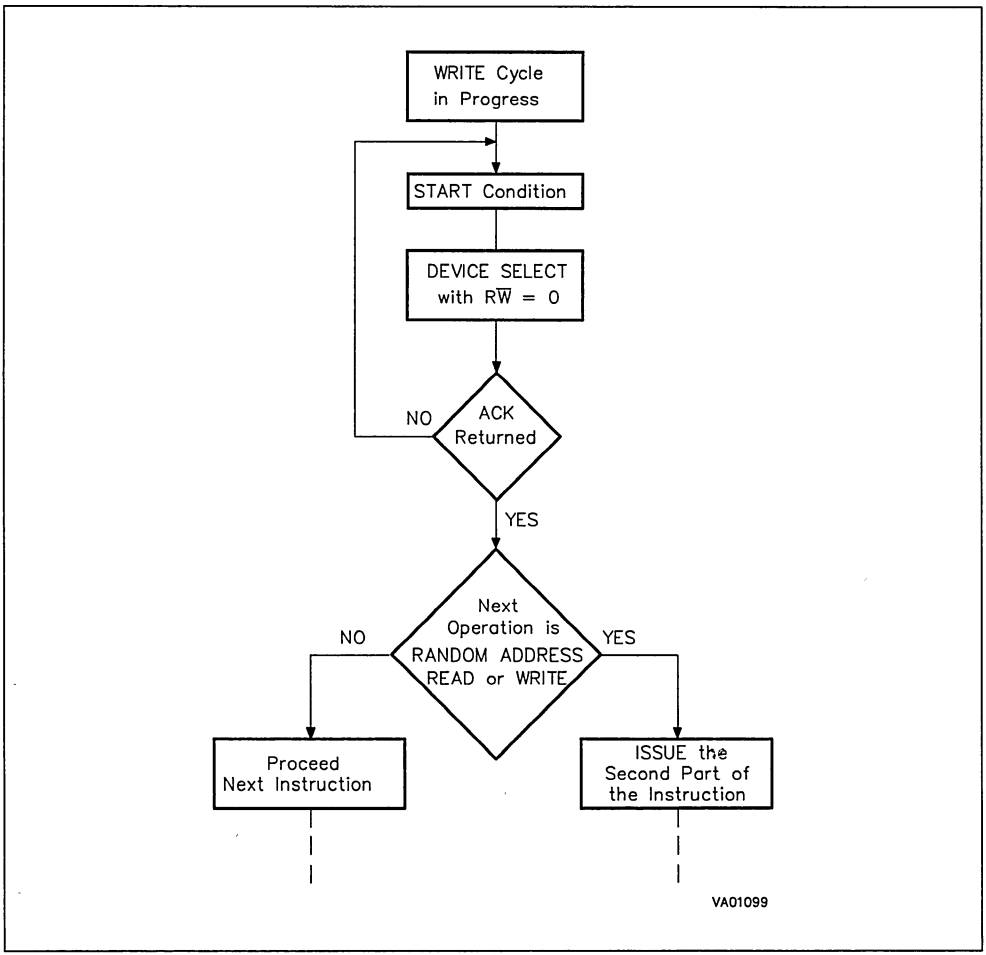
Page Write. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same row of 16 bytes in the memory, that is the same Address bits (b10-b4). The master sends one up to 16 bytes of data, which are each acknowledged by the ST24/25E16D. After each byte is transfered, the internal byte address counter (4 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over'

which could result in data being overwritten. Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST24/25E16D will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the ST24/25E16D disable itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master. The sequence is:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte. (1st byte of the new instruction)
- Step 2: if the ST24/25E16D are internally writing, no ACK will be returned. The Master goes back to Step1. If the ST24/25E16D have terminated the internal writing, it will issue an ACK. The ST24/25E16D are ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step1).

Figure 7. Write Cycle Polling using ACK



Read Operations

On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The ST24/25E16D have an internal 11 bits address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the $\overline{RW}$ bit set to '1'. The ST24/25E16D acknowledge this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the $\overline{RW}$ bit set to '1'. The ST24/25E16D acknowledge this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the ST24/25E16D continue to output the next byte in

Figure 8. Write Modes Sequence with Write Control = 0

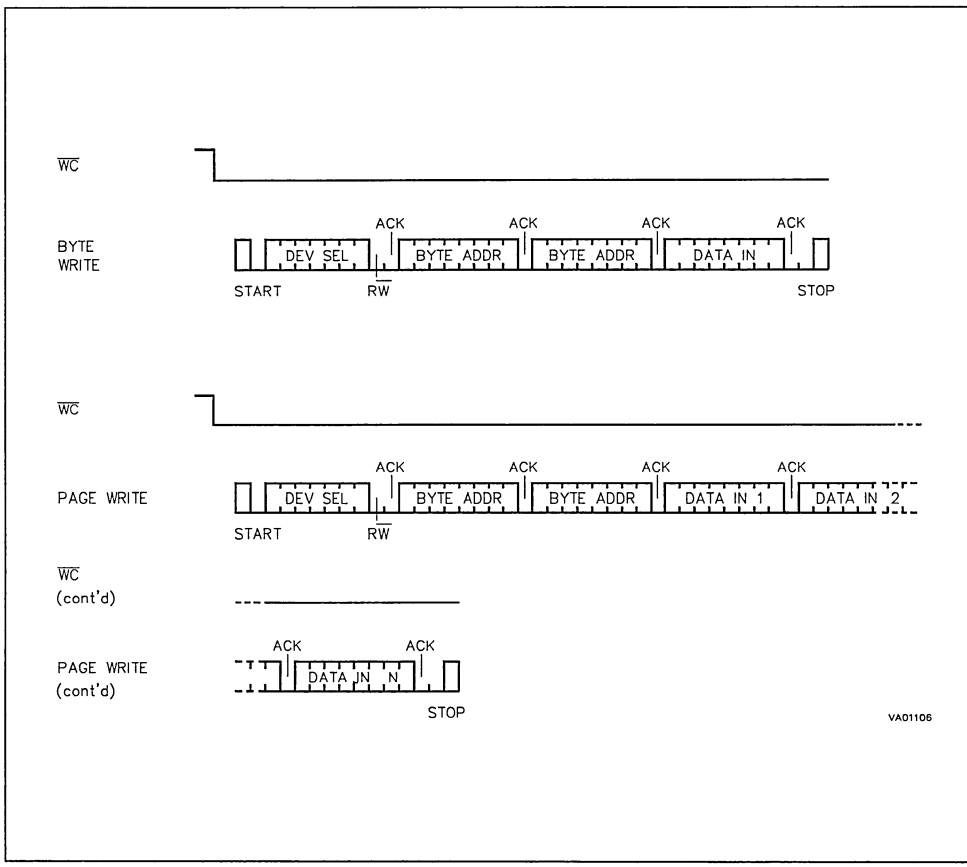
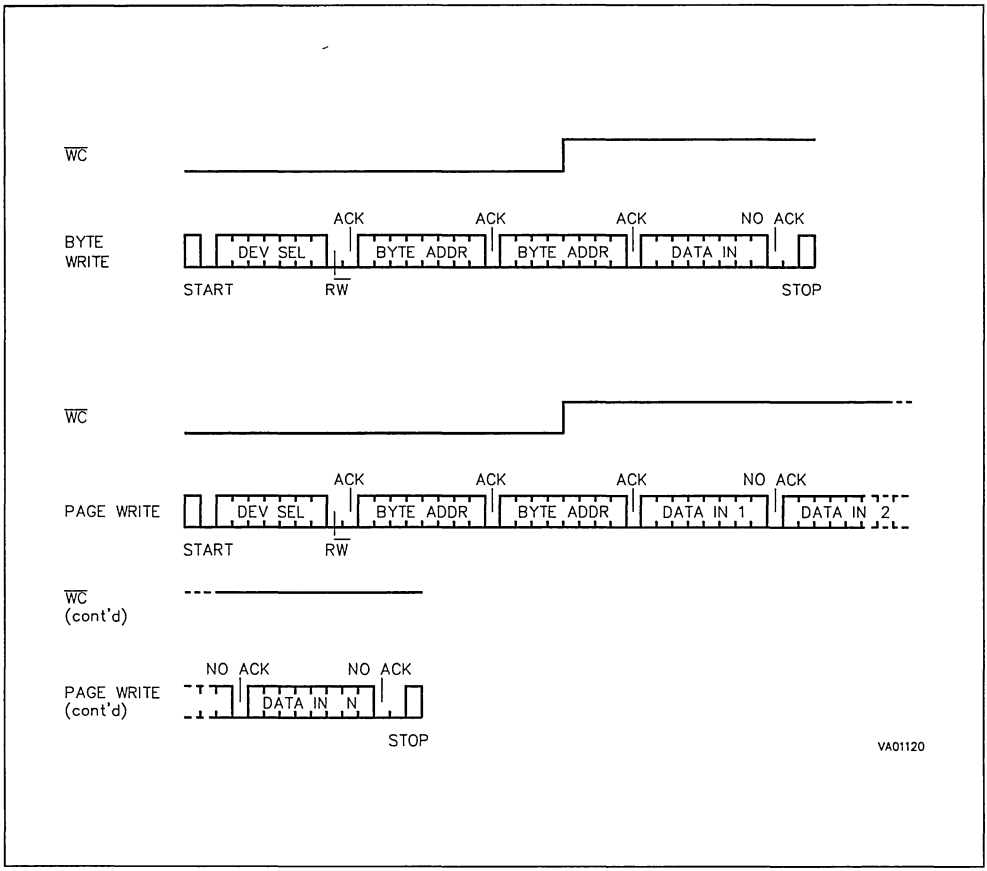


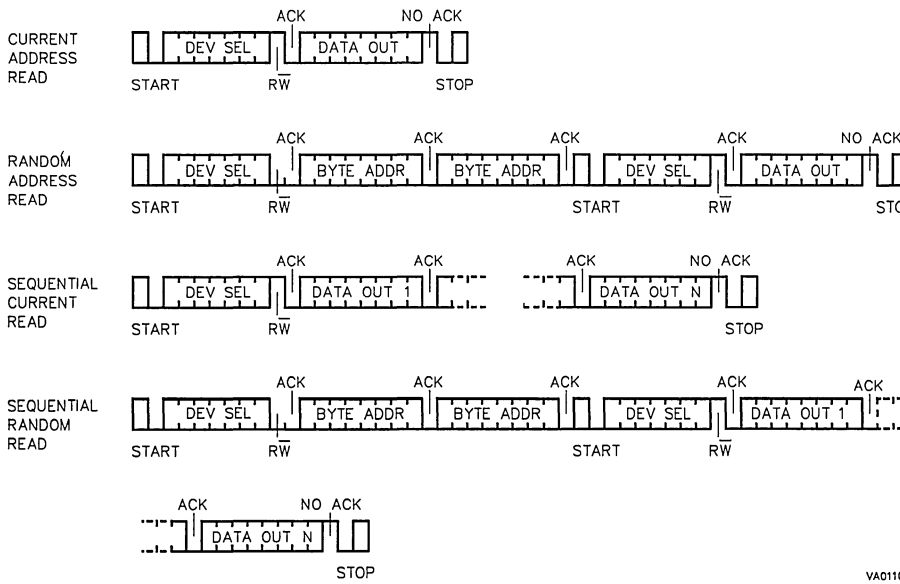
Figure 9. Write Modes Sequence with Write Control = 1



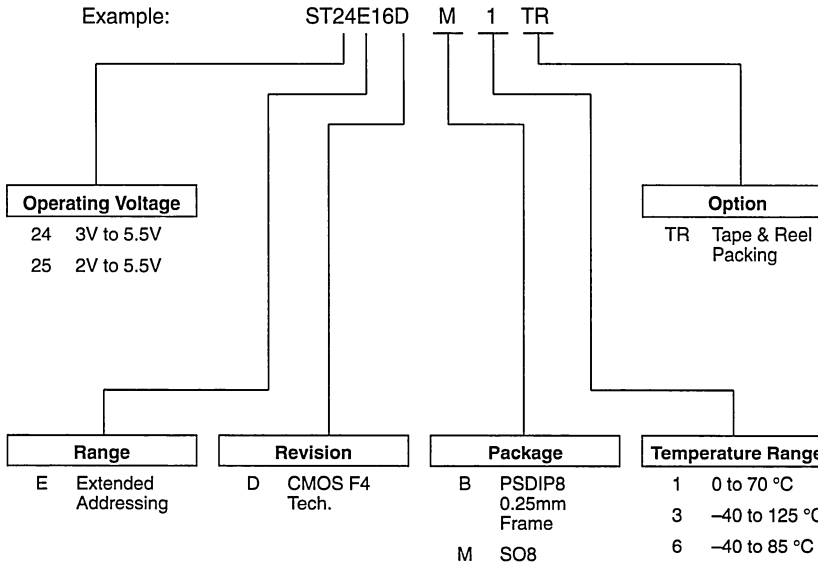
sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25E16D wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25E16D terminate the data transfer and switch to a standby state.

Figure 10. Read Modes Sequence



ORDERING INFORMATION SCHEME



Parts are shipped with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Range, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SGS-THOMSON MICROELECTRONICS

ST24E32D
ST25E32D

SERIAL ACCESS CMOS 32K (4096 x 8) EEPROMs EXTENDED ADDRESSING COMPATIBLE WITH I²C BUS

PRODUCT CONCEPT

- COMPATIBLE with I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24E32D version
  - 2V to 5.5V for ST25E32D version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 32 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

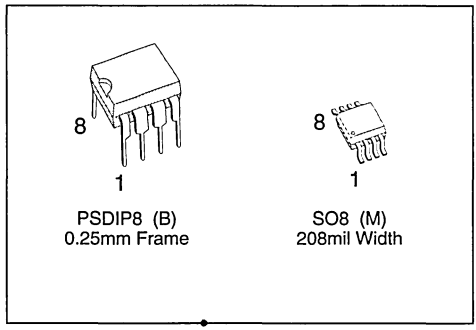
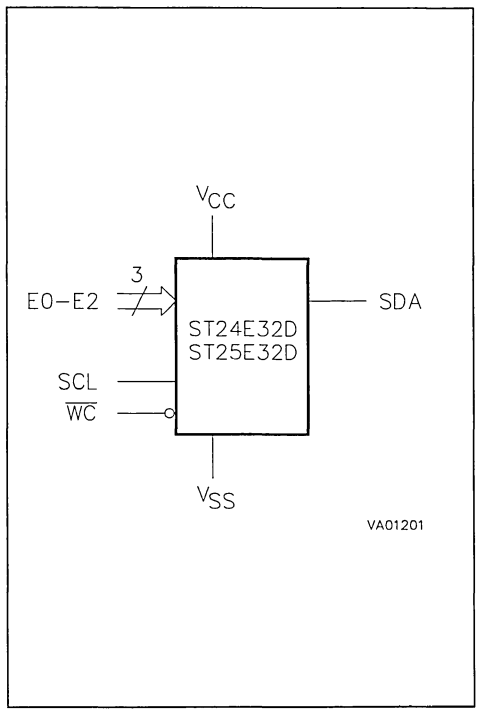


Figure 1. Logic Diagram



DESCRIPTION

The ST24/25E32D are 32K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 512 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The ST25E32D operates with a power supply value as

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

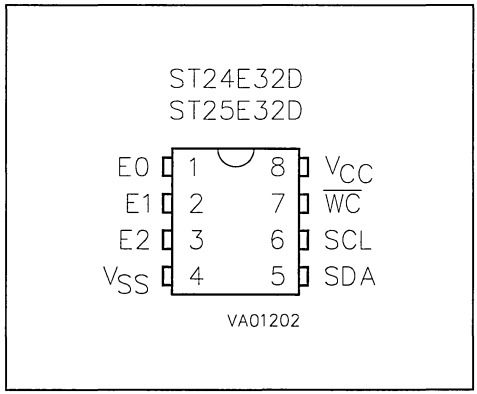


Figure 2B. SO Pin Connections

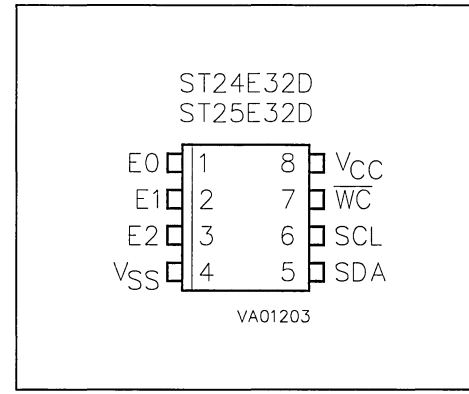


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 3 grade 6	–40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

low as 2.0V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E32D carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E32D behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknow-

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	RW bit	Bytes	Initial Sequence
Current Address Read	'1'	1	START, Device Select, RW = '1'
Random Address Read	'0'		START, Device Select, RW = '0', Address
	'1'	1	reSTART, Device Select, RW = '1'
Sequential Read	'1'	1 to 4096	As CURRENT or RANDOM Mode
Byte Write	'0'	1	START, Device Select, RW = '0'
Page Write	'0'	32	START, Device Select, RW = '0'

Note: X = V_{IH} or V_{IL}.

ledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way.

Data transfers are terminated with a STOP condition. In this way, up to 8 ST24/25E32D may be connected to the same I^2C bus and selected individually, allowing a total addressing field of 256 Kbit.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3)

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL compatible.

Write Control ($\overline{WC}$). The Write Control feature $\overline{WC}$ is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH}) or disable ($\overline{WC}$ at V_{IL}) the internal write protection. The devices with this Write Control feature no longer supports the multibyte mode of operation. When pin $\overline{WC}$ is unconnected, the $\overline{WC}$ input is internally read as V_{IL}.

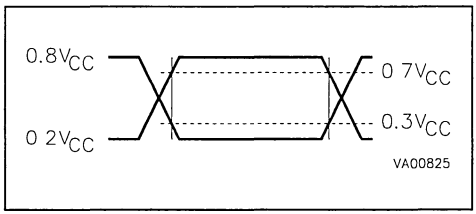
When $\overline{WC}$=1, Device Select and Address bytes are acknowledged; Data bytes are not acknowledged.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION

I²C Bus Background

The ST24/25E32D support the extended addressing I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25E32D are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25E32D continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25E32D and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus, f_C = 400kHz

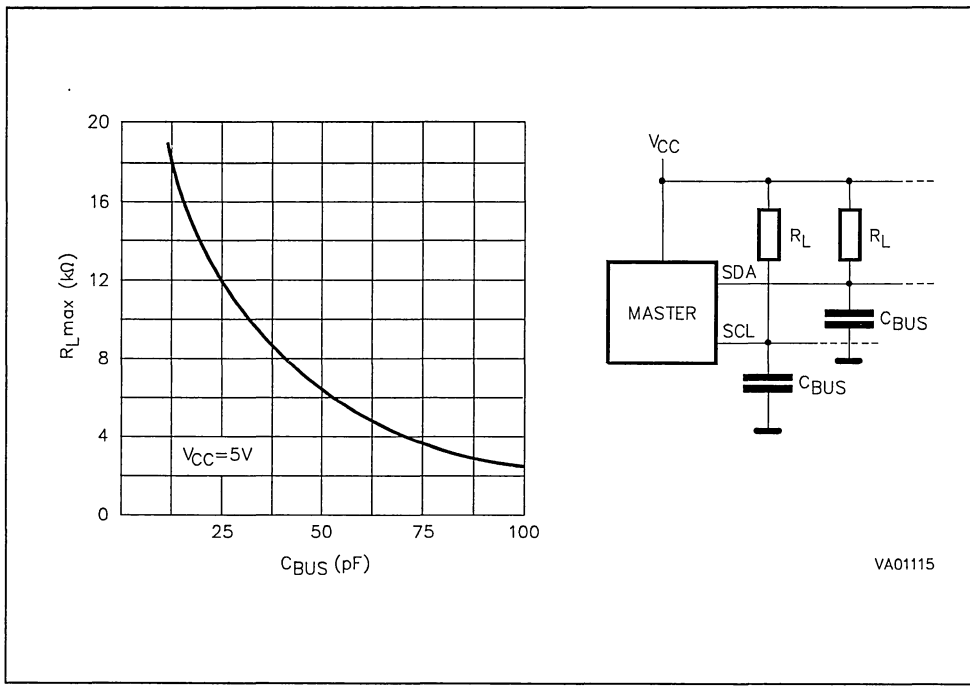


Table 5. Capacitance (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter		Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
R_{IN}	$\overline{WC}$ Input Resistor	$0V \leq V_{IN} \leq 0.3V_{CC}$	8	25	kΩ
		$0.7\ V_{CC} \leq V_{IN} \leq V_{CC}$	1		kΩ
I_{LI}	Input Leakage Current (SCL, SDA, E0-E2)	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2V, f_C = 400kHz		1	mA
I_{CC1}	Supply Current (Standby)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		20	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2V, f_C = 400kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2V		0.4	V
V_{CC} Read	V_{CC} Range for Read Operations (ST25 series)		2		V
V_{CC} Write	V_{CC} Range for Write Operations		2		V

Table 7. AC Characteristics
(T_A = –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		300	ns
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD.STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD.DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	200	800	ns
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_{NS}	t_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W	t_{WR}	Write Time (ST25E32D at V_{CC} = 2V)		5	ms
		Write Time (ST24E32D at V_{CC} = 5V)		10	ms

Note: 1. For a reSTART condition, or following a write cycle.

DEVICE OPERATION (cont'd)

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25E32D sample the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave ST24/25E32D, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, 3 Chip Enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation. There are two modes both for read and write. These are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Memory Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. The Least Significant Byte addresses a block of 256 bytes, bits b11,b10,b9,b8 of the Most Significant Byte select one block among 16 blocks (one block is 256 bytes).

Most Significant Byte

0	0	0	0	b11	b10	b9	b8

Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Figure 5. AC Waveforms

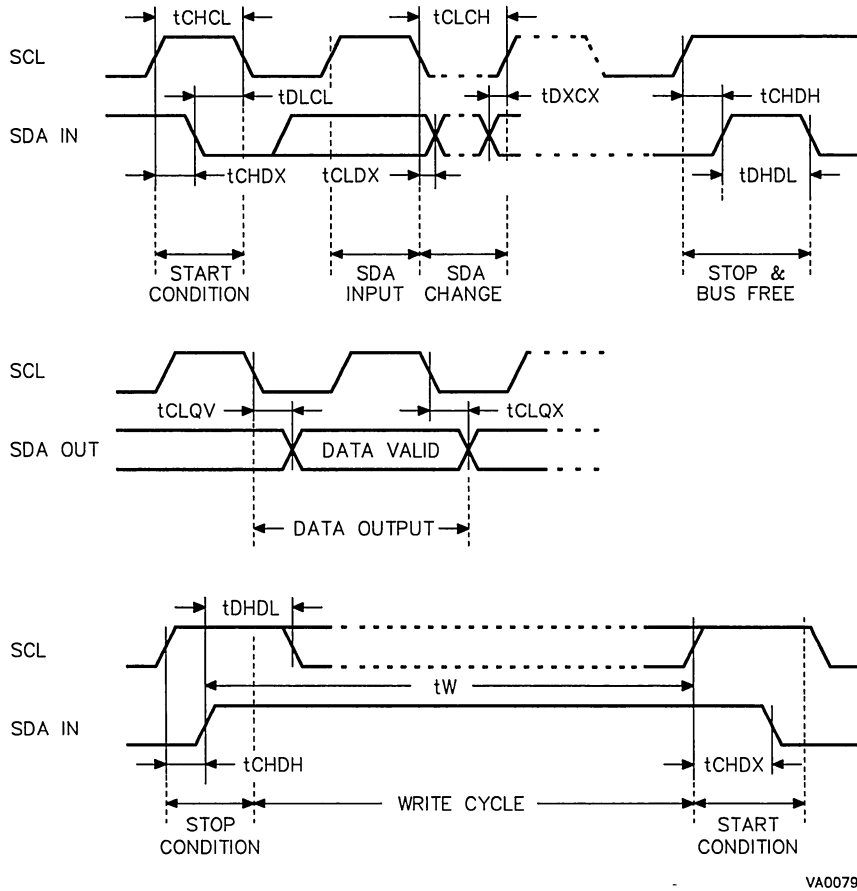
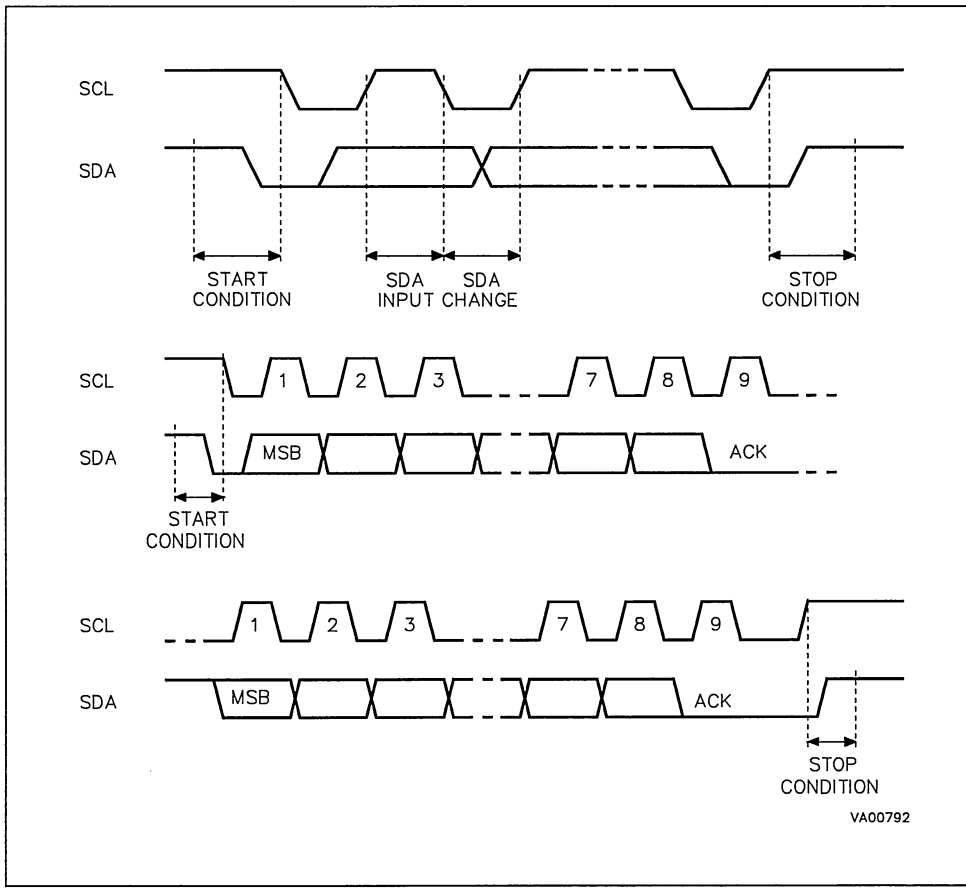


Figure 6. I²C Bus Protocol



Write Operations

Following a START condition the master sends a device select code with the RW bit reset to '0'. The ST24/25E32D acknowledge this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the 16 blocks of 256 bytes each. Writing in the ST24/25E32D may be inhibited if input pin WC is taken high.

For the ST24/25E32D versions, any write command with WC = 1 (during a period of time from the START condition untill the end of the 2 Bytes Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the ST24/25E32D. The master then terminates the transfer by generating a STOP condition.

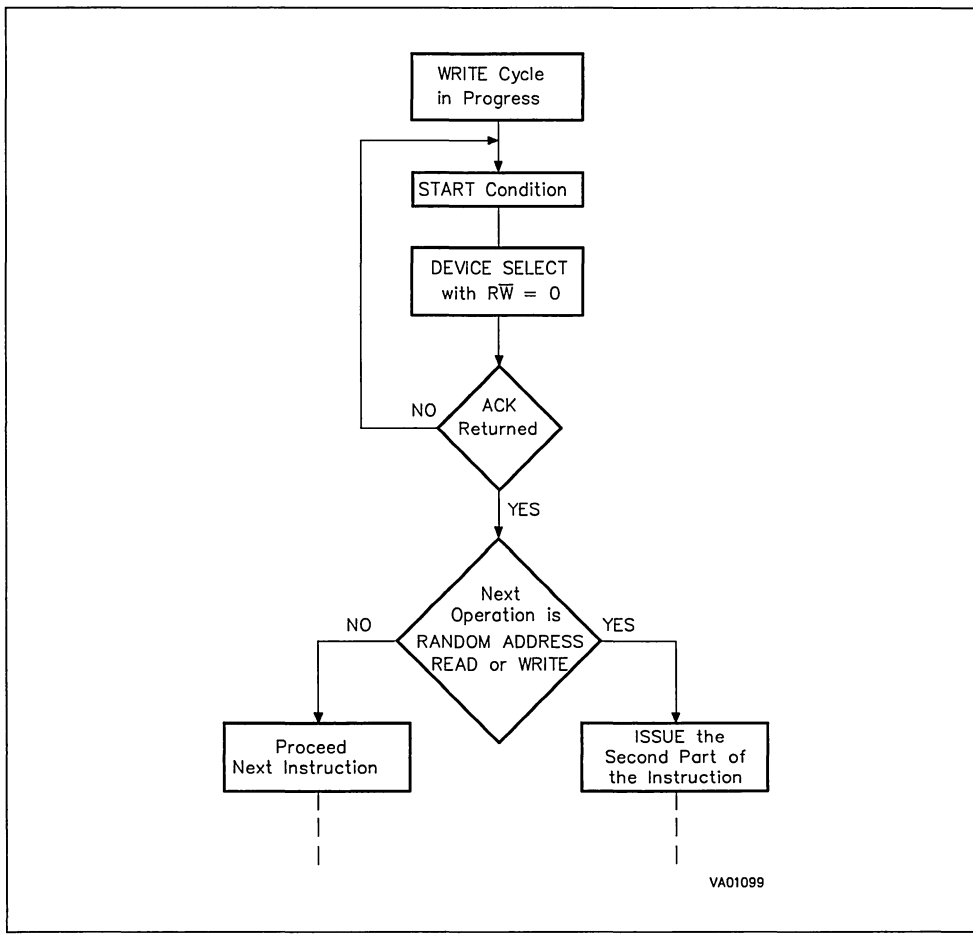
Page Write. The Page Write mode allows up to 32 bytes to be written in a single write cycle, provided that they are all located in the same row of 32 bytes in the memory, that is the same Address bits (b11 to b5). The master sends one up to 32 bytes of data, which are each acknowledged by the ST24/25E32D. After each byte is transfered, the internal byte address counter (5 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. This STOP condition will trigger an internal memory program cycle only if the STOP condition is internally decoded right after the ACK bit; any STOP condition decoded out of this "10th bit" time slot will not trigger the internal programming cycle. All inputs are disabled until the completion of this cycle and the ST24/25E32D will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the ST24/25E32D disable itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master. The sequence is:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte. (1st byte of the new instruction)
- Step 2: if the ST24/25E32D are internally writing, no ACK will be returned. The Master goes back to Step1. If the ST24/25E32D have terminated the internal writing, it will issue an ACK. The ST24/25E32D are ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step1).

Figure 7. Write Cycle Polling using ACK



Read Operations

On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The ST24/25E32D have an internal 12 bits address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the $\overline{RW}$ bit set to '1'. The ST24/25E32D acknowledge this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the $\overline{RW}$ bit set to '1'. The ST24/25E32D acknowledge this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the ST24/25E32D continue to output the next byte in

Figure 8. Write Modes Sequence with Write Control = 0

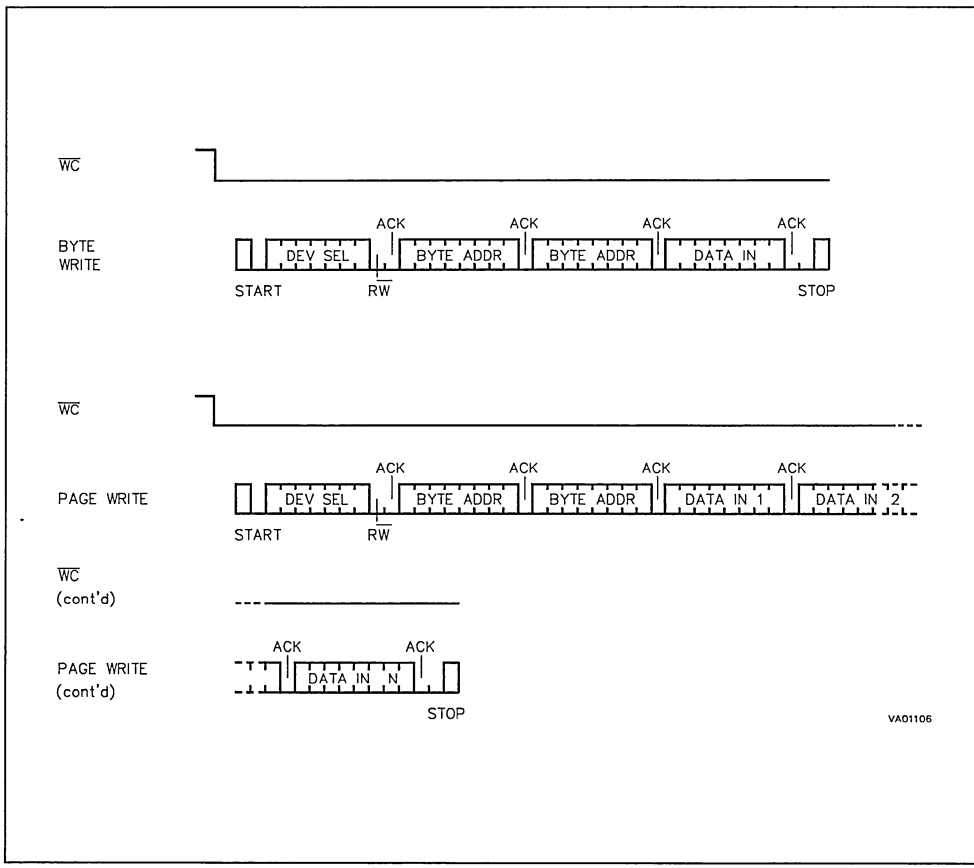
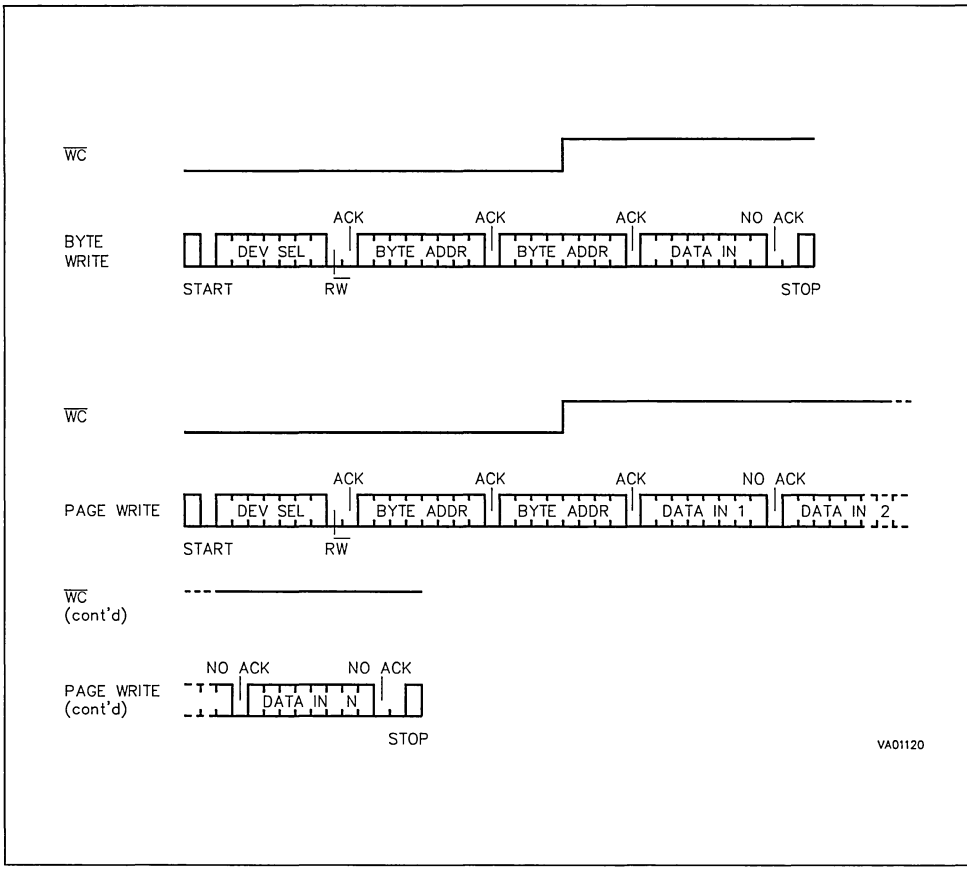


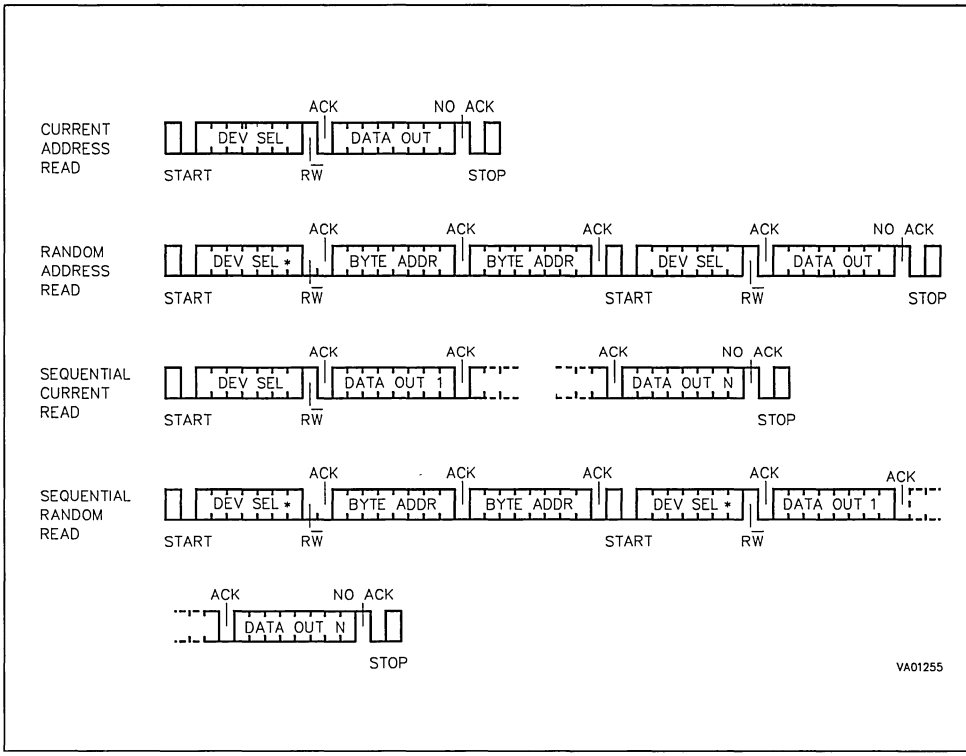
Figure 9. Write Modes Sequence with Write Control = 1



sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

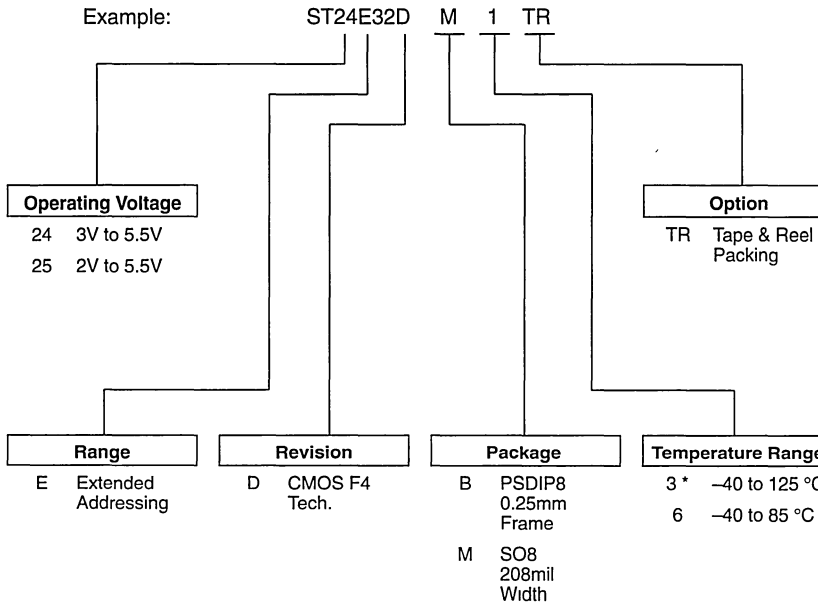
Acknowledge in Read Mode. In all read modes the ST24/25E32D wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25E32D terminate the data transfer and switch to a standby state.

Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 4th byte) must be identical.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on request only.

Parts are shipped with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Range, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SGS-THOMSON MICROELECTRONICS

ST24E64D
ST25E64D

SERIAL ACCESS CMOS 64K (8192 x 8) EEPROMs EXTENDED ADDRESSING COMPATIBLE WITH I²C BUS

PRODUCT CONCEPT

- COMPATIBLE with I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24E64D version
  - 2V to 5.5V for ST25E64D version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 32 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

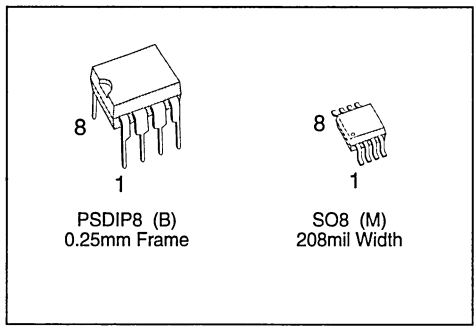
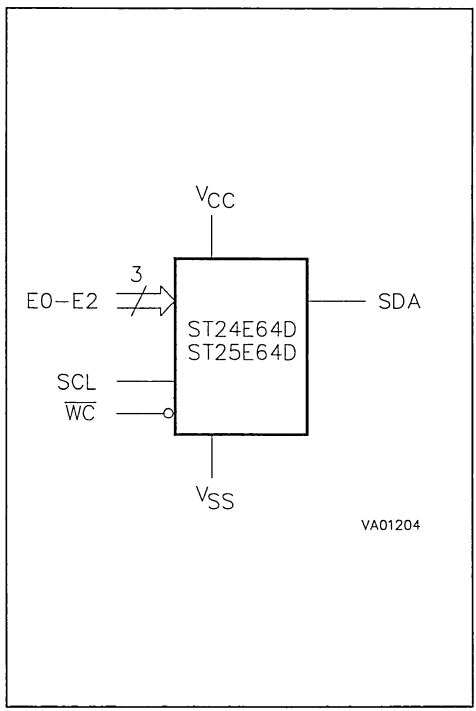


Figure 1. Logic Diagram



DESCRIPTION

The ST24/25E64D are 64K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 1024 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The ST25E64D operates with a power supply value as

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

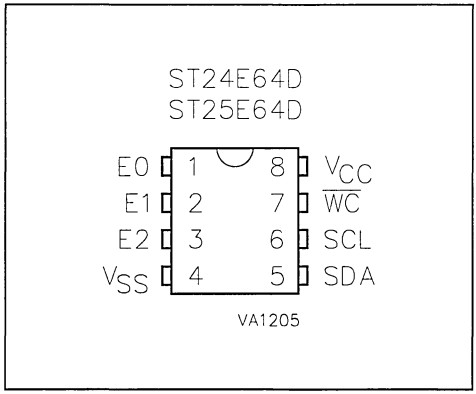


Figure 2B. SO Pin Connections

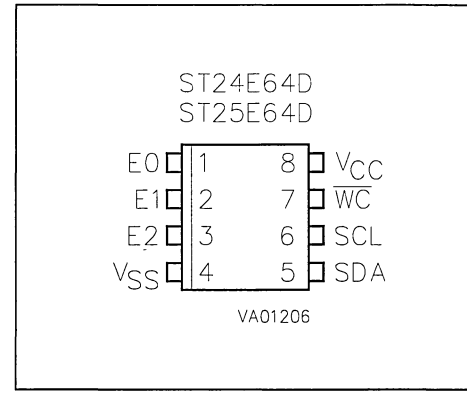


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 3 grade 6	–40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

low as 2.0V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E64D carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E64D behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknow-

Table 3. Device Select Code

	Device Code				Chip Enable			$\overline{RW}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	$\overline{RW}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	$\overline{RW}$ bit	Bytes	Initial Sequence
Current Address Read	'1'	1	START, Device Select, $\overline{RW}$ = '1'
Random Address Read	'0'		START, Device Select, $\overline{RW}$ = '0', Address
	'1'	1	reSTART, Device Select, $\overline{RW}$ = '1'
Sequential Read	'1'	1 to 8192	As CURRENT or RANDOM Mode
Byte Write	'0'	1	START, Device Select, $\overline{RW}$ = '0'
Page Write	'0'	64	START, Device Select, $\overline{RW}$ = '0'

Note: X = V_{IH} or V_{IL}.

ledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way.

Data transfers are terminated with a STOP condition. In this way, up to 8 ST24/25E64D may be connected to the same I^2C bus and selected individually, allowing a total addressing field of 512 Kbit.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3)

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL compatible.

Write Control ($\overline{WC}$). The Write Control feature $\overline{WC}$ is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH}) or disable ($\overline{WC}$ at V_{IL}) the internal write protection. The devices with this Write Control feature no longer supports the multibyte mode of operation. When pin $\overline{WC}$ is unconnected, the $\overline{WC}$ input is internally read as V_{IL}.

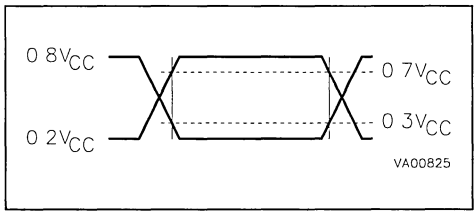
When $\overline{WC}$=1, Device Select and Address bytes are acknowledged; Data bytes are not acknowledged.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION

I²C Bus Background

The ST24/25E64D support the extended addressing I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25E64D are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25E64D continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25E64D and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus, f_C = 400kHz

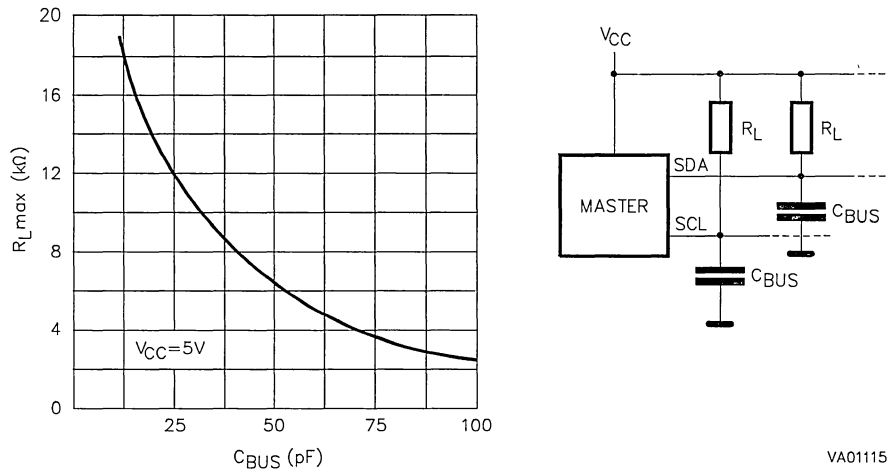


Table 5. Capacitance (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter		Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
R_{IN}	$\overline{WC}$ Input Resistor	$0V \leq V_{IN} \leq 0.3V_{CC}$	8	25	kΩ
		$0.7\ V_{CC} \leq V_{IN} \leq V_{CC}$	1		kΩ
I_{LI}	Input Leakage Current (SCL, SDA, E0-E2)	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2V, f_C = 400kHz		1	mA
I_{CC1}	Supply Current (Standby)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		20	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2V, f_C = 400kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2V		0.4	V
V_{CC} Read	V_{CC} Range for Read Operations (ST25 series)		2		V
V_{CC} Write	V_{CC} Range for Write Operations		2		V

Table 7. AC Characteristics
(T_A = –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V or 2V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		300	ns
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	200	800	ns
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_{NS}	t_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W	t_{WR}	Write Time (ST25E64D at V_{CC} = 2V)		5	ms
		Write Time (ST24E64D at V_{CC} = 5V)		10	ms

Note: 1. For a reSTART condition, or following a write cycle.

DEVICE OPERATION (cont'd)

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25E64D sample the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave ST24/25E64D, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, 3 Chip Enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation. There are two modes both for read and write. These are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Memory Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. The Least Significant Byte addresses a block of 256 bytes, bits b12,b11,b10,b9,b8 of the Most Significant Byte select one block among 32 blocks (one block is 256 bytes).

Most Significant Byte

0	0	0	b12	b11	b10	b9	b8

Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Figure 5. AC Waveforms

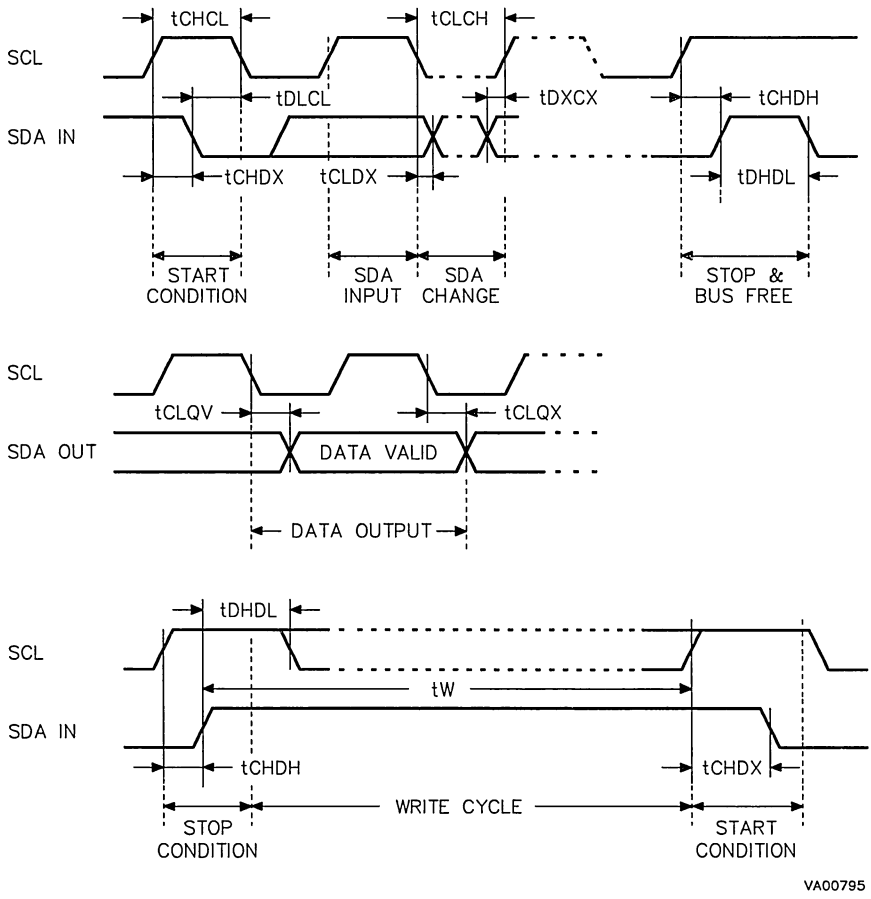
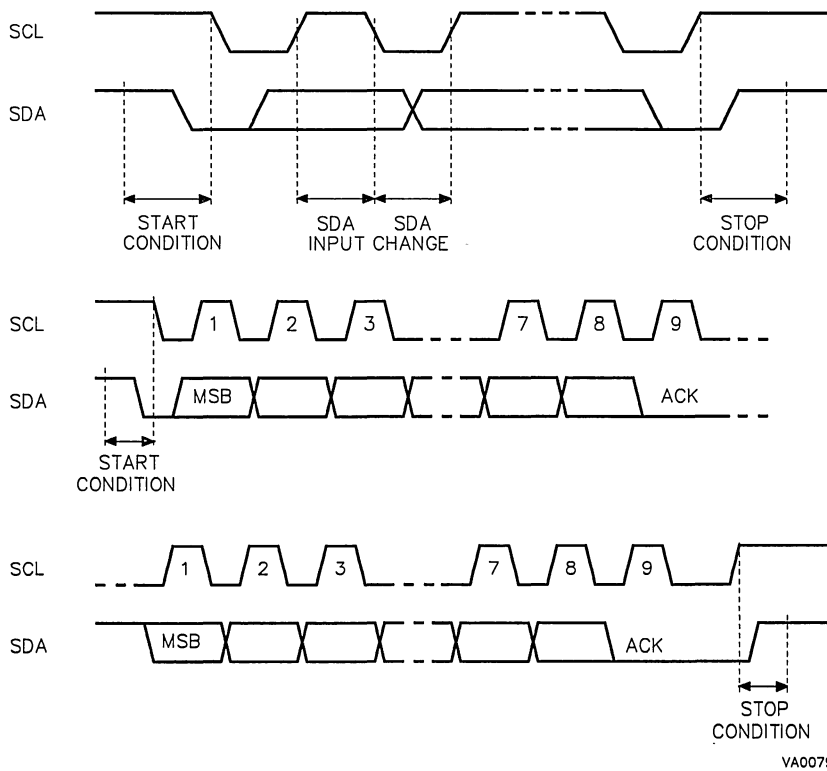


Figure 6. I²C Bus Protocol



Write Operations

Following a START condition the master sends a device select code with the RW bit reset to '0'. The ST24/25E64D acknowledge this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the 32 blocks of 256 bytes each. Writing in the ST24/25E64D may be inhibited if input pin WC is taken high.

For the ST24/25E64D versions, any write command with WC = 1 (during a period of time from the START condition untill the end of the 2 Bytes Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the ST24/25E64D. The master then terminates the transfer by generating a STOP condition.

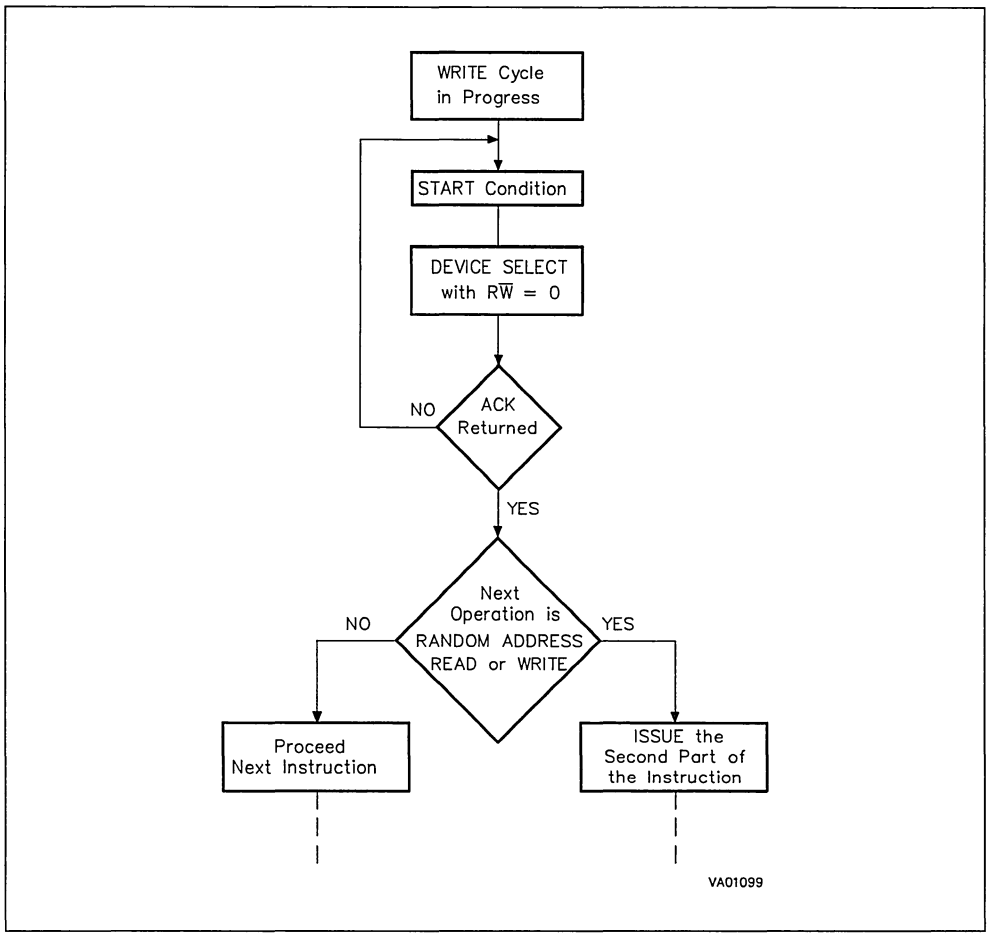
Page Write. The Page Write mode allows up to 32 bytes to be written in a single write cycle, provided that they are all located in the same row of 32 bytes in the memory, that is the same Address bits (b12 to b5). The master sends one up to 64 bytes of data, which are each acknowledged by the ST24/25E64D. After each byte is transfered, the internal byte address counter (5 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. This STOP condition will trigger an internal memory program cycle only if the STOP condition is internally decoded right after the ACK bit; any STOP condition decoded out of this "10th bit" time slot will not trigger the internal programming cycle. All inputs are disabled until the completion of this cycle and the ST24/25E64D will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the ST24/25E64D disable itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master. The sequence is:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte. (1st byte of the new instruction)
- Step 2: if the ST24/25E64D are internally writing, no ACK will be returned. The Master goes back to Step1. If the ST24/25E64D have terminated the internal writing, it will issue an ACK. The ST24/25E64D are ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step1).

Figure 7. Write Cycle Polling using ACK



Read Operations

On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The ST24/25E64D have an internal 13 bits address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the $\overline{RW}$ bit set to '1'. The ST24/25E64D acknowledge this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the $\overline{RW}$ bit set to '1'. The ST24/25E64D acknowledge this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the ST24/25E64D continue to output the next byte in

Figure 8. Write Modes Sequence with Write Control = 0

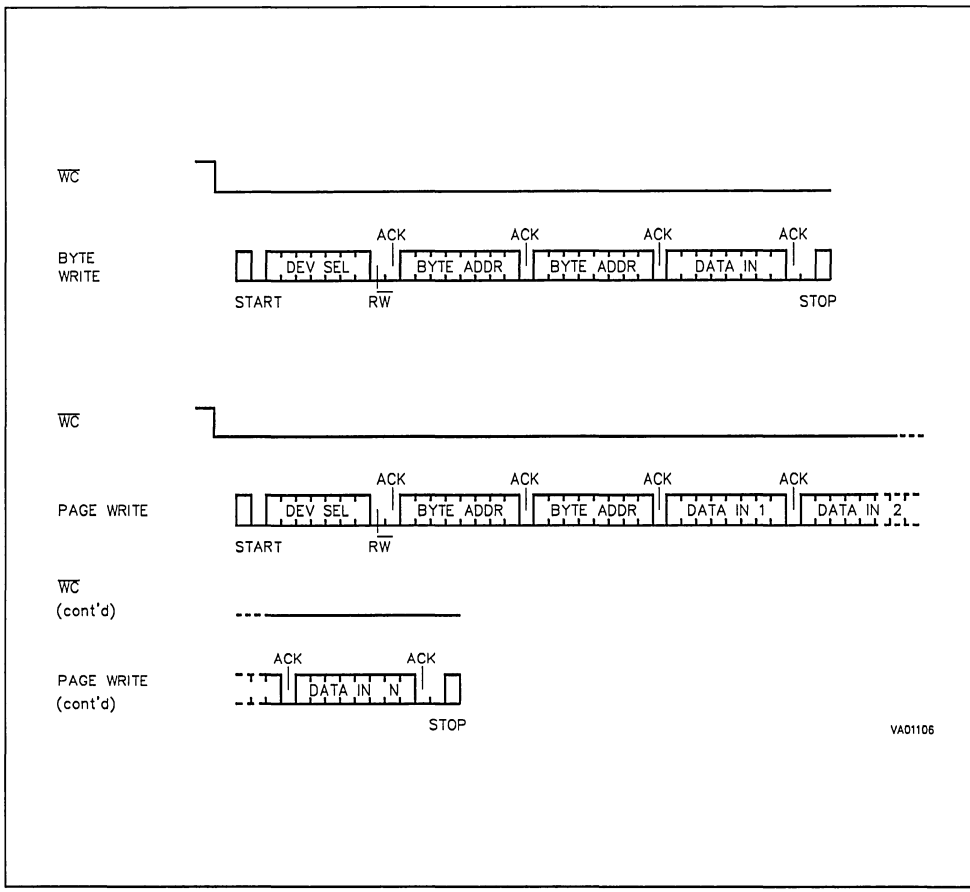
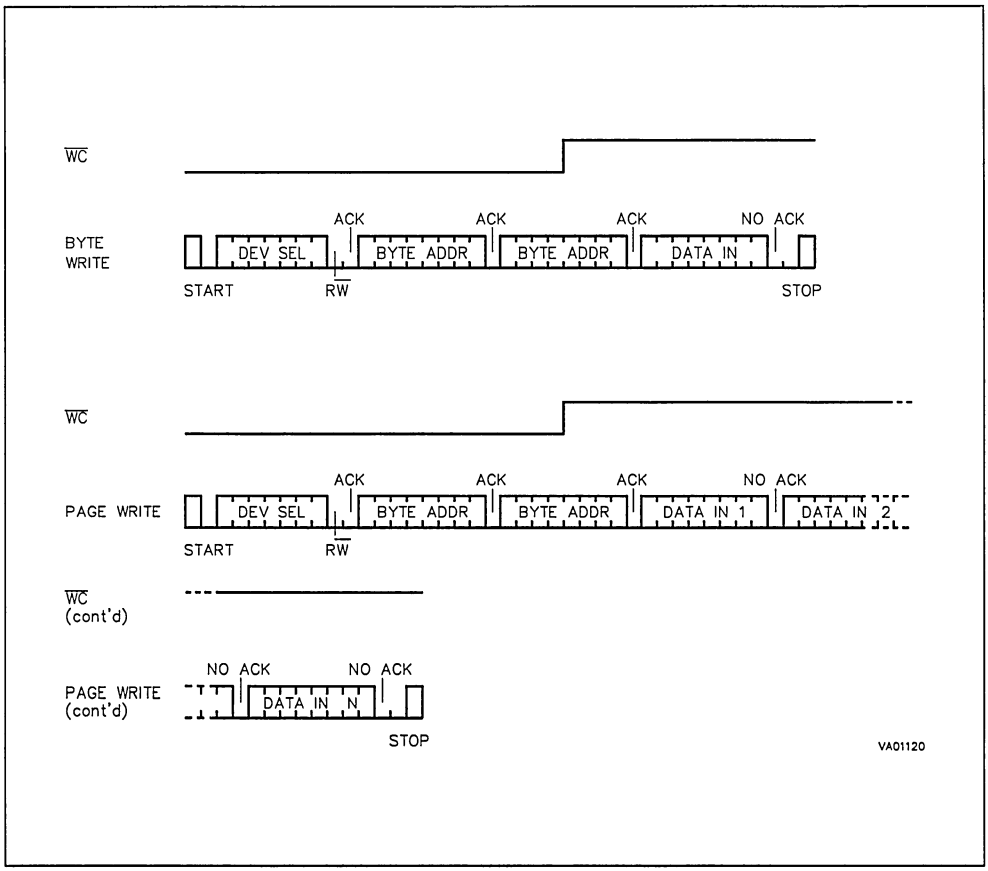


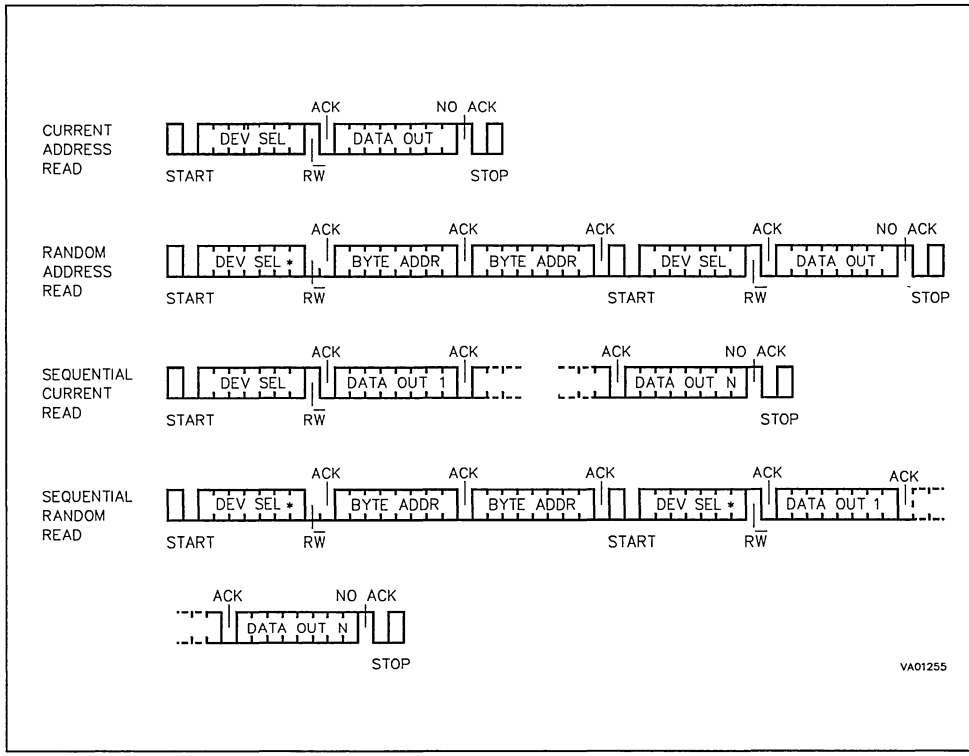
Figure 9. Write Modes Sequence with Write Control = 1



sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

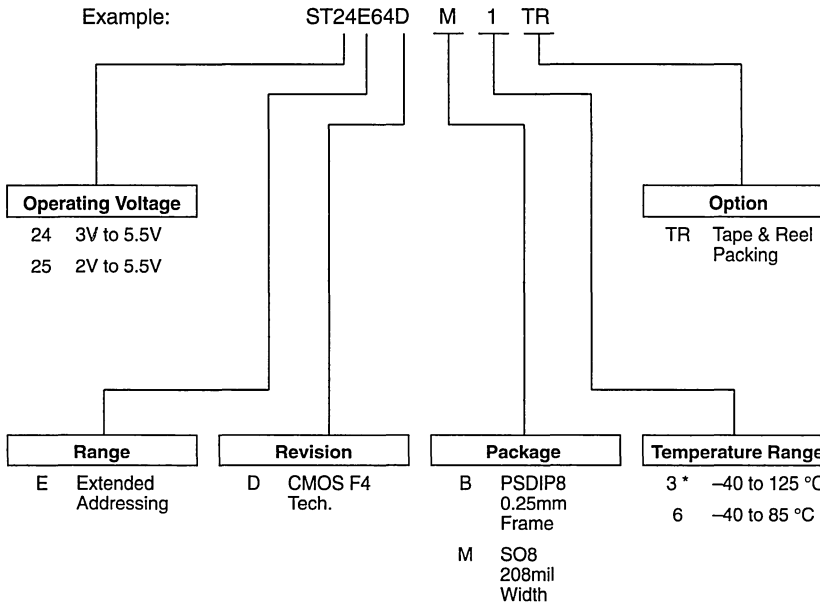
Acknowledge In Read Mode. In all read modes the ST24/25E64D wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25E64D terminate the data transfer and switch to a standby state.

Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 4th byte) must be identical.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on request only.

Parts are shipped with the memory content set at all "1's" (FFh).

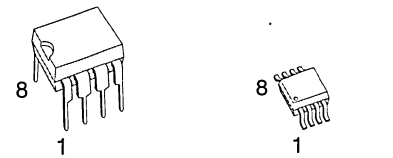
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

MICROWIRE BUS EEPROM

SERIAL ACCESS CMOS 256 bit (16 x 16 or 32 x 8) EEPROM

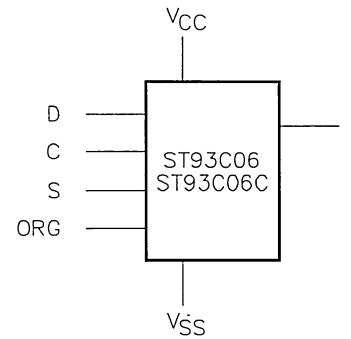
- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- DUAL ORGANIZATION: 16 x 16 or 32 x 8
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE
  - 5V ±10% for ST93C06 version
  - 3V to 5.5V for ST93C06C version
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ENHANCED ESD/LATCH UP PERFORMANCES for "C" VERSION



PSDIP8 (B)
0.4mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST93C06 and ST93C06C are 256 bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. In the text the two products are referred to as ST93C06.

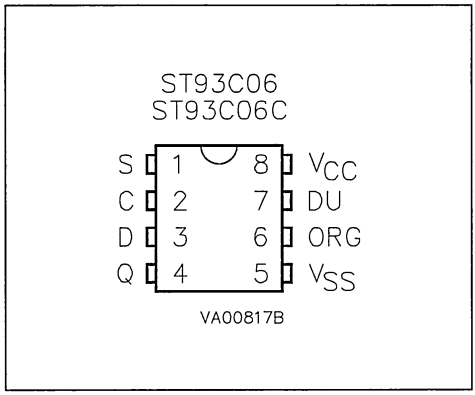
The memory is divided into either 32 x 8 bit bytes or 16 x 16 bit words. The organization may be selected by a signal applied on the ORG input.

The memory is accessed through a serial input (D) and by a set of instructions which includes Read a

Table 1. Signal Names

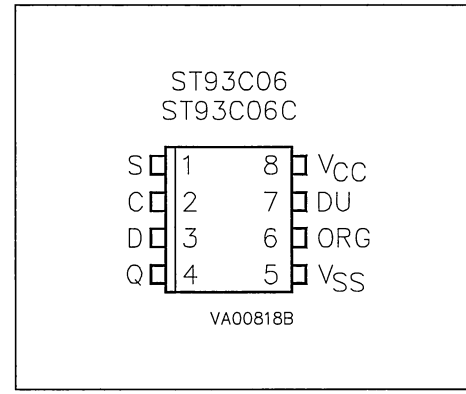
S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST93C06 ST93C06C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST93C06 ST93C06C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

byte/word, Write a byte/word, Erase a byte/word, Erase All and Write All. A Read instruction loads the address of the first byte/word to be read into an internal address pointer. The data contained at this address is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93C06 can output a sequential stream of data bytes/words. In this way, the memory can be read as a data stream from 8 to 256 bits long, or continuously as the address counter automatically rolls over to 00 when the highest address is reached.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the 32 bytes or 16 words. After the start of the programming cycle a Busy/Ready signal

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

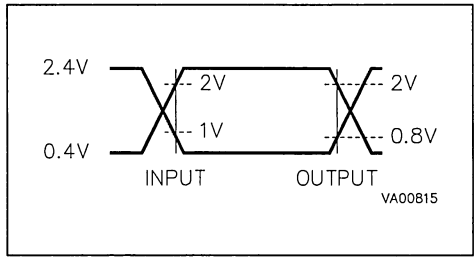


Table 3. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST93C06, ST93C06C	1,000,000	10

Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 5. DC Characteristics (T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10% for ST93C06 and V_{CC} = 3V to 5.5V for ST93C06C)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 6. AC Characteristics (T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10% for ST93C06 and V_{CC} = 3V to 5.5V for ST93C06C)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	Temp. Range: grade 1	100		ns
			Temp. Range: grades 3, 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			100	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

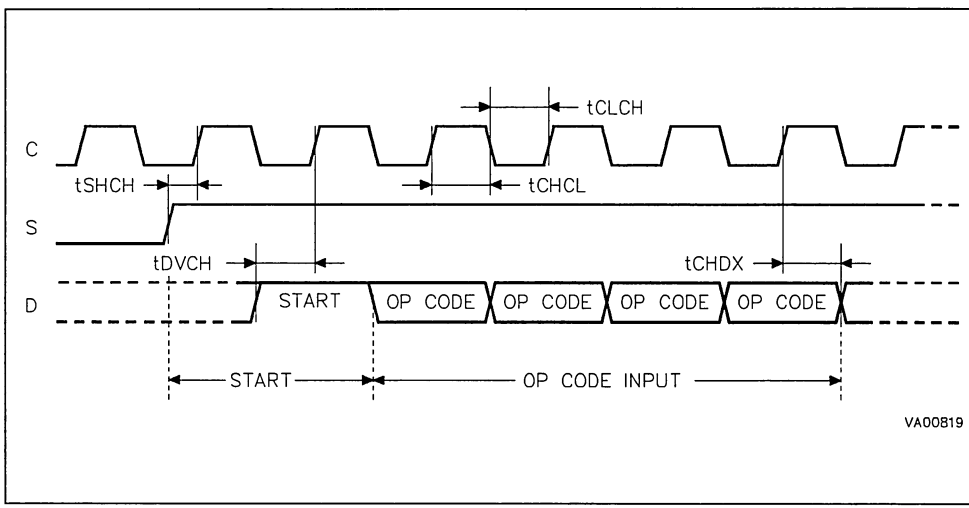
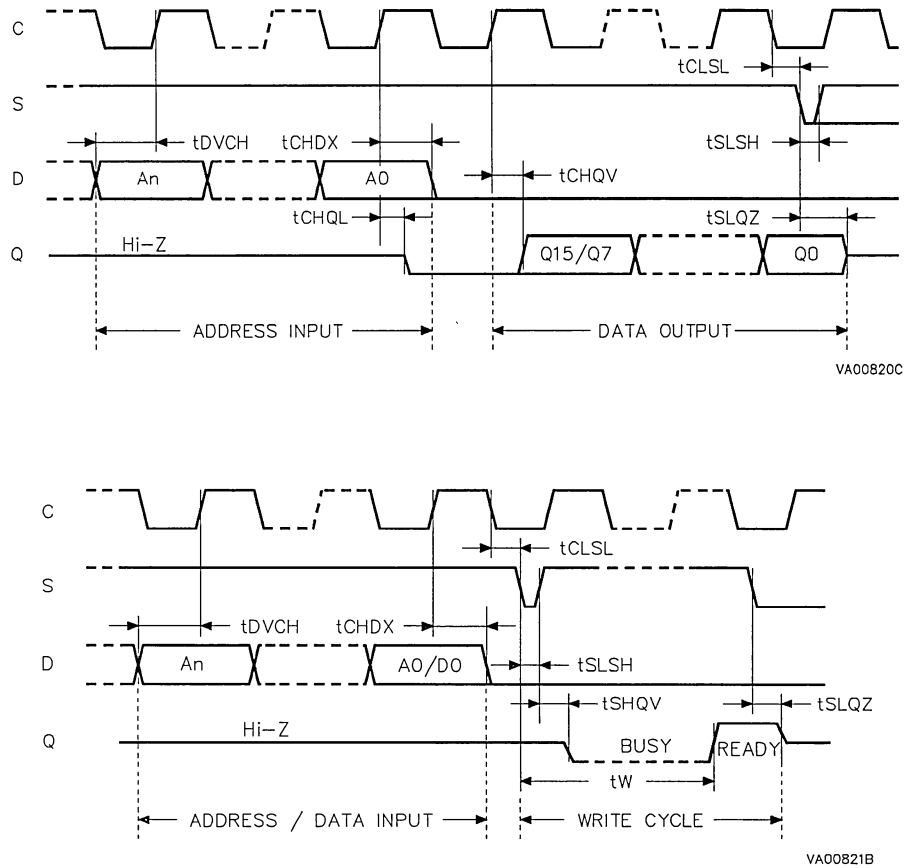


Figure 5. Synchronous Timing, Read or Write



DESCRIPTION (cont'd)

is available on the Data output (Q) when Chip Select (S) is driven High. The design of the ST93C06 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

MEMORY ORGANIZATION

The ST93C06 is organized as 32 bytes x 8 bits or 16 words x 16 bits. If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected, when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the ST93C06 is in standby mode, the ORG input should be unconnected or set to either V_{IL} or V_{IH} in order to achieve the minimum power consumption. Any voltage between V_{IL} and V_{IH} applied to ORG may increase the standby current value.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied before any logic signal.

!NSTRUCTIONS

The ST93C06 has seven instructions, as shown in Table 7. The op-codes of the instructions are made up of 4 bits: some instructions use only the first two bits, others use all four bits to define the op-code. The op-code is followed by an address for the byte/word which is four bits long for the x16 organization or five bits long for the x8 organization.

Each instruction starts with the rising edge of the signal applied on the S input, followed by a first clock pulse which is ignored by the ST93C06 optional clock pulse for the ST93C06C. The data input D is then sampled upon the following rising edges of the clock C untill a '1' is sampled and decoded by the ST93C06 as a Start bit. Even though the first clock pulse is ignored, it recommended to pull low the data input D during this first clock pulse in order to keep the timing upwardly compatible with other ST93Cxx devices.

The ST93C06 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 6).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The ST93C06 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

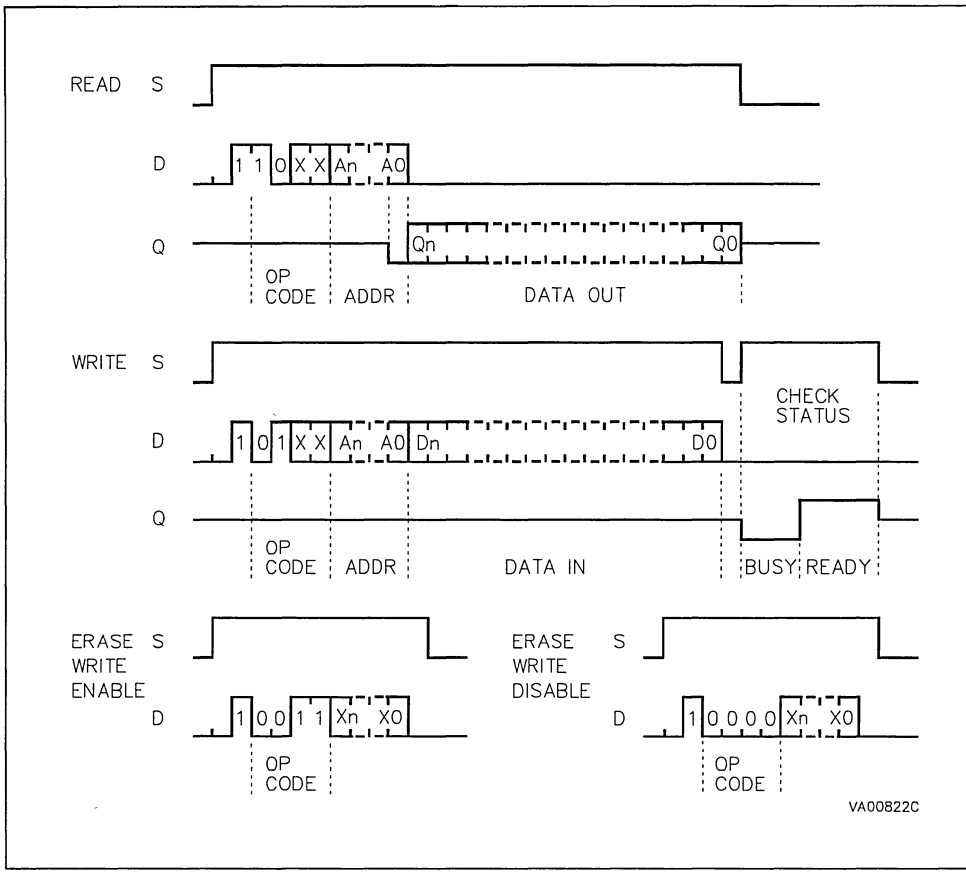
The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be

Table 7. Instruction Set

Instruction	Description	Op-Code	x8 Org Address (ORG = 0)	Data	x16 Org Address (ORG = 1)	Data
READ	Read Data from Memory	10XX	A4-A0	Q7-Q0	A3-A0	Q15-Q0
WRITE	Write Data to Memory	01XX	A4-A0	D7-D0	A3-A0	D15-D0
EWEN	Erase/Write Enable	0011	XXXXX		XXXX	
EWDS	Erase/Write Disable	0000	XXXXX		XXXX	
ERASE	Erase Byte or Word	11XX	XXXXX		XXXX	
ERAL	Erase All Memory	0010	XXXXX		XXXX	
WRAL	Write All Memory with same Data	0001	XXXXX	D7-D0	XXXX	D15-D0

Note: X = don't care bit.

Figure 6. READ, WRITE, EWEN, EWDS Sequences



Notes: 1. An: n = 5 for x16 org. and 6 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

executed, the Erase/Write Disable instruction (EWDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93C06 enters the Disable mode. When the Erase/Write Enable instruction (EWEN) is executed, Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or if the Power-on reset circuit becomes active due to a reduced V_{CC}. To protect the memory contents from accidental corruption, it is advisable to issue the EWDS instruction after every write cycle.

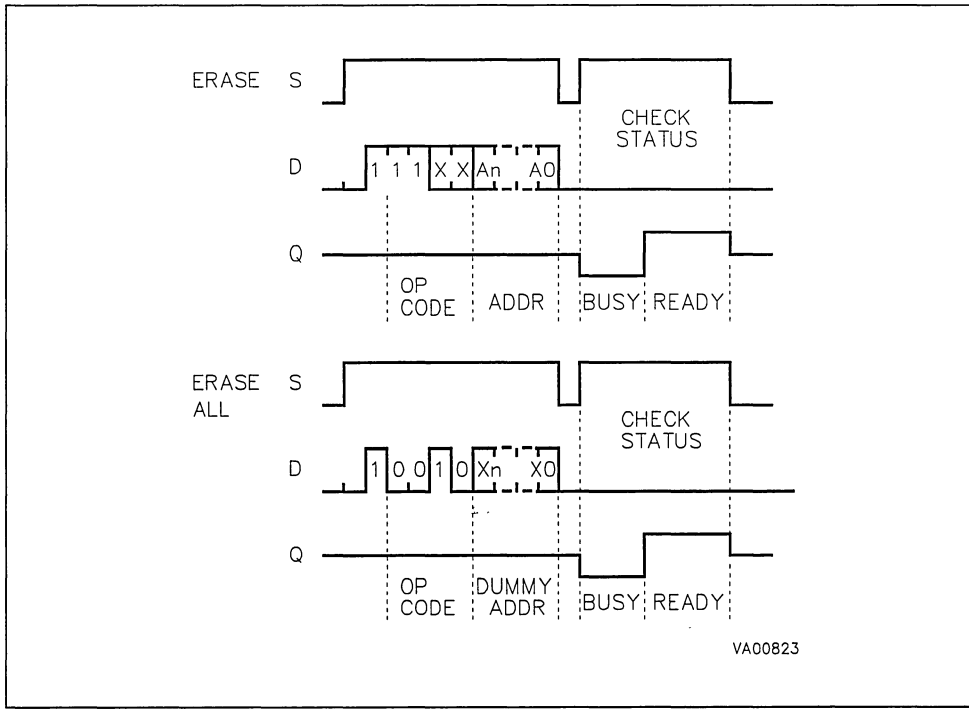
The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) triggers a self-timed erase cycle.

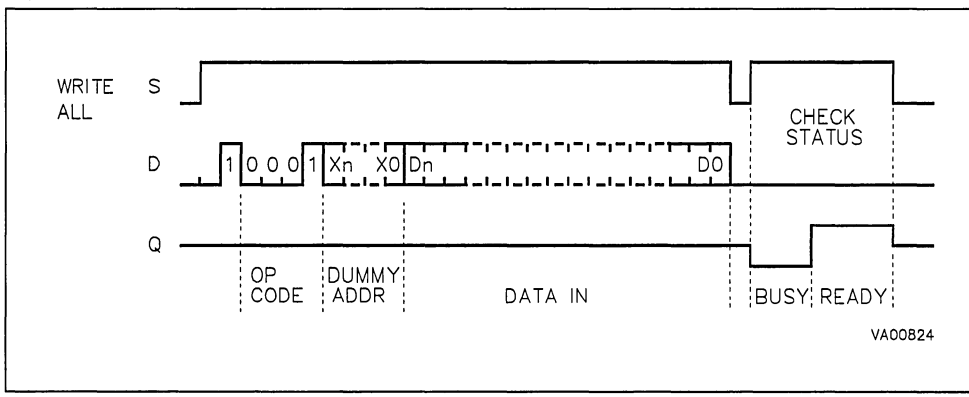
If the ST93C06 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction.

Figure 7. ERASE, ERAL Sequences



Notes: 1. An: n = 5 for x16 org. and 6 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

Figure 8. WRAL Sequence



Note: 1 Xn: n = 3 for x16 org. and 4 for x8 org.

INSTRUCTION (cont'd)

Write

The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C) in order to start the self-timed programming cycle. If the ST93C06 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a programming cycle) and does not require an Erase instruction prior to the Write instruction (The Write instruction includes an automatic erase cycle before programing data).

Erase All

The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to '1'). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction. If the ST93C06 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction.

Write All

For correct operation, an ERAL instruction should be executed before the WRAL instruction: the WRAL instruction DOES NOT perform an automatic erase before writing. The Write All instruction (WRAL) writes the Data Input byte or word to all the addresses of the memory. If the ST93C06 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction.

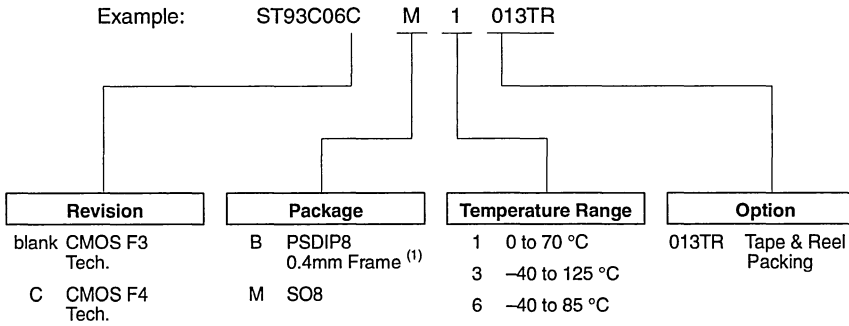
READY/BUSY Status

During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select (S) is driven High. Once the ST93C06 is Ready, the Ready/Busy status is available on the Data Output (Q) until a new start bit is decoded or the Chip Select (S) is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader may also refer to the SGS-THOMSON application note "Microwire

ORDERING INFORMATION SCHEME



Note: 1. ST93C08CB1 is available with 0.25mm lead Frame only.

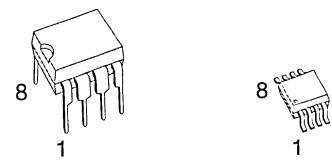
Parts are shipped with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

For a list of available options (Package, Temperature Range, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SERIAL ACCESS CMOS 1K bit (64 x 16 or 128 x 8) EEPROM

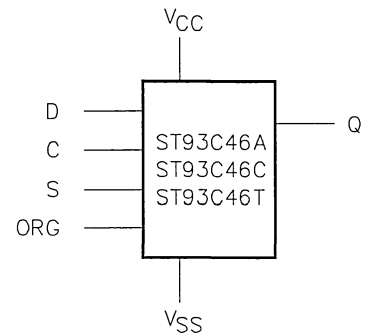
- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- DUAL ORGANIZATION: 64 x 16 or 128 x 8
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE
  - 5V ±10% for ST93C46A and ST93C46T versions
  - 3V to 5.5V for ST93C46C version
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ENHANCED ESD/LATCH UP PERFORMANCES for "C" VERSION



PSDIP8 (B)
0.4mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

This specification covers a range of 1K bit EEPROM products, the ST93C46A, ST93C46C and ST93C46T. In the text, products are referred to as ST93C46.

The ST93C46 is a 1K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input (D) and output (Q).

Table 1. Signal Names

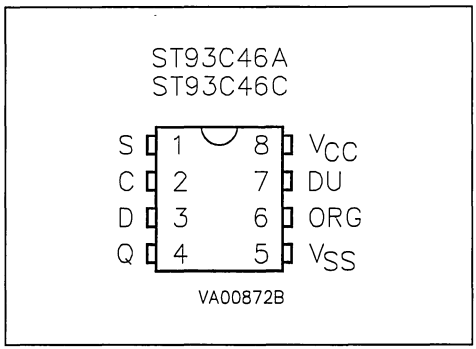
S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST93C46A,T ST93C46C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST93C46	500	V

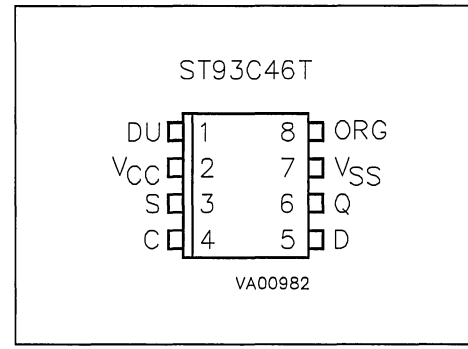
Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

Figure 2A. DIP Pin Connections



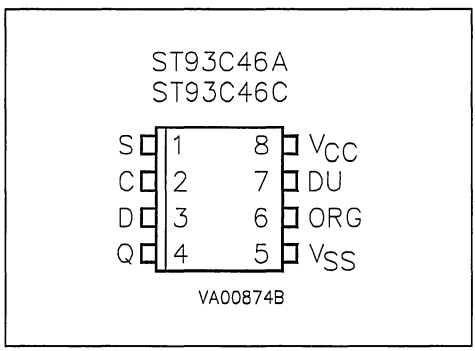
Warning: DU = Don't Use

Figure 2B. SO, 90° Turn, Pin Connections



Warning: DU = Don't Use

Figure 2C. SO Pin Connections



Warning: DU = Don't Use

DESCRIPTION (cont'd)

The 1K bit memory is divided into either 128 x 8 bit bytes or 64 x 16 bit words. The organization may be selected by a signal on the ORG input.

The memory is accessed by a set of instructions which includes Read a byte/word, Write a byte/word, Erase a byte/word, Erase All and Write All.

A Read instruction loads the address of the first byte/word to be read into an internal address pointer. The data is then clocked out serially.

The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93C46 can output a sequential stream of data bytes/words. In this way, the

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

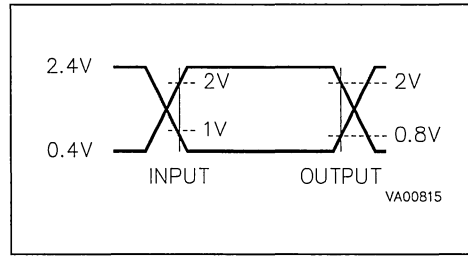


Table 3. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST93C46A, ST93C46T	1,000,000	10
ST93C46C	1,000,000	10

Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 5. DC Characteristics (T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10% for ST93C46A, C46T and V_{CC} = 3V to 5.5V for ST93C46C)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 6. AC Characteristics (T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10% for ST93C46A, C46T and V_{CC} = 3V to 5.5V for ST93C46C)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	Temp. Range: grade 1	100		ns
			Temp. Range: grades 3, 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			100	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

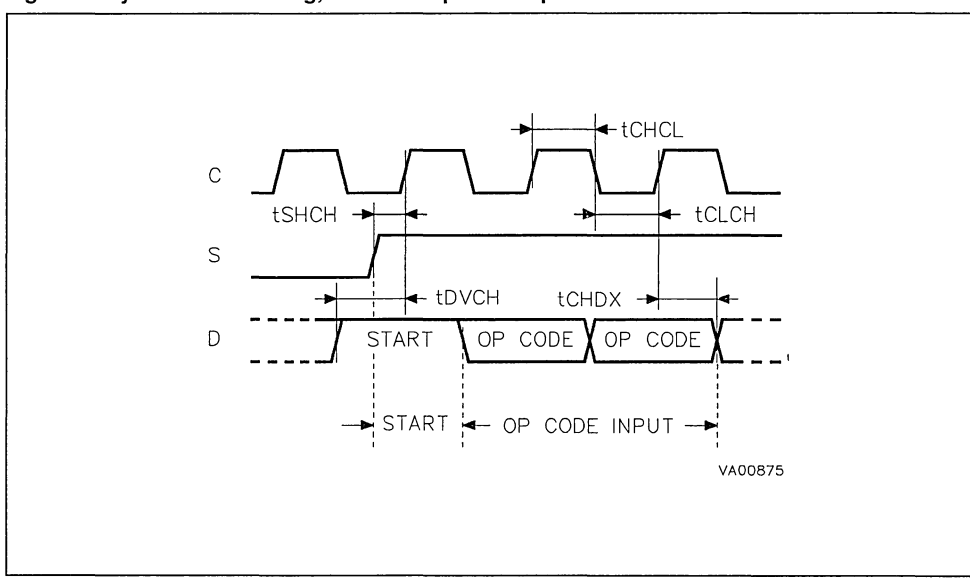
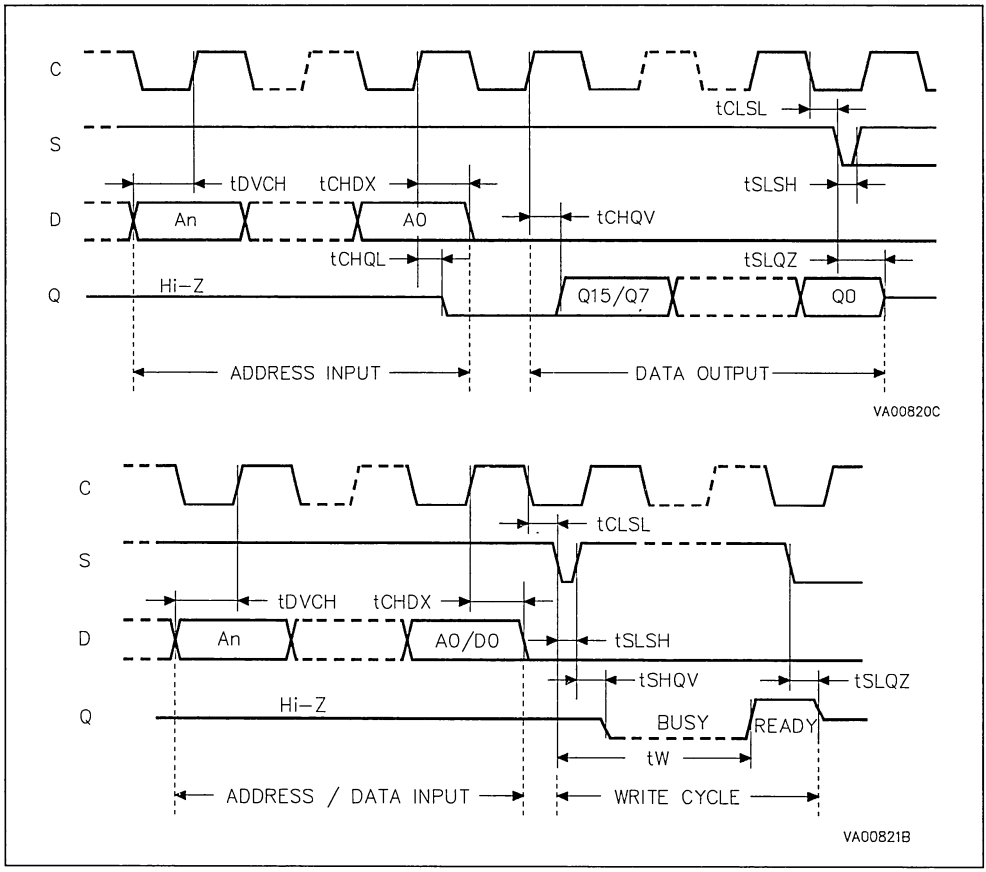


Figure 5. Synchronous Timing, Read or Write



DESCRIPTION (cont'd)

memory can be read as a data stream from 8 to 1024 bits long, or continuously as the address counter automatically rolls over to 00 when the highest address is reached.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the 128 bytes or 64 words. After the start of the programming cycle a Busy/Ready signal is available on the Data output (Q) when Chip Select (S) is High.

An internal feature of the ST93C46 provides Power-on Data Protection by inhibiting any operation when the Supply is too low.

The design of the ST93C46 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

MEMORY ORGANIZATION

The ST93C46 is organised as 128 bytes x 8 bits or 64 words x 16 bits. If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected, when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the ST93C46 is in standby mode, the ORG input should be unconnected or set to either V_{IL} or V_{IH} in order to get minimum power consumption. Any voltage between V_{IL} and V_{IH} applied to ORG may increase the standby current value.

POWER-ON DATA PROTECTION

During power-up, A Power On Reset sequence is run in order to reset all internal programming circuitry and the device is set in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction.

INSTRUCTIONS

The ST93C46 has seven instructions, as shown in Table 7. Each instruction Starts with the rising edge of the signal applied on the S input, followed by a '1' read on D input during the rising edge of the clock C. The op-codes of the instructions are made up of the 2 following bits. Some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is followed by an address for the byte/word which is made up of six bits for the x16 organization or seven bits for the x8 organization.

The ST93C46 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 6).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The ST93C46 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be executed, the Erase/Write Disable instruction (EWDS) freezes the execution of the following Erase/Write instructions. When power is first applied to the ST93C46, Erase/Write is inhibited. When the EWEN instruction is executed, Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or V_{CC} falls below the power-on reset threshold. To protect the memory contents from accidental corruption, it is advisable to issue the EWDS instruction after every write cycle.

The READ instruction is not affected by the EWEN or EWDS instructions.

Table 7. Instruction Set

Instruction	Description	Op-Code	x8 Org Address (ORG = 0)	Data	x16 Org Address (ORG = 1)	Data
READ	Read Data from Memory	10	A6-A0	Q7-Q0	A5-A0	Q15-Q0
WRITE	Write Data to Memory	01	A6-A0	D7-D0	A5-A0	D15-D0
EWEN	Erase/Write Enable	00	11XXXXX		11XXXX	
EWDS	Erase/Write Disable	00	00XXXXX		00XXXX	
ERASE	Erase Byte or Word	11	A6-A0		A5-A0	
ERAL	Erase All Memory	00	10XXXXX		10XXXX	
WRAL	Write All Memory with same Data	00	01XXXXX	D7-D0	01XXXX	D15-D0

Note: X = don't care bit.

Erase

The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) starts a self-timed programming cycle.

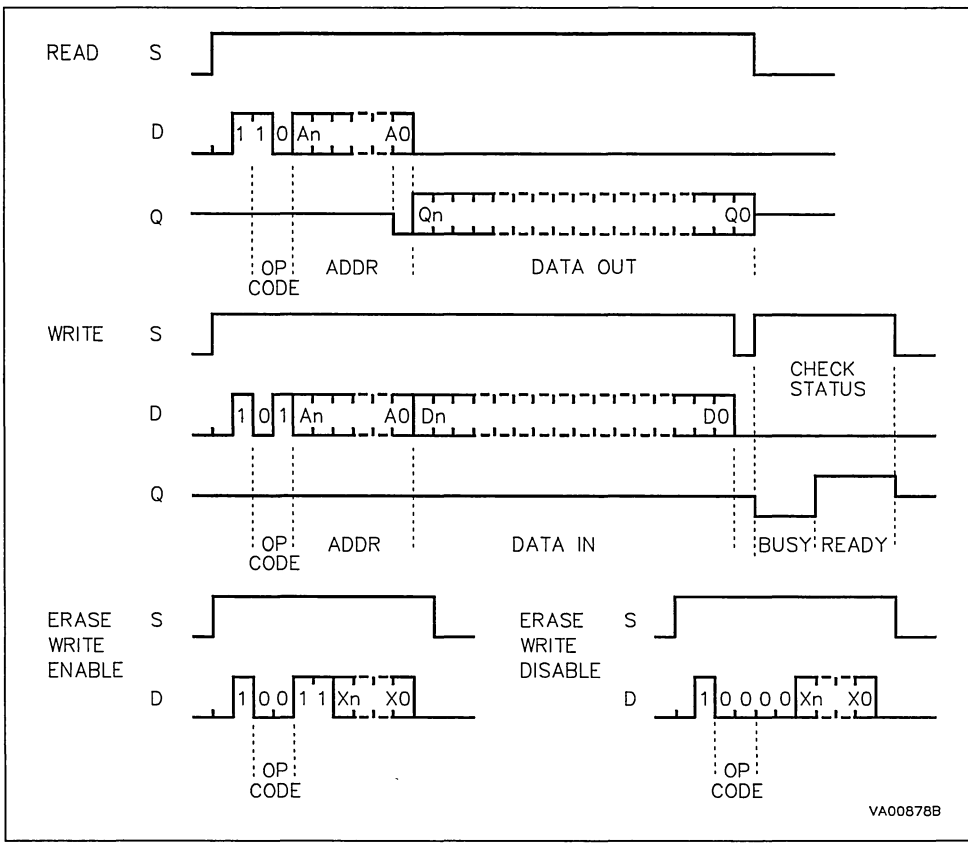
If the ST93C46 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C46 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C46 is ready to receive a new instruction.

Write

The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C), in order to start the self-timed programming cycle. If the ST93C46 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C46 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C46 is ready to receive a new instruction.

The Write instruction includes an automatic Erase cycle before writing the data, it is therefore unnecessary to execute an Erase instruction before a Write instruction execution.

Figure 6. READ, WRITE, EWEN, EWDS Sequences



Notes: 1. An: n = 5 for x16 org. and 6 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

Erase All

The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to "1"). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction above. If the ST93C46 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C46 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C46 is ready to receive a new instruction.

Write All

For correct operation, an ERAL instruction should be executed before the WRAL instruction.

The Write All instruction (WRAL) writes the Data Input byte or word to all the addresses of the memory. In the WRAL instruction, NO automatic erase is made so all bytes/words must be erased before the WRAL instruction. If the ST93C46 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C46 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C46 is ready to receive a new instruction.

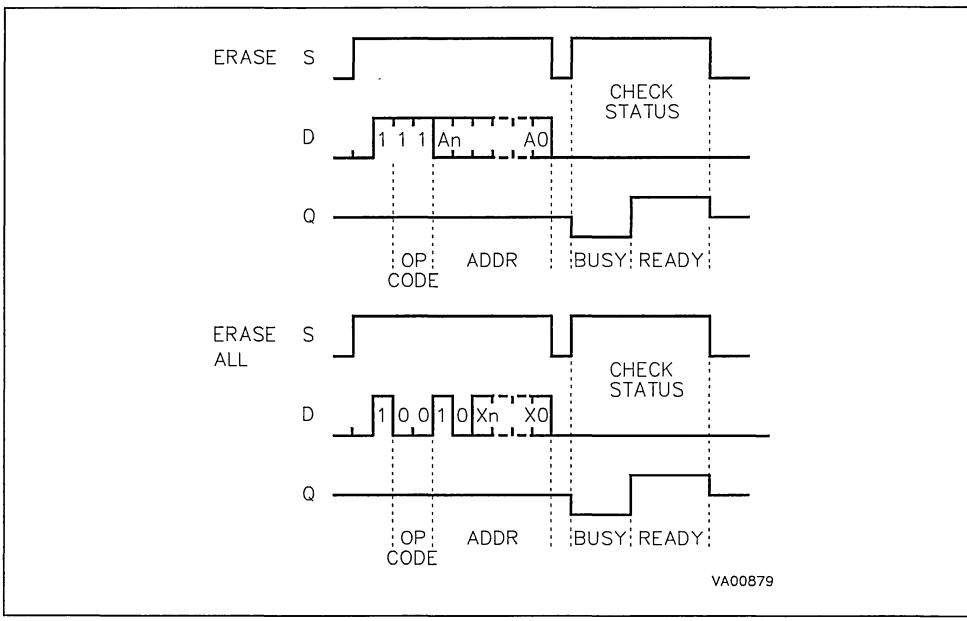
READY/BUSY Status

During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select is driven High. Once the ST93C46 is Ready, the Data Output is set to '1' until a new start bit is decoded or the Chip Select is brought Low.

COMMON I/O OPERATION

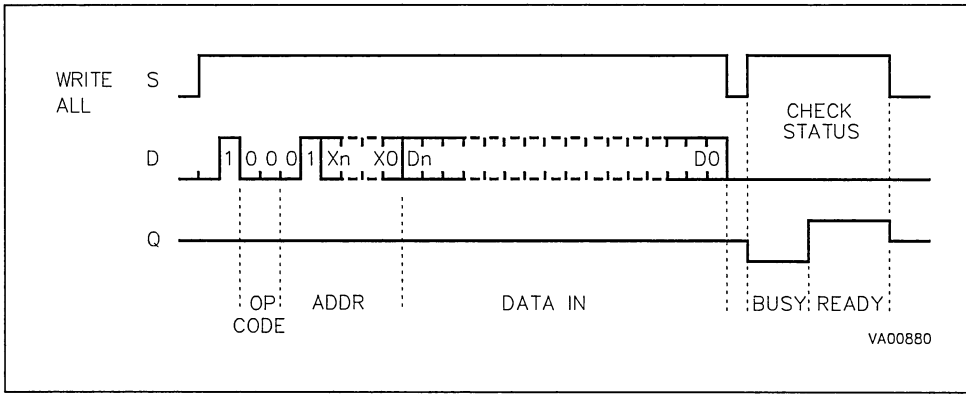
The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the SGS-THOMSON application note "Microwire EEPROM Common I/O Operation".

Figure 7. ERASE, ERAL Sequences



Notes: 1. An: n = 5 for x16 org. and 6 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

Figure 8. WRAL Sequence



Note: 1. Xn: n = 3 for x16 org. and 4 for x8 org.

ORDERING INFORMATION SCHEME

Example: ST93C46A M 1 013TR

Revision	Package	Temperature Range	Option
A CMOS F3 Tech.	B PSDIP8 0.4 mm Frame(1)	1 0 to 70 °C	013TR Tape & Reel Packing (A, T version)
C CMOS F4 Tech.	M SO8	3 –40 to 125 °C	TR Tape & Reel Packing (C version)
T CMOS F3 Tech. 90° Turn pin out		6 –40 to 85 °C	

Note: 1. ST93C46CB1 is available in 0.25mm lead Frame only.

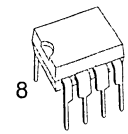
Parts are shipped with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

For a list of available options (Revision, Package etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SERIAL ACCESS CMOS 2K bit (128 x 16 or 256 x 8) EEPROM

- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- DUAL ORGANIZATION: 128 x 16 or 256 x 8
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE 5V ±10% SUPPLY VOLTAGE
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame

SO8 (M)

DESCRIPTION

The ST93C56 is a 2K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input (D).

The memory is divided into either 256 x 8 bit bytes or 128 x 16 bit words. The organization may be selected by a signal applied on the ORG input.

The memory is accessed by a set of instructions which includes Read a byte/word, Write a byte/word, Erase a byte/word, Erase All and Write All. A Read instruction loads the address of the first byte/word to be read into an internal address pointer. The data contained at this address is then clocked out serially. The address pointer is auto-

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

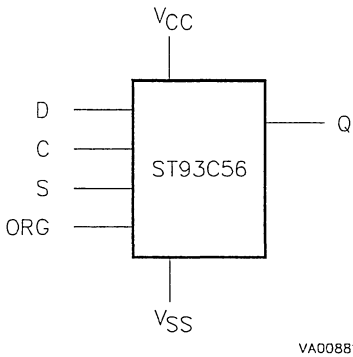
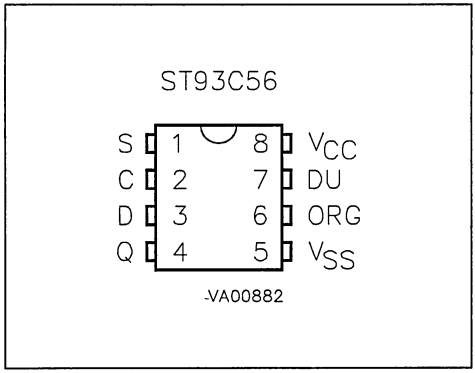
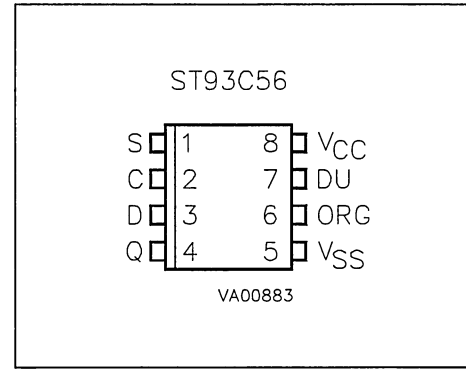


Figure 2A. DIP Pin Connections



Warning: DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			6000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

matically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93C56 can output a sequential stream of data bytes/words. In this way, the memory can be read as a data stream from 8 to 2048 bits long, or continuously as the address counter automatically rolls over to 00 when the highest address is reached.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the 256 bytes or 128 words. After the start of the programming cycle, a Busy/Ready signal is available on the Data output (Q) when Chip Select (S) is driven High.

The design of the ST93C56 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

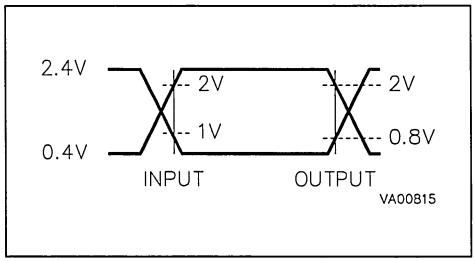


Table 3. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST93C56	1,000,000	10

Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 5. DC Characteristics (T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 6. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	Temp. Range: grade 1	100		ns
			Temp. Range: grades 3, 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			100	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns

Figure 4. Synchronous Timing, Start and Op-Code Input

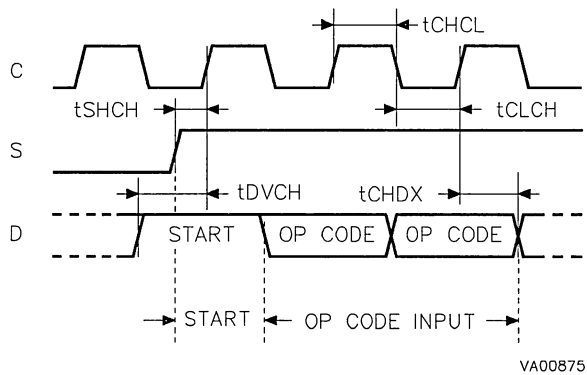
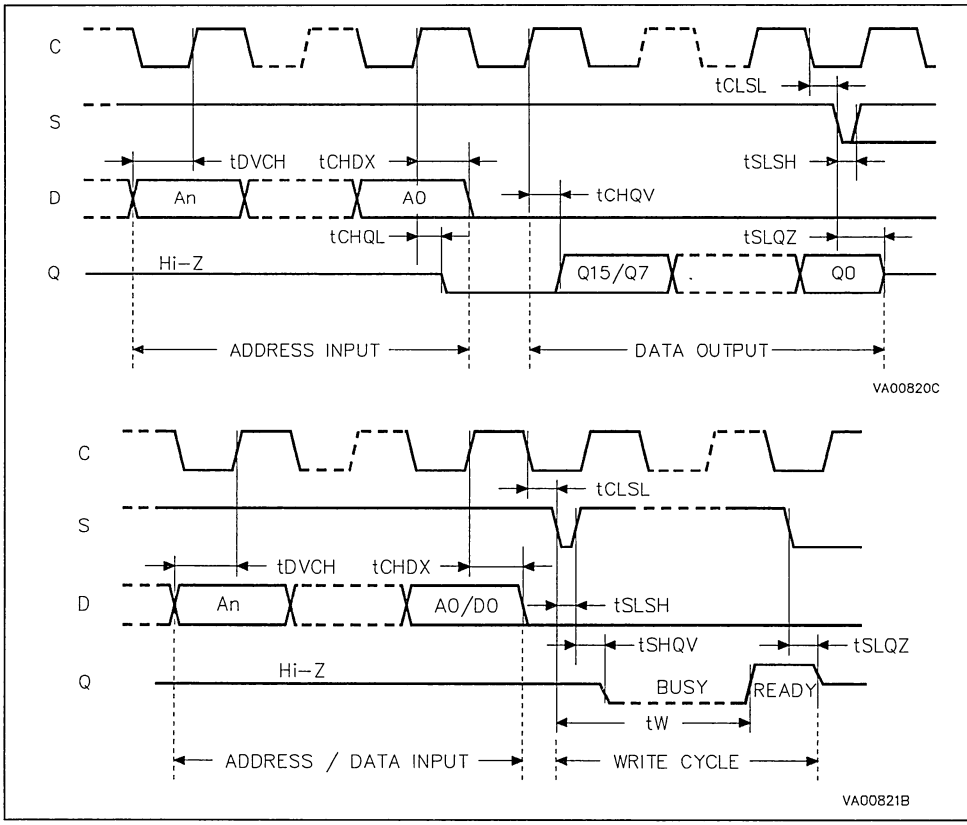


Figure 5. Synchronous Timing, Read or Write



MEMORY ORGANIZATION

The ST93C56 is organized as 256 bytes x 8 bits or 128 words x 16 bits. If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected, when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the ST93C56 is in standby mode, the ORG input should be unconnected or set to either V_{IL} or V_{IH} in order to achieve the minimum power consumption. Any voltage between V_{IL} and V_{IH} applied to ORG may increase the standby current value.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied, before applying any logic signal.

INSTRUCTIONS

The ST93C56 has seven instructions, as shown in Table 7. The op-codes of the instructions are made up of 2 bits. The op-code is followed by an address for the byte/word which is eight bits long for the x16 organization or nine bits long for the x8 organization. Each instruction starts with the rising edge of the signal applied on the Chip Select (S) input. The data input D is then sampled upon the following rising edges of the clock C untill a '1' is sampled and decoded by the ST93C56 as a Start bit.

The ST93C56 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 6).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first, followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The ST93C56 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be executed, the Erase/Write Disable instruction (EWDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93C56 enters the Disable mode. When the EWEN instruction is executed, Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or V_{CC} falls below the power-on reset threshold. To protect the memory contents from accidental corruption, it is advisable to issue the EWDS instruction after every write cycle.

The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) triggers a self-timed erase cycle.

If the ST93C56 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C56 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C56 is ready to receive a new instruction.

Write

The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C) in order to start the self-timed programming cycle. If the ST93C56 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C56 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C56 is ready to receive a new instruction. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a programming cycle) and does not require an Erase instruction prior to the Write instruction (The Write instruction includes an automatic erase cycle before programing data).

Erase All

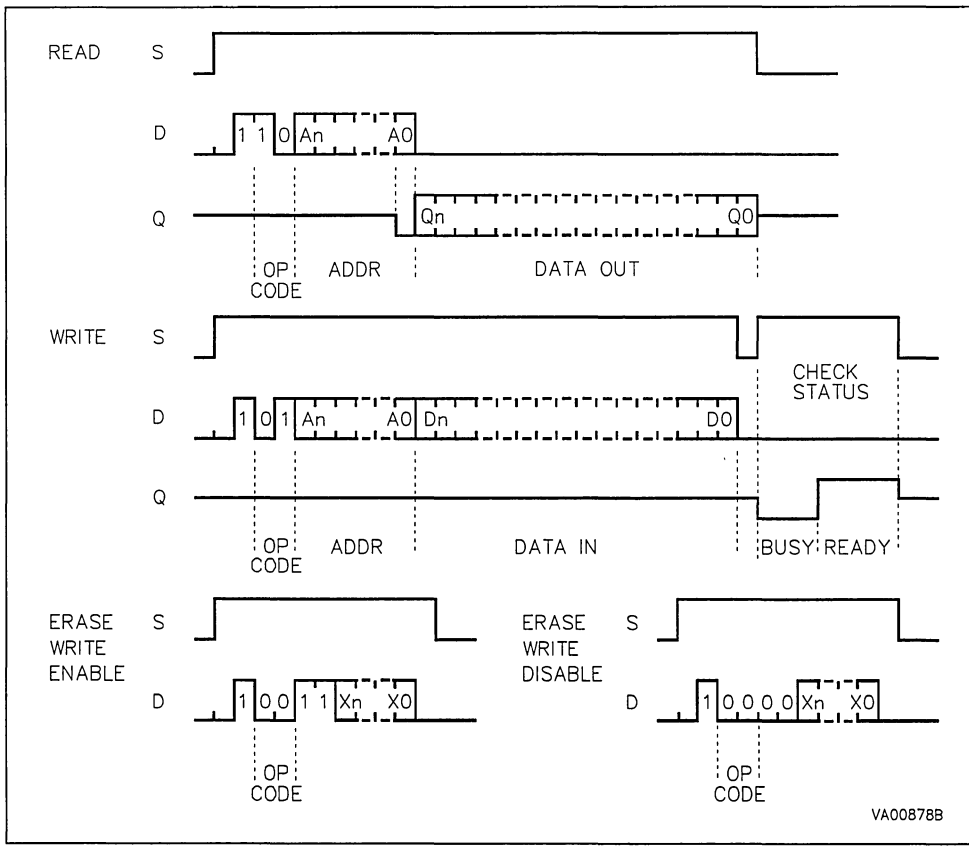
The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to '1'). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction. If the ST93C56 is still performing the

Table 7. Instruction Set

Instruction	Description	Op-Code	x8 Org Address (ORG = 0) (1, 2)	Data	x16 Org Address (ORG = 1) (1, 3)	Data
READ	Read Data from Memory	10	A8-A0	Q7-Q0	A7-A0	Q15-Q0
WRITE	Write Data to Memory	01	A8-A0	D7-D0	A7-A0	D15-D0
EWEN	Erase/Write Enable	00	11XXX XXXX		11XX XXXX	
EWDS	Erase/Write Disable	00	00XXX XXXX		00XX XXXX	
ERASE	Erase Byte or Word	11	A8-A0		A7-A0	
ERAL	Erase All Memory	00	10XXX XXXX		10XX XXXX	
WRAL	Write All Memory with same Data	00	01XXX XXXX	D7-D0	01XX XXXX	D15-D0

Notes: 1. X = don't care bit.
2. Address bit A8 is not decoded by the ST93C56.
3. Address bit A7 is not decoded by the ST93C56.

Figure 6. READ, WRITE, EWEN, EWDS Sequences



Notes: 1. An: n = 5 for x16 org. and 6 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C56 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C56 is ready to receive a new instruction.

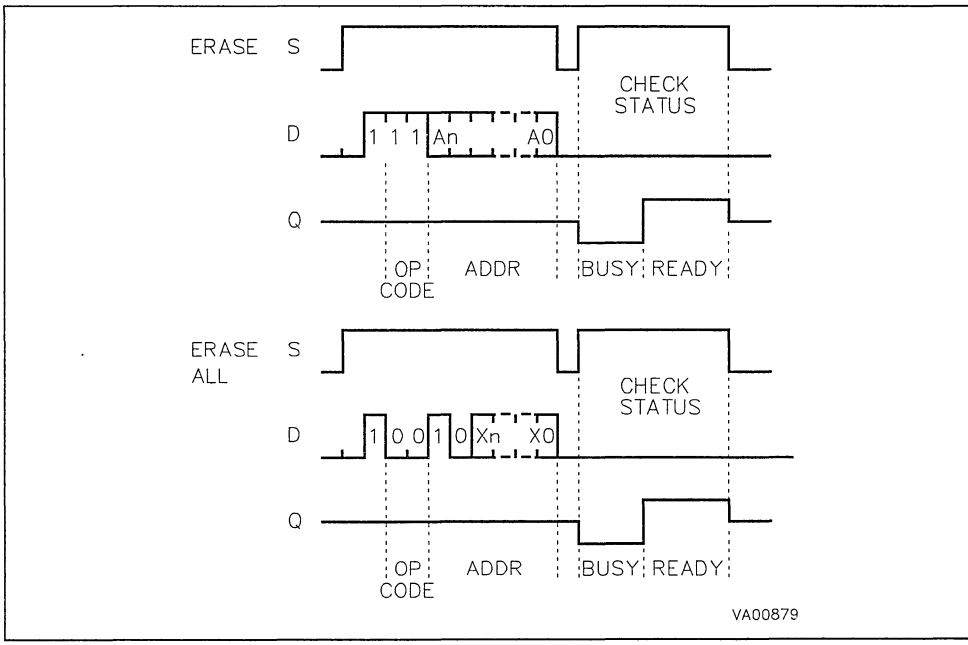
Write All

For correct operation, an ERAL instruction should be executed before the WRAL instruction: the WRAL instruction DOES NOT perform an automatic erase before writing. The Write All instruction (WRAL) writes the Data Input byte or word to all the addresses of the memory. If the ST93C56 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C56 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C56 is ready to receive a new instruction.

READY/BUSY Status

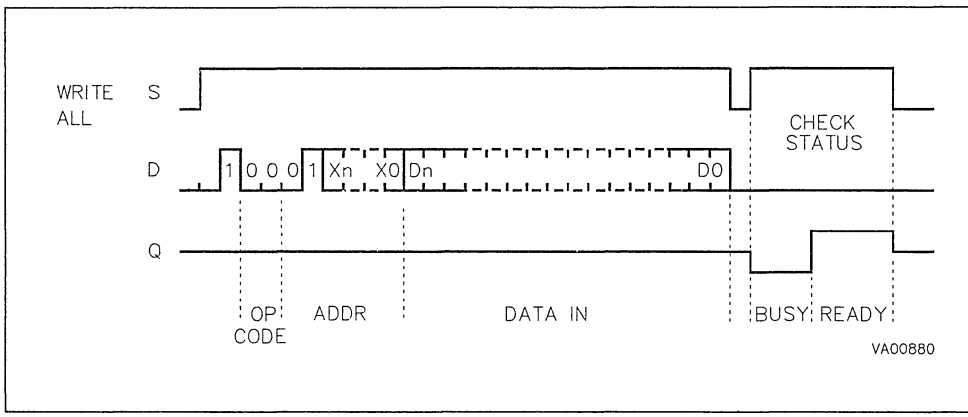
During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select (S) is driven High. Once the ST93C56 is Ready, the Ready/Busy status is available on the Data Output (Q) until a new start bit is decoded or the Chip Select (S) is brought Low.

Figure 7. ERASE, ERAL Sequences



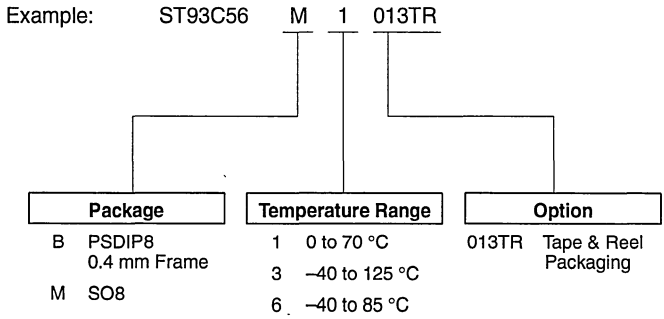
Notes: 1 An: n = 5 for x16 org. and 6 for x8 org.
2. Xn: n = 3 for x16 org and 4 for x8 org.

Figure 8. WRAL Sequence



Notes: 1 Xn: n = 3 for x16 org. and 4 for x8 org.

ORDERING INFORMATION SCHEME



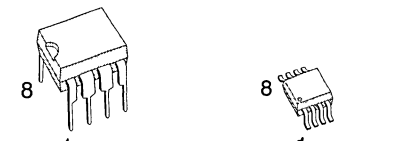
Parts are shipped with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

For a list of available options (Package, Temperature Range etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SERIAL ACCESS CMOS 4K bit (256 x 16 or 512 x 8) EEPROM

- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- DUAL ORGANIZATION: 256 x 16 or 512 x 8
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE 3V to 5.5V SUPPLY VOLTAGE
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame

SO8 (M)

DESCRIPTION

The ST93C66 is a 4K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input (D).

The memory is divided into either 512 x 8 bit bytes or 256 x 16 bit words. The organization may be selected by a signal applied on the ORG input.

The memory is accessed by a set of instructions which includes Read a byte/word, Write a byte/word, Erase a byte/word, Erase All and Write All. A Read instruction loads the address of the first byte/word to be read into an internal address pointer. The data contained at this address is then clocked out serially.

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

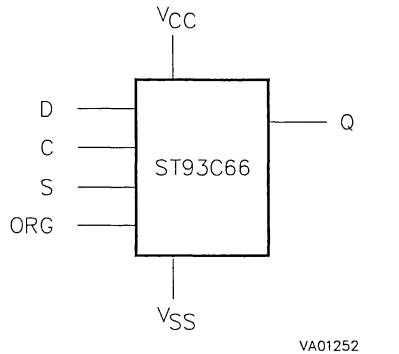
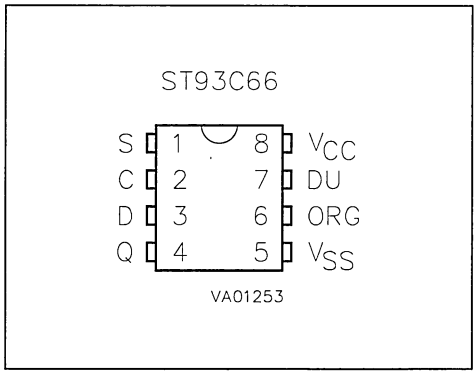
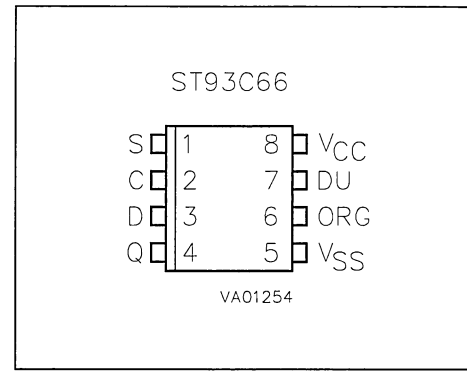


Figure 2A. DIP Pin Connections



Warning: DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 3 grade 6	–40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93C66 can output a sequential stream of data bytes/words. In this way, the memory can be read as a data stream from 8 to 4096 bits long, or continuously as the address counter automatically rolls over to 00 when the highest address is reached.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the 512 bytes or 256 words.

After the start of the programming cycle, a Busy/Ready signal is available on the Data output (Q) when Chip Select (S) is driven High.

The design of the ST93C66 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

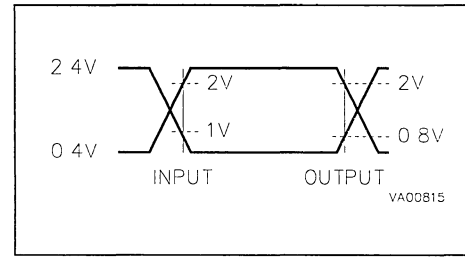


Table 3. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST93C66	1,000,000	10

Table 4. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested

Table 5. DC Characteristics (T_A = –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage	4.5V ≤ V_{CC} ≤ 5.5V	–0.1	0.8	V
		3V ≤ V_{CC} ≤ 4.5V	–0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage	4.5V ≤ V_{CC} ≤ 5.5V	2	V_{CC} + 1	V
		3V ≤ V_{CC} ≤ 4.5V	0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 6. AC Characteristics
(T_A = –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	tDIH	Clock High to Input Transition		200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			100	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

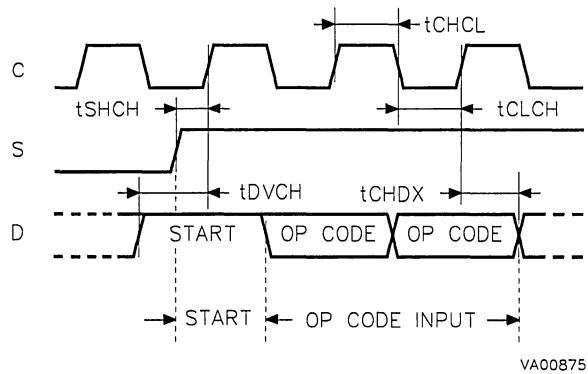
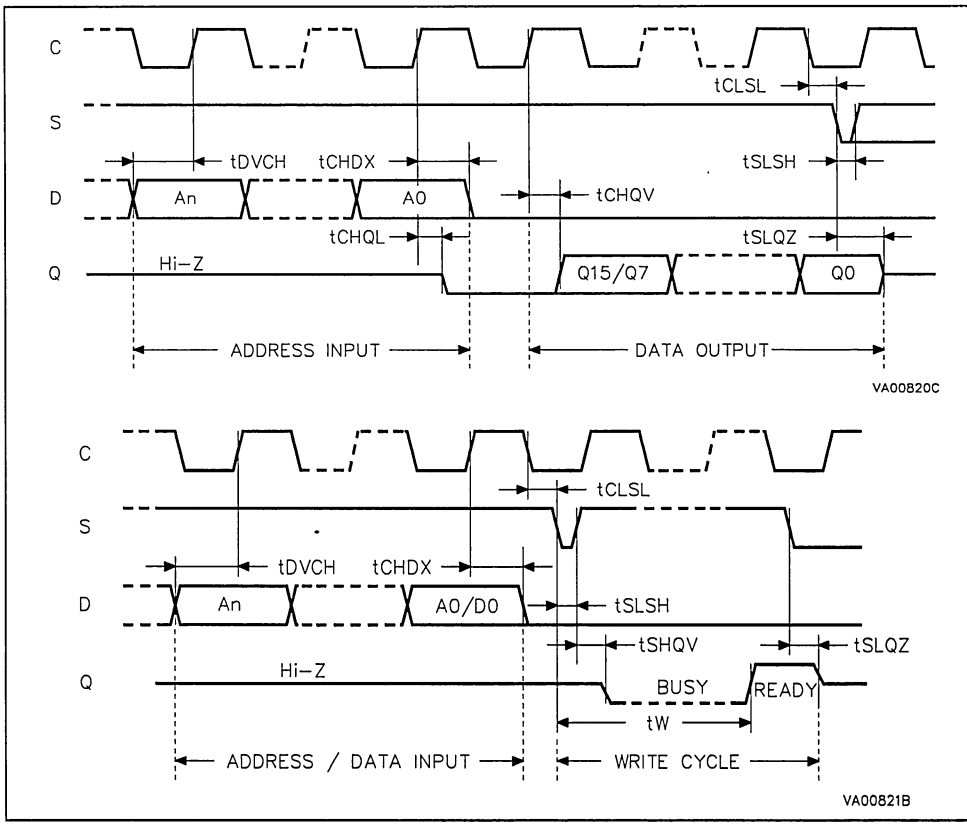


Figure 5. Synchronous Timing, Read or Write



MEMORY ORGANIZATION

The ST93C66 is organized as 512 bytes x 8 bits or 256 words x 16 bits. If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected, when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the ST93C66 is in standby mode, the ORG input should be unconnected or set to either V_{IL} or V_{IH} in order to achieve the minimum power consumption. Any voltage between V_{IL} and V_{IH} applied to ORG may increase the standby current value.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied, before applying any logic signal.

INSTRUCTIONS

The ST93C66 has seven instructions, as shown in Table 7. The op-codes of the instructions are made up of 2 bits. The op-code is followed by an address for the byte/word which is eight bits long for the x16 organization or nine bits long for the x8 organization. Each instruction starts with the rising edge of the signal applied on the Chip Select (S) input. The data input D is then sampled upon the following rising edges of the clock C untill a '1' is sampled and decoded by the ST93C66 as a Start bit.

The ST93C66 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 6).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first, followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The ST93C66 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be executed, the Erase/Write Disable instruction (EWDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93C66 enters the Disable mode. When the EWEN instruction is executed, Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or V_{CC} falls below the power-on reset threshold. To protect the memory contents from accidental corruption, it is advisable to issue the EWDS instruction after every write cycle.

The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) triggers a self-timed erase cycle.

If the ST93C66 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C66 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C66 is ready to receive a new instruction.

Write

The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C) in order to start the self-timed programming cycle. If the ST93C66 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C66 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C66 is ready to receive a new instruction. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a programming cycle) and does not require an Erase instruction prior to the Write instruction (The Write instruction includes an automatic erase cycle before programing data).

Erase All

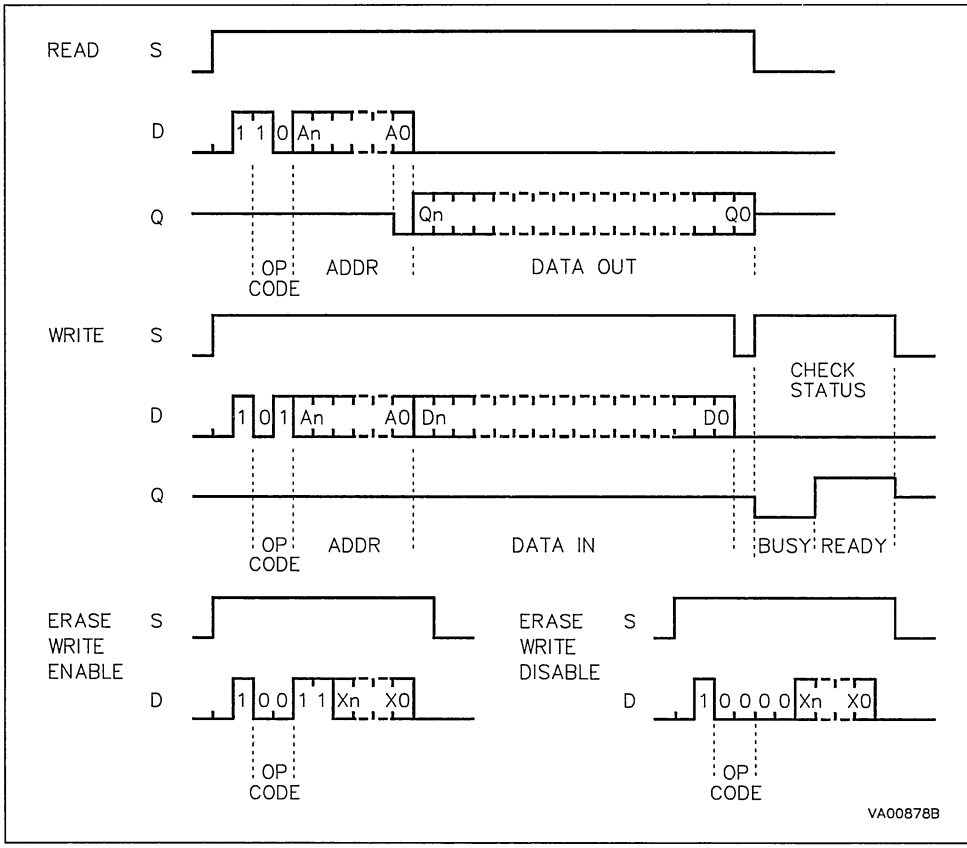
The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to '1'). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction. If the ST93C66 is still performing the

Table 7. Instruction Set

Instruction	Description	Op-Code	x8 Org Address (ORG = 0) (1)	Data	x16 Org Address (ORG = 1) (1)	Data
READ	Read Data from Memory	10	A8-A0	Q7-Q0	A7-A0	Q15-Q0
WRITE	Write Data to Memory	01	A8-A0	D7-D0	A7-A0	D15-D0
EWEN	Erase/Write Enable	00	11XXX XXXX		11XX XXXX	
EWDS	Erase/Write Disable	00	00XXX XXXX		00XX XXXX	
ERASE	Erase Byte or Word	11	A8-A0		A7-A0	
ERAL	Erase All Memory	00	10XXX XXXX		10XX XXXX	
WRAL	Write All Memory with same Data	00	01XXX XXXX	D7-D0	01XX XXXX	D15-D0

Note: 1. X = don't care bit.

Figure 6. READ, WRITE, EWEN, EWDS Sequences



erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C66 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C66 is ready to receive a new instruction.

Write All

For correct operation, an ERAL instruction should be executed before the WRAL instruction: the WRAL instruction DOES NOT perform an automatic erase before writing. The Write All instruction (WRAL) writes the Data Input byte or word to all the addresses of the memory. If the ST93C66 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C66 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C66 is ready to receive a new instruction.

READY/BUSY Status

During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select (S) is driven High. Once the ST93C66 is Ready, the Ready/Busy status is available on the Data Output (Q) until a new start bit is decoded or the Chip Select (S) is brought Low.

Figure 7. ERASE, ERAL Sequences

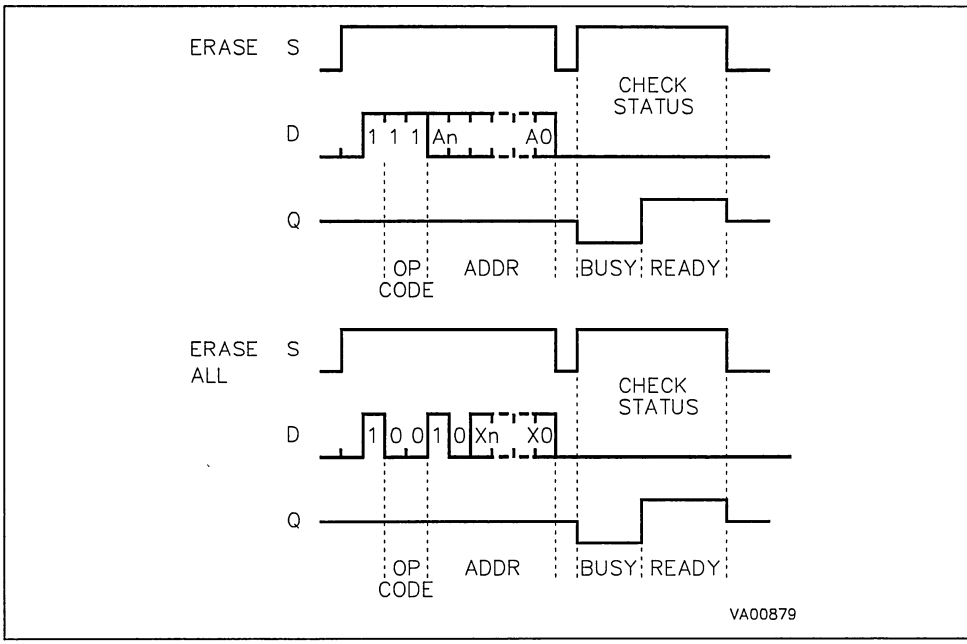
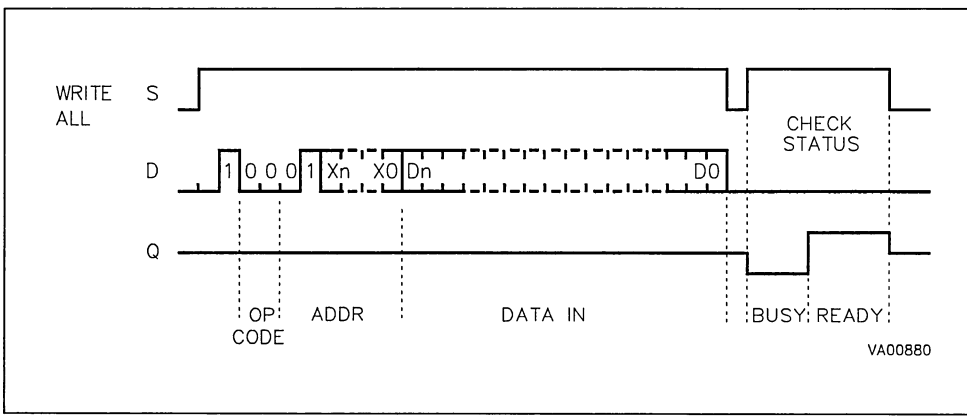
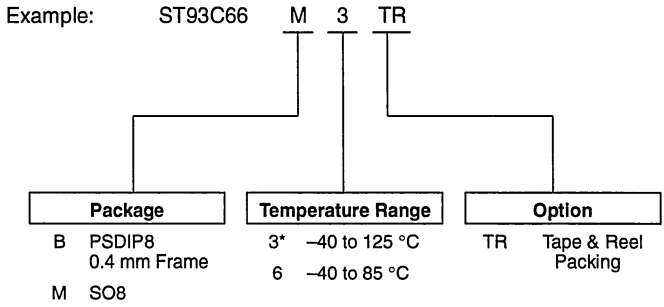


Figure 8. WRAL Sequence



ORDERING INFORMATION SCHEME



Note: 3* Temperature range on request only.

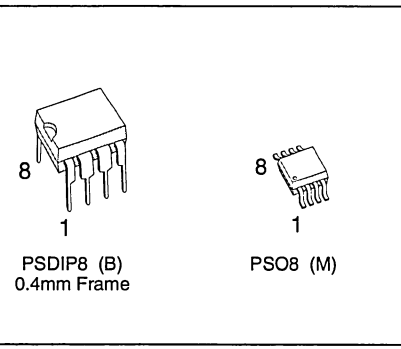
Parts are shipped with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

For a list of available options (Package, Temperature Range etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SERIAL ACCESS CMOS 1K bit (64 x 16) EEPROM

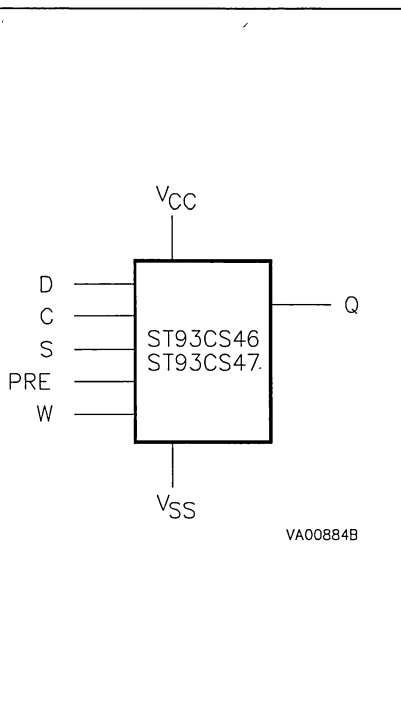
- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE
  - 3V to 5.5V for the ST93CS46
  - 2.5V to 5.5V for the ST93CS47
- USER DEFINED WRITE PROTECTED AREA
- PAGE WRITE MODE (4 WORDS)
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame

PSO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST93CS46 and ST93CS47 are 1K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input D and output Q.

The 1K bit memory is organized as 64 x 16 bit words.The memory is accessed by a set of instructions which include Read, Write, Page Write, Write All and instructions used to set the memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer.

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

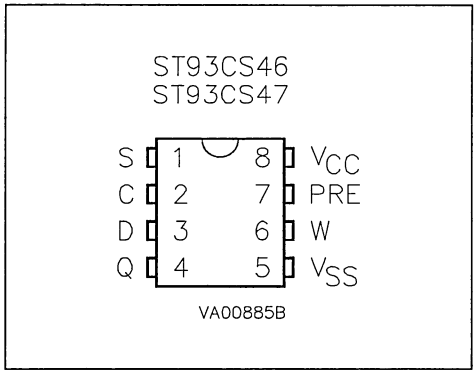


Figure 2B. SO Pin Connections

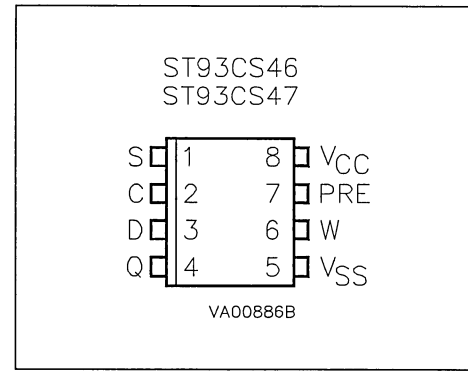


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			3000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The data is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93CS46/47 can output a sequential stream of data words. In this way, the memory can be read as a data stream of 16 to 1024 bits, or continuously as the address counter automatically rolls over to 00 when the highest address is reached. Within the time required by a programming cycle (t_W), up to 4 words may be written with the help of the Page Write instruction; the whole memory may also be erased, or set to a predetermined pattern, by using the Write All instruction.

Within the memory, an user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protect Register, located outside of the memory array. As a final protection step, data may be permanently protected by programming a One Time Programing bit (OTP bit) which locks the Protect Register content.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruc-

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

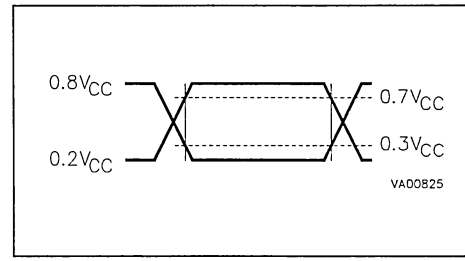


Table 3. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST93CS46, ST93CS47	1,000,000	10

Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 5. DC Characteristics (T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V for ST93CS46 and V_{CC} = 2.5V to 5.5V for ST93CS47)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}		50	µA
V_{IL}	Input Low Voltage (ST93CS46,47)	$4.5V \le V_{CC} \le 5.5V$	–0.1	0.8	V
	Input Low Voltage (ST93CS46)	$3V \le V_{CC} \le 5.5V$	–0.1	0.2 V_{CC}	V
	Input Low Voltage (ST93CS47)	$2.5V \le V_{CC} \le 5.5V$	–0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage (ST93CS46,47)	$4.5V \le V_{CC} \le 5.5V$	2	V_{CC} + 1	V
	Input High Voltage (ST93CS46)	$3V \le V_{CC} \le 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
	Input High Voltage (ST93CS47)	$2.5V \le V_{CC} \le 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 6. DC Characteristics (T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V for ST93CS46 and V_{CC} = 2.5V to 5.5V for ST93CS47)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			100	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

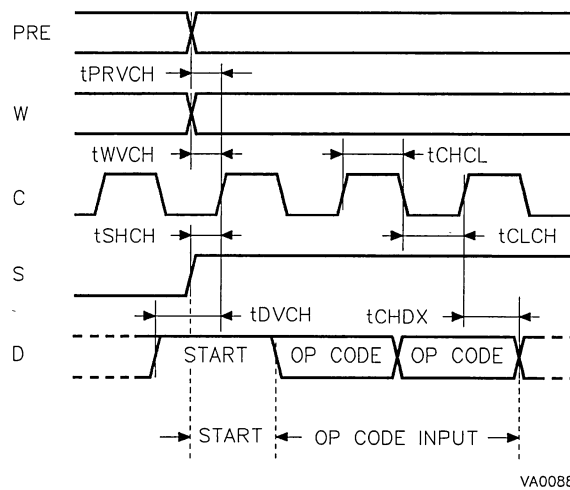
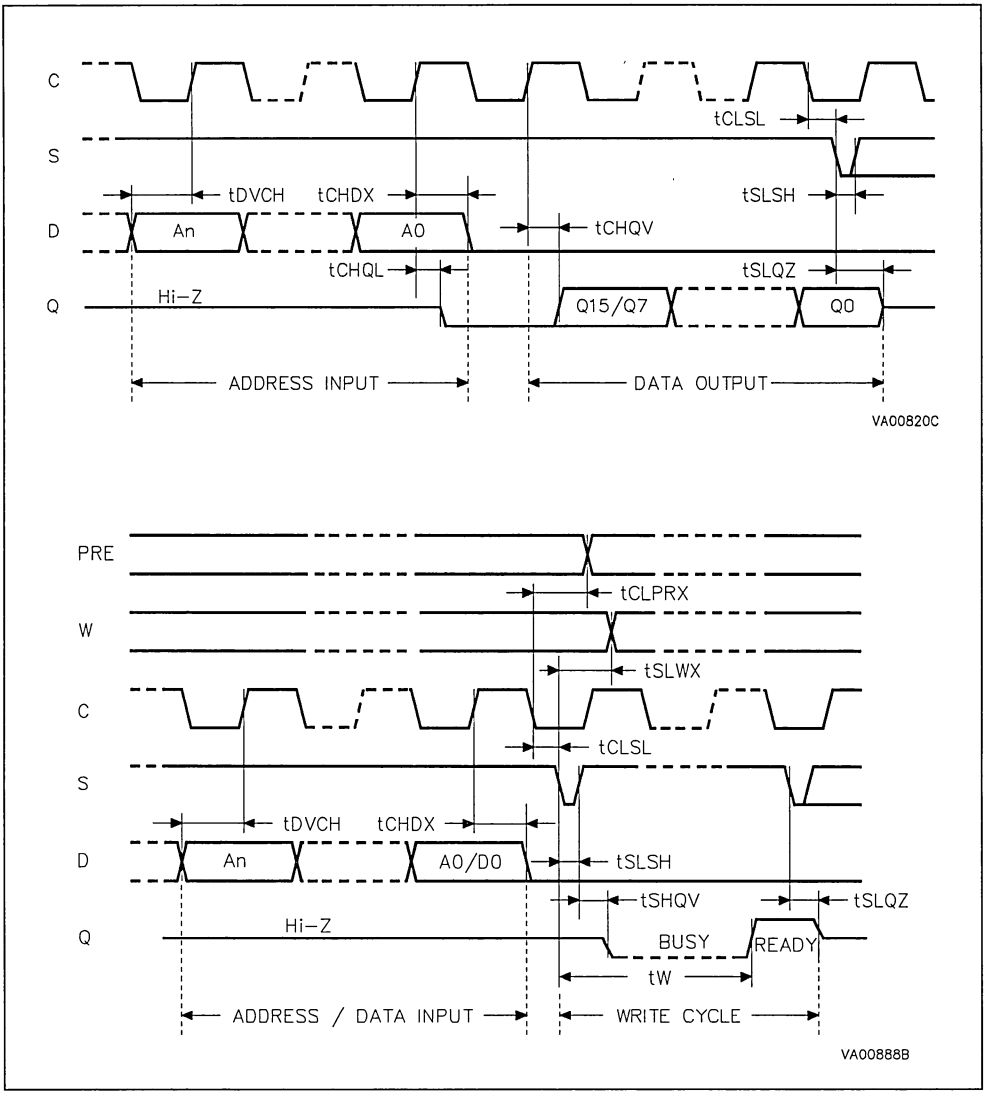


Figure 5. Synchronous Timing, Read or Write



DESCRIPTION (cont'd)

tion. The Write instruction writes 16 bits at one time into one of the 64 words, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, assuming in both cases that all addresses are outside the Write Protected area.

After the start of the programming cycle, a Ready/Busy signal is available on the Data output (Q) when the Chip Select (S) input pin is driven High.

The design of the ST93CS46/47 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied before any logic signal.

INSTRUCTIONS

The ST93CS46/47 has eleven instructions, as shown in Table 7. Each instruction starts with the rising edge of the signal applied on the Chip Select input (S), followed by a '1' read on D input during the rising edge of the clock C. The op-codes of the instructions are made up of the 2 following bits. Some instructions use only these first two bits, others use also the first two bits of the address field to define the op-code. The address field is six bits long (A5-A0).

The ST93CS46/47 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 6).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first. Output data changes are triggered by the Low to

Table 7. Instruction Set

Instruction	Description	W Pin (1)	PRE Pin	Op Code	Address (1)	Data	Additional Information
READ	Read Data from Memory	X	'0'	10	A5-A0	Q15-Q0	
WRITE	Write Data to Memory	'1'	'0'	01	A5-A0	D15-D0	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	'1'	'0'	11	A5-A0	D15-D0	Write is executed if all the addresses are not inside the Protected area
WRALL	Write All Memory	'1'	'0'	00	01XXXX	D15-D0	Write all data if the Protect Register is cleared
WEN	Write Enable	'1'	'0'	00	11XXXX		
WDS	Write Disable	'1'	'0'	00	00XXXX		
PRREAD	Protect Register Read	X	'1'	10	XXXXXX	Q8-Q0	Data Output = Protect Register content + Protect Flag bit
PRWRITE	Protect Register Write	'1'	'1'	01	A5-A0		Data above specified address A5-A0 are protected
PRCLEAR	Protect Register Clear	'1'	'1'	11	111111		Protect Flag is also cleared (cleared Flag = 1)
PREN	Protect Register Enable	'1'	'1'	00	11XXXX		
PRDS	Protect Register Disable	'1'	'1'	00	000000		OTP bit is set permanently

Note: 1. X = don't care bit.

INSTRUCTIONS (cont'd)

High transition of the Clock (C). The ST93CS46/47 will automatically increment the address and will clock out the next word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable and Write Disable

The Write Enable instruction (WEN) authorizes the following Write instructions to be executed, the Write Disable instruction (WDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93CS46/47 enters the Disable mode. When the Write Enable instruction (WEN) is executed, Write instructions remain enabled until a Write Disable instruction (WDS) is executed or if the Power-on reset circuit becomes active due to a reduced V_{CC}. To protect the memory contents from accidental corruption, it is advisable to issue the WDS instruction after every write cycle.

The READ instruction is not affected by the WEN or WDS instructions.

Write

The Write instruction (WRITE) is followed by the address and the word to be written. The Write Enable signal (W) must be held high during the WRITE instruction. Data input D is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C), in order to start the self-timed programming cycle, providing that the address is NOT in the protected area. If the ST93CS46/47 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS46/47 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS46/47 is ready to receive a new instruction.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be held High during the Write instruction. Input address and data are read on the Low to High transition of the clock. After the receipt of each data word, bits A1-A0 of the internal address register are incremented, the high order bits A5-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same four upper order address bits as the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The Page Write operation will not be performed if any of the 4 words is addressing the protected area. If the ST93CS46/47 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS46/47 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS46/47 is ready to receive a new instruction.

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes the whole memory with the same data word included in the instruction. The Write Enable signal (W) must be held High before and during the Write instruction. Input address and data are read on the Low to High transition of the clock. If the ST93CS46/47 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS46/47 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS46/47 is ready to receive a new instruction.

MEMORY WRITE PROTECTION AND PROTECT REGISTER

The ST93CS46/47 offers a Protect Register containing the bottom address of the memory area which has to be protected against write instructions. In addition to this Protect Register, two flag bits are used to indicate the Protect Register status: the Protect Flag enabling/disabling the protection of the Protect Register and the OTP bit which, when set, disables access to the Protect Register and thus prevents any further modifications of this Protect Register value. The content of the Protect Register is defined when using the PRWRITE instruction, it may be read when using the PRREAD instruction. A specific instruction PREN (Protect Register Enable) allows the user to execute the protect instructions PRCLEAR, PRWRITE and PRDS; this PREN instruction being used together with the signals applied on the input pins PRE

Figure 6. READ, WRITE, WEN, WDS Sequences

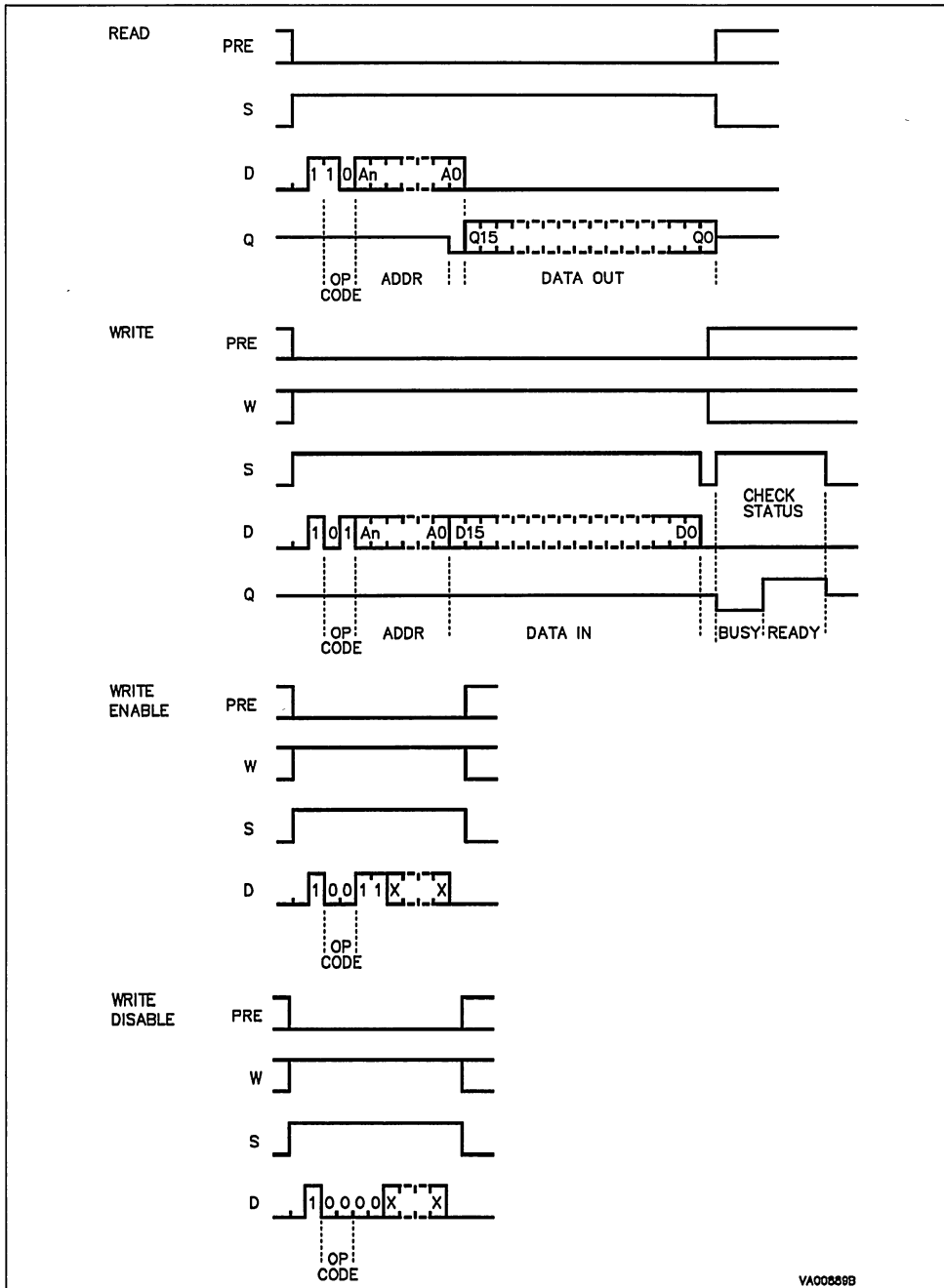
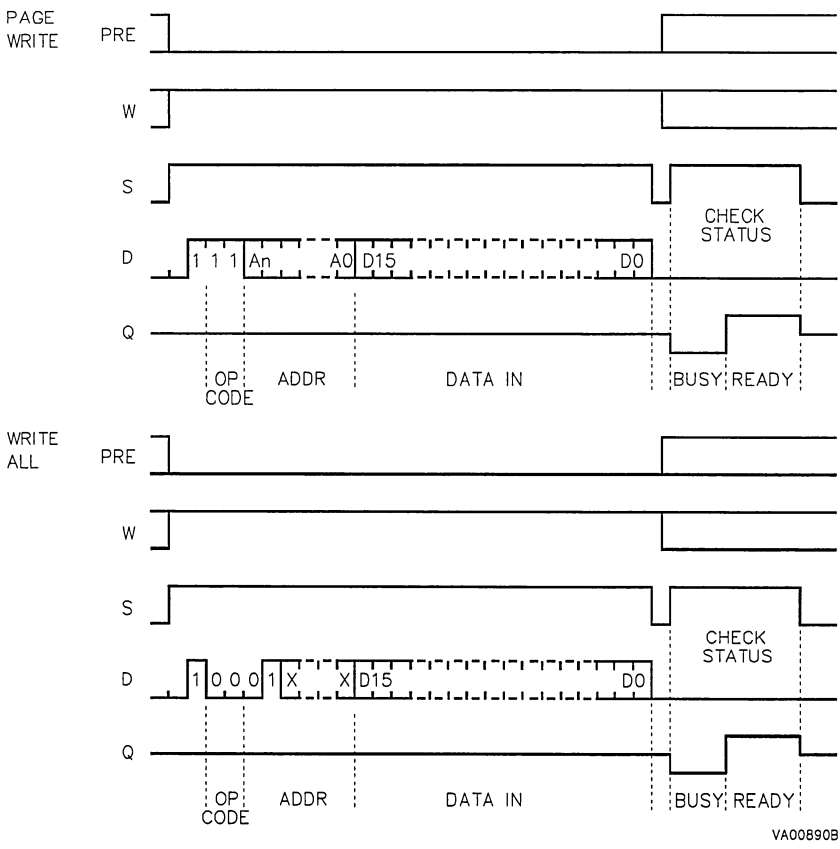


Figure 7. PRWRITE, WRALL Sequences



MEMORY WRITE PROTECTION (cont'd)

(Protect Register Enable pin) and W (Write Enable).

Accessing the Protect Register is done by executing the following sequence:

- WEN: execute the Write Enable instruction,
- PREN: execute the PREN instruction,
- PRWRITE, PRCLEAR or PRDS: the protection then may be defined, in terms of size of the protected area (PRWRITE, PRCLEAR) and may be set permanently (PRDS instruction).

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the content of the Protect Register, followed by the Protect Flag bit. The Protect Register Enable pin (PRE) must be driven High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish if the Protect Register is cleared (all 1's) or if it is written with all 1's, user must check the Protect Flag status (and not the Protect Register content) to ascertain the setting of the memory protection.

Protect Register Enable

The Protect Register Enable instruction (PREN) is used to authorize the use of further PRCLEAR, PRWRITE and PRDS instructions. The PREN insruction does not modify the Protect Flag bit value.

Note: A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be held High during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the Protect Register to all 1's, and thus enables the execution of WRITE and WRALL instructions. The Protect Register Clear execution clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the Protect Register the address of the first word to be protected. After the PRWRITE instruction execution, all memory locations equal to and above the specified address, are protected from writing. The Protect Flag bit is set to '0', it can be read with Protect Register Read instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRWRITE instruction, but it is not necessary to execute first a PRCLEAR.

Protect Register Disable

The Protect Register Disable instruction sets the One Time Programmable bit (OTP bit). The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which latches the Protect Register content, this content is therefore unalterable in the future. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution. The OTP bit cannot be directly read, it can be checked by reading the content of the Protect Register (PRREAD instruction), then by writing this same value into the Protect Register (PRWRITE instruction): when the OTP bit is set, the Ready/Busy status cannot appear on the Data output (Q); when the OTP bit is not set, the Busy status appear on the Data output (Q).

A PREN instruction must immediately precede the PRDS instruction.

READY/BUSY Status

When the ST93CS46/47 is performing the write cycle, the Busy signal (Q = 0) is returned if S is driven high, and the ST93CS46/47 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate, if S is driven high, that the ST93CS46/47 is ready to receive a new instruction. Once the ST93CS46/47 is Ready, the Data Output Q is set to '1' until a new Start bit is decoded or the Chip Select is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the SGS-THOMSON application note "Microwire EEPROM Common I/O Operation".

Figure 8. PRREAD, PRWRITE, PREN Sequences

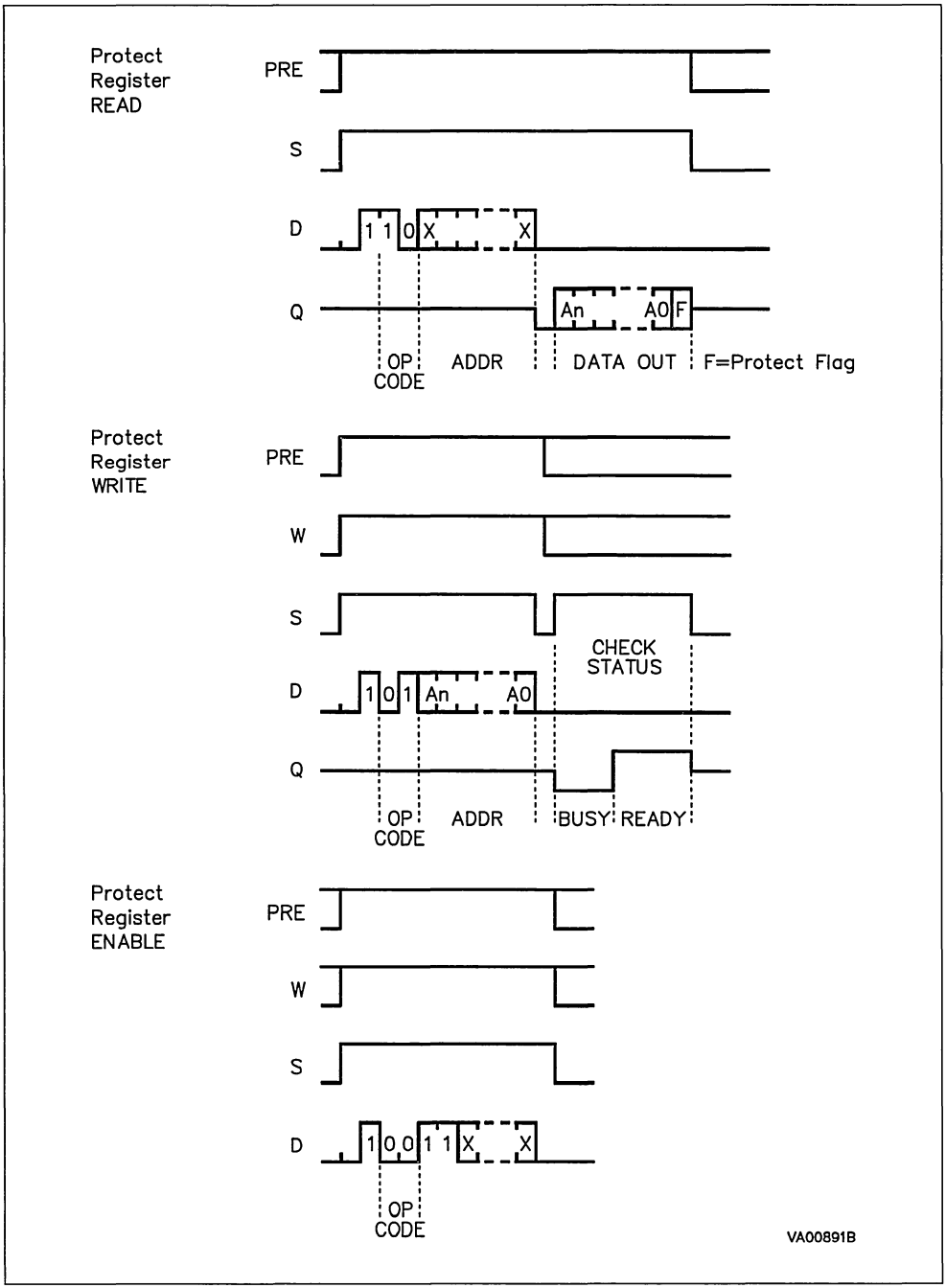
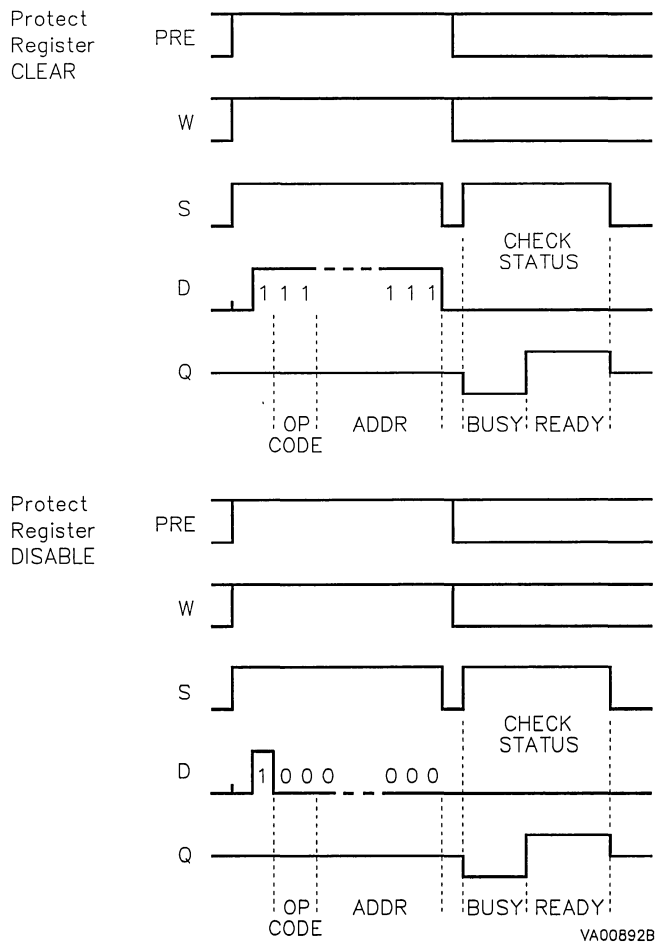
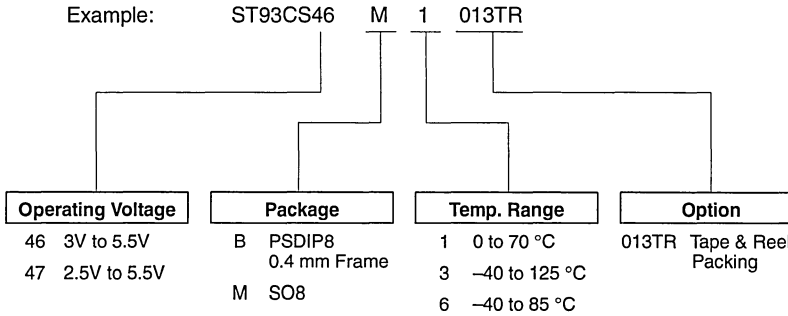


Figure 9. PRCLEAR, PRDS Sequences



ORDERING INFORMATION SCHEME



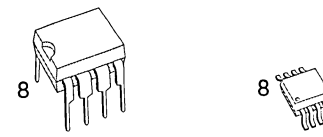
Parts are shipped with the memory content set at all "1's" (FFFFh).

For a list of available options (Operating Voltage, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SERIAL ACCESS CMOS 2K bit (128 x 16) EEPROM

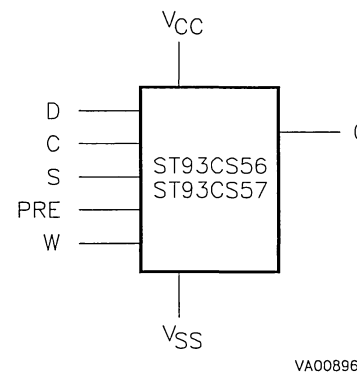
- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE
  - 3V to 5.5V for the ST93CS56
  - 2.5V to 5.5V for the ST93CS57
- USER DEFINED WRITE PROTECTED AREA
- PAGE WRITE MODE (4 WORDS)
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST93CS56 and ST93CS57 are 2K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input D and output Q.

The 2K bit memory is organized as 128 x 16 bit words.The memory is accessed by a set of instructions which include Read, Write, Page Write, Write All and instructions used to set the memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer. The data is then clocked out serially.

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

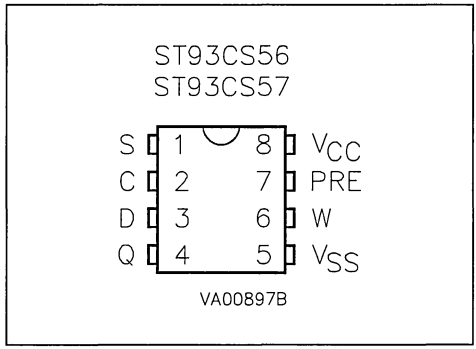


Figure 2B. SO Pin Connections

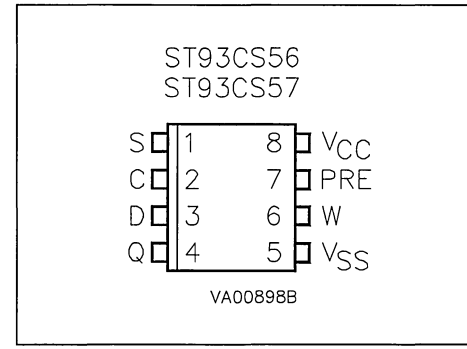


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			3000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93CS56/57 can output a sequential stream of data words. In this way, the memory can be read as a data stream of 16 to 2048 bits, or continuously as the address counter automatically rolls over to 00 when the highest address is reached.

Within the time required by a programming cycle (t_W), up to 4 words may be written with the help of the Page Write instruction; the whole memory may also be erased, or set to a predetermined pattern, by using the Write All instruction.

Within the memory, an user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protect Register, located outside of the memory array. As a final protection step, data may be permanently protected by programming a One Time Programing bit (OTP bit) which locks the Protect Register content.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction.

The Write instruction writes 16 bits at one time into one of the 128 words, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, assuming in both cases that all addresses are outside the Write Protected area.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

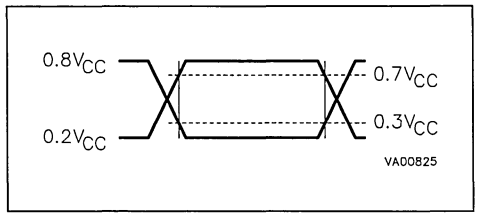


Table 3. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST93CS56, ST93CS57	1,000,000	10

Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 5. DC Characteristics (T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V for ST93CS56 and V_{CC} = 2.5V to 5.5V for ST93CS57)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}		50	µA
V_{IL}	Input Low Voltage (ST93CS56,57)	$4.5V \le V_{CC} \le 5.5V$	–0.1	0.8	V
	Input Low Voltage (ST93CS56)	$3V \le V_{CC} \le 5.5V$	–0.1	0.2 V_{CC}	V
	Input Low Voltage (ST93CS57)	$2.5V \le V_{CC} \le 5.5V$	–0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage (ST93CS56,57)	$4.5V \le V_{CC} \le 5.5V$	2	V_{CC} + 1	V
	Input High Voltage (ST93CS56)	$3V \le V_{CC} \le 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
	Input High Voltage (ST93CS57)	$2.5V \le V_{CC} \le 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 6. AC Characteristics (T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V for ST93CS56 and V_{CC} = 2.5V to 5.5V for ST93CS57)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			100	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

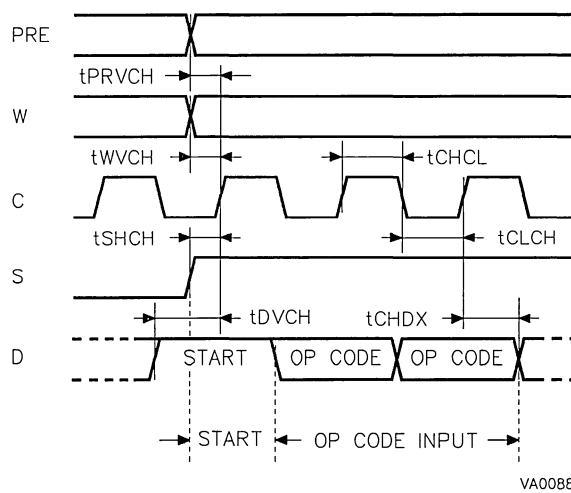
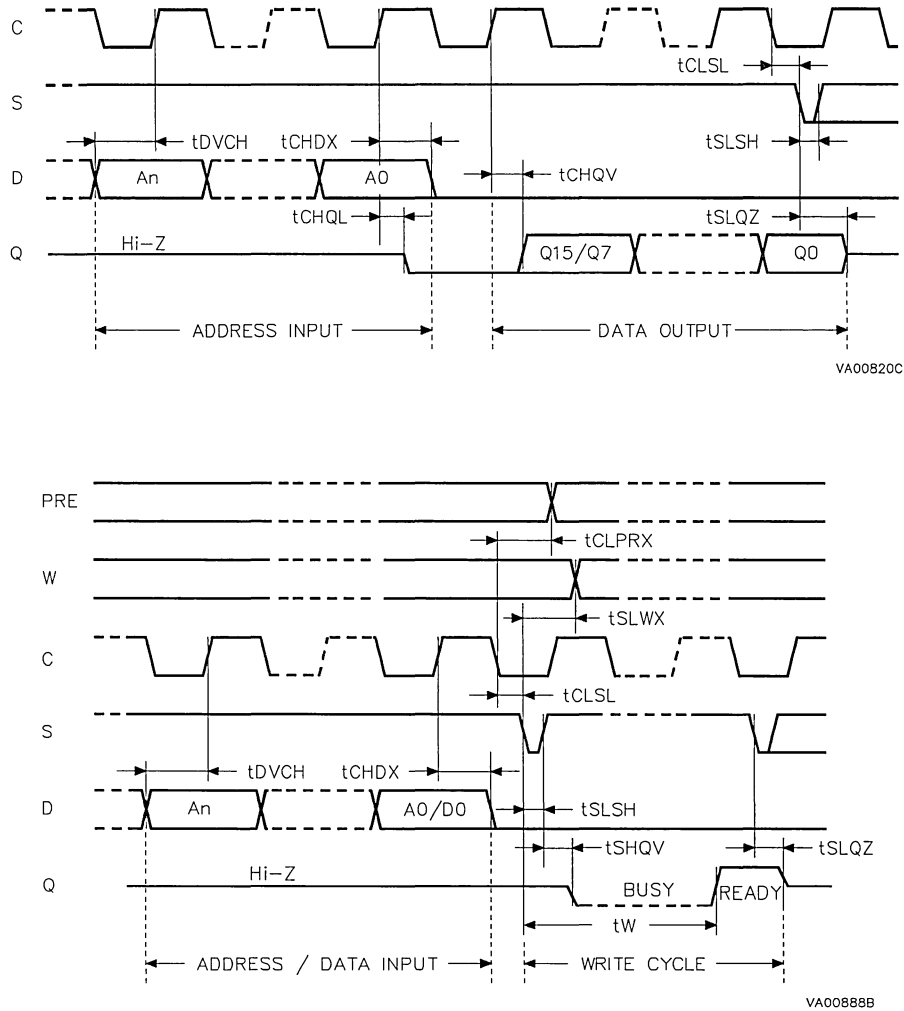


Figure 5. Synchronous Timing, Read or Write



DESCRIPTION (cont'd)

After the start of the programming cycle, a Ready/Busy signal is available on the Data output (Q) when the Chip Select (S) input pin is driven High.

The design of the ST93CS56/57 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied before any logic signal.

INSTRUCTIONS

The ST93CS56/57 has eleven instructions, as shown in Table 7. Each instruction is composed of a 2 bit op-code and an 8 bit address. Each instruction starts with the rising edge of the signal applied on the S input. The data input D is then sampled upon the following rising edges of the clock C until a '1' is sampled and decoded by the ST93CS56/57 as a Start bit.

The ST93CS56/57 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 6).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first. Output data changes are triggered by the Low to

Table 7. Instruction Set

Instruction	Description	W pin (1)	PRE pin	Op Code	Address (1, 2)	Data	Additional Information
READ	Read Data from Memory	X	'0'	10	A7-A0	Q15-Q0	
WRITE	Write Data to Memory	'1'	'0'	01	A7-A0	D15-D0	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	'1'	'0'	11	A7-A0	D15-D0	Write is executed if all the addresses are not inside the Protected area
WRALL	Write All Memory	'1'	'0'	00	01XX XXXX	D15-D0	Write all data if the Protect Register is cleared
WEN	Write Enable	'1'	'0'	00	11XX XXXX		
WDS	Write Disable	'1'	'0'	00	00XX XXXX		
PRREAD	Protect Register Read	X	'1'	10	XXXX XXXX	Q8-Q0	Data Output = Protect Register content + Protect Flag bit
PRWRITE	Protect Register Write	'1'	'1'	01	A7-A0		Data above specified address A7-A0 are protected (2)
PRCLEAR	Protect Register Clear	'1'	'1'	11	1111 1111		Protect Flag is also cleared (cleared Flag = 1)
PREN	Protect Register Enable	'1'	'1'	00	11XX XXXX		
PRDS	Protect Register Disable	'1'	'1'	00	0000 0000		OTP bit is set permanently

Note: 1. X = don't care bit.
2. Address bit A7 is not decoded by the ST93CS56/57.

INSTRUCTIONS (cont'd)

High transition of the Clock (C). The ST93CS56/57 will automatically increment the address and will clock out the next word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable and Write Disable

The Write Enable instruction (WEN) authorizes the following Write instructions to be executed, the Write Disable instruction (WDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93CS56/57 enters the Disable mode. When the Write Enable instruction (WEN) is executed, Write instructions remain enabled until a Write Disable instruction (WDS) is executed or if the Power-on reset circuit becomes active due to a reduced V_{CC}. To protect the memory contents from accidental corruption, it is advisable to issue the WDS instruction after every write cycle.

The READ instruction is not affected by the WEN or WDS instructions.

Write

The Write instruction (WRITE) is followed by the address and the word to be written. The Write Enable signal (W) must be held high during the WRITE instruction. Data input D is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C), in order to start the self-timed programming cycle, providing that the address is NOT in the protected area. If the ST93CS56/57 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS56/57 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS56/57 is ready to receive a new instruction.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be held High during the Write instruction. Input address and data are read on the Low to High transition of the clock. After the receipt of each data word, bits A1-A0 of the internal address register are incremented, the high order bits A7-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same five upper order address bits as the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The Page Write operation will not be performed if any of the 4 words is addressing the protected area. If the ST93CS56/57 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS56/57 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS56/57 is ready to receive a new instruction.

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes the whole memory with the same data word included in the instruction. The Write Enable signal (W) must be held High before and during the Write instruction. Input address and data are read on the Low to High transition of the clock. If the ST93CS56/57 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS56/57 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS56/57 is ready to receive a new instruction.

MEMORY WRITE PROTECTION AND PROTECT REGISTER

The ST93CS56/57 offers a Protect Register containing the bottom address of the memory area which has to be protected against write instructions. In addition to this Protect Register, two flag bits are used to indicate the Protect Register status: the Protect Flag enabling/disabling the protection of the Protect Register and the OTP bit which, when set, disables access to the Protect Register and thus prevents any further modifications of this Protect Register value. The content of the Protect Register is defined when using the PRWRITE instruction, it may be read when using the PRREAD instruction. A specific instruction PREN (Protect Register Enable) allows the user to execute the protect instructions PRCLEAR, PRWRITE and PRDS; this PREN instruction being used together with the signals applied on the input pins PRE

Figure 6. READ, WRITE, WEN, WDS Sequences

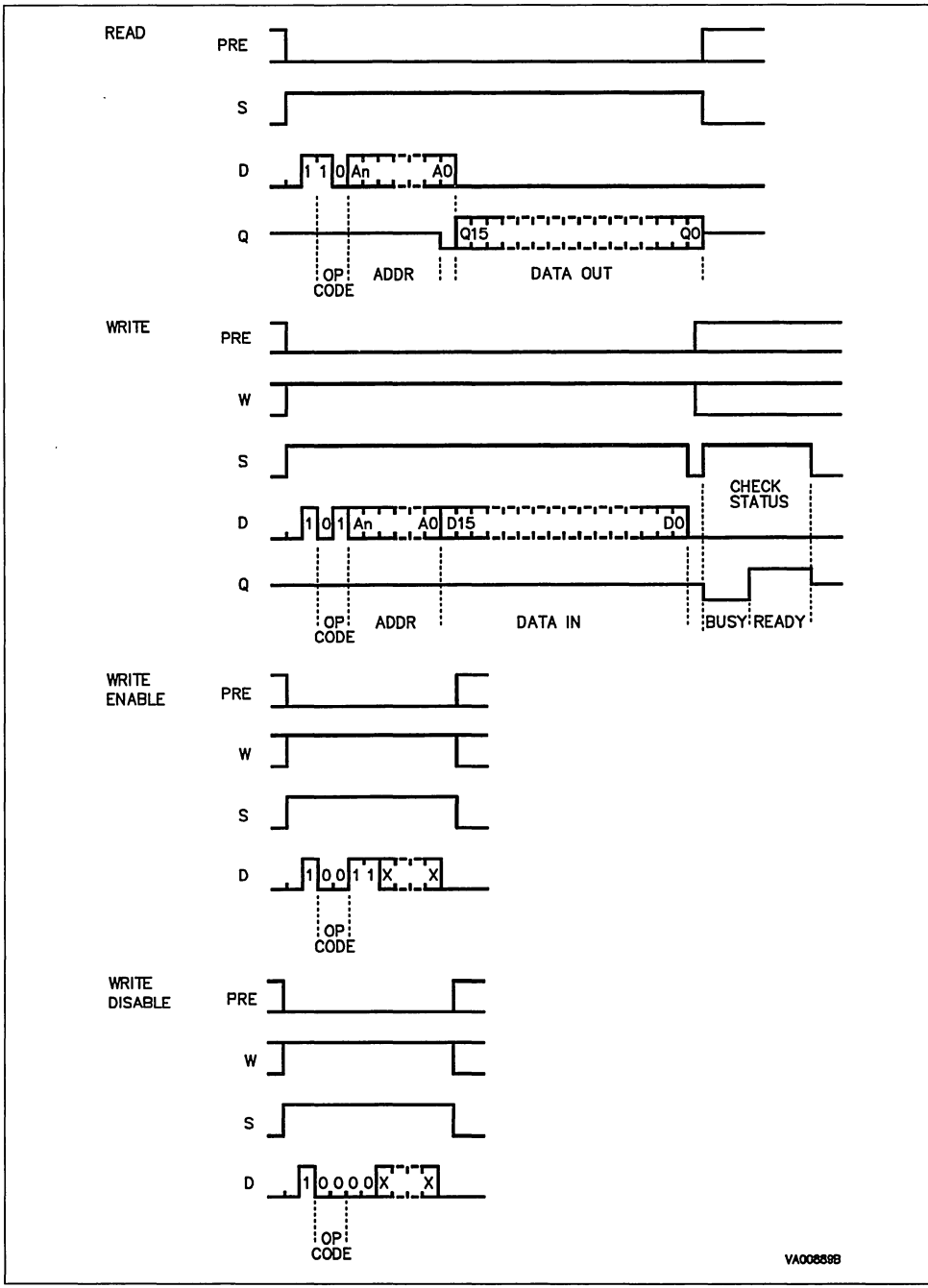
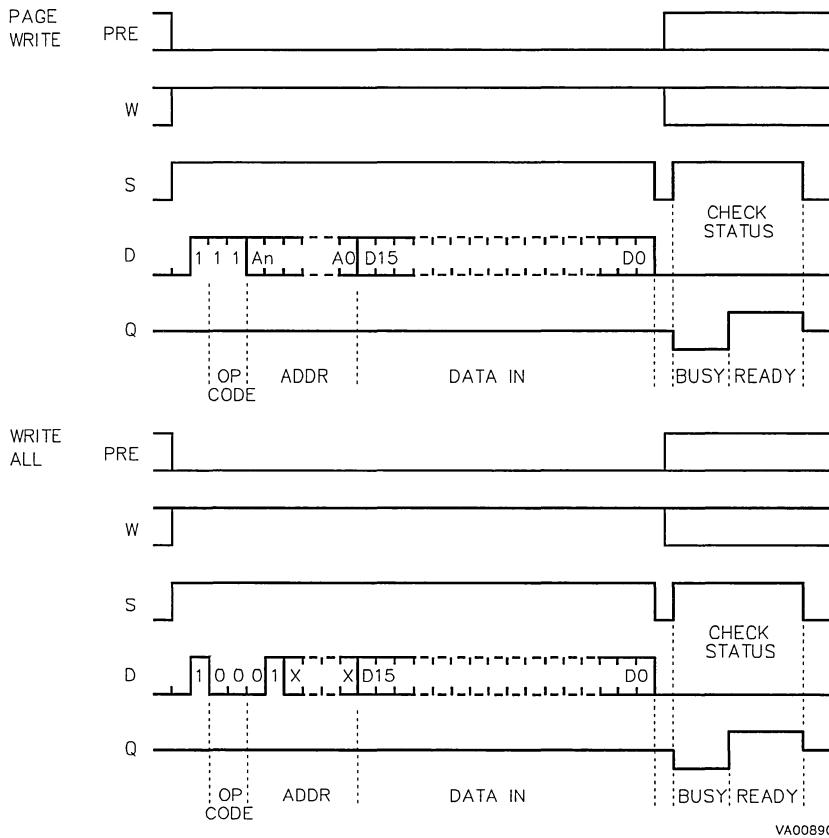


Figure 7. PAWRITE, WRALL Sequences



MEMORY WRITE PROTECTION (cont'd)

(Protect Register Enable pin) and W (Write Enable).

Accessing the Protect Register is done by executing the following sequence:

- WEN: execute the Write Enable instruction,
- PREN: execute the PREN instruction,
- PRWRITE, PRCLEAR or PRDS: the protection then may be defined, in terms of size of the protected area (PRWRITE, PRCLEAR) and may be set permanently (PRDS instruction).

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the content of the Protect Register, followed by the Protect Flag bit. The Protect Register Enable pin (PRE) must be driven High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish if the Protect Register is cleared (all 1's) or if it is written with all 1's, user must check the Protect Flag status (and not the Protect Register content) to ascertain the setting of the memory protection.

Protect Register Enable

The Protect Register Enable instruction (PREN) is used to authorize the use of further PRCLEAR, PRWRITE and PRDS instructions. The PREN insruction does not modify the Protect Flag bit value.

Note: A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be held High during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the Protect Register to all 1's, and thus enables the execution of WRITE and WRALL instructions. The Protect Register Clear execution clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the Protect Register the address of the first word to be protected. After the PRWRITE instruction execution, all memory locations equal to and above the specified address, are protected from writing. The Protect Flag bit is set to '0', it can be read with Protect Register Read instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRWRITE instruction, but it is not necessary to execute first a PRCLEAR.

Protect Register Disable

The Protect Register Disable instruction sets the One Time Programmable bit (OTP bit). The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which latches the Protect Register content, this content is therefore unalterable in the future. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution. The OTP bit cannot be directly read, it can be checked by reading the content of the Protect Register (PRREAD instruction), then by writing this same value into the Protect Register (PRWRITE instruction): when the OTP bit is set, the Ready/Busy status cannot appear on the Data output (Q); when the OTP bit is not set, the Busy status appear on the Data output (Q).

A PREN instruction must immediately precede the PRDS instruction.

READY/BUSY Status

When the ST93CS56/57 is performing the write cycle, the Busy signal (Q = 0) is returned if S is driven high, and the ST93CS56/57 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate, if S is driven high, that the ST93CS56/57 is ready to receive a new instruction. Once the ST93CS56/57 is Ready, the Data Output Q is set to '1' until a new Start bit is decoded or the Chip Select is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the SGS-THOMSON application note "Microwire EEPROM Common I/O Operation".

Figure 8. PRREAD, PRWRITE, PREN Sequences

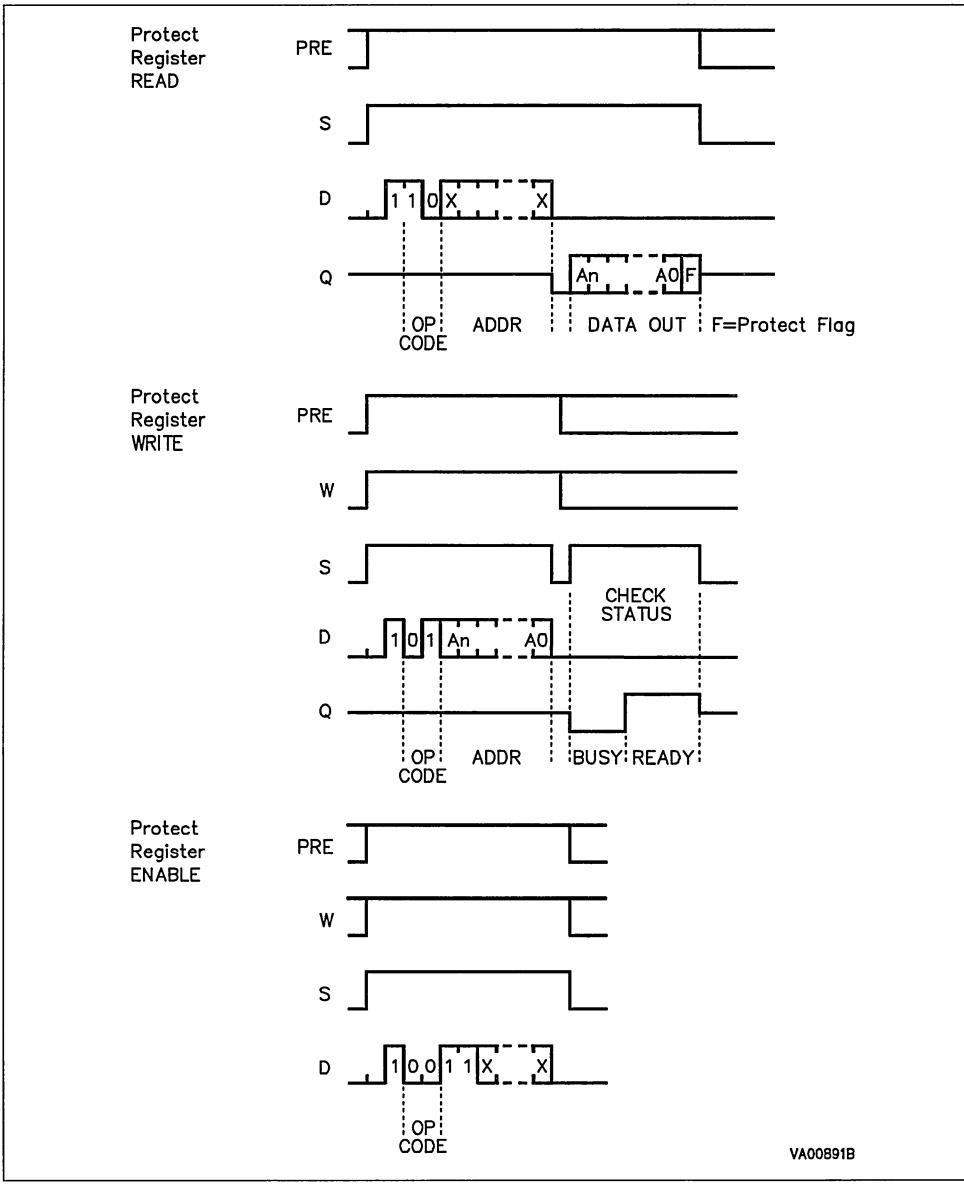
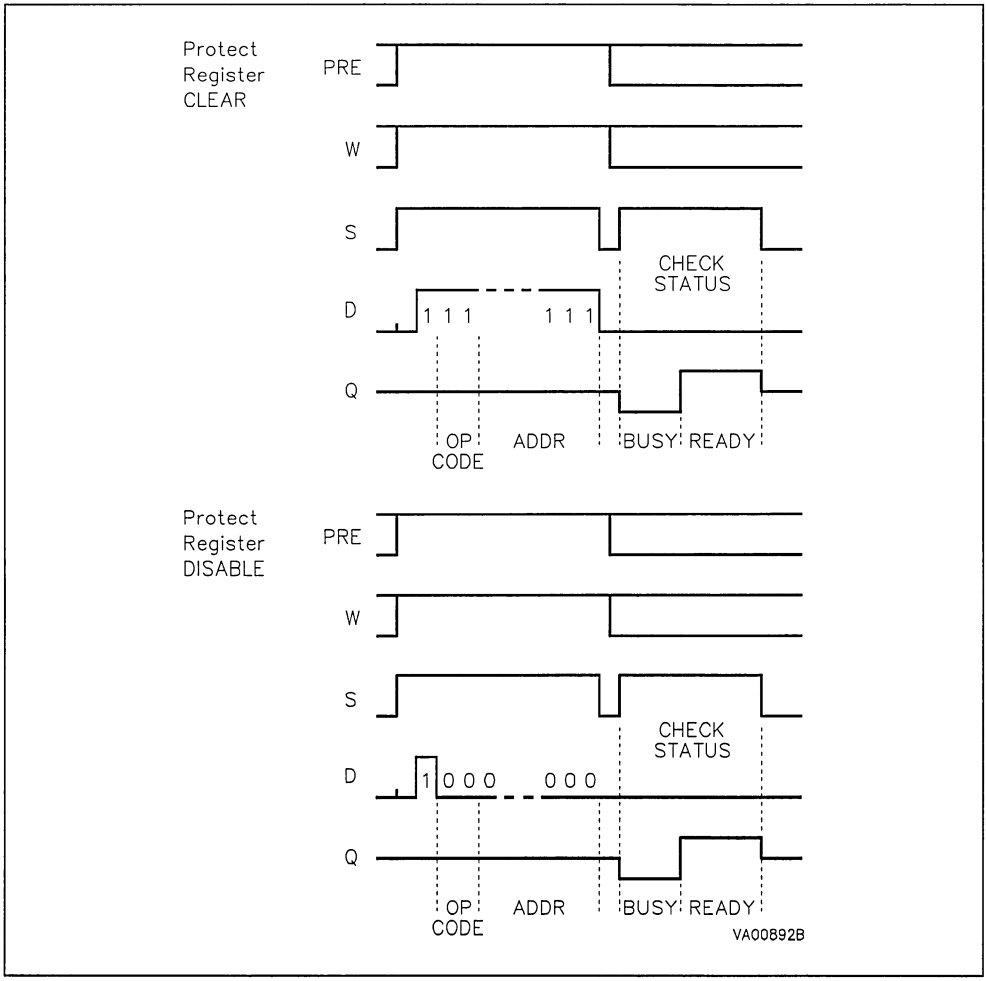
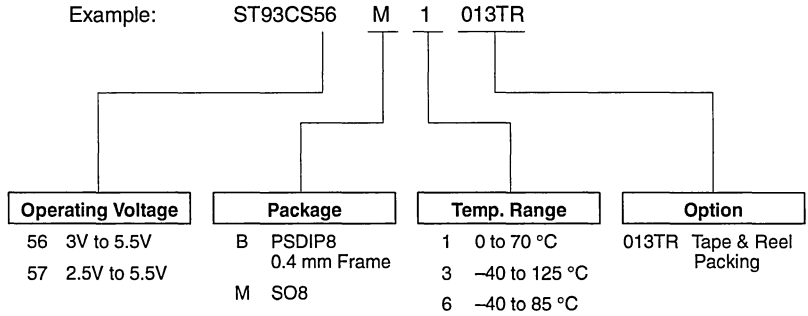


Figure 9. PRCLEAR, PRDS Sequences



ORDERING INFORMATION SCHEME



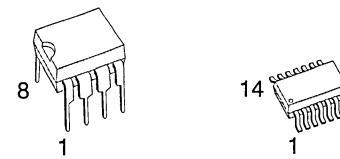
Parts are shipped with the memory content set at all "1's" (FFFFh).

For a list of available options (Operating Voltage, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SERIAL ACCESS CMOS 4K bit (256 x 16) EEPROM

- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE
  - 3V to 5.5V for the ST93CS66
  - 2.5V to 5.5V for the ST93CS67
- USER DEFINED WRITE PROTECTED AREA
- PAGE WRITE MODE (4 WORDS)
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.25mm Frame

SO14 (ML)

DESCRIPTION

The ST93CS66 and ST93CS67 are 4K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input D and output Q.

The 4K bit memory is organized as 256 x 16 bit words.The memory is accessed by a set of instructions which include Read, Write, Page Write, Write All and instructions used to set the memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer.

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

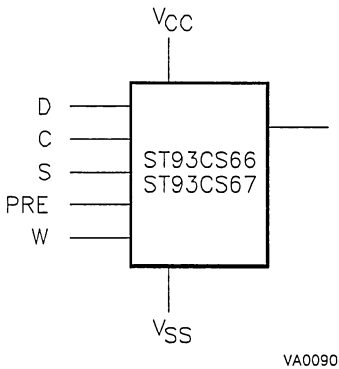


Figure 2A. DIP Pin Connections

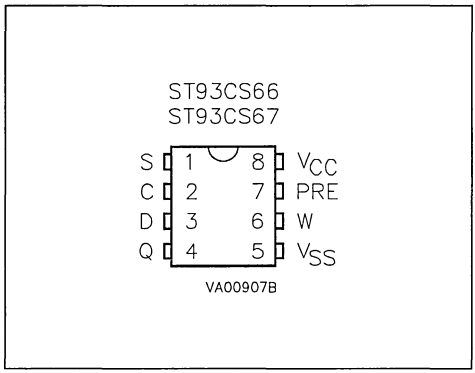
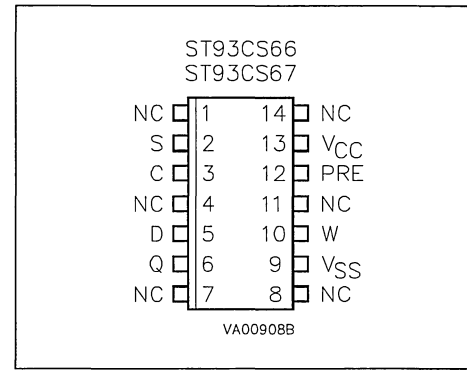


Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to V_{CC} +0.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			2000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3 EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The data is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93CS66/67 can output a sequential stream of data words.

In this way, the memory can be read as a data stream of 16 to 4096 bits, or continuously as the address counter automatically rolls over to 00 when the highest address is reached.

Within the time required by a programming cycle (t_W), up to 4 words may be written with the help of the Page Write instruction; the whole memory may also be erased, or set to a predetermined pattern, by using the Write All instruction.

Within the memory, an user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protect Register, located outside of the memory array. As a final protection step, data may be permanently protected by programming a One Time Programing bit (OTP bit) which locks the Protect Register content.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction.

The Write instruction writes 16 bits at one time into one of the 256 words, the Page Write instruction writes up to 4 words of 16 bits to sequential loca-

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

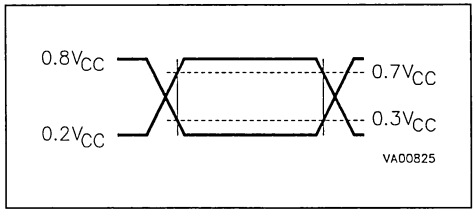


Table 3. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST93CS66, ST93CS67	1,000,000	10

Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 5. DC Characteristics (T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V for ST93CS66 and V_{CC} = 2.5V to 5.5V for ST93CS67)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}		50	µA
V_{IL}	Input Low Voltage (ST93CS66,67)	4.5V ≤ V_{CC} ≤ 5.5V	–0.1	0.8	V
	Input Low Voltage (ST93CS66)	3V ≤ V_{CC} ≤ 5.5V	–0.1	0.2 V_{CC}	V
	Input Low Voltage (ST93CS67)	2.5V ≤ V_{CC} ≤ 5.5V	–0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage (ST93CS66,67)	4.5V ≤ V_{CC} ≤ 5.5V	2	V_{CC} + 1	V
	Input High Voltage (ST93CS66)	3V ≤ V_{CC} ≤ 5.5V	0.8 V_{CC}	V_{CC} + 1	V
	Input High Voltage (ST93CS67)	2.5V ≤ V_{CC} ≤ 5.5V	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 6. AC Characteristics (T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V for ST93CS66 and V_{CC} = 2.5V to 5.5V for ST93CS67)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			100	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

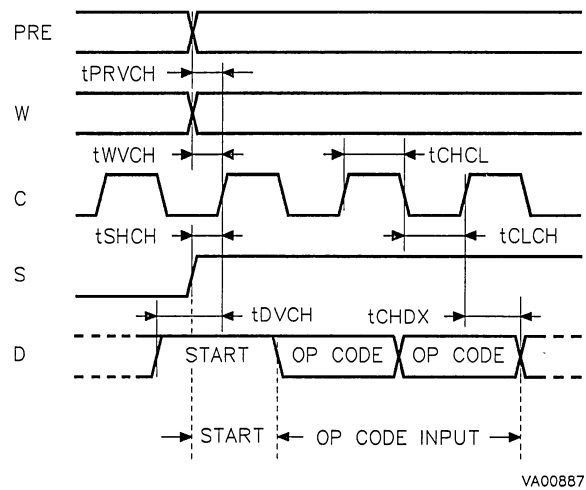
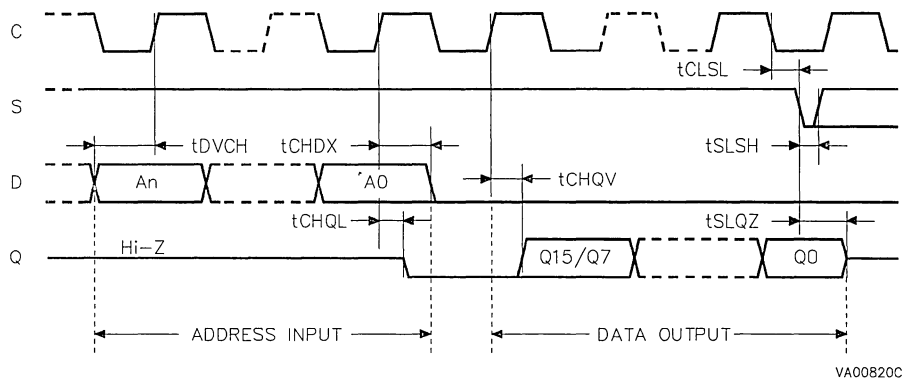
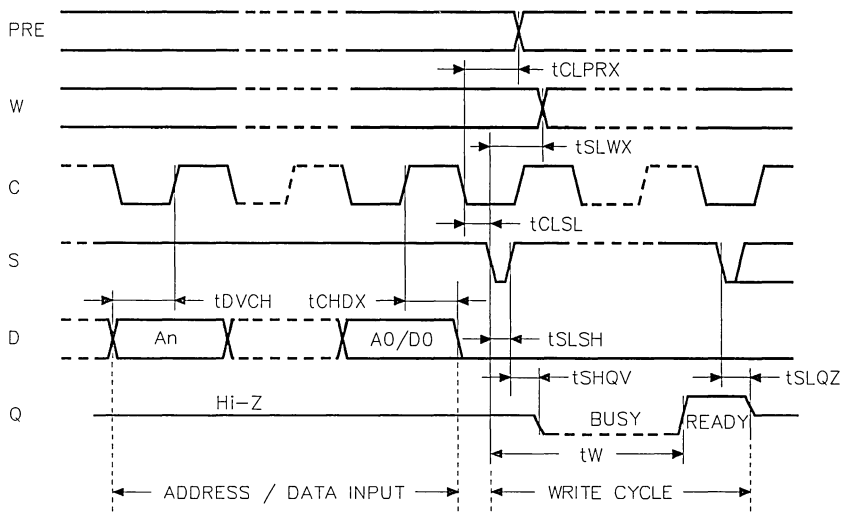


Figure 5. Synchronous Timing, Read or Write





DESCRIPTION (cont'd)

tions, assuming in both cases that all addresses are outside the Write Protected area. After the start of the programming cycle, a Ready/Busy signal is available on the Data output (Q) when the Chip Select (S) input pin is driven High.

The design of the ST93CS66/67 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied before any logic signal.

INSTRUCTIONS

The ST93CS66/67 has eleven instructions, as shown in Table 7. Each instruction is composed of a 2 bit op-code and an 8 bit address. Each instruction starts with the rising edge of the signal applied on the S input.

The data input D is then sampled upon the following rising edges of the clock C until a '1' is sampled and decoded by the ST93CS66/67 as a Start bit. The ST93CS66/67 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 6).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C).

The ST93CS66/67 will automatically increment the address and will clock out the next word as long as

Table 7. Instruction Set

Instruction	Description	W pin (1)	PRE pin	Op Code	Address (1)	Data	Additional Information
READ	Read Data from Memory	X	'0'	10	A7-A0	Q15-Q0	
WRITE	Write Data to Memory	'1'	'0'	01	A7-A0	D15-D0	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	'1'	'0'	11	A7-A0	D15-D0	Write is executed if all the addresses are not inside the Protected area
WRALL	Write All Memory	'1'	'0'	00	01XX XXXX	D15-D0	Write all data if the Protect Register is cleared
WEN	Write Enable	'1'	'0'	00	11XX XXXX		
WDS	Write Disable	'1'	'0'	00	00XX XXXX		
PRREAD	Protect Register Read	X	'1'	10	XXXX XXXX	Q8-Q0	Data Output = Protect Register content + Protect Flag bit
PRWRITE	Protect Register Write	'1'	'1'	01	A7-A0		Data above specified address A7-A0 are protected
PRCLEAR	Protect Register Clear	'1'	'1'	11	1111 1111		Protect Flag is also cleared (cleared Flag = 1)
PREN	Protect Register Enable	'1'	'1'	00	11XX XXXX		
PRDS	Protect Register Disable	'1'	'1'	00	0000 0000		OTP bit is set permanently

Note: 1. X = don't care bit.

INSTRUCTIONS (cont'd)

the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable and Write Disable

The Write Enable instruction (WEN) authorizes the following Write instructions to be executed, the Write Disable instruction (WDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93CS66/67 enters the Disable mode. When the Write Enable instruction (WEN) is executed, Write instructions remain enabled until a Write Disable instruction (WDS) is executed or if the Power-on reset circuit becomes active due to a reduced V_{CC}. To protect the memory contents from accidental corruption, it is advisable to issue the WDS instruction after every write cycle.

The READ instruction is not affected by the WEN or WDS instructions.

Write

The Write instruction (WRITE) is followed by the address and the word to be written. The Write Enable signal (W) must be held high during the WRITE instruction. Data input D is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C), in order to start the self-timed programming cycle, providing that the address is NOT in the protected area. If the ST93CS66/67 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS66/67 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS66/67 is ready to receive a new instruction.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be held High during the Write instruction. Input address and data are read on the Low to High transition of the clock. After the receipt of each data word, bits A1-A0 of the internal address register are incremented, the high order bits A7-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same six upper order address bits as the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The Page Write operation will not be performed if any of the 4 words is addressing the protected area. If the ST93CS66/67 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS66/67 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS66/67 is ready to receive a new instruction.

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes the whole memory with the same data word included in the instruction. The Write Enable signal (W) must be held High before and during the Write instruction. Input address and data are read on the Low to High transition of the clock. If the ST93CS66/67 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS66/67 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS66/67 is ready to receive a new instruction.

MEMORY WRITE PROTECTION AND PROTECT REGISTER

The ST93CS66/67 offers a Protect Register containing the bottom address of the memory area which has to be protected against write instructions. In addition to this Protect Register, two flag bits are used to indicate the Protect Register status: the Protect Flag enabling/disabling the protection of the Protect Register and the OTP bit which, when set, disables access to the Protect Register and thus prevents any further modifications of this Protect Register value. The content of the Protect Register is defined when using the PRWRITE instruction, it may be read when using the PRREAD instruction. A specific instruction PREN (Protect Register Enable) allows the user to execute the protect instructions PRCLEAR, PRWRITE and PRDS; this PREN instruction being used together with the signals applied on the input pins PRE (Protect Register Enable pin) and W (Write Enable).

Figure 6. READ, WRITE, WEN, WDS Sequences

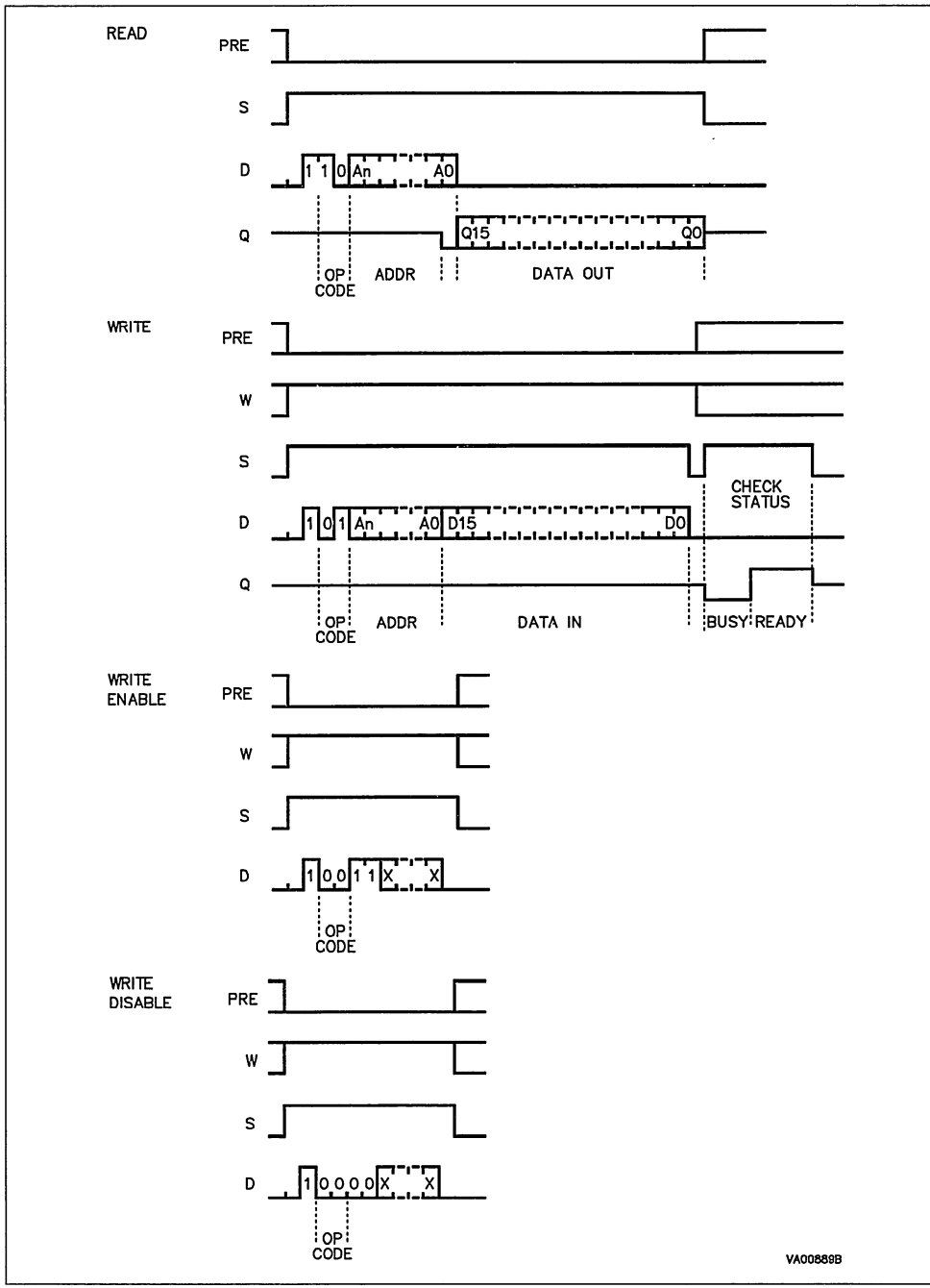
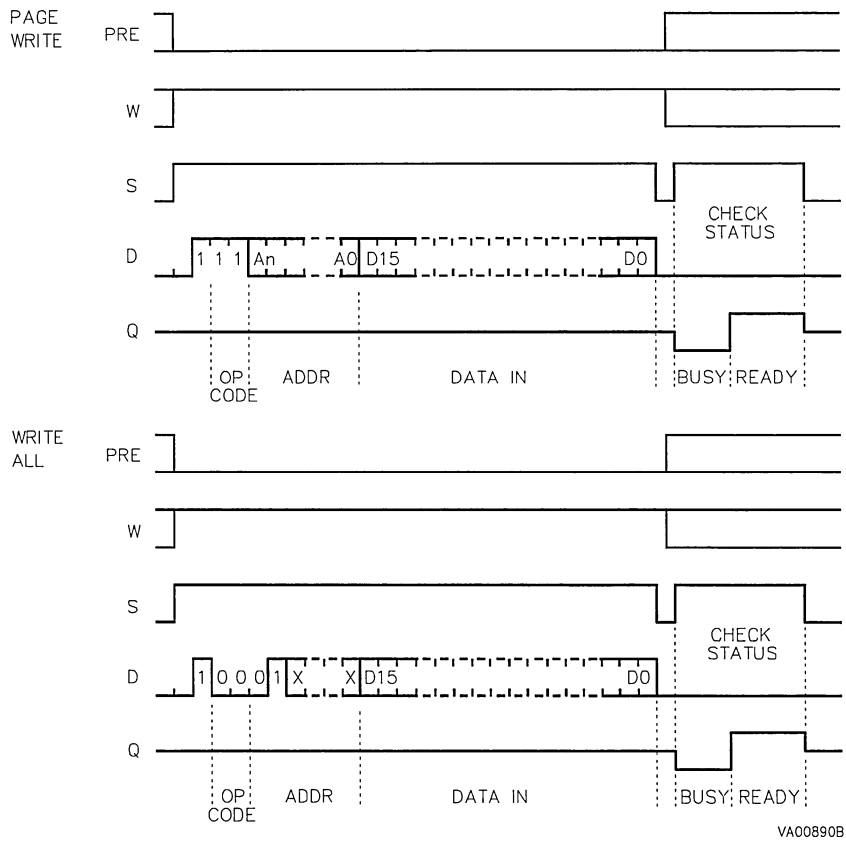


Figure 7. PAWRITE, WRALL Sequences



MEMORY WRITE PROTECTION (cont'd)

Accessing the Protect Register is done by executing the following sequence:

- WEN: execute the Write Enable instruction,
- PREN: execute the PREN instruction,
- PRWRITE, PRCLEAR or PRDS: the protection then may be defined, in terms of size of the protected area (PRWRITE, PRCLEAR) and may be set permanently (PRDS instruction).

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the content of the Protect Register, followed by the Protect Flag bit. The Protect Register Enable pin (PRE) must be driven High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish if the Protect Register is cleared (all 1's) or if it is written with all 1's, user must check the Protect Flag status (and not the Protect Register content) to ascertain the setting of the memory protection.

Protect Register Enable

The Protect Register Enable instruction (PREN) is used to authorize the use of further PRCLEAR, PRWRITE and PRDS instructions. The PREN insruction does not modify the Protect Flag bit value.

Note: A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be held High during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the Protect Register to all 1's, and thus enables the execution of WRITE and WRALL instructions. The Protect Register Clear execution clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the Protect Register the address of the first word to be protected. After the PRWRITE instruction execution, all memory locations equal to and above the specified address, are protected from writing. The Protect Flag bit is set to '0', it can be read with Protect Register Read instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRWRITE instruction, but it is not necessary to execute first a PRCLEAR.

Protect Register Disable

The Protect Register Disable instruction sets the One Time Programmable bit (OTP bit). The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which latches the Protect Register content, this content is therefore unalterable in the future. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution. The OTP bit cannot be directly read, it can be checked by reading the content of the Protect Register (PRREAD instruction), then by writing this same value into the Protect Register (PRWRITE instruction): when the OTP bit is set, the Ready/Busy status cannot appear on the Data output (Q); when the OTP bit is not set, the Busy status appear on the Data output (Q).

A PREN instruction must immediately precede the PRDS instruction.

READY/BUSY Status

When the ST93CS66/67 is performing the write cycle, the Busy signal (Q = 0) is returned if S is driven high, and the ST93CS66/67 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate, if S is driven high, that the ST93CS66/67 is ready to receive a new instruction. Once the ST93CS66/67 is Ready, the Data Output Q is set to '1' until a new Start bit is decoded or the Chip Select is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the SGS-THOMSON application note "Microwire EEPROM Common I/O Operation".

Figure 8. PRREAD, PRWRITE, PREN Sequences

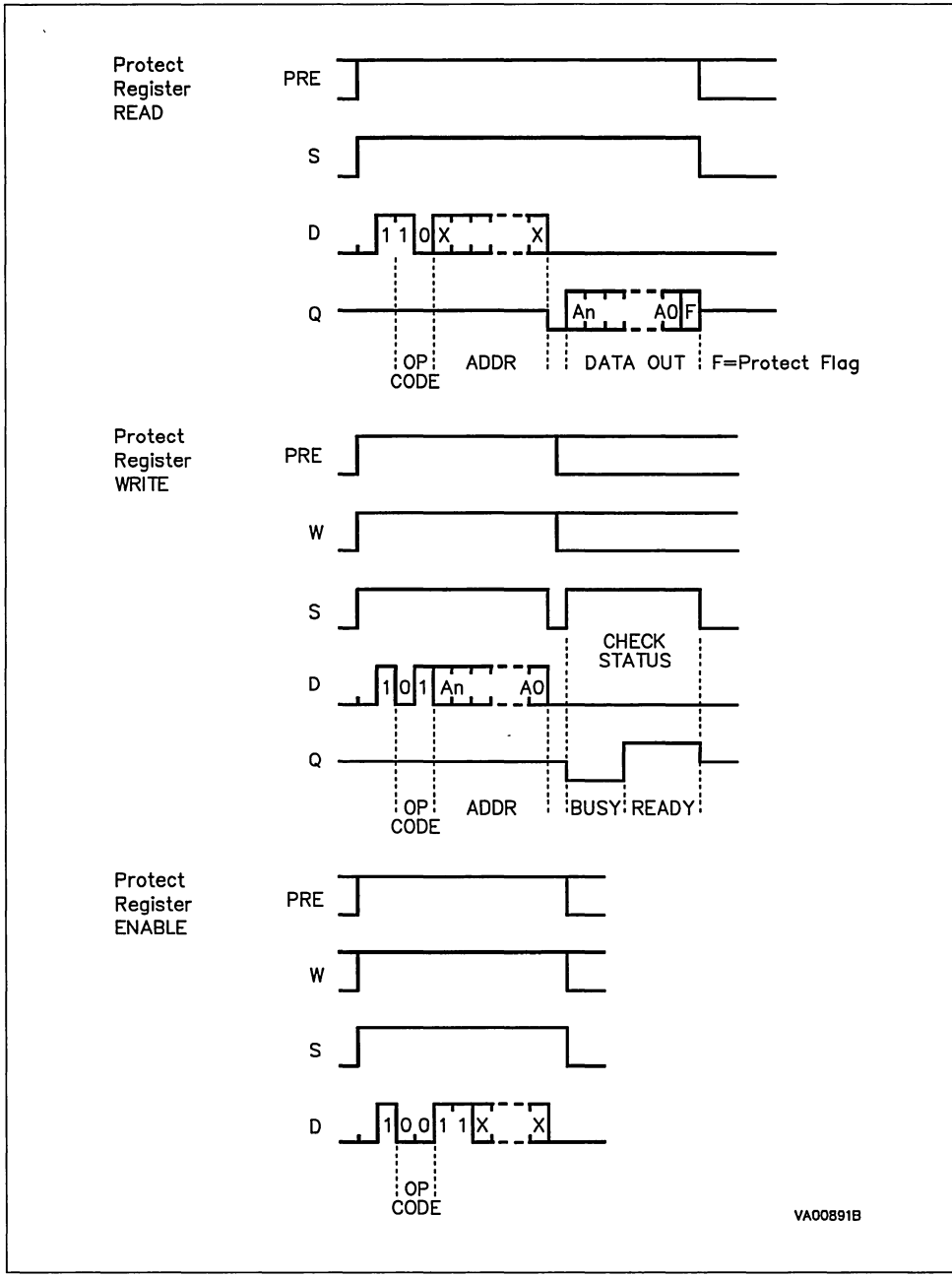
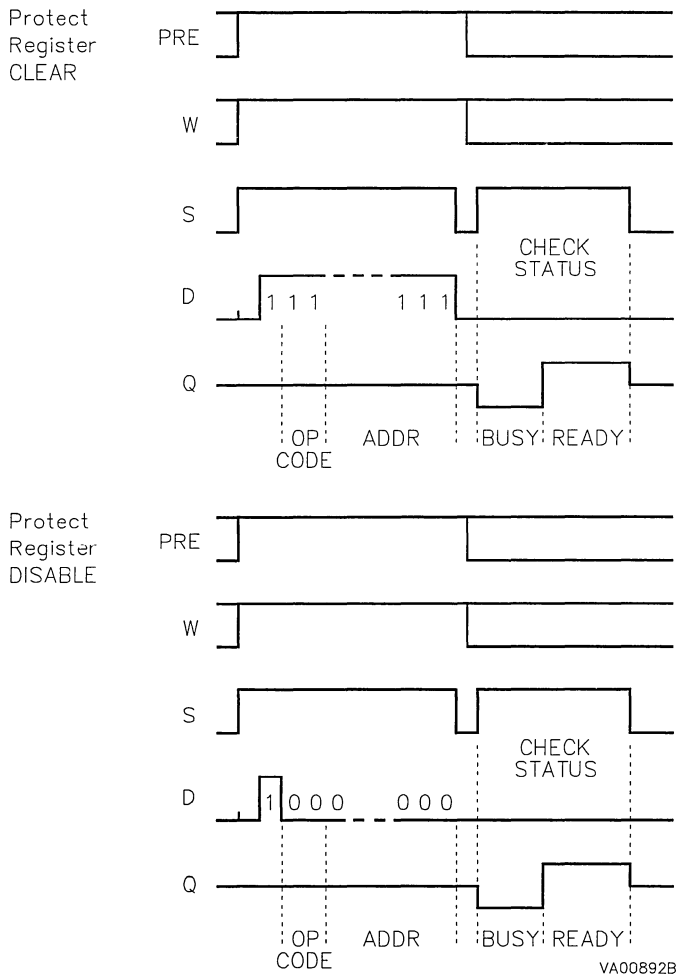
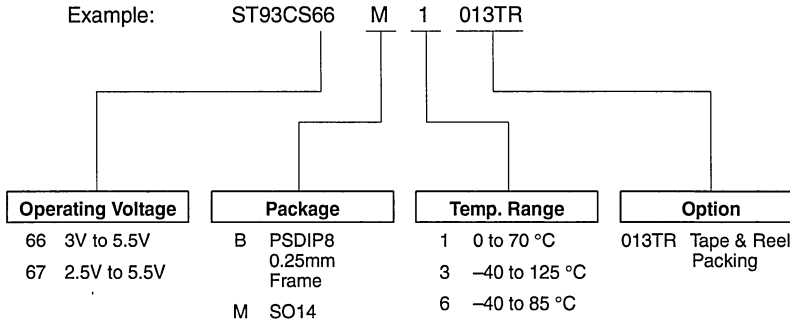


Figure 9. PRCLEAR, PRDS Sequences



ORDERING INFORMATION SCHEME



Parts are shipped with the memory content set at all "1's" (FFFFh).

For a list of available options (Operating Voltage, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

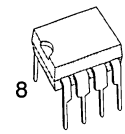
For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SPI BUS EEPROM

SERIAL ACCESS SPI BUS CMOS 4K (512 x 8) EEPROM

PRODUCT CONCEPT

- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SINGLE 3V to 5.5V SUPPLY VOLTAGE
- SPI SERIAL INTERFACE COMPATIBLE
- 1 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED 5ms (max) PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V



PSDIP8 (PS)
0.25mm Frame

SO8 (M)

DESCRIPTION

The ST95P04C is a 4K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The 4K bit memory is organised as 32 pages of 16 bytes. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q). The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Figure 1. Logic Diagram

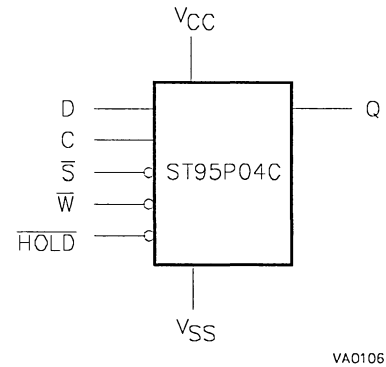


Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

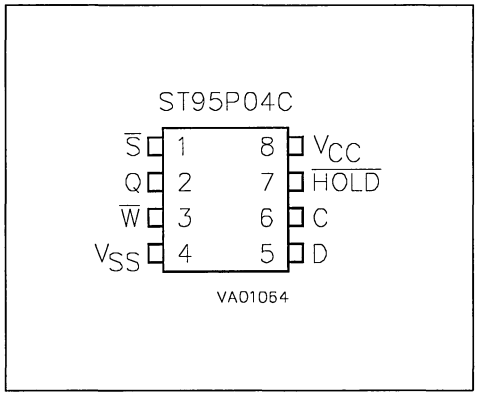


Figure 2B. SO Pin Connections

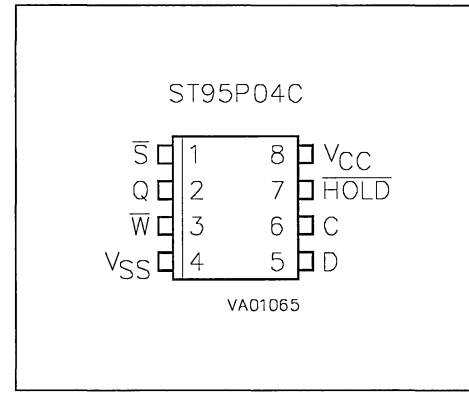


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature:		grade 3 grade 6	–40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliabilty. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out of the ST95P04C. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the rising edge of the serial clock.

Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). This input is used to select the ST95C04P. The chip is selected by a high to low transition on the $\overline{S}$ pin when C is at '0' state. At any time, the chip is deselected by a low to high transition on the $\overline{S}$ pin when C is at '0' state. As soon as the chip is deselected, the Q pin is at high impedance state. This pin allows multiple ST95P04C to share the same SPI bus. After power up, the chip is at the deselect state. Non valid $\overline{S}$ transitions are ignored.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

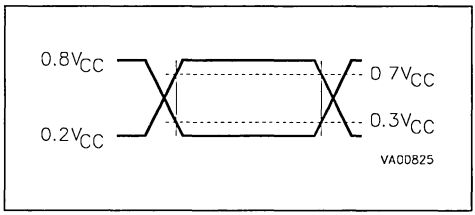


Figure 4. AC Testing Load Circuit

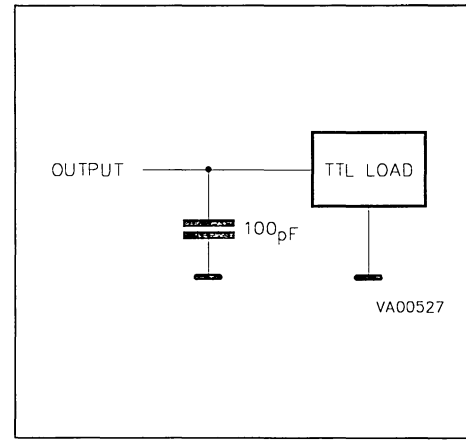


Table 3. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = –40 to 85°C or –40 to 125°C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC} , @ 1 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V		50	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3V		10	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = 2mA	0.8 V_{CC}		V

Table 5. AC Characteristics
(T_A = –40 to 85°C or –40 to 125°C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	1	MHz
t_{SLCH}	t_{SU}	$\overline{S}$ Setup Time		100		ns
t_{CLSH}	t_{SH}	$\overline{S}$ Hold Time		100		ns
t_{CH}	t_{WH}	Clock High Time		400		ns
t_{CL}	t_{WL}	Clock Low Time		400		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		100		ns
t_{CHDX}	t_{DH}	Data In Hold Time		100		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HXCH}	t_{HSU}	$\overline{HOLD}$ Setup Time		100		ns
t_{CLHX}	t_{HH}	$\overline{HOLD}$ Hold Time		100		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time		400		ns
t_{SHQZ}	t_{DIS}	Output Disable Time			300	ns
t_{QVCL}	t_V	Output Valid from Clock Low			350	ns
t_{CLQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH}	t_{RO}	Output Rise Time			150	ns
t_{QHQL}	t_{FO}	Output Fall Time			150	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			300	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z			300	ns
t_W	t_W	Write Cycle Time			5	ms
t_{LPF}	-	Pulse Time Filtered by Input Low-pass Filter			30	ns

Figure 5. Output Timing

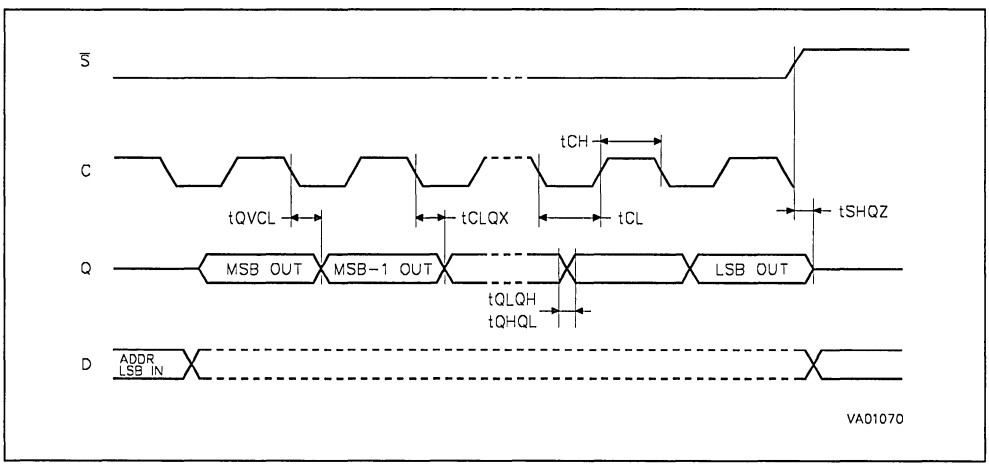


Figure 6. Serial Input Timing

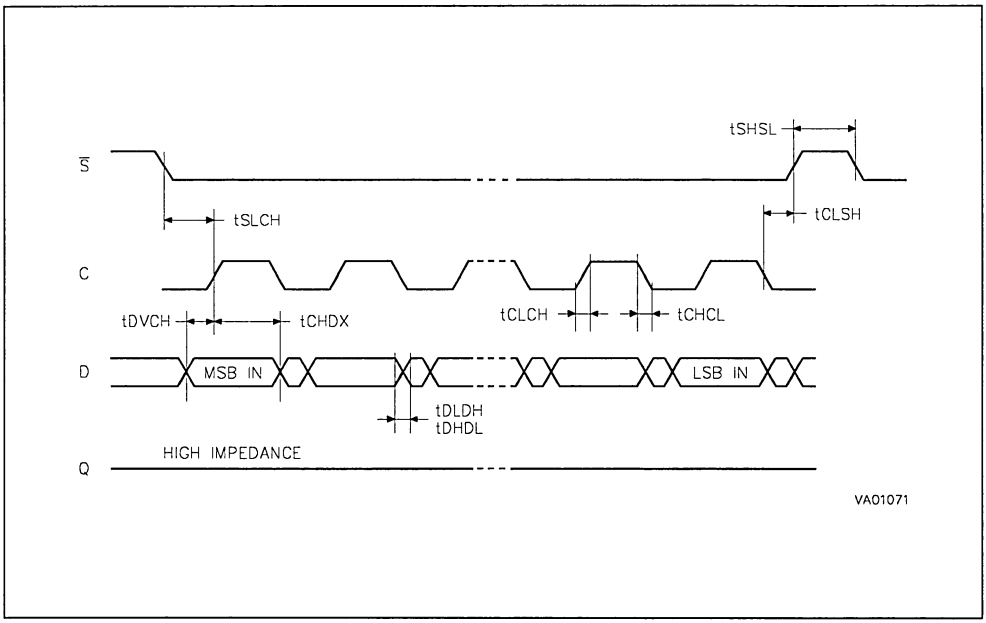
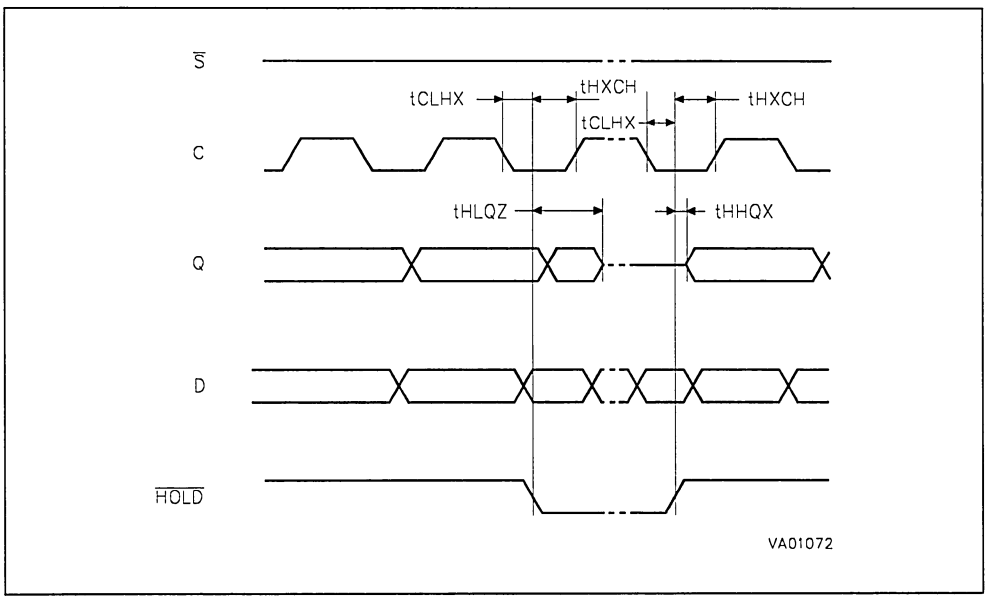


Figure 7. Hold Timing



SIGNALS DESCRIPTION (cont'd)

Write Protect ($\overline{W}$). This pin is for hardware write protect. When $\overline{W}$ is low, non-volatile writes to the ST95P04C are disabled but any other operation functions normally. When $\overline{W}$ is high, all operations including non-volatile writes function normally. $\overline{W}$ going low at any time will reset the write enable latch and prevent programming. However, no action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications with a ST95P04C without resetting the serial sequence. To take the Hold condition into account, the product must be selected. Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high when C is low. During Hold condition D, Q, and C are at a high impedance state.

When the ST95P04C is under Hold condition, it is possible to deselect it. However, the serial communications will remain paused after a reselect, and the chip will be reset. Non valid $\overline{HOLD}$ transitions are ignored.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 7 shows the instruction set and format for device operation. When an invalid instruction is sent (one not contained in Table 7), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The ST95P04C contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95P04C, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a non-volatile write. As soon as the 8th bit of the status register is read out, the

Table 6. Array Addresses Protect

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	none
0	1	180h - 1FFh
1	0	100h - 1FFh
1	1	000h - 1FFh

Table 7. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 X110
WRDI	Reset Write Enable Latch	0000 X100
RDSR	Read Status Register	0000 X101
WRSR	Write Status Register	0000 X001
READ	Read Data from Memory Array	0000 A011
WRITE	Write Data to Memory Array	0000 A010

Notes: A = 1, Upper page selected
A = 0, Lower page selected
X = Don't care

product enters a wait mode (data on D are not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

During a non-volatile write to the memory array, all bits BP1, BP0, WEL, WIP are valid. During a non-volatile write to the status register, bits WEL and WIP are valid. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write - In - Process (WIP) bit indicates whether the ST95P04C is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset.

The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The ST95P04C is divided into four 1024 bit blocks. The user may read the blocks but will be unable to write within the selected blocks.

The blocks and respective WRSR control bits are shown in Table 6.

To start the write cycle, the chip must be deselected during the clock pulse just after the eigth bit of status register has been latched in, otherwise, the WRSR process is cancelled (see Figure 12).

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0). Bit 3 of the read instruction contains address A8 (most significant address bit). This bit is used to select the first or second page of the device. Then, the data stored in the memory at the selected address is shifted out on the Q output pin. The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFh), the address counter rolls over to 0h allowing the read cycle to be continued

Figure 8. Read Operation Sequence

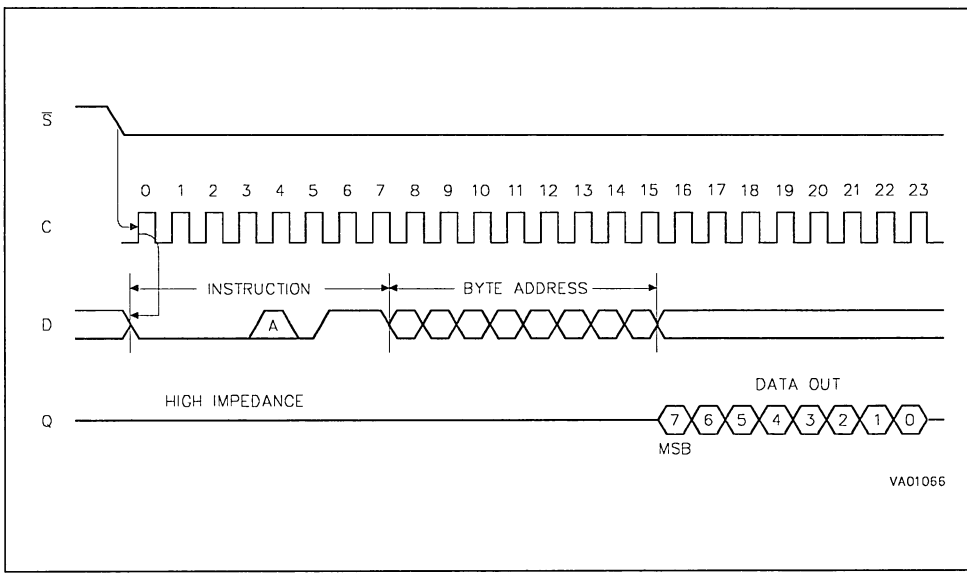


Figure 9. Write Enable Latch Sequence

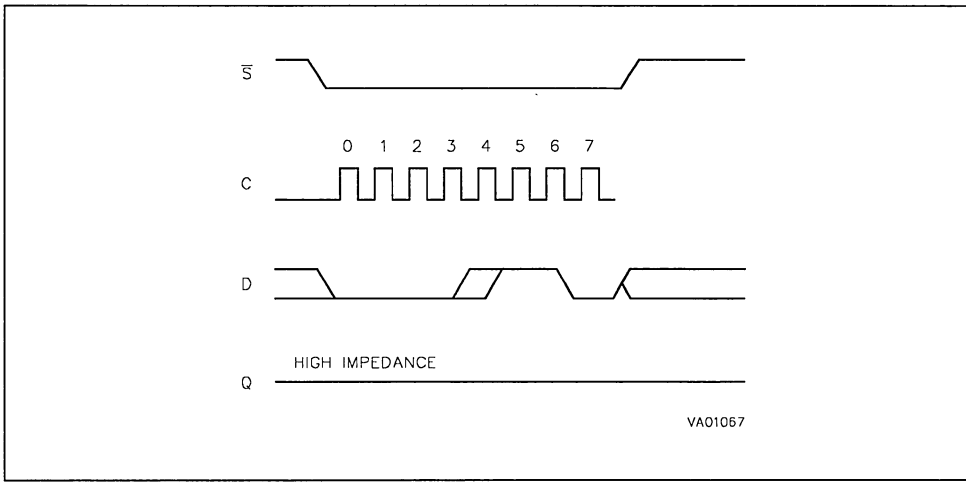


Figure 10. Write Operation Sequence

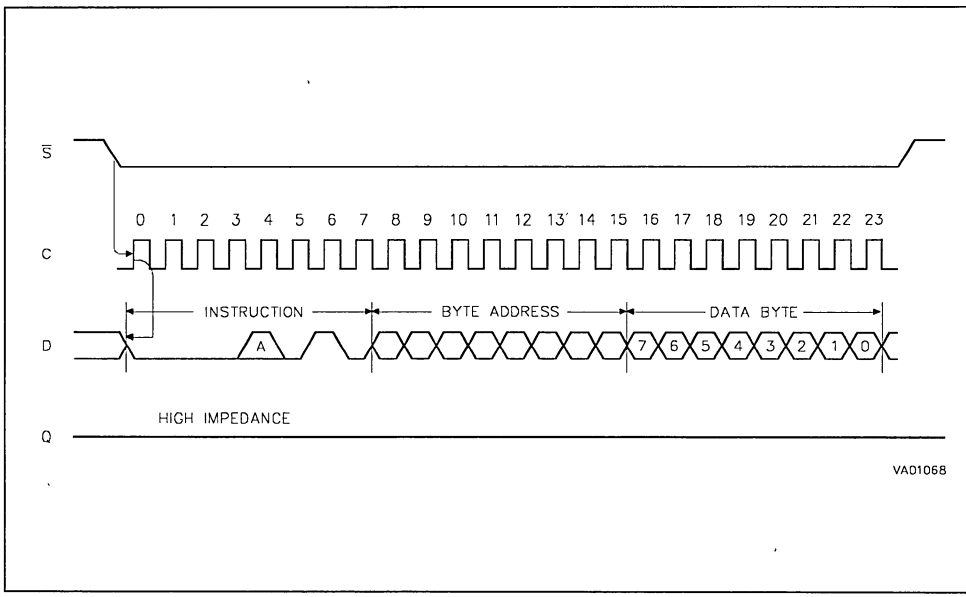


Figure 11. Page Write Operation Sequence

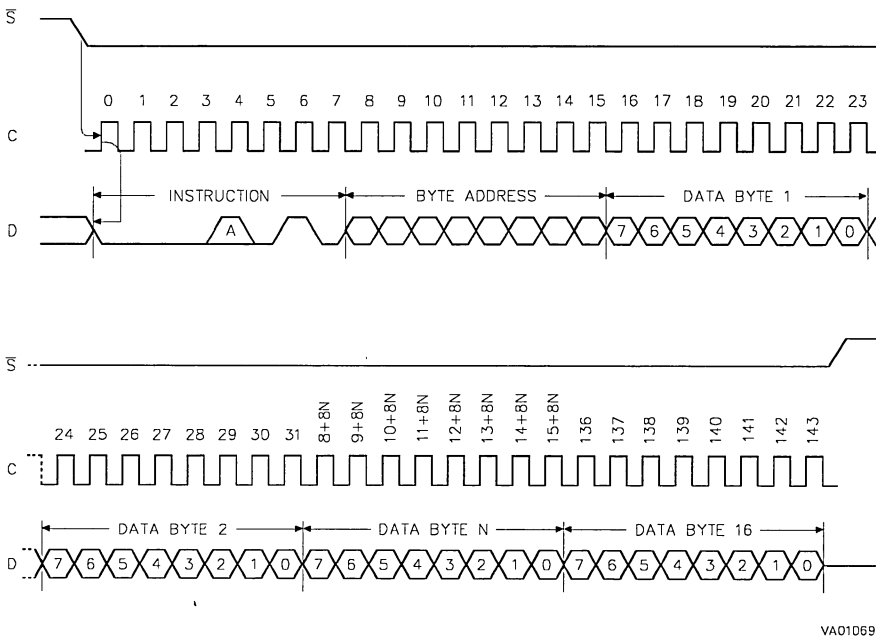


Figure 12. RDSR: Read Status Register Sequence

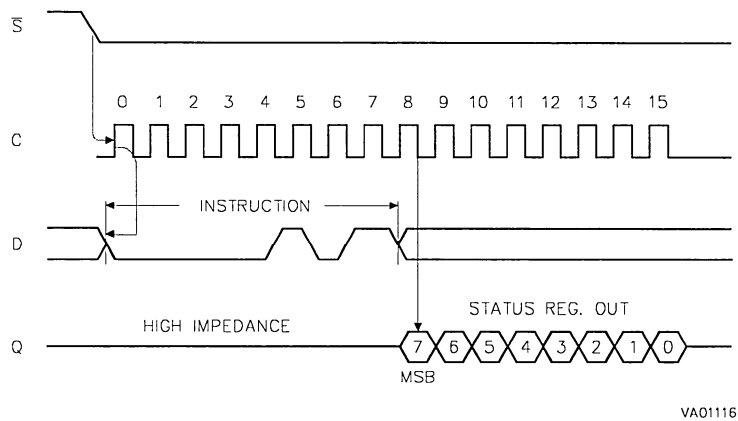
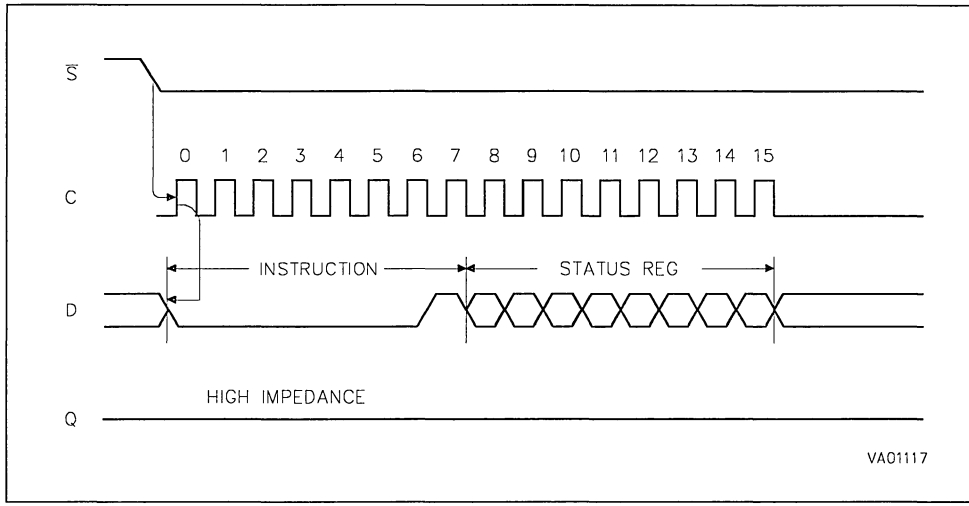


Figure 13. WRSR: Write Status Register Sequence



OPERATIONS (cont'd)

indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a non-volatile write cycle will be rejected and will deselect the chip.

Byte Write Operation

Prior to any write attempt, the write enable latch must have been set by issuing the WREN instruction. First, the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then, the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95C04P will set the write enable latch and then remain in standby until it is deselected. Then, the write state is entered by selecting the chip, issuing a one byte address (A7-A0), and one byte of data. Bit 3 of the write instruction contains address A8 (most significant address bit). $\overline{S}$ must remain low for the entire duration of the operation. The product must be deselected just after the eigth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is close to completion, the write enable latch is reset.

Page Write Operation

A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previous written data. The programming cycle will only start if the $\overline{S}$ transition does occur at the clock low pulse just after the eigth bit of data of a word is received.

POWER ON STATE

After a Power up the ST95P04C is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

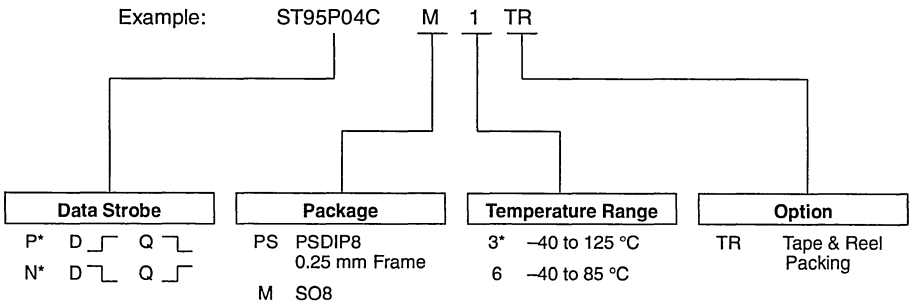
DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 5.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register). The Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is cancelled and the chip is automatically deselected; however, the programming cycle continues.
- After either of the following operations (WREN, WRDI, RDSR) is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

ORDERING INFORMATION SCHEME



Notes: P* Data In strobed on rising edge of the clock (C) and Data Out synchronized from the falling edge of the clock.
N* **On Request Only.** Data In strobed on the falling edge of the clock and Data Out synchronized on the rising edge of the clock.
3* Temperature range on request only.

For a list of available options (Package, Temperature Range, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PARALLEL EEPROM

PARALLEL ACCESS CMOS 64K (8K x 8) EEPROM

- FAST ACCESS TIME: 150, 200, 250ns
- SINGLE SUPPLY VOLTAGE: 5V ± 10%
- LOW POWER CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- FAST WRITE CYCLE:
  - 32 Bytes Page Write Operation
  - Byte or Page Write Cycle: 5ms
- ENHANCED END OF WRITE DETECTION:
  - Ready/Busy Open Drain Output
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABLITY SINGLE POLYSILICON, CMOS TECHNOLOGY:
  - Endurance > 100,000 Erase/Write Cycles
  - Data Retention > 10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- ADDRESS and DATA LATCHED ON-CHIP

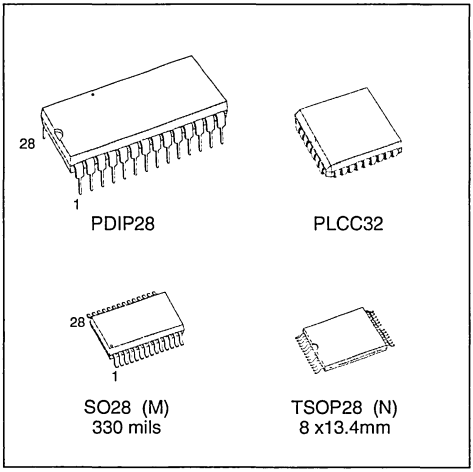
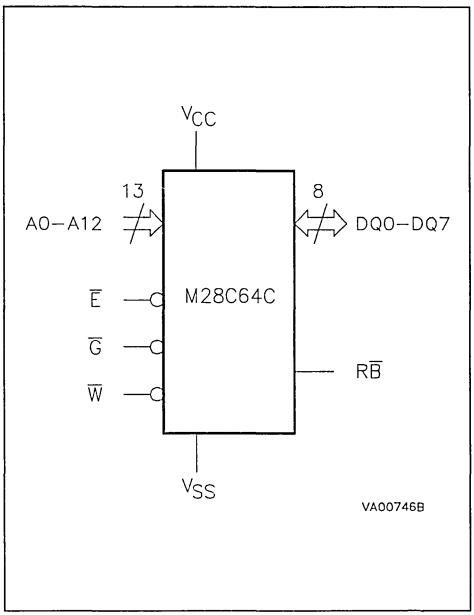


Figure 1. Logic Diagram



DESCRIPTION

The M28C64C is an 8K x 8 low power EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time (150ns) with low power dissipation and requires a 5V power supply.

Table 1. Signal Names

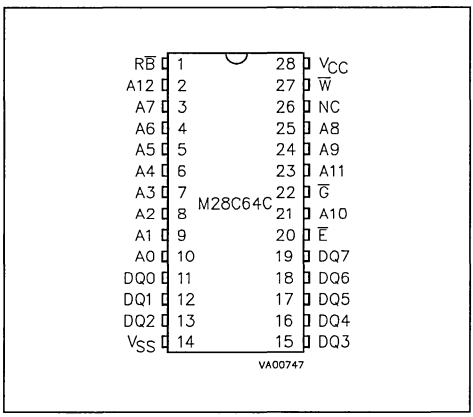
A0 - A12	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 6	0 to 70 – 40 to 85	°C
T_{STG}	Storage Temperature Range		– 65 to 150	°C
V_{CC}	Supply Voltage		– 0.3 to 6.5	V
V_{IO}	Input/Output Voltage		– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage		– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)		2000	V

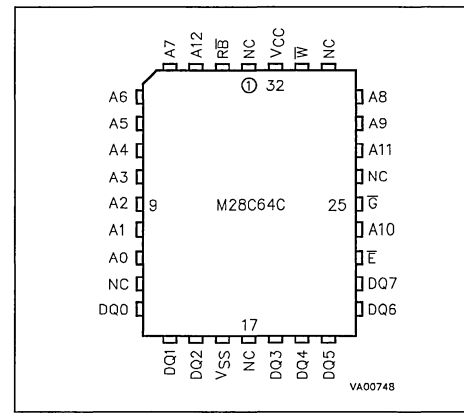
Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

Figure 2A. DIP Pin Connections



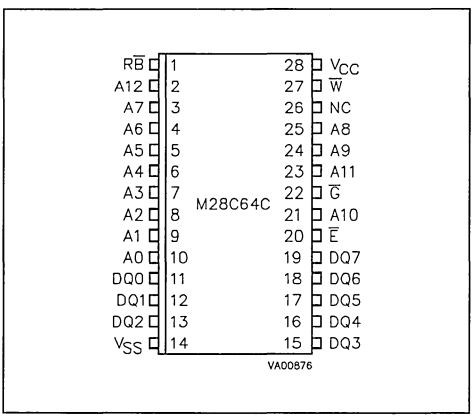
Warning: NC = No Connection

Figure 2B. LCC Pin Connections



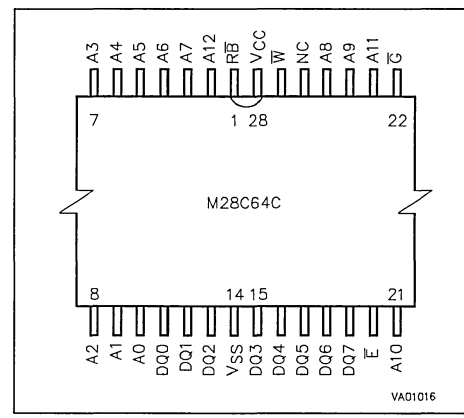
Warning: NC = No Connection

Figure 2C. SO Pin Connections



Warning: NC = No Connection

Figure 2D. TSOP Pin Connections



Warning: NC = No Connection

Figure 3. Block Diagram

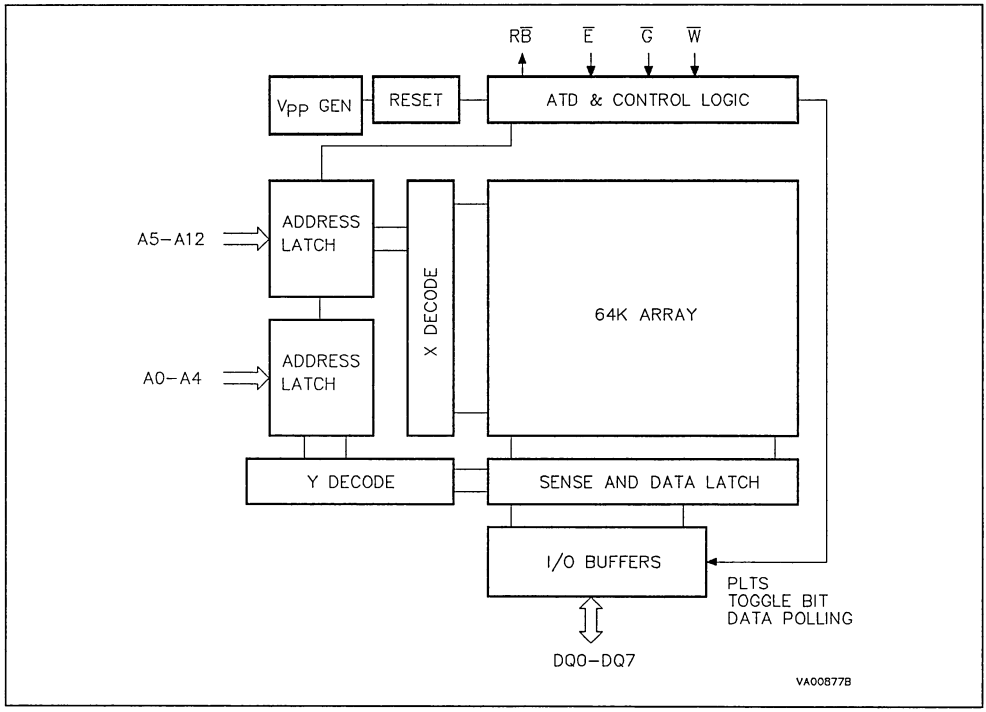


Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z

Note: X = V_{IH} or V_{IL}

DESCRIPTION (cont'd)

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking with Ready/Busy, Data Polling and Toggle Bit. The M28C64C supports 32 byte page write operation.

PIN DESCRITPION

Addresses (A0-A12). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

PIN DESCRIPTION (cont'd)

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28C64C through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28C64C.

Ready/Busy ($R\overline{B}$). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle.

OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming cicuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 6.

Read

The M28C64C is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high.The M28C64C supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion within 5ms.

Page Write

Page write allows up to 32 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A5 - A12 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data up to a maximum of 100µs after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first (t_{BLC}). If a transition of $\overline{E}$ or $\overline{W}$ is not detected within 100µs, the internal programming cycle will start.

Microcontroller Control Interface

The M28C64C provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the $R\overline{B}$ signal on a separate pin.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28C64C also offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by $\overline{E}$ or $\overline{W}$ up to 100µs after the previous byte. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low (t_{PLTS}). DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Ready/Busy pin. The $R\overline{B}$ pin provides a signal at its open drain output which is low during the erase/write cycle, but which is released at the completion of the programming cycle.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Input Output Waveforms

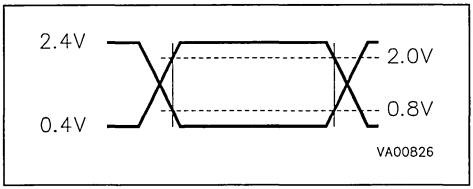


Figure 6. AC Testing Equivalent Load Circuit

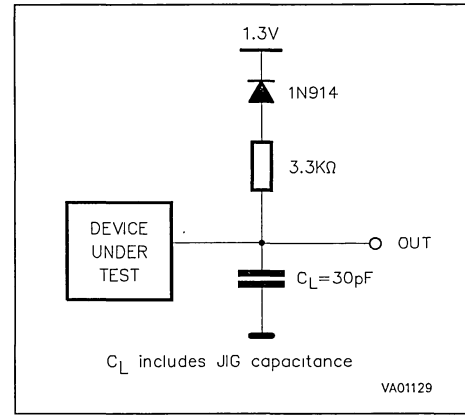


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics (T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC}	Supply Current (TTL and CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		2	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		100	µA
V_{IL}	Input Low Voltage		– 0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V

Table 6. Power Up Timing (1) (T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation	1		µs
t_{PUW}	Time Delay to Write Operation	10		ms

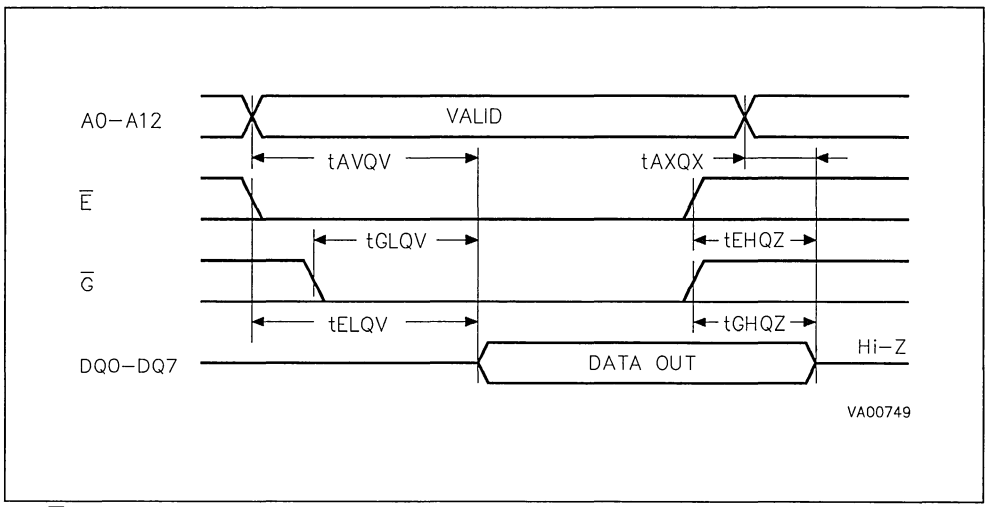
Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	M28C64C						Unit
				-150		-200		-250		
				min	max	min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		150		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		75		100		110	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	50	0	60	0	65	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	60	0	65	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. Read Mode AC Waveforms



Note: $\overline{W}$ = High

Table 8. Write Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 5V ±10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		150		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		150		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}		1	µs
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		150		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		150		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		10		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		10		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		30		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		30		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		200		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time			100	µs
t_{WHRH}	t_{WC}	Write Cycle Time			5	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		150	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		150	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. With a 3.3 kΩ pull-up resistor.

Figure 8. Write Mode AC Waveforms - Write Enable Controlled

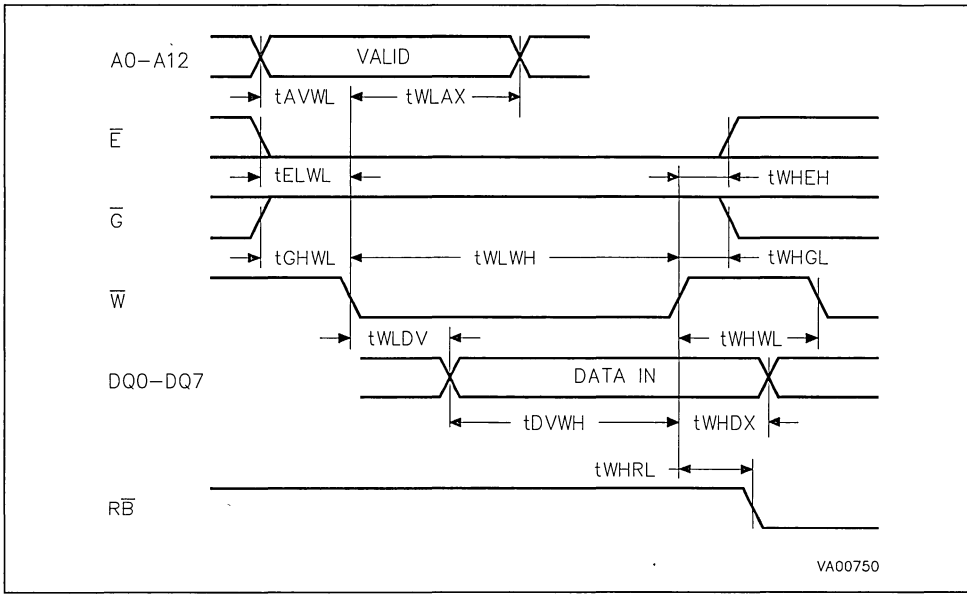


Figure 9. Write Mode AC Waveforms - Chip Enable Controlled

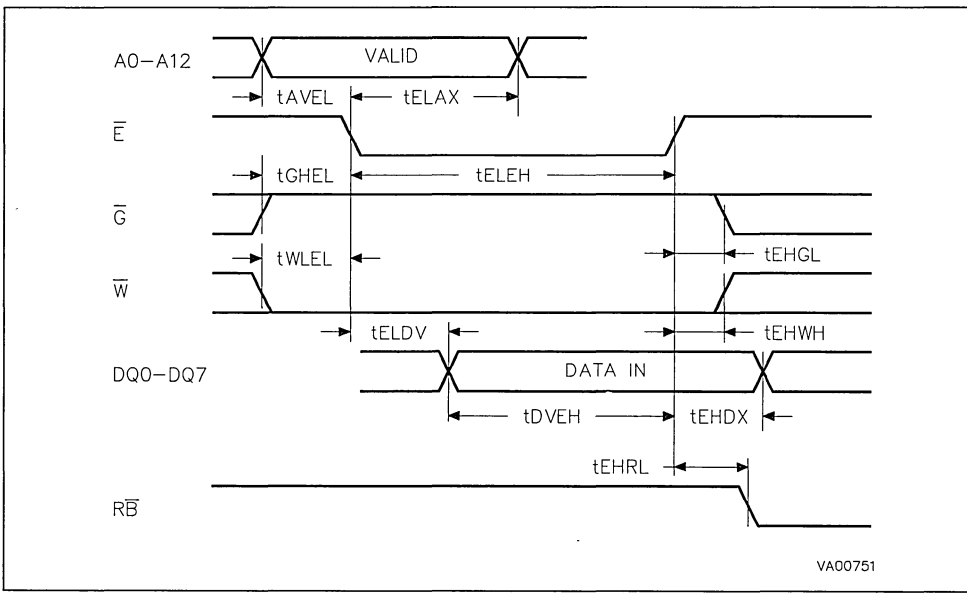


Figure 10. Page Write Mode AC Waveforms - Write Enable Controlled

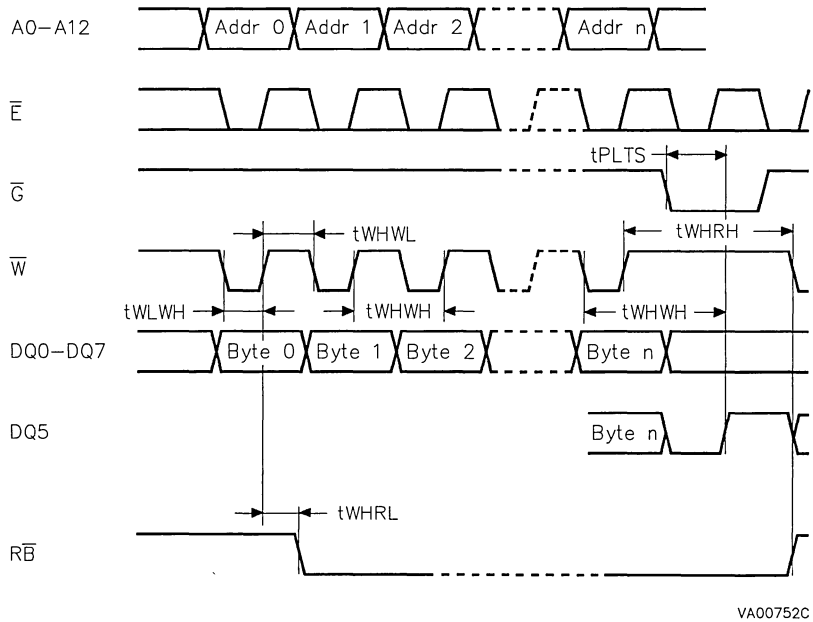


Figure 11. Data Polling Waveforms Sequence

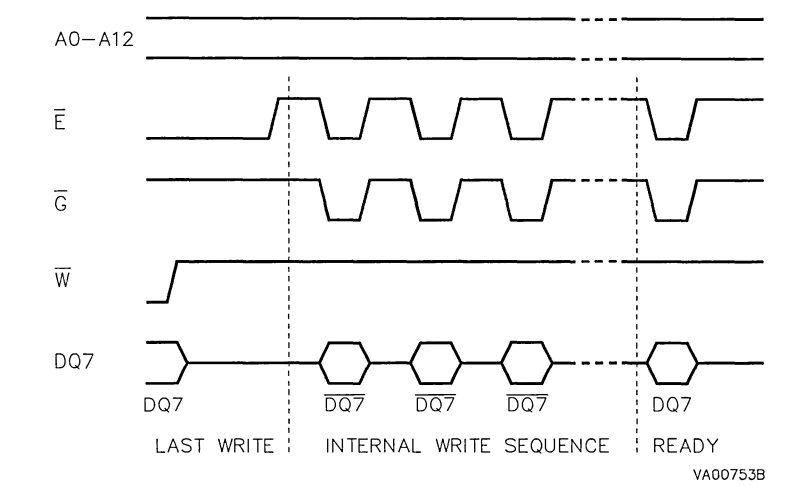
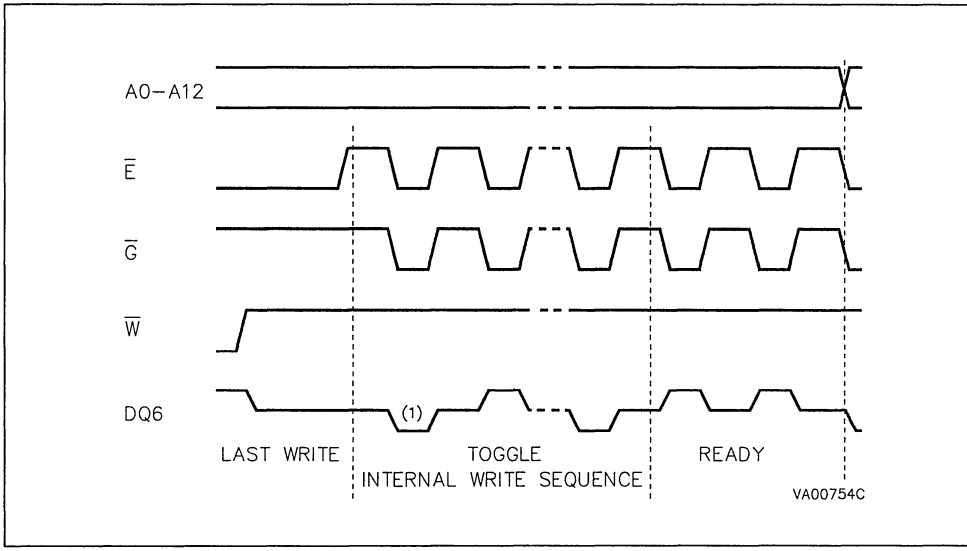


Figure 12. Toggle Bit Waveforms Sequence



Note: 1. First Toggle bit is forced to '0'

ORDERING INFORMATION SCHEME

Example: M28C64C -150 K 1

Speed		Package		Temperature Range	
-150	150 ns	K	PLCC32	1	0 to 70 °C
-200	200 ns	P	PDIP28	6	–40 to 85 °C
-250	250 ns	M	SO28 330 mils		
		N	TSOP28 8 x 13.4mm		

For a list of available options (Speed, Package, Temperature Range, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FAST SRAM

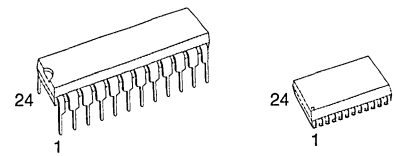
SGS-THOMSON MICROELECTRONICS

M624064

VERY FAST CMOS 64K x 4 SRAM

ADVANCE DATA

- 64K x 4 CMOS FAST SRAM
- EQUAL CYCLE and ACCESS TIMES: 12, 15, 20ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ and DIP, 300 mil PACKAGES



PSDIP24 (PS)

SOJ24 (E)
300 mils

DESCRIPTION

The M624064 is a 256K (262,144 bit) Fast CMOS SRAM, organized as 65,536 words by 4 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Figure 1. Logic Diagram

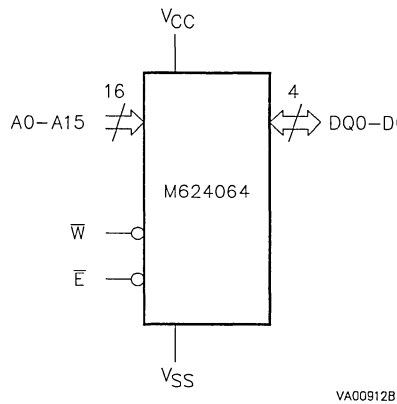


Table 1. Signal Names

A0 - A15	Address Inputs
DQ0 - DQ3	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. SDIP Pin Connections

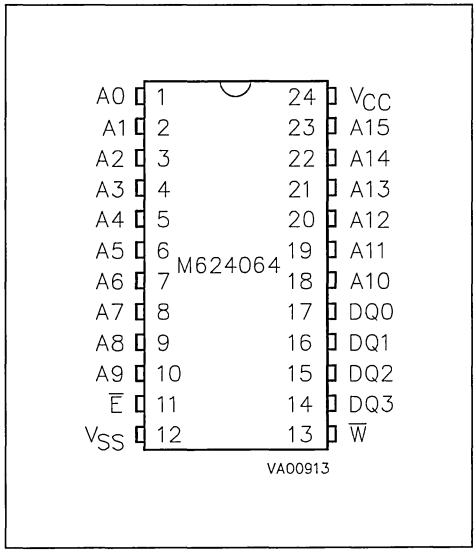


Figure 2B. SOJ Pin Connections

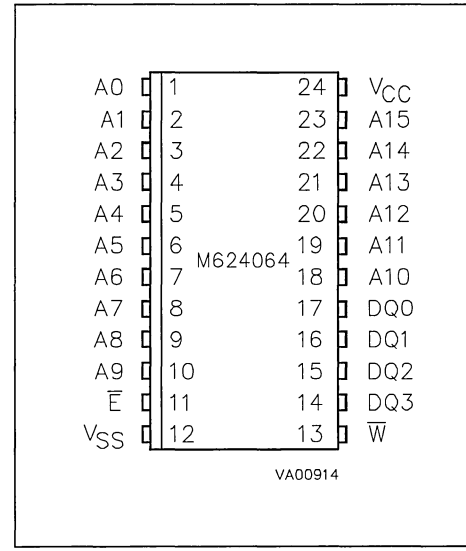


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (3)	Output Current	20	mA
P_D	Power Dissipation	1	W

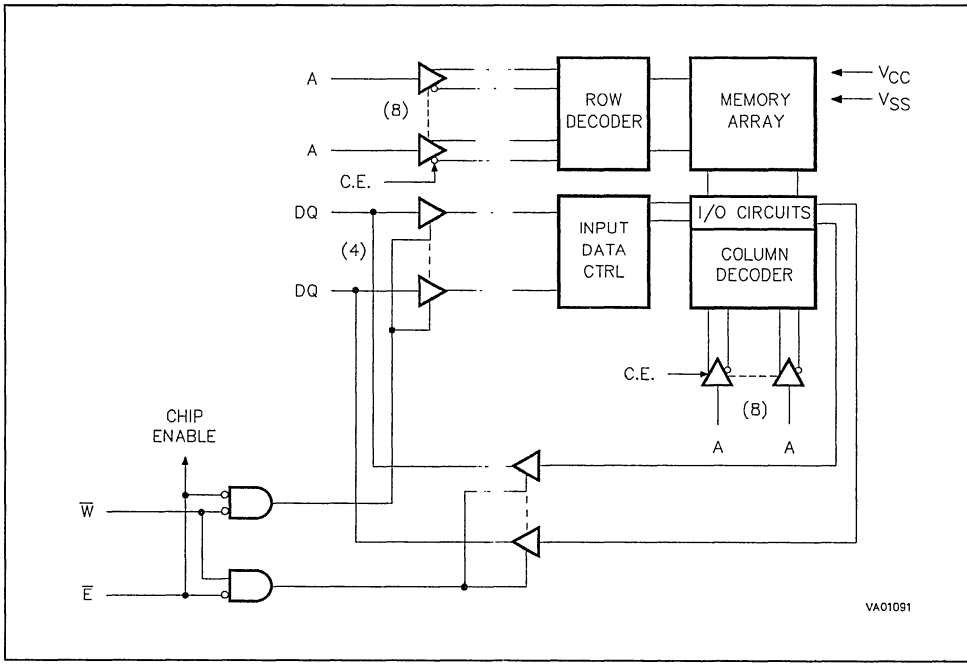
Note: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Up to a maximum operating V_{CC} of 5.5V only.
3. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	DQ0-DQ3	Power
Read	V_{IL}	V_{IH}	Data Output	Active
Write	V_{IL}	V_{IL}	Data Input	Active
Deselect	V_{IH}	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

Figure 3. Block Diagram



READ MODE

The M624064 is in the Read mode whenever Write Enable ($\overline{W}$) is high, with Chip Enable ($\overline{E}$) asserted low. This provides access to data from four of the 262,144 locations in the static memory array, specified by the 16 address inputs. Valid data will be available at the four output pins within t_{AVQV} after the last stable address, providing $\overline{E}$ is Low. If Chip Enable access time is not met, data access will be measured from the limiting parameter (t_{ELQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, but datalines will always be valid at t_{AVQV}.

WRITE MODE

The M624064 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Either the Chip Enable input ($\overline{E}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

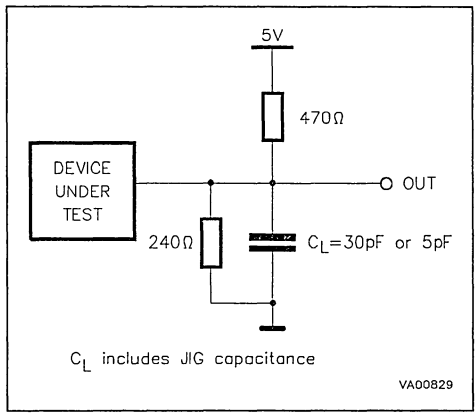


Table 4. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		8	pF
C_{OUT} [2]	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC1} [1]	Supply Current	V_{CC} = 5.5V, (-12)		160	mA
		V_{CC} = 5.5V, (-15)		160	mA
		V_{CC} = 5.5V, (-20)		160	mA
I_{CC2} [2]	Supply Current (Standby) TTL	V_{CC} = 5.5V, $\overline{E}$ ≥ V_{IH}, f = 0		25	mA
I_{CC3} [3]	Supply Current (Standby) CMOS	V_{CC} = 5.5V, $\overline{E}$ ≥ V_{CC} – 0.2V, f = 0		1	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at V_{IL} ≤ 0.8V or V_{IH} ≥ 2.2V
3. All other Inputs at V_{IL} ≤ 0.2V or V_{IH} ≥ V_{CC} – 0.2V

WRITE MODE (cont'd)

If the Output is enabled ($\overline{E}$ = Low), then Write Enable ($\overline{W}$) will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$ whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

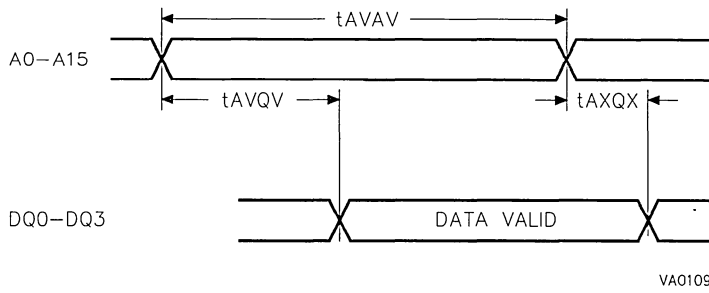
The M624064 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E}$ = High). Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$ as summarized in the Operating Modes table.

Table 6. Read and Standby Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M624064						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		12		15		20	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		12		15		20	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	3		3		3		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		ns
t_{PU} (3)	Chip Enable to Power Up	0		0		0		ns
t_{PD} (3)	Chip Enable to Power Down		12		15		20	ns

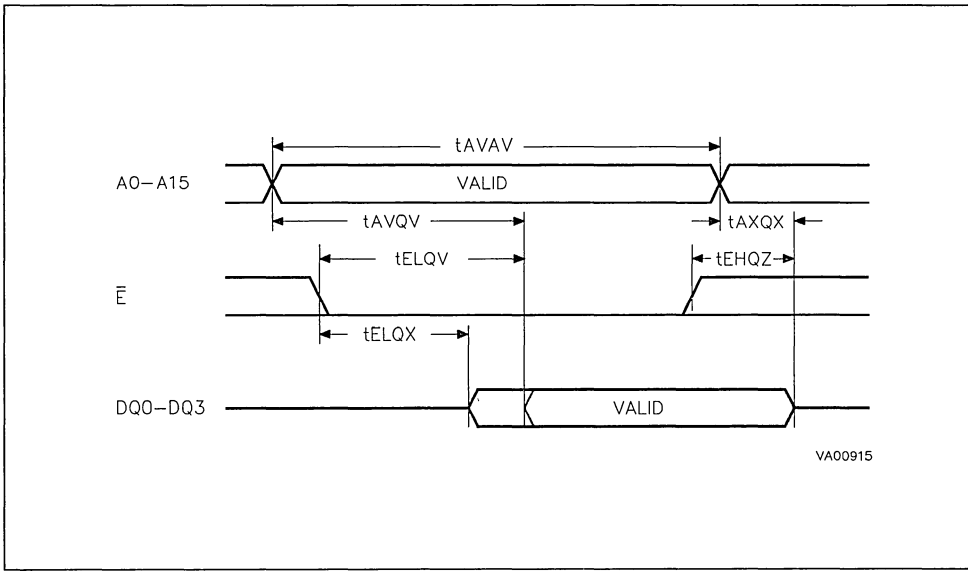
Notes: 1. C_L = 30pF (see Figure 4)
2. C_L = 5pF (see Figure 4)
3. Guaranteed but not tested (see Figure 7)

Figure 5. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{W}$ = High

Figure 6. Chip Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High

Figure 7. Standby Mode AC Waveforms

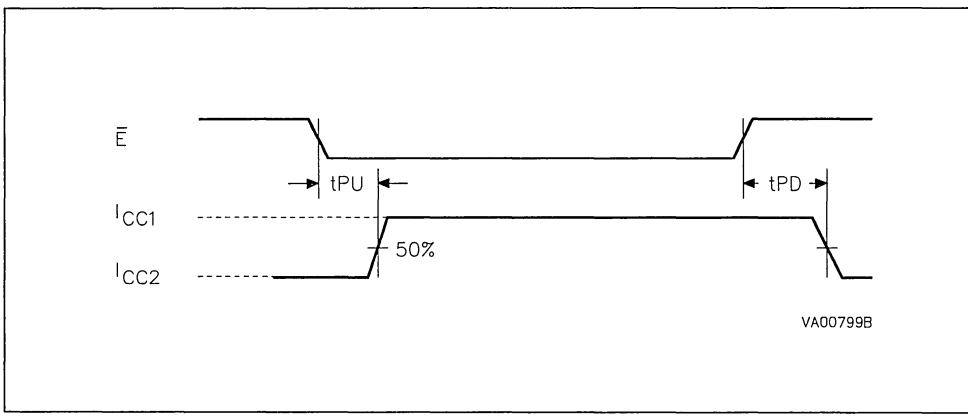


Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M624064						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	9		10		12		ns
t_{AVEH}	Address Valid to Chip Enable High	9		10		12		ns
t_{WLWH}	Write Enable Pulse Width	9		10		12		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	9		10		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	7		8		10		ns
t_{DVEH}	Input Valid to Chip Enable High	7		8		10		ns

Note: 1. C_L = 5pF (see Figure 4)

Figure 8. Write Enable Controlled, Write AC Waveforms

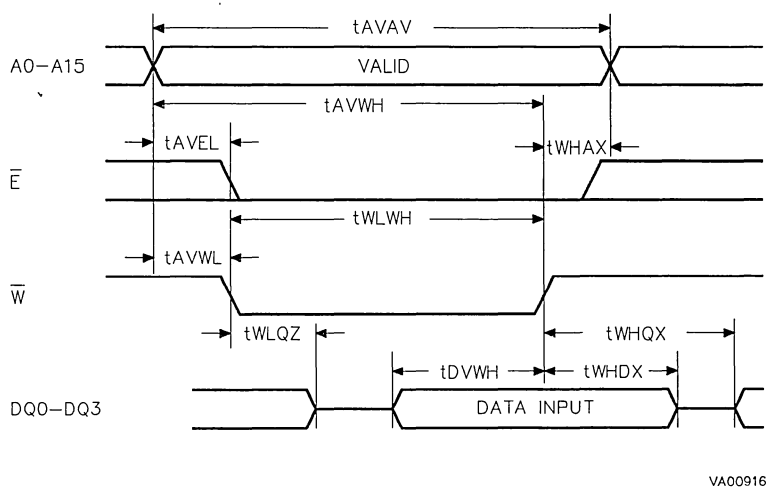


Figure 9. Chip Enable Controlled, Write AC Waveforms

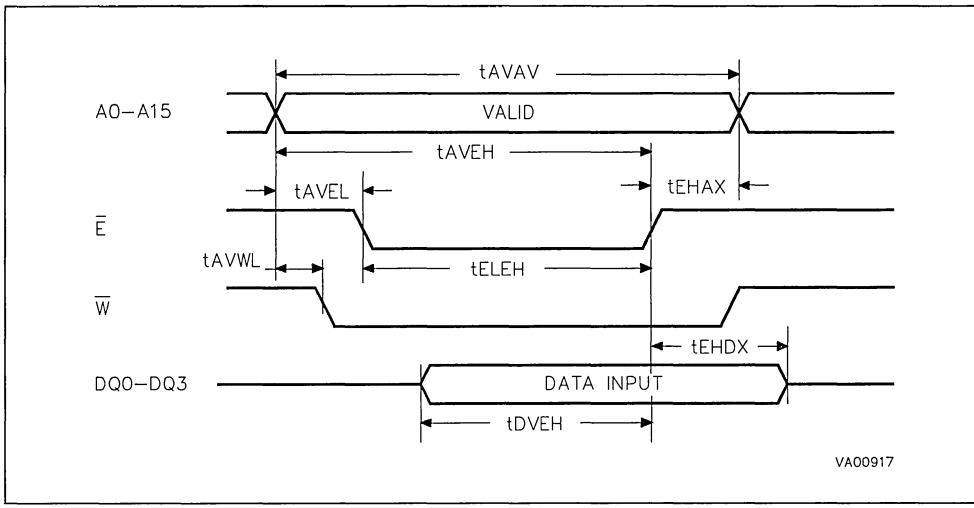
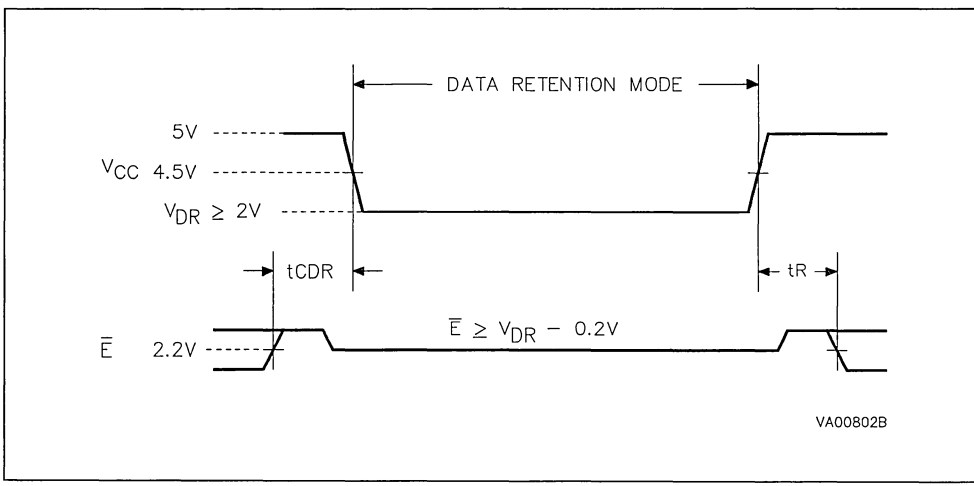


Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 2V to 4.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CCDR} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E} \geq V_{CC} - 0.2V$, f = 0		200	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E} \geq V_{CC} - 0.2V$, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E} \geq V_{CC} - 0.2V$, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

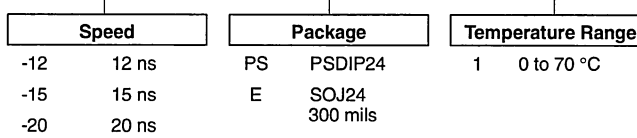
Notes: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.2V$ or $V_{IL} \leq 0\ 2V$
2. See Figure 10 for measurement points. Guaranteed but not tested

Figure 10. Low V_{CC} Data Retention AC Waveforms



ORDERING INFORMATION SCHEME

Example: M624064 -12 E 1



Speed		Package		Temperature Range	
-12	12 ns	PS	PSDIP24	1	0 to 70 °C
-15	15 ns	E	SOJ24 300 mils		
-20	20 ns				

For a list of available options (Speed, Package etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

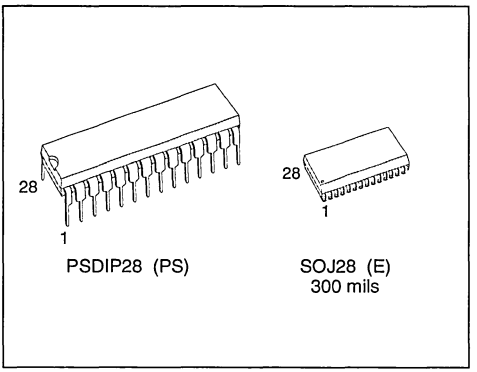
SGS-THOMSON MICROELECTRONICS

M624065

VERY FAST CMOS 64K x 4 SRAM WITH OUTPUT ENABLE

ADVANCE DATA

- 64K x 4 CMOS FAST SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 12, 15, 20ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ and DIP, 300 mil PACKAGES



PSDIP28 (PS)

SOJ28 (E)
300 mils

DESCRIPTION

The M624065 is a 256K (262,144 bit) Fast CMOS SRAM, organized as 65,536 words by 4 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Figure 1. Logic Diagram

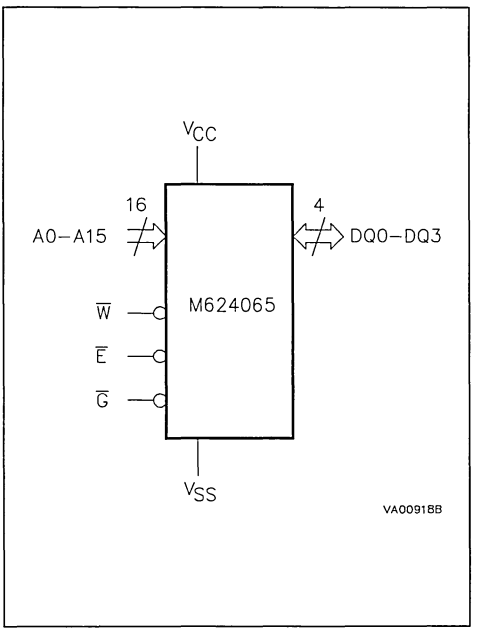


Table 1. Signal Names

A0 - A15	Address Inputs
DQ0 - DQ3	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. SDIP Pin Connections

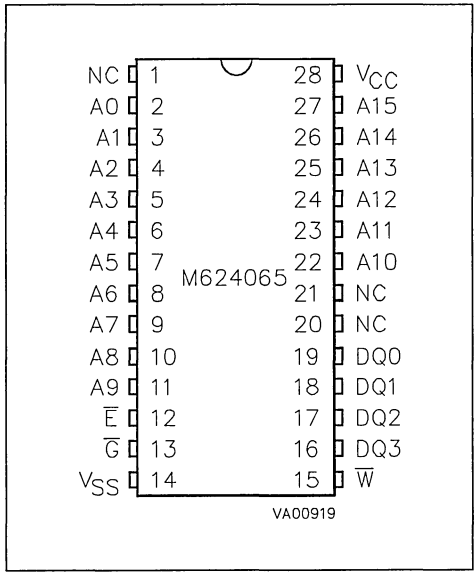


Figure 2B. SOJ Pin Connections

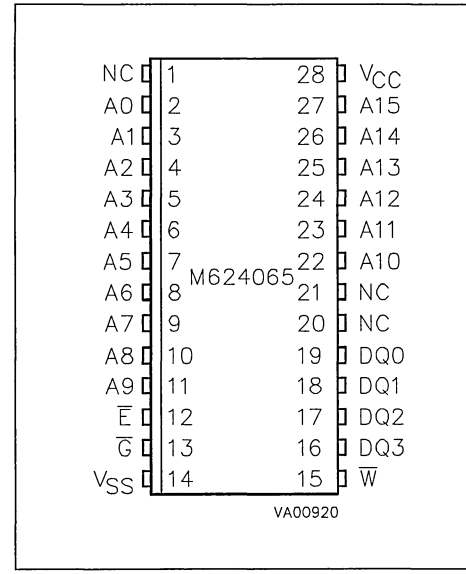


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	20	mA
P_D	Power Dissipation	1	W

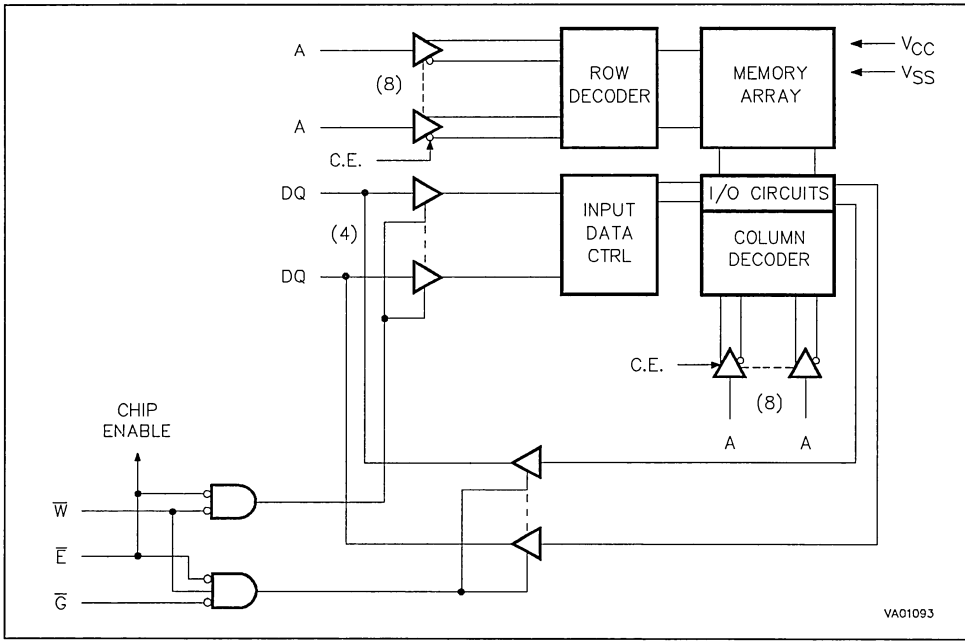
Note: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Up to a maximum operating V_{CC} of 5.5V only.
3. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ0-DQ3	Power
Read	V_{IL}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

Figure 3. Block Diagram



READ MODE

The M624065 is in the Read mode whenever Write Enable ($\overline{W}$) is High, with Output Enable ($\overline{G}$) Low, with Chip Enable ($\overline{E}$) asserted Low. This provides access to data from four of the 262,144 locations in the static memory array, specified by the 16 address inputs. Valid data will be available at the four output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low, and $\overline{E}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The M624065 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Chip Enable $\overline{E}$ or $\overline{W}$ must be deasserted during Address transitions for subsequent write cycles. The Write begins with the concurrence of Chip Enable and $\overline{W}$ being asserted low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively and is determined to the latter concurrence edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$. If the Output is Enabled ($\overline{E}$ = Low, $\overline{G}$ = Low), then $\overline{W}$ will return the

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

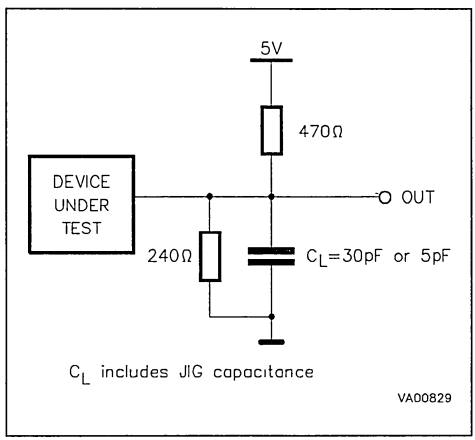


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance an all pins (except DQ)	V_{IN} = 0V		8	pF
C_{OUT} (2)	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC1} (1)	Supply Current	V_{CC} = 5.5V, (-12)		160	mA
		V_{CC} = 5.5V, (-15)		160	mA
		V_{CC} = 5.5V, (-20)		160	mA
I_{CC2} (2)	Supply Current (Standby) TTL	V_{CC} = 5.5V, $\overline{E}$ = V_{IH}, f = 0		25	mA
I_{CC3} (3)	Supply Current (Standby) CMOS	V_{CC} = 5.5V, $\overline{E}$ ≥ V_{CC} – 0.2V, f = 0		1	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at V_{IL} ≤ 0.8V or V_{IH} ≥ 2.2V
3. All other Inputs at V_{IL} ≤ 0.2V or V_{IH} ≥ V_{CC} – 0.2V

WRITE MODE (cont'd)

outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$ whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

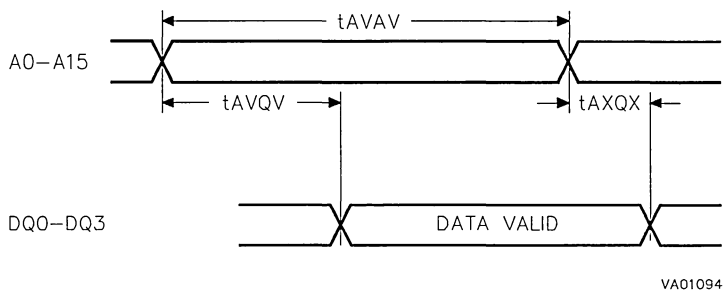
The M624065 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is deasserted ($\overline{E}$ = High). An Output Enable ($\overline{G}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$ as summarized in the Operating Modes table.

Table 6. Read and Standby Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M624065						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		12		15		20	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		12		15		20	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		7		8		10	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	3		3		3		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	7	0	8	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		ns
t_{PU} (3)	Chip Enable to Power Up	0		0		0		ns
t_{PD} (3)	Chip Enable to Power Down		12		15		20	ns

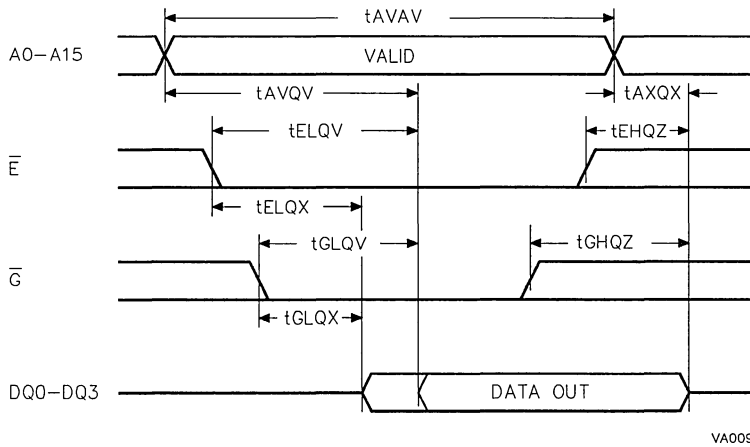
Notes: 1. C_L = 30pF (see Figure 4)
2. C_L = 5pF (see Figure 4)
3. Guranteed but not tested (see Figure 7)

Figure 5. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High

Figure 6. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High

Figure 7. Standby Mode AC Waveforms

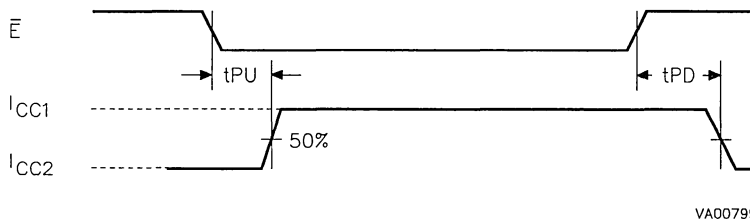
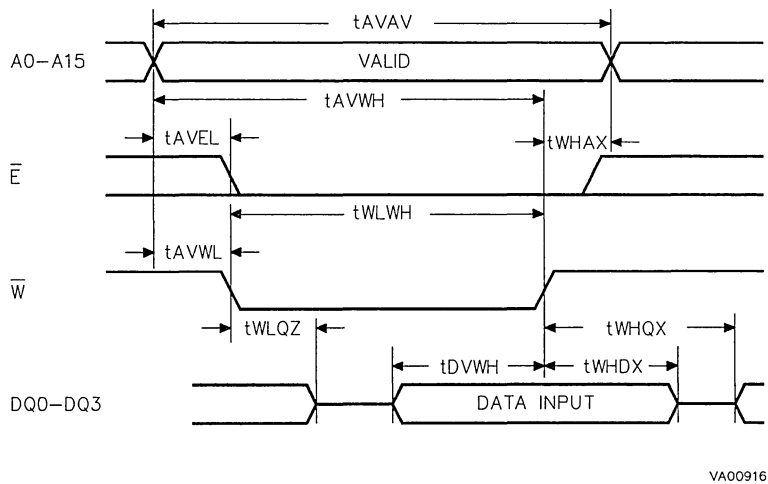


Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M624065						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	9		10		12		ns
t_{AVEH}	Address Valid to Chip Enable High	9		10		12		ns
t_{WLWH}	Write Enable Pulse Width	9		10		12		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	9		10		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	7		8		10		ns
t_{DVEH}	Input Valid to Chip Enable High	7		8		10		ns

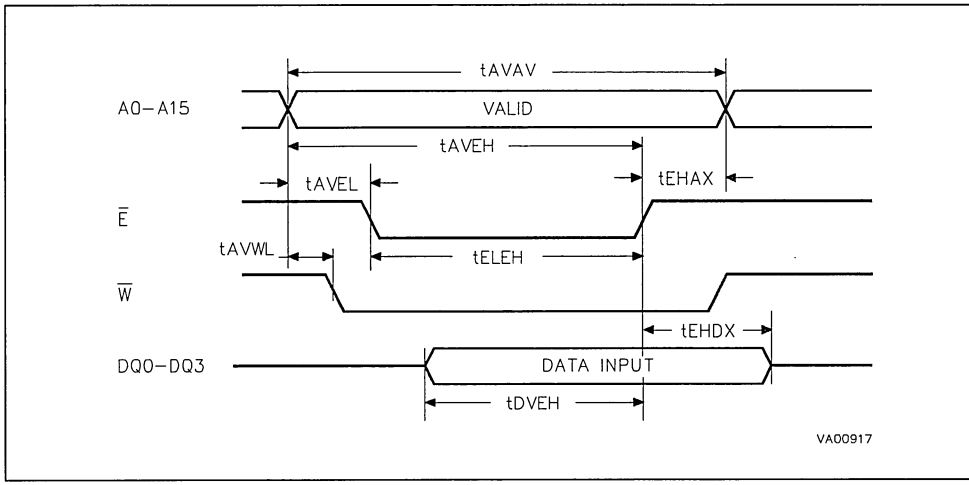
Note: 1. C_L = 5pF (see Figure 4)

Figure 8. Write Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = Low

Figure 9. Chip Enable Controlled, Write AC Waveforms



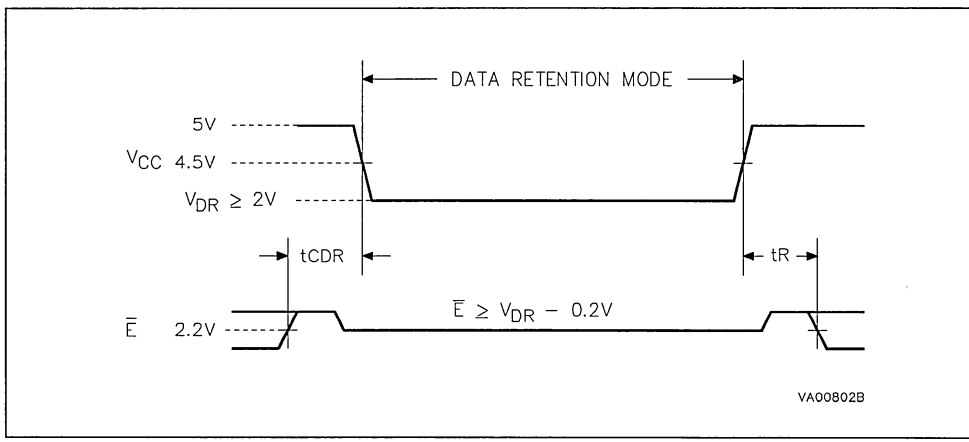
Note: $\overline{G}$ = High

Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 2V to 4.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CCDR} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E} \geq V_{CC} - 0.2V$, f = 0		200	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E} \geq V_{CC} - 0.2V$, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E} \geq V_{CC} - 0.2V$, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

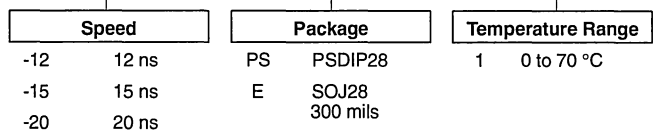
Notes: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.2V$ or $V_{IL} \leq 0.2V$
2. See Figure 10 for measurement points. Guaranteed but not tested.

Figure 10. Low V_{CC} Data Retention AC Waveforms



ORDERING INFORMATION SCHEME

Example: M624065 -12 E 1



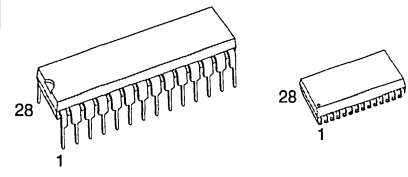
Speed		Package		Temperature Range	
-12	12 ns	PS	PSDIP28	1	0 to 70 °C
-15	15 ns	E	SOJ28 300 mils		
-20	20 ns				

For a list of available options (Speed, Package etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

VERY FAST CMOS 32K x 8 SRAM WITH OUTPUT ENABLE

- 32K x 8 CMOS FAST SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 12, 15, 20ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ and DIP, 300 mil PACKAGES



PSDIP28 (PS)

SOJ28 (E)
300 mils

DESCRIPTION

The M628032 is a 256K (262,144 bit) Fast CMOS SRAM, organized as 32,768 words by 8 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

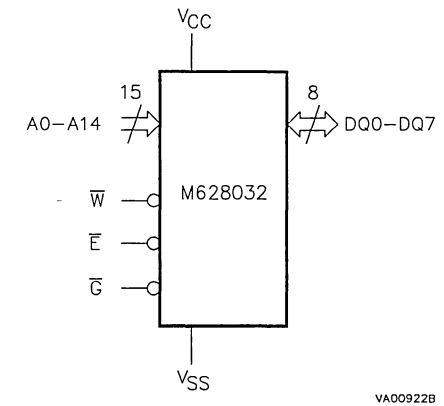


Figure 2A. SDIP Pin Connections

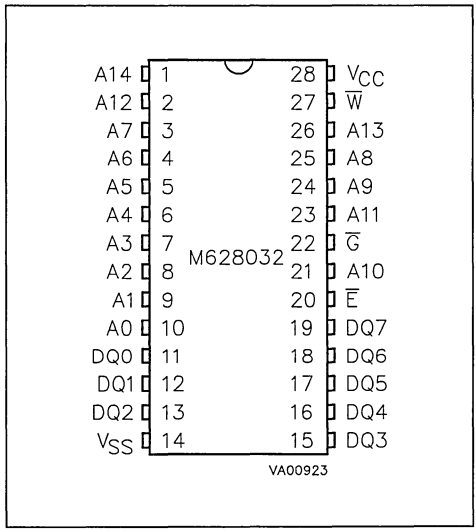


Figure 2B. SOJ Pin Connections

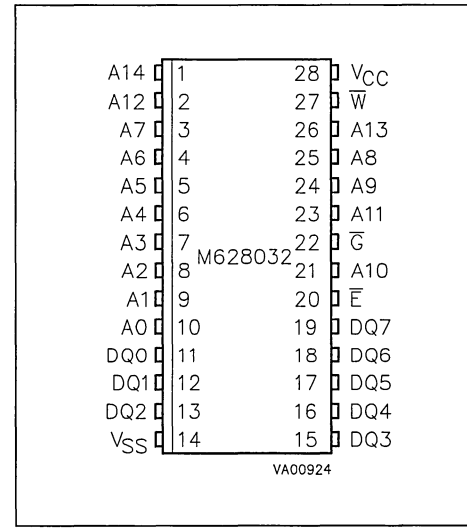


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (3)	Output Current	20	mA
P_D	Power Dissipation	1	W

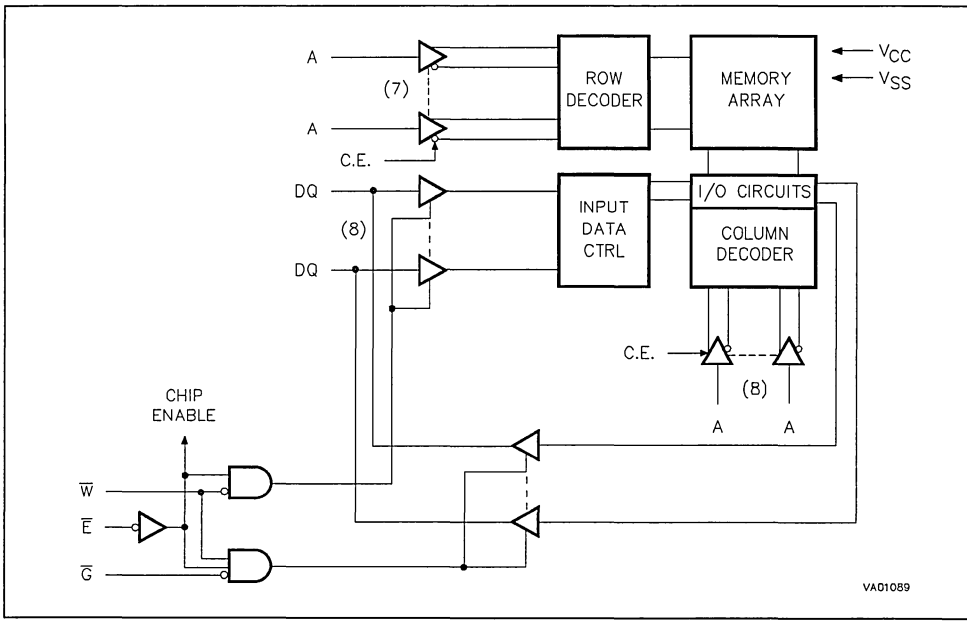
Notes: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Up to a maximum operating V_{CC} of 5.5V only.
3. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ0-DQ7	Power
Read	V_{IL}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

Figure 3. Block Diagram



READ MODE

The M628032 is in the Read mode whenever Write Enable ($\overline{W}$) is High, with Output Enable $\overline{G}$ Low, and Chip Enable ($\overline{E}$) asserted Low. This provides access to data from nine of the 262,144 locations in the static memory array, specified by the 15 address inputs. Valid data will be available at the eight output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low, and Chip Enable $\overline{E}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} and t_{GLQX}, but datalines will always be valid at t_{AVQV}.

WRITE MODE

The M628032 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Chip Enable input $\overline{E}$ or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

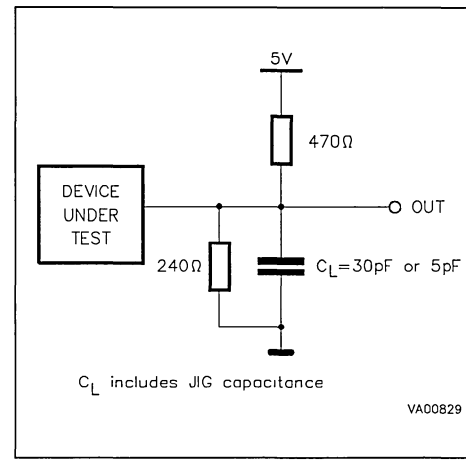


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		8	pF
C_{OUT} (2)	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC1} (1)	Supply Current	V_{CC} = 5.5V, (-12)		160	mA
		V_{CC} = 5.5V, (-15)		160	mA
		V_{CC} = 5.5V, (-20)		160	mA
I_{CC2} (2)	Supply Current (Standby) TTL	V_{CC} = 5.5V, $\overline{E}$ = V_{IH}, f = 0		25	mA
I_{CC3} (3)	Supply Current (Standby) CMOS	V_{CC} = 5.5V, $\overline{E}$ ≥ V_{CC} – 0.2V, f = 0		1	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at V_{IL} ≤ 0.8V or V_{IH} ≥ 2.2V
3. All other Inputs at V_{IL} ≤ 0.2V or V_{IH} ≥ V_{CC} – 0.2V

WRITE MODE (cont'd)

If the Output is enabled ($\overline{E}$ = Low and $\overline{G}$ = Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$, whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

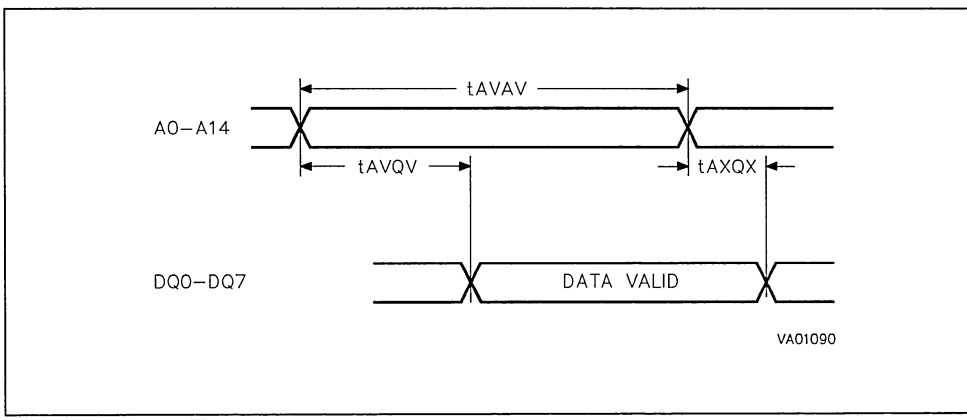
The M628032 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E}$ = High). An Output Enable ($\overline{G}$) pin provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$ as summarized in the Operating Modes table.

Table 6. Read and Standby Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M628032						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		12		15		20	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		12		15		20	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		7		8		10	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	3		3		3		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	7	0	8	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		ns
t_{PU} (3)	Chip Enable to Power Up	0		0		0		ns
t_{PD} (3)	Chip Enable to Power Down		12		15		20	ns

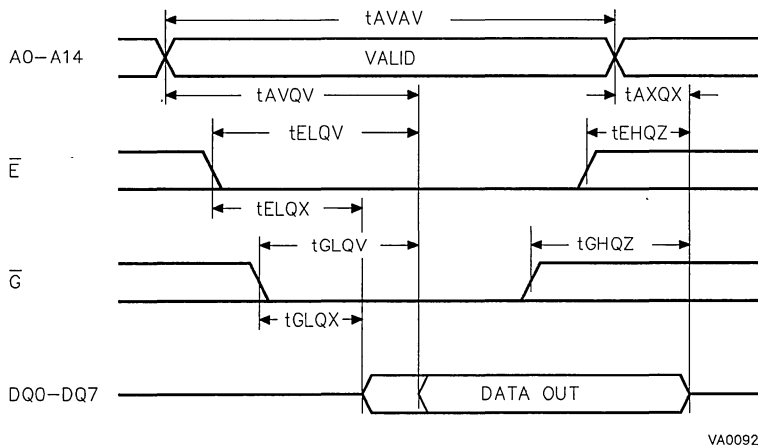
Notes: 1. C_L = 30pF (see Figure 4)
2. C_L = 5pF (see Figure 4)
3. Guaranteed but not tested (see Figure 7)

Figure 5. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High

Figure 6. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High

Figure 7. Standby Mode AC Waveforms

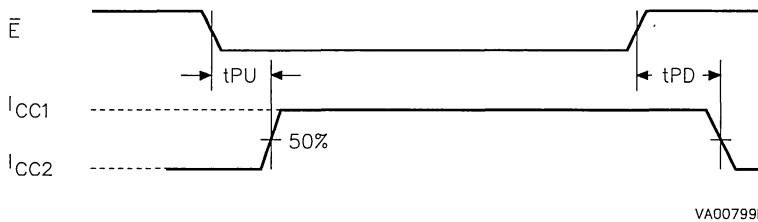
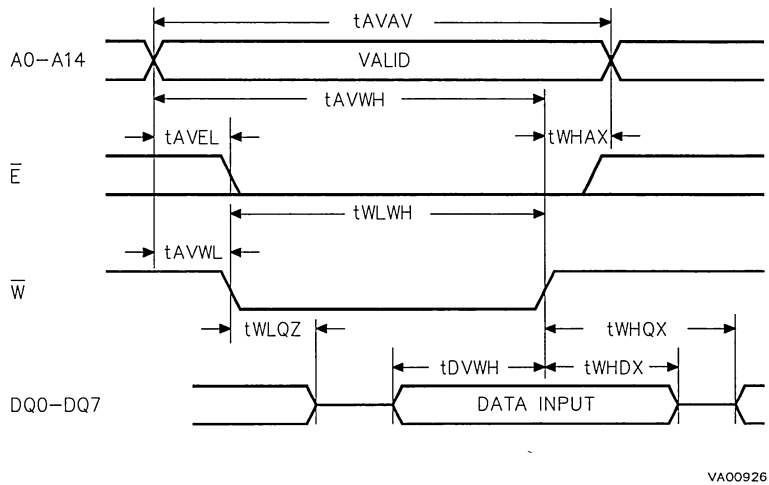


Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M628032						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	9		10		12		ns
t_{AVEH}	Address Valid to Chip Enable High	9		10		12		ns
t_{WLWH}	Write Enable Pulse Width	9		10		12		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	9		10		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	7		8		10		ns
t_{DVEH}	Input Valid to Chip Enable High	7		8		10		ns

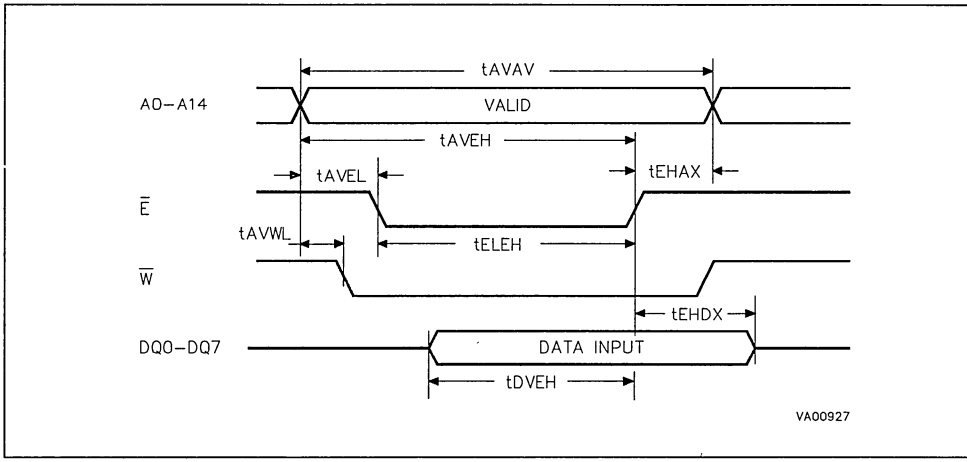
Note: 1. C_L = 5pF (see Figure 4)

Figure 8. Write Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = Low

Figure 9. Chip Enable Controlled, Write AC Waveforms



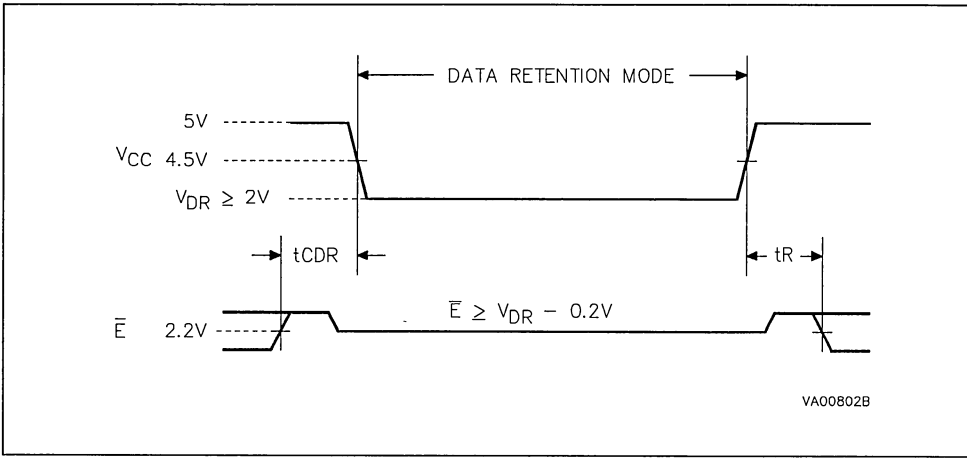
Note: $\overline{G}$ = High

Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 2V to 4.5V)

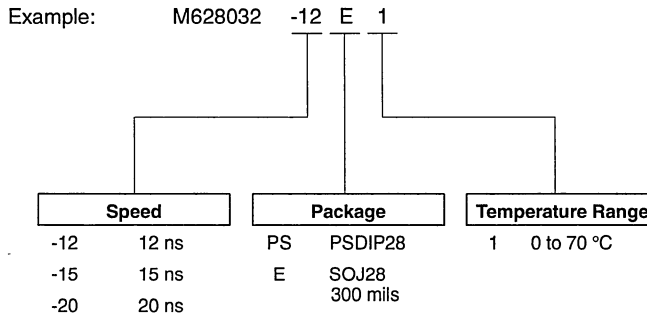
Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CCDR} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E} \geq V_{CC} - 0.2V$, f = 0		200	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E} \geq V_{CC} - 0.2V$, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E} \geq V_{CC} - 0.2V$, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

Notes: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.2V$ or $V_{IL} \leq 0.2V$
2. See Figure 10 for measurement points. Guaranteed but not tested

Figure 10. Low V_{CC} Data Retention AC Waveforms



ORDERING INFORMATION SCHEME



For a list of available options (Speed, Package etc...) refer to the Selector Gude in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

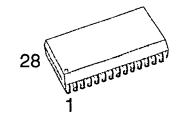
SGS-THOMSON MICROELECTRONICS

M624256

VERY FAST CMOS 1 Megabit (256K x 4) SRAM WITH OUTPUT ENABLE

ADVANCE DATA

- 256K x 4 CMOS FAST SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 15, 17, 20, 25ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ, 400 mil PACKAGE



SOJ28 (E)
400 mils

DESCRIPTION

The M624256 is a 1 Megabit (1,048,567 bit) Fast CMOS SRAM, organized as 262,144 words by 4 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Figure 1. Logic Diagram

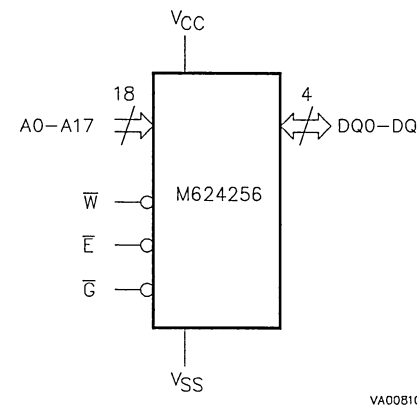


Table 1. Signal Names

A0 - A17	Address Inputs
DQ0 - DQ3	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (3)	Output Current	20	mA
P_D	Power Dissipation	1	W

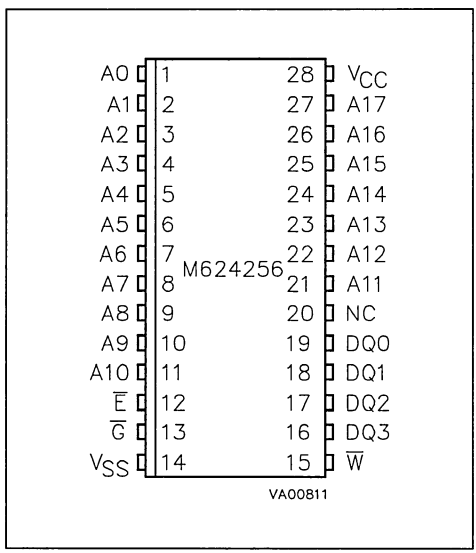
Notes: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Up to a maximum operating V_{CC} of 5.5V only.
3. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ0-DQ3	Power
Read	V_{IL}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}.

Figure 2. SOJ Pin Connections



Warning: NC = No Connection.

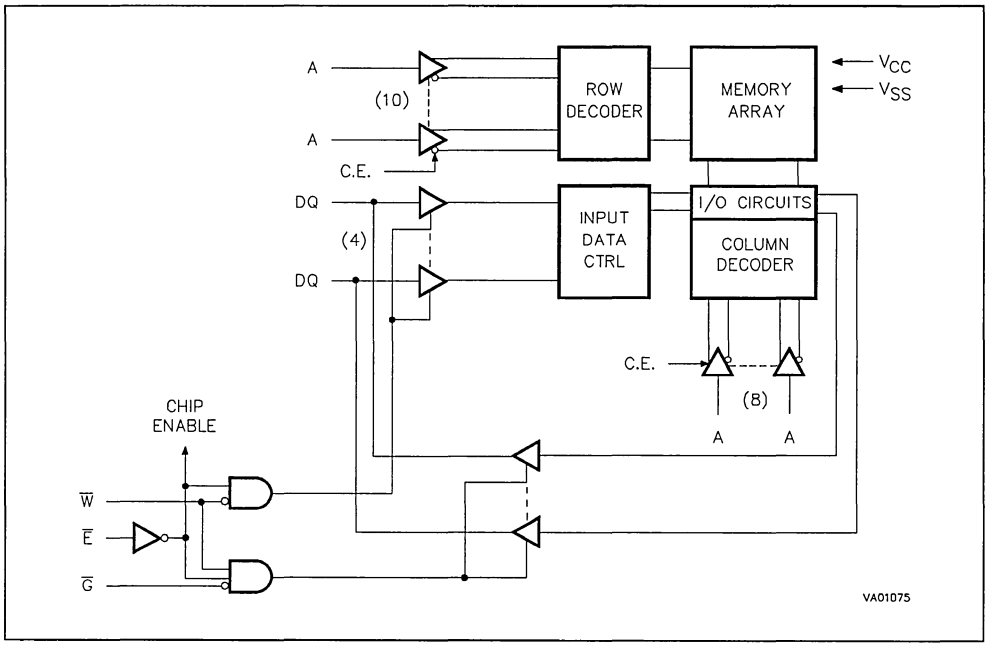
READ MODE

The M624256 is in the Read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and Chip Enable ($\overline{E}$) asserted. This provides access to data from four of the 1,048,576 locations in the static memory array, specified by the 18 address inputs. Valid data will be available at the four output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low and $\overline{E}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The M624256 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Either the Chip Enable input ($\overline{E}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively,

Figure 3. Block Diagram



WRITE MODE (cont'd)

and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

If the Output is enabled ($\overline{E}$ = Low and $\overline{G}$ = Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$ whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

The M624256 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E}$ = High). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$ as summarized in the Operating Modes table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

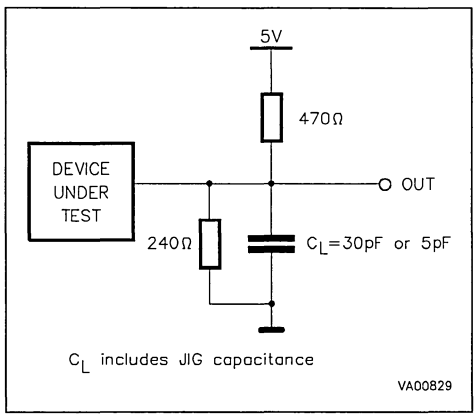


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN} (2)	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		8	pF
C_{OUT} (3)	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled only, not 100% tested
2. Except DQ0-DQ3
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC1} (1)	Supply Current	V_{CC} = 5.5V, (-15 & -17)		175	mA
		V_{CC} = 5.5V, (-20)		140	mA
		V_{CC} = 5.5V, (-25)		130	mA
I_{CC2} (2)	Supply Current (Standby) TTL	V_{CC} = 5.5V, $\overline{E}$ = V_{IH}, f = 0		25	mA
I_{CC3} (3)	Supply Current (Standby) CMOS	V_{CC} = 5.5V, $\overline{E}$ ≥ V_{CC} – 0.2V, f = 0		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

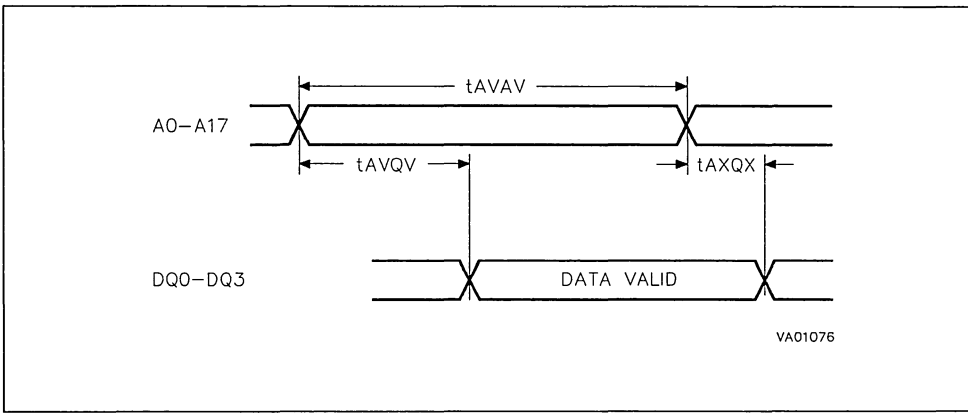
Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at V_{IL} ≤ 0.8V or V_{IH} ≥ 2.2V
3. All other Inputs at V_{IL} ≤ 0.2V or V_{IH} ≥ V_{CC} – 0.2V

Table 6. Read and Standby Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M624256								Unit
		-15		-17		-20		-25		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	15		17		20		25		ns
t_{AVQV} (1)	Address Valid to Output Valid		15		17		20		25	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		15		17		20		25	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		7		7		8		10	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	2		2		2		2		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	8	0	10	0	10	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	7	0	8	0	9	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		3		ns
t_{PU} (3)	Chip Enable Low to Power Up	0		0		0		0		ns
t_{PD} (3)	Chip Enable High to Power Down		15		17		20		25	ns

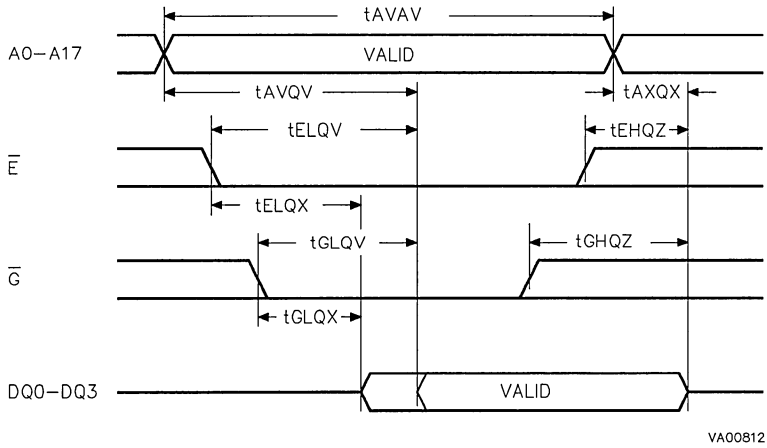
Notes: 1. C_L = 30pF (see Figure 4)
2. C_L = 5pF (see Figure 4)
3.Guaranteed but not tested (see Figure 7)

Figure 5. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High

Figure 6. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High

Figure 7. Standby Mode AC Waveforms

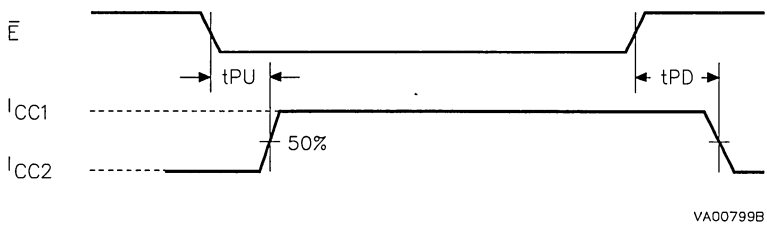
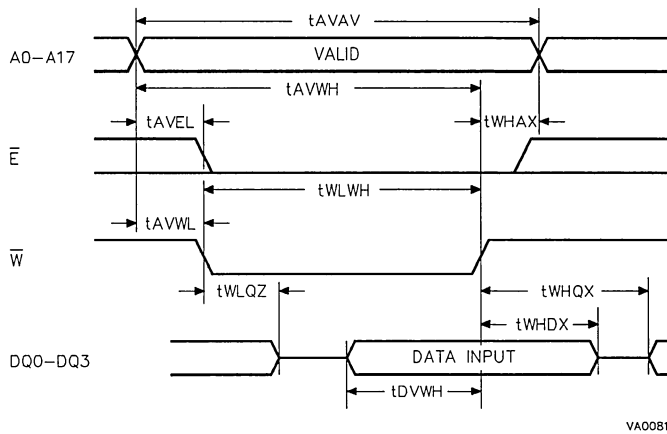


Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M624256								Unit
		-15		-17		-20		-25		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	15		17		20		25		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	10		12		12		15		ns
t_{AVEH}	Address Valid to Chip Enable High	11		12		12		15		ns
t_{WLWH}	Write Enable Pulse Width	10		12		12		15		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	0	12	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	11		12		12		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	8		10		12		12		ns
t_{DVEH}	Input Valid to Chip Enable High	8		10		12		12		ns

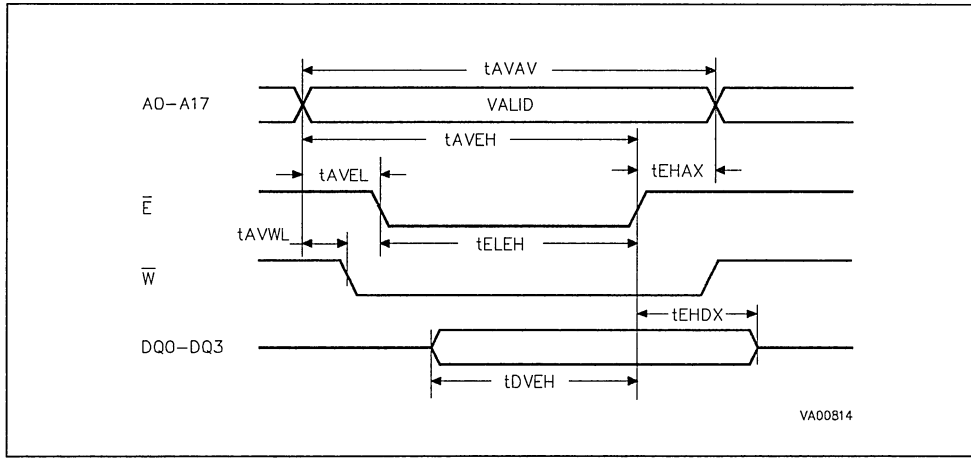
Note: 1. C_L = 5pF (see Figure 4)

Figure 8. Write Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = Low

Figure 9. Chip Enable Controlled, Write AC Waveforms



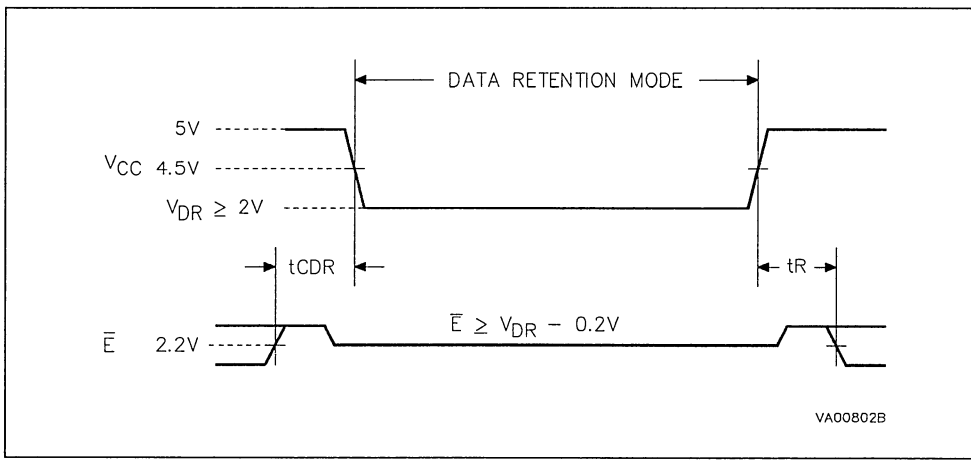
Note: $\overline{G}$ = High

Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 2V to 4.5V)

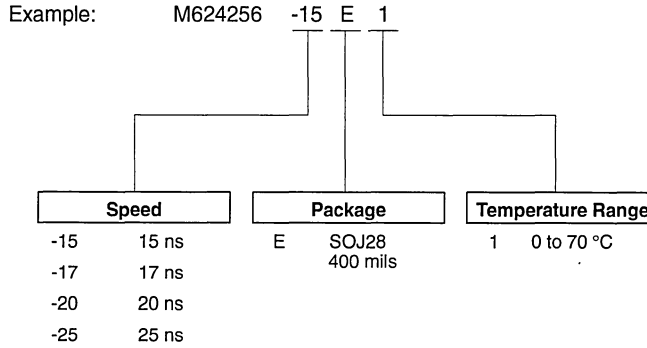
Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CCDR} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E} \geq V_{CC} - 0.2V$, f = 0		500	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E} \geq V_{CC} - 0.2V$, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E} \geq V_{CC} - 0.2V$, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

Notes: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.2V$ or $V_{IL} \leq 0.2V$
2. See Figure 8 for measurement points. Guaranteed but not tested

Figure 8. Low V_{CC} Data Retention AC Waveforms



ORDERING INFORMATION SCHEME



For a list of available options (Speed, Package etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

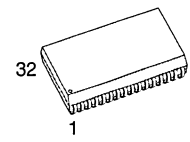
For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SGS-THOMSON MICROELECTRONICS

M628128

VERY FAST CMOS 1 Megabit (128K x 8) SRAM WITH OUTPUT ENABLE

- 128K x 8 CMOS FAST SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 15, 17, 20, 25ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ, 400 mil PACKAGE



SOJ32 (E)
400 mils

DESCRIPTION

The M628128 is a 1 Megabit (1,048,576 bit) Fast CMOS SRAM, organized as 131,072 words by 8 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Figure 1. Logic Diagram

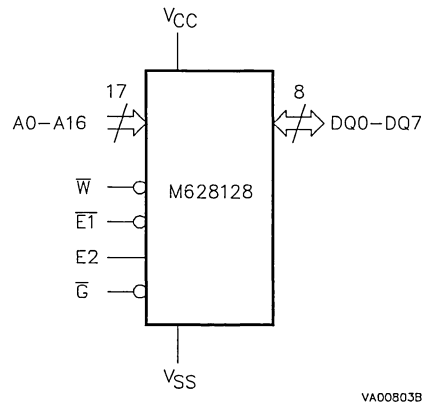


Table 1. Signal Names

A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (3)	Output Current	20	mA
P_D	Power Dissipation	1	W

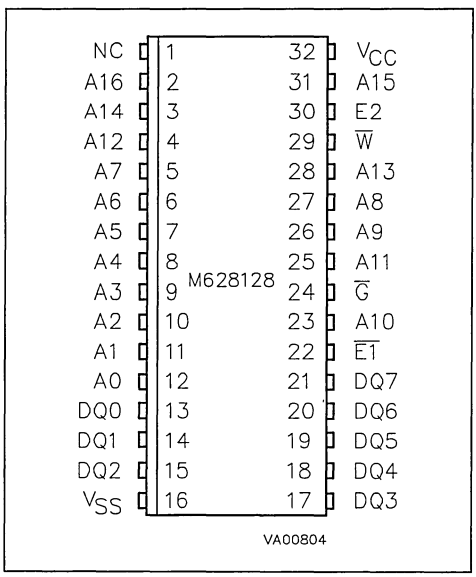
Notes: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Up to a maximum operating V_{CC} of 5.5V only
3. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0-DQ7	Power
Read	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IH}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	X	Hi-Z	Standby
Deselect	X	V_{IL}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

Figure 2. SOJ Pin Connections



Warning: NC = No Connection.

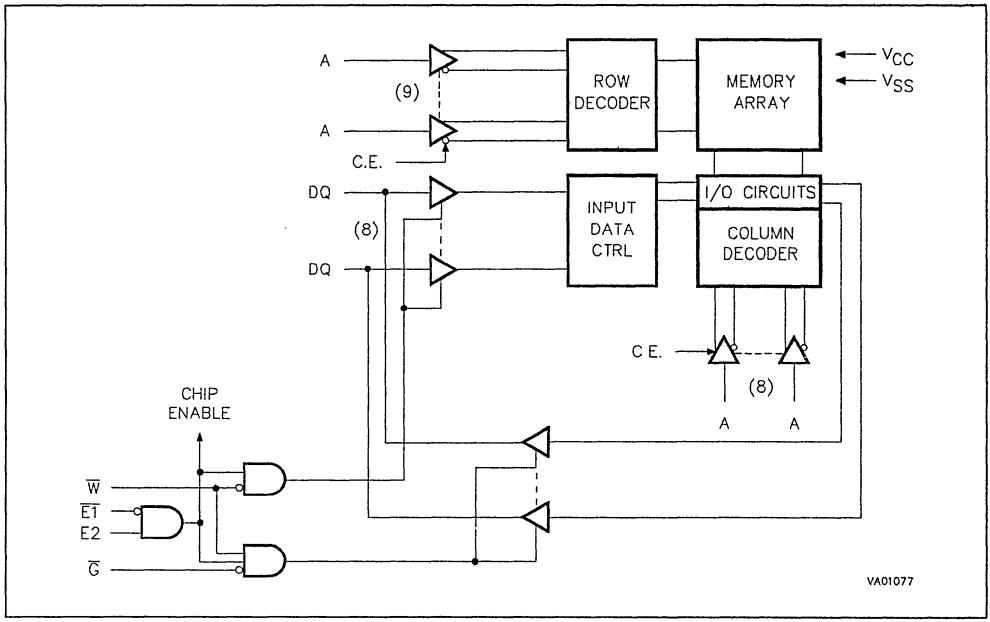
READ MODE

The M628128 is in the Read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and both Chip Enables ($\overline{E1}$ and E2) are asserted. This provides access to data from eight of the 1,048,576 locations in the static memory array, specified by the 17 address inputs. Valid data will be available at the eight output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low, $\overline{E1}$ is Low and E2 is High. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The M628128 is in the Write mode whenever the $\overline{W}$ and $\overline{E1}$ pins are Low, with E2 High. Either the Chip Enable inputs ($\overline{E1}$ and E2) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of both Chip Enables being active with $\overline{W}$ low. Therefore, address setup time is referenced to Write Enable and both Chip Enables as t_{AVWL}, t_{AVE1L} and t_{AVE2H} respectively, and is determined by the latter occurring edge.

Figure 3. Block Diagram



WRITE MODE (cont'd)

The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$, $\overline{W}$, or the falling edge of E2.

If the Output is enabled ($\overline{E1}$ = Low, E2 = High and $\overline{G}$ = Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVE1H} before the rising edge of $\overline{E1}$ or for t_{DVE2L} before the falling edge of E2, whichever occurs first, and remain valid for t_{WHDX}, t_{E1HDX} or t_{E2LDX}.

OPERATIONAL MODE

The M628128 has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E1}$ = High or E2 = Low). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{E1}$, and E2 as summarized in the Operating Modes table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

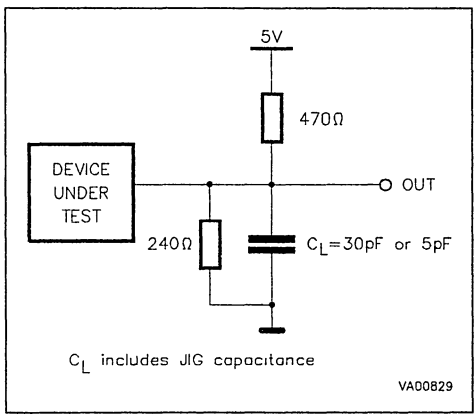


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		8	pF
C_{OUT} (2)	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC1} (1)	Supply Current	V_{CC} = 5.5V, (-15 & -17)		175	mA
		V_{CC} = 5.5V, (-20)		140	mA
		V_{CC} = 5.5V, (-25)		130	mA
I_{CC2} (2)	Supply Current (Standby) TTL	V_{CC} = 5.5V, $\overline{E1}$ = V_{IH} or E2 = V_{IL}, f = 0		25	mA
I_{CC3} (3)	Supply Current (Standby) CMOS	V_{CC} = 5.5V, $\overline{E1}$ ≥ V_{CC} – 0.2V or E2 ≤ 0.2V, f = 0		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

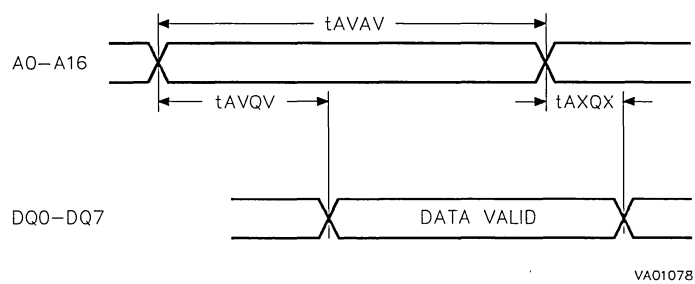
Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at V_{IL} ≤ 0.8V or V_{IH} ≥ 2.2V
3. All other Inputs at V_{IL} ≤ 0.2V or V_{IH} ≥ V_{CC} – 0.2V

Table 6. Read and Standby Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M628128								Unit
		-15		-17		-20		-25		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	15		17		20		25		ns
t_{AVQV} (1)	Address Valid to Output Valid		15		17		20		25	ns
t_{E1LQV} (1)	Chip Enable 1 Low to Output Valid		15		17		20		25	ns
t_{E2HQV} (1)	Chip Enable 2 High to Output Valid		15		17		20		25	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		7		7		8		10	ns
t_{E1LQX} (2)	Chip Enable 1 Low to Output Transition	2		2		2		2		ns
t_{E2HQX}	Chip Enable 2 High to Output Transition	2		2		2		2		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		0		0		ns
t_{E1HQZ} (2)	Chip Enable 1 High to Output Hi-Z	0	8	0	10	0	10	0	10	ns
t_{E2LQZ} (2)	Chip Enable 2 Low to Output Hi-Z	0	8	0	10	0	10	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	7	0	8	0	9	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		3		ns
t_{PU} (3)	Chip Enable 1 Low or Chip Enable 2 High to Power Up	0		0		0		0		ns
t_{PD} (3)	Chip Enable 1 High or Chip Enable 2 Low to Power Down		15		17		20		25	ns

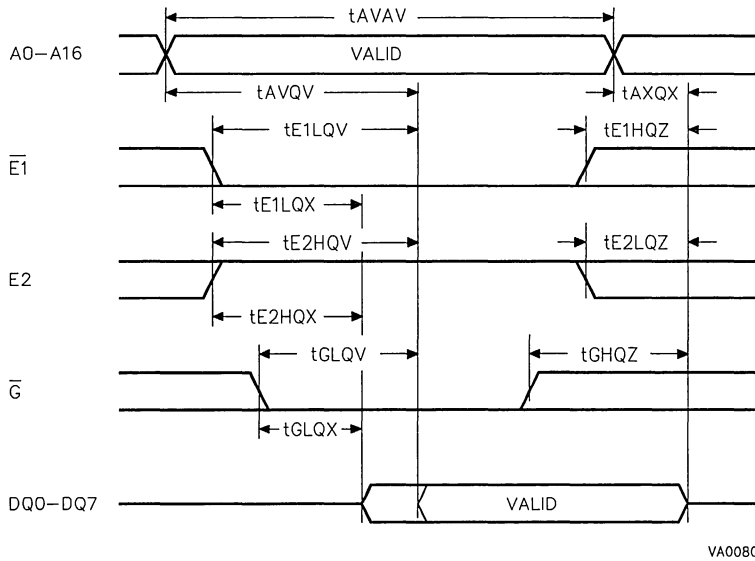
Notes: 1. C_L = 30pF (see Figure 4)
2. C_L = 5pF (see Figure 4)
3. Guaranteed but not tested (see Figure 7)

Figure 5. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E1}$ = Low, E2 = High, $\overline{G}$ = Low, $\overline{W}$ = High

Figure 6. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High

Figure 7. Standby Mode AC Waveforms

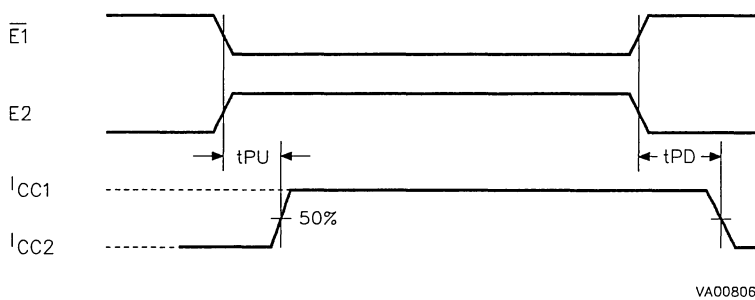
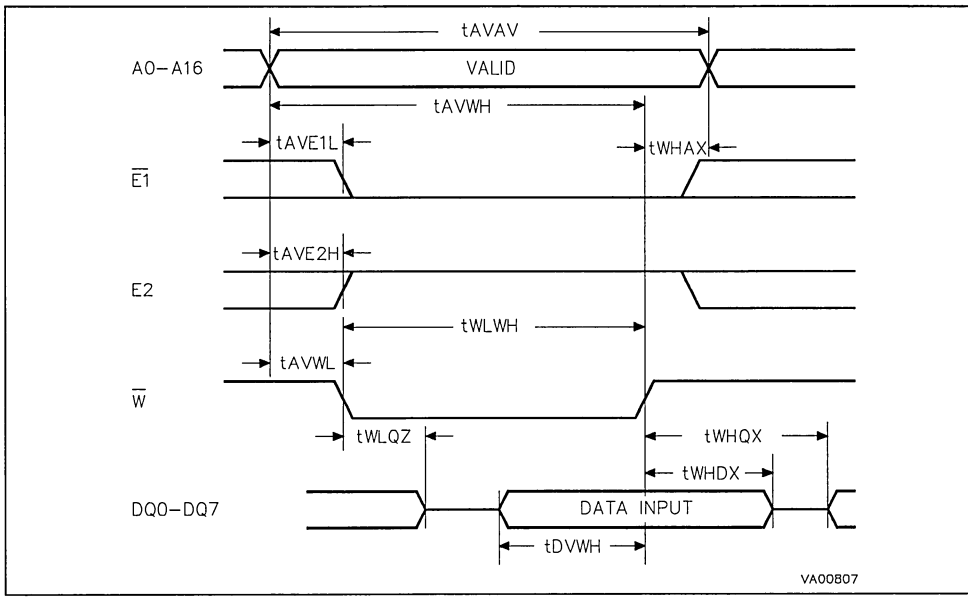


Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M628128								Unit
		-15		-17		-20		-25		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	15		17		20		25		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	10		12		12		15		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	11		12		12		15		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	11		12		12		15		ns
t_{WLWH}	Write Enable Pulse Width	10		12		12		15		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	0	12	ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		0		0		0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		0		0		0		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	11		12		12		15		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	11		12		12		15		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	0		0		0		0		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	0		0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	8		10		12		12		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	8		10		12		12		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	8		10		12		12		ns

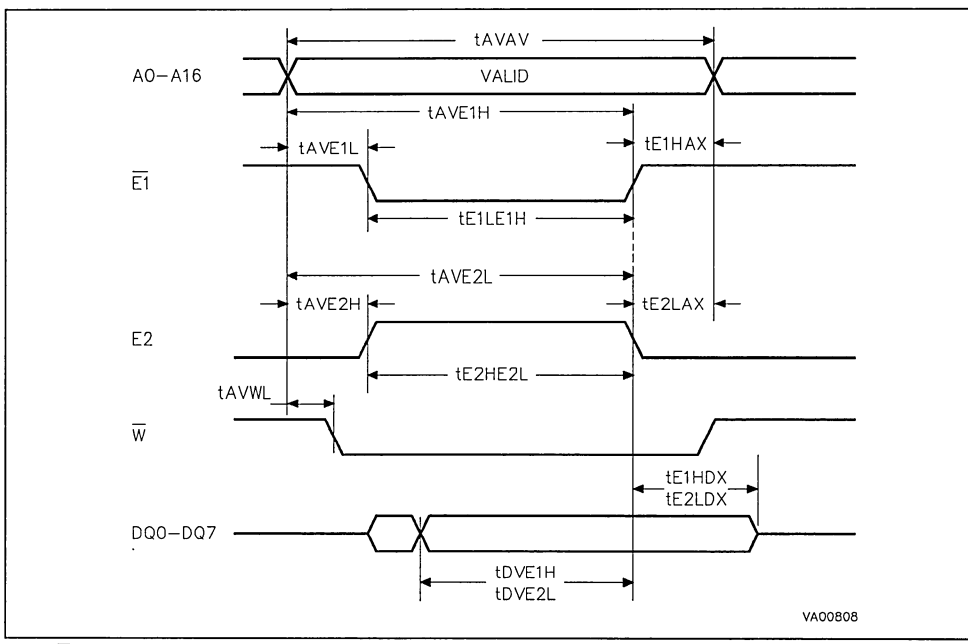
Note: 1. C_L = 5pF (see Figure 4)

Figure 8. Write Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = Low

Figure 9. Chip Enable Controlled, Write AC Waveforms



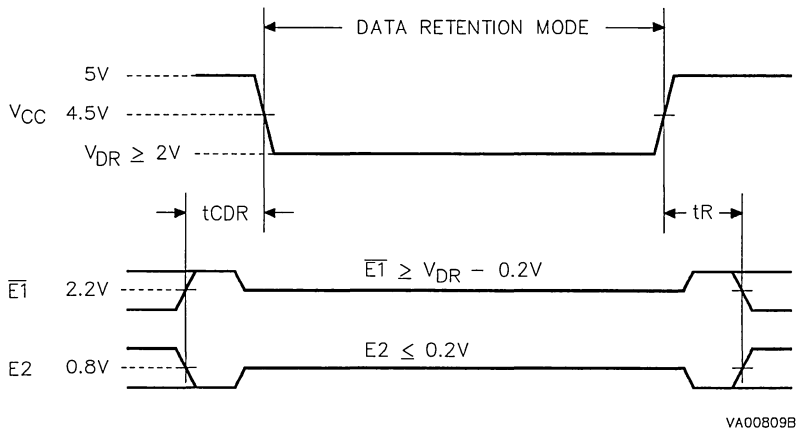
Note: $\overline{G}$ = High

Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 2V to 4.5V)

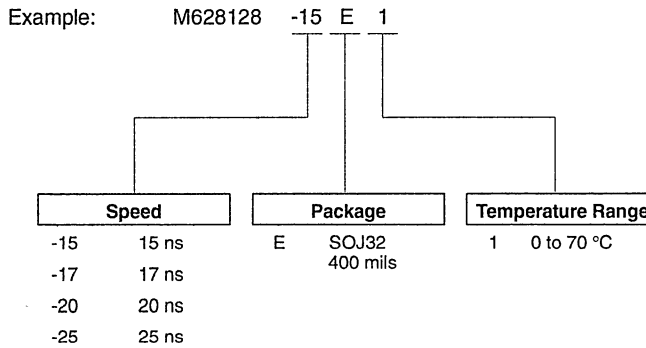
Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CCDR} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E1} \geq V_{CC} - 0.2V$, $E2 \leq 0.2V$, f = 0		500	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E1} \geq V_{CC} - 0.2V$, $E2 \leq 0.2V$, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E1} \geq V_{CC} - 0.2V$, $E2 \leq 0.2V$, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

Notes: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.2V$ or $V_{IL} \leq 0.2V$
2. See Figure 10 for measurement points. Guaranteed but not tested

Figure 10. Low V_{CC} Data Retention AC Waveforms



ORDERING INFORMATION SCHEME



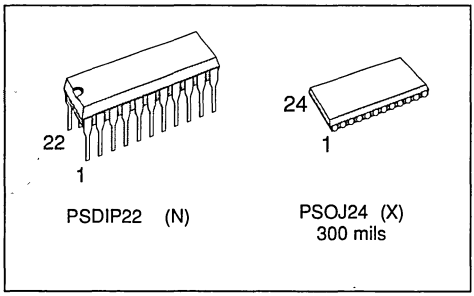
For a list of available options (Speed, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CACHE MEMORIES

VERY FAST CMOS 4K x 4 CACHE TAGRAM

- 4K x 4 FAST HCMOS CACHE TAGRAM
- ADDRESS TO COMPARE ACCESS TIMES: 10,12,15,20,25ns
- FLASH CLEAR FUNCTION
- 22-PIN 300 MIL PLASTIC DIP 24-PIN 300 MIL SOJ
- APPLICATIONS: HIGH SPEED 32-BIT CACHE SUB-SYSTEMS



PSDIP22 (N)

PSOJ24 (X)
300 mils

DESCRIPTION

The MK41S80 is a 16,384-bit CMOS Static TAGRAM™, organized as 4K x 4 using SGS-THOMSON Microelectronics' advanced fast HCMOS process technology. This device is functionally compatible with the industry standard MK41H80 4K x 4 TAGRAM. All inputs and outputs are TTL compatible using a single 5V supply.

The MK41S80 provides full static operation, requiring no external clocks or refresh operations, and features a MATCH output for indicating either a cache hit or miss condition. The on-board 4-bit comparator compares RAM contents with current input (tag) data. The result is an active high level on the MATCH pin for a hit, or an active low on the MATCH pin indicating a miss. The MK41S80 offers a totem-pole MATCH output design.

The MK41S80 incorporates a Flash Clear Cycle which begins as $\overline{CLR}$ is brought active low. A Flash Clear sets all 16,384 bits in the RAM to logic zero.

Pin Names

A0-A11	Address Inputs
DQ0-DQ3	Data Inputs / Outputs
MATCH	Comparator Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{CLR}$	RAM Flash Clear
V_{CC}, GND	+5 Volts, Ground
NC	Not Connected

Figure 1. Pin Connections

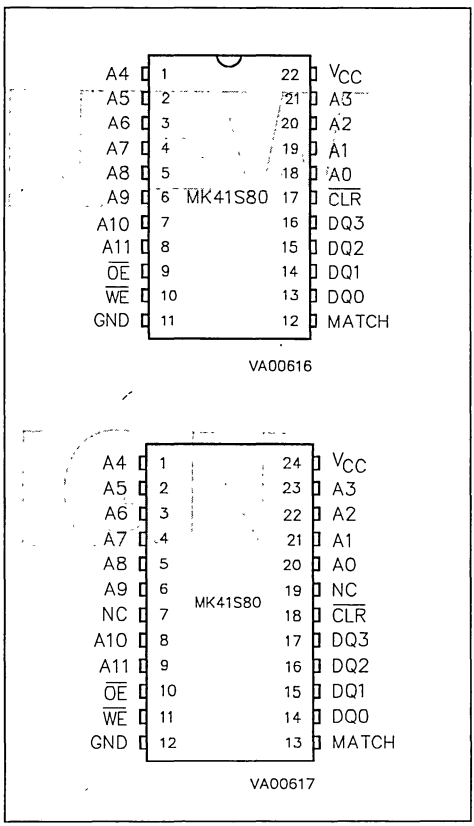
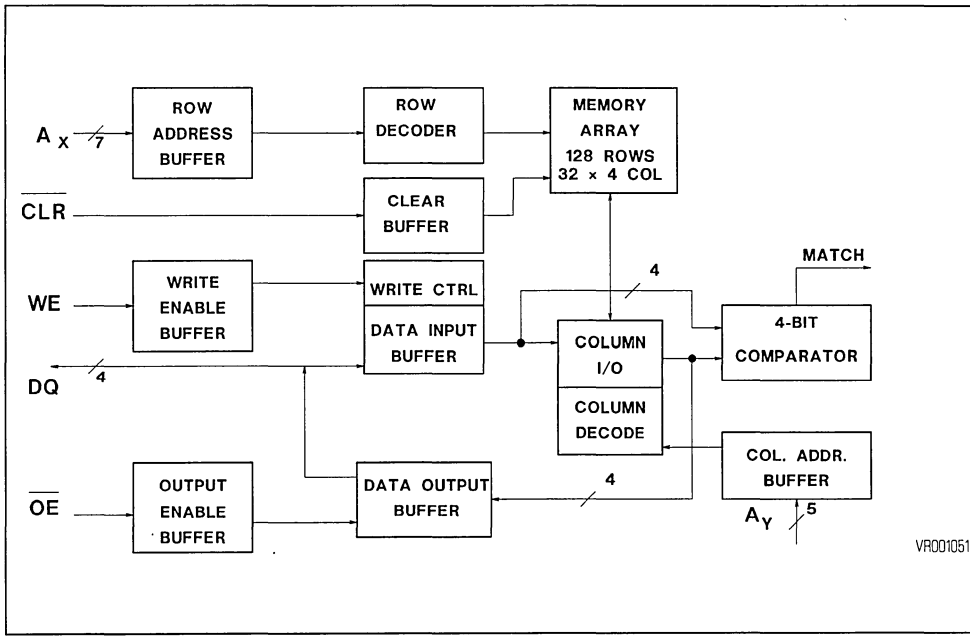


Figure 2. MK41S80 Block Diagram



TAGRAM FUNCTION

The MK41S80 is an SRAM based Cache Tag directory (hence the name TAGRAM). Figure 7 shows a general block diagram using a cache tag directory (TAGRAM) in a cache subsystem application. The system must detect whether the requested data resides in the cache data RAM, or if extended read cycles to main memory are necessary.

The MK41S80 features four modes of operation: Write, Read, Compare, and Clear. The MK41S80 incorporates an on-board 4 bit comparator that compares internal RAM contents with current (tag) input data. If the device is in the compare mode, and the comparator detects a "match", then the MATCH pin will go high for a hit condition. If a match is not detected by the comparator, then the MATCH pin drives low to denote a "miss" condition. Standard write/read operations are performed with Write ($\overline{WE}$) and Output ($\overline{OE}$) Enable inputs. Additionally, the device provides a Flash Clear operation via the $\overline{CLR}$ pin (Figure 6). When a low level (V_{IL}) is applied to the $\overline{CLR}$ input pin for the specified t_{CLP} time, all RAM bits are set to a logic zero.

Compare data (internal RAM) can be read from the data pins by bringing Output Enable ($\overline{OE}$) low. This will allow data stored in the memory array to be displayed at the Outputs (DQ0 - DQ3).

MK41S80 TRUTH TABLE

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	Match	Mode
H	H	H	Valid	Compare
L	X	H	Invalid	Write
H	L	H	Invalid	Read
X	X	L	Invalid	RAM Clear

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	– 0.5 to 6	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	– 65 to 150	°C
P_D	Power Dissipation	1	W
I_O(2)	Output Current	50	mA

Notes :

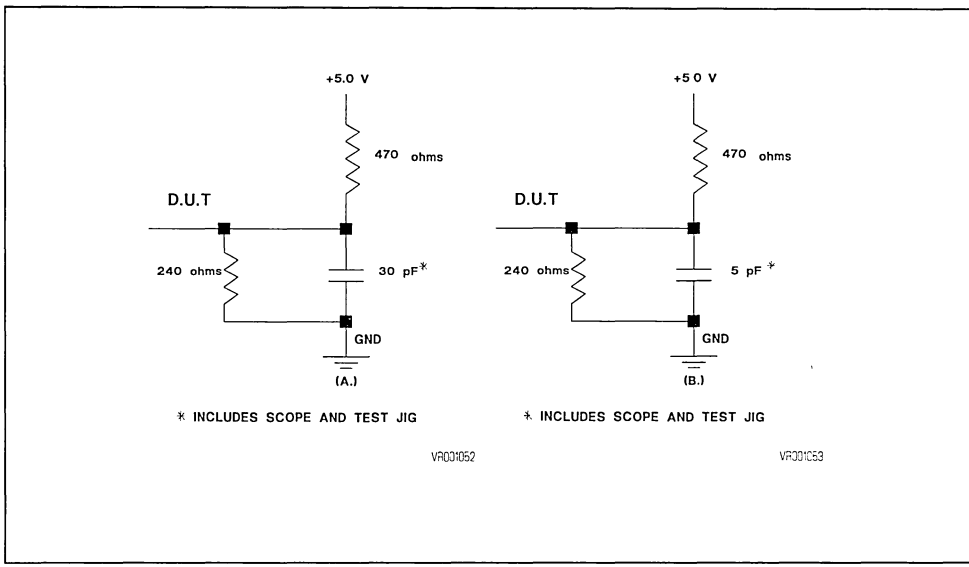
1. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliare-liability.
2. Output current absolute maximum rating is specified for one output at a time, not to exceed a duration of 1 second.

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels(1)	0 to 3	V
Transition Time	1.5	ns
Input and Output Signal Timing Reference Level	1.5	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ± 5 %	V

Note: 1. AC input levels for the $\overline{CLR}$ pin are GND to 3.5 V.

Figure 3. Equivalent Output Load Circuits



COMPARE, WRITE, AND READ TIMING

The MK41S80 TAGRAM begins a Compare Cycle with the application of a valid address (see Figure 4). A valid compare is enabled when $\overline{OE}$ and $\overline{WE}$ go high in conjunction with their respective set-up and hold times. MATCH will occur t_{ACA} after a valid address, and t_{DCA} after valid Data In (Tag). If the address and tag data are presented simultaneously, the compare-to-match access is t_{ACA}. MATCH will go invalid t_{ACH} after an address change, or t_{DCH} after the tag data changes.

A Write Cycle starts with stable addresses (Figures 4 and 5), with the $\overline{WE}$ input active low. $\overline{OE}$ may be in either logic state. $\overline{WE}$ may fall with stable addresses, and must remain low until t_{AW} with a duration of t_{WEW}. Data in must be valid t_{DS} before and t_{DH} after $\overline{WE}$ goes high. DQ will go high-Z at t_{WEZ} from $\overline{WE}$ going active low. MATCH will be invalid during this cycle.

The device begins a Read Cycle with stable addresses and $\overline{WE}$ high (Figure 5). DQ becomes valid t_{AA} after a valid address, and t_{OEA} after the fall of $\overline{OE}$. The DQ outputs become invalid t_{OH} after addresses become invalid, and become high-Z at t_{OEZ} when $\overline{OE}$ goes high. Ripple through data access may be accomplished by holding $\overline{OE}$ active low while strobing address A0-A11, and holding $\overline{CLR}$ and $\overline{WE}$ high. The MATCH output will be invalid during this cycle.

FLASH CLEAR CYCLE

The MK41S80 incorporates a Flash Clear Cycle which begins as $\overline{CLR}$ is brought active low. A Flash Clear sets all 16,384 bits in the RAM to logic zero. Control inputs will not be recognized from t_{CX} after $\overline{CLR}$ goes low, until t_{CR} after $\overline{CLR}$ is brought high. The $\overline{OE}$ and $\overline{WE}$ inputs are Don't Care, and DQ is High-Z. MATCH will be invalid during a Flash Clear Cycle.

APPLICATION

The MK41S80 operates from a single 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Also, because the outputs can drive rail-to-rail into high impedance loads, the device can interface to 5 volt CMOS on its inputs and outputs.

The MK41S80 compares contents of addressed RAM locations to the current tag data inputs. A logic one "1" output on the MATCH pin indicates that the input data and the RAM contents match. Conversely, a logic zero "0" on the MATCH pin

Figure 4. Compare and Write Cycle

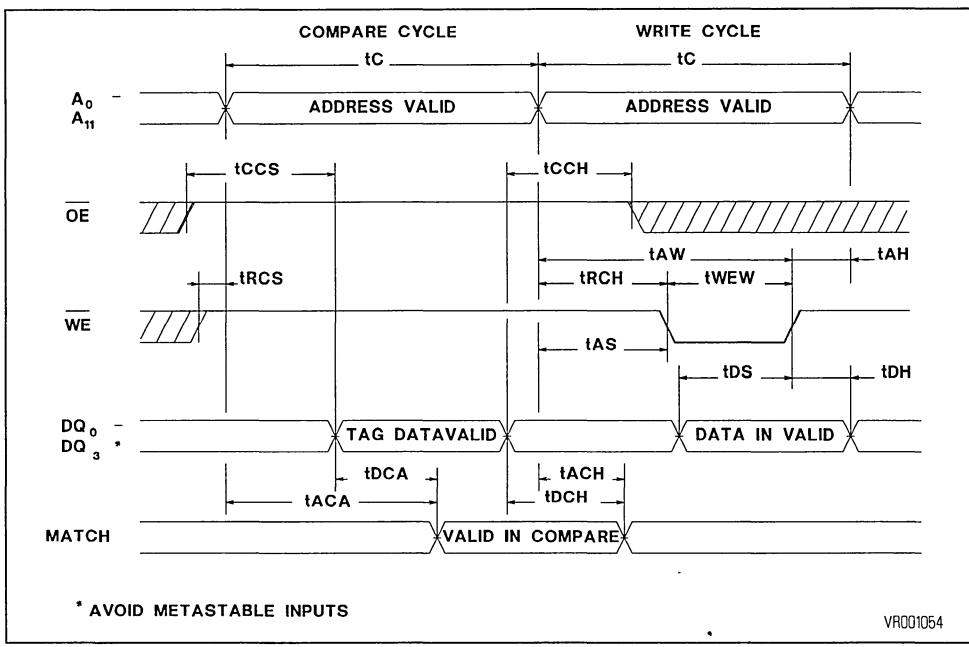


Figure 5. Write and Read Cycle

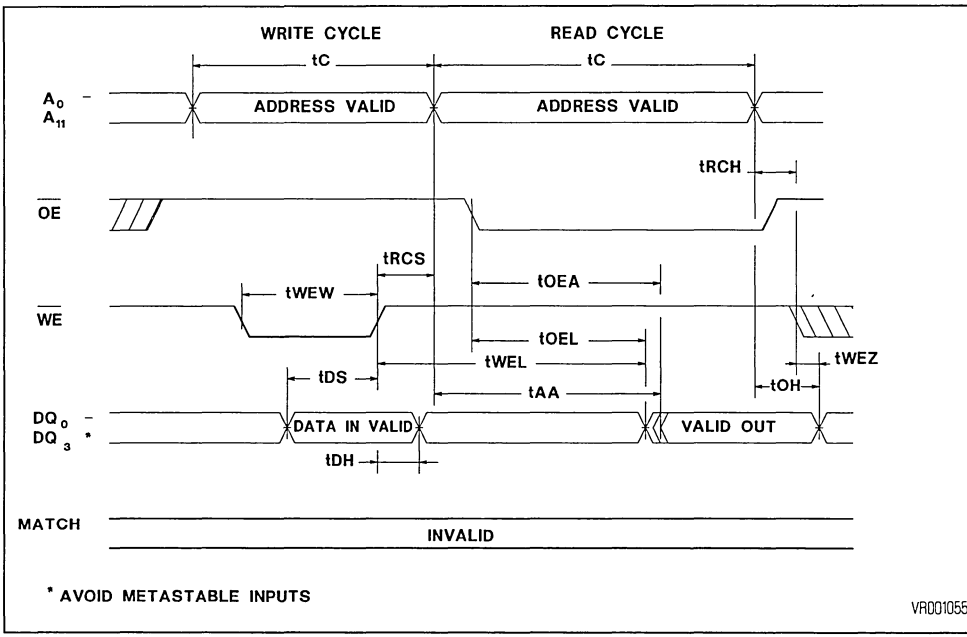
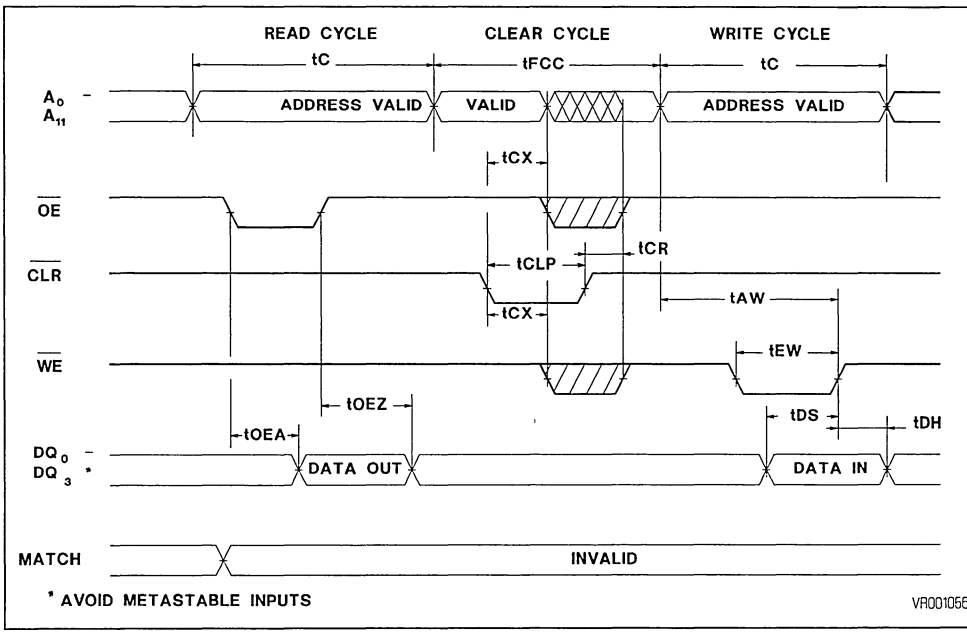


Figure 6. Read-Flash Clear-Write Cycle

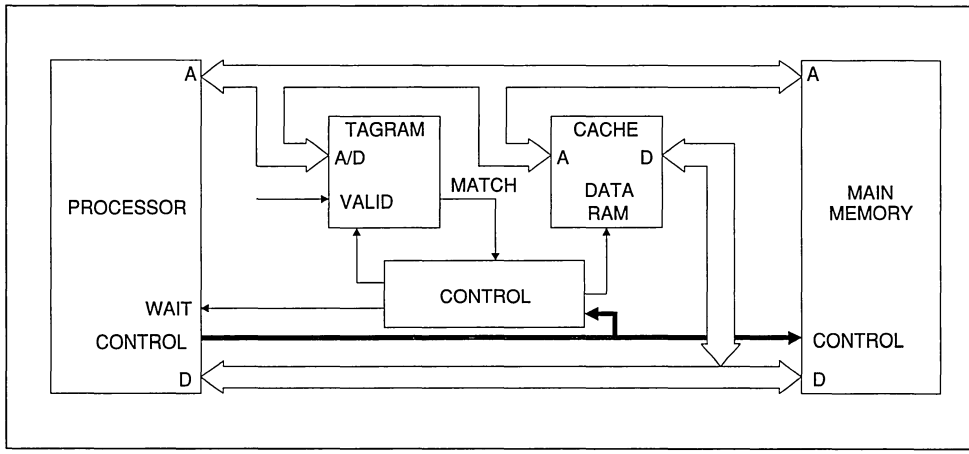


indicates at least one bit of difference between the RAM contents and input data.

Metastable inputs can result in excessive MATCH output activity. Therefore, the use of pull-up or pull-down resistors is recommended on the data bus. Additionally, a pull-up resistor is suggested for the $\overline{CLR}$ input to enhance system operation. This will ensure that any low going system noise coupled onto the input does not drive $\overline{CLR}$ below V_{IH} minimum specifications.

Because high frequency current transients will be associated with the operation of the MK41S80, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding, or separate power planes can be employed to reduce line inductance. Additionally, any low impedance transmission lines are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination is suggested in close proximity to the drivers to improve driver/signal path impedance matching.

Figure 7. General Cache Subsystem Block Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATION

($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	-10		-12		-15		-20		-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_C	Cycle Time	15		15		20		20		25		ns	
t_{CCS}	Compare Command Set-Up Time	4		5		6		7		8		ns	
t_{CCH}	Compare Command Hold Time	0		0		0		0		0		ns	
t_{RCS}	Read Command ($\overline{WE}$) Set-Up Time	0		0		0		0		0		ns	
t_{RCH}	Read Command ($\overline{WE}$) Hold Time	0		0		0		0		0		ns	
t_{AS}	Address Set-Up Time	0		0		0		0		0		ns	
t_{AW}	Address to End of Write ($\overline{WE}$)	10		10		12		16		20		ns	
t_{AH}	Address Hold after End of Write	1		1		1		1		1		ns	
t_{WEW}	Write Command ($\overline{WE}$) Pulse Width	10		11		12		16		20		ns	
t_{DS}	Data Set-Up Time	10		12		12		12		13		ns	
t_{DH}	Data Hold Time	0		0		0		0		0		ns	
t_{DCA}	Data (Tag) Compare Access Time		7		8		10		12		15	ns	3
t_{ACA}	Address Compare (Match) Access Time		10		12		15		20		25	ns	3
t_{ACH}	Address Compare Hold Time	2		2		2		2		2		ns	3
t_{DCH}	Data Compare Hold Time	0		0		0		0		0		ns	3
t_{OEA}	Output Enable ($\overline{OE}$) Access Time		8		8		10		10		12	ns	3
t_{OH}	Output (Q) Hold Time	2		2		2		2		2		ns	3
t_{AA}	Address to Valid Data Out Access Time		12		15		20		20		25	ns	3
t_{OEZ}	Output Enable ($\overline{OE}$) High to Q High-Z		7		7		7		7		7	ns	4
t_{OEL}	Output Enable ($\overline{OE}$) Low to Q Active	0		0		0		0		0		ns	4
t_{WEZ}	Write Enable ($\overline{WE}$) High to Q High-Z		7		7		7		7		7	ns	4
t_{WEL}	Write Enable ($\overline{WE}$) High to Q Active	1		1		1		1		1		ns	4
t_{FCC}	Flash Clear Cycle Time	50		50		50		50		50		ns	
t_{CX}	Clear ($\overline{CLR}$) to Inputs Don't Care	0		0		0		0		0		ns	
t_{CR}	End of Clear to Inputs Recognized	0		0		0		0		0		ns	
t_{CLP}	Flash Clear Pulse Width	35		35		35		35		35		ns	

RECOMMENDED DC OPERATING CONDITIONS
($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{CC}	Supply Voltage	4.75	5	5.25	V	1
GND	Ground	0	0	0	V	1
V_{IH}	Logic 1 All Inputs	2.2	3	V_{CC} + 0.3	V	1
V_{IL}	Logic 0 All Inputs	0.3	0.2	0.8	V	1

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average V_{CC} Power Supply Current (Both Ports)		120	mA	5
I_{LI}	Input Leakage Current (Any Input)	– 1	1	µA	2
I_{LO}	Output Leakage Current	– 10	10	µA	2
V_{OH}	Output Logic 1 Voltage (I_{OH} = -4.0mA)	2.4		V	1
V_{OL}	Output Logic 0 Voltage (I_{OL} = 8mA)		0.4	V	1

CAPACITANCE
($T_A = 25°C$, f = 1.0 MHz)

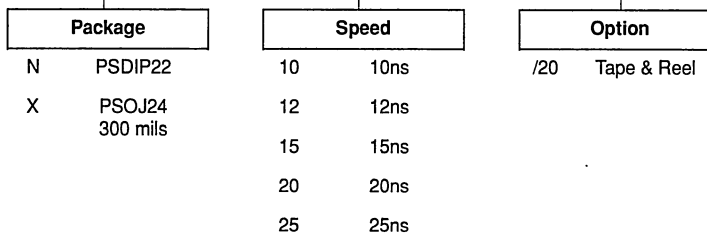
Symbol	Parameter	Typ.	Max.	Unit	Notes
C_I	Input Capacitance on all pins (except DQ)	4	6	pF	7
C_O	Output Capacitance	8	10	pF	6, 7

Notes :

1. All voltages referenced to GND.
2. Measured with GND ≤ V ≤ V_{CC}. Outputs are deselected with the exception to MATCH which is always enabled.
3. Measured with load as shown in Figure 3A.
4. Measured with load as shown in Figure 3B.
5. I_{CC1} measured with outputs open, $V_{CC\ max}$, f = min cycle.
6. Output buffer is deselected.
7. Capacitances are sampled and not 100% tested.

ORDERING INFORMATION

Example: MK41S80 X 10 /20

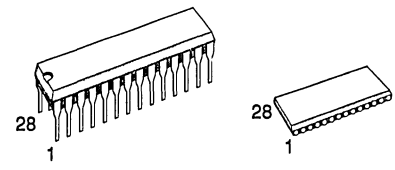


For a list of available options of Package and Speed, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

VERY FAST CMOS 8K x 8 CACHE TAGRAM

- 8K x 8 CMOS SRAM WITH ONBOARD COMPARATOR
- ADDRESS TO COMPARE ACCESS TIME: 20, 25, 35ns
- FAST CHIP SELECT COMPARE ACCESS 10ns
- MATCH OUTPUT WITH FAST TAG DATA TO COMPARE ACCESS OF 12ns Max
- STATIC OPERATION - NO CLOCKS OR TIMING STROBES REQUIRED
- ALL INPUTS AND OUTPUTS ARE FULLY TTL COMPATIBLE
- FULL CMOS FOR LOW POWER OPERATION
- OPEN DRAIN MATCH OUTPUT
- 28 PIN 300 MIL DIP & 28 PIN 300 MIL SOJ



PSDIP28 (N)

PSOJ28 (X)
300 mils

TRUTH TABLE

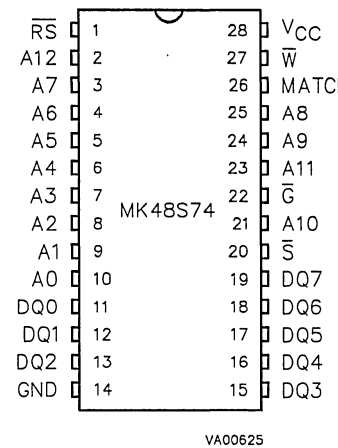
$\overline{W}$	$\overline{S}$	$\overline{G}$	$\overline{RS}$	Mode	DQ	Match
X	X	X	L	Reset Clear	High-Z	Invalid
X	H	X	H	Deselect	High-Z	Invalid
H	L	H	H	Miss	D_{IN}	Low
H	L	H	H	Match	D_{IN}	High-Z
H	L	L	H	Read	Q_{OUT}	Invalid
L	L	X	H	Write	D_{IN}	Invalid

Note: MATCH is High-Z during an invalid state

PIN NAMES

A0 - A12	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
MATCH	Comparator Output
$\overline{S}$	Chip Select
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RS}$	Rest Flash Clear
V_{CC}, GND	5 Volts, Ground

Figure 1. Pin Connection



DESCRIPTION

The MK48S74 is a 65, 536 fast static cache TAGRAM™ organized as 8K x 8 bits. It is fabricated using SGS-THOMSON's low power, high performance HCMOS4 technology. The MK48S74 features fully static operation requiring no external clocks or timing strobes, and equal access and cycle times. The device requires a single 5V ± 5 % supply and is fully TTL compatible. The MK48S74 has a fast Chip Select control for high speed oper-ation to the Match Compare valid, and device se-lect/deselect operations. Additionally, the MK48S74 provides a Reset Clear, and MATCH compare pin. The Reset Clear input provides an asynchronous RAM clear control which clears all internal RAM bits to zero in only two cycles. The MATCH output features an open drain for wired-OR operations. During a MATCH compare cycle, an on-board 8-bit comparator compares the Data Inputs (8-bit TAG) at the specified address index (A0-A12) to the internal RAM data. If a miss condition exists, where at least one bit of TAG data does not match the internal RAM, then the MATCH output issues a LOW miss signal.

OPERATIONS

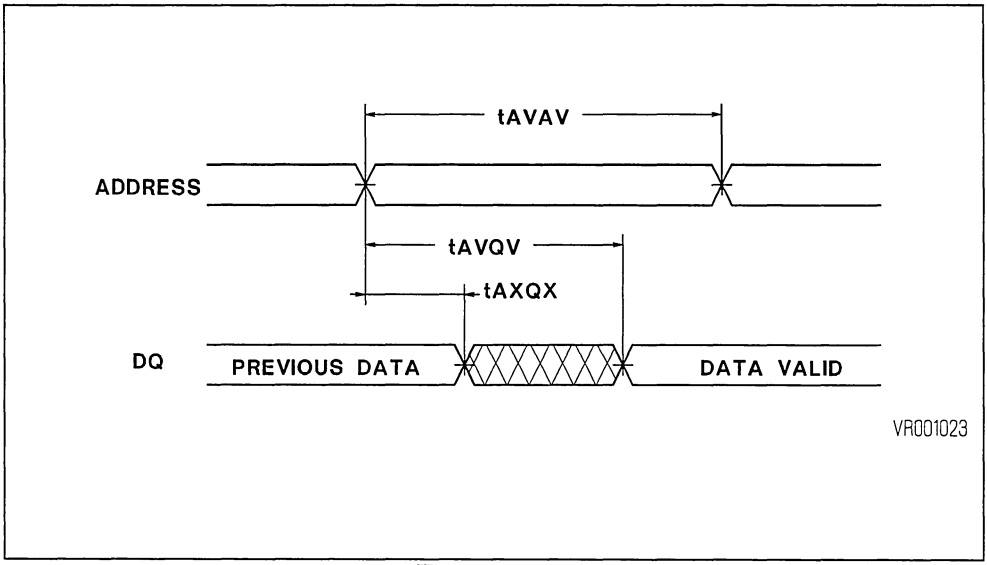
READ MODE

The MK48S74 is in the read mode whenever Write Enable ($\overline{W}$) is HIGH with Output Enable ($\overline{G}$) LOW and Chip Select ($\overline{S}$) is active. This provides access to data from eight of 65, 536 locations in the static memory array. The unique address specified by the 13 address inputs defines which one of the 8192-8-bit bytes is to be accessed. Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is LOW and $\overline{S}$ is LOW. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{SLQV} or t_{GLQV} rather than the addresses. The state of the DQ pins is controlled by the $\overline{S}$, $\overline{G}$ and $\overline{W}$ control signals. Data out may be inderterminate at t_{SLQX} and t_{GLQX} but data lines will always be valid at t_{AVQV}.

READ CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

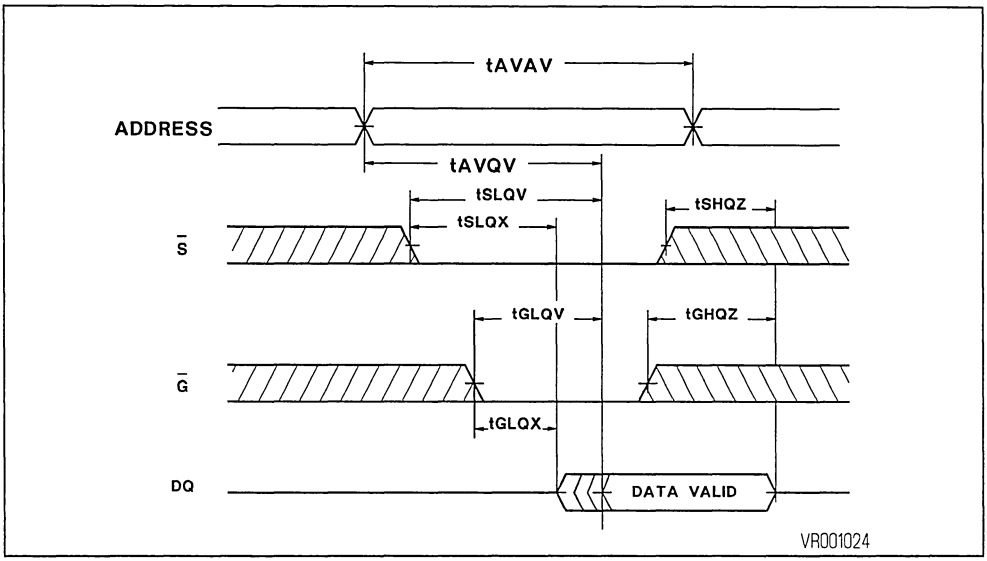
Symbol		Parameter	-20		-25		-35		Unit	Notes
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AVQV}	t_{AA}	Address Access Time		20		25		35	ns	1
t_{SLQV}	t_{CSA}	Chip Select Access Time		15		15		20	ns	
t_{GLQV}	t_{OEA}	Output Enable Access Time		15		15		20	ns	1
t_{SLQX}	t_{CSL}	Chip Select to Output Low-Z	0		0		0		ns	
t_{GLQX}	t_{OEL}	Output Enable to Low-Z	0		0		0		ns	
t_{SHQZ}	t_{CSZ}	Chip Select to High-Z		9		9		9	ns	
t_{GHQZ}	t_{OEZ}	Output Enable to High-Z		8		8		8	ns	2
t_{AXQX}	t_{OH}	Output Hold From Address Change	3		3		3		ns	1

Figure 2. Read Timing No. 1 (Address Access)



Note: Chip Select and Output Enable one presumed valid, $\overline{W} = V_{IH}$

Figure 3. Read Timing No. 2 ($W = V_{IH}$)



WRITE MODE

The MK48S74 is the Write mode whenever the $\overline{W}$ and $\overline{S}$ pins are LOW. Chip Select or $\overline{W}$ must be inactive during address transitions. The Write begins with the concurrence of Chip Select being active with $\overline{W}$ LOW. Therefore address setup times are referenced to Write Enable and Chip Select as t_{AVWL} and t_{AVSL} and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{S}$ or $\overline{W}$. If the outputs are enabled ($\overline{S}$ = LOW, $\overline{G}$ = LOW), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{S}$, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{S}$ or $\overline{W}$.

WRITE CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol		Parameter	-20		-25		-35		Unit	Notes
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AVWL}	t_{AS}	Address Set-up to Write Enable Low	0		0		0		ns	
t_{AVSL}	t_{AS}	Address Set-up to Chip Select	0		0		0		ns	
t_{AVWH}	t_{AW}	Address Valid to End of Write	15		20		25		ns	
t_{WLWH}	t_{WEW}	Write Pulse Width	15		20		25		ns	
t_{WHAX}	t_{AH}	Address Hold Time After End of Write	0		0		0		ns	
t_{SLSH}	t_{CSW}	Chip Select to End of Write	15		20		25		ns	
t_{SHAX}	t_{WR}	Write Recovery Time To Chip Select	0		0		0		ns	
t_{DVWH}	t_{DW}	Data Valid to End of Write	10		13		15		ns	
t_{WHDX}	t_{DH}	Data Hold Time	0		0		0		ns	
t_{WHQX}	t_{WEL}	Write High to Output Low-Z (Active)	0		0		0		ns	2
t_{WLQZ}	t_{WEZ}	Write Enable to Output High-Z		5		5		5	ns	2

Figure 4. Writing Timing No.1 (Write Control)

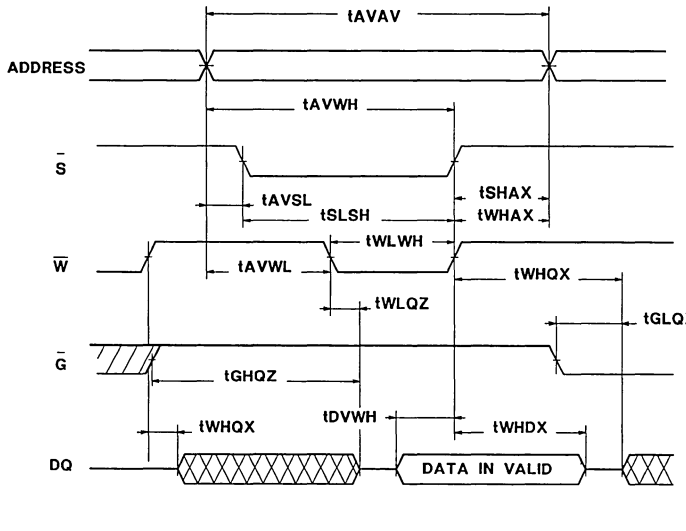
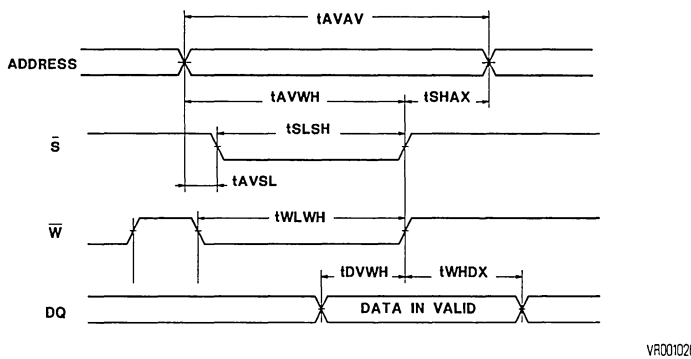


Figure 5. Writing Timing No. 2 (Chip Select Control)



Note: $\overline{G} = V_{IH}$

COMPARE MODE

THe MK48S74 is in the Compare mode whevenver $\overline{W}$ and $\overline{G}$ are HIGH provided Chip Select ($\overline{S}$) is active LOW. The 13 index address inputs (A0-A12) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ_0-DQ_7) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal, then a hit condition occurs (MATCH = High-Z). When at least one bit is not equal, the MATCH will go LOW signifying a miss condition. The MATCH output will be valid t_{AVMV} from stable address, or t_{TVMV} from valid Tag Data when $\overline{S}$ is LOW. Should the address be stable with valid Tag Data, and the device is deselected ($\overline{S}$ = HIGH), then MATCH will be valid t_{SLMV} from the falling edge of Chip Select ($\overline{S}$). When executing a write-to-compare cycle ($\overline{W}$ = LOW, $\overline{G}$ = LOW or HIGH), MATCH will be valid t_{WHMV} or t_{GHMV} from the latter rising edge of $\overline{W}$ or $\overline{G}$ respectively.

RESET MODE

The MK48S74 allows an asynchronous reset clear whevever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits (65, 536 bits) to a logic zero as long as $t_{RSL-RSH}$ is satisfied. The MATCH output will go HIGH-Z t_{RSL-MH} from the falling edge of $\overline{RS}$ and all inputs will not be recongnized until t_{RSH-AV} from the rising edge of reset ($\overline{RS}$).

COMPARE CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions

($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

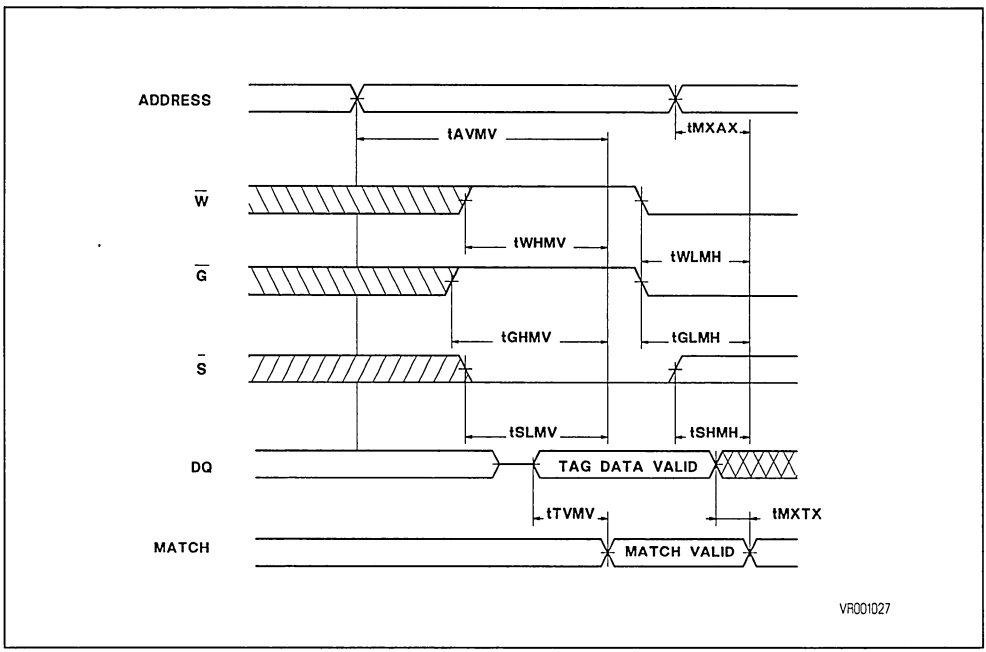
Symbol		Parameter	-20		-25		-35		Unit	Notes
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVMV}	t_{AMA}	Address to MATCH Valid		20		25		35	ns	3
t_{SLMV}	t_{CSM}	Chip Select to MATCH Valid		10		15		15	ns	3
t_{SHMH}	t_{CSMH}	Chip Deselect to MATCH High-Z		8		12		12	ns	3
t_{TVMV}	t_{DMA}	Tag Data to MATCH Valid		12		15		15	ns	3
t_{GHMV}	t_{OEM}	$\overline{G}$ High to MATCH Valid		10		15		15	ns	3
t_{GLMH}	t_{OEMH}	$\overline{G}$ Low to MATCH High-Z		10		12		12	ns	3
t_{WHMV}	t_{WEM}	$\overline{W}$ High to MATCH Valid		10		20		20	ns	3
t_{WLMH}	t_{WEMH}	$\overline{W}$ Low to MATCH High-Z		10		15		15	ns	3
t_{MXAX}	t_{MHA}	MATCH Hold From Address	2		2		2		ns	3
t_{MXTX}	t_{MHD}	MATCH Hold From Tag Data	0		0		0		ns	3

RESET CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions

($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol		Parameter	-20		-25		-35		Unit	Notes
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	t_{RC}	Flash Clear Cycle Time	80		80		100		ns	
t_{RSL-AX}	t_{RSX}	Reset Clear ($\overline{RS}$) to Inputs Don't Care	0		0		0		ns	
t_{RSH-AV}	t_{RSV}	$\overline{RS}$ to Inputs Valid	5		5		5		ns	
$t_{RSL-RSH}$	t_{RSP}	Reset ($\overline{RS}$) Pulse Width	75		75		95		ns	
t_{RSL-MH}	t_{RSM}	Reset ($\overline{RS}$) to MATCH High-Z		15		15		15	ns	

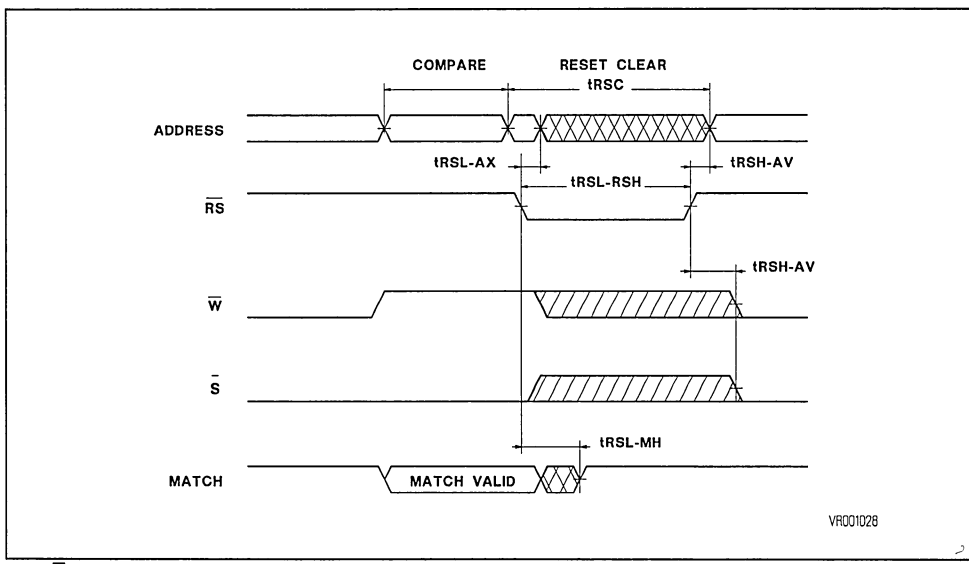
Figure 6. Match Compare Timing



APPLICATION

The MK48S74 operates from a 5V supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaces with it, particularly TTL devices. A pull-up resistor is also recommended for the $\overline{RS}$ input. This will ensure that any low going system noise, coupled onto the input does not drive $\overline{RS}$ below V_{IH} minimum specifications. This will enhance proper device operation, and avoid possible partial flash clear cycles. Additionally because the outputs can drive rail-to-rail into high impedance loads, the MK48S74 can also interface to 5V CMOS on all inputs and outputs. The MK48S74 provides the system designer with 64K fast static memory, a MATCH output, and a BYTEWIDE on-board comparator — all in one chip. The MK48S74 compares contents of addressed RAM locations to the current data inputs. A High-Z output on the MATCH Pin indicates that the input data and the RAM data match. Conversely, a logic zero "0" on the MATCH pin indicates at least one bit of difference between the RAM contents and the input TAG, generating in a miss. The MATCH output is constructed with an open drain arrangement. The open drain provides easy wired-OR implementation when generating a composite MATCH signal. In a cache subsystem, the MATCH signal provides the processor or CPU with the necessary information concerning wait state conditions. The purpose of a cache subsystem is to maintain a duplicate copy of portions of the main memory. When a valid match occurs, the system processor uses data from the fast cache memory, and avoids longer cycles to the main memory. Therefore, implementing cache subsystems with the MK48S74, and providing good hit or match ratio designs will enhance overall system performance. Because high frequency current transients will be associated with the operation of the MK48S74, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or seprarate power planes can be employed to reduce line inductance. Though often times not thought of as such, the traces of a memory board are basically unterminated, low impedance trasmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentaiton most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

Figure 7. Reset Timing



Note: $\overline{G}$ = High

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	– 0.3 to 6	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	– 65 to +150	°C
P_D	Power Dissipation	1	W
I_{OUT}	Output Current	50	mA

Note: This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage	4.75	5.25	V	4
GND	Ground	0	0	V	4
V_{IH}	Logic 1 All Inputs	2.2	V_{CC} + 0.3	V	4
V_{IL}	Logic 0 All Inputs	– 0.3	0.8	V	4

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current		160	mA	5
I_{IL}	Input Leakage Current	– 1	1	µA	6
I_{OL}	Output Leakage Current	– 5	5	µA	7
V_{OH}	Logic 1 Output Voltage (I_{OUT} = –4 mA)	2.4		V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8 mA)		0.4	V	4
V_{OL}	Match Output LOgic 0 Voltage (I_{OUT} = 18 mA)		0.4	V	4

Notes :

1. Measured with load shown in Figure 8A.
2. Measured with load in Figure 8B.
3. Measured with load in Figure 8C.
4. All Voltages referenced to GND.
5. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}$ (max) and with the outputs open circuits. $t_{AVAV} = t_{AVAV}$ (min) duty cycle 100%.
6. Input leakage current specifications are valid for all V_{IN} such that $0V < V_{IN} < V_{CC}$. Measured at $V_{CC} = V_{CC}$ (max).
7. Output leakage current specifications are valid for all V_{OUT} such that $0V < V_{OUT} < V_{CC}$, S = V_{IH} and V_{CC} in valid operating range.
8. Sampled, not 100% tested, outputs deselected.

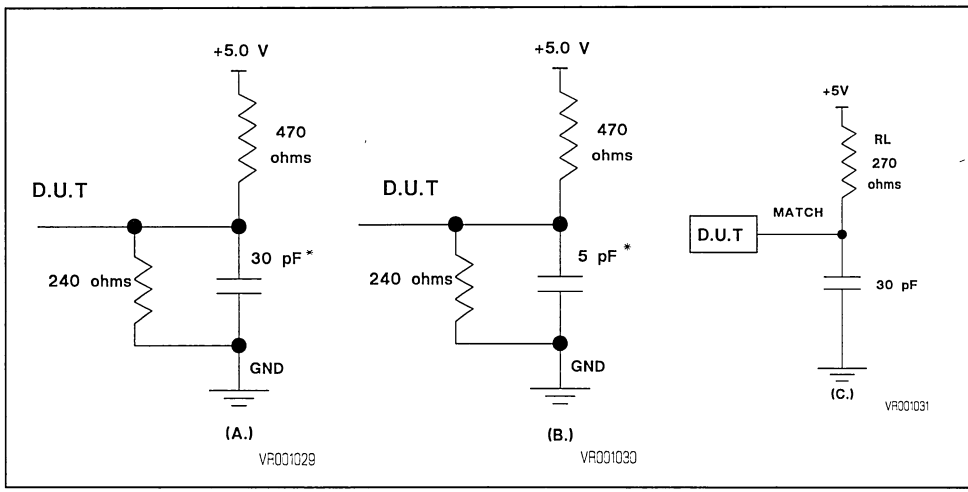
CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit	Notes
C_{IN}	Capacitance on all Input pins	4	pF	8
C_{OUT}	Capacitance on Q Output pins	10	pF	8

AC TEST CONDITIONS

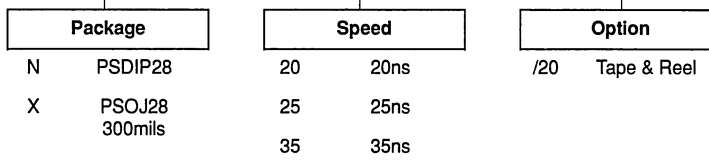
Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	1.5	ns
Input and Output Signal Timing Reference Level	1.5	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ± 5%	V

Figure 8. Equivalent Output Load Circuits



ORDERING INFORMATION

Example: MK48S74 X 20 /20



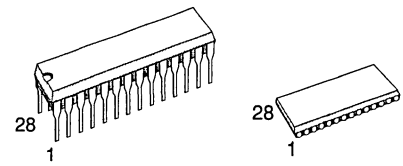
Package		Speed		Option	
N	PSDIP28	20	20ns	/20	Tape & Reel
X	PSOJ28 300mils	25	25ns		
		35	35ns		

For a list of available options of Package and Speed, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

VERY FAST CMOS 8K x 8 CACHE TAGRAM

- 8K x 8 CMOS SRAM WITH ON BOARD COMPARATOR
- ADDRESS TO COMPARE ACCESS TIME: 15, 17, 20, 25ns
- FAST CHIP SELECT COMPARE ACCESS : 8ns
- MATCH OUTPUT WITH FAST TAG DATA TO COMPARE ACCESS OF: 12, 15ns Max
- STATIC OPERATION-NO CLOCKS OR TIMING STROBES REQUIRED
- FULL CMOS FOR LOW POWER OPERATION.
- TOTEM-POLE MATCH OUTPUT
- THREE-STATE OUTPUTS
- 28 PIN 300 MIL DIP & 28 PIN 300 MIL SOJ
- HIGH SPEED ASYNCHRONOUS RAM CLEAR



PSDIP28 (N)

PSOJ28 (X)
300 mils

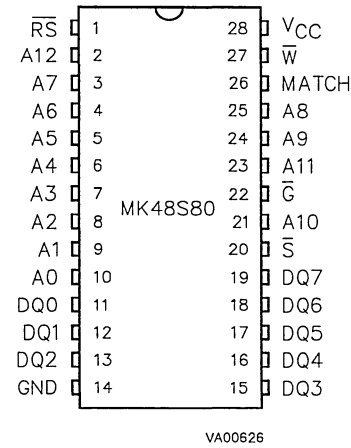
TRUTH TABLE

$\overline{W}$	$\overline{S}$	$\overline{G}$	$\overline{RS}$	Mode	DQ	Match
X	X	X	L	Reset Clear	High-Z	High
X	H	X	H	Deselect	High-Z	High
H	L	H	H	Miss	D_{IN}	Low
H	L	H	H	Match	D_{IN}	High
H	L	L	H	Read	Q_{OUT}	High
L	L	X	H	Write	D_{IN}	High

PIN NAMES

A0 - A12	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
MATCH	Comparator Output
$\overline{S}$	Chip Select
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RS}$	Reset Flash Clear
V_{CC}, GND	5 Volts, Ground

Figure 1. Pin Connection



DESCRIPTION

The MK48S80 is a 65,536 fast static cache TAGRAM™ organized as 8K x 8 bits. It is fabricated using SGS-THOMSON's low power, high performance HCMOS4 technology. The MK48S80 features fully static operation requiring no external clocks or timing strobes. The device requires a single 5V supply and is fully TLL compatible. The MK48S80 has a fast Chip Select control for high speed operation to the Match Compare valid, and device select/deselect operations. Additionally, the MK48S80 provides a Reset Clear, and MATCH compare pin. The Reset Clear input provides an asynchronous RAM clear control which clears all internal RAM bits to zero. The MATCH output is in a totem-pole configuration to minimize swtiching delays associated with open-drain devices. During a MATCH compare cycle, an on-board 8-bit comparator compares the Data Inputs (8-bit TAG) at the specified address index (A0-A12) to the internal RAM data. If a miss condition exists, where at least one bit of TAG data does not match the internal RAM, then the MATCH output issues a LOW miss signal.

OPERATIONS

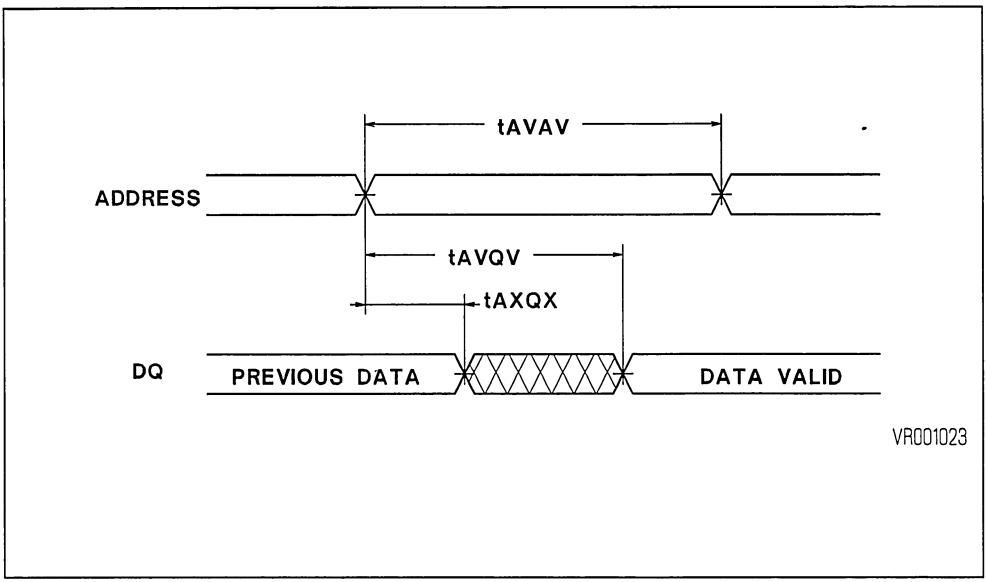
READ MODE

The MK48S80 is in the read mode whenever Write Enable ($\overline{W}$) is HIGH with Output Enable ($\overline{G}$) LOW, and Chip Select ($\overline{S}$) is active. This provides access to data from eight of 65,536 locations in the static memory array. The unique address specified by the 13 Address Inputs defines which one of the 8192 8-bit bytes is to be accessed. Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is LOW, and $\overline{S}$ is LOW. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{SLQV} or t_{GLQV}) rather than the addresses. The state of the DQ pins is controlled by the $\overline{S}$, $\overline{G}$, and $\overline{W}$ control signals. Data out may be indeterminate at t_{SLQX} and t_{GLQX}, but data line will always be valid at t_{AVQV}.

READ CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
(0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

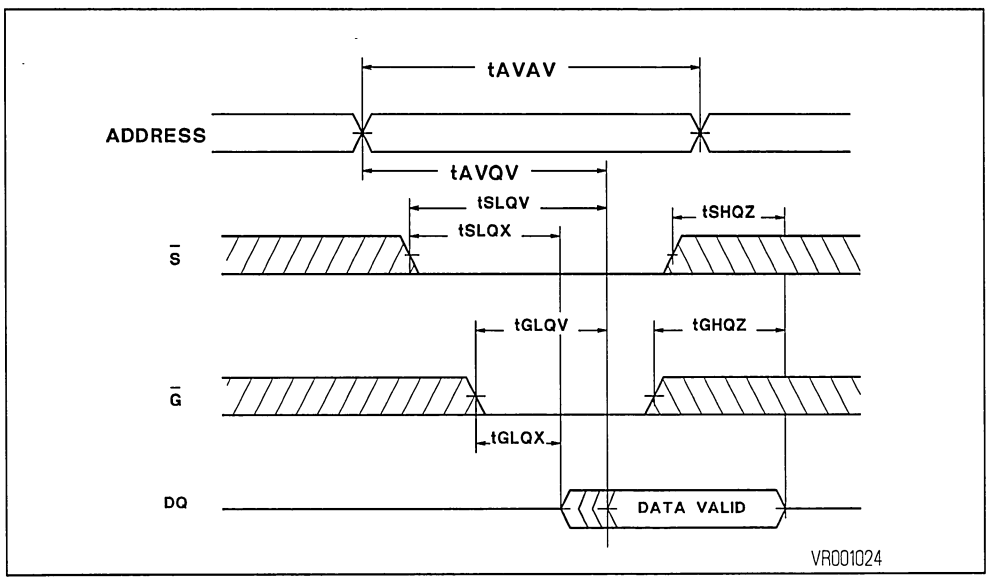
Symbol		Parameter	-15		-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_{RC}	Read Cycle Time	20		20		20		25		ns	
t_{AVQV}	t_{AA}	Address Access Time		20		20		20		25	ns	1
t_{SLQV}	t_{CSA}	Chip Select Access Time		15		15		15		15	ns	
t_{GLQV}	t_{OEA}	Output Enable Access Time		10		10		10		15	ns	1
t_{SLQX}	t_{CSL}	Chip Select to Output Low-Z	0		0		0		0		ns	
t_{GLQX}	t_{OEL}	Output Enable to Low-Z	0		0		0		0		ns	
t_{SHQZ}	t_{CSZ}	Chip Select to High-Z		9		9		9		9	ns	
t_{GHQZ}	t_{OEZ}	Output Enable to High-Z		8		8		8		8	ns	2
t_{AXQX}	t_{OH}	Output Hold From Address Change	3		3		3		3		ns	1

Figure 2. Read Timing No. 1 (Address Access)



Note: Chip Select and Output Enable are presumed Valid, $\overline{W} = V_{IH}$

Figure 3. Read Timing No. 2 ($W = V_{IH}$)



WRITE MODE

The MK48S80 is in the Write mode whenever the $\overline{W}$ and $\overline{S}$ pins are LOW. Chip Select or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of Chip Select being active with $\overline{W}$ LOW. Therefore address setup times are referenced to Write Enable and Chip Select as t_{AVWL} and t_{AVSL}, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{S}$ or $\overline{W}$. If the output is enabled ($\overline{S}$ = LOW, $\overline{G}$ = LOW), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{S}$, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{S}$ or $\overline{W}$.

WRITE CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions

(0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

Symbol		Parameter	-15		-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_{WC}	Write Cycle Time	20		20		20		25		ns	
t_{AVWL}	t_{AS}	Address Set-up to Write Enable Low	0		0		0		0		ns	
t_{AVSL}	t_{AS}	Address Set-up to Chip Select	0		0		0		0		ns	
t_{AVWH}	t_{AW}	Address Valid to End of Write	15		15		15		20		ns	
t_{WLWH}	t_{WEW}	Write Pulse Width	15		15		15		20		ns	
t_{WHAX}	t_{AH}	Address Hold Time After End of Write	0		0		0		0		ns	
t_{SLSH}	t_{CSW}	Chip Select to End of Write	15		15		15		20		ns	
t_{SHAX}	t_{WR}	Write Recovery Time to Chip Select	0		0		0		0		ns	
t_{DVWH}	t_{DW}	Data Valid to End of Write	10		10		10		13		ns	
t_{WHDX}	t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{WHQX}	t_{WEL}	Write High to Output Low-Z (Active)	0		0		0		0		ns	2
t_{WLQZ}	t_{WEZ}	Write Enable to Output High-Z		5		5		5		5	ns	2

Figure 4. Writing Timing No. 1 (Write Control)

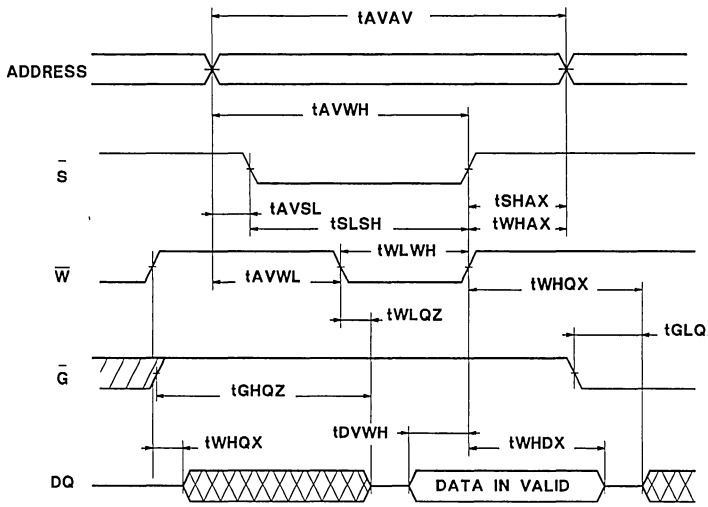
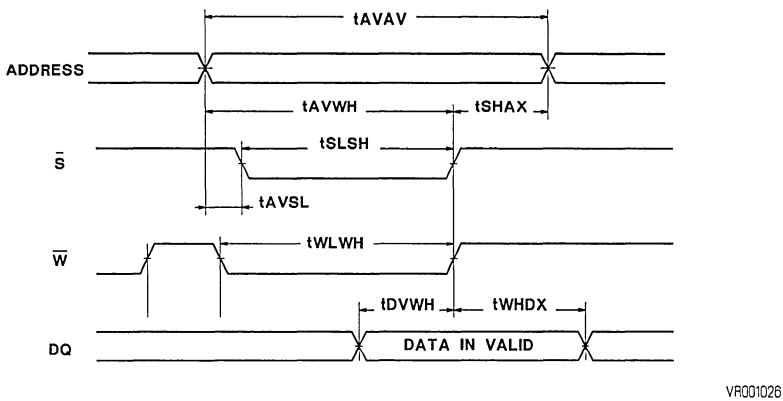


Figure 5. Writing Timing No. 2 (Chip Select Control)



Note: $\overline{G} = V_{IH}$

COMPARE MODE

The MK48S80 is in the Compare mode whenever $\overline{W}$ and $\overline{G}$ are HIGH provided Chip Select ($\overline{S}$) is active LOW. The 13 index address inputs (A0-A12) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ_0-DQ_7) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal, then a hit condition occurs (MATCH = HIGH). When at least one bit is not equal, then MATCH will go LOW signifying a miss condition. The MATCH output will be valid t_{AVMV} from stable address, or t_{TVMV} from valid Tag Data when S is LOW. Should the address be stable with valid Tag Data, and the device is deselected ($\overline{S}$ = HIGH), then MATCH will be valid t_{SLMV} from the falling edge of Chip Select ($\overline{S}$). When executing a write-to-compare cycle ($\overline{W}$ = LOW, $\overline{G}$ = LOW or HIGH), MATCH will be valid t_{WHMV} or t_{GHMV} from the latter rising edge of $\overline{W}$ or $\overline{G}$ respectively.

RESET MODE

The MK48S80 allows an asynchronous reset clear whenever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits (65,536 bits) to a logic zero as long as $t_{RSL-RSH}$ is satisfied. The state of the outputs is determined by the control logic input pins $\overline{S}$, $\overline{W}$, and $\overline{G}$ during reset (see Truth Table). The MATCH output will go HIGH t_{RSL-MH} from the falling edge of $\overline{RS}$, and all inputs will not be recognized unit t_{RSH-AV} from the rising edge of reset ($\overline{RS}$).

APPLICATION

The MK48S80 operates from a 5V supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. A pull-up resistor is also recommended for the $\overline{RS}$ input. This will ensure that any low going system noise, coupled onto the input does not drive $\overline{RS}$ below V_{IH} minimum specifications. This will enhance proper device operation, and avoid possible partial flash clear cycles. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK48S80 can also interface to 5V CMOS on all inputs and outputs. The MK48S80 provides the system designer with 64K fast static memory, a MATCH out-put, and a BYTEWIDE on-board comparator, all in one chip. The MK48S80 compares the contents of addressed RAM locations to the current

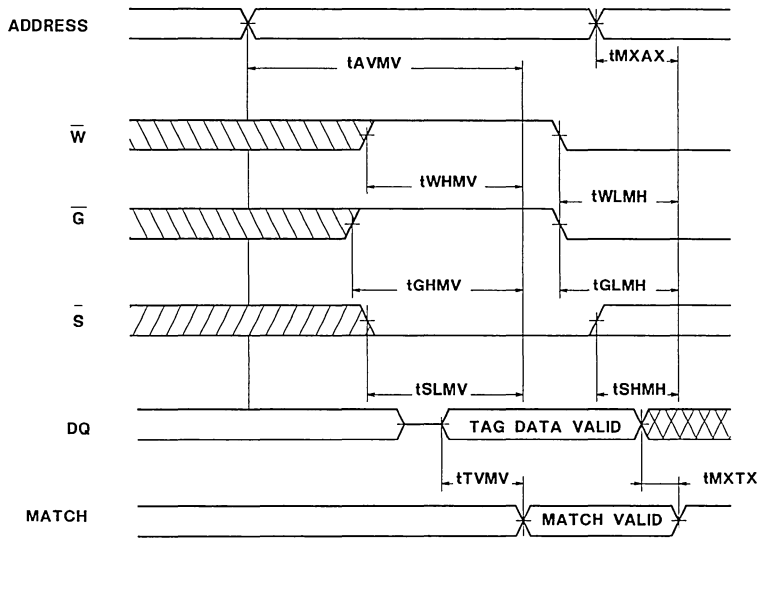
COMPARE CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
(0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

Symbol		Parameter	-15		-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVMV}	t_{AMA}	Address to MATCH Valid		15		17		20		25	ns	1
t_{SLMV}	t_{CSM}	Chip Select to MATCH Valid		8		8		10		15	ns	1
t_{SHMH}	t_{CSMH}	Chip Deselect to MATCH High		5		5		8		12	ns	1
t_{TVMV}	t_{DMA}	Tag Data to MATCH Valid		12		12		12		15	ns	1
t_{GHMV}	t_{OEM}	$\overline{G}$ High to MATCH Valid		10		10		10		15	ns	1
t_{GLMH}	t_{OEMH}	$\overline{G}$ Low to MATCH High		10		10		10		12	ns	1
t_{WHMV}	t_{WEM}	$\overline{W}$ High to MATCH Valid		10		10		10		20	ns	1
t_{WLMH}	t_{WEMH}	$\overline{W}$ Low to MATCH High		10		10		10		15	ns	1
t_{MXAX}	t_{MHA}	MATCH Hold From Address	1		1		1		1		ns	1
t_{MXTX}	t_{MHD}	MATCH Hold From Tag Data	0		0		0		0		ns	1

RESET CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
(0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

Symbol		Parameter	-15		-17		-20		-25		Unit
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RSC}	t_{RC}	Flash Clear Cycle Time	80		80		80		80		ns
t_{RSL-AX}	t_{RSX}	Reset Clear (RS) to Inputs Don't Care	0		0		0		0		ns
t_{RSH-AV}	t_{RSV}	$\overline{RS}$ to Inputs Valid	5		5		5		5		ns
$t_{RSL-RSH}$	t_{RSP}	Reset ($\overline{RS}$) Pulse Width	75		75		75		75		ns
t_{RSL-MH}	t_{RSM}	Reset ($\overline{RS}$) to MATCH High		15		15		15		15	ns

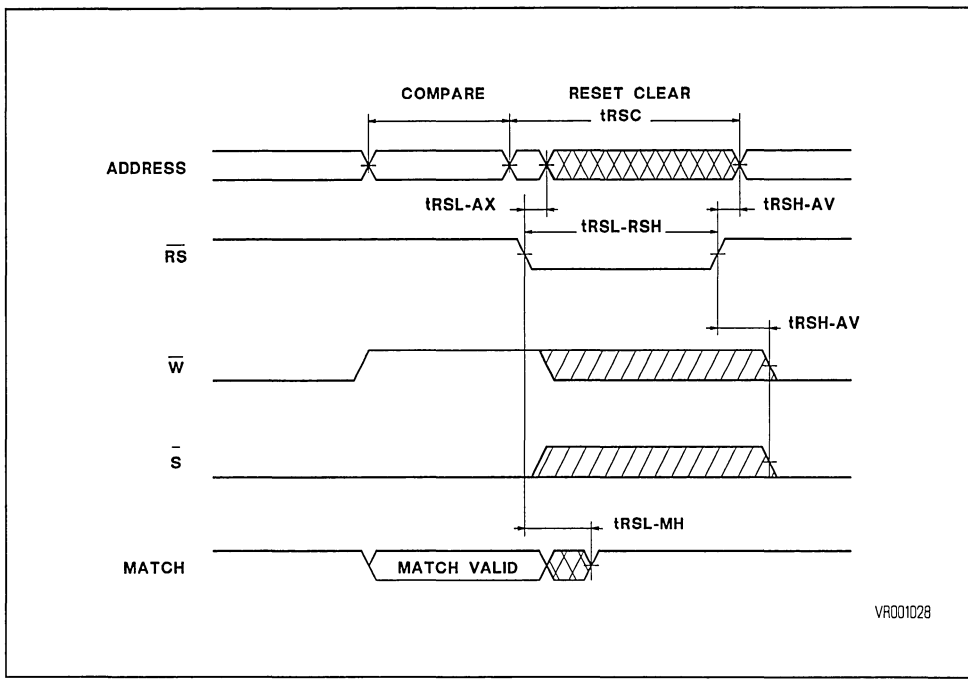
Figure 6. Match Compare Timing



data inputs. A logic one "1" output on the MATCH pin indicates that the input data and the RAM data match. Conversely, a logic zero "0" on the MATCH pin indicates at least one bit of difference between the RAM contents and the input TAG, generating a miss.

The MATCH output is constructed with a totem-pole arrangement. The totem-pole configuration allows the designer to minimize switching delays and noise problems associated with open-drain devices. In a cache subsystem, the MATCH signal provides the processor or CPU with the necessary information concerning wait state conditions. The purpose of a cache subsystem is to maintain a duplicate copy of portions of the main memory. When a valid match occurs, the system processor uses data from the fast cache memory, and avoids longer cycles to the main memory. Therefore, implementing cache subsystems with the MK48S80, and providing good hit or match ratio designs will enhance overall system performance. Because high frequency current transients will be associated with the operation of the MK48S80, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Though often times not thought of as such, the traces of a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

Figure 7. Reset Timing



Note: $\overline{G}$ = High

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	–0.3 to 6	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
P_D	Power Dissipation	1	W
I_{OUT}	Output Current	50	mA

Note: This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0\ °C \le T_A \le +70\ °C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage	4.75	5.25	V	3
GND	Ground	0	0	V	3
V_{IH}	Logic 1 All Inputs	2.2	V_{CC} + 0.3	V	3
V_{IL}	Logic 0 All Inputs	–0.3	0.8	V	3

DC ELECTRICAL CHARACTERISTICS ($0\ °C \le T_A \le +70\ °C$; $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current		160	mA	4
I_{IL}	Input Leakage Current	–1	1	µA	5
I_{OL}	Output Leakage Current	–5	5	µA	6
V_{OH}	Logic 1 Output Voltage (I_{OUT} = –4 mA)	2.4		µA	3
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8 mA)		0.4	V	3

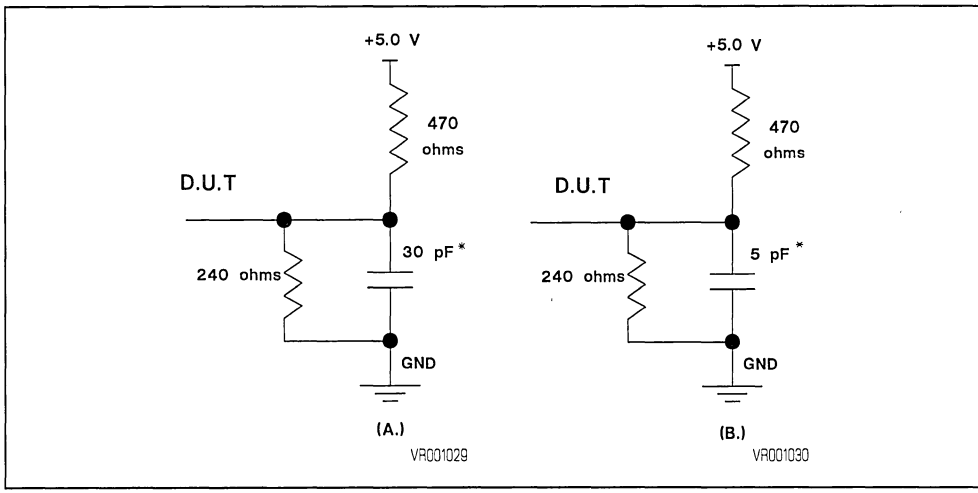
CAPACITANCE ($T_A = 25\ °C$, f = 1MHz)

Symbol	Parameter	Max.	Unit	Notes
C_{IN}	Capacitance on all Input pins	4	pF	7
C_{OUT}	Capacitance on Q Output pins	10	pF	7

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	1.5	ns
Input and Output Signal Timing Reference Level	1.5	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ± 5%	V

Figure 8. Equivalent Output Load Circuits

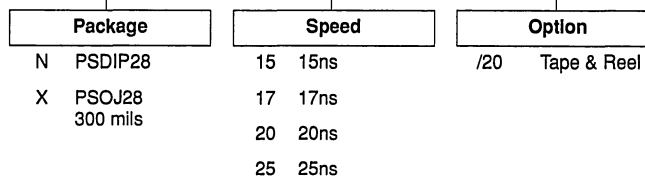


Notes :

1. Measured with load shown in Figure 8A.
2. Measured with load shown in Figure 8B.
3. All voltages referenced to GND.
4. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}$ (max) and with the outputs open circuit. $t_{AVAV} = t_{AVAV}$ (min) duty cycle 100%.
5. Input leakage current specifications are valid for all V_{IN} such that $0\ V < V_{IN} < V_{CC}$. Measured at $V_{CC} = V_{CC}$ (max).
6. Output leakage current specifications are valid for all V_{OUT} such that $0\ V < V_{OUT} < V_{CC}$, $\overline{S} = V_{IH}$ and V_{CC} in valid operating range.
7. Sampled, not 100% tested.

ORDERING INFORMATION

Example: MK48S80 X 17 /20

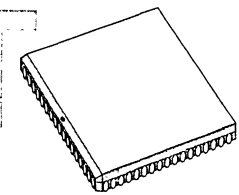


For a list of available options of Package and Speed, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.

VERY FAST CMOS 2K x 20 CACHE TAGRAM

- 2048 x 20 CMOS SRAM WITH ONBOARD COMPARATOR
- MATCH ACCESS TIME: 17, 20, 25ns
- READ ACCESS TIME: 20ns Max
- RESET CYCLE: 25ns Max
- I_{CC} (OUTPUTS DESELECTED): 250mA Max
- STANDBY: 50mA Max
- FLASH CLEAR VALID BIT FUNCTION
- TARGET APPLICATION: 68040-30, AND 80486-50 CACHE



PLCC68 (Q)

PIN NAMES

V_{CC}, GND	5 Volts, Ground
A0 - A10	Index Address Inputs
CDO0	Clearable Tag Data I/O
DQ1 - DQ19	Tag Data I/O
E0 - E3	Chip Enable (Programmable Active Low or High)
P0 - P3	Chip Enable Program Inputs
$\overline{RS}$	Reset Input (Active Low)
$\overline{S}$	Chip Select Input (Active Low)
$\overline{W}$	Write Enable (Active Low)
$\overline{G}$	Data Output Enable (Active Low)
C0	Compare 0 Output (3-State) Hit = High, Miss = Low
C1	Compare 0 Output (3-State) Hit = High, Miss = Low
$\overline{H0}$	Force Hit 0 Input (Active Low)
$\overline{H1}$	Force Hit 1 input (Active Low)
$\overline{M0}$	Force Miss 0 Input (Active Low)
$\overline{M1}$	Force Miss 1 Input (Active Low)
$\overline{CG0}$	Compare 0 Output Enable (Active Low)
$\overline{CG1}$	Compare 1 Output Enable (Active Low)

Figure 1. Logic Diagram

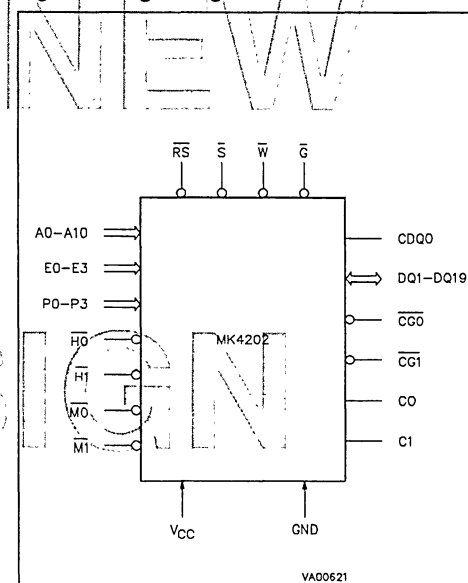
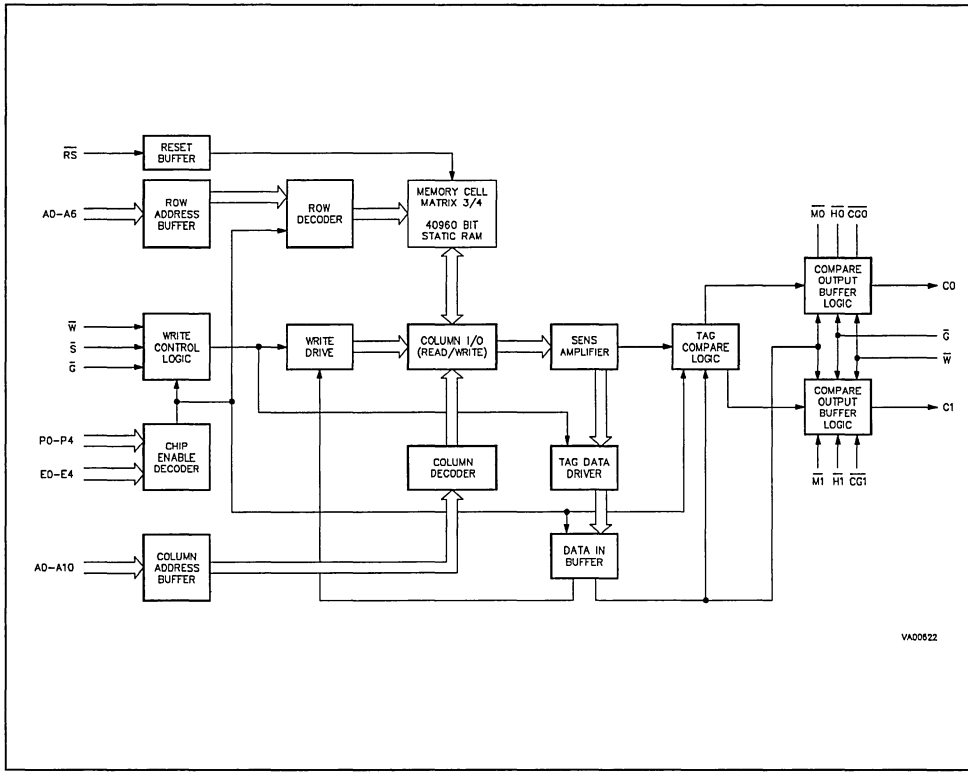


Figure 2. Block Diagram



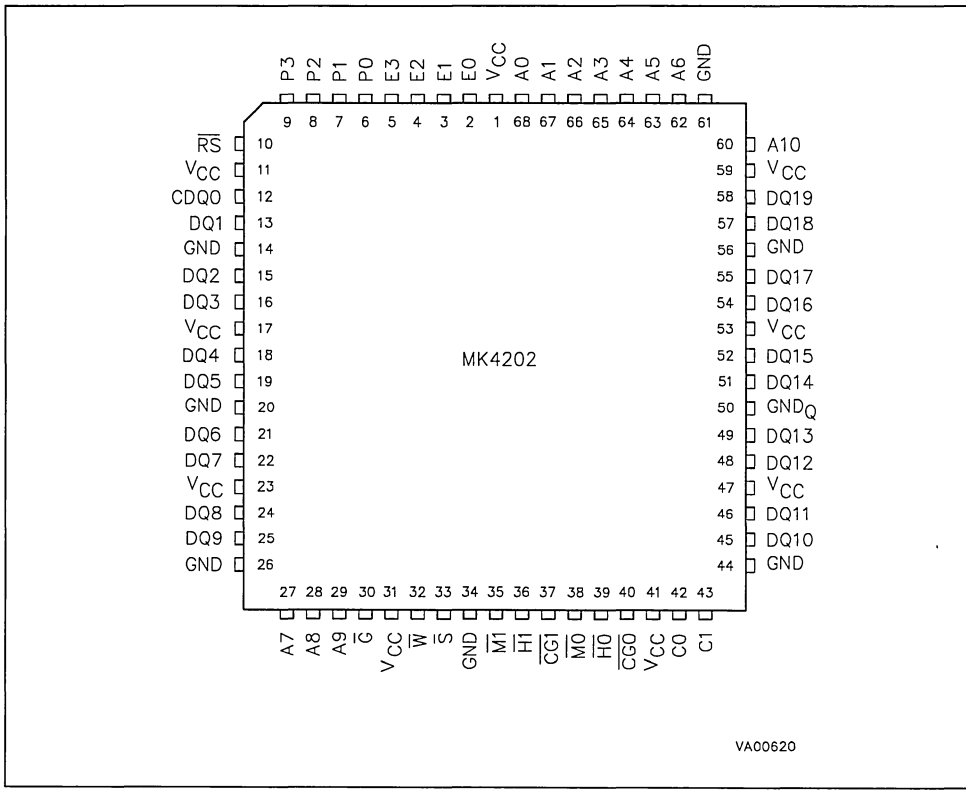
DEVICE DESCRIPTION AND FEATURES

The MK4202 is designed to be connected DIRECTLY to a high performance 32 bit microprocessor, allowing the elimination of the logic delays associated with collecting HIT or Miss outputs into a subsequent gate or the RC delays associated with wired-OR open collector match outputs.

The MK4202 TAGRAM™ has four major features that allow direct connection:

1. Wide enough for almost any TAGRAM application without requiring multiple chip width expansion and the delays that would result.
2. Four (4) programmable CHIP ENABLE inputs, allowing DEPTH EXPANSION without any of the attendant chip enable decode delays that would otherwise be required.
   P0-P3 should be tied directly to V_{CC} or Ground, or through pull-up or pull-down resistors. The MK4202 is selected when E0-E3 equals P0-P3 in a binary match.
   (Example: E0-E1 = 0110, P0-P3 = 0110.)
3. 3-STATE COMPARE OUTPUTS, allowing all Compare outputs to be bused together so the Address-to-Compare access time for a depth expanded application is identical to that of a single device. The Programmable Chip Enables prevent bus contention by assuring that only one TAGRAM at a time drives each Compare bus when in Compare mode.

Figure 3. Pin Connection



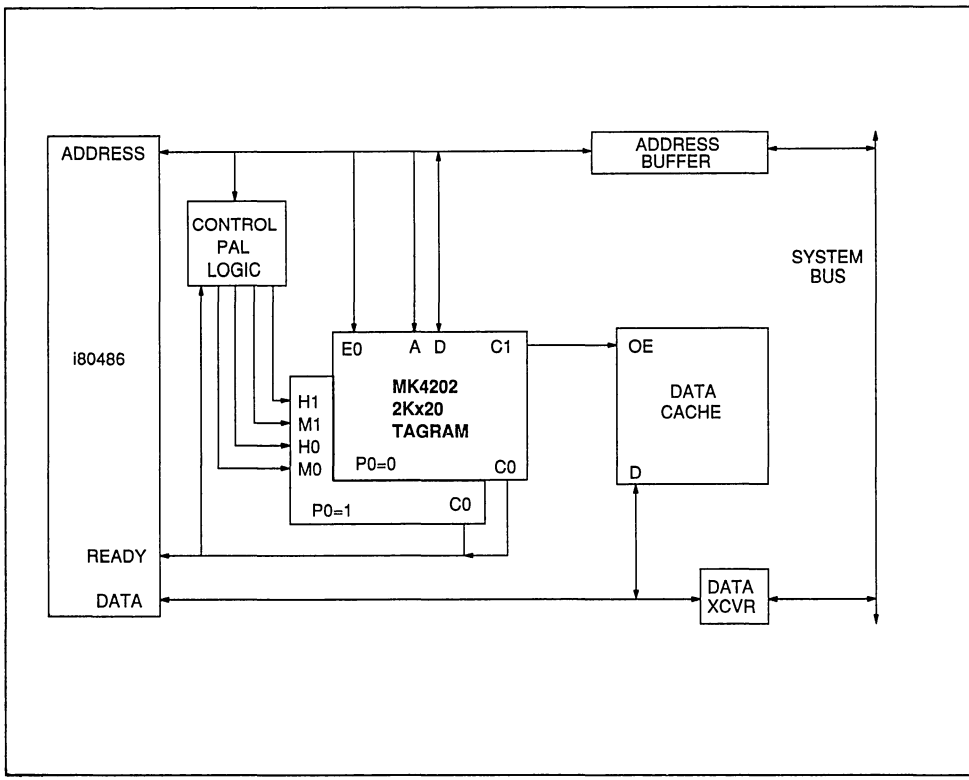
4. DUAL COMPARE OUTPUTS (C0 and C1) and FORCED HIT ($\overline{H0}$ and $\overline{H1}$) and FORCED MISS ($\overline{M0}$ and $\overline{M1}$) inputs for each. The arrangement allows direct connection of the TAGRAM to a processor input (such as the READY input on Intel based processors), and to the Output Enable (OE) on a Data CACHE bank. The connection of the signals which would have been connected to the processor inputs and/or data CACHE inputs, are PASSED THRU the MK4202 TAGRAM, thus eliminating the need for subsequent gates to collect the COMPARE OUTPUTS to develop an input to the processor and/or data CAHE. The net effect is that the Address-to-Compare access time dem-onstrated by the MK4202 is all of the delay the user must consider. The alternative approach, using narrow TAGRAMs with open collector output or narrow TAGRAMs with 2-state outputs and 7.5ns programmable logic, requires that the narrow TAGRAMs demonstrate a 9ns Address-to-Compare access time to yield the same performance in a user's system that the MK4202 provides.

POWER DISTRIBUTION

The MK4202, being a 20 output device, obviously requires the use of good power bussing techniques. MK4202 has been designed in such a way as to allow the user to minimize the effects of switching transients on overall circuit operation. Of particular interest is the separate bussing of the V_{CC} and GND lines to the output drivers. The advantage provided by these separate power pins is that voltage sags and ground bumps seen on these pins are not reflected into the other portions of the chip, particu-larly the input structures. As a result, switching noise in the supply has much less effect on input levels, providing the user with more noise margin than would otherwise be available.

Of course all V_{CC} and GND pins must always be at the same DC potential. Differences between them due to AC effects are expected, but must be minimized through the adequate use of bussing and bypassing. All specifications and testing are done with GND ± 10mV RMS, V_{CC} = ± 10mV RMS with instantaneous peak differences not exceeding 50mV.

Figure 4. Application Block Schematic



TRUTH TABLE

$\overline{RS}$	$\overline{S}$	E	$\overline{W}$	$\overline{G}$	$\overline{M0}$, $\overline{M1}$	$\overline{H0}$, $\overline{H1}$	$\overline{CG0}$, $\overline{CG1}$	MODE	C0, C1	DQ	NOTES
Hi	–	X	–	–	Lo	X	X	Force Miss	Low	–	1
Hi	–	X	–	–	Hi	Lo	X	Force Hit	High	–	1
Hi	–	X	–	–	HI	Hi	Hi	Comp Disable	Hi-Z	–	1
Hi	X	F	X	X	Hi	Hi	X	Standby	Hi-Z	Hi-Z	
Hi	X	T	Hi	Hi	Hi	Hi	Hi	Compare	Hi-Z	D in	
Hi	X	T	Hi	Hi	Hi	Hi	Lo	Compare	Hi/Lo	D in	
Hi	Hi	T	Lo	X	Hi	Hi	Lo	Hit	Hi	Hi-Z	
Hi	Hi	T	X	Lo	Hi	Hi	Lo	Hit	Hi	Hi-Z	
Hi	Lo	T	Lo	X	Hi	Hi	Lo	Write	Hi	D in	
Hi	Lo	T	Hi	Lo	Hi	Hi	Lo	Read	Hi	D Out	
Lo	Hi	X	X	X	–	–	–	Reset	–	Hi-Z	
Lo	X	F	X	X	–	–	–	Reset	–	Hi-Z	
Lo	X	X	Hi	Hi	–	–	–	Reset	–	Hi-Z	
Lo	X	X	Hi	Lo	–	–	–	Reset	–	Lo-Z	
Lo	Lo	T	Lo	X	–	–	–	Not Allowed	–	Hi-Z	2
Lo	X	T	Hi	Hi	Hi	Hi	Lo	Reset	Lo	D in	3

Notes:
1. Force hit/miss operations independent of other RAM operations.
2. May disrupt Reset, will not damage device.
3. Reset will force C0 and C1 low during a valid compare when CDQ0 is D_{IN}= HIGH.

Key: X = Don't Care
F = (False) E0-E3 pattern DOES NOT match P0-P3 pattern.
T = (True) E0-E3 pattern DOES match P0-P3 pattern.
– = Not related to identified mode of operation.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to GND	–0.3 to 7.0	V
T_A	Ambient Operating Temperature (T_A)	0 to 70	°C
T_{STG}	Ambient Storage Temperature (plastic)	–55 to 125	°C
P_D	Total Device Power Dissipation	2.5	W
I_{OUT}	RMS Output Current per Pin	25	mA

Note : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5V ±5%)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
I_{CC}	Average Power Supply Current			250	mA	1
I_{CCA}	Active Power Supply Current (f = 0)			200	mA	1
I_{SB1}	TTL Standby Current			50	mA	1
I_{IL}	Input Leakage Current			±1	µA	2
I_{OL}	Output Leakage Current			±10	µA	3
V_{IL}	Input Low Voltage	–0.3		0.8	V	4
V_{IH}	Input High Voltage	2.2		V_{CC}+0.3	V	4,5
V_{OH}	Logic 1 Output Voltage (I_{OUT} = –4mA)	2.4			V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8mA)			0.4	V	4

Notes :

1. Measured with outputs open. V_{CC} max.
2. Measured with V_{IN} = 0V to V_{CC}.
3. Measured at CDQ0, DQ1-DQ19, C0 and C1.
4. All voltages referenced to GND.
5. Inputs (P0-P3) require V_{IH} min. = 4.5 volts and V_{IL} max. = 0.5 volts.
6. Sampled, not 100% tested. Measured at 1 MHz.
7. Measured at all data I/O's, C0 and C1.

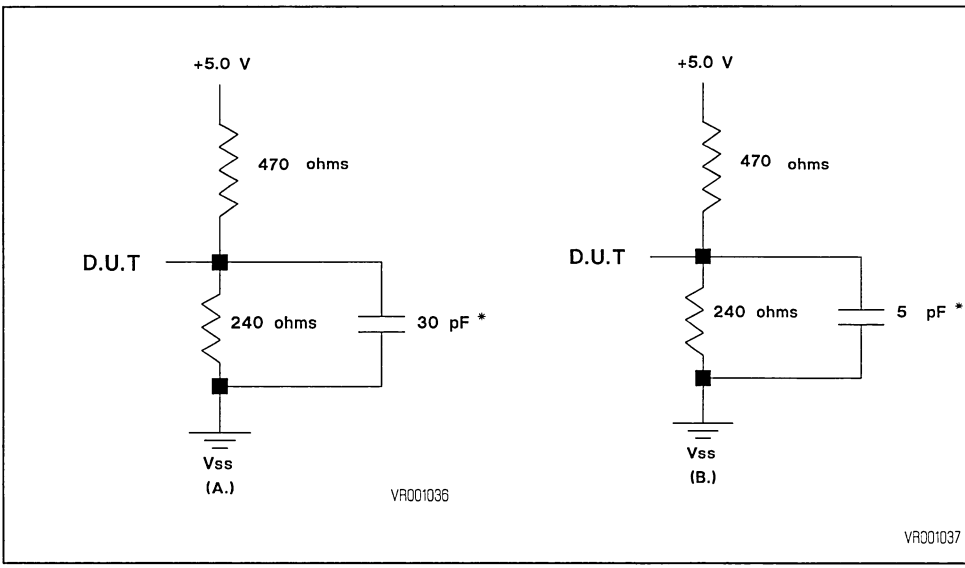
CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_1	Input Capacitance	4		4	pF	6
C_0	Output Capacitance	8		10	pF	6.7

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	5	ns
Input and Output Timing Reference Level	1.5	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ± 5%	V

Figure 5. Equivalent Output Load Circuits



READ MODE

The MK4202 is in the Read mode whenever $\overline{W}$ is HIGH, and $\overline{G}$ is LOW provided Chip Select ($\overline{S}$) is LOW and a true Chip Enable pattern (E0-E3) is applied. The 11 address inputs (A0-A10) define a unique index address giving access to 20 of 40,960 bits of data in the static memory array. Valid data will be present at the 20 output pins within t_{AVQV} of the last stable address provided Chip Enable, Chip Select ($\overline{S}$), and Output Enable ($\overline{G}$) access times have been met. If Chip Enable, $\overline{S}$, or $\overline{G}$ access times are not met, data access will be measured from the latter falling edge or limiting parameter (t_{EVQV}, t_{SLQV}, or t_{GLQV}). The state of the tag data I/O pins is controlled by the (E0-E3), $\overline{S}$, $\overline{G}$, and $\overline{W}$ input pins. The data lines may be indeterminate at t_{EVQX}, or t_{SLQX}, or t_{GLQX}, but will always have valid data at t_{AVQV}.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Read Cycle Timing) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol		Parameter	-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_C	Cycle Time	20		25		30		ns	
t_{AVQV}	t_{AA}	Address Access Time		20		25		30	ns	
t_{AXQX}	t_{AOH}	Address Output Hold Time	5		5		5		ns	
t_{AEQV}	t_{EA}	Chip Enable Access Time		20		25		30	ns	
t_{EXQX}	t_{EOH}	Chip Enable Output Hold Time	4		4		4		ns	
t_{EVQX}	t_{ELZ}	Chip Enable TRUE to Low-Z	4		4		4		ns	
t_{EXQZ}	t_{EHZ}	Chip Enable FALSE to high-Z		8		8		10	ns	
t_{SLQV}	t_{SA}	Chip Select Access Time		12		15		18	ns	
t_{SHQX}	t_{SOH}	Chip Select Output Hold Time	2		2		2		ns	
t_{SLQX}	t_{SLZ}	Chip Select to Low-Z	3		3		3		ns	
t_{SHQZ}	t_{SHZ}	Chip Select to High-Z		4		4		6	ns	
t_{GLQV}	t_{GA}	Output Enable Access Time		10		13		15	ns	
t_{GHQX}	t_{GOH}	Output Enable Output Hold Time	2		2		2		ns	
t_{GLQX}	t_{GLZ}	Output Enable to Low-Z	2		2		2		ns	
t_{GHQZ}	t_{GHZ}	Output Enable to High-Z		5		5		8	ns	

Figure 6. Read Cycle

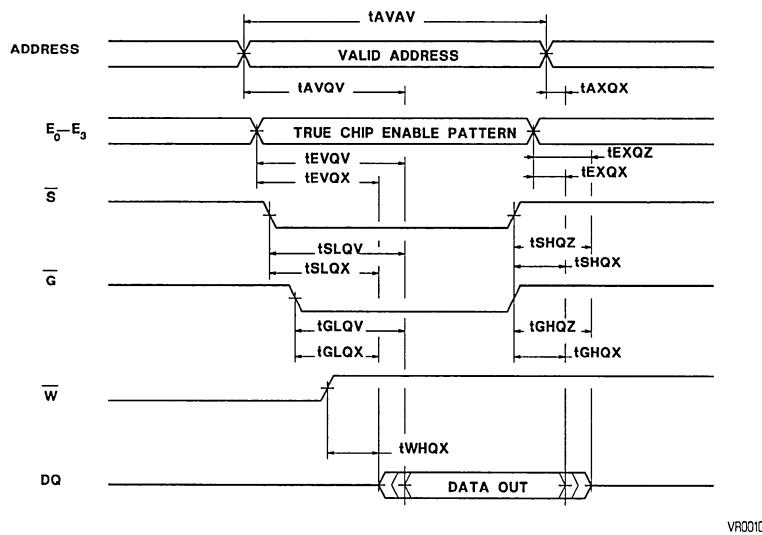


Figure 7. Address Read Cycle

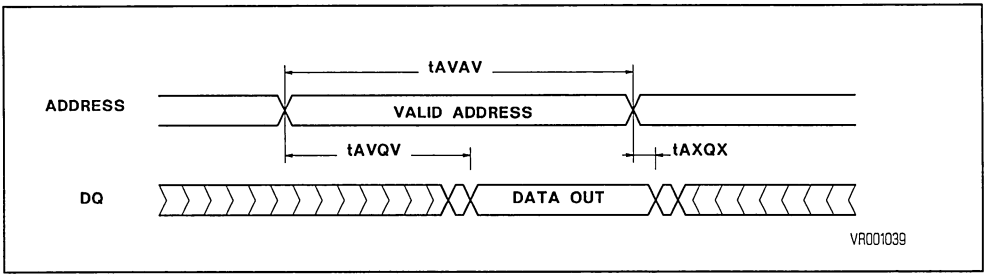


Figure 8. Chip Enable Read Cycle

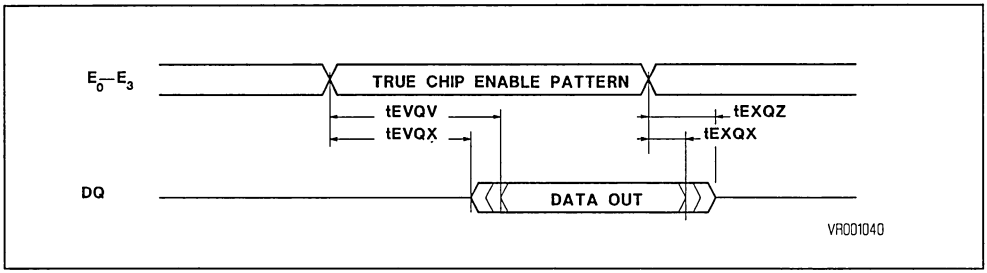


Figure 9. Chip Select Read Cycle

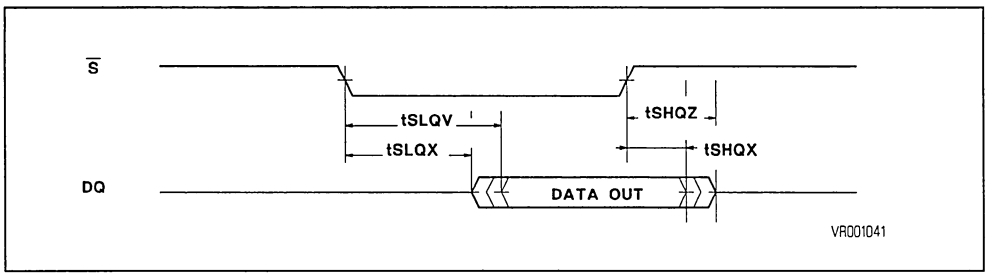
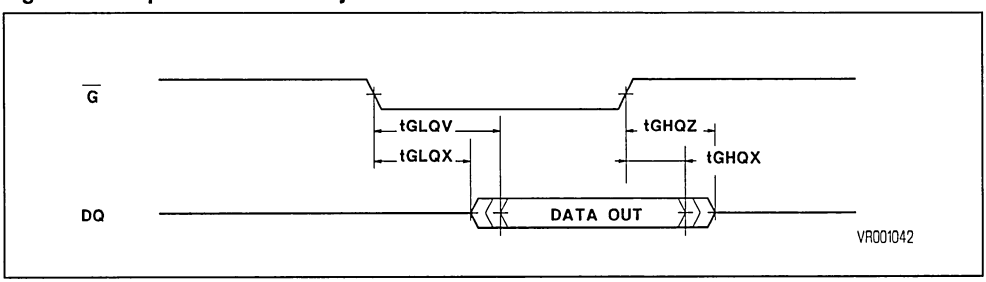


Figure 10. Output Enable Read Cycle



WRITE MODE

The MK4202 is in the Write mode whenever $\overline{W}$ is LOW provided Chip Select ($\overline{S}$) is LOW and a true Chip Enable pattern (E0-E3) is applied ($\overline{G}$ may be in either logic state). Addresses must be held valid throughout a write cycle, with either $\overline{W}$ or $\overline{S}$ inactive HIGH during address transitions. $\overline{W}$ may fall with stable addresses, but must remain valid for t_{WLWH}.

Since the write begins with the concurrence of $\overline{W}$ and $\overline{S}$, should $\overline{W}$ become active first, then t_{SLSH} must be satisfied. Either $\overline{W}$ or $\overline{S}$ can terminate the write cycle, therefore t_{DVWH} or t_{DVSH} must be satisfied before the earlier rising edge, and t_{WHDX} or t_{SHDX} after the earlier rising edge. If the outputs are active with $\overline{G}$ and $\overline{S}$ asserted LOW and with true Chip Enable, then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Write Cycle Timing) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol		Parameter	-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_C	Cycle Time	20		25		30		ns	
t_{AVWL}	t_{AS}	Address Set-up Time to $\overline{W}$ LOW	0		0		0		ns	
t_{WHAX}	t_{AH}	Address Hold Time from $\overline{W}$ HIGH	0		0		0		ns	
t_{AVSL}	t_{AS}	Address Set-up Time from $\overline{S}$ LOW	0		0		0		ns	
t_{SHAX}	t_{AH}	Address Hold Time from $\overline{S}$ HIGH	0		0		0		ns	
t_{EVWL}	t_{ES}	Chip Enable Set-up Time to $\overline{W}$ LOW	3		3		3		ns	
t_{WHEX}	t_{EH}	Chip Enable Hold Time from $\overline{W}$ HIGH	0		0		0		ns	
t_{EVSL}	t_{ES}	Chip Enable Set-up Time to $\overline{S}$ LOW	3		3		3		ns	
t_{SHEX}	t_{EH}	Chip Enable Hold time to $\overline{S}$ HIGH	0		0		0		ns	
t_{WLWH}	t_{WW}	Write Pulse Width	12		15		18		ns	
t_{SLSH}	t_{SW}	Chip Select Pulse Width	16		16		20		ns	
t_{DVWH}	t_{DS}	Data Set-up Time to $\overline{W}$ HIGH	12		12		15		ns	
t_{WHDX}	t_{DH}	Data Hold Time from $\overline{W}$ HIGH	0		0		0		ns	
t_{DVSH}	t_{DS}	Data Set-up Time to $\overline{S}$ HIGH	12		12		15		ns	
t_{SHDX}	t_{DH}	Data Set-up Time to $\overline{S}$ HIGH	0		0		0		ns	
t_{WLQZ}	t_{WZ}	Outputs Hi-Z from $\overline{W}$ LOW		8		8		10	ns	
t_{WHQX}	t_{WL}	Outputs Low-Z from $\overline{W}$ HIGH	5		5		5		ns	

Figure 11. $\overline{W}$ Write Cycle

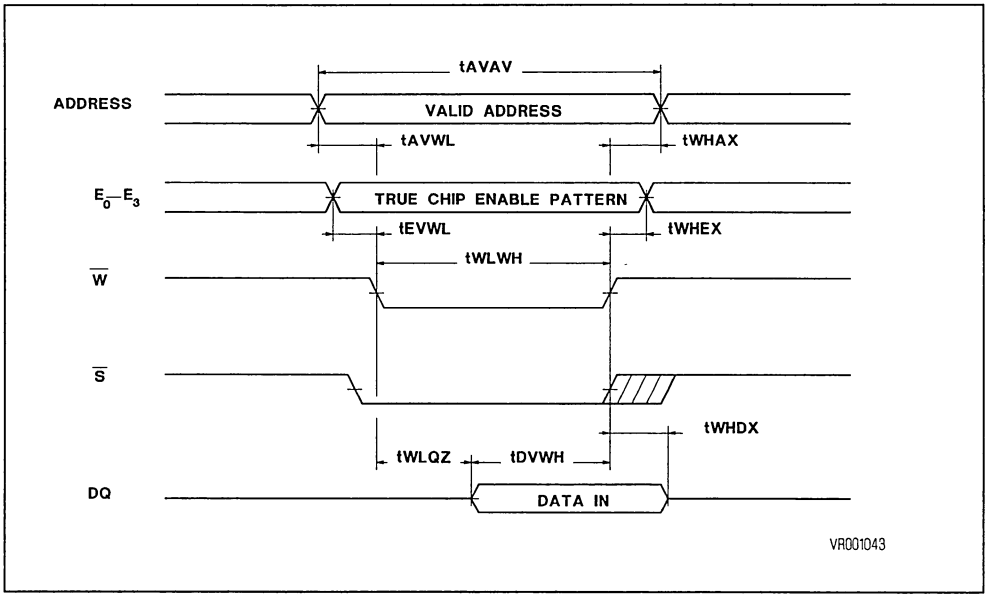
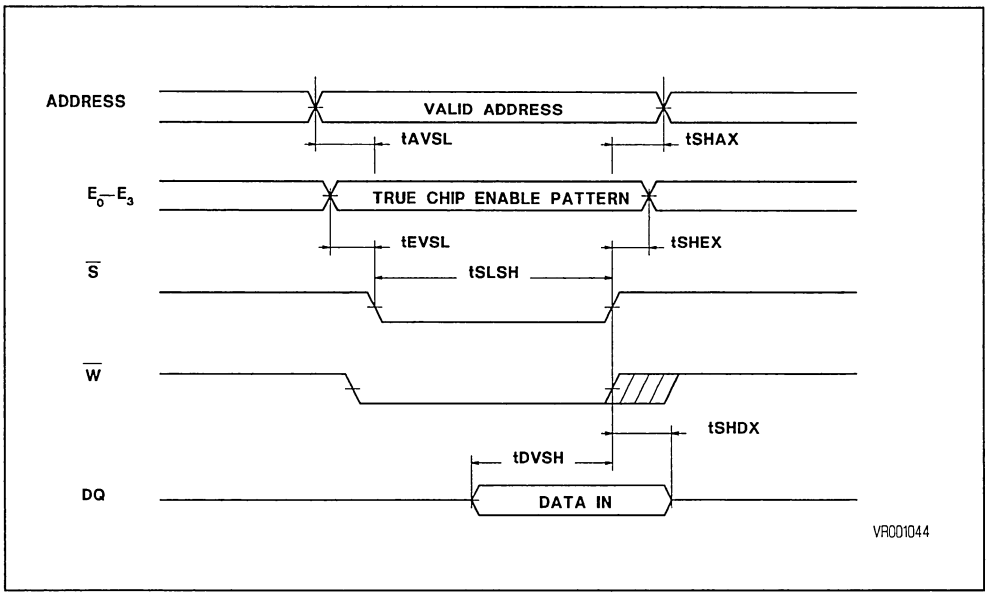


Figure 12. $\overline{S}$ Write Cycle



COMPARE MODE

The MK4202 is in the Compare mode whenever $\overline{W}$ and $\overline{G}$ are HIGH provided a true Chip Enable (E0-E3) pattern is applied. Chip Select ($\overline{S}$) is re-guarded as a don't care since the user is not concerned with the data outputs, but only with the Compare (C0, C1) outputs. $\overline{Mx}$ and $\overline{Hx}$ must be HIGH, and $\overline{CG0}$, $\overline{CG1}$ active LOW to enable the Compare outputs for a valid compare hit or miss.

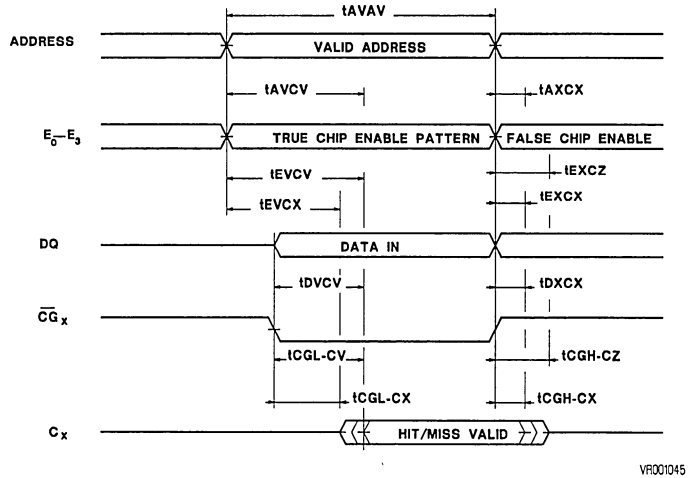
The 11 index address inputs (A0-A10) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ1-DQ19 and CDQ0) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal (match) then a hit condition occurs (C0 and C1 = HIGH). If at least one bit is not equal, then a miss occurs (C0 and C1 = LOW).

The Compare output will be valid t_{AVCV} from stable address, or t_{DVCV} from valid tag data provided Chip Enable is true, and $\overline{CGx}$ is active LOW. Should the address be stable with valid tag data, and Chip Enable false, then compare access will be within t_{EVCV} from true Chip Enable. When executing a write-to-compare cycle ($\overline{W}$ = LOW, and $\overline{G}$ = LOW or HIGH), C0 and C1 will be valid t_{WHCV} or t_{GHCV} from the latter rising edge of $\overline{W}$ or $\overline{G}$ respectively. Finally, when gating the Cx output in the compare mode with $\overline{CGx}$, the compare output will be valid t_{CGL-CV} from the falling edge of $\overline{CGx}$.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Compare Cycle Timing) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol		Parameter	-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVCV}	t_{ACA}	Address Compare Access Time		17		20		25	ns	
t_{AXCX}	t_{ACOH}	Address Compare Output Hold Time	5		5		5		ns	
t_{DVCV}	t_{DCA}	Tag Data Compare Access Time		14		16		20	ns	
t_{DXCX}	t_{DCH}	Tag Data Compare Hold Time	2		2		2		ns	
t_{WLCH}	t_{WCH}	$\overline{W}$ LOW to Compare HIGH		10		10		12	ns	
t_{WHCX}	t_{WCOH}	$\overline{W}$ Compare Output hold Time	1		1		1		ns	
t_{WLCX}	t_{WLCZ}	$\overline{W}$ to Compare HOLD	3		3		3		ns	
t_{WHCV}	t_{WCV}	$\overline{W}$ to Compare Valid		10		10		12	ns	
t_{GLCH}	t_{GCH}	$\overline{G}$ Low to Compare HIGH		10		10		12	ns	
t_{GHCX}	t_{CGOH}	$\overline{G}$ Compare Output Hold Time	1		1		1		ns	
t_{GLCX}	t_{GLCZ}	$\overline{G}$ to Compare to HOLD	3		3		3		ns	
t_{GHCV}	t_{GCV}	$\overline{G}$ to Compare Valid		10		10		12	ns	
t_{EVCV}	t_{ECA}	E True to Compare Access Time		17		20		25	ns	
t_{EXCX}	t_{ECOH}	E False Compare Hold Time	4		4		4		ns	
t_{EVCX}	t_{ECLZ}	E True to Compare Low-Z	4		4		4		ns	
t_{EXCZ}	t_{ECHZ}	E False to Compare High-Z		8		8		10	ns	
t_{CGL-CV}	t_{CGA}	$\overline{CGx}$ to Compare Access Time		6		8		10	ns	
t_{CGH-CX}	t_{CGOH}	$\overline{CGx}$ Compare Hold Time	2		2		2		ns	
t_{CGL-CX}	t_{CGLZ}	$\overline{CGx}$ LOW to Compare Low-Z	2		2		2		ns	
t_{CGH-CZ}	t_{CGHZ}	$\overline{CGx}$ HIGH to Compare High-Z		8		8		10	ns	

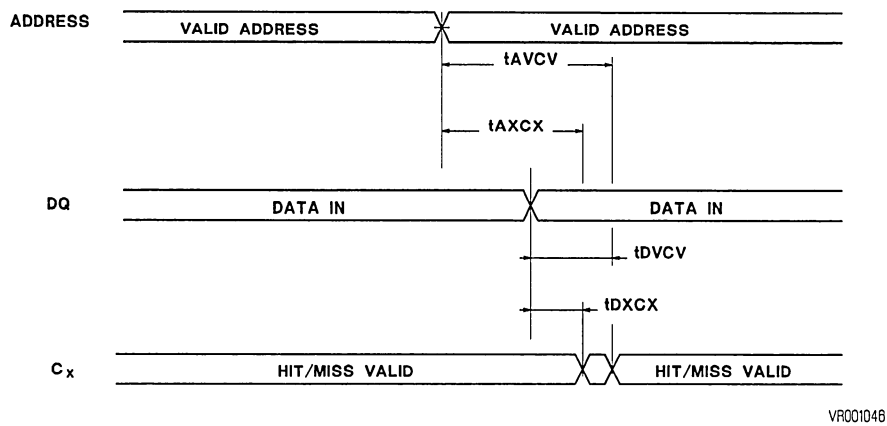
Figure 12. Summary Compare Cycle



Notes :

1. $\overline{W}$ and $\overline{G}$ are both assumed to be HIGH.
2. $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH.

Figure 13. Compare Cycle



Notes :

1. $\overline{W}$ and $\overline{G}$ are both HIGH, $\overline{CGx}$ is LOW and a true Chip Enable pattern is present.
2. $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH.

RESET MODE

The MK4202 allows an asynchronous reset whenever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits in CDQ0 (2048 bits) to a logic zero. This output can be used as a valid tag bit to insure a valid compare miss or hit . It should be noted that a valid write cycle is not allowed during a reset cycle ($\overline{W}$ = LOW, $\overline{S}$ = LOW, $\overline{RS}$ = LOW, and Chip Enable is true). The state of the data outputs is determined by the input control logic pins : Chip Enable, $\overline{S}$, $\overline{G}$, and $\overline{W}$ (see truth table). Should a reset occur during a valid compare cycle, and the CDQ_0 valid tag bit is set to a logic "1", then $\overline{C_X}$ will go LOW at t_{RSL-CL} from the falling edge of $\overline{RS}$.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Reset Cycle Timing) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol		Parameter	-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RLSL-AV}$	t_{RSC}	Reset Cycle Time	20		25		30		ns	
$t_{RSL-RSH}$	t_{RSW}	Reset pulse Width	20		25		30		ns	
t_{RSL-CL}	t_{RSCL}	$\overline{RS}$ LOW to Compare Output LOW		20		25		30	ns	
t_{RSH-AV}	t_{RSR}	Address Recovery Time	0		0		0		ns	
t_{RSH-EV}	t_{RSR}	Chip Enable Recovery Time	0		0		0		ns	

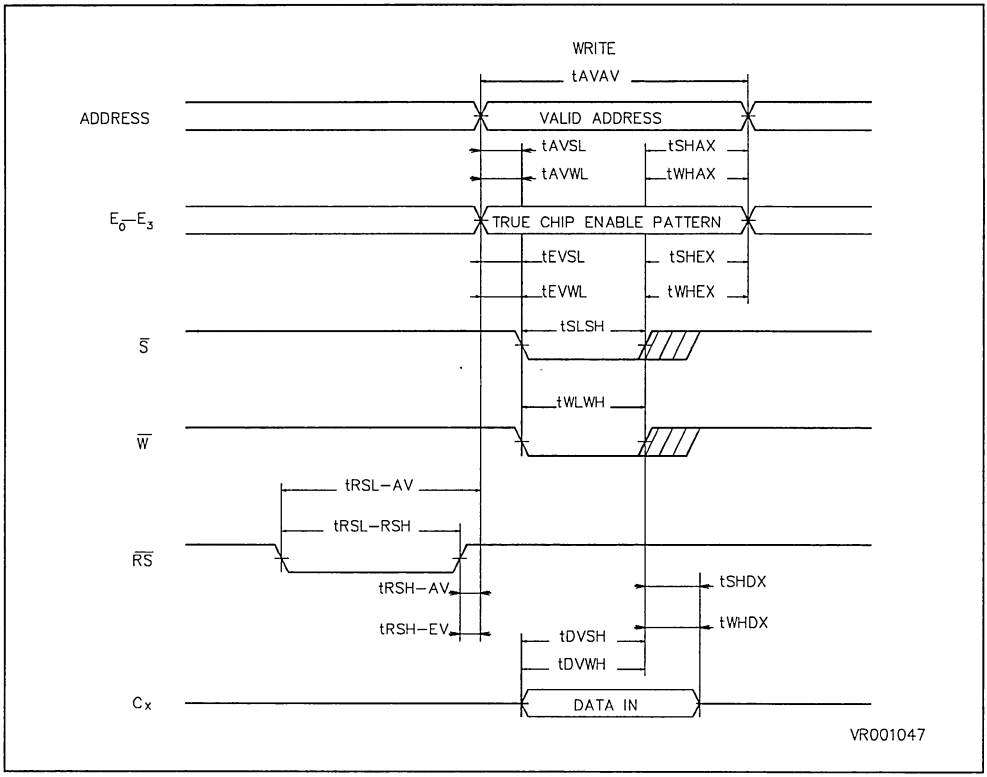
FORCE HIT AND FORCE MISS

The MK4202 can force either a miss or hit condition on the C0 and C1 outputs by asserting $\overline{M0}$, $\overline{M1}$ or $\overline{H0}$, $\overline{H1}$ LOW. A Force Miss overrides a Force Hit condition and is not dependent upon Compare Output Enables ($\overline{CGx}$) (see truth table). The C0 and C1 outputs will go HIGH within t_{HLCH} from the falling edge of $\overline{H0}$, $\overline{H1}$ or C0 and C1 will go LOW within t_{MLCL} from the falling edge of $\overline{M0}$, $\overline{M1}$. All $\overline{M0}$, $\overline{M1}$ and $\overline{H0}$, $\overline{H1}$ inputs must be HIGH during a valid compare cycle.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Force Hit or Miss Cycle Timing) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

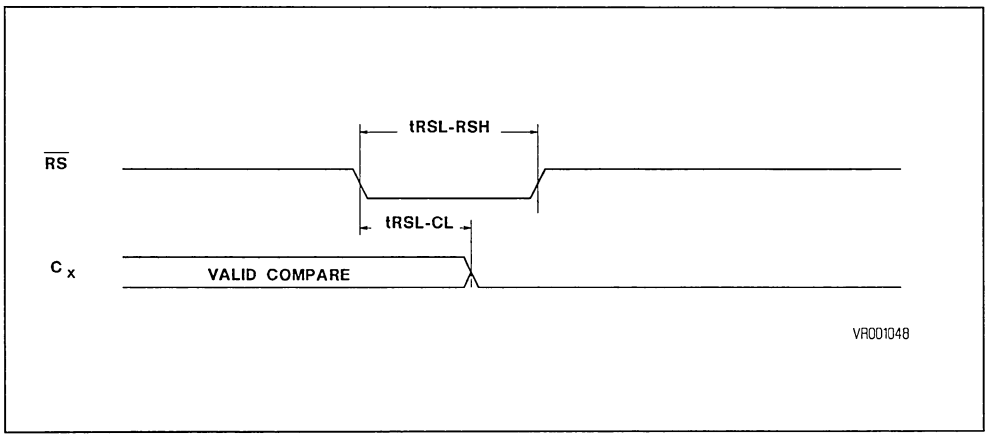
Symbol		Parameter	-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{HLCH}	t_{HA}	$\overline{Hx}$ to Force Hit Access Time		8		8		10	ns	
t_{HHCZ}	t_{HHZ}	$\overline{Hx}$ to Compare High-Z		5		5		8	ns	
t_{HL-CGX}	t_{HS}	Force Hit to $\overline{CGx}$ Don't Care	2		2		2		ns	
t_{HH-CGH}	t_{HR}	Force Hit to $\overline{CGx}$ Recognized	2		2		2		ns	
t_{MLCL}	t_{MA}	$\overline{Mx}$ to Force Miss Access Time		8		8		10	ns	
t_{MHCZ}	t_{MHZ}	$\overline{Mx}$ to Compare to High-Z		5		5		8	ns	
t_{ML-CGX}	t_{MS}	Force Miss to $\overline{CGx}$ Don't Care	2		2		2		ns	
t_{MH-CGH}	t_{MR}	Force Miss to $\overline{CGx}$ Recognized	2		2		2		ns	
t_{MLHX}	t_{MHS}	Force Miss to $\overline{Hx}$ Don't Care	2		2		2		ns	
t_{MHHH}	t_{MHR}	Force Miss to $\overline{Hx}$ Recognized	2		2		2		ns	

Figure 14. Reset Cycle



Note : Reset during an active write cycle is not allowed. A write cycle may disrupt Reset, but will not damage device.

Figure 15. Valid Compare - Reset



Note : CDQ0 is presumed to be HIGH.

Figure 16. Force Hit Force Miss

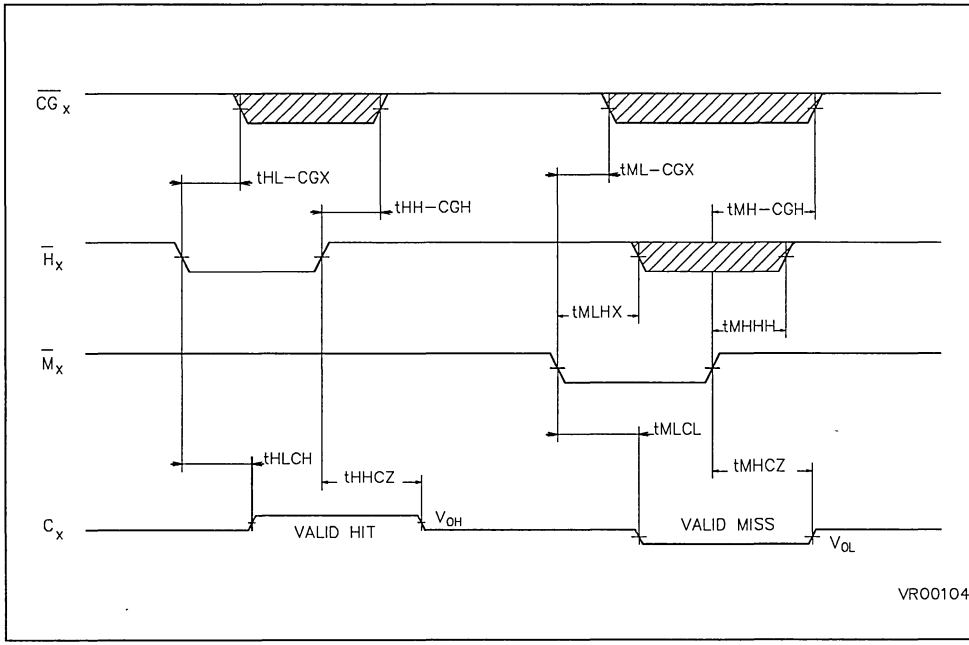
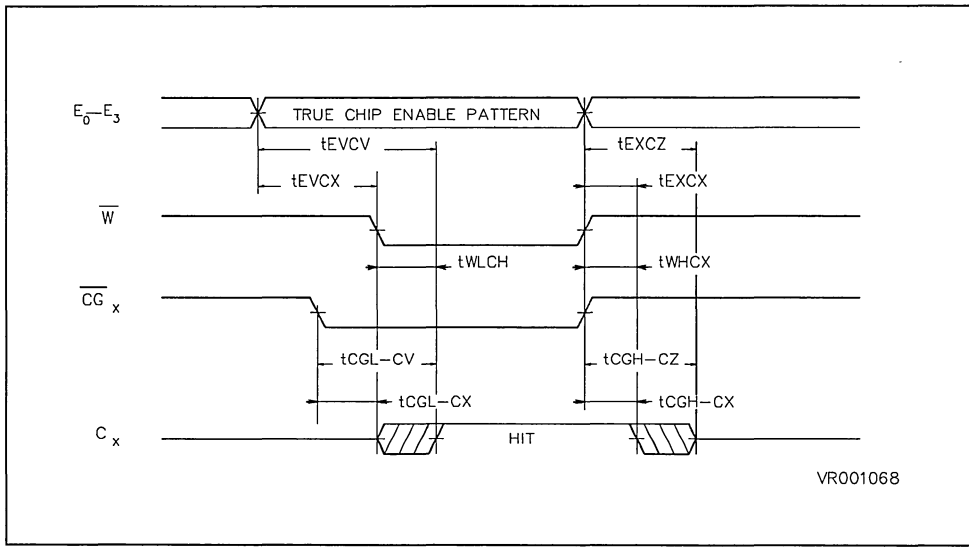
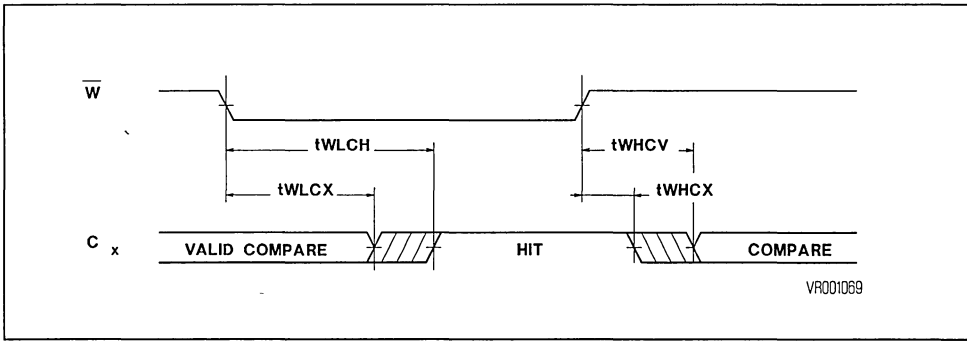


Figure 17. Late Write - Hit Cycle



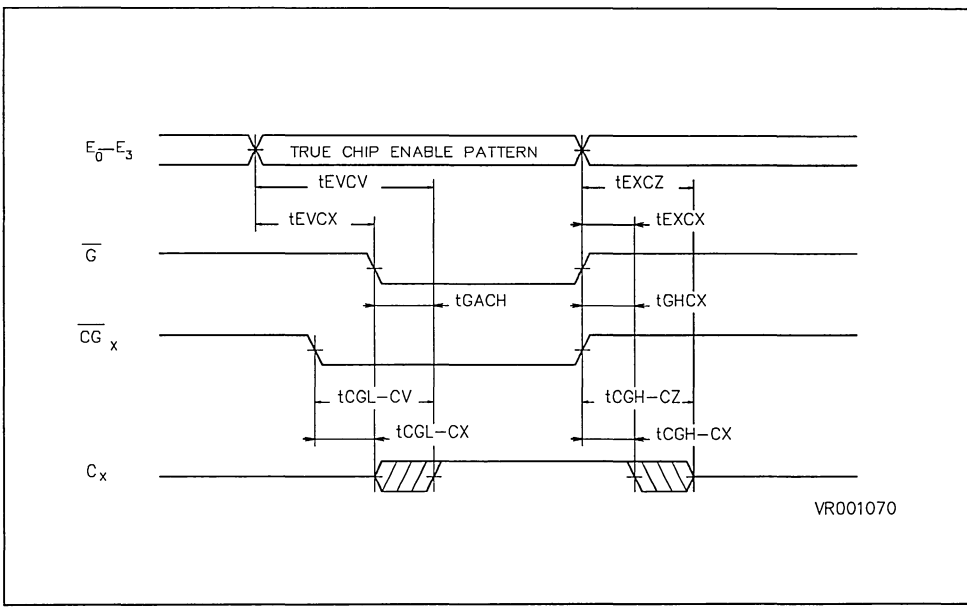
Note : $\overline{G}$ is HIGH and a Valid Address is present, $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH, with $\overline{CGx}$ LOW.

Figure 18. Compare - Write Hit - Compare Cycle



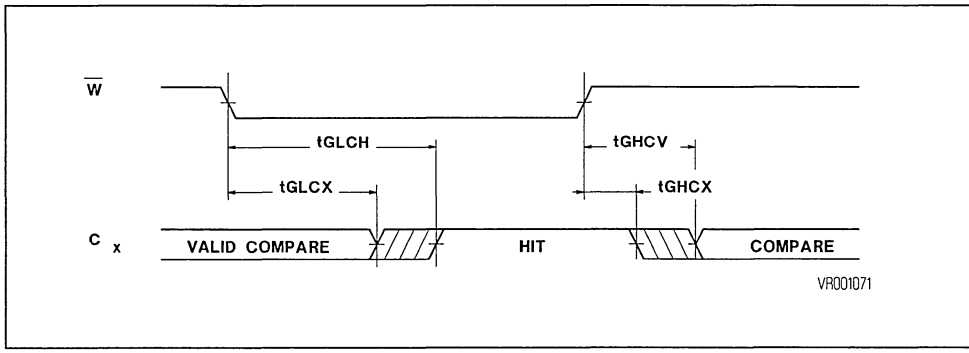
Note : $\overline{G}$ is HIGH and a Valid Address is present, $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH, with $\overline{CGx}$ LOW.

Figure 19. Late Read - Hit Cycle



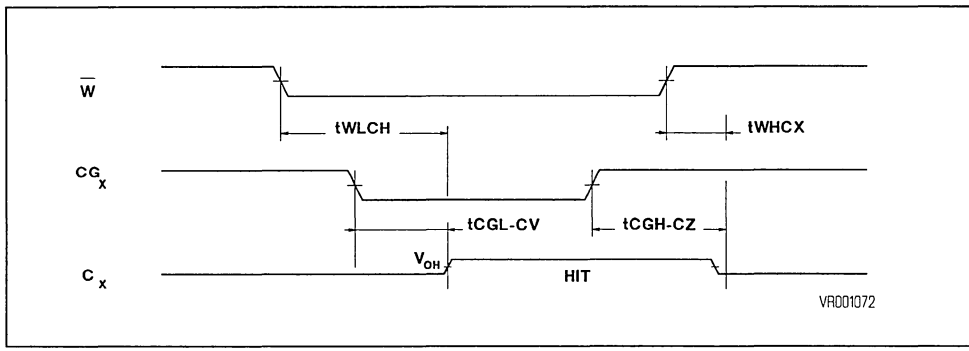
Note : $\overline{G}$ is HIGH and a Valid Address is present, $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH, with $\overline{CGx}$ LOW.

Figure 20. Compare - Read Hit - Compare Cycle



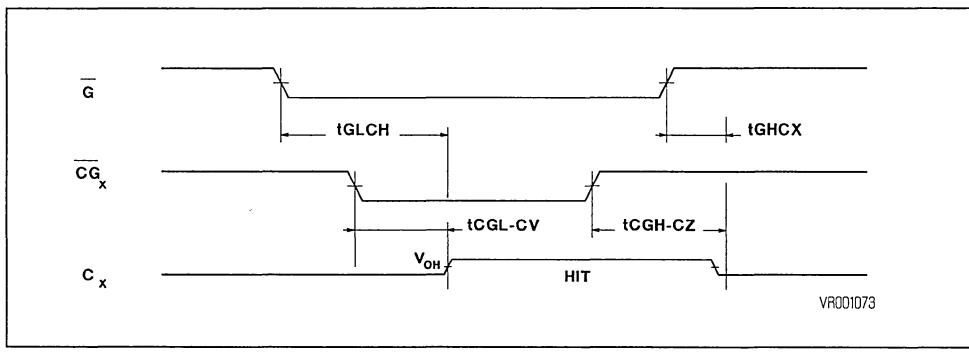
Note : $\overline{W}$ is HIGH and a Valid Address is present, $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH, with $\overline{CGx}$ LOW.

Figure 21. Early Write - Hit Cycle



Note : $\overline{G}$ is HIGH and a Valid Address is present, (E0 - E3) = True. $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH.

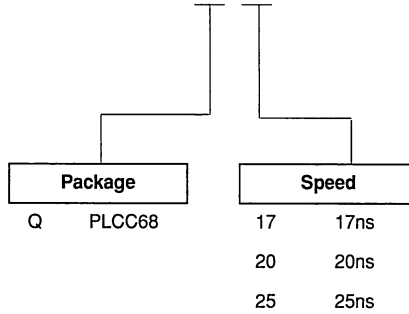
Figure 22. Early Read - Hit Cycle



Note : $\overline{W}$ is HIGH and a Valid Address is present, (E0 - E3) = True. $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH.

ORDERING INFORMATION

Example: MK4202 Q 17

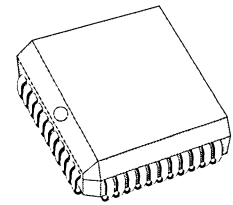


For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

VERY FAST CMOS 32K x 9 CACHE BRAM

- 32K x 9 CMOS SYNCHRONOUS BURST SRAM
- FAST CYCLE TIMES: 25, 30ns
- FAST ACCESS TIMES: 19, 24ns Max
- ON-BOARD BURST COUNTER
- INPUT REGISTERS (ADDR.,DATA,CTRL)
- SELF-TIMED WRITE CYCLE
- THREE STATE COMMON I/O
- HIGH OUTPUT DRIVE CAPABILITY
- ASYNCHRONOUS OUTPUT ENABLE ($\overline{G}$)
- BURST CONTROL INPUTS: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$
- DUAL CHIP SELECTS for EASY DEPTH EXPANSION



PLCC44 (Q)

DESCRIPTION

The MK62486 BRAM™ is a 288K (294,912 bit) CMOS Burst SRAM, organized as 32,768 words x 9 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology.

Figure 1. Logic Diagram

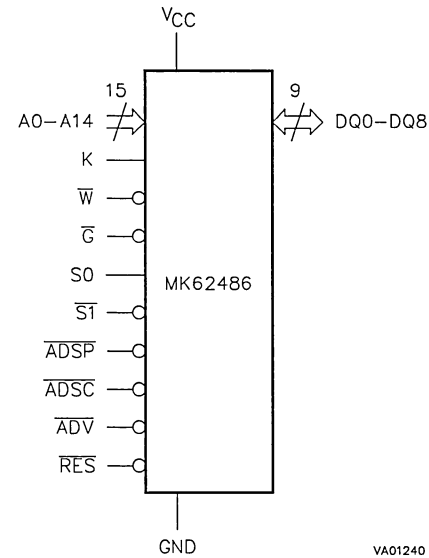


Table 1. Signal Names

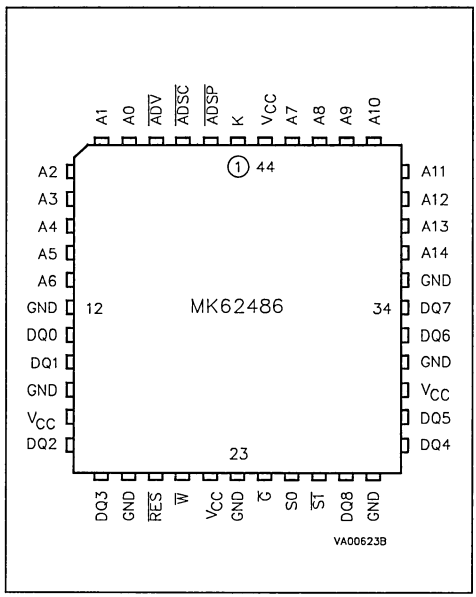
A0 - A14	Address Inputs
DQ0 - DQ8	Data Inputs / Outputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0	Chip Select 0, Active High
$\overline{S1}$	Chip Select 1, Active Low
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Cache Controller
$\overline{ADV}$	Burst Address Advance
$\overline{RES}$	Reserve, Tied Low
V_{CC}	Supply Voltage
GND	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.5 to 7	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (3)	Output Current	20	mA
P_D	Power Dissipation	1.2	W

Notes: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Up to a maximum operating V_{CC} of 5 5V only.
3. One output at a time, not to exceed 1 second duration.

Figure 2. LCC Pin Connections



DESCRIPTION (cont'd)

The device integrates a 2-bit burst counter, input regis-ters, high output drive capability, and high speed synchronous SRAM onto a single chip. The synchronous design provides precise control using an external clock (K) input.

The MK62486 is specifically adapted to provide a burstable, high performance secondary cache for the i486® microprocessor.

The MK62486 is available in a 44 lead Plastic Leaded Chip Carrier package (PLCC). The device provides multiple power and ground pins to reduce effects induced by output noise for high performance applications. The main Burst SRAM power requires a single 5V ± 5% supply, and all inputs and outputs are TTL compatible.

DEVICE OPERATIONS

Addresses (A0-A14), data inputs (DQ0-DQ8), and control signals, with exception of Output Enable ($\overline{G}$), are clock controlled inputs through non-inverting, pos-itive edge triggered registers. A cache burst address sequence can be initiated by either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) inputs, with subsequent burst addresses being internally generated by the Burst SRAM. The $\overline{ADV}$ input (burst address advance) provides control of the burst sequence, which imitates the i486 cache burst address sequence. Once a cache burst cycle begins, the subsequent burst address is generated internally each time the $\overline{ADV}$ input is asserted at the rising edge of the clock (K) input. The burst counter operates in the same manner for either cache burst write or read cycles.

The $\overline{ADSP}$ and the $\overline{ADSC}$ inputs control the start and the duration of the burst sequence respectively. Each time either address status input is asserted low, a new external base address is registered on the positive going edge of the clock (K).

Table 3. Asynchronous Truth Table

Mode	$\overline{G}$	DQ Status
Read	L	Data Out
Read	H	High-Z
Write[2]	X	Data In (High-Z)
Deselect	X	High-Z

Notes: 1. X = Don't Care.
2. For a cache write cycle following a read operation, $\overline{G}$ must be high before the input data required set-up time, and be held high through the input data hold time.

Table 4. Burst Count Sequence

External Address	A14-A2	A1	A0
1st Burst Address	A14-A2	A1	$\overline{A0}$
2nd Burst Address	A14-A2	$\overline{A1}$	A0
3rd Burst Address	A14-A2	$\overline{A1}$	$\overline{A0}$

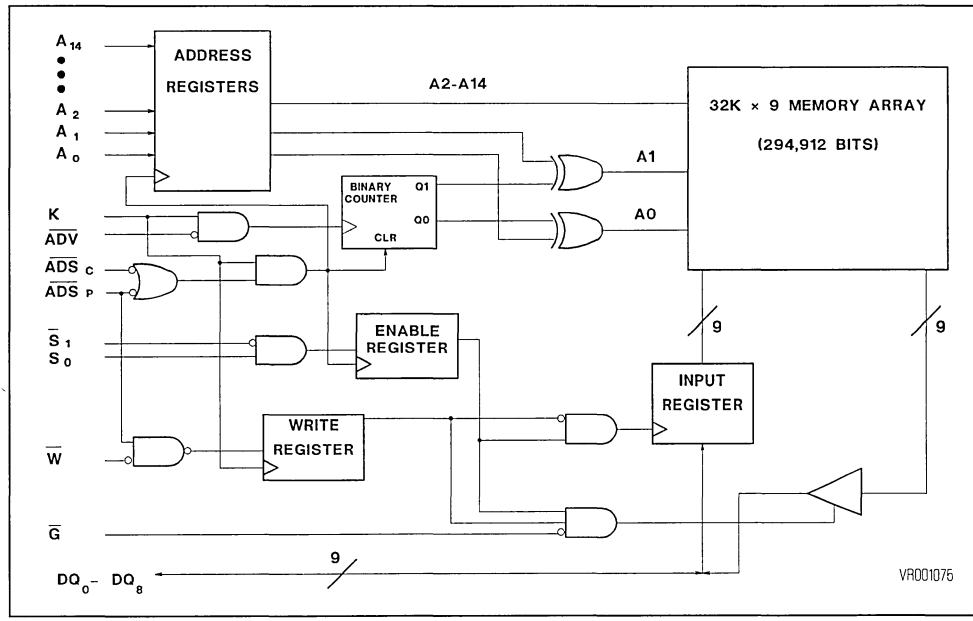
Note: The burst count sequence wraps around to the initial address after a full count is completed.

Table 5. Synchronous Truth Table

S0	$\overline{S1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K	Address	Operation
L	X	L	X	X	X	↑	N/A	Deselected
X	H	H	L	X	X	↑	N/A	Deselected
H	L	L	X	X	X	↑	External Base Address	Read Cycle - Begin Burst
H	L	H	L	X	L	↑	External Base Address	Write Cycle - Extend Burst
H	L	H	L	X	H	↑	External Base Address	Read Cycle - Extend Burst
X	X	H	H	L	L	↑	Advance Burst Address	Write Cycle - Continue Burst Sequence
X	X	H	H	L	H	↑	Advance Burst Address	Read Cycle - Continue Burst Sequence
X	X	H	H	H	L	↑	Hold Current Burst Address	Write Cycle - Suspend Burst Sequence
X	X	H	H	H	H	↑	Hold Current Burst • Address	Read Cycle - Suspend Burst Sequence

Notes: 1. X = Don't Care.
2. All inputs except $\overline{G}$ require set-up and hold times to the rising edge (low to high transition) of the external clock (K).
3. All read and write timings are referenced from $\overline{G}$ or K.
4. A read cycle is defined by $\overline{W}$ high or $\overline{ADSP}$ low for the required set-up and hold times. A write cycle is defined by $\overline{W}$ being asserted low for the set-up and hold times.
5. $\overline{G}$ is a don't care when $\overline{W}$ is registered low from the previous rising clock edge
6. Chip Selects must be true (S0 = high, $\overline{S1}$ = low) at each rising of the clock while $\overline{ADSP}$ or $\overline{ADSC}$ is asserted for the device to remain enabled; Chip Selects are registered whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted low at the rising edge of the clock.

Figure 3. Block Diagram



DEVICE OPERATIONS (cont'd)

When $\overline{ADSP}$ is asserted low, any ongoing burst cycle is interrupted, and a read operation (independent of $\overline{W}$ and $\overline{ADSC}$) is performed at the new registered external base address. A new burst cycle is initiated each time $\overline{ADSP}$ is asserted. By asserting $\overline{ADSC}$ low, the present burst cycle (initiated by $\overline{ADSP}$) is interrupted and an extended burst read or write (depending upon the logic state of $\overline{W}$ at the rising edge of K) is performed at the new registered base address. Chip selects (S0 and $\overline{S1}$) are only sampled when a new base address is loaded. Therefore, the chip selects are registered when either address status input is asserted low at the rising edge of the clock (K), and remain latched internally until the next assertion of either $\overline{ADSP}$ or $\overline{ADSC}$. The MK62486 Truth Tables and timing diagrams reference specific device operations.

It should be noted that the MK62486 allows a non-burst mode of operation where $\overline{ADSP}$ is the ADS# of the i486 processor in a 2-2 cycle mode of operation, and $\overline{ADSC}$ is held high during T2 (see Figure 5). However, the non-burst mode obviously negates the advantage of the internal burst counter for fast cache fill operations. In either mode (burst or non-burst), the write cycles are internally self-timed, and are initiated by the rising edge of the clock input. Self-timed write cycles eliminate com-

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

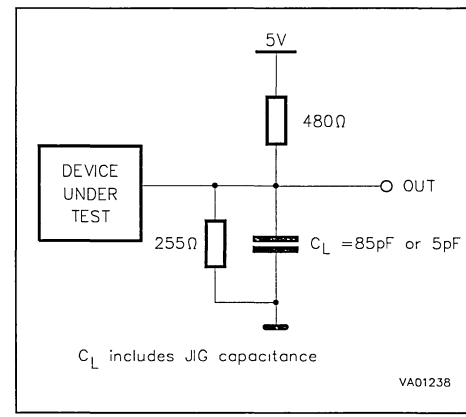


Table 6. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		5	pF
C_{OUT} [2]	Output Capacitance	V_{OUT} = 0V		10	pF

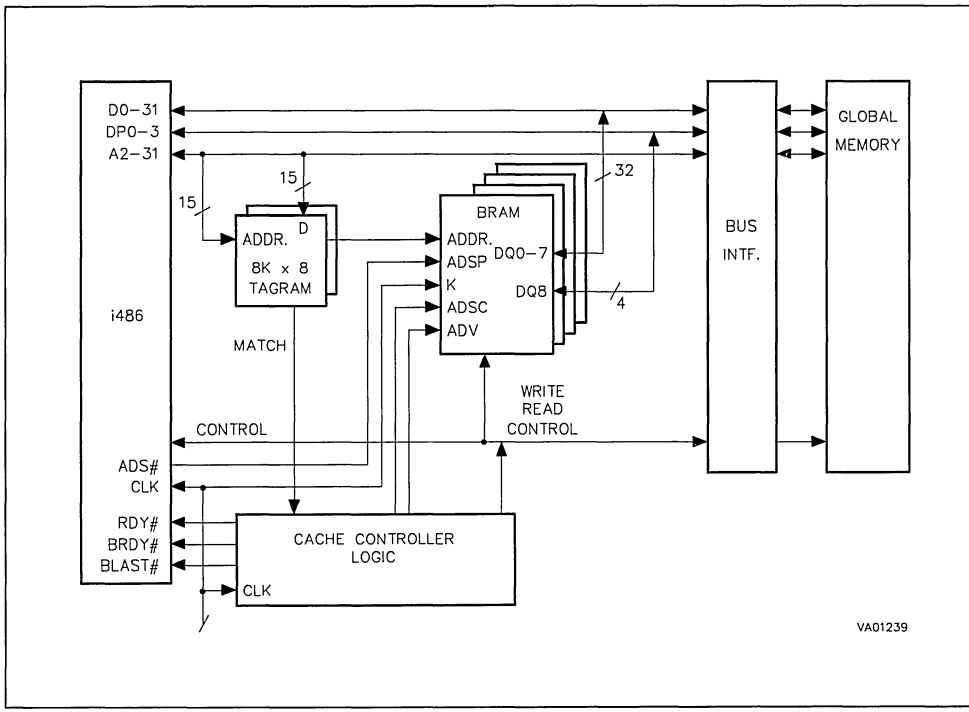
Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Table 7. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±1	µA
I_{CC1} [1]	Supply Current	$\overline{G}$ = V_{IH}, S0 = V_{IH}, $\overline{S1}$ = V_{IL}, All inputs = V_{IL} = 0V and V_{IH} ≥ 3V		160	mA
I_{CC2} [2]	Supply Current (Standby) TTL	S0 = V_{IL}, $\overline{S1}$ = V_{IH}		40	mA
I_{CC3} [3]	Supply Current (Standby) CMOS	S0 ≤ 0.2V, $\overline{S1}$ ≥ V_{CC} –0.2V		30	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{KHKH} minimum
2. All other Inputs at V_{IL} ≤ 0.8V or V_{IH} ≥ 2.2V
3. All other Inputs at V_{IL} ≤ 0.2V or V_{IH} ≥ V_{CC} – 0.2V

Figure 5. General 128K Byte Cache Block Diagram



DEVICE OPERATIONS (cont'd)

plex off-chip write pulse generation providing more flexibility for incoming signals.

The $\overline{ADV}$ input controls subsequent burst data accesses after the first data of the burst cycle is processed. Each time $\overline{ADV}$ is asserted low for subsequent bursts at the rising edge of the clock input, the burst counter is advanced to the next burst address sequence. The address is advanced before the operation. Wait states can be inserted during burst cycles by holding the $\overline{ADV}$ pin high during positive clock transitions. Upon completion of the full internal burst count, the address will wrap-around to its initial base address.

GENERAL APPLICATION

The MK62486 is organized using the ninth bit as the parity bit to support byte parity. Since the i486 processor provides on-board parity generation and checking, the ninth bit of the cache Burst SRAM can be passed to one of the DP0-DP3 pins of the microprocessor. Thus the MK62486 provides an architecture for building a 32K x 32bit burstable data cache SRAM array, with byte parity, by using four devices in a 128K byte cache application.

Table 8. Read and Write Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter	MK62486				Unit	Note
		19		24			
		Min.	Max.	Min.	Max.		
t_{KHKH}	Cycle Time	25		30		ns	
t_{KHQV}	Clock Access Time		19		24	ns	1
t_{KHKL}	Clock High Pulse Width	9.5		11		ns	
t_{KLKH}	Clock Low Pulse Width	9.5		11		ns	
t_{GLQV}	Output Enable Access Time		8		9	ns	1
t_{KHQX2}	Clock High to Output Hold Time	4		4		ns	1
t_{GLQX}	Output Enable to Output Active	0		0		ns	2
t_{KHQX1}	Clock High to Q Active (Low-Z)	4		4		ns	2
t_{KHQZ}	Clock High to Q High-Z		12		15	ns	2
t_{GHQZ}	Output Disable to Q High-Z		8		9	ns	2
t_{AVKH}	Address Set-up Time	3		3		ns	3
t_{ADSVKH}	Address Status Set-up Time	3		3		ns	3
t_{DVKH}	Data In Set-up Time	3		3		ns	3
t_{WVKH}	Write/Read Set-up Time	3		3		ns	3
t_{ADVVKH}	Address Advance Set-up Time	3		3		ns	3
t_{S0VKH}	Chip Select 0 (S0) Set-up Time	3		3		ns	3
t_{S1VKH}	Chip Select 1 ($\overline{S1}$) Set-up Time	3		3		ns	3
t_{KHAX}	Address Hold Time	2		2		ns	3
t_{KHADSX}	Address Status Hold Time	2		2		ns	3
t_{KHDX}	Data In Hold Time	2		2		ns	3
t_{KHWX}	Write/Read Hold Time	2		2		ns	3
t_{KHADVX}	Address Advance Hold Time	2		2		ns	3
t_{KHS0X}	Chip Select 0 (S0) Hold Time	2		2		ns	3
t_{KHS1X}	Chip Select 1 ($\overline{S1}$) Hold Time	2		2		ns	3

Notes: 1. C_L = 85pF (see Figure 4).
2. Transition is measured ± 500 mV from steady-stage voltage with C_L = 5pF (see Figure 4). This parameter is sampled and not 100 % tested.
3. This is a synchronous device requiring that all inputs must meet the specified set-up and hold times with stable logic levels for all rising edges of the clock input (K).

Figure 6. Non-Burst Read/Write 2-2 Cycles

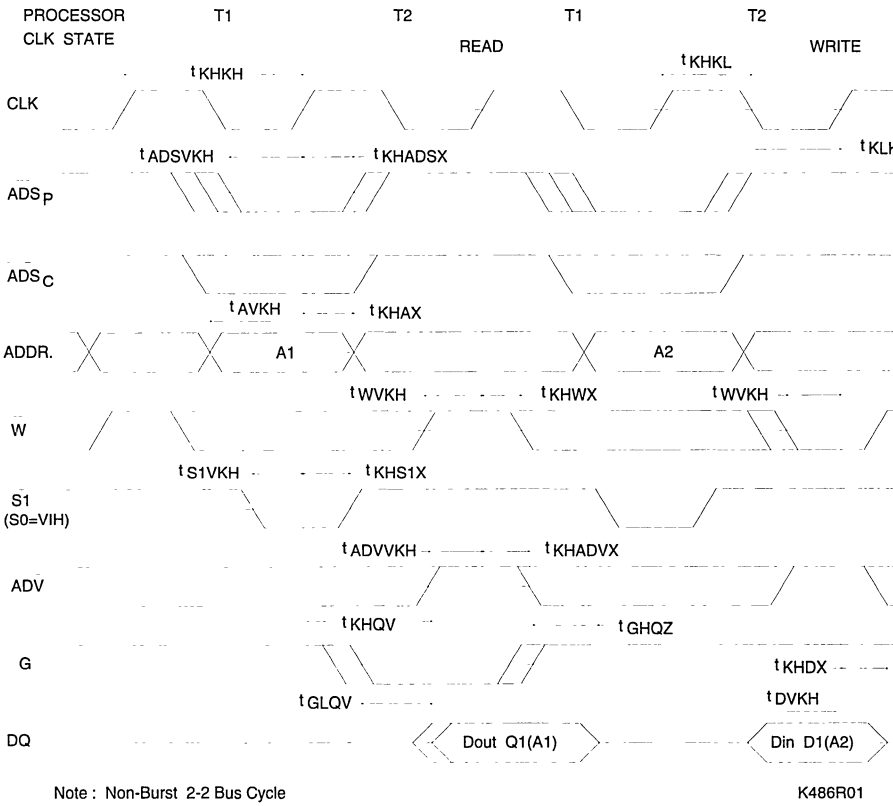


Figure 7. Burst Read Cycle

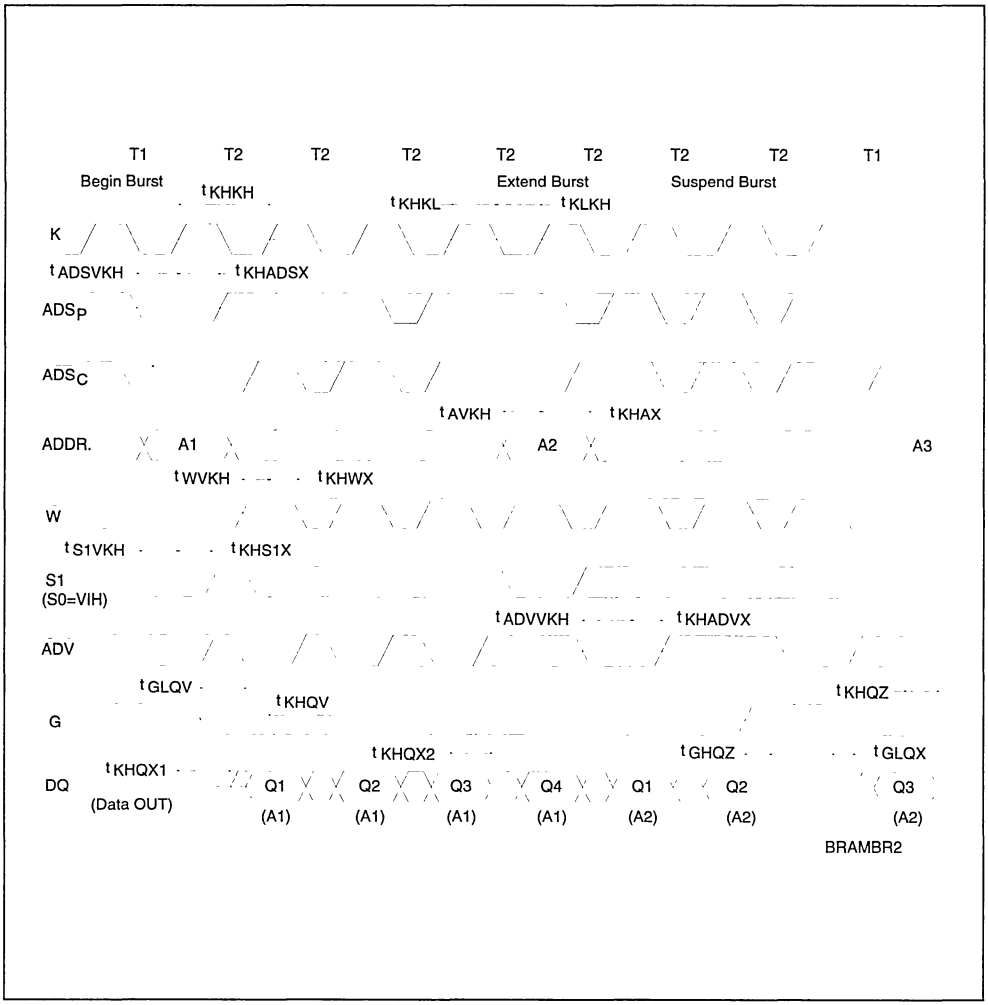


Figure 8. Burst Write Cycle

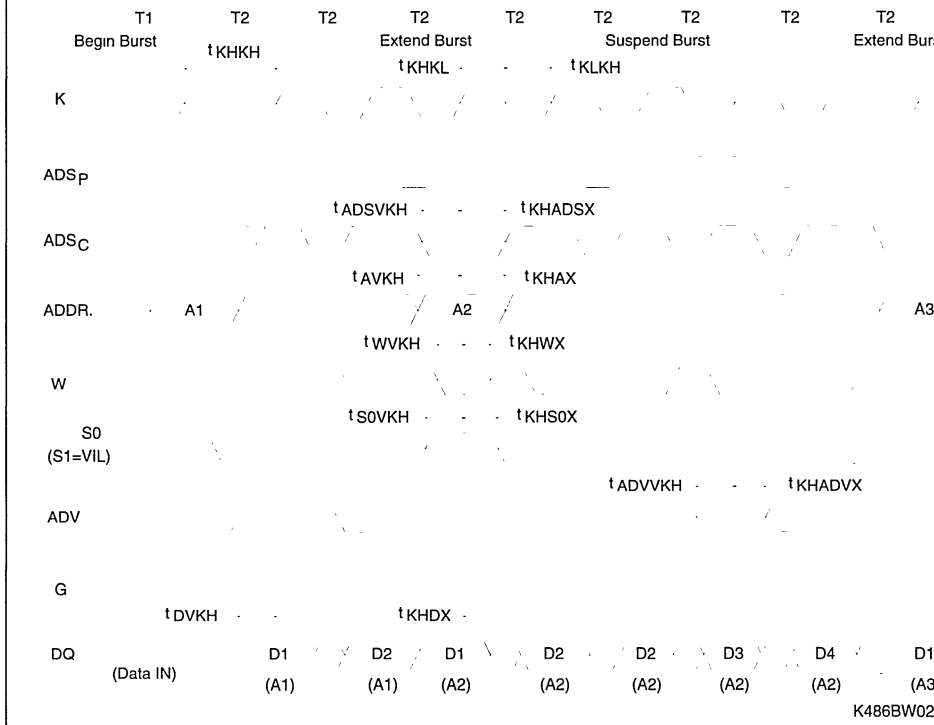
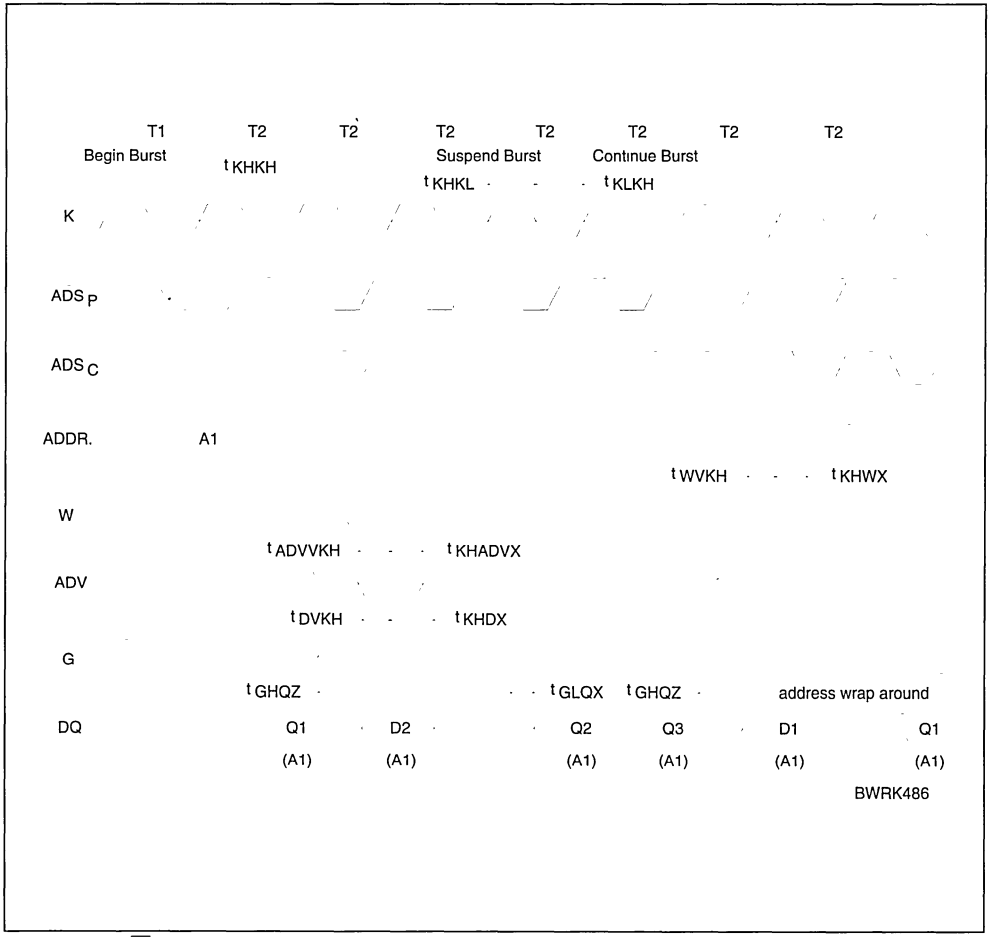
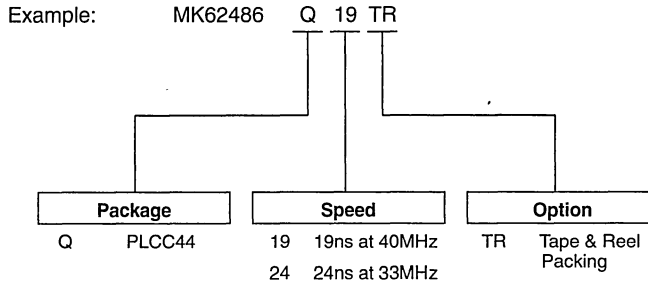


Figure 9. Combined Burst Read/Write Cycle



Note: SO = High, $\overline{S1}$ = Low.

ORDERING INFORMATION SCHEME



For a list of available options (Package, Speed, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

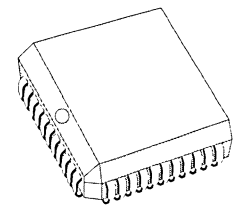
SGS-THOMSON MICROELECTRONICS

M62486A

VERY FAST CMOS 32K x 9 CACHE BRAM

ADVANCE DATA

- 32K x 9 CMOS SYNCHRONOUS BURST SRAM
- FAST CYCLE TIMES: 15, 20ns
- FAST ACCESS TIMES: 11, 12, 14ns Max
- ON-BOARD BURST COUNTER
- INPUT REGISTERS (ADDR.,DATA,CTRL)
- SELF-TIMED WRITE CYCLE
- THREE STATE COMMON I/O
- HIGH OUTPUT DRIVE CAPABILITY
- ASYNCHRONOUS OUTPUT ENABLE ($\overline{G}$)
- BURST CONTROL INPUTS: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$
- DUAL CHIP SELECTS for EASY DEPTH EXPANSION



PLCC44 (Q)

DESCRIPTION

The M62486A BRAM™ is a 288K (294,912 bit) CMOS Burst SRAM, organized as 32,768 words x 9 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology.

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ8	Data Inputs / Outputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0	Chip Select 0, Active High
$\overline{S1}$	Chip Select 1, Active Low
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Cache Controller
$\overline{ADV}$	Burst Address Advance
V_{CC}	Supply Voltage
GND	Ground
V_{CCQ}	Supply Voltage (DQ)
GND_Q	Ground (DQ)

Figure 1. Logic Diagram

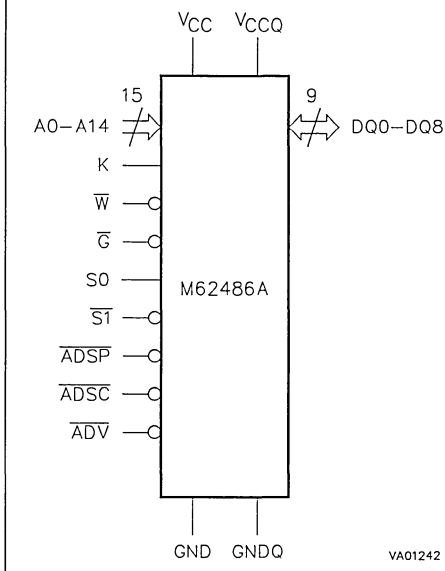
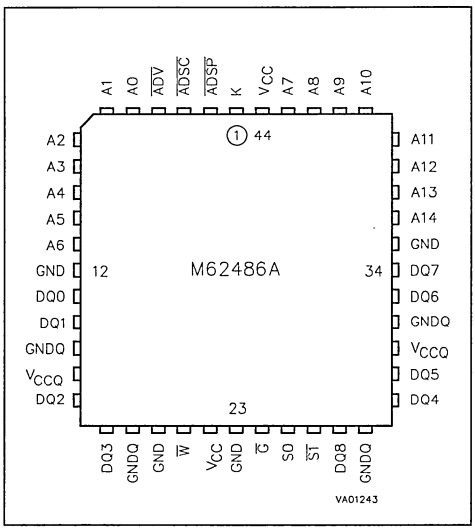


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.5 to 7	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (3)	Output Current	20	mA
P_D	Power Dissipation	1.2	W

Notes: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Up to a maximum operating V_{CC} of 5.5V only.
3 One output at a time, not to exceed 1 second duration

Figure 2. LCC Pin Connections



DESCRIPTION (cont'd)

The device integrates a 2-bit burst counter, input regis-ters, high output drive capability, and high speed synchronous SRAM onto a single chip. The synchronous design provides precise control using an external clock (K) input. The M62486A is specifically adapted to provide a burstable, high performance secondary cache for the i486® microprocessor. The M62486A is available in a 44 lead Plastic Leaded Chip Carrier package (PLCC).

The device provides multiple power and ground pins to reduce effects induced by output noise for high performance applications. Separate power and ground pins (V_{CCQ} and GND_Q) have been employed for DQ0-DQ8 to allow output levels referenced to 5V or 3.3V. For proper operation all GND and GND_Q pin must be connected to ground. $V_{CC} \geq V_{CCQ}$ at all times including power-up. The main Burst SRAM power requires a single 5V ± 5% supply, and all inputs and outputs are TTL compatible.

DEVICE OPERATIONS

Addresses (A0-A14), data inputs (DQ0-DQ8), and control signals, with exception of Output Enable ($\overline{G}$), are clock controlled inputs through non-inverting, pos-itive edge triggered registers. A cache burst address sequence can be initiated by either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) inputs, with subsequent burst addresses being internally generated by the Burst SRAM. The $\overline{ADV}$ input (burst address advance) provides control of the burst sequence, which imitates the i486 cache burst address sequence. Once a cache burst cycle begins, the subsequent burst address is generated internally each time the $\overline{ADV}$ input is asserted at the rising edge of the clock (K) input. The burst counter operates in the same manner for either cache burst write or read cycles.

The $\overline{ADSP}$ and the $\overline{ADSC}$ inputs control the start and the duration of the burst sequence respectively. Each time either address status input is asserted low, a new external base address is registered on the positive going edge of the clock (K).

Table 3. Asynchronous Truth Table

Mode	$\overline{G}$	DQ Status
Read	L	Data Out
Read	H	High-Z
Write[2]	X	Data In (High-Z)
Deselect	X	High-Z

Notes: 1. X = Don't Care.
2. For a cache write cycle following a read operation, $\overline{G}$ must be high before the input data required set-up time, and be held high through the input data hold time.

Table 4. Burst Count Sequence

External Address	A14-A2	A1	A0
1st Burst Address	A14-A2	A1	$\overline{A0}$
2nd Burst Address	A14-A2	$\overline{A1}$	A0
3rd Burst Address	A14-A2	$\overline{A1}$	$\overline{A0}$

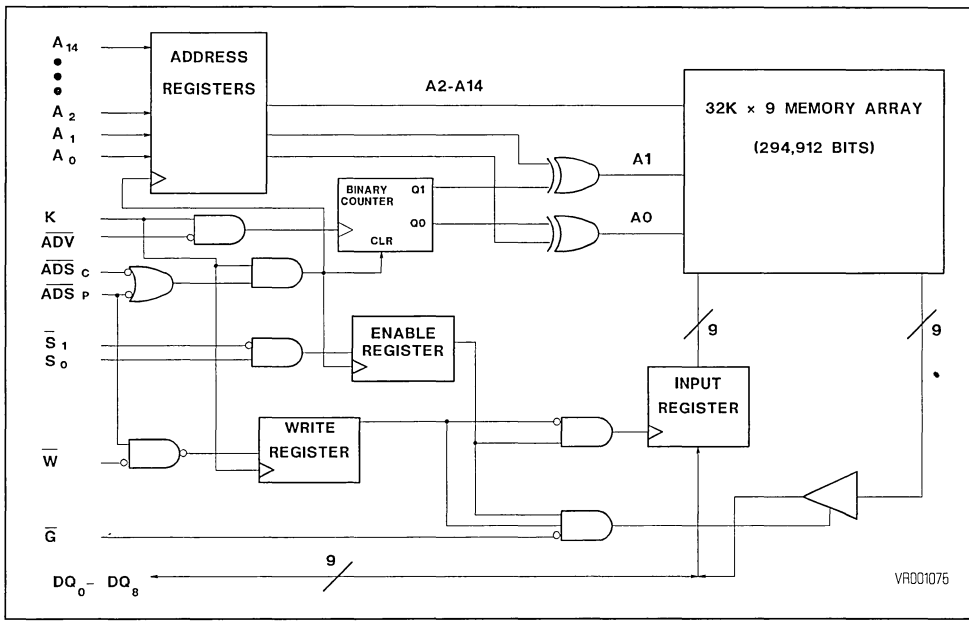
Note: The burst count sequence wraps around to the initial address after a full count is completed.

Table 5. Synchronous Truth Table

S0	$\overline{S1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K	Address	Operation
L	X	L	X	X	X	↑	N/A	Deselected
X	H	H	L	X	X	↑	N/A	Deselected
H	L	L	X	X	X	↑	External Base Address	Read Cycle - Begin Burst
H	L	H	L	X	L	↑	External Base Address	Write Cycle - Begin Burst
H	L	H	L	X	H	↑	External Base Address	Read Cycle - Begin Burst
X	X	H	H	L	L	↑	Advance Burst Address	Write Cycle - Continue Burst Sequence
X	X	H	H	L	H	↑	Advance Burst Address	Read Cycle - Continue Burst Sequence
X	X	H	H	H	L	↑	Hold Current Burst Address	Write Cycle - Suspend Burst Sequence
X	X	H	H	H	H	↑	Hold Current Burst • Address	Read Cycle - Suspend Burst Sequence

Notes: 1. X = Don't Care.
2. All inputs except $\overline{G}$ require set-up and hold times to the rising edge (low to high transition) of the external clock (K).
3. All read and write timings are referenced from $\overline{G}$ or K.
4. A read cycle is defined by $\overline{W}$ high or $\overline{ADSP}$ low for the required set-up and hold times. A write cycle is defined by $\overline{W}$ being asserted low for the set-up and hold times.
5. $\overline{G}$ is a don't care when $\overline{W}$ is registered low from the previous rising clock edge
6. Chip Selects must be true (S0 = high, $\overline{S1}$ = low) at each rising of the clock while $\overline{ADSP}$ or $\overline{ADSC}$ is asserted for the device to remain enabled, Chip Selects are registered whenever ADSP or ADSC is asserted low at the rising edge of the clock.

Figure 3. Block Diagram



DEVICE OPERATIONS (cont'd)

When $\overline{ADSP}$ is asserted low, any ongoing burst cycle is interrupted, and a read operation (independent of $\overline{W}$ and $\overline{ADSC}$) is performed at the new registered external base address. A new burst cycle is initiated each time $\overline{ADSP}$ is asserted. By asserting $\overline{ADSC}$ low, the present burst cycle (initiated by $\overline{ADSP}$) is interrupted and an extended burst read or write (depending upon the logic state of $\overline{W}$ at the rising edge of K) is performed at the new registered base address. Chip selects (S0 and $\overline{S1}$) are only sampled when a new base address is loaded. Therefore, the chip selects are registered when either address status input is asserted low at the rising edge of the clock (K), and remain latched internally until the next assertion of either $\overline{ADSP}$ or $\overline{ADSC}$. The M62486A Truth Tables and timing diagrams reference specific device operations.

It should be noted that the MK62486 allows a non-burst mode of operation where $\overline{ADSP}$ is the ADS# of the i486 processor in a 2-2 cycle mode of operation, and $\overline{ADSC}$ is held high during T2 (see Figure 5). However, the non-burst mode obviously negates the advantage of the internal burst counter for fast cache fill operations. In either mode (burst or non-burst), the write cycles are internally self-timed, and are initiated by the rising edge of the clock input. Self-timed write cycles eliminate com-

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

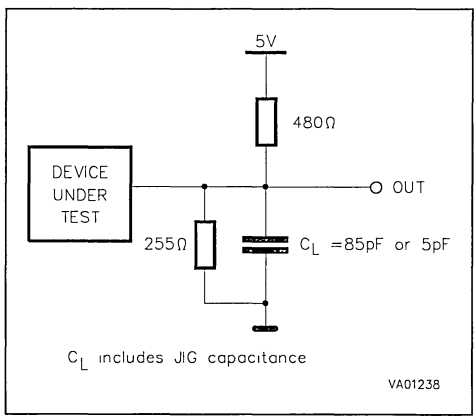


Table 6. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		5	pF
C_{OUT} [2]	Output Capacitance	V_{OUT} = 0V		10	pF

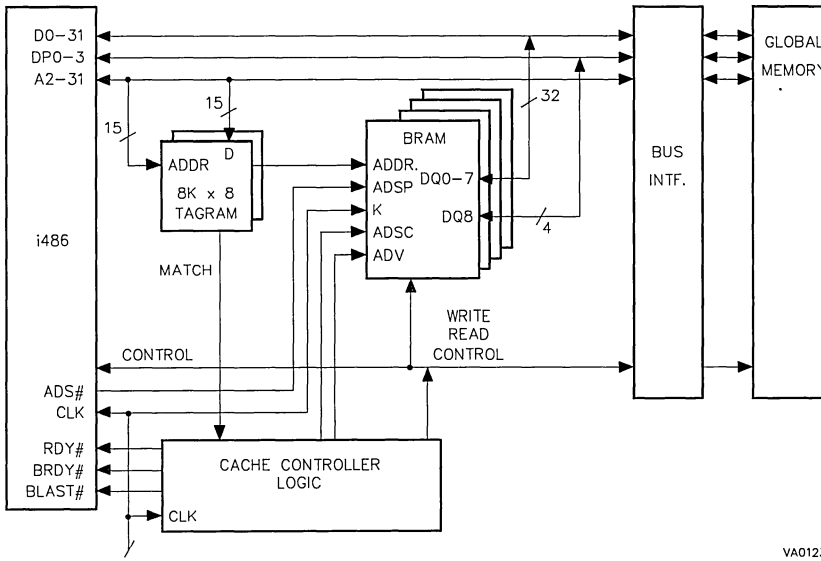
Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Table 7. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1} [1]	Supply Current	$\overline{G} = V_{IH}$, S0 = V_{IH}, $\overline{S1} = V_{IL}$, All inputs = V_{IL} = 0V and $V_{IH} \ge 3V$		180	mA
I_{CC2} [2]	Supply Current (Standby) TTL	S0 = V_{IL}, $\overline{S1} = V_{IH}$		40	mA
I_{CC3} [3]	Supply Current (Standby) CMOS	$S0 \le 0.2V$, $\overline{S1} \ge V_{CC} - 0.2V$		30	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{KHKH} minimum
2. All other Inputs at $V_{IL} \le 0.8V$ or $V_{IH} \ge 2.2V$
3. All other Inputs at $V_{IL} \le 0.2V$ or $V_{IH} \ge V_{CC} - 0.2V$

Figure 5. General 128K Byte Cache Block Diagram



DEVICE OPERATIONS (cont'd)

plex off-chip write pulse generation providing more flexibility for incoming signals.

The $\overline{ADV}$ input controls subsequent burst data accesses after the first data of the burst cycle is processed. Each time $\overline{ADV}$ is asserted low for subsequent bursts at the rising edge of the clock input, the burst counter is advanced to the next burst address sequence. The address is advanced before the operation. Wait states can be inserted during burst cycles by holding the $\overline{ADV}$ pin high during positive clock transitions. Upon completion of the full internal burst count, the address will wrap-around to its initial base address.

GENERAL APPLICATION

The M62486A is organized using the ninth bit as the parity bit to support byte parity. Since the i486 processor provides on-board parity generation and checking, the ninth bit of the cache Burst SRAM can be passed to one of the DP0-DP3 pins of the microprocessor. Thus the M62486A provides an architecture for building a 32K x 32bit burstable data cache SRAM array, with byte parity, by using four devices in a 128K byte cache application.

Table 8. Read and Write Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter	M62486A						Unit	Note
		11		12		14			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{KHKH}	Cycle Time	15		15		20		ns	
t_{KHQV}	Clock Access Time		11		12		14	ns	1
t_{KHKL}	Clock High Pulse Width	5.5		5.5		8		ns	
t_{KLKH}	Clock Low Pulse Width	5.5		5.5		8		ns	
t_{GLQV}	Output Enable Access Time		5		5		6	ns	1
t_{KHQX2}	Clock High to Output Hold Time	3		3		4		ns	1
t_{GLQX}	Output Enable to Output Active	0		0		0		ns	2
t_{KHQX1}	Clock High to Q Active (Low-Z)	4		4		4		ns	2
t_{KHQZ}	Clock High to Q High-Z		6		6		6	ns	2
t_{GHQZ}	Output Disable to Q High-Z		6		6		6	ns	2
t_{AVKH}	Address Set-up Time	2		2		3		ns	3
t_{ADSVKH}	Address Status Set-up Time	2		2		3		ns	3
t_{DVKH}	Data In Set-up Time	2		2		3		ns	3
t_{WVKH}	Write/Read Set-up Time	2		2		3		ns	3
t_{ADVVKH}	Address Advance Set-up Time	2		2		3		ns	3
t_{S0VKH}	Chip Select 0 (S0) Set-up Time	2		2		3		ns	3
t_{S1VKH}	Chip Select 1 ($\overline{S1}$) Set-up Time	2		2		3		ns	3
t_{KHAX}	Address Hold Time	2		2		2		ns	3
t_{KHADSX}	Address Status Hold Time	2		2		2		ns	3
t_{KHDX}	Data In Hold Time	2		2		2		ns	3
t_{KHWX}	Write/Read Hold Time	2		2		2		ns	3
t_{KHADVX}	Address Advance Hold Time	2		2		2		ns	3
t_{KHS0X}	Chip Select 0 (S0) Hold Time	2		2		2		ns	3
t_{KHS1X}	Chip Select 1 ($\overline{S1}$) Hold Time	2		2		2		ns	3

Notes: 1. C_L = 85pF (see Figure 4).
2. Transition is measured ± 500 mV from steady-stage voltage with C_L = 5pF (see Figure 4). This parameter is sampled and not 100 % tested
3. This is a synchronous device requiring that all inputs must meet the specified set-up and hold times with stable logic levels for all rising edges of the clock input (K).

Figure 6. Non-Burst Read/Write 2-2 Cycles

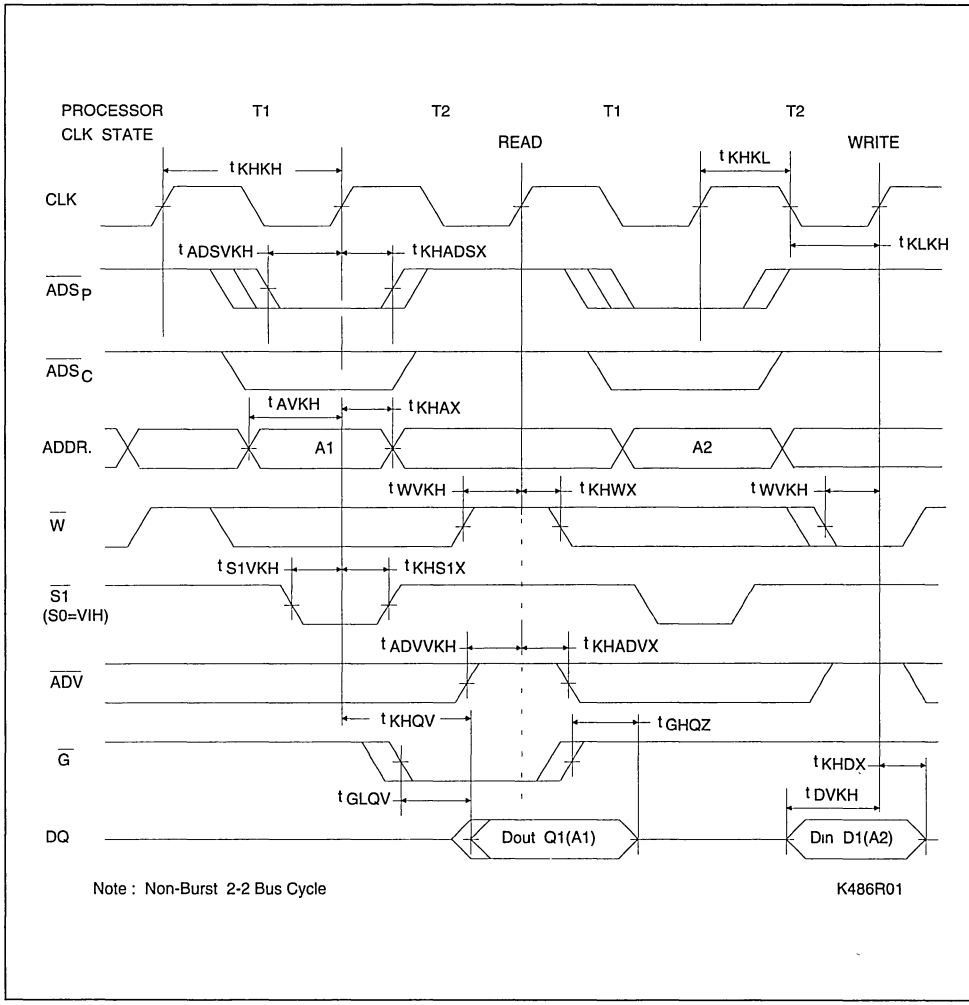


Figure 7. Burst Read Cycle

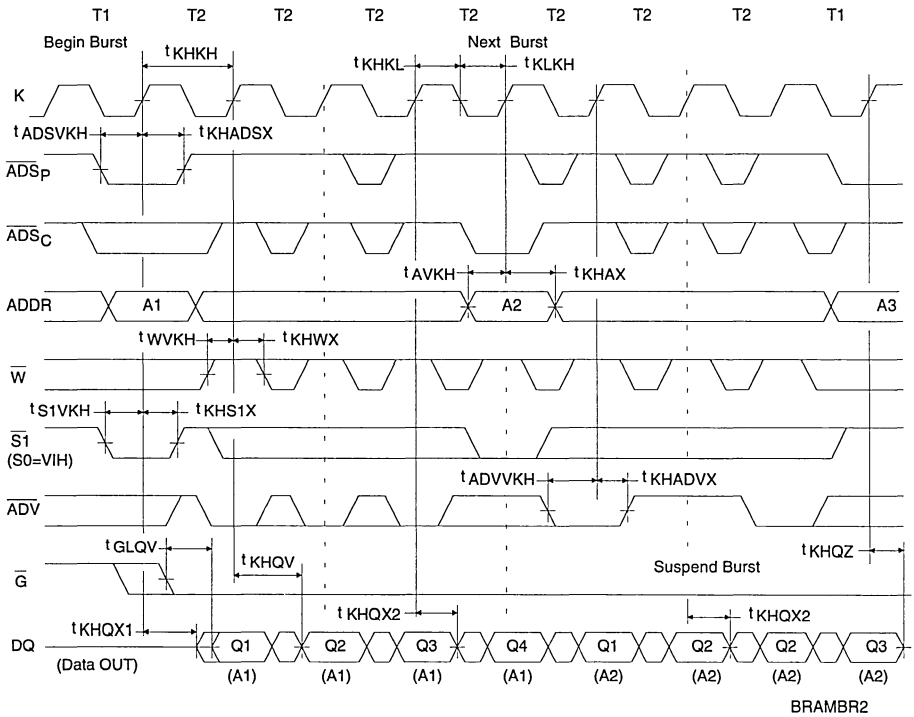


Figure 8. Burst Write Cycle

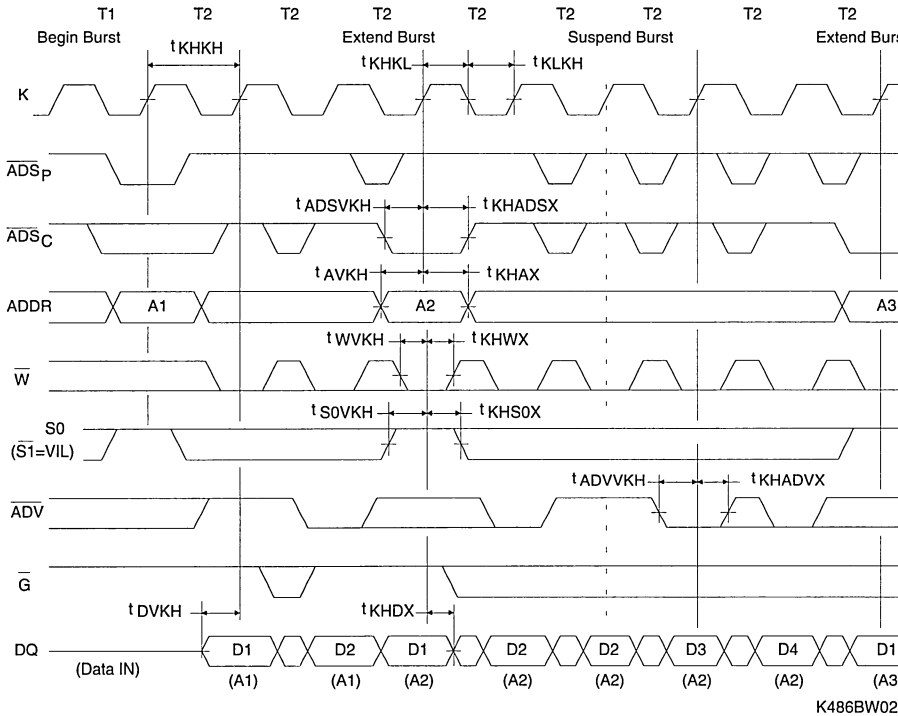
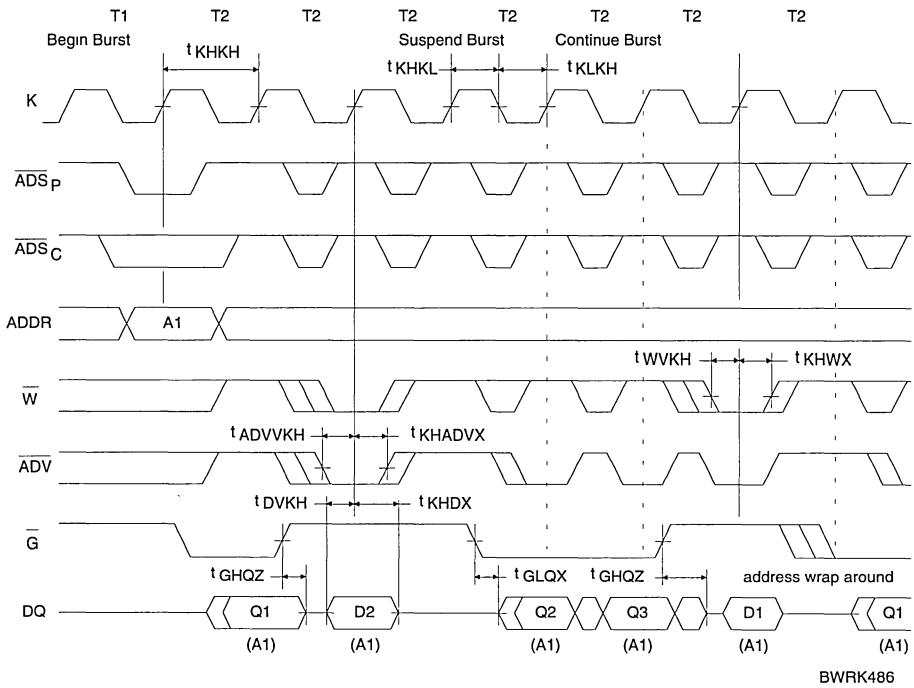
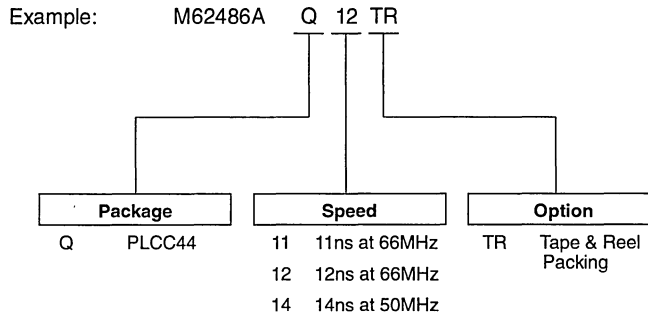


Figure 9. Combined Burst Read/Write Cycle



Note: SO = High, $\overline{S1}$ = Low.

ORDERING INFORMATION SCHEME



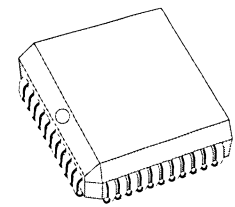
For a list of available options (Package, Speed, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

VERY FAST CMOS 32K x 9 CACHE BRAM

ADVANCE DATA

- 32K x 9 CMOS SYNCHRONOUS BURST SRAM
- FAST CYCLE TIME 15ns
- FAST ACCESS TIMES: 8, 9ns Max
- ON-BOARD BURST COUNTER
- INPUT REGISTERS (ADDR.,DATA,CTRL)
- SELF-TIMED WRITE CYCLE
- THREE STATE COMMON I/O
- HIGH OUTPUT DRIVE CAPABILITY
- ASYNCHRONOUS OUTPUT ENABLE ($\overline{G}$)
- BURST CONTROL INPUTS: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$
- DUAL CHIP SELECTS for EASY DEPTH EXPANSION
- OUTPUT REGISTERS for PIPE-LINE READ BURSTS



PLCC44 (Q)

DESCRIPTION

The M62486R BRAM™ is a 288K (294,912 bit) CMOS Burst SRAM, organized as 32,768 words x

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ8	Data Inputs / Outputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0	Chip Select 0, Active High
$\overline{S1}$	Chip Select 1, Active Low
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Cache Controller
$\overline{ADV}$	Burst Address Advance
V_{CC}	Supply Voltage
GND	Ground
V_{CCQ}	Supply Voltage (DQ)
GND_Q	Ground (DQ)

Figure 1. Logic Diagram

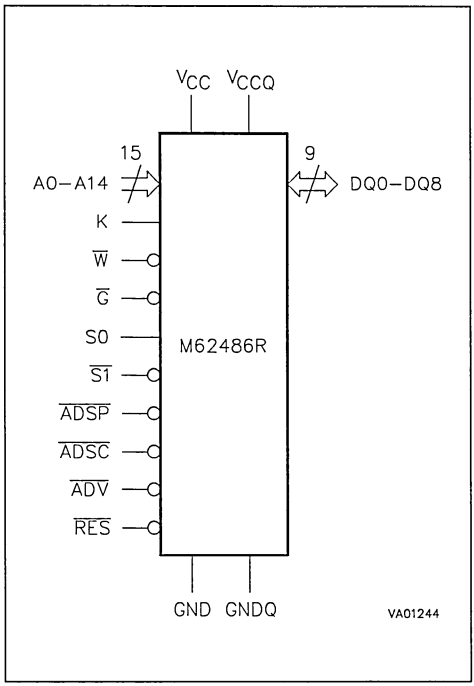
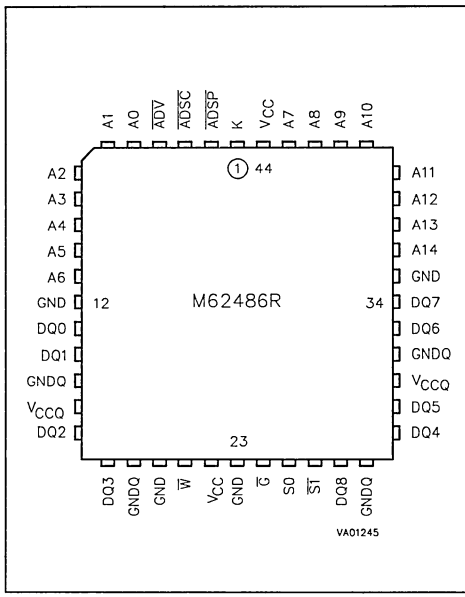


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.5 to 7	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (3)	Output Current	20	mA
P_D	Power Dissipation	1.2	W

Notes: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Up to a maximum operating V_{CC} of 5.5V only.
3. One output at a time, not to exceed 1 second duration.

Figure 2. LCC Pin Connections



DESCRIPTION (cont'd)

9 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology. The device integrates a 2-bit burst counter, input registers, high output drive capability, and high speed synchronous SRAM onto a single chip.

The synchronous design provides precise control using an external clock (K) input. The M62486R is specifically adapted to provide a burstable, high performance secondary cache for the i486® microprocessor. The M62486R is available in a 44 lead Plastic Leaded Chip Carrier package (PLCC). The device provides multiple power and ground pins to reduce effects induced by output noise for high performance applications. Separate power and ground pins (V_{CCQ} and GND_Q) have been employed for DQ0-DQ8 to allow output levels referenced to 5V or 3.3V. For proper operation all GND and GND_Q pin must be connected to ground. $V_{CC} \geq V_{CCQ}$ at all times including power-up.

The main Burst SRAM power requires a single 5V ± 5% supply, and all inputs and outputs are TTL compatible.

DEVICE OPERATIONS

Addresses (A0-A14), data inputs (DQ0-DQ8), and control signals, with exception of Output Enable ($\overline{G}$), are clock controlled inputs through non-inverting, pos-itive edge triggered registers. A cache burst address sequence can be initiated by either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) inputs, with subsequent burst addresses being internally generated by the Burst SRAM. The $\overline{ADV}$ input (burst address advance) provides control of the burst sequence, which imitates the i486 cache burst address sequence. Once a cache burst cycle begins, the subsequent burst address is generated internally each time the $\overline{ADV}$ input is asserted at the rising edge of the clock (K) input.

Table 3. Asynchronous Truth Table

Mode	$\overline{G}$	DQ Status
Read	L	Data Out
Read	H	High-Z
Write[2]	X	Data In (High-Z)
Deselect	X	High-Z

Notes: 1. X = Don't Care.
2. For a cache write cycle following a read operation, $\overline{G}$ must be high before the input data required set-up time, and be held high through the input data hold time.

Table 4. Burst Count Sequence

External Address	A14-A2	A1	A0
1st Burst Address	A14-A2	A1	$\overline{A0}$
2nd Burst Address	A14-A2	$\overline{A1}$	A0
3rd Burst Address	A14-A2	$\overline{A1}$	$\overline{A0}$

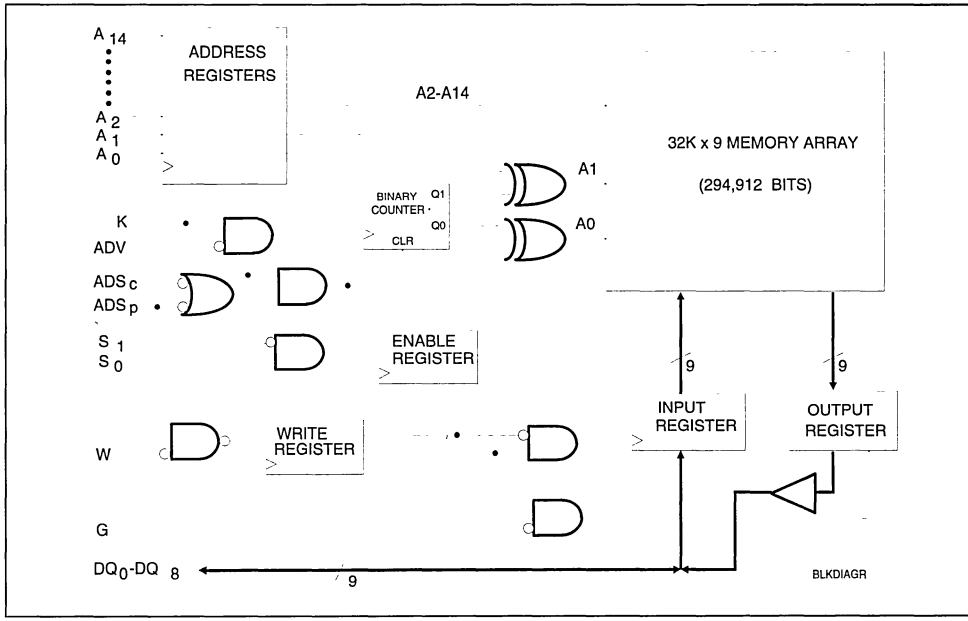
Note: The burst count sequence wraps around to the initial address after a full count is completed

Table 5. Synchronous Truth Table

S0	$\overline{S1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K	Address	Operation
L	X	L	X	X	X	↑	N/A	Deselected
X	H	H	L	X	X	↑	N/A	Deselected
H	L	L	X	X	X	↑	External Base Address	Read Cycle - Begin Burst
H	L	H	L	X	L	↑	External Base Address	Write Cycle - Begin Burst
H	L	H	L	X	H	↑	External Base Address	Read Cycle - Begin Burst
X	X	H	H	L	L	↑	Advance Burst Address	Write Cycle - Continue Burst Sequence
X	X	H	H	L	H	↑	Advance Burst Address	Read Cycle - Continue Burst Sequence
X	X	H	H	H	L	↑	Hold Current Burst Address	Write Cycle - Suspend Burst Sequence
X	X	H	H	H	H	↑	Hold Current Burst • Address	Read Cycle - Suspend Burst Sequence

Notes: 1. X = Don't Care.
2. All inputs except $\overline{G}$ require set-up and hold times to the rising edge (low to high transition) of the external clock (K).
3. All read and write timings are referenced from $\overline{G}$ or K.
4. A read cycle is defined by $\overline{W}$ high or $\overline{ADSP}$ low for the required set-up and hold times. A write cycle is defined by $\overline{W}$ being asserted low for the set-up and hold times.
5. $\overline{G}$ is a don't care when $\overline{W}$ is registered low from the previous rising clock edge
6. Chip Selects must be true (S0 = high, $\overline{S1}$ = low) at each rising of the clock while $\overline{ADSP}$ or $\overline{ADSC}$ is asserted for the device to remain enabled; Chip Selects are registered whenever ADSP or ADSC is asserted low at the rising edge of the clock.

Figure 3. Block Diagram



DEVICE OPERATIONS (cont'd)

The burst counter operates in the same manner for either cache burst write or read cycles. The $\overline{ADSP}$ and the $\overline{ADSC}$ inputs control the start and the duration of the burst sequence respectively. Each time either address status input is asserted low, a new external base address is registered on the positive going edge of the clock (K).

When $\overline{ADSP}$ is asserted low, any ongoing burst cycle is interrupted, and a read operation (independent of $\overline{W}$ and $\overline{ADSC}$) is performed at the new registered external base address. A new burst cycle is initiated each time $\overline{ADSP}$ is asserted. By asserting $\overline{ADSC}$ low, the present burst cycle (initiated by $\overline{ADSP}$) is interrupted and an extended burst read or write (depending upon the logic state of $\overline{W}$ at the rising edge of K) is performed at the new registered base address. Chip selects (S0 and $\overline{S1}$) are only sampled when a new base address is loaded. Therefore, the chip selects are registered when either address status input is asserted low at the rising edge of the clock (K), and remain latched internally until the next assertion of either $\overline{ADSP}$ or $\overline{ADSC}$. The M62486R Truth Tables and timing diagrams reference specific device operations.

It should be noted that the M62486R allows a non-burst mode of operation where $\overline{ADSP}$ is the ADS# of the i486 processor in a 2-2 cycle mode of

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

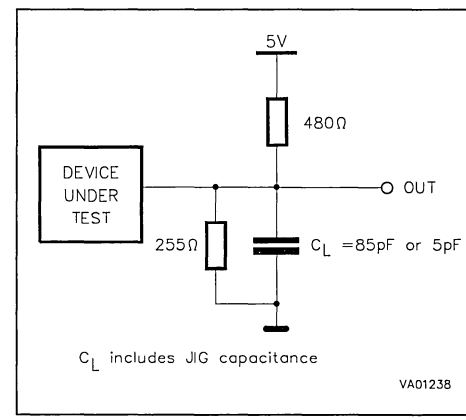


Table 6. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		5	pF
C_{OUT} [2]	Output Capacitance	V_{OUT} = 0V		10	pF

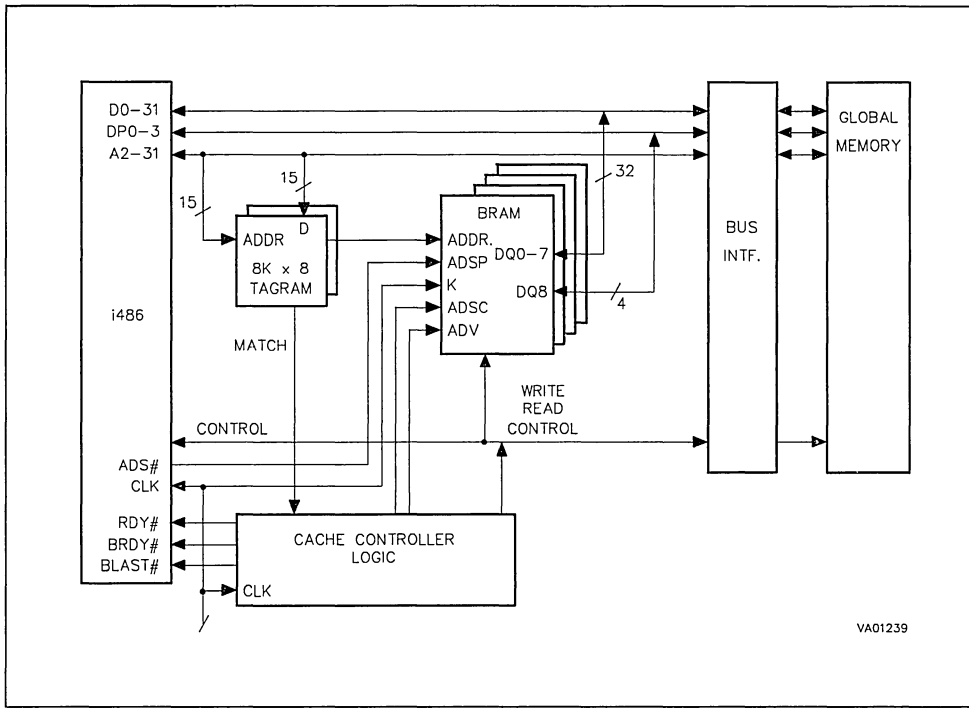
Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Table 7. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1} [1]	Supply Current	$\overline{G} = V_{IH}$, S0 = V_{IH}, $\overline{S1} = V_{IL}$, All inputs = V_{IL} = 0V and $V_{IH} \ge 3V$		180	mA
I_{CC2} [2]	Supply Current (Standby) TTL	S0 = V_{IL}, $\overline{S1} = V_{IH}$		40	mA
I_{CC3} [3]	Supply Current (Standby) CMOS	$S0 \le 0.2V$, $\overline{S1} \ge V_{CC} - 0.2V$		30	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{KHKH} minimum
2. All other Inputs at $V_{IL} \le 0.8V$ or $V_{IH} \ge 2.2V$
3. All other Inputs at $V_{IL} \le 0.2V$ or $V_{IH} \ge V_{CC} - 0.2V$

Figure 5. General 128K Byte Cache Block Diagram



DEVICE OPERATIONS (cont'd)

operation, and $\overline{ADSC}$ is held high during T2 (see Figure 5). However, the non-burst mode obviously negates the advantage of the internal burst counter for fast cache fill operations. In either mode (burst or non-burst), the write cycles are internally self-timed, and are initiated by the rising edge of the clock input. Self-timed write cycles eliminate complex off-chip write pulse generation providing more flexibility for incoming signals.

The $\overline{ADV}$ input controls subsequent burst data accesses after the first data of the burst cycle is processed. Each time $\overline{ADV}$ is asserted low for subsequent bursts at the rising edge of the clock input, the burst counter is advanced to the next burst address sequence. The address is advanced before the operation. Wait states can be inserted during burst cycles by holding the $\overline{ADV}$ pin high during positive clock transitions. Upon completion of the full internal burst count, the address will wrap-around to its initial base address.

GENERAL APPLICATION

The M62486R is organized using the ninth bit as the parity bit to support byte parity. Since the i486 processor provides on-board parity generation and checking, the ninth bit of the cache Burst SRAM can be passed to one of the DP0-DP3 pins of the microprocessor. Thus the M62486R provides an architecture for building a 32K x 32bit burstable data cache SRAM array, with byte parity, by using four devices in a 128K byte cache application.

Table 8. Read and Write Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter	M62486R				Unit	Note
		8		9			
		Min.	Max.	Min.	Max.		
t_{KHKH}	Cycle Time	15		15		ns	
t_{KHQV}	Clock Access Time		8		9	ns	1
t_{KHKL}	Clock High Pulse Width	5.5		5.5		ns	
t_{KLKH}	Clock Low Pulse Width	5.5		5.5		ns	
t_{GLQV}	Output Enable Access Time		5		6	ns	1
t_{KHQX2}	Clock High to Output Hold Time	2		2		ns	1
t_{GLQX}	Output Enable to Output Active	0		0		ns	2
t_{KHQX1}	Clock High to Q Active (Low-Z)	3		3		ns	2
t_{KHQZ}	Clock High to Q High-Z		6		6	ns	2
t_{GHQZ}	Output Disable to Q High-Z		6		6	ns	2
t_{AVKH}	Address Set-up Time	2		2		ns	3
t_{ADSVKH}	Address Status Set-up Time	2		2		ns	3
t_{DVKH}	Data In Set-up Time	2		2		ns	3
t_{WVKH}	Write/Read Set-up Time	2		2		ns	3
t_{ADVVKH}	Address Advance Set-up Time	2		2		ns	3
t_{S0VKH}	Chip Select 0 (S0) Set-up Time	2		2		ns	3
t_{S1VKH}	Chip Select 1 ($\overline{S1}$) Set-up Time	2		2		ns	3
t_{KHAX}	Address Hold Time	2		2		ns	3
t_{KHADSX}	Address Status Hold Time	2		2		ns	3
t_{KHDX}	Data In Hold Time	2		2		ns	3
t_{KHWX}	Write/Read Hold Time	2		2		ns	3
t_{KHADVX}	Address Advance Hold Time	2		2		ns	3
t_{KHS0X}	Chip Select 0 (S0) Hold Time	2		2		ns	3
t_{KHS1X}	Chip Select 1 ($\overline{S1}$) Hold Time	2		2		ns	3

Notes: 1. C_L = 85pF (see Figure 4).
2. Transition is measured ± 500 mV from steady-stage voltage with C_L = 5pF (see Figure 4). This parameter is sampled and not 100 % tested.
3. This is a synchronous device requiring that all inputs must meet the specified set-up and hold times with stable logic levels for all rising edges of the clock input (K).

Figure 6. Non-Burst Read/Write Cycles

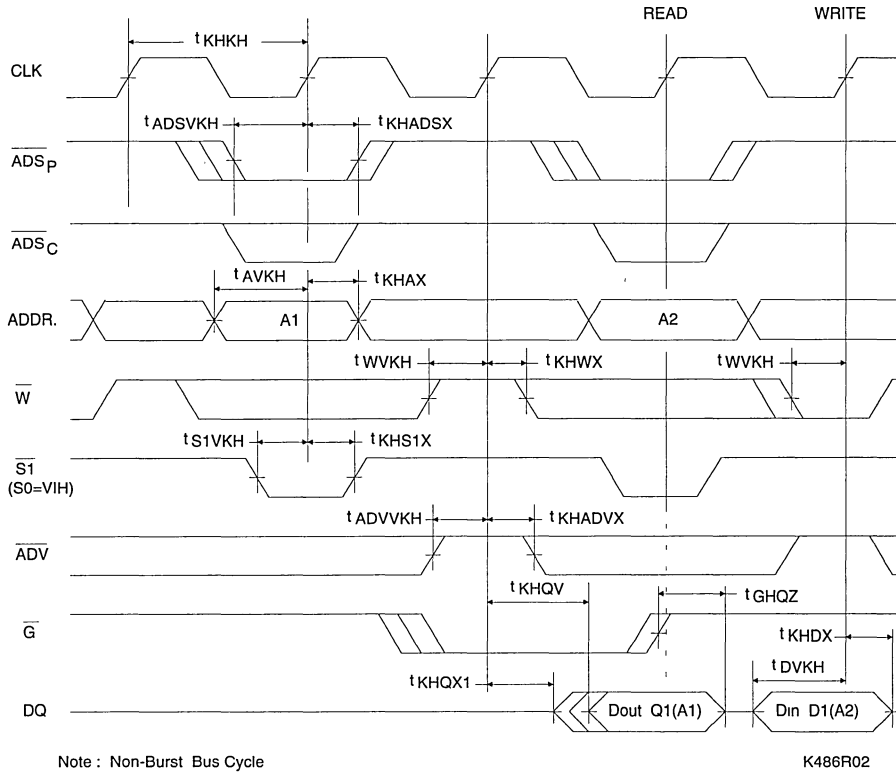


Figure 7. Burst Read Cycle

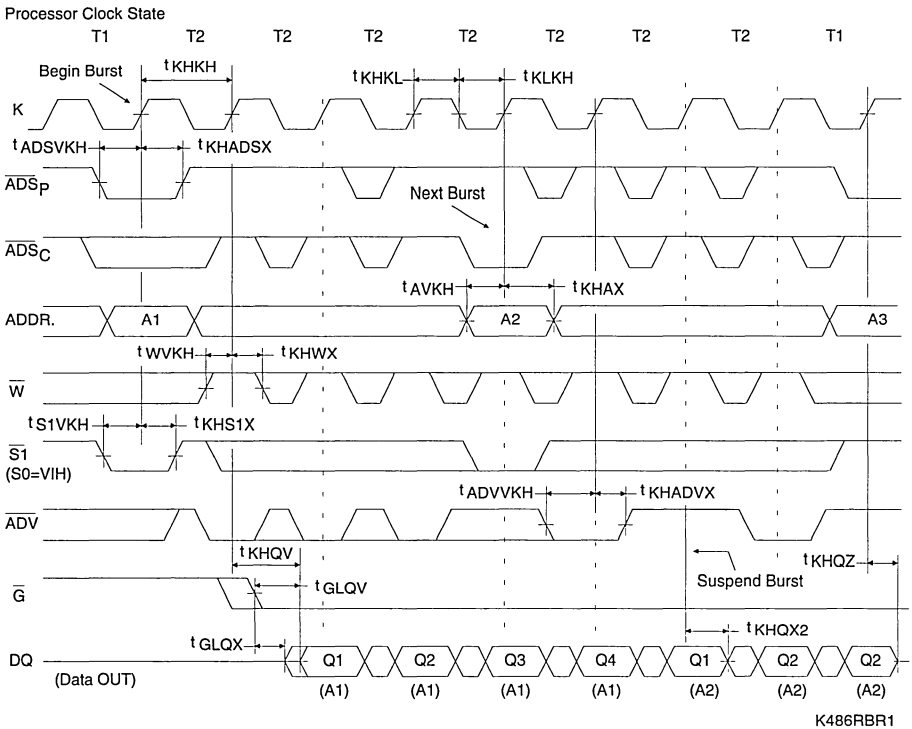


Figure 8. Burst Write Cycle

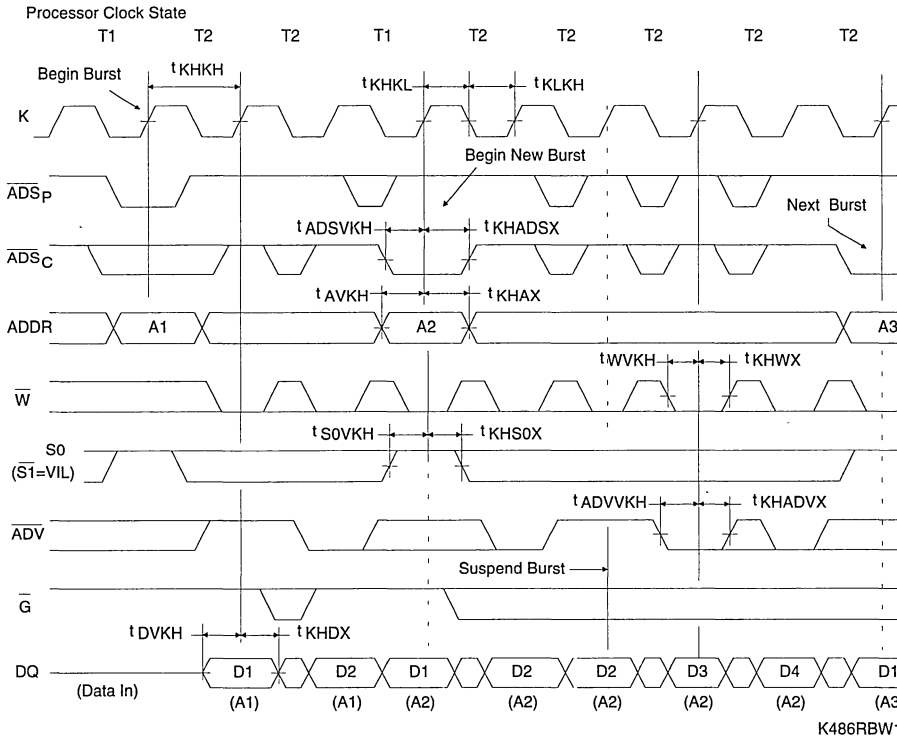
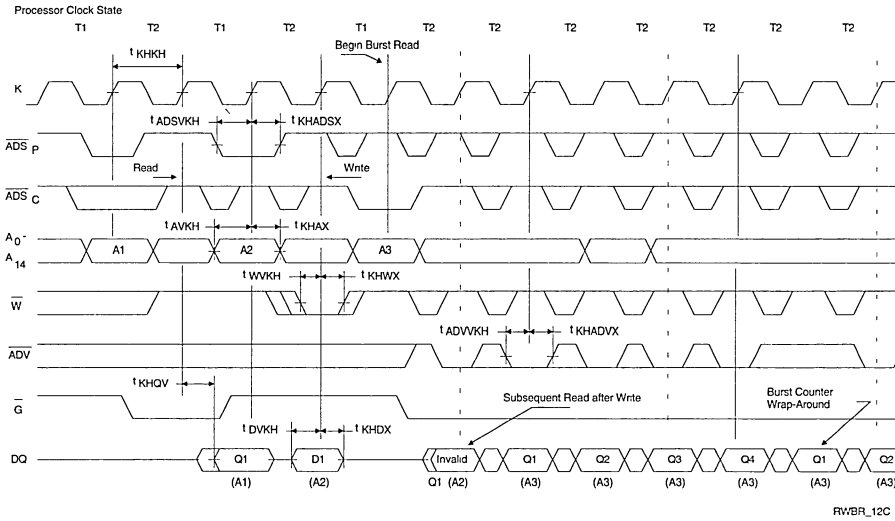
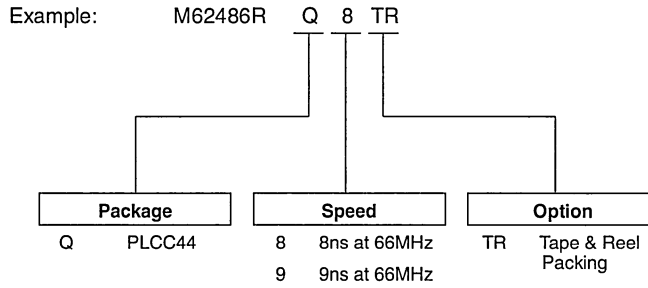


Figure 9. Combined Burst Read/Write Cycle



ORDERING INFORMATION SCHEME

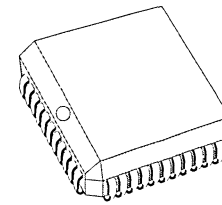


For a list of available options (Package, Speed, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

VERY FAST CMOS 32K x 9 CACHE BRAM

- 32K x 9 CMOS SYNCHRONOUS BURST SRAM
- FAST CYCLE TIMES: 25, 30ns
- FAST ACCESS TIMES: 19, 24ns Max
- ON-BOARD BURST COUNTER
- INPUT REGISTERS (ADDR.,DATA,CTRL)
- SELF-TIMED WRITE CYCLE
- THREE STATE COMMON I/O
- ASYNCHRONOUS OUTPUT ENABLE ($\overline{G}$)
- BURST CONTROL INPUTS: $\overline{TSP}$, $\overline{TSC}$, $\overline{BAA}$
- DUAL CHIP SELECTS for EASY DEPTH EXPANSION



PLCC44 (Q)

DESCRIPTION

The MK62940 BRAM™ is a 288K (294,912 bit) CMOS Burst SRAM, organized as 32,768 words x 9 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology. The device integrates a 2-bit burst counter, input registers, high output drive capability, and high speed

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ8	Data Inputs / Outputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0	Chip Select 0, Active High
$\overline{S1}$	Chip Select 1, Active Low
$\overline{TSP}$	Address Start Processor
$\overline{TSC}$	Address Start Cache Controller
$\overline{BAA}$	Burst Address Advance
RES	Reserve, Tied High
V_{CC}	Supply Voltage
GND	Ground

Figure 1. Logic Diagram

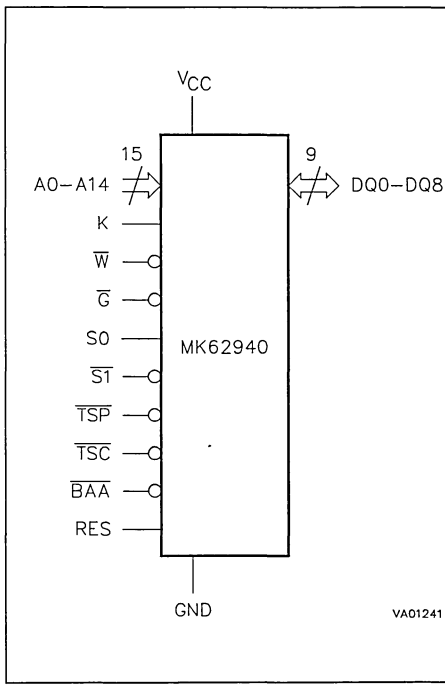
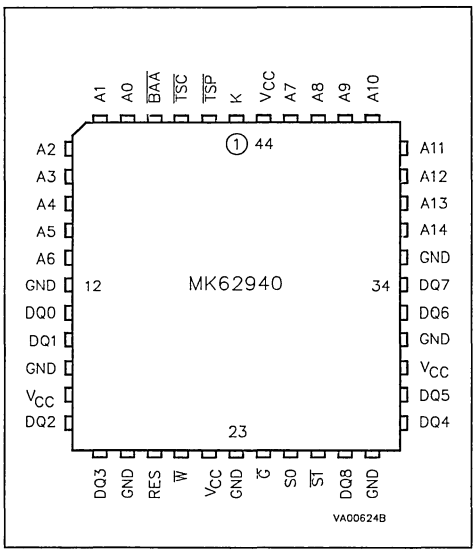


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.5 to 7	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (3)	Output Current	20	mA
P_D	Power Dissipation	1.2	W

Notes: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Up to a maximum operating V_{CC} of 5.5V only.
3. One output at a time, not to exceed 1 second duration.

Figure 2. LCC Pin Connections



DESCRIPTION (cont'd)

synchronous SRAM onto a single chip. The synchronous design provides precise control using an external clock (K) input. The MK62940 is specifically adapted to provide a burstable, high performance secondary cache for the MC68040 microprocessor. The device is pin compatible and functional equivalent to the Motorola MCM62940, but employs a single power supply design.

The MK62940 is available in a 44 lead Plastic Leaded Chip Carrier package (PLCC). The device provides multiple power and ground pins to reduce effects induced by output noise for high performance applications.

The main Burst SRAM power (V_{CC}) requires a single 5V ± 5% supply, and all inputs and outputs are TTL compatible.

DEVICE OPERATION

Addresses (A0-A14), data inputs (DQ0-DQ8), and control signals, with exception of Output Enable ($\overline{G}$) are clock controlled inputs through non-inverting, positive edge triggered registers. A cache burst address sequence can be initiated by either $\overline{TSP}$ (Transfer Start Processor) or $\overline{TSC}$ (Transfer Start Cache Controller) inputs, with subsequent burst addresses being internally generated by the Burst SRAM. The $\overline{BAA}$ input (Burst Address Advance) provides control of the burst sequence, which imitates the required MC68040 cache burst address sequence. A cache burst cycle begins by loading the internal counter with the present values of A1 and A0. Thereafter, subsequent burst addresses are generated internally. The burst counter operates in the same manner for either cache burst write or read cycles.

The $\overline{TSP}$ and the $\overline{TSC}$ inputs control the start of the burst sequence. When either $\overline{TSx}$ is asserted low at the rising edge of the clock, any ongoing burst cycle is interrupted and a new external base address is registered. Chip selects (S0 and $\overline{S1}$) are only sampled when a new base address is loaded.

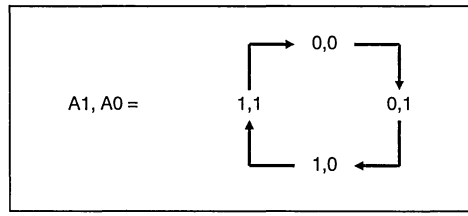
Therefore, the chip selects are registered when either transfer start input is asserted low at the

Table 3. Asynchronous Truth Table

Mode	$\overline{G}$	DQ Status
Read	L	Data Out
Read	H	High-Z
Write[2]	X	High-Z
Write[2]	X	Data In
Deselect	X	High-Z

Note: 1. X = Don't Care.
2. For a cache write cycle following a read operation, $\overline{G}$ must be high before the input data required set-up time, and be held high through the input data hold time.

Figure 3. Burst Count Sequence



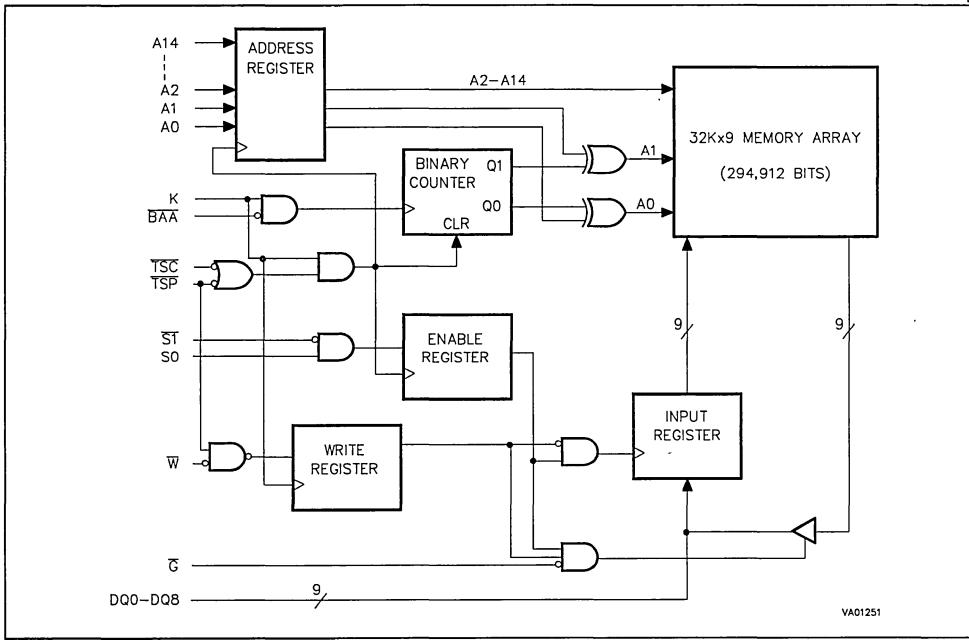
Note: The external values for A1, A0 are the starting point for the burst sequence graph. The burst counter will internally advance A1 and A0 as shown. After the counter reaches a full count from the initial value, the address will wrap around.

Table 4. Synchronous Truth Table

S0	$\overline{S1}$	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{W}$	K	Address	Operation
L	X	L	X	X	X	↑	N/A	Deselected
X	H	H	L	X	X	↑	N/A	Deselected
H	L	L	X	X	X	↑	External Base Address	Read Cycle - Begin Burst
H	L	H	L	X	L	↑	External Base Address	Write Cycle - Extend Burst
H	L	H	L	X	H	↑	External Base Address	Read Cycle - Extend Burst
X	X	H	H	L	L	↑	Advance Burst Address	Write Cycle - Continue Burst Sequence
X	X	H	H	L	H	↑	Advance Burst Address	Reade Cycle - Continue Burst Sequence
X	X	H	H	H	L	↑	Hold Current Burst Address	Write Cycle - Suspend Burst Sequence
X	X	H	H	H	H	↑	Hold Current Burst Address	Read Cycle - Suspend Burst Sequence

Notes: 1. X = Don't Care.
2. All inputs except $\overline{G}$ require set-up and hold times to the rising edge (low to high transition) of the external clock (K).
3. All read and write timings are referenced from $\overline{G}$ or K.
4. A read cycle is defined by $\overline{W}$ high or $\overline{TSP}$ low for the required set-up and hold times. A write cycle is defined by $\overline{W}$ being asserted low for the set-up and hold times.
5. $\overline{G}$ is a don't care when $\overline{W}$ is registered low from the previous rising clock edge.
6. Chip Selects must be true (S0 = high, S1 = low) at each rising of the clock while $\overline{TSP}$ or $\overline{TSC}$ is asserted for the device to remain enable; Chip Selects are registered whenever $\overline{TSP}$ or $\overline{TSC}$ is asserted low at the rising edge of the clock.
7. Chip Selects must be true (S0 = high, $\overline{S1}$ = low) at each rising of the clock while $\overline{TSP}$ or $\overline{TSC}$ is asserted for the the device to remain enabled; Chip Selects are registered whenever $\overline{TSP}$ or $\overline{TSC}$ is asserted low at the rising edge of the clock.

Figure 4. Block Diagram



DEVICE OPERATIONS (cont'd)

rising edge of the clock (K), and remain latched internally until the next assertion of either $\overline{TSP}$ or $\overline{TSC}$. The MK62940 Truth Tables and timing diagrams reference specific device operations.

It should be noted that the MK62940 allows a non-burst mode of operation where $\overline{TSP}$ is the $\overline{TS}$ pin of the MC68040 processor in a typical 2 clock cycle mode of operation, and $\overline{TSC}$ is held high during C2 (see Figure 7). However, the non-burst mode obviously negates the advantage of the internal burst counter for fast cache fill operations. In either mode (burst or non-burst), the write cycles are internally self-timed, and are initiated by the rising edge of the clock input when $\overline{W}$ is low.

The $\overline{BAA}$ input controls subsequent burst data accesses after the first data of the burst cycle is processed. Each time $\overline{BAA}$ is asserted low for subsequent bursts at the rising edge of the clock input, the burst counter is advanced to the next burst address sequence. The address is advanced from the rising edge of K. Wait states can be inserted during burst cycles by holding the $\overline{BAA}$ pin high during positive clock transitions. Upon completion of the full internal burst count, the address will wrap-around to its initial base address.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Load Circuit

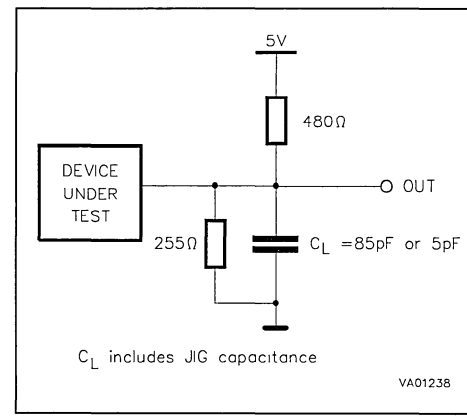


Table 5. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		5	pF
C_{OUT} [2]	Output Capacitance	V_{OUT} = 0V		10	pF

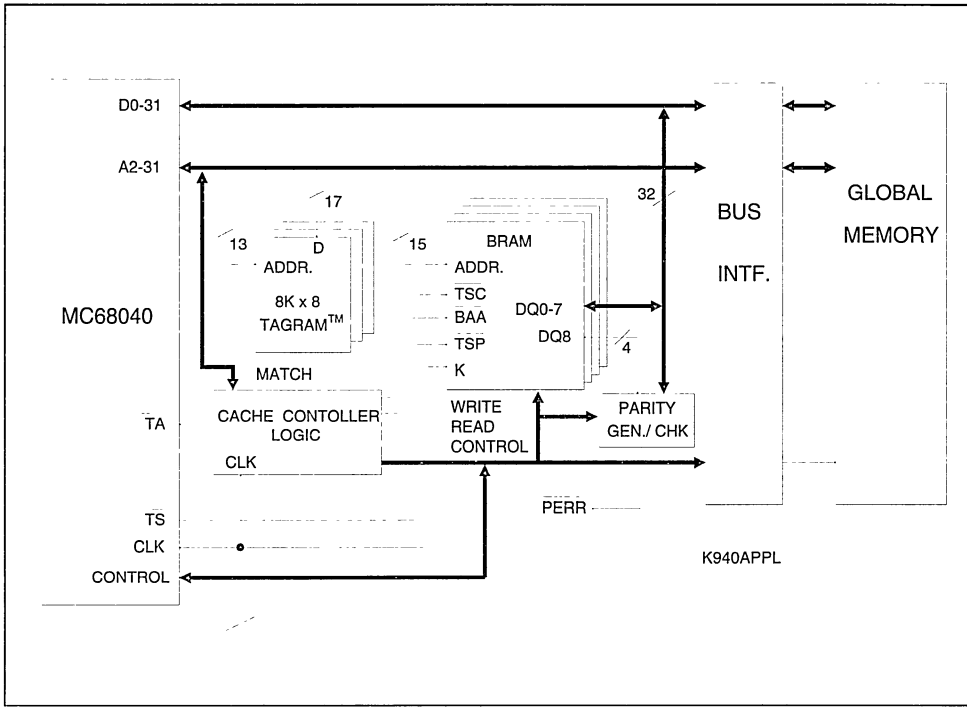
Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Table 6. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±1	µA
I_{CC1} [1]	Supply Current	$\overline{G}$ = V_{IH}, S0 = V_{IH}, $\overline{S1}$ = V_{IL}, All inputs = V_{IL} = 0V and V_{IH} ≥ 3V		160	mA
I_{CC2} [2]	Supply Current (Standby) TTL	S0 = V_{IL}, $\overline{S1}$ = V_{IH}		40	mA
I_{CC3} [3]	Supply Current (Standby) CMOS	S0 ≤ 0.2V, $\overline{S1}$ ≥ V_{CC} –0.2V		30	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{KHKH} minimum
2. All other Inputs at V_{IL} ≤ 0.8V or V_{IH} ≥ 2.2V
3. All other Inputs at V_{IL} ≤ 0.2V or V_{IH} ≥ V_{CC} – 0.2V

Figure 6. General 128K Byte Cache Block Diagram



GENERAL APPLICATION

The MK62940 is organized as 32K x 9 bit words to support byte parity. By incorporating TAGRAM™ with a 15 bit tag field and a 15 bit index address, a cache address scheme of 30 bits is monitiored. The TAGRAM in addtion to the MK62940 provides an architecture for building a 32K x 32 bit burstable data cache SRAM array, with byte parity, by using four devices in a 128K byte cache application.

Table 7. Read and Write Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter	MK62940				Unit	Note
		19		24			
		Min.	Max.	Min.	Max.		
t_{KHKH}	Cycle Time	25		30		ns	
t_{KHQV}	Clock Access Time		19		24	ns	1
t_{KHKL}	Clock High Pulse Width	9.5		11		ns	
t_{KLKH}	Clock Low Pulse Width	9.5		11		ns	
t_{GLQV}	Output Enable Access Time		8		9	ns	1
t_{KHQX2}	Clock High to Output Hold Time	4		4		ns	2
t_{KHQX1}	Clock High to Output Active	4		4		ns	2
t_{GLQX}	Output Enable to Output Active	0		0		ns	2
t_{KHQZ}	Clock High to Q High-Z		12		15	ns	2
t_{GHQZ}	Output Disable to Q High-Z		8		9	ns	2
t_{AVKH}	Address Set-up Time	3		3		ns	3
t_{TSVKH}	Transfer Start Set-up Time	3		3		ns	3
t_{DVKH}	Data In Set-up Time	3		3		ns	3
t_{SWVKH}	Write/Read Set-up Time	3		3		ns	3
t_{BAVKH}	Burst Address Advance Set-up Time	3		3		ns	3
t_{S0VKH}	Chip Select 0 (S0) Set-up Time	3		3		ns	3
t_{S1VKH}	Chip Select 1 ($\overline{S1}$) Set-up Time	3		3		ns	3
t_{KHAX}	Address Hold Time	2		2		ns	3
t_{KHTSX}	Transfer Start Hold Time	2		2		ns	3
t_{KHDX}	Data In Hold Time	2		2		ns	3
t_{KHWX}	Write/Read Hold Time	2		2		ns	3
t_{KHBAX}	Burst Address Advance Hold Time	2		2		ns	3
t_{KHWX}	Asynchronous Write ($\overline{AW}$) Hold Time	2		2		ns	3
t_{KHS0X}	Chip Select 0 (S0) Hold Time	2		2		ns	3
t_{KHS1X}	Chip Select 1 ($\overline{S1}$) Hold Time	2		2		ns	3

Notes: 1. C_L = 85pF (see Figure 5).
2. Transition is measured ± 500 mV from steady-stage voltage with C_L = 5pF (see Figure 5). This parameter is sampled and not 100 % tested.
3. This is synchronous device requiring that all inputs must meet the specified set-up and hold times with stable logic levels for all rising edges of the clock input (K)

Figure 7. Typical Non-Burst Read/Write Cycles

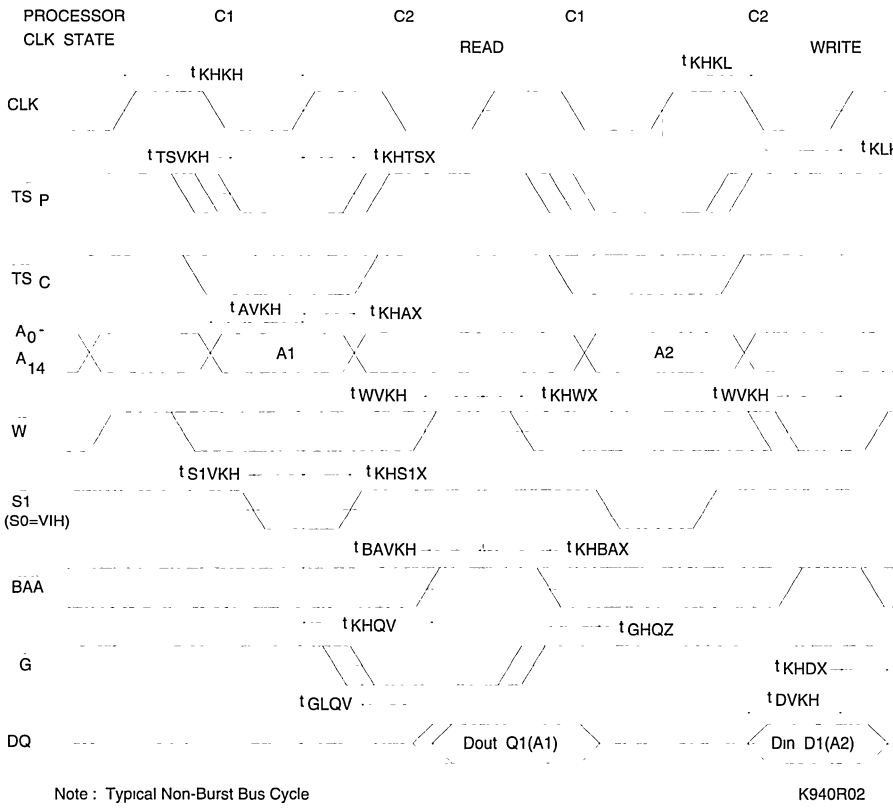


Figure 8. Burst Read Cycle

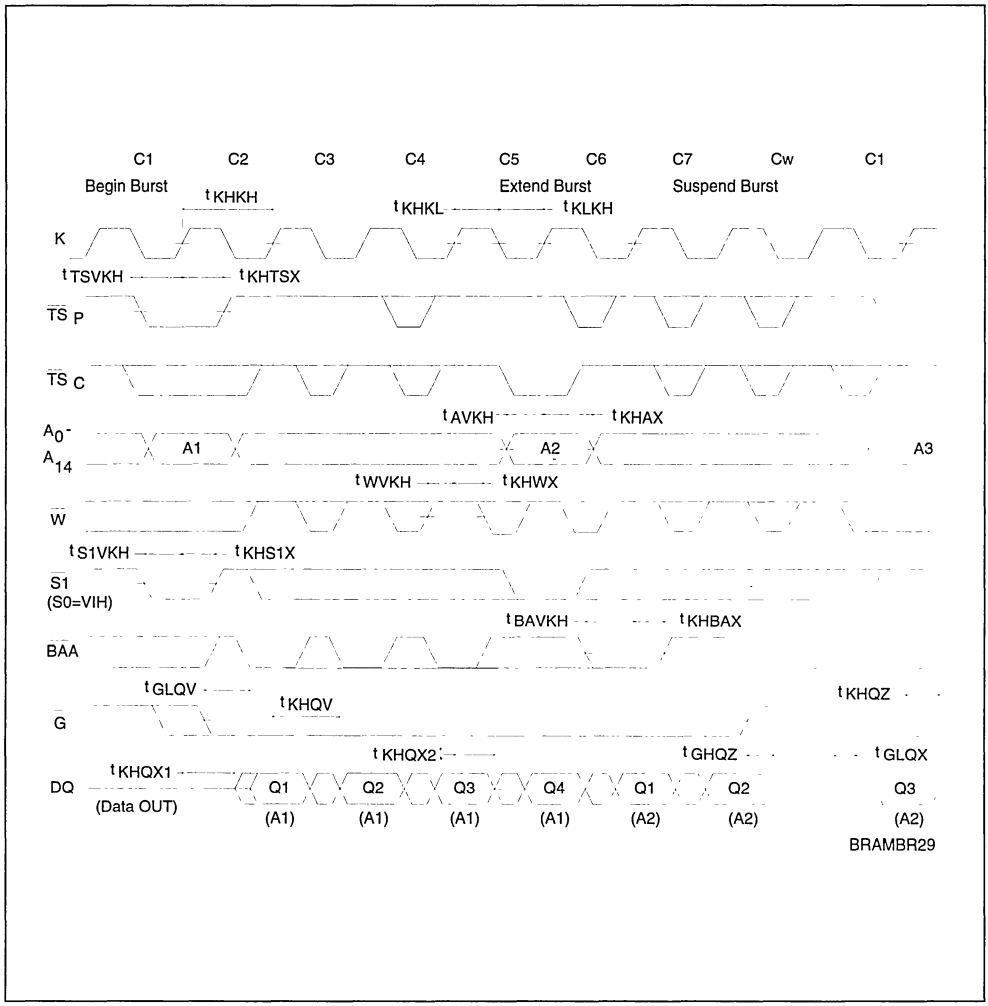


Figure 9. Burst Write Cycle

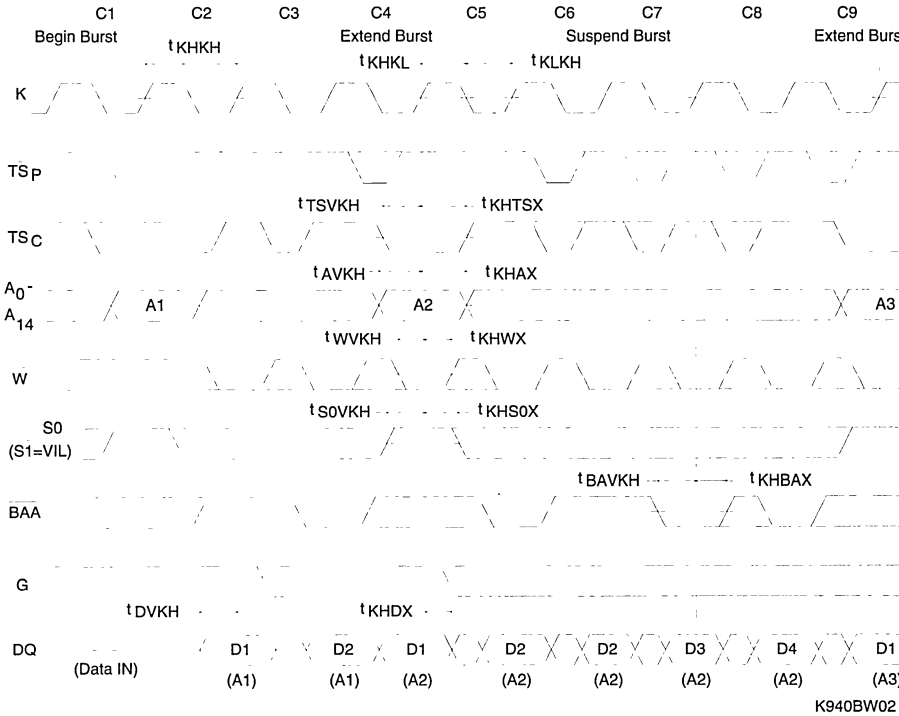
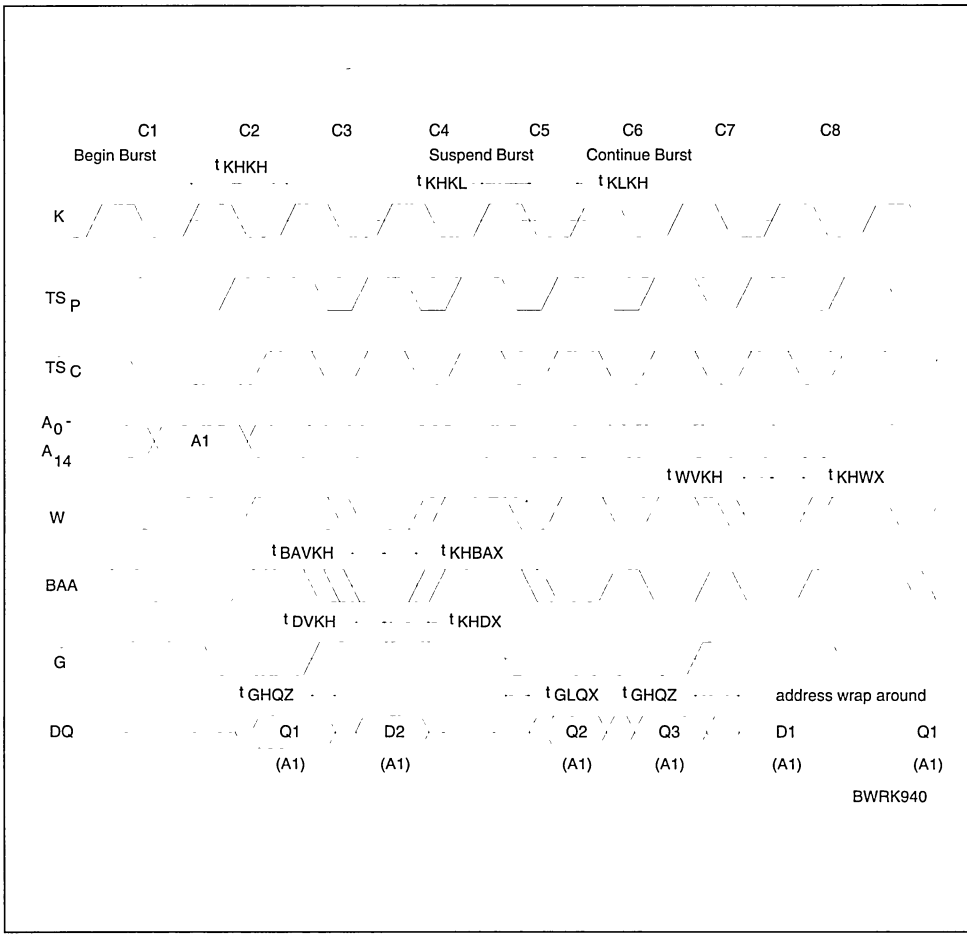
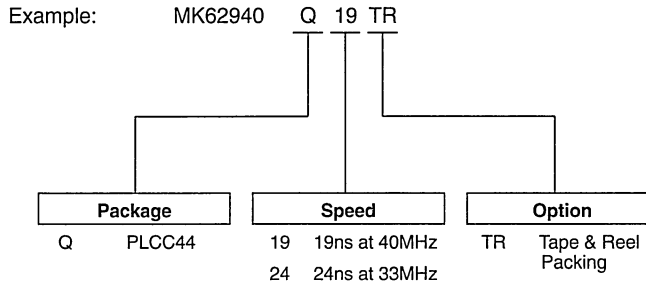


Figure 10. Combined Burst Read/Write Cycle



Note: SO = High, $\overline{S1}$ = Low.

ORDERING INFORMATION SCHEME



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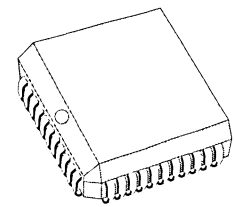
For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

VERY FAST CMOS 32K x 9 CACHE BRAM

ADVANCE DATA

- 32K x 9 CMOS SYNCHRONOUS BURST SRAM
- FAST CYCLE TIMES: 15, 20ns
- FAST ACCESS TIMES: 11, 12, 14ns Max
- ON-BOARD BURST COUNTER
- INPUT REGISTERS (ADDR.,DATA,CTRL)
- SELF-TIMED WRITE CYCLE
- THREE STATE COMMON I/O
- HIGH OUTPUT DRIVE CAPABILITY
- ASYNCHRONOUS OUTPUT ENABLE ($\overline{G}$)
- BURST CONTROL INPUTS: $\overline{TSP}$, $\overline{TSC}$, $\overline{BAA}$
- DUAL CHIP SELECTS for EASY DEPTH EXPANSION



PLCC44 (Q)

DESCRIPTION

The M62940A BRAM™ is a 288K (294,912 bit) CMOS Burst SRAM, organized as 32,768 words x 9 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology.

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ8	Data Inputs / Outputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0	Chip Select 0, Active High
$\overline{S1}$	Chip Select 1, Active Low
$\overline{TSP}$	Address Start Processor
$\overline{TSC}$	Address Start Cache Controller
$\overline{BAA}$	Burst Address Advance
V_{CC}	Supply Voltage
GND	Ground
V_{CCQ}	Supply Voltage (DQ)
GND_Q	Ground (DQ)

Figure 1. Logic Diagram

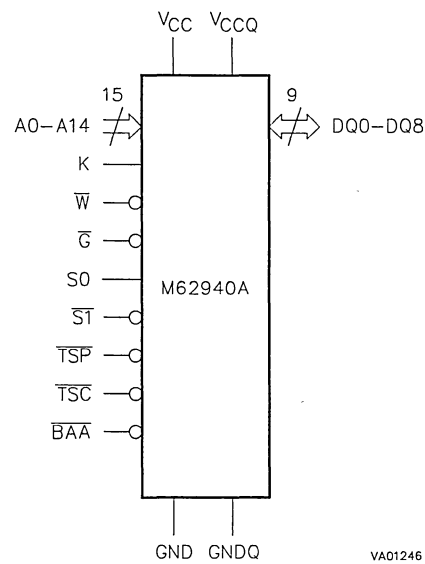
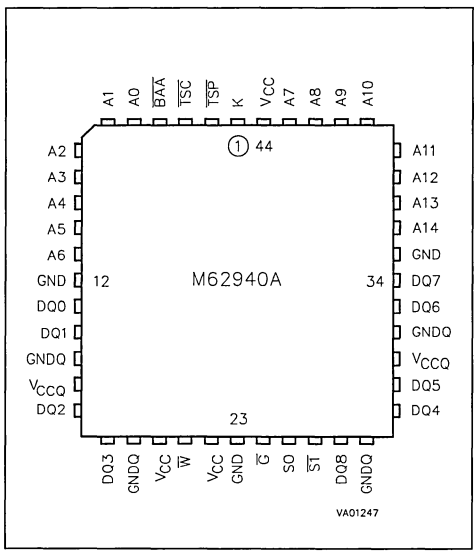


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.5 to 7	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (3)	Output Current	20	mA
P_D	Power Dissipation	1.2	W

Notes: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents
2. Up to a maximum operating V_{CC} of 5.5V only.
3. One output at a time, not to exceed 1 second duration.

Figure 2. LCC Pin Connections



DESCRIPTION (cont'd)

The device integrates a 2-bit burst counter, input registers, high output drive capability, and high speed synchronous SRAM onto a single chip. The synchronous design provides precise control using an external clock (K) input. The M62940A is specifically adapted to provide a burstable, high performance secondary cache for the MC68040 microprocessor.

The device is pin compatible and functional equivalent to the Motorola MCM62940. The M62940A is available in a 44 lead Plastic Leaded Chip Carrier package (PLCC).

The device provides multiple power and ground pins to reduce effects induced by output noise for high performance applications. Separate power and ground pins (V_{CCQ} and GND_Q) have been employed for DQ0-DQ8 to allow output levels referenced to 5V or 3.3V. For proper operation all GND and GND_Q pin must be connected to ground. $V_{CC} \geq V_{CCQ}$ at all times including power-up. The main Burst SRAM power requires a single 5V ± 5% supply, and all inputs and outputs are TTL compatible.

DEVICE OPERATION

Addresses (A0-A14), data inputs (DQ0-DQ8), and control signals, with exception of Output Enable ($\overline{G}$) are clock controlled inputs through non-inverting, positive edge triggered registers. A cache burst address sequence can be initiated by either $\overline{TSP}$ (Transfer Start Processor) or $\overline{TSC}$ (Transfer Start Cache Controller) inputs, with subsequent burst addresses being internally generated by the Burst SRAM.

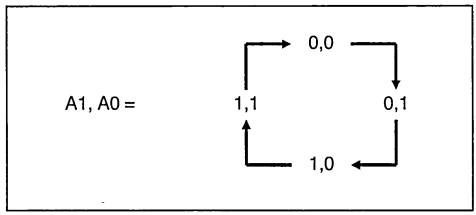
The $\overline{BAA}$ input (Burst Address Advance) provides control of the burst sequence, which imitates the required MC68040 cache burst address sequence. A cache burst cycle begins by loading the internal counter with the present values of A1 and A0. Thereafter, subsequent burst addresses are generated internally. The burst counter operates in the same manner for either cache burst write or read cycles.

Table 3. Asynchronous Truth Table

Mode	$\overline{G}$	DQ Status
Read	L	Data Out
Read	H	High-Z
Write[2]	X	Data In
Deselect	X	High-Z

Note: 1. X = Don't Care.
2. For a cache write cycle following a read operation, $\overline{G}$ must be high before the input data required set-up time, and be held high through the input data hold time.

Figure 3. Burst Count Sequence



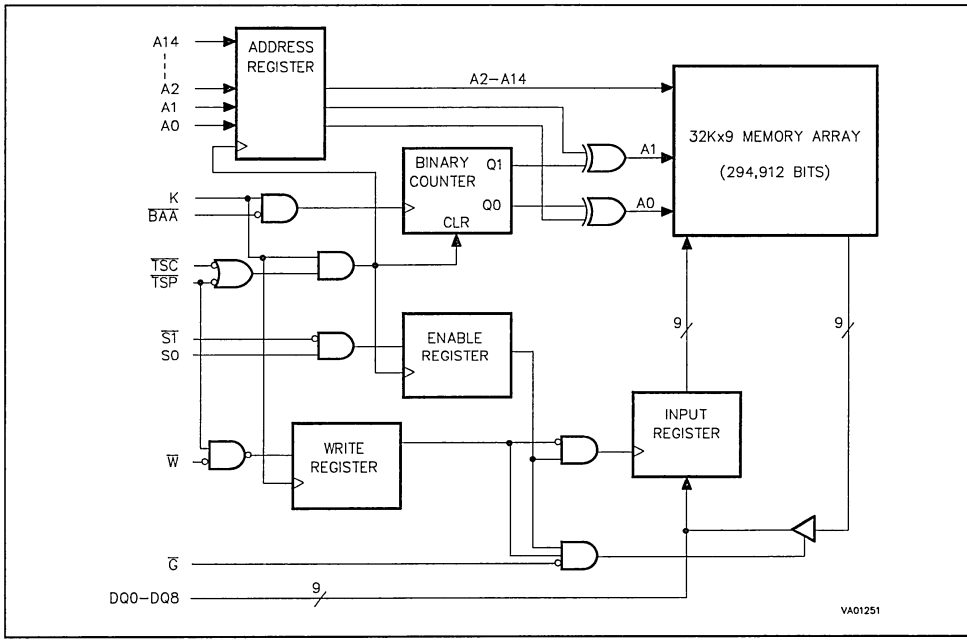
Note: The external values for A1, A0 are the starting point for the burst sequence graph. The burst counter will internally advance A1 and A0 as shown After the counter reaches a full count from the initial value, the address will wrap around.

Table 4. Synchronous Truth Table

S0	$\overline{S1}$	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{W}$	K	Address	Operation
L	X	L	X	X	X	↑	N/A	Deselected
X	H	H	L	X	X	↑	N/A	Deselected
H	L	L	X	X	X	↑	External Base Address	Read Cycle - Begin Burst
H	L	H	L	X	L	↑	External Base Address	Write Cycle - Begin Burst
H	L	H	L	X	H	↑	External Base Address	Read Cycle - Begin Burst
X	X	H	H	L	L	↑	Advance Burst Address	Write Cycle - Continue Burst Sequence
X	X	H	H	L	H	↑	Advance Burst Address	Reade Cycle - Continue Burst Sequence
X	X	H	H	H	L	↑	Hold Current Burst Address	Write Cycle - Suspend Burst Sequence
X	X	H	H	H	H	↑	Hold Current Burst Address	Read Cycle - Suspend Burst Sequence

Notes: 1. X = Don't Care.
2. All inputs except $\overline{G}$ require set-up and hold times to the rising edge (low to high transition) of the external clock (K).
3. All read and write timings are referenced from $\overline{G}$ or K.
4. A read cycle is defined by $\overline{W}$ high or $\overline{TSP}$ low for the required set-up and hold times. A write cycle is defined by $\overline{W}$ being asserted low for the set-up and hold times.
5. $\overline{G}$ is a don't care when $\overline{W}$ is registered low from the previous rising clock edge.
6. Chip Selects must be true (S0 = high, S1 = low) at each rising of the clock while $\overline{TSP}$ or $\overline{TSC}$ is asserted for the device to remain enable; Chip Selects are registered whenever $\overline{TSP}$ or $\overline{TSC}$ is asserted low at the rising edge of the clock.
7. Chip Selects must be true (S0 = high, $\overline{S1}$ = low) at each rising of the clock while $\overline{TSP}$ or $\overline{TSC}$ is asserted for the the device to remain enabled; Chip Selects are registered whenever $\overline{TSP}$ or $\overline{TSC}$ is asserted low at the rising edge of the clock.

Figure 4. Block Diagram



DEVICE OPERATIONS (cont'd)

The $\overline{TSP}$ and the $\overline{TSC}$ inputs control the start of the burst sequence. When either $\overline{TSx}$ is asserted low at the rising edge of the clock, any ongoing burst cycle is interrupted and a new external base address is registered. Chip selects (S0 and $\overline{S1}$) are only sampled when a new base address is loaded.

Therefore, the chip selects are registered when either transfer start input is asserted low at the rising edge of the clock (K), and remain latched internally until the next assertion of either $\overline{TSP}$ or $\overline{TSC}$. The M62940A Truth Tables and timing diagrams reference specific device operations.

It should be noted that the M62940A allows a non-burst mode of operation where $\overline{TSP}$ is the $\overline{TS}$ pin of the MC68040 processor in a typical 2 clock cycle mode of operation, and $\overline{TSC}$ is held high during C2 (see Figure 7). However, the non-burst mode obviously negates the advantage of the internal burst counter for fast cache fill operations. In either mode (burst or non-burst), the write cycles are internally self-timed, and are initiated by the rising edge of the clock input when $\overline{W}$ is low.

The $\overline{BAA}$ input controls subsequent burst data accesses after the first data of the burst cycle is processed. Each time $\overline{BAA}$ is asserted low for subsequent bursts at the rising edge of the clock

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Load Circuit

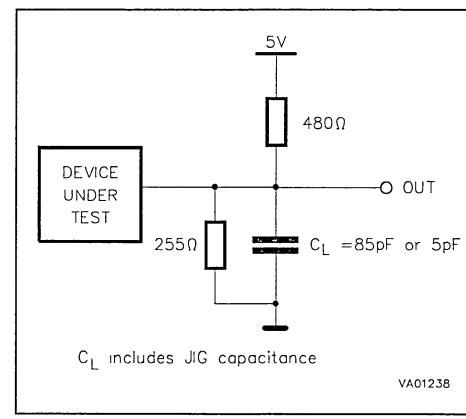


Table 5. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		5	pF
C_{OUT} [2]	Output Capacitance	V_{OUT} = 0V		10	pF

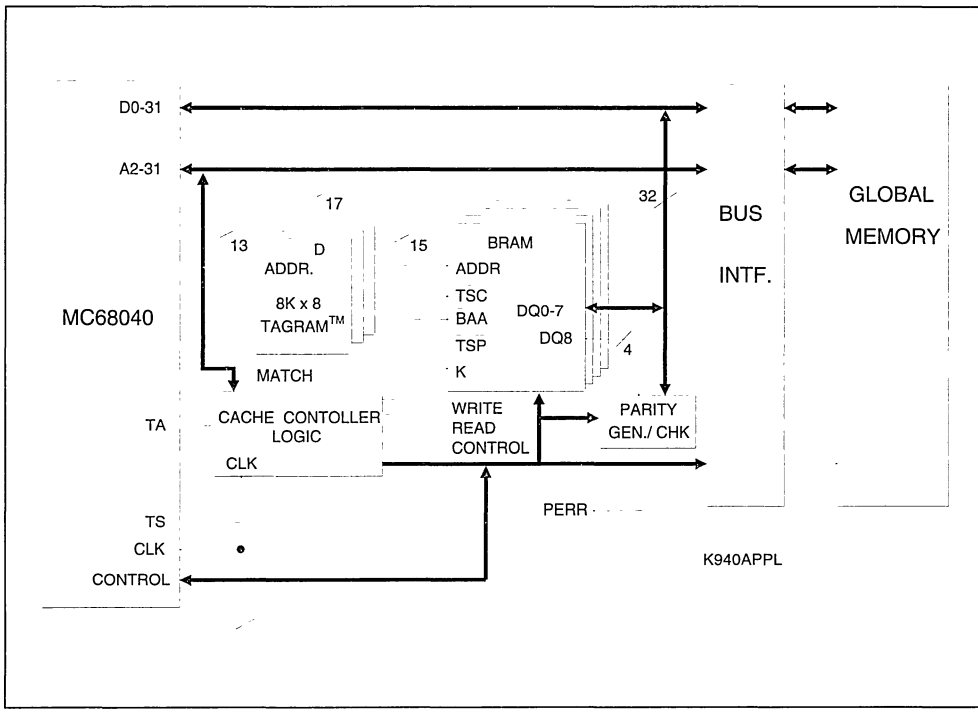
Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Table 6. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±1	µA
I_{CC1} [1]	Supply Current	$\overline{G}$ = V_{IH}, S0 = V_{IH}, $\overline{S1}$ = V_{IL}, All inputs = V_{IL} = 0V and V_{IH} ≥ 3V		180	mA
I_{CC2} [2]	Supply Current (Standby) TTL	S0 = V_{IL}, $\overline{S1}$ = V_{IH}		40	mA
I_{CC3} [3]	Supply Current (Standby) CMOS	S0 ≤ 0.2V, $\overline{S1}$ ≥ V_{CC} –0.2V		30	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{KHKH} minimum
2. All other Inputs at V_{IL} ≤ 0.8V or V_{IH} ≥ 2.2V
3. All other Inputs at V_{IL} ≤ 0.2V or V_{IH} ≥ V_{CC} – 0 2V

Figure 6. General 128K Byte Cache Biock Diagram



DEVICE OPERATIONS (cont'd)

input, the burst counter is advanced to the next burst address sequence. The address is advanced from the rising edge of K. Wait states can be inserted during burst cycles by holding the $\overline{BAA}$ pin high during positive clock transitions. Upon completion of the full internal burst count, the address will wrap-around to its initial base address.

GENERAL APPLICATION

The M62940A is organized as 32K x 9 bit words to support byte parity. By incorporating TAGRAM™ with a 15 bit tag field and a 15 bit index address, a cache address scheme of 30 bits is monitiored. The TAGRAM in addtion to the M62940A provides an architecture for building a 32K x 32 bit burstable data cache SRAM array, with byte parity, by using four devices in a 128K byte cache application.

Table 7. Read and Write Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter	M62940A						Unit	Note
		11		12		14			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{KHKH}	Cycle Time	15		15		20		ns	
t_{KHQV}	Clock Access Time		11		12		14	ns	1
t_{KHKL}	Clock High Pulse Width	5.5		5.5		8		ns	
t_{KLKH}	Clock Low Pulse Width	5.5		5.5		8		ns	
t_{GLQV}	Output Enable Access Time		5		5		6	ns	1
t_{KHQX2}	Clock High to Output Hold Time	3		3		4		ns	2
t_{KHQX1}	Clock High to Output Active	4		4		4		ns	2
t_{GLQX}	Output Enable to Output Active	0		0		0		ns	2
t_{KHQZ}	Clock High to Q High-Z		6		6		6	ns	2
t_{GHQZ}	Output Disable to Q High-Z		6		6		6	ns	2
t_{AVKH}	Address Set-up Time	2		2		3		ns	3
t_{TSVKH}	Transfer Start Set-up Time	2		2		3		ns	3
t_{DVKH}	Data In Set-up Time	2		2		3		ns	3
t_{SWVKH}	Write/Read Set-up Time	2		2		3		ns	3
t_{BAVKH}	Burst Address Advance Set-up Time	2		2		3		ns	3
t_{S0VKH}	Chip Select 0 (S0) Set-up Time	2		2		3		ns	3
t_{S1VKH}	Chip Select 1 ($\overline{S1}$) Set-up Time	2		2		3		ns	3
t_{KHAX}	Address Hold Time	2		2		2		ns	3
t_{KHTSX}	Transfer Start Hold Time	2		2		2		ns	3
t_{KHDX}	Data In Hold Time	2		2		2		ns	3
t_{KHWX}	Write/Read Hold Time	2		2		2		ns	3
t_{KHBAX}	Burst Address Advance Hold Time	2		2		2		ns	3
t_{KHWX}	Asynchronous Write ($\overline{AW}$) Hold Time	2		2		2		ns	3
t_{KHS0X}	Chip Select 0 (S0) Hold Time	2		2		2		ns	3
t_{KHS1X}	Chip Select 1 ($\overline{S1}$) Hold Time	2		2		2		ns	3

Notes: 1. C_L = 85pF (see Figure 5).
2. Transition is measured ± 500 mV from steady-stage voltage with C_L = 5pF (see Figure 5) This parameter is sampled and not 100 % tested.
3. This is synchronous device requiring that all inputs must meet the specified set-up and hold times with stable logic levels for all rising edges of the clock input (K).

Figure 7. Typical Non-Burst Read/Write Cycles

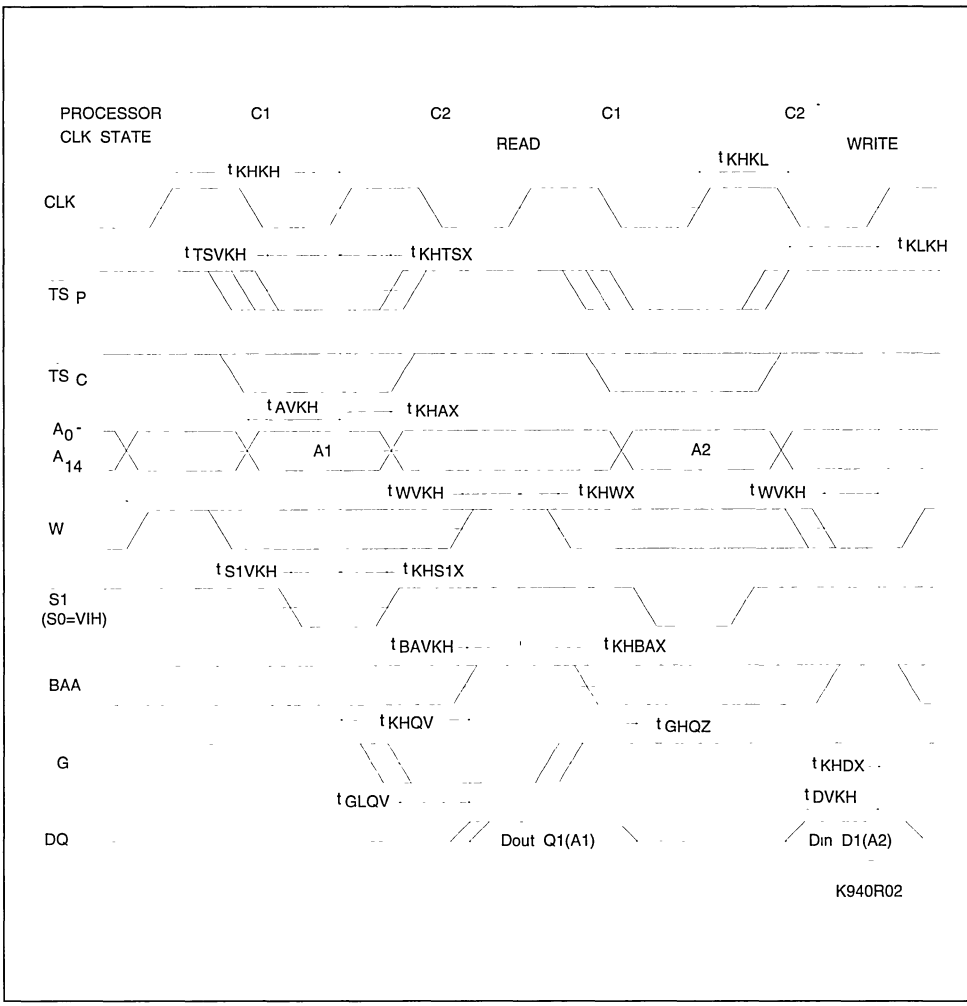


Figure 8. Burst Read Cycle

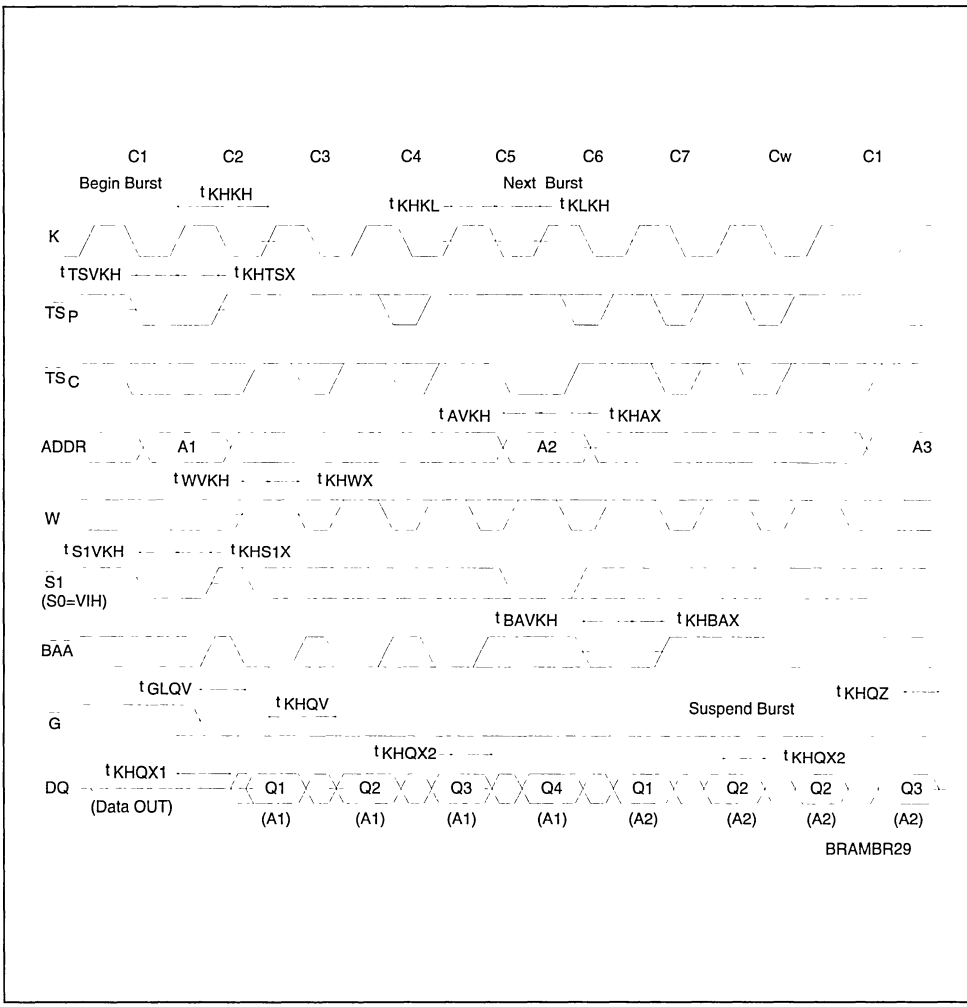


Figure 9. Burst Write Cycle

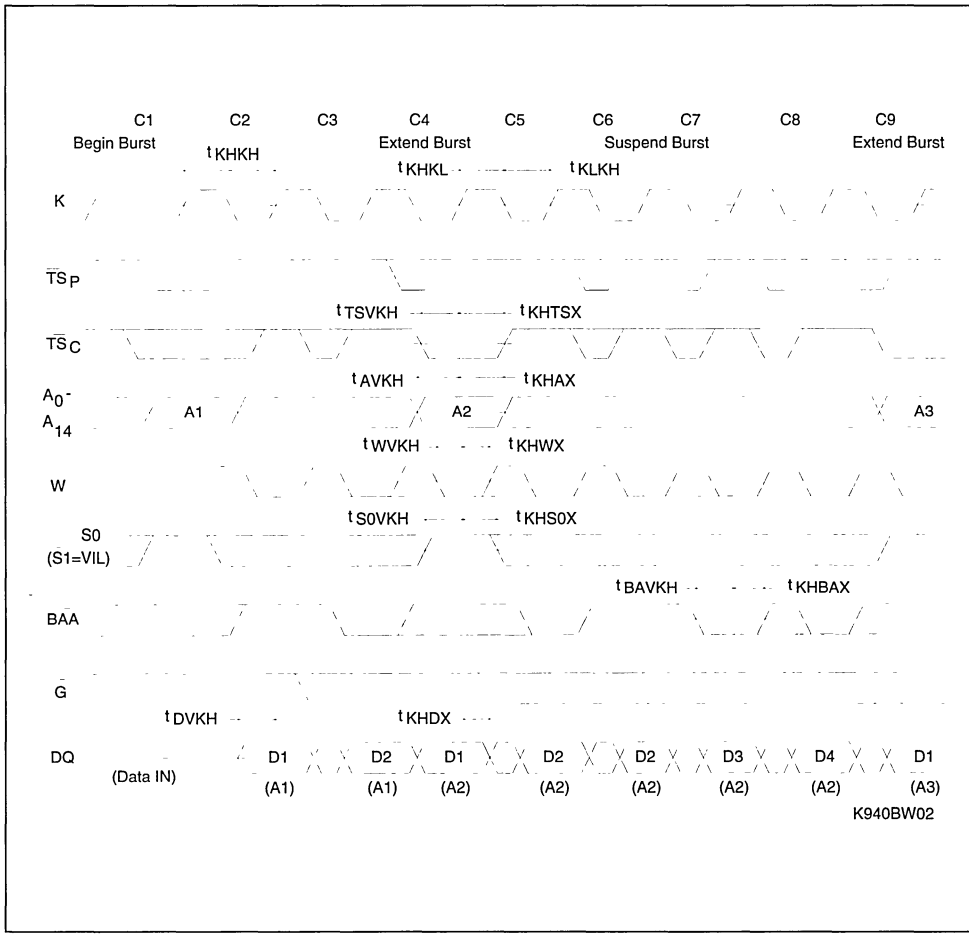
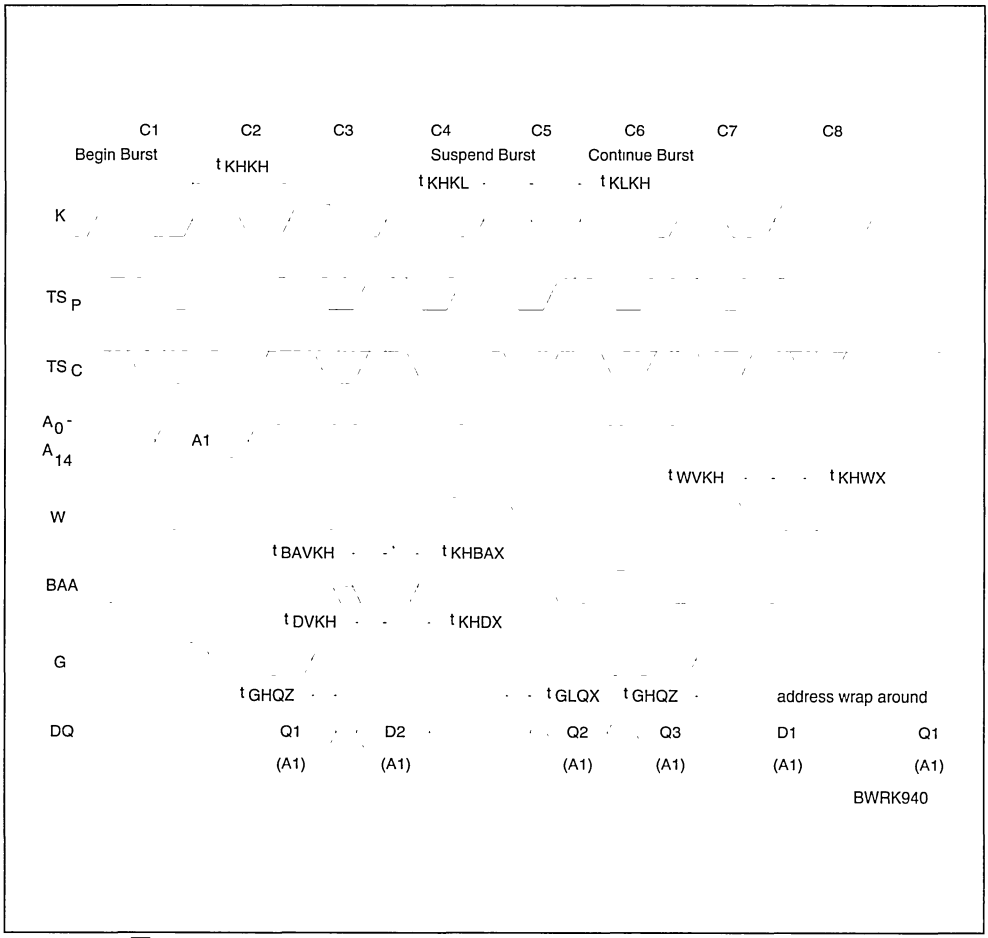
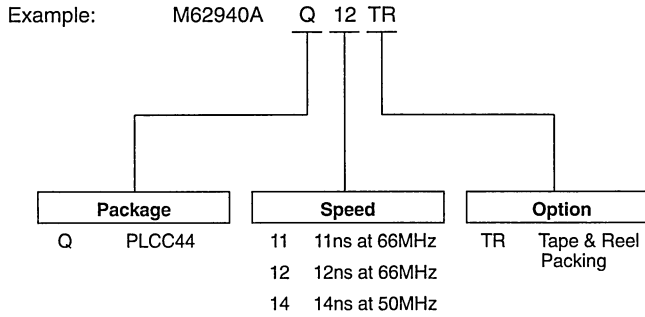


Figure 10. Combined Burst Read/Write Cycle



Note: SO = High, $\overline{S1}$ = Low.

ORDERING INFORMATION SCHEME



For a list of available options (Package, Speed, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

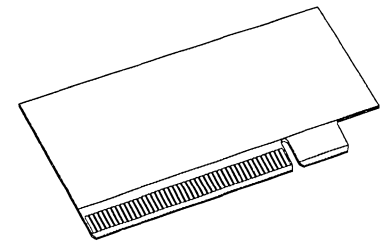
SGS-THOMSON MICROELECTRONICS

STCM128
STCM256

128K/256K BYTE L2 CACHE RAM MODULE WITH TAG

PRODUCT CONCEPT

- 128K BYTE and 256K BYTE LEVEL-2 i486 CACHE MODULES
- SUPPORTS BURST CACHE LINE FILLS; FAST ACCESS TIME 15ns, TAG ACCESS 12ns
- CONFIGURED as 128K DIRECT MAPPED WITH 8K x 8 SRAM (TAG) or 256K TWO WAY SET ASSOCIATIVE with 16K x 8 SRAM (TAG)
- INCLUDES SOCKET for X1 SRAM (DIRTY BIT)
- SINGLE SUPPLY VOLTAGE: 5V ±10%
- ALL I/O TTL COMPATIBLE
- MULTIPLE V_{CC} and V_{SS} PINS for MAXIMUM NOISE IMMUNITY
- HIGH QUALITY FR4 MULTI LAYER PCB



Card

DESCRIPTION

The STCM128 and STCM256 are L2 Cache modules designed to work with the i486® processor. Both are constructed from high grade FR4 Laminate material and feature multiple power and ground pins as well as separate power and ground planes. All inputs and outputs are TTL compatible, and operate from a single 5V ±10% supply.

The modules are designed to offer 15ns data access times and 12ns Tag access to support burst cache line fills to the i486 microprocessor for fast clock rates up to 50MHz.

To minimize processor address hold time, all addresses are latched as controlled by an independent latch control signal. The design incorporates enough tag field for a valid bit and provision for a dirty bit to support copy back cache updates.

Table 1. Pin Description Overview

Pin Name	Type	Active	Description
Control Signals			
ALE	I	High	Address Latch Enable
CWE0#	I	Low	Cache Write Enable 0
CWE1#	I	Low	Cache Write Enable 1
CWE2#	I	Low	Cache Write Enable 2
CWE3#	I	Low	Cache Write Enable 3
COE#	I	Low	Cache Output Enable
LCS#	I	Low	Lower Bank Cache Select
UCS#	I	Low	Upper Bank Cache Select (256K only)
TWE#	I	Low	Tag Write Enable
TOE#	I	Low	Tag Output Enable
TCEN	I	High	Tag Chip Enable High
TCEN#	I	Low	Tag Chip Enable Low
DWE#	I	Low	Dirty Bit Write Enable
DCE#	I	Low	Dirty Bit Chip Enable
Address Signals			
A4 - A17	I		Address Lines: A4 - A17
BA2 - BA3	I		Burst Address Inputs, Bank A
BB2 - BB3	I		Burst Address Inputs, Bank B (256K only)
Data Signals			
D0 - D31	I/O		Cache Sram Data Lines: D0 - D31
DI	I		Dirty Bit Input
DO	O		Dirty Bit Output
TD0 - TD7	I/O		Tag Data Inputs / Outputs
Power Pins			
V_{CC}	Supply	5V ±10%	5V System Supply Voltage
V_{SS}	Ground	0V	System Ground Plane

Figure 1. STCM128 Block Diagram

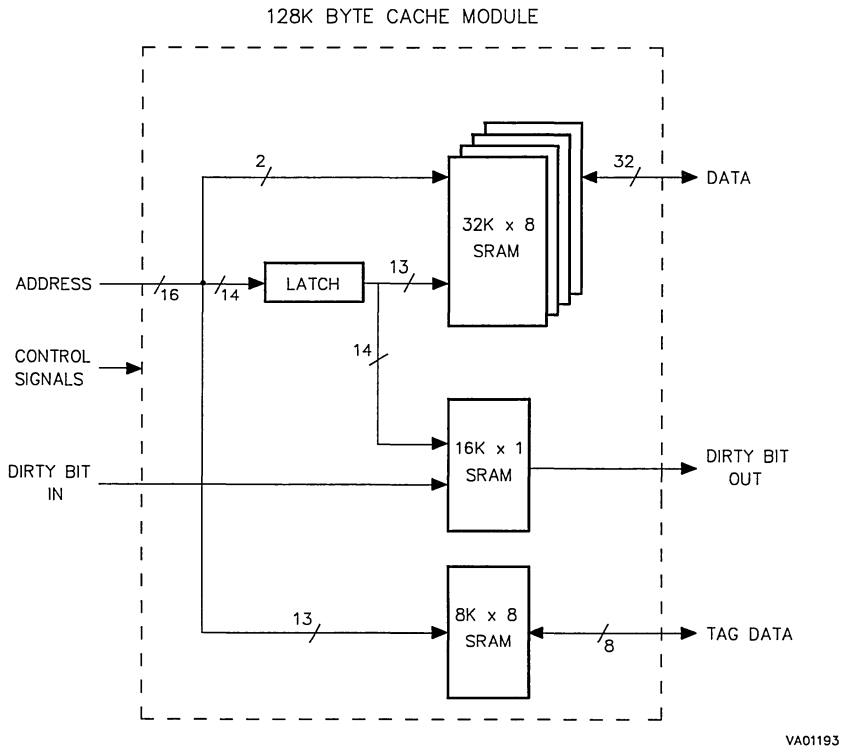
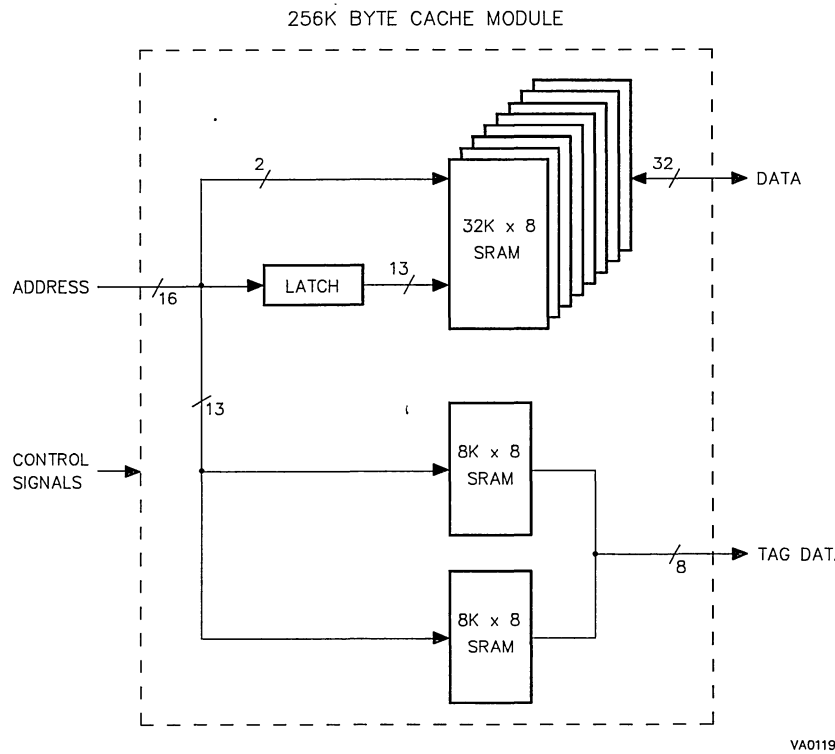


Figure 2. STCM256 Block Diagram



FIFO MEMORIES

VERY FAST CMOS 1K x 5 CLOCKED FIFO

- FIRST-IN-FIRST-OUT MEMORY BASED ARCHITECTURE
- 1024 x 5 ORGANIZATION
- RISING EDGE TRIGGERED CLOCK INPUTS
- SUPPORTS FREE-RUNNING 40% TO 60% DUTY CYCLE CLOCK INPUTS
- SEPARATE READ AND WRITE ENABLE INPUTS
- BiPORT RAM ARCHITECTURE ALLOWS FULLY ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE OPERATION
- CASCADABLE TO ANY DEPTH WITH NO ADDITIONAL LOGIC
- WIDTH EXPANDABLE TO MORE THAN 40 BITS WITH NO ADDITIONAL LOGIC
- HALF FULL STATUS FLAG
- FULL AND EMPTY FLAGS, ALMOST FULL, ALMOST EMPTY, INPUT READY, OUTPUT VALID STATUS FLAGS (4505M)

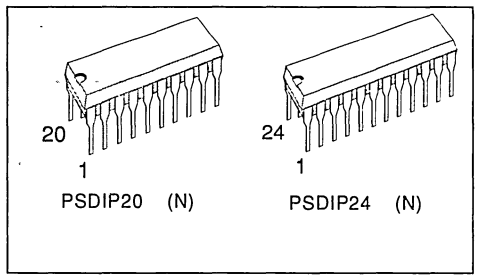
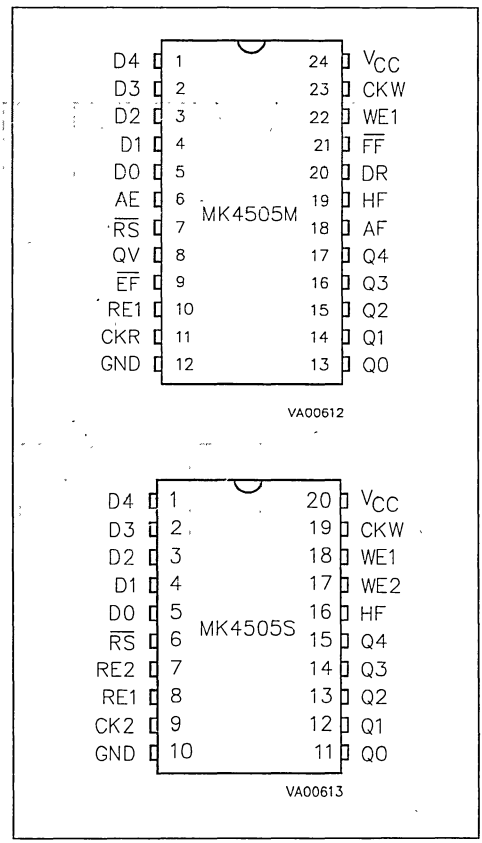


Figure 1. Pin Connections.



DESCRIPTION

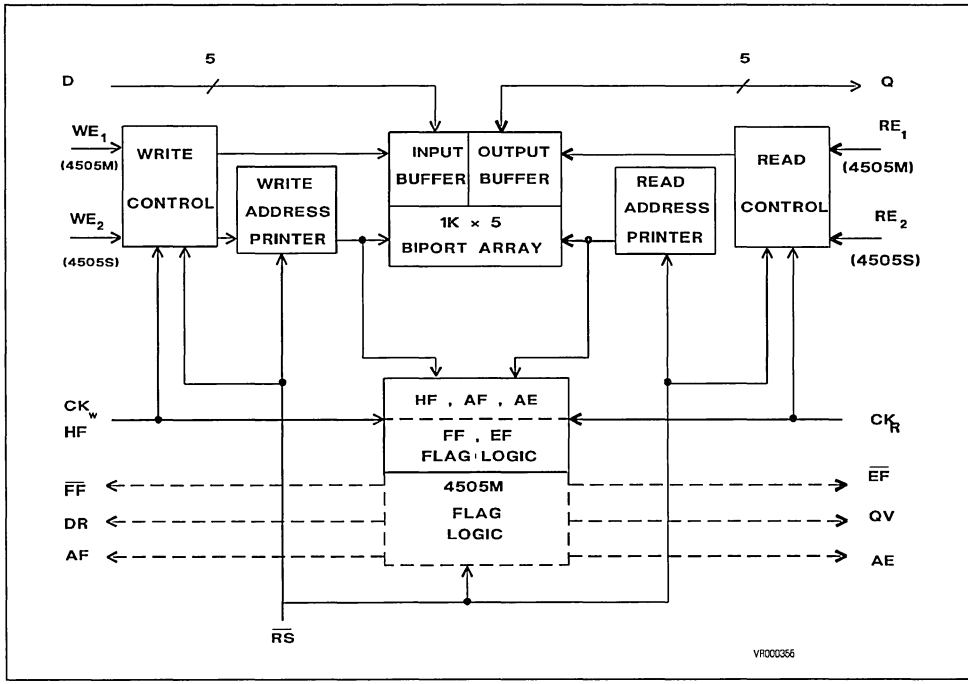
The MK4505 is a Very High Speed 1K x 5 Clocked FIFO memory. It achieves its high performance through the use of a pipelined architecture, a 1.2µ full CMOS, single poly, double level metal process, and a memory array constructed using SGS-THOMSON's 8 transistor BiPORT™ memory cell.

The device is designed for use in applications where data is moving through a system on a square wave clock ; applications such as digitized video and audio, image processing, A-to-D and D-to-A conversions, high speed data links, Radar return sampling or data tracing.

PIN NAMES

D0 - D4	Data Inputs
Q0 - Q4	Data Outputs
CKW, CKR	Write and Read Clock
WE1	Write Enable Input 1
RE1	Read Enable Input 1
$\overline{RS}$	Reset (active low)
HF	Half Full Flag
V_{CC}, GND	5 Volts, Ground

Figure 2 . Block Diagram.



DESCRIPTION (Continued)

The device is available in two versions; a Master, the MK4505M, and a Slave, the MK4505S. The Master provides all of the control signals necessary for reliable, full speed, fully asynchronous width expansion and/or depth expansion. The Master also provides a full compliment of status flags, including Output Valid, Empty, Almost Empty, Half Full, Almost Full, Full, and Input Ready. The Master cannot be written while Full or read while Empty. The Slave, in contrast, can be forced to write and/or read continuously regardless of device status ; a feature useful in triggered data acquisitions, or for retransmit (repeat reading) applications.

4505M only

$\overline{FF}$,$\overline{EF}$	Full and Empty Flags (active low)
AF,AE	Almost, Full, Almost Empty Flags
DR,QV	Input Ready, Output Valid

4505S only

WE2	Write Enable Input 2
RE2	Read Enable Input 2 (rising edge triggered 3 state control)

ASBOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	– 1.0 to 70	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Ambient Storage Temperature (plastic)	– 55 to 125	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current per Pin	25	mA

Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
V_{CC}	Supply voltage	4.5	5	5.5	V	1
GND	Ground	0	0	0	V	1
V_{IH}	Logic 1 input	2.2		V_{CC} + 1.0	V	1
V_{IL}	Logic 0 input	– 0.3		0.8	V	1

Note : 1. All voltages referenced to GND.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$; V_{CC} =5V ±10%)

Symbol	Parameter	4505-25			4505-33			4505-50			Unit	Note
		Min.	Typ.	Max	Min.	Typ.	Max	Min.	Typ.	Max		
I_{CC}	Average Power Supply Current		115	140		95	140		75	140	mA	1

Symbol	Parameter	Min.	Max.	Unit	Note
I_{IL}	Input Leakage Current		± 1	µA	2
I_{CL}	Output Leakage Current		± 10	µA	2,3
V_{OH}	Logic 1 Output Voltage (I_{OUT} = –4 mA)	2.4		V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8 mA)		0.4	V	4

Notes : 1. Measured with both ports operating at t_{CK} Min, 50% duty cycle, outputs open, V_{CC} max. Typical values reflect t_{CK} Min, outputs open, with V_{CC} = 5V, 25°C, with 50% duty cycle.
2. Measured with V = 0V to V_{CC}.
3. Measured at Q0 – Q4, with QV = Low (4505M) ; after clocking with RE2 = Low (4505S).
4. All voltages referenced to GND.

CAPACITANCE (T_A =25°C, f =1.0MHz)

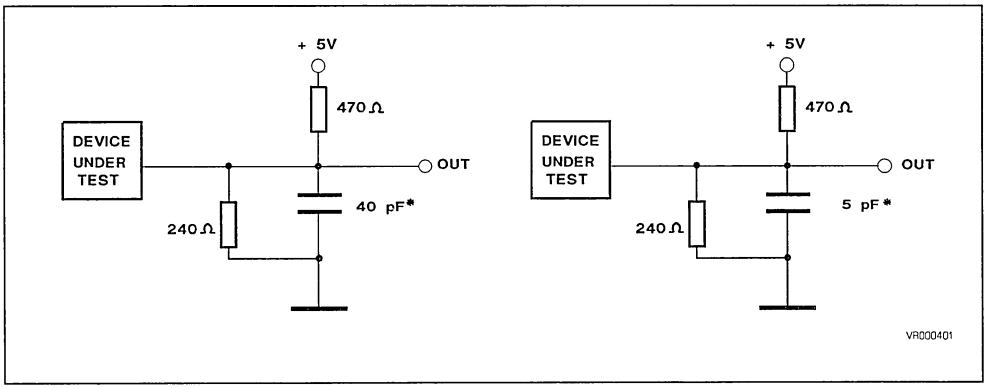
Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
C_I	Input Capacitance	4		5	pF	1
C_{O1}	Output Capacitance	8		10	pF	1,2
C_{O2}	Output Capacitance	12		15	pF	1,3

Notes : 1. Sampled, not 100% tested. Measured at 1MHz.
2. Measured at all data and flag outputs except $\overline{EF}$ and $\overline{FF}$.
3. Measured at $\overline{EF}$ and $\overline{FF}$.

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Times	5	ns
Input and Output Timing Reference Levels	1.5	V
Ambient Temperature	0 to 70	°C
V_{CC}	5 ± 10%	V

Figure 3. Output Load Circuits.



Note : * Includes scope and test fixture.

READ AND HOLD OPERATIONS

The device will perform a Read on the next rising edge of the Read Clock (CKR) whenever (see Figure 4) :

- (4505S) RE1 and RE2 are high at the rising edge of the clock.
- (4505M) RE1 and $\overline{EF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Empty Flag ($\overline{EF}$) on the rising edge of CKR, the appearance of an active Empty Flag at valid flag access time, t_{F1A}, assures the user that the next rising edge of CKR will generate an inhibit condition. All Q outputs will be High Z at t_{QZ} from the rising edge of CKR. $\overline{EF}$ is latched between subsequent read clocks.

The device will perform a Hold Cycle (hold over previous data) if RE1 is low at the rising edge of the clock (CKR). If $\overline{EF}$ (4505M) or RE2 (4505S) is low at the rising edge of the clock, then the outputs will go to High-Z.

WRITE OPERATIONS

The device will perform a Write on the next rising edge of the Write Clock (CKW) whenever (see Figure 5) :

- (4505S) WE1 and WE2 are high at the rising edge of the clock.
- (4505M) WE1 and $\overline{FF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Full Flag ($\overline{FF}$) on the rising edge of CKW, the appearance of an active Full Flag at valid flag access time, t_{F1A}, assures the user that the next rising edge of CKW will generate a No-Op condition. $\overline{FF}$ is latched between subsequent write clocks.

MK4505M (Master) WRITE TRUTH TABLE

CKW	Present State			Operation	Next State	
	$\overline{RS}$	WE1	$\overline{FF}$		$\overline{FF}$	Data in
X	0	X	X	Reset	1	Don't Care
↑	1	0	0	No-Op	?	Don't Care
↑	1	0	1	No-Op	1	Don't Care
↑	1	1	0	No-Op	?	Don't Care
↑	1	1	1	Write	?	Data in

? = Device Status is referenced to the "next state" logic conditions.
The "next state" flag logic level is unknown due to the possible occurence of a read operation.

MK4505M (Master) READ TRUTH TABLE

CKR	Present State			Operation	Next State	
	$\overline{RS}$	RE1	$\overline{EF}$		$\overline{EF}$	Q_{OUT}
X	0	X	X	Reset	0	Hi Z
↑	1	0	0	Inhibit	?	Hi Z
↑	1	0	1	Hold	1	Previous Q
↑	1	1	0	Inhibit	?	Hi Z
↑	1	1	1	Read	?	Data Out

? = Device Status is referenced to the "next state" flag logic and Q_{OUT} conditions.
The "next state" flag logic level is unknown due to the possible occurrence of a write operation.

MK4505S (Slave) WRITE TRUTH TABLE

CKW	Present State			Operation	Next State
	$\overline{RS}$	WE1	WE2		Data
X	0	X	X	Reset	Don't Care
↑	1	0	0	No-Op	Don't Care
↑	1	0	1	No-Op	Don't Care
↑	1	1	0	No-Op	Don't Care
↑	1	1	1	Write	Data in

MK4505S (Slave) READ TRUTH TABLE

CKR	Present State			Operation	Next State
	$\overline{RS}$	RE1	RE2		Q_{OUT}
X	0	X	X	Reset	Hi Z
↑	1	0	0	Inhibit	Hi Z
↑	1	0	1	Hold	Previous Q
↑	1	1	0	Inhibit	Hi Z
↑	1	1	1	Read	Data Out

RESET

$\overline{RS}$ is an asynchronous master reset input. A Reset is required after power-up, before first write. Reset commences on the falling edge of $\overline{RS}$ irrespective of the state of any other input or output. The user is required to observe Reset Set Up Time (t_{RSS}) only if the device is enabled (see Figure 7). The t_{RSS} specification is a don't care if the device remains disabled (WE1 = RE1 = LOW). All status flag outputs will be valid t_{RSA} from the falling edge of $\overline{RS}$, and all Q data outputs will be high impedance t_{RSQZ} from the same falling edge.

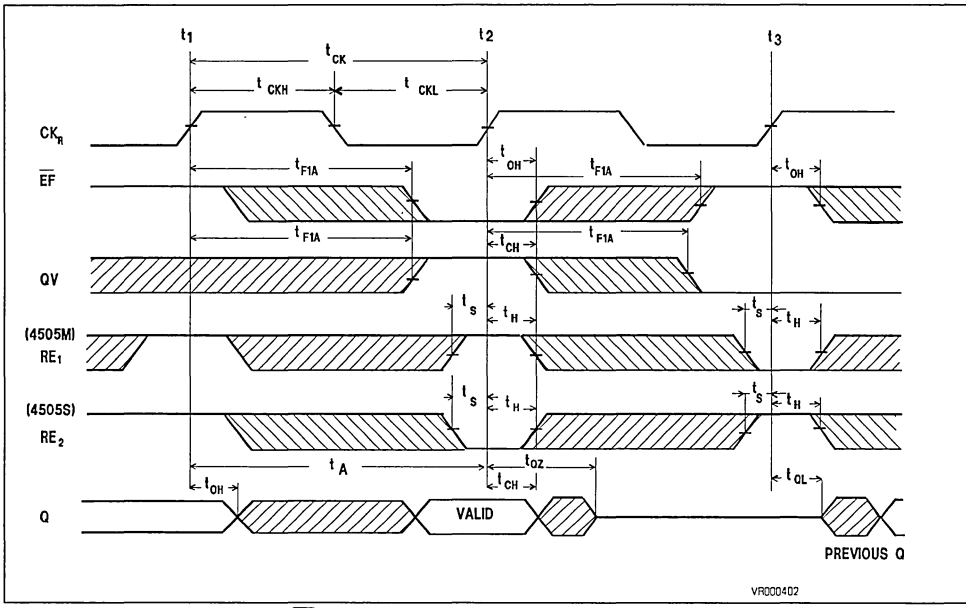
After Reset, if no valid Read operations have been performed since Reset, the "previous data" that will be output when executing the first Hold cycle will be all zeros (see Figure 8).

AC ELECTRICAL CHARACTERISTICS (T_A =0°C to 70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	4505-25		4505-33		4505-50		Unit	Note
		Min.	Max	Min.	Max	Min.	Max.		
t_{CK}	Clock Cycle Time	25		33		50		ns	1
t_{CKH}	Clock High Time	10		13		20		ns	1
t_{CKL}	Clock Low Time	10		13		20		ns	1
t_S	Set Up Time	10		13		16		ns	1
t_H	Hold Time	0		0		0		ns	
t_A	Output (Q) Access Time		15		20		25	ns	1, 2
t_{F1A}	Flag 1 Access Time (7)		15		20		25	ns	1, 2
t_{F2A}	Flag 2 Access Time (8)		20		25		30	ns	1, 2
t_{OH}	Output Hold Time	5		5		5		ns	1, 2
t_{OZ}	Clock to Outputs High-Z		15		20		25	ns	1, 3
t_{OL}	Clock to Outputs Low-Z	5		5		5		ns	1, 3
t_{RSS}	Reset Set Up Time	12		16		25		ns	1, 4
t_{RS}	Reset Pulse Width	25		33		50		ns	
t_{RSA}	Reset Flag Access Time		50		66		100	ns	1, 3
t_{RSQZ}	Reset to Outputs High-Z		25		33		50	ns	1, 3
t_{FRL}	First Read Latency	50		66		100		ns	1, 5
t_{FFL}	First Flag Cycle Latency	25		33		50		ns	1, 6

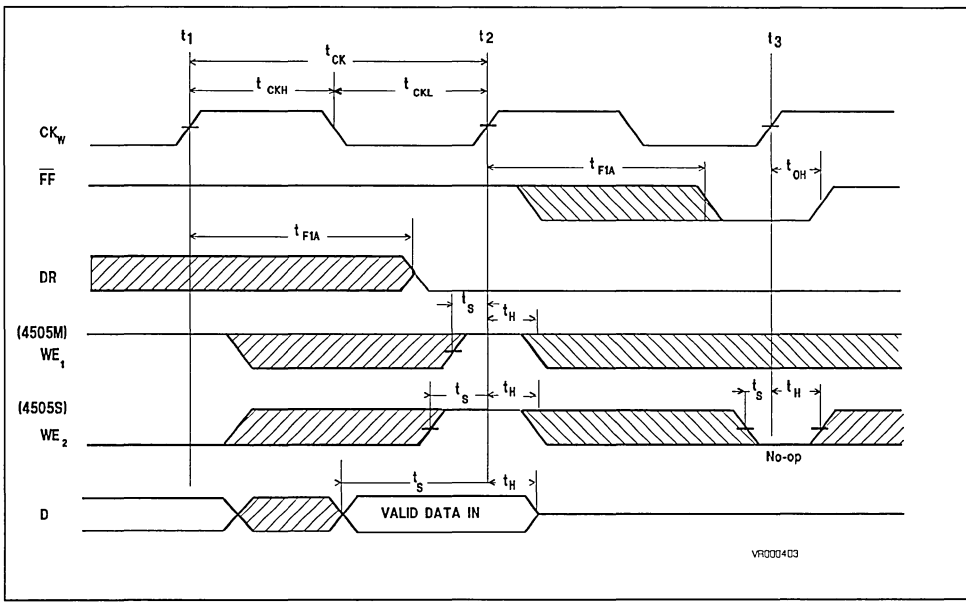
Notes : 1. All AC Electrical Characteristics measured under conditions specified in "AC Test Conditions".
2. Measured w/40pf Output Load (Figure 3A)
3. Measured w/5pf Output Load (Figure 3B).
4. Need not be met unless device is Read and/or Write Enabled.
5. Minimum first Write to first Read delay required to assure valid first Read.
6. Minimum first Write to first Read Clock delay required to assure clearing the Empty Flag.
7. Flag 1 = EF, FF, QV, DR.
8. Flag 2 = AE, AF, HF.

Figure 4. Read Cycle Timing.



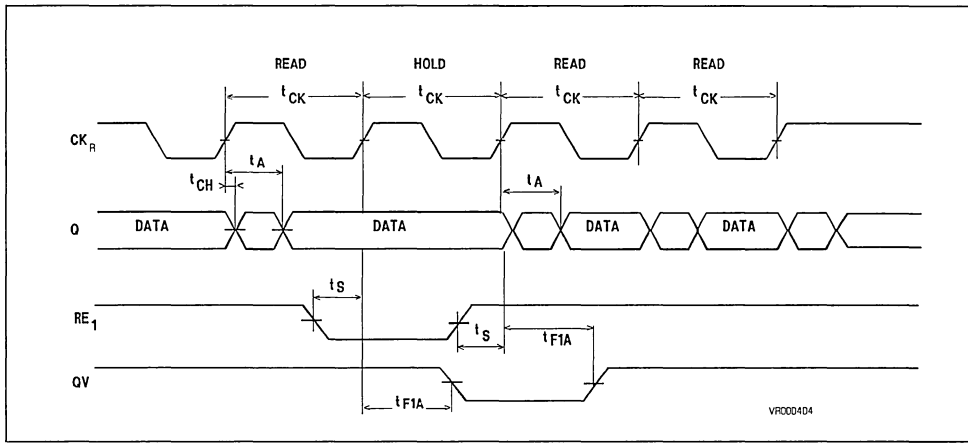
Note : For this particular diagram the $\overline{EF}$ changes logic states presuming that a valid WRITE operation has occured prior to the rising edge of CKR at t_2.

Figure 5. Write Cycle Timing.



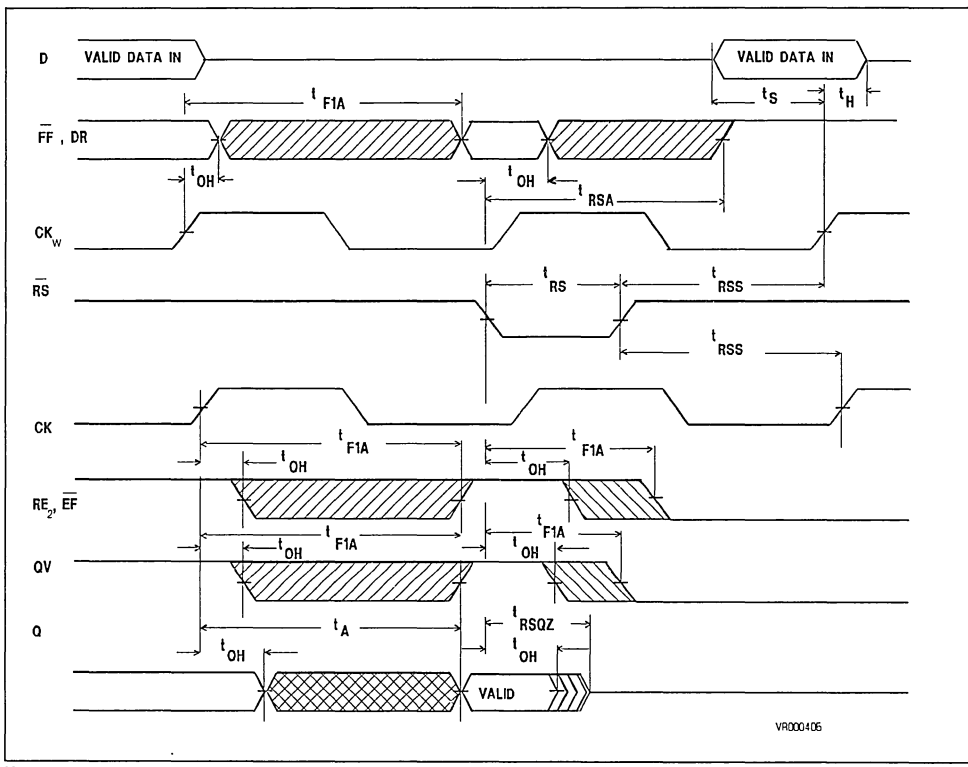
Note : For this particular diagram the $\overline{FF}$ changes logic states presuming that a valid READ operation has occured prior to the rising edge of CKW at t_3.

Figure 6 . Hold Cycle Timing.



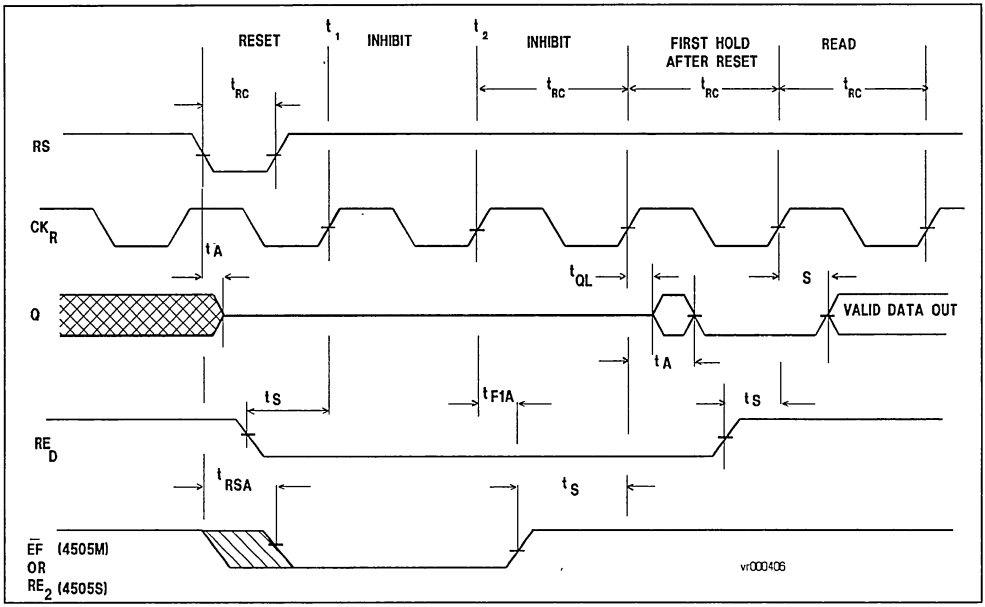
Note : $\overline{EF}$ = HIGH (master)
RE2 = HIGH (slave)

Figure 7. Reset Cycle Timing.



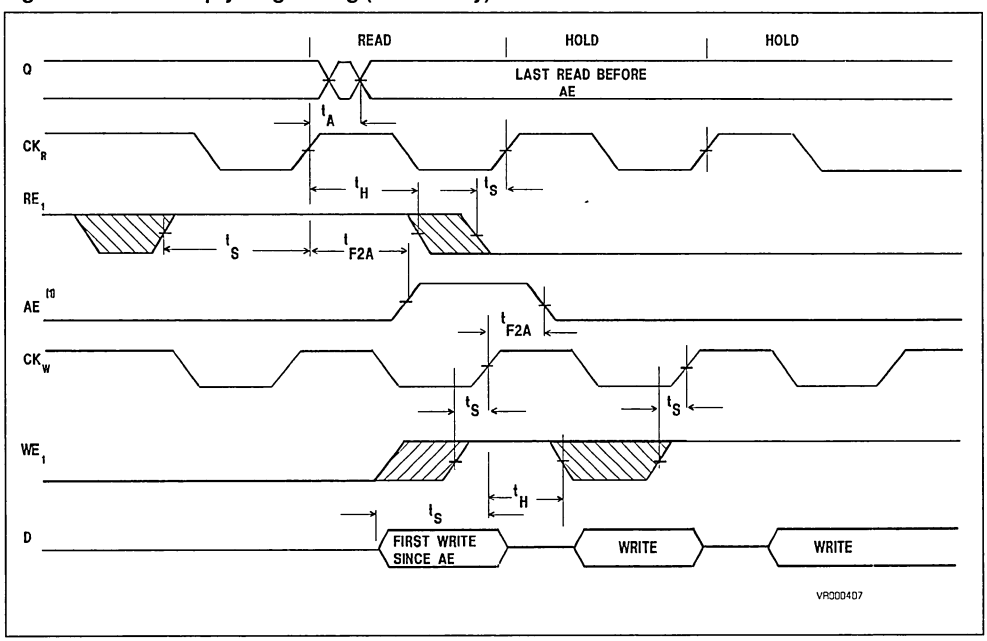
Note : t_{RSS} must be met if the device is read AND/OR write enabled (WE1, RE1 = High).

Figure 8. First Hold After Reset.



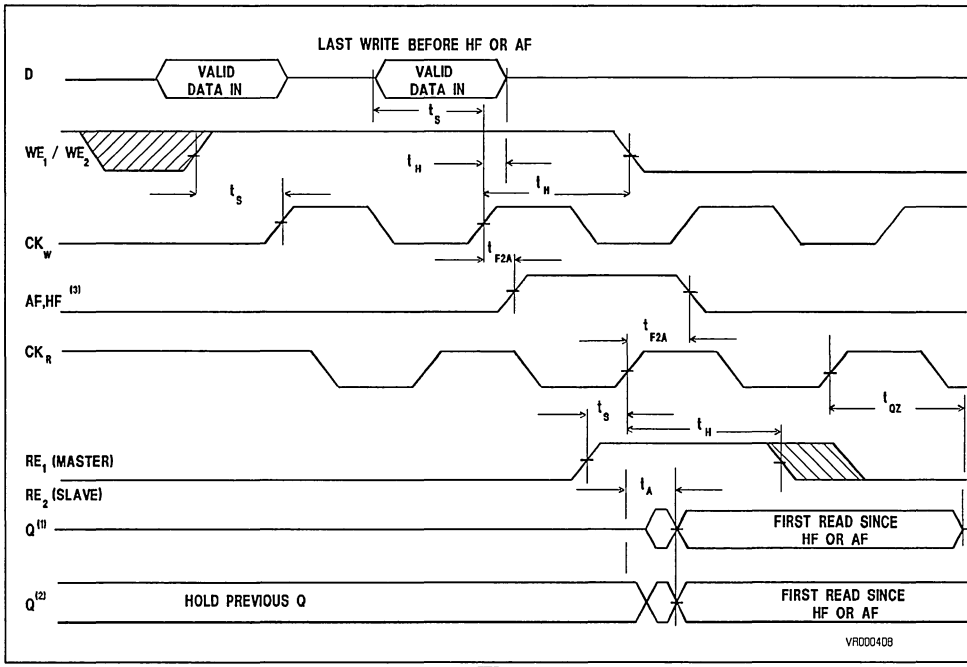
Note : A valid write operation is presumed between t_1 and t_2.

Figure 9. Almost Empty Flag Timing (4505M only).



Note : 1. This example does not show the hysterisis in the ALMOST FLAGS.

Figure 10. Almost Full, Half Full Flag Timing.



Notes : 1. Q outputs in Master/Slave Width Expansion (RE2 = $\overline{EF}$), or when using MK4505S Slave separately.
2. Q outputs in Master-to-Master Depth Expansion (RE1 with $\overline{EF}$ = HIGH), or when using the MK4505M separately.
3. This example does not show the hysterisis in the ALMOST FLAGS.

Gating Clock		Gating Operation	Flag Affected	Flag Transition	Read Locations Remaining to Empty	Write Locations Available to Full
CKR	CKW					
↑	-	READ	AE	↗	8*	1016
-	↑	WRITE	AE	↗	10	1014
↑	-	READ	AE	↘	9	1015
-	↑	WRITE	AE	↘	11	1013
↑	-	READ	AF	↗	1014	10
-	↑	WRITE	AF	↗	1016	8*
↑	-	READ	AF	↘	1013	11
-	↑	WRITE	AF	↘	1015	9
↑	-	READ	HF	↗	510	514
-	↑	WRITE	HF	↗	512	512*
↑	-	READ	HF	↘	509	515
-	↑	WRITE	HF	↘	511	513

Notes : *. Flag definition to the respective operation and clock.
1. All examples are given in reference to the flag transition point, in the direction shown, for the given clock edge and operation. The flag remains stable as long as the condition that set or cleared the flag exists in the device.
2. The table describes the number of the cycles that can be performed, including the next rising edge.
3. Remaining Read or Available Write locations at the flag transition point reflects the hysterisis inherent to the internal scheme that detects the flag status.
4. Asynchronous or simultaneous dual port operations at the flag transition point may result in a false flag status. When this occurs, the flag is evaluated and updated on the subsequent clock.

Figure 11. Simultaneous Write/Read Timing (4505M only).

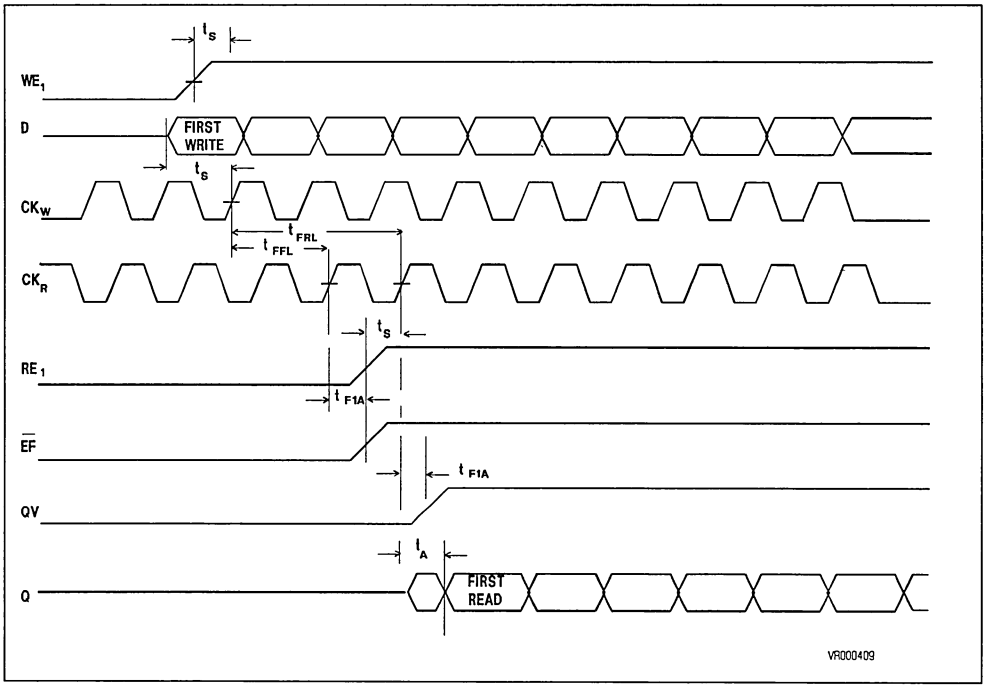
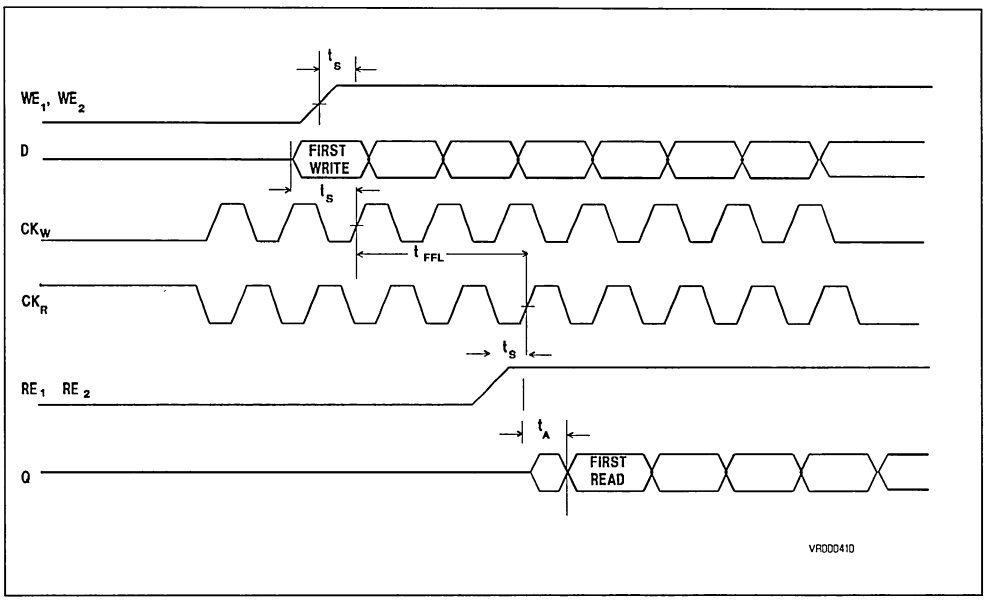


Figure 12.. Simultaneous Write/Read Timing (4505S only).



SIMULTANEOUS WRITE/READ TIMING

The Empty Flag ($\overline{EF}$) is guaranteed to clear (go HIGH) in response to the first rising edge of the read clock (CKR) to occur t_{FFL} (First Flag Latency) after a valid First Write (from the rising edge of CKW). Read clocks occurring less than t_{FFL} after a First Write may clear the $\overline{EF}$, but are not guaranteed (see Figure 10). As always, reads attempted in conjunction with an active Empty Flag are inhibited. Therefore, the next rising edge of CKR following t_{FFL} will produce the first valid read. This is the t_{FRL} (First Read Latency) pa-rameter, and must be observed for proper system operation with the latched $\overline{EF}$. Coming from an empty condition, the First Read operation should be accomplished by enabling RE1 no less than t_S before the rising edge of CKR at t_{FRL}. The Q outputs will present valid data t_A from the rising edge of CKR.

When using the MK4505S (Slave) separately, the user must observe the t_{FRL} (First Read Latency) parameter to ensure first-write-to-first-read valid data. Referring to Figure 12, the first rising edge of CKR to occur t_{FRL} after a First Write clock will guarantee valid data t_A from the rising edge of CKR. Read operations attempted before t_{FRL} is satisfied may result in reading RAM locations not yet written. Careful observance of t_{FRL} by the user is a must when using free running asynchronous read/write clocks on the MK4505S ; there is no automatic read and write protection circuitry in the Slave.

It should also be noted that the MK4505M/S has an expected "fall-through delay time" described as First Write data presented to the FIFO and clocked out to the outside world. This can be calculated as : $t_S + t_{FRL} + t_A$ (from Figure 11 or 12). Further occurring valid read clocks will present data to the Q outputs t_A from the rising edge of CKR.

WIDTH AND DEPTH EXPANSION

A single Master (MK4505M) is required for each 1K of depth configured. The number of Slaves that can be driven by a single Master is limited only by the effects of adding extra load capacitance (Write and Read Enable Input Capacitance) onto the Input Ready (DR), Output Valid (QV), Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$) outputs. However, even 40 bits of width (8 devices) results in only 40pf of loading, which corresponds to the amount of load called out in the AC Test Conditions. Additional loading will slow the flags down, but as long as Enable Set Up time (t_S) is met, slowing the flags has no negative consequences.

DEPTH EXPANSION HANDSHAKE PROTOCOL

The depth expansion handshake device connections are shown in Figure 13. The expansion interface signals can be considered transparent to the user, as long as the expansion clock continues to run. The Output Ready (QV) flag, and the Data Ready (DR) flag logic descriptions are detailed in the following charts. Since the expansion clock is the read clock for the sending FIFO, as well as the write clock for the receiving FIFO, these two signals prevent data loss during depth expansion applications where the receiving bank (bank B, Figure 13) goes full simultaneously as the sending bank goes empty (bank A, Figure 13).

Before Read Clock				Operation at CKR	After Read Clock		Note
RE1	$\overline{EF}$	QV	Reads Remaining		QV	Status	
X	0	X	0	Inhibit	0	Empty	1
0	1	1	≥ 1	Hold	0	Active	2
1	1	0	1	Read	1	Empty	3
1	1	X	≥ 2	Read	1	Active	4

Notes : 1. Whenever EF is active low, further attempted read cycles are inhibited.
2. QV is gated by RE1 such that the QV flag will be latched low t_{f1A} from the rising edge of CKR when RE1 is low. The RE1 input must meet the set-up time (t_S) prior to the read clock edge. QV does not logically allow or prevent a read operation.
3. Whenever RE1 is active high, QV will always follows the $\overline{EF}$ signal by one read clock cycle.
4. This condition displays a typical read operation when remaining memory locations (prior to the read operation) are from 2 to 1024. $\overline{EF}$ and QV continue to acknowledge that the FIFO has more data available.

Before Write Clock				Operation at CKW	After Write Clock		Note
WE1	$\overline{FF}$	DR	Write Available		DR	Status	
X	0	0	0	No-Op	0	Full	1
0	1	0	1	No-Op	1	Full-1	2
0	1	1	1	No-Op	0	Full-1	2
1	1	X	1	Write	0	Full	1
0	1	X	2	No-Op	1	Active	3
1	1	1	2	Write	0	Full-1	4
0	1	1	≥ 3	No-Op	1	Active	
1	1	1	≥ 3	Write	1	Active	5

Notes : 1. DR can be low only when the MK4505M is full or (full-1). Whenever the device goes full ($\overline{FF}$ = low), then DR will be latched low t_{F1A} from the same write clock edge (CKW) regardless of the logic state of the DR flag at the clock transition. Further attempted write operations are blocked since FF is low.

2. If DR changes logic states after the write clock, then this example reflects the condition when the MK4505M has one (1) memory location available (full-1). DR will presume the opposite logic state of the previous cycle for subsequent write clocks if WE1 is disabled (low) and one memory location is available. Whenever the MK4505M goes full ($\overline{FF}$ = low), DR will be latched low in the same clock cycle. (This is part of the Depth Expansion Protocol, and acts to notify the sending unit that space is available.) The DR flag does not logically allow or prevent a write operation.
3. If DR is a logic 1 before and after the write clock, then this example signifies that the available memory locations in the MK4505M are greater than or equal to 2, after the completed write operation.
4. During a valid write cycle, the DR flag will go inactive low t_{F1A} from the rising edge of CK_W if the write counter is (full-2) at the clock transition. This results is a (full-1) condition. (Refer to notes 1 and 2.)
5. This condition displays a typical write cycle, where available memory locations (prior to the write operation) are from 3 to 1024. DR and $\overline{FF}$ continue to acknowledge that the FIFO is ready to accept more data.

In summary, the QV flag follows the $\overline{EF}$ signal by one read clock cycle (in all instances) when RE1 is active high at the rising edge of CKR. Whenever RE1 is disabled (low), the QV flag will go low t_{F1A} from the rising edge of CKR. Of course, the RE1 input must satisfy the set-up time (t_S) prior to CKR. The QV flag does not enable or inhibit read operations. Read protection is provided by the EF signal.

The DR flag will go low one cycle prior to a full condition (full-1), or DR will go high at (full-2) from the rising edge of CKW. However, if WE1 is disabled (low), and the device has one location available, then DR will toggle each subsequent write cycle until full. This way the device notifies the sending unit that at least one more byte of data can be accepted. When the device goes full, the DR flag will be latched low t_{F1A} from the clock edge (during the same write cycle), regardless of its previous logic state. As with all valid write cycles, the WE1 input must satisfy the set-up time (t_S) prior to CKW. The DR flag does not enable or inhibit write operations. Write protection is provided by the $\overline{FF}$ signal.

WIDTH AND DEPTH EXPANSION EXAMPLES

The width and depth expansion interface timing diagrams (Figures 14 and 15) are in reference to the width and depth expansion schematic in Figure 13 (For simplicity all clocks have the same frequency and transition rate).

Example 1 - First Write Since Empty - Reading the timing diagram from the top left to bottom right, one can determine that figure 13 illustrates the effects of the first WRITE/READ cycles from an EMPTY array of FIFOs. Both of the $\overline{EF}$ pins are initially low ($\overline{EF_X}$, $\overline{EF}$ and RE2). As data is written into Bank A, the expansion clock reads data from Bank A and writes it to Bank B, the interface $\overline{EF}$ ($\overline{EF}$ and RE2) and the external $\overline{EF}$ ($\overline{EF_X}$) go inactive (logic 1) while data is shifted through the FIFO array from Bank A through Bank B to the external output (Q0 - Q4). The $\overline{EF}$ logic goes valid (logic 0) once data is shifted out of its respective bank.

Example 2 - First Read Since Full - Reading the timing diagram from the bottom left to top right, one can determine that figure 15 illustrates the effects of the first READs from a FULL array of FIFOs. As data is read out of the system (Q0 - Q4), it allows Bank B to receive data (Q_{EXP}) shifted from Bank A. As Bank B shifts data out via Q0 - Q4, allowing Bank A to shift data into Bank B, both banks will show a cleared $\overline{FF}$ status (logic 1) on the expansion $\overline{FF}$ ($\overline{FF}$ and WE2) as well as the internal $\overline{FF}$ ($\overline{FF_X}$). When Bank A is no longer considered FULL, Data In from the system (D0 - D4) is now written into Bank A. The FIFO array is again completely Full.

APPLICATION

The MK4505 operates from a 5V supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK4505 can also interface to 5V CMOS on all inputs and outputs.

Since very high frequency current transients will be associated with the operation of the MK4505, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. A high frequency decoupling capacitor should be placed next to each FIFO. The capacitor should be 0.1µF or larger. Also, a pull-up resistor in the range of 1KΩ is recommended for the $\overline{\text{RESET}}$ input pin to improve proper operation.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10Ω to 33Ω often prove most suitable.

Figure 13. MK4505M/S 2K x 10 Width and Depth Expansion Schematic.

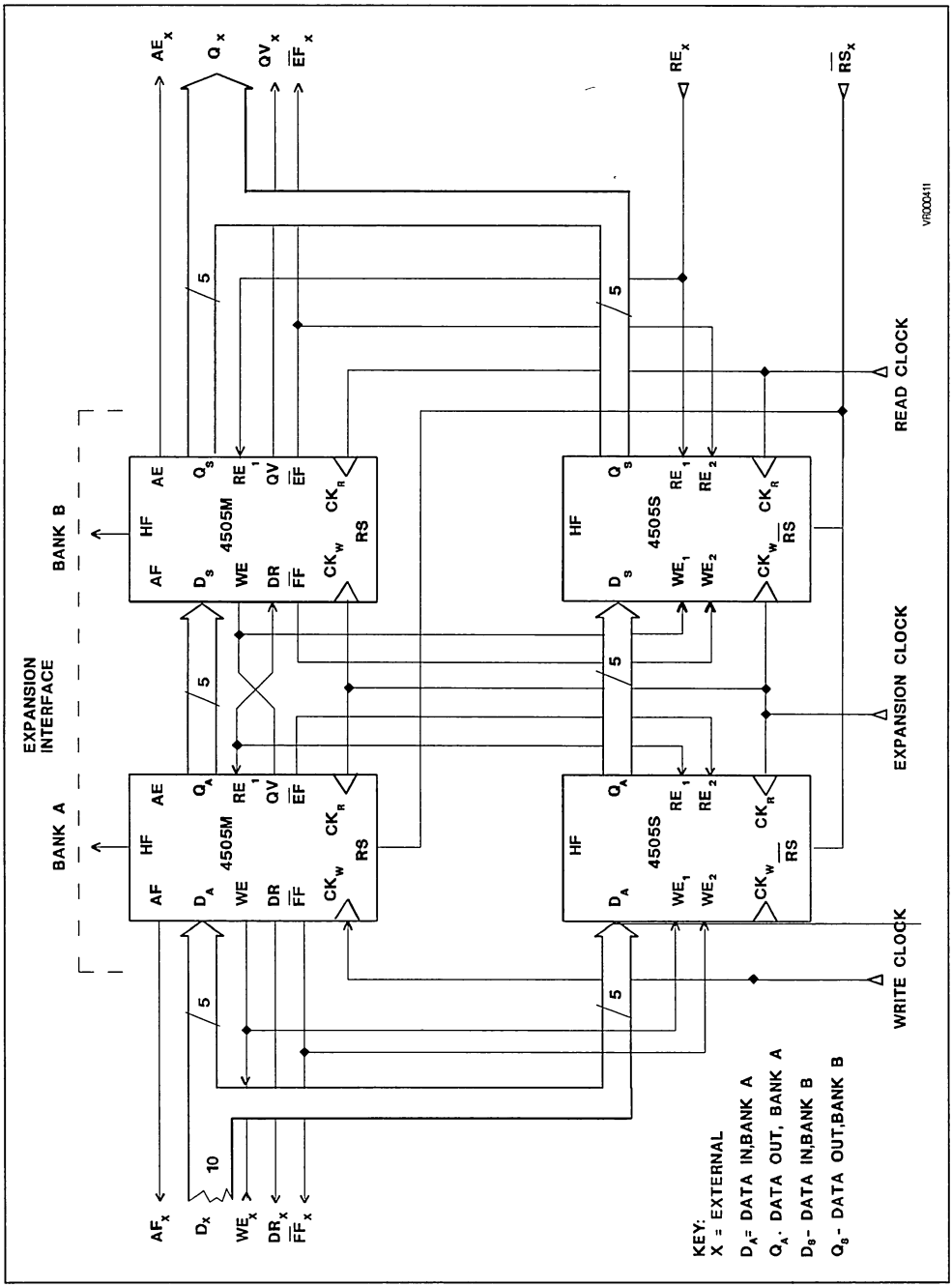
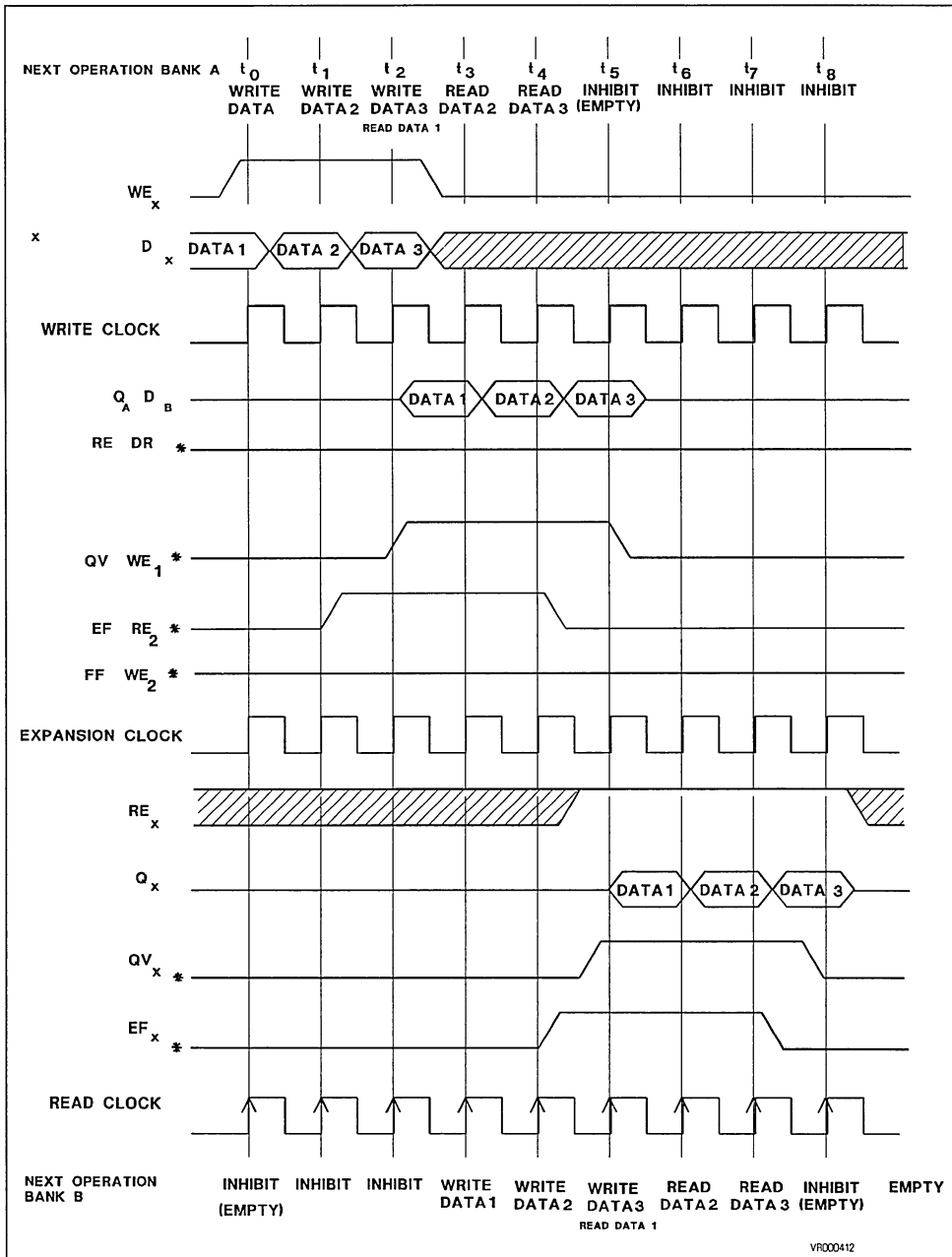
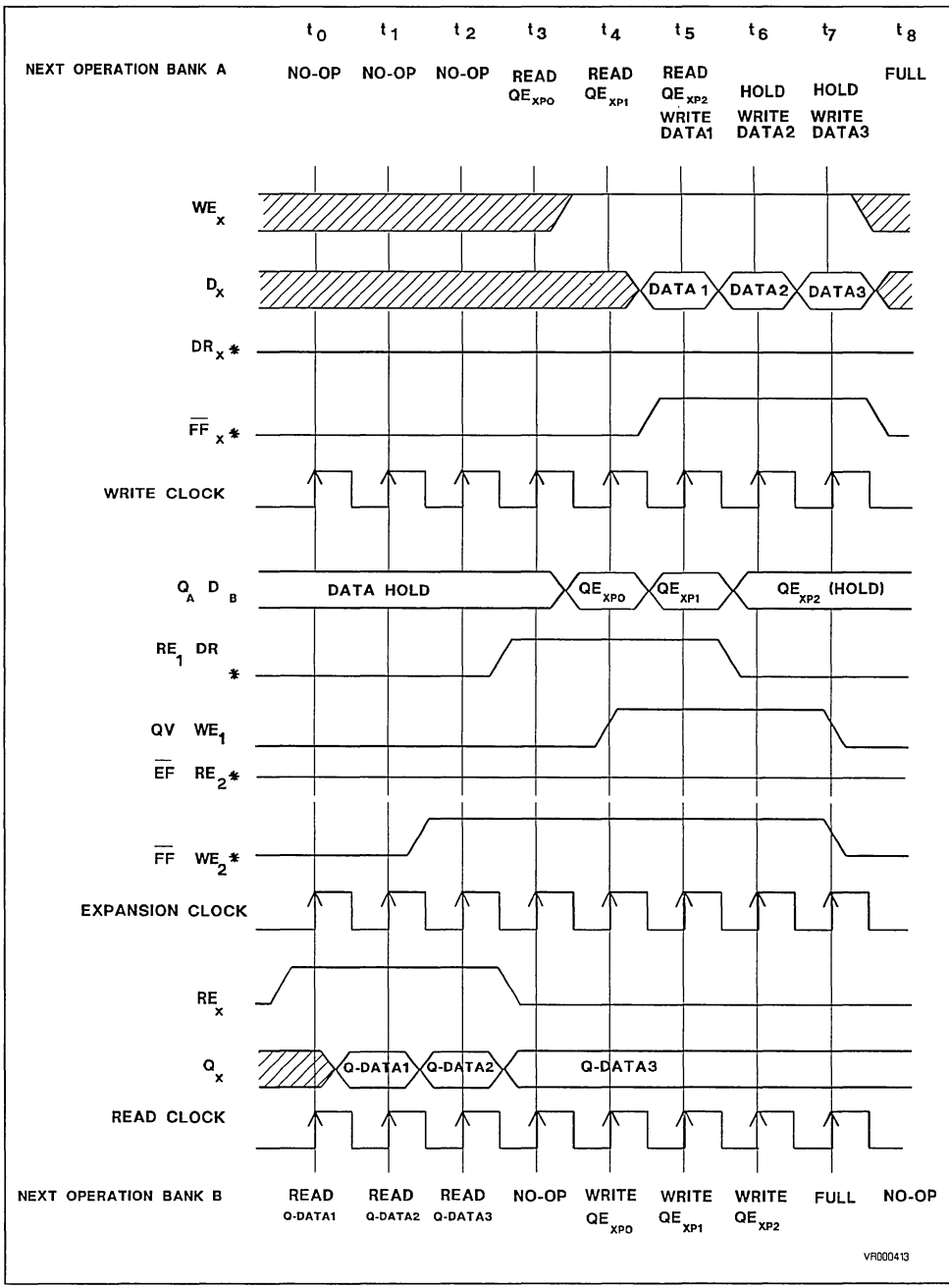


Figure 14. Example 1 - Width and Depth Expansion Interface Timing.



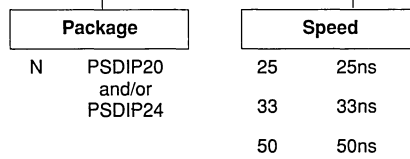
Note : *. Example begins with both banks empty, as status flags indicate.

Figure 15. Example 2 - Width and Depth Expansion Interface Timing.



ORDERING INFORMATION

Example: MK4505M N 25



Package		Speed	
N	PSDIP20 and/or PSDIP24	25	25ns
		33	33ns
		50	50ns

In a System using both M4505M and M4505S, parts should be ordered individually.

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

CMOS 512 x 9 BiPORT FIFO

- FIRST-IN, FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE 512 x 9 ORGANIZATION
- LOW POWER HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- BIDIRECTIONAL APPLICATIONS
- FULLY EXPANDABLE BY WORD WIDTH OR DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HIGH PERFORMANCE

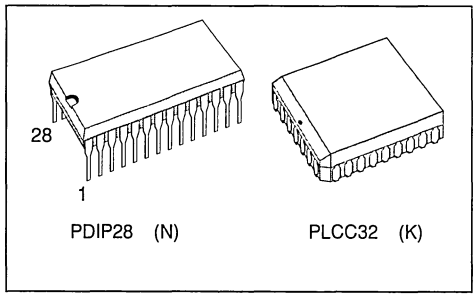
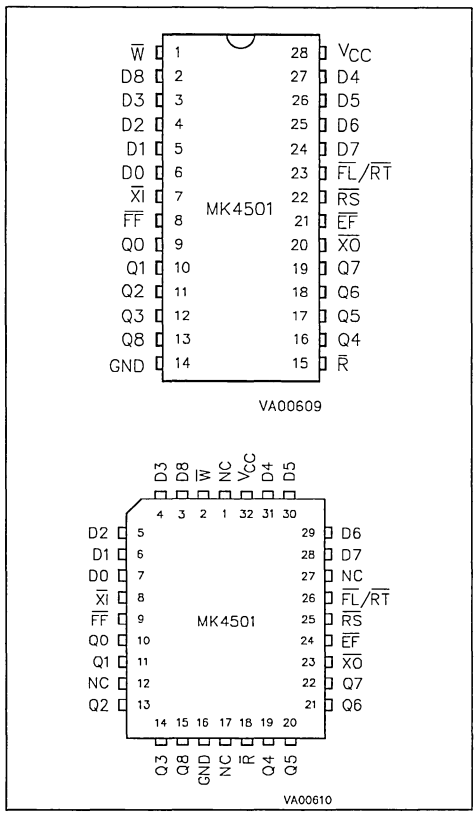


Figure 1. Pin Connections



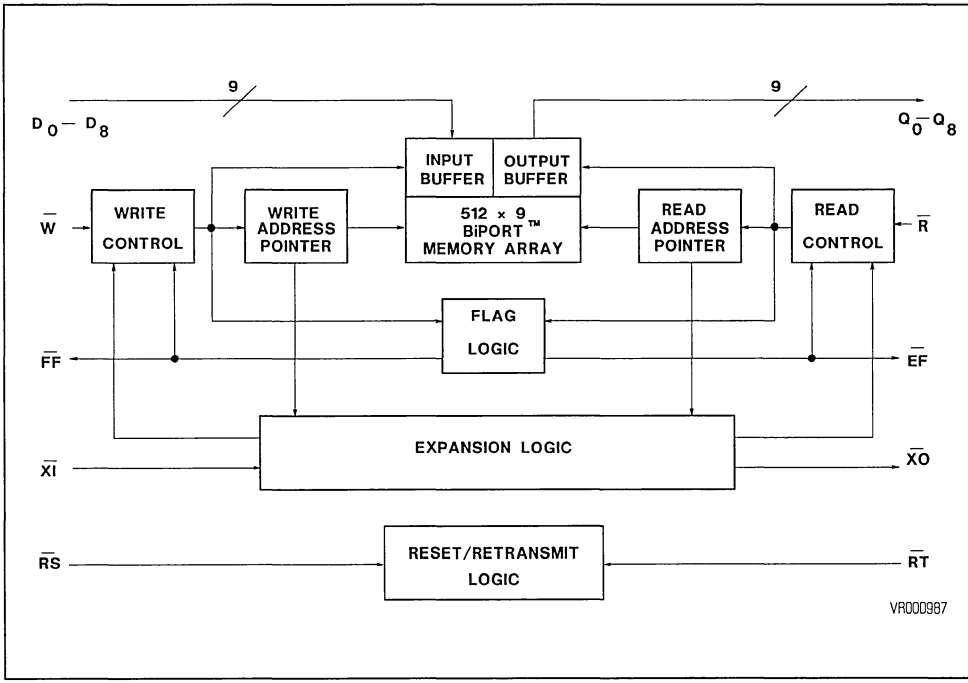
DESCRIPTION

The MK4501 is a BiPORT™ FIFO memory, which utilizes special two-port cell tech- niques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4501 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to

PIN NAMES

$\overline{W}$	Write
$\overline{R}$	Read
$\overline{RS}$	Reset
D0-D8	Data Inputs
Q0-Q8	Data Outputs
GND	Ground
$\overline{XI}$	Expansion Input
$\overline{XO}$	Expansion Output
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
$\overline{FL/RT}$	First Load / Retransmit
V_{CC}/GND	5 Volts/Ground
NC	Not Connected

Figure 2. Block Diagram



INTRODUCTION (Continued)

prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK4501 employs a memory-based architecture wherein a byte written into the device does not "ripple-through". Instead, a byte written into the MK4501 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired.

Twin address pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. Address pointers automatically loop back to address zero after reaching address 511. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the indi-vidual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The 4501 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the MK4501 allows connecting the read, write, data in, and data out lines of the MK4501s in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins as appropriate (see the Expansion Timing section for a more complete discussion).

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{CC}	Supply Voltage	4.5	5	5.5	V	3
GND	Ground	0	0	0	V	
V_{IH}	Logic "1" All Inputs	2.0		V_{CC} + 1	V	3
V_{IL}	Logic "0" All Inputs	–0.3		0.8	V	3, 4

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
I_{IL}	Input Leakage Current (Any Input)			± 1	µA	5
I_{OL}	Output Leakage Current			± 10	µA	6
V_{OH}	Output Logic 1 Voltage (I_{OUT} = –1mA)	2.4			V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = 4mA)			0.4	V	3
I_{CC1}	Average V_{CC} Power Supply Current			80	mA	7
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})			8	mA	7
I_{CC3}	Power Down Current (all Inputs ≥ V_{CC} – 0.2V)			500	µA	7

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
C_I	Capacitance on Input Pins			7	pF	
C_O	Capacitance on Output Pins			12	pF	8

Notes :

1. Pulse widths of less than minimum values are not valid.
2. Measured using output load shown in figure Output Load Circuit.
3. All voltages are referenced to ground.
4. 1.5 volt negativeundershoots are allowed for 10ns, once per cycle.
5. Measured with $0.4V \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.4V \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.

ABSOLUTE MAXIMUM RATINGS

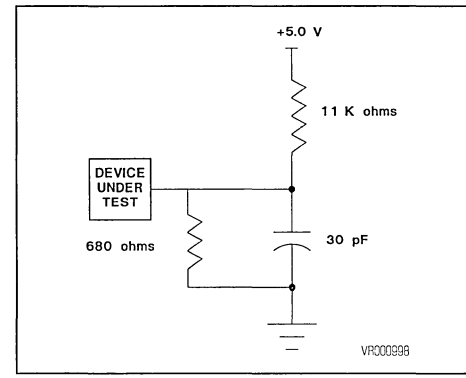
Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	–0.5 to +7	V
T_A	Operating Temperature T_A (ambient)	0 to 70	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current per Pin	20	mA

Note : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

AC TEST CONDITIONS

Input Levels	GND to 3V
Transition Times	5ns
Input Signal Timing Reference Level	1.5V
Output Signal Timing Reference Level	0.8V and 2.2V
Ambient Temperature	0°C to 70°C
V_{CC}	5V ± 10%

Figure 3. Equivalent Output Load Circuit



READ MODE

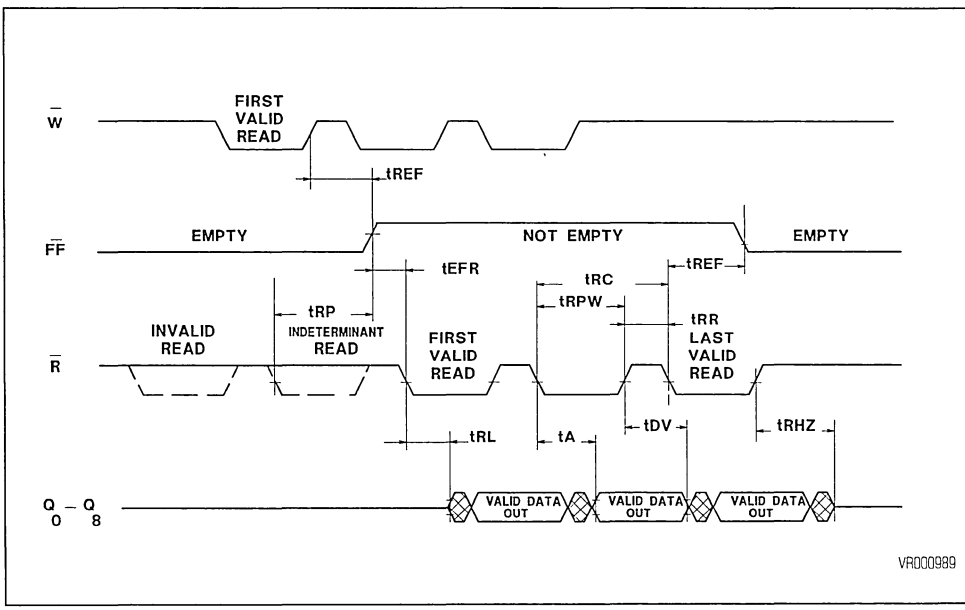
The MK4501 initiates a Read Cycle (see Figure 4a) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not set. In the Read mode of operation, the MK4501 provides a fast access to data from 9 of 4608 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent READ operation, provided that a second WRITE has not been completed (see figure 4B). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

AC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	80		100		120		140		175		235		ns	
t_A	Access Time		65		80		100		120		150		200	ns	2
t_{RR}	Read Recovery Time	15		20		20		20		25		35		ns	
t_{RPW}	Read Pulse Width	65		80		100		120		150		200		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		0		ns	2
t_{DV}	Data Valid from High $\overline{R}$	5		5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		25		25		25		35		50		60	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		60		75		95		115		145		195	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read	10		10		10		10		10		10		ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		60		75		95		110		140		190	ns	2
t_{RPI}	Read Protect Indeterminant		35		35		35		35		35		35	ns	2

Figure 4A. Read and Empty Flag Waveforms



WRITE MODE

The MK4501 initiates a Write Cycle (see Figure 4B) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not set. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK4501 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 4A). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

AC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	80		100		120		140		175		235		ns	
t_{WPW}	Write Pulse Width	65		80		100		120		150		200		ns	1
t_{WR}	Write Recovery Time	15		20		20		20		25		35		ns	
t_{DS}	Data Set Up Time	20		25		35		40		50		65		ns	
t_{DH}	Data Hold Time	10		10		10		10		10		10		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		60		75		95		115		145		195	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write	10		10		10		10		10		10		ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		60		75		95		110		140		190	ns	2

Figure 4B. Write and Full Flag Waveforms

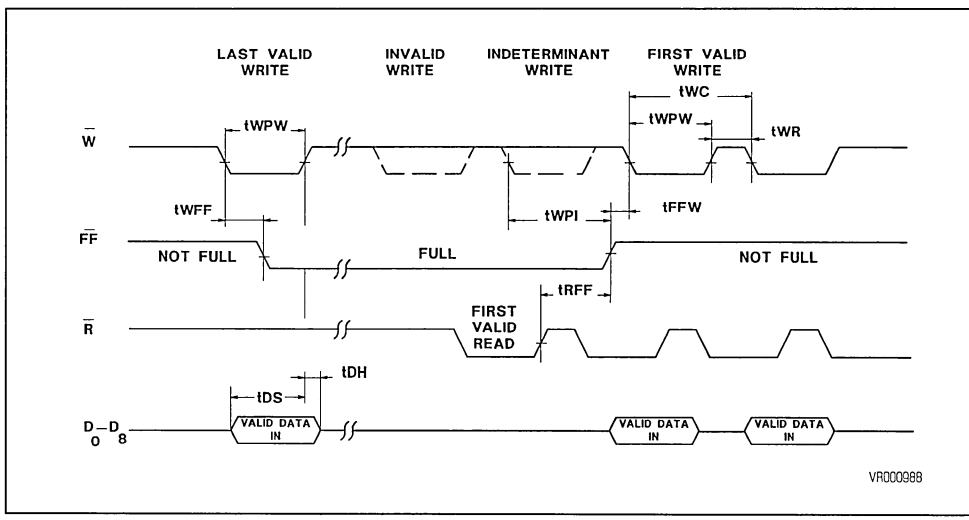


Figure 5B. Write/Read to Empty Flag Waveforms

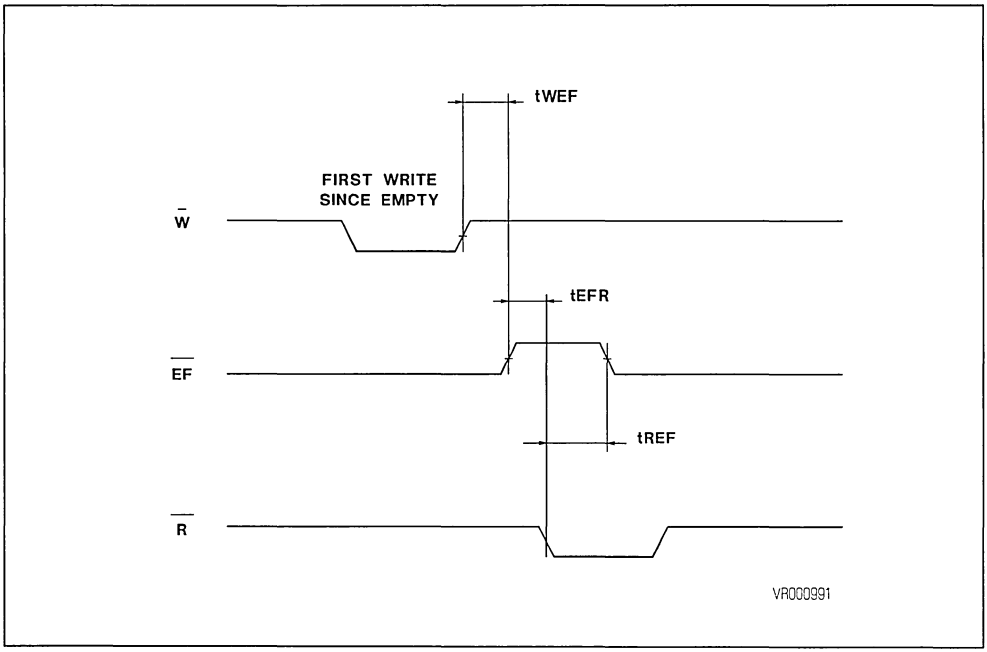
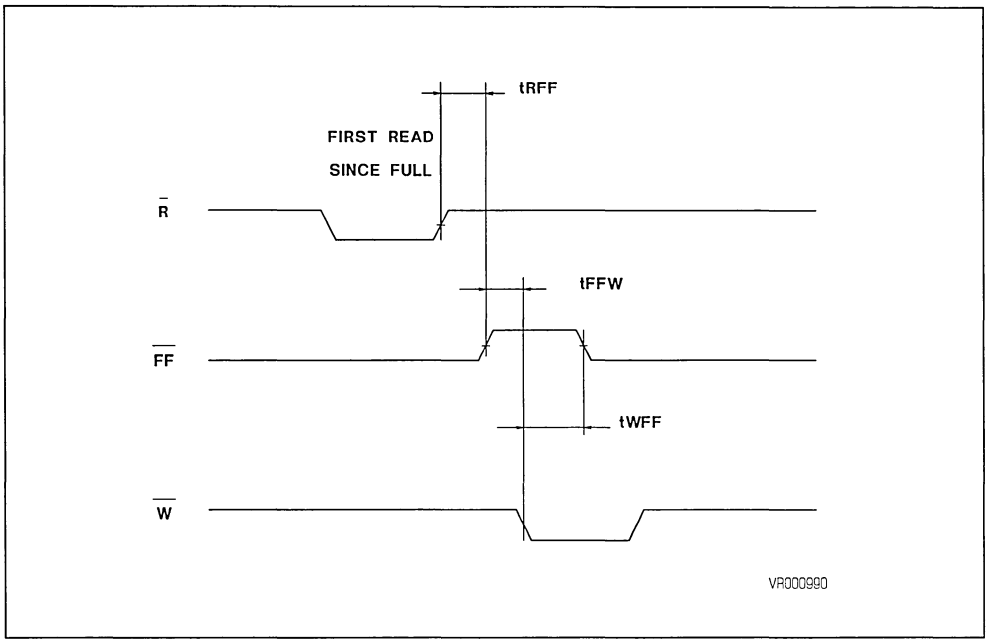


Figure 5B. Read/Write to Full Flag Waveforms



RESET

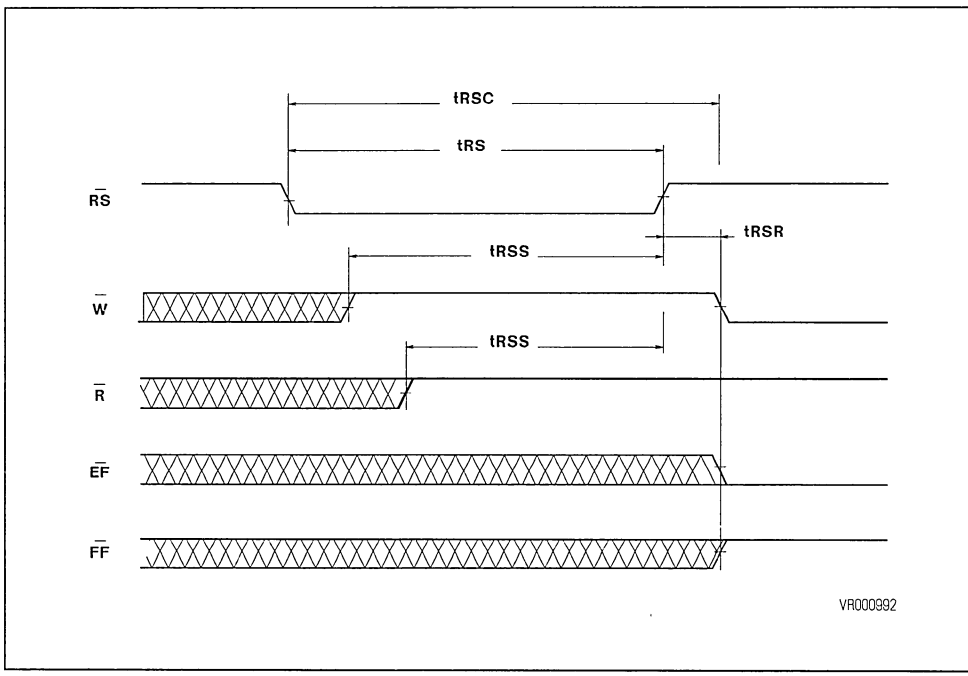
The MK4501 is reset (see Figure 6) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a Write operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	80		100		120		140		175		235		ns	
t_{RS}	Reset Pulse Width	65		80		100		120		150		200		ns	1
t_{RSR}	Reset Recovery Time	15		20		20		20		25		35		ns	
t_{RSS}	Reset Set Up Time	45		60		80		100		130		180		ns	

Figure 6. Reset Waveforms



Note : $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

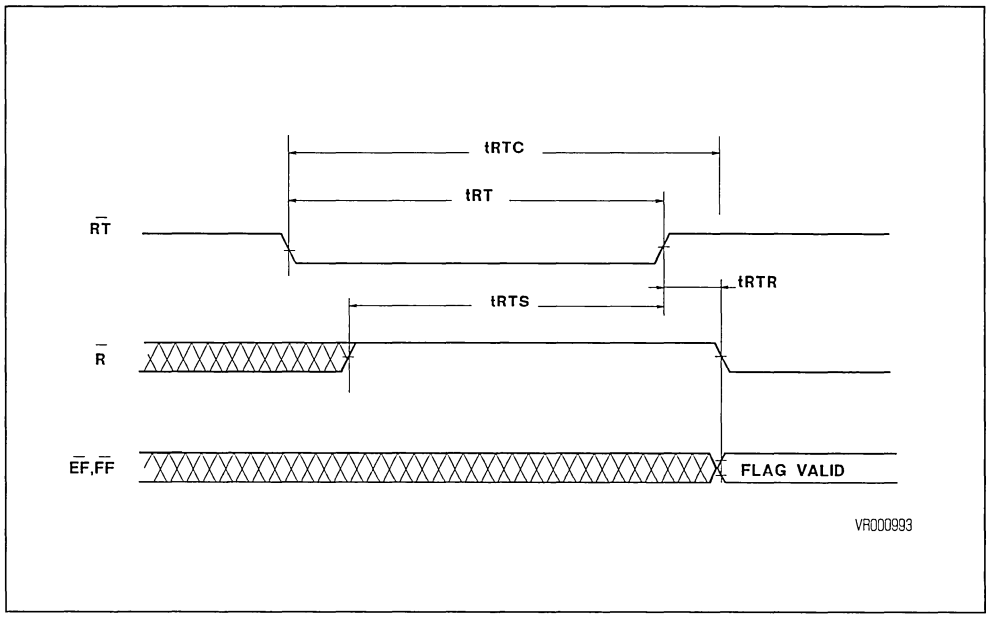
RETRANSMIT

The MK4501 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (see Figure 7).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 512 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 7. Retransmit Waveforms



Note : $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	80		100		120		140		175		235		ns	
t_{RT}	Retransmit Pulse Width	65		80		100		120		150		200		ns	1
t_{RTR}	Retransmit Recovery Time	15		20		20		20		25		35		ns	

SINGLE DEVICE CONFIGURATION

A single MK4501 may be used when application requirements are for 512 words or less. The MK4501 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 8).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 18-bit word width by using two MK4501s. Any word width can be attained by adding additional MK4501s.

Figure 8. A Single 512 x 9 FIFO Configuration

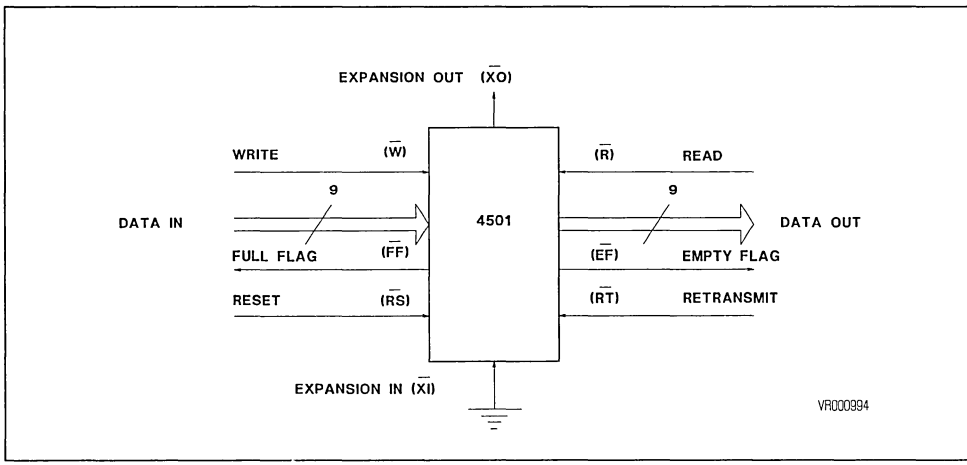
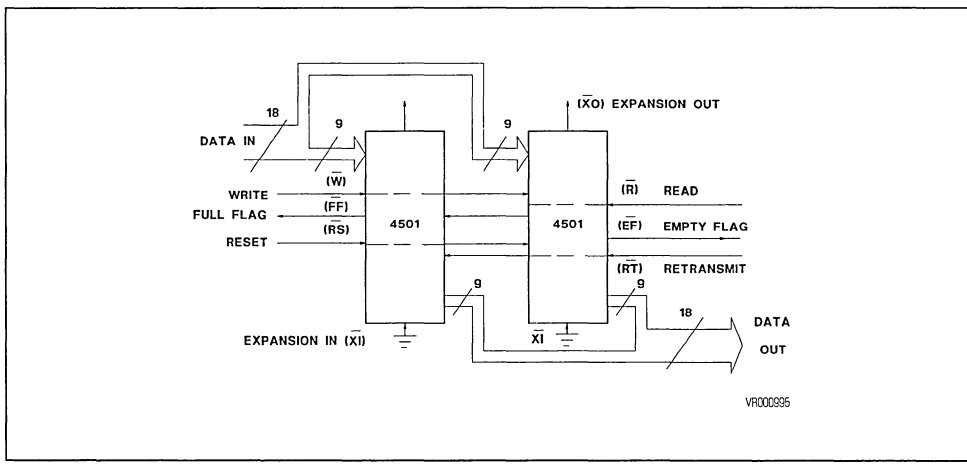


Figure 9. A 512 x 18 FIFO Configuration (Width Expansion)



Note : Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

DEPTH EXPANSION (Daisy Chain)

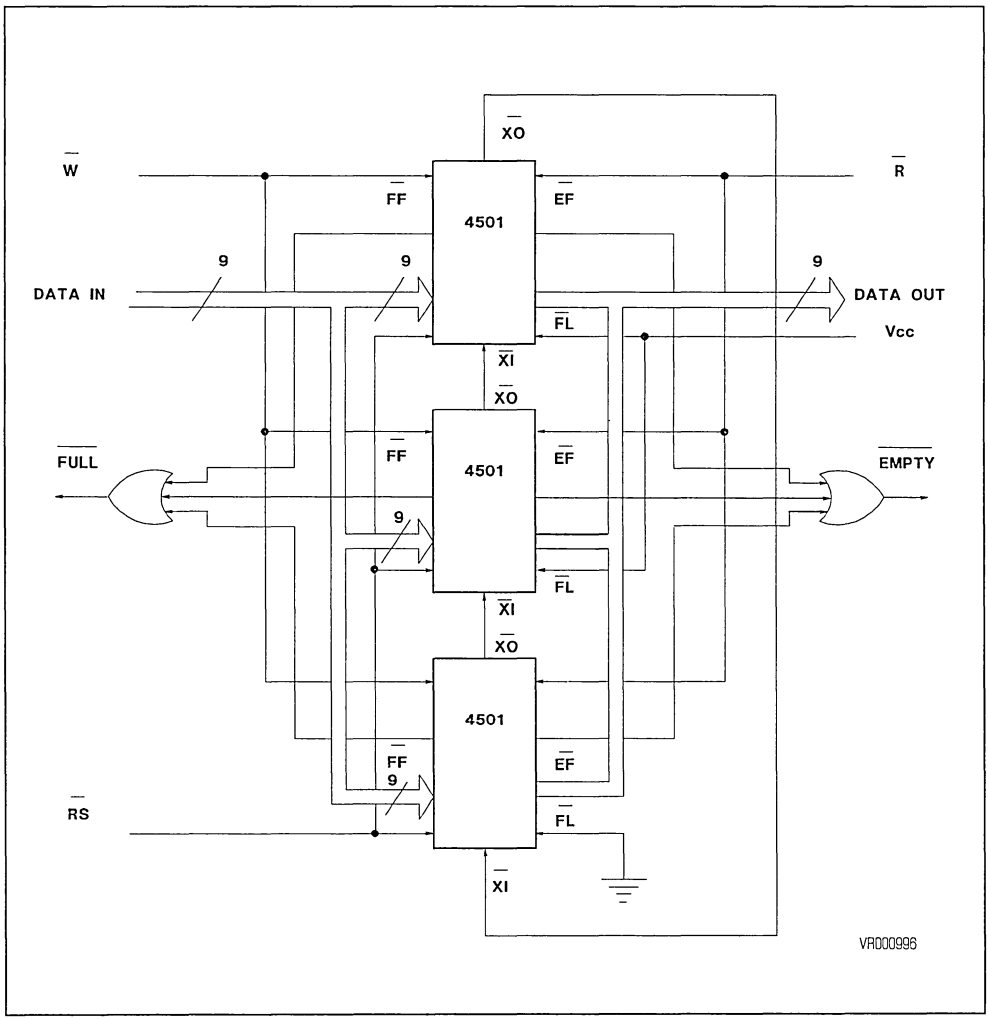
The MK4501 can easily be adapted to applications when the requirements are for greater than 512 words. Figure 10 demonstrates Depth Expansion using three MK4501s. Any depth can be attained by adding additional MK4501s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all FFs (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The MK4501 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not valid in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.

Figure 10. A 1536 x 9 FIFO Configuration (depth expansion)

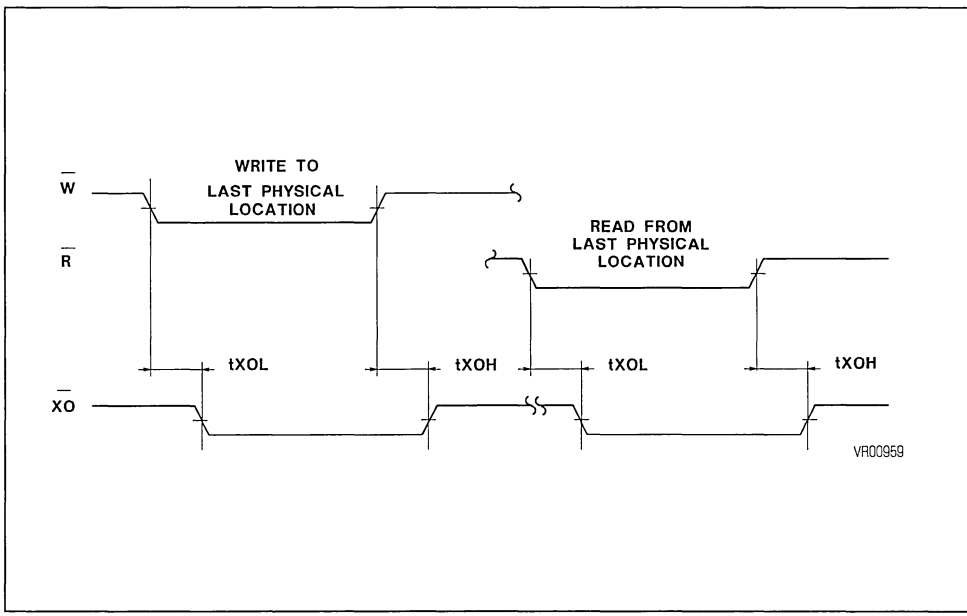


EXPANSION TIMING

Figures 11 and 12 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. In as much as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them ; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

Figure 11. Expansion Out Timing Waveforms

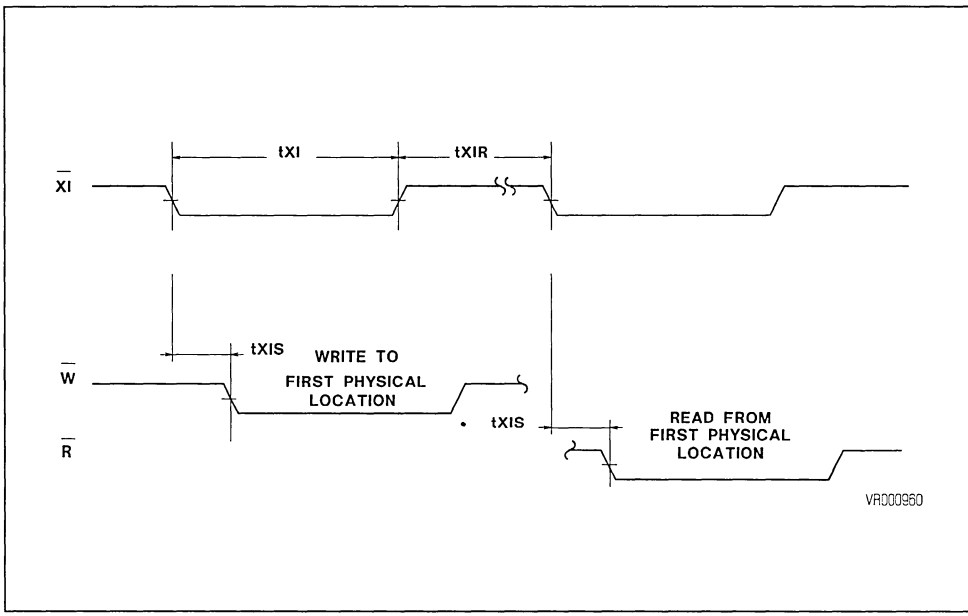


AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XOL}	Expansion Out Low		55		70		75		90		115		150	ns	
t_{XOH}	Expansion Out High		60		80		90		100		125		155	ns	

When in Depth Expansion mode, a given MK4501 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK4501 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

Figure 12. Expansion In Timing Waveforms



AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	60		75		95		115		145		195		ns	1
t_{XIR}	Expansion In Recovery Time	15		20		20		20		25		35		ns	
t_{XIS}	Expansion In Setup Time	25		30		45		50		60		85		ns	

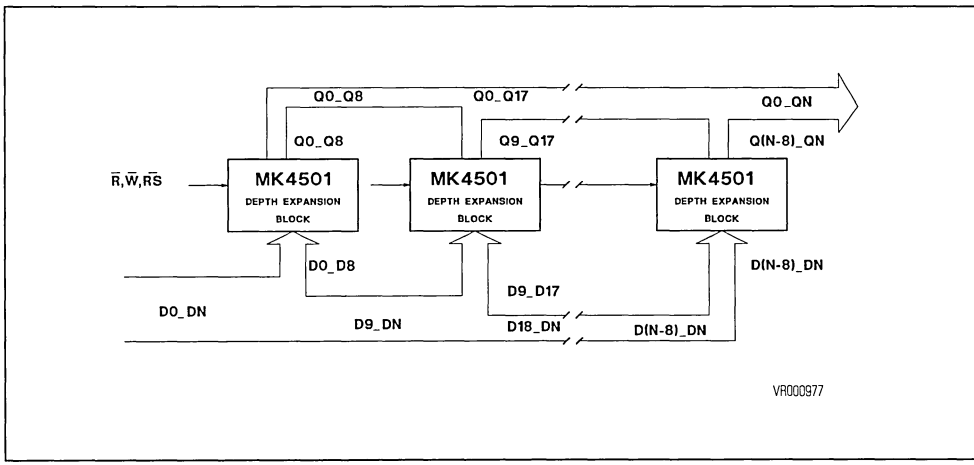
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 13).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK4501s, as shown in Figure 14. Care must be taken to ensure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used ; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

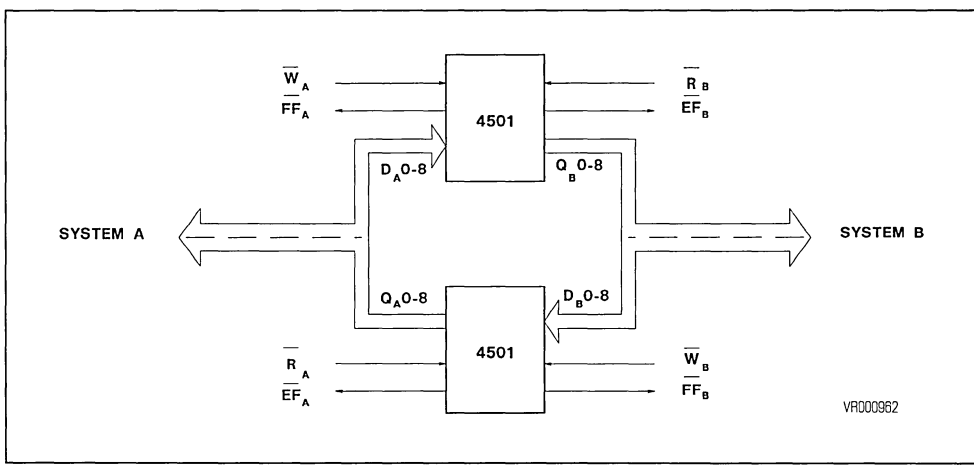
Figure 13. Compound FIFO Expansion Configuration



Notes :

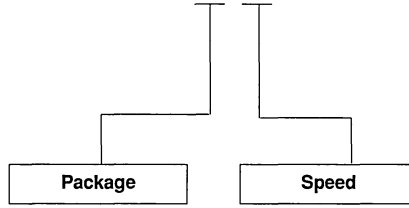
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag operation see WIDTH EXPANSION Section and Figure 9.

Figure 14. Bidirectional FIFO Application



ORDERING INFORMATION

Example: MK4501 N 65



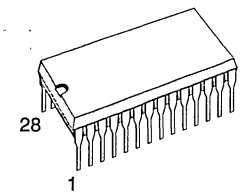
Package		Speed	
N	PDIP28	65	65ns
K	PLCC32	80	80ns
		10	100ns
		12	120ns
		15	150ns
		20	200ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.

CMOS 2K x 9 BiPORT FIFO

- FIRST-IN, FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE 2048 x 9 ORGANIZATION
- LOW POWER HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- BI-DIRECTIONAL APPLICATIONS
- FULLY EXPANDABLE BY WORD WIDTH OR DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HIGH PERFORMANCE
- HALF FULL FLAG IN SINGLE DEVICE MODE



PDIP28 (N)

DESCRIPTION

The MK4503 is a BiPORT™ FIFO memory, which utilizes special two-port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asyn-chronous Read/Write operations, full, half full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4503 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals).

PIN NAMES

$\overline{W}$	Write
$\overline{R}$	Read
$\overline{RS}$	Reset
$\overline{FL/RT}$	First Load / Retransmit
D0-D8	Data Inputs
Q0-Q8	Data Outputs
$\overline{XI}$	Expansion Input
$\overline{XO/HF}$	Expansion Output / Half Full Flag
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
V_{CC}	5 Volts
GND	Ground
NC	Not Connected

Figure 1. Pin Connection

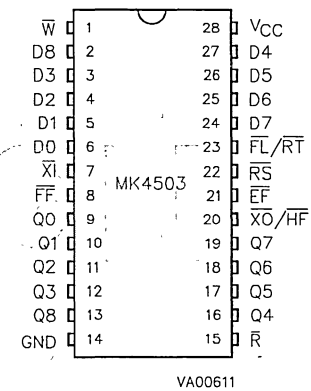
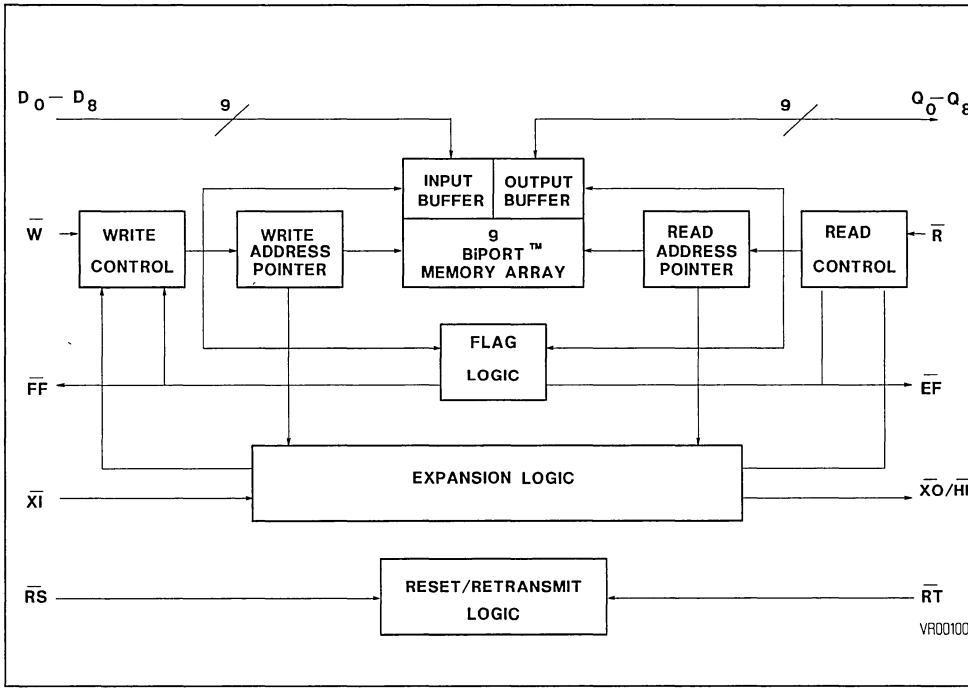


Figure 2. Block Diagram



DESCRIPTION (Continued)

The full, half full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK4503 employs a memory-based architecture wherein a byte written into the device does not "Ripple-Through". Instead, a byte written into the MK4503 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Twin internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

The address pointers automatically loop back to address zero after reaching address 2047. The empty/half full and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The 4503 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the MK4503 allows connecting the read, write, data in, and data out lines of the MK4503s in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to GND	–0.5 to +7	V
T_A	Ambiant Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current per Pin	20	mA

Note : Stresses above those listed under "Absolute Maximum Ratings" may be cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device.

RECOMMENDED DC OPERATING CONDITIONS
($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5	5.5	V	3
GND	Ground	0	0	0	V	
V_{IH}	Logic "1" Voltage all Inputs	2.2		V_{CC} + 0.3	V	3, 9
V_{IL}	Logic "0" Voltage all Inputs	–0.3		0.8	V	3, 4, 9

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
I_{IL}	Input Leakage Current (any input)			± 1	µA	5
I_{OL}	Output Leakage Current			± 10	µA	6
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -1mA$	2.4			V	3
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 4mA$			0.4	V	3
I_{CC1}	Average V_{CC} Power Supply Current			120	mA	7
I_{CC2}	Average Standby Current ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH}$)			12	mA	7
I_{CC3}	Power Down Current (all inputs ≥ V_{CC} –0.2V)			4	µA	7

CAPACITANCE

(T_A = 25°C, f = 1 MHZ)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
C_I	Capacitance on Input Pins			7	pF	
C_O	Capacitance on Output Pins			12	pF	8

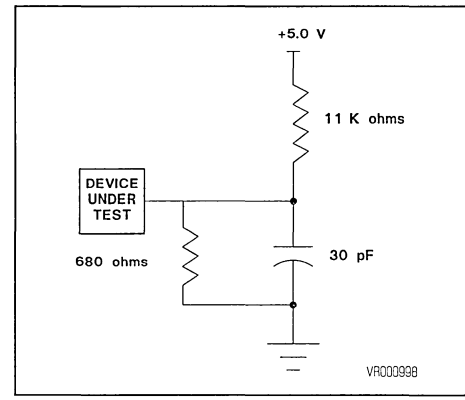
Notes :

1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Circuit.
3. All voltages are referenced to ground.
4. - 1.5 volt undershoots are allowed for 10ns once per cycle.
5. Measured with $0.0 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.0 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.
9. Input levels tested at 500ns cycle time.

AC TEST CONDITIONS

Input Levels	GND to 3V
Transition Times	5ns
Input Signal Timing Reference Level	5V
Output Signal Timing Reference Level	0.8V and 2.2V
Ambient Temperature	0°C to 70°C
V_{CC}	5V ± 10%

Figure 3. Equivalent Output Load Circuit

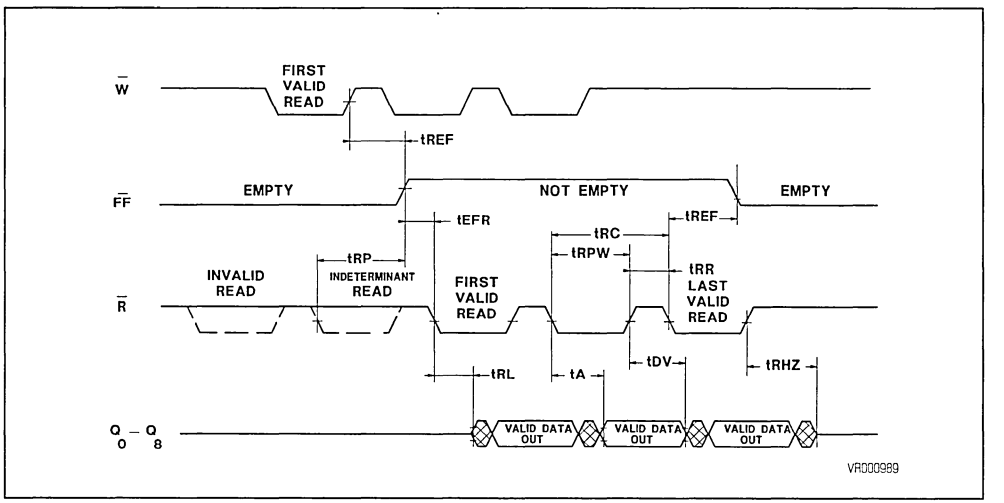


READ MODE

The MK4503 initiates a Read Cycle (see Figure 4) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the MK4503 provides a fast access to data from 9 of 18432 locations in the static storage array. The data is accessed on a FIFO basis independent of any on-going WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent READ operation, provided that a second WRITE has not been completed (see Figure 6B). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

Figure 4. Read And Empty Flag Waveforms



AC ELECTRICAL CHARACTERISTICS

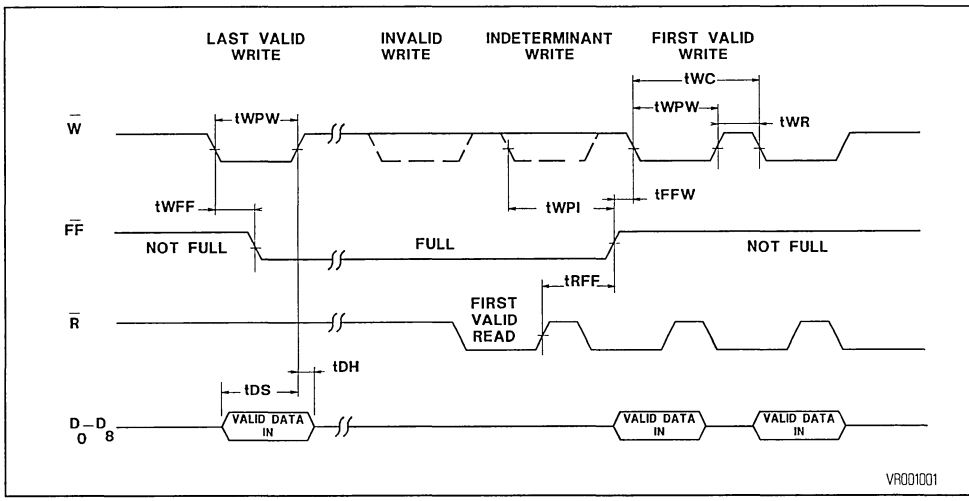
($0°C \leq T_A \leq +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	80		100		120		140		175		235		ns	
t_A	Access Time		65		80		100		120		150		200	ns	2
t_{RR}	Read Recovery Time	15		20		20		20		25		35		ns	
t_{RPW}	Read Pulse Width	65		80		100		120		150		200		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		25		25		25		35		50		60	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		60		75		95		115		145		195	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read	10		10		10		10		10		10		ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		60		75		95		110		140		190	ns	2
t_{RPI}	Read Protect Indeterminant		35		35		35		35		35		35	ns	2

WRITE MODE

The MK4503 initiates a Write Cycle (see Figure 5) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK4503 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 6A). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

Figure 5. Write And Full Flag Waveforms



AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	80		100		120		140		175		235		ns	
t_{WPW}	Write Pulse Width	65		80		100		120		150		200		ns	1
t_{WR}	Write Recovery Time	15		20		20		20		25		35		ns	
t_{DS}	Data Set-Up Time	30		40		40		40		50		65		ns	
t_{DH}	Data Hold Time	10		10		10		10		10		10		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		60		70		95		115		145		195	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write	10		10		10		10		10		10		ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		60		70		95		110		140		190	ns	2
t_{WPI}	Write Protect Indeterminant		35		35		35		35		35		35	ns	2

Figure 6A. Read/Write To Full Flag Waveforms

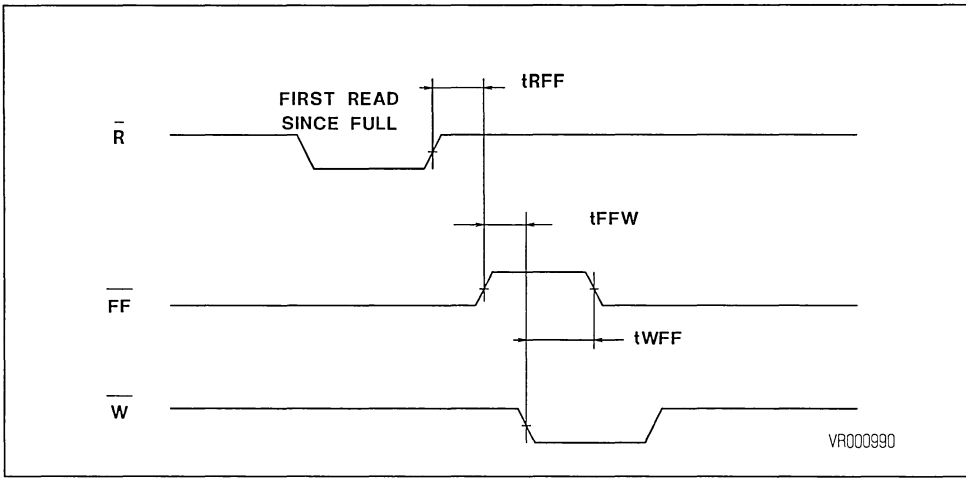
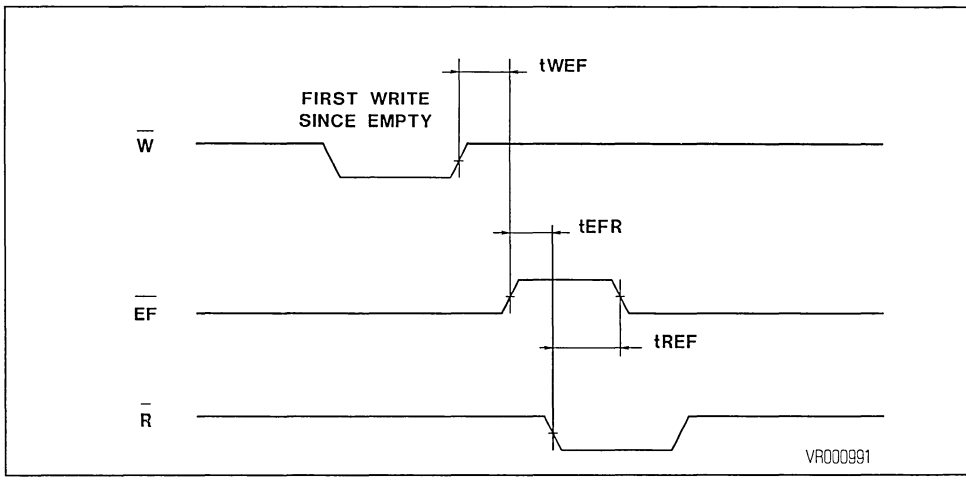


Figure 6B. Write/Read To Empty Flag Waveforms

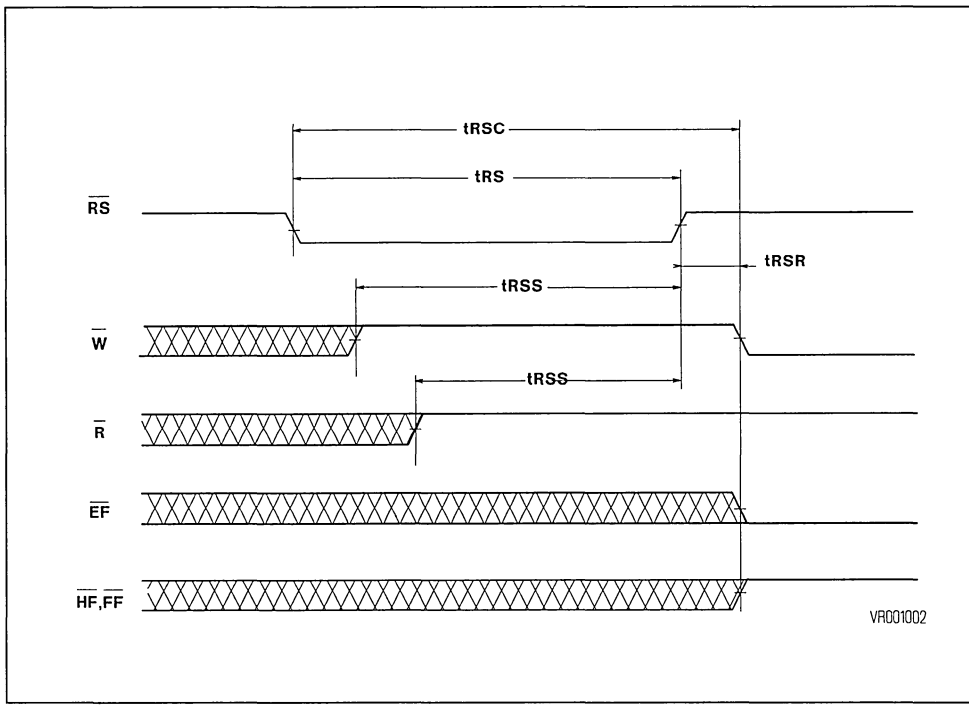


RESET

The MK4503 is reset (see Figure 7) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a Write operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

Figure 7. Reset Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	80		100		120		140		175		235		ns	
t_{RS}	Reset Pulse Width	65		80		100		120		150		200		ns	1
t_{RSR}	Reset Recovery Time	15		20		20		20		25		35		ns	
t_{RSS}	Reset Set-Up Time	45		60		80		100		130		180		ns	

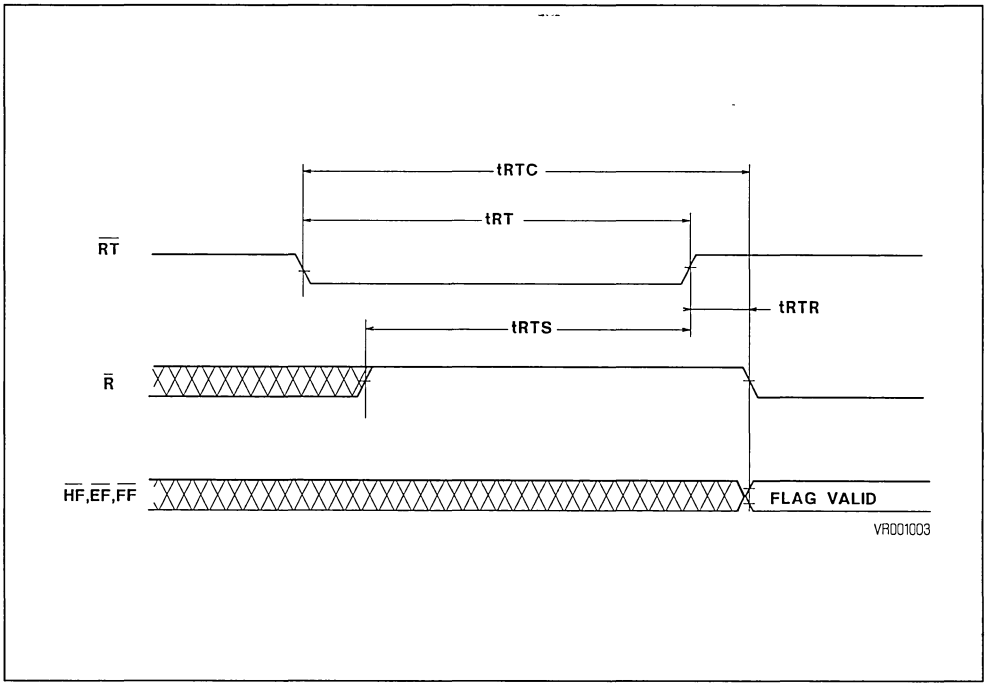
RETRANSMIT

The MK4503 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (See Figure 8).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 2048 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 8. Retransmit Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	80		100		120		140		175		235		ns	
t_{RS}	Retransmit Pulse Width	65		80		100		120		150		200		ns	1
t_{RTR}	Retransmit Recovery Time	15		20		20		20		25		35		ns	
t_{RTS}	Retransmit Set-Up Time	45		60		80		100		130		180		ns	

SINGLE DEVICE CONFIGURATION

A single MK4503 may be used when application requirements are for 2048 words or less. The MK4503 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 9).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 10 demonstrates an 18-bit word width by using two MK4503s. Any word width can be attained by adding additional MK4503s. The half full flag ($\overline{HF}$) operates the same as in the single device configuration.

Figure 9. A Single 2047 x 9 FIFO Configuration

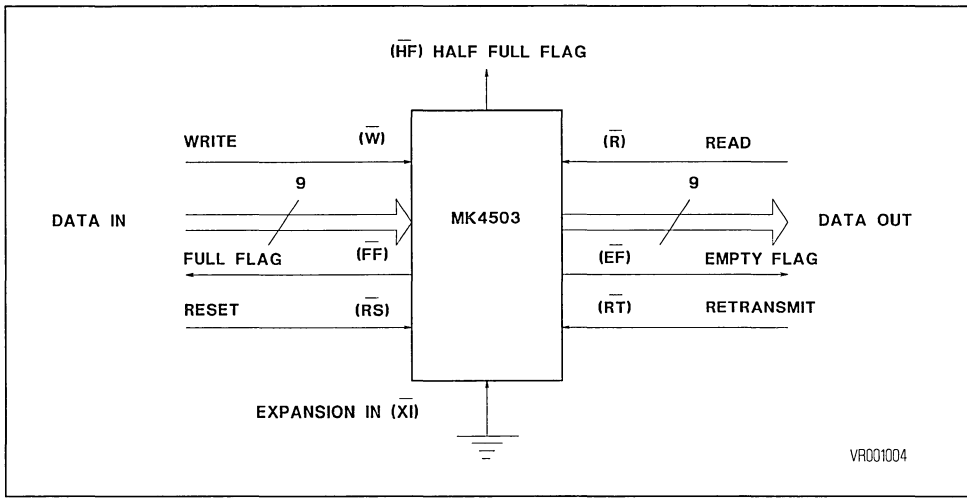
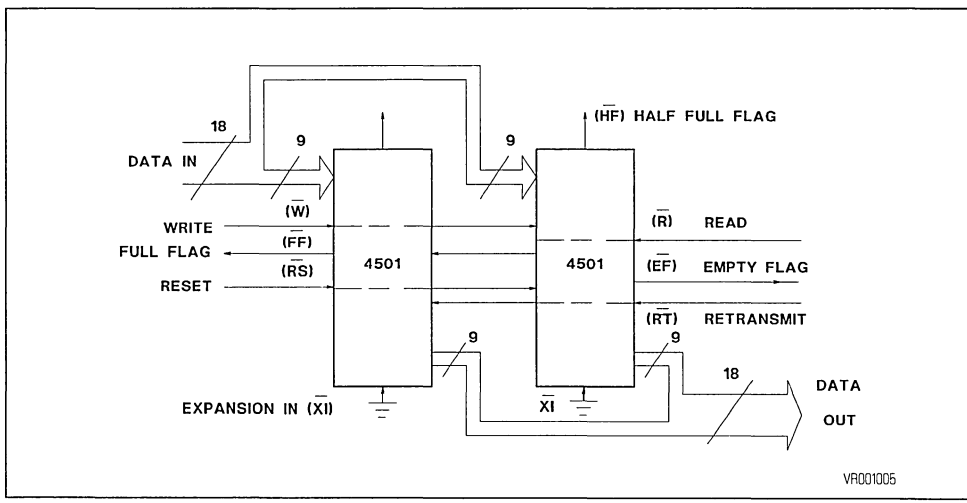


Figure 10. A 2048 x 18 FIFO Configuration (width expansion)

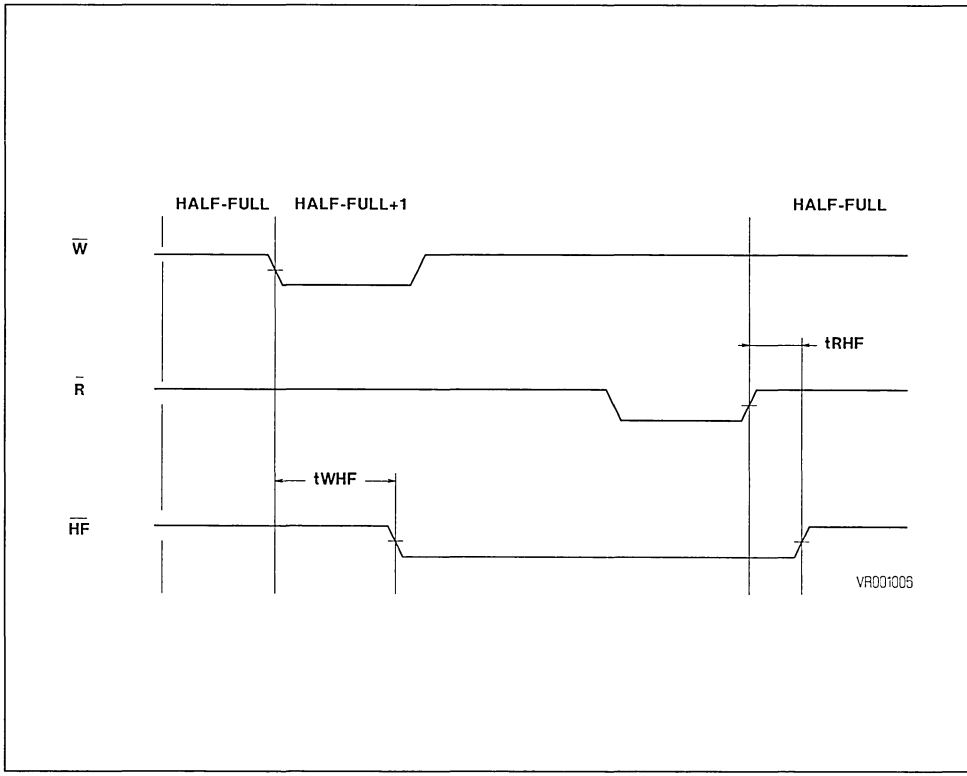


Note : Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration Do not connect flag output signals together.

HALF FULL FLAG LOGIC

When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag ($\overline{HF}$) is then reset by the rising edge of the read operation (see Figure 11).

Figure 11. Half Full Flag Waveforms



AC CHARACTERISTICS

($0°C \leq T_A \leq +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WHF}	Write Low to Half Full Flag Low		80		100		120		140		175		235	ns
t_{RHF}	Read High to Half Full Flag High		80		100		120		140		175		235	ns

DEPTH EXPANSION (Daisy Chain)

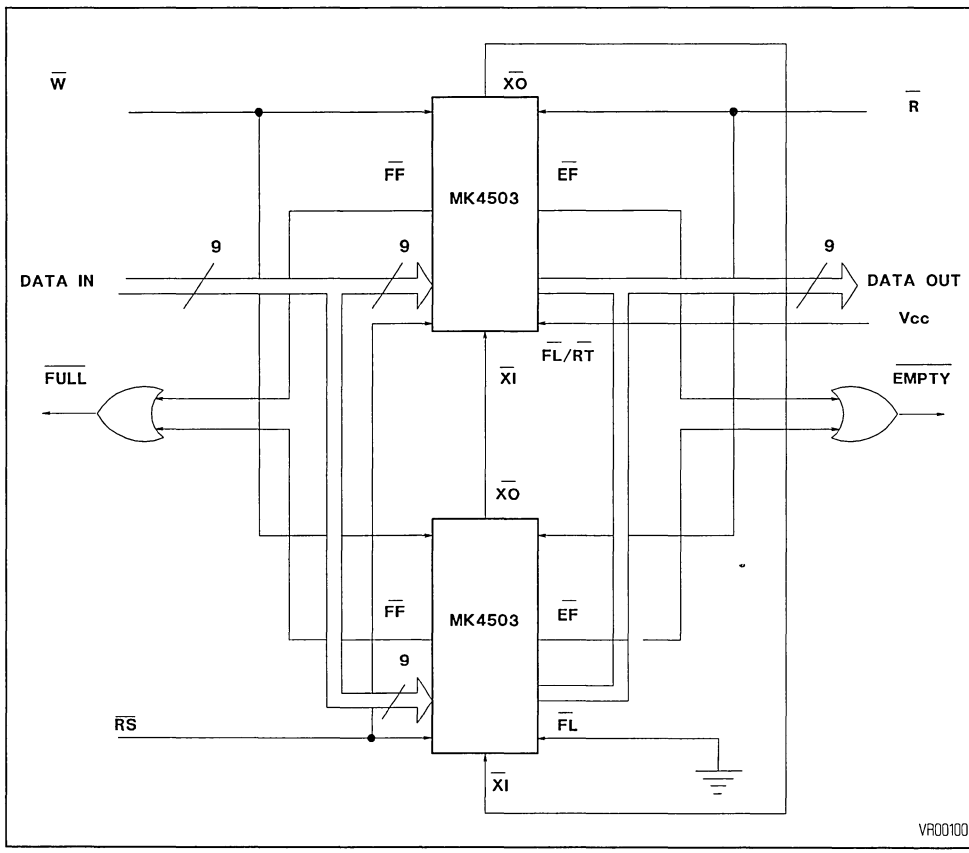
The MK4503 can easily be adapted to applications when the requirements are for greater than 2048 words. Figure 12 demonstrates Depth Expansion using the MK4503s. Any depth can be attained by adding additional MK4503s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The MK4503 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this mode.

Figure 12. A 4K x 9 FIFO Configuration (Depth Expansion)



EXPANSION TIMING

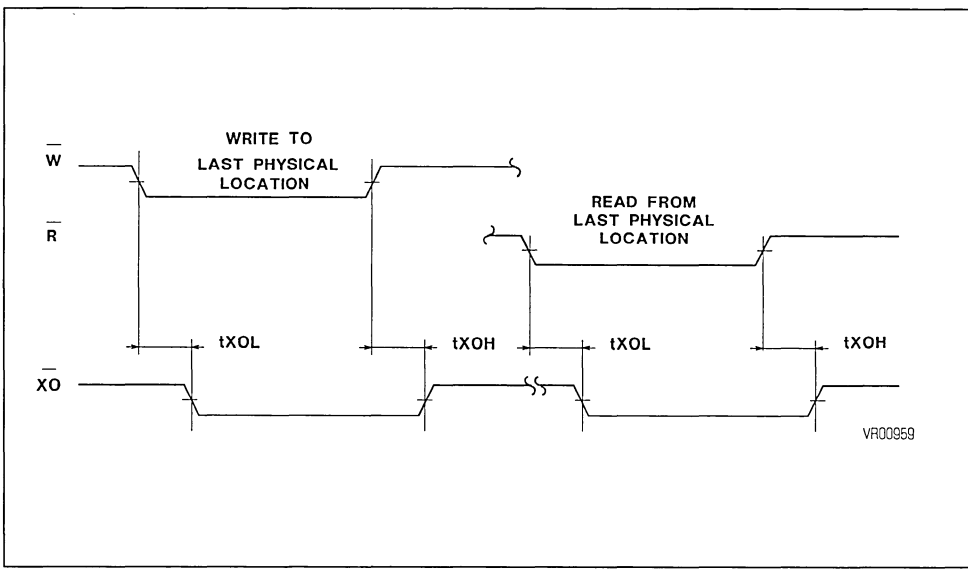
Figures 13 and 14 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. In as much as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them ; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

When in Depth Expansion mode, a given MK4503 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK4503 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs.

It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

Figure 13. Expansion Out Waveforms

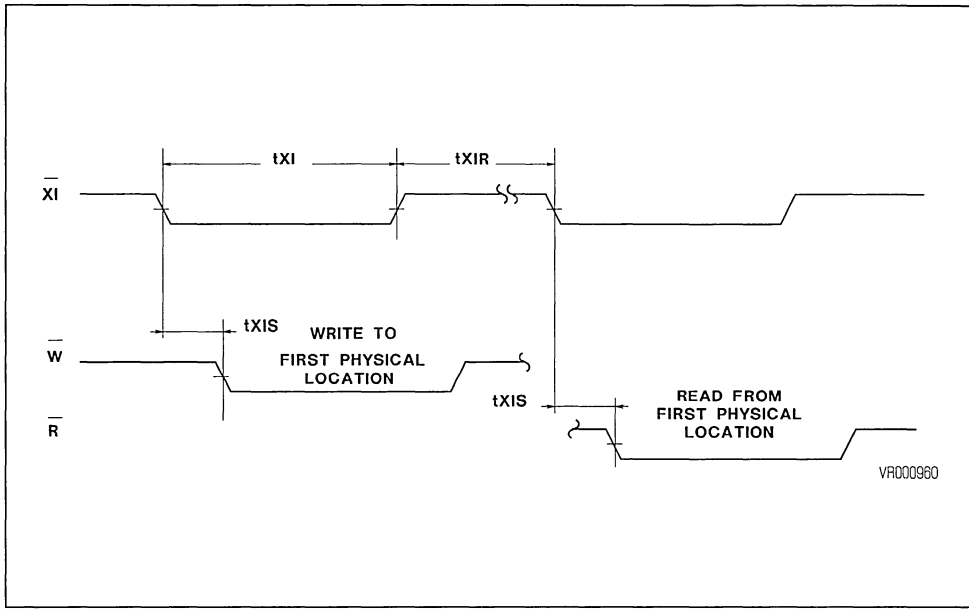


AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{XOL}	Expansion Out Low		55		70		75		90		115		150	ns
t_{XOH}	Expansion Out High		60		80		90		100		125		155	ns

Figure 14. Expansion In Waveforms



AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	60		75		95		115		145		195		ns	1
t_{XIR}	Expansion in Recovery Time	15		20		20		20		25		35		ns	
t_{XIS}	Expansion in Set-up Time	25		30		45		50		60		85		ns	

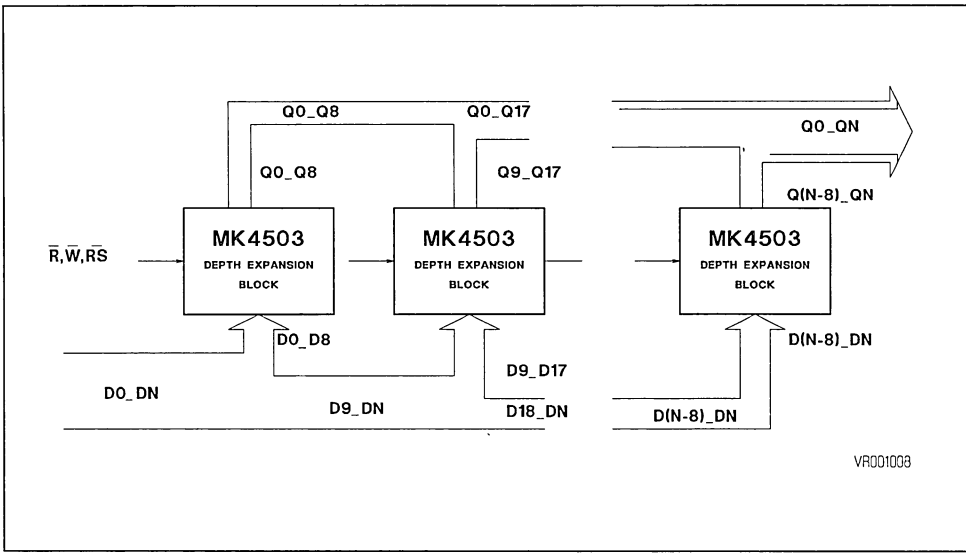
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL APPLICATIONS

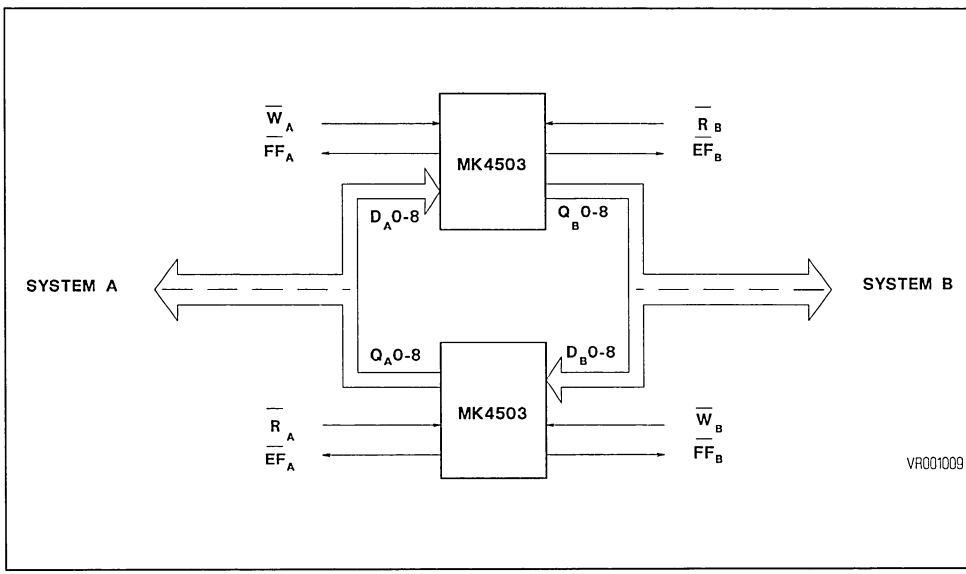
Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK4503s, as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used ; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Figure 15. Compound FIFO Expansion Configuration



Notes :
1. For depth expansion block see DEPTH EXPANSION Section and Figure 12.
2. For Flag operation see WIDTH EXPANSION Section and Figure 10.

Figure 16. Bidirectional FIFO Application



ORDERING INFORMATION

Example: MK4503 N 65

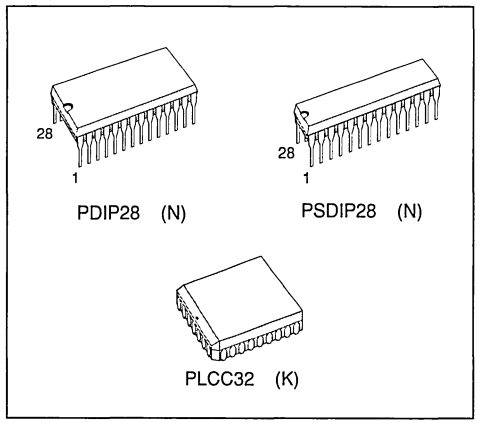
Package		Speed	
N	PDIP28	65	65ns
		80	80ns
		10	100ns
		12	120ns
		15	150ns
		20	200ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

VERY FAST CMOS 512 / 1K / 2K x 9 BiPORT FIFO

- FIRST-IN-FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE x 9 ORGANIZATIONS:
  - MK45H01,11 (512 x 9)
  - MK45H02,12 (1K x 9)
  - MK45H03,13 (2K x 9)
- LOW POWER, HIGH SPEED HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- FULLY EXPANDABLE IN WORD WIDTH AND DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HALF-FULL FLAG IN SINGLE DEVICE MODE



DESCRIPTION

The MK45H01,11,02,12,03,13 are BiPORT™ FIFO memories from SGS-THOMSON Microelectronics, which utilize special two-port memory cell techniques. Specifically, these devices implement a First-In-First-Out (FIFO) algorithm, featuring asynchronous read/write operations, full, empty, and half full status flags, and unlimited expansion capability in both word size and depth. The full and empty flags are provided to prevent data overflow and underflow.

PIN NAMES

$\overline{W}$	Write
$\overline{R}$	Read
$\overline{RS}$	Reset
D0-D8	Data Inputs
Q0-Q8	Data Outputs
$\overline{FL}/\overline{RT}$	First Load / Retransmit
$\overline{XI}$	Expansion Input
$\overline{XO}/\overline{HF}$	Expansion Output / Half-full Flag
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
V_{CC}, GND	5 Volts, Ground
NC	Not Connected

Figure 1. Pin Connections

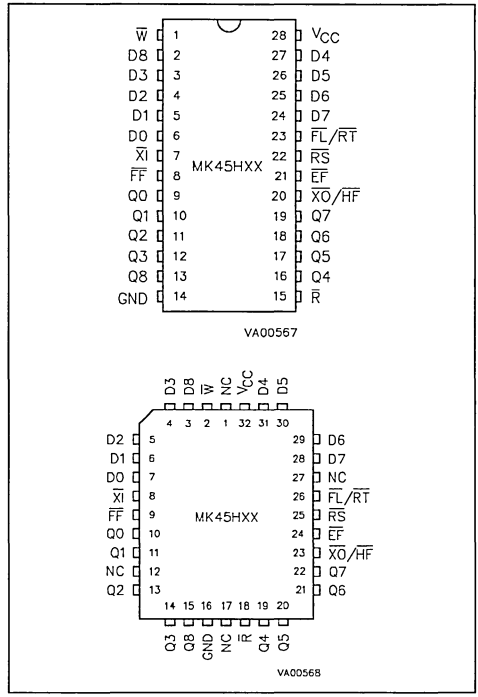
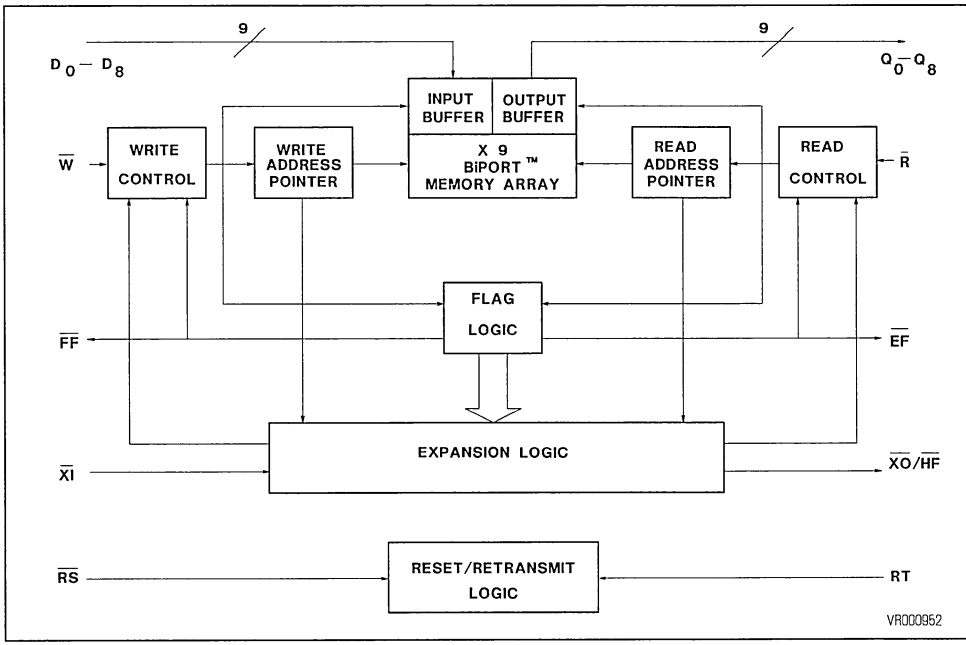


Figure 2. Block Diagram



DESCRIPTION (Continued)

The data is loaded and emptied on a first-in-first-out basis, and the latency for retrieval of data is approximately one load (write) cycle. These devices feature a read/write cycle time of only 35ns (28.5MHz).

The reads and writes are internally sequential through the use of separate read and write pointers in a ring counter fashion. Therefore, no address information is required to load or unload data. Data is loaded and unloaded with the use of $\overline{W}$ (write), and $\overline{R}$ (read) input pins. Separate data in (D0-D8) and data out (Q0-Q8) pins allow simultaneous and asynchronous read/write operations, provided the status flags are not protecting against data underflow or overflow.

The main application of these devices is a buffer for sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The MK45HX1, MK45HX2, and MK45HX3 incorporate 9-bit wide data arrays that provide for support control or parity bit functions. This feature is helpful in data communications where the extra parity bit is used for transmission and reception error checking. These devices also offer retransmit ($\overline{RT}$) and half-full features in single device or width expansion modes. The retransmit function allows data to be re-read by resetting the read pointer while not disturbing the write pointer. This is for applications where the FIFO is not full, or is written with less than 512, 1024, or 2048 words.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK45HX1, MK45HX2, and MK45HX3 employ a memory-based architecture wherein a byte written into the device does not "ripple through". Instead, a byte written into the device is stored in a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Two internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching the final address in the FIFO (512, 1024, or 2048). The empty, half full, and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location.

FUNCTIONAL DESCRIPTION (Continued)

As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

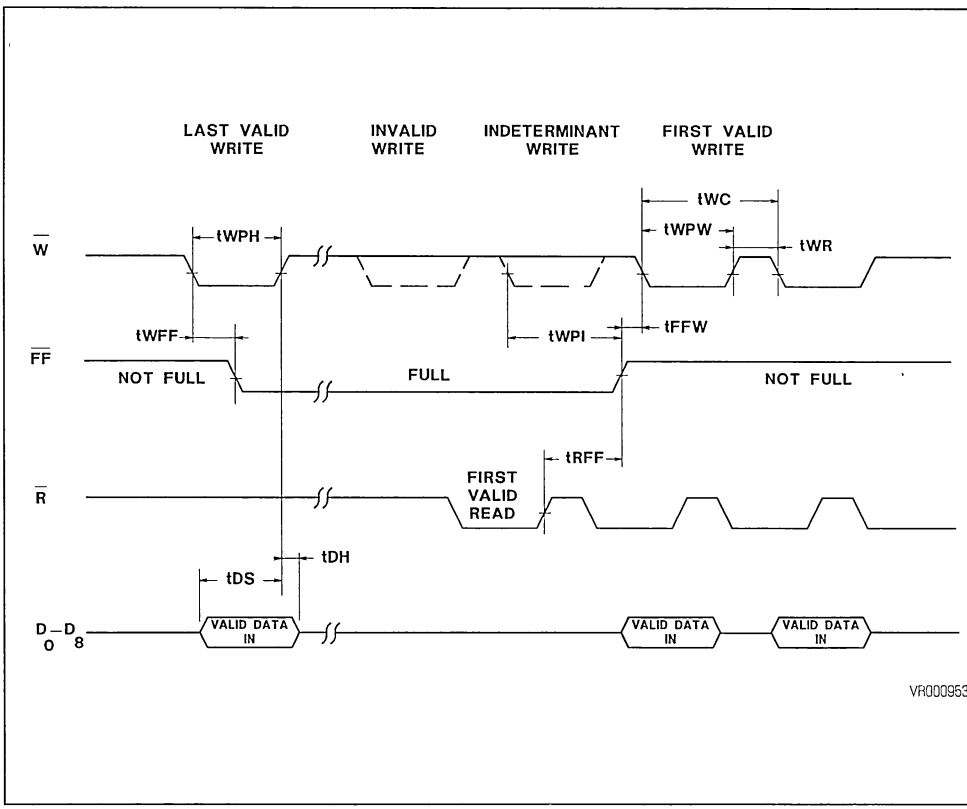
Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without effecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading individual FIFOs. The penalty of cascading is often unacceptable ripple through delays. The MK45HX1, MK45HX2, and MK45HX3 allow implementation of very large FIFOs with no timing penalties. The memory-based architecture of the device allows the connection of the read, write, data in, and data out lines of the device in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

WRITE MODE

The MK45HXX initiates a Write Cycle (see Figure 3) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not set. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is set during the last valid write as the MK45H03 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 5). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on the internal flag status.

Figure 3. Write and Full Flag Waveforms



Write and Full Flag AC Operating Conditions
(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

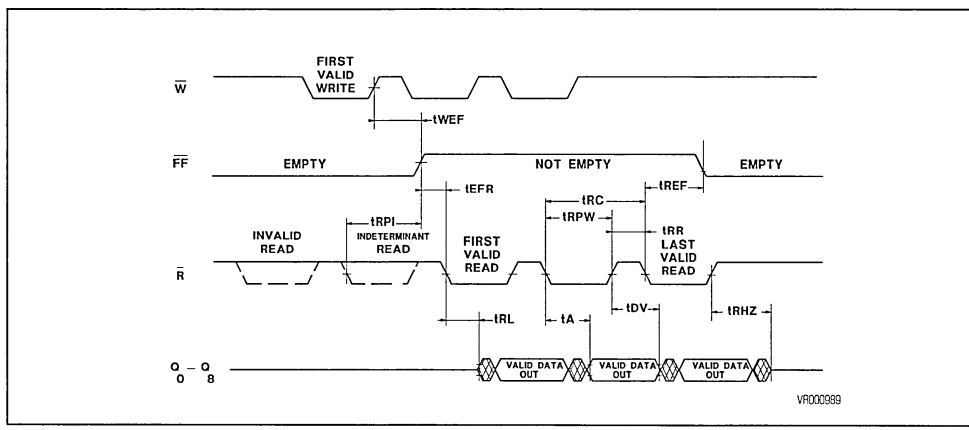
Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	35		45		65		80		140		ns	
t_{WPW}	Write Pulse Width	25		35		50		65		120		ns	1
t_{WR}	Write Recovery Time	10		10		15		15		20		ns	
t_{DS}	Data Set Up Time	15		18		30		30		40		ns	
t_{DH}	Data Hold Time	0		0		0		0		0		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		25		35		45		60		60	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write		10		10		10		10		10	ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		25		35		45		60		60	ns	2
t_{WPI}	Write Protect Indeterminant	10		10		10		10		10		ns	2

Notes: 1. Pulse widths less than minimum values are not allowed
2. Measured using equivalent output load circuit

READ MODE

The MK45HXX initiates a Read Cycle (see Figure 4) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not set. In the read mode of operation, the MK45H0X provides fast access to data from 9 of the locations in the static storage array. The data is accessed on a FIFO basis independent of any on-going WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next read operation. In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further READ operations will be inhibited (the data inputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid WRITE operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent read operation, provided that a second WRITE has not been completed (see Figure 6). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more that t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less then t_{EFR} later may or may not occur (be valid) depending on internal flag status.

Figure 4. Read and Empty Flag Waveforms



Read and Empty Flag AC Operating Conditions

($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	35		45		65		80		140		ns	
t_A	Access Time		25		35		50		65		120	ns	2
t_{RR}	Read Recovery Time	10		10		15		15		20		ns	
t_{RPW}	Read Pulse Width	25		35		50		65		120		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		18		20		25		25		35	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		25		35		40		60		60	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read		10		10		10		10		10	ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		25		35		45		60		60	ns	2
t_{RPI}	Read Protect Indeterminant	10		10		10		10		10		ns	2

Notes: 1. Pulse widths less than minimum values are not allowed
2. Measured using equivalent output load circuit

Figure 5. Read/Write to Full Flag Waveforms

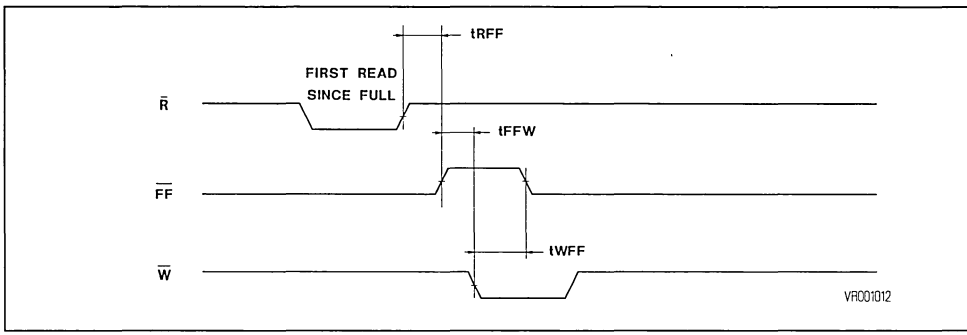
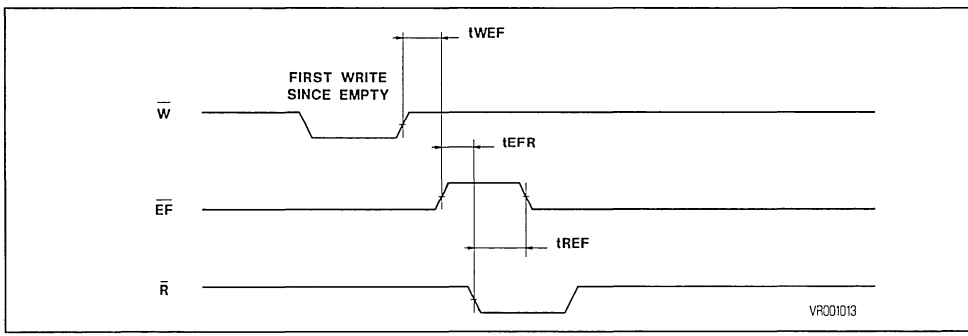


Figure 6. Write/Read to Empty Flag Waveforms

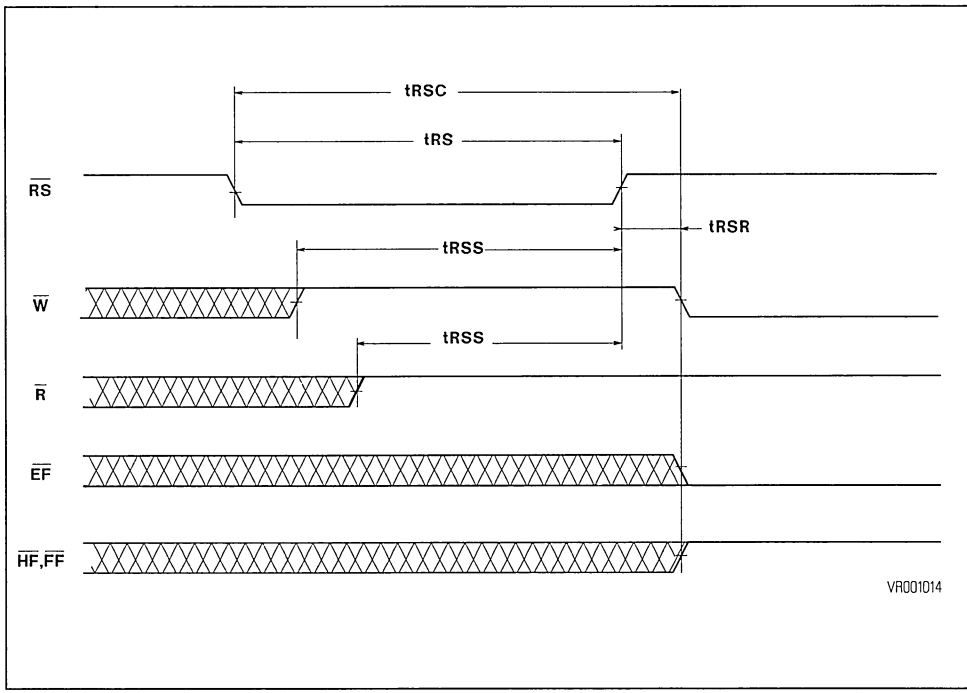


RESET

The MK45HXX is reset (see Figure 7) whenever the Reset pin ($\overline{RS}$) is in the low state. During a reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a WRITE operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{R}$ and $\overline{W}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

Figure 7. Reset Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

Reset AC Operating Conditions ($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	35		45		65		80		140		ns	
t_{RS}	Reset Pulse Width	25		35		50		65		120		ns	1
t_{RSR}	Reset Recovery Time	10		10		15		15		20		ns	
t_{RSS}	Reset Set Up Time	25		30		30		45		100		ns	

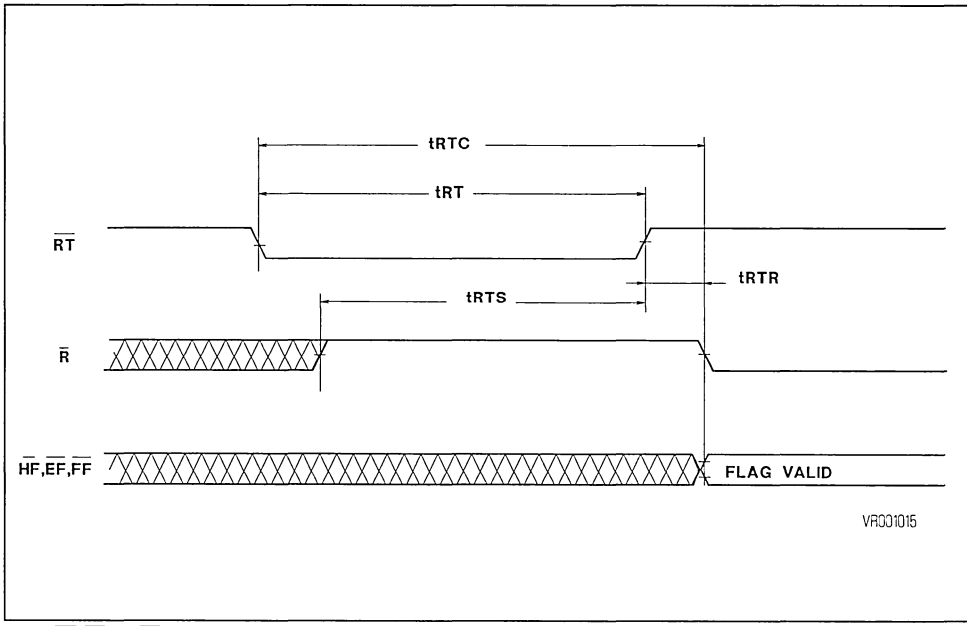
Note: 1. Pulse widths less than minimum values are not allowed

RETRANSMIT

The MK45HXX can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 8). A Retransmit operation sets the internal read pointer to the first location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than the total FIFO depth are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 8. Retransmit Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Retransmit AC Operating Conditions

($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	35		45		65		80		140		ns	
t_{RT}	Retransmit Pulse Width	25		35		50		65		120		ns	1
t_{RTR}	Retransmit Recovery Time	10		10		15		15		20		ns	
t_{RTS}	Retransmit Set Up Time	25		30		30		45		100		ns	

Note: 1. Pulse widths less that minimum values are not allowed

SINGLE DEVICE CONFIGURATION

A single MK45HXX may be used when application requirements are for a depth of the device depth or less. The MK45HXX is placed in the Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 9).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 10 demonstrates an 18-bit word width by using two MK45HXXs. Any word width can be attained by adding additional MK45HXXs. The half full flag ($\overline{HF}$) operates the same as in single device configuration.

Figure 9. A Single MK45HXX FIFO Configuration

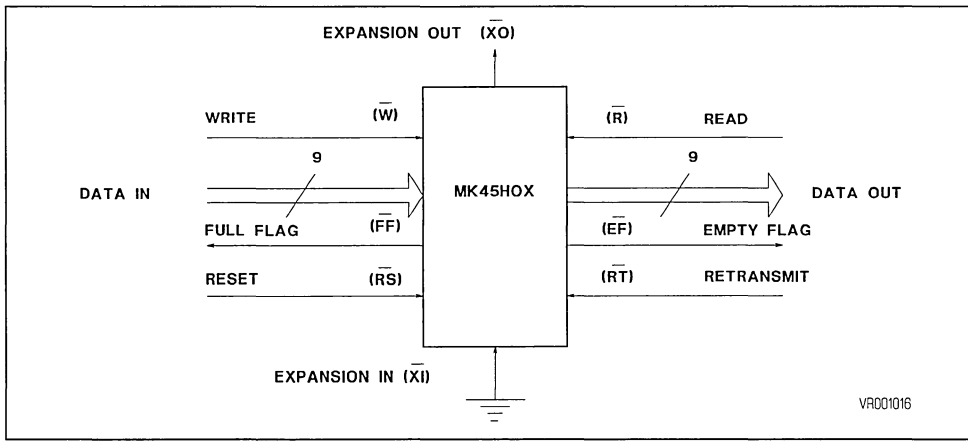
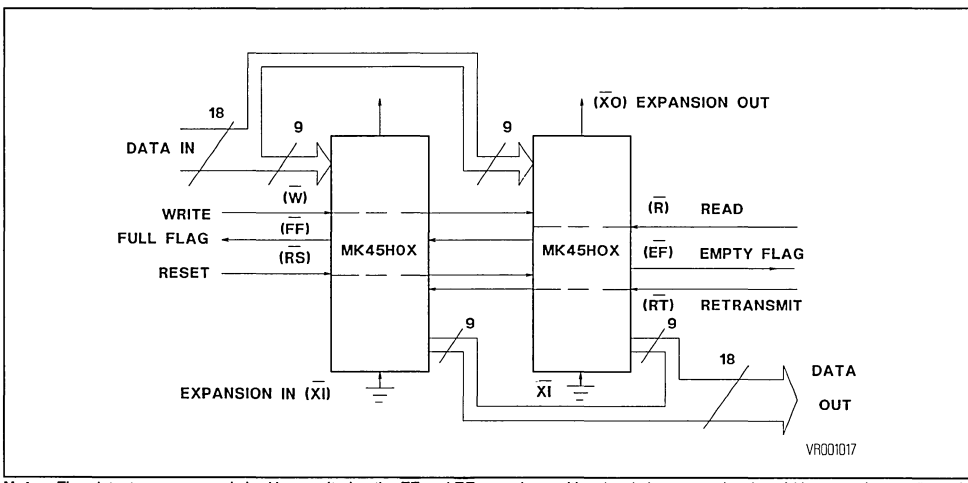


Figure 10. A Two Device Width Expansion FIFO Configuration



Note : Flag detection is accomplished by monitoring the FF and EF signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

HALF FULL FLAG LOGIC

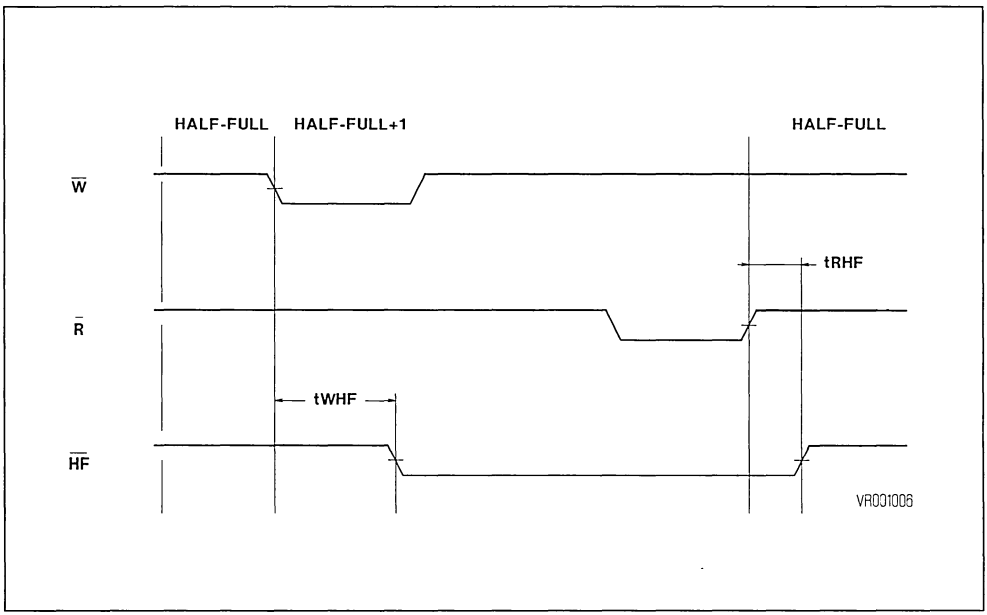
When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag ($\overline{HF}$) is then reset by the rising edge of the read operation (see Figure 11).

DEPTH EXPANSION (Daisy Chain)

The MK45HXX can be easily adapted to applications when the requirements are greater than the individual device word depth. Figure 12 demonstrates Depth Expansion using two MK45HXXs. Any depth can be attained by adding additional MK45HXXs.

External logic is needed to generate a composite Full and Empty Flag. This requires the ORing of all the $\overline{EF}$s and the ORing of all the $\overline{FF}$s (i.e., all must be set to generate the composite $\overline{FF}$ or $\overline{EF}$).

Figure 11. Half Full Flag Waveforms



Half Full Flag AC Operating Conditions

(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WHF}	Write Low to Half Full Flag Low		30		35		45		60		60	ns	
t_{RHF}	Read High to Half Full Flag High		30		35		45		60		60	ns	

The MK45HXX operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions :

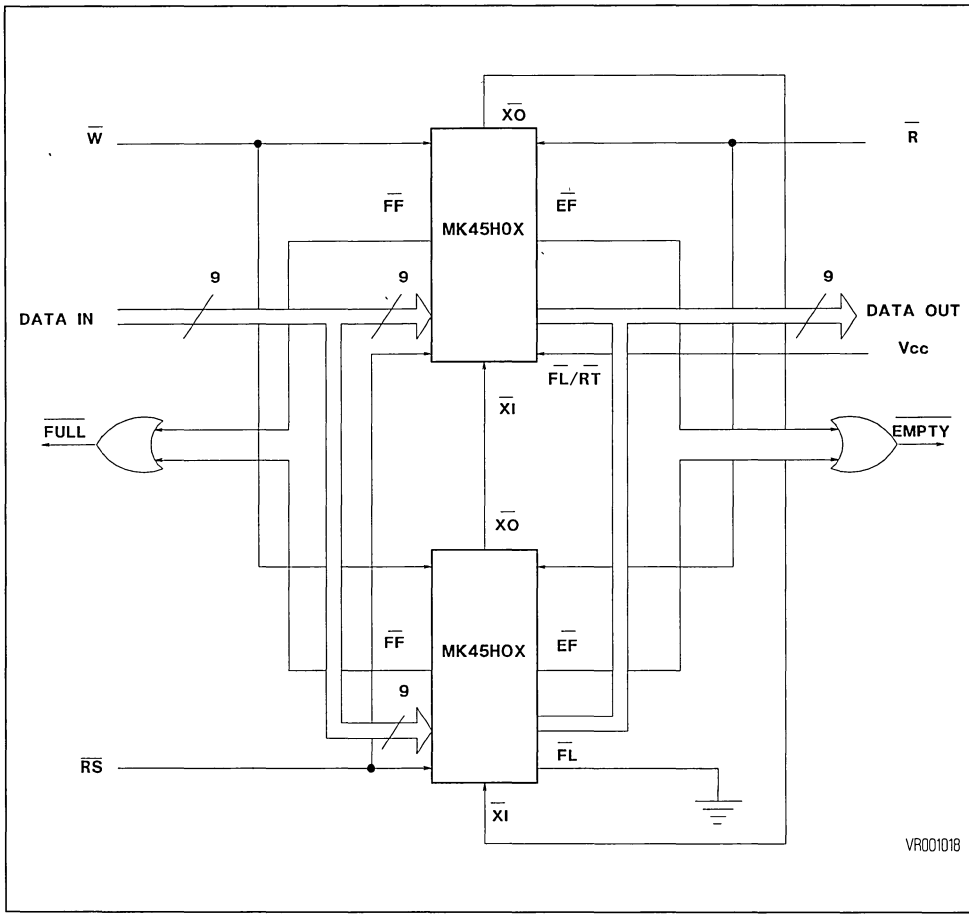
1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not available in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this mode.

EXPANSION TIMING

Figures 13 and 14 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Due to the fact that Expansion Out pins are generally connected only to Expansion In pins, the user does not need to be concerned with the actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

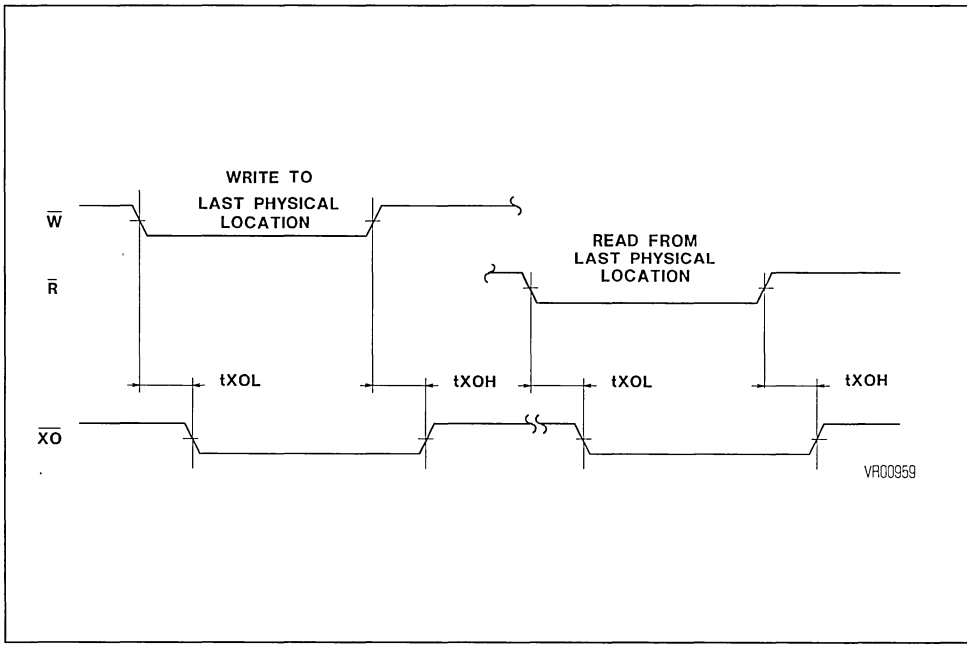
Expansion Out pulses are the identical to the WRITE and READ signals but ; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

Figure 12. A Two Device Depth Expansion Configuration



When in Depth Expansion mode, a given MK45HXX will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK45HXX in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

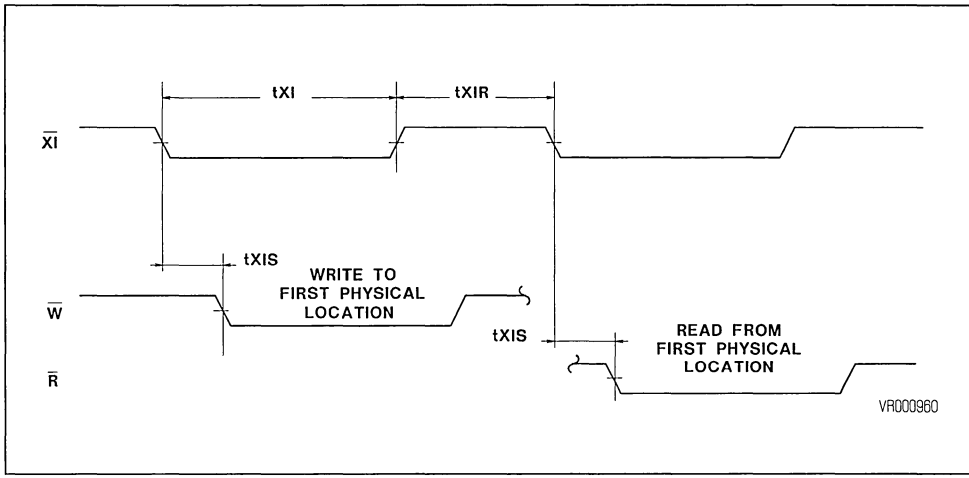
Figure 13. Expansion Out Waveforms



Expansion Out AC Operating Conditions
($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XOL}	Expansion Out Low		25		35		40		55		90	ns	
t_{XOH}	Expansion Out High		25		35		40		55		90	ns	

Figure 14. Expansion In Waveforms



Expansion In AC Operating Conditions
($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	25		35		45		60		115		ns	1
t_{XIR}	Expansion In Recovery Time	10		10		10		10		10		ns	
t_{XIS}	Expansion In Setup Time	15		15		15		15		15		ns	

Note: 1. Pulse widths less than minimum values are not allowed

COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK45HXXs, as shown in Figure 16. Care must be taken to ensure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used ; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Figure 15. Compound FIFO Expansion Configuration

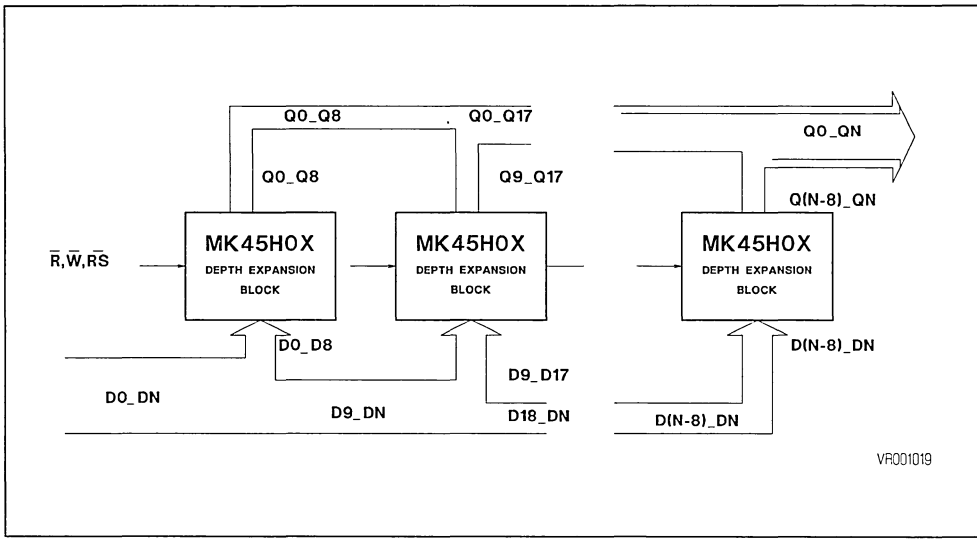
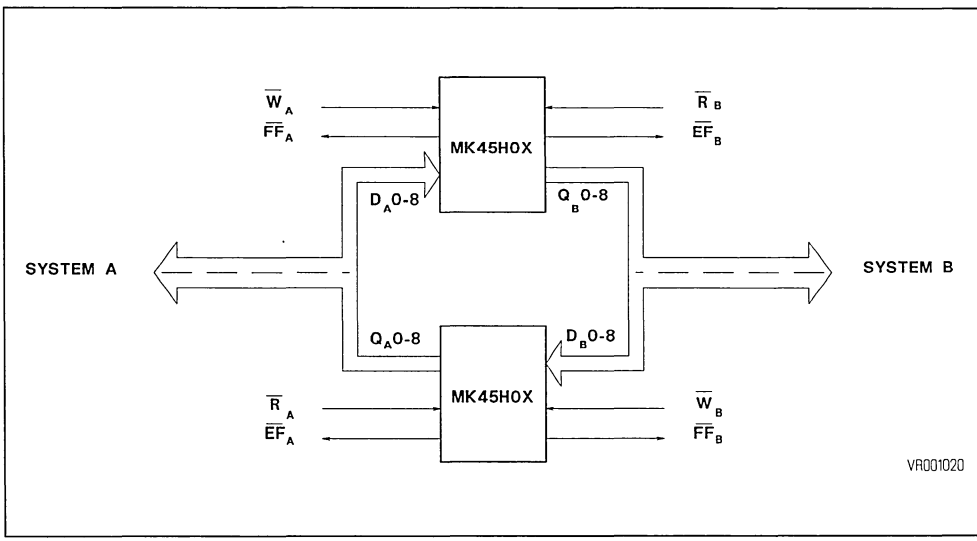


Figure 16. Bidirectional FIFO Application



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	–0.3 to +7	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_D	Power Dissipation	1	W
I_{OUT}	Output Current	20	mA

Note : This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this spefication in not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Max.	Units	Note
V_{CC}	Supply Voltage	4.5	5.5	V	1
GND	Ground	0	0	V	
V_{IH}	Logic 1 All Inputs	2	V_{CC} + 0.3	V	1,2
V_{IL}	Logic 0 All Inputs	–0.3	0.8	V	1

Notes: 1. All Voltages are referenced to ground
2. V_{IH} = 2.5V on the RS pin for MK45H01,11, 02,12

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$, V_{CC}= +5V± 10%)

Symbol	Parameter	Min.	Max.	Units	Note
I_{CC1}	Average V_{CC} Power Supply Current		120	mA	1
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ /$\overline{RT}$ = V_{IH})		12	mA	1
I_{CC3}	Power Down Current (Inputs ≥ V_{CC} -0.2V)		2	mA	1
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	2
I_{OL}	Output Leakage Current	–10	10	µA	3
V_{OH}	Output Logic 1 Voltage (I_{OUT} = -4.0mA)	2.4		V	4
V_{OL}	Output Logic 0 Voltage (I_{OUT} = 8.0mA)		0.4	V	4

Notes : 1. I_{CC} measurements are made with outputs open.
2. Measured with $0.4V \leq V_{IN} \leq V_{CC}$.
3. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
4. All voltages are referenced to ground.

CAPACITANCE (T_A= 25°C, f= 1MHz)

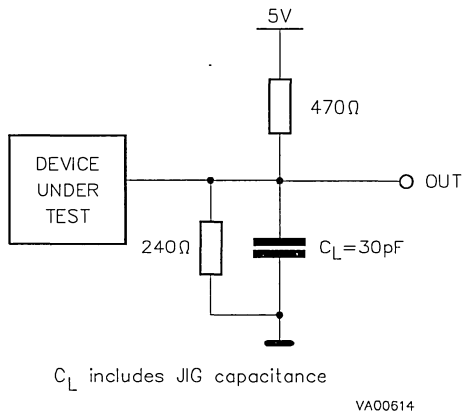
Symbol	Parameter	Typ.	Max.	Unit	Note
C_1	Capacitance on Input Pins		8	pF	1
C_0	Capacitance on Output Pins		12	pF	1,2

Notes : 1. This parameter is only sampled and not 100% tested
2. Output buffer deselected

AC TEST CONDITIONS

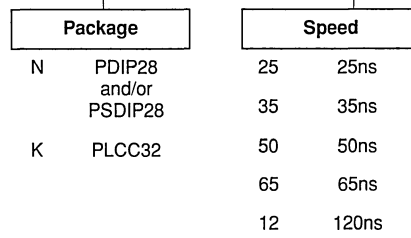
Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	5	ns
Input Signal Timing Reference Level	1.5	V
Output Signal Timing Reference Levels	1.5 and 1.9	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ±10%	V

Figure 17. Equivalent Output Load Circuit



ORDERING INFORMATION

Example: MK45H02 N 25

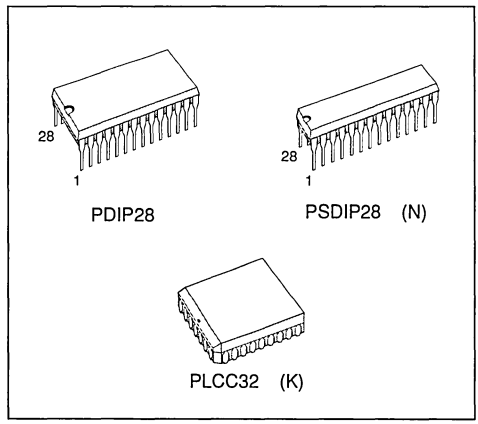


For a list of available options of Package and Speed, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.

VERY FAST CMOS 4K / 8K x 9 BiPORT FIFO

- FIRST-IN-FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE x 9 ORGANIZATIONS:
  - MK45H04,14 (4K x 9)
  - MK45H08 (8K x 9)
- LOW POWER, HIGH SPEED HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- FULLY EXPANDABLE IN WORD WIDTH AND DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HALF-FULL FLAG IN SINGLE DEVICE MODE



DESCRIPTION

The MK45HX4 and MK45H08 are BiPORT™ FIFO memories from SGS-THOMSON Microelectronics, which utilize special two-port mem-ory cell techniques. Specifically, these devices implement a First-In-First-Out (FIFO) algorithm, featuring asynchronous read/write operations, full, empty, and half full status flags, and unlimited expansion capability in both word size and depth. The full and empty flags are provided to prevent data overflow and underflow.

PIN NAMES

$\overline{W}$	Write
$\overline{R}$	Read
$\overline{RS}$	Reset
D0-D8	Data Input
Q0-Q8	Data Output
$\overline{FL}/\overline{RT}$	First Load / Retransmit
$\overline{XI}$	Expansion Input
$\overline{XO}/\overline{HF}$	Expansion Output / Half-full Flag
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
V_{CC}, GND	5 Volts, Ground
NC	Not Connected

Figure 1. Pin Connections

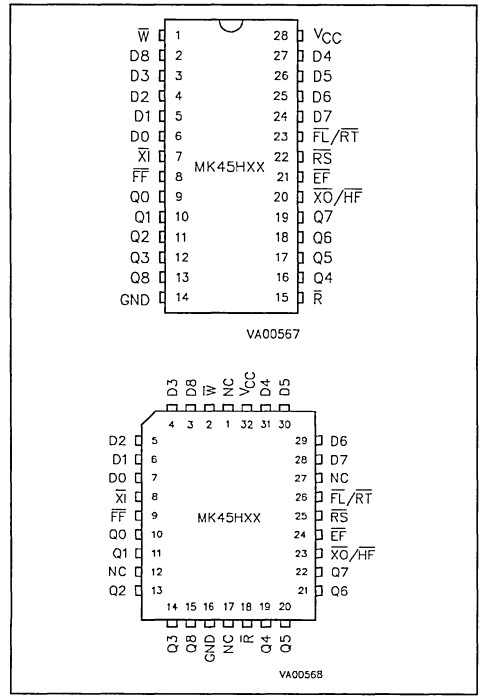
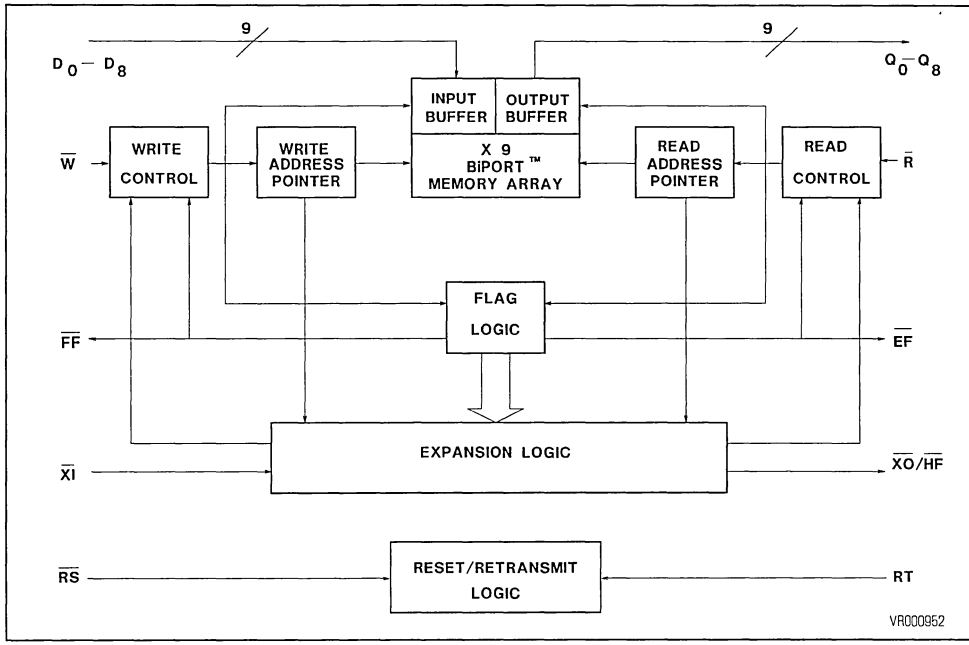


Figure 2. Block Diagram



DESCRIPTION (Continued)

The data is loaded and emptied on a first-in-first-out basis, and the latency for retrieval of data is approximately one load (write) cycle. These devices feature a read/write cycle time of only 35ns (28.5MHz).

The reads and writes are internally sequential through the use of separate read and write pointers in a ring counter fashion. Therefore, no address information is required to load or unload data. Data is loaded and unloaded with the use of $\overline{W}$ (write), and $\overline{R}$ (read) input pins. Separate data in (D0-D8) and data out (Q0-Q8) pins allow simultaneous and asynchronous read/write operations, provided the status flags are not protecting against data underflow or overflow.

The main application of these devices is a buffer for sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The MK45HX4 and MK45H08 incorporate 9-bit wide data arrays that provide for support control or parity bit functions. This feature is helpful in data communications where the extra parity bit is used for transmission and reception error checking. These devices also offer retransmit ($\overline{RT}$) and half-full features in single device or width expansion modes. The retransmit function allows data to be re-read by resetting the read pointer while not disturbing the write pointer. This is for applications where the FIFO is not full, or is written with less than 4096 or 8192 words.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK45HX4 and MK45H08 employ a memory-based architecture wherein a byte written into the device does not "ripple through". Instead, a byte written into the device is stored in a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Two internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching the final address in the FIFO (4096 or 8192). The empty, half full, and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location.

FUNCTIONAL DESCRIPTION (Continued)

As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

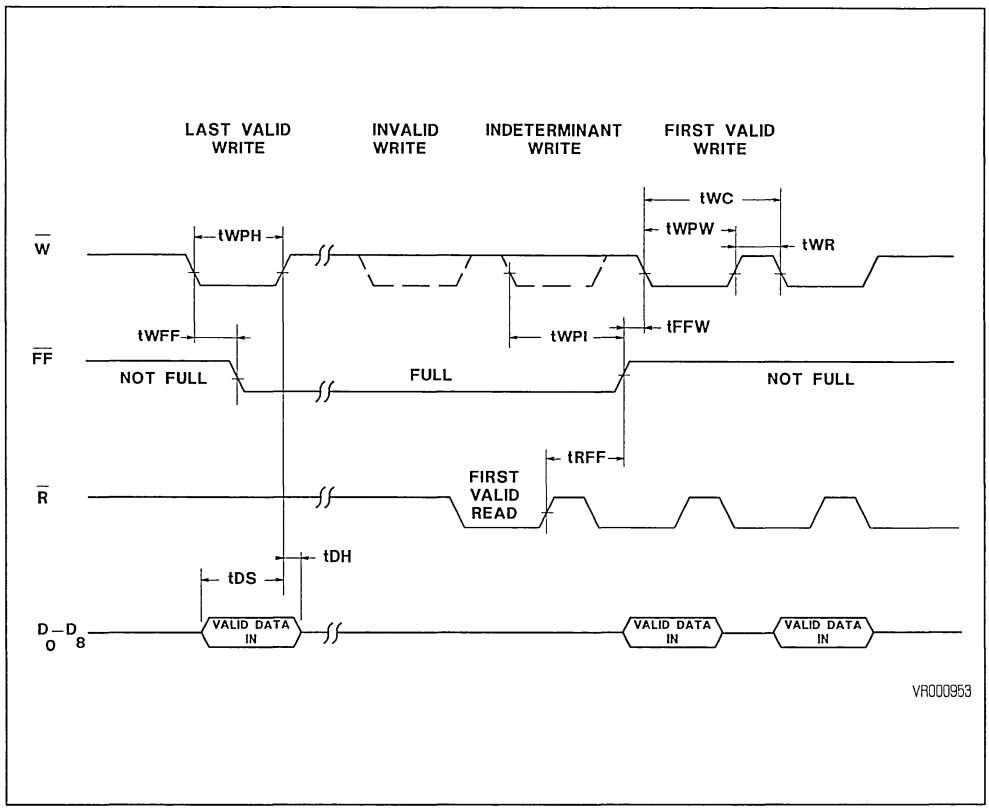
Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without effecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading individual FIFOs. The penalty of cascading is often unacceptable ripple through delays. The MK45HX4, and MK45H08 allow implementation of very large FIFOs with no timing penalties. The memory-based architecture of the device allows the connection of the read, write, data in, and data out lines of the device in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

WRITE MODE

The MK45HXX initiates a Write Cycle (see Figure 3) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not set. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is set during the last valid write as the MK45HXX becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 5). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on the internal flag status.

Figure 3. Write and Full Flag Waveforms



Write and Full Flag AC Operating Conditions
(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

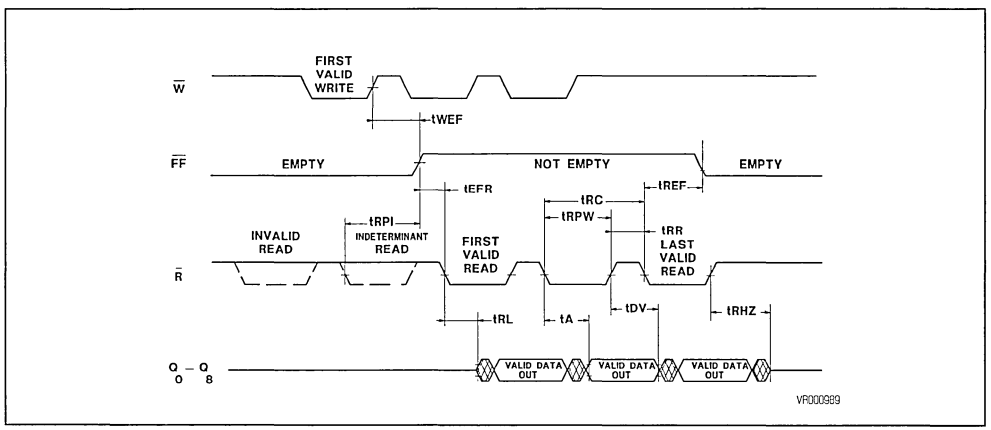
Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	35		45		65		80		140		ns	
t_{WPW}	Write Pulse Width	25		35		50		65		120		ns	1
t_{WR}	Write Recovery Time	10		10		15		15		20		ns	
t_{DS}	Data Set Up Time	15		18		30		30		40		ns	
t_{DH}	Data Hold Time	0		0		0		0		0		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		25		35		45		60		60	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write		10		10		10		10		10	ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		25		35		45		60		60	ns	2
t_{WPI}	Write Protect Indeterminant	10		10		10		10		10		ns	2

Notes: 1. Pulse widths less than minimum values are not allowed
2. Measured using equivalent output load circuit

READ MODE

The MK45HXX initiates a Read Cycle (see Figure 4) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not set. In the read mode of operation, the MK45HXX provides fast access to data from 9 of the locations in the static storage array. The data is accessed on a FIFO basis independent of any on-going WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next read operation.In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further READ operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid WRITE operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent read operation, provided that a second WRITE has not been completed (see Figure 6). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more that t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less then t_{EFR} later may or may not occur (be valid) depending on internal flag status.

Figure 4. Read and Empty Flag Waveforms



Read and Empty Flag AC Operating Conditions
($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	35		45		65		80		140		ns	
t_A	Access Time		25		35		50		65		120	ns	2
t_{RR}	Read Recovery Time	10		10		15		15		20		ns	
t_{RPW}	Read Pulse Width	25		35		50		65		120		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		18		20		25		25		35	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		25		35		40		60		60	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read		10		10		10		10		10	ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		25		35		45		60		60	ns	2
t_{RPI}	Read Protect Indeterminant	10		10		10		10		10		ns	2

Notes: 1. Pulse widths less than minimum values are not allowed
2. Measured using equivalent output load circuit

Figure 5. Read/Write to Full Flag Waveforms

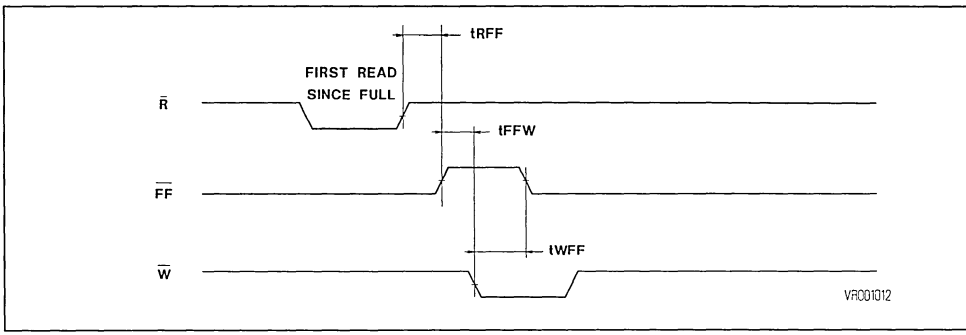
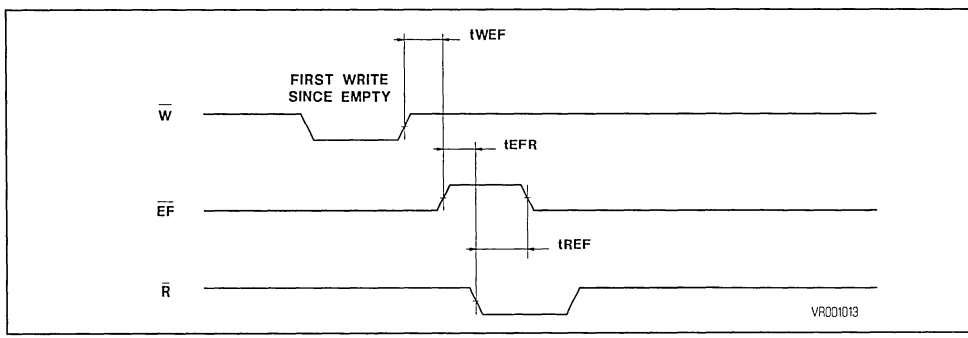


Figure 6. Write/Read to Empty Flag Waveforms

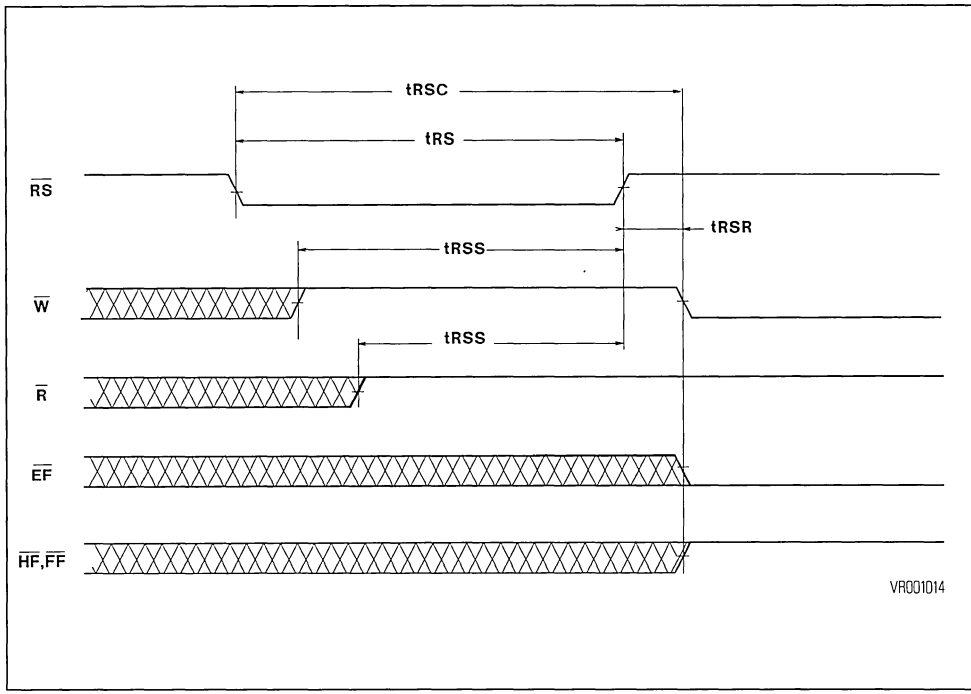


RESET

The MK45HXX is reset (see Figure 7) whenever the Reset pin ($\overline{RS}$) is in the low state. During a reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a WRITE operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{R}$ and $\overline{W}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

Figure 7. Reset Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

Reset AC Operating Conditions ($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	35		45		65		80		140		ns	
t_{RS}	Reset Pulse Width	25		35		50		65		120		ns	1
t_{RSR}	Reset Recovery Time	10		10		15		15		20		ns	
t_{RSS}	Reset Set Up Time	25		30		30		45		100		ns	

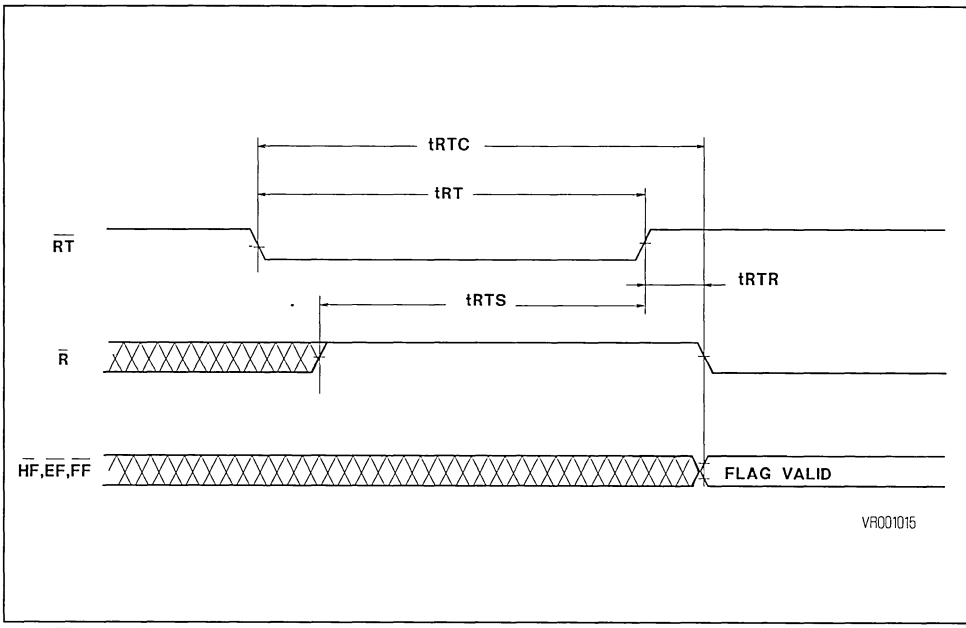
Note: 1. Pulse widths less than minimum values are not allowed

RETRANSMIT

The MK45HXX can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 8). A Retransmit operation sets the internal read pointer to the first location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than the total FIFO depth are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 8. Retransmit Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Retransmit AC Operating Conditions

($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	35		45		65		80		140		ns	
t_{RT}	Retransmit Pulse Width	25		35		50		65		120		ns	1
t_{RTR}	Retransmit Recovery Time	10		10		15		15		20		ns	
t_{RTS}	Retransmit Set Up Time	25		30		30		45		100		ns	

Note: 1. Pulse widths less that minimum values are not allowed

SINGLE DEVICE CONFIGURATION

A single MK45HXX may be used when application requirements are for a depth of the device depth or less. The MK45HXX is placed in the Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 9).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 10 demonstrates an 18-bit word width by using two MK45HXXs. Any word width can be attained by adding additional MK45HXXs. The half full flag ($\overline{HF}$) operates the same as in single device configuration.

Figure 9. A Single MK45HXX FIFO Configuration

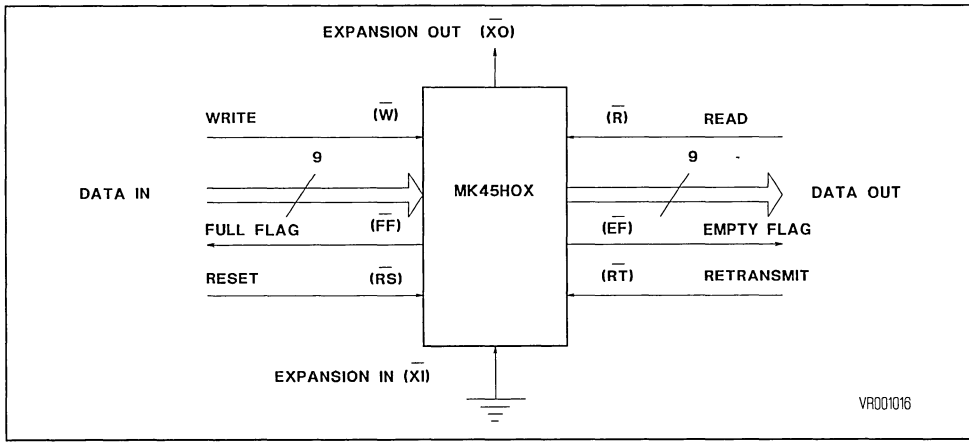
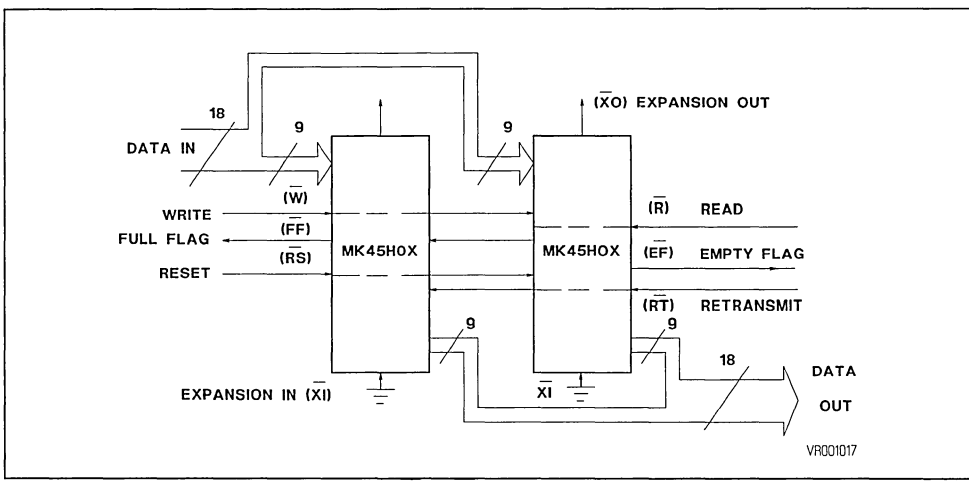


Figure 10. A Two Device Width Expansion FIFO Configuration



Note : Flag detection is accomplished by monitoring the FF and EF signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

HALF FULL FLAG LOGIC

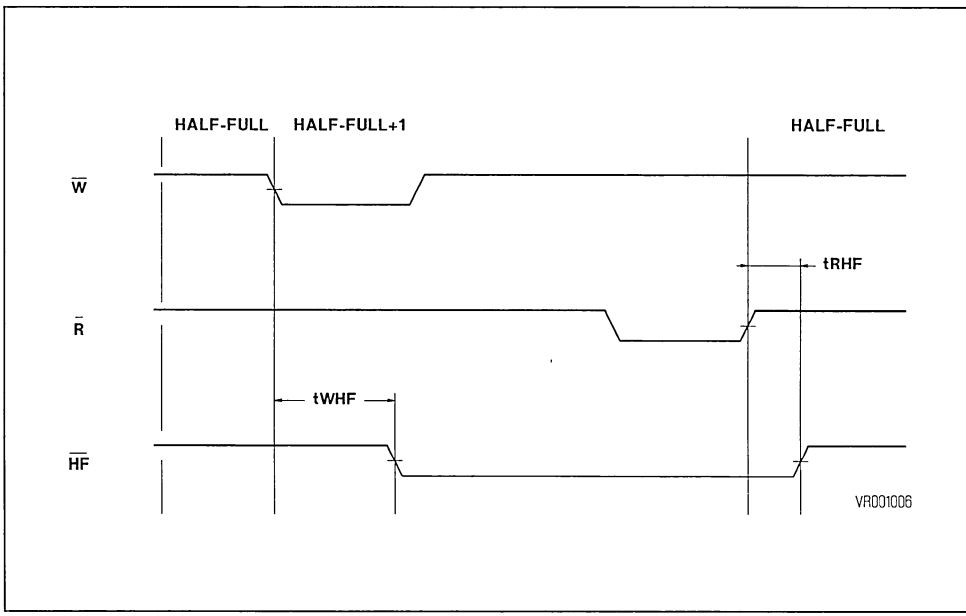
When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag ($\overline{HF}$) is then reset by the rising edge of the read operation (see Figure 11).

DEPTH EXPANSION (Daisy Chain)

The MK45HXX can be easily adapted to applications when the requirements are greater than the individual device word depth. Figure 12 demonstrates Depth Expansion using two MK45HXXs. Any depth can be attained by adding additional MK45HXXs.

External logic is needed to generate a composite Full and Empty Flag. This requires the ORing of all the $\overline{EF}$s and the ORing of all the $\overline{FF}$s (i.e., all must be set to generate the composite $\overline{FF}$ or $\overline{EF}$).

Figure 11. Half Full Flag Waveforms



Half Full Flag AC Operating Conditions
(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WHF}	Write Low to Half Full Flag Low		30		35		45		60		60	ns	
t_{RHF}	Read High to Half Full Flag High		30		35		45		60		60	ns	

The MK45HXX operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions :

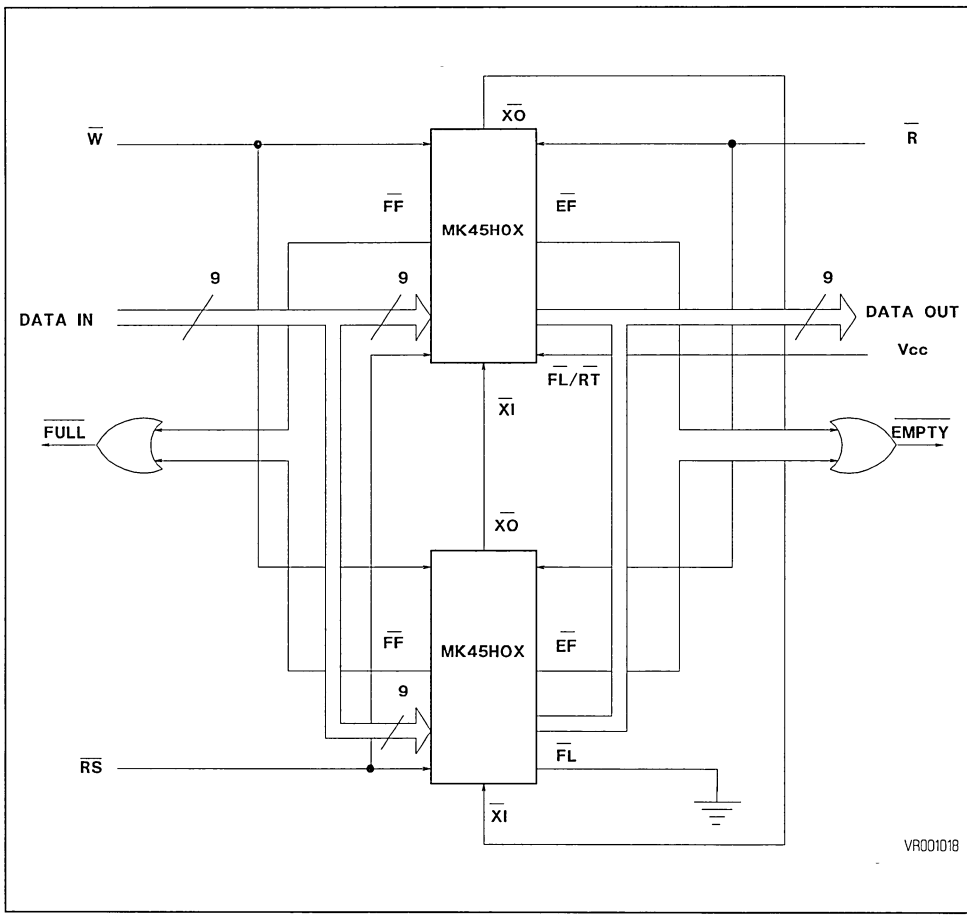
1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not available in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this mode.

EXPANSION TIMING

Figures 13 and 14 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Due to the fact that Expansion Out pins are generally connected only to Expansion In pins, the user does not need to be concerned with the actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

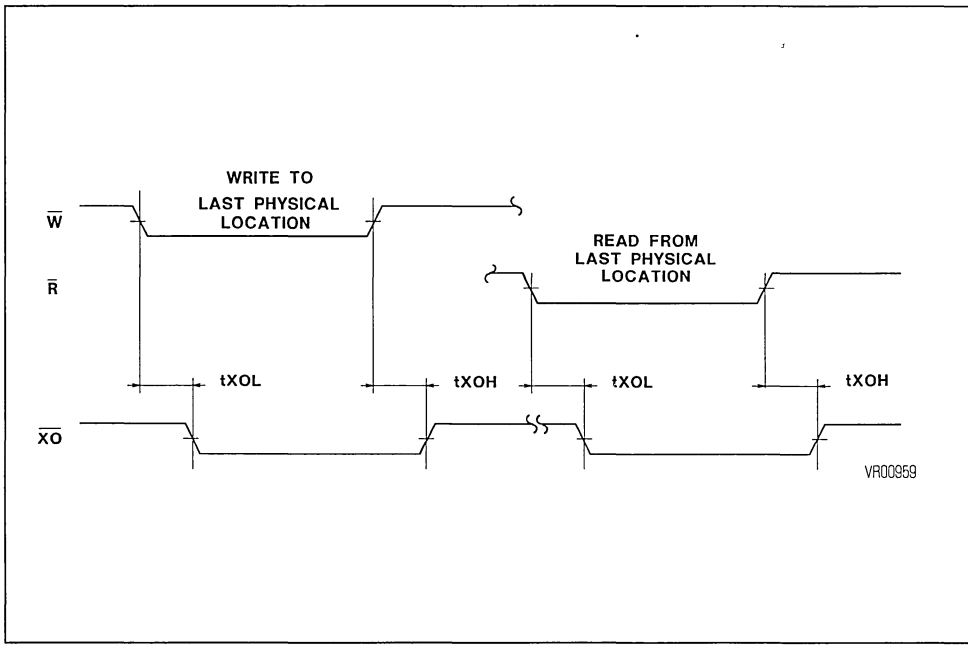
Expansion Out pulses are the identical to the WRITE and READ signals but ; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

Figure 12. A Two Device Depth Expansion Configuration



When in Depth Expansion mode, a given MK45HXX will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK45HXX in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

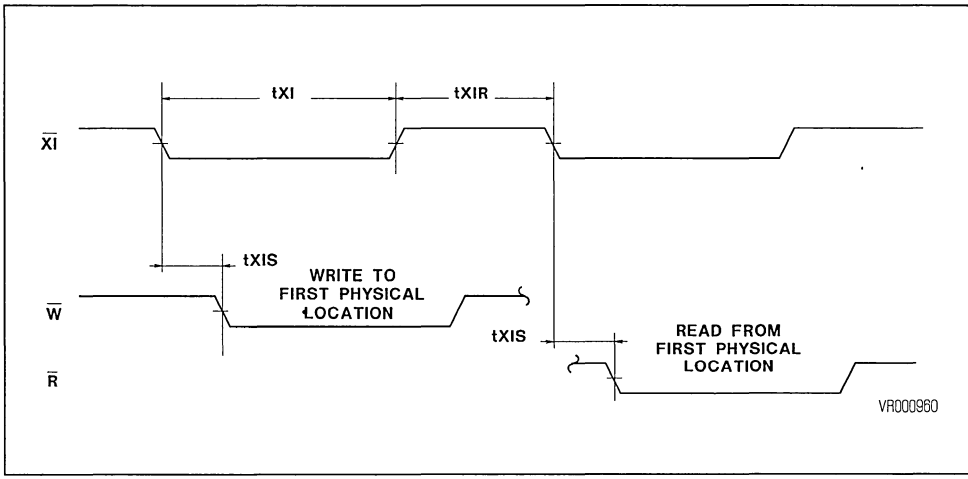
Figure 13. Expansion Out Waveforms



Expansion Out AC Operating Conditions
($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XOL}	Expansion Out Low		25		35		40		55		90	ns	
t_{XOH}	Expansion Out High		25		35		40		55		90	ns	

Figure 14. Expansion In Waveforms



Expansion In AC Operating Conditions

($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	25		35		45		60		115		ns	1
t_{XIR}	Expansion In Recovery Time	10		10		10		10		10		ns	
t_{XIS}	Expansion In Setup Time	15		15		15		15		15		ns	

Note: 1. Pulse widths less than minimum values are not allowed

COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK45HXXs, as shown in Figure 16. Care must be taken to ensure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used ; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Figure 15. Compound FIFO Expansion Configuration

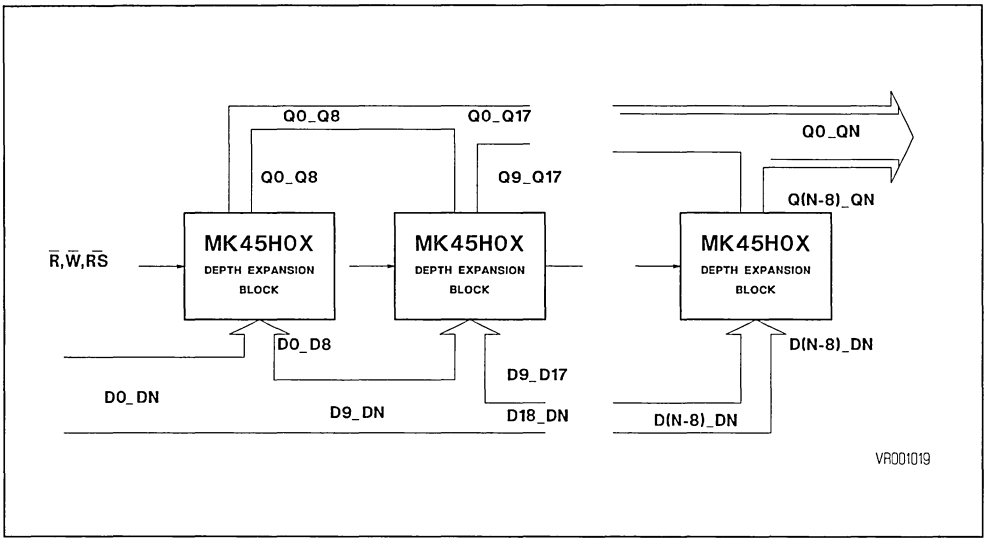
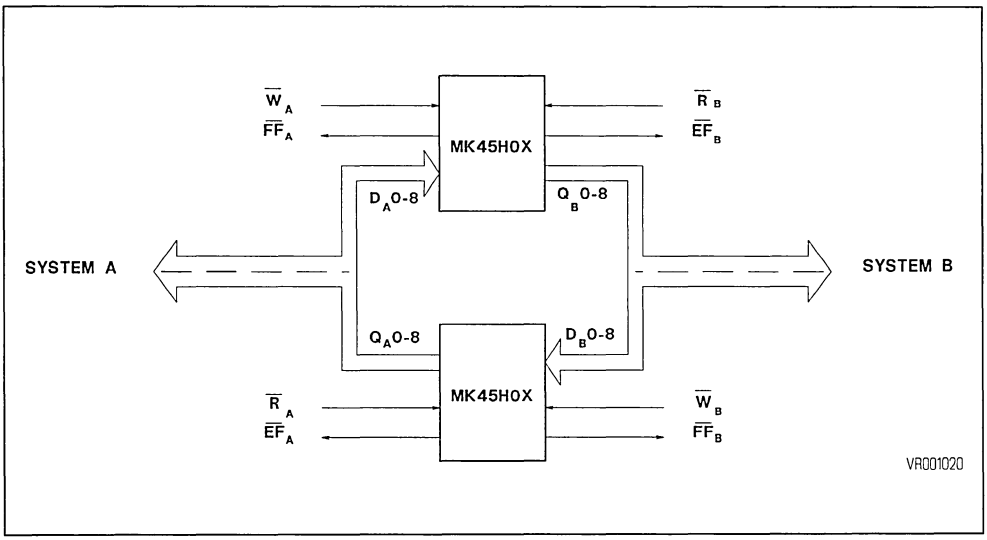


Figure 16. Bidirectional FIFO Application



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	–0.3 to +7	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_D	Power Dissipation	1	W
I_{OUT}	Output Current	20	mA

Note : This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this spefication in not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Max.	Units	Note
V_{CC}	Supply Voltage	4.5	5.5	V	1
GND	Ground	0	0	V	
V_{IH}	Logic 1 All Inputs	2	V_{CC} + 0.3	V	1
V_{IL}	Logic 0 All Inputs	–0.3	0.8	V	1

Note : 1. All Voltages are referenced to ground

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$, V_{CC} = +5V ±10%)

Symbol	Parameter	Min.	Max.	Units	Note
I_{CC1}	Average V_{CC} Power Supply Current		120	mA	1
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ /$\overline{RT}$ = V_{IH})		12	mA	1
I_{CC3}	Power Down Current (Inputs ≥ V_{CC} -0.2V)		2	mA	1
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	2
I_{OL}	Output Leakage Current	–10	10	µA	3
V_{OH}	Output Logic 1 Voltage (I_{OUT} = -4.0mA)	2.4		V	4
V_{OL}	Output Logic 0 Voltage (I_{OUT} = 8.0mA)		0.4	V	4

Notes : 1. I_{CC} measurements are made with outputs open.
2. Measured with $0.4V \leq V_{IN} \leq V_{CC}$.
3. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
4 All voltages are referenced to ground.

CAPACITANCE (T_A= 25°C, f= 1MHz)

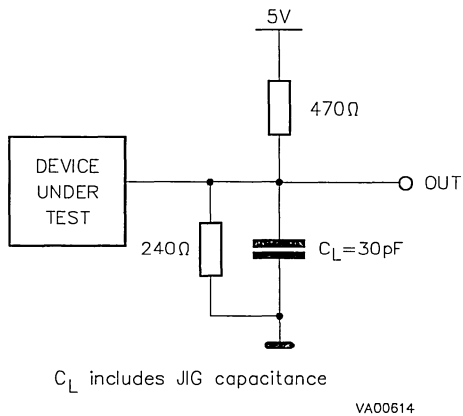
Symbol	Parameter	Typ.	Max.	Unit	Note
C_1	Capacitance on Input Pins		8	pF	1
C_0	Capacitance on Output Pins		12	pF	1,2

Notes : 1. This parameter is only sampled and not 100% tested
2. Output buffer deselected

AC TEST CONDITIONS

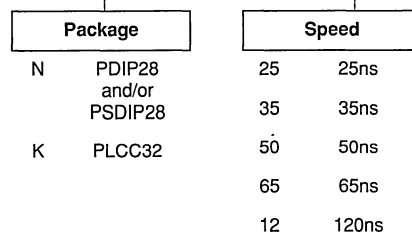
Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	5	ns
Input Signal Timing Reference Level	1.5	V
Output Signal Timing Reference Levels	1.5 and 1.9	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ±10%	V

Figure 17. Equivalent Output Load Circuit



ORDERING INFORMATION

Example: MK45H04 N 25



For a list of available options of Package and Speed, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.

ZEROPOWER MEMORIES

CMOS 2K x 8 ZEROPOWER SRAM

- LOW CURRENT (1µA @ 70°C) BATTERY INPUT FOR DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- + 5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- LOW POWER 440mW ACTIVE ; 5.5mW STANDBY
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- LOW-BATTERY WARNING
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE:
  – MK48C02A 4.75V ≥ V_{PFD} ≥ 4.50V
  – MK48C12A 4.50V ≥ V_{PFD} ≥ 4.20V
- POWER FAIL INTERRUPT OUTPUT

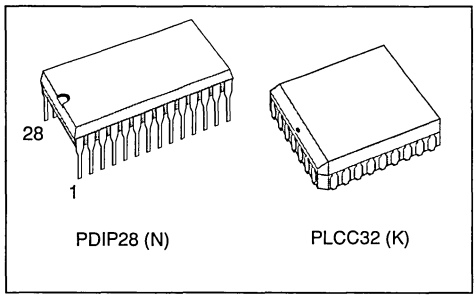
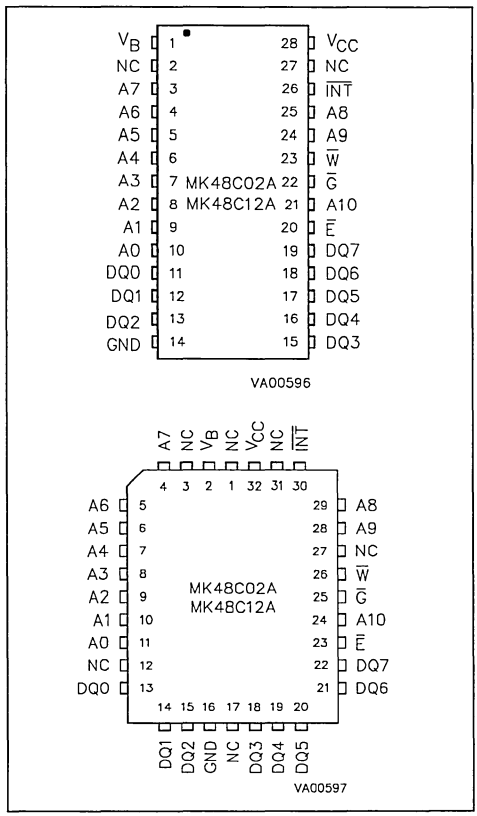


Figure 1. Pin Connections



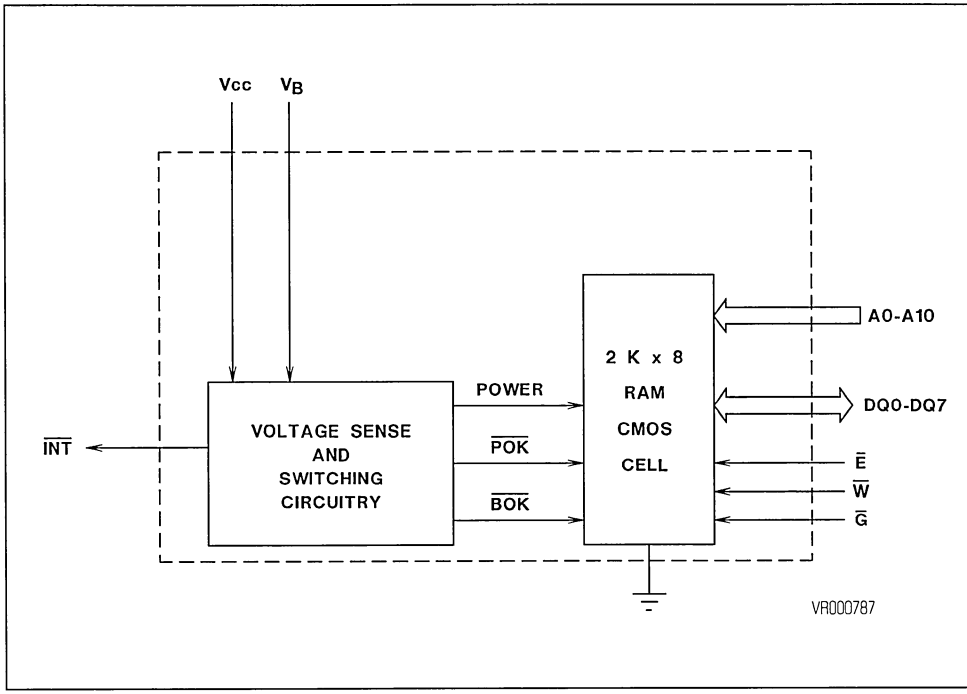
DESCRIPTION

The MK48C02A/12A ZEROPOWER™ are CMOS RAM memories with internal power fail support circuitry for battery backup applications. The fully static RAM uses an HCMOS six transistor cell and is organized 2K x 8. Included in the device is a feature to conserve battery energy and a method of providing data security during V_{CC} transients. A precision voltage detector write-protects the RAM to prevent inadvertent loss of data when V_{CC} falls

PIN NAMES

A0-A10	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
GND	Ground
V_{CC}	5 Volts
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
V_B	Battery Input
$\overline{INT}$	Power Fail Interrupt (Open Drain Type)
NC	No Connected

Figure 2. Block Diagram



DESCRIPTION (Continued)

out of tolerance. In this way, all input and output pins (including $\overline{E}$ and $\overline{W}$) become "don't care". The device permits full functional ability of the RAM for V_{CC} above 4.75V (MK48C02A) and 4.5V (MK48C12A). Data protection is provided for V_{CC} below 4.5V (MK48C02A) and 4.2V (MK48C12A), and maintains data in the absence of V_{CC} with no additional support circuitry other than a primary cell. The current supplied by the battery during data retention is for junction leakage only (typically less than 5nA) because all power-consuming circuitry is turned off. The low battery drain allows use of a long life Lithium primary cell.

TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	DQ
<V_{CC}(max)	V_{IH}	X	X	Deselect	High-Z
	V_{IL}	X	V_{IL}	Write	D_{IN}
>V_{CC}(min)	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z
<V_{PFD}(min)>V_{SO}	X	X	X	Power-Fail Deselect	High-Z
≤V_{SO}	X	X	X	Battery Back-up	High-Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage On Any Pin Relative to Ground	–0.3 to +7.0	V
T_A	Ambient Operating Temperature	0 to +70	°C
T_{STG}	Ambient Storage (V_{CC} Off) Temperature	–55 to +125	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current Per Pin	20	mA

Notes: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION : *Under no conditions can the "Absolute Maximum Ratings" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e. do not force these pins below – 0.3V DC.*

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48C02A)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48C12A)	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2
V_B	Battery Voltage	1.8	4.0	V	1

DC ELECTRICAL CHARACTERISTICS

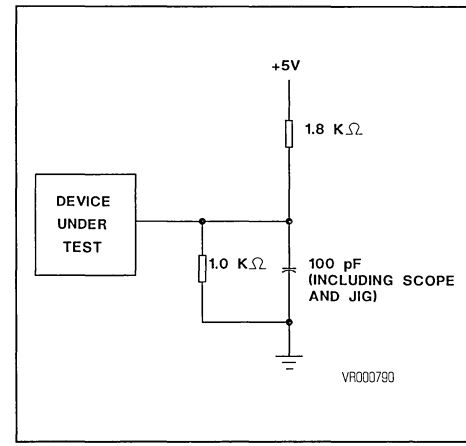
(0°C ≤ T_A ≤ 70°C $V_{CC\ max}$ ≥ V_{CC} ≥ $V_{CC\ min}$)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E}$= V_{IH})		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E}$ ≥ V_{CC} –0.2V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	4
I_{OL}	Output Leakage Current	–5	5	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –1.0mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1mA)		0.4	V	
V_{PFL}	INT Logic "0" Voltage (I_{OUT} = 0.5 mA)		0.4	V	
I_{BATT}	Battery Backup Current V_B = 4.0V		1	µA	
I_{CHG}	Battery Charging Current V_{CC} = 5.5V	–5	5	nA	
V_{LB}	Battery OK Flag	1.8	2.6	V	

AC TEST CONDITIONS

Input Levels	0.6 V to 2.4 V
Transition Times	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V

OUTPUT LOAD DIAGRAM



CAPACITANCE

(T_A = 25°C)

Symbol	Parameter	Max.	Notes
C_I	Capacitance on all pins (except D/Q)	7 pF	5
$C_{D/Q}$	Capacitance on D/Q pins and $\overline{INT}$	10 pF	4, 5

Notes :

1. All voltages referenced to GND
2. Negative spikes of – 1.0 volts allowed for up to 10ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with GND ≤ V_I ≤ V_{CC} and outputs deselected.
5. Effective capacitance calculated from the equation C = I Δt/ΔV with ΔV = 3 volts and power supply at nominal level.

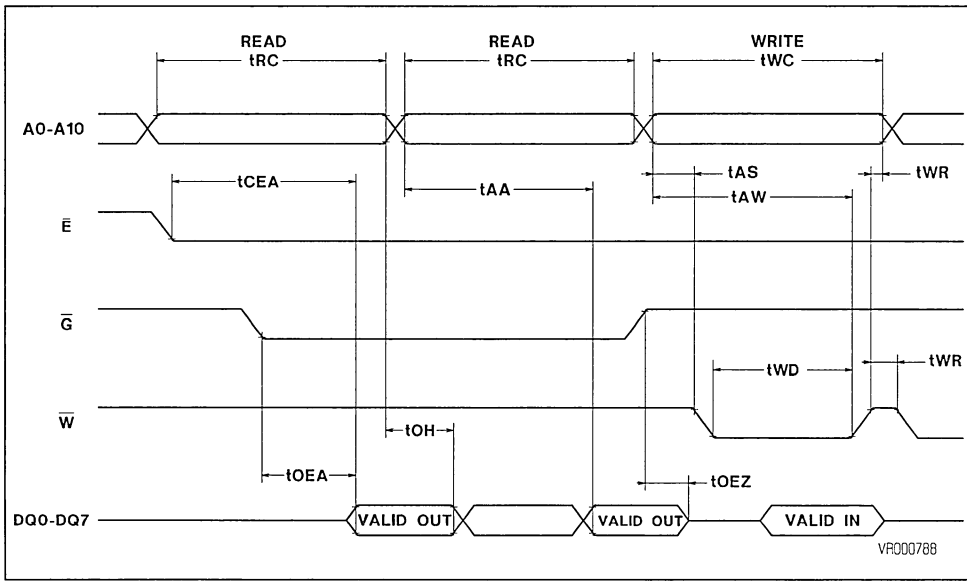
OPERATION

Read Mode

The MK48C02A/12A is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

Figure 3. Read-Read-Write Timing



AC ELECTRICAL CHARACTERISTICS (Read Cycle Timing)

($0°C \leq T_A \leq 70°C$; $V_{CC\,max} \geq V_{CC} \geq V_{CC\,min}$)

Symbol	Parameter	48CX2A-15		48CX2A-20		48CX2A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		ns	1

Note : Measured using the Output Load Diagram shown page 4.

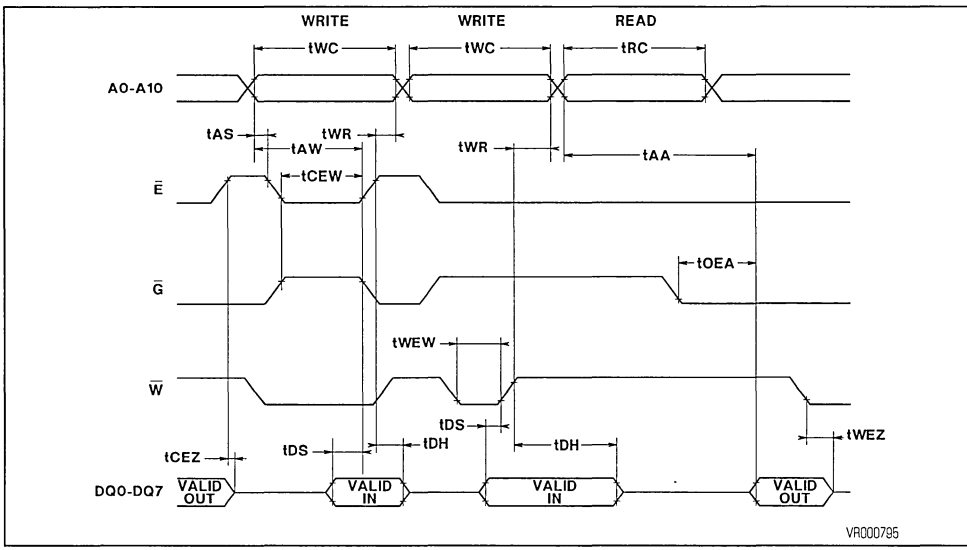
WRITE MODE

The MK48C02A/12A is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high, for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterwards.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stabilizes.

The MK48C02A/12A $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

Figure 4. Write-Write-Read Timing



AC ELECTRICAL CHARACTERISTICS (Write Cycle Timing)

(0°C ≤ T_A ≤ 70°C; $V_{CC\ max}$ ≥ V_{CC} ≥ $V_{CC\ min}$)

Symbol	Parameter	48CX2A-15		48CX2A-20		48CX2A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	150		200		250		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{AW}	Address Valid to End of Write	120		140		180		ns
t_{CEW}	Chip Enable to End of Write	90		120		160		ns
t_{WEW}	Write Enable to End of Write	90		120		160		ns
t_{WR}	Write Recovery Time	10		10		10		ns
t_{DS}	Data Setup Time	40		60		100		ns
t_{DH}	Data Hold Time	5		5		5		ns
t_{WEZ}	Write Enable Low to High-Z		50		60		80	ns

DATA RETENTION MODE

With V_{CC} applied, the MK48C02A/12A operates as a conventional BYTEWIDE static RAM. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48C02A has a V_{PFD} (max) - V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48C12A has a V_{PFD} (max) - V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note : A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48C02A/12A may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

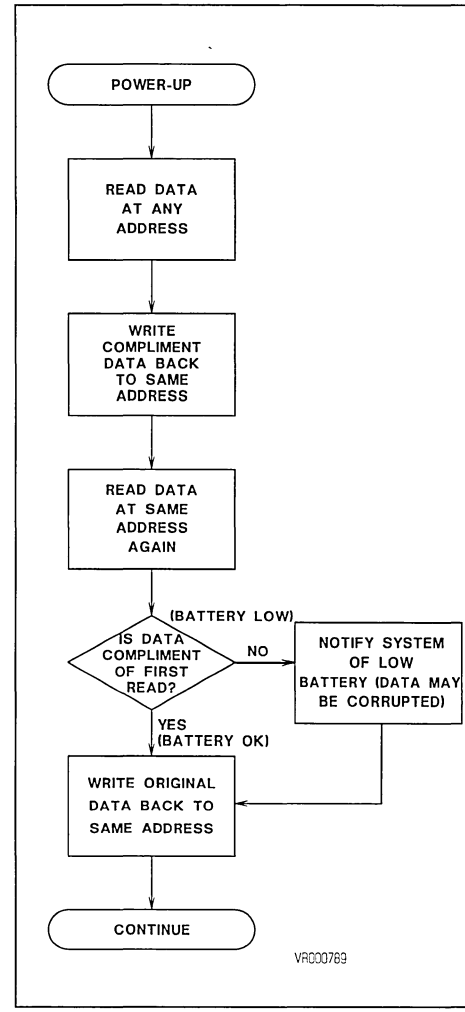
The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

INTERRUPT FUNCTION

The MK48C02A/12A provides a power-fail interrupt output labeled $\overline{INT}$. The $\overline{INT}$ pin eliminates the need for external power sensing components in applications where an orderly shut down of the system is necessary. The $\overline{INT}$ pin is open drain for "wire or" applications and provides the user with 10µs to 40µs advanced warning of an impending power-fail write protect.

Figure 5. Checking the $\overline{BOK}$ Flag Status



AC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Timing)
(0°C ≤ T_A ≤ +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300			µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10			µs	3
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1			µs	
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0			µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after V_{PFD} (max)	120			µs	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10		40	µs	
t_{PFH}	V_{PFD} (max) to $\overline{INT}$ High			120	µs	4

DC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Trip Point Voltages)
(0°C ≤ T_A ≤ +70°C)

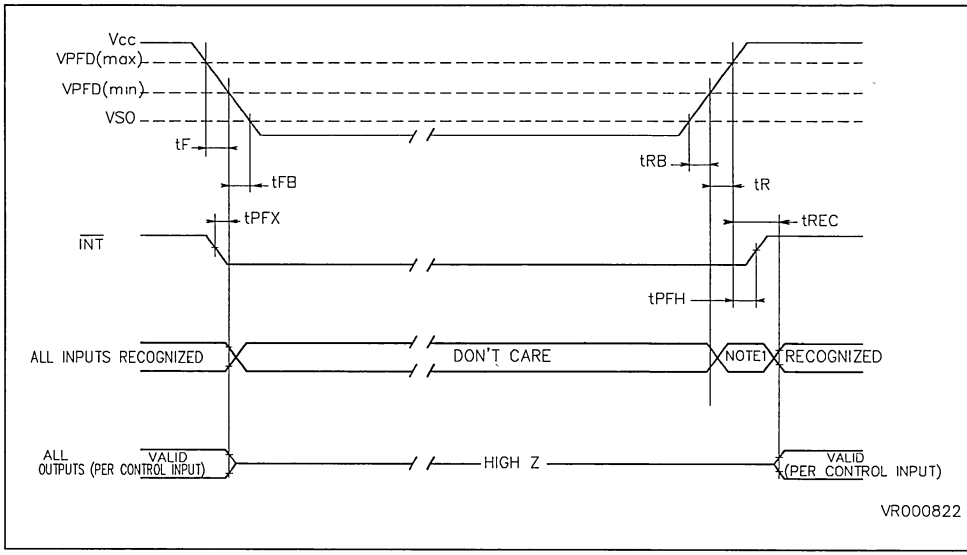
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{PFD}	Power-Fail Deselect Voltage (MK48C02A)	4.50	4.6	4.75	V	1
V_{PFD}	Power-Fail Deselect Voltage (MK48C12A)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-Up Switchover Voltage		3		V	1

Notes :

1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 40µs after V_{CC} passes V_{PFD} (Min).
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.
4. $\overline{INT}$ may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

CAUTION: *Negative Undershoots Below -0.3V are not allowed on any pin while in Battery Back-up mode .*

Figure 6. Power-Down/Power-Up Timing



Notes :

1. Inputs may or may not be recognized at this time.
2. Caution should be taken to keep $\overline{E}$ or $\overline{W}$ in the high state V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertent write cycles after Vcc rises but before normal system operation begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

ORDERING INFORMATION

Example: MK48C02 K 15

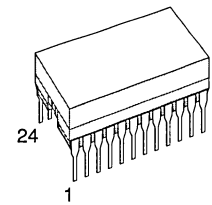
Package		Speed	
N	PDIP28	15	150ns
K	PLCC32	20	200ns
		25	250ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

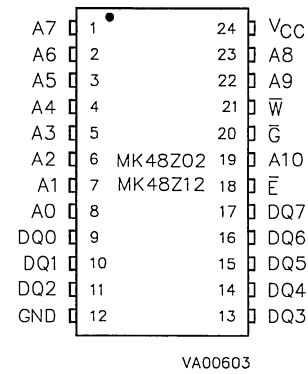
CMOS 2K x 8 ZEROPOWER SRAM

- PREDICTED WORST CASE BATTERY LIFE OF 11 YEARS @ 70°C
- DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- + 5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- FULL CMOS-440mW ACTIVE ; 5.5mW STANDBY
- 24-PIN DUAL IN LINE PACKAGE, JEDEC PINOUTS
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- LOW-BATTERY WARNING
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE:
  - MK48Z02 4.75V ≥ V_{PFD} ≥ 4.50V
  - MK48Z12 4.50V ≥ V_{PFD} ≥ 4.20V



PHDIP24 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connection



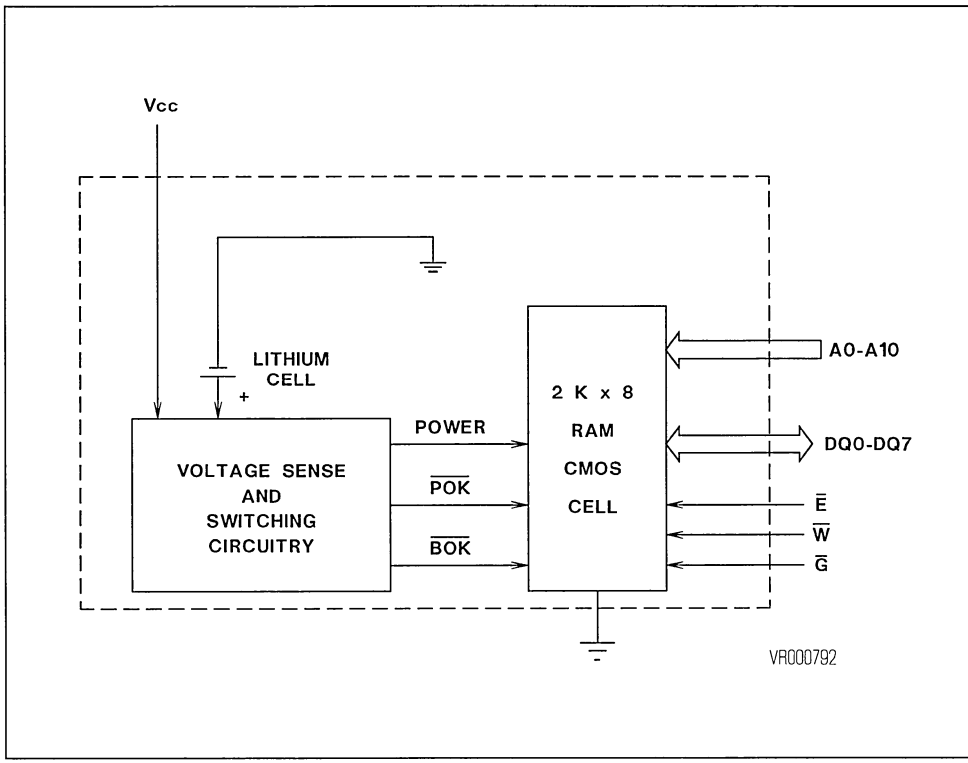
DESCRIPTION

The MK48Z02/12 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an en-ergy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace existing 2K x 8 static RAM, directly conforming to the popular Byte Wide 24-pin DIP package (JEDEC). MK48Z02/12 also matches the pinning of 2716 EPROM and 2K x 8 EEPROM. Like other static RAMs, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250ns and require only + 5 volts, no additional support circuitry is needed for interface to a microprocessor.

PIN NAMES

A0-A10	Address Inputs
$\overline{E}$	Chip Enable
GND	Ground
V_{CC}	5 Volts
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Inputs/Outputs

Figure 2. Block Diagram



TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	DQ
$<V_{CC(max)}$ $>V_{CC(min)}$	V_{IH} V_{IL} V_{IL} V_{IL}	X X V_{IL} V_{IH}	X V_{IL} V_{IH} V_{IH}	Deselect Write Read Read	High-Z D_{IN} D_{OUT} High-Z
$<V_{PFD(min)}$ $>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage On Any Pin Relative to Ground	–0.3 to +7.0	V
T_A	Ambient Operating Temperature	0 to +70	°C
T_{STG}	Ambient Storage (V_{CC} Off) Temperature	–40 to +85	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current Per Pin	20	mA

NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION : *Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e. do not force these pins below – 0.3V DC.*

RECOMMENDED DC OPERATING CONDITIONS
(0°C ≤ T_A ≤ 70°C)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48Z02)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48Z12)	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

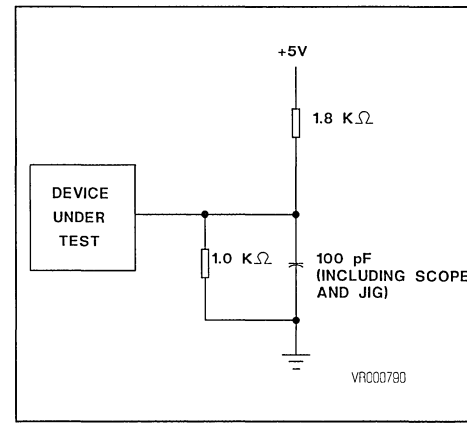
DC ELECTRICAL CHARACTERISTICS
(0°C ≤ T_A ≤ 70°C; $V_{CC\,max} \geq V_{CC} \geq V_{CCmin}$)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \geq V_{CC}$ –0.2V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	4
I_{OL}	Output Leakage Current	–5	5	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –1.0mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1mA)		0.4	V	

AC TEST CONDITIONS

Input Levels	0.6V to 2.4V
Transition Times	5ns
Input and Output Timing Reference Levels	0.8V or 2.2V

EQUIVALENT OUTPUT LOAD DIAGRAM



CAPACITANCE

(T_A = 25°C)

Symbol	Parameter	Max.	Notes
C_I	Capacitance on all pins (except D/Q)	7 pF	4
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4, 5

Notes :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with $V_{CC} \geq V_I \geq$ GND and outputs deselected.
5. Effective capacitance calculated from the equation $C = I \Delta t/\Delta V$ with ΔV = 3 volts and power supply at 5.0V.

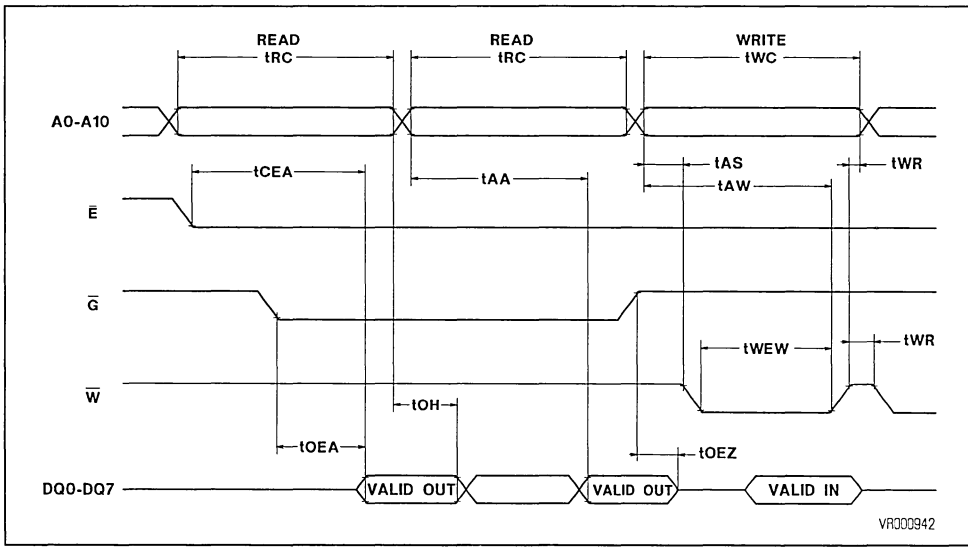
OPERATION

READ MODE

The MK48Z02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

Figure 3. Read-Read-Write Timing



AC ELECTRICAL CHARACTERISTICS (Read Cycle Timing)

(0°C ≤ T_A ≤ 70°C; $V_{CC\,max} \geq V_{CC} \geq V_{CC}$ min)

Symbol	Parameter	48Z02-12		48Zx2-15		48Zx2-20		48Zx2-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		120		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		30		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		30		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		15		ns	1

Note : Measured using the Output Load Diagram shown Page 4.

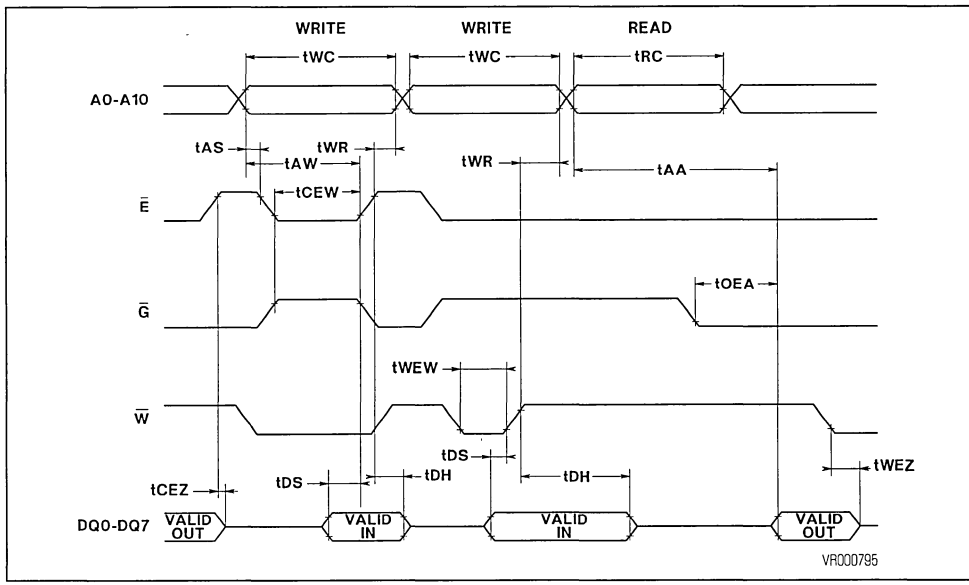
WRITE MODE

The MK48Z02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stabilizes.

The MK48Z02/12 $\overline{G}$ input is a DON'T CARE in the write mode, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

Figure 4. Write-Write-Read Timing



AC ELECTRICAL CHARACTERISTICS (Write Cycle Timing)

($0°C \le T_A \le 70°C$; $V_{CC\,max} \ge V_{CC} \ge V_{CC\,min}$)

Symbol	Parameter	48Z02-12		48Zx2-15		48Zx2-20		48Zx2-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{AW}	Address Valid to End of Write	90		120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	75		90		120		160		ns	
t_{WEW}	Write Enable to End of Write	75		90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		10		ns	
t_{DS}	Data Setup Time	35		40		60		100		ns	
t_{DH}	Data Hold Time	5		5		5		5		ns	
t_{WEZ}	Write Enable Low to High-Z		40		50		60		80	ns	

DATA RETENTION MODE

With V_{CC} applied, the MK48Z02/12 operates as a conventional BYTEWIDE static RAM. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48Z02 has a V_{PFD} (max) - V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48Z12 has a V_{PFD} (max) - V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note : A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48Z02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

Figure 5. Checking the $\overline{BOK}$ Flag Status

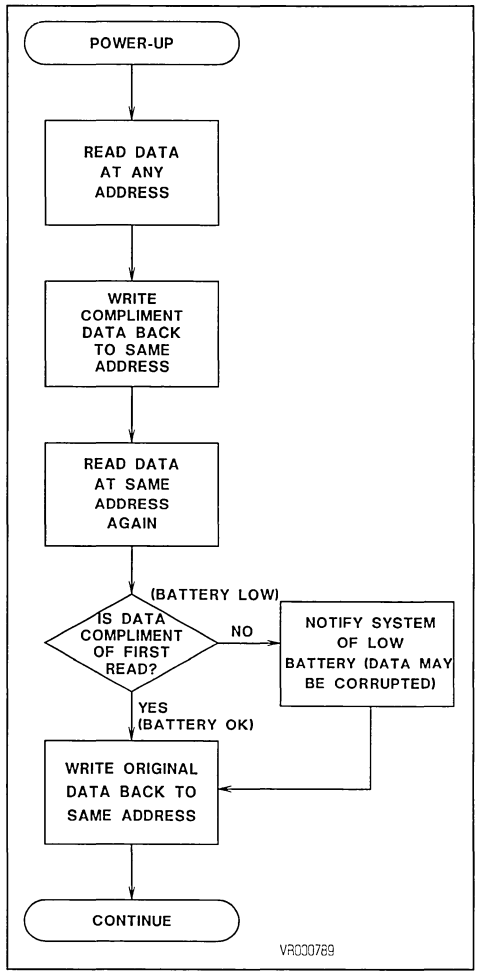
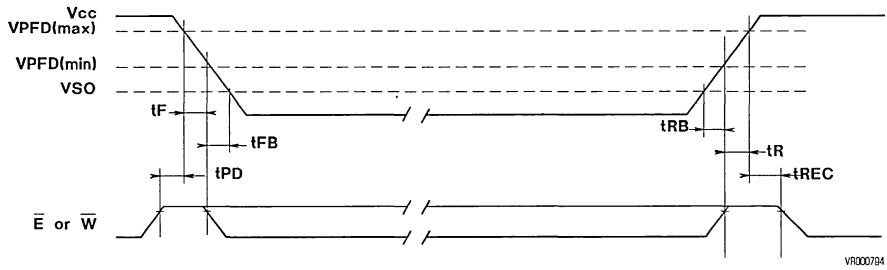


Figure 6. Power-Down/Power-Up Timing



DC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Trip Point Voltages)
(0°C ≤ T_A ≤ +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{PFD}	Power-Fail Deselect Voltage (MK48Z02)	4.50	4.6	4.75	V	1
V_{PFD}	Power-Fail Deselect Voltage (MK48Z12)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-Up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Timing)
(0°C ≤ T_A ≤ +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0			ns	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300			µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10			µs	3
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1			µs	
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0			µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2			ms	

Notes :
1. All voltages referenced to GND.
2. V_{PFD} (max) to V_{PFD} (min) fall times of less t_F may result in deselection/write protection not occurring until 50µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.

DATA RETENTION TIME

About Figure 7

Figure 7 illustrates how expected MK48Z02/12 battery life is influenced by temperature. The life of the battery is controlled by temperature and is virtually independent of the percentage of time the MK48Z02/12 spends in battery back-up mode.

Battery life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-tem-perature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's ongoing battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note : The summary presented in Figure 7 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final ; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 7 indicates that a particular MK48Z02/12 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years ; 50% of them can be expected to fail within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case ana-lysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48Z02/12 is marked with a nine digit manufacturing date code in the form H99XXYYZZ, example: H995B9231 is H-fabricated in Carrollton, TX; 9- assembled in Muar, Malaysia; 9-tested in Muar, Malaysia; 5B-lot designator; 9231-assembled in the year 1992, work week 31.

CALCULATING PREDICTED BATTERY LIFE

As Figure 7 indicates, the predicted life of the battery in the MK48Z02/12 is a function of temperature. The back-up current required by the memory matrix in the MK48Z02/12 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 7. If the MK48Z02/12 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{1}{[(TA_1/TT)/BL_1)] + [(TA_2/TT)/BL_2] + \ldots + [(TA_n/TT)/BL_n)]}$$

Where: TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

BL_1, BL_2, BL_n = Predicted Battery Lifetime at Temp 1, Temp 2, etc (see Figure 7).

EXAMPLE PREDICTED BATTERY LIFE CALCULATION

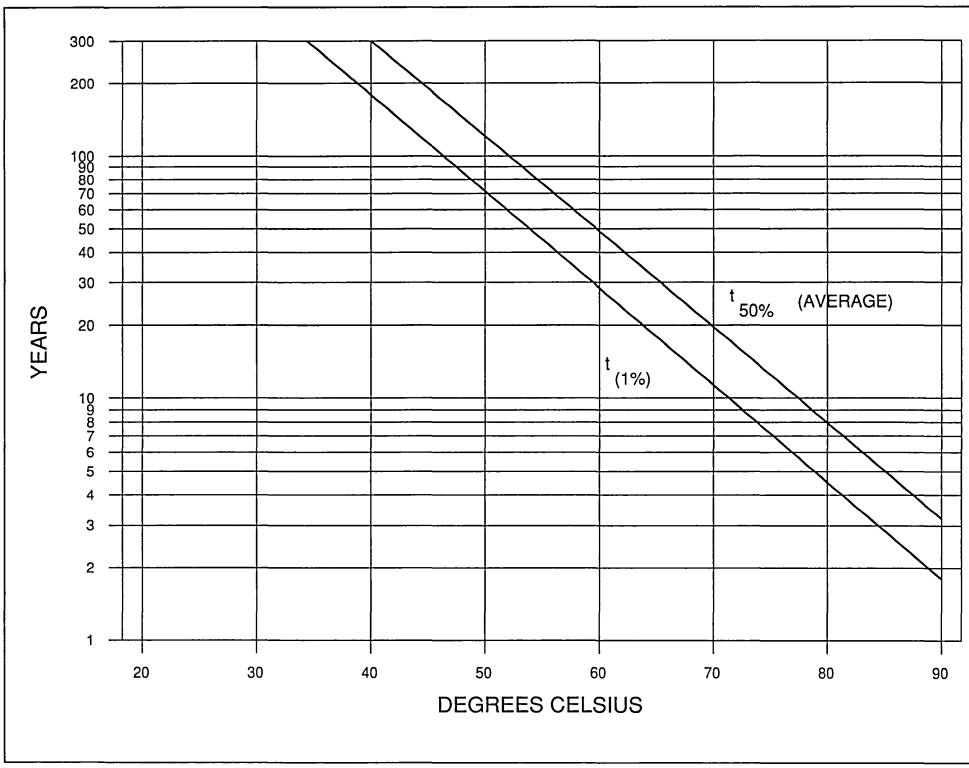
A cash register/terminal operates in an environment where the MK48Z02/12 is exposed to temperatures of 30°C or less for 3066 hrs/yr ; temperatures greater than 25°C, but less than 40°C for 5256 hrs/yr ; and temperatures greater than 40°C, but less than 70°C for the remaining 438 hrs/yr.

Reading predicted typical life values from Figure 7 ; BL_1 = 456 yrs., BL_2 = 175 yrs., BL_3 = 11.4 yrs.
Total Time (TT) = 8760 hrs./yr. TA_1 = 3066 hrs./yr. TA_2 = 5256 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Battery Life} \geq \frac{1}{[(3066/8760)/456] + [(5256/8760)/175] + [(438/8760)/11.4]}$$

$$\geq 116.5 \text{ yrs.}$$

Figure 7. Predicted Battery Storage Life Versus Temperature



ORDERING INFORMATION

Example: MK48Z02 B 12

Package		Speed	
B	PHDIP24	12	120ns
		15	150ns
		20	200ns
		25	250ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

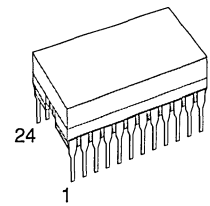
For further information or any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON MICROELECTRONICS

MKI48Z02
MKI48Z12

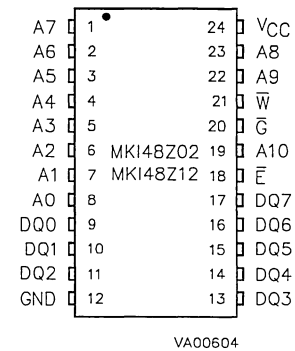
CMOS 2K x 8 ZEROPOWER SRAM

- INDUSTRIAL TEMPERATURE RANGE - 40°C to + 85°C.
- PREDICTED WORST CASE BATTERY LIFE OF 6 YEARS @ 85°C.
- DATA RETENTION IN THE ABSENCE OF POWER.
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE.
- + 5 VOLT ONLY READ/WRITE.
- CONVENTIONAL SRAM WRITE CYCLES.
- LOW POWER-440mW ACTIVE ; 5.5mW STANDBY.
- 24-PIN DUAL IN LINE PACKAGE, JEDEC 24 PIN MEMORY PINOUT.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- ON BOARD LOW-BATTERY WARNING CIRCUITRY.
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE :
  - MKI48Z02 4.75V ≥ V_{PFD} ≥ 4.50V
  - MKI48Z12 4.50V ≥ V_{PFD} ≥ 4.20V



PHDIP24 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connections



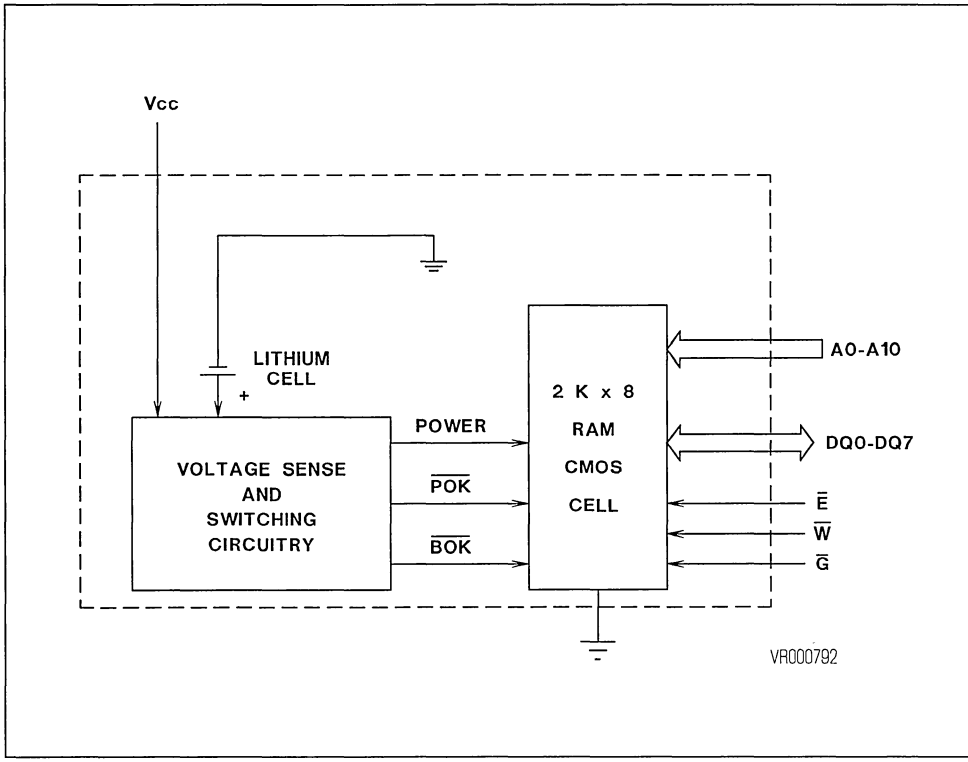
DESCRIPTION

The MKI48Z02/12 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an en-ergy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace exist-ing 2K x 8 static RAM, directly conforming to the popular Byte Wide 24-pin DIP package (JEDEC).

PIN NAMES

A0-A10	Address Inputs
$\overline{E}$	Chip Enable
GND	Ground
V_{CC}	5 Volts
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 - DQ7	Data Inputs/Outputs

Figure 2. Block Diagram



DESCRIPTION (Continued)
MKI48Z02/12 also matches the pinning of 2716 EPROM and 2K x 8 EEPROM. Like other static RAMs, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250ns and require only + 5 volts, no additional support circuitry is needed for interface to a microprocessor.

TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	DQ
$<V_{CC(max)}$	V_{IH}	X	X	Deselect	High-Z
$>V_{CC(min)}$	V_{IL}	X	V_{IL}	Write	D_{IN}
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z
$<V_{PFD(min)}$ $>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage On Any Pin Relative to Ground	–0.3 to +7.0	V
T_A	Ambient Operating Temperature	–40 to +85	°C
T_{STG}	Ambient Storage (V_{CC} Off) Temperature	–40 to +85	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current Per Pin	20	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION : *Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e. do not force these pins below – 0.3V DC.*

RECOMMENDED DC OPERATING CONDITIONS
(–40°C ≤ T_A ≤ +85°C)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MKI48Z02)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MKI48Z12)	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

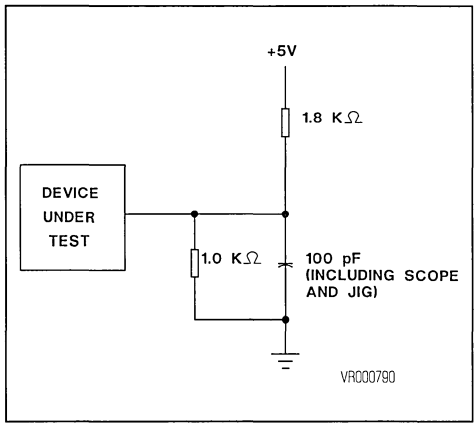
DC ELECTRICAL CHARACTERISTICS
(–40°C ≤ T_A ≤ +85°C; $V_{CC\ max} \geq V_{CC} \geq V_{CC}$ min)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \geq V_{CC}$ –0.2V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	4
I_{OL}	Output Leakage Current	–5	5	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –1.0mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1mA)		0.4	V	

AC TEST CONDITIONS

Input Levels	0.6V to 2.4V
Transition Times	5ns
Input and Output Timing Reference Levels	0.8V or 2.2V
Ambient Temperature	–40 to 85°C
VCC (MKI48Z02)	4.75 to 5.5V
VCC (MKI48Z12)	4.5 to 5.5V

EQUIVALENT OUTPUT LOAD DIAGRAM



CAPACITANCE

(T_A = 25°C)

Symbol	Parameter	Max.	Notes
C_I	Capacitance on all pins (except D/Q)	7 pF	4
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4, 5

Notes :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with $V_{CC} \geq V_I \geq$ GND and outputs deselected.
5. Effective capacitance calculated from the equation C = I $\Delta t/\Delta V$ with ΔV = 3 volts and power supply at 5.0V.

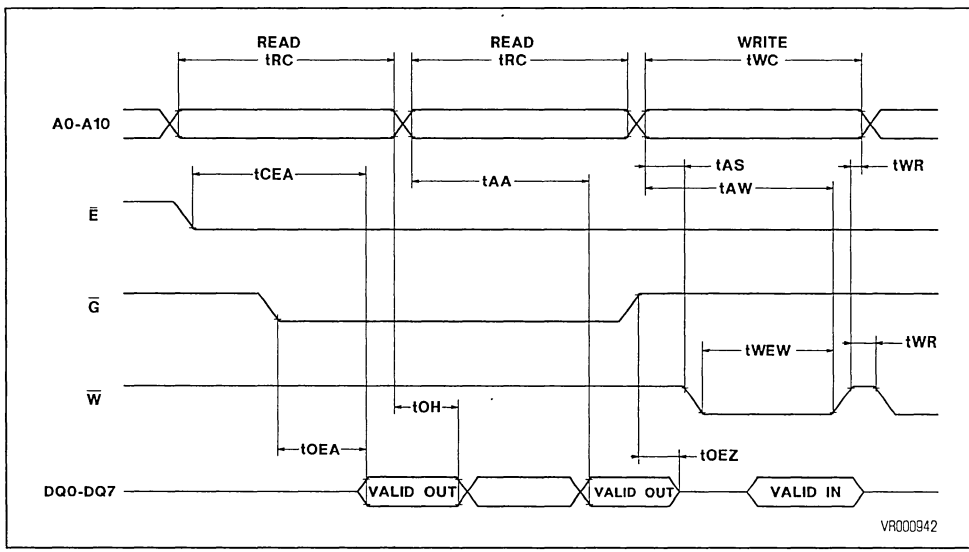
OPERATION

READ MODE

The MKI48Z02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

Figure 3. Read-Read-Write Timing



AC ELECTRICAL CHARACTERISTICS (Read Cycle Timing)

($-40°C \leq T_A \leq +85°C$; V_{CC} max $\geq V_{CC} \geq V_{CC}$ min)

Symbol	Parameter	MKI48ZX2-15		MKI48ZX2-20		MKI48ZX2-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		ns	1

Note : Measured using the Output Load Diagram shown Page 4.

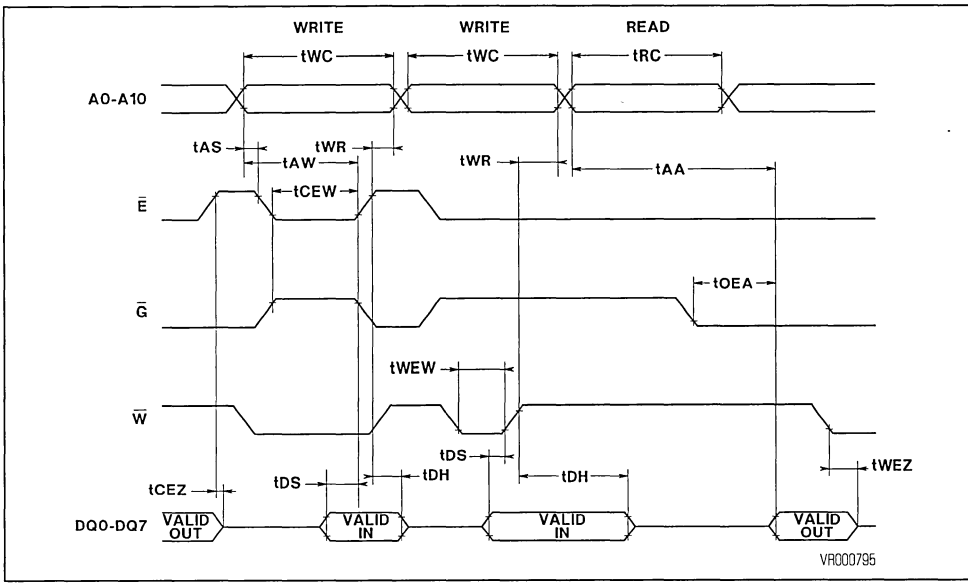
WRITE MODE

The MKI48Z02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterwards.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC}(min) but before the processor stabilizes.

The MKI48Z02/12 $\overline{G}$ input is a don't care in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

Figure 4. Write-Write-Read Timing



AC ELECTRICAL CHARACTERISTICS (Write Cycle Timing)

($-40°C \leq T_A \leq +85°C$; V_{CC} max $\geq V_{CC} \geq V_{CC}$ min)

Symbol	Parameter	MKI48ZX2-15		MKI48ZX2-20		MKI48ZX2-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	90		120		160		ns	
t_{WEW}	Write Enable to End of Write	90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		ns	
t_{DS}	Data Setup Time	40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		50		60		80	ns	

DATA RETENTION MODE

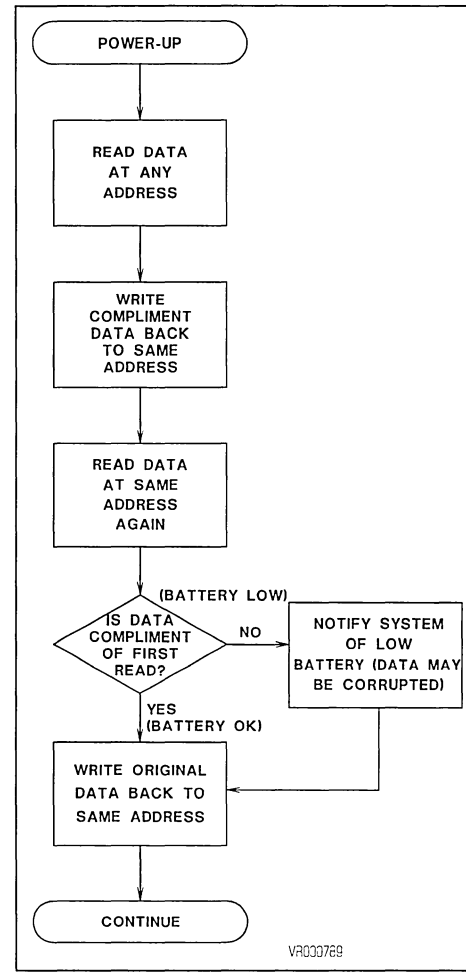
With V_{CC} applied, the MKI48Z02/12 operates as a conventional BYTEWIDE static RAM. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MKI48Z02 has a V_{PFD} (max) to V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MKI48Z12 has a V_{PFD} (max) to V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note : A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MKI48Z02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

Figure 5. Checking the $\overline{BOK}$ Flag Status



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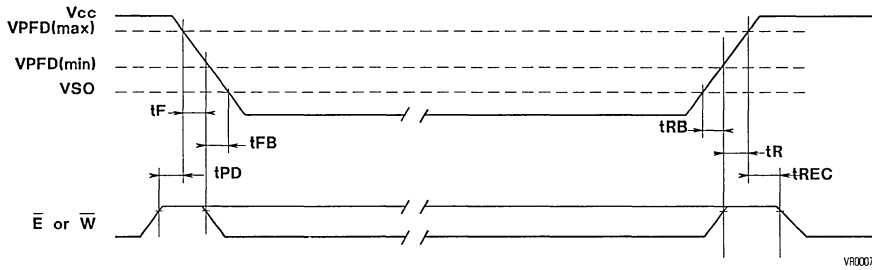

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Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
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V_{SO}	Battery Back-Up Switchover Voltage		3		V	1

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(–40°C ≤ T_A ≤ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0			ns	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300			µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10			µs	3
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1			µs	
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0			µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2			ms	

Notes :

1. All voltages referenced to GND.
2. V_{PFD} (max) to V_{PFD} (min) fall times of less t_F may result in deselection/write protection not occurring until 50µs after V_{CC} passes V_{PFD} (min).
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Battery life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's ongoing battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note : The summary presented in Figure 7 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final ; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 80°C is at issue, Figure 7 indicates that a particular MKI48Z02/12 has a 1% chance of having a battery failure 10 years into its life and a 50% chance of failure at the 17 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 10 years ; 50% of them can be expected to fail within 17 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MKI48Z02/12 is marked with a nine digit manufacturing date code in the form H99XXYYZZ, example: H995B9231 is H -fabricated in Carrollton, TX; 9 -assembled in Muar, Malaysia; 9 -tested in Muar, Malaysia; 58 -lot designator; 9231 -assembled in the year 1992, work week 31.

CALCULATING PREDICTED BATTERY LIFE

As Figure 7 indicates, the predicted life of the battery in the MKI48Z02/12 is a function of temperature. The back-up current required by the memory matrix in the MKI48Z02/12 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 7. If the MKI48Z02/12 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{1}{[(TA_1/TT)/BL_1)] + [(TA_2/TT)/BL_2] + \ldots + [(TA_n/TT)/BL_n)]}$$

Where: TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

BL_1, BL_2, BL_n = Predicted Battery Lifetime at Temp 1, Temp 2, etc (see Figure 7).

EXAMPLE PREDICTED BATTERY LIFE CALCULATION

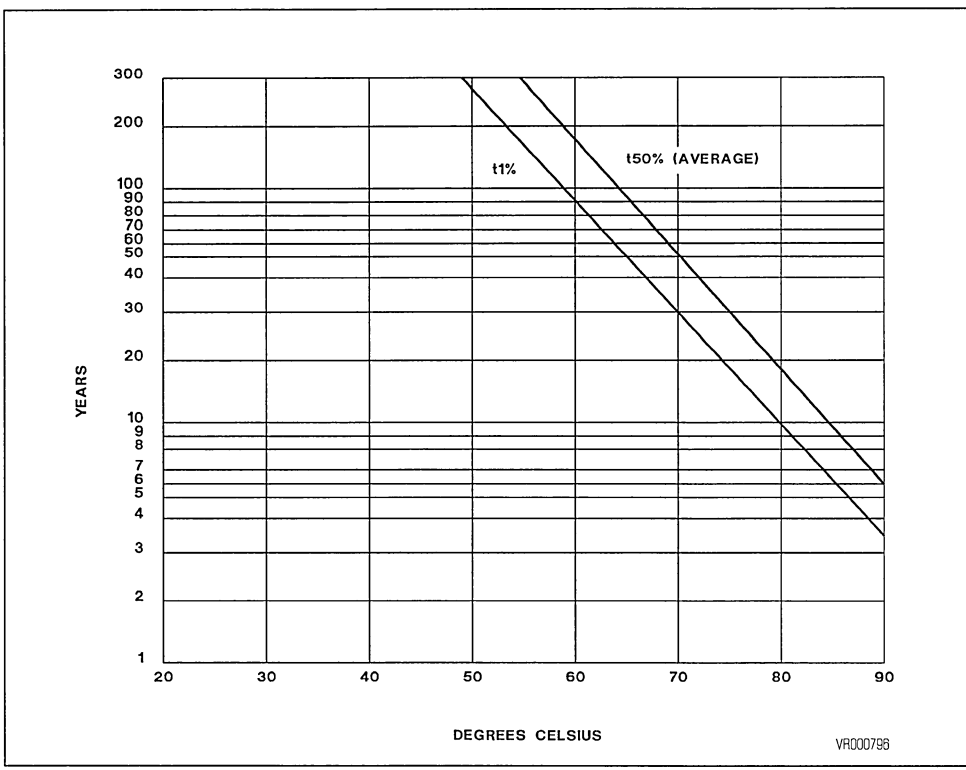
A process control computer operates in an environment where the MKI48Z02/12 is exposed to temperatures of 50°C or less for 3066 hrs/yr ; temperatures greater than 25°C, but less than 60°C for 5256 hrs/yr ; and temperatures greater than 40°C, but less than 85°C for the remaining 438 hrs/yr.

Reading predicted typical life values from Figure 7 ; BL_1 = 275 yrs., BL_2 = 95 yrs., BL_3 = 6 yrs.
Total Time (TT) = 8760 hrs./yr. TA_1 = 3066 hrs./yr. TA_2 = 5256 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Battery Life} \geq \frac{1}{[(3066/8760)/275] + [(5256/8760)/95] + [(438/8760)/6]}$$

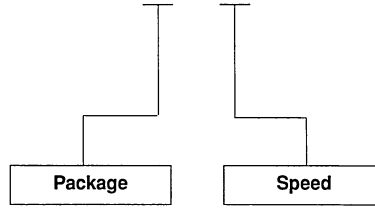
$$\geq 62.8 \text{ yrs.}$$

Figure 7. Predicted Battery Storage Life Versus Temperature



ORDERING INFORMATION

Example: MKI48Z02 B 15



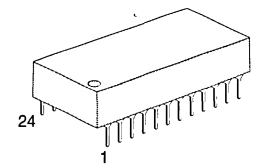
Package		Speed	
B	PHDIP24	15	150ns
		20	200ns
		25	250ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

CMOS 2K x 8 ZEROPOWER SRAM

- PIN and FUNCTION COMPATIBLE with the MK48Z02,12
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- 11 YEARS of DATA RETENTION in the ABSENCE of POWER
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z02: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z12: 4.2V ≤ V_{PFD} ≤ 4.5V



PCDIP24 (PC)
Battery CAPHAT

DESCRIPTION

The M48Z02,12 ZEROPOWER® RAM is a 2K x 8 non-volatile static RAM which is pin and function compatible with the MK48Z02,12.

A special 24 pin 600mil DIP CAPHAT™ package houses the M48Z02,12 silicon with a long life lithium button cell to form a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A10	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

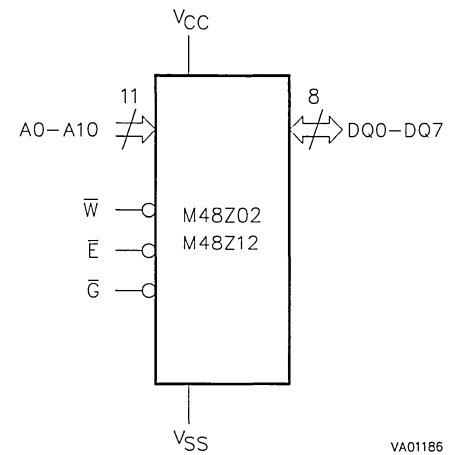
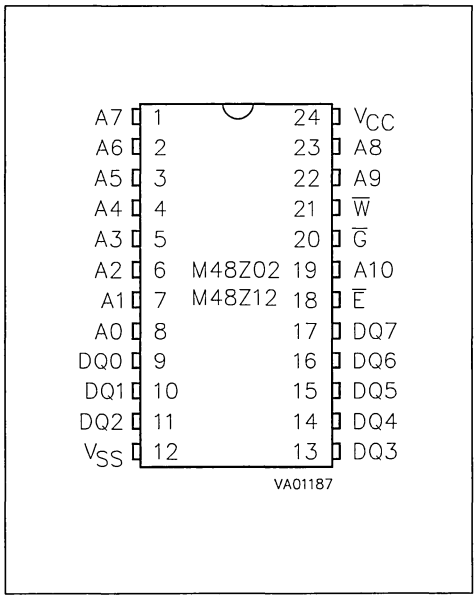


Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

The M48Z02,12 button cell has sufficient capacity and storage life to maintain data for an accumulated time period of at least 11 years in the absence of power over the operating temperature range.

For a complete description of electrical characteristics and bus timing, refer to the MK48Z02,12 data sheet.

ORDERING INFORMATION SCHEME

Example: M48Z02 -120 PC 1

Supply Voltage and Write Protect Voltage

02 V_{CC} = 4.75V to 5.5V
V_{PFD} = 4.5V to 4.75V

12 V_{CC} = 4.5V to 5.5V
V_{PFD} = 4.2V to 4.5V

Speed

-120 120ns

-150 150ns

Package

PC PCDIP24

Temp. Range

1 0 to 70 °C

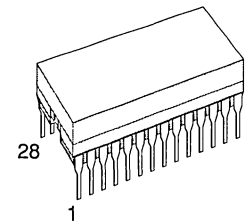
6 –40 to 85 °C

For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 8K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- PREDICTED WORST CASE BATTERY LIFE OF 11 YEARS @ 70°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION.
- CHOICE OF TWO WRITE PROTECT VOLTAGES :
  – MK48Z08/09 - 4.50V ≤ V_{PFD} ≤ 4.75V
  – MK48Z18/19 - 4.20V ≤ V_{PFD} ≤ 4.50V



PHDIP28 WITH BATTERY TOP HAT (B)

DESCRIPTION

The MK48Z08/18/09/19 ZEROPOWER™ RAM combines an 8K x 8 full CMOS SRAM and a long life lithium carbon mono-fluoride battery in a single plastic DIP package. The MK48Z08/18/09/19 is a Non Volatile, pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

In addition, the MK48Z08/18/09/19 has its own Power-fail Detect circuit. The circuit deselects the device whenever V_{CC} is below tolerance, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

PIN NAMES

A0-A12	Address Inputs
$\overline{E}_1$, E_2	Chip Enables
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Inputs/Outputs
$\overline{INT}$	Power Fail Interrupt
V_{CC} / GND	5 Volts / Ground
NC	Not Connected

Figure 1. Pin Connections

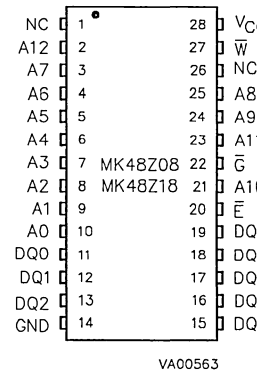
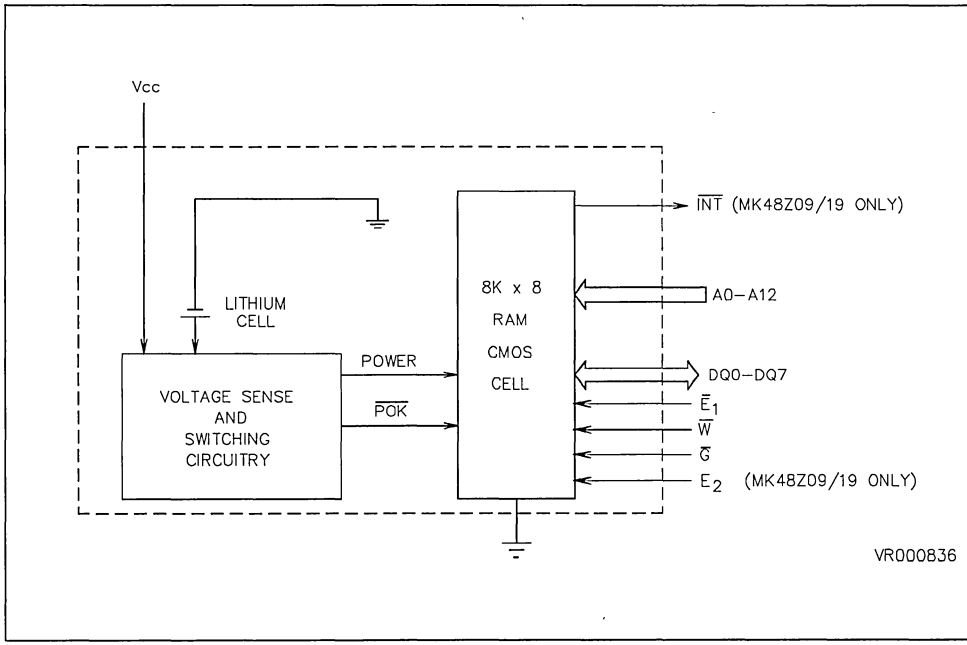


Figure 2. Block Diagram



TRUTH TABLE (MK48Z08/18)

Vcc	E	G	W	Mode	DQ	Power
< Vcc (max)	VIH	X	X	Deselect	High Z	Standby
	VIL	X	VIL	Write	DIN	Active
> Vcc(min)	VIL	VIL	VIH	Read	DOUT	Active
	VIL	VIH	VIH	Read	High Z	Active
< VPFD (min) > VSO	X	X	X	Deselect	High Z	CMOS Standby
≤ VSO	X	X	X	Deselect	High Z	Battery Back-up

TRUTH TABLE (MK48Z09/19)

Vcc	$\overline{E}_1$	E_2	G	W	Mode	DQ	Power
< Vcc (max)	VIH	X	X	X	Deselect	High Z	Standby
	X	VIL	X	X	Deselect	High Z	Standby
	VIL	VIH	X	VIL	Write	DIN	Active
> Vcc(min)	VIL	VIH	VIL	VIH	Read	DOUT	Active
	VIL	VIH	VIH	VIH	Read	High Z	Active
< VPFD (min) > VSO	X	X	X	X	Deselect	High Z	CMOS Standby
≤ VSO	X	X	X	X	Deselect	High Z	Battery Back-up

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
P_D	Total Power Dissipation	1.0	W
I_{OUT}	Output Current per Pin	20	mA
V_{DD}	Voltage on any Pin Relative to GND	–0.3 to +7.0	V
T_{STG}	Ambient Storage (V_{CC} Off) Temperature	–40 to 85	°C
T_A	Ambient Operating Temperature	0 to 70	°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION *: Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_A \le 70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48Z08/09)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48Z18/19)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS
($0°C \le T_A \le +70°C$; $V_{CC\,min} \le V_{CC} \le V_{CC\,max}$)

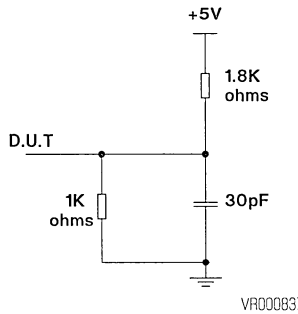
Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current		80, 125	mA	3, 6
I_{CC2}	TTL Standby Current ($\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E}_1 = V_{CC} - 0.2V$)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	5
I_{OL}	Output Leakage Current	–5	5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –1.0mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1mA)		0.4	V	
V_{INT}	$\overline{INT}$ Logic "0" Voltage (I_{OUT} = +0.5mA)		0.4	V	

AC TEST CONDITIONS

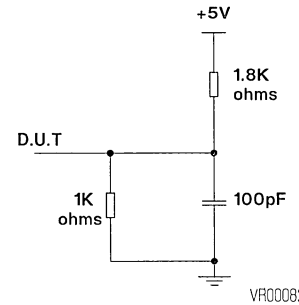
Input Levels	0.0V to 3.0V
Transition Times	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD DIAGRAM

MK48Z08-70



MK48Z08,18,09,19



CAPACITANCE

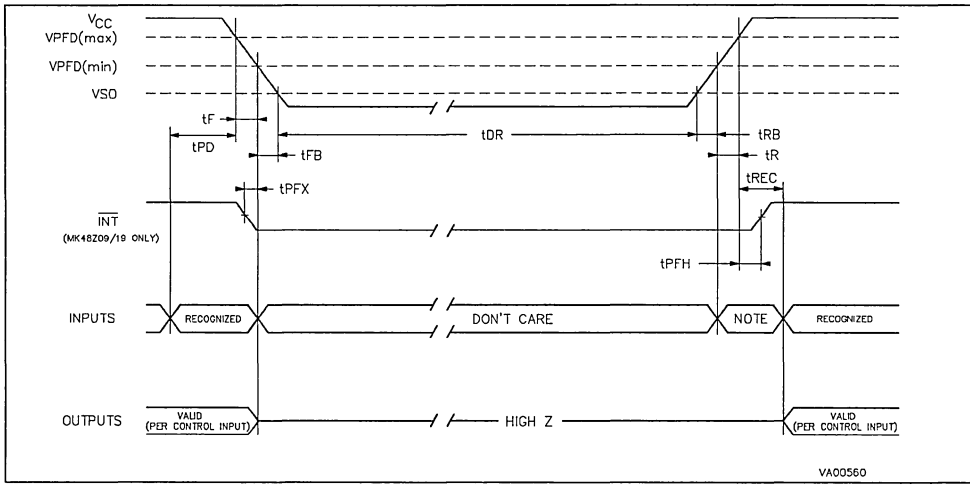
(T_A = 25°C)

Symbol	Parameter	Max.	Unit	Notes
C_I	Capacitance On All Pins (except DQ)	10.0	pF	7
C_Q	Capacitance On DQ Pins	10.0	pF	7, 8

Notes :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with $V_{CC} \geq V_I \geq$ GND and outpus deselected.
6. 80mA@ 100ns, & 125mA @ 70ns.
7. Effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with ΔV = 3 volts and power supply at 5.0V.
8. Measured with outputs deselected.

Figure 3. Power Down/Up Timing



Note: Inputs may not be recognized at this time. Caution should be taken to keep $\overline{E}_1$ high or E_2 low as V_{CC} rises past V_{PFD}(min). Some systems may perform inadvertent write cycles after V_{CC} rises above V_{PFD}(min)but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

AC ELECTRICAL CHARACTERISTICS (Power Up/Down Timing)

($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Max.	Units	Note
t_{PD}	$\overline{E}_1$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} before Power Down	0		µs	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0		µs	
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs	
t_{REC}	$\overline{E}_1$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} after Power Up	1		ms	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs	
t_{PFH}	V_{PFD} (max) to $\overline{INT}$ High		120	µs	4

DC ELECTRICAL CHARACTERISTICS (Power Up/Down Trip Points)

($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Values			Unit	Note
		Min.	Typ.	Max.		
V_{PFD}	Power-fail Deselect Voltage (MK48Z08/09)	4.5	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z18/19)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	11			YEARS	

Notes :
1. All voltages referenced to GND.
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.
4. $\overline{INT}$ may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

READ MODE

The MK48Z08/18/09/19 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E}_1$(Chip Enable 1) is low, and E_2(Chip Enable 2) is high (MK48Z09/19). The device architecture allows ripple-through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and Output Enable access times are satisfied.

If Chip Enable or Output Enable access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by Chip Enable and Output Enable. If the Outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while Chip Enable and Output Enable remain low, output data will remain valid for Output Hold from Address (t_{AXQX}) but will go indeterminate until the next Address Access.

AC ELECTRICAL CHARACTERISTICS (Read Cycle)

($0°C \le T_A \le +70°C$; $V_{CC\ min} \le V_{CC} \le V_{CC\ max}$)

Symbol	Parameter	MK48Z08-70		MK48Zxx-10		Unit	Note
		Min.	Max.	Min.	Max.		
t_{E1LQX}	Chip Enable 1 to Q Low-Z	10		10		ns	
t_{E2HQX}	Chip Enable 2 to Q Low-Z	10		10		ns	
t_{AXQX}	Output Hold from Address	5		5		ns	
t_{GLQX}	Output Enable to Q Low-Z	5		5		ns	
t_{AVAV}	Read Cycle Time	70		100		ns	
t_{AVQV}	Address Access Time		70		100	ns	
t_{E1LQV}	Chip Enable 1 Access Time		70		100	ns	
t_{E2HQV}	Chip Enable 2 Access Time		70		100	ns	
t_{GLQV}	Output Enable Access Time		20		50	ns	
t_{E1HQZ}	Chip Enable 1 to Q High-Z		20		50	ns	
t_{E2LQZ}	Chip Enable 2 to Q High-Z		20		50	ns	
t_{GHQZ}	Output Disable to Q High-Z		15		40	ns	

Figure 4. Read Timing n° 1 (Address Access)

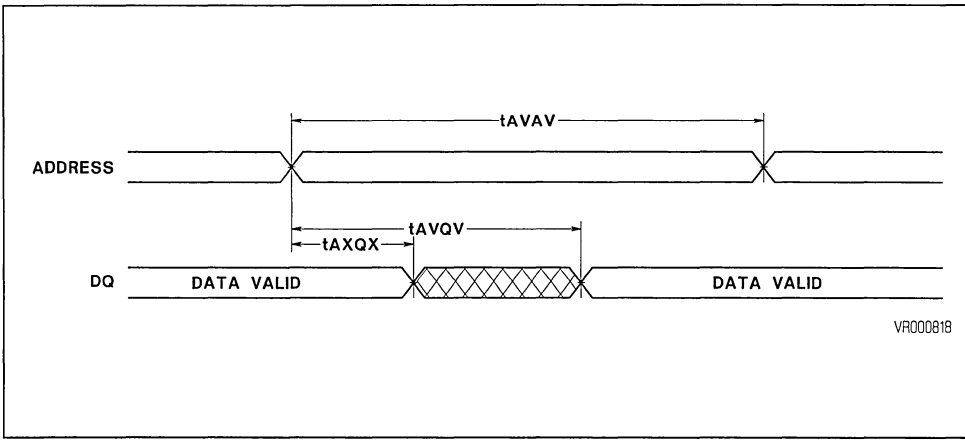
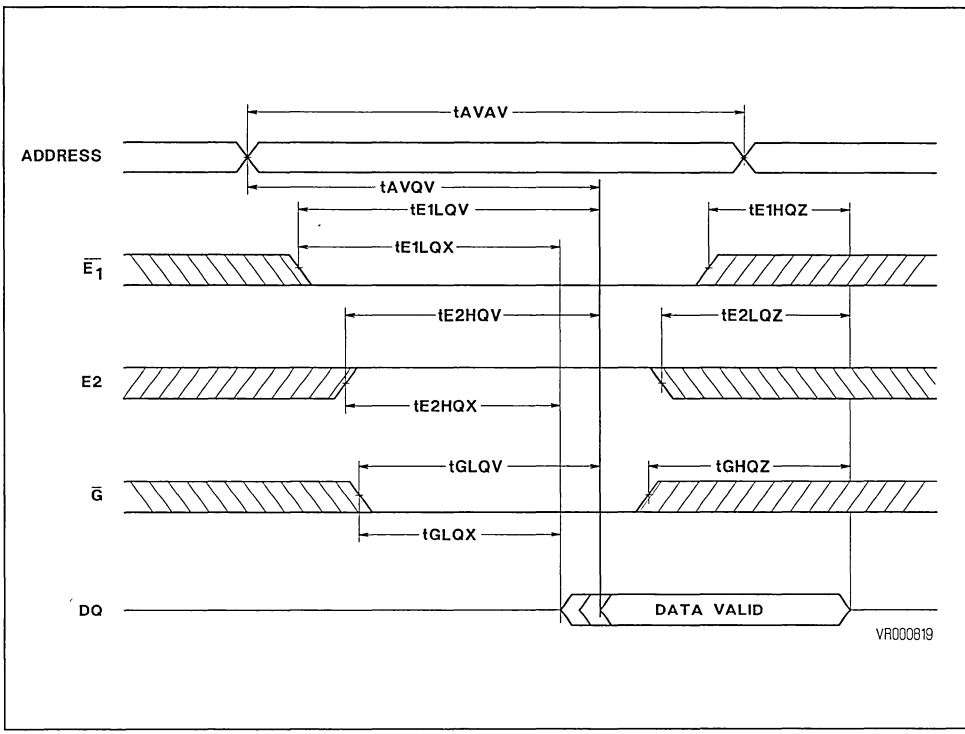


Figure 5. Read Timing n° 2



WRITE MODE

The MK48Z08/18/09/19 is in the Write Mode whenever Write Enable and Chip Enable are active. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E}_1$ or rising edge of E_2 (MK48Z09/19). A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}_1$, or the falling edge of E_2 (MK48Z09/19). The addresses must be held valid throughout the cycle. $\overline{E}_1$ or $\overline{W}$ must return high or E_2 low for minimum of t_{E1HAX} or t_{E2LAX} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterwards.

Because $\overline{G}$ is a Don't Care in the Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ goes low. Take care to avoid bus contention when operating with two-wire control.

AC ELECTRICAL CHARACTERISTICS (Write Cycle)

($0°C \leq T_A \leq +70°C$; $V_{CC\ min} \leq V_{CC} \leq V_{CC\ max}$)

Symbol	Parameter	MK48Z08-70		MK48Zxx-10		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AVWL}	Address Set-Up Time to $\overline{W}$ Low	0		0		ns	
t_{AVE1L}	Address Set-Up Time to Chip Enable Active	0		0		ns	
t_{AVE2H}		0		0		ns	
t_{E1HAX}	Write Recovery from Chip Enable (Address Hold Time)	10		10		ns	2
t_{E2LAX}		10		10		ns	2
t_{WHDX}	Data Hold Time	5		5		ns	1, 2
t_{AVAV}	Write Cycle Time	70		100		ns	
t_{AVWH}	Address Valid to $\overline{W}$ High	50		80		ns	
t_{WLWH}	Write Pulse Width	50		80		ns	
t_{WHAX}	Address Hold after End of Write	10		10		ns	1
t_{E1LE1H}	Chip Enable Active to End of Write	50		80		ns	2
t_{E2HE2L}		50		80		ns	2
t_{DVWH}	Data Valid to End of Write	40		50		ns	1, 2
t_{WHQX}	End of Write to Q Low-Z	10		10		ns	
t_{WLQZ}	$\overline{W}$ Low to Q High-Z		40		50	ns	

Notes :

1. In a $\overline{W}$ Controlled Cycle.
2. In a $\overline{E}_1$, E_2 Controlled Cycle.

Figure 6. Write Control Write Cycle Timing

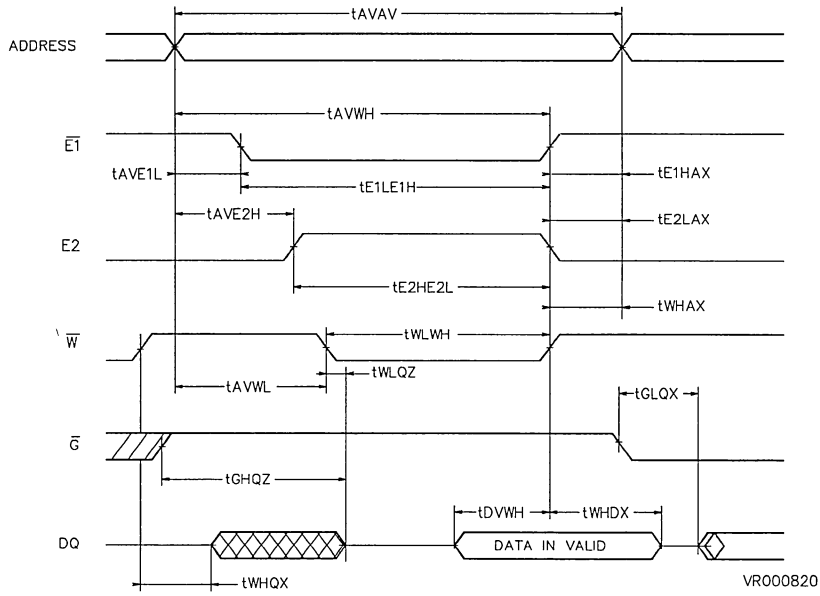
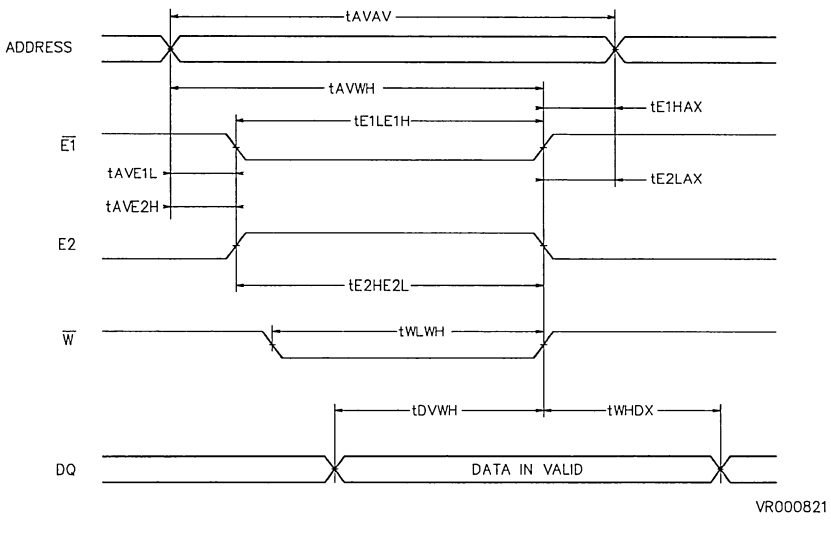


Figure 7. Chip Enable Control Write Cycle Timing



DATA RETENTION MODE

With V_{CC} applied, the MK48Z08/18/09/19 operates as a conventional BYTEWIDE™ Static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window.

Note : A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(Min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The MK48Z08/18/09/19 may respond to transient noise spikes that reach into the deselect window if this should occur during the time the device is sampling V_{CC}. Therefore decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max). Caution should be taken to keep $\overline{E}_1$ high (MK48Z08/18) or E_2 low (MK48Z09/19) as V_{CC} rises past V_{PFD}(min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

POWER FAIL INTERRUPT

The MK48Z09/19 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point of the MK48Z09/19 an interrupt is immediately generated. An internal clock provides a delay no less than 10µs but no greater than 40 µs before automatically deselecting the MK48Z09/19. The $\overline{INT}$ pin is an open drain output and requires an external pull up resistor.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48Z08/18/09/19 is expected to ultimately come to an end for one of two reasons : either because it has been discharged while providing current to an external load ; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

With V_{CC} on, the battery is disconnected from the RAM and aging effects become the determining factor in battery life. With V_{CC} off, leakage currents in the RAM provide the only load on the Battery during battery back-up. For the MK48Z08/18/09/19, the leakage currents are so low that the Back-up System Life of the device is simply the Storage Life of the cell. The Storage Life of the cell is a function of temperature.

PREDICTING STORAGE LIFE

Figure 8 illustrates how temperature affects Storage Life of the MK48Z08/18/09/19 battery. The life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48Z08/18/09/19.

Storage Life predictions presented in Figure 8 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K load resistance.

A Special Note : The summary presented in Figure 8 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final ; they can be expected to change as yet more data becomes available. We believe that future read points of life test presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 8. They are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 8 indicates that a particular MK48Z08/18/09/19 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 11 years ; 50% of them can be expected to experience a failure within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning at the date of manufacture. Each MK48Z08/18/09/19 is marked with a nine digit manufacturing date code in the form H99XXYYZZ, example: H995B9231 is H -fabricated in Carrollton, TX; 9 - assembled in Muar, Malaysia; 9-tested in Muar, Malaysia; 5B - lot designator; 9231 - assembled in the year 1992, work week 31.

Calculating Predicted Storage Life of the Battery

As Figure 8 indicates, the predicted Storage Life of the battery in the MK48Z08/18/09/19 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 8. If the MK48Z08/18/09/19 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

Example Predicted Storage Life Calculation

$$\text{Predicted Storage Life} = 1 / \{ [(TA_1 / TT) / SL_1] + [(TA_2 / TT) / SL_2] + ... + [(TA_N / TT) / SL_N] \}$$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, etc.

$$TT = \text{Total Time} = TA_1 + TA_2 + ... + TA_N$$

SL_1, SL_2, SL_N = Predicted Storage Life at Temp. 1, Temp. 2, etc. (See Figure 8)

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48Z08/18/09/19 is exposed to temperatures of 55°C or less for 8322 hrs./yr.; and temperatures greater than 60°C, but less than 70°C, for the remaining 438 hrs./yr.

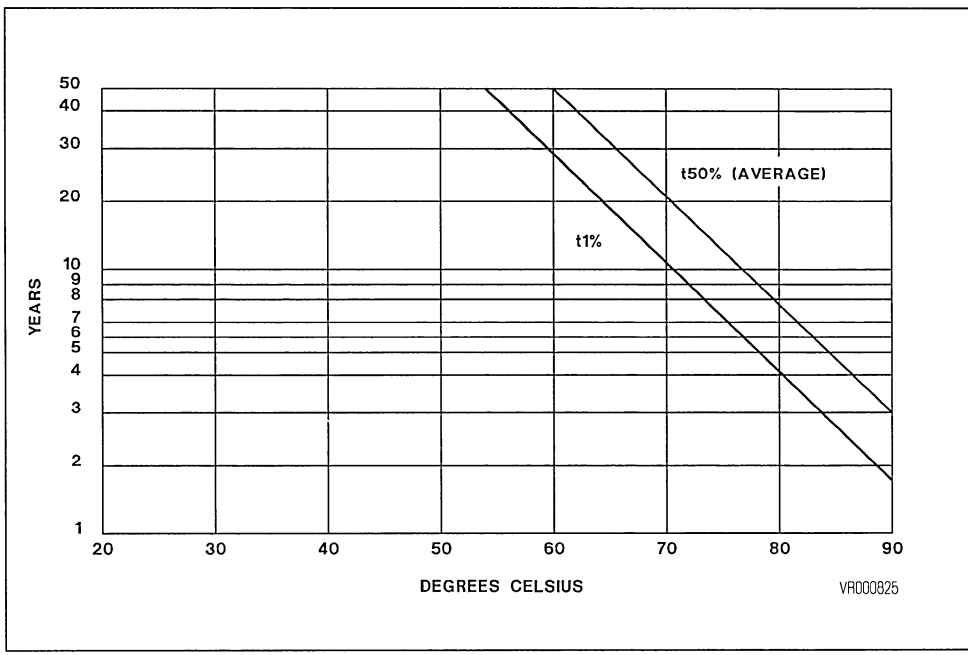
Reading Predicted $t_{1\%}$ values from Figure 8; SL_1 = 41 yrs., SL_2 = 11.4 yrs.,

Total Time (TT) = 8760 hrs./yr. TA_1 = 8322 hrs./yr. TA_2 = 438 hrs./yr. .

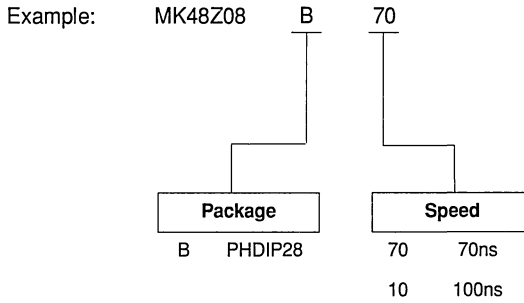
$$\text{Predicted Typical Storage Life} \geq 1 / \{ [(8322 / 8760) / 41] + [(438 / 8760) / 11.4] \}$$

$$\text{Predicted Typical Storage Life} \geq 36 \text{ years}$$

Figure 8. Predicted Battery Storage Life Versus Temperature



ORDERING INFORMATION



For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

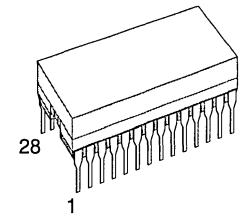
SGS-THOMSON MICROELECTRONICS

MKI48Z18

CMOS 8K x 8 ZEROPOWER SRAM

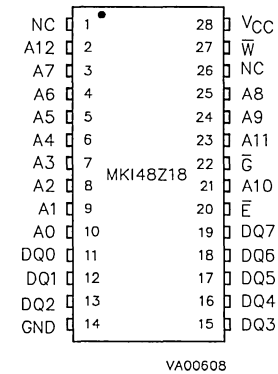
ADVANCE DATA

- INDUSTRIAL TEMPERATURE RANGE -40°C TO +85°C
- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND ENERGY SOURCE
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- PREDICTED WORST CASE BATTERY LIFE OF 6 YEARS @ 85°C
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT /WRITE PROTECTION.



PHDIP28 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connection



DESCRIPTION

The MKI48Z18 8K x 8 ZEROPOWER™ RAM is a nonvolatile 65,536 bit SRAM organized as 8192 words by 8 bits. The device combines an internal long life lithium battery and a full CMOS SRAM in a plastic 28 pin DIP. The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The MKI48Z18 has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which sustains data until valid power returns.

The MKI48Z18 is offered with an access time of 100ns. The device is operational over a temperature range of -40°C to +85°C. For a complete description of electrical characteristics and bus timing, refer to the MK48Z18B10 specifications contained within the MK48Z08,18 data sheet.

PIN NAMES

A0-A12	Address Inputs
$\overline{E}$	Chip Enable
GND	Ground
Vcc	5 Volts
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data In/Data Out

ABSOLUTE MAXIMUM RATINGS

Symbol	PARAMETER	VALUES	UNITS
P_D	Total Device Power Dissipation	1.0	W
I_{OUT}	Output Current Per Pin	20	mA
V_I	Voltage on any Pin Relative to Ground	–0.3 to + 7.0	V
T_{STG}	Ambient Storage (V_{cc} Off) Temperature	–40 to +85	°C
T_A	Ambient Operating Temperature	–40 to +85	°C

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS (–40°C≤ T_A ≤+85°C)

Symbol	Parameter	Min.	Max.	Unit	Notes
Vcc	Supply Voltage	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

(-40°C≤ T_A ≤+85°C; Vcc min ≤ Vcc ≤ Vcc max)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{cc1}	Average Vcc Power Supply Current		80	mA	3
I_{cc2}	TTL Standby Current ($\overline{E}$= V_{IH})		3	mA	
I_{cc3}	CMOS Standby Current ($\overline{E}$ = Vcc –0.2V)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	5
I_{OL}	Output Leakage Current	–5	5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)		0.4	V	

NOTES :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 ns once per Cycle.
3. I_{cc1} measured with outputs open.
4. 1mA typical.
5. Measured with Vcc ≥ V_I ≥ GND and outputs deselected.

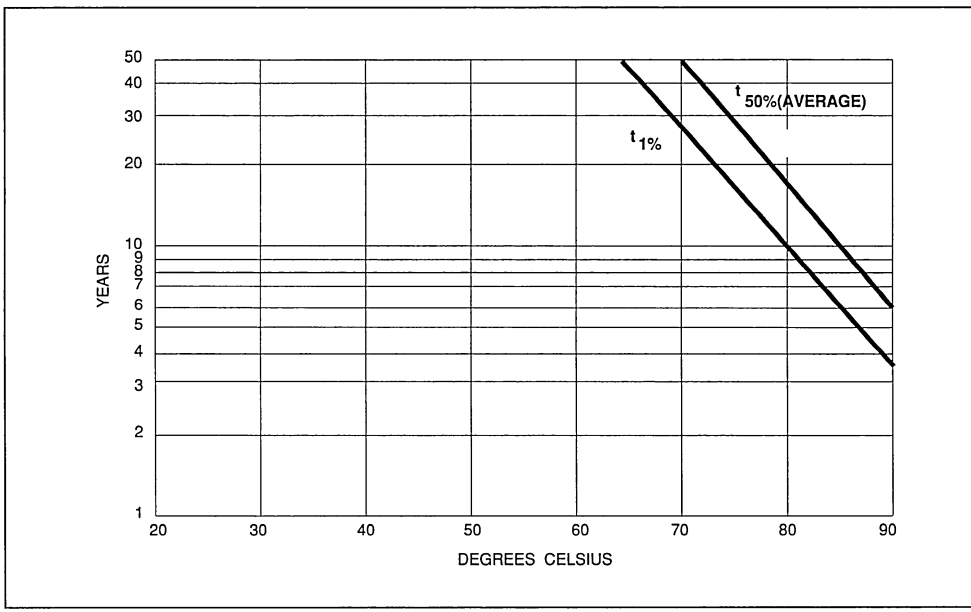
PREDICTING BATTERY LIFE

Figure 2 illustrates how temperature affects Battery Storage Life of the MKI48Z18. Since the leakage currents of the MKI48Z18 are so low, Storage Life of the battery is the limiting factor in defining the Battery Lifetime of the device. Thus, Battery Lifetime is controlled by temperature and is virtually unaffected by the current requirements of the MKI48Z18 RAM.

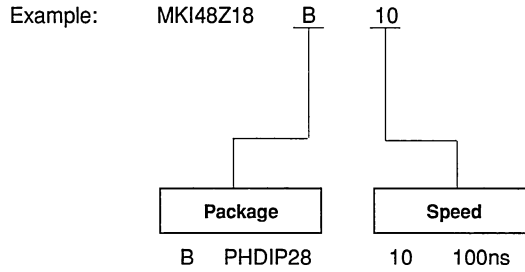
Storage Life predictions presented in Figure 2 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K load resistance.

Two end of life curves are presented in Figure 2. They are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 85°C is at issue, Figure 2 indicates that a particular MKI48Z18 has a 1% chance of having a battery failure 6.5 years into its life and a 50% chance of failure at the 10 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 6.5 years; 50% of them can be expected to experience a failure within 10 years.

Figure 2. Predicted Battery Storage Life Versus Temperature



ORDERING INFORMATION

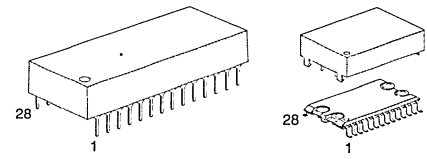


For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

CMOS 8K x 8 ZEROPOWER SRAM

- PIN and FUNCTION COMPATIBLE with the MK48Z08,18
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY
- SNAPHAT HOUSING (BATTERY) REPLACEABLE
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

DESCRIPTION

The M48Z08,18 ZEROPOWER® RAM is an 8K x 8 non-volatile static RAM which is pin and functional compatible with the MK48Z08,18. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

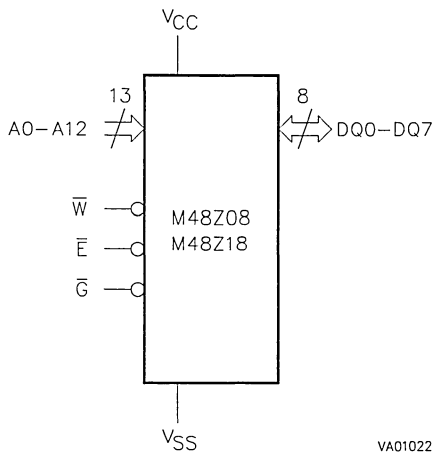
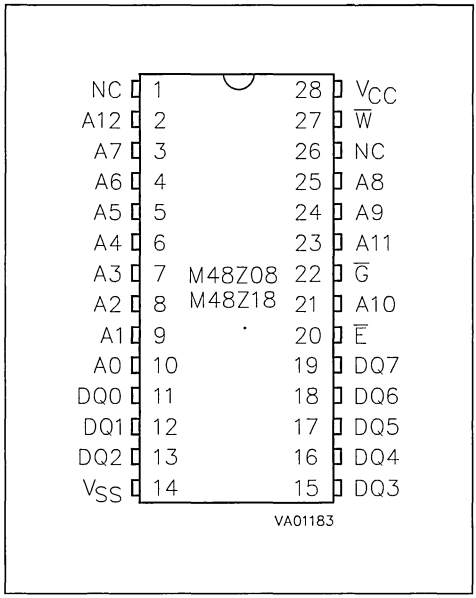
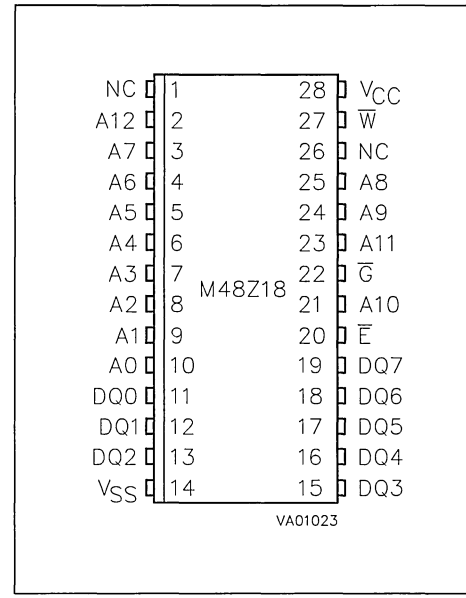


Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

DESCRIPTION (cont'd)

The 28 pin 600mil DIP CAPHAT™ houses the M48Z08,18 silicon with a long life lithium button cell in a single package.

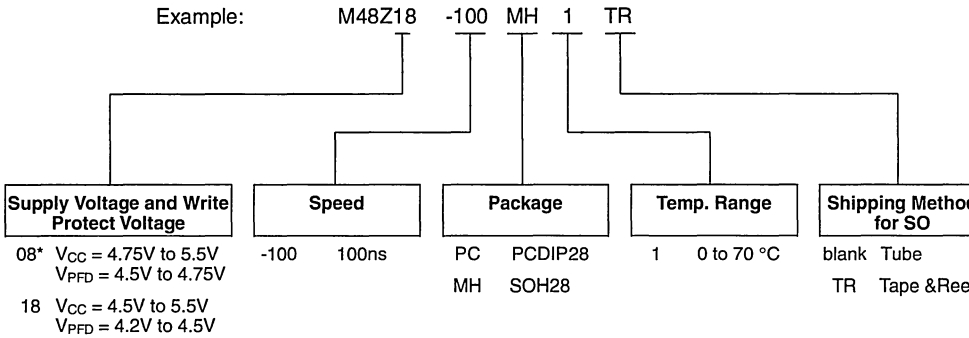
The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery package are shipped separately in plastic anti-static tubes. The SO is also available to ship in Tape & Reel form. For the M48Z18, the battery package part number is "M4Z28-BR00SH1".

The ordering information scheme shows the part number for the CAPHAT DIP and the SNAPHAT SOIC. For a complete description of electrical characteristics and bus timing, refer to the MK48Z08,18 data sheet.

ORDERING INFORMATION SCHEME



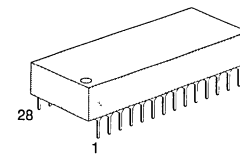
Note: 08* CAPHAT package only.

For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 8K x 8 ZEROPOWER SRAM

- PIN and FUNCTION COMPATIBLE with the MK48Z09,19
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- 11 YEARS of DATA RETENTION in the ABSENCE of POWER
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z09: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z19: 4.2V ≤ V_{PFD} ≤ 4.5V



PCDIP28 (PC)
Battery CAPHAT

DESCRIPTION

The M48Z09,19 ZEROPOWER® RAM is an 8K x 8 non-volatile static RAM which is pin and function compatible with the MK48Z09,19.

A special 28 pin 600mil DIP CAPHAT™ package houses the M48Z09,19 silicon with a long life lithium button cell to form a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{INT}$	Power Fail Interrupt
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

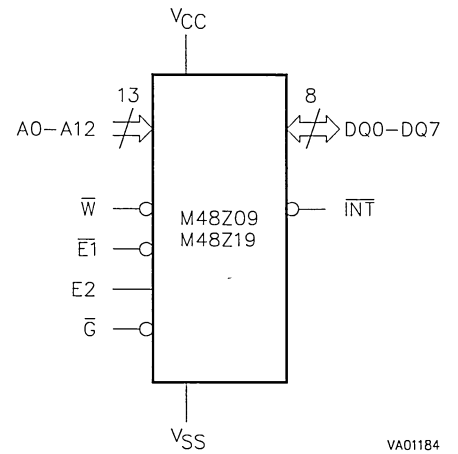
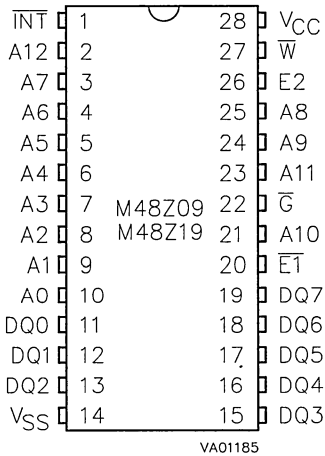


Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

The M48Z09,19 button cell has sufficient capacity and storage life to maintain data for an accumulated time period of at least 11 years in the absence of power over the operating temperature range.

For a complete description of electrical characteristics and bus timing, refer to the MK48Z09,19 data sheet.

ORDERING INFORMATION SCHEME

Example: M48Z09 -100 PC 1

Supply Voltage and Write Protect Voltage

09 V_{CC} = 4.75V to 5.5V
V_{PFD} = 4.5V to 4.75V

19 V_{CC} = 4.5V to 5.5V
V_{PFD} = 4.2V to 4.5V

Speed

-100 100ns

Package

PC PCDIP28

Temp. Range

1 0 to 70 °C

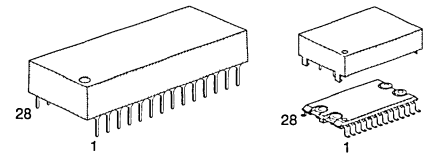
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 8K x 8 ZEROPOWER SRAM

PRODUCT CONCEPT

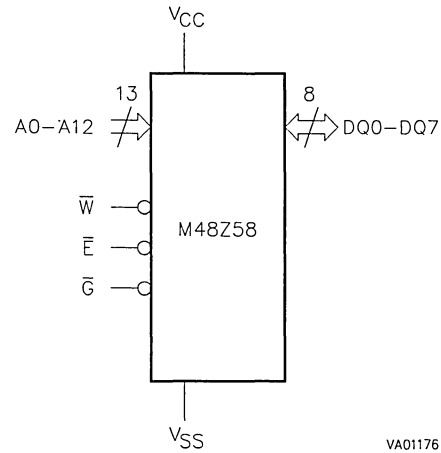
- INTEGRATED LOW POWER SRAM and POWER-FAIL CONTROL CIRCUIT
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 8K x 8 SRAMs
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY
- SNAPHAT HOUSING (BATTERY) REPLACEABLE
- LONG DATA RETENTION TIME in the ABSENCE of POWER
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

Figure 1. Logic Diagram



DESCRIPTION

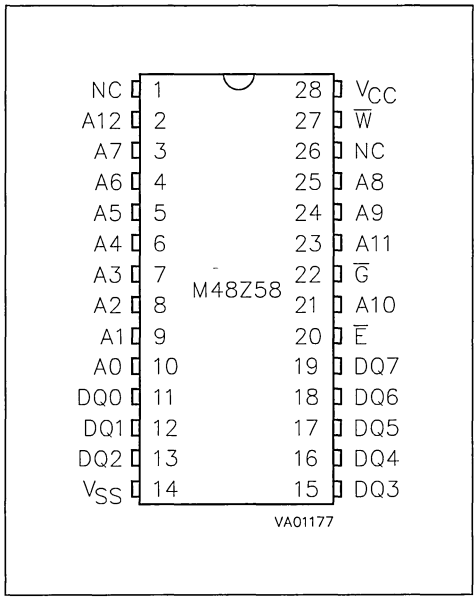
The M48Z58 ZEROPOWER® RAM is an 8K x 8 non volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

The 28 pin 600mil DIP CAPHAT™ houses the M48Z58 silicon with a long life lithium button cell in a single package.

Table 1. Signal Names

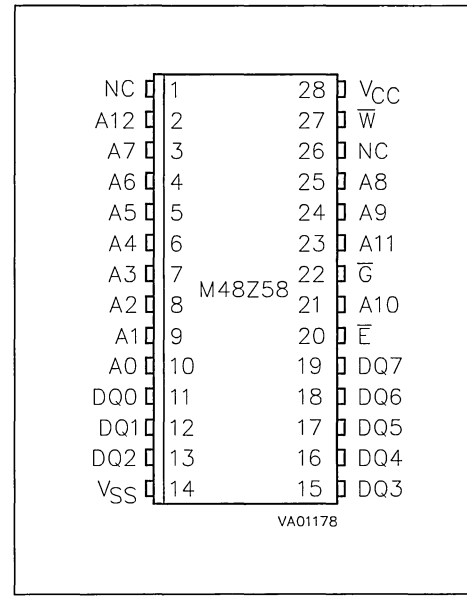
A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

DESCRIPTION (cont'd)

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SO after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

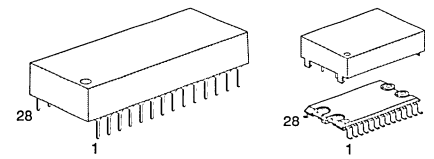
The M48Z58 is a pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the non volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z58 also has its own power-fail detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

CMOS 8K x 8 ZEROPOWER SRAM

PRODUCT CONCEPT

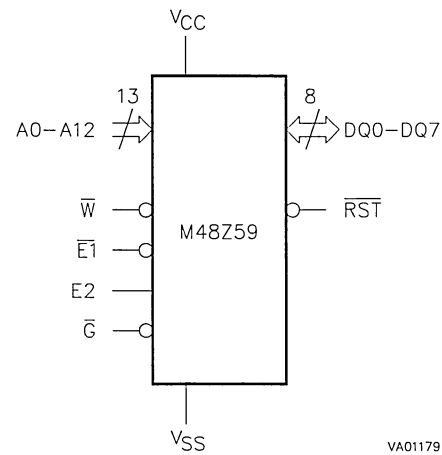
- INTEGRATED LOW POWER SRAM and POWER-FAIL CONTROL CIRCUIT
- FUNCTION COMPATIBLE with JEDEC STANDARD 8K x 8 SRAMs
- MICROPROCESSOR POWER-ON RESET (VALID all the WAY to $V_{CC} = V_{SS}$)
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY
- SNAPHAT HOUSING (BATTERY) REPLACEABLE
- LONG DATA RETENTION TIME in the ABSENCE of POWER
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

Figure 1. Logic Diagram



DESCRIPTION

The M48Z59 ZEROPOWER® RAM is an 8K x 8 non volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{RST}$	Reset
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

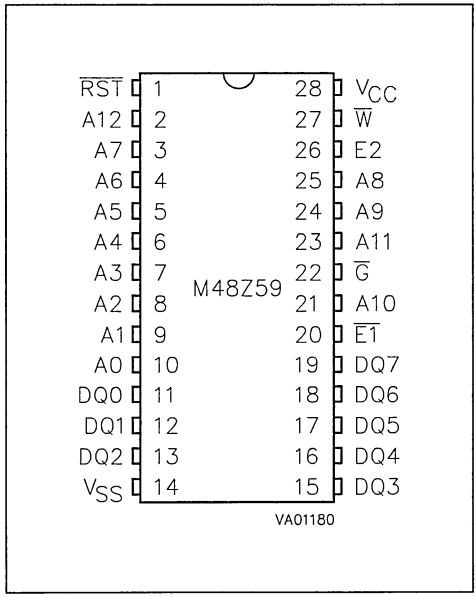
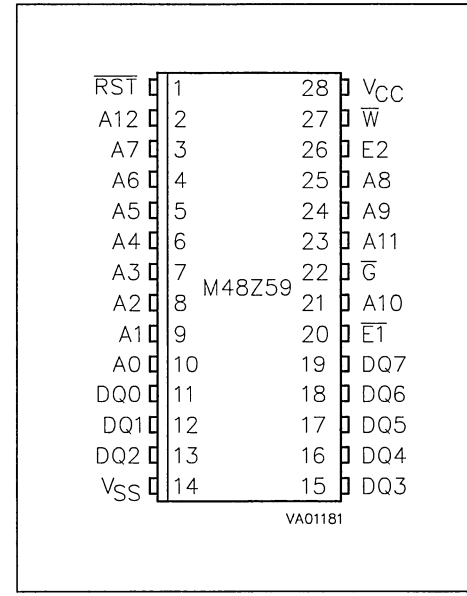


Figure 2B. SO Pin Connections



DESCRIPTION (cont'd)

The 28 pin 600mil DIP CAPHAT™ houses the M48Z59 silicon with a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SO after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The M48Z59 is functional equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the non volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

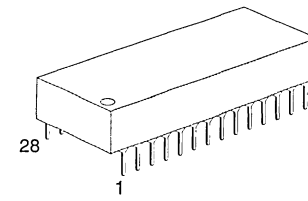
A power-on reset output provides a reset pulse to the microprocessor. The reset pulls low (open drain) on power-down and remains low on power-up for 40ms to 200ms after V_{CC} passes V_{PFD}.

The M48Z59 also has its own power-fail detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}.

As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

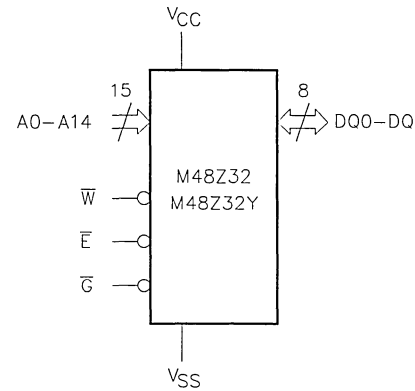
CMOS 32K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER at 70 °C
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 32K x 8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z32: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z32Y: 4.2V ≤ V_{PFD} ≤ 4.5V



PCDIP28 (PC)
Battery CAPHAT

Figure 1. Logic Diagram



DESCRIPTION

The M48Z32/32Y, 32K x 8 ZEROPOWER® RAM is a non-volatile 262,144 bit Static RAM organized as 32,768 words by 8 bits. A special 28 pin 600mil dual-in-line plastic package houses the M48Z32/32Y silicon with a long life button cell

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 70	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	50	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

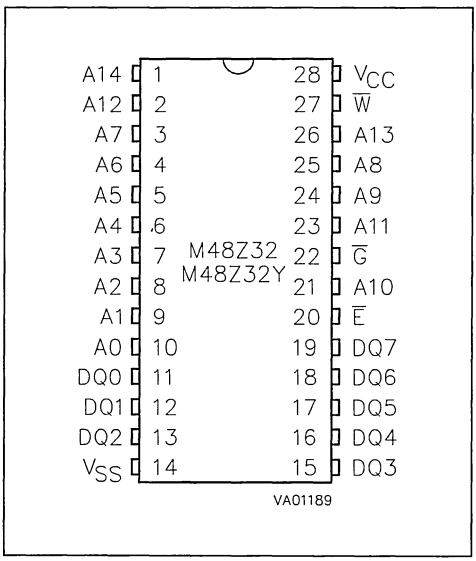
CAUTION: *Negative undershoots below –0 3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

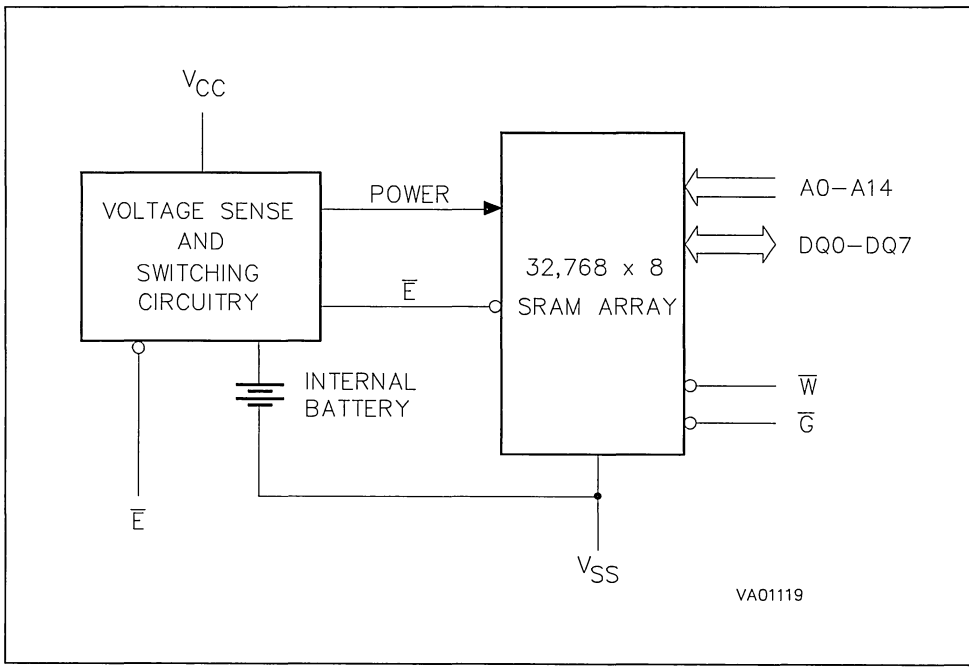
battery to form a highly integrated battery backed-up memory solution. The M48Z32/32Y is a non-volatile pin and function equivalent to any JEDEC standard 32K x 8 SRAM. It also easily fits into many ROM, EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z32/32Y also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

READ MODE

The M48Z32/32Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low.

Figure 3. Block Diagram



READ MODE (cont'd)

The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ or $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

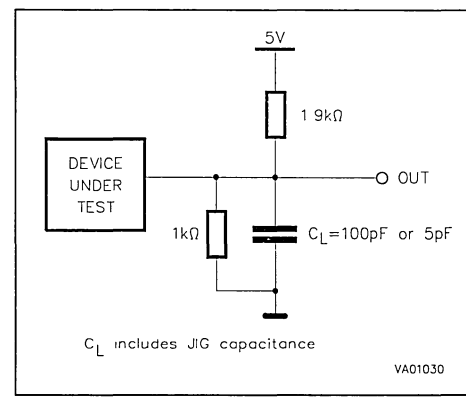


Table 4. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [2]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO} [1]	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±2	µA
I_{CC}	Supply Current	Outputs open		75	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} \ge V_{CC} - 0.3V$		3	mA
V_{IL} [2]	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs deselected.
2. Negative spikes of –1V allowed for up to 10ns once per Cycle

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z32)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z32Y)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		2.5		V
t_{DR}	Data Retention Time	10			YEARS

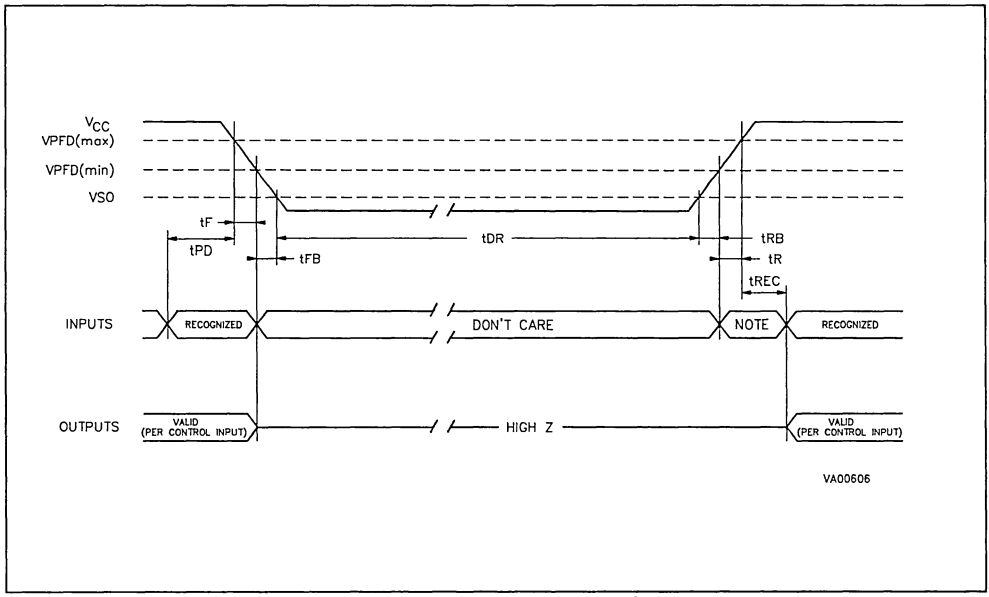
Note: 1. All voltages referenced to V_{SS}.

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		ns
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	5		ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms



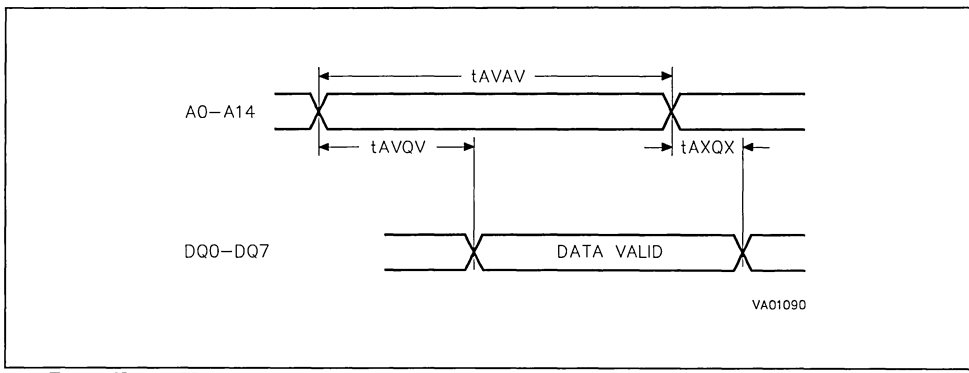
Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z32 / 32Y				Unit
		-85		-100		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	85		100		ns
t_{AVQV} (1)	Address Valid to Output Valid		85		100	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		85		100	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		45		50	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		30		35	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		30		35	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		10		ns

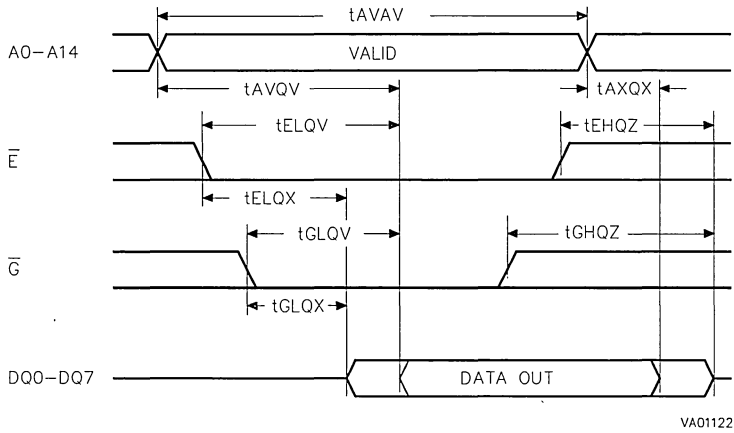
Note: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4).

Figure 6. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = Low.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



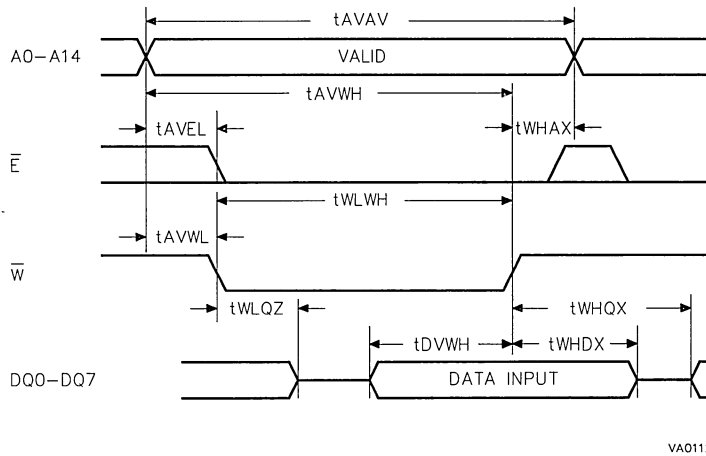
Note: $\overline{W}$ = High.

Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z32 / 32Y				Unit
		-85		-100		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	85		100		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	65		75		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	70		80		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		ns
t_{DVWH}	Input Valid to Write Enable High	35		40		ns
t_{DVEH}	Input Valid to Chip Enable High	35		40		ns
t_{WHDX}	Write Enable High to Input Transition	5		5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		5		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z		30		35	ns
t_{AVWH}	Address Valid to Write Enable High	70		80		ns
t_{AVEH}	Address Valid to Chip Enable High	70		80		ns
t_{WHQX} (1)	Write Enable High to Output Transition	5		5		ns

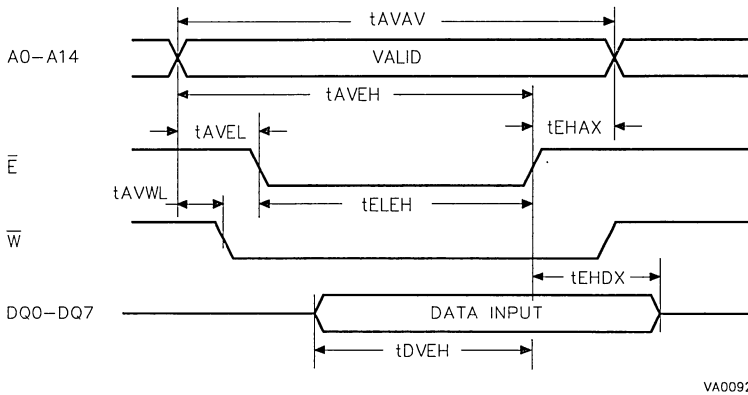
Note: 1. C_L = 5pF (see Figure 4).

Figure 8. Write Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High.

Figure 9. Chip Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High.

WRITE MODE

The M48Z32/32Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z32/32Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

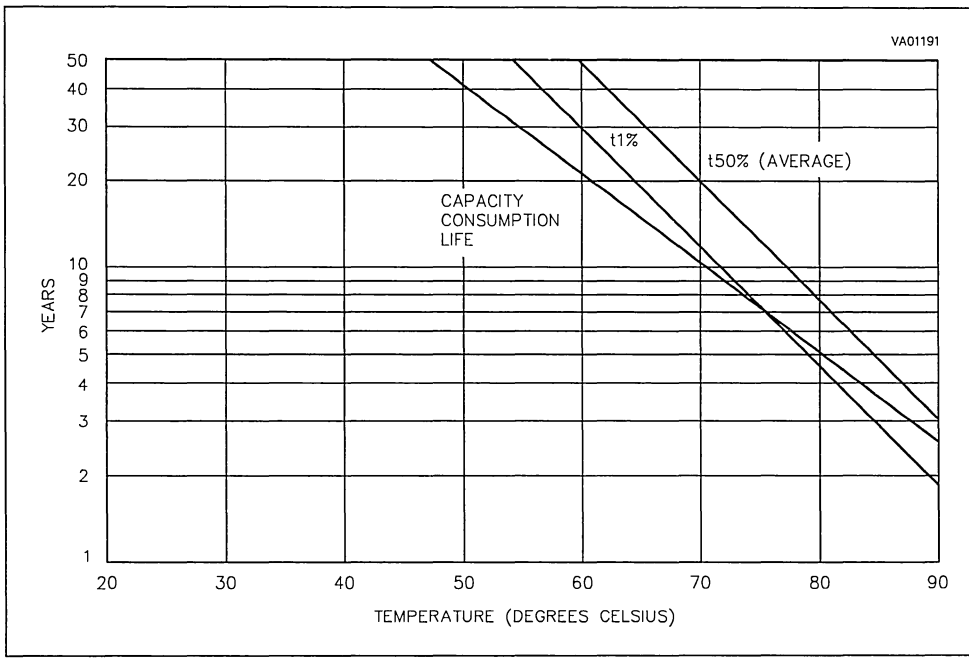
Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z32/32Y may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data. The internal button cell will maintain data in the M48Z32/32Y for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD}(min). $\overline{E}$ should be kept high as V_{CC} rises past V_{PFD}(min) to prevent inadvertent write cycles prior to processor stabilization. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

SYSTEM BATTERY LIFE

The useful life of the battery in the M48Z32/32Y is expected to ultimately come to an end for one of

Figure 10. Predicted Battery Storage and Capacity Life versus Temperature



SYSTEM BATTERY LIFE (cont'd)

two reasons: either because it has been discharged while providing current to the RAM in the battery back-up mode, or because the effects of aging render the cell useless before it can actually be completely discharged. The two effects are virtually unrelated allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms. The earlier occurring failure mechanism defines the battery system life of the M48Z32/32Y.

Cell Storage Life

Storage life is primarily a function of temperature. Figure 10 illustrates the approximate storage life of the M48Z32/32Y battery over temperature. The results in Figure 10 are derived from temperature accelerated life test studies performed at SGS-THOMSON. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4V closed circuit voltage across a 250 kΩ load resistor. The two lines, $t_{1\%}$ and $t_{50\%}$, represent different failure rate distributions for the cell's storage life. At 70°C, for example, the $t_{1\%}$ line indicates that an M48Z32/32Y has a 1% chance of having a battery failure 11 years into its life while the $t_{50\%}$ shows the part has a 50% chance of failure at the 20 year mark. The $t_{1\%}$ line represents the practical onset of wear out and can be considered the worst case Storage Life for the cell. The $t_{50\%}$ can be considered the normal or average life.

Cell Capacity Life

Figure 10 also shows how Capacity Consumption varies with temperature.

The M48Z32/32Y internal cell has a rated capacity of 39mAh. The device places a nominal RAM load of less than 445nA at 70°C. At this rate, the capacity consumption life is 39E-3/445E-9 = 87640 hours or about 10 years.

Calculating Capacity Life

As long as ambient temperature remains reasonably constant, capacity consumption life can be estimated directly from Figure 8. As V_{CC} duty cycle increases, though, so does capacity consumption life. At 70°C and 20% power on duty cycle, the capacity consumption life is: 10/(1-0.20) = 12.5 years.

Estimated System Life

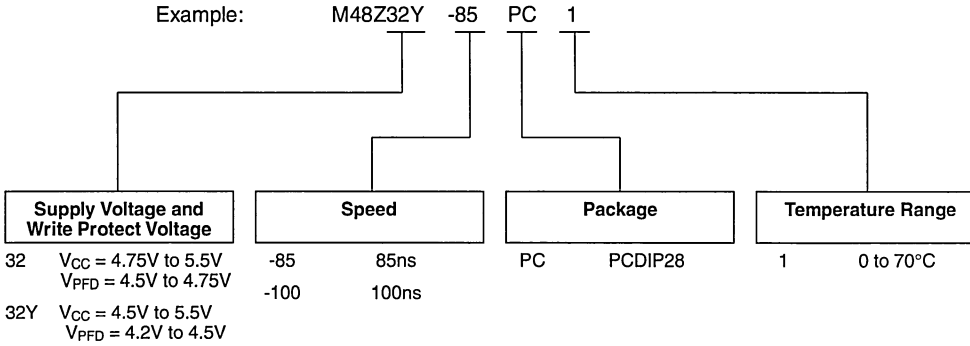
Since either storage life or capacity consumption can end the battery's life, the system life is marked by which ever occurs first. At 70°C and a 0% power on duty cycle (always in the battery back-up mode), the system life would be 10 years as limited by capacity consumption.

Reference for System Life

Each M48Z32/32Y is marked with a nine digit manufacturing date code in the form of H99XXYYZZ. For example, H995B9231 is:

- H = fabricated in Carrollton, TX
- 9 = assembled in Muar, Malaysia,
- 9 = tested in Muar, Malaysia,
- 5B = lot designator,
- 9231 = assembled in the year 1992, work week 31.

ORDERING INFORMATION SCHEME



For a list of available options (Package and Speed) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

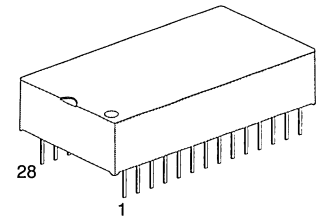
For further information or any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SGS-THOMSON MICROELECTRONICS

M48Z30
M48Z30Y

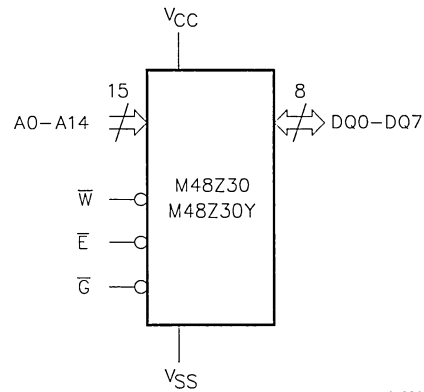
CMOS 32K x 8 ZEROPOWER SRAM

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 32K x 8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z30: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z30Y: 4.2V ≤ V_{PFD} ≤ 4.50V
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED



PMDIP28 (PM)
Module

Figure 1. Logic Diagram



DESCRIPTION

The M48Z30/30Y 32K x 8 ZEROPOWER® RAM is a non-volatile 262,144 bit Static RAM organized as 32,768 words by 8 bits. The device combines an internal lithium battery and a full CMOS SRAM in a plastic 28 pin DIP Module. The ZEROPOWER

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 70	°C
T_{BIAS}	Temperature Under Bias	–10 to 70	°C
T_{SLD}	Lead Soldering Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

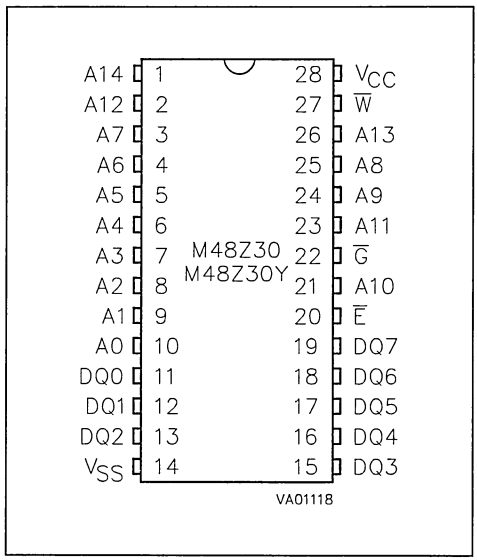
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

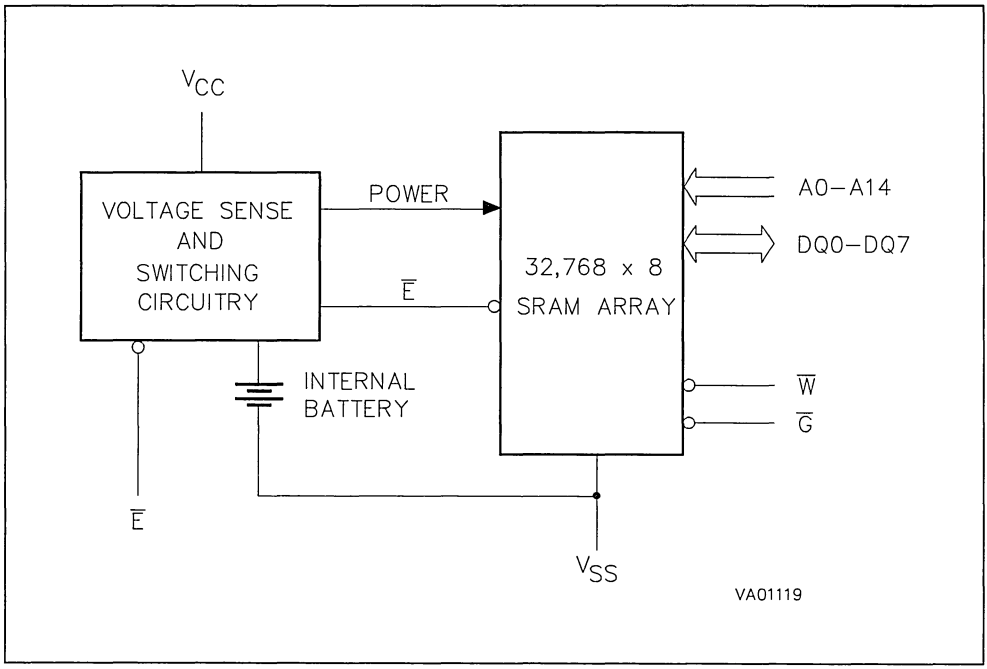
RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z30/30Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which sustains data until valid power returns.

READ MODE

The M48Z30/30Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address

Figure 3. Block Diagram



specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z30/30Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

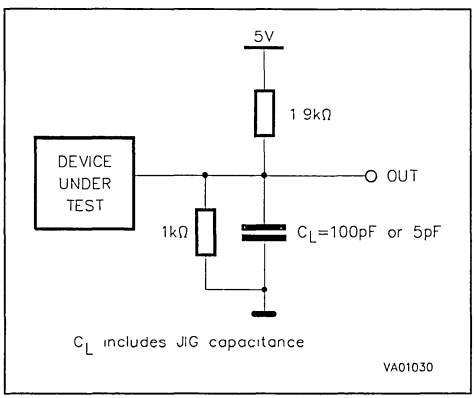


Table 4. Capacitance [1, 2] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3 Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} [1]	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±1	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, Outputs open		85	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		7	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ ≥ V_{CC} – 0.2V		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z30)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z30Y)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3		V
t_{DR} [2]	Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_{WP}	Write Protect Time from V_{CC} = V_{PFD}	40	150	µs
t_R	V_{SO} to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{ER}	$\overline{E}$ Recovery Time	40	120	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).

2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

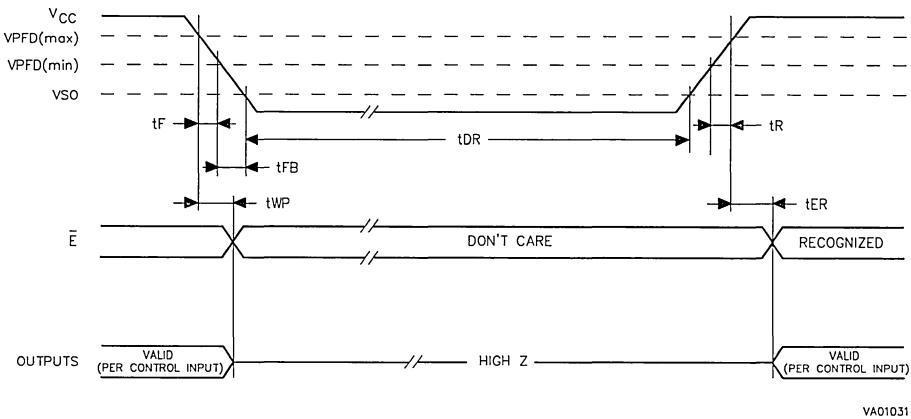
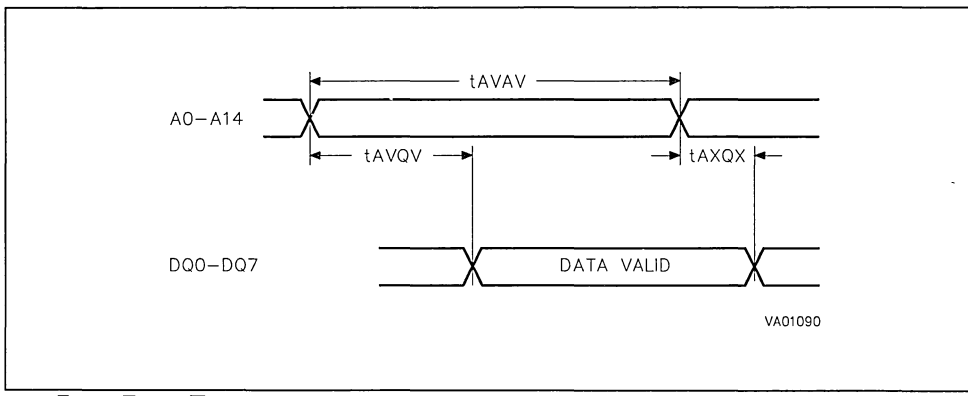


Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z30 / 30Y				Unit
		-85		-100		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	85		100		ns
t_{AVQV} (1)	Address Valid to Output Valid		85		100	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		85		100	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		45		50	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		40		40	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		35		35	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		10		ns

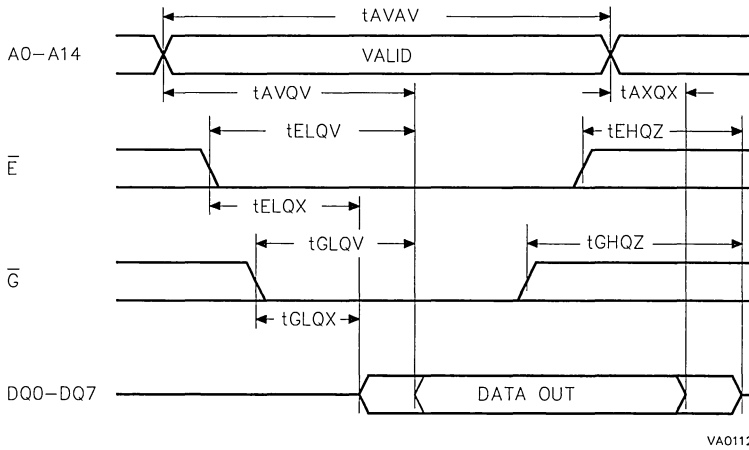
Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4)

Figure 6. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High.

WRITE MODE (cont'd)

A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z30/30Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

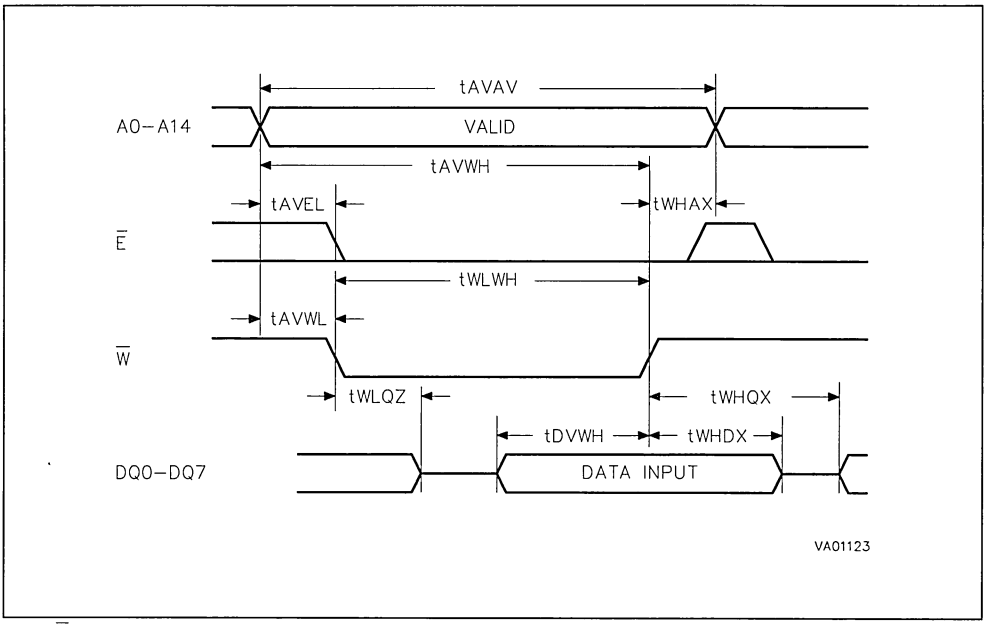
The internal coin cell will maintain data in the M48Z30/30Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the battery is disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z30 / 30Y				Unit
		-85		-100		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	85		100		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	65		75		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		90		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to Write Enable High	35		40		ns
t_{DVEH}	Input Valid to Chip Enable High	35		40		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	15		15		ns
t_{WLQZ} (1,2)	Write Enable Low to Output Hi-Z		35		35	ns
t_{AVWH}	Address Valid to Write Enable High	75		80		ns
t_{AVEH}	Address Valid to Chip Enable High	75		80		ns
t_{WHQX} (1,2)	Write Enable High to Output Transition	5		5		ns

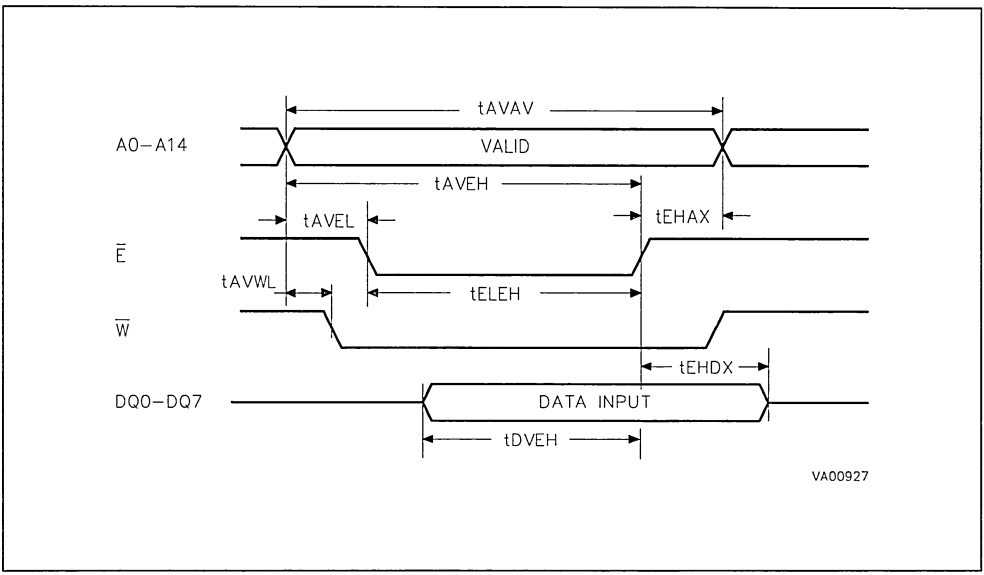
Notes: 1. C_L = 5pF (see Figure 4)
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low after $\overline{W}$ going low, the outputs remain in the high-impedance state

Figure 8. Write Enable Controlled, Write AC Waveforms



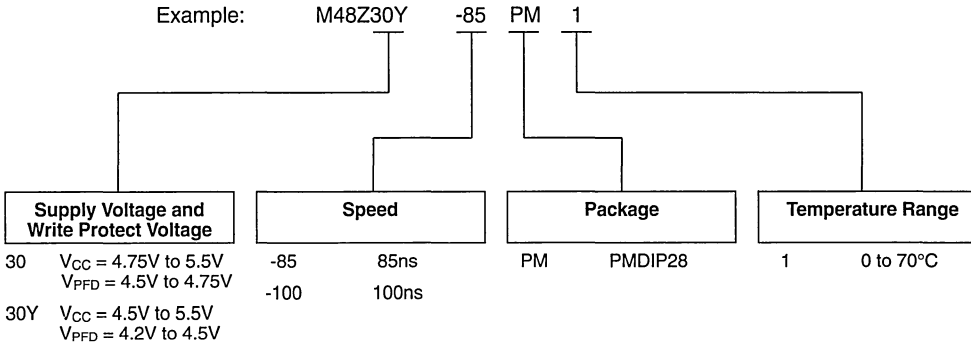
Note: $\overline{G}$ = High.

Figure 9. Chip Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High.

ORDERING INFORMATION SCHEME

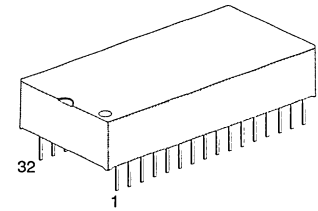


For a list of available options (Package and Speed) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information or any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

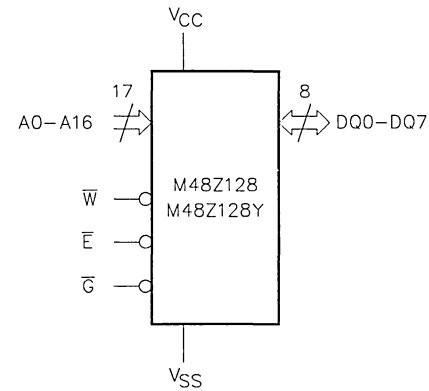
CMOS 128K x 8 ZEROPOWER SRAM

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 128K x 8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z128: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z128Y: 4.2V ≤ V_{PFD} ≤ 4.50V
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED



PMDIP32 (PM)
Module

Figure 1. Logic Diagram



DESCRIPTION

The M48Z128/128Y 128K x 8 ZEROPOWER® RAM is a non-volatile 1,048,576 bit Static RAM organized as 131,072 words by 8 bits. The device combines an internal lithium battery and a full CMOS SRAM in a plastic 32 pin DIP Module.

Table 1. Signal Names

A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 70	°C
T_{BIAS}	Temperature Under Bias	–10 to 70	°C
T_{SLD}	Lead Soldering Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

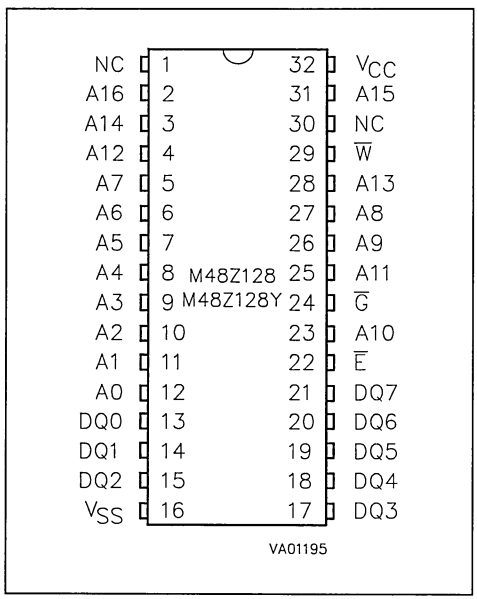
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

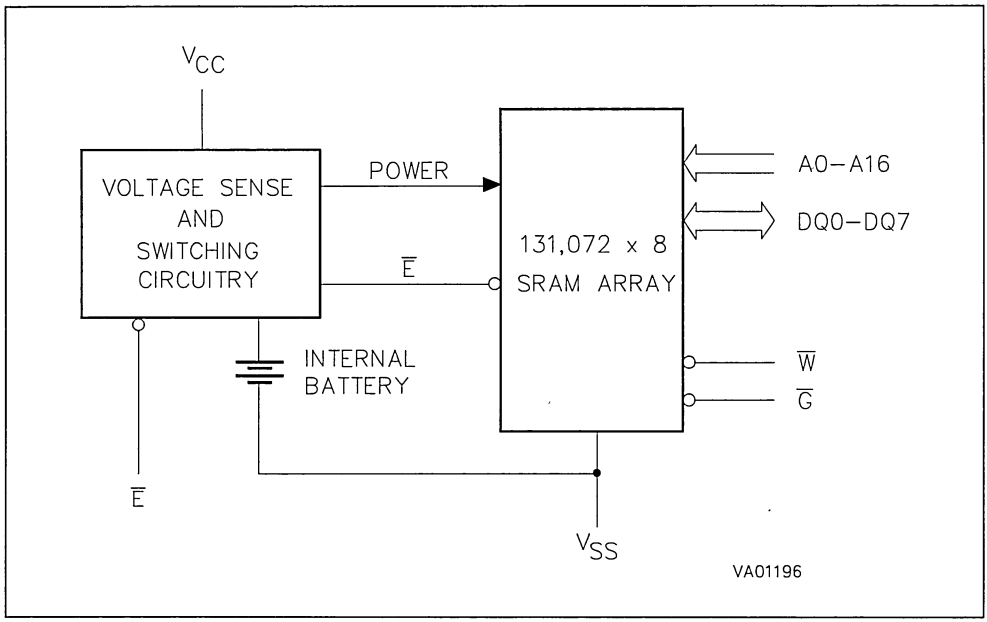
The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z128/128Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which sustains data until valid power returns.

READ MODE

The M48Z128/128Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 1,048,576 locations in the static storage array. Thus, the unique address specified by the 17 Address Inputs defines which

Figure 3. Block Diagram



one of the 131,072 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z128/128Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

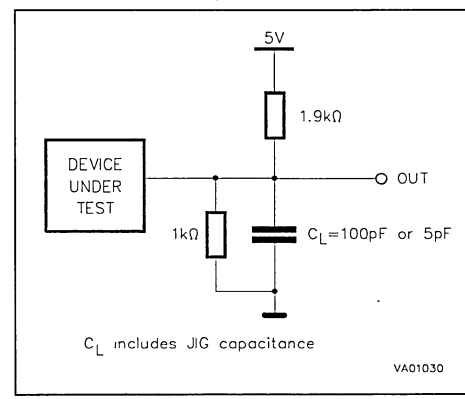


Table 4. Capacitance (1, 2) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (3)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±1	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, Outputs open		105	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		7	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ ≥ V_{CC} – 0.2V		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z128)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z128Y)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3		V
t_{DR} (2)	Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_{WP}	Write Protect Time from V_{CC} = V_{PFD}	40	150	µs
t_R	V_{SO} to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{ER}	$\overline{E}$ Recovery Time	40	120	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

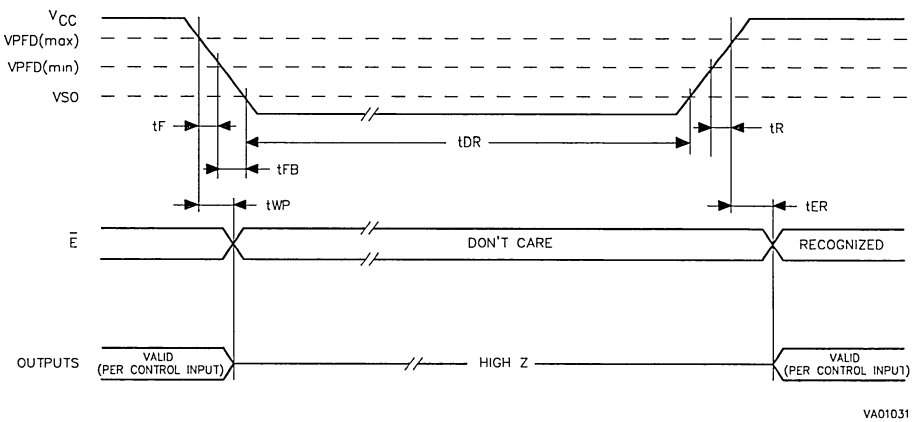
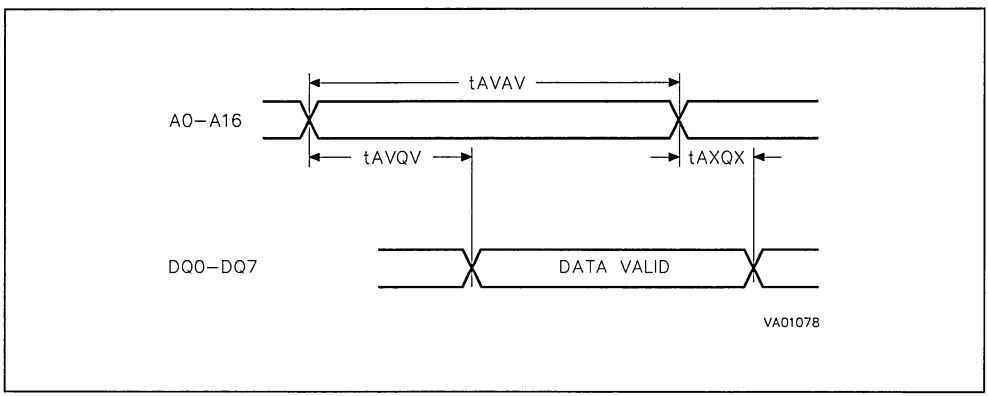


Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z128 / 128Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	85		120		ns
t_{AVQV} (1)	Address Valid to Output Valid		85		120	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		85		120	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		45		60	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		35		45	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25		35	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		10		ns

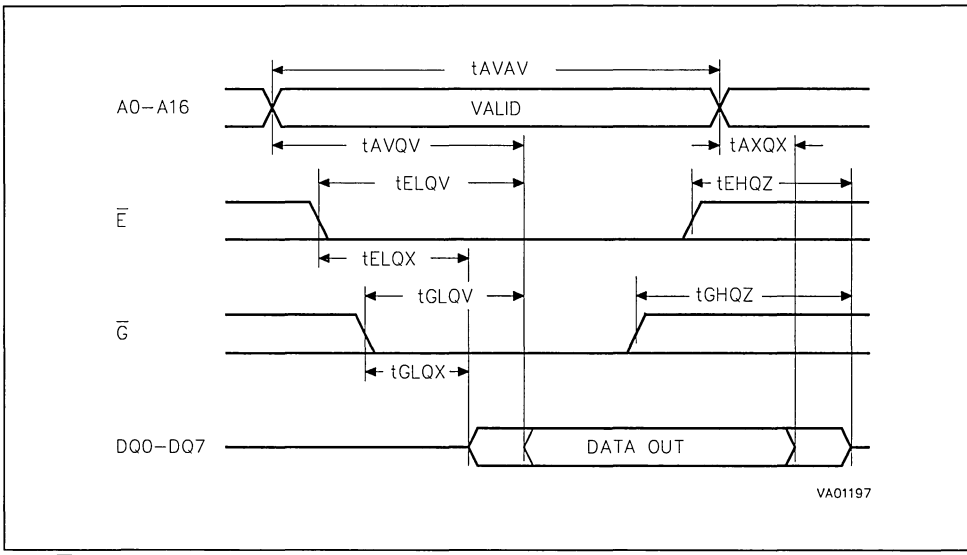
Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4)

Figure 6. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High.

WRITE MODE (cont'd)

The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z128/128Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

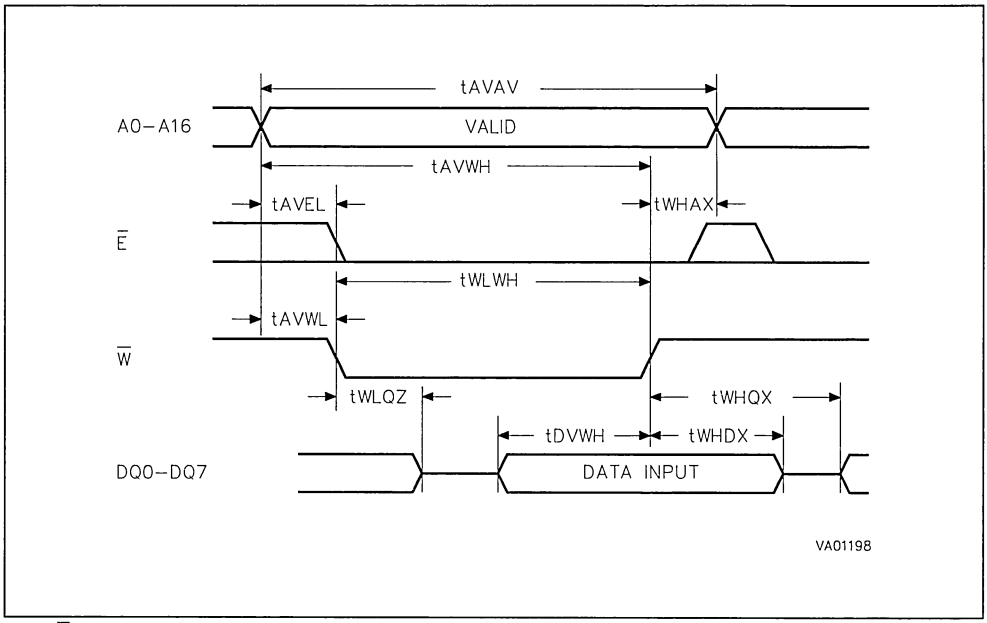
The internal coin cell will maintain data in the M48Z128/128Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the battery is disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z128 / 128Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	85		120		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	65		85		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		100		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to Write Enable High	35		45		ns
t_{DVEH}	Input Valid to Chip Enable High	35		45		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	10		10		ns
t_{WLQZ} (1,2)	Write Enable Low to Output Hi-Z		30		40	ns
t_{AVWH}	Address Valid to Write Enable High	75		100		ns
t_{AVEH}	Address Valid to Chip Enable High	75		100		ns
t_{WHQX} (1,2)	Write Enable High to Output Transition	0		0		ns

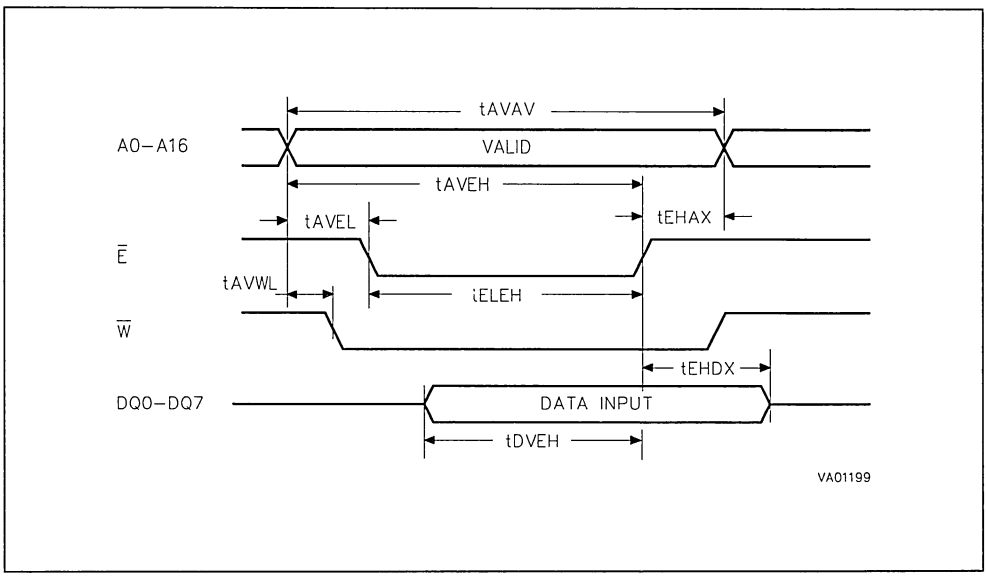
Notes: 1. C_L = 5pF (see Figure 4).
2. If E goes low simultaneously with $\overline{W}$ going low after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 8. Write Enable Controlled, Write AC Waveforms



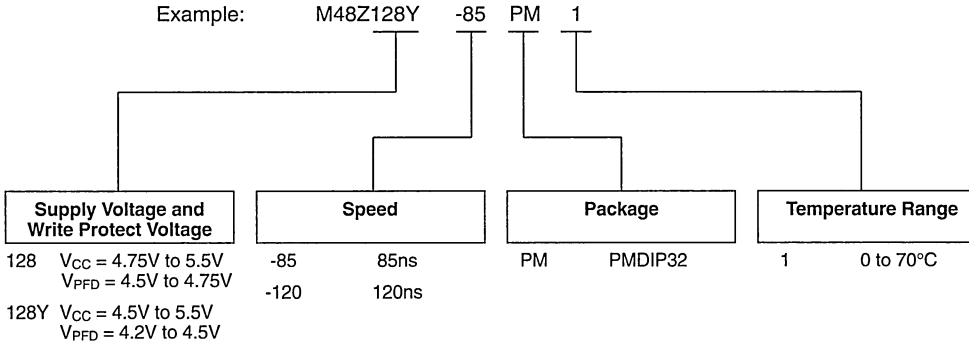
Note: $\overline{G}$ = High.

Figure 9. Chip Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High.

ORDERING INFORMATION SCHEME

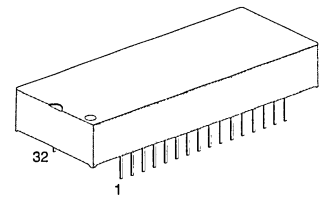


For a list of available options (Package and Speed) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information or any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 256K x 8 ZEROPOWER SRAM

- INTEGRATED LOW POWER SRAMs, POWER-FAIL CONTROL CIRCUIT and BATTERIES
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 256K x 8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z256: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z256Y: 4.2V ≤ V_{PFD} ≤ 4.50V
- BATTERIES INTERNALLY ISOLATED UNTIL POWER IS APPLIED



PMLDIP32 (PL)
Module

DESCRIPTION

The M48Z256/256Y 256K x 8 ZEROPOWER® RAM is a non-volatile 2,097,152 bit Static RAM organized as 262,144 words by 8 bits. The device combines two internal lithium batteries and full CMOS SRAMs in a plastic 32 pin DIP long Module.

Table 1. Signal Names

A0 - A17	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

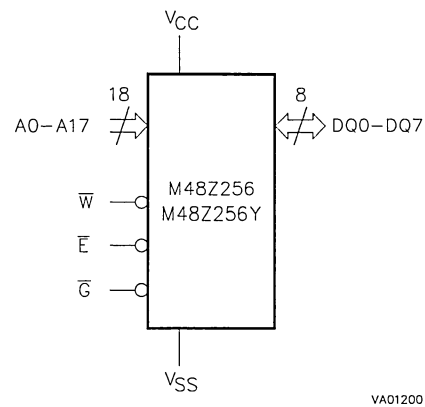


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 70	°C
T_{BIAS}	Temperature Under Bias	–10 to 70	°C
T_{SLD}	Lead Soldering Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

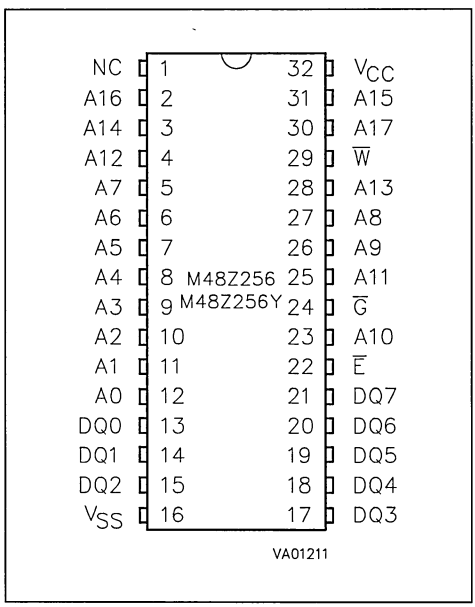
CAUTION: *Negative undershoots below –0 3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

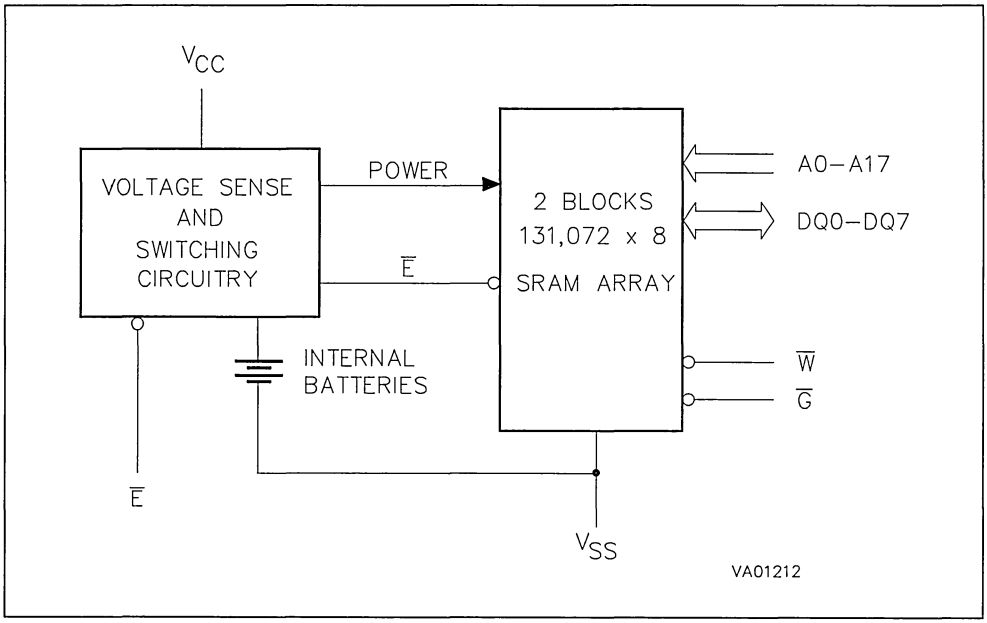
The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z256/256Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the batteries which sustain data until valid power returns.

READ MODE

The M48Z256/256Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 2,097,152 locations in the static storage array. Thus, the unique address specified by the 18 Address Inputs defines which

Figure 3. Block Diagram



one of the 262,144 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z256/256Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

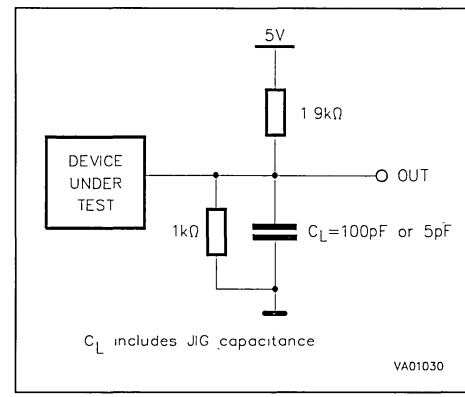


Table 4. Capacitance [1, 2] (T_A = 25 °C, f = 1 MHz.)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		20	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		20	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO} [1]	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±2	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, Outputs open		110	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		12	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} \ge V_{CC} - 0.2V$		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z256)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z256Y)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3		V
t_{DR} [2]	Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_{WP}	Write Protect Time from V_{CC} = V_{PFD}	40	150	µs
t_R	V_{SO} to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{ER}	$\overline{E}$ Recovery Time	40	120	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

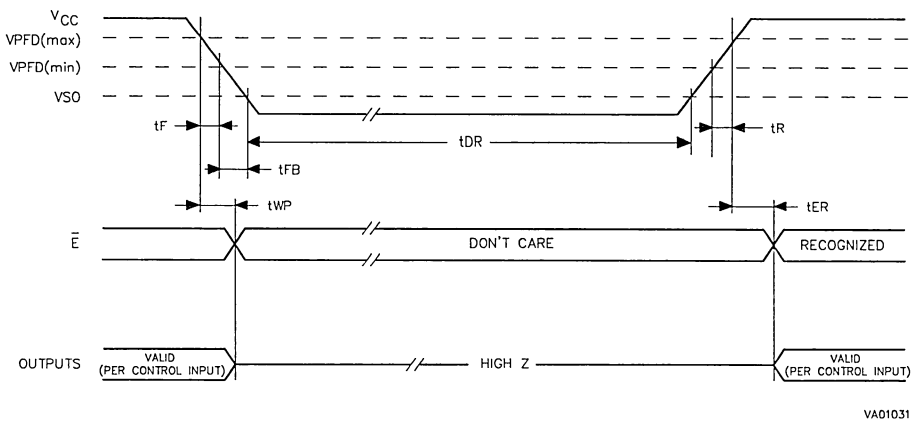
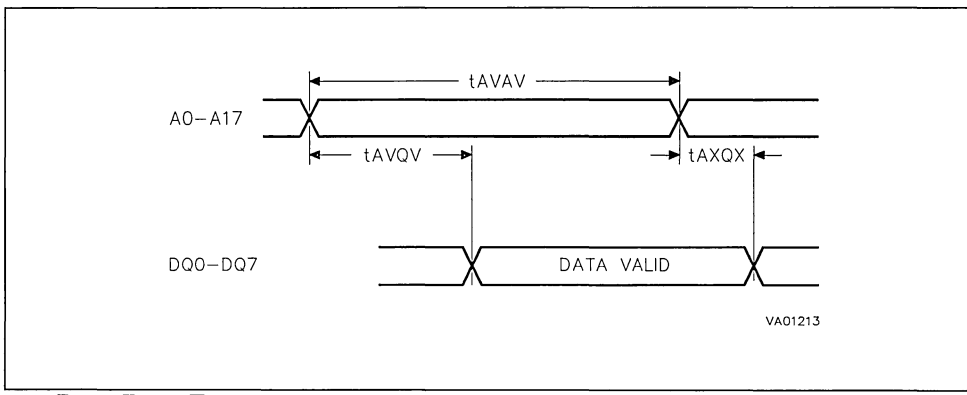


Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z256 / 256Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	85		120		ns
t_{AVQV} (1)	Address Valid to Output Valid		85		120	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		85		120	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		45		60	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		35		45	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25		35	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		10		ns

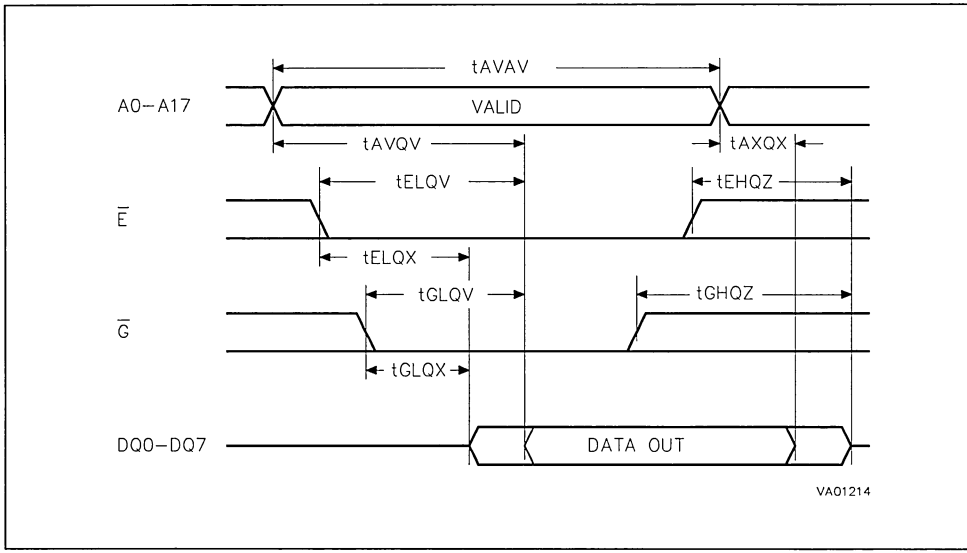
Notes: 1. C_L = 100pF (see Figure 4).
2 C_L = 5pF (see Figure 4)

Figure 6. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High.

WRITE MODE (cont'd)

The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z256/256Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

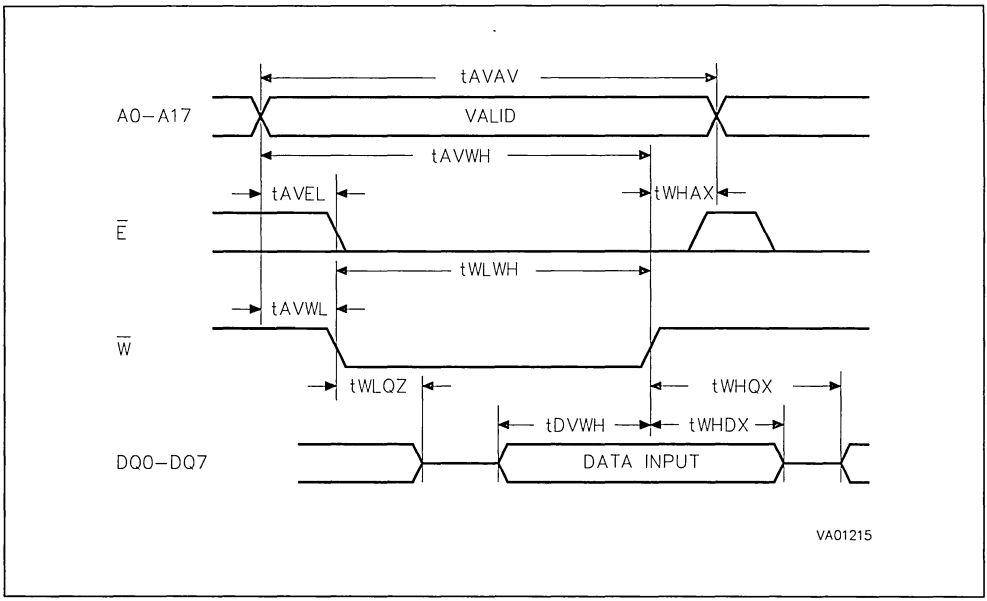
The internal coin cells will maintain data in the M48Z256/256Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the batteries are disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z256 / 256Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	85		120		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	65		85		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		100		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to Write Enable High	35		45		ns
t_{DVEH}	Input Valid to Chip Enable High	35		45		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	10		10		ns
t_{WLQZ} (1,2)	Write Enable Low to Output Hi-Z		30		40	ns
t_{AVWH}	Address Valid to Write Enable High	75		100		ns
t_{AVEH}	Address Valid to Chip Enable High	75		100		ns
t_{WHQX} (1,2)	Write Enable High to Output Transition	0		0		ns

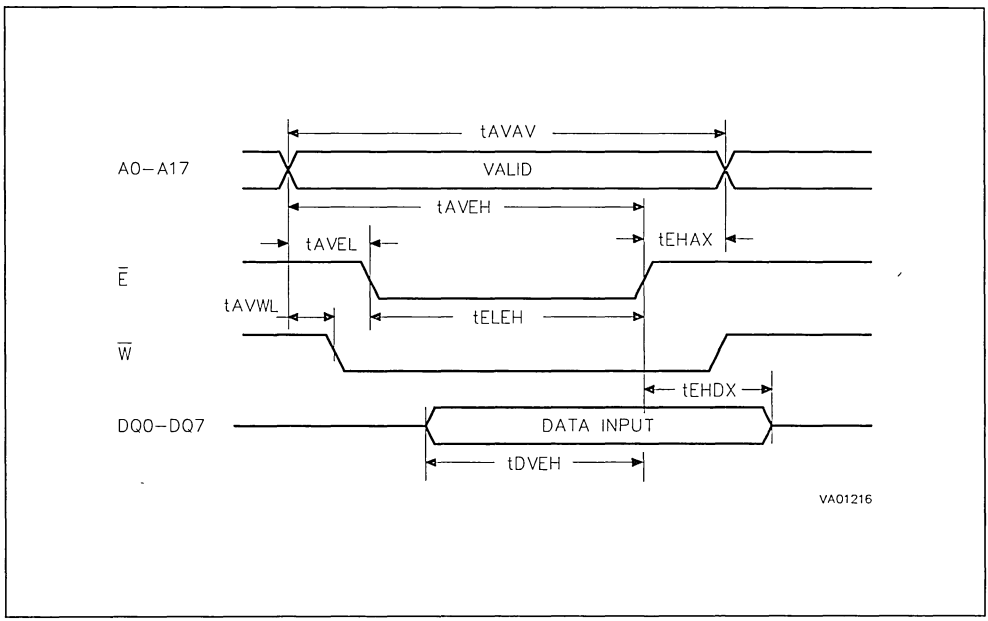
Notes: 1. C_L = 5pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 8. Write Enable Controlled, Write AC Waveforms



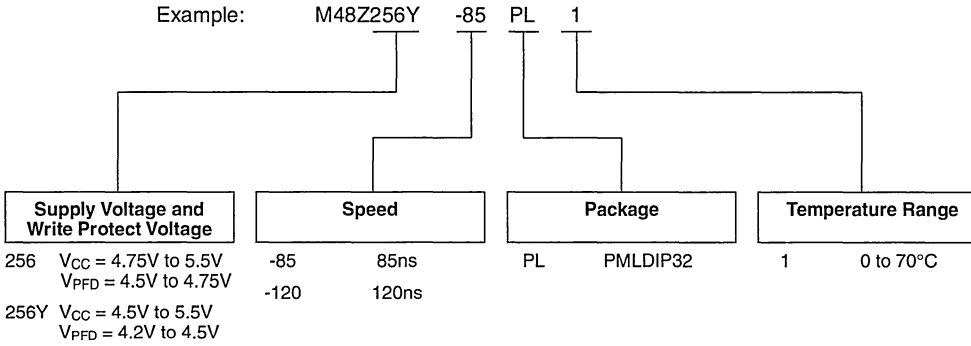
Note: $\overline{G}$ = High

Figure 9. Chip Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High

ORDERING INFORMATION SCHEME

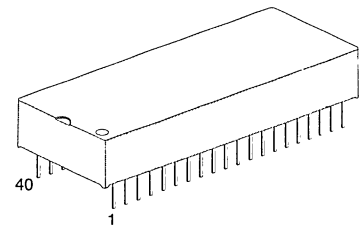


For a list of available options (Package and Speed) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information or any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 128K x 16 ZEROPOWER SRAM

- INTEGRATED LOW POWER SRAMs, POWER-FAIL CONTROL CIRCUIT and BATTERIES
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 128K x 16 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M46Z128: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M46Z128Y: 4.2V ≤ V_{PFD} ≤ 4.50V
- BATTERIES INTERNALLY ISOLATED UNTIL POWER IS APPLIED



PMDIP40 (PM)
Module

DESCRIPTION

The M46Z128/128Y 128K x 16 ZEROPOWER® RAM is a non-volatile 2,097,152 bit Static RAM organized as 131,072 words by 16 bits. The device combines two internal lithium batteries and full CMOS SRAMs in a plastic 40 pin DIP Module.

Table 1. Signal Names

A0 - A16	Address Inputs
DQ0 - DQ15	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

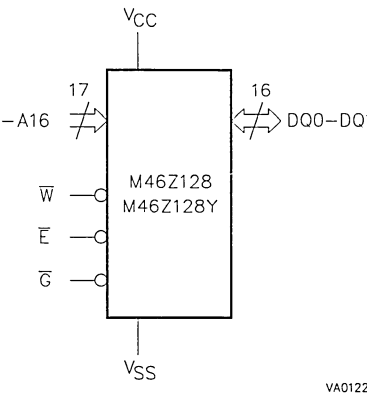


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 70	°C
T_{BIAS}	Temperature Under Bias	–10 to 70	°C
T_{SLD}	Lead Soldering Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

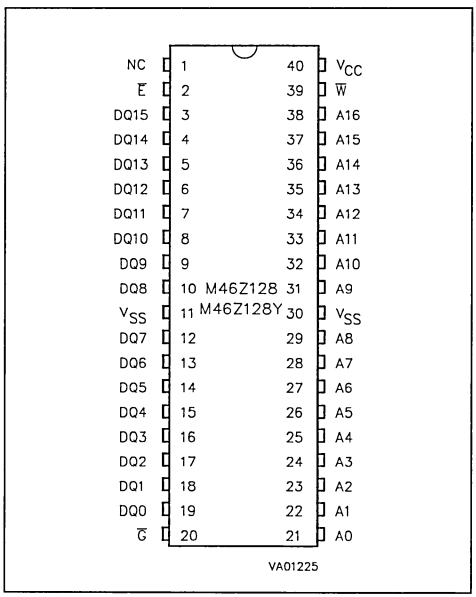
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ15	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

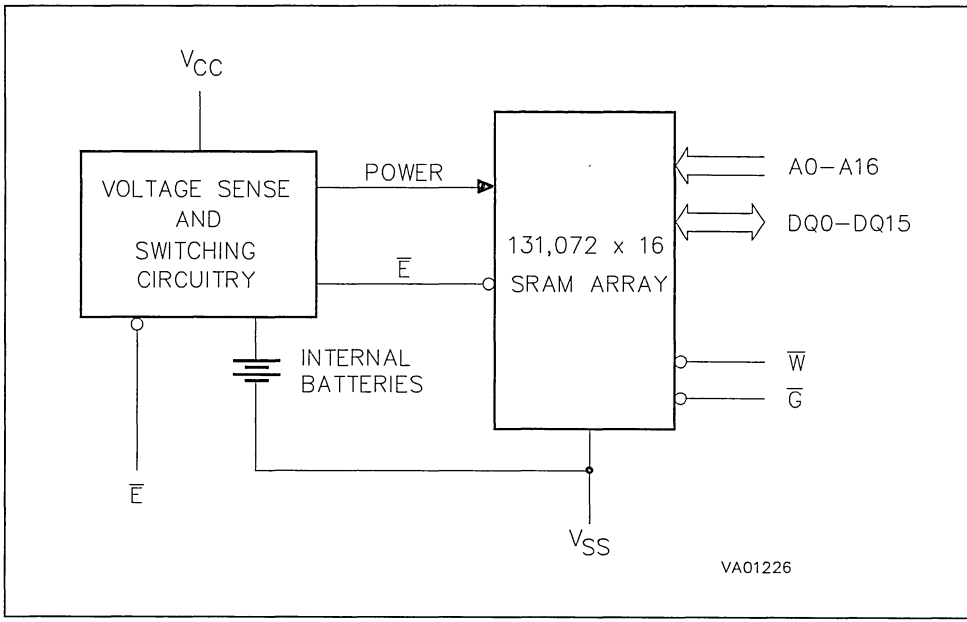
The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M46Z128/128Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the batteries which sustain data until valid power returns.

READ MODE

The M46Z128/128Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from sixteen of 2,097,152 locations in the static storage array. Thus, the unique address specified by the 17 Address Inputs defines which

Figure 3. Block Diagram



one of the 131,072 words of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the sixteen three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M46Z128/128Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

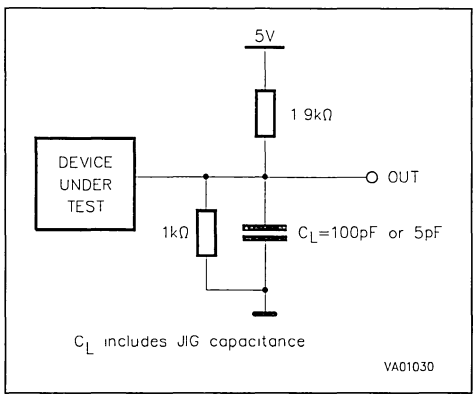


Table 4. Capacitance [1, 2] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		20	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±2	µA
I_{LO} [1]	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±1	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, Outputs open		200	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		11	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ ≥ V_{CC} – 0.2V		5	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M46Z128)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M46Z128Y)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3		V
t_{DR} [2]	Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_{WP}	Write Protect Time from V_{CC} = V_{PFD}	40	150	µs
t_R	V_{SO} to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{ER}	$\overline{E}$ Recovery Time	40	120	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).

2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

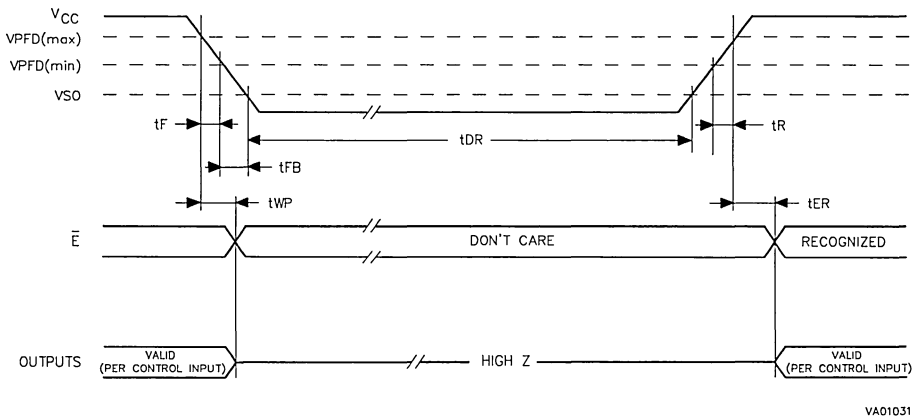
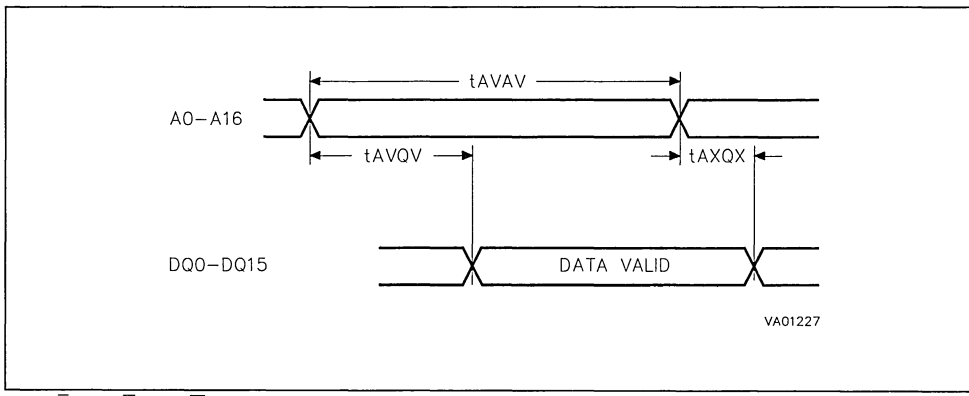


Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M46Z128 / 128Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	85		120		ns
t_{AVQV} (1)	Address Valid to Output Valid		85		120	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		85		120	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		45		60	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		35		45	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25		35	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		10		ns

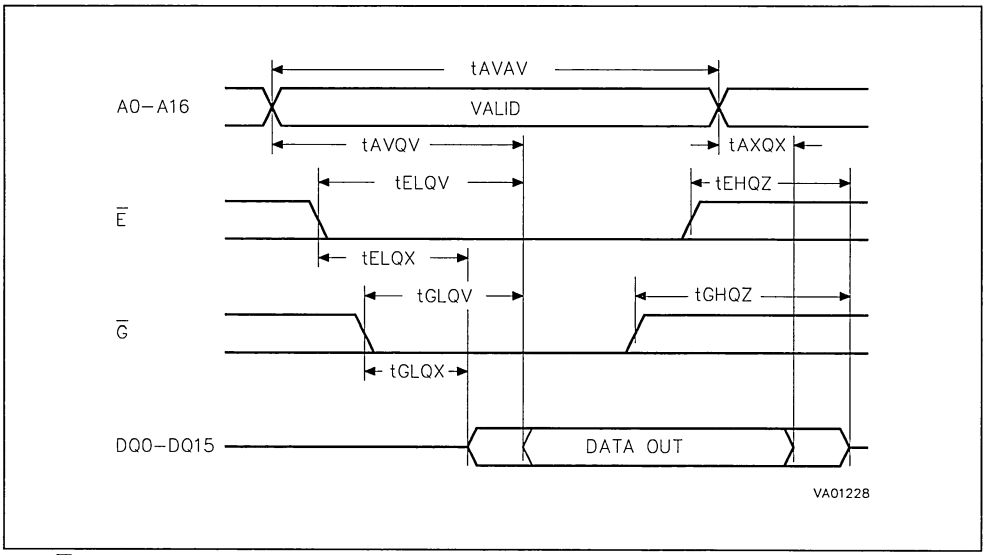
Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4)

Figure 6. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High.

WRITE MODE (cont'd)

The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M46Z128/128Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

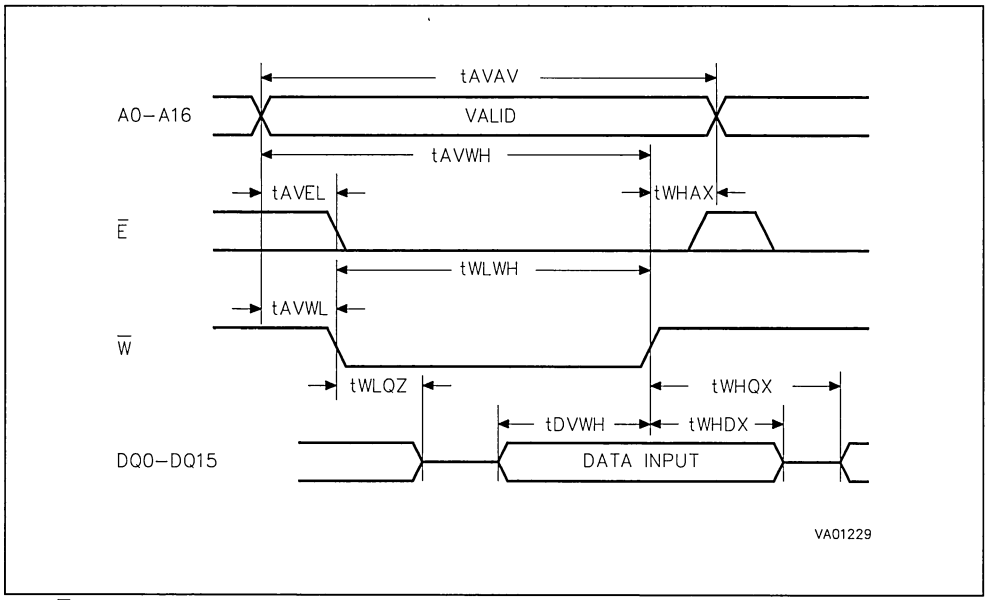
The internal coin cells will maintain data in the M46Z128/128Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the batteries are disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M46Z128 / 128Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	85		120		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	65		85		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		100		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to Write Enable High	35		45		ns
t_{DVEH}	Input Valid to Chip Enable High	35		45		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	10		10		ns
t_{WLQZ} (1,2)	Write Enable Low to Output Hi-Z		30		40	ns
t_{AVWH}	Address Valid to Write Enable High	75		100		ns
t_{AVEH}	Address Valid to Chip Enable High	75		100		ns
t_{WHQX} (1,2)	Write Enable High to Output Transition	0		0		ns

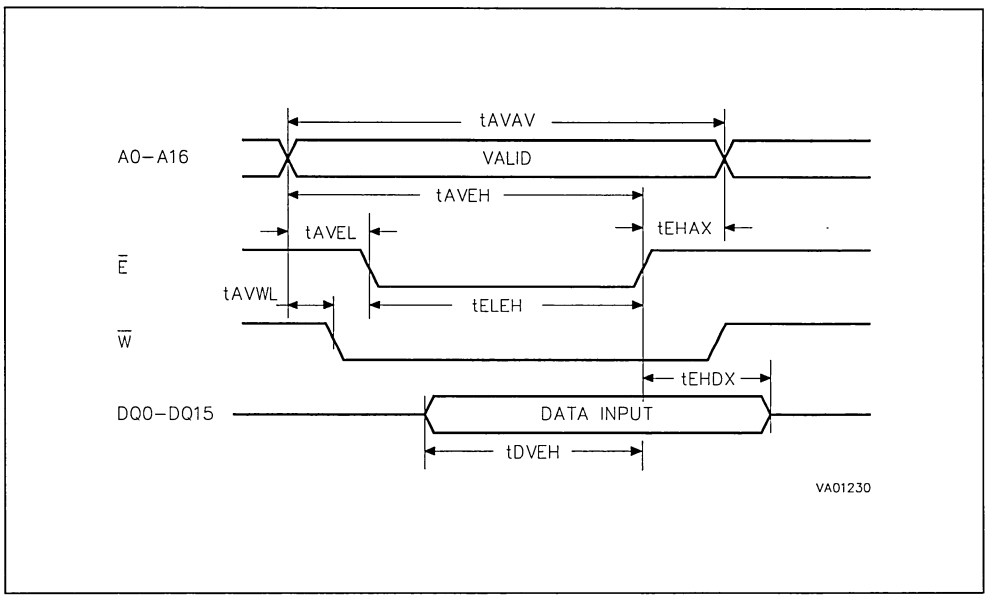
Notes: 1. C_L= 5pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 8. Write Enable Controlled, Write AC Waveforms



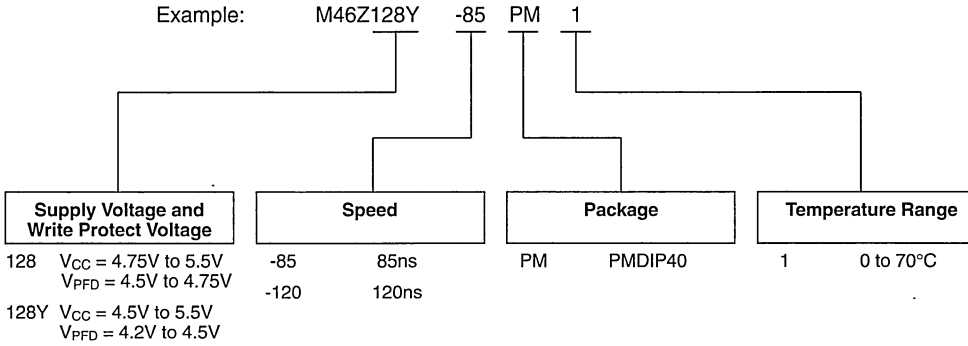
Note: $\overline{G}$ = High.

Figure 9. Chip Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High.

ORDERING INFORMATION SCHEME

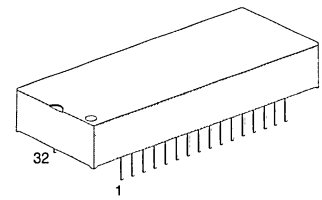


For a list of available options (Package and Speed) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information or any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 512K x 8 ZEROPOWER SRAM

- INTEGRATED LOW POWER SRAMs, POWER-FAIL CONTROL CIRCUIT and BATTERIES
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 5 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 512K x 8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z512: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z512Y: 4.2V ≤ V_{PFD} ≤ 4.50V
- BATTERIES INTERNALLY ISOLATED UNTIL POWER IS APPLIED



PMLDIP32 (PL)
Module

DESCRIPTION

The M48Z512/512Y 512K x 8 ZEROPOWER® RAM is a non-volatile 4,194,304 bit Static RAM organized as 524,288 words by 8 bits. The device combines two internal lithium batteries and full CMOS SRAMs in a plastic 32 pin DIP long Module.

Table 1. Signal Names

A0 - A18	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

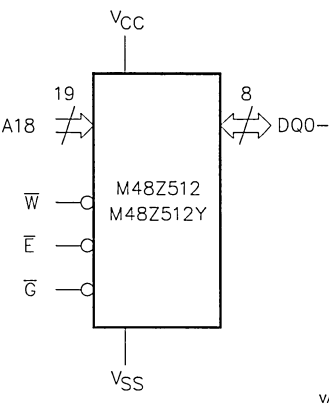


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 70	°C
T_{BIAS}	Temperature Under Bias	–10 to 70	°C
T_{SLD}	Lead Soldering Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

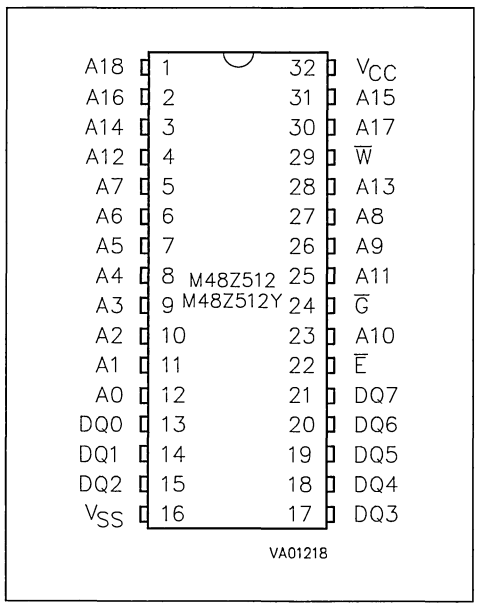
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

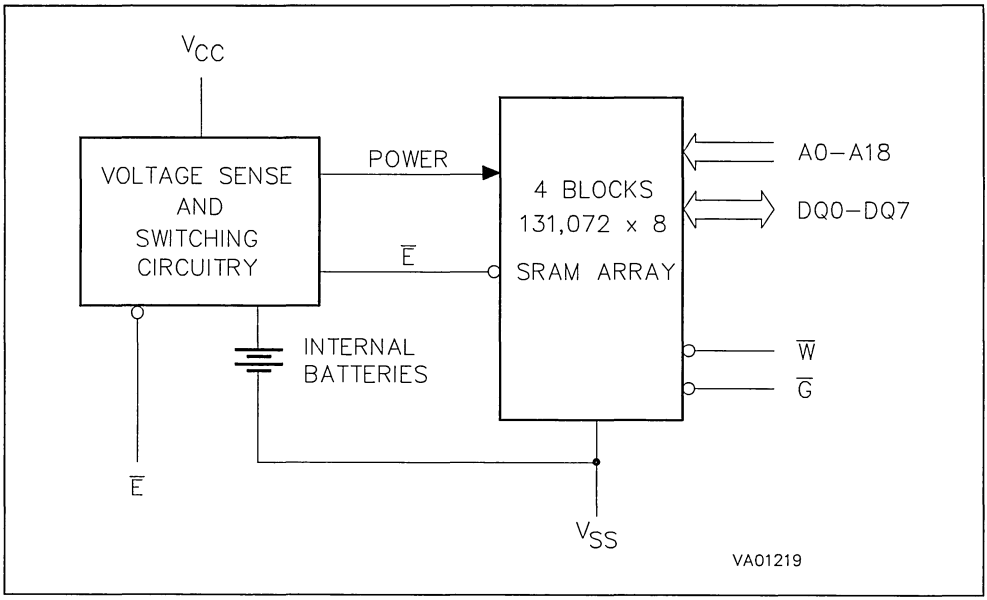
The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z512/512Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the batteries which sustain data until valid power returns.

READ MODE

The M48Z512/512Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 4,194,304 locations in the static storage array. Thus, the unique address specified by the 19 Address Inputs defines which

Figure 3. Block Diagram



one of the 524,288 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z512/512Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

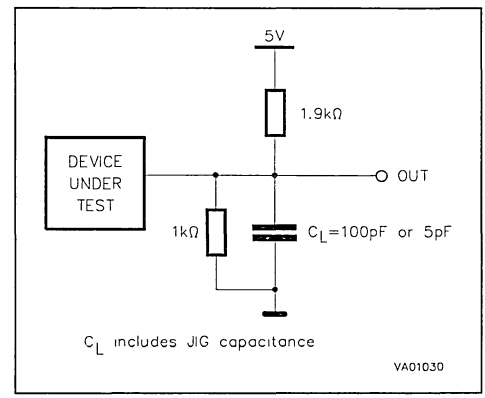


Table 4. Capacitance [1, 2] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		40	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		40	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±4	µA
I_{LO} [1]	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±4	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, Outputs open		115	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		17	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ ≥ V_{CC} – 0.2V		5	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z512)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z512Y)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3		V
t_{DR} [2]	Data Retention Time	5			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_{WP}	Write Protect Time from V_{CC} = V_{PFD}	40	150	µs
t_R	V_{SO} to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{ER}	$\overline{E}$ Recovery Time	40	120	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

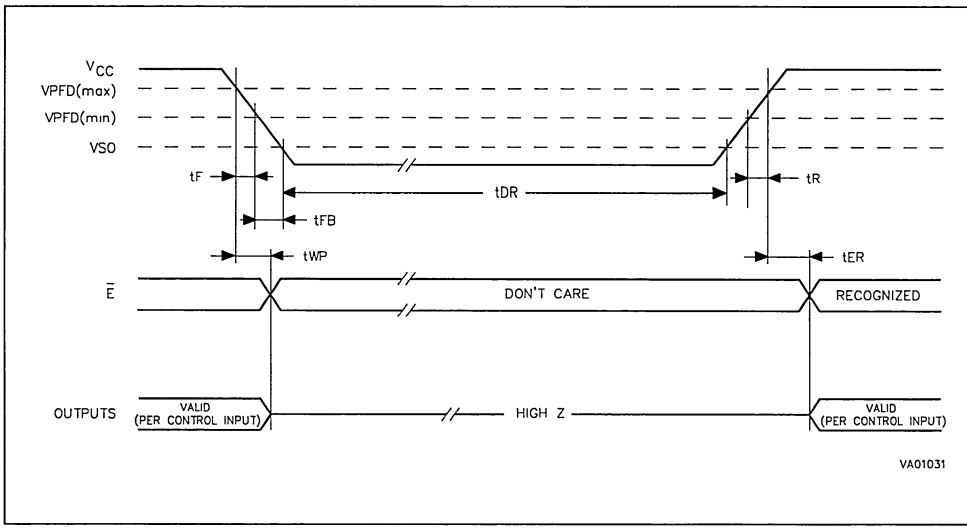
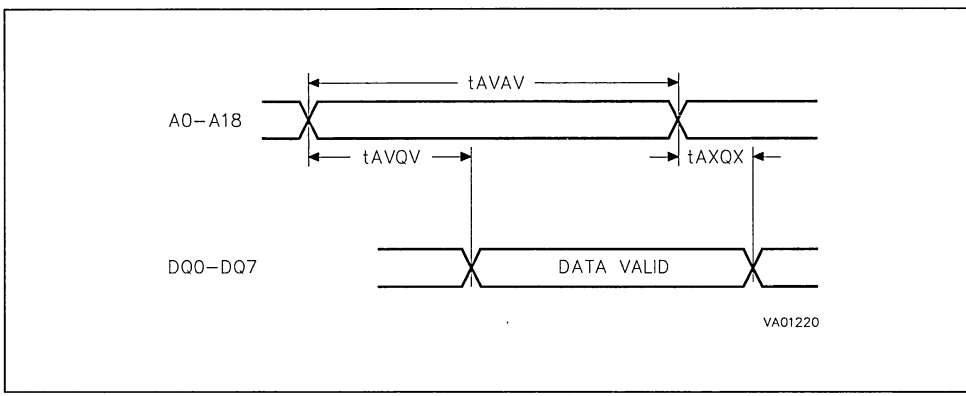


Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z512 / 512Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	85		120		ns
t_{AVQV} (1)	Address Valid to Output Valid		85		120	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		85		120	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		45		60	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		35		45	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25		35	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		10		ns

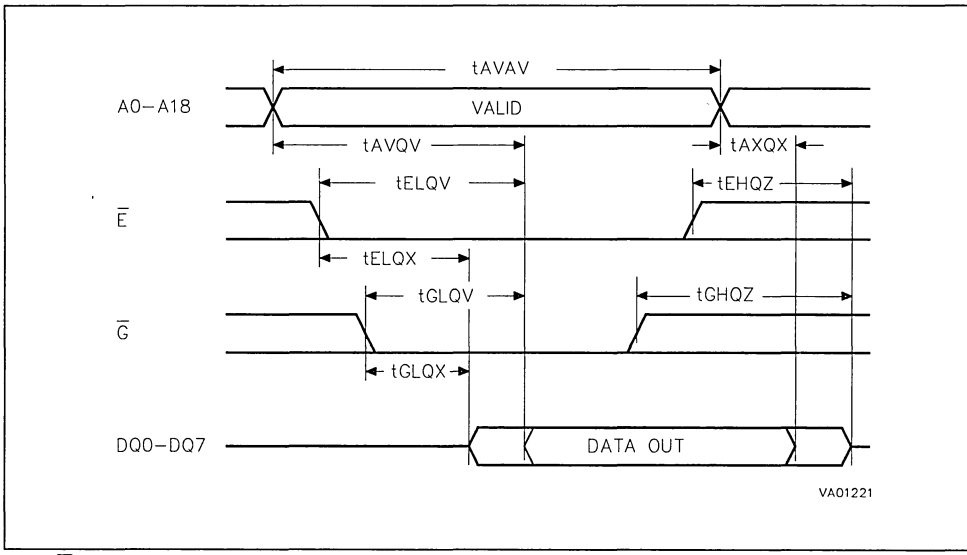
Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4)

Figure 6. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High.

WRITE MODE (cont'd)

The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z512/512Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

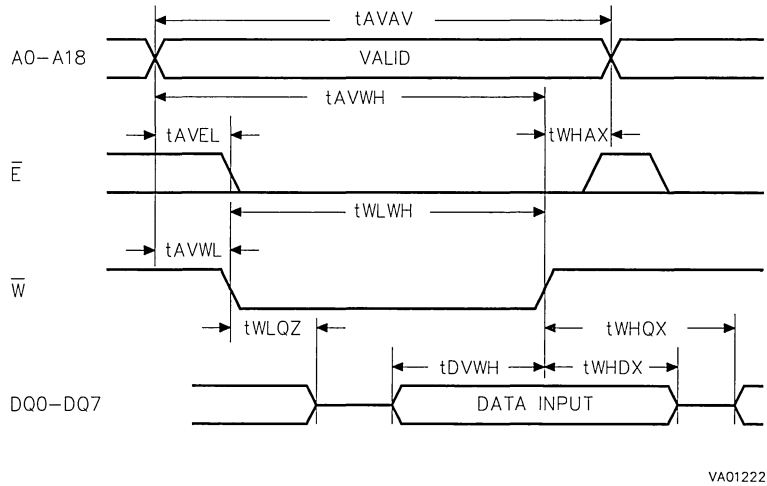
The internal coin cells will maintain data in the M48Z512/512Y after the initial application of V_{CC} for an accumulated period of at least 5 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the batteries are disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z512 / 512Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	85		120		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	65		85		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		100		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to Write Enable High	35		45		ns
t_{DVEH}	Input Valid to Chip Enable High	35		45		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	10		10		ns
t_{WLQZ} (1,2)	Write Enable Low to Output Hi-Z		30		40	ns
t_{AVWH}	Address Valid to Write Enable High	75		100		ns
t_{AVEH}	Address Valid to Chip Enable High	75		100		ns
t_{WHQX} (1,2)	Write Enable High to Output Transition	0		0		ns

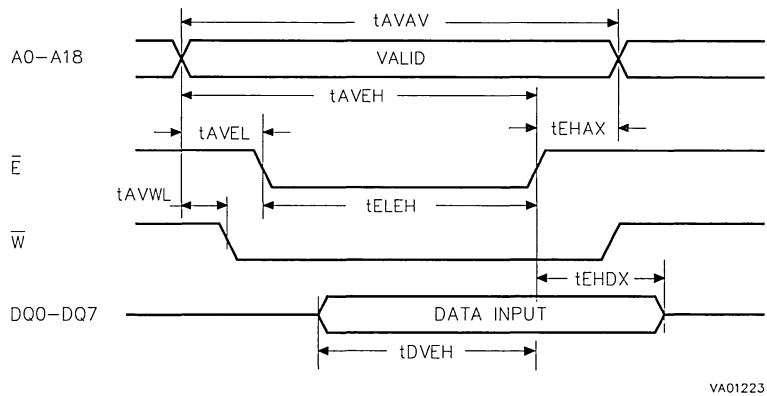
Notes: 1. C_L = 5pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 8. Write Enable Controlled, Write AC Waveforms



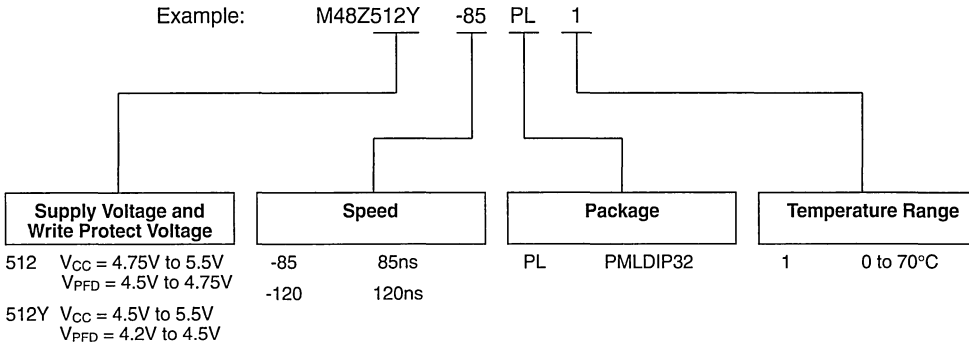
Note: $\overline{G}$ = High.

Figure 9. Chip Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High.

ORDERING INFORMATION SCHEME



For a list of available options (Package and Speed) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

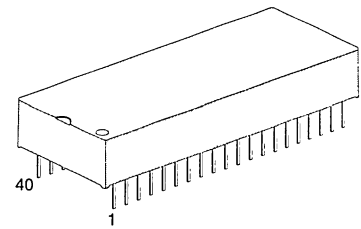
For further information or any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SGS-THOMSON MICROELECTRONICS

M46Z256
M46Z256Y

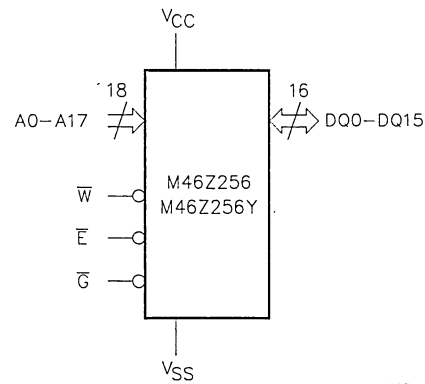
CMOS 256K x 16 ZEROPOWER SRAM

- INTEGRATED LOW POWER SRAMs, POWER-FAIL CONTROL CIRCUIT and BATTERIES
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 5 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 256K x 16 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M46Z256: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z256Y: 4.2V ≤ V_{PFD} ≤ 4.50V
- BATTERIES INTERNALLY ISOLATED UNTIL POWER IS APPLIED



PMDIP40 (PM)
Module

Figure 1. Logic Diagram



DESCRIPTION

The M46Z256/256Y 256K x 16 ZEROPOWER® RAM is a non-volatile 4,194,304 bit Static RAM organized as 262,144 words by 16 bits. The device combines two internal lithium batteries and full CMOS SRAMs in a plastic 40 pin DIP Module.

Table 1. Signal Names

A0 - A17	Address Inputs
DQ0 - DQ15	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 70	°C
T_{BIAS}	Temperature Under Bias	–10 to 70	°C
T_{SLD}	Lead Soldering Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

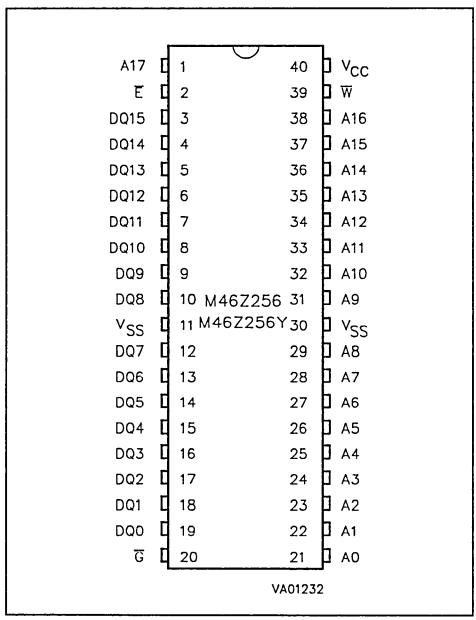
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ15	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

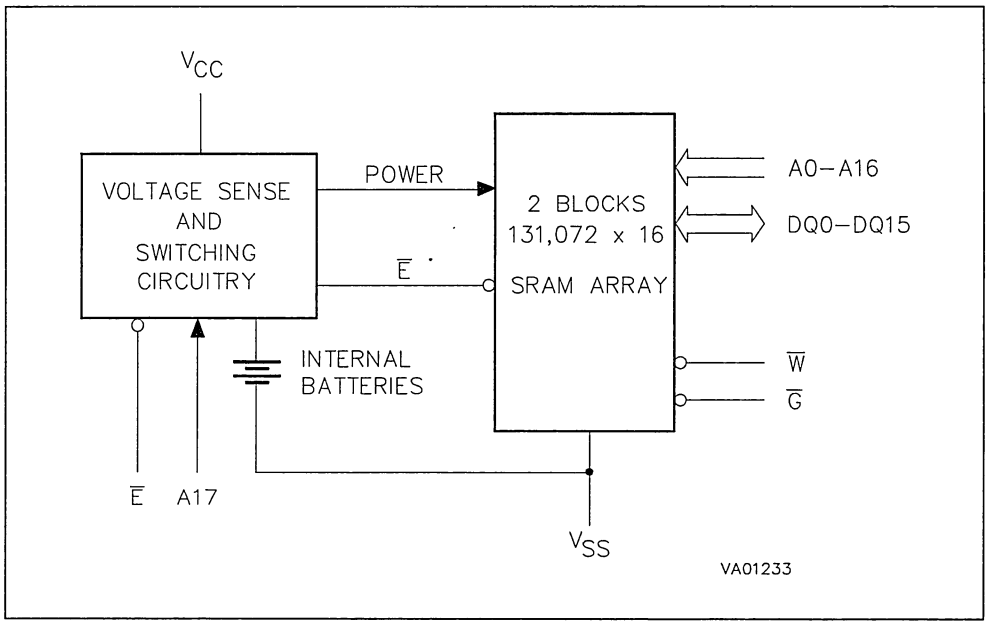
The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M46Z256/256Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the batteries which sustain data until valid power returns.

READ MODE

The M46Z256/256Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from sixteen of 4,194,304 locations in the static storage array. Thus, the unique address specified by the 18 Address Inputs defines which

Figure 3. Block Diagram



one of the 262,144 words of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the sixteen three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M46Z256/256Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

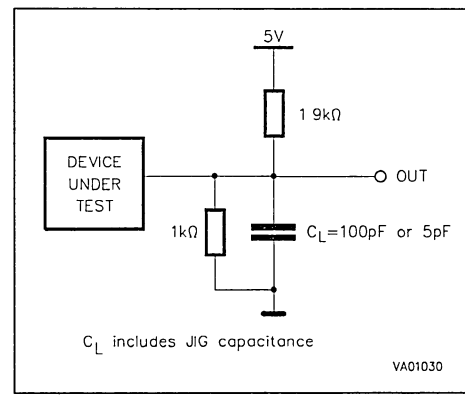


Table 4. Capacitance [1, 2] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		40	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		20	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±4	µA
I_{LO} [1]	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±2	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, Outputs open		200	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		18	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} \ge V_{CC} - 0.2V$		5	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M46Z256)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M46Z256Y)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3		V
t_{DR} [2]	Data Retention Time	5			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_{WP}	Write Protect Time from V_{CC} = V_{PFD}	40	150	µs
t_R	V_{SO} to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{ER}	$\overline{E}$ Recovery Time	40	120	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

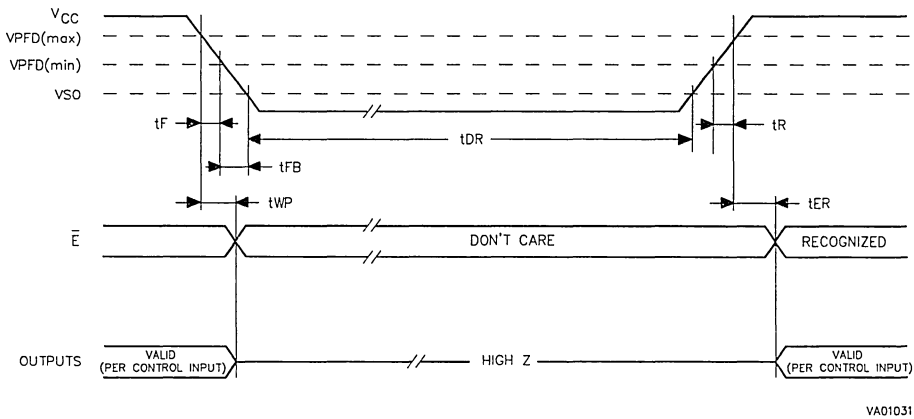
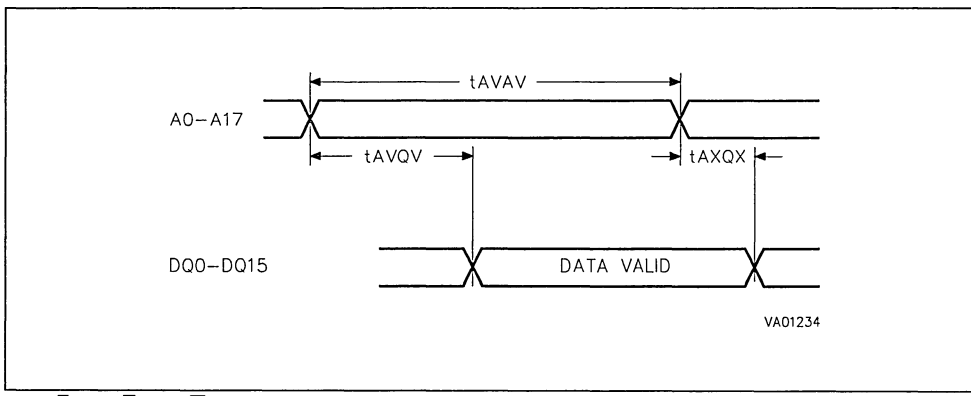


Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M46Z256 / 256Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	85		120		ns
t_{AVQV} (1)	Address Valid to Output Valid		85		120	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		85		120	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		45		60	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		35		45	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25		35	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		10		ns

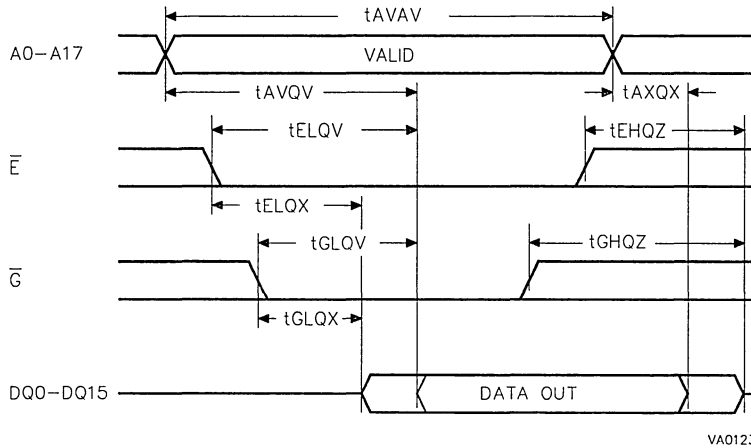
Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4)

Figure 6. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High.

WRITE MODE (cont'd)

$\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M46Z256/256Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

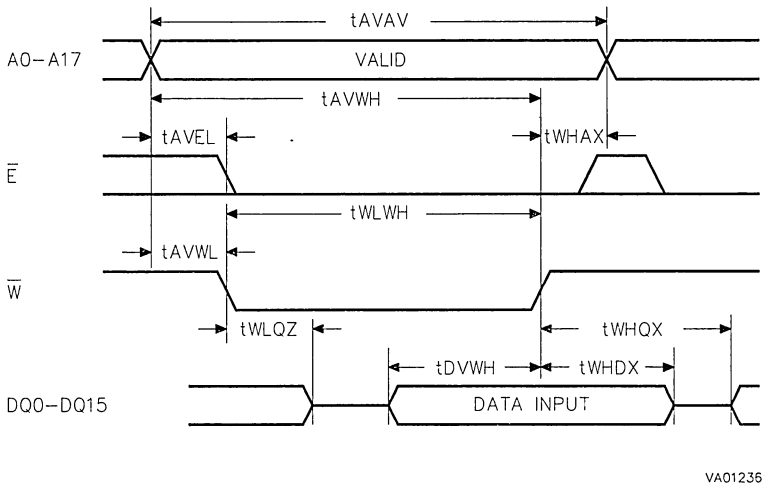
The internal coin cells will maintain data in the M46Z256/256Y after the initial application of V_{CC} for an accumulated period of at least 5 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the batteries are disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M46Z256 / 256Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	85		120		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	65		85		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		100		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to Write Enable High	35		45		ns
t_{DVEH}	Input Valid to Chip Enable High	35		45		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	10		10		ns
t_{WLQZ} (1,2)	Write Enable Low to Output Hi-Z		30		40	ns
t_{AVWH}	Address Valid to Write Enable High	75		100		ns
t_{AVEH}	Address Valid to Chip Enable High	75		100		ns
t_{WHQX} (1,2)	Write Enable High to Output Transition	0		0		ns

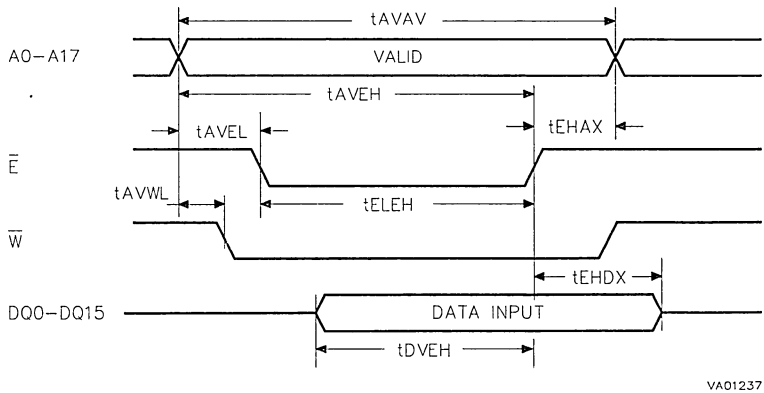
Notes: 1. C_L = 5pF (see Figure 4).
2. If E goes low simultaneously with $\overline{W}$ going low after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 8. Write Enable Controlled, Write AC Waveforms



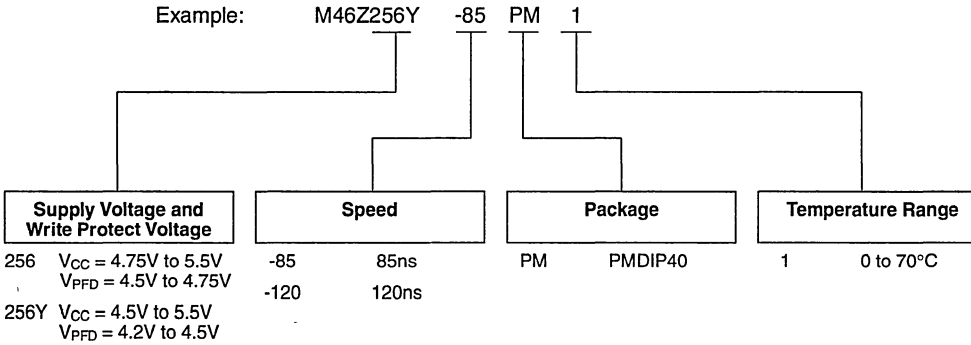
Note: $\overline{G}$ = High.

Figure 9. Chip Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High.

ORDERING INFORMATION SCHEME



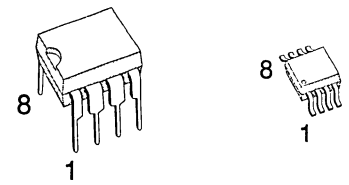
For a list of available options (Package and Speed) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information or any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

TIMEKEEPER MEMORIES

CMOS 64 x 8 SERIAL ACCESS TIMEKEEPER SRAM

- COUNTERS for SECONDS, MINUTES, HOURS, DAY, DATE, MONTH and YEARS
- SOFTWARE CLOCK CALIBRATION
- AUTOMATIC POWER FAIL DETECT and SWITCH CIRCUITRY
- I^2C BUS COMPATIBLE
- 56 BYTES of GENERAL PURPOSE RAM
- ULTRA-LOW BATTERY SUPPLY CURRENT of 500nA
- AVAILABLE with an OPERATING TEMPERATURE of –40 to 85 °C



PSDIP8 (N)
0.4mm Frame

SO8 (S)
0.15mm Frame

DESCRIPTION

The MK41T56 TIMEKEEPER™ RAM is a low power 512 bit static CMOS RAM organized as 64 words by 8 bits. A built-in 32.768 kHz oscillator (external crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in BCD format. Addresses and data are transferred serially via a two-line bi-directional bus. The built-in address register is incremented automatically after each write or read data byte. The MK41T56 clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power failures. The energy needed to sustain the RAM and clock operations can be supplied from a small lithium button cell.

Table 1. Signal Names

OSCI	Oscillator Input
OCSO	Oscillator Output
FT/OUT	Frequency Test / Output Driver
SDA	Serial Data Address Input / Output
SCL	Serial Clock
V_{BAT}	Battery Supply Voltage
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

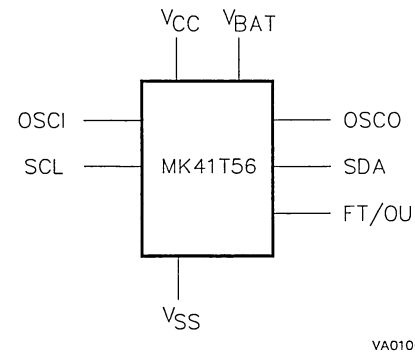


Figure 2A. DIP Pin Connections

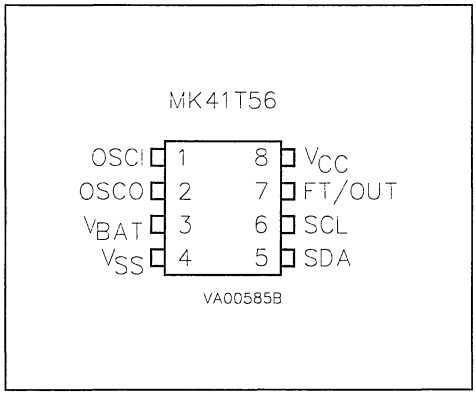


Figure 2B. SO Pin Connections

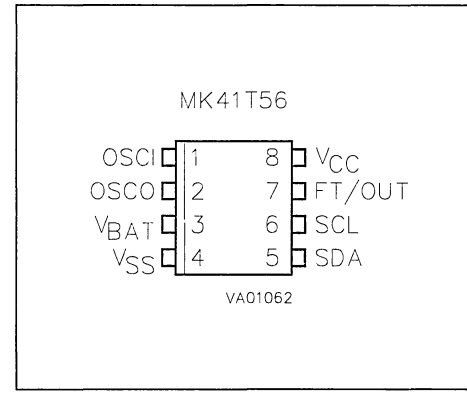


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–55 to 125	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	0.25	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

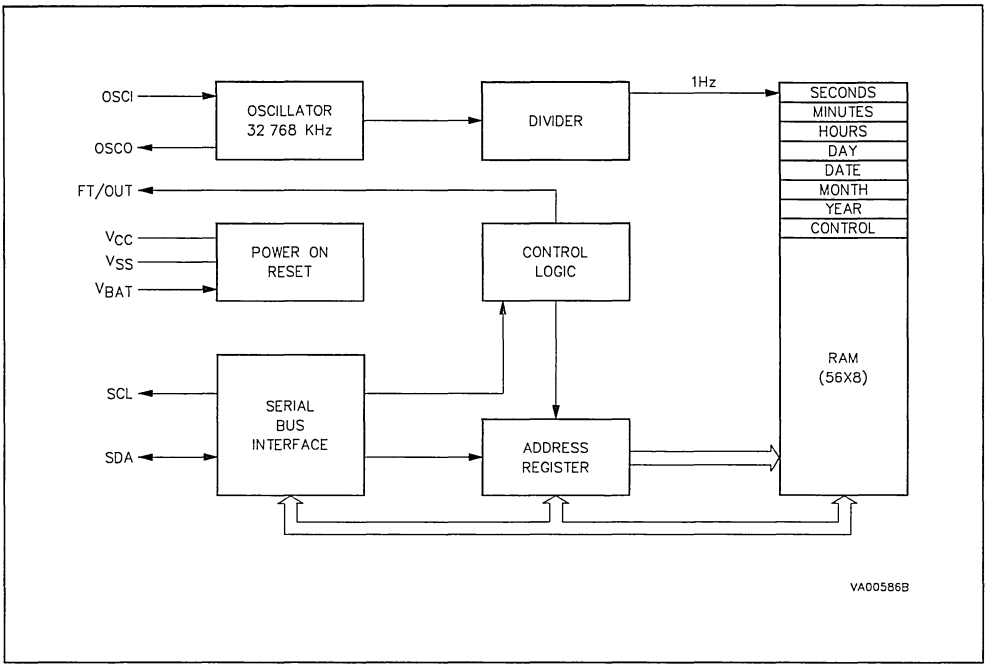
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST								Seconds	00-59
1	X								Minutes	00-59
2	X	X							Hour	00-23
3	X	X	X	X	X				Day	01-07
4	X	X							Date	01-31
5	X	X							Month	01-12
6									Year	00-99
7	OUT	FT	S						Control	

Keys: **S** = SIGN Bit; **FT** = FREQUENCY TEST Bit; **ST** = STOP Bit; **OUT** = Output level; **X** = Don't care.

Figure 3. Block Diagram



DESCRIPTION (cont'd)

Typical data retention time is in excess of 10 years with a 39 mA/h 3V lithium cell. The MK41T56 clock is supplied in 8 Pin Plastic Dual-in-Line and 8 pin Plastic Small Outline packages.

OPERATION

The MK41T56 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct address (D0). The 64 bytes contained in the device can then be accessed sequentially in the following order:

1. Seconds Register
2. Minutes Register
3. Hours Register
4. Day Register
5. Date Register
6. Month Register
7. Years Register
8. Control Register

9 to 64. RAM

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

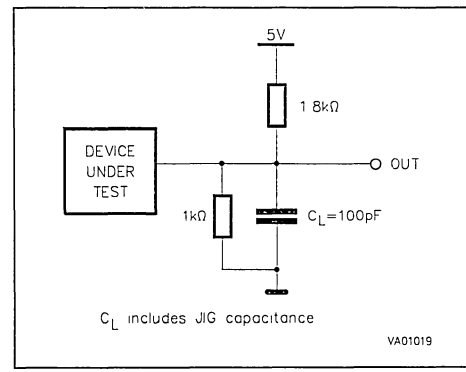


Table 4. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SCL)		7	pF
C_{OUT} [2]	Output Capacitance (SDA, FT/OUT)		10	pF

Notes: 1. Effective capacitance calculated from the equation C = IΔt/ΔV with ΔV = 3V and power supply at 5V.
2. Outputs deselected.

Table 5. DC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}			±10	µA
I_{CC1}	Supply Current	SCL/SDA = V_{CC}–0.3V			3	mA
I_{CC2}	Supply Current (Standby)				1	mA
V_{IL}	Input Low Voltage		–0.3		1.5	V
V_{IH}	Input High Voltage		3		V_{CC} + 0.8	V
V_{OL}	Output Low Voltage	I_{OL} = 5mA, V_{CC} = 4.5V			0.4	V
V_{BAT} [1]	Battery Supply Voltage		2.6	3	3.5	V
I_{BAT}	Battery Supply Current	T_A = 25°C, V_{CC} = 0V, Oscillator ON, V_{BAT} = 3V		450	500	nA

Note: SGS-THOMSON recommends the RAYOVAC BR1225 or equivalent as the battery supply.

Table 6. Power Down/Up Trip Points DC Characteristics[1] (T_A = 0 to 70°C or –40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage	1.22 V_{BAT}	1.25 V_{BAT}	1.28 V_{BAT}	V
V_{SO}	Battery Back-up Switchover Voltage		V_{BAT}		V

Note: 1. All voltages referenced to V_{SS}.

Table 7. Crystal Electrical Characteristics (Externally Supplied)

Symbol	Parameter	Min	Typ	Max	Unit
f_O	Resonant Frequency		32.768		kHz
R_S	Series Resistance			35	kΩ
C_L	Load Capacitance		12.5		pF

Notes: Load capacitors are internally supplied with the MK41T56. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

SGS-THOMSON recommends the ECS-.327-12.5-8SP-2 quartz crystal for industrial temperature operations. ESC Inc. can be contacted at 800-237-1041 or 913-782-7787 for further information on this crystal type.

Table 8. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C or –40 to 85°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	SCL and SDA at V_{IH} before Power Down	0		ns
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	300		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	100		µs
t_{REC}	SCL and SDA at V_{IH} after Power Up	200		µs

Figure 5. Power Down/Up Mode AC Waveforms

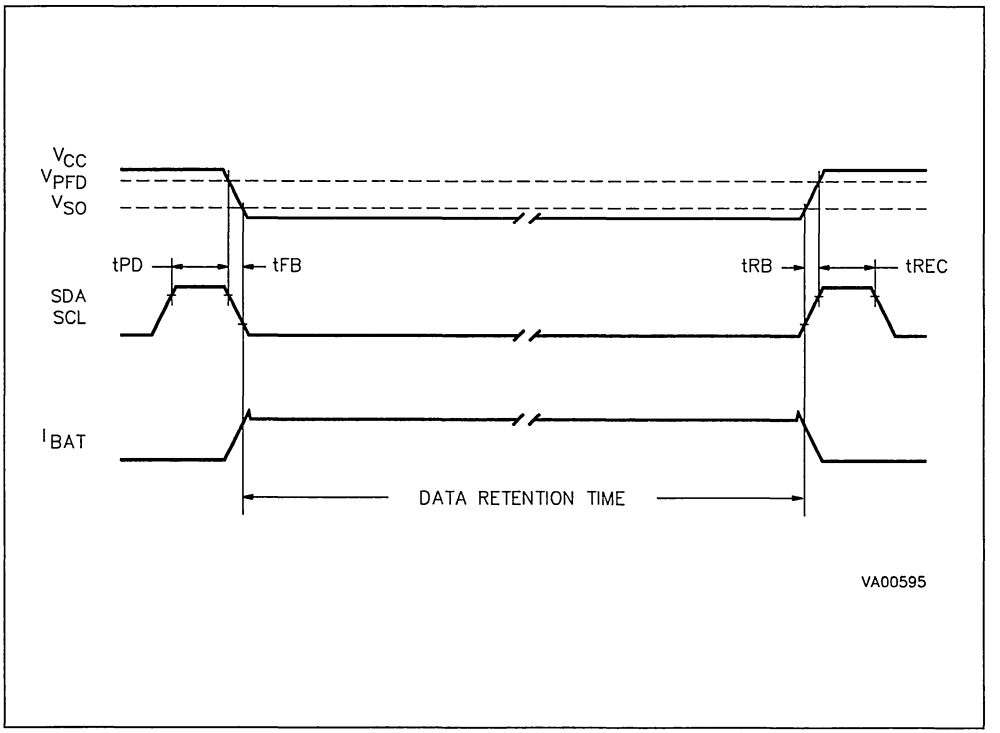


Table 9. AC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL Clock Frequency	0	100	kHz
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4		µs
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{HD\ STA}$	START Condition Hold Time (after this period the first clock pulse is generated)	4		µs
$t_{SU\ STA}$	START Condition Setup Time (only relevant for a repeated start condition)	4.7		µs
$t_{SU\ DAT}$ (1)	Data Setup Time	250		ns
$t_{HD\ DAT}$	Data Hold Time	0		µs
$t_{SU\ STO}$	STOP Condition Setup Time	4.7		µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		µs
t_I	Noise suppresion time constant at SCL and SDA input	0.25	1	µs

Note: 1. Transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

OPERATION (cont'd)

The MK41T56 clock continually monitors V_{CC} for an out of tolerance condition. Should V_{CC} fall below V_{PFD} the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When V_{CC} falls below V_{BAT} the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. Upon power up the device switches from battery to V_{CC} at V_{BAT} and recognizes inputs when V_{CC} goes above V_{PFD} volts.

2-WIRE BUS CHARACTERISTICS

This bus is intended for communication between different ICs. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

– Data transfer may be initiated only when the bus is not busy.

– During data transfer, the data line must remain stable whenever the clock line is High. Changes in the data line while the clock line is High will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy. Both data and clock lines remain High.

Start data transfer. A change in the state of the data line, from High to Low, while the clock is High, defines the START condition.

Stop data transfer. A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

Data valid. The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is trans-

Figure 6. Serial Bus Data Transfer Sequence

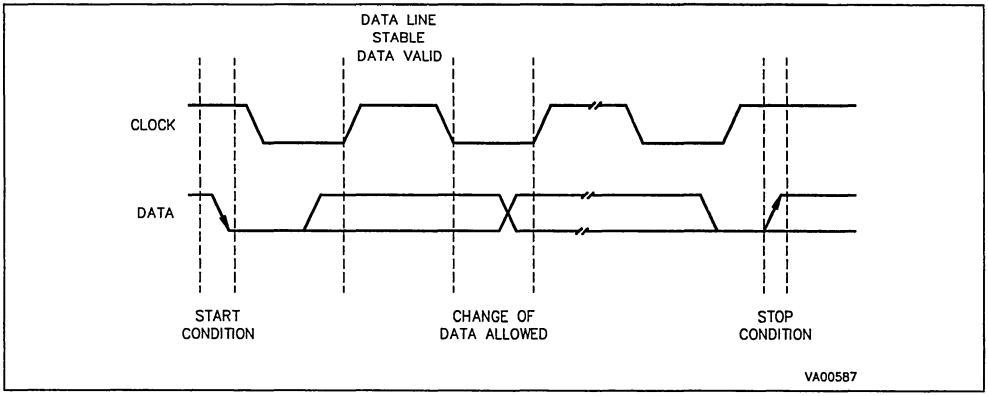


Figure 7. Acknowledgement Sequence

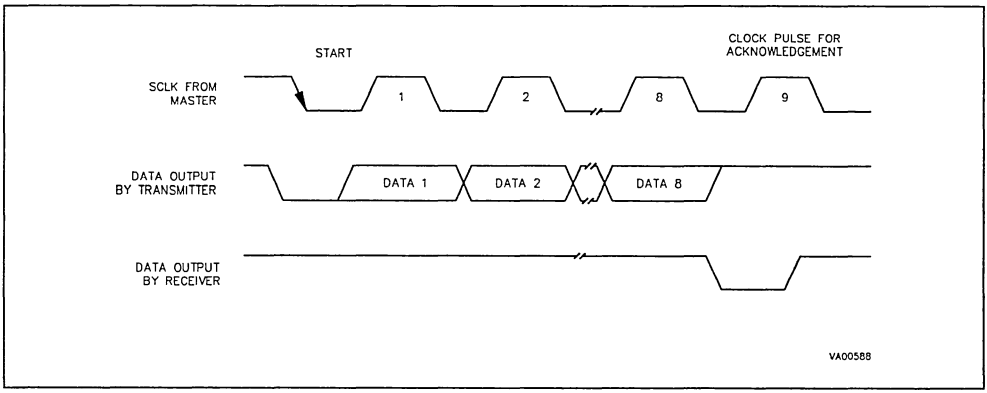
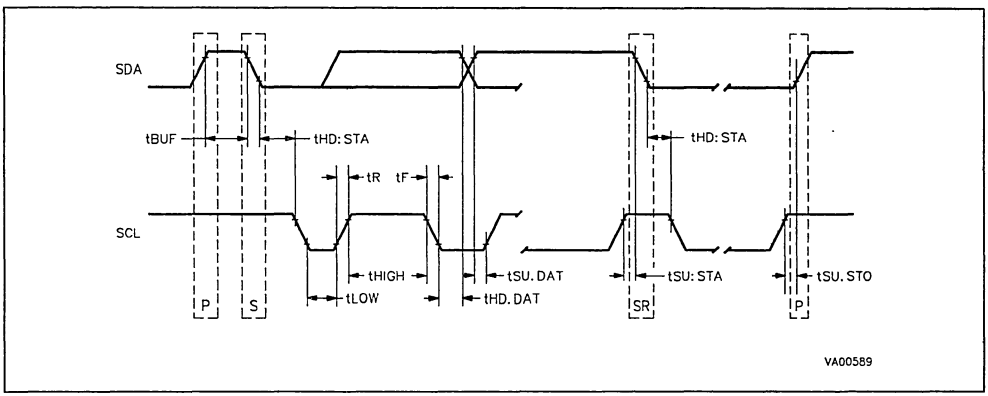


Figure 8. Bus Timing Requirements Sequence



2-WIRE BUS CHARACTERISTICS (cont'd)

mitted byte-wide and each receiver acknowledges with a nineth bit.

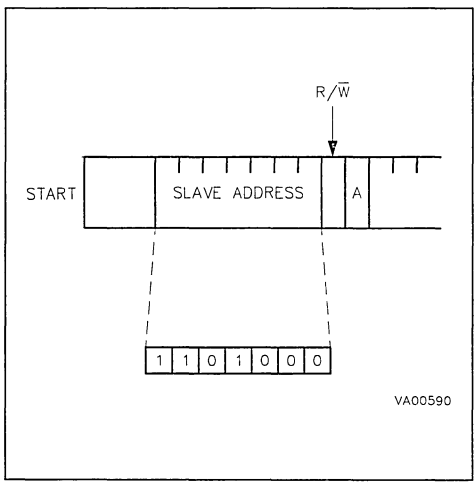
Within the bus specifications a low speed mode (2kHz clock rate) and a high speed mode (100kHz clock rate) are defined. The MK41T56 clock works in both modes. By definition a device that gives out a message is called "transmitter", the receiving device that gets the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

Acknowledge. Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line High to enable the master to generate the STOP condition.

Figure 9. Slave Address Location



WRITE MODE

In this mode the master transmitter transmits to the MK41T56 slave receiver. Bus protocol is shown in Figure 10. Following the START condition and slave address, a logic '0' ($R/\overline{W} = 0$) is placed on the bus and indicates to the addressed device that word address A_n will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The MK41T56 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte, see Figure 9.

READ MODE

In this mode the master reads the MK41T56 slave after setting the slave address, see Figure 11. Following the write mode control bit ($R/\overline{W} = 0$) and the acknowledge bit, the word address A_n is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit ($R/\overline{W} = 1$). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The MK41T56 slave transmitter will now place the data byte at address An + 1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented whereby the master reads the MK41T56 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer, see Figure 12.

CLOCK CALIBRATION

The MK41T56 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. A typical MK41T56 is accurate within ± 1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim

Figure 10. Write Mode Sequence

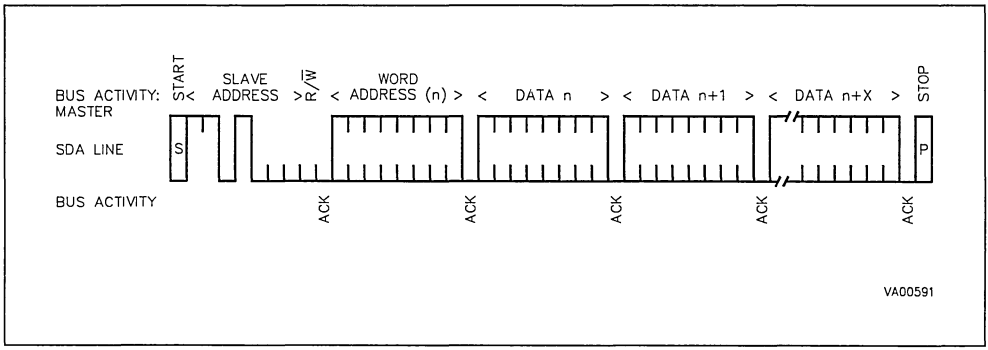


Figure 11. Read Mode Sequence

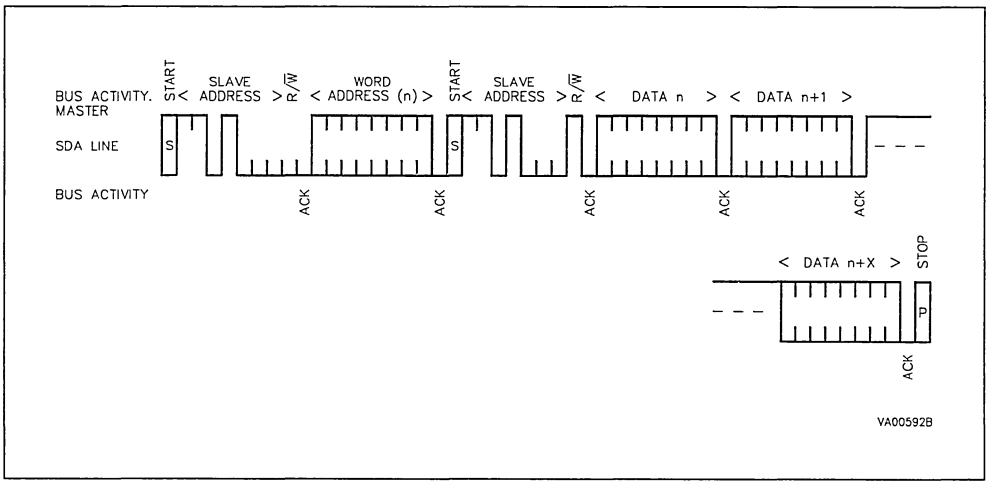
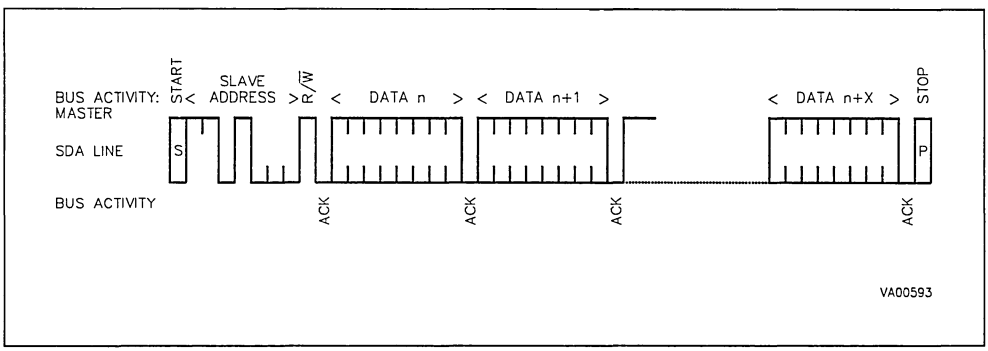


Figure 12. Alternate Read Mode Sequence

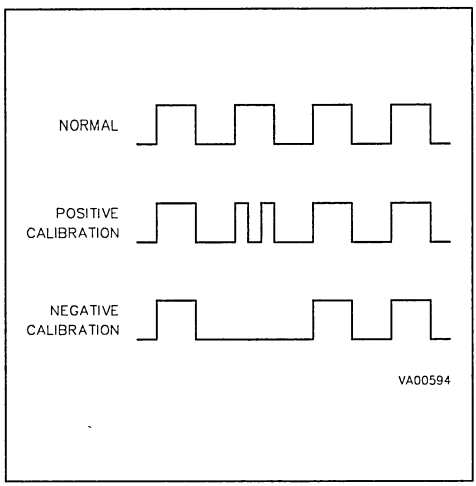


CLOCK CALIBRATION (cont'd)

capacitors. The MK41T56 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 13. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minutes cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minutes cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Figure 13. Divide by 128 Stage



Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is + 4.068 or –2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32768 Hz, each of the 31 increments in the Calibration byte would represent 10.7 seconds per month.

Two methods are available for ascertaining how much calibration a given MK41T56 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accessed the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Control Register, is set to a '1', and the oscillator is running at 32768 Hz, the FT/OUT pin of the device will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature.

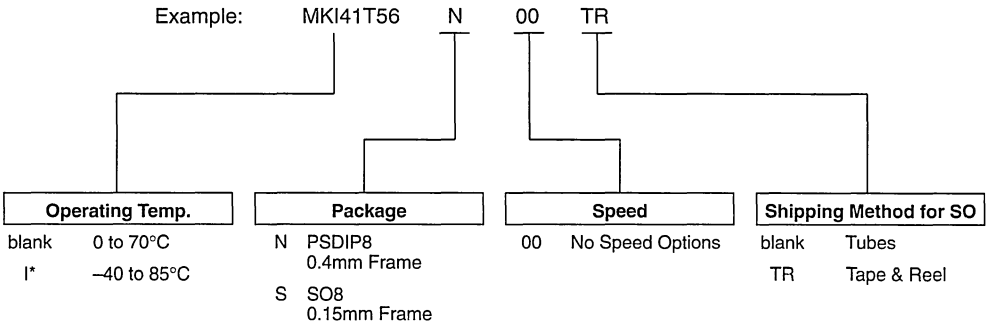
For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a –10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

OUTPUT DRIVER PIN

When the FT bit is not set the FT/OUT pin becomes an output driver that reflects the contents of D7 of the control register. In other words when D6 of location 7 is a zero and D7 of location 7 is a zero and then the FT/OUT pin will be driven low.

Note: The FT/OUT pin is open drain which requires an external pull-up resistor.

ORDERING INFORMATION SCHEME



Note: I* Available in the SO package only.

For a list of available options refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

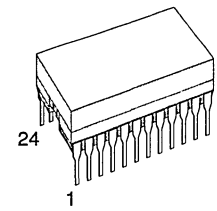
For further information or any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

SGS-THOMSON MICROELECTRONICS

MK48T87

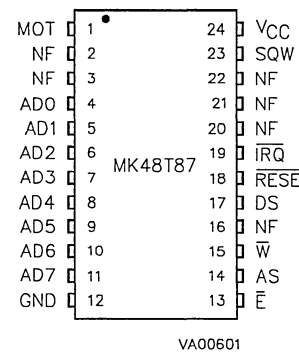
CMOS 64 x 8 ADDRESS/DATA MULTIPLEXED TIMEKEEPER SRAM

- DROP-IN REPLACEMENT FOR PC AT COMPUTER CLOCK/CALENDAR
- TOTALLY NONVOLATILE WITH 10 YEARS OF OPERATION IN THE ABSENCE OF POWER
- SELF-CONTAINED SUBSYSTEM INCLUDES LITHIUM BATTERY, QUARTZ CRYSTAL AND SUPPORT CIRCUITRY
- COUNTS SECONDS, MINUTES, HOURS, DAYS, DAY OF THE WEEK, DATE, MONTH AND YEAR WITH LEAP YEAR COMPENSATION
- BINARY OR BCD REPRESENTATION OF TIME, CALENDAR AND ALARM
- 12 OR 24 HOUR CLOCK WITH AM AND PM IN 12 HOUR MODE
- SELECTABLE BUS TIMING
- MULTIPLEX BUS FOR PIN EFFICIENCY
- INTERFACED WITH SOFTWARE AS 64 RAM LOCATIONS:
  - 14 Bytes Of Clock And Control Registers
  - 50 Bytes Of General Purpose RAM
- PROGRAMMABLE SQUARE WAVE OUTPUT SIGNAL
- BUS COMPATIBLE INTERRUPT SIGNALS (IRQ)
- THREE INTERRUPTS ARE SEPARATELY SOFTWARE-MASKABLE AND TESTABLE:
  - Time-of-day Alarm Once/Second To Once/Day
  - Periodic Rates From 122 µs to 500 ms
  - End Of Clock Update Cycle



PHDIP24 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connection



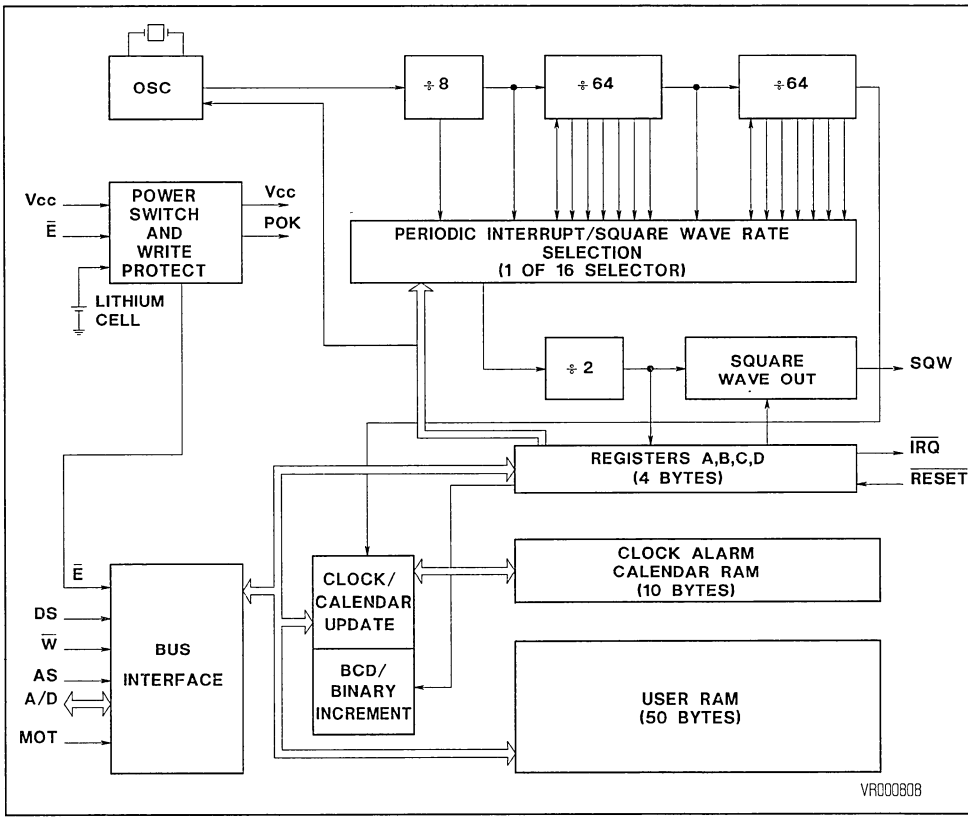
PIN NAMES

AD0 - AD7	Address / Data
V_{CC}/GND	5 Volts/Ground
$\overline{E}$	Chip Select
AS	Address Strobe
$\overline{W}$	Read/Write
SQW	Square Wave Out
MOT	Bus Type Selection

$\overline{IRQ}$	Interrupt Request
$\overline{RESET}$	Reset
DS	Data Strobe
NF	No Function

NF pin serves no function and may be connected to other signals, within Absolute Maximum Ratings, without affecting device operation. The electrical characteristics are the same as the other inputs pins.

Figure 2. Block Diagram



DESCRIPTION

The MK48T87 TIMEKEEPER™ RAM is designed to be a compatible replacement for the MC146818 and the DS1287. A lithium energy source, a quartz crystal and write-protection circuitry are contained within a 24-pin dual in-line package. The MK48T87 is, therefore, a complete subsystem replacing as many as 16 components in a typical application. The functions available to the user include a non-volatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The Real Time Clock/RAM is unique in that the time-of-day and memory are maintained even in the absence of power.

Automatic deselection of the device provides insurance that data integrity is not compromised should V_{CC} fall below specified (V_{PFD}) levels. The automatic deselection of the device remains in effect upon power up for a period of 100ms after V_{CC} rises above V_{PFD}, provided the Real Time Clock is running and the count down chain is not in reset. This allows sufficient time for V_{CC} to stabilize and gives the system clock a wake up period so that a valid system reset can be established.

The block diagram in Figure 2 shows the pin connection with the major internal functions of MK48T87 (Real Time Clock/RAM). The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} - D.C. power is provided to the device on these pins. V_{CC} is the +5 volt input. When V_{CC} is applied and is above V_{PFD}, the device is fully accessible and the data can be written and read. When V_{CC} is below V_{PFD}, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below V_{SO}, the RAM and timekeeper are switched over to an internal Lithium energy source. The timekeeping function maintains an accuracy of 1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

MOT (Mode Select) - The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 KΩ .

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin may be changed by programming Register A. As shown in Table 1, the SQW signal may be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than V_{PFD}.

Table 1. Periodic Interrupt Rate and Square Wave Frequency

Select Bits Register A				t_{PI} Periodic Interrupt Rate	SQW Output Frequency
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 KHz
0	1	0	0	244.141 µs	4.096 KHz
0	1	0	1	488.281 µs	2.048 KHz
0	1	1	0	976.5625 µs	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0-AD7 (Multiplexed Bi-Directional Address/Data Bus) - Multiplexing the bus reduces the device pin count because address information and data information time share the same signal paths. The addresses are presented during the first portion of the bus cycle and the same pins and signal paths are used for data transfer during the second portion of the cycle. Address/data multiplexing does not slow the access time of the MK48T87 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the MK48T87 latches the address from AD0 to AD5. Valid write data must be present and held stable during the latter portion of the DS or RD pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as RD transitions high in the case of Intel timing.

AS (Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the MK48T87.

DS (Data Strobe or Read Input) - The DS/RD pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the MK48T87 is to drive the bi-directional bus. In write cycles the trailing edge of DS causes the MK48T87 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read (RD). RD identifies the time period when the MK48T87 drives the bus with read data. The RD signal is the same definition as the Output Enable ($\overline{G}$) signal on a typical memory.

W (Read/Write Input) - The $\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, $\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on $\overline{W}$ while DS is high. A write cycle is indicated when $\overline{W}$ is low during DS. When the MOT pin is connected to GND for Intel timing, the $\overline{W}$ signal is an active low signal called WR. In this mode the $\overline{W}$ pin has the same meaning as the Write Enable signal ($\overline{W}$) on generic RAMs.

E (Chip Select Input) - The Chip Select signal ($\overline{E}$) must be asserted low for a bus cycle in which the MK48T87 is to be accessed. $\overline{E}$ must be kept in the active state during DS and AS for Motorola timing and during RD and $\overline{W}$ for Intel timing. Bus cycles which take place without asserting $\overline{E}$ will latch addresses but no access will occur. When V_{CC} is below V_{PFD}, the MK48T87 internally inhibits access cycles by internally disabling the $\overline{E}$ input. This action protects both the Real Time Clock data and RAM data during power outages.

IRQ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the MK48T87 that may be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt- enable bit is set. To clear the $\overline{IRQ}$ pin the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts. When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupt devices may be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull-up resistor.

RESET (Reset Input) - The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{RESET}$ pin may be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power up, the time $\overline{RESET}$ is low should exceed 200 ms to make sure that the internal timer which controls the MK48T87 on power-up has timed out. When $\overline{RESET}$ is low and V_{CC} is above V_{PFD}, the following occurs:

A. Periodic Interrupt Enable (PIE) bit is cleared to zero.

B. Alarm Interrupt Enable (AIE) bit is cleared to zero.

C. Update Ended Interrupt Flag (UF) bit is cleared to zero.

D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.

E. Periodic Interrupt Flag (PF) bit is cleared to zero.

F. The device is not accessible until $\overline{RESET}$ is returned high.

G. Alarm Interrupt Flag (AF) bit is cleared to zero.

H. $\overline{IRQ}$ pin is in the high impedance state.

I. Square Wave Output Enable (SQWE) bit is cleared to zero.

J. Updated Ended Interrupt Is Cleared To Zero.

In a typical application $\overline{RESET}$ may be connected to Vcc. This connection will allow the MK48T87 to go in and out of power fail without affecting any of the control registers.

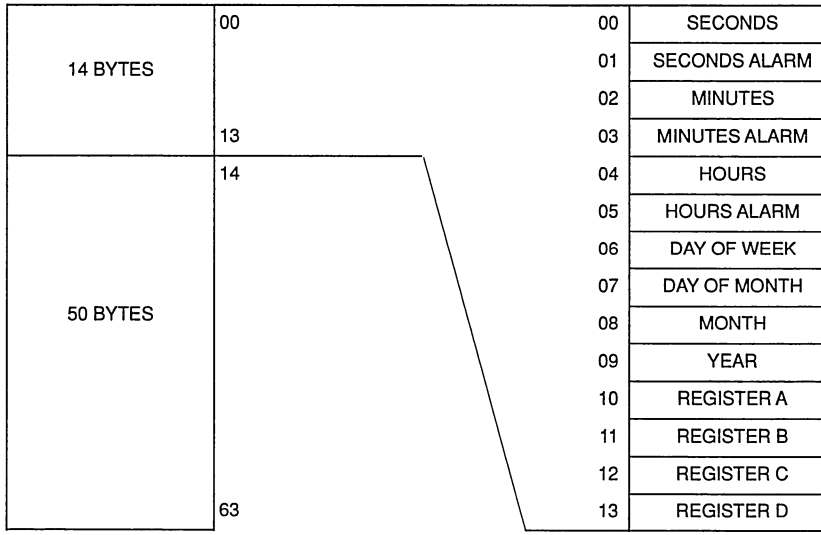
ADDRESS MAP

The Address Map of the MK48T87 is shown in Figure 3. The address map consists of 50 bytes of user RAM, 10 bytes of RAM which contain the RTC time, calendar and alarm data, and 4 bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

The contents of four control registers (A,B,C,D) are described in the "Register" section.

Figure 3. Address Map



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar and alarm bytes may be either Binary or Binary-Coded (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a Logic one to prevent updates from occuring while access is being attempted. In addition to writing the ten time, calendar and alarm registers in a selected format (Binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the Real Time Clock to update the time and calendar bytes. Once initialized, the Real Time Clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the Binary and BCD formats of the ten time, calendar and alarm locations. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exits that seconds, minutes, hours, etc., may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

Table 2. Calendar and Alarm Data Modes

Address Location	Function	Decimal Range	Range	
			Binary Data Mode	BCD Data Mode
0	SECONDS	00 - 59	00 - 3B	00 - 59
1	SECONDS ALARM	00 - 59	00 - 3B	00 - 59
2	MINUTES	00 - 59	00 - 3B	00 - 59
3	MINUTES ALARM	00 - 59	00 - 3B	00 - 59
4	HOURS - 12hrs MODE	1 - 12	01 - 0C AM, 81 - 8C PM	01 - 12 AM, 81 - 92 PM
	HOURS - 24hrs MODE	0 - 23	00 - 17	00 - 23
5	HOURS ALARM - 12hrs	1 - 12	01 - 0C AM, 81 - 8C PM	01 - 12 AM, 81 - 92 PM
	HOURS ALARM - 24hrs	0 - 23	00 - 17	00 - 23
6	DAY OF THE WEEK (SUNDAY=1)	1 - 7	01 - 07	01 - 07
7	DAY OF THE MONTH	1 - 31	01 - 1F	01 - 31
8	MONTH	1 - 12	01 - 0C	01 - 12
9	YEAR	0 - 99	00 - 63	00 - 99

The three alarm bytes may be used in two ways. First, when the alarm time is written in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at Logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

NONVOLATILE RAM

The 50 general purpose non-volatile RAM bytes are not dedicated to any special function within the MK48T87. They can be used by the processor program as non-volatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt may be programmed to occur at rates from once per second to once per day. The periodic interrupt may be selected for rates from 122 µs to 500 ms. The update-ended interrupt may be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a Logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in an interrupt enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to Logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary.

When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two or three bits may be set when reading Register C. Each utilized flag bit should be examined when read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in Bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the MK48T87. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the MK48T87 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 2. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the IRQ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which may be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

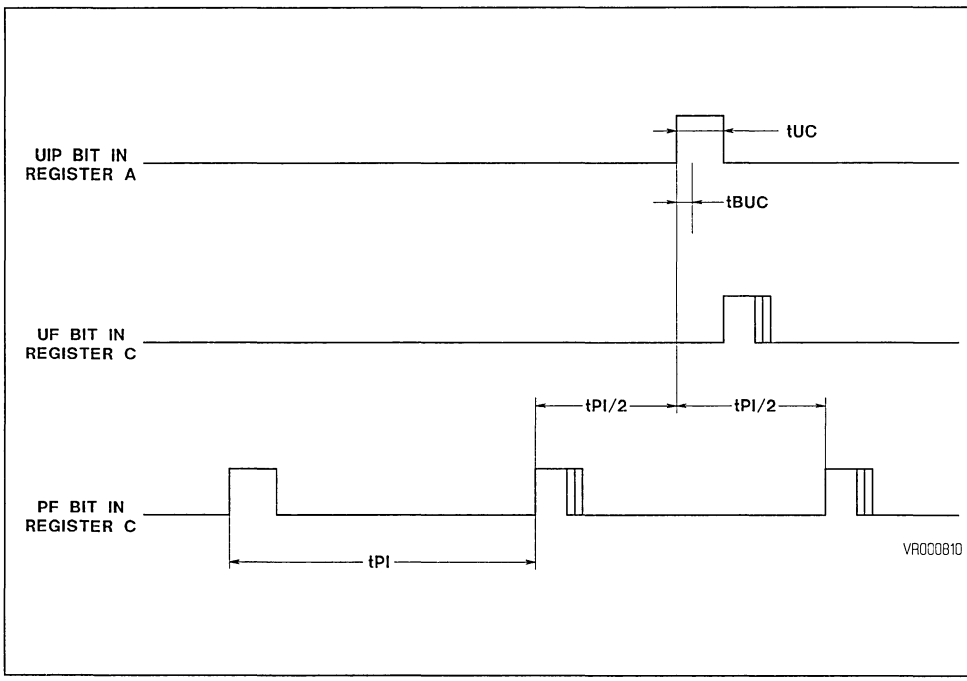
The MK48T87 executes an update cycle once per second regardless of the set bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information are consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues and alarm if a match or if a "don't care" code is present in all three positions.

There are three methods which can be employed to handle access of the Real Time Clock which avoids any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 998 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 4). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($T_{PI/2}$+t_{BUC}) to insure that data is not read during the update cycle.

Figure 4. Update Ended and Periodic Interrupt Relationship



Note : t_{PI} = Periodic Interrupt Time interval per table 1.
t_{BUC} = Delay Time Before Update Cycle = 244µs.
t_{UC} = 2ms.

REGISTERS

REGISTER A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP

The Update in Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is one, the update transfer will soon occur. When the UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a "1" inhibits any update transfer and clears the UIP status bit.

DVO, DV1, DV2

These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits which will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 1second after a pattern of 010 is written to DV0, DV1 and DV2.

RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user may do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that may be chosen with the RS bits. These four read/write bits are not affected by $\overline{\text{RESET}}$.

REGISTER B

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET

When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit which is not modified by $\overline{\text{RESET}}$ or internal functions of the MK48T87.

PIE

The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to cause the $\overline{\text{IRQ}}$ pin to be driven low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3 through RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal MK48T87 functions, but is cleared to zero on $\overline{\text{RESET}}$.

AIE

The Alarm Interrupt Enable (AIE) bit is a read/write bit which when set to a one permits the Alarm Flag (AF) bit in register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to zero. The internal functions of the MK48T87 do not affect the AIE bit.

UIE

The Update Ended Interrupt Enable (UIE) bit is a read/write bit which enables the Update End Flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears the UIE bit.

SQWE

When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. SQWE is a read/write bit.

DM

The Data Mode (DM) bit indicates whether time and calendar information are in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{\text{RESET}}$. A one in DM signifies binary data and a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is a read/write and is not affected by internal functions or $\overline{\text{RESET}}$.

DSE

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or $\overline{\text{RESET}}$.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF

The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF=PIE=1

AF=AIE=1

UF=UIE=1

i.e.,IRQF=PF•PIE+AF•AIE+UF•UIE

Any time the IRQF bit is a one the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{RESET}$ pin is low.

PF

The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are one, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{RESET}$ or a software read of Register C.

AF

A one in the AF (Alarm Interrupt Flag) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A $\overline{RESET}$ or a read of Register C will clear AF.

UF

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in the UF bit causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C or a $\overline{RESET}$.

BIT 0 THROUGH BIT 3

These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT

The Valid RAM and Time (VRT) bit is set to the one state by SGS-THOMSON prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{RESET}$.

BIT 6 THROUGH BIT 0

The remaining bits of Register D are not usable. They cannot be written and when read, they will always read zero.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_I	Voltage On Any Pin Relative to Ground	–0.3 to +7.0	V
T_A	Ambient Operating Temperature	0 to +70	°C
T_{STG}	Ambient Storage (V_{CC} off, Oscillator off) Temperature	–40 to +85	°C
P_D	Total Device Power Dissipation	1	W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATIONING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
GND	Ground	0	0	V
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3	V
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$; V_{CC} max $\leq V_{CC} \leq V_{CC}$ min)

Symbol	Parameter	Min.	Max.	Unit
I_{CC1}	Average V_{CC} Power Supply Current		15	mA
I_{MOT}	Input Current	–1	500	µA
I_{IL}	Input Leakage Current	–1	1	µA
I_{OL}	Output Leakage Current	–5	5	µA
V_{OH}	Output Logic "1" Voltage (I_{OUT} = 1.0mA)	2.4		V
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 4.0mA)		0.4	V

CAPACITANCE (T_A = 25°C)

Symbol	Parameter	Max.	Unit
C_L	Capacitance on all pins (except D/Q)	5	pF
C_{DQ}	Capacitance on DQ pins	7	pF

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 4.5V to 5.5V)

N°	Symbol	Parameter	Min.	Max.	Unit
1	t_{CYC}	Cycle Time	953	D.C.	ns
2	PW_{EL}	Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High	300		ns
3	PW_{EH}	Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low	325		ns
4	t_R, t_F	Input Rise and Fall Time		30	ns
8	t_{RWH}	R/$\overline{W}$ Hold Time	10		ns
13	t_{RWS}	R/$\overline{W}$ Set-up Time Before DS/E	80		ns
14	t_{CS}	Chip Select Set-up Time Before DS, $\overline{WR}$ or $\overline{RD}$	25		ns
15	t_{CH}	Chip Select Hold Time	0		ns
18	t_{DHR}	Read Data Hold Time	10	100	ns
21	t_{DWH}	Write Data Hold Time	0		ns
24	t_{ASL}	Muxed Address Valid Time to AS/ALE Fall	50		ns
25	t_{AHL}	Muxed Address Hold Time	20		ns
26	t_{ASD}	Delay Time DS/E to AS/ALE Fall	50		ns
27	PW_{ASH}	Pulse Width AS/ALE High	135		ns
28	t_{ASED}	Delay Time, AS/ALE to DS/E Rise	60		ns
30	t_{DDR}	Output Data Delay Time From DS/E or $\overline{RD}$	20	240	ns
31	t_{DSW}	Data Set-up Time	200		ns
32	t_{RWL}	Reset Pulse Width	5		µs
33	t_{IRDS}	$\overline{IRQ}$ Release from DS		2	µs
34	t_{IRR}	$\overline{IRQ}$ Release from $\overline{RESET}$		2	µs

Figure 5. Bus Timing for Motorola® Interface

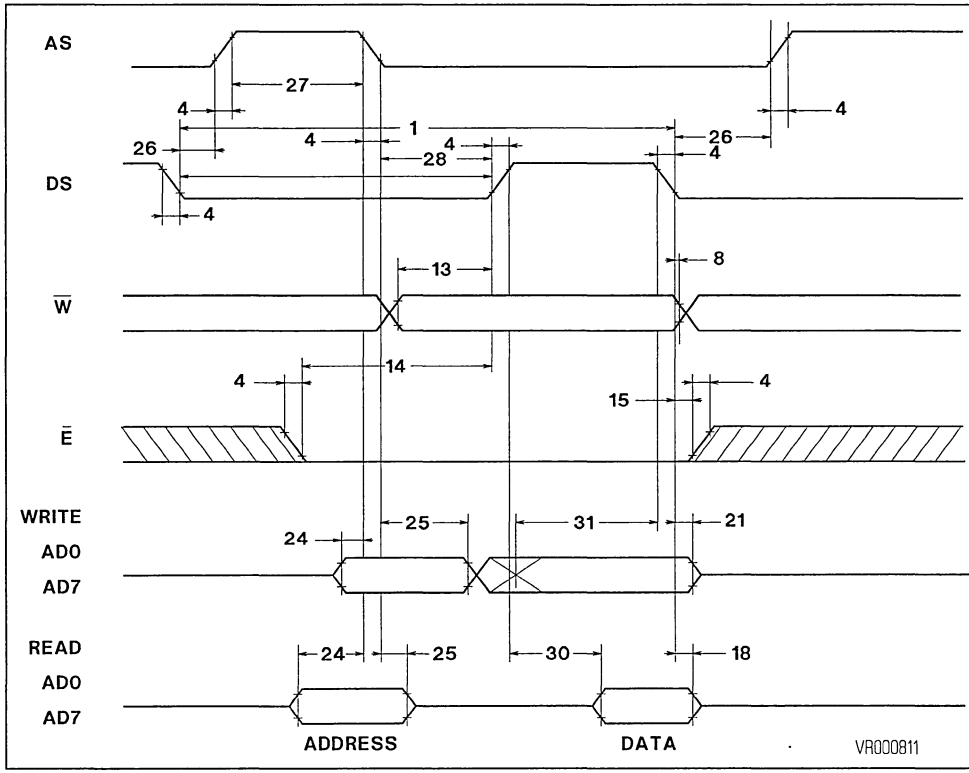


Figure 6. Bus Timing for Intel® Interface Read Cycle

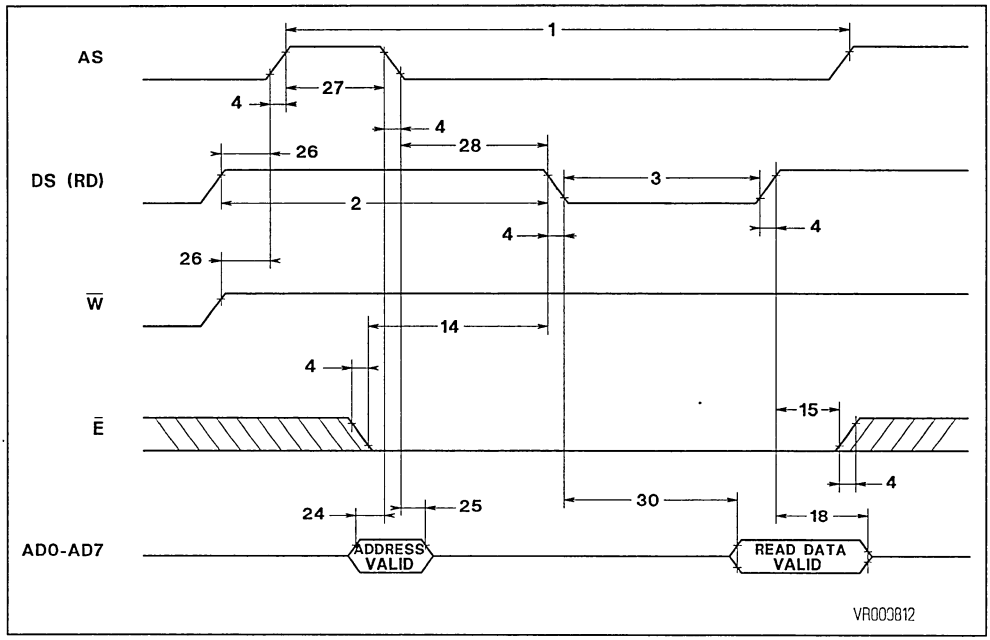


Figure 7. Bus Timing for Intel Interface Write Cycle

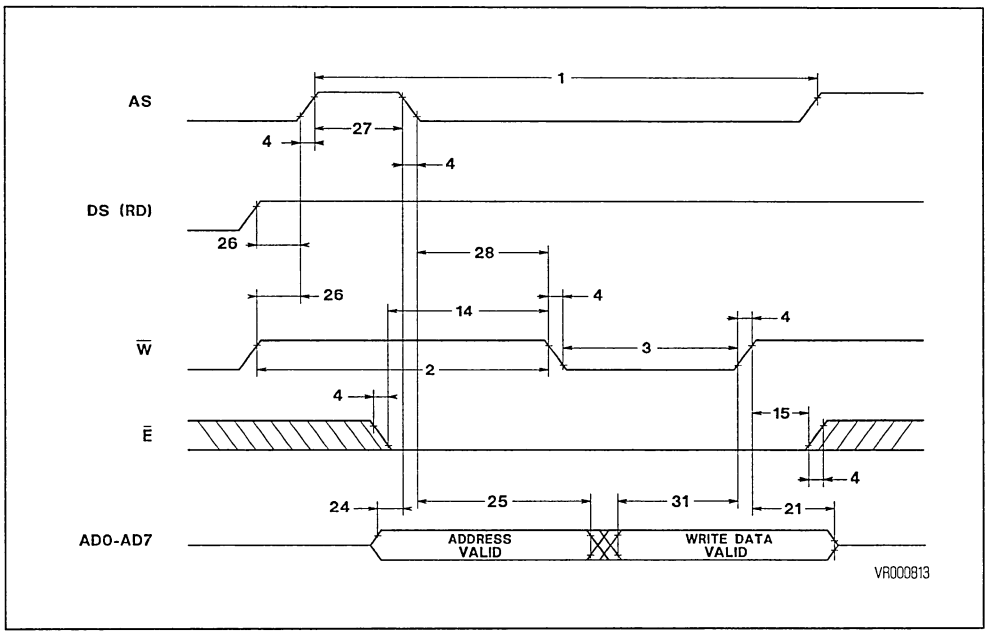


Figure 8. IRQ Release Timing

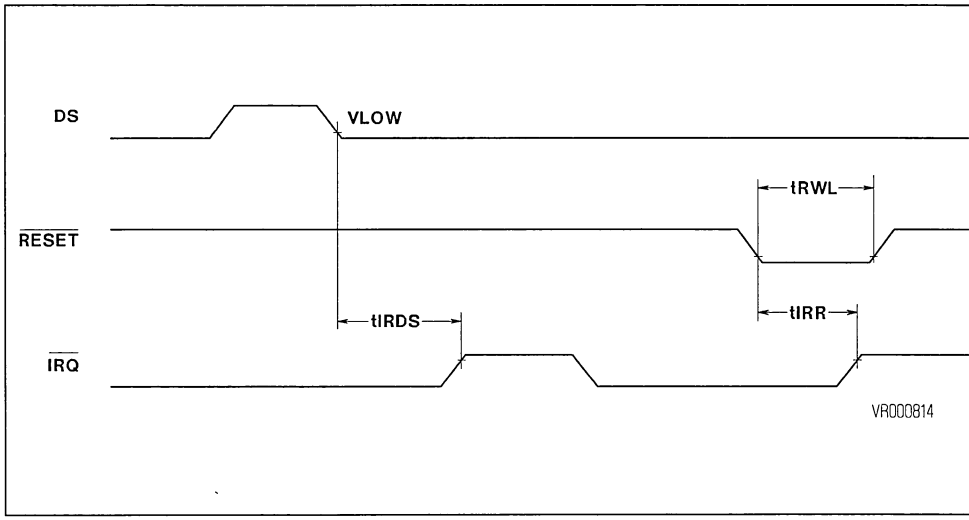
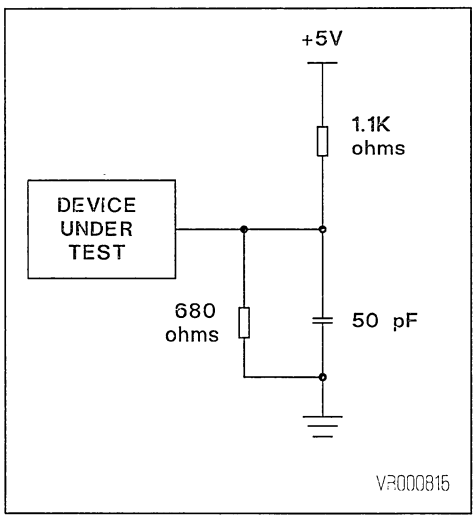


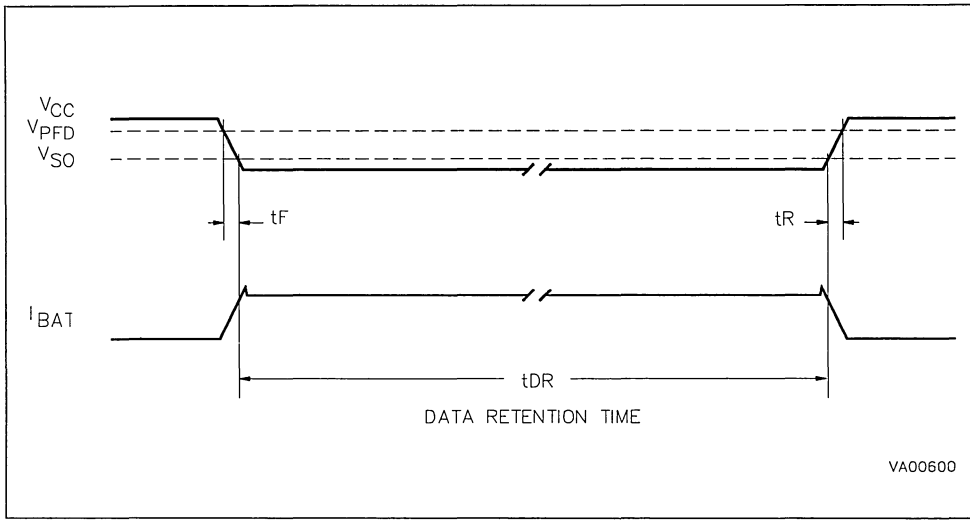
Figure 9. Output Load



Notes :

1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pull-down of 20K
4. Applies to the AD0-AD7 pins, the $\overline{IRQ}$ pin and the SQW pin when each is in the high impedance state.
5. The $\overline{IRQ}$ pin is open drain.
6. Measured with a load as shown in Figure 9.

Figure 10. Power Up/Down Conditions



AC ELECTRICAL CHARACTERISTICS (Power Up/Down Timing) ($0°C \le T_A \le 70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
t_F	V_{PFD} to V_{SO} V_{CC} Fall Time	310		µs	
t_R	V_{SO} to V_{PFD} V_{CC} Rise Time	100		µs	

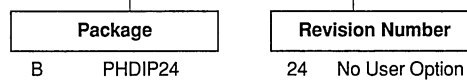
DC ELECTRICAL CHARACTERISTICS (Power Up/Down Trip Points) ($0°C \le T_A \le 70°C$)

Symbol	Parameter	Min.	Typ.	Unit	Notes
V_{PFD}	Power-Fail Deselect Voltage		4.25	V	
V_{SO}	Battery Back-up Switchover Voltage		3.2	V	
t_{DR}	Expected Data Retention Time (Oscillator on)	10		YEARS	1

Note :
1 @ 25°C.

ORDERING INFORMATION

Example: MK48T87 B 24



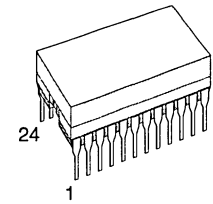
Package		Revision Number	
B	PHDIP24	24	No User Option

For a list of available options refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

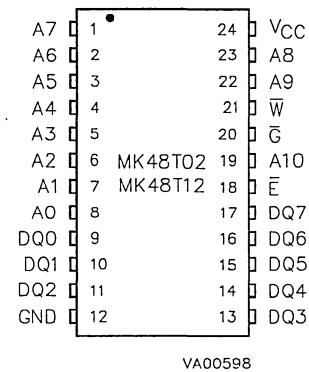
CMOS 2K x 8 TIMEKEEPER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, CRYSTAL, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- BYTEWIDE RAM-LIKE CLOCK ACCESS.
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES AND SECONDS.
- SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS.
- PREDICTED WORST CASE BATTERY STORAGE LIFE OF 11 YEARS @ 70°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 2K x 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION.
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE :
  – MK48T02 4.75V ≥ V_{PFD} ≥ 4.50V
  – MK48T12 4.50V ≥ V_{PFD} ≥ 4.20V



PHDIP24 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connection



DESCRIPTION

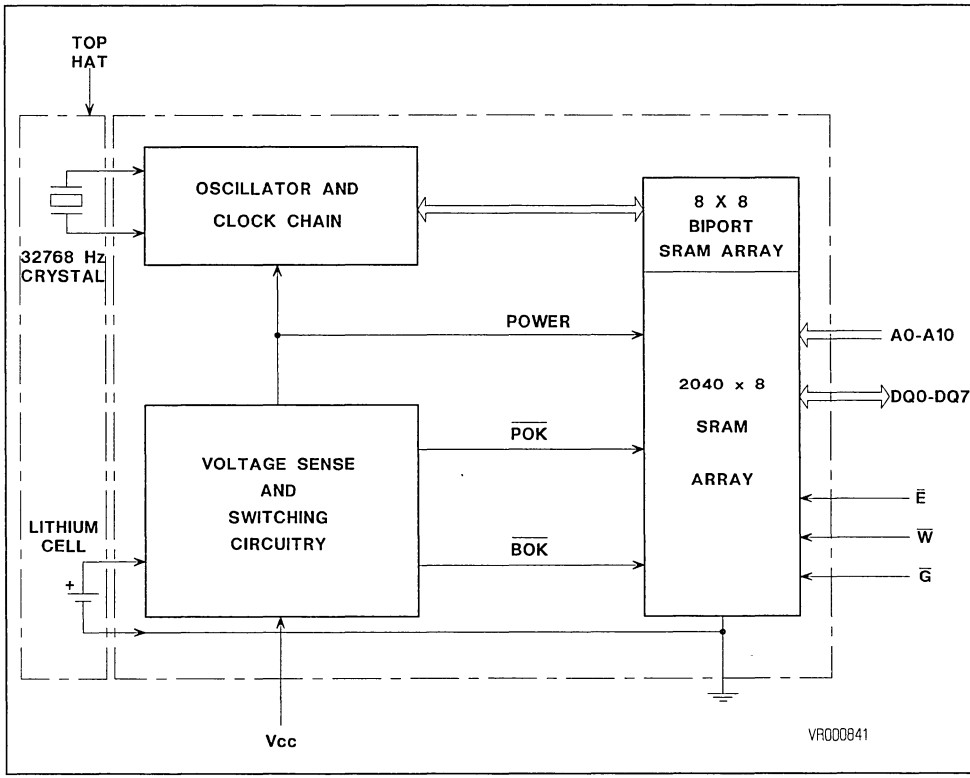
The MK48T02/12 TIMEKEEPER™ RAM combines a 2K x 8 full CMOS SRAM, a BYTEWIDE™ accessible real time clock, a crystal and a long life lithium carbon mono-fluoride battery, all in a single plastic DIP package. The MK48T02/12 is a non-volatile pin and function equivalent to any JEDEC standard 2K x 8 SRAM, such as the 6116 or 5517. It also easily fits into many EPROM AND EEPROM sockets, providing the non-volatility of the PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

Access to the clock is as simple as conventional BYTEWIDE RAM access because the RAM and the Clock are combined on the same die. As Figure 2 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top: year, month, date, day, hours, minutes, and seconds data in 24 Hour BCD format. Corrections for 28, 29 (Leap Year), 30 and 31 day months are made automatically. The eight location is a Control register. These registers are not the actual clock counters ; they are BiPORT™ read/write Static RAM memory locations. The MK48T02/12 includes a clock control circuit that, once every second, transfers the counters into the BiPORT RAM.

PIN NAMES

A0-A10	Address Inputs
$\overline{E}$	Chip Enable
GND	Ground
V_{CC}	5 Volts
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 - DQ7	Data Inputs/Outputs

Figure 2. Block Diagram



DESCRIPTION (Continued)

Because the Clock Registers are constructed using BiPORT memory cells, access to the rest of the RAM proceeds unhindered by updates to the TIMEKEEPER registers, even if the TIMEKEEPER registers are being updated at the very moment another location in the memory array is accessed.

The MK48T02/12 also has its own Power-fail detect circuit. The circuit deselects the device whenever V_{CC} is out of range, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	DQ
$<V_{CC(max)}$ $>V_{CC(min)}$	V_{IH} V_{IL} V_{IL} V_{IL}	X X V_{IL} V_{IH}	X V_{IL} V_{IH} V_{IH}	Deselect Write Read Read	High-Z D_{IN} D_{OUT} High-Z
$<V_{PFD(min)}$ $>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage On Any Pin Relative to Ground	–0.3 to +7.0	V
T_A	Ambient Operating Temperature	0 to +70	°C
T_{STG}	Ambient Storage (V_{CC} Off, Oscillator Off) Temperature	–40 to +85	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current Per Pin	20	mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION:Negative undershoots below –0.3 volts are not allowed on any pin while in Battery Back-up mode.

RECOMMENDED DC OPERATING CONDITIONS
(0°C ≤ T_A ≤ 70°C)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48T02)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48T12)	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

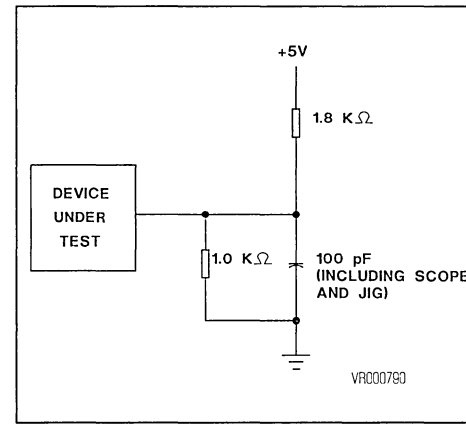
DC ELECTRICAL CHARACTERISTICS
(0°C ≤ T_A ≤ 70°C; $V_{CC\ max}$ ≥ V_{CC} ≥ $V_{CC\ min}$)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E}$ = V_{IH})		5	mA	4
I_{CC3}	CMOS Standby Current ($\overline{E}$ ≥ V_{CC} –0.2V)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	5
I_{OL}	Output Leakage Current	–5	5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –1.0mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1mA)		0.4	V	

AC TEST CONDITIONS

Input Levels	0.6V to 2.4V
Transition Times	5ns
Input and Output Timing Reference Levels	0.8V or 2.2V

EQUIVALENT OUTPUT LOAD DIAGRAM



CAPACITANCE

(T_A = 25°C)

Symbol	Parameter	Max.	Notes
C_I	Capacitance on all pins (except D/Q)	7 pF	6
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	6, 7

Notes :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with Control Bits set as follows : R = 1 ; W, ST, KS, FT = 0.
5. Measured with $V_{CC} \geq V_I \geq$ GND and outputs deselected.
6. Effective capacitance calculated from the equation C = I $\Delta t/\Delta V$ with ΔV = 3 volts and power supply at 5.0V.
7. Measured with outputs deselected.

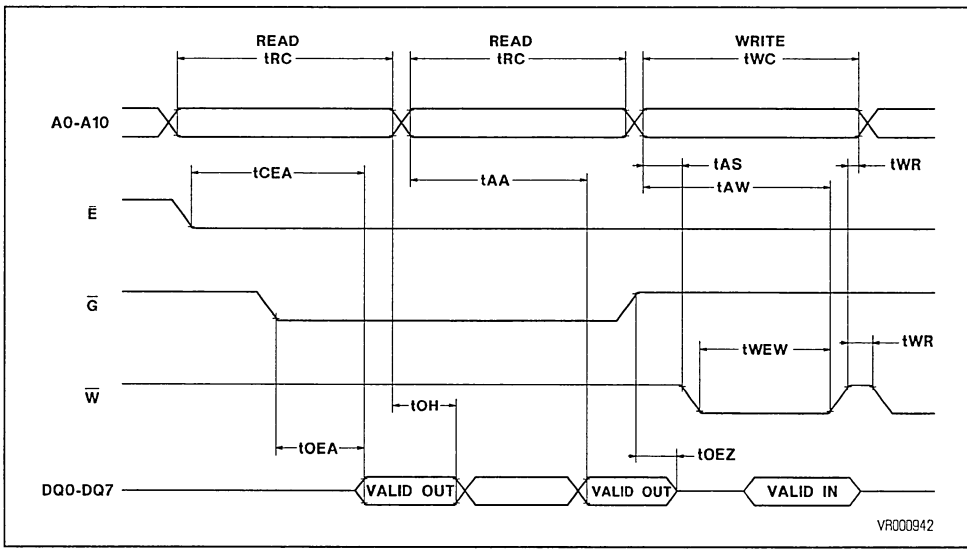
OPERATION

READ MODE

The MK48T02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access (changing Addresses without removing Chip Enable) to any of the 2048 address locations in the static storage array. Valid data will be available at the Data I/O pins within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied.

If $\overline{E}$ or $\overline{G}$ access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{CEA}) or at Output Enable Access Time (t_{OEA}). The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the Outputs are activated before t_{AA}, the data lines will be driven to an indeterminate state until t_{AA}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for Output Data Hold Time (t_{OH}) but will go indeterminant until the next t_{AA}.

Figure 3. Read-Read-Write Timing



AC ELECTRICAL CHARACTERISTICS (Read Cycle Timing)

($0°C \le T_A \le 70°C$; $V_{CC\,max} \ge V_{CC} \ge V_{CC\,min}$)

Symbol	Parameter	48T02-12		48Tx2-15		48Tx2-20		48Tx2-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		120		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		30		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		30		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		15		ns	1

Note : Measured using the Output Load Diagram shown Page 4.

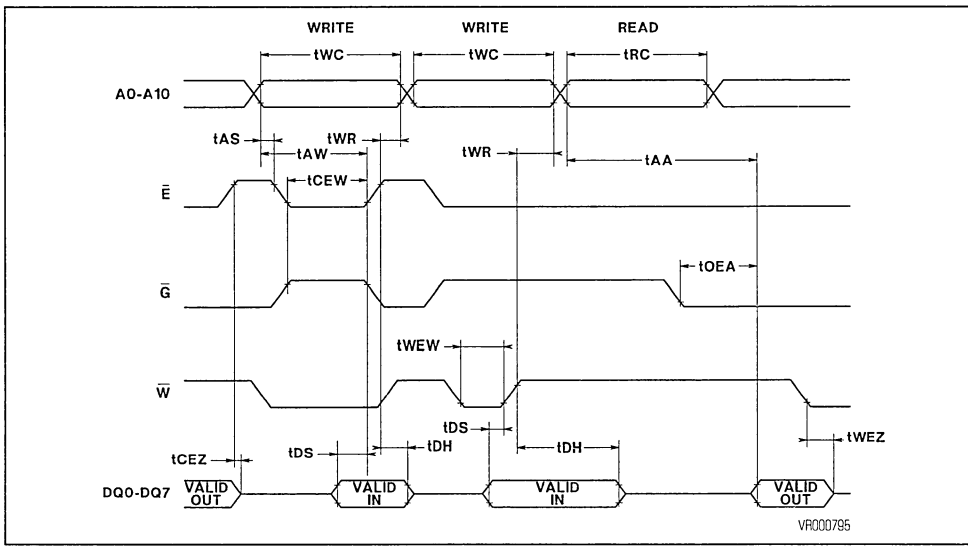
WRITE MODE

The MK48T02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterwards.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stabilizes.

The MK48T02/12 $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

Figure 4. Write-Write-Read Timing



AC ELECTRICAL CHARACTERISTICS (Write Cycle Timing)

(0°C ≤ T_A ≤ 70°C; $V_{CC\ max} \geq V_{CC} \geq V_{CC\ min}$)

Symbol	Parameter	48T02-12		48Tx2-15		48Tx2-20		48Tx2-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{AW}	Address Valid to End of Write	90		120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	75		90		120		160		ns	
t_{WEW}	Write Enable to End of Write	75		90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		10		ns	
t_{DS}	Data Setup Time	35		40		60		100		ns	
t_{DH}	Data Hold Time	5		5		5		5		ns	
t_{WEZ}	Write Enable Low to High-Z		40		50		60		80	ns	

CLOCK OPERATIONS

Reading The Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a "1" is written into the "Read" bit, the seventh most significant bit in the Control Register. As long as a "1" remains in that position, updating is halted. After a Halt is issued, the registers reflect the count, that is day, date, and time that were current at the moment the Halt command was issued. All of the TIMEKEEPER registers are updated simultaneously. A Halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a "0".

Setting The Clock

The eighth bit of the Control register is the "Write" bit. Setting the Write bit to a "1", like the Read Bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data in 24 Hour BCD format. Resetting the Write bit to a "0" then transfers those values the actual TIMEKEEPER counters and allows normal operation to resume. The KS bit, FT bit and the bits marked with zeros in Figure 5 must be written with zeros to allow normal TIMEKEEPER and RAM operation.

Calibrating The Clock

The MK48T02/12 is driven by a quartz crystal controlled oscillator with a nominal frequency of 32768 Hz. The crystal is mounted in the Top Hat along with the battery. A typical MK48T02/12 is accurate within ± 1 minute per month at 25°C without calibration. The devices are tested not to exceed ± 35ppm (Parts Per Million) oscillator frequency error at 25°C, which equates to about 1.53 minute per month. Of course the oscillation rate of any crystal changes with temperature. Figure 6 shows the frequency error that can be expected at various temperatures.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T02/12 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 7. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. The byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit, "1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have

Figure 5. The MK48T02/12 Register Map

ADDRESS	DATA								FUNCTION	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
7FF	-	-	-	-	-	-	-	-	YEAR	00-99
7FE	0	0	0	-	-	-	-	-	MONTH	01-12
7FD	0	0	-	-	-	-	-	-	DATE	01-31
7FC	0	FT	0	0	0	-	-	-	DAY	01-07
7FB	KS	0	-	-	-	-	-	-	HOURS	00-23
7FA	0	-	-	-	-	-	-	-	MINUTES	00-59
7F9	ST	-	-	-	-	-	-	-	SECONDS	00-59
7F8	W	R	S	-	-	-	-	-	CONTROL	

KEY									
	ST	=	STOP BIT	R	=	READ BIT	FT	=	FREQUENCY TEST
	W	=	WRITE BIT	S	=	SIGN BIT	KS	=	KICK START

one second either shortened or lengthened by 128 oscillator cycles, that is one tick of the divide by 256 stage. If a binary 1 is loaded into the register, only the first two minutes in the 64 minute cycle will be modified ; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding or subtracting 256 oscillator cycles for every 125,829,120 (32768 x 60 x 64) actual oscillator cycles, that is 2.034 ppm of adjustment per calibration step ; giving the user a ±63.07 ppm calibration range. Assuming that the oscillator is in fact running at exactly 32768 Hz, each of the 31 increments in the Calibration byte would represent 5.35 seconds per month, which corresponds to a total range of ± 2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given MK48T02/12 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While this may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple untility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day register, is set to a "1", and the oscillator is running at 32768 Hz, the LSB (DQ_0) of the Seconds register will toggle at a 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.00512Hz would indicate a +10 ppm (1 – (512/512.00512)) oscillator frequency error, requiring a –5 (000101_2) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency Test output frequency. The device must be selected and addresses must be stable at Address 7F9 when reading the 512 Hz on DQ_0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds register is monitored by holding the MK48T02/12 in an extended read of the Second register, without having the Read bit set. The FT bit MUST be reset to a "0" for normal clock operations to resume.

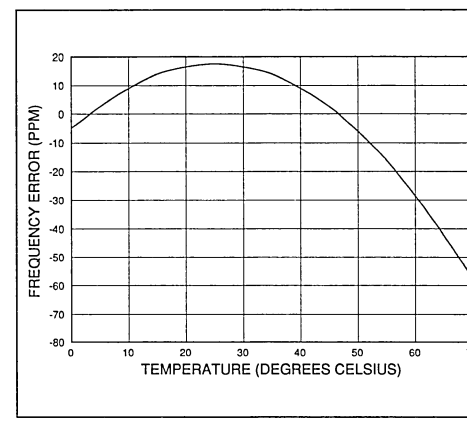
STOPPING AND STARTING THE OSCILLATOR

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain from the battery. The "Stop" bit is the MSB of the Seconds register. Setting it to a "1" stops the oscillator. In order to make the oscillator as stingy with current as possible, the oscillator is designed to require an extra "kick" to begin oscillation again. The extra kick is provided by the Kick Start (KS) bit, the MSB of the Hours register. To start the oscillator, implement the following procedure :

1. Set the Write Bit to "1".
2. Reset the Stop Bit to "0".
3. Set the Kick Start Bit to "1".
4. Reset the Write Bit to "0".
5. Wait 2 seconds.
6. Set the Write Bit to "1".
7. Reset the Kick Start Bit to "0".
8. Set the Correct time and date.
9. Reset the Write Bit to "0".

Note : Leaving the KS bit set will cause the Clock to draw excessive current and will shorten battery life.

Figure 6. Oscillator Frequency VS Temperature



DATA RETENTION MODE

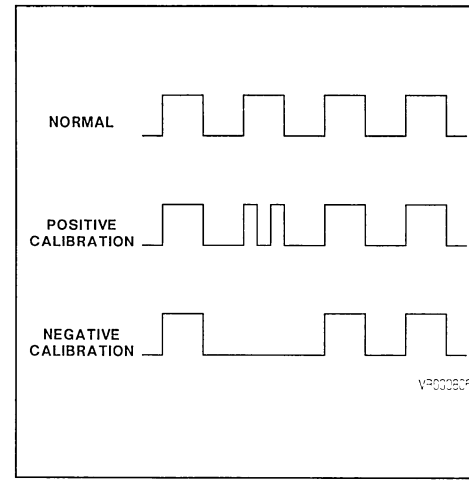
With V_{CC} applied, the MK48T02/12 operates as a conventional BYTEWIDE static RAM. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48T02 has a V_{PFD} (max) - V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48T12 has a V_{PFD} (max) - V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note : A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48T02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 9 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal $\overline{RAM}$ operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

Figure 7. Adjusting the Divide by 256 Pulse Train

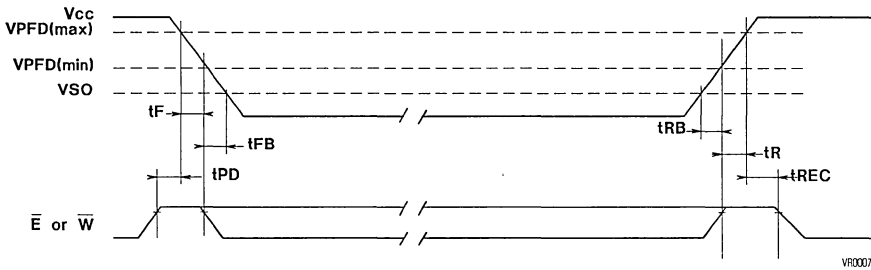


PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48T02/12 is expected to ultimately come to an end for one of two reasons : either because it has been discharged while providing current to an external load ; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption and the effects of aging, or Storage Life to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

The current drain that is responsible for Capacity Consumption can be reduced either by applying V_{CC} or turning off the oscillator. With the oscillator off, only the leakage currents required to maintain data in the RAM are flowing. With V_{CC} on, the battery is disconnected from the RAM. Because the leakage currents of the MK48T02/12 are so low, they can be neglected in practical Storage Life calculations. Therefore, application of V_{CC} or turning off the oscillator can extend the effective Back-up System life.

Figure 8. Power-Down/Power-Up Timing



DC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Trip Point Voltages)
(0°C ≤ T_A ≤ +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{PFD}	Power-Fail Deselect Voltage (MK48T02)	4.50	4.6	4.75	V	1
V_{PFD}	Power-Fail Deselect Voltage (MK48T12)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-Up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Timing)
(0°C ≤ T_A ≤ +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0			ns	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300			µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10			µs	3
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1			µs	
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0			µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2			ms	

Notes :

1. All voltages referenced to GND.
2. V_{PFD} (max) to V_{PFD} (min) fall times of less t_F may result in deselection/write protection not occurring until 50µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data or stop the clock.

PREDICTING STORAGE LIFE

Figure 10 illustrates how temperature affects Storage Life of the MK48T02/12 battery. As long as V_{CC} is applied or the oscillator is turned off, the life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48T02/12.

Storage Life predictions presented in Figure 10 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K ohm load resistance.

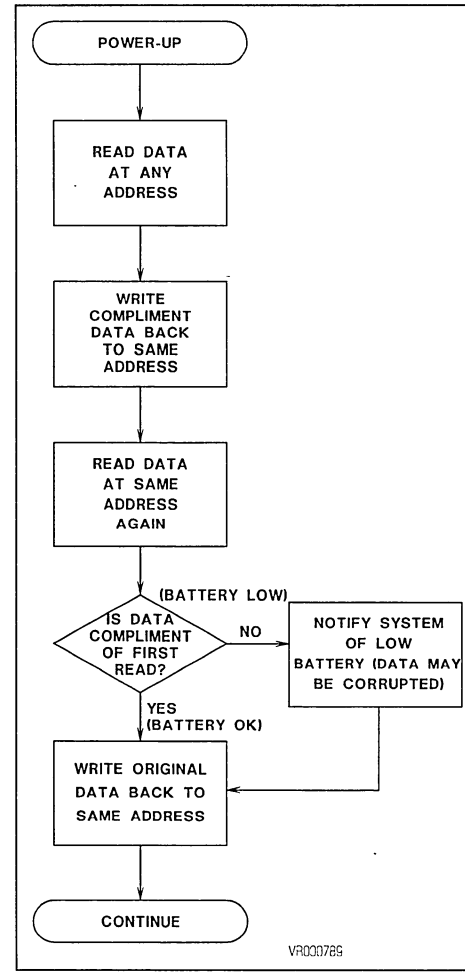
A Special Note : The summary presented in Figure 10 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final ; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 10. They are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 10 indicates that a particular MK48T02/12 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years ; 50% of them can be expected to fail within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The t50% figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48T02/12 is marked with a nine digit manufacturing data code in the form H99XXYYZZ, example: H995B9231 is H - fabricated in Carrollton, TX; 9 - assembled in Muar, Malaysia; 9 - tested in Muar, Malaysia; 5B - lot designator; 9231 - assembled in the year 1992, work week 31.

Figure 9. Checking the $\overline{BOK}$ Flag Status



CALCULATING PREDICTED STORAGE LIFE OF THE BATTERY

As Figure 10 indicates, the predicted Storage Life of the battery in the MK48T02/12 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 10. If the MK48T02/12 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

$$\text{Predicted Storage Life} = \frac{1}{[(TA_1/TT)/SL_1] + [(TA_2/TT)/SL_2] + \ldots + [(TA_n/TT)/SL_n]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

SL_1, SL_2, SL_n = Predicted Storage Life at Temp 1, Temp 2, etc. (See Figure 10).

EXAMPLE PREDICTED STORAGE LIFE CALCULATION

A cash register/terminal operates in an environment where the MK48T02/12 is exposed to temperatures of 30°C (86°F) or less for 4672 hrs/yr ; temperatures greater than 25°C, but less than 40°C (104°F), for 3650 hrs/yr ; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

Reading predicted $t_{1\%}$ values from Figure 10 ; SL_1 = 456 yrs., SL_2 = 175 yrs., SL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 4672 hrs./yr. TA_2 = 3650 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Storage} \geq \frac{1}{[(4672/8760)/456] + [(3650/8760)/175] + [(438/8760)/11.4]}$$

$$\geq 126 \text{ yrs}$$

PREDICTING CAPACITY CONSUMPTION LIFE

The MK48T02/12 internal cell has a nominal capacity of 39mAh. The device places a nominal combined RAM and TIMEKEEPER load of 1.2µA on the internal battery when the clock is running and the device is in Battery Back-up mode. At that rate, the MK48T02/12 will consume the cell's capacity in 32,500 hours, or about 3.7 years. But, as Figure 11 shows, Capacity Consumption can be spread over a much longer period of time.

Naturally, Back-up current varies with temperature. As Figure 12 indicates, the rate of Current Consumption by the MK48T02/12 with the clock running in Battery Back-up mode is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate consumption rates in a given design. As long as ambient temperature is held reasonably constant, expected Capacity Consumption life can be estimated by reading 0% V_{CC} Duty Cycle Capacity Consumption life directly from Figure 12, and dividing by the expected V_{CC} Duty Cycle (i.e. at 25°C with a 66% Duty Cycle, Capacity Consumption Life = 3.7/(1-.66) = 10.9 years).

If the MK48T02/12 spends an appreciable amount of time at a variety of temperatures, the same equation provided in the previous Storage Life section should be used to estimate Capacity Consumption life.

Example consumption life calculation

Taking the same cash register/terminal used earlier, let's assume that the high and low temperature periods are the non-operating, Battery Back-up mode periods, and that the register is turned on 10 hours a day seven days per week. The two points of interest on the curves in Figure 12 will be the 25°C and the 70°C points.

Reading Capacity Life values from Figure 12 ; CL_1 = 3.7 yrs., CL_2 = 3.96 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 4672 hrs./yr. TA_2 = 438 hrs./yr.

$$\text{Capacity Life} \geq \frac{1}{[(4672/8760)/3.7] + [(438/8760)/3.96]}$$

$$\geq 6.38 \text{ yrs.}$$

ESTIMATING BACK-UP SYSTEM LIFE

The procedure for estimating Back-up System Life is simple. Pick the lower of the two numbers. In the case calculated in the examples, that would be 6.38 years. The fact is, since either mechanism, Storage Life or Capacity Consumption, can end the system's life, the end is marked by whichever occurs first.

Figure 11. Typical Capacity Consumption Life at 25°C VS. V_{CC} Duty Cycle

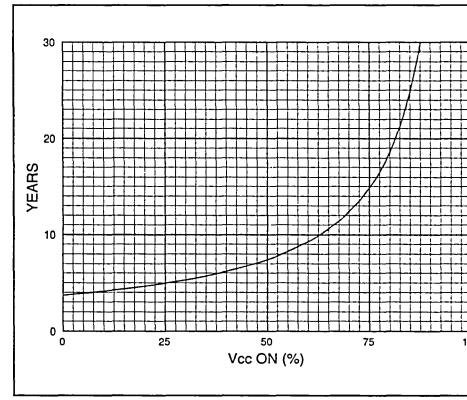


Figure 10. Predicted Battery Storage Life Versus Temperature

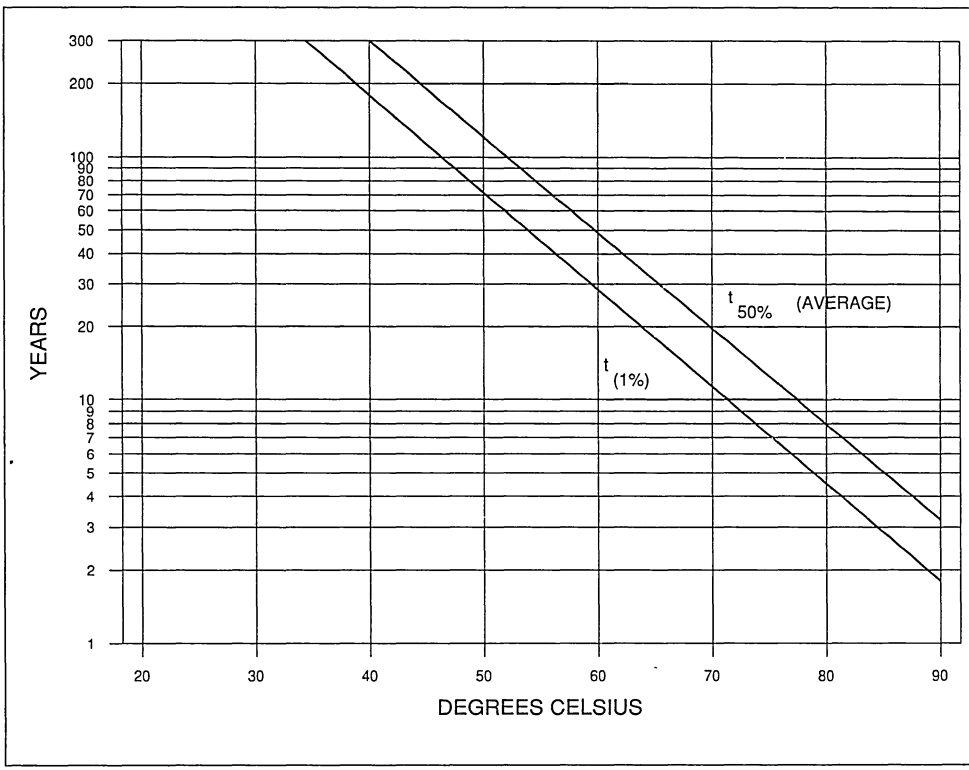
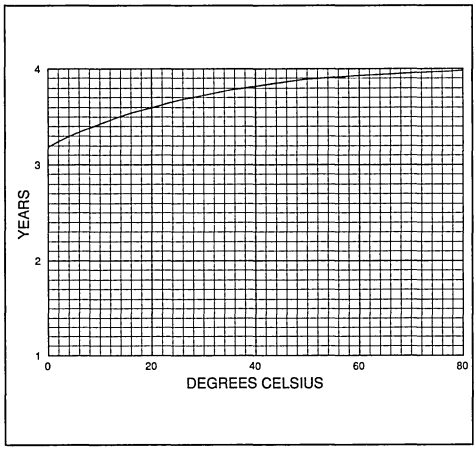


Figure 12. Current Consumption Life over Temperature with 0% V_{CC} Duty Cycle



APPLICATION NOTE :

BINARY TO BCD, AND BCD TO BINARY CONVERSION

The MK48T02/12 presents and accepts TIMEKEEPER data in BCD format. Conversion to or from other formats can be executed in a single line of code, as the following example BASIC program demonstrates.

```
10  REM  BINARY TO BCD
20  DEF  FNA (X) = INT (X/10)*16+X-INT
         (X/10)*10
30  REM  BCD TO BINARY
40  DEF  FNB (X) = INT (X/16)
         *10+(XAND15)
```

ORDERING INFORMATION

Example: MK48T02 B 12

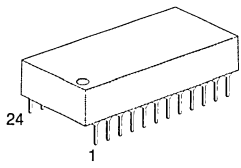
Package		Speed	
B	PHDIP24	12	120ns
		15	150ns
		20	200ns
		25	250ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

CMOS 2K x 8 TIMEKEEPER SRAM

- PIN and FUNCTION COMPATIBLE with the MK48T02,12
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- 10 YEARS of DATA RETENTION and CLOCK OPERATION in the ABSENCE of POWER
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48T02: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48T12: 4.2V ≤ V_{PFD} ≤ 4.5V



PCDIP24 (PC)
Battery CAPHAT

DESCRIPTION

The M48T02,12 TIMEKEEPER™ RAM is a 2K x 8 non-volatile static RAM and real time clock which is pin and function compatible with the MK48T02,12.

A special 24 pin 600mil DIP CAPHAT™ package houses the M48T02,12 silicon with a quartz crystal and a long life lithium button cell to form a highly integrated battery backed-up memory and real time clock solution.

Figure 1. Logic Diagram

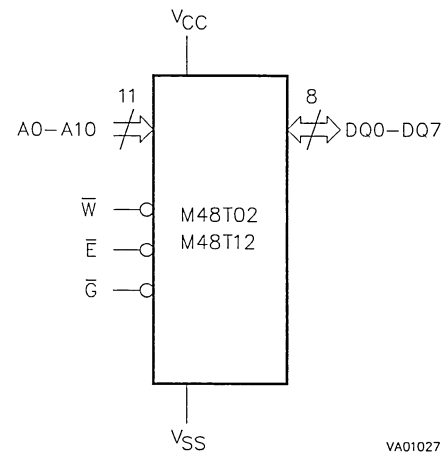
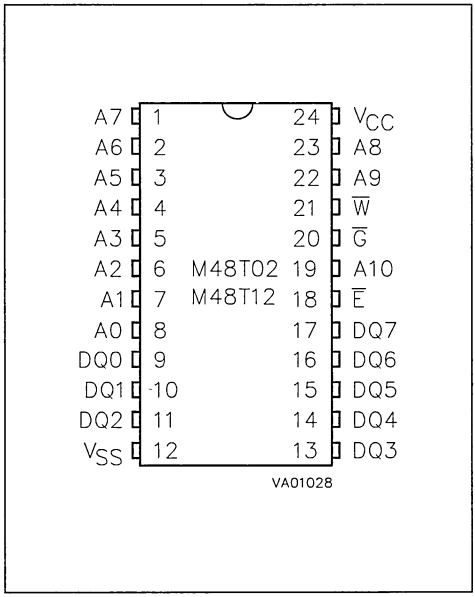


Table 1. Signal Names

A0-A10	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

The M48T02,12 button cell has enough capacity to maintain data and clock functionality for an accumulated time period of at least 10 years in the absence of power at room temperature.

For a complete description of electrical characteristics and bus timing, refer to the MK48T02,12 data sheet.

ORDERING INFORMATION SCHEME

Example: M48T02 -120 PC 1

Supply Voltage and Write Protect Voltage

02 V_{CC} = 4.75V to 5.5V
V_{PFD} = 4.5V to 4.75V

12 V_{CC} = 4.5V to 5.5V
V_{PFD} = 4.2V to 4.5V

Speed

-120 120ns

-150 150ns

Package

PC PCDIP24

Temp. Range

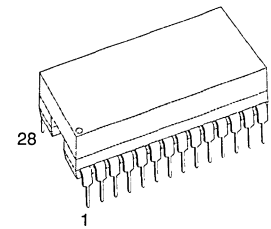
1 0 to 70 °C

For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 8K x 8 TIMEKEEPER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, CRYSTAL, POWER-FAIL CONTROL CIRCUIT and BATTERY
- BYTEWIDE RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS
- CLOCK ACCURACY of ± 1 MINUTE a MONTH, @ 25°C
- SOFTWARE CONTROLLED CLOCK CALIBRATION for HIGH ACCURACY APPLICATIONS
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 8K x 8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - MK48T08: 4.5V ≤ V_{PFD} ≤ 4.75V
  - MK48T18: 4.2V ≤ V_{PFD} ≤ 4.5V



PHDIP28 (B)
Battery TOPHAT

Figure 1. Logic Diagram

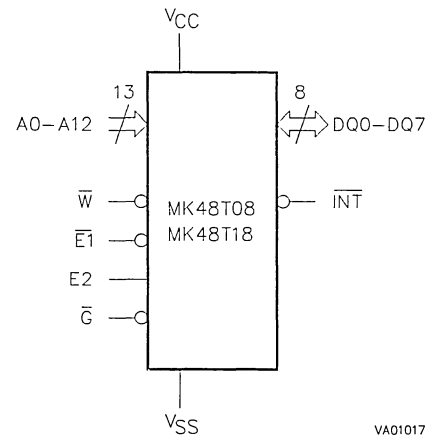


Table 1. Signal Names

A0 - A12	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{INT}$	Power Fail Interrupt
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

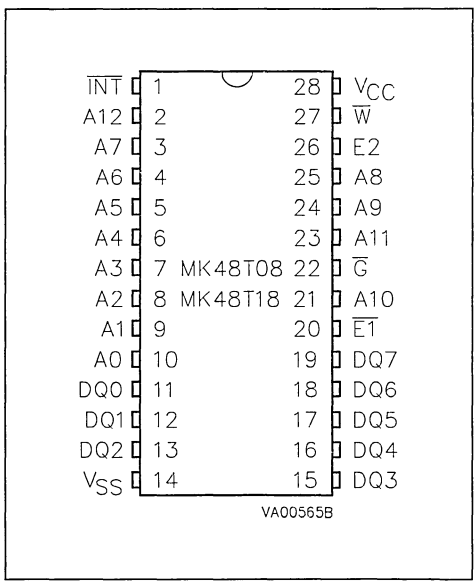
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	X	High Z	Standby
Deselect		X	V_{IL}	X	X	High Z	Standby
Write		V_{IL}	V_{IH}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections

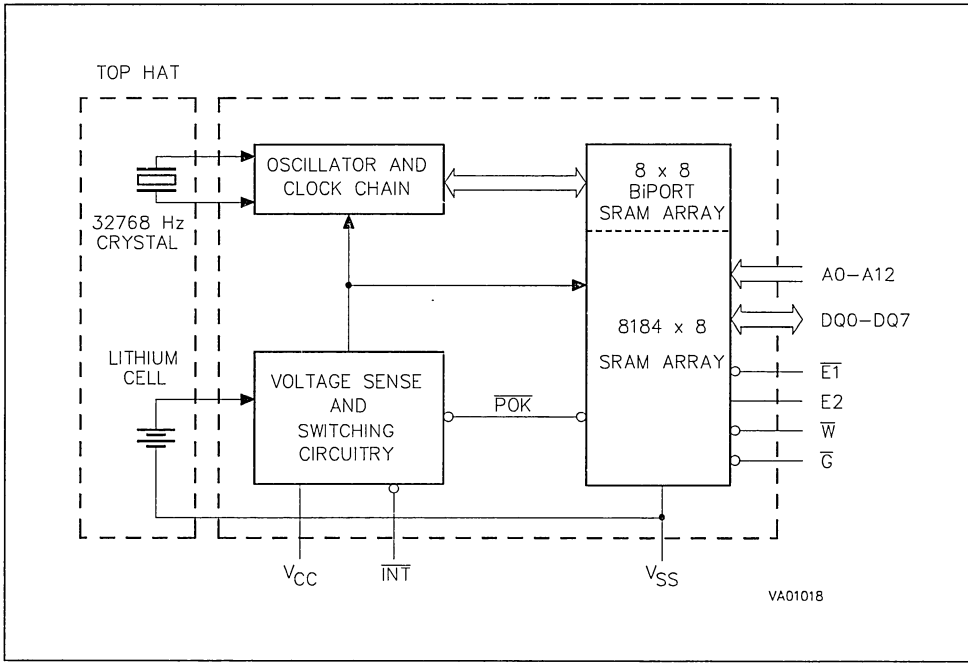


DESCRIPTION

The MK48T08/18 TIMEKEEPER™ RAM is an 8K x 8 non-volatile Static RAM and real time clock. A special 28 pin 600 mil dual-in- line plastic package houses the MK48T08/18 silicon with a quartz crystal and a long life button cell battery to form a highly integrated battery backed-up memory and real time clock solution. The MK48T08/18 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the MK48T08/18 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF8h-1FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register.

Figure 3. Block Diagram



DESCRIPTION (cont'd)

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The MK48T08/18 includes a clock control circuit which updates the clock bytes with current information once a second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The MK48T08/18 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

READ MODE

The MK48T08/18 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E1}$ (Chip Enable 1) is low, and E2 (Chip Enable 2) is high. The device architecture allows ripple- through access of data from eight of 65,536 locations in the static storage array.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

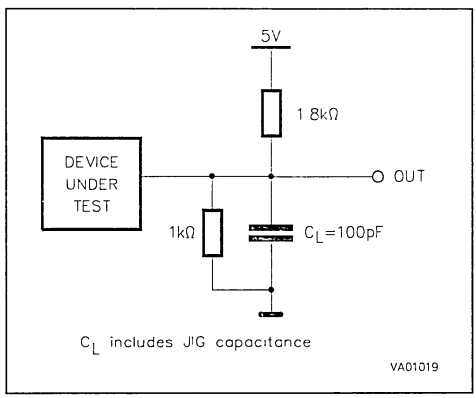


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (2)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation C = IΔt/ΔV with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1} (2)	Supply Current (Standby) TTL	$\overline{E1}$ = V_{IH}, E2 = V_{IL}		3	mA
I_{CC2} (2,3)	Supply Current (Standby) CMOS	$\overline{E1}$ = V_{CC} – 0.2V, E2 = V_{SS} + 0.2V		3	mA
V_{IL} (4)	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
	Output Low Voltage ($\overline{INT}$)	I_{OL} = 0.5mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselect.
2 Measured with Control Bits set as follows: R = '1'; W, ST, FT = '0'.
3 Typical value = 1mA.
4. Negative spikes of –1V allowed for up to 10ns once per Cycle.

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (MK48T08)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (MK48T18)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} (2)	Expected Data Retention Time	10			YEARS

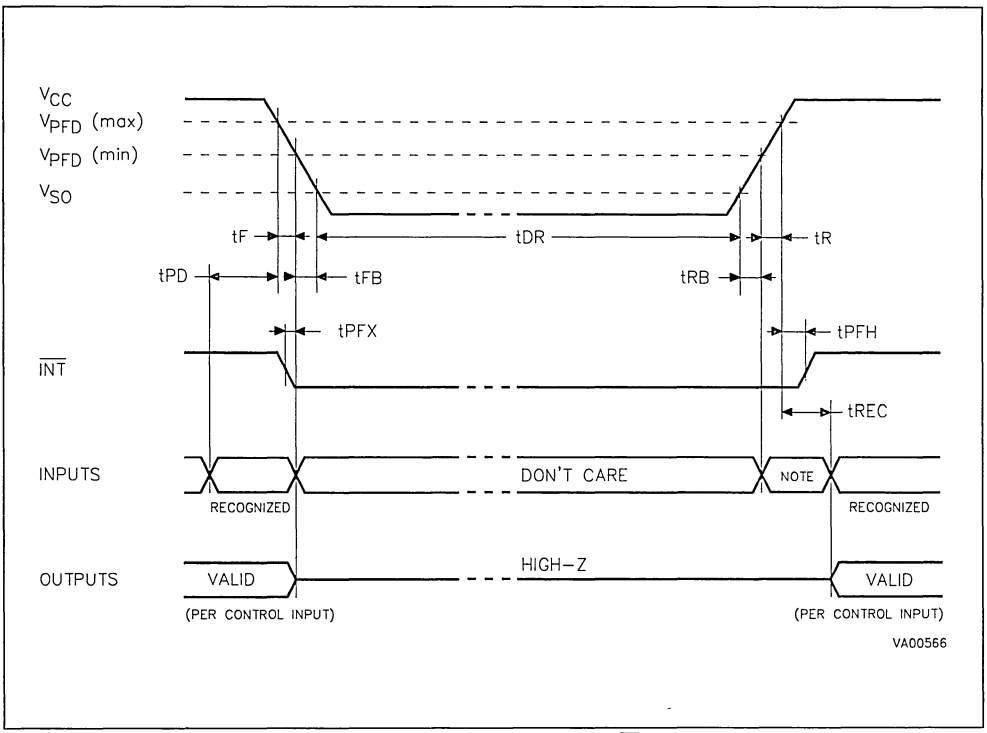
Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} after Power Up	1		ms
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs
t_{PFH} (3)	V_{PFD} (max) to $\overline{INT}$ High		120	µs

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min)
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data
3. $\overline{INT}$ may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

Figure 5. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E1}$ high or E2 low as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	MK48T08 / 18				Unit
		10		15		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	100		150		ns
t_{AVQV}	Address Valid to Output Valid		100		150	ns
t_{E1LQV}	Chip Enable 1 Low to Output Valid		100		150	ns
t_{E2HQV}	Chip Enable 2 High to Output Valid		100		150	ns
t_{GLQV}	Output Enable Low to Output Valid		50		75	ns
t_{E1LQX}	Chip Enable 1 Low to Output Transition	10		10		ns
t_{E2HQX}	Chip Enable 2 High to Output Transition	10		10		ns
t_{GLQX}	Output Enable Low to Output Transition	5		5		ns
t_{E1HQZ}	Chip Enable 1 High to Output Hi-Z		50		75	ns
t_{E2LQZ}	Chip Enable 2 Low to Output Hi-Z		50		75	ns
t_{GHQZ}	Output Enable High to Output Hi-Z		40		60	ns
t_{AXQX}	Address Transition to Output Transition	5		5		ns

Figure 6. Read Mode AC Waveforms

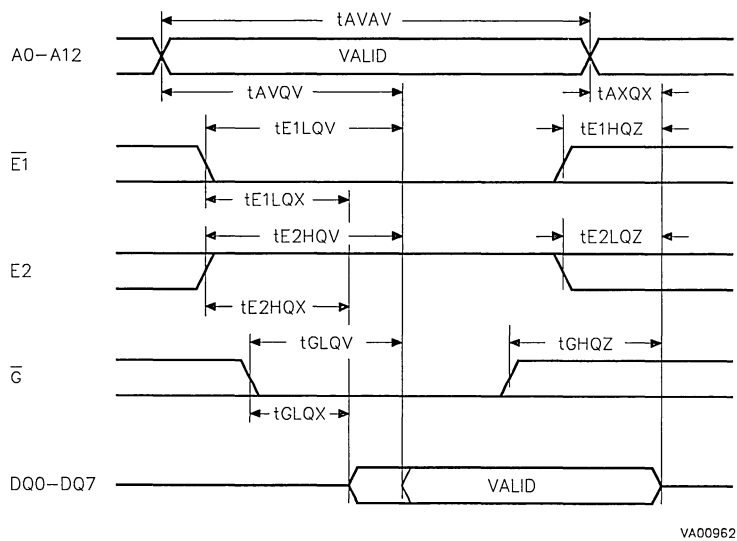


Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	MK48T08/18				Unit
		10		15		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	100		150		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		0		ns
t_{WLWH}	Write Enable Pulse Width	80		100		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	80		130		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	80		130		ns
t_{WHAX}	Write Enable High to Address Transition	10		10		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	10		10		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	10		10		ns
t_{DVWH}	Input Valid to Write Enable High	50		70		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	50		70		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	50		70		ns
t_{WHDX}	Write Enable High to Input Transition	5		5		ns
t_{E1HDX}	Chip Enable 1 High to Input Transition	5		5		ns
t_{E2LDX}	Chip Enable 2 Low to Input Transition	5		5		ns
t_{WLQZ}	Write Enable Low to Output Hi-Z		50		70	ns
t_{AVWH}	Address Valid to Write Enable High	80		130		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	80		130		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	80		130		ns
t_{WHQX}	Write Enable High to Output Transition	10		10		ns

Figure 7. Write Enable Controlled, Write AC Waveforms

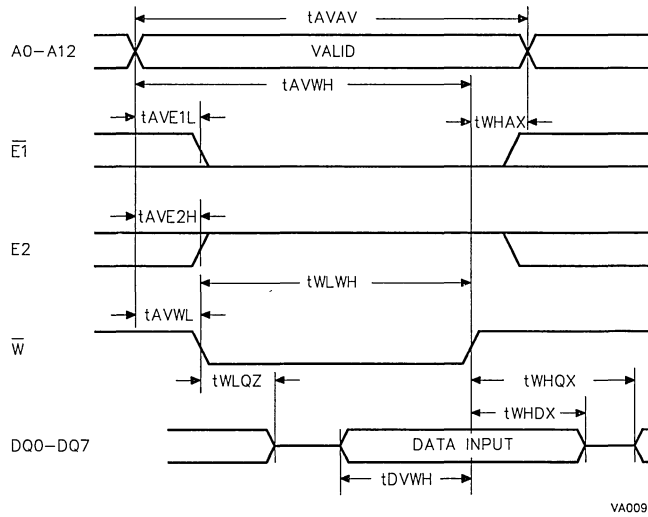
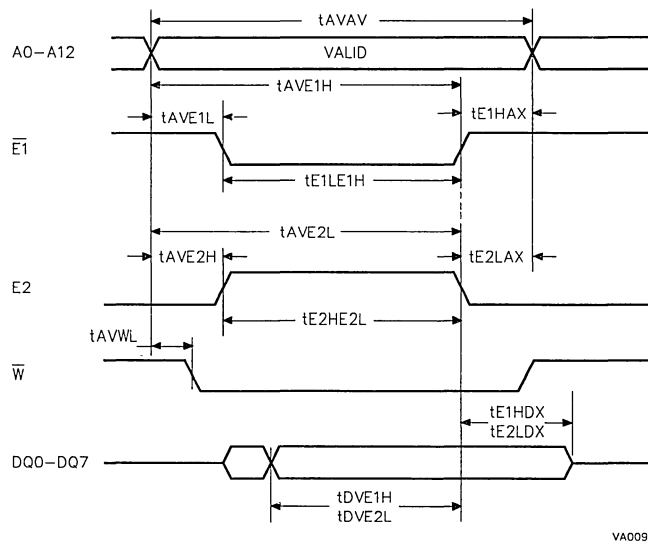


Figure 8. Chip Enable Controlled, Write AC Waveforms



READ MODE (cont'd)

Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E1}$, E2, and $\overline{G}$ access times are also satisfied. If the $\overline{E1}$, E2 and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t_{E1LQV} or t_{E2HQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E1}$, E2 and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E1}$, E2 and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The MK48T08/18 is in the Write Mode whenever $\overline{W}$, $\overline{E1}$, and E2 are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E1}$, or the rising edge of E2. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E1}$, or the falling edge of E2. The addresses must be held valid throughout the cycle. $\overline{E1}$ or $\overline{W}$ must return high or E2 low for minimum of t_{E1HAX} or t_{E2LAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E1}$ and $\overline{G}$ and a high on E2, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the MK48T08/18 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The MK48T08/18 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the MK48T08/18 for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD}(min). $\overline{E1}$ should be kept high or E2 low as V_{CC} rises past V_{PFD}(min) to prevent inadvertent write cycles prior to processor stabilization. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

POWER FAIL INTERRUPT PIN

The MK48T08/18 continuously monitors V_{CC}. When V_{CC} falls to the power-fail detect trip point, an interrupt is immediately generated. An internal clock provides a delay of between 10µs and 40µs before automatically deselected the MK48T08/18. The $\overline{INT}$ pin is an open drain output and requires an external pull up resistor, even if the interrupt output function is not being used.

SYSTEM BATTERY LIFE

The useful life of the battery in the MK48T08/18 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to the RAM and clock in the battery back-up mode, or because the effects of aging render the cell useless before it can actually be completely discharged. The two effects are virtually unrelated allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms. The earlier occurring failure mechanism defines the battery system life of the MK48T08/18.

Cell Storage Life

Storage life is primarily a function of temperature. Figure 9 illustrates the approximate storage life of the MK48T08/18 battery over temperature. The results in Figure 9 are derived from temperature accelerated life test studies performed at SGS-THOMSON. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4V closed circuit voltage across a 250 kΩ load resistor. The two lines, $t_{1\%}$ and $t_{50\%}$, represent different failure rate distributions for the cell's storage life. At 70°C, for example, the $t_{1\%}$ line indicates that an MK48T08/18 has a 1% chance of having a battery failure 11 years into its life while the $t_{50\%}$ shows the part has a 50% chance

SYSTEM BATTERY LIFE (cont'd)

of failure at the 20 year mark. The $t_{1\%}$ line represents the practical onset of wear out and can be considered the worst case Storage Life for the cell. The $t_{50\%}$ can be considered the normal or average life.

Calculating Storage Life

The following formula can be used to predict storage life:

$$\frac{1}{\{[(TA1/TT)/SL1]+[(TA2/TT)/SL2]+...+[(TAN/TT)/SLN]\}}$$

where,

- TA1, TA2, TAN = time at ambient temperature 1, 2, etc.
- TT = total time = TA1+TA2+...+TAN
- SL1, SL2, SLN = storage life at temperature 1, 2, etc.

For example an MK48T08/18 is exposed to temperatures of 55°C or less for 8322 hrs/yr, and temperatures greater than 60°C but less than 70°C for the remaining 438 hrs/yr. Reading predicted $t_{1\%}$ values from Figure 9,

- SL1 = 41 yrs, SL2 = 11.4 yrs
- TT = 8760 hrs/yr
- TA1 = 8322 hrs/yr, TA2 = 438 hrs/yr

Predicted storage life ≥

$$\frac{1}{\{[(8322/8760)/41]+[(431/8760)/11.4]\}}$$

or 36 years.

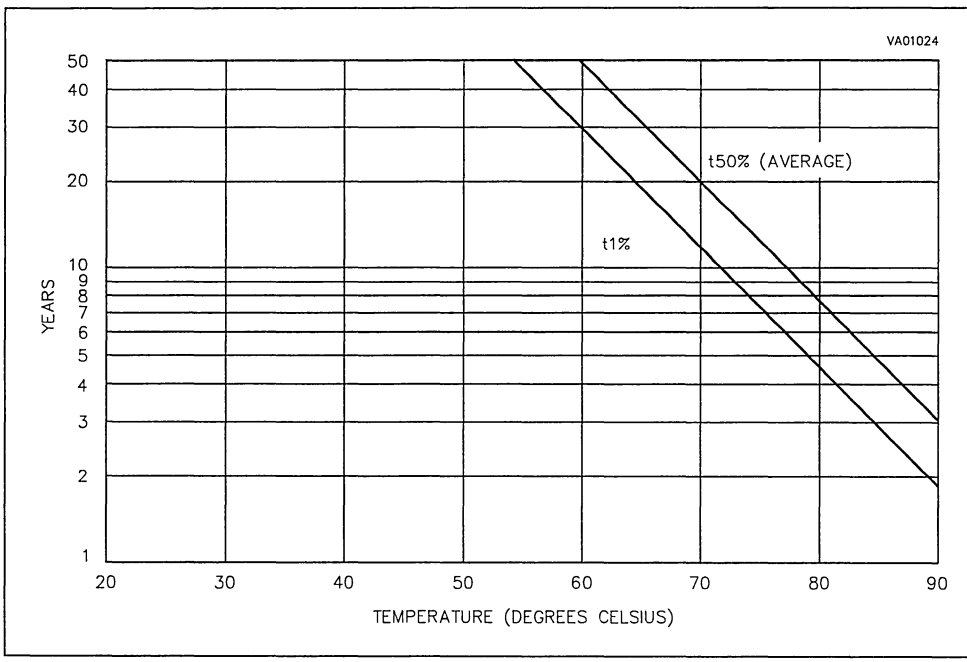
Cell Capacity Life

The MK48T08/18 internal cell has a rated capacity of 39mAh. The device places a nominal RAM and TIMEKEEPER load of less than 445nA at room temperature. At this rate, the capacity consumption life is 39E-3/445E-9 = 87,640 hours or about 10 years. Capacity consumption life can be extended by applying V_{CC} or turning off the clock oscillator prior to system power down.

Calculating Capacity Life

The RAM and TIMEKEEPER load remains relatively constant over the operating temperature range. Thus, worst case cell capacity life is essentially a function of one variable, V_{CC} duty cycle. For

Figure 9. Predicted Battery Storage Life versus Temperature



example, if the oscillator runs 100% of the time with V_{CC} applied 60% of the time, the capacity consumption life is 10/(1-0.6), or 25 years.

Estimated System Life

Since either storage life or capacity consumption can end the battery's life, the system life is marked by which ever occurs first. In the above example, this would be 25 years.

Reference for System Life

Each MK48T08/18 is marked with a nine digit manufacturing date code in the form of H99XXYYZZ. For example, H995B9231 is:

- H = fabricated in Carrollton, TX
- 9 = assembled in Muar, Malaysia,
- 9 = tested in Muar, Malaysia,
- 5B = lot designator,
- 9231 = assembled in the year 1992, work week 31.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, the seventh bit in the control register. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Setting the Clock

The eighth bit of the control register is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10). Resetting the WRITE bit to a '0' then transfers those values to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in Table 10 must be written to '0' to allow for normal TIMEKEEPER and RAM operation.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The MK48T08/18 is shipped from SGS-THOMSON with the STOP bit set to a '1'. When reset to a '0', the MK48T08/18 oscillator starts within 1 second.

Table 10. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFFh									Year	00-99
1FFEh	0	0	0						Month	01-12
1FFDh	0	0							Date	01-31
1FFCh	0	FT	0	0	0				Day	01-07
1FFBh	0	0							Hour	00-23
1FFAh	0								Minutes	00-59
1FF9h	ST								Seconds	00-59
1FF8h	W	R	S						Control	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit (Set to '0' for normal clock operation)
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be written to '0'

Calibrating the Clock

The MK48T08/18 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The crystal is mounted in the tophat along with the battery. A typical MK48T08/18 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 11 shows the frequency error that can be expected at various temperatures. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T08/18 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 11. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given MK48T08/18 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register, is set to a '1', and the oscillator is running at 32,768 Hz, the LSB (DQ0) of the Seconds Register will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency. The device must be selected and addresses must stable at Address 1FF9h when reading the 512 Hz on DQ0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds Register is monitored by holding the MK48T08/18 in an extended read of the Seconds Register, without having the Read bit set. The FT bit MUST be reset to '0' for normal clock operations to resume.

Figure 10. Clock Calibration

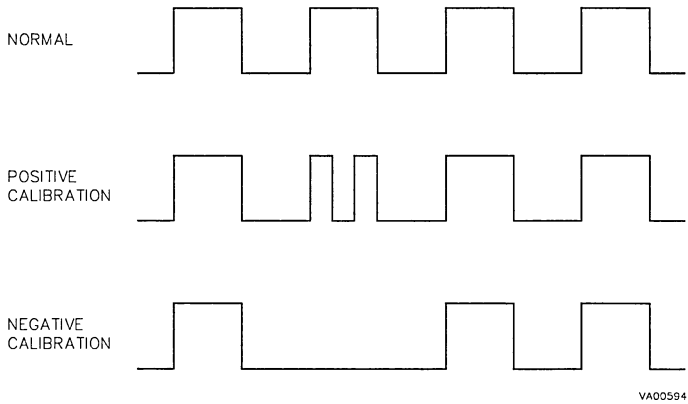
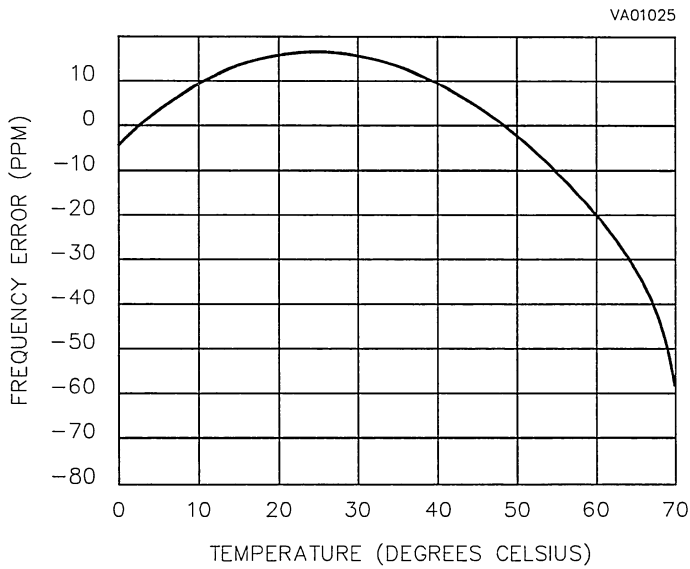
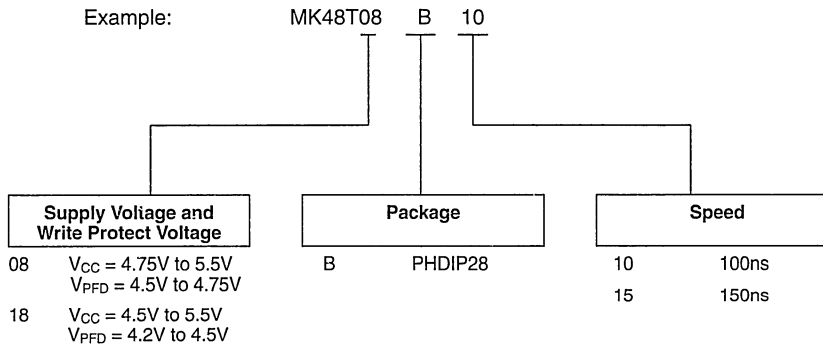


Figure 11. Crystal Frequency Error



ORDERING INFORMATION SCHEME

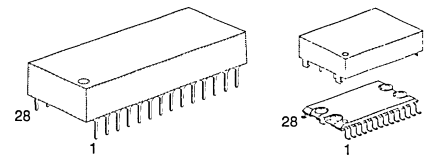


For a list of available options (Package and Speed) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information or any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

CMOS 8K x 8 TIMEKEEPER SRAM

- PIN and FUNCTION COMPATIBLE with the MK48T08,18
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY and CRYSTAL
- SNAPHAT HOUSING (BATTERY and CRYSTAL) REPLACEABLE
- 10 YEARS of DATA RETENTION and CLOCK OPERATION in the ABSENCE of POWER



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

DESCRIPTION

The M48T08,18 TIMEKEEPER™ RAM is an 8K x 8 non-volatile static RAM and real time clock which is pin and functional compatible with the MK48T08,18. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory and real time clock solution.

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{INT}$	Power Fail Interrupt
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

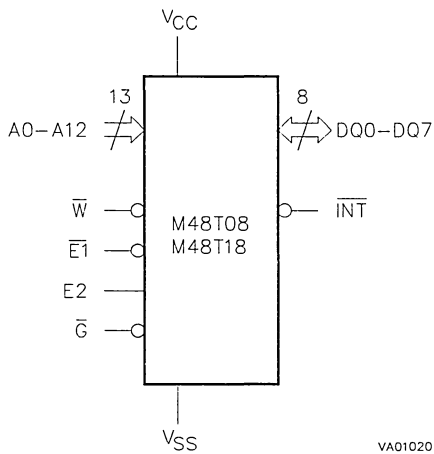


Figure 2A. DIP Pin Connections

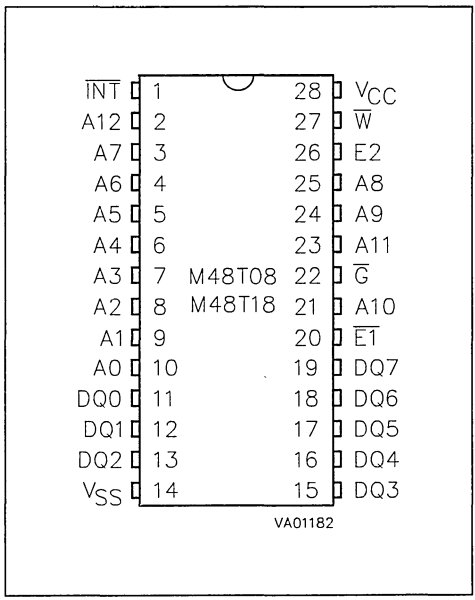
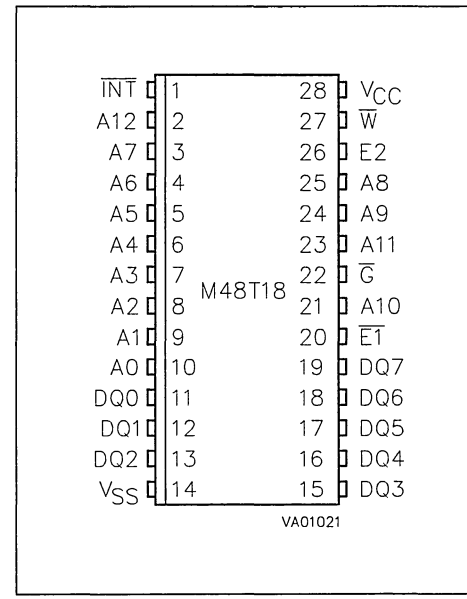


Figure 2B. SO Pin Connections



DESCRIPTION (cont'd)

The 28 pin 600mil DIP CAPHAT™ houses the M48T08,18 silicon with a quartz crystal and a long life lithium button cell in a single package.

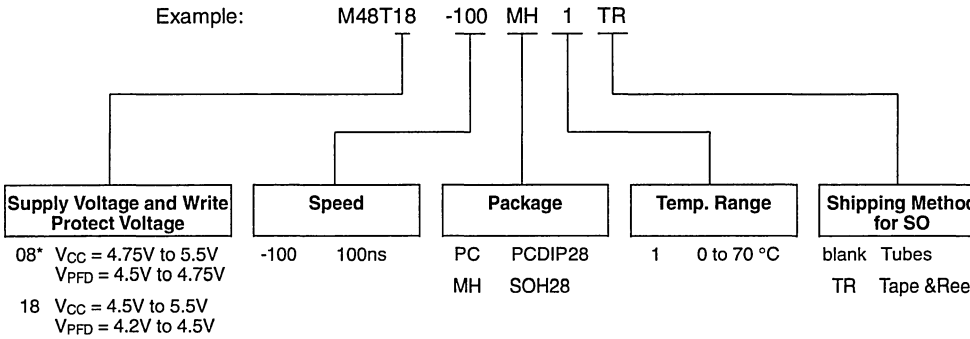
The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery package are shipped separately in plastic anti-static tubes. The SO is also available to ship in Tape & Reel form. For the M48T18, the battery package part number is "M4T28-BR12SH1".

The ordering information scheme shows the part number for the CAPHAT DIP and the SNAPHAT SOIC. For a complete description of electrical characteristics and bus timing, refer to the MK48T08,18 data sheet.

ORDERING INFORMATION SCHEME



Note: 08* CAPHAT package only.

For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

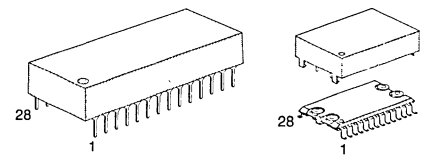
SGS-THOMSON MICROELECTRONICS

M48T58

CMOS 8K x 8 TIMEKEEPER SRAM

- INTEGRATED LOW POWER SRAM, REAL TIME CLOCK, and POWER-FAIL CONTROL CIRCUIT
- CLOCK CALIBRATED at FACTORY for HIGH ACCURACY
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- DIRECT CONNECTION for a SNAPHAT BATTERY/CRYSTAL PACKAGE on the SO PACKAGE
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS with BYTWIDE RAM-LIKE ACCESS
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- FREQENCY TEST OUTPUT for REAL TIME CLOCK

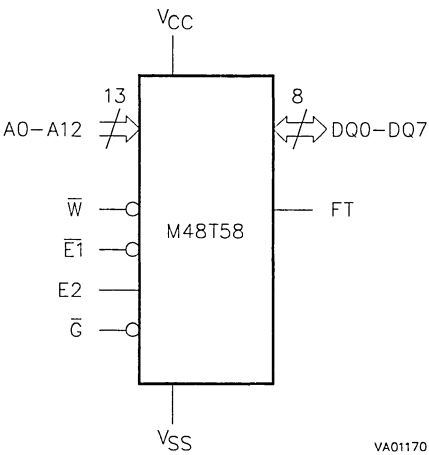
PRODUCT CONCEPT



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

Figure 1. Logic Diagram



DESCRIPTION

The M48T58 TIMEKEEPER™ RAM is an 8K x 8 non volatile static RAM and real time clock. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory and real time clock solution.

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
FT	Frequency Test Output
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

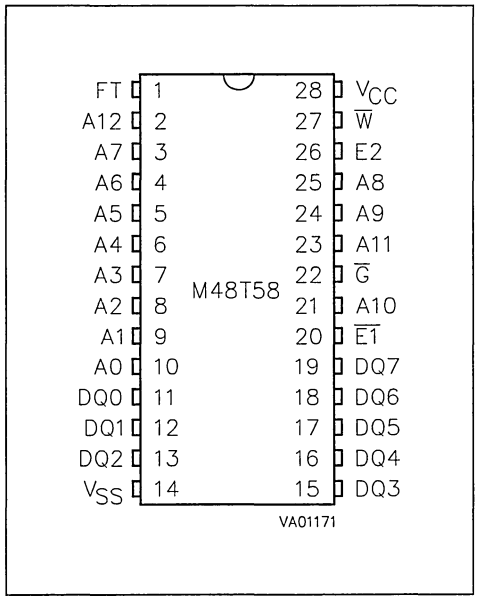
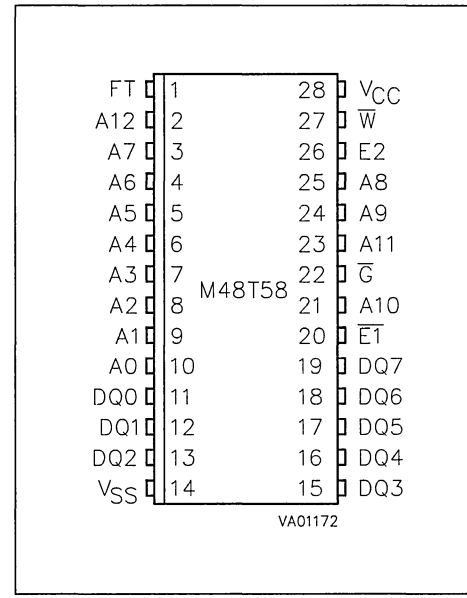


Figure 2B. SO Pin Connections



DESCRIPTION (cont'd)

The 28 pin 600mil CAPHAT™ DIP houses the M48T58 silicon with a quartz crystal and a long life lithium button cell in a single package. The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The M48T58 is functional equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The static memory array and the quartz controlled clock oscillator of the M48T58 are integrated on one silicon chip. The two circuits are interconnected at the upper seven memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF9h-1FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register. This byte controls user clock access and stores the digital clock calibration setting.

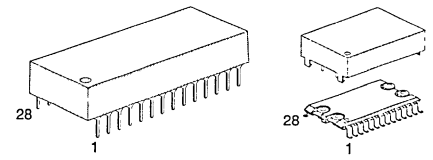
The clock related bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T58 includ es a clock control circuit which updates the clock bytes with current information once a second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T58 also has its own power-fail detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

CMOS 8K x 8 TIMEKEEPER SRAM

PRODUCT CONCEPT

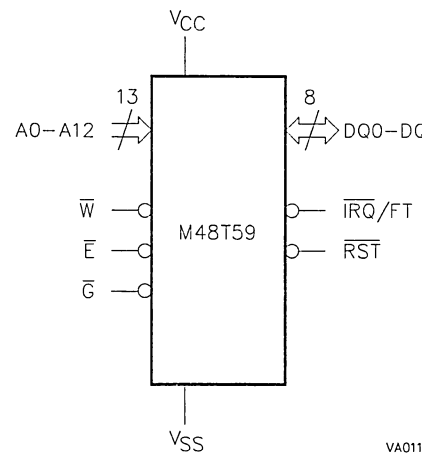
- INTEGRATED LOW POWER SRAM, REAL TIME CLOCK, and POWER-FAIL CONTROL CIRCUIT
- CLOCK CALIBRATED at FACTORY for HIGH ACCURACY
- MICROPROCESSOR POWER-ON RESET (VALID all the WAY to $V_{CC} = V_{SS}$)
- PROGRAMMABLE WATCHDOG OUTPUT
- PROGRAMMABLE ALARM OUTPUT ACTIVE in the BATTERY BACK-UP MODE
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- DIRECT CONNECTIONS for a SNAPHAT BATTERY/CRYSTAL PACKAGE on the SO PACKAGE
- BATTERY LOW WARNING



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

Figure 1. Logic Diagram



DESCRIPTION

The M48T59 TIMEKEEPER™ RAM is an 8K x 8 non volatile static RAM and real time clock. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory and real time clock solution.

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{RST}$	Reset
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{IRQ}$/FT	Interrupt / Frequency Test Output
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

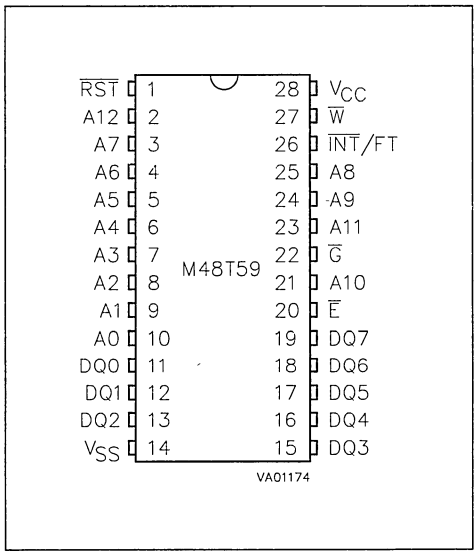
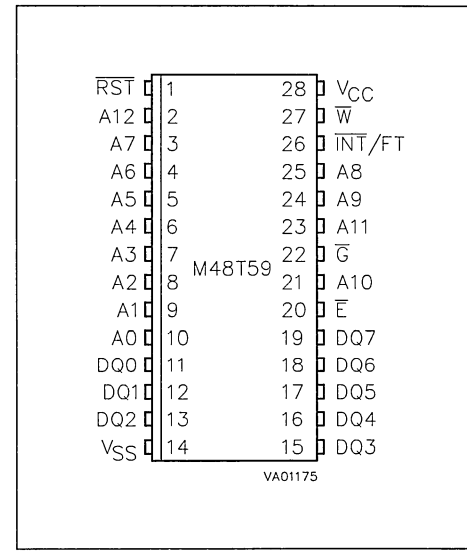


Figure 2B. SO Pin Connections



DESCRIPTION (cont'd)

The 28 pin 600mil DIP CAPHAT™ houses the M48T59 silicon with a quartz crystal and a long life lithium button cell in a single package. The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The M48T59 is functional equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The static memory array and the quartz controlled clock oscillator of the M48T59 are integrated on one silicon chip. The two circuits are interconnected at the upper seven memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF9h-1FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register. This byte controls user clock access and stores the digital clock calibration setting. Byte 1FF7h contains the watchdog timer setting. Bytes 1FF5h-1FF2h are reserved for clock alarm programming.

The clock related bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T59 includes a clock control circuit which updates the clock bytes with current information once a second. The information can be accessed by the user in the same manner as any other location in the static memory array.

A power-on reset output provides a reset pulse to the microprocessor. It pulls low (open drain) on power-down and remains low on power-up for 40ms to 200ms after V_{CC} passes V_{PFD}. The reset pulse remains active with V_{CC} at V_{SS}.

The M48T59 also has its own power-fail detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

SMARTCARD PRODUCTS

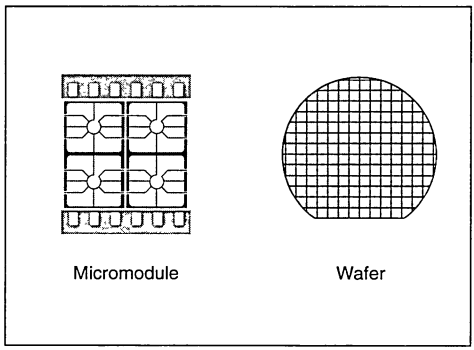
SGS-THOMSON MICROELECTRONICS

ST1305

HIGH ENDURANCE CMOS 192 bit EEPROM WITH SECURE LOGIC ACCESS CONTROL

ADVANCE DATA

- SINGLE 5V SUPPLY VOLTAGE
- PROGRAMMING TIME: 5 ms
- MEMORY DIVIDED INTO:
  - 24 bits of Chip Data
  - 40 bits of Application Data
  - 48 bits of Count Data
  - 12 extra-bits of Transport Code
  - 64 bits of Issuer Data
- COUNTING CAPABILITY up to 262,144 UNITS
- CIRCUIT PROTECTED by TRANSPORT CODE for DELIVERY from SGS-THOMSON to the CUSTOMER
- 5 EXTERNAL CONTACTS ONLY (ISO 7816 COMPATIBLE)
- ANSWER to RESET FULLY COMPATIBLE with ISO 7816-3
- E.S.D. GREATER THAN 4000V
- POWER-ON and LOW V_{CC} RESET



DESCRIPTION

The ST1305 is a 192 bits EEPROM memory with associated security logic to control memory access. The circuit includes counting capabilities and thus is very well adapted to prepaid card applications.

The ST1305 is protected by hardwired security logic and special fuses. The memory is a matrix of 24 x 8 cells accessed bit by bit for reading and programming, and by byte for internal erasing in final application.

Figure 1. Logic Diagram

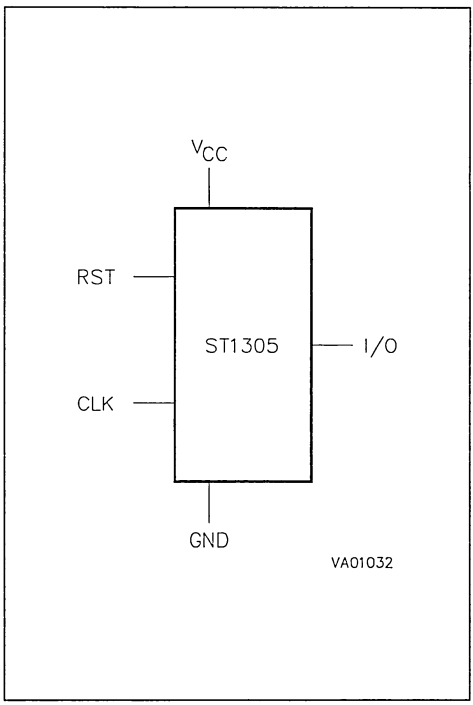


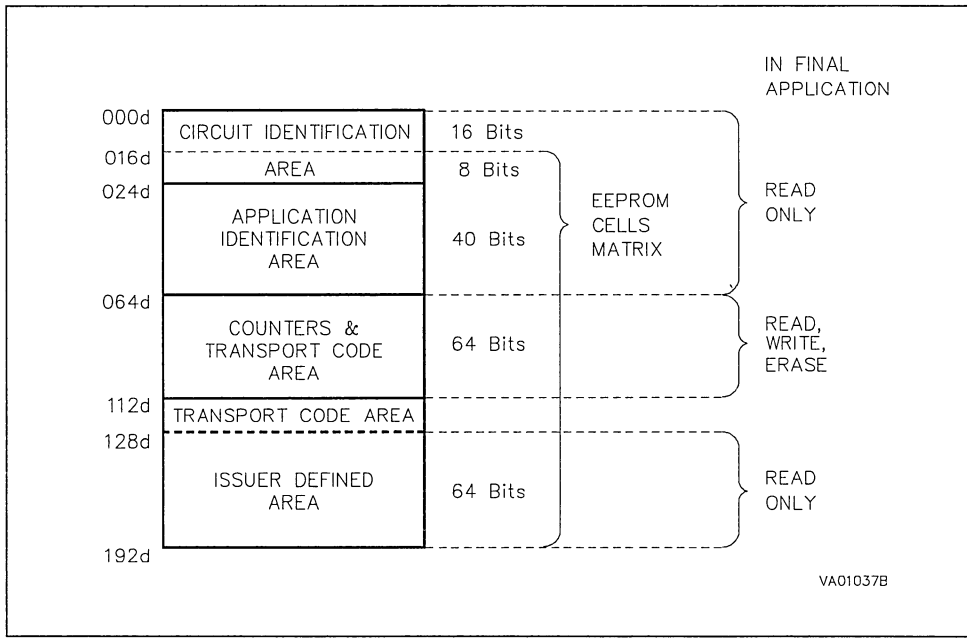
Table 1. Signal Names

CLK	Clock
RST	Reset
I/O	Data Input / Output
V_{CC}	Supply Voltage
GND	Ground

INTERNAL ADDRESS MAPPING

The internal address space of the ST1305 is divided into five zones as shown in Figure 2. These zones are the actual EEPROM memory array. The Transport Code or Counter area is used in two configurations: In the ISSUER configuration it is used to store the Transport Code loaded by SGS-THOMSON for security during delivery to the card issuer; in the USER configuration it is used as a serie of counters.

Figure 2. Memory Map



SGS-THOMSON MICROELECTRONICS

ST1331
ST1336

SMARTCARD CMOS 272 bit EEPROMs

ADVANCE DATA

- SINGLE 5V SUPPLY VOLTAGE
- PROGRAMMING TIME < 5 ms
- MEMORY DIVIDED INTO:
  - 16 bits of Chip Identification Data
  - 48 bits of Card Identification Data
  - up to 40 bits of Counter
  - 16 bits for Valorisation Certificate
  - 64 bits for Issuer Defined Data
  - 32 bits for Anti-Tearing Flags
  - 56 bits of User/Issuer Defined Data
- COUNTING CAPABILITY up to 32,768 (8^5) UNITS
- CIRCUIT PROTECTED by TRANSPORT CODE for DELIVERY from SGS-THOMSON to the CUSTOMER
- CERTIFICATE for CARD VALORISATION
- SPECIAL ANTI-TEARING MECHANISM
- 2 COMMUNICATION PROTOCOLS POSSIBLE
  - 6 Contacts for ST1331
  - 5 Contacts for ST1336
- ANSWER to RESET COMPATIBLE with ISO 7816-3
- E.S.D. GREATER THAN 4000V
- POWER-ON, LOW and HIGH V_{CC} RESET
- ST1336 COMPATIBLE with ST1305 or EQUIVALENT

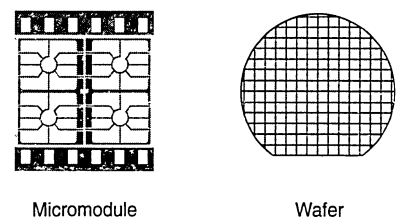


Figure 1. Logic Diagram

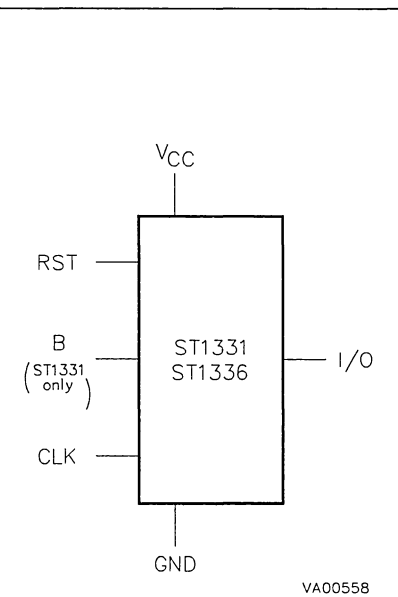


Table 1. Signal Names

CLK	Clock
RST	Function Code for ST1331
	Reset for ST1336
B	Function Code (ST1331 only)
I/O	Data Input / Output
V_{CC}	Supply Voltage
GND	Ground

DESCRIPTION

The ST1331 and ST1336 are 272 bits EEPROM memories protected by hard wired security logic and special fuses. The memory is a matrix of 34 x 8 cells, accessed bit by bit for reading and programming, and by byte for internal erasing in final application.

A valorisation certificate is implemented in the memory and allows the recognition of the circuit by the appropriate security module. An anti-tearing mechanism allows the prevention of any loss of units in the case of an aborted operation when using open reader (unwanted card extraction). The circuits are very well adapted for prepaid phone card applications.

Figure 2. Memory Map

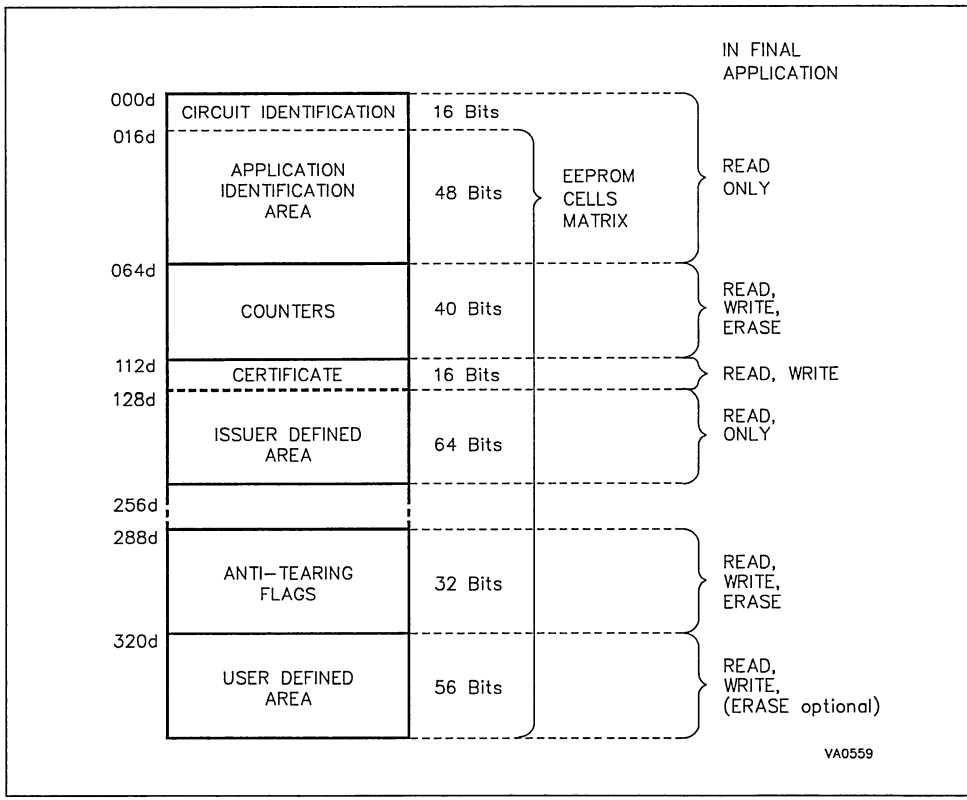
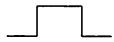
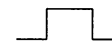


Figure 3. ST1331 - 6 Contacts Protocol

Function Code		CLK	Command
RST	B		
0	0		RESET
1	0		NO EFFECT
0	1		READ
0	1		COMPARE
1	1		PROGRAM

Programmed bit at '1' (I/O line = V_{CC})

Figure 4. ST1336 - 5 Contacts Protocol

RST (Reset)	CLK	Command
1		RESET
0		READ
0		COMPARE
	0	PROGRAM
0		

Programmed bit at '0' (I/O line = GND)

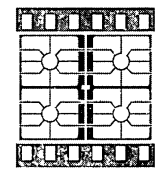
SGS-THOMSON MICROELECTRONICS

ST1333
ST1335

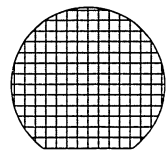
SMARTCARD CMOS 272 bit EEPROMs

ADVANCE DATA

- SINGLE 5V SUPPLY VOLTAGE
- PROGRAMMING TIME < 5 ms
- MEMORY DIVIDED INTO:
  - 16 bits of Chip Identification Data
  - 48 bits of Card Identification Data
  - up to 40 bits of Counter
  - 16 bits for Valorisation Certificate
  - 64 bits for Authentication Secret Key
  - 32 bits for Anti-Tearing Flags
  - 56 bits of User/Issuer Defined Data
- COUNTING CAPABILITY up to 32,768 (8^5) UNITS
- CIRCUIT PROTECTED by TRANSPORT CODE for DELIVERY from SGS-THOMSON to the CUSTOMER (ST1335 only)
- CERTIFICATE for CARD VALORISATION
- ADVANCED AUTHENTICATION FUNCTION
- SPECIAL ANTI-TEARING MECHANISM
- 2 COMMUNICATION PROTOCOLS POSSIBLE
  - 6 Contacts for ST1333
  - 5 Contacts for ST1335
- ANSWER to RESET COMPATIBLE with ISO 7816-3
- E.S.D. GREATER THAN 4000V
- POWER-ON, LOW and HIGH V_{CC} RESET
- ST1335 COUNTERS COMPATIBLE with ST1305 or EQUIVALENT



Micromodule



Wafer

Figure 1. Logic Diagram

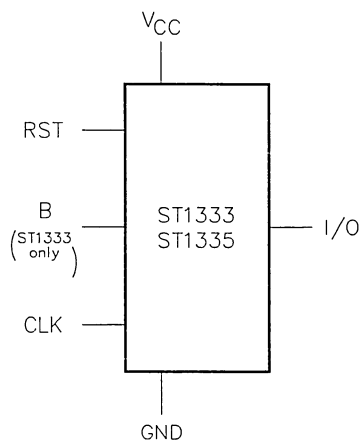


Table 1. Signal Names

CLK	Clock
RST	Function Code for ST1333
	Reset for ST1335
B	Function Code (ST1333 only)
I/O	Data Input / Output
V_{CC}	Supply Voltage
GND	Ground

DESCRIPTION

The ST1333 and ST1335 are 272 bits EEPROM memories protected by hard wired security logic and special fuses. The memory is a matrix of 34 x 8 cells, accessed bit by bit for reading and programming, and by byte for internal erasing in final application.

Authentication secret key and valorisation certificate are implemented in the memory and allow the recognition of the circuit by the appropriate security module. A unique 4 bits authentication signature is generated from chip data and chip secret key when this circuit is challenged by the security module. An anti-tearing mechanism allows the prevention of any loss of units in the case of an aborted operation when using open reader (unwanted card extraction). The circuits are very well adapted for prepaid phone card applications.

Figure 2. Memory Map

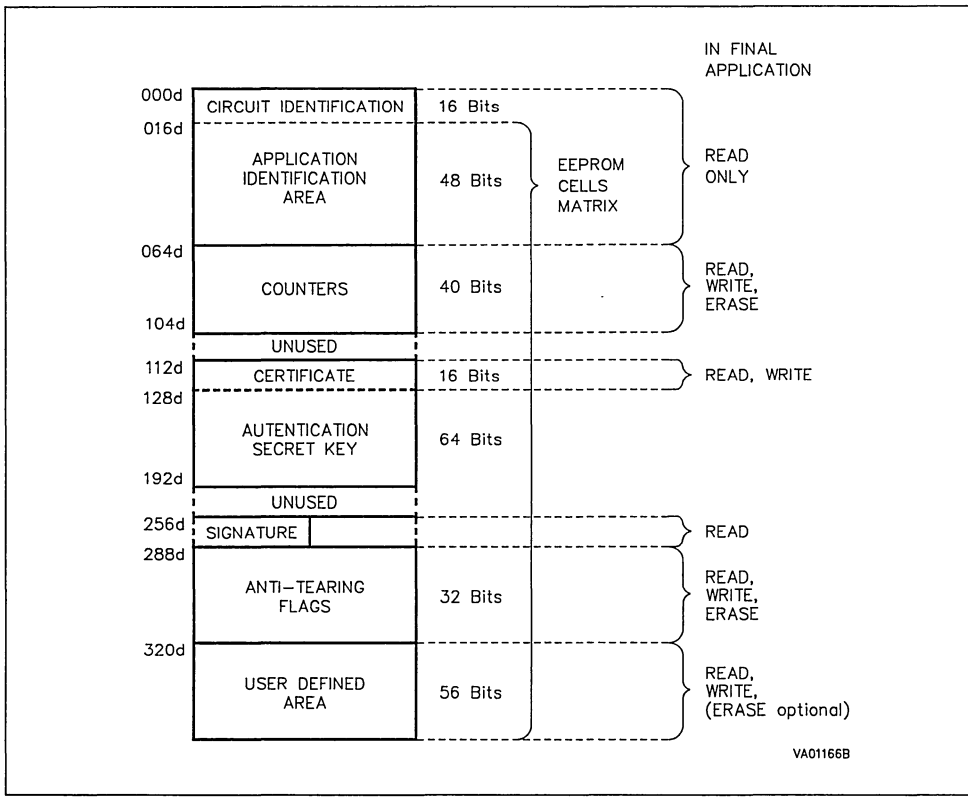
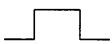
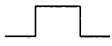


Figure 3. ST1333 - 6 Contacts Protocol

Function Code		CLK	Command
RST	B		
0	0		RESET
1	0		NO EFFECT
0	1		READ
0	1		COMPARE
1	1		PROGRAM

Programmed bit at '1' (I/O line = V_{CC})

Figure 4. ST1335 - 5 Contacts Protocol

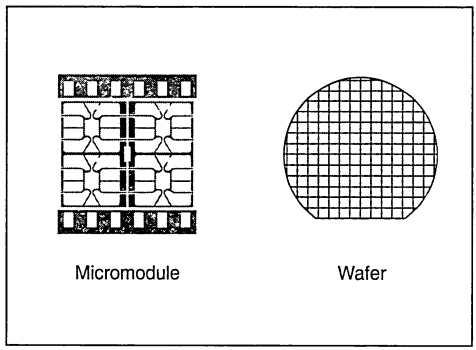
RST (Reset)	CLK	Command
1		RESET
0		READ
0		COMPARE
	0	PROGRAM
0		

Programmed bit at '0' (I/O line = GND)

SERIAL ACCESS CMOS 2K (256 x 8) EEPROM

ADVANCE DATA

- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE 3V to 5.5V SUPPLY VOLTAGE
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES



DESCRIPTION

The ST14C02C is a 2K bit electrically erasable programmable memory (EEPROM), organized as 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. This memory operates with a supply voltage value as low as 3V. Both sawn and unsawn wafers and modules on film are available.

The memory is compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. It carries a built-in 7 bit, unique device identification code (1010000) corre-

Figure 1. Logic Diagram

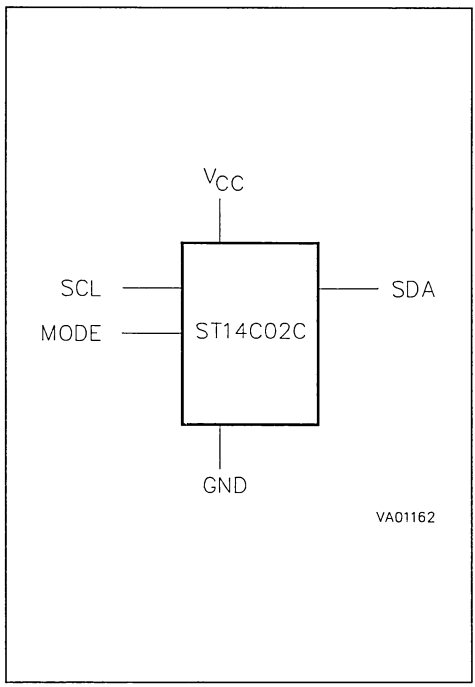


Table 1. Signal Names

SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode
V_{CC}	Supply Voltage
GND	Ground

Figure 2A. Contact Connections

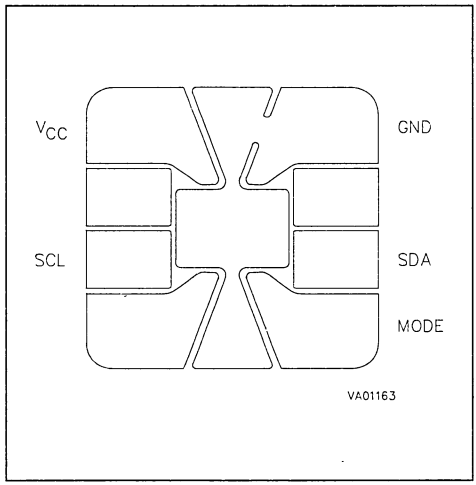
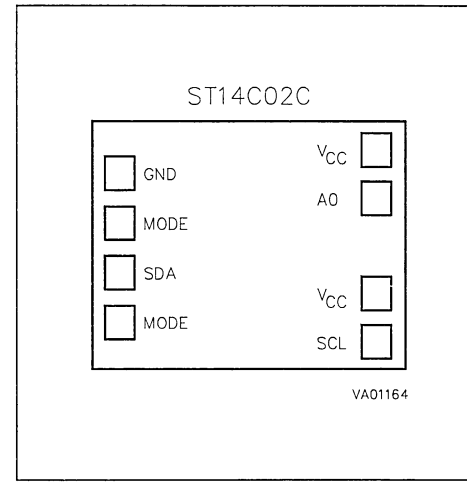


Figure 2B. Die Floor Plan



Note: A0 is internally connected to GND. The two MODE pads and the two V_{CC} pads are internally connected together.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		0 to 70	°C
T_{STG}	Storage Temperature	Wafer form Module form	–65 to 150 –40 to 120	°C
V_{IO}	Input or Output Voltage		–0.3 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

sponding to the I^2C bus definition. Only one memory can be attached to the I^2C bus. This memory behaves as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010000), plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code							$\overline{RW}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	0	0	0	$\overline{RW}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	$\overline{RW}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $\overline{RW}$ = '1'
Random Address Read	'0'	X		START, Device Select, $\overline{RW}$ = '0', Address
	'1'	X	1	reSTART, Device Select, $\overline{RW}$ = '1'
Sequential Read	'1'	X	1 to 256	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, $\overline{RW}$ = '0'
Multibyte Write	'0'	V_{IH}	4	START, Device Select, $\overline{RW}$ = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, $\overline{RW}$ = '0'

Note: 1. X = V_{IH} or V_{IL}

Table 5. Endurance and Data Retention Guarantees

Device	Endurance E/W Cycles	Data Retention Years
ST14C02C	1,000,000	10

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 4).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 4).

Mode (MODE). The MODE input may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as a V_{IH} (Multibyte Write mode). Note that the voltages are CMOS levels, not TTL compatible.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 3. AC Testing Input Output Waveforms

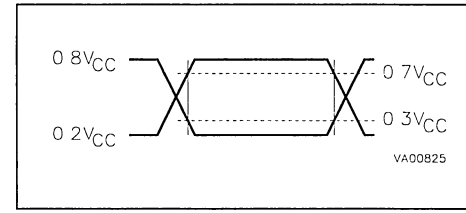
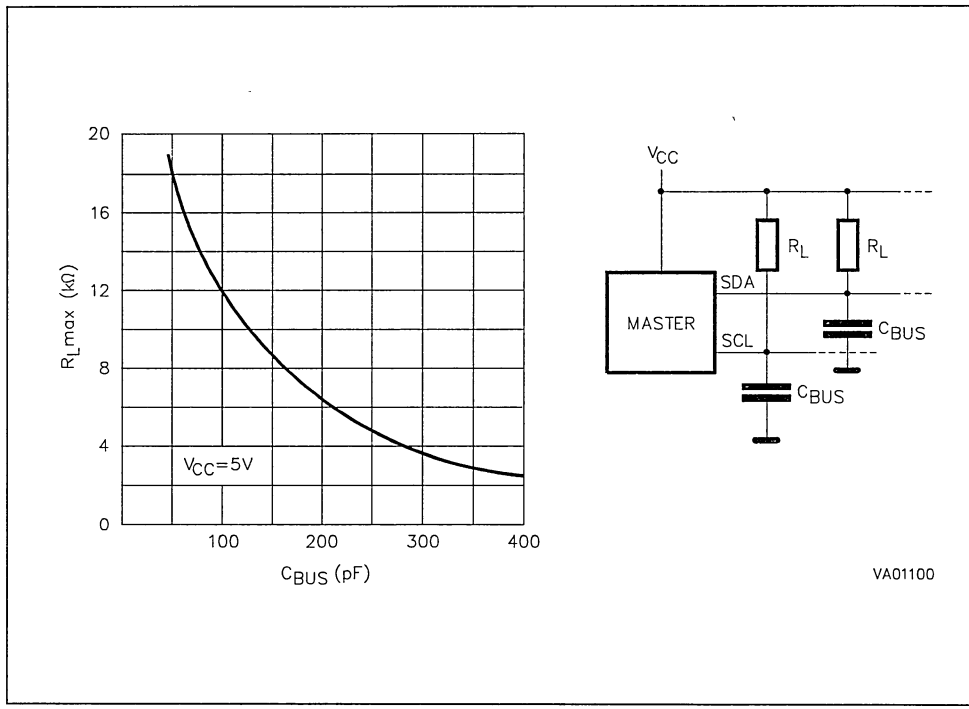


Table 6. Capacitance (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF

Note: 1. Sampled only, not 100% tested

Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus



DEVICE OPERATION

I²C Bus Background

The ST14C02C supports the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. This memory is always slave device in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the memory continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST14C02C samples the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave memory, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

The 7 most significant bits of the device select code are the device type identifier, corresponding to the I²C bus definition. For these memories the 7 bits are fixed as 1010000b (A0h).

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Write Operations

The Multibyte Write mode is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 6 most significant address bits A7-A2), the programming time is then doubled to a maximum of 20ms. Writing more than 4 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 8 bytes long). However, the Multibyte Write can properly write up to 8 consecutive bytes only if the first address of these 8 bytes is the first address of the row, the 7 following bytes being written in the 7 following bytes of this same 'row'.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data

Table 7. DC Characteristics (T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V)

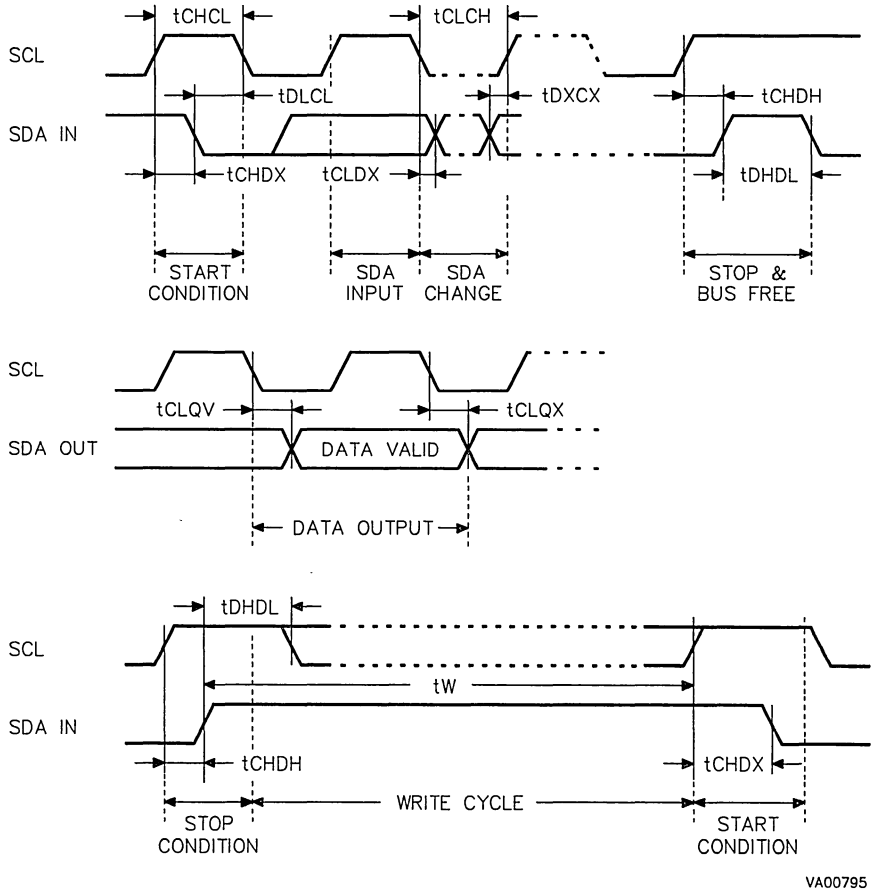
Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LI}	Input Leakage Current (MODE pad)	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
I_{CC1}	Supply Current (Standby)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (MODE)		–0.3	0.5	V
V_{IH}	Input High Voltage (MODE)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V

Table 8. AC Characteristics (T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time After Clock Low	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	T_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms

Figure 5. AC Waveforms



DEVICE OPERATION (cont'd)

being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (tw) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master.

The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the master issues a START condition followed by a device select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Figure 6. I^2C Bus Protocol

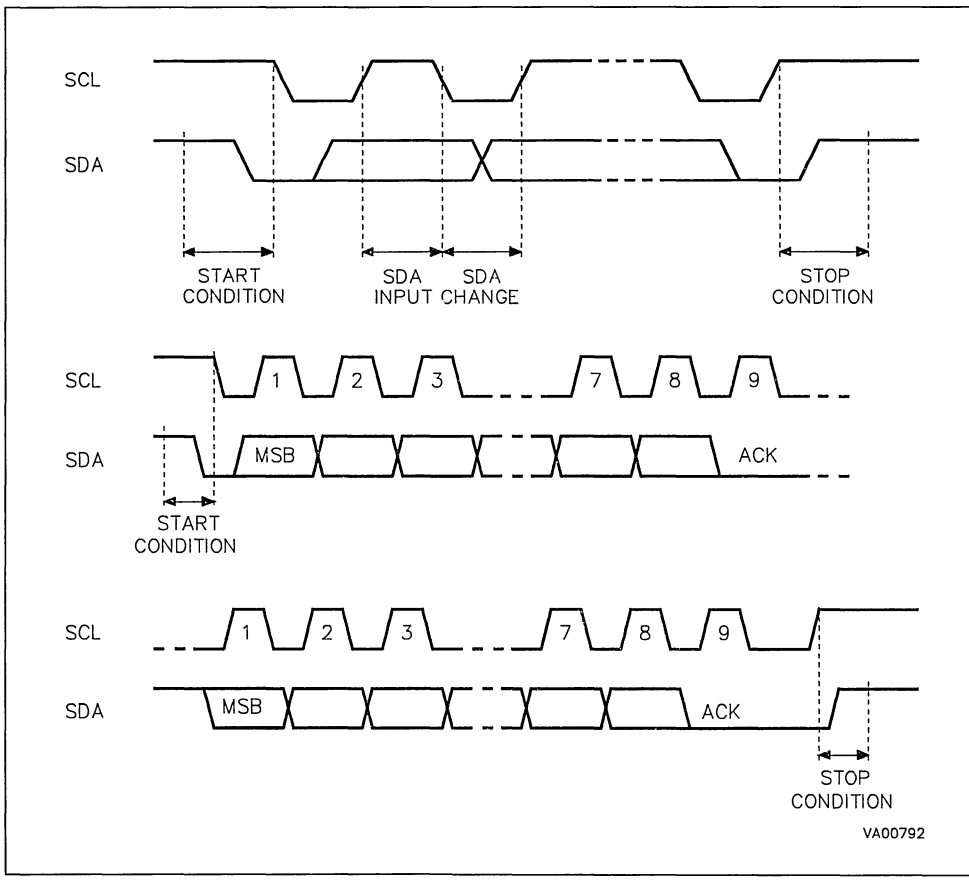


Figure 7. Write Cycle Polling using ACK

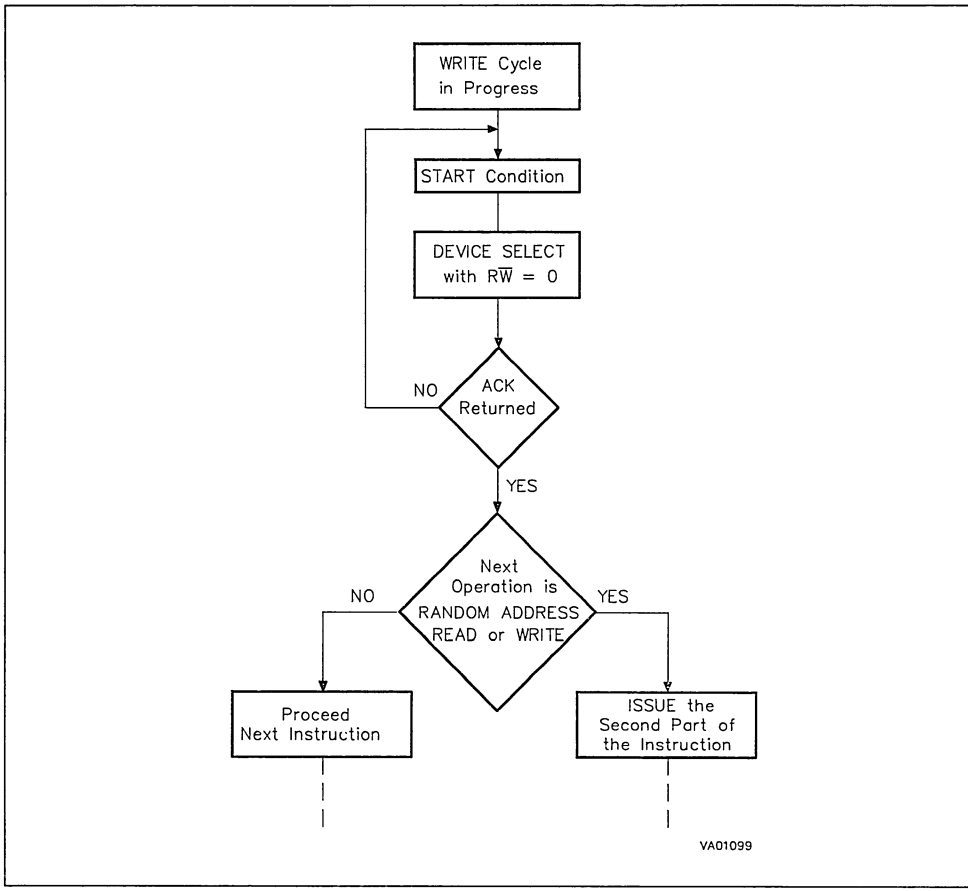
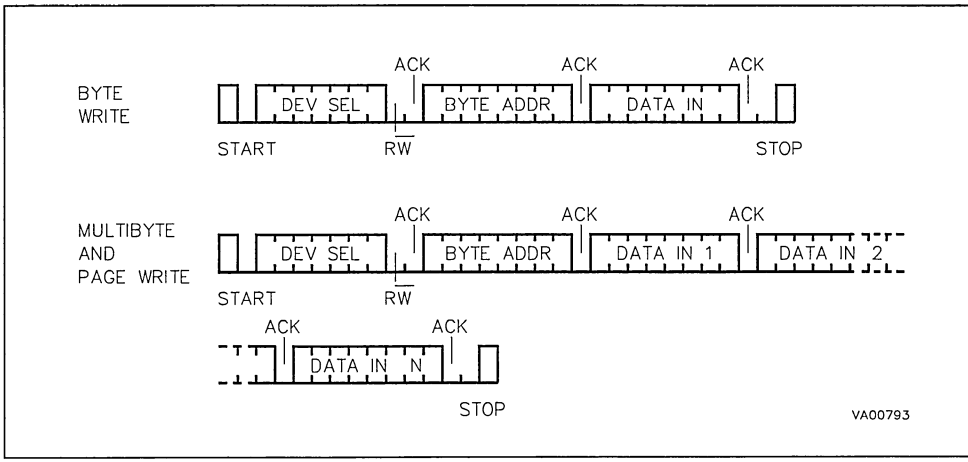


Figure 8. Write Modes Sequence



Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

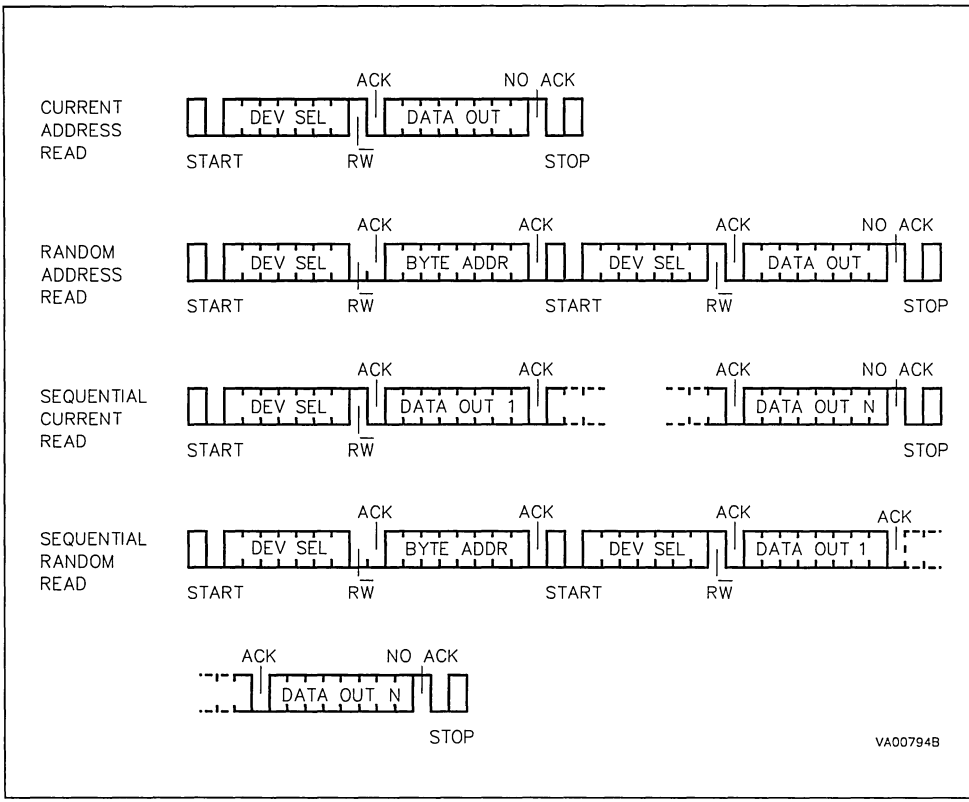
Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 9. This is followed by another START condition from the master and the byte address is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

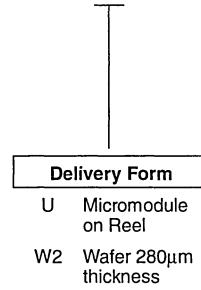
Acknowledge in Read Mode. In all read modes the memory waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST14C02C terminate the data transfer and switches to a standby state.

Figure 9. Read Modes Sequence



ORDERING INFORMATION SCHEME

Example: ST14C02C U



Parts are shipped with the memory content set at all "1's" (FFh).

For a list of available options refer to the Selector Guide in this Data Book or to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

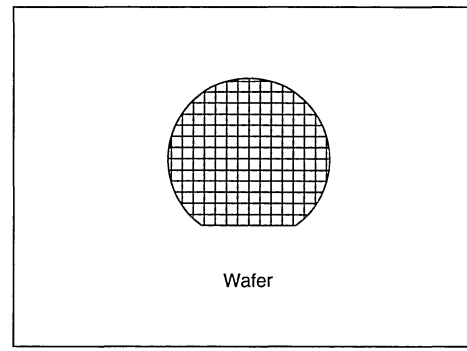
SGS-THOMSON MICROELECTRONICS

ST16XYZ

CMOS MCU BASED FAMILY OF SMARTCARDS ICs

ADVANCE DATA

- 8 BIT ARCHITECTURE CPU
- 2 to 16K BYTES of USER ROM
- 96 to 1K BYTES of USER RAM
- 64 to 64K BYTES of EEPROM
- SERIAL ACCESS, ISO 7816-3 PIN OUT COMPATIBLE
- 5 MHz INTERNAL OPERATING FREQUENCY
- SINGLE SUPPLY VOLTAGE IN ALL OPERATING MODES (5V ± 10%)
- POWER ON RESET
- 1 to 32 BYTES MULTIBYTE EEPROM PROGRAMMING CAPABILITY
- VERY HIGH SECURITY LEVEL
- CUSTOMER OPTIONS FOR: SECURITY, SPEED, INTERRUPT, I/O CONFIGURATION
- HIGHLY RELIABLE CMOS EEPROM TECHNOLOGY



Wafer

DESCRIPTION

The ST16XY is the generic name of a family of serial access devices perfectly suited to smartcard applications. Built around an 8 bit CPU core, each "family member" includes on chip memories: static RAM can range from 96 up to 1024 bytes, from 2K to 16K bytes of user ROM and 64 to 64K bytes of EEPROM are also user selectable.

A large choice of user defined options regarding the clock speed, security, the interrupts and the I/O buffer configurations provide the user with extra flexibility.

The SGS-THOMSON Microelectronics ST16XYZ family has been especially designed for applications requiring a very high level of security.The 100% compatibility of the ST16XYZ products with the ISO standard (serial access, 5 contacts only, 5V single power supply in all operating modes, answer to reset conforming to ISO 7816-3...) makes these devices particularly suitable for "Smartcard" type applications.

Table 1. ST16XYZ Family Members

Product	RAM	ROM	EEPROM
ST16301	128 bytes	3K bytes	1K bytes
ST16612	160 bytes	6K bytes	2K bytes
ST16B22	224 bytes	11K bytes	2K bytes
ST16623	224 bytes	6K bytes	3K bytes
ST16F48	288 bytes	16K bytes	8K bytes

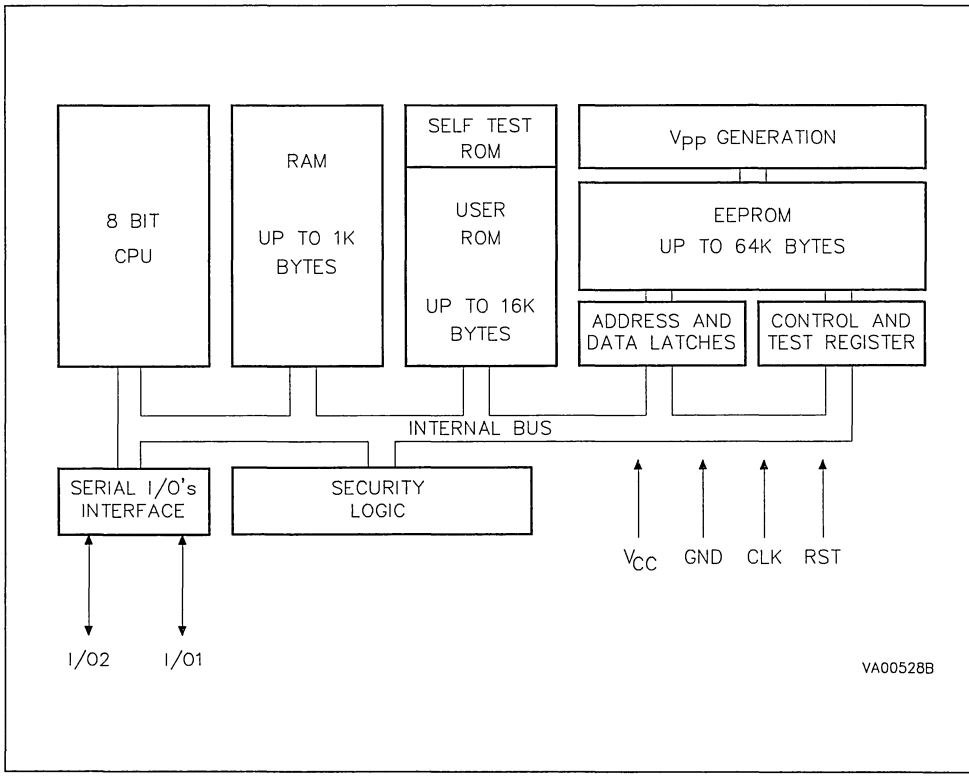
DESCRIPTION (Cont'd)

The design of the "on-chip" EEPROM along with a very high reliability CMOS process yields typical endurance of over 100k Erase/Write cycles and data retention greater than 10 years.

In order to develop the software and determine the ROM code, the ST16XYZ-EMU development system is available. The customer can define its product configuration in term of memory sizes and options and validate its code.

Then SGS THOMSON-Microelectronics will process this product according to customer requirements.

Figure 2. Block Diagram



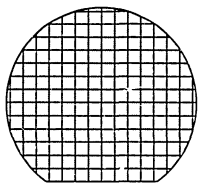
SGS-THOMSON MICROELECTRONICS

ST16F48

CMOS MCU BASED SAFEGUARDED SMARTCARD IC WITH 8K EEPROM

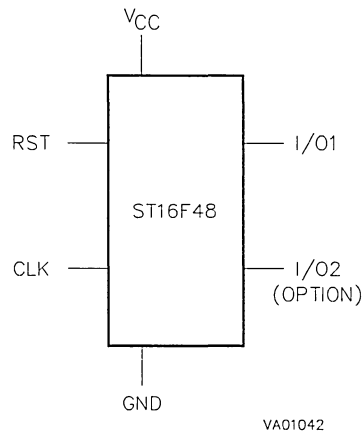
ADVANCE DATA

- 8 BIT ARCHITECTURE CPU
- 16K BYTES of ROM
- 288 BYTES of RAM
- 8176 BYTES of EEPROM, SECTORS COMBINATIVE:
  - Highly reliable CMOS EEPROM Technology
  - 10 Years Data Retention
  - 100k Erase/Write Cycles Endurance
  - Protected one time programmable block (32 or 64 bytes)
  - Separate Write and Erase cycle for fast "1" programming
  - 1 to 32 bytes block Erase or Write single cycle programming
- SERIAL ACCESS, ISO 7816-3 COMPATIBLE
- SINGLE 5V ± 10% SUPPLY VOLTAGE
- IDLE MODE for POWER SAVING
- 5 MHz INTERNAL OPERATING FREQUENCY
- VERY HIGH SECURITY FEATURES
- 6 PINS CONTACT ASSIGNMENT as for ISO 7816-2
- E.S.D. PROTECTION GREATER than 4000V



Wafer

Figure 1. Logic Diagram



DESCRIPTION

The ST16F48, a member of the standard ST16XYZ family devices, is a serial access microcontroller especially designed for very large volume and cost competitive smartcards applications, where firmware security algorythm must be implemented, and a large EEPROM memory capacity is required.

Table 1. Signal Names

CLK	Clock
RST	Reset
I/O1	Data Input / Output
I/O2	Data Input / Output (Option)
V_{CC}	Supply Voltage
GND	Ground

DESCRIPTION (cont'd)

The ST16F48 is based on an SGS-THOMSON 8 bit CPU core and includes on-chip memories: 288 bytes of RAM, 16K bytes of ROM and 8176 bytes of EEPROM structured in two main sectors to be used in different conbinations, as here follow described:

Sector A	Sector B
0	8176
1024	7152
2048	6128
4096	4080

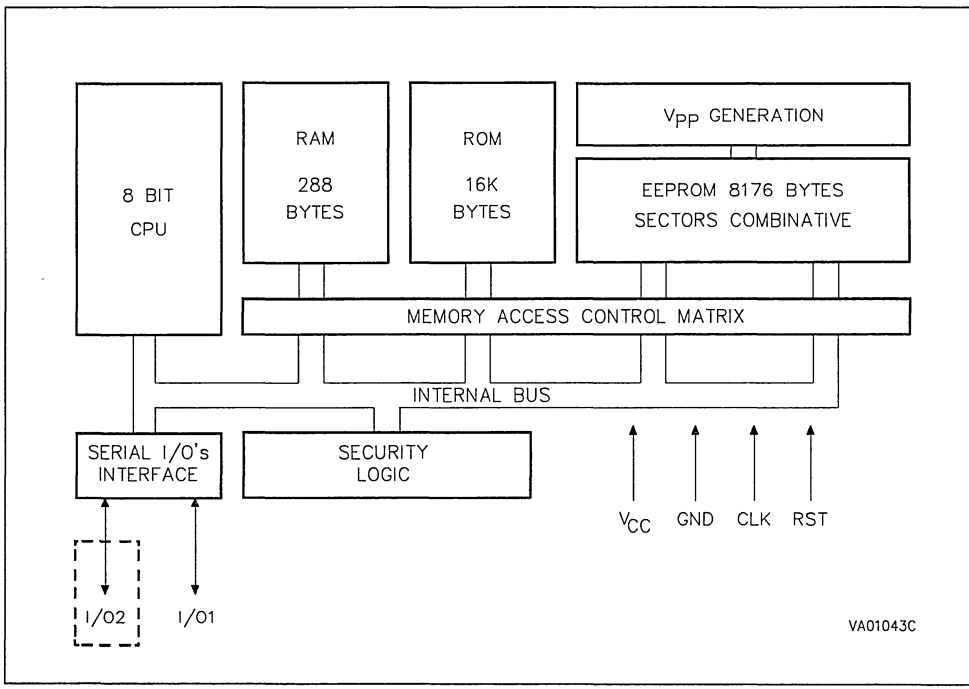
It is manufactured using the high reliable 1µm CMOS EEPROM technology.

As all the other ST16XYZ family members, it is fully compatible with the ISO standards for smartcards applications.

Software development and firmware (ROM code/options) generation can be done with the ST16XYZ-EMU development system.

The ST16F48 can be delivered in 5 or 6 inches sawn or unsawn, 280µm thickness wafers.

Figure 2. Block Diagram



SGS-THOMSON MICROELECTRONICS

ST16601

CMOS MCU BASED SAFEGUARDED SMARTCARD IC WITH 1K EEPROM

ADVANCE DATA

- 8 BIT ARCHITECTURE CPU
- 6K BYTES of ROM, SECTORS COMBINATIVE
- 128 BYTES of RAM
- 1088 BYTES of EEPROM, SECTORS COMBINATIVE:
  - Highly reliable CMOS EEPROM Technology
  - 10 Years Data Retention
  - 100k Erase/Write Cycles Endurance
  - Protected one time programmable block (32 or 64 bytes)
  - Separate Write and Erase cycle for fast "1" programming
  - 1 to 16 bytes block Erase or Write single cycle programming
- SERIAL ACCESS, ISO 7816-3 COMPATIBLE
- LOW VOLTAGE OPERATION
  - V_{CC} Range: 2.7V to 5.5V
- POWER SAVING IDLE MODE
- 5MHz INTERNAL OPERATING FREQUENCY
- VERY HIGH SECURITY FEATURES
- 6 PINS CONTACT ASSIGNMENT as for ISO 7816-2
- E.S.D. PROTECTION GREATER than 5000V

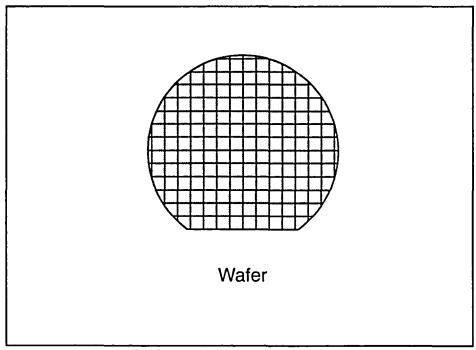
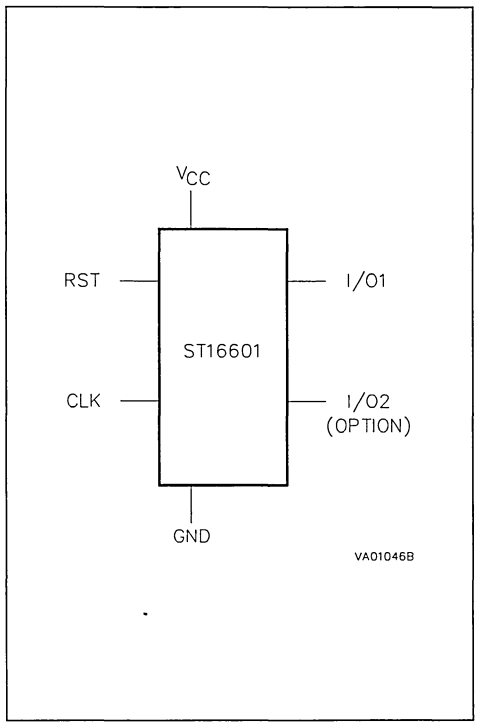


Figure 1. Logic Diagram



DESCRIPTION

The ST16601, a member of the standard ST16XYZ family devices, is a serial access microcontroller especially designed for very large volume and cost competitive smartcards applications, where firmware security algorythm must be implemented.

Table 1. Signal Names

CLK	Clock
RST	Reset
I/O1	Data Input / Output
I/O2	Data Input / Output (Option)
V_{CC}	Supply Voltage
GND	Ground

DESCRIPTION (cont'd)

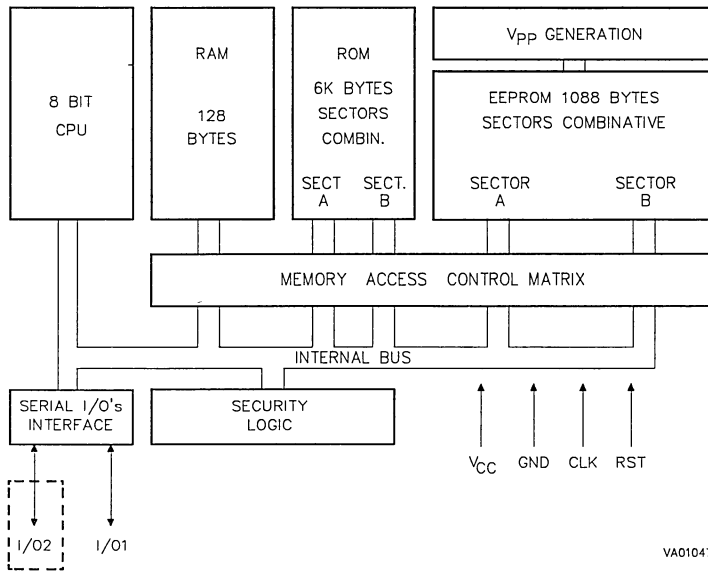
The ST16601 is based on an SGS-THOMSON 8 bit CPU core and includes on-chip memories: 128 bytes of RAM, 6K bytes of ROM and 1088 bytes of EEPROM. Both ROM and EEPROM memories can be configured into two sectors. Access rules from any memory section (sector) to any other are setup by User's defined Memory Access Control Matrix.

It is manufactured using the high reliable SGS-THOMSON 1µm CMOS EEPROM technology.

As all the other ST16XYZ family members, it is fully compatible with the ISO standards for smartcards applications. Software development and firmware (ROM code/options) generation can be done with the ST16XYZ-EMU development system.

The ST16601 can be delivered in 5 inches sawn or unsawn,180µm or 280µm thickness wafers.

Figure 2. Block Diagram



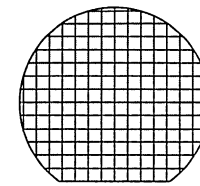
SGS-THOMSON MICROELECTRONICS

ST16SF48

CMOS MCU BASED SAFEGUARDED SMARTCARD IC WITH 8K EEPROM

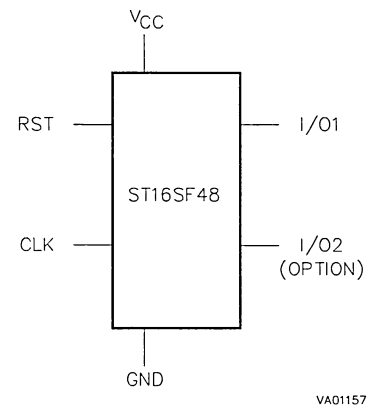
ADVANCE DATA

- 8 BIT ARCHITECTURE CPU
- 16K BYTES of ROM, SECTORS COMBINATIVE
- 288 BYTES of RAM
- 8176 BYTES of EEPROM, SECTORS COMBINATIVE
  - Highly reliable CMOS EEPROM Technology
  - 10 Years Data Retention
  - 100k Erase/Write Cycles Endurance
  - Protected one time programmable block (32 or 64 bytes)
  - Separate Write and Erase cycle for fast "1" programming
  - 1 to 32 bytes block Erase or Write single cycle programming
- SERIAL ACCESS, ISO 7816-3 COMPATIBLE
- LOW VOLTAGE OPERATION
  - V_{CC} Range: 2.7V to 5.5V
- IDLE MODE for POWER SAVING
- 5 MHz INTERNAL OPERATING FREQUENCY
- VERY HIGH SECURITY FEATURES
- 6 PINS CONTACT ASSIGNMENT as for ISO 7816-2
- E.S.D. PROTECTION GREATER than 5000V



Wafer

Figure 1. Logic Diagram



DESCRIPTION

The ST16SF48, a member of the standard ST16XYZ family devices, is a serial access microcontroller especially designed for very large volume and cost competitive smartcards applications, where firmware security algorythm must be imple-

Table 1. Signal Names

CLK	Clock
RST	Reset
I/O1	Data Input / Output
I/O2	Data Input / Output (Option)
V_{CC}	Supply Voltage
GND	Ground

DESCRIPTION (cont'd)

mented, and a large EEPROM memory capacity is required.

The ST16SF48 is based on an SGS-THOMSON 8 bit CPU core and includes on-chip memories: 288 bytes of RAM, 16K bytes of ROM and 8176 bytes of EEPROM.

Both ROM and EEPROM memories can be configured into two sectors. Access rules from any memory section (sector) to any other are setup by User's defined Memory Access Control Matrix.

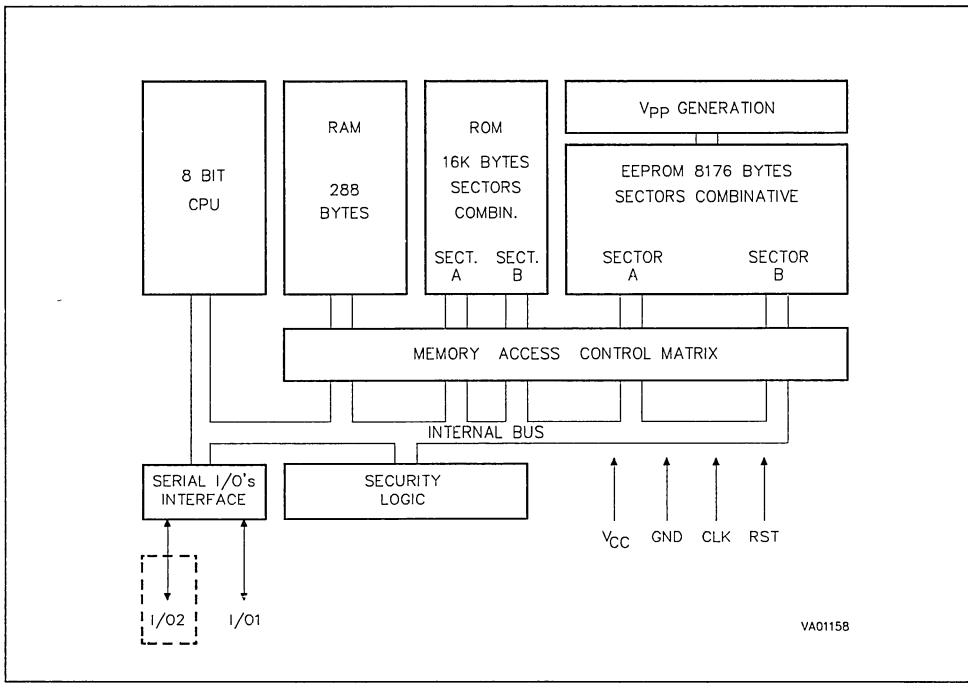
It is manufactured using the high reliable SGS-THOMSON 1µm CMOS EEPROM technology.

As all the other ST16XYZ family members, it is fully compatible with the ISO standards for smartcards applications.

Software development and firmware (ROM code/options) generation can be done with the ST16XYZ-EMU development system.

The ST16SF48 can be delivered in 5 or 6 inches sawn or unsawn, 180µm or 280µm thickness wafers.

Figure 2. Block Diagram



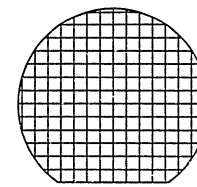
SGS-THOMSON MICROELECTRONICS

ST16CF54

CMOS MCU BASED SAFEGUARDED SMARTCARD IC WITH MODULAR ARITHMETIC PROCESSOR

ADVANCE DATA

- 8 BIT ARCHITECTURE CPU
- 16K BYTES of ROM, SECTORS COMBINATIVE
- 352 BYTES of RAM
- 4K BYTES of EEPROM, SECTORS COMBINATIVE:
  - Highly reliable CMOS EEPROM Technology
  - 10 Years Data Retention
  - 100k Erase/Write Cycles Endurance
  - Protected one time programmable block (32 or 64 bytes)
  - Separate Write and Erase cycle for fast "1" programming
  - 1 to 32 bytes block Erase or Write single cycle programming
- MODULAR ARITHMETIC PROCESSOR
  - Fast modulo N multiplication, squaring and calculation of MONTGOMERY constants.
  - Software selectable operand length (256/512 bit)
  - Double operand operation (1024 bit)
- SERIAL ACCESS, ISO 7816-3 COMPATIBLE
- SINGLE 5V ± 10% SUPPLY VOLTAGE
- POWER SAVING IDLE MODE
- 5 MHz INTERNAL OPERATING FREQUENCY
- VERY HIGH SECURITY FEATURES
- 6 PINS CONTACT ASSIGNMENT as for ISO 7816-2
- E.S.D. PROTECTION GREATER than 5000V



Wafer

- FAST CRYPTATION PROCESSING
  - 66ms RSA Signature
  - 100ms DSS Signature
  - 200ms DSS Authentification

Figure 1. Logic Diagram

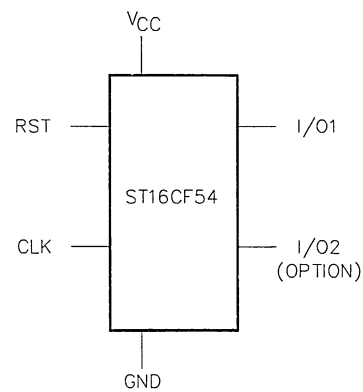


Table 1. Signal Names

CLK	Clock
RST	Reset
I/O1	Data Input / Output
I/O2	Data Input / Output (Option)
V_{CC}	Supply Voltage
GND	Ground

DESCRIPTION

The ST16CF54, a member of the ST16XYZ family devices, is a serial access microcontroller especially designed for very large volume and cost competitive smartcards applications, where high performance Public Key Algorithms will be implemented, to cut down initiallization and communication costs and to increase security.

Its internal Modular Arithmetic Processor is designed to speed up cryptographic calculations using Public Key Algorithms. It processes modular multiplications and squaring on 256/512 bit operands or a double operand of 1024 bits. The ST16CF54 is based on an SGS-THOMSON 8 bit CPU core including on-chip memories: 352 bytes of RAM, 16K bytes of ROM and 4K of EEPROM.

Both ROM and EEPROM memories can be configured into two sectors. Access rules from any memory section (sector) to any other are setup by User's defined Memory Access Control Matrix.

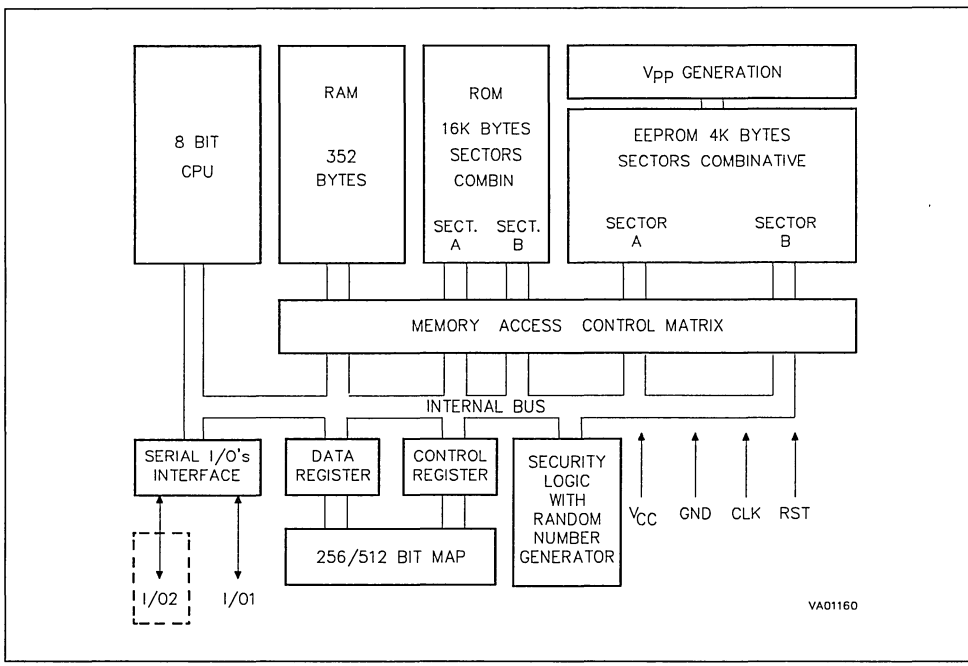
It is manufactured using the high reliable SGS-THOMSON 1µm CMOS EEPROM technology.

As all the other ST16XYZ family members, it is fully compatible with the ISO standards for smartcards applications.

Software development and firmware (ROM code/options) generation can be done with the ST16XYZ-EMU development system.

The ST16CF54 can be delivered in 5 inches sawn or unsawn, 180µm or 280µm thickness wafers.

Figure 2. Block Diagram



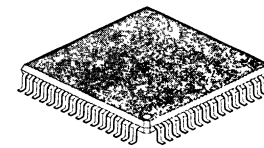
SGS-THOMSON MICROELECTRONICS

ST16xF74

CMOS CRYPTO-COMPUTER FAMILY

ADVANCE DATA

- 8 BIT ARCHITECTURE CPU
- 20K BYTES of ROM
- 608 BYTES oF RAM
- 4K BYTES of EEPROM SECTORS COMBINATIVE:
  - Highly reliable CMOS EEPROM Technology
  - 10 Years Data Retention
  - 100K Erase/Write Cycles Endurance
  - Protected one time programmable block (32 or 64 bytes)
  - Separate Write and Erase cycle for fast "1" programming
  - 1 to 32 bytes block Erase or Write single cycle programming
- SINGLE 5V ± 10% SUPPLY VOLTAGE
- SOPHISTICATED HIGH SECURITY FEATURES
- PROGRAMMABLE 8 BIT PARALLEL HOST BUS INTERFACE
- FIVE I/0 PORTS
  - Two 8 bit ports
  - One 4 bit port
  - Two serial ports
- MODULAR ARITHMETIC PROCESSOR
  - Fast modulo N addition, subtraction, multiplication, exponentiation and calculation of MONTGOMERY constants
  - Software selectable operand length (256/512 bit)
  - Double operand operation (1024 bit)
- REAL RANDOM NUMBER GENERATOR (can generate secret keys on board)
- OPTIONAL DES ACCELERATOR



PQFP64

- 64 PIN PQFP PACKAGE
- 512 BIT RSA SIGNATURES with 5MHz EXTERNAL CLOCK in 17ms

DESCRIPTION

The ST16xF74 is a family of safeguarded 8 bit MCU, especially designed for large volume and cost competitive smartcard terminals applications where high performance Public Key Algorithm are implemented, and Secret Keys are generated on board.

Its internal Modular Arithmetic Processor is designed to speed up cryptographic calculation using Public Key Algorithms. It can process modular addition, subtraction and exponentiation on 256/512 bit operands or 1024 bit double operand.

The optional DES Accelerator speeds up the necessary permutation specified by the NIST DEA standards.

The ST16xF74 is based on the SGS-THOMSON ST16XYZ family of 8 bit MCU.

Product Variance

ST16KF74	All features
ST16LF74	All features except DES accelerator
ST16MF74	All features except parallel I/O ports
ST16NF74	All features except DES accelerator and parallel I/O ports

DESCRIPTION (cont'd)

On-chip memories include: 608 bytes of RAM, 16K bytes of ROM and 4K bytes of EEPROM. The EEPROM can be configured into any of the following sector conbinations:

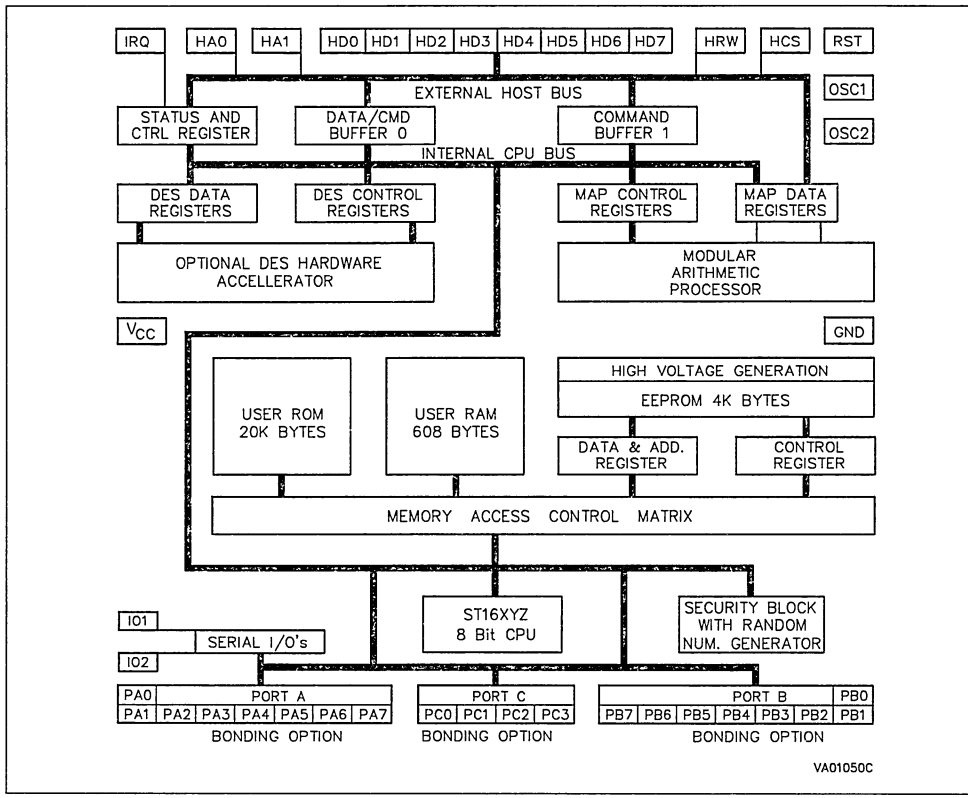
Sector A	Sector B
0	4096
512	3584
1024	3072
2048	2048

It is manufactured using the high reliable SGS-THOMSON 1µm CMOS EEPROM technology.

Software development and firmware (ROM code/options) generation can be done with the SGS-THOMSON ST16XYZ-EMU development system.

The ST16xF74 can be delivered in 64 pin PQFP.

Figure 1. Block Diagram



SGS-THOMSON MICROELECTRONICS

ST16XYZ-EMU

DEVELOPMENT SYSTEM FOR ST16XYZ, MCU BASED SMARTCARD IC FAMILY

HARDWARE

- Supports the whole ST16XYZ Smartcard IC family including low voltage range products
- Support of all ST16XYZ mask options and memory sizes
- Real time emulation
- 64K bytes of emulation memory
- Up to 16 breakpoints
- Tracing of 32 bits including 4 external lines
- Trace triggering events defined with up to 32 bits
- 3 triggering events with associated counters
- 2 synchronization outputs
- Emulation with external or internal clock

SOFTWARE

- Window based interfaces and menus
- Assembler-linker
- Macro call and conditional assembly
- Relocatable or absolute output files

GENERAL DESCRIPTION

The ST16XYZ-EMU is an advanced real time development system designed and configured to provide comprehensive support for the ST16XYZ products, a family of MCU based Smartcard IC products. This one box system contains the CPU part emulating the ST16XYZ CPU core, and the Memory part emulating all security logic and secure memory, which may be implemented inside any ST16XYZ device.

The software provided enables the hardware to be driven by any PC compatible host computer through 2 serial ports.

CPU EMULATION

The source software can be prepared in a modular fashion to enable good testability and fast debugging. It can be written using any word processing package and then assembled and linked by the assembler-linker. Assembly directives and macro functions are available.

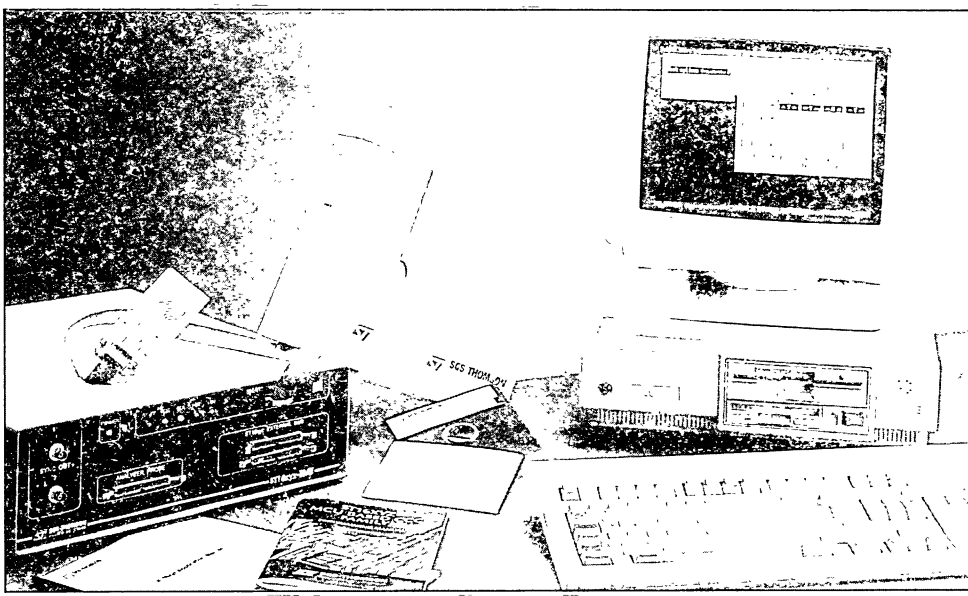
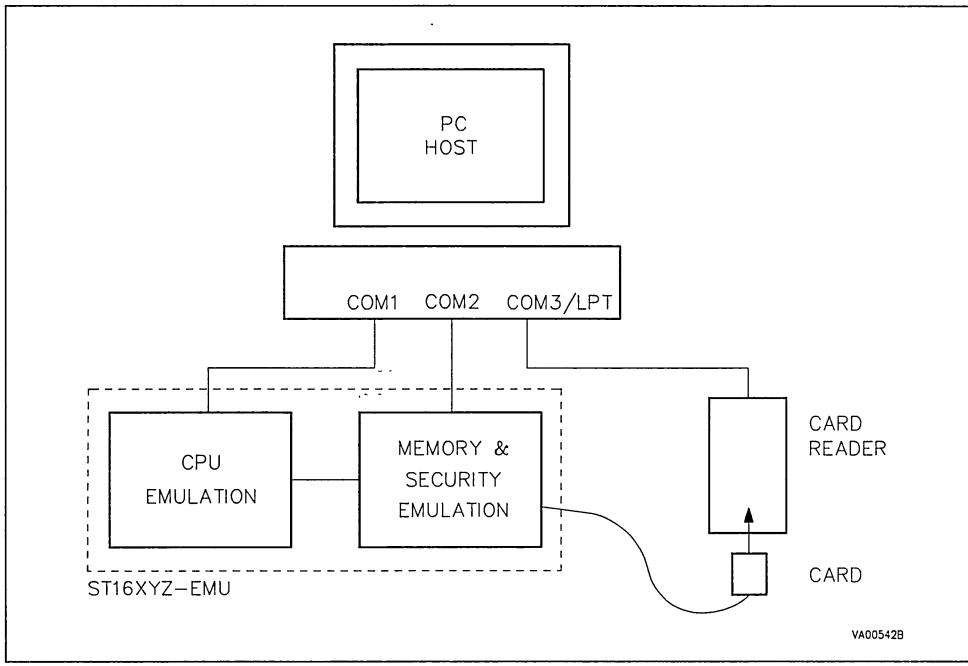


Figure 1. ST16XYZ-EMU System Configuration



CPU EMULATION (cont'd)

Hardware and software breakpoints allow the user to stop the MCU whenever the application ROM code execution reaches selected addresses, addresses within a selected range, or on data fetch cycles. The user is then able to read and modify any register or memory location within the simulated memory, inspect trace or place other breakpoints or triggers.

The logic analyser can be used when real time emulation is needed. It allows the recording of 32 bits words, including address bus, data bus, control bits and 4 external signals. Up to 1024 states per bit can be stored into the 32 Kbyte emulation memory.

Using the powerful triggering conditions of the logic analyser, it is possible to only record cycles which are of interest to the user. Events are defined as a pattern of up to 32 bits occurring up to 64,000 times. The acquisition mode can be defined by up to 3 events. The following examples show the powerful capabilities of this logic analyser:

- Records status of all specified bits until 'N' occurrences of event 1.
- Records 'N' cycles within a specified address range.
- Records status of all specified bits until 'N' occurrences of event 1, then records 'M' cycles within a range and finally, records everything until 'P' cycles after event 3.

Such a powerful tool enables the user to detect and trap any pattern and thus quickly debug the application. The trapping of random patterns is greatly improved by the capability to temporarily quit the emulation session while the emulator continues to run the application software. The whole memory of the PC is then available for any use, while the trace function continues to track defined events.

MEMORY EMULATION

The Memory part of the ST16XYZ-EMU emulates the ROM, RAM and EEPROM memories, the security logic of the family of devices, and support the mask options simulation for the ST16XYZ family.

Memories

ST16XYZ-EMU is configured with the help of a window menu allowing the user to define the size of each block of the emulated memory: ROM, RAM and EEPROM. A control of each memory block accesses is automatically performed by the Memory part when running the ROM code (real time emulation), any access out of a defined memory block is signalled on the screen of the host computer.

The EEPROM programming time is monitored by an internal time base and a warning is given to the user if a programming delay is shorter than the specified value. This value is set by default to nominal 3ms, and can be adjusted by the user to any value up to 100ms.

Security

The ST16XYZ-EMU front panel displays the status of the security detectors as well as the status of the chip external ISO 7816-3 compatible signals (V_{CC}, RST, CLK, I/O).

CARD READER

A card reader can be connected to the host computer through either serial or parallel link. The ST16XYZ-EMU command interpreter directs each command either towards the CPU or Memory part of the ST16XYZ-EMU, or the card reader. This enables the development loop to be closed, and complete applications to be emulated on one single host computer.

ORDERING INFORMATION

Part Number	Description
ST16XYZ-EMU	Development system for ST16XYZ, MCU based Smartcard IC's family

Note: The ST16XYZ-EMU is delivered with all necessary software for use on a PC or compatible host computer. Software is delivered on 1 2M density, 51/4 inch floppy disks.

APPLICATION AND QUALITY

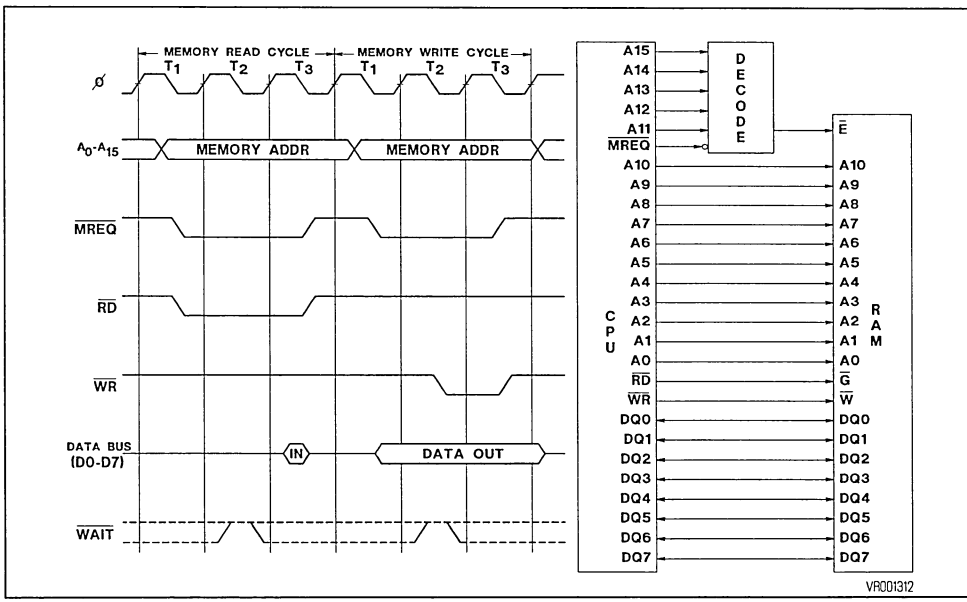
REPLACING EEPROM WITH ZEROPOWER

Currently there are two approaches for implementing non-volatile memory that can be electrically altered within the system. The first is EEPROM (electrically erasable programmable read only memory). The second is battery backed-up RAM. Many misconceptions about battery backed-up RAMs have swayed system designers away from this technology into using EEPROMs with lower performance specifications. All is not lost however, the ZEROPOWER™ technology developed by SGS THOMSON Microelectronics provides a totally integrated approach to battery backed-up RAMs, which in most cases can provide direct replacement of EEPROMs with an added advantage of upgrading system performance.

First let's clear the air about the misconceptions concerning battery backed-up RAM. The integration of a long life lithium cell and the low standby current of CMOS RAMs have made possible data retention times that typically extend beyond ten years. Periodic replacement of batteries or battery charging circuits are no longer necessary. Power fail detection and switching circuitry can be integrated into the same package along with RAM and a small button lithium cell making a complete battery backed-up system that fits into the same socket as conventional RAM. This system in a DIP (dual in-line package) has been invented and trademarked as ZEROPOWER technology by SGS-THOMSON. Extensive reliability studies of the ZEROPOWER technology have been undertaken at SGS-THOMSON which demonstrate a highly reliable approach to non-volatile memory.

Because microprocessors are designed to interface to RAMs, a ZEROPOWER RAM provides the ideal replacement for conventional RAM. Figure 1 shows a typical output timing and interface of an 8 bit microprocessor (Z80). RAM interface can be made by decoding MREQ and address information for $\overline{E}$, connecting $\overline{RD}$ to $\overline{G}$, and connecting $\overline{WR}$ to $\overline{R}$.

Figure 1. Z80 Timing



EEPROMs, on the other hand, require some modification to the write cycle. This modification can be as simple as adding wait cycles until a write to the EEPROM is completed. In this case direct replacement with a ZEROPOWER RAM is possible. The wait cycles can be left in or eliminated to improve performance.

Some early versions of EEPROMs (2816 without any suffix), however, require a 21 volt VPP signal. This type of EEPROM is programmed the same way conventional EPROMS are programmed. The only difference being that both "ones" and "zeros" can be programmed not just "zeros". Figure 2 shows how complicated interface to this type of EEPROM can be. Replacement with a ZEROPOWER RAM can be accomplished by eliminating almost all of the external circuitry. In the example shown in Figure 2 only the inverter E is required for interface to a ZEROPOWER RAM. For interface to a ZEROPOWER RAM the output of inverter $\overline{E}$ should be connected to $\overline{G}$, and $\overline{WR}$ should be connected directly to $\overline{W}$ on the ZEROPOWER RAM.

In contrast, current technology EEPROMs are 5 volts only. There are two popular types of EEPROMs in production today. The are referred to as latched and timer EEPROMs. Latched EEPROMs latch both data and address on the falling (beginning) edge of the write pulse. Although addresses and data are allowed to change before the completion of a write cycle, write enable must be held active for the complete write cycle. Figure 3 shows latched EEPROM write timing. Timer EEPROMs, however, latch addresses on the falling edge of the write pulse and data on the rising edge. Figure 4 shows timer EEPROM write cycle timing.

Figure 2. 2816 Interface

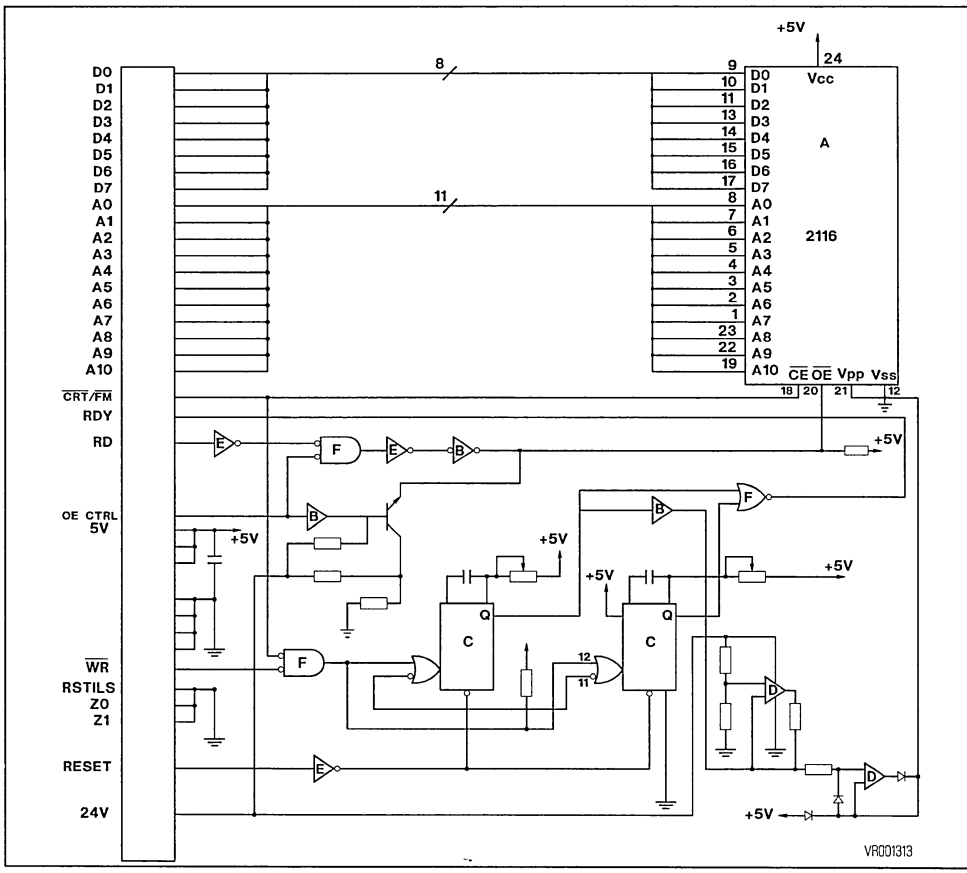


Figure 3. Latched EEPROM Write Cycle

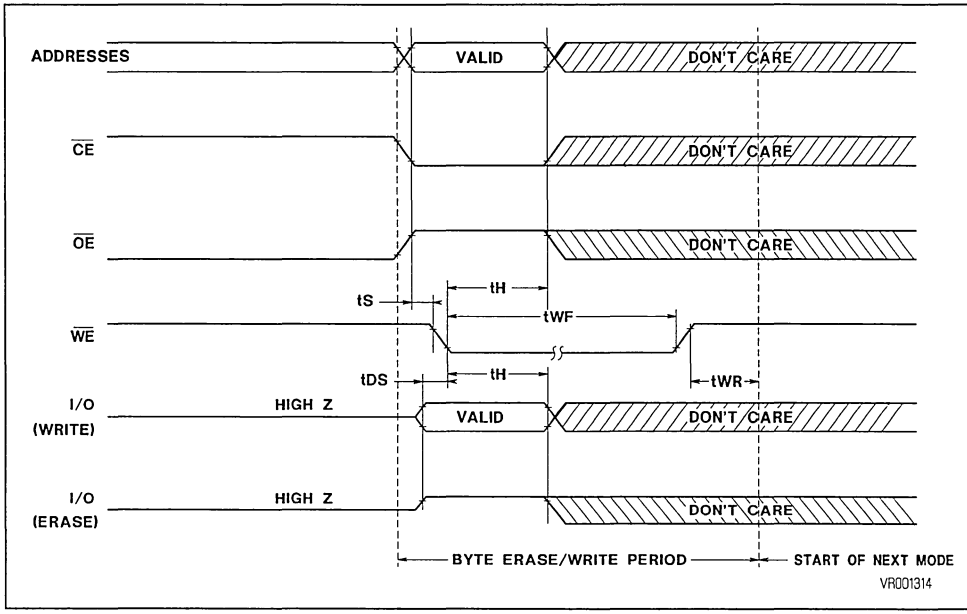
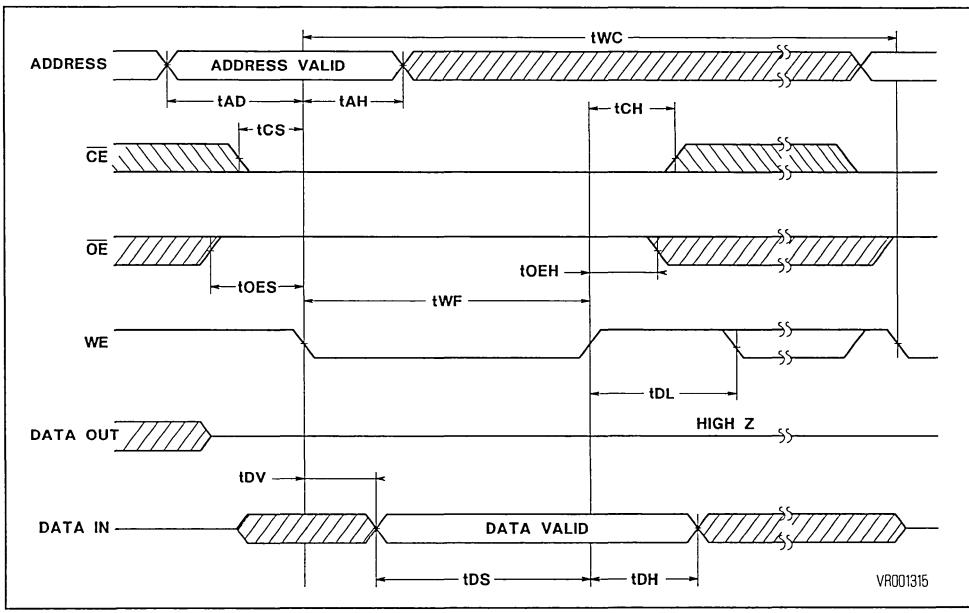


Figure 4. Timer EEPROM Write Cycle



Latched EEPROMs are interfaced in the system two ways. One, by latching the $\overline{WE}$ pulse until completion of the write cycle. Two by implementing multiple wait states to complete the write. Replacing latched EEPROM can be done by eliminating the $\overline{WE}$ latch, allowing the write cycle to follow the microprocessor. Multiple wait states will have no effect on the ZEROPOWER RAM, however for system efficiency they should be eliminated.

Timer EEPROMs are the most popular EEPROMs in use today because their write cycle timing is compatible with microprocessors that have cycle times in the 200 to 500 nanosecond range. The initialization of a timer EEPROM write cycle can be completed in the normal cycle time of the microprocessor and the EEPROM completes the write cycle independent of the system. Some timer EEPROMs will even allow multiple successsive writes (in page mode) before completion of the first write. ZEROPOWER RAMs are directly replaceable for timer EEPROMs in this application and have the advantage of even faster cycle times with no page mode restrictions. Timer EEPROMs, however, can also allow data and address changes during the write cycle. These data and address changes are not permited on conventional RAM and therefore in this application, data and address must be externally latched before replacement with ZEROPOWER RAM can be done. The later case is not industry standard for memories, and many systems with multiplexed address/data already have address and data latches for this reason.

Note :

Many EEPROMs require output enable to be high during the write cycle. With RAMs output enable is a "don't case" during write. In the very unlikely event that output enable should be used to gate the write cycle, a change in the circuit needs to be implemented before ZEROPOWER RAM can be used as a replacement.

PROGRAMMING THE MK48Z02

The MK48Z02 serves many varied applications. It provides the ease of access for both reads and writes that conventional RAMs offer, as well as nonvolatile memory that is associated with read only memories. Because of this nonvolatile characteristic, the MK48Z02 is often utilized as a medium for storage of alterable program code (firmware) as well as parametric data.

This type of data is usually generated on a software development system and then loaded into memory prior to installation of the device into the final product. Most software development systems provide the means of downloading code either directly into an EPROM device or provide a port for transferring this code to an external PROM programmer. The MK48Z02 will of course not work in an EPROM programming circuit because of the high voltages requires for EPROM write cycles.

Figure 1 shows an inexpensive circuit, however, that can be used for transferring code from an EPROM (master) to an MK48Z02 (copy). (If data already exists in an MK48Z02 it also can be used as the master, because read cycles of the MK48Z02 and EPROM devices are similar). This circuit uses an oscillator and counter to step through all address locations in a binary sequence. The first phase of the clock (positive cycle) generates the write pulse. The second phase of the clock (negative edge) is used to clock the counter circuit to the next address. Once all addresses have been accessed, the next cycle will set a latch that resets the circuit and lights a finished light. Pushing the start button resets the latch and starts the sequence from the beginning. A switch going to V_{CC} on the master and copy sockets is provided so that V_{CC} can be removed when inserting or removing devices to insure maximum data security. Removing V_{CC} from the MK48Z02 will deselect the device making all other inputs don't care, therefore intermittent contact to the socket when inserting or removing devices will not generate spurious write cycles.

Verification of data should not be a significant issue because the MK48Z02 does not suffer from programming yield problems like EPROM devices do. However, if a device is suspected of having faulty code, verification can be accomplished on the EPROM programmer IN THE VERIFICATION MODE ONLY (caution : check with the manufacturer of the programmer to make sure no high voltages are applied to the device in the verify only mode).

There is no limit to the number of times the MK48Z02 can be programmed, and the MK48Z02 does not need to be erased before it can be programmed.

MK48Z02 Inexpensive Programmer

- Power Supply
  - 12V, 500mA
  - sleeve negative, tip positive input.
- Fuse : 1A, 250V.
- LED Busy indicator.
- Copy time under 5 seconds.
- Test sockets for easy insertion and extraction.

Operation

1. Plug the AC or DC adapter into the coaxial power input, making sure that the polarity is correct, and plug in the power supply.
2. Make sure that the power switch is in the OFF position before inserting the chips.
3. Raise the levers on the test sockets, and insert both chips with the indicator dots on the same side as the levers.
   Securely clamp the levers down all the way.
4. Switch the power ON.
5. Depress and release the start button. The busy light will stay lit for about 4 seconds as the chip is being copied.
6. When the light has turned off, switch the power off before releasing the levers on the test sockets and removing the chips.
7. Store the chips in anti-static foam.

Troubleshooting

If the MK48Z02 Programmer is not functioning properly, take the following steps :

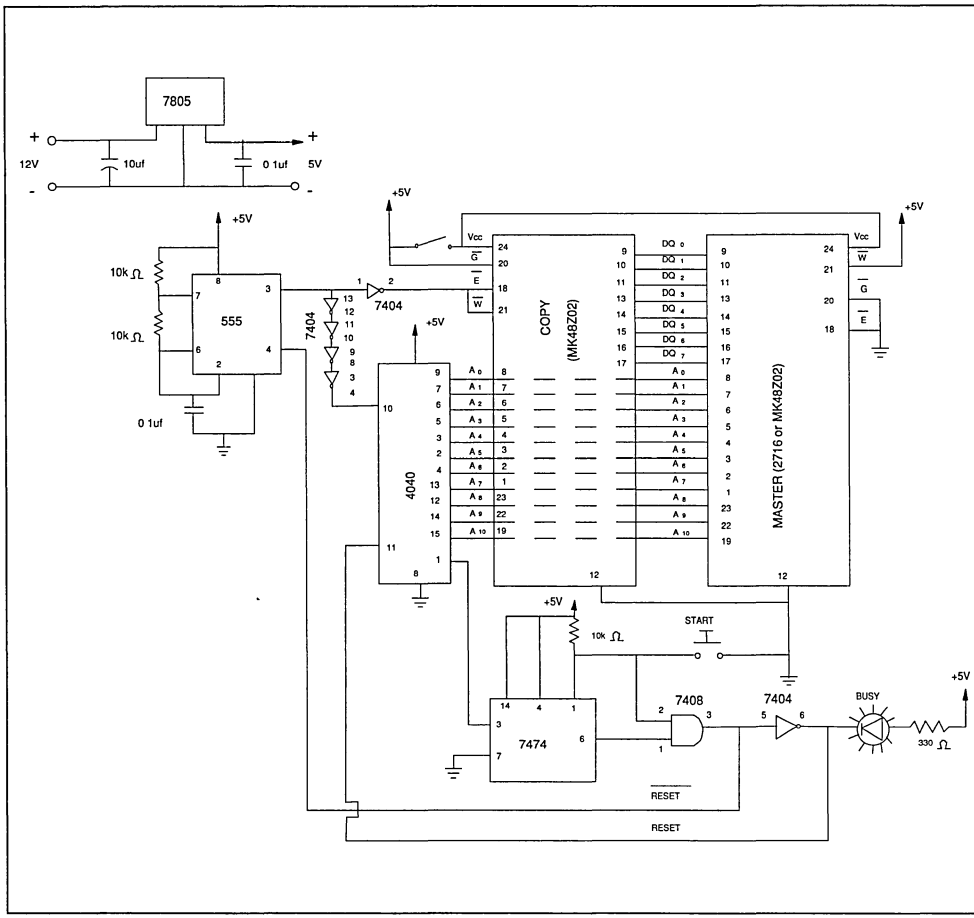
Check the fuse and replace if blown.

Make sure the polarity on the power supply is correct. (sleeve negative, tip positive).

Follow the operating instructions through step by step.

Remove the bottom of device and make sure all chips are securely in their sockets.

Figure 1. Inexpensive MK48Z02 Programmer



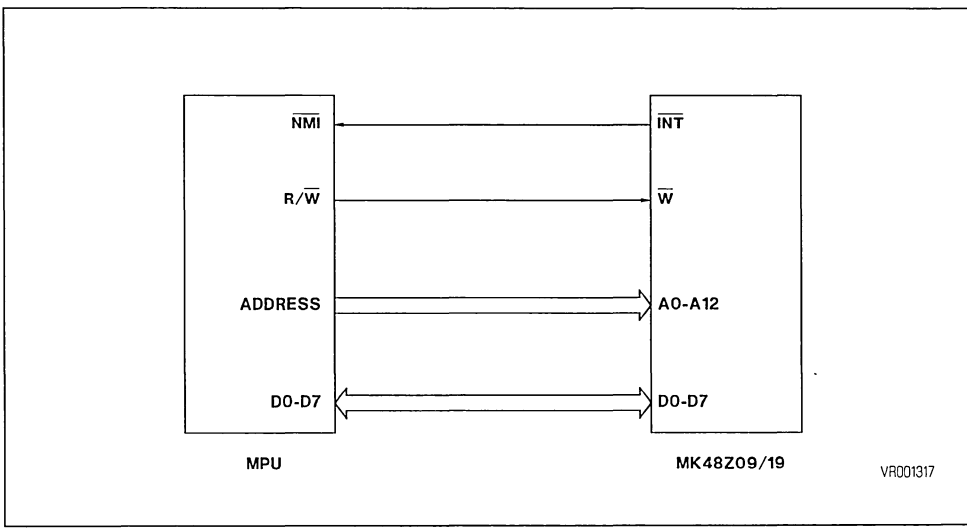
POWER FAIL INTERRUPT OF THE MK48Z09/19

A frequent dilemma faced by system designers is how to handle a power failure. Because power fail sensing components add real estate and cost to the system, some designers choose not to implement a power fail routine, allowing "the chips to fall where they may". This approach is frequently rationalized given the in-frequency of power failures and the industry drive to minimize circuit board space. It does not however represent an ideal solution. Other designers have gone to great expense to design a power fail sensing circuit only to find it difficult to control voltage trip points and experience timing requirements that are hard to predict.

The MK48Z09/19 provides a solution to the power fail dilemma. While occupying no more board area than conventional memories of the same density, the MK48Z09/19 also offers a power fail interrupt output pin along with nonvolatile memory. Because the voltage trip point of the interrupt signal on the MK48Z09/19 is temperature compensated, the user can be assured that its operation remains within specifications over the entire temperature range. The MK48Z09/19 also provides predictable timing. The amount of time between an interrupt low and a power fail write protect condition is a function of an internal oscillator within the MK48Z09/19 and therefore is independent of what may be happening at the system level. The only restriction imposed on the user is that a minimum V_{CC} fall time not be exceeded. The minimum V_{CC} fall time is, however, easily within the normal V_{CC} fall time characteristics of most applications.

The power fail interrupt pin of the MK48Z09/19 is open drain and can be easily implemented by connecting the interrupt signal to a non maskable interrupt input on the microprocessor used, thus initializing a short power fail routine. Because the MK48Z09/19 is battery backed up, the power fail routine can store important data and parameters. Sign off to data communication links and notification of a local power failure to supervisory systems are also applications made possible to the local controller through the use of the power fail interrupt.

Figure 1. Suggested MK48Z09/19 Hook Up



POWER FAIL CONDITIONS

The MK48Z09/19 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point of the MK48Z09/19 an interrupt is immediately generated. An internal clock provides a delay no less than 10µs but no greater than 40µs before automatically deselecting the MK48Z09/19.

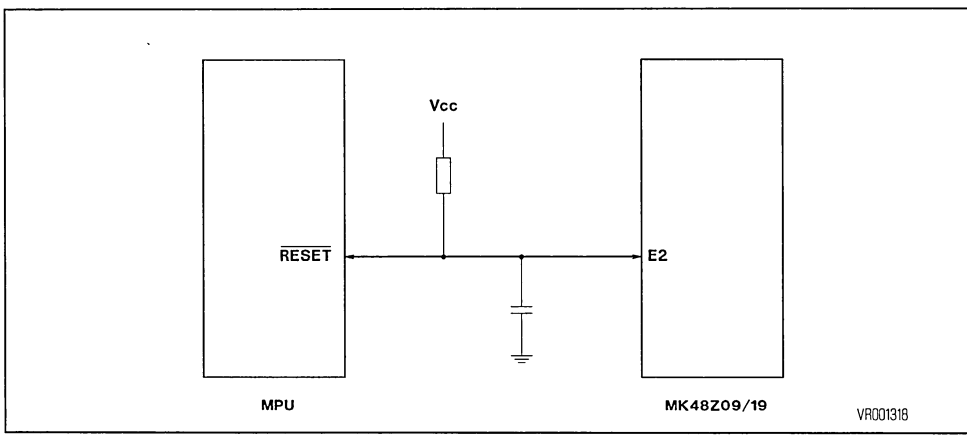
With V_{CC} allowed to fall at its maximum rate from 4.75V to 4.5V in 300µs (833V/sec), a delta voltage between when a power fail is detected and the device is deselected will be established. Because the maximum V_{CC} fall rate and maximum delay between power fail detect and deselection are given values, this delta voltage can be easily calculated 40µs * 833/V = 48mV). Therefore final testing of the MK48Z09/19 at SGS-THOMSON can assure the user that the device will be deselected no lower than the specified Power-Fail Deselect (VPFD min) level, provided that the maximum V_{CC} fall rate is not exceeded.

With V_{CC} fall times that stretch over a long period of time, the voltage at which an interrupt is generated and the voltage at which the MK48Z09/19 automatically deselects will approach the same value. Once again final testing at SGS-THOMSON can assure the user that a power fail detect or deselection will occur no higher than the specified Power-Fail Deselect (VPFD max) level.

POWER UP CONDITIONS

The MK48Z09/19, like most NVRAMs, provides automatic write protection under low voltage conditions. Unfortunately, many processors generate spurious cycles during power up, despite V_{CC} being within spec. Some processors even continue to behave erratically though their reset pin is being held low, until the system clock has had time to wake up and produce sufficient cycles to clear the processor. The MK48Z09/19 makes it easy to combat this problem by providing an active high E2 input (chip select). This input when tied to the reset line will lock out the MK48Z09/19 during the power on reset time, protecting the data in memory from being inadvertently over written with erroneous data. Figure 2 illustrates a simple power up reset scheme.

Figure 2. Write Protect Application of E2 Input



Notes :

1. Although trip points are tested by holding V_{CC} to given DC levels, the device is by no means in a static state. Address, data lines, and control lines are all toggling. A series of complex patterns are input to the device to ensure that worst case noise conditions generated within the MK48Z09/19 will not affect trip point performance.
2. With even the slowest MK48Z09/19, the 250ns device, and the minimum 10µs advanced warning of a deselect condition, there is enough time for 40 memory cycles to take place. The amount of MPU cycles that can take place will of course vary according to the processor used and programming techniques.
3. The MK48Z09/19 can provide an inherent safe guard against a "Brown Out" condition i.e. V_{CC} that droops or slowly fades below spec. or operational limits and then comes back up. Applications requiring the interrupt pin to remain low until a completion of a sequence of events (within 10µs), can relay on the MK48Z09/19 not to interrupt the sequence should power unexpectedly return. Once a power failure is detected and the interrupt pin goes low, the interrupt pin will remain low for the full 10µs to 40µs period and the device will be accessible during this time. Therefore the power fail interrupt application can not be aborted mid cycle. After the interrupt time period the interrupt pin will go high, should V_{CC} rise in the interim, allowing normal operation to resume. The MK48Z09/19, however, waits for a minimum of 30µs to a maximum of 120µs from the time interrupt goes high until another power fail can be selected. (Should V_{CC} remain at a level very close to the trip point for an extended period of time, a number of power failures could be detected due to noise on the V_{CC} line. Interrupt will always follow the above timing however).

TIMEKEEPER CALIBRATION OF THE MK48T02

The term "quartz accurate" has become a familiar phrase used to describe the accuracy of many time keeping functions. Although quartz oscillators provide an accuracy far superior to other conventional oscillator designs they are, however, not perfect. Quartz crystals are sensitive to temperature variations. Figure 1 shows the relationship between temperature and accuracy of the 32.768khz crystal oscillator used on the MK48T02 TIMEKEEPER™. Variations in resonant frequency from one crystal to the next also exist, although these variations typically do not exceed 20ppm (approx. 1 min. per month).

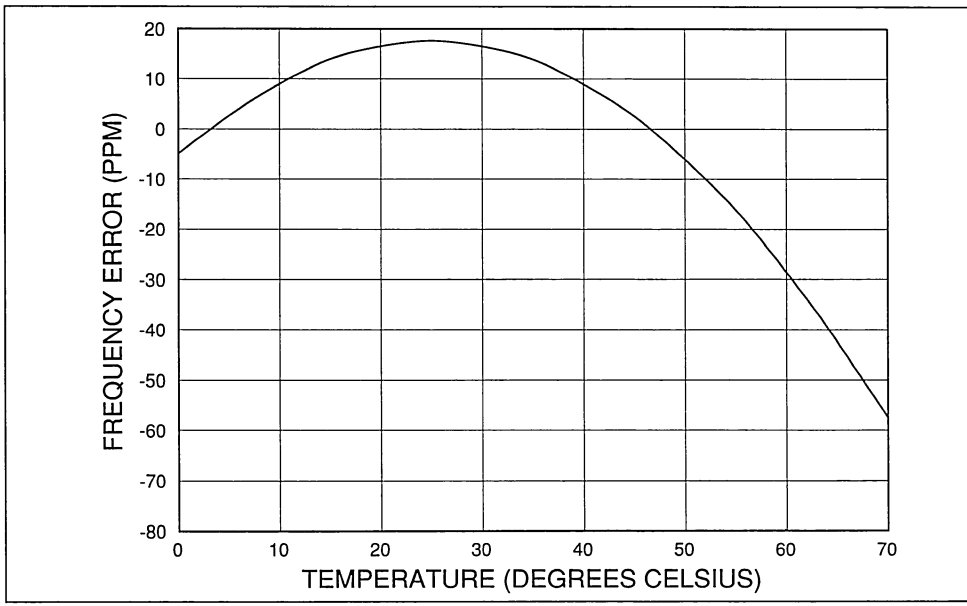
Clocks used in applications requiring a greater accuracy of 1 min. per month or have an ambient temperature that is not centered around room temperature (25°C) will need a means of calibration.

Typically, most crystal oscillators are calibrated by adjusting the load capacitance of the oscillator. This method, while effective, has several disadvantages.

1. It requires external components.
2. It requires the use of test equipment (fre- quency counter).
3. It can increase oscillator current (an important factor in battery backed-up applications).

At SGS-THOMSON Microelectronics, we believe these disadvantages are unacceptable. The MK48T02 calibrates its clock by adding or subtracting pulses from the clock chain in a predictable manner (periodic counter correction). This method can be employed under software control eliminating the disadvantages of the previously stated method and making it end user friendly.

Figure 1. Typical MK48T02 Oscillator Frequency vs. Temp.



TWO METHODS FOR CALCULATING CALIBRATION

There are two methods for establishing how much calibration will be required in a given application. The first method can be easily implemented in the user environment allowing the average ambient temperature be taken into consideration. The other method provides a fast means of calibration at the OEM site.

Empirical In System Method

This method involves setting the clock to a known standard and then comparing at a fixed time later. The longer the time period the greater the accuracy. When setting the clock, all counters in the 32.768khz to 1 second divider chain start from zero as soon as the write bit is released. Therefore, it is possible to set the clock to the standard within the response time of the system.

How to calculate the amount of calibration necessary.

N = number of seconds in the time period

T = number of seconds elapsed on the MK48T02

X = error in parts per million

X = (T-N)/N * 1E6

Notes :

1. Setting the sign bit does not indicate a ones complement number. Setting the sign bit speeds up the clock.
2. Each bit in the calibration bits represents a change of 2.034 parts per million.
3. Depending upon when the MK48T02 is read with respect to an update a one second error can occur. Make sure the time period for calculations is long enough so that this error becomes negligible.

Frequency Test Method

This method is best suited for use at incoming inspection on a sophisticated tester or on a bench set up. It is not practical for in system use unless a means for latching address and control lines can be implemented because the device must be held in a read state for and indefinite period of time.

Procedure for frequency test method.

1. set write bit.
2. set FT bit (DQ6 for day register).
3. reset write bit.
4. set address to seconds register and control lines for a device read.
5. measure 512hz frequency at DQ0.
6. set write bit.
7. reset FT bit.
8. set correct time and calculated calibration.
9. reset write bit.

Notes :

1. Instruments for measuring frequency should be accurate to 1 ppm for reasonable results.
2. Error in ppm = (frequency measured-512)/512 * 1E6.
3. Failure to reset the FT bit will result in gross timekeeping errors.

TIMEKEEPER CONTROL REGISTER

The control register of the MK48T02 serves three separate functions, all within the same byte of data. It allows the user to write time (write bit), read time (read bit) and calibrate the clock. When writing or reading the clock care should be taken not to disturb the calibration data.

When setting the write bit, data contained in the calibration bits will be entered into the calibration circuitry. Care should be taken to ensure this calibration data to be valid.

When setting the read bit, data contained in the calibration bits will be entered into memory only. This may seem harmless, however, it should be noted that the calibration data is not refreshed with a clock update. Therefore any record of valid calibration data will be lost if valid calibration data is not included with the read bit. This is important because valid calibration data is needed when setting the write bit.

Procedure For Setting And Resetting The Read And Write Bits

Set Write bit.

1. Read contents of Control Register.		00XXXXXX
2. Logical OR contents with the number 128.	OR	10000000
3. Load results into Control Register.		10XXXXXX

Reset Write Bit.

1. Read contents of Control Register.		10XXXXXX
2. Logical AND contents with the number 127.	AND	01111111
3. Load results into Control Register.		00XXXXXX

Set Read Bit.

1. Read contents of Control Register.		00XXXXXX
2. Logical OR contents with the number 64.	OR	01000000
3. Load results into Control Register.		01XXXXXX

Reset Read Bit.

1. Read contents of Control Register.		01XXXXXX
2. Logical AND contents with the number 191.	AND	10111111
3. Load results into Control Register.		00XXXXXX

Example BASIC program.

```
10 REM CONTROL REGISTER LOCATION
20 A = 2040
30 REM SET WRITE BIT
40 POKE A, PEEK (A) OR 128
50 REM RESET WRITE BIT
60 POKE A, PEEK (A) AND 127
70 REM SET READ BIT
80 POKE A, PEEK (A) OR 64
90 REM RESET READ BIT
100 POKE A, PEEK (A) AND 191
```

MEMORY MAPPED TIMEKEEPER REGISTERS OF THE MK48T02

Although software is usually thought of as being flexible, there can be applications where the memory management of the system defines how the memory will be utilized. Because the TIMEKEEPER™ registers of the MK48T02 reside within a predetermined position within the memory map, this may present a problem in these applications. Fortunately there are easy solutions to this problem.

There are several options possible for moving the location of the TIMEKEEPER registers within memory. The first option involves inverting one, all, or any combination of the eight most significant address lines of the MK48T02. Figure 1 shows an example of how inverting address A10 will move the apparent position of the TIMEKEEPER from the top of the device memory to the middle of device memory (from 7F8-7FF to 3F8-3FF).

Another option is to use higher order address lines (above A10) to decode the chip enable input of the MK48T02, therefore moving the apparent location of the entire MK48T02 within memory. Figure 2. shows an example of how this can be done. With this technique the TIMEKEEPER registers will remain in consecutive locations. Combinting options can place the TIMEKEEPER registers in any block of eight bytes of memory.

Finally, a third option would be to bank select the MK48T02. This method would allow the TIMEKEEPER to become transparent to memory directly accessible from the processor. Implementing a bank select requires generating a pseudo address line or lines that can be decoded with other address information to select the appropriate memory. The most convenient method for creating this pseudo address is to use an output port for this purpose. Microcontrollers have these ports on board while Microprocessors require a PIA chip to accomplish I/O functions. Figure 3 shows a typical Microprocessor to PIA combination that utilizes an I/O port to bank select memory. The I/O port can be programmed high or low by loading a register within the PIA. The PIA chip is selected by decoding IOREQ (I/O request). IOREQ also disables main memory and the MK48T02.

Figure 1.

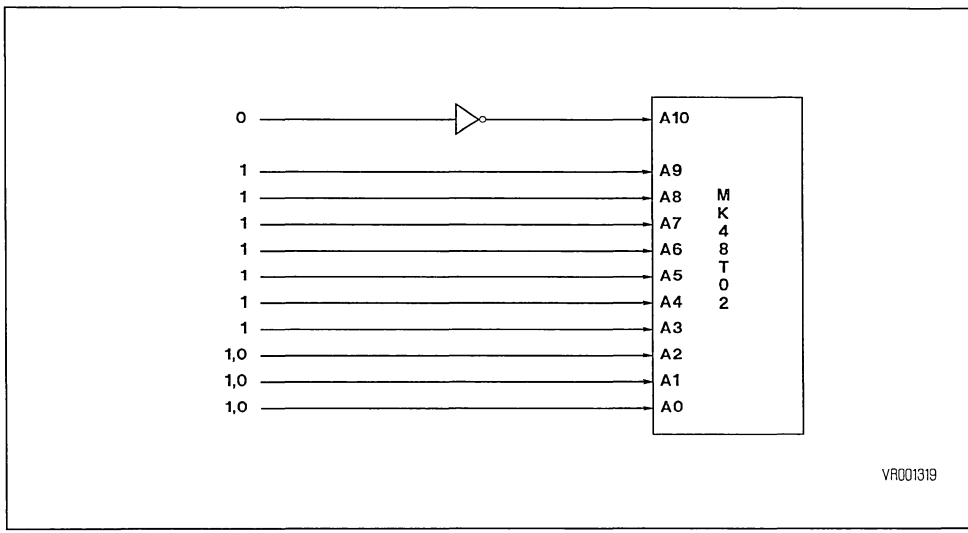


Figure 2.

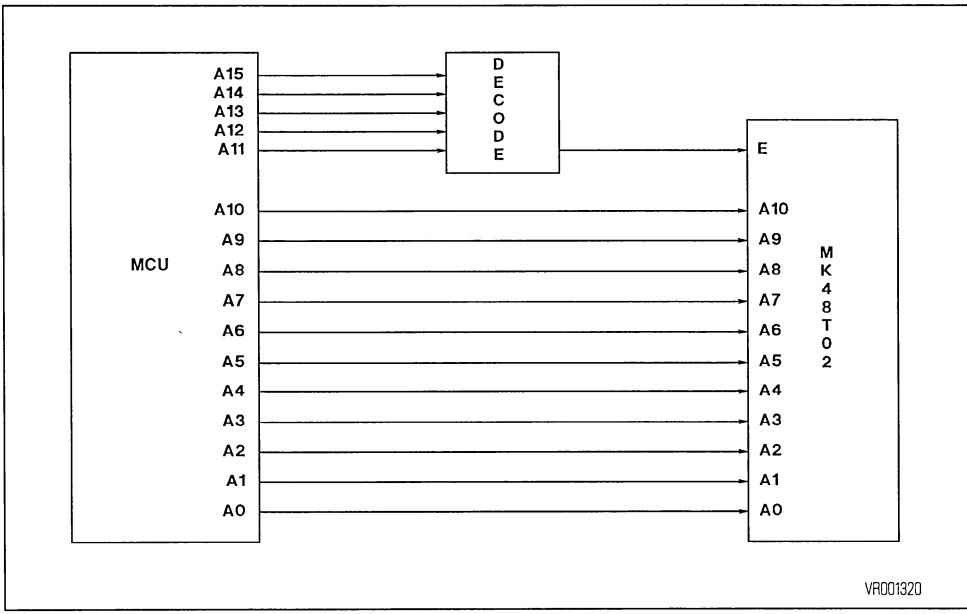
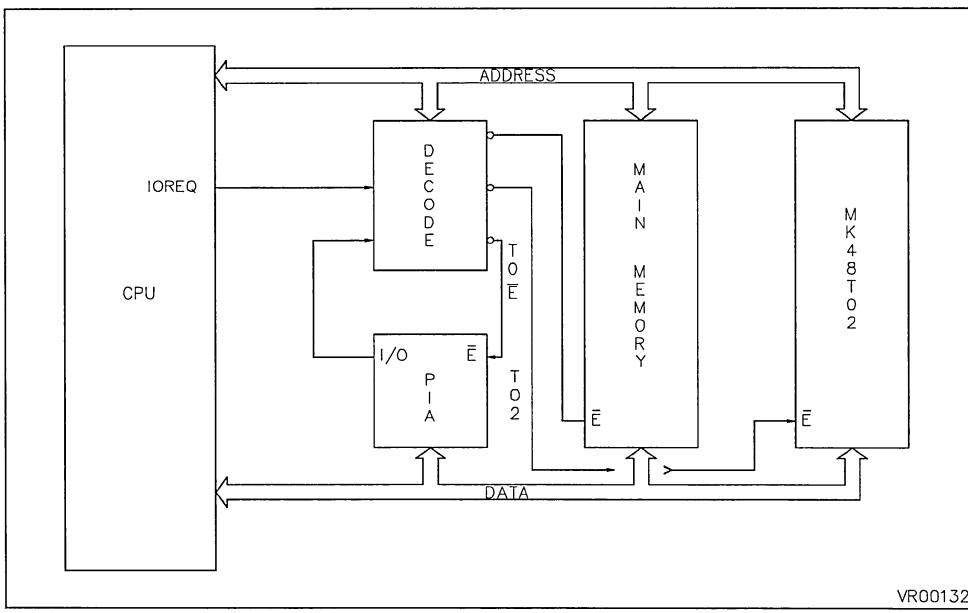


Figure 3.



THE MK45H03 BiPORT FIFO 16-BIT TO 8-BIT CONVERSION

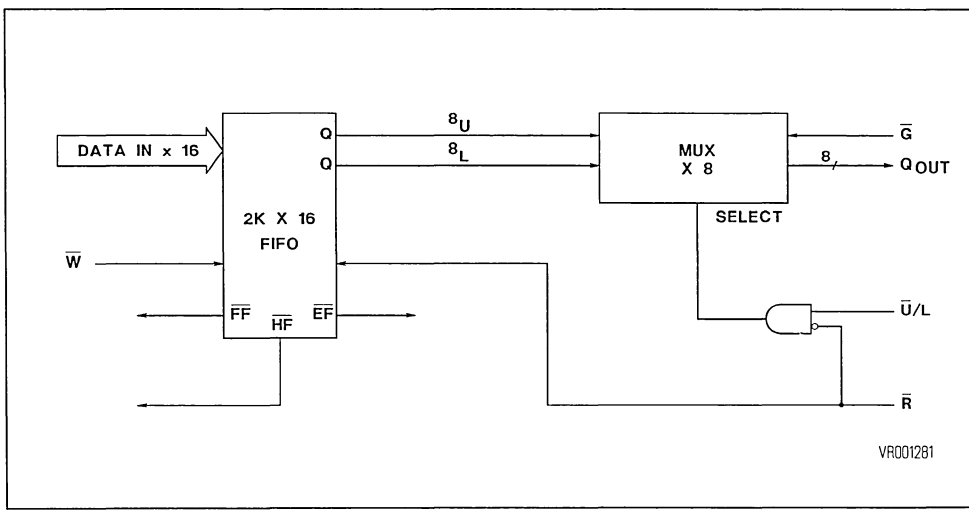
INTRODUCTION

When SGS-THOMSON Microelectronics introduced the MK4501 in 1983, it was the first high density FIFO with a BiPORT™ memory cell architecture. The MK4501 quickly became the industry standard with an organization of 512 x 9 bits, and included both an Empty and Full status flag. SGS-THOMSON has extended this technology to develop a device with four times the density - the MK45H03. The MK45H03 has a 2K x 9-bit organization, and includes the addition of a Half Full ($\overline{HF}$) status flag, as well as the Empty and Full status flags. Its BiPORT™ RAM cell design allows simultaneous and asynchronous Write/Reads, and avoids the added ripple-through delay times of conventional shift register based FIFOs. As with the MK4501, word with and depth expansion is easily achieved by using the $\overline{XI}$ and $\overline{XO}$ pins. The MK45H03 is pin-for-pin compatible with the MK4501 and MK45H01, and thus can be used as a density upgrade in many applications.

CIRCUIT DESCRIPTION

As shown in Figure 1, the block diagram for this application concept shows an example of how to interface a 16-bit Microprocessor to an 8-bit peripheral. Due to the MK45H03's architecture, which provides easy width expansion, we can interface two MK45H03 FIFOs to a 16-bit Microprocessor for collecting and holding our data dumps. By using a small amount of additional logic, we can retrieve this data in consecutive 8-bit bytes. (The diagram in Figure 2 shows the basic idea in an equivalent circuit). Using the two MK45H03 FIFOs, we start with a 2K x 16 memory buffer as our input, and convert it to a 4K x 8 memory buffer output. The status flags will keep us updated to let us know when we are Full ($\overline{FF}$ = low), or Empty ($\overline{EF}$ = low). The Half-Full status flag ($\overline{HF}$ = low) will help to avoid those sudden unpredicted halts, for example, should there not be adequate block memory space available. We will also take advantage of the asynchronous and simultaneous Write/Read capability of the MK45H03's BiPORT™ design.

Figure 1. Block Diagram



CIRCUIT OPERATION

The schematic diagram in Figure 3, shows that we will be writing 16-bit words designated as UPPER and LOWER 8-bit bytes, and then reading first the UPPER 8-bit byte, and then the LOWER 8-bit byte. As with all FIFO applications, we must start with Reset ($\overline{RS}$) to initialize the circuit. Remembering that upon reset our $\overline{EF}$ output goes active low, all Read cycles are ignored until the first Write cycle has been completed. Once a succesful Write has been performed, the $\overline{EF}$ output will go inactive high. The ideal operation would allow the Write count to remain at least one cycle ahead of the Read, thus avoiding $\overline{EF}$ from being asserted active. Referring again to Figure 3, the A/B select to the data multiplexers via Q of the D-type flip-flop, alternates at the **end** (rising edge) of each Read to get ready for the next Read cycle. This avoids additional gate delay time, as well as providing a READ strobe during the full $\overline{R}$ pulse width. Therefore, after Write, and upon the first Read, we access the UPPER byte ($Q_{A\ 0\text{-}7}$), and alternate thereafter between the LOWER ($Q_{B\ 0\text{-}7}$) and UPPER byte with each consecutive Read. The flag status needs only to be taken from the LOWER byte FIFO since it will be Read last, and both are written simultaneously. Of course an (Empty - 1) function could be implemented on the 8-bit side by using the Empty Flag output from the UPPER FIFO.

In this application we have included data bus control with a fast external Output Enable ($\overline{G}$) on the multiplexer. The waveform timing diagram is referenced in Figure 4. Since there will be a specific Q-valid access time from the enabled FIFO to the data inputs of the multiplexer, the $\overline{G}$ input can be tied to the $\overline{R}$ system input without any penalty. The timing diagram in Figure 5 displays the typical access times to be considered. For example, t_{A1} is the combined access time of the OR gate plus Read access (t_A) of the MK45H03. Further definitions are : t_{A2} = MUX Q-Valid access time, t_{A3} = MUX Q-Valid access time from $\overline{R}$ asserted low, t_{GLQV} is MUX $\overline{G}$ (Output Enable) access to Q-Valid, t_{OH1} = Q-Hold time of the FIFO, t_{OH2} = Q-Hold time of the MUX, and t_{GHQZ} is output Enable to High Z. It should be noted that t_{A3} is equal to ($t_{A1} + t_{A2}$), where the limiting factor is t_{A1} not t_{GLQV}, when $\overline{G}$ = R (see Figure 5).

CONCLUSION

This implementation presumes that Read strobes will be halted when the lower MK45H03 indicates itself empty. In this example, should the lower FIFO become empty, additional Read strobes will continue to toggle the select D-type flip-flop even though the FIFOs will not respond. Should Read-while-Empty compatibility be required, then additional logic will be needed to disable the select flip-flop when the lower FIFO is empty.

Figure 2. Equivalent Circuit

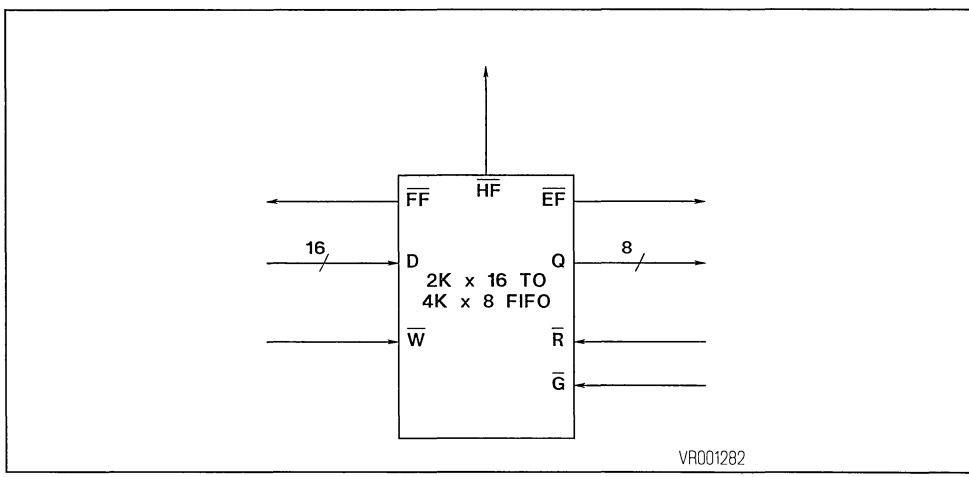


Figure 3. Asynchronous 16-Bit to Asynchronous 8-Bit Schematic

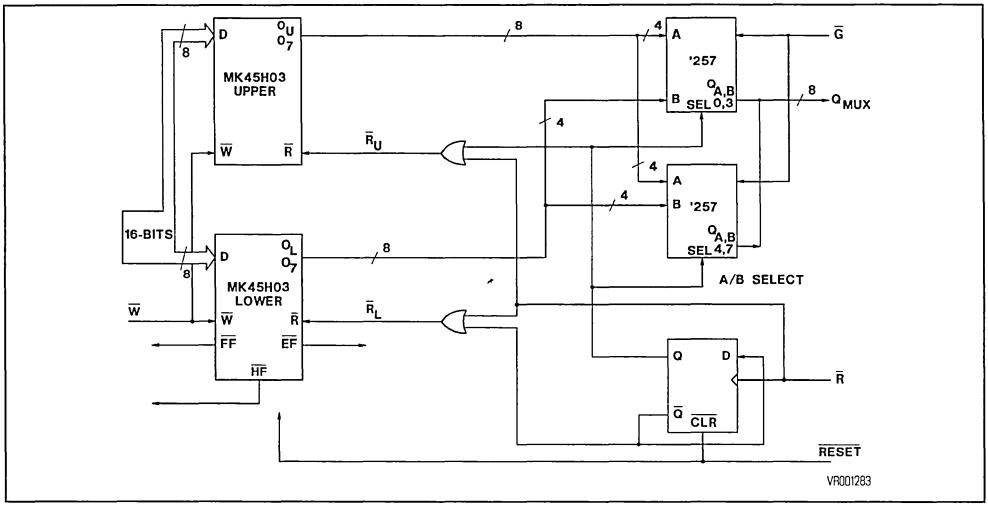


Figure 4. Timing Diagram

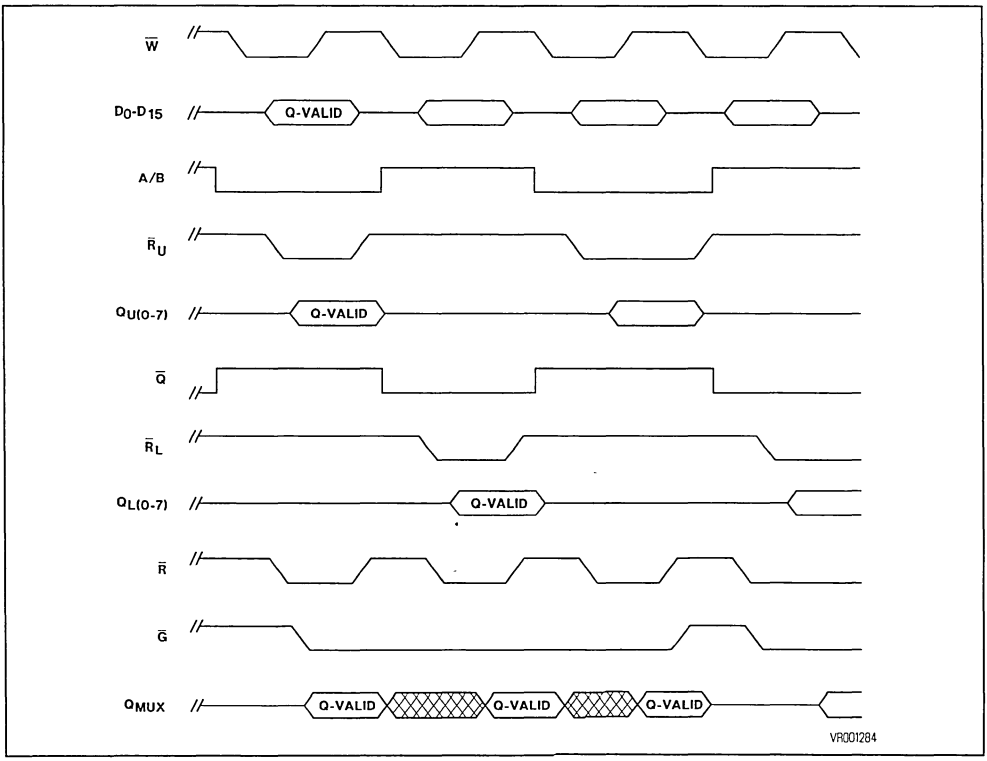
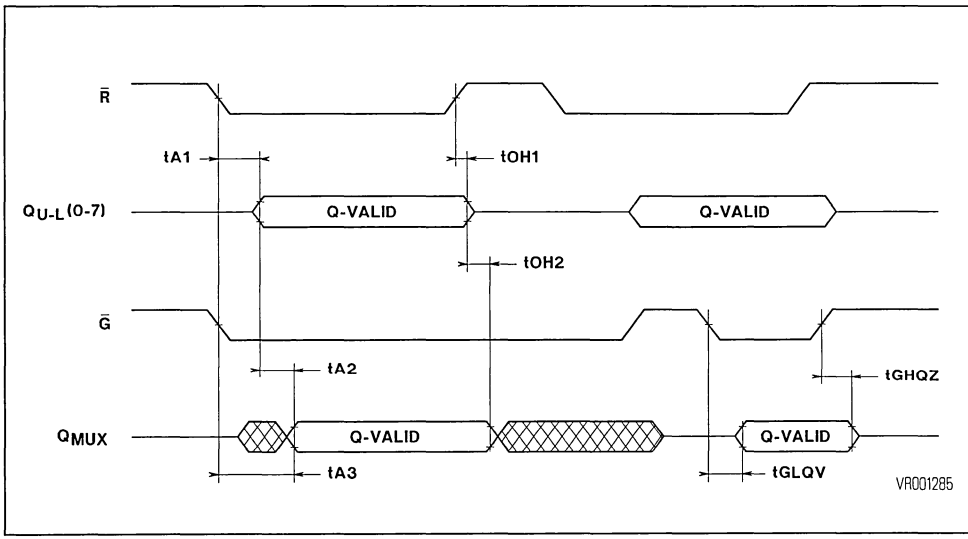


Figure 5. Access Times



MICROWIRE EEPROM COMMON I/O OPERATION

Bernard SABY

SGS-THOMSON Microelectronics provides a wide range of serial access EEPROMs. The MICROWIRE™ product line is designed for a 4-wire interface: SK the Clock input, CS the Chip Select Input, DI the Serial Data Input, and DO the Serial Data Output. Some MCUs such as the SGS-THOMSON ST9 or ST7 series include a Serial Peripheral Interface (SPI) "on-chip", that can fit this MICROWIRE interface, but those EEPROMs can be used with any general purpose microcontroller where the interface wires are hooked to I/O ports or some equivalent circuitry.

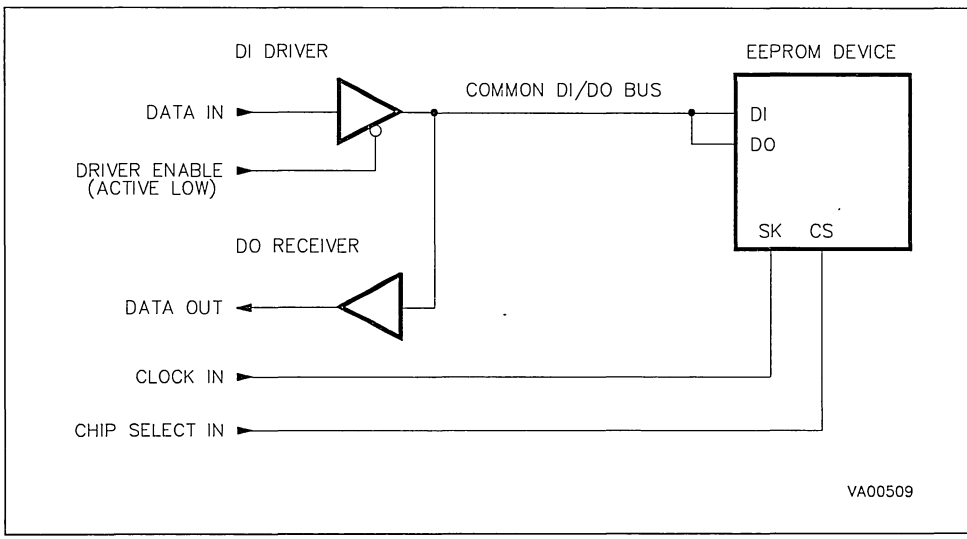
Since DO output is in high impedance while instructions, addresses and data are shifted into the DI serial input, it seems attractive to tie DI and DO pins together to provide a common DI/DO bus. The chips can operate correctly in this configuration, provided that appropriate design rules are carefully followed. The possible troublesome situations are limited to the instructions where DO output is activated.
Such instructions include: READ,WRITE, ERASE, WRAL and ERAL.

This note reviews and details the specific points where precautions must be taken in common DI/DO applications. In order to provide the designer with a safe-design guide, all calculations are carried out upon the worst case values as specified in the data sheet of these EEPROM devices.

READ INSTRUCTION

Let's consider a typical common DI/DO application (as in Figure1). The DI driver and the DO receiver can be discrete logic or part of a microcontroller I/O port or any equivalent circuitry.
DO pin is in high impedance while the READ opcode and the address bits are clocked into the chip upon the rising edge of SK clock. These bits must be kept valid for a minimum hold time of t_{DIH}: see data sheet. However, upon the rising edge of SK where the last address bit (A0) is clocked into DI, the DO pin comes out of high impedance and outputs the leading bit (logical 0) which precedes the 16 bit data string (see example in Figure 2).

Figure 1. Typical Common DI/DO Application



The maximum delay between the rising edge of SK and the leading "0" bit is specified for a maximum of t_{PD0} (between 500 ns and 1µs, depending on the product); nevertheless, typical values of less than 100 ns can be found.
Since the DI driver must remain enabled with the A0 bit for a minimum of t_{DIH} (hold time) before being disabled, a bus conflict will occur if the A0 bit is a "1" (odd address registers). The consequences are:

- a low impedance path is created between V_{CC} and ground through DI driver and the on-chip DO out-

Figure 2. Read Instruction Example

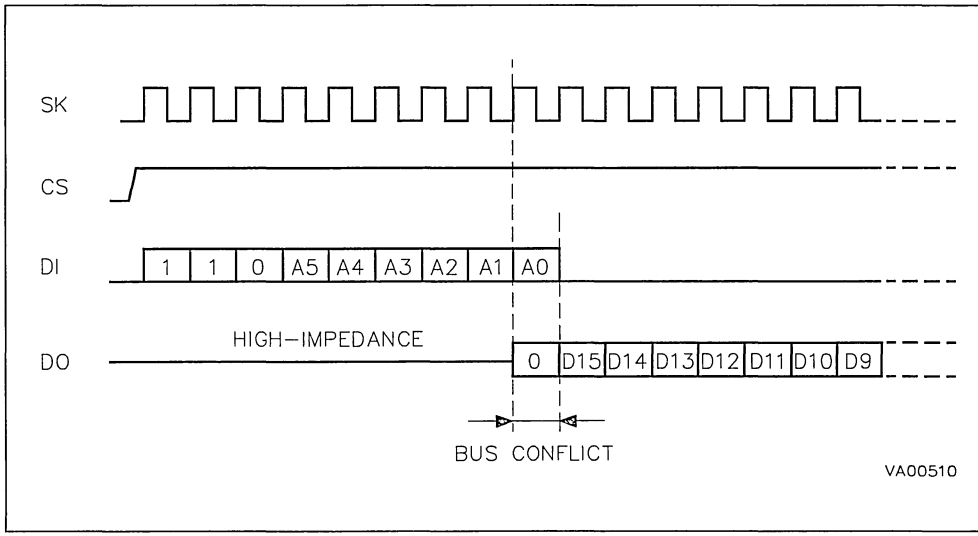
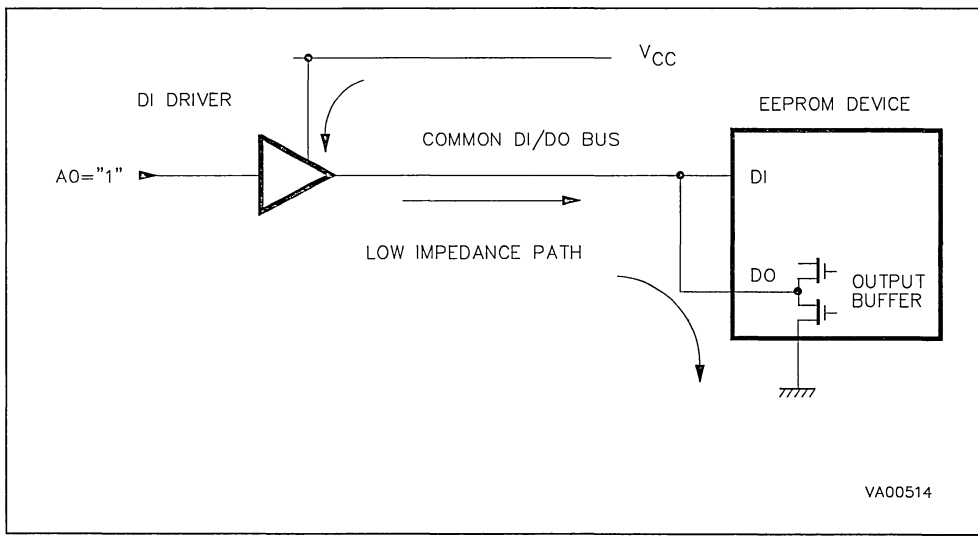


Figure 3. Short-Circuit between V_{CC} and Ground



put buffer (see Figure 3); this short-circuit may produce glitches on the power supply which can disturb all the circuits on the board;

- the logical level on the DI/DO bus is not well-defined as it is the result of the relative driving capability of the DI driver and the DO output buffer; the DI pin can even see a logical "0" preventing the access of the odd address registers.

This trouble can be solved by inserting a current limiting resistor in the sinking current path. Figure 4 shows some possible locations for this resistor; however, the best location is between the DO out-

Figure 4. Possible Locations for the Current Limiting Resistor

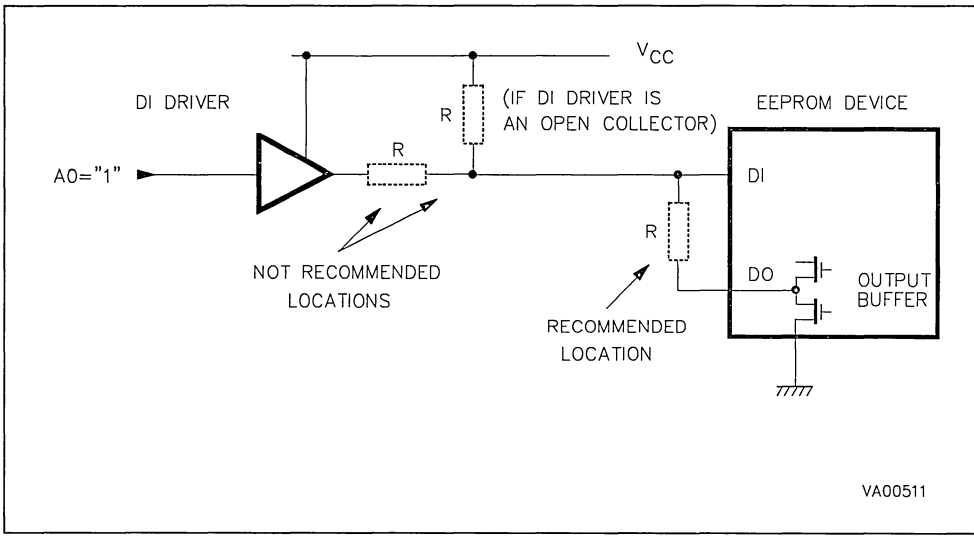
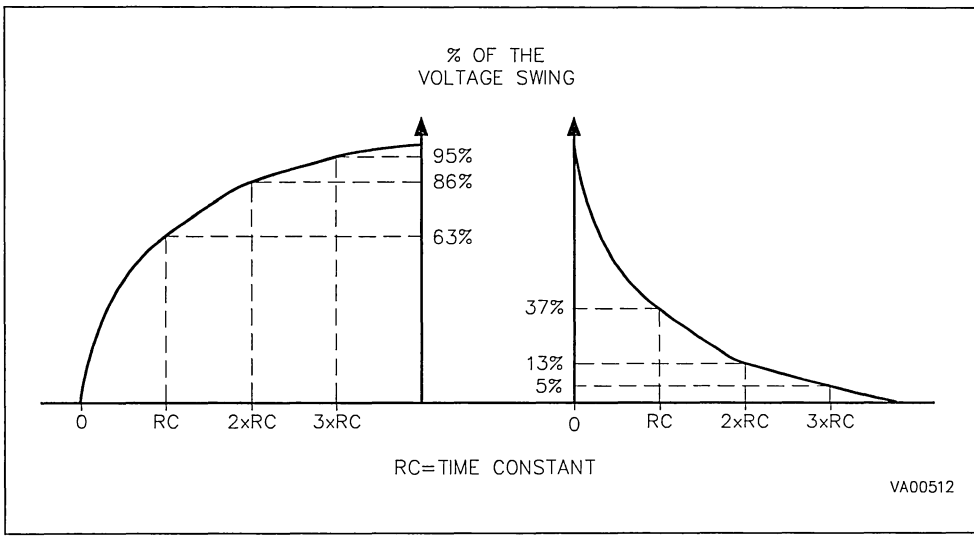


Figure 5. Exponential Charge and Discharge of the Bus Capacitance



put and the DI/DO bus for the following reasons:

- during the overlap time, the logical level on the DI/DO bus will be defined by the DI driver only, allowing the respect of the t_{DIH} hold time specification.
- as we discuss later, the R resistor slows down the propagation time of the DO output signals on the DI/DO bus, but only the 16 bits of data read from the chip are affected. If R were in series with the DI driver, all the input signals for all the instructions would be slowed down in the same way.

The R resistor doesn't have any effect as long as DO is in high impedance. During the execution of a READ instruction, R sinks some current from the DI driver during the short overlap time; then the DI driver is disabled and DO output takes control of the DI/DO bus through the R resistor.
Because of the bus capacitance C, the signals are distorded: the rising and falling edges of DO output are transformed into exponential curves whose shape depends on the time constant RC (see Figure 5).

The consequence is: after a rising edge of SK clock, the logical level on the DI/DO bus needs some delay before being considered as steadily established and ready to be sampled by the DO receiver. This safety delay can be estimated to be at least 3xRxC; after sampling, the subsequent rising edge of SK can occur.
When applying the results of Figure 5 to the worst case of DO output levels (see data sheet): V_{OH} min = 2.4 V, V_{OL} max = 0.4 V, Voltage Swing = 2 V, the DI/DO bus levels will be:

- logical "1" = 2.3 V minimum for a delay of 3xRC
- logical "0" = 0.5 V maximum after SK rising edge

It will be necessary to reduce the SK clock frequency when and only when shifting the 16 bits of data out from the EEPROM. All other operations can be performed at the nominal clock rate.

This reduction is of course directly related to the RC time constant of the DI/DO bus. Figures 6, 7, 8 show some experimental examples replotted from the scope with different values of R and C.

In the last example, the maximum clock frequency is: 1 / 3xRC = 100 KHz, assuming that DI/DO bus is sampled by the DO receiver circuitry just before the rising edge of the SK clock.

In order to avoid an important reduction of the clock frequency, the following techniques can be used which minimize the R and C values:

Figure 6. Oscilloscope Plot, R = 10 kΩ, C = 100 pF, RC = 1 µs

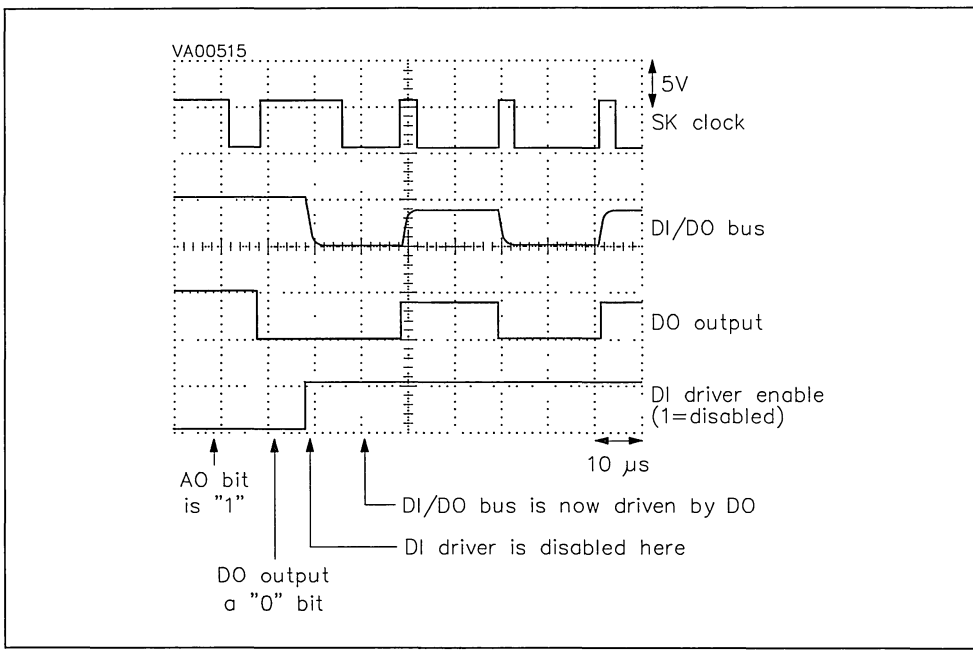


Figure 7. Oscilloscope Plot, R = 5 kΩ, C = 100 pF, RC = 500 ns

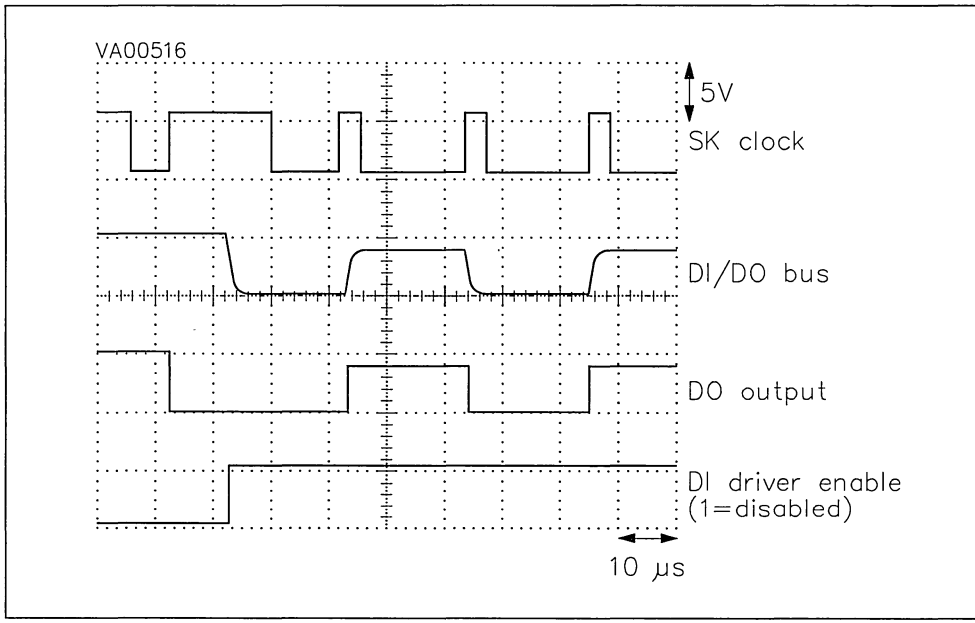
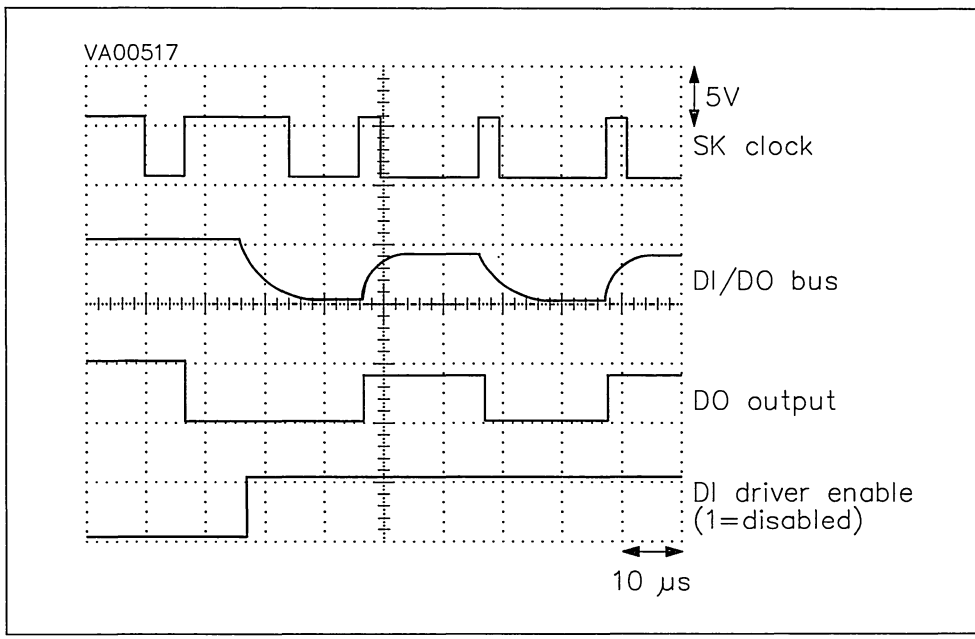


Figure 8. Oscilloscope Plot, R = 10 kΩ, C = 330 pF, RC = 3.3 µs



- to minimize the bus capacitance, it is important to implement the EEPROM device as close as possible to the DI driver/DO receiver circuitry for the shortest connection, and not share too many devices on the same DI/DO bus since the capacitance will be proportionnal to the number of devices connected in parallel to the same DI/DO bus.
- the value of the R resistor can be decreased as long as the DI driver can source the corresponding amount of current during the bus conflict time and as long as the power supply is adequately decoupled to withstand this transient of current. It's up to the designer to decide about the best trade-off based upon his specific application's requirements.

INTERFACE WITH CMOS CIRCUITS

The MICROWIRE EEPROM devices are specified for TTL compatible input/output levels; when using CMOS circuits to interface these devices, some precautions must be taken to ensure the correct interpretation of the logical levels.
Since the CMOS output-high levels are close to V_{CC} and output-low level close to 0V, it is obvious that there are no difficulties in driving the DI, CS and SK inputs of the EEPROM devices.

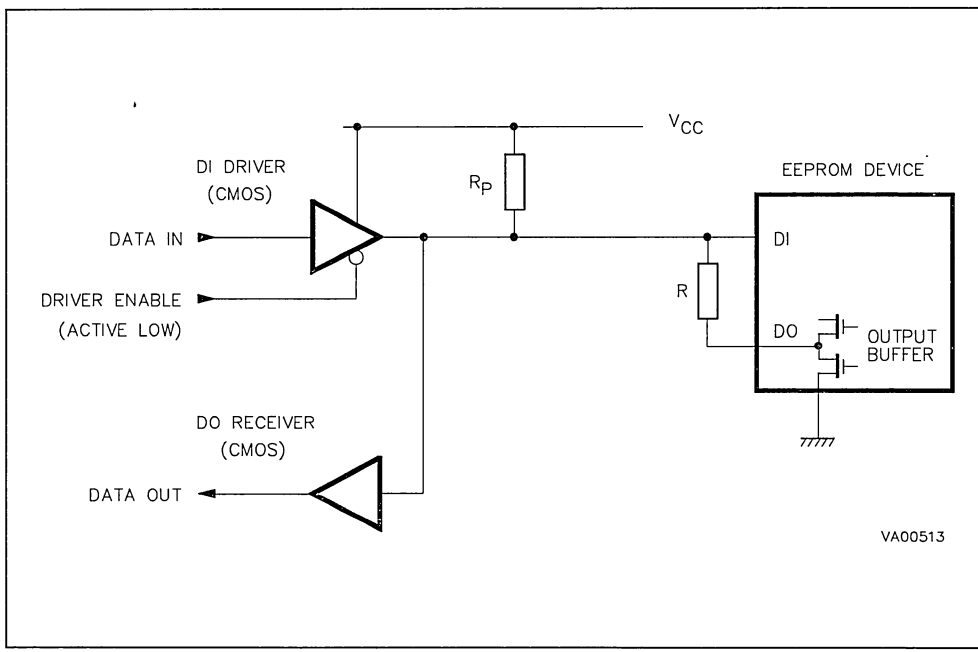
Concerning the DO output, the minimum output-high level is specified to 2.4 V, which is lower than the minimum input high level of CMOS (3.5 V for V_{CC} = 5 V). A common practice is to connect a pull-up resistor Rp between the DO output and V_{CC}, thus increasing the effective high-level in order to meet the CMOS specs.
Although this configuration suits perfectly to a separate DI and DO, it raises some difficulties in common DI/DO applications.
When DO output is a "zero" level, i.e. V_{OL}= 0.4 V, worst case conditions, the R and Rp resistors act together as a voltage divider on the DI/DO bus (see Figure 9); hence, the Rp resistor value must be at least 5 times greater than R value and the "zero" level on the DI/DO bus is:

$$0.4\ V + (5\ V - 0.4\ V) \times R / (R + Rp) = 1.17\ V$$

when Rp = 5xR

Although this value is 330 mV below the 1.5 V, maximum "zero" input level of CMOS, the wide noise margin traditionally associated with CMOS is then significantly reduced.
For a "1" to "0" transition, the DO output on-chip buffer will have to discharge the bus capacitance through the R resistor and to sink some current from the V_{CC} through Rp resistor. In that case, we may

Figure 9. DI/DO Bus Configuration with Pull-up Resistor (Rp)



see that the new time constant is equal to the product of the bus capacitance C with the parallel combination of R and Rp, which is 17% smaller than the one without Rp. However, the steady "0" level is no more 0.4 V, as we assumed for TTL levels but 1.17 V as calculated above (if Rp = 5xR). Despite of this smaller time constant, the voltage swing between "0" and "1" is greater in this case (see later on); hence it is advised before sampling to keep the same "rule of the thumb" delay of 3xRC after the SK clock rising edge.

The major problem is for the "0" to "1" transition. During a first step, the bus capacitance is charged through DO output in series with R and the Vcc power supply in series with Rp. These conditions lead to the same time constant as above (i.e. 17% smaller than the one without Rp).

But once the DI/DO bus voltage reaches the DO output level, the DO on-chip buffer is automatically turned off and the Rp resistor remains the only contributor to the charge of the bus capacitance, resulting into a much higher time constant: RpxC = 5xRxC (if Rp = 5xR).
If we consider the worst case "1" output level for DO (V_{OH}= 2.4 V), it lasts a long time to go up to 3.5 V, which is the minimum "1" input level for CMOS. It will last exactly 0.55xRpC (if Vcc = 5 V) or 2.75xRC after the DO output turn off, and we must add a reasonable noise margin (300 or 400 mV).
As a result: the minimum delay between the rising edge of SK and the sampling of the DI/DO bus should be 2 or 3 times longer than the one we've found for the TTL levels (without Rp), and the clock frequency must be reduced as much.
It is possible to avoid this situation by using a TTL level compatible input CMOS device such as the 74HCTXXX devices as DO receiver circuit, or a CMOS microcontroller that provides a "TTL input levels" option on its I/O ports, such as the ST9 series, and thus get rid of this Rp resistor.

PROGRAMMING MODE: ACKNOWLEDGEMENT OF READY/BUSY STATUS

On the MICROWIRE EEPROM devices, the self-timed programming cycle uses DO output to indicate the ready/busy status of the chip.
The self-timed programming cycle begins with the falling edge of CS at the end of a programming instruction; such instructions include: WRITE, ERASE, WRAL and ERAL.

Figure 10. Oscilloscope Plot, R = 10 kΩ, C = 100 pF, Rp = 50 kΩ

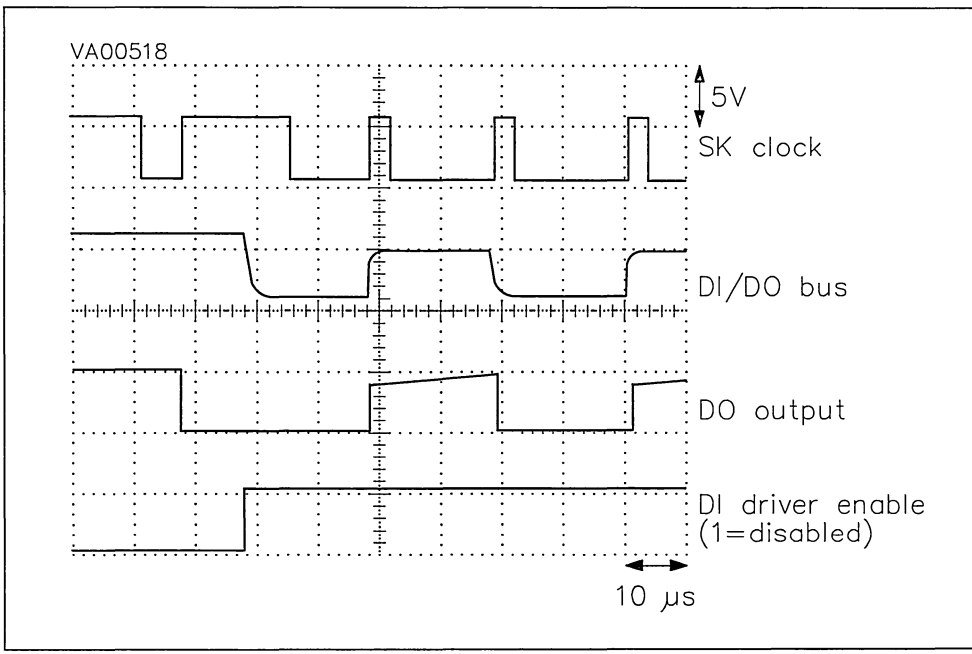
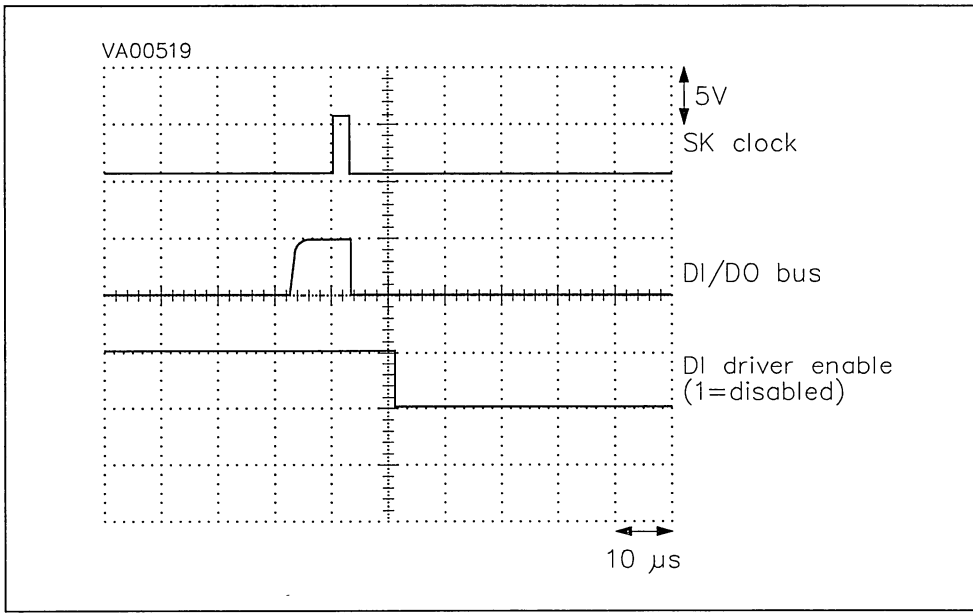


Figure 11. Acknowledge of the Ready/Busy Signal on DO Output



CS pin must be kept low for a minimum of t_{CS} (see data sheet). DO output remains in high impedance as long as CS is low; if CS is brougth high for clocking a new instruction, DO comes out of high impedance state and indicates the Ready/Busy status of the chip (0 = Busy, 1= Ready).
In common DI/DO applications, this may create again a bus conflict; therefore, it is recommended to cancel this status signal: this is very simply done by applying a single clock pulse on SK input while CS is high (see Figure 11).

The operation is scheduled as follows:

- shift into the chip a programming instruction
- bring CS low for t_{CS} minimum
- bring CS high
- monitor DI/DO bus till a "1" level is detected (Ready)
- clock SK once
- bring CS low
- the chip is ready to accept a new instruction

It should also be noted that this Ready/Busy status can be found active after the power-up of the chip; therefore, it is recommended to clock SK once (with CS = 1) prior to any instruction.

CONCLUSION

This note gives some guidelines for the possibilities and the conditions of a safe operation in common DI/DO applications. The safety of these designs is based on the good safety margins and the worst case data sheet values used in the calculations. These calculations are of course not exhaustive, each designer may adapt them for any given application.

SGS-THOMSON MICROELECTRONICS

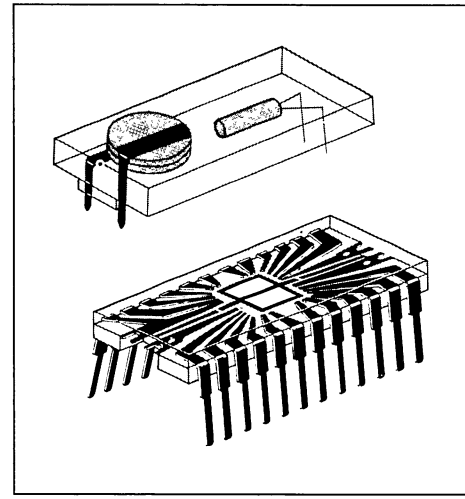
APPLICATION NOTE

ENSURING DATA INTEGRITY IN ZEROPOWER AND TIMEKEEPER RAMs

The ZEROPOWER™ and TIMEKEEPER™ product families offer a unique non-volatile RAM solution. ZEROPOWER products consist of a single chip containing an ultra low power SRAM, a comparator for power supply voltage detection and battery control logic. TIMEKEEPERs include, in addition, a real time clock which loads clock/calendar information into specific locations of the memory array.

The monolithic ZEROPOWER and TIMEKEEPER chips are packaged in 600 mil wide dual-in-line plastic packages with 24 or 28 pins. The "top-hat" housing attached to the top of the DIP package contains the battery and also a crystal for the TIMEKEEPER products.

The products operate as conventional SRAMs when external power is applied. They have standard SRAM footprints and fast read and write access times. When the applied power supply drops below the specified threshold, the control circuitry write protects the memory. At a lower voltage the internal battery supplies power to maintain the data



ZEROPOWER Main Part Numbers

Size	Type	Organisation	V_{CC} Trip	Feature
16K	MK48C02	2K x 8	4.75 V	No battery
	MK48Z02	2K x 8	4.75 V	
	MKI48Z02	2K x 8	4.75 V	–40 °C to 85 °C
	MK48Z12	2K x 8	4.5 V	
	MKI48Z12	2K x 8	4.5 V	–40 °C to 85 °C
64K	MK48Z08	8K x 8	4.75 V	Power Fail Interrupt
	MK48Z09	8K x 8	4.75 V	
	MK48Z18	8K x 8	4.5 V	
	MKI48Z18	8K x 8	4.5 V	–40 °C to 85 °C
	MK48Z19	8K x 8	4.5 V	Power Fail Interrupt

TIMEKEEPER Main Part Numbers

Size	Type	Organisation	V_{CC} Trip	Feature
16K	MK48T02	2K x 8	4.75 V	
	MK48T12	2K x 8	4.5 V	
64K	MK48T08	8K x 8	4.75 V	Power Fail Interrupt
	MK48T18	8K x 8	4.5 V	Power Fail Interrupt

in the SRAM and power the real time clock until the system power becomes valid again.

Correct operation of the ZEROPOWER and TIMEKEEPER products requires the usual design considerations for high speed SRAM systems, however some additional points which sometimes give rise to incorrect operation are discussed below.

Data Corruption or Loss

Negative Undershoots. Loss or corruption of the data in the entire address space of the RAM can be caused by negative undershoots of more than 0.3V occurring on the device pins during a power cycle. Negative undershoots are often the result of improper termination of the signal lines. A resistor network can be used to correctly terminate the signal lines and prevent reflections and undershoots.

Inadvertent Writes. Corruption of data in isolated bytes of the SRAM after a power cycle can be caused by inadvertent write cycles occurring on power up. Inadvertent writes can occur before the system stabilizes but after the ZEROPOWER or TIMEKEEPER is active. The memory should be protected against writing during the start-up phase and the signals are stable, by gating the system RESET with the memory CHIP ENABLE, as shown in Figure 1.

Low or Noisy Power Supplies. ZEROPOWER and TIMEKEEPER products have well specified windows for the power supply voltage within which they deselect or reselect. These windows are specified as either 4.75V to 4.5V or 4.5V to 4.2V. During normal operation the supply voltage for the products must exceed the maximum window value. If however, during a memory access, the supply volt-

Figure 1. Gating of the system RESET and memory CHIP ENABLE for MK48Z02, MK48T02 and MK48Z08

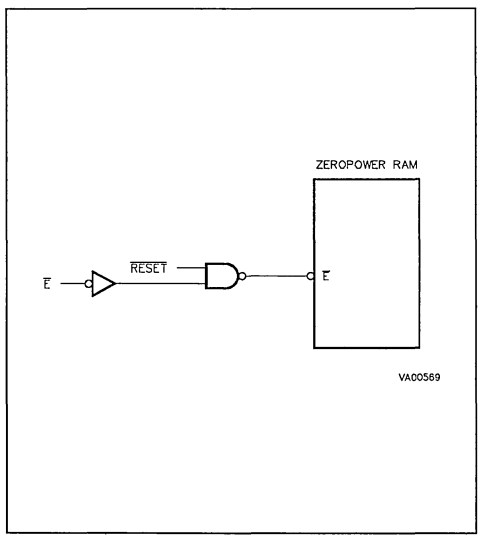
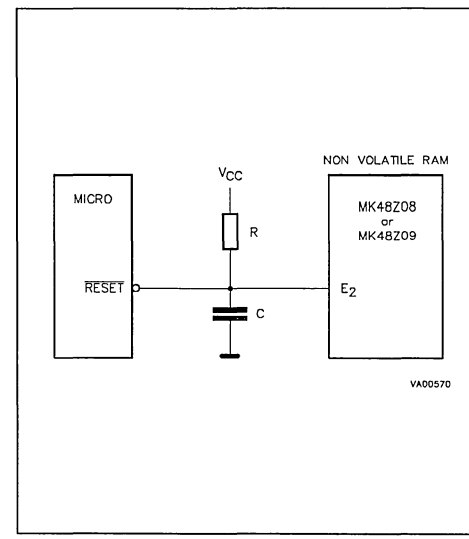


Figure 2. Power on reset using E2 input of the MK48Z08 or MK48Z09



age drops into the deselect window, an invalid read or write to the ZEROPOWER or TIMEKEEPER may occur. Power supply fluctuations caused by current transients can be reduced through the use of a supply bypass capacitor mounted close the memory package. A suggested value is 0.01 µF. If the system power supply is low and cannot be modified easily to bring it within specification, a change in the product type from a 5% to a 10% tolerance part may cure instances of unwanted deselection and apparent data corruption or loss.

TIMEKEEPER Clock Errors

Setting Unused Bits in Clock Registers. Within the eight bytes of clock/calendar information, contained in the memory array of the TIMEKEEPER products, are a number of bits which are specified as 'unused', but which must be written to zero. Some of these bits control internal test modes which speed up the clock in order to efficiently test the products at the factory. The bits are always set to zero before shipment, but if an application sets these bits a test mode may be invoked and the clock may run erratically. In a test mode the clock may run extremely fast or the seconds may not roll over to minutes after 60 counts. Software routines addressing the control registers should specifically set the unused bits to zero.

Immediate Access of Clock Information after a Power Up. During normal operation of the TIMEKEEPER products, the memory locations of the SRAM that contain the clock/calendar information are updated by the internal clock counter once per second. When a TIMEKEEPER is in the battery back-up mode, no updates to the memory locations occur. After a power up, the actual time is transferred to the memory locations one second after the product reselects. Thus access to the clock information in the memory in less than one second after a power up may yield the same information that was present at power down, not the new time.

The precautions described above are the most frequent that many users enquire about, it is hoped that this brief Application Note will provide a fast solution.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

UPGRADED MEMORY CAPABILITY USING ZEROPOWER AND TIMEKEEPER PRODUCTS

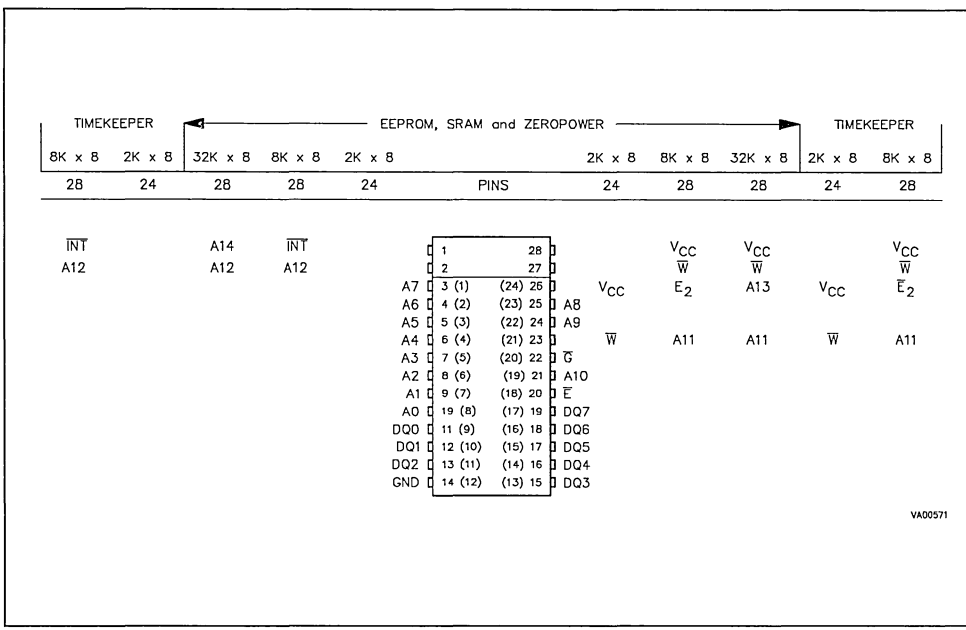
Systems that need read/write non-volatile memory have several choices available: EEPROM, SRAM plus battery or the ZEROPOWER™ and TIMEKEEPER™ products from SGS-THOMSON. Many microprocessor based systems require a non-volatile memory for storing vital data such as calibration constants, set up parameters, adaptable boot programs or other routines, systems status or clock & calendar information. Consequently many systems from computer and POS terminals, video games, process controllers, medical equipment, trip computers, PABXs, to TV sets are using non- volatile memories today.

EEPROM memory access times are fast for data reading (100-200ns) but relatively slow (5-10ms) for writing which means that in many system applications data has to be copied in fast RAM and written to the EEPROM only when neccessary.

Standard SRAMs can be incorporated directly into the memory map of processors since they have fast, equal read and write speeds. However additional circuitry must be designed to monitor the power supply and switch them over to battery back-up operation to make them non-volatile. A perfect solution to the need for non-volatile RAM is provided by the SGS-THOMSON ZEROPOWER and TIMEKEEPER RAMs which provide an SRAM together with battery back-up and the power supply and switch over circuitry in a single package. In addition the TIMEKEEPER products include a real time clock providing year, month, day, date, hour, minute and second information which may be read from locations in the SRAM address space.

System designers can adopt a flexible solution to non-volatile memory by making a PC board layout which will allow users to have an easy upgrade from

Figure 1. Signal definitions for 24 and 28 pin DIP



one solution to another. Three jumpers can be used to select the use of 2k x 8, 8k x 8 or 32k x 8 EEPROM, standard SRAMs or ZEROPOWER/ TIMEKEEPER products. Product enhancements can be easily made by changing, for example, an EEPROM to a TIMEKEEPER. This would retain the non-volatile memory, but would add the ability for fast reading and writing of the memory and have a real time clock available. Typical benefits from using the TIMEKEEPER would be to timestamp events such as data transfers or files.

The standard pin out for 2k to 32k memories is based on either a 24 or 28 pin dual-in-line package. Figure 1 shows in the center a 24 or 28 pin package with the signal definitions for the 2k x 8 memory - which can be an SRAM, EEPROM or ZEROPOWER product in 24 pin DIP. The difference in the signal definitions for each type and size of memory are show to the left and right.

Table 1 gives the full listing of memory types and the jumper connections corresponding to the circuit of Figure 2. The PC board is provided with 28 connections, but only the lower 24 are used for smaller memory sizes. Pin 2 is jumpered across to either the $\overline{INT}$ line for the TIMEKEEPER MK48T08, or the A14 address line for the larger 32k x 8 EEPROM, SRAM or MK48Z32 ZEROPOWER products. Pin 26 is jumpered across to one of three signals, the supply Vcc for smaller memories of 2k x 8 capacity including the ZEROPOWER MK48Z02, the second chip enable $\overline{E2}$ for the TIMEKEEPER MK48T08 or the address line A13 for larger memories of 32k x 8 capacity including the MK48Z32. The third jumper on pin 23 connects to either the write line $\overline{W}$ for 2k x 8 EEPROM, SRAM and ZEROPOWER/TIMEKEEPER products or to A11 for the 8k x 8 and larger 32k x 8 sizes.

Figure 2. Jumpers for pins 1, 23(21) and 26(24)

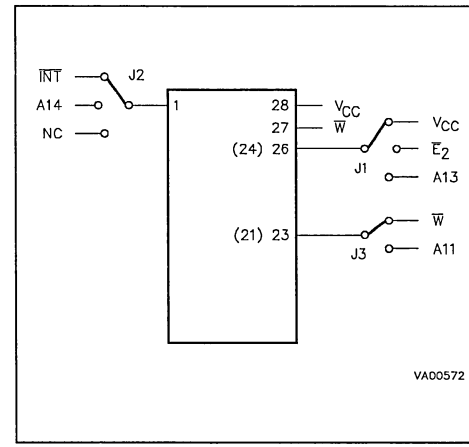


Table 1. Jumper positions for each type of memory

Type	Part Number	Size	J1	J2	J3
EEPROM		2K x 8	V_{CC}		$\overline{W}$
		8K x 8			A11
		32K x 8	A13	A14	A11
SRAM		2K x 8	V_{CC}		$\overline{W}$
		8K x 8			A11
		32K x 8	A13	A14	A11
ZEROPOWER	MK48Z02	2K x 8	V_{CC}		$\overline{W}$
	MK48Z08	8K x 8			A11
	MK48Z09	8K x 8	E2	$\overline{INT}$	A11
	MK48Z19	8K x 8	E2	$\overline{INT}$	A11
	MK48Z32	32K x 8	A13	A14	A11
TIMEKEEPER	MK48T02	2K x 8			$\overline{W}$
	MK48T08	8K x 8	$\overline{E2}$	$\overline{INT}$	A11
	MK48T18	32K x 8	$\overline{E2}$	$\overline{INT}$	A11

TIMING SPECIFICATIONS

There has been for some years misunderstandings about the definition and specification of memory timing parameters. Many companies have used different timing names and different waveform diagrams. Sometimes parameters are not clearly and unequivically defined.

Timing parameter names have historically tended to describe the functions of the time, for example:

- t_{AH} Address Hold time
- t_{DH} Data Hold time
- t_{ACC} Access time

These names do not describe very well the actual time specified, t_{AH} does not say hold time from what, to what. t_{ACC} does not specify whether this is the time from, for example, addresses valid or from chip enable asserted.

A better system is to follow that outlined by JEDEC. This uses both signal names and logic states to define the timing parameters.

The system follows the rules as in the example "t_{1234}", where 1 and 3 specify the signal names (negative logic signals eg. $\overline{E}$ are shown without the negation bar), for example:

- Q Data Output
- D Data Input
- E Chip Enable
- G Output Enable
- A Addresses
- W Write Enable

and, 2 and 4 specify the logic level as in Figure 2 and follows:

- H a Low to High transition to above a High level measurement threshold
- L a High to Low transition to below a Low level measurement threshold
- V valid signals, above High or below Low measurement levels
- X transition or invalid signals, signals that are possibly changing and are below a high level or above a low measurement level.

Figure 1. Signal Names

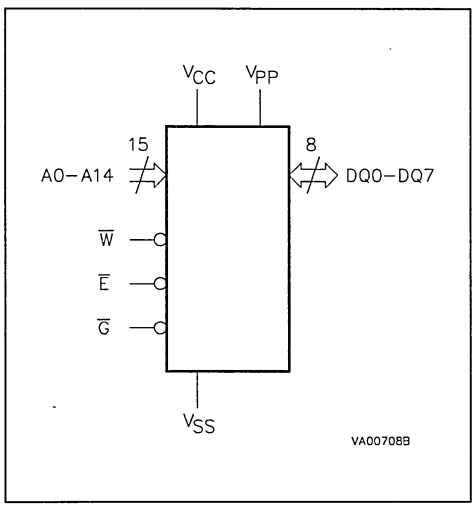
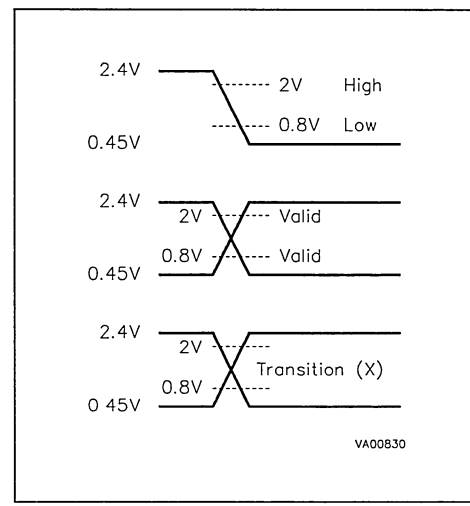


Figure 2. Input Output Waveforms References



Note: High. Low, Valid and Transition (X) levels.

Some examples of these definitions, with the name it replaces, are in Table 1.

Table 1. Timing Characteristics Example

Symbol	Alt	Parameter
t_{AVAV}	t_{RC}	Read Cycle Time
t_{AVQV}	t_{ACC}	Address Valid to Output Valid
t_{ELQX}	t_{LZ}	Chip Enable Low to Output Transition
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid
t_{GLQX}	t_{OLZ}	Output Enable Low to Output Transition
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid
t_{EHQZ}		Chip Enable High to Output Hi-Z
t_{GHQZ}	t_{DF}	Output Enable High to Output Hi-Z
t_{AXQX}	t_{OH}	Address Transition to Output Transition

Note: These are taken from the FLASH MEMORY data sheets.

MEASUREMENT CONDITIONS

The signal measurement conditions are also important for the definition of timings, there are three important definitions,

The input signal rise and fall time. Although, in theory, no timings depend on this - that is the definition of parameters is not dependant on the rise or fall time of the input signals - some products may have characteristics which vary with the slew rate of the input.

The levels of the input signal. Both the Low level and High level voltage. These obviously must be at least equal to the specified V_{IL} and V_{IH} for the device input signals.

The voltage level at which the timing measurement starts and stops.

For example, for EPROMs the SGS-THOMSON specification states:

- Input Rise and Fall times are 20ns max
- Input and Output signal levels are 0.4V(min) to 2.4V(max)
- Input and Output timing reference levels are 0.8V(Low) to 2.0V(High)

and, a signal is defined as Hi-Z (high impedance) when it is not driving or being driven.

USING THIS SYSTEM

The system then works, for example, like here after described.

A time specification of t_{AVQV} means a time from the point where the address lines are ALL below 0.8V for signals at or going to a logic Low level and above 2.0V for those at or going to a High logic level, to a time where the data output signals are ALL either below 0.8V or above 2.0V.

A time specification of t_{EHQZ} means a time from the chip enable input going above 2.0V to the point where the data output is no longer driving.

A time specification of t_{AXQX} means a time from the point where any single address line rises above or falls below its stable, valid level (0.8V for Low level or 2.0V for High level), to the point where any data output line transition passes these levels and is consequently no longer valid.

TIMING DIAGRAMS

The use of these definitions makes it unneccessary to draw the timing diagrams with times shown from a notional high or low measurement point, as the measurement points are clearly specified by the definition of measurement conditions and the signals and logic are described by the timing parameter description. The diagrams can be simplified for maximum clarity and understanding by indicating, diagrammatically, the timings from the waveform center point.

For example, if the measurement conditions for timing are specified as:

- Input Voltage levels are 0.45 to 2.4V
- Input and Output reference levels are 0.8 to 2V

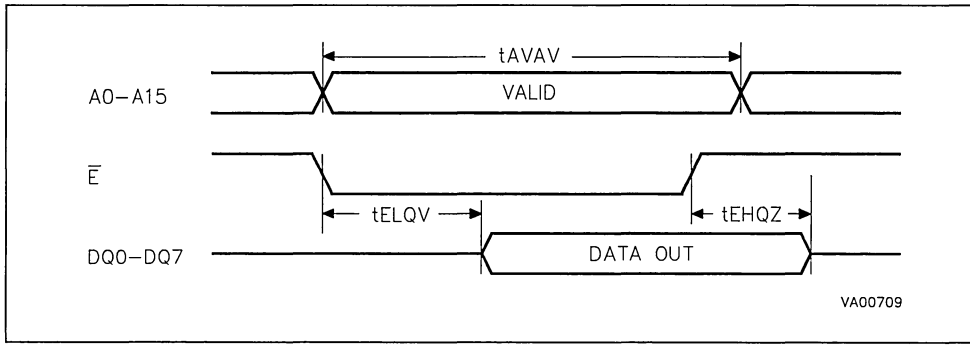
and, Output Hi-Z is defined as the point where the signal is no longer driving; then in the diagram:

- t_{AVAV} is measured from the point where all address lines are either above 2V or below 0.8V to the same levels at the end of the cycle.
- t_{ELQV} is measured from $\overline{E}$ Low, or below 0.8V to the point where all data lines are either above 2V or below 0.8V.
- t_{EHQZ} is measured from $\overline{E}$ High, or above 2V, to where the data outputs are no longer driving the signal lines.

Note that the t_{ELQV} timing, for example, is shown diagramatically not from a "low" point on the $\overline{E}$ falling edge, but from the center and is shown not to a "high/low" point on the Data Output but again to the center. This is for clarity of the diagram, as the actual measurement points are clear from the definitions and timing names.

This system has been, or will be, adopted for all SGS-THOMSON memory products.

Figure 3. Timing Diagram Example

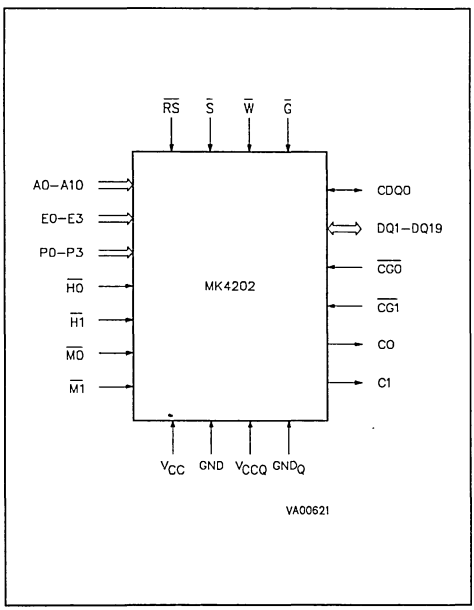


THE MK4202 TAGRAM 32-BIT CACHE DESIGN CONCEPTS

INTRODUCTION

The MK4202 cache TAGRAM™ from SGS-THOMSON Microelectronics is a very fast CMOS SRAM based Cache Directory Comparator. The MK4202 offers high performance with a 20ns cycle time, and a 17ns address to tag compare access time. It is configured for the new generation 32-bit microprocessors, and implements a 2K x 20 architecture (see Figure 1). The device contains a 20-bit on-board comparator with dual compare or match outputs for easy interface to various 32-bit processors. An on-board chip enable decoder is also included to allow both width and/or depth expansion. Depth expansion is allowed up to a 32K density without speed (propagation time) penalties.

Figure 1. MK4202 TAGRAM Logic Symbol



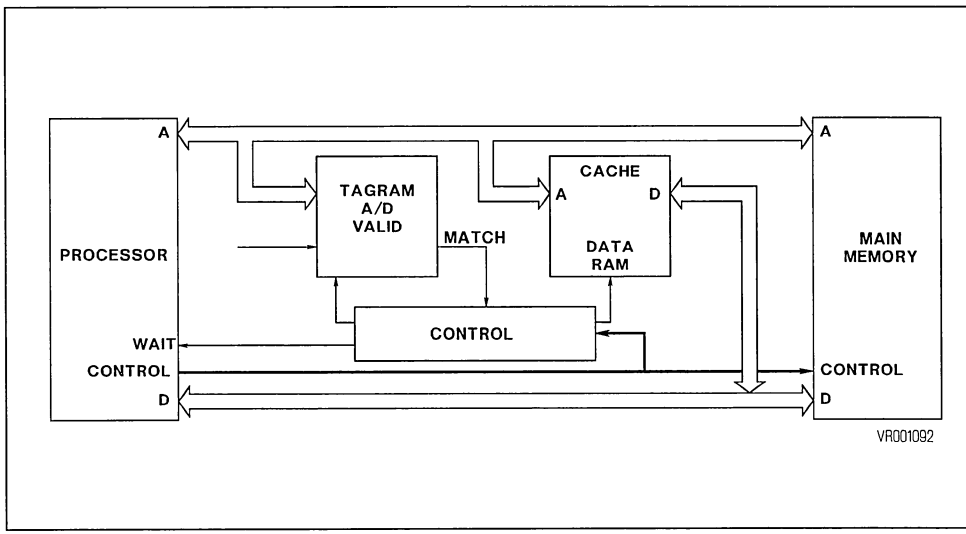
The MK4202 can enhance both system performance and cost. The high speed compare access time enhances the zero wait state logic to the processor for better system performance. Secondly, the MK4202 has high impedance data bus control inputs ($\overline{S}$) ($\overline{G}$), and eliminates separate latch, transceiver, and comparator components. This reduces the required real estate in PC board area, and results in lower system cost with no added gate delays through separate components.

TAGRAM OPERATION

A TAGRAM is that part of a ***cache subsystem*** that determines if data or instructions is retained in the cache memory (data cache). While this may be obvious, it should be noted that typical cache subsystems are designed in three sections: the **data cache** which stores the data to be used by the microprocessor, the **cache tag buffer** or **cache directory,** which stores the upper order address of each cache entry, and the **cache control** logic for processor interface, and cache read/write operations (see Figure 2). The data is identified by address location, and is stored in the cache directory (the MK4202 serves as the cache directory). If the TAGRAM "sees" a match, meaning that the necessary data is resident in the cache, it determines a **hit** and initiates a zero wait state operation to the processor. Conversely, a **miss** (nomatch) condition results in longer cycles for program execution since the cache does not contain the requested information.

During a compare cycle, the MK4202's on-board 20-bit comparator compares the upper address inputs (DQ_0 - DQ_{19}) with internal RAM data at the specified index address (A_0 - A_{10}). (The TAGRAM's architecture is shown in Figure 3). If all bits are equal (match), a hit is determined, and both Compare Outputs (C_0 and C_1) will go HIGH. If at least one bit is different, a miss condition exists, and both C_0 and C_1 will go LOW. The user can optionally force a MISS or HIT on either or both compare outputs by asserting $\overline{M}_X$ or $\overline{H}_X$ active LOW. A forced MISS overrides a forced HIT input (note the data sheet Truth Table). The Compare Ouput Enable ($\overline{CG}_X$) has no affect during a Force Hit or Force Miss operation.

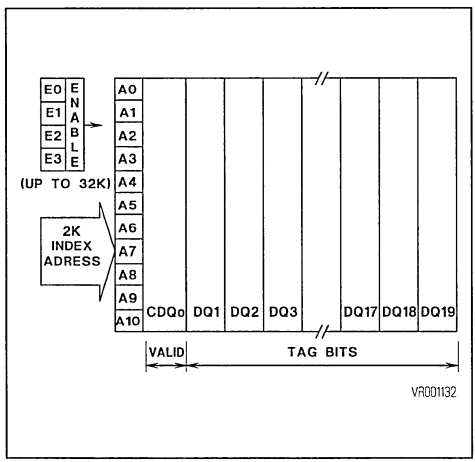
Figure 2. Generalized Cache Block Diagram



CIRCUIT DESCRIPTION

A Direct Mapped Cache subsystem application using the MK4202 is shown in the schematic block diagram in Figure 4. In this example, we are serving a 32-bit microprocessor with a 32-bit address bus and data bus. The 12 lower significant address lines (A_0 - A_{11}) are connected to the address inputs of the MK4202, with A_{11} connected to E_0 of both TAGRAMs as shown.

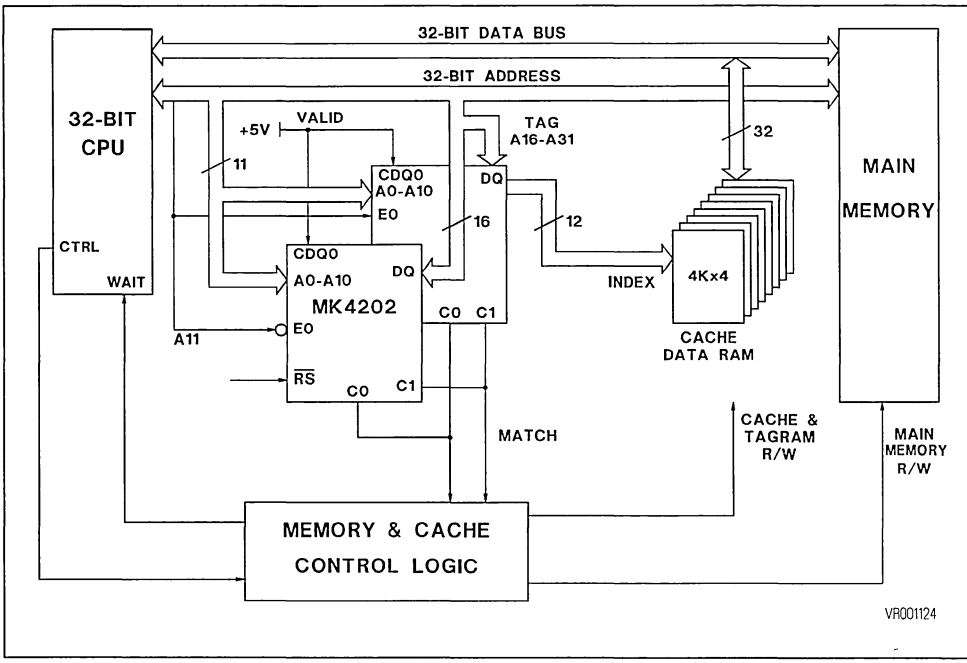
Figure 3. MK4202 TAGRAM Organization



This input will implement a 4K address index for the Cache Directory in this example, and a 4K address for the Cache Data RAM. The upper address bits of the processor (A_{16} - A_{31}), function as the tag data bits for the MK4202 TAGRAM, with CDQ_0 pulled up to V_{CC} (+5 volts) as a **valid bit.** Therefore, the cache tag buffer, or Cache Directory, consists of 4K x 16 bits, or 8K bytes. The Data Cache consists of eight very fast 4K x 4 SRAMs with Chip Enable ($\overline{E}$) for a 32-bit line width, resulting in a total of 16K bytes of memory (refer to Figure 5). Cache subsystems studies have shown that a cache design using this mapping scheme and combined memory size can yield a hit rate of better than 80%.

The MK4202 TAGRAM uniquely identifies each cache entry with an *address scheme consisting of the index and tag.* The upper addresses of a 32-bit microprocessor are considered as the tag, and are connected to the DQ pins (DQ_1 - DQ_{16}) of the MK4202 (see Figure 4). The CDQ_0 pin is designated to serve as the valid bit, as it allows the internal RAM to be reset or cleared to all zeros at all locations for the CDQ_0 output. The 11 address inputs (A_0 - A_{10}) of the MK4202 function as the **address index**, and are connected to the lower addresses of the processor. Extra lower order address lines can be connected to the Enable Inputs (E_0 - E_3) for on-board chip enable decode for depth expansion. (The E_0 - E_3 inputs correspond directly to the P_0 - P_3 inputs as described in the MK4202 data sheet). In this example, A_{11} is connected to E_0 for a depth expansion of 4K. The C_0 and C_1 Compare Outputs incorporate a CMOS totem-pole *3-state* design. This high impedance state allows

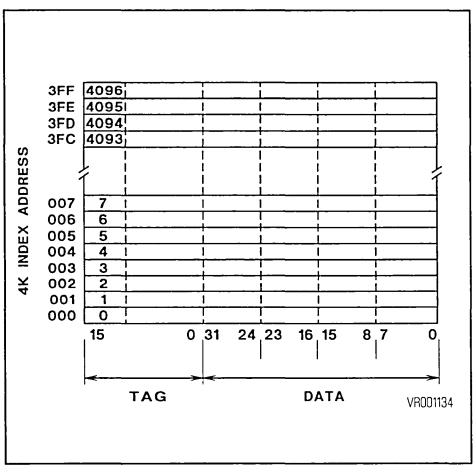
Figure 4. 16K-Byte Direct Mapped Cache Subsystem



CIRCUIT DESCRIPTION (Continued)

each output to be tied together in a wired-OR configuration for multiple device applications, as shown in Figures 4 and 6. A pull-up resistor is suggested to enhance proper operation.

Figure 5. Cache Example Organization

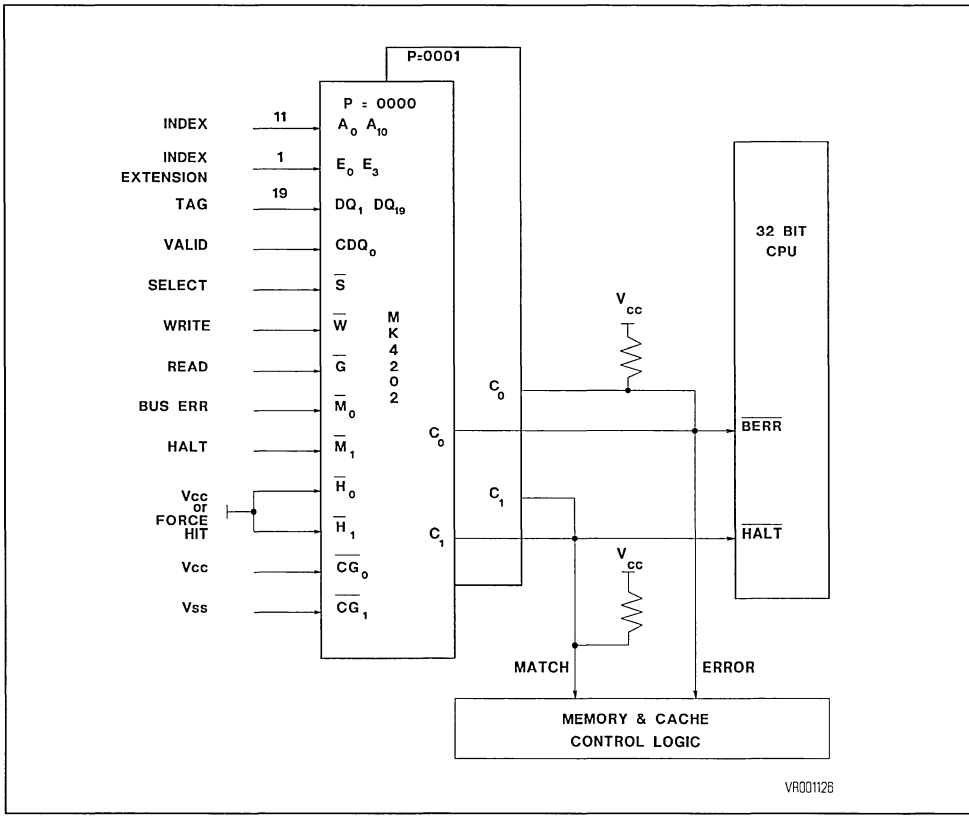


All processor address lines do not have to be connected to the TAGRAM, as most systems require designated *non-cached* addresses. Some address lines may define peripherals from an address vector for various I/O devices, or define DMA operations. Thus, a certain amount of address space is often required for various non-cacheable operations. Therefore, extra address lines from the processor can be used to decode these system operations. Unused addresses from the processor can be left open ; however, unused control and address inputs or tag data inputs to the MK4202 should be tied to be determined as a logic one or logic zero.

CIRCUIT OPERATION

The basic purpose of our Direct Mapped Cache subsystem is to provide the microprocessor (henceforth CPU) with a quick response for requested data from the **data cache** to avoid long memory cycles to main memory. Since typical programs spend most of their execution time in loops or nested procedures from a few localized areas of the program, the cache subsystem can maintain a copy of this localized data for faster execution. This will make our system more efficient and provide optimum performance.

Figure 6. Application Block Schematic



CIRCUIT OPERATION (Continued)

Operation begins by initializing the MK4202 TAGRAM by asserting $\overline{RS}$ to clear all internal SRAM bits for the CDQ_0 output to a logic zero. This invalidates all entries in the cache directory. When the CPU begins its first read command cycle, the lower address bits select a location in the MK4202. This location in the TAGRAM is compared against the 16 bits of tag along with the single valid bit ($CDQ_0 = V_{CC}$). The valid bit will determine a miss condition causing C_X to go LOW since data ones is being compared against data zeros. This is a **cache miss**, and the CPU will wait for a response from main memory.

In our Direct Mapped Cache subsystem example, we will assume the *write-through* method for main memory and cache coherency. This means that while the CPU is waiting for data during a **read/miss** operation, that the cache write/read control logic is designed to write data from main memory into the data cache SRAMs at the address defined by the index. When this happens, the 16 bits of tag, along with the valid bit, will be written simultaneously into the MK4202 cache directory. This way both the main memory and the **cache subsystem** contain the same information.

Now the logic one valid bit on the MK4202 TAGRAM can verify that the data in the data cache is a valid copy of main memory, since both the internal data and CDQ_0 (valid) are data ones. Of course, a cache miss will not occur after a reset operation, but every time the lower 12 address index bits select a location where the 17 tag bits (16 bits plus valid bit) do not match. However, each time a miss occurs, the most recent data will be written into the cache memory. This maintains cache coherency with main memory by constantly updating the cache with the most recent data.

CIRCUIT OPERATION (Continued)

After the cache has been written with valid data, and the CPU executes a read command from the same location that has been written into the cache subsystem, then the data tag bits will match, and a **cache hit** results. During a hit condition, both compare outputs, C_0 and C_1, will go HIGH. This will cause the CPU to operate in a no-wait state, and data will be gated onto the data bus from the data cache memory. The match/hit operation takes the requested data from the data cache, avoids wait state cycles to main memory, and terminates the cycle with a data acknowledge to the CPU.

It should be noted that even though both C_0 and C_1 go HIGH during a hit, that both compare/match outputs may not be required for the cache hit/miss control logic. The user could use one match output for determining a miss or hit condition, and use the other compare output to pass inputs through the MK4202 to the CPU. This is illustrated in Figure 6, where C_0 is normally HIGH except in an error condition. In this manner, a system error or halt will alert the CPU and invalidate cache execution at the same time. This is another benefit using the MK4202 and can reduce the number of required logic gates, and therefore system components.

CONCLUSION

We have given a general application and overview of the MK4202 cache TAGRAM in conjunction with a 32-bit data bus Direct Mapped Cache subsystem concept. System operation allows the cache subsystem to be updated with the most recent data for each access to main memory. The MK4202 allows easier implementation, and reduces the number of devices or components. Of course the MK4202 can also be used to implement a two or more set-associative cache design. In fact, by using the enable and chip select inputs on the MK4202, one can easily implement several cache design arrangements.

There are several features and organizational benefits when using the MK4202 for cache design. The device provides a flash clear ($\overline{RS}$) function to invalidate cache entries, which is useful for single processor systems, and for multi-processor systems sharing a cache subsystem. Additionally, the MK4202 is wide enough to provide extra bits for storing other information besides address tag data. One example might be "dirty bit" storage in a multi-processor application using a copy *back* method for cache coherency. Another example could be identification of non-cached addresses.

With the introduction of SGS-THOMSON's MK4202 TAGRAM, implementing cache subsystem designs for a 32-bit processor has been made easier. Cache subsystem implementation can now be provided for small-to-medium microcomputer systems without a large investment. The MK4202 TAGRAM provides for cost effective, high speed cache memory designs for today's 32-bit microprocessors, and is fully TTL compatible on its inputs and outputs.

UNDERSTANDING CACHE MEMORY SYSTEMS

INTRODUCTION

Each new generation of microprocessors on the market has become faster and faster. Today, microprocessors, such as the Intel 486 and the Motorola 68030 have cycle times of 25 ns and plan to go faster in the future. The speed of DRAM main memory in such microprocessor-based systems has not come close to matching these cycle times. For example, it is quite common to use a DRAM with a cycle time of 100ns with an Intel 486 microprocessor. The resultant difference in cycle times between the microprocessor and DRAM means that the microprocessor cannot operate at full speed, because it must perform "wait states" during memory cycles. Wait states seriously reduce system throughput and performance.

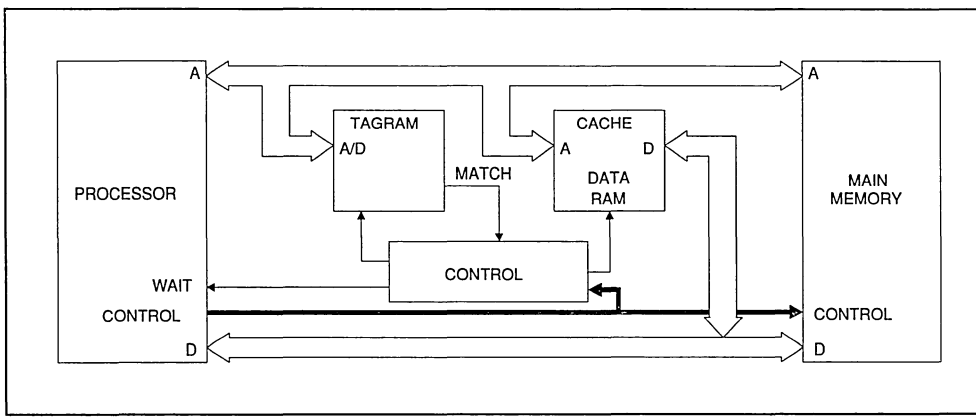
Cache memories are used to increase system throughput by reducing these microprocessor wait states. A cache system is a small, fast access SRAM bank, capable of single cycle accesses, which resides between the microprocessor and DRAM. The cache contains a copy of a block of DRAM memory which is frequently accessed by the microprocessor. By putting frequently accessed memory in the fast cache memory, the microprocessor can receive data from the cache instead of the slow DRAM during memory cycles. The DRAM only supplies data to the microprocessor when the cache memory does not have the needed data. In this way, using a cache subsystem reduces microprocessor wait states.

The theory works because most software code and data is contiguously stored in memory, and accessed repeatedly; therefore, the principals of temporal and spatial locality can be applied. The principal of temporal locality dictates that information currently being used by the microprocessor is likely to be used again in the near future. The principal of spatial locality dictates that the information to be used during the next memory cycle is likely to be close to the addresses of the information previously used by the microprocessor. Thus temporal locality is related to timing and spatial locality is related to actual physical location. According to these principles, there is a greater likelihood the microprocessor will find requested data in the cache memory and avoid wait-states.

ELEMENTS OF A CACHE SUBSYSTEM

The cache subsystem resides between the microprocessor and main memory and is comprised of three elements: the data cache, the cache tag buffer, and the cache control logic. The data cache contains the copy of prefetched data from the DRAM. The cache tag buffer or TAGRAM™ stores addresses for each corresponding entry, also called the TAG, in the data cache. The cache control logic interfaces with the microprocessor and controls all read/write operations between the processor, main memory, and cache memory. The block diagram in Figure 1 shows how these ele-

Figure 1: CACHE SUB-SYSTEM Block Diagram



ments interact with one another, the microprocessor, and the DRAM.

THEORY OF OPERATION

In order to better understand how a typical cache subsystem works, lets look at the operation of a direct mapped cache. In a direct mapped cache, each data cache location is mapped to one main memory location as shown in Figure 2 below.

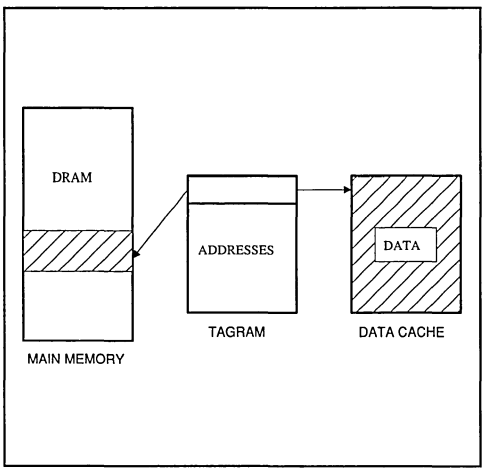
Cache Miss

Upon power-up, all locations in the data cache are set to zero. When the microprocessor initiates its first read cycle, the upper bits of the address bus are compared with the address bits stored in the TAGRAM. For this first compare, there will not be a match since the data cache is empty and the TAGRAM has no corresponding addresses. This is called a cache miss, and the MATCH output on the TAGRAM will be a logic zero. In this case, the required data will have to come from DRAM. The cache controller signals the DRAM to provide the requested data and directs the microprocessor to execute wait states until it receives data. When there is a cache miss, the controller also initiates logic which insures the data cache will be updated with a copy of DRAM data.

Cache Hit

The next time the microprocessor performs a read cycle to the same address, the data cache will contain the needed data since the data cache has been updated to reflect what is in the DRAM. Again, the address inputs to the TAGRAM are compared with the address bits stored in the TAGRAM. If there is a match, this is called a "hit" condition. The comparator inside the TAGRAM will output a logic 1 on the MATCH output for a hit condition. A MATCH output of logic 1 means that the data contained in the data cache at this location is valid. The cache control logic will gate the data immediately onto the data bus and signal the microprocessor to complete its memory cycle. This happens so quickly that the microprocessor never has to execute a wait state.

Figure 2: Direct Mapped Cache Organization



An Example ...

Consider your friendly local television repairman. When he is dispatched to your residence, he carries only those parts which are most often required for repair. It would be impractical for him to bring every part that might possibly be needed; that would be tantamount to transporting the entire inventory of parts from the shop to your home!

The repairman checks his list of parts and, if the required part is on the list, he fetches it from the truck. Since most repair jobs can be performed with those parts in the truck, it is likely your television set will be repaired immediately. However, if the required part is not in the truck, it will have to be fetched from warehouse inventory. Since this part broke in your television set, there is a greater chance of it needing to be replaced than previously thought. Hence, when the repairman goes to the warehouse, he selects two of the needed parts: one to repair your television set and the other to put in his truck. This increases the likelihood that you will not have to wait on a part if your television breaks again.

CACHE SUBSYSTEM PERFORMANCE

The performance of any cache subsystem can be measured by its hit rate. The hit rate is the percentage of memory cycles which can be completed using data from cache instead of data from the slower DRAM. For purposes of this discussion, we will talk about the cache performance of direct mapped caches. A cache hit occurs when the data cache has data requested by the microprocessor during a memory cycle. The microprocessor will receive data from the data cache and will avoid the wait states it would have incurred waiting on the DRAM. Therefore, the higher the hit rate, the more time the microprocessor spends working from fast cache memory and system performance is enhanced.

A hit rate of about 80% is common for a 64K byte direct mapped cache in a PC. This means that the microprocessor can operate with no wait states 80% of the time.

Hit Rate Versus Organization

Hit rate, for the same size cache memory, can be increased by varying the organization of the cache subsystem. Besides direct mapped, there are set associative cache organizations which achieve higher hit rates. 2-way and 4-way set associative caches are the most commonly used. The 2-way set associative cache is divided into two separate banks of memory. The 4-way set associative cache is very similar to the 2-way except that it has four banks. Figure 3 shows a typical 2-way set associative memory. The 2-way set associative system contains two TAGRAM banks, two data cache banks, and the control logic. Also, unlike the direct mapped cache, it has a LRU (Least Recently Used) memory. This is a small memory used by the control logic to determine which of the two memory banks should be updated next after a "miss". The memory bank that was not read last, the least recently used, is updated to match main memory.

As mentioned above, the hit rate for a 64K byte direct mapped cache in a PC environment is about 80%. For a 64K byte system, the 2-way set associative memory has a hit rate of approximately 94% and the 4-way set associative is only slightly higher with a hit rate of approximately 98%. The performance increase of a set associative cache should be weighed against its higher cost. The increase in performance from the direct mapped organization to the 2-way set associative organization is substantial: from 80% to 94%. On the other hand, there is a relatively small performance increase of the 4-way set associative over the 2-way set associative cache (94% to 98%). Moreover, 4-way set associative caches generally are much more expensive than 2-way set associative caches. Figure 4 shows typical hit rates for direct mapped and set associative organizations.

CACHE EXPANSION

Cache expansion allows the designer to construct wider and deeper caches subsystems while working with readily available and relatively inexpensive parts. There are basically two types of cache expansion: width expansion and depth expansion. Below, Figure 5 shows width expansion and Figure 6 shows depth expansion using SGS-THOMSON parts.

Figure 3: 2-Way Set Associative CACHE Origanization

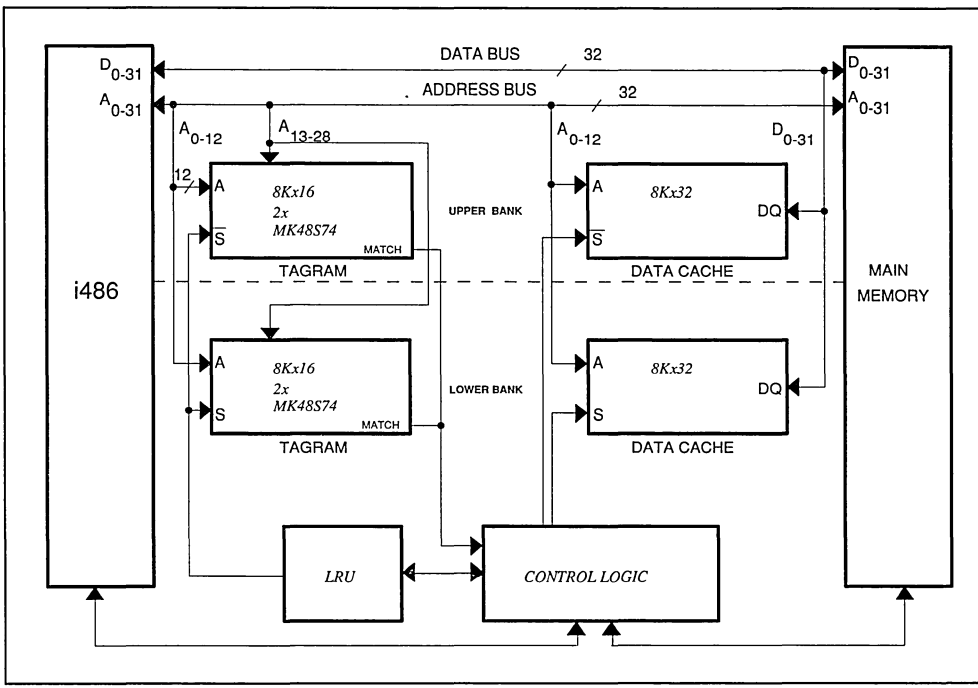
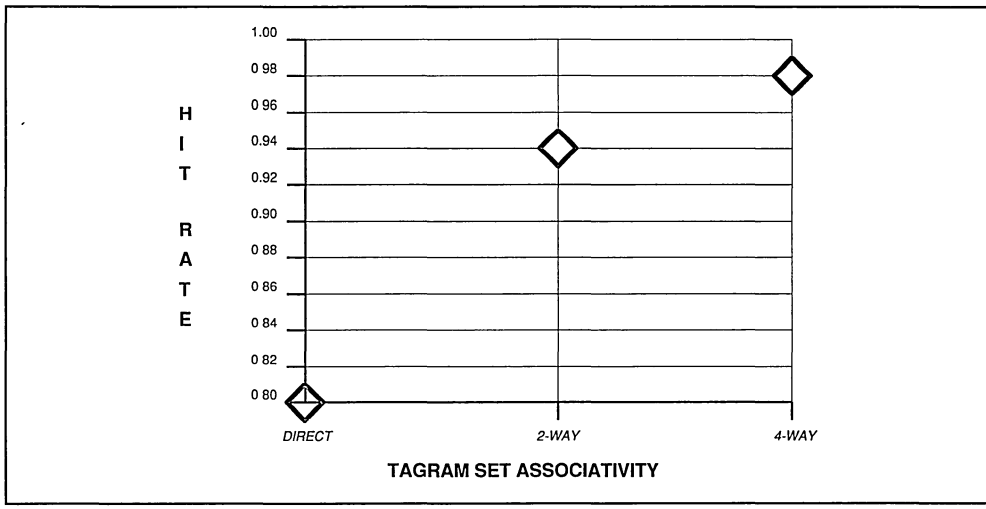


Figure 4: Hit Rate Versus Set Associativity



Width Expansion

Width expansion allows the designer to cache a larger section of main memory as shown in Figure 5. The data bus is widened by increasing the number of data cache RAMs; in the figure, four 4K x 4 SRAMs are used to increase the width of the data bus from 4 to 16 bits. The correct number of data cache RAMs is determined by dividing the width of the desired data bus by the width of the data cache RAMs. In this instance, 16 divided by 4 yields 4 data cache RAMs. Similarly, the address bus can be expanded to a wider size by increasing the number of TAGRAMs. Figure 5 shows how three MK41S80 4K x 4 TAGRAMs are used to increase the width of the address bus from 16 to 24 bits. By utilizing width expansion, the same devices can be reconfigured to adjust for the different bus widths required by various microprocessors.

Depth Expansion

Depth expansion differs from width expansion in that it increases the actual depth of the cache. Cache depth expansion is accomplished by duplicating the TAGRAM and the data cache SRAM as shown in Figure 6. In this example, the cache size was doubled from 8K x 16 to 16K x 16 by adding copies of the MK48S74 TAGRAM as well as copies of the data caches. The upper bits of the address bus are used to provide chip enable selection for the added components. Notice that adding copies of the TAGRAM and the data cache did not expand the bus width; it only increased the size of the cache as a whole. Increasing depth of the cache improves the hit rate, because you are expanding the address map and increasing the likelihood of finding requested data in the cache.

SUMMARY

Cache memories provide the means for dramatically improving microprocessor-based system performance in a cost effective way.

Using SGS-THOMSON TAGRAMs and SRAMs gives the designer the tools needed to significantly increase system throughput by minimizing wait states. Several factors, such as cache organization and size, determine cache effectiveness and must be weighed against system objectives to determine the most cost effective solution. SGS-THOMSON features a full line of TAGRAMs of varying organization and size that empowers the designer to design the right cache to fit individual system needs.

Figure 6: Width Expansion for TAGRAMs and Data Caches

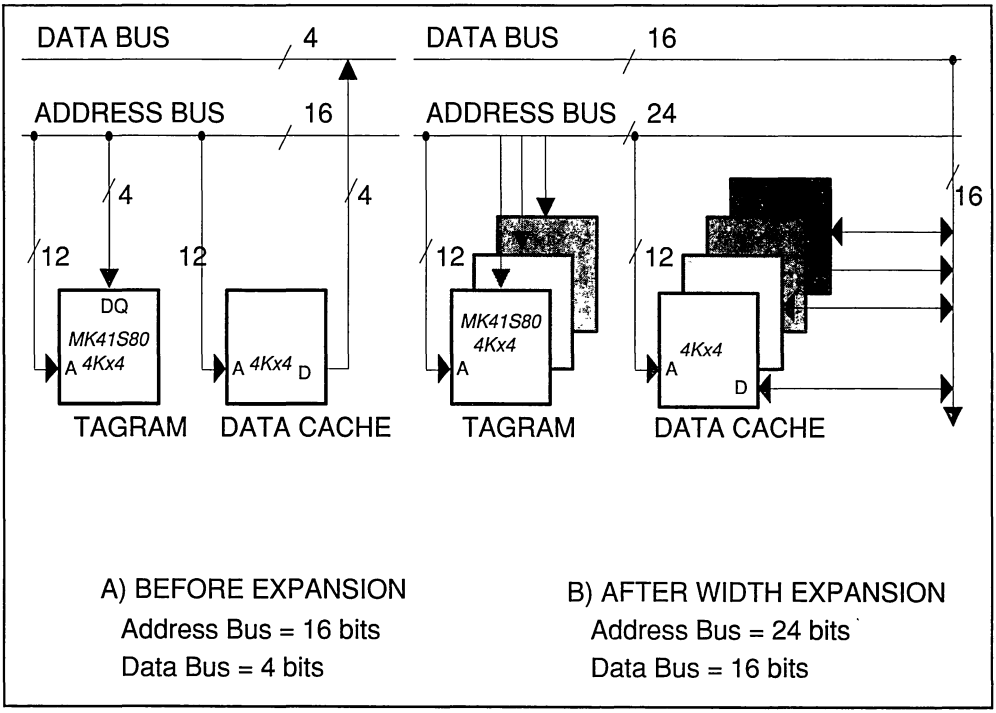
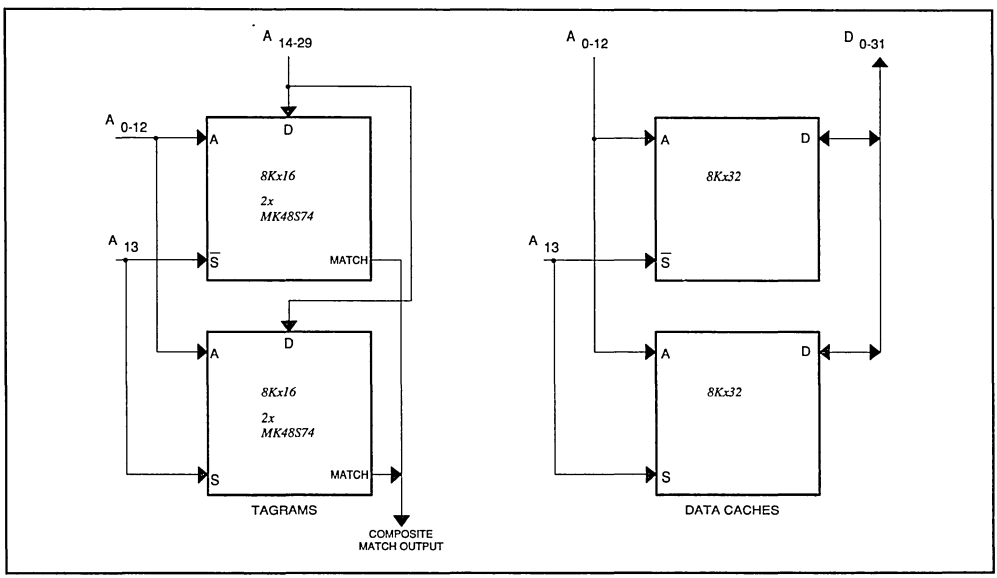


Figure 5: Depth Expansion for TAGRAMs and Data Caches



LIST OF TERMS

Associativity. Cache organization where main memory addresses are mapped to different SETs of SRAM banks.

Cache. Fast, local memory containing a copy of frequently used main memory code and data.

Cache Hit. Microprocessor requested data is found in the cache.

Cache Miss. Microprocessor requested data is not found in the cache.

DRAM. Dynamic Random Access Memory.

Data Cache RAM. Portion of cache that stores copies of main memory data.

Direct Mapped. Type of cache organization in which each data cache location is mapped to one main memory location.

Hit Rate. Percentage of memory requests that are cache hits.

Least Recently Used (LRU). Cache update policy. Used in set associative caches to update the oldest memory bank.

Set Associative. Type of cache organization in which the cache sub-system is divided into memory banks which cache different sections of main memory.

Spatial Locality. Programs usually request data or instructions with main memory addresses close to the address of the data currently being used.

SRAM. Static Random Access Memory

TAGRAM. Portion of cache that stores the main memory addresses of data stored in the data cache RAM.

Temporal Locality. Information currently being used is likely to be used again in the near future.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

WRITE PROTECTION IN THE ST24Wxx/ST25Wxx EEPROM FAMILY

Y. BAHOUT

Among the non-volatile memories available today, the EEPROM is one of the most flexible memories which can be read, erased and written by byte or by block of bytes. This flexibility is appreciated in many applications but one aspect of flexibility in non-volatile memories is to not accept to store (and retain!) erroneous data. The EEPROM has therefore to offer an Erase/Write protect function in order to prevent erroneous Erase/Write cycles occuring. The ST24/25Wxx serial EEPROMs compatible with the I^2C protocol, offer several features for protecting the data stored in the memory.

GLOBAL CONTROL OF THE ERASE/WRITE PROTECTION

Write Control Feature

The Write Control security feature ($\overline{WC}$ signal) is a global memory protection. In addition to the data line SDA and the serial clock SCL, the Write Control input signal can be driven to enable or inhibit the execution of an incoming Write command. When driven low ($\overline{WC}$=0), the EEPROM can be accessed (Erase/Write), when driven high ($\overline{WC}$=1), the EEPROM cannot be accessed (no Erase/Write). This $\overline{WC}$ input pin is driven by the bus master or by some other circuitry.

Dynamic Drive of the Write Control Signal

In order to get the best protection of data within the EEPROM, the bus master has to set the EEPROM in the Write protect mode; in this configuration, data stored in the memory cannot be modified. When the bus master has to write in the EEPROM, the bus master first deselects the memory protection (by driving low the $\overline{WC}$ pin), secondly writes and thirdly sets back the memory protection.

Address Counter Status

When using the Page Write instruction with the $\overline{WC}$ protection disabled ($\overline{WC}$ pin is driven low), the EEPROM internal address counter is incremented after each received byte and, in the case of the last received byte, it will set the EEPROM internal address counter to the right value for the first byte of the following Page Write command. When using the Page Write mode with the $\overline{WC}$ protection enabled ($\overline{WC}$ pin is driven high), the EEPROM internal address counter is incremented after each received byte except for the last received byte; the EEPROM internal address counter remains at the last received byte address.

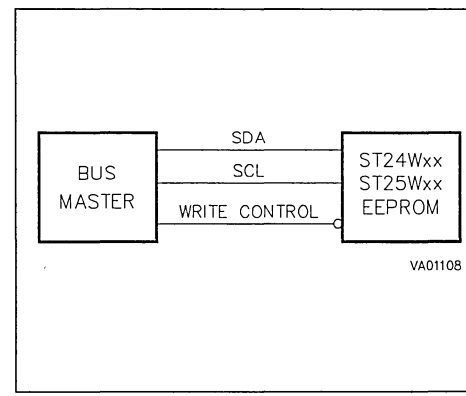
SELECTIVE CONTROL OF THE ERASE/WRITE PROTECTION

Write Protect Enable Feature

In addition to the Write Control feature, a second protection feature is offered on the ST24/25Wxx devices with the help of the input pin PRE. This Protect Enable feature, associated to the PRE pin, is based on external and internal conditions, the external part is driven by the PRE pin and the internal part (software) allowing the definition of the size of the memory to be write controlled.

The memory area to be write protected is defined by an address pointer whose value is stored in the top byte of the memory (address 1FFh, 3FFh and 7FFh for ST24/25W04, ST24/25W08 and ST24/25W16 respectively). All the bytes between this top address and the address defined by the address pointer are protected if the PRE condition is met, as detailed further on. The maximum size of the protected memory is one half of the whole memory for ST24/25W04 and ST24/25W16, one quarter of the whole memory for ST24/25W08 (see Figure 2).

Figure 1. EEPROM Interface with Write Control Line



PRE Software Sequence

The complete sequence in order to protect an area is the following:

a. PRE pin is driven low (by the bus master)

b. Write the data inside the area to be write protected

c. Write the top byte. The Most Significant Bits (MSB) part of the top byte is the address pointer (see Figure 4 and Figure 5), the Least Significant Bits (LSB) are the control bits among which the Write Protect Disable Flag (bit 2) has to be set to '0' for enabling the write control feature.

d. PRE pin is driven high (by the bus master)

Data above the byte pointed by the address pointer are now write protected, they cannot be modified and are functionally equivalent to a ROM block.

Static and Dynamic PRE Control

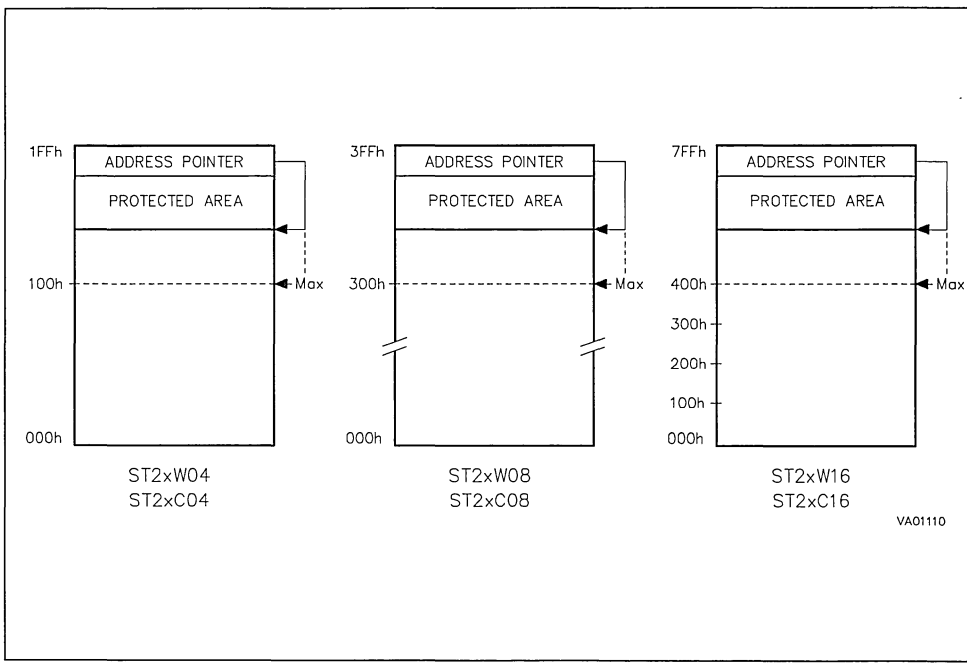
The PRE pin may be driven dynamically by the bus master or wired to V_{CC} (or V_{SS}).

The dynamic drive from the bus master is performed in the same way that the $\overline{WC}$ pin driven. When the bus master has to write in the EEPROM, the bus master first deselects the memory protection, secondly writes and third sets back the PRE pin active. However, this dynamic mode does not make sense when the bus master controls the $\overline{WC}$ pin. The static drive of PRE is generally used with the help of a pull-up resistor, as shown in Figure 3.

The external pull-up resistor on PRE input pin allows the following steps:

- **Initialization of the secure area:** the EEPROM after insertion in the application board can still be driven externally by forcing the PRE pin to 0V (typically a short circuit to V_{SS} pin); under these conditions, the application designer may write application data (such as fabrication date, serial number, customer or dealer area, ...) and address pointer value which must stay unmodified when running the application. Once the PRE protected area is written, the external PRE short circuit is released.
- **When delivered to the end user**, the data written in the PRE protected area cannot be modified (the external pull up resistor on PRE disables the Erase/Write access to this area), only the complementary area inside the EEPROM can be fully accessed.

Figure 2. PRE Protected Areas



Leaving the PRE Mode

The PRE protected mode is active if the two following conditions are true: PRE pin is driven high and bit 2 of the protected memory Address Pointer (top location byte) is '0'. If one of these conditions is not true, the PRE protection is no longer active. In order to leave the PRE mode, the following sequence has to be run:

- PRE pin is driven low
- The Address Pointer (top location byte) is written with 0FFh to freeze the PRE protection and to reset the Address Pointer value.

More About the Address Pointer

The Address Pointer slightly differs with the ST24/25Wxx memory capacity. The following details the structure of this Address Pointer for each memory.

The ST24/25W04 and the ST24/25W08 have the same address pointer, as shown in Figure 4.

The address pointer consists of the 5 MSB (b7-b3) of the byte located at address 1FFh (ST24/25W04), 3FFh (ST24/25W08) with the 3 least significant bits being forced to '0' in all cases. Such an address pointer can define a protected area with a maximum size of 256 bytes, by steps of 8 bytes (because the 3 LSB are forced to '0').

The ST24/25W16 offers a larger address pointer, as shown in Figure 5.

The address pointer consists of the 4 MSB (b7-b4) of the byte located at address 7FFh, the 4 least significant bits being forced to '0' in all cases. Such an address pointer can define an address with a maximum range of 256 bytes, by steps of 16 bytes. In addition to this address pointer, two additional bits are selecting the block number (Block 0,1, 2 or 3) within which the (b7-b4) address pointer is defining the boundary of the protected area.

The size of the protected area is therefore extended up to 4 x 256 = 1024 bytes. These two additional bits (protect block) are driven by the logical level applied on input pins PB0,PB1.

Figure 3. Write Protect Enable Static Drive

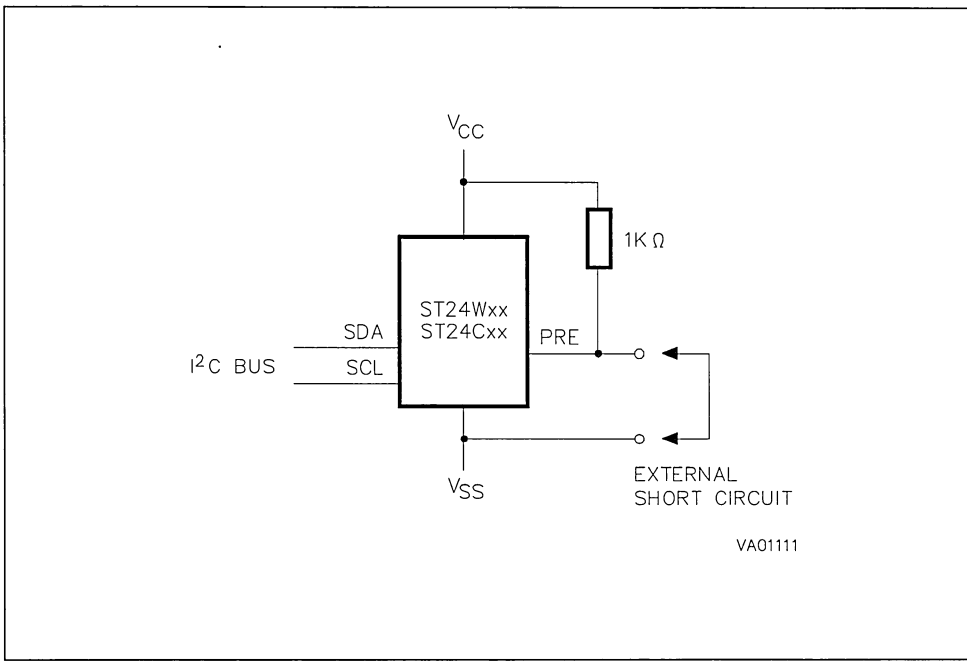


Figure 4. Address Pointer in 4K and 8K Devices

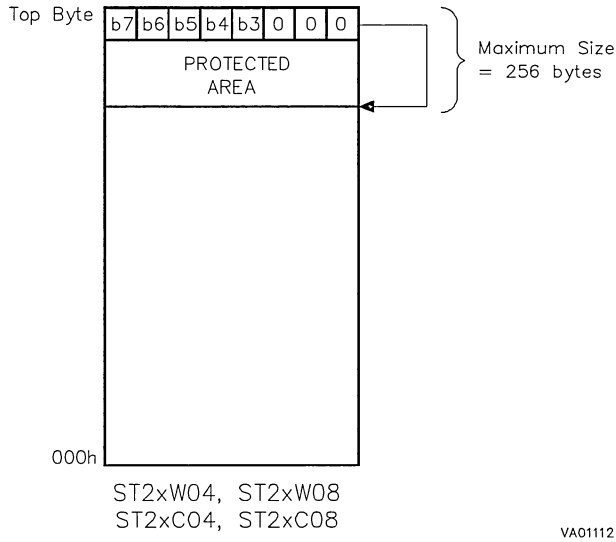
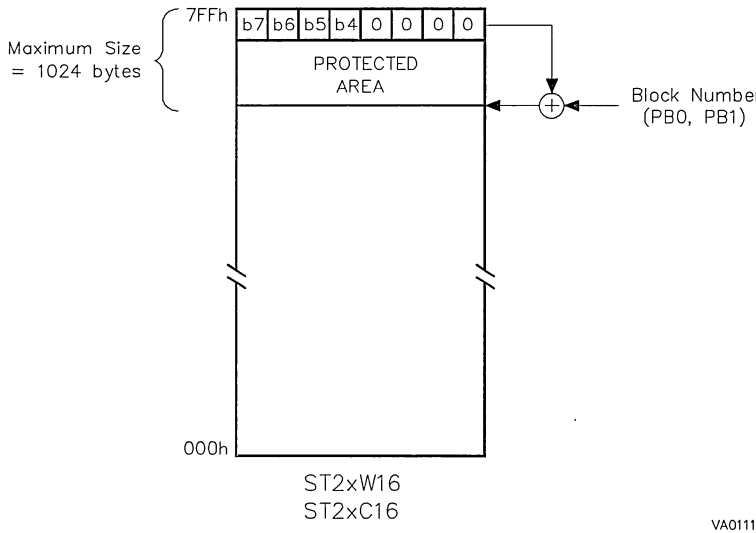


Figure 5. Address Pointer in 16K Device



PRE PROTECTION AND DEVICE PIN-OUT

The WriteProtect Enable feature is not available on all the ST24/25Cxx, ST24/25Wxx devices therefore the application designer should note that the pin-out of the ST24/25Cxx, ST24/25Wxx devices may differ for pins 1, 2 and 3. This device specific pin-out is related to the I^2C bus protocol when addressing devices of different memory size: for each ST24/25Cxx, ST24/25Wxx devices, the 4 MSB of the first byte (Device Select) are constant (1010), the following bits have a specific function dedicated to the size of the memory.

The following paragraph review the detail of each ST24/25Cxx, ST24/25Wxx device and the relationship between the pin-out and the PRE function.

ST24/25C01, ST24/25W01 (128 bytes)

The Device Select byte is composed of:

b7							b0
1	0	1	0	E2	E1	E0	R/W

where:

- E2 is the upper bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 2).
- E1 is the middle bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 1).
- E0 is the lower bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 0).

The Address Byte handles 7 significant bits, the MSB is a Don't Care bit (the ST24/25C01, ST24/25W01 is a 128 bytes memory, therefore addressed with only 7 bits). Pins 1, 2, 3 are E0, E1, E2 Chip Enable input pins (see Figure 6), this device does not offer the PRE feature.

ST24/25C02, ST24/25W02 (256 bytes)

The Device Select byte is composed of:

b7							b0
1	0	1	0	E2	E1	E0	R/W

where:

- E2 is the upper bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 2).
- E1 is the middle bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 1).
- E0 is the lower bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 0).

The Address Byte handles 8 significant bits (the ST24/25C02, ST24/25W02 is a 256 bytes memory, therefore addressed with 8 bits).

Pins 1, 2, 3 are E0, E1, E2 Chip Enable input pins (see Figure 6), this device does not offer the PRE feature.

ST24/25C04, ST24/25W04 (512 bytes)

The Device Select byte is composed of:

b7							b0
1	0	1	0	E2	E1	A8	R/W

where:

- E2 is the upper bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 2).
- E1 is the middle bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 1).
- A8 is the Memory Block number. A8 may also be considered as the upper bit of the address.

The Address Byte handles 8 significant bits (the ST24/25C04, ST24/25W04 is a 512 bytes memory splitted in 2 blocks of 256 bytes addressed with 8 bits). Pins 2, 3 are E1, E2 Chip Enable input pins (see Figure 6), pin 1 is the PRE input pin.

ST24/25C08, ST24/25W08 (1024 bytes)

The Device Select byte is composed of:

b7							b0
1	0	1	0	E2	A9	A8	R/W

where:

- E2 is the upper bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 2).
- A9,A8 is the Memory Block number. A9,A8 may also be considered as the upper bits of the address.

The Address Byte handles 8 significant bits (the ST24/25C08, ST24/25W08 is a 1024 bytes memory splitted in 4 blocks of 256 bytes addressed with 8 bits). Pin 3 is E2 Chip Enable input pin (see Figure 6), pin 2 is unused and pin 1 is the PRE input pin.

ST24/25C16, ST24/25W16 (2048 bytes)

The Device Select byte is composed of:

b7							b0
1	0	1	0	A10	A9	A8	R/W

where:

- A10,A9,A8 is the Memory Block number. A10,A9,A8 may also be considered as the upper bits of the address.

The Address Byte handles 8 significant bits (the ST24/25C16, ST24/25W16 is a 2048 bytes memory splitted in 8 blocks of 256 bytes addressed with 8 bits). Pin 1 is the PRE input pin, pins 2 and 3 are selecting the block of memory inside which the PRE pointer is defining the boundary of the protected area.

ST24/25E16 (2048 bytes)

The Device Select byte is composed of:

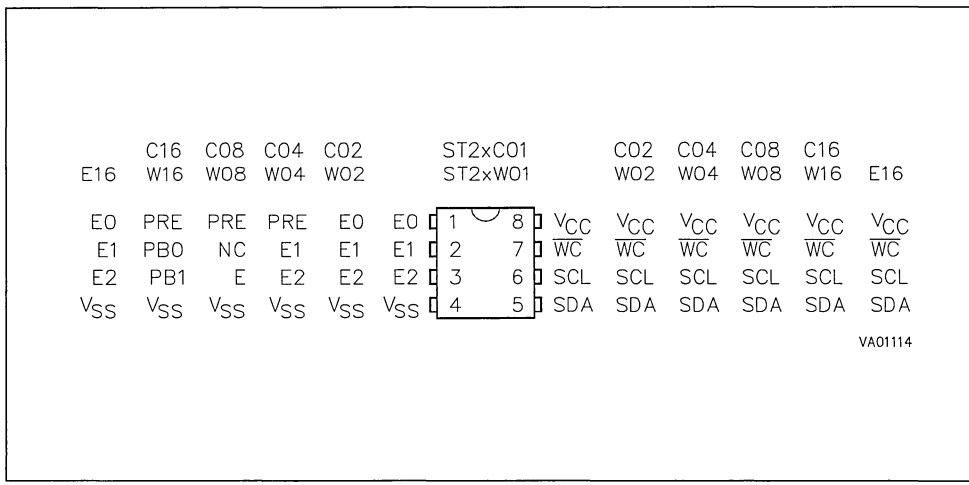
b7							b0
1	0	1	0	E2	E1	E0	R/W

where:

- E2 is the upper bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 2).
- E1 is the middle bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 1).
- E0 is the lower bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 0).

The Address Bytes handle 16 bits (the 11 Lower bits are significant). Pins 1, 2, 3 are E0, E1, E2 Chip Enable input pins (see Figure 6), the ST24/25E16 does not offer the PRE feature.

Figure 6. Pin Connections Compatibility in ST24/25Cxx, ST24/25Wxx Product Family



TIMEKEEPER SRAMs FIND MANY APPLICATIONS

Jerry MILLER

One aspect that is common among systems using microcomputers is the need to maintain configuration data, protected against corruptions that can occur at un-predicted power-downs.

POWER-FAIL SOLUTIONS

There are many options that a designer can select to provide Non-Volatile Memory in his system:

- FLASH MEMORY
- Serial or Parallel EEPROM
- NV-RAM
- Discrete solutions using SRAMs
- Integrated TIMEKEEPER products

FLASH Memories are able to store large amounts of data and have access times fast enough to allow direct access by the CPU. However, a FLASH MEMORY must be erased before it can be re-written and this means that existing data has to be buffered in DRAM while the erase process takes place. Moreover FLASH Memories are slow to erase and write (10-20 seconds in worst cases) which makes them unsuitable for fast power-fail back-up applications. Serial and Parallel EEPROM are better than FLASH MEMORY for re-writing as they are byte addressable and only the new data need be overwritten.

The Serial devices are, today at least, still of small capacity (16K max) and both Serial and Parallel need a relatively long time to write data (write cycle times are 5-10ms for page modes of 8-32 bytes which is still too slow for power-fail conditions).

The best solution then is a battery backed SRAM. This can be implemented by the designer in one of two ways, by designing his own power fail detect and battery switch-over circuitry, or by using the integrated ZEROPOWER® or TIMEKEEPER™ devices.

Figure 1. Work Station System Application

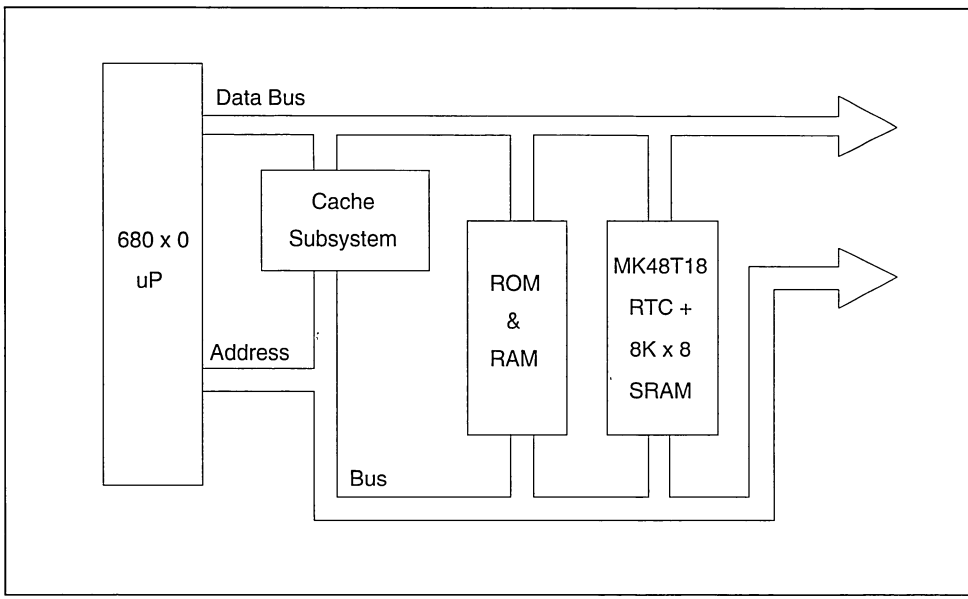


Figure 2. Data Acquisition System Application

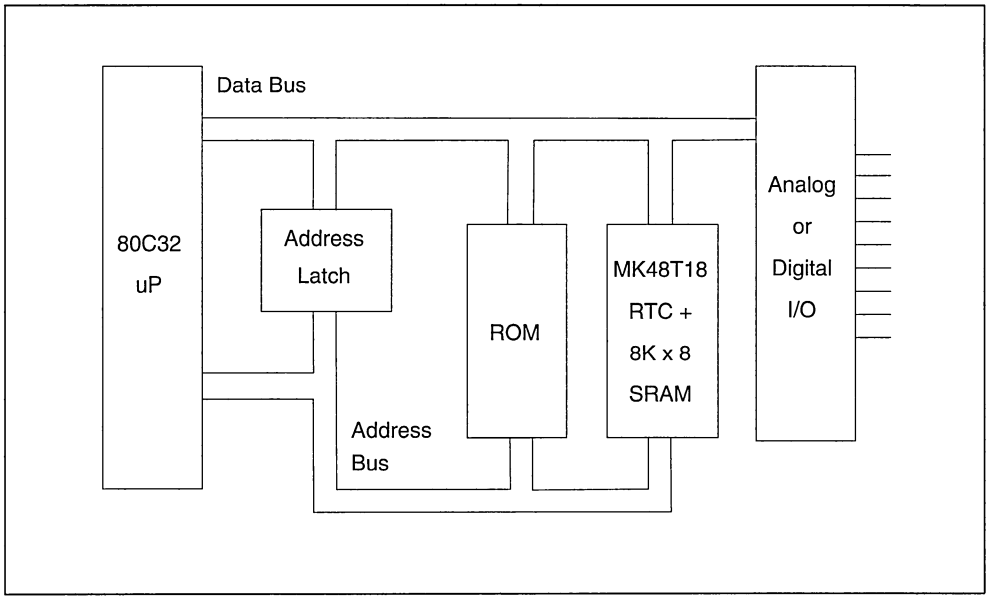
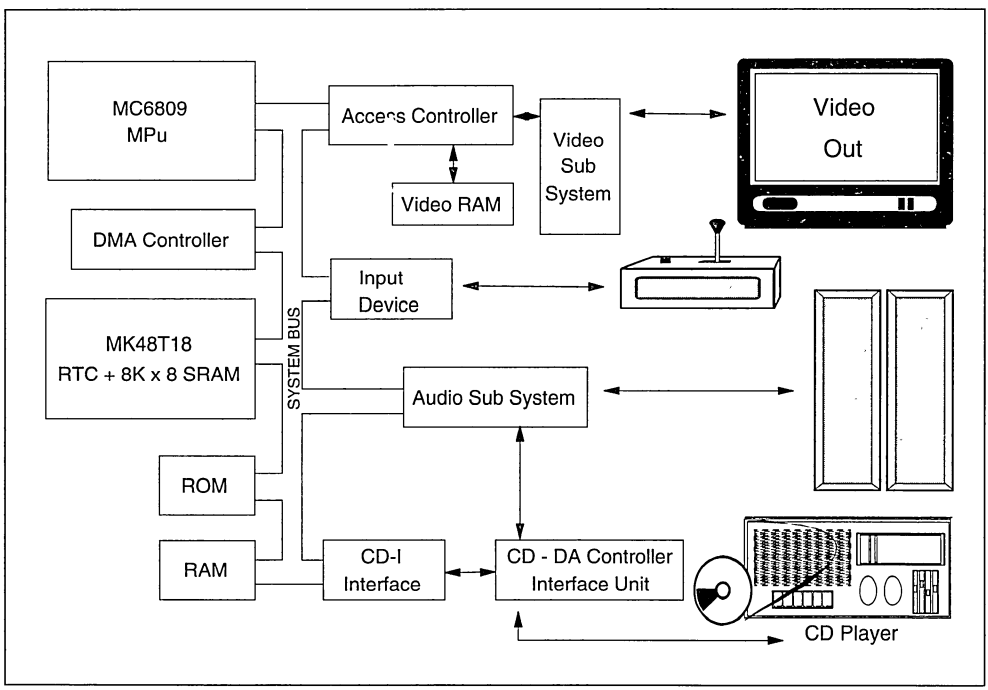


Figure 3. CDI ROM System Application



MAINTAINING TIME

Another key demand of many systems is to maintain a real time clock. Used for example in time and date stamping files or print-outs.

Specialised circuits are used with battery back-up to provide clock and calendar data to the CPU.

THE TIMEKEEPER SOLUTION

The TIMEKEEPER products provide one of the best solutions to both these needs. They incorporate up to 64K of battery backed SRAM and include on the SRAM chip all the circuitry to provide a smooth switch over from external to internal battery power in the case of a power failure. Also included on the chip is a very low power real time clock which maintains the time in a form easily readable by the CPU.

APPLICATIONS

Work Station System

A typical workstation can incorporate the MK48T08 or MK48T18 in the system memory map, in this way data in the memory can be read or written just as other data in the main ROMs or RAMs. Parameters such as system configuration data, clock and calendar information is stored in a completely Non-Volatile way, but available on-line.

A typical use of the time information in a workstation is the date and time stamp on files saved on the system disk drives (see Figure 1).

Data Acquisition System

Data acquisition systems collect analogue and/or digital information and store it until needed. Obviously one of the most important aspects is that the data acquired must be stored in a Non-Volatile memory to protect it against loss on power failure. Most data acquisition systems also need to record the time that each piece of data was acquired in order to be able to then reconstruct the map of events with an accurate time line.

Here again the battery backed SRAM stores the system configuration information and stores the acquired data. The real time clock provides time stamping for the data (see Figure 2).

CDI ROM System

A consumer system that uses the Non-Volatile memory with Real TIME CLOCK is the Compact Disk Interactive system. In the CDI system the SRAM stores the system configuration data and a directory of pointers to the images stored on the CD ROM, these are stored in the SRAM to provide very fast access time to the images for quick retrieval.

In addition the clock provides the system with time data for events, delays or time display (see Figure 3).

TIMEKEEPER APPLICATIONS

- **COMPUTERS:** workstations, mainframes, PC's, portables, VXI boards, VME boards, industrial controllers, POS terminals and data terminals.
- **FAX MACHINES**
- **INSTRUMENTS:** data loggers, utility meters, medical intruments, traffic signal controllers and test instruments.
- **TELECOM:** satellite receivers/decoders, cellular radios, modems,transmission cards and LAN's.
- **GAMES:** interactive CD, video games, security systems and slot machines.

These applications use TIMEKEEPERs for the following functions:

- Real Time Clock
- Configuration Files
- Boot Strap Programs
- Data Protection/Storage
- Real Time Clock for Time Stamping Data

TECHNICAL ARTICLE

Synchronous Burst SRAM for secondary CACHE systems

Ricky Tuttle
SGS-THOMSON Microelectronics
Carrollton, USA

The advent of high speed microprocessors and the requirement for high performance systems has opened the door to the Fast SRAM (FSRAM) market place. FSRAM is needed to provide the fast memory access for these high performance systems. SGS-THOMSON Microelectronics has developed the strategy and technology to be a major player in the world wide FSRAM market. The company's strategy includes asynchronous and synchronous SRAM products developed with a cutting-edge HCMOS technology.

The company has recently introduced four new products that are manufactured on its state-of-the-art 0.7µ, triple poly, double metal HCMOS process technology. There are two standard asynchronous FSRAM products organized as :

– 32K x 8 - M628032

– 128K x 8 - M628128

These standard SRAM devices are offered in different speed grades from 15-25ns for 40MHz to 66MHz clock rates. Also two Specialty, processor specific, CACHE Burst RAMs (BRAM™), the MK62486 and MK62940, have been introduced employing an on-chip 2-bit burst counter. The MK62486 and MK62940 each have a unique count sequence to suit the processor. All of these products are offered in JEDEC or industry standard pin-out configurations and package types.

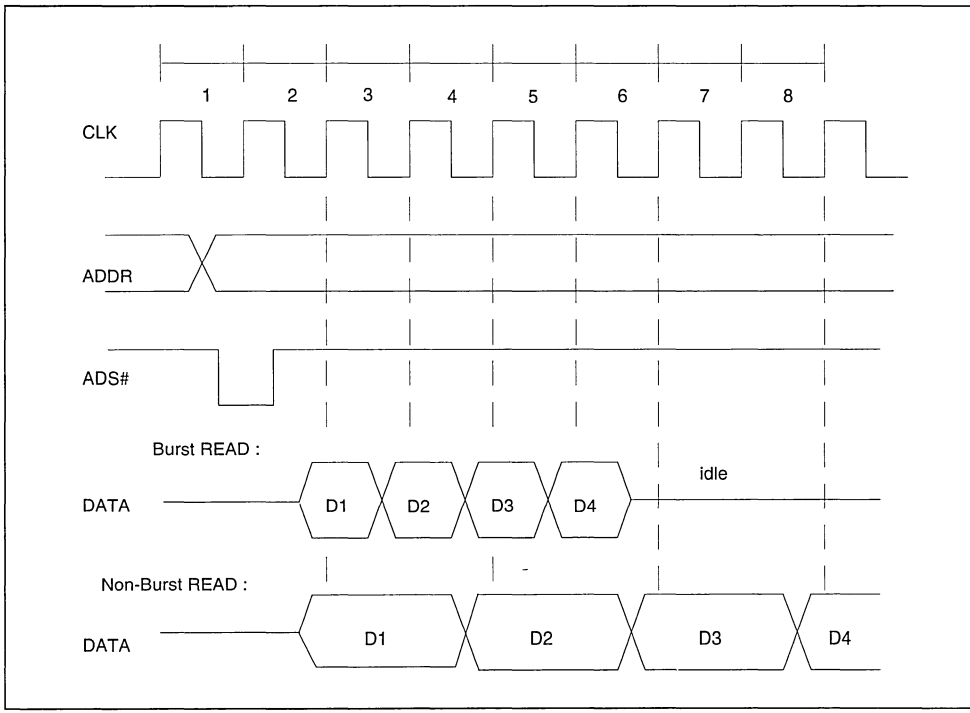
PROCESSOR SPECIFIC BRAMS

The two Specialty SRAMs are processor specific to either the i486™ microprocessor, or the 68040 microprocessor. The MK62486, 32K x 9 BRAM is for the 486 processor, and the MK62940 32K x 9 BRAM is for the 68040 processor. Both processors employ a Burst CACHE line-fill algorithm of 128 bits, but each processor has a unique burst sequence requirement of four (4) bursts of 32 bits (36 bits including parity). Therefore, the two devices incorporate a different 2-bit counter along with address and data registers. Both devices are organized as 32K x 9 with control pins that connect directly to the processor or Cache controller. The burst algorithm allows 16 bytes of data (128 bits) to be transferred in five (5) subsequent processor clock periods, whereas a non-burst sequence would take eight (8) clock periods. This can be seen in Figure 1. where data and clock cycles for both burst and non-burst are shown. As a comparison, the burst sequence with a 33MHz clock rate would allow data to be transferred at 106M bytes/second. In a non-burst sequence, only 66.5M bytes/second can be transferred with the same 33MHz clock (this comparison assumes zero-wait states). The advantage of the burst algorithm over a non-burst transfer is obvious for high performance systems.

CACHE ADVANTAGES

The i486 microprocessor has an on-chip primary Cache that is used for both data and instruction accesses. The Cache is organized as a four-way set associative Cache with 128 unique entries of 16 bytes each (2K x 4-way set) for a total primary Cache of 8k bytes. The on-chip Cache has a high hit rate and allows internal high speed processing

Figure 1. 16 Byte (128 bit) Line Fill



without external bus traffic. This is the basis of any Cache subsystem: to allow more performance in through-put with fewer external bus requests.

The larger the Cache the more entries of data and instructions it can hold. With all other factors being equal, a larger Cache will provide better system performance with a higher hit rate. Therefore, many 486 designs include a larger secondary Cache which is a Level Two (referred to as "L2") Cache subsystem. This is simply a second layer of high speed FSRAM between the primary or Level One "L1" Cache, and the system main memory composed of DRAM. As the "L2" Cache is a subset of the main memory, so the "L1" Cache is a subset of the "L2" Cache. Therefore, the "L2" Cache is larger than the on-chip primary Cache. Popular "L2" Cache sizes for 486 systems range from 64k and 128K bytes to 256K bytes.

"L2" CACHE ARCHITECTURE

Secondary Cache designs can use either a look-aside or look-through architecture. The look-aside Cache subsystem architecture allows all memory requests to be sent to main memory while the Cache executes a parallel look-up. If the Cache memory does not contain the requested data (miss), the main memory cycle continues. When the data is found in the cache "Hit", the main memory bus cycle is terminated, and the Cache sub-system supplies the data requested by the microprocessor. This type of design does not provide the best memory bus utilization since each request is forwarded to the system bus. Since both the main memory and Cache memory are accessed using the same memory bus, the look-aside architecture does not provide for bus concurrence. This means another bus master cannot access the main memory even when the microprocessor is operating out of Cache.

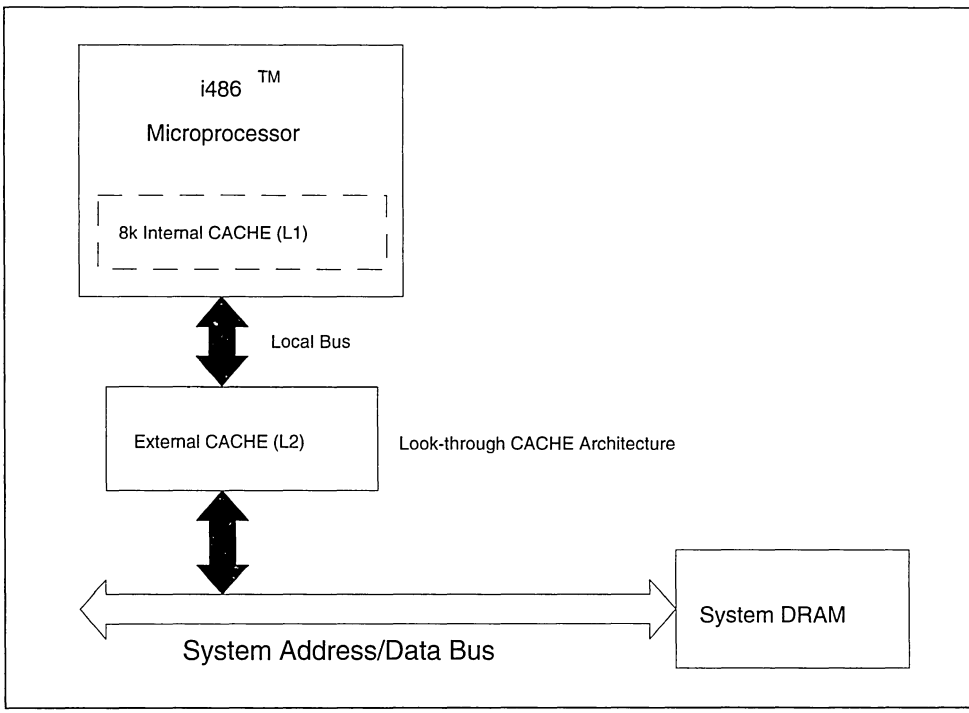
The look-through (or Serial) Cache architecture fits in series between the microprocessor and system main memory. It is a more complex design, but allows excellent system bus utilization and provides for bus concurrence. The look-through Cache reduces the number of memory requests to the global DRAM system bus. This means less system bus utilization which increases the overall system bus band width, and is an important factor in calculating how effective the Cache performs. Also, the look-through architecture allows the microprocessor to operate from the Cache memory while other bus masters can take advantage of the idle system bus. This is called concurrence processing. The only disadvantage is that the look-through design uses extra clock cycles to determine a hit or miss before transferring a memory request to the system bus. Of course a high hit rate defers this disadvantage by providing better overall system performance.

There are other factors that determine the performance of the Cache subsystem architecture such as set associativity, replacement or update policy such as write-through or write-back, line size, burst algorithms, and coherency control. These subjects can be studied by the reader in various printed literature. The main objective in Cache design is to have a high "Hit" rate. This is the percentage of memory requests that are determined as Cache hits, and can be calculated as :

$$\text{HIT RATE \%} = \frac{\text{Cache Hits}}{\text{Total Memory Requests}} \times 100\%$$

A high hit rate means that the microprocessor is operating from Cache memory, and has a low percentage of requests to the external system memory.

Figure 2. Look-through "L2" Block Diagram



It should be noted that the Cache hit rate is determined by the Cache hardware design and the software code being implemented. One cannot always assume that all software programs will benefit by the same amount from a particular Cache architecture. In short, Cache design should be tailored with considerations to the product application.

USING THE 32K x 9 BRAM IN "L2" CACHE DESIGNS

There are many chip sets now available for easy "L2" Cache designs for the i486 processor. These chip sets support the look-through Cache architecture with a local bus, and offer support of various Cache sizes, associativity, and replacement policies. Some vendors include the Cache controller, memory management unit (MMU), and bus control interface all in one device. Other vendors offer a "Set" of devices which include a Cache controller, a system local bus and memory controller, and a system bus I/O (ISA/EISA) bridge unit. Figure 3 is a block diagram of how a typical chip set will interface to the i486 microprocessor using a local bus configuration.

Many chip set Cache control units will support either asynchronous FSRAM or synchronous Cache RAM in their designs. Synchronous Cache RAM for the i486 is the MK62486 32K x 9 BRAM with an on-chip burst counter, and a self-timed write cycle. The MK62486 from SGS-THOMSON Microelectronics supports 2-1-1-1 zero-wait state read cycles, and is available now with clock to data access time of 19ns. These devices will fit in designs with clock rates up to 40MHz. The BRAM can be connected to the Cache controller unit. It should be noted that this is a general connection scheme, and actual pin and control connections may vary with the chip set units.

Figure 3. Local Bus Block Diagram

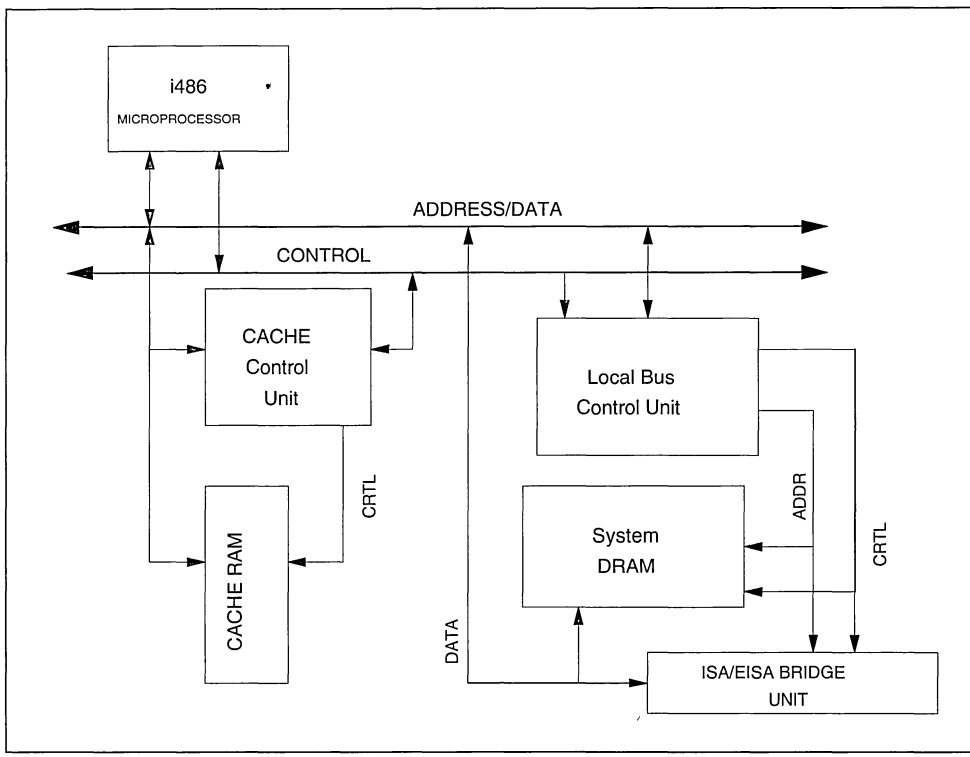
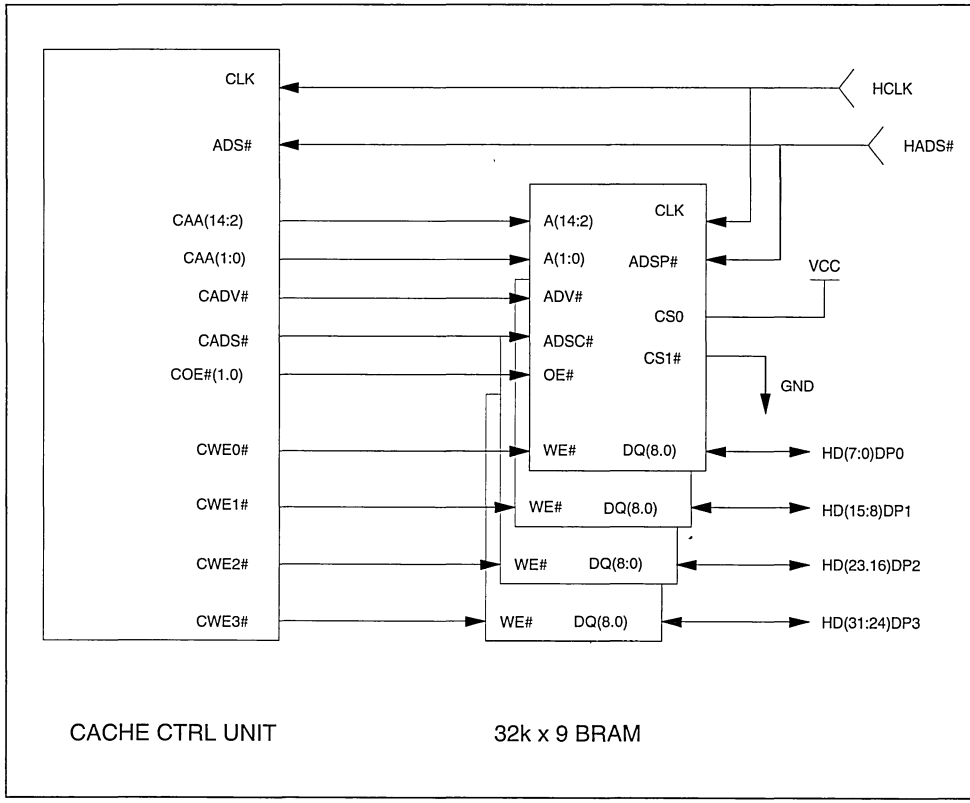


Figure 4. 128K Byte, Cache Control Unit Connections

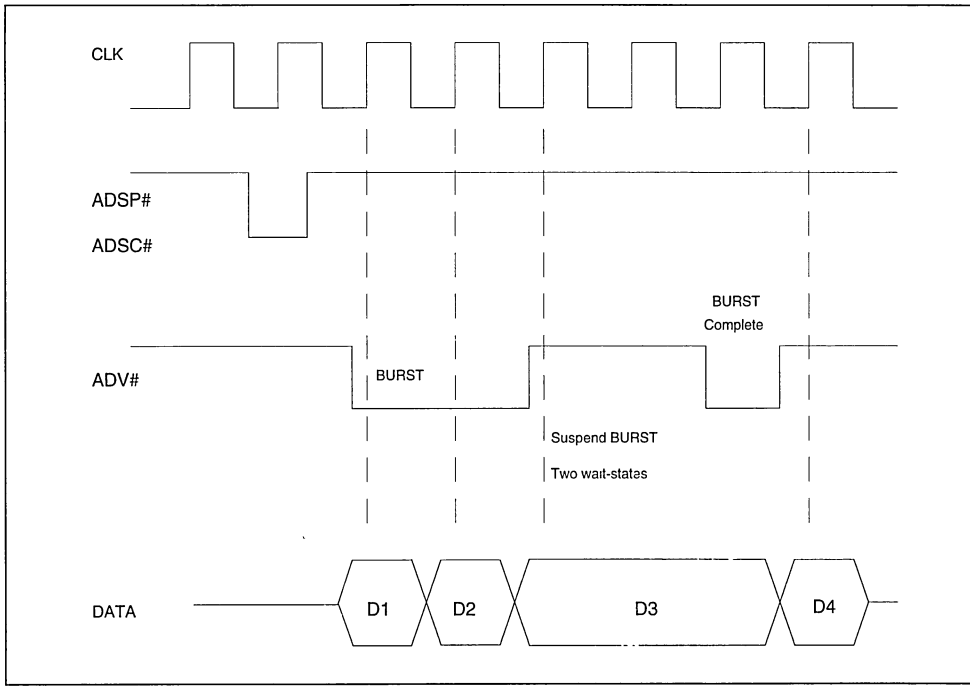


The BRAM provides several advantages over the standard SRAM. First, the BRAM has an on-chip burst address counter which is faster than any external address generator. Second, the device employs address and data registers to avoid external latches. Finally, the synchronous Cache RAM provides the best performance allowing the most design margin. In summary, the BRAM can provide for an easier design with more margin, lower real estate, and higher system performance. This results in better production yields with lower costs.

SGS-THOMSON will soon introduce a faster 32K x 9 BRAM device with access times of 12-14ns for processor clock rates to 66MHz. The faster 32K x 9 BRAM, dubbed M62486A, will meet Cache design requirements for faster 486 microprocessors or the new Pentium ™ 64-bit microprocessor. A synchronous device will be required to meet the zero-wait state operation the Pentium processor. The Cache BRAM will work for either microprocessor since the burst algorithm for the i486 and the Pentium are the same. The M62486A supports the zero-wait state 2-1-1-1 algorithm.

Another synchronous Cache RAM device to be introduced is the M62486R. This product is a 32K x 9 BRAM with registered outputs. The device has common I/O with registers on both the input and output circuitry. This allows for a pipe-line architecture during a burst read operation where data out is valid from the rising edge of the clock in 8ns. The M62486R will provide the necessary speed and design margin for 66MHz Pentium designs using a 3-1-1-1 burst algorithm. The Burst Read clock sequences are shown here for both the M62486A, and the M62486R. These 32K x 9 BRAM products from SGS-THOMSON will be further developed using a similar definition for two 64K x 18 BRAM family devices. The 64K x 18 organization will support Cache size upgrades without major redesign.

Figure 5. BRAM Asynchronous and Registered Outputs



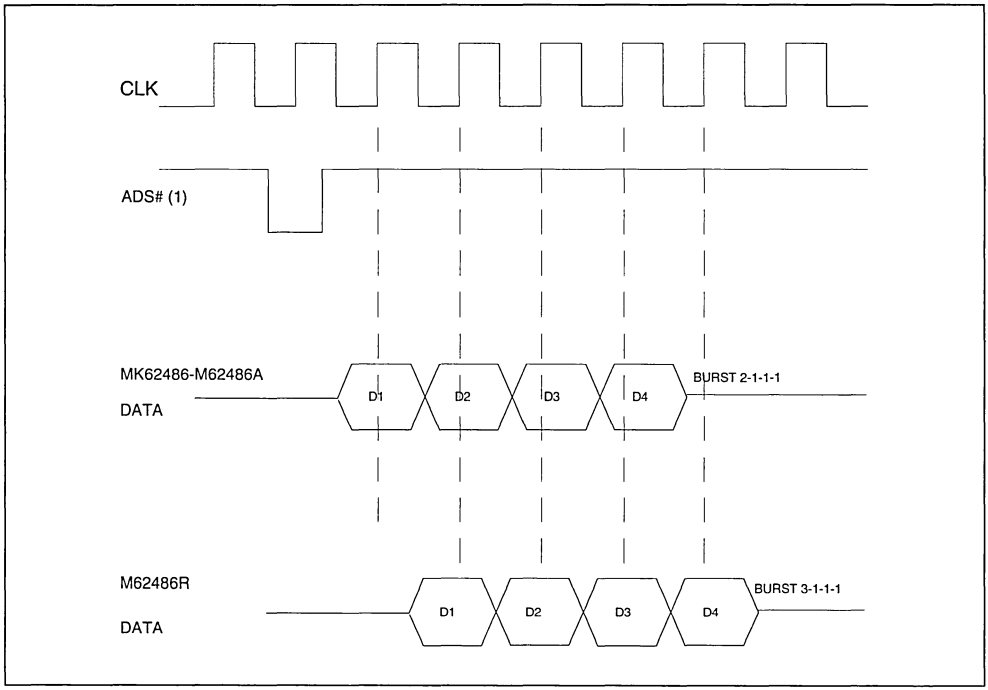
KEY BURST TIMING PARAMETERS

The BRAM can support burst read Cache line-fill cycles for the i486, or both burst write and burst read cycles for the Pentium microprocessor. Once the i486 microprocessor (or Pentium) has asserted a valid address, the BRAM registers the address at the rising clock edge where ADS# is asserted (Asserted in this context means an active signal). After the BRAM has registered the base address, the three subsequent addresses are generated by the on-chip burst counter. The BRAM allows wait states to be inserted in the burst sequence by using the ADV# control pin. The on-chip burst counter is not affected, and the burst sequence will continue as expected after the wait state(s) is completed. It is up to the Cache controller to abort a Cache line-fill or begin a new one. A burst cycle in the BRAM is always initiated by asserting either ADSP# or ADSC# at the rising edge of the clock. These signals allow the device to register a new base address, and set-up for the burst sequence.

The BRAM also allows immediate control of the data bus by featuring an asynchronous Output Enable (OE#). Although clock-to-data-out is the limiting access time, the fast Output Enable can provide data within 8ns after being asserted. This allows the OE# to be asserted later in the read cycle without access penalty. Using OE# as the output data bus control has no affect on the burst counter sequence. During wait-states the data bus can be driven to a high impedance state. Once the burst cycle continues, the data bus can become active for the duration of the burst without consequence to the burst algorithm. Figure 7 depicts the BRAM pin configuration in an industry standard 44-pin PLCC.

Today's popular microprocessors demand high speed memory products to keep pace with their Cache requirements. Many chip sets exist for quick "L2" Cache designs to meet the needs of these high speed microprocessors. They offer support of zero-wait state performance using either standard FSRAM or synchronous Cache Burst RAM.

Figure 6. Burst Counter Control Allows Wait-States



To meet this challenge, SGS-THOMSON has introduced four byte-wide fast SRAM products in a 0.7µ HCMOS technology. For a processor with a 32-bit data bus, only four (4) devices are required to provide from 128K bytes to 512K bytes of Cache memory as:

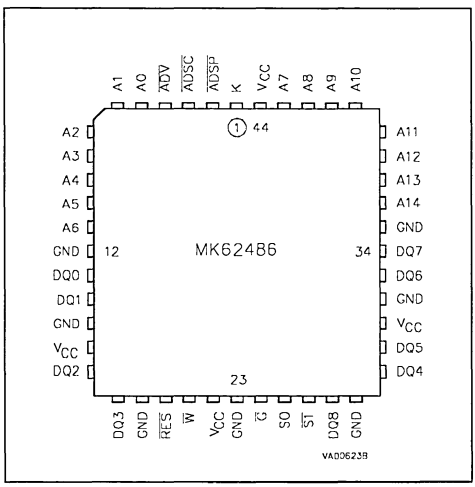
– 32K x 8 x (4) or 32K x 9 x (4) (128K bytes)

– 128K x 8 x (4) (512K bytes)

Larger Cache sizes for direct mapped or set associative Caches can be easily implemented.

Although the present 32-bit and 64-bit microprocessors have larger and faster "L1" Caches on-chip, the "L2" Cache needs for these data hungry processors is expected to remain for a long time. FSRAM and specialty synchronous Cache RAM provide the means to meet these high speed secondary Cache requirements.

Figure 7. MK62486 Top View



SGS-THOMSON MICROELECTRONICS

QUALITY NOTE

MEMORY PRODUCTS QUALITY PROGRAM

The Corporate quality program of SGS-THOMSON is published as the SURE (Semiconductor Users Reliability Evaluation) Program. The quality program for memory products follows closely this Program. Described here are the particular controls that apply specifically to memories starting with the Lot Acceptance and AOQ assessment and followed by the program for memory product qualification, an indication of the the manufacturing SPC (Statistical Process Controls) and the Short and Long term reliability tests.

Lot Acceptance

The role of a final Lot Acceptance sampling has changed from that of lot acceptance - although this still applies - more to the collection of statistical data about the outgoing quality, and the monitoring of the quality to the target defectivity in Parts Per Milion (ppm).

The Average Outgoing Quality (AOQ) is estimated from the results of Lot Acceptance testing. The measure developed by and used by SGS-THOMSON for the AOQ is known as the Average Outgoing Quality Estimator and is given by:

$$\frac{\text{Total Defective units in sample, with } d \leq c + 1}{\text{Total inspected units in samples of accepted lots}}$$

Where d = number of defects in sample, c = acceptance number. The totals are those of ALL lots inspected (1st, 2nd, etc controls).

This AOQE converges towards the real AOQ as the number of sampled lots increases, even though an acceptance number of zero is used.

Memort Product Qualification/Major Changes

Memory Product qualification is made on new memory products, new die designs and new packages and existing products when there are major changes to the design or manufacturing.

The tests performed depend on the parameters affected by a major change or the qualification of combinations of new die designs and new Plastic or Ceramic packages.

The tests performed are selected as appropriate from those listed in Tables 3 through 6.

Table 1. Finished Product Acceptance

Subgroup	Parameters	Minimum Sample Size	Acceptance Number
A1	Visual and mechanical inspection	315	0
A2+A3+A4	Cumulative electrical and inoperative mechanical failures	315	0

Table 2. Qualification

1	Wafer Fabrication Major Changes	Tests selected to control the parameters that are affected by the change, varying from the design or mask set to the fabrication plant.
2	Assembly Major Changes	Tests selected to control the parameters that are affected by the change, varying from package material changes to the assembly plant.
3	Product Qualification	Tests selected to control the parameters depending on the type of package and whether the die is new or already qualified.

Table 3. Product Qualification, Ceramic Packages - Package Related Tests

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Physical Dimensions	2016	Published Data
2	Bond Strength	2011	
3	Die Attach	2019 or 2027	
4	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1
5	Lid Torque	2024	
6	Internal Water Vapour	1018	5000 ppm (max)
7	Solderability:		
	– FDIP Package	2003	245°C, 5sec, Precondition Steam, 1hr
	– JLCC, LCCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air 150°C, 16hrs
8	Resistance to Solvents	2015	4 Solvent Solutions
9	Salt Atmosphere	1009	Test Condition A, 35°C, 24hrs
10	Lead Integrity	2004	Test Condition B2
11	Resistance to Soldering Heat		260°C, 10sec
12	Thermal Shock	1011	–55 to 125°C, 15 cycles
	Temperature Cycling	1010	–65 to 150°C, 100 cycles
	Moisture Resistance	1004	–10 to 65°C, RH = 90%
	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1
13	Mechanical Shock	2002	Test Condition B
	Vibration Variable Frequency	2007	Test Condition A
	Constant Acceleration	2001	Teat Condition E
	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1
14	Temperature Cycling	1010	–65 to 150°C, 10 cycles
	Constant Acceleration	2001	Test Condition E
	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1

Table 4. Product Qualification, Plastic Packages - Package Related Tests

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Physical Dimansions	2016	Published Data
	Coplanarity PLCC, PSOJ & JLCC Packages		Published Data
2	Bond Strength	2011	
3	Die Attach	2019 or 2027	
4	Solderability:		
	– PSO, PSOJ & PLCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs
	– PDIP package	2003	245°C, 5sec, Precondition Steam, 8hrs
5	Resitance to Solvents	2015	4 Solvent Solutions
6	Salt Atmosphere	1009	Test Condition A, 35°C, 24hrs
7	Lead Integrity	2004	Test Condition B2
8	Resistance to Soldering Heat:		
	– PSO, PSOJ & PLCC Packages		215°C, 40sec
	– PDIP Package		260°C, 10sec
9	Resistance to Surface Mounting:		
	Temperature Humidity:		85°C, RH = 85%
	– PSO Package		24hrs
	– PLCC & PSOJ Packages		48hrs
	Solder Dipping:		
	– PSO Package		260°C, 10sec
	– PLCC & PSOJ Packages		215°C, 120sec
	Visual Inspection		Body Cracks
	Pressure Pot		121°C, 2Atm, 168hrs

Table 5. Product Qualification, Ceramic Packages - Die Related Tests

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Operating Life Test	1005	140°C, V_{CC} = 5 to 7V, 500hrs
2	Operating Life Test	1005	125°C, V_{CC} = 5.5V, 1000hrs
3	Retention Bake (EPROM)	1008	250°C, 500hrs
4	Temperature Cycling	1010	–65 to 150°C, 1000 cycles
5	Thermal Shock	1011	–55 to 125°C, 500 cycles
6	Electrostatic Discharge	3015	1500Ω, 100pF, 2000V (min)
7	Electrostatic Discharge	EIAJ IC-121	0Ω, 200pF, 200V (min)
8	Latch-up	JEDEC STD-17	Current Injection 200mA (min), Overvoltage 14V (min)

Table 6. Product Qualification, Plastic Packages - Die Related Tests

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Operating Life Test	1005	140°C, V_{CC} = 5 to 7V, 500hrs
2	Operating Life Test	1005	125°C, V_{CC} = 5.5V, 1000hrs
3	Retention Bake (OTP, EEPROM)	1008	150°C, 1000hrs
4	Write/Erase Cycling (EEPROM, FLASH)		Published Data
5	Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5.5V, 1000hrs
6	Temperature Cycling	1010	–40 to 150°C, 1000 cycles
7	Thermal Shock	1011	–55 to 125°C, 500 cycles
8	Pressure Pot		121°C, 2Atm, 168hrs
9	HAST	CECC 90,000	130°C, RH = 85%, 96hrs
10	Electrostatic Discharge	3015	1500Ω, 100pF, 2000V (min)
11	Electrostatic Discharge	EIAJ IC-121	0Ω, 200pF, 200V (min)
12	Latch-up	JEDEC STD-17	Current Injection 200mA (min), Overvoltage 14V (min)
13	Soft Error Testing (SRAM)		

Statistical Process Control

One of the most powerfull tools implemented throughout the production of memory products is SPC. The final goal of the SPC program is to bring each critical step of the process to "6 Sigma" capability ($Cp \geq 2$). Current controls are at Cp and Cpk 1.33. For example, in a typical wafer processing line more than 200 variables may be controlled for SPC. Data is gathered and analysed by on-line computers and provides up-to-the minute control charts (eg $\bar{X}$, R charts). The critical process steps are defined by FMEA (Failure Mode and Effects Analysis).

A selection of the most important SPC steps and the Cp and Cpk results is regularly available and can help customers to avoid the costly qualification of new products when the products come from a qualified design and a manufacturing process that is demonstrated to be under control.

The Table 7 and Table 8 show some typical SPC results from both wafer fabrication and assembly processes.

Table 7. Statistical Process Control, Wafer Fabrication, CMOS EPROM (1.2 micron)

#	Parameter	Dependant Performance	4q91		1q92	
			CP	CPK	CP	CPK
1	VTH Field Minimum P-Channel Transisitor	Latch-up Related	2.49	1.58	2.84	1.81
2	VTH Field Minimum N-Channel Transistor	Latch-up Related	2.28	2.42	2.62	2.42
3	Gate Oxide Thickness	Data Retention & ESD	1.60	1.55	1.68	1.65
4	Interpoly Oxide Thickness	Data Retention	1.70	1.64	1.43	1.41
5	Intermediate Dielectric Thickness	Data Retention	1.46	1.36	1.44	1.34

Table 8. Statistical Process Control, Ceramic Package Assembly EPROM

#	Parameter	Dependant Performance	4q91		1q92	
			CP	CPK	CP	CPK
1	Shear Test	Die Attach	1.69	1.69	2.20	2.20
2	Bond Strength	Bond Weakness	2.17	2.15	2.50	2.50
3	Torque Test	Hermeticity	2.40	2.19	1.70	1.70
4	Lead Plating Thickness	Solderability	1.50	1.13	1.70	1.90

Short Term Reliability Testing

In order to provide a rapid feedback on product reliability to manufacturing, a series of Short Term Reliability tests are performed on a lot-by-lot or weekly basis. These are summarised in Table 9 and Table 10.

Table 9. Short Term Reliability Tests, Ceramic Packages

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Thermal Shock	1011	–55 to 125°C, 60 cycles
2	Retention Bake (EPROM)		180°C, 72hrs
3	Solderability	2003	245°C, 5sec, Precondition Steam, 1hr
4	Resistance to Solvents	2015	4 Solvent Solutions
5	Physical Dimensions	2016	Published Data
6	Lead Integrity	2004	Test Condition B2
7	Hermeticity:	1014	
	– Fine Leak		Test Condition A1
	– Gross Leak		Test Condition C1
8	Lead Torque	2024	

Table 10. Short Term Reliability Tests, Plastic Packages

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Temperature Cycling	1010	–40 to 150°C, 100 cycles
2	Write/Erase Cycles (EEPROM & FLASH)		Published Data
3	Solderability:		
	– PSO, PSOJ & PLCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs
	– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs
4	Resistance to Solvents	2015	4 Solvent Solutions
5	Physical Dimensions	2016	Published Data
6	Lead Integrity	2004	Test Condition B2
7	Pressure Pot		121°C, 2Atm, 168hrs

Long Term Reliability Testing

Long Term Reliability tests are performed to provide evidence of the life time reliability of memory products. Sampling is made either monthly, 3 or 6 monthly depending on the tests performed. Table 11 and Table 12 summarise the tests.

Table 11. Long Term Reliability Tests, Ceramic Packages

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Operating Life	1005	125°C, V_{CC} = 5 to 6V, 1000hrs
2	Retention Bake (EPROM)	1008	250°C, 500hrs
3	Thermal Shock	1011	–55 to 125°C, 15cycles
	Temperature Cycling	1010	–65 to 150°C, 100cycles
	Moisture Resistance	1004	–10 to 65°C, RH = 90%, 10 cycles of 24hrs
	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1
4	Mechanical Shock	2002	Test Condition B
	Vibration Variable Frequency	2007	Test Condition A
	Constant Acceleration	2001	Test Condition E
	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1
5	Temperature Cycling	1010	–65 to 150°C, 10 cycles
	Constant Acceleration	2001	Test Condition E
	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1
6	Electrostatic Discharge	3015	1500Ω, 100pF, 2000V (min)
7	Salt Atmosphere	1009	Test Condition A, 35°C, 24hrs
8	Internal Water Vapour	1018	5000 ppm (max)
9	Temperature Cycling	1010	–65 to 150 °C, 500 cycles

Table 12. Long Term Reliability Tests, Plastic Packages

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Operating Life	1005	125°C, V_{CC} = 5 to 6V, 1000hrs
2	Retention Bake (OTP & EEPROM)	1008	150°C, 1000hrs
3	Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5.5V, 1000hrs
4	Electrostatic Discharge	3015	1500Ω, 100pF, 2000V (min)
5	HAST	CECC 90,000	130°C, RH = 85%, 96hrs
6	Temperature Cycling	1010	–40 to 150 °C, 500 cycles

Conclusion

SGS-THOMSON believes that the extensive attention given to process control and product evaluation, combined with clear design rules and a well designed technology base, give the Company a world class overall quality rating.

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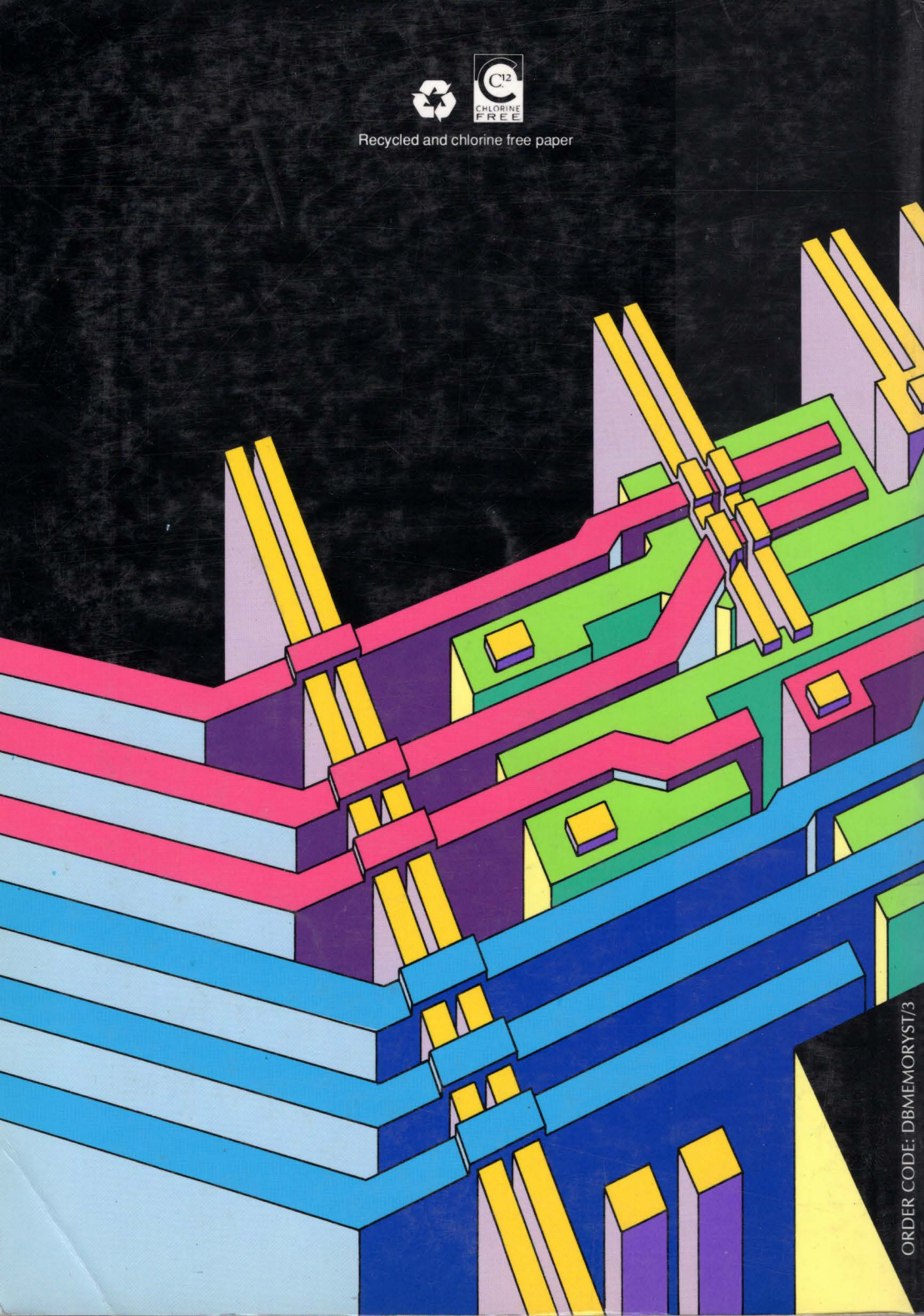

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