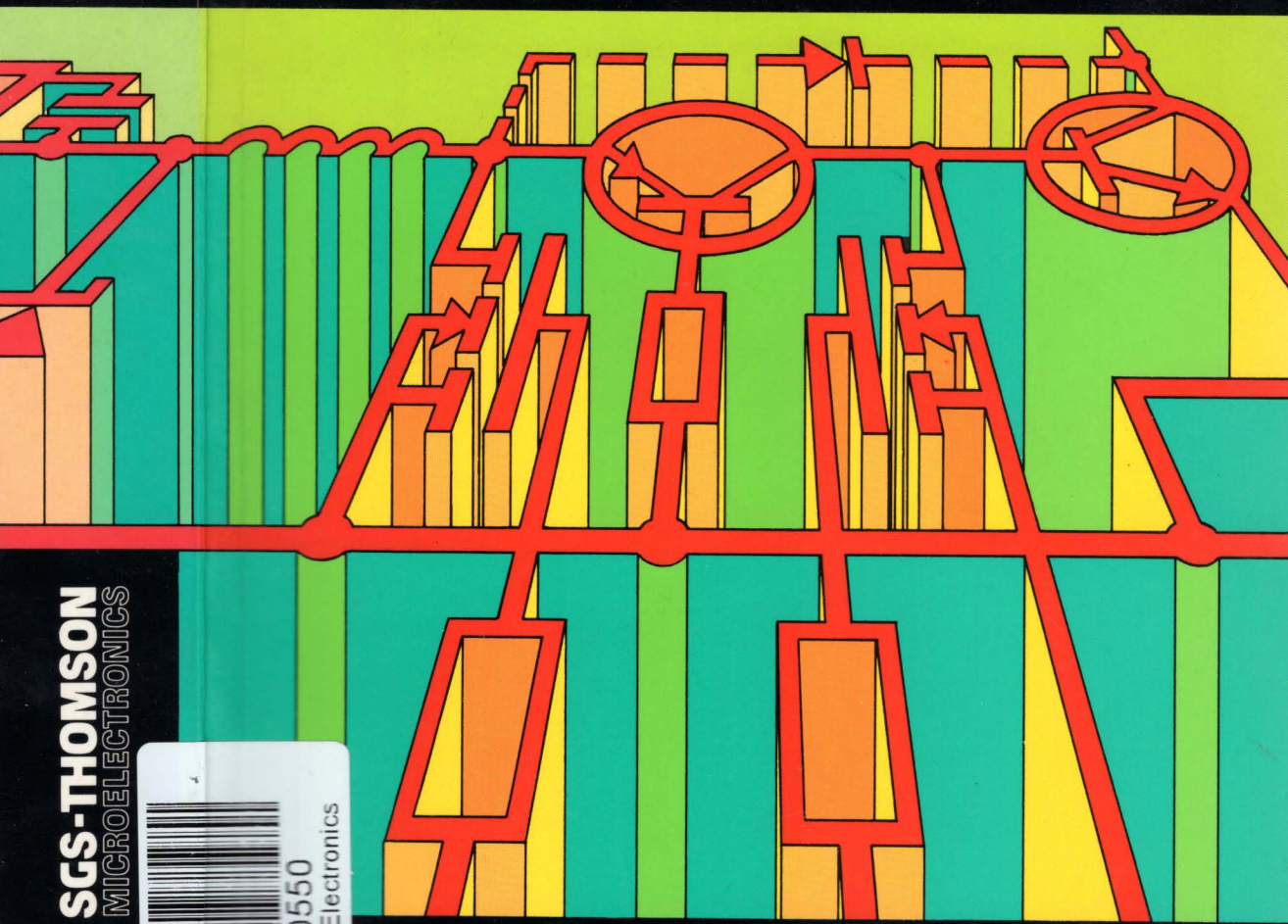


DISCRETE POWER
SEMICONDUCTOR
HANDBOOK

DISCRETE POWER SEMICONDUCTOR

HANDBOOK

1st EDITION



SGS-THOMSON
MICROELECTRONICS



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DISCRETE POWER SEMICONDUCTOR

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APRIL 1995

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TABLE OF CONTENTS

INTRODUCTION	Page 5
---------------------	---------------

GENERAL INDEX	7
----------------------	----------

APPLICATION NOTES

POWER SEMICONDUCTOR BASICS

– SEMICONDUCTOR DEVICES	11
– DRIVE, CONTROL and PROTECTION	277
– CIRCUITS and TOPOLOGIES	337
– THERMAL MANAGEMENT and PCB LAYOUT	407

APPLICATIONS OF POWER SEMICONDUCTORS

– SWITCH MODE POWER SUPPLIES	443
– MOTOR CONTROL	481
– AUTOMOTIVE APPLICATIONS	547
– LIGHTING APPLICATIONS	587
– TELEVISION and MONITORS	611

INTRODUCTION

This book is intended as an update of the publication "The Power Transistor in its Environment", written as an introduction to power electronics for students and engineers, and as a guide for designers.

This new book reflects the changes which have occurred in the semiconductor industry since that time. Whereas "The Power Transistor in its Environment" covered only Power Bipolar transistors and diodes, to fully represent SGS-THOMSON's power product range, any current book must also include Power MOSFETs, IGBTs, Smart Power devices, thyristors and TRIACs. As with all semiconductor technologies, power semiconductors continue to advance, and new markets and applications develop all the time; examples of market areas which have appeared or grown drastically in recent years include a large number of automotive applications, electronic lamp ballasts, and solid-state replacements for relays. Meanwhile older applications continue to evolve.

SGS-THOMSON maintains its position at the cutting edge of these technologies. We continue to develop innovative new devices and packages, such as VIPower, our proprietary smart high-power technology, and the PowerSO series of packages, the world's first true power SMD package, leading the trend toward surface mounting of power applications. Details of all aspects of SGS-THOMSON's power products can be found in this book. The first part covers the basics of power semiconductors, providing an introduction to the characteristics of the various classes. Bipolars, MOSFETs, IGBTs, TRIACs and diodes are discussed. The second half describes applications of these devices, using circuits developed in our application laboratories as examples, giving guidelines to help in the design of real-world systems. Topics include power supplies, motor control, lighting and television deflection.

GENERAL INDEX

SEMICONDUCTOR DEVICES

BASICS

	Page
AN512 – Characteristics of Power Semiconductors	13
AN656 – Power Transistors - Devices and Datasheets	27
AN480 – Series Connection of MOSFET, Bipolar and IGBT Devices	35

POWER MOSFETs

AN657 – An Introduction to Power MOSFETs	49
AN473 – A New Approach to Parameter Extraction for the Spice Power MOSFET Model	65
AN475 – Gate Charge Characteristics Lead to Easy Drive Design for Power MOSFET Circuits	71

IGBTs

AN521 – An Introduction to IGBTs	81
AN478 – How Short Circuit Capabilities Govern the Desired Characteristics of IGBTs	91
AN476 – Safe Behaviour of IGBTs Subjected to dV/dt	101
AN477 – Static and Dynamic Behaviour of Paralleled IGBTs	111
AN479 – Switching with IGBTs: How to Obtain a Better Performance	125
AN466 – An Analysis of Losses in an IGBT	135

BIPOLAR TRANSISTORS

AN363 – Bipolar Transistors and Darlington: Design, Function Control and Protection	145
---	-----

TRIACS

AN301 – The Nature of Triacs	169
AN439 – Improvement in the Triac Commutation	199

INTELLIGENT POWER

AN525 – An Introduction to Intelligent Power	211
AN516 – From Standard to Intelligent MOSFETs	221

POWER DIODES

AN370 – Analysis and Optimisation of High Frequency Power Rectification	231
AN604 – The Conduction Losses in a Power Rectifier	243
AN443 – Series Operation of Fast Rectifiers	245
AN599 – Parallel Operation of Power Rectifiers	253
AN601 – New High Voltage Ultra-Fast Diodes: the Turboswitch™ A & B Series	261
AN603 – Turboswitch™ in a PFC Boost Converter	265
AN602 – Modelling Parallel Operation of Power Rectifiers with PSPICE	271

GENERAL INDEX

DRIVE, CONTROL and PROTECTION

DRIVES

	Page
AN509 – Influence of Gate and Base Drive on Power Switch Behaviour	279
AN524 – Drive Circuits for Power MOSFETs and IGBTs	291
AN461 – An Isolated Gate and Base Drive for Power MOSFETs and IGBTs	301
AN351 – Novel Protection and Gate Drives for MOSFETs Used in Bridge Leg Configurations	309
AN472 – Drive Circuit for Integration with IGBTs	315

PROTECTION

AN328 – Protect Your Triacs	323
AN316 – How to Choose a Transil	327
AN318 – Transil or Varistor	333
AN444 – Transistor Protection by Transil: Dissipation Power and Surge Current Duration	335

CIRCUITS and TOPOLOGIES

AN253 – Power Supply Design Basics	339
AN513 – Topologies for Switch Mode Power Supplies	345
AN523 – Understanding Power Factor	363
AN510 – Circuits for Power Factor Correction with Regards to Mains Filtering	369
AN659 – Digital Power Factor Correction with Non-Sinewave Current	379
AN658 – Resonant Converter Topologies	389
AN662 – IGBTs in Resonant Converters	395
AN661 – Calculation of the Losses in a Chopper Topology	403

THERMAL MANAGEMENT and PCB LAYOUT

AN358 – Design of Low Inductive PCBS	409
AN526 – Plastic Packages for Power Discretes and ICs	419
AN515 – The PowerSO-10™ A new Surface Mount Power Package	435

SWITCH MODE POWER SUPPLIES

AN486 – A Cost Effective Ultra Fast Ni-Cd Battery Charger	445
AN356 – Use of Internal MOSFET Diode in Bridge-Legs for High Frequency Applications	451
AN511 – Modular Design for Multi Output SMPS with Synchronous Post Regulation	461
AN389 – Automatic Mains Selector	475

MOTOR CONTROL

AN663 – Comparison of MOSFET and IGBT Transistors in Motor Drive Applications	483
AN424 – Versatile and Cost Effective Induction Motor Drive with Digital Three Phase Generation	487
AN359 – Compact High Performance Brush DC Motor Servo Drives Using MOSFETs	501
AN235 – Stepper Motor Driving	511
AN522 – Pulse Controlled Inverter	527
AN519 – PWM Technique for Acoustic Noise Reduction in Power Applications	533
AN660 – Digital Control for a Brush DC Motor	539

GENERAL INDEX

AUTOMOTIVE APPLICATIONS

Page

AN514 – High Side Drivers	549
AN484 – Car Ignition with IGBTs	569
AN517 – The VB027 - Electronic Ignition in VIPower™ Technology	579

LIGHTING APPLICATIONS

AN527 – Electronic Fluorescent Lamp Ballast	589
AN518 – Soft Light Dimmer	599
AN528 – Electronic Transformer for 12V Halogen Lamp	607

TELEVISIONS and MONITORS

AN520 – Transistors for Horizontal Deflection in Televisions and Monitors	613
AN600 – TV and Monitors: Choice of a Diode for Horizontal Deflection	623

SEMICONDUCTOR DEVICES BASICS

CHARACTERISTICS OF POWER SEMICONDUCTORS

by J. M. Peter

ABSTRACT

This paper aims to give a brief overview of the essential characteristics of power semiconductors, and to provide a guide in their selection for particular applications.

It considers the characteristics of various power components when operating like a switch - either blocking current or voltage, or conducting with a small voltage drop.

Their behaviour is examined in terms of:

- (i) Typical current and voltage ratings (switchable power) permanent current - short overcurrent;
- (ii) The switching behaviour: switching speed and switching losses;
- (iii) Drive requirements.

Advantages and disadvantages are summarised, and the relative cost of each solution indicated.

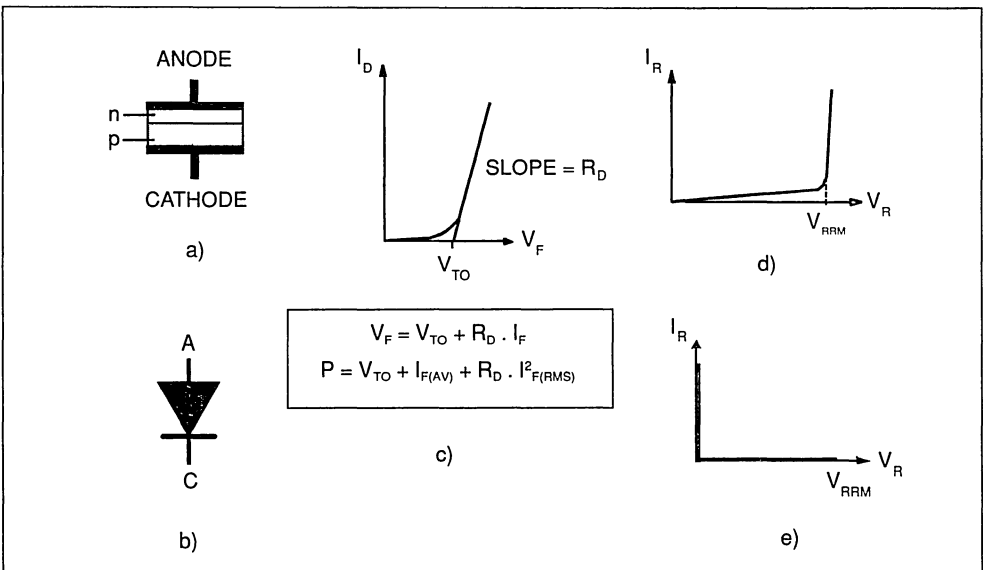
Currently, the main types of power semiconductors are the Power Diode, the power Bipolar Junction Transistor (BJT), the Thyristor (Triacs and SCRs), the Gate Turn-off Thyristor (GTO), the Power MOSFET, and the Insulated Gate Bipolar Transistor (IGBT).

2 THE POWER DIODE see figure 1.

2.1 Current

The physical parameter which limits current is the maximum junction temperature; the temperature at which destruction of the device occurs. Hence the maximum current in a diode depends essentially on the cooling; in practical terms on the thermal resistance (for DC operation), and on the thermal

Figure 1. Power Diode: a) Simplified structure
 b) Circuit symbol
 c) Current limits
 d) Voltage limits
 e) Safe Operating Area



impedance (for short duration surge currents).

2.2 Voltage

The device is destroyed if the electric field across the N region of the diode becomes strong enough to cause breakdown - hence the voltage ratings of the transistor (forward, V_F and reverse, V_{DRM}) depend upon the thickness of this region.

2.3 Switching

Power PN diodes have a "memory" effect due to the storage of minority carriers. If the voltage across a diode which has been conducting in the forward direction is suddenly reversed, the p and n regions of the diode are still full of minority carriers, which can cause the diode to behave like a short circuit for a short period of time until the minority carrier density falls. The reverse current due to this effect can cause problems: current spikes, noise, overvoltages, and supplementary switching losses.

Figure 2 shows the turn-off behaviour. The main parameter is the reverse current, I_{RM} , and in some case the recovery charge Q_r . The reverse current increases with dI_F/dt (slope of decreasing current before turn-off) and with junction temperature.

A fast PN diode is a diode made with a reduced minority-carrier lifetime, which leads to a reduction in the diffusion length (ie the average distance travelled by a minority carrier before recombination).

If the diffusion length is shorter than the thickness of the silicon N region, the diode's on-resistance increases drastically. However the maximum voltages that the diode can withstand depend upon the thickness of this region. The design of a fast diode is therefore the result of a trade-off between maximum voltage V_{DRM} , forward voltage drop V_F and speed (t_{rr}) - see figure 3.

Figure 4 shows losses introduced by a freewheel diode. Using a faster diode reduces these losses, but it is not always possible to have an ultra fast diode with a high voltage rating. Instead it could be possible to use several low voltage ultra-fast diodes in series - see reference [3].

When the diode switches off in series with an inductance L, a supplementary energy $L.I_{RM}^2$ is dissipated in the circuit. For this reason the choice of circuit configuration is very important (figure 5).

2.4 Schottky Power Diodes

Schottky power diodes, which use only majority carriers, have a different behaviour; they have a smaller voltage drop and no recovery charge, and are many times faster than PN diodes. However, they have the disadvantages of a limited voltage range (60 to 100V) and a very high internal capacitance. The leakage current is also large, and becomes larger at high temperatures.

Figure 2. Diode turn-off behaviour

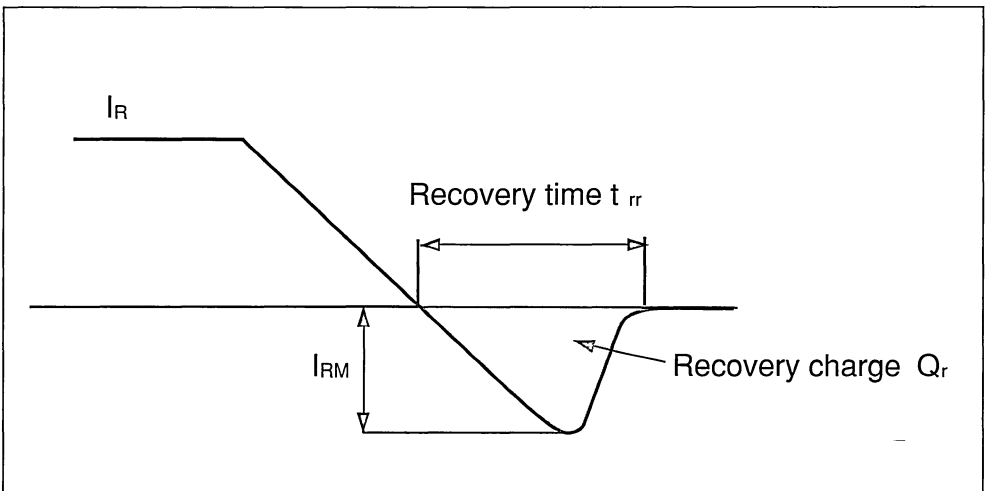


Figure 3. Speed versus V_{DRM}

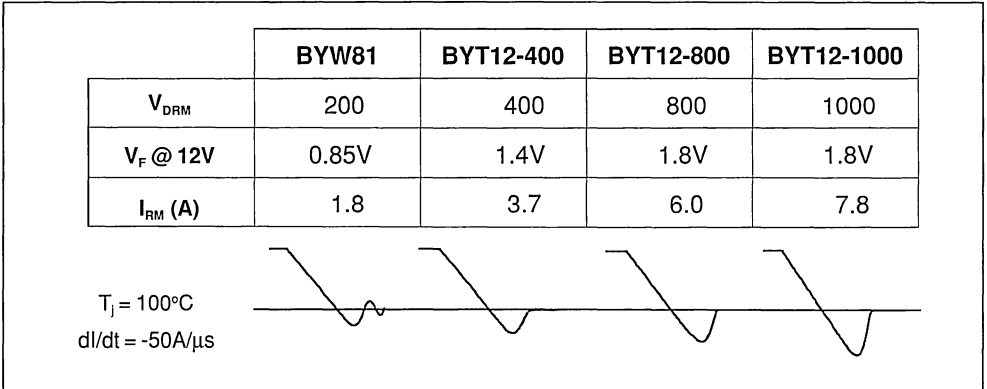


Figure 4. Freewheel diode losses

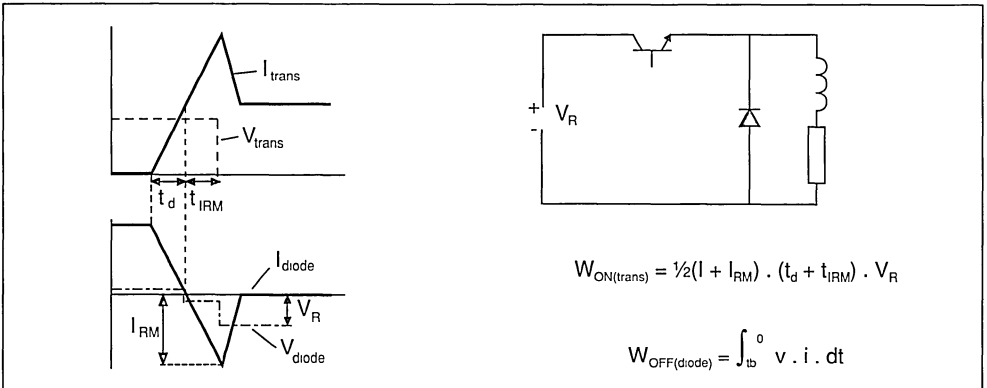
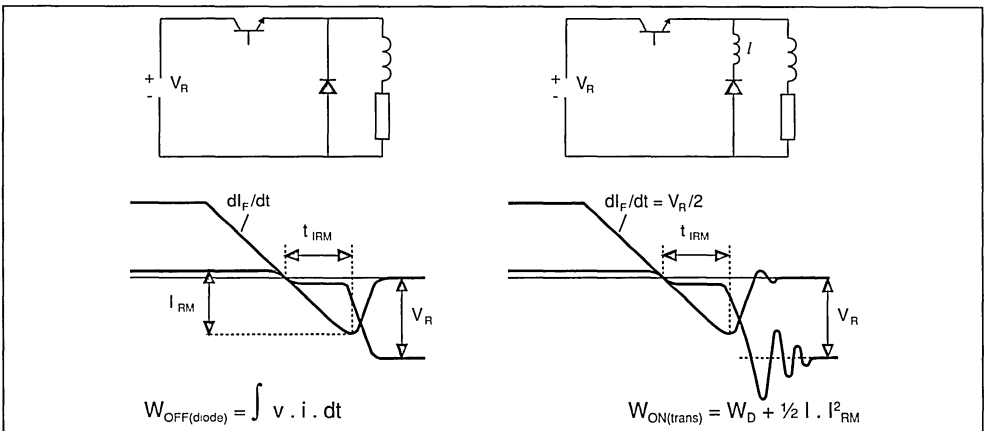


Figure 5. Effect of circuit topology on diode behaviour



3 THE BIPOLAR TRANSISTOR see figure 6.

3.1 Current

The current capability is defined by:

$$V_{CE(sat)} < 1.5V \quad @ \quad \begin{matrix} I_C = I_{C(sat)} \\ I_B = I_{B(sat)} \end{matrix}$$

If $I_C < I_{C(sat)}$, the voltage drop V_{CE} is proportional to it, and can be very small.

If $I_C > I_{C(sat)}$, V_{CE} remains relatively constant with changing I_C , and so the transistor can be considered as a current source.

The bipolar transistor has no overcurrent capability (I_C cannot exceed $I_{C(max)}$), and this maximum operating current is defined by the gain, not by thermal considerations.

3.2 Voltage

Two parameters define bipolar transistor voltage capability:

- V_{CEV} , the maximum voltage with the base emitter junction blocked ($V_{CEV} = V_{CBO}$, the maximum collector-base voltage).

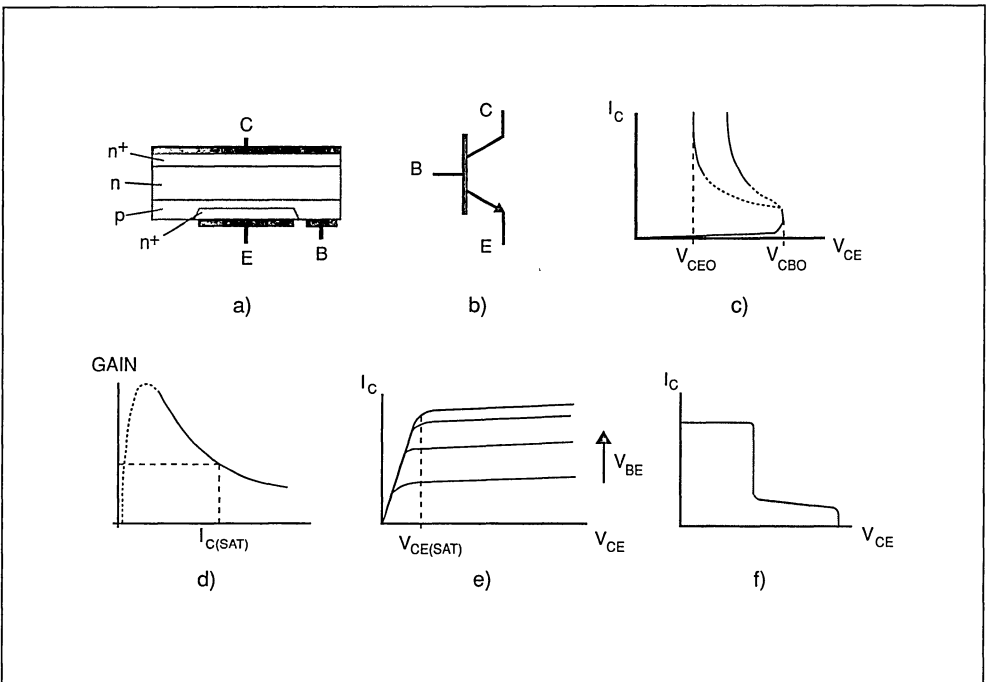
- V_{CEO} , the maximum voltage with base open.

For switching applications, voltage limits are defined by the Safe Operating Area (SOA). (V_{CEW} , the working voltage at high current, is often equal to V_{CEO}).

Maximum capabilities for the early 1990s

	V_{CEO}	V_{CEV}	$I_{C(sat)}$
Fast transistors	800V	1300V	60A
Slow transistors	1000V	1400V	400A

Figure 6. The Bipolar Transistor: a) Simplified structure b) Circuit symbol c) Gain characteristics d) Output characteristics e) Forward breakdown characteristics f) Forward-bias safe operating area (FBSOA)



Voltage drop: If $I_C < I_{C(sat)}$ the voltage drop (with optimised drive) is very low.

$$V_{CE} = \frac{I_C}{I_{C(sat)} \cdot V_{CE(sat)}}$$

3.3 Drive requirements

See figure 7.

The BJT is a current-driven device: during the conducting phase its necessary to deliver a base current

$$I_{B1} = \frac{I_C}{\beta} \quad \beta = \text{gain}$$

At nominal current the gain specified for low voltage transistors ($V_{CE0} < 250V$) is around 10, and for high voltage transistors is around 5, near $I_{C(sat)}$ as defined

in the data sheets.

The following empirical relation can be used to estimate gain at other current levels.

$$\beta @ I_C = [\beta @ I_{C(sat)}] \cdot \frac{I_C}{I_{C(sat)}}$$

3.4 Switching times

The total turn-off time t_{off} is the sum of two components (see figure 8):

- The storage time t_s . This is a “memory” effect, due to the storage of minority carriers in the base. (1s for $V_{CE0} = 100V$, 3s for $V_{CE0} = 400V$).
- The fall time t_f . The majority of switching losses are due to the fall time (but modern transistors using cellular technology have very small fall times).

Figure 7. Driving a bipolar transistor: a) Driving circuit b) Choosing the base drive current

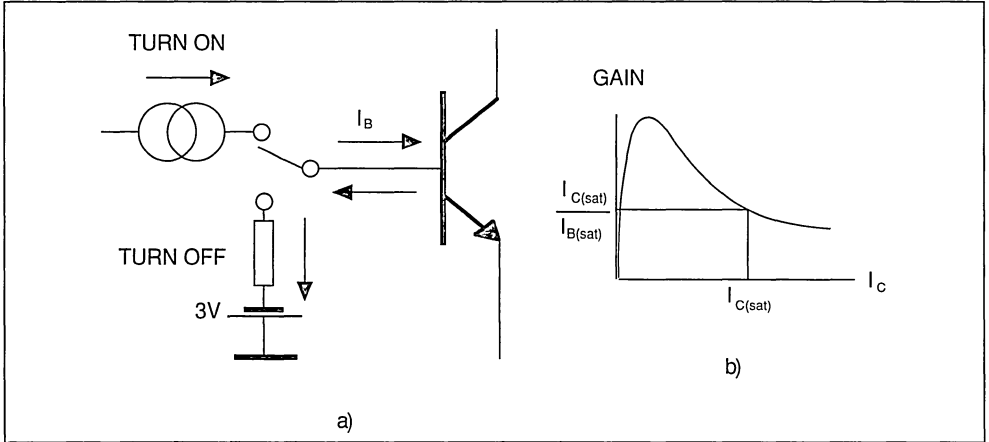
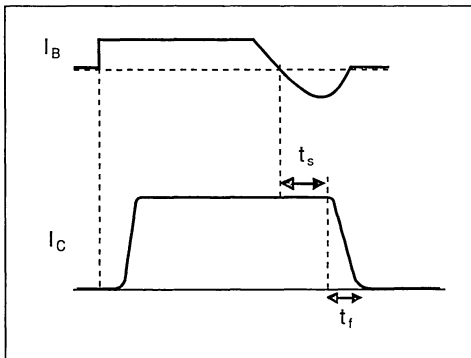


Figure 8. Bipolar transistor switching times



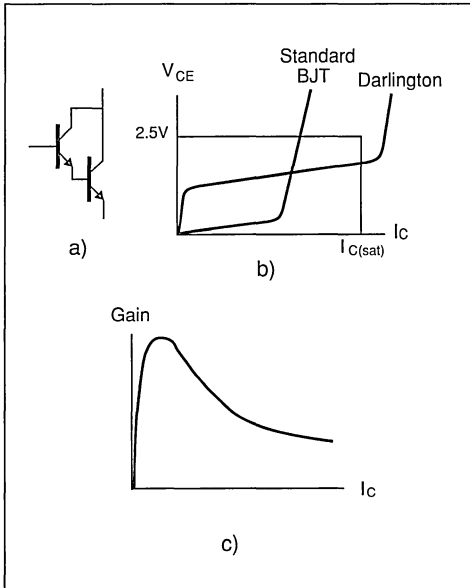
To ensure fast turn-off, it is necessary to force a negative current I_{B2} in the base to increase the rate of recombination of minority carriers.

3.5 The Darlington

This is a structure which behaves like two bipolar transistors connected, as shown in figure 9: the first acting as a driver, and the second as a power stage.

The Darlington offers higher gain than a conventional BJT, and the ability to operate at higher current density (because the gain of the power stage can be very high), but these advantages are offset by a

Figure 9. Darlington Transistor characteristics
 a) Equivalent structure
 b) Output characteristics
 c) Gain characteristics



higher voltage drop:

$$V_{CE(sat)} \text{ Darlington} = 0.8V + V_{CE(sat)} \text{ BJT}$$

and also the increased turn-off time - the power stage transistor can only begin to turn off after the driver has turned off.

4. THE THYRISTOR

“Thyristor” is a generic term for a semiconductor device having four or more layers. The two main members of the family are the Silicon Controlled Rectifier, or SCR (often simply called a thyristor) and the TRIAC (derived from TRIode for Alternating Current). Both share similar current and voltage characteristics. The structure and characteristics of the SCR are shown in figure 10.

The thyristor operates using positive feedback - once the device is turned on or “fired” by applying the current pulse to the gate, it continues to conduct until the current through it falls below a certain small fixed value, known as the holding current. This effect occurs because, as shown in figure 10b, the SCR

behaves like two bipolar transistors connected back to back, which once fired effectively provide their own base drive current.

4.1 Current

The maximum operating current is defined, like the power diode, by the rate at which the device is cooled. The thyristor can withstand very high surge currents (within the capabilities of the cooling arrangements).

4.2 Voltage

The blocking voltage can be very high - up to 5kV. Its voltage drop is around 0.8V at low current, rising to 1.2V at nominal current.

4.3 Drive requirements - see figure 11.

Because of the positive feedback, the thyristor needs only a very low current for a short time at turn-on (firing). In practice a small “holding current” is required to maintain the device in conduction. However it has the disadvantage that the device cannot be turned off by controlling the gate current - instead the anode current must be forced to zero, by forcing the anode-cathode voltage to zero. In switching or AC circuits this can be achieved using a resonant LC circuit connected in series or parallel.

4.4 Switching times

When the anode current is forced to zero, the thyristor turns off. However, it is necessary to wait for a time t_q (the turn-off time, like the fall time of a bipolar device) before the anode voltage is reapplied - otherwise the device will continue to conduct.

4.5 The TRIAC

The TRIAC is effectively two SCRs connected in anti-parallel, with a single gate - see figure 12. This device can conduct current in both directions (ie from A1 to A2 and from A2 to A1) and so can be used to control the flow of AC currents - the current through the device will fall below the holding current every half cycle, and at this point the device will turn off automatically unless it is refired. Hence for continuous conduction the device must be refired at twice the frequency of the current it is conducting.

As shown in figure 13, the TRIAC can operate in one of two ways:

- a) The device is fired on only for a certain proportion of AC half waves, or
- b) The firing of the device can be delayed such that

Figure 10. The SCR: a) Simplified structure b) Equivalent circuit c) Circuit symbol d) Current limits e) Voltage limits f) Switching Safe Operating Area

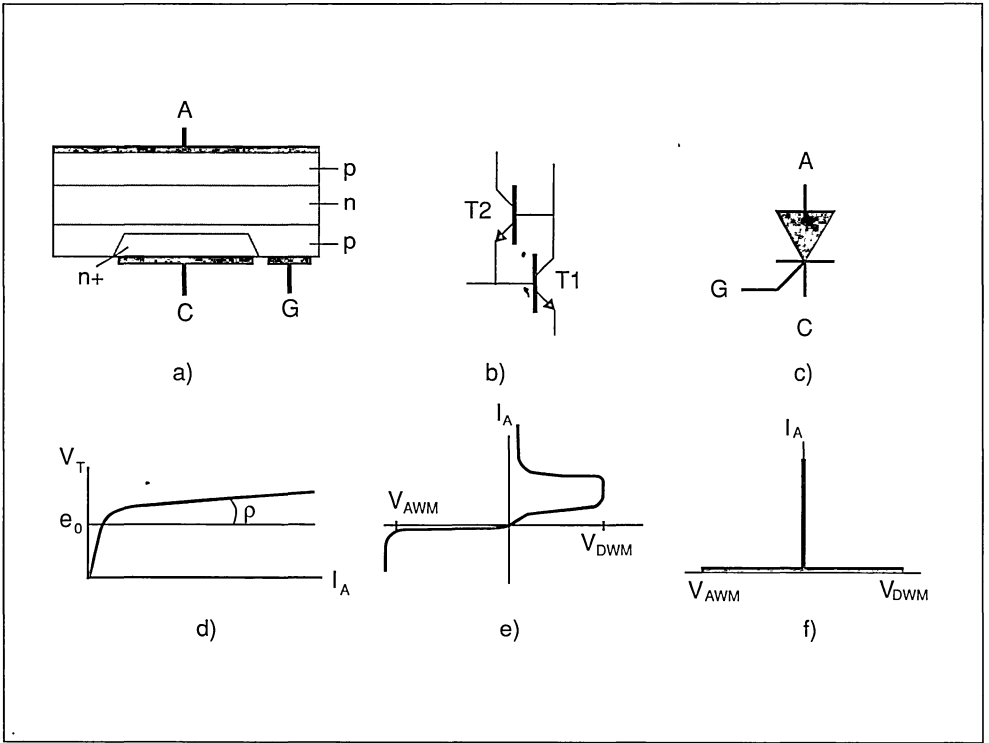


Figure 11. Thyristor drive requirements

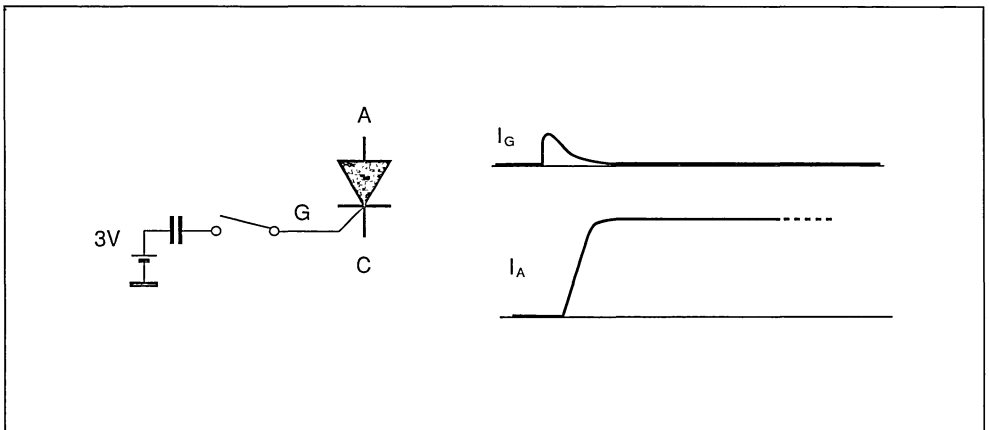


Figure 12. The TRIAC a) Simplified structure b) Circuit symbol c) Equivalent circuit

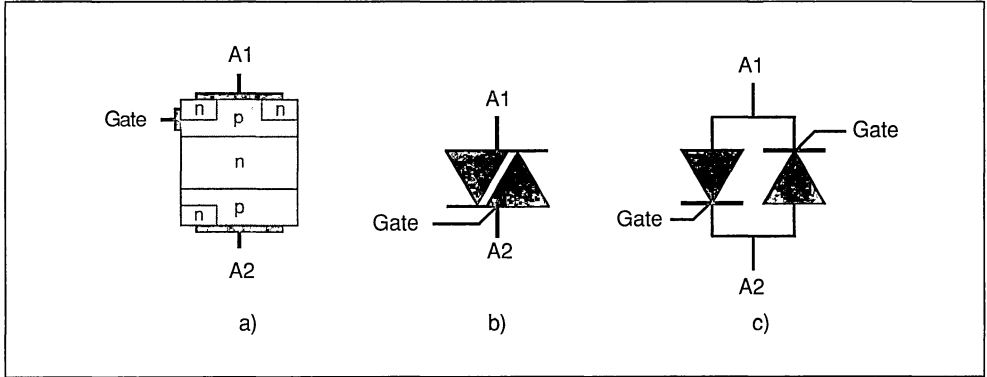
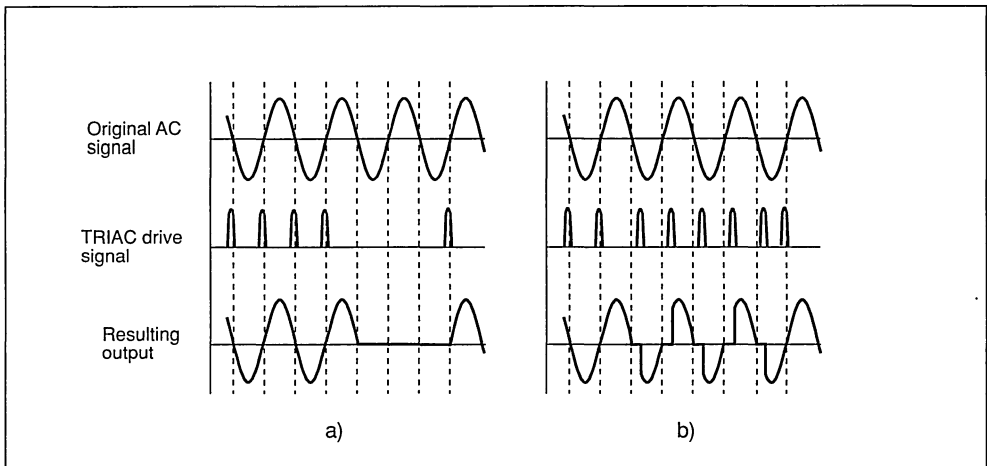


Figure 13. Driving a TRIAC: a) Using as an on-off switch b) Phase control



only a portion of each half wave is allowed through. This is known as phase control.

Operating in the first way, the device can be used as a simple on-off AC switch, while used in the second way, the device can be used to control AC power - for example as a speed control for an AC motor.

5 THE GTO see figure 14.

The GTO is another "positive feedback" component and is similar to the thyristor, but it has an

interdigitated structure, as shown in figure 14. Consequently it has similar characteristics to the thyristor, but it can be blocked like a transistor.

5.1 Voltage

GTOs can support up to around 4kV with a maximum rated current of 1kA. During turn-off the maximum voltage is defined by the SOA. The GTO has a poor S.O.A. when operating at high currents. Its voltage drop is marginally higher than that of the thyristor.

5.2 Drive requirements see figure 15.

Figure 14. The Gate Turn-Off Thyristor: a) Simplified structure b) Equivalent circuit c) Circuit symbol d) Current limits e) Voltage limits

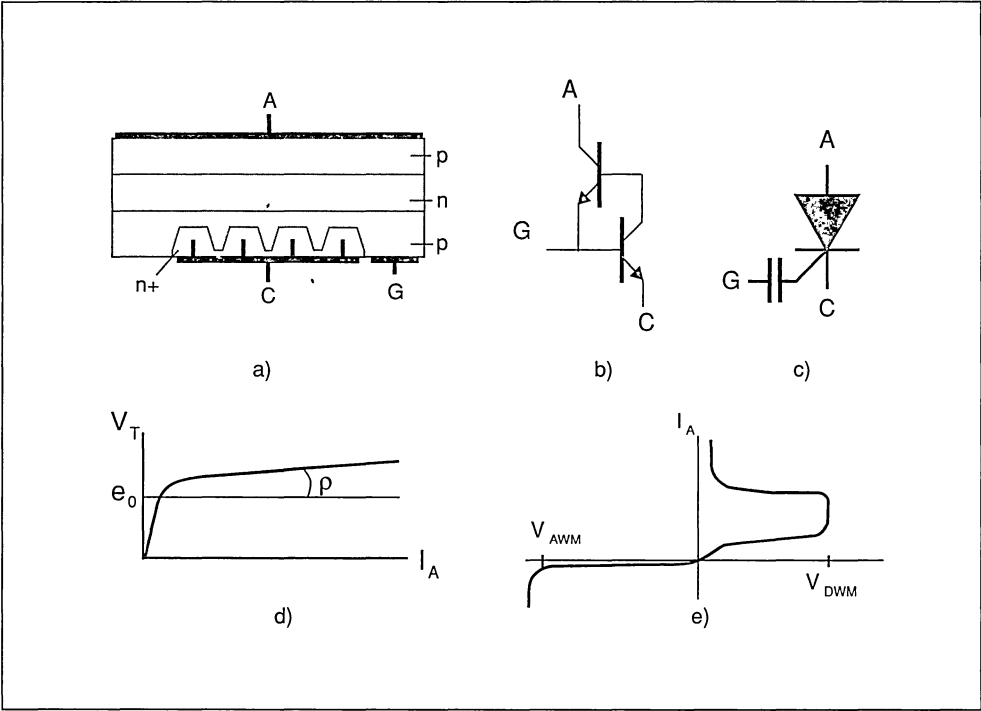
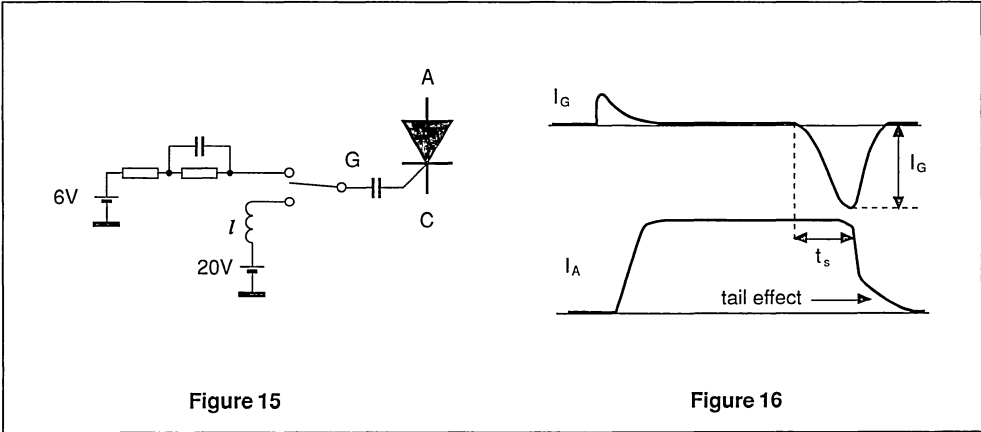


Figure 15. Driving a GTO
Figure 16. GTO switching times



APPLICATION NOTE

The GTO requires a very high negative gate current to turn-off quickly; its has a gain of only 3 which means it requires a sophisticated and expensive gate drive if it is to be run at any speed. This means that it is often impractical to use a charge extracting drive circuit, and so the device has a "tail effect" whereby the device still conducts while the minority carriers combine naturally.

5.3 Switching times see figure 16

Like the bipolar transistor the GTO has a storage time, and during the fall time its tail effect considerably increases the turn-off losses.

6 THE POWER MOSFET see figure 17.

This component uses only majority carriers in conduction, which accounts for its specific behaviour.

The majority carriers flow into the component due to the influence of gate voltage; the current cannot be limited by a "gain phenomenon". Hence the voltage drop depends only on the resistance of the silicon path between the drain and source, $R_{DS(ON)}$.

6.1 Current

The maximum operating current is defined, as for a diode, by the rate at which it is cooled. Its surge current capabilities are defined by the thermal time

constant of cooling arrangements (figure 18).

6.2 Voltage

Because the area of silicon used and hence $R_{DS(ON)}$ increase considerably with the maximum rated voltage, this voltage is currently limited to around 1000V.

The MOSFET has a large S.O.A, as it is able to sustain its maximum rated voltage during turn-off.

Present technology current ratings are governed by the following $R_{DS(ON)}$ (25°C) values for the relevant voltage ranges.

$R_{DS(ON)}$ @ 25°C (mW)	Max. rated voltage (V)
77	100
850	500
3500	1000

Figure 17. The Power MOSFET: a) Simplified structure b) Circuit symbol c) Equivalent circuit d) Output characteristics e) Forward breakdown characteristics f) Switching Safe Operating Area

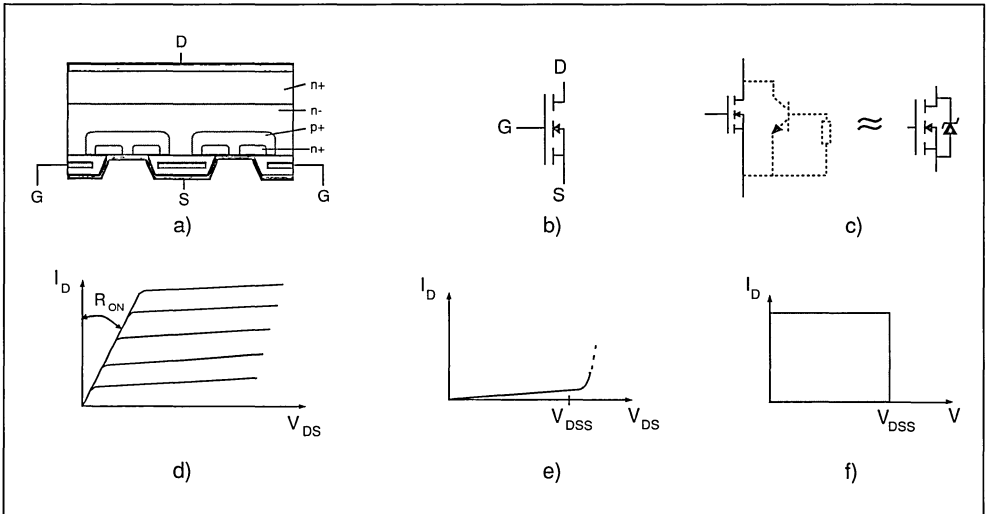
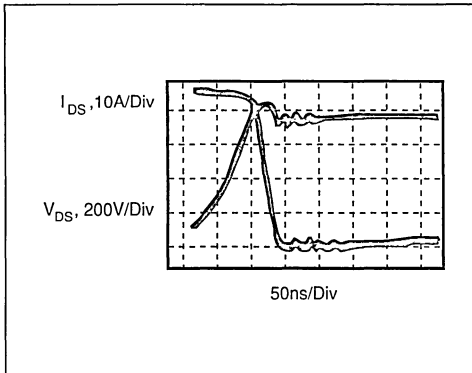


Figure 18. Turnoff with high current



It is frequently said that the MOSFET has a very high voltage drop, but this is not correct. The MOSFET voltage drop, $R_{DS(ON)} \cdot I$, can be very low at a low current density, though that would be compensated by the need for a large silicon surface area.

The $R_{DS(ON)}$ is (unfortunately) specified in manufacturers datasheets at 25°C. At a more realistic operating temperature:

$$R_{DS(ON)} @ 100^\circ\text{C} \approx 1.7 \times R_{DS(ON)} @ 25^\circ\text{C}$$

6.3 Drive requirements

During conduction the gate requires only a voltage (approximately 15V) without any significant energy consumption - see figure 19.

MOSFETs turn off very quickly when the gate-source voltage falls to zero. However, the presence of a capacitance between the gate and source means that to switch the device, charge must be supplied or removed to make the gate voltage rise or fall.

The designer must consider losses due to the charge/discharge of this capacitance at each turn-on/off.

6.4 Switching times

The MOSFET, a majority carrier device, has no storage time. This is very important for many applications. Fall time (depending on drive) can be very small, but for a rated voltage higher than 300V, it is approximately the same for both fast bipolar and MOSFET devices.

7 THE IGBT see figure 20.

The IGBT can be considered as a pseudo-Darlington with a MOSFET as driver and a bipolar transistor as the power stage.

7.1 Current

The maximum current is generally limited by cooling. It has over-current capability.

Figure 19: a) Driving a Power MOSFET

b) MOSFET switching waveforms

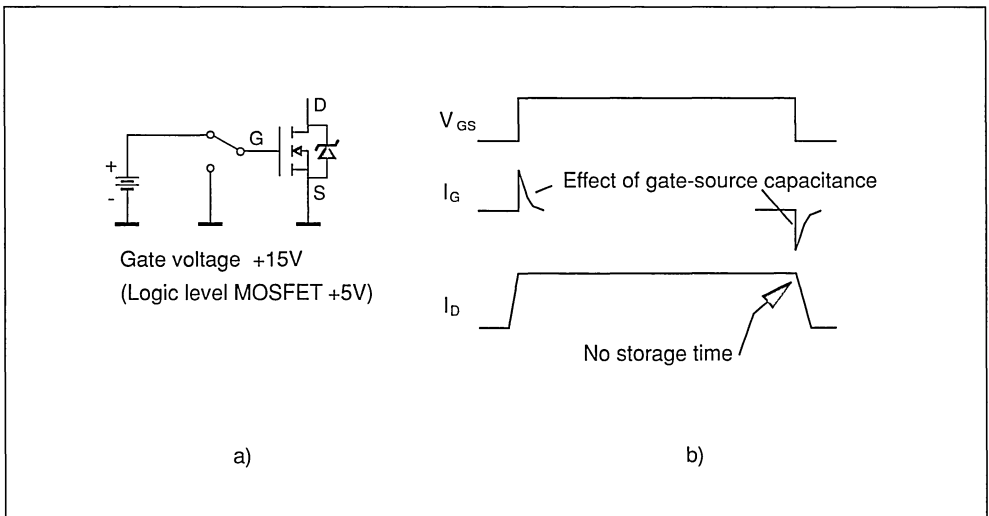
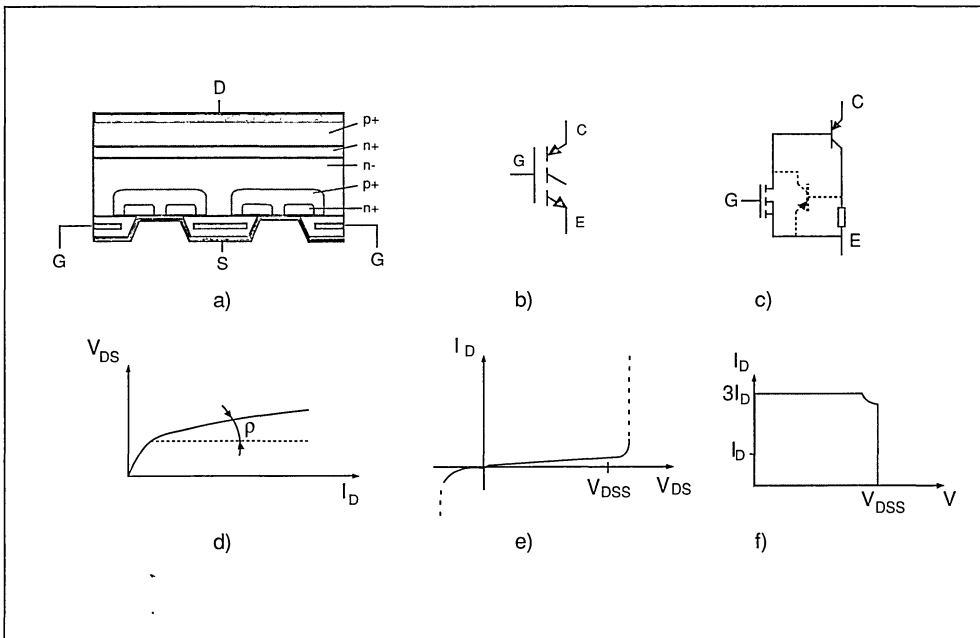


Figure 20. The IGBT: a) Simplified structure b) Circuit symbol c) Equivalent circuit

d) Output characteristics e) Forward breakdown characteristics f) Switching Safe Operating Area



7.2 Voltage

At present, the maximum rated voltage is 1.2kV. This limit is rapidly increasing towards 1800V and a maximum rated current of 500A. The SOA is approximately rectangular.

The voltage drop across the IGBT is relatively constant with respect to the current. This means that at high current levels, conduction losses are lower than those of a MOSFET, but at low current levels they are considerably higher. This causes a limit to the efficiency of IGBT circuits.

7.3 Drive requirements

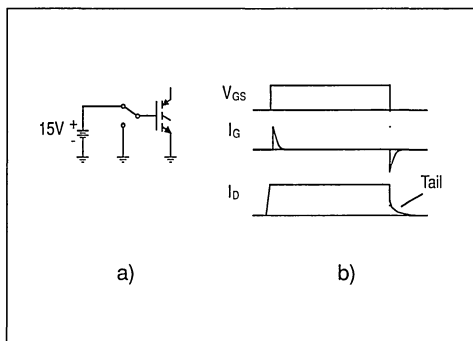
Similar to the MOSFET drive (figure 21).

7.4 Switching times

The MOSFET stage has practically no storage time, but the bipolar section causes a tail current like that in the GTO, where the device continues to conduct due to the presence of residual minority carriers in the base. As the base section of the device cannot

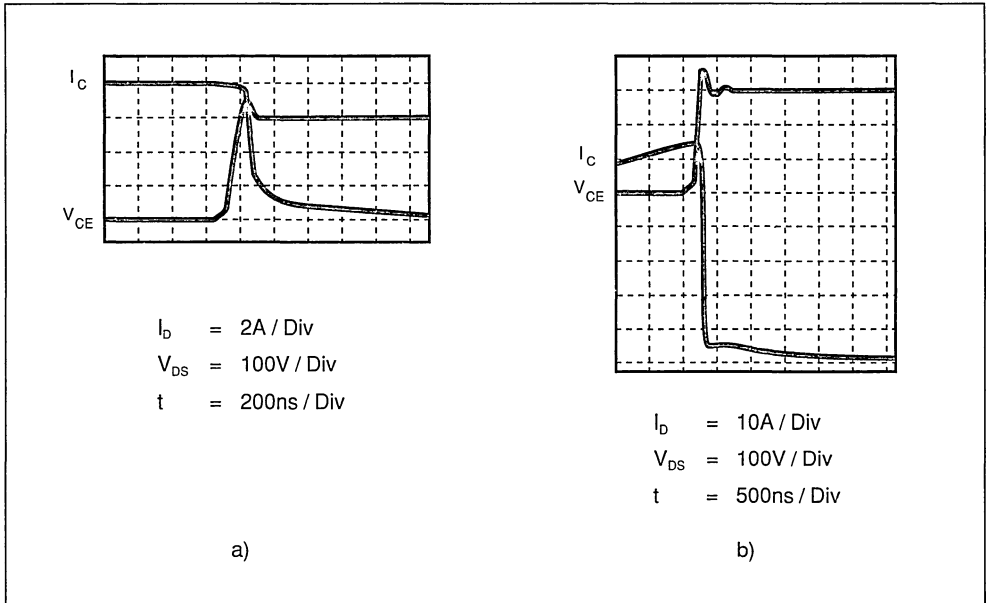
Figure 21. Driving an IGBT.

a) Driving circuit b) Switching waveforms



be accessed externally to remove these charges, this tail current persists until the carriers recombine naturally. This current causes switching losses, which increase with operating frequency.

Figure 22. IGBT Switch-off behaviour: a) Normal current
b) Very high surge current



8. LIMITS AND MAXIMUM RATINGS

The absolute maximum ratings are defined by the semiconductor manufacturer. These ratings must not be exceeded under any circumstances - to do so risks destroying the component. Examples of maximum ratings are the maximum junction temperature $T_{j(max)}$, the maximum current and the maximum blocking voltage.

It should be noted that the user cannot measure these parameters, as the device will probably be destroyed in the attempt. Characteristics which may be measured are for example the collector-emitter saturation voltage $V_{CE(sat)}$, and the switching times.

The manufacturer specifies a maximum and/or minimum value, depending on the parameter. In the design of circuits it is important to take into account the "worst case" value of the component, and to verify that the circuit operates correctly with the spread of all parameters.

9. CHOOSING THE RIGHT SEMICONDUCTOR

When selecting the type of semiconductor device to use in a particular application, the designer must

take into account a number of factors, such as:

- i) The cost of the device, and the cost constraints on the application.
- ii) The magnitude of voltages and currents encountered.
- iii) The drive requirements of the device - the need for a complex drive circuit can increase design time and the cost of the circuit.
- iv) The frequency at which the device will switch.

9.1 Typical applications of each type

9.1.1 Bipolar transistors

In general terms bipolar transistors compete with Power MOSFETs and IGBTs. Their main advantage over these types is the lower cost, particularly for high voltage devices, while their main disadvantages are the cost of the drive circuit and the limit on their switching speed imposed by the storage and fall times. The applications in which they are used are typically characterised by low to medium operating frequency and high voltage, where they result in a cheaper solution than the equivalent MOSFET or

IGBT. Examples are in electronic lamp ballasts, automotive ignition switches, and horizontal deflection circuits in TVs and monitors.

9.1.2 Power MOSFETs

The main advantages of Power MOSFETs are their minimal drive requirements and ability to operate at high frequencies. In power supplies, operation at high frequencies allows the size of circuit magnetics to be reduced, decreasing the circuit cost. In compact fluorescent lamp ballasts (such as those used in domestic environments) operating at high frequencies leads to smaller overall dimensions. The low currents and relatively low voltages in this application means that in this case the Power MOSFET leads to a cheaper solution than the power bipolar.

Power MOSFETs are also frequently used as power actuators (solid-state relays) in automotive circuits, because of the low voltages involved means that they are inexpensive, and types are available which can be driven directly from a microprocessor, which are increasingly being used to control automotive systems.

9.1.3 IGBTs

The main applications of IGBTs are in motor control and automotive ignition - again these are characterised by high voltages and relatively low operating frequencies. In these applications they compete with bipolars. Although the basic device is more expensive than a bipolar transistor, the minimal drive requirements can lead to a cheaper overall solution, particularly where there is a need to interface with a microprocessor. Its main disadvantage is the unavoidable losses caused by the tail current (which become more significant at high frequencies),

9.1.4 GTOs

GTOs are used in conditions of very high voltage and very high current, and low switching frequencies. An example of their use is in electric trains.

9.1.5 Thyristors

This component is very cheap, but its use is limited by the difficulty of turning it off. It can be used to control devices which can be fed with half-wave rectified AC current, for example DC motors (when it will turn off automatically every half cycle, like the TRIAC), and also to protect other devices, for example in power supplies.

9.1.6 TRIACs

TRIACs are unique in their ability to conduct and control current in both directions. They are the cheapest way of controlling AC currents, for example in AC motor speed controls or lamp dimmers.

11. CONCLUSION

"Power MOSFET has very high voltage drop"

"Bipolar ... an old technology"

"Epitaxial is better..."

This type of commercial jargon does not help the designer to produce optimal circuits. At the present time the designer has a choice between a lot of components. Which is the best solution? The answer is, there is no best solution - this is the field of technical design, not scientific research.

For some applications, for example 1MHz Switch Mode Power Supplies, only one solution (MOSFET) is possible. For most applications, there are always several solutions. The designer's job is to optimize the "switching function" after thorough analysis. Experience shows that the quality of this analysis, and the work done by the designer (drive, protection, etc.) play a bigger role in the total cost than the actual price of the component.

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POWER TRANSISTORS - DEVICES AND DATASHEETS

by V. Sukumar

ABSTRACT

The purpose of this paper is to give a general overview of how to read a transistor specification. We will discuss bipolar transistors, power MOSFETs and IGBTs, and introduce some intelligent power circuits that resemble discrete transistors. The emphasis is on switching transistors. Rules of thumb often followed in the selection of the right transistor are discussed. Some common pitfalls are mentioned and the reader is advised as to which parameters are more important.

1. INTRODUCTION

1.1 Using the specifications with care

The specifications for each power switching transistor today cover between three and ten pages. Some of these specifications are more important than others. In fact, from a user's point of view, there is a real danger in over-specifying a transistor. Broadly speaking a general power transistor specification gives information that will enable the user to use the component in a variety of applications. Parameters that are not critical in the particular circuit designed should not be specified; this will result in eliminating potentially usable and more economical components which will function perfectly well. A good understanding of the operation and the construction of transistors will teach the user which parameters are important.

This paper will concentrate only on commercial switching transistors used in the common emitter configuration. Transistors designed for military operations are typically specified and tested much more rigorously than their commercial equivalents.

1.2 Derating

In general, it is a good idea to derate some important parameters (i.e. allow an additional safety margin) in power switching transistors. The most important parameters to derate are the maximum voltage applied in the off-state, and the power dissipated. In general, heat is the most important reason for degradation of power semiconductors. Studies have

shown that even a 7°-10°C increase in junction temperature can result in halving the Mean-Time-Between-Failures (MTBF) of the device. Therefore in many applications, the switch is chosen such that under the worst case, steady-state operating conditions, the transistor junction temperature does not exceed about 125°C.

1.3 Testing

In general, most commercial transistors are only 100% tested in production at 25°C, and also only static characteristics of the devices are tested. The dynamic performance and certain other characteristics of the device at other temperatures are guaranteed by design. Unless otherwise specified, all graphs show only the typical characteristics of a typical sample of the device. The trends, not individual limits, of a particular sample are shown by these graphs.

1.4 Standardisation of information

For over twenty years, power semiconductor manufacturers have tried to tackle the tricky problems related to standardisation of specifications between one manufacturer and another. However, most power switching transistor datasheets have a first page discussing absolute maximum characteristics that should never be exceeded. The Absolute Maximum system currently in use was defined by the American organisation JEDEC and accepted by various organisations such as EIA and NEMA. Similar organisations in Europe and Japan also help in similar efforts at standardisation. However, it is unrealistic to expect complete standardisation. The user has come to expect that no two manufacturers' specifications are exactly alike. Some specifications that one manufacturer may choose to emphasise find only a passing mention in another transistor datasheet.

2. POWER TRANSISTOR PACKAGES

The package style and size often important in the circuit performance of the power transistor. The thermal performance of the transistor depends on

the package chosen. High temperature performance of different types of transistors - MOSFETs, IGBTs or bipolar transistors - are quite different. Generally speaking, choose a transistor whose die size is between 40-100% of the maximum die size that can be accommodated in the package with good reliability. Too small a die size for a given package will lead to an unnecessarily large circuit board and circuit parasitics. A smaller package may also have a lower cost.

Certain power transistor module packages - for example the TO-240 - result in high parasitic inductances and capacitances which affect the device performance. A cross-section of the TO-240 package reveals that about 60% of the package consists of air, and the needless increase in height can result in unacceptable levels of circuit parasitics in high frequency applications. Other packages, such as the ISOWATT series of isolated packages, are to be used only if the application demands electrical isolation of the device from heatsinks. Otherwise we run the risk of unnecessarily increasing the junction temperature and needlessly compromising device reliability. The mounting methods of power transistors, including the maximum values of mechanical parameters such as screw torque or pressure exerted by mounting clip, need careful attention to avoid damage to the device.

In certain applications, the transient thermal impedance (that is the ability of the device to absorb short pulses of energy) is also important. This characteristic is dependent on the package and the die size. It is explained in detail in reference [5].

3. POWER BIPOLAR TRANSISTORS

Power bipolar transistors represent the most mature of the three kinds of discrete transistors discussed here. They have been in common use for over thirty years, but these devices and their manufacturing technologies are still evolving. There are a number of different technologies used in the manufacture of power bipolar transistors. Each technology has its own advantages and disadvantages, and has found its niches in certain applications.

3.1 General Characteristics

It should be remembered that power bipolar transistors resemble rectifier diodes in their on state. Their on-state voltage does not increase as significantly as unipolar devices when the current carried by them is doubled. They switch on and off

much slower than similar MOSFETs, and the drive currents necessary to keep the device in the on state and to switch the device off are quite significant. Most Darlington transistors are too slow and have too high an on-state voltage to be considered for most switching transistor applications. However, today it is possible to use fast Darlington transistors for switching applications in the tens of kilohertz in colour television horizontal deflection.

3.2 Bipolar Transistor types

3.2.1 General Purpose Transistors

Epitaxial base transistors are some of the most common general purpose transistors in use today. They are used mainly in low voltage applications (below say 100 to 200V) where low cost is most important. The popular "TIP" series of power transistors are manufactured using this technology. Single epitaxial layer planar transistors are general purpose devices used in low voltage applications (up to 100 to 200 V). These transistors however are very fast compared to epitaxial base transistors with "f_T" values of around 40Mhz, against about 1MHz for epi-base devices. Their on-state voltage is usually lower than equivalent epitaxial base transistors. Examples of these transistors are the well-known "D44" and "D45" series of transistor.

3.2.2 Switching transistors

The above two technologies are known as general purpose transistors rather than switching transistors. Higher voltage transistors, which have V_{CEO} values up to say 1000V use multiple epitaxial planar or mesa technologies. Examples of multi-epitaxial mesa transistor the BUV48, BUV98 etc.

In the early 1980s, multi-epitaxial mesa transistors with "hollow" emitters became popular. These devices, with part numbers such as the SGSF or MJH16 series are significantly faster than their non-"Hollow Emitter" counterparts since their hollow emitter designs decreased current crowding and this resulted in faster switching. One small disadvantage of these faster transistors was that they were less rugged during the turn off time.

3.3 Important Parameters

3.3.1 Breakdown voltages: V_{(BR)CEO}, V_{(BR)CES}*

These values represent the maximum voltage which the device can withstand across its collector and emitter terminals when turned off, specified with the base terminal open, and shorted to the emitter

respectively. If this value is exceeded, the transistor will go into breakdown and will be destroyed.

These breakdown voltages of course do not relate very well to the voltages actually experienced during normal switching. If the voltage at turn-off plus the safety margin exceeds the $V_{(BR)CES}$ of the device, then the device must simply not be used for the application.

In most applications the power transistor is never used with its base terminal opened, hence the $V_{(BR)CES}$ is the value used to choose the transistor. The $V_{(BR)CEO}$, generally around 60% of the $V_{(BR)CES}$, becomes important when the both currents and voltages are present in the device simultaneously, for example when switching an inductive load. This topic is discussed in more depth in the later section on RBSOA.

3.3.2 $I_{C(max)}$ Maximum Collector Current

This specifies the maximum current that should be allowed into the collector terminal. However, as a general rule the maximum current that the device experiences in normal operation should depend not only on the maximum current but also the current at turn off. Most switching transistors are used with inductive or resistive loads where the current at turn off is the maximum current through the transistor. The current at turn off should be close to the level used by the manufacturer to test the switching times of the transistor, as shown in the "Conditions" column of the specifications of the switching times of the device. This allows the dynamic performance of the device to be predicted with some confidence.

3.3.3 Reverse Bias Safe Operating Area.

During inductive switching, it is possible that collector current and collector-emitter voltage can exist at the same time as the transistor turns off. The simultaneous high values of current and voltage is stressful to the transistor and can often result in device destruction. The transistor manufacturer often provides a diagram of the V_{CE} - I_C locus below which the transistor operation is guaranteed to be non-destructive - an example is shown in figure 1. This curve is called the RBSOA. Values of the I_C - V_{CE} locus straying outside the specified RBSOA curve may lead to the transistor reverse bias second breakdown, a destructive phenomenon. The mechanisms of reverse bias second breakdown phenomenon of the bipolar transistor is very complex. However, it simply must be remembered that

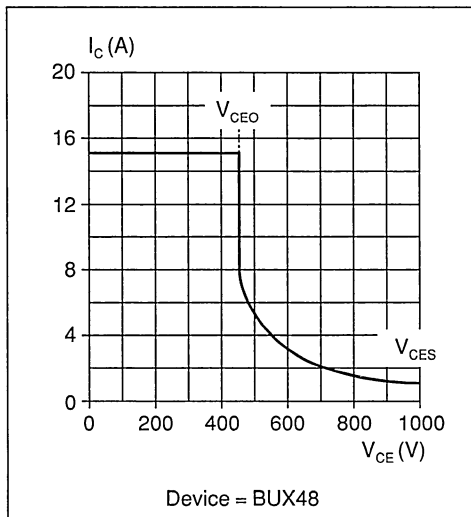
excessive turn-off base drive current extraction could lead to failures that are difficult to explain.

Where possible, the application circuit should switch the transistor on and off with base drive values similar to those mentioned during the switching times in the electrical characteristics section of the datasheet. Turn-off snubber circuits delay the rise of voltage across the transistor and can help ensure that the RBSOA of the transistor is not exceeded.

Usually, switching transistors can be turned with the maximum possible extraction base currents between $V_{(BR)CEO}$ and $I_{C(max)}$. For applications such as switching power supplies or halogen lamp ballasts, how high the current switched between the $V_{(BR)CEO}$ and $V_{(BR)CES}$ of the transistor is of primary importance.

The silicon die design of the modern high voltage switching transistor involves a certain compromise between the switching speed and the dc transistor gain. High frequency transistors often have a minimum dc gain (hFE) of only between 4 and 8 over the operating temperature range. In these cases, we have to pay special attention to the on-state and turn off base currents. Too low a base current or too slow a turn off base drive will increase the losses of the transistor significantly. Too large an on-state base current can result in driving the transistor into hard saturation which will then require high turn off

Figure 1. The RBSOA of a typical bipolar transistor



base currents. Excessive turn off base drive can result in exceeding RBSOA of the transistor and could cause destruction.

Base drive currents - On-state Current I_{b1} and Extraction Base Current I_{b2}

Poor base drive design is responsible more than any other single factor for destruction of power bipolar transistors. Not only should the maximum values of base drives in the forward (into the base of the transistor) and reverse (out of the base of the transistor) be optimised, but also, as far as possible the oversaturation of the transistor during the on time and driving the transistor too fast during turn off of the transistor should be avoided.

The on-state base current I_{b1} should ideally resemble the collector current waveform. In many inductive switching applications, the base current waveforms are roughly rectangular whereas the collector current is roughly triangular. The transistor is usually forced into hard saturation in the beginning of the drive waveform. Proportional base drive circuits and Baker clamps may be used to prevent the excess base current from sending the transistor into hard saturation.

The turn off base current, I_{b2} should be high enough to prevent excessive turn off times and power losses. It should be low enough to keep the locus of the switching collector current and V_{CE} within the RBSOA specified in the datasheet. The values of the base currents mentioned in the "switching times" section of the datasheet serve as a rough guide in choosing the values of I_{b1} and I_{b2} .

3.3.4 Switching times

The switching times of a bipolar transistor consist of the delay time and rise time at turn-on, and the storage time and fall time at turn-off; see figure 2.

In general, the losses due to switching times are most significant at turn-off. The storage time is generally longer than the fall time, but the voltage across the device is smaller and so losses in both phases are of the same order.

An optimised base drive will reduce the storage and fall times, and hence reduce losses.

3.3.5 High Temperature Performance and thermal runaway.

BJT turn-off times and h_{FE} increase with temperature. This means that as temperatures increase, the

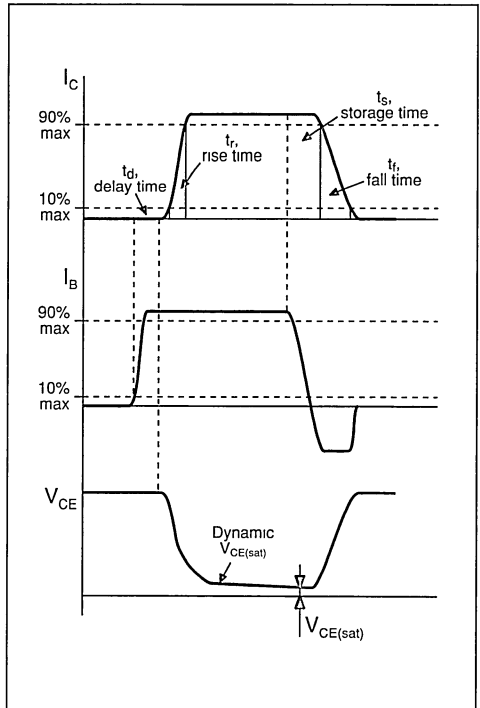
switching losses also increase, which will in turn increase the junction temperature of the device (if the heatsinks etc. are insufficient). This positive feedback effect is called thermal runaway, and can easily lead to the destruction of the device if care is not taken with thermal management.

This effect also makes BJT devices difficult to parallel, as the device with the largest losses will tend to heat up more, causing it to "hog" the current (i.e. conduct a disproportionately large amount) and go into thermal runaway.

3.3.6 Polarity - NPN or PNP.

Most applications which use switching transistors - power supplies, lamp ballasts, horizontal deflection and some motor drives - use faster switching NPN bipolar transistors or N-channel MOSFETs. PNP transistors (and in the case of power MOSFETs, p-channel devices), are used in applications such as low voltage motor drives only when their simplified drive design is preferred to device performance and reduced power losses.

Figure 2. Bipolar Transistor switching times



3.3.7 Second Breakdown Current with base forward biased, $I_{s/b}$ and Forward Biased Safe Operating Area FBSOA

These parameters are often used in linear power supplies where external transistors especially PNP transistors are used to increase the power output of the linear series regulator.

3.4 Some rarely specified parameters

Certain parameters which are not often specified could be very useful in certain types of applications or designs but are not needed in others. The challenge of the transistor manufacturer is to condense as much information as relevant in a wide variety of applications all within a few pages. Invariably some items that could be useful in some applications do get left out. Two examples of parameters are:

3.4.1 Dynamic Saturation.

In very fast switching applications or applications with short on times, the on voltage of the transistor may not reach the steady-state $V_{CE(sat)}$ value. For these applications, a dynamic saturation voltage better reflects the real application conditions and allows a more accurate calculation of the power losses.

3.4.2 Very low current transistor gain - especially at low temperatures

Some applications such as lamp ballasts and self-oscillating power supplies depend on the gain of the transistor at very low current levels for circuit start up. Here, the gain specified at low current levels such as around 10mA or even less, is very important. As this is temperature dependent, the worst case condition is start up at the minimum ambient temperature.

4. POWER MOSFETS

Generally speaking, power MOSFETs are more similar from one manufacturer to another than power bipolar transistors. However it is increasingly seen that in high frequency applications, the performances can vary quite significantly even though the datasheet values are quite similar.

4.1 Important Parameters

4.1.1 $V_{(BR)DSS}$ Drain-Source Breakdown Voltage

This value indicates the maximum voltage which can be withstood by the drain and source terminals

of the MOSFET. If this value is exceeded, the device will break down and begin to conduct. The effect can be thought of as similar to the reverse breakdown of the intrinsic anti-parallel diode. It is specified with the gate and source terminals shorted together.

This parameter represents the worst case sustained voltage that the MOSFET should experience in normal operation. However, exceeding this value is not instantly destructive. It is possible that the power MOSFET can withstand pulses of low energy at voltages above this published breakdown level. This phenomenon is called Avalanche breakdown. During this time, the voltage across the drain-source terminals of the MOSFET is clamped (in a similar way to the clamping of a Zener diode), but the current through the device and hence also its power dissipation start to increase. For this reason the power MOSFET is often shown schematically as having an anti-parallel diode, even though it is not a true Zener.

Having said this however, it is always best to treat the avalanche energy breakdown withstand capability of the MOSFET as an extra level of safety margin that we give to the design. During normal operation, the breakdown voltage of the MOSFET is not to be exceeded.

However too high a safety margin in $V_{(BR)DSS}$ leads to other problems. The on resistance of MOSFETs rise steeply as the breakdown voltage increases. For the same die size, doubling the breakdown voltage results in a five fold increase in on-resistance. The challenge of the circuit designer is choosing the MOSFET with the optimum safety margin. $V_{(BR)DSS}$ is essentially independent of temperature though the worst case (minimum) for the circuit designer is at the lowest operating temperature.

4.1.2 $R_{DS(on)}$ Static Drain-Source On-Resistance

The on-resistance, and not the current carrying capacity, is the fundamental factor in the design and specification of power MOSFETs. In fact, the continuous current rating I_D is normally a derived value that supposes ideal conditions such as infinite heatsinks.

The on-resistance is highly temperature dependent. Between room temperature (25°C) and the maximum operating temperatures (150 or 175°C), the on-resistance often more than doubles. The variation in on-resistance at elevated temperatures is somewhat higher for higher voltage transistors. The positive

temperature coefficient of resistance makes the MOSFET an easier device to parallel than a bipolar transistor.

4.1.2 $V_{GS(th)}$ and $V_{GS(on)}$

$V_{GS(th)}$ is the value of the gate-source voltage required to make the device start to conduct. The drain current at which this parameter is measured is usually small - for example 1mA .

The value of the gate voltage which should be used to drive the device in normal operation, $V_{GS(on)}$, is not specified explicitly in the datasheet. A value should be chosen which is around that given in the "CONDITIONS" column of the $R_{DS(on)}$ specification.

In terms of $V_{GS(on)}$ requirements, power MOSFETs fall into two basic categories: standard and logic-level. Standard power MOSFETs are meant to be driven on with a positive voltage of +10V. Logic-level devices can be driven with a voltage of +5V, compatible with the TTL logic level voltage. Thanks to a need for automotive and digitally driven applications, these power MOSFETs are becoming increasingly popular, especially at lower voltages (below about 100V $V_{(BR)DSS}$). These lower voltage components have a thinner gate oxide than the normal threshold equivalents.

4.1.3 $V_{GS(MAX)}$

Exceeding this value when driving the device can lead to punch-through of the gate oxide, and destruction of the device.

Currently, the specified maximum values of gate-source voltages are generally around +/-20V for normal (10V) MOSFETs and +/-15V for logic level (5V) MOSFETs. In reality modern MOSFETs have a considerably higher $V_{GS\ max}$. than that stated on datasheets, and as control of the thickness and integrity of the gate oxide in the manufacturing process improves, this is increasing. For high voltage MOSFETs (400V-1000V) a value of +/-30V is guaranteed when state-of-the-art manufacturing processes are used. However, it is best to treat this as additional insurance against spikes in the drive circuit and not drive the MOSFET on at voltages far higher than the 10V suggested in the datasheet.

Negative voltages are sometimes used to ensure that MOSFETs do not accidentally turn on in noisy environments.

4.2 Other parameters

The next few characteristics of mosfets are less

important in most applications than the first three mentioned above.

4.2.1 Switching Times [$t_{d(off)}$, t_r , $t_{d(on)}$, t_f]

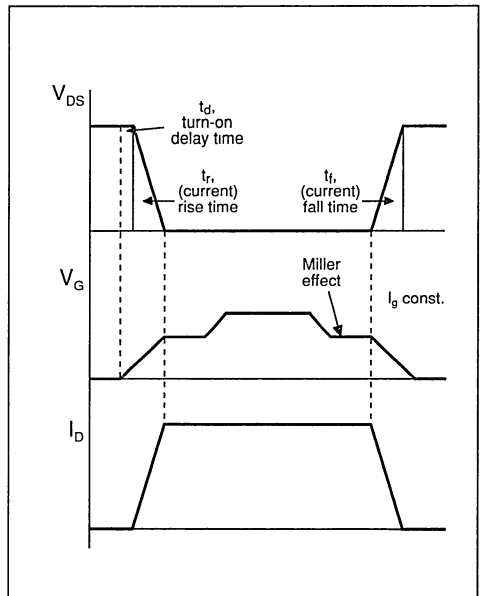
The turn on delay , rise time, turn-off delay and the fall time of the MOSFET comprise the switching times of the MOSFET - see figure 3. In general, MOSFET switching times do not mean much to the user. Careful design may result in a faster switching MOSFET but, since the switching times are in the order of tens of nanoseconds, the differences are small. Furthermore, faster switching mosfets may result in other system problems such as noise and EMI.

4.2.2 Total Gate Charge, Q_g and Input Capacitance, C_{iss}

Q_g represents the amount of charge required to turn the device fully on; that is to charge the input capacitance to $V_{GS(on)}$. It allows the currents and switching times at turn-on and turn-off to be deduced.

The input capacitance of a MOSFET, C_{iss} is the sum of two components - C_{gs} and C_{gd} . To a first approximation, C_{gs} does not vary whereas C_{gd} varies quite significantly with the applied voltage with the highest value of C_{gd} (and hence C_{iss}) being at low

Figure 3. Power MOSFET switching times



impressed gate-source voltage. Because of the widely varying nature of C_{iss} and since it is of limited value to the user, the parameter Q_g , introduced relatively recently, is used to describe the charge necessary to turn the device on. However C_{iss} is still used on datasheets to give a rough estimate of the peak currents necessary to turn on the device in a certain time period.

4.2.3 Other Parasitic Capacitances : Output Capacitance, C_{oss} and Reverse Capacitance, C_{rss}

The Output capacitance and the reverse or "Miller" capacitance of the MOSFET are represented by the symbols " C_{oss} " and " C_{rss} " respectively. These parameters are not very important in circuit design. C_{oss} and C_{rss} are functions of die size and to a lesser extent, breakdown voltage. It is interesting to note that there is a certain equivalent output capacitance, C_{oss} , for MOSFETs. This capacitance is charged at every MOSFET turn off and discharged through the MOSFET at turn on. This means that in certain high frequency switching circuits, where frequencies run into hundreds of kilohertz, a smaller die with lower total gate charge and lower parasitic capacitances could result in not only a lower device die size (and hence cost) but also lower overall losses (since lower switching losses will be more than adequate to offset any higher on-state losses).

5. IGBTs

Insulated Gate Bipolar Transistors are relatively new devices that have the potential to replace bipolar transistors in many low frequency applications. The notable improvements in IGBTs have led to their replacing bipolar Darlington transistors in numerous medium and high power high voltage applications.

The important advantages of the IGBTs are the easy of drive thanks to its (MOSFET like) MOS gate and low on-state drop thanks to bipolar, diode-like conduction during the on state. The disadvantages are the relatively slow turn off rate which cannot be influenced significantly by turn-off circuit design (because of the MOS gate!) and the possibility under certain extreme conditions to "latch". Latching is the accidental turn on of a suppressed parasitic transistor which results in a thyristor like condition, loss of gate control and usually device destruction.

5.1 Important parameters

5.1.1 Breakdown Voltage $V_{(BR)CE}$

This specification is not to be exceeded under any

condition. Unlike avalanche rated MOSFETs, we do not have much to gain and we have much to lose by choosing an IGBT with a breakdown voltage very close to the highest impressed instantaneous voltage. The on state voltage of the IGBT increases when the breakdown voltage of the IGBT is increased, but the rate of increase is much less than that of similar parameters in a power MOSFET.

5.1.2 Switching Times and Switching Losses.

Below about 300 or 400V, the power MOSFET is a more suitable power device in most applications. Between 400V and 1200V, the IGBT is more likely to be used in low frequency applications such as automotive ignition (about 100Hz) and industrial motor control (2 to 25kHz). Ultrafast IGBTs which can switch at 50 or even 100kHz are possible but currently the economies of scale favour the MOSFET over the IGBT in most high-frequency applications. IGBTs can be used in resonant applications.

A major disadvantage of IGBTs results from being unable to extract excess charge from the n- epi and p region of the IGBT at turn-off. This results in the turn-off collector current exhibiting a non-linear tail. In order to compute the turn-off losses, this can be divided into two piece-wise linear regions: t_{f1} , where the collector current falls from 100% to 20% of its maximum value; and t_{f2} , where the collector current falls from 20% to 0%. The second portion of the tail, t_{f2} can be a very dissipative region because of the high voltage across the part at the same time when there is current flowing through the device.

The structure of IGBT gives the device manufacturers the ability to optimize the performance for a given breakdown voltage and switching frequency, or in other words, manufacture IGBTs targeted to a certain application.

5.1.3 On-State Collector-Emitter Voltage, $V_{CE(on)}$

The voltage drop across the collector-emitter of the IGBT when it is full on is identified by the symbol $V_{CE(on)}$. The maximum value for the on-state voltage is very important for low frequency applications such as solid state relays and automotive ignition. As discussed in the above paragraph, very fast IGBTs can have significantly (three or four times) higher on-voltage compared to IGBTs optimised for low frequency operations.

In high voltage applications, above about six hundred volts, the on-state voltage of the IGBT is very significantly smaller than that of an equivalent

MOSFET. The IGBTs are therefore most popular in high voltage, relatively low frequency applications.

5.1.4 On-State Gate-Emitter Voltage, $V_{GE(on)}$

The positive voltage placed on the gate to keep the IGBT in the on-state is called its on-state Gate-Emitter Voltage, $V_{GE(on)}$. This gate voltage value specified in IGBT datasheets is usually +15V for IGBTs (against 10V for MOSFETs). Here too, reliability studies have shown that values of the gate-emitter voltage much higher than necessary are not recommended. The absolute maximum value specified for the gate source voltage is usually $\pm 20V$ or $\pm 25V$. In the off-state, since many motor drive IGBTs operate in noisy environments, a negative voltage is sometimes used. Usually, the expense of a negative power supply and a more complicated drive scheme is to be weighed against the possibility of destruction due to accidental turn on and if absolutely necessary, negative gate-emitter voltages are used to keep the device in the off state. In rare cases the on-state gate voltage of an IGBT drive circuit is deliberately lowered to increase short circuit immunity at the expense of on state losses.

5.1.5 Energy Dissipated Per Turn Off Cycle, W_{off}

Since the turn off voltage exhibits a tail, this specification is especially popular for slow, low $V_{CE(sat)}$ IGBTs. This measure, multiplied by the switching frequency forms the bulk of the switching losses. Usually speaking, the turn on losses of the IGBT are far less than the turn off losses.

5.1.6 $I_{C(max)}$ Collector Current at 100°C

This shows the maximum continuous current that the device must see during normal operation. IGBTs in general cannot handle "peaky" currents (High peak, low RMS currents) the way MOSFETs can because of this tendency to latch. Therefore it is a fairly common practice to derate the peak instantaneous current IGBT to the maximum specified current level at 100°C.

5.2 Special IGBTs

5.2.1 Logic Level IGBTs

These devices require a drive voltage lower than standard IGBTs. They are ideal for high voltage solenoid/plunger applications, automotive ignition applications where low battery voltage operation (7V) is possible. The technology used to create logic level IGBTs is similar to that of power MOSFETs.

5.2.2 Short Circuit Proof IGBTs

By decreasing the transconductance or g_{FS} of the IGBT, the device manufacturer can make the device withstand overload currents until the a short circuit detect circuit can be triggered. Normally the device designer attempts to have as high a device transconductance as possible. In the case of short-circuit proof IGBTs, however, the transconductance is deliberately lowered. This results in a higher on state voltage but the ability of the MOSFET to withstand a high short circuit for a few milliseconds till a short circuit detect and turn-off circuit comes into operation.

Similarly, as described in section 5.1.5 above, it is possible to lower the on-state drive voltage to increase the overload current withstand.

6. "SMART" TRANSISTORS

A new trend in the transistor industry is the recent appearance of a variety of self protecting, three pin intelligent power ICs that are pin compatible with and functionally equivalent to power transistors. The added advantages of these transistors is the additional features possible thanks to monolithically integrating these protection, status and alarm functions on to the same piece of silicon. These sophisticated power intelligent circuits all have device specifications characteristic to the intelligent power technology used. While some of these transistors will find use on diverse applications, most of the smart transistors are designed specifically for one main application area. A number of three pin intelligent "transistors" are used today in the automotive industry.

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**SERIES CONNECTION OF MOSFET,
BIPOLAR AND IGBT DEVICES**

by R. Letor

ABSTRACT.

Fast power switches with voltage ratings much higher than those of single fast switching devices can be made by connecting Bipolar Transistors, Power MOSFET and IGBTs in series.

Problems associated with device characteristics such as balanced switching, steady state and thermal behaviour must be carefully considered when designing with such switches.

This note deals with the series connection behaviour analyzing both static and dynamic characteristics of the devices.

Two philosophies for driving circuits are

described and design criteria are given for obtaining optimum performance.

1.0 INTRODUCTION.

Advantages of BIPOLAR TRANSISTORS, Power MOSFETs and IGBTs reside in the simplicity of the driving circuit and on their high switching speed. But, applications of these devices are limited to maximum reverse voltage, generally up to 1000V - 1500V. Higher voltage ratings would make these devices unattractive due to problems related to their structure.

For example, theoretical $R_{DS(on)}$ of a Power MOSFET increases with the square of the voltage breakdown ($R_{DS(on)} = 5.93 \text{ E-9} \cdot (V_{DSMAX})^{2.5}$). Figure 1 showing the real behaviour of SGS-THOMSON Power MOSFETs versus breakdown voltage, demonstrates that the current rating of three 800V Power MOSFETs in series will be higher than a single 2000V Power MOSFET.

Moreover, the design of IGBTs and BIPOLAR transistors with higher voltage ratings can be difficult due to the rise time of the switching waveform shown in figure 2.

Therefore, in some applications like battery chargers, inverters for medium voltage lines such as railway traction using frequencies up to 20kHz or high resolution TV deflection with operating frequencies of up to 64kHz, the series connection of fast switching power devices can be an interesting solution.

When connecting switching devices in series, voltage sharing during the off-state, and during transient must be carefully considered.

In fact the spread of leakage current creates unequal reverse voltage sharing. Delay between commutation due to switching time

differences causes transient overvoltage. If the parameters are temperature dependent, junction temperature difference must also be considered.

2.0 STEADY STATE VOLTAGE SHARING.

2.1 HOW TO BALANCE STEADY STATE VOLTAGE SHARING.

Figure 4 illustrates how the difference in blocking voltage characteristics results in unequal state voltage and how a resistor connected in parallel to each device (figure 3) equalizes the voltage sharing.

Equations 1 and 2 can be derived from the graphical information in figure 4 and to evaluate the value of R that reduces the difference of blocking voltage to a fixed value ΔV_R with a fixed V_M .

$$\Delta V_{R12} = V_{R1} - V_{R2} = R_1 \cdot \Delta I_{R12} \quad (1)$$

$$V_M = V_{R1} + V_{R2} + \dots + V_{Rn} \quad (2)$$

Equation (1) assumes that the leakage current is constant, this approximation is errs on the side of caution and introduces a safety margin.

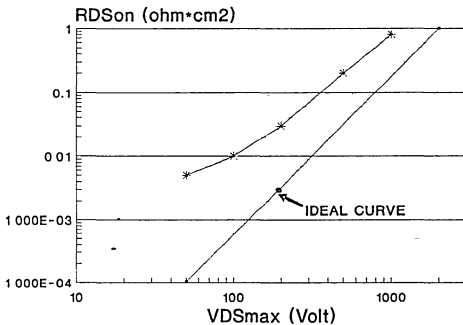


Fig. 1. Ideal and real behaviour of $R_{DS(on)}$ vs breakdown voltage.

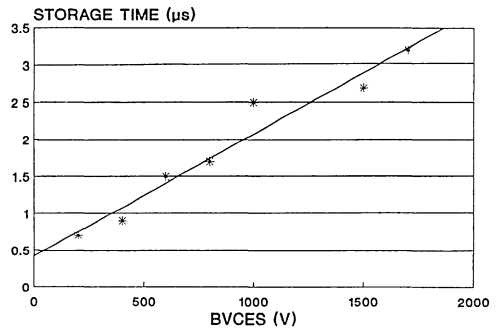


Fig. 2. Storage time behaviour versus rated BV_{CES} for bipolar transistors.

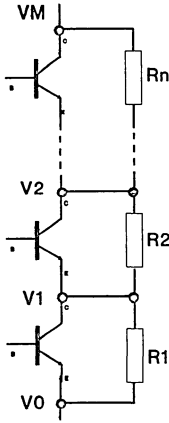


Fig. 3. Connection of sharing capacitors.

If we suppose that device 1 has the lower I_{RM} , V_{R1} will be the maximum reverse voltage ($V_{R1} = V_{RM}$) and developing the equation (2):

$$V_M = V_{RM} + V_{RM} - \Delta V_{R12} + \dots + V_{RM} - \Delta V_{R1n} = n \cdot V_{RM} - \sum_2^n \Delta V_{R1n} \quad (3)$$

The worst case condition, when n devices are connected in series, occurs when (n-1) devices have maximum leakage current and one device has the lowest possible leakage current: $\Delta I_{R1n} = \Delta I_{Rmax}$.

In this case, setting $R_1 = R_2 = \dots = R_n$, the solution of the equations 1 and 2 gives:

$$R = (n \cdot V_{RRM} - V_M) / (n-1) \cdot \Delta I_{Rmax} \quad (4)$$

2.2 EVALUATION OF ΔI_{Rmax} .

ΔI_{Rmax} is the sum of ΔI_{RD} + ΔI_{RT} , where:
 - ΔI_{RD} is the maximum leakage current dispersion at a fixed V_R and T_j .
 - ΔI_{RT} is due to the difference between the junction temperatures of each device (ΔT_j).
 For devices today available $\Delta I_{RD} \approx 0.6IRM$ @ $V_R = V_{RRM}$ and $T_j = 100^\circ C$.

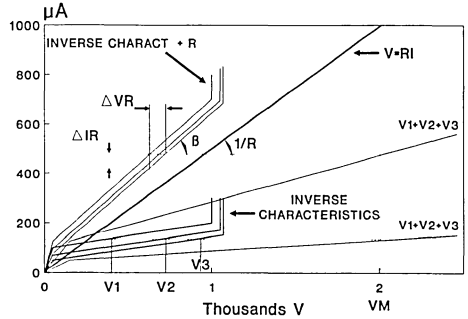


Fig. 4. Graphical calculation of sharing resistors when V_M and ΔV_R are fixed.

The difference in junction temperature depends on both differences of power dissipation and on the thermal resistance between devices.

$$\Delta T_j = \Delta (R_{th} \cdot P_{DISSIPATION})$$

Experience shows that $\Delta T_j = 10^\circ C$ is the maximum value for insulated devices mounted on the same heatsink.

Using the derating shown in figure 5, for $\Delta T_j = 10^\circ C$:

$$\Delta I_{RT} = 0.2 IRM.$$

Taking a safety margin we can use:

$$\Delta I_R = 0.85 IRM.$$

2.3 EXAMPLE 1: series connection of three STHV82 Power MOSFETs:

- Ratings:
 $V_{DSS} = 800V$
 $I_{DSS} \text{ max} = 1000\mu A @ T_j=125^\circ C$
 $R_{DS(on)} \text{ max} = 2\Omega @ T_j=25^\circ C$
 $R_{thj-case} = 1^\circ C/W$

Conditions:

Maximum blocking voltage: $V_M = 2000V$

Maximum Current and duty cycle:

$I_M = 3A, t_{on}/T = 0.5$

Case temperature:

$T_{CASE} = 80^{\circ}C$

Switching frequency : 50KHz.

Calculation of sharing resistor values.

T_j can be estimated using:

$$R_{DS(on)} @ T_j = 100^{\circ}C \approx R_{DS(on)}(25^{\circ}C) \cdot 1.7$$

$$T_j \approx T_{case} + R_{thj-case} \cdot$$

$$R_{DS(on)} \cdot I_D^2 \cdot t_{on}/T \approx 100^{\circ}C.$$

For $T_j = 100^{\circ}C$ using the derating of figure 5:

$$I_{RM} = (1 - 0.6)mA = 0.4mA$$

For safety operation and reliability

$$V_{RM} = 0.9 V_{DSS} = 720V.$$

Using equation (4):

$$R = (3 \cdot 720 - 2000)/(2 \cdot 0.4 E-3) = 200 \text{ k}\Omega.$$

Maximum power dissipation of each resistor when $t_{on}=0$: $V^2/R = 2.6 \text{ W}$.

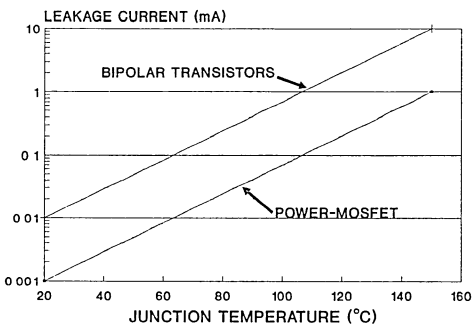


Fig. 5. Leakage current versus junction temperature.

2.4 IS IT POSSIBLE TO ELIMINATE THE SHARING RESISTORS?

For high frequency operation, it is necessary to consider the impedance of the output capacitance of the device which is in parallel with the sharing resistors.

In the previous example the impedance of the STHV82 output capacitance (150pF) is much lower than the calculated value of the sharing resistors:

$$Z_{Coss} = 1/2\pi f Coss \approx 21 \text{ K}\Omega \ll 200K\Omega$$

Therefore, if only high switching frequency conditions are expected, then the sharing resistors can be omitted.

3.0 DRIVING CIRCUIT FOR FAST SWITCHING DEVICES IN SERIES.

Two philosophies for driving switching power devices in series and for optimizing transient voltage sharing can be developed:

- 1) Driving each device in series with synchronized pulses and masking the difference of switching time.
- 2) Equalizing switching times with an optimized driving circuit.

Synchronized driving pulses can be generated by a transformer and delay turn-off time difference can be masked by snubber capacitors.

When continuous mode and wide range of duty cycle are required, it is difficult to design a method for driving the transformer. In this case auxiliary supplies and optocouplers can be used.

Equalization of switching times and continuous mode can be achieved using capacitive coupling between output circuit and driving circuit and diode network can be used for continuous bias.

3.1 DRIVING CIRCUIT GENERATING SYNCHRONIZED PULSES AND TRANSFORMER COUPLING.

It is possible to achieve excellent synchronization of the driving pulses together with good control of the driving voltage and current.

Figure 6 shows a driving circuit for both voltage and current controlled devices.

The coupling inductances between the primary winding and every secondary must be as balanced as possible in order to equalize all the transfer impedances.

In both circuits the device driving current is limited on the primary side of the transformer; this feature reduces the difference in delay turn-off time of devices in series.

In fact during delay turn-off time or storage:

$$(I_{D1} + I_{D2}) = I_D \cdot n_2/n_1$$

Input impedances of devices ≈ 0

$$(-I_{B1} \approx -I_{B2} = I_D/2).$$

At the end of storage for bipolar transistors or at the end of Miller effect for voltage controlled devices (Power MOSFET, IGBT) the input

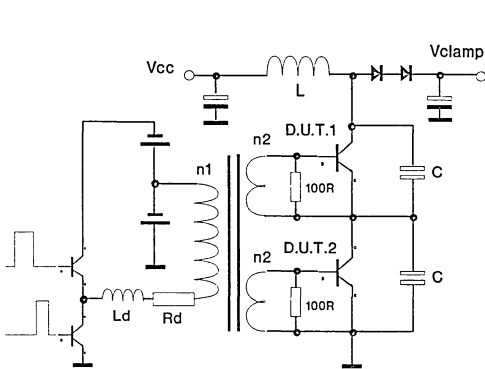


Fig. 6. Synchronized Drive of fast switching power devices in series using a transformer.

impedance becomes very high and the driving current fall, when the faster device turns-off, the device with the higher turn-off delay time increases its switching speed because it is driven by all the available current ($-I_{B(G)} = I_D \cdot n_2/n_1$).

3.2 EQUALIZATION OF TURN-OFF DELAY TIMES USING CAPACITANCES.

In the circuit of figure 7, the capacitors transmit driving voltage to the high side devices and the diodes supply continuous gate voltage during the on state. The circuit works as follows.

During transition: We suppose that initially all Power MOSFETs are in the off state and capacitor voltages are balanced. When the positive edge is applied to drive circuit, P₁ turns-on and pulls down the source of P₂. The capacitor network charges the gate of P₂. P₂ starts turn-on phase and pulls down source of P₃ etc...

The turn-off phase is similar to the turn-on phase. When P₁ turns-off, the source of P₂ is pulled up. A negative voltage discharges the gate of P₂ into the capacitor network turning

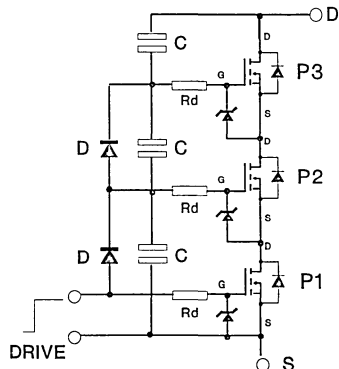


Fig. 7. Capacitors and diode network driving Power MOSFETs connected in series.

P₂ off, etc.

For a better voltage balance during switching, the capacitor must be charged to the same voltage ($V_{C1}=V_{C2}=...=V_{C3}$); imbalance is due to Power MOSFET gate charge and discharge of the capacitors network. For this

$$\Delta V_{max} = (n-1) \cdot Q_{GATE\ CHARGE} / n \cdot C$$

During on state:

$$V_{GATE}(n) = V_{DRIVE} - (n-1) \cdot (V_{DS(on)} + V_{F\ diode})$$

Therefore, for full saturation of every device connected in series a driving voltage greater than 15V is necessary.

Possible configurations. This circuit configuration can be used for series connection of IGBTs and BIPOLAR TRANSISTORS.

When connecting IGBTs, sharing capacitors are necessary because the turn-off current tail of IGBTs does not depend on the driving circuit.

ADVANTAGES: Using POWER MOSFETs this circuit allows optimum dynamic voltage balance with low values of capacitors so minimizing energy dissipation.

DISADVANTAGES: The circuit is critical when driving bipolar transistors due to high drive energy.

It is difficult to optimize switching waveforms. You can see in Photo 1 that current fall waveforms are not correct.

The driving voltage necessary for full saturation can be greater than the rated gate voltage.

For better on-state and switching performances, a regulator for each POWER MOSFET gate must be introduced (Figure 8) and optimization of the driving circuit will be necessary.

EXAMPLE 2.

Photo 2 shows POWER MOSFET drain voltage balance and drain current behaviour in the circuit of figure 7, where STHV102 devices are connected in series and in parallel.

$$C = 1500pF.$$

$$Q_{GATE\ CHARGE\ of\ 2 \cdot STHV102\ @\ (V_G = 15V) = 2 \cdot 85nc = 170nc$$

$$\Delta V = 170\ E-9 / 2 \cdot 1500\ E-12 = 56.5V$$

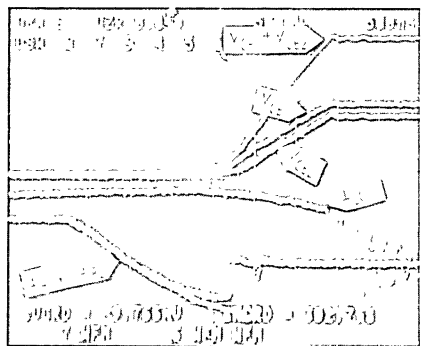
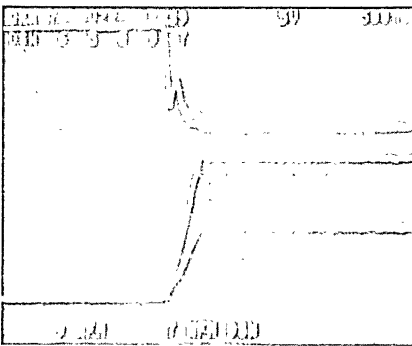


Photo 1. Voltage sharing and drain current of two Power MOSFETs in series as described in the example 1.
I = 2A/div, V = 500V/div.

Photo 2. Load current and voltage sharing behaviour of two BUV46 in series as shown in figure 5. C_S = 4.7nF,
I_B = 0.5A/div, I_{LOAD} = 2A/div, V = 500V/div.

4.0 TRANSIENT VOLTAGE SHARING WITH SYNCHRONIZED DRIVING CIRCUIT.

The transition overvoltages due to the difference between turn-off times can be controlled using sharing capacitors as shown in figure 9.

During switching operation, discharge of the sharing capacitors generates power losses so reducing efficiency of the converter.

In this note we define the losses of efficiency due to the capacitors discharge as follows:
Balancing losses/handled power = $n \cdot 0.5 \cdot C \cdot V^2 \cdot f / (V_M \cdot I_C \cdot \text{duty cycle})$.

4.1 HOW TO CALCULATE SHARING CAPACITORS.

Worst case condition occurs at turn-off with a inductive load. When the faster device in series turns-off, all the current load charges the capacitance in parallel to the slower device output, and generates a fast voltage rise. Using suitable capacitances it is possible to retard the voltage rise and to fix ΔV_R as shown in figure 9.

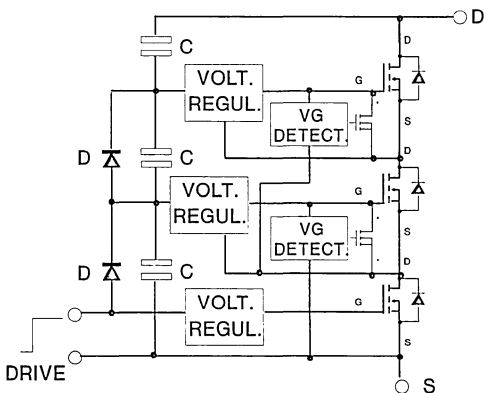


Fig. 8. Driving circuit of figure 7 for optimized driving voltage and switch-off.

$$C = \Delta Q / \Delta V_R = \int_{t_2}^{t_1} (I_1(t) - I_2(t)) dt / \Delta V_R \quad (5)$$

For n devices connected in series and setting $C_1 = C_2 = \dots = C_n$, Δt and ΔI are fixed to the maximum value.

4.2 SERIES OF BIPOLAR TRANSISTORS.

At turn-off the difference in storage time must be considered. In fact, denaturation at the end of the storage will cause collector voltage rise. For bipolar transistors the spread of this parameter, about 50%, is much higher than the fall time. For this $\Delta Q \approx I_{OFF} \cdot \Delta t_{storage}$ and the equation (5) becomes:

$$C_{MIN} = I_{OFF} \cdot \Delta t_{storage} / \Delta V_R \text{ max.} \quad (6)$$

EXAMPLE 3:

Series connection of two BUV46AFI.

Ratings:

- $V_{CES} = 1000V$
- $1.5\mu s < t_{storage} < 2.5 \mu s @ I_C = 2.5A;$
- $I_{B1} = -I_{B2} = 0.5A, T_C = 25^\circ C.$
- $I_C \text{ nom.} = 5A$

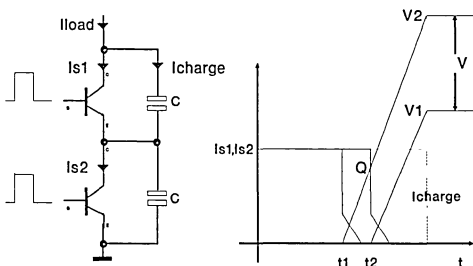


Fig. 9. Evaluation of sharing capacitors reducing the effect of delay turn-off time spread.

Conditions:

Maximum turn-off clamping voltage:

$$V_M = 1600V.$$

$$I_{OFF \text{ max.}} = 3A.$$

Switching frequency:

$$15 \text{ KHz, duty cycle} = 0.5$$

$$I_{B1} = -I_{B2} = 0.5A$$

Solution:

For safety margin:

$$V_{CEmax} = 0.9 \cdot V_{CES} = 900V$$

$$\Delta V_{R \text{ max}} = 2 \cdot V_{CEmax} - V_M = 200V$$

Using equation (6):

$$C_{2MIN} = (3 \cdot 1E-6)/200 = 15nF.$$

The power dissipation due to discharge of sharing capacitors is:

$$\text{Balancing losses} = P_D = C \cdot V^2 \cdot F = 144 \text{ W.}$$

(Balancing losses/handled power %) =

$$P_D / I \cdot V_{max} \cdot 0.5 \cdot \% = 6 \%$$

For better efficiency this energy must be reduced. For this, it is necessary to limit the maximum spread by a selection of devices.

If $\Delta t_{storage} = 300ns$, then a 4.7 nF sharing capacitor can be used as shown in photo 2.

4.3 SERIES OF POWER MOSFETs.

The current fall in POWER MOSFETs is very fast; equation (5) becomes:

$$\Delta V_R = I_{OFF} \cdot \Delta t_{OFF} / C$$

t_{OFFmax} can be calculated using gate charge, as shown in figure 7:

$$- t_{OFF} = (Q_1 + Q_2)/I_{GATE}$$

If I_{GATE} is balanced for all devices in series , then $\Delta t_{OFF \text{ max}}$ can be calculated using the distribution of figure 11; moreover, due to

temperature independance of gate charge, temperature difference between junction devices can be disregarded:

$$- \Delta t_{OFF} = 5/100 \cdot (\text{typical value of } t_{OFF})$$

If each POWER MOSFET has its own driving resistor, then tollerance of resistors must be considered and delay turn-off time can be calculated as follows:

$$- t_{OFF} = t_a + t_b = R_G C_{GS} \ln 3 + Q_2 R_G / (V_{Drive} - G_m I_D)$$

EXAMPLE 4: Series of two STHV102.

Ratings:

$$V_{DS} = 1000V$$

$$\text{Gate charge: } Q_1 + Q_2 = 62 \text{ nc} \pm 5\%$$

Conditions:

$$I_G = 100 \text{ mA.}$$

Maximum clamping voltage:

$$V_M = 1600V$$

$$I_{OFF} = 3A$$

$$F = 15 \text{ KHz, duty cycle} = 0.5$$

Solution:

For safety margin:

$$V_{DSmax} = 0.9 \cdot V_{DS} = 900V$$

$$\Delta V_{R \text{ max}} = 2 \cdot V_{DSmax} - V_{max} = 200V$$

$$\Delta t_{OFF} = \Delta (Q_1 + Q_2)/I_G =$$

$$6.2 \text{ E} - 9/ 100 \text{ E} - 3 = 62ns.$$

$$C_{MIN} = (3 \cdot 62 \text{ E} - 9) / 200 = 930pF.(1000pF)$$

$$P_D @ F=15 \text{ KHz} = C V^2 \cdot f = 9.6 \text{ W}$$

(Balancing Losses/handled power) = 0.4 %
Photo 3 shows devices behaviour with the conditions of the example and C = 1500pF.

4.4 SERIES OF IGBTs.

Photo 4 shows the behaviour of two 1000 V IGBTs in series at turn-off using an inductive load with sharing capacitors (1500pF). Due to the high fall time value (figure 9), the total voltage ($V_{CE1} + V_{CE2}$) can reach the clamping voltage before the end of current fall.

Therefore, the equation (6) can not be simplified and ΔV_R must be split as follows:

$$\Delta V_R = \Delta V_{R1} + \Delta V_{R2}$$

where:

$\Delta V_{R1} = V_1 - V_2$ @ $t = t_a$ (photo 4) is due both, to the delay turn-off time difference, and to the difference of current tail during voltage rise.

ΔV_{R2} is due to the difference of sharing capacitor charge when $V_1 + V_2 = V_{CLAMP}$ = constant due to the difference of current tail and Δt_{FALL} : $\Delta V_2 = \Delta Q_2 / 2C$

The minimum value of sharing capacitor can not be calculated easily due to the influence of dV/dt on the current tail behaviour.

For easy evaluation, the charge time of the sharing capacitor ($t_a - t_0$) must be equal to the maximum t_{FALL} . In this case:

$$C = 2 \cdot (I_{OFF} - I_{TAIL}/2) \cdot t_{FALLmax}$$

$$\Delta V_R = \Delta V_{R1} = (\Delta t_{OFF} \cdot (I_{OFF} - I_{TAIL}/2)) / C + \Delta I_{TAIL} \cdot t_{FALLmax} / 2C$$

Δt_{OFF} depending on gate charge spread is temperature independent.

I_{TAIL} , ΔI_{TAIL} , t_{FALL} are temperature dependent as shown in figure 13.

EXAMPLE 5:

Series of two IGBTs STGH8N100.

Ratings:

$$V_{CESmax} = 1000 \text{ V}$$

$$I_{Cmax} = 8 \text{ A @ } T_c = 125^\circ \text{C}$$

$$t_{FALL} = 800 \text{ ns } \pm 20\% \text{ @ } T_c = 125^\circ \text{C}$$

(see figure 9)

Gate charge $\approx 60 \text{ nc } \pm 5\%$
(similar to STHV102)

Conditions:

$$V_{CLAMP} = 1600 \text{ V}$$

$$\Delta V_{Rmax} = 200 \text{ V}$$

$$I_{Cmax} = 8 \text{ A}$$

$$T_{jmax} = 125^\circ \text{C}$$

$$I_{GATE} = 100 \text{ mA}$$

$$f = 15 \text{ KHz, duty cycle} = 0.5$$

Solution:

$$C = 2 \cdot (I_{OFF} - I_{TAIL}/2) \cdot t_{FALLmax}$$

$$t_{FALLmax} / V_{CLAMP} = 7.8 \text{ nF}$$

$$\Delta t_{OFF} = \Delta (Q_1 + Q_2) / I_G =$$

$$6.2 \text{ E} - 9 / 100 \text{ E} - 3 = 62 \text{ ns.}$$

$$\Delta V_R = \Delta V_{R1} = (\Delta t_{OFF} \cdot (I_{OFF} - I_{TAIL}/2)) / C +$$

$$\Delta I_{TAIL} \cdot t_{FALLmax} / 2C = 113 \text{ V}$$

Resulting $\Delta V_R \ll 200 \text{ V}$, a 6.8 nF capacitor can be used and $\Delta V_R = 130 \text{ V}$.

Balancing losses =

$$P_D (15 \text{ KHz}) = C \cdot V^2 \cdot f = 65 \text{ W}$$

(Balancing Losses/handled power) =

$$P_D / V_{max} \cdot I \cdot 0.5 = 1 \text{ \%}.$$



Photo 3. Load current and voltage sharing of two Power MOSFET STHV102 in series as shown in figure 5. $C_S = 1.5\text{nf}$, $\Delta t_{\text{off}}^t = 60\text{ns}$, $I = 2\text{A/div}$, $V = 500\text{V/div}$.

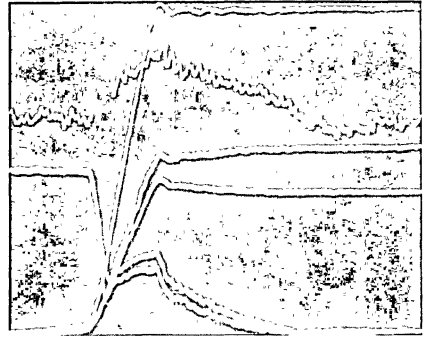


Photo 4. Turn-off behaviour of two IGBTs STGH8N100 in series with synchronized driving pulses. $C = 1.5\text{nF}$, $T_J = 100^\circ\text{C}$. $I = 2\text{a/div}$, $I_{\text{CHARGE}} = 0.5\text{A/div}$, $V = 200\text{V/div}$.

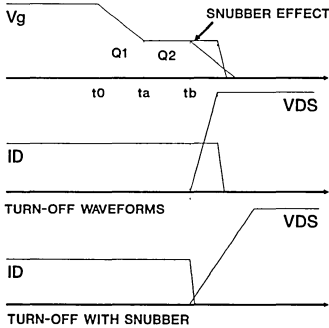


Fig. 10. Turn-off behaviour of Power MOSFET when connecting snubber capacitors.

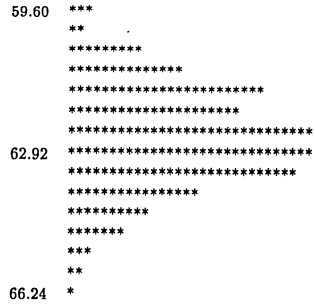


Fig. 11. Spread of the Power MOSFET gate charge.

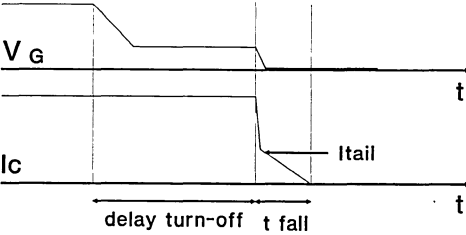


Fig. 12. Current fall behaviour of IGBT devices.

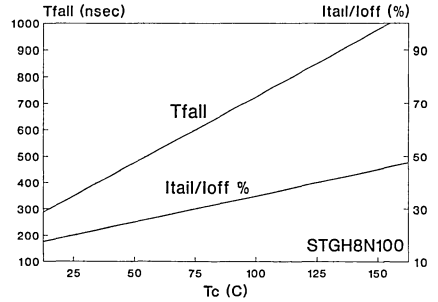


Fig. 13. t_{FALL} and current tail of IGBTs vs junction temperature.

5.0 CONCLUSIONS.

Every switching power device can be connected in series successfully in order to make a power switch for fast switching applications working at a voltage greater than 1500 V.

For optimum voltage sharing during steady state and switching, it is necessary:

- to make a compromise with the additional power losses introduced by sharing capacitors and by sharing resistors.
- that the junction temperature difference between devices in series must be as low as possible; especially for bipolar transistors and IGBTs.

Bipolar transistors require a selection by storage time.

Power MOSFETs are temperature independent and have very low parameter

spread, making them easy to connect in series.

IGBTs need considerable sharing capacitors, but these devices are attractive thanks to their very low saturation voltage and low driving energy.

The driving circuit can be made either by using a transformer for synchronized driving pulses, or with a diode and capacitor network.

When using a transformer, driving voltage or current can be controlled easily, but, continuous mode and a wide range of duty cycle can be a problem .

The diode and capacitor network allows equalisation of devices turn-off time, so reducing sharing capacitors value when gate voltage controlled devices are used. This method requires hard optimization of the circuit for very fast switching applications.

**SEMICONDUCTOR DEVICES
POWER MOSFETS**



AN INTRODUCTION TO POWER MOSFETS

1. INTRODUCTION

1.1 MOSFET Operation

A MOSFET is a three-terminal device which in basic terms behaves as a voltage controlled switch - see figure 1. The device allows conduction between the source and drain terminals only if an appropriate voltage is applied to the gate.

The term MOSFET is an acronym, standing for **Metal-Oxide-Semiconductor Field Effect Transistor**. MOS describes the original structure of the device, which essentially consisted of three layers:

- a Metal layer which forms the drive electrode or gate, (replaced by polysilicon in modern designs)
- an Oxide isolation layer, which prevents current flow between the drive electrode and the other two electrodes of the device, but does not block the electric field, and
- a Semiconductor layer, which depending on the voltage at (and hence electric field caused by) the gate, either blocks or allows current to flow between the source and drain contacts.

See figure 2.

Figure 1. a) MOSFET circuit symbol b) Driving a MOSFET

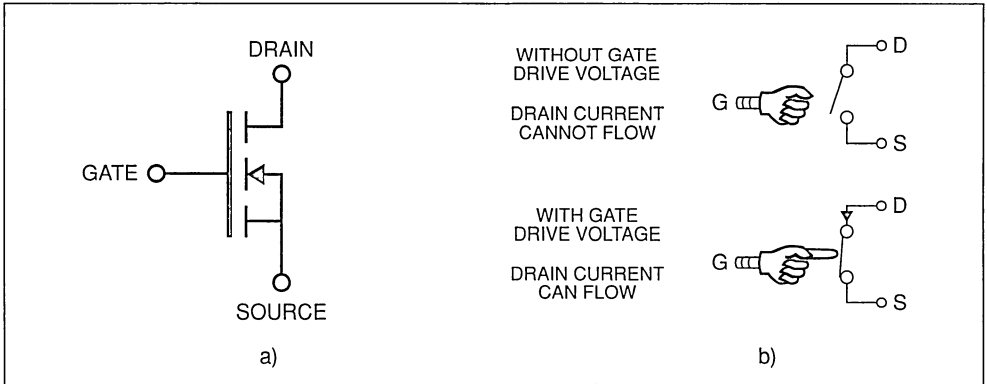
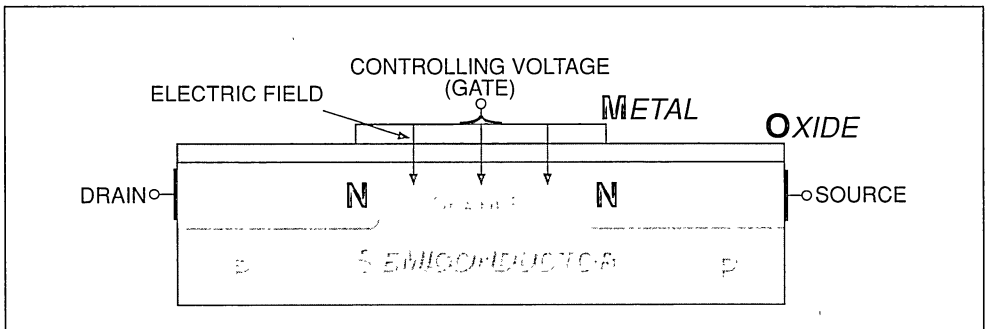


Figure 2. MOSFET Basic Structure



The controlled conduction path between the source and the drain is known as the channel. In the most conceptually simple type of MOSFET (and in the case of Power MOSFETs the most common), the N-Channel Enhancement type, if the gate is held at 0V, the channel does not conduct. However, if a positive drive voltage is applied to the gate (or more accurately between the gate and the source), the electric field it generates through the insulating oxide layer causes negative carriers to be attracted towards the gate, forming an "inversion layer" of minority carriers in the p-type silicon under the gate, and making the channel conductive.

1.2 Comparison of p and n Channel MOSFETs

The type of carrier generated depends upon the doping of the silicon in the channel - negative carriers for n-type silicon, and positive for p-type - that is to say the majority carrier. These types of MOSFETs are known as n-channel and p-channel respectively.

The fundamental difference between the p and n channel MOSFET is the polarity of the gate voltage required to make the channel more conductive. In the n-channel MOSFET, as discussed above, a positive gate voltage induces more negative carriers in the p type silicon of the channel, and so the channel becomes more conductive. Conversely, the drive voltage of a p channel transistor must be made more negative to increase the channel conductivity, as the carriers in this case are positive.

From a practical point of view, the main difference between the p and n channel MOSFET is the channel resistivity and consequently the relative size and cost of the devices. The mobility of n carriers is around 2.6 times the mobility of p carriers, and so to achieve the same channel on-resistance (and hence power dissipation when conducting current), a p-channel device would have to be around 2.6 times the size of an equivalent n-channel device. For this reason the vast majority of current Power MOSFET transistors are of the n-channel type.

1.2.1 Problems with generating the gate voltage

In many applications the transistor is placed between the load and the main positive rail of the supply. Thus, when the device is turned off, the source voltage is almost at the level of the positive rail. If an n-type device is used in this situation, the voltage required to turn it on is actually greater than the level of the positive supply. This means that additional circuitry is required to supply this.

The opposite applies to a p-type device connected between the load and ground, but as p-type devices are much less common, the problem is encountered less often.

1.3 Comparison of Enhancement and Depletion types

The example given in section 1.1 above discussed an enhancement mode transistor - that is when no voltage is applied to the gate, the channel is not conductive. However, another type of MOSFET exists, known as depletion mode. In this type, impurities implanted under the gate oxide during the fabrication of the transistor create a permanent channel, which is conductive even when no gate voltage is applied. In this type a gate voltage is applied to stop, rather than start, conduction.

The majority of current Power MOSFET transistors are of the enhancement type. This type is used partly because of the convention of using positive voltages to turn on devices, and partly because from a safety point of view in most applications it is desirable for the device to turn off if the power for the gate drive is lost.

1.4 Lateral and Vertical Structures

The simplified structure shown in figure 2 above is a lateral structure - the current flows sideways through the wafer from the source to the drain, and all three contacts are on the upper surface of the wafer. This structure is suitable for low power transistors, for example those in microprocessors and memories, and some medium power applications, but the restricted width of the conduction path means that its resistivity is relatively high. For higher power applications, this means poor energy efficiency and a potentially destructive buildup of heat. The alternative is to increase the effective width of the conduction path by allowing the current flow through the silicon substrate, and placing the drain contact on the lower surface of the wafer. This results in a device known as a vertical MOSFET, which is the most common type of Power MOSFET structure.

2. EVOLUTION OF POWER MOSFET STRUCTURE

Vertical double diffused MOS silicon gate technology represents the final stage in the evolution of vertical Power MOSFET devices. The principal steps in this evolution have been:

- a) V groove MOSFET (VMOS)
- b) U groove MOSFET (UMOS)

- c) Double diffused MOS metal gate (VDMOS - metal gate)
- d) Double diffused MOS polycrystalline silicon gate (VDMOS - silicon gate).

See figure 3.

Currently, the VDMOS - silicon gate structure is still used, while the other three have become obsolete, due to problems in the manufacturing process.

All share some common characteristics: in all structures current flows vertically through the wafer from a source contact on the upper surface to a drain contact on the lower surface, and construction of all starts from an epitaxial lightly doped n⁻ layer grown on a heavily doped n⁺ substrate (for n channel devices).

The n⁻ region supports the largest proportion of the applied drain potential, as its doping level is much lower (and hence resistivity much higher) than the p body region.

2. VDMOS SILICON GATE

2.1 Structure

The VDMOS structure (figure 4) combines the best features of earlier technologies with improved fabrication techniques, similar to VLSI techniques,

to achieve much better performance.

Electron current flows from the source metal to the source contact, laterally through the channel, and then vertically through the drain and substrate to the drain metal.

The VDMOS structure consists of two layers: the lower layer consisting of doped polycrystalline silicon, and the upper being the source metallization. It is a self-aligned structure, as the holes etched in the polysilicon layer can be used as the mask for the diffusion of the p⁺ well and the n⁺ source. In this way the MOS channel regions are obtained by the difference in lateral diffusion of the two impurity distributions. The use of double diffusion results in very short channels (<= 1.5 micron).

The higher packing density resulting from the VDMOS structure directly reduces the cost and improves the performance of the device. The use of a highly doped polysilicon gate also reduces the possibility of sodium ion contamination of the gate oxide (and hence means that the gate voltage required to make the channel conductive, known as the gate threshold voltage $V_{GS(th)}$, has a more consistent value between MOSFETs of the same type) and the full surface source metallization allows better current distribution.

Figure 3. a) VMOS b) UMOS
c) VDMOS - Metal Gate d) VDMOS - Silicon Gate

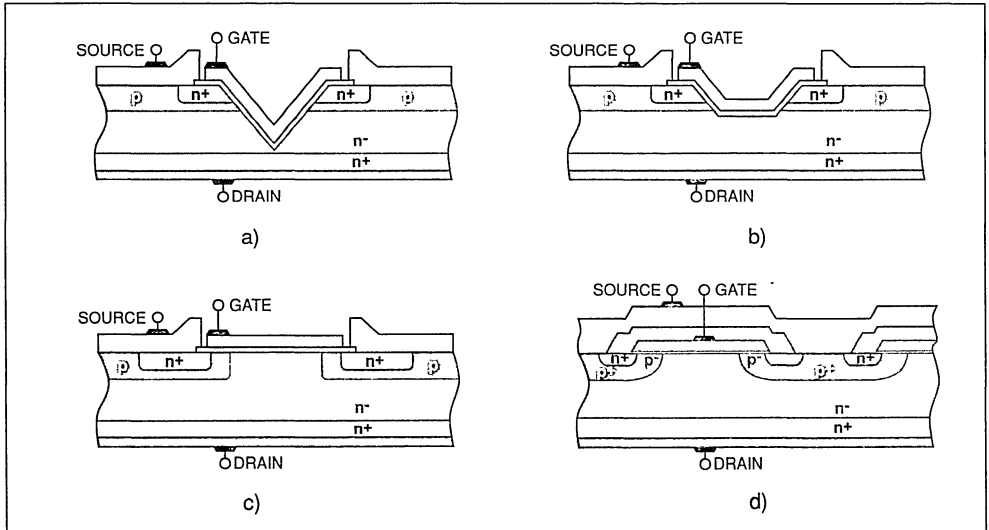
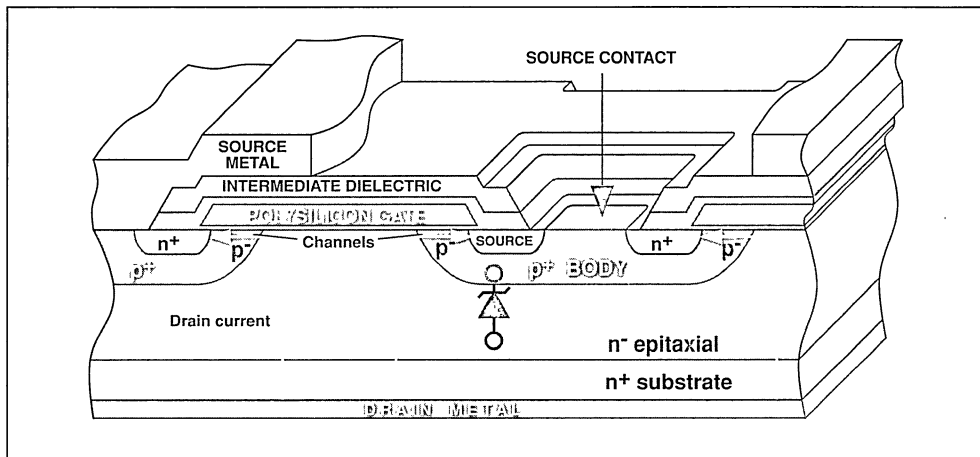


Figure 4. Schematic representation of VDMOS cell structure, showing parasitic diode



2.1.1 The Parasitic Diode

In the basic MOSFET structure, the n source region, the p well and the n drain combine to form a parasitic bipolar transistor. In practical designs this is removed by shorting together the n source and the p body regions. However, this still leaves a parasitic diode connected in anti-parallel between the drain and source - see figure 4. This diode conducts when the source is positive with respect to the drain, and can handle forward current equal to the drain current rating, and can be useful in some applications.

4. DESIGN OF A POWER MOSFET

In the design of a Power MOSFET transistor, the two parameters of most interest are the on-resistance of the conduction path between the drain and source ($R_{DS(on)}$) for a given chip area, and the drain-source breakdown voltage - that is the maximum voltage the device can block when turned off.

4.1 Drain-source on resistance - $R_{DS(on)}$

The vertical power DMOS consists of a large number of cells connected in parallel on a single piece of silicon, or die. The value of $R_{DS(on)}$ is heavily dependent on the topological layout - the shape and size of the cells, and the packing density.

Optimization of this parameter requires comparison between different geometrical solutions at both low and high voltages. If the behaviour of the components of the $R_{DS(on)}$ is analyzed (figure 5), it can be seen that for low voltage applications (< 400V) the channel

has the greater effect in defining its value. To optimize the $R_{DS(on)}$ it is necessary to maximize the Power MOSFET channel perimeter per unit area with a high packing density. Low voltage devices have a packing density of around 1.3 million cells per square inch - see figure 6a.

For high voltage devices (> 400V), the epitaxial layer resistance has a greater effect than the overall on-resistance. To optimize the $R_{DS(on)}$ it is necessary to minimise bulk resistance by selecting a low packing density layout which increases the area of the epitaxial drift region. High voltage devices have a packing density of around 350 000 to 500 000 cells per square inch - see figure 6b.

4.2 Drain-source breakdown voltage $V_{(BR)DSS}$

For the best possible ruggedness of the device, the Power MOSFET should be designed to break down first in avalanche mode in the bulk silicon. In this area the breakdown voltage depends upon the size of the n⁻ epitaxial layer. However, increasing the size of this layer increases the $R_{DS(on)}$ of the device, and so the design of the device is a result of a tradeoff between these two parameters.

At high voltages however, breakdown at the edges of the junctions begins to occur before the avalanche rating of the bulk silicon is reached, caused by surface electric field curvature and crowding.

To combat this, special edge structures have been developed to make the electric field along the edge of the junction more uniform and thus prevent

Figure 5. Comparison of elements of $R_{DS(on)}$ for low and high voltage devices

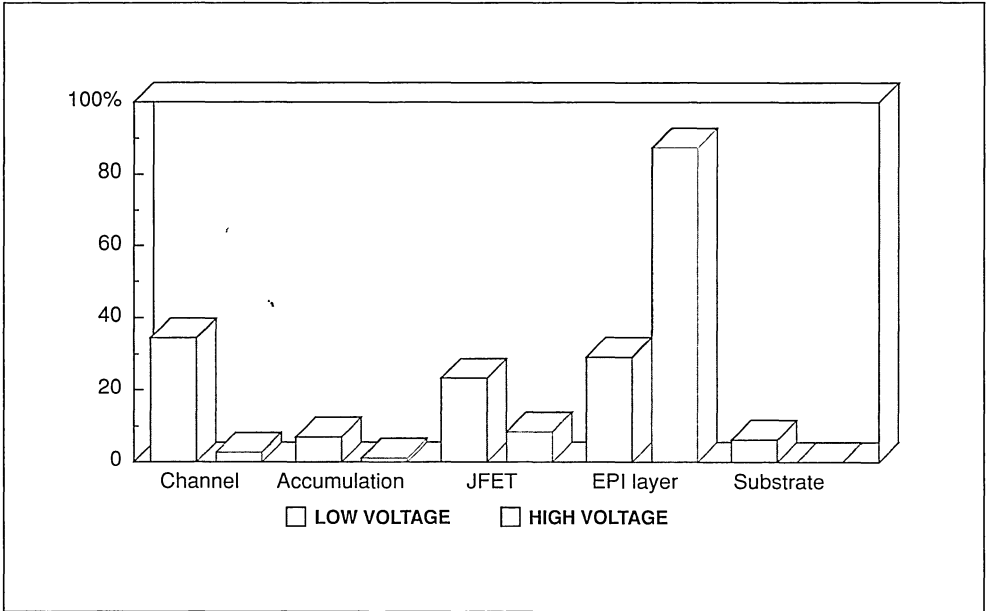
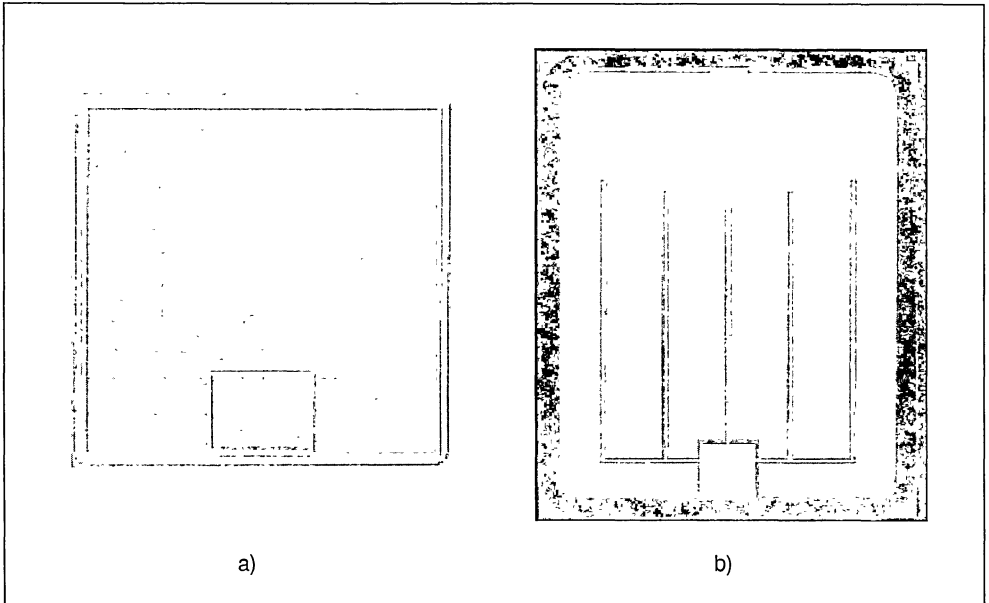


Figure 6. Power MOSFET die: a) 100V device
b) 800V device



breakdown at any point. This is achieved by adjusting the charge density along the edge of the junction by varying the dopant strength - see figure 7.

4.3 Threshold voltage

The value of the gate threshold voltage $V_{GS(th)}$ is dependent upon the thickness of the gate oxide, and on N_A , the peak impurity concentration in the laterally diffused body in the region between the source and drain.

Under strong reverse bias, channel punch-through can occur as a result of insufficient impurity charge in the channel. To avoid this a tradeoff between $V_{GS(th)}$ and channel length must be made. For a fixed gate oxide thickness, a shorter channel implies a greater peak N_A and a higher $V_{GS(th)}$. However a lower $V_{GS(th)}$ sets a lower limit to the channel length in relation to the punch-through problem.

Because $V_{GS(th)}$ has a negative temperature coefficient, its value cannot be too low. However, if it is too high, devices cannot be driven directly from low voltage logic circuits.

5. APPLICATIONS

In general terms Power MOSFETs compete with

Bipolar transistors and IGBTs, and find applications in power conversion (switch mode power supplies etc.), motor drive, lamp ballast, and power switches.

Its main advantages over the other types of device are its simple drive requirements, lower switching losses at high frequencies, and low cost at low voltages.

At medium to high voltages (above around 200V) and low frequencies, the MOSFET becomes less attractive in comparison with the bipolar transistor. This is because at these voltages the large area of silicon required to sustain the breakdown voltage while keeping the on-resistance to an acceptable level makes the device relatively expensive.

For a MOSFET:

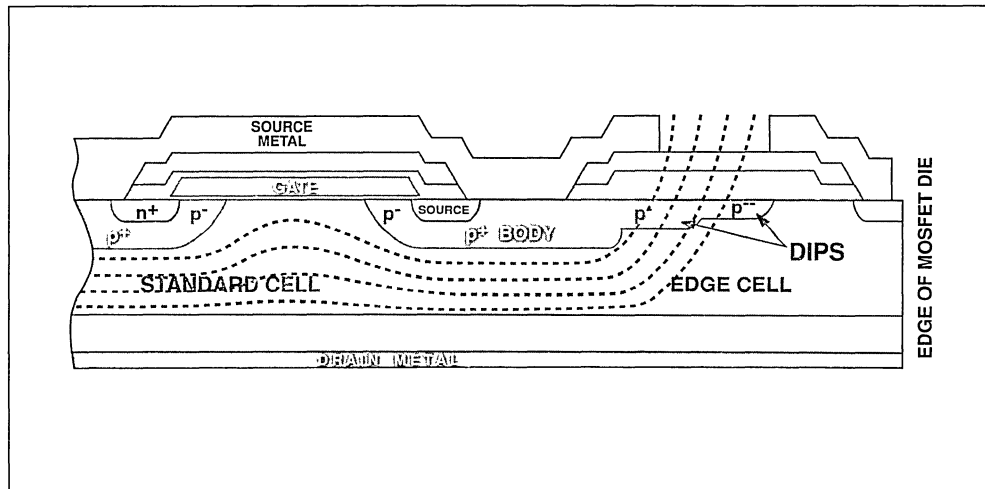
$$\frac{R_{DS(on)} @ V2}{R_{DS(on)} @ V1} = \frac{V2}{V1}^{2.4-2.6}$$

while for a Power Bipolar:

$$\frac{R_{ON} @ V2}{R_{ON} @ V1} = \frac{V2}{V1}^{0.7}$$

At high operating frequencies (>100kHz) MOSFETs are the only suitable power semiconductor.

Figure 7. Preventing field crowding and breakdown with DIPS (Double Implanted Planar Structure) edge termination



6. SWITCHING

The fundamental objective of the Power MOSFET device is to switch high quantities of power with as low losses as possible - to maximize the ratio:

$$\frac{\text{Total power switched}}{\text{Energy dissipated per cycle}}$$

In practical conditions, three main states of the device can be identified:

ON state

When the device is on and the channel is conducting, the dissipated power is:

$$P_{on} = V_{DS(on)} \cdot I_D$$

or alternatively:

$$P_{on} = R_{DS(on)} \cdot I_D^2$$

This depends upon the device design (cell dimensions and layout) and the technology used.

OFF state

When the device is off, the drain is at the supply voltage, and the power dissipated is:

$$P_{off} = V_{DD} \cdot I_{DSS}$$

I_{DSS} is the zero gate voltage drain current, and is usually very small.

Transitions

The power dissipated at the switching instant is:

$$P_{SW} = V_{DS}(t) \cdot I_D(t)$$

This depends upon the on/off switching speed of the device: see figures 8 and 9.

6.1 Switching frequency

Unlike the Power Bipolar, whose maximum operating frequency is limited by the rate at which the minority carriers in the base recombine, the Power MOSFET is only limited by the rate at which the drive circuit can charge the gate capacitance. Its operating frequency can thus be very high, for example hundreds of kHz.

7. SWITCHING CHARACTERISTICS OF THE POWER MOSFET INPUT

Power MOSFETs, unlike bipolar devices, require drive energy only during the charge and discharge of the input capacitances at the switching instants. Figure 10 shows an equivalent circuit of a MOSFET, driven by a voltage source with internal resistance

Figure 8. Current / Voltage switching waveforms

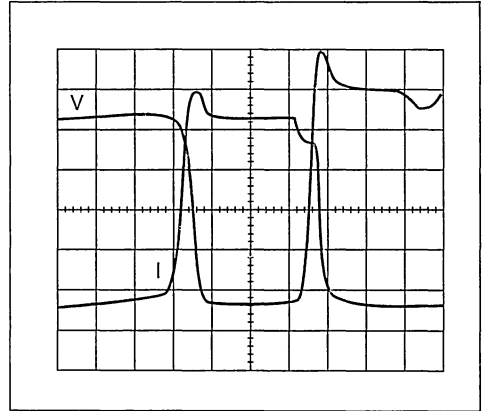


Figure 9. Power dissipation waveforms

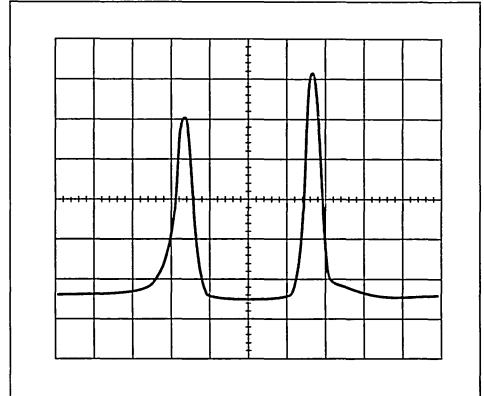
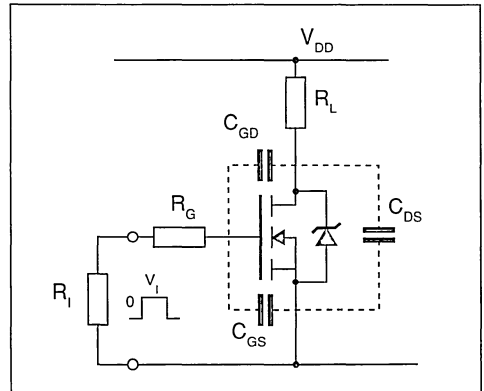


Figure 10. Power MOSFET equivalent circuit, showing parasitic capacitances



R_1 , and with a load R_L .

It should be noted that the effective input capacitance C_{iss} (a combination of the effects of C_{GS} and C_{GD}) does not remain constant, but varies through the switching cycle, because C_{GD} , the gate-drain capacitance, varies with V_{DS} , for two reasons:

- C_{GD} varies with the thickness of the drain depletion layer. As V_{DS} increases, the layer becomes thicker, and C_{GD} decreases.
- A more pronounced effect is due to the fact that when the device switches on, V_{DS} (and hence the voltage across C_{GD}) falls from V_{DD} to $V_{DS(on)}$. The input must be fed a charge Q , where:

$$Q = C_{GD}(V_{DD} - V_{DS(on)})$$

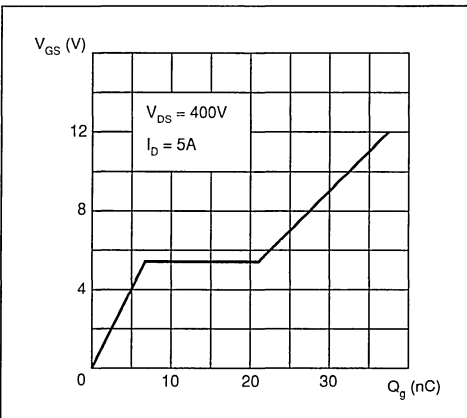
to account for this voltage variation across C_{GD} .

This occurs when the gate voltage becomes greater than $V_{GS(th)}$, and the drain voltage begins to fall. At this point the gate-source voltage V_{GS} cannot increase further until the charge Q has been supplied - thus for a while the input capacitance appears infinite. This phenomenon is known as the Miller effect.

Figure 11 shows the net effect of these two phenomena. The flat "step" in the centre of the graph is caused by the Miller effect, while the fact that the other two sections of the graph have different slopes is due to the former effect.

At turn-off the effects occur in reverse order, and so

Figure 11. Gate charge versus gate-source voltage (STP5NA50)



the turn-off behaviour is simply the inverse of the turn-on behaviour.

The drive energy required to drive the MOSFET during switching can thus be calculated using:

$$E_p = 1/2 Q_G \cdot V_{GS}$$

Q_G (the total gate charge) and V_{GS} can be obtained from figure 11.

The input energy can also be calculated in a more direct manner by calculating the integral of the input current I_g during turn-on or turn-off switching (the two areas are equal, see figure 12). This integral represents Q_G , which then allows calculation of E_p .

The driving energy required varies only with the die size of the device, assuming the same drive voltage.

Figure 13 shows a practical implementation of a drive circuit. The NPN transistor T1 conducts at the beginning of the ON phase to charge the MOSFET capacitance, while the PNP transistor T2 conducts at the beginning of the OFF phase to discharge the device.

The total energy dissipated per cycle in the input stage (including the MOSFET input) is:

$$E_p = Q_G \cdot V_{CC}$$

where V_{CC} is the supply voltage of the drive (12V in figure 13). This energy is actually dissipated in the two driving transistors, as the input capacitance acts only as a non-dissipative element, storing energy from T1 at turn on, and returning it to T2 at turn off.

Figure 12. Gate voltage and current switching waveforms

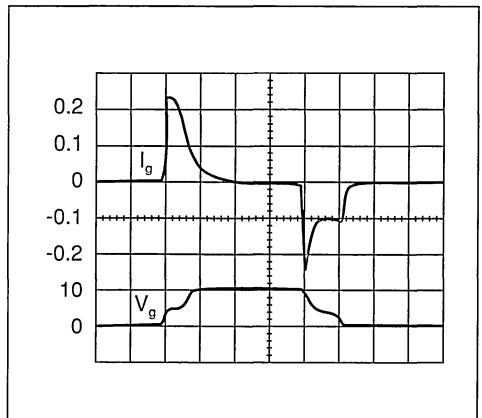
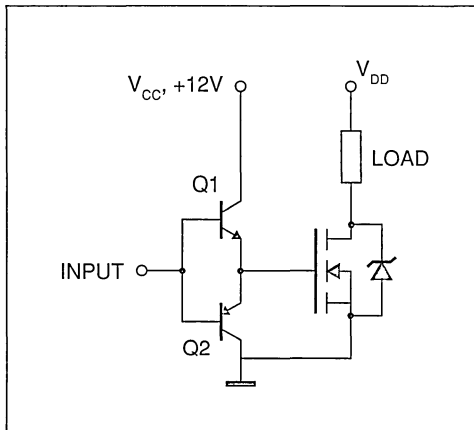
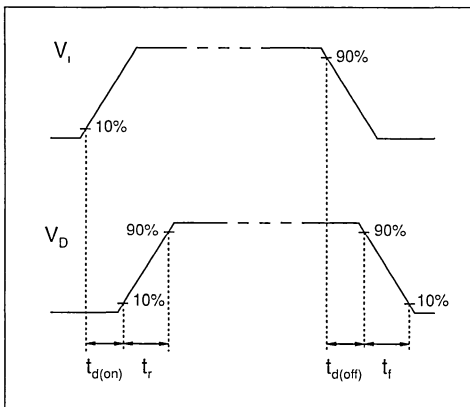


Figure 13. Practical MOSFET drive circuit

Figure 14. V_{GS} and V_{DS} waveforms when switching a resistive load

8. SWITCHING CHARACTERISTICS OF THE POWER MOSFET OUTPUT

8.1 Switching times

See figure 14.

8.1.1 Turn-on delay time ($t_{d(on)}$)

This represents the time required for V_{GS} to reach the threshold level $V_{GS(th)}$ at which the device begins to conduct. The increase of V_{GS} depends on the charging of a capacitor, and so is exponential:

$$V_{GS} = V_i(1 - e^{-t/R_i C_{ISS}}) \quad (1)$$

By substituting V_{GS} with $V_{GS(th)}$ and rearranging we can obtain:

$$t_{d(on)} = R_i \cdot C_{ISS} \cdot \ln \frac{V_i}{V_i - V_{th}}$$

Inserting typical values for V_i and $V_{GS(th)}$ ($V_i = 10V$, $V_{GS(th)} = 3V$) we get:

$$t_{d(on)} = 0.35 R_i \cdot C_{ISS}$$

In practice this time is very small (10 - 20ns) and during this time the device is off, and so the energy dissipated is in the order of picojoules, and is negligible in comparison with overall energy losses.

8.1.1.1 t_{rise} and t_{fall}

t_{rise} and t_{fall} are defined by the slopes of V_{DS} as shown in figure 14.

8.1.2 Turn-off delay time

$t_{d(off)}$ can be referred to as the delay time, since it represents the time necessary to remove the excess

charge from the gate and the channel, caused by too great a value of input voltage. Typical drain current and voltage waveforms are shown in figure 15.

8.3 Parasitic capacitances and resistances

The term R_i in equation 1 incorporates R_{DRIVE} , the equivalent output resistance of the drive circuit, and R_G , the internal resistance of the gate (the resistance between the external connection of the gate, and actual gate area on the die). C_{ISS} is a sum of the effects of C_{GS} , the capacitance between the gate and source, and C_{DS} , the capacitance between the drain and source, see figure 16a.

Obviously the smaller the value of the term $R_i C_{ISS}$, the faster V_{GS} reaches its final value, and the lower the switching losses. To minimize this time constant, the device user can adjust the value of R_{DRIVE} , and the device designer can control C_{ISS} and R_G .

The value of V_{DD} , the MOSFET supply voltage, influences the switching of the MOSFET - the higher the supply voltage, the higher the stored charge, and therefore the higher the t_r and the drive energy required. Figures 17, 18, 19 and 20 show the variation of the delay time t_d , the fall time t_f and the rise time t_r as a function of drain current and supply voltage, for a low voltage and a high voltage MOSFET switching resistive loads.

The variation of t_r and t_f with V_{DD} is similar to that of E_{pr} , as they are caused by the same phenomena. t_d is a function of C_{ISS} only, which, since the Miller effect is not present, is constant during this phase.

Figure 15. a) Turn-on with resistive load
b) Turn-off with resistive load

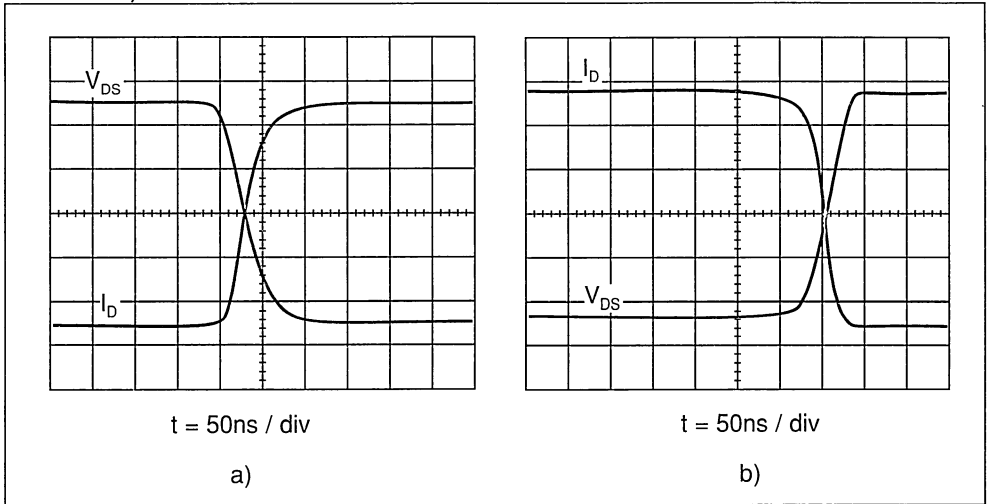


Figure 16. a) Power MOSFET equivalent circuit, showing internal gate resistance
b) Parasitic capacitances as a function of V_{DS}
c) Charging and discharging of parasitic capacitances at turn-on and turn-off

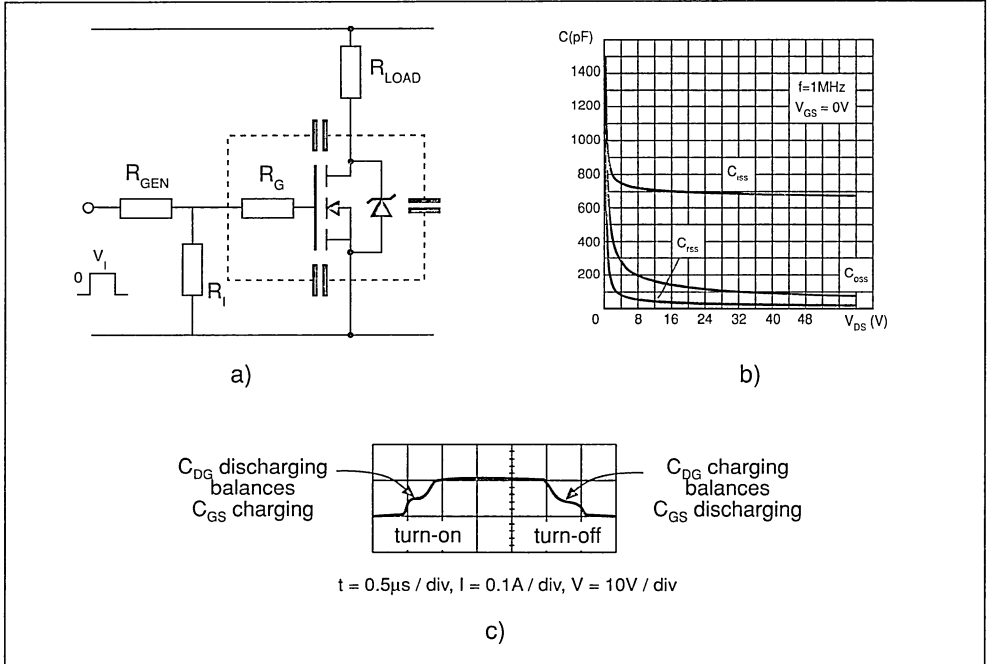


Figure 17. Delay, rise and fall times as a function of I_D (STP18N10, 100V, 140m Ω)

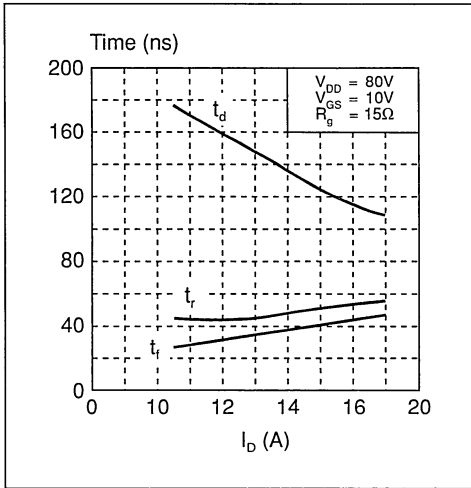


Figure 18. Delay, rise and fall times as a function of V_{DD} (STP18N10)

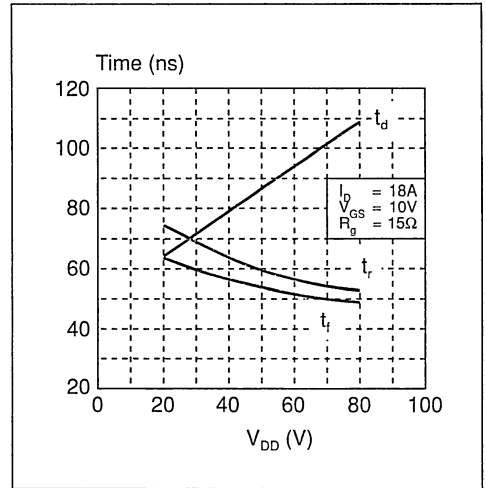


Figure 19. Delay, rise and fall times as a function of I_D (STP5NA50, 500V, 1.6 Ω)

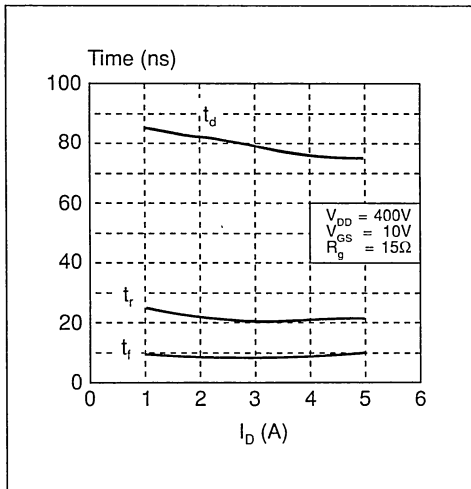
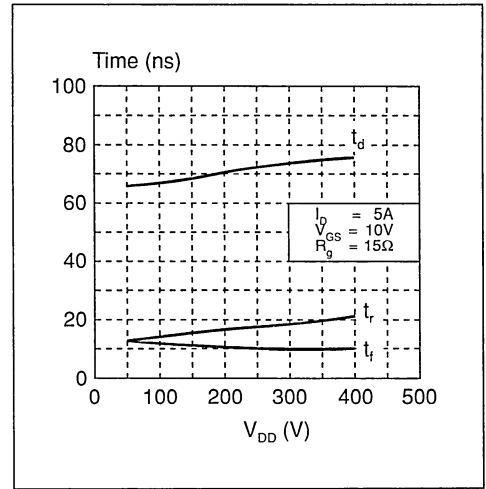


Figure 20. Delay, rise and fall times as a function of V_{DD} (STP5NA50)



The equivalent output capacitance C_{OSS} can have a great effect on the turn-on switching losses. When the device is turned on, C_{OSS} must be discharged, releasing an energy in the transistor equal to:

$$E = 1/2 C_{OSS} \cdot V_{DD}^2$$

and the power dissipated increases with voltage and

frequency. In high frequency, high voltage applications the device must be therefore be selected through a compromise between turn-on losses (affected by C_{OSS} , minimised by using a device with a smaller die size), and the conduction losses (affected by $R_{DS(on)}$, minimised by using a device with a larger die size).

8.4 Parasitic inductances

Figure 21 shows the main parasitic inductive elements, which affect di_D/dt . These are:

L_d -the parasitic inductance due to the connections between the clamping diode and the load

L_D -the parasitic inductance between the drain of the Power MOSFET device and the load

L_G -the parasitic inductance between the gate and the driving circuit

L_S -the parasitic inductance between the source and ground.

8.5 Energy dissipation in switching

Energy dissipation can be divided into four phases:

- i) the ON state
- ii) the OFF state
- iii) transition ON-OFF
- iv) transition OFF-ON

8.5.1 The ON state

In the ON state, when the channel is completely open, Power MOSFET devices have a minimum on-resistance, $R_{DS(on)}$, which is dependent on the junction temperature, T_J . This gives a power dissipation of:

$$P_{D(on)} = R_{DS(on)}(T_J) \cdot I_D^2_{RMS}$$

$$= R_{DS(on)} \cdot [1 + a(T_J - 25^\circ C)] \cdot I_D^2_{RMS}$$

where a is the positive temperature coefficient of $R_{DS(on)}$, equal to $8 \times 10^{-3} \text{ } ^\circ C^{-1}$.

The lower the $R_{DS(on)}$, the lower the power dissipation. This parameter can be controlled by the device manufacturer, by improving the back metallisation of the chip and its attachment to the case, by controlling the epitaxial growth of the drain, and by optimizing the Power MOSFET structure.

8.5.2 Off state

When the device is switched off, V_{DS} is equal to V_{DD} . Only the leakage current I_{DSS} flows through the device. The power dissipation during this period is given by:

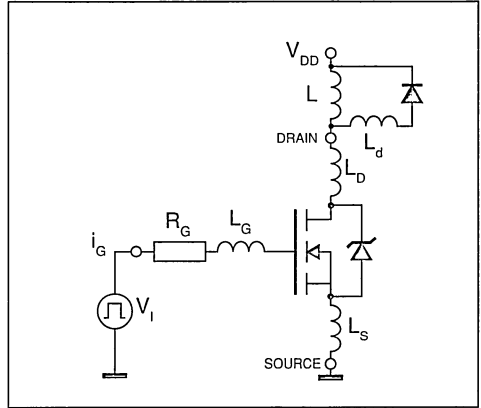
$$P_{off} = V_{DD} \cdot I_{DSS}$$

This energy is in the range of picojoules and is negligible in comparison with other losses.

8.5.3 Transitions

During transitions the instantaneous dissipated

Figure 21. Parasitic inductances



power is:

$$P(t) = V_{DS}(t) \cdot I_D(t)$$

The total energy consumption during each transition can be calculated with:

$$E = \int_{t_a}^{t_b} P(t) dt$$

$$= \int_{t_a}^{t_b} V_{DS}(t) \cdot I_D(t)$$

where t_a and t_b represent the beginning and end of the transitions respectively.

8.5.4 Calculating the total energy dissipation per cycle

The total energy dissipated per cycle in the Power MOSFET can be expressed as:

$$E_{TOT} = E_{on} + E_{off} + E_{off-on} + E_{on-off} + E_p$$

where:

- E_{TOT} = total energy dissipated per cycle
- E_{on} = total energy dissipated during the on-state
- E_{off} = total energy dissipated during the off-state
- E_{off-on} = total energy dissipated during turn-on
- E_{on-off} = total energy dissipated during turn-off
- E_p = total energy dissipated by the drive circuit

As E_{off} is in the order of picojoules, and E_p is in the order of nanojoules, they can be neglected, giving:

$$E_{TOT} = E_{on} + E_{off-on} + E_{on-off}$$

These three terms depend to differing degrees on

the operating conditions of the device, I_D , V_{DD} and the duty cycle.

8.6 Switching with an inductive load

In the majority of applications Power MOSFETs are used to switch power through inductive loads - for example in motor drives and switch mode power supplies. A typical clamped inductive load circuit is shown in figure 22.

The fast diode D is placed in the circuit to prevent large destructive overvoltages being generated. When the current through the inductor falls at turn-off, a voltage is generated in the inductor in the opposite sense to the supply voltage. When this occurs, diode D becomes forward biased and hence acts as a short circuit of the inductor, preventing the overvoltage from becoming too large. This process is known as freewheeling.

8.6.1 ON state

Figure 23 can be used to calculate the energy dissipation during the ON phase. The slope of I_D during the conduction phase is given by:

$$\frac{dI_D}{dt} = \frac{V_D}{L}$$

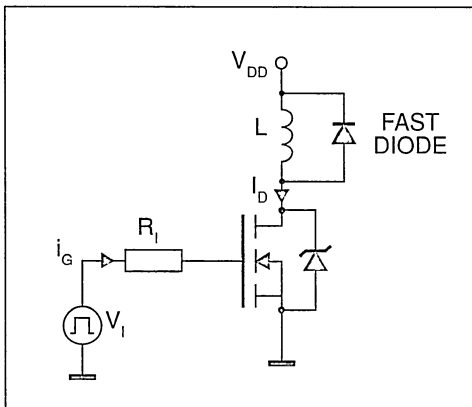
and the energy lost per cycle is given by:

$$E_{on} = \int_0^t I_D^2(t) \cdot R_{DS(on)} \cdot dt$$

where t is the pulse width.

In most cases, the slope of I_D is quite smooth, and

Figure 22. Power MOSFET with clamped inductive load



the above expression can be reasonably approximated as:

$$E_{on} = R_{DS(on)}(T) \cdot I^2 \cdot t$$

where I is the average value of I_D in the period t .

8.6.2 OFF state

The energy loss in the OFF state is the same as that given in section 8.5.2 above.

8.6.3 Turn ON transition

The turn on characteristics of the circuit are shown in figures 24 and 25.

Before the turn-on phase diode D is freewheeling (re-circulating) the load current.

Turn-on itself can be divided into two phases:

Point A to point B

Part of the current in the load begins to flow through the MOSFET device. Diode D begins to turn off, but until its reverse recovery time has passed, the diode continues to conduct and still appears as a short

Figure 23. I_D waveform during switching cycles

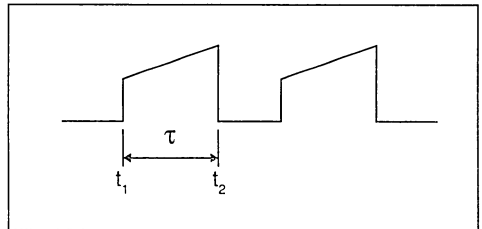
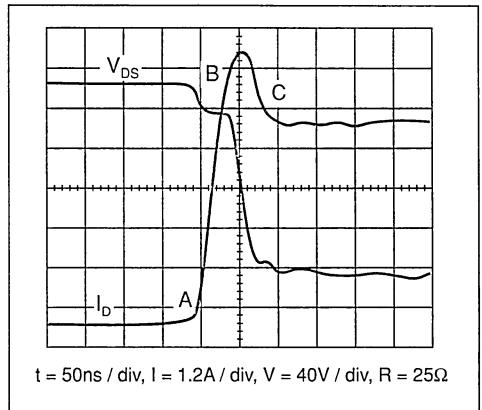


Figure 24. Turn-on with inductive load



circuit to the load. Because the load is shorted, the voltage across the MOSFET is almost equal to the supply voltage. There is a small step in the V_{DS} waveform due to the effects of the parasitic inductances L_D and L_S (which depend on the circuit layout). The size of this step depends on the rate of change of drain current di_D/dt .

Point B to point C

In this phase, the reverse recovery time of the diode has passed, and it has become reverse biased. The current in the Power MOSFET is the sum of the currents in the load and the diode, causing the peak in the I_D waveform (an overvoltage is created in the inductor by the increasing drain current).

The voltage V_{DS} falls to $V_{DS(on)}$ as the load is no longer shorted. The fall of V_{DS} is delayed by the Miller effect.

The output energy dissipation per turn-on cycle is shown in figure 25.

All of these phenomena mean that even if the switching is very fast, the existence of significant currents through and voltages across devices simultaneously means that losses can be high. Reducing these losses requires minimization of the rise time of I_D (increasing di_D/dt) and of the reverse recovery time of the clamping diode.

8.6.4 Turn OFF transition

The initial conditions of the turn off phase can be taken to be $I_D = I_{LOAD}$ and $V_{DS} = V_{DS(on)} = R_{DS(on)} \cdot I_D$, and the freewheel diode reverse biased. Figure 26

shows the turn-off characteristics.

Again it is possible to distinguish two phases:

Point D to point E

V_{DS} increases while I_D remains constant and equal to I_{LOAD} . The diode remains reverse biased.

Point F to point G

Diode D begins to conduct and so I_D begins to fall.

Figure 27 shows the energy dissipated in the output during the turn-off phase. Even though there is no effect of the diode reverse recovery time during this phase, losses are still high, as the Miller effect in the Power MOSFET delays fall of V_{DS} and therefore the turn-on of the freewheeling diode.

8.6.5 Power dissipation in the transitions

The power waveform is triangular in shape (see figures 25 and 27).

8.6.6 Improving power dissipation in the transitions

8.6.6.1 Increasing di_D/dt

The equation which applies to the input loop is:

$$V_i = R_i \cdot I_G + L_G \cdot di_G/dt + V_{GS} + L_S \cdot di_D/dt$$

where R_i is the equivalent resistance of the driving circuit. Considering the phase when I_D increases, it is possible to ignore the term $L_G \cdot di_G/dt$ as at this time di_G/dt is zero (the threshold voltage has been overcome, and i_G is constant), and so the expression can be rearranged as:

$$\frac{di_D}{dt} = \frac{V_i - R_i \cdot I_G - V_{GS}}{L_S}$$

So di_D/dt can be increased increasing V_i , and by reducing R_G and L_S .

8.6.6.1 Improving the reverse recovery of the diode

The faster the clamping diode used, the lower the current peak in the Power MOSFET, and the lower the energy dissipated.

The effects of the inductances L_D and L_S of the diode connections on V_D and I_D are shown in figure 28.

Figure 25. Energy dissipation during turn-on of inductive load

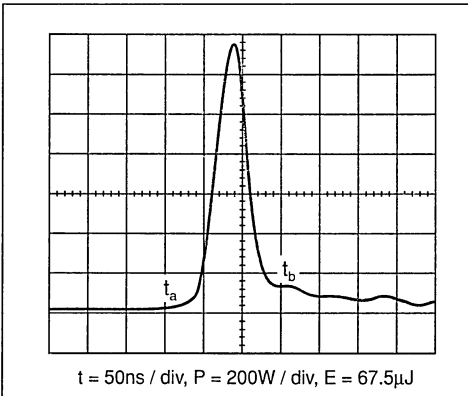


Figure 26. Turn-off with inductive load

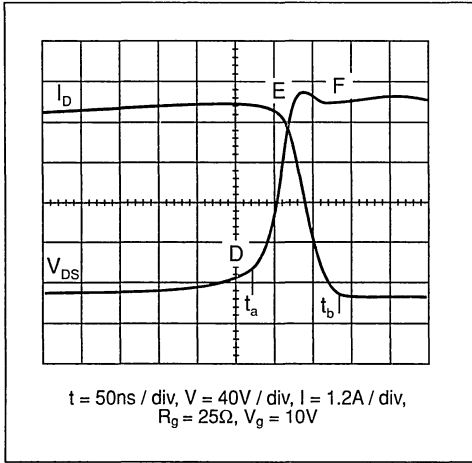


Figure 28. Effect of L_D and L_S on V_{DS} and I_D

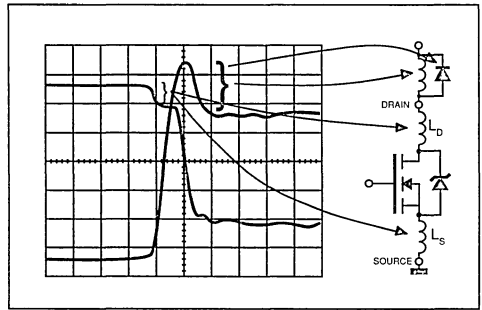
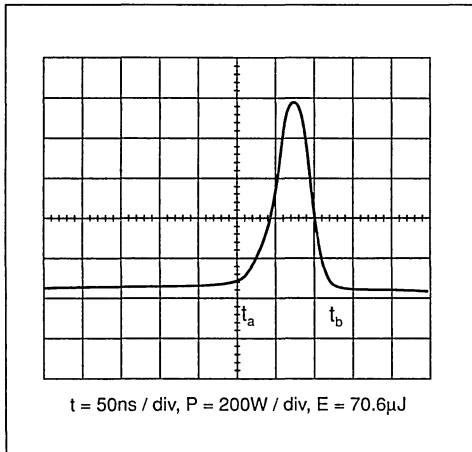


Figure 27. Energy consumption during turn-off of inductive load



A NEW APPROACH TO PARAMETER EXTRACTION FOR THE SPICE POWER MOSFET MODEL

by M. Melito, F. Portuese

ABSTRACT

The increasing complexity of Power MOSFET technology and the inclusion, on the same chip, of more and more intelligence together with the power switch, requires an accurate simulation of DC and AC characteristics of the power device to obtain a good correlation between simulation results and experimental data.

A robust design has to take the worst cases into consideration as well as the typical conditions. Also the simulation has to make provision for the spread of device characteristics due to manufacturing tolerances.

This paper describes a new approach to parameter extraction for a sub-circuit model of Power MOSFETs to be used in the SPICE circuit simulator which uses a powerful analytical simulator developed by SGS-THOMSON Microelectronics.

This simulator, whose models have been built considering physical structure and layout parameters, allows the optimisation of the most important device characteristics and also takes into account the possible parameter spread due to the process. For this reason the program output can give not only the average values of required parameters but also their statistical distribution.

1. INTRODUCTION

The modelling of power MOSFETs, in spite of the contributions from numerous authors, still exhibits some points to be improved. From the user point of view the choice of the model topology is determined by the degree of accuracy the results require, the computation time, convergence problems and the robustness and simplicity of the parameter extraction method.

One of the weak points of the actual models is due to drain-gate capacitance modelling which complicates the switching behaviour because of its high degree of non-linearity. But leaving apart this drawback which can be mitigated at the cost of increasing model complexity, (and thus computation time), the usefulness of model accuracy has often

been limited by the lack of robustness of the parameter extraction method employed. The aim of this paper is to give a contribution to solving this weak point.

The parameter extraction is usually performed by elaboration of experimental measurements, but some parameters are not directly measurable and others are not related to the physics of the device but are simply fit parameters to model the device as close as possible to reality. This paper shows a different way to tackle the problem which employs a new powerful package, COSMOS, entirely developed in-house by SGS-THOMSON Microelectronics. A number of analytical models have been developed to allow the extraction of parameters tied to the elements of the sub-circuit to be very fast and rugged. In the same way this package allows extraction of the worst case parameters because it also takes into account manufacturing tolerances.

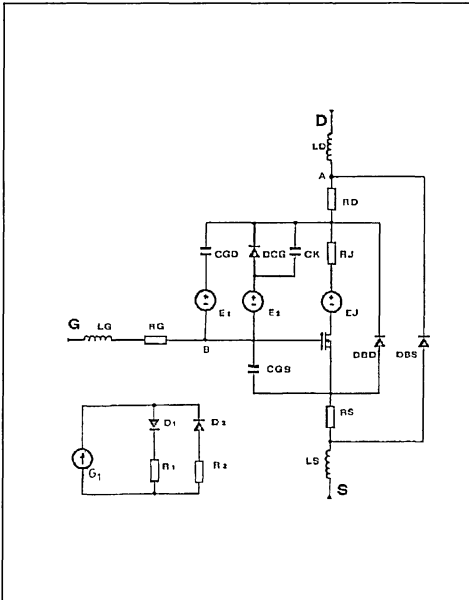
2. SGS-THOMSON SPICE MODEL OF POWER MOSFET

Figure 1 illustrates the components of the sub-circuit model. A Spice MOSFET model is the main switching element in the circuit. The other elements take into account the stray inductances due to the wires (L_s , L_d , L_g), the poly-silicon gate resistance (R_g), the resistance due both to silicon and to bonding (R_s , R_d), the body-drain capacitance modulation (DBD) and the leakage current when the device is in breakdown.

Two points need a more detailed explanation:

- the additional voltage dependent series drain resistance (R_s , E_s) is used in order to model the extra resistance of the epitaxial layer and substrate due to the depletion modulation of body-drain junction by the drain-source voltage and not accounted for in the ideal MOSFET model;
- the high non-linearity of the gate-drain capacitance is typical of a MOS structure switching from being strongly inverted to the accumulation state. The only difference is due

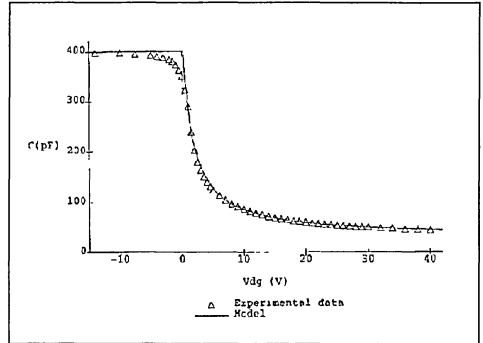
Figure 1. Sub-circuit SPICE model for Power MOSFET



to the fact that modulation of the depletion zone is caused not only by the voltage but also by lateral injection of the charge coming from the channel. This behaviour has been modelled by making the drain-gate and gate-source capacitances of the ideal MOSFET negligible by setting to zero the length of the overlapping regions between the gate and the other two elements.

These capacitances have been replaced by a constant gate-source capacitance, C_{GS} , and a two-element gate-drain capacitance, C_{GD} . Figure 2 shows an experimental CV diagram and its simulation obtained by the model described above. When the drain-gate voltage is positive, i.e. $V(a) - V(b) > 0$, then the leg containing the diode DD is activated and C_{GD} is modelled by the diode depletion capacitance. The insertion of a capacitance, C_K , in parallel with this diode gives not only a better fitting of C_{GD} for high values of drain- source voltages but also improves the simulation for low values of V_{DS} . When the drain-gate voltage is negative the C_{GD} capacitance is modelled disabling this leg and activating the other one.

Figure 2. C_{ISS} modelling



3. COSMOS: AN ANALYTICAL SIMULATOR FOR POWER MOSFET

COSMOS was born as a tool to optimise the Power MOSFET design. It is becoming more and more difficult to do this because of increasing demands of users to improve performance and of the large number of variables involved which interact with each other.

This software package provides some tools to match the most important device characteristics (R_{on} , BV_{DSS} , Capacitances, V_{th} , Gate-charge etc.) with the demands made and the netlist and the model parameters (average value and worst case) for the SPICE sub-circuit.

3.1 Program structure

The schematic is shown in figure 3. The statistical data for manufacturing processes and device design (figure 4) collected in a data base are processed by the analytical models of COSMOS which performs various analyses.

3.1.1 Sensitivity Analysis

This option allows the evaluation of the influence of a single layout or process parameter on the desired characteristic of the device (e.g. R_{on} , BV_{DSS} , C_{ISS} , C_{OSS} , C_{ISS} , gate-charge, etc.).

3.1.2 Statistical Analysis

The statistical input data allows COSMOS to output not only the average value of the required response but also its statistical distribution. The average value is also given divided into its various components to make optimisation of the device easier. Figure 5 shows an example referred to R_{on} and figure 6 to intrinsic capacitances.

Figure 3. COSMOS structure

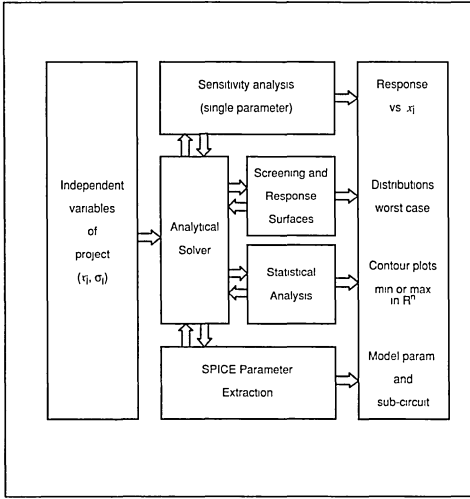


Figure 5. COSMOS outputs, R_{on} example:
a) Average values
b) Descriptive statistics

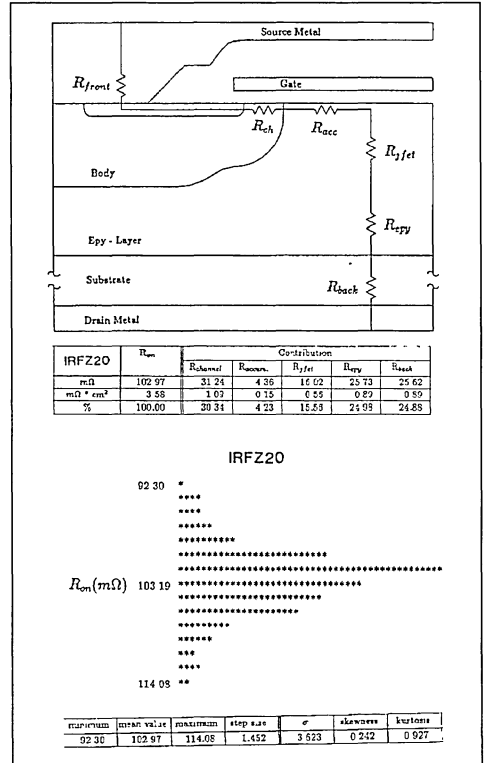
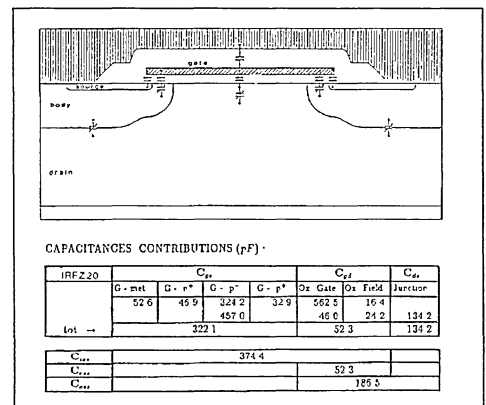


Figure 4. Layout and process parameters

Parameter	
1	Cell dimension
2	Cell spacing
3	Gate-drain area related to gate oxide
4	Gate-drain area related to field oxide
5	Gate-p ⁺ area related to gate oxide
6	Gate-p ⁺ area related to field oxide
7	Gate-Source metal area
8	Deep Body area
9	Channel width measured on poly mask

Parameter	
1	Gate oxide thickness
2	Field oxide thickness
3	P-Vapox Thickness
4	Oxide charge (Q _o + Q _{ss})
5	Channel length
6	Channel doping (peak)
7	Epy layer doping
8	Epy layer width
9	Cs deep body
10	X _j deep body

Figure 6. COSMOS output - capacitances



3.1.3 Screening and Response Surfaces.

It is possible to screen between the most important variables influencing the requested response (figure 7) and to obtain the response surfaces related to the simultaneous variation of two or more input factors (figure 8).

3.1.4 Spice Parameters Extraction

This option, which is discussed in more detail later, allows the extraction of the values of the elements of the SPICE sub-circuit model.

3.2 Models

The COSMOS models are derived from the classical ones [1][2][3], but they have been improved taking into account some effects that can not be disregarded due to the most recent technology.

3.2.1 R_{on}

The lateral depletion of the body, due to the built-in voltage and to V_{DS} , which leads to a reduction of the region available for the current flow, now must be considered not only for high voltage devices but also for the low voltage ones. The increased packing density makes this depletion significant with respect to the dimensions of the bodies thus resulting in a magnification of the JFET effect. Moreover, the extremely low values of $R_{on} \times Area$ in new High Density devices requires that the model considers not only the silicon contribution but also those due to metallization.

Other effects such as the mobility variation caused

by surface scattering and electric fields [4][5] and the influence of doping non-uniformity in the channel [2] are also considered.

3.2.2 BV_{DSS}

In a power MOSFET both breakdown voltage and R_{on} optimisation are directly related. They depend on doping (N_d) and epitaxial layer thickness (W_d) which act on BV and R_{on} optimisation in opposite ways. The problem is finding the pair, N_d , W_d , that minimise R_{on} at a fixed BV_{DSS} . The latter is computed taking into account the body doping profile, the eventual reach-through condition and the efficiency of the edge termination employed. The graphics tools of the program make this search for optimum conditions easier: in fact we can obtain BV and R_{on} maps (vs. N_d , W_d) and the N_d and W_d level lines in a BV - R_{on} coordinate system.

3.2.3 Capacitance

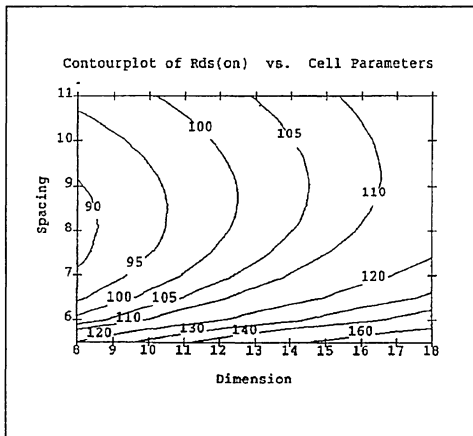
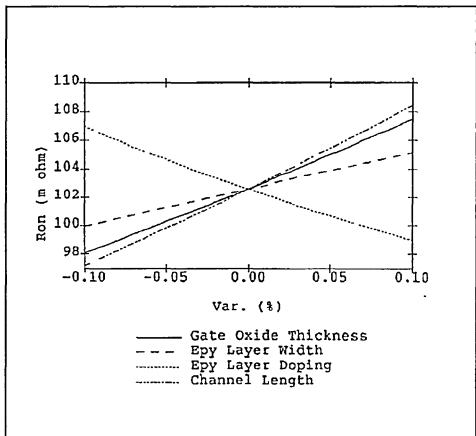
The models of the intrinsic capacitances of a Power MOSFET have been developed taking into account not only the doping non-uniformity but also the influence of the charge associated with the body lateral depletion.

4. COSMOS AS SPICE PREPROCESSOR

The modern design of electronic devices means that the mark must be hit with the first shot to minimise costs in terms of time and money. This can be achieved only by having a set of powerful simulators that make sure that the manufacturing of the first device is very close to the target. COSMOS, figure

Figure 8. COSMOS output - response surface example

Figure 7. COSMOS output - screening example



9, is placed between the process simulator (e.g. SUPREM, SUPRA) and the circuit simulator (e.g. SPICE) allowing the device optimisation to match the characteristics requested in the specific application.

4.1 Generation of statistical distribution of parameters and worst case extraction.

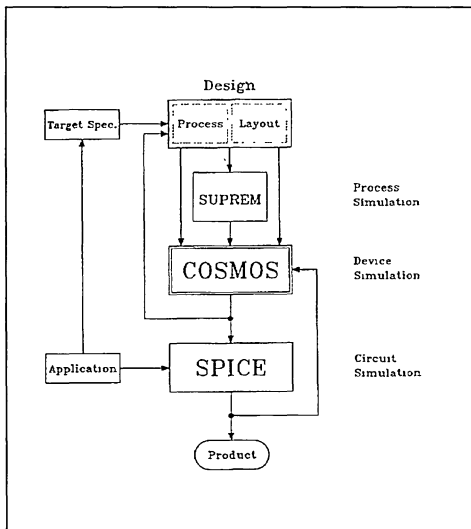
Starting from the distribution of the experimental data of process variables and from the design tolerances, the inherent speed of the analytical method allows the production of a random and statistically relevant set of input variables, using a Box-Muller transformation [6].

This set in turn, is used to generate the distribution of the desired output responses. This is possible also for the parameters of the sub-circuit model for SPICE. The MODEL cards related to typical values and to worst cases are generated taking into account the mean and the boundary values of the distributions above discussed. A typical output file is shown in appendix A.

CONCLUSION

The implementation of analytical models validated by a 2-D numerical simulator [5] is a powerful tool for studying device performance and optimisation. COSMOS allows a very fast computation of the

Figure 9. Total CAD approach to Power MOSFET design



influence of one or more parameters of the final characteristics of the device. Moreover it gives the average and worst case models for SPICE allowing the device designer to have fast feedback thus reducing the time needed for designing.

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APPLICATION NOTE

APPENDIX A. TYPICAL SPICE OUTPUT FILE

* Sub-circuit for IRFZ20

```
*
*.SUBCKT PWRMOS 1 2 3
*
LG 2 4 0.7500E-08
LS 12 3 0.7500E-08
LD 6 1 0.4500E-08
*
RG 4 5 0.1000E+02
RS 9 12 0.4000E-02
RD 7 6 0.5017E-01
RJ 8 7 0.2071E-01
*
CGS 5 9 0.1430E-09
CGD 7 10 0.5023E-09
*
CK 11 7 0.0000E+00
DGD 11 7 DGD
*
DBS 12 6 DBS
DBD 9 7 DBD
*
MOS 13 5 9 9 MOS L=0.1800E-05 W=0.4593
*
E1 10 5 101 0 1
E2 11 5 102 0 1
*
EJ 8 13 POLY(2) 6 8 6 12 0 0 0 0.03
*
G1 0 100 7 5 1.0E-06
D1100 101 DID
D2 102 100 DID
R1 101 0 1.0E+06
R2 102 0 1.0E+06
*
.ENDS PWRMOS
```

Models for IRFZ20

```
*
MODEL MOS NMOS
```

```
*
+ LEVEL = 3
+ TOX = 0.8500E-07
+ VTO = 3.134
+ PHI = 0.821
+ NSUB = 0.1150E+18
+ IS = 0.0000E+00
```

```
+ JS = 0.0000E+00
+ KAPPA = 0.180
+ UO = 491.335
+ THETA = 0.020
*
*.MODEL DGD D
*
+ IS = 0.0000E+00
+ CJO = 0.3980E-09
+ VJ = 1.060
+ M = 0.630
*
*.MODEL DBD D
*
+ IS = 0.0000E+00
+ CJO = 0.5100E-09
+ VJ = 0.670
+ M = 0.380
*
*.MODEL DBS D
*
+ IS = 0.1950E-II
+ BV = 72.10
+ N = 1.10
+ TT = 0.1250E-07
+ RS = 0.2275E-01
*
*.MODEL DID D
*
+ IS = 0.2000E-11
+ RS = 0.0000E+00
*
- End Models -
```



GATE CHARGE CHARACTERISTICS LEAD TO EASY DRIVE DESIGN FOR POWER MOSFET CIRCUITS

by M. Melito, F. Portuese

ABSTRACT

The traditional method of specifying input impedance for power MOSFETs is not incorrect, but it is incomplete and often leads to confusion when it is used as a design tool. An alternative method is to use the gate charge curve, which is directly related to the total input impedance and allows a simple evaluation of the drive energy and the switching performance to be made. This paper deals firstly with an analysis of the gate-charge waveform which is related to the device physics and develops an analytical expression, which gives a very good

approximation of the total gate-charge. Secondly, the influence of the electrical parameters, both external to the device (e.g. I_D , V_{DD}) and the internal ones (V_{th} , g_{fs} , C_{iss} , C_{oss} , C_{rss} , cell density) are analysed. The paper also highlights how it is possible to extrapolate the actual dynamic behaviour of the device easily from this curve. Finally, an evaluation criterion is suggested that allows a comparison to be made between the actual performances, both static and dynamic, of devices with similar nominal characteristics.

GATE CHARGE MEASUREMENT

During the switching of a POWER MOSFET, the gate current has the typical behaviour of current in an RC circuit, see figure 1. The transient lasts for some tens of nanoseconds or more, due essentially to the RC time constant and the maximum current available in the driving circuit. If the current in the gate, I_{G} , is constant and small enough, the switching time can be increased to a level where the voltage and the current waveforms are free from the parasitic effects caused by the stray

inductances that are usually associated with high frequency power switching. In this way it is possible to isolate the influence of the external factors and analyse only the internal parameters. The test circuit and the related waveforms are shown in figure 2.

GATE-CHARGE CURVE ANALYSIS

To get a better understanding of the phenomena which occur during switching it is useful to refer to the model of the POWER MOSFET shown in figure 3b. The figure 3a shows the cross section of a single cell illustrating the parasitic capacitances. The gate-charge waveform is strictly related to the modulation of the gate-source equivalent capacitances during switching. This is due to the variation of the intrinsic capacitance of the device with gate and/or drain voltage. Figure 4 shows the load line and C_{gs} , C_{gd} variation during each phase of switching. Figure 5 shows a typical gate-charge curve: the capacitances influencing the shape and the length of each zone are marked.

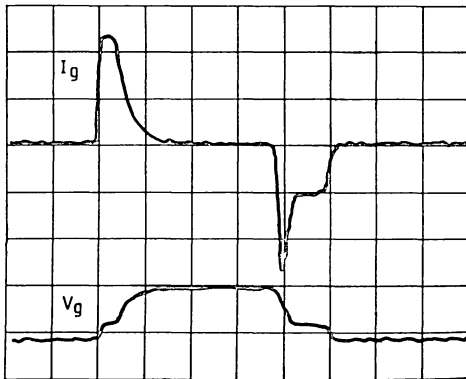


Fig. 1 - I_g , V_{gs} waveforms

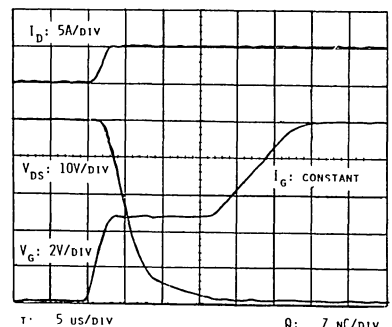
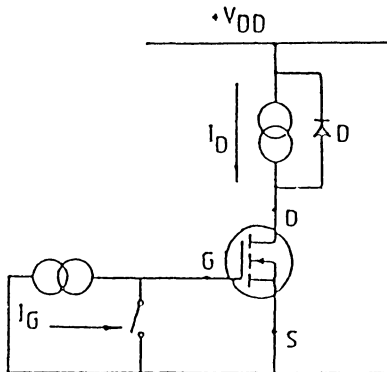
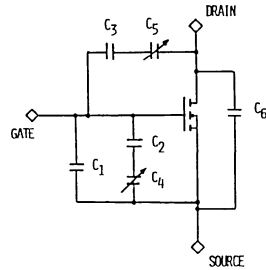
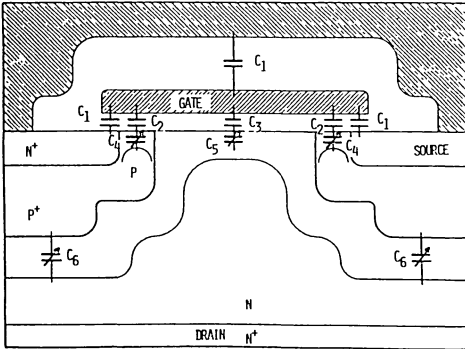


Fig. 2 - Test circuit and related waveforms.



- C₁: Capacitance between gate and source (both N^o and metal)
- C₂: Capacitance between gate and P zone.
- C₃: Capacitance between gate and epi N.
- C₄: Capacitance of the depletion zone in the superficial epi.
- C₅: Capacitance of the depletion zone in the superficial epi.
- C₆: Capacitance of the body-drain junction.

Fig. 3 - Cross section of a Power MOSFET cell and its electrical equivalent.

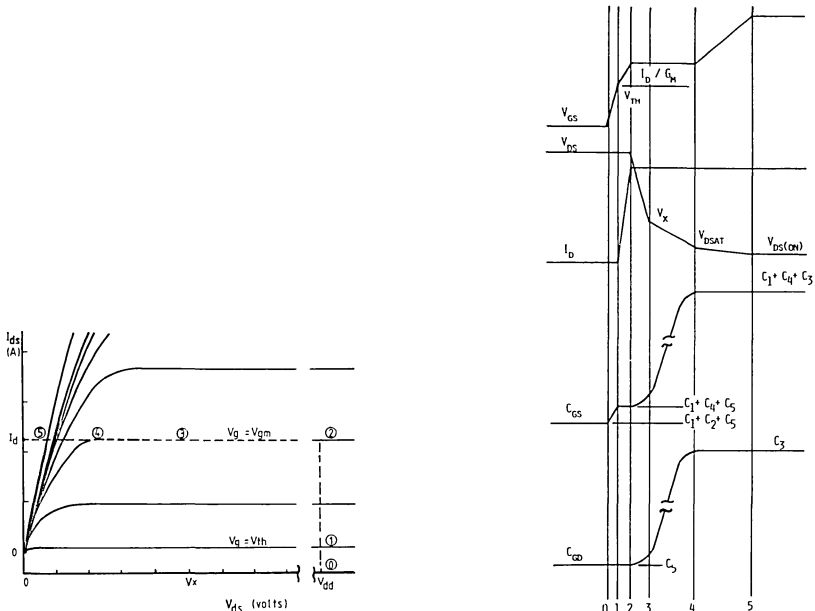


Fig. 4 - Load line and capacitances modulation.

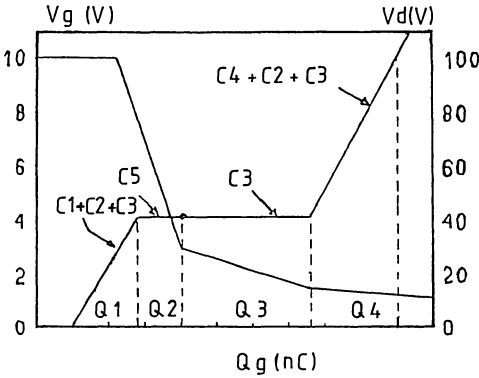


Fig. 5 - Gate charge curve

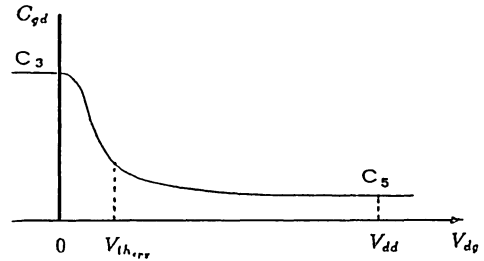


Fig. 6 - C_{gd} modulation

In the first zone the equivalent capacitance is nearly equal to C_{iss} because V_d is constant and the variation of V_g has no influence. The charge supplied to the gate can be approximated by the expression :

$$Q_1 = (C_1 + C_2 + C_5) \cdot V_{gm} = C_{iss} \cdot V_{gm}$$

where V_{gm} is the gate to source voltage required to just carry the desired I_d and it can be easily deduced using the output characteristic. In the horizontal zone the equivalent capacitance seems to be infinite, in fact V_{gs} remains constant though charge is supplied to the gate. This phenomenon, known as the Miller effect, is due to the modulation of the capacitance C_{gd} by V_{ds} . The waveform of this capacitance variation is typical of a MOS structure switching from being strongly inverted to the accumulation status, see figure 6.

The only difference is due to the fact that modulation of the depletion zone is caused not only by the voltage but also by lateral injection of the charge coming from the channel.

Looking at the drain voltage, figure 4 and figure 5, a slope variation can be observed occurring at a voltage, V_x , physically corresponding to the transition from a highly charged P zone to simple depletion of the MOSFET capacitor that exists between the deep body cells. The first slope is related to $C_5 \approx C_{rss}$, the second to C_3 , the polarity of V_{gd} being so that $C_5 \gg C_3$. So the charge supplied to the gate during the Miller effect can be split into two parts:

$$Q_2 = C_5 \cdot (V_{dd} - V_x) \approx C_{rss} \cdot (V_{dd} - V_x)$$

$$Q_3 = C_3 \cdot (V_x - V_{d(sat)})$$

being $V_x = V_{gm} + V_{th-epy} + R_{epy} \cdot I_d$ and $V_{d(sat)}$ the voltage drain corresponding to the "knee" of the output characteristic with $V_{gs} = V_{gm}$. The slope of the final part is associated with the oxide capacitances. (V_{th-epy} is the threshold voltage of the MOSFET capacitor existing between the P zone; R_{epy} is the resistance of the drain due to the epi). The charge supplied during this phase is:

$$Q_4 = (C_1 + C_2 + C_3) \cdot (V_{g(max)} - V_{gm})$$

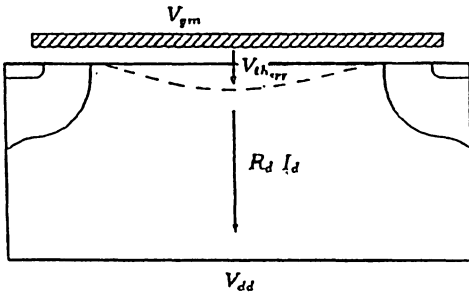


Fig. 7 - V_x evaluation.

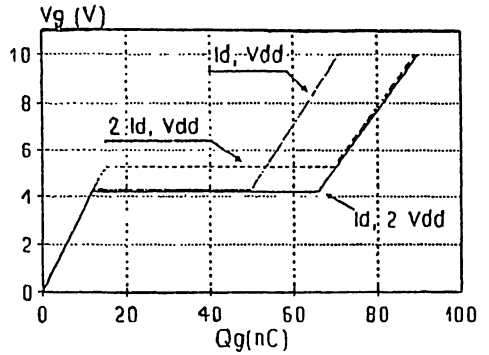


Fig. 8 - Gate charge curves as a function of I_d and V_{dd} .

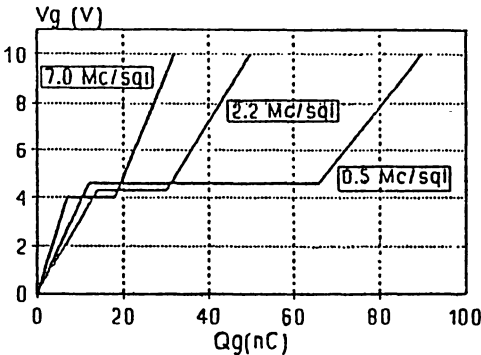


Fig. 9 - Influence of cell density on gate charge.

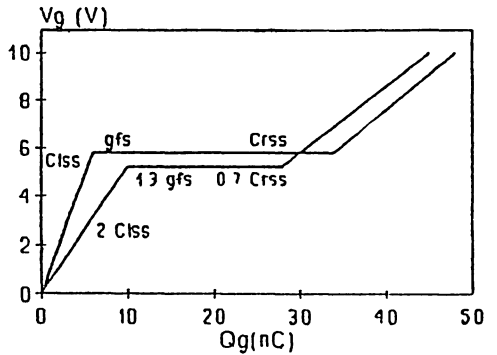


Fig 10 - Comparison of gate charge curves of two devices with different values of C_{iss} , g_{fs} and C_{rss} .

EFFECTS OF THE PHYSICAL AND ELECTRICAL PARAMETERS ON THE GATE-CHARGE CURVE

The previous discussion has shown that the total charge supplied to the gate is influenced by several parameters, which are essentially:

- a) electrical parameters (V_{dd} , I_d)
- b) structural parameters (cell density, capacitances, V_{th} , g_{fs})

The electrical parameters are imposed by the external circuit and depend on the application; the structural parameters are typical of the

device and can be adjusted during the device design stage in order to optimise its performance. Figure 8 shows the influence of I_d and V_{dd} on the shape of the gate-charge curve.

Figure 9 summarizes the effects of the structural parameters: the gate-charge curves of devices having the same static characteristics ($R_{ds(on)}$, BV_{dss} , I_d) and different

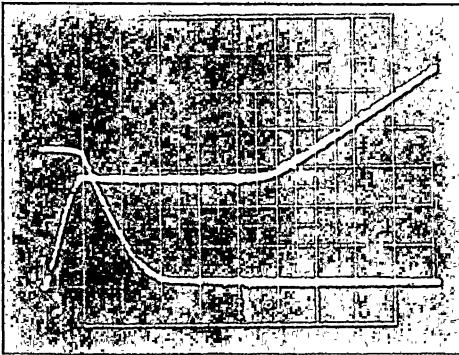


Fig. 11 - Gate charge curve of STP5N50.
 $V_{gs} = 2V/div$, $V_d = 100V/div$,
 $Q_g = 5nC/div$.

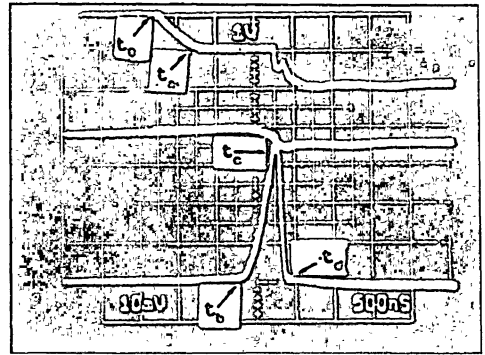


Fig. 12 - STP5N50 turn-off. $V_{gs} = 5V/div$, $V_d = 100V/div$,
 $I_d = 1A/div$, $t = 500ns/div$, $R_g = 180$
 Ohms.

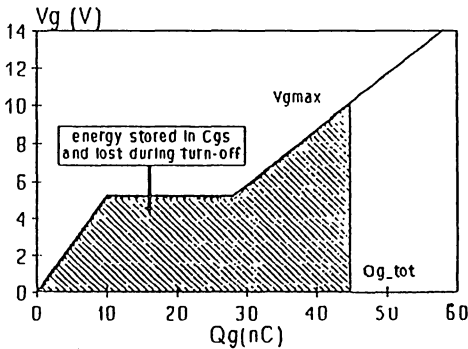


Fig. 13 - Driving energy and gate charge.

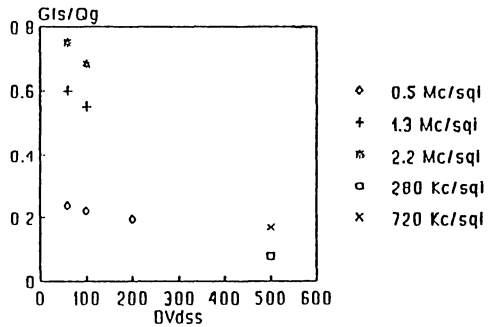


Fig. 14 - Comparison of technologies.

cell densities, are shown. Figure 10 shows the influence of the capacitances and of the transconductance on the same curve.

Use of the gate-charge curve

The gate-charge curve analysis is useful for obtaining important information about device switching characteristics. The following example evaluates the switching time of the SGS-THOMSON STP5N50 as an example.

Figure 11 and figure 12 show, respectively, the gate charge curve and the turn-off of the IRF832 measured under similar conditions of I_d and V_{dd} . Note that the horizontal axes of the gate-charge graph are in nanocoulombs ($Q = I_g \cdot t$, $I_g = \text{const.}$) while the vertical axes are in volts. Referring to figure 5 and figure 11, the values of the single contribution to gate charge are:

$$Q_1 = 5 \text{ nC}$$

$$Q_2 = 11 \text{ nC}$$

$$Q_3 = 13 \text{ nC}$$

$$Q_4 = 18 \text{ nC}$$

During t_a , C_{gs} is constant so this time is easy to evaluate using the usual calculation for RC circuits:

$$t_a = R_g \cdot C_{gs} \cdot \ln(V_{gs}(t_0)/V_{gs}(t_a))$$

substituting:

$$R_{gs} = 180,$$

$$C_{gs} = dQ/dV = 18\text{nC} / 4.7\text{V} = 3829\text{pF},$$

$$V_{gs}(t_0) = 10\text{V}, V_{gs}(t_a) = 5.3\text{V}$$

$$t_a = 438\text{ns}.$$

From t_a to t_c , I_g is constant and its value is $I_g = V_{gm} / R_{gs} = 29.4\text{mA}$ hence:

$$t_b = Q_3 / I_g = 442 \text{ ns}$$

$$t_c = Q_2 / I_g = 374 \text{ ns}$$

During t_d C_{gd} is constant and using the previous expression :

$$t_d = R_g \cdot C_{gs} \cdot \ln(V_{gs}(t_c)/V_{gs}(t_h)) = 96\text{ns}$$

$$\text{Note } C_{gs} = C_{iss}$$

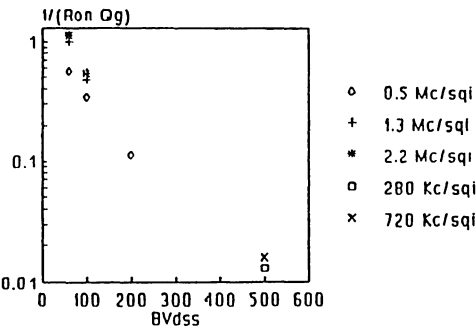


Fig. 15 - Comparison of technologies.

Looking at figure 12 it is possible to see that the calculated times are very close to the measured ones.

The gate charge curve is also helpful because it allows the driving energy to be calculated. The area under the gate-charge curve represents, in fact, the total amount of energy needed to turn-on the device while $V_{gmax} \cdot Q_{g-tot}$ is the total energy that the driving circuit has to supply, see figure 13.

In order to obtain fast switching with low driving energy and low energy dissipation during the cross-over, the optimum device should have low Q_g and high g_{fs} . To obtain low power dissipation during the on state, the optimum device should have low R_{dson} .

It is useful to define two merit coefficients to give a measure of device performance:

$$K_1 = g_{fs}/Q_g \quad K_2 = (R_{ds(on)} \cdot Q_g)^{-1}$$

Devices having analogous nominal characteristics (BV_{dss} , I_d) but manufactured using different technologies can be quickly compared, see figure 14 and figure 15. Note that the two coefficients are not dependent on device die size because of their definition. They both depend on switching features (Q_g) but K_1 is related to the saturation zone (g_{fs}) of the Power MOSFET out characteristics whilst K_2 is related to the linear characteristic (R_{on}).

CONCLUSION

The gate charge curve supplies useful information about the actual behaviour when the device switches. From the user's point of view, these curves allow the correct design of the drive circuit and correct choice of the device which best satisfies the design criteria. The use of two merit coefficients allows a quick comparison of devices having similar

nominal characteristics but manufactured using different technologies.

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SEMICONDUCTOR DEVICES
IGBTs



AN INTRODUCTION TO IGBTs

by M. Melito, A. Galluzzo

INTRODUCTION

In the low and medium power range, Bipolar Junction Transistors (BJTs) have up to now been the most commonly used power semiconductors, and they still hold a large part of the market, despite some limitations due in part to the current drive (which can be uneconomic in terms of the number of components and the dimensions of the resulting circuits), and also the fact that minority carrier conduction places a limit on the maximum frequency of use.

The introduction of Power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices allowed much simpler voltage drives to be used, and made operation at much higher frequencies possible, as conduction occurs with majority carriers. The use of this device has grown rapidly in low voltage

applications, but the dissipation characteristics in conduction have limited its use in high voltage.

IGBTs (Insulated Gate Bipolar Transistors) are a newer class of high voltage devices which combine the simplicity of drive of the MOS structure with the ability to handle high values of current typical of a bipolar device.

This paper includes a brief description of the structure and the physics of the device, followed by an analysis of the principal static and dynamic characteristics. Aspects of the device which must be considered to obtain maximum performance are also discussed, in particular the robustness in forward bias, reverse bias and short circuit, and the influence of gate polarisation.

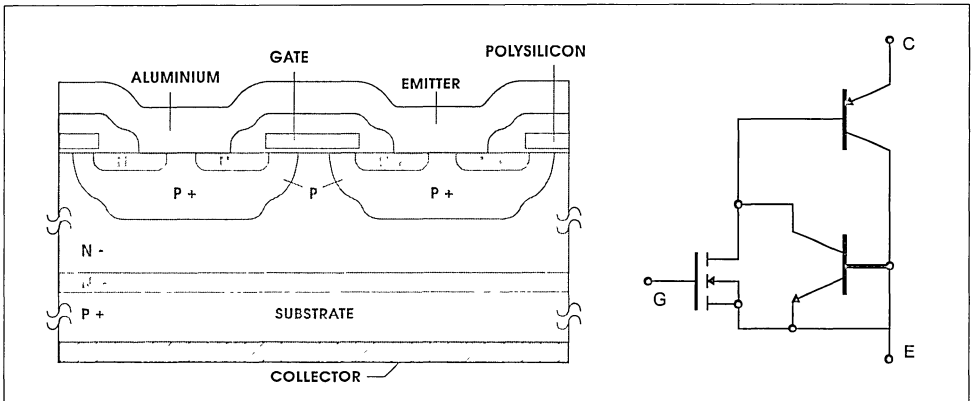
1 IGBT STRUCTURE

The IGBT is a natural evolution of the vertical Power MOSFET for high current, high voltage applications. It eliminates the main disadvantage of current high voltage Power MOSFETs, which is the high value of $R_{DS(on)}$ caused by the high resistivity of the source-drain path necessary to obtain a high breakdown voltage BV_{DSS} . The lower $V_{CE(sat)}$ which can be obtained with IGBTs allows operation with a current density much higher than that which can be achieved with bipolar devices; alternatively, under the same conditions, the $V_{CE(sat)}$ of the IGBT is lower. The vertical section shown in figure 1 together with the equivalent circuit shows

that the structure of the IGBT is very similar to that of a Power MOSFET. The fundamental difference is in the addition of a p^+ type substrate. In this way a junction is created with the n^- area of the collector; such a junction injects holes into the n^- area during conduction, modulating the resistance and significantly reducing the $V_{CE(sat)}$ of the device.

When the device is blocked there is no injection of holes and consequent modulation of resistance, and so the breakdown voltage of the IGBT depends only on the doping and the thickness of the n^- region.

Figure 1: IGBT Basic Structure



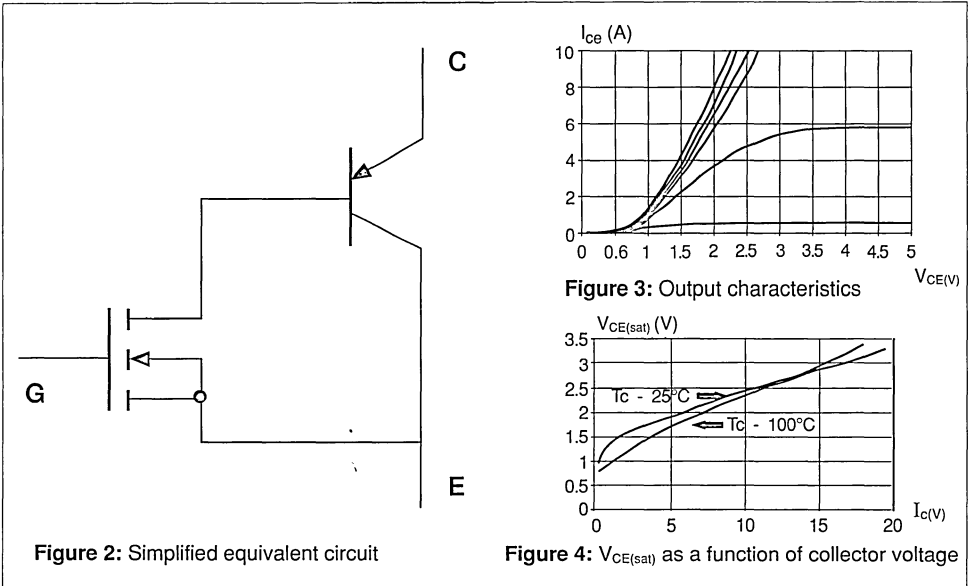
2 STATIC CHARACTERISTICS

The IGBT can be modelled, as a first approximation, as a pnp transistor driven by a Power MOSFET. Figure 2 shows only the elements of the structure necessary for the understanding of the operation of the device; ignoring, for the moment, the parasitic elements. The output characteristics of the IGBT are shown in figure 3, and it can be seen that they are very similar to those of a Darlington type bipolar device.

2.1 Temperature dependence

As the IGBT structure includes both a bipolar and a Power MOSFET, its temperature characteristics depend on the net effect of the two components, which have contrasting properties. The Power MOSFET has a positive temperature coefficient, while that of the bipolar is negative. Figure 4 shows the change in $V_{CE(sat)}$ as a function of the collector current for two different values of junction temperature.

Figures : 2,3 & 4



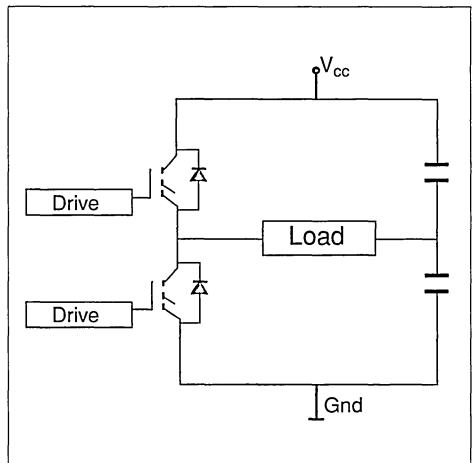
3 DYNAMIC CHARACTERISTICS

The equivalent circuit of the input of the IGBT is of a MOSFET type and so is purely capacitive. This allows the use of voltage drive which means that it is possible to have a less complex circuit with lower power consumption than that required by a bipolar device.

3.1 Gate Polarisation Voltage and Drive Resistance

The gate drive voltage generally adopted is 15V both to obtain a saturation voltage large enough to have negligible conduction losses, and because the information provided in data sheets refers to such a value which has almost become a standard. In some circuit configurations, for example the half bridge shown in figure 5, the increased value of dV/dt generated by the turn off of one of the devices can cause the accidental turn on of the other. A high value of dV/dt applied between the collector and the emitter can cause, due to the collector-gate capacitance

Figure 5: Half Bridge circuit

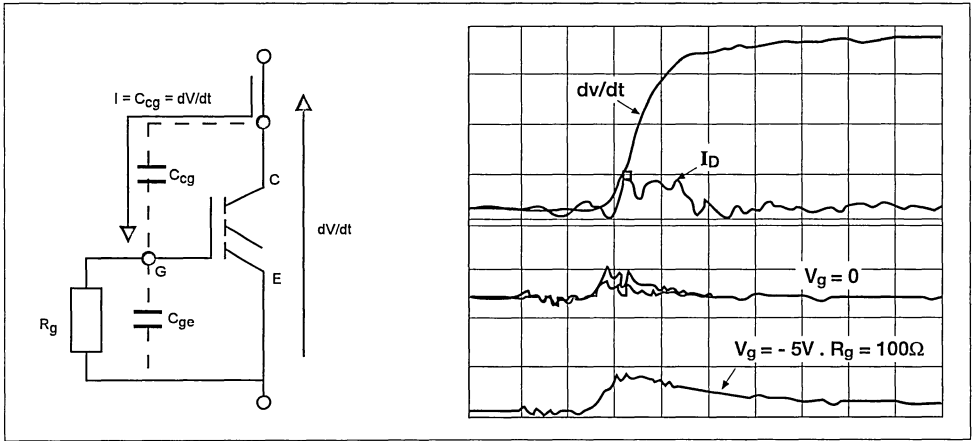


(C_{res}) and the impedance of the drive circuit (R_g, C_{ies}), the turn on of the device at high currents and voltages. Such undesirable behaviour is not generally destructive, but can cause large power dissipation. To

prevent this problem arising the MOSFET should be driven with a negative offset (typically 5V is sufficient) and with the lowest drive impedance possible compatible with

the demands of the RBSOA (which will be discussed later). Figure 6 shows waveforms demonstrating the effect of dV/dt , along with the relevant equivalent circuit.

Figure 6: Effect of dV/dt



3.2 Turn on

The turn on behaviour of the IGBT is identical to that of the Power MOSFET, and the turn on time is a function of the output impedance of the drive circuit and the applied gate voltage. It is possible to control the turn on

speed of the device by choosing an appropriate value of gate resistance. Figure 7 shows waveforms for the switching of an inductive load, and the equivalent circuit.

Figure 7: Turn-on with inductive load

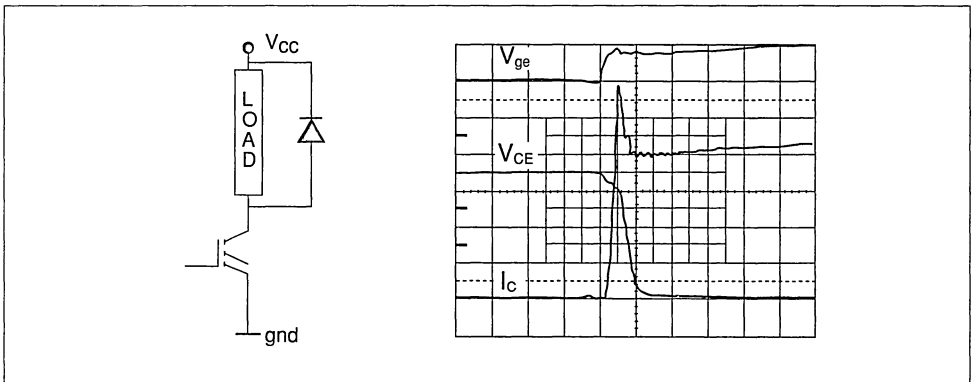


Figure 8 shows the variation of the current gradient with the value of the gate resistance for a typical device.

Turn on losses can be calculated using the following relationship:

$$E_{on} \approx 0.5 * V_{CC} * (I_O + I_{RM})^2 * (dl/dt)^{-1}$$

This is shown graphically in figure 9.

Figure 8: dl/dt as a function of drive resistance

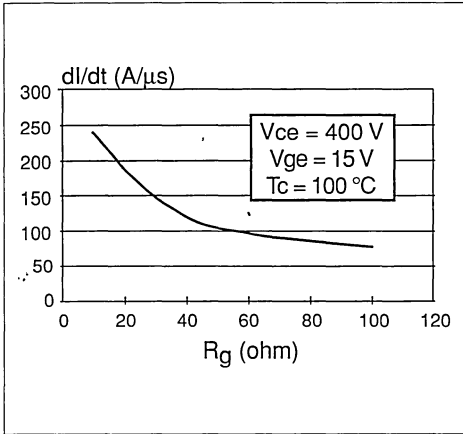
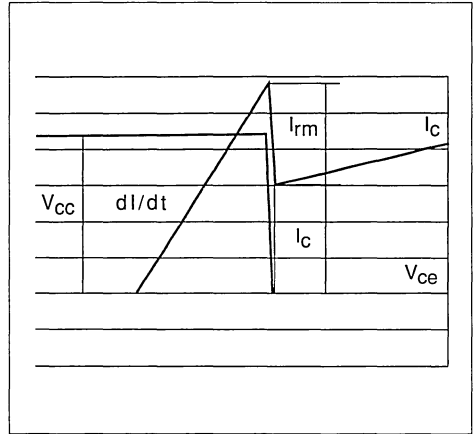


Figure 9: Calculation of energy dissipated in turn on of inductive load



3.3 Turn off

The turn off behaviour has typical characteristics of both Power MOSFET and BJT devices. The turn off waveform shown in figure 10 shows distinct phases.

During the first phase, the gate voltage decreases to a value at which the Miller effect begins and the V_{CE} starts to increase. In the second phase the gate voltage remains constant because of the modulation of the collector-gate capacitor by V_{CE} which continues to increase to its maximum value at a rate controlled by the drive circuit. The third phase, which defines t_{fall} , can be divided, with respect to the collector current, into two parts: the first, very fast and due to the turn off of the MOSFET part of the device; the second slower and caused by the recombination of the minority carriers that cannot be extracted from the base of the pnp bipolar section which is already open. The length of this "tail" depends essentially on the lifetime of these carriers.

Figure 10: Turn off with inductive load

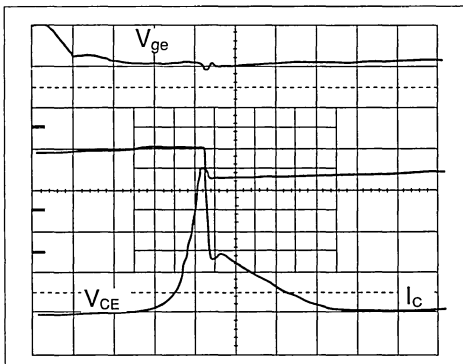
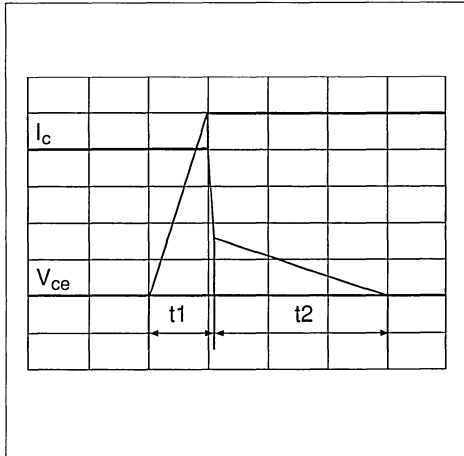


Figure 11 shows that the energy dissipated at turn off can be considered as being due the result of two elements: the first is tied to the speed at which the collector voltage reaches its maximum voltage; the second to the duration of the tail of the collector current.

Figure 11: Calculation of energy dissipated in turn-off of inductive load



In total:

$$E_{off} = 0.5 * (I_C * t_1 + I_{tail} * t_2) * V_{ce}$$

To minimise this energy, at a fixed I_C , V_{ce} and temperature it is only possible to affect t_1 . This parameter can be controlled via the gate resistor. The contribution of the tail, related to the value of I_{tail} and to its duration, depends strongly on the junction temperature and on the values of I_C and V_D . Figures 12-15 show, for a typical device, the variation in dV/dt as a function of R_g , and the variation of I_{tail} as a function of I_C , V_D and T_C .

Figure 12: dV/dt as a function of drive resistance

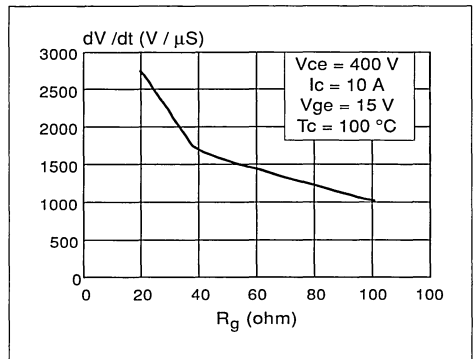


Figure 13: I_{tail} as a function of I_c

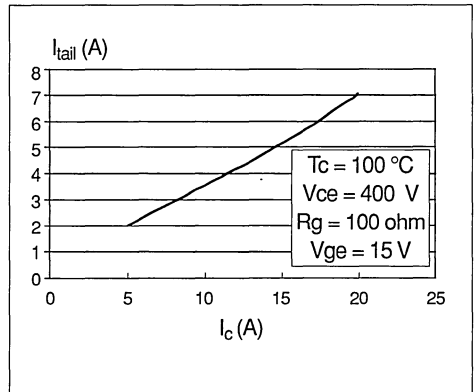


Figure 14: I_{tail} as a function of clamp voltage

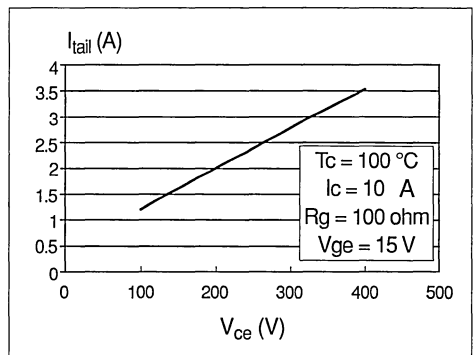
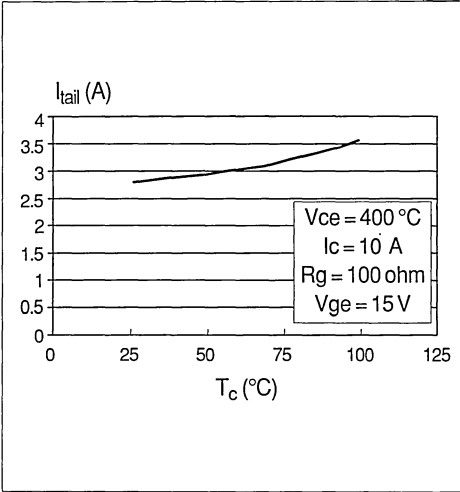


Figure 15: I_{tail} as a function of temperature



The total power dissipated in the device is:

$$P_d = (I_{(AV)} * E_O + I_{(RMS)}^2 * R) * \delta + (E_{on} + E_{off}) * f$$

$I_{(AV)}$ = Mean Current

$I_{(RMS)}$ = Effective Current

δ = Duty Cycle

R = Differential Resistance

f = frequency

This formula was used to calculate the continuous power dissipation in the approximation of the output characteristics shown in figure 16. Figure 17 shows the variation of switchable power with switching frequency, with the device held a constant voltage and the current adjusted such that the power dissipated by the device remains constant at 10W.

3.4 Maximum Operating Frequency

The dissipation of power during switching limits the maximum operating frequency of electronic switches. The junction temperature during normal operation depends on the amount of power dissipated from the device and on the efficiency of the cooling system:

$$T_j = T_{ambient} + P_d * R_{th(ja)}$$

The more efficient the heatsink on which the device is mounted, the lower the case temperature, the greater the temperature difference allowed between case and junction, and therefore the greater the power that can be dissipated. T_j should be maintained as low as possible with the smallest size, and hence cost, of heatsink possible. In practice it is acceptable to have, with a switchable power of 10kW, a maximum power of 10W dissipated in the device.

Figure 16: Approximation of output characteristics

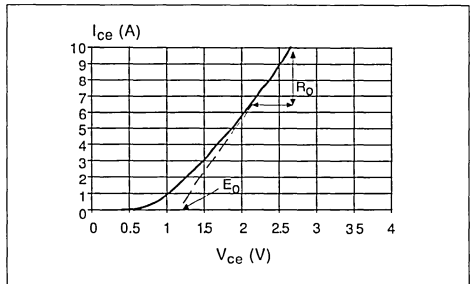
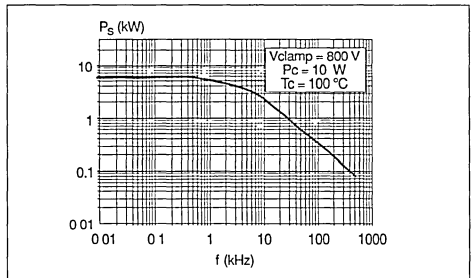


Figure 17: Switchable power at constant dissipated power



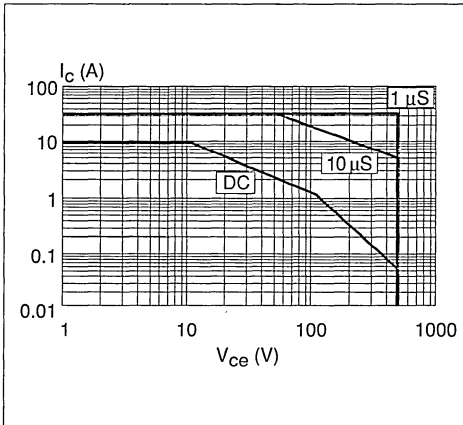
4 SAFE OPERATING AREA

A power device must have a safe operating area large enough in terms of switchable current and voltage and also to allow it to survive in anomalous conditions, for example short circuit, for a long enough time to allow protection circuits to take action. Typically the curves describing robustness in forward conduction (Forward Bias Safe Operating Area, FBSOA), in reverse (Reverse Bias Safe Operating Area, RBSOA), and in short circuit are available.

4.1 FBSOA

The forward conduction robustness characteristics of the IGBT are more similar to those of the Darlington than to those of a Power MOSFET. The FBSOA graph shown in figure 18 shows a variation in the gradient, which depends on an effect known as secondary breakdown which does not occur in the Power MOSFET.

Figure 18: FBSOA



4.2 RBSOA

In the equivalent circuit of the IGBT shown in figure 1 shows the presence of a parasitic

npn transistor. This transistor, together with the pnp, forms an SCR, which in certain conditions can trigger. When this occurs, the device can no longer be controlled via the gate. The latest IGBTs do not exhibit this type of behaviour, since with appropriate modifications to the structure and the process the triggering of this parasitic SCR can be made to occur at a current much higher than that encountered in normal operation (typically $I_{latch} > 5 * I_{nominal}$). Figures 19 and 20 show the variation in latch current as a function of junction temperature and gate resistance respectively.

Figure 19: I_{latch} as a function of junction temperature

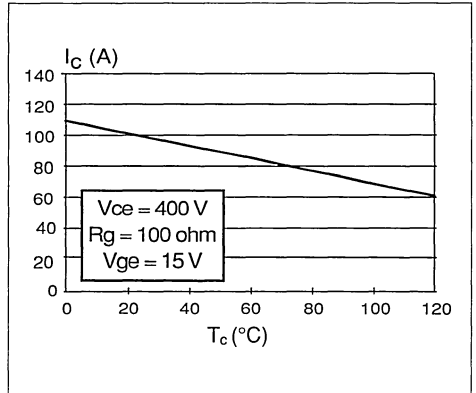
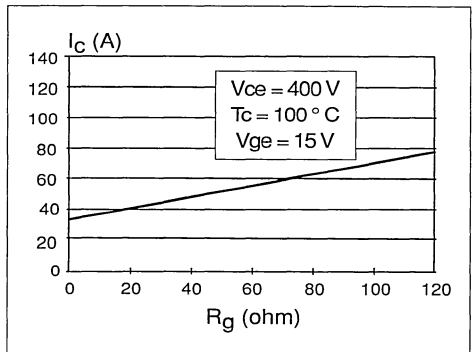


Figure 20: I_{latch} as a function of drive resistance

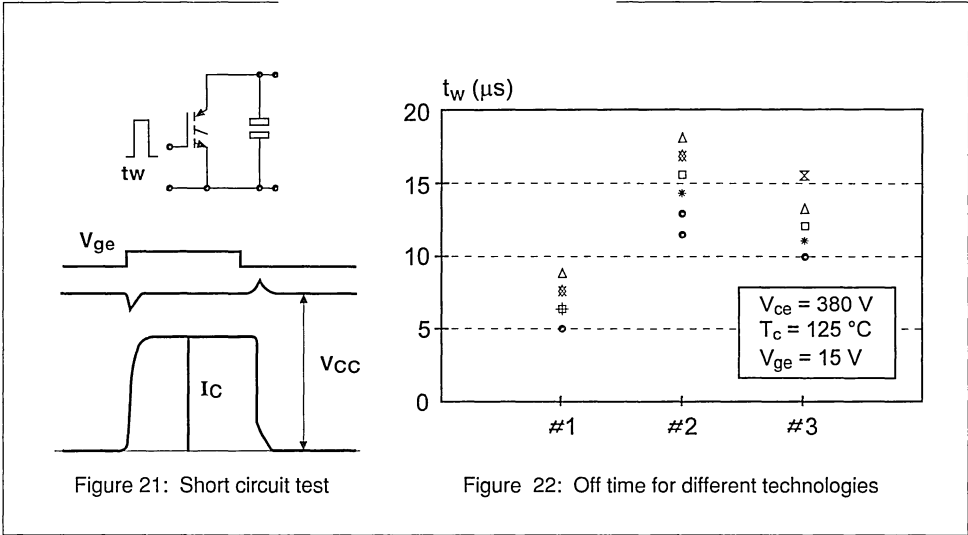


4.3 Short Circuit Robustness

This is measured by turning on the device at the supply voltage and measuring the maximum time during which the drive circuit can control the device under test. Figure 21

shows the shape of the waveform and figure 22 the off time for three devices with equivalent characteristics but manufactured using different technologies.

Figures : 21 and 22



5 FUTURE DEVELOPMENTS

The particular structure of the IGBT means that the turn off of the device is controlled by the turn off of the pnp bipolar which, in practice, turns off with an open base. For this reason the switching can only end after the recombination of the excess minority carriers in the base region of the pnp, which therefore dominate the turn off behaviour.

To increase the speed of the turn off characteristics of the device requires the adoption of techniques to reduce the minority carrier lifetime, through which the t_{fall} of the IGBT can be reduced to a time in the order of hundreds of nanoseconds.

The technique involves doping the device with gold or platinum, irradiation with electrons, or bombardment with heavy ions.

Changes can also be made at the structural level, for example the introduction of a buried n+ type layer, see figure 1, between the base and emitter of the pnp. This results in both an increase in the turn off speed, and an improvement in the robustness due to the decrease in the gain of the parasitic transistors. The optimisation of the above technique allows the best compromise between the conflicting demands of speed, current handling capability and robustness, eliminating the inconveniences of first generation IGBTs.

The latest generation IGBTs are at least twice as fast as the first, and the RBSOA is rectangular.



HOW SHORT CIRCUIT CAPABILITIES GOVERN THE DESIRED CHARACTERISTICS OF IGBTs

by C.G. Aniceto, R. Letor

ABSTRACT.

Short circuit tolerance of IGBTs can be obtained by the optimization of both the protection circuit and the intrinsic ruggedness of devices.

This note discusses application design criteria and IGBT characteristics compared to the intrinsic short circuit ruggedness.

1.0 INTRODUCTION.

The continuous growth of IGBT applications requires more differentiation of device electrical characteristics. In fact, the structure of IGBTs makes them flexible to use and their

switching performance can be specifically matched to many different applications.

For the best match between application requirements and IGBT characteristics, some compromise between the saturation voltage, switching speed and ruggedness is necessary.

To define the suitable IGBT short circuit ruggedness specification, this note analyzes the parameters influencing their behaviour during short circuit operation, and verifies the performance of the more usual short circuit protection compared to IGBT short

circuit ruggedness.

It is also shown that modification of the IGBT structure improves the short circuit performance without compromising the saturation voltage and switching speed.

2.0 SHORT CIRCUIT OPERATION OF IGBTs.

Static and dynamic characteristics are not sufficient to predict the short circuit behaviour of IGBTs. Also, dynamic phenomena correlated to stray parameters and to the short circuits circumstances must be carefully considered.

2.1 SHORT CIRCUIT MODES AND WAVEFORMS.

Real short circuit mode can be simulated using the test circuits "A" and "B" illustrated respectively in figure 1 and figure 5.

TEST CIRCUIT "A": The device is turned on when the collector is directly connected to

the supply voltage and the short circuit inductance can be changed. This circuit simulates either a short circuit in one leg of a bridge circuit, or a permanent short circuit of the load [4].

The waveforms of figure 2 show the behaviour in the test circuit "A" when all the stray parameters are reduced to a minimal value. The effect of a significant short circuit inductance is shown in figure 4. The inductance, the reverse capacitance " C_{RS} ", the gate capacitance " C_G ", R_G , together with the IGBT amplification, constitute a resonant R,L,C circuit as shown in figure 3. Hence di/dt at turn-on generates a very high peak current due to a gate voltage overshoot.

TEST CIRCUIT "B": The short circuit is activated during the on-state. In this case a dV/dt is applied to the collector when the gate voltage is high and the device is in full conduction. This condition simulates accidental short circuit of the load during normal operation [4].

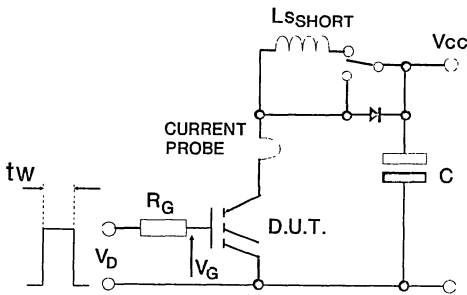


Fig. 1. Test circuit "A" $L_{SHORT} \approx 4\mu H$, $L_{STRAY} \approx 150nH$.

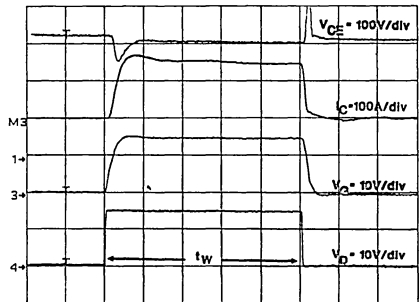


Fig. 2. Short circuit test with short circuit inductance = L_{STRAY} . Time scale: $2\mu s/div$.

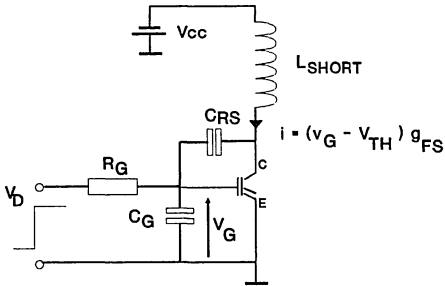


Fig. 3. Simplified equivalent circuit of the short circuit condition.

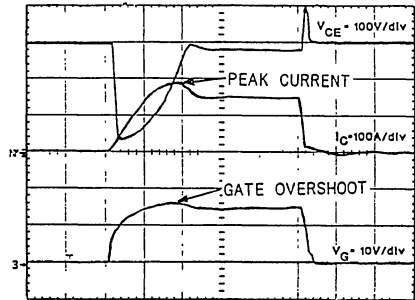


Fig. 4. Short circuit test with short circuit inductance = L_{SHORT} . Time scale = $2\mu s/div$.

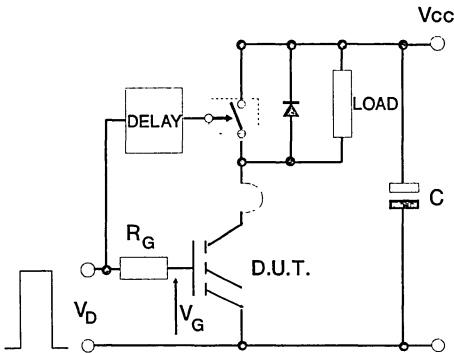


Fig. 5. Test circuit "B". Short during saturation.

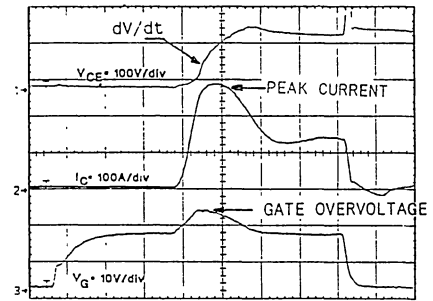


Fig. 6. Effect of the dV/dt when the short circuit occurs during IGBT full conduction. $t = 2\mu s/div$.

The waveforms of figure 6 show the effect of the dV/dt in the test circuit "B". The dV/dt acting through reverse capacitance causes the gate voltage to rise over the driving voltage [6]. A peak current much higher than short circuit current is generated.

2.2 SHORT CIRCUIT STRESSES.

The failure of IGBTs during short circuit condition occurs either with static latch or with dynamic latch of the parasitic SCR of the structure (figure 14) [2]:

- Static latch is due to the high current density.
- Dynamic latch is due to the high dV/dt at turn-off.

The influence of the temperature is critical because the latching current decreases when temperature increases. Moreover, during short circuit there is a very fast temperature rise due to the very high energy increase dissipated in the device.

For this, gate voltage overshoot must be avoided and the short circuit current must be reduced as much possible. In fact:

During overshoot, the collector current ($i_C = g_{FS} (v_g - V_{TH})$) can reach the static latching current, especially if the transconductance of the device is high.

At turn-off the junction temperature is higher than at turn-on, so the dV/dt due to the stray inductance " L_{sC} " can cause a dynamic latch-up.

Moreover, the stray inductance " L_{sC} " creates an overvoltage at turn-off (see figures 2,4,6) due to the di/dt . If the di/dt at turn-off is not controlled by a suitable gate resistance the overvoltage can reach breakdown causing device failure.

2.3 PARAMETERS INFLUENCING SHORT CIRCUIT BEHAVIOUR (figure 7).

The main parameters influencing static and dynamic short circuit behaviour are:

- Transconductance g_{FS} , C_G , C_{RS} (Device parameters)
- Driving voltage V_D , R_G (Driving circuit)

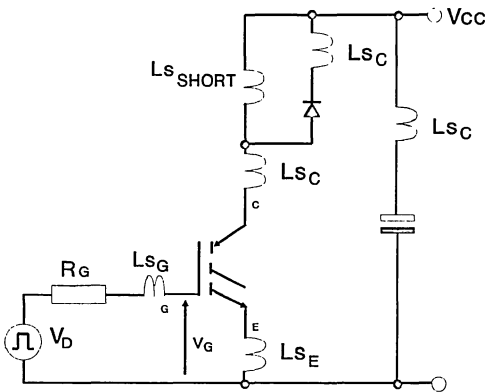


Fig. 7. Circuit parameters influencing short circuit current of the IGBTs.

- L_{sC} , L_{sE} (Stray inductance of lay-out and of capacitance)
- L_{sSHORT} , dV_{CE}/dt , V_{CE} (Short circuit conditions)

The stray inductances L_{sE} (emitter-ground) and L_{sG} (gate-drive) mainly influence di/dt at turn-on, but they are not critical for usual circuit lay-out and must be carefully considered, only when devices are paralleled [8].

Transconductance g_{FS} is the most critical parameter. In fact, a high value of g_{FS} can generate very high continuous short circuit current and very high peak current during transient.

2.4 SHORT CIRCUIT CAPABILITY CHARACTERIZATION.

In order to make test conditions as reproducible as possible, the short circuit capability characterization was implemented using test circuit "A" with stray inductances reduced to minimum value.

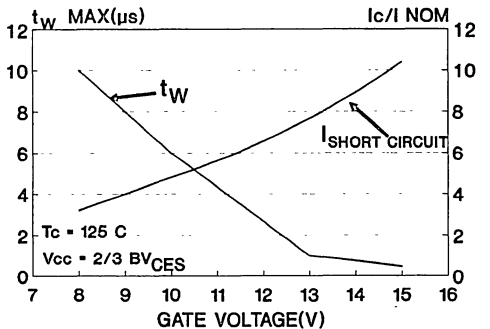


Fig. 8. Short circuit performance versus gate bias of IGBTs having a high transconductance. Maximum current overshoot $\leq 20\%$ $I_{SHORT CIRCUIT}$.

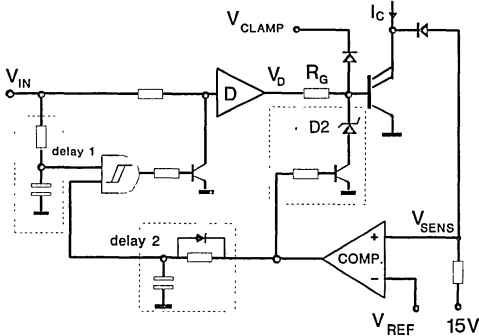


Fig. 9. Short circuit protection with high false alarm immunity.

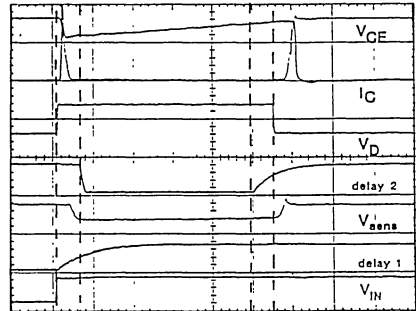


Fig. 10. Timing diagram of the protection circuit at turn-on and during overcurrent condition.

Short circuit capability is expressed in terms of:

- MAX SHORT CIRCUIT TIME (t_W as defined in figure 2)
 - SHORT CIRCUIT CURRENT & PEAK CURRENT (I_{SHORT} , I_{PEAK})
- Versus: - V_G , R_G , T_C , V_{CC} .

Figure 8 shows a characterization example of a IGBT having a high value of the transconductance. For $V_G \geq 13V$ the device fails at turn-on due to static latch-up.

3.0 SHORT CIRCUIT PROTECTION.

To ensure short circuit tolerance of a power control system and of its output power switches, the following problems must be carefully considered:

- 1 - Limitation of the short circuit current.
- 2 - Limitation of short circuit protection delay.
- 3 - Nuisance tripping creating false alarm.

3.1 DESCRIPTION OF THE PROTECTION CIRCUIT.

The figure 9 shows the schematic diagram of a protection circuit using the IGBT

saturation voltage for sensing. Sensing resistors or current transformers can also be employed without significant changes. The zener diode limits the gate voltage during a short circuit condition so limiting short circuit current.

Delay 1 and delay 2 realized with a R, C filter and Schmitt trigger avoid activation of the protection circuit in case of false short circuit conditions. Delay 1 must filter transitory phenomena at IGBT turn-on, delay 2 gives noise immunity to the circuit.

The diode "D2" clamps gate voltage overshoots due to dV/dt . When a short circuit is detected the IGBT is turned off by its gate resistor in order to limit dV/dt and collector overvoltages.

The timing diagram in figure 10 shows the working mode of the circuit at turn-on and with an overcurrent condition during operation:

- At turn-on, the input 1 of the "AND" becomes high ($IN_{HIGH} = 8V$) after delay 1; If IGBT saturation was not detected ($IN_{LOW} = 2V$) during delay 1 the driving circuit input taken low.

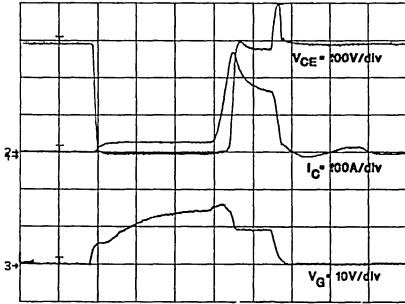


Fig. 11. Short circuit protection waveforms in the test condition "B". IGBT is TSG50N50DV. Time scale: 2µs/div.

- When, during normal operation, there is an overcurrent condition, the IGBT saturation voltage reaches reference voltage " V_{REF} " and the comparator activate the zener and the delay 2. If the overcurrent condition continues after delay 2, then the driver input is pulled down and the IGBT is turned-off.

This circuit works as a monostable multivibrator with positive edge triggering, but the IGBT is "ON" only if V_{IN} is high, so the noise immunity is assured. If an overcurrent or a short circuit condition were detected, it is necessary to take V_{IN} to the low.

3.2 PERFORMANCE OF THE PROTECTION CIRCUIT.

When the short circuit exists at turn-on (test circuit "A"), test conditions of the characterization are respected.

The performances of the circuit can be critical when the short circuit occurs during normal working conditions and the devices is in full saturation. Figure 11 shows that a significant current overshoot stresses the IGBT (TSG50N50DV) under this short circuit

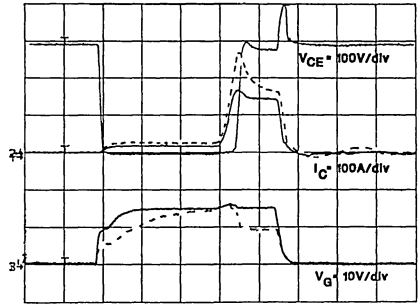


Fig. 12. Short circuit waveforms without voltage reduction of a IGBT having low transconductance compared to waveforms of figure 11 in dotted lines. $t = 2\mu\text{s}/\text{div}$.

condition even if the protection works correctly.

In fact the protection circuit needs a delay to pull the gate voltage to a safe value. This delay depends on the saturation voltage detection time and on the discharge time of the IGBT input capacitance. The discharge time can be significant due to the Miller effect during collector voltage rise. Moreover a high value of g_{FS} can induce a very sharp rise of the current during delay.

To avoid this phenomenon, IGBTs with a lower value of saturation current and transconductance should be employed. In fact, if the short circuit current is limited by the device itself, then it is not necessary to reduce the gate voltage during short circuit time. Figure 12 shows collector current and gate voltage waveforms of an IGBT having low saturation current ($I_{CSat} = 3 \cdot I_{NOM}$ @ $V_G = 15V$) subjected to the same short circuit condition shown in figure 11 and without any gate voltage reduction, compared to the TSG50N50DV with high transconductance and gate voltage reduction during short circuit (same waveforms of figure 11 in dotted lines).

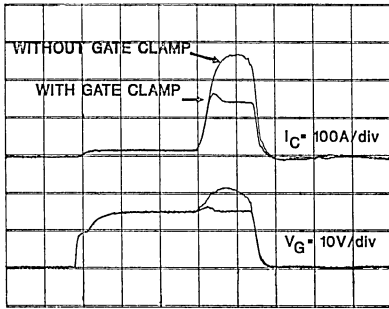


Fig. 13. Gate voltage and collector current with and without gate voltage clamping. $t = 2\mu\text{s}/\text{div}$.

If the gate voltage reduction is eliminated a fast clamping circuit is necessary. Figure 13 shows a comparison of the gate voltage and collector current waveforms with and without gate clamping voltage. This diode also limits gate voltage overshoots in the short circuit condition.

3.3 SHORT CIRCUIT SPECIFICATION OF IGBTs.

The criteria for providing short circuit protection to match the reliability of the more usual protection circuits are:

- $t_W > 5\mu\text{s}$ (delay to avoid false alarm)
- $I_{C\text{sat}} < 3 \cdot I_{\text{NOM}}$ (to ensure safe turn-off)
- $T_C = 125^\circ\text{C}$ (working temperature)

$5\mu\text{s}$ is the time necessary to ensure full saturation of IGBTs.

To give sufficient margin for safe operation $t_W \approx 10\mu\text{s}$.

4.0 DESIGN OF AN IGBT UNDER SHORT CIRCUIT CONDITIONS

The intrinsic short circuit ruggedness of IGBTs was improved by a optimization of the device structure aimed at obtaining a suitable value of the saturation current ($I_{C\text{sat}}$ @ $V_G=15\text{V}$, $T_j=150^\circ\text{C}$).

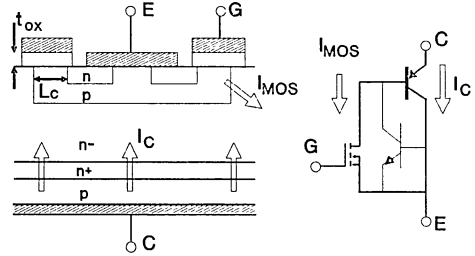


Fig. 14. Cross section of IGBT structure and simplified equivalent circuit.

Parameters influencing transconductance and $I_{C\text{sat}}$ ($I_{C\text{sat}} = g_{\text{FS}} \cdot (V_G - V_{\text{TH}})$ saturation current also affect saturation voltage " V_{CEsat} " [2] as shown by (1) and (2).

$$I_{C\text{sat}} = \frac{1}{(1-\alpha_{\text{PNP}})} \cdot \frac{\mu_{\text{ns}} C_{\text{ox}}}{2} \cdot \frac{Z}{L_C} (V_G - V_{\text{TH}}) \quad (1)$$

$$V_{\text{CE}} = \frac{KT}{q} \ln \left[\frac{(1-\alpha_{\text{PNP}}) d I_C}{2qW_R Z D_a n_i F(d/L_a)} \right] + \frac{(1-\alpha_{\text{PNP}}) L_C I_C}{\mu_{\text{ns}} C_{\text{ox}} Z (V_G - V_{\text{TH}})} \quad (2)$$

Where " L_C " is the channel length, " Z " is the channel perimeter, " C_{ox} " is the oxide capacitance ($C_{\text{ox}} = \epsilon S/t_{\text{ox}}$).

$I_{C\text{sat}}$ can be limited both by reducing the gain of the PNP transistor (α_{PNP}) and by acting on the MOSFET characteristics (L_C , Z , C_{ox}).

" α_{PNP} " influence both the PN junction threshold (first term of equation (2)) and the second term. For this reason only the MOSFET characteristics were optimized, so gaining advantages both in dynamic performances (C_G reduction) and in thermal stability [8].

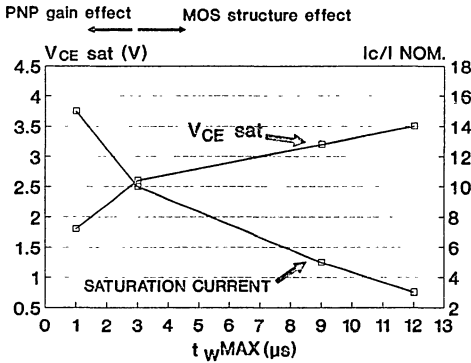


Fig. 15. Trade-off between saturation voltage and the short circuit ruggedness expressed as MAX t_w and saturation current @ $V_G = 15V$.

To reduce the saturation current by 70%, channel length (L_c) and oxide thickness " t_{ox} " were increased by 40%. This gives the best compromise between short circuit performances and saturation voltage as figure 15 and 16 show.

The lefthand side of figure 15 shows the effect of the PNP gain reduction due to life time reduction processes.

5.0 CONCLUSION.

The analysis of parameters influencing short circuit operation of IGBTs has led to the design of a suitable protection circuit, even for devices having modest short circuit performance.

This solution allows the use of IGBTs with very low saturation voltage.

However, an additional very fast circuit that reduces gate voltage during short circuit is necessary. During the delay of this circuit the dV/dt due to the IGBT desaturation can cause a dangerous peak current. IGBTs having low transconductance can solve this problem.

Decreasing transconductance of a IGBT

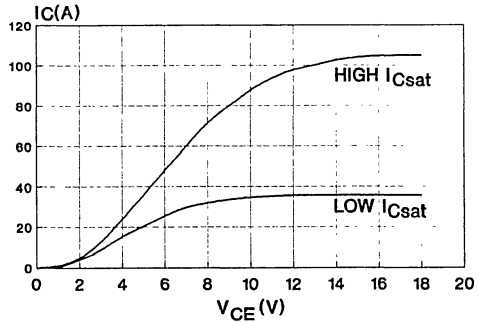


Fig. 16. Comparison of two IGBT output characteristics, with low I_{Csat} ($I_{Csat}=3 \cdot I_{NOM}$) and HIGH I_{Csat} ($10 \cdot I_{NOM}$) @ $V_G = 15V$.

causes saturation voltage to increase. The optimization of the IGBT structure allowed the realization of an IGBT with sufficient short circuit capability ($t_w MAX = 10 \mu s$), and with a value of V_{CEsat} that is 20% higher than the V_{CEsat} of a IGBT having $t_w MAX = 1 \mu s$. This IGBT requires a simplified short circuit protection network and it does not compromise the efficiency or the short circuit ruggedness of the system.

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SAFE BEHAVIOUR OF IGBTs
SUBJECTED TO dV/dt

by R. Letor, M. Melito

ABSTRACT

When an IGBT in the off state is subjected to a high dV/dt , parasitic turn-on can occur leading to additional losses.

This paper describes the phenomenon and indicates the main parameters influencing this behaviour.

Several methods of suppressing this parasitic phenomenon are described.

Using a suitable design of gate drive, it is possible to increase the circuit reliability in all conditions.

Practical examples and measurements are given.

INTRODUCTION

The behaviour of IGBTs subjected to a dV/dt differs according to the working conditions. We can consider two distinct cases:

- static dV/dt

The static condition occurs when the dV/dt applied to an IGBT in the off state, acting through the reverse capacitance $C_g \approx C_{res}$, causes the gate voltage to rise turning the device on. This behaviour is typical of a circuit in bridge configuration, where the dV/dt is generated during complementary switch turn-on. This undesired effect generates

additional losses, mostly in devices in the off-state, due to the presence of both high voltage and high current on the collector. Parasitic turn-on must be avoided and this can be prevented by modifying the design of the drive circuit.

- **dynamic dV/dt**

In this condition the dV/dt is applied to an IGBT during the recombination of minority carriers in the substrate and a peak current appears during the collector voltage rise time even if the gate and the emitter are in short circuit. The dynamic condition can occur when the IGBT works in thyristor mode, typically in a quasi resonant converter with a zero current switch (QRC-ZCS). In this case the power losses depend on the device structure and on the converter resonant frequency. Thus, this phenomenon sets a limit to the operating frequency.

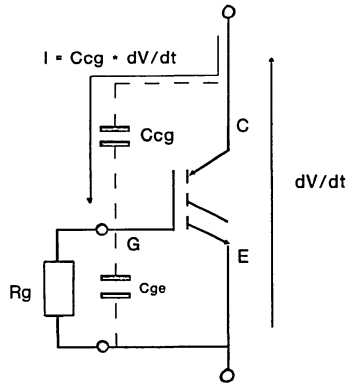


Fig.1 - Current flow through IGBT capacitances due to dV/dt

1. SPURIOUS TURN-ON IN STATIC dV/dT CONDITION.

1.1 Description of the Phenomenon.

The equivalent diagram of fig.1 shows current flow across the structure of an IGBT in the off-state when a rising collector-emitter voltage is applied.

The current through the reverse capacitance C_{gc} ($C_{gc} \ll C_{ge} \approx C_{res} \Rightarrow i = C_{res} \cdot dV/dt$), charges the gate capacitance; in this way, the gate voltage can reach the IGBT threshold voltage and a conduction current appears.

Photo 1 shows the waveforms during a spurious dV/dt turn-on giving prominence to the simultaneous presence of high voltage and high current.

If the output impedance of the drive source is high this phenomenon occurs more easily because of the higher ratio between the reflected V_{ge} and the applied dV/dt.

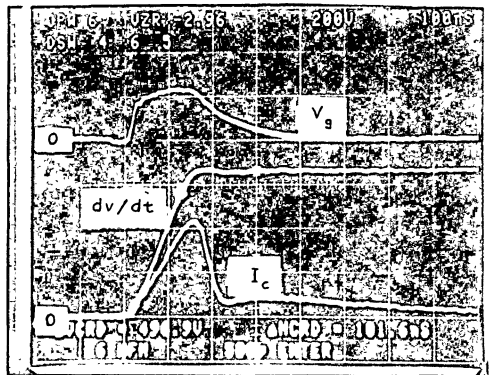


Photo 1 - Waveforms during a spurious turn-on due to static dv/dt condition.

Gate voltage = 2V/div,
 Drain Voltage = 200V/div,
 Drain current = 2A/div.

Thus the main parameters influencing an IGBT's behaviour in static dV/dt condition are:

- device characteristics (C_{res} , C_{ge} , V_{th} , g_{fs})
- temperature
- R_{ge} , dV/dt value
- gate bias

1.2 The influence of temperature.

When the temperature increases, IGBT parameters vary as follows:

- transconductance at low current increases
- threshold voltage decreases
- turn-off time increases

As a consequence, when the temperature increases the power losses due to dV/dt turn-on increase and the phenomenon occurs at a lower dV/dt value.

Photo 2 shows a comparison of the peak current at $T_j = 25^\circ\text{C}$ and $T_j = 100^\circ\text{C}$ with the same static dV/dt conditions.

1.3 The influence of dV/dt and R_{ge} .

The effect of R_{ge} and dV/dt can be evaluated with the simplified circuit in fig.2 but the mathematical resolution is not easy because of the influence of the voltage on C_{gc} and C_{ge} . The behaviour of SGS-THOMSON's IGBTs were characterized by the test circuit in fig.3, taking care to measure the energy dissipated in the devices at $T_c = 100^\circ\text{C}$ $E = \int v(t) \cdot i(t) dt$.

The curves in fig.4 show this measured energy versus both R_{ge} and a typical dV/dt.

Considering a single curve, $dV/dt = \text{constant}$, it can be observed that it has a minimum constant value for R_{ge} lower than the "knee" value.

In this region IGBT parasitic turn-on does not occur and the absorbed energy only charges the IGBT output capacitance.

1.4 The influence of gate bias.

Gate bias voltage influence was analyzed for negative voltage (V_{EE}) using the test circuit in fig. 3.

Figs.5 and 6 show that, when $V_{EE} = -5V$ spurious turn-on does not occur even if the value of the resistance connected to the gate is high (180Ω). Looking at the waveforms in fig. 7 we can note two different effects on the gate voltage due to the negative bias. The first is obviously that the gate voltage is offset from V_{EE} and the second is that there is a different gate voltage peak even if the applied dV/dt is the same. This happens because of the influence of gate voltage on C_{ge} .

Photo 3 shows the gate charge curve and clearly demonstrates the variation of the slope

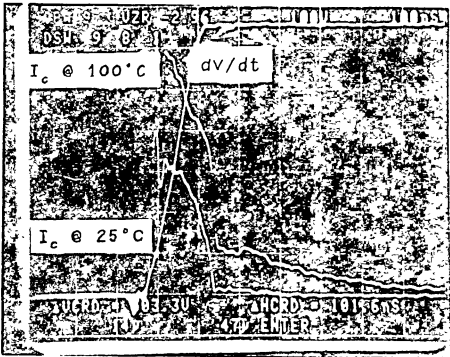


Photo 2 - Comparison between the peak current due to static dv/dt with $T_c = 25^\circ\text{C}$ and $T_c = 100^\circ\text{C}$, $I_D = 2A/\text{div}$, $V_D = 100V/\text{div}$, $R_g = 100 \text{ W}$, $E@25^\circ\text{C} = 226 \text{ mJ}$, $E@100^\circ\text{C} = 1.2\text{m6 mJ}$

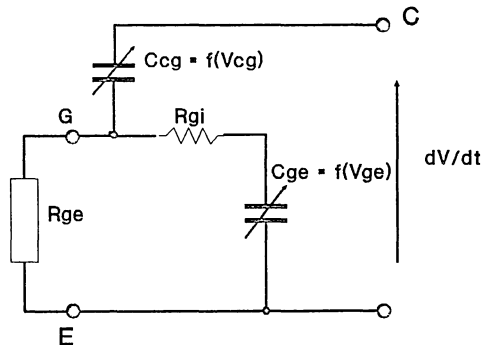


Fig. 2 - Simplified input circuit.

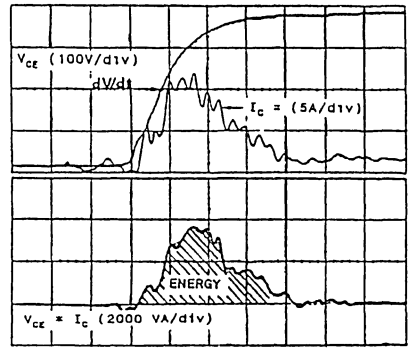
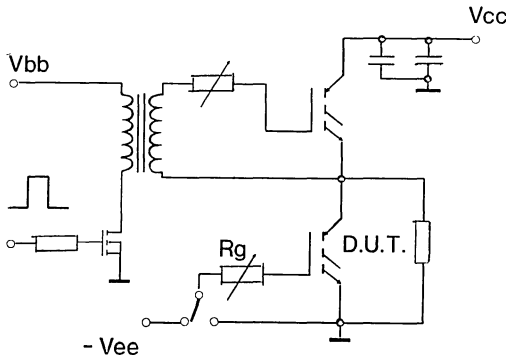


Fig. 3 - Test circuit and related waveforms

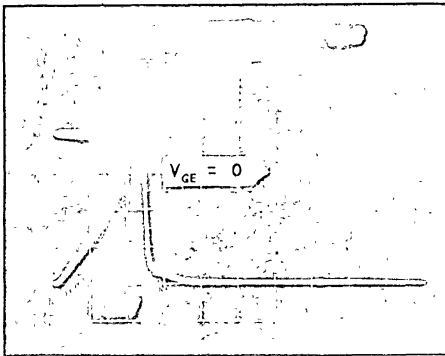


Photo 3 - Gate charge. Curve $V_{ge} = 2V/div$. $V_{ce} = 100V/div$

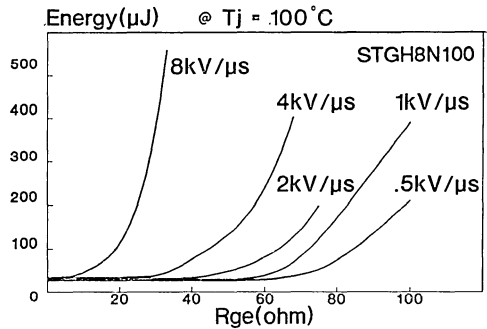


Fig. 4 - Energy dissipated versus R_{ge} and dV/dt

of the voltage occurring at $V_{ge} = -2V$. If V_{ge} is greater than this value then $C_{ge} = C_{ies}$ (input capacitance, output short circuited) if V_{ge} is lower than this then C_{ge} is about four times C_{ies} and reduces the gate voltage peak.

2. HOW TO AVOID PARASITIC dV/dt TURN-ON.

The previous paragraph shows that it is possible to avoid undesired turn-on during dV/dt by:

- a) connecting gate and emitter by a low turn-off resistance
- b) reducing dV/dt
- c) biasing the gate, during the off state, with a negative voltage

2.1 LOW R_{ge} VALUE DURING THE OFF PHASE.

Depending on the required performance, this solution can be applied as follows:

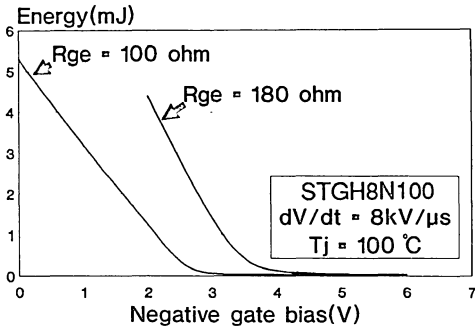


Fig. 5 - Dissipated energy versus negative gate bias and R_{ge}

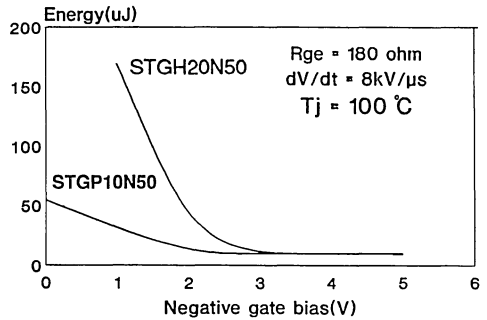


Fig. 6 - Dissipated energy versus negative gate bias

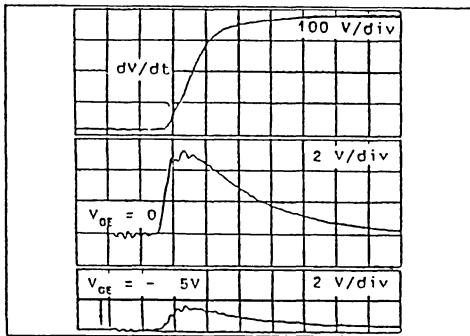


Fig. 7 - Comparison of gate voltage behaviour with and without negative bias

- 1) R_{ge} is the gate turn-off resistance as shown in fig.8a.
- 2) R_{ge} is connected just after turn-off as shown in fig.8b.

The disadvantage of the driving circuit shown in fig.8a is that this circuit does not guarantee the full safe operating area (RBSOA) when R_{gs} is less than 100Ω , for the following reasons:

- the latching current depends on dV/dt during turn-off

- R_{ge} strongly influences dV/dt at turn-off

- the RBSOA is guaranteed for $R_g = 100\Omega$

Fig.9 shows this behaviour and the diagram in fig.10 shows that the maximum R_{ge} necessary to avoid dV/dt problem is less than 100Ω

Thus, the driving circuit of fig.9 is suitable for applications where the full safe operating area @ $R_g = 100\Omega$ is not required.

The driving circuit of fig.8b turns-off the IGBT with $R_g = 100\Omega$ obtaining the full RBSOA but the delay " $d = t_{storage} + t_{fall}$ " for each must be optimised for each application.

2.2 Reduction of dV/dt .

The spurious turn-on problem due to dV/dt is typical of the circuit shown in fig.11; in this circuit, the free-wheeling diode in the parallel with the lower IGBT, which is in the off state, is turned off during the upper IGBT turn-on and a high dV/dt is generated.

Thus, dV/dt value depends on :

- complementary IGBT turn-on speed (dI/dt)
- free-wheeling diode "softness"
- wiring inductances

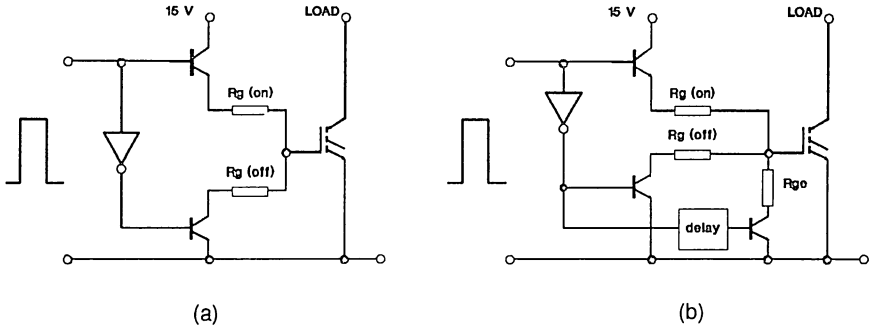


Fig. 8 - IGBT driving circuits

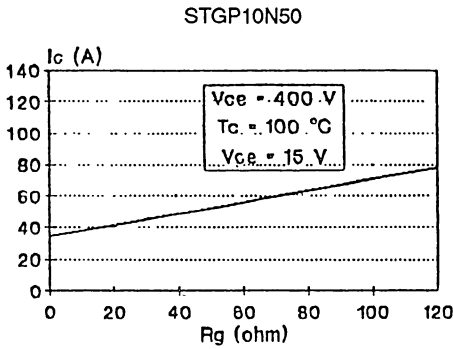


Fig. 9 - I_{latch} versus R_{goff}

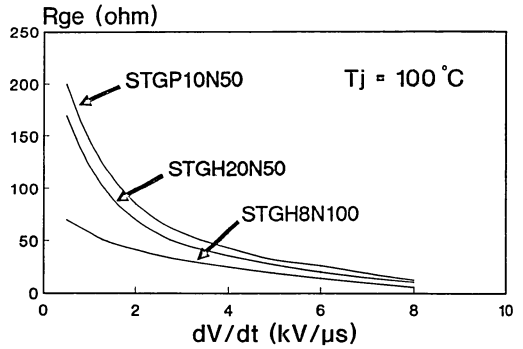


Fig. 10 - Max R_{ge} values that avoid static dV/dt turn-on versus dV/dt

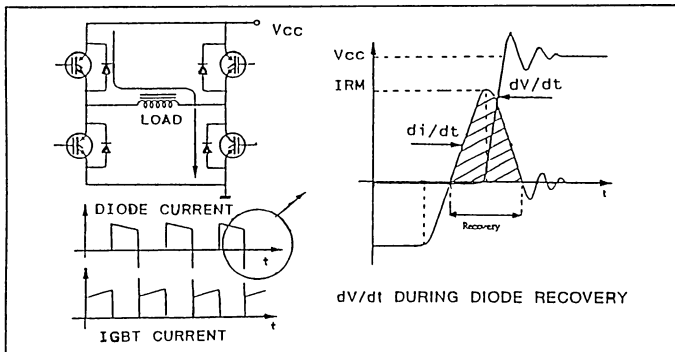


Fig. 11 - Typical circuit where static dV/dt conduction can occur.

Diode current recovery during turn-off = 10A/div

Drain voltage and dv/dt due to the diode turn off 200V/div.

Current due to spurious turn-on with $R_{g\text{on}} = 100 \Omega$ 2A/div

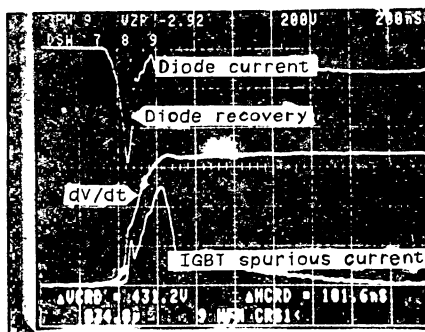


Photo 4 - Waveforms in the circuit of fig. 11 when: $R_{g\text{on}} = 100 \Omega$

Diode recovery = 5A/div.

Dv/dt due to diode turn-off 200V/div.

Current in the IGBT in off state 2A/div.

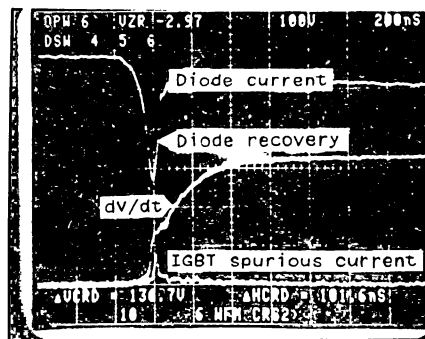


Photo 5 - Waveforms in the circuit of fig. 11 when $R_{g\text{on}} = 200 \Omega$. In this condition turn-on due the dv/dt does not occur.

and it can be minimized:

- using fast soft recovery diodes.
- reducing wiring length.
- turning on IGBTs slowly, with a high value of turn-on gate resistance.

Photo 4 and 5 show that the dv/dt is reduced to a safe value in the circuit of fig.11. Photo 4 uses a low value of turn-on gate resistance whereas photo 5 uses a high value gate

resistance. In the case of photo 5 spurious turn-on due to the dv/dt does not occur.

2.3 driving the IGBT with a negative voltage.

Biasing the gate negatively, as shown in photo 6, causes a higher dv/dt during turn off because of the availability of a large gate current. It is possible to avoid this drawback, which reduces the effective RBSOA, simply by increasing the value of $R_{g(\text{off})}$.

3. DYNAMIC dV/dt .

This condition may occur in a zero current quasi resonant converter where the IGBT works as a thyristor.

In this application, see fig. 12 and photo 6 the IGBT is turned-off when the collector current is zero and the collector voltage starts to rise after a delay time $t_d \approx (2 * f_{resonance})^{-1}$, corresponding to the end of the reverse recovery phase of the antiparallel diode.

This increasing voltage causes a current spike,

leading to power losses because of the minority carriers in the IGBT substrate. The amplitude of the spike depends on several factors which involve both IGBT and circuit characteristics. One of the factors is the amount of the stored charge when the dV/dt is applied. The stored charge depends on the type of IGBT (slow or fast), junction temperature and resonant frequency.

Increasing temperature and/or frequency leads

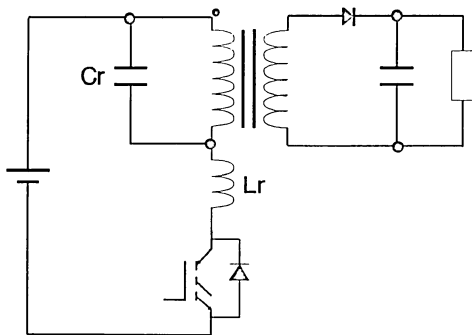


Fig. 12

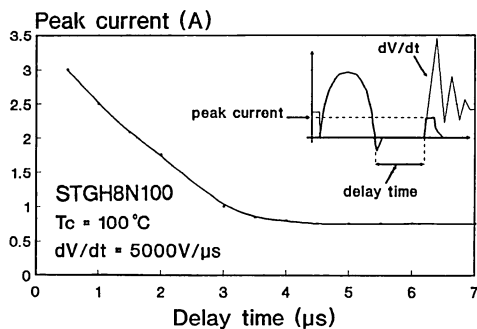


Fig. 13 - Peak current versus t_{delay}

Gate voltage = 10V/div

Drain current = 2A/div

Drain voltage = 200V/div

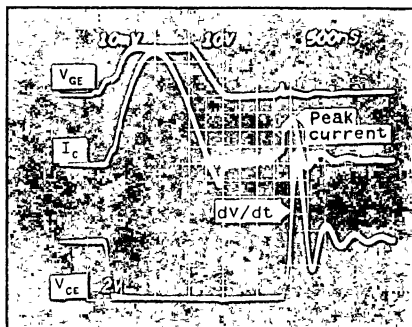


Photo 6 - Waveforms in a resonant converter where dynamic dV/dt occurs. Device = STGH8N100, Tc = 100°C

to a higher current peak. The diagram in fig.13 shows how increasing resonant frequency affects the current peak.

For frequencies lower than about 120 kHz the current peak is constant, because there is no more stored charge and due solely to capacitive effects that are similar to those in Power MOSFETs.

The other factor is related to the rate of voltage rise which depends strongly on the softness of the diode. Using a slower IGBT emphasizes the effects discussed above. In low frequency working conditions the power losses are no longer negligible and must be considered during the circuit design in order to avoid thermal runaway and consequent device failure.

4. CONCLUSION.

The dV/dt phenomenon causes power dissipation in IGBT devices and this may lead to the failure due to thermal runaway. The

way to avoid this phenomenon depends on the operating conditions.

When an IGBT works in a static dV/dt condition, as for example in a bridge circuit, it is possible to prevent the dV/dt phenomenon by modifying the design of the IGBT drive circuit:

- reducing dV/dt .
- connecting a low gate-emitter resistance.
- driving the IGBT with a negative voltage at turn-off.

If a high current is to be controlled with a switched mode technique, it is necessary to design the drive circuit to obtain the full guaranteed RBSOA.

When the IGBT works in dynamic dV/dt condition, as in a QRC-ZCS, it is not possible to avoid power dissipation in the device by optimization of the drive circuit. These kind of losses can only be limited by selecting a suitable converter resonant frequency and antiparallel diode.



**STATIC AND DYNAMIC BEHAVIOUR
OF PARALLELED IGBTs**

by R. Letor

ABSTRACT

Problems associated with power device characteristics when power devices are connected in parallel, such as thermal stability and balanced switching behaviour can be solved by using insulated gate bipolar transistors (IGBT).

This note deals with parallel IGBT behaviour analyzing both static and dynamic characteristics.

The influence of heatsink mounting, lay-out, and drive circuit are described in order to demonstrate the best way to parallel IGBTs for optimum performance.

In addition the major advantages of the ISOTOP package are shown.

I. INTRODUCTION

When switching devices are paralleled, the following points must be carefully considered:

- 1) On-state losses balance.
- 2) Switching losses balance.
- 3) Thermal stability.

The loss unbalance, depending mainly on the spread of the device parameters (V_{CEsat} , switching time), can cause excessive power dissipation in one or more devices.

The thermal instability, correlated to the behaviour of the devices when the temperature increases, can cause thermal runaway and lead to the failure of the device. This note explains the theory, describes practical examples and suggests possible solutions.

The behaviour of the IGBTs considered is not dependent on type, hence, the results can be extended to all SGS-Thomson IGBTs.

II. BEHAVIOUR OF PARALLELED IGBTs IN THE ON STATE.

The IGBT is a voltage driven device, hence when the devices are in parallel the drive conditions are the same for all devices (i.e. they all have the same V_{GE}). Thus the influence of output characteristics and of the transfer characteristics can be studied separately.

A. Current balance in the on state.

Current balance can be studied with the simplified circuit of fig.1 where the following conditions are respected:

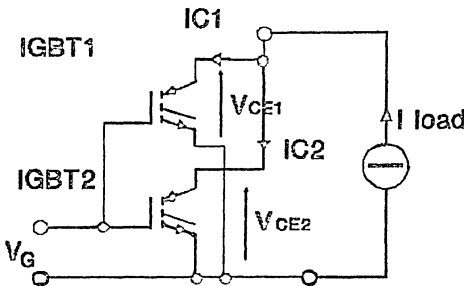


Fig. 1. Circuit where current balance depends only on IGBT characteristics.

$$\begin{aligned}
 V_{CEsat1} &= V_{CEsat2} \\
 I_{C1} + I_{C2} &= I_{LOAD} \\
 V_{CEsat1} &= f(I_{C1}, T_{j1}, V_{GE1}) \\
 V_{CEsat2} &= f(I_{C2}, T_{j2}, V_{GE2}) \quad (1)
 \end{aligned}$$

This system of equations (1) has a graphical solution which is shown in fig.2 for the extrapolation of current balance in two paralleled IGBTs with the same junction temperature ($T_{j1} = T_{j2}$).

Figure 3 shows the influence of the spread of V_{CEsat} on the current balance.

B. The influence of the temperature on current balance.

The fig.4 shows the basic equivalent structure of the IGBT.

The device functions as a bipolar transistor which is supplied base current by a Power-MOSFET.

The IGBTs output characteristic combines both the bipolar and the Power-MOSFET characteristics.

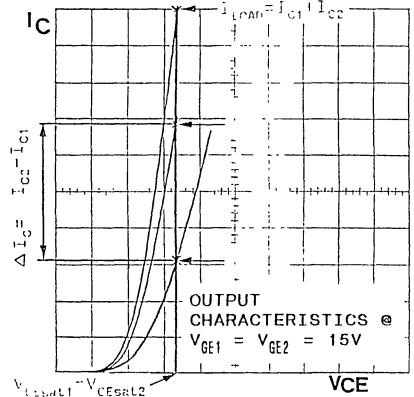


Fig. 2. Graphical extrapolation of current balance in the on state for two STGP10N50 @ $I_{LOAD} = 10A$; $T_{j1} = T_{j2} = 25^{\circ}C$; $I_C = 1A/div.$; $V_{CE} = 0.5V/div.$

The curves in fig.5 show these effects and highlight the following points:

- 1 - The temperature coefficient of V_{CEsat} is negative at low current density ($I < I_{NOM}$) (bipolar effect).
- 2 - The temperature coefficient of V_{CEsat} is positive at high current density ($I > I_{NOM}$) (Power-MOSFET effect).
- 3 - The temperature coefficient of the dynamic resistance (di/dv) is positive (Power-MOSFET effect).

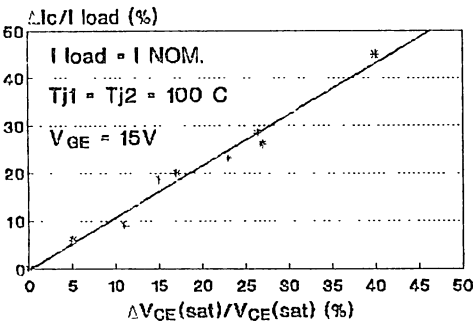


Fig. 3. Current balance versus the $V_{CE(sat)}$ difference in two paralleled IGBTs.

The effect of this behaviour is that the influence of the temperature on current balance is small and that the current balance improves when the temperature increases, if $T_{j1} = T_{j2}$ ($\Delta T_j = 0$), (fig.6).

Figure 7 shows the effect on current balance when the junction temperature of paralleled devices are different ($\Delta T_j \neq 0$) and the medium temperature is constant $(T_{j1} + T_{j2})/2 = K$:

- At low current, current balance is worst when the temperature difference increases, but the temperature coefficient is low.

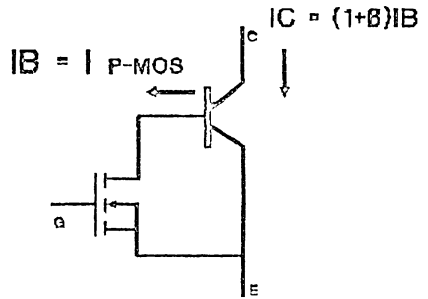


Fig. 4. Simplified equivalent circuit of an IGBT.

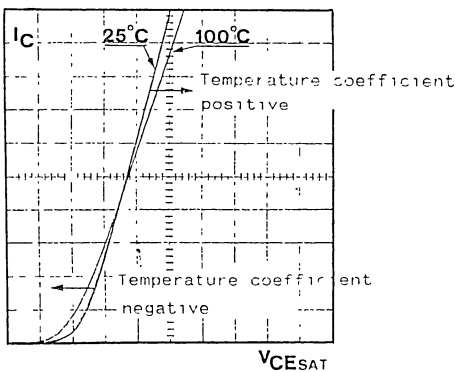


Fig. 5. Output characteristics versus the temperature for STGP10N50. $I = 2\text{ A/div.}$; $V = 0.5\text{ V/div.}$

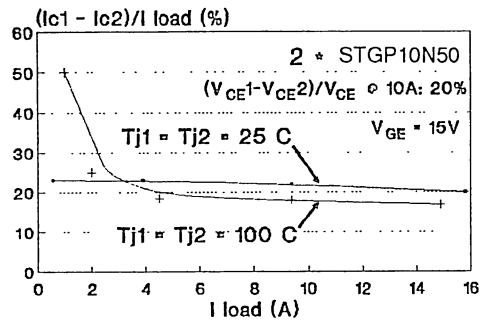


Fig. 6. Current balance versus I_{LOAD} and temperature in two paralleled IGBTs.

- At high current the behaviour is similar to the power- MOSFET behaviour; in fact, current balance improves when the temperature difference increases.

C. INFLUENCE OF THE TRANSFER CHARACTERISTICS.

When IGBTs are strongly saturated, the influence of the transfer characteristics on paralleled devices behaviour is small.

The figure 8 shows that the gate voltage scarcely influences the V_{CEsat} value; hence it is not possible to improve the current balance in the on-state by connecting an emitter-ground resistance.

III. PARAMETERS INFLUENCING SWITCHING BEHAVIOUR.

The IGBT's switching behaviour depends on:

- Device parameters (V_{th} , g_{fs} , C_i , C_{rSS} , C_o).
- Drive circuit.
- Lay-out (Parasitic inductances).

The switching behaviour is studied in the circuit of figure 9 where the stray inductance " $L_{s1}+L_{s2}+L_{s3}$ " is small and the IGBTs are

turned on, while the free wheeling diode is still conducting; with this working condition di/dt is not limited by the stray inductances and depends on the IGBTs switching speed

$$(di/dt \gg V_{cc}/(L_{s1} + L_{s2} + L_{s3}).$$

A. Turn-on.

During turn-on, the switching losses depend mainly on the di/dt that influences the peak current due to the diode recovery ($E_{co} \approx I_{peak} \cdot t_{cross} \cdot V_{cc}/2$).

In the circuit of figure 9, the voltage drop caused by the inductance of the emitter-ground connection (L_{s1}), reduce the drive current ($I_G = (V_d - V_G - L_{s1} \cdot di/dt) / R_G$), and acts as a negative feedback during current rise time. Taking into account the effect of L_{s1} , the value of di/dt is:

$$di/dt \approx (V_d - V_{th}) / (R_G C_i / g_{fs} + L_{s1})$$

For 1000V devices and with $R_G = 100\Omega$:

$$15 \cdot 10^{-9} < R_G C_i / g_{fs} < 25 \cdot 10^{-9}$$

The inductance of 1cm of wiring is:

$$L_{s1} \approx 10 \cdot 10^{-9} \text{ H/cm}$$

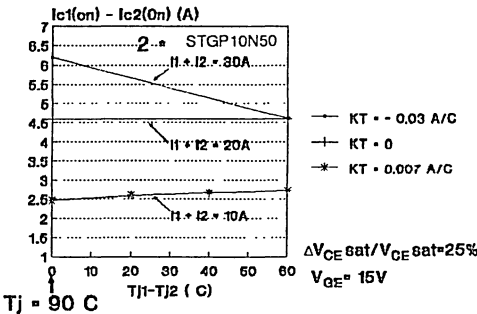


Fig. 7. Influence of ΔT_j on current balance during the ON-state. K_T is a temperature coefficient.

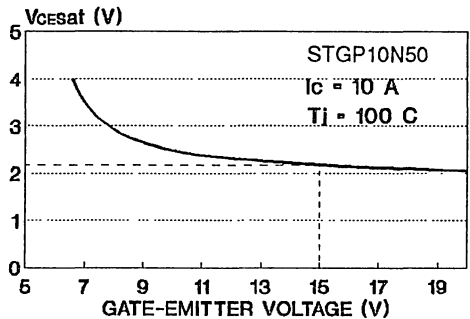


Fig. 8. Typical V_{CEsat} versus gate bias.

From this it can be seen that the spread of device parameters has less influence on the di/dt value than the parasitic inductance of the emitter-ground connection.

B. Fall.

During current fall two distinct phases can be seen (figure 10).

Phase 1 is similar to the current fall of power-MOSFET and the parameters influencing the di/dt are the same parameters that influence di/dt during turn-on.

The tail during phase 2 which is due to the minority carriers stored in the substrate mainly affects the switching losses.

The tail amplitude depends on T_j and on the turn-off current; hence, the turn-off current and the working temperature mainly influence the losses during the fall time (Fig. 11,12).

C. Storage.

During the storage time " $I_C = g_{fs} (V_{GE} - V_{th})$ ", " $di/dt \approx 0$ ", and the current waveform depends only on the IGBTs parameters (g_{fs} , V_{th}) and on the drive circuit.

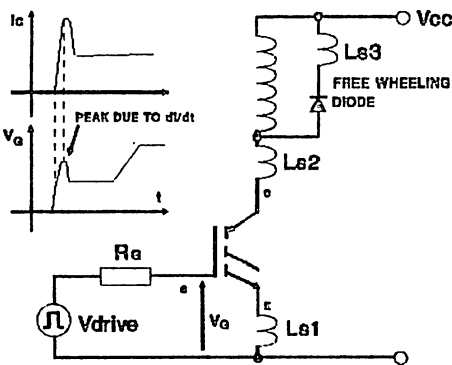


Fig. 9. Circuit showing the parasitic inductances influencing the switching behaviour.

IV. PARALLELED IGBT'S SWITCHING BEHAVIOUR.

The influence of the drive circuit, of the layout and of the device parameters was verified using the following conditions:

- 1 Gate drive with separate gate resistances (fig.13).
- 2 Gate drive with one gate resistance (fig.14).
- 3 Unbalanced emitter-ground wiring connection (fig.15).
- 4 Paralleling devices with the maximum spread of the parameters.

The voltage and collector current waveforms are stable in all conditions, even in the worst case condition where the gates are driven with a common resistance and the wiring inductances are strongly unbalanced

A. Turn-on.

Photo 1,2 show that the drive circuit influence on peak current balance is small and photo 3 shows that the peak current unbalance is significant in condition 3, where $\Delta L_{s1} = 0.15\mu H$.

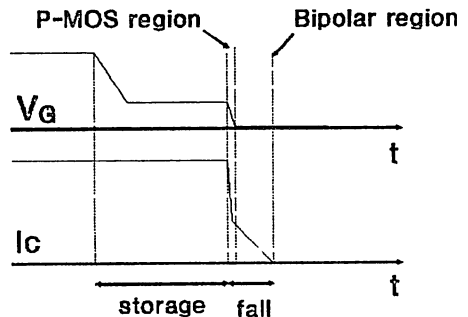


Fig. 10. Gate voltage and current waveforms during turn-off time.

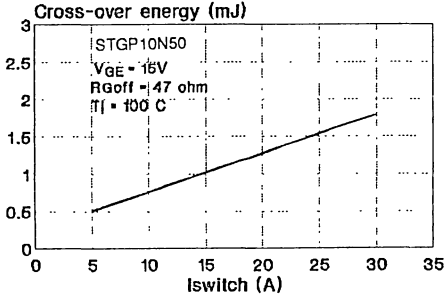


Fig. 11. Switching losses at turn-off V_s turn-off current.

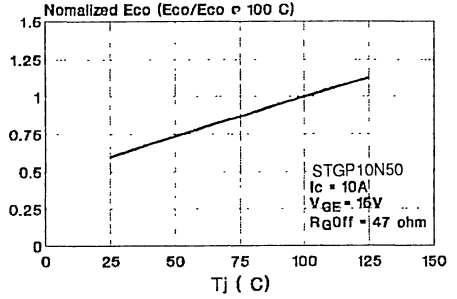


Fig. 12. Influence of temperature on turn-off losses.

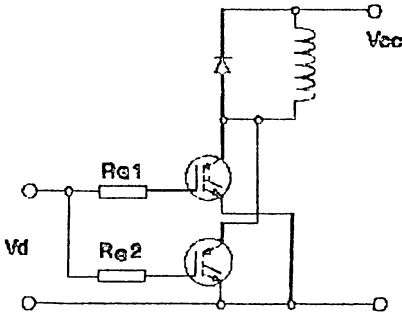


Fig. 13. Driving with separate gate resistance.

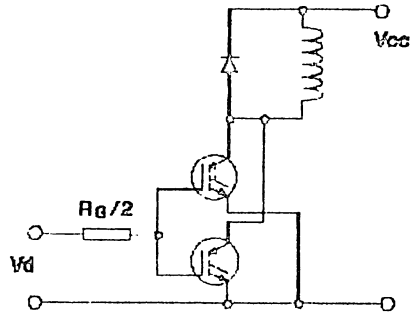


Fig. 14. Driving with one gate resistance.

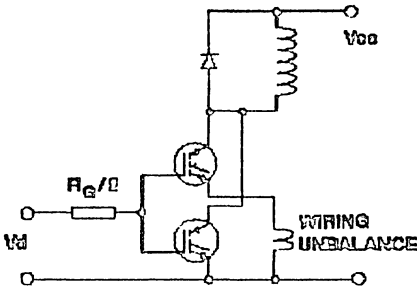


Fig. 15. Emitter ground wiring unbalance.

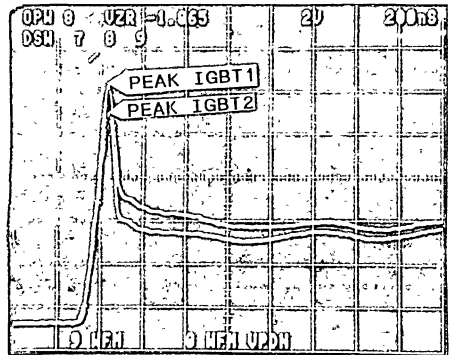


Photo 1. Turn-on with separate gate drive (fig. 13) of an STGH8N100:
 $I = 2A/div., t = 200ns/div.$

IGBTs with the maximum difference in parameter values were paralleled; the comparison of current waveforms in photo 1 and 2 demonstrates that the influence of parameter spread is low ($L_{s1} \approx 30 \text{ nH}$).

B. Fall.

Photo 4 and 5 show that the wiring inductance unbalance affects only the power-MOSFET phase; but this behaviour creates negligible

switching loss unbalance in comparison to the total turn-off switching losses.

The current unbalance just before current fall that affects the tail amplitude can create significant switching loss unbalance (see fig 17).

C. Storage.

During the storage time, the spread of the IGBTs parameters (g_{fs} , v_{th}) and the difference

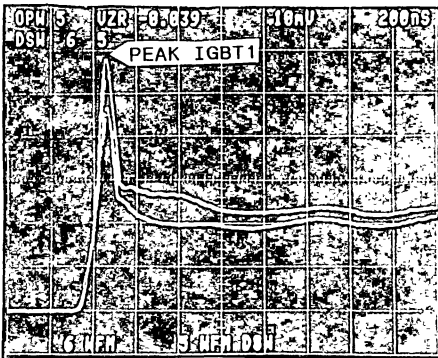


Photo 2. Turn-on with one gate resistance (fig. 14) of an STGH8N100; $I = 2\text{A/div.}$, $t = 200\text{ns/div.}$

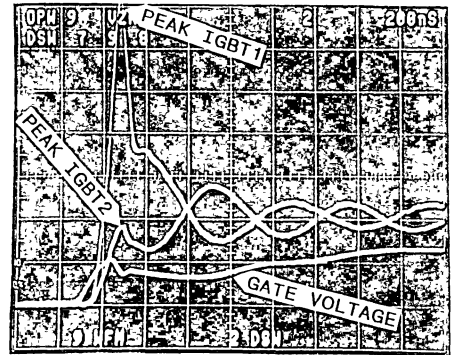


Photo 3. Turn-on with unbalanced emitter-ground wiring (fig. 15) of a STGH8N100; $I = 2\text{A/div.}$, $t = 200\text{ns/div.}$

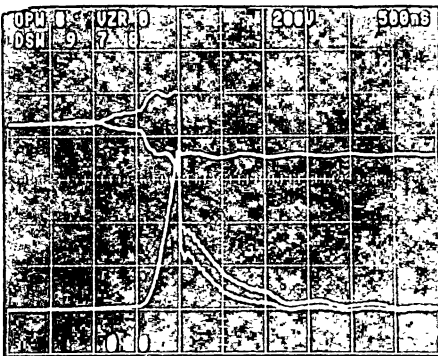


Photo 4. Turn-off with balanced gate-emitter wiring (fig. 14) of a STGH8N100; $I = 2\text{A/div.}$, $V = 200\text{V/div.}$, $t = 500\text{ns/div.}$

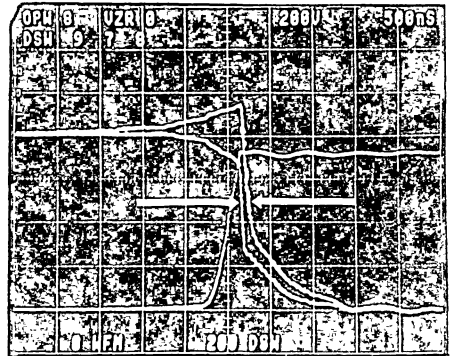


Photo 5. Turn-off with unbalanced emitter-ground wiring (fig. 15) of a STGH8N100; $I = 2\text{A/div.}$, $V = 200\text{V/div.}$, $t = 500\text{ns/div.}$

between storage times causes current unbalance thus creating switching loss unbalance.

Photo 6 shows the effect of the storage time differences when the gates are driven with separate gate resistances.

The collector current begins to fall in the device with the smaller storage time, consequently the current increases in the other IGBT so increasing storage current unbalance.

Driving the gates with only one gate resistance minimize this effect (photo 7); the device with the higher storage time hold the gate voltage to " $V_{th} + g_{fs} I_C$ " until the fall time phase, so equalizing the storage times.

Current unbalance due to the IGBTs parameter spread can be calculated with the equations (2) and (3).

The curves of fig.16,17 show, respectively, storage current unbalance and the consequent switching loss unbalance between two devices where the V_{th} and g_{fs} values are the limits of the parameter spread.

$$I_{load} = I_{1st} + I_{2st} = V_{GE} (g_{fs1} + g_{fs2}) - (g_{fs1}V_{th1} + g_{fs2}V_{th2}) \quad (2)$$

$$I_{storage} = I_{1st} - I_{2st} = V_{GE} (g_{fs1} - g_{fs2}) - (g_{fs1}V_{th1} - g_{fs2}V_{th2}) \quad (3)$$

V. THERMAL STABILITY.

When IGBTs are connected in parallel the on-state current is greater in the device with the smaller V_{CEsat} (fig.2); thus, the power dissipation and the junction temperature is higher in this device.

This phenomenon can cause a thermal instability because of the following reasons:

- Current unbalance increases when junction temperature difference increases (fig.7).
- Switching loss unbalance increases when junction temperature difference increases (fig.12).

The thermal stability can be achieved by mounting the paralleled IGBTs on the same heatsink; in this way the heatsink works as a negative feedback, because it transmits the heat from the device with the higher T_j to the device with the lower T_j so reducing the junction temperature difference.

In the ideal case where the thermal resistances (R_{thjh}, R_{thx}) are null, the thermal stability is assured because the devices work at the same temperature and the current balance improves when the temperature increases as shown in fig.6.

In real conditions the thermal resistances " R_{thjh} " are not negligible and the thermal stability can be studied with the equivalent thermal circuit of fig.18 which can be simulated with the system shown in fig.19.

The behaviour of the system near the final working point, is simulated using two paralleled IGBTs driving a constant inductive load; the devices are only active when the

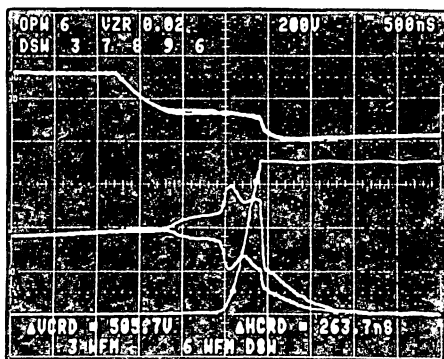


Photo 6. Effect of separate gate drive on storage current waveform. $I_C=2A/div.$, $V_{CE}=200V/div.$, $V_{GE}=10V/div.$, $t=500ns/div.$

heatsink temperature is uniform and at the final temperature which is independent of the current balance as the equations (4),(5),(6), (7),(8) show.

$$(T_{\text{heatsink}} = T_{\text{amb.}} + R_{\text{th h-amb.}} \cdot (V_{\text{CE(sat)}}(I_{\text{C1}} + I_{\text{C2}}) + \text{Switching losses}) \approx \text{const.} \quad (4)$$

$$I_{\text{C1}} + I_{\text{C2}} = I_{\text{LOAD}} = \text{const.} \quad (5)$$

$$V_{\text{CEsat}} \approx \text{const.} \quad (6)$$

$$\text{Switching losses} \approx \text{const.} \quad (7)$$

$$T_{\text{amb.}} = \text{const.} \quad (8)$$

The stability was evaluated with the following conditions:

- heatsink temperature constant (load constant).
- Initial junction temperature equal to the heatsink temperature (100°C).
- Turn-off current unbalance constant and equal to the maximum value (worst case).
- Thermal capacitances disregarded.

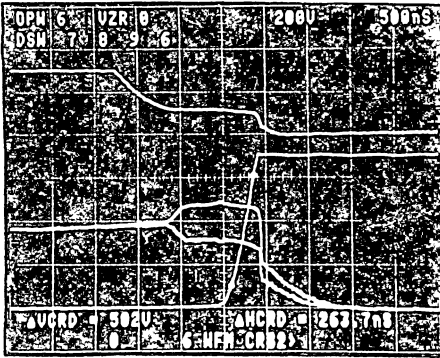


Photo 7. Turn-off with one gate drive resistance; $I_C = 2A/div.$, $V_{CE} = 200V/div.$, $V_{GE} = 10V/div.$, $t = 500ns/div.$

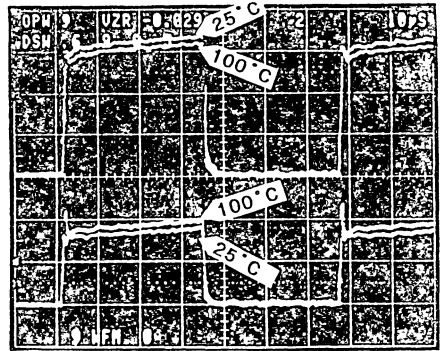


Photo 8. Comparison of current balance at $T_j = 25^\circ C$ and $100^\circ C$; $I_C = 2A/div.$, $t = 10\mu s/div.$

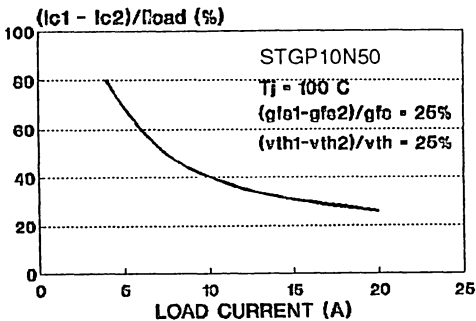


Fig. 16. Storage current unbalance versus load current.

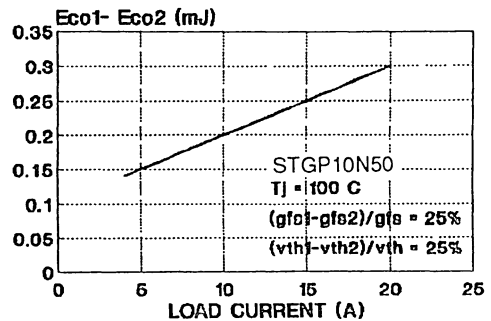


Fig. 17. Switching losses unbalance due to storage current unbalance.

The blocks in fig.19 signify the following computations:

- 1 - calculates initial current unbalance ($\Delta T_j = 0$) depending on the output characteristics of paralleled IGBTs.
- 2 - Calculates junction temperature difference depending on the on-state current unbalance (ΔI_{on}) and on switching current unbalance (ΔI_S).

$$\Delta T_j = R_{thjh} * (\Delta \text{ Power dissipation}).$$

- 3 - Calculates the growth of current unbalance (incr. ΔI) due to junction temperature difference (fig.16).

If R_{thx} is negligible ($R_{thx} \ll R_{thjh}$):

$$f(\Delta I_{on}) = R_{thjh} * \Delta P_{d_{on}} = R_{thjh} * V_{CEsat} * (t_{on}/T) * \Delta I_{on} = K_R * \Delta I_{on} \quad (9)$$

$$f(\Delta I_S, \Delta T_j) = R_{thjh} * P_{d_{switching}} = R_{thjh} * f * \Delta E_{co}(\Delta I_S, \Delta T_j) \quad (10)$$

$$\Delta E_{co}(\Delta I_S, \Delta T_j) = \Delta E_{co}(\Delta I_S, 100^\circ\text{C}) * (1 + \Delta T_j * K_S) \quad (\text{see fig.12,17}) \quad (11)$$

$$\text{incr } \Delta I_{on} = K_T * \Delta T_j \quad (\text{see fig.7}) \quad (12)$$

The equation (13) is the transfer function of the system.

$$\Delta T_j = K_R * \Delta I_{on} + R_{thjh} * f * \Delta E_{co} / (1 - (K_R * K_T + K_S * R_{thjh} * \Delta E_{co} * f)) \quad (13)$$

Thermal stability is guaranteed if the equation (14) is true.

$$(K_R K_T + K_S R_{thjh} * \Delta E_{co} * f) < 1. \quad (14)$$

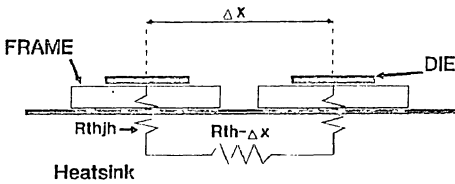


Fig. 18. Equivalent thermal circuit.

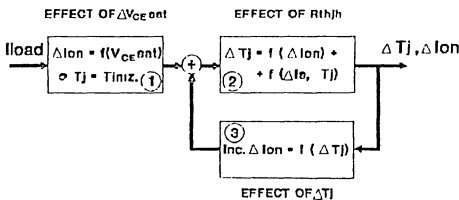


Fig. 19. Simulation of the temperature changes for two paralleled IGBTs.

A. Example of two paralleled STGP10N50FI (Fully insulated package).

Conditions: $f = 15\text{KHz}$

$$I_{LOAD} = 10\text{A}$$

$$\Delta V_{CEsat}/V_{CEsat} = 20\%$$

$$R_{thjh} = 3.5^\circ\text{C/W}$$

$$t_{on}/T = 0.5$$

Parameters Reference

$$\Delta E_{co} = 0.2 \text{ mJ} \quad \text{See fig.17}$$

$$K_S = 0.005/^\circ\text{C} \quad \text{See fig.12}$$

$$K_T = 0.007 \text{ A}/^\circ\text{C} \quad \text{See fig.7}$$

$$K_R = 3.5 \quad K_R = 2 R_{th\ jh} \cdot t_{on}/T$$

$$\Delta I_{on} (\Delta T_j = 0) = 2A \text{ See fig.3}$$

$$V_{CEsat} = 2V$$

$$\Delta T_j = 19^\circ C \quad (16)$$

$$\Delta I_{on} (\Delta T_j = 19^\circ C) = 2.13 A \quad (17)$$

Solution of the equations (13) and (14):

$$K_R K_T + K_S \cdot R_{th\ jh} \cdot \Delta E_{co} \cdot f) = 0.08 \ll 1 \quad (15)$$

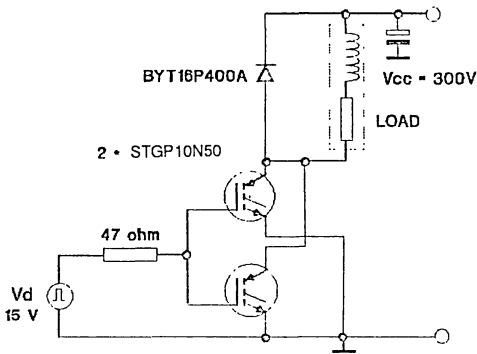


Fig. 20. Chopper circuit where paralleled IGBT behaviour was checked.

The equations (15) (16) (17) show that the thermal stability is very high even when the devices are insulated and switching loss unbalance is high (worst case). The conditions studied in this paper were carried out by mounting the paralleled devices in the chopper circuit shown in fig.20. Photo 8 shows the current balance improvement when the heatsink temperature increases (25°C - 100°C) and the devices are working in the chopper circuit.

The fig.21 shows the output characteristics of the paralleled devices and the estimated on-state current.

The fig.21 shows the output characteristics of the paralleled devices and the estimated on-state current.

The fig.21 shows the output characteristics of the paralleled devices and the estimated on-state current.

VI. IGBTs IN THE ISOTOP PACKAGE.

To reduce parameter spread, the IGBTs dice are mounted in the ISOTOP package with the "die sister" technique; the thermal resistance between the device junctions is reduced to a minimum and the gates are connected in parallel.

When the ISOTOP packages are paralleled, they give the following advantages:

- The small and compact size of the package (fig.22) and the low R_{thjc} value (0.5°C/W) give a minimal thermal resistance between the paralleled devices.
- This package was designed in order to minimize emitter ground wiring effects; In fact Isotop packages provide an auxiliary emitter pin which makes it simple to separate the driving circuit from the power circuit (fig.22,23).

Photo 9 & 10 show that unbalanced wiring connections have very little effect on the

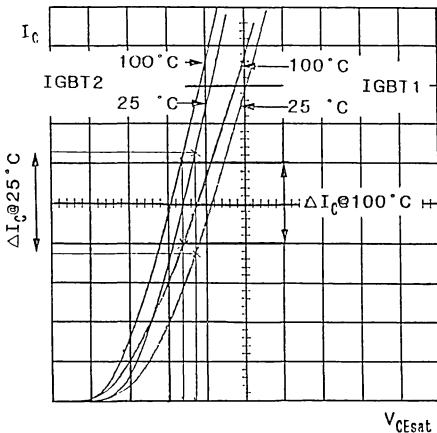


Fig.21. Output characteristics of the devices in fig. 20 and estimation of current balance at $T_{j1} = T_{j2} = 25^\circ C$ and $100^\circ C$.

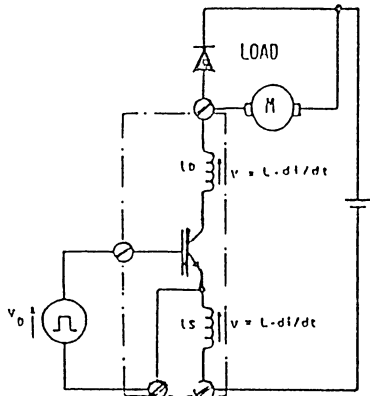
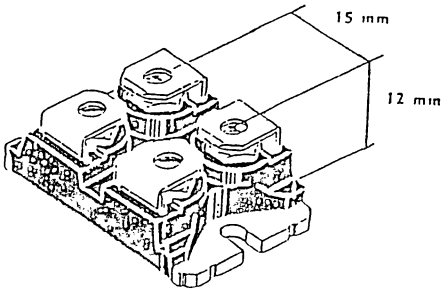


Fig. 22. Dimensions of the ISOTOP package and schematic diagram showing an auxiliary emitter pin.

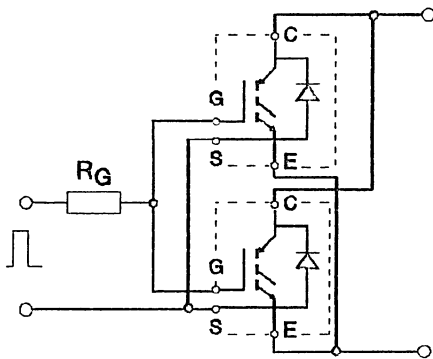


Fig. 23. Paralleling ISOTOP.

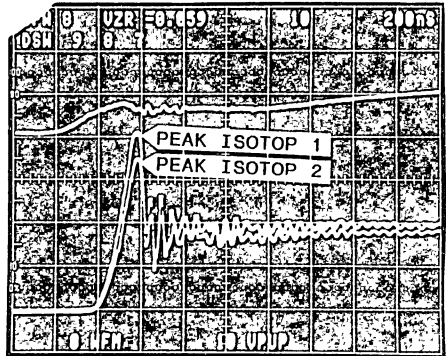


Photo 9. Turn-on of two TSG50N50DV with unbalanced emitter ground wiring. $I_C=25A/div$. $V_{GE}=10V/div$. $t=200ns/div$.

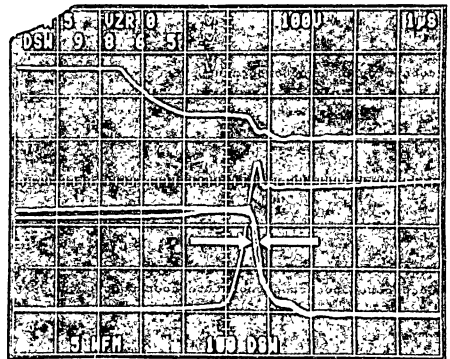


Photo 10. Turn-off of two paralleled TSG50N50DV. $I_C = 25A/div$. $V_{CE} = 100V/div$. $V_{GE} = 10div$. $t = 1\mu s/div$.

switching behaviour: the difference in length of emitter ground connections is 15 cm. It can be seen in photo 10 that there is no peak voltage due to di/dt ($V = L di/dt$) on the gate-emitter auxiliary pin during current rise.

VII. CONCLUSIONS.

The performances in terms of current balance, thermal stability and switching behaviour when SGS-THOMSON IGBT devices are paralleled, are very satisfactory.

The transfer characteristics has no real influence on current balance in the on-state.

The on state current and the switching current balance are ensured respectively by the low spread of the V_{CEsat} values and by the low spread of device parameters.

High thermal stability is obtained by mounting the paralleled devices on the same heatsink even when the devices are insulated (mica, insulated package).

For an optimum switching behaviour of paralleled devices, it is necessary:

- to drive the gates with only one gate resistance.
- to balance the emitter-ground wiring.

When IGBTs are in the ISOTOP package, the wiring unbalance tolerance is high and the thermal resistance (R_{thjh}) is low; thus, the advantages of the ISOTOP package are:

- easy to design the lay-out when paralleling IGBTs in ISOTOP.

- small thermal resistance between the junctions of paralleled devices; thus, temperature difference between the junction of the devices in parallel is reduced to a minimal value.

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- [5] **M. HIDESHIMA, T. KURAMOTO & A. NAKAGAWA**, "1000V 300A bipolar-mode mosfet (IGBT) module", Proceedings of 1988 International Symposium on Power Semiconductor Devices, Tokyo, pp. 80-85.



SWITCHING WITH IGBTs: HOW TO OBTAIN A BETTER PERFORMANCE

by A. Galluzzo, R. Letor, M. Melito

ABSTRACT

IGBTs are now being used in a variety of switching applications due to their attractive characteristics, particularly their current density, ruggedness and gate driving circuit. To exploit the best aspects of IGBTs it is necessary to understand how their switching performance can be controlled by the designer and how much the voltage and current waveforms can be shaped to obtain an acceptable compromise in terms of switching speed, ruggedness, power dissipation and EMI.

This paper, starting with voltage and current waveform analysis, highlights both the device and driving circuit characteristics which govern the switching. It suggests, by using a simple driving circuit, how to control both voltage and current slopes, independently.

The influence of negative gate bias and driving impedance versus dV/dt ruggedness are analyzed.

Finally the IGBTs switching behaviour, when connected in parallel, is examined.

1 - ANALYSIS OF PARAMETERS WHICH INFLUENCE SWITCHING WAVEFORMS

The switching behaviour of IGBTs is affected by the unavoidable parasitic capacitance of the structure. Moreover the turn-off losses are strongly dependent on the characteristic of the tailing effect on the collector current during turn-off. Nevertheless switching losses can be predicted and then limited to an acceptable value, that is compatible with the need for safe and noiseless switching. The main parameters governing switching behaviour: gate bias, driving impedance, stray inductances, gate charge must also be taken into account.

Fig. 1 shows a schematic circuit where the parasitic inductances which influence switching behaviour are highlighted.

In the following discussion it has been assumed that the stray inductances are small enough so that $dI/dt \gg V_{cc}/(L_s+L_c+L_d)$.

1.1 TURN-ON

When the freewheeling diode is conducting during turn-on switching (fig. 2) , increased losses occur in the diode if the dI/dt in the IGBT collector is increased. However the losses in the IGBT decrease with increasing dI/dt in the IGBT collector (fig. 3).

Reducing dI/dt leads to higher losses in the power switch but it makes the reverse recovery behaviour of the freewheeling diode softer, thus reducing EMI problems. Fig. 4 shows dI/dt versus R_g with L_s as a parameter. L_s includes both stray inductances due to package and external inductances due to source grounding layout. These inductances strongly influence dI/dt at turn-on because they act as negative feedback to the gate thus reducing the effective voltage applied to the device. This effect is emphasized in fig. 5 where the collector and gate current are shown.

The gate voltage was set at 15 V to give a low V_{cesat} and also because this value is applied as a standard gate voltage when various device characteristics are defined in data sheets.

1.2 TURN-OFF

The IGBTs turn-off (fig. 6) can be divided into three consecutive phases:

- a) the gate voltage begins to decrease until it reaches the value when the Miller effect occurs; during this phase the collector voltage increases slightly changing the output characteristics with $I_c = \text{constant}$.
- b) this phase is the Miller effect and the gate voltage remains constant because of modulation of the collector-gate capacitance.
This is due to collector voltage rapidly increasing to its maximum value.
- c) the collector current begins to fall quickly (it is related to the turn-off of the MOS part of the IGBT structure) then it continues with a "tail" which is due to recombination of minority carriers in the substrate.

This tail, which causes the major losses, is strongly related to technology and its effect can not be mitigated by driving circuit.

After the collector current, collector voltage and junction temperature has been determined, turn-off losses can be controlled only during phase b) varying dV/dt through R_g while losses occurring during phase c) are slightly influenced by the driving circuit.

Increasing dV/dt decreases losses but it is necessary to take care not to exceed the RBSOA boundaries which also depend on junction temperature, collector current and collector voltage.

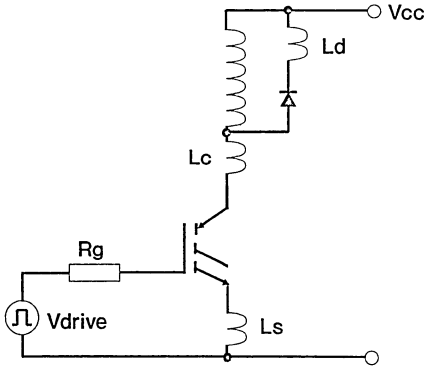


Fig. 1: Parasitic inductances influencing the switching behaviour

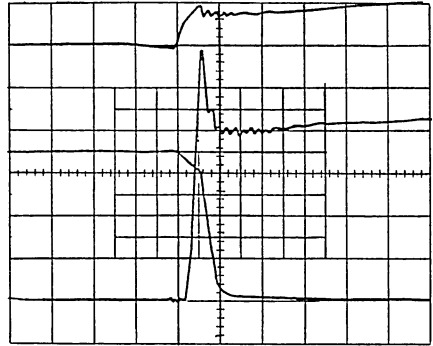


Fig. 2: Turn-on switching during freewheeling diode conduction

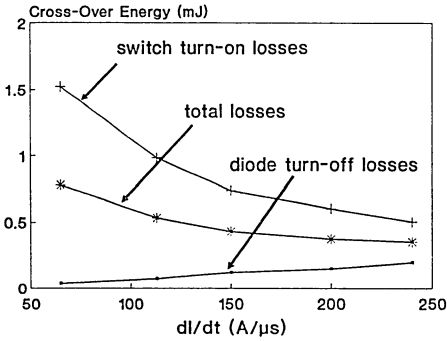


Fig. 3: Switching losses comparison

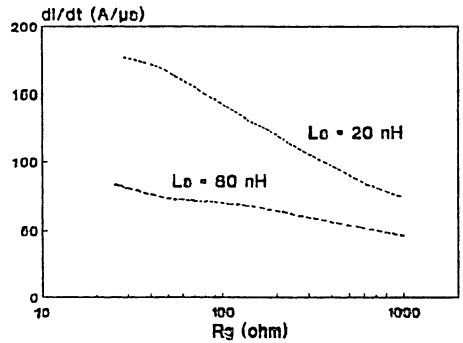
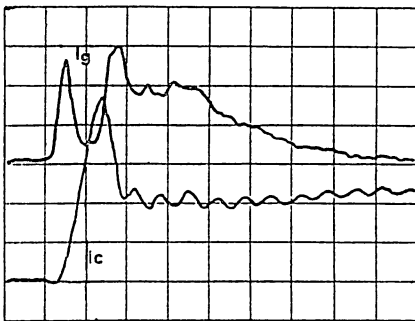


Fig. 4: Rg and Ls influence on di/dt during turn-on



nd Ig during turn-on

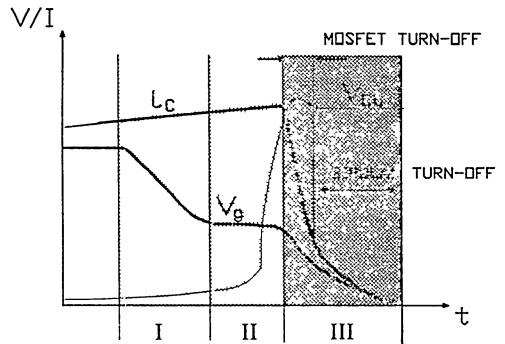


Fig. 6: IGBTs turn-off

2 - HOW TO MANAGE DI/DT AND DV/DT

Useful information about switching behaviour of IGBTs can be obtained from the gate charge curve. Even if the measuring conditions are quite different from the operating ones the total charge supplied to gate during switching is the same. The switching speed of a voltage driven device is strictly related to the rate of supplying charge to the gate input. This is true for IGBTs too, except during the falling edge of the collector current.

If we are able to control the rate of supplying this charge, i.e. if we can manage the amplitude of the gate current during switching we can independently vary both the voltage and the current slope.

2.2 TURN-ON

The driving circuit shown in fig. 7 allows di/dt to be varied through R1 but at the same time this resistance fixes the collector voltage slope. Increasing R1 leads to a lower di/dt and also to a lower dV/dt which increases turn-on losses.

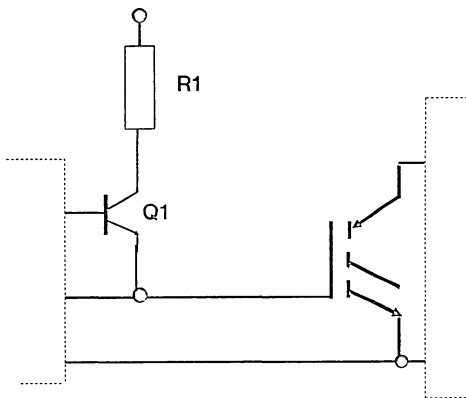


Fig. 7: Standard driving circuit

It would be useful to have a di/dt low enough to reduce EMI problems and a dV/dt fast enough to keep power losses to a minimum. It is possible to achieve that using a driving circuit which operates according to the schematic shown in fig. 8.

The current slope is fixed by R1 and voltage slope by R2 by turning Q2 on after Q1 with a suitable delay. The waveforms in figures 9a and 9b show the difference between the standard circuit and the improved version.

2.3 TURN-OFF

The driving circuit can only control the slope of the collector voltage (fig. 10) and only slightly influences the fall of the collector current which is responsible of the major losses due to the tailed turn-off.

Figures 11, 12 and 13 show the effect of V_c , I_c and T_j on the amplitude of the tail of the collector current.

To minimize turn-off losses it is best to choose a device whose characteristics matches better the required operating conditions in terms of V_c , I_c and T_j .

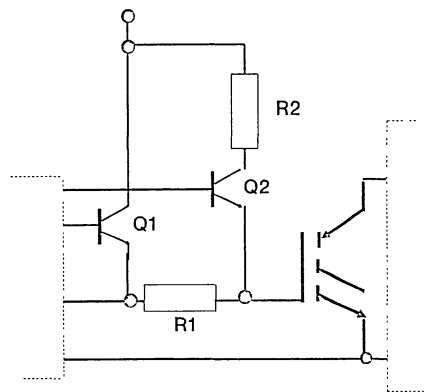


Fig. 8: Improved driving circuit

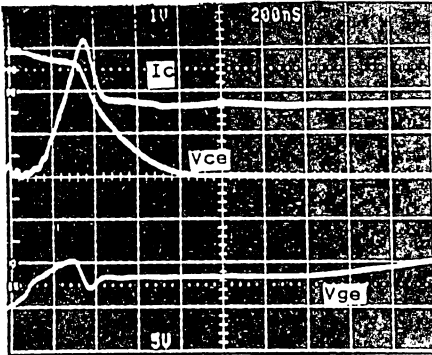


Fig. 9 a: Switching waveforms with standard driving circuit

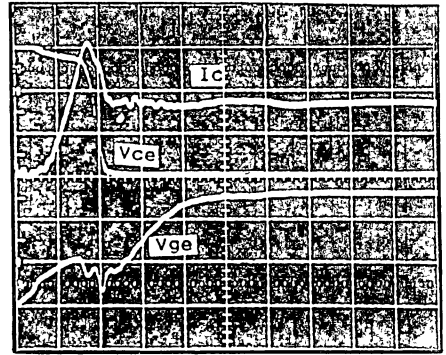


Fig. 9 b: Switching waveforms with improved driving circuit

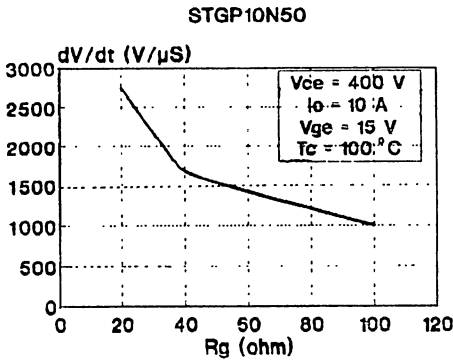


Fig. 10: Rg influence on dv/dt during turn-off

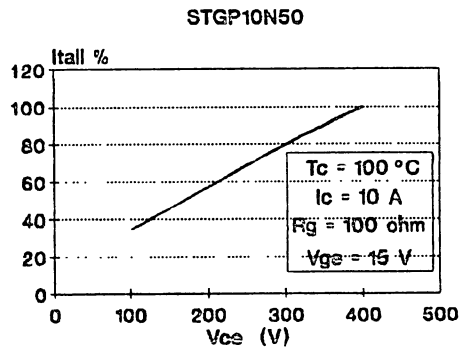


Fig. 11: I_{tail} versus collector voltage

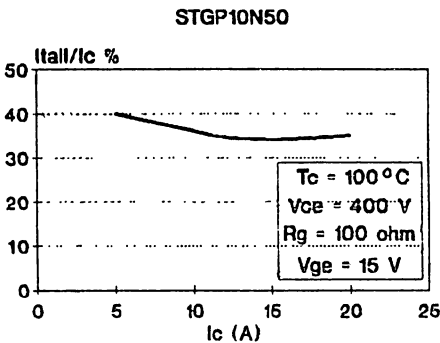


Fig. 12: I_{tail} versus collector current

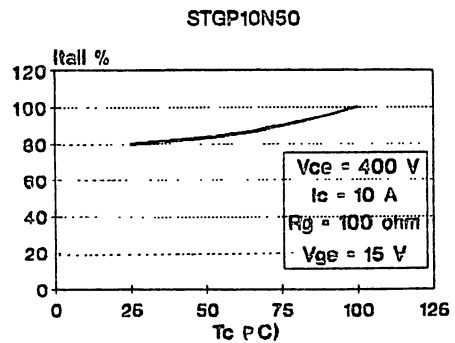


Fig. 13: I_{tail} versus Tj

3 - HOW TO AVOID DV/DT PROBLEMS

The spurious turn-on problem due to dV/dt is typical of the circuit shown in fig. 14.

The free-wheeling diodes in parallel with each IGBT are turned off during the opposite IGBT turn-on generating a dV/dt whose value depends on :

- opposite IGBT turn-on speed (di/dt)
- free-wheeling diode "softness"
- wiring inductances
- gate bias and driving impedance

This applied dv/dt , acting through the collector-gate capacitance (fig.15) causes the gate voltage to rise turning the device on and leading to additional losses. This undesired effect is emphasized when temperature increases because of temperature dependence of V_{th} and gfs .

It is possible to avoid this effect either minimizing the dv/dt value or making the device less sensitive to dV/dt by a driving circuit specifically designed for this purpose or combining the two techniques above mentioned.

The first item requires using fast soft recovery diodes, reducing wiring length and turning the IGBTs on slowly. The second one requires the driving impedance to be fixed at such low value that the gate voltage can not exceed the threshold voltage during dV/dt . The value of this driving impedance depends on die-size of the device: fig. 16 shows the R_{ge} needed to avoid spurious turn-on due to dv/dt .

Another way of avoiding spurious turn-on is to bias the gate negatively. Fig. 17 shows the different behaviour of gate voltage with and without negative bias.

The lower peak of the gate voltage is due to the different equivalent input capacitance when the gate is negatively biased.

4 - PARALLELED IGBTs SWITCHING BEHAVIOUR

The influence of the spread of parameters, of drive circuit and lay-out unbalance was investigated splitting the analysis as follows:

- a) driving IGBTs with one gate resistance for each device (fig. 18);
- b) driving IGBTs with a common gate resistance for all the devices (fig.19);
- c) unbalancing emitter wire connection (fig. 20);
- d) paralleling devices with the maximum spread of the parameters.

The performed analysis pointed out that voltage and collector current waveforms are stable even in the worst case conditions which occur when the gates are driven with a common resistance and the wiring inductances are strongly unbalanced.

In detail :

- IGBTs behaviour during turn-on is not very different in a) or b) conditions (fig. 21 and fig. 22).

If the paralleled devices have different storage times, driving the gates with one resistance for each device has the drawback shown in fig. 23: the collector current of the device having the smaller storage time begins to fall before the other one do.

Consequently, because of the inductive load, the 2nd IGBT has to switch-off a collector current greater than the other device thus increasing storage current unbalance. Driving the gates with only one gate resistance minimizes this effect (fig. 24): the device with the higher storage time holds the gate voltage to " $V_{th} + I_c/gfs$ " until the fall time phase, so equalizing the storage times.

- The effect of a poorly balanced emitter connection is highlighted during the rising and the falling edge of the collector current.

Fig. 25 shows the peak current unbalance, during turn-on, when the condition c) occurs. In the case shown $\Delta L_s = 0.15\mu\text{H}$.

Fig. 26 and fig. 27 show the corresponding effect during turn-off: wiring inductance imbalance affects only the power-MOSFET phase.

This behaviour creates negligible switching losses imbalance compared with the total turn-off ones. The current unbalance just before current fall affects the tail amplitude and it can create significant imbalance in the switching losses.

- IGBTs with the maximum spread in parameter values were paralleled; the comparison of current waveforms in fig. 21 and fig. 22 demonstrates that, during turn-on, the influence of parameter spread is low ($L_s \approx 30\text{ nH}$).

The spread of IGBTs parameters (g_{fs} , V_{th} , gate-charge) leads to different storage times and causes current imbalance thus creating switching losses imbalance.

Current imbalance due to the IGBTs parameter spread can be calculated with the equations (2) and (3).

The curve of fig. 28 shows the imbalance in switching losses between two devices where the V_{th} and g_{fs} values are the limits of the parameter spread.

$$I_{load} = I_{1st} + I_{2st} = V_{GE} (g_{fs1} + g_{fs2}) - (g_{fs1}V_{th1} + g_{fs2}V_{th2}) \quad (2)$$

$$I_{storage} = I_{1st} - I_{2st} = V_{GE} (g_{fs1} - g_{fs2}) - (g_{fs1}V_{th1} - g_{fs2}V_{th2}) \quad (3)$$

CONCLUSION

A careful analysis of circuit and device parameters, influencing switching waveforms, was carried out taking into account negative

gate bias, dV/dt influence and effects of device paralleling.

The following statements were explained:

- it is possible to manage separately both the current and the voltage slope except the collector current tail;

- negative gate bias reduces spurious turn on caused by dV/dt in bridge configurations;

- negative gate bias without R_g adjustment reduces the RBSOA because of increased dV/dt ;

- common resistor on the gate of paralleled devices improves switching losses balance;

- stray inductance on emitter connection reduces switching speed and can causes losses unbalance in paralleled devices;

Performance improvements obtained by optimization of gate driving circuit involve cost increases. It is task of the system designer to define a good trade off between cost and performances.

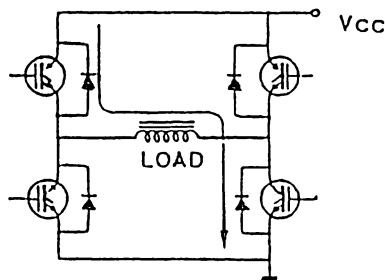


Fig. 14: Typical circuit where dV/dt conduction can occur

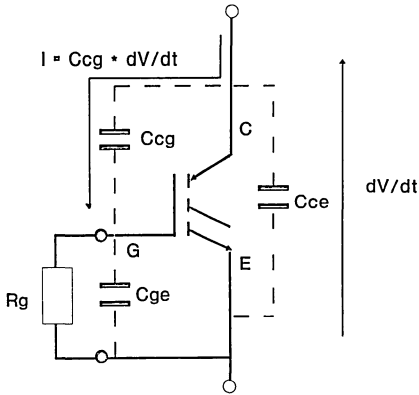


Fig. 15: Current flow through IGBT capacitance due to dV/dt

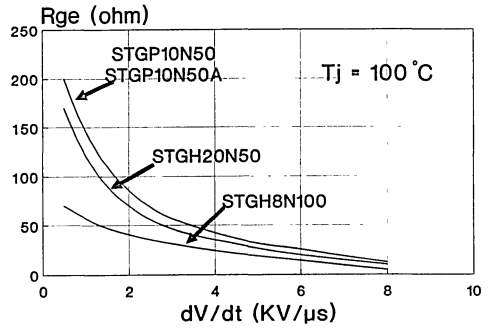


Fig. 16: Rge values that avoid dV/dt conduction versus dV/dt

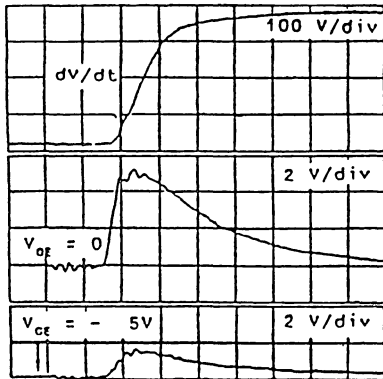


Fig. 17: Comparison of gate voltage behaviour with and without negative bias

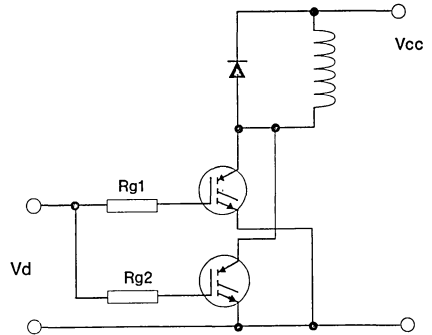


Fig. 18: Driving with separate gate resistance

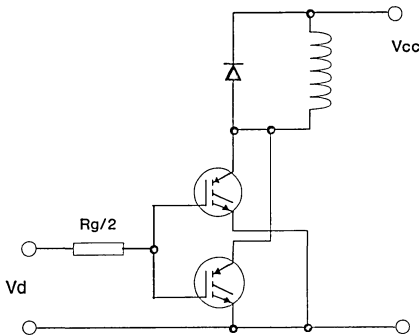


Fig. 19: Driving with one gate resistance

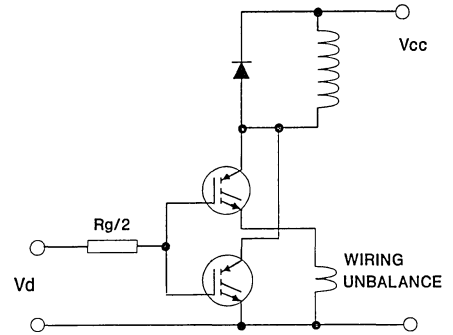


Fig. 20: Emitter grounding unbalance

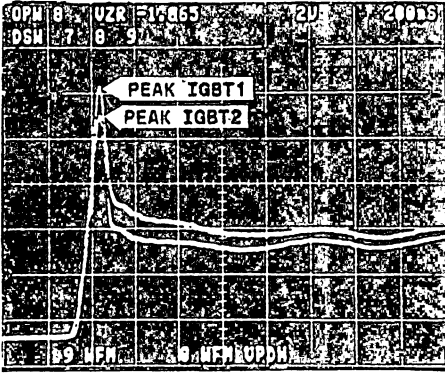


Fig. 21: Turn-on with separate gate drive (fig. 18) of an STGH8N100. $I_c = 2A/div$

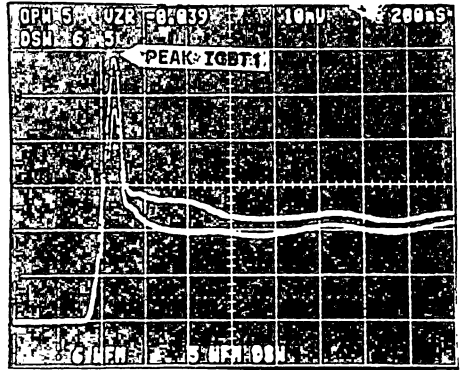


Fig. 22: Turn-on with one gate resistance (fig. 19) of an STGH8N100. $I_c = 2A/div$

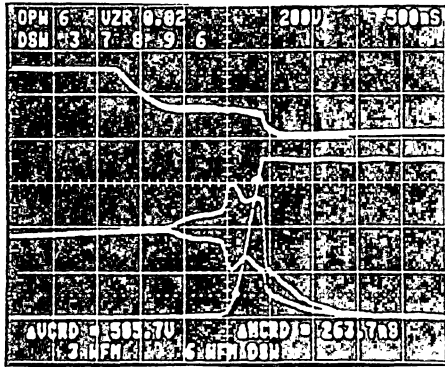


Fig. 23: Effect of separate gate drive on storage current waveforms. $I_c = 2A/div$, $V_{ce} = 200/div$, $V_{ge} = 10/div$

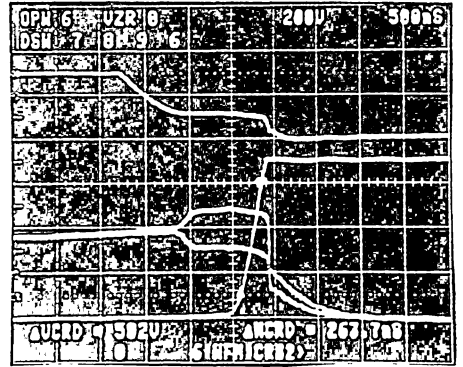


Fig. 24: Turn-off with one gate resistance. $I_c = 2A/div$, $V_{ce} = 200/div$, $V_{ge} = 10/div$

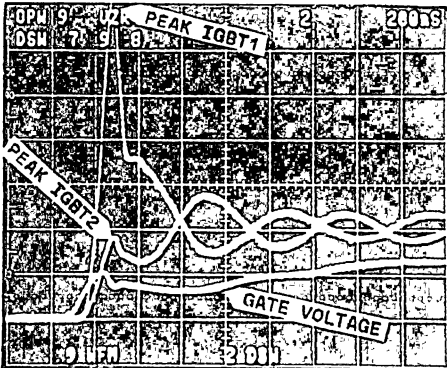


Fig. 25: Turn-on with unbalanced emitter-ground connection (fig. 20). $I_c = 2A/div$

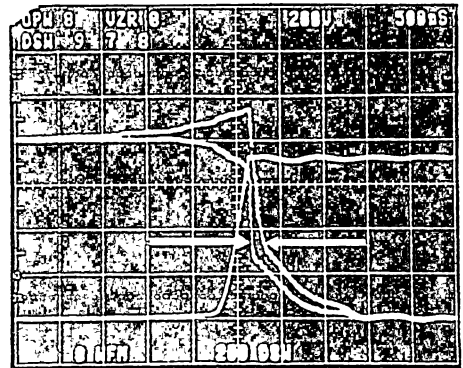


Fig. 26: Turn-off with unbalanced emitter-ground connection (fig. 20). $I_c = 2A/div$

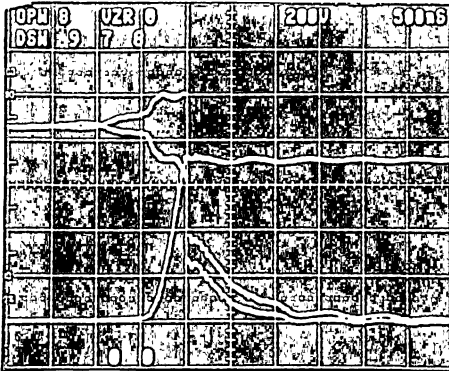


Fig. 27: Turn-off current waveforms with balanced gate-emitter wiring (fig. 19). $I_c = 2A/div$

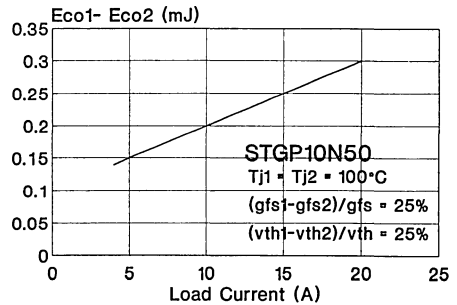


Fig. 28: Switching losses unbalance

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AN ANALYSIS OF LOSSES IN AN IGBT

by P. Fichera

1. INTRODUCTION

Insulated gate bipolar transistors are now being used in a variety of switching applications. These range from automotive ignition, where they replace the mechanical contact breaker, to electric motor drives, where they provide an economic, easy to drive chopper switch with high voltage capability.

More recently work has been done in using these devices in various types of power supplies.

They are attractive to use due to the high

impedance input, a MOS gate that requires a minimum of only 8V and microjoules of energy to turn it on and off and the bipolar nature of the output that makes them capable of controlling high current densities.

To obtain the optimum performance from IGBTs it is necessary to understand the limits imposed by the structure of the device and their particular operating conditions.

This paper looks at the use of IGBTs in chopper circuits and shows how to evaluate the losses during switching and conduction.

2. LIMITING FACTORS FOR IGBTs IN CHOPPER CIRCUITS

Chopper circuits operate at frequencies determined by the nature of the application and of the power switch employed to control the current flow. As is the case with Power MOSFETs, power is dissipated in IGBTs at turn-on of the device, during conduction and at turn-off. The major difference between IGBT and Power MOSFET switching losses occurs in the turn-off switching behaviour. Figure 1 illustrates the typical losses for an IGBT used in a chopper application.

2.1 TURN-ON LOSSES

It is not sufficient to know the rise time, t_r , of the turn-on current. The free-wheeling diode used in conjunction with the IGBT, figure 8, is responsible for a large amount of the losses as a result of its reverse recovery current. Within a given application it is necessary to know the $(di_D/dt)_{on}$ for this diode in order to evaluate the reverse recovery current, I_{RM} . Once I_{RM} is known it is possible to calculate the turn-on losses.

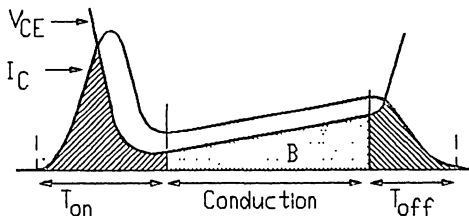


Fig. 1 - Typical IGBT losses

2.2 CONDUCTION LOSSES

The following simple expression shows how to calculate the conduction losses.

$$P_{on} = E_o I_{AVG} + R_o I_{RMS}^2$$

where:

P_{on} = on-state power dissipation

I_{RMS} = RMS current value for the application

I_{AVG} = average current value of the application

E_o, R_o = are parameters defined by the IGBT output characteristic I_C, V_{ce} - see figure 2.

E_o = abscissa of the intersection between the tangent to the output characteristic calculated at $I_C = I_o$ and the V_{ce} axis.

R_o = inverse slope of the tangent to the output characteristic curve I_C, V_{CE} , calculated at $I_C = I_o$.

The area B in figure 1 illustrates these losses.

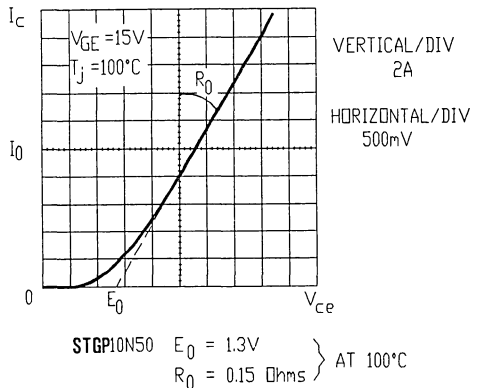


Fig. 2 - Output characteristics of STGP10N50

2.3 TURN-OFF LOSSES

Calculation of the turn-off losses in an IGBT requires more information than just the fall time, t_f . On its own it leads to erroneous results. It is necessary to know how other parameters influence these losses.

Most care has to be taken with the current tail phenomenon of the IGBT when it is operated in hard switching. Two parameters define the current tail: its amplitude, I_t , and its duration, t_t .

A) THE INFLUENCE OF THE SUPPLY VOLTAGE ON TURN-OFF LOSSES.

The supply voltage and the current tail amplitude are directly proportional. However, the duration of the tail remains almost constant when the supply voltage is varied.

B) THE INFLUENCE OF DV/DT ON THE TURN-OFF LOSSES

A low dV/dt value at turn-off (imposed by an external circuit, e.g. a snubber) reduces the current tail amplitude, I_t . The tail duration does not change when dV/dt is varied.

C) THE INFLUENCE OF TEMPERATURE ON TURN-OFF LOSSES.

Operating temperature affects the duration and amplitude of I_t and t_t . Experimental analysis shows that both increase in value by the same percentage as the temperature increases.

D) THE INFLUENCE OF THE GATE RESISTANCE, $R_{g(off)}$.

The gate resistance does not affect the current tail. Varying $R_{g(off)}$ controls the slope of dV/dt at turn off and consequently can give some reduction in the turn-off losses. A minimum value of $R_{g(off)}$ is required to prevent oscillations occurring during turn-off (as is the case with power MOSFETs).

5 CALCULATING CONDUCTION LOSSES

When calculating conduction losses at 100°C it is better to base the calculation on the output characteristics of the IGBT (I_c versus V_{ce}) at a given V_{ge} .

Table 1. *Additional parameters required to calculate turn-off losses in IGBTs.*

V	- the re-applied supply voltage
dV/dt	- slope of re-applied supply voltage
T_j	- junction temperature
$R_{g(off)}$	- gate resistance at turn off.

3. SAMPLE CALCULATIONS.

It is possible, using the curves given in figure 9 and the energy curves characteristic of figure 10 for different operating conditions, to calculate the switching losses for a given set of conditions. This in turn allows the maximum operating frequency for the IGBT to be calculated.

The basic circuit in figure 8 shows the configuration used for the STGP10N50 500V, 10A IGBT and its switching waveforms.

3.1 CALCULATION OF THE TURN-ON LOSSES AT $T_j = 100^\circ\text{C}$.

The value of the gate resistor during turn-on is 47 Ohms. Using the graph in figure 9a this gives a value for dI_D/dt_{on} of 100A/ μs . As the IGBT controls dI/dt it follows that the recovery current of the free-wheeling diode can be determined from the diode datasheet (graph of I_{RM} versus dI/dt is shown in figure 9b). This gives a value of $I_{RM} = 10\text{A}$.

Applying the formula for the turn-on losses:

$$W_{t(on)} = 1/2 V_{supply} (I_O + I_{RM})^2 \cdot 1/(dI/dt)_{on}$$

$$W_{t(on)} \text{ is calculated to be: } W_{t(on)} = 0.4\text{mJ}$$

3.2 CALCULATION OF CONDUCTION LOSSES AT $T_j = 100^\circ\text{C}$.

The value of the parameters E_o and R_o have been evaluated from the graph of I_c versus V_{ce} shown in figure 2.

$$E_o = 1.3\text{V}$$

$$R_o = 0.15 \text{ Ohms}$$

Taking I_{AVG} to be 3.5A and I_{RMS} as 5.8A, P_{on} can be calculated using the equation from section 2.2

$$P_{on} = 9.6\text{W}$$

3.3 CALCULATION OF THE TURN-OFF LOSSES.

A. High dV/dt (2500V/ μs)

Using a value for $R_{g(off)} = 47\text{Ohms}$ and taking into account the dV/dt curve of figure 10 a; at a switched current of 10A the energy dissipated in turning off is

$$W_{t(off)} = 1.1 \text{ mJ/cycle}$$

B. LOW dV/dt (500V/ μs)

Using $R_{g(off)} = 47 \text{ Ohms}$ and switched current of 10A again

$$W_{t(off)} = 0.3 \text{ mJ/cycle.}$$

Summarising these values show that the total power dissipated is dependent on the operating frequency.

Accepting that the maximum power that can be dissipated from the device at 100°C is 40 Watts for this device in a TO-220 package, it is simple to calculate that using high dV/dt the IGBT has an upper limit of operation of 20kHz while with low dV/dt operation is possible up to 40kHz.

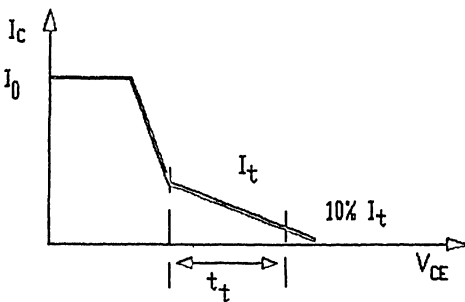


Fig. 3 - Turn-off losses

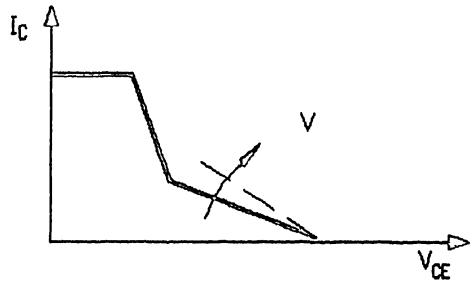


Fig. 4 - Influence of supply voltage on turn-off losses

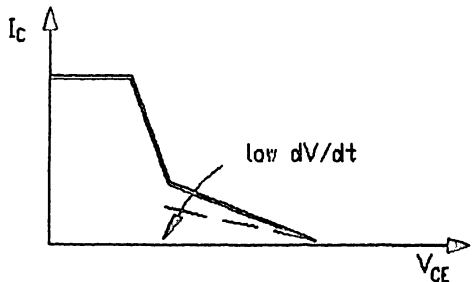


Fig. 5 - dV/dt effect

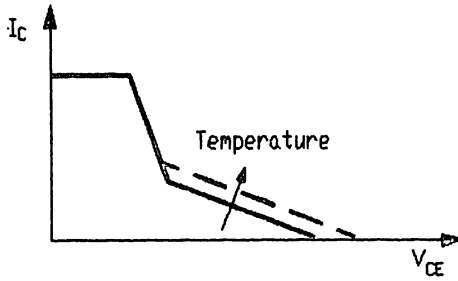


Fig. 6 - The effect of temperature on I_t and t_t

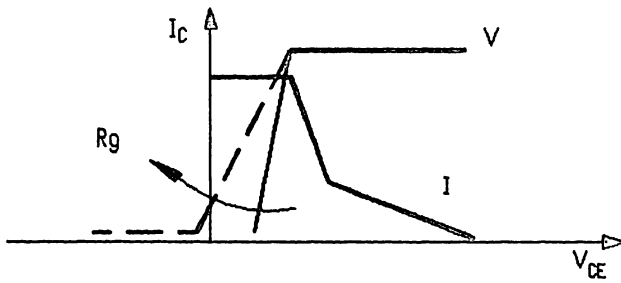


Fig. 7 - The influence of gate resistance

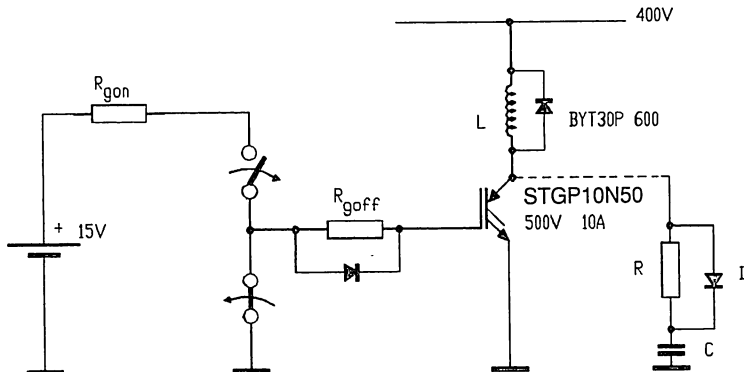
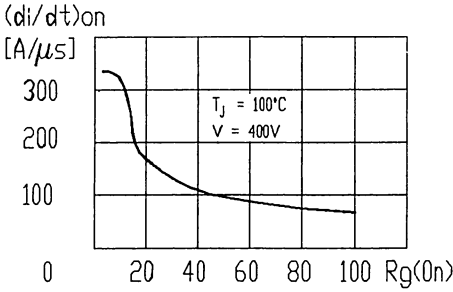
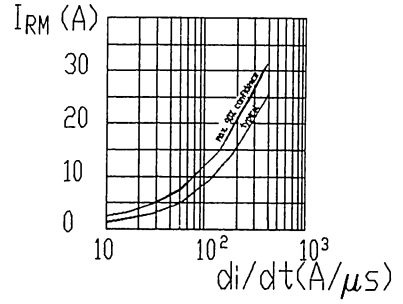


Fig. 8 - Basic circuit

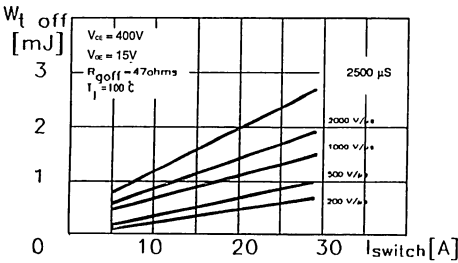


9a

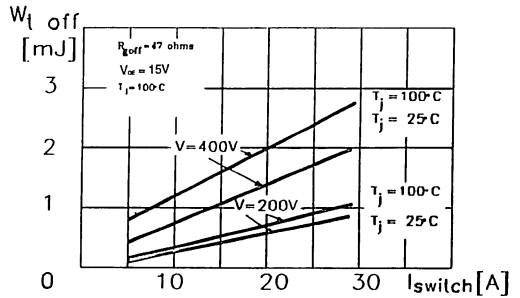


9b

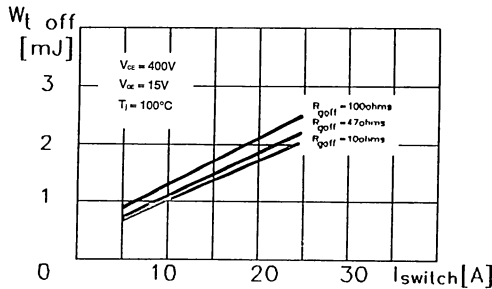
Fig. 9



(a) influence of dv/dt



(b) influence of Tj and V supply



(c) influence of Rgoff, gate resistance at turn-off

Fig. 10 (a,b,c) - Controlling factors for turn-off losses in a "2nd generation"500V/10A IGBT

	Wt(on)+Wt(off)	P(on)	Total Power Dissipated
High dV/dt	1.5mJ/cycle	9.6W	$1.5 \cdot 10^{-3} \cdot \text{frequency} + 9.6 \text{ W}$
Low dV/dt	0.7mJ/cycle	9.6W	$0.7 \cdot 10^{-3} \cdot \text{frequency} + 9.6 \text{ W}$

4. CONCLUSION

IGBTs are rugged, easy to drive and cost effective switches for high voltage chopper applications. They are capable of sustaining high current densities. Their operating frequency has been shown to be dependent on the operating conditions and a straight

forward method of estimating this was discussed.

For applications such as motor drives they are robust and reliable alternatives to bipolar transistors and Power MOSFETs.



**SEMICONDUCTOR DEVICES
BIPOLAR TRANSISTORS**

**BIPOLAR TRANSISTORS AND DARLINGTONS-
DESIGN FUNCTION DRIVE AND PROTECTION**

by **K. Rischmuller**

1. INTRODUCTION

The field of applications open to bipolar transistors and Darlington's is wide. They are used as circuit breakers in ignition systems, in switch mode power supplies with output powers up to 100kW and in converters where they switch currents of several hundred amperes at voltages of up to 1000V. The common switching frequency range is from several tens of Hz in an automobile ignition system to over 100kHz in resonance converters on the 380/440V industrial mains supply.

Technology and circuit design have a major effect on the switching behaviour and load line capabilities of bipolar transistors. They cannot be used to the full without knowledge of their technology and the drive and protection methods they require. This

Figure 1 : Cross Section of a Transistor with (a) a high blocking voltage and (b) a low blocking voltage. The resistance of the n-collector layer of the high voltage transistor is considerably higher.

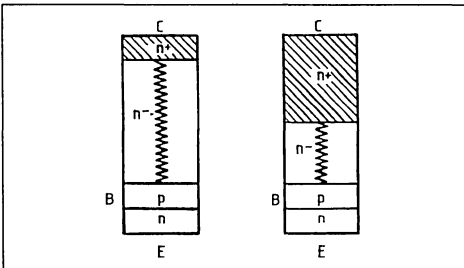
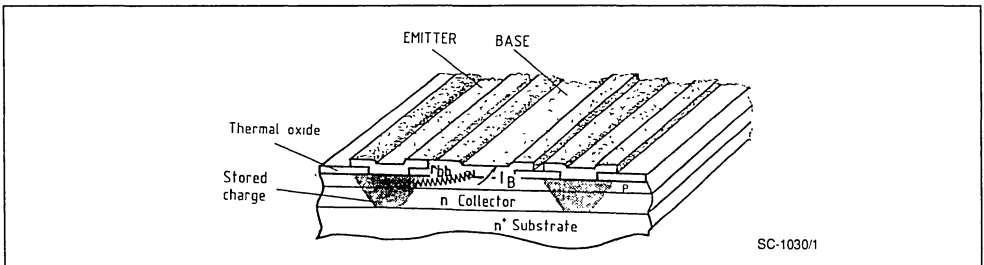


Figure 3 : Emitter-like Fingers in a Conventional Bipolar Transistor. The base current flows through the parasitic base resistance, r_{bb} .



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paper attempts to furnish or refresh this knowledge. It also discusses new developments in component technology and applications.

2. DESIGN OF BIPOLAR TRANSISTORS

2.1 VERTICAL STRUCTURE

The properties of NPN bipolar transistors can be described with the aid of a simple model. Figure 1 is a simplified section through an NPN transistor with (a) a high blocking voltage and (b) a low blocking voltage. At the bottom is the n-emitter followed by the p-base and on the top, the n-collector. The difference between the two transistors lies in the thickness and the resistivity of the n-collector layer. The individual layers influence the transistor's properties as follows :

Figure 2 : Current gain as a function of the collector current of transistors with high and low voltage ratings. The current gain of the high voltage transistor decreases rapidly at high collector currents.

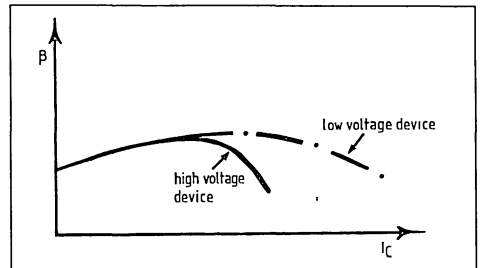
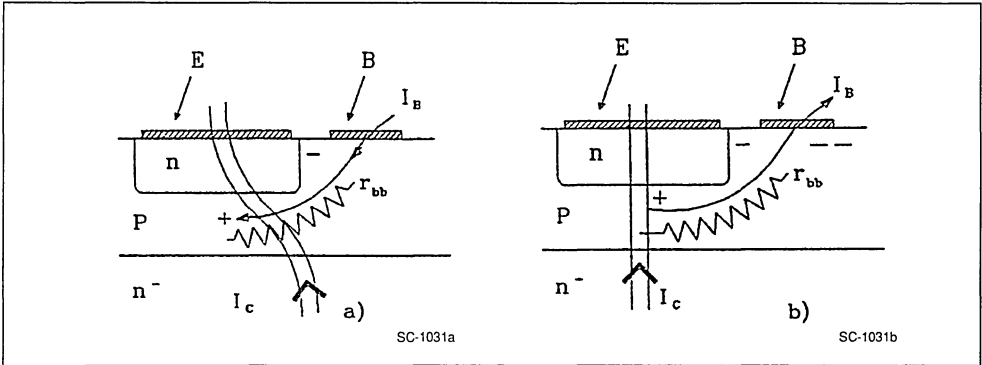


Figure 4 : The voltage drop at the parasitic base resistor, r_{bb} , leads to heterogeneous current distribution.
 a) Positive base current : current flow at the edge of the emitter finger.
 b) Negative base current : current focusing under the middle of the emitter finger.



The emitter-base doping profile determines current gain at low to medium collector currents. The thickness and doping of the p-base influence current gain, switching times and the safe operating area in the switching mode. The n-collector layer determines the blocking voltage of the transistor. The blocking voltage is increased twofold by doubling both the thickness and the resistivity of the collector layer. The internal resistance of the n-layer thus increases with roughly the square of the blocking voltage. As a result of high resistivity in the collector layer the current gain at high collector currents is reduced, figure 2. A transistor with high blocking voltage therefore requires more base current to reach saturation than a comparable transistor with a low blocking voltage. A high voltage transistor stores more minority carriers in the n-collector layer. These carriers have to be injected to switch the transistor on and removed to switch it off. With a given base current this takes more time with a high voltage transistor than with a low voltage transistor. Hence a high voltage transistor is "slower" than a transistor with a low blocking voltage.

2.2 HORIZONTAL STRUCTURE

To produce a conventional bipolar transistor, interdigitated emitter fingers are diffused into the base layer and contacted by a finger-like metallization, figure 3. A second finger-like metallization establishes contact to the base. The base layer below the

emitter is resistive and forms a resistor. (This resistance is referred to throughout this text as the parasitic base resistor, r_{bb} .) If the transistor is turned-on by a positive base current a voltage difference appears across the parasitic base resistance, r_{bb} polarising the edge zone of the emitter fingers to a larger extent than the middle of the emitter finger. Current distribution in the transistor becomes heterogeneous, figure 4.

Turn-off with a negative base current causes a voltage drop that first blocks the edge and then the centre of the emitter finger, figure 4b. This effect is known as "current focusing". It makes the energy stress in the transistor heterogeneous during turn-off switching, thus reducing the components power handling ability.

The driver circuit can be adapted so as to minimise the current focusing effect. "Soft" driving with a relatively low negative base current produces a less severe voltage drop across r_{bb} , which in turn means less current focusing, increasing the transistors power handling ability. However, this drive method also prolongs the turn-off delay, ("storage time").

The designers of modern bipolar transistors opt for reducing the effective width, w , of the emitter fingers, thus reducing the parasitic base resistance. This measure improves switching times and increases the power handling capability of the transistor.

Figure 5 : Section through the emitter finger of (a) a conventional transistor, (b) a hollow-emitter transistor. The central zone of the hollow emitter transistor is masked ; current focusing cannot occur.

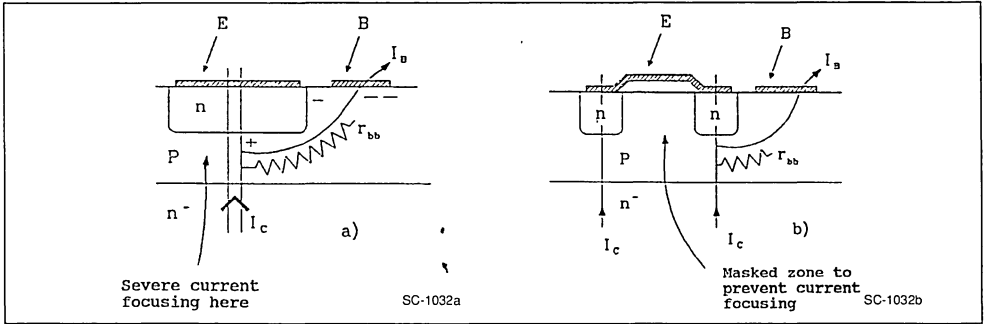


Figure 6 : Section Through a Cellular ETD Transistor. Due to the small cells the parasitic base resistance is negligibly small.

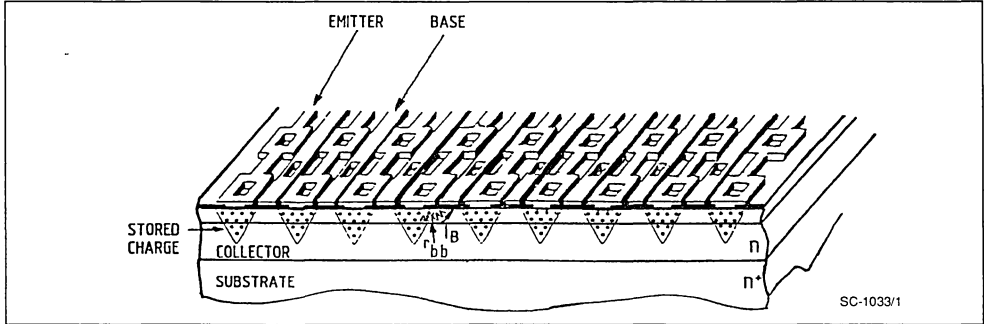


Figure 7 : Saturation States of a High Voltage Transistor.

- a) active,
- b) quasi-saturated,
- c) saturated,
- d) over-saturated.

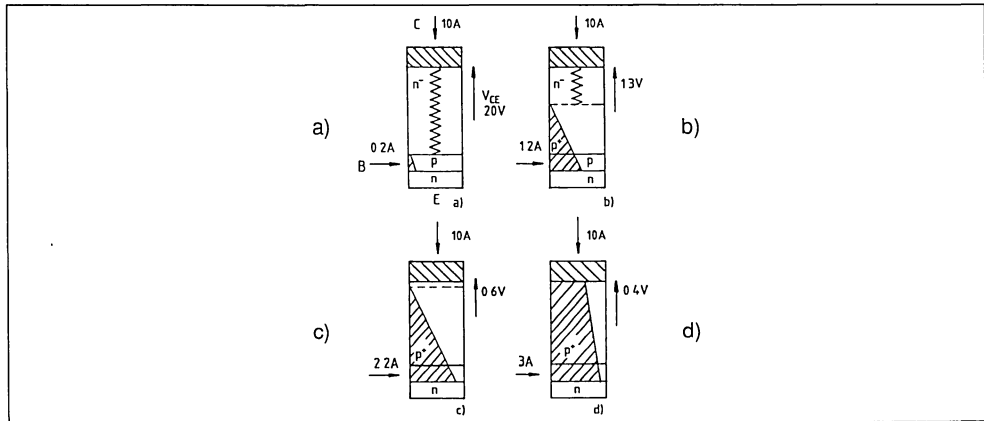
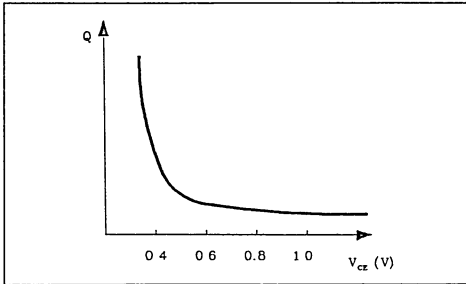


Figure 8 : Transistor in the on-state ; stored charge is very large if the collector-emitter voltage is very small. The resultant turn-off delay depends on the stored charge.



The introduction of the hollow-emitter and cellular ETD technologies has meant further advances.^{1 2} In a hollow-emitter transistor, the central zone of the emitter finger is masked, with the result that no significant current focusing can take place during turn-off, figure 5. In a cellular ETD transistor a large number of extremely small transistors are connected in parallel, figure 6. Each cell is so small that the parasitic resistance is negligible. The structure of ring-emitter transistors is similar to that of cellular ETD transistors. In these transistors, the base and emitter are contacted by two superimposed, mutually insulated metal layers. These transistors also have very low parasitic base resistance.

3. CONDUCTION

When in conduction, a transistor may have different saturation states which are dependent on the base current, figure 7. These different saturation states lead to different conduction losses and switching times.

3.1 ACTIVE STATE, figure 7a

If we provide a positive base current of a certain value to a transistor, the collector current will reach the value : base current x current gain of the transistor. The collector emitter voltage may reach 20V. In this state of conduction there are a very small number of carriers in the transistor, consequently the transistor reacts to any variation of the base current with a quasi-spontaneous change in collector current.

3.2 Quasi-saturation, figure 7b.

If the base current is further increased, more minority carriers are injected into the n-doped collector region.

This reduces the on-resistance of this layer, which in turn reduces the collector-emitter voltage drop.

3.3 SATURATION, figure 7c.

With more base current, the transistor becomes saturated. The entire n-collector layer is flooded with injected p-carriers and attains an extremely low resistance. The collector emitter voltage is now no more than a few 100mV. The advantage of this low voltage drop is counter-balanced by a high base current and longer turn-off switching times.

3.4 OVER-SATURATION, figure 7d.

Any further increase in the base current will not significantly reduce the collector-emitter voltage. At the same time the number of minority carriers and the resultant turn-off delay are much increased, figure 8. The reverse-biased safe operating area (RBSOA) may be reduced when switching off from over-saturation.³

In Darlington configuration, the collector-emitter voltage is always higher than the base-emitter voltage of the output transistor, T2 - figure 9. The output transistor always operates in quasi-saturation and behaves accordingly. Depending on how it is driven, the first stage, T1, may be quasi-saturated or over-saturated. The turn-off delay time of a Darlington is thus determined primarily by the turn-off delay of the first stage transistor. The collector current fall time depends on the output transistor.

3.5 CONDUCTION LOSSES

Conduction losses are the sum of the loss, P_c , on the collector-emitter junction and the loss, P_{dp} in the driver circuit. These two losses are interdependent. An increase of the positive base current will reduce the collector-emitter voltage, figure 10. A higher base current results in higher driving losses and longer turn-off delay times. In any application a compromise has to be found between low driving losses, low losses across the collector-emitter and switching speed.

The base current should be matched to the collector current flowing at any given time. For low conduction losses the auxiliary voltage, V_{aux} , should have the lowest acceptable value. However, during turn-on switching the driver circuit should act as a current source. Some examples of driver circuits with low conduction losses are described below.

Figure 9 : Voltages in a Darlington Configuration in the On-state ;
 a) first stage, T1, saturated,
 b) first stage, T1, quasi-saturated.

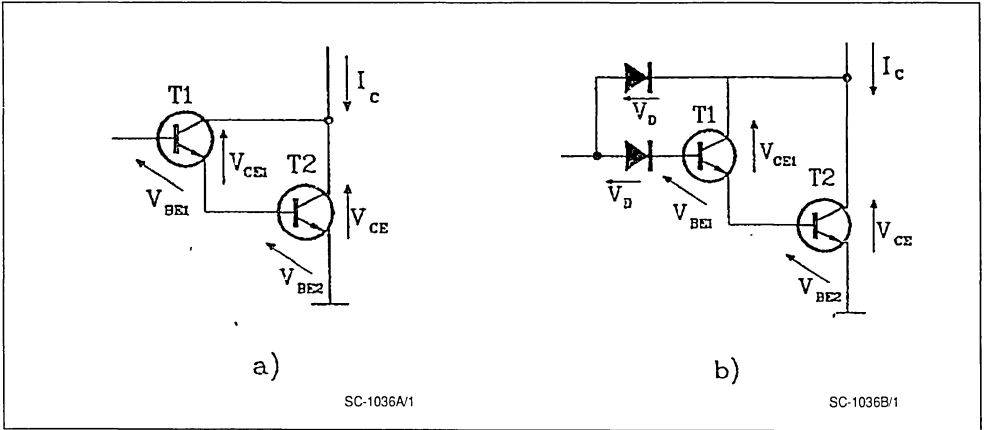
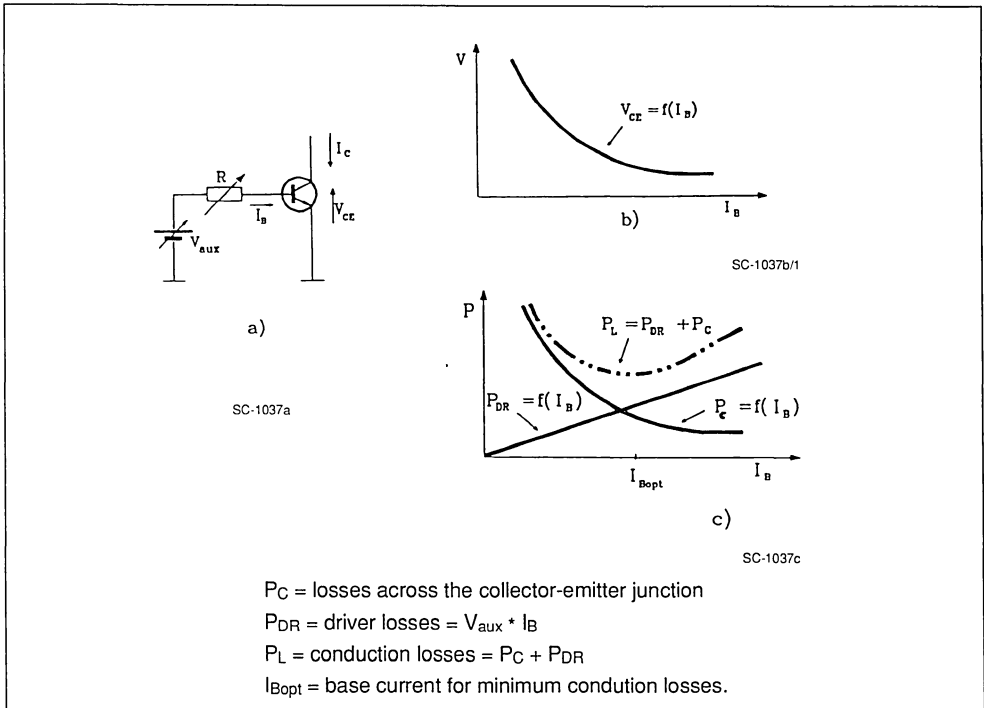


Figure 10 : Conduction losses as functions of base Current ;
 a) test circuit,
 b) collector-emitter voltage V_{CE} as function of base current,
 c) conduction losses as a function of base current.



4. TURN-ON AND TURN-OFF SWITCHING

For fast and low loss turn-on switching carriers have to be injected very rapidly into the base of the transistor. For this reason the positive base current has to rapidly reach a sufficient amplitude. After the turn-on transition the amplitude of the positive base current may be reduced.

4.1 INFLUENCE OF CIRCUIT PARAMETERS

The rate of rise of the base current is limited by parasitic inductances and by the dynamic response of the base-emitter junction. At the beginning of turn-on switching the value of r_{bb} is relatively high ; its value decreases after several tens of nanoseconds.

If the transistor is driven from a driver with a low supply voltage, the rate of rise of the base current is limited by the parasitic base resistance. If the driver

stage acts as a current source, the rate of rise of the base current is determined by the driver stage and not by the dynamic response of r_{bb} .

In circuits without switching aid networks the rate of rise of the collector current should be as high as possible. If there is a parasitic inductance in series with the emitter connection and if both the collector and base currents flow through this inductance, a voltage appears in opposition to the driver voltage. This reduces the rate of rise of the base current and consequently of the collector current.

INFLUENCE OF DEVICE DESIGN

The parasitic base resistance of advanced bipolar transistors has been reduced by means of fine finger or fine cellular structures. This is the reason why they are capable of very high switching speeds.

Figure 11 : Rate of rise of positive base current when the driver circuit acts as
 a) a voltage source.
 b) a current source.

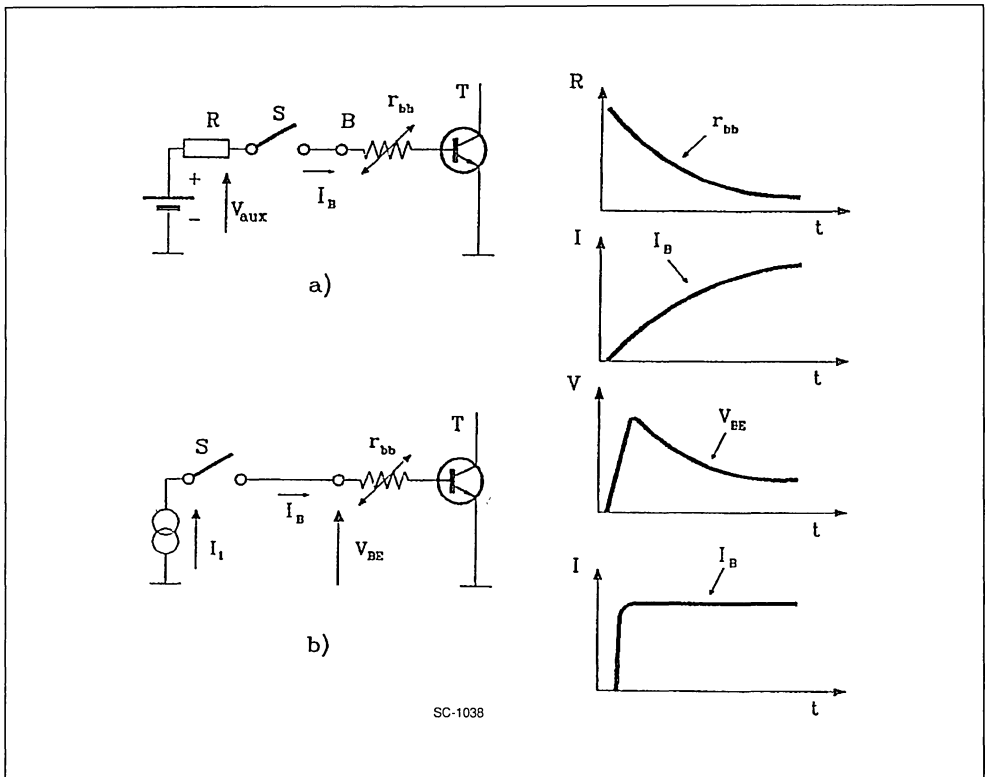
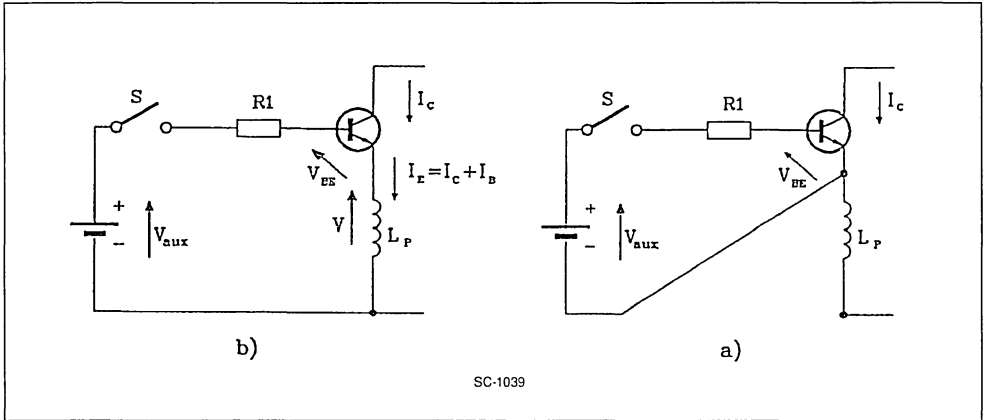


Figure 12 : Effect of a Parasitic Inductance in the Emitter Circuit.

- The base current and the collector current flow through the inductance. the feedback effect may lead to a greatly increased switching time.
- The driver circuit is directly connected to the emitter of the power transistor. The feedback effect of the parasitic inductance becomes negligible.



SC-1039

Darlington's have a particularly high rate of rise of current which is explained as follows. During turn-on switching, and especially during the reverse recovery time of the free-wheeling diode, a voltage that can be as high as several hundred volts is applied between the collector and emitter of the Darlington. At high collector-emitter voltages, the first stage of the Darlington has a large current gain and thus imposes a fast positive base current with a high amplitude to the output stage, figure 13.

The turn-on speed di_c/dt of Darlington's is excessive for some applications. In this case the measures explained in paragraph 8.2 can be used to reduce the speed.

For fast switching and for high switching frequency low inductance wiring is required. In any case it is best to use transistors, Darlington's and fast diodes in low inductance packages. The TO-220 (ISO-WATT220), TO-218 (ISOWATT218) and ISOTOP packages exhibit such low parasitic inductance.

5. TURN-OFF SWITCHING

5.1 INFLUENCE OF THE CIRCUIT

The transistor's behaviour during turn-off switching depends on the negative base current and the saturation state that existed during conduction. When an

over saturated transistor is turned off, more charge has to be removed than is the case when the transistor is quasi-saturated. The higher the amplitude of the negative base current I_{B2} and the lower the transistor's degree of saturation, the shorter is the turn-off delay and storage time, figure 14.

If the transistor is switched on for only a few μs , it does not reach saturation and remains in the active region. The turn-off delay is then considerably shorter than the storage time specified in the data sheet, figure 26. This is why, in the data sheet of modern transistors, the storage time is specified as a function of conduction time. (See the extract from data sheet for BUF410 for an example, figure 14b.). The turn-off delay time for a pulse width in the region of $10 \mu s$ is a few μs , reducing to no more than a few hundred nanoseconds for pulse widths of around $1 \mu s$.²

The amplitude of the negative base current I_{B3} sets the fall time t_p . The higher the negative current during the fall time t_p , the shorter is the fall time. When an over saturated transistor is switched off, a very high negative base current can cause a tail of the collector current and reduce the safe operating area⁵. Hence a high negative base current should be applied only when a quasi-saturated transistor is switched off.

Figure 13 : Turn-on Switching of Darlings and MOS gated bipolar transistors. At the beginning of turn-on the voltage applied to the switch and the driver transistor T1 is high. The base current of the power transistor can increase very rapidly.

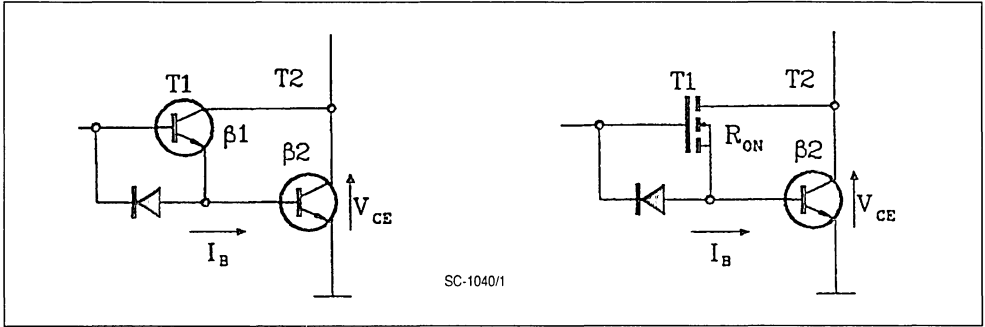


Figure 14 : (a) Schematic Presentation of the Base Current and the Turn-off Behaviour of a Bipolar Transistor.

(b) Storage Time vs. Pulse Time : BUF410 (from the datasheet).

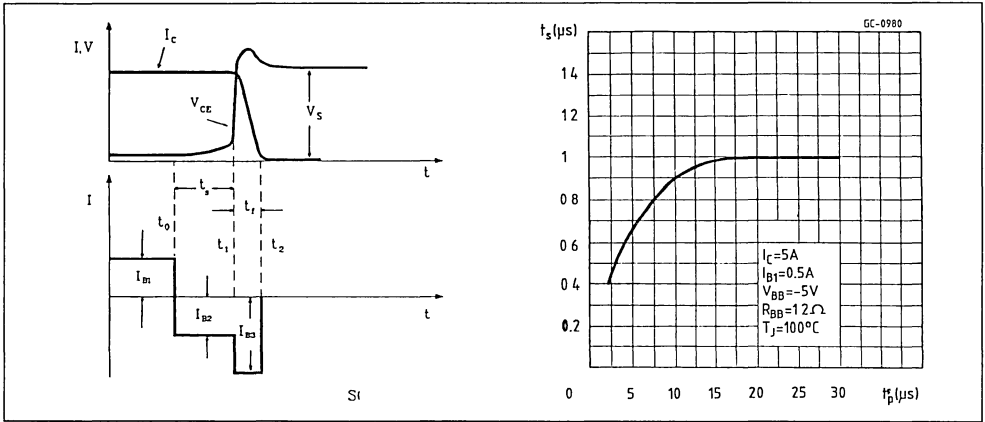
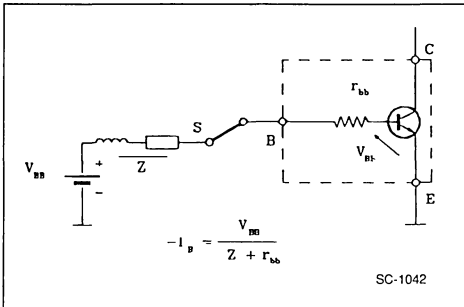


Figure 15 : Limiting of the Negative Base Current by the parasitic resistance and inductance.



Frequently, the negative base current is limited by the modulated parasitic base resistance of the transistor rather than by the external driver circuit. If a standard bipolar (power) transistor is driven from a negative voltage source, for example 2.5V, the negative base current has, initially, a high amplitude. Towards the end of the fall-time, the parasitic base resistance increases and the amplitude of the negative base current is reduced. This leads to an unacceptable increase in fall time, figure 15.

5.2 FAST TURN-OFF

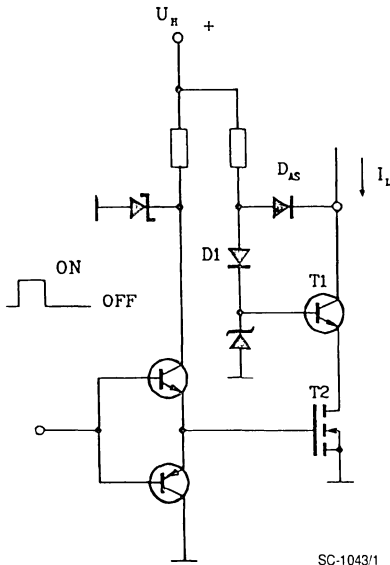
A negative base-emitter voltage as high as the base-emitter breakdown voltage of the device can be applied briefly in order to reduce the effect of the parasitic base resistor. This allows the negative

base current to reach its highest possible amplitude. Collector current fall-times of less than 10 nanoseconds can be achieved when a quasi-saturated transistor is switched off in this way. This driving method is used in cascode circuits, figure 16, and REC driver circuits, figure 17.

Switching times can be reduced by using modified technologies. Hollow emitters, ring emitters and cellular structures exhibit an extremely low parasitic base resistance. These transistors achieve high ne-

gative base currents and thus extremely short collector current fall-times, without any negative bias. For example, if a high voltage cellular ETD transistor BUF410 is turned off by a MOSFET with an on-resistance of 0.3Ω , connected between base and emitter, its collector current fall-time is less than 100ns at 8A and a junction temperature of 100°C , figure 18a. The fall-time is better than 50ns when a negative base-emitter voltage of around 2.5V is applied, figure 18b.

Figure 16 : Cascode Configuration of a High Voltage Bipolar Transistor and a Low Voltage Power MOSFET.



APPLICATION NOTE

Figure 17 : REC driver circuit which briefly applies a high negative voltage to the base-emitter junction of the transistor. When this driver method is used, the amplitude of the negative base current exceeds that of the collector current and the emitter current goes briefly negative. (REC = reverse emitter current).

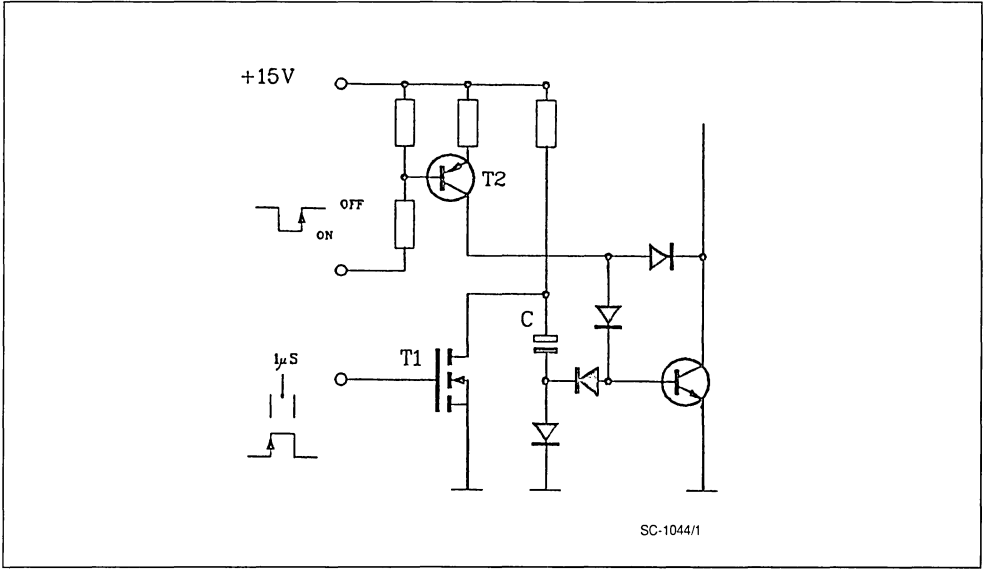


Figure 18 : Turn of Switching of Cellular Transistors,
a) without and

b) with negative base-emit-

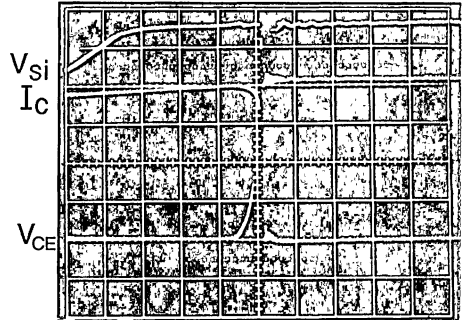
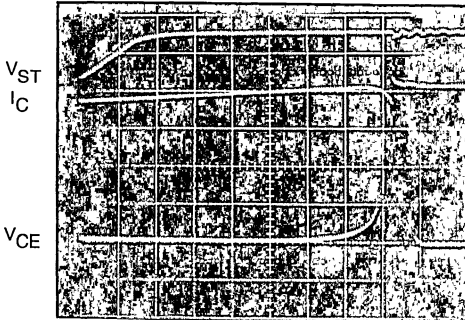
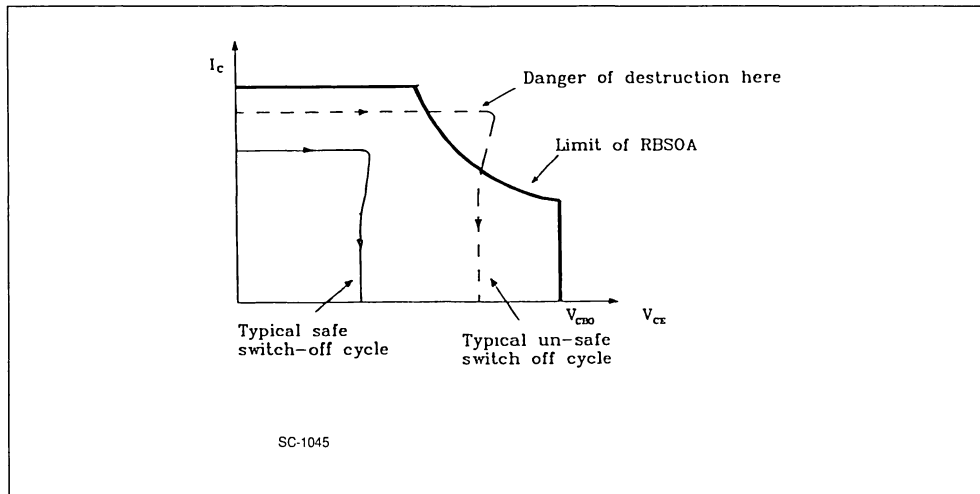


Figure 19 : Safe Operating Area with Typical Safe and Unsafe Switching Cycles.



The figures for Darlingtonts are similar. The output stage acts like a quasi-saturated transistor. The turn-off delay time of the Darlington configuration is determined primarily by the degree of saturation and the way in which the input transistor T1 is driven.

6. POWER HANDLING AND SAFE OPERATION

Safe operation is assured when the switching cycle $I_c - V_{ce}$ is completed within the specified safe operating area of the transistor, figure 19. The safe operating areas depend on the operating and drive conditions. The more homogeneous the current distribution in the transistor, the better is its power handling capability.

6.1 INFLUENCE OF CIRCUIT PARAMETERS

Homogeneity can be improved by an optimised base drive. Any measures that counter current focusing of the collector current increase the power handling capability of the transistor.

In quasi-saturation, a part of the n-collector layer will act like a resistor with a positive temperature coefficient. If the current distribution is heterogeneous the junction temperature rises at points of high current density. The resistance of the n-collector layer is higher at these points and in turn, local current density is reduced - the transistor operates homo-

geneously and local avalanche injection occurs only at exceptionally high collector currents. When a quasi-saturated transistor is turned off, its power handling capability may thus be assumed to be higher compared to turn-off from hard saturation. Soft base drive implemented with a small inductance between drive and base, for example, counters current focusing and increases the power handling capability.

The amplitude of the negative base current has, depending on the collector current level, the following influence :

- 1) when switching off from relatively low current, that means operation with low current density, a negative base current equal to the collector current will block the base emitter junction and turn-off will happen as with a diode. In this case the transistor can turn-off with voltages up to V_{cbo} .
- 2) when switching off high current, that means operation with high current density, a high negative base current leads to increased current focusing and consequently to reduction of the voltage handling ability.

Depending on the level of collector current, an increase of the negative base current will lead to an increase of the safe operating area at low current and a reduction of the safe operating area at high current.

Figure 20 : Effect of Negative Base Current Amplitude on the Transistor's load-line Capability.

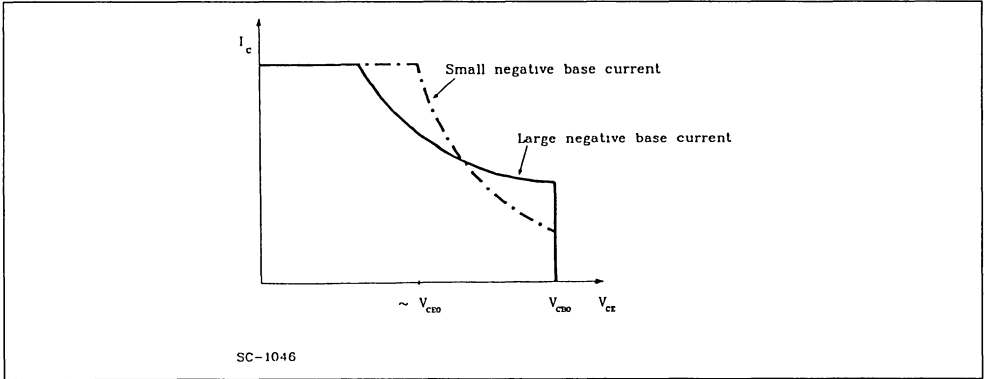


Figure 21 : Safe Operating Areas for Turn-on Switching (FBSOA) and turn-off Switching (RBSOA) of Modern Bipolar Transistors.

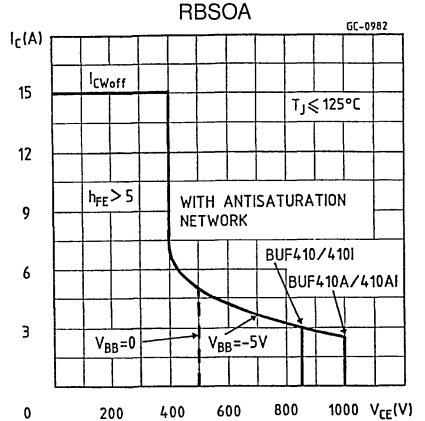
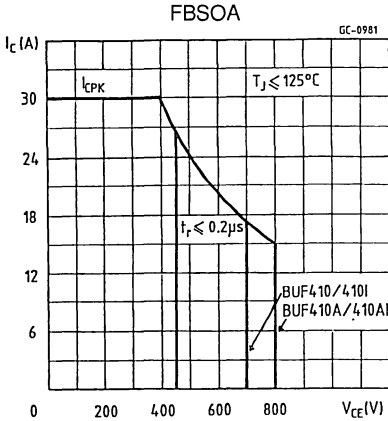
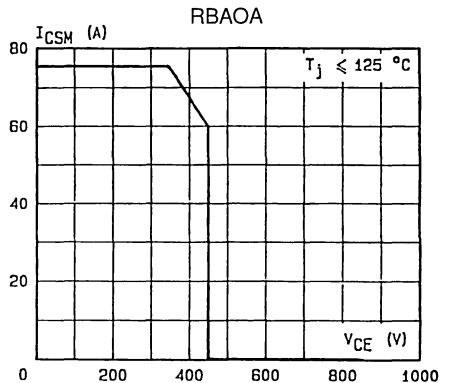
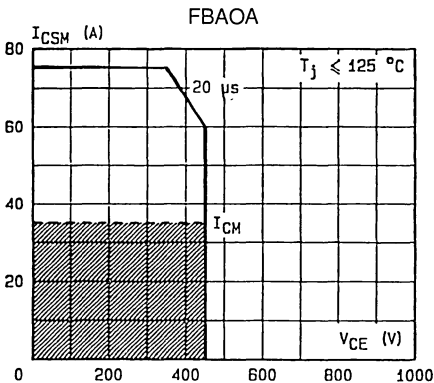


Figure 22 : Accidental Overload Areas (FBAOA, RBAOA).



6.2 INFLUENCE OF TRANSISTOR STRUCTURE

Suitable horizontal geometry will also help improve the homogeneity of current distribution in the transistor. This is taken into account in the design of the finger or cell structures of advanced bipolar transistors.

6.3 SAFE OPERATING AND ACCIDENTAL OVERLOAD AREAS

In the data sheets several safe operating areas are specified. The switching areas apply when the transistor is used in the switching mode. The switching cycle must remain within the limits of the FBSOA (forward-biased safe operating area) during turn-on and within those of the RBSOA (reverse biased safe operating area) during turn-off, figure 21. The RBSOA is increased if the transistor is turned off from quasi-saturation or if the negative base current has a limited rate of rise.

Two types of turn-off load-line, as discussed below, may occur in buck, boost or inverter circuits.

1) Turn-off when the rate of rise dV_C/dt of the collector-emitter voltage is limited by a capacitive load :

This type of load-line occurs in resonance converters or if a switching aid network (snubber) is connected to the transistor. In this case the transistor can be exploited to the maximum of the blocking voltage, V_{CEV} or V_{CBO} .

2) Turn-off with unlimited dV_C/dt , e.g. in circuits without snubbers :

Turn-off without a snubber network constitutes the most critical application. Without dV/dt limitation and at the nominal current $I_{C_{sat}}$, the transistor can switch up to its rated voltage V_{CEW} . This voltage is specified in the data sheets of many transistors. Cellular transistors can be used up to V_{CEX} without dV/dt limitation. In this case the switched current has to be smaller than the nominal current, $I_{C_{sat}}$. The data sheets of modern transistors specify the accidental overload areas FBAOA and RBAOA. These overload areas specify how far and how often the transistor can be exposed to accidental overload, figure 22.³

7. TYPICAL DRIVER CIRCUITS

An optimum drive for bipolar and Darlington transistors can be realised with low cost and with a few components.

7.1 DRIVER STAGE FOR USING TRANSISTORS IN QUASI-SATURATION

Driver stages such as the one shown in figure 23 are used to drive the transistors in quasi-saturation. The transistor never receives more base current than is necessary for quasi-saturation under a given collector current. Under this condition the collector-emitter voltage of the transistor is typically 0.8V. The driving losses and turn-off delay times are minimized.

7.2 DRIVING WITH A BASE CURRENT PROPORTIONAL TO THE COLLECTOR CURRENT

The primary winding of a transformer is connected in the collector circuit, figure 24a. The secondary winding is connected to the base-emitter junction. The turns ratio of the transformer is chosen to be equal to the current gain of the transistor. The transformer functions as a current transformer ; it supplies a base current proportional to the collector current during the on-state. In this case the driver losses are no more than $V_{BE} \cdot I_C / \beta$. For example, when switching 500V at 10A (5kW) the driver losses are only 3 to 4 watts.⁶

If a power MOSFET with a blocking voltage of about 50V is inserted in the emitter circuit of the high-voltage bipolar transistor, the result is a cascode with extremely short turn-off times, figure 24b. The bipolar transistor and the MOSFET are driven together from the driver transformer. The driver transformer takes the necessary driving power from the collector circuit. The circuit is bistable, a short positive pulse can trigger it to the on-state. A short negative pulse switches the circuit off. One draw back of this driver stage is the limited maximum pulse width. For this reason the configuration is used mostly in switch mode power supplies.

Figure 23 : Principle of a Driver for Operating the Transistor in Quasi-saturation :
 a) with constant current consumption independent of the collector current,
 b) with reduced current consumption dependent on the collector current.

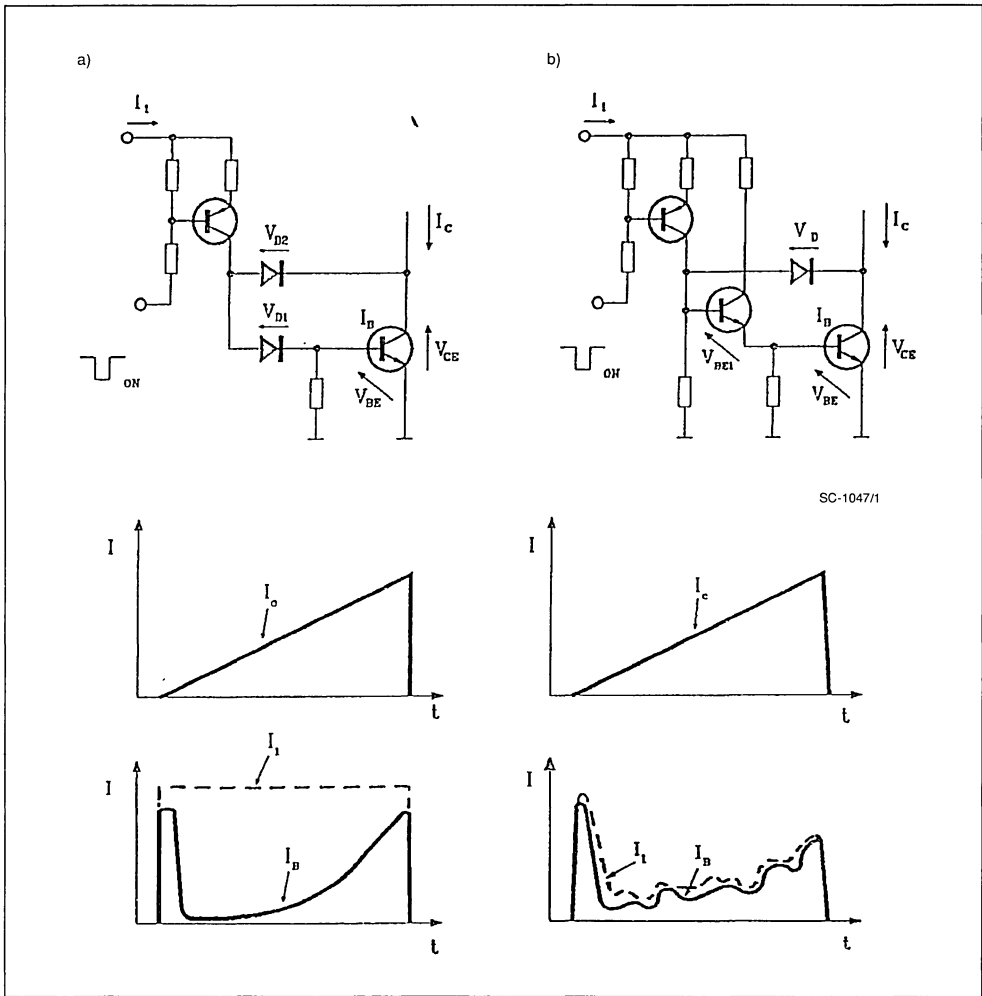
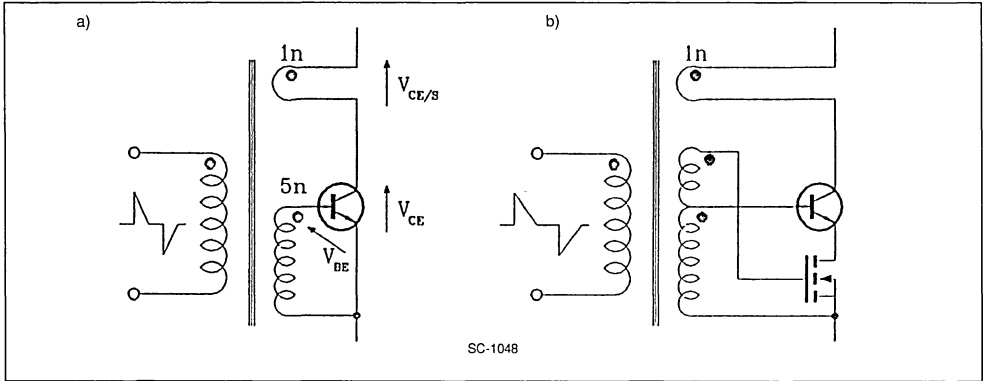


Figure 24 : Principle of a Driver with a Base Current Proportional to the Collector Current.

- a) with a bipolar transistor,
- b) with a bipolar transistor and a power MOSFET as a fast, high voltage, cascode.



7.3 DRIVER CIRCUITS WITHOUT NEGATIVE AUXILIARY SUPPLIES

Even without negative base voltages cellular bipolar transistors exhibit short turn-off times. This is the key for extremely simple driver circuits, figures 25, 26. In this circuit a current source delivers the base current for fast turn-on switching and a Power MOSFET acts as a base-emitter short circuit for fast turn-off switching. This principle can also be used to drive Darlington transistors made with cellular technology, figure 27.

Where shorter switching times are required some additional components can be used to accelerate the turn-off switching, figures 28, 29. A capacitor, C2, is charged during both the conducting and the non-conducting times.

The capacitor is, during storage and fall-times, switched to the base-emitter junction of the power transistor and acts as a negative voltage source. It

is only during these times that the capacitor charging is briefly interrupted. Unlike other driver concepts involving capacitors, this configuration exhibits a state of charge independent of the duty cycle. When used in a bridge configuration, the power transistors can be protected against the effect of reverse currents by the insertion of two diodes into the driver circuit, figure 28b.⁵

7.4 DRIVER STAGE WITH HIGH EFFICIENCY

Smartpower ICs can be used to design particularly low-loss base drivers.⁷ The configuration shown in figure 30 is based on the switch mode principle. It delivers a base current of, for example, 4A. The input current of the driver stage is only a fraction of this value. The circuit can operate from an unregulated auxiliary voltage source and can deliver output pulses of any duration. The negative bias is made with a zener diode.

Figure 25 : Driver circuit that short-circuits the transistor's base emitter junction for turn-off switching.

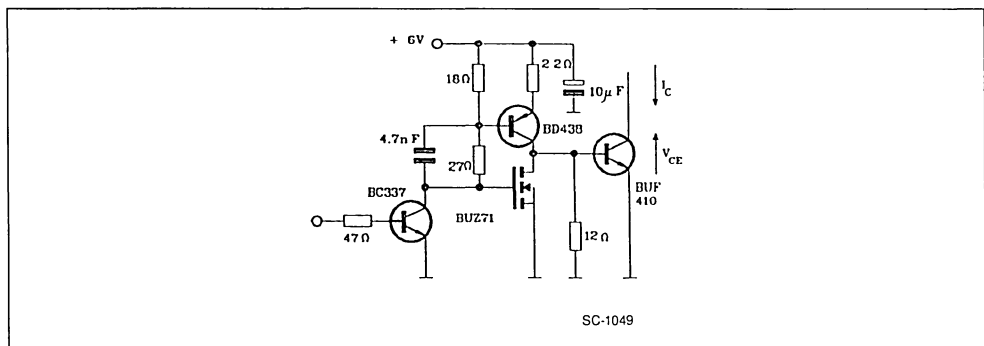


Figure 26 : Turn-off Switching of a 450/1000 volt transistor driven by the circuit in figure 25. The transistor switches to a short circuit at a supply voltage of 320V.

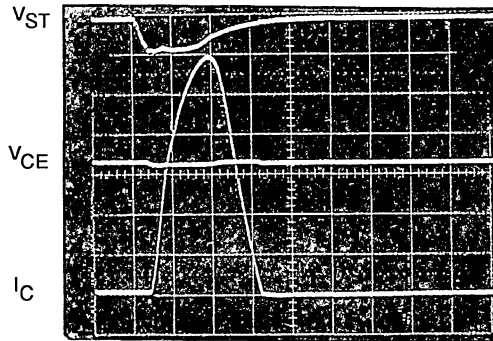
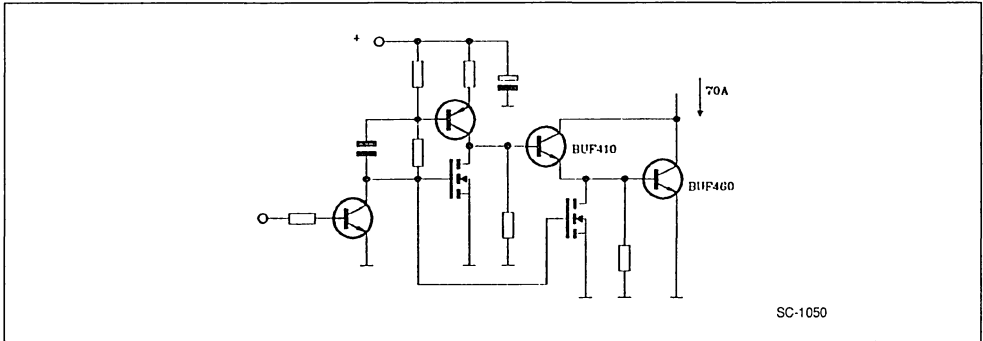


Figure 27 : Driver Circuit as in Figure 25 Modified for Cellular Darlingstons.



SC-1050

Figure 28 : a) Drive for fast turn-off switching without negative auxiliary supply, b) additional circuit for generation of a permanent bias voltage by diodes for protection against the effects of reverse current.

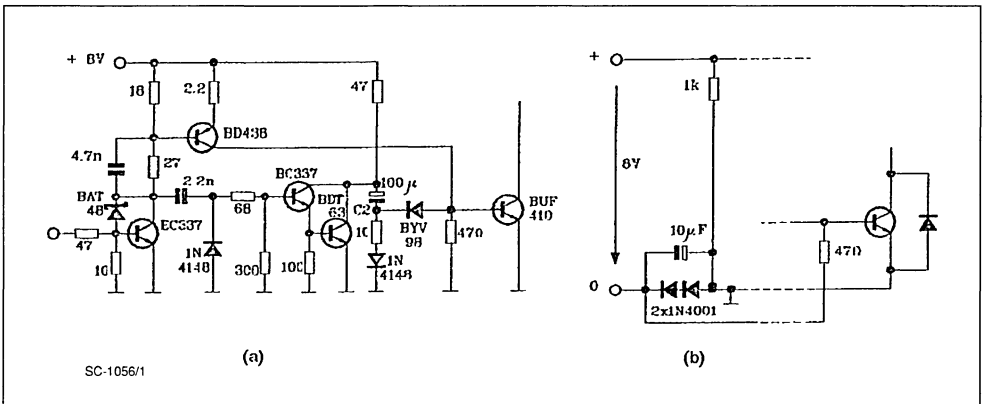


Figure 29 : Turn-off Switching of a 400/1000V Transistor Driven by the Circuit as Shown in Figure 28.

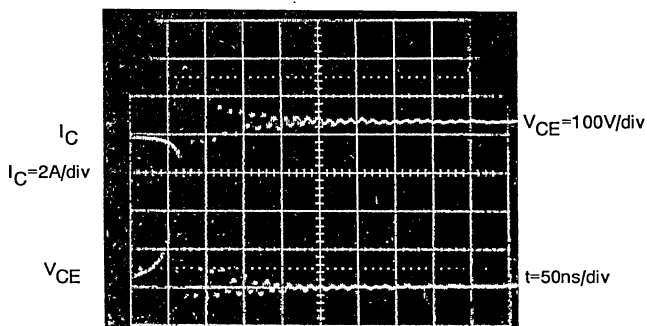
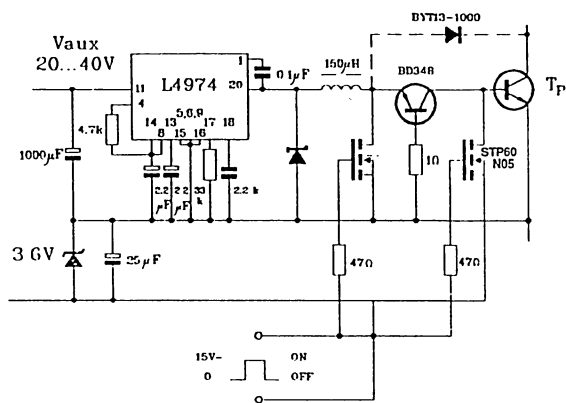
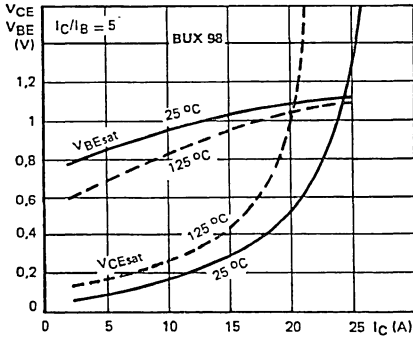


Figure 30 : Driver Stage with High Efficiency. The smart power IC is in a DIL package and is cooled only by the PCB. ICs with output currents of 10A, for example, are available for transistors requiring currents greater than 4A.



SC-1027

Figure 31 : Base-emitter and Collector-emitter Voltages as a Function of Collector Current and Junction Temperature. At high collector current the temperature coefficients of both voltages are positive.



7.5 PARALLELING BIPOLAR TRANSISTORS AND DARLINGTONS

The base-emitter voltage is the sum of the threshold voltage and the voltage drop across the parasitic base resistance. The threshold voltage has a negative temperature coefficient, whereas the temperature coefficient of the parasitic base resistance is positive. The positive temperature coefficient is predominant when the base current is high, figure 31. At high collector current the base emitter voltage increases with temperature. With parallel transistors this leads to reduction of the base current and the

circuit stabilises itself. The temperature coefficient of the collector-emitter voltage is also positive, leading to a very good static current sharing between the paralleled transistors, figure 31b. Dynamic symmetry is obtained by strict symmetry in the layout and by operating the transistor in quasi-saturation. This has been analysed in a 500A switch mode regulator. In this switch mode regulator six Darlington's share the current of 500A. A driver circuit with an internally generated negative bias as described in Section 7.3 was used to drive the Darlington's, figure 32. Static and dynamic asymmetry of the currents was less than 10%, due to the concentric and strictly symmetrical layout, the interconnection of the Darlington output stage base connections and operation in quasi-saturation.

8. PROTECTION

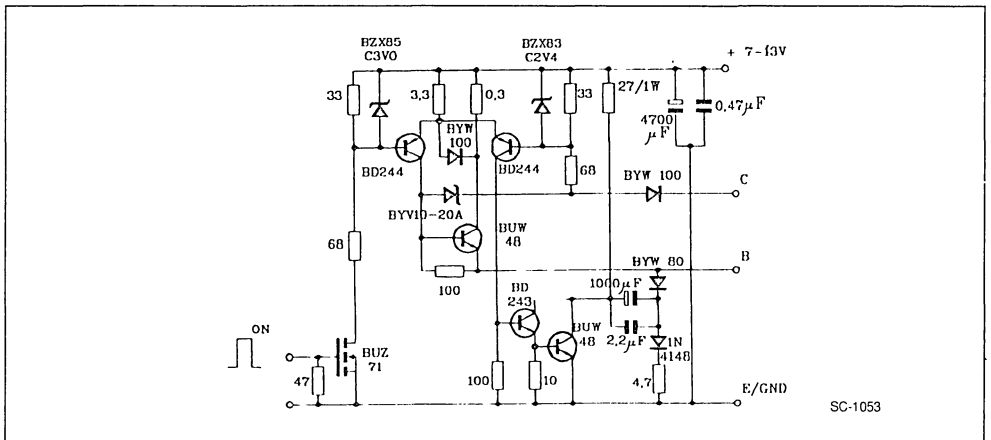
In case of over current and short-circuit it is possible to distinguish between three different types of overload :

- 1) over current in the on-state
- 2) turn-on to an existing short circuit
- 3) connecting a short circuit on to a conducting transistor.

8.1 PROTECTION AGAINST OVER CURRENT DURING CONDUCTION

If the collector current in the transistor exceeds the product of the base current and the current gain, the collector voltage rises to several volts. This condi-

Figure 32 : Driver Circuit, Without a Negative Auxiliary Voltage, Designed for Switching off 500A with Darlington's.



is called desaturation. This causes a high power loss in the transistor leading to high junction temperature and ends with the destruction of the device. Protection of the transistor can be achieved by monitoring the collector-emitter voltage during conduction. If the collector-emitter voltage exceeds a reference voltage the transistor is turned-off immediately. This configuration is known as desaturation detection, figure 33. Transistors with blocking voltages in the 1000V range require, at turn-on switching, a few μs before the collector-emitter voltage drops to the saturation voltage. A dynamic reference voltage can be used to improve the efficiency of the desaturation detection. At turn-on switching the dynamic reference voltage falls from, for example, several tens of volts to a few volts. When this method is used, an inhibit time of about 0.5 to 1.0 μs can be chosen, figure 34, 35.

8.2 TURN-ON TO AN EXISTING SHORT-CIRCUIT

If the output of a bridge-leg is short-circuited, for example to the positive supply, the lower transistor switches to a voltage source V_B with a low internal resistance, figure 36. The collector current, I_C , of the transistor increases with a certain rate of rise of di/dt . The rate of rise is determined by the base current and the current gain of the transistor. The current gain of Darlington's is very high and consequently the collector current of these devices increases very quickly under short-circuit conditions. After some microseconds, the collector current stabilises at a high level I_{SC} . In this state, the collector-emitter junction is subject to a high voltage. The energy present in the transistor is very high. The melting point of silicon would be reached after a few μs , and the device destroyed.

Figure 33 : Principle of a Driver Circuit with Desaturation Detection. The positive edge of the input signal activates the monoflop, MF, for 2 μs in the example given. The power transistor receives a positive base current. If the collector-emitter voltage drops during this time to a value lower than V_{ref} , the comparator output goes positive and the transistor remains conducting. If the input signal goes to zero or if the collector-emitter voltage exceeds V_{ref} , the transistor is blocked.

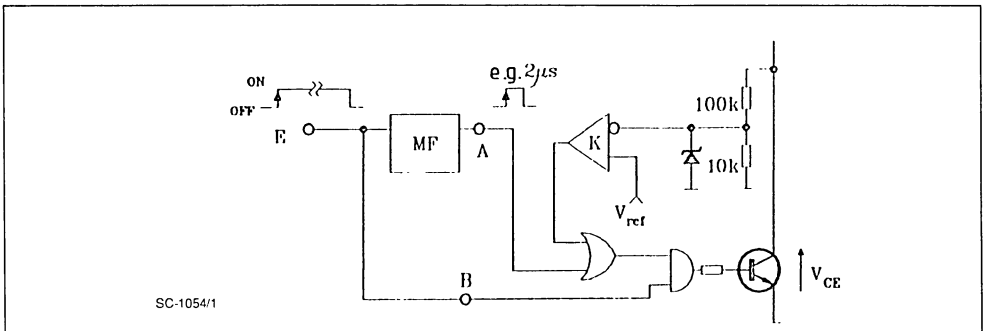
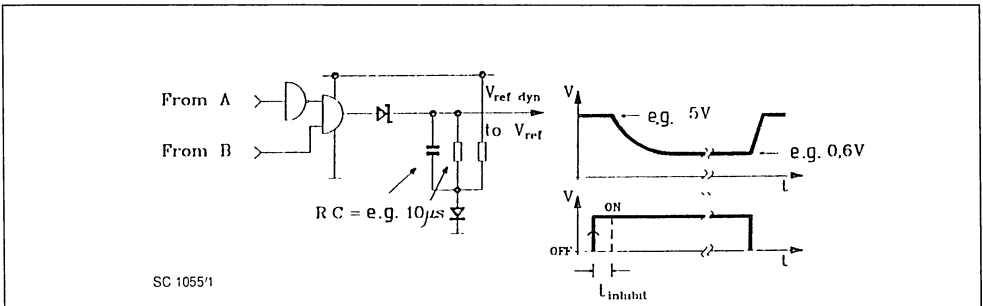


Figure 34 : This circuit generates a dynamic reference voltage for the driver circuit of figure 33.

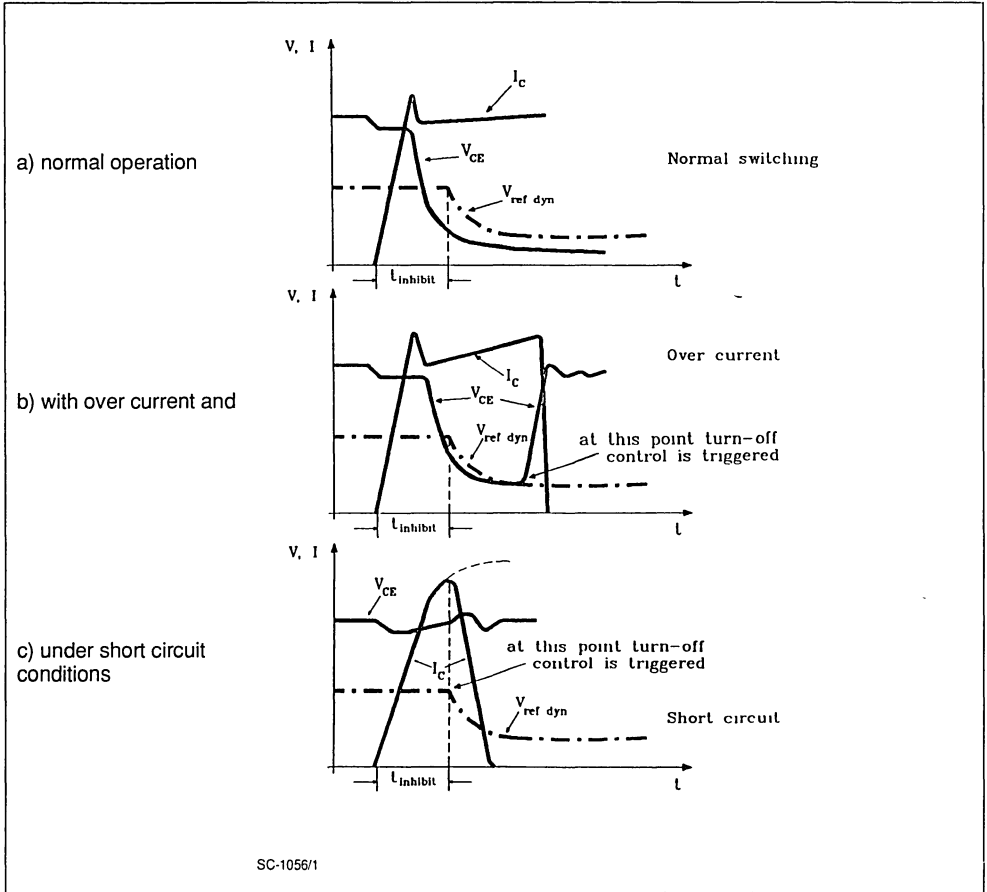


Also at normal turn-on switching to a conducting free-wheeling diode, the transistor is subjected to a short-circuit during the reverse recovery time, t_{RM} of

the diode. For this reason the over current comparators have to be inhibited for approximately 1 μs at turn-on switching, figure 35.

Figure 35 : Waveforms of Collector-emitter Voltage.

The inhibition time of the protection circuit can be reduced to approximately $1\mu\text{s}$ when a dynamic reference voltage is used.



Under short-circuit conditions, the amplitude of the short-circuit current I_{sc} and its duration t_{sc} should be reduced to lower the energy stress. In this condition the storage time of a transistor is extremely short. The time t_{sc} depends on the propagation delay times of the over current comparators and the drive circuit. The propagation delay times of these stages should be as short as possible.

The amplitude of the short-circuit current can be controlled by the base current, I_B . Reducing the positive base current reduces the amplitude of the collector current during a short-circuit. It is possible to use a particularly effective method of limiting the short-circuit current with Darlingtons : at turn-on switching, S2 in figure 37, is closed. The

first stage transistor T1 remains off and the output transistor T2 receives the unamplified driver current. This reduces the short-circuit current to less than 50% for the same device driven conventionally. The collector-emitter voltage of the Darlington is monitored and the transistor is switched off after a few μs when switching on to a short circuit. Under normal operating conditions the collector-emitter voltage collapses after the reverse recovery time of the free-wheeling diode. This blocks the switch S2 and the Darlington operates with its normal high current gain.

This method reduces the transistor stress considerably but slightly increases the turn-on by between 20% to 30%.

Figure 36 : Short-circuit between output and positive supply voltage of a bridge-leg. The collector current rises to a high level. The collector-emitter voltage is equal to the supply voltage.

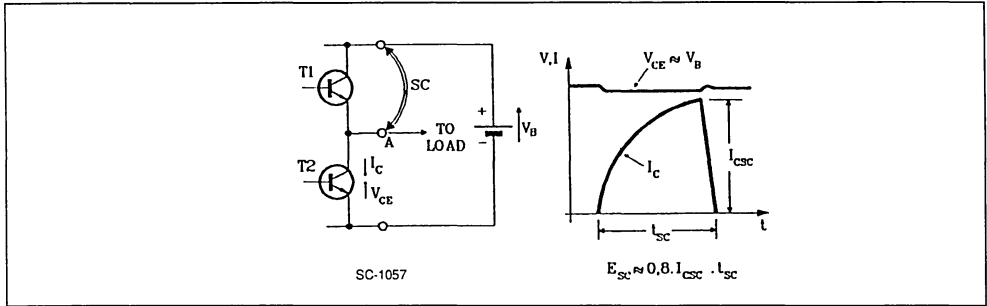
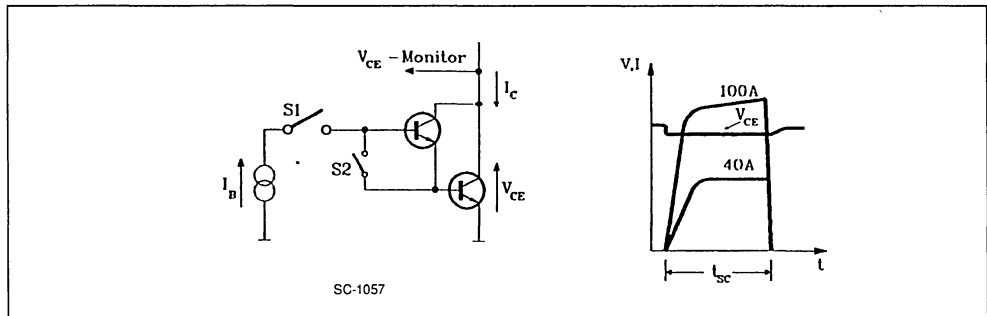


Figure 37 : Reducing the short-circuit current amplitude in Darlington's. At the beginning of turn-on switching S2 is closed, T1 is blocked and T2 receives only the unamplified drive current I_B . Instead of 100A the short-circuit current, I_{sc} , only reaches 40A. In normal operation S2 is opened as soon as V_{ce} has dropped to approximately 30V to 50V.



8.3 CONNECTING A SHORT-CIRCUIT ONTO A CONDUCTING TRANSISTOR

In this case a high collector-emitter voltage is suddenly applied to a conducting transistor, in other words, to a transistor that is unable to withstand voltage immediately, figure 38. The collector current rises to an extremely high level and the transistor may be destroyed. The amplitude of the collector current is determined by the degree of saturation of the transistor at the beginning of the process and by the impedance of the short-circuit.

Resilience to short-circuit can be increased by operating the transistor/Darlington in the quasi-saturated state and by limiting the rate of rise of the short-circuit current. Frequently transistors and Darlington's are already used in the quasi-saturated mode in order to achieve high switching speeds. An inductance is often connected in series with the output to reduce radio frequency interference. This inductance will also limit the rate of rise of the short-circuit current.

The protective measures described in this section are no substitute for properly designed current regulation, but they can be combined with a circuit of this type.

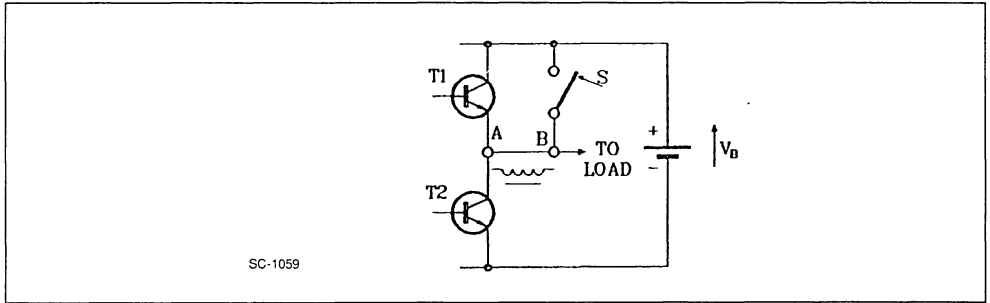
9. CONCLUSION

The switching speed and the load handling capability of bipolar transistors and Darlington's are to a large extent determined by their base drive. Operation in the quasi-saturated mode has a beneficial effect on all characteristics with the exception of conduction losses. Fast turn-on switching with low losses can be obtained by using driver circuits with current source behaviour.

Advanced bipolar transistors do not require a negative bias for fast, low-loss turn-off switching. The protection methods recommended in this paper can also be adapted for use with MOSFETs and IGBTs.

APPLICATION NOTE

Figure 38 : Connecting a Short-circuit onto a Conducting Transistor. Inserting a small inductance between A and B reduces the transistor stress to an acceptable level.



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SEMICONDUCTOR DEVICES
TRIACS

THE TRIAC

by M. Sauvanet - P. Rault

The TRIAC* is a semi-conductor device which has been specifically designed to operate as a controlled switch in an alternating-current power system.

With the introduction of electronic component into industrial applications, the utilization of the Triac as a complement to, or replacement for, electromechanical switches or relays and magnetic control systems, has been rapidly expanding in this field. In addition, its availability has led to the development of new control systems which were not feasible with the previously known devices.

The advantages of the Triac are its noiseless oper-

ation, its ability to be controlled at precise instants and without rebounds, its automatic turn-off when the current reaches zero after the control has been removed, and its ability to withstand without wear an unlimited number of operating cycles when used in the conditions specified by the manufacturer.

We shall briefly describe the principle of operation of triacs used as controlled switches, then insist on the precautions required during utilization to maintain high reliability (section 2 and appendix 1) and, finally, give, in Section 3, examples of applications as on-off control switches, static relays and power variations units.

SYMBOLS AND TERMINOLOGY

Half wave : half cycle of the alternating input voltage V_a . The polarity (positive or negative) of each half wave is defined with reference to the potential of the triac electrode A_1 .

Full wave : couple of consecutive half waves (one positive, one negative)

Trigger pulse : gate current pulse switching on the triac.

Firing : change to conduction of the triac until the current i_T flowing through it reaches the value I_L enabling it to remain in the conducting state up to the end of the half wave (until i_T has dropped below I_H) : see I_H and I_L below.

V_a : instantaneous value of the alternating input voltage (mains voltage, as a generale rule)

V_{RMS} , I_{RMS} : rms values of V_a and of the load current.

V_T , i_T : voltage across the triac in the conduction mode, and current flowing through the triac.

V_M : "breakover voltage" : voltage applied, in the static state, between A_2 and A_1 and beyond which the triac is changed to the conduction mode without gate current.

V_{DWM} : minimum guaranteed value of V_M (= peak working forward voltage : see 2.3).

I_G : gate current, or trigger pulse peak value.

I_{GT} : minimum gate current I_G required to switch-on the triac (if permitted by the load conditions : see I_L).

I_H : "holding current" : minimum value of i_T required to maintain the triac in the on state (below which the triac turns off).

I_L : "latching current" : minimum value of i_T required to hold the triac in the steady conducting state after the triggering pulse has been removed.

I_{TSM} : non-repetitive peak overload current in the conduction mode.

I_{RSM} : repetitive peak overload current in the conduction mode.

α : "angle of conduction" of the triac (α/π represents the fraction of each half wave during which power is applied to the load).

φ : load current phase shift with respect to the input voltage v_a

di/dt : see 2-2

dv/dt , $(dv/dt)_c$, $(di/dt)_c$: see 2-3

* The word "TRIAC" is an acronym for "TRIode for Alternating Current".

1. OPERATION OF THE TRIAC AS A CONTROLLER SWITCH

1.1. STRUCTURE

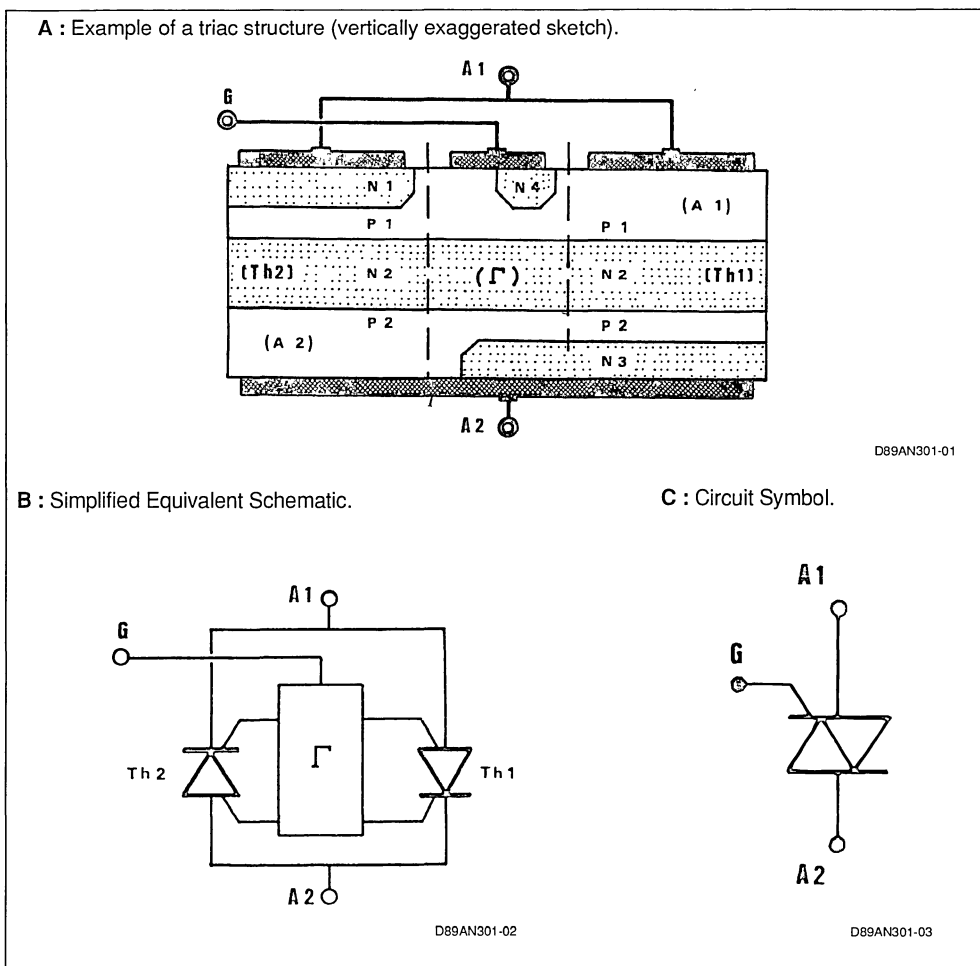
Like the transistor or the thyristor, the triac consists of alternate layers of p-type (majority carriers = holes) and n-type (majority carriers = electrons) semiconductor material. In the case of the triac, the imbrication of these layers is such, that the device can be compared to a power monolithic integrated circuit. Figure A illustrates a possible arrangement of the p and n regions (scale enlarged in the direction of thickness).

Layers P1 N2 P2 N3 form a thyristor Th 1 whose anode consists of layer P1, and the cathode, of layer N3.

Layers P2 N2 P1 N1 form a thyristor Th 2 with anode A2 on P2, which is, therefore and through the external metal connections, antiparallel connected with Th 1 as regards terminals A2 and A1.

Finally, layers P2 N2 P1 N4 form auxiliary element Γ which couples gate G of the triac with the cathode and anode gates of Th 1 and Th 2 in order to permit triggering of the triac in the various possible polarities of the gate and of electrode A2 with respect to electrode A1. Consequently, the triac can be roughly represented by the equivalent electrical schematic of Figure 1B.

Figure 1 : Structure of a Triac.



With no pulse applied to the gate, the current cannot begin to flow spontaneously between A1 and A2. The triac is in the "blocked state".

The application of a current pulse to gate G causes Th1 and Th2 to change to the conducting state (through auxiliary element T), in accordance with the polarity of the terminal voltage. Electrode A1 being taken as reference for the potentials, Th1 conducts during negative half waves (A2 negative with respect to A1) while Th2 conducts during positive half waves (A2 positive with respect to A1). The triac is said to be in the "conducting state" (refer to figure 3, P. 7). When the gate current pulse is suppressed, for instance during a positive half wave, elementary triac Th2 continues to conduct and, consequently, the triac remains in the conducting state until the current decreases to almost zero, below the holding current of Th2.

1.2. OPEN-GATE STATIC CHARACTERISTICS

The study of the operation in conditions in which the voltages and currents change slowly, as in the case of a 50 or 60 Hz alternating-current supply mains without any superimposed interference, can be carried out by starting from the I/V static characteristics of the triac (plotted point by point or observed with the aid of a curve plotter) V (on the X-axis) is the voltage applied between main terminals A2 and A1, with A1 as reference, and I is the current flowing from A2 to A1 in the triac.

The graph of figure 2 corresponds to the case where the triac is not controlled, i.e. where its gate is open ($I_G = 0$).

When a peak-amplitude alternating-current voltage V_a lower than both V_M in positive half-waves and V_M in negative half-waves, is applied to A2, current I always remains very low and, in any case, negligible when compared with the nominal operating current. The triac is in the blocking condition.

When the load is a resistor R, its L/V characteristic: in this diagram is a straight line of slope $1/R$, which moves parallel to itself when the instantaneous value V_a of the supply voltage varies. The operating point moves along section A'A to the points of intersection of the static characteristic of the triac in the blocked state, with the individual load straight lines corresponding to the various values of V_a .

However, when an overvoltage V_P higher than V_M is temporarily applied to the circuit, the load straight

can reach the position indicated by a dotted line, thus moving the operating point to B. Following the removal of the overvoltage, the operating point moves down along section CD of the static characteristic, where voltage V is low and the current high. Thus, this section corresponds to the conditions in which the triac is in the conducting state. It has been "fired" by overvoltage V_P . As a general rule, such a mode of firing is not used in practical applications, for it is difficult to implement, and liable to produce dangerous stresses in the triac and user circuit. If it accidentally occurs for a short duration, it does not cause the destruction of the device, provided the peak current I_P and its rate of rise di/dt do not exceed the specified values.

1.3. FIRING THROUGH GATE CURRENT

When a current I_G is caused to flow between gate G and electrode A1, the blocking voltage decreases abruptly when this current reaches a critical value $I_{G\text{ mini}}$.

As long as I_G is equal to, or higher than, $I_{G\text{ mini}}$, section 'MOM' of the characteristic of Figure 2 is replaced by section E'OE of the curve in dotted line (Figure 4), which joins together the "conducting state" characteristics D'x' Dx. Now, when the applied voltage varies from $-V_a$ to $+V_a$, the operating point describes curves C'C of these characteristics. The current varies from $-I_T$ to $+I_T$ and the voltage across the triac varies from $-V_T$ to $+V_T$.

This voltage drop V_T generally ranges from 1 to 2 V for a peak current $I_{\text{reff}} \sqrt{2}$ corresponding to the triac nominal current. Its maximum possible value V_{TM} at 25 °C is given for each triac in the applicable sheets of characteristics.

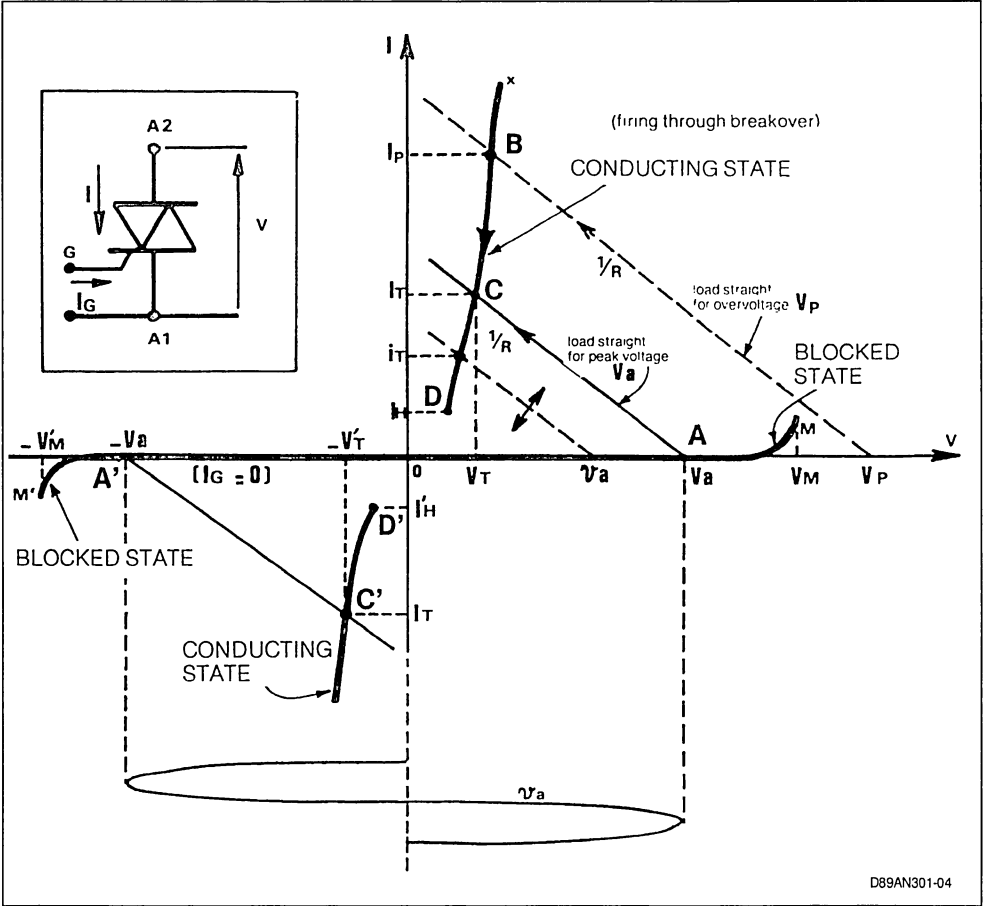
For currents equal to, or lower than, the nominal current, this value decreases when the junction temperature increases, which provides a self-regulating effect of the temperature rise through internal heat dissipation.

If I_G is interrupted at instant t_2 (Figure 3) when the instantaneous value of the current is still high, the operating point remains on the conducting-state characteristic drawn in full line on Figure 4, up to instant t_3 (point D) when the current has decreased to a sufficiently low value I_H . The minimum anode current I_H for which the triac remains conducting without gate current, is called **holding current** (or hypostatic current)* as in the case of the thyristors.

* As a matter of fact, there are two holding current values I_{H1} and I_{H2} depending upon the polarity of V_a . These two values are generally very close to each other.

APPLICATION NOTE

Figure 2 : Triac Static Characteristics with Open Gate (not to scale).



I_H is very low with respect to the triac nominal current (in the cold condition the maximum value of I_H guaranteed by the specifications never exceeds a hundred mA, even for very large triacs ; in the warm condition, the value of I_H decreases considerably). Therefore, its influence on the operation as a switch does not have to be taken into consideration, as a general rule, in practical applications, except in operating conditions in which the load temporarily offers a high impedance at an instant at which the effective supply voltage is low.

The delay in the rise of the current following the application of the control does not exceed a few micro-

seconds. But, to achieve steady firing, current I_G must be applied for a sufficiently long time.

The gate pulse duration must at least be long enough for a sufficient charge :

$$q_G = \int I_G \cdot dt$$

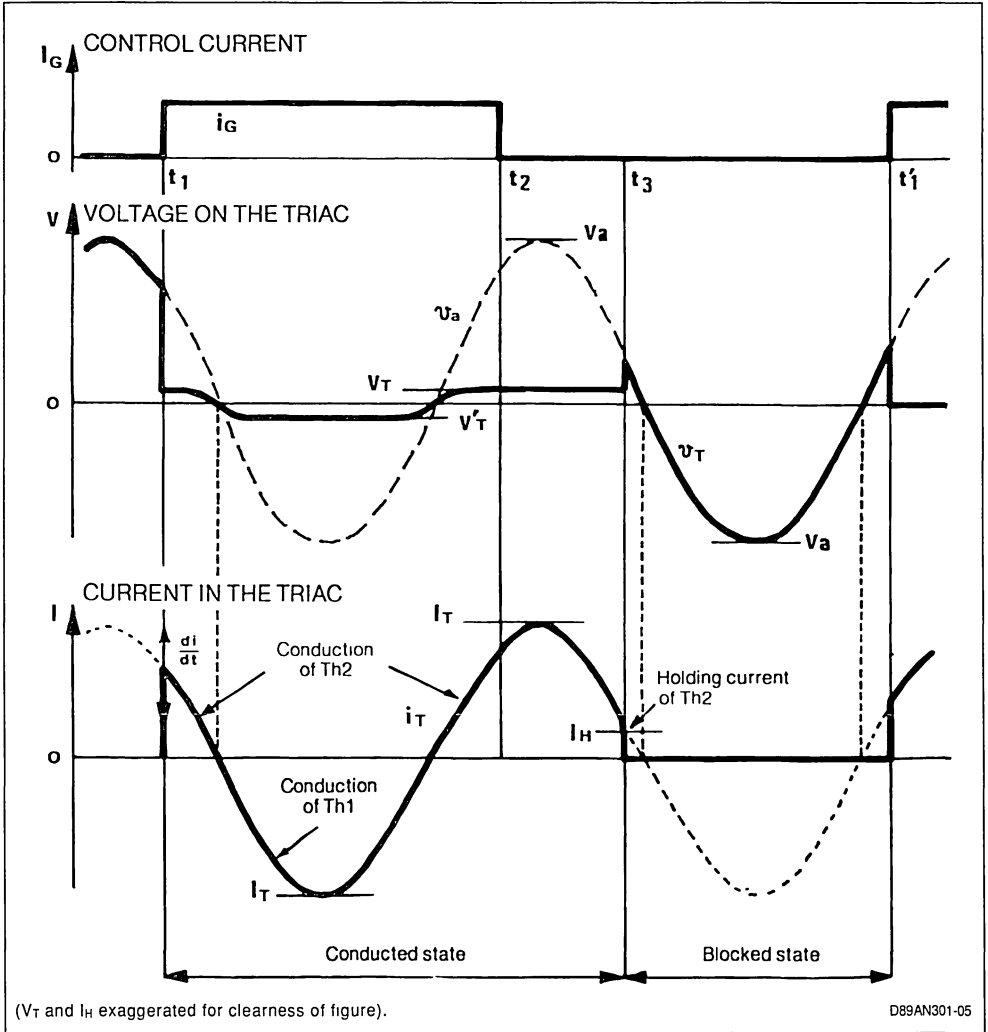
to be injected into the gate region. The minimum duration Δt of a rectangular-wave pulse of current I_G having just the specified value $I_{GT \text{ min}}$ is on the order of about ten μs .

This required duration decreases when the value of I_G increases.

If current I_C in the load does not immediately build up (inductive load) it is necessary, in addition, to hold the gate current until the load has given passage to a minimum current I_L . The "latching current" is equal to, or higher than, I_H , depending upon the respective polarities of A2 and G. It corresponds to point E on the conducting-state characteristic (Figure 4).

Current I_G applied to the gate to fire the triac with either polarity of the supply voltage, can indifferently be of positive or negative sign with, however, triggering abilities which, for average-power triacs, can be somewhat different depending upon these polarities *. There are four possible cases which are determined in accordance with four "triggering quadrants" defined in Table 1.

Figure 3 : Waveforms in a gate-controlled triac with resistive load.



Certain series are not specified in quadrant IV as regards firing current.

APPLICATION NOTE

Figure 4 : Static Characteristics with $I_G = I_{GT}$ (exaggerated around zero).

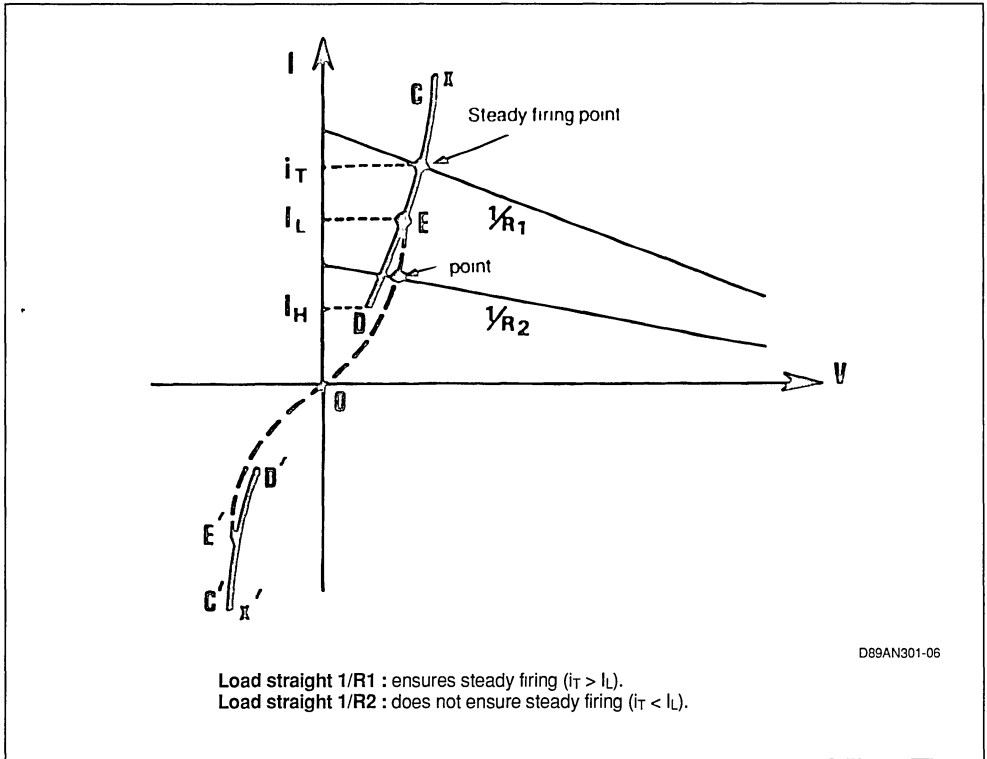


Table 1 .

Triggering Quadrant	Polarity with Respect to A1		Firing Conditions for Small Triacs	
	of A2	of G	I_{GT}	I_L/I_H
Q. I	+	+	Low	≈ 1
Q. II	+	-	Medium	2 to 5
Q. III	-	-	Medium	≈ 1
Q. IV	-	+	High	1.5 to 3

1.4. VARIOUS MODES OF CONTROL OF THE TRIAC

On Figure 3, instants t_1 of gate current application were supposed to occur randomly with respect to input voltage V_a . This operation is similar to that of an electromechanical relay ; the difference, however, is that the triac switch becomes conducting at the precise instant (to within a microsecond) of application of the control, and blocks again, after the control has been removed, at the precise instant at which the current drops below I_H (i.e. practically to zero with respect to the nominal current).

This precision can be made use of to carry out the control in exact synchronism with voltage V_a , in order to sample periodically the voltage applied to the load over intervals of several half waves * (control by half-wave trains), or over half-wave fractions (control by conduction angle). By causing the respective durations of the "conducting" intervals to vary with respect to the "blocked" intervals, a variation of the power applied to the load is achieved. Whenever permitted by the inertia of the user cir-

cuits, the control by half-wave trains offers substantial advantages when, in addition, the firing of the triac is allowed to occur only close to the point where the voltage across the triac goes through zero (i.e. just after zero crossing of the current). Since the triac will next stop conduction also at the zero crossing of the current, this mode of control always ensures a whole number of complete "conducting" half waves (Figure 5 a). On the other hand, triggering on going through zero eliminates any sudden variation of the current flowing through the load, which avoids parasitic radiations and strains in the triac and user circuits. With this type of control, the mean power allied to the load is merely :

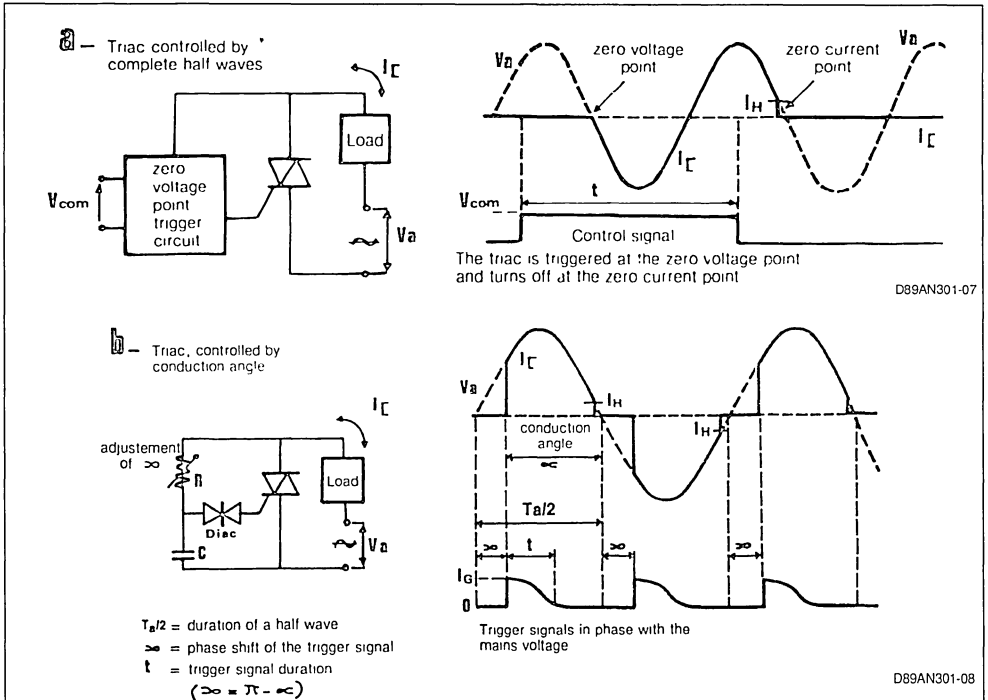
$$P_{AV} = \frac{n T_a}{2 T_e} V_{RMS} \cdot I_{RMS} \quad (1)$$

with : n = number of "conducting" half waves in each sampling period T_e

T_a = period of the mains current (20 ms in the case of a 50 Hz mains).

V_{RMS}, I_{RMS} = rms values of the input voltage and current

Figure 5 : Modes of Control of the Triac in Synchronism with the Mains Voltage (theoretical waveforms on resistive load).



*. The term « half wave » designates each (positive or negative) half of the mains current alternating wave

APPLICATION NOTE

The fineness of adjustment of P_{AV} obviously improves when T_e increases with respect to T_a . A sampling period of 1 second permits adjustment in steps of 1/100. If the load does not stand any dc component, it is necessary to add to the circuit a system of variation per couples of half waves (full waves) requiring, for the same fineness of adjustment, a double sampling period.

In many cases, however (for instance for light dimmers, for the control of highly loaded low-inertia motors or for regulators with low time constant), it is necessary to sample the power at the frequency of the ac supply mains. To do this, it is only necessary to control the gate by current pulses occurring with a

phase shift ($\pi - \alpha$) with respect to the beginning of each half wave. Figure 5b illustrates the principle of this control, with waveforms obtained on resistive loads as well as a simple example of practical application. The conduction angle of the current is α and the mean applied to the load is fairly equal to :

$$P_{AV} = \frac{1}{\pi} \frac{(V_{RMS})^2}{R_L} \int_0^\alpha \sin^2 \alpha \cdot d\alpha$$

$$\text{or } P_{AV} = \frac{2\alpha + \sin 2\alpha}{2\pi} \frac{(V_{RMS})^2}{R}$$

Figure 6 : Triac Power Control.

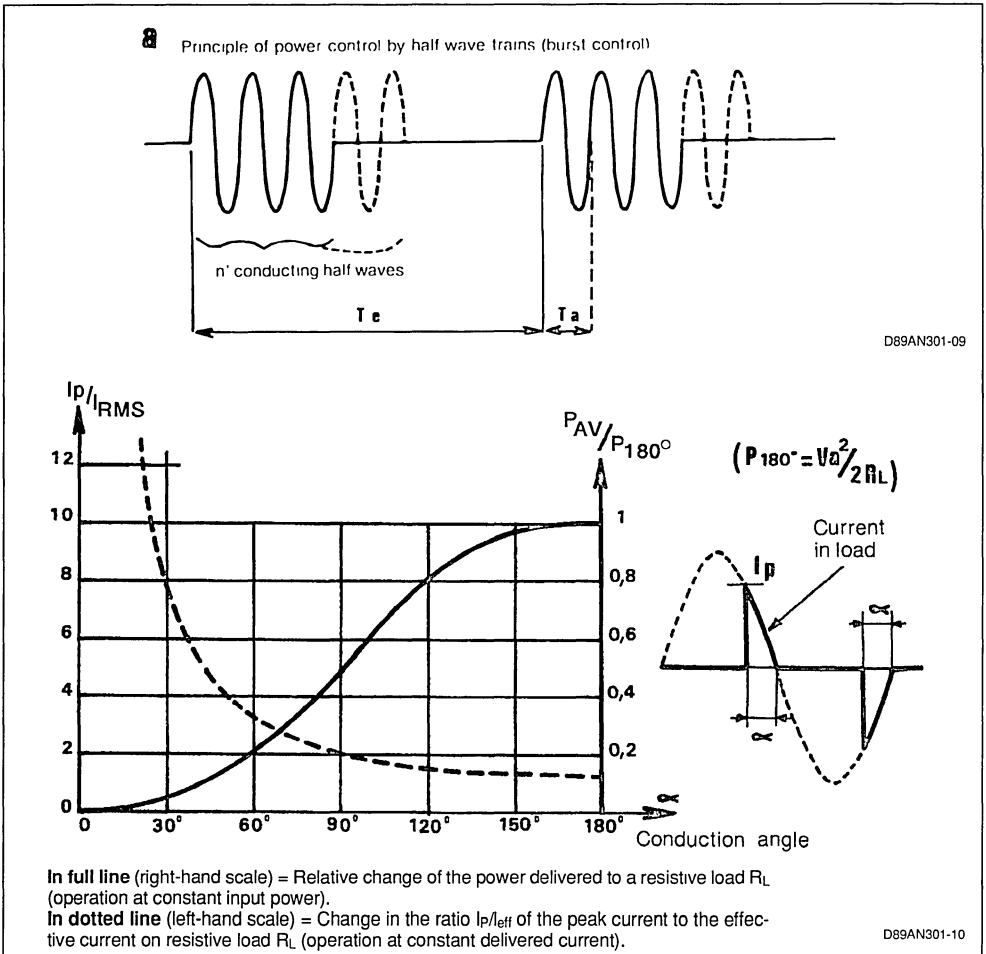


Figure 6 b shows the change in the delivered power P as a function of conduction angle α , when the input power is kept constant. As can be seen, the relationship between P and α is highly non-linear. To obtain a linear relationship between the mean vol-tage on the load and an adjustment voltage V_r , the latter must act on α with an inverse law.

Figure 6 b also shows (in dotted line) the curve of the change in peak current I_p as a function of the conduction angle with left kept constant, i.e. for a constant power in the load. That curve clearly shows the dangerous condition which exists in case of operation at low power with a low conduction angle when I_p exceeds the permissible repetitive surge current.

1.5. OPERATION ON INDUCTIVE LOAD

In the case illustrated by figure 3, where the triac operates on a pure resistive load ($\cos \varphi = 1$), the current reaches immediately the value V_a/R_L when the gate current I_G is applied. This is a theoretical case, for the leads connecting the triac to the mains and load always offer an inductive component which slows down the rate of rise di/dt of the current, and causes a slight phase shift of the instant of current interruption with respect to the zero input voltage point.

With a load offering a high inductive component ($\cos \varphi$ lower than 1), inductance L limits the current rate of rise to :

$$\frac{di}{dt} = \frac{V_a}{L} \tag{3}$$

where V_a is the instantaneous value of the input volt-

age at the instant of application of the firing control. If the gate signal is applied for a duration which is long with respect to that, $T_a/2$, of a half wave of V_a , the waveforms shown in full lines on figure 7 are obtained. Following a period of transition, current I_C reaches the value :

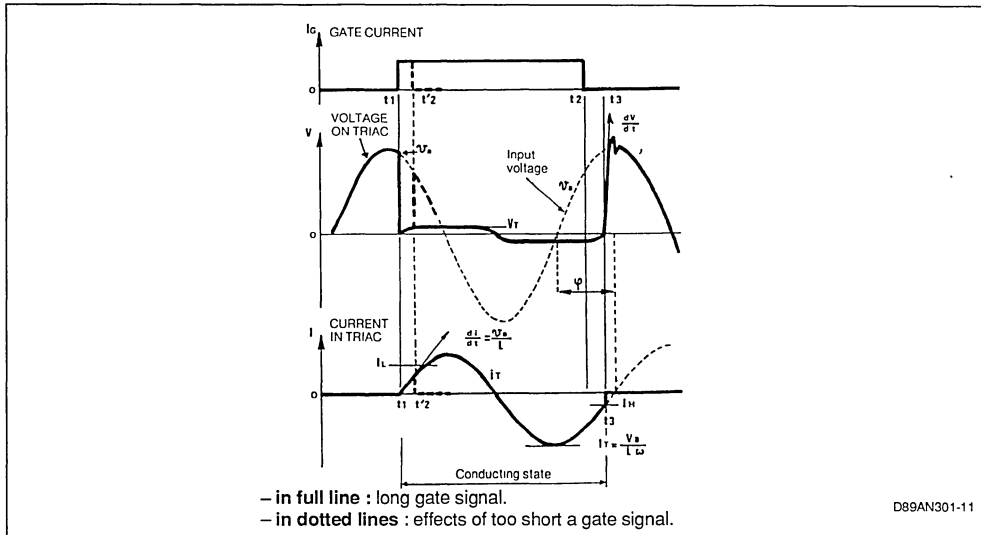
$$\frac{V_a}{L \omega} \sin(\omega t + \varphi), \text{ with } \omega = \frac{2 \pi}{T_a}$$

φ represents the phase shift of I_C with respect to V_a , close to $/2$ when the load is highly inductive. After $\pi/2$ the control has been removed, the current is maintained in the load, as mentioned previously, until its instantaneous value drops below I_H . But, due to phase shift φ , the value of the input voltage is different from zero at that instant. Consequently, the vol-tage across the triac increases suddenly up to value v_a (close to V_a), at a high rate of rise dV/dt which is limited only by capacitive elements possibly present in the circuit.

If the triac control had been removed at time t_2 , immediately after reaching value I_G (short-duration gate pulse), the current in the inductance might not have had the time to reach value I_L of the triac latching current. Firing would not have taken place in a steady way, and the voltage would have increased again up to v_a as indicated by the dotted lines on figure 7.

During operation on an inductive load with short-duration gate pulses, other unwanted conditions may be present when these pulses are applied at the beginning of each half wave of V_a , within angle φ .

Figure 7 : Waveforms with Inductive Load.



These conditions are represented by the full-line waveforms on figure 8 : when the first gate pulse (a) appears, for instance at the beginning of a positive half wave, current I_C increases up to a value at least equal to that of the continuous-duty current and, then, decreases again to a value below I_H only after a period of the time corresponding to angle φ during the next negative half wave. Since the new control pulse (a') already ends at t'_2 , i.e. prior to the cancellation of the current, there will be no gate current at t_3 to fire again the triac during the negative half wave. The next firing will not occur until t''_1 , through pulse a'', during the subsequent positive half wave.

Thus, with this control, the triac behaves like a unilateral switch, conducting only on the positive half waves (similarly, if the first pulse (a) had appeared during a negative half wave, the current would pass only during negative half waves). This results in a rectifying effect introducing a high mean positive (or negative) current into the load. When the latter consists of a coil wound on a magnetic core with small air gap, or of a transformer primary coil, the operating point describes a large portion of the hysteresis loop. This presents the risk of creating a situation in which the core is almost saturated, with the disastrous consequence of an extremely high surge current.

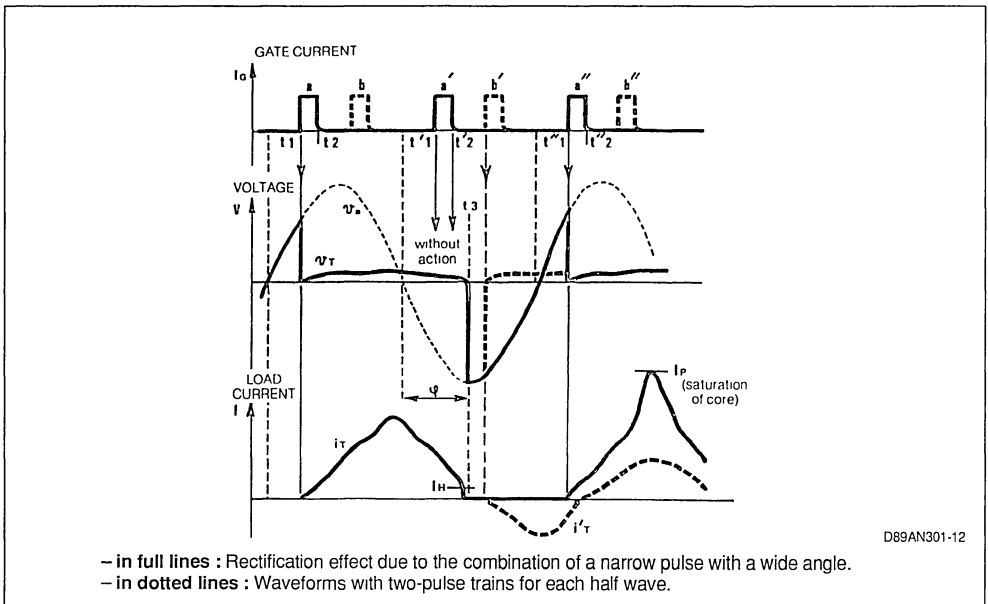
This abnormal operation would not have taken place if the pulses had a duration equal to, or higher than,

that corresponding to angle φ , at the price higher control energy. The effect of the rectification phenomenon can be suppressed through a power-saving means which consist in controlling the triac by pulse trains instead of only one pulse for each half wave. As a matter of fact, figure 8 shows (waveforms in dotted lines) that a new pulse (b') occurring immediately after the current has been cancelled, permits triggering again the triac during the negative half wave. There still remains a dissymmetry between the positive and negative current arches, but the rectifying effect can be considered negligible when the pulses are sufficiently closely spaced.

The various modes of control illustrated by figure 5 in the case of a resistive load, can be used as well with an inductive load, provided the following precautions are taken :

- A) - For control by half-wave trains, the gate pulses should be centred around the zero point of the current that is to say when the voltage is re-applied. This permits ensuring re-firing of the triac immediately after the cancellation of the current (instant t''_2 on figure 8).
- B) - For control by conduction angle, gate pulses of sufficiently long duration, or pulse trains starting from phase.
 - corresponding to the required opening angle , and ending toward the end of the half wave, should be used.

Figure 8 : Control by Wide Conduction Angle on Inductive Load with Short-Duration Gate Pulses.



2. SAFE-OPERATION PARAMETERS

The reliability of the triac is dependent upon a number of utilization precautions which cannot be taken without a thorough knowledge of the stresses or spurious phenomena to which the triac is liable to be exposed.

We shall examine the influence of thermal stresses and of current surges on its service life, and of over-voltages on its blocking capability. Finally, we shall indicate a few means of protection against these parasitic conditions.

2.1. THERMAL STRESSES

The data sheets give a limit value of the virtual junction temperature : $(t_{vj})_{max}$. When the effects of a high-temperature operating environment and of the increase of semiconductor self heating due to the dissipated power, cause the triac junctions to reach a temperature higher than $(t_{vj})_{max}$, the result can be a temporary alteration of the performances, then a irreversible degradation gradually evolving to the complete destruction of the device when that situation remains unchanged for an extended period of time, or occurs repeatedly. Any degradation will be accelerated in cases where an excessive temperature combines with other stresses (overvoltages, short spikes of current or of di/dt etc). In case where the occurrence of such conditions is anticipated, appropriate measures have to be taken to keep the junc-

tions at a temperature substantially lower than the maximum specified value.

Direct measurement of junction temperature t_{vj} is hardly possible during operation. An approximation of its average value $(t_{vj})_{AV}$ can be obtained from the case temperature t_{case} , specified junction/case thermal resistance $(R_{th})_{jc}$ and dissipated power P_{AV} :

$$(t_{vj})_{AV} - t_{case} = (R_{th})_{jc} \cdot P_{AV} \quad (5)$$

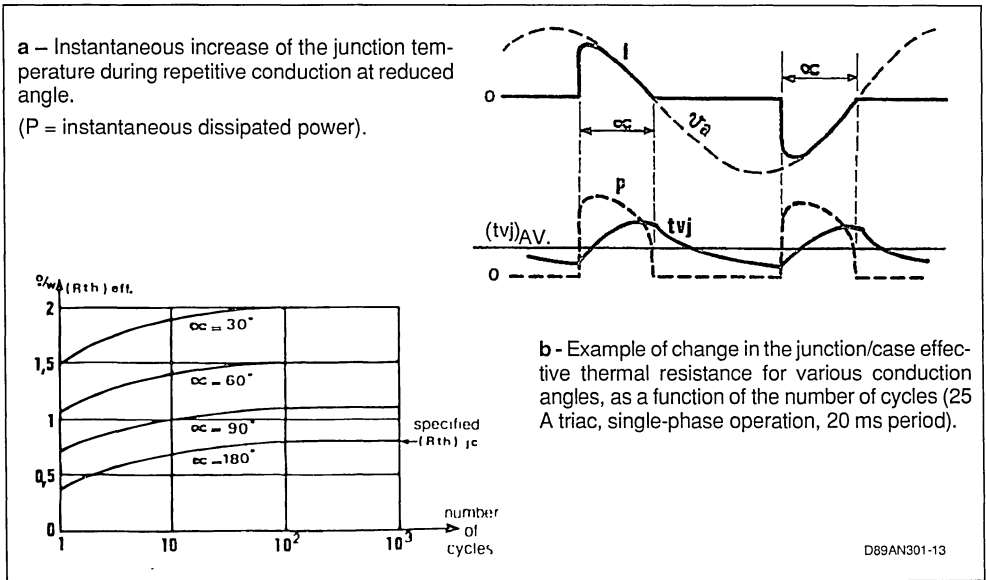
The data sheets of characteristics often give curves of P_{AV} versus condition angle α , showing a decrease of P_{AV} , and consequently of the mean temperature, at small angles α . But, it is to be remembered that the instantaneous junction temperature at small conduction angles may rise substantially higher than $(t_{vj})_{AV}$, as can be seen on figure 9 a.

To take into account these instantaneous temperature increases as well as the decrease in temperature during short-time operation, it has been necessary to introduce the notion of "effective thermal resistance $(R_{th})_{eff}$ ", defined by :

$$t_{vj} - t_{case} = (R_{th})_{eff} \cdot P_{AV} \quad (6)$$

in which t_{vj} now represents the maximum instantaneous junction temperature reached during the cycle. $(R_{th})_{eff}$ is dependent upon the transient thermal impedance Z_{th} of the triac and upon the waveforms to which the device is submitted. It is higher during operation with a small conduction angle, and lower for a few number of cycle, as shown by the example of figure 9b.

Figure 9 : "Effective" Thermal Resistance.



D89AN301-13

Its limit value for continuous duty at 50 Hz, full angle, is the value $(R_{th})_c$ specified by the slopes of characteristics. In case of full conduction, an excess value for the dissipated power can be easily calculated by considering that voltage drop V_T in the triac is of the form :

$$1 \text{ volt} + Ri = 1 \text{ volt} (V_{TM} - 1 \text{ volt}) \frac{1}{I_{TM}} \quad (7)$$

in which V_{TM} is the maximum voltage drop specified at 25 °C for a peak current I_{TM} corresponding to the nominal rms current $(I_{RMS})_{nom}$. If I_T is the peak value of rms current I_{RMS} in the case of operation considered, then :

$$P_{AV} \leq \frac{2 I_T}{\pi} + R_{I_{RMS}} \cdot I_{RMS} \cdot \left[1 + \frac{V_{TM} - 1}{\sqrt{2}} \cdot \frac{I_{RMS}}{(I_{RMS})_{nom}} \right] \quad (8)$$

(I_{RMS} in amperes, V_{TM} in volts, P_{AV} in watts).

Formulae (5) and (8) give an excess value for the average junction temperature $(t_{vj})_{AV}$.

Inversely, these formulae permit determining the thermal resistance $(R_{th})_{da}$ of the heat sink to be used to keep the junction at a mean temperature lower than the value of t_{vj} which has been selected for a maximum possible ambient temperature t_{amb} :

$$(R_{th})_{da} = \frac{t_{vj} - t_{amb}}{P_{AV}} - (R_{th})_c - (R_{th})_{cd} \quad (9)$$

in which : $(R_{th})_c$ is the junction/case thermal resistance specified by the sheets, $(R_{th})_{cd}$ is the contact thermal resistance between the case and heatsink.

2.2. CURRENT STRESSES

In many practical applications the triac may have to withstand current surges. Let us mention more particularly :

- short-circuits of the load,
- user circuits including a capacitive component,
- utilization with incandescent lamps (resistance when cold 10 to 20 times lower than when hot),
- utilization with coils wound on magnetic cores liable to saturation,
- untimely firing of the triac by high-energy overvoltages.

NON-REPETITIVE CURRENT SURGES

The datasheet indicates a limit value I_{TSM} for the peak of the non repetitive* alternating current allowed to flow through the triac during one, and only one, period of the supply mains .

As a general rule, this limit value is 6 to 7 times higher

than the nominal peak current I_{TM} of the triac (i.e. 8 to 10 times higher than the nominal rms current I_{Teff}). Most of the devices are capable of withstanding without destruction an even higher non-repetitive current peak when its duration is lower than 10 ms.

The slopes of characteristics give a limit value for the expression $\int i^2 dt$ for current surge durations ranging from a few milliseconds to some ten milliseconds. This expression fairly well characterizes the operation of a cutout ; its value is helpful in selecting the "I²t" of a fast-acting fuse intended to protect the device against possible short-circuits of the load. However, it should be used cautiously when the value of the permissible peak current is to be deduced from it, because it is only valuable to represent the surge capability of the triac for a given pulse duration t_2 , within a narrow interval. For lower durations ranging from a hundred microseconds to a few milliseconds, the permissible non-repetitive current surge in the triac follows a curve closer to that given by the expression :

$$\int i^4 dt = \text{constant}$$

as represented on the theoretical curves of figure 10.

Finally, for very short current-pulse durations, the permissible current surge is mainly limited by the rate of rise di/dt of the current, which necessarily accompanies it (figure 10).

The limitation by di/dt occurs in a more critical way at the instant the triac is fired (willingly or accidentally) on a little-inductive, low-resistance load. An examination of the waveforms of figure 3 shows that firing on a purely resistive load outside of the zero voltage point, entails an extremely fast increase of the current. Practically, there always exists, fortunately, a small inductive component (due to the leads connecting the device to the mains and load) which limits the rate of rise of the current. But, that rate of rise can reach prohibitive values at the instant the current reaches an high value due, for instance, to the presence of capacitances on the triac terminals, or to a very low instantaneous value of the voltage (untimely firing by an overvoltage).

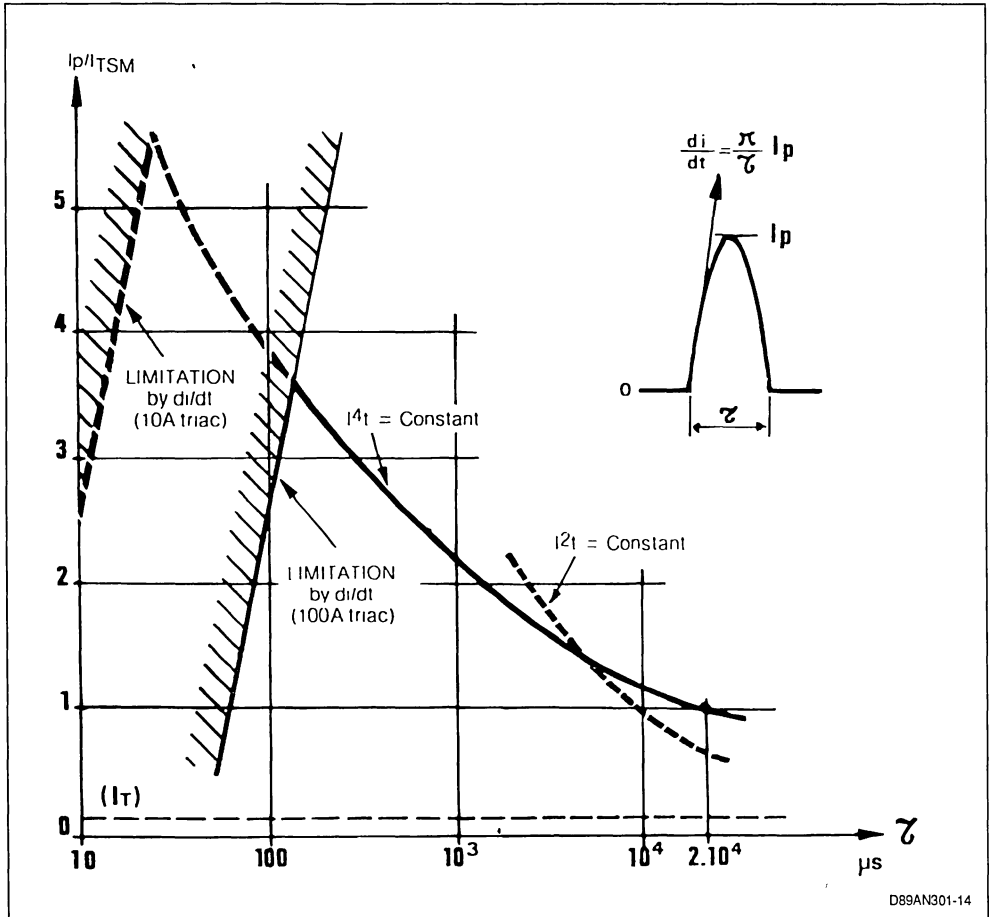
The harmful effect of a high rate of rise di/dt can be explained, as for the thyristors, by the concentrations of current, and, consequently, by hot points, produced at the instant of the firing, due to the fact that firing first occurs in a very narrow region before spreading out over the full area of the junctions. Since the spreading speed of the conducting region increases when the gate current increases, the behaviour in the presence of non-repetitive high di/dt values will be considerably improved when the triac is fired by a current I_g rapidly reaching a high value.

* The device is supposed to withstand this non-repetitive anomaly a limited number of times (a hundred times, according to the JEDEC standards) during its lifetime

In case of firing through the gate by a steep leading edge with an amplitude in any case higher than the specified I_{GT} , the SGS-THOMSON Microelectronics power-controlling triacs can withstand without damage di/dt values of $100 \text{ A}/\mu\text{s}$ or more (for comparison, a 50 Hz alternating current of 30 A amplitude rises at a maximum rate of about $10 \text{ mA}/\mu\text{s}$, i.e. at a rate 10 000 times lower than the critical rate).

When the current leading edge intervenes following an untimely firing on a steep voltage leading edge, the user is evidently not in a position to control the intrinsic gate current created by the di/dt . This gate current being generally low, the permissible di/dt values in such cases of untimely triggering will also be relatively low (less than $10 \text{ A}/\mu\text{s}$), particularly when they are accompanied by instantaneous thermal overloads (high surge current amplitude).

Figure 10 : Permissible non-repetitive current surge I_p in the case of a sine wave arch of duration τ .



D89AN301-14

REPETITIVE CURRENT SURGES

Repetitive stresses with surge current values much lower than the limit value indicated for non-repetitive stresses can lead to an alteration of the triac performances as a result of the cumulative elevation of the instantaneous junction temperature which accompanies them.

This is particularly the case when the triac operates continuously with a small conduction angle while delivering high power. This mode of operation corresponds to high peak currents during short periods of time. At the instant of each passage of the current peak, there is a risk of the triac junctions reaching a prohibitive temperature. The knowledge of the global transient thermal impedance of both the triac and the heat sink, permits verifying that the instantaneous value of the junction temperature does not exceed $(t_{vj})_{max}$ (refer to 2.1, *figure 9*).

At least, it is necessary to limit the power to a value preventing the repetitive current surge from exceeding the specified value of I_{TRM} , and to make sure, in any case that the peak current corresponding to the full conduction angle would remain notably lower than I_{TSM} in case of untimely triac firing during a complete half wave.

For very small conduction angles with a resistive or capacitive load, another limitation is given by the rate of rise di/dt of the current in the repetitive state, as will be seen hereafter.

Due to the relatively intricate current paths imposed by the triac firing technique, frequently repeated steep current leading edges can entail a slow alteration of the triac characteristics. The values of di/dt permissible in the repetitive state are lower (in a ratio of 2 to 3, as a general rule) than the values of di/dt specified for non-repetitive current surges. Such repetitive di/dt values are particularly harmful when the user circuit is capacitive. For asynchronous operation (*figure 3*) or for operation with a small conduction angle (*figure 5 b*), it is highly recommended to connect a low-value resistor (a few tens of ohms) in series with the capacitances possibly present on the triac terminals.

Operation with "zero voltage point" triggering (*figure 5 a*) does not give rise to any difficulty due to a **repetitive** di/dt since the triac is fired at the precise instant at which the voltage, hence the current draw, is null. (but, non-repetitive di/dt values are still liable to occur when all the required precautions have not been taken for the avoidance of untimely triggering at instants at which the voltage value is different from zero).

2.3. BLOCKING CAPABILITIES

PEAK VOLTAGE IN THE BLOCKED STATE : V_{DWM} .

In normal working conditions, with an input voltage of low frequency (lower than 100 Hz) free of strong parasitic transients, the triac behaves like an open circuit so long as no gate current is applied and that the ac voltage amplitude does not exceed the V_{DWM} value guaranteed by the data sheet particular to this triac. That specified voltage V_{DWM} is actually guaranteed for a value notably lower than V_M and V'_M (*figure 2*) throughout the authorized temperature range. For that voltage, the leakage current, "peak current in the blocked state", has a maximum value guaranteed at the maximum authorized temperature. In that worst case, it does not exceed the milliampere with small triacs, or ten milliamperes with large triacs. But, these values decrease very rapidly with a decrease of the temperature and voltage. At 50 °C, the leakage current under voltage V_{DWM} is already lower than a microampere, which represents at 400 volts a resistance higher than 400 megohms and reaching several thousands of megohms at a lower voltage.

An applied voltage markedly overshooting V_{DWM} (due, for instance, to an overvoltage of the supply mains) can cause the triac to be triggered into conduction, which entails a temporary loss of its blocking capability, but without causing its destruction when this triggering action is not accompanied by a high overload in current or in di/dt .

CRITICAL RATE OF RISE OF THE VOLTAGE IN THE BLOCKED STATE : "STATIC" dv/dt .

During operation in the presence of parasitic transients, the triac may lose its blocking capabilities, even if the peak voltage of the transient does not exceed V_{DWM} , but when its rate of rise dv/dt is higher than a critical value. As a matter of fact, in such a case current $C_T dv/dt$ developed across the space-charge capacitance C_T of the reverse biased junction with reverse bias in the blocked state, acts as a gate current liable to fire the triac. This susceptibility to steep voltage leading edges obviously increases with a higher sensitivity of the triac (low I_{GT}) and a higher temperature of the semiconductor. The data-sheets indicate a value of dv/dt withstanding capability with a leading edge of 0.6 V_{DWM} amplitude and with a junction temperature close to the permissible maximum. These values are typically on the order of a few hundreds of volts/ μ s for low-sensitivity devices and decrease down to some ten volts/ μ s for highly sensitive devices.

CRITICAL RATE OF RISE OF THE VOLTAGE DURING SWITCHING : $(dv/dt)_c$

1° - Conventional triacs

The susceptibility to dv/dt of the triac in the blocked state is based on the same phenomenon, and leads to values of the same order as in the case of the thyristors. However, in a conventional triac, the two elementary thyristors Th1 and Th2 illustrated by figure 1 (section 1) being strongly coupled, one can expect reactions between these elements, which are liable to affect the blocking capabilities when the current cancels after each reversal of the input voltage polarity.

In extreme cases, this coupling can cause the triac to remain conducting without gate current, through the following process : when, following the suppression of the control signal, the current reverses in the load, for instance, by positive values (*figure 11A*), "internal thyristor" element Th2, which was in the conducting state, keeps stored charges. The discharge of these charges results in a reverse current (curve in full lines of figure 11 B) which can act as gate current for the other "internal thyristor" element Th1 of the triac and, thus, spontaneously fire the triac on the subsequent negative half wave.

However, the risk of spontaneous self-firing of the triac from one half wave to the other, exists only in conditions where, at the same time :

(1) - the reverse current would have a notable amplitude, which would be the case if the slope of the current decays $(di/dt)_c$ at the instant of turn-off were steep, and

(2) - the gate sensitivity intrinsic to each element Th were very high.

With the usual passive loads of fairly linear I/V characteristics, the di/dt on turn-off is proportional to I_{RMS}/T_a . With a 50 or 60 Hz supply mains and a junction temperature lower than t_{vj} MAX, the first unfavourable condition only arises, when the triac controls a very high rms current I_{RMS} (high-power

applications). However, there are risks of high di/dt values occurring on turn-off, even with effective currents of not very high nominal intensity :

a) when the frequency of the ac input voltage is much higher than 60 Hz,

b) or when the triac switches the ac terminals of a single-phase rectifier with inductive load, or, still, in certain cases of switching on polyphase rectifiers,

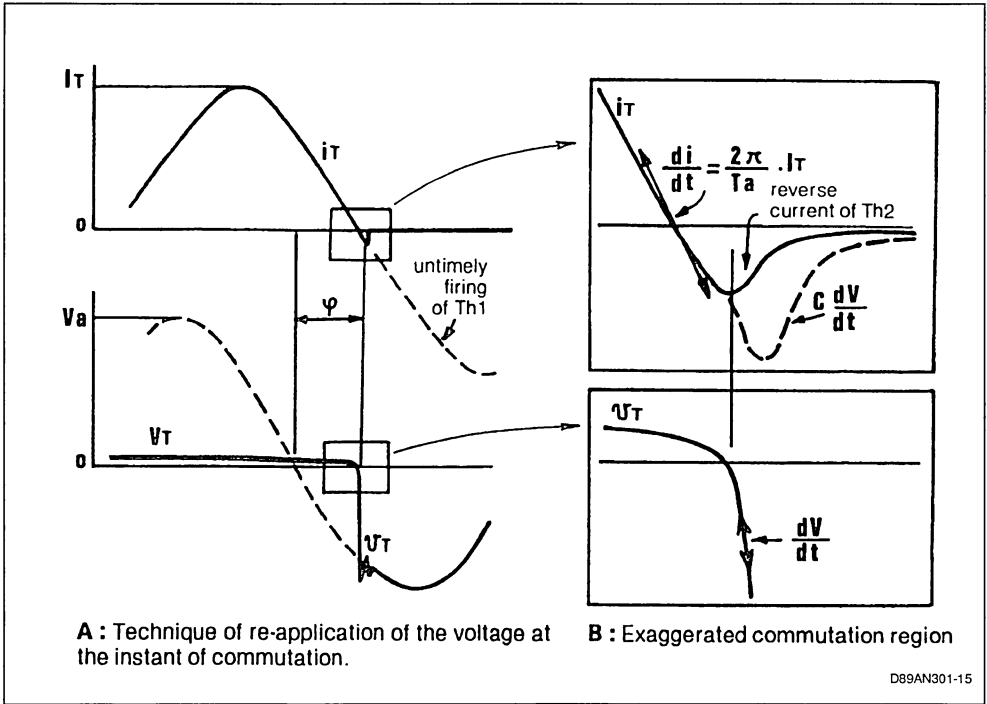
c) or, finally, after the passage of a high current surge, as can be the case when turn-on occurs on a load including a saturable core, or on lamps of very low resistance when cold.

The second unfavourable condition (high intrinsic sensitivity) arises with triacs of low I_{GT} and low I_H , when the junction temperature reaches some hundred degrees Celsius. However, on a resistive load there is a risk of spontaneous self-firing only when the junction reaches an instantaneous temperature higher than the specified limit value. (this situation can arise, for instance, following an overload, or when, through poor knowledge of the transient thermal impedance, the user operates the triac at a small opening angle with high peak currents and a high case temperature).

A second parasitic phenomenon occurs when the load is an inductive one : since the inductive component of the load causes a phase shift of the current with respect to the voltage, the voltage across the triac tends to change, at the instant of turn-off of Th2, from a very low value (V_T at low current) to a high value which is the input voltage value at that instant (*figure 11 A*). The resulting voltage wavefront adds to the reverse current and additional current $C dv/dt$ (in dotted line on figure 11 B) which contributes to the firing of the other element Th1.

Conventionally, the immunity of triacs to self-firing is characterized by the value of dv/dt to be introduced by an inductive load at the instant of switching, in order to cause the spontaneous re-firing of a triac from one half wave to the other.

Figure 11 : Spurious re-firing by "commutating dv/dt" on inductive load (cos ≠ 1).



This "commutating dv/dt" parameter is given by the data sheets for a specified value of di/dt on turn-off (as a general rule, the value corresponding to the nominal operating current at 50 Hz of the triac), and for specified values of the peak voltage and junction temperature (voltage V_{DWM} and maximum permitted temperature, as a general rule).

Figure 12 indicates typical variations of the $(dv/dt)_c$ with respect to the specified minimum value, versus the di/dt on turn-off (relatively to its specified nominal value). These curves show that a lowering of the working intensity, consequently of the di/dt (X-axis) and the junction temperature (T_j) leads to a considerable increase of the triac immunity to untimely firing. Inversely, for a given current, this shows the interest of oversizing the triac current rating in cases where the commutation problems could be critical.

In all usual circumstances, without turn-off di/dt higher than the nominal value for the 50 or 60 Hz supply mains, the most appropriate precautions warranting the triac blocking capabilities at commutation, consist in selecting a device of not too high a sensitivity and, above all, in using a heat sink sufficient to prevent the instantaneous junction temperature from ever exceeding 80° to 90°C. An additional preventive measure in case of an inductive load is the addition, to the triac terminals, of an RC network limiting the rate of rise of the voltage. The dimensioning of such a protective network will be discussed later on.

Like overvoltages, spurious firing actions through dv/dt are detrimental to the triac only when the entail excessive overloads through surge current and di/dt.

Figure 12 : Influence of the Turn-off di/dt and Junction Temperature T_J on the "Commutating dv/dt" of a Conventional Triac.

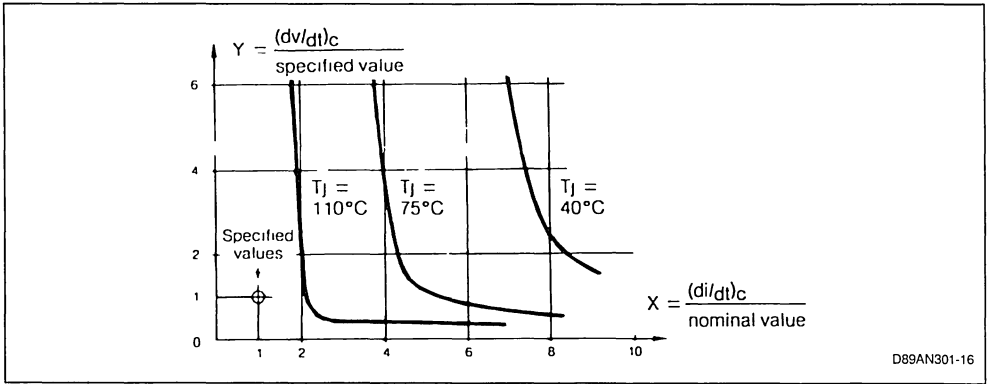
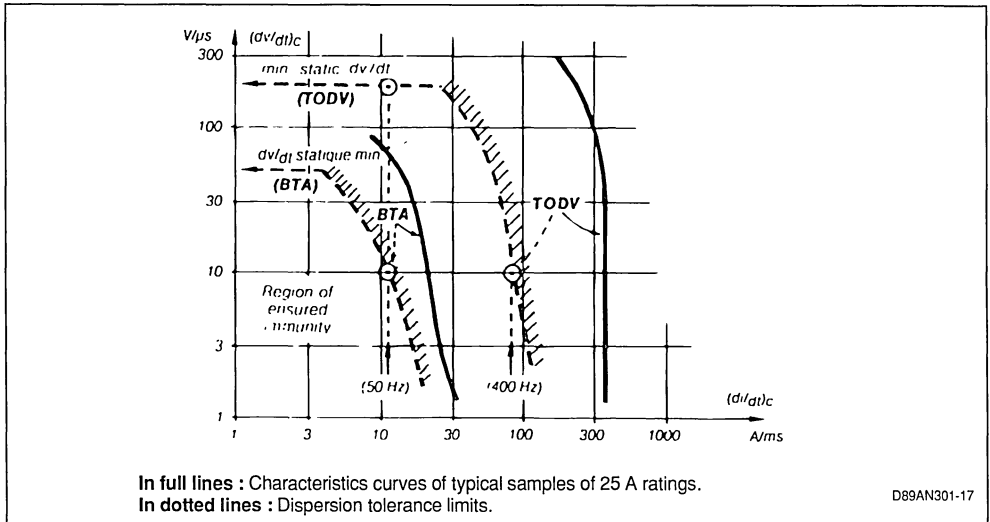


Figure 13 : Comparison of the Immunity to the (dv/dt)_c between an Alternistor (TODV) and a Conventional Triac (BTA), at T_{vj} = 110 °C.



In full lines : Characteristics curves of typical samples of 25 A ratings.
In dotted lines : Dispersion tolerance limits.

2° - Alternistors

For the severe case a), b), c) previously mentioned of high turn-off di/dt values, it is recommended to use preferably SGS-THOMSON Microelectronics triacs presenting the ALTERNISTORS structure.

This structure introduces a decoupling between the two internal thyristors Th1, Th2, which ensures the same blocking capabilities as two anti-parallel connected thyristors, even in "commutating" conditions (but with the advantage of much easier control). This permits warranting a minimum value of (dv/dt)_c, in operation at nominal current on the 50 Hz supply mains, identical

to the static dv/dt (several hundreds of volts/μs). The specification sheets also indicate a (dv/dt)_c value in operation on a 400 Hz supply mains (i.e. for a turn-off di/dt eight times higher than at 50 Hz).

The improvement of the immunity to spontaneous re-firing with respect to the conventional triacs, even when very performing from this point of view, clearly appears on figure 13 which gives, in logarithmic coordinates, the typical curves of (dv/dt)_c versus di/dt, at T_{vj} = 100 °C, for a triac (BTA) and an alternistor (TODV) of the same current rating (25 Arms).

Figure 13 also shows the (circled) representative points of the minimum values specified for each of these devices, and, in dotted lines, an extrapolation defining the limits of the operating region in which immunity to spontaneous refiring is ensured for any device of the family considered.

Some Medium-power triacs of the ALTERNISTOR type show a low gate sensitivity. When the required control current is not available, the user still has the possibility of increasing the effective sensitivity through the addition of a small sensitive triac (TLC series) between A2 and G of the main triac, while still maintaining a high immunity to the $(dv/dt)_c$ (refer to section 3, figure 18 A).

2.4. PROTECTION CIRCUITS

PROTECTION AGAINST CURRENT SURGES AND HIGH CURRENT RATES OF RISE.

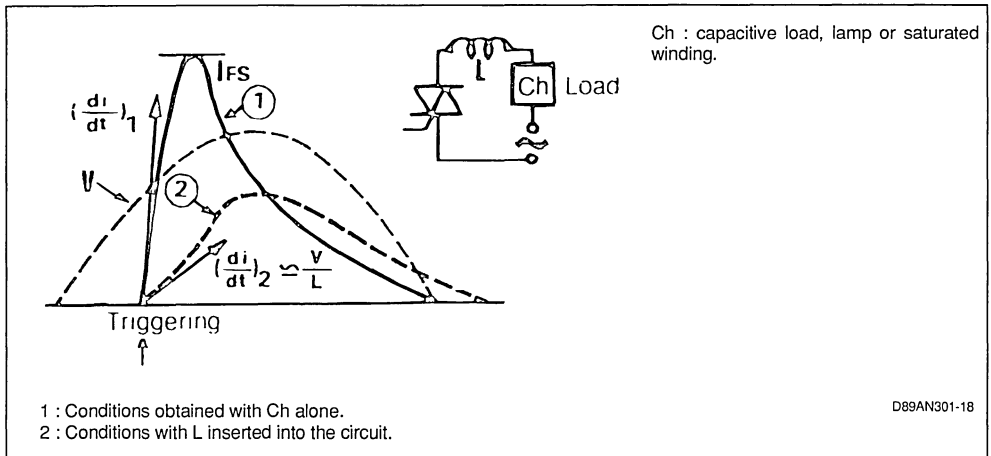
When non-repetitive peak currents are liable to exceed the I_{TMS} specified for the triac, and when their rate of rise is not decreased by the user circuit inductances, it is advisable to protect the triac by

means of an ultra-fast-acting fuse. This fuse will be selected with an " I^2t " value notably lower than the value specified for the triac considered.

The best protection against very short overloads or very high current rates of rise di/dt consists in connecting an inductance in series, as shown by figure 14. An inductance of a few hundreds of microhenrys is sufficient to make sure the current rate of rise will not exceed a few amperes per microsecond, which ensures, even in repetitive conditions, a satisfactory reliability. When this inductance is included in the circuit, the triac has only to be protected against overloads of long duration. An ordinary fuse (but not of the slow-acting type), with a rating equal to one-half or two-thirds of the triac nominal current, can satisfactorily ensure this protection.

It is to be noted that a possible short-circuit current will follow a path closed by the power line leads. Consequently, the inductance of these leads added to that of the load or of an interference filter (when its magnetic core is not too rapidly saturable), is often sufficient to limit the current rate of rise to a permissible value.

Figure 14 : Lowering of the Current Stresses by Means of an Inductance L.



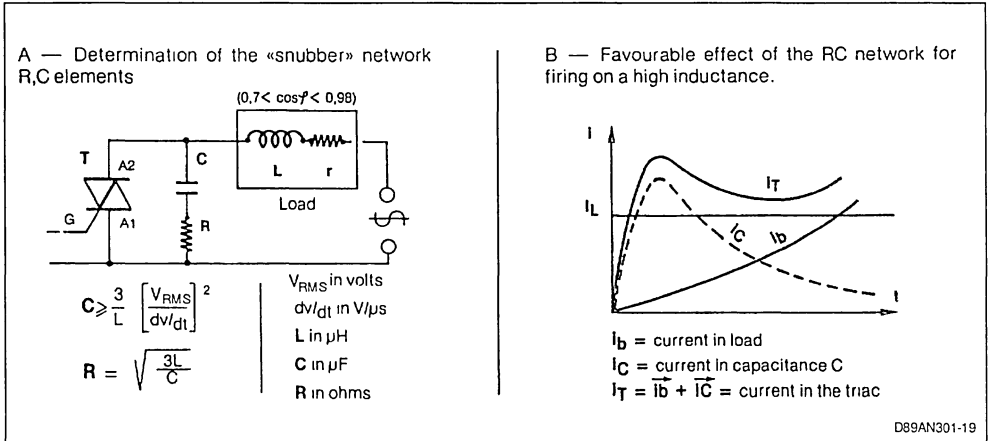
PROTECTION AGAINST UNTIMELY FIRING

1° - Inductive load

With a high load inductance, the process most currently used to eliminate the risks of untimely firing through interferences, or of spontaneous re-firing through $(dv/dt)_c$, consists in connecting an RC network, known as "snubber", to the triac terminals (figure 15). Capacitance C, in conjunction with the

impedance of the load, attenuates the voltage wavefronts transmitted from the mains, or reapplied at commutation on an inductive load. Besides, the energy stored in C in the triac blocking condition, then provides, at the instant of on-triggering, the current necessary to exceed the latching value I_L necessary for the steady firing of the triac (figure 15 B). This effect is particularly useful during operation with a small conduction angle on a high-inductance load.

Figure 15 : Lowering the Risks of Untimely Firing on Inductive Load by Means of an RC Network.



Resistor R in series with C is determined for a damping of resonant circuit R, L, C, close to the critical value; this avoids overshoots which could re-fire the triac through radiation onto the control circuits, or even, at the limit, through exceeding voltage V_M (firing through breaker). The resistor will be selected so that $R = 1.6$ to $1.8 \sqrt{L/C}$.

The minimum value to be taken for the network capacitance C is the larger of the two values :

$$(1) C > \frac{4}{L} \left[\frac{V_{RMS}}{v's} \right]^2, \text{ and } (2) C > \frac{6}{L} \left[\frac{V_{RMS} - \sin \varphi}{V'c} \right]^2$$

$$\text{with } \sin \varphi = \frac{L \omega I_{RMS}}{V_{RMS}}$$

(V_{RMS} = rms mains voltage ; I_{RMS} = rms current in the full-angle conduction mode).

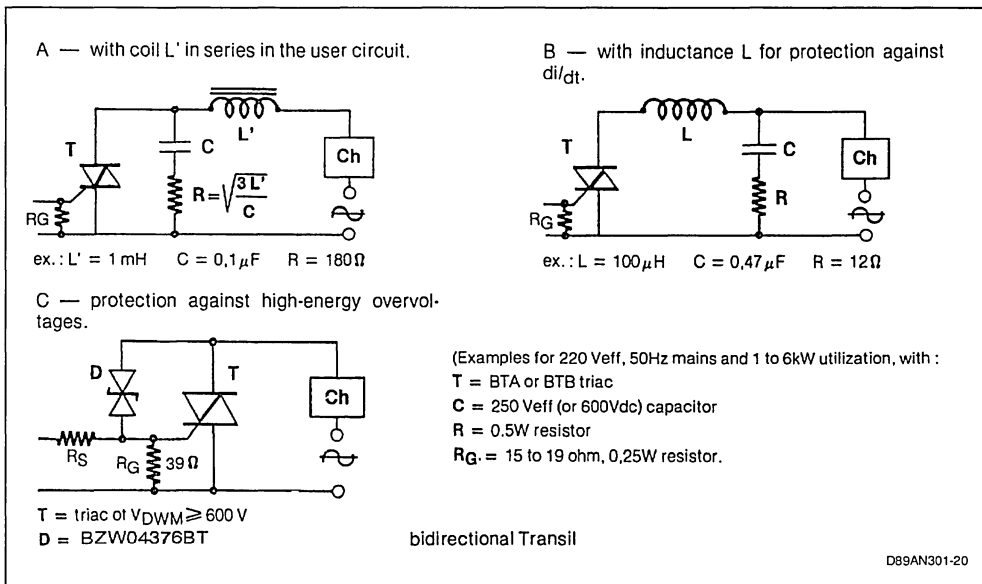
The first inequality, in which $v's$ is the static dv/dt specified for the triac considered, alleviates the effect of short-duration interferences whose amplitude would be of the same order as the peak voltage of supply mains. The second inequality alleviates the commutating dv/dt on inductance, $v'c$ in the conditions of turn-off di/dt as imposed by the utilization considered.

When the triac operates at low current and low instantaneous junction temperature, or if it is of the "alternistor" structure, $v'c$ is generally close to $v's$, and only the first inequality will have to be taken into consideration.

With a conventional triac operating near its nominal current, the second inequality is predominant in operation on an inductive load. For a load $\cos \varphi$ between 0.98 and 0.7, it will be possible to determine C through the simplified expression on figure 15 A.

If $\cos \varphi$ is higher than 0.99, expression (1) should be used for protection against the dv/dt of interferences superimposed on the supply mains. On a 220 V, 50 Hz mains, with a triac whose specified static dv/dt , $v's$ is 50 $V/\mu s$, the minimum capacitance so found exceeds the microfarad when L is equal to, lower than, 75 μH , and its size and price can be considered as prohibitive. In addition, the corresponding value of R being lower than 15 ohms, the repetitive di/dt values imposed on the triac by the discharges of C are detrimental to the triac. When the load inductance is low and not well known, it may be useful to add systematically an inductance of known value (L') to it, as shown by figure 16 A (the interference filter can ensure this function).

Figure 16 : Various Processes for Improving the Protection against Drastic Parasitic Voltage Wavefronts.



2° - Mainly resistive load

With a high current and mainly resistive load ($\cos \varphi$ close to 1), the user circuit will have to be designed, or the triac selected, so that the turn-off di/dt be notably lower than the value specified for the triac (dv/dt)_c. It is then only necessary to take into account the effects of the static dv/dt values and of the parasitic overvoltages.

We have seen (sub-section 2.3) that the SGS-THOMSON Microelectronics triacs can withstand without destruction, firing through breakover or dv/dt, so long as such firing is not followed by an overload in current or in di/dt. Consequently, in applications where occasional untimely triggering into conduction on one or two half waves can be permitted, the "snubber" network is not necessary, as a general rule. However, a solution of compromise with C = 0.1 to 0.22 μF may be useful to prevent untimely firing or low-energy interferences of short duration. The major purpose of resistor R in series with C then consists in limiting the value of the discharge current of C, at each firing or re-firing, whose repetitive di/dt could be detrimental to the triac lifetime. Practically, R will be selected with a value higher than 50 ohms for small triacs, or higher than 15 to 20 ohms for large triacs.

It is also advisable to desensitize the triac by means of a low-value resistor RG, connected between G and A1, at the price of an extra current IG approximately equal to 1 V/RG to be provided for gate control.

Increased protection will be obtained by selecting either the previously mentioned circuit shown by the diagram of figure 16 A, with an iron-core coil L' in series with the load, or the circuit shown by the diagram of figure 16 B, where the small inductance L, in series with the triac, limits the values of the di/dt. The latter configuration not only increases the triac protection against non-repetitive di/dt possibly resulting from untimely firing through overvoltages, but also permits decreasing the repetitive di/dt introduced by the snubber network or, inversely, lowering the impedance of the latter, thus increasing its efficiency.

The triac fired by a pulse with steep leading edge applied to its gate can withstand overloads and di/dt values considerably higher than those it accepts on firing through breakover (overshooting of VM). In cases presenting a risk of high-energy current surges, the triac can be effectively protected by forcing its firing through the gate as soon as the voltage exceeds 30 to 50 % of the mains nominal peak. Figure 16 C shows how this protection can be ensured by means of a bidirectional TRANSIL D connected between A2 and G. The choice of the characteristics of D is quite stringent as regards the satisfactory effectiveness of this arrangement. The TRANSIL family of SGS-THOMSON Microelectronics has been designed to meet this requirement.

3. APPLICATION EXAMPLES

The field of application of the triac is extremely wide. As a matter of fact, it covers the control of all the equipment operating on alternating current. We shall merely give here the diagrams of a few examples of typical applications, and recall, at the end of this note, the general precautions recommended for the utilization of triac (APPENDIX 1).

Before describing these examples, we shall add a few precisions of practical order to the information given in Sub-section 1.3 about the control of triacs, by referring more particularly to Table I.

As can be seen on table I, the best gate sensitivity homogeneity with either polarity of the mains voltage (applied to A2) is obtained in firing quadrants II and III, which corresponds to gate pulses of negative polarity with respect to A1 (figure 17 b). Recent triac control ICs are, generally, designed for this mode of firing.

But, when the latching current constitutes a critical

parameter (operation at very low or highly variable current, or at low conduction angle on an inductive load), it is preferable to control the gate by alternate pulses in accordance with the mains voltage polarity (quadrants I, III, figure 17 a). The switches shown on figure 19 and 20, and the diac controllers which will be described in Sub-section 3.2 operate in these conditions.

When the control circuit does not directly deliver alternate pulses, or when the control power is insufficient with respect to the gate sensitivity of the triac to be used, there always remains the possibility of controlling that triac through low-energy pulses by inserting a sensitive auxiliary static switch between A2 and G. Such a switch can consist either of a small triac of the "TLC" series, (figure 18 A), or of a diode bridge switched by a thyristor of the "TL" series, (figure 18 B). Thus, the main triac will be fired in quadrants I, III, and its gate current automatically adjusted for the amplitude and duration required for steady firing of the triacs.

Figure 17.

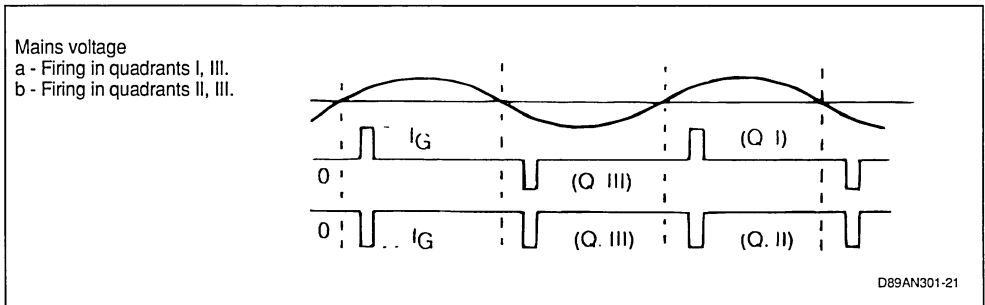
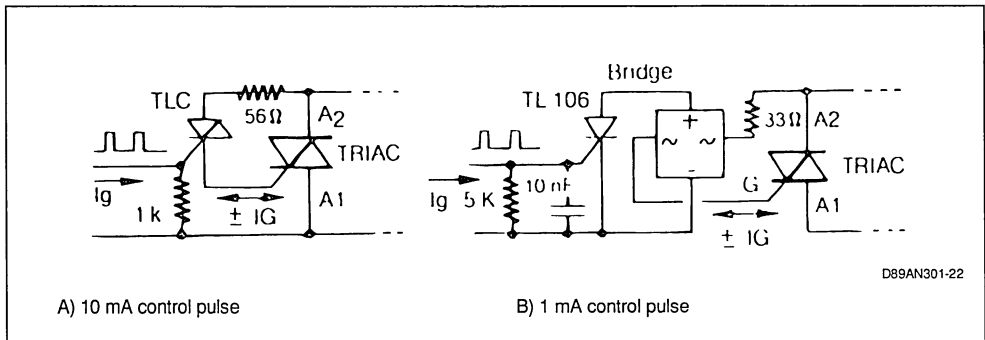


Figure 18.



3.1. STATIC SWITCHES

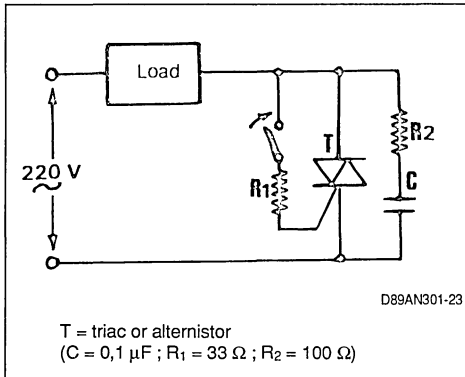
The use of a triac as an "on/off" device in an alternating-current circuit represents the simplest application of that semiconductor switch. Such a utilization offers many advantages with respect to mechanical and electromechanical devices :

- low control power with respect to the controlled power,
- short response time on closing of the circuit, and absence of contact bounce,
- possibility to select the firing instant within the phase,
- in particular, possibility of firing at the zero voltage point, thus minimizing interference caused by the mains and environment,
- no wear related to the number of switching cycles,
- automatic breaking of the circuit at the zero current point, i.e. without arcing, even an inductive load.

MICROSWITCH-CONTROLLED STATIC SWITCH (PERMANENT CONTACT).

With the circuit represented by the diagram of figure 19, the control energy is taken from anode A2 of the triac, i.e. directly from the mains power through the load, which permits providing a gate current of the required intensity. As soon as triac T is fired, the voltage across it almost cancels, as well as the gate current which is then exactly proportioned to achieve steady firing (R_1 is of low value, 15 to 50 ohms, so

Figure 19 : Asynchronous Triggering through Microswitch.



STATIC RELAY INSERTED ON ONE LEAD.

The switch shown by figure 19 can be inserted on one lead, without access to the other mains pole. But, it cannot be directly used for the synchronization on a zero crossing of the AC voltage. However, it is possible to set up a static relay with zero-point

that each re-firing after closing occurs near the zero voltage point, with a sufficiently steep leading edge).

"ON/OFF" SWITCH CONTROLLED BY MOMENTARY-CONTACT SWITCH (fig. 20).

Closing of the "on/off" switch is controlled through a (momentary-contact) push-button switch M ; operation is then ensured by the capacitor current which is in phase quadrature with the input voltage.

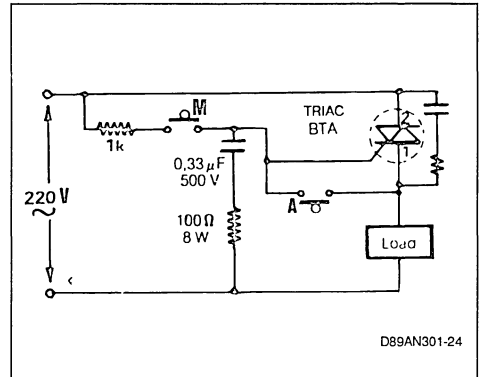
Opening of the switch is then achieved either by short circuiting between the control electrode and electrode "1" of the triac (momentary-contact switch A), or by opening the gate circuit.

STATIC SWITCHES CONTROLLED AT THE "ZERO VOLTAGE POINT".

To meet the requirements of the standards concerning the limitation of interference injected into the mains through electrical house appliances, it is necessary to eliminate any sudden current surge at each firing and re-firing of the triac.

With single-phase voltage and a purely resistive load ($\cos \varphi = 1$), this is achieved by firing the triac with pulses centred on the zero crossing of the mains voltage. But, with a phase shift φ between load current and mains voltage (inductive load or polyphase circuits), it is absolutely necessary to synchronize the gate pulses with the voltage across the triac (see sub-section 1.5) and not with the mains voltage.

Figure 20 : Setup of an «On/Off» Switch.

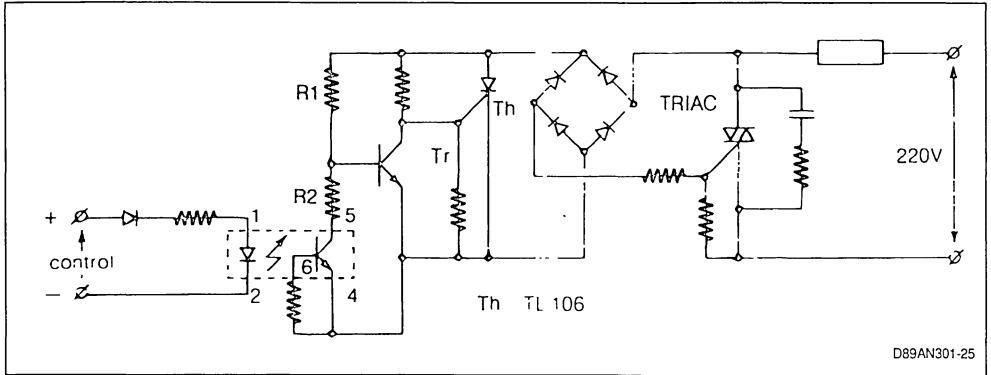


firing, in accordance with the same principle of gate current supply from the voltage across the triac, by replacing the mechanical contact with the arrangement shown by figure 18 b, and by controlling the sensitive thyristor through a photocoupler (fig. 21).

The triac gate pulse is provided by the thyristor. Transistor Tr enables inhibiting firing of the thyristor depending on the instantaneous amplitude of the mains voltage and the photocoupler control. If the photocoupler is not supplied, transistor Tr is continuously saturated. It prevents firing of the thyristor.

When the photocoupler is controlled by the voltage divider consisting of resistors R1 and R2, transistor Tr is blocked only when the mains voltage is close to 0 V. The triac is then controlled at the mains zero voltage point.

Figure 21.



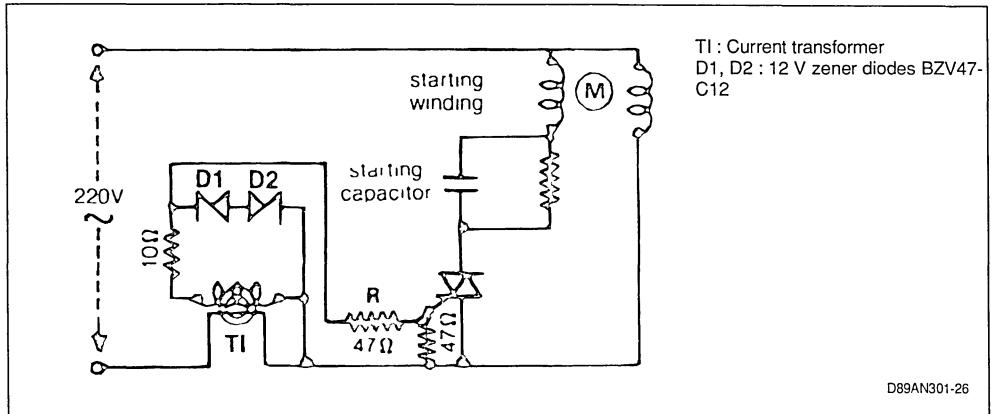
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STARTING OF AC MOTORS (figure 22).

The triac is controlled by means of two zener diodes which detect, on the secondary side of a current transformer, the current surge due to the starting of the motor. The semi-conductor device operates only

during the time required by the motor to reach synchronism. Consequently, it is not necessary to use a large heat sink. But the compromise between I_r and the transformation ratio of TI has to be correctly adjusted.

Figure 22 : AC Motor Starting Control.



TI : Current transformer
D1, D2 : 12 V zener diodes BZV47-C12

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3.2. POWER CONTROLLERS

The systems for burst or phase control mentioned in Sub-section 1.4 (figures 5 and 6) are used to vary the average power delivered to a load (lamp, motor, heating elements, transformers etc).

We shall give the diagrams of a few power controllers as examples. By feeding back to their control terminals the information provided by suitable sensors coupled to the user circuits, it is possible to make up lighting, speed, pressure, temperature, voltage or current regulators.

DIAC CONTROLLERS.

This is the simplest method for power variation through phase control. In spite of its low accuracy, this method is applicable without particular difficulty for power control on resistive loads, or for speed variation of small motors.

To ensure a satisfactory adjustment range, and improve the reversibility of the adjustment, it is advisable to complete the circuit shown by figure 5 b, by an additional RC network, known as "antihysteresis" network (6.8 k Ω and 100 nF on the light dimmer diagrams of figure 23).

Slave control of the phase angle by the ambient lighting, or by an external light phenomenon may be required to ensure a constant illumination level. With the circuit shown by figure 25 a, this will be achieved by

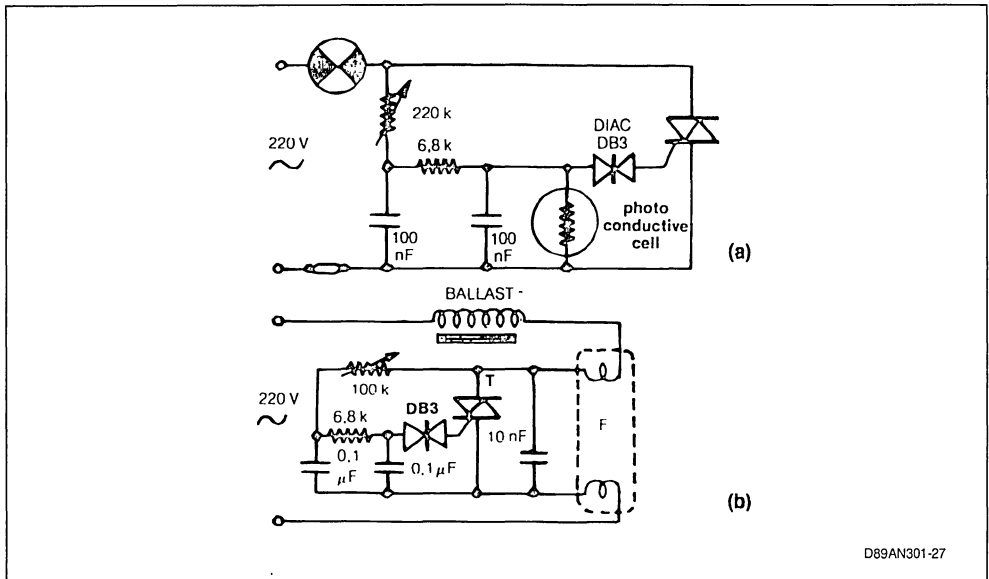
connecting a photoresistor in parallel with the phase-shift capacitor for varying the charging voltage of the latter in accordance with the illumination level.

A variation of the luminous flux of a fluorescent strip light can be obtained in the same manner. This is a particularly attractive application, since the colour of the visible light produced by a fluorescent lamp is almost entirely independent of the luminous intensity, which is not the case with incandescent lamps. With the set-up shown by figure 23 b, highly progressive intensity variation is achieved over a wide luminosity range by connecting the triac in parallel with the fluorescent lamp. Thus, the lamp conduction angle corresponds to the triac off-state angle and, consequently, commences at the beginning of each mains voltage half wave.

Figure 24 illustrates a circuit used for speed control of a fan drive motor. Since this type of motor generally comes to a stop long before the conduction angle has decreased down to the triac turn-off point, no antihysteresis network is required. A limitation of the speed adjustment range (resistor R3, possibly adjustable) may be sufficient to avoid hysteresis problems.

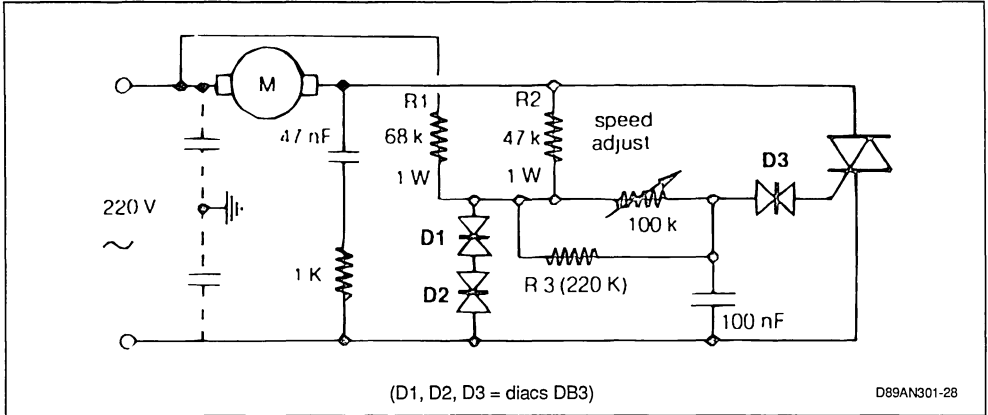
However, in this example a partial antihysteresis effect is accessorially produced by the circuit consisting of R₁, R₂ and diodes D₁, D₂, the main purpose of which is to linearise the speed adjustment and, above all, to render it substantially independent of mains voltages variations.

Figure 23 : Luminosity Adjustment of an Incandescent (a) or Fluorescent (b) Lamp.



D89AN301-27

Figure 24 : Motor Speed Adjustment with Compensation of Mains Voltage Variations.



3.3. SWITCHING OF TRANSFORMERS

As a general rule, the switching of taps on the secondary (*figure 25 b*) does not give rise to any particular overload difficulties : it is only necessary to comply with the previously given instructions relative to thermal dissipation (sub-section 2.1), and operation on inductive load (Sub-sections 1.5 and 2.3), particularly when the load on the secondary is a rectifier.

When switching the primary connections (*figure 25 a*), applying power at a random instant can entail destructive current surges. Such current surges have two origins :

- building up of the magnetizing current to a value twice that of the transformer nominal current,
- remanence of the magnetic circuit consecutive to the preceding turn off, which can lead to its saturation when power is applied.

To avoid these two difficulties, it would be advisable to control the triac at the maximum of the supply voltage, and at a polarity of this voltage opposite to that in which the transformer remained at the preceding turn-off. This can be achieved with the aid of the electronic circuit illustrated by *figure 26*.

Unless the switching of the primary of a transformer of very high induction is concerned, such a sophis-

ticated control circuit is not required, as a general rule, and the following precautions may be sufficient :

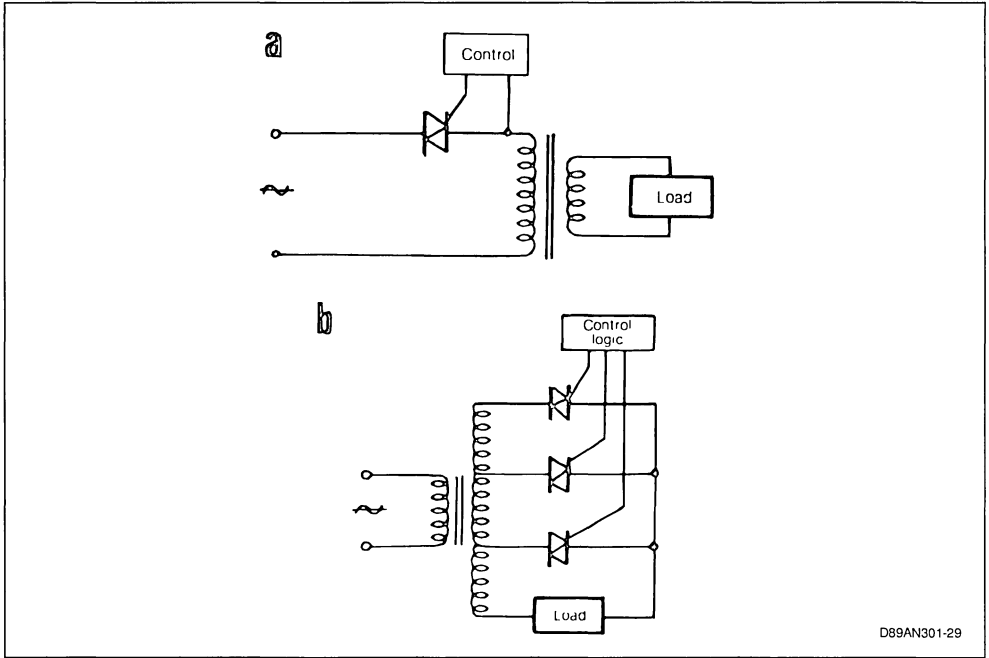
- In the case of phase control, or when there are no difficulties due to interference from the environment, proceed to a starting up at progressively increasing conduction angle. *Figure 27* illustrates the example of a simple controller. Progressive energization is achieved at the opening of switch S through the charge of capacitor C (2 to 10 μ F, 100 V), potentiometer P is used for power adjustment in normal operation.

- For on-off control at the zero voltage point, carry out the first firing of the triac at the beginning of a half wave whose polarity is opposite that of the half wave at the end of which the triac has ceased conducting.

In any case, these cares will be illusory if no precautions (as described in sub-section 2.4) are taken against untimely triac firing on violent interference or mains overvoltages occurring at any instant.

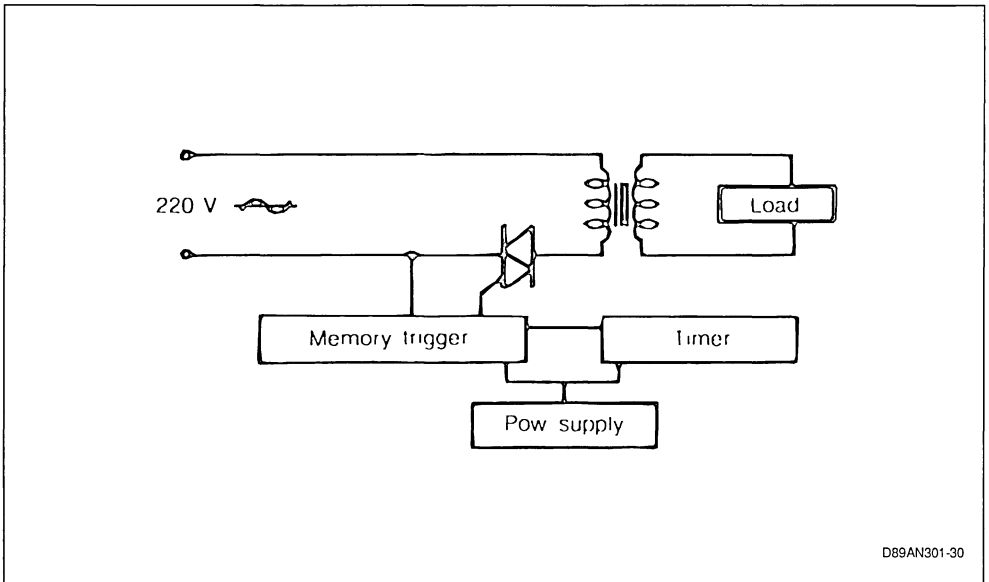
Anyway, it is recommended, for these applications, to use preferably "alternistors" of a rating overdimensioned with respect to the continuous-duty nominal current, and to protect the circuit by means of fast-acting fuses (refer to sub-section 2.2).

Figure 25 : Switching with Triacs on the Primary (a), or Secondary (b) of a Transformer.



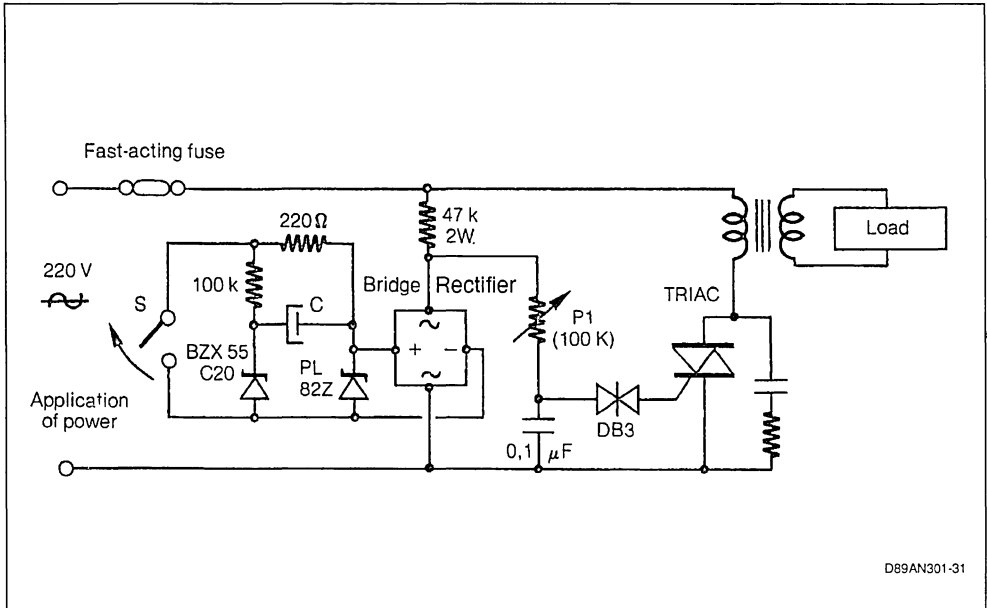
D89AN301-29

Figure 26 : Static sequence switch for transformer primary, taking into account the various requirements imposed in such an application.



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Figure 27 : Diac Controller with Progressive Energization of the Transformer.



D89AN301-31

CONCLUSION

The triac is a switch for alternating current which changes from the blocked to the conducting state when a current or current pulses of any polarity are applied to the control electrode. Turn-on of the device can be achieved with precision in synchronism with the alternating-current input voltage, while turn-off occurs when the current passes through zero following the control signal removal.

This permits setting up systems for the switching, variation or regulation of the power delivered to any load (lamp, resistor, transformer, motor). Provided an ap-

propriate heat sink keeps the junction temperature below the specified maximum value, the service life of the triacs used in these systems is almost unlimited.

Owing to the remarkable overloads capabilities of the triacs and alternistors, users will but exceptionally experience difficulties as regards the reliability of these devices. We have insisted on the various cases of applications requiring particular precautions, in order to give all the information necessary to solve possible problems in the best possible way. Appendix I sums up all useful instruction, in relation with the parameters specified by the individual datasheets.

APPENDIX 1

RELATIVE CONSIDERATIONS TO A FEW TRIAC UTILIZATION PARAMETERS

Parameters	To be Particularly Considered for	Precautions to be Taken (together or separately)
<p>1) Thermal Stresses I_{TRMS} : Triac Nominal Current (rms current at 80 °C case temperature). $R_{th(jc)}$: Junction/case Thermal Resistance; see Sub-section 2.1</p>	<p>Permanent Operation at I_{Teff} in High Ambient Temperature t_{amb}</p> <p>Permanent Operation at Small Conduction Angle, with High Peak Currents</p> <p>Operation with High-frequency γ_{ac} Input Voltage</p>	<p>Suitable Heat Sink Its thermal resistance with respect to t_{amb} should be at the most :</p> $\frac{t_{vj} - t_{amb}}{P} - R_{th(jc)} - R_{th(cd)}$ <p>With : P = Dissipated power : fig. 3, 4 t_{vj} = max. permissible junction temperature : see Sub-section 2.1 and 4) below (untimely firing)</p>
<p>2) Current Stresses I_{TSM} : non repetitive peak overload current (peak current permissible during one period only) di/dt : critical rate of rise of the current at turn-on ; see Sub-section 2.2</p>	<ul style="list-style-type: none"> - Capacitive Load (or capacitor across the triac terminals) - Utilization on Incandescent Lamps (high current in cold condition) - Winding on Saturable Core, transformer primary (magnetizing current) - Risk of Short-circuit Load - Risk of Untimely firing occurring on overvoltages (see 4) below 	<ul style="list-style-type: none"> - Inductive Circuit (addition of L higher than a few hundreds of μH) ; see figure 13 - At least 30 Ω in series with possible capacitor - Triggering at zero voltage point - Triggering through gate pulse of steep leading edge, with peak much higher than specified I_{GT} - Non-delayed fuser rated for less than 2/3 of triac I_{Teff}
<p>3) Holding of Firing Instantaneous output value (current in load) below which the triac turns off (I_H) or does not steadily fire (I_L) after the removal of the gate current (see Sub-section 1.3)</p> <p>a) at End Conduction : holding Current I_H b) at Beginning of Conduction : Latching Current I_L</p>	<ul style="list-style-type: none"> - Highly Variable Loads (low currents) - Highly Inductive Loads (see fig. 7) - Presence of an LC Resonant Circuit (for instance, under-damped interference filter) 	<ul style="list-style-type: none"> - Long trigger pulse or long trains of closely spaced pulses - RC network across triac terminal (see fig. 15) - Triac of Low I_H (sensitive series) - Zero point firing in mode T
<p>4) Untimely Firing a) Firing through breaker (through momentary over-shooting of the maximum specified voltage V_{DMW} ; see sub-section 2.3) b) Firing by dv/dt (critical rate of rise of the voltage in the blocked state-parasitic triac firing, without gate signal, by a voltage wavefront acting on the triac terminals) c) Commutating dv/dt (critical rate of rise of the voltage at commutation-see fig. 11) ; spontaneous triac re-firing through the voltage slope on inductive load at the end of a current half wave</p>	<ul style="list-style-type: none"> - High Mains Interference - Atmospheric interference - Commutator-type Motors, intermittent contacts - Under-dimensioned heat sink - High Input Voltage Frequency - Forced commutation, rectifiers with inductive load 	<ul style="list-style-type: none"> - Limit Junction Temperature t_{vj} to Less than 80 °C (largely dimensioned heat sink) ; see fig. 12 - ALTERNISTOR - RC Network on Triac Terminals (see fig. 15)

APPENDIX II

INTERFERENCE SUPPRESSION OF PHASE-CONTROLLED CIRCUITS

Triac switches, contrary to electromagnetic relays, automatically open when the current passes through zero. Consequently, they cannot produce any substantial interference, except when turn-on does not occur at the "zero voltage" point. But, if possible interference at turn-on can often be tolerated with "on/off" relays triggered at widely spaced intervals, such interference can be extremely disturbing in power control through chopping of the mains wave. This is mainly the case for systems ensuring control by conduction angle on resistive load, where the current wave front (figure 5 b) is generally very fast and, therefore, rich in harmonics. It is then necessary to insert between the device and mains, a filter sufficient to keep the level of the disturbances below that specified by the standards.

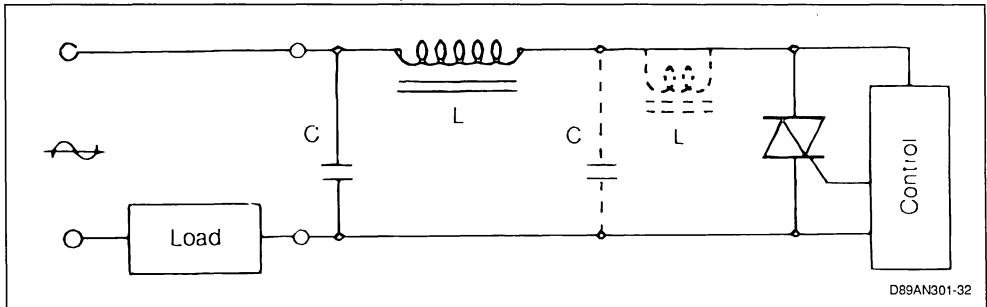
When the switched currents are of low intensity (a few amperes at the most) a simple LC filter like the

one shown by figure 28, will generally be sufficient for the rejection of harmonics in the radio-broadcasting frequency bands (CISPR standards).

The effectiveness of the filter coil is dependent upon the quality of its magnetic circuit, and its value should range from 2 to 5 mH to ensure results complying with the standards. The coil should be wound on a high-loss toroidal core, or be suitably damped, to prevent high-amplitude current oscillations from interrupting the triac conduction, which would cause a relaxation whose disturbing effect would be worse than that of the circuit without filter. The utilization of triacs with low holding current is a precaution against this phenomenon, but there still is a risk of its occurrence when the circuit is underloaded (for instance, 500 W light dimmer used with a 25 W lamp).

Capacitor C, of 0.1 or 0.3 μF , is placed ahead of the filter, on the mains side (note that a filtering capacitor should never be directly connected in parallel with the triac, for it could cause the device destruction through too high a di/dt on turn-on).

Figure 28 : Simple Interference Filter L, C (the addition of L', C' improves, if necessary the rejection of the interference symmetrical components).

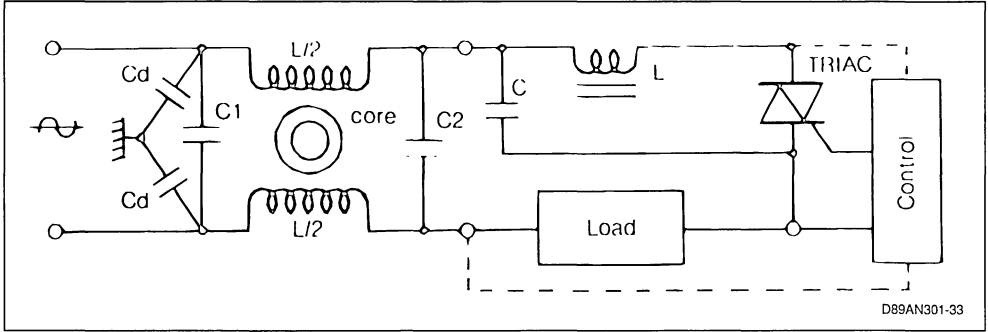


To comply with the European standards (EN 50.006 or NF-C70-100) relative to the reinjection of the lower-rank harmonics into the mains power leads, it is necessary, particularly when the involved powers are high, to resort to more complex filtering, taking into account not only the symmetrical components of the disturbing voltages (in differential between conductors), but also its asymmetrical components (in common mode, between conductors and ground).

The diminution of the symmetrical components can be improved by means of a pi filter C, L, C' (dotted line on figure 28). Inductance L' connected in series with the triac is necessary to limit the repetitive di/dt at each firing of the triac, due to capacitor C' added to complete the pi filter.

Diminution of the interference asymmetrical components is achieved by decoupling each mains power lead to ground (appliance chassis) through capacitors Cd. To comply with the rules relative to the protection of persons against electric current, the value of these capacitors is practically limited to 15 or 20 nF for appliances with Class II insulation, and to only 2 to 3 nF for appliances with Class I insulation. The rejection of asymmetrical components can possibly be improved by breaking down the filter inductance L into two opposite-coupled windings respectively connected to one of the mains power leads on the input of the system consisting of the triac, its control and the load (figure 29).

Figure 29 : Improved filtering taking into account the interference asymmetrical components.



In the most critical cases, a double pi element may be required for the diminution of the lower-rank harmonics of the symmetrical components. As a general rule, the determination of the filter and the

location of the various elements and ground connections require the possibility of experimental verification by specialized technicians.

D89AN301-33

IMPROVEMENT IN THE TRIAC COMMUTATION

P. Rault

In the last few years, the use of triacs has spread to all areas of electronics, including domestic appliances and industrial applications.

The use of triacs has been traditionally limited by their switching behavior in applications where there is a risk of spontaneous firing after conduction. In order to obtain the required reliability in today's equipment, the designer must take a certain number of precautions: over dimensioning of the device, switching aid networks (snubber), significant margin of security of the junction temperature, etc. This generally involves additional costs.

After a brief discussion of commutation problem when a triac is turned off, this article will describe the progress made in this area and the newest possibilities now offered to triac user thanks to the new series Logic Level and SNUBBERLESS™ triac.

THE COMMUTATION PROBLEM OF THE TRIAC

In its electrical representation the triac can be compared to two thyristors mounted in anti-parallel and coupled with a control device which allows activation of this AC switch with only one gate (fig. 1a).

In considering the structure of a triac (fig. 1b), one notices that the conduction zones, corresponding to these two thyristors and which control the current in one direction and then in the other, narrowly overlap each other and the control zone.

During the conduction time, a certain quantity of charges is injected into the structure. The biggest part of these charges disappears by recombining during the fall of the current in the circuit, while another part is extracted at the moment of blocking by the inverse recovery current. Nonetheless an excess charge remains, particularly in the neighboring regions of the gate, which can provoke in certain cases the firing of the other conduction zone at the moment when the supply voltage of the circuit is reapplied across the triac. This is the problem of commutation.

For a given structure at a determined junction temperature, the switching behavior depends on:

1/ The quantity of charges which remains at the moment when the current drops to zero. This number of charges is linked to the value of the current which was circulating in the triac approximately 100 microseconds before the cut-off. (This time corresponds to two or three times the life time of the minority carriers). Thus, the parameter to consider here will be the slope of the decreasing current which is called the commutating di/dt , or $(di/dt)_c$ (fig. 2)

2/ The speed at which the reapplied voltage increases at the moment when the triac turns off, which is called the commutating dv/dt , or $(dv/dt)_c$ (fig. 2)

A capacitive current, proportional to the $(dv/dt)_c$, flows into the structure, and therefore injected charges are added to those coming from the previous conduction.

Figure 1 : (A) Simplified equivalent schematic of triac circuit.
(B) Example of a triac structure.

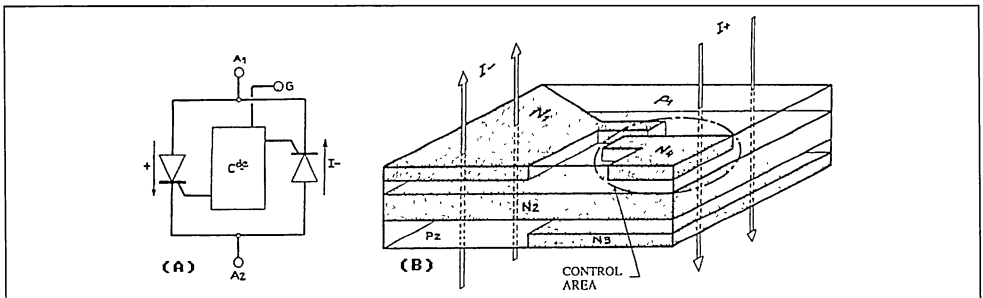
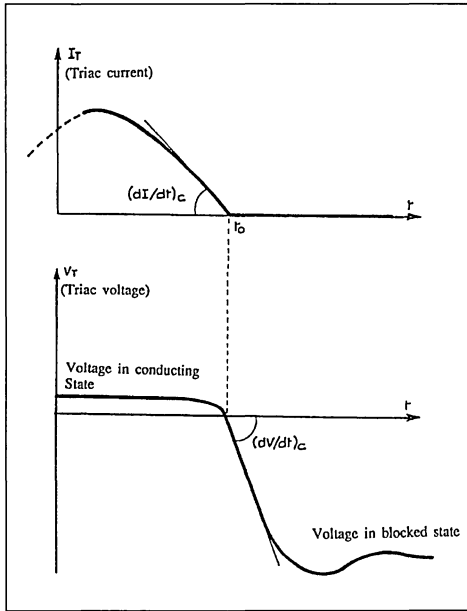


Figure 2 : Triac voltage and current at commutation.



CHARACTERIZATION

In order to characterize the switching behavior of a triac when it turns off, we consider a circuit in which we can vary the slope of the decrease in current $(di/dt)_c$. In addition, we control the slope of the reapplied voltage by using, for example, a circuit of resistors and capacitors connected across triac to be measured. For a determined $(dv/dt)_c$, we progressively increase the $(di/dt)_c$ until a certain level which provokes the spontaneous firing of the triac. This the critical $(di/dt)_c$ value.

Therefore, for different $(dv/dt)_c$ values, we note the critical $(di/dt)_c$ value for each sample. This makes possible to trace the curve of the commutation behavior of the triac under consideration.

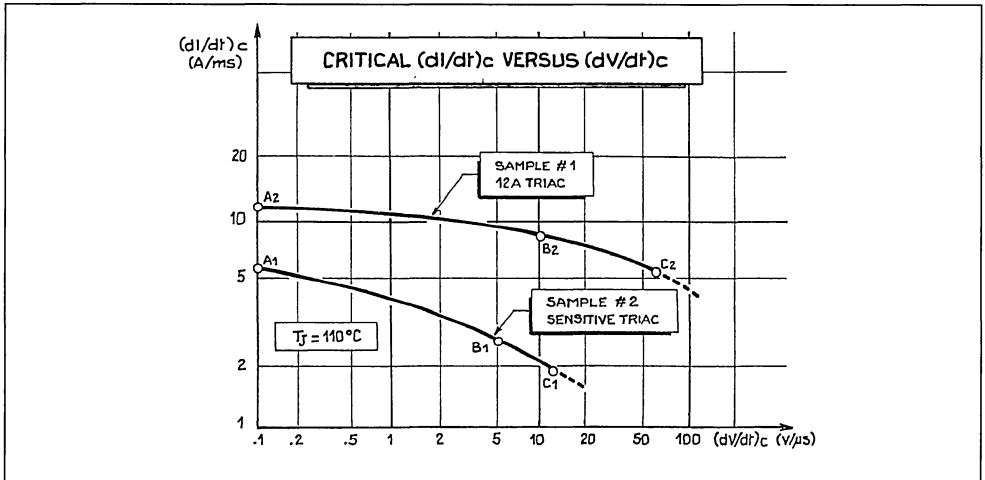
Figure 3 represents the results obtained with a standard 12 Amp triac (I_{GT} 50mA) and a sensitive gate, 6 Amp triac (I_{GT} 10mA). For standard triacs the critical $(di/dt)_c$ is slightly modified when we vary the $(dv/dt)_c$. For sensitive gate triacs, this parameter noticeably decreases when the slope of the reapplied voltage is increased.

Figure 3 : Critical $(di/dt)_c$ versus $(dv/dt)_c$ (below the curve the triac turns on spontaneously.)

A1 and A2 : The rate of re-application of the off-state voltage of these points corresponds to the mains (sinusoidal wave form) at zero crossing.

B1 and B2 : The $(dv/dt)_c$ is limited by a snubber at the values generally specified in the data sheets ($5V/\mu s$ or $10V/\mu s$).

C1 and C2 : These points are obtained without snubber.



In practice, the current wave form, and thus the $(di/dt)_c$, is imposed by the circuit. Generally we cannot change it.

So, in triacs applications it is always necessary to know the $(di/dt)_c$ of the circuit in order to choose a triac with a suitable critical $(di/dt)_c$. This is the most important parameter.

Suppose a circuit in which the $(di/dt)_c$ reaches 15 A/ms. The triac N°1 characterized by the upper curve in figure 3 is not suitable in such a circuit even if the $(dv/dt)_c$ is reduced nearly to zero by connecting a huge snubber network across it.

APPLICATIONS IN BASIC CIRCUITS

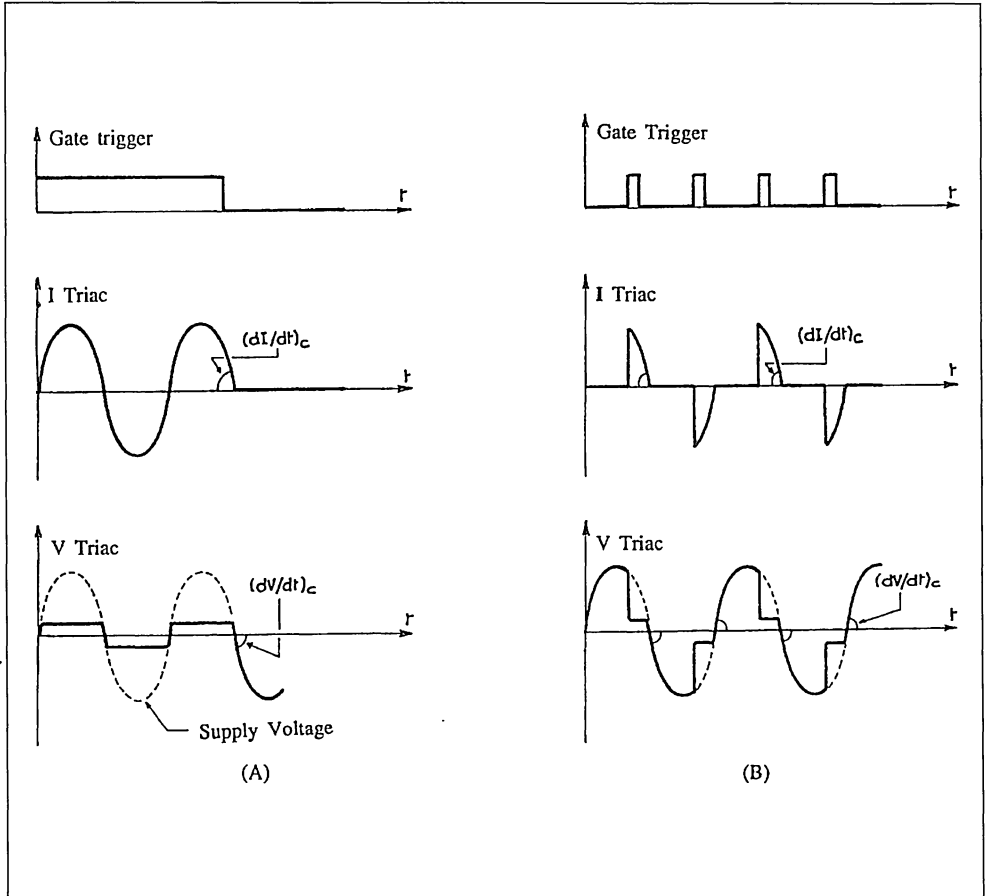
When considering the constraints in commutation at the turn off of a triac, we can distinguish two cases:

1/ The use of a triac on resistive load (fig. 4)

In this case the current and the voltage are in phase. When the triac switches off (i.e. when the current drops to zero), the supply voltage is nullified at this instant and will increase across the triac according to the sinusoidal law :

$$V = V_m \sin \omega t$$

Figure 4 : Current and voltage wave forms for resistive loads
 (A) Case On / Off switching
 (B) Case of phase control



APPLICATION NOTE

Example :

For the European mains of $V_{rms} = 220$ volts at 50Hz, the slope will be:

$$(dv/dt)_c = V_m \times \omega = V_{rms} \times \sqrt{2} \times \omega = 0.1 V_{\mu}S$$

This relatively low $(dv/dt)_c$ corresponds to points A1 and A2 on the curves in figure 3. As far as the $(di/dt)_c$ is concerned in the circuit, it depends on the load. For a resistance of loads R and under a V_{rms} voltage, we will have:

$$(di/dt)_c = I_m \times \omega = (V_{rms} \times \sqrt{2}/R) \times \omega$$

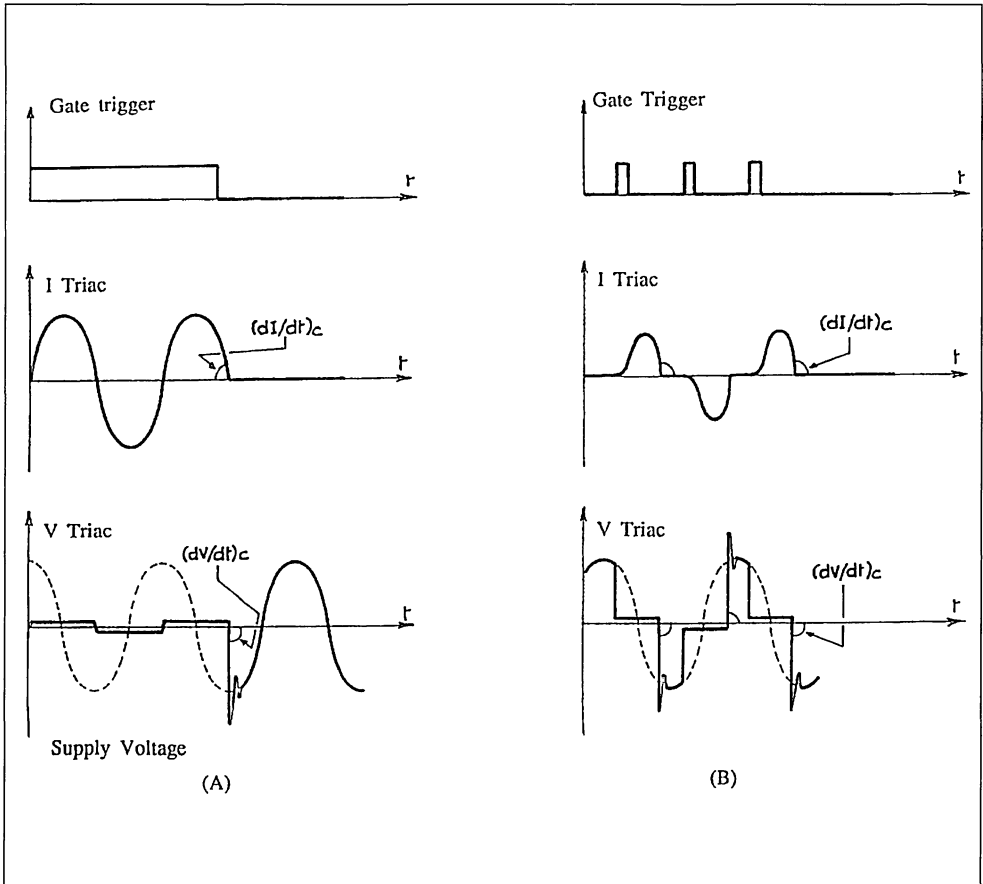
2/ The use of a triac on inductive load

In this case there is a phase lag between the current and the supply voltage (fig. 5).

When the currents drops to zero the triac turns off and the voltage is abruptly pushed to its terminals. To limit the speed of the increasing voltage, we generally use a resistive/capacitive network mounted in parallel with the triac. This "snubber" is calculated to limit the $(dv/dt)_c$ to 5 or 10 volts/ μ S according to the specified value in the data sheet. This case corresponds to points B1 and B2 in figure 3. The $(di/dt)_c$ is also determined in this case by load impedance (Z) and the supply voltage.

Figure 5 : Current and voltage wave forms for inductance loads

- (A) Case On / Off switching
- (B) Case of phase control



THE USE OF A TRIAC WITHOUT A SNUBER NETWORK

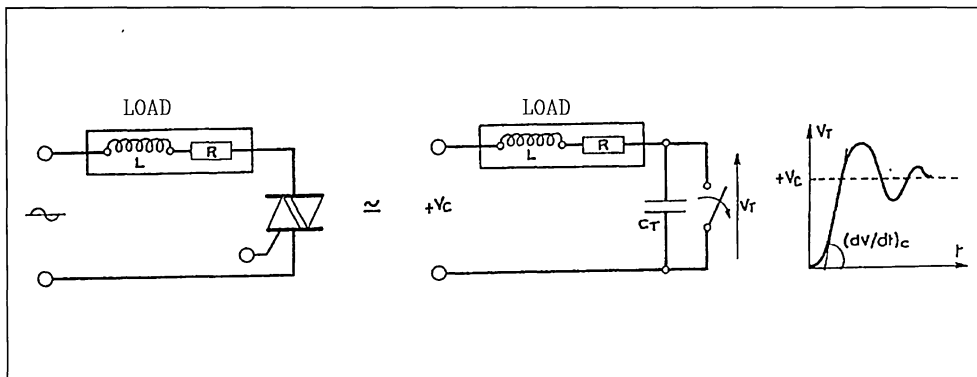
The triac can thus be considered as a switch which turns off at the moment when the current is cut off in the damped oscillating circuit constituted by the loads L and R and the internal capacity of the triac C_t (fig. 6). In the case of a pure inductive load, the maximum reapplied (dv/dt) is:

$$(dv/dt)_c = \sqrt{2} V_{rms} \times I_{rms} \times \omega / C_t$$

For example, the internal capacitance of a 12 Amp triac is about 70pF. Therefore, on inductive load, the maximum (dv/dt)_c without snubber will be limited to 50 or 100 V/S according to the characteristics of the load.

It is interesting to know the behavior of the triac, in particular the critical (di/dt)_c value, in these conditions. This characterization corresponds to the points C1 and C2 of the curve fig 3.

Figure 6 : Triac commutation on an inductance load without a snubber network



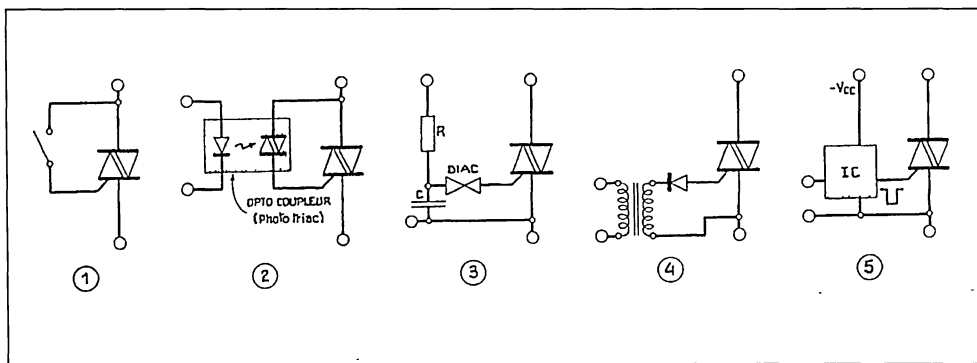
A progress: THE NEW TECHNOLOGY

To make significant progress in the triac area is to essentially improve the commutating behavior at the turn off of the triac. In other words the critical (di/dt)_c has to be improved.

In order to reach this goal, a new structure has been developed. In this structure, the different active zones have been de-coupled to the

maximum in such a way as to separate the elementary thyristors and the gate area. This is made possible by sacrificing the gate triggering in the fourth quadrant. In practice this does not pose a problem because the gate drive circuits of a triac generally use two of the third first quadrants. (fig. 7)

Figure 7 : Basic gate drive circuits (the fourth quadrant is not used)



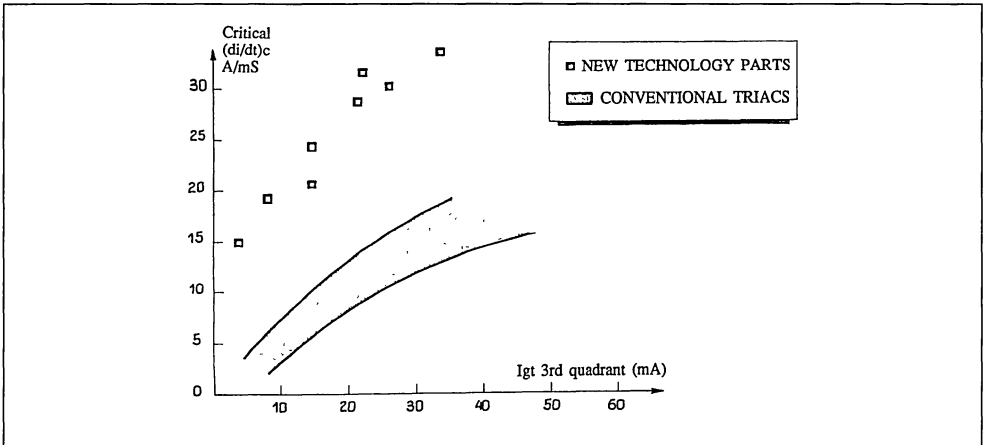
APPLICATION NOTE

For a given technology, the commutating behavior of triacs depends on the sensitivity of the gate. The correlation between the critical $(di/dt)_c$ and the gate current for 12 Amp triacs is represented in figure 8.

In the same chart, we can see the results obtained with conventional triacs versus the new technology triacs. As can be seen, the progress that has been made at this level is significant.

1/ The performances and specifications

Figure 8 : Correlation between commutating behavior and sensitivity.
(Measurements performed on several lots of 12 A triacs)



The new technology has been put into place with the manufacturing of the two new series, Logic Level and SNUBBERLESS Triacs. In the data sheets of these new triacs a critical $(di/dt)_c$ limit is specified at the maximum junction temperature (T_j max).

a- Logic Level triacs

In this category we consider sensitive triacs in which the maximum gate current (I_{GT}) is 5mA for the TW type and 10mA for the SW one.

In the data sheets of the Logic Level triacs a minimum $(di/dt)_c$ is specified for the following cases:

- * Resistive load with a $(dv/dt)_c$ of 01.V/ μ s.
- * Inductive load with a $(dv/dt)_c$ of 20 V/ μ s

For example the 6 Amp triac is specified as follows:

Symbol	Test conditions		Quadrant		Suffix		Unit
					TW	SW	
I_{GT}	$V_D = V_{DRM}$ $I_G = 90$ mA	$T_j = 25^\circ\text{C}$	I - II - III	TYP	2	2	μ s
$(di/dt)_c$ *	$dV/dt = 0.1$ V/ μ s	$T_j = 110^\circ\text{C}$		MIN	3.5	4.5	A/ms
	$dV/dt = 20$ V/ μ s			MIN	1.8	3.5	

* For either polarity of electrode A_2 voltage with reference to electrode A_1 .

b- SNUBBERLESS TRIACS

This series of triacs presently covers the range 6 to 25 Amps with gate currents of 35mA (CW type) and 50mA (BW type) according to the type required. This series has been specially designed so that the triacs switches from the on state to the off state without the use of an external snubber circuit.

Whatever the nature of the load, there is absolutely no risk of spurious firing at the turn off of the triac as long as it is functioning under the specified $(di/dt)_c$ value.

The SNUBBERLESS triacs are specified at critical $(di/dt)_c$ values which are greater than the decreasing slope of the nominal current in a sinusoidal configuration. For example, the slope of the current in a triac conducting 16 Amp when the current drops to zero is:

$$(di/dt)_c = I_{rms} \times \sqrt{2} \times \omega = 7A/mS \text{ at } 50Hz$$

The BTA/BTB16-600BW is specified at $(di/dt)_c = 14A/ms$.

The following table summarizes the characteristics of the BW, CW SNUBBERLESS triacs which are presently available:

TYPE	CURRENT / VOLTAGE	SUFFIX	I_{GT} MAX (mA)	STATIC dV/dt MIN (V/ μ s)	WITHOUT SNUBBER
					$(di/dt)_c$ MIN (A/ms)
BTA / BTB	06A 200 to 800V	BW	50	500	5
		CW	35	250	3.5
BTA / BTB	08A 200 to 800V	BW	50	500	7
		CW	35	250	4.5
BTA / BTB	10A 200 to 800V	BW	50	500	9
		CW	35	250	5.5
BTA / BTB	12A 200 to 800V	BW	50	500	12
		CW	35	250	6.5
BTA / BTB	16A 200 to 800V	BW	50	500	14
		CW	35	250	8.5
BTA / BTB	20A 200 to 800V	BW	50	500	18
		CW	35	250	11
BTB	24A 200 to 800V	BW	50	500	22
		CW	35	250	13
BTA	26A 200 to 800V	BW	50	500	22
		CW	35	250	13

2/ The advantages and Applications

a - Logic Level

The goal of these triacs is to be controlled directly by logic circuits and microcontrollers like the ST6 series:

Outputs of ST6 can sink currents up to 20mA per I/o line, and therefore drive TW and SW.

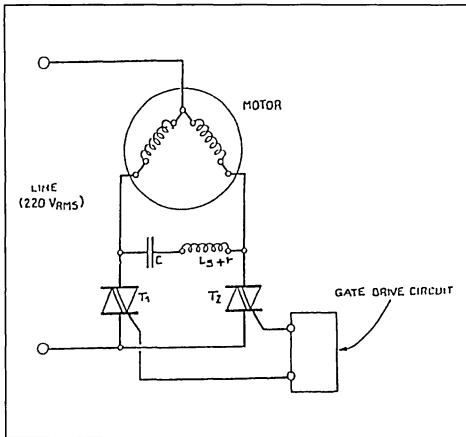
These triacs are ideal interface for power components supplied by 110 or 220 volts, such as valves, heating resistances, and small motors.

The specification of the critical $(di/dt)_c$ value on both resistive and inductive loads allows one

1/ to know the margin of security of the circuit in relation to the risk of the spurious firing, which results in improved reliability, and

2/ to optimize the performance of the triac to be used, which results in a cost reduction.

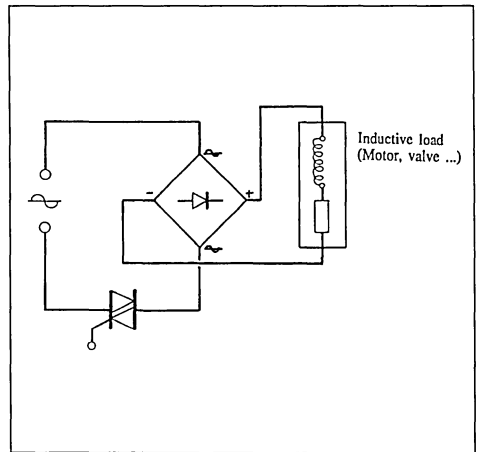
**Figure 11 : Motor control circuit using
SNUBBERLESS triacs**
($L_s + r$ = network for series protection)



2. Motor drive circuits. Figure 11 shows an inversion circuit of an asynchronous motor where spurious firing of the triac, normally assumed to be in off- state, must be absolutely be avoided.

The critical $(di/dt)_c$ of SNUBBERLESS triacs is greater than the slope of the nominal current of the specific type under consideration. This is important for several applications, including : Circuits in which the $(di/dt)_c$ in a transient state is greater than in the steady state. This is the case for universal motors controlled by AC phase control circuit. The table in figure 12 shows how to the use of a SNUBBERLESS triac can optimize the efficiency of the circuit.

**Figure 13 : Example of a circuit with high
 $(di/dt)_c$**



Circuits which generate wave forms with a very high $(di/dt)_c$, such as inductive load supplied by a diode bridge (fig. 13). It is only limited by the parasitic inductance of the AC circuit.

Figure 12 : Universal motor control : Triac choice must comply with maximum $(di/dt)_c$
For example, a SNUBBERLESS 10 A triac is sufficient to control
a 110 V AC 600 W moytor

POWER	SUPPLY VOLTAGE	NOMINAL CURRENT	MAX CURRENT TO CONTROL	TRIAC RANGE	$(di/dt)_c$ MAX (1)	STANDARDS TRIAC	SNUBBERLESS TRIAC
600 W	220V/50Hz	3 ARMS	3,5 A	6 A	6 A/ms	BTA10-600B	BTA06-600BW
	110V/60Hz	6 ARMS	7 A	10 A	7 A/ms	BTA16-400B (2)	BTA10-400BW
1200 W	220V/50Hz	6 ARMS	7 A	10 A	7 A/ms	BTA16-600B	BTA10-600BW
	110V/60Hz	12 ARMS	14 A	16 A	15 A/ms	BTB24-400B	BTA20-600BW

(1) Maximum transient $(di/dt)_c$. This parameter depends very much on the type of the motor.

(2) This type specified at 7 A/ms munimum can be too small certain applications could need 25 A standard triac.

CONCLUSION

Thanks to the recent progress made in triac technology, the designer now has at disposal devices with a commutating behavior which is compatible with all applications in the 50 or 60Hz range. This includes phase control and static commutation for loads going from a few watts to several kilowatts.

The capability of this new generation of triacs allows :

1/ To increase the reliability of circuits, particularly where there is a risk of spontaneous firing even in the most difficult configurations.

2/ To reduce the cost by using sensitive gate, LOGIC LEVEL triacs without the need for an interface between the gate and the logic circuit, or utilizing SNUBBERLESS triacs which are specified without a resistive/capacitive network.

Additionally, the limit of the $(di/dt)_c$ parameter is now listed in SGS-Thomson Microelectronics data sheets.

This permits the optimization of the circuit by specifying stricter guidelines in the choice of the component.

**SEMICONDUCTOR DEVICES
INTELLIGENT POWER**



AN INTRODUCTION TO INTELLIGENT POWER

by A. Hayes

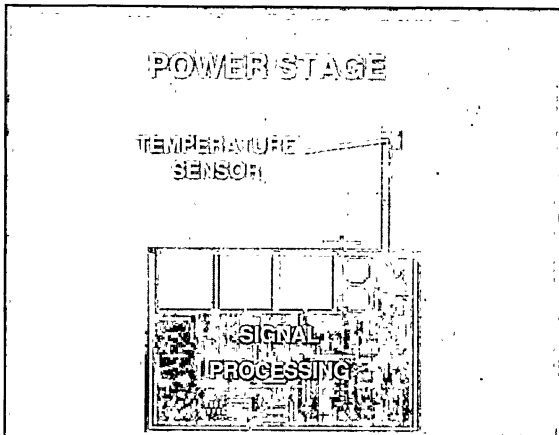
ABSTRACT

This paper gives an overview of one of the fastest growing and most exciting areas of power electronics: Intelligent Power technology. It explains what the term Intelligent Power means, why intelligent power is needed, where it is applied, and finally the technologies involved in its construction.

1. INTRODUCTION

To achieve optimum performance, the power element of a system may require a considerable amount of supplementary circuitry: circuits to protect it from harsh conditions, circuits to ensure that it switches in the most efficient way possible, and, increasingly, circuits to feed back information on the status of the power stage back to

Figure 1: Layout of an Intelligent Power chip



control logic. The need for these circuits can make the design of the power stage complex, and can require a lot of components and board space.

One solution to this problem is to integrate all of the protection, drive and feedback circuitry along with the power element on a single chip - in effect giving the device "intelligence". This concept forms the basis of intelligent power technology.

2. WHAT IS INTELLIGENT POWER?

The additional circuits required for safe, reliable and efficient operation of a power transistor fall into three basic categories:

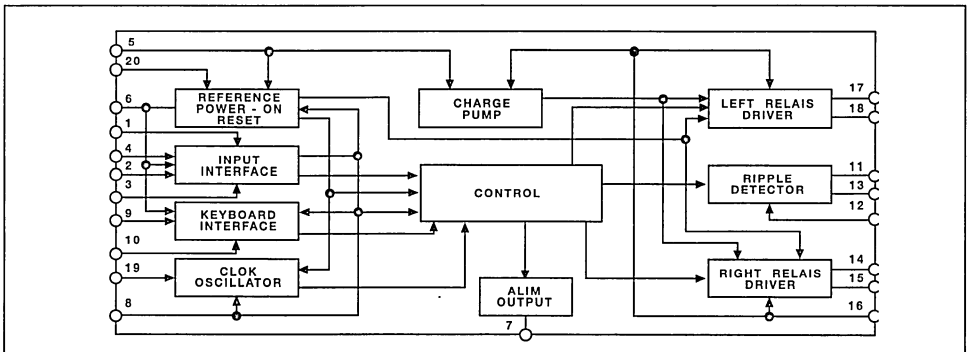
- i) Circuits to drive the device, compensate for different types of loads (inductive, capacitive etc.), to reduce losses and optimize switching speed.
- ii) Circuits to protect the chip (and surrounding components) from destruction by, for example, excessive current, voltage or temperature.
- iii) Logic level control and interface circuits: the use of simple logic-level systems, microprocessors and microcontrollers in the control of power systems has become widespread, and it is often necessary for the power stage to interface with logic-level devices to allow transfer of information; both control information passed from the

controller to the power stage, and status information (for example fault alarms) passed back from the power stage to the controller. Standard power MOSFETs and bipolar transistors require driving voltages or currents greater than those which can be supplied by logic level circuits.

If the demands placed on the protection and drive circuitry are particularly severe (for example when the system operates in a harsh environment), or where the application imposes a particularly exacting set of constraints, design of these circuits may require considerable effort on the part of the designer, and may result in a high component count, with attendant problems of large board space requirement, reduced circuit reliability and increased assembly costs.

Intelligent Power technology eases these problems by integrating both low voltage interface, drive, protection and control circuitry, and high power transistors on the same chip. This gives the system designer a device which will protect itself, switch efficiently and allows easy and flexible control, that is enclosed in a single package and requires only a few external components. This can help to reduce system design time considerably. The functional blocks of a typical device are shown in fig. 2.

Figure 2: Functional blocks of a typical Intelligent Power device - car window lift controller



3. AREAS OF APPLICATION

Intelligent Power devices find most use where there is a need for good protection, high reliability and compactness, and where logic level compatibility is required. In some cases the protection features they offer, for example over temperature protection, are difficult or impractical to implement with discrete components (it is impossible to monitor the junction temperature of the power switch in any other method), and so they are the only real option.

3.1 Automotive systems

Electronic systems contained within cars must be able to withstand very harsh conditions. Physically, they are subjected to vibration and extremes of temperature, while electrically, inductances such as those in the ignition system and the alternator give rise to large voltage spikes and interference. Short circuits can easily occur, causing large currents to flow.

These conditions can make the design of a reliable circuit using conventional parts difficult in automotive systems: a great deal of protection must be built in, leading to a large number of components. This gives rise to two problems: firstly, the space to mount such a circuit may be restricted; and secondly, the larger the number of components, the greater the risk of system breakdown due to failure of solder joints caused by the vibration. The possibility of system breakdown also means that ease of replacement and hence system simplicity are an advantage. Thus Intelligent Power devices offer an attractive alternative to conventional devices, and in some cases are the only alternative to a mechanical solution.

Additionally, as the price of microprocessors falls, they are increasingly being used to control automotive systems (in particular engine management systems), and so direct logic-level interfacing is an advantage.

The processing and problem solving power available in the microprocessor, in conjunction with the fault detection and reporting capabilities of intelligent power devices (which are effectively acting partly as sensors) means that the whole process can be carefully controlled and adjusted, and it may even be possible for adaptive changes to be made in the case of faults to ensure continued safe operation. Thus intelligent power devices help to improve engine efficiency and system reliability.

The use of intelligent power devices will increase dramatically with the development of multiplexed automotive systems. In conventional systems, a large amount of wiring is required to carry information between all the electronic control elements and the central controller. In multiplexed systems, instead of employing a set of wires for each individual electronic element, a single digital serial communications bus connected to all elements is used. This bus is constantly monitored by all the elements of the system, which identify the commands relevant to them by means of an individual code.

By reducing the amount of wiring in the car, this technology improves system reliability and flexibility, cuts hardware, assembly and testing costs, and reduces the car's weight. However, its digital nature means that the ability of the power devices of the system to interface with and preferably interpret digital signals is very important, and so intelligent power devices will be very attractive in this field.

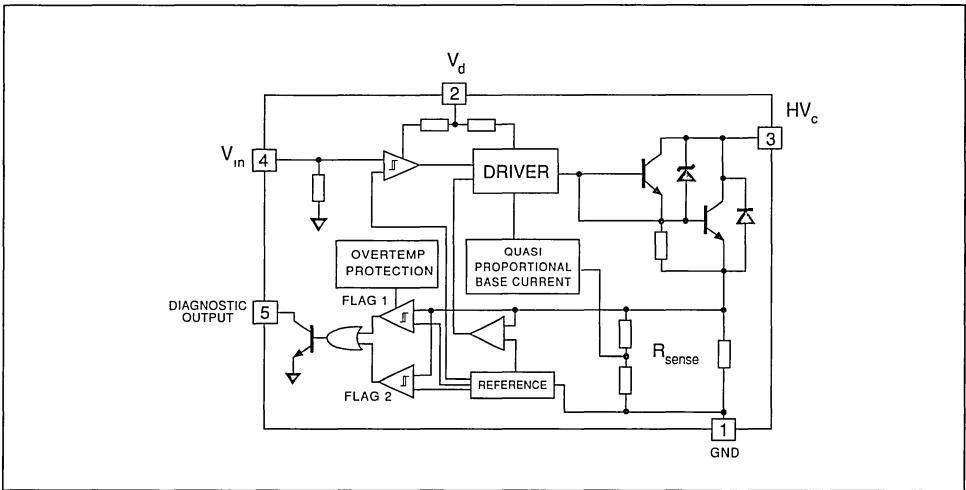
The most common automotive applications of Intelligent Power are ignition systems, where they replace either mechanical systems or discrete IGBTs or bipolar transistors, as transducer drivers, where they replace mechanical relays for switching loads (for example lamps, motors, and solenoids), and in car entertainment systems.

3.1.1 Automotive ignition

Electronic ignition systems replace the conventional mechanical distributor with an electronic switch to provide controlled current to the primary side of the ignition coil transformer, which is switched off at a precisely timed instant to generate a voltage spike across the coil and consequently the ignition spark. This operation is usually under the control of a microprocessor (as part of the Engine Management System) which adjusts the system to obtain maximum efficiency.

This sector is currently dominated by the discrete Darlington bipolar transistor. However, the harsh conditions encountered by the device (voltage spikes, vibration etc), the high power levels involved (500V, 10A, with consequences for the design of protection circuitry) and the common requirement to interface directly with a microprocessor, mean that Intelligent Power devices are becoming increasingly popular. The functional block diagram of a typical device is shown in figure 3.

Figure 3: Functional blocks of an electronic ignition device - the VB027



3.1.2 Transducer Drivers

The modern automotive system typically includes a variety of transducers: for example lamps, window lift motors, electric door locks, fuel injection systems etc. Intelligent power components can be used to form the interface between these electro-mechanical devices and the car control system, providing appropriate control voltages and currents while monitoring for faults, giving safe, reliable system operation.

Their main advantages over mechanical

relays are the ability to drive them directly from logic level signals, their protection and diagnostic facilities, and their reduced size and weight.

3.1.2.1 High side drivers

In an automotive system, a control switch is generally placed between the positive rail and the load, see figure 4.

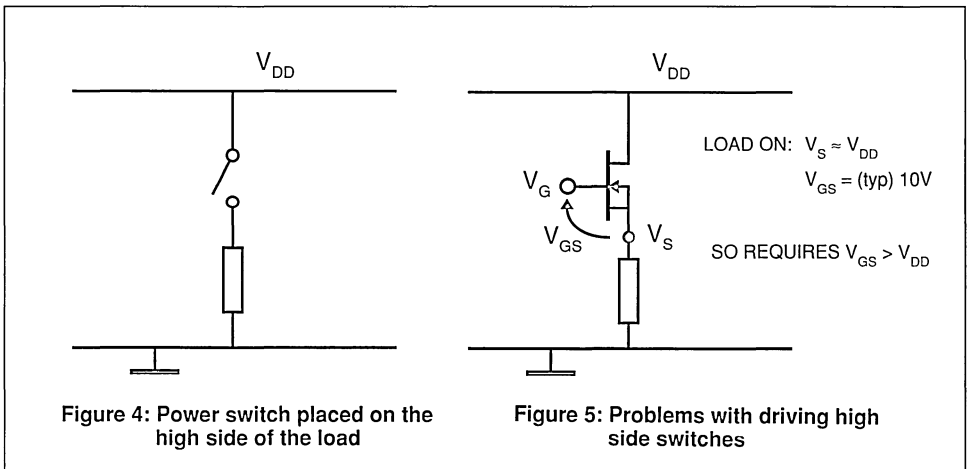
The first reason for this is that because a large area of the car (the body and the chassis) is effectively ground, keeping the

load at a low potential when turned off reduces the risk of a short circuit accidentally turning it on.

The second is that an automotive component is particularly susceptible to electrochemical corrosion, because of the conditions of heat, humidity and salt in which it exists. Because

of this, when the component is turned off (which will be the majority of its lifetime), it is desirable that it should remain at as low an electrical potential as possible.

Figure 5 illustrates the problems incurred by this requirement, using a Power MOSFET switch as an example.



When the switch is turned on, the drain-source voltage falls to approximately zero, and so the source voltage rises to a value close to the level of the positive rail. However, a gate-source voltage of typically 10V for a standard device is needed to keep the switch turned on, and so the gate voltage required is higher than the level of the positive rail. A level shifter is thus needed to drive the device.

Care must also be taken in the design of this drive. As an example, if the source voltage of the switch rises to 12V after turn-on, and a gate-source voltage of 10V is required to keep the device turned on, the gate must be driven with 22V relative to

ground while turned on. However, if this voltage is applied to the device before it is turned on, when the source voltage is close to zero, there is a risk that the gate-source breakdown voltage will be exceeded, and the device will be destroyed. Hence the device must always be driven with a voltage referenced to the source voltage, rather than referenced to ground.

The complexity of the circuits required for this drive, along with the adverse conditions discussed previously, and the increasing need for status feedback, means that Intelligent Power components will in the future replace electromechanical relays in this application.

3.1.3 In-Car Entertainment Systems

The circuits contained within a car stereo or similar system exist in a completely different environment to that of a domestic system. They must function in the presence of a significant amount of electrical interference, and remain reliable despite sustained vibration, but must be squeezed into a very limited space. For these reasons Intelligent Power devices are ideal for these applications.

3.2 Regulators and power supplies

Devices using intelligent power technologies can offer compact circuits with a high degree of efficiency and good protection in power supply and regulation applications.

The efficiency and flexibility of single-chip linear regulation devices can be improved by integrating control circuits onto the chip to implement switch mode techniques, while medium-power power supply systems be fully integrated. Integrated power devices can incorporate for example a half bridge along with all the necessary drive and protection circuits.

Higher power systems can employ devices to drive, monitor and regulate the power switches, for example the PWM controller circuits, and bipolar base or MOSFET gate drivers along with other circuits to form the basis of a switch-mode power supply.

Although most of the components for a high power off-line (that is one powered from rectified AC mains) switch mode power supply can be incorporated onto a single chip, it is not yet commercially practicable to construct a high power off-line supply using intelligent power technology for a number of reasons. The first is that the noise levels generated by the power stage make reliable fault-free operation of the signal stage very difficult to achieve - an ever-present problem in the design of intelligent power devices. The second is due to the fact that a high

power system requires a high degree of device optimisation and quality, and accuracy in all stages of the system. To produce an acceptable yield of multiple high accuracy stages on a single chip at a cost to compete with a discrete solution is a significant technical challenge. Additionally, as the device technologies available to construct each stage of the system are limited by the intelligent power fabrication process, it may be difficult to achieve the required accuracy (for example of a regulation stage) while keeping the area of silicon used small (to keep costs down and reduce the incidence of random defects).

However these problems will be overcome in the future, when the increased system reliability offered by integrated power solutions over their discrete counterparts will make them very attractive.

3.2.1 Battery chargers

Battery chargers represent a special case of power supplies. Simple chargers may just supply the battery with a constant current, but higher performance chargers must carefully monitor and control the charging current throughout the charging cycle to charge the batteries as quickly and efficiently as possible without shortening their lifetime. To supply the battery with the optimal current, and to stop charging before damage occurs, a number of factors must be monitored, most importantly the voltage across the battery (which varies throughout charging cycle, reaching a maximum when the battery is optimally charged but falling when the battery becomes overcharged), and the battery temperature (if this becomes too high due to too large a charging current the battery will be damaged). The charging process is often overseen by a microcontroller, and this along with the complex control circuitry required means that Intelligent Power devices are often used in these applications.

3.3 Motor control and servo drivers

Many motor control applications require a great deal of circuitry to regulate the motor, and in servo applications, monitor and feed back information on the status of the device. Intelligent power is used to improve the compactness of the circuits and reduce system design time. Intelligent power solutions can eliminate bulky PCBs, and can even shrink the electronics enough to be placed actually inside the shaft of the motor.

In servo applications, circuits to monitor the status of position and status sensors, microprocessor feedback circuits, and the power switches to drive the motor can be integrated onto a single chip. Stepper motors are often used in these applications, and the designer can use standard intelligent power devices incorporating all of the circuits required to drive and control the stepper motor (for example the generation of signals in appropriate phases to drive the motor, position control etc) along with the power stage to reduce the complexity of the design and speed up system design time.

In motor control applications, devices range from simple protected transistors to complete bridge drivers with full open- or closed-loop control circuits, monitoring for example the torque delivered by the motor, regulating the current and / or voltage, and providing feedback to a microprocessor controller.

Applications-specific intelligent power devices can integrate all the control and power functions of specialised applications onto a single chip, for example a typewriter controller, incorporating motor drives for carriage positioning, paper feed, and daisy-wheel control, plus a solenoid driver for the hammer and a switch-mode power supply for the typewriter's microprocessor. Again, the integration of all these facilities leads to increased system reliability and reduced

material and assembly costs.

3.4 Audio amplifiers

Intelligent Power audio amplifiers integrate protection circuits along with the transistors for the power amplifier, offering a compact and reliable alternative to discrete solutions.

3.5 Protected Power MOSFETs

Intelligent Power devices exist which under normal circumstances behave exactly as normal Power MOSFETs, and are packaged in the same three pin packages. However, a number of protection features are integrated onto the wafer - over temperature, over current, and voltage clamping. These devices can be used as direct replacements for standard power MOSFETs in any application where there is a requirement for compact, reliable, cost-effective protection.

3.6 Other applications

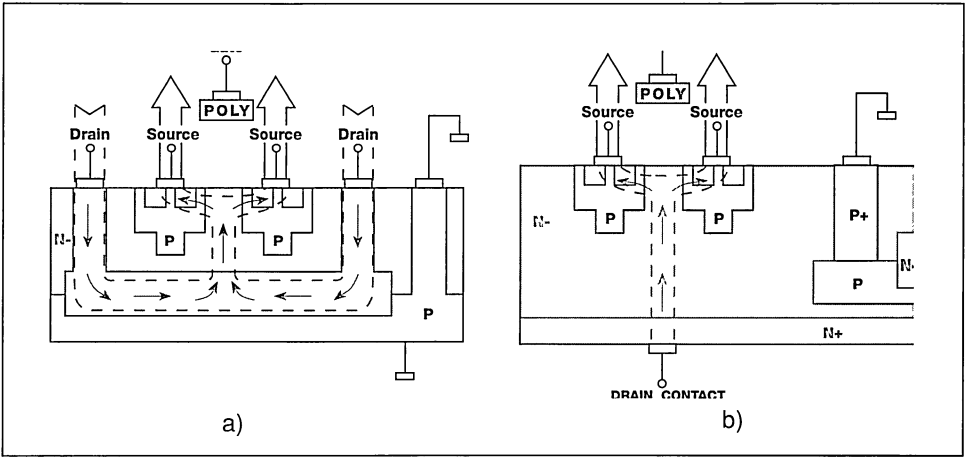
Intelligent power can be used in many other areas using standard or application-specific circuits with special protection requirements or need for compactness. The nature of intelligent power also lends itself to easy design of application specific devices.

Examples are lamp ballast circuits, incorporating drivers for power switches, with starter and oscillator circuits, display drivers, solid state relays, process control high side drivers, telecommunication circuits, and many others.

4. TECHNOLOGIES

Intelligent Power technologies can be split into two basic categories: those which use horizontal power current flow (ie the power current flows parallel to the surface of the silicon wafer), and those which use vertical power current flow - see figure 6. Examples of these technologies are SGS-THOMSON's BCD and VIPower technologies respectively.

Figure 6: Current flows: a) Vertical current flow
b) Horizontal current flow

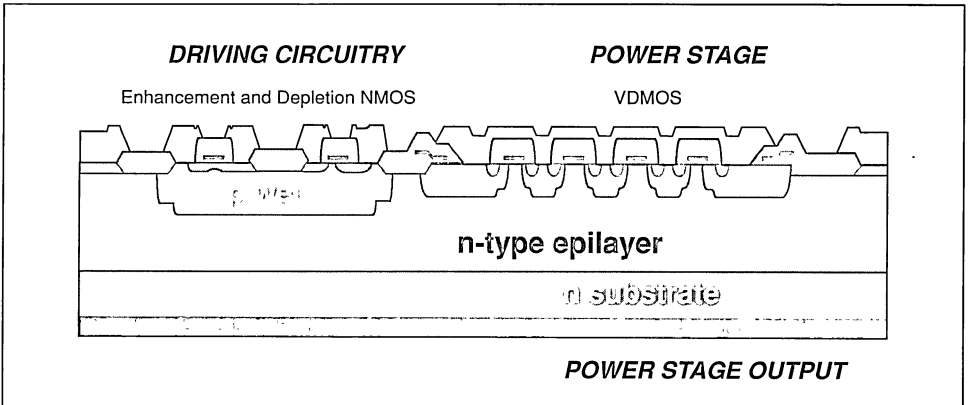


4.1 Vertical technology - VIPower

An example of the basic VIPower structure is shown in figure 7. The signal stage grown in a p-type well to isolate it from the power stage. The current enters the lower surface of the wafer, and flows vertically through the power stage, as it does in a conventional discrete power semiconductor. This means

that they have voltage and current ratings similar or even equal to discrete devices, for example devices are available with Bipolar outputs with blocking voltage ratings of 1200V, and MOSFET devices with output current ratings of 100A.

Figure 7: Basic VIPower structure: VIPower M0 technology



Depending on the particular technology used, the devices employ NMOS, DMOS, CMOS and/or bipolar type transistors for the signal stages, and high voltage bipolar or VDMOS transistors for the outputs.

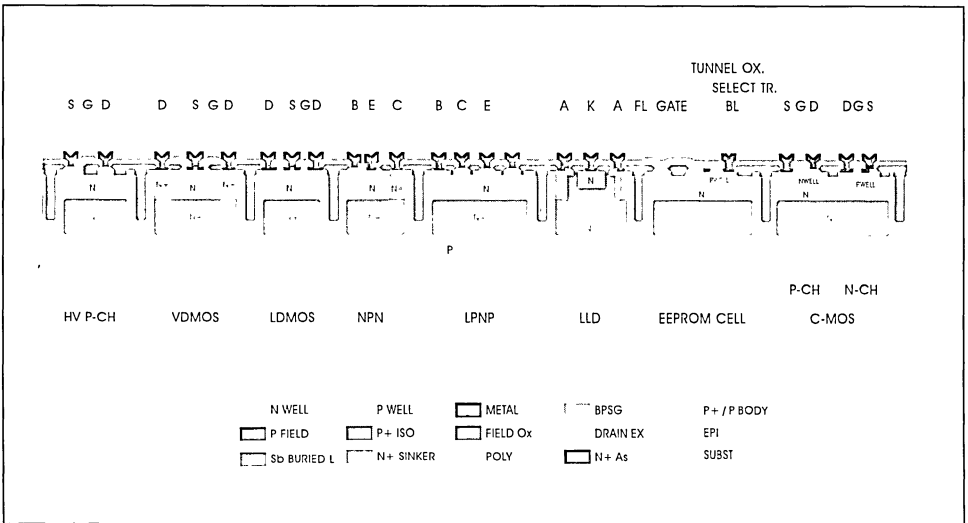
4.2 Horizontal technology - Multipower-BCD

This structure employs the integration of Bipolar, CMOS and DMOS (hence the name) type transistors on the same wafer.

The chip designer is thus able to select the appropriate type of transistor for each part of their design: bipolar for linear functions where high precision is required, CMOS for high density logic and analogue circuits, and DMOS for power stages. The breakdown voltage of this type of device is currently limited to around 250V.

The underlying structure of Multipower-BCD devices is shown in figure 8.

Figure 8: Multipower-BCD structure



4.3 Comparison of vertical and horizontal technologies

Because of the wider conduction path allowed by vertical conduction through the wafer, VIpower gives lower specific conduction resistance and so is able to handle higher power than the BCD approach. However, as the power current flows through the substrate of the device, it is only possible to have multiple power outputs if the power elements of each output have shared collectors/drains (this is possible in some applications, for example high side drivers).

The complexity of the control circuitry that can be integrated onto the chip is also limited because of the chip area occupied by the p-type isolation well.

BCD can be more complex, and can have multiple power outputs, but the use of horizontal current flow results in an $R_{DS(on)}$ per unit area higher than that of vertical technologies, and hence higher costs or higher losses.

These properties mean that as a general rule Multipower-BCD is used to produce complex medium power devices, possibly with multiple power outputs and perhaps a custom or application specific design, while VIPower is suitable for more general devices with greater power handling capability and simpler design. For example VIPower is often used to produce high current car ignition drivers, while a typical Multipower-BCD application may be a computer hard disk drive controller, incorporating a multiple-output motor drive, feedback and a large amount of control circuitry.

4.4 BCD3

The development of BCD3 technology is a further step toward the goal of full integration of power and signal systems. The use of advanced integration technology in these devices allows the construction of an 8 bit microcontroller and supplementary circuitry (for example EEPROM memory) on the same chip as 60V power stages. This opens the door for the production of a whole new generation of highly adaptable and user configurable power devices. Example applications include programmable single-chip power supplies, or families of general purpose very intelligent power drivers.

The incorporation of a microprocessor means that the characteristics of the device can be completely changed at any time, simply by loading the appropriate software into the memory.

5. FUTURE DEVELOPMENTS

The future of intelligent power will see more complexity and more power handling capability, at lower prices. High power single chip switch mode power supplies will be developed, as well as simple 3 pin devices which behave exactly like standard discrete power transistors, but include a comprehensive range of protection features. Mechanical power switches will increasingly be replaced by electronic devices. The distinction between power stages and controllers will become less distinct as more intelligence and logic, microprocessors and microcontrollers, are integrated onto the same chip as high power transistors.

6. CONCLUSION

Intelligent Power bridges the traditional gap between small signal and true power devices. It makes the job of designing reliable, compact power circuits easier. As technology improves, devices becoming more complex, more capable both in terms of the number of control functions and the power they can handle, and the prices are falling. The traditional dividing line between small signal or logic level devices and power devices will become increasingly blurred.

FROM STANDARD TO INTELLIGENT MOSFETS

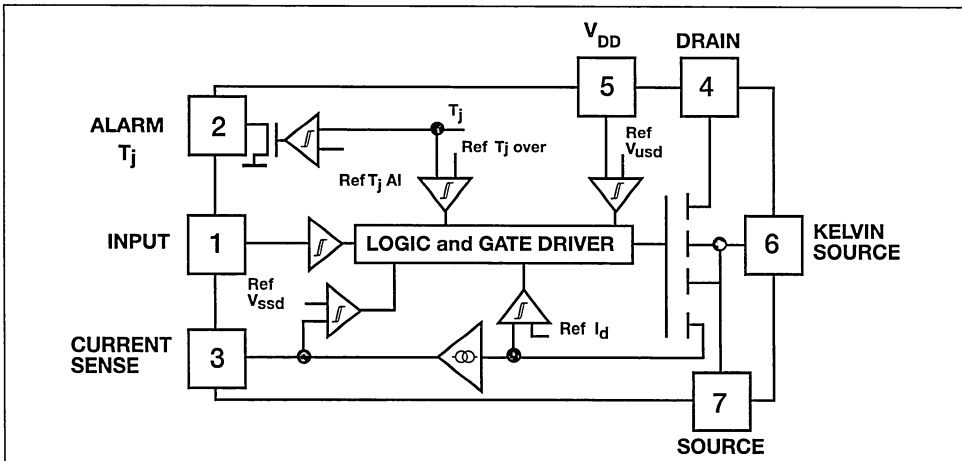
by M. Bildgen

INTRODUCTION

"Smart Power" components are becoming more and more popular in the semiconductor market. These intelligent power switches are today well known in low voltage applications such as automotive switches, stepper motor drives etc. The VN440FI presented in this paper is a

member of a new high voltage smart power family. This 450V, 0.75 Ohm Power MOSFET also includes on the same chip, the driver circuit, over temperature protection, over temperature alarm, current sense, programmable current limitation and short circuit protection (see fig. 1)

Fig. 1 - Block diagram of the VN440FI intelligent MOSFET



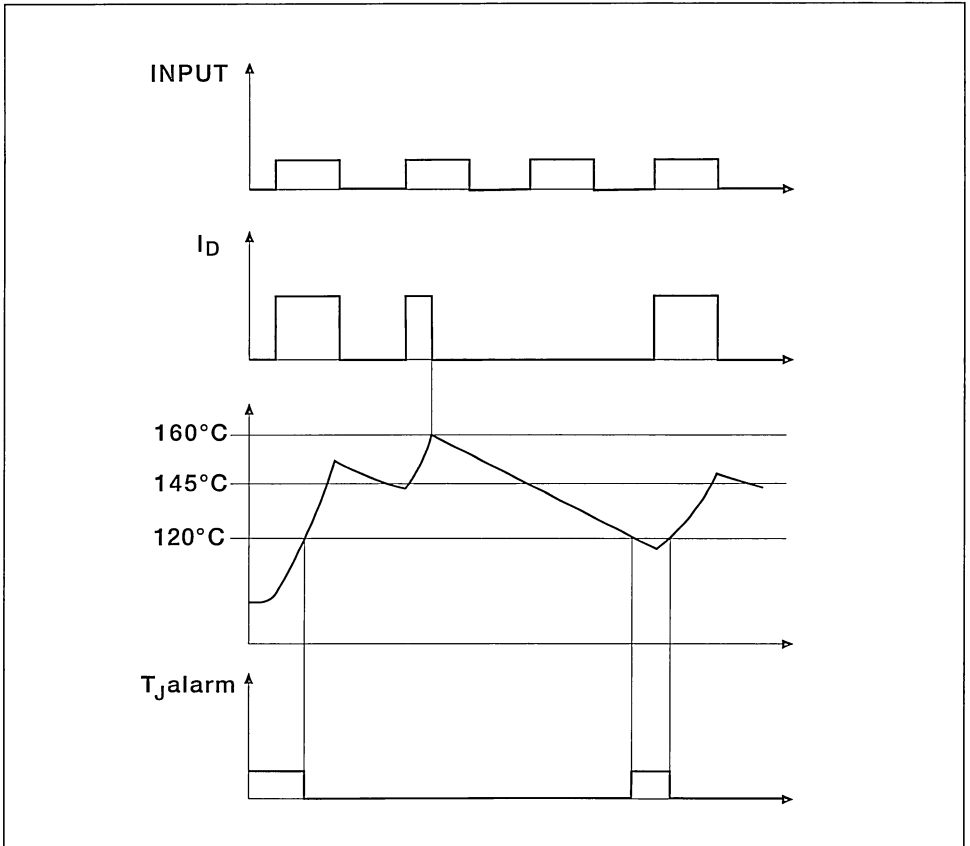
INPUT

The input to the VN440FI is TTL/CMOS logic compatible. The maximum input low level voltage, V_{IL} , is 1V while the minimum input high level voltage, V_{IH} , is 4V with a maximum V_{IH} of 15V. The device can be driven directly by a logic gate or a micro-controller. The interfacing driver between logic and power is integrated in the device. The power MOSFET is always driven under optimal conditions.

OVERTEMPERATURE PROTECTION

The VN440FI has over temperature protection to avoid destruction of the device from excessive dissipation. At a typical junction temperature of 160°C, the Power MOSFET is turned off by the internal logic. When the junction temperature decreases to under a value of typically 145°C, the device can turn on again. As an internal flip-flop is set when the over temperature protection acts, the input has to go to logic "0" before the device can turn on again, see fig. 2.

Fig. 2 - Thermal cycling



When the junction temperature reaches typically 120°C, the T_{JALARM} pin is set to "0". This indicates abnormal operation before thermal shut down of the Power MOSFET. This information can be used to control the system switch-off, saving information before thermal shut down, control lamp, etc.

CURRENT SENSE

A small part of the Power MOSFET cells are not connected to the power source. These cells can be considered as a current source proportional to the drain current. Practically, this information has a very low level and the current image is very noisy during commutation.

A current amplifier with its compensation network is integrated in the VN440FI (see fig. 3).

The information coming from the sense cells is amplified and filtered. The overall ratio between drain and output current of the current amplifier is 1/4000.

In practice, this allows lossless current sensing at pin 3.

Typical rise time of the current amplifier is 3.5V/μs. So, the reverse recovery current of a diode can be ignored because it is filtered (see fig. 4).

CURRENT LIMITATION

The current sense pin is internally connected to the non-inverting input of a comparator. The inverting input is connected to a 3.7V reference. When the voltage across the current sense resistor reaches 3.7V, the Power MOSFET is turned off. The value of the sense resistor determines the limiting current of the devices (see fig. 5).

This function can also be used for current mode control(see fig. 6).

The error voltage adds an offset to the current sense.

The higher the error, the lower the converter current.

SHORT CIRCUIT PROTECTION

The current sense with its associated current amplifier having a limited band width, cannot be used for short circuit protection. The reaction time would be too slow for the high di/dt occurring at short circuit.

Therefore, the short circuit is detected by another, faster current sense that is not amplified. This information is compared to a reference and turns off the device when the short circuit current reaches typically 26A (see fig. 7). This circuit also suffers from a delay time, so that the short circuit current can have much higher values than 26A. The device cannot be destroyed by short circuits.

TURN ON BEHAVIOUR

The di/dt at turn on is limited internally to typical value of 100A/μs, see fig. 8 in order to reduce EMI problems of the equipment.

TURN OFF BEHAVIOUR

When the input goes "low", a small signal MOSFET, T1, with a low on-resistance, discharges the gate of the Power MOSFET. The delay time between input low and desaturation of the Power MOSFET will be very low.

When the beginning of the desaturation is detected internally, T1 is turned off and the gate of the Power MOSFET is now discharged through T2. As T2 has higher on resistance, dV/dt at turn off are controlled (see fig. 8).

When the switching is finished, T1 is turned on again in order to improve the noise immunity.

Fig. 3, 4, 5,

Fig. 3 - Current sense

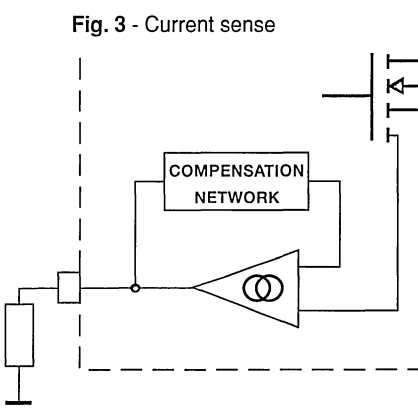
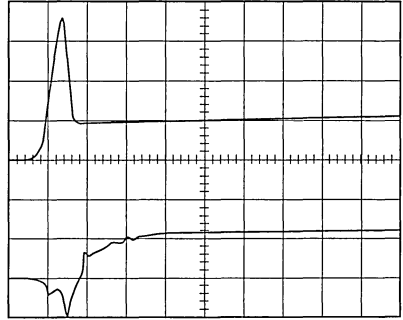
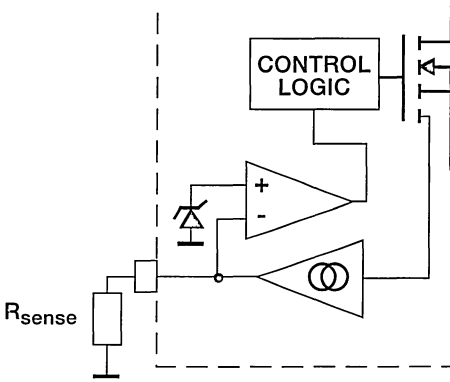


Fig. 4 - Filtered information on current

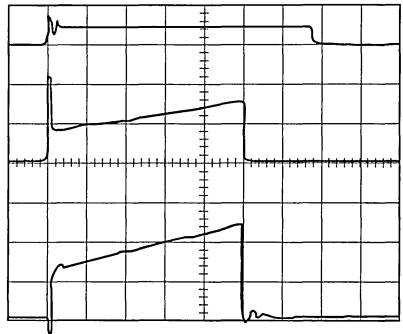


$t = 250\text{ns/DIV}$
 $I_D = 5\text{A/DIV}$
 $V_{\text{sense}} = 2\text{V/DIV}$

Fig. 5 - Internal current limitation



a) Internal circuit



$t = 5\mu\text{s/DIV}$
 $I_D = 10\text{A/DIV}$
 $V_{\text{sense}} = 2\text{V/DIV}$

b) Current limited at 15A

Fig. 6, 7, 8, 9

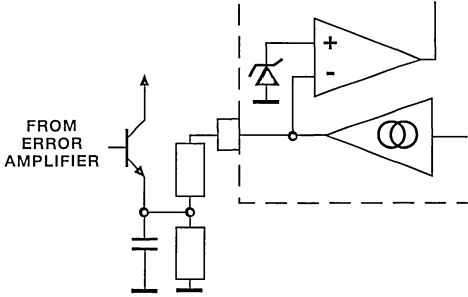
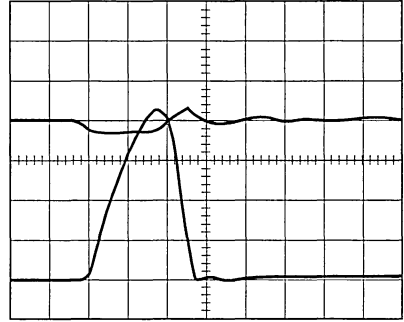
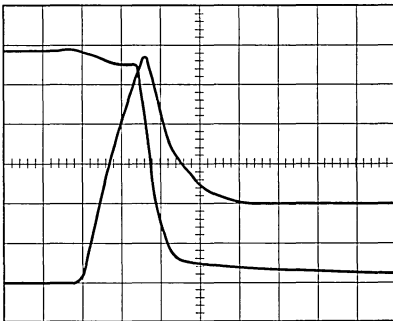


Fig. 6 - Current mode regulation



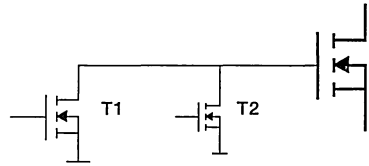
$t = 250\text{ns/DIV}$ $I_D = 20\text{A/DIV}$ $V_{DS} = 100\text{V/DIV}$

Fig. 7 - Short Circuit Protection

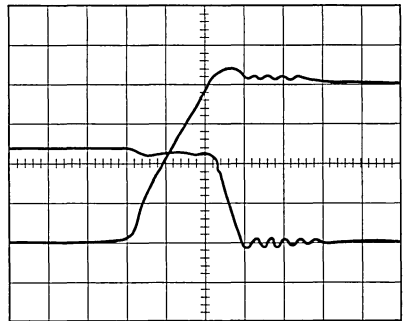


$t = 100\text{ns/DIV}$
 $I_D = 5\text{A/DIV}$
 $V_{DS} = 100\text{V/DIV}$

Fig. 8 - Turn on behaviour



a) Internal circuit



$t = 50\text{ns/DIV}$ $I_D = 2\text{A/DIV}$ $V_{DS} = 100\text{V/DIV}$

b) turn off waveforms

Fig. 9 - Turn off behaviour

INTERNAL BODY DIODE

The internal body diode cannot be used as a free wheeling diode. Due to the technology, current in the anti-parallel diode has to be avoided.

KELVIN SOURCE

The Kelvin source allows proper separation of power ground and signal ground. V_{DD} , the input signal and R_{sense} should be referred to signal source. The signal side of the smart power MOSFET will not be influenced by the power part.

OVERVOLTAGE

The VN440FI does not withstand any over voltages. Over voltages have to be avoided, either by the chosen topology or by external clamping between drain and source.

EXAMPLE CIRCUIT

An example circuit using the VN440FI is shown in figure 10.

The basic circuit is a single switch flyback converter operating in self-oscillating mode. When the switch is turned on, a current flows through the primary side of the transformer. The switch turns off when the current reaches a value defined by the regulation loop (Current Mode Control).

When the switch is turned off, the energy stored in the transformer is transferred to the secondary. The switch remains off until the transformer is completely demagnetized (all the stored energy is transferred to the secondary). The stability obtained in this mode of operation is very good.

Regulation loop

The voltage on the current sense pin is

internally compared to a voltage reference of typically 4.8V. When the voltage on the current sense reaches this value, the Power MOSFET is turned off via an internal logic circuit. The input of the VN440 is not influenced by this internal shutdown.

This feature is used for the regulation loop. An offset depending on the error amplifier is added to V_{SENSE} . The higher this offset, the lower the turnoff current (see figure 6). Another advantage of this regulation mode is the current limitation. Even if the offset voltage on V_{SENSE} is zero, the current on the primary side is limited to a maximum of $I_{prim} * R_{SENSE} + R_{OFFSET} = 4.8V$.

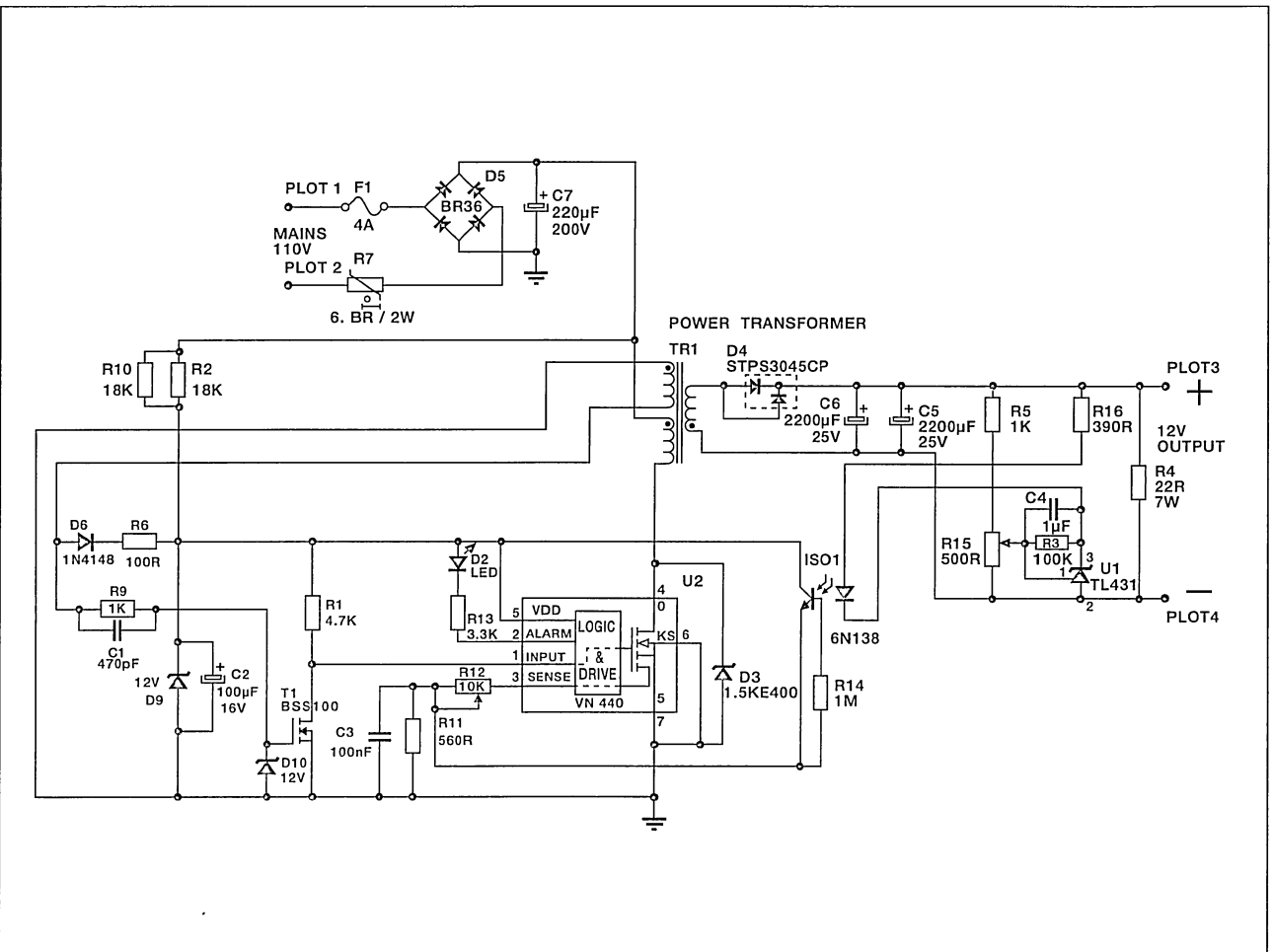
Detection of Demagnetization

The input of the Smart MOSFET must go to a high level when the transformer is completely demagnetized, and this input must be maintained until the regulation loop turns off the device.

As the Smart MOSFET is turned off by the internal shutdown on the internal current sense, the input voltage does not change. The external circuit must set the input to zero in order to reset the internal latches, and this low level must be maintained until the energy stored in the transformer is completely transferred to the secondary. Once the transformer is demagnetized, the gate driver must turn on the gate again.

Figure 10 shows the principle of operation of the gate driver. The VN440 is naturally turned on by applying V_{CC} through R_1 at the input. When the MOSFET is turned off by the internal shutdown on the current sense, the voltage on the power transformer is inverted. T_{GD} turns on and pulls the input of the VN440 to zero. During the transfer of energy to the secondary, T_1 remains on. Once the energy is transferred to the secondary, the transformer voltage goes to zero. T_1 is turned off and the input of the VN440 is set again through R_1 .

Fig. 10 - Self Oscillating Power Supply, 100W / 12V using VN440.



CONCLUSION

The VN440FI is a "standard MOSFET" with on-chip driving interface and protection features.

- * The on-chip protection has a very quick reaction time and allows real, fast protection. This increases the system reliability.
- * As the driving interface and the protection are already integrated, designers can concentrate more fully on the systems approach.

**SEMICONDUCTOR DEVICES
POWER DIODES**

ANALYSIS AND OPTIMISATION OF HIGH FREQUENCY POWER RECTIFICATION

By J.M. PETER

How can the performance of power electronics be improved? Today, in many cases, it is the job of the designer. The fast rectifier switching behaviour depends on the operating conditions. The analysis and the optimisation of these conditions can be an important source of improvement in performance.

1. SWITCH-OFF OF FAST RECOVERY RECTIFIERS

It is possible to define theoretically two types of switch-off¹.

1.1. FREE-WHEEL MODE (figures 1 & 2)

When the rectifier switches-off it is always in parallel with a voltage source. In this case the assumption is that the parasitic inductances are negligible. This type of behaviour can be met in the majority of rectifier applications such as free-wheel rectifiers in step-down and step-up converters, full wave rectifiers, etc... (figure 2). Generally, a rectifier in free-wheel mode is always in parallel with a voltage source when it turns-off.

1.2. RECTIFIER MODE (figures 1 & 3)

An inductance defines the dI_F/dt (decreasing slope of the rectifier current) and when the rectifier switches-off it is always in series with this inductance. This type

of behaviour can be met in some applications such as rectifiers in flyback converters and many functions in thyristor circuits, (figure 3). Generally speaking a rectifier in the rectifier mode is always in series with an inductance L and this inductance L defines the dI_F/dt . The fundamental difference between these two modes is that in the rectifier mode there is a stored energy $1/2LI_{RM}^2$ due to the series inductance. After the turn-off this energy is dissipated in the rectifier and/or in the associated circuits.

1.3. TURN-OFF LOSSES

Free-wheel mode

W_{OFF} is the energy dissipated in the rectifier during turn-off.

$$WFR = \int_{t_1}^{t_2} v_I dt \quad (\text{refer to figure 1})$$

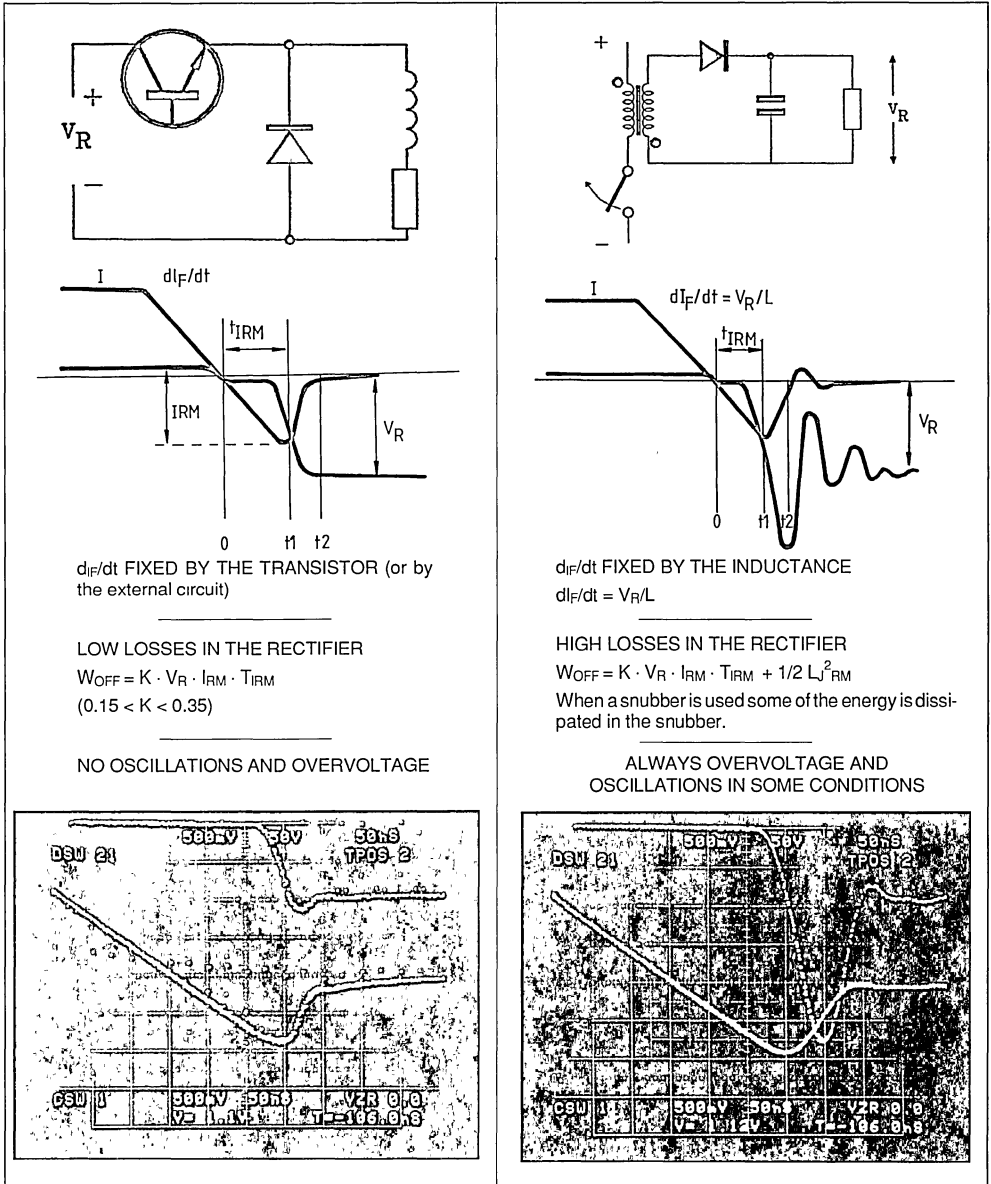
Low voltage (< 200V) fast rectifiers have a high internal capacity and the minority carriers have a very short life time. High voltage fast rectifier have a thicker N silicon layer and the minority carriers have longer life time and consequently different behaviour during the turn-off condition blocking state. (Higher I_{RM} and t_{IRM} - more damping).

APPLICATION NOTE

Figure 1 : Fast Rectifier : the two turn-off modes.

a) Free-wheel Mode.

b) Rectifier Mode.



5A/div. 50V/div. 0.05μs/div.
 BYT30 - 1000 - I_F = 3A - dI_F/dt = - 75A/μs - V_R = 100V - T_{CASE} = 25°C

According to the experimental results the turn-off energy loss $(W)_{FR}$ in the free-wheel mode can be written :

$$(W)_{FR} = K \times V_R \times I_{RM} \times t_{IRM} \quad (1)$$

Max Voltage Rating (V)	200	400	800	1000	1200
K	0.12	0.14	0.22	0.28	0.35

Rectifier mode

Losses in this mode, $(W)_{REC}$, are the sum of the stored energy $1/2 L I_{RM}^2$ and the recovery energy $(W)_{FR}$:

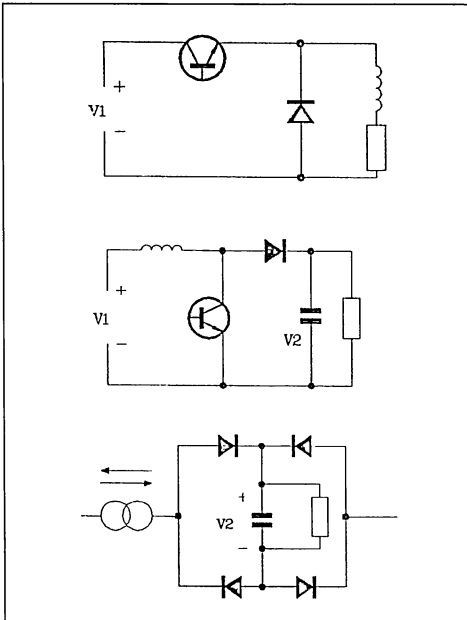
$$(W)_{REC} = (W)_{FR} + 1/2 L I_{RM}^2 \quad (2)$$

In some cases, oscillations can occur. This depends on the damping due to the current tail effect after switch-off. When oscillations occur energy is dissipated during the oscillations partly in the rectifier and partly in the circuit. When snubbers are used a significant part of the energy is dissipated in the snubber.

2. PRACTICAL SWITCH-OFF BEHAVIOUR

The two cases, free-wheel mode and rectifier mode are simplified cases that are easy to simulate in a laboratory characterisation. In practical equipment there is always a possible overlap between the two theoretical modes, because :

Figure 2 : Rectifiers in Free Wheel Mode.



$K^{(1)}$ is a constant that depends on the thickness of the N type silicon layer.

1. No circuit is without parasitic inductances.
2. The rise time (or the fall time) of the switch is not infinitely fast when compared with the rate of change of current, di/dt .

Experimental results show that in all cases the following formula can be used :

$$(W)_{OFF} = (W)_{FR} + 1/2 L_S I_{RM}^2 \quad (3)$$

Where L_S = series inductance

This important relationship is a useful tool for the designer, giving him the main parameters that influence the turn-off energy.

N.B. : The following relationship (4) is only true for the pure rectifier mode.

$$(W)_{OFF} = Q_R \times V_R \quad (4)$$

Where Q_R = recovered charge

(1) K is experimental - Defined for SGS-THOMSON Microelectronics fast rectifiers.

Figure 3 : Rectifiers in Rectifier Mode.

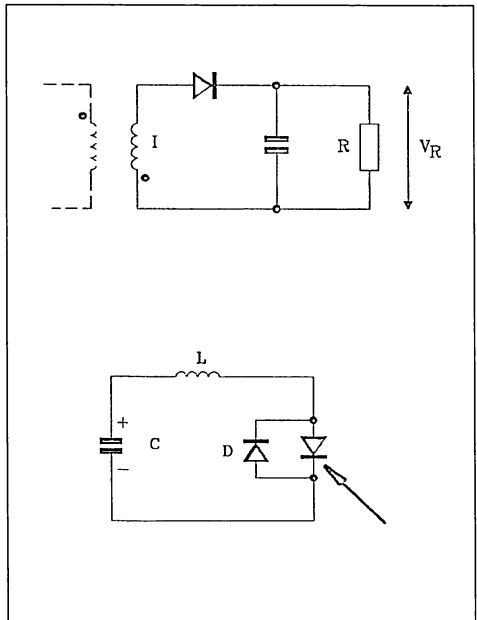


Figure 4 : Switch-off Behaviour of the Ultrafast BYT12-400V Rectifier (current rating 12A - voltage rating 400V).

Conditions : $I_F = 13A$ $di_F/dt = -150A/\mu s$ $V_R = 100V$ $T_{case} = 25^\circ C$.

In the case of rectifier mode : $L = 0,6\mu H$.

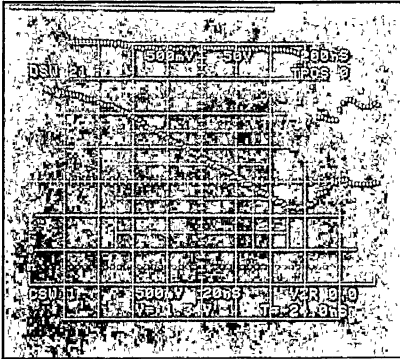
The turn-off lost energy calculated by the current and voltage is :

$(W)_{FR} = 3\mu J$ free-wheel mode.

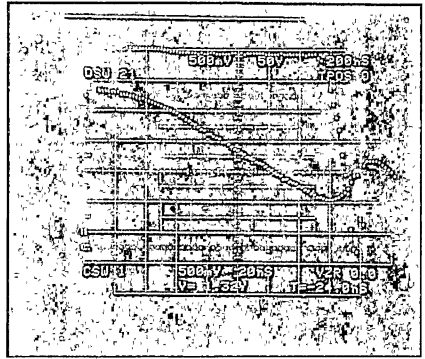
$(W)_{REC} = 10\mu J$ rectifier mode.

The storage energy in the inductance is : $1/2 L I_{RM}^2 = 7.5\mu J$.

a) Free wheel mode.



b) Rectifier mode.



The use of this equation for a lot of practical circuits can be considered as a first approximation. It leads to over estimated losses, if the rectifier does not operate in pure "rectifier mode".

a trade off between :

- Speed (I_{RM})
- Max voltage rating (V_{RRM})
- Forward voltage drop (V_F).

Example : 12A fast rectifiers.

3. CHARACTERISTICS OF FAST RECTIFIERS

The characteristics of fast rectifiers are the result of

V_{RRM}	200	400	800	1000
Type	BYW81	BYT12-400	BYT12-800	BYT12-1000
$T_j = 100^\circ C$				
$I_{RM}(A)$	1.8	3.7	6	7.8
$di_F/dt = -50A/\mu s$				
$t_{IRM}(\mu s)$	0.05	0.075	0.160	0.200
V_F				
(V)	$0.66 + 0.0071$	$11 + 0.021$	$1.3 + 0.031$	$1.3 + 0.031$

Operating conditions

I_{RM} increases with di_F/dt (figure 5).

I_{RM} increases with T_j (figure 6).

The important points that emerge are :

1. High voltage fast rectifiers are not so fast as low voltage fast rectifiers, (comparing devices of equal current rating).
2. T_j and di_F/dt have a strong influence on the reverse recovery current.

4. EXAMPLES

4.1. FLYBACK CONVERTER (figure 7)

The behaviour is as a pure rectifier ; the rectifier is driven by a current source, the inductor, L.

For a frequency less than 100kHz the switching losses are small in comparison to the conduction losses, because di_F/dt defined by V_o/L is always small, (see table figure 7).

Figure 5 : Switch-off Behaviour of the Fast Rectifier BYT12P 1000 (current rating 12A voltage rating 1000V). Influence of the di/dt .

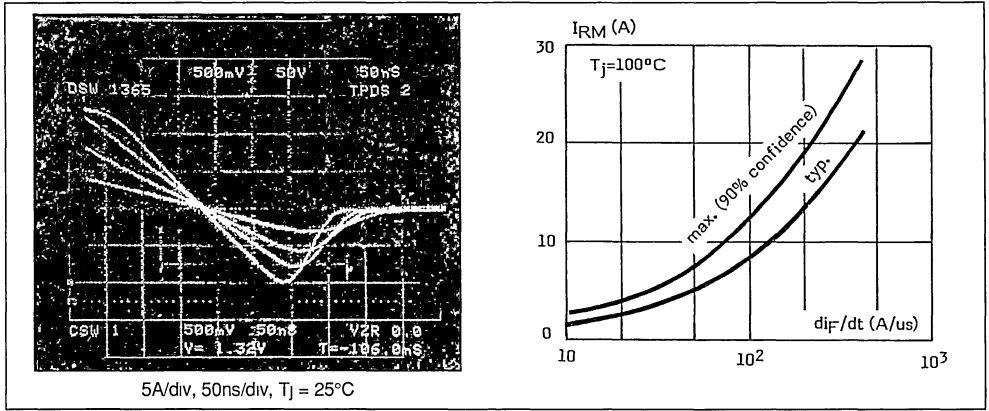
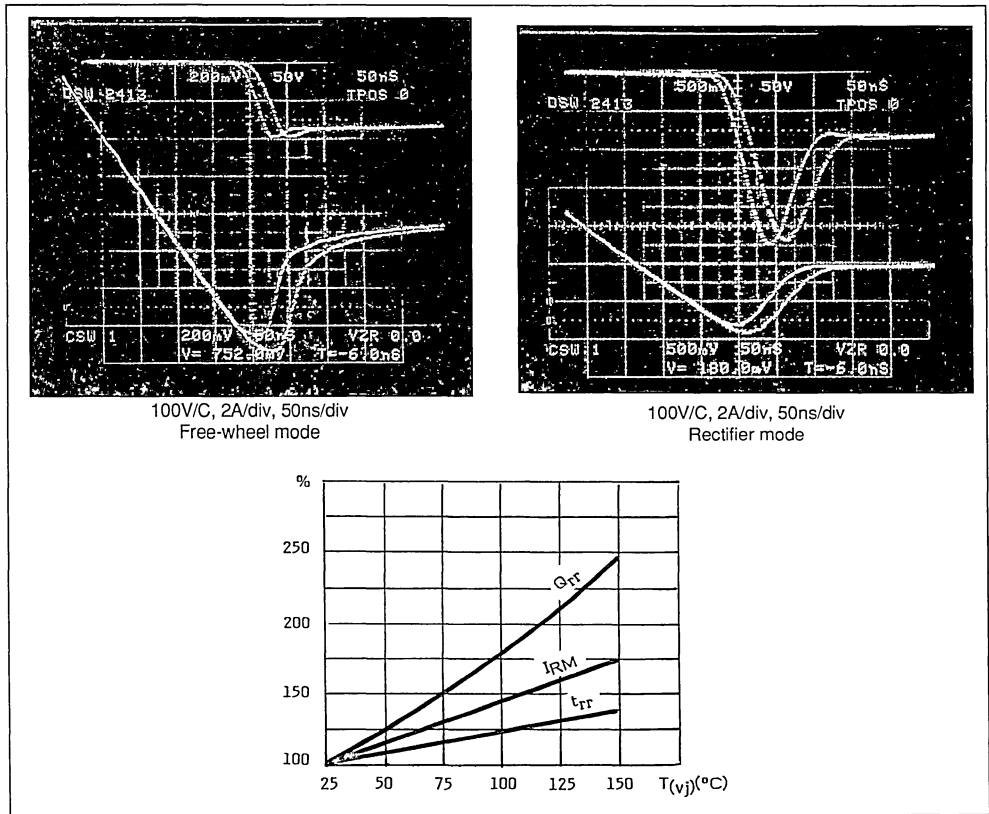


Figure 6 : Switch-off Behaviour of the Fast Rectifier BYT12 1000 Influence of T_j . One Curve $T_j = 25^\circ$, one curve $T_j = 60^\circ$.



APPLICATION NOTE

How can the designer reduce the losses ?

1. The ratio I_{peak}/I_{AVG} , is very unfavourable in this type of circuit. It is essential when the peak voltage is less than 200V that the "high efficiency ultra fast" family which have very low conduction losses are used. When the peak voltage is greater than 200V one solution is to use a rectifier with higher current rating.

Example :

In the same circuit at 12A with :

- BYT12-800 : conduction losses = 7.6W, a 12A rectifier.
- BYT30-800 : conduction losses = 6W, a 30A rectifier

2. Reduce the junction temperature. If T_j is decreased from 100 to 75°C the switching losses are reduced by 20%.

4.2. SMALL CURRENT RECTIFIER (figure 8)

A transformer with a leakage inductance measured on the secondary side $L_S = 1\mu H$ supplies a fast diode D. The average output current is 0.8A and the output voltage is 48V.

The designer wants to use the popular diode BA157. This is not possible because the total power dissipation is 1.15W at 40kHz. At this frequency he can only use a popular 2A current rated diode (for 0.8A rectified current) and at 200kHz there is no solution with popular diodes (see table in figure 8).

How can the designer reduce the losses ?

1. Choose a diode in the "high efficiency family". For example he can use the BYW100 for 40kHz to 200kHz, (see table figure 8).
2. Reduce the leakage inductance : with a leakage inductance $L_S = 0.1\mu H$, BY218 at 200kHz ($1.24W$, $\Delta T_j = 93^\circ C$).

4.3. FULL WAVE OUTPUT RECTIFIER

There are two different full wave rectifying circuits.

4.3.1. VOLTAGE SOURCE - CURRENT OUTPUT

Current and voltage behaviour are indicated in figure 9. The inductance L_S is the leakage inductance of the insulation transformer.

The 4 rectifiers operate in an intermediate mode between "free wheel" and "rectifier", because there are some $1/2 L_S I_{RM}^2$ losses.

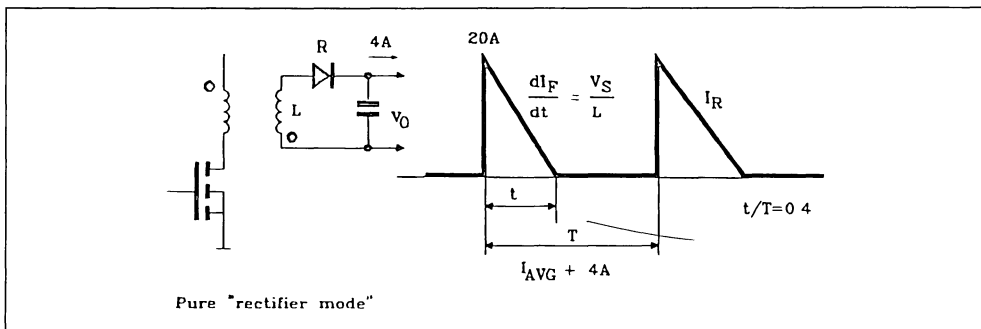
4.3.2. CURRENT SOURCE - VOLTAGE OUTPUT (figure 10).

In this circuit, each rectifier operates in "free wheel" mode. The series inductance does not introduce additional losses. (This assumes there is no parasitic inductance between the rectifiers and the capacitor C).

How can the designer reduce the losses ?

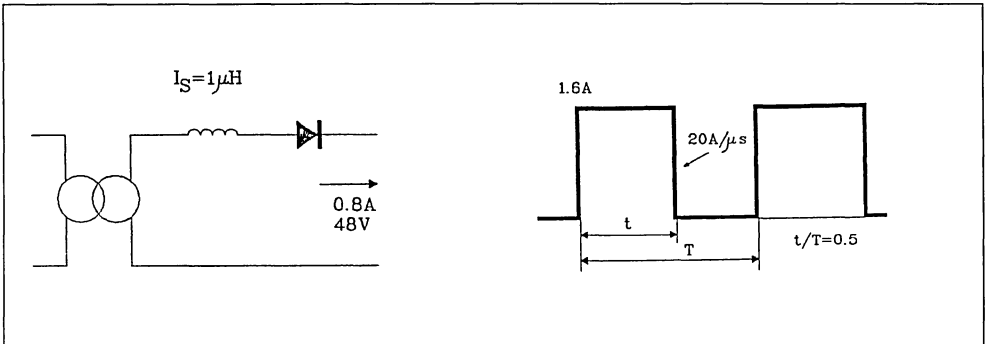
Figure 7 : Flyback Rectifier Output Average Current 4A.

Below 100kHz the switching losses are negligible, in comparison with the conduction losses. The reason is limited dI_F/dt , consequently limited I_{RM} .



V_O (V)	12	48	100
Rectifier	BYW81-100 "High Efficiency"	BYT12-400	BYT12-800
Conduction Losses (W)	3.2	6	7.6
Switching Losses a 50kHz (W)	0.006	0.05	0.81
Switching Losses a 200kHz (W)	0.05	0.5	5.5

Figure 8 : The Popular Diodes BA157 – BY218 are not Fast Enough for High Frequency Rectifying. The BYW100 is well adapted.



DIODE	BA157 Popular	BY218 Popular	BYW100-200 High Efficiency
I_{RM} a 100°C $di/dt = -20A/\mu s$ (A)	2.8	2.8	0.75
t_{IRM} a 100°C $di/dt = -20A/\mu s$ (A)	0.14	0.14	0.05
$(W)_{FR}$ (μJ)	2.08	2.08	0.01
$1/2 L_S I_{RM}^2$ (μJ)	3.9	3.9	0.28
Conduction Losses (W)	0.944	0.744	0.592
Switching Losses a 40kHz (W)	0.2	0.2	0.012
Switching Losses a 200kHz (W)	1.3	1.3	0.06
Total Diode Losses a 40kHz (W)	1.15	0.44	0.6
ΔT_j a 40kHz (°C)	115°	71°	60°
Total Diode Losses a 200kHz (W)	1.97	1.77	0.65
ΔT_j a 200kHz (°C)	197°	132°	65°

- a) Voltage source - current output .
 Reduce the transformer leakage inductance. Table of figure 11 shows that in the case of the 400V 10A 200kHz bridge circuit the suppression of the inductance L_S can save $4 \times 16.5W = 66W$. Replace in the same circuit the high voltage fast rectifier BYT12-600 by 3 "high efficiency" BYW81-200 in series (see figure 12 - table). The total losses decrease from 186W to 58W. This result is very important as it shows it is more efficient to use several "high efficiency" ultra fast rectifiers instead of a single high voltage one for high frequency operation.
- b) Both

Use of sinusoidal current (resonant converter) instead of rectangular waveforms. Figure 11 shows that for the same conditions (400V - 10A - 200kHz) the switching losses with a sinusoidal current are only $4 \times 7.5 = 30W$ ($4 \times 22 = 88W$ with rectangular wave forms).

4.4. STEP UP CONVERTER

The rectifier operates in free wheel mode. The main losses in this case occur in the transistor during the

turn-on (similar to the step down converter). Figure 13 shows that with 600V output at 40kHz, if the rectifier switching losses are reasonable, the transistor turn-on losses are too high.

How can the designer reduce these turn-on losses ? (fig. 13).

- a) Decrease the rectifier junction temperature by more efficient cooling.
 If the BYT12-800 junction temperature decreases from 100 to 70°C, the transistor turn-on losses decrease from 39.5W to 33W.
- b) To replace one BYT12-800 by 4 high efficiency BYW81-200 in series. The total balance is a reduction in losses from 39.5 to 16.6W in the transistor with same losses in the rectifier.

IN SUMMARY

Two major actions reduce switching losses caused by fast recovery rectifiers :

1. APPROPRIATE CHOICE OF COMPONENT
 - The fastest rectifier compatible with the peak voltage in the application.

APPLICATION NOTE

- If the peak voltage V_R exceeds 400V the designer must analyse carefully the switching losses :
 - These losses are proportional to $I_{RM}^2 \times V_R$.
- A 800V fast rectifier has an I_{RM} approximately two times higher than a 400V fast rectifier (same current rating).

Figure 9 : Voltage Source, Output Current Full Bridge Circuit.

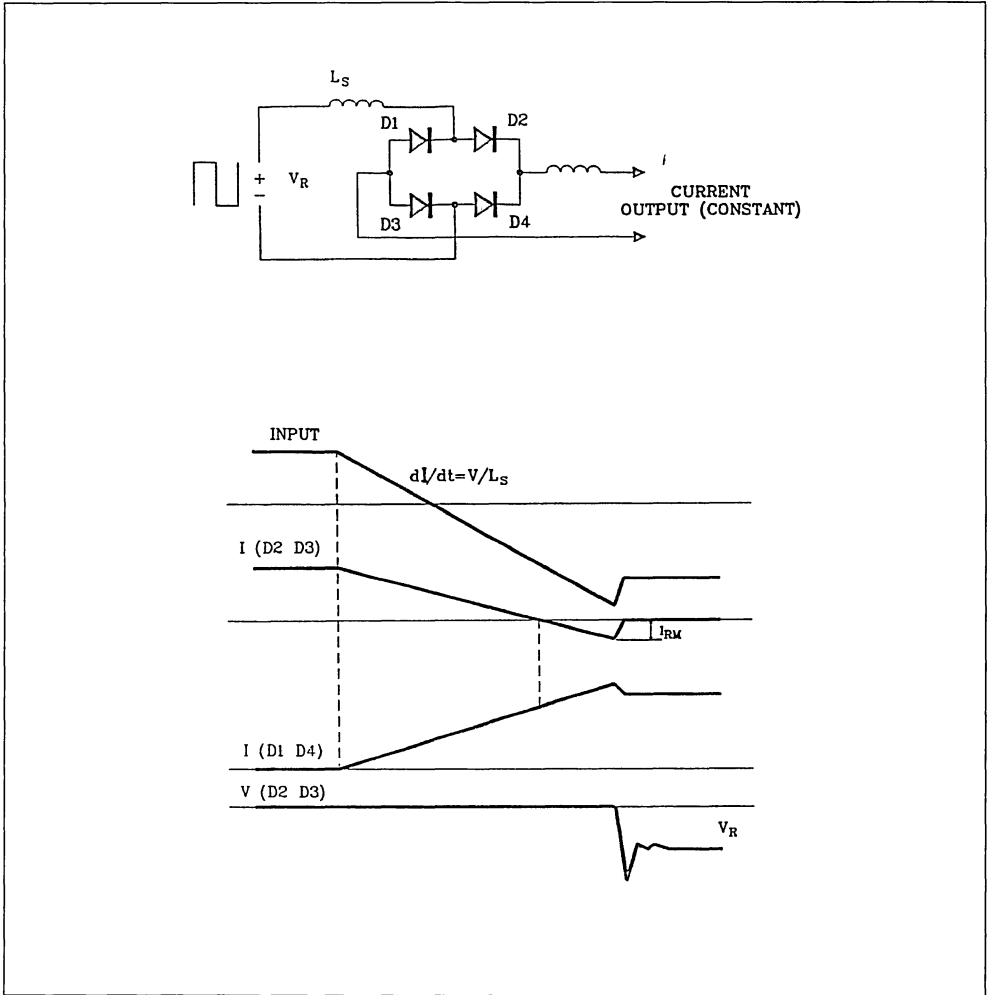
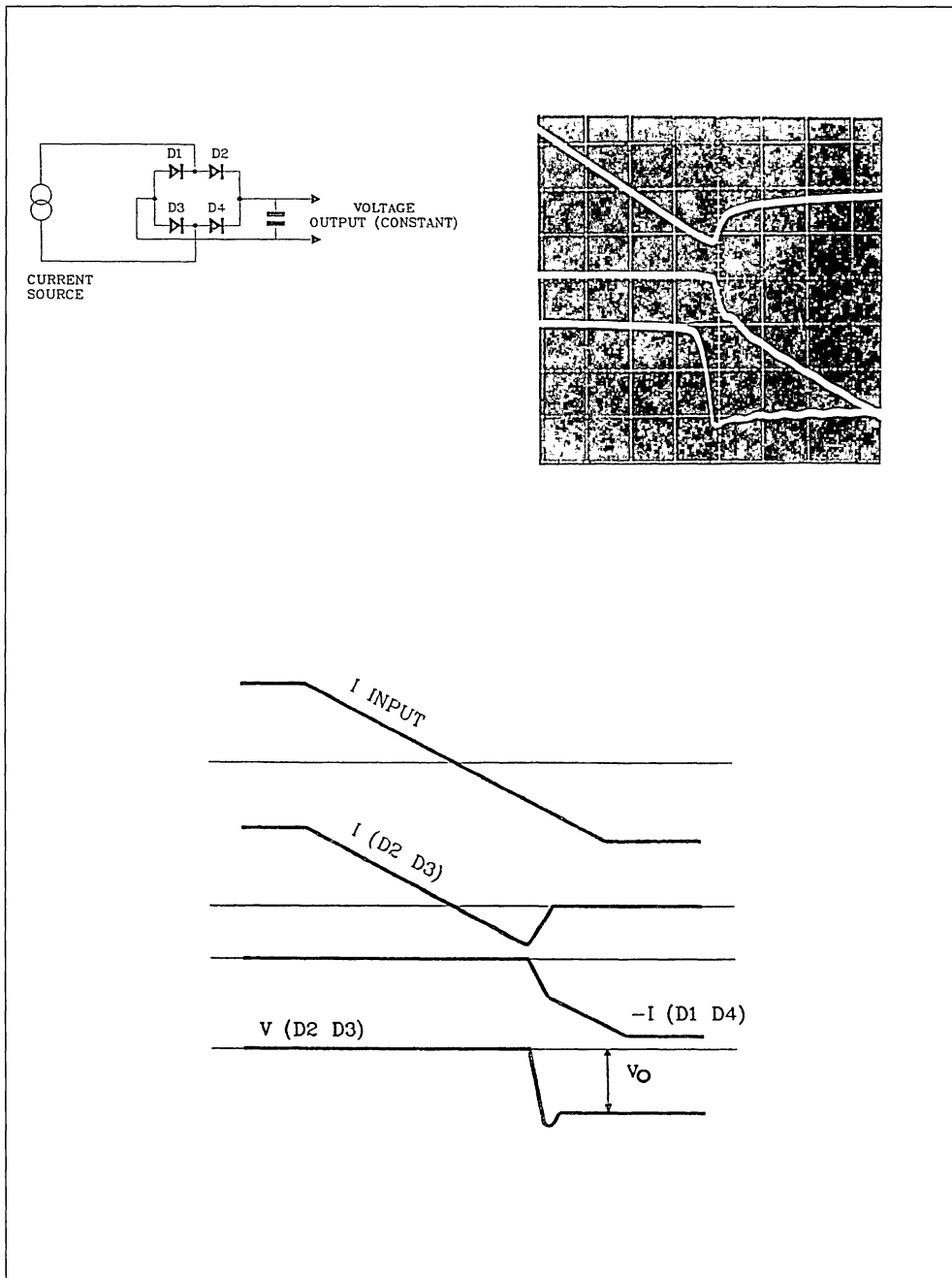


Figure 10 : Current Source, Output Voltage Full Bridge Circuit.



APPLICATION NOTE

Figure 11 : Switching Losses (per leg) in a full Wave 200kHz Bridge Circuit. Output 10A.

In case of voltage source, current output, the (leakage) inductance L_S introduces $L_S I_{RM}^2$ losses.

In case D, the losses are smaller ($6 \times 4 = 24W$ instead of $22 \times 4 = 88W$) because dI/dt is smaller, consequently I_{RM} is smaller.

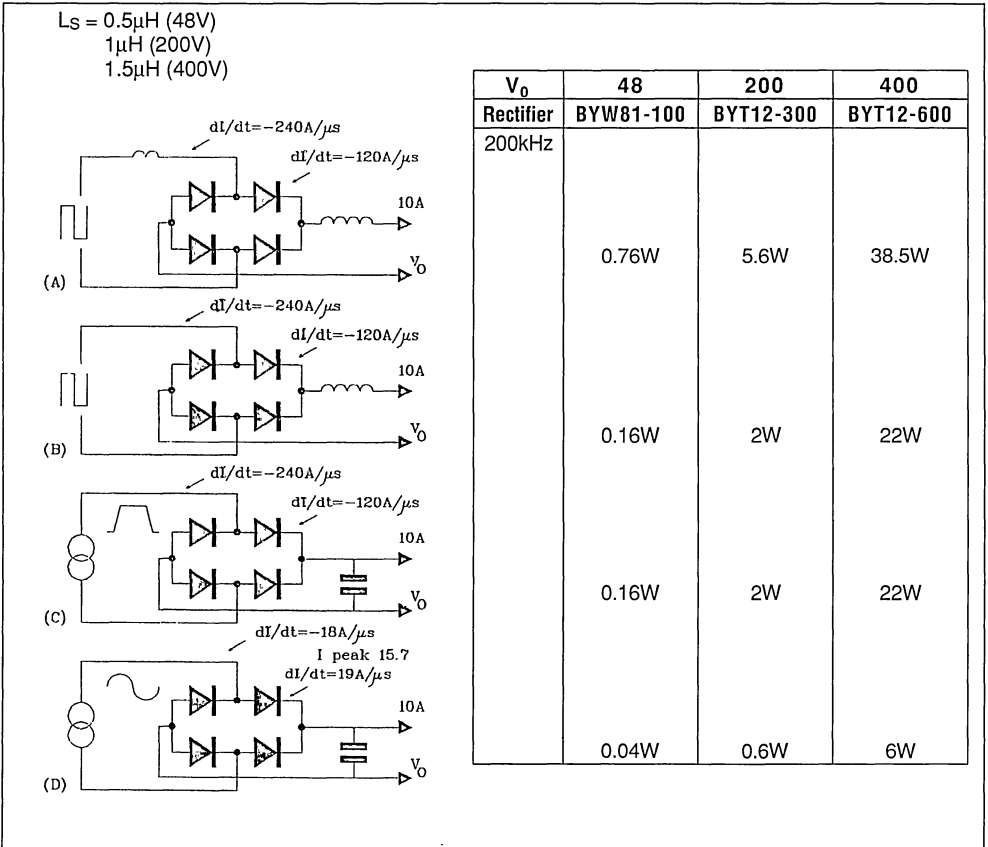


Figure 12 : Switching Losses (per leg) in the Full Wave 400V 200kHz Bridge Circuit with two Different "rectifiers".

Replacing the high voltage BYT12 – 600 rectifier by 3 "high efficiency" ultra fast BYW81 – 200 in series reduces the total losses dramatically. This is why the I_{RM} from BYW81 is very low and the voltage drop of this high efficiency rectifier is very low.

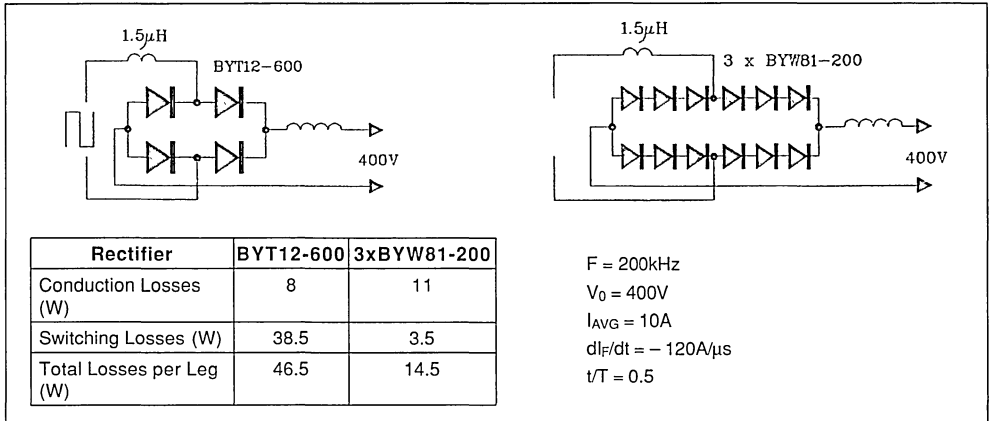


Figure 13 : In the Step-up (or step down) Converter the Majority of Losses Occur in the Transistor, Specially when a High Voltage Rectifier is used. In some case replacing a high voltage rectifier by several faster rectifiers in series (and consequently with a lower voltage rating) can minimize the total losses despite the increase of the rectifier conduction losses.

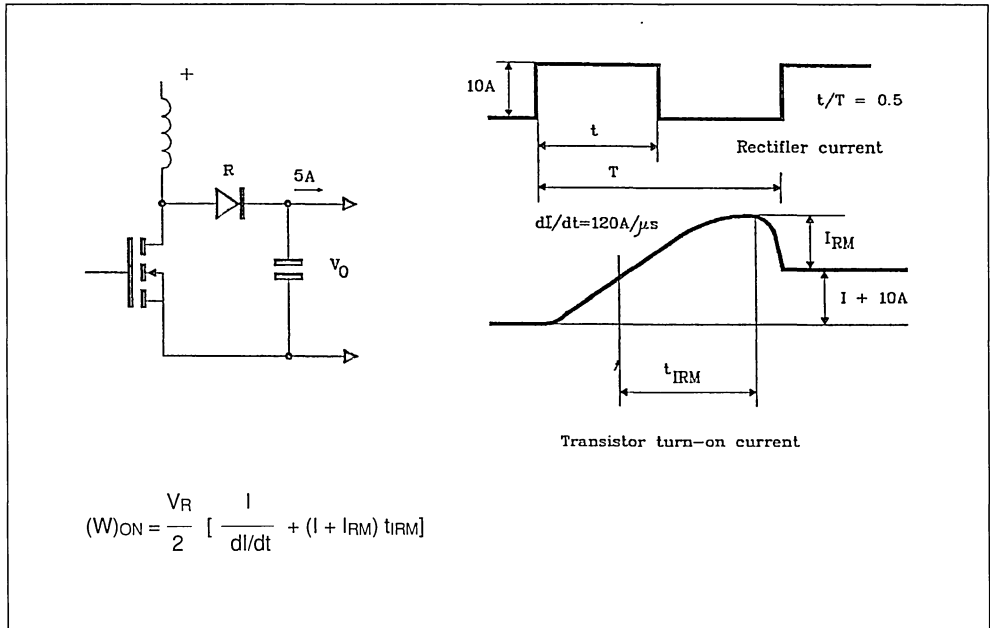


Figure 13 (continued).

V ₀	48	300	600	600
Rectifier	BYW81-100	BYT12-400	BYT12-800	4 x BYT81-200
(di/dt = 120A/μs) I _{RM} (A)	3.8	6	10.5	3.8
(T _J = 100°) t _{IRM} (μs)	0.04	0.06	0.12	
Rectifier Conduction Losses (W)	3.65	6.5	8	14.6
Rectifier Switching Losses a 40kHz (W)	0.04	0.6	6.7	0.5
Total Rectifier Losses a 40kHz (W)	3.7	7.1	14.7	15.1
Transistor Turn-on Losses a 40kHz (W)	1.32	1	0.7	39.5

The rectifier voltage drop increases with the rating voltage.

Example : BYW81 "high efficiency" 200V rating V_F = 0.85V (max).

BYT12-600 600V rating V_F = 1.8 (max).

IMPORTANT CONSEQUENCES :

If the switching frequency is greater than 40kHz in many cases it will be more efficient to replace one high voltage (600 - 800 - 1000V) rectifier by a series of ultrafast rectifiers (200V or 400V). Despite the increase of conduction losses, a dramatic reduction of switching losses results in a decrease in the total losses.

2. OPTIMAL OPERATING CONDITIONS

2.1. In many cases parasitic inductance gives additional losses. A reduction of those parasitic inductances L_S decreases not only the voltage spikes but also the switching losses.

2.2. Junction temperature plays an important rôle. The switching losses are approximately proportional to T_J. Improving the rectifier cooling is very important for all high frequency rectifiers.

2.3. For full wave rectifying circuits, with an isolation transformer the switching losses are always lower in case of :

Current source → rectifying → voltage source
than :

Voltage source → rectifying → current source

because the impedance due to the transformer leakage inductance is integrated in the current source, and does not play any part in the additional losses. 2.4. The use of the resonant circuit with sinusoidal current waveforms results in a significant reduction in the switching losses due to the limited di/dt or to the smaller V_{RI} re-applied voltage.

CONCLUSION

Reducing the switching losses in high frequency converters is team work.

The manufacturer has improved the fast recovery rectifier characteristics. The designer has now some tools to analyse, with a greater accuracy, the rectifier behaviour and choose the optimal solution in order to minimize the losses.

REFERENCE

[1] "Switching behaviour of fast diodes in the converter circuits" - p.63 to 78 in the hand book SGS-THOMSON Microelectronics "Transistors & Diodes in Power Processing".

THE CONDUCTION LOSSES IN A POWER RECTIFIER

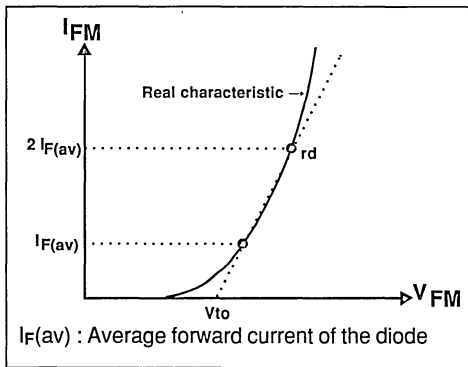
B. Rivet

INTRODUCTION

In spite of the high operating frequency, the conduction losses remain the main cause of the junction's temperature increase in the majority of the applications. Therefore, it is important to accurately estimate these losses. The purpose of this note is to give data to calculate the conduction losses in the diodes.

The forward characteristic of a diode is shown in fig.1

Fig.1 : Forward characteristics of a diodes



We can define two areas :

1) The peak current I_M is lower than $3 I_{F(av)}$:

The forward characteristic of a diode may be assimilated to a straight line defined by V_{to} and r_d (Fig.1).

The forward voltage can be expressed by

$$V_{FM} = V_{to} + r_d I_{FM}$$

V_{to} and r_d are given in the datasheet for each part number. With this model the expression of the conduction losses is :

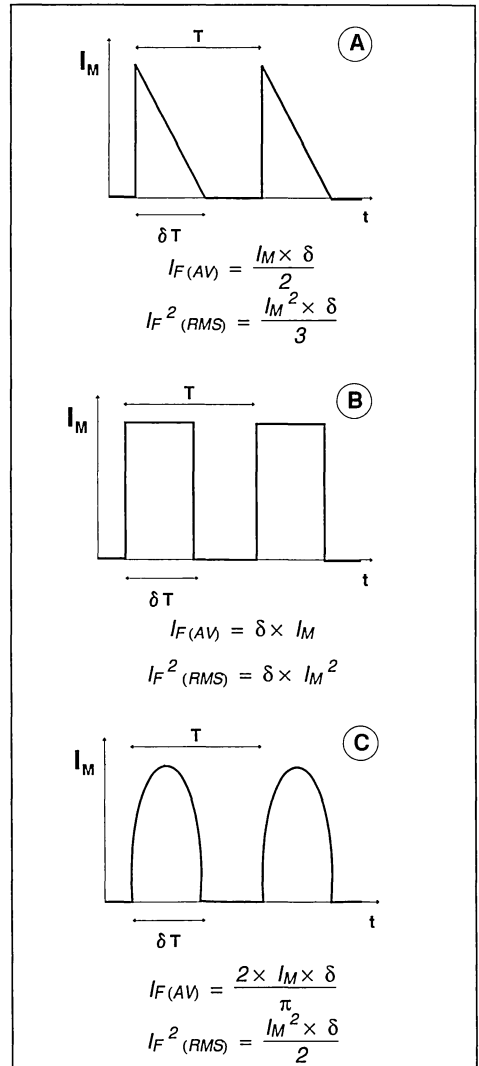
$$P_{cond} = V_{to} I_{F(av)} + r_d I_{F(RMS)}^2$$

$I_{F(av)}$: average forward current in the diode

$I_{F(RMS)}$: RMS forward current in the diode

Fig.2 shows the average and RMS values for different current wave forms.

Fig.2 : Average and RMS values for different currents wave forms.



APPLICATION NOTE

Example :

With a STTA1206D : $V_{to} = 1.15V$ $r_d = 0.029 \text{ Ohm}$
and a rectangular current : $I_M = 20A$ $\delta = 0.5$
we find :

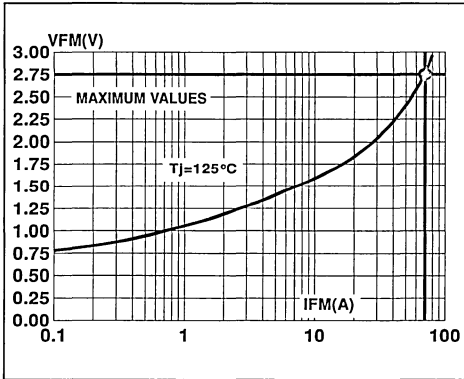
$$P_{cond} = 17.3W$$

2) The peak current I_M is higher than $3 I_{F(av)}$:

When the peak current I_M is higher than $3 I_{F(av)}$, the forward voltage and the conduction losses values calculated with V_{to} and r_d becomes very pessimistic (Fig.1).

A more accurate estimation of the conduction losses can be done with the curve V_{FM} , I_{FM} given in the datasheet (fig.3).

Fig.3 : Forward voltage drop versus forward current of a STTA806D.



In the case of a rectangular current conduction losses can be expressed by :

$$P_{cond} = V_{FM}(I_M) \times I_{F(av)}$$

Where $V_F(I_M)$ is the V_{FM} value when $I_{FM} = I_M$

Example :

With a rectangular current : $I_M = 70A$ $\delta = 0.1$

and a STTA806D $V_{FM}(70A) = 2.75V$ (Fig.3)

$P_{cond} = V_{FM}(70A) \times \delta \times I_M$

we find :

$$P_{cond} = 19W$$

In these conditions, conduction losses calculated with V_{to} and r_d give : $P_{cond} = 29W$!

Conclusion

This short note provides the designer with the rules to properly estimate the conduction losses in a power diode. It also highlights the limitation of the traditional forward characteristic model $V_F = V_{to} + r_d I_F$, gives a value very pessimistic at high level current.

SERIES OPERATION OF FAST RECTIFIERS

B. Rivet

The use of several rectifiers connected in series is necessary to obtain voltage ratings beyond the capabilities of single diodes and also when some special requirement, such as very low switching losses, oblige to implement several low voltage ultra fast diodes.

Rectifiers connected in series tend to share unequally the voltage across the string in blocking conditions because of the variations in reverse characteristics : leakage currents and turn off switching parameters.

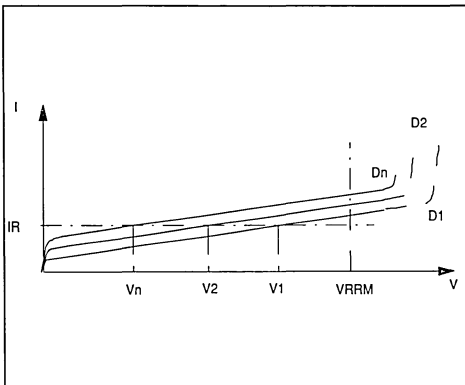
To ensure that each diode operates within its voltage rating it is generally necessary to add a voltage sharing network.

This paper gives the rules of calculation of this auxiliary network and shows how this circuit could be optimized : reduction of power dissipation and cost.

I - STEADY STATE VOLTAGE SHARING :

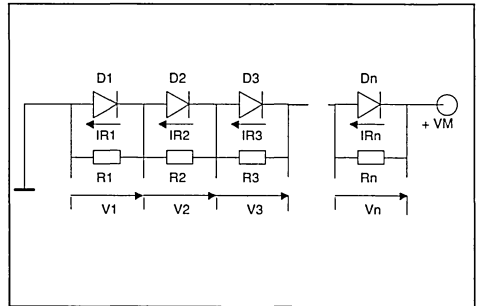
The difference in blocking characteristics results in unequal steady state voltage (fig.1).

Figure 1 : Dispersion of diodes reverse characteristics. The reverse current through the string D1, D2, ..., Dn is I_R and the voltages across the diodes are respectively $V_1, V_2; \dots V_n$.



In order to equalize the voltage, a resistor is connected across each diode (Fig.2).

Figure 2 : Use of shunt resistors for steady state voltage sharing.



1) Calculation of sharing resistors :

The calculation of these resistances is based on the worst case situation.

The maximum unbalance in blocking voltage when n diodes are connected in series occurs when (n-1) diodes have the maximum leakage current and one diode D1 has the lowest possible leakage current.

In this case D1 will support the highest voltage V_1 and this tendency is aggravated by the assumption that the corresponding resistor R1 is at the upper limit of its tolerance (a), while all the others are at the lowest limit so,

$$R1 = R(1+a)$$

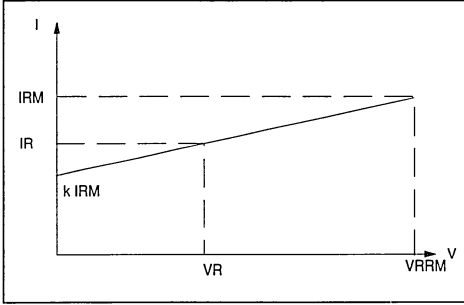
$$R2 = R3 = \dots Rn = R$$

In order to calculate the current in the string we approximate the reverse characteristic with a straight line. We define the slope by the coefficient k according to fig.3.

Figure 3 : Reverse characteristic modelisation of a fast rectifier.

$$I_R + I_{RM}(T_j) \cdot \left[k + \frac{V_R(1-k)}{V_{RRM}} \right]$$

With $k = 0.8$



So the leakage current I_{RM} of diodes D2 ... Dn under the blocking voltage $V_2 \dots V_n$ is :

$$I_{R2} = I_{R3} = \dots I_{Rn} = I_{RM} \left[k + \frac{V_n(1-k)}{V_{RRM}} \right]$$

where I_{RM} is the maximum leakage current at V_{RRM} (maximum voltage specified for this diode) and at the operating junction temperature. For D1 the maximum reverse current at V_{RRM} is :

$$I_{RM} - \Delta I_R$$

In these conditions the leakage current of diode D1 is :

$$I_{R1} = (I_{RM} - \Delta I_R) \left(k + \frac{V_1(1-k)}{V_{RRM}} \right)$$

Taking into account all these parameters, the voltage V_1 across the diode D1 is given by the relation :

$$V_1 = \frac{V_M(1+a)(V_{RRM} + (1-k)I_{RM}R) + k(n-1)(1+a)\Delta I_R R V_{RRM}}{R I_{RM} n(1-k)(1+a) + V_{RRM}(n+a) - R\Delta I_R(1-k)(1+a)(n-1)} \quad (1)$$

The resistance R must be chosen to limit the voltage V_1 under the maximum value V_{RRM} specified for this rectifier. Thus :

$$R < \frac{V_{RRM}(V_{RRM}(n+a) - V_M(1+a))}{\Delta I_R V_{RRM}(1+a)(n-1) - I_{RM}(1-k)(1+a)(nV_{RRM} - V_M)} \quad (2)$$

For the to-day fast rectifiers we can use $k=0.8$

2) I_{RM} evaluation

I_{RM} is the maximum leakage current at the

maximum reverse voltage V_{RRM} . This current depends on the junction temperature (Fig.4).

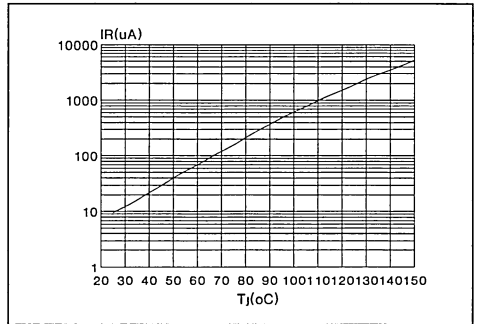
Generally in the data sheet the manufacturer specifies a maximum value I_{RM} at V_{RRM} at $T_j=100^\circ\text{C}$.

When we know the operating junction temperature (T_j) it is possible to calculate I_{RM} by using the following relation :

$$I_{RM}(T_j) = I_{RM}(100^\circ\text{C}) \exp[-0.054(100-T_j)]$$

Figure 4 : Reverse leakage current versus junction temperature.

Example :
BYT 261-1000 (typical value)



3) ΔI_R estimation

In fact ΔI_R is the sum ΔI_{R1} and ΔI_{R2}

- ΔI_{R1} is due to the leakage current dispersion of the rectifiers in the same conditions of voltage and temperature.

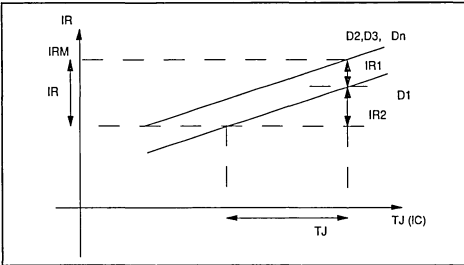
For the fast rectifiers to day available on the market the dispersion of the reverse current at $V_R = V_{RRM}$ and $T_j = 100^\circ\text{C}$ is about :

$$\Delta I_{R1} = 0.6 I_{RM}$$

This dispersion varies from one batch to another.

- ΔI_{R2} is due to the difference between the junction temperatures of each devie (ΔT_j).

Figure 5 : The variation ΔI_R is the dispersion of I_R at max operation junction temperature (ΔI_{R1}) plus the variation due to T_j (ΔI_{R2})



The junction temperature is given by the thermal resistance junction to ambient $R_{th(j-a)}$ and the power dissipation due to the conduction losses (PC) and the switching losses (PS).

PC is linked to the forward voltage (V_F) and PS is linked to the reverse recovery charge (Q_{RR}). So the variation of the junction temperature is :

$$\Delta T_j = \Delta R_{th} (PC + PS) + R_{th} \left(\frac{\Delta V_F}{V_F} PC + \frac{\Delta Q_{RR}}{Q_{RR}} PS \right)$$

Where ΔV_F is the dispersion of the forward voltage and Q_{RR} the dispersion of the reverse recovery charge.

For series operation, it is recommended to use pieces coming from the same lot, so the dispersion on the parameters V_F , Q_{RR} and R_{th} is minimized;

In most cases the evaluation of ΔT_j is difficult but, from experience, it is generally lower than 10°C.

We propose to take a safety margin and to use :

$$\Delta I_R = 0.85 I_{RM}$$

4) Simplified formula

The relation (2) is often used by using the following approximations

$k = 1$: supposing the reverse current I_{RM} constant, whatever the blocking voltage across the diode.

$a = 0$: Neglecting the effect of the tolerance of resistors. thus :

$$R < \frac{n V_{RRM} - V_M}{(n-1) \Delta I_R}$$

As for the ΔI_R the worst case is taken into account.

$$\Delta I_R = I_R \quad \text{with } I_R = I_{R \text{ max at } T_j \text{ max specified (100°C)}}$$

$$R < \frac{n V_{RRM} - V_M}{(n-1) I_R}$$

This formula is "pessimistic" and induces a low resistance and then a high power dissipation.

5) Example

- Given

Maximum blocking voltage : $V_M = 2500V$

Part number used : BYT12-PI1000

Power dissipation per diode : $P = 7W$

Case temperature : $T_{case} = 52^\circ C$

- Rectifier specification :

$V_{RRM} = 1000V$

I_R (Max at $T_j = 100^\circ C$) = 2.5mA

$R_{th j-c} = 4^\circ C/W$

- Problem :

Calculation of sharing resistors for 3 diodes in series.

- Solutions :

a) Simplified method :

$$R < \frac{n V_{RRM} - V_M}{(n-1) I_R}$$

With

$$n = 3$$

$$V_{RRM} = 1000V$$

$$V_M = 2500V$$

$$I_R = 2.5mA$$

Thus

$$R_{min} = 100 \text{ kOhms}$$

Power dissipation per resistor : 3.45 W ! (with duty cycle $\delta = .5$)

b) Calculation with relation (2) :

$$R < \frac{V_{RRM} (V_{RRM} (n+a) - V_M (1+a))}{\Delta I_R V_{RRM} (1+a)(n-1) - I_{RM} (1-k)(1+a)(n V_{RRM} - V_M)}$$

General data for fast rectifiers :

$$\Delta I_R = 0.85 I_{RM}$$

$$k = 0.8$$

Intermediate calculations :

$$T_j = P.R_{th j-c} + T_{case} = 80^\circ C$$

$$I_{RM} = I_{RM}(80^\circ C)$$

$$= I_{RM}(100^\circ C) \exp[-0.0054(100-80)]$$

$$= 0.85mA$$

$$\Delta I_{RM} = 0.72mA$$

APPLICATION NOTE

Assuming we use resistors with 5% of tolerance, then $a = .10$

Let : $R_{min} = 220 \text{ kOhms}$

Power dissipation per resistor = $1.58W$ (with $\delta = .5$)

6) Question : is it possible to remove the sharing resistors ?

With the relation (1) we can find the value of $V1$ when the value of R tends to infinite. Then we calculate the condition to have

$$V1 < V_{RRM}$$

Solving we find

$$\frac{\Delta I_R}{I_{RM}} < \frac{(1-k)(n V_{RRM} - V_M)}{V_{RRM}(n-1)}$$

In the previous example this condition should be

$$\frac{\Delta I_R}{I_{RM}} = 5\%$$

If is obvious that this condition is generally very difficult to meet without hard selection.

II - TRANSIENT VOLTAGE SHARING

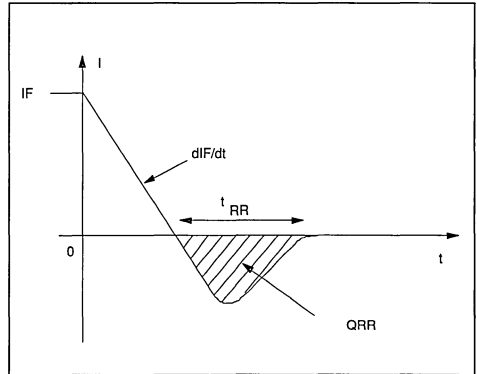
1) The problem

When a diode is switched from the forward conduction to the reverse blocking state, a reverse current flows through the device during the reverse recovery time t_{rr} .

After this delay all the charges (minority carriers) stored in the junction are eliminated and the diode turns off. The time integral of the reverse recovery current is called reverse recovery charge (Q_{RR}).

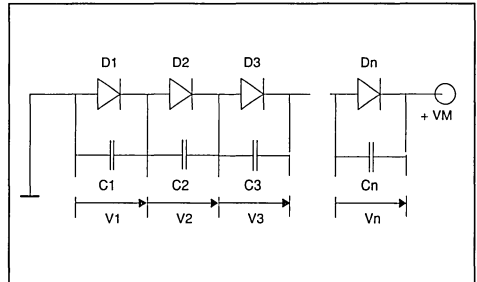
Fig.6 defines the reverse recovery parameters. When a string of n diodes in series switches off, the diode which has the lowest recovery charge turns off the first and supports an important proportion of the total voltage V_M and its maximum reverse voltage V_{RRM} could be reached or exceeded.

Figure 6 : Reverse recovery current waveform.



Voltage sharing during the reverse recovery phase is achieved by using a shunt capacitors string connected across the diodes (Fig.7).

Figure 7 : Use of shunt capacitors for transient voltage sharing.



2) Calculation of sharing capacitors

The calculation of capacitance C is also based on the worst case situation.

We assume that $(n-1)$ diodes $D2, D3 \dots Dn$ with a reverse recovery charge $Q_{RR} + \Delta Q_{RR}$, and one diode $D1$ with lowest value Q_{RR} .

We suppose also that the corresponding capacitor $C1$ is at the lowest limit of tolerance (a) while the others are at the upper limit

so : $C1 = C$
 $C2 = C3 = \dots = Cn = C(1+a)$

When all the stored charges of diode $D1$ have been evacuated, the charge remaining in the other diodes is ΔQ_{RR} .

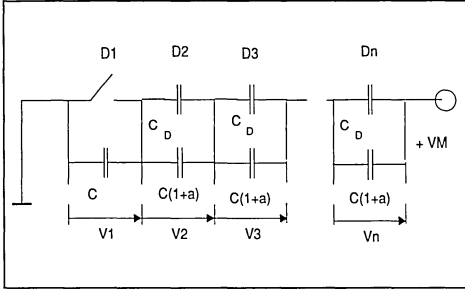
At this time the voltage across $D1$ is $V1$ and the voltage across the other diodes of the string is :

$$V_2 = V_3 = \dots V_n = \frac{V_M - V_1}{(n-1)}$$

So these diodes can be assimilated to a capacitor

$$C_D = \frac{\Delta Q_{RR}}{V_n} = \frac{\Delta Q_{RR} (n-1)}{V_M - V_1}$$

Figure 8 : Equivalent diagram when D1 switches off. Diodes D2, D3,Dn are equivalent to a capacitor CD = ΔQRR(n-1) / (VM-V1)



In these conditions the voltage across D1 is :

$$V_1 = \frac{\Delta Q_{RR} (n-1) + C V_M (1+a)}{C (n+a)}$$

In order to limit the voltage across D1 under the specified value V_{RRM} we calculate C by solving thus : $V_1 < V_{RRM}$

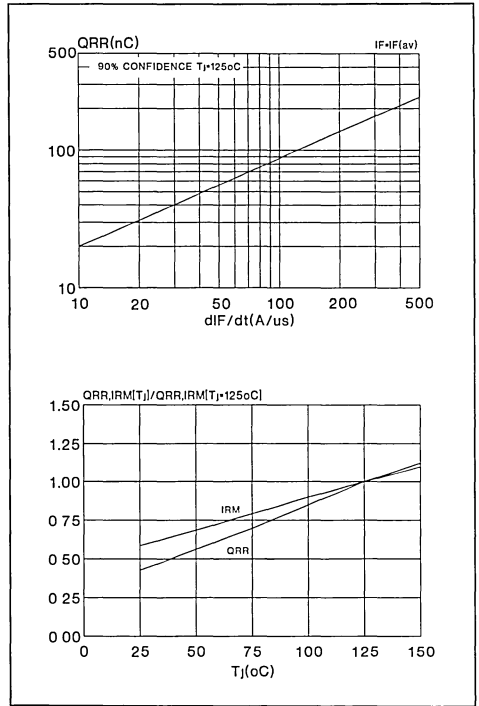
$$C > \frac{(n-1)\Delta Q_{RR}}{(n+a)V_{RRM} - V_M(1+a)}$$

3) QRR and ΔQRR consideration

For a given diode the reverse recovery charge QRR is function of the circuit commutation conditions such as the magnitude of forward current (IF), the rate of decay of this current (dIF/dt) and the junction temperature.

Typical values of QRR are given in the data sheet of each part number (Fig.9).

Figure 9 : Example of reverse recovery charge specification. (case of BYW 51)



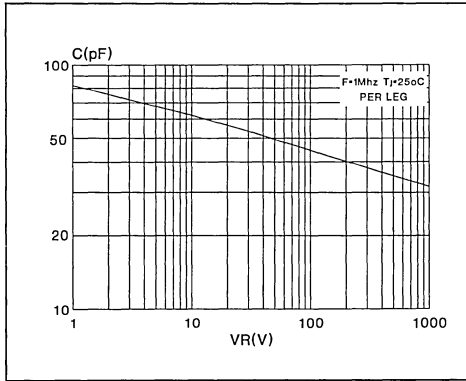
For fast rectifiers coming from the same lot the dispersion of this parameter is low and we can use, with a good safety margin :

$$\Delta Q_{RR} = .30 Q_{RR}$$

4) Is it possible to remove the equalizing capacitor ?

In blocking state diodes have a junction capacitance. For a given diode this capacitance decreases with an increase in the applied reverse voltage according to Fig.10.

Figure 10 : Junction capacitance versus reverse voltage
(example : BYT 261-1000)



When D1 has evacuated all its stored charge it is equivalent to a capacitor CJ1 and the other diodes D2, D3 ... Dn are equivalent to a capacitor which is the sum of the junction capacitance CJ2, CJ3 ... CJn and the capacitance

$$C_D = \frac{\Delta Q_{RR} (n-1)}{V_M - V_1}$$

Figure 11 : Equivalent diagram when D1 switches off in case of low QRR : The junction capacitances CJ1, CJ2;CJn, play the role of sharing capacitors.

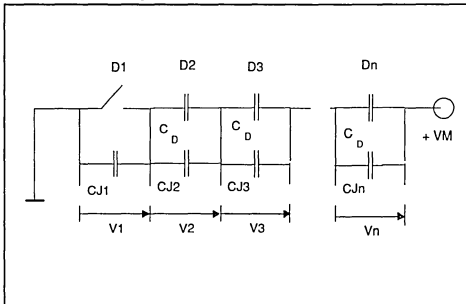


Fig.11 shows the equivalent circuit

In the worst case CJ1 is the junction capacitor of D1 at the maximum voltage VRRM
Putting

$$C_{J1} = C_J \text{ at } V_{RRM}$$

$$C_{J2} = C_{J3} \dots C_{Jn} = C_J \text{ at } \frac{V_M - V_{RRM}}{n-1}$$

We have

$$V_1 = \frac{\Delta Q_{RR} (n-1) + V_M C_{Jn}}{C_{J1} (n+1) + C_{Jn}}$$

Auxiliary capacitors are not necessary if

$$V_1 < V_{RRM}$$

$$\text{or } \Delta Q_{RR} < \frac{V_{RRM} [C_{J1} (n-1) + C_{Jn}] - V_M C_{Jn}}{n-1}$$

Generally, the value of the junction capacitance at the operating voltage is very close to the value at VRRM (CJ1) so we can write

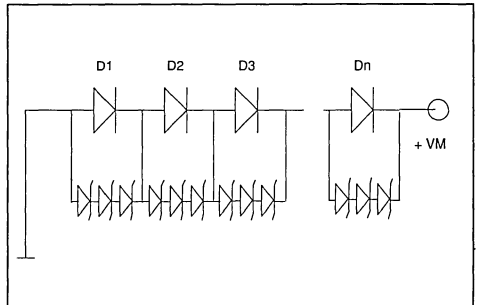
$$\Delta Q_{RR} < \frac{C_{J1} (n V_{RRM} - V_M)}{n-1}$$

This condition can be met by using very fast rectifiers in applications where the diF/dt is low (like in some resonant converters or flyback converters) and consequently low QRR.

III - EQUALIZATION BY TRANSIL DIODES

TRANSIL are avalanche diodes designed for operation in breakdown characteristic and they are used as clamping device in a wide field of applications. To limit the voltage across the rectifiers of a string below the maximum value, TRANSIL diodes can be used according to diagram Fig.12.

Figure 12 : Voltage sharing by TRANSIL diodes.



TRANSIL operates as a voltage limiter at steady state, during the switching phase, and also in case of external voltage transients.

1) Steady state

In blocking condition the TRANSILs connected across the diode D1 (Which has the lowest reverse current) operate in the breakdown

characteristic. The current through these TRANSILS is I_R and the power dissipation is :

$$V_{BR} \cdot \Delta I_R \cdot \delta \quad (\delta = \text{duty cycle})$$

Where V_{BR} is the maximum breakdown voltage of TRANSILS. In general this extra power dissipation is lower than in the case of sharing by resistors and TRANSILS in axial packages can be used.

2) Switching phase

When the fastest diodes of the string switches off the TRANSILS across it operate in breakdown characteristic and the reverse recovery current of the other diodes flows through these TRANSILS. The charge remaining in the string at this moment is :

$$(n-1) \Delta Q_{RR}$$

and we can estimate the maximum energy in the TRANSILS with

$$E < 1/2(n-1) \cdot \Delta Q_{RR} \cdot V_{BR}$$

This relation does not take into account the losses due to the capacitive current through the string.

3) Example

GIVEN :

Use of a 3-BYT12-PI1000 for $V_M = 2500V$

Operating conditions :

$$\begin{aligned} T_j &= 100^\circ C \\ di/dt &= 20A/\mu s \\ F &= 25 \text{ kHz} \\ \delta &= .5 \end{aligned}$$

RECTIFIER SPECIFICATION :

$$\begin{aligned} V_{RRM} &= 1000V \\ I_{RM} \text{ at } V_{RRM} &= 2.5mA \text{ at } T_j = 100^\circ C \\ Q_{RR} &= .5\mu C \text{ (in operating conditions)} \end{aligned}$$

PROBLEM :

3 TRANSILS diodes are connected in series across each rectifier. What is the suitable part number ?

DESIGN STEPS :

- V_{BR} calculation :

$$V_{BR} \min > \frac{2500}{3 \times 3} = 277V$$

$$V_{BR} \max < \frac{1000}{3} = 333V$$

- Power dissipation in steady state :

$$P1 < I_R \cdot V_{BR} \max \cdot \delta$$

$$\begin{aligned} \text{with } I_R &= .85 \times 2.5 \approx 2mA \\ V_{BR} \max &= 330V \\ P1 &< 330mW \end{aligned}$$

- Power dissipation in switching phase :

$$\begin{aligned} P2 &= E \cdot F < 1/2 (n-1) Q_{RR} \cdot V_{BR} \max \cdot F \\ \text{with } \Delta Q_{RR} &= .5 \times .3 = .15\mu C \\ F &= 25 \text{ kHz and } n = 3 \\ \text{then } P2 &< 1.2W \end{aligned}$$

- Max total power dissipation $P1 + P2$ 1.530 W

Solution : 1.5 KE series can be used (1.5KE300CP)

CONCLUSION

When using several fast rectifiers in series it is necessary to make sure that any diode will not be subjected to continuous or transient voltages in excess of their ratings.

In most cases, this is achieved by using sharing networks across each diode. It is important to optimize this circuit in order to reduce power consumption and to save space.

Parallel resistor can be optimized by using the modelisation of the fast recovery diodes reverse characteristic proposed in this paper. Then, thanks to a good knowledge of the reverse current and its variation in the operating conditions (possibly by measurement and selection) it is possible to implement a resistor with a value as high as possible.

Parallel capacitors also have to be reduced as much as possible with the knowledge the switching characteristics of the string in the actual conditions. The reverse recovery charge (Q_{RR}) is not always accessible with the datasheet and a measurement is often necessary.

In certain applications using ultra fast diodes of the same lot, where the Q_{RR} , and therefore the ΔQ_{RR} is very low, the sharing capacitor can be reduced to zero.

In systems where there is a risk of external overvoltages or where there are transient states not well known, TRANSIL diodes are a solution to the sharing voltage problem insofar as the total power dissipation of the TRANSIL string remains compatible with the existing packages for these devices.

References :

1. B.M. BIRD and K.G. KING : "An introduction to Power Electronics"
2. J.M. PETER - SGS-THOMSON Microelectronics : "Analysis and optimisation of high frequency Power rectification"

PARALLEL OPERATION OF POWER RECTIFIERS

B. Rivet

INTRODUCTION

In parallel operation of several diodes, the current is not split into equal parts because of differences between forward characteristics.

The current through the rectifier having the lowest voltage drop will be higher than the current through the other diodes.

On the other hand the temperature coefficient of the forward voltage is negative and therefore this unbalanced situation at switching ON can become worse up to a stable equilibrium state.

The designer has to be sure that at this final state the diodes operate below the maximum specified limits.

The aim of this study is to calculate the acceptable difference between forward voltage drops of diodes to be paralleled in a given application.

I - QUALITATIVE ANALYSIS AND LIMITATIONS

Let's assume that we have two diodes D1 and D2 connected in parallel.

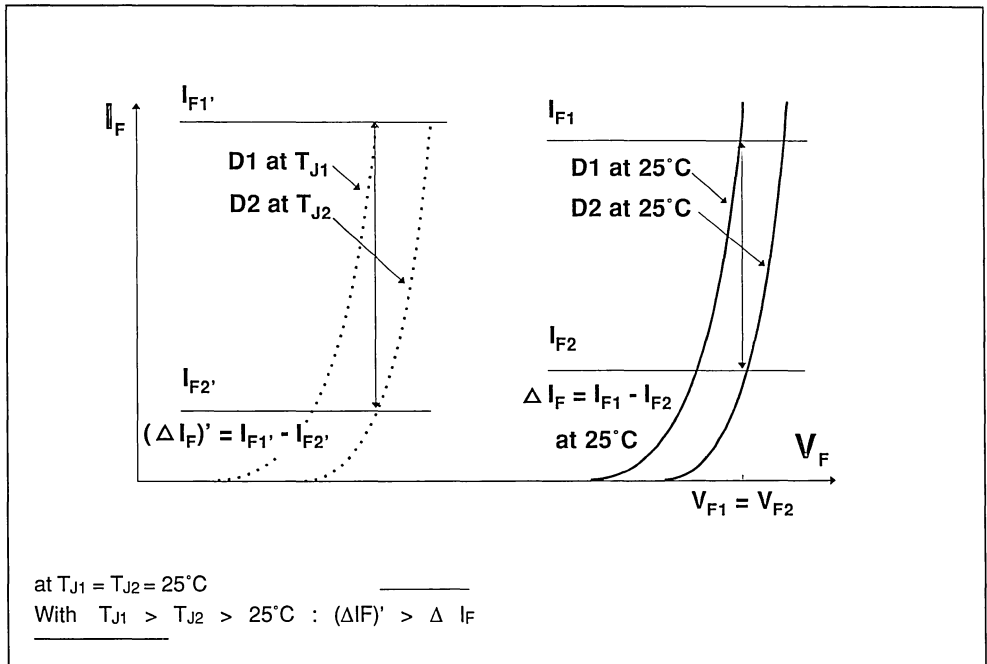
The forward characteristics of the two diodes at $T_{J1} = T_{J2} = 25^\circ\text{C}$ are shown in fig.1.

The total current $I_T = I_{F1} + I_{F2}$ is not split into equal parts.

The thermal dissipation makes the difference $\Delta I_F = I_{F1} - I_{F2}$ increase.

Indeed, the current through D1 is higher than through D2 so $T_{J1} > T_{J2}$, and because the forward voltage has a negative temperature coefficient, the difference ΔI_F increases.

Fig.1 : Forward characteristics of two diodes D1 and D2 in parallel



APPLICATION NOTE

For a safe and reliable operation it is absolutely necessary to remain within the maximum ratings of the devices :

- 1) T_{J1} lower than the maximum junction temperature
- 2) Current through D1 compatible with the specified maximum RMS current.

II - SIMPLIFIED FORWARD CHARACTERISTIC MODEL

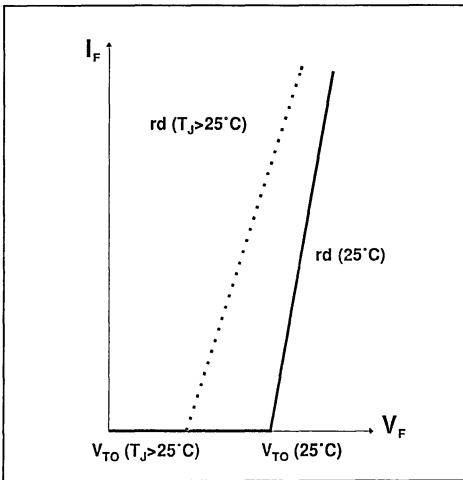
The forward characteristic of a diode may be assimilated to a straight line whose equation is :

$$V_F = V_{TO} + r_d \times I_F \quad (\text{fig.2})$$

V_{TO} and r_d act as a function of the temperature.

V_{TO} has a negative temperature coefficient (α_{TO}) and r_d has a positive temperature coefficient (α_{rd}).

Fig.2 : Forward characteristics model of rectifier versus temperature

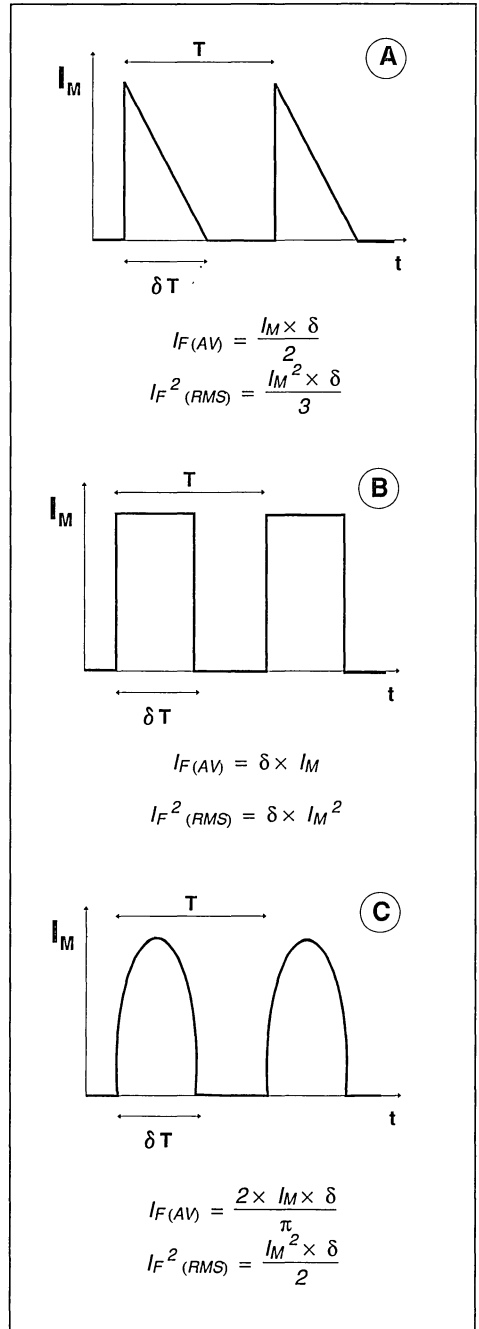


This model allows to easily calculate the operating point (V_F , I_F) of each diode and to evaluate the power losses due to the conduction.

$$P_{cond} = V_{TO} \times I_{F(AV)} + r_d \times I_{F(RMS)}^2 \quad (1)$$

In practice the waveforms of current can be assimilated to simple forms (rectangular, triangular, sinusoidal), so $I_{F(AV)}$ and $I_{F(RMS)}$ can be expressed with the peak current (I_M) and the duty cycle (δ) (Figure 3)

Fig.3 : Average and RMS values for different currents wave forms

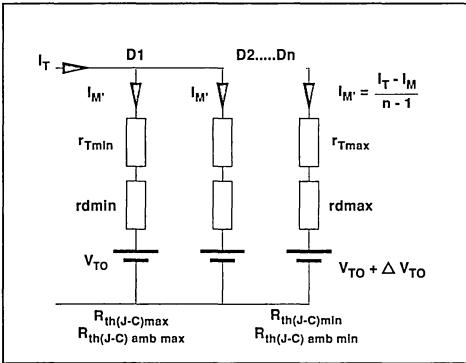


III - OPERATING WITH SEVERAL DIODES IN PARALLEL

Taking into consideration the dispersion of both the diodes parameters as well as the circuit parameters, we can calculate the maximum difference between V_F (measured at 25°C and at the nominal current specified for the device $I_F = I_{F(AV)}$) in order to be sure than no diode will operate out of its specification.

The calculation is based on the worst case situation (Figure 4) : we suppose that D1 has the lowest V_{TO} and r_d and the highest $R_{th(j-c)}$ and T_{CASE} . This diode supports the highest current I_M and operates at the highest junction temperature.

Fig.4 : Worst configuration of several diodes in parallel



As a first step, we have to determine the maximum acceptable peak current (I_M) through D1 in these conditions.

III.1. Thermal limitation : I_{M1}

The maximum total power dissipation in the diode is given by :

$$P_T = \frac{T_{Jmax} - T_{CASE(max)}}{R_{th(j-c)max} + R_{th(c)}^*}$$

The total power dissipation is

$$P_T = P_{COND} + P_{COM}$$

P_{COND} : conduction losses $P_{COND} = \rho P_T$

P_{COM} : commutation losses $P_{COM} = (1 - \rho) P_T$

For SCHOTTKY diodes, the commutation losses are negligible ($\rho = 1$)

(*) Case of double diodes.

$R_{th(c)}$: Coupling thermal resistance

We can write P_{COND} versus I_M for rectangular waveform :
(For the other waveforms see the annex).

$$P_{COND} = V_{TO}(100^\circ C) \delta \cdot I_M + r_d(100^\circ C) \delta \cdot I_M^2$$

So

$$I_{M1} = \frac{-V_{TO} \cdot \delta + [(V_{TO} \cdot \delta)^2 + 4 \cdot P_{COND} \cdot r_d \cdot \delta]^{+1/2}}{2 \cdot r_d \cdot \delta} \quad (2)$$

III.2. RMS current limitation : I_{M2}

If $I_{F(RMS)}$ is the maximum RMS current specified in the data sheet, the limit in the case of a rectangular waveform will be :

$$I_{M2} = \frac{I_{F(RMS)}}{\sqrt{\delta}}$$

It is obvious that we will take the minimum value of I_{M1} and I_{M2}

III.3. Calculation of ΔV_F

* THE DIODES PARAMETERS ARE :

∞T_O	Temperature coefficient of V_{TO}
∞r_d	Temperature coefficient of r_d
V_{TO}	Threshold voltage at $T_J = 25^\circ C$
r_d	Dynamical resistance at $T_J = 25^\circ C$ and its dispersion (r_{dmin} , r_{dmax})
$R_{th(j-c)}$	Junction to case thermal resistance and its dispersion $R_{th(j-c)min}$, $R_{th(j-c)max}$.
T_{Jmax}	max operating junction temperature

* THE "APPLICATION" PARAMETERS ARE :

I_T	Peak current through the diodes and its waveform.
δ	Duty cycle
n	Number of diodes
T_C	Case temperature and the dispersion T_{Cmin} (coldest case) and T_{Cmax} (hottest case)
r_{tmax} r_{tmin}	Min and max values of the resistances of wires and various connections.

By solving electrical and thermal equations corresponding to the circuit of the fig.5 in the case of rectangular waveform , we find :

$$\Delta V_F < \frac{\Delta V_{F1} + \Delta V_{F2} + \Delta V_{F3} - \Delta V_{F4}}{\Delta}$$

APPLICATION NOTE

With

$$\Delta V_{F1} = (r_T \text{ min} + rd \text{ min}) I_M - (r_T \text{ max} + rd \text{ max}) I_M'$$

$$\Delta V_{F2} = R_{th(j-c) \text{ max}} (\alpha_{TO} + \alpha_{rd} \cdot I_M) \cdot P_1$$

$$\Delta V_{F3} = (\alpha_{TO} + \alpha_{rd} \cdot I_M) \cdot (T_{C \text{ max}} - T_{C \text{ min}})$$

$$\Delta V_{F4} = R_{th(j-c) \text{ min}} \cdot (\alpha_{TO} + \alpha_{rd} \cdot I_M') \cdot P_2$$

$$\Delta = 1 + R_{th(j-c) \text{ min}} [\alpha_{TO} + rd \cdot I_M'] \cdot \delta \cdot I_M'$$

$$P_1 = \frac{V_{TO} \delta I_M + rd \text{ min} \delta I_M'^2}{\rho}$$

$$P_2 = \frac{V_{TO} \cdot I_M' + rd \text{ max} \cdot I_M'^2}{\rho}$$

$$I_M' = \frac{I_T - I_M}{n - 1}$$

III.4. Information about of diodes parameters

α_{TO} and α_{rd} are given for some part numbers in the following table :

	BYV255 -xxx	BYT60P -xxx	BYW51 -xxx
$\alpha_{TO} \left(\frac{V}{^\circ C} \right)$	-1.6 10 ⁻³	-1.6 10 ⁻³	-1.6 10 ⁻³
$\alpha_{rd} \left(\frac{\Omega}{^\circ C} \right)$	+2 10 ⁻⁶	+3 10 ⁻⁶	+16 10 ⁻⁶

* Datasheet gives $V_{TO \text{ max}}$ (100°C) and $rd \text{ max}$ (100°C)

with these values we can determine $V_{TO}(25^\circ C)$ and $rd \text{ max}$ (25°C) :

$$V_{TO} (25^\circ C) = V_{TO \text{ max}} (100^\circ C) - \alpha_{TO} \times 75$$

$$rd \text{ max} (25^\circ C) = rd \text{ max} (100^\circ C) - \alpha_{rd} \times 75$$

* $rd \text{ min}$ and $R_{th(j-c) \text{ min}}$ can be calculated by :

$$rd \text{ min} = k \cdot rd \text{ max} \quad \text{with } k = 0.75$$

$$R_{th(j-c) \text{ min}} = k \cdot R_{th(j-c) \text{ max}} \quad \text{with } k = 0.75$$

* We recommende to take $T_{J \text{ max}} = 110^\circ C$ to increase the safety margin for parallel operation.

IV - EXAMPLES OF APPLICATION

IV.1. Example of rectifiers in discret package

In this example we look for the maximum peak current I_T versus V_F that can flow in three BYV255 ($n = 6$) connected in parallel.

The current is rectangular and we consider 3 different duty cycles ($\delta = 0.3$ $\delta = 0.5$ $\delta = 0.7$).

As a good estimation, the conduction losses can be considered to be 95 % of the total losses ($\delta = 0.95$)

Application data is

$$\begin{aligned} T_{C \text{ max}} &= 80^\circ C \\ T_{C \text{ min}} &= 78^\circ C \\ \rho &= 0.95 \\ r_T \text{ max} &= 0.5 \text{ m } \Omega \\ r_T \text{ min} &= 0.4 \text{ m } \Omega \end{aligned}$$

Diodes data is

From data sheet of BYV255 we get :

$$\begin{aligned} R_{th(j-c) \text{ max}} &= 0.4^\circ C/W \\ R_{th(c)} &= 0.1^\circ C/W \\ V_{TO \text{ max}} &= 0.7 \text{ V (at } 100^\circ C) \\ rd \text{ max} &= 1.35 \text{ m } \Omega \text{ (at } 100^\circ C) \\ I_{F(RMS)} &= 150 \text{ A} \end{aligned}$$

From the recommandations of § 3.4 we can calculate :

$$\begin{aligned} R_{th(j-c) \text{ min}} &= 0.3^\circ C/W \\ V_{TO} \text{ at } 25^\circ C &= 0.82 \text{ V} \\ rd \text{ max at } 25^\circ C &= 1.20 \text{ m } \Omega \\ rd \text{ min at } 25^\circ C &= 0.9 \text{ m } \Omega \end{aligned}$$

Calculations :

a) I_{M1}

In this example we have to take into account $R_{th(c)}$ because there are two diodes in the package. Thus :

$$P_{COND} = \frac{\rho (T_{J \text{ max}} - T_{C \text{ max}})}{R_{th(j-c)} + R_{th(c)}}$$

$$P_{COND} = 57 \text{ W}$$

The following table gives I_{M1} value for $\delta = 0.3 - 0.5 - 0.7$ (according to the relation (2) of page 3)

δ	$I_{M1} [A]$
0.3	196
0.5	130
0.7	97

b) I_{M2}

$$I_{M2} = \frac{I_{F(RMS)}}{\sqrt{\delta}}$$

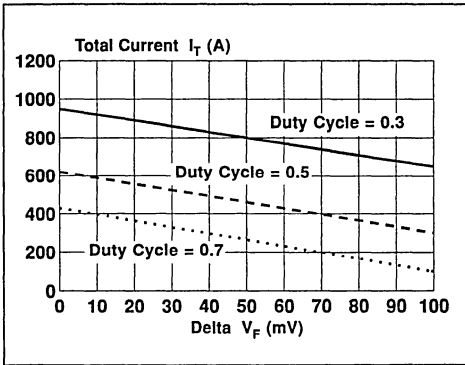
The following table gives the I_{M2} limits for $\delta = 0.3 - 0.5 - 0.7$

δ	I_{M2} [A]
0.3	274
0.5	212
0.7	179

c) Results

These two tables show that the I_M current is imposed by thermal considerations ($I_{M1} < I_{M2}$).

Using formulas (5) - (6) - (7) - (8) we can draw the Fig.5 : Peak current I_T versus ΔV_F for different duty cycles with 3 BY255 in parallel



curve Fig.5 I_T versus ΔV_F for different duty cycles.

IV.2 Example of double rectifiers

In this example we consider a BYW51. The two diodes in the same package are connected in parallel. The current is rectangular with $\delta = 0.5$. The commutation losses are negligible ($\rho = 1$)

Application data is :

- $\rho = 1$
- $r_{T \min} = 0.5 \text{ m}\Omega$
- $r_{T \max} = 0.5 \text{ m}\Omega$

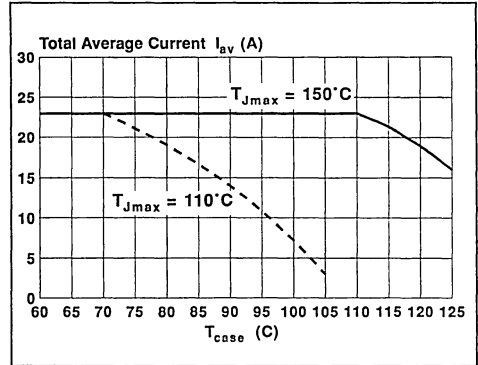
Diode data :

From data sheet of BYW51 we get

- $R_{th(j-c)} = 2.5C/W$
- $R_{th(c)} = 0.1C/W$
- $V_{TO \max} = 0.66 \text{ V (at } 100C)$
- $rd \max = 14 \text{ m}\Omega \text{ (at } 100C)$

Fig.6 shows the total average current versus T_c . The flat part of the curves corresponds to the $I_{F(RMS)}$ limitation and the other part corresponds to the thermal limitation. The calculation is done with $\Delta V_F = 30 \text{ mV}$.

Fig.6 : I_{AV} versus T_c for BYW51 double rectifier in parallel operation ($\delta = 0.5$)

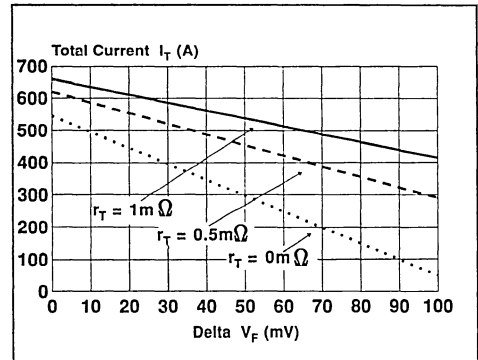


V - INFLUENCE OF THE WIRING RESISTANCE : r_T

When all diodes are connected through the same wiring resistance, the total current is better split into the circuitry.

Fig.7 shows the good influence of the wiring resistance when all diodes are connected through the same r_T (Same conditions as BYV255 example, with $\delta = 0.5$)

Fig.7 : I_T versus ΔV_F for different resistances of connections. (Case of 3 BYV255 with $\delta = 0.5$)

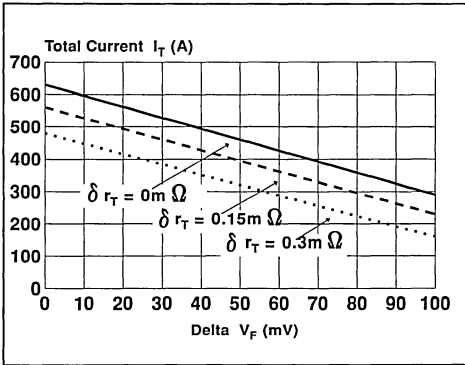


If diodes are connected through very different wiring resistance, the current imbalance can be important.

Fig.8 shows r_T influence for different values of r_T tolerance.

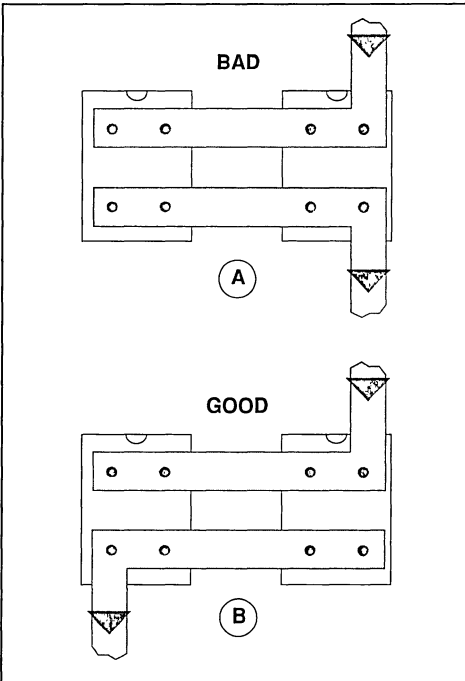
APPLICATION NOTE

Fig.8 : It versus ΔV_F for different wiring resistance dispersion.
(Case of 3 BYV255 with $\delta = 0.5$)



Particular care must be taken to connect several diodes in parallel. The assembly must be as symmetrical as possible in order to reduce variation of r_T from one rectifier to another (see Fig.9). In the same way it is necessary to mount the packages on a single and efficient heat sink in order to reduce the variation of the case temperatures.

Fig.9 : Assembly of 2 ISOTOP packages :
(B) configuration provides a better balance of stray resistances



VI - COMMENTS ABOUT ΔV_F IN MANUFACTURING

VI.1 Double rectifiers (*) (2 diodes in the same package) :

These devices house 2 silicon dice coming from the same wafer and the dispersion is low :

90% of the production offers a ΔV_F lower than 30 mV.

VI.2 Rectifiers in separate packages : (or discrete)

In this case the dispersion is more important and when a ΔV_F lower than 100 mV is needed in the application, a screening is necessary.

VII - CONCLUSION

Ultra fast rectifiers and power schottky diodes can be easily connected in parallel to provide a reliable high current device if a few simple rules are applied.

This paper shows how we can calculate, for a given application, the maximum value of the forward voltage drop variation (ΔV_F) which guarantees that each diode will operate always below its maximum ratings.

This calculation takes into account the dispersion of the diode parameters (given by the manufacturer) and the electrical and thermal characteristics of the circuit.

Thus, it is possible to know if a special selection in term of V_F is needed or if the number of diodes connected in parallel is large enough to allow the use of standard parts without risk of overcurrent for one of the rectifiers.

(*) BYT261 - BYV255 - BYW51, ... etc

ANNEX

A - TRIANGULAR WAVEFORM

$$I_{M1} = \frac{-V_{TO} \left(\frac{\delta}{3}\right) + \left[V_{TO} \cdot \frac{\delta}{2}\right]^2 + 4 \cdot P_{COND} \cdot rd \cdot \frac{\delta}{3}]^{1/2}}{(2/3) \cdot rd \cdot \delta}$$

$$I_{M2} = \frac{I_{F(RMS)} \sqrt{3}}{\delta}$$

$$\Delta V_F < \frac{\Delta V_{F1} + \Delta V_{F2} + \Delta V_{F3} - \Delta V_{F4}}{\Delta}$$

With

$$\Delta V_{F1} = (r_T \min + rd \min) \cdot I_M - (r_T \max + rd \max) \cdot I_M'$$

$$\Delta V_{F2} = R_{th(j-c) \max} (\alpha_{TO} + \alpha_{rd} \cdot I_M) \cdot P_1$$

$$\Delta V_{F3} = (\alpha_{TO} + \alpha_{rd} \cdot I_M) \cdot (T_{C \max} - T_{C \min})$$

$$\Delta V_{F4} = R_{th(j-c) \min} \cdot (\alpha_{TO} + \alpha_{rd} \cdot I_M') \cdot P_2$$

$$\Delta = 1 + R_{th(j-c) \min} [\alpha_{TO} + rd \cdot I_M'] (\delta/2) \cdot I_M'$$

$$P_1 = \frac{V_{TO} (\delta/2) \cdot I_M + rd \min (\delta/3) \cdot I_M^2}{\rho}$$

$$P_2 = \frac{V_{TO} (\delta/2) \cdot I_M' + rd \max (\delta/3) \cdot I_M'^2}{\rho}$$

$$I_M' = \frac{I_T - I_M}{n - 1}$$

B - SINUSOIDAL WAVEFORM

$$I_{M1} = \frac{-2 V_{TO} \left(\frac{\delta}{\pi}\right) + \left[2 V_{TO} \cdot \frac{\delta}{\pi}\right]^2 + 2 \cdot P_{COND} \cdot \delta \cdot rd]^{1/2}}{rd \cdot \delta}$$

$$I_{M2} = I_{F(RMS)} \cdot (\sqrt{2}/\delta)$$

$$\Delta V_F < \frac{\Delta V_{F1} + \Delta V_{F2} + \Delta V_{F3} - \Delta V_{F4}}{\Delta}$$

With

$$\Delta V_{F1} = (r_T \min + rd \min) \cdot I_M - (r_T \max + rd \max) \cdot I_M'$$

$$\Delta V_{F2} = R_{th(j-c) \max} (\alpha_{TO} + \alpha_{rd} \cdot I_M) \cdot P_1$$

$$\Delta V_{F3} = (\alpha_{TO} + \alpha_{rd} \cdot I_M) \cdot (T_{C \max} - T_{C \min})$$

$$\Delta V_{F4} = R_{th(j-c) \min} \cdot (\alpha_{TO} + \alpha_{rd} \cdot I_M') \cdot P_2$$

$$\Delta = 1 + R_{th(j-c) \min} [\alpha_{TO} + rd \cdot I_M'] (\delta/\pi) \cdot I_M'$$

$$P_1 = \frac{2 V_{TO} (\delta/\pi) \cdot I_M + rd \min (\delta/3) \cdot I_M^2}{\rho}$$

$$P_2 = \frac{2 V_{TO} (\delta/\pi) \cdot I_M' + rd \max (\delta/3) \cdot I_M'^2}{\rho}$$

$$I_M' = \frac{I_T - I_M}{n - 1}$$

NEW HIGH VOLTAGE ULTRA-FAST DIODES : THE TURBOSWITCH™ A and B SERIES

B. Rivet

In today's power converter, the commutation speed of the transistor and the operating frequencies are higher and higher.

Fast diodes used for freewheel, snubber, and rectifier functions become one of the main causes of the power losses. In the range of 600V-1200V, SGS THOMSON has developed a new family of ultrafast diodes.

Taking into account these new constraints which are different from one application to another, SGS-THOMSON proposes two series : TURBOSWITCH "A" and TURBOSWITCH "B".

The specific characteristics of these two series offer to the designer a double choice, allowing him to use the best diode in this application.

I. INTRODUCTION

The choice of the optimum diode for a given application depends on the estimation of the power losses generated by the diode. This note explains how to calculate the different losses with information given in the datasheet and shows the difference between TURBOSWITCH "A" and TURBOSWITCH "B" and their respective advantages.

II. LOSSES CALCULATION

II.1 Conduction losses

Conduction losses are estimated with the classical formula :

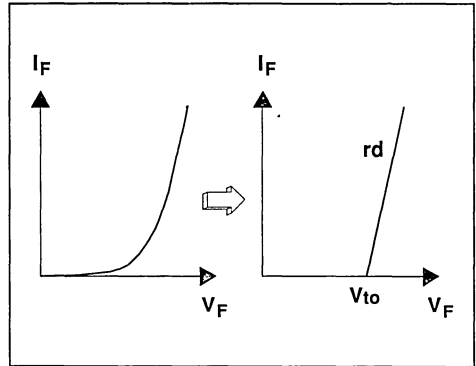
$$P_{con} = V_{to} I_{F(AV)} + rd I_{F(RMS)}^2$$

- V_{to} : Threshold voltage (Fig.1)
- rd : Dynamical resistance (Fig.1)
- $I_{F(AV)}$: Average current
- $I_{F(RMS)}$: RMS current

TM : TURBOSWITCH is a trademark of
SGS-THOMSON Microelectronics

AN601/0193

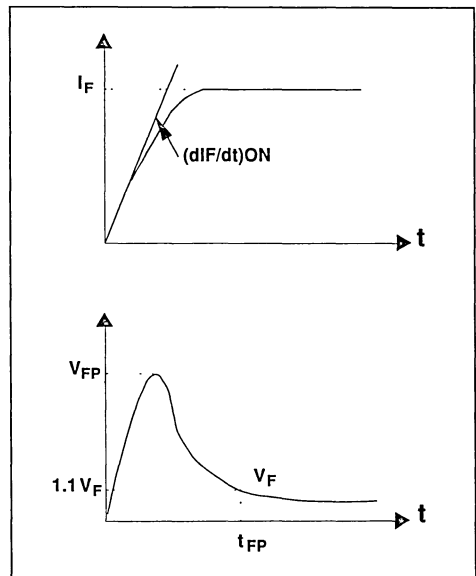
Fig.1 : Approximation of the forward characteristic



II.2. Turn on losses

When the diode turns ON, the voltage across the diode increases to V_{FP} (Peak forward voltage) before it decreases to $1.1 V_F$ at the time t_{rF} (Forward recovery time) (Fig.2).

Fig.2 : Turn ON waveforms



APPLICATION NOTE

Turn ON losses can be approximated by the following formula :

$$P_{on} = 0.4 (V_{FP} - V_F) \times t_{FR} \times I_F \times f$$

Where f is the operating frequency :

V_{FP} and t_{FR} depend on $(di_F/dt)_{ON}$ and I_F . Curves in the datasheet giving V_{FP} and t_{FR} versus $(di_F/dt)_{ON}$ allow the estimation of P_{on} for each application.

Example :

- I_F = 8A
- $(di_F/dt)_{ON}$ = 64A/ μ s
- f = 100 kHz

With an STTA806D (TURBOSWITCH A, 8 A / 600 V / TO220AC)

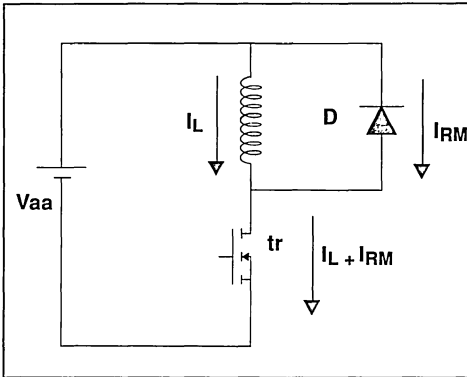
in these conditions

- $V_{FP(max)}$ = 10V
- $t_{FR(max)}$ = 500ns
- P_{on} = 1.4 W

II.3. Turn-on losses

Turn-off losses are studied in the case of a freewheel function where the switch is a MOS transistor (Fig.3).

Fig.3 : Basic circuit with freewheel diode

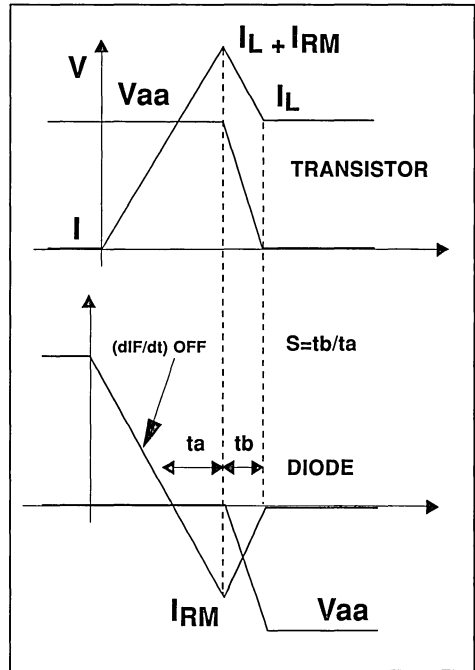


I_L = Load current

I_{RM} = Maximum reverse recovery current of the freewheel diode D

The typical waveform of the current and the voltage when the transistor switches ON and the diode switches OFF is shown in Fig.4 in the case where the stray inductance is low (< 50 nH).

Fig.4 : Current and voltage waveforms of a freewheel diode at turn-OFF and the associated transistor at turn-ON



The turn-OFF losses in the diode can be calculated by :

$$P_{OFF} = \frac{V_{aa} \cdot I_{RM}^2 \cdot S \cdot f}{6 (di_F/dt)_{OFF}}$$

II.4. Transistor losses due to the diode

When the diode switches OFF, the recovery current flows in the transistor which induces turn-ON losses in the transistor. The turn-ON losses in the transistor due to the diode can be estimated by :

$$P_{ON}(tr) = \frac{V_{aa} \cdot I_{RM}^2 (3+2S) f}{6 (di_F/dt)_{OFF}} + \frac{V_{aa} \cdot I_{RM} \cdot I_L (S+2) f}{2 (di_F/dt)_{OFF}}$$

Turn-ON losses in the transistor are generally much higher than turn-OFF losses in the diode.

These two formulas include I_{RM} and S parameters which characterize the turn ON behaviour. These parameters depend on the $(di_F/dt)_{OFF}$.

In the datasheet, curves giving I_{RM} and S versus $(di/dt)_{OFF}$ allow to calculate these losses for a given application.

Example :

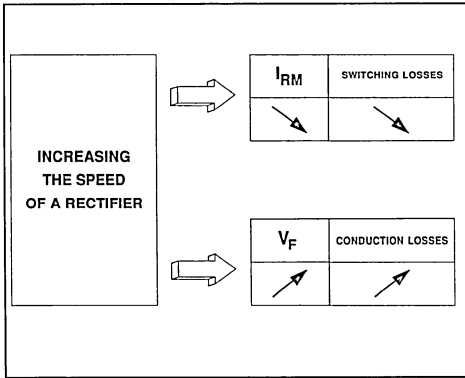
$V_{aa} = 400V$
 $f = 30\text{ kHz}$
 $I_L = 12\text{ A}$
 $(di/dt)_{OFF} = -500A/\mu s$
 $T_j = 125^\circ C$
 with a STTA12060
 (TURBOSWITCH"A", 12 A / 600 V / TO220AC)
 we find :
 $P_{off} = 0.43\text{ W}$
 $P_{on(tr)} = 9.5\text{ W}$

III. COMPARISON BETWEEN TURBOSWITCH "A" AND TURBOSWITCH "B"

III.1. Difference between characteristics

The design of a fast rectifier is known to be the result of a trade-off for a given reverse voltage, and the compromise can be explained in the fig.5.

Fig.5 : Compromise between I_{RM} and V_F for a given reverse voltage



For the diode of the family "A", the compromise $V_F - I_{RM}$ has been chosen to reduce the total losses in both the diode and the companion transistor in a freewheel configuration.

On the other hand, the compromise of the family "B" has been chosen to minimize the conduction losses.

Table in Fig.6 summarizes the main characteristics of a STTA806D (TURBOSWITCH"A", 8 A / 600V / TO220AC) and a STTB806D (TURBOSWITCH"B", 8 A / 600V / TO220AC)

Fig.6 : Main characteristics of a STTA806D and a STTB806D

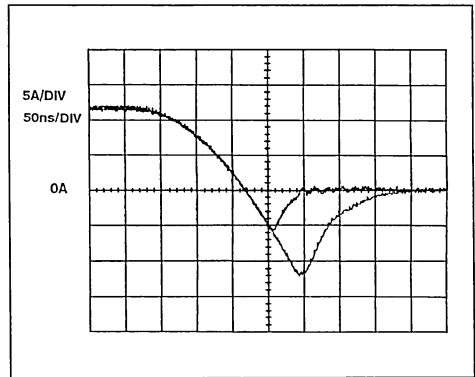
TYPE	$(di/dt)_{OFF} = 500\text{ A}/\mu s$ $I_F = 8A$ $T_j = 125^\circ C$		$I_F = 8A$ $T_j = 125^\circ C$		$(di/dt)_{ON} = 64\text{ A}/\mu s$ $T_j = 25^\circ C$	
	I_{RM}	S	V_F	V_{FP}	t_{FR}	
	typ	typ	max	max	max	
STTA806D	14 A	0.45	1.5 V	10 V	500 ns	
STTB806D	28 A	0.79	1.3 V	8 V	500 ns	

Data in this table show that conduction losses and switch-ON losses will be lower in a TURBOSWITCH "B" while switch-OFF losses will be lower in a TURBOSWICH "A".

The oscillogram in Fig.7 shows the current in a STTA806D and in a STTB806D when the diodes switch-OFF in the following conditions :

$V_R = 350V$
 $(di/dt)_{OFF} = -300\text{ A}/\mu s$
 $T_j = 100^\circ C$
 $I_F = 12\text{ A}$

Fig.7 : Switch-OFF oscillogram of STTA806D and STTB806D



This oscillogram shows that the I_{RM} value is approximately two times lower with a STTA1206D, and that STTB1206D is a very soft diode.

III.2. Application examples

Example 1 : In this example, a comparison of the loss differences is done in a freewheel application where the current in the diode is rectangular. The main parameters are :

Peak current
 $I_M = 12\text{ A}$
 $V_{aa} = 400\text{ V}$

Duty cycle: $\delta = 0.6$
 $(di_F/dt)_{ON} = 200 \text{ A}/\mu\text{s}$
 $(di_F/dt)_{OFF} = 500 \text{ A}/\mu\text{s}$
 $T_j = 125^\circ\text{C}$
 $f = 30 \text{ kHz}$

In these conditions the reverse recovery characteristics of the diodes are given in fig.7 :

The losses of the table fig.8 are calculated by

Fig.7 : Reverse recovery characteristics of STTA1206D and STTB1206D with the conditions of the example 1

TYPE	I_{RM}	S
STTA1206D	16 A	0.42
STTB1206D	30 A	0.90

using relations given in part 2.

In this type of application, the TURBOSWITCH "A"

Fig.8 : Comparison between STTB1206D and STTA1206D in a freewheel diode function

TYPE	Conduction losses	Switch ON losses	Switch OFF losses	Transistor losses	Total losses
STTA1206D	9 W	0.1 W	0.43 W	9.5 W	19 W
STTB1206D	7.8 W	0.07 W	3.2 W	29.8 W	40.9 W

is obviously the better choice.

Example 2 : In this example, the diode is used as a rectifier diode with the following conditions :

$I_F = 12 \text{ A}$
 $(di_F/dt)_{ON} = (di_F/dt)_{OFF} = 100 \text{ A}/\mu\text{s}$
 $V_{aa} = 350 \text{ V}$
 $T_j = 125^\circ\text{C}$
 $\delta = 0.8$
 $f = 20 \text{ kHz}$

The estimated losses are summarized in the table fig.9

Fig.9 : Comparison between STTA1206D and STTB1206D in a rectifier function

TYPE	Conduction losses	Switch ON losses	Switch OFF losses	Total losses
STTA1206D	14.4 W	negligible	0.2 W	14.6 W
STTB1206D	12.4 W	negligible	1 W	13.4 W

In this application, we have to take into account the leakage inductance and the fact that a very soft diode is required to limit the overvoltage. The total losses are 10% lower with the STTB1206D, therefore the TURBOSWITCH "B" is the best choice.

IV. CONCLUSION

This note shows how to calculate the different losses due to the diodes in basic power switching circuits. These calculations can be done by using the parameters given in the datasheet of the TURBOSWITCH "A" and the TURBOSWITCH "B".

In most of cases, it is easy to choose between the "A" type and the "B" type.

The "A" type is very efficient in freewheel diode applications with high frequencies ($f > 10 \text{ kHz}$). The "B" type is better when conduction losses are predominant like in the case of the power factor corrector circuit in discontinuous mode (low $(di_F/dt)_{OFF}$), or for applications where very high soft recovery behaviour is required (commutation with series inductances, for example).

TURBOSWITCH™ IN A PFC BOOST CONVERTER

B. Rivet

1.INTRODUCTION

SGS-THOMSON offers two families of 600V ultrafast diodes (TURBOSWITCH™A" and "B") having different compromises between the forward characteristics and the reverse recovery characteristics.

This paper explains why TURBOSWITCH™B" is a suitable family for PFC boost converters working in discontinuous mode, and why the TURBOSWITCH™A" should be used for PFC's working in continuous mode.

In this kind of application, the main concern for the designer is to evaluate the power losses. For that, SGS-THOMSON proposes a very powerful tool. A program has been developed in order to calculate the losses in the diode and in the transistor in a PFC working in continuous mode at a constant frequency. This application note describes how the calculations are performed. This software determines clearly that there is an optimum MOSFET turn on di/dt to increase the efficiency of the design and reduce EMI.

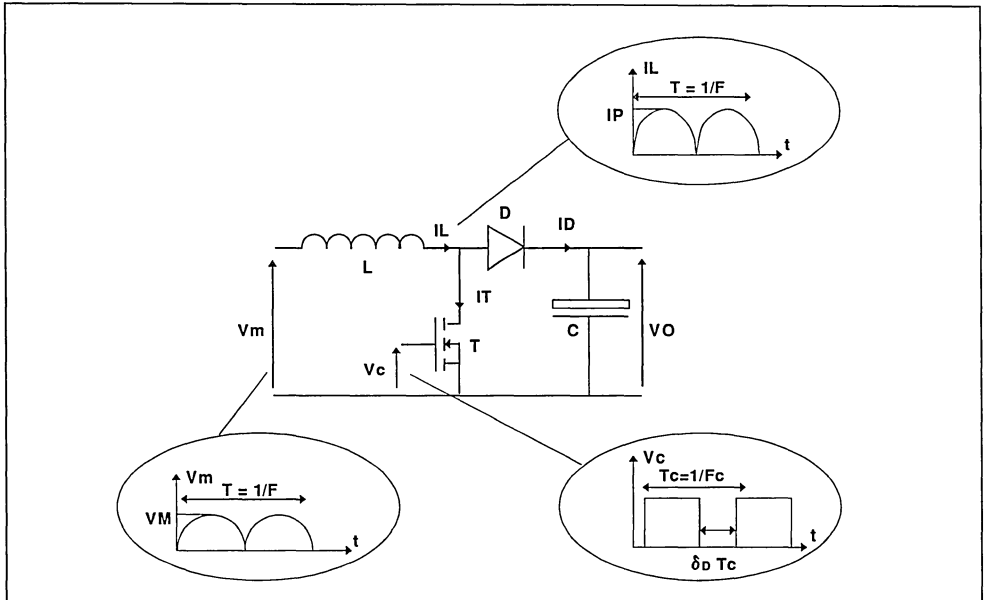
Fig.1 : Boost PFC converter notations

2.PARAMETERS DEFINITION

The basic circuit of the fig.1 shows the current, voltage and frequencies notations used in this paper.

List of the parameters :

- V_m : mains voltage
- V_M : peak value of the mains voltage
- I_L : current in the coil
- I_D : current in the diode
- I_T : current in the transistor
- I_P : peak current in the coil
- δ_D : duty cycle of the diode
- F_c : switching frequency
- V_o : output voltage
- F : mains frequency



3. TURBOSWITCH IN A PFC BOOST CONVERTER WORKING IN DISCONTINUOUS MODE

The discontinuous mode is used for power below 200-300W. In this mode, the current in the diode before reaching zero A decreases very slowly (less than 1A/μs). The slope is fixed by the coil and is equal to $(V_m - V_o)/L$. The low value of this slope generates low values of reverse recovery current (I_{RM}) and therefore low switch-off losses. For this reason the forward voltage (V_F) of the diode becomes the most important parameter. The best choice is to use a TURBOSWITCH" B" 1-2A/600V.

The major part of the losses is the conduction losses (P_{cond}). They can be calculated with a good approximation by :

$$P_{cond} = V_F (I_{F(AV)}) \times I_{F(AV)}$$

The average current in the diode is equal to the output power (P_{OUT}) divided by the output voltage V_o :

$$I_{F(AV)} = P_{OUT} / V_o$$

4. TURBOSWITCH IN PFC BOOST CONVERTER WORKING IN CONTINUOUS MODE

In continuous mode (output power higher than 200-300W) the current in the diode decreases very quickly. The $(di_F/dt)_{OFF}$ of the diode is fixed by the MOS transistor control and is equal to a few hundred A/μs ($(di_F/dt)_{OFF}$ of the diode is equal to the $(di_F/dt)_{ON}$ of the transistor).

The reverse recovery current of the diode when the transistor switches on flows in the transistor and generates high turn-on losses in the transistor. For this reason the most important parameter of the diode is the I_{RM} .

The TURBOSWITCH "A" family represents the optimum in term of V_F/I_{RM} compromise for this type of application and is recommended.

The calculations of the average current, RMS current and power losses in the diode and in the transistor are very complex. This is why SGS-THOMSON has developed a software which performs calculations and proposes the best TURBOSWITCH for the application. The boost converter is assumed to work in a continuous mode and at a constant frequency. This development tool, the PFC diskette, is available in a 5 1/4 inches format. The following paragraph explains how the calculations are performed.

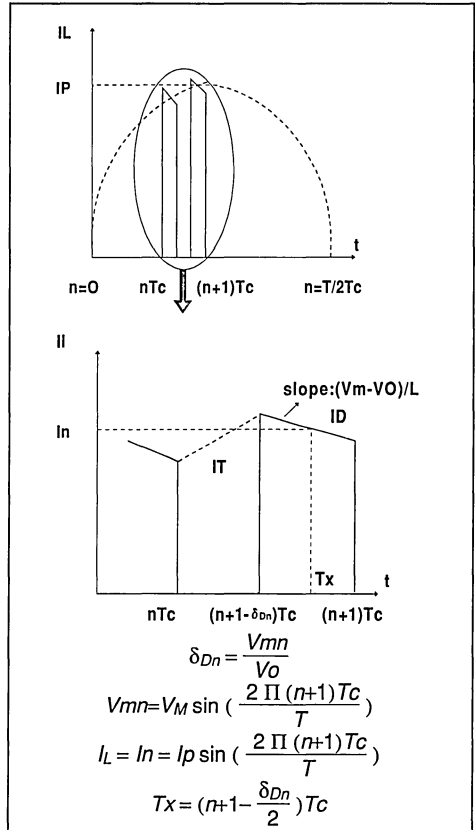
4.1. Results concerning the diode

4.1.1. Conduction losses

The current waveform in the diode is a succession of trapezoids. The duty cycle δ_{Dn} and the amplitude of the latter are varying as a function of the input mains voltage.

The fig.2 shows the current in the diode between the time nTc and $(n+1)Tc$.

Fig.2 : Current in the diode between nTc and $(n+1)Tc$



Average current and RMS current in the diode

The program calculates the average and RMS current in the diode with the iterative formulae :

$$I_{D(AV)} = \frac{2}{T} \sum_{n=0}^{N-1} \left[\frac{A}{2} Tc^2 \delta_{Dn} (2n+2-\delta_{Dn}) + BTc\delta_{Dn} \right]$$

$$I_{D(RMS)} = \left[\frac{2}{T} \sum_{n=0}^{N-1} (Cn + Dn) \right]^{1/2}$$

with :

$$A = \frac{V_{mn} - V_o}{L}$$

$$N = \frac{T}{2Tc}$$

$$B = \ln - A \left(n + 1 - \frac{\delta_{Dn}}{2} \right) Tc$$

$$Cn = \frac{A^2}{3} Tc^3 \delta_{Dn} [3(n(n+2 - \delta_{Dn}) + 1 - \delta_{Dn}) + \delta_{Dn}^2]$$

$$Dn = AB Tc^2 \delta_{Dn} (2n + 2 - \delta_{Dn}) + B^2 Tc \delta_{Dn}$$

Conduction losses in the diode

The conduction losses in the diode are calculated with the maximum value of V_{TO} and R_d (respectively the threshold voltage and the dynamic resistance of the forward characteristic). It must be pointed out that these power losses correspond to a worst case situation.

$$P_{cond} = V_{TO} I_{D(AV)} + R_d I_{D(RMS)}^2$$

4.1.2. Turn-on losses in the diode

These losses are estimated with the formula

$$P_{ON} = 0.4 (V_{FP} - V_F) I_F \cdot t_{FR} \cdot F$$

V_{FP} : Peak forward voltage

t_{FR} : forward recovery time

This formula provides only an estimate, which is sufficient because turn ON losses are low with regard to conduction losses. The program interpolates data of the curve V_{FP} and t_{FR} versus $(di/dt)_{ON}$ of the diode (Fig 3). These data have been stored on the disk for each part number.

Fig.3 : V_{FP} versus di/dt .

(STTA806D)

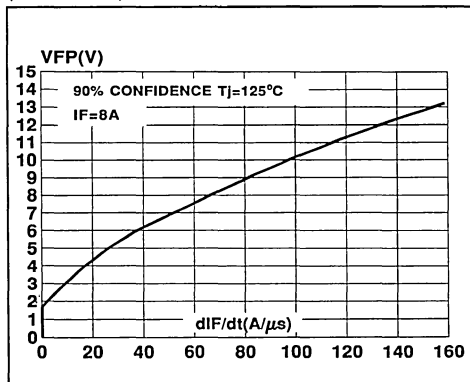
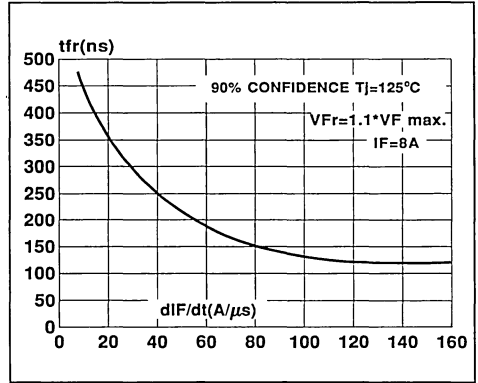


Fig.3 Bis : t_{FR} versus di/dt .

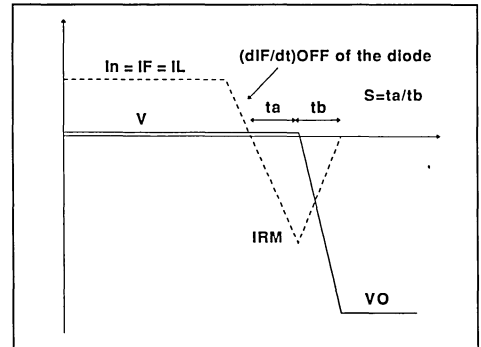
(STTA806D)



4.1.3. Turn-off losses in the diode

The fig.4 shows the theoretical waveform of the current and the voltage when the diode switches off.

Fig.4 : Current and voltage waveform during diodes switch OFF



In a PFC working in a continuous mode, the $(di/dt)_{OFF}$ of the diode is fixed. But current ($I_F = I_L$) acts as a function of the time, as do the softness factors and the current I_{RM} (Fig.5).

These data were also stored for each individual part number.

$$P_{OFF} = \frac{1}{T} \sum_{n=0}^{N-1} \frac{V_o I_{RMn}^2 S_n}{3 (di/dt)_{OFF}}$$

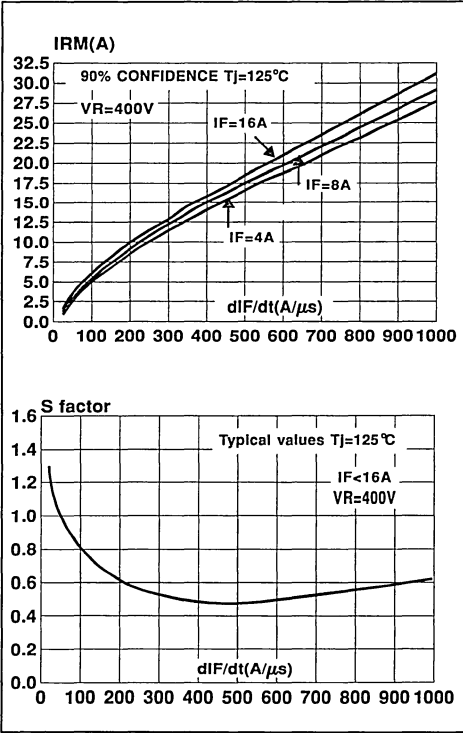
I_{RMn} and S_n are respectively the reverse current and softness factor corresponding to the $(di/dt)_{OFF}$ of the application and at the time nTc when

APPLICATION NOTE

$$I_F = I_n I_p \left(\sin \frac{2 \Pi (n+1) T_c}{T} \right)$$

These losses are calculated with data (S, I_{RM}) at 90% confidence.

Fig.5 : I_{RM} and S versus diF/dt. (STTA806D)



4.1.4. Turn-on losses in the transistor due to the diode

When the transistor turns on the reverse recovery current flows in the transistor (Fig.6)

Turn-on losses in the transistor due to the diode are calculated with the same data as the turn-off losses in the diode.

The formula used is :

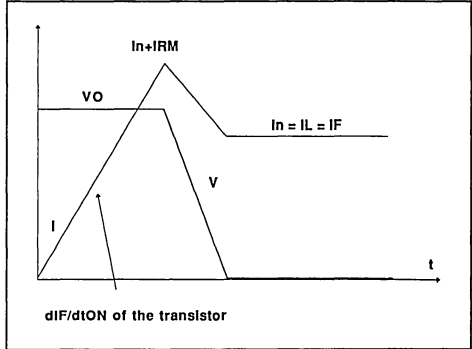
$$P_{ON} = 2 \frac{V_0}{T} \sum_{n=0}^{N-1} (Mn + Gn)$$

with :

$$Mn = \frac{I_{RMn}^2 (3 + 2 Sn)}{6 (diF/dt)_{OFF}}$$

$$Gn = \frac{In I_{RMn} (2 + Sn)}{2 (diF/dt)_{OFF}}$$

Fig.6 : Current and voltage waveform during transistor turn-on.

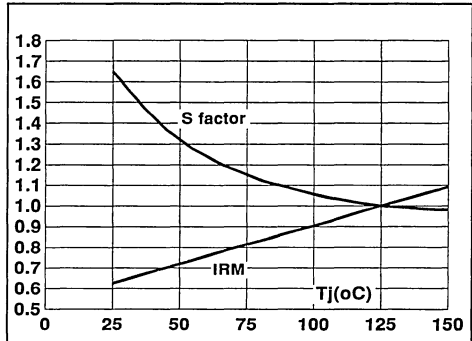


4.1.5. Junction temperature of the diode

S factor and I_{RM} depend on the temperature (Fig.7). This program takes into account these variations to calculate the junction temperature. Two options are available :

Enter Tcase (case temperature) or, Enter Tamb (ambient temperature) and Rth (c-a) (case ambient thermal resistance).

Fig 7 : Relative variation of dynamic parameters versus junction temperature (STTA806D)

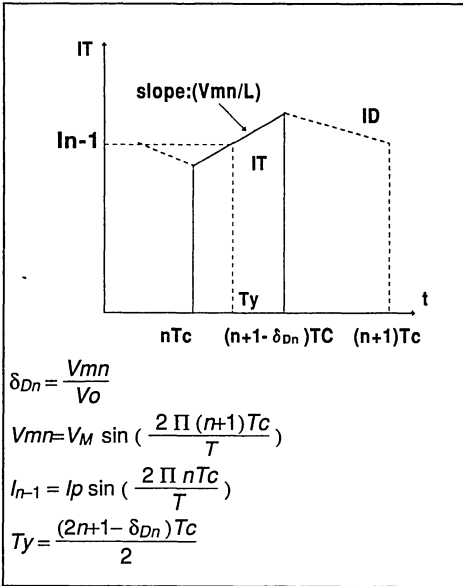


4.2. Results concerning the transistor

4.2.1. Conduction losses

The current waveform in the transistor is also a succession of N trapezoids and the duty cycle of the transistor, and the amplitude of which varies as a function of the input main voltage. Fig.8 shows the current in the transistor between the time nT_c and (n+1)T_c.

Fig.8 : Current in the transistor between T_c and $(n+1)T_c$



The program calculates the average and RMS current in the transistor with the formulae.

$$I_{T(AV)} = \frac{2}{T} \sum_{n=0}^{N-1} \left[\frac{A((n+1-\delta_{Dn})^2 - n^2) T_c^2}{2} + Ln \right]$$

$$I_{T(RMS)} = \left[\frac{2}{T} \sum_{n=0}^{N-1} [In + Jn] \right]^{1/2}$$

with :

$$A = \frac{Vmn}{L}$$

$$B = I_{n-1} - A \left(\frac{2n+1-\delta_{Dn}}{2} \right) T_c$$

$$Ln = BT_c(1-\delta_{Dn})$$

$$In = \frac{A^2}{3} T_c^3 ((n+1-\delta_{Dn})^3 - n^3)$$

$$Jn = ABT_c^2 ((n+1-\delta_{Dn})^2 - n^2) + B^2 T_c (1-\delta_{Dn})$$

Conduction losses

We have :

$$P_{cond} = r_{dSON} I_{T(RMS)}^2$$

r_{dSON} : r_{dSON} of the transistor

4.2.2.Total turn-on losses in the transistor

The principle of the calculation is the same as the calculation of turn-off losses in the diode.

The formula used is :

$$P_{ON}(T_R) = \frac{2V_o}{T} \sum_{n=0}^{N-1} [Kn / (di_F/dt)_{OFF}]$$

with :

$$Kn = \frac{(In + I_{RMn})^2}{2} + Sn \frac{I_{RMn}^2}{3} + Sn \frac{I_{RMn} I_n}{2}$$

5. EXAMPLE OF SIMULATION

Data entered in the software :

Diode : STTA2006P

$(di_F/dt)_{OFF}$ of the diode = 500A/ μ s

$(di/dt)_{ON}$ of the diode = 500A/ μ s

- F = 50Hz
- Fc = 50 000HZ
- VM = 300V
- VO = 400V
- L = 100 μ H
- Ip = 20A
- RdSON = 0.1 Ω
- Tcase = 60°C

Results

Diode results

- ID(AV) = 7.5A
- ID(RMS) = 11.8A
- PON = 0.5W
- POFF = 1W
- Pcond = 11W
- Tj = 76°C
- PON TR(D) = 18.6W

Transistor results

- IT(AV) = 5.2A
- IT(RMS) = 9.1A
- PON(TR) = 22.6W
- Pcond(TR) = 8.3W

6. OPTIMUM MOSFET TURN ON di/dt

P_{OFF} in the diode and $P_{ON(Tr)}$ are the only losses depending on the $(di/dt)_{ON}$ of the transistor ((di/dt) of the diode).

The software allows you to draw the curve $P_{ON(Tr)} + P_{OFF(D)}$ versus the $(di/dt)_{ON}$ of the transistor ($(di/dt)_{OFF}$ of the diode).

Example :

The curve fig.9 shows the variation of $P_{OFF(D)} + P_{ON(Tr)}$ versus the $(di/dt)_{OFF}$ of the diodes. We enter in the program the following data :

Diode : STTA2006P

- F = 50Hz
- F_C = 50kHz
- V_M = 300V
- V_O = 400V
- L = 100 μ H
- T_C = 80°C
- I_p = 12A

This curve shows that in order to optimize the efficiency, the designer has to fix the $(di/dt)_{ON}$ of the transistor at 500A/ μ s. When the switching time decreases in the area of $di/dt < 500A/\mu s$, $P_{OFF} + P_{ON(Tr)}$ decreases. But for $di/dt > 500A/\mu s$, the increasing of I_{RM} takes over the influence of the switching time and $P_{OFF} + P_{ON(Tr)}$ increases.

The reverse recovery of the diode produces EMI that increases with the di/dt . In this application the

best compromise to reduce the noise and have the best efficiency is to fix $di_F/dt \approx 350A/\mu s$ ($P_{OFF(D)} + P_{ON(Tr)}$) at 350A/ $\mu s \approx (P_{OFF(D)} + P_{ON(Tr)})$ at 500A/ μs .

Another way to reduce EMI produced by the diode is to overdimension the diode. Indeed the noise generated by the diode decreases as a function of the junction temperature.

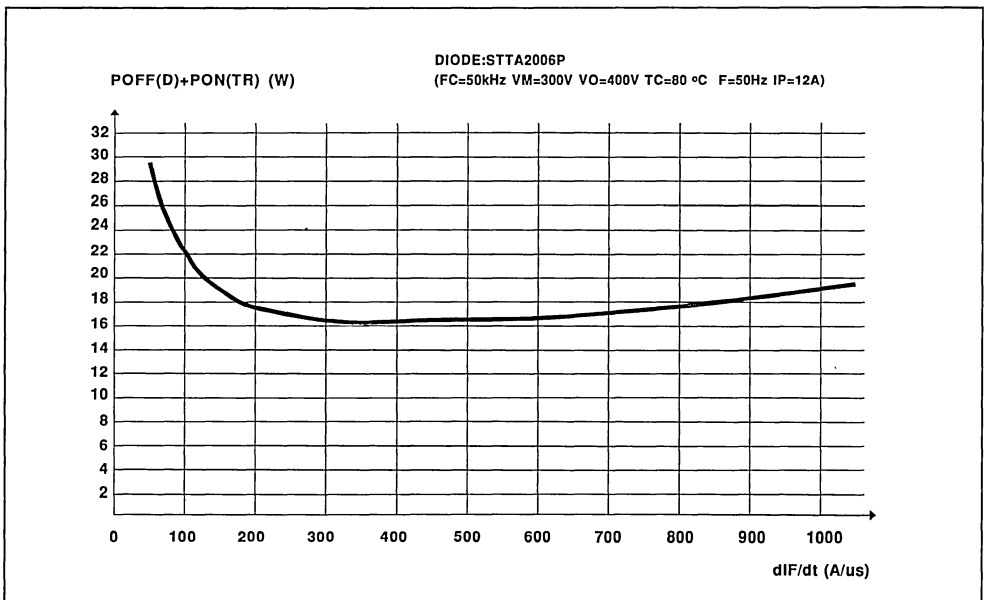
7. CONCLUSION

This paper explains why TURBOSWITCH"A" and TURBOSWITCH"B" are the right choices of diodes respectively for PFC working in continuous and discontinuous mode.

The software described in the application note is now available. It can help the designer to evaluate the influence of the different parameters (switching frequency, coil, $(di/dt)_{ON}$ of the transistor ...) on the power losses in the diode and in the transistor.

This program is especially interesting to determine the optimum $(di/dt)_{ON}$ of the transistor. This will increase the efficiency of the converter and decrease noise.

Fig.8 : OFF losses (D) + ON losses (TR) versus $(di_F/dt)_{ON}$ of the transistor .



MODELLING PARALLEL OPERATION OF POWER RECTIFIERS WITH PSPICE

B. Rivet

I - INTRODUCTION

The behaviour of semiconductor components is always linked with the junction temperature.

This is the case, for example, in current-sharing between diodes connected in parallel. The current in each diode depends on the forward characteristic but also on the junction temperature.

This study describes thermal and electrical modelling of diodes connected in parallel. It allows the variation in current and junction temperature of each diode to be visualized between turn on and the equilibrium state.

II - ELECTRICAL AND THERMAL MODELLING OF A DIODE

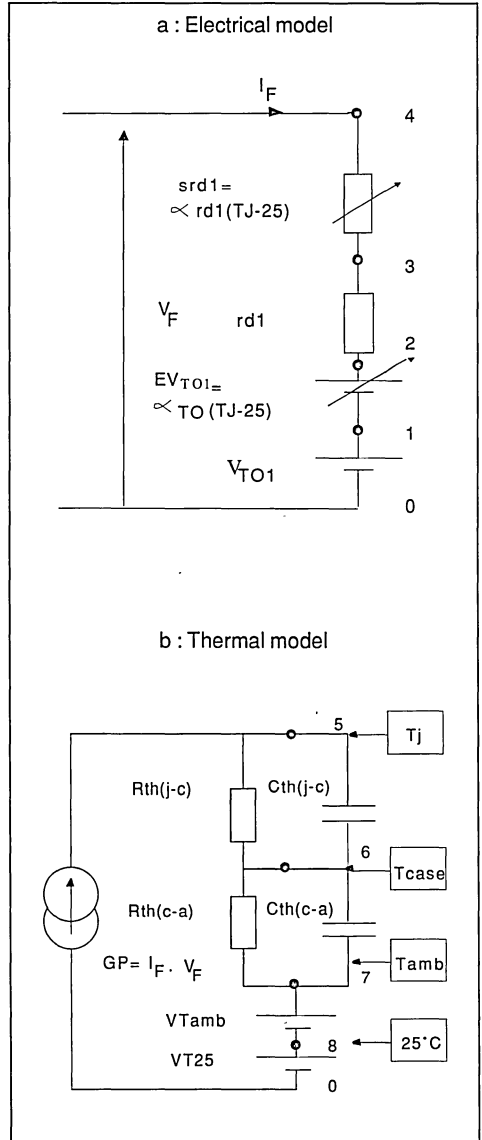
The forward characteristic of a diode is modelled by a threshold voltage V_{T0} in series with a dynamic resistance rd . These two parameters depend on the junction temperature of the diodes. V_{T0} has a negative temperature coefficient $\propto -T_0$ and rd have a positive temperature coefficient $\propto rd$.

One way to simulate the operation of such a device is to split the model into 2 different circuits : one "electrical" model and one "thermal" model.

The electrical and thermal models of a diode are shown in fig.1.

The thermal model is represented by electrical components.

Fig.1 : Electrical and thermal models of a diode



APPLICATION NOTE

THE ELECTRICAL PARAMETERS ARE :

- V_{T01} : Threshold voltage at $T_j = 25^\circ\text{C}$
- EV_{T01} : Threshold voltage versus junction temperature
- $EV_{T01} = \infty T_O (T_j - T_{amb})$
 $= \infty T_O (V(5) - V(8))$
- $rd1$: Dynamic resistance at $T_j = 25^\circ\text{C}$
- $srd1$: Dynamic resistance versus temperature
 $srd1 = \infty rd1 (T_j - T_{amb})$
 $= \infty rd1 (V(5) - V(8))$
- V_F : Instantaneous forward voltage across the diode
- I_F : Instantaneous forward current in the diode

THE THERMAL PARAMETERS ARE :

- GP : Generator current representing the instantaneous power dissipated in the diode.
 $GP = V_F \times I_F$
- $R_{th(j-c)}$: Resistor representing the junction to case thermal resistance
- $C_{th(j-c)}$: Capacitor representing the junction to case thermal capacitance
- $R_{th(c-a)}$: Resistor representing the case to ambient thermal capacitance
- $C_{th(c-a)}$: Capacitor representing the case to ambient thermal capacitance
- V_{Tamb} : Voltage generator representing the ambient temperature
 $V_{Tamb} = T_{amb} - 25^\circ\text{C}$
- V_{T25} : Voltage generator representing the 25°C temperature

III - MODELLING OF SEVERAL DIODES IN PARALLEL

See the application note : "Parallel operation of power rectifiers" (B.RIVET) for the qualitative analysis. In this note the acceptable difference between forward voltage drops (ΔV_F) is calculated so that the diodes can be safely connected in parallel.

The modelling will be based on the worst case situation. Suppose D1 has the lowest V_{T0} and rd and the highest $R_{th(j-c)}$ so that this diode supports the highest current. The diode D2 and D3 have the same characteristics (maximum V_{T0} and rd , minimum $R_{th(j-c)}$).

The electrical and thermal models are shown in Fig.2.

Fig.2a : Thermal model of 3 rectifiers in parallel

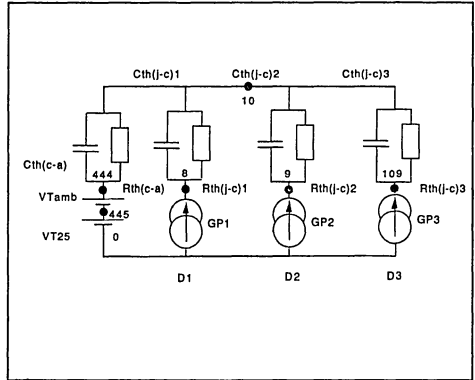
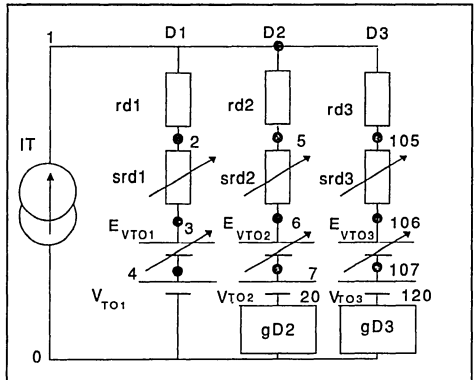


Fig.2b : Electrical model of 3 rectifiers in parallel



The modelling of several diodes in parallel will be treated with an example. Consider three BYV255 in parallel. The total current I_T is rectangular with a duty cycle equal to 0.5, a peak current of 300 A and a frequency of 100 Hz.

In this example the following values have been taken.

$$rd1 = 1.2 \text{ m}\Omega$$

$$rd2 = rd3 = 0.9 \text{ m}\Omega$$

$$V_{T01} = 0.82 \text{ V}$$

$$\infty T_O = -1.6 \times 10^{-3} \text{ V}/^\circ\text{C}$$

$$\infty rd = 2.10^{-6} \Omega/^\circ\text{C}$$

$$R_{th(j-c)1} = 0.4^\circ\text{C}/\text{W}$$

$$R_{th(j-c)2} = R_{th(j-c)3} = 0.3^\circ\text{C}/\text{W}$$

Their calculation is explained in the previously mentioned application note.

$C_{th(j-c)1}$, $C_{th(j-c)2}$, $C_{th(j-c)3}$, $C_{th(j-c)}$ are not very important parameters; they influence only the

transient behaviour of the circuit and not the equilibrium state.

In the example $C_{th}(j-c)1 = C_{th}(j-c)2 = C_{th}(j-c)3 = C_{th}(c-a) = 1 \text{ sW/}^\circ\text{C}$ has been assumed.

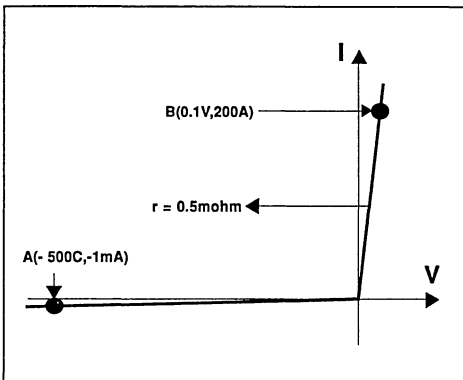
The simulation has been done with $\Delta V_F = 80 \text{ mV}$

Consider

$\Delta V \approx \Delta V_{T0}$ so $V_{T02} = V_{T03} = V_{T01} + \Delta V_F = 0.9 \text{ V}$

In the electrical modelling of the diode D2 and D3, components gD2, gD3 have been added. Their characteristic is drawn in Fig.3

Fig.3 : Characteristic of gD2 and gD3



These auxiliary components are needed to avoid a current flow in the diodes when the current I_T is equal to zero. When the diodes conduct, these components are equivalent to the resistance of $0.5 \text{ m}\Omega$.

To take these resistances into account, make $rd2 = rd3 = 0.4 \text{ m}\Omega$

The PSPICE description of this circuit is given in the appendix.

Fig.4 and 5 show the results of the simulation.

These curves represent the variations of the current in D1 and D2 (fig.4) and the junction temperatures T_{j1} and T_{j2} (fig.5)

At $t = 0 \text{ s}$ $T_{j1} = T_{j2} = T_{amb} = 40^\circ\text{C}$: the current is higher in D1 than in D2 so T_{j1} will increase more quickly than T_{j2} and the difference between I_{F1} and I_{F2} will increase also.

When the equilibrium state is reached this difference becomes constant.

If the frequency and the thermal capacitor are high the simulation time needed to reach the equilibrium state is long. So to reduce this time the C_{th} values can be decreased (This change will affect only the transient behaviour).

IV - CONCLUSION

A very flexible analysis of operation of several rectifiers in parallel can be done easily by using simulation on PSPICE. Because of the importance of the thermal effect on the various parameters of each diode we have design 2 models operating simultaneously. The first circuit calculates the electrical parameters while the second monitors the junction temperature.

One example of calculation with 3 diodes in parallel has shown how the curves of the currents and the junction temperatures can be obtained.

This double model is very powerful. The designer can add other diodes, insert wiring resistance, change the current waveform and also the cooling characteristic of the design.

Fig.4 : Variation of the current in D1 (IRD1) and in D2 (IRD2) versus time

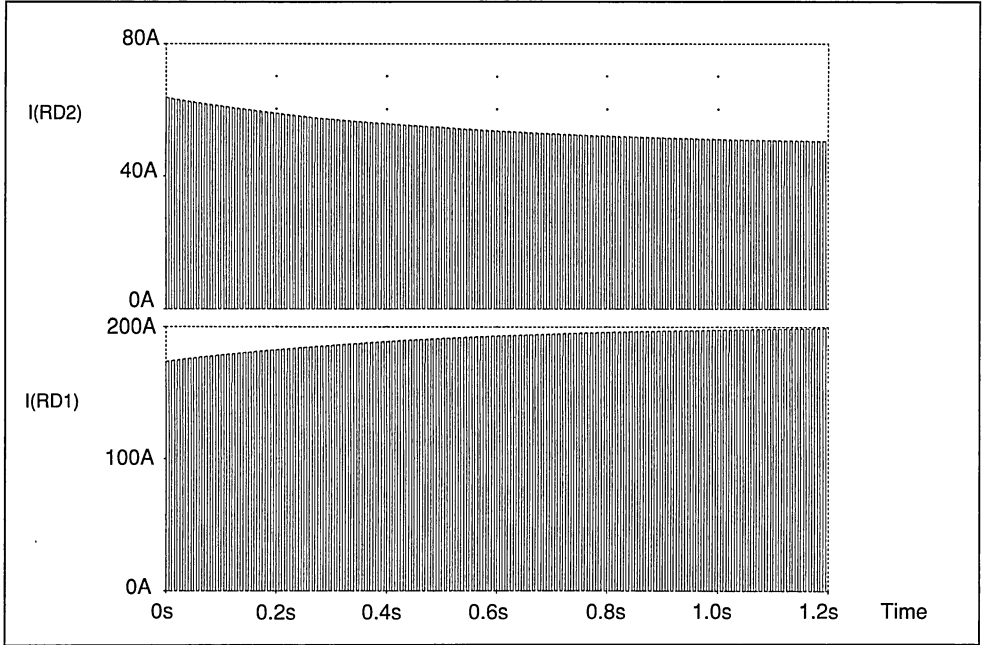
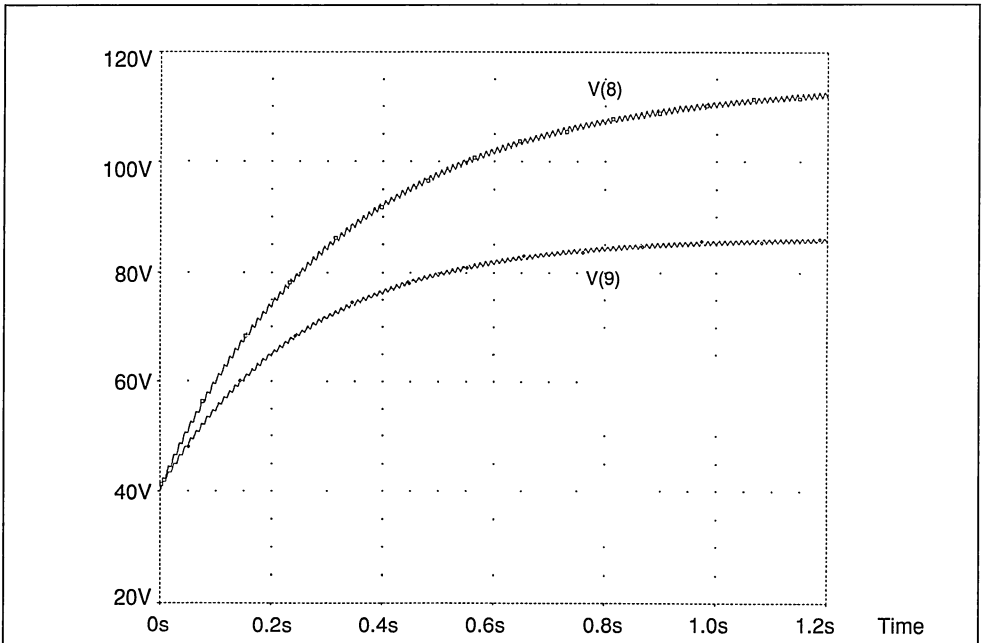


Fig.5 : Variation of the junction temperature of the diode D1 (V(8)) and D2 (V(9)) versus time



APPENDIX

DIODES-PARALLEL

```

I1 1 0 PULSE50 -300 0 0 0 5m 10m)
RD1 1 2 .9m
SRD1 2 3 8 445 SMOD
EVTO1 3 4 VALUE={-0.0016*V(8,445)}
VTO1 4 0 0.82
RD2 1 5 0.7m
SRD2 5 6 9 445 SMOD
EVTO2 6 7 VALUE={-0.0016*V(9,445)}
VTO2 7 20 0.9
GD2 20 0 TABLE {V(20)} =
+ (-500,-0.001) (0,0) (0.1,200)
RD3 1 105 0.7m
SRD3 105 106 109 445 SMOD
EVTO3 106 107 VALUE={-0.0016*V(109,445)}
VTO3 107 120 0.9
GR3 120 0 TABLE {V(120)} =
+ (-500,-0.001) (0,0) (0.1,200)
GP1 8 0 VALUE={-V(1,0)*V(1,2)*1111.11}
RTHJC1 8 10 .4
CTHJC1 8 10 1
GP2 9 0 VALUE={-V(1,0)*V(1,5)*1428.57}
RTHJC2 9 10 .3
CHTJC2 9 10 1
GP3 109 0 VALUE={-V(1,0)*V(1,105)*1428.57}
RTHJC3 109 10 .3
CTHJC3 109 10 1
RTHCA 10 444 .3
CTHCA 10 444 1
VTAMB 444 445 15
VT25 445 0 25
MODEL SMOD VSWITCH
(ROn=0.0006 ROFF=0.00001 VON=250
VOFF=25)
tran 100.000u 1.2 0 0 ;*ipsp*
END

```


**DRIVE, CONTROL and PROTECTION
DRIVES**

INFLUENCE OF GATE AND BASE DRIVE ON POWER SWITCH BEHAVIOUR

by P. Fichera

ABSTRACT

This paper looks at the influence of the drive circuit on the switching behaviour of electronic devices belonging to different families. In particular Bipolar Junction Transistors (BJT) are considered as a representative of current driven devices, and Power MOSFETs and IGBTs as representatives of voltage driven devices.

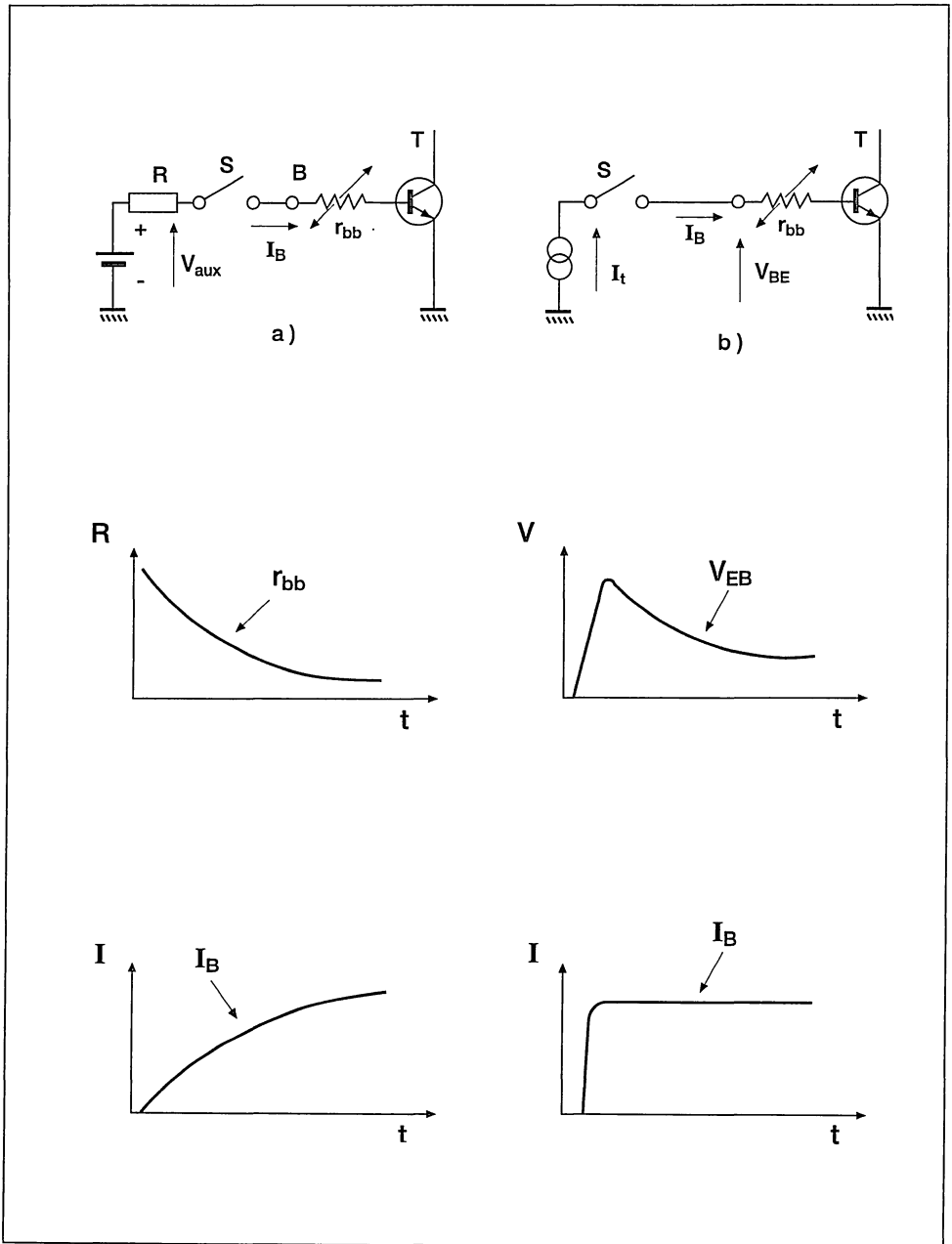
1. BJT

In order to switch a BJT quickly and with low switching losses, minority carriers must be injected into and extracted from the base of the transistor very rapidly.

1.1 Turn-On Switching

In terms of input signal, the transistor base-emitter junction can be schematically represented by a variable resistance r_{bb} and a voltage source. When the base-emitter junction is cut-off the r_{bb} value is relatively high. When carrier injection begins, r_{bb} is modulated and its value decreases in a time which is of the order of the carrier lifetime (a few tenths of a nanosecond). If the transistor is driven from a current source, the rate of rise of the base current is imposed by the driver stage and the initial high value of r_{bb} does not influence the rate of rise of the collector current (see fig. 1).

Figure 1: Rate of rise of positive base current when the driver circuit acts as:
 a) a voltage source
 b) a current source



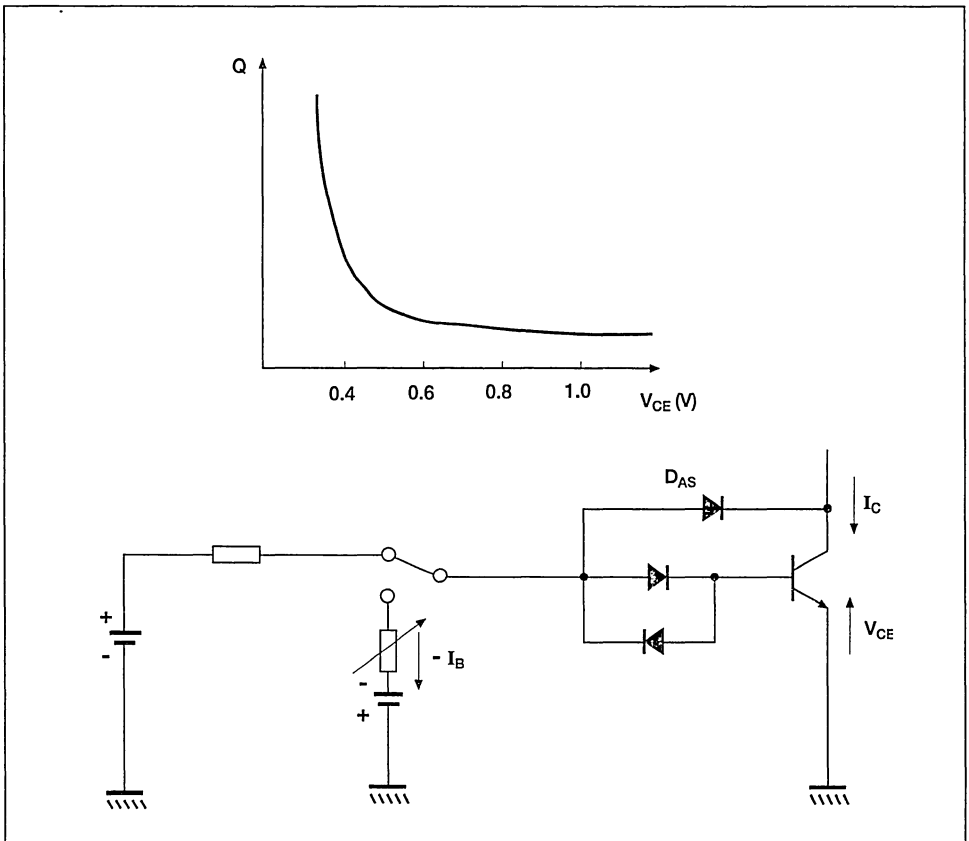
1.2 On-state

Once the transistor is turned on, the driver stage has to provide a positive base current in such a way as to prevent the device entering an over-saturated state. This state corresponds to very low $V_{CE(sat)}$ (low conduction losses), but the collector region is fully saturated by the minority carriers injected from the base. Consequently the advantage of the low voltage drop is offset by a longer turn-off switching time.

Over-saturation can be avoided if the drive is able to supply a base current proportional to the collector current in such a way as to keep the ratio of I_C/I_B constant; however this requires a complex driver. The use of an anti-saturation network can avoid the collector-emitter voltage falling below than 0.6-0.7 Volts, and hence can keep the transistor operating point outside the deeply saturated region; see fig. 2.

Figure 2: Transistor in the on - state

- stored charge Q is very large if the V_{ce} is very small
- an anti - saturation circuit avoids the V_{ce} being lower than 0.6 - 0.7 Volts

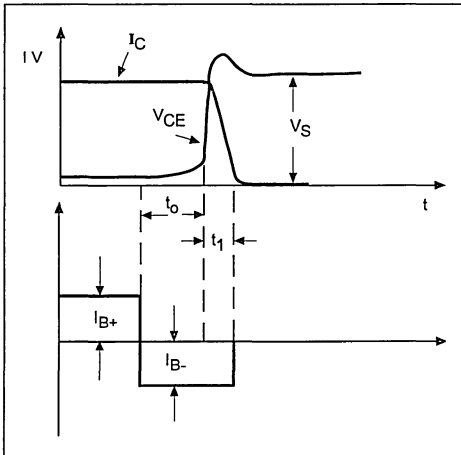


1.3 Turn-Off Switching

The transistor behaviour during this phase essentially depends upon the following parameters:

- a. the negative base current or extraction current I_{b-} (see fig. 3)
- b. the saturation state of the transistor during the previous conduction phase.

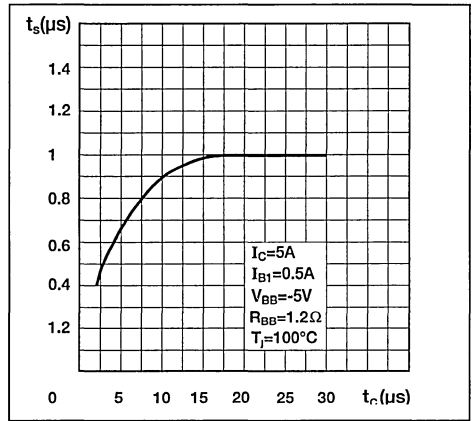
Figure 3: Schematic behaviour of the base current at turn - off



The quantity of charge the driver stage has to remove in an over-saturated transistor is higher than in the case of a quasi-saturated transistor. The larger the magnitude of the negative base current I_{b-} and the lower the degree of saturation of the transistor, the shorter the storage and fall times.

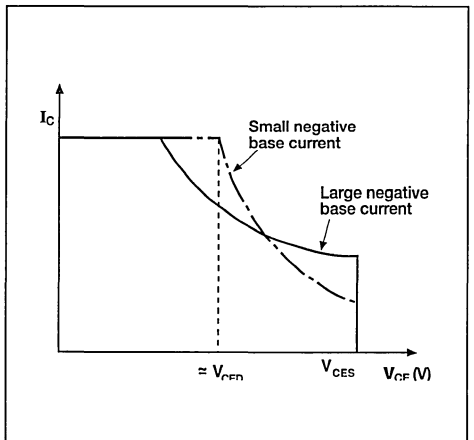
Typical values of storage time and fall time are given on the datasheet of the transistor for specified conditions. However, if the transistor conduction time lasts only a few microseconds, the saturation state cannot be reached. In this condition the turn-off delay time is smaller than the values on the datasheet. Today, most transistor manufacturers specify the storage time as a function of the conduction time t_p (see fig. 4).

Figure 4: Storage time VS. conduction time for BUF410 transistor



Reduction of the storage time may require an extremely high value of extraction current. However a high value of I_{b-} can lead to a change in the safe operating area (SOA) due to the current focussing effect. Fig. 5 shows how an increase of the negative base current leads to an increase of the SOA at low current and a reduction of the SOA at high current.

Figure 5: Effect of the negative base current magnitude on the transistor safe operating area

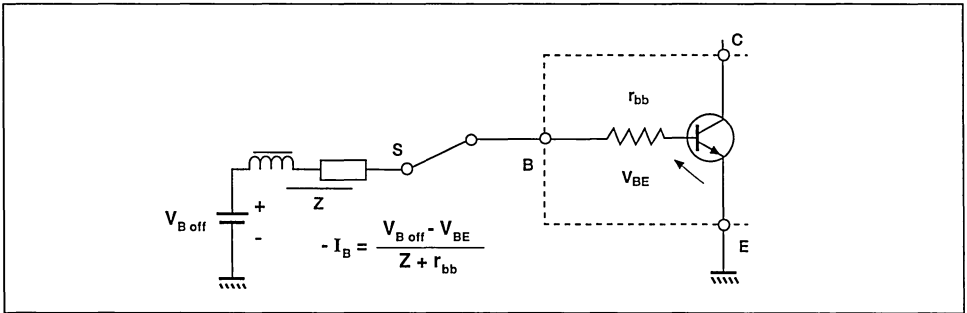


The design of modern bipolar transistors is oriented towards structures with reduced current focussing effect and reduced switching times. Hollow emitter and cellular ETD technologies has been developed for this purpose.

1.3.1 Negative Polarisation at Turn-Off

A negative base-emitter voltage (in the order of the transistor base-emitter breakdown voltage BV_{EB}) can be applied in order to reduce the effect of the parasitic base resistor r_{bb} at turn off. This resistor behaves inversely to the turn on phase and limits the extraction current when the base-emitter junction approaches cut-off (see fig. 6).

Figure 6: Limitation of the negative base current due to the base resistance r_{bb}

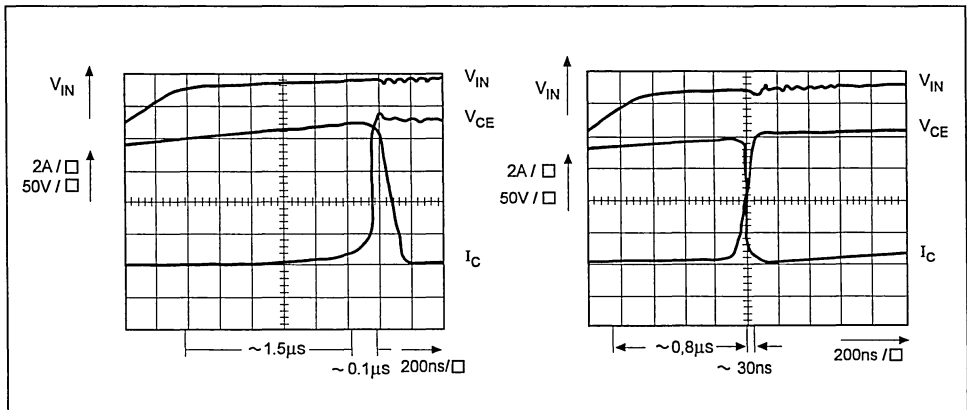


For example a high voltage ETD transistor such as the BUF410 can be turned off with a base-emitter resistance in the order of 0.3 Ohms. In this condition oscillogram 1 shows a fall time $t_f < 100\text{ns}$. ($I_c = 8\text{A}$, $T_j = 100^\circ\text{C}$).

If an negative base-emitter voltage of 2.5 Volts is applied, the fall time is reduced to less than 50ns, see oscillogram 2.

Oscillograms 1&2: BUF410 turn - off

- 1) without negative bias
- 2) with negative bias



2. MOSFET/IGBT

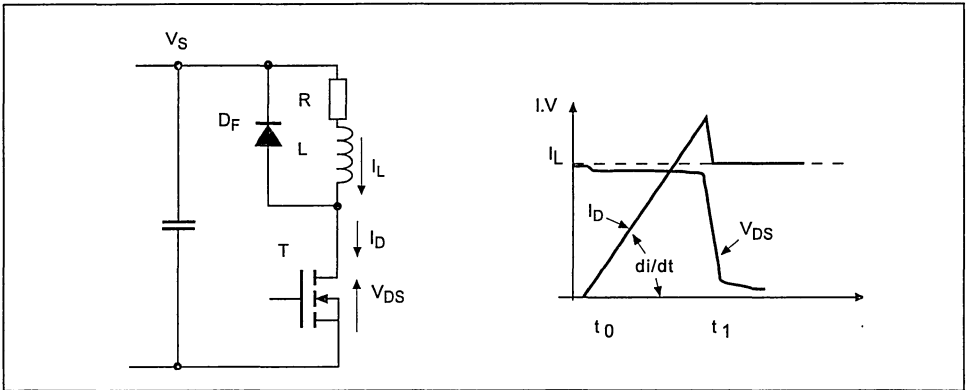
Voltage driven devices have gained great popularity because of the high impedance of their input; a MOSFET gate that requires a minimum of only 8 Volts and microjoules of energy to switch on and off. These characteristics mean that the drive circuit is very simple compared to that of the BJT.

2.1 Turn-On Switching

The most important parameter the drive has to control during the turn-on switching

is the di/dt of the drain/collector current. This parameter is important because turn-on losses depend on the di/dt value. In fact in most applications with inductive loads the turn-on switching occurs when the freewheeling diode is conducting. The recovery of the freewheeling diode permits the device and not the load to define its di/dt . An increase of the di/dt of the drain/collector current corresponds to a reduction of turn-on losses, but at the same time RFI will increase (see fig. 7).

Figure 7: Turn-on switching with a conducting freewheeling diode



The di/dt can be controlled by controlling the rate of increase of the gate voltage.

The circuit can be implemented simply by a gate resistor $R_{G(on)}$ as shown in fig. 8.

Figure 8: Principle of drive stage controlling di/dt at turn - off

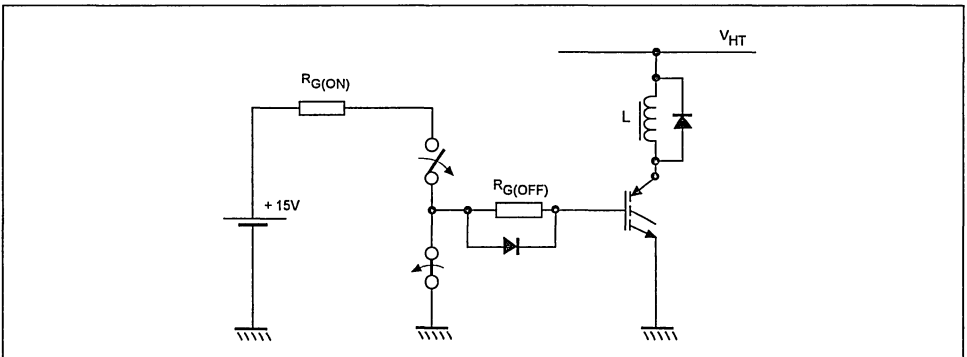


Fig. 9 shows the curves of di/dt as a function of the gate resistor $R_{G(on)}$ for a 500 Volt, 20 Amp IGBT.

Figure 9: di/dt at turn - on $V_s R_{G(on)}$ for the 500V - 20A IGBT (STGH20N50)

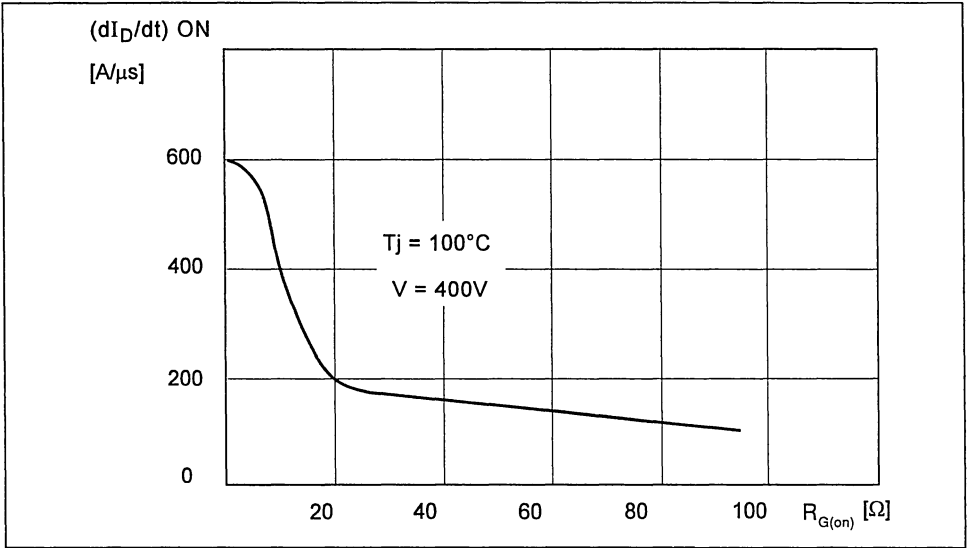
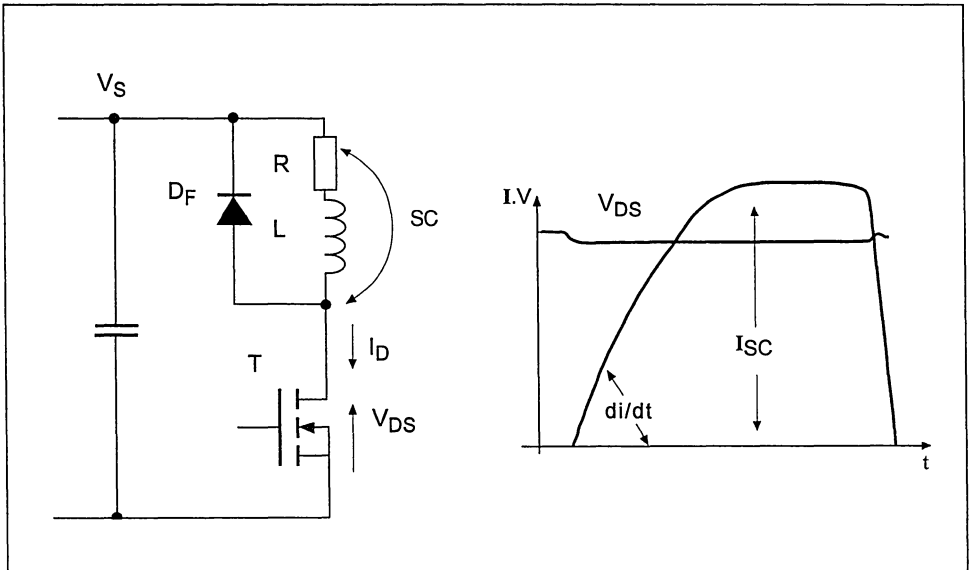


Figure 10: Switching on to a short circuit

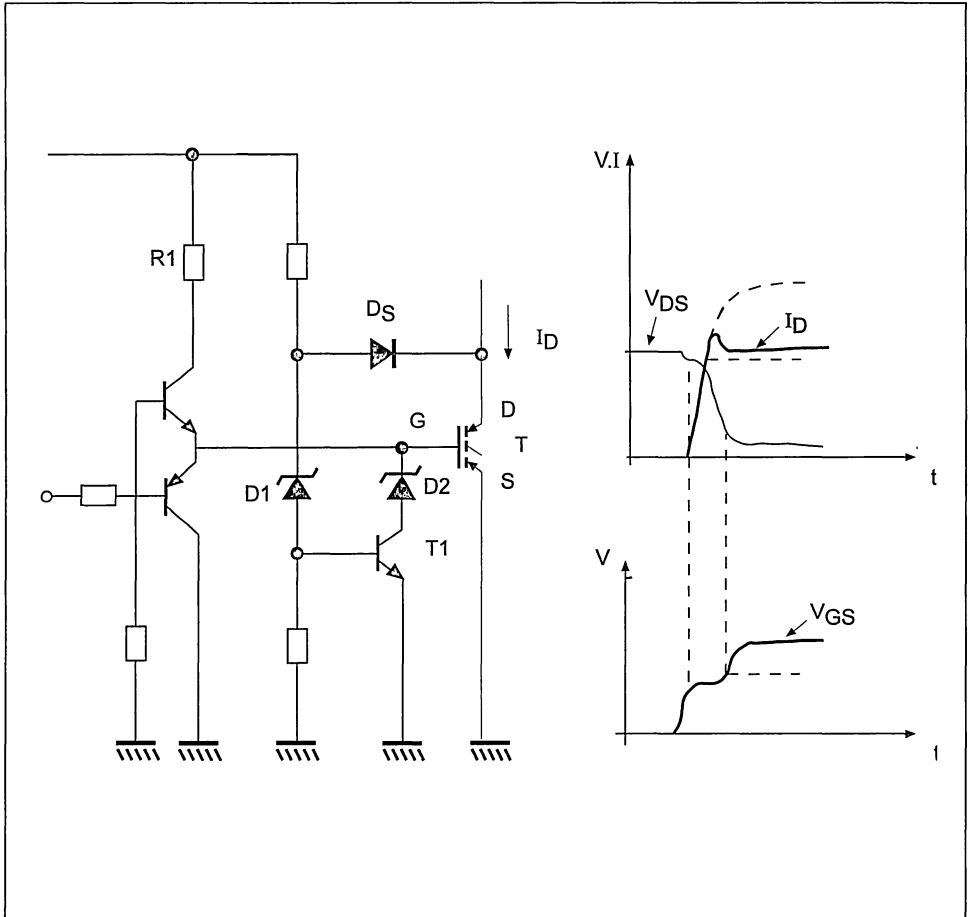


2.1.1 Turn-On Switching during Short Circuit Conditions

In load short circuit conditions, all the supply voltage is applied across the device

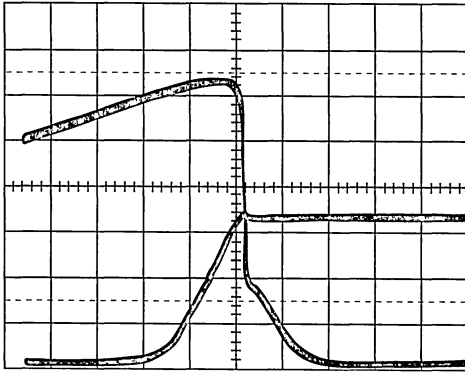
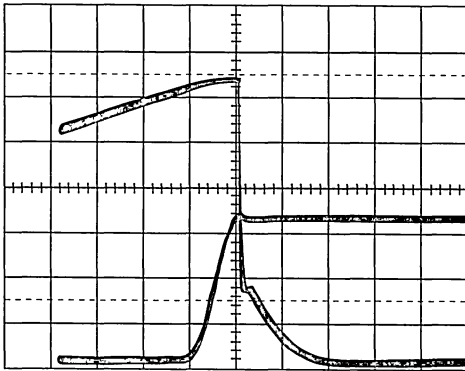
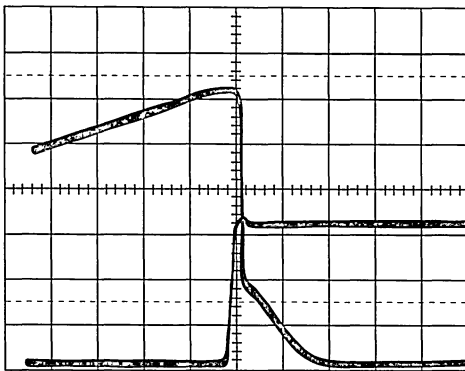
and the short circuit current I_{sc} is fixed by the gate-source/emitter voltage (see fig. 11).

Figure 11: Principle of drive stage controlling di/dt and short circuit current amplitude



The energy the device dissipates in this condition can be very high and destruction of the device can occur in a few microseconds if no protection is activated. All protection circuits have a feedback loop to inform the drive of the abnormal condition; however it can take too long for

the drive to turn off the devices. A reduction of the gate-source/emitter voltage leads to a reduction in the short circuit current I_{sc} which in turn leads to a lower power dissipation and hence to a longer time before destruction. The simple circuit of fig. 12 will carry out this function.

Oscillograms 3 - 5: Turn - off behaviour as a function of $R_{G(off)}$ for 1000V - 30 A IGBTOscillogram 3: $R_{G(off)} = 100\Omega$ V_D I_D Oscillogram 4: $R_{G(off)} = 47\Omega$ V_D I_D Oscillogram 5: $R_{G(off)} = 10\Omega$ V_D I_D

2.2 On State

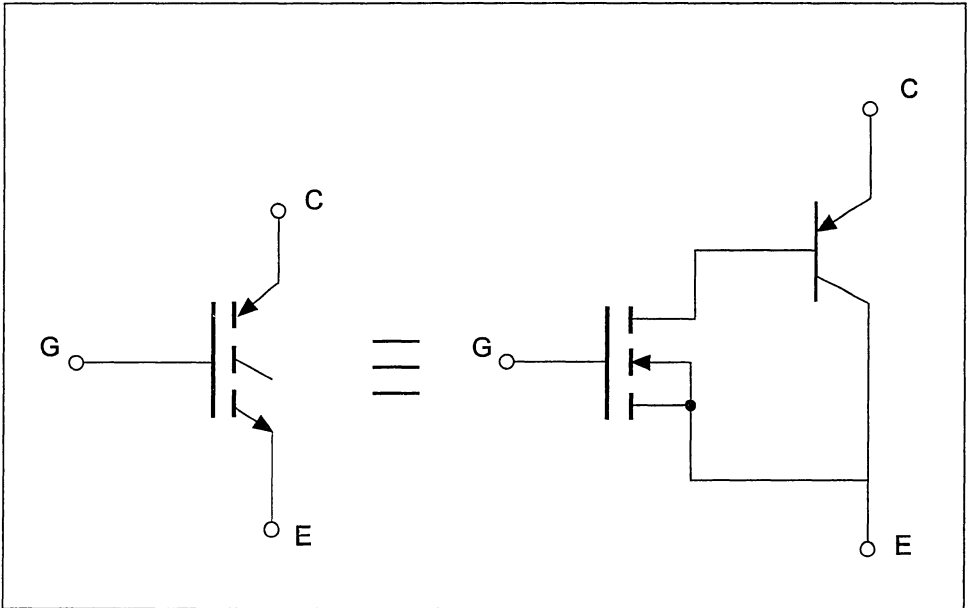
Gate drive does not influence the on state and consequently has no effect on the conduction losses.

2.3 Turn-Off Switching

If the drive circuit is able to control the rate of change of the gate-source/emitter voltage at turn off, then the dV/dt of the collector voltage can also be controlled. Once again the control can be performed by a gate resistor $R_{G(off)}$ as shown in fig. 12. The higher the intrinsic value of

dV/dt the lower the turn off losses, as can be observed by the sequence of oscillograms 3 through 5 for a 1000 Volt IGBT turn off. The gate resistance is varied between 100 Ohms and 10 Ohms. In particular, an IGBT device shows the current tail phenomenon. The sequence of oscillogram shows how the gate drive cannot attenuate the tail effect and associated losses. This is because once the MOSFET section of the IGBT has turned off, the bipolar part remains open base and the base extraction current mechanism cannot work, as shown in fig. 13.

Figure 13: Equivalent circuit of IGBT

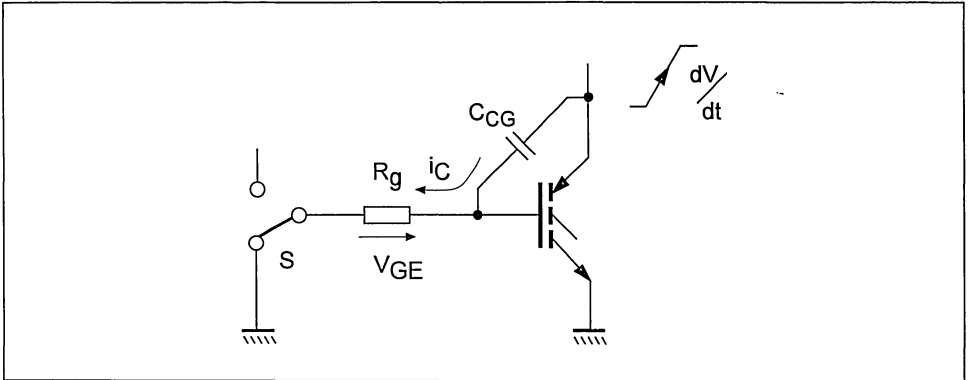


2.4 Off State

During the off state the MOSFET/IGBT can be subjected to dV/dt caused by others devices (static or passive dV/dt). For example in a half-bridge structure, the switching on of the upper switch causes a dV/dt on the lower switch. The presence of a parasitic capacitance

C_{GD}/C_{GC} between drain/collector and gate exposed to the external dV/dt causes a current which flows through the drive output resistance. Depending on the value of the drive output resistance, the switch can be turned on, increasing global losses (see fig. 14).

Figure 14: IGBT reconnection can happen at off - state due to the static dV/dt



In order to avoid switch reconnection, during the off state the driver stage must have:

- a) a very low output impedance
- b) an eventual negative bias.

The negative bias is necessary in all cases where the parasitic inductance L_p of the device package can reach high values. For packages such as the TO-220, TO-218 and ISOTOP, point (a) is enough to ensure that there is no risk of reconnection. Larger packages require a negative bias.

CONCLUSION

A well-designed drive stage can improve the performance of power switches and reduce global losses.

- The storage time and switching losses in a BJT circuit can be reduced and SOA extended by using a base drive circuit which behaves as a current source at turn on, avoids transistor over-saturation in the on state, and which supplies a suitable value of extraction current at turn off.

- It is possible to modify the switching times of a power MOSFET or an IGBT in order to reduce switching losses and the generation of RFI by using a three state gate drive circuit, i.e. with a different output impedance at turn on, turn off and off state.

DRIVE CIRCUITS FOR POWER MOSFETs AND IGBTs

1. INTRODUCTION

Unlike the bipolar transistor, which is current driven, Power MOSFETs, with their insulated gates, are voltage driven. A basic knowledge of the principles of driving the gates of these devices will allow the designer to speed up or slow down the switching speeds according to the requirements of the application.

It is often helpful to consider the gate as a simple capacitor when discussing drive circuits.

2. IGBT / MOSFET DRIVE BASICS

2.1 Gate vs Base

Power MOSFETs and IGBTs are simply voltage driven switches, because their insulated gate behaves like a capacitor. Conversely, switches such as triacs, thyristors and bipolar transistors are "current" controlled, in the same way as a PN diode.

2.2 Driving a gate

As shown in figure 2, driving a gate consists of applying different voltages: 15V to turn on the device through S1, and 0V to turn off the device through S2.

by B. Maurice, L. Wuidart

A remarkable effect can be seen in both the turn-on and turn-off switching waveforms; the gate voltage exhibits a "step", remaining at a constant level while the drain voltage rises or falls during switching. The voltage at which the gate voltage remains during switching is known as the Miller voltage, V_{gm} . In most applications, this voltage is around 4 to 6V, depending on the level of current being switched. This feature can be used to control the switching waveforms from the gate drive.

2.3 MOSFET and IGBT turn-on / turn-off.

When turned on under the same conditions, IGBTs and MOSFETs behave in exactly the same way, and have very similar current rise and voltage fall times - see figure 3.

However, at turn-off, the waveforms of the switched current are different, as shown in figure 4. At the end of the switching event, the IGBT has a "tail current" which does not exist for the MOSFET.

This tail is caused by minority carriers trapped in the "base" of the bipolar output section of the IGBT causing the device to remain turned on. Unlike a

Figure 1. Nature of power semiconductor inputs

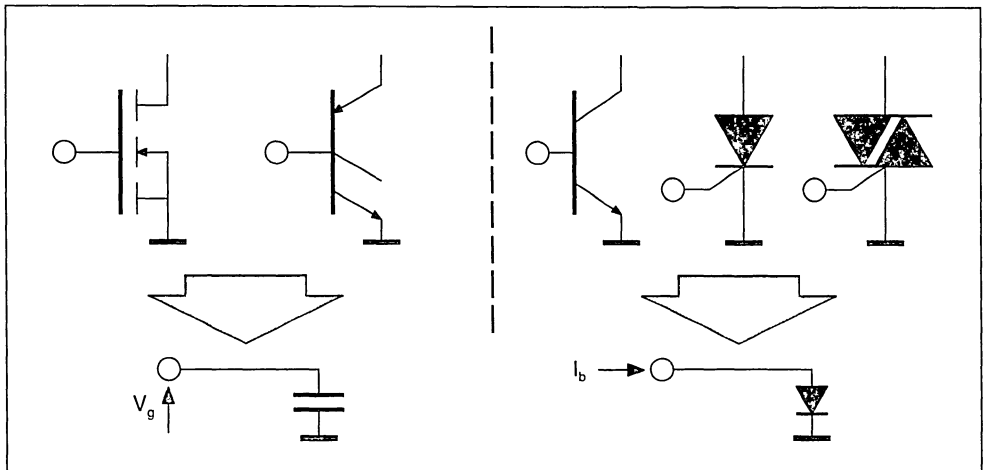


Figure 2. Driving MOSFET / IGBT gates

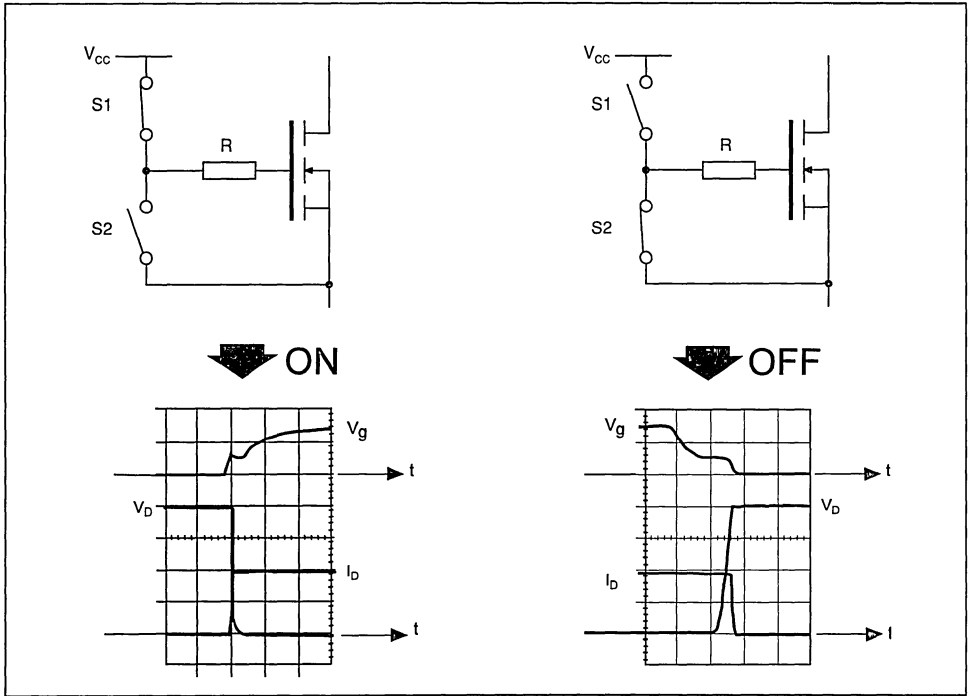


Figure 3. MOSFET / IGBT turn-on

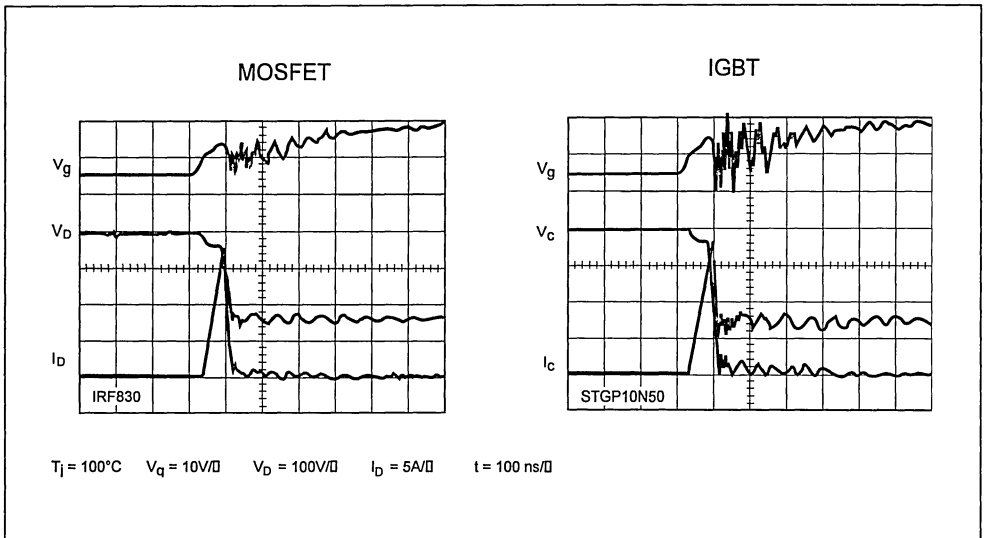
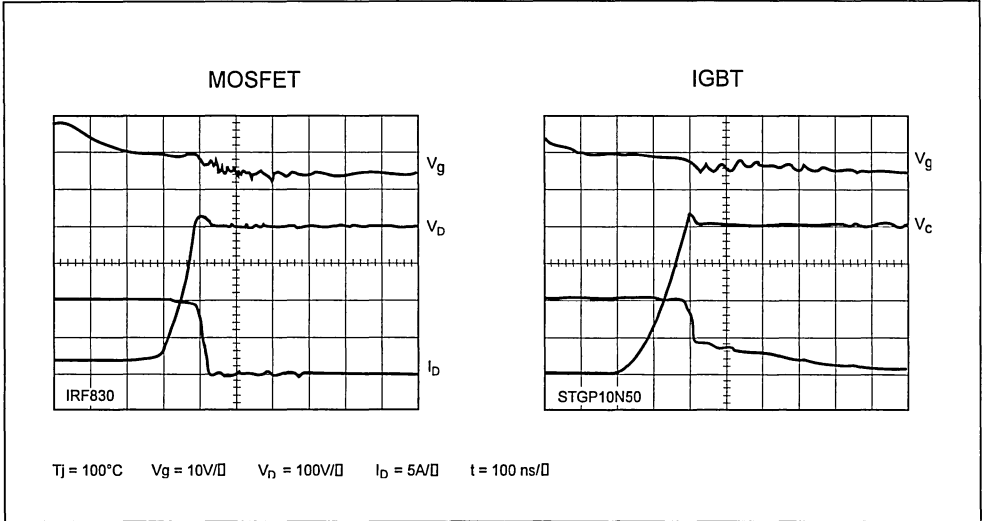


Figure 4. MOSFET / IGBT turn-of



bipolar transistor, it is not possible to extract these carriers to speed up switching, as there is no external connection to the base section, and so the device remains turned on until the carriers recombine naturally. Hence the gate drive circuit has no effect on the tail current level and profile. The tail current does however increase significantly with temperature.

2.4 IGBT turn-off losses

The turn-off of an IGBT can be separated into two distinct periods, as shown in figure 5. In the first period, its behaviour is similar to that of a MOSFET. The increase in drain voltage (dV/dt) is followed by a very fast fall of the switched current. Losses in this “ dV/dt ” period depend mainly on the speed of the voltage increase, which can be controlled by a gate drive resistor.

The second “tail current” period is specific to the IGBT. As this period occurs while there is already a large voltage across the device, it causes losses at each turn-off.

The total turn-off losses are shown in figure 5 by the shaded area.

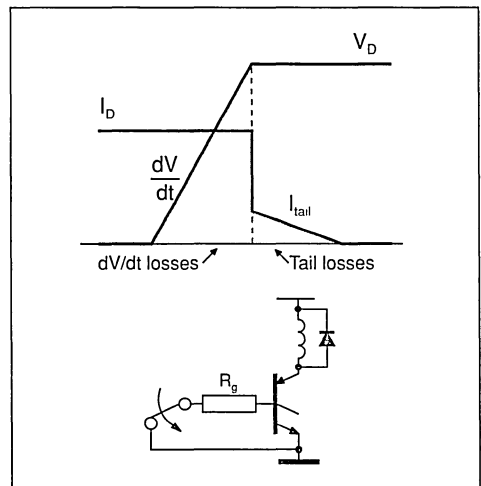
3. FROM GATE DRIVE TO SWITCHING

3.1 Speeding up turn-off

The power involved in these two types of switching

losses is linked to the switching frequency. Turn-off losses become critical when operating at high frequencies. In this case, the dV/dt can be increased (and hence losses reduced) by decreasing the size of the gate drive resistor R_g , which will allow the gate to charge more quickly. The turn-off losses are proportional to the size of the gate resistor - for example decreasing the gate resistor from 100 to 10

Figure 5. IGBT turn-off losses



APPLICATION NOTE

will reduce the dV/dt losses by a factor of 10 - see figure 6.

However, it should be remembered that IGBT tail current losses are completely independent of the value of the gate resistor.

It can be noted that in figure 6 the dV/dt and tail current losses are around the same with a gate resistance of 47Ω .

Even though the tail current is constant, the losses in a system are often predominantly due to dV/dt , because the value of the gate resistance is often too high. In the example of figure 7, the total losses per cycle are reduced from 13mJ to 4mJ by decreasing the gate resistance from 100Ω to 10Ω .

3.2 Reducing dV/dt at turn-off

Conversely, in low frequency applications, fast switching waveforms can cause problems in the form of EMI. A gate driven switch can be used to reduce the amount of EMI, by slowing down the switching speed. This is particularly useful in applications where the mains phase angle is controlled.

The dV/dt can be expressed as:

$$\frac{dV}{dt} = \frac{V_{gm}}{(R_g \cdot C_{iss})}$$

where V_{gm} (the Miller gate voltage) is around 6V, C_{iss} is the equivalent gate-drain capacitance and R_g is

Figure 6. Speeding up turn-off

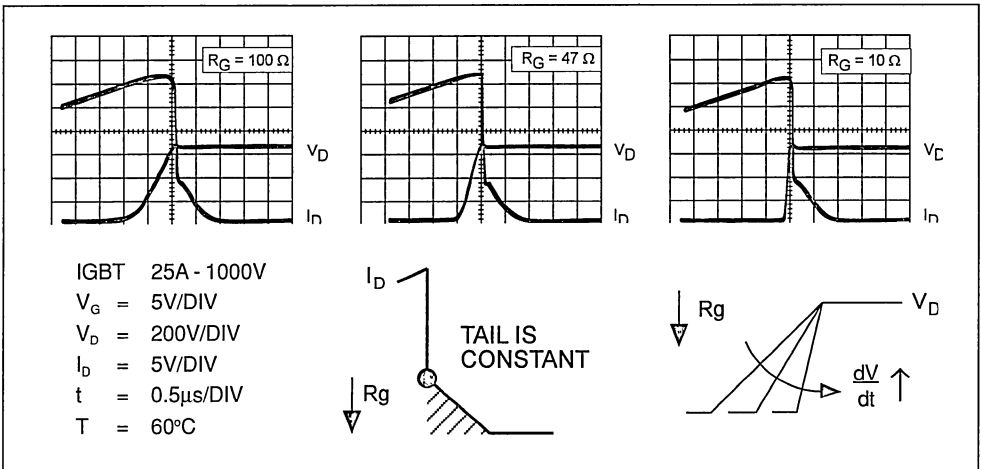
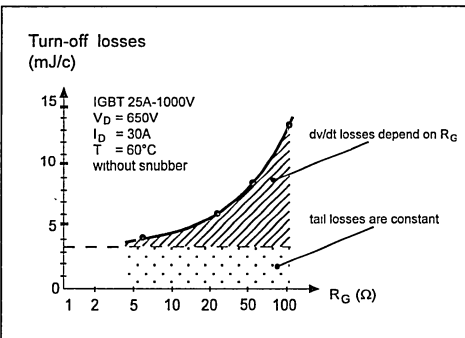


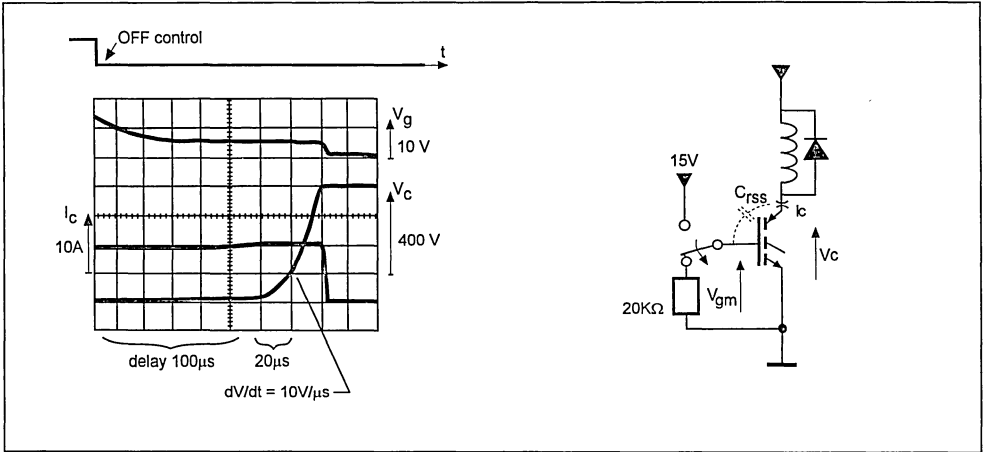
Figure 7. Variation of turn-off losses with gate resistance



the value of the gate resistor at turn-off. One method of slowing down the switching is thus to slow the rate at which the gate capacitor is charged - see figure 8. This can be achieved using a large gate resistor to make the gate charge more slowly and hence increase the dV/dt time. Throughout the dV/dt period, the voltage across the gate resistor is equal to the Miller voltage (V_{gm}), and for a short time the power switch operates in linear mode. In this example, with a STGP10N50 IGBT ($C_{iss} \approx 40pF$) the dV/dt will be around $7.5V/\mu s$.

Alternatively, a capacitor can be connected between the gate and collector / source of the device, which increases the capacitance which must be discharged through the gate resistance at turn-off.

Figure 8. Slowing down turn-off using a gate resistor



3.3 Reducing di/dt at turn-off and turn-on

A technique which slows both turn-on and turn-off uses a small inductor I_E placed in the emitter/source lead of the device, as shown in figure 9. The voltage e developed across the inductor during switching, given by:

$$e = I_E \cdot \frac{di}{dt}$$

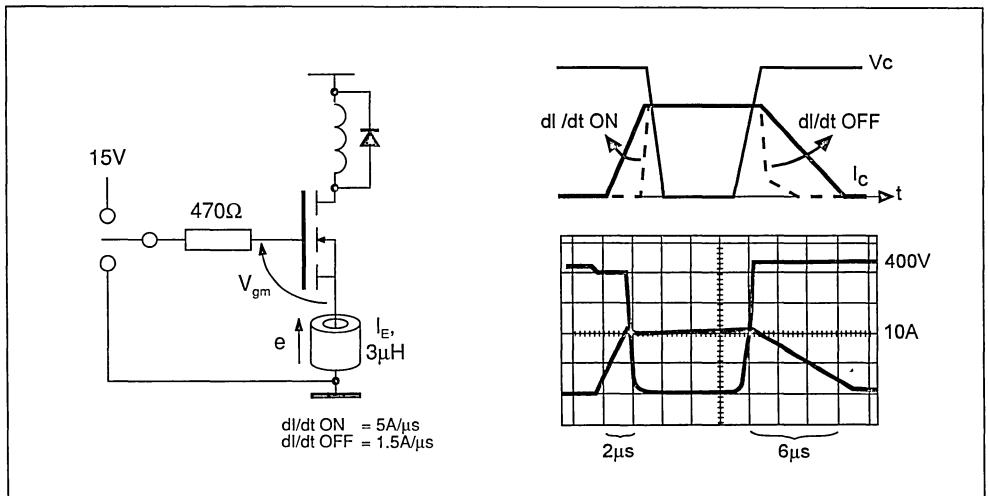
must be equal to the difference between the gate

drive voltage and the Miller gate voltage (V_{gm} , around 6V). The value of di/dt can thus be calculated as:

$$\frac{di}{dt} = \frac{(V_g - V_{gm})}{I_E}$$

For example, in the 4kW example shown in figure 9, at turn-off ($V_g = 0V$) $di/dt = -6V / 3\mu H = -2A/\mu s$. To give an idea, in the circuit used in this example the switching losses are only around 0.8W.

Figure 9. Slowing down the switching of the current using a feedback inductor



4. THE GATE AS A CAPACITOR

4.1 Gate as memory

The capacitive nature of the gate input can be exploited in many different ways, for example as a memory.

In the circuit of figure 10 a single voltage pulse applied to the gate through diode D1 is sufficient to charge the input capacitance C_{in} and turn on the switch T1. When the pulse has finished, D1 prevents the gate discharging, and so the device remains on: the gate is behaving as a memory of the on-state of the switch. To "erase" the gate memory and turn off the switch, a pulse is applied to the diode D2 which turns on T2, which in turn discharges the gate of T1 and turns the device off. As T2 remains on, T1 cannot be accidentally turned on due to dV/dt effects, and so the gate of T2 is now behaving as a memory of the off state of T1.

As the pulse duration times required to turn the devices on and off are very small, this principle can be adapted to suit a wide variety of switching frequencies: from almost continuous operation up to 1MHz.

In low frequency applications, refresh pulses can be used to prevent the gate capacitor discharging due to leakage currents.

The major benefit of this technique lies in the very small size of the pulse transformer required for a wide range of switching frequencies.

For further information on this subject, see reference 1.

4.2 Using the gate in resonant circuits

The gate capacitor can also be used as part of a resonant LC network - see figure 11. With the same peak current value, the capacitor is charged around twice as fast with an inductor compared to a resistor. If the resistor is replaced with an inductor, losses in the gate drive resulting from the charge and discharge current of the gate capacitor become negligible. This solution is particularly efficient in very high frequency applications where gate drive losses become more critical.

An additional benefit is that a resonant circuit has an inherent voltage step-up ability, which means that the 15V required to drive the gate can be generated from a much lower voltage.

Figure 12 shows an example of the gate capacitance being used as part of a resonant circuit.

This type of solution is mainly of use in drive circuits of high power MOSFETs which interface directly with standard 5V CMOS microcontrollers.

Figure 10. Using the gate as a state memory

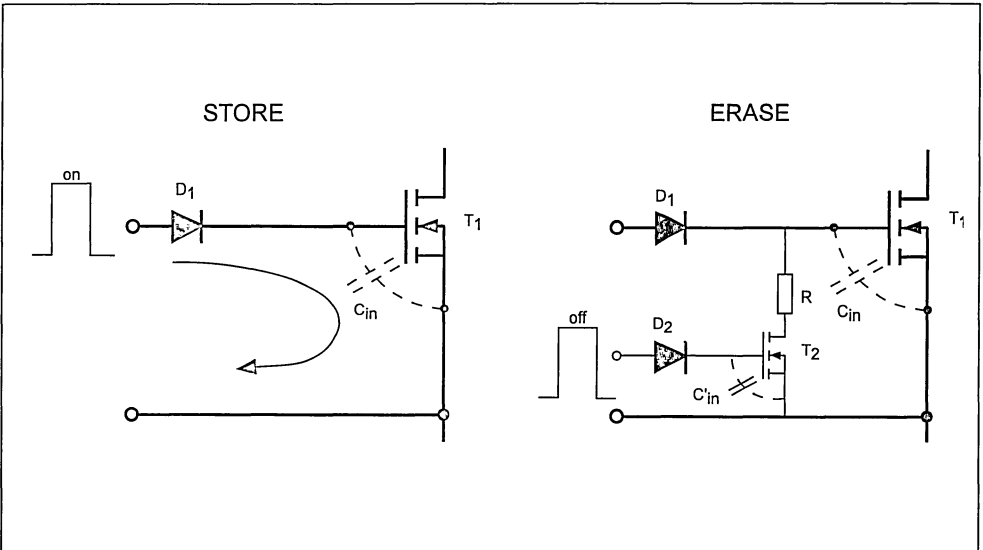


Figure 11. Using the gate capacitance in a resonant circuit

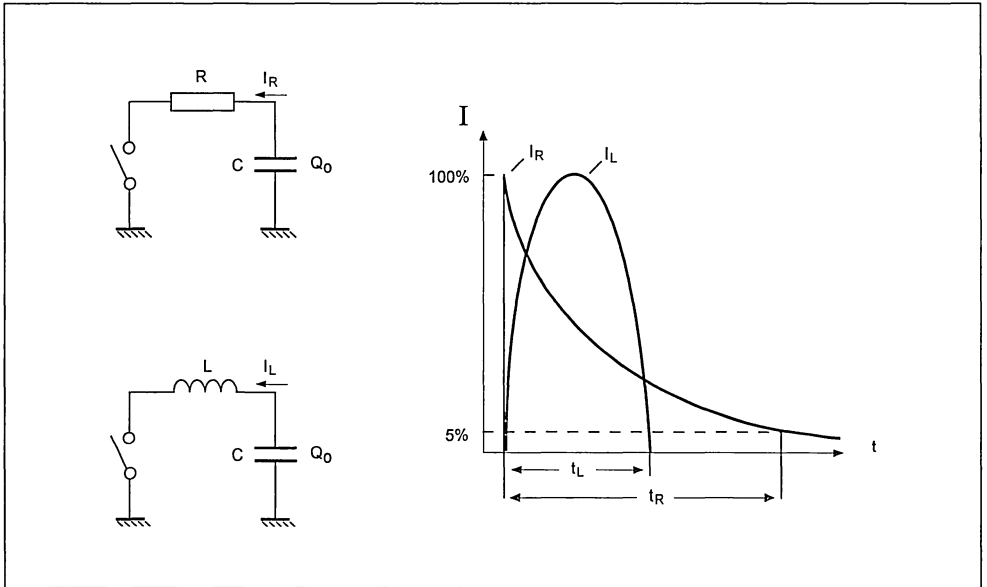
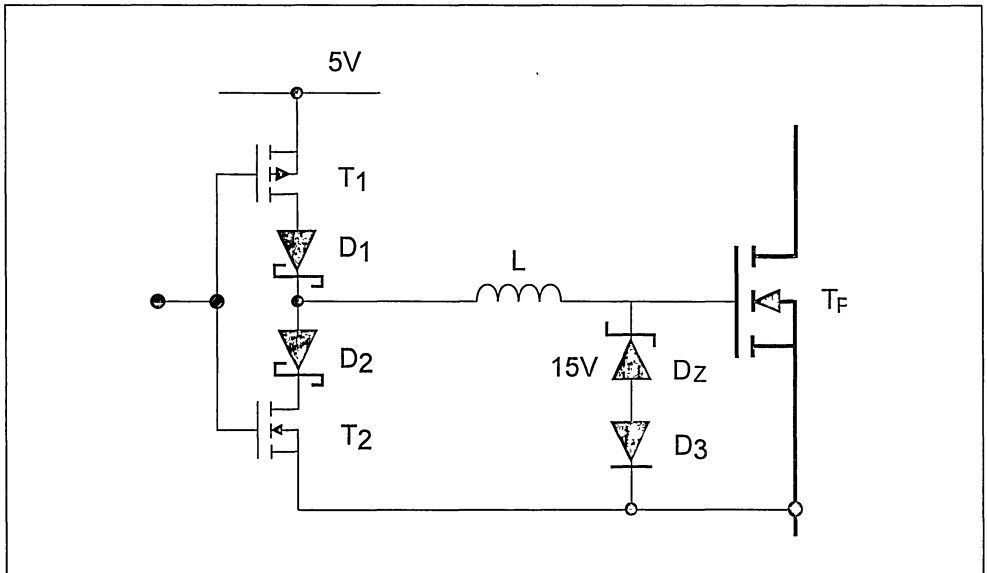


Figure 12. Resonant gate drive circuit



4.3 The gate as an EMI reducer

As mentioned above, the switching waveforms of Power MOSFETs and IGBTs can easily be slowed by adjusting the value of the gate resistor. This feature can be used as an EMI reducer in applications where the mains phase angle is switched (figure 13), for example light dimmer circuits.

Conventional dimming circuits are controlled by TRIACs. Turning a TRIAC on or off generates voltage spikes and uncontrolled dV/dt. In most cases a TRIAC requires a series inductor for EMI filtering.

When the power is controlled by an IGBT, the

switching behaviour can be softened at both turn-on and turn-off so that the inductor is no longer required. The switching losses incurred by slowing down the turn-off of the IGBT are not critical at mains frequency.

The soft light dimmer shown in figure 14 and discussed in reference 2 is based on the use of an IGBT as a switch whose turn-off may be controlled. Such a circuit allows the current switching slopes to be controlled, removing the need for an EMI filter, reducing costs and eliminating the associated acoustic noise. Short circuit protection can also be built in, which means that a fuse is no longer required.

Figure 13. EMI reduction

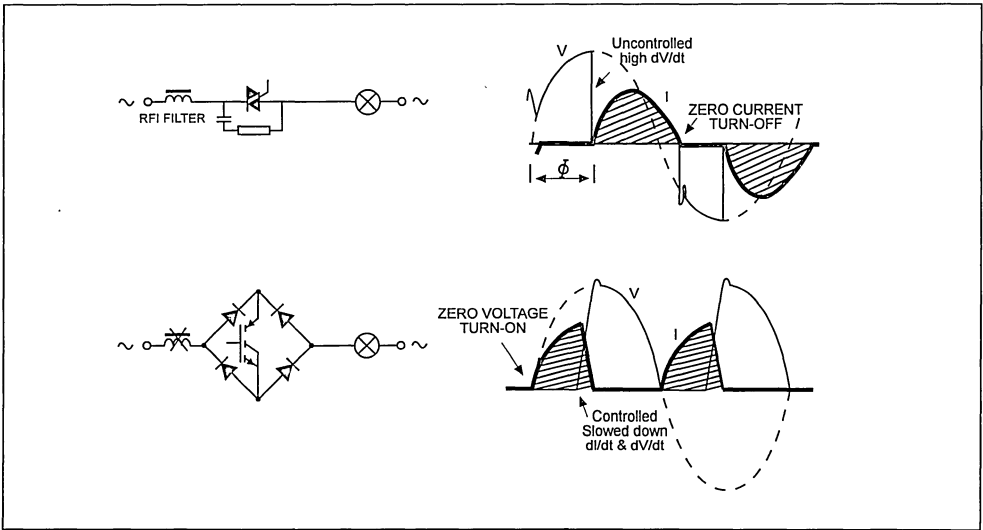
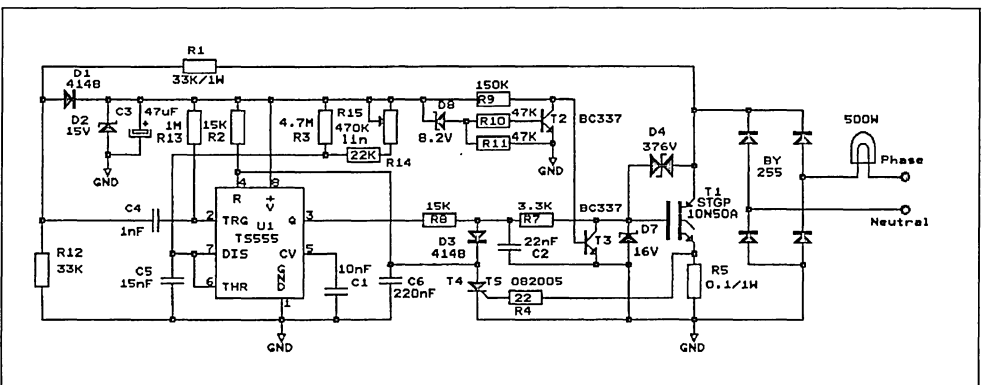


Figure 14. Soft light dimmer circuit



4.4 Automatic floating gate drive

Another useful feature resulting from the small size of the gate capacitor is the low drive energy required to switch high current levels. This characteristic has been used for automatic floating gate drives in asymmetrical half bridges - see reference 3.

Because the drain/emitter voltage of the high side switch in an asymmetrical half bridge floats, most applications require an additional pulse transformer to drive it. In most cases this pulse transformer provides the isolation required to interface the high side switch with the ground-connected PWM control circuit.

However, in the circuit shown in figure 15 an auxiliary winding of the power transformer is used to drive the high side switch as a synchronized slave of the grounded low side switch; when the low side switch turns on or off, the high side switch is automatically turned off or on.

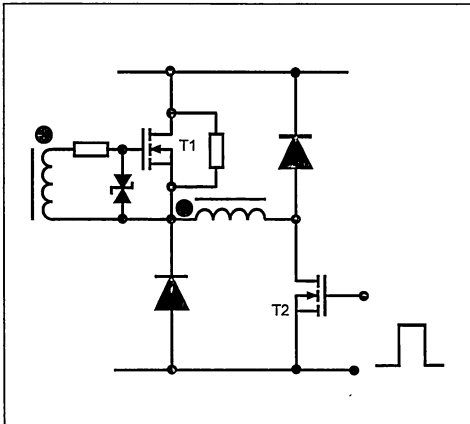
This circuit removes the need for a pulse transformer, and works with very few external components.

4.5 Using multiple drive voltages

The drive circuit shown in figure 16 takes advantage of the voltage driven nature of the gate. In normal operation, 15V is applied to drive the gate fully on, but if an overcurrent is detected, the gate voltage is clamped at 6V (the Zener diode voltage of Z2), limiting the collector current.

Overcurrent is detected by monitoring the collector-emitter voltage of the IGBT - in normal operation the

Figure 15. Automatic floating gate drive

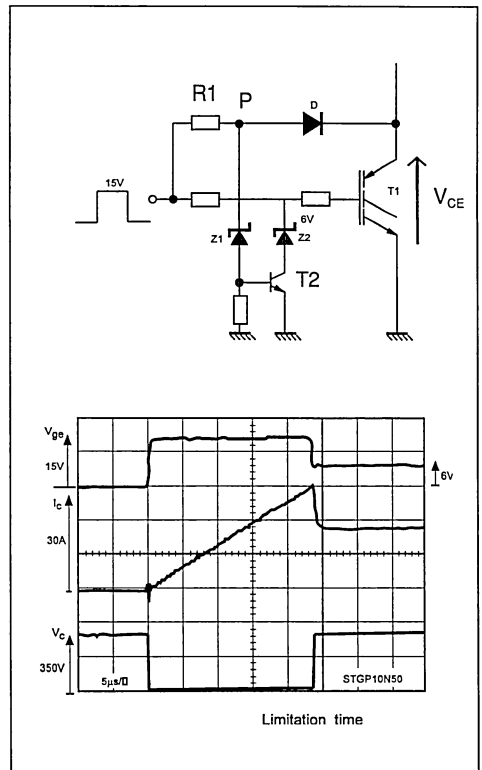


V_{CE} voltage drop will typically be around 2 - 3V, but this increases with increasing collector current. The Zener diode Z1 is selected to set the V_{CE} level at which the protection will operate.

Consequently, in the normal mode of operation, 15V is applied to the input to turn the transistor fully on, which also causes the diode D to be forward biased through resistor R1. The voltage at point P is thus equal to the V_{CE} voltage drop across the IGBT, plus the voltage drop across D. The rating of Z1 is chosen such that in these conditions it remains blocked.

However, if an overcurrent causes the V_{CE} of the IGBT to increase, when the voltage at point P reaches the rating of the Zener Z1, Z1 begins to conduct, turning on T2, and clamping the voltage at point P, causing D to become reverse biased. Turning on T2 causes Zener Z2 to clamp the IGBT gate voltage at 6V, limiting the collector current to a lower level.

Figure 16. Current limitation using multiple drive voltages



5. TRENDS

Although insulated gate devices are widely used and well understood, it remains interesting to reconsider the gate operating as a simple capacitor. A useful feature of insulated gate switches is their ability to soften switching waveforms easily. IGBTs used in this way, as EMI reduction / turn-off controllable switches, are a very attractive alternative to TRIACs in lamp dimming circuits.

Additionally, the ability of insulated gate switches to be driven with a small amount of energy has lowered the power level at which half bridge topologies can effectively be used. This trend of the last decade is highlighted demonstrated by the advent of integrated high side driver circuits. For this reason, equipment designers will no longer hesitate to drive high side floating Power MOSFETs and IGBTs, even in the 100W power range.

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AN ISOLATED GATE DRIVE FOR POWER MOSFETs AND IGBTs

by J.M. Bourgeois

ABSTRACT

Power MOSFET and IGBT gate drives often face isolation and high voltage constraints. The gate drive described in this paper uses a Printed Circuit Board based transformer in combination with the memory effect of the Power MOSFET input capacitance to achieve the isolation.

This transformer is a bi-directional link between the ground-referenced control IC and the floating gate drive. It transfers drive energy and signal information to the gate drive, provides full duty cycle range and perfect dV/dt immunity, and imposes virtually no voltage constraint. No floating auxiliary supply is required.

If the short circuit protection is triggered, an alarm signal is transmitted back to the primary through the same transformer. This circuit is perfectly suited to driving floating and/or isolated switches in motor drives, uninterruptible power supplies and AC switches.

1. INTRODUCTION

Isolated power switches are often used in motor drives, uninterruptible power supplies and AC switches. Isolation is usually a requirement of safety norms and operating conditions when the switch voltage floats with respect to ground.

This paper highlights a specific characteristic of the Power MOSFET which is often neglected: the use of the gate input capacitance as an ON state memory. It proposes an innovative isolated gate drive using a pulse transformer constructed using copper PCB tracks, combined with the memory effect of the Power MOSFET.

2. PRINCIPLES OF OPERATION

The circuit operates using the Power MOSFET input capacitance to memorize the ON-state, a second auxiliary capacitor to memorize the OFF-state, and PCB tracks to form the windings of the transformer.

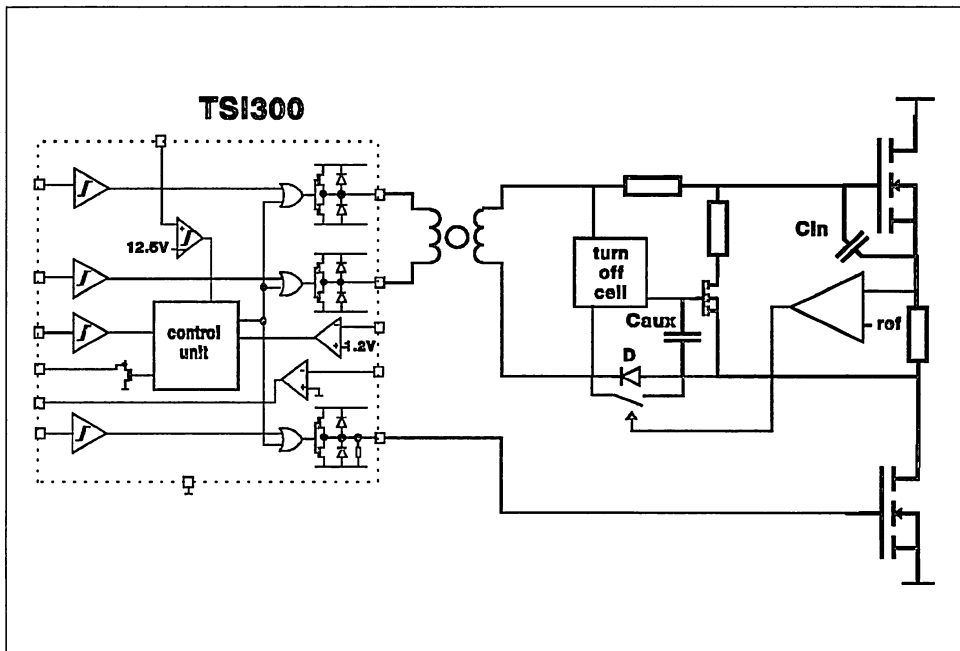
4. FUNCTIONAL DESCRIPTION

Figure 2 shows a block diagram of the circuit. It consists of a TD300 pulse transformer driver, a PCB based transformer and an isolated secondary circuit.

4.1 Primary circuit

The TD300 is a three channel MOSFET driver with pulse transformer driving capability. It has been optimized for both capacitive load drive and pulse transformer demagnetization.

Figure 2: Circuit block diagram



It can therefore directly drive a low side switch and, through a pulse transformer, an high side switch. Its low buffer $R_{DS(ON)}$ can conduct a demagnetizing current of 100mA with no significant voltage drop. The transformer inductance can therefore be kept low, and the transformer windings can be implemented with few turns laid on a Printed Circuit Board.

The TD300 integrates three additional circuits enabling protection and control functions: an undervoltage lockout, an operational amplifier and a comparator.

4.2 Pulse transformer

The pulse width required to fully charge the gate capacitance is typically around $1\mu\text{sec}$. Supposing that double pulses can occur during the operation, the maximum Volt.second product is $30\text{V}/\mu\text{sec}$. With a magnetizing current of 100mA, the primary transformer inductance required is:

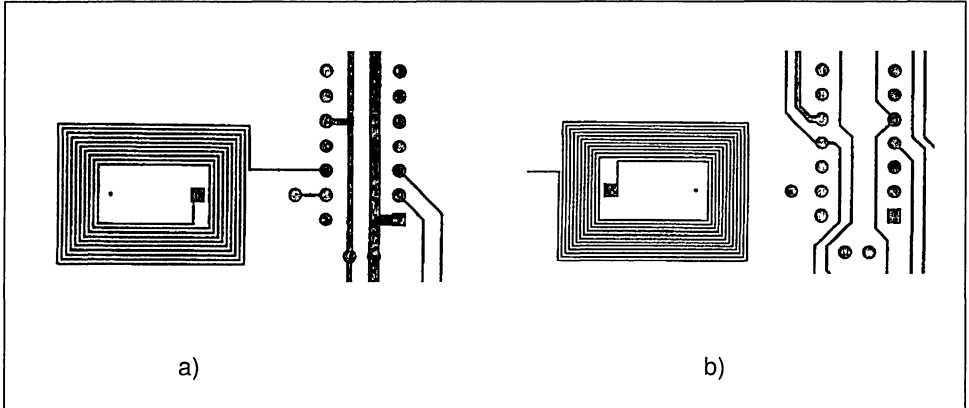
$$L = V \cdot (di/dt)^{-1} = 300\mu\text{H}$$

This low value of inductance allows the primary winding to be limited to 10 turns using a realistic section of ferrite.

Figure 3 shows an implementation using PCB tracks to form the inductor. Track widths are 12 mils at the primary and 10 mils at the secondary. The inter-line distance is 4 mils in both cases (mask definition).

Experimental tests showed that the magnetizing current reaches 100mA after 2 μ sec using a standard A4-U-1606A made of high permeability material ($\mu_i = 6000$ - standard THOMSON Passive Components).

Figure 3: PCB layout: a) Upper side
b) Lower side



However the magnetic path of this U core is too long for through-hole applications. Using a bus bar core shape with the same section but with shorter legs to fit the PCB, the magnetizing current should fall to 60mA. It is then possible to increase the pulse time or to decrease the core section to obtain a magnetizing current of 100mA.

4.3 Secondary circuit

Many different secondary circuit topologies can be used, depending on application performance and cost. The cheapest solution uses one zener diode and one resistor, but the digital control is more complex, and it has no floating short circuit protection (see reference 6).

For more sophisticated applications, figure 4 shows a step by step analysis of the secondary circuit shown in figure 1.

Turn-ON pulse: figure 4a shows the charge current I_c of the MOSFET input capacitor when a positive pulse is applied across the

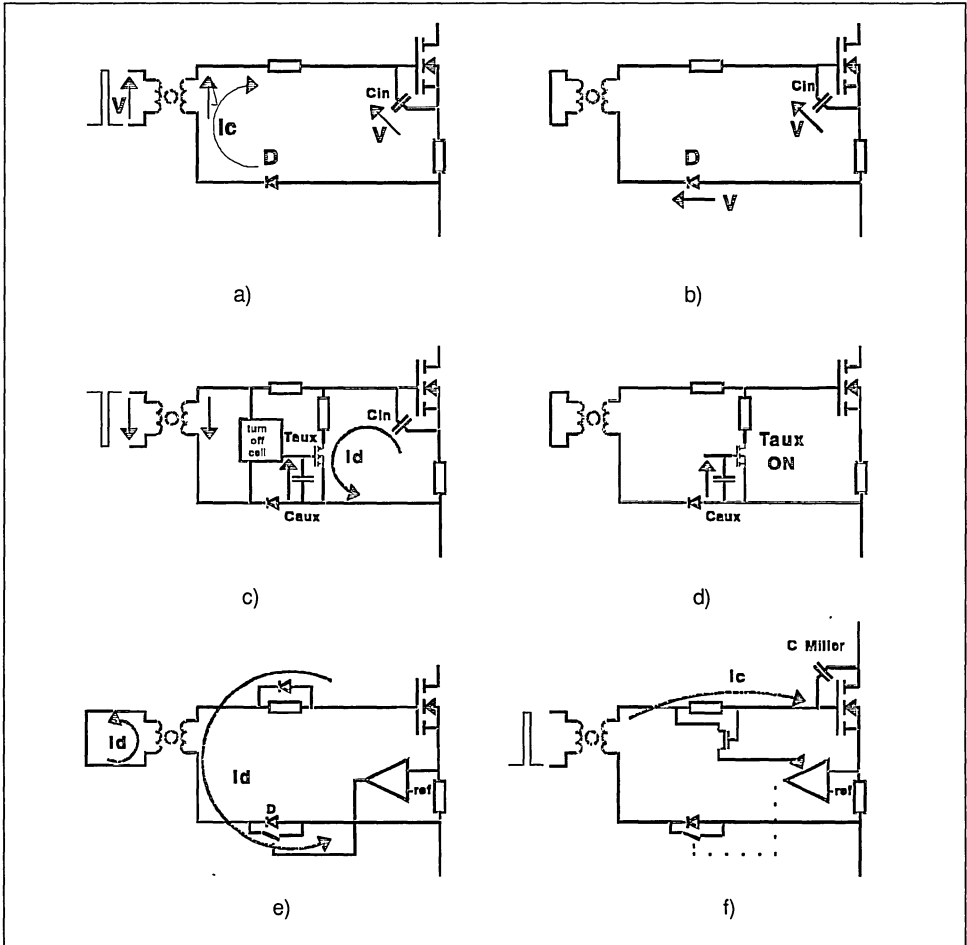
pulse transformer primary. When the primary pulse ends, the transformer secondary voltage is approximately zero, and the diode D prevents C_{in} from being discharged.

In figure 4b, the MOSFET keeps its gate charge after the pulse and remains in the conducting state. The ON-state is memorized in the input capacitor C_{in} .

Turn-OFF pulse: Figure 4c shows the input capacitor discharge current I_d when a negative pulse is applied across the pulse transformer primary. Discharge occurs when an additional circuit transfers the secondary voltage to the auxiliary capacitor C_{aux} , making T_{aux} conduct. When the pulse ends, the OFF-state is memorized in the auxiliary capacitor. A low impedance is then maintained across the power switch, avoiding unwanted turn-on (see figure 4d).

Short circuit protection: A short circuit can be detected by means of a shunt or current sense. Then, the diode D is shorted,

Figure 4: Details of circuit operation



allowing the power input capacitor to discharge through the pulse transformer just after the turn-on pulse. This produces a negative current pulse in the transformer secondary, enabling the short circuit to be detected via the primary winding. Indeed, this discharge current inverts the demagnetizing current temporarily, inverting the buffer output voltage (see current I_d , figure 4e). The short circuit conduction time is approximately the turn-on pulse time.

Diode recovery current: Generally, inverter power switches face a diode recovery current at turn on. This creates a brief over-current in the switch that requires masking from the short circuit detection during the recovery time.

Due to the Miller effect, the current I_c lasts for as long as the collector/drain voltage falls. Inhibiting the short circuit detection by means of I_c masks all the diode recovery current (see figure 4f).

5. MAIN FEATURES OF THE CIRCUIT

5.1 No floating auxiliary supply

The power MOSFET switches are supplied by pulses from the transformer. No floating auxiliary supply is required.

5.2 Large operating frequency range

This driver can operate at up to several tens of kiloHertz because the transformer delivers very short pulses, typically 500nsec or 1µsec. If DC or very low frequency operation is required, circuits to perform an automatic refresh of memory capacitors must be implemented; the primary circuit should then drive the transformer with a burst of positive or negative pulses. (see reference 6).

5.3 Large duty cycle

Again because of the length of the transformer pulses, the possible range of duty cycles is large: the minimum ON or OFF time is about 500nsec, allowing the duty cycle to range from 1% to 99% at 20kHz. There is no maximum ON or OFF time.

5.4 Low energy and cheap transformer

The energy transferred to the secondary by the pulse transformer is (on average per cycle) about four times the energy stored in the gate capacitor (average current of about 2mA at 10kHz for 50nF). The transformer magnetizing energy must be added two times per cycle (average current of about 2mA at 10kHz for 300µH), so global driver energy consumption is very small.

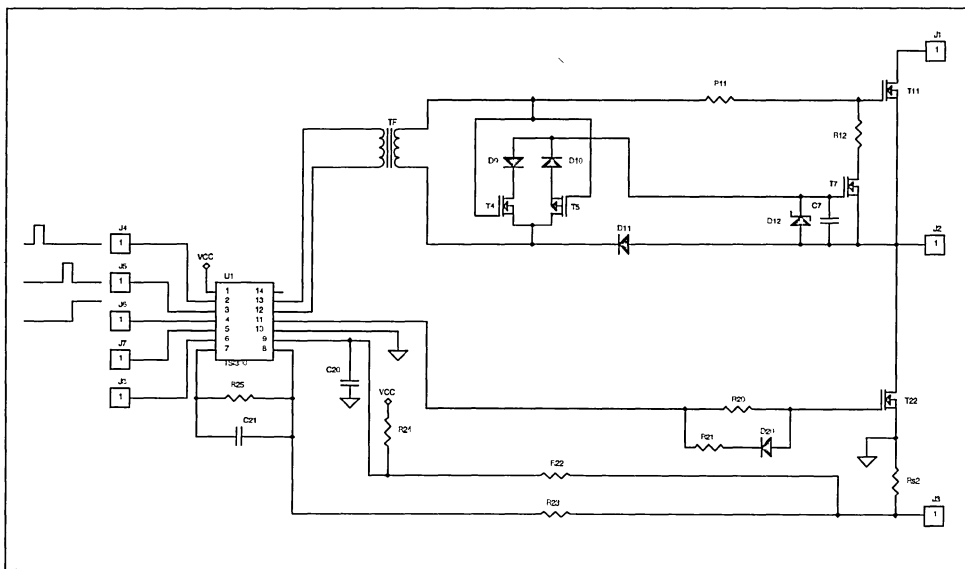
The construction of the transformer can be automated using PCB based windings.

5.5 Good ground to gate drive isolation and perfect dV/dt immunity

Because the pulse transformer provides the isolation, creepage distance and clearance are easily adjusted to suit the application requirements.

The primary-secondary electrostatic coupling effects are negligible, and immunity to fast voltage variations (dV/dt) is perfect.

Figure 5: Simplified circuit



5.6 Low gate drive output impedance during OFF-state

During its OFF-state, a low impedance is maintained across the gate-source terminals of the Power MOSFET, avoiding unwanted turn-on should any external dV/dt be applied to the MOSFET.

5.7 Short circuit protection

The secondary circuit has an automatic short-circuit protection. This protection is inhibited during turn-on pulses in order to mask diode recovery current.

5.8 Alarm signal

When the short-circuit protection is operating, the Power MOSFET input capacitor is discharged through the pulse transformer, causing an alarm signal to be transmitted in the reverse direction from the secondary to the primary of the pulse transformer.

6. CONCLUSION

This Power MOSFET drive is perfectly suited to drive floating and/or isolated switches. Its operating mode permits a large range of duty cycles, requiring no floating auxiliary supply, and has perfect dV/dt immunity. The short circuit protection provides an alarm signal to the grounded circuit control via the pulse transformer.

This circuit operates whatever the line voltage as long as suitably rated power switches are used. Its transformer windings are laid on a double-sided PCB, allowing automation of the transformer construction process.

Its major fields of application are motor drives, uninterruptible Power supplies and AC switches.

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PROTECTION AND GATE DRIVERS FOR MOSFETS USED IN BRIDGE LEG CONFIGURATIONS

by C. Patni

INTRODUCTION

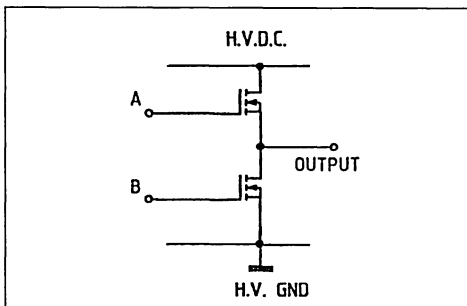
The bridge-leg is an important building block for many applications such as drives and switch-mode power supplies. Simple gate drives with protection for POWER MOSFETs need to be designed for the "low-side" and the "high-side" switches in the bridge-leg. The POWER MOSFET can conduct a peak drain current, I_D , which is more than three times its continuous current rating. The POWER MOSFET peak current capability and its linear operating mode are used to good effect in designing device protection circuitry.

Bridge-leg configurations have a direct bearing on the degree of protection that can be incorporated. Consequently, bridge-leg configurations, protection concepts and gate drives are created simultaneously to design optimised and reliable power electronic circuits.

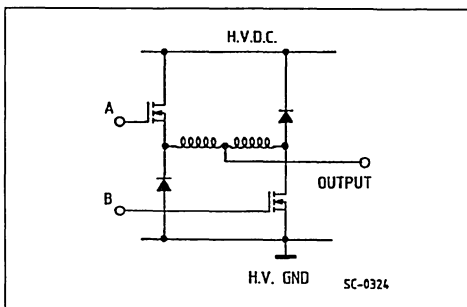
H-BRIDGE USING POWER MOSFETs

Three POWER MOSFET based bridge configurations are illustrated in figure 1. Figure 1a illustrates a bridge-leg which uses the internal parasitic diode as a free-wheeling diode thus reducing cost. However, since the reverse recovery of this parasitic diode is in the order of a microsecond, the turn-on switching times of the POWER MOSFET have to be increased in order to reduce the reverse recovery current. The turn-on time of the POWER MOSFET is controlled such that the pulse current rating of the internal diode is not exceeded. Hence a compromise is made between maintaining the safe operating area of the MOSFET and reducing turn-on switching losses. For example, an IRF640 MOSFET has a diode pulse current rating in excess of 80A and a typical diode reverse recovery time of 300ns. A rate of change of current at turn-on, limited to 50A/s, is a realistic compromise between reverse recovery current magnitude and turn-on losses. Consequently switching speed is sacrificed for cost. For switching frequencies up to 10kHz, when operating on a 400V DC high voltage rail, this configuration can be chosen as switching losses are limited, thus enabling a realistic thermal design.

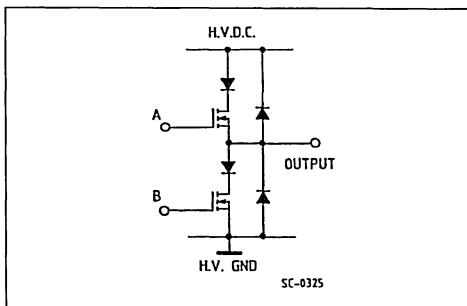
Figure 1 : Bridge Configurations.



a) Bridge-leg using Internal Parasitic Diode.



b) Asymmetrical Bridge-leg providing di/dt Protection.



b) Bridge-leg with blocking Diodes.

APPLICATION NOTE

The turn-off speed of the POWER MOSFET in this configuration has no restrictions. Thus a fast turn-off is desirable to reduce turn-off losses. As the rate of change of current is limited, radio frequency interference (RFI) and electromagnetic interference (EMI) are reduced.

An asymmetrical bridge-leg, illustrated in figure 1b ; can be used to limit di/dt during a short-circuit condition thus providing sufficient time to switch-off the appropriate power devices. The inductors limit the rate of rise of output current. They also limit the free-wheeling current through the internal parasitic diodes of the MOSFETs. Adding external free-wheel diodes and inductors increases reliability at the cost of increased complexity. The inductors reduce RFI and EMI as the rate of change of current is limited.

The configuration illustrated in figure 1c has Schottky "blocking" diodes to prevent current going through the MOSFET internal parasitic diodes. Schottky diodes are often used since conduction losses are kept to a minimum.

Bridge configurations shown in figure 1b and 1c are considered for high frequency switching applications. The advantage of the asymmetrical bridge-leg configuration over the bridge configurations in figures 1a and 1c is that the bridge-leg is capable of withstanding simultaneous conduction of the two devices in the bridge-leg since there are series inductors which reduce the di/dt under this condition. Hence the short-circuit detection loop time is not so critical and the devices are not stressed with high di/dt and high pulse currents.

The choice of the bridge configuration depends on the technical specification of the application. For example, if the technical specification for a specific application can be met by using the configuration shown in figure 1a, then this configuration should be used as costs are lower than with the other two configurations shown in figures 1b and 1c.

GATE DRIVE CIRCUITS

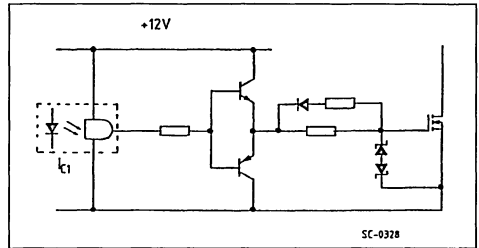
The POWER MOSFET is a voltage controlled device, unlike the bipolar transistor which requires a continuous base drive. An application of a positive voltage between the gate and the source results in the device conducting a drain current. The gate to source voltage sets up an electric field which modulates the drain to source resistance. The following precautions should be considered when designing the gate drive ;

- 1 - Limit V_{GS} to 20V maximum. Use of a gate to source voltage in excess of 16V has a marked effect on the lifetime of the device.

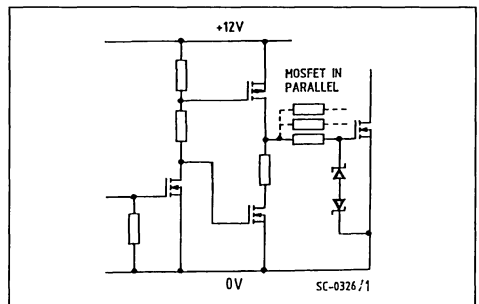
- 2 - Gate drive parasitic inductance can cause oscillations with the MOSFET input capacitance. This problem becomes more pronounced when connecting devices in parallel.
- 3 - There should be sufficient gate to source voltage for the transistor to be fully conducting.

Figure 2 : Gate Drive Circuits.

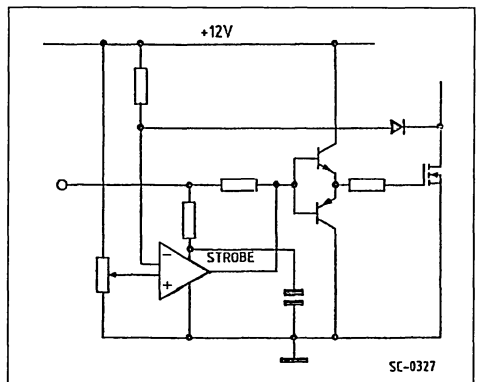
- a) Isolated gate drive with controllable switching times.



- b) Simple gate drive for N-Channel MOSFETs in parallel.



- c) Gate drive with V_{DS} (on) control for short-circuit protection.



Bipolar, MOSFET, CMOS or open-collector TTL logic can be used in the design of simple high performance gate drives. Totem-pole buffers, (figure 2a), are often effectively used to control the turn-on and turn-off individually. Figure 2b illustrates a total MOSFET based gate drive with which the switching speeds at turn-off can be individually controlled. CMOS or open-collector TTL logic can be used to drive MOSFETs directly, provided an ultrafast switching speed (50ns) is not necessary. In motor drive applications switching speeds of 100 to 200 nanoseconds are sufficient as switching frequency is seldom in excess of 50kHz. Discrete buffers are used to provide high current source and sinking capability when improved switching speeds are required or when MOSFETs are connected in parallel.

Short-circuit protection techniques similar to bipolar transistors may be considered for MOSFETs. $V_{DS(on)}$ monitoring permits the detection of short-circuit conditions which lead to device failure. The device can be switched off before the drain current reaches a value in excess of the peak pulse current capability of the MOSFET. This form of protection is very effective with MOSFETs as they can sustain a pulse current in excess of three times the nominal continuous current. Figure 2c illustrates a gate drive which incorporates $V_{DS(on)}$ monitoring and linear operating mode detection for the MOSFET in the case of short-circuit conditions. When the MOSFET is turned on the on-state voltage of the device ($V_{DS(on)}$) is compared with a fixed reference voltage. At turn-on, $V_{DS(on)}$ monitoring is inhibited for a period of approximately 400ns in order to allow the MOSFET to turn-on fully. After this period, if $V_{DS(on)}$ becomes greater than the reference value, the device is latched-off until the control signal is turned-off and turned-on again.

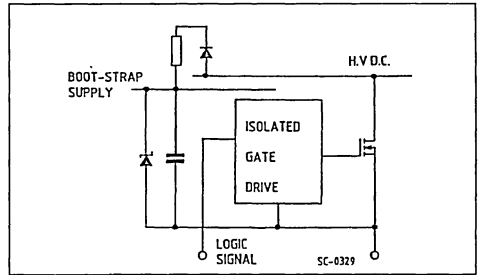
"HIGH-SIDE" SWITCH GATE DRIVES

The top transistor in a bridge-leg requires a "high-side" gate drive circuit with respect to the bridge ground. Three possible gate drive concepts are shown in figure 3 :

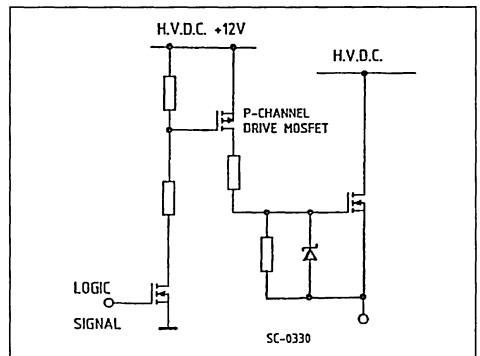
- The "bootstrap" drive, requiring logic signal isolation, but no auxiliary floating supply.
- The level shifting drive.
- The floating gate drive with optically coupled isolators, pulse transformers or DC to DC chopper circuit with transformer isolation.

Figure 3 : Gate Drives for Top Transistor of Inverter Leg.

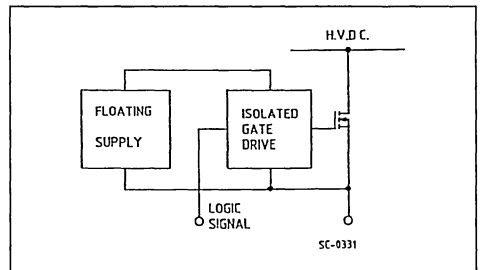
a) "Bootstrap" supply floating gate drive.



b) Level shifting gate drive.



c) Floating supply isolated gate drive.



Bootstrap supplies are particularly well suited to POWER MOSFET gate drives which require low power consumption. Figure 4 illustrates two bootstrap supply techniques. Bootstrap supplies limit transistor duty cycle since they require a minimum transistor off time during which they are refreshed.

APPLICATION NOTE

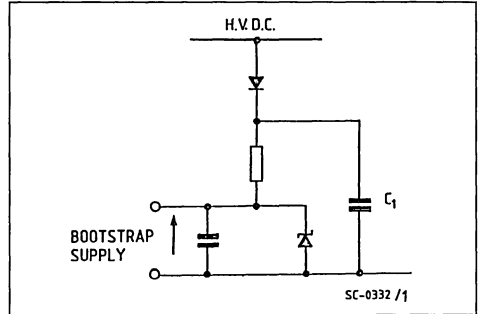
Supply efficiency and maximum duty-cycle are parameters which govern the design of the bootstrap. Figure 4a illustrates a conventional bootstrap with an additional capacitor, C1, which improves the maximum duty cycle as the supply is refreshed even during transistor on time by this capacitor. Figure 4b illustrates a high efficiency bootstrap supply which uses a small MOSFET, Q1, for regulation. In this design a low power bootstrap drives the gate of Q1.

The level shifting gate drive, (figure 3b), requires a high voltage p-channel MOSFET which drives the n-channel power device. The p-channel MOSFET is switched using a resistor divider network. No floating supplies are required. A power supply of 12V, referenced to the high voltage d.c., is used to provide positive gate source voltage for n-channel POWER MOSFET. This circuit eliminates the need for logic signal isolation and a floating supply. The disadvantage of this circuit is the high cost of the p-channel drive MOSFET.

Figure 3c illustrates a floating gate drive with a floating supply. This drive is the most expensive out of the three shown in figure 3. However, the floating supply need only have a low output power, since MOSFETs are voltage controlled devices. The advantages of this drive are its high efficiency and unrestricted transistor duty-cycle.

Figure 4 : Bootstrap Supply Techniques.

a) Conventional bootstrap with additional capacitor C1.



b) High efficiency bootstrap.

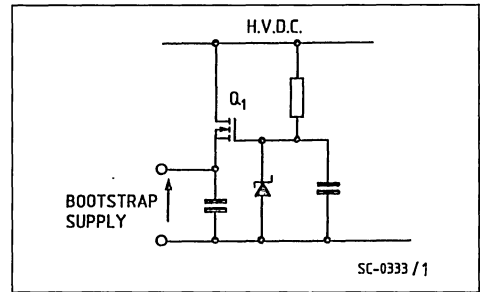


Figure 5 : Isolated CMOS Drive with V_{DS} Control for Short-circuit Protection.

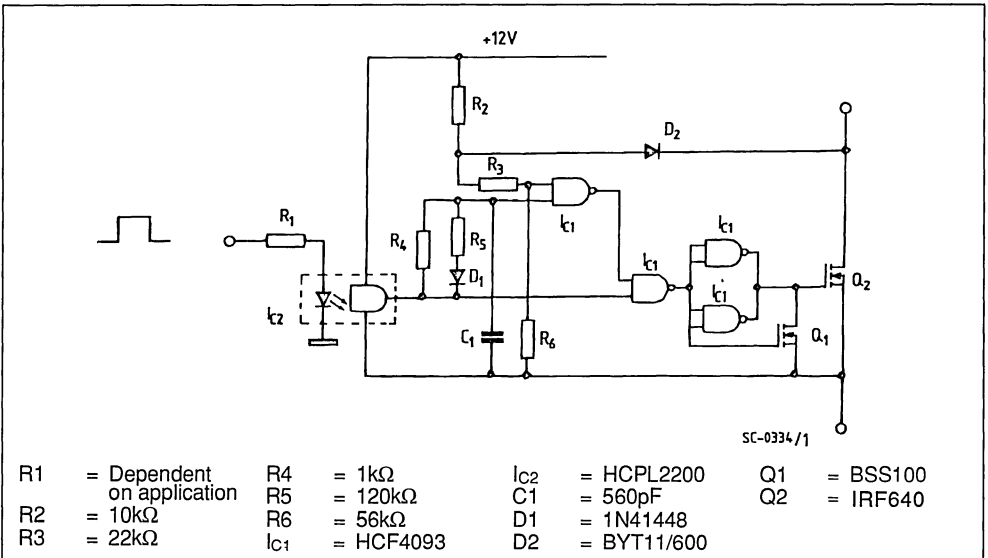


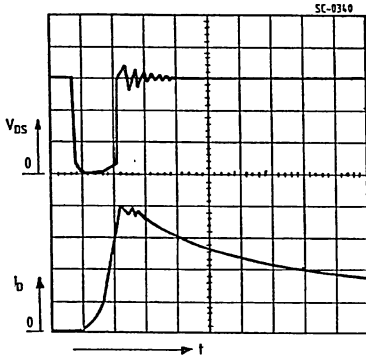
Figure 6 : Short-circuit Conditions for an IRF640
 V_{DS} & I_D .

V_{DS} : 50V/DIV

I_D : 10A/DIV

t : 2 μ s/DIV

a) Output to high voltage short-circuit.



b) Output to Output Short-circuit.



PROTECTION

Power electronic circuits such as bridge-legs are often required to have protection against output to output short-circuit, over-temperature, simultaneous conduction of devices in series in a bridge-leg and output to high voltage supply or ground rail short-circuit. These power stages are generally part of an expensive system such as a machine-tool or a robot motor drive. Thus the additional cost of protection circuitry is commercially acceptable. A compromise is generally reached between equipment costs and the degree of protection required.

Short-circuit protection of a power MOSFET can be achieved by either $V_{DS(on)}$ monitoring or a current sense. In the previous section gate drives using the $V_{DS(on)}$ monitoring technique were presented. Figure 6 illustrates the MOSFET drain to source voltage, V_{DS} , and the drain current, I_D , when short-circuits are experienced by the POWER MOSFET, IRF640, driven by the gate drive illustrated in figure 5.

The MOSFET is turned-off when the drain current increases sufficiently and $V_{DS(on)}$ monitoring is inhibited for a period of 400ns to allow the device to turn-on fully.

An inductor is used in series with the device, as illustrated in figure 1b. This inductor saturates when a large short-circuit current flows. The rate of change of the short-circuit current due to the saturation of this inductor is illustrated in figure 6a and 6b. Figure 6a illustrates the POWER MOSFET drain to source voltage, V_{DS} , and the drain current, I_D , when a bridge-leg output to high voltage supply rail short-circuit occurs. Figure 6b illustrates an output to output short-circuit of two bridge-legs.

Another protection technique uses the "current mirror concept", (1). An image of drain current is obtained by having a small MOSFET, (integral or discrete), in parallel with the main power MOSFET as illustrated in figure 7.

Figure 7 : The Current Mirror.

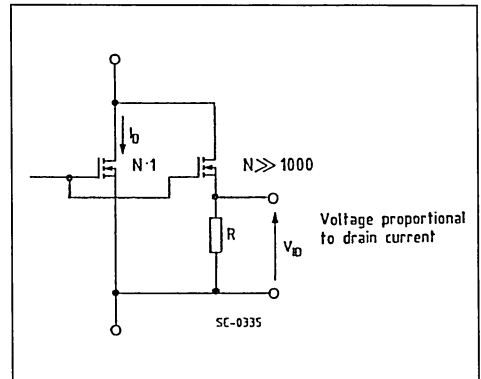


Figure 8 illustrates a floating gate drive which utilizes a pulse transformer for transmitting simultaneously the MOSFET on-signal together and the gate to source capacitance charging current. The current mirror technique is used to provide short-circuit and over-load current protection. The pulse transformer operates at an oscillating frequency of 1MHz when a turn-on control signal is present.

APPLICATION NOTE

The secondary is rectified to provide the gate source capacitance charging voltage. The current mirror provides a voltage "image" of the main MOSFET drain current. This voltage is compared with a fixed reference voltage in order that the gate drive be

latched-off when the drain current becomes in excess of a specified value. Figure 9 illustrates how the MOSFET, SGSP477, is latched-off when the drain current exceeds 10A with this gate drive circuit.

Figure 8 : Pulse Transformer Gate Drive with Current Mirror Protection for an IRF640.

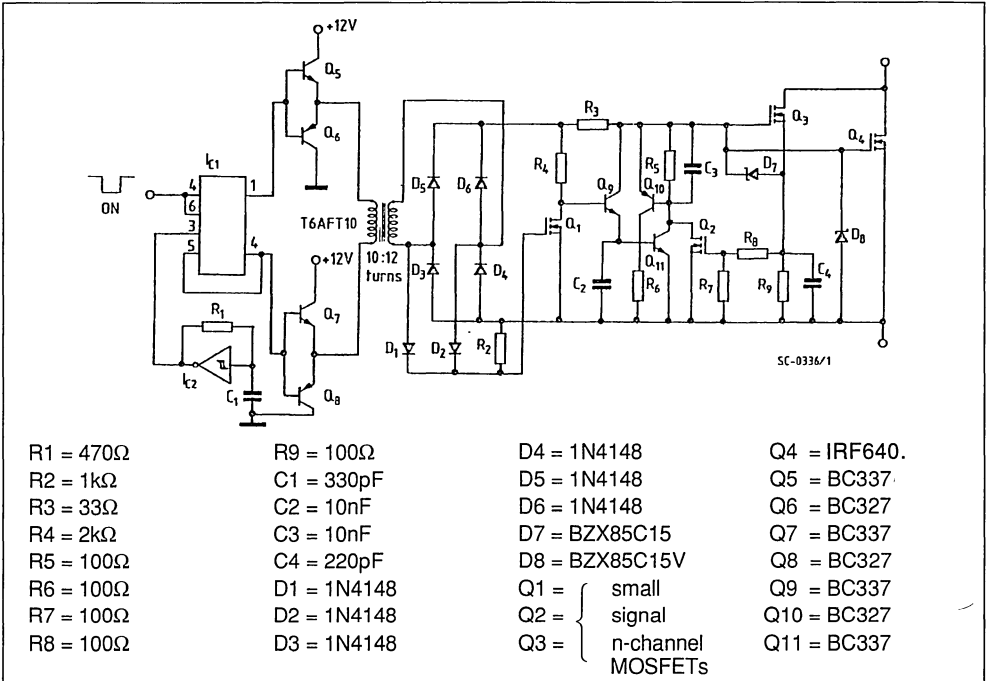
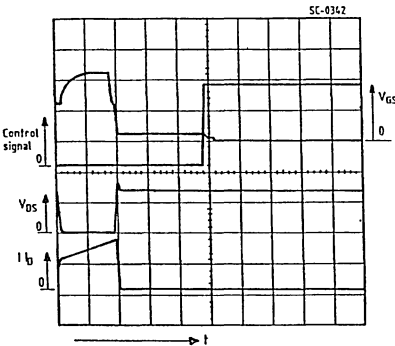


Figure 9 : Overload Current Protection using Current Mirror Concept with the Gate Drive of Figure 8 for an IRF640



Time scale : 5μs/DIV – I_D : 5A/DIV – V_{DS} : 100V/DIV
Control signal : 5V/DIV – V_{GS} : 5V/DIV.

CONCLUSION

MOSFET based bridge-leg configurations requiring protection and floating gate drives have been presented. Novel self-protecting gate drives for the "high-side" and "low-side" switching have been discussed. These drives provide protection against output to high voltage d.c., output to ground and output short-circuit. For the high-side switch "bootstrap" supply gate drive, level shifting gate drive and floating supply isolated gate drives have been compared. Protection against short-circuit condition has been demonstrated using $V_{DS(on)}$ monitoring and the current mirror concept. Both techniques are well suited for protection against short-circuit conditions. However, the current mirror concept also provides a sufficiently linear image of the current for regulation.

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DRIVE CIRCUIT FOR INTEGRATION WITH IGBTs

by C. Licitra, S. Musumeci, A. Raciti, A. Galluzzo, R. Letor, M. Melito

ABSTRACT

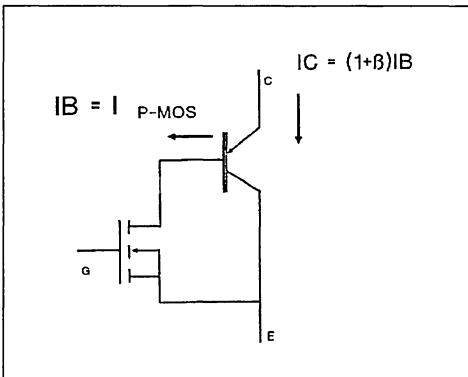
IGBT devices are increasingly used in power electronic equipment due their high power handling capability. The present paper deals with the problems that concern the turn-on, turn-off and short-circuit of these devices. An optimal new driving circuit is proposed that gives excellent device output performance. Experimental oscillogram traces of transient condition tests are given, which clearly demonstrate the advantages of using the new driving circuit. Finally, the suitability of the driving circuit for integration is analysed.

1. INTRODUCTION

Recent developments in industrial power electronic applications have demanded a concerted effort be made to produce new electronic devices, able to handle high currents, voltages and frequencies, as well as being easy to control. Among the innovative new electronic products, IGBTs are increasingly used in high voltage applications, > 500V up to frequencies of 20kHz to 30kHz. Essentially IGBT components have the following characteristics:

- Both turn-on and turn-off capability by means of an applied voltage to the gate requiring only low driving power, equivalent to that which is required by MOSFET structures.

Figure 1. Simplified equivalent circuit of an IGBT



- Low direct voltage drop and high current density like BJT devices.

The former is a very important point because it implies a loss reduction, hence costs decrease in making the driving stage, while the latter makes it suitable for high current applications.

IGBT structures can be represented by means of a simplified circuit using two devices, a MOSFET and a BJT, as shown in Figure 1. IGBTs are very "user-friendly" to drive, but in order to obtain the best performance they require suitable driving techniques [1] [2].

In this paper the most important phenomena occurring during the switching are discussed, with the aim of analysing and optimising the IGBT behaviour. In particular, an original driving circuit is proposed able to function during turn-on, turn-off and short-circuit conditions and is a powerful tool for improving IGBT performance. Moreover, the proposed driving circuit provides suitable protection for avoiding switch failure during stress conditions.

Extensive laboratory tests have been carried out to demonstrate the advantages of the new driving circuit in comparison to the more traditional ones.

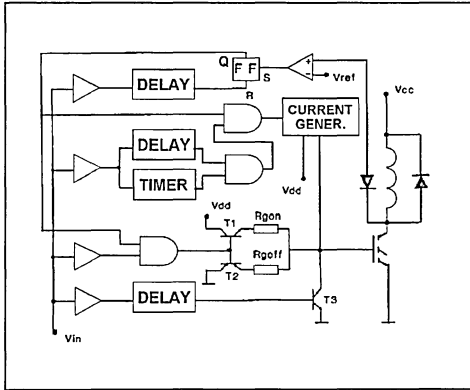
2. THE DRIVING CIRCUIT

The proposed circuit, shown in Figure 2, can be ideally split in three main functional blocks and an output stage. The output stage is a push-pull scheme with separated turn-on and turn-off paths for driving the gate terminal. The main functional blocks contain circuitry for improving turn-on, improving turn-off and providing short-circuit protection.

The following sections explain in more details the behaviour of IGBTs during the transients. A 30A, 500V IGBT was used in the laboratory tests. Its main characteristics are:

- $V_{CES} > 500V$ @ $I_C = 250\mu A$
- $V_{CE(sat)} < 3.3V$ @ $I_C = 30A$ and $V_g = 15V$
- $C_{iss} = 2500pF$ typical
- $C_{oss} = 330pF$ typical
- $C_{riss} = 80pF$ typical

Figure 2. Schematic of IGBT drive circuit



2.1 Turn-on

The dynamic behaviour of an IGBT is affected by the unavoidable parasitic capacitances of the structure, often referred to as C_{ge} , C_{ce} and C_{cg} . They are shown in Figure 3. Such parasitic capacitances together with stray inductances, gate bias, and driving impedance define the device performance in terms of switching speed and power losses.

The switching speed of a device having an insulated gate, i.e. voltage driven, is strictly related to the rate of supplying charge to the gate input capacitance [3]. This is true for IGBTs too, except during the falling edge of the collector current. The target of the device designer is to obtain a switching speed fast

enough to reduce power losses without any increase in electromagnetic interference.

During turn-in in inductive load switching, the power losses mainly depend on both the di/dt , which influences the peak current due to the diode recovery, and the dynamic saturation voltage phenomenon. Moreover, the di/dt influences the EMI [4]. In the circuit of Figure 4, the voltage drop caused by the stray inductance L_{s1} of the emitter ground connection, reduces the drive current I_g that is defined by the equation:

$$I_g = (V_d - V_g - (L_{s1} \times di/dt)) / R_g \quad (1)$$

and moreover acts as a negative feedback during the current rise time. Taking into account the effect of L_{s1} , the di/dt gradient can be calculated by the relationship:

$$di/dt = V_d - V_{th} / (R_g C_{ge} / G_{fs}) + L_{s1}$$

where V_{th} , C_{ge} , and G_{fs} depend on the particular device; L_{s1} , and V_d are fixed by the circuit. The only way to manage the di/dt is to act on the gate resistance. In order to reduce the EMI it is better to reduce di/dt by increasing R_g , but that means reduction of the switching speed and hence increased power losses [5]. To solve the problem described above, the proposed circuit acts as follows. The initial gate current is fixed by adjusting $R_{g(on)}$ in agreement with both device electrical specifications and EMI requirements. When the collector current reaches its maximum value, the collector voltage starts to decrease and in this condition the circuit

Figure 3. Parasitic capacitances affecting the dynamic behaviour of IGBTs

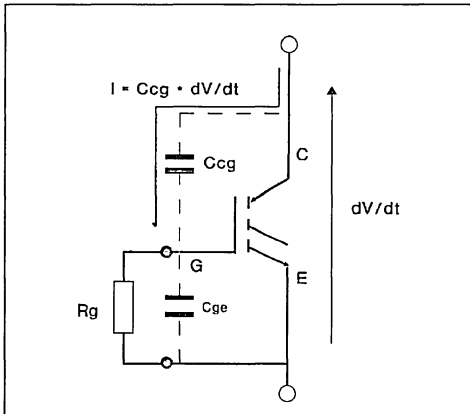
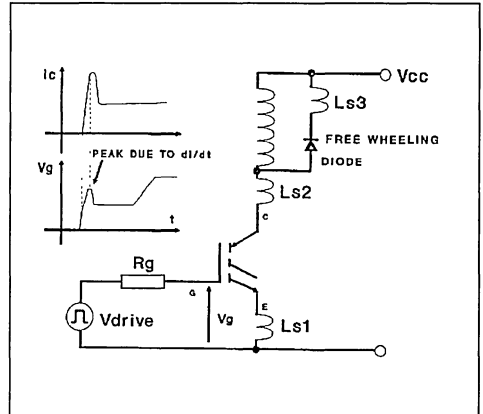


Figure 4. Parameters influencing di/dt at turn-on



enables a current generator. The current generator increases the gate current making the collector voltage fall faster and so eliminating the dynamic saturation voltage phenomenon. The delay between the positive edge of input signal and the duration of the enable signal of the current generator are both adjustable and so the best match between driving circuit and device is obtainable. Figure 5 shows the gate and collector waveforms at turn-on with traditional driving (i.e. only gate resistance), whereas figure 6 shows the same waveforms when the proposed driving circuit is used.

Note that the di/dt is the same, $200A/\mu s$ whilst the cross-over time is reduced by about 50%.

Figure 5. Turn-on with conventional drive circuit

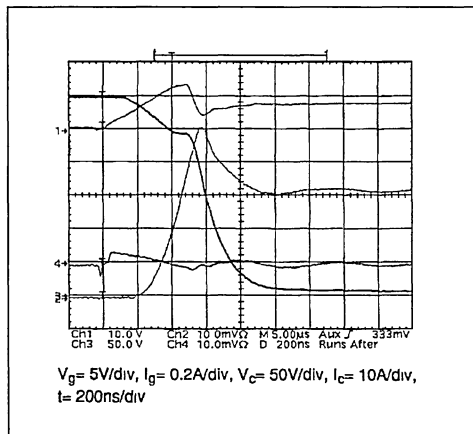
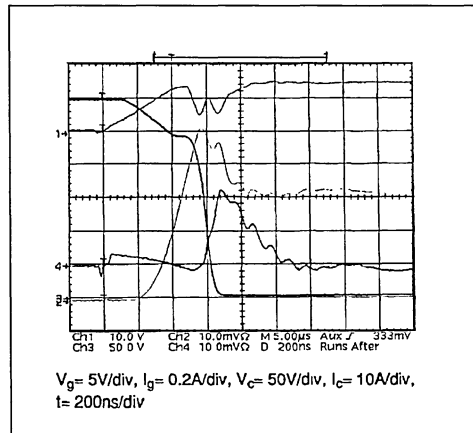


Figure 6. Turn-on with improved drive circuit



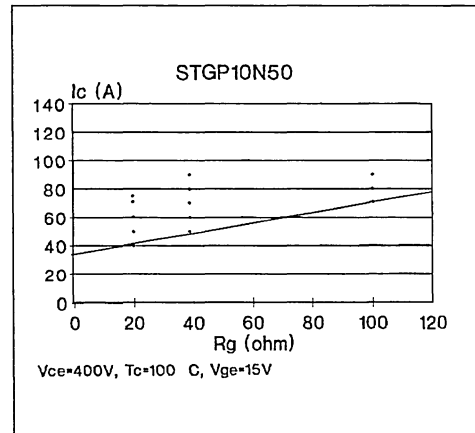
2.2 Turn-off

At turn-off the gate voltage starts to decrease from V_d until it reaches the "Miller" value. At the same time the collector voltage increases slightly as shown by the output characteristics with $I_c = \text{constant}$. At this point the collector voltage increases rapidly to its maximum value, causing the modulation of the collector-gate capacitance (Miller effect). During the Miller effect V_g is constant. Then, the collector current begins to fall quickly, due to the turn-off of the IGBT PMOS part and thereafter it continues with a tail due to the recombination of minority carriers in the substrate - this is the turn-off phase of the PNP transistor with open base. This tail, responsible for major losses, is strongly related to the device construction technology, and its effects cannot be reduced by means of the driving circuit.

Turn-off losses can be only controlled during both the Miller effect and the PMOS turn-off phases and with the aim being to reduce losses it is necessary to decrease the value of R_g [6]. As consequence of a reduction in gate resistance, dv/dt increases and so losses decrease, but it is necessary to take care not to exceed the RBSOA limits. In fact, the latching current and the RBSOA are strongly related to dv/dt , i.e. with the value of R_g . Figure 7 shows how the latching current depends on the gate resistance value. The manufacturer guarantees the RBSOA with a carefully specified R_g minimum value.

Based only on the above criteria, the gate impedance in bridge configurations has a high value, making

Figure 7. Latching current versus gate resistance



the circuit susceptible to spurious turn-on of the IGBTs, if an excessive dv/dt occurs across one of the devices in the off-state [7]. In fact, the voltage drop across the gate impedance, due to the current that flows through C_{CG} , figure 3, can reach the threshold voltage and so switch-on the device. Figure 8 shows the spurious turn-on phenomenon, when the device under test is subjected to a dv/dt of $2kV/\mu s$. In this case the energy lost has been calculated as about $350\mu J$.

At turn-off the proposed circuit acts only through $R_{g\ off}$, that is fixed in agreement with the device electrical specifications. During the off-state phase, the proposed driving circuit avoids the spurious turn-on by reducing the gate impedance by a large amount, so preventing the gate voltage from reaching the threshold voltage. Such transient phenomenon is evident in Figure 9, which shows the IGBT improved waveforms under the same test conditions of figure 8, $2kV/\mu s$. Note that the collector current trace shown in figure 9 is not due to spurious turn-on, but it is the unavoidable current necessary to charge the output capacitance of the device.

2.3 Short-Circuit

When a short-circuit occurs in the collector path, the current starts to increase until it reaches its maximum value, that is defined by the supply voltage, the gain of the device and the gate voltage. The devices that have good current performance, i.e. high gain, can fail under short circuit stresses and hence they need to be protected [8]. The presence of high voltage

and high current simultaneously into the device, causes instantaneous very high power losses, consequently the device temperature increases. If the stress duration exceeds that specified in the data sheet, failure occurs. The proposed circuit operates by reducing the conduction time when a short circuit is detected by a high voltage, fast recovery diode that senses the IGBT desaturation [9]. An adjustable time delay inhibits the protection at turn-on, in order to allow for inrush currents. The relevant traces of current and various voltages during a short-circuit transient are shown in figure 10. From these it is evident how the protection block operates

Figure 9. Improved behaviour with new drive circuit in presence of di/dt

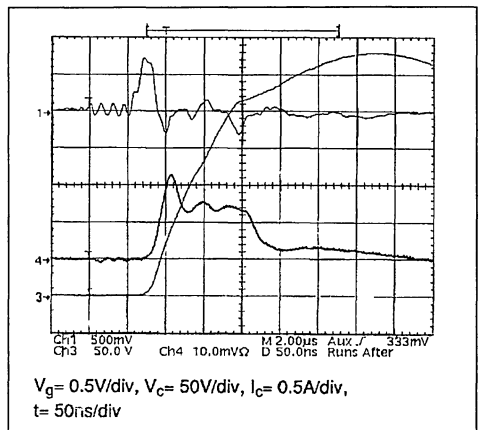


Figure 10. Traces during operation of short-circuit protection

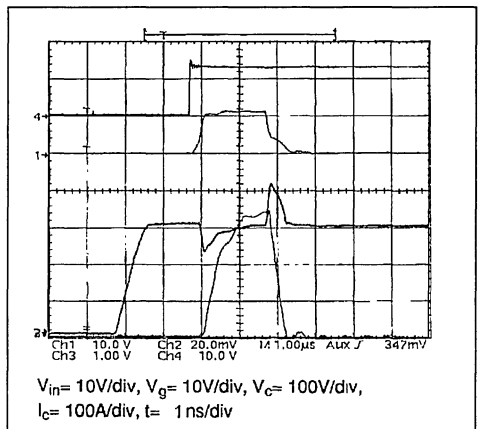
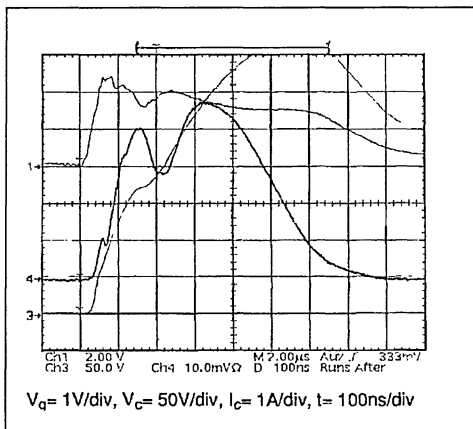


Figure 8. Traces during spurious turn-on caused by $2kV/\mu s$ dv/dt



preventing the fail condition. Note that the current peaks above 300A during the protection inhibit period due to the high current gain.

2.4 Integration

The proposed circuit has been developed having as the target its possible integration. In the case of driving circuit integration separated from the power device, bipolar or BCD technologies can be used, taking into account the necessity to provide external delay adjustments, in order to match it to several different devices. At the present time, integration of the driving circuit and power stage on the same chip is possible with VI Power technology using a Power MOSFET output stage. It has not yet been accomplished using IGBT output stages.

CONCLUSIONS

The characteristics of an optimal driving circuit for IGBT devices have been analysed. Experimental evaluation of IGBT performance has been carried out with both traditional and new driving circuits. The aim has been to demonstrate the advantages of the new proposals. The most important results obtained can be summarised as follows:

- in turn-on conditions the circuit provides separate control of the voltage and current gradients, so reducing both power losses and EMI,
- in turn-off conditions, the spurious triggering caused by sharp voltage gradients are avoided by means of a low impedance path offered by the driving circuit. Thus the power losses related to switching are reduced to a minimum value due to the output parasitic capacitance,
- in short-circuit conditions, the device is protected and turned-off in a preset time depending on the maximum time fixed by the manufacturer,

The new circuit can also be used to drive Power MOSFET devices with the same performance. Overall the results obtained have shown that the proposed driving circuit makes the IGBT perform in a manner that gives increased efficiency and higher reliability.

ACKNOWLEDGEMENTS

This work has been supported by the Italian National Research Council, P.F. MADESS, and Ministry of Development of Southern Italy within the Microelectronic Research Group.

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**DRIVE, CONTROL and PROTECTION
PROTECTION**

PROTECT YOUR TRIACS

By P. Rault

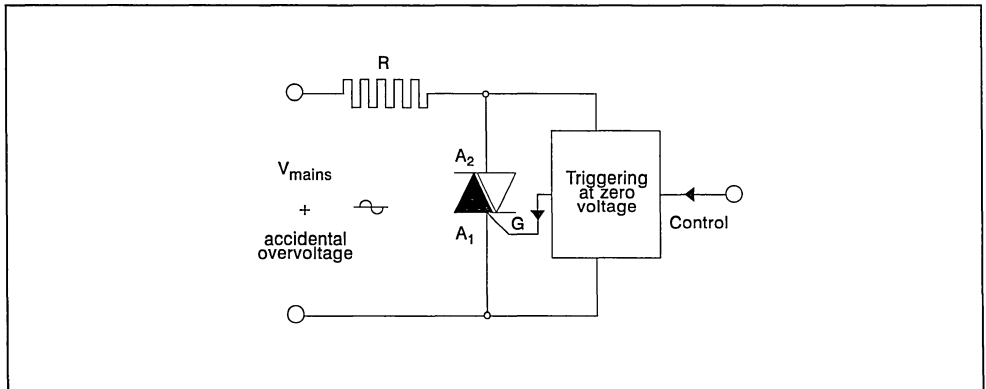
In most of their applications, triacs are directly exposed to overvoltages transmitted by the mains. When used to drive resistive loads (temperature regulation), it is essential to provide them with efficient protection.

WHY PROTECTION ?

In a typical circuit (figure 1), an overvoltage superimposed on the network voltage can turn on the triac by exceeding its avalanche voltage.

Figure 1 : Typical Circuit.

The triac is directly connected to the distribution network : risk of damage



WHAT WE PROPOSE

The principle of the protection which we have studied consists of turning on the triac by the gate as soon as the voltage across it exceeds a certain value (figure 2), thus ensuring a high level of safety. To do this we use a bidirectional TRANSIL diode whose current/voltage characteristic is shown in figure 3.

When the voltage applied to the triac reaches the VBR voltage of the TRANSIL, the latter conducts, producing a current in the triac gate and turning it on (figure 4). The triac continues to conduct till the half cycle current passes through zero (figure 5).

Figure 2 : Protection of the Triac by a Bidirectional TRANSIL Diode.

The Triac is turned on by gate current (i) as soon as voltage A2 exceeds the voltage V_{BR} of the TRANSIL.

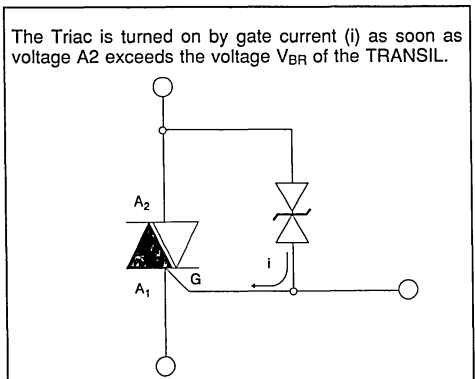


Figure 3 : Voltage-current Characteristic of a TRANSIL Diode.

V_{BR} Specified at 1mA (tolerance 5 or 10%)

V_{CL} limitation voltage is given for a high I_{pp} current level (from several amperes to several tens of amperes, depending on the type).

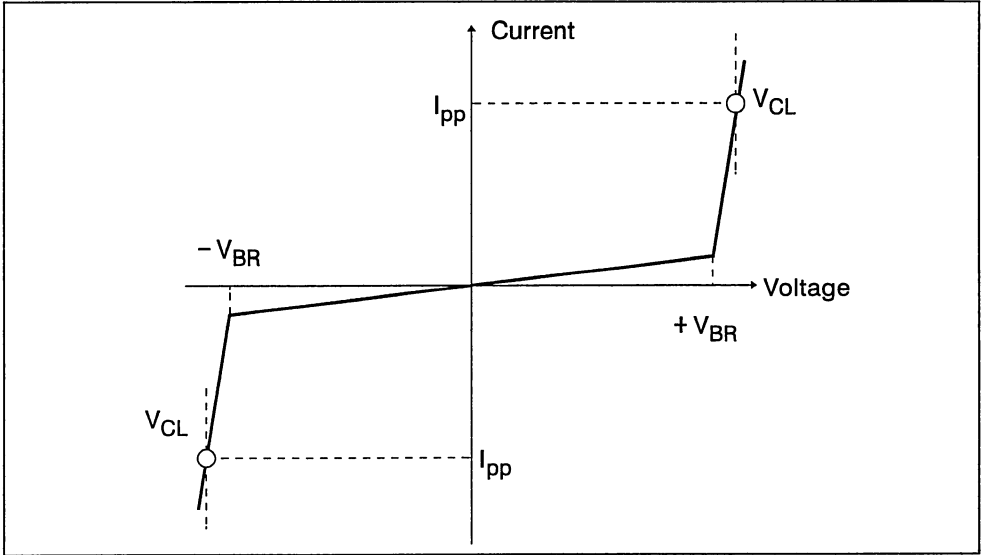


Figure 4 : Characteristic of the TRIAC + TRANSIL Assembly. Case of a 600V/12A triac protected by a 440V TRANSIL diode (the dotted line gives the characteristic of the triac alone)

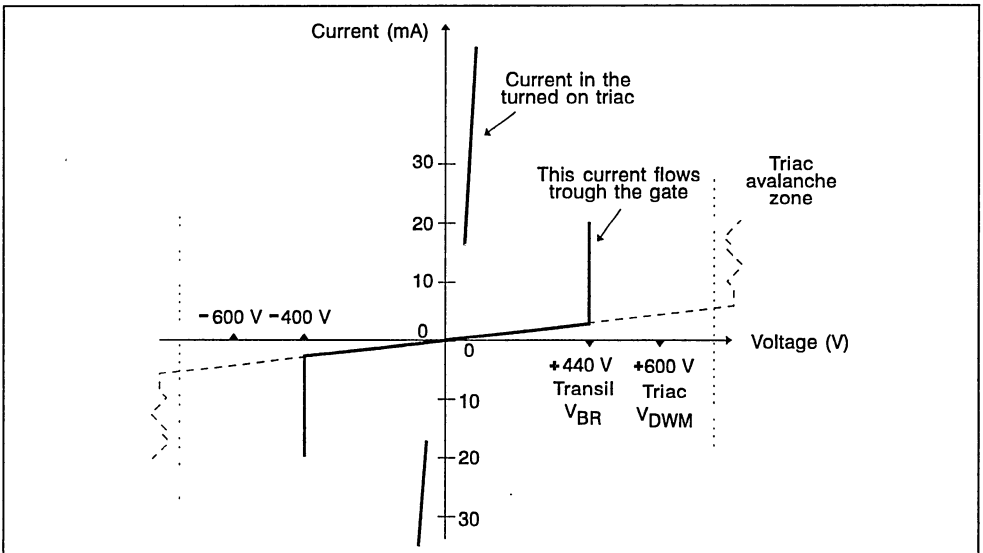
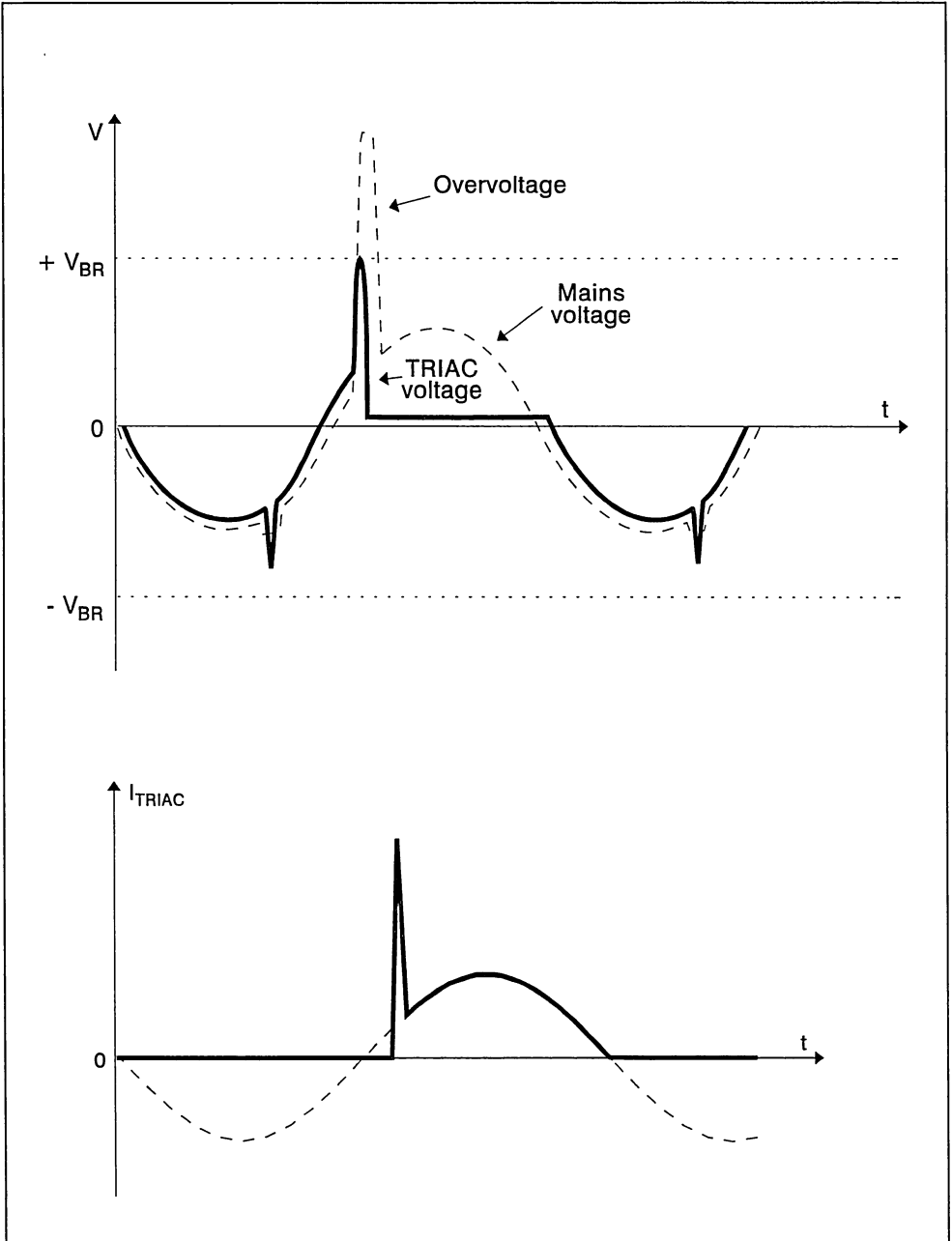


Figure 5 : Behaviour of a Triac Protected by a TRANSIL Diode (the triac is turned on by the gate at the beginning of the overvoltage and continues conducting through the rest of the half-wave)



THE ADVANTAGES OF THIS SOLUTION

- The triac will always operate within the voltage limits given by the manufacturer (VDWM) and thus far from the avalanche zone.
- Not much power is dissipated in the triac during the disturbance before the turn-on, the dissipated power is localized in the protection component (the TRANSIL is made for that !).

The triac is turned on by a gate current which will ensure optimal di/dt conditions.

THE RESULTS

We have carried out tests with repetitive overloads (1Hz) under various conditions : Exponential shock waves of about 1ms, calibrated in voltage (up to 2000V) and controlled in di/dt (500 A/μs max). The tests were carried out with steep-edged voltage pulses (dV/dt > 1000 V/μs) and also with gradual slopes (< 50 V/μs). All these tests were successful : zero failure.

SELECTION OF THE TRANSIL DIODE REQUIRED FOR PROTECTING A TRIAC

VOLTAGE : V_R

Obviously the triac associated with the TRANSIL diode should not be turned on by the maximum mains voltage. An additional safety margin should be given to prevent untimely turning on by the small voltage spikes, often repetitive, which are always present on a "normally" disturbed mains line.

$$V_R > V_{\text{mains}} \times \sqrt{2} + \text{safety margin.}$$

In the absence of accurate specifications, add 20% for the safety margin.

Example : 220V network :

$$V_R > 220 \sqrt{2} + 20\% = 375V$$

POWER

The TRANSIL only conducts when turning on the triac ($t \approx 1\mu\text{s}$).

The current during this time can reach very high levels (several tens of amperes) in the case of disturbances with steep edges (> 1000V/S), however the dissipated power remains well within the capability of TRANSILS.

The BZW 04(400W/1ms) is suitable for all cases.

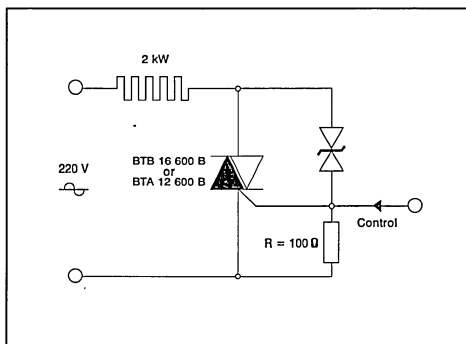
PRACTICAL EXAMPLE

Drive circuit for a 2kW heating element on 220V mains (figure 6).

The BZW 04.376B type TRANSIL perfectly protects the BTB 16.600B triac (VDWM = ± 600V).

The 100 Ω resistor, R, between the gate and A1 is not absolutely indispensable, but it preserves the dV/dt characteristic of the triac which would be reduced (by about 20%) by the junction capacitance of the TRANSIL between anode and gate.

Figure 6 : Practical Example of the Protection of a 12 or 16A Triac against Overvoltages



CONCLUSION

With the protection circuit proposed, the triac always operates under perfectly defined conditions in case of overvoltages :

- The voltage remains limited to the maximum specified for the triac
- Turn-on is ensured by a gate current.

This circuit, which we have tested in a number of different setups (different lads, high amplitude overvoltages, disturbances of long duration, etc...), enables a considerable increase in the reliability of circuits using triacs and is indispensable for driving resistive loads on highly disturbed networks.

TRANSIL CLAMPING PROTECTION MODE

By Jean Marie Peter

INTRODUCTION

The Transil is an avalanche diode specially designed to clamp overvoltages and dissipate high transient power. A Transil has to be selected in two steps :

A) Check that the circuit operating conditions do not exceed the specified limit of the component.

- . For non-repetitive "shock" operation,
- . For repetitive load operation,
- . For continuous operation.

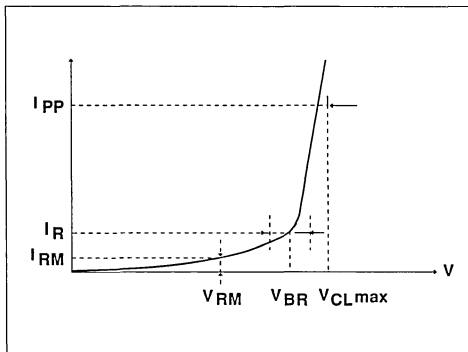
B) Check that the maximum value of the clamped voltage under the most adverse conditions corresponds to the specification of the circuit, i.e. there is no danger for the protected circuits.

REVIEW OF TRANSIL CHARACTERISTICS

1. THE PEAK REVERSE VOLTAGE V_{RM} is the voltage which the Transil can withstand in continuous operation.

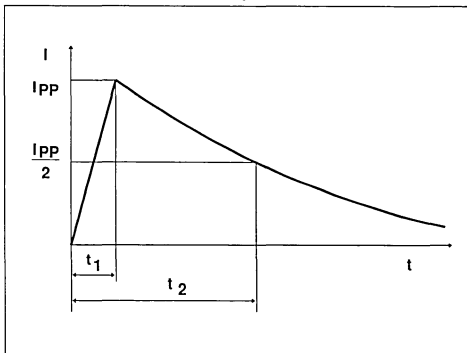
2. THE BREAKDOWN VOLTAGE OR KNEE VOLTAGE V_{BR} is the voltage value above which the current in the Transil increases very fast for a slight increase in voltage. The breakdown voltage V_{BR} is specified at 25°C and its temperature coefficient is positive. The V_{BR} tolerance is normally $\pm 5\%$ or $- 5\% + 10\%$, however it is important to note that Transil technology results in much lower tolerance in mass production than other technologies.

Figure 1 : Main Characteristics of a Transil.



3. THE CLAMPING VOLTAGE V_{CL} as specified in the data-sheets is the maximum value for a "standard" current pulse with a peak value of I_{PP} , specified for any type of Transil (fig.2). If the Transil is subjected to a different pulse, the value of V_{CL} can be calculated using the application note "CALCULATION OF TRANSIL APPARENT DYNAMIC RESISTANCE". The clamping factor is represented by V_{CL}/V_{BR} . This ratio between the maximum value of overvoltage for a given current and the maximum voltage which the diode can withstand in continuous operation characterizes the degree of protection.

Figure 2 : Standard Exponential Pulse. This type of pulse corresponds to most of the standards used for the protection device.



	t_1 μs	t_2 μs
WAVE "8/20 μs "	8	20
WAVE "10/1000 μs "	10	1000

4. TRANSIL PEAK POWER DISSIPATION

The first protection devices, designed to meet electrotechnical standards, were mostly used for overvoltages of short duration (1/50 μs waves of the type shown in fig.2) encountered on high voltage lines.

APPLICATION NOTE

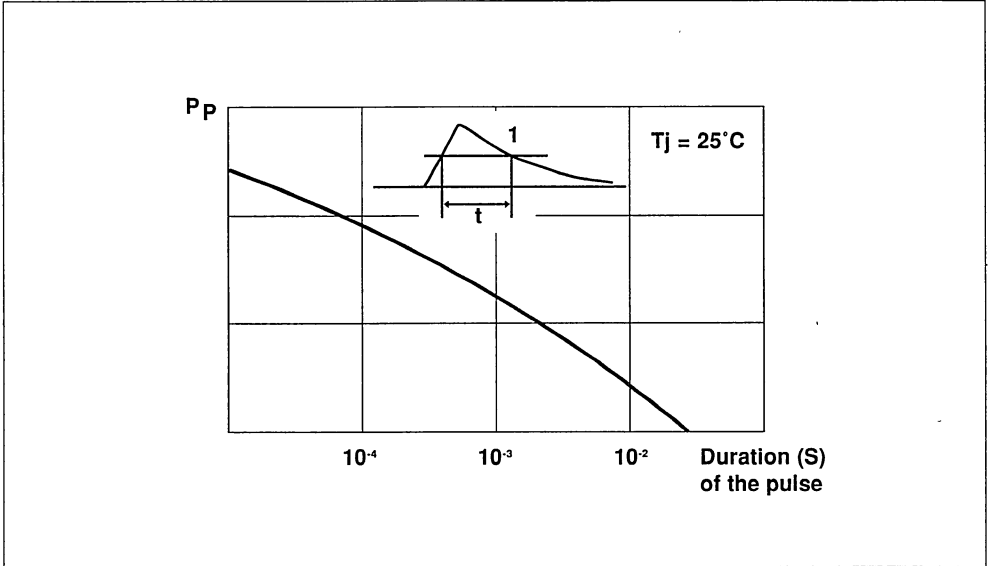
Research carried out by CNET (French Telecommunications Agency), confirmed by other organisations, tends to show that low-power electronic equipment is subjected to over voltages of a much longer duration, better represented by a 10/1000 μs exponential wave.

Transils are meant to protect electronic equipment and hence have been designed to

perform well for over voltages which last several tens of milliseconds.

The performance of Transils has thus been determined with reference to the standard exponential wave 10/1000 μs .

Figure 3 : Maximum Power for an Exponential Pulse of Duration t.



The peak power dissipated in the Transil is given by :

$$P_P = V_{CL} \times I_{PP}$$

This maximum corresponds to non-repetitive operation. If the pulse has a different duration, a curve similar to that in fig.3, provided in the datasheets, enables the specifications of the Transil to be determined.

If the initial temperature exceeds 25°C, the power (P_P) should be reduced in accordance with the curve of fig.4 which is the same for all Transils.

If the current surge through the Transil is not exponential, the diagrams of fig.5 should enable the equivalent exponential pulse to be calculated.

Figure 4 : Variation of Peak Power as a Function of the Initial Temperature.

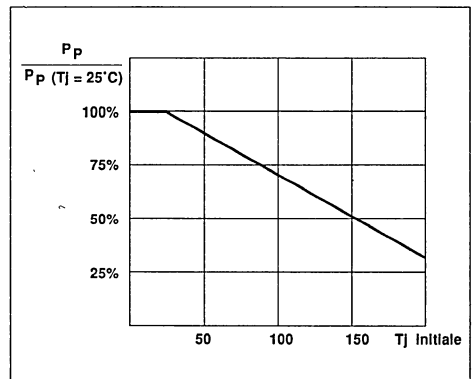
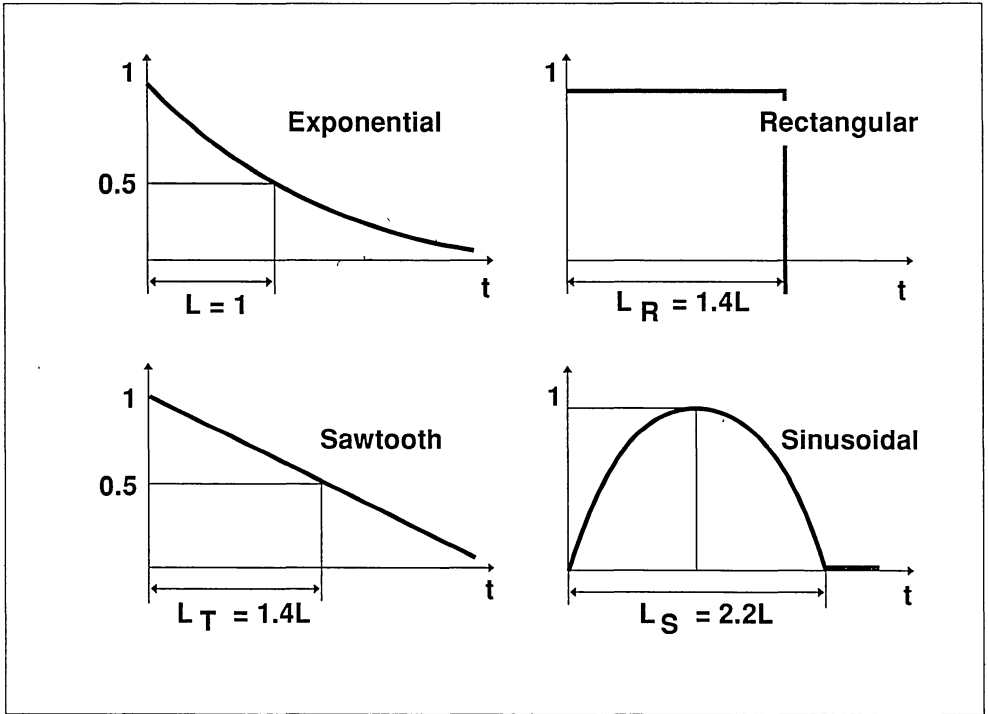


Figure 5 : The four pulses shown below, each of the same peak value, result in identical power being dissipated in a Transil. For example, the rectangular pulse which gives the same dissipation as the exponential pulse of the same peak value is 1.4 times longer in duration.



5. TRANSIL MEAN POWER DISSIPATION

In repetitive operation, the specification to be considered is mean power P_{AV} .

$$P_{AV} = f \times W$$

(f : frequency, W : energy dissipated at each pulse)

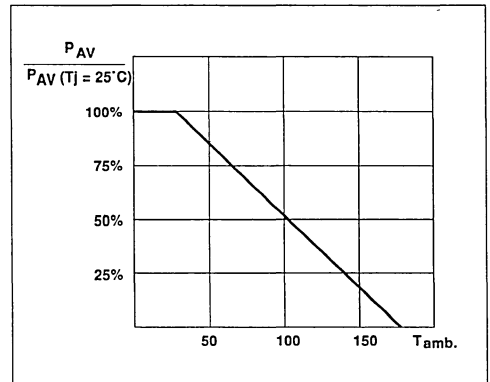
The junction temperature calculated from this power should never exceed the specified maximum junction temperature.

This temperature is calculated from the thermal resistance, exactly like for a diode.

$$T_J = T_{amb} + R_{th} \times P_{AV}$$

$$R_{th} = R_{th(j-a)} \text{ for axial lead Transil}$$

Figure 6 : Maximum Average Power as a Function of Ambient Temperature.



6. SPEED

The primary purpose of a Transil is to clamp overvoltages produced by current surges.

A conventional lightning arrester system only responds with a certain delay which can reach 2 μ s. A metal oxide varistor does not respond immediately either (delay of about 25 ns).

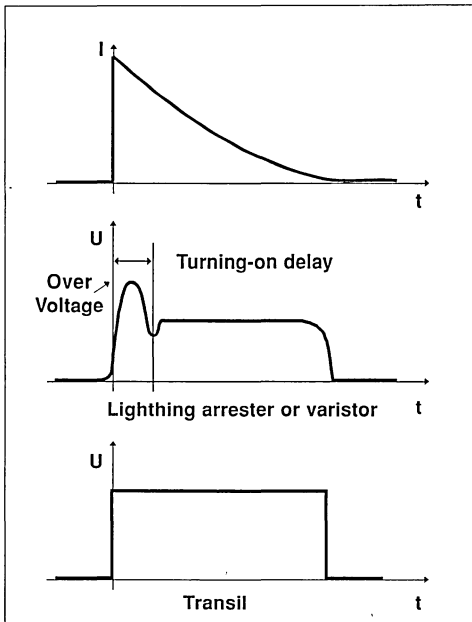
If a current with a very low rise time flows through these components, an overvoltage could appear before the device reacts.

In the case of a Transil, the avalanche phenomenon of a silicon diode is extremely fast (theoretical value about one picosecond).

Laboratory tests have never succeeded in producing overvoltages across Transils, even by using special devices producing very steep current gradients (dischargers, mercury relays).

In conclusion it can be said that Transils respond instantaneously in clamping, on condition that di/dt overvoltages are not introduced by connection inductances.

Figure 7 : Voltage Response of a Classical Component used for Protection and a Transil.



The low capacitance Transil and the bidirectional models have clamping times of about 5 ns. These times remain negligible for practically all applications.

7. SPEED IN "DIODE" OPERATION.

A Transil operating as a rectifier is not a fast recovery diode (it has a high stored charge). As a result, Transils cannot be used for the rectifier function instead of fast recovery diodes.

On the other hand, a Transil operating as a diode has very low forward recovery time (and a very low forward peak voltage VFP). This property can be used for particular applications since no other existing diode has a lower turn-on time for a given VBR (or VRM) voltage.

8. CALCULATION EXAMPLE

Figure 8 : Behaviour of a Transil Operating as a Diode at Turn-off.

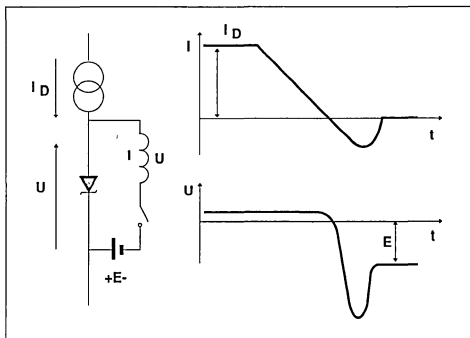
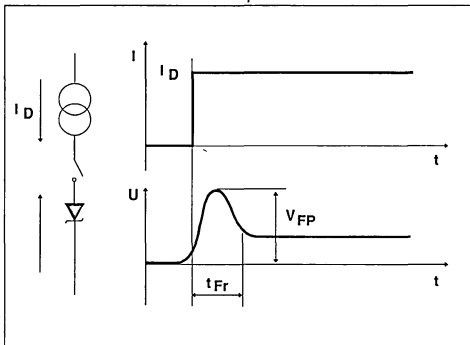


Figure 9 : Behaviour of a Transil Operating as a Diode at Turn-on.

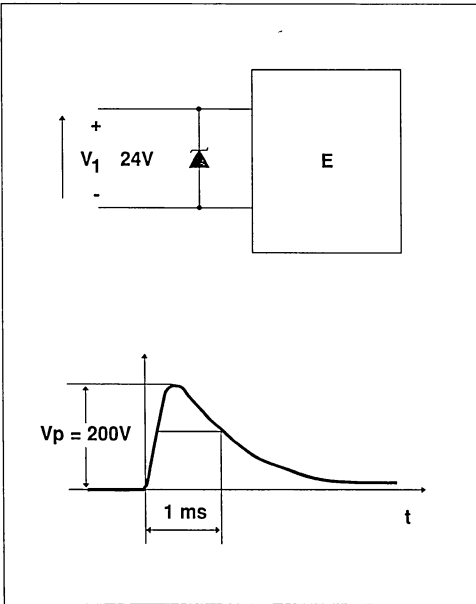


8.1. NON-REPETITIVE SURGES.

A source (V_1) with a rated voltage of 24 V supplies equipment E which is to be protected against overvoltages. This source is subjected to random non repetitive exponential overvoltages with amplitudes of 200 V and a duration of 1 ms at 50% (standard wave) (see fig.10). The equivalent internal impedance Φ of the source with respect to 1 ms exponential waves is 13 Ω .

The maximum ambient temperature is 80°C. In no circumstances should equipment E be subjected to a voltage higher than 50 V.

Figure 10 : Protected Equipment And Surge



Assuming that there is a Transil which meets this criterion, an initial calculation of the Transil power can be made.

$$P_P = V_{CL} \times I_P \text{ where } I_P = \frac{V_P - V_{CL}}{\Phi}$$

$$I_P = \frac{+200 - 50}{13} = 11.5A$$

$$P_P = 50 \times 11.5 = 575W$$

This power corresponds to an operating temperature of 80°C. The data sheets indicate power at 25°C so we have to correct the power according to the curves of admissible power versus initial temperature.

So we obtain :

$$P_P (25^\circ C) = \frac{P_P (80^\circ C)}{0.8}$$

$$P_P (25^\circ C) = \frac{575}{0.8} = 719W$$

8.1.3. Selection of the Transil.

We can now establish an initial specification of the Transil to use.

$$V_{RM} \geq 29V$$

$$V_{CL} \leq 50V \text{ for } I_P = 11.5V$$

$$P_P (25^\circ C) = 719W/1ms$$

The type corresponding to these characteristics is the 1.5 KE 36 P.

$$V_{RM} = 30.8 V$$

$$V_{BR \text{ nom}} = 36 V ; \text{ min } 34.2 V ; \text{ max } 39.6 V$$

$$V_{CL \text{ max}} = 49.9 V \quad I_{PP} = 30 A$$

$$P_P = 1500W/1ms$$

$$\alpha_T = 9.9 \times 10^{-3}$$

8.1.4. Determination of the clamping voltage V_{CL} .

To determine the voltage V_{CL} at 11.5 A, we can use the I_{PP}/V_{CL} parameters included in the 1.5 KE data sheets.

$$V_{CL \text{ at } I_P} \approx V_{BR \text{ max}} + R_D \times I_P$$

8.1.1. Selection of the protection voltage

In the absence of specific information, we assume that voltage V_1 varies by $\pm 20\%$, i.e. between 20 V and 29 V.

The protection voltage V_{RM} of the Transil should then be greater than or equal to 29 V.

8.1.2. Predetermination of the peak power P_P

The equipment E cannot withstand a voltage above 50 V $\rightarrow V_{CL} \leq 50 V$.

$$R_D \leq \frac{V_{CL} - V_{BR}}{I_{PP}}$$

$$V_{CL} \text{ at } 11.5A \approx 39.6 + \frac{49.9 - 36}{30} \times 11.5 = 44.9V$$

8.1.5. Temperature correction

The voltage at 80°C is :

$$V_{CL} (80^\circ C) = V_{CL} (25^\circ C) [1 + \alpha_T (T_j - 25^\circ)]$$

$$V_{CL} (80^\circ C) = 44.9 [1 + 9.9 \cdot 10^{-4} (80 - 25)]$$

$$V_{CL} (80^\circ C) \approx 47.3V$$

This value is below the 50 V limit. The Transil ensures the protection.

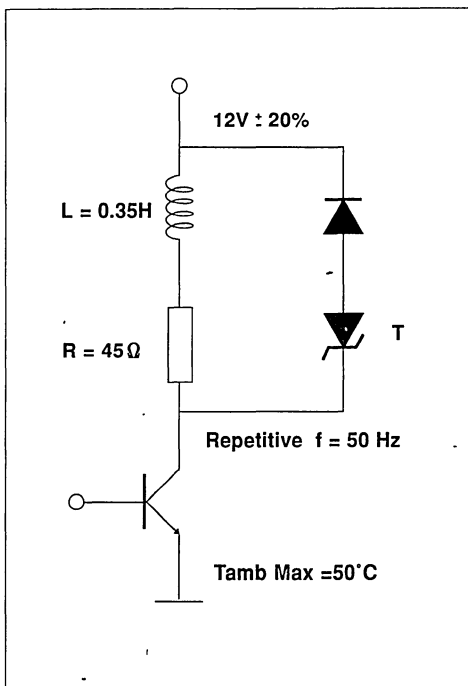
8.2. REPETITIVE SURGE.

We have to protect the transistor shown in fig.11 with a Transil whose clamping voltage, Vcl, does not exceed 85 V.

Calculation method

To avoid a long calculation, we assume :

Figure 11 : Transistor Protection



$V_{CL} \approx V_{BR}$ only true in the case of repetitive surges.

Experience shows this hypothesis is confirmed in most cases with a Transil, therefore a Transil ought to be selected initially according to its thermal characteristics.

8.2.1. PAV

An approximate value can be obtained by supposing that all the energy contained in the inductance is absorbed by the Transil. This hypothesis is close to reality when the ratio

$$\frac{V_{BR}}{V} \text{ is significant.}$$

$$P_{AV} = \frac{1}{2} \times LI^2 f = \frac{1}{2} \times 0.35 \left[\frac{12 + 2.4}{45} \right]^2 \times 50$$

$$= 0.9 W$$

8.2.2. First choice

We choose the type BZW O4P64

$$V_{BR} \text{ max} = 82.5 V$$

$$R_{th} = 100^\circ C/W$$

8.2.3. Tj calculation

$$T_j = T_{amb} + P_{AV} \times R_{th} = 50 + 90 = 140^\circ C$$

This value is compatible with the Transil characteristics.

8.2.4. Determination of VCL

We see on the data sheets that for such a low current level $V_{CL} \approx V_{BR} \text{ max}$

8.2.5. Temperature correction

$$V_{CL} (140^\circ C) = V_{CL} (25^\circ C) [1 + \alpha_T (140 - 25)]$$

$$V_{CL} (140^\circ C) = 92.5 V$$

This value is too high.

8.2.6. Second choice

$$\text{BZW04P58 } V_{BR} \text{ max} = 74.8 V$$

$$V_{CL}(140C) = 83.5 V$$

The Transil BZW04P58 is suitable for this application.

N.B: This example shows that due to the component dispersion, we have to add the variation due to the temperature.

TRANSIL OR VARISTOR

by A. Bernabe

1. INTRODUCTION

Transils and Metal Oxide Varistors (MOVs) are protective components (suppressors).

Table 1 lists their major characteristics and properties.

Table 1. Comparison of the major characteristics of Transils and Varistors

Parameter	Varistor	Transil
Voltage range (V) ¹	14 to 1200	5 to 500
Leakage current @ 25°C, V=V_{RM} ²	Typ. 50µA, Max 200µA	Typ. 0.05µA, Max. 5µA
Capacitance value	200 to 500pF All voltages	200 to 500pF ⁴ @ V = 0 2 to 5 times less @ V=V _{RM}
Temperature coefficient	-0.05% / °C	1% / °C
Operating temperature	-40°C to 115°C	-40°C to 150°C
Response time	Around 10ns	A few ns
Clamping factor ³	1.7 to 3	1.12 to 3
Power dissipation		
1 overload (20µs duration)	1 to 150J	0.1 to 0.7J
10 overloads (20µs duration)	0.4 to 60J	0.1 to 0.7J
Continuous operation	0.3 to 1.3W	1 to 2W

NOTES

- 1) Varistors are available for lower voltage, but their electrical performance is much worse
- 2) V_{RM} = Voltage stand-off
- 3) Clamping factor = V_{CL}, clamping voltage (for Transil at I_{pp}) / V_{BR}, avalanche voltage (@ 1mA)
- 4) These values must be divided by 2 for bidirectional Transils

2. IMPORTANT PARAMETERS

2.1 Clamping

See figures 1 and 2.

The clamping factor characterises the degree of protection offered by the component. As the Transil operates by the mechanism of volume avalanche in the silicon, it limits the voltage (for a given current) to a value lower than that of the Varistor.

2.2 Overload current

2.2.1 Short overloads (< 100µs)

As a general rule the Varistor can stand much higher short-duration currents than the Transil.

2.2.2 Long (> 1ms) or repetitive overloads

As long as its structure, mounting and thermal resistance are taken into consideration, the Transil is better suited to this type of operation, due to the

Figure 1. Comparison of clamping behaviour

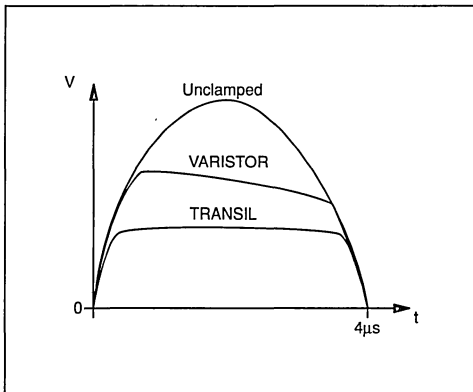


Figure 2. Camp voltage versus overload current

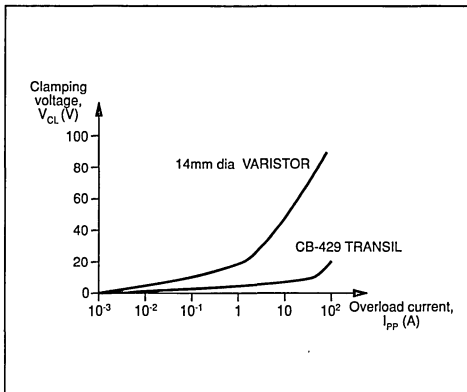


Figure 3. Overload capacity vs. No. of overloads

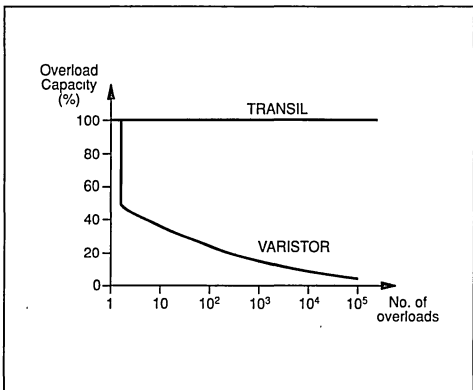
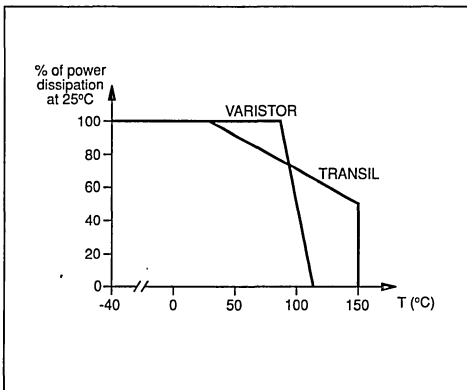


Figure 4. Temperature characteristics



poor medium-power dissipation performance of the Varistor.

2.3 Reliability in overload conditions

See figure 3. After each overload, the structure of the Varistor is changed slightly, leading to a reduction in voltage and an increase in the leakage current. The performance of the Transil on the other hand does not vary depending on the number of overloads experienced (providing the specified maximum amplitude is not exceeded).

2.4 Temperature characteristics

See figure 4. The Varistor maintains 50% of its performance at 85°C, but is not usable above 115°C. The Transil maintains 50% of its performance at 150°C.

CONCLUSIONS

The Transil operates very well as a clipper, and has good long term reliability. It is suited to the clamping and protection of components (e.g. transistors, microprocessors).

The Varistor is a low-cost component which can withstand very high level surge currents for short times. It is best adapted to the protection of electrical equipment (e.g. transformers and motors) from high-level transients.

**TRANSISTOR PROTECTION BY TRANSIL :
DISSIPATION POWER AND SURGE CURRENT DURATION**

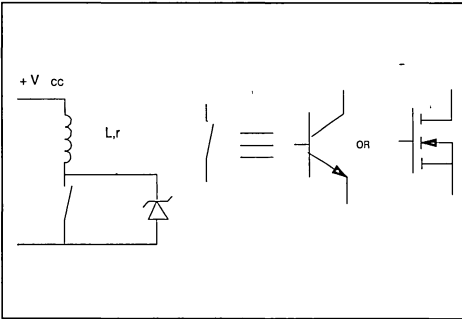
B. Rivet

I - INTRODUCTION

In a great number of applications, we find the diagram FIG.1 where a TRANSIL is used to protect a switch which controls an inductive load. The switch can be a bipolar or a MOS transistor.

The purpose of this paper is to calculate the dissipated power in the Transil and the pulse current duration.

Figure 1 : Basic Diagram

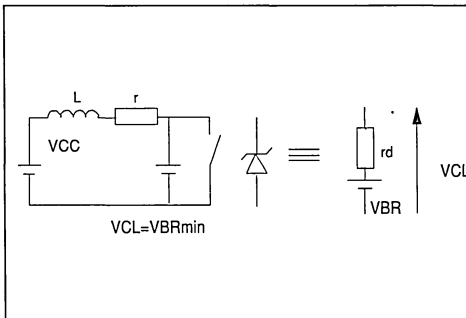


II - CIRCUIT MODELISATION

When the switch turns off we use the equivalent circuit represented FIG.2.

The worst case is to consider $V_{CL} = V_{BR \text{ min}}$. This hypothesis will be used in all formulas.

Figure 2 : Equivalent Circuit



V_{CL} : clamping voltage
 V_{BR} : breakdown voltage
 r_d : apparent resistance

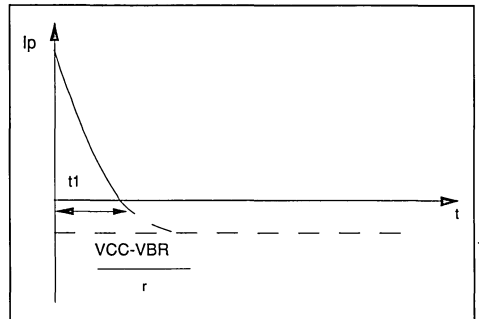
III - CURRENT IN THE TRANSIL

We can express the current i through the TRANSIL by the following formula :

$$i = (I_p + \frac{V_{BR \text{ min}} - V_{CC}}{r}) \exp(-r \frac{t}{L}) + (\frac{V_{BR \text{ min}} - V_{CC}}{r})$$

I_p is the current through the coil when the transistor switches off. The FIG.3 shows the current variation versus time.

Figure 3 : Current Waveform



t_1 can be calculated by

$$t_1 = - \frac{L}{r} \ln \left(\frac{V_{BR \text{ min}} - V_{CC}}{V_{BR \text{ min}} - V_{CC} - r I_p} \right)$$

IV - TRANSIL POWER DISSIPATION

We can consider two cases, single pulse operation and repetitive pulses operation.

a) Single pulse operation

In this case, in order to define a TRANSIL we need peak power P_p and the pulse current standard duration t_p .

P_p is given by

$$P_p = V_{BR \text{ min}} \times I_p$$

APPLICATION NOTE

If we assimilate the pulse current with a triangle the standard exponential pulse duration t_p is calculated by the formula :

$$t_p = - \left(\frac{1,4L}{2r} \right) \ln \left(\frac{V_{BRmin} - V_{CC}}{V_{BRmin} - V_{CC} + rI_p} \right)$$

The energy in the Transil can be expressed by :

$$W = \frac{V_{BRmin} \cdot L}{r} \left[I_p + \left(\frac{V_{BRmin} - V_{CC}}{r} \right) \ln \left(\frac{V_{BRmin} - V_{CC}}{V_{BRmin} - V_{CC} + rI_p} \right) \right]$$

When r tends to zero we find :

$$W = \frac{1}{2} L I_p^2 \left(\frac{V_{BRmin}}{V_{BRmin} - V_{CC}} \right)$$

b) Repetitive pulses operation

In repetitive pulse operation the power dissipation can be calculated by the following formula.

$$P = F \times \frac{V_{BRmin} \cdot L}{r} \left[I_p + \left(\frac{V_{BRmin} - V_{CC}}{r} \right) \ln \left(\frac{V_{BRmin} - V_{CC}}{V_{BRmin} - V_{CC} + rI_p} \right) \right]$$

When r tends to zero we find :

$$P = \frac{1}{2} L F I_p^2 \left(\frac{V_{BRmin}}{V_{BRmin} - V_{CC}} \right)$$

Where F is the commutation frequency.

V - EXAMPLE OF APPLICATION

Commutation of a coil supplied by a battery. The different parameters of the application are :

$V_{CC} = 14V$ $L = 10mH$ $r = 3 \text{ Ohms}$ $I_p = 4A$

TRANSIL : 1.5KE36P $V_{BRmin} = 34.2V$ (cf data sheet)

a) Single pulse

We find

$$P_p = 34.2 \times 4 = 136.8W$$

$$t_p = - \left(\frac{-1.4 \cdot 10 \cdot 10^{-3}}{2 \times 3} \right) \ln \left(\frac{34.2 - 14}{34.2 - 14 + 3 \times 4} \right)$$

$$t_p = 1.08ms$$

The data sheet gives $P_p 1500W$ for $t_p = 1.08ms$ then this 1.5KE36P can be used in this application.

b) Repetitive pulse operation

The commutation frequency is equal to 10HZ so

$$P = 10 \times \left(\frac{34.2 \times 10 \cdot 10^{-3}}{3} \right) \left[4 + \left(\frac{34.2 - 14}{3} \right) \ln \left(\frac{34.2 - 14}{34.2 - 14 + 3 \times 4} \right) \right]$$

$$= 980mW$$

$$R_{th} = 75^\circ C/W \text{ and } T_j \text{ max.} = 175^\circ C$$

$$\text{So } T_j = P \times R_{th} + T_{amb. \text{ max.}}$$

With $T_{amb. \text{ max.}} = 50^\circ C$ we find :

$$T_j = 0.98 \times 75 + 50 = 123.5^\circ C < T_j \text{ max}$$

So we can also use this Transil in repetitive pulse operation.

CIRCUITS and TOPOLOGIES

POWER SUPPLY DESIGN BASICS

by P. ANTONIAZZI

Aimed at system designers whose interest focusses on other fields, this note reviews the basic power supply design knowhow assumed in the rest of the book.

In mains-supplied electronic systems the AC input voltage must be converted into a DC voltage with the right value and degree of stabilization.

Figures 1 and 2 show the simplest rectifier circuits. In these basic configurations the peak voltage across the load is equal to the peak value of the AC voltage supplied by the transformer's secondary winding. For most applications the output ripple produced by these circuits is too high. However, for some applications - driving small motors or lamps, for example - they are satisfactory.

If a filter capacitor is added after the rectifier diodes the output voltage waveform is improved considerably. Figures 3 and 4 show two classic circuits commonly used to obtain continuous voltages starting from an alternating voltage. The Figure 3 circuit uses a center-tapped transformer with two rectifier diodes while the Figure 4 circuit uses a simple transformer and four rectifier diodes.

Figure 1 : Basic Half Wave Rectifier Circuit.

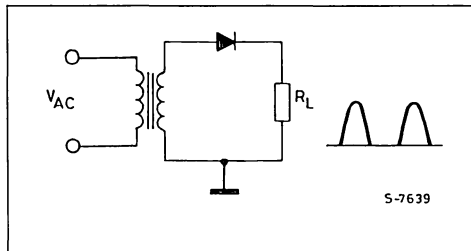


Figure 2 : Full Wave Rectifier Which uses a Center-tapped Transformer.

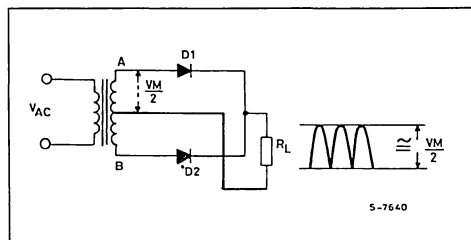


Figure 3 : Full Wave Rectified Output From the Transformer/rectifier Combination is filtered by C1.

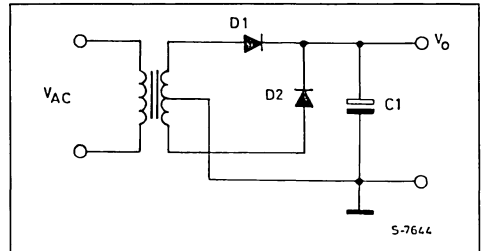


Figure 4 : This Circuit Performs Identically to that Shown in Figure 3.

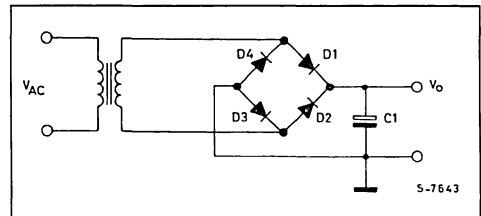


Figure 5 shows the continuous voltage curve obtained by adding a filter capacitor to the Figure 1 circuit. The section b-c is a straight line. During this time it is the filter capacitor that supplies the load current. The slope of this line increases as the current increases, bringing point c lower. Consequently the diode conduction time (c-d) increases, increasing ripple. With zero load current the DC output voltage is equal to the peak value of the rectified AC voltage.

Figure 6 shows how to obtain positive and negative outputs referred to a common ground. Useful design data for this circuit is given in figures 7, 8 and 9. In particular, the curves shown in Figure 7 are helpful in determining the voltage ripple for a given load current and filter capacitor value. The value of the voltage ripple obtained is directly proportional to the load current and inversely proportional to the filter capacitor value.

APPLICATION NOTE

Figure 5 : Output Waveforms from the Half-wave Rectifier Filter.

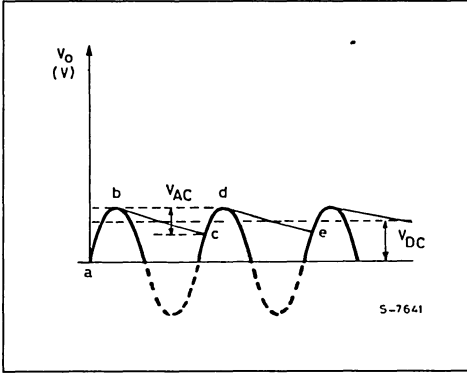


Figure 6 : Full-wave Split Supply Rectifier.

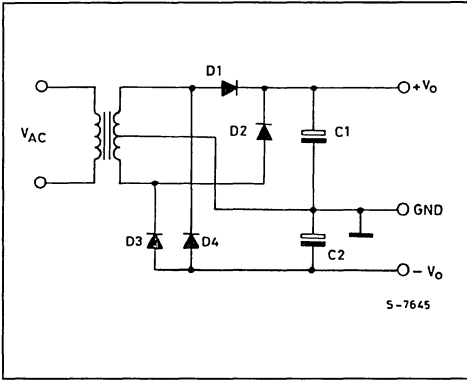


Figure 7 : Ripple Voltage vs. Filter Capacitor Value (full-wave Rectifier).

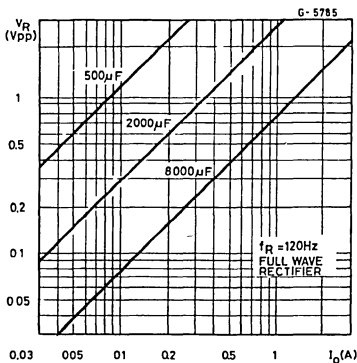


Figure 8 : DC to Peak Ratio for Half Wave rectifiers.

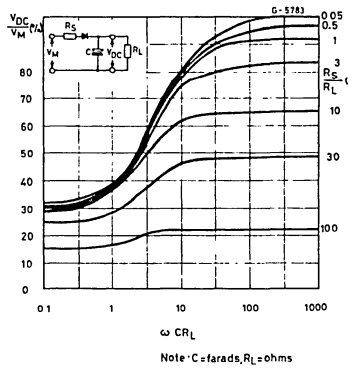


Figure 9 : DC to Peak Ratio for Full-wave Rectifiers.

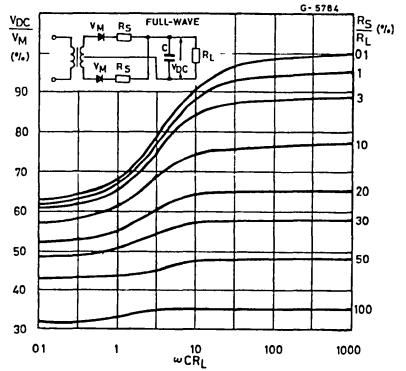


Figure 10 : DC Characteristics of a 50 VA Non-regulated Supply.

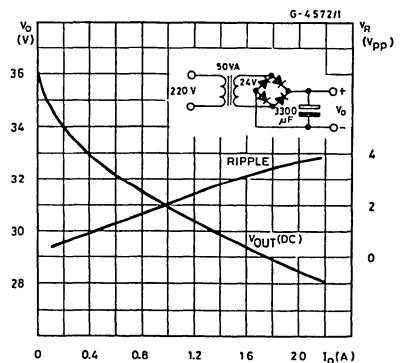


Table 1.

Mains (220V)	Secondary Voltage	DC Output Voltage (V _O)		
		I _O = 0	I _O = 0.1A	I _O = 1A
+ 20%	28.8V	43.2V	42V	37.5V
+ 15%	27.6V	41.4V	40.3V	35.8V
+ 10%	26.4V	39.6V	38.5V	34.2V
	24V	36.2V	35V	31V
- 10%	21.6V	32.4V	31.5V	27.8V
- 15%	20.4V	30.6V	29.8V	26V
- 20%	19.2V	28.8V	28V	24.3V

The performance of a supply commonly used in consumer applications - in audio amplifiers, for example - is described in figure 10 and table 1.

When a low ripple voltage is required an LC filter network may be used. The effect on the output voltage of this addition is shown in figure 11. As figure 11 shows, the residual ripple can be reduced by 40 dB. But often the inductor is costly and bulky.

Often the degree of stability provided by the circuits described above is insufficient and a stabilizer circuit is needed. Figure 12 shows the simplest solution and is satisfactory for loads of up to about 50mA. This circuit is often used as a reference voltage to apply to the base of a transistor or to the input of an op amp to obtain higher output current.

The simplest example of a series regulator is shown in Figure 13. In this circuit the transistor is connected as a voltage follower and the output voltage is about 600 - 700mV lower than the zener voltage. The resistor R must be dimensioned so that the zener is correctly biased and that sufficient base current is supplied to the base of Q1.

For high load currents the base current of Q1 is no longer negligible. To avoid that the current in the zener drops to the point where effective regulation is not possible a darlington may be used in place of the transistor.

When better performance is required the op amp circuit shown in Figure 14 is recommended. In this circuit the output voltage is equal to the reference voltage applied to the input of the op amp. With a suitable output buffer higher currents can be obtained.

The output voltage of the Figure 14 circuit can be varied by adding a variable divider in parallel with the zener diode and with its wiper connected to the op amp's input.

The design of stabilized supplies has been simplified dramatically by the introduction of voltage regulator ICs such as the L78xx and L79xx - three-terminal series regulators which provide a very stable output and include current limiter and

thermal protection functions. Figures 16, 17 and 18 show how these circuits are used. Refer to the data sheets for more information.

Figure 11 : Ripple Reduction Produced by a Single Section Inductance-capacitance Filter.

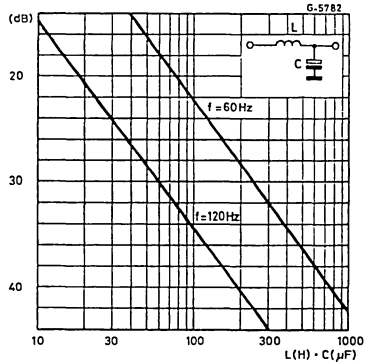


Figure 12 : Basic Zener Regulator Circuit.

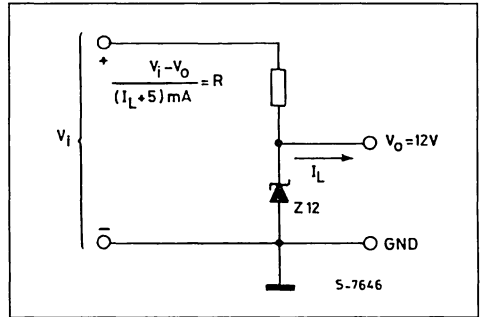
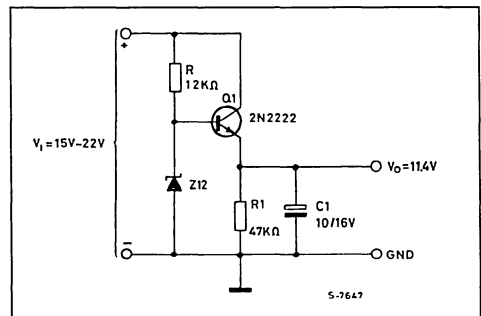


Figure 13 : The Series Pass Zener-based Regulator Circuit can Supply Load Currents up to about 100mA.



APPLICATION NOTE

Figure 14 : The Op-amp-based Regulator can Supply 100mA with Excellent Regulation.

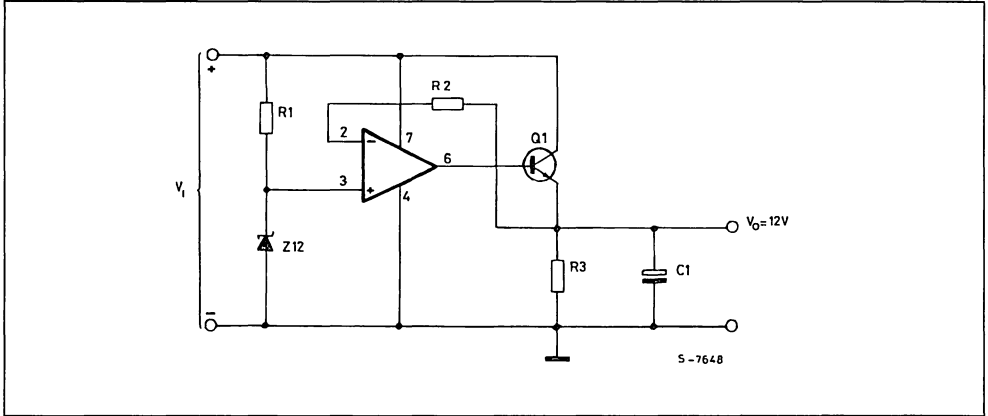


Figure 15 : Zener Regulator Circuit Modified for Low-noise Output.

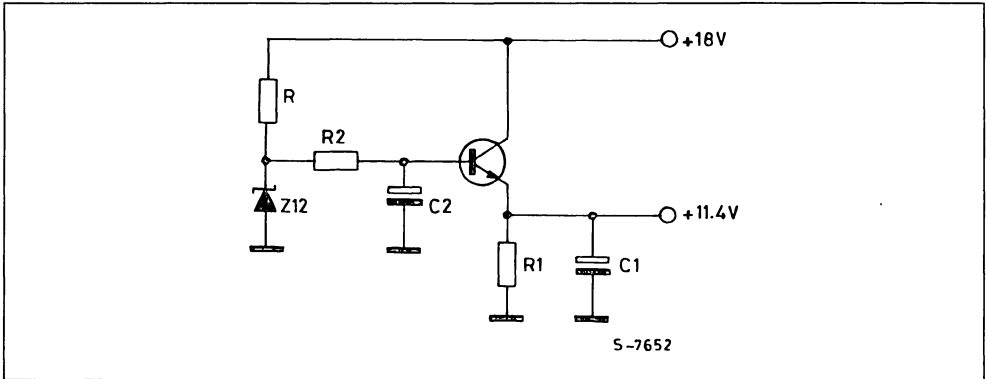


Figure 16 : A Three Terminal 1A Positive Regulator Circuit is very Simple and Performs very Well.

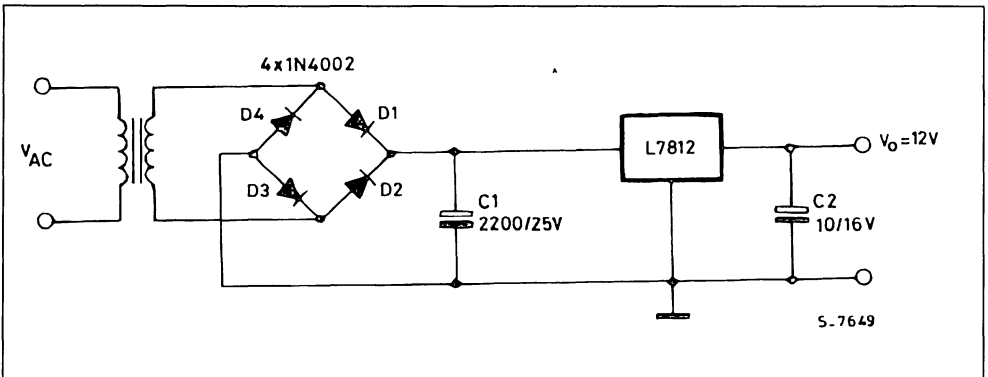
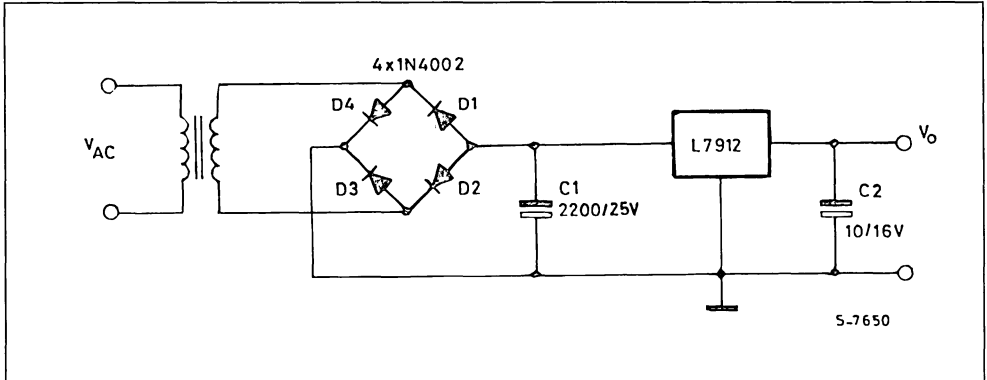
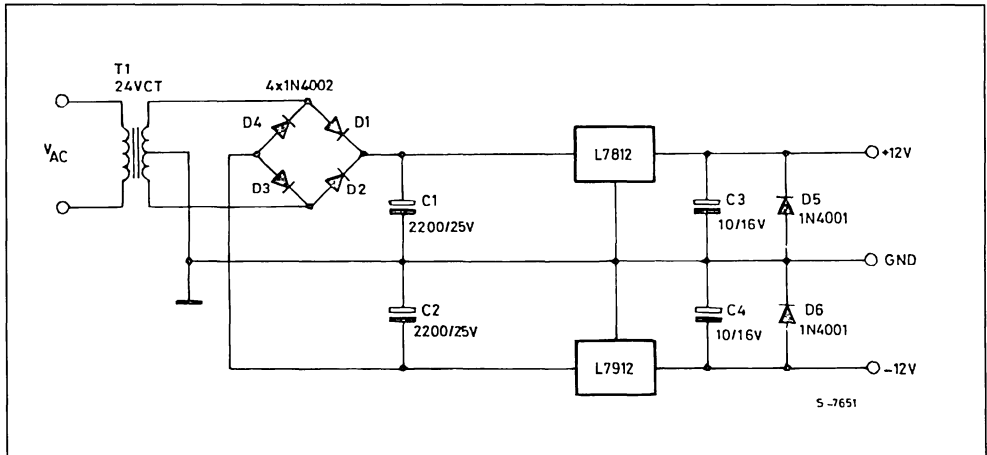
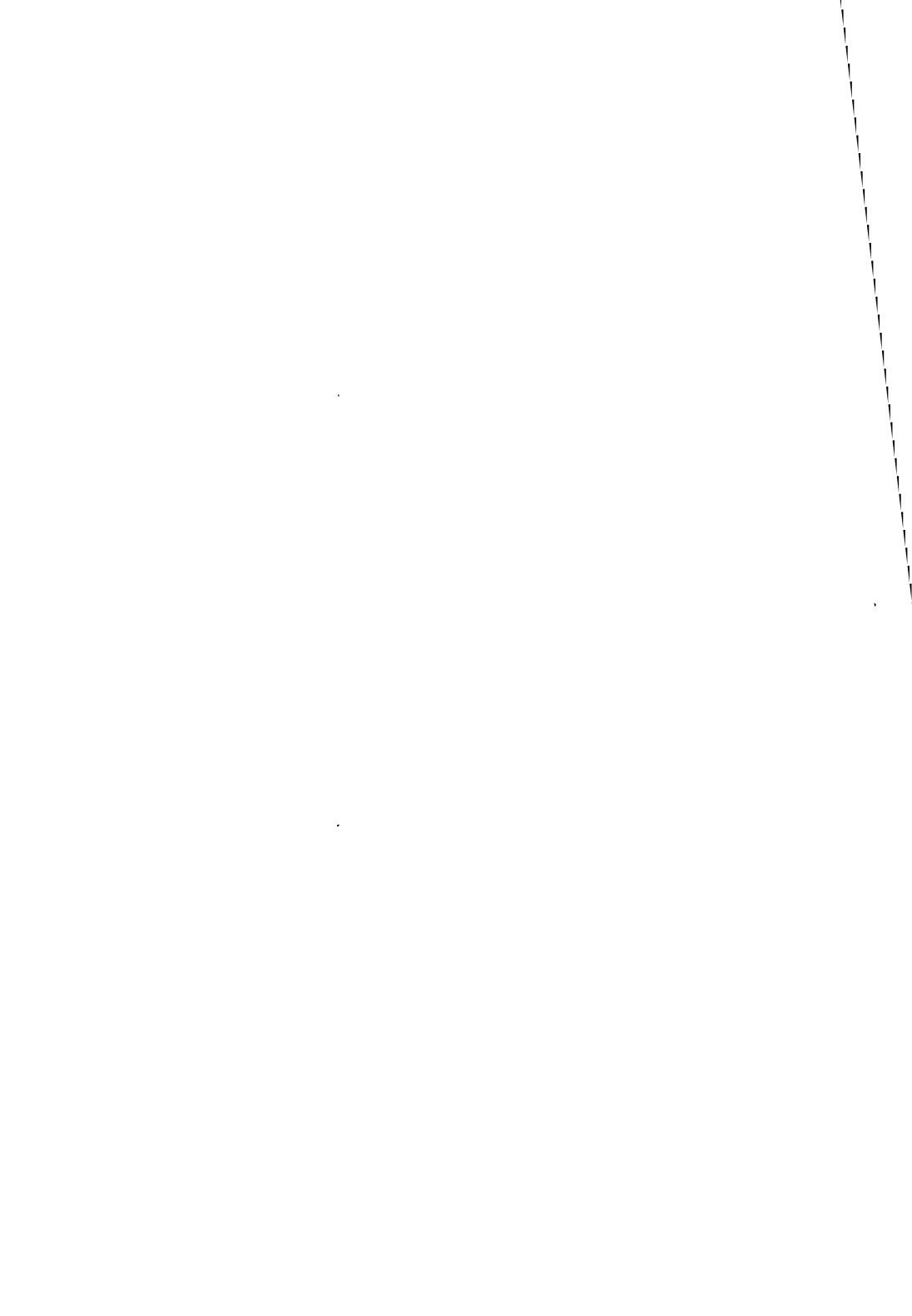


Figure 17 : A Three Terminal 1A Negative Voltage Regulator.

Figure 18 : Complete $\pm 12V - 1A$ Split Supply Regulator Circuit.



TOPOLOGIES FOR SWITCHED MODE POWER SUPPLIES

by L. Wuidart

I INTRODUCTION

This paper presents an overview of the most important DC-DC converter topologies. The main object is to guide the designer in selecting the topology with its associated power semiconductor devices.

The DC-DC converter topologies can be divided in two major parts, depending on whether or not they have galvanic isolation between the input supply and the output circuitry.

II NON - ISOLATED SWITCHING REGULATORS

According to the position of the switch and

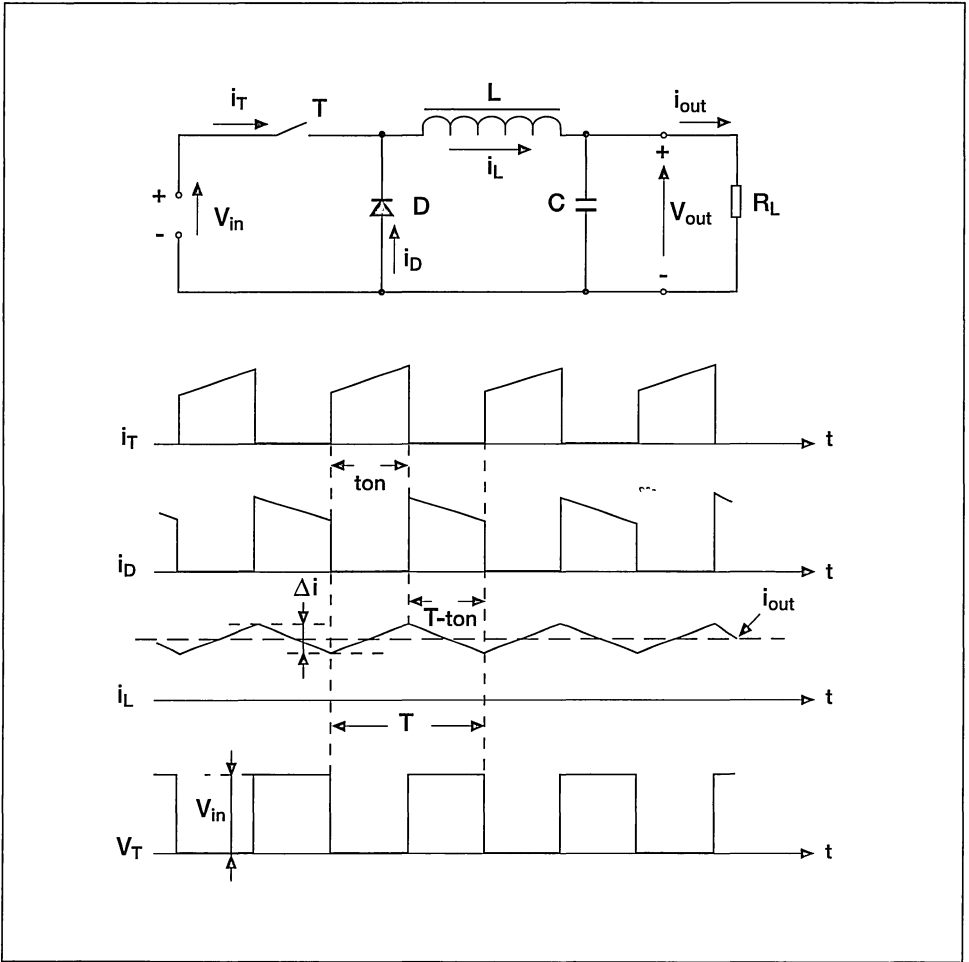
the rectifier, different types of voltage converters can be made:

- Step down "Buck" regulator
- Step up "Boost" regulator
- Step up/Step down "Buck-Boost" regulator

II - 1 The "Buck" converter: Step down voltage regulator

The circuit diagram, often referred to as a "chopper" circuit, and its principal waveforms are represented in figure 1:

Figure 1: The step down "Buck" regulator



The power device is switched at a frequency $f = 1/T$ with a conduction duty cycle, $\delta = t_{on}/T$. The output voltage can also be expressed as: $V_{out} = V_{in} \cdot \delta$

* Rectifier:

$$V_{RRM} \geq V_{in \max}$$

$$I_{F(AV)} \geq I_{out} (1-\delta)$$

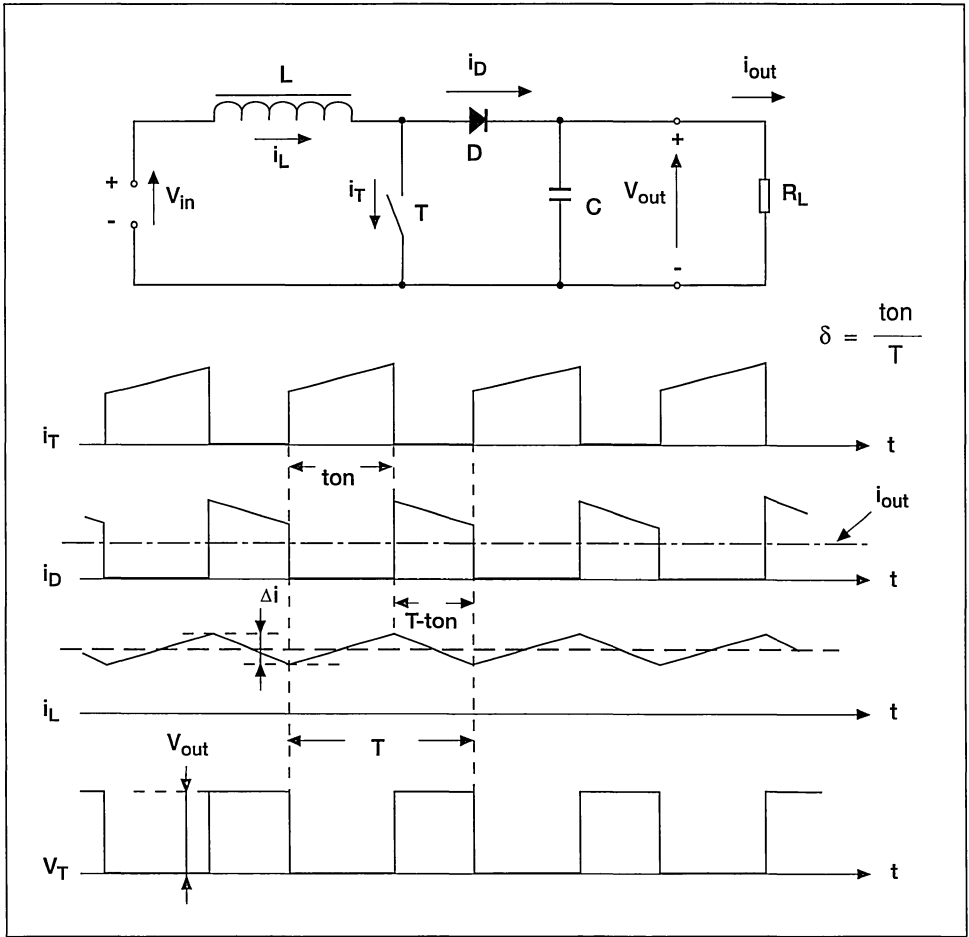
Device selection:

* Power switch: V_{cev} or $V_{DSS} > V_{in \max}$

$$I_{cmax} \text{ or } I_{D \max} > I_{out} + \frac{\Delta I}{2}$$

II.2 The "Boost" converter: Step up voltage regulator

Figure 2 : The step up "Boost" regulator



In normal operation, the energy is fed from the inductor to the load, and then stored in the output capacitor. For this reason, the output capacitor is stressed a lot more than in the Buck converter.

$$V_{out} = \frac{V_{in}}{1-\delta}$$

Device selection:

* *Power switch:* V_{cev} or $V_{DSS} > V_{out}$

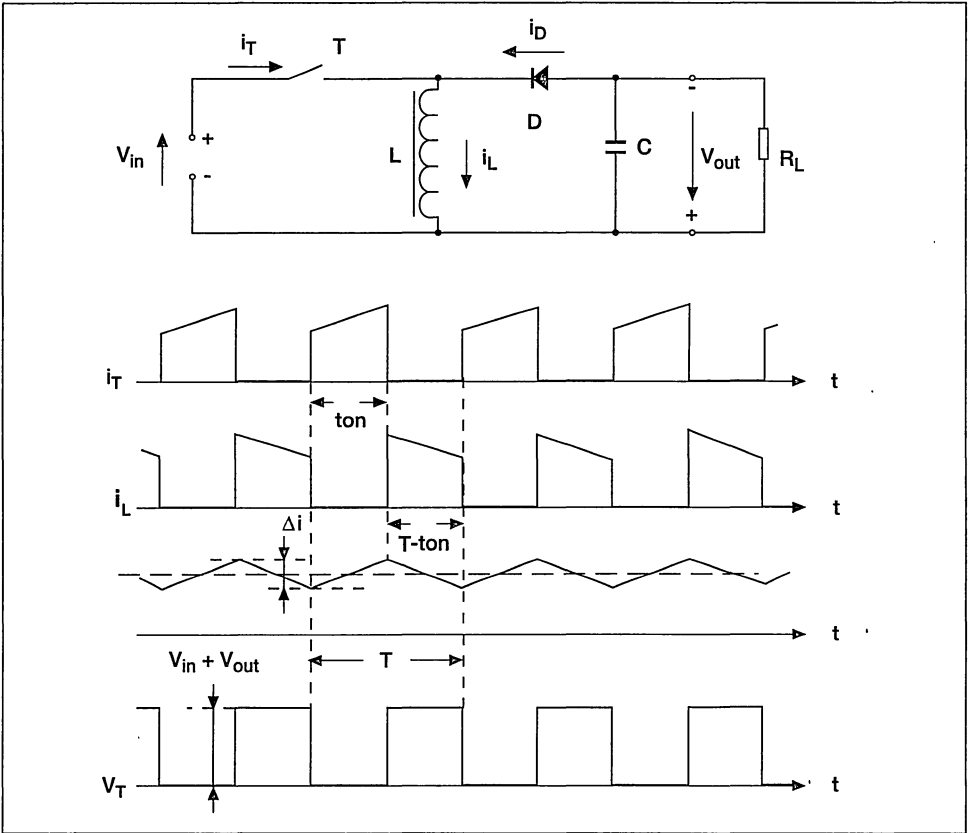
$$I_{cmax}$$
 or $I_{Dmax} > \frac{I_{out}}{1-\delta} + \frac{\Delta I}{2}$

* *Rectifier:* $V_{RRM} > V_{out}$

$$I_{F(av)} > I_{out}$$

II - 3 “Buck-Boost converter: Step up/Step down voltage regulator

Figure 3 : The step up/step down “Buck-Boost” regulator



For a duty cycle under 0.5 the conversion works in step down mode, for a duty cycle over 0.5, the converter then operates in the step up mode.

* Rectifier:

$$V_{RRM} > V_{inmax} + V_{out}$$

$$I_{F(av)} > I_{out}$$

$$V_{out} = - \frac{V_{in} \cdot \delta}{1 - \delta}$$

Device selection:

* Power switch :

$$V_{cevmax} \text{ or } V_{DSS} > V_{inmax} + V_{out}$$

$$I_{cmax} \text{ or } I_{Dmax} > \frac{I_{out}}{1 - \delta} + \frac{\Delta I}{2}$$

II.4 Summary

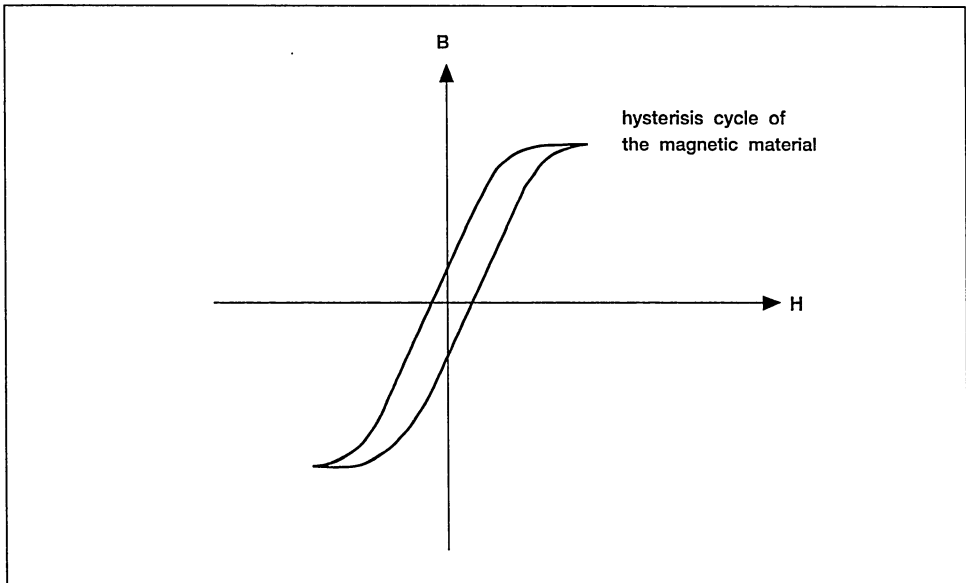
	STEP DOWN	STEP UP	STEP UP/DOWN
V_{out}	$V_{in} \cdot \delta$	$V_{in}/1-\delta$	$[-V_{in} \cdot \delta] / [1-\delta]$
RMS current in C_{out}	low	high	high
Supplied input current	discontinuous	continuous	discontinuous
Gate drive	floating	grounded	floating

III - ISOLATED CONVERTERS:

The isolated converters can be classified according to their magnetic cycle swing in the B-H plot (see figure 4). An isolated converter

is asymmetrical if the magnetic operating point of the transformer remains in the same quadrant. Any other converter is, of course, called symmetrical.

Figure 4 : B-H plot of symmetrical converters



III - 1 Asymmetrical converters

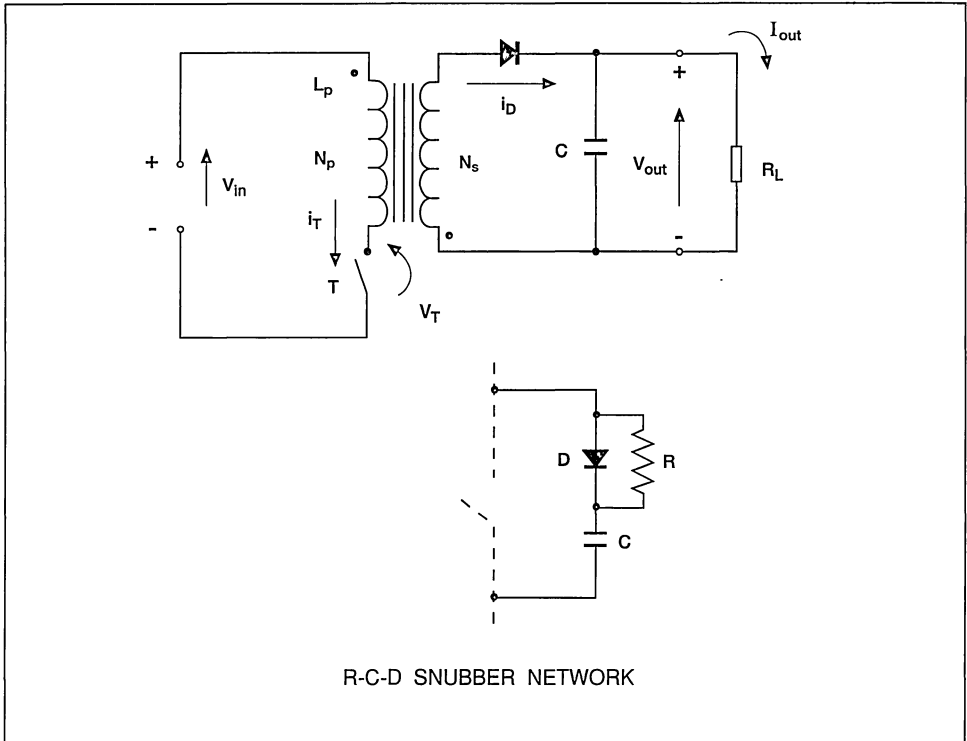
$$V_{out} = \frac{V_{in}}{n} \cdot \frac{\delta}{1-\delta}$$

III - 1.1 Off-line flyback regulators

The energy is stored in the primary L_p inductance of the transformer during the time the power switch is on, and transferred to the secondary output when the power switch is off. If $n = N_p / N_s$ is the turns ratio of the transformer we have:

Off-line flyback regulators are mainly used for an output power ranging from 30W up to 250W. Flyback topology is dedicated to multiple low cost output SMPS as there is no filter inductor on the output.

Figure 5 : Isolated single switch flyback



*Power switch:

$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax} + nV_{out} + \text{leakage inductance spike}$$

* Secondary Rectifier:

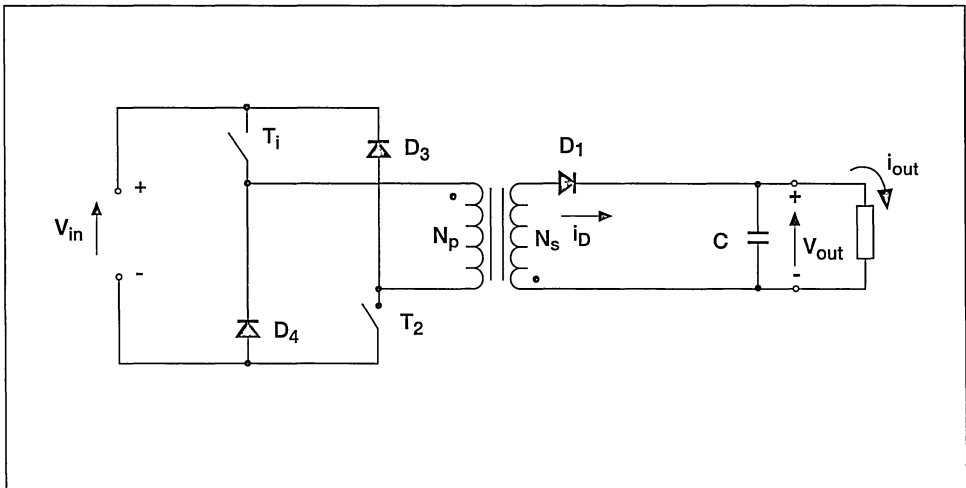
$$V_{RRM} \geq V_{out} + \frac{V_{inmax}}{n}$$

a. Single switch versus double switch flyback

In the single switch flyback, an overvoltage spike is applied across the power switch at each turn off. The peak value of this overvoltage depends upon the switching time, the circuit capacitance and the primary to secondary transformer leakage inductance. So, a single switch flyback nearly always requires a snubber circuit limiting this voltage spike (see figure 5).

In a double switch flyback, the leakage inductance of the power transformer is much less critical (see figure 6). The two demagnetization diodes (D_1 and D_2) provide a single non dissipative way to systematically clamp the voltage across the switches to the input DC voltage V_{in} . This energy recovery system allows us to work at higher switching frequencies and with a better efficiency than that of the single switch structure. However, the double switch structure requires driving a high side switch. This double switch flyback is also known as asymmetrical half bridge flyback.

Figure 6: Isolated double switch flyback



* Power switch:

$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax}$$

* Primary Rectifiers: D_3 and D_4

$$V_{RRM} \geq V_{inmax}$$

b. Discontinuous versus continuous mode flyback

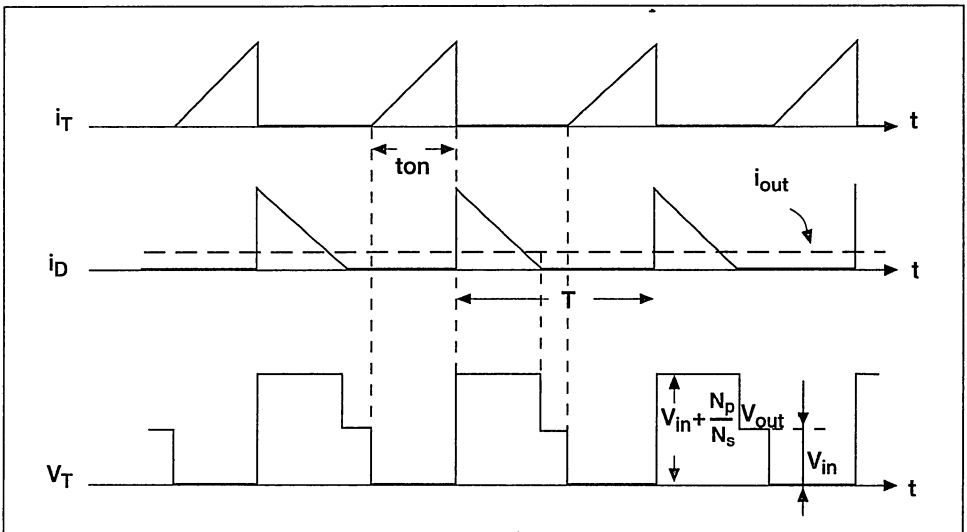
inductance of the transformer is completely demagnetized or not.

The flyback converter has two operating modes depending whether the primary

Discontinuous mode

ADVANTAGES	DISADVANTAGES
- Zero turn-on losses for the power switch	- High peak currents in rectifiers and power switches
- Good transient line/load response	- Large output ripple: $C_{out} (disc.) \approx 2 \cdot C_{out} (cont.)$
- Feedback loop (single pole) easy to stabilize	
- Recovery time rectifier not critical: current is zero well before reverse voltage is applied	

Figure 7: Discontinuous mode flyback waveforms



* Power switch: $I_{Cpeak} \geq \frac{2P_{out}}{\eta V_{inmin} \delta_{max}}$

* Rectifier: $I_{Fpeak} \geq \frac{2P_{out}}{V_{out} (1 - \delta_{max})}$

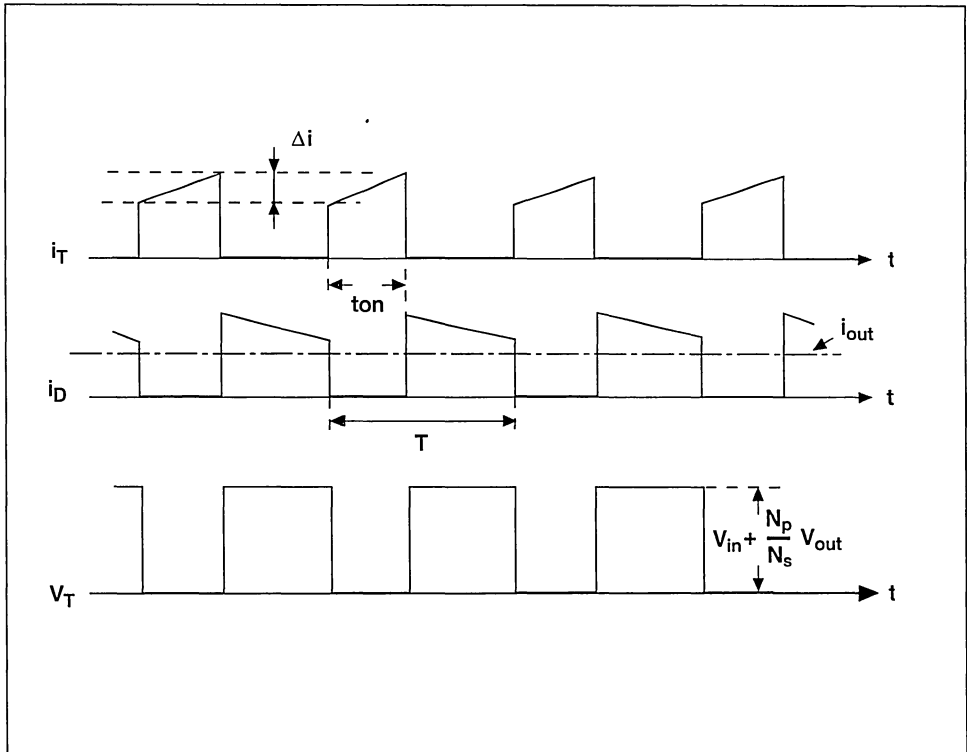
$I_{Drms} \geq \frac{2P_{out}}{\eta V_{inmin} \sqrt{(3\delta_{max})}}$

$I_{F(AV)} \geq \frac{P_{out}}{V_{out}}$

Continuous mode

ADVANTAGES	DISADVANTAGES
<ul style="list-style-type: none"> - Peak current of rectifier and switch is half the value of discontinuous mode - Low output ripple: $C_{out}(\text{cont.}) \approx 0.5 C_{out}(\text{disc.})$ 	<ul style="list-style-type: none"> - Recovery time rectifier losses -Feedback loop difficult to stabilize (2 poles and right half plane zero)

Figure 8: Continuous mode flyback waveforms



* *Power switch:*

$$I_{Cpeak} \geq \frac{2P_{outmax}}{\eta \delta_{max} V_{inmin} (1+A)}$$

$$I_{Drms} \geq \frac{2P_{out}}{\eta V_{inmin}} \sqrt{\frac{(1 + A + A^2)}{3\delta_{max}}}$$

* *Rectifier:*

$$I_{Fpeak} \geq \frac{2P_{out}}{V_{out} (1 - \delta_{max})(1+A)}$$

$$I_F(AV) \geq \frac{P_{out}}{V_{out}}$$

$$\text{with } A \geq = \frac{I_{peak} - \Delta I}{I_{peak}}$$

in single switches, and up to 1kW in double switch structures.

Single switch vs. double switch forward

In the single switch forward, the magnetizing energy stored in the primary inductance is restored to the input source by a demagnetization winding N_d . Most commonly, the primary and the demagnetization windings have the same number of turns.

So, at turn-off, the power switch has to withstand twice the input voltage during the demagnetization time, and then, once the input voltage (see figure 9).

The demagnetization and primary windings have to be tightly coupled to reduce the voltage spike - more than the theoretical $2V_{in}$ - occurring at turn-off across the power switch.

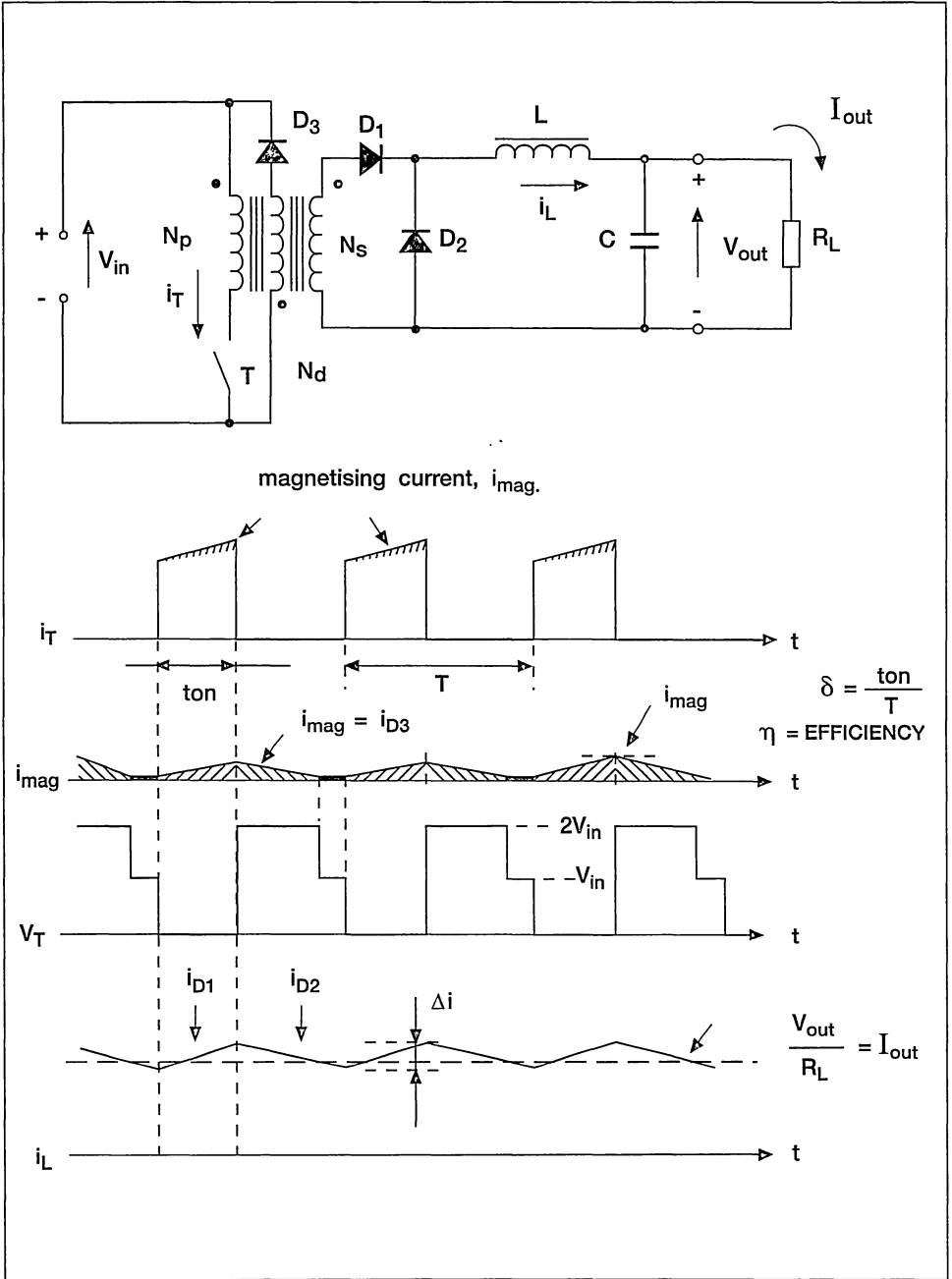
III - 1.2 Off line forward regulators

The forward converter transfers directly the energy from the input source to the load during the on-time of the power switch. During off-time of the power switch, the energy is freewheeling through the output inductor and the rectifier D_2 , like in a chopper (see figure 1).

$$V_{out} = \delta \cdot \frac{V_{in}}{n}$$

A forward regulator can be realized with a single switch structure or with a double switch structure, according to the way the energy stored in the transformer primary inductance is demagnetized. Forward converters are commonly used for output power up to 250W

Figure 9: Isolated single switch forward



* Power switch:

$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax} \left[1 + \frac{N_p}{N_d} \right] + \text{leakage inductance spike}$$

$$I_{cpeak} \geq \frac{1.2 \cdot P_{out}}{\eta V_{inmin} \cdot \delta_{max}}$$

$$I_{Drms} \geq \frac{1.2 \cdot P_{out}}{\eta V_{inmin} \cdot \sqrt{\delta_{max}}}$$

*Rectifiers:

FORWARD D1:
$$\left[\begin{array}{l} V_{RRM} \geq V_{inmax} \cdot \frac{N_s}{N_d} + \text{leakage inductance spike} \\ I_{F(av)} \geq I_{out} \cdot \delta_{max} \end{array} \right.$$

FREEWHEELING D2:
$$\left[\begin{array}{l} V_{RRM} \geq \frac{V_{inmax} \cdot (V_{out} + V_F)}{V_{inmin} \cdot \delta_{max}} \\ I_{F(av)} \geq I_{out} \end{array} \right.$$

DEMAGNETIZATION D3:
$$\left[\begin{array}{l} V_{RRM} \geq \left[1 + \frac{N_d}{N_p} \right] V_{inmax} \\ I_{F(av)} \geq \frac{I_{magnpeak}}{2} \cdot \delta_{max} \end{array} \right.$$

In the "double switch forward", also called asymmetrical half bridge forward, the magnetizing energy stored in the primary inductance is automatically returned to the bulk capacitor by the two demagnetization diodes D_1 and D_2 .

The two power switches and demagnetisation diodes have to withstand only once the input voltage V_{in} . As for the double switch flyback, the asymmetrical half bridge needs a floating gate drive for the high side switch.

$$I_{Drms} \geq \frac{1.2 \cdot P_{out}}{\eta V_{inmin} \cdot \sqrt{\delta_{max}}}$$

* Rectifiers:

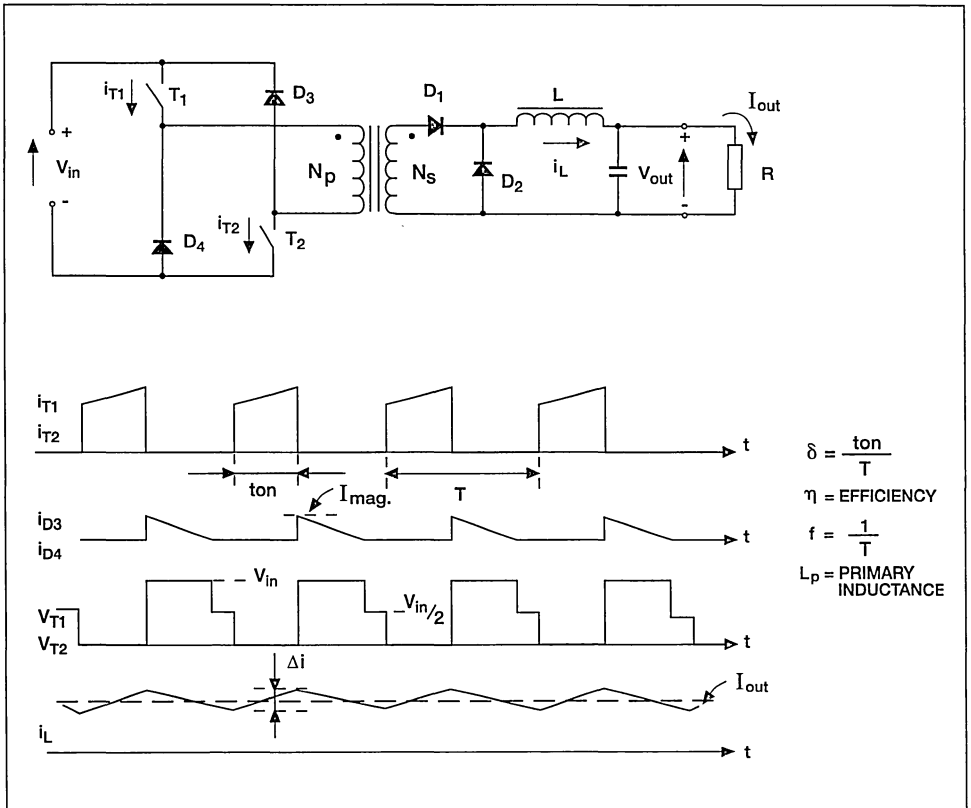
$$\text{FORWARD D1: } \begin{cases} V_{RRM} \geq \frac{V_{inmax} (V_{out} + V_F)}{V_{inmin} \cdot \delta_{max}} \\ I_{F(av)} \geq I_{out} \cdot \delta_{max} \end{cases}$$

$$\text{FREEWHEELING D2: } \begin{cases} V_{RRM} \geq V_{inmax} (V_{out} + V_F) \\ I_{F(av)} \geq I_{out} \end{cases}$$

* Power switch:

$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax}$$

Figure 10: Half bridge asymmetrical forward converter



III - 2 Symmetrical converters

This type of converter always uses an even number of switches. It also better exploits the transformer's magnetic circuit than in asymmetrical converters. So, smaller size and weight can be achieved.

The three most common structures used are:

- PUSH/PULL
- HALF BRIDGE with capacitors
- FULL BRIDGE

III - 2.1 Push/Pull converter

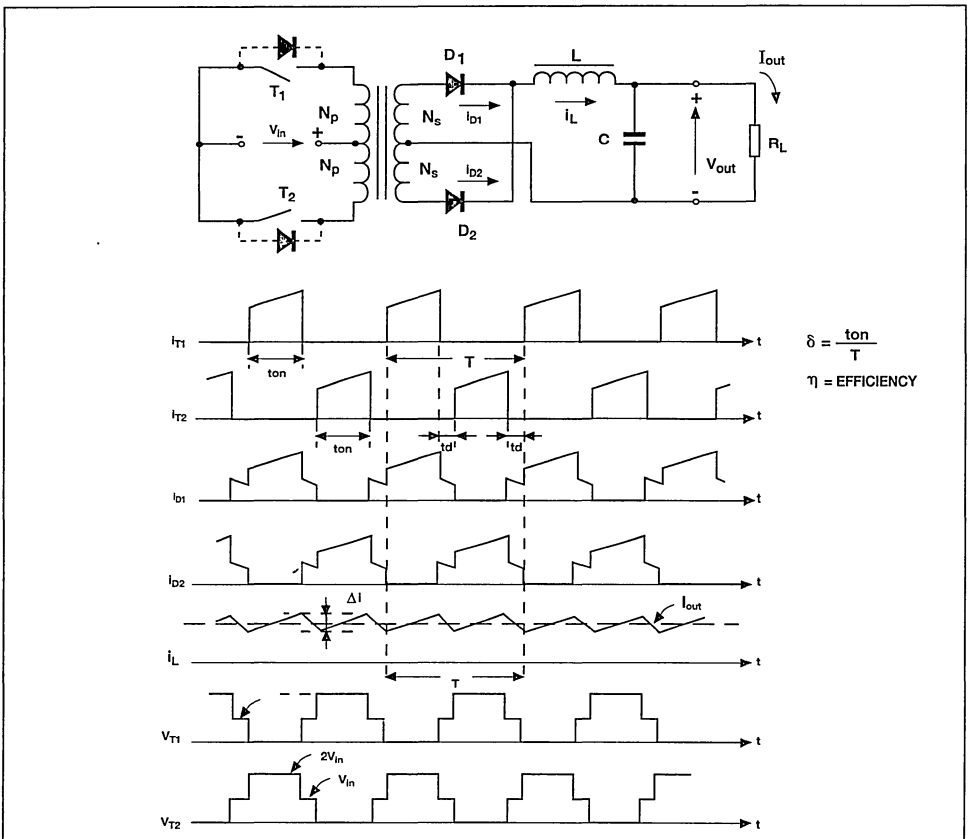
T_1 and T_2 switches (see figure 11) are alternately turned-on during a time t_{on} . The secondary circuit operates at twice the switching frequency.

A deadtime t_d between the end of conduction of one switch and the turn-on time of the other one is required in order to avoid simultaneous conduction of the two switches.

$$V_{out} = 2 \frac{\delta V_{in}}{n}$$

Moreover, the snubber network in symmetrical converters must be carefully designed, since they inter-react with one another.

Figure 11: Push-Pull converter



* *Power switch*

$$I_{Dpeak} \text{ or } I_{Cpeak} \geq \frac{P_{out}}{\eta V_{inmin}}$$

$$V_{CEV} \text{ or } V_{DSS} \geq 2V_{inmax} + \text{leakage inductance spike}$$

* *Rectifier*

$$V_{RRM} \geq \frac{(V_{out} + V_F) V_{inmax}}{\delta_{max} \cdot V_{inmin}} + \text{Voltage spike}$$

$$I_{F(av)} \geq \frac{I_{outmax}}{2}$$

The switches are easy to drive since they are both referenced to ground, however they must withstand twice the input supply voltage.

The capacitors in series across the supply fix a mid-point so that switches withstand only once the input voltage V_{in} .

The inherent flux symmetry problems can be corrected with a current mode PWM control circuit.

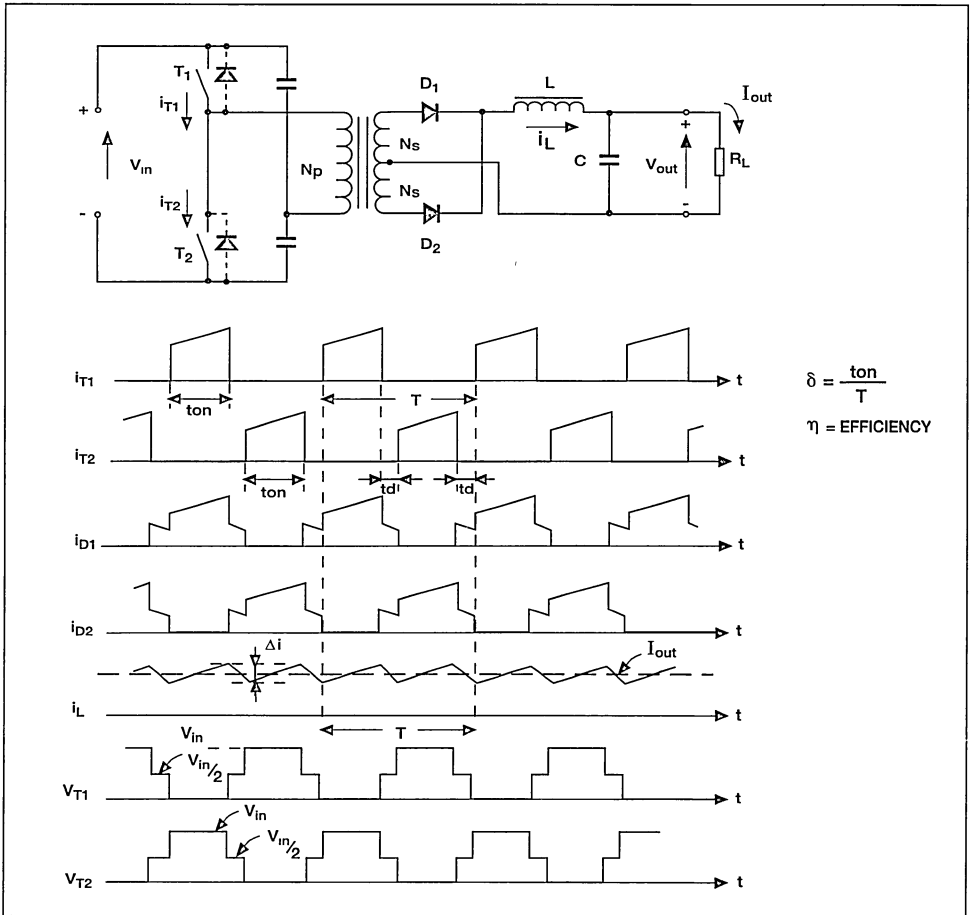
However, this topology requires driving a high side switch. When using bipolar switches, transistor's storage time should have tight tolerances to avoid imbalance in operating flux level.

III - 2.2 Half bridge converter

This topology can be used for an output power capability up to 500W. As for the push-pull converter, T_1 and T_2 switches are alternately turned on during a time t_{on} .

$$V_{out} = \frac{V_{in} \cdot \delta}{n}$$

Figure 12: Half bridge converter



* Power switch:

$$I_{Cpeak} \text{ or } I_{Dpeak} \geq \frac{2P_{out}}{\eta V_{inmin}}$$

$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax}$$

* Rectifier:

$$V_{RRM} \geq \frac{(V_{out} + V_F) \cdot V_{inmax}}{\delta_{max} \cdot V_{inmin}} + \text{leakage inductance spike}$$

$$I_{F(av)} \geq \frac{I_{outmax}}{2}$$

Deadtimes (t_d on figure 12) between two consecutive switch conduction are absolutely mandatory to avoid bridge-leg short circuit.

Sometimes, power transformers are paralleled to provide higher output power.

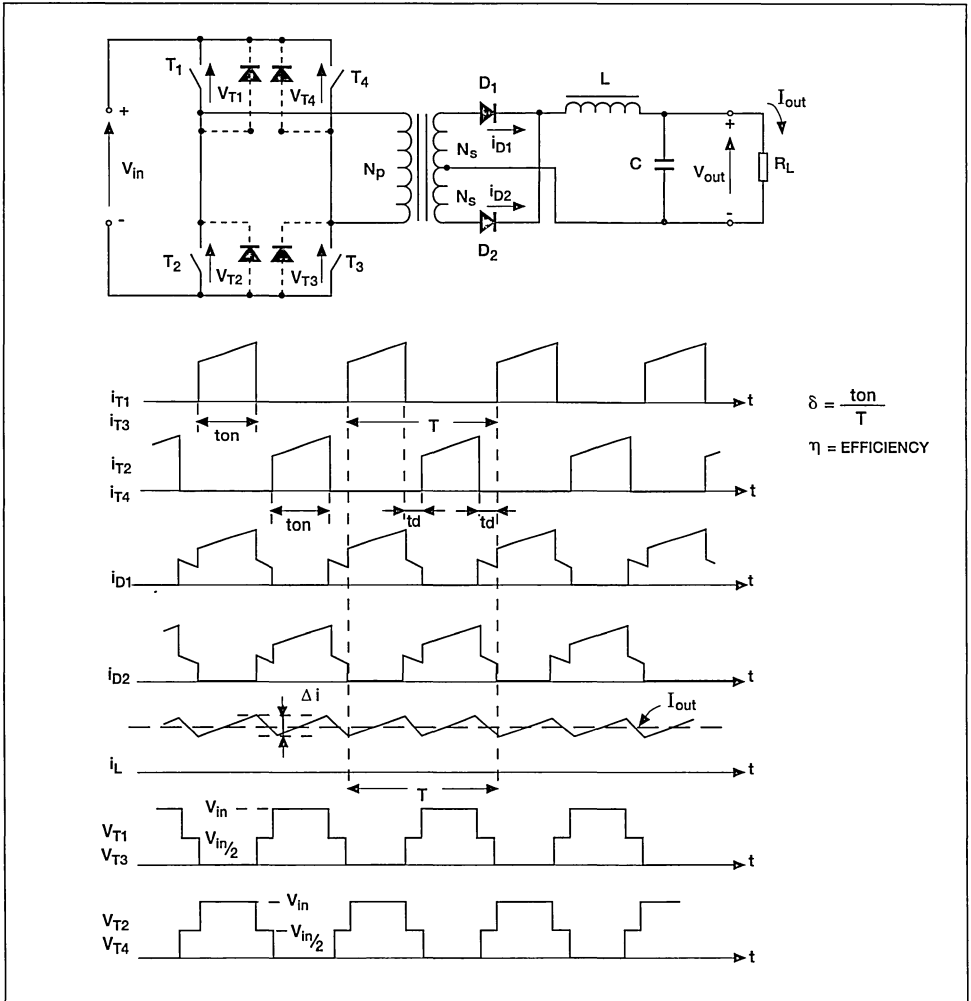
III - 2.3 Full bridge converter

$$V_{out} = \frac{2V_{in}\delta}{n}$$

Because of the number of components, the full bridge is for high power applications, ranging from 500 up to 2000W.

Switch pairs T_1 and T_3 , T_2 and T_4 are alternately driven.

Figure 13: Full bridge converter



* *Power switch:*

$$I_{Cpeak} \text{ or } I_{Dpeak} \geq \frac{P_{out}}{\eta V_{inmin}}$$
$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax}$$

* *Rectifier:*

$$V_{RRM} \geq \frac{(V_{out} + V_F) V_{inmax}}{\delta_{max} \cdot V_{inmin}} + \text{leakage inductance spike}$$
$$I_F(av) \geq \frac{I_{outmax}}{2}$$

The full bridge provides twice the output power of the half bridge circuit with the same switch ratings.

Nevertheless, this topology requires 4 switches and clamping diodes.

IV - CONCLUSION

Many significant technological changes in power supply design have resulted in lower cost per Watt with improved performance.

Today, designers keep going ahead with the state-of-the-art in switching regulator technology in order to reduce size and weight of power packages.

Output voltage and load current always depend upon the application. The power supply designs are often tailored to specific applications. No simple procedure exists to select the right topology.

This paper provides an overview of the most commonly used topologies and lists the most important features for each topology.

UNDERSTANDING POWER FACTOR

by L. Wuidart

1. INTRODUCTION

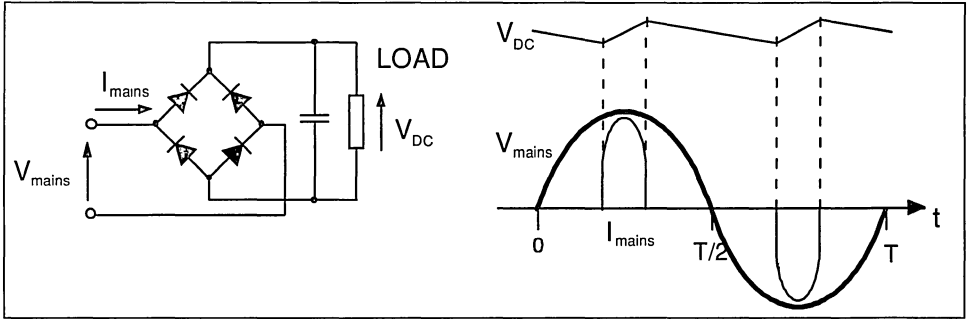
The majority of electronics designers do not worry about Power Factor (PF); PF is something that you learnt one day at school in your "electrotechnics course" as being the \cos of ϕ , the phase angle between the voltage and current waveforms. However, this conventional definition is only valid when considering ideal sinusoidal signals for both current and voltage waveforms, and in reality most off-line power supplies draw a non-sinusoidal current.

Many off-line systems will typically have a front end section consisting of a rectifier bridge and an input filter capacitor, which act as a peak detector - see figure 1. A current flows to charge the capacitor only when the instantaneous AC voltage exceeds

the voltage of the capacitor. A single phase off-line supply draws a current pulse during a small fraction of the half-cycle duration. Between those current peaks, the load draws the energy stored in the input capacitor. The phase lag ϕ and also the harmonic content of the pulsed current waveform produce additional RMS currents, affecting the real power available from the mains. So Power Factor is much more than $\cos \phi$!

The P.F. value measures how much the mains efficiency is affected by both the phase lag ϕ and the harmonic content of the input current. In this context, the European Standard EN 60555 only defines the limit of current harmonics in mains supplied equipment.

Figure 1: Full-Wave Rectifier



2. THEORETICAL MEANING

The Power Factor is defined by:

$$P.F. = \frac{P}{S} = \frac{\text{REAL POWER}}{\text{APPARENT POWER}}$$

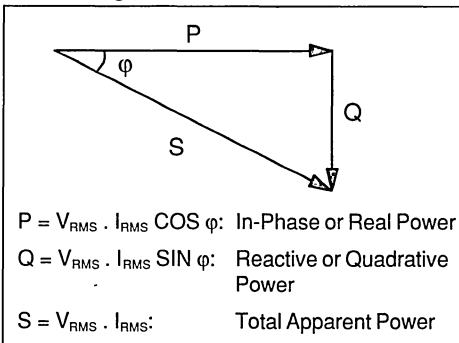
2.1 Ideal sinusoidal signals

For ideal sinusoidal voltage and current waveforms, if there is a phase difference φ between the voltage and current waveforms, the total apparent power can be modelled as being composed of two components: one in phase with the input voltage, and the other 90° out of phase (in quadrature) with it - see figure 2.

Then by definition,

$$P.F. = \frac{P}{S} = \cos \varphi$$

Figure 2: Power vectors of ideal sinusoidal signals



2.2 Non-ideal sinusoidal current

Assuming that the mains voltage is an ideal sinusoidal voltage waveform, its RMS value is:

$$V_{RMS} = \frac{V_{peak}}{\sqrt{2}}$$

If the current has been distorted in some way (for example as in figure 1) into a periodic non-sinusoidal waveform, applying a Fourier transform gives:

$$I_{RMS(total)} = \sqrt{I_0^2 + I_{1RMS}^2 + I_{2RMS}^2 + \dots + I_{nRMS}^2}$$

where I_0 is the DC component of the current, I_{1RMS} the fundamental of the RMS current (that is the component at the frequency of the voltage input) and $I_{2RMS} \dots I_{nRMS}$ are the harmonics created by the distortion.

For a pure AC signal, there is no DC component and so $I_0 = 0$.

The fundamental of the RMS current can be modelled as in section 2.1 above as an in-phase component $I_{1RMS P}$ and a quadrature component $I_{1RMS Q}$, and so the RMS current can be expressed as:

$$I_{RMS(total)} = \sqrt{I_0^2 + I_{1RMS P}^2 + I_{1RMS Q}^2 + \sum_{n=2}^{\infty} I_{nRMS}^2}$$

Then, the Real Power is given by the RMS voltage multiplied by the in-phase current:

$$P = V_{RMS} \cdot I_{1RMS P}$$

As φ_1 is the displacement angle between the input voltage and the in-phase component of the fundamental current:

$$I_{1RMS\ P} = I_{1RMS} \cos \varphi_1$$

so

$$P = V_{RMS} \cdot I_{RMS} \cos \varphi_1$$

As the total apparent power is given by:

$$S = V_{RMS} \cdot I_{RMS\ total}$$

the Power Factor can be calculated as :

$$P.F. = \frac{P}{S} = \frac{I_{1RMS} \cdot \cos \varphi_1}{I_{RMS\ (total)}}$$

If the phase angle between I_{1RMS} and $I_{RMS(total)}$ is defined as θ :

$$\cos \theta = \frac{I_{1RMS}}{I_{RMS\ (total)}}$$

θ is linked to the harmonic content of the current; as the harmonic content of $I_{RMS(total)}$ approaches zero, θ approaches 0 and $\cos \theta$ approaches 1.

2.3 Summary

Finally then, the Power Factor can be expressed as:

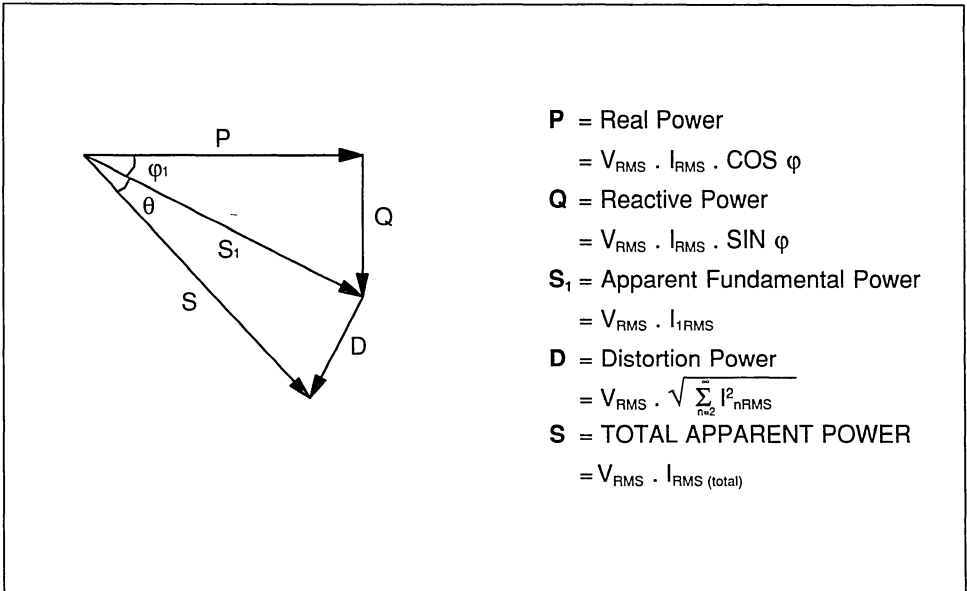
$$P.F. = \cos \theta \cdot \cos \varphi_1$$

and the representation of the power vectors becomes that shown in figure 3.

φ_1 is the "conventional" displacement angle (phase lag) between the voltage and the fundamental component of the current, while θ is the distortion angle caused by the harmonic content of the current.

Both the reactive power, Q, and the distortion power, D, produce extra RMS currents, giving additional losses and reducing the efficiency of the mains supply network.

Figure 3: Power vectors with non-sinusoidal signals



Improving the Power Factor means reducing both elements:

$$\varphi_1 \rightarrow 0 \text{ means } \text{COS } \varphi_1 \rightarrow 1:$$

reduction of the phase lag between I and V,

$$\theta \rightarrow 0 \text{ means } \text{COS } \theta \rightarrow 1:$$

reduction of harmonic content of I.

3. PRACTICAL IMPLICATIONS OF POWER FACTOR

3.1 Benefits of reduced Power Factor

Both the user and the electricity supply company can benefit from a reduction in Power Factor. Adding a PFC also reduces the component costs in a downstream converter.

3.1.1 Benefits to the user

At the minimum line voltage ($85V_{AC}$), a standard $115V_{AC}$ wall socket should be able to deliver the nominal 15A to a common load. However, an SMPS without a Power Factor Corrector (PFC), which will typically have a Power Factor of 0.6, reduces the available current to around 9A.

As an example, a single wall socket will supply four 280W computers equipped with PFCs, but only two without.

3.1.2 Benefits to the distribution company

Both the reactive power Q and the distortion power D give rise to extra RMS currents, significantly reducing the efficiency of the mains supply network. This means that the copper distribution wires must be thicker than would otherwise be necessary.

Delivering power at frequencies other than the line frequency (ie the distortion power D) also causes difficulties. The distortion disturbs the zero voltage crossing detection systems, and generates overcurrent in the neutral line and resonant overvoltages.

In Europe, the standard EN 60555 and the international project IEC 555-2 limit the

harmonic content of the current of mains supplied equipment.

3.1.3 Reduction of component costs in the downstream converter

For the same output power capability, a conventional converter using an input mains voltage doubler has primary RMS current 1.8 times higher than one employing a PFC regulator. Consequently, if a PFC is used in a system using Power MOSFET switches, the on-resistance ($R_{DS(ON)}$) of the switches can be up to three times higher than in a system without PFC, allowing significantly cheaper parts to be used.

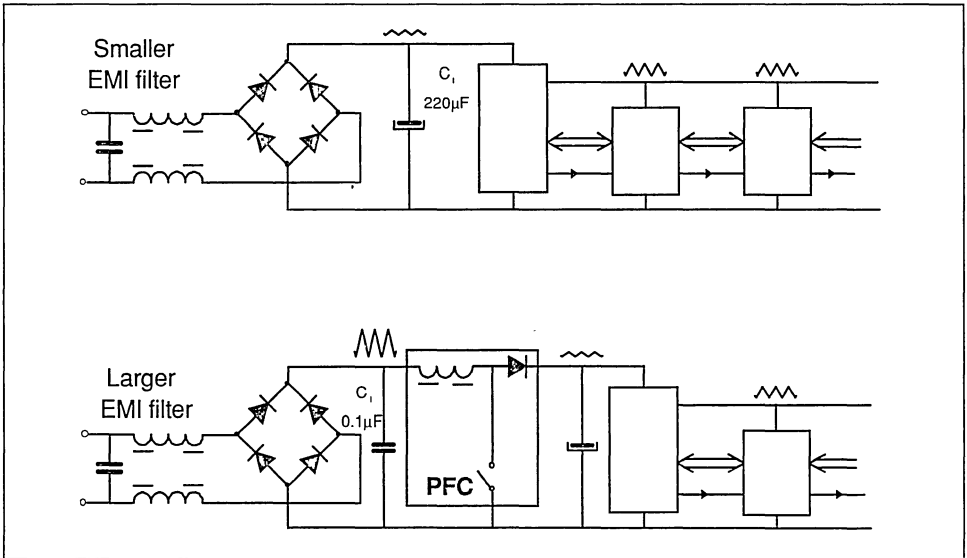
The size of the converter transformer can be reduced not only because the thickness of the windings is smaller, but also because of the regulation of the DC bulk voltage delivered by the PFC pre-regulator.

The PFC provides an automatic mains selection on a wide range of voltages from $85V_{AC}$ up to $265V_{AC}$. Compared to the conventional doubler front-end section the same hold-up time can be achieved with a bulk storage capacitor 6 times smaller. For example, to achieve a 10ms hold-up time, a 100W converter in doubler operation requires a series combination of two $440\mu\text{F}$ capacitors without a PFC, but only a single $130\mu\text{F}$ with.

3.2 RFI filter

However, the size and cost optimisation of the PFC has to take the RFI filter into consideration. A PFC circuit generates more high frequency interference to the mains than a conventional rectifier front-end - see figure 4. Thus the use of a PFC means that additional filtering is required. For this reason, modulation techniques and mode of operation for the PFC have to be carefully adapted to the requirements of the application.

Figure 4: SMPS with (a) conventional rectifier front-end, and
(b) PFC front-end



4. CONCLUSIONS

For new designs, SMPS designers will have to take into account the IEC 555-2 standard. In practice, this will require the use of a PFC on the front end of much mains supplied equipment. The additional cost of the PFC is compensated by the significant reduction

in the cost of components for the downstream converter. The PFC also provides additional functions such as automatic mains voltage selection and constant output voltage.

CIRCUITS FOR POWER FACTOR CORRECTION WITH REGARDS TO MAINS FILTERING

by J. M. Bourgeois

1. INTRODUCTION

The new European Norms EN 60555 and the international standard IEC555 will impose a limit on the harmonic content of the input current of mains supplied equipment. In practice this will require the addition of a Power Factor Corrector (PFC) at the input of many types of mains operated electronic equipment, for example electronic lamp ballasts, TV power supplies and motor drives. A correctly designed PFC draws a sinusoidal input current from the mains supply, in phase with the mains voltage, and meets the EN60555 norm. It may also provide additional functions, such as automatic mains voltage selection and a regulation of the voltage supplied to the attached equipment.

Size and cost optimization of PFCs must include the RFI filter on the input, which prevents interference being fed back to the mains. The addition of the PFC represents another switching stage in the system, meaning that larger amount of high frequency noise is applied to the mains than with a conventional rectifier/capacitor front end, and so additional RFI filtering is required. The amount of filtering needed can be minimized by choosing suitable modulation techniques and mode of operation of the PFC.

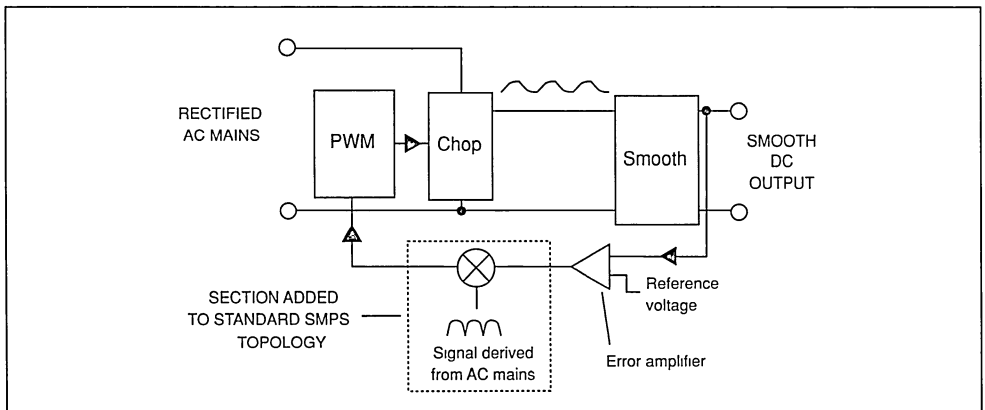
1.1 Basic principles of operation

A power factor corrector is basically a AC to DC converter, and is usually based on an SMPS structure. The basic functional blocks of a Power Factor Corrector are shown in figure 1.

A standard SMPS uses Pulse Width Modulation (PWM) to adjust the amount of power it supplies to the attached equipment. The Pulse Width Modulator controls the power switch, which chops the dc input voltage into a train of pulses. This train of pulses is then smoothed, producing the dc output voltage. This output voltage is then compared with a voltage reference representing the voltage desired by the equipment being supplied, and the resulting voltage difference (the error voltage) is fed back to the input of the PWM, which varies the width of the pulses it supplies accordingly - if the output voltage is too high, the pulse width is reduced, and thus less power is supplied, and vice versa.

A PFC also uses this method, but adds a further element to ensure that the current it draws from the mains is sinusoidal, and remains in phase with the mains voltage. The error voltage is modulated with a signal derived from the rectified AC mains, before

Figure 1. Block diagram of a Power Factor Corrector (PFC)



being fed to the PWM input. This means that the width of the power pulse supplied to the output device depends both on the basic error voltage and also on the instantaneous value of the mains voltage. The PFC thus draws more power from the mains when the level of the mains voltage is high, and less when it is low, which results in a reduction of the harmonics in the drawn current.

2. ACTIVE POWER FACTOR CORRECTOR TOPOLOGIES

Among the topologies shown in figure 2, the boost configuration operating in a continuous current mode (ie the value of the inductor at the input is calculated such that it conducts continuously throughout the switching cycle) applies the smallest amount of high frequency current to the input capacitor C_i . It is the only topology which allows the noise across the input capacitor to be reduced, which is the major factor defining the size and cost of the filter. Additionally, the boost inductor stores only a part of the transferred energy (because the mains still supplies energy during the inductor demagnetization) and so the inductor required is smaller in comparison with the other topologies.

The boost topology thus leads to the cheapest PFC solution, but does not provide either in-rush current or short circuit protection. The buck/boost topology can also be used; its advantages are that it can provide output isolation and adjustable output voltage.

This paper will take the cost as the most important consideration, and so will concentrate on the boost circuit topology.

3. BOOST CIRCUIT PARAMETER OPTIMIZATION

Figure 3 shows the general topology of a boost PFC. Its optimization requires careful adjustment of the following parameters:

- the value of the input capacitor C_i ,
- the current ripple in boost inductor L_b ,
- the parasitic capacitances of the boost inductor and the power semiconductors, including those associated with the heatsink
- the operating frequency and frequency modulation techniques.

3.1 Value of input capacitor C_i

The noise across the input capacitor, which determines the cost of the filter, is proportional to the current ripple and inversely proportional to the capacitor value.

A value of $3.3\mu\text{F}/\text{kW}$ is a good compromise between current distortion and noise generation.

3.2 Current ripple in the boost inductor

The current ripple (Δi) is a function of the input voltage (V_i), output voltage (V_{out}), inductor value (L_b) and switching frequency (f_s), and can

Figure 2. Active PFC topologies

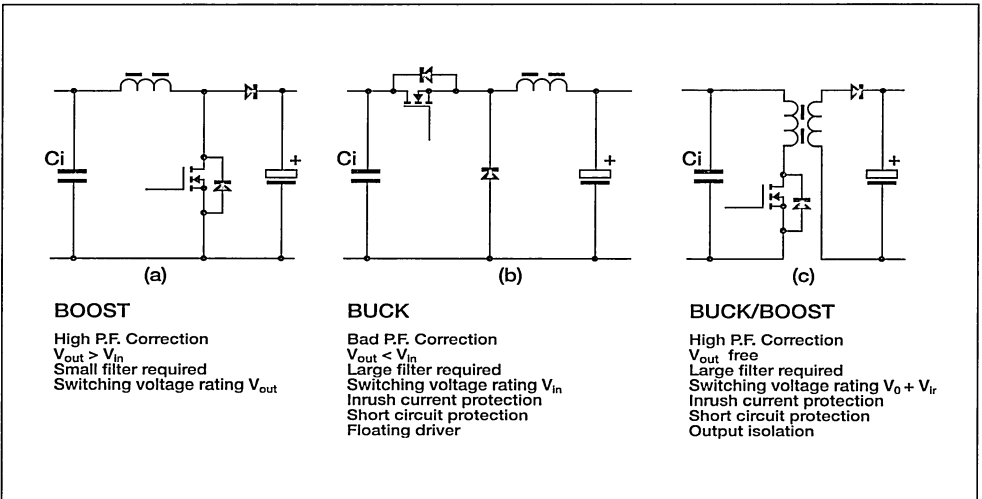
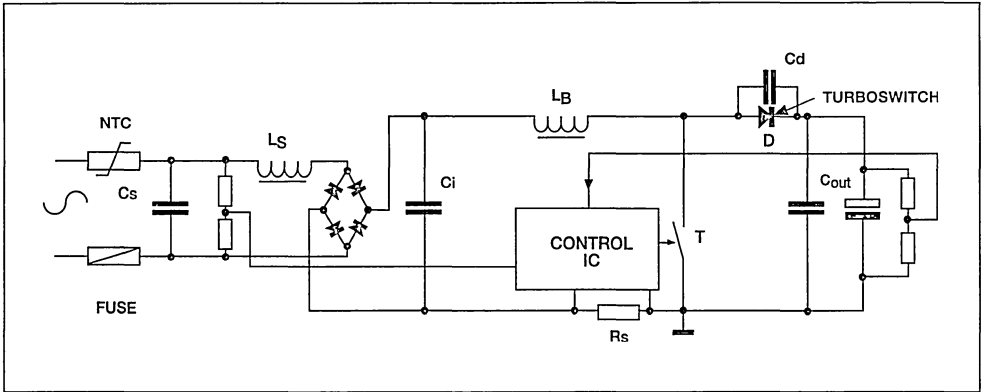


Figure 3. Basic topology of a Boost PFC



be expressed as:

$$\Delta i = \frac{(V_{out} - V_i) \cdot V_i}{F_s \cdot L_b \cdot V_{out}}$$

Typical values may be $V_i = 300V$, $V_{out} = 400V$ and $F_s = 70kHz$.

If the system is operating in continuous mode, a typical value of Δi may be 1A. This means an inductor value $L_b = 1mH$.

If instead the system operates in discontinuous mode, Δi might be 6A, in which case $L_b = 150\mu H$.

The inductor current waveforms represented by these ripple values are shown in figure 4.4.

Using continuous mode requires an inductance value about ten times that needed when operating in discontinuous mode; however, the low value of current ripple means that a cheap and efficient iron powder core can be used.

When operating with ripple currents larger than around 1A, the larger di/dt leads to the occurrence of skin effects and large eddy currents in an iron powder core, meaning that operation in discontinuous mode requires a more expensive ferrite core.

As the maximum possible flux density in an iron powder core is much higher than that in a ferrite core (around 1.5 Tesla in iron powder against 0.25 in ferrite), this means that the size (and hence cost) of inductor required in both cases is around the same. So, a cheaper system is achieved controlling a small current ripple by operating in continuous mode, despite the large inductor value.

3.3 Frequency modulation techniques

The switching frequency used can be constant or variable. If variable, the switching frequency can be controlled, or be free to vary within set limits. A circuit using variable switching frequencies can result in lower EMI and lower power losses, but the topology is harder to analyse, and the frequency characteristics sometimes more difficult to predict.

3.4 Choosing the switching frequency to match the power semiconductor

When using constant current ripple, increasing the switching frequency allows a reduction in the value of the boost inductor. However, increasing the switching frequency will lead to increased switching losses in the power semiconductors. In standard boost PFC circuits, conduction losses in the power switch will be lower than the switching losses, and consequently the switching frequency will be limited by the switching losses of the chosen power transistor, and the recovery losses of the boost diode.

Also, if compliance with VFG243 is required, using a switching frequency below 50kHz (where the constraints are more relaxed) will lead to a significant reduction in the cost of the filter.

Power MOSFET transistors are practical and cost effective in applications using up to 277V AC mains, with an output power of up to 3kW. The STE36N50-DK is a perfect solution for applications in the 1 to 3kW range. This device combines a low $R_{DS(on)}$ Power MOSFET with an ultra-fast

TURBOSWITCH™ diode in a low inductance and capacitance ISOTOP® package. An active snubber should be added to achieve maximum efficiency.

Above 3kW, IGBTs are more suitable due to their lower on-state losses and higher current capability. They can be used at up to 30kHz when used with a snubber.

The recovery behaviour of the diode at turn-on is responsible for the majority switching losses in PFC applications. Diodes of the new TURBOSWITCH family have a typical reverse recovery time (t_{rr}) of 25ns at 600V with a maximum V_f of 1.5V. The TURBOSWITCH A series significantly reduces losses and is available in ratings from 5A to 60A. If an active snubber is used, the B series is better suited due to its lower forward voltage drop.

4. MAINS FILTERING AND RFI NORMS

This analysis has been made with reference to EN60555 (reference [1]) and VDE0871B (reference [2]) norms and design requirements.

4.1. RFI Norms

The limits given by VDE0871/B are shown in figure 4.1. With increasing operating frequency, limits given by the norm decrease, while the noise measured across the normalized impedance increases (figure 4.2, 4.3). When the switching frequency is increased, the required filter attenuation is not reduced as much as one would expect. The margin between the limits and the noise is only improved by about 10dB/decade. As an example, an increase of switching frequency from 10kHz to 100kHz would improve the filter attenuation by about 10dB, but would increase the switching losses by a factor of 10.

4.2 Filter optimization parameters

Because of the increase in switching losses, instead of increasing the operating frequency, it is preferable to reduce the generated noise. The noise generated across the input capacitor is proportional to the current ripple. Figure 4.4 shows possible inductor current waveforms resulting from operation a) in continuous mode and b) in discontinuous mode.

Reducing the current ripple in the boost inductor by a factor of 20 will reduce the noise by 26dB. Continuous mode operation leads to minimum noise.

Operation with variable frequency is another means of noise reduction. This causes the noise spectrum to be spread over a wide frequency range, reducing the peak amplitude of the noise and so reducing the

amount of filter attenuation needed. Figure 4.5 shows the noise across the input capacitor (C_i) of a boost PFC operating with either fixed or variable frequency. A 10dB noise attenuation is achieved with a modulation depth of 10kHz.

The norms demand the use of a wider bandwidth for noise measurements above 150kHz.; the window is increased from 200Hz to 9kHz. The result is an increased measurement sensitivity at frequencies above 150kHz.

This means that when the switching frequency of a PFC is increased, the effect of low harmonics increases suddenly at 150kHz: they are in effect generating more noise. This fact has to be taken into account when choosing a suitable switching frequency.

In the range 1-30 MHz, the noise is conducted by the parasitic capacitance of the boost inductor. During turn-on switching of the power transistor, the discharge current of this parasitic capacitor can exceed 1A. Using a boost inductor with a low parasitic capacitance can therefore significantly reduce noise and filter cost.

Multi-section winding techniques can be used to produce inductors with low parasitic capacitance, see figure 4.6. When an iron powder core is used, a single layer winding is the best way to achieve a low parasitic capacitance.

Slowing the commutation is also a good means of noise reduction in the range 1-30 MHz. Figure 4.7(a) shows the noise spectrum of a P.F.C. with fast switching and conventional windings. Figure 4.7(b) shows the effects of slowing the commutation, while figure 4.7(c) shows the effects of using multi-section windings.

The parasitic capacitance between the power semiconductors and the heatsink can be kept to a minimum by using insulated packages such as ISOWATT220, ISOWATT218, ISOTOP or DO220I, minimizing asymmetrical filtering.

5. CURRENT CONTROL BOOST PFC WITH VOLTAGE FEED-FORWARD

Figure 5 shows a block diagram of a circuit implementing a current control boost PFC. A current reference is obtained by multiplying a number of feedback signals. This current reference is then compared with the average inductor current, and the results of the comparison are fed to the input of the PWM controller.

Figures 4.1 - 4.5

Figure 4.1. Limiting values of interference voltage

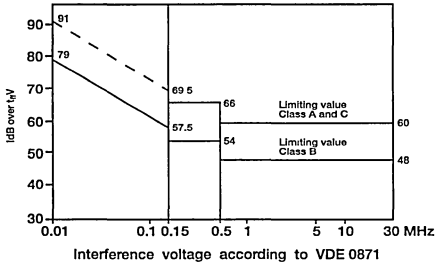


Figure 4.2. Normalized mains impedance

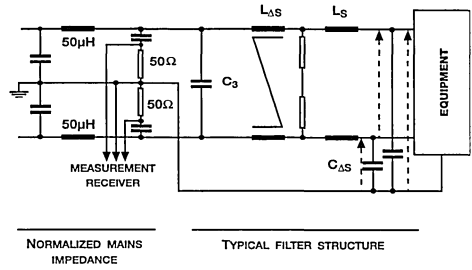
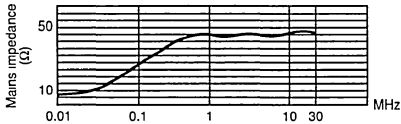


Figure 4.3. Overall filter performance between 30kHz and 150kHz



- Filter attenuation = - 40dB / decade
- Normalized mains impedance of measurement receiver = + 10dB / decade
- VDE 0871 constraints (see above) = + 20dB / decade
- Overall performance = - 10dB/decade

Figure 4.4. Continuous or discontinuous current mode: current ripple amplitude

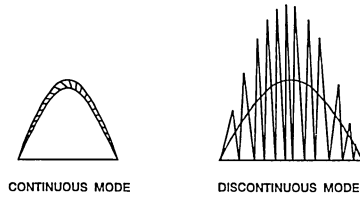
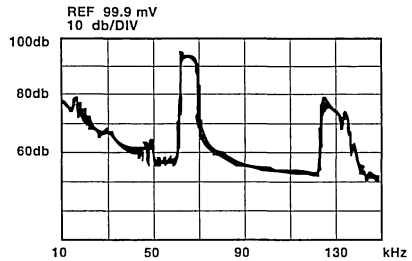
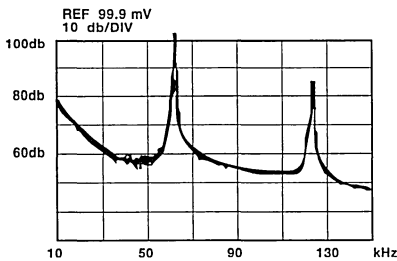


Figure 4.5. Symmetrical interference voltage

- Constant operating frequency

- Variable switching frequency



Figures 4.6 - 4.8

Figure 4.6. Frequency modulation method

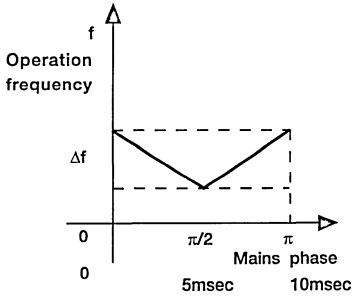


figure 4.7. Winding the Boost inductor

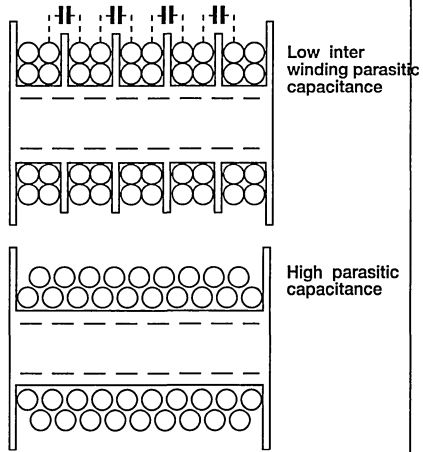


Figure 4.8. High frequency conducted noise

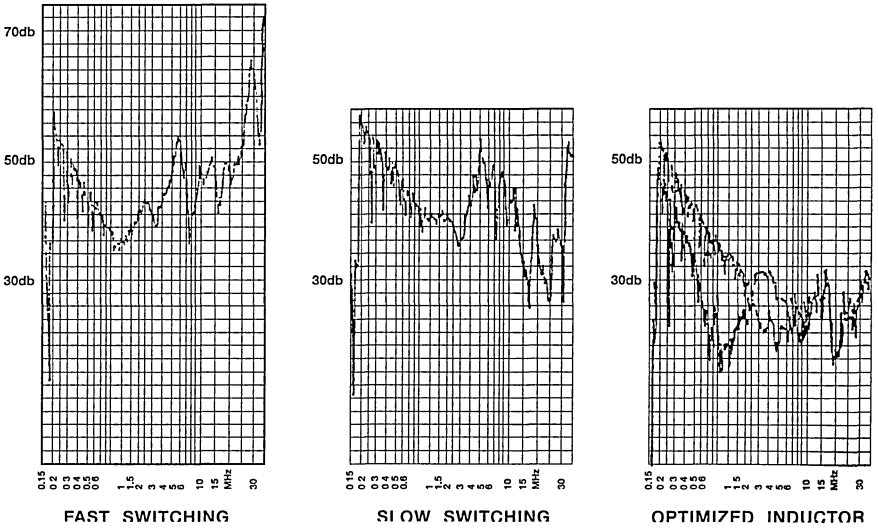
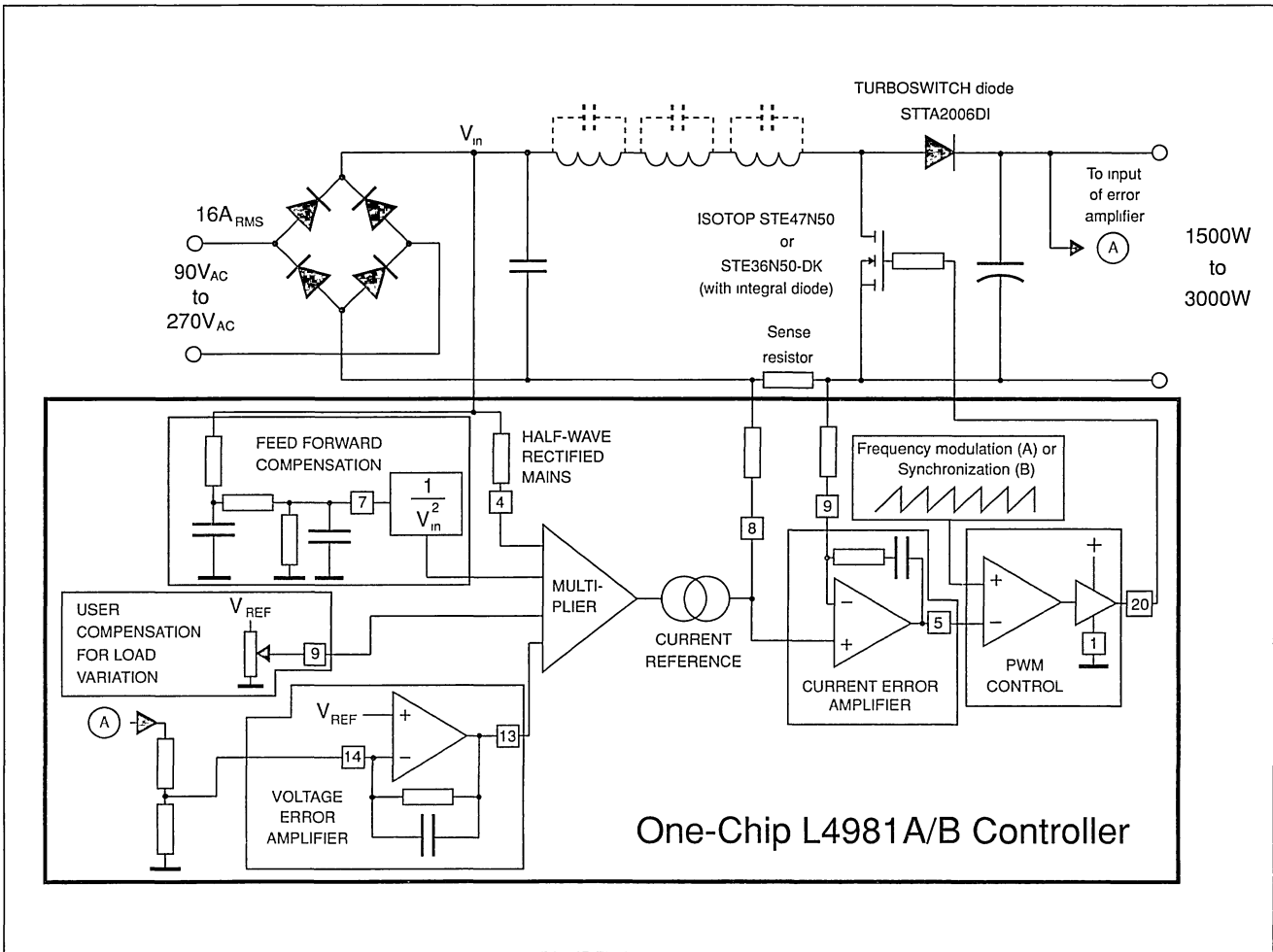


Figure 5. PFC circuit employing average current control



5.1 Operation of the PFC

To operate fully, the power factor corrector must maintain the following conditions:

- 1) The instantaneous value of the current drawn from the supply must follow the instantaneous value of the supply voltage, to ensure that the supply current waveform is sinusoidal and in phase.
- 2) The RMS power drawn from the supply must remain constant even if the the RMS supply voltage varies. This means that if the RMS value of the supply voltage falls, the RMS current drawn must increase.
- 3) The DC output voltage must remain constant despite variations in the load. For example if the DC output voltage falls the current through the load must be increased.

Condition (1) is maintained by feeding a half wave rectified signal at the mains frequency into the multiplier as described in section 1.1, while in certain applications, the voltage error amplifier can compensate for variations in both the RMS supply voltage and in the DC output voltage (as variations in the first lead to variations in the second).

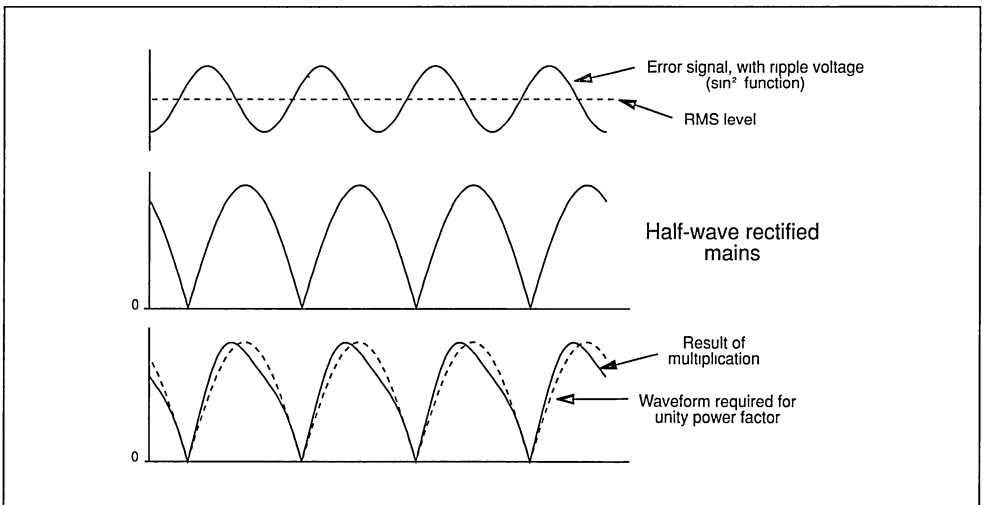
However, in most applications the voltage error amplifier cannot be used to compensate for variations in the input supply voltage. This is because the

output of the PFC is not pure DC - a small amount of ripple still exists on top of the DC signal, which at high levels of voltage and current cannot be eliminated with a realistically sized bulk capacitor. This ripple is at the frequency of the half-wave rectified mains signal, but is slightly out of phase. Hence if it is multiplied with the signal derived directly from the half-wave rectified AC mains, the result is a distorted half sine wave - see figure 6. A low-pass filter must therefore be applied to the input of the voltage error amplifier to remove this ripple. To remove enough of the ripple to allow the error amplifier to operate correctly, this filter usually designed to have a crossover frequency of around 20Hz.

However, the cutoff frequency of this filter decreases with the supply voltage. This is a problem where the value of the supply voltage is not known exactly, or where it is subject to large variations.

As an example, a typical system may be required to operate from a supply where the voltage can vary between 90V and 270V. As the crossover frequency decreases with supply voltage, the filter must be designed for correct operation of the system at the upper voltage limit. If the filter has a crossover frequency of 20Hz at 270V, the frequency will fall to a few Hz at 90V. This means that in this case the error amplifier has an unacceptably slow response to rapid changes of voltage at the input, and large

Figure 6. Distortion of error voltage



damaging overvoltages may occur on the output.

To account for rapid variations in the supply voltage a signal proportional to the RMS supply voltage must therefore be fed directly from the mains supply at the input. This technique is known as voltage feed forward.

5.2 Voltage feed-forward

The current reference is obtained by modulating the error voltage of the voltage loop with a signal derived from the half-wave rectified mains. The magnitude of this signal should be adjusted such that if the mains voltage doubles (with a constant load), the current reference, and hence the input current, halve. To keep the same voltage error signal requires division of the sinewave modulating signal by four. Using this method, the voltage loop bandwidth is kept constant and voltage overshoot is avoided with varying loads.

5.2 Variable frequency operation

The oscillator can operate at constant or varying frequency. In applications where a varying frequency is used, the noise spectrum can be spread adjusting the depth of modulation using an external resistor. In this way, the maximum inductor current depends upon the minimum operating frequency and there is no asymptote, giving a flat noise spectrum (see figure 4.5). All of these modes of operation are implemented in the L4981 control IC.

6. CONCLUSIONS

Whenever size and cost optimisation are required, a PFC circuit and its input filter must be designed as a whole. PFC circuits generate more noise than a conventional SMPS front end, and their mode of operation and the control techniques strongly influence the filter requirements.

Continuous current mode operation combined with a carefully designed frequency control technique leads to the lowest overall size and cost.

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DIGITAL POWER FACTOR CORRECTION WITH NON-SINEWAVE CURRENT

by P. Guillemain, J. M. Charreton, B. Maurice

ABSTRACT

Following the emergence of European and International standards concerning Power Factor and giving new limits to current harmonics content, electronic designers have to face the problem of Power Factor Correction (PFC).

This paper gives an example of a pre-regulator supplied from the 230V mains in which the harmonic correction function is performed by software using a standard microcontroller. This application, well-suited to applications in the power range below 1kW, is easy to adapt to a specific application, and avoids the use of dedicated PFC ICs. It is shown that such an incomplete harmonic compensation is a realistic solution in this power range, and the principles and methods of generating the correct mains current waveform. Closed loop voltage regulation, performed by software, is also described. This can be easily adapted to different types of loads. Practical results are given.

1. INTRODUCTION

Since the introduction of European and International standards limit current harmonics content, Power Factor limitation is becoming an important feature for mains supplied equipment.

Power Factor is defined by the ratio of the Real Power to the Total Apparent Power (see ref. [2]).

$$P.F = \frac{P}{S} = \frac{\text{Real Power}}{\text{Total Apparent Power}} \quad (1)$$

The theoretical calculation for a non-ideal sinusoidal signal gives the final definition of Power Factor.

$$P.F. = \cos \theta \times \cos \varphi \quad (2)$$

in which φ is the displacement angle between the input voltage and the in-phase fundamental current signal and $\cos \theta$ is the coefficient characterizing the distortion of the waveform. This coefficient is linked to the current harmonic content and is affected by the IEC555 standard.

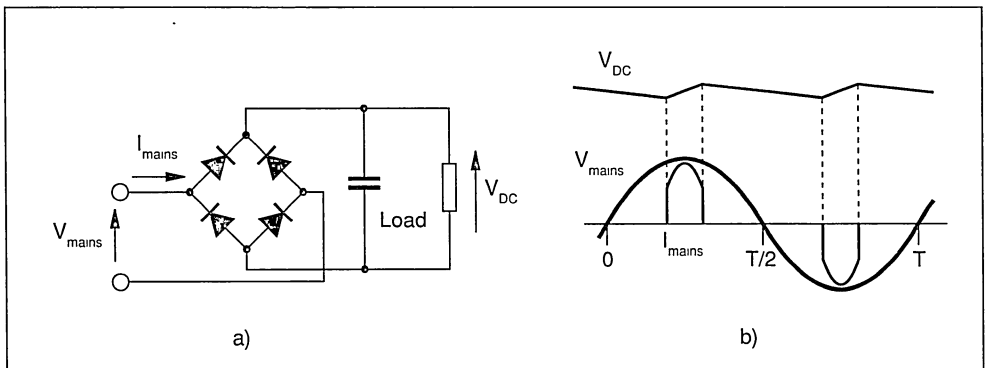
Currently, many applications already use dedicated PFC ICs.

This note describes an original PFC technique using a standard microcontroller which meets all the emerging standards.

The digital technique illustrated here allows the current waveform drawn from the mains to be shaped and its amplitude to be adapted to particular requirements.

In this example, a voltage pre-regulator is constructed

**Figure 1. a) Full-wave bridge rectifier front-end
b) Waveforms, showing current pulses**



using a boost topology to generate 400V DC voltage. This DC voltage is regulated by an ST9 microcontroller. The microcontroller also manages the harmonic reduction and other safety features.

2. BASIC PRINCIPLES

In most equipment supplied from the mains, the first step is to rectify the sine wave and to charge the bulk capacitor to obtain the DC voltage.

As shown in figure 1, the current drawn from the mains pulses at each peak of the line voltage. This pulsed current generates a number of harmonic currents and gives a poor power factor (typically between 0.5 and 0.7). This Power Factor does not comply with the permissible amplitudes of the various harmonic constituents defined by the present or future standard (EN6055, IEC555). The IEC555 limits are low and generally need special harmonic correction circuits.

One simple solution to force the harmonic levels under the limits of the standards is to draw a “flattened” non-sinewave current from the mains, as shown in the figure 2.

In figure 3a the input current takes the values 0 and $I_L/2$ at the beginning and at the end of each half period (i.e. when the mains voltage is zero or very close to it) and takes a DC value in-between.

Such a current waveform maximizes the form factor value and the useful power available from a given mains supply.

The shape of this current contains harmonics, each of which must remain under the acceptable limits fixed by the standards. One way of ensuring this is to calculate the Fourier transformation of the waveform and use this to calculate the corresponding maximum value of I_L available from the mains while keeping each harmonic under the permissible value. The calculation is given in appendix 1, and the results are summarized in figure 3b.

The simple current waveform shown in figure 3a gives a harmonic repartition in which the maximum value of I_L is limited (mainly by harmonics 19 and 21) to 2.8A - see figure 3b. With this value, the 50Hz fundamental current is 2.18A RMS, which corresponds to an input power of 500 Watts.

Optimizing the current waveform allows the input power available from the mains to be increased. By changing slightly the instant of the rising and the falling edge of the current (figure 3c), the current harmonic repartition is changed: the amplitude of harmonics 19 and 21 are reduced, while the other harmonics amplitudes are slightly increased (figure 3d).

A 5A line current can now be drawn from the mains giving a 4.3A RMS fundamental current corresponding to an input power of 1000 Watts.

3. PRACTICAL APPLICATION

Figure 4 shows the topology of the power factor pre-regulator in Boost converter configuration, and controlled by an ST9 microcontroller.

**Figure 2. a) PFC pre-regulator added to diode bridge
b) Waveforms, showing non-sinewave current**

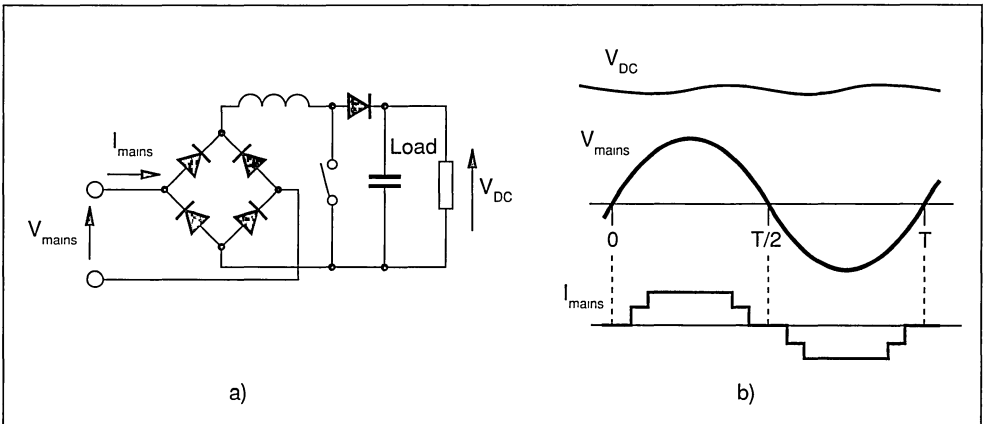


Figure 3. a) Simple current waveform
c) Modified current waveform

b) Spectrum of simple waveform
d) Spectrum of modified current waveform

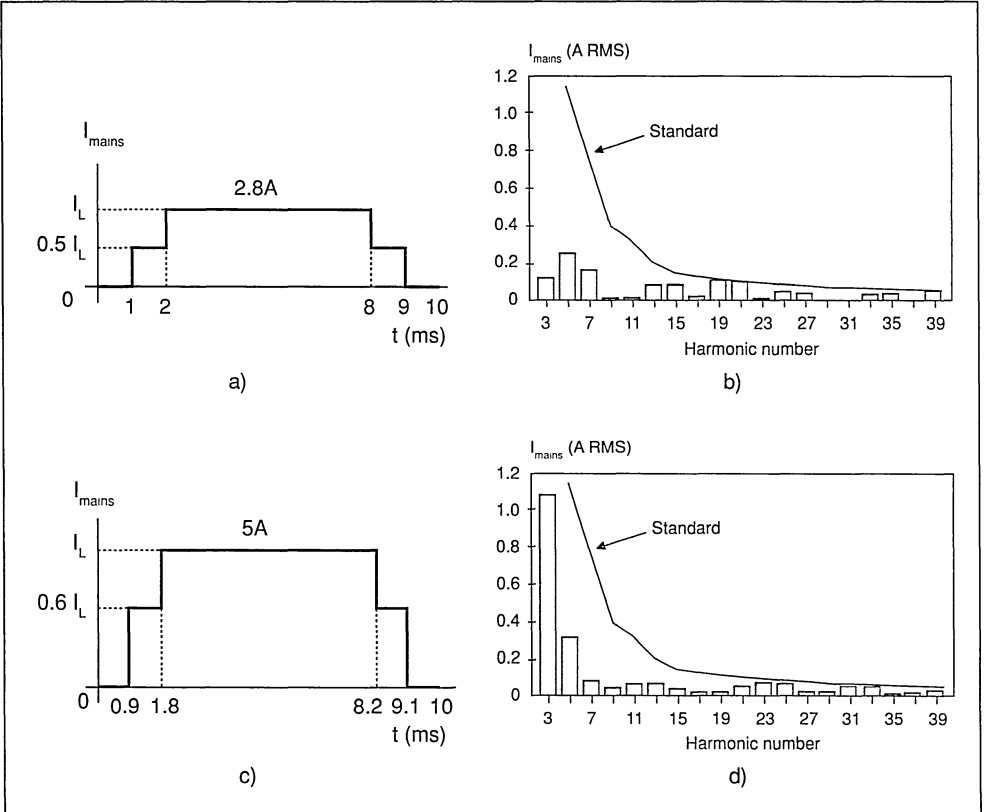
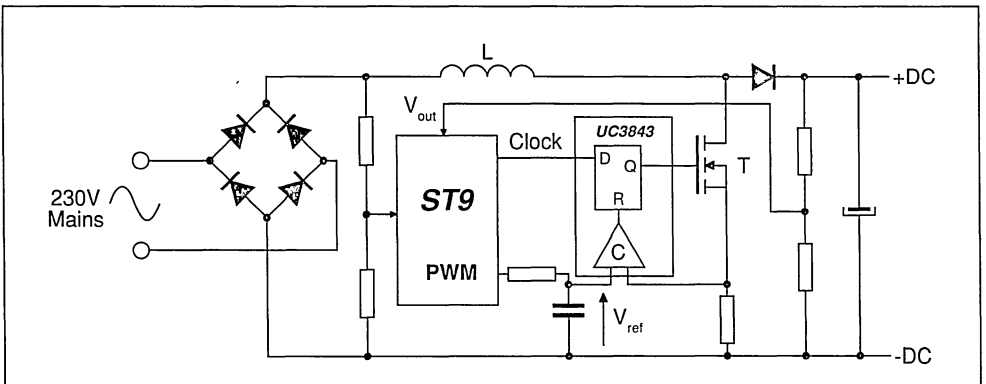


Figure 4. Block diagram of digital PFC with ST9 microcontroller and UC3843 PWM control IC.



This circuitry aims to deliver the power requested by the output load under a regulated voltage, and to draw from the mains a non-sinusoidal current such as shown in figure 3a.

Control of the mains current waveform and regulation of the output voltage requires two dependant closed loops.

3.1 DC output voltage regulation loop

When the load is varying, the output voltage is kept constant by the DC output voltage regulation loop (which has a slow loop response as detailed in section 4).

In order to do this, the output voltage is measured by one of the microcontroller A/D converter channels through a resistor bridge. A setpoint for the current regulation loop is calculated with the output DC voltage variations. This setpoint is provided by one of the microcontroller's internal timers in P.W.M. mode. After filtering, this gives a voltage reference V_{ref} as shown in figure 4.

3.2 Current regulation loop

The current regulation loop controlling the current waveform is based on a comparator, a flip-flop and a power transistor. This loop is fast, because the

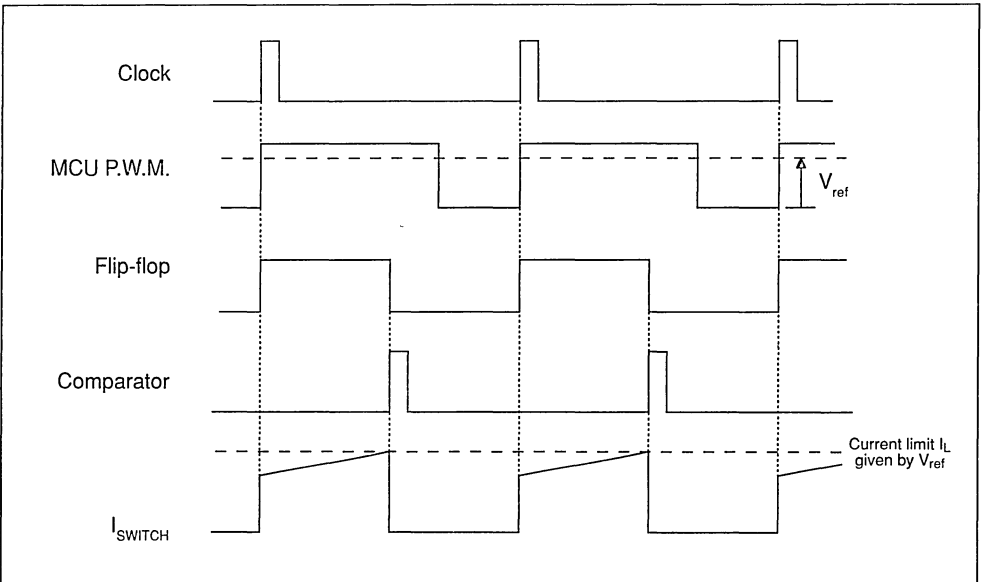
current in the switch reacts at the P.W.M. frequency. The filtered P.W.M. voltage reference V_{ref} given by the output voltage regulation loop is compared to the current-sense voltage, and defines the peak current value I_L in the power chopper transistor.

The P.W.M. current in the power transistor is synchronized with a clock pulse from the microcontroller (figure 5). On the rising edge of the clock, the flip-flop is set, the power transistor turns on, and the current in the inductor increases. When the current reaches the limit I_L given by V_{ref} , the flip-flop is reset by the comparator and the power transistor turns OFF. In the practical circuit, a UC3843 current mode P.W.M. control IC is used, which incorporates a comparator, a flip-flop and a 15 Volt buffer able to drive the power MOSFET directly.

3.3 Shaping the mains current waveform

In order to obtain the current outline shown in figure 3a, the value of I_L is computed at the beginning of each half cycle according to the corrections required by the output DC voltage regulation loop. The current waveform is synchronized with the mains voltage zero crossing. This zero crossing detection is performed using one of the microcontroller A/D converter channels (see section 4.3.).

Figure 5. Current regulation loop timing



The revised duty cycle calculated from this measurement is applied synchronously with the mains zero crossing. Three coefficients 0%, 50%, 100%, are automatically applied to this P.W.M. value at specific instant of each period (1,2,8,9 ms). This gives the current shape shown in figure 3a.

4. OPERATION OF VOLTAGE REGULATION

A simplified diagram showing the operation of the voltage regulation is shown in figure 6.

The value of the output capacitor C_{out} is 220 μ F. The power varies from 0 to 400 Watts with a fixed output voltage of 400V. The current generator supplying the output current I_{out} is a boost stage regulated in current mode. The reference voltage V_{ref} results from the filtered P.W.M. duty cycle generated by the microcontroller multifunction timer.

The voltage regulation loop, which keeps the output voltage constant when the load varies, is characterized by the transfer function of the current generator. It is obtained by measuring in open loop the relationship between the variation in duty cycle $\Delta\delta$ and the variation in the output current ΔI_{out} .

$$\Delta\delta_{(\%) } = 50 \times \Delta I_{out (A)} \quad \text{with:} \quad \begin{aligned} V_{line} &= 220V \\ C &= 220\mu F \\ V_{out} &= 400V \end{aligned} \quad (3)$$

The microcontroller samples the output voltage once per sine period (9ms after the previous zero crossing) using its A/D converter. It computes the difference between this measurement and the target value of the output voltage (V_{tgt}) stored in its memory, and compensates for the detected error (ϵ) by modifying (+/- $\Delta\delta$) the previous PWM duty cycle. The new PWM duty cycle will be:

$$\delta_{(\%) } = \delta_{n-1(\%) } + \Delta\delta \quad (4)$$

To complete static and dynamic output voltage regulation, the microcontroller uses two consecutive samples of the output voltage and computes the static error ϵ and its speed variation $d\epsilon/dt$ - see figure 7.

4.1 Static error compensation, S- Static parameter

At each sample of the output voltage, the microcontroller evaluates the voltage error ϵ_n between the output voltage V_{out} and the target voltage V_{tgt} stored in memory:

$$\epsilon_n = V_{out} - V_{tgt} \quad (@ t_n) \quad (5)$$

In order to compensate for this error, the microcontroller computes the current change (ΔI_{out})

Figure 6. Block diagram of voltage regulation

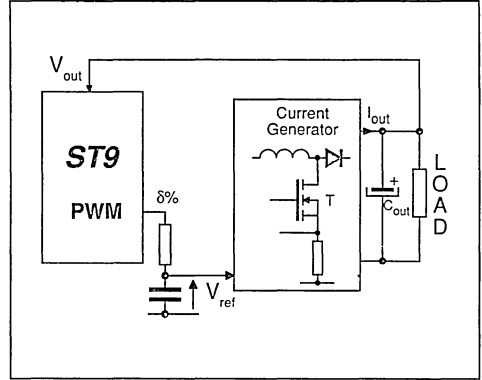
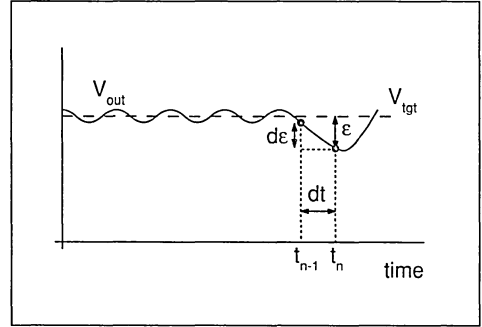


Figure 7. Calculation of ϵ and $d\epsilon/dt$



necessary to complete the capacitor charge during a fixed time (ΔT). The choice of this time value gives the response time of the voltage compensation.

$$\Delta I_{out} = -C \frac{\epsilon_n}{\Delta T} \quad (6)$$

Combining equations (3) and (6), we obtain the dutycycle variation necessary to compensate the voltage error.

$$\Delta\delta_{(\%) } = -50C \frac{\epsilon_n}{\Delta T} = S \times \epsilon_n \quad (7)$$

The static compensation parameter S depends on the output capacitor value and defines the chosen response time (ΔT). This parameter must to be adjusted according to the response time behaviour required for each particular application. It is stored in the microcontroller memory.

In this application $C = 220\mu F$, and $\Delta T = 50ms$

(response time 5 times longer than the sample period), giving the relation:

$$\Delta\delta_{(\%) } = -50 \times \frac{220 \times 10^{-6}}{50 \times 10^{-3}} \varepsilon_n = -0.2 \varepsilon_n \quad (8)$$

Example: on detecting an under-voltage of 10V, the duty-cycle will be increased by 2%; 50ms later the voltage variation will be completely cancelled.

4.2 Dynamic compensation, D - Dynamic parameter

Between two consecutive samples of the output voltage, and referring to the previous measurement, the microcontroller computes the speed variation of the error $d\varepsilon/dt$ using:

$$\frac{d\varepsilon}{dt} = \frac{\varepsilon_n - \varepsilon_{n-1}}{t_n - t_{n-1}} \quad (9)$$

This rate of variation of the output voltage results from a difference ΔI between the input and the output capacitor current, caused by a variation in either the load or the mains voltage. This current difference is directly given by the rate of the voltage variation

$$\Delta I = C \frac{d\varepsilon}{dt} \quad (10)$$

One solution to immediately stop the voltage variation is to compensate this current difference with an equal and opposite quantity. By combining (3) and (10), we obtain the corresponding change of δ .

$$\Delta\delta_{(\%) } = -50 \times \Delta I = -50 \times C \frac{d\varepsilon}{dt} = D \times d\varepsilon_{(V)} \quad (11)$$

The dynamic compensation parameter D depends on the output capacitor and the time interval (dt) between two consecutive measurements. This parameter must be adjusted to the particular application and then stored in the microcontroller memory.

In this application when $C = 220\mu\text{F}$ and $dt = 10\text{ms}$ between two voltage measurements, we get:

$$\Delta\delta = -1 \times d\varepsilon \quad (12)$$

Example: if detecting 50V between two successive measurements, the duty cycle must be increased by 50% to immediately stop this voltage variation.

The general relationship giving the duty cycle change after each voltage measurement is given by equation (13). This cancels the voltage variation and compensates the error voltage in 50ms. The S and D parameters are the regulation loop parameters, which must be calculated for each application and

stored in microcontroller memory.

$$\Delta\delta = (S.\varepsilon) + (D.d\varepsilon) \quad S = -\frac{50C}{\Delta T} \quad (13)$$

$$D = -\frac{50C}{dt}$$

With the numerical parameters, in our application, we obtain:

$$\Delta\delta_{(\%) } = -0.2 \varepsilon_{(V)} - 1 d\varepsilon_{(V)} \quad (14)$$

4.3 Voltage measurement and zero crossing technique

To avoid incorrect voltage measurement and to obtain good electrical immunity, a digital filter is implemented, using software. This filtering is achieved by taking the average of three output voltage measurements. Each measurement is separated in time by $100\mu\text{S}$.

In order to synchronize the current waveform with the mains voltage, zero crossing detection is performed by the software. The mains voltage is sensed every millisecond. Before the end of the period (9ms after the previous zero crossing), the A/D converter mode is switched to a continuous conversion mode. When the output voltage goes through 50V a zero crossing signal is generated after a 0.5ms delay. A reset of the time base is performed. Without zero crossing detection, synchronization is performed by default by the current time base timer.

4.4 Safety functions:

Software security functions can be easily implemented, due to the periodic output voltage measurement. This measurement is automatically performed every millisecond through the microcontroller A/D converter. The main safety function which can be implemented is output over-voltage detection. This stops the PFC when the output voltage reaches 450V. The system restarts with a P.W.M. duty cycle equal to zero when the output voltage falls below 420V. This security prevents dangerous over-voltages being generated caused by an open load commutation.

By using other A/D converter channels, several other safety functions have been implemented in software:

- voltage monitoring on the power switch gates (the system can be stopped if the gate voltage decreases under a fixed value: eg 13V).

- at power on, the PFC function only starts if the output voltage is greater than a predefined value.
- mains voltage monitoring. The system stops if mains voltage is too low.
- short circuit detection. A serial switch is often required to open the circuit and disconnect the load. The management of this serial switch can be made by the microcontroller, which also provides a soft start.

5. EXPERIMENTAL RESULTS

A 400V DC pre-regulator including harmonic correction controlled by a SGS-THOMSON ST9 microcontroller is shown in appendix 2. The implementation of Power Factor Correction within the ST9 requires one multifunction timer (for PWM generation) and three channels of the A/D converter (for voltage monitoring). Several other peripherals functions of the ST9 remain free for the user:

- one multi-function timer,
- 4 A/D converter channels,
- one Serial Communication Interface (SCI),
- one Serial Peripheral Interface (SPI),
- one watchdog timer
- Direct Memory Access controller

Consequently, the ST9 microcontroller is able to manage both a PFC pre-regulator and a downstream converter application such as a 3-phase induction

motor drive (see reference [4]), a U.P.S., and also the associated bus management.

5.1 Static response of the PFC

In this case, the PFC is permanently loaded with a 400W resistive load.

Figure 8 compares the mains current waveform obtained with and without Power Factor Correction.

When the digital PFC is used:

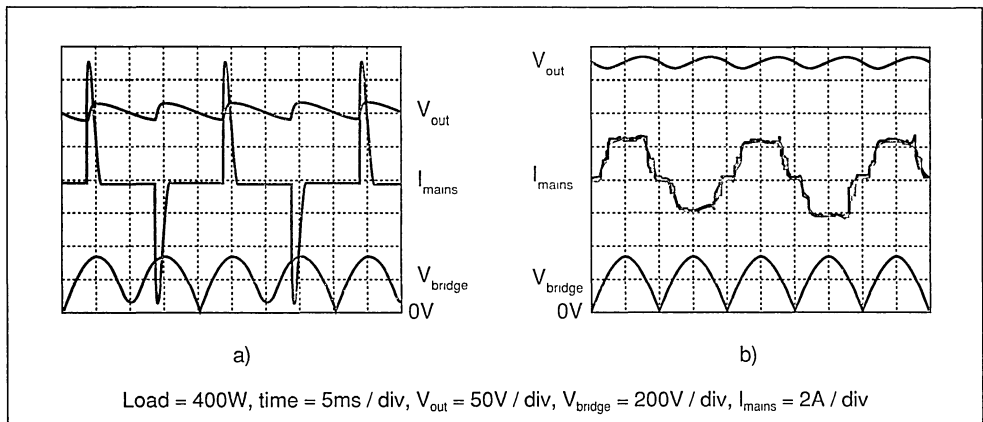
- The mains current is in phase with the mains voltage
- The output voltage ripple is reduced to 15V peak to peak
- the peak current is limited to 2.2 A instead of 7A.

The DC voltage regulation loop was also tested, maintaining a DC output voltage of 400V while supplying a 400W load when the mains voltage varies from 140V to 300V. The variations in the DC output voltage were less than 2%.

Harmonic measurements on the mains current made using a Fast Fourier Transform for an output power of 400W are shown below in table 1.

	I_{mains}	Harmonic order # n				
		1	3	5	7	9
I_{RMS} with PFC	1.8	1.7	0.07	0.25	0.10	0.02
I_{RMS} without PFC	2.6	1.6	1.4	1.0	0.60	0.35
Standard limits	-	-	2.3	1.14	0.77	0.40

Figure 9. System waveforms: a) With PFC
b) Without PFC



By comparing the measurements made without PFC it can be seen that the two fundamental currents have the same magnitude in both cases. When the PFC is ON, the fundamental current and the mains current have the same order of magnitude and the other current harmonics are drastically reduced.

The overall Power Factor can be calculated from current values shown in table 2. The phase angle between the input voltage and the mains fundamental current is very close to 0 ($\cos \theta = 0.99$), while the overall power factor is given by the waveform distortion coefficient (see reference [2])

$$\frac{I_{\text{fundamental term}}}{I_{\text{mains}}} = \cos \theta$$

which gives overall power factor values of:

$$\cos \theta \text{ with PFC} = 0.95$$

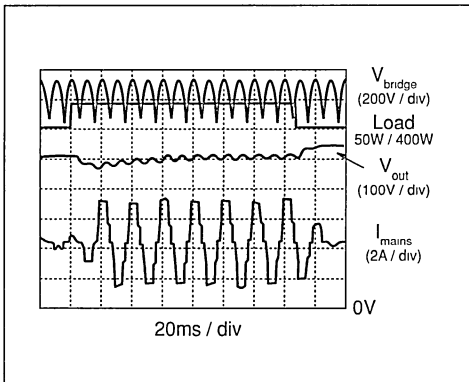
$$\cos \theta \text{ without PFC} = 0.60$$

Despite the non-sine waveform of the current drawn from the mains, the overall power factor is very close to 1.

5.2 Dynamic response

Figure 9 shows the dynamic response of the digital PFC when the load varies from 50W to 450W. For this load variation, the maximum transient output voltage drop is 40V, and the voltage recovers its regulated value within 100ms. For applications requiring faster dynamic response time, this last value can be decreased by reducing the response time (ΔT) as described in section 4.1. No occurrence of voltage overoscillations was observed.

Figure 9. Dynamic response of system when load is changed from 50W to 400W



6. CONCLUSIONS

For applications in the power range under 1kW, Power Factor Correction using the non-sinewave current concept allows the current harmonic content to be maintained under the limits fixed by the standards. Additionally, despite the non-sine waveform current drawn from the mains, the overall power factor is very close to 1.

The static and dynamic responses are sufficient for many applications, particularly for the majority of motor drives used in industrial and home appliances environments.

In applications where a microcontroller is already used, it is easy to implement such a PFC controlled and regulated by software. Other features can be implemented, such as fast current loop, voltage regulation, safety functions by voltage monitoring and softstart procedures.

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Appendix 1. Calculation of Fourier Harmonics

All periodic functions can be factorized by the Fourier Transform using the following equation:

$$F(t) = a_0 + \sum_{n=1}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t)$$

Taking $\theta = \frac{2\pi}{T}t = \omega t$, we get:

$$a_0 = \frac{1}{2\pi} \int_{-\pi}^{\pi} f(\theta) d\theta, a_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(\theta) \cos n\theta d\theta, b_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(\theta) \sin n\theta d\theta$$

With a current waveform $f(\theta)$ such as that shown in figure A1, and considering the current as an odd function, the a_0 and a_n coefficients are zero, and the b_n coefficients can be written:

$$b_n = \frac{2}{\pi} \int_0^x f(\theta) d\theta, a_n$$

If I is the maximum value of current, b_n is given by the following expression:

$$b_n = I \frac{2}{n\pi} [k \cos n\alpha_1 - \cos n\alpha_2 + \cos n\alpha_2 - \cos n\alpha_3 + k(\cos n\alpha_3 - \cos n\alpha_4)]$$

The expression of the Fourier transform function

becomes:

$$F(\theta) = \sum_{n=1}^{\infty} b_n \sin n\theta$$

Table 2 shows the calculation for each odd harmonics with:

$I = 2.8A$ with $k = 0.5, \alpha_1 = \pi/10, \alpha_2 = 2\pi/10, \alpha_3 = 8\pi/10$, and $\alpha_4 = 9\pi/10$

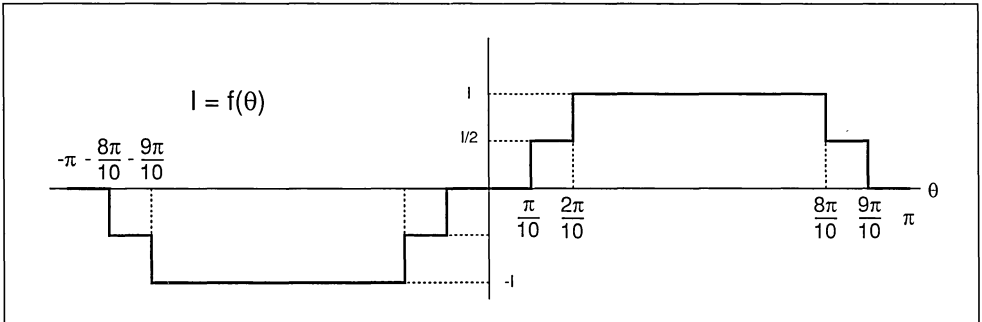
and with:

$I = 5A$ with $k = 0.6, \alpha_1 = 0.9\pi/10, \alpha_2 = 0.8 \times 2\pi/10, \alpha_3 = (2-0.8) \times 8\pi/10, \alpha_4 = (2-0.9) \times 9\pi/10$

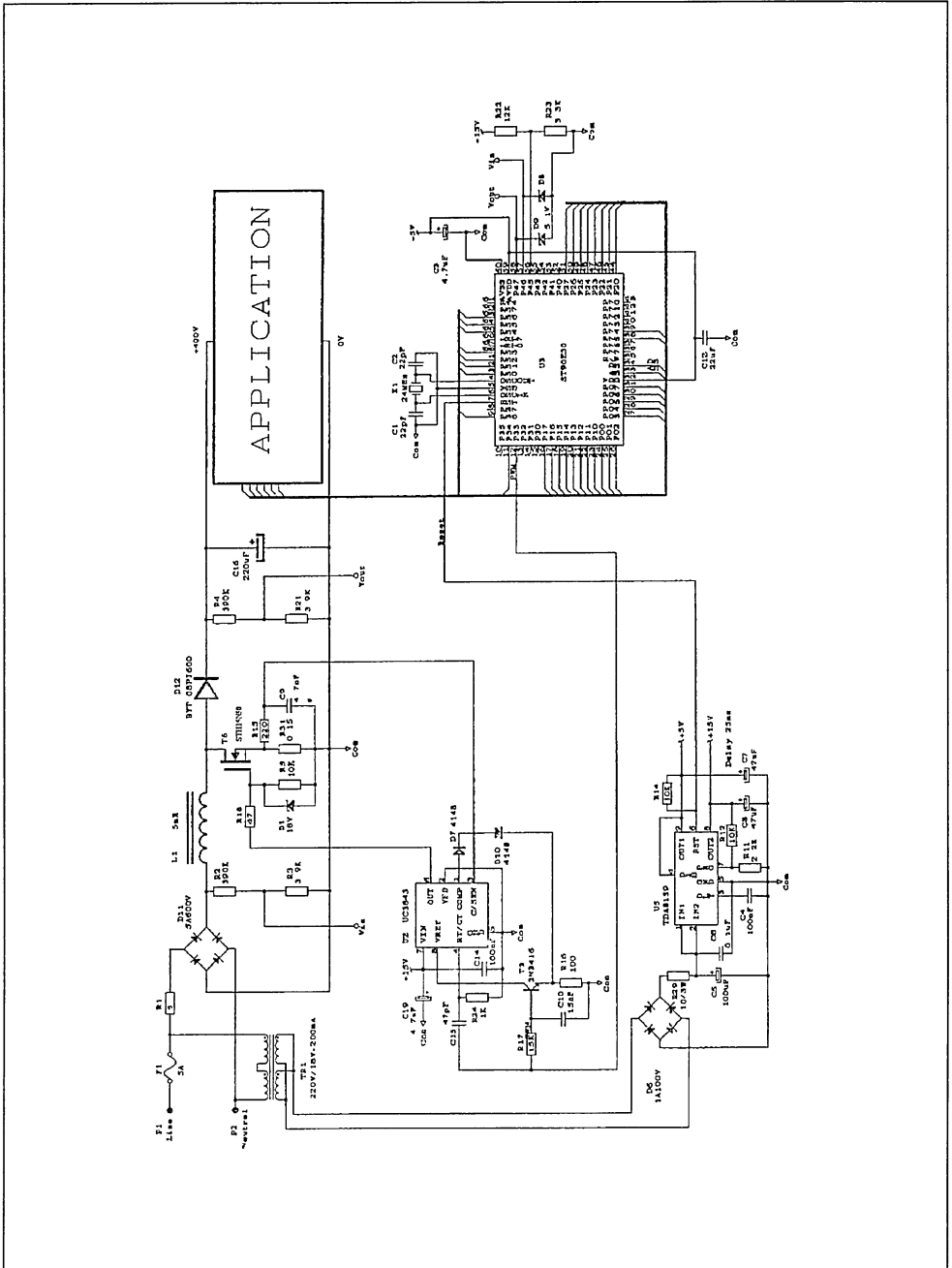
The limit of the standard are noted for reference.

Harmonic	Standard limit(A _{RMS})	Calculated Harmonics	
		I=2.8A	I=5A
1		2.18	4.33
3	2.3	0.117	1.04
5	1.14	0.252	0.309
7	0.77	0.161	0.074
9	0.4	0.02	0.044
11	0.33	0.016	0.068
13	0.21	0.087	0.069
15	0.15	0.084	0.039
17	0.132	0.021	0.014
19	0.118	0.117	0.021
21	0.107	0.106	0.055
23	0.098	0.015	0.084
25	0.09	0.05	0.076
27	0.083	0.042	0.03
29	0.073	0.006	0.027
31	0.073	0.006	0.06
33	0.068	0.034	0.052
35	0.064	0.036	0.017
37	0.061	0.009	0.018
39	0.058	0.057	0.034

Figure a1. Current waveform used in calculation



Appendix 2. Schematic of Power Factor Corrector using ST90E30 microcontroller.



RESONANT CONVERTER TOPOLOGIES

by M. Bildgen

1. INTRODUCTION

Increasing the frequency of operation of power converters is desirable, as it allows the size of circuit magnetics and capacitors to be reduced, leading to cheaper and more compact circuits. However, increasing the frequency of operation also increases switching losses and hence reduces system efficiency. One solution to this problem is to replace the "chopper" switch of a standard SMPS topology (Buck, Boost etc.) with a "resonant" switch, which uses the resonances of circuit capacitances and inductances to shape the waveform of either the current or the voltage across the switching element, such that when switching takes place, there is no current through or voltage across it, and hence no power dissipation - see figure 1. A circuit employing this technique is known as a resonant converter (or, more accurately, a quasi-resonant converter, as only part of the resonant sinusoid is utilized).

A Zero Current Switching (ZCS) circuit shapes the current waveform, while a Zero Voltage Switching (ZVS) circuit shapes the voltage waveform.

2. ZERO CURRENT SWITCH

A typical Zero Current Switch consists of a switch, S, in series with the resonant inductor L_{RES} , and the

resonant capacitor C_{RES} connected in parallel. Energy is supplied by a current source. The circuit and waveforms are shown in figure 2.

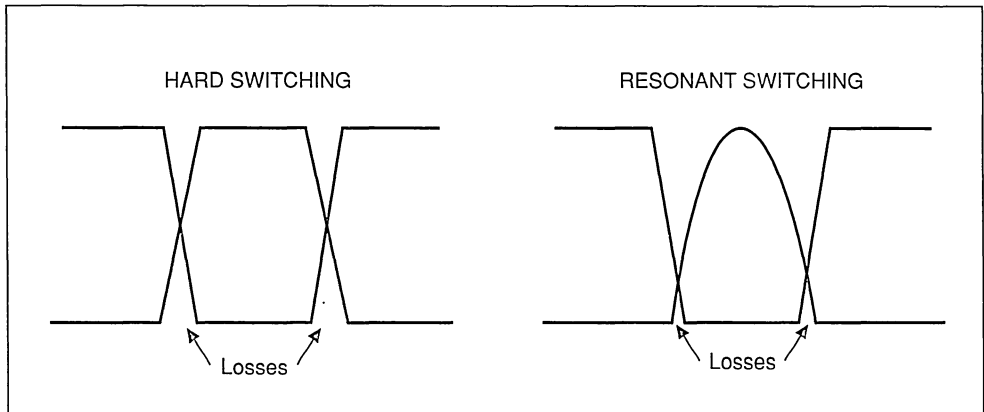
If an output transformer is used, in certain cases its parasitic inductance can be used as the resonant inductance (in both this and the zero voltage topology). However, as its value is generally not known, the resonant frequency will not be fixed, which may cause problems in the circuit design.

When the switch S is off, the resonant capacitor is charged up with a more or less constant current, and so the voltage across it rises linearly.

When the switch is turned on, the energy stored in the capacitor is transferred to the inductor, causing a sinusoidal current to flow in the switch. During the negative half wave, the current flows through the anti-parallel diode, and so in this period there is no current through or voltage across the switch; and it can be turned off without losses.

This type of switching is also known as thyristor mode, as it is one of the more suitable ways of using thyristors; these devices will only turn off if the current through them is forced to zero, which occurs naturally in this topology.

Figure 1. Current and voltage waveforms of hard and resonant switching systems



3. ZERO VOLTAGE SWITCH

A typical Zero Voltage Switch consists of a switch in series with a diode. The resonant capacitor is connected in parallel, and the resonant inductor is connected in series with this configuration. A voltage source connected in parallel injects the energy into this system. The circuit and waveforms are shown in figure 3.

When the switch is turned on, a linear current flows through the inductor. When the switch turns off, the energy that is stored in the inductor flows into the resonant capacitor. The resulting voltage across the capacitor and the switch is sinusoidal. The negative half-wave of the voltage is blocked by the diode. During this negative half wave, the current and voltage in the switch are zero, and so it can be turned on without losses.

4. POWER SEMICONDUCTORS IN RESONANT CONVERTERS

Because they require a substantial drive current, Bipolar transistors are not generally used in resonant converters, unless the base drive is provided by the resonant circuit itself (for example in TV deflection circuits and fluorescent lamp ballasts). Power MOSFETs and IGBTs, with their effectively capacitive inputs and low drive energy requirements, are the most frequently used types.

The graph in figure 4 shows the die size of Power MOSFETs and IGBTs required to conduct 1 amp with a voltage drop of 2 volts, against the maximum rated voltage. For low voltage applications, the MOSFET is interesting, as the die size is very small (and so the device is cheap). However for higher breakdown voltages, the IGBT is more suitable, as

Figure 2. Full-wave zero-current switch - topology and waveforms

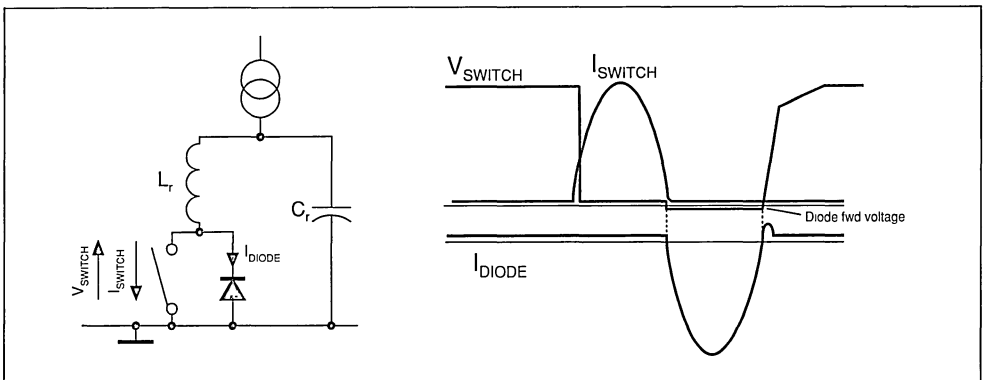


Figure 3. Full-wave zero-voltage switch - topology and waveforms

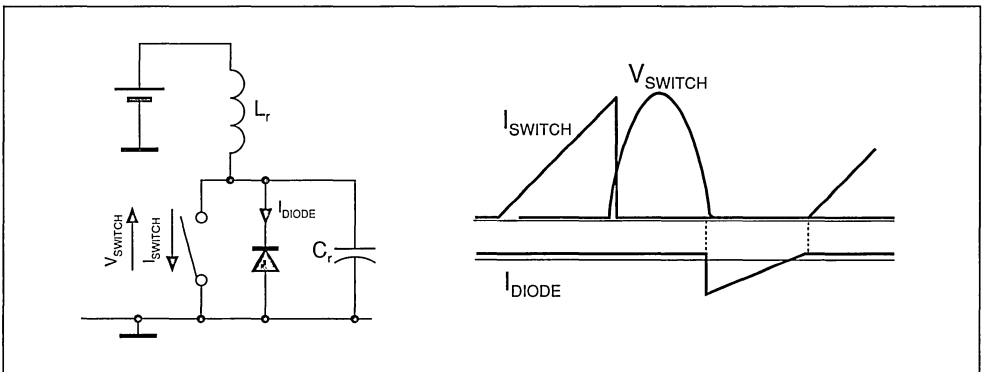
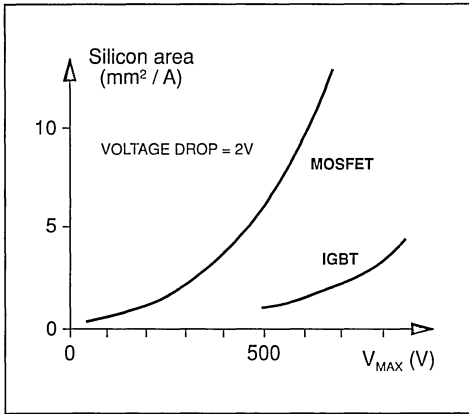


Figure 4. Comparison of MOSFET and IGBT



the die size required is almost constant approaching the maximum rated voltage.

4.1 MOSFETs

The MOSFET has a resistive behaviour in its on state, and the output characteristic passes through zero. It can conduct a small current with a very low voltage drop.

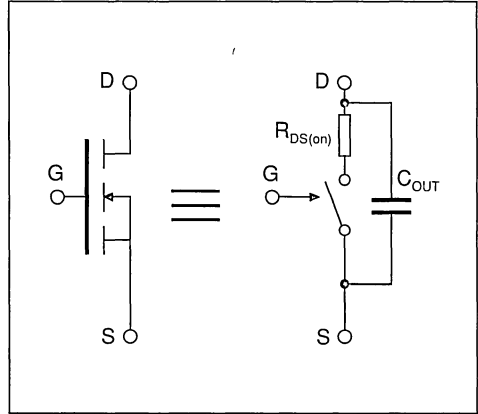
4.1.1 Zero Current Switch

A MOSFET can be modelled as an ideal switch with a series resistance, and a capacitor connected in parallel - see figure 5. Every time it is turned on, the parallel capacitor is discharged through the resistance and $(0.5 \times C_{out} \times V_{DS})$ units are lost. A MOSFET in a Zero Current Switch will have to turn on with a high drain-source voltage, and there will be capacitive switching losses. Additionally, the reactive overcurrent in the switch is very high, and as the MOSFET does not perform well in overcurrent conditions, the conduction losses will be very high. Therefore the MOSFET is not very suitable as a Zero Current Switch.

4.1.2 Zero Voltage Switch

In a Zero Voltage Switch, the MOSFET turns on without any voltage between drain and source, and so there are no capacitive switching losses. There is no reactive overcurrent and the conduction losses are not very important. The MOSFET does have to turn off a current, but as the switching times of a MOSFET are small, the turn off losses will not be excessive.

Figure 5. Simple MOSFET model



4.2 IGBTs

The IGBT has a threshold voltage of around 0.7V; a voltage drop lower than this value is not possible. The "resistive part" of the output characteristics of an IGBT is very low, and so it can conduct large currents with a low voltage drop. It is thus most suitable for use at high current densities.

An IGBT can be simply modelled as a pnp-transistor driven by a MOSFET. The disadvantage of this structure is the turn off. If a pnp transistor is to be turned off quickly, a positive base current must be supplied, to force the carriers in the base to recombine and stop the device conducting. In the IGBT, the base of the pnp stage cannot be accessed directly, and so this current cannot be delivered at turn off, meaning that the device continues to conduct while the carriers recombine "naturally". During this time, a current tail appears.

4.2.1 Zero Voltage Switch

In a Zero Voltage Switch, the IGBT must turn off a current. Even if the voltage across the switch rises with a limited dV/dt (sinusoidal waveform), the current tail phenomenon means that turn off losses will be important. Therefore the IGBT is not very suitable for zero voltage switching.

4.2.2 Zero Current Switch

In a Zero Current Switch, the external circuit defines the current in the switch. This current tends to zero, and hence the IGBT does not turn off current, so no tail appears. Another problem that can occur with

the IGBT, latching, does not occur in this mode. Even if the IGBT latches at the maximum current, it can turn off later because the current is defined by the external circuit. The carriers that remained in the base of the pnp-transistor can be recovered by a positive current into the base. In a Zero Current Switch, the negative half wave of the resonant current flows through the antiparallel diode. During that time, a negative voltage is applied to the IGBT. A current flows through the body diode of the internal MOSFET into the base of the pnp-transistor.

5. TWO-SWITCH RESONANT CONVERTERS

As in standard power converters, for higher power applications, two switches can be connected as shown in figure 6 to form a half-bridge resonant converter. The same passive components are used for the resonance of both switches, and a transformer has been added to drive the load.

5.1 Thyristor Mode

In the example above, the commutation frequency of the switches (f_{sw}) is lower than the resonant frequency of the circuit (f_0). This results in a "dead" zone in the transformer waveform, giving a poor overall efficiency. If the switching frequency is increased, as shown in figure 8, the resonant waveforms overlap and the transformer is used more

efficiently. However, the switch now has to turn on at a non-zero current level, and as the diodes turn off at a high current level (e.g. point A in figure 7), losses due to their recovery time will be high.

5.2 Dual Thyristor Mode

The effect of the diode recovery time can be reduced by increasing the switching frequency further - see figure 8. In this case, the diode turns off at zero current.

The main advantage of this type of circuit is that the intrinsic diode of the MOSFET, which has very poor reverse recovery characteristics, can be used in the circuit, removing the need for a further discrete diode.

CONCLUSIONS

Resonant converter topologies can be used to increase circuit switching speeds, allowing the cost of circuit magnetics to be reduced, while still keeping switching losses to a minimum. Full wave rather than half wave topologies are generally used, as they generate less EMI. Capacitive switching losses when turning on with a high drain-source voltage means that MOSFETs are more suitable for Zero-Voltage than Zero-Current switches, while its poor turn-off characteristics mean that the IGBT is more suited to Zero-Current topologies.

Figure 6. Half-Bridge Zero-Current resonant converter

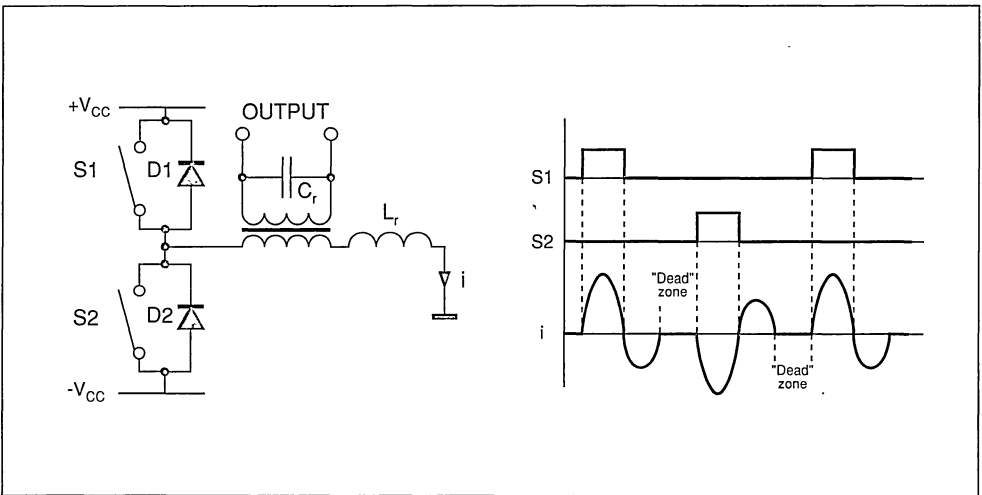
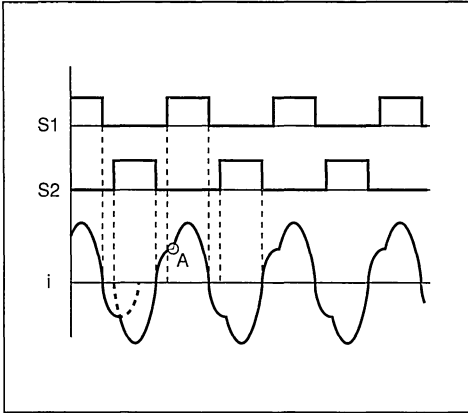
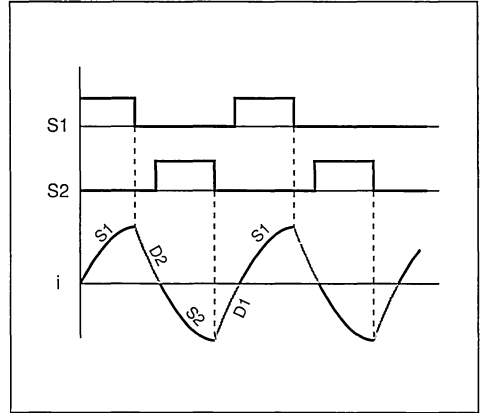


Figure 7. Half-Bridge waveforms with $f_{sw} > f_0$ Figure 8. Half-Bridge waveforms with $f_{sw} \gg f_0$ 

IGBTS IN RESONANT CONVERTERS

by R. Letor, S. Musumeci, F. Frisina

ABSTRACT

The aim of this paper is to give help to the designers of resonant converters in the selection of IGBTs for use in their circuits. A method of characterizing IGBTs in resonant converters is developed and used to obtain graphs demonstrating the dependence of the power losses of the IGBT on certain key parameters, the circuit topology and the application requirements.

1. INTRODUCTION

Resonant and quasi-resonant switching techniques have been widely used in high-frequency power conversion systems, leading to reductions in size, weight and power losses. By forcing the switching transitions to take place when there is either zero current through or zero voltage across the power switch allows the switching losses to be minimized. However, the necessary current or voltage rating of the device used is much higher than that required in a device used in a conventional hard-switching system, and so the devices are more expensive.

MOSFETs are often chosen for the power switch in soft-switching applications, due to their high speed and easy drive. However, for medium and high power applications, their high conduction losses begin to cause problems, and IGBTs begin to become more attractive. Even in hard-switching applications, their higher current density, lower saturation voltages and high reliability mean that they are often used to replace MOSFETs.

Although in the past few years a large number of applications have been developed and a number of product families introduced, the behaviour of IGBTs in resonant circuits is still poorly understood, and designers are often reluctant to use them in this type of application.

This paper presents guidelines for the selection of IGBT devices for resonant applications, taking into consideration circuit parameters such as topology, power, switching frequency and input-output voltage ratio.

2. RESONANT TOPOLOGIES

The idealised switching waveforms of a Zero-Current (ZC) converter are shown in figure 1; a) shows "half wave" operation, while b) shows "full wave" (similar waveforms can be visualised for Zero-Voltage (ZV) systems by simply substituting the current waveform for the voltage and vice versa).

The parameters which characterise the ZC switching waveforms in both modes of operation are:

- at turn on, the current slope (di/dt) and the maximum voltage (V_{off})
- during conduction, the peak current ($I_{C(max)}$) and the conduction time (t_{on})
- at turn off, the voltage rise delay time (t_{delay}) and the current slope (di/dt).

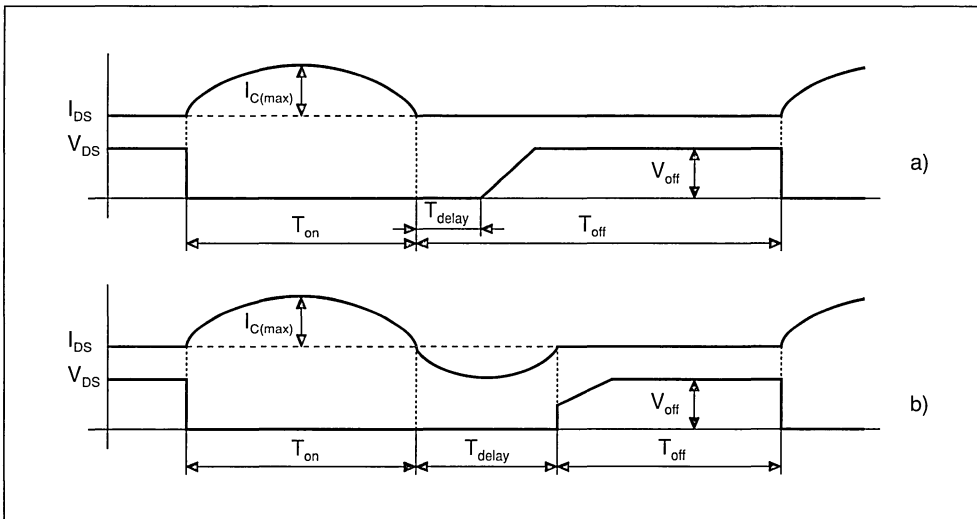
For a ZC converter, the above parameters have current in place of voltage, and vice versa.

These parameters determine the power losses of the system, and second-order effects during the switching transients. The approach followed in this paper is to examine separately the effect of each of these key parameters on the behaviour of a number of different commercially available IGBTs in soft-switching applications.

3. IGBT DEVICES

The current density of an IGBT is higher than that of a Power MOSFET with the same voltage rating, particularly in the case of high voltage devices, as the on-voltage and hence conduction loss of the device is considerably lower. However, in hard-switching applications the switching losses of the IGBT can be much higher due to the effect of the "tail current" (see reference [6]), which results from the delay in turn-off of the bipolar section of the IGBT caused by the slow recombination of the minority carriers in its base. In soft-switching applications these losses can be reduced significantly, if the switching times required are longer than the minority carrier lifetime.

Figure 1. Idealized switching waveforms of a ZC converter: a) "Half Wave" mode b) "Full Wave" mode



A number of IGBT devices are commercially available with a variety of saturation voltages and fall times. Figure 2 shows how, by increasing the gain of the intrinsic bipolar transistor, it is possible to reduce the saturation voltage, at the cost of increased fall time. The IGBTs considered in this paper are characterised in the following way:

- IGBTs with a very low saturation voltage ($V_{CE(sat)} = 1.5V$, fall time = $2\mu s$);
- Standard IGBTs ($V_{CE(sat)} = 2.2V$, fall time = $0.8\mu s$)
- Fast IGBTs ($V_{CE(sat)} = 3.2V$, fall time = $0.3\mu s$)

4. CHARACTERIZATION OF IGBTs

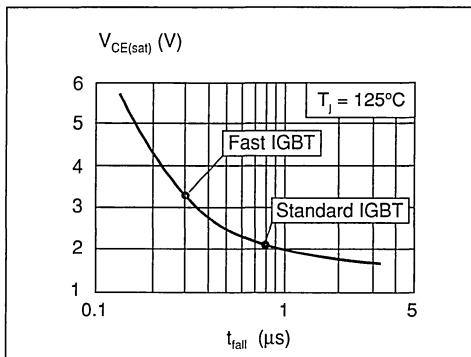
4.1 Test circuits

Figure 3 shows two circuits useful for the characterisation of IGBTs. a) shows a ZV test circuit, while b) shows a ZC circuit. The circuits allow simulation of a wide variety of operating conditions, and allow the di/dt and the maximum switching current to be controlled separately.

It should be noted that in ZV switchings the initial voltage can be negative, and the di/dt must be kept high.

In this case the Power MOSFET S1 is used to control the di/dt and the maximum current. In ZC switchings the di/dt is lower than is the case with ZV,

Figure 2. Standard vs. fast IGBTs



and depends upon both the resonant frequency and the maximum load current. The di/dt is controlled by means of the inductor L.

Figure 4 shows circuits to examine turn-off transients in a) ZV and b) ZC circuits. These circuits allow the di/dt, dv/dt and the voltage rise delay time to be controlled separately.

In the ZV resonant converter the parameters which influence the power losses most at turn-off are the collector current and the dv/dt - the di/dt is large enough to have no influence on the switching power losses.

Figure 3. Investigating turn-on: a) Test circuit for ZV turn-on c) ZV turn-on waveforms

b) Test circuit for ZC turn-on d) ZC turn-on waveforms

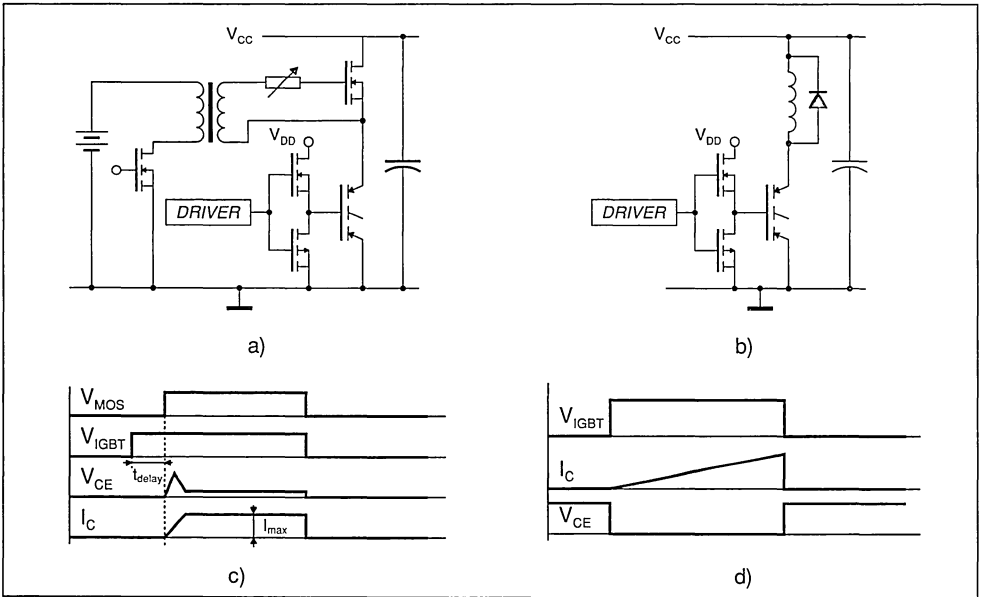
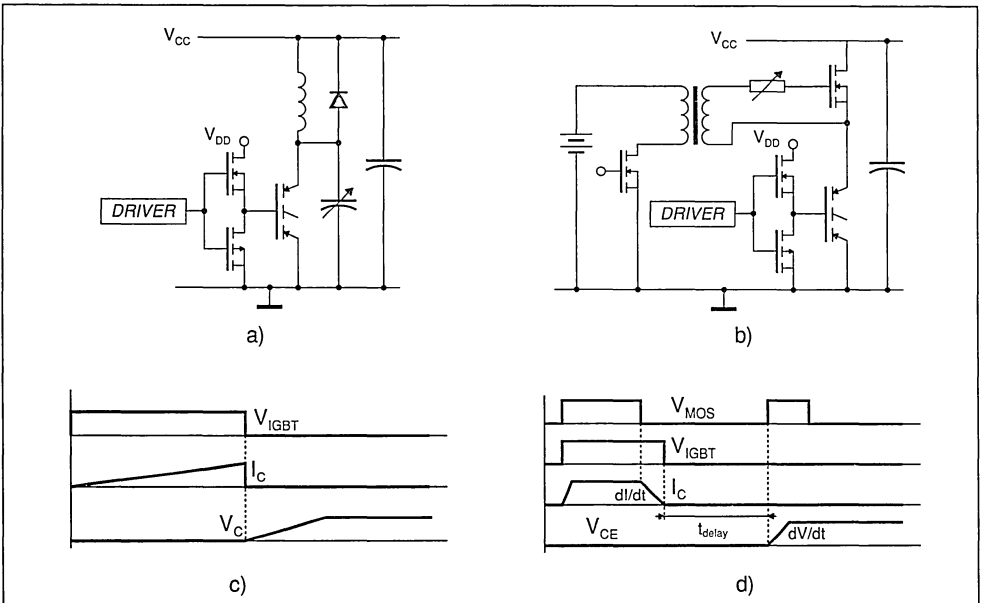


Figure 4. Investigating turn-off: a) Test circuit for ZV turn-off c) ZV turn-off waveforms

b) Test circuit for ZC turn-off d) ZC turn-off waveforms



4.2 Experimental Results

Figure 5 shows collector current, dynamic saturation voltage and power loss waveforms for ZV turn-on. It can be seen that the peak value of the switching power losses is very similar to the value of the conduction losses. Figure 6 shows ZV turn-on losses for different values of current slope, with a fixed conduction current.

Figure 7 shows waveforms for the turn-on of the ZC circuit. The turn-on losses are very similar to those in the ZV circuit.

Figure 8 shows the influence of the current tail on the dv/dt at turn-off of the ZV circuit. Figure 9 shows the same waveform at various temperatures (note

the different order of magnitude on the power losses axis compared with figure 6). It can be seen that at very high junction temperatures the power losses begin to increase exponentially.

Figure 10 shows turn-off waveforms for ZC operation with various values of voltage rise delay time. Figure 11 shows that increasing the voltage rise delay time reduces the turn-off losses very quickly.

Figures 12 and 13 show the effects of di/dt and junction temperature on the power losses at turn-off for ZC operation.

Figures 14 and 15 compare the waveforms and turn-off losses of different IGBT types in ZC converters.

Figure 5. ZV turn-on waveforms at 125°C

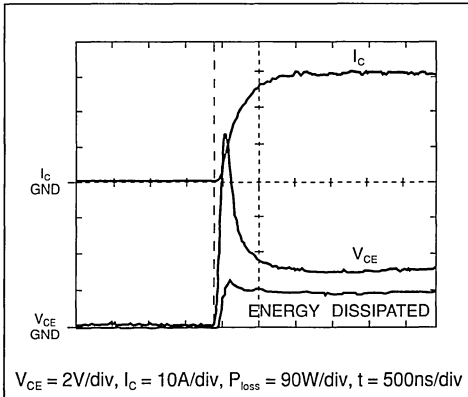


Figure 7. ZC turn-on waveforms at 25°C and 125°C

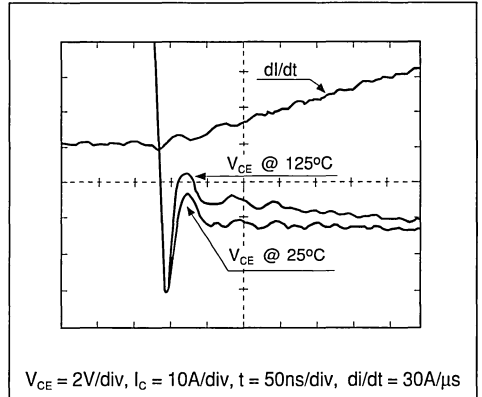


Figure 6. Variation of ZV turn-on losses with T_j for various values of di/dt

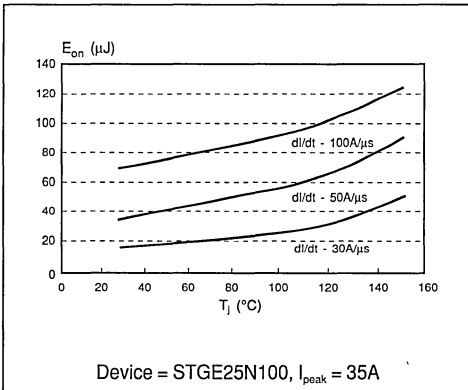


Figure 8. ZV turn-off waveforms at 150°C

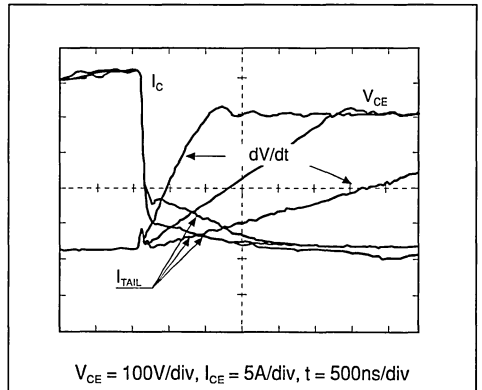


Figure 9. Variation of ZV turn-off losses with dV/dt , for various values of T_j

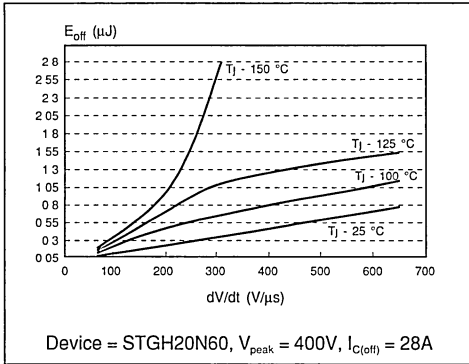


Figure 10. ZC turn-off waveforms at $100^\circ C$, varying the delay time. $di/dt = 18A/\mu s$

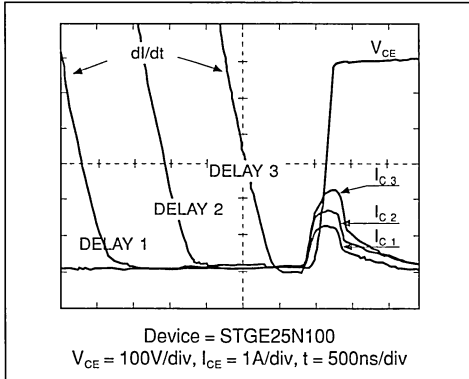


Figure 11. ZC turn-off losses against delay time, with various values of dI/dt

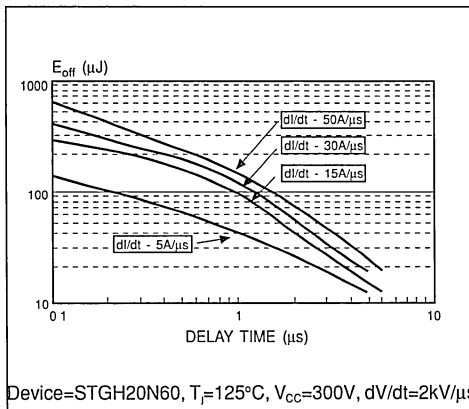


Figure 12. Variation of ZC turn-off losses with dI/dt , for various values of delay time

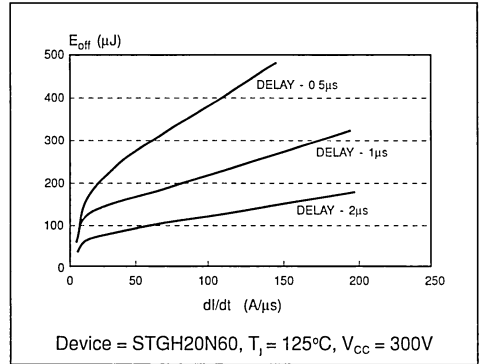


Figure 13. Variation of ZC turn-off losses with T_j , for various values of delay time

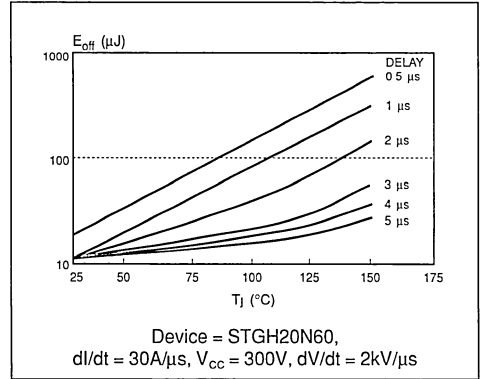


Figure 14. ZC turn-off waveforms for three types of IGBT

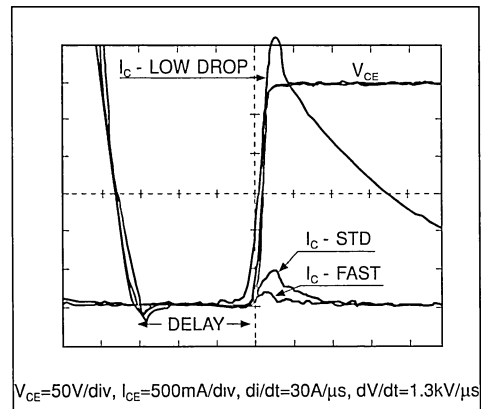
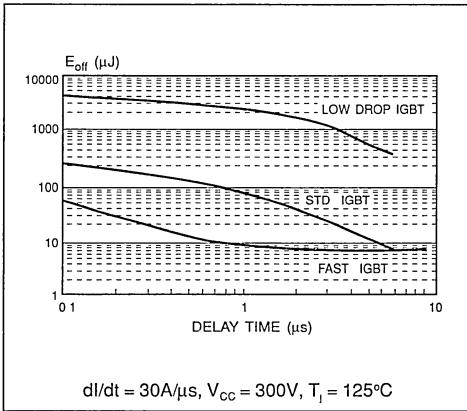


Figure 15. Comparison of turn-off losses of three types of IGBT with equal die size



5. USING THE RESULTS OF THE CHARACTERIZATION

5.1 Evaluation of turn-on losses

As shown above, the power losses are much lower at turn-on than at turn-off. It can also be seen from figure 5 that the energy loss waveform at turn-on is in the shape of a step; so as a first approximation the saturation voltage can be assumed to be a square wave with amplitude equal to its maximum value in the calculation of the turn-on losses.

5.2 Evaluation of turn-off losses

Calculation of the turn off losses requires evaluation of the following parameters:

- the di/dt
- the dv/dt
- the delay time.

These are determined by the design parameters of the converter such as the switching frequency f_s , the resonant frequency f_r , the voltage conversion ratio M , and the power ratings. As an example, for a buck ZC Quasi Resonant Converter (QRC) rated at 1.4kW with 300V input voltage and 100V output, these parameters may be:

$$M = f_s / f_r = 1/3 \rightarrow f_r = 3f_s$$

$$di/dt = 2\pi f I_{max} \text{ where } I_{max} = 2I_{out} = 28A$$

$$t_{on} = 1/2f_r$$

$$t_{delay} = t_{on} = t_r/2 = 1/2f_r$$

while for a buck ZV QRC rated at 1.4kW with 100V input and 70V output, they may be (assuming $V_{max} = 4 \times V_{min}$)

$$f_r = 1.5f_s / (1-M)$$

$$dv/dt = 2\pi f V_{max}$$

$$t_{on} / T = 1 - (f_s/f_r)$$

Different voltage ratings were chosen with the aim of comparing the behaviour of the same device in both resonant configurations, for converters having the same power ratings.

5.3 Power Losses vs Switching Frequency

Figure 16 shows the variation of power losses with frequency for a 600V - 20A IGBT in ZV operation, calculated using the values given in the examples of the previous section. It can be seen that the high voltage IGBT used (the ZV technique usually requires a high voltage device) has high switching losses even at low switching frequencies. Also, this application is characterized by a large duty cycle, increasing the conduction losses. As IGBTs seem to be more suited to ZC-QRCs, figure 17 compares the losses resulting from the use of a standard and a fast IGBT, along with a Power MOSFET with the same silicon size and voltage rating for comparison.

5.4 IGBTs and MOSFETs in ZC QRC

From figure 17 it follows that a MOSFET device requires a die size three or four times that needed by an IGBT in the same converter, in order to reduce the conduction losses to acceptable levels. However, on the other hand, IGBTs are affected much more by the switching frequency than MOSFETs. To calculate the optimum operating frequency of an IGBT, the maximum possible power dissipation in the application must first be calculated; the frequency can be found from figure 17.

As an example, with the set of conditions:

$$T_{amb} = 50^\circ C$$

$$T_{j(max)} = 125^\circ C$$

$$R_{th(heatsink)} = 3^\circ C/W$$

$$R_{th(j-c)} = 0.8^\circ C/W$$

the maximum possible power dissipation is:

$$P_{tot} = (T_{j(max)} - T_{amb}) / (R_{th(heatsink)} + R_{th(j-c)}) = 20W.$$

Figure 17 thus gives a maximum switching frequency of 100kHz for a standard IGBT, and 280kHz for a fast IGBT.

Figure 16. Variation of power losses with frequency for a ZV Buck QRC

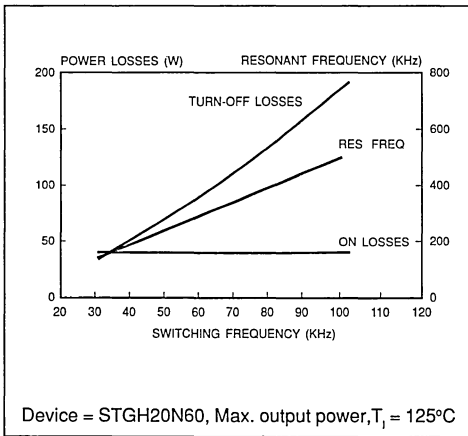
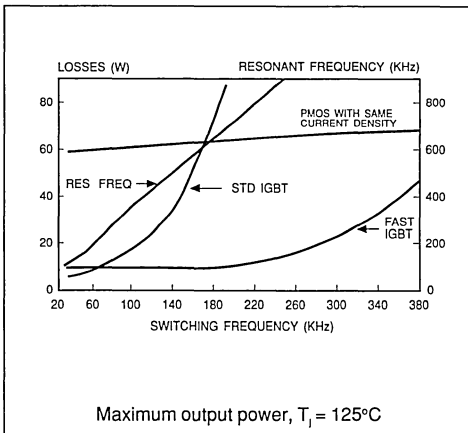


Figure 17. Comparison of losses for IGBT and MOSFET in a ZV Buck QRC



CONCLUSIONS

This paper presented a method of characterizing the behaviour of IGBTs in resonant converters. The switching characteristics of various types of IGBTs were examined, and the results used to obtain graphs of the variation of power losses with respect to various parameters. It was noted that:

- the switching losses are mainly affected by the bipolar transistor behaviour of the IGBT;
- as a first approximation, the losses related to the

dynamic saturation voltage can be included in the conduction losses for the frequency range considered;

- the "low drop" IGBT is not suited to use in this type of application due to its high switching losses;
- operating temperature is of key importance, due to the effects of the intrinsic bipolar of the IGBT.

Example applications were calculated using a buck QRC in both ZC and ZV operation. The ZC QRC proved to be the more attractive both for the lower voltage and current ratings required for the IGBT and the performance of the power switch under ZC conditions.

Possible switching frequency ranges were calculated for two types of IGBT, and also a Power MOSFET. It was shown that although the MOSFET can operate at much higher frequencies, it requires a much larger silicon area (and hence is more expensive) to keep down conduction losses to an acceptable level.

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CALCULATION OF THE LOSSES IN A CHOPPER TOPOLOGY

by T. Castagnet

1. INTRODUCTION

In chopper applications, the components which dissipate power are:

- the input rectifier bridge;
- the free wheeling diode; and
- the power switch.

This paper analyses the losses in the chopper in the fast rectifier (using a STTA806DI as an example) and the IGBT (using a STGP10N50).

The input capacitor has a small value in order to reduce inrush current at start-up, and to reduce input low frequency harmonic currents. The input voltage is 100 Hz full-wave rectified (see figure 5). The transistor is controlled through a low gate resistance (20Ω) in order to increase turn-off speed. Turn-on is controlled by the transistor emitter inductance.

2. CALCULATION OF THE LOSSES IN ONE SWITCHING CYCLE

2.1 The fast rectifier

For "free wheeling" operation, we can neglect the turn-on and off state losses:

$$e_{\text{ton}} = 0 ; e_{\text{off}} = 0 ;$$

The dissipated energy of the device mainly consists of the conduction energy, e_{on} , and the turn-off losses energy, e_{toff} :

$$e_{\text{on}} = T_{\text{sw}} \cdot (V_{\text{to}} \cdot I_{\text{FAV}} + R_{\text{d}} \cdot I_{\text{FRMS}}^2)$$

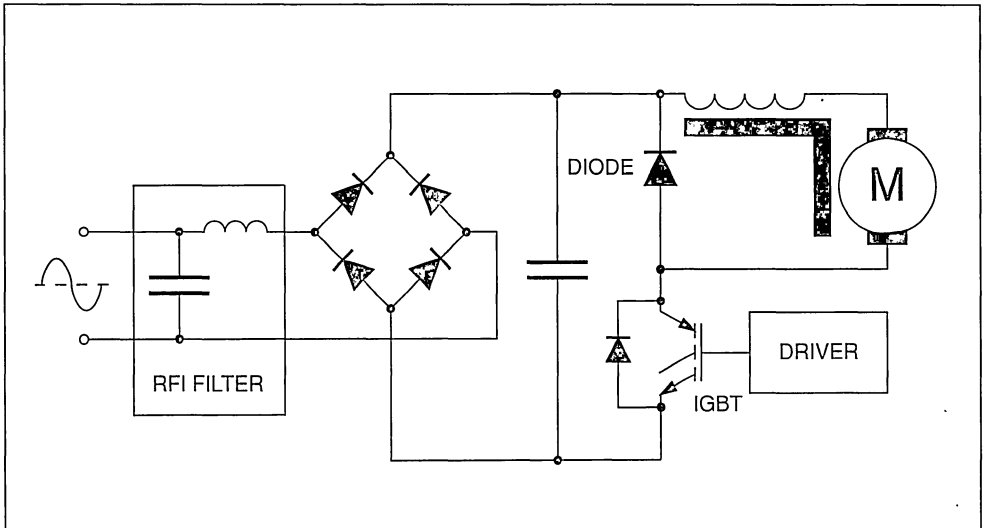
with $I_{\text{FAV}} = \delta' \cdot I_{\text{p}}$; $I_{\text{FRMS}} = I_{\text{p}} \cdot \sqrt{\delta'}$ on high inductive load (square waveforms)

δ' = diode duty cycle (1 - transistor duty cycle)

$$e_{\text{toff}} = (S \cdot V_{\text{R}} \cdot I_{\text{RM}}^2) / (6 \cdot dl_{\text{F}}/dt)$$

with $dl_{\text{F}}/dt = dl_{\text{C}}/dt$ (controlled by transistor drive)

Figure 1. Basic diagram of a general DC motor control



2.2 The IGBT transistor

In motor control applications the switching frequency f_{SW} of the IGBT transistor is generally less than 20kHz; therefore we neglect its gate energy e_G . The off state energy e_{OFF} is also negligible. The dissipated energy is the conduction energy, e_{ON} , the turn on energy, e_{ton} , and the turn off energy, e_{toff} :

$$e_{ON} = T_{SW} \cdot (E_O \cdot I_{CAV} + R_T \cdot I_{CRMS}^2)$$

with $I_{CAV} = \delta \cdot I_p$, $I_{CRMS} = I_p \cdot \sqrt{\delta}$ on high inductive load (square waveforms)

$$e_{ton} = V_{CE} \cdot [(I_{RM} + I_C)^2/2 + S \cdot I_{RM} \cdot (2 \cdot I_C + 3 \cdot I_{RM})/6] / (dl_C/dt)$$

$$\approx 1.1 \cdot V_{CE} \cdot (I_{RM} + I_C)^2 / (2 \cdot dl_C/dt)$$

where diode parameters I_{RM} and S depend mainly from dl_C/dt & T_{JD}

$$e_{toff} \approx V_{CE} \cdot I_T \cdot t_T / 2 + I_C \cdot V_{CE}^2 / (2 \cdot dV_{CE}/dt)$$

The information given by this formula can often be found in the device datasheet. The value for a particular application is obtained using the figures 2., 3. and 4. : e_{toff} is almost proportional to V_{CE} and I_C .

Figure 2. Turn-off energy e_{toff} versus applied voltage V_{CE} . $R_G=47\Omega$, $I_C=10A$, $T_J=100^\circ C$

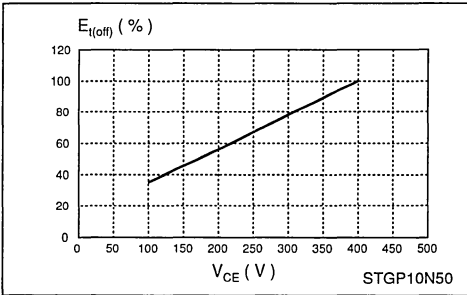


Figure 3. Turn-off energy e_{toff} versus collector current I_C . $R_G=47\Omega$, $V_{CE}=400V$, $T_J=100^\circ C$

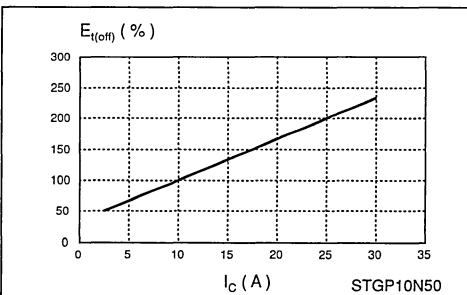
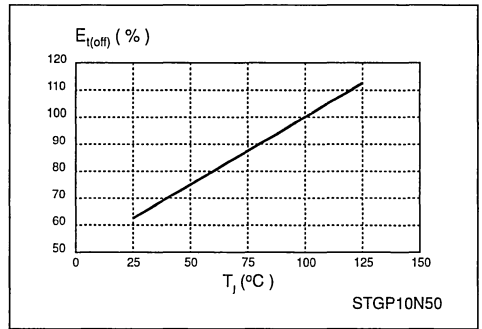


Figure 4. Turn-off energy e_{toff} versus junction temperature T_J . $R_G=47\Omega$, $I_C=10A$, $V_{CE}=400V$, $V_{GE}=15V$



3. CALCULATION OF LOSSES IN ONE MAINS HALF CYCLE (10mS)

3.1 An approach to the calculation of the losses

In chopper applications, devices turn on and off the motor current I_{mot} , while the voltage across them is the direct line voltage U_d ; these two values define the chopper losses.

In one mains half cycle, the dissipated energy can be calculated by adding the losses of all switching cycles during this time. Modelling I_{mot} and U_d simplifies the evaluation.

For switching losses, it can be assumed we suggest that the motor current I_{mot} is almost constant ($I_C = I_{AV}$), and that the direct voltage U_d is full wave rectified ($U_d = 2 \times \sqrt{2} \times U_A / \pi$).

$$E_{SW} = \sum_j [e_{SW}(V_{CEj}, I_{Cj})] = \sum_j e_{SW}(U_{dj}, I_{AV})$$

with $1 \leq j \leq n \approx T / T_{SW}$, and $n \geq 50$

$$E_{SW} = 2 \cdot e_{SW}(U_A \cdot \sqrt{2}, I_{AV}) / \pi \quad (A)$$

when e_{SW} is proportional to V_{CE} (A)

$$E_{SW} = e_{SW}(U_A \cdot \sqrt{2}, I_{AV}) / 2$$

when e_{SW} is proportional to V_{CE}^2

3.2 Calculation of conduction losses of the IGBT

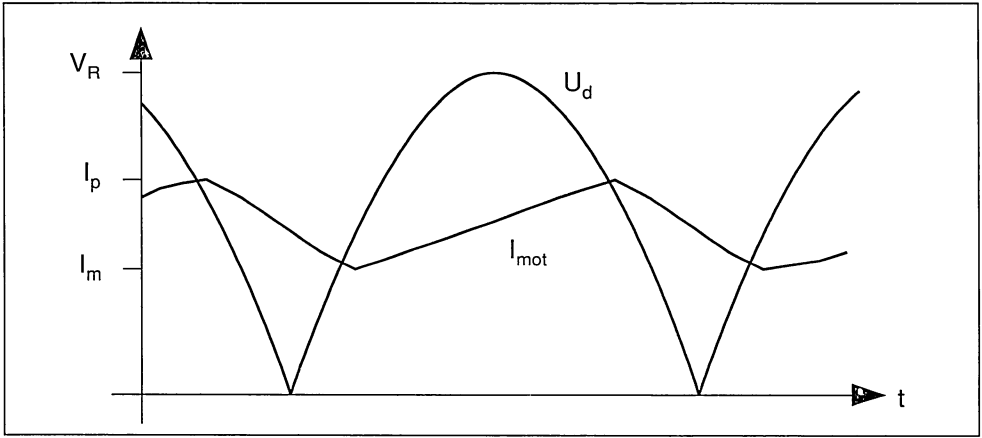
Conduction losses energy of all switching cycles on one half cycle are added :

$$E_{ON} = \sum_j (e_{ON})$$

$$= T_{SW} \cdot [E_O \cdot \delta \cdot \sum_j I_{CP}(j) + R_T \cdot \delta \cdot \sum_j I_{CP}(j)^2]$$

$$E_{ON} = T \cdot \delta \cdot [E_O \cdot I_{AV} + R_T \cdot I_{RMS}^2]$$

Figure 5. Waveforms of applied mains voltage U_d and the motor current I_{mot} (worst case) in a washing machine application



because $n \geq 50$ and $\sum_j I_{CP}(j) \cdot T_{SW} \approx I_{AV} \cdot T$

$$\sum_j I_{CP}(j)^2 \cdot T_{SW} \approx I_{RMS}^2 \cdot T$$

The conduction losses in one half mains cycle are:

$$P_{ON} = \delta \cdot [E_O \cdot I_{AV} + R_T \cdot I_{RMS}^2] \quad (B)$$

3.3 Calculation of the switching losses of the IGBT

The switching losses are evaluated as shown with formula (A) :

$$E_{ton} \approx 1.1 \cdot T \cdot f_{SW} \cdot U_A \cdot \sqrt{2} \cdot (I_{AV} + I_{RM})^2 / (\pi \cdot dl_C/dt)$$

$$E_{toff} \approx T \cdot 2 \cdot f_{SW} \cdot e_{toff}(U_A \cdot \sqrt{2}, I_{AV}) / \pi$$

$$P_{SW} \approx (E_{ton} + E_{toff}) / T \quad (C)$$

3.4 Calculation of the diode conduction losses

The dissipation in conduction can be calculated in the same way as with the IGBT :

$$P_{ON} = (1 - \delta) \cdot [V_{Io} \cdot I_{AV} + R_d \cdot I_{RMS}^2] \quad (D)$$

3.5 Calculation of the diode switching losses

dl_C/dt is assumed to be constant, and therefore the diode parameters S and I_{RM} become independent of V_R :

$$P_{SW} \approx E_{toff} / T$$

$$P_{SW} \approx U_A \cdot \sqrt{2} \cdot f_{SW} \cdot S \cdot I_{RM}^2 / (3 \cdot \pi \cdot dl_C/dt) \quad (E)$$

The result is overrated because dl_C/dt depends on U_A and S depends on I_{mot} , but these are much lower than other chopper losses .

4. THERMAL RATING

For a reasonable safety margin, the aim should be to limit the operating junction temperature of the diode and the IGBT to around 125°C.

Generally the diode and the IGBT are considered to be far enough apart on the heat sink for their cooling to be independent of each other. The thermal resistances of the IGBT and the rectifier are calculated separately. The whole heat sink is the result of paralleling the heatsinks required for the two devices.

For each power device thermal cooling is defined as:

$$(P_{SW} + P_{ON}) = (R_{TH} + R_{TH(CT)} + R_{TH(JC)}) \cdot (T_J - T_{AMB}) \quad (F)$$

The heat sink thermal resistance is calculated as:

$$R_{TH(HT)} = R_{TH(D)} \cdot R_{TH(T)} / (R_{TH(D)} + R_{TH(T)}) \quad (G)$$

When the devices are too close for this assumption to be made, mutual thermal impedances should be taken into account.

5. CONCLUSION

This note gives some pointers to the design of the cooling system of a chopper converter. The thermal calculation should be confirmed by practical tests to fully validate the cooling rating.

When the power of the system is less than 500W and the switching frequency is round 16kHz, the losses will be mainly generated by the turn off of the IGBT.

APPENDIX 1. TERMINOLOGY

- e_{ton} = turn on energy)
- e_{ON} = conduction energy) for the diode and
- e_{toff} = turn off energy) the IGBT
- e_{OFF} = OFF state energy)
- e_G = gate energy
- T_{JD} = junction temperature of the diode
- S = softness factor of the diode
- I_{RM} = reverse recovery of the diode
- V_{io} = on state threshold voltage of the diode (@
 T_{JMAX})
- R_d = dynamic on state resistance of the diode
(@ T_{JMAX})
- I_{FAV} = average forward diode current
- I_{FRMS} = r.m.s forward diode current
- di_e/dt = rate of removal of diode current at turn off
- V_R = reapplied diode voltage (direct voltage)
- δ' = diode duty cycle
- δ = transistor duty cycle
- T_{SW} = switching period
- f_{SW} = switching frequency
- I_{CRMS} = R.M.S. collector current)
- I_{CAV} = average collector current) of the IGBT
- I_{CP} = peak collector current)
- di_c/dt = turn on rate of rise of collector current of
the IGBT
- V_{CE} = turn off reapplied voltage of the transistor
- T_{JT} = junction temperature of the transistor
- E_o = on state threshold voltage of the IGBT (@
 T_{JMAX})
- R_T = dynamic resistance of the IGBT (@ $T_{J(MAX)}$)
- I_T = tail current of the IGBT
- t_T = tail current duration
- U_A = mains voltage
- I_{RMS} = R.M.S. motor current
- I_{AV} = average motor current
- I_p = peak motor current
- T = half period of the mains (10 ms)
- P_{ON} = total conduction losses power) for
- P_{SW} = total switching losses power) diode
- $R_{TH,X}$ = device heat sink thermal) (X=F)
resistance) or
- $R_{TH,JC}$ = junction case thermal) IGBT
resistance) (X=T)
- P_T = total losses power)
- $R_{TH,HT}$ = total heat sink thermal resistance
- $R_{TH,CT}$ = case contact thermal resistance

APPENDIX 2. CALCULATION OF THE AVERAGE AND RMS VALUES OF COMMON WAVEFORMS

Sine wave: $I_{AV} = \frac{2 \cdot I_p \cdot \delta}{\pi}$

$$I_{RMS} = I_p \cdot \sqrt{\frac{\delta}{2}}$$

Square wave: $I_{AV} = I_p \cdot \delta$

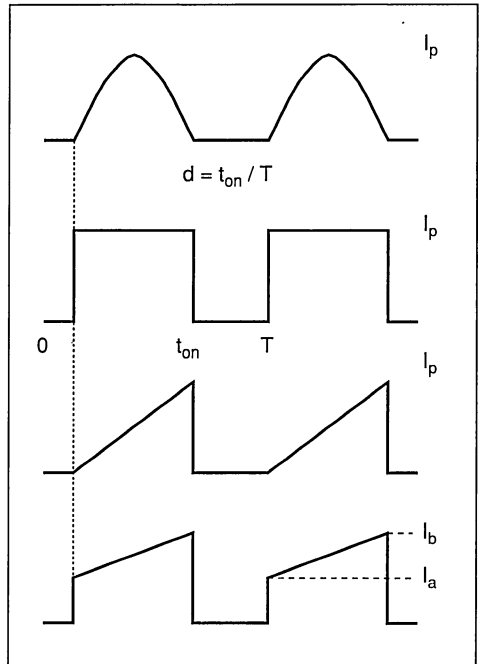
$$I_{RMS} = I_p \cdot \sqrt{\delta}$$

Triangular wave: $I_{AV} = \frac{I_p \cdot \delta}{2}$

$$I_{RMS} = I_p \cdot \sqrt{\frac{\delta}{3}}$$

Trapezoid: $I_{AV} = \delta \cdot \frac{I_a + I_b}{2}$

$$I_{RMS} = \sqrt{\delta \cdot \frac{I_a^2 + I_a \cdot I_b + I_b^2}{3}}$$



**THERMAL MANAGEMENT
and PCB LAYOUT**

ENVIRONMENT DESIGN RULES OF MOSFET IN MEDIUM POWER APPLICATION

by B. Maurice

ABSTRACT

The use of POWER MOSFET allows high switching speed in power applications above 10kW. Nevertheless the main limitations come from the characteristics of the circuit design. From a practical example, this paper analyses and proposes solutions to adapt the POWER MOSFET and the layout in order to minimize parasitic inductances. Special emphasis is given to the driver circuit, package, wiring rules and voltage spike protection at turn-off.

I - INTRODUCTION

POWER MOSFETs are now considered standard tools by circuit designers working at tens of Amps and hundreds of Volts. Their traditional advantages (easy drive and over current capability) remain true when switching over 10KWatts. Nevertheless, the main limitations encountered are not from the MOSFET itself as it can switch high current at high speed (over 1000Amps/sec), but from characteristics of the circuit design. After presentation of a specific example of Power MOS drive, the optimisation of the power devices and the layout will be analysed in the practical example of a chopper operating with ISOFET (1000V - 0.7 Ω or 100V - 0.009 Ω). Finally,

an over-voltage protection circuit is presented.

II - HIGH POWER MOS DRIVE

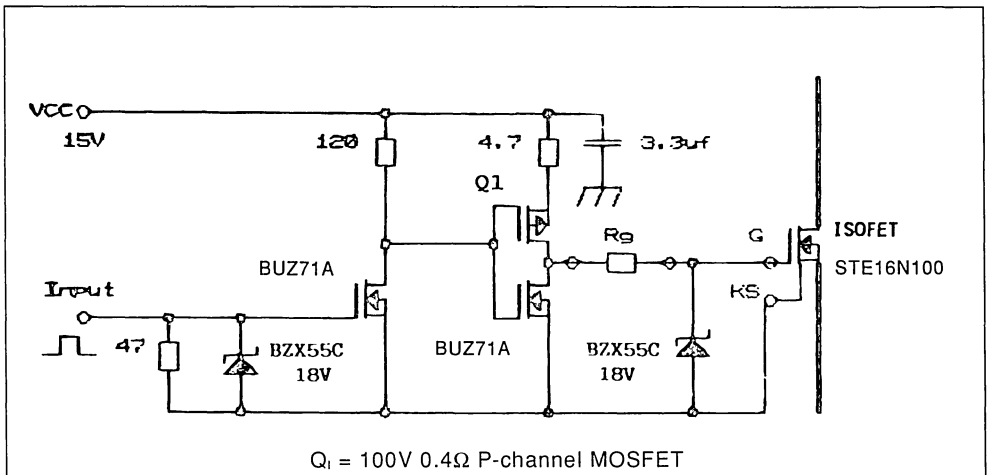
Even with high power switching (over 10KW), the driver circuit can be very simple (fig. 1), comparable to the ones used for low power circuits.

The major characteristics of a POWER MOSFET is its high input capacitance (ie : $C_{ISS} \approx 13nF$ for 100V - 9m Ω MOSFET) which must be rapidly charged and discharged when switching without creating oscillations.

The following rules have been used for the design of the driver :

- A low dynamic internal impedance which permits peak current greater than 1Amp for 300nanosec to charge and discharge the ISOFET input capacitance.
- A low impedance circuit reduces the sensitivity to dV_{DS}/dt at turn-off of the ISOFET.
- The total resistance of the gate circuit must be greater than 5 Ω in order to sufficiently damp the circuit preventing oscillations and possible parasitic turn-on of the ISOFET.

Figure 1 : Driving Circuit for ISOFET Over 10kW Switching.



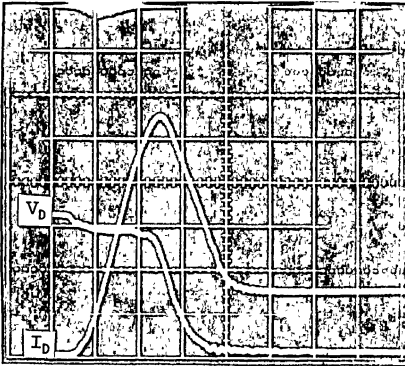
- The links between drive and gate, short and non-inductive, are made between the gate pin and the "Kelvin Source" pin. The use of the "Kelvin Source" pin is very important when driving Power MOS. It

avoids parasitic effects caused by di/dt in the source lead.

- The gate protection Zener diode has to be mounted close to the ISOFET package.

Figure 2 : Over Current Capability and Switching Speed with ISOFET STE16N100 (1000V – 0.7Ω – $I_D = 16A$)

- Turn-on ; the ISOFET controls 30A-650V and sustains 110A peak ($8 \times I_D$). The over current is due to the recovery of the free-wheeling diode (BYT230PIV 1000).
- Turn-off ; with $di/dt = 1600A/usec$; and $dV/dt = 15000V/usec$.
The switched power = 25kW ; and the switching losses = 1.3mj



a. Turn-on

$V_D = 200V/div$

$I_D = 20A/div$

$t = 50ns/div.$

$R_g = 5\Omega$



b. Turn-off

$V_D = 100V/div$

$I_D = 10A/div$

III - LAYOUT DESIGN FOR HIGH SPEED SWITCHING

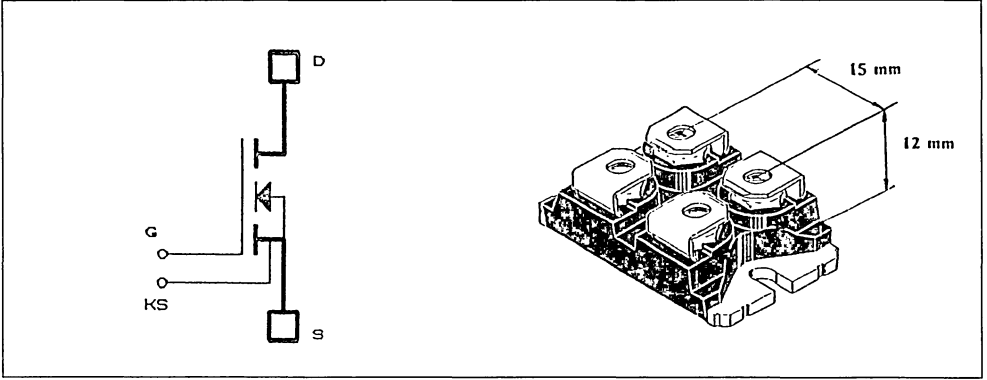
The reduction of the parasitic inductances is a major challenge for power switching especially with a power MOSFET switching over 1000Amps/usec (figure 2). With this switching leading edge, a 10cm diameter wiring loop causes a 100V voltage overshoot. To solve this potential problems two actions are necessary : choosing a well adapted device and optimise the layout design.

- Adapting the device to the layout

ISOFET is a MOSFET housed in an ISOTOP package (figure 3) :

- The ISOTOP package can be directly screwed on the printboard because all of its terminals are at the same level. Therefore, all inductances due to the length of external wiring connexions, are eliminated.
- As a result of a low profile package (12mm), the internal parasitic inductance is less than 10nH. Moreover, its Kelvin source (KS) enables the minimisation of disturbances induced by the power circuit in the driver circuit.
- Even though it has a thermal resistance value of only $0.25^\circ C/W$, the case is fully internally insulated at $2.5kV_{RMS}$. Therefore it can be mounted near to the diode package on a common heatsink in order to obtain a very compact circuit layout.

Figure 3 : An ISOFET is a MOSFET housed in an ISOTOP package, which has a low profile. It is easily integrated in low inductive layouts. The "Kelvin Source" lead (KS) separates the gate circuit from the internal inductance of the source connection.



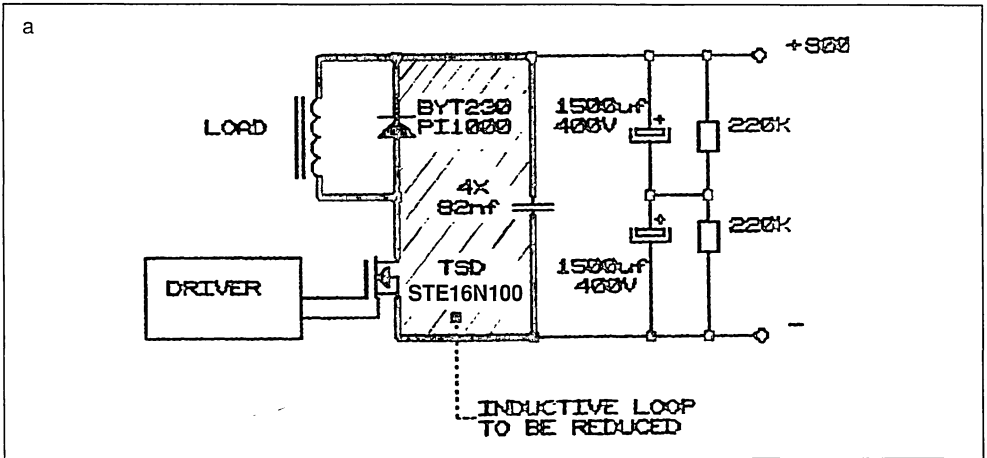
b. Design of the layout

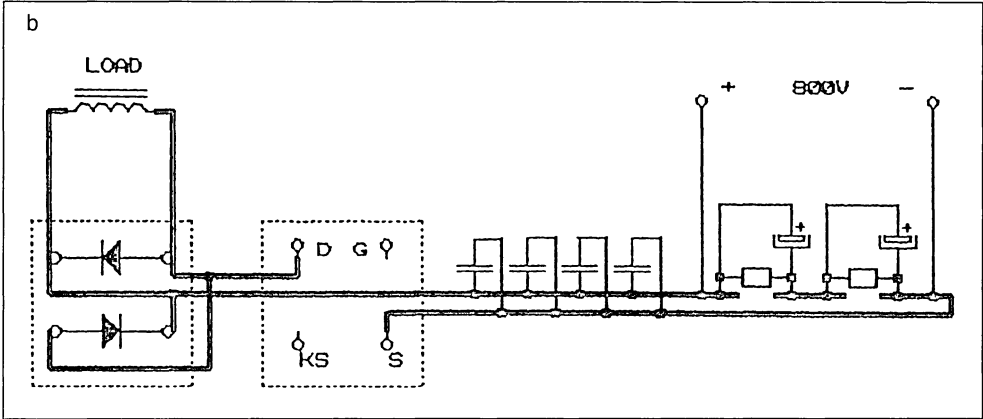
The chopper shown in figure 4 contains two active components : the Power MOS and the freewheel-

ing diode ; both in ISOTOP package screwed side by side, on a common heatsink and directly connected on the printed circuit board (PCB).

Figure 4 : a. Chopper Schematic showing the Inductive Loop to be Reduced.

b. The Same Circuit with two ISOTOP Packages (diode and ISOFET). The packages and links adopt an "in line" configuration in order to reduce the inductive loop.





By observation of the facts presented in appendix 1, the design rules used for the layout are summarized :

- Use of double sided PCB where each high current path is immediately above its returns path on the other side of the board.
- The current density has been reduced by enlarging the copper tracks in order to decrease the local dI/dt and consequently the resulting induced voltage.
- Use of several links instead of one, between two large copper tracks, avoids high current concentrations and reduces the inductance (figure 5).

- Decoupling capacitors have been configured in the same direction as the direction of current flow. This prevents the formation of an inductive loop. (compare figure 6a and figure 6b hatched surfaces).
- The use of several smaller capacitors in parallel permits reduction of the equivalent internal parasitic inductance. (figure 6c).
- Choose components (e.g. capacitors) specified with a low internal inductance. (electrolytical capacitor $700\mu F/400V$ can have a parasitic inductance of several tens of nH). Prefer the capacitor packages which minimize the inductive connection length.

Figure 5 : Junction between two wide copper tracks is less inductive when several spaced links are used rather than a single link.

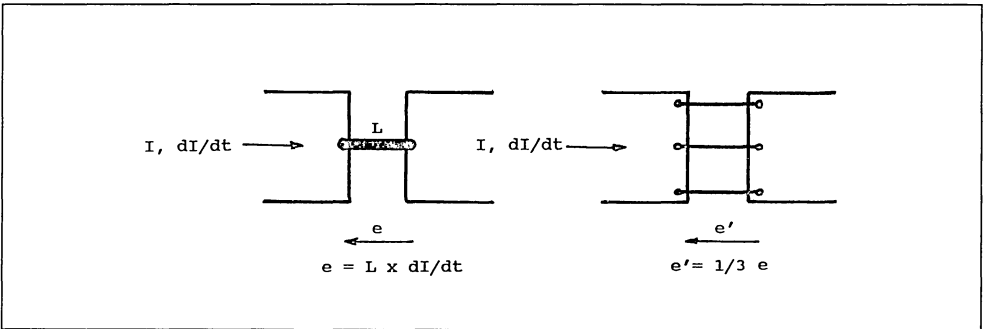
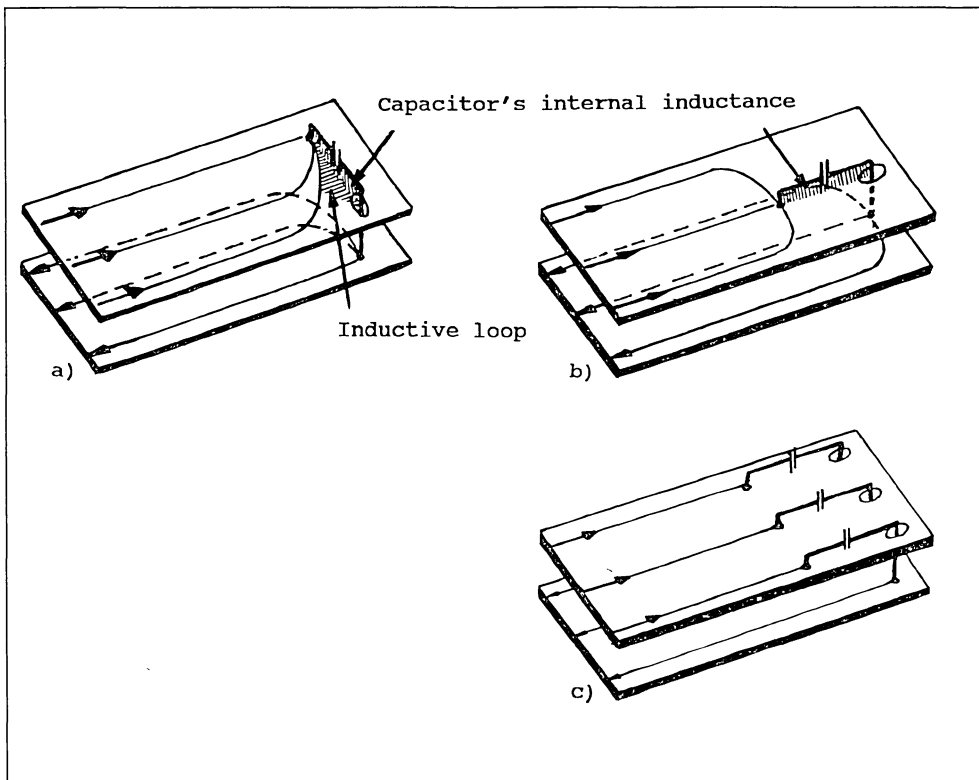


Figure 6 : Configuration of Decoupling Capacitors :

- An inductive loop is formed, perpendicular to the current flow, because the current flow is not super imposed near the capacitor,
- Capacitor lying in the same direction as the direction of current flow. inductive loop minimised.
- Several smaller capacitors in parallel reduce their equivalent internal parasitic inductance for the optimum solution.

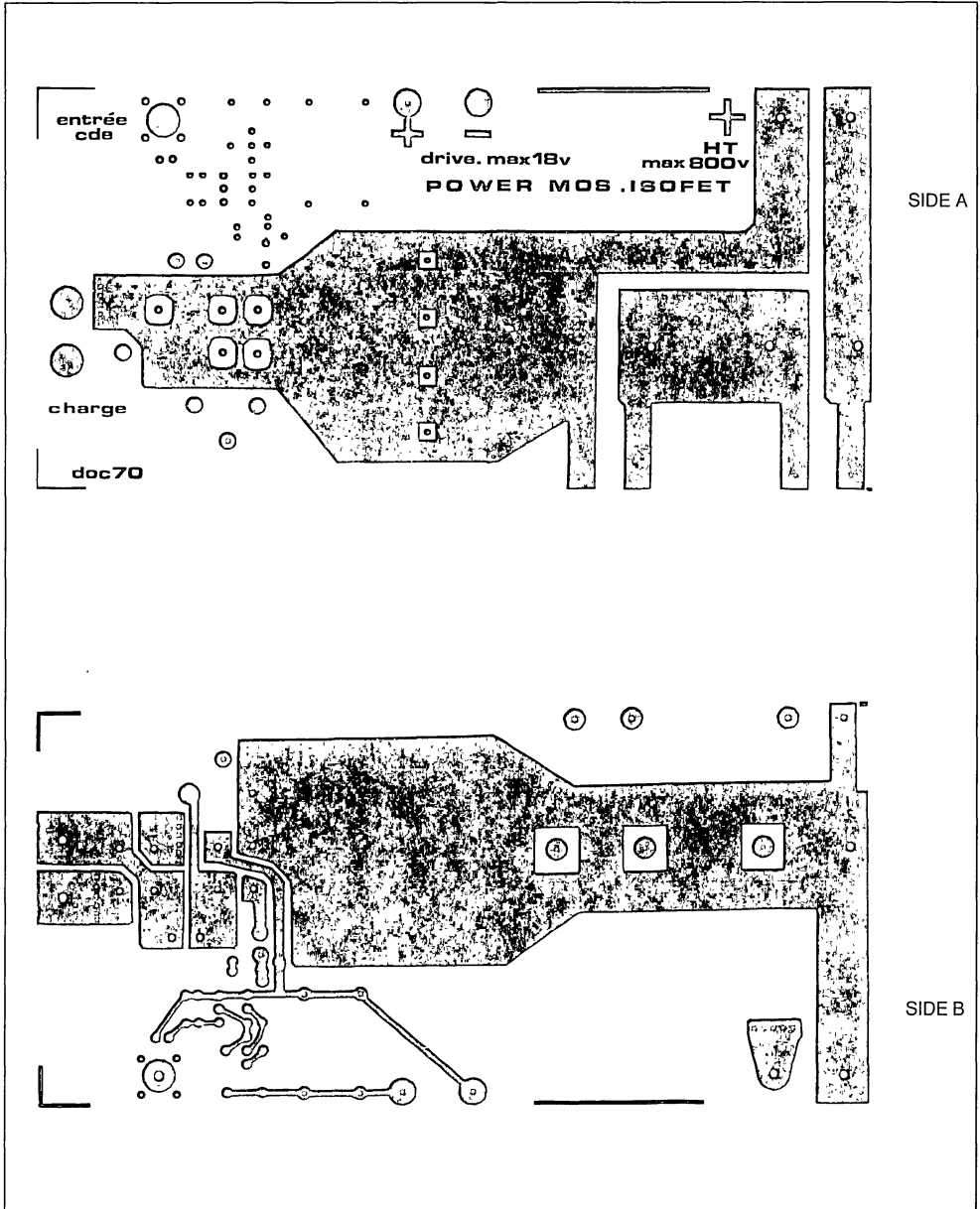


APPLICATION NOTE

As a result the residual inductance of the finished layout (fig. 7) has been measured as 35nH, (fig. 8)

plus 15nH when a current sensing loop (15mm²) is added to the layout.

Figure 7 : A Double Side Very Low Inductive Print Circuit Board. (scale : 0.5)
Note the Multi Links (A) to connect One Side to the Other.



IV - OVERVOLTAGE DURING TURN OFF

We have previously seen that by following these sound rules a parasitic inductance value of 35nH can be achieved. It represents the sum of several small components : active components, passive components and PCB. It seems difficult to reduce it further in a circuit without paralleling several power switches.

In view of the ISOFET fast switching speed at turn-off (1000Amp/usec), the inductive voltage spike with 35nH will be 35 Volts. This overvoltage is accept-

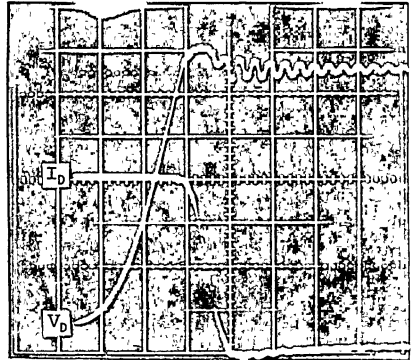
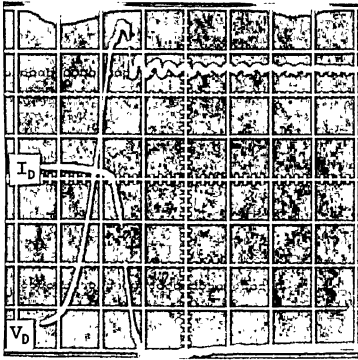
able for devices rated over 500V. It is not negligible in low voltage applications such as battery powered equipment.

Two solutions are possible :

a. Slowing down the ISOFET

The switching speed at turn-off can be slowed down by increasing the gate resistor value. This method increases the commutating time and consequently the switching losses. These losses are increased by 50% when R_g increases from 5 to 10 Ω . (figure 8).

Figure 8 : Increased Gate Resistor reduce dI/dt and Overvoltage at Turn-off. (driver circuit fig. 1). The total parasitic inductive loop (50nH) includes the inductance of the sense current loop.
 $I_D = 10A/div$ $V_D = 100V/div$ $t = 50ns/div$ (ISOFET STE16N100 1000V - 0.7 Ω)
 Switched power = 25kW; Switching losses = 1.3mJ in (a) and 2.0mJ in (b).



b. Protection against over-voltage at turn-off

Use of a MOSFET with a low margin for the rating voltage ($V_{BR(DSS)}$) can be achieved by using active protection (i.e. Transil) in order to clamp the voltage spikes.

One solution is to connect a Transil across the drain-source leads. In this case, the energy is dissipated in the Transil which has to be cooled in order to dissipate the average power.

$$(1/2) L I^2 f = 20W \text{ with } 40nH, 100A, 100kHz$$

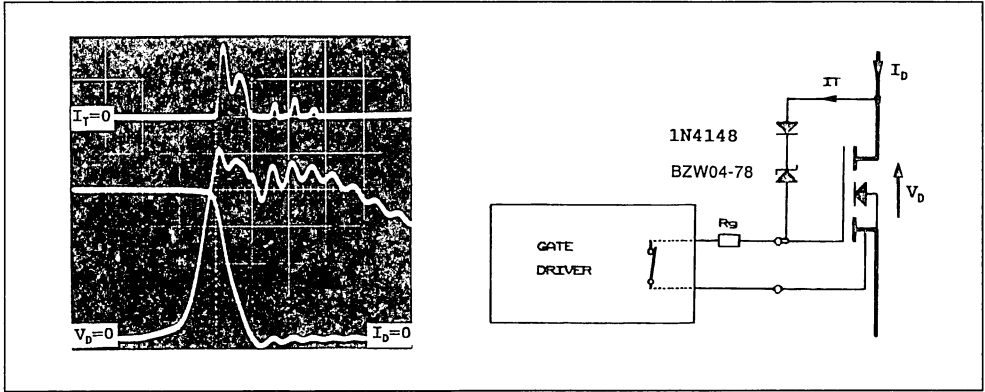
We have chosen another solution by connecting the Transil across the drain-gate leads (figure 9). When the over voltage transient reaches the clamping voltage, the clamping current goes through the gate resistance and biases gate above 5V. (ex : 1A into 5 Ω).

This way, the clamping power is dissipated in the MOSFET and a smaller Transil is required ($P \approx 1W$ at 100kHz in our case).

As the Transil does not heat up, the clamping voltage does not vary with temperature. The equivalent dynamic resistance is very low because the serial resistance of the Transil is divided by R_g and by the MOSFET transconductance.

The current though the Transil being low, the voltage to be considered for its choice is the breakdown voltage at test level (V_{BR} at I_R) instead of the surge clamping voltage (V_{CL}). The Transil breakdown voltage should be chosen to be lower than the maximum desired clamping voltage less 5 Volts to take into account the MOSFET gate threshold voltage.

Figure 9 : Over Voltage clamping by a Transil across the Drain-gate Leads durring turn-off. (ISOFET STE150N10 100V – 9mΩ). Upper Trace shows the Current in the Transil (IT).
 $I_D = 20A/div$, $V_D = 20V/div$, $I_T = 1A/div$, $t = 100ns/div$.



V - CONCLUSION

MOSFETs switching power over 10kW have the same basic advantages as lower power Mosfet. The driving circuit remains very simple and the over current capability is huge. A specific emphasis has been placed on the minimization of circuit layout inductance. Because of the very fast switching (easily over 1000A/s) it is advantageous to use :

- packages like ISOFET which minimise their internal inductance and allow easy connection to printed circuit board and to heatsink. Also Kelvin Source contact to minimise drive circuit interference.
- double side printed circuit board with symmetrical

copper tracks, reduced current concentration, and components positioned in order to minimise parasitic inductance.

- overvoltage protection which avoids oversizing the voltage rating of MOSFETs in low voltage applications.

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- [2] POWER MOS DEVICES Data Book 1st edition June 1988 SGS-THOMSON Microelectronics.

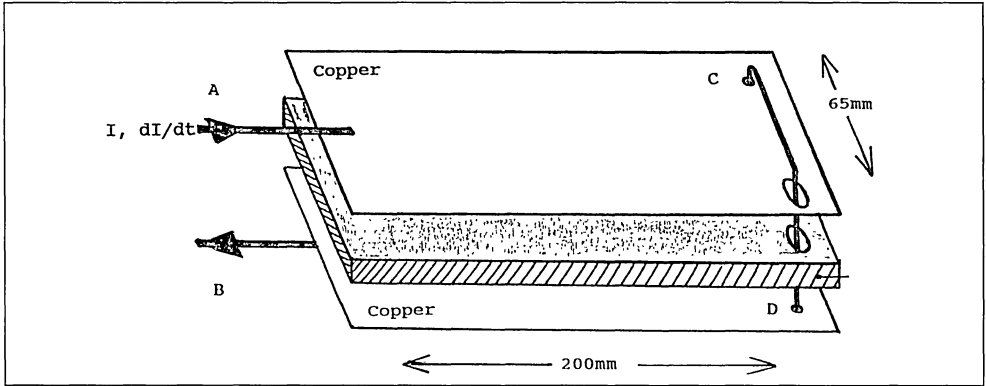
APPENDIX 1

MEASUREMENT OF PARASITIC INDUCTANCES ON A DOUBLE SIDED PCB

- In the figure below, the link between points C and

D simulates the connection of a capacitor with no internal inductance, connected on double sided Printed Circuit Board.

Figure 10.

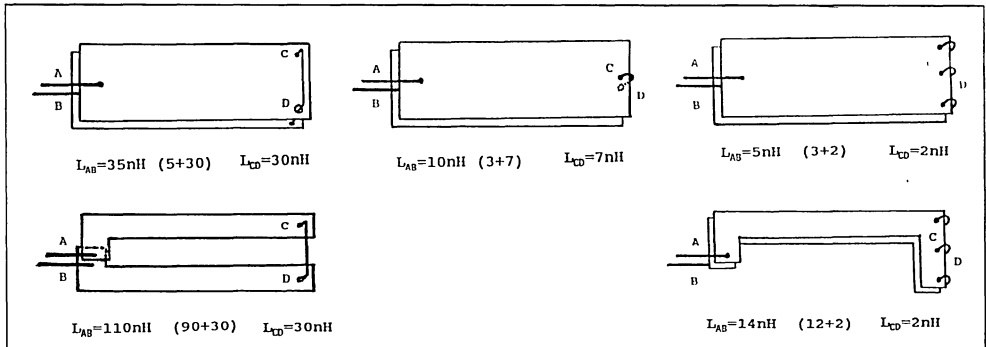


- The measurements are made with a dI/dt generator :
 - $I = 0$ to 40Amps , with a $dI/dt = 1000\text{A.s}$

The measurement of the induction voltage V_L between A to B, and C to D, permits calculation of $L = V_L / (dI/dt)$

MEASUREMENT RESULTS

Figure 11.



MEASUREMENT CONCLUSIONS

- Capacitors should be positioned in the same direction as direction of current flow. Compare : a. to b.
- Several links between two large copper tracks are less inductive than a single link. Compare : b. to c.

- Every current path should be exactly above its return path on the other side of the board. Compare : d. to e.
- Decrease local dI/dt density by enlarging copper tracks. Compare : c. to e.

PLASTIC PACKAGES FOR POWER DISCRETES AND ICs

by C. Cognetti

1. BRIEF OVERVIEW OF TECHNOLOGY

The plastic package of a power chip serves four main functions:

- i) Electrical interconnection between the silicon chip and the external circuit;
- ii) Protection from chemically aggressive agents, for long term reliability;
- iii) Mechanical support to the chip die, to make handling easier;
- iv) A thermally conductive path to transfer the heat generated in operation from the silicon to the ambient or to a heatsink.

The most characteristic feature of power packages is the massive heat conductive slug (usually copper) integrated into the package body, in close contact with the silicon die.

The metal “chassis” of the device, consisting of the copper slug and the package leads, is known as the leadframe. The leadframes for a number of individual devices (usually around 5 to 20) are manufactured in a single continuous strip, to simplify handling and processing (figure 1a).

After the silicon wafer is cut into individual dice, the die are brazed onto the metal slug using a high melting temperature ($> 280^{\circ}\text{C}$) tin solder alloy such as PbSn, PbSnAg, or SnAgSb. The process used to attach the die to the slug is critical to maintain the thermal performance of power device; it must produce a uniform, void free joint

between the silicon back metallization (TiNiAu or equivalent) and the copper slug, in order to avoid hot spots in the active area, which can cause failures in the short term due to second breakdown of the transistor, and in the long term through thermal fatigue.

After die attach, the silicon is connected to the lead frame with aluminium or gold wires, which are ultrasonically bonded to both the aluminium metallization on the chip and to a nickel (or silver) layer on the lead frame (figure 1b). The diameter of the wire used is chosen according to the current to be handled, using the approximated rule of about 1 mil/Amp (1 mil = $\frac{1}{1000}$ inch = $25\mu\text{m}$).

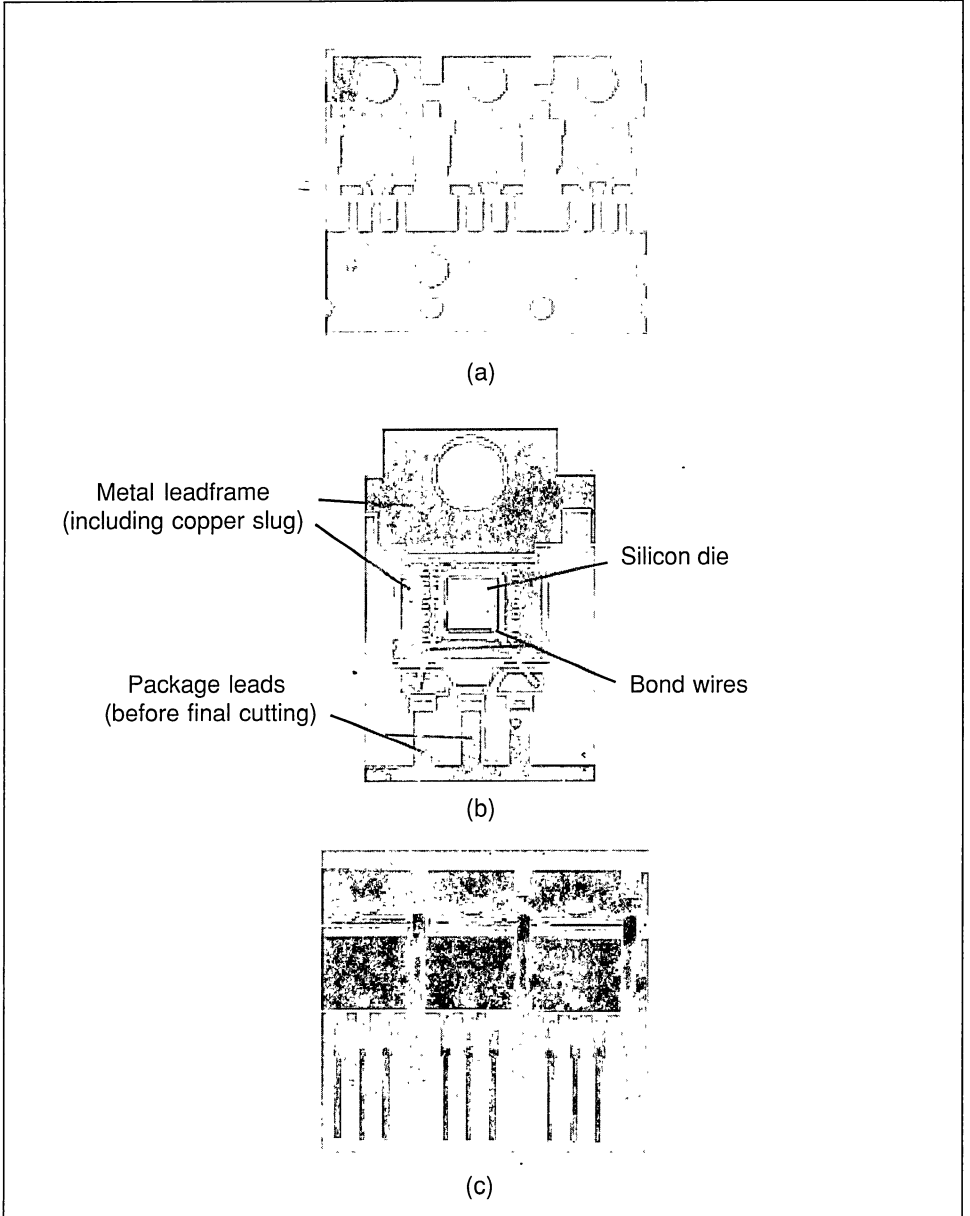
Molding is the third step of assembly (figure 1c); the leadframe strips are positioned in molding cavities which are then pressure filled with liquid thermosetting epoxy which, after solidification, provides a hard, reliable and cost effective encapsulation.

The last major process is to coat the leads with a low melting temperature thin solder alloy, to provide a “wetable” surface when the device is soldered to the printed board.

After singulation (separation of the leadframe strips into individual devices) and lead forming (bending of the leads into the required shape), devices are marked and tested before being packed and shipped.

Figure 1: Stages in the packaging process (the package shown is a TO-220)

- a) Part of a strip of leadframes
- b) Package prior to molding (enlarged)
- c) Completed packages before singulation



2 POWER PACKAGE TYPES

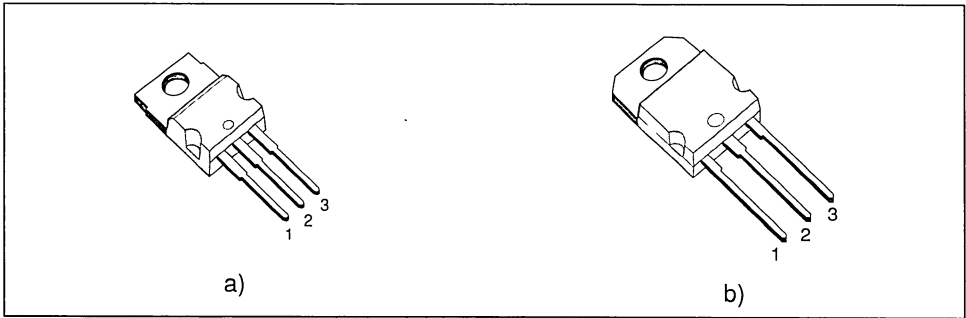
The main types of packages available are:

- 1] Single chip insertion package
- 2] Isolated single chip insertion package
- 3] Surface mount package
- 4] Multichip power module

2.1) Single chip insertion package

This family includes the two most widely used types of power package: the TO-220 and the SOT-93 (also known as TO-218). These packages are shown in figure 2.

**Figure 2: Single chip insertion packages: a) TO-220
b) SOT-93 (TO-218)**



The main difference between these two packages is their size, and hence the size of die which they can accommodate. This also defines the maximum operating current and power dissipation capability. Their characteristics are summarized in table 1 (see section 3 for an explanation of θ_{jc} , the thermal resistance).

These packages are inserted in through-hole technology (THT) boards and secured to the external heatsink using screws through the fixing holes, which are in the upper portion of the slug. In recent years substitution of screws with clips has become increasingly common for cost reasons.

Table 1: Characteristics of TO-220 and TO-218

	Maximum die size (mm ²)	Maximum current (A)	Minimum θ_{jc} (°C/W)
TO-220	25.5	60	1.0
TO-218	54	80	0.7

APPLICATION NOTE

Other single chip packages include the medium power SOT-32 and SOT-82, the TO-251 (also known as IPAK), and the high power TO-247. (See figure 3).

Some power devices, for example intelligent power devices, require more than 3 leads.

To accommodate this, a number of packages derived from the basic TO-220 configuration have been developed. The Pentawatt (5 leads), Heptawatt (7 leads) and the double size Multiwatt (11 and 15 leads) packages are shown in figure 4.

Figure 3: Single chip insertion packages: a) SOT-32 c) TO-251 (IPAK)
b) SOT-82 d) TO-247

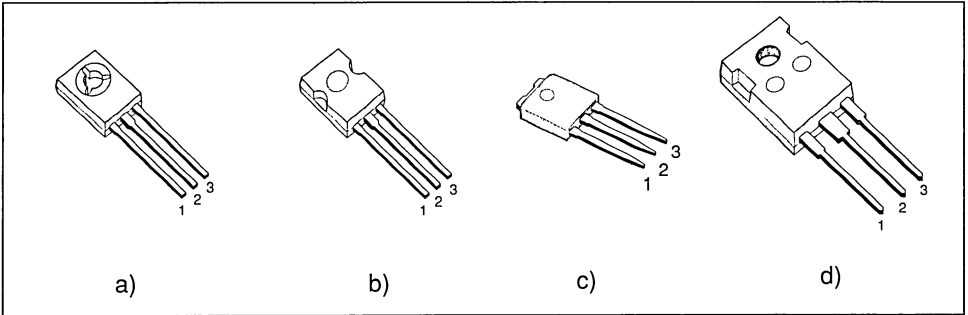
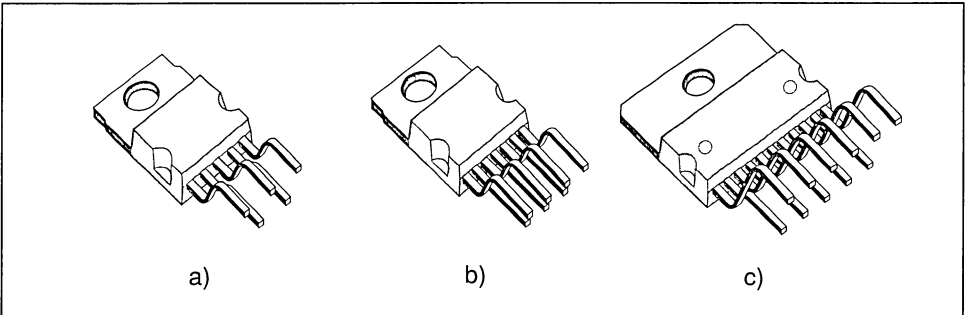


Figure 4: Multiple pin single chip insertion packages: a) Pentawatt
b) Heptawatt
c) Multiwatt (11 lead version)



2.2 Isolated single chip insertion package

In many applications a number of devices are attached to a single heatsink. Because the package slug is connected to the collector for a bipolar device or the drain in

the case of a MOS transistor, each individual package must be isolated from the heatsink. This can be achieved by placing a thin sheet of mica or adhesive mylar between the slug and heatsink.

Drawbacks of this solution are:

- a) The operation must be performed manually and so is very expensive, especially in high labour cost areas such as Europe and the USA.
- b) The thermal performance is inconsistent, due to variations in thickness, position, and adhesion of the isolating sheet. This inconsistency is unacceptable in many applications.
- c) The isolation achieved by the washer can be unreliable in some situations; the fixing screw can easily be overtightened, causing cracking of the washer.

An innovative solution to this problem was the development of new package structures, which surround the copper slug with a thin layer of epoxy. This layer is obtained by maintaining a set distance between the slug and the mold cavity during the molding process. The epoxy behaves as a thermal conductor but an electrical isolator.

This solution is very competitive with conventional ones, particularly if high thermal conductivity molding compounds are used - see table 2.

Table 2: Comparison of isolation methods

PACKAGE	ISOLATION	θ_{j-c} (°C/W)
TO-220	none	1.3
TO-220	100mm mica	3.3
TO-220	mylar	4.4
ISOWATT220	none	3.0
ISOWATT221	none	3.8
ISOWATT218	none	2.1

The flatness of the mounting surface achieved with the epoxy layer is also much better than that practicably achievable for a metal contact surface, which helps to compensate for the inferior thermal conductivity.

Isolated versions of the TO-220 and SOT-93 are called the ISOWATT220 and ISOWATT218 respectively, while the

ISOWATT221 is a version of the ISOWATT220 adapted to withstand higher voltages, and able to meet the creepage and clearance requirements of UL, VDE and EN specifications - see figure 5.

Table 3 summarizes the most important isolation characteristics of ISOWATT packages.

Figure 5: Isolated single chip insertion packages: a) ISOWATT220
 b) ISOWATT218
 c) ISOWATT221

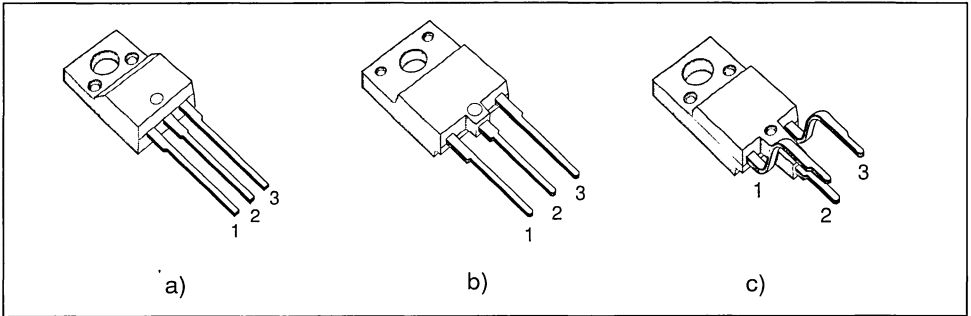


Table 3: Isolation characteristics of ISOWATT packages

	ISOWATT220	ISOWATT218	ISOWATT221
V_{RMS} @ 150°C	1500V	2500V	2500V
DC isolation	2000V	4000V	4000V
Specifications	UL	UL, VDE, CEN	UL, VDE, CEN

2.3 Surface mount power packages

Surface mount technology (SMT) was introduced in the early 80s as an alternative to insertion technology. The fundamental difference is that the components are soldered onto the surface of the board rather than being inserted through holes.

Among other things this technology removes the limit placed on the lead pitch of the packages, which is constrained by the minimum distance between holes which can be drilled through the board - in most cases this is 2.54mm (100 mils).

Using surface mount technology, the lead

pitch can be reduced to a few tenths of a millimetre, and substantial miniaturization at package and system level is achieved.

This allows systems to be produced with the same performance in a smaller space, at a lower cost, which has particular importance in portable systems and consumer electronics, but also has advantages in industrial and automotive power applications.

The use of SMT also leads to easier handling due to the smaller dimensions of the packages, which can be placed automatically onto the board using cost effective machines fed from carriers and tapes.

The advantages of surface mount are best exploited if all the components of the circuit can be mounted on a single board. This is the reason for the increasing interest in power SM packages. These started to appear very recently, in the form of modified versions of existing packages (for example the TO-263 from the TO-220, the SOT-194 from the SOT-82 and the TO-252 from the TO-251) and purpose designed packages, such as the PowerSO-10 and the PowerSO-20 - see figure 6.

The PowerSO packages meet the requirements of SMT, including miniaturization, while maintaining the thermal characteristics required by power applications, both in steady state and pulsed conditions as shown in table 4.

In applications using laminate boards or power substrates, the maximum possible dissipation increases from 2 W to 20-30 W per device, covering the same range of insertion packages.

Figure 6: Surface Mount power packages: a) SOT-194 c) PowerSO-10 e) TO-263 (D2PAK)
 b) TO-252 (DPAK) d) Power SO-20

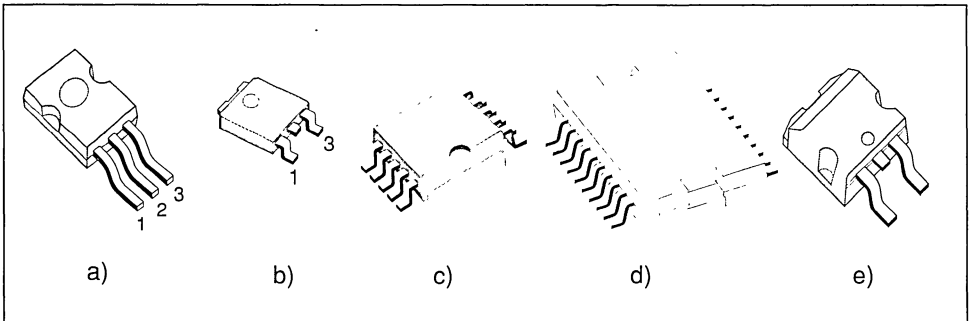


Table 4: Comparison of the PowerSO-10 and the TO-263

	TO-220 (SMD version)	PowerSO-10	Diff.
Footprint area in mm ²	203	141	-30%
Heat spreader in mm ²	50 to 60 †	67	10~30%
θ_{j-c} in °C/W	0.8	0.8	equal
Chip size in mils	180x220	180x220	equal
Total volume in mm ³	597	373	-37%
Package height in mm	4.5	3.5	-22%

† Area varies depending on manufacturer

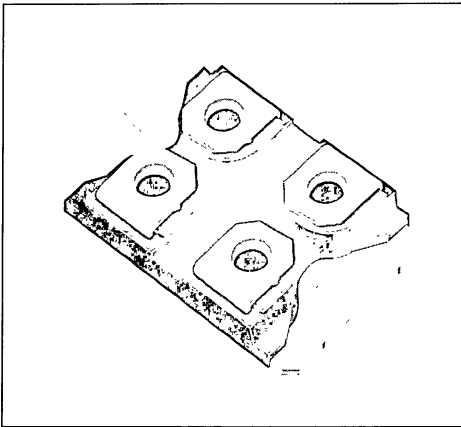
2.4 - Multichip power module

High power applications, with up to 600W of dissipation and currents of up to 300A require multiple chips connected in parallel, and large heatsinks. This can be conveniently achieved by mounting a number of die together in a single package with hard-wired connections between them.

A typical example of a multichip power module is the ISOTOP® package, shown in figure 8. This can house several diode or power transistor die, which are brazed onto an isolating alumina layer, which is in turn soldered onto a copper heat dissipation mass.

The isolation between the dice and the copper mass is 2500V_{RMS} (4000V DC). The package has a low parasitic inductance (5pH) and capacitance (< 100pF).

Figure 7: The ISOTOP package



3. THERMAL MANAGEMENT

3.1 Thermal resistance

Thermal resistance is the physical quantity which indicates how “easily” the heat flows between two points A and B. If thermal resistance is small, heat is transferred from

A to B with little temperature difference between A and B. If thermal resistance is large, the transfer of the same quantity of heat from A to B requires a much higher temperature difference in the two points.

The thermal resistance is in some ways an allegory of electrical resistance. Ohm’s law defines the electrical resistance as:

$$R = \frac{V}{I}$$

where I is the current, or rate of flow of charge between the two points, and V is the voltage difference between two points, which represents the “motive force” - the larger the voltage for the same resistance, the higher the resulting current.

Instead the thermal resistance is defined as:

$$\theta = \frac{\Delta T}{P}$$

(Note - θ is often written as R_{TH})

where P is the power, or the rate of flow of heat between the two points, which is the thermal equivalent of I, while ΔT is the temperature difference between the two points, which is again the motive force, and is the thermal equivalent of V.

In electronic devices, the two most important temperatures are the ambient temperature T_a and the temperature T_j reached by the junction when a given thermal power P_d is generated in the silicon.

Thermal resistance junction to ambient θ_{ja} is the ratio between junction temperature increase and heat flow :

$$[1] \quad \theta_{ja} = \frac{T_j - T_a}{P_d}$$

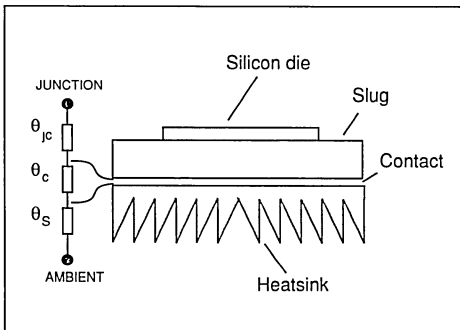
θ_{ja} depends upon a number of factors, including the size of the device, the thermal conductivity of the materials used in the construction of the device, and the size of the heatsink.

In electronic systems, the failure rate is affected by junction temperature; it doubles for every 10°C increase of T_j .

The main aim of thermal design is to keep the junction temperature within defined limits, which is usually lower than 150-170°C for discretes, and 125-150°C for ICs. At the same time, systems are increasingly being used in ambient temperatures of up to 125°C, for example in "under the hood" car electronic systems. In this case, $T_j - T_a$ can be as low as 20-25°C. This causes particular problems where large amounts of power (10-20W) are to be dissipated, where θ_{ja} may be limited to a few °C/Watt.

θ_{ja} is controlled by attaching a suitably sized heatsink to the power package slug. From a physical viewpoint, a thermal chain exists from the silicon to the ambient through the die attach, the slug, the interface between the slug and the external dissipator and finally the dissipator itself (see figure 8).

Figure 8: Thermal chain from silicon to ambient



This can be represented as follows:

$$[2] \quad \theta_{ja} = \theta_{jc} + \theta_c + \theta_s$$

where θ_{jc} is the thermal resistance from the silicon junction to the case, defined by the conduction properties of the device from the junction to the portion of the case where the heatsink is applied; θ_c is a parasitic element describing the loss at the point of

contact between the package and the heatsink; while θ_s is the thermal resistance of the external sink, which indicates the efficiency with which the heatsink dissipates heat through convection and radiation.

3.2 Thermal resistance and heat transfer mechanisms.

The flow of heat from the silicon to the ambient is ruled by three important mechanisms: conduction, convection and radiation.

3.2.1 Conduction and θ_{jc}

Conduction is the heat transfer mechanism due to thermal excitation at molecular level, by direct contact. No motion of material is associated to this mechanism. Thermal resistance depends on the thermal conductivity c of the material and its dimensions (length L and cross sectional area A) according to the relationship :

$$[3] \quad \theta = \frac{1}{c} \frac{L}{A}$$

Equation [2] can be applied to the J-C pattern as shown in figure 9.

In this simple model, the heat generated at the junction flows in a 45° cone through the silicon, the die attach alloy and the copper slug up to its external surface. Table 5 shows the thermal conductivity of some materials commonly used in microelectronics.

Figure 9: Junction-case heat dissipation pattern

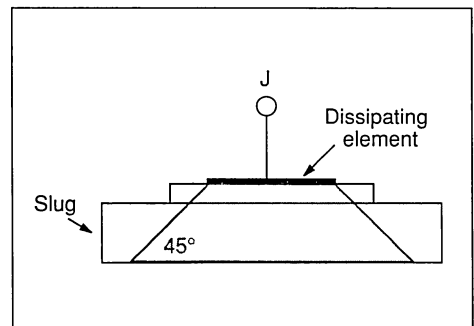


Table 5: Thermal conductivity of materials commonly used in packaging

MATERIAL	THERMAL CONDUCTIVITY (Wm ⁻¹ K ⁻¹)
Silicon	150
Glass (Silicon Oxide, SiO ₂)	0.6
Silicon Carbide (SiC)	85
Aluminium	210
Aluminium Nitride (AlN)	150
Aluminium Oxide (Al ₂ O ₃)	30
Resin (Standard packages)	0.71
Resin (Isolated packages)	2.51
Mica	0.5
Air	0.03

The following points should be noted:

a) θ_{jc} is mainly affected by the chip size and by the size of power element(s) in the chip. The theoretical relationship is given in figure 10.

b) The thermal conductivity of silicon increases with an increase of temperature, as shown in figure 11. In the temperature range considered in microelectronics a variation of 20-30% is common.

c) The dimensions of the slug are important. In principle, a thinner slug should provide a lower resistance (as there will be a shorter conducting path); in practice, due to the existence of parasitic effects at the contact with the external heatsink (uneven surface, air, dust, etc.) a thicker and larger slug performs better; indeed it can spread the heat much more than the 45° considered in figure 9 and reduce the losses at the contact because of the larger area of contact.

3.2.2 Convection, radiation and θ_{ja}

Convection

Convection is the transfer of heat associated with the movement of material in a fluid (liquid or gas). It is due to the heating and thus decreasing density of the fluid in contact

Figure 10: Variation of θ_{jc} with die size

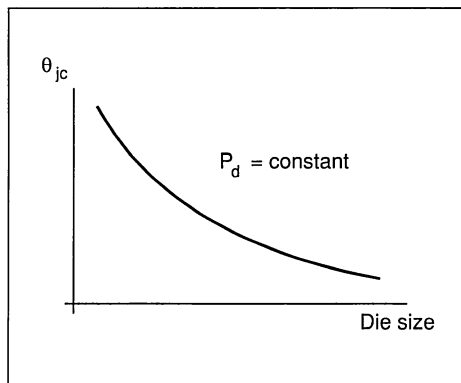
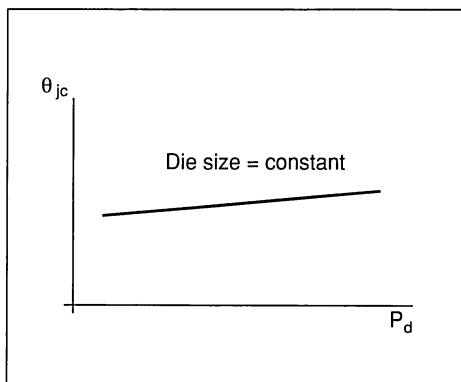


Figure 11: Variation of θ_{jc} with dissipated power



with the heat source, which movement upward and is replaced by cooler fluid. The process is ruled by the heat-transfer coefficient h depending on the source temperature T_s and the ambient temperature T_a .

The quantity of heat removed by convection is given by the relationship:

$$[4] \quad Q = h(T_s, T_a) \cdot A \cdot (T_s - T_a)$$

where A is the area of the heat exchange surface.

In case of forced cooling, h is a function of the speed of flow of the cooling fluid and is always higher than in equation [4]. The following considerations are important:

a) The size of the heatsink has the greatest effect on the final performance of the cooling systems. As the exchange surface dominates in equation [4], it is common to increase it with the use of fins and grooves. However, this solution is most effective in forced cooling.

b) The higher the source temperature, the stronger the convection effect. This can compensate for the negative effect of the temperature on the θ_{jc} considered in the previous paragraph, and the final result is a θ_{ja} which decreases with increasing power dissipation (figure 12).

c) The thickness of the heatsink is important, in order to spread the heat in the sink by conduction, and to have a larger exchange surface.

Radiation

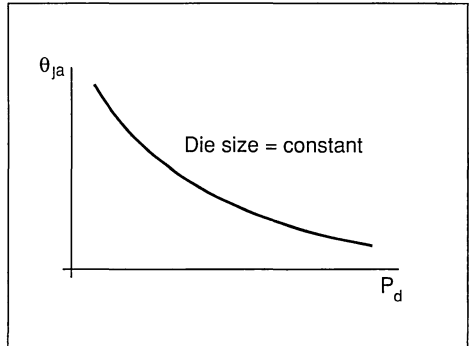
Transport of electromagnetic energy is associated with radiation, which involves a transmitting surface at temperature T_s and a receiving ambient at a temperature T_a .

The heat Q exchanged by radiation from a surface area S is :

$$[5] \quad Q = \sigma \cdot \alpha \cdot S \cdot (T_s^4 - T_a^4)$$

where σ is the Stefan-Boltzmann constant

Figure 12: Variation of θ_{jc} with P_d



and α is the emissivity of the material, which varies between 0 and 1.

Black surfaces have emissivity close to 1, indicating the maximum radiation energy theoretically possible at T_s . Polished, white metals (like aluminium) have the lowest emissivity, between 0.1 and 0.3.

Due to the 4th power relationship with the temperature, radiation dominates only when T_s is much larger than T_a (in absolute units). This is generally not the case for applications in electronics; however the effect of radiation cannot be ignored.

As an example of values associated with convection and radiation, if a 1mm x 10cm x 10cm red (natural oxide) copper sheet is used as a heatsink positioned vertically at a T_s of 100°C, the thermal resistances due to both radiation and convection are around 7°C/W, giving an overall value of 3.5°C/W.

3.3 Thermal Impedance

In section 3.2, thermal exchange was studied in steady state conditions, that is once the system had reached thermal equilibrium. In this situation the heat flow behaves as the thermal equivalent of DC current. However, in many situations the power dissipation of the system is often not constant, for example when the device conducts varying or pulsed currents. In these situations the heat flow

behaves as the thermal equivalent of AC current, and the “capacitances” of the circuit must be taken into consideration.

Thermal capacitances exist because the elements in the heat transfer path take a finite amount of time to heat up or “charge” to their equilibrium temperature. In practice this has beneficial effects: if excessively high dissipation peaks occur, it is possible that the maximum junction temperature will not be exceeded, provided that the pulse is not too long - just as an electrical capacitor will prevent voltages exceeding certain limits in the presence of current spikes.

The two most common situations are:

- a) A single “square” pulse of intensity P_d and duration t_0 (representing the switching on/off of loads, such as lamps, motors, inductive loads)
- b) A train of “square” pulses with intensity P_d , duration t_0 and duty cycle DC.

In both cases an important parameter is the thermal capacitance C_{th} associated with the various structural elements of the thermal chain from the junction to the ambient. This parameter can be expressed as:

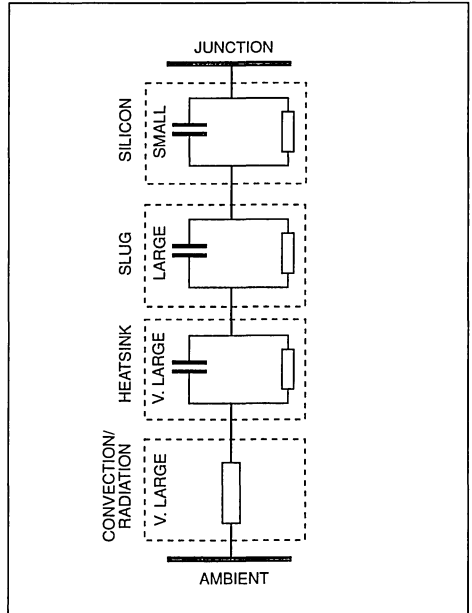
$$[6] \quad C_{th} = c \cdot d \cdot V$$

where c is the specific heat, d is the density and V is the volume of the material.

In a simple model, the above elements are the silicon, the slug and the external heat sink. These can be modelled as RC cells, as shown in figure 13.

The first cell represents the thermal behaviour of the silicon itself, characterized by a small volume with a correspondingly low thermal capacitance (a few mJ/°C). The thermal resistance between the junction and the silicon/slug interface is about 0.2-2°C/W depending on the die size and on the size of the dissipating element on the chip. The time constant τ ($= R.C$) of this first cell is typically in the order of few milliseconds.

Figure 13: RC equivalent of thermal path from junction to ambient



The second cell represents the copper slug, with a relatively large thermal capacitance and a time constant of a few seconds.

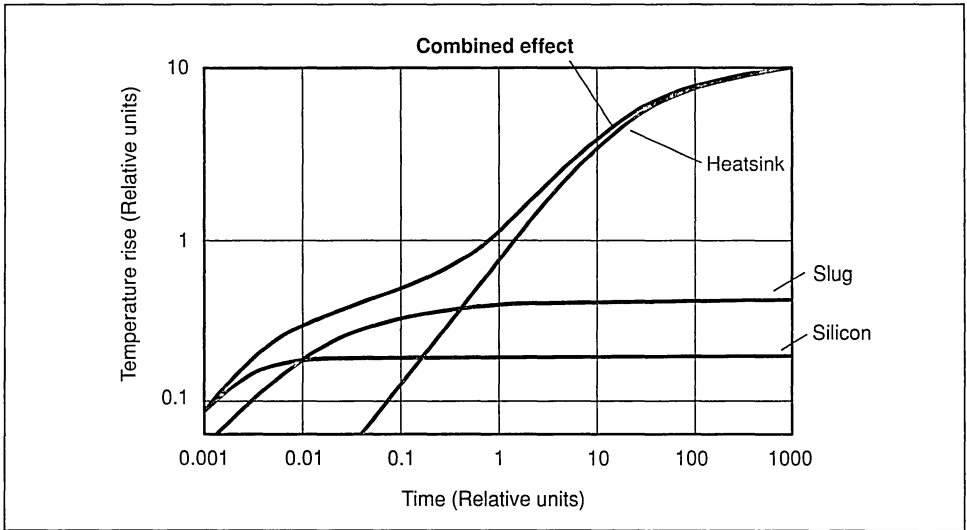
When an external heat sink is used the third cell can have a time constant of hundreds of seconds and equilibrium can take several minutes. A simplified example of the contribution of the different cells is given in figure 14; each element is ruled by an theoretical relationship

$$[7] \quad \Delta T = \theta \cdot P_d [1 - e^{-t/\tau}]$$

and the actual behaviour of the package is a combination of the effects of the three cells.

A large plateau occurs up to 1-2 sec, due to the copper slug, limiting the thermal impedance to 0.2 - 2.0°C/W. This effect is often used in switching applications, as a large number of power pulses can be dissipated before there is a large variation in the junction temperature.

Figure 14: Contribution of each thermal cell (Qualitative)



4. HEATSINK MOUNTING CONDITIONS

This section will describe recommended procedures for mounting power packages on a heatsink, and precautions to minimise the thermal resistance at the contact with the heatsink.

4.1 - Insertion packages

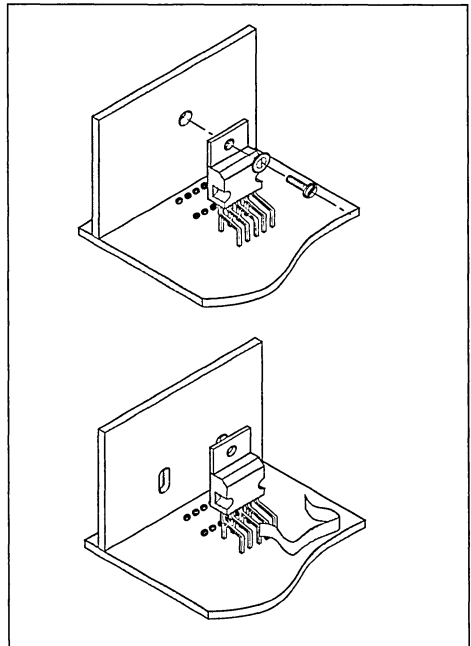
Insertion packages are secured to the heatsink using screws, bolts or rivets fixed through the hole in the upper part of the copper tab (figure 15a). In order to reduce the cost of mounting, the use of clips is becoming more common, with the pressure applied to the top of the plastic body, at the centre (figure 15b).

The contact thermal resistance θ_c can be minimized by adding a thin layer of silicon grease, uniformly distributed between slug and dissipator and applying an appropriate force.

In case of screw mounting, this force can be controlled by choosing the torque (in kg.cm) applied to the fixing screw, by means of a dynamometric screwdriver.

Figure 15: Securing insertion packages

- a) Screw fixing
- b) Clip fixing



Experimental values of θ_c are shown in table 6 with different torque levels, for both conditions with and without grease.

In practical cases, the recommended value of torque is 6-8 kg.cm. Values up to 10 kg.cm. are possible, but in order to avoid mechanical damage to the package or to the silicon die, the planarity of the interfaces

between the tab and heat sink must be better than 50 μ m.

When a spring clip is used, the danger of mechanical damage is much reduced. In this case θ_c is also decreased if the force F of the clip is higher; a minimum of 5kg is recommended.

Table 6: Contact thermal resistance for TO-220 package (experimental data)

TORQUE kg/cm	θ_c with grease °C/W	θ_c without grease °C/W
3	0.27	0.9
4	0.22	0.82
5	0.17	0.78
7	0.12	0.75
10	<0.1	<0.7
12	<0.1	<0.7
15	<0.1	<0.7

4.2 Surface mount packages

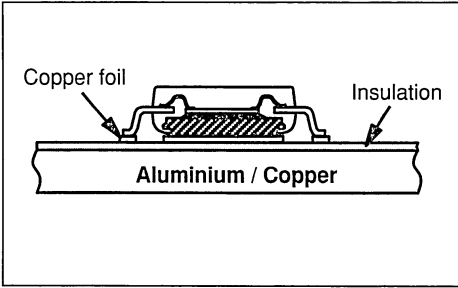
In surface mount technology power dissipation is a major issue, because of the density of components and the problems involved in applying a large external heatsink to a miniaturized package. However a number of solutions have been studied and are presented here, although it should be remembered that this subject is relatively new and progress in the technology will provide more efficient solutions in the future.

4.2.1 Power substrate

This solution uses a specially developed substrate, with aluminium foils used as a baseplate, known as an Insulated Metal Substrate (IMS) - see figure 16.

A copper printed circuit is constructed on the top of the Al plate and isolated with a heat conductive polyimide layer. The surface mount package slug is soldered using PbSn in pre-defined areas. Because of the isolating layer, the junction to substrate

Figure 16: Cross section of PowerSO-10 mounted on IMS



thermal resistance is slightly higher than θ_{jc} , about 0.5-0.7°C/W, which is acceptable for most applications. For large dissipation, the power substrate can be screwed to a suitable external heatsink, and up to 20W dissipation can be managed in practical cases.

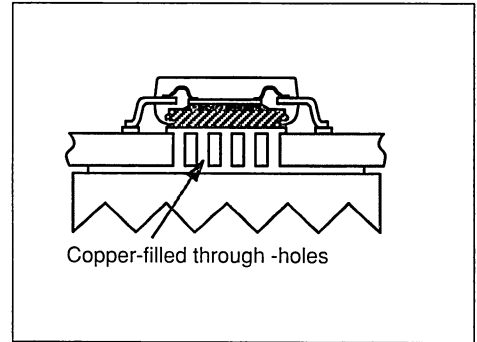
4.2.2 PCB layout

If a power substrate cannot be used for any reason, the PCB layout should be designed to minimize the thermal resistance between

its upper face, onto which the power devices are soldered, and its lower face, where the heatsink is attached.

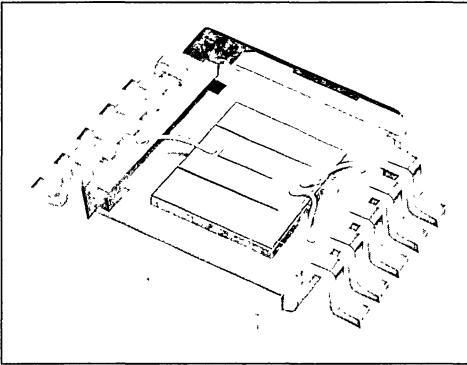
This can be achieved using holes drilled through the PCB and filled with copper, as shown in figure 17. This solution can provide up to 5-6W dissipation, with θ_{PCB} in the range of 7-9°C/W.

Figure 17: Copper filled holes to reduce thermal resistance



THE Power SO-10™: A NEW SURFACE MOUNT POWER PACKAGE

by A. Ehnert, V. Sukumar and J. Diot



ABSTRACT

A new surface mount power package is introduced in this paper. Today there is a great need for a true high power surface mount package. This power package was designed from the start with surface mounting in mind, and is thus suitable for all reflow soldering methods. The main advantages of the package are excellent thermal performance, high power capability and high power density, versatility and thermally efficient reliable soldering. This paper shows that the new PowerSO-10 is a perfect successor to the well-known TO-220 package for the SMT environment.

1. THE NEED FOR SURFACE MOUNT POWER

During the last 10 years, as the size of electronic assemblies decreased and their reliability increased, there has been a need, across the board, for various components which have to be surface mounted. So far there have been very few components designed specifically for high power surface mounting.

The completely moulded SO-packages that can handle very limited power, or adaptations of discrete through-hole packages like the TO-220 for surface mounting, have until now been the only two alternatives available. This paper introduces a high power package that has superior characteristics to the TO-263, a surface mount version of the TO-220

package (lead-formed with the protruding part of the tab cut-off).

Surface mounting, by its very nature, is restricted to smaller footprints, but power devices need larger footprints to dissipate heat. The PowerSO-10 is an optimized balance between these two conflicting requirements.

Desirable features of a surface mount package include:

1) Real power dissipation capability. It should be capable of accommodating large die. The greater the area of heatsink available, the better. Small overall size and low package height are very important.

2) Versatility. It should handle various die, including devices with large pin-outs.

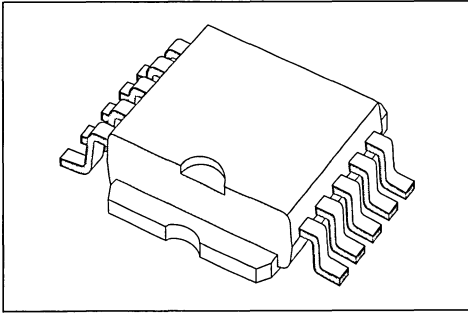
3) Compatibility with different surface mount processes. It should be suitable for Tape and Reel delivery.

4) Excellent package reliability. Today, package reliability is an absolute necessity in every industry. This requirement is even more important for surface mount components, since rework is comparatively difficult. In automotive, consumer and computer applications where this package is most attractive, reliability standards are very high.

2. THE STRUCTURE AND THERMAL CHARACTERISTICS OF THE POWERSO-10 PACKAGE

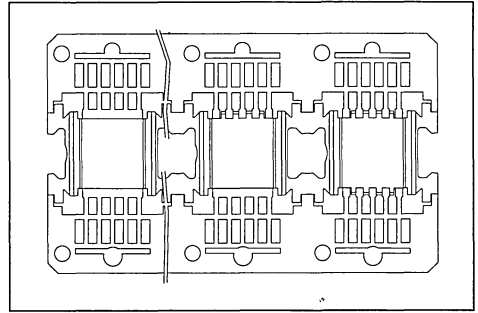
The PowerSO-10 package is shown in Figure 1. It was decided to manufacture a 10 pin DIP package to enable it to be used for intelligent power devices, which require many leads. Discretes can use high pin count packages to distribute the current through the power circuit. This also offers the designer more flexibility to lay out the board i.e. the power unit and driving unit can be separated. Figure 2 shows a typical lead frame, demonstrating the different options available. The leads are either separated to allow multiple outputs (eg. for VIPower devices), or all the

Figure 1. PowerSO-10 package



leads on each side are connected to increase the current handling capability. The maximum die size is the same as TO-220 and its derived versions (180x220 mils²). For a number of years, automotive assemblies in particular have surface mounted through-hole TO-220 devices with their tab removed and leads formed. Other circuits use through-hole mounting with TO-220s up to the leads' standoff to decrease the height of the devices. The lowering of the PowerSO-10 package height results in about a 37% decrease in total volume of the package, while the spreader area remains large. Not only does this result in a lower package cost, but at high operating frequencies, low height and inductance big advantage.

Figure 2. Leadframe options of PowerSO-10 package



Various devices including rectifier diodes, protection diodes, triacs, ASDs (Application Specific Devices), VIPower such as single/double high/low side drivers, electronic ignition circuits, and Power transistors (Bipolar, MOSFETs and IGBTs) are offered in this package.

The thermal characteristics of the PowerSO-10 package are comparable with those of the TO-220, as the frames are structurally similar. Steady-state thermal resistance (junction-case) studies show approximately 0.8°C/W for both the PowerSO-10 and TO-220. See table 1 for a comparison of these packages.

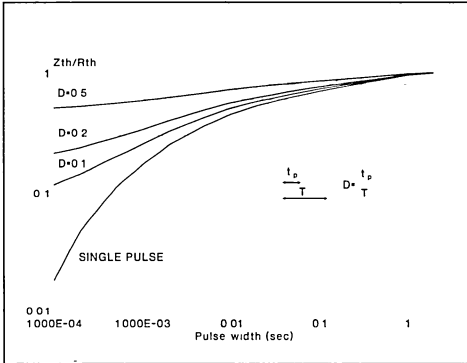
Table 1. Comparison PowerSO-10 and TO-220 SMD-version

DESCRIPTION	TO-220 SMD-version	PowerSO-10	DELTA
Footprint Area in mm ²	203	141	-30%
Heat Spreader in mm ²	50 to 60 (#)	67	+10% to 30%
R _{(m(t-c))} in °C/W	0.8	0.8	equal
Chip Size in mils ²	180x220	180x220	equal
Total Volume in mm ³	597	373	-37%
Package Height in mm	4.5	3.5	-22%

(#) area varies depending on manufacturer

Thermal management in switched power applications is one of the key points in the design of a cost effective circuit. By considering the effect of thermal capacitance, the junction temperature can be limited to the rated values, even in the presence of high transients. Figure 3 shows typical thermal impedance curves. The test vehicle used was a bipolar transistor with a die size of 32 000 mils².

Figure 3. Normalized thermal impedance of a typical device in PowerSO-10

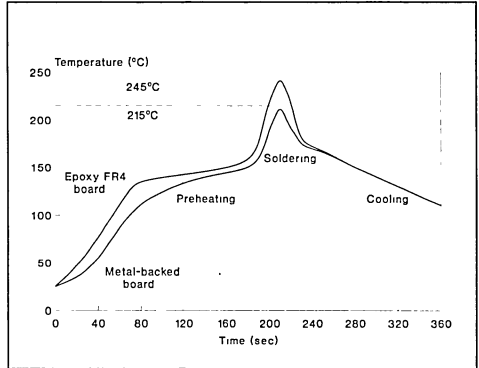


3. SOLDERING INFORMATION

The soldering process causes considerable thermal stress to a semiconductor component. This has to be minimized to ensure a long and reliable life of the device. The PowerSO-10 package can be exposed to a maximum temperature of 260°C for 10 seconds. However, correct soldering of the package is guaranteed at 215°C for 3 seconds after 8 hours ageing in steam. Any solder temperature profile should be within these limits. As reflow techniques are most common in surface mounting, typical heating profiles are given in Figure 4, either for mounting on FR4 or mounting on metal-backed boards. For each particular board however the appropriate heat profile must be adjusted experimentally. The following points must always be considered:

- The device should always be preheated
- Peak temperature should be at least 30°C higher than the melting point of the solder chosen
- The amount of heat supplied must be adjusted according to the thermal conductivity/thermal mass of the base substrate
- All components mounted on the board must have sufficiently high thermal limits.

Figure 4. Typical reflow soldering heat profile



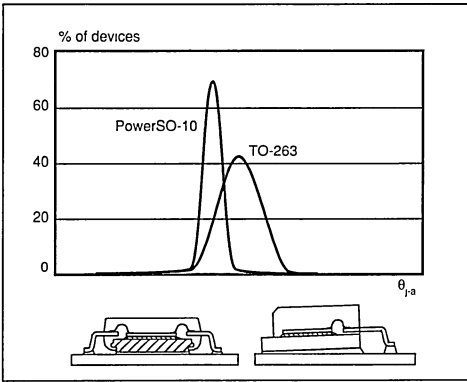
Voids pose a difficult reliability problem for large surface mount devices. Pockets of air under the package result in poor thermal contact and the resulting high thermal resistance leads to component failures. Because of coplanarity problems, weight balance is critical. Since the PowerSO-10 has been designed solely to be a surface mount package, symmetry in the x- and y- planes gives the package excellent weight balance. Moreover, the PowerSO-10 offers the unique opportunity to easily check the flatness and quality of the soldering process. Both the top and the bottom soldered edges of the package are accessible for visual inspection. The PowerSO-10 is a package "designed for testability". Coplanarity between the substrate and the package can be easily verified. The quality of the solder joints is very important for two reasons: firstly poor quality solder joints result directly in poor reliability, and secondly solder thickness affects the thermal resistance significantly. Thus a tight control of this parameter results in thermally efficient and reliable solder joints. Thermal conductivity in the region of 0.5°C/W can easily be lost through uneven solder and poor coplanarity of tabs and leads (see Figure 5)

4. SUBSTRATES AND MOUNTING

Here we will discuss two of the various techniques for mounting power surface mount devices.

The use of epoxy FR4 boards is quite common in through hole techniques; for surface mounting techniques, however, its poor thermal conduction means that it is not possible to benefit from the outstanding thermal performance of the PowerSO-10. Here below we will discuss some methods to reduce this limitation.

Figure 5: Loss of thermal performance due to poor coplanarity and uneven solder joints



One way to improve the thermal conduction is the use of large heat spreader areas at the copper layer of the PC board. This leads to a reduction of thermal resistance to 30 - 36°C/W for 3 to 6 cm² on-board heatsink (see fig. 6.2.).

Use of copper-filled through holes on conventional FR4 techniques increases the metallization and decreases thermal resistance accordingly. Using a configuration with 16 holes under the spreader of the package with a pitch of 1.8mm and a diameter of 0.7mm, the thermal resistance (junction - heatsink) can be reduced to 12° C/W (see fig. 6.3.). Apart from the thermal advantage, this solution allows the use of multi-layer boards. However, the limitations of this conventional material prevent its use in very high power, high current circuits. For instance, it is not advisable to surface mount devices with currents greater than say, 20A on FR4 boards. A Power MOSFET or Schottky diode in a surface mount power package can handle up to 50A if better substrates are used.

A new technology available today is IMS - an Insulated Metallic Substrate. This offers greatly enhanced thermal characteristics for surface mount components. IMS is a substrate consisting of three different layers: the base material which is available as a aluminium or a copper plate, a thermally conductive dielectric layer, and a copper foil, which can be etched as a circuit layer. Using this material a thermal resistance of 8°C/W with 40 cm² of board floating in air is achievable (see fig. 6.4.). If even higher power is to be dissipated, an external heatsink

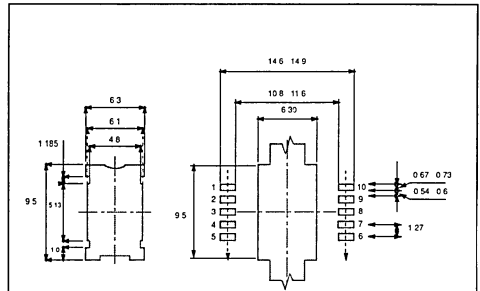


Figure 6.1: Header and pad layout

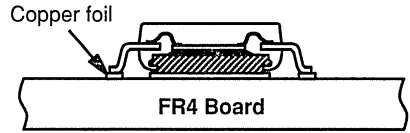


Figure 6.2: Mounting on epoxy FR4 - heat dissipation by extending the area of the copper layer

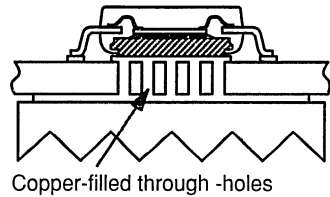


Figure 6.3: Mounting on epoxy FR4 using copper-filled through-holes for heat transfer

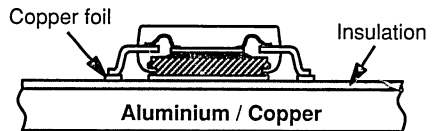
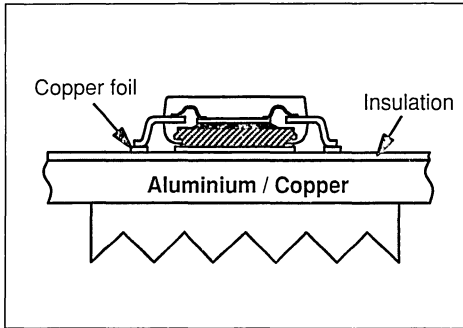


Figure 6.4: Mounting on IMS-board

Figure 6.5: Mounting on IMS-board with an external heatsink applied



could be employed, which leads to a $R_{th(j-a)}$ of $3.5^{\circ}\text{C}/\text{W}$ (see fig.6.5.), assuming that $R_{th(\text{heatsink-air})}$ is equal to $R_{th(\text{junction - heatsink})}$, which is commonly applied in practice. Often power devices are compared by considering the maximum rated temperature of the device; for PowerSO-10 it is 175°C . A summary of the different mounting methods based on a reasonable delta T of 70°C junction to air is shown in table 2.

Table 2. Comparison of different mounting methods (Delta $T_{(j-a)} = 70^{\circ}\text{C}$)

PowerSO-10 package mounted on	$R_{th(j-a)}$	P_{Diss}
1. FR4 using the recommended pad-layout	$50^{\circ}\text{C}/\text{W}$	1.5W
2. FR4 with heatsink on board (6 cm^2)	$35^{\circ}\text{C}/\text{W}$	2.0W
3. FR4 with copper-filled through holes and external heatsink applied	$12^{\circ}\text{C}/\text{W}$	5.8W
4. IMS floating in air (40 cm^2)	$8^{\circ}\text{C}/\text{W}$	8.8W
5. IMS with external heatsink applied	$3.5^{\circ}\text{C}/\text{W}$	20W

Another option that is gaining popularity today is chip-on-board (C.O.B.) technologies. Here the big challenge from the manufacturer's standpoint is how to test high power chips. Accurate testing of chips at wafer level is difficult. Today's techniques result in good die being thrown away, decreasing yields. The PowerSO-10 concept represents an attractive alternative to C.O.B. techniques. PowerSO-10 offers devices fully tested at low and high temperature. Mounting is easy - only conventional SMT is required - enabling the users to avoid bond wire problems and also the problem of controlling the high temperature soft soldering. An optimum thermal management is guaranteed through PowerSO-10 as the power chips have to be mounted on heat spreader anyway before being mounted onto the substrate.

5. RELIABILITY DATA

Originally, this package was developed for the automotive market, which is known for exacting reliability standards. The information presented in this section shows that the PowerSO-10 will work reliably when quality tests for standard power devices are performed. A list of the tests, their features and failure modes associated with these tests is given in Table 3.

In most plastic semiconductor packages, good adhesion between the frame and the epoxy resin is critical for good package reliability. This should be built into the package design. A state-of-the-art transfer molding process with low stress and high adherence resins is used for PowerSO-10 production. Table 4 shows a complete qualification program performed on a 20 Amp High Side Driver, the VN20NSP. The package passed all package-relevant tests such as T.H.B (High temperature - humidity - bias), thermal cycles / shocks and pressure cooker successfully. The test criteria and acceptance conditions are the same as those for standard through-hole packages like TO-220. Further it is essential for automotive applications, that MOSFETs and other devices in the PowerSO-10 package are rated up to 175°C .

Table 3. Reliability test description

TEST	FEATURES	PURPOSE
H.T.B	Biased device at elevated temperature	To detect surface defects like poor passivation, contamination
T.H.B.	Biased on in presence of steam	Metal corrosion detection
Thermal shock and thermal cycles	Shock samples placed in liquids at high, low temperature. Cycles samples in high, low temperature ambient	Detect cracked die, wire bond breaking, mechanical damage to package
Pressure Pot Pressure Cooker	High temperature & pressure with saturated steam	Electrochemical and galvanic corrosion
Marking Permanency	10 strokes with brush per MIL Stds.	Measures resistance to solvent
Solderability	Verifies tinning process	Detects poor solder joints
Terminal Ruggedness	Pull strength of the terminals	Detects poor welds

Table 4. Reliability Test Results (VN20SP)

Failure / Sample size

TEST	RESULTS (1st lot)	RESULTS (2nd lot)	RESULTS (3rd lot)
H.T.B. off condition Ta = 125°C + Bias	0/100 @ 1000h	0/100 @ 1000h	0/100 @ 1000h
T.H.B. Ta = 85°C; HR = 85% + Bias	0/100 @ 1000h	0/100 @ 1000h	0/100 @ 1000h
Thermal cycles Air to Air -65°C to +150°C	0/100 @ 500h	0/100 @ 500h	0/100 @ 500h
Pressure Cooker Ta = 121°C; Pa = 2bar	0/100 @ 168h	0/100 @ 168h	0/100 @ 168h
H.T.S. Ta = 150°C	0/100 @ 1000h	0/100 @ 1000h	0/100 @ 1000h
Marking permanency	0/100	0/100	0/100
Solderability	0/100	0/100	0/100
Terminal ruggedness	0/100	0/100	0/100
Thermal shock Liquid to liquid -85°C to +150°C	0/100 @ 100sh	0/100 @ 100sh	0/100 @ 100sh

6. CONCLUSION

In this paper the Power SO-10, a new surface mount power package, has been introduced. It is the equivalent of the well-known TO-220 package designed specifically for the surface mount industry. The main advantages of the PowerSO-10 package are:

- 1) Good thermal characteristics. Capacity to handle die the same size as TO-220.
- 2) Versatility. Ten output pins to handle a wide variety of discrete and integrated power products.
- 3) Solder interface visible at the top and bottom of the package. Solder quality can be inspected visually
- 4) High power density through reduced package volume and height. Symmetrical package design.

In the future, the need for higher power surface mount packages will increase dramatically as surface mount technology becomes even more widespread. Power surface mount packages that can house even larger die and have lower thermal resistances will become more popular. Inexpensive plastic power surface mount packages that can accommodate more than ten pins will become common as intelligent power circuits gain popularity.

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March 1993

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SWITCH MODE POWER SUPPLIES

A COST EFFECTIVE ULTRA FAST Ni-Cd BATTERY CHARGER

ABSTRACT

Cordless and portable battery powered equipment are proliferating thanks to the increasing capacity of rechargeable Ni-Cd batteries. A useful feature in applications where the battery is rapidly discharged, such as power tools, is ultra fast charging in under an hour. The solution described in this paper is an efficient 100kHz converter charging a Ni-Cd battery in half an hour. The battery charge is monitored by a low cost microcontroller (ST6210) enabling battery voltage identification, temperature monitoring and charge control.

1. INTRODUCTION

Today, many types of cordless and portable equipment are supplied by a Ni-Cd battery. Ultra fast charging in under one hour is a very attractive service for users. Such a short charging time requires a charge control circuit that is more complex than for standard chargers.

The power converter presented in this paper is able to fully charge a common Ni-Cd battery pack of 7.2V/1.2Ah in 30 minutes. It has a corresponding output power capability of roughly 35W and operates as a current source providing a constant 3.5A current to the battery while charging.

The battery charger is controlled by a low cost microcontroller, the ST6210. This control is compatible with the charge of Ni-Cd battery packs from 2 to 6 cells (2.4V to 7.2V). The microcontroller IC is supplied from an auxiliary winding of the power transformer.

2. THE POWER CONVERTER

2.1 Circuit description

The asymmetrical half-bridge is considered today as one of the most attractive topologies for the primary side of a 220V ac off-line Switch Mode Power Supply, SMPS, see figure 1.

Contrary to single switch structures, the leakage inductance of the power transformer is much less critical. The two demagnetisation diodes, BYT01/400 provide a simple non-dissipative way to

by L. Wuidart, J.M. Ravon

systematically clamp the voltage across the switches to the input DC voltage, V_{in} . This allows the use of standard 500V Power MOSFETs such as the isolated ISOWATT220 packaged IRF820FI.

The power converter is totally controlled from the primary side with a standard PWM control IC, the UC3845, regulating in current mode. A single optocoupler controls how the SMPS functions, either in battery charge mode or in burst mode standby current charge. The charger is controlled from the secondary side of the SMPS by the microcontroller via this optocoupler.

The switching frequency has been fixed at 100kHz, in order to keep the magnetic part to a reasonable manufacturing cost level. The power transformer and the output inductor can be integrated on a single ferrite core [1][2]. Well optimised, this integrated magnetic technique can bring significant shrinking of the power converter size.

2.2 "Transformerless" driver

In an asymmetrical half bridge, the high side Power MOSFET requires a floating level shifter circuit in order to be driven properly. Usually, this level shifter function is realised with a pulse transformer.

In this application, the level shifter is simply an auxiliary winding of the power transformer plus a few discrete small signal devices (see figure 1).

The high side Power MOSFET is turned on as soon as the transformer primary inductance is completely demagnetised.

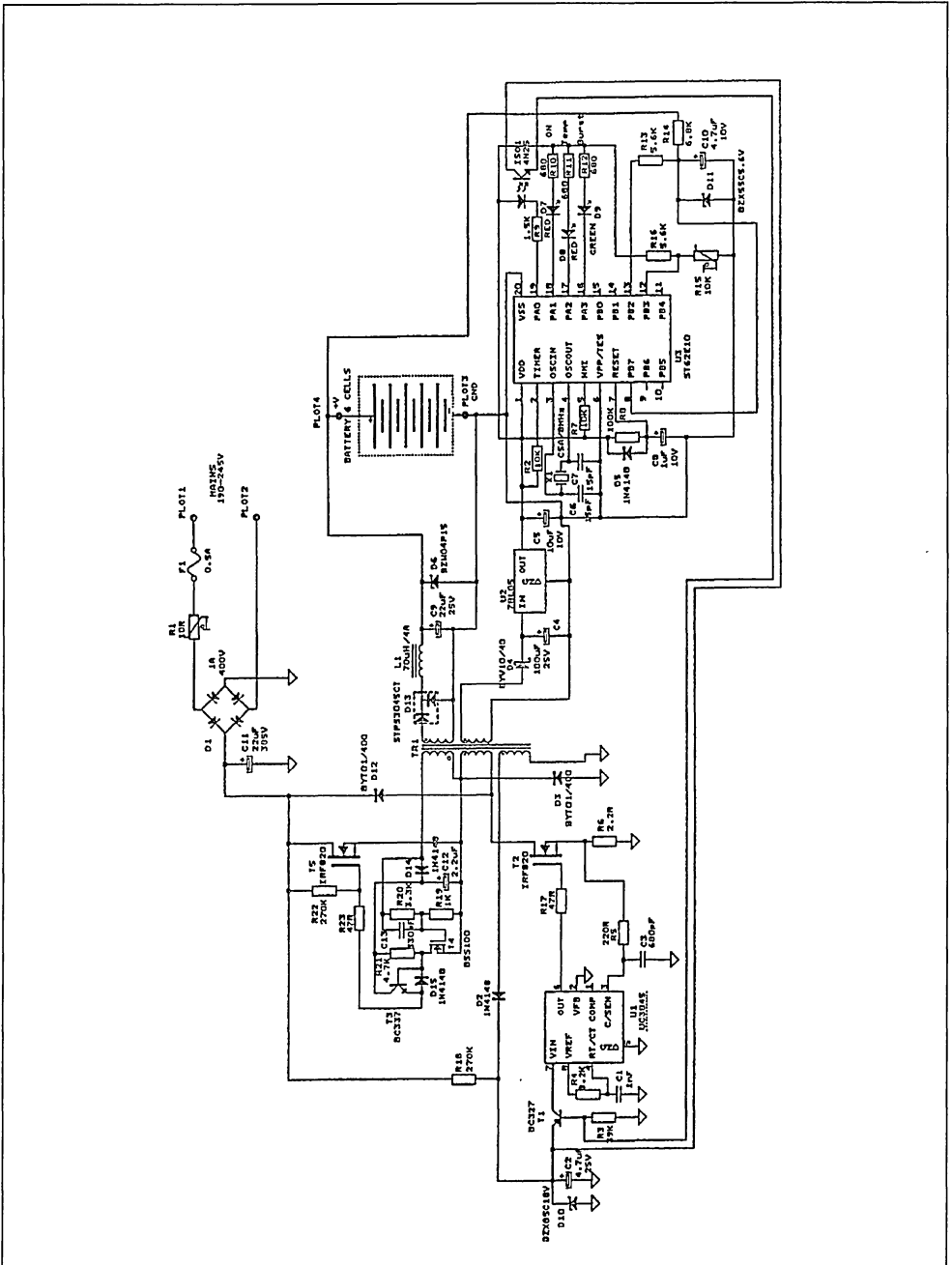
At turn off, the high side Power MOSFET is synchronised with the low side device by the voltage polarity inversion across the auxiliary winding.

2.3 Current mode forward

A Ni-Cd battery requires charging with a constant current. A current mode control is the recommended way to realise such a charge characteristic. In a Forward converter, the primary peak current gives an image of the current flowing in the output choke.

An output current ripple of 25% instead of the typical

Figure 1. Ultra fast Ni-Cd battery charger schematic



10% encountered in conventional forward SMPSs, is quite acceptable for correct charge of Ni-Cd batteries. A larger output current ripple also gives a steeper primary current ramp (see figure 2).

This way, the current spike due to rectifier recovery, typically occurring on the leading edge of the waveform, does not stop the pulse prematurely.

The current mode control can be easily realised with a sufficient noise immunity from the primary side by using a simple current sense resistor (see figure 1).

Constant DC output current is regulated by limiting the primary peak current to a fixed value.

This type of current mode control provides a natural pulse-by-pulse short-circuit protection. Moreover, this current mode control supplies the battery with a constant current of 3.5A whatever the input line

voltage variations (from 245V DC to 375V DC).

A low cost PWM current mode IC such as UC3845 is well suited to regulate the complete power converter efficiently.

3. BATTERY CHARGE CONTROL

3.1 Ultra fast charge control method

For ultra fast charge systems - under half an hour - the majority of battery manufacturers recommend the negative delta voltage method ($-\Delta V$) otherwise called negative slope cut-off circuit [3] [4].

When a Ni-Cd battery reaches full charge, its voltage decreases slightly (see figure 3).

The negative delta voltage method ($-\Delta V$) consists of stopping the charge as soon as the voltage characteristic slope becomes negative. This

Figure 2. Using a steeper primary current ramp to cancel effect of diode recovery current spike

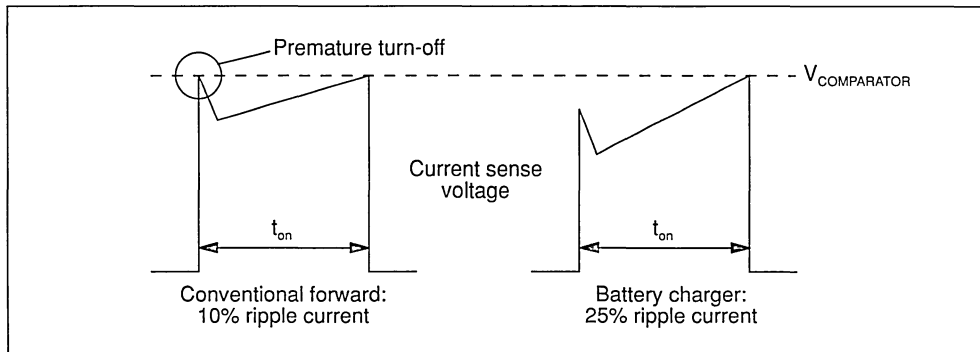
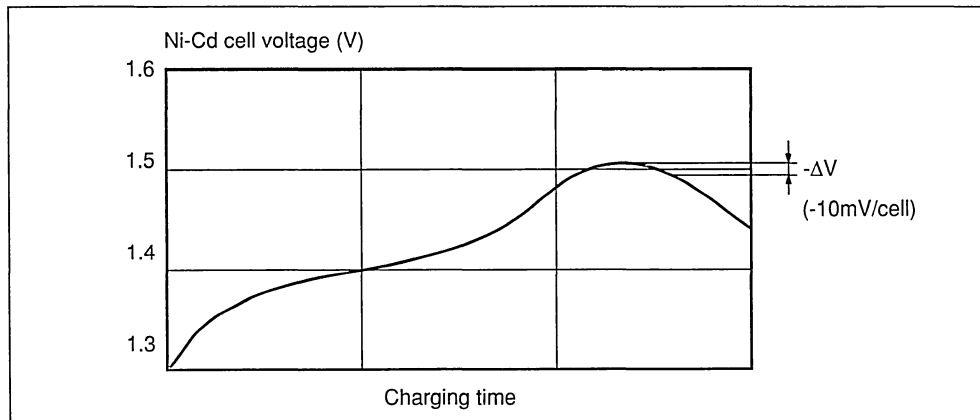


Figure 3. Charging characteristics of a single Ni-Cd cell



technique allows the very rapid charge of a Ni-Cd battery, near to its full capacity. Moreover, no compensation for the age of the battery is required because only relative voltages are measured.

In this application, the battery voltage is sensed by a ST6210 micro-controller housed in 20 pin dual in line package. The integrated analogue to digital (A/D) converter of this microcontroller is able to detect a typical voltage drop of -10mV/cell. The overall system is reset after each new mains connection. The ST6210 can automatically identify the battery voltage from 2 to 6 cells (2.4V to 7.2V).

3.2 Monitoring functions

The battery charge is totally monitored by an 8-bit HCMOS micro-controller (in PDIP or PSO 20 pin package), the ST6210 [5]. By using this microcontroller, additional monitoring functions can be easily added to the ultra fast charge control program.

3.2.1 Stand-by current charge: Burst mode

Once the negative voltage drop has been detected by the microcontroller, the ultra fast charging is stopped and the power converter supplies the battery with a stand-by current of around 100mA. This stand-by charge is provided by burst mode current control.

The converter is successively turned on and off at 50Hz with a small duty cycle of 0.03. The microcontroller manages this burst mode from the

secondary side via an optocoupler, to the auxiliary supply of the PWM control IC (UC 3845).

Thanks to the low current consumption of this HCMOS micro-controller, a small 100µF reservoir capacitor (see figure 1) is sufficient to keep the ST6210 properly powered during the off periods of the burst mode.

3.2.2 Battery temperature protection

A Temperature protection is simply realised by using an NTC resistor placed on the battery pack. This NTC is directly connected to another input of the A/D converter of the ST6210. When the battery temperature reaches 40°C during an Ultra Fast charge phase, the micro-controller turns the converter into burst mode to protect the battery.

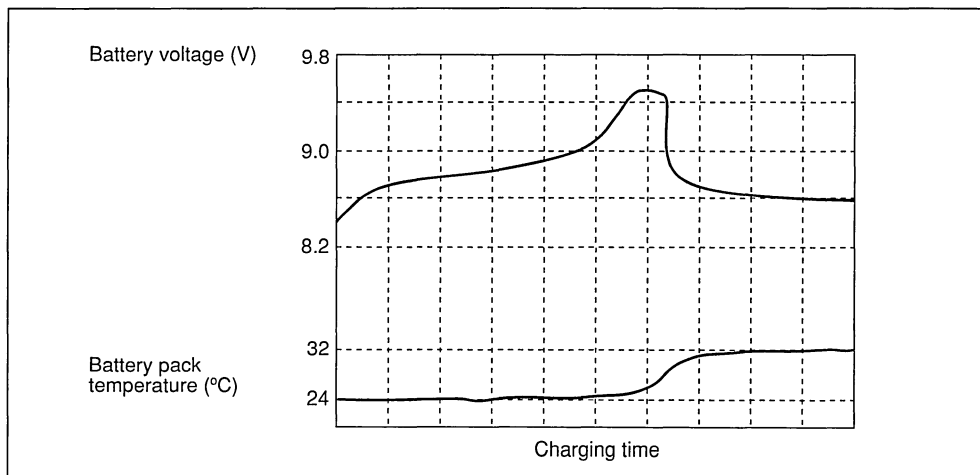
3.2.3 Battery presence

The micro-controller detects whether the battery pack is connected or not. When the battery is not connected, the microcontroller turns the converter into burst mode. The resulting stand-by current (100mA) flows into the output Transil diode (BZW04P15, see figure 1).

4. PRACTICAL RESULTS

The battery voltage and pack temperature versus charging time are shown in figure 4. These recordings have been made with a popular 1.2Ah/7.2V Ni-Cd battery pack for cordless drills. The temperature of the battery pack does not exceed 32°C for an ambient temperature of 23.6°C.

Figure 4. Battery voltage and pack temperature versus charging time



5. CONCLUSION

Charging a Ni-Cd battery in half an hour can save battery packs and time. It can expand the use of battery powered equipment, especially for professional applications. Such an ultra fast charge has to be carefully monitored to maximise the life time of the battery and the charge safety. Moreover, this improvement should be achieved with compact equipment including a minimum of components.

The forward half-bridge circuit for this battery charger has been realised without any pulse transformer.

The paper shows that an ultra fast charge can be totally monitored by a single 20 pin HCMOS microcontroller, the ST6210. The actual software includes a stand-by charge, temperature protection, battery presence detection and battery voltage rating identification.

Other specific requirements can be implemented inside the existing microcontroller program.

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USE OF INTERNAL MOSFET DIODE IN BRIDGE-LEGS FOR HIGH FREQUENCY APPLICATIONS

by C.K. Patani - D. Steed - J.M. Charreton

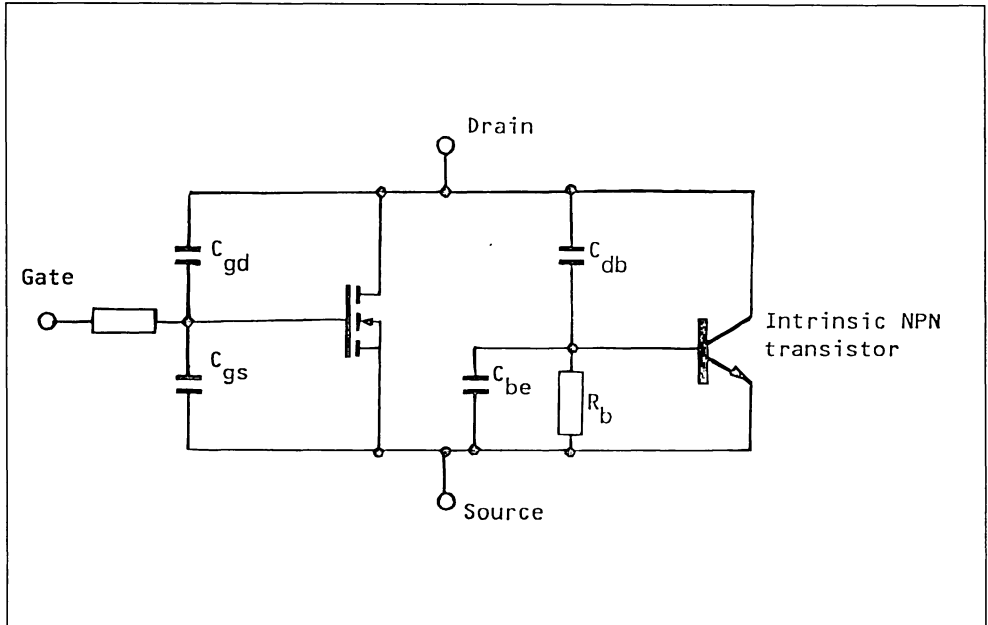
ABSTRACT

Reverse recovery of the intrinsic MOSFET diodes is investigated for the classical MOSFET and the MOSFET with minority carrier lifetime control. Turn-on losses in bridge-legs using intrinsic MOSFET diodes limit the switching frequency particularly in the case of the classical MOSFET. Adapted bridge-leg configurations are presented which enable the use of the intrinsic MOSFET diodes for the free wheeling function in inductive load switching without any appreciable reverse recovery current and MOSFET turn-on switching losses !

INTRODUCTION

The MOS field effect transistor (MOSFET) contains an intrinsic PN diode within the structure which can conduct a current from source to drain. The PN junction diode is in fact part of a parasitic NPN bipolar transistor as shown in figure 1. Free-wheeling

diodes in bridge-legs are necessary when switching inductive loads. The intrinsic diode can be used to fulfil this free-wheeling function. However, the intrinsic diode of the classical MOSFET has a long reverse recovery time and "snap-off" characteristic which can cause large dV/dt . The snap-off can result in the device failing in one of two ways. Firstly, due to internal capacitances, C_{db} and C_{be} , a base current may be established which turns-on the intrinsic bipolar transistor (see figure 1)¹. Secondly, the dV/dt may be such that the drain to source voltage of the MOSFET exceeds the blocking voltage thus causing avalanche breakdown. This paper investigates various means of limiting the maximum reverse recovery current of the intrinsic diode to ensure reliable operation. A comparison is made between the novel solutions presented permitting the use of internal diode, and conventional solutions for using MOSFETs in bridge-legs, such as lifetime controlled MOSFETs and series blocking diodes.

Figure 1 : Equivalent Circuit for a MOS Field Effect Transistor (MOSFET).


METHODS OF LIMITING REVERSE RECOVERY CURRENT

Limiting the reverse recovery current of the intrinsic diode can be achieved by stopping current from passing through the blocked MOSFET by means of a series blocking diode or limiting the rate of change of current in the intrinsic diode. The snap-off characteristics of the internal diode can be limited by having small RC snubbers across the drain to source of MOSFETS in bridge-leg configuration. Solutions which limit the rate of change of current in the intrinsic diode are discussed below.

BRIDGE-LEG DESIGNS UTILIZING MOSFET INTRINSIC DIODES

a) SOLUTION WITH UNCOUPLED UNSATURABLE INDUCTORS

In the circuit shown in figure 2, if T1 is blocked and T2 is conducting, the load current flows through T2.

As T2 turns-off the current transfers to the freewheeling diode D2, as the rate of change of current into the intrinsic MOSFET diode of T1 is limited by inductors L1 and L2. The zener voltage across Z2 causes the current to transfer from the external freewheeling diode D2 to the intrinsic MOSFET diode in T1 until D2 no longer conducts (as shown in figure 3). When T2 is turned-on subsequently the current transfers from the intrinsic diode of T1 to T2. The reverse recovery of the intrinsic diode is, however, limited by inductances L1 and L2. This can be seen clearly in figure 4. The bridge-leg can be designed (by dimensioning L1, L2 and Vz) such that the external freewheeling and zener or transil diodes only conduct for a small fraction of the freewheeling period. Consequently, they do not have to be mounted on a heatsink. The disadvantage of using the zener is that the MOSFETs must now be rated for at least the high voltage DC rail, HVDC, plus the zener voltage.

Figure 2 : Bridge-leg with Uncoupled Unsaturable Inductors.

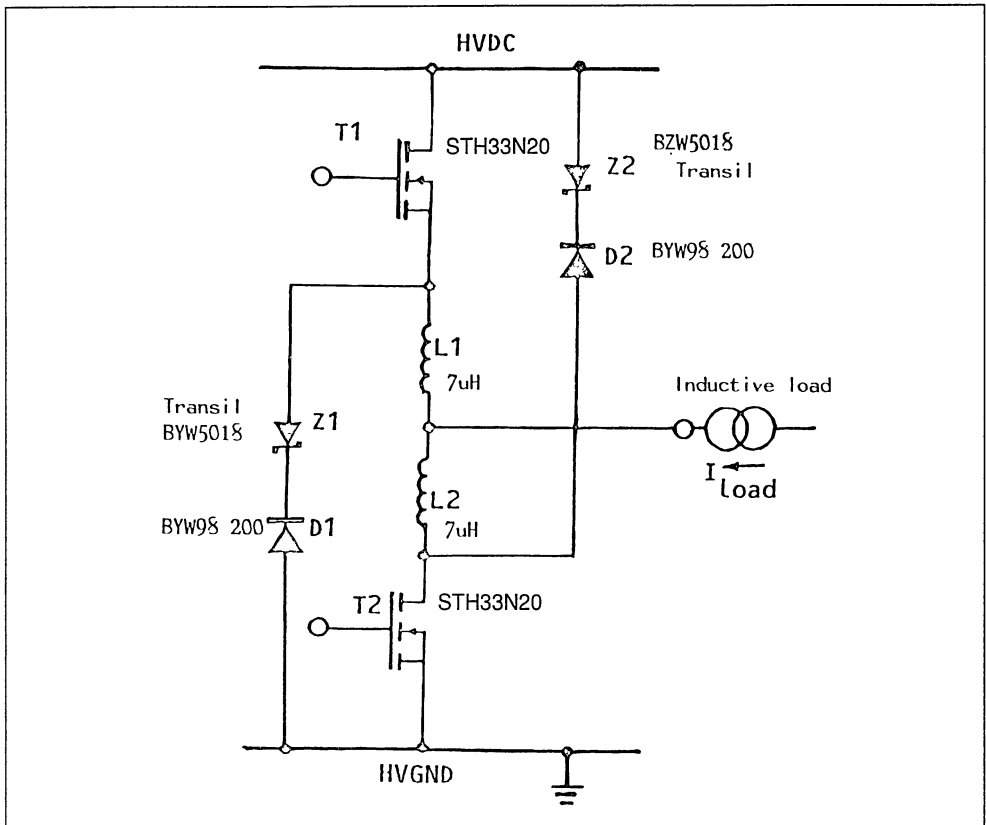
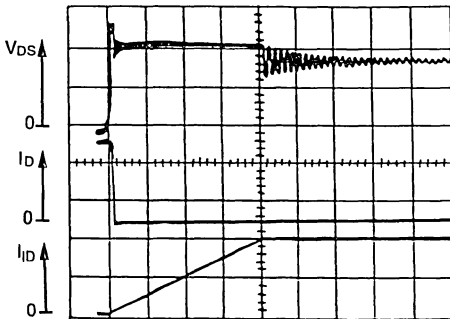
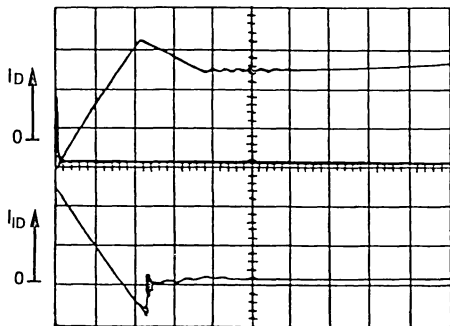


Figure 3 : Transfer of Current to Intrinsic Diode.

Time scale : 2 μ s/DIV
 V_{DS} : 50V/DIV
 I_D : 10A/DIV

Intrinsic
 Diode : 10A/DIV
 Current (I_{ID})

MOSFET : STH33N20

Figure 4 : Turn-off of the Intrinsic Diode.

Time scale : 1 μ s/DIV
 V_{DS} : 50V/DIV
 I_D : 10A/DIV

Intrinsic
 Diode : 10A/DIV
 Current (I_{ID})

MOSFET : STH33N20

Another advantage of inductances L1 and L2 in the circuit is that they limit the build up of current during fault conditions such as simultaneous conduction of the two devices.

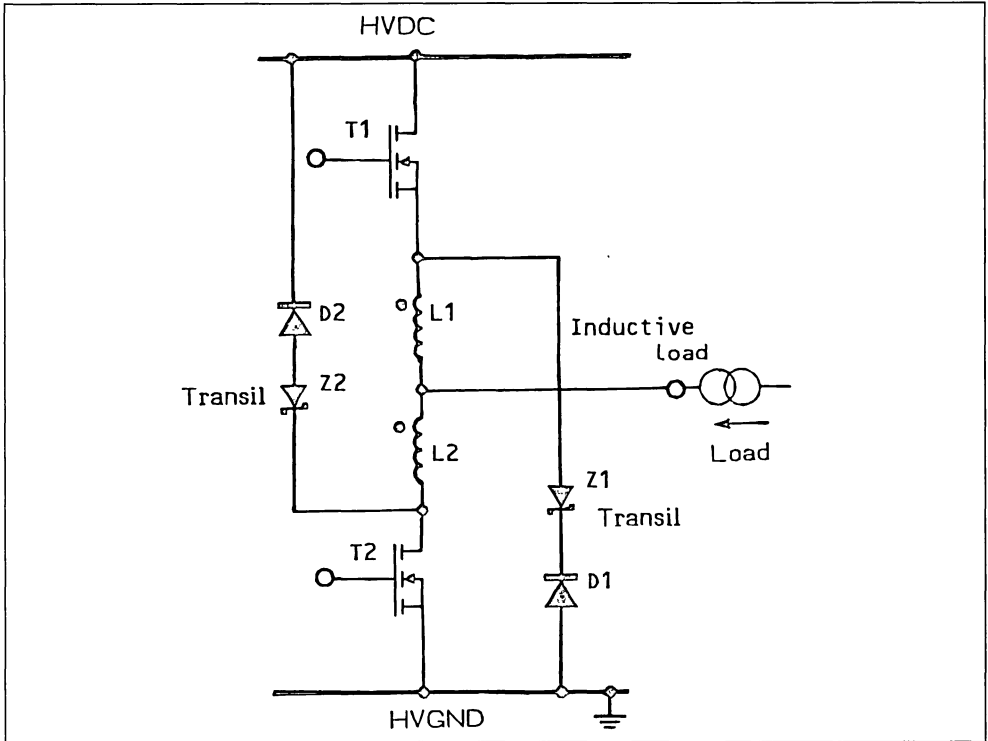
L1 and L2 must be chosen such that their inductances are big enough to prevent intrinsic diode reverse recovery problems hence reduce losses. They must be small enough to allow current to transfer from the freewheeling diodes D2 and D1 to the intrinsic MOSFET diodes in T1 and T2 such that the average current passing through the external diode and zener or transil is low.

b) SOLUTION WITH MUTUALLY COUPLED INDUCTORS

Inductors L1 and L2 can be mutually coupled as shown in figure 5. Coupling L1 and L2 doubles the

inductance between transistors T1 and T2 (SGSP477), thus reducing the reverse recovery problem of the intrinsic diode as the rate of change of current is reduced. Coupling, therefore, saves the cost of one core and less windings are necessary to provide the same degree of protection as in the case of uncoupled inductors. The voltage and current waveforms of the MOSFETs and their intrinsic diodes for this solution are similar to that obtained with solution (a).

Figure 5 : Bridge-leg with Mutual Inductors.



C) SOLUTION WITH SATURABLE INDUCTORS

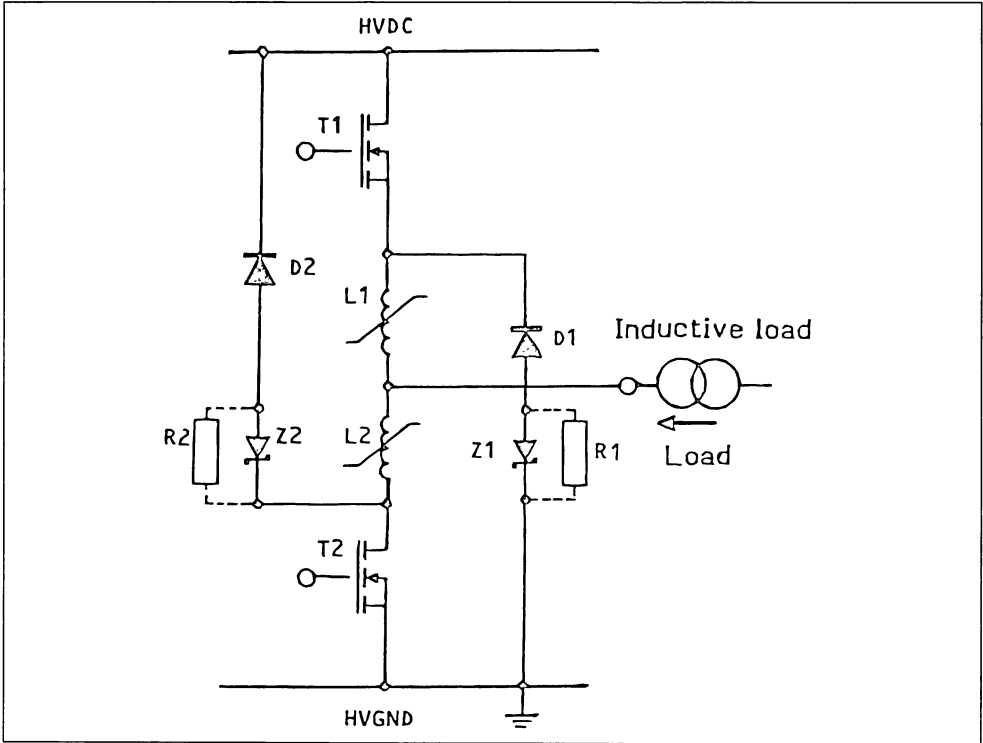
Saturable inductors such as toroids with a few turns can be used in the bridge configuration shown in figure 6. Saturable inductors are better suited than non-saturable inductors in so much as they can be used to limit the reverse recovery of the intrinsic diode to an almost negligible level. The saturable inductor is designed to saturate after the intrinsic diode has reverse recovered. Before saturation the inductor presents a high impedance and only a low magnetising current flows.

In figure 6, it is assumed that T1 and T2 are blocked and the intrinsic diode of T1 is conducting. If T2 is now turned-on, the current in the intrinsic diode decreases rapidly since inductor L1 is saturated until this current reverses resulting in negative volts-seconds across the inductor which thus desaturates. The inductor thus presents a high impedance while the current through it is equal to or less than the magnetising current. The intrinsic MOSFET diode

begins to reverse recover as the current through it becomes negative. The inductor is designed not to saturate for a period of at least $1\mu\text{s}$, thus enabling the reverse recovery of the intrinsic diode without excessive reverse recovery current. There is a certain degree of minority carrier recombination while the inductor is unsaturated which also reduces the maximum reverse recovery current, I_{RM} . The reverse recovery of the intrinsic diode can be seen in figure 7.

While T2 is conducting the load current inductor L2 is saturated. When T2 turns-off the MOSFET current transfers to diode D2. The free-wheeling current path through the intrinsic diode of T1 has a high impedance due to L1 being unsaturated. Consequently the build-up of current through the intrinsic diode of T1 is slow until this current reaches a value equal to the magnetising current, I_{mag} , of inductor L1 which then saturates. This effect can be clearly seen in figure 8.

Figure 6 : Bridge-leg with Saturable Inductors.



The turn-on of the MOSFET in the solution with saturable inductors (shown in figure 6) is illustrated in figure 9. It can be seen that the MOSFET losses are negligible, since the saturable inductor in series with the MOSFET that turns-on, limits the rate of rise of current while it is unsaturated. Figure 9 also illustrates that the reverse recovery of the intrinsic diode of the free wheeling MOSFET is also limited..

In the bridge-leg with saturable inductors (figure 6), if transils (Z1 and Z2) and resistors (R1 and R2) are removed, the external free-wheeling diodes have to be of high current rating as they conduct all the load current until the saturation of L1 and L2. Subsequently the external diode shares part of the free-wheeling current with the intrinsic diode. It is advantageous to reduce the current through the external free-wheel diodes D1 and D2 as rapidly as possible for the following reasons :

1. If D1 and D2 conduct for a small fraction of the maximum free-wheeling duty cycle, then their power rating is substantially reduced.
2. If the free wheeling current through the external diode D1 or D2 is reduced rapidly, the inductor in series (L1 or L2) is no longer saturated. At the consecutive turn-on of T1, L1 presents a high impedance thus performing a turn-on snubber function. Transistor turn-on losses are thus minimised particularly for inductive loads.
3. Output short-circuit protection is also enhanced if the inductors are unsaturated prior to transistor turn-on.

The current through the external free-wheeling diodes can be reduced rapidly by increasing the rate of release of inductor stored energy by transils (Z1 and Z2) and/or resistors (R1 and R2) as shown in figure 6.

Figure 7 : Reverse Recovery of Intrinsic Diode using Saturable Inductors in the Configuration of Figure 6.

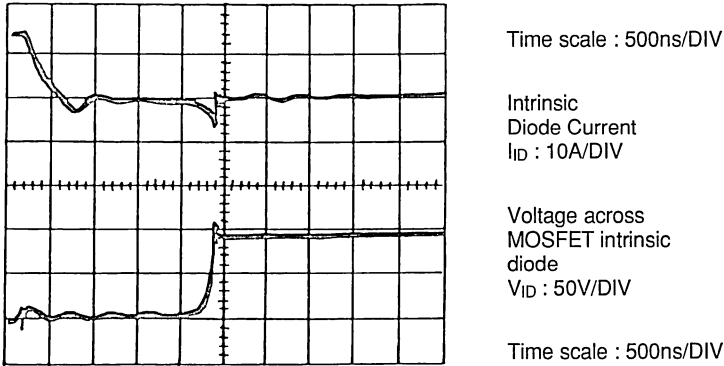


Figure 8 : Transfer of Current to Intrinsic Diode using Saturable Inductors in the Configuration of Figure 6.

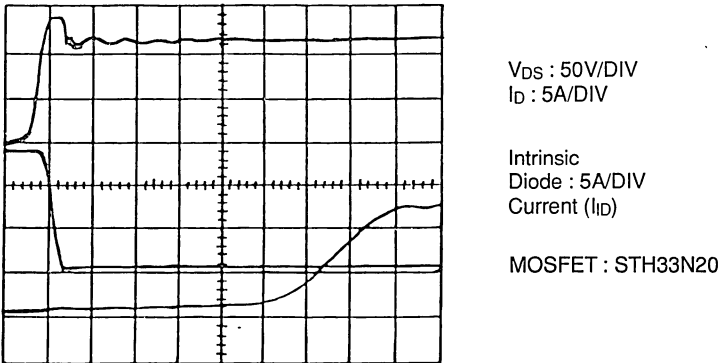


Figure 9 : Turn-on of the MOSFET in the Configuration with Saturable Inductors.
 (The turn-on snubber and the intrinsic diode reverse recovery actions are illustrated).

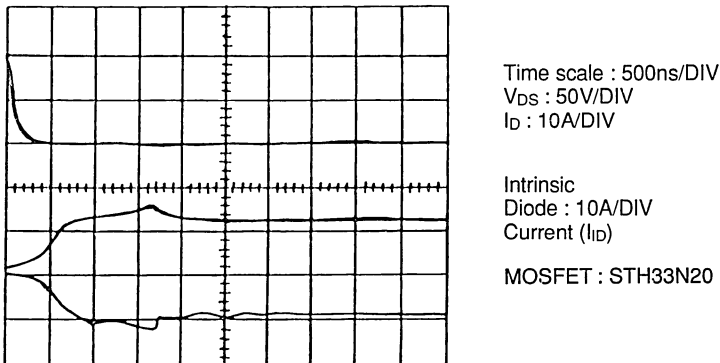


Table 1 : Advantages and Disadvantages of Solutions for limiting Reverse Recovery Current in the Intrinsic MOSFET Diode.

Sol.	Type of Protection Used	Advantages	Disadvantages
a)	Unsaturation Inductors	<ul style="list-style-type: none"> - Reduction of turn-on losses. - Controlled di/dt at turn-on. - Controlled reverse recovery of intrinsic diode. 	<ul style="list-style-type: none"> - In order to use low current rated freewheeling diodes, transient diodes have to be used increasing the voltage rating of the MOSFETs in the circuit.
b)	Unsaturation Mutual Inductances	<ul style="list-style-type: none"> - Smaller and less expensive than two inductors since only one coupled inductor. - As above. 	<ul style="list-style-type: none"> - As above.
c)	Saturable Inductors	<ul style="list-style-type: none"> - Negligible turn-on losses. - Negligible intrinsic MOSFET diode reverse recovery losses. - Controlled di/dt turn-on. 	<ul style="list-style-type: none"> - As above.

COMPARISON OF USE OF INTRINSIC MOSFET DIODE WITH ALTERNATIVE SOLUTION

Figure 10 illustrates three bridge-leg configurations that can be used with MOSFETs when switching inductive loads. Figure 10a) illustrates a bridge-leg which uses the intrinsic diode of a classical MOSFET having a reverse recovery in the order of a microsecond. The same configuration can be used with a lifetime controlled MOSFET which has an intrinsic diode having a reverse recovery time around 250ns. An asymmetrical bridge-leg illustrated in figure 10b), is similar to the above mentioned solutions permitting the use of the intrinsic diode. The configuration illustrated in figure 10c) has series

"blocking" diodes which prevent conduction of the intrinsic MOSFET diodes and thus avoid reverse recovery problems associated with the slow intrinsic diodes. In this configuration fast recovery epitaxial diodes are used as external free wheeling diodes.

Tests were performed using 500V, 0.6 ohm at 25°C classical STW12NA50 and lifetime controlled MOSFETs in the bridge-leg illustrated in figure 10a). Experimentally obtained losses within the diode and the MOSFET at turn-on are presented in figure 11. The solution enabling the use of the intrinsic diode without reverse recovery problems (figure 10b) has practically no losses due to reverse recovery of the intrinsic diode.

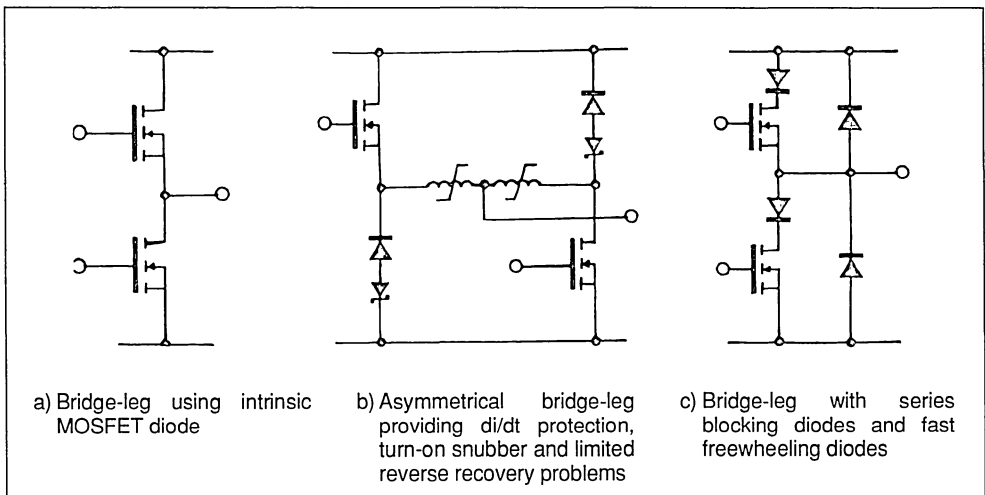
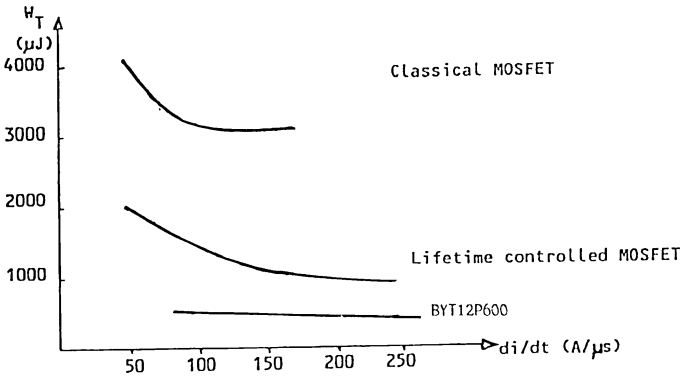
Figure 10 : Bridge-leg Configurations.

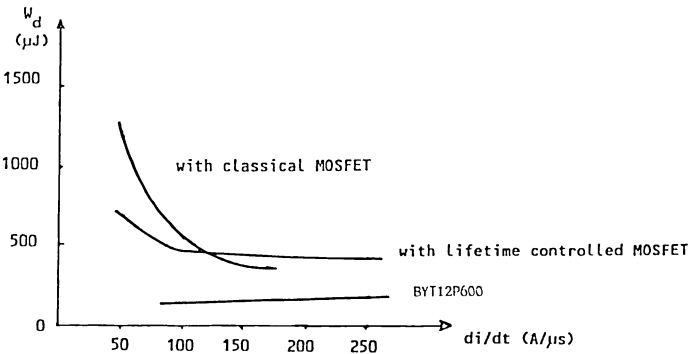
Figure 11 : Turn-on Losses in a Bridge-leg.

Turn-on Losses in the MOSFET



a) Turn-on losses in the MOSFET when switching 10A inductive load current on 400V_{DC} rail as a function of the rate of change of MOSFET drain current (di_D/dt)

Reverse Recovery Losses in the Diode



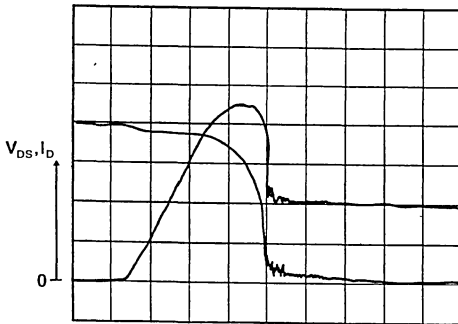
b) Reverse recovery losses in the freewheeling diode when switching 10A inductive load current on 400V_{DC} rail as a function of the rate of change of freewheeling diode current (di_{FD}/dt) during diode turn-off.

Figure 12 : Turn-on Illustrations of the MOSFET Drain to Source Voltage (V_{DS}) and Current (I_D) at Turn-on of the Transistor Limited to 100A/ μ s.



a) Classical MOSFET
(500V, 0.6 ohm)
STW12NA50
Diode losses = 540 μ J
MOSFET losses = 3200 μ J

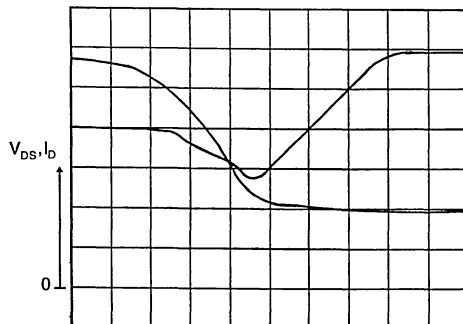
V_{DS} MOSFET drain to source voltage
100V/DIV
 I_D Drain current
5A/DIV
Time 200ns/DIV



b) Lifetime controlled MOSFET
(500V, 0.6 ohm)

Diode losses = 460 μ J
MOSFET losses = 1600 μ J

V_{DS} 100V/DIV
 I_D 5A/DIV
Time 100ns/DIV



c) External fast diode
BYT12P-600

Diode losses = 130 μ J
MOSFET losses = 560 μ J

V_{DS} 100V/DIV
 I_D 5A/DIV
Time 50ns/DIV

It can be seen that due to the slow intrinsic diode of the classical MOSFET, turn-on losses are twice that with a lifetime controlled MOSFET. With external

fast freewheeling diodes losses are only 20% of the losses in the classical MOSFET.

CONCLUSION

Reverse recovery of the intrinsic MOSFET diode has been investigated. Losses caused by slow intrinsic diode recovery for the classical MOSFET have been compared with losses using lifetime controlled MOSFETs in a bridge-leg and losses using fast external freewheeling diodes. It has been shown that turn-on losses in a bridge-leg using classical MOSFETs are five times greater than losses in bridge-legs with fast external freewheeling diodes and two times greater than losses in bridge-legs using lifetime controlled MOSFETs.

By using different types of inductors (such as saturable inductors) in bridge-legs it has been shown that negligible turn-on losses can be achieved as reverse recovery of the intrinsic MOSFET diode can

be limited. Practical results confirm that by using saturable inductors astutely in bridge-legs, it is possible to use the intrinsic diode of the classical MOSFET in high frequency inductive load switching applications with negligible turn-on losses.

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MODULAR DESIGN FOR MULTI-OUTPUT SMPS WITH SYNCHRONOUS POST REGULATION

by L. Wuidart

ABSTRACT

This paper proposes a modular way of designing multiple output SMPS. A Synchronous Post Regulator, (SPR), circuit is described in detail. This circuit is able to post-regulate both flyback and forward outputs and has built-in protection features.

An asymmetrical half bridge converter working in flyback mode was made using two independent modular SPR outputs.

A comparison of the resulting operation is made between this modular SPR circuit and an equivalent conventional SMPS with two outputs.

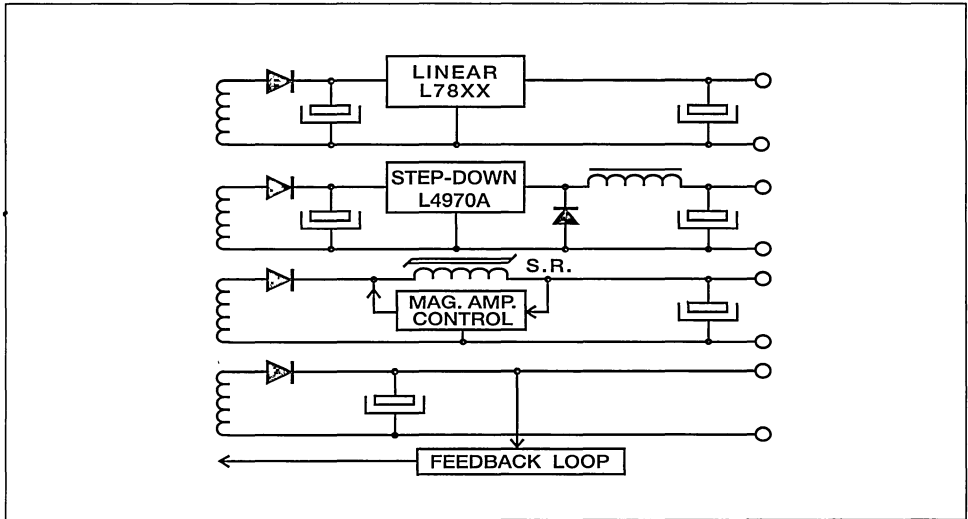
INTRODUCTION

Usually Switch Mode Power Supplies, (SMPS), use a transformer as galvanic insulation between the primary source, which can be the rectified mains or a battery, and the secondary low voltage d.c. outputs.

A particular difficulty that power supply designers often encounter is: how to regulate several output voltages, independently loaded, but having a common duty cycle fixed by the power level switched in the primary.

For this reason a compromise between cost and performance of the solutions available must be made by the designer. These solutions are outlined in figure 1a, which shows the secondary side of a multi-output flyback converter.

Figure 1A : Post regulators review in a multi-output flyback:
 - L78XX linear (<1A): cost effective but low efficiency.
 - Step down converter L497XA (3A->8A): High precision output voltage with additional LC filter and rectifier.
 - Mag. amp. circuit (>8A): High efficiency but no "open load" regulation.



REVIEW OF EXISTING POST REGULATORS

The linear post regulator is probably the most popular solution for low current applications (<1A). But this cost effective approach suffers from high dissipation and poor efficiency.

For the higher current range, >8A, the magnetic amplifier still has a good overall performance. The magnetic amplifier circuit has a high efficiency and the ability to handle high output currents. But the difficulty in implementing effective current limiting and the poor regulation output performance (open load) has often restricted the use of this circuit.

For the medium current range, 3A to 8A, the housing size and especially the cost of a magnetic amplifier core are no longer attractive. In this range of application, high

efficiency step down converters, for example the L4970A family can be used as non-synchronized post regulators. This type of solution provides a high precision output voltage and is well suited to distributed power supply concept [1]. However, this step-down topology always requires additional components, i.e. an LC filter and rectifier.

A synchronous semiconductor switch has many advantages over a comparable saturable reactor, particularly in medium power applications. Indeed, a semiconductor switch gives excellent load regulation performance. Control and protection functions such as over current limiting, short-circuit shutdown, remote on/off, etc. are easily implemented in a semiconductor switch. This type of synchronous post regulator allows the construction of a multi-output SMPS in a completely modular way, see Fig. 1b.

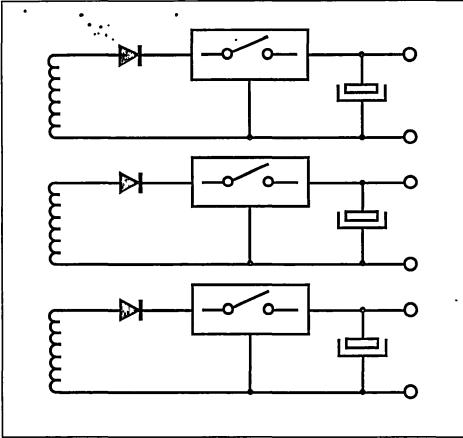


Figure 1b : SPR modular multi-output SMPS design: Each output can be designed as an independent single output channel delivering

$$P_{out} = V_{out} \times I_{out}$$

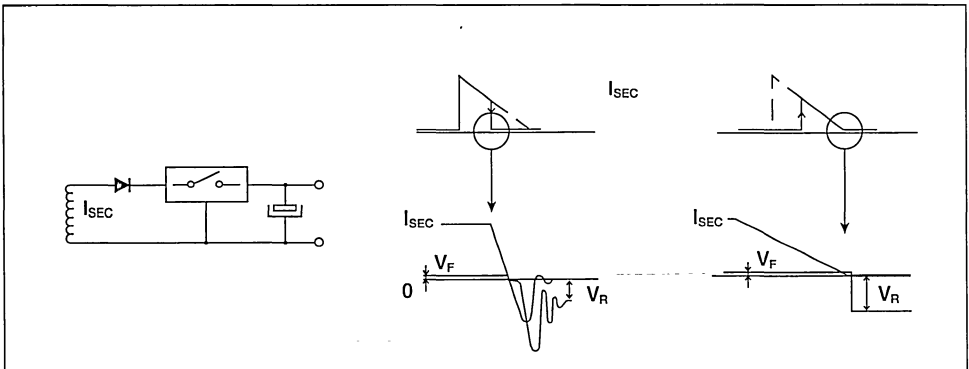
SYNCHRONOUS POST REGULATOR CONTROL PRINCIPLES

The saturable reactor of a magnetic amplifier used in an SMPS output stage (Fig.1a) can be replaced by a driven switch in series with the rectifier. This configuration has given rise to the term Synchronous Post Regulator, SPR. In this configuration a voltage controlled PWM circuit synchronized with the switching frequency controls the turn-on delay of the power switch. The circuit is designed so that zero turn-on delay corresponds to maximum load level.

The basic reason for using delayed turn-on rather than delayed turn-off for controlling the output is because interrupting the flow of current through the secondary parasitic stray inductance would produce over-voltages across the switch (fig.2). This would require a dissipative clamping snubber to protect the SPR against potentially damaging over-voltages.

Delayed turn-on control is well suited to discontinuous mode flyback operation because zero turn-off current avoids recovery losses in the series rectifier.

Figure 2 : SPR control principle : "delayed turn-on rather than delayed turn-off" in order to avoid over-voltages across the switch due to sharp current changes in the parasitic stray inductance.

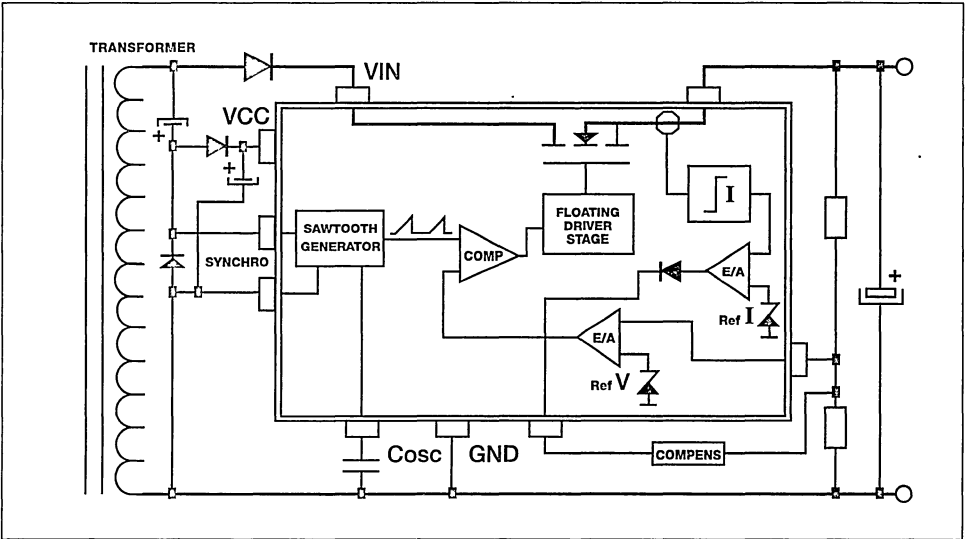


CIRCUIT DESCRIPTION

The block diagram in figure 3 shows the principle of operation. The output voltage of

the transformer is pulse width modulated by a power MOSFET switch. The efficiency of the switch will depend on the $R_{DS(on)}$ of the Power MOSFET.

Figure 3: SPR block diagram : A voltage mode PWM synchronized with the switching frequency controls the turn-on delay of the power MOS.

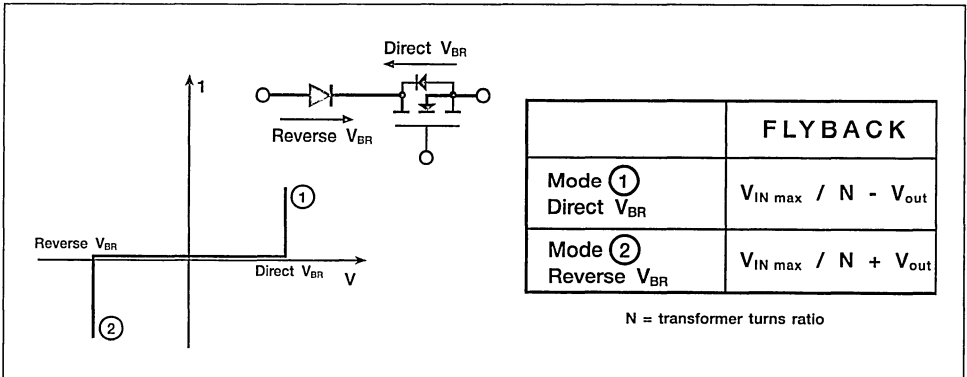


A series rectifier is necessary to avoid reverse conduction through the power MOSFET body diode during primary on-time (reverse mode : see fig.4). The

reverse breakdown voltage rating of this rectifier is the same as for a conventional flyback :

$$(V_{in\ max}/N)+V_{out}$$

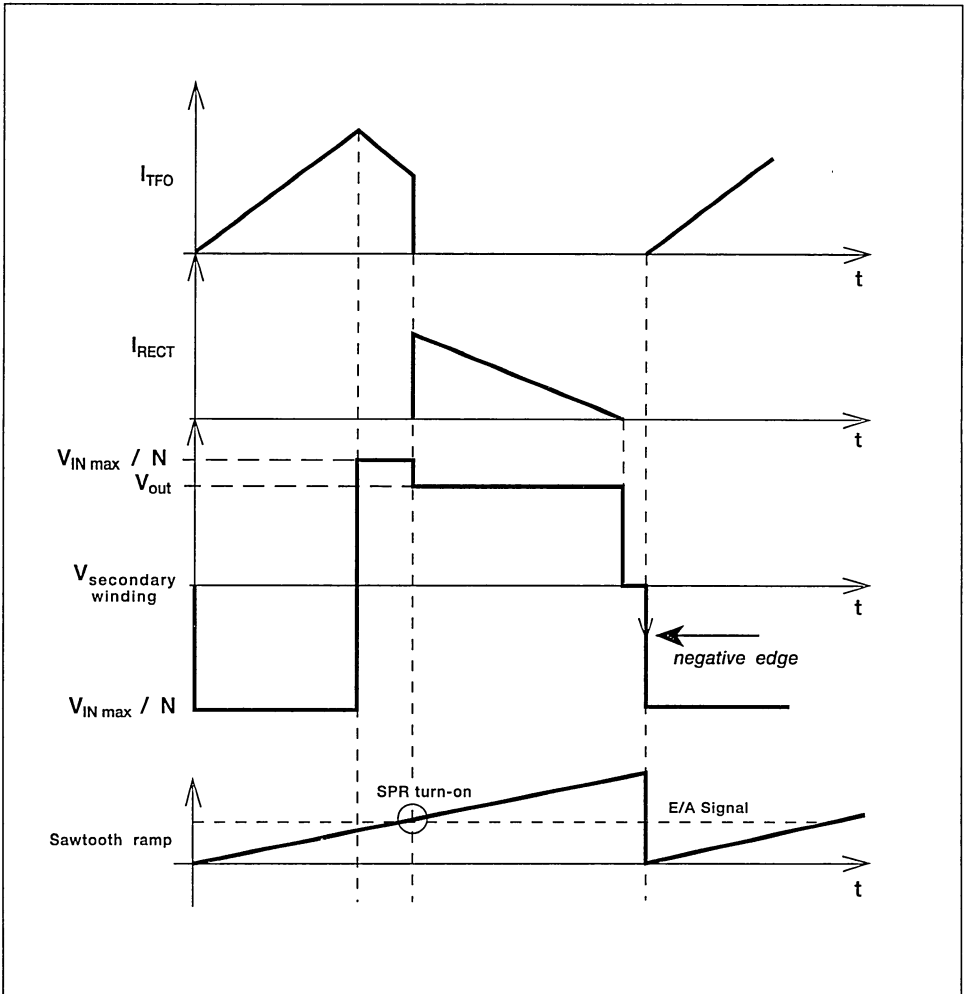
Figure 4: Minimum breakdown voltage ratings required for the power MOSFET (mode 1 : direct V_{BR}) and the series rectifier (mode 2 : reverse V_{BR})



When the SPR is kept off during the flyback direct mode (fig.4), the power MOSFET has to withstand a voltage of $(V_{in,max}/N) - V_{out}$. In practice, a Power MOSFET with a 50V breakdown voltage is enough for both 5V and 15V flyback outputs. Low voltage drops can be achieved by using a power MOSFETs in the isolated ISOWATT218 package such as STH80N05FI ($R_{DSon} = 0.012$ Ohms).

The output voltage error signal controls the delay width before turning the power MOSFET on. The PWM sawtooth ramp is synchronized with the negative edge of the secondary winding voltage (fig.5). This means that 100% of the available flyback current can be transferred to the load without any propagation delay due to the control loop.

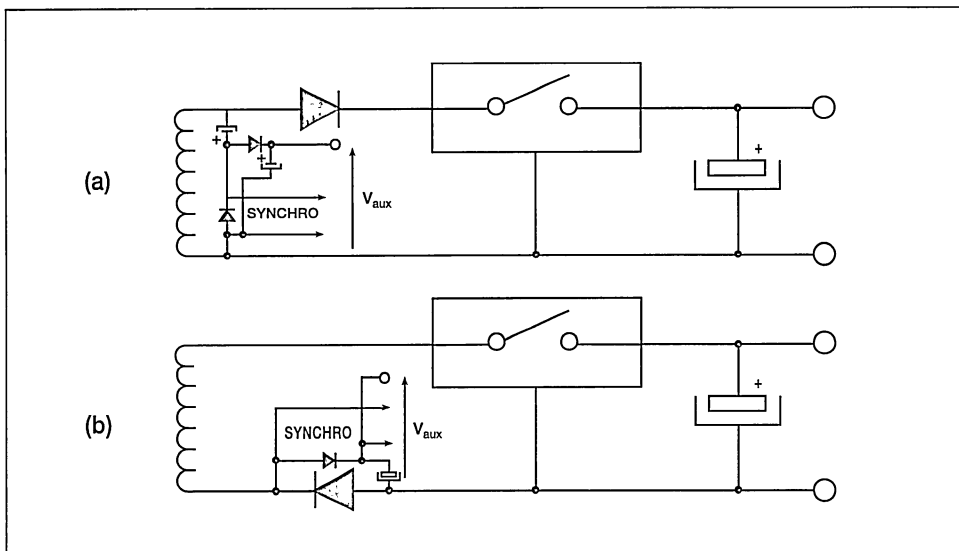
Figure 5 : Synchronization of the PWM sawtooth ramp with the negative edge of the secondary winding voltage allows 100% of the flyback energy to be transferred to the load.



As the power MOSFET has to be driven properly in "high side configuration", the gate driver supply requires a higher voltage than the output. A suitable auxiliary supply can be made without an additional transformer winding. One possibility is to build a voltage doubler with two signal diodes and two small capacitors (fig.6a).

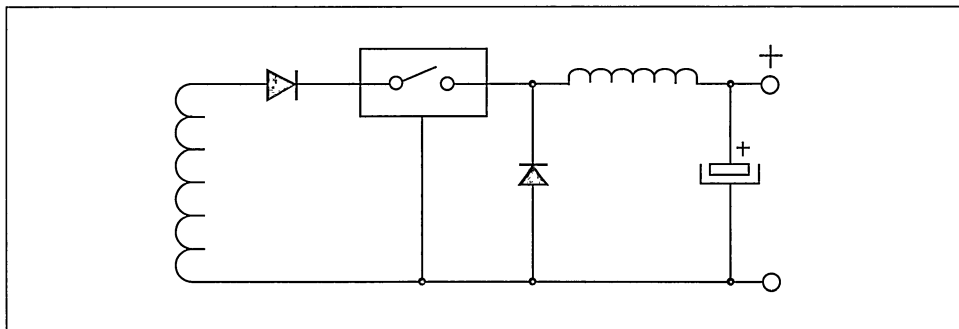
Another method can be to put the flyback rectifier in the negative output rail. Then use a signal diode/capacitor network across the power rectifier which will provide a supply voltage with a maximum output $(V_{out} + V_{in}/N)$ (fig.6b).

Figure 6 : An auxiliary supply, (V_{aux}), higher than the output voltage can be made in flyback mode in two ways:
 6a : Voltage doubler circuit
 6b : Peak voltage detection circuit across the rectifier put in the negative rail



This SPR circuit is also compatible with forward converters (fig.7).

Figure 7: The same Synchronous Post Regulator circuit can be used in forward configuration.

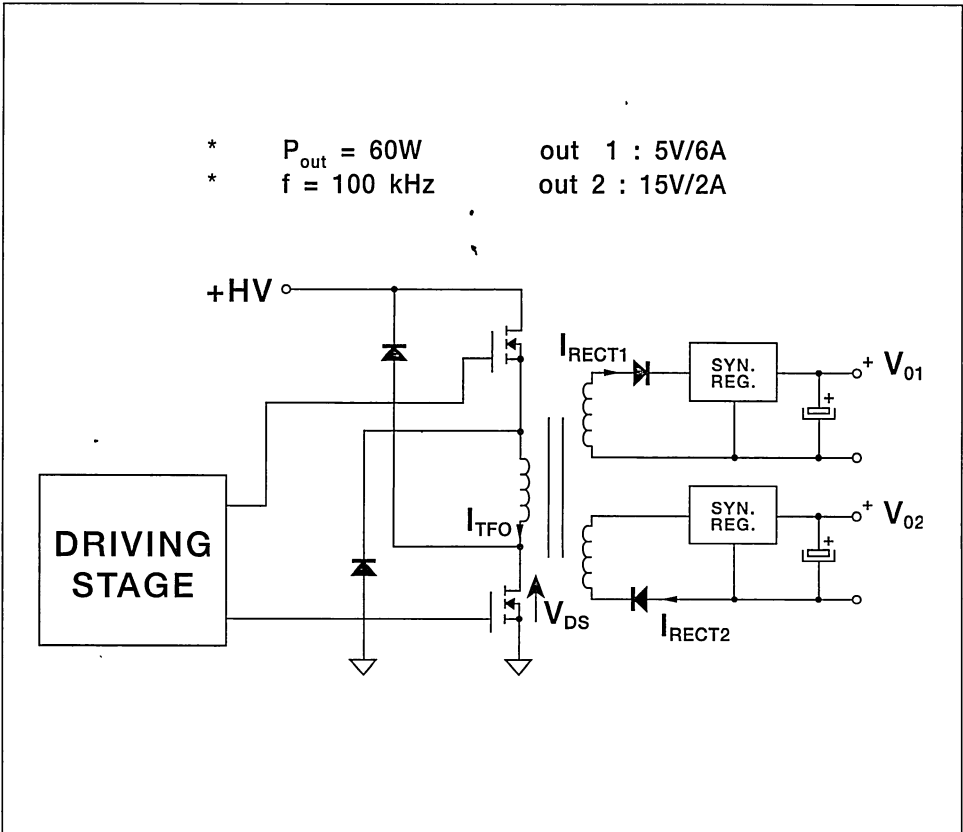


PRACTICAL EXAMPLE

A 60W output asymmetrical half-bridge flyback working in discontinuous mode at 100kHz has been designed to illustrate the

operation of this type of power supply. The converter has two SPR outputs which are completely independent from the primary circuit. Explicitly, there is no feedback loop from secondary to primary side (fig.8).

Figure 8: Asymmetrical half bridge flyback with two Synchronous Post Regulated outputs. There is no feedback loop from secondary to primary.



DOUBLE VERSUS SINGLE SWITCH FLYBACK

Earlier applications of some ten years ago avoided the asymmetrical half-bridge configuration for flyback converters because the base drive of the high-side bipolar switch was very complex. The circuit has the advantage of replacing one

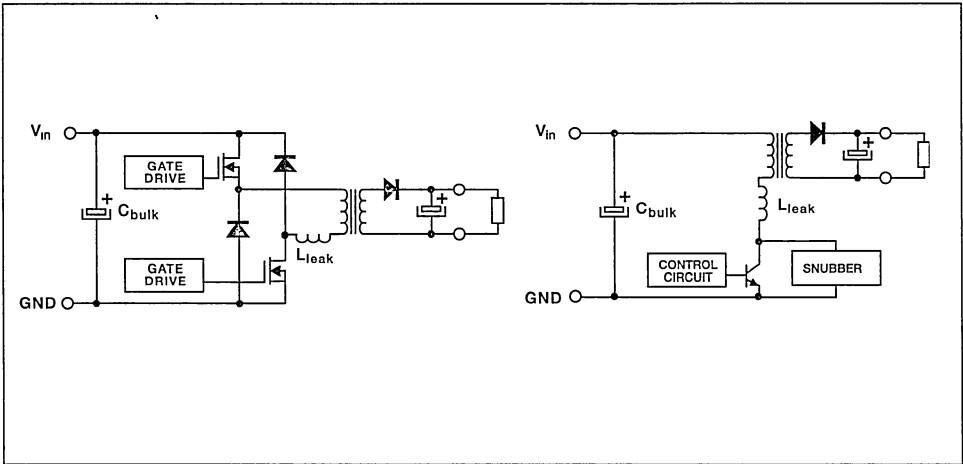
1000V switch by two 500V switches. Now it is possible for such an asymmetrical structure to be reconsidered with great interest for 220V AC off-line applications. Indeed, two 500V MOSFETs such as the IRF830FI (isolated ISOWATT220 package) only require a very simple gate driver and, at today's prices, are cost effective (fig.9).

This type of converter structure improves efficiency. Usually, a single switch flyback requires an additional dissipative snubber network to dump the transformer leakage inductance L_{leak} energy (up to 15% of the total output power). In the asymmetrical half-bridge, the energy stored in the

transformer leakage inductance is returned to the reservoir capacitor (fig.10). The two demagnetisation diodes D_1 and D_2 (Axial BYT03-400) provide a simple non-dissipative systematic way to clamp the voltage across the switch to the input line value V_{in} .

Figure10: Single versus double switch flyback:

The energy stored in the transformer leakage inductance, (L_{leak}), of the double switch flyback is returned to reservoir capacitor C_{bulk} avoiding additional dissipative snubber network.



The asymmetrical half-bridge flyback allows the use of SPR without any additional transformer winding and/or components. All the energy stored in the primary inductance which is not transferred to the secondary side is automatically returned to the reservoir capacitor C_{bulk} through the two demagnetisation diodes.

In this way, a completely modular design approach can be used to separate primary and secondary sides:

*On the primary side, (fig.9), the input line voltage is regulated through a simple current mode control, using the low cost UC3845 control IC. For a given line input voltage, current mode control determines

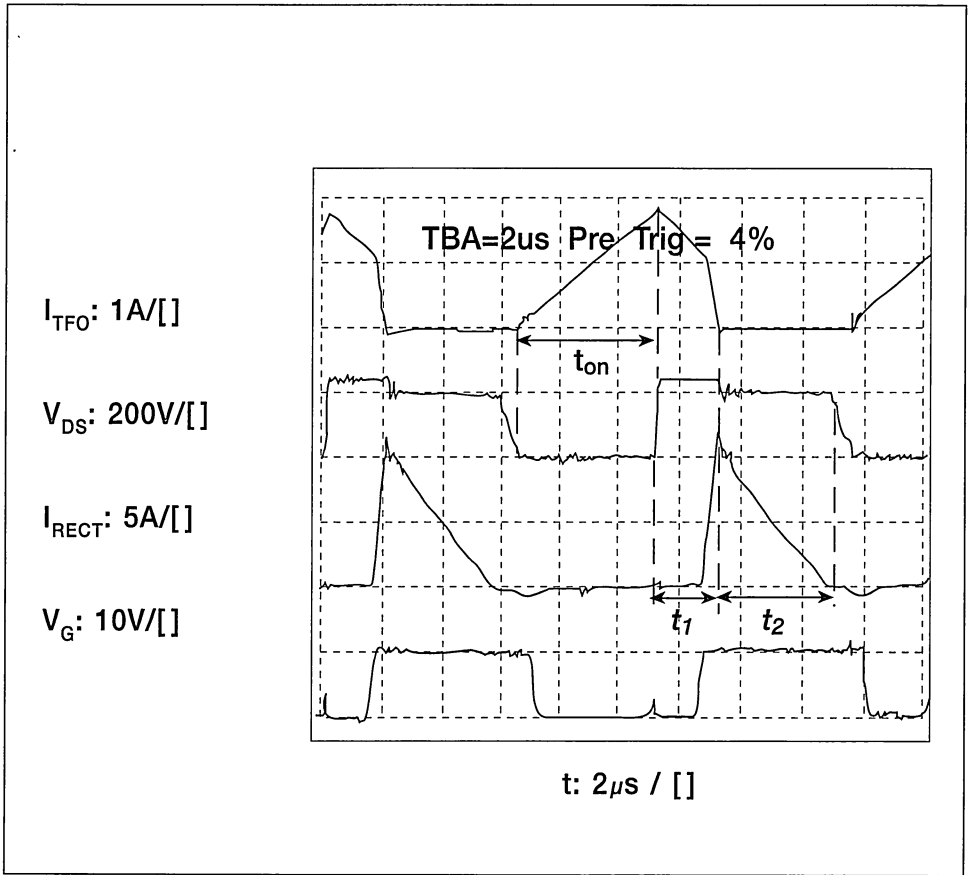
the maximum duty cycle available for all the output channels. The weak point of such a simple system is the poor efficiency at low load level.

*On the secondary side, the SPR only compensates for any load variations since the complete SPR feedback loop is looking for the output voltage variations. So, each SPR output can be designed as an independent self-protected module (fig.1b).

UNDERSTANDING PRACTICAL WAVEFORMS

Practical waveforms of an SPR used in an asymmetrical half-bridge are represented in the oscillogram of Fig.11.

Figure 11: Practical waveforms of a Synchronous Post Regulator used in the asymmetrical half-bridge flyback. Parameters are defined in the diagram of Fig. 8. V_G is the gate to source voltage of the SPR power MOSFET.



During the on-time, (t_{on}), the current in the transformer primary winding, I_{tfo} , increases with a slope of typically V_{in}/L_p , L_p being the transformer primary winding inductance.

SPR off: interval t_1

When the primary power MOSFETs are turned off, the energy is first returned to reservoir capacitor through demagnetisation diodes, the output being open since the SPR is off. During this period (t_1) the primary current I_{tfo} is

freewheeling with a decreasing slope of $(V_{in}+2V_r)/L_p$ and a voltage of V_{in} is applied across each power MOSFET.

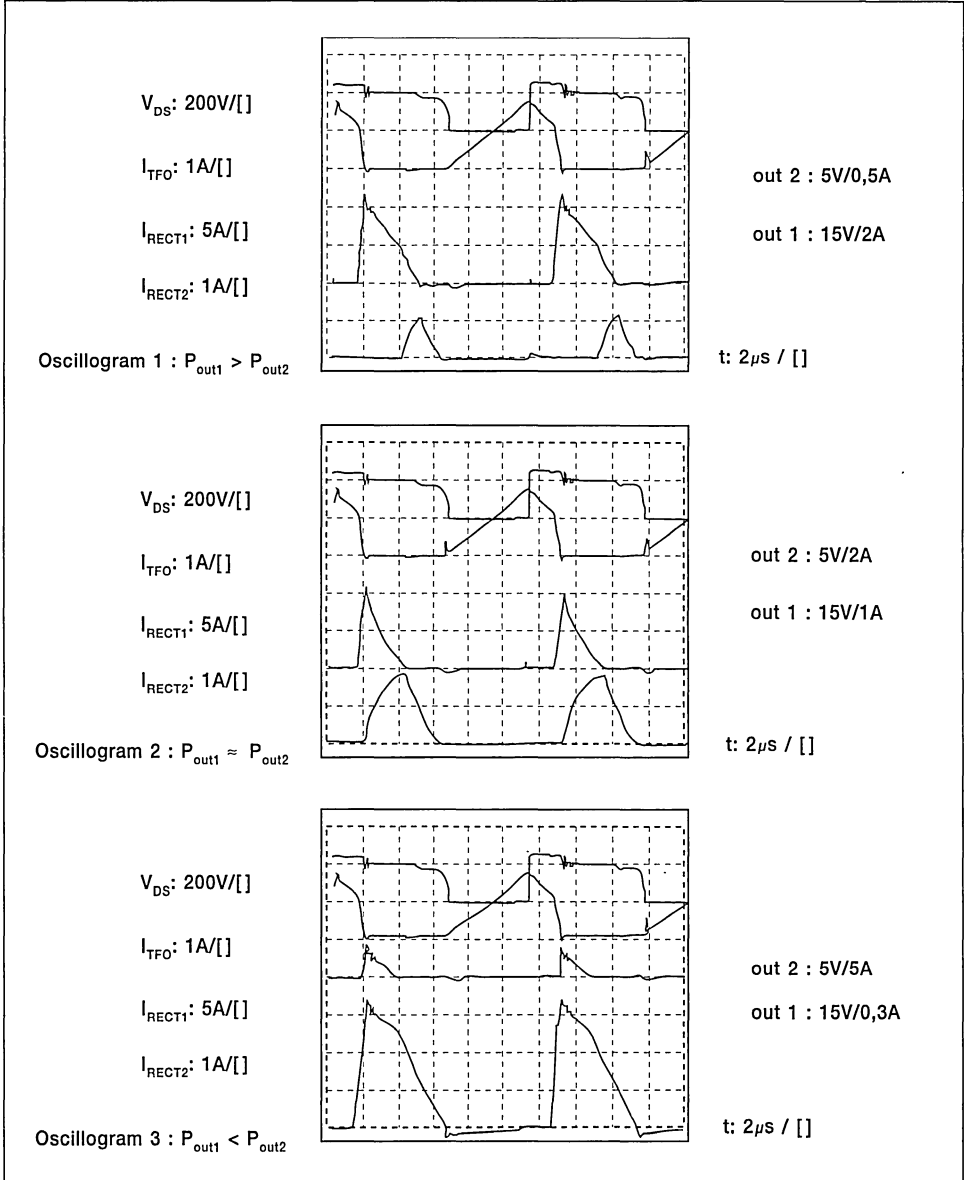
SPR on: interval t_2

As soon as the SPR turns on, energy is transferred from primary to secondary with a corresponding primary current slope of $(V_{in}-NV_0)/L_{leak}$. The rectifier current I_{rect} decreases to zero as in a standard discontinuous flyback circuit.

TWO SPR OUTPUT WAVEFORMS

The following oscillograms (Fig. 12) were taken at 3 different output power levels:

Figure 12: Oscillograms of the 2 Synchronous Post Regulated outputs used in the asymmetrical half-bridge flyback.



Whatever the power balance between the outputs, output 1 is always the first to turn the SPR on. This sequence occurs because of the unbalanced values of each primary reflected output voltage ($N_i V_{oi}$). The primary winding of the transformer has 74 turns. Three turns on the secondary give 5V on output 2, and 6 turns are enough to give 15V on output 1. Output 1, therefore, has a greater reflected voltage than output 2 :

$$N_1 \cdot V_{o1} > N_2 \cdot V_{o2}$$

Serial voltage drops are included in V_{oi} , N_1 and N_2 being the turns ratios of output 1 and output 2, to the primary, respectively.

This ratio of secondary winding turns, which is non-linearly connected to the output voltages, can be realized only by using SPR outputs. This is not possible in conventional flyback circuits.

EFFECTS OF UNBALANCED $N_i V_{oi}$

Assuming that $N_1 V_{o1} > N_2 V_{o2}$ and $(N_1 V_{o1}/N_2 V_{o2}) = C$, then:

1.The lowest reflected output voltage ($N_2 V_{o2}$) has the maximum output power capability.

$$P_{out2\ max} = P_{out1\ max} \times C \text{ with } C > 1$$

2.The highest reflected voltage ($N_1 V_{o1}$) has a degraded load regulation effect.

Those two effects have also been detected in our example. In this case ,

$$(N_1 V_{o1}/N_2 V_{o2}) = 197/160 \approx 1.2$$

The maximum measured output power capability for each secondary channel, the other channel being open loaded:

$$\begin{aligned} P_{out2\ max} &= 60W \text{ (5V output)} \\ \text{and } P_{out1\ max} &= 49W \text{ (15V output)} \end{aligned}$$

With the other output 50% loaded, the load regulation for a 0 --> 100% load variation was measured as:

$$\begin{aligned} \text{output 1: } 15V &\text{ --> } +/- 0.45\% \\ \text{output 2: } 5V &\text{ --> } +/- 0.1\% \end{aligned}$$

SMPS DESIGN CONSEQUENCES

The use of an SPR circuit facilitates SMPS design by avoiding several difficult points commonly met in a typical multi-output flyback.

* Power transformer

- Even if a high frequency transformer gives high volts per turn, the secondary turns adjustment is more flexible than in the conventional flyback. In our example, 3 turns for 5V, and 6 turns for 15V output.

- Tight coupling between secondary windings is not so critical anymore, since cross regulation effects between the different output channels are compensated by SPR circuits.

* Protection

A SPR circuit can perform effective output protection against overload, short-circuit and over-voltage since these functions are decentralized in each channel.

* Standard approval costs

The cost of the expensive UL/VDE approved opto-coupler in conventional secondary to primary feedback loops can be saved by using SPR modular approach. Moreover, any combination of any approved SPR module that complies with safety standards, makes approval procedures more rapid.

CONVENTIONAL VERSUS MODULAR APPROACH

Load and cross regulation performance between a conventional and an SPR modular flyback converter are compared in Fig. 13.

Figure 13: Comparison of load and cross regulation between the SPR modular flyback converter under test and a comparable conventional version.

$P_{out} = 60W$ at: $5V/6A$ $f = 100kHz$ and $15V/2A$		
	CONVENTIONAL	MODULAR
LOAD REGULATION 50% load on the other output - Reg. out. (0 -> 100% load) - Unreg. out. (50 -> 100% load)	$\pm 0,2\%$ $\pm 5\%$	$\pm 0,05\%$ $\pm 2\%$
CROSS REGULATION Influence on the indicated out (50% load) for a load variation from 20% to 100% on any other output - reg. out. - unreg. out.	$\pm 1\%$ $\pm 5\%$	nil $< \pm 2,5\%$

Better load and cross regulation are observed in the unregulated outputs of the modular approach. This is because the

maximum duty cycle in the modular approach is independent of the load.

CONCLUSION

In typical multi-output SMPS, a common design difficulty is to achieve tight regulation in auxiliary outputs, mainly because of leakage inductances between the power transformer windings but also because of the different forward voltage drops of rectifiers.

Also, high frequency transformer design gives high volts per turn, meaning more volts supplied than are actually required.

The proposed SPR circuit can easily compensate for the cross regulation effects and also efficiently protect each output. Furthermore, a secondary to primary feedback loop is not required when using this modular concept.

For medium current range the synchronous post regulator offers many advantages over the other comparable solutions. Decentralized control and protection functions can be easily implemented in an SPR circuit. An interesting application example is the tape video recorder SMPS. Here an SPR circuit can be directly interfaced with a microcontroller, programming the output voltage for proper motor control. Another diagnostic function could indicate a fault condition, over-temperature, short-circuit etc., to the microcontroller by an external status output signal.

The potential to integrate all those control functions into a monolithic IC, gives the SPR an additional advantage over other circuits. Each output can be effectively considered as an independent self-protected module. This modular design approach can dramatically reduce power supply development time.

REFERENCE

- [1] DATA SHEET L4970A, 10A switching regulator. Industrial and computer peripheral ICs DATA BOOK, 2nd Edition
- [2] R.D. Middlebrook: Topics in multiple - loop regulators and current - mode programming.
IEEE: PESC 1985

AN AUTOMATIC LINE VOLTAGE SWITCHING CIRCUIT

by Vajapeyam Sukumar
Thierry Castagnet

ABSTRACT

The voltages found in line sockets around the world vary widely. Power supply designers have, most often, overcome this problem by the use of a doubler/bridge switch that can double the 120V nominal line and simply rectify the 240V nominal voltage.

A two device solution (comprising an integrated circuit and a customized triac) that will adapt the power supply to various line voltages around the world is described in the following paper. This circuit replaces a manual switch and could also open special markets. Other advantages of this integrated circuit solution are ease of circuit design, lower power dissipation, a smaller component count and additional safety features.

INTRODUCTION - THE DOUBLER/BRIDGE CIRCUIT.

AC line voltages the world over can be divided into two main categories :

a) 120V nominal, 60Hz systems. Electronic equipment is usually designed to run in the

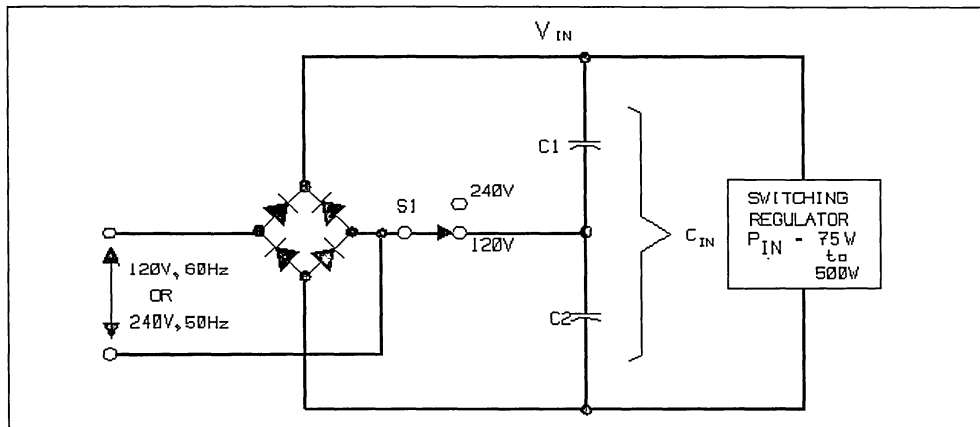
90V - 132V range.

b) 240V nominal, 50Hz systems. Equipment has to be designed to run in the 187V-264V range.

A good reference for the various line voltages around the world is found in [1].

Power supplies built to run off these voltages have to be either wide range input or must use a doubler/bridge circuit. The disadvantage of the wide range input scheme - that all components have to meet worst case current and voltage requirements - makes such a solution popular only at less than 75W power levels. The popular doubler/bridge circuit is shown in Fig. 1. When the AC input voltage is 120V nom. (doubler mode) the switch S1 is closed. During the positive half cycle of the input voltage capacitor C1 is charged. During the negative half cycle of the input voltage, capacitor C2 is charged to the peak line voltage. When the line voltage is 240V nom. (bridge mode), the switch S1 is open and the circuit works like a conventional bridge rectifier.

Figure 1. Schematic Diagram of a Doubler/Bridge Circuit.



APPLICATION NOTE

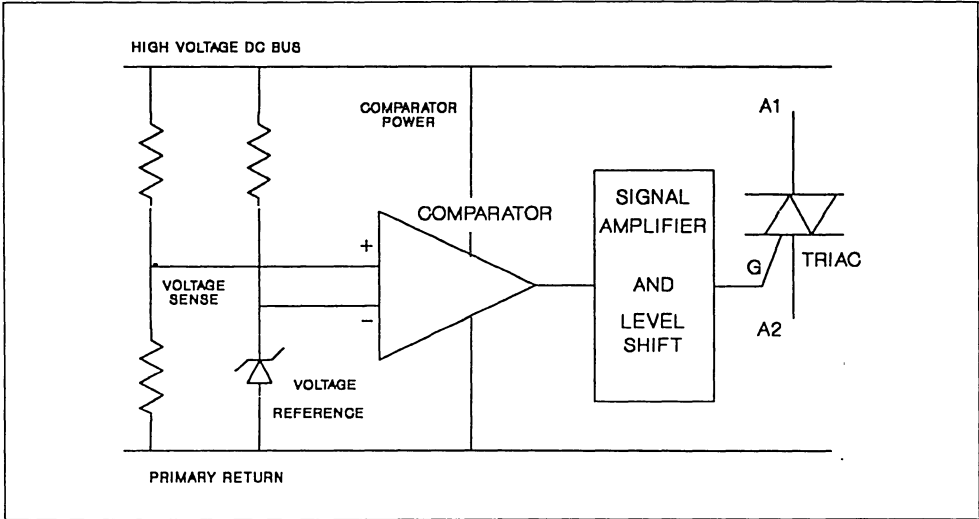
At power levels of over 500W, power factor correction circuits and three phase line input voltage circuits dominate. So, the automatic line voltage switching (AVS) circuit is used mostly in the 75W-500W power range.

The recent push to replace the mechanical switch S1 in Fig.1 with an automatic line voltage switching (AVS) circuit came from computer

manufacturers. They found that the small additional cost of the AVS circuit is less than the costs of power supply failures incurred by inadvertently positioning the switch in the wrong position.

While many of the early AVS designs used relays, the triacs, with their superior reliability, small size and low cost are now more popular.

Figure 2. Discrete AVS Circuit Block Diagram



DISCRETE AUTOMATIC VOLTAGE SWITCHING CIRCUIT

Figure 2 shows a diagram of the various blocks comprising a discrete implementation of the AVS circuit. The line voltage selection circuit can be divided into three main functions:

1. Detection of peak line input voltage. Various schemes use resistive or capacitive dividers to measure the voltage across C1 and C2.
2. Comparison with a reference voltage that is generated with the help of a zener diode. A simple comparator can be implemented with two small signal transistors.
3. Drive for the triac. If the circuit is to be in the doubler mode, then the output signal of the comparator is boosted to provide the

drive to turn the triac on. This interface circuitry can consist of a high voltage transistor and bias resistors.

DISCRETE VS INTEGRATED CIRCUIT AVS.

An IC based AVS circuit should be designed to overcome the disadvantages of the discrete solution that are listed below.

1. Power Dissipation.

This is critical because the entire supply current necessary for the operation of the AVS circuit comes from the high voltage bus. Every milliamperere of current saved in the sensing, comparison and drive circuitry increases the efficiency of the entire system.

$$P_D(\text{AVS}) = k \cdot (V_{AC})^2. \quad (1)$$

About 80% of the power lost in the AVS scheme

is in the gate drive to the triac. This means that a sensitive gate triac is the best candidate for the switch S1 in Figure 1.

Discrete AVS solutions usually use between 5W and 12W.

2. Immunity to Input Line Voltage Transients.

Most power supplies today are designed to meet IEEE 587 or similar line transient specifications. We must choose a triac that withstands these transient voltages without any triggering. So we have to make a compromise between low gate drive requirements (I_{GT}) and good static dv/dt immunity. The gate drive circuit of the triac must also be designed to reduce any parasitic voltages at the gate. The gate non-trigger voltage (V_{GD}) of most triacs is about 0.2V.

3. Effect of Line Sags and Surges.

Line voltages are generally considered to vary about $\pm 10\%$ from their nominal values. The 120V nominal can be as high as 132V and the 208V nom. can fall to 187V. Between 132Vac and 187Vac, there exists a window, in which we have to design the threshold voltage of the comparator in Fig. 2. Additional ('strife', etc.) test requirements can reduce this window to a smaller 140V to 170V. An analysis of worst case component tolerances is critical in AVS design.

Ultimately, however, there will always be line voltage waveforms that will fool an automatic voltage selection scheme. One can think of situations where, say, a large motor will pull the line voltage down below the threshold voltage during startup. A good AVS system will monitor the line voltage and protect the power supply. In some applications, the bridge mode (240V mode) is considered the fail safe mode and if the unit starts off in the bridge mode, it should not be able to change modes till the power is recycled.

SGS-THOMSON AVS10 SOLUTION.

We at SGS-THOMSON studied the possibility of an integrated circuit solution for this application. The cost constraints ruled out any exotic single chip solutions and forced us to opt for an 8 pin DIP IC for sensing and a TO-220 triac as the power switch. This IC+triac solution, called AVS10, also offers optimal protection against noise.

In order to maximize the design flexibility and reduce turn around time, we chose a semi-custom solution called ANACA. A 12V CMOS ANACA process used offers mixed analog/digital standard cell capability.

OPERATION OF THE AVS10 CIRCUIT

A typical application diagram for the AVS10 in a power supply is shown in Fig. 3.

Figure 3. AVS10 Application Schematic Diagram

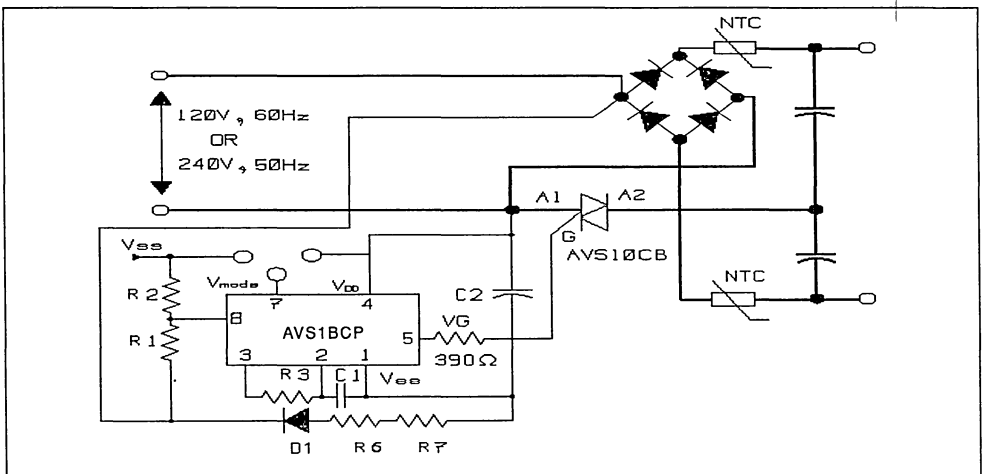
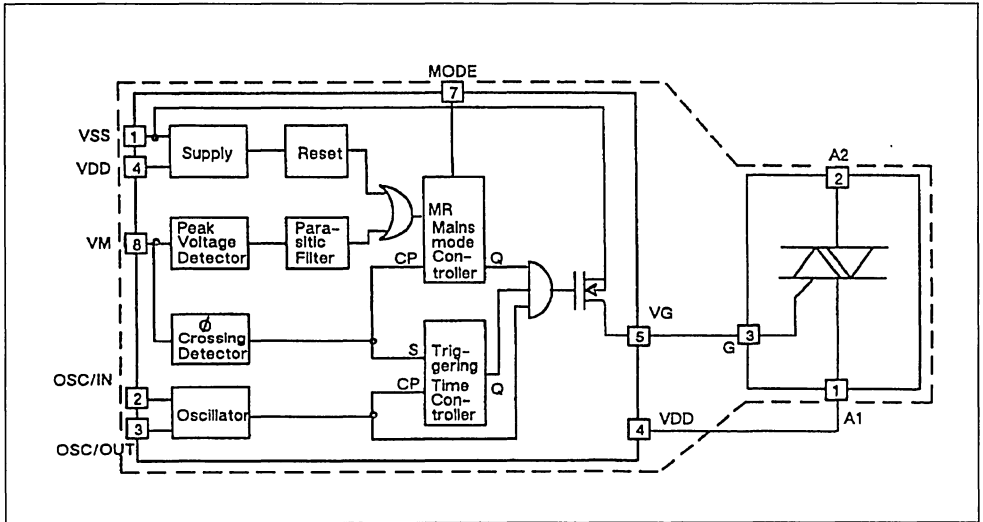


Figure 4. AVS10 Block Diagram



The series circuit of D1, R6, R7 and C2 provide power for the chip. Pin 1, Vss, is a shunt regulator that provides a -9V (nom.) output. R1 and R2 are resistive divider precision resistors that are a measure of the input line. The voltage at Pin 8 varies with the input line. Thus the voltage at Pin 8 is not only a measure of the peak input voltage, but it can also sense line voltage zero crossing. Pins 2 and 3 are inputs to an oscillator. The resistor R3 and C1 set the oscillator frequency. Pin 5 drives the gate of the triac through a 390Ω resistor. Pin 7 offers the user a choice of two different modes of operation. The block diagram of the IC is given in Fig. 4.

1. Decreased Power Dissipation.

Decreased power dissipation is an important advantage of the AVS10. While most discrete AVS schemes need 5W to 12W of power, the AVS10 uses about 2W. This performance is thanks to an innovative gate triggering scheme (Patent Pending). The gate current is made up of a pulse train that has a typical duration of around 23μs (45kHz±5%). The duty cycle of the pulses is typically 10%. The values of R2 and C3 in Fig. 3 are chosen to give us the pulse frequency.

2. Immunity To Voltage Transients.

The triac of the AVS10 is a sensitive gate triac

that is specified to remain off when subjected to dv/dt of 50V/μs. Circuit layout is critical in preventing false dv/dt turn on of the triac [2]. The IC of the AVS10 circuit has a built in digital filter that suppresses the effect of all spikes of less than 200μs duration.

3. Operating In The Failsafe Mode. $V_{mode} = V_{ss}$.

The mode pin on the AVS10 IC, Pin 7 determines the behavior of the circuit if it is turned on into a line surge/sag situation. If Pin 7 is tied to Vss (Pin 1), the AVS10 circuit is in a failsafe mode. This means that if the device is turned into a bridge mode, it will remain in the bridge mode, even if the voltage were to suddenly dip into the 110V range.

4. Operation In Reactive Mode. $V_{mode} = V_{DD}$.

If Pin 7, the mode pin, is tied to VDD, then the device will switch between bridge and doubler modes if the input voltage changes. If the 110V input changes to 220V, then the AVS10 turns the triac off by the next mains cycle. If the 220V input falls to 110V, the AVS10 circuit has a validation period of 8 mains cycles (when it verifies that the voltage is still at 110V) after which the triac turns on. Thus, safety features are built into the AVS10 circuit. Typical timing diagrams for the two modes are given in Figs. 5 and 6.

Figure 6. Timing diagram - $V_{mode} = V_{SS}$

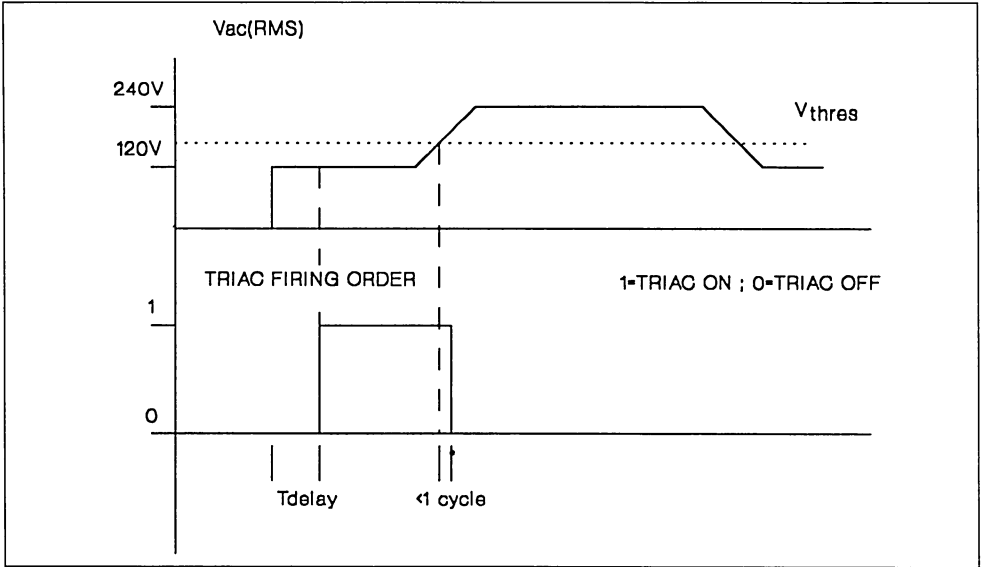
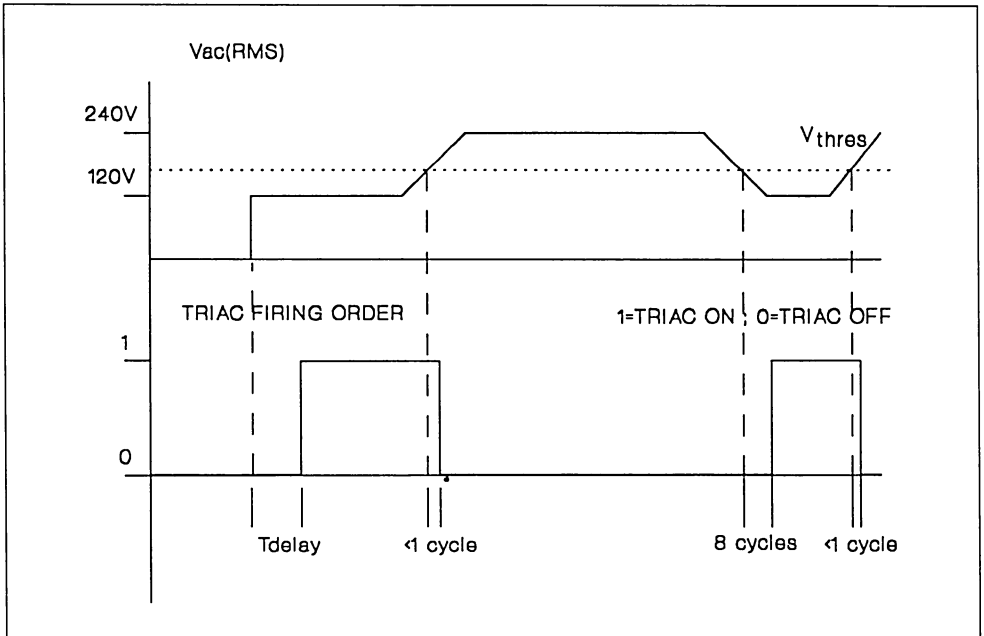


Figure 5. Timing Diagram - $V_{mode} = V_{dd}$



A detailed account of how to set the input voltage threshold is found in [2].

5. Additional Safety Features.

Additional steps are taken to enhance the safety of design include starting up always into the bridge mode. There is a delay of around 250 ms at start up before the AVS10 goes into the doubler mode.

Hysteresis is also built into the comparator to prevent small line voltage variations from causing toggling between bridge and doubler modes. Only a voltage variation of over 10% of the line voltage can cause the AVS10 to change modes.

CONCLUSION

This paper describes an efficient way of implementing an automatic doubler/bridge circuit. The primary use of this circuit is in 75W to 500W SMPS. Other innovative uses are possible. One example would be industrial motor drives which can be designed to accept either 120V line-to-neutral or 208V line-to-line input.

The main advantages of the AVS10 solution are:

1. High Efficiency. Losses are just 2W vs. 5W-10W for discrete schemes.

2. Safety. Uses digital spike suppression, hysteresis, validation of range, a failsafe mode and good control over the triac triggering.

3. Space Optimization., small supply resistor good reliability.

4. Ease of Use. Eliminates manual line selection errors.

5. Suitable solution for various power range:
AVS10 up to 300W
AVS12 up to 500W.

REFERENCES.

[1] PSMA Handbook of Standardized Terminology for the Power Sources Industry. Appendix C.

[2] SGS-THOMSON technical note 'How To Use The AVS Kit'.

MOTOR CONTROL

COMPARISON OF MOSFET AND IGBT TRANSISTORS IN MOTOR DRIVE APPLICATIONS

by B. Maurice, G. Izzo, T. Castagnet

1. INTRODUCTION

The increase of the switching frequency and the reduction of the power transistors losses are always important issues for the designer of power conversion systems. In recent years these issues have drawn attention to the comparison between IGBTs and Power MOSFETs.

In practice there is no single solution, and the choice will depend on the intrinsic transistor characteristics and the requirements of the application. These main characteristics can be summarised as:

- The ruggedness of the device (i.e., its ability to withstand surge voltages from the AC line input), and
- Its total losses, particularly at turn off and in conduction.

2. VOLTAGE RUGGEDNESS

This is the ability of the transistors to withstand pulses of energy in avalanche breakdown.

The MOSFET has high avalanche capability: for instance ST's IRF840 is specified at 510mJ single pulse avalanche energy.

The IGBT has a lower clamping capability than the equivalent MOSFET because of the junction temperature is more limited. This device usually requires external clamping protection.

3. COMPARISON OF DRIVE TOPOLOGIES

The comparison involves usually PWM switched transistors, with frequencies above the audible range (>20kHz). The cross-over point between the use of MOSFETs and IGBTs is not generally definable. The topology of the inverter and the DC input voltage will affect the choice.

For the purposes of this paper, we shall split the types of application into two categories:

- the single transistor chopper, the symmetric half bridge, the asymmetric half bridge topologies; and
- 120V RMS AC (200V DC), and 277V RMS AC (450V DC) mains supplies.

3.1 Single Transistor Chopper

This topology is usually used for brush DC motor drives. Its basic layout is shown in figure 1.

A single transistor chopper application was tested using two similar transistors with the same voltage capability: the IRF840 MOSFET and then the STGP10N50 IGBT.

The switching frequency was fixed at 17kHz with a 50% duty cycle with an applied voltage of 400V. An STTA806 TURBOSWITCH was used as the freewheeling diode. Figure 2 compares the losses of the two types of transistor. It can be seen that the MOSFET has the lower losses below 5A peak current, and the IGBT above.

3.2 Asymmetric Half Bridge

See figure 3. In this topology the motor coil current is unidirectional. It is suited for use with the switched reluctance motor.

The above comparison also applies to the asymmetric half bridge topology.

Figure 1. Single Transistor Chopper

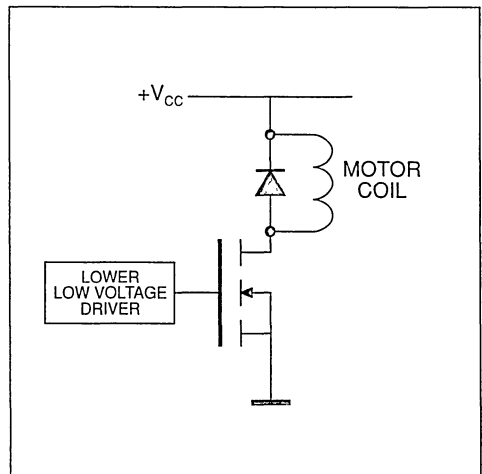
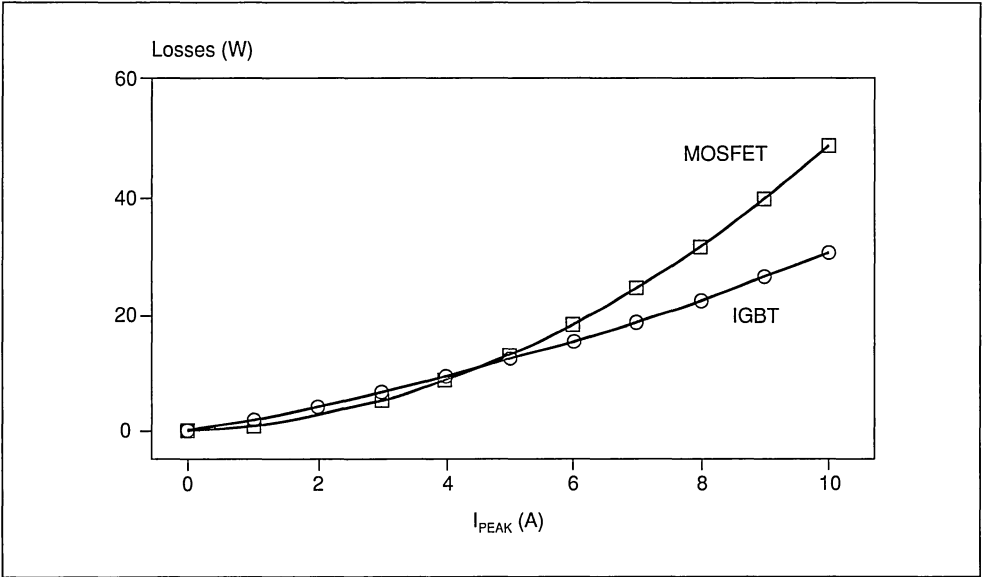


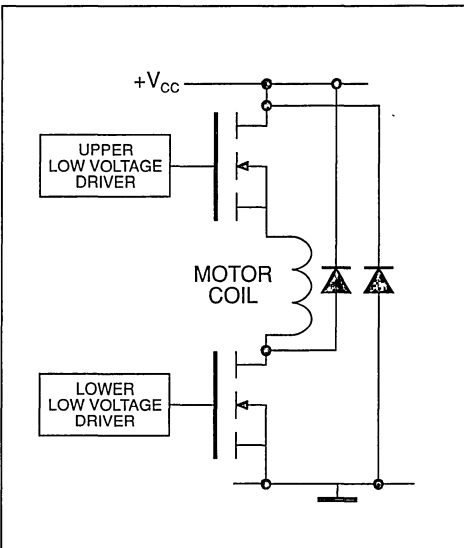
Figure 2. Comparison of 500V IGBT and MOSFET in a single transistor chopper



3.3 Symmetrical Half Bridge

This topology can generate bidirectional current. It can be used with induction motors and brushless

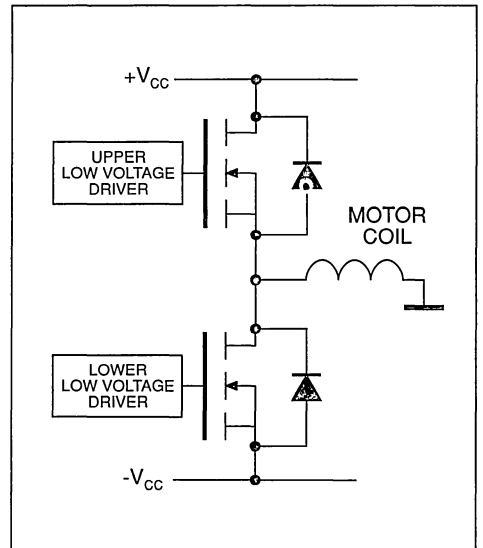
Figure 3. Asymmetric Half Bridge



permanent magnet DC motors. Figure 4 shows the basic configuration.

MOSFETs are less suited to this application, as the

Figure 4. Symmetrical Half Bridge



intrinsic body diode has poor switching characteristics, and their use leads to higher losses. The turn-off speed of the MOSFET (its maximum di/dt) is limited to reduce the reverse recovery of the diode. The crossover point between the 500V MOSFET and the IGBT is lower, around 3-4A.

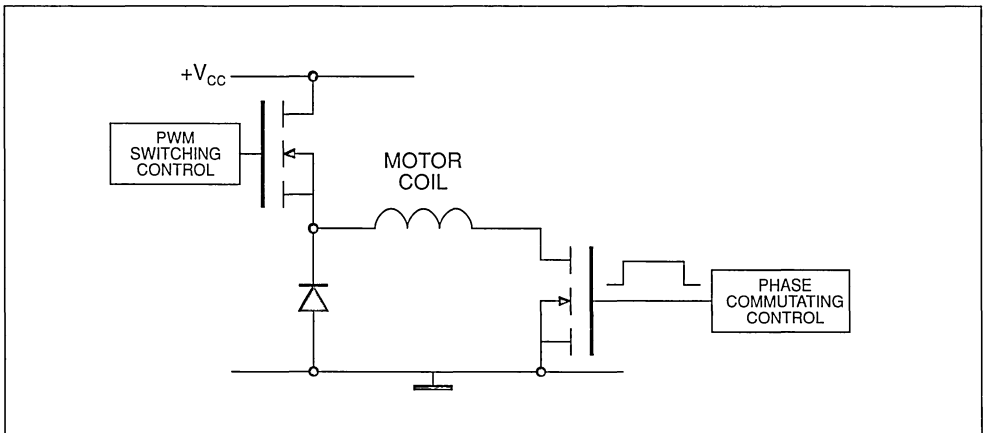
In low frequency operation (<5kHz) IGBTs perform better, as conduction losses dominate. The phase commutating transistor used in a symmetrical or asymmetric half bridge (see figure 5) corresponds to this case.

Home Appliance Electric Motors

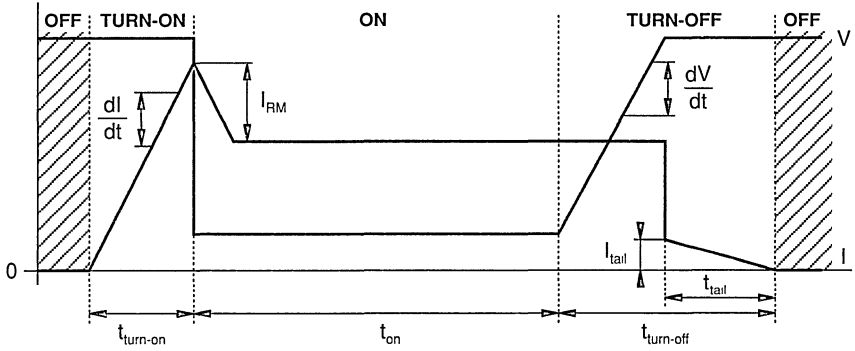
These applications usually involve a speed drive power of less than 600W. With a three-phase inverter the transferred power per phase is around 200W, and the transistor RMS current is around 3A. Such applications will require the MOSFET at least as a PWM switching transistor.

Additionally, when operating from a mains supply voltage of 120V AC, the MOSFET is the better choice. This is because 250V MOSFETs have a better $R_{DS(on)} / BV_{DSS}$ (breakdown voltage) ratio and therefore lower conduction losses.

Figure 5. Half bridge showing phase commutating transistor



APPENDIX 1. FORMULÆ FOR THE CALCULATION OF SWITCHING LOSSES IN MOTOR DRIVE APPLICATIONS



AT TURN-ON: $P_{\text{turn-on}} = 0.55 \times V \times (I + I_{RM})^2 \times f_{SW} \times (di/dt)^{-1}$

IN THE ON PHASE: $P_{\text{on}} = [(E_O \times I) + (R_D \times I^2)] \times \delta$

AT TURN-OFF: $P_{\text{turn-off}} = [(V^2 \times I \times (dV/dt)^{-1}) + (I_{\text{tail}} \times t_{\text{tail}} \times V)] \times \frac{f_{SW}}{2}$

WHERE:

f_{SW} = Switching frequency

δ = duty cycle = $t_{\text{on}} \times f_{SW}$

E_O = ON-state threshold voltage (Zero for MOSFET)

R_D = ON-state resistance

**VERSATILE AND COST EFFECTIVE INDUCTION MOTOR DRIVE
WITH DIGITAL THREE PHASE GENERATION**

B. Maurice/JM. Bourgeois/B. Saby

INTRODUCTION

The three phase induction motor is a simple design, rugged, maintenance-free which appears in home appliances requiring cost effective solutions. For speed control of these motors, a frequency variation of the inverter output voltage is required. The voltage/frequency ratio must be maintained constant, so control of these motors normally require complex control circuitry for the generation of the balanced three phase sine wave outputs.

Usually the generation of the three phase PWM signals may be controlled by a dedicated circuit, such as the SGS-THOMSON L6234, which is driven by a separate microcontroller. This solution is optimum while performance prevails over cost.

The solution demonstrated in this application note is a simplified solution using a standard ST9 microcontroller which includes large on-chip ROM memory and an internal Direct Memory Access (DMA) controller. This combination reduces the need of dedicated ICs (hardware being replaced by software), and allows over 50% of the CPU time to perform control, environmental and supervision tasks.

A practical solution to quantize three phase sine-

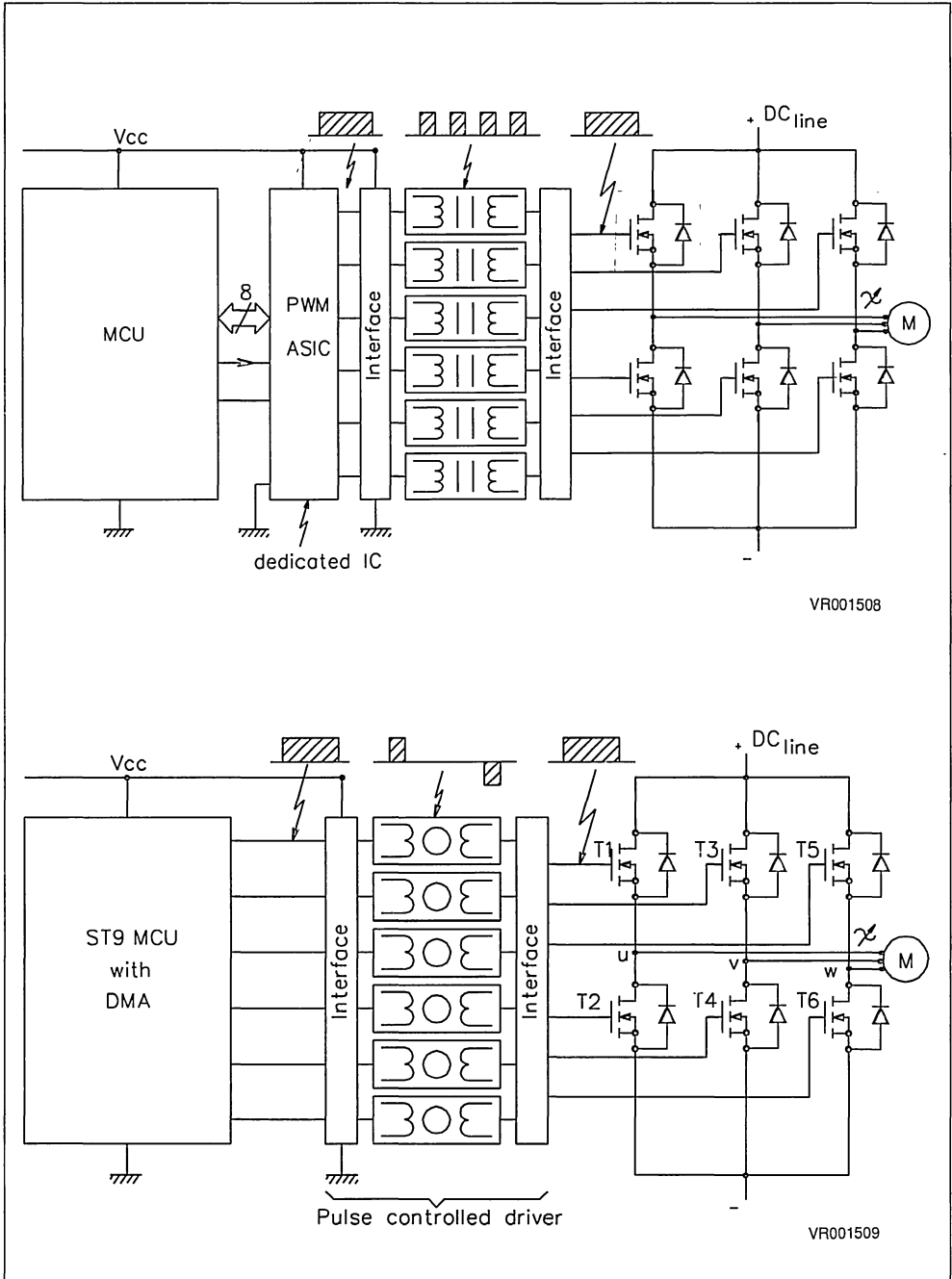
waves, and to create the corresponding DMA table is shown allowing motor voltage and motor frequency to be chosen independently. A dead time avoiding cross conduction through the bridge is also created by software. Very low acoustic noise operation can be achieved despite a switching frequency below 10kHz, due to a shifting of the switching instants leading to a virtual doubling of switching frequency.

Each of the six digital outputs of the ST9 sets directly the state of the six power MOSFETs (or IGBTs) of the bridge via an insulated interface. This interface is described in the second part of this note. The fully isolated pulse controlled gate driver requires no floating auxiliary supply, meets safety standards and achieves a large dV/dt immunity.

Figure 1 shows how to generate a three phase sine wave by modulation of pulse width. This modulation is often obtained with a special dedicated IC controlled by a MCU (above).

Using a MCU having large memory integrated on the chip combined with DMA, spares the use of dedicated IC (below). Hardware is replaced by software. The sine waves are directly synthesized by the MCU.

Figure 1. Three Phase PWM Generation Techniques



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DIGITAL CONTROL OF POWER SWITCHES

In this proposed solution, the ST9 microcontroller controls simultaneously the ON- and OFF- states of the six power switches of the inverter bridge. All these instantaneous ON-OFF states are stored in internal memory (ROM) and are sequentially transferred (every 5s for example) to six bits of a parallel output port by DMA (see Figure 2). The voltage level 0-5V of each output bit drives directly the gate interfaces of the six power switches .

All data corresponding to the switching duty cycle values is permanently stored in ROM and generates the quantized three phase sine waves. A dead time between adjacent Power switches is also stored, avoiding cross-conduction through the power bridge. The motor frequency and motor voltage are also stored independently.

The major part of the ROM is occupied by this permanent data, used to generate, step by step, the three phase sine-waves. This data is grouped in several tables (patterns), constituting series of bytes that have to be sequentially output on the parallel output port. A full scrolling of each pattern corresponds to a complete switching basic cycle of the six power switches. This is repeated the necessary number of times to complete the step duration of sine wave. The following pattern will then be scrolled to realize the following step.

This direct sequential transfer from memory to output port is performed by DMA [2], and is self operating. The central unit only works when the last byte of one pattern appears, the program then deter-

mines whether the same pattern must be scrolled again, or if another new pattern has to be scrolled.

All patterns needed for an application, as well as the program managing their scrolling order and their number of repetitions, are to be created and stored in ROM.

MOTOR DRIVE CONFIGURATION

Microcontroller

The ST9036 microcontroller from the ST9 family with 16k-byte of ROM or EPROM memory [1], of which only one output port and one multifunction timer are used for PWM generation. Six bits of its output port are gathered in pairs, one pair for every bridge leg (phases: u,v,w). The two bits remaining free can be used, for example, either to control two other power switches (i.e for heat control in a washer), or to generate a synchronized signal to perform measurement of V/I phase.

The ST9 microcontroller is able to manage two further functions:

- a) Slow operations for motor and environment controls, such as timing of sequential operations, speed control, safety supervision tasks, etc. (These are not detailed in this application note).
- b) Faster operations for real time management of the states of the power switches for PWM generation.

All others functionalities of the ST9036 remain available, such as other I/O ports, Timers, Analog/Digital converters and all interrupt functions.

Figure 2. DMA Transfer to control power switches

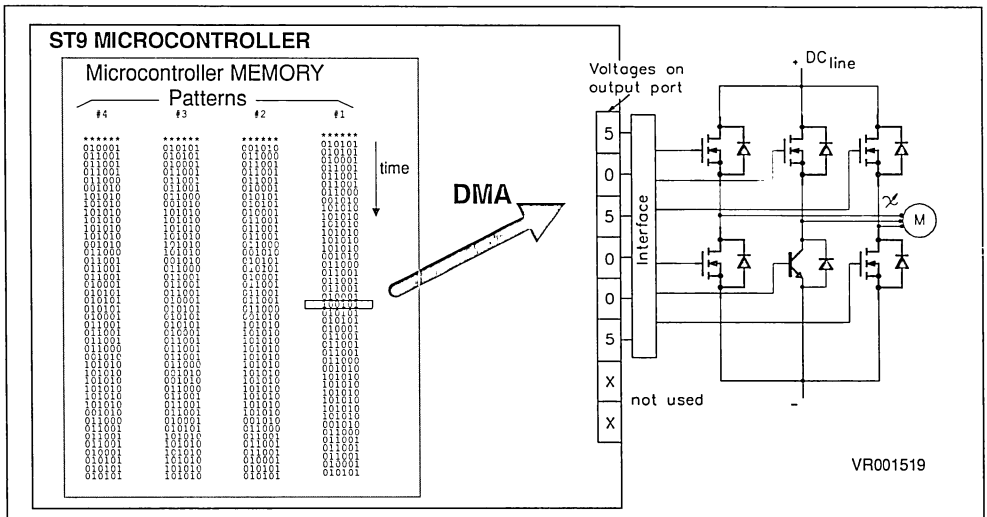
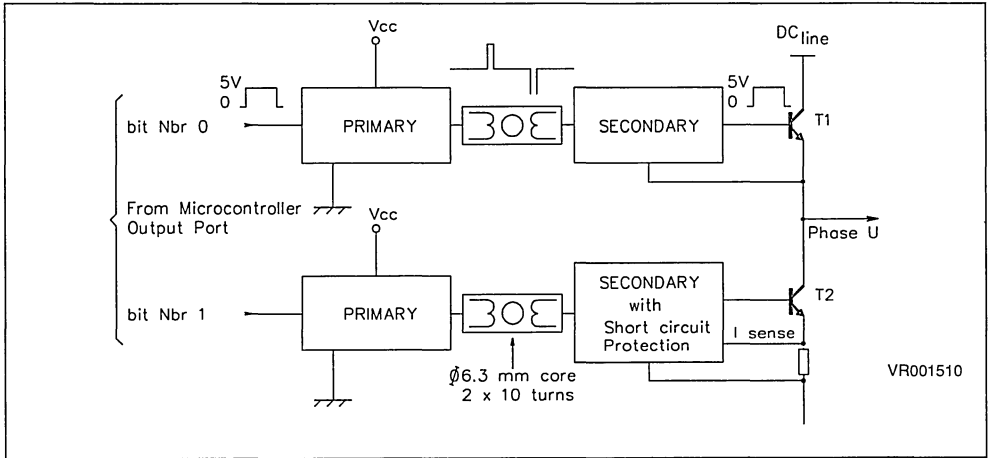


Figure 3. Driver for one Bridge Leg



In the practical example described in the following sections, ST9 is not heavily occupied by these real time operations:

- Using DMA is similar to slowing down the ST9 and engages only 35-40% of the CPU time.
- Speed control (frequency variation) needs only few instruction lines but no memory space. The memory space is mainly used to store necessary data to generate six various three phase voltages supplying the motor (1k-byte for each voltage).

Drivers For Power Switches

The driver interfaces the ST9 output port to the gate of the power switches.

- it converts the output level (5V) to the required gate-source voltage level (15V) of IGBT or Power-MOSFET.
- it provides a galvanic isolation.
- it protects against current surges and short circuits.

It is constituted by six independent circuits for the six power switches. Each is a pulse controlled driver [4] including: (see Figure 3)

- a primary circuit to create a calibrated Pulse with short duration.
- a small pulse transformer. (DIL molded package)
- a floating secondary circuit operating without any auxiliary supply and including the autonomous short circuit protection.

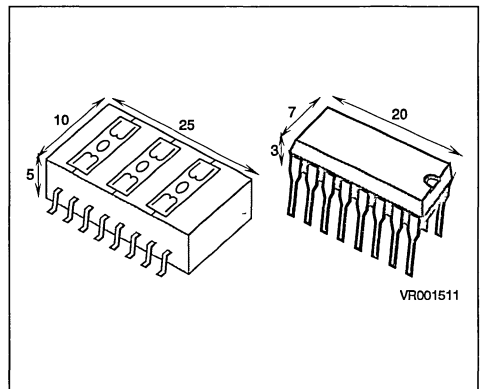
The primary circuit differentiates the logic level input signal. The positive and negative calibrated output pulses ($\pm 15V/0.5\mu s$) correspond to the switch-

on/switch-off command. The primary circuit output stage is a full bridge having a low output impedance in order to obtain short rise times and high amplitude current pulses.

The pulse transformer can be small. A ferrite core of 6.3mm diameter with 10 turns is sufficient as it has to sustain 15V for 0.5 μs . In this application, three core transformers are housed in the same standard or SMD package [3].

The secondary circuit needs no supply and uses the input gate capacitor of the Power-MOSFET or IGBT like an R/S memory latch. The required energy is limited to charge and discharge the input gate capacitor. During the OFF-state, a low impedance is maintained across the gate-source of the Power switch, avoiding any reconduction due to externally applied dV/dt.

Figure 4. Transformer Core Size vs 16 pin DIL



In several applications, when isolation between the power and control sections is not mandatory, the low side driver can be a simple non-insulated driver. Nevertheless, the fully isolated solution performs high dV/dt immunity and meets insulation standards.

DC/AC Inverter

For this function, a three-phase bridge with six switches (Power-MOSFETs or IGBTs) is used. (Figure 1). The two switches of each bridge leg are opposite phase controlled. A dead time, avoiding simultaneous conduction, is generated directly by the ST9036 microcontroller.

Sine wave generation: (Figure 5)

The voltage on middle point of "u-phase" bridge leg is given by:

$$V_u = V_{DC} \cdot \delta_u \quad \delta_u = \text{u-phase duty cycle}$$

$$t_{\text{on hi}} = \text{"ON state" duration of high side switch}$$

$$\delta = t_{\text{on hi}} / T_s \quad T_s = \text{switching period}$$

$$V_{uw} = V_u - V_w \quad V_{uw} = \text{phase to phase motor voltage}$$

If δ_u is sinusoidal modulated, the average voltage on half bridge middle point describes sinusoidal wave form centered to $V_{DC}/2$. To avoid DC components in the motor, each phase voltage has to be symmetrical compared to $V_{DC}/2$.

Motor voltage value

Motor voltage is maximal when the duty cycle modulation varies from 0% to 100% (modulation depth: $K=100\%$)

Motor voltage is minimal (nil) when modulation depth $K=0$; δ does not vary and is equal to 50% (Figure 5b)

Sine wave frequency variation

This is obtained by varying the frequency of the duty cycle modulation.

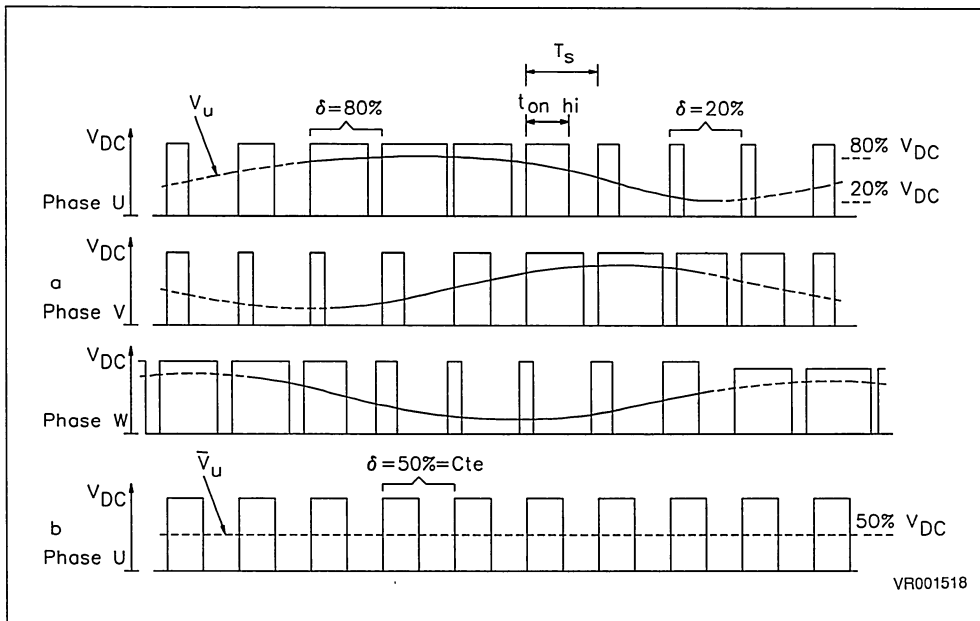
CREATING TABLES OF DATA

The variable speed drive of induction motors requires generating three voltage sine waves and control of their amplitude, phase and frequency. The first step is to digitize the three phase system in order to create all the necessary data to be stored into the ROM of the ST9 microcontroller.

Figure 5. Sine Wave Generation at the output of one bridge leg

a. Modulation depth 60%, duty cycle 20 to 80%

b. Constant duty cycle



Fundamental period quantification

The fundamental period of motor voltage is divided into 24 "segments"; (each segment equals 15° of arc). This gives a good sine wave accuracy in many applications. During each "segment" the voltage is a percentage of the DC line voltage, given by duty cycle (δ). For example, the duty cycle must be 55% during the segment from 165° to 180° for phase U (Figure 6).

Creating the duty cycle table

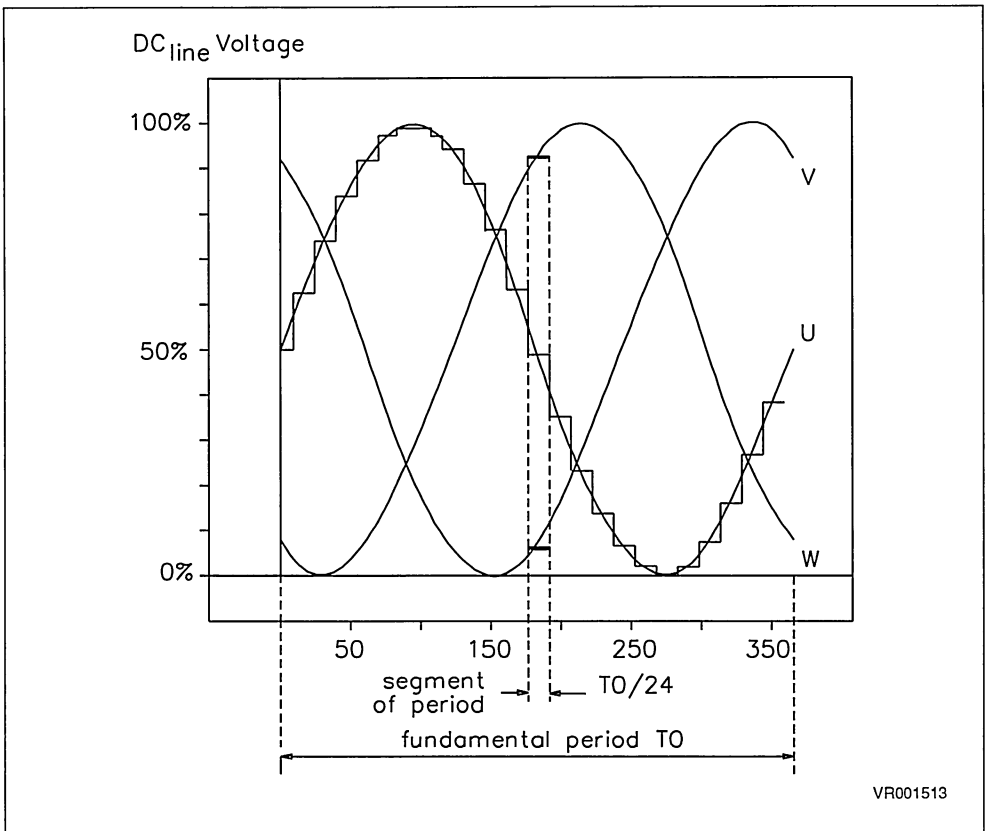
The second step is to establish a table giving, for each segment, the duty cycle value (δ) for each of the three phases. In fact δ_1 , δ_3 , δ_5 are duty cycle values for each high-side switch (T1, T3, T5). The low side switches are in the opposite states and

their duty cycle value is complementary to 100%. This entire table defines exactly the three-phase sine wave system during one period (T_0) and for one motor voltage. (Figure 7) These table values respect phase balance and avoid neutral currents. To achieve these conditions it must be ensured that:

- a) on each line, the sum of the three duty cycle values is constant (equal to 150%).
- b) The duty cycle has a symmetrical value either side of 50%. In practice the quantized values have to be chosen close to the mathematical value of sinus for only a quarter of the period, then symmetrically repeated respecting the condition (a).

This duty cycle table is not stored in ROM. It only defines the necessary data to create the patterns. One line of this table defines one pattern (see following section).

Figure 6. The fundamental period divided into "segments"



VR001513

Figure 7 . Duty cycle table defining data to create patterns $V_{PHASE} = 0.6 \times V_{LINE}$

Pattern #	U δ1%	V δ3%	W δ5%
1	80	40	30
2	80	45	25
3	75	55	20
4	70	60	20
5	60	70	20
6	55	75	20
7	45	80	25
8	40	80	30
9	30	80	40
10	25	80	45
11	20	75	55
12	20	70	60
13	20	60	70
14	20	55	75
15	25	45	80
16	30	40	80
17	40	30	80
18	45	25	80
19	55	20	75
20	60	20	70
21	70	20	60
22	75	20	55
23	80	25	45
24	80	30	40

One Pattern

9

010101
010101
010001
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010101

Pattern definition

A pattern is a succession of bytes stored in memory. Each bit (1;0) of these bytes gives the instantaneous state (ON;OFF) of each of the 6 six power switches (Figures 7&9). Pattern contains number of bytes necessary to define one entire basic switching cycle.

A particular pattern has to be created for each segment of the sine wave period. All these patterns are stored in the ST9036 ROM.

For example (Figure 8), a pattern contains sequence of 42 bytes defining one basic switching

cycle. The switching period T_s , shared into 42 units of times, gives a good sensibility of duty cycle adjustment of about 2.5% (1/42th). This time unit corresponds to the rhythm of the DMA timer and its duration is chosen as a multiple of the ST9 micro-controller clock period (0.25 μ s).

In this example, one unit of time equals 4.75 μ s in order to have a pattern scrolling time or switching period $T_s = 200\mu$ s. This corresponds to 5kHz of switching frequency.

Two dead times (one time unit each) at every state change of adjacent switches avoid cross conduction of the bridge leg.

Figure 9. Pattern table

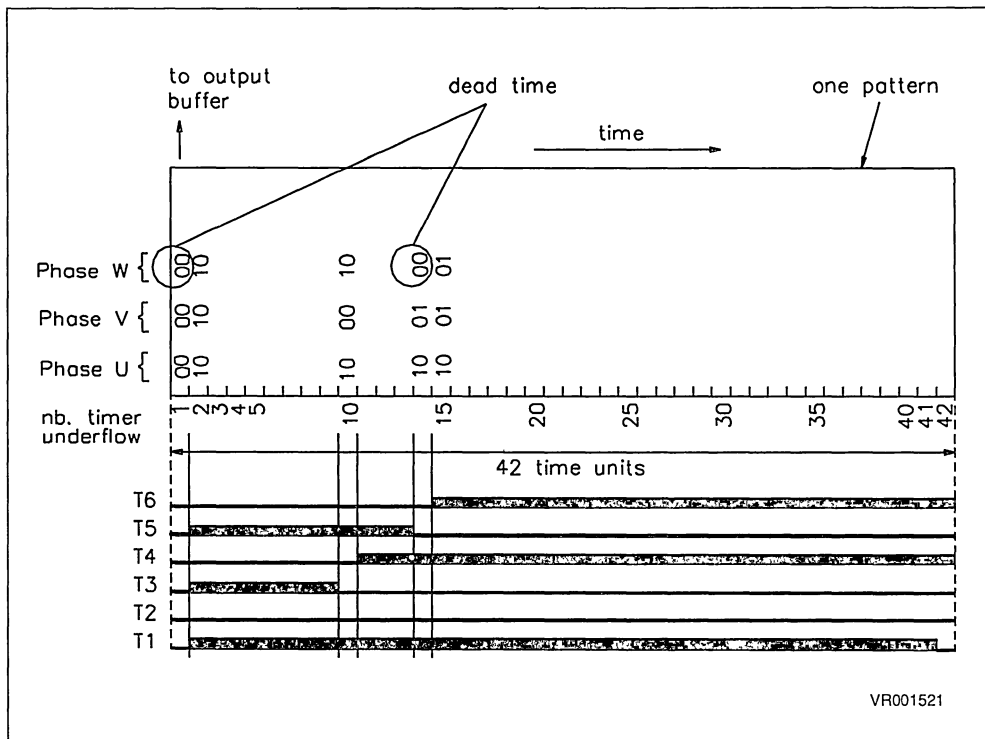


Figure 9: One pattern is an elementary table grouping all necessary bits to define the basic switching cycle of every six inverter switches. Bytes are sequentially read by DMA, and transferred to the output buffer. The resulting switching cycles shown on the bottom of the figure gives the following duty cycles:

- phase U: $\delta 1$ (T1) = 100% ; $\delta 2$ (T2) = 100% - $\delta 1$
- phase V: $\delta 3$ (T3) = 20% ; $\delta 4$ (T4) = 100% - $\delta 3$
- phase W: $\delta 5$ (T5) = 30% ; $\delta 6$ (T6) = 100% - $\delta 5$

MOTOR VOLTAGE CONTROL

One table of duty cycle defines the 24 stored patterns (set of patterns) containing information to one AC motor voltage. As an example, the peak value of phase voltage generated by the table given on Figure 7 is equal to 60% of V_{DCline} . It is necessary to create a set of patterns for each of the needed motor voltage.

The motor voltage can be controlled independently of the frequency. This voltage depends on the set

of pattern which the DMA is reading. By storing within ROM and reading different set of patterns, the voltage across the motor can be changed and shaped. In this example, a set of patterns includes 24 patterns of 42 bytes each = 1008 bytes.

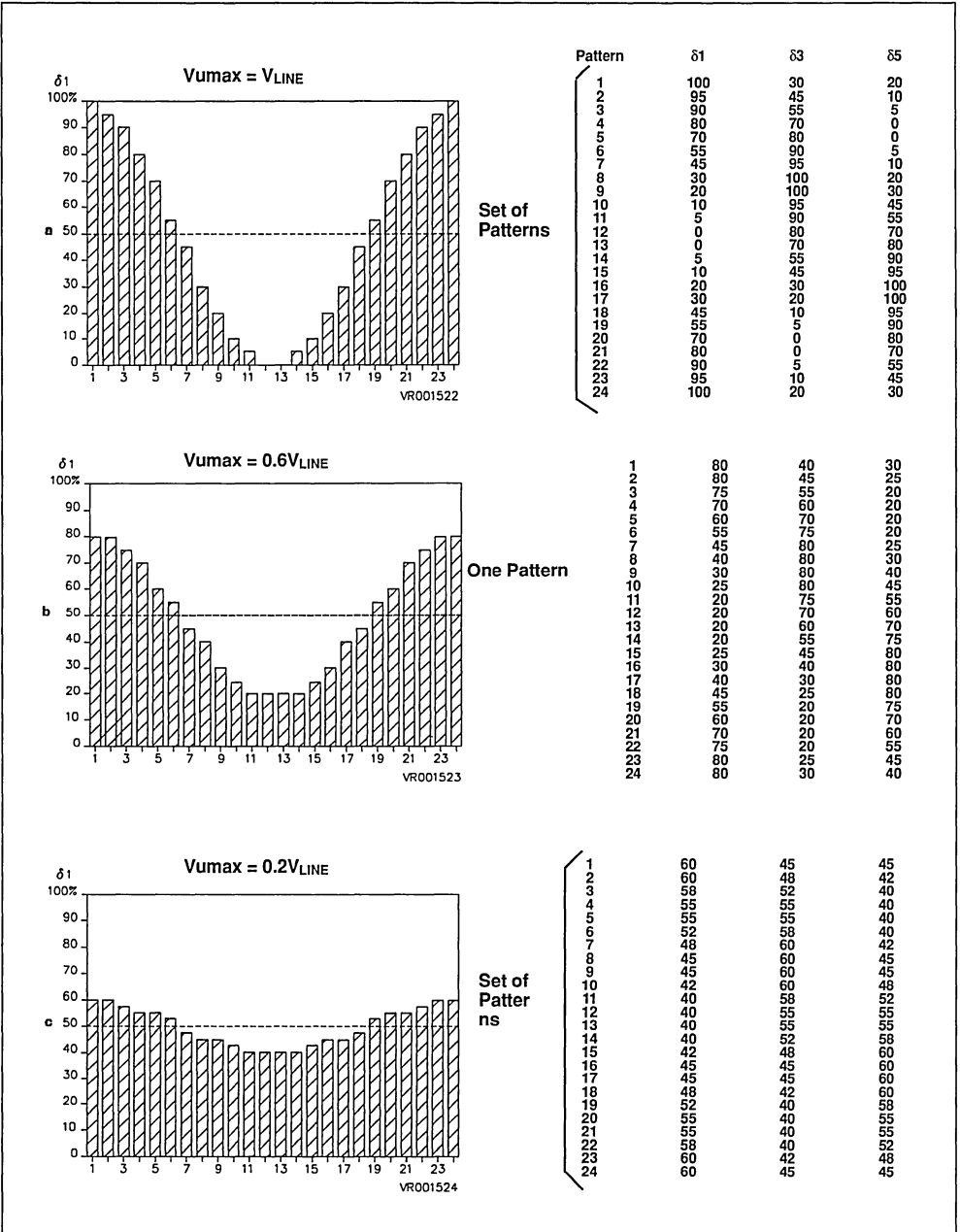
Figure 10 shows $\delta 1$ duty cycle of the T1 switch for various values of motor voltage. On the right side the chart gives the corresponding values of $\delta 3$ and $\delta 5$. Each line of these charts defines a pattern. These values respect the phase balance and avoid current in neutral line. The useful RMS voltage across motor phases is given by:

$$V_{RMS} = \frac{1}{2} \cdot K \cdot \sqrt{\frac{3}{2}} \cdot V_{DCline}$$

The K factor corresponds to modulation depth of the duty cycle (δ) as shown on examples (a,b,c).

- a: K= 1.0 when duty cycle varies from 0% to 100%
- b: K= 0.6 when duty cycle varies from 20% to 80%
- c: K= 0.2 when duty cycle varies from 40% to 60%

Figure 10.81 Duty Cycle of T1 Switch



MOTOR FREQUENCY CONTROL

Motor frequency is controlled via duration of the fundamental period T_0 .

The shortest duration of the period (the highest frequency) is reached when each segment of this period corresponds to only one reading of the corresponding pattern. In our example (Figure 11) the pattern reading duration equals $200\mu\text{s}$, and with 24 segments.

When each segment corresponds to two readings of pattern, the fundamental period is twice as long. Thus the frequency (motor speed) can be controlled step by step whether the pattern is read once or several times. Consequently when starting from the highest frequency, it is possible to have discrete submultiples of frequency.

$F = F_0/N$ N = number of times of patterns being read

The speed resolution is low for high motor speed, but high for low motor speed. So, to perform the

speed control by software, it is sufficient to give the number of times the pattern is to be read. For example, when repeating 20 times the same pattern the following results are obtained:

$4.75\mu\text{s}$ = time unit

42 = number of time units per pattern

20 = number of patterns (or switching cycle) reading per segment

24 = number of segments per fundamental period

This gives a fundamental frequency of 10.4Hz

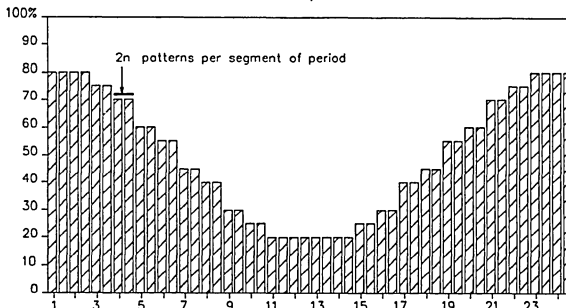
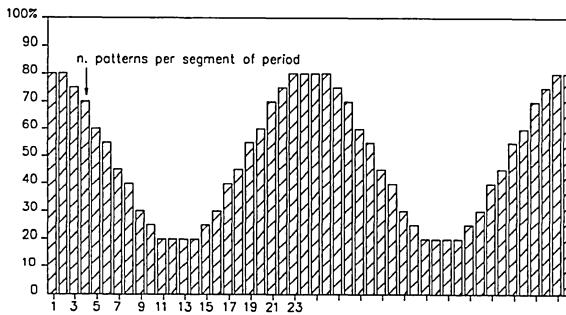
Another way to adjust motor speed by software is to change the DMA timer period. That is equivalent to modifying the "time unit" duration. The reduction of time unit duration is limited by the highest consumption of CPU time to be accepted and the shortest permissible dead time is according to power switches used.

By combining these two methods, pattern repetition and timer variation, it is possible to perform quasi-continuous variation of motor speed.

Figure 11. Fundamental Frequency variation

a. $T_0 = 200 \times 24 = 4800 \text{ ms}$ $F_0 = 208 \text{ Hz}$

b. $T_0 = 200 \times 2 \times 24 = 9600 \text{ ms}$ $F_0 = 104 \text{ Hz}$



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DEPHASING SWITCHING INSTANTS

When creating the pattern, the instant of switching can be chosen specifically for each bridge leg. For example it is possible to simultaneously turn-on all the high side switches (T₁, T₃, T₅) and stop them when respectively each duty cycle is reached (Figure 12a).

Through other ways for the same duty cycle the ON-state is centered at the middle of pattern (Figure 12b).

Various other possibilities can be chosen to create the pattern. The acoustic noise of the motor will depend on this choice. For example the pattern shown in Figure 12c gives a large current ripple and very noisy motor, while, on the contrary, Figure 12b gives a noiseless motor according to small current ripple (shown at 20ms/div; 2A/div).

When the three high side switches or the three low side switches are simultaneously ON or simultaneously OFF, no energy is transmitted into the motor, which is freewheeling. Another possibility is to choose simultaneously the OFF-state rather than the ON state simultaneously as shown Figure 12e to compare with Figure 12b. In this case two swit-

ches of one bridge-leg are not switched and switching losses are reduced.

Figure 12 shows how various possibilities can be chosen for pattern creation .

Current ripple and acoustic noise of motor will depend on this choice.

On the right side, motor current with:

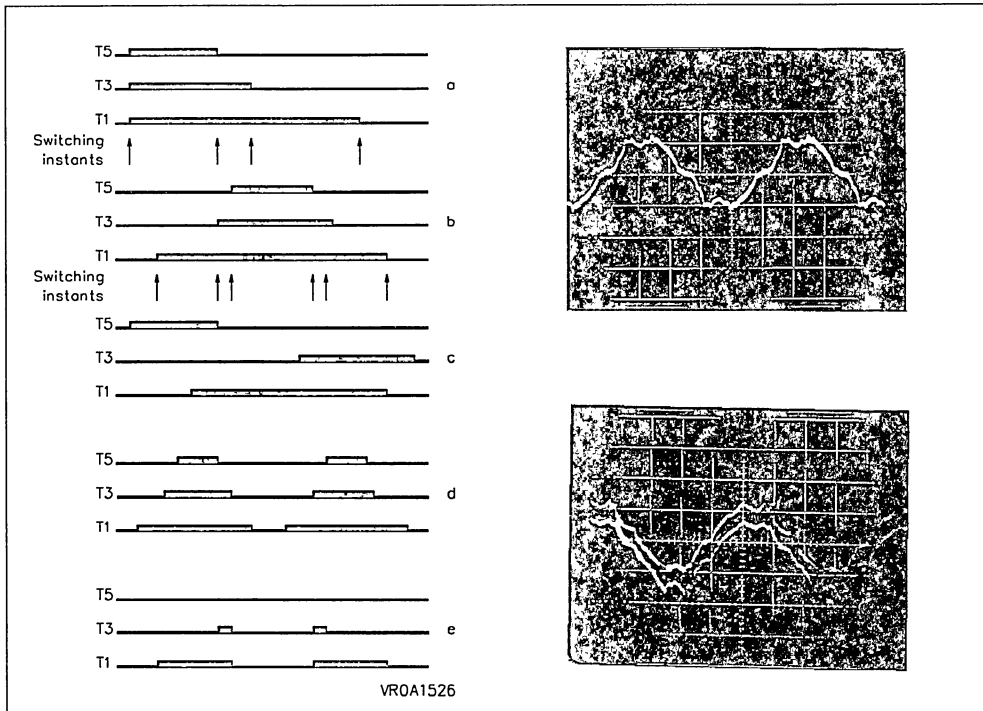
- noiseless motor according to small current ripple.
- noisy motor according to large current ripple.

As the energy is transmitted when switches are not in the same state, the rule to create a pattern is to maximize the instants where the switches are in the same state and simultaneously shift the switching instants.

All these methods can be used to obtain very low acoustic noise operation in spite of a switching frequency below 10kHz.

Without reducing the time unit, it is possible to increase the acoustic frequency by sharing in two equal parts each duty cycle time ($\delta=60\% \Rightarrow \delta=30\%+30\%$). The switching frequency is doubled and acoustic noise is close to the inaudible region and becomes very low (Figure 12d)

Figure 12. Pattern options affecting ripple and acoustic noise



EXPERIMENTAL EXAMPLES

Figure 13 shows an example of generated three phase PWM signals on microcontroller outputs. It represents three control signals for T1, T3, T5. The set of pattern corresponds to a modulation depth of 100% as shown on table Figure 10a. The phase angle between each phase is 120°.

Figure 14 shows current measured in motor phase (20ms/div, 2A/div).

- a) obtained with set of pattern shown on Figure 10b, and repeated twenty time, $f=10\text{Hz}$
- b) patterns are repeated twice, $f=100\text{Hz}$.

The used set of pattern (at 60%) of Figure.10b, combined with doubly of switching instants (Figure 12d), gives a well defined sine wave.

Very little ripple of current and doubling switching frequency give a noiseless motor operation.

The motor is speeded up by repeating patterns only twice (Figure 14b). Simultaneously the motor voltage is increased by using set of pattern (Figure 10a) having modulation depth of 100%.

Figure 13. Three microcontroller outputs: 5ms/div, 5V/div

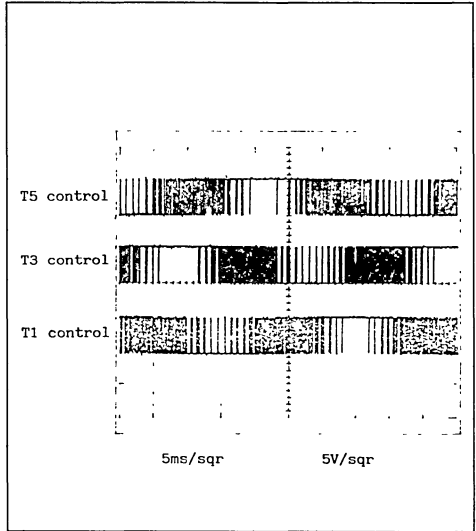
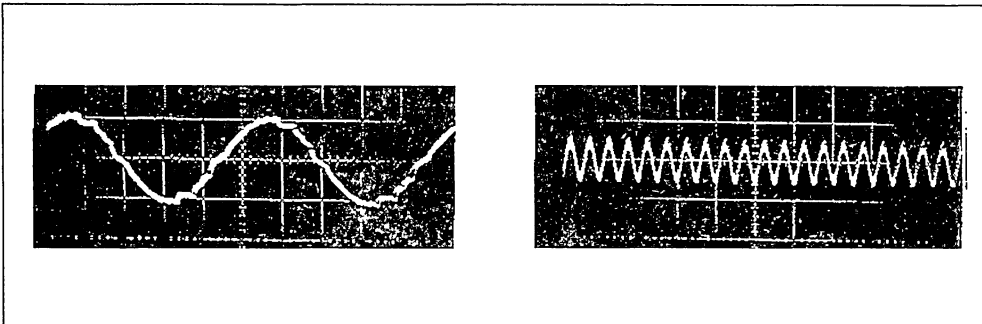


Figure 14. Current measured in motor phase



SUMMARY

For large volume applications such as washing machines, air conditioning or cooling pump motor drives, cost optimization is a key issue. The solution to drive induction motor presented in this paper simplifies conventional digital solution. Using a ST9 microcontroller with Direct Memory Access and fast data transfer, replaces dedicated ICs by software or more precisely by data stored in microcontroller memory.

The proposed solution is very versatile because a standard microcontroller, the ST9036, can be programmed for various applications, only the software will has to be adapted.

This note presents methods to generate data in order to shift the switching instants of inverter switches. This allows to reduce motor acoustic noise in spite of switching frequency being below 10 kHz, and to minimize motor and converter losses.

The described pulse controlled gate driver uses standard components and small enough core transformers that can be fitted into a Surface Mounting Package. This way offers a cheap fully galvanic insulation when required.

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APPENDIX MICROCONTROLLER WITH DMA

The feature of microcontroller with DMA (direct Memory Access) consists in having a possibility of direct access between microcontroller memory and its on-chip peripherals. Moreover, one of the parallel I/O ports can be coupled with the timer's DMA channel, allowing fast data transfers between memory and this I/O port with minimum CPU overhead. Data transfers are scheduled by the timer.

The only task of the Microcontroller software is to specify which pattern is to be read by the DMA channel at a given time in order to reproduce the three-phase sinewaves, as described in the previous sections. After a complete pattern transfer, the Micro-controller CPU is interrupted (DMA End of block interrupt) and the DMA should start to read the next pattern.

In order to achieve high speed continuous transfers without stringent response time requirements for this End of block interrupt, a "swap mode" is used: while a pattern is read by the DMA channel, the subsequent pattern can be prepared in advance; so, once the last byte of the pattern is read, the DMA automatically switches to the new pattern while the old one can be updated during the DMA End of block interrupt routine.

First tests show that the DMA operation in swap mode, as described hereabove, accounts for 35-40% of the total available CPU time of the Microcontroller. Therefore, thanks to its processing power, the Microcontroller can easily perform any control and supervision task in addition to this DMA-driven PWM generation.

COMPACT HIGH PERFORMANCE BRUSH D.C. MOTOR SERVO DRIVES USING MOSFETS

by C.K. Patni

ABSTRACT

For medium power (200VA to 6kVA) brush D.C. motor servo drives, MOS field effect transistors (MOSFET) are ideally suited. A compact high performance (20 to 50kHz) 1.2kVA brush D.C. motor velocity servo drive, which has been developed and tested, is presented. IRF640 and BYW8PI200 high efficiency fast recovery epitaxial diode (FRED) are used in the 1.2kVA power stage. A 6kVA motor drive design using ISOFETs is also presented.

STE100N20 (ISOFET), and BYV54V200 FRED diodes are utilized in the 6kVA design in which FREDs are used as the MOSFET series blocking diode and the free-wheel diode. Different power H-bridge configurations are chosen and justified for the 1.2 and 6kVA drives. Particular emphasis is placed on short-circuit protection techniques and simple gate drives.

INTRODUCTION

Brush D.C. permanent magnet motors are extensively used as velocity servo drives for high performance applications such as robotics and machine-tools. The high voltage D.C. (HVDC) supply of the power stage for such motors rated up to 6kVA is generally limited to 200V D.C. because of sparking of the commutator and brush assembly.

The commutator has a maximum volts per segment rating at rated power above which there is excessive brush wear. MOSFETs are well adapted for medium power applications at voltages up to 500V. Consequently the ease of paralleling, high peak current capability and the ease with which MOSFETs can be controlled and protected make them ideal power semiconductor switching devices for such motor drives. Medium power brush D.C. motor voltage limitation of 200V D.C. enables fast recovery epitaxial diodes (FRED) to be used which have high efficiency due to very low conduction losses and negligible switching losses :

BYW81PI-200 : FRED :

$$V_f < 0.85V \quad (I_f = 12A ; T_j = 100^\circ C)$$

$$t_{rr} < 35ns$$

Block diagram schemes for brush D.C. permanent magnet velocity servo drives are discussed. Servo drive specifications shown in table 1 are considered and sol-

utions for the 1.2kVA and 6kVA motor drives are presented. The 1.2kVA motor drive is developed and tested. Protection, efficiency and switching frequency requirements have strongly influenced the designs.

Other than the power ratings, the parameters listed in the specification are common for many high performance servo drives. The main component in the design of the hardware is the power H-bridge switching ideally above the audio-frequency range. High frequency switching permits a compact power output filter to be used to filter the switching frequency if so desired.

SWITCH-MODE MOTOR DRIVE CONCEPTS

Figure 1 illustrates a conventional pulse width modulated (PWM) D.C. motor servo drive. The velocity demand and the tachogenerator feedback signals are compared and the resultant velocity error is amplified. This error is fed to the current servo amplifier where it is compared with the actual current flowing in the motor armature. The amplified current error is fed into a linear PWM generator. The control of the mark to space ratio of the PWM generator is achieved by comparing the input error signal with a constant frequency triangular waveform. This results in a fixed frequency PWM signal which is fed to the power stage.

A switch-mode drive designed to the specification in table 1 comprises of :

- 1/ Drive and protection for power devices
- 2/ Power supplies
- 3/ Regenerative energy clamp (4 quadrant control)
- 4/ Current loop
- 5/ Control and logic for PWM and velocity servo.

The block diagram of the drive which has been developed is outlined in figure 2. (The complete circuit diagram is provided in figure 14). The differences between the two schemes outlined in figures 1 and 2 are that the current control loop and the PWM integrated circuit are eliminated in the second scheme. In the second scheme the velocity error is fed directly into a velocity compensation and modulation circuit. The elimination of the current feedback loop limits this scheme in so much as it can not be used in torque control applications.

APPLICATION NOTE

Table 1 : Typical Brush D.C. Servo Drive Specification.

Specification	1.2kVA	6.0kVA
Modulation Frequency	> 20kHz < 50kHz	
Continuous Power	1300VA	6000VA
Maximum Continuous Current	10A	50A
Bus Voltage Input	120V _{DC}	
Efficiency	> 90%	
Short to Ground	Shut down	
Short to Bus Voltage	Shut down	
Armature Short	Shut down	
Operating Temperature	0 to 50°C	
Velocity Demand	10V	
Regenerative Energy Dissipation	10% of Continuous Rating	

Figure 1 : PWM D.C. Servo Drive.

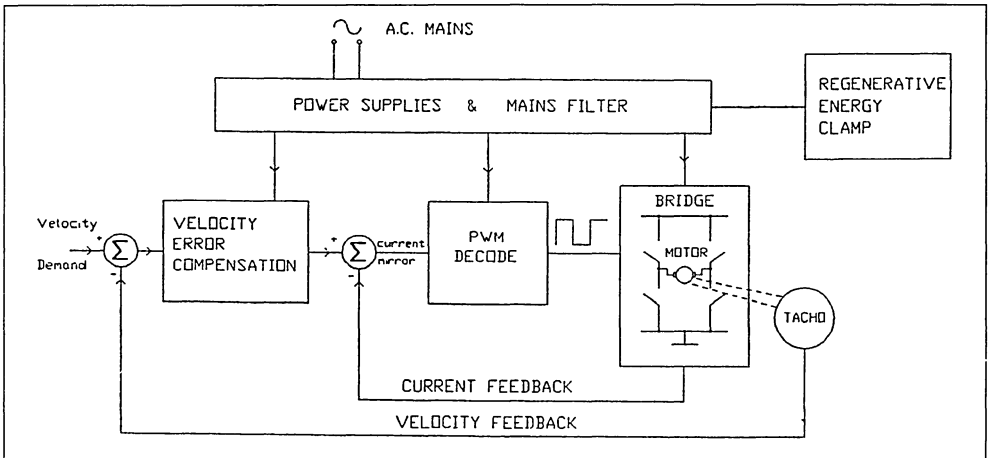
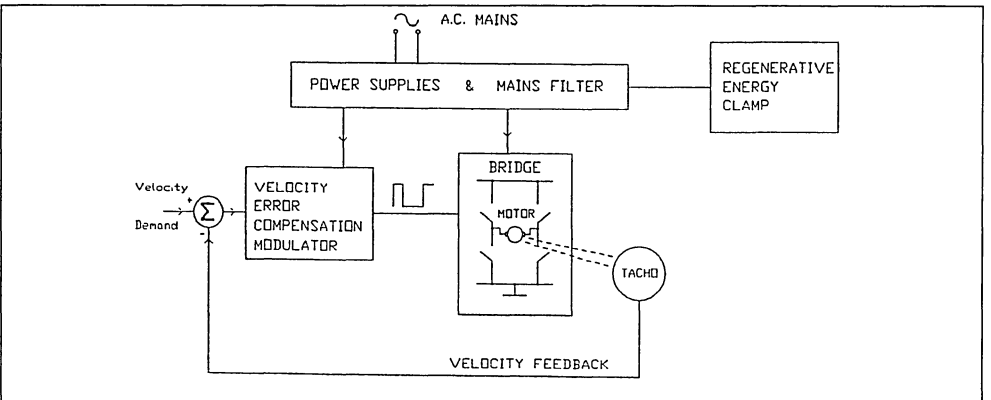


Figure 2 : Schematic Diagram of Brush D.C.P.M. Motor Drive.



BRIDGE CONFIGURATIONS & MODULATION TECHNIQUES

The bridge design must be capable of supplying bi-directional current to the motor for optimal four quadrant control. This can be achieved by using a "T-bridge" or an "H-bridge", as shown in figure 3. The H-bridge is generally chosen since it requires a single power supply. The voltage rating of the power semiconductor devices matches the motor voltage rating for the H-bridge alternative.

The H-bridge has eight operating modes when connected to a D.C. motor load. These modes can be seen in figure 4. Two of the modes increase current supplied to the motor winding in either direction. The other six operating modes reduce current in the motor winding and are commonly known as free-wheeling modes. Numerous switching modes are possible for PWM and current control. For example,

it is possible to PWM both the top and bottom devices in the bridge or simply either the top or bottom device. It is possible to use the PWM mark to space ratio such that the mark provides a positive rate of change of current in the motor winding and the space provides a negative rate of change of current. The control of the pulse width thus establishes an adjustable average voltage across the motor load.

A modulation technique used in the developed servo drive is illustrated in figure 5. This modulator is based on "delta modulation" (reference 1). The mark to space ratio of the modulator output ($0(t)$), determines the conduction period of the MOSFETs in the H-bridge. The modulator comprises of the standard delta modulator (part A), the proportional term (part B) and the integral term (part C) of the PID controller.

Figure 3 : Bridge Configurations.

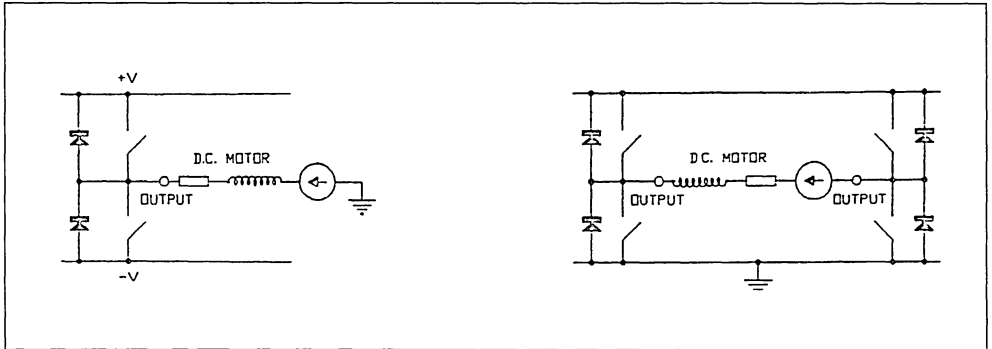


Figure 4 : Operating Modes of the H-bridge Showing Current Flow Paths.

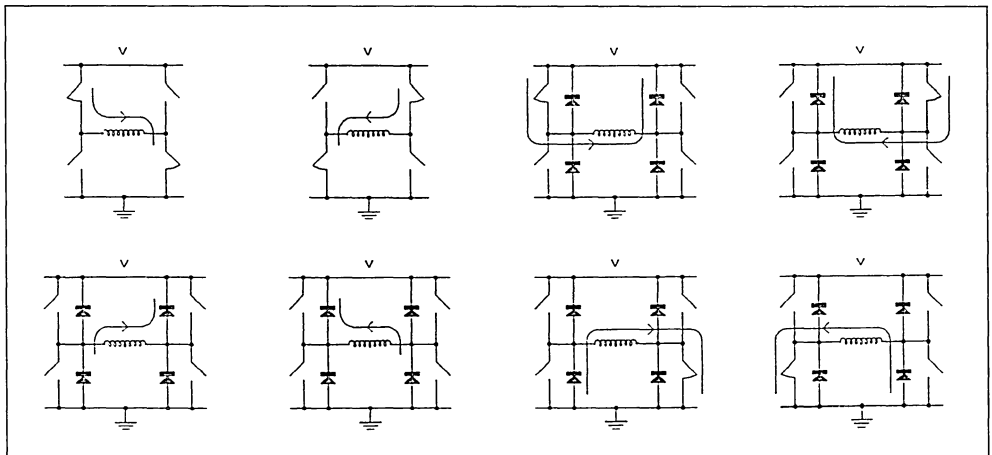
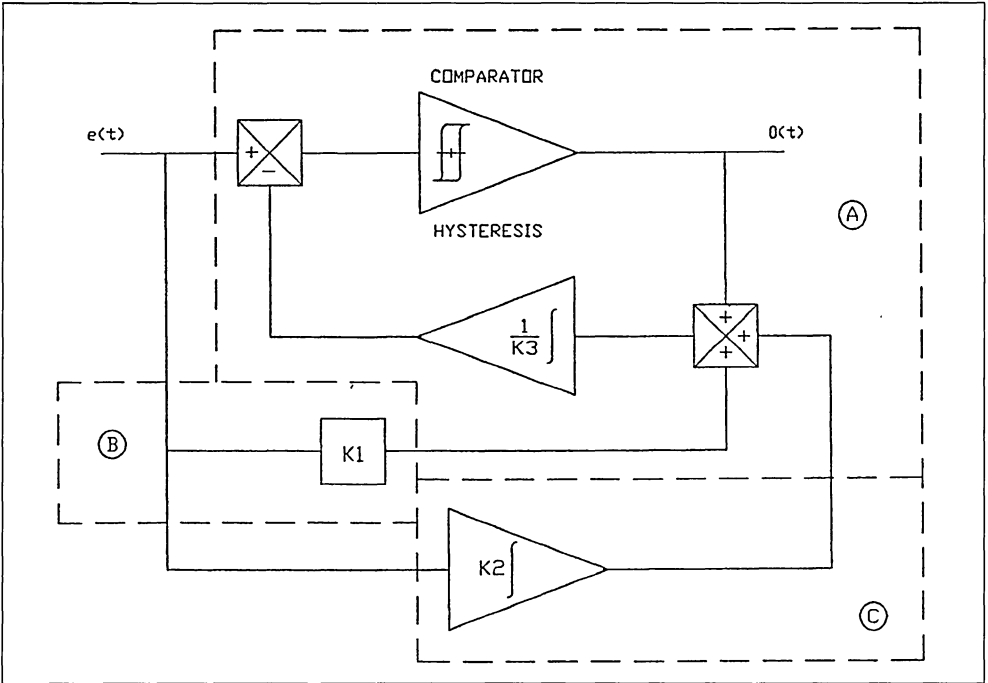


Figure 5 : A PID Controller with Binary Output.



SWITCHING DEVICES FOR A RANGE OF D.C. MOTOR SERVO DRIVES

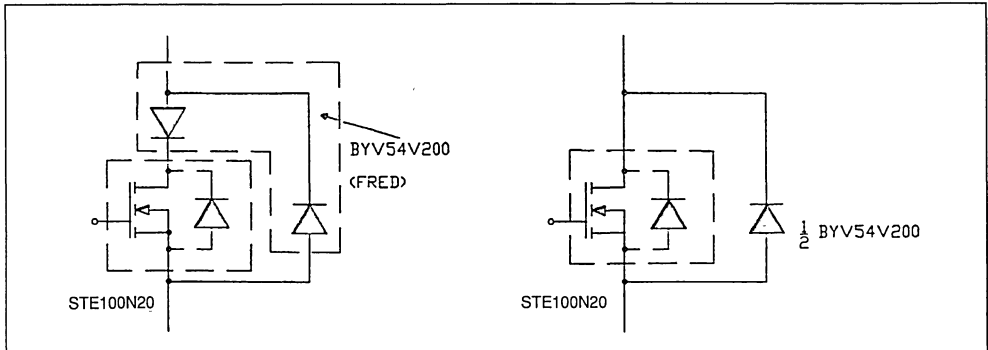
At medium power levels the MOSFET is ideally suited offering high switching speed, ease of paralleling and simple gate drive and protection. SGS-Thomson has introduced a range of MOSFET devices in plastic isolated packages. The 200V devices, summarised in table 2, can be used to design a servo drive range from 600VA to 6kVA without the need to parallel MOSFETs in separate plastic packages.

The MOSFET internal parasitic diode is too slow for applications requiring ultrasonic switching frequen-

cies. Excessive switching losses in the MOSFET can result from the reverse recovery time of the internal parasitic diode (greater than 600ns). Noise is also induced on the supply rails when the conducting diodes reverse recover. Table 2 specifies high efficiency ultra fast recovery epitaxial diodes for freewheeling. These diodes, having a conduction voltage of less than 0.85V at rated nominal current, are ideally suited as MOSFET series blocking diodes used to prevent the conduction of the internal parasitic diode.

Figure 6 illustrates possible techniques for utilizing fast external diodes for the 6kVA brush D.C. motor design.

Figure 6 : 6kVA MOSFET Switch Configurations Using ISOFETs and FREDs.



Manufacture : SGS - THOMSON MICROELECTRONICS					Basic Brush D. C. Motor Drive Spec. Switching Freq. > 20KHz				
Part N° MOSFET	$R_{DS(ON)}$ $T_j = 25^\circ C$ (Ω)	I_D $T_c = 100^\circ C$ (A)	R_{TH} ($^\circ C/W$)	Part N° Diode FRED	V_F at $T_j = 100^\circ C$ (V)	I_F (A)	POWER (VA)	V_{nom} (V)	I_{nom} (A)
IRF640 ¹	0.18	11	1	BYW80PI200	0.85	7	600	120	5
STH33N20 ¹	0.085	20	0.69	BYW81PI200	0.85	12	1200	120	10
STE100N20 ²	0.021	65	0.27	BYV54V200	0.85	50	6000	120	50

Table 2 A range of brush D. C. motor velocity servo drives.

1 - without insulation.

2 - ISOFET . MOSFET chips in parallel in ISOTOP package.

1.2.KVA BRUSH D.C. SERVO DRIVE

Figure 7 illustrates the block diagram of the developed 1.2kVA brush D.C. servo drive. The H-bridge operates at a nominal voltage of 120V_{DC}. The D.C. motor in certain applications is driven by its load and hence is a generator of energy. This regenerative energy causes the HVDC rail voltage to increase as energy is stored in the smoothing capacitors.

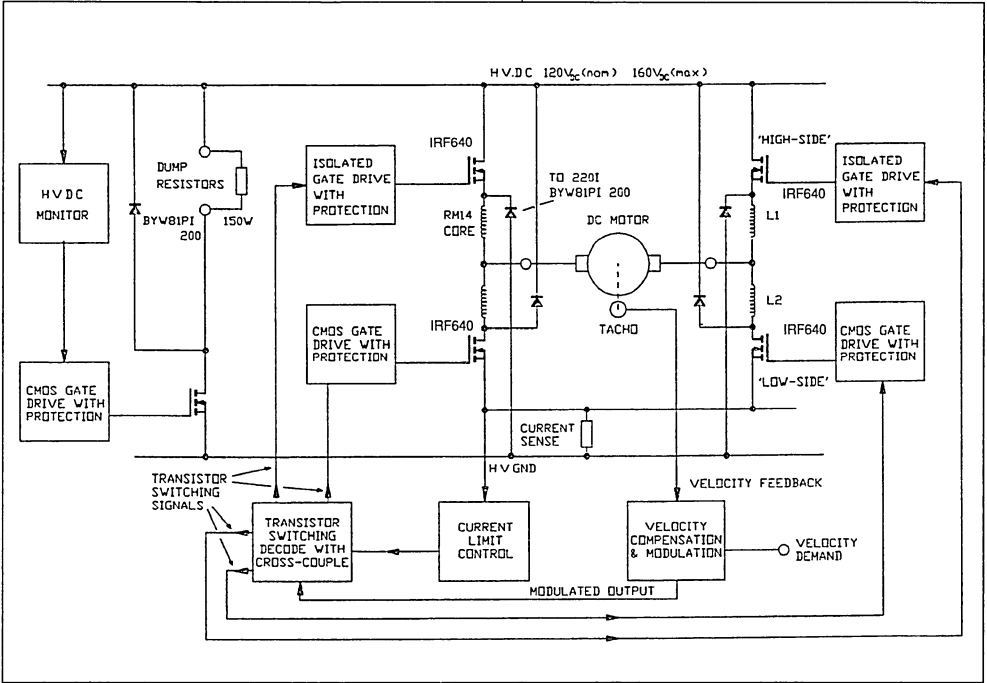
At a maximum voltage of 160V_{DC}, a resistive dump is turned-on to dissipate the regenerative energy and thus limit the HVDC to 160V_{DC}. The drive utilizes the velocity PID controller illustrated previously in figure 5. A current sense resistor is incorporated in the H-bridge to provide load current feedback necessary to limit this load current to the maximum continuous current rating of the drive.

MOSFET based bridge-leg configurations have previously been discussed (reference 2). The bridge-leg utilized comprises of "low-side" and "high-side"

switches connected in series across the HVDC. In this asymmetrical bridge-leg, (illustrated in figure 7), the rate of change of short-circuit current is limited by inductors (L1 and L2 : RM14 cores) which also limit freewheeling current from going through the parasitic diodes of the MOSFETs. At the 10A maximum continuous current rating of the drive, these inductors are still a manageable size. This bridge-leg configuration is capable of withstanding simultaneous conduction of the two devices in the bridge-leg since there are series inductors which reduce the rate of change of drain current. This provides sufficient time for the short-circuit detection loop to operate. The power devices are thus turned-off without being stressed with high rates of change of pulse currents.

At a maximum continuous current rating of 3A, IRF640 MOSFETs and BY81PI200 fast free-wheel diodes plastic packages are optimally rated for the 1.2kVA power stage.

Figure 7 : 1.2 Brush D.C. Motor Velocity Servo Drive (120V_{DC} ; 10A : nom.)



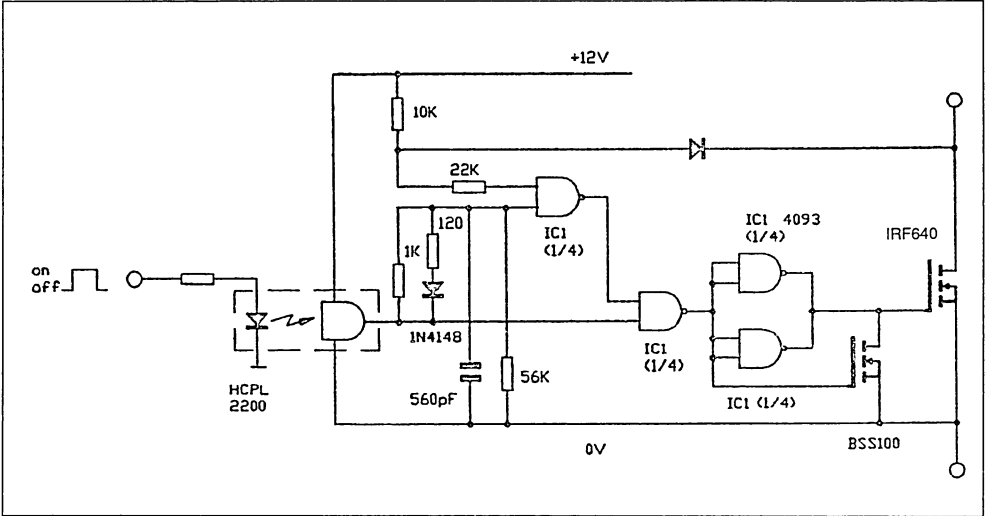
GATE DRIVES AND PROTECTION

Similar gate drives and protection circuits, (illustrated in figure 8), have been used for the "high-side" and "low-side" switches. This CMOS gate drive is well suited as switching speeds of 100 to 250 nano-seconds are sufficient in motor drive applications requiring a switching frequency of around 20 to 30kHz. Monitoring of the drain to source voltage while the device is conducting permits the detection of short-circuit conditions which lead to device failure. The device is turned-off before the drain current reaches a value in excess of the peak pulse current capability of the MOSFET. When the MOSFET is turned-

on the on-state voltage of the device ($V_{DS(on)}$) is compared with a fixed reference voltage of approximately 8V. At the turn-on instant, $V_{DS(on)}$ monitoring is inhibited for a period of approximately 400 nano-seconds in order to allow the MOSFET to turn-on fully. After this period, if $V_{DS(on)}$ is detected to be greater than the fixed reference voltage, the device is latched-off until the control signal is turned-off and turned-on again.

The "high-side" gate drives have isolated low voltage supplies and isolated command signals using high speed opto-couplers.

Figure 8 : An Isolated CMOS Gate Drive with Protection.



MOTOR DRIVE PERFORMANCE

Figure 9 illustrates the dynamic response of the motor drive to a step demand of 4000rpm. The response has been optimised for the no-load case (trace 1). Under heavy load inertia there is an over-

shoot in the velocity response (trace 2). The effects of changing the proportional gain and the integrator time constant of the PID controller can be seen in figures 10 and 11.

Figure 9 : Velocity Response of Motor Drive.

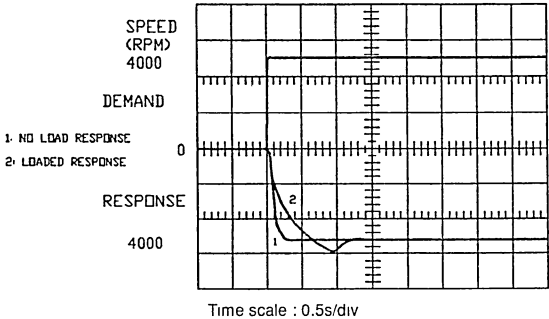


Figure 10 : The Effect Upon the Dynamic Response of the Analogue Velocity Servo System, When the Gain of the Proportional Term in the PID Controller is Varied.

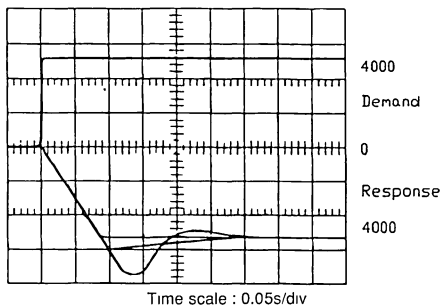
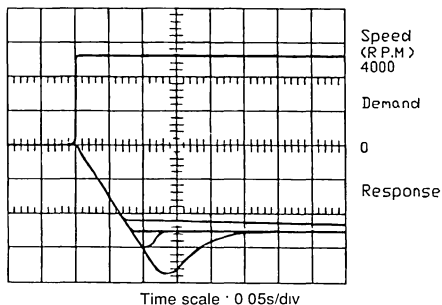


Figure 11 : The Effect Upon the Dynamic Response of the Analogue Velocity Servo System, when the Time Constant of the Integrator in the PID Controller is Varied.



6KVA BRUSH D.C. MOTOR SERVO DRIVE

Figure 12 illustrates the block diagram of the proposed 6kVA (120V_{DC} ; 50A) motor drive using ISO-TOP packages for the MOSFETs in parallel (ISOFET) and the FRED diodes.

Blocking diodes in series with the MOSFETs are proposed to prevent the MOSFET internal parasitic diodes from conducting. The asymmetrical bridge-leg configuration is not a cost-effective solution since inductors rated for 50A continuous operation are large and expensive. The series blocking diode has to be an ultra fast high voltage type. If the transistor F2 (shown in figure 12) is conducting, the drain to source capacitance of the transistor F1 is charged to the HVDC voltage. If F2 is turned-off, the load current transfers from F2 to the free-wheel diode, D1. Consequently the series blocking diode, D2, supports the drain to source capacitance voltage of F1 (equal to HVDC) provided this capacitance is not discharged by turning-on F1.

An isolated D.C. current measurement device, (such as an Hall-effect current sensor, LT80-P, manufactured by LEM), is recommended for the measurement of load current necessary for current limit control.

Pulse transformer based floating gate drives illustrated in figure 13 can be used for the STE100N20 ISOFETs. The pulse transformer is used to transmit simultaneously the ISOFET logic command signal together with the gate to source capacitance charging current. The current mirror technique (reference 2) is used to provide short-circuit and overload current protection. The pulse transformer operates at an oscillating frequency of 1MHz when a turn-on control signal is present. The secondary is rectified to provide gate source capacitance voltage. The current mirror provides a voltage "image" of the main drain current. This voltage is compared with a fixed reference voltage in order that the gate drive be latched-off whenever the drain current exceeds the specified overload current level.

Figure 12 : 6kVA Brush D.C. Motor Velocity Servo Drive (120V_{bc} ; 50A : nom.).

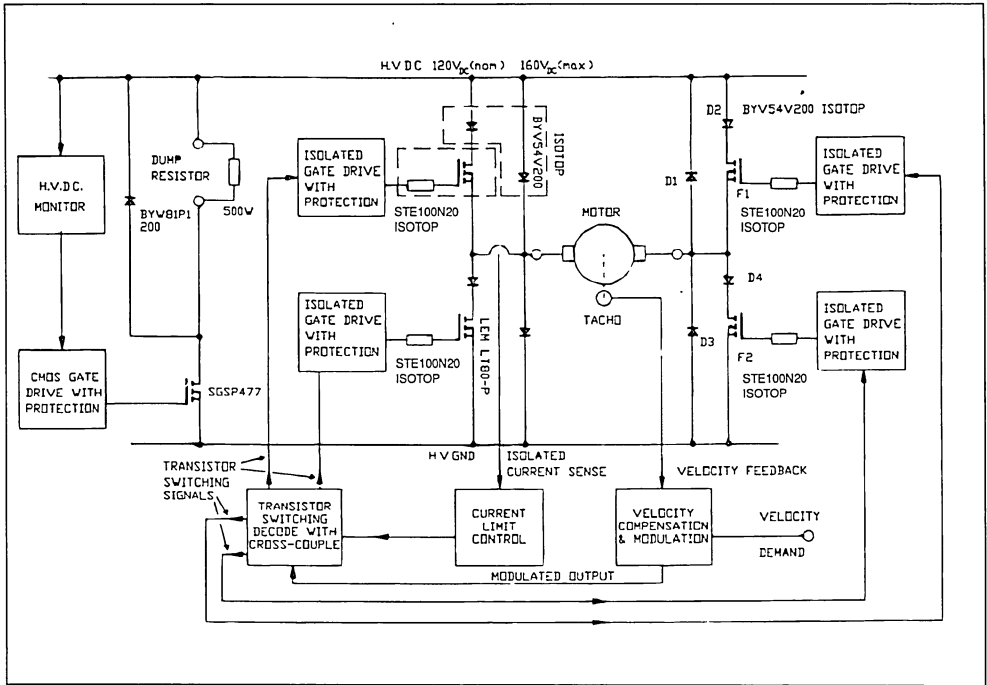
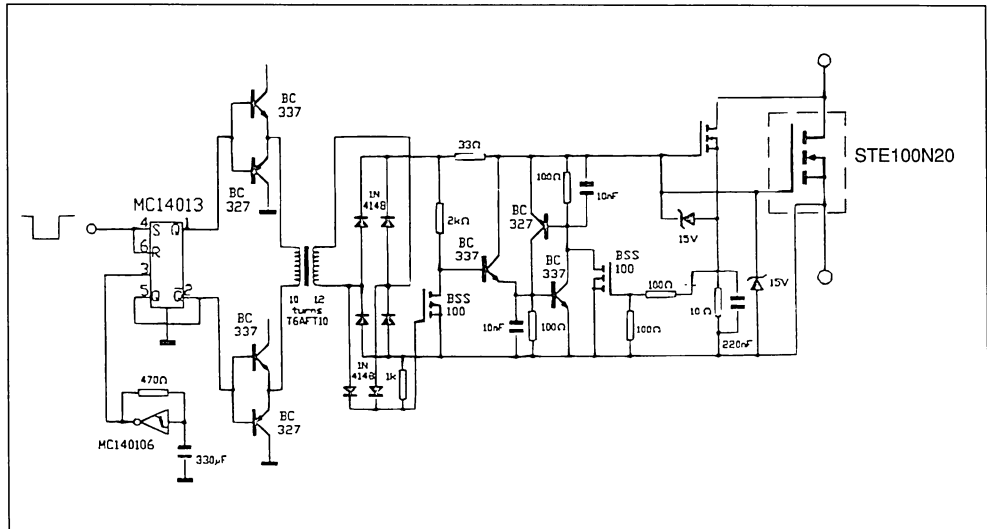


Figure 13 : Pulse Transformer Gate Drive with Current Mirror Protection for a STE100N20.

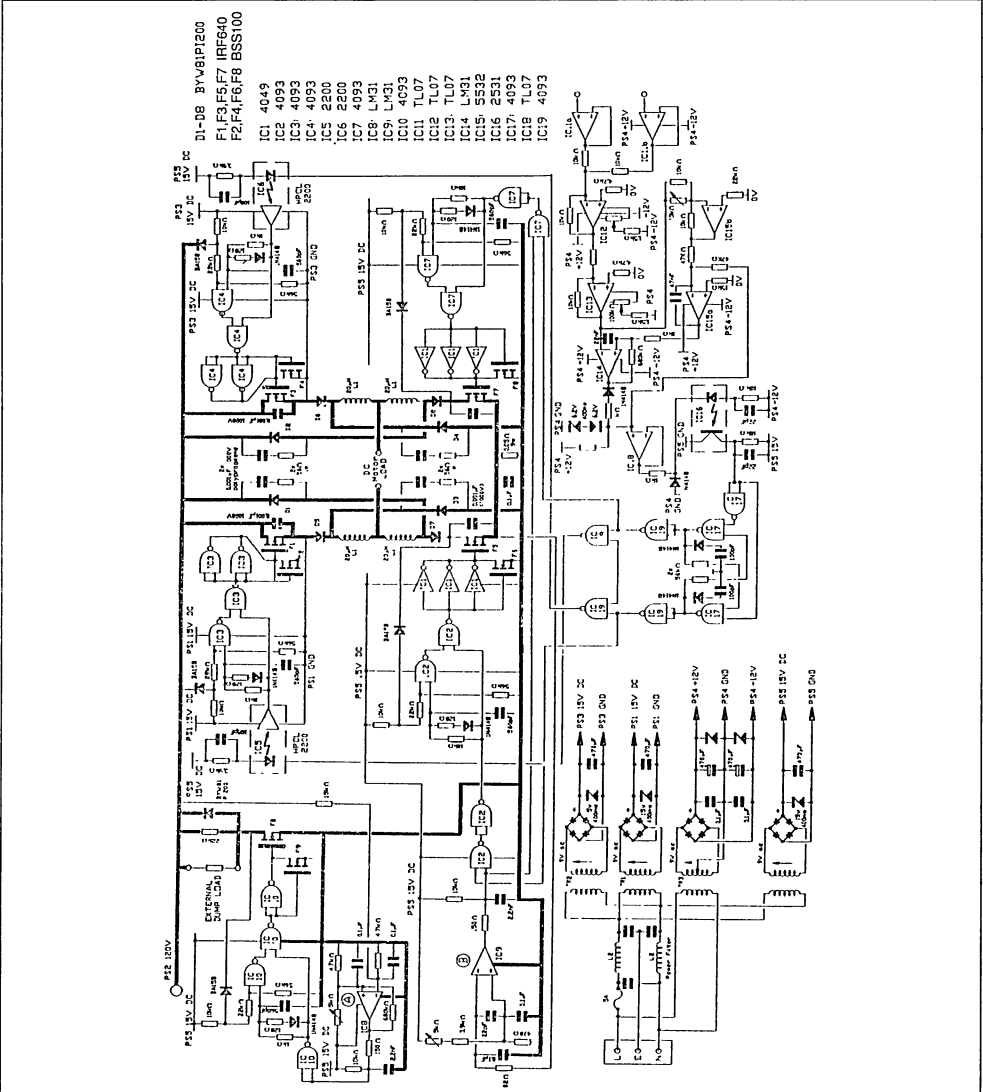


CONCLUSION

MOSFET based brush D.C. motor velocity servo drives have been described, with particular emphasis placed on the bridge-leg configuration, the PID compensation and modulation, the gate drive and protection techniques. The PID compensation and modulation circuits require few components to achieve good velocity servo performance.

The development has led to a compact high performance 1.2kVA drive which is fully protected against output short-circuit conditions. A 6kVA motor drive is proposed using ISONETs. MOSFET switching devices and their associated free-wheel and blocking diodes have been specified for a range of brush D.C. motor drives rated between 600VA to 6kVA without the need to parallel MOSFETs in separate plastic packages.

Figure 14 : 1.2kVA Switched-mode Motor Drive.



STEPPER MOTOR DRIVING

By H. SAX

Dedicated integrated circuits have dramatically simplified stepper motor driving. To apply these ICs designers need little specific knowledge of motor driving techniques, but an understanding of the basics will help in finding the best solution. This note explains the basics of stepper motor driving and describes the drive techniques used today.

From a circuit designer's point of view stepper motors can be divided into two basic types : unipolar and bipolar.

A stepper motor moves one step when the direction of current flow in the field coil(s) changes, reversing the magnetic field of the stator poles. The difference between unipolar and bipolar motors lies in the way that this reversal is achieved (figure 1) :

Figure 1a : BIPOLAR - with One Field Coil and Two Chargeover Switches That are Switched in the Opposite Direction.

Figure 1b : UNIPOLAR - with Two Separate Field Coils and are Chargeover Switch.

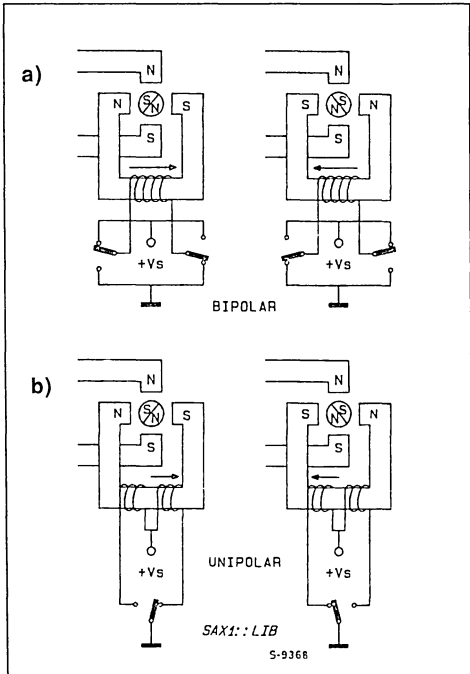
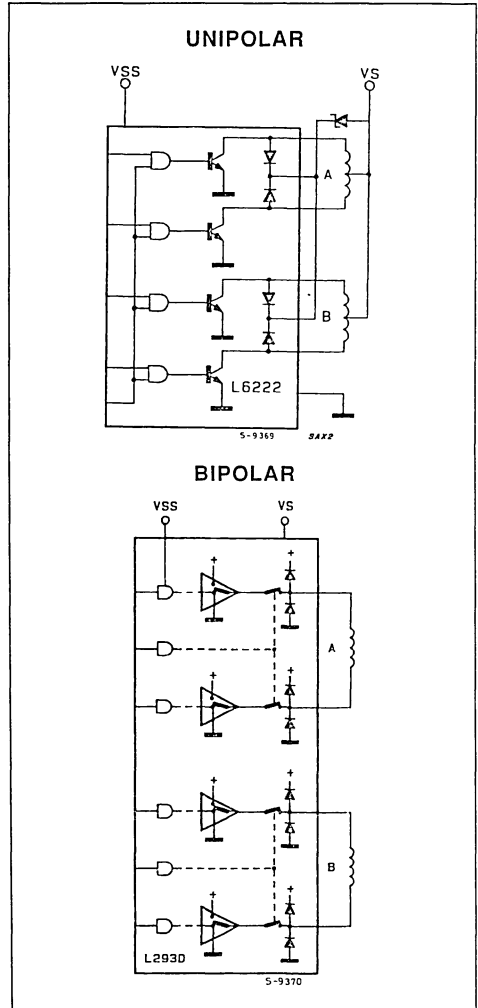


Figure 2 : ICs for Unipolar and Bipolar Driving.



APPLICATION NOTE

The advantage of the bipolar circuit is that there is only one winding, with a good bulk factor (low winding resistance). The main disadvantages are the two changeover switches because in this case more semiconductor are needed.

The unipolar circuit needs only one changeover switch. Its enormous disadvantage is, however, that a double bifilar winding is required. This means that at a specific bulk factor the wire is thinner and the resistance is much higher. We will discuss later the problems involved.

Unipolar motors are still popular today because the drive circuit appears to be simpler when implemented with discrete devices. However with the integrated circuits available today bipolar motors can be driven with no more components than the unipolar motors. Figure 2 compares integrated unipolar and bipolar devices.

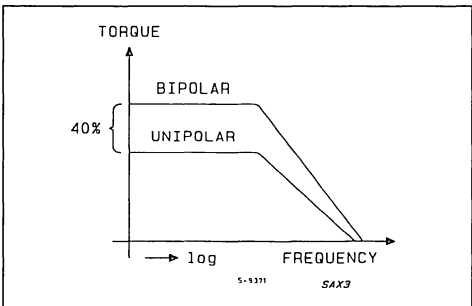
BIPOLAR PRODUCES MORE TORQUE

The torque of the stepper motor is proportional to the magnetic field intensity of the stator windings. It may be increased only by adding more windings or by increasing the current.

A natural limit against any current increase is the danger of saturating the iron core. Though this is of minimal importance. Much more important is the maximum temperature rise of the motor, due to the power loss in the stator windings. This shows one advantage of the bipolar circuit, which, compared to unipolar systems, has only half of the copper resistance because of the double cross section of the wire. The winding current may be increased by the factor $\sqrt{2}$ and this produces a direct proportional affect on the torque. At their power loss limit bipolar motors thus deliver about 40 % more torque (fig. 3) than unipolar motors built on the same frame.

If a higher torque is not required, one may either reduce the motor size or the power loss.

Figure 3 : Bipolar Motors Driver Deliver More Torque than Unipolars.



CONSTANT CURRENT DRIVING

In order to keep the motor's power loss within a reasonable limit, the current in the windings must be controlled.

A simple and popular solution is to give only as much voltage as needed, utilizing the resistance (R_L) of the winding to limit the current (fig. 4a). A more complicated but also more efficient and precise solution is the inclusion of a current generator (fig. 4b), to achieve independence from the winding resistance. The supply voltage in Fig. 4b has to be higher than the one in Fig. 4a. A comparison between both circuits in the dynamic load/working order shows visible differences.

Figure 4 : Resistance Current Limiter (a) and Current Generator Limiting.

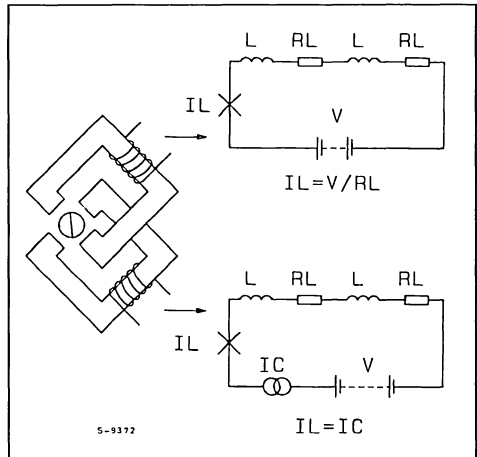
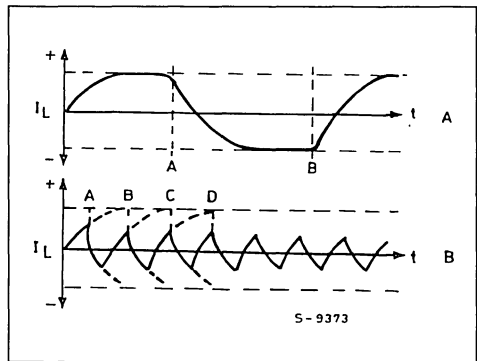


Figure 5 : At High Step Frequencies the Winding Current cannot Reach its Setting Value because of the Continuous Direction Change.



It has already been mentioned that this power of the motor is, among others, proportional to the winding current.

In the dynamic working order a stepper motor changes poles of the winding current in the same stator winding after two steps. The speed with which the current changes its direction in the form of an exponential function depends on the specified inductance, the coil resistance and on the voltage. Fig. 5a shows that at a low step rate the winding current I_L reaches its nominal value V_L/R_L before the direction is changed. However, if the poles of the stator windings are changed more often, which corresponds to a high step frequency, the current no longer reaches its saturating value because of the limited change time ; the power and also the torque diminish clearly at increasing number of revolutions (fig. 5).

MORE TORQUE AT A HIGHER NUMBER OF REVOLUTIONS

Higher torque at faster speeds are possible if a current generator as shown in Fig. 4b is used. In this application the supply voltage is chosen as high possible to increase the current's rate of change. The current generator itself limits only the phase current and becomes active only the moment in which the coil current has reached its set nominal value. Up to this value the current generator is in saturation and the supply voltage is applied directly to the winding.

Fig. 6, shows that the rate of the current increase is now much higher than in Figure 5. Consequently at higher step rates the desired current can be maintained in the winding for a longer time. The torque decrease starts only at much higher speeds.

Fig. 7 shows the relation between torque and speed in the normal graphic scheme, typical for the stepper motor. It is obvious that the power increases in the upper torque range where it is normally needed, as the load to be driven draws most energy from the motor in this range.

EFFICIENCY - THE DECISIVE FACTOR

The current generator combined with the high supply voltage guarantees that the rate of change of the current in the coil is sufficiently high.

At the static condition or at low numbers of revolutions, however, this means that the power loss in the current generator dramatically increases, although the motor does not deliver any more energy in this range ; the efficiency factor is extremely bad.

Help comes from a switched current regulation using the switch-transformer principle, as shown in

fig. 8. The phase winding is switched to the supply voltage until the current, detected across R_s , reaches the desired nominal value. At that moment the switch, formerly connected to $+V_s$, changes position and shorts out the winding. In this way the current is stored, but it decays slowly because of inner winding losses. The discharge time of the current is determined during this phase by a monostable or pulse oscillator. After this time one of the pole changing switches changes back to $+V_s$, starting an induction recharge and the clock-regulation-cycle starts again.

Figure 6 : With a Step Current Slew, it is not a Problem to Obtain, even at High Step frequencies Sufficient Current in Windings.

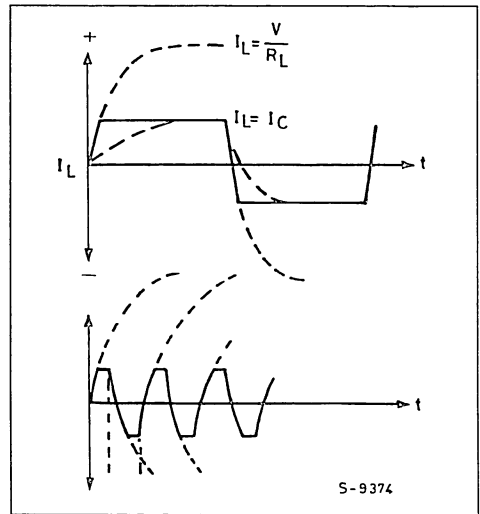
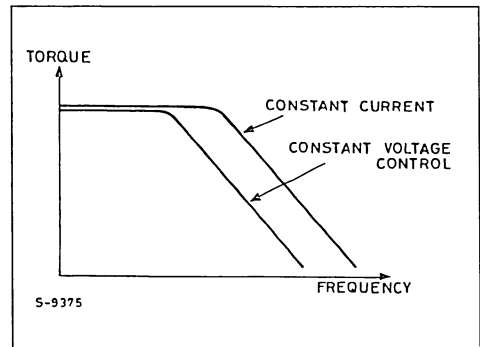


Figure 7 : Constant Current Control of the Stepper Motor Means more Torque at High Frequency.



Since the only losses in this technique are the saturation loss of the switch and that of the coil resistance, the total efficiency is very high.

The average current that flows from the power supply line is less than the winding current due to the concept of circuit inversion. In this way also the power unit is discharged. This kind of phase current control that has to be done separately for each motor phase leads to the best ratio between the supplied electrical and delivered mechanical energy.

POSSIBLE IMPROVEMENTS OF THE UNIPOLAR CIRCUIT

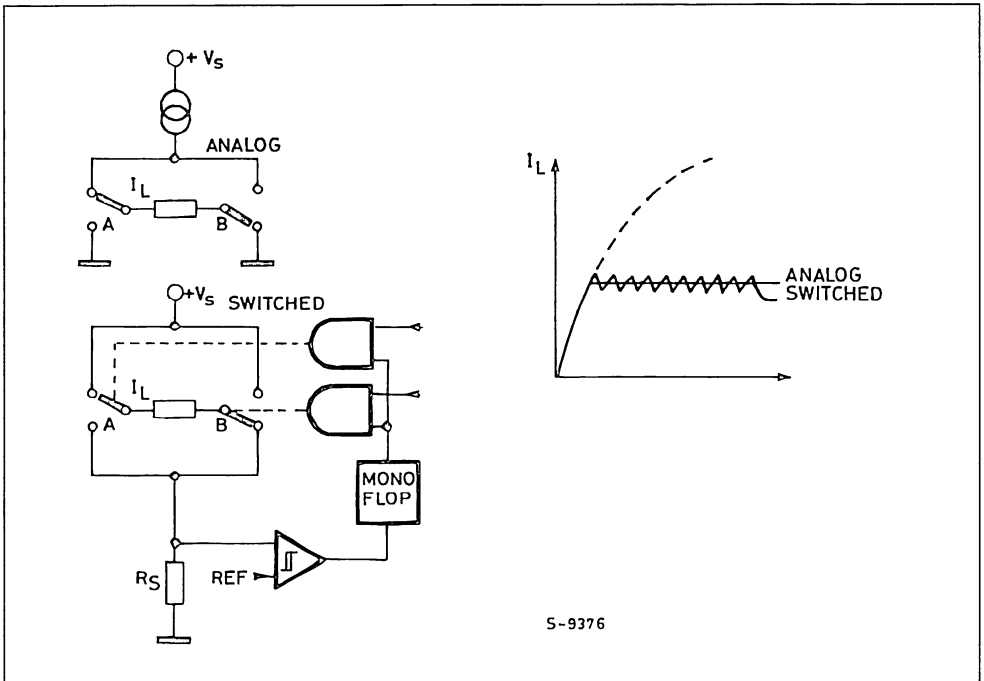
It would make no sense to apply the same principle to a stabilized current controlled unipolar circuit, as two more switches per phase would be necessary for the shortening out of the windings during the free phase and thus the number of components would be the same as for the bipolar circuit ; and more-

over, there would be the well known torque disadvantage.

From the economic point of view a reasonable and justifiable improvement is the "Bi-Level-Drive" (fig. 9). This circuit concept works with two supply voltages ; with every new step of the motor both windings are connected for a short time to a high supply voltage. This considerably increases the current rate of change and its behaviour corresponds more or less to the stabilized power principle. After a pre-determined the switch opens, a no a lower supply voltage is connected to the winding thru a diode.

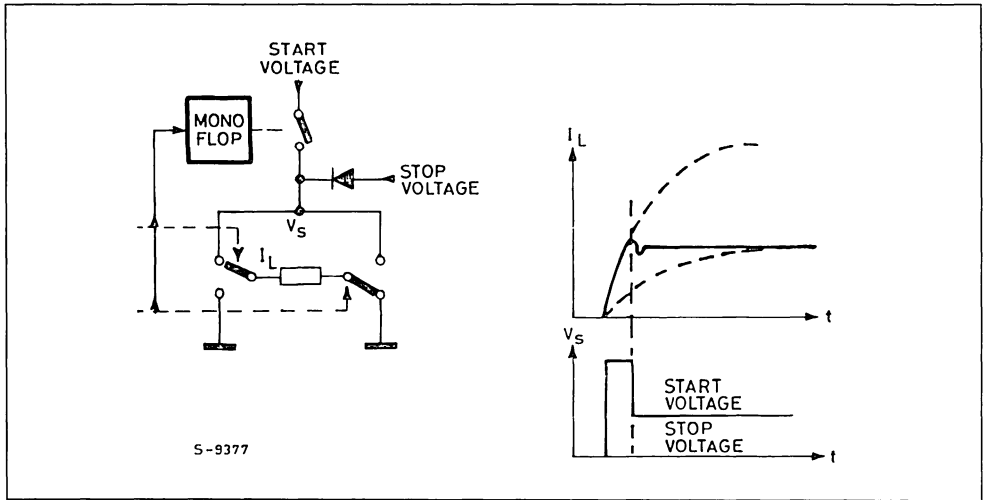
This kind of circuit by no means reaches the performance of the clocked stabilized power control as per fig. 8, as the factors : distribution voltage oscillation, B.e.m.f., thermal winding resistance, as well as the separate coil current regulation are not considered, but it is this circuit that makes the simple unipolar R/L-control suitable for many fields of application.

Figure 8 : With Switch Mode Current Regulation Efficiency is Increased.



S-9376

Figure 9 : At Every New Step of the Motor, it is Possible to Increase the Current Rate with a Bilevel Circuit.



ADVANTAGES AND DISADVANTAGES OF THE HALF-STEP

An essential advantage of a stepper motor operating at half-step conditions is its position resolution increased by the factor 2. From a 3.6 degree motor you achieve 1.8 degrees, which means 200 steps per revolution.

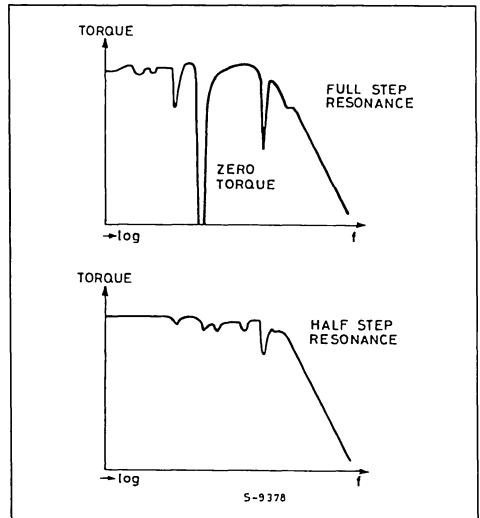
This is not always the only reason. Often you are forced to operate at half-step conditions in order to avoid that operations are disturbed by the motor resonance. These may be so strong that the motor has no more torque in certain step frequency ranges and loses completely its position (fig. 10). This is due to the fact that the rotor of the motor, and the changing magnetic field of the stator forms a spring-mass-system that may be stimulated to vibrate. In practice, the load might deaden this system, but only if there is sufficient frictional force.

In most cases half-step operation helps, as the course covered by the rotor is only half as long and the system is less stimulated.

The fact that the half-step operation is not the dominating or general solution, depends on certain disadvantages :

- the half-step system needs twice as many clock-pulses as the full-step system ; the clock-frequency is twice as high as with the full-step.
- in the half-step position the motor has only about half of the torque of the full-step.

Figure 10 : The Motor has no More Torque in Certain Step Frequency Ranges with Full Step Driving.



For this reason many systems use the half-step operation only if the clock-frequency of the motor is within the resonance risk area.

The dynamic loss is higher the nearer the load moment comes to the limit torque of the motor. This effect decreases at higher numbers of revolutions.

TORQUE LOSS COMPENSATION IN THE HALF-STEP OPERATION

It's clear that, especially in limit situations, the torque loss in half-step is a disadvantage. If one has to choose the next larger motor or one with a double resolution operating in full-step because of some insufficient torque percentages, it will greatly influence the costs of the whole system.

In this case, there is an alternative solution that does not increase the costs for the bipolar chopping stabilized current drive circuit.

The torque loss in the half-step position may be compensated for by increasing the winding current by the factor $\sqrt{2}$ in the phase winding that remains active. This is also permissible if, according to the motor data sheet, the current limit has been reached, because this limit refers always to the contemporary supply with current in both windings in the full-step position. The factor $\sqrt{2}$ increase in current doubles the stray power of the active phase. The total dissipated power is like that of the full-step because the non-active phase does not dissipate power.

The resulting torque in the half-step position amounts to about 90 % of that of the full-step, that means dynamically more than 95 % torque compared to the pure full-step ; a neglectable factor.

The only thing to avoid is stopping the motor at limit current conditions in a half-step position because it would be like a winding thermal phase overload concentrated in one.

The best switch-technique for the half-step phase current increase will be explained in detail later on Fig. 11 shows the phase current of a stepping motor in half-step control with an without phase current increase and the pertinent curves of step frequency and torque.

Figure 11 : Half Step Driving with Shaping Allows to Increase the Motor's Torque- to about 95 % of that of the Full Step.

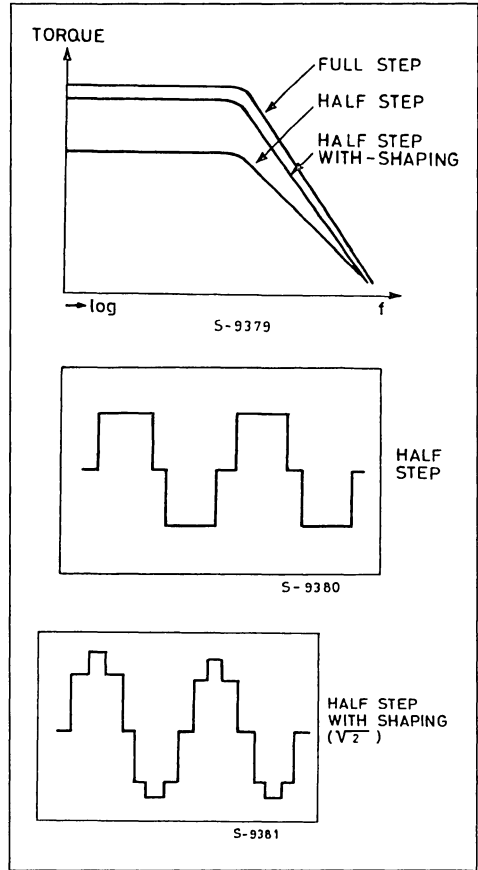
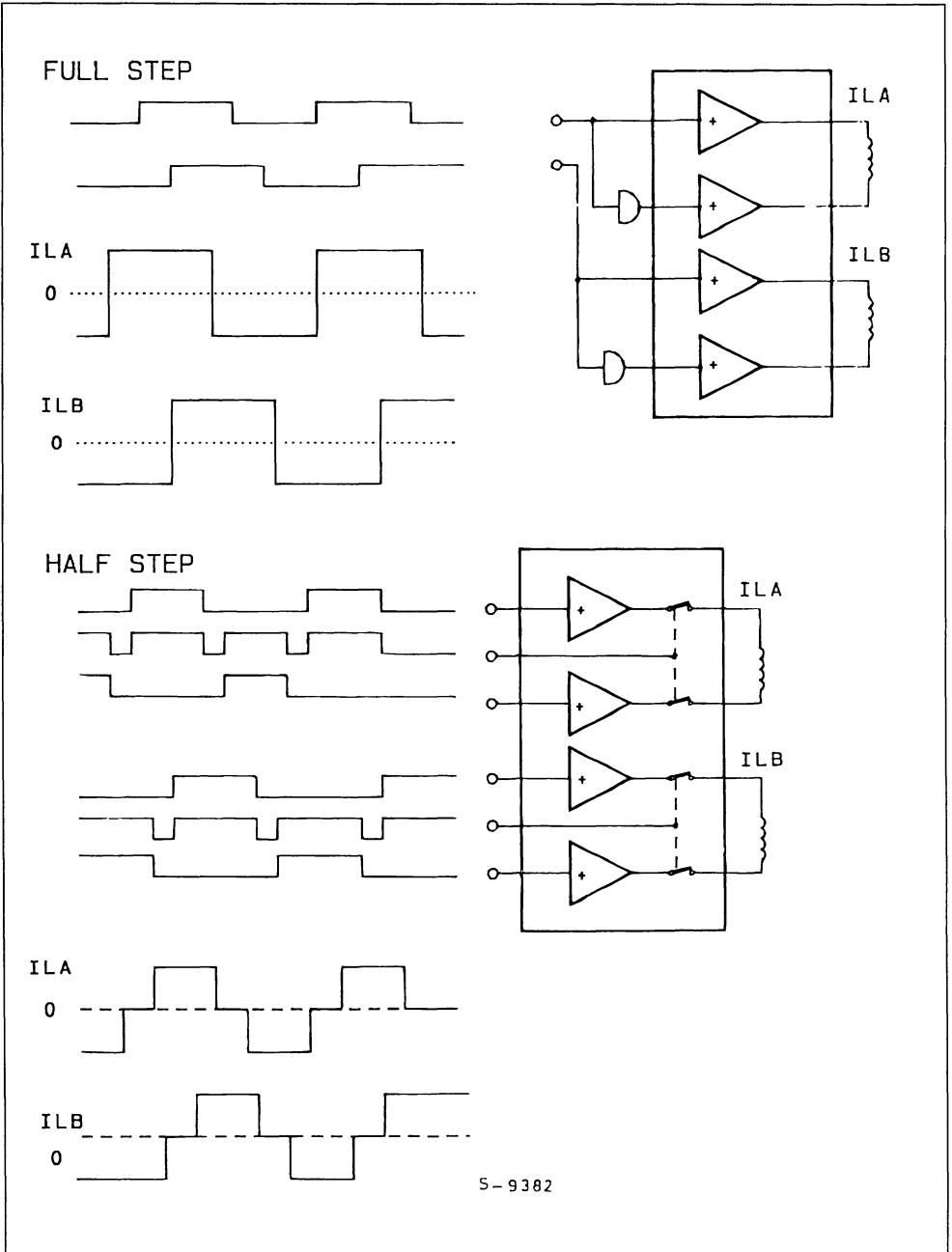


Figure 12 : Only Two Signals for Full Step Driving are Necessary while Four (six if three-state is needed on the output stages) for half Step.



APPLICATION NOTE

DRIVE SIGNALS FOR THE MICRO ELECTRONIC

A direct current motor runs by itself if you supply it with voltage, whereas the stepping motor needs the commutation signal in form of several separated but linkable commands. In 95 % of the applications today, the origin of these digital commands is a microprocessor system.

In its simplest form, a full-step control needs only two rectangular signals in quadrature. According to which phase is leading, the motor axis rotates clockwise or counter-clockwise, whereby the rotation speed is proportional to the clock frequency.

In the half-step system the situation becomes more complicated. The minimal two control signals become four control signals. In some conditions as many as six signals are needed. If the Tri-state-command for the phase ranges without current, necessary for high motor speeds, may not be obtained from the 4 control signals. Fig. 12 shows the relationship between the phase current diagram and the control signal for full and half-step.

Since all signals in each mode are in defined relations with each other, it is possible to generate them using standard logic. However, if the possibility to

choose full and half-step is desired, a good logic implementation becomes quite expensive and an application specific integrated circuit would be better. Such an application specific integrated circuit could reduce the number of outputs required from a microprocessor from the 6 required to 3 static and dynamic control line.

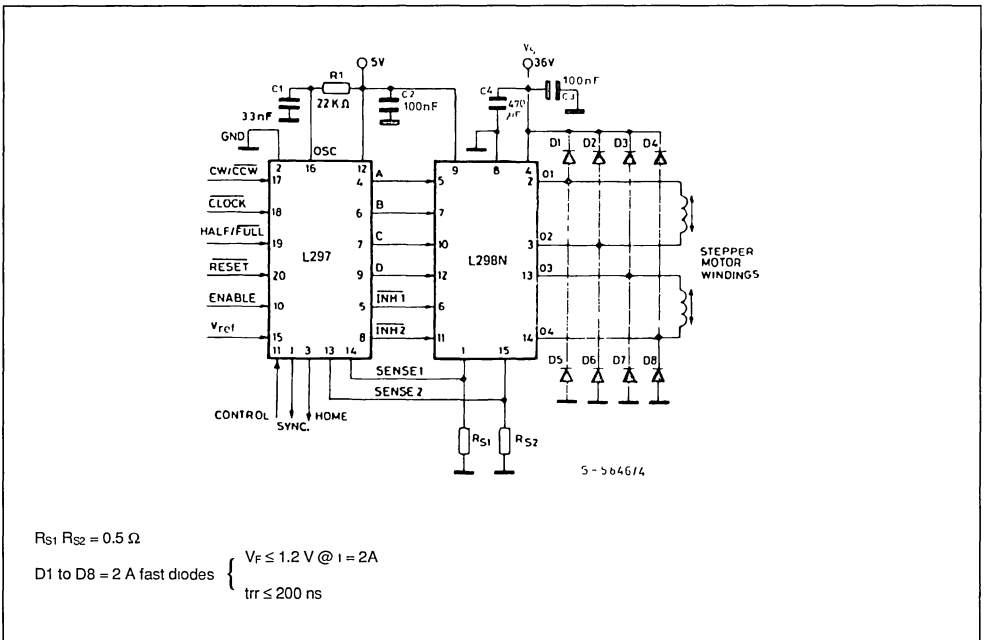
A typical control circuit that meets all these requirements is the L297 unit (fig. 13).

Four signals control the motor in all operations :

1. CLOCK : The clock signal, giving the stepping command
2. RESET : Puts the final level signals in a defined start position
3. DIRECTION : Determines the sense of rotation of the motor axis.
4. HALF/FULL : Decides whether to operate in full or in half-step.

Another inhibit input allows the device to switch the motor output into the Tri-state-mode in order to prevent undesired movements during undefined operating conditions, such as those that could occur during.

Figure 13 : The L297 avoids the Use of Complicated Standard Logic to Generate Both Full and Half-step Driving Signals Together with Chopper Current Control.



SWITCH-MODE CURRENT REGULATION

The primary function of the current regulation circuit is to supply enough current to the phase windings of the motor, even at high step rates.

The functional blocks required for a switchmode current control are the same blocks required in switching power supplies ; flip-flops, comparators ; and an oscillator are required. These blocks can easily be included in the same IC that generates the phase control signals. Let us consider the implementation of chopper current control in the L297.

The oscillator on pin 16 of the L297 resets the two flip-flops at the start of each oscillator period. The flip-flop outputs are then combined with the outputs of the translator circuit to form the 6 control signals supplied to the power bridge (L298).

When activated, by the oscillator, the current in the winding will raise, following the L/R time constant curve, until the voltage across the sense resistor (pin 1, 15 of L298) is equal to the reference voltage input (pin 15, L297) the comparator then sets the flip-flop, causing the output of the L297 to change to an equiphase condition, thus effectively putting a short circuit across the phase winding. The bridge is activated into a diagonally conductive state when the oscillator resets the flip-flop at the start of the next cycle.

Using a common oscillator to control both current regulators maintains the same chopping frequency for both, thus avoiding interference between the two.

The functional block diagram of the L297 and the power stage (L298) are shown in Figure 14 along with the operating wave forms.

An important characteristics of this circuit implementation is that, during the reset time, the flip-flops are kept reset. The reset time can be selected by selecting the impedance of the R/C network or pin 16. In

this way, the current spike and noise across the sense resistors that may occur during switching will not cause a premature setting of the flip-flop. Thus the recovery current spike of the protection diodes can be ignored and a filter in the sense line is avoided.

THE RIGHT PHASE CURRENT FOR EVERY OPERATING CONDITION

The Chopper principle of the controller unit reveals that the phase current in the motor windings is controlled by two data : the reference voltage at pin 15 of the controller and the value of the sense resistance at pins 1 and 15 of the L298, that is $I_L = V_{REF}/R_s$. By changing V_{REF} it is very easy to vary the current within large limits. The only question is for which purpose and at which conditions.

More phase current means more motor torque, but also higher energy consumption.

An analysis of the torque consumption for different periods and load position changes shows that there is no need for different energies.

There is a high energy need during the acceleration or break phases, whereas during continuous operation or neutral or stop position less energy has to be supplied. A motor with its phase current continuously oriented at the load moment limit, even with the load moment lacking, consumes needlessly energy, that is completely transformed into heat.

Therefore it is useful to resolve the phase current in at least two levels controllable from the processor. Fig. 18 shows a minimal configuration with two resistance and one small signal transistor as change-over switch for the reference input. With another resistance and transistor it is possible to resolve 2 Bits and consequently 4 levels. That is sufficient for all imaginable causes.

Fig. 16 shows a optimal phase current diagram during a positioning operation.

Figure 14 : Two ICs and very Few External Components Provide Complete Microprocessor to Bipolar Step- per Motor Interface.

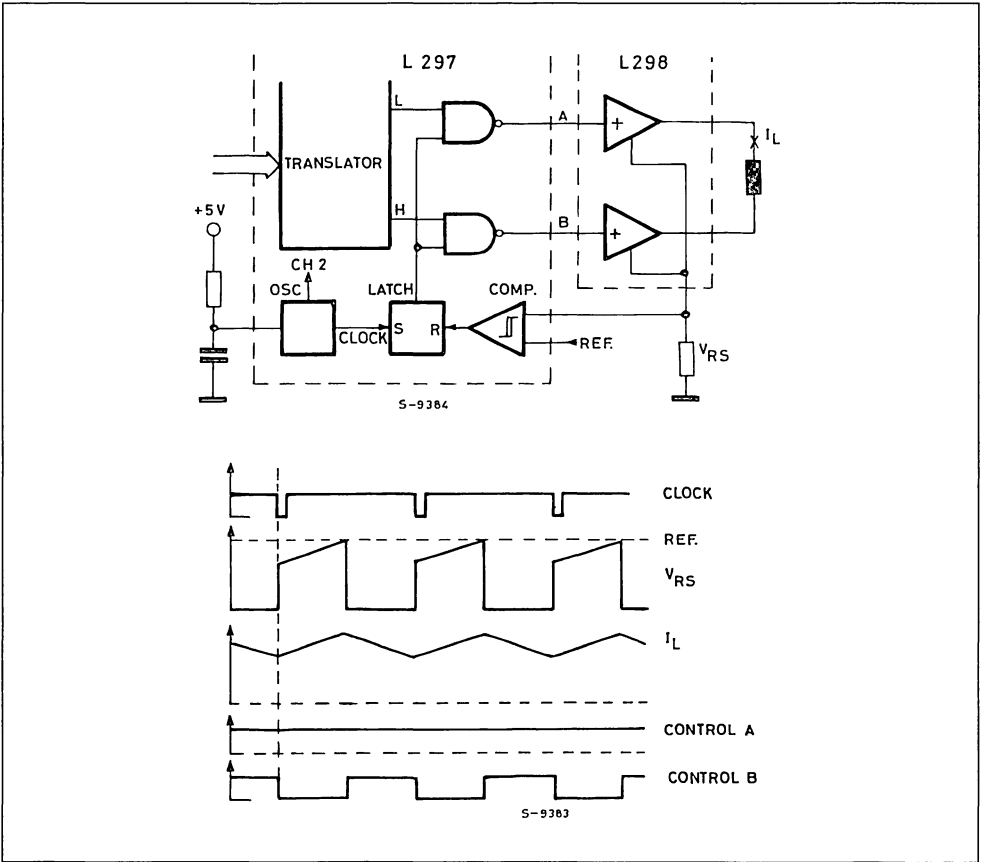


Figure 15 : Because of the Set-dominant Latch Inside the L297 it is Possible to Hide Current Spikes and Noise Across the Sense Resistors thus Avoiding External Filters.

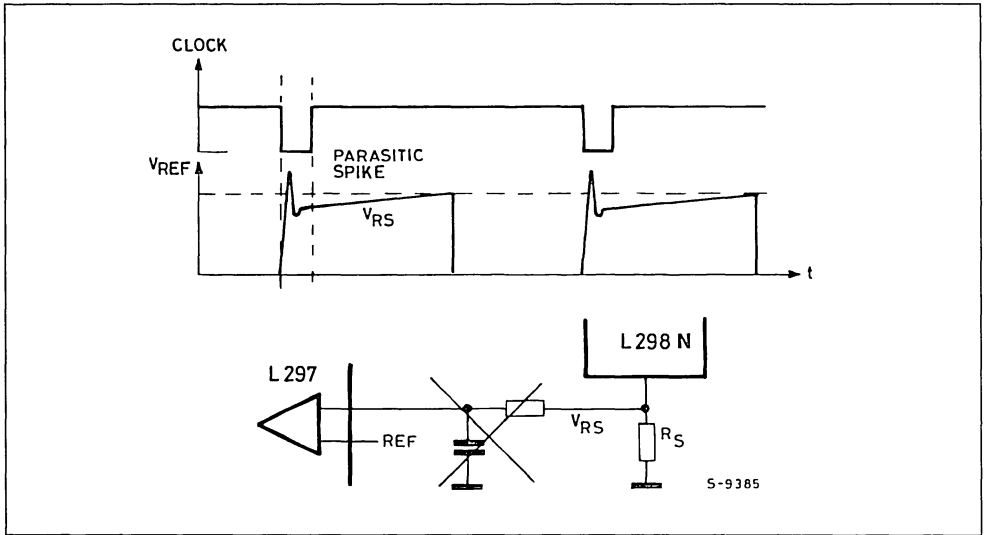
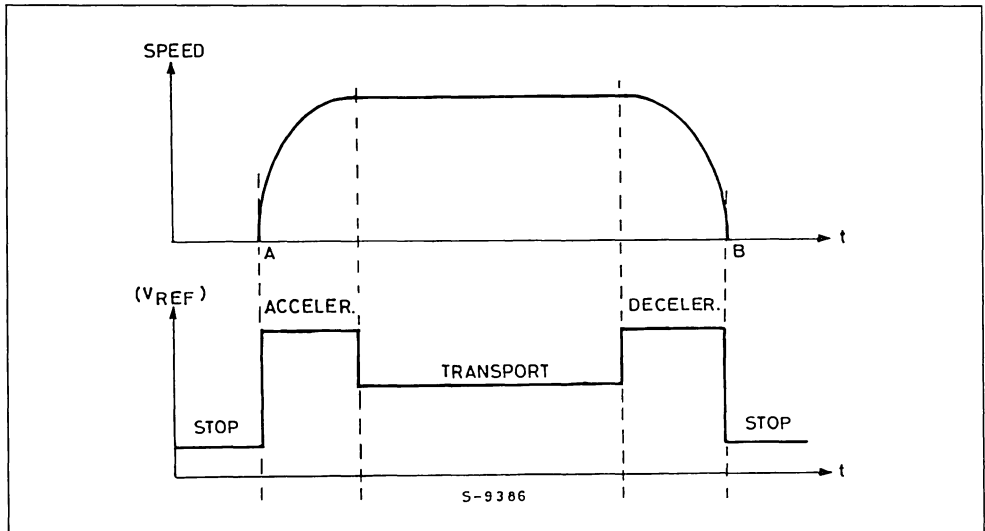


Figure 16 : More Energy is needed During The Acceleration and break Phases Compared the Continuous Operation, Neutral or Stop Position.



HIGH MOTOR CLOCK RESETS IN THE HALF-STEP SYSTEM

In the half-step position one of the motor phases has to be without current. If the motor moves from a full-step position into a half-step position, this means that one motor winding has to be completely discharged. From the logic diagram this means for the high level bridge an equivalent status of the input signals A/B, for example in the HIGH-status. For the coil this means short circuit (fig. 17 up) and consequently a low reduction of the current. In case of high half-step speeds the short circuit discharge time constant of the phase winding is not sufficient to discharge the current during the short half-step

phases. The current diagram is not neat, the half step is not carried out correctly (fig. 17 center).

For this reason the L297 controller-unit generates an inhibit-command for each phase bridge, that switches the specific bridge output in the half-step position into Tri-state. In this way the coil can start swinging freely over the external recovery diodes and discharge quickly. The current decrease rate of change corresponds more or less to the increase rate of change (fig. 17 below).

In case of full-step operation both inhibit-outputs of the controller (pin 5 and 8) remain in the HIGH-status.

Figure 17 : The Inhibit Signal Turns Off Immediately the Output Stages Allowing thus a Faster Current Decay (mandatory with half-step operation).

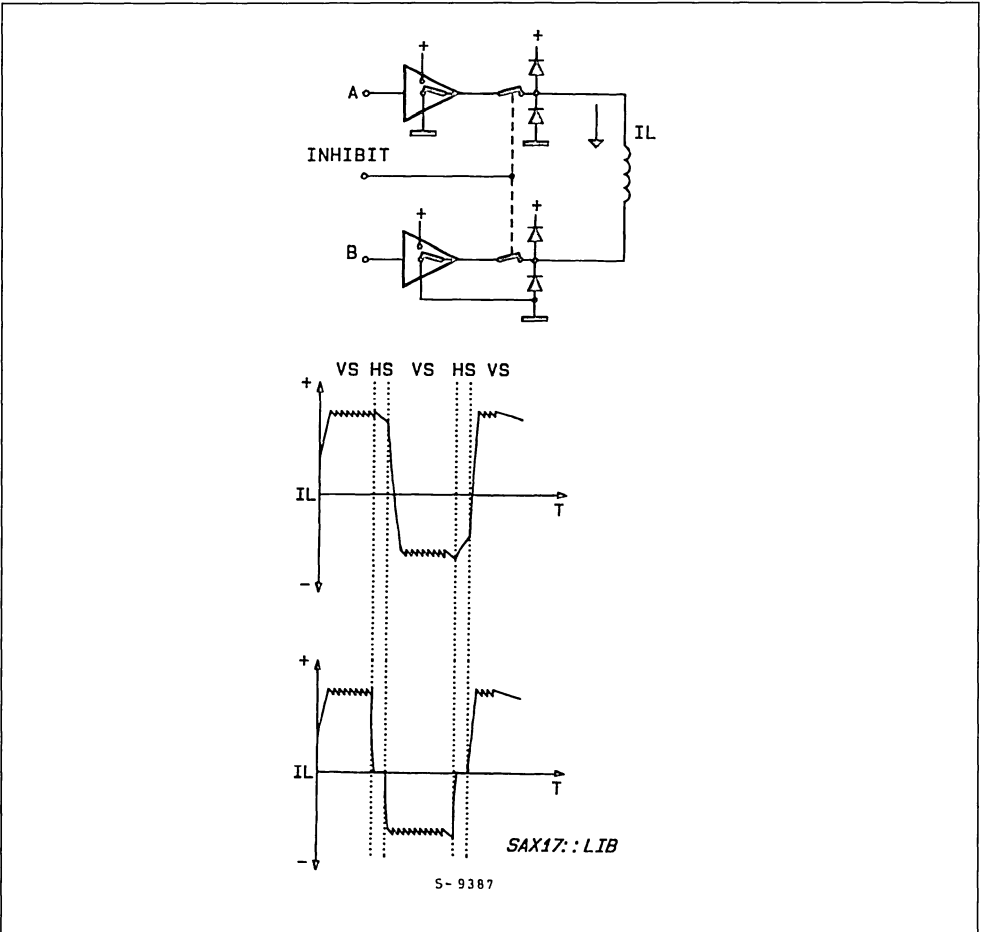
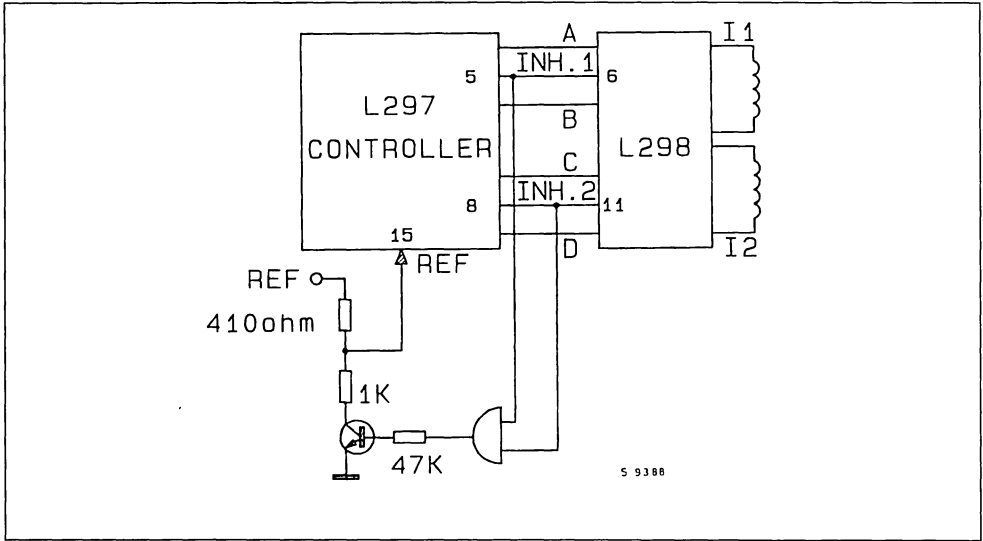


Figure 18 : With This Configuration it is Possible to Obtain Half-step with Shaping Operation and Therefore More Torque.



MORE TORQUE IN THE HALF-STEP POSITION

A topic that has already been discussed in detail. So we will limit our considerations on how it is carried out, in fact quite simply because of the reference voltage controlled phase current regulation.

With the help of the inhibit-signals at outputs 5 and 8 of the controller, which are alternatively active only when the half-step control is programmed, the reference voltage is increased by the factor 1.41 with a very simple additional wiring (fig. 18), as soon as one of the two inhibit-signals switches LOW. This increases the current in the active motorphase proportionally to the reference voltage and compensates the torque loss in this position. Fig. 19 shows clearly that the diagram of the phase current is almost sinusoidal, in principle the ideal form of the current graph.

To sum up we may say that this half-step version offers most advantages. The motor works with poor resonance and a double position resolution at a torque, that is almost the same as that of the full-step.

BETTER GLIDING THAN STEPPING

If a stepper motor is supposed to work almost gliding and not step by step, the form of the phase current diagram has to be sinusoidal.

The advantages are very important :

- no more phenomena of resonance
- drastic noise reduction
- connected gearings and loads are treated with care
- the position resolution may be increased further.

However, the use of the L297 controller-unit described until now is no longer possible of the more complicated form of the phase current diagram the Controller may become simpler in its functions.

Fig. 20 shows us an example with the L6505 unit. This IC contains nothing more than the clocked phase current regulation which works according to the same principle as L297. The four control signals emitting continuously a full-step program are now generated directly by the microprocessor. In order to obtain a sinusoidal phase current course the reference voltage inputs of the Controller are modulated with sinusoidal half-waves.

The microprocessor that controls the direction of the current phase with the control signals also generates the two analog signals.

For many applications a microprocessor with dedicated digital to analog converters can be chosen. Eliminating the need for separate D/A circuits.

About 5 bit have proved to be the most suitable subdivision of the current within one full-step. A higher

APPLICATION NOTE

resolution brings no measurable advantages. On the contrary, the converter clock frequency is already very high in case of low motor revolutions and very difficult to process by the processor-software. It is recommended to reduce the D/A resolution at high step frequencies.

In case of higher motor revolutions it is more convenient to operate only in full-step, since harmonic control is no longer an advantage as the current has only a triangular waveform in the motor winding.

PRECISION OF THE MICRO STEP

Any desired increase of the position resolution between the full step position has its physical limits. Those who think it is possible to resolve a 7.2° - stepper motor to 1.8° with the same precision as a

1.8° - motor in full-step will be received, as there are several limits :

The rise rate of the torque diagram corresponding to the twisting angle of the rotor for the 7.2° - motor is flatter by a factor of 4 then for the original 1.8° - motor. Consequently with friction or load moment, the position error is larger (fig. 21).

For most of the commercial motors there isn't a sufficiently precise, linear relationship between a sinusoidal-current-diagram and an exact micro step angle. The reason is a dishomogeneous magnetic field between the rotor and the two stator fields.

Above all, problems have to be expected with motors with high pole feeling. However, there are special stepper motors in which an optimized micro step operation has already been considered during the construction phase.

Figure 19 : The Half-step with Shaping Positioning is Achieved by Simply Changing Reference Voltages.

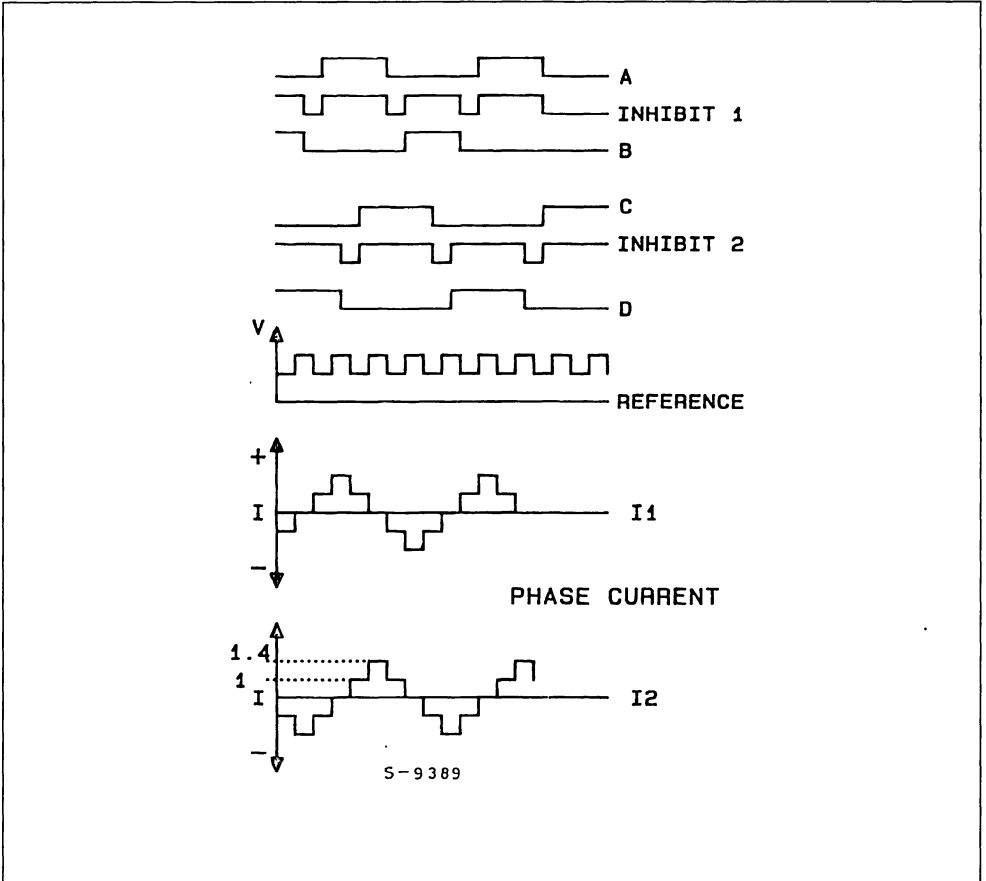
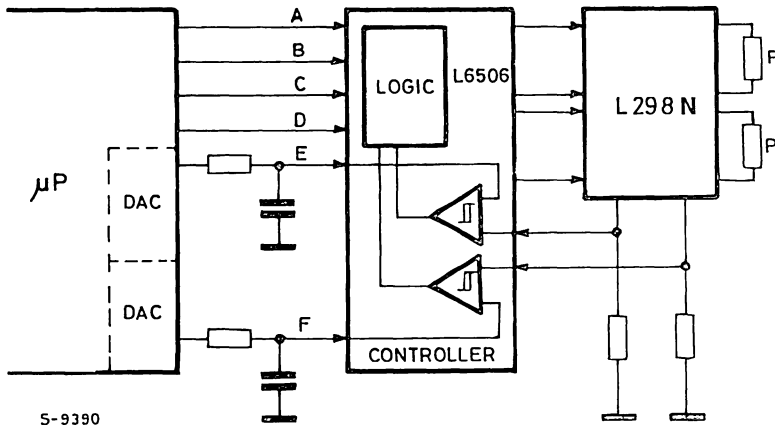
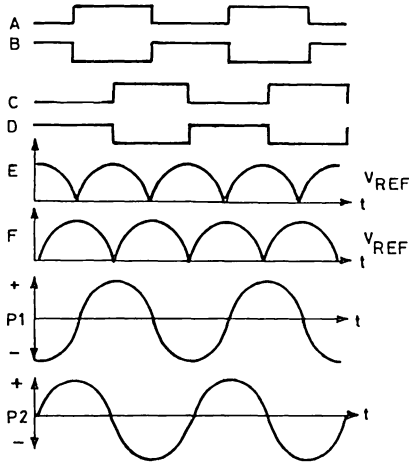


Figure 20 : L6506 Unit Gives The Possibility to Modulate Separately the Two Reference Voltage Inputs in Order to obtain a Sinusoidal Phase Current.

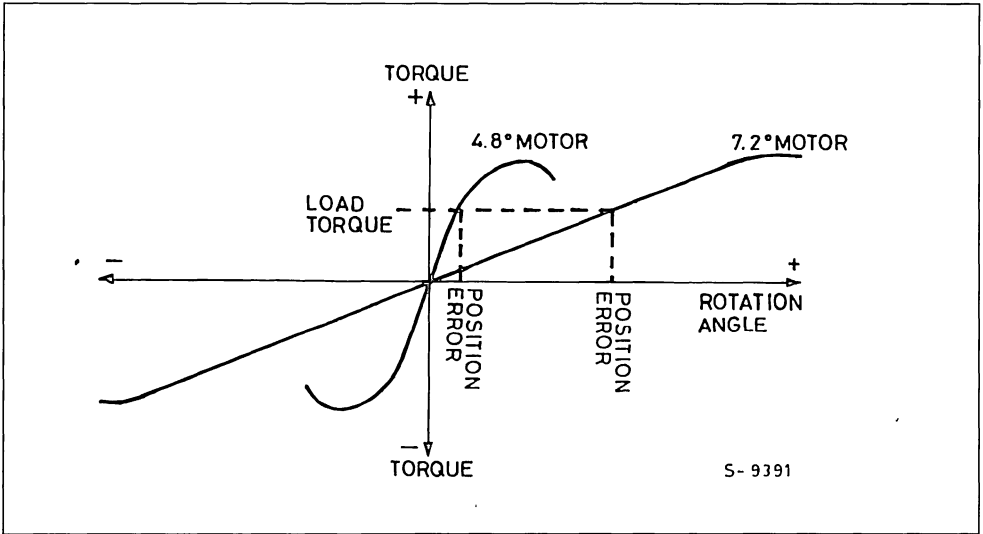


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Figure 21 : Better Resolution is achieved with Low Degree Motor but More torque is delivered with high Degree Motor.



CONCLUSIONS

The above described application examples of modern integrated circuits show that output and efficiency of stepper motors may be remarkably increased without any excessive expense increase like before.

Working in limit areas, where improved electronics with optimized drive sequences allow the use of less expensive motors, it is even possible to obtain a cost reduction.



PULSE CONTROLLED INVERTER

by J. M. Bourgeois

ABSTRACT

With the development of insulated gate transistors, interfacing digital control with a power inverter is becoming easier and less expensive.

This paper presents a new interface concept that takes advantage of digital based control to reduce the cost of the digital-to-power interface. The interface is greatly simplified by allowing the digital control to carry out a large part of the interface functions. This is one of the cheapest solutions available today and it has potential for further cost reduction.

A proposal for a Brushless DC Permanent Magnet motor drive is examined, although the technique can be easily applied to UPS or AC motor drives.

1. INTRODUCTION

Power MOSFETs and IGBTs, with their simple gate drive, make the design of DC/AC inverters relatively easy. For designers, the major problem is now to reduce the system cost while keeping the performance level high.

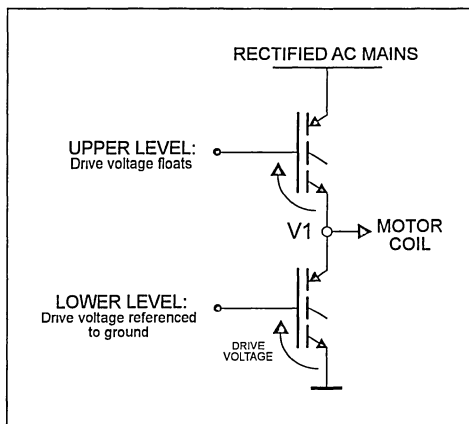
More difficult is the choice of the signal-power interface circuit from the variety of solutions available. For this type of circuit to be cost effective the design must use few components and cheap silicon technologies.

This paper proposes such an optimized interface based on a pulse control technique.

2. THE STATE OF THE ART

Digital controller based control circuits increasingly form the heart of high voltage/high frequency DC/AC inverters. As the cost of the interface is significant, keeping it to a minimum is a key issue. There are a number of methods of interfacing the controller to the power stage, which has a lower and an upper level - see figure 1.

Figure 1: Upper and lower levels of power stage



Generally the interface with the lower level is easy to design, as the gate-emitter/gate-drain drive voltage of the transistors is referenced to ground, as are the controller output voltages. However, upper level transistors are connected to the high side of the motor, and so their emitter/drain voltages (voltage V1 in figure 1) float. This means that there is a large difference in the voltage levels required for their drive and the output level of the digital controller, and so some form of isolation is required. The conventional solutions to this problem are as follows:

a) use of high voltage integrated circuit technology. This technique is at present expensive and cannot benefit from

shrink technology in the future, as the silicon area for this type of product is mainly defined by the size of insulation rings and buffer output current capability. Moreover, they required floating auxiliary power supplies as bootstrap or charge pump circuits.

b) the second technique consists of using a high frequency transformer interfacing each upper gate drive with the digital controller. The primary circuit is driven with a 1Mhz carrier, the secondary circuit rectifying this carrier to charge or discharge the Power MOSFET gate (see reference [1]).

c) the third technique exploits the opportunity of using the power MOSFET input capacitance as an ON state memory, the OFF state memory using another auxiliary capacitor. Then signals are no more provided continuously (see reference 2). Then the pulse transformer requires fewer turns than with the second proposal. Consequently this pulse transformer is small and versions are available for use with surface mounting techniques. If cost prevails, the very small operating duty cycle of this pulse transformer can allow construction using tracks on a Printed Circuit Board as its windings.

3. PULSE CONTROLLED INVERTER

The major feature of this inverter is that the upper level interface is controlled by pulses in such a way that the gate drive is inexpensive and the pulse transformer can be implemented with PCB track windings.

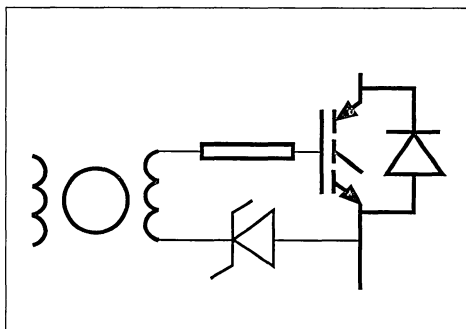
This technique is amongst the cheapest available at present and has the advantage of being able to benefit from the trend to digital integration.

3.1 Drive Circuit

Because of its very small operating duty cycle the interface is able to use a pulse transformer built with a few turns around a small ferrite core. Triple transformer versions are now available in a plastic package for automatic assembly. This transformer provides reliable, low capacitance isolation between the control section and the upper level floating gate drive. It is used to transfer both energy and signals to the upper gate drive.

The transformer secondary circuit is simplified, consisting of a zener diode and a series resistor (see figure 2).

Figure 2: Basic secondary circuit



The switching sequence is as follows:

- a positive pulse (ON pulse) applied to the transformer primary charges the gate through the zener diode. The resistance limits the charging current thus adjusting the switching time. The gate-to-source capacitance C_{GE} is used as a switch ON state memory.

- after the positive pulse a short circuit is applied across the primary transformer and the gate remains charged, as the zener diode is reverse biased.

- switching off requires the application of a negative pulse (OFF pulse) to overcome the zener voltage and discharge the gate

capacitance. During this negative pulse, the impedance across gate and source is defined by the series resistance.

The primary circuit requires only buffers to boost the digital signals to a current/voltage level compatible with the power MOSFET gate.

An interface like this does not require a floating auxiliary supply, nor does it limit the duty cycle which in this case has a pulse time of typically 500ns. Consequently the minimum ON and OFF times are about 500ns.

The sustaining voltage is determined by the pulse transformer which means that it can easily be much higher than the sustaining voltage of the power switches themselves. The same goes for the dV/dt immunity.

The total gate drive efficiency is unmatched due to the low transformer operation duty cycle and the non dissipative secondary circuit.

3.2 Digital controller features

The digital controller acts as a pulse generator providing two outputs (ON and OFF) for each upper switch and the direct gate drive for the lower switches. For high frequency operation, a typical pulse duration is less than 1 microsecond. For a three phase application, nine outputs are dedicated to the inverter drive; the digital controller generates three conventional output signals for the lower gate drives, the six others generating ON or OFF pulses for the upper gate drives.

Pulse timing

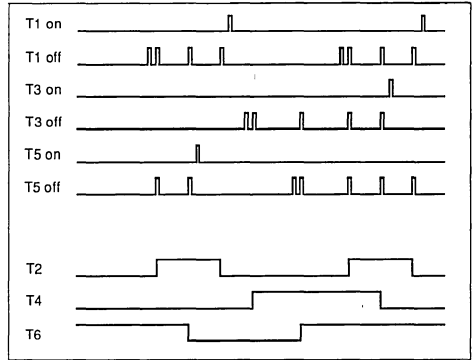
In bridge configuration, the upper switches are subject to dV/dt stresses during the commutation. To avoid cross-conduction, a low impedance must be applied across gate and source during a dV/dt .

Considering the secondary circuit shown fig.2, this condition requires the application

APPLICATION NOTE

of a negative pulse across the transformer during each critical dV/dt . Figure 3 shows an example of such a timing for a three phase AC motor drive. Transistor T1 is operated by channels T1-on and T1-off. T1-on corresponds to the positive pulses applied across the pulse transformer primary to switch on T1. T1-off corresponds to the negative pulses turning off T1. These negative pulses are applied to switch off T1 at the appropriate point in the switching sequence, and also each time another transistor switches during the off period of T1, to prevent spurious turn-on.

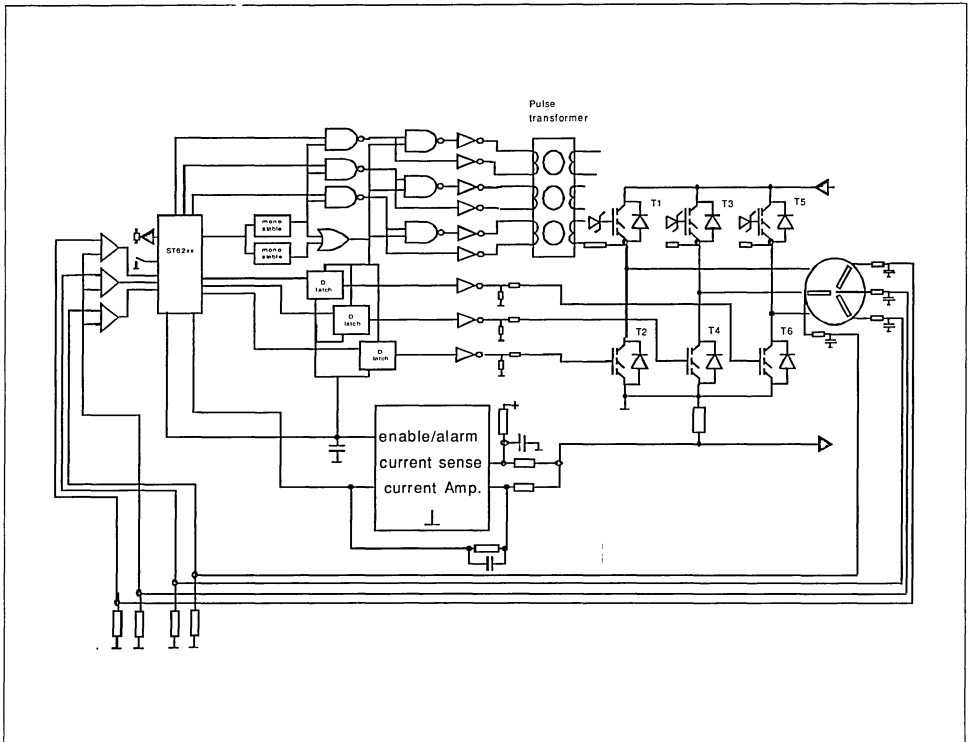
Figure 3: Inverter pulse timing



4. USING A PULSED CONTROLLED INVERTER IN A BRUSHLESS PM DC MOTOR DRIVE

Figure 4 shows the block diagram of a DC PM brushless motor drive using this technique. The inverter uses six STGW20N50D TO-247 packages housing

Figure 4: DC PM brushless motor drive bloc schematic

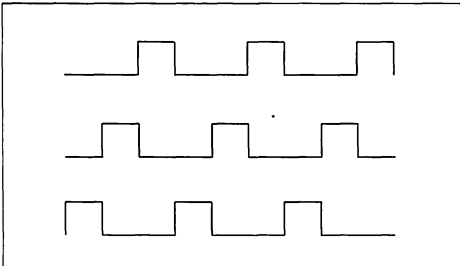


an IGBT and a discrete anti-parallel diode. The two devices are rated at 40A with $T_c = 25^\circ\text{C}$ and 20A with $T_c = 90^\circ\text{C}$. The triple pulse transformer is fully integrated in a plastic package (23Z284 from FEE-FIL-MAG Corp.). Nine push-pull buffers are required to interface the digital circuit with the power stage. The dedicated TD300/310 triple channel buffer is the ideal solution for interfacing the digital IC with these transformers.

The digital circuit is made of a low cost 8 bit CMOS micro-controller and a few logic gates. This ST6292 integrates 4kROM, 128bytes of RAM, 48 bytes of EEPROM, 21 fully software programmable I/O, one general purpose timer, one auto reload timer and one watchdog timer.

The micro-controller generates one PWM signal and six phase signals. Three of these are directly applied to the lower level buffers via a latch (see figure 5).

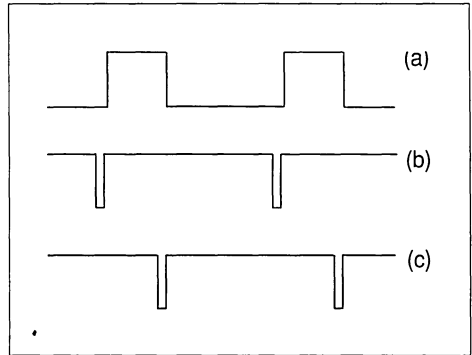
Figure 5: 120 degree 3 phase commutation signals



The three other phase signals are used to direct the PWM signal to the appropriate upper power switch to perform the current control. To operate the pulse transformers, this PWM signal is processed and only pulses are applied to the upper level buffer as following:

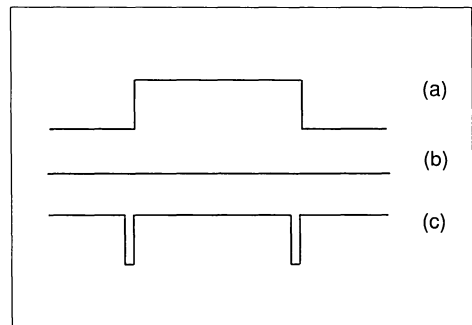
- figure 6 shows the PWM signal and the corresponding ON and OFF pulses driving the transformer buffer to turn ON/OFF the floating switches. Inputs of the transformer buffers are called channel ON and channel OFF.

**Figure 6: Basic PWM signal
ON channel signal
OFF channel signal**



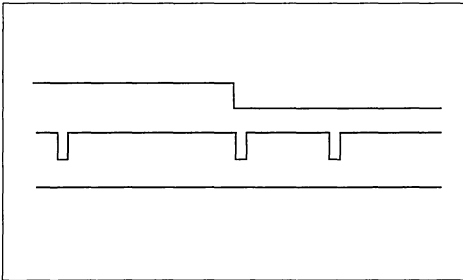
- when the upper switch has to be kept OFF (non activated phase), the PWM signal is processed in two OFF pulses via the OFF channel (see figure 7).

**Figure 7: Basic PWM signal
ON channel (unoperated)
OFF channel**



- when the lower switch is turned ON, there is a risk of cross conduction. At this point, the OFF channel generates a pulse synchronized with the phase signal in order to keep a low impedance across the gate and the source of the floating switch to prevent spurious turn-on (see figure 8).

Figure 8: Low level phase commutation (inverted)
OFF channel (synchronized)
ON channel (unoperated)



This pulse controlled inverter has been successfully operated in DC PM brushless motor drive with the previous circuit and AC squirrel cage motor drive using a thru-sinusoidal control performed with a ST9 micro-controller. When low inductance packages are used, it is a very effective and cheap solution. It can be easily implemented with Power MOSFET or IGBT in ISOTOP package, in applications up to 10kW.

5. CONCLUSION

This pulse controlled inverter has been designed for AC and DC brushless motor drives, but it is also suitable for UPS. It has the potential to reduce the digital to power interface cost while providing excellent performance. Driving Power MOSFET transistors by means of pulses only requires a cheap transformer and standard ICs resulting in a more cost effective solution.

This particular example takes advantage of a low cost ST6 micro-controller for large volume applications. In such a case product cost prevails on design time consideration, making this solution attractive.

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PWM TECHNIQUE FOR ACOUSTIC NOISE REDUCTION IN POWER APPLICATIONS

by J. M. Bourgeois

ABSTRACT

If PWM techniques are used in power control applications, high frequency current ripple appears in power actuators, generating acoustic noise at the corresponding frequency (switching noise). In many applications, these noises are disturbing and must be reduced or kept inaudible.

This paper presents a PWM technique for shaping the switching noise spectrum in such a way as to make it merge with the

natural system noise. It avoids a discrete switching frequency spectrum by using a pseudo-random PWM generator. Hence the switching frequency is continuously and randomly varied over a given range, which means that the switching noise spectrum is almost flat in this range, and is much less disturbing.

Practical solution and results are presented for a motor drive application.

1. INTRODUCTION

Pulse Width Modulation (PWM) techniques are widely used for control of current or voltage across electro-mechanical actuators such as motors or relays; the control pulses determine the conduction time of the converter power switches. This allows adjustment of the average current or voltage applied across the load.

As a consequence of these PWM techniques, high frequency current ripple appears in the actuator, generating acoustic noise at the corresponding frequency usually called switching noise. In many applications, this noise is disturbing and to be acceptable must be reduced or kept inaudible.

Generally the problem is solved by switching at frequencies above 20kHz, but this induces significant additional costs, for example increased power dissipation in the equipment requires a larger heatsink and high speed power switches, and a more expensive filter may be required (the interference regulation requirements may be increased for switching frequencies above 10kHz).

However, equipment is often inherently noisy because of moving parts. In such a case the aim should be to reduce the switching noise by merging it with the natural noise of the system. The PWM technique described here spreads the switching noise over a fixed frequency range. Using this technique the perception of switching noise is reduced and the switching noise spectral density significantly lowered.

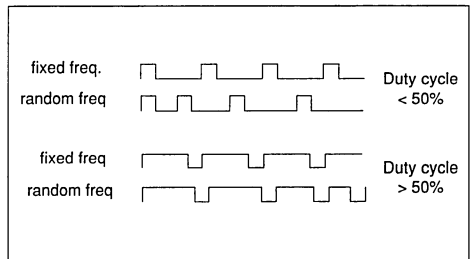
2. RANDOM PULSE WIDTH MODULATION TECHNIQUE

The basic principle of the technique is to change the switching frequency continually from one period of commutation to another. These frequency changes are randomly set within a given frequency range, and so the

frequency spectrum is flat inside this range. This can be achieved with a constant or variable duty cycle (δ). However a constant duty cycle implies a predetermined on and off time for each value of period, and this is not easy to implement while avoiding unpredictable current ripple. Thus it is easier to allow the duty cycle to vary along with the switching frequency.

The simplest solution uses digital control to implement the method shown in figure 1.

Figure 1: Basic PWM method



- If the required average duty cycle is less than 50%, it determines the t_{on} time which is then fixed. The t_{off} time is random over a given range and can be easily generated from a ROM look-up table. No calculation is required, and if the table is loaded with appropriate values, the frequency range can be delimited.

- If the required average duty cycle is more than 50%, its complement determines the t_{off} time which is then fixed. The t_{on} time is random over a given range.

This is easily implemented when the required average duty cycle and the random number generator have the same size (n bit). This means that the random number average value equals a duty cycle value of 50%, and there is no break around 50% of duty cycle when swapping from one alternative to another.

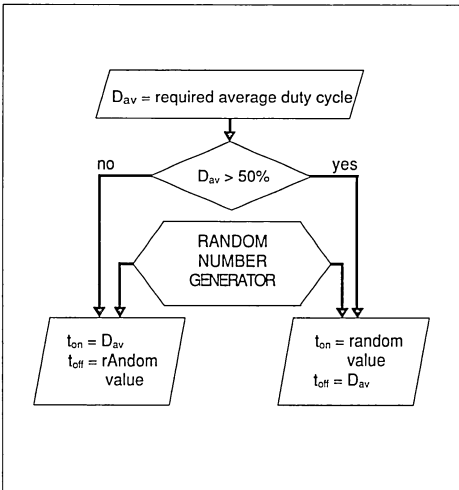
The random value table size should be determined to keep the repetition frequency

below 20Hz. Around 256 values is enough for operation below 5kHz.

The algorithm shown in figure 2 generates this type of pseudo-random PWM. However the actual average duty cycle is not a linear function of the required average duty cycle. If necessary, where a control loop cannot provide the linearisation, " D_{av} " should be multiplied by a linearisation factor, K_l , before setting t_{on} or t_{off} . This requires an additional look-up table of typically 50 words.

$$\begin{aligned} K_l &= \text{linearisation factor} \\ &= 2n-1 / (2n - D_{av}) \quad \text{with } D_{av} < 50\% \\ &= 2n-1 / D_{av} \quad \text{with } D_{av} > 50\% \end{aligned}$$

Figure 2: Random PWM generator



3. APPLICATION TO MOTOR DRIVE

This PWM technique has been implemented in different motor drive applications such as PM DC brushless DC motor drive, brush DC motor drive, Universal motor drive, and six step controlled induction motor drive, using micro-controllers:

- The ST90xx family was selected for three phase AC current control. These 8/16 bit micro-controllers are fast enough to generate with software, three independent random PWM signals. (see reference 1)

- The ST62xx family was selected for three phase DC current control. In this particular case only one random PWM channel is needed, and the ST62xx offers a more economic solution.

However if CPU time is critical in a given application, the random PWM generation can be performed by an external ASIC. STKM2000 series of mixed analog-digital standard cells is a particularly suitable solution.

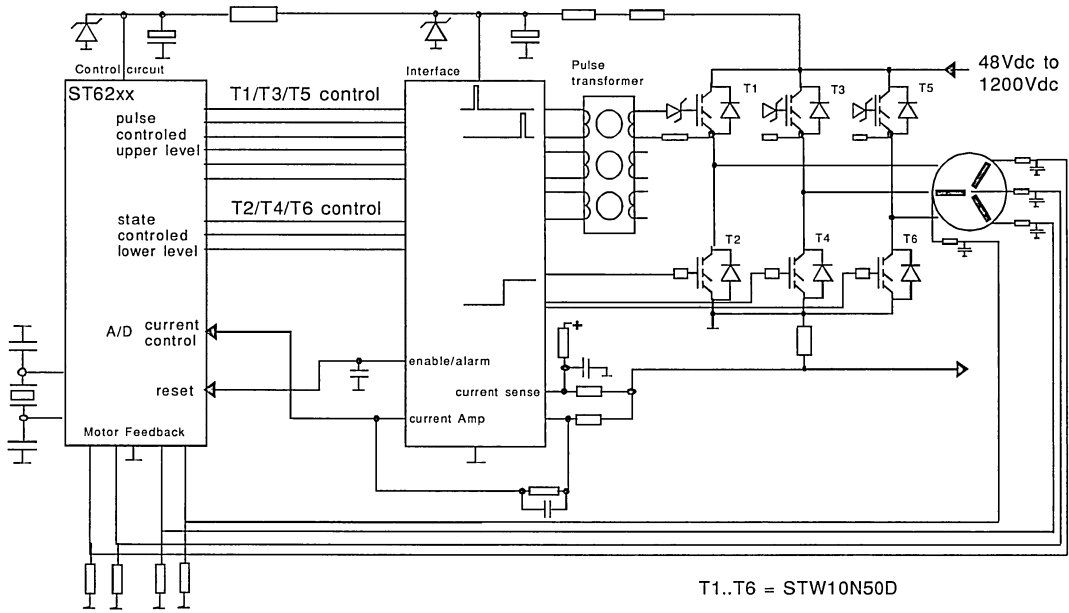
Figure 3 shows an example of a brushless permanent magnet DC motor drive using this technique. The power switches are STGW10N50D which has a 10A/500V IGBT and an anti-parallel fast diode in TO-247 package. The random PWM signal is generated by an ST6291 micro-controller, the external logic circuits being used to operate the pulse controlled inverter (see reference 1).

This pseudo-random PWM signal is used to drive the upper level switches for current control. The signal is generated with the appropriate phase providing 120 degree commutation. The lower level switches are operated only for phase commutation and over-current protection.

The micro-controller/power interface is simplified by using the input capacitance of the gate of the IGBT as an ON state memory, OFF state memory being stored in the micro-controller. The pulse transformer requires few turns due to its small operating duty cycle, and could be accommodated on a PCB.

The secondary circuit is simplified as far as possible while maintaining the functionality. A positive pulse across the transformer charges the gate through a Zener diode.

Figure 3: DC PM brushless motor drive



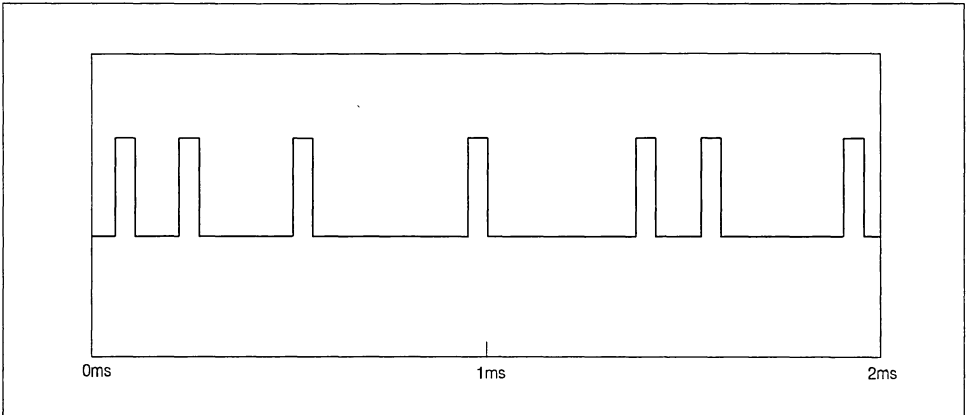
Switching off requires a negative pulse to compensate the Zener voltage. To be functional such a secondary requires synchronised pulses from the micro-controller to avoid cross conduction.

This hardware solution is very cheap and

gives many advantages: no power switch duty cycle limitation, virtually no maximum dV/dt and sustaining voltage limitation, and very low gate drive consumption.

Figure 4 shows an example of a pseudo-random PWM signal with constant t_{on} .

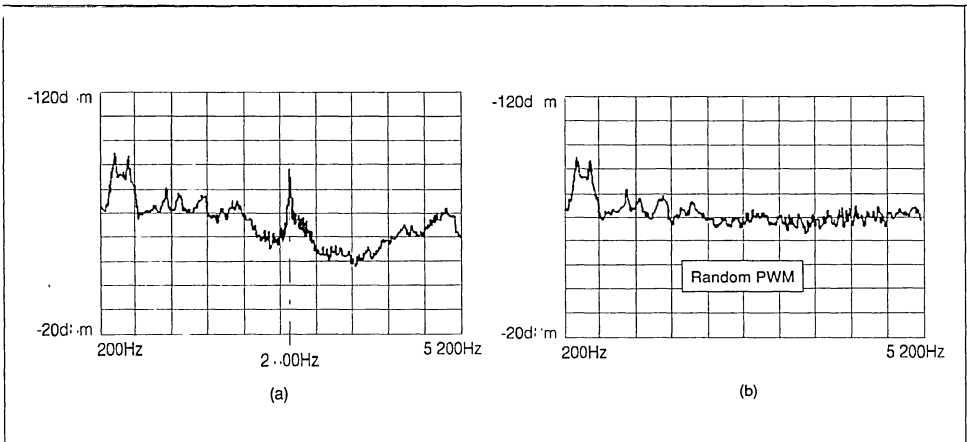
Figure 4: Random PWM signal ($\Delta < 50\%$)



Acoustic measurements were made with an open air brushless motor inside an acoustic chamber. The signals from an electret microphone placed close to the motor were amplified with a wide-band audio pre-

amplifier. Figure 5 shows the noise spectrum recorded whilst operating with a) a constant and b) a random switching frequency. The noise amplitude scale is logarithmic and the frequency scale is linear.

Figure 5: Acoustic noise spectra



- in the range 200Hz/2kHz the spectra are identical and are due to noise generated by the motor fan, the bearing and the vibration generated by the torque ripple.

- in the range 2kHz/5.2Khz the spectra are completely different: a constant operating frequency gives a spike at the corresponding frequency (2.8kHz).

a random operating frequency gives a flat spectrum over the range in which the frequency varies. In this particular case, t_{off} is somewhere between 100 and 500 micro-seconds, t_{on} being 60 micro-seconds; the frequency range is set from 1.8 to 6 kHz.

The human ear is better equipped for more subjective investigations. It is far better than the best computer, and, more to the point, is the most concerned with the results (see reference 2). In this particular case, this random noise is similar to that of a domestic audio amplifier with, fortunately, a less efficient loudspeaker.

4. CONCLUSION

The Pulse Width Modulation technique presented in this paper enables the spreading of switching noise over a pre-determined audio range, merging it with the natural noise of the system. Consequently, the motors of naturally noisy systems such as food processors, washing machines, fans, can be operated with a switching frequency of around 3kHz creating no extra disturbance. The benefits of this low switching frequency can be counted in terms of cost reduction due to the reduced demands on the components: smaller heatsink, slower switching components and smaller filter.

This technique has been made successfully with both the ST6 and ST9 micro-controller families, but can also be made with the STKM2000 mixed analog-digital standard cells ASIC.

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PRESENTED AT APEC
SAN DIEGO MARCH 1993

DIGITAL CONTROL FOR A BRUSH DC MOTOR

by T. Castagnet, J. Nicolai

ABSTRACT

In home appliances applications the brush D.C motor, driven by a chopper, can be controlled by a standard microcontroller. However, microcontrollers are often considered unsuitable for the power environment because of their limited computing speed, or problems with noise immunity.

This paper shows how a cost effective digital motor drive can be designed by combining a chopper and an 8 bit microcontroller. The speed of the motor is simply controlled through direct voltage compensation and motor power limitation.

The microcontroller performs both the motor control and interface functions of the application, replacing the analogue circuits of a conventional motor control.

Performances and practical results are given for a 300W / 12000 RPM motor drive.

1. INTRODUCTION

In home appliance applications the Permanent Magnet DC motor is replacing the AC universal motor, improving speed and drive performance. Traditionally, the control of this motor is implemented

using analogue circuits, with an associated microcontroller performing only an interface function.

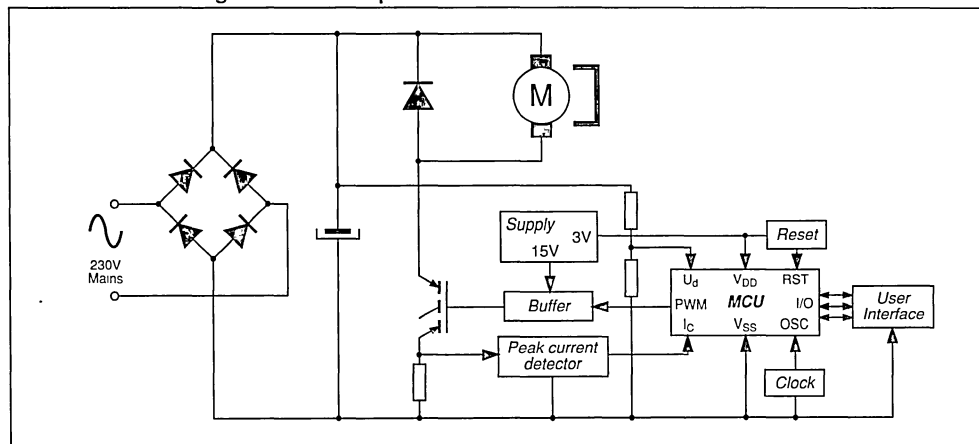
This paper shows that a low end microcontroller can control directly a chopper driven DC motor in addition to these interface functions. In this example the adjustable speed drive is made with a 300W-2000 RPM permanent magnet DC motor for a food processor application.

2. THE PERMANENT MAGNET DC MOTOR AND ITS CONVERTER

The brush DC motor can be controlled by a chopper circuit. This adjustable speed drive controls the load in only one direction of rotation, and does not allow electrical braking. This type of operation is sufficient in applications such as food processors, drills or washing machines.

The design of the control circuit is simplified with the use of insulated gate transistors in the chopper, and with the use of permanent magnets for the motor excitation. Permanent magnets (e.g. ferrite materials) replace the stator windings and make an excitation circuit unnecessary, as the motor has an independent excitation. See figure 1.

Figure 1. Application block diagram. The microcontroller generates a PWM signal and controls the IGBT through the buffer-amplifier.



APPLICATION NOTE

In home appliance applications the Permanent Magnet DC motor, driven by a chopper, is replacing the common AC universal motor when improved speed/drive performance is required (see appendix 1) for the following reasons:

- the motor efficiency is increased: the permanent magnets remove excitation losses, and iron and copper motor losses are reduced because the motor current ripple is reduced (more than 50%) thanks to the DC mode operation and to a suitable motor voltage control;
- the motor noise is reduced: the 100Hz torque ripple is reduced because of the motor current ripple reduction, and the switching frequency is almost inaudible;
- the motor voltage determines the speed directly because the excitation is independent; the speed is therefore stable, particularly when the torque is varies quickly (during 1s) and frequently (10 times);
- the operating speed range is increased because the motor can provide maximal torque (here $T_{max} = 2 \text{ N.m}$) at low speed (less than 1000 RPM).

3. THE MICROCONTROLLER : THE HEART OF THE MOTOR CONTROL

In home appliance or industrial applications, microcontrollers are usually dedicated to interfacing and sequence management. Here we will show that a microcontroller can also integrate the motor control.

This speed drive is controlled by an 8-bit

microcontroller, the ST6260/65 (see figure 2).

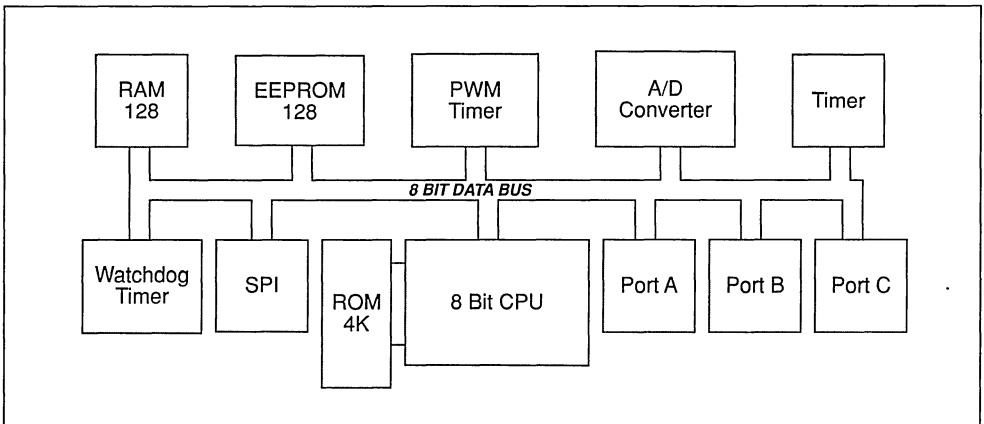
Such microcontrollers can meet all interface and motor control requirements:

- design of interface functions is simplified due to their 8-bit analogue-to-digital converter (ADC), and their many inputs/outputs (up to 21 I/O); these allow the MCU to measure sensors, manage actuators and the user interface (for example push buttons, potentiometers, keyboard, LED diodes, bar-graph or LCD displays);
- they have additional functions useful for the design of a motor speed drive: a Pulse Width Modulation (PWM) timer for chopper control; an ADC with up to 13 inputs for voltage and current measurement; and a Non Maskable Interrupt (NMI) to generate safety protection in the Central Processor Unit (CPU).
- their safety and immunity is fully compatible with off-line circuits (hardware watchdog, careful supply lay out, decoupled oscillator, filtered inputs).

The performance required for the speed control is the following :

- accuracy of speed is not very important: there is no need for a speed sensor, and so costs are reduced; and the microcontroller adjusts the speed directly with the motor voltage;
- the motor is controlled using direct voltage compensation, and so the speed is insensitive to the input power and to variations in the mains

Figure 2. Block diagram of the ST6260/65 micro-controller. PWM timer and A/D converter are suitable for motor control.



voltage; the motor current ripple is also reduced by this compensation;

- the user speed selection is performed by two +/- push buttons; its variation is adjusted by software and the start up request speed is zero ;
- the motor is protected against too big a load when the user request is out of the motor safe operating area. A 300W motor power limitation is implemented, avoiding overheating and hard brush switching ;
- the chosen chopper frequency is 8kHz : the circuit can meet the R.F.I. standards (VDE 875) with a small input filter while keeping a low switching noise level ;
- speed drive start up is validated after a voltage check of the 230V mains supply.

To achieve this speed drive, software functions have been implemented as shown in figure 3.

The autoreload PWM timer controls the switching of the chopper, generating the PWM signal. The CPU controls the duty cycle d and the switching period T_s by software (see figure 4). The duty cycle varies

Figure 3. Main algorithm for motor control. Direct voltage compensation and motor power limitation are the key functions of the control.

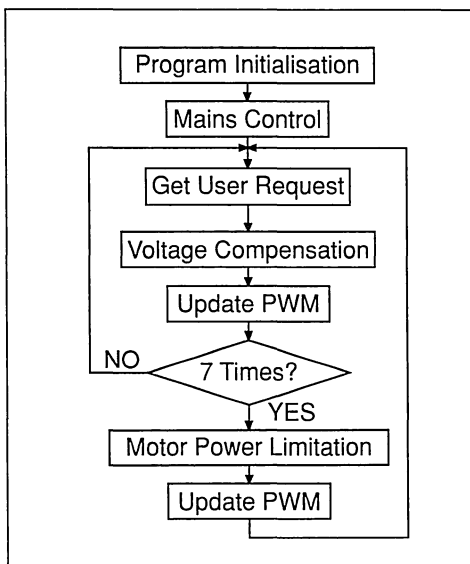
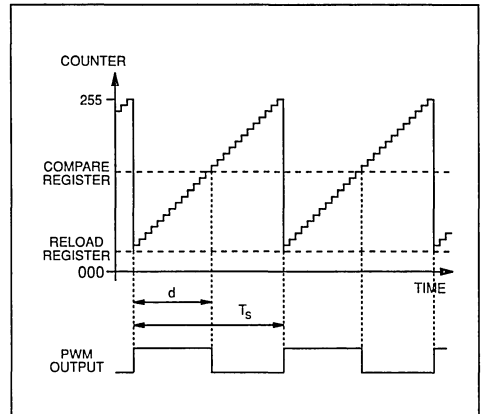


Figure 4. Operation of the autoreload PWM timer. CPU controls the period T_s with the Reload register, and the duty cycle d with the Compare register ; the timer counts independently of the CPU.



from 0 to 100%, with 0.4% (1/256) duty cycle resolution. The maximum switching frequency is 31 kHz: by software it has been adjusted to the required 8 kHz.

The direct voltage compensation aims to keep the motor voltage V_{mot} and the speed constant, particularly when the mains voltage is varying, or when the input power is transmitted to the motor. The duty cycle is modulated as a hyperbolic function of the direct voltage U_d around a reference point given by d_0 = user request duty cycle and $U_{d(nom)}$ = nominal direct voltage:

$$V_{mot} = d \times U_d$$

$$V_{mot} = \text{constant} = d_0 \times U_{d(nom)} \quad (\text{see figure 5})$$

To achieve this, U_d is measured and quantized in 32 steps, and d_0 is quantized in 16 steps: duty cycle correction is taken from a look-up table of U_d versus d_0 . The correction is added to d_0 and the sum is loaded into the PWM timer.

The voltage compensation needs a table of 512 bytes, and takes 380 μ s. The practical results are characterized in 2 ways :

Figure 6 demonstrates the immunity of the motor voltage to variations in U_d for a fixed speed reference. The variation of V_{mot} is less than 10% over the whole range of values of U_d , and the speed becomes

Figure 5. Direct voltage compensation

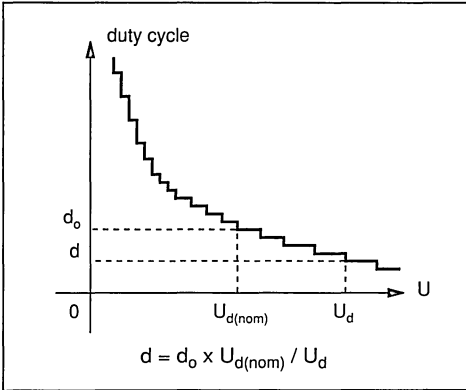


Figure 6. Static performance of direct voltage compensation

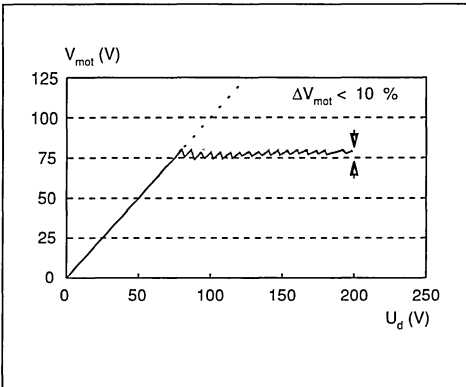
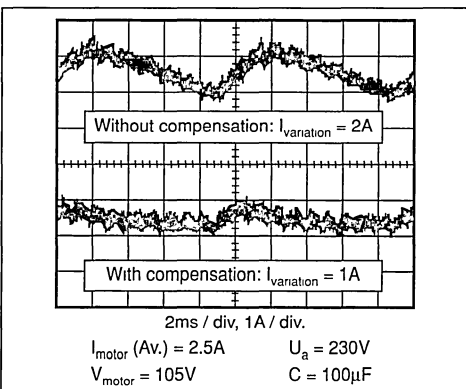


Figure 7. Dynamic performance of the voltage compensation



almost insensitive to the input power and mains voltage variations.

Figure 7 shows the dynamic influence of compensation on motor current ripple. The ripple is reduced by a factor of two in normal operation.

Motor power limitation is performed by measuring the peak motor current I_p using a resistor or a SENSEFET. With a capacitor, diode, and the sample-and-hold method this measurement is easy and accurate (see figure 8).

The motor power limitation aims to limit d to a maximum duty cycle d_{max} . Assuming that the motor current I_{mot} is almost constant, d_{max} is defined as a hyperbolic function of U_d and I_{mot} (see figure 9) :

$$P_{mot} = I_{mot} \times V_{mot} = I_{mot} \times U_d \times d$$

$$P_{mot} \leq P_{max}$$

$$d < d_{max} = P_{max} / U_d \times I_{mot}$$

d_{max} is taken from a look-up table versus U_d and I_{mot} which are measured and quantized in 16 and 32 steps respectively. Power limitation needs a table of 512 bytes, and is performed every 3ms. Figure 10 shows the result with 300W limitation.

The two look-up tables are computed using a high level language program or by hand in order to avoid calculation in the CPU, speeding up the process. The tables used in this example are suitable for 230V or 120V mains applications.

The compensation and limitation tables can be modified and optimized to special requirements.

The accuracy of results is mainly governed by the resolution of the ADC (20 mV) and the basic step of converted measures ($1/2^n$ for $n \geq 8$).

4. THE SWITCH : THE POWER ACTUATOR OF THE MOTOR CONTROL

Insulated gate transistors like Insulated Gate Bipolar Transistors (IGBTs) or Power MOSFET transistors are usually used for this purpose. Such transistors simplify and improve the chopper design because :

- their gate driver is simple: they are controlled by connecting a 15V voltage source to the transistor gate ;
- they are fast: the switching frequency can be made high enough to be inaudible (up to 16 kHz) because of their low turn-off energy.

The interface between the MCU and the switching

Figure 8. Peak motor current sensing:
 a) Operation is independent of switching; measurement is made when T₁ is OFF, analogue value is reset when T₁ turns on.
 b) Block diagram.

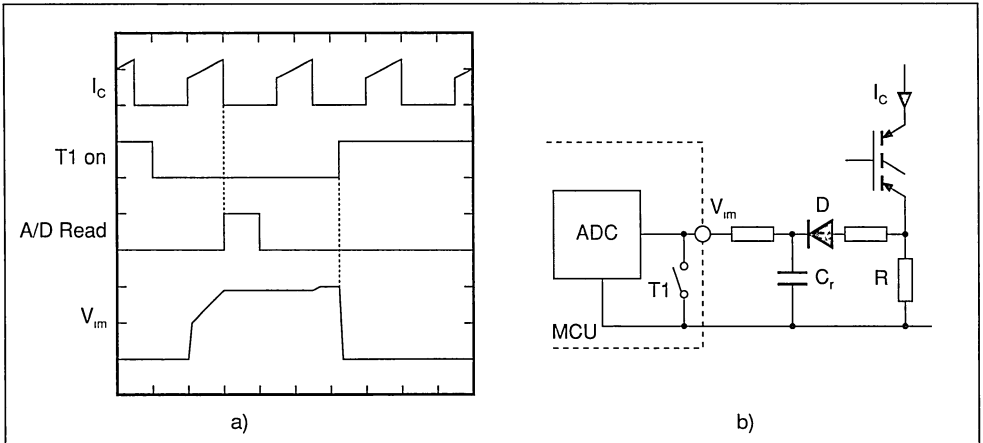


Figure 9. Motor power limitation.

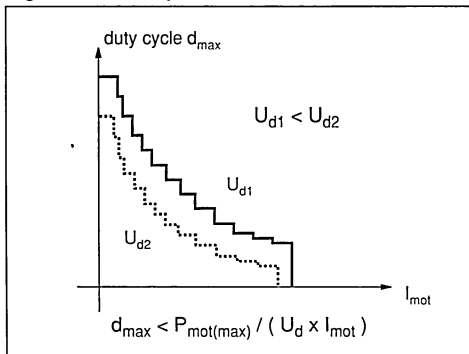
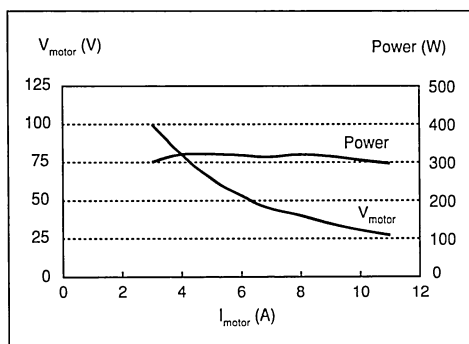


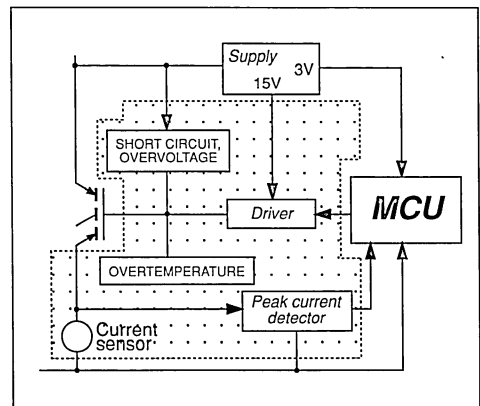
Figure 10. Motor power limitation performance.



transistor is made by a 15V auxiliary supply that is connected to the 350V DC supply, and by a buffer-amplifier that is driven directly by the PWM timer output. To this basic driver we can add other functions (see figure 11) :

- A transistor current sensor (necessary for power limitation). A resistor or a SENSEFET can be used with an analog peak current detector (capacitance and diode).

Figure 11. Basic diagram of the MCU-switch interface. Fast transistor protection could be added to the driver functions.



- Some fast transistor protection. The MCU cannot generally assume that the protection is present, because its reaction time is slower (12 μ s typ.) than required response time (less than 1 μ s). With its own protection the transistor immunity is increased. Short circuit, overvoltage and overtemperature protection are the most important types of protection for good functional safety.

CONCLUSION

The design presented proposes a kit "microcontroller plus IGBT" that meets all requirements for controlling a permanent magnet DC motor in home appliances or industrial applications.

This kit reduces the components count on the board because the microcontroller can integrate in one package all the functions of interface and motor control.

The MCU + IGBT becomes a flexible and adaptable solution for power control. The switching transistor can be changed, and therefore the motor power, up to about 4 kW. The motor control software can be modified (speed regulation, current compensation) to include other functions (bus interfacing, heating, power supply control).

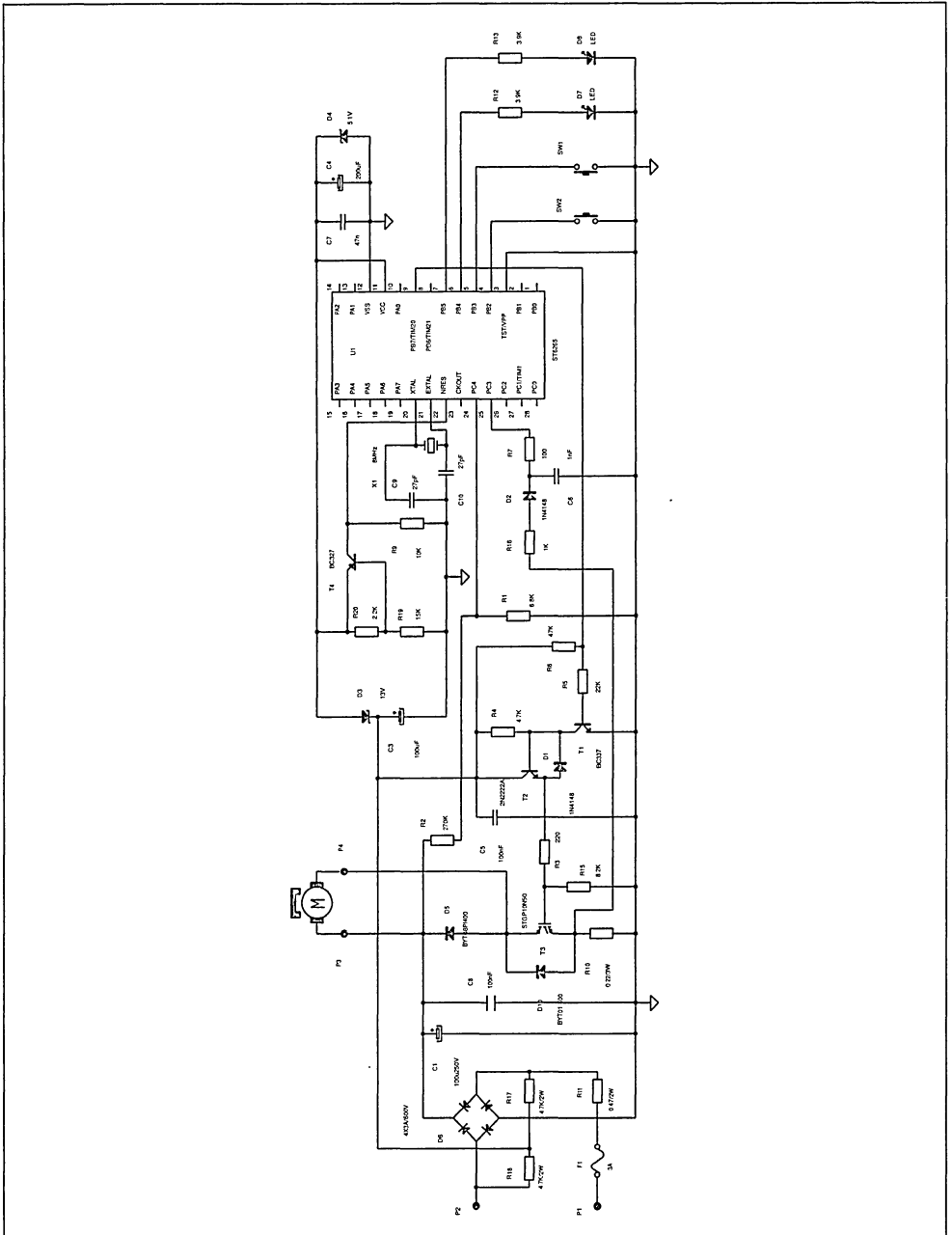
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Appendix 1. Comparison of AC universal motor and Permanent Magnet DC motor.

CRITERIA	AC UNIVERSAL MOTOR	PERMANENT MAGNET DC MOTOR
Driver	Single triac	Rectifier bridge+ chopper Simple transistor driver
Speed range (RPM)	1000 → 25000	100 → 25000
Speed control	Runaway if no load	Closed loop speed regulation is necessary if large torque variation
Torque capability at low speed	High, but needs control loop	Natural nominal torque
Motor efficiency	40-50%	60-70%
Motor losses	50Hz copper and iron losses	No excitation losses
Driver losses	Lower (TRIAC)	Higher (rectifier + chopper)
Noise	Higher 100Hz torque ripple, brushes commutation	Motor control reduces torque ripple, inaudible switching frequency brushes commutation.
Magnetization	Sensitive to iron saturation	Overcurrent and overtemperature can demagnetize permanent magnets
Basic Diagram		

Appendix 2. Complete diagram of the Permanent Magnet DC motor drive with ST6265 microcontroller, STGP10N50 IGBT transistor and STTA806DI diode.



AUTOMOTIVE APPLICATIONS

HIGH SIDE DRIVERS

by A. Russo, B. Bancal, J. Eadie

INTRODUCTION

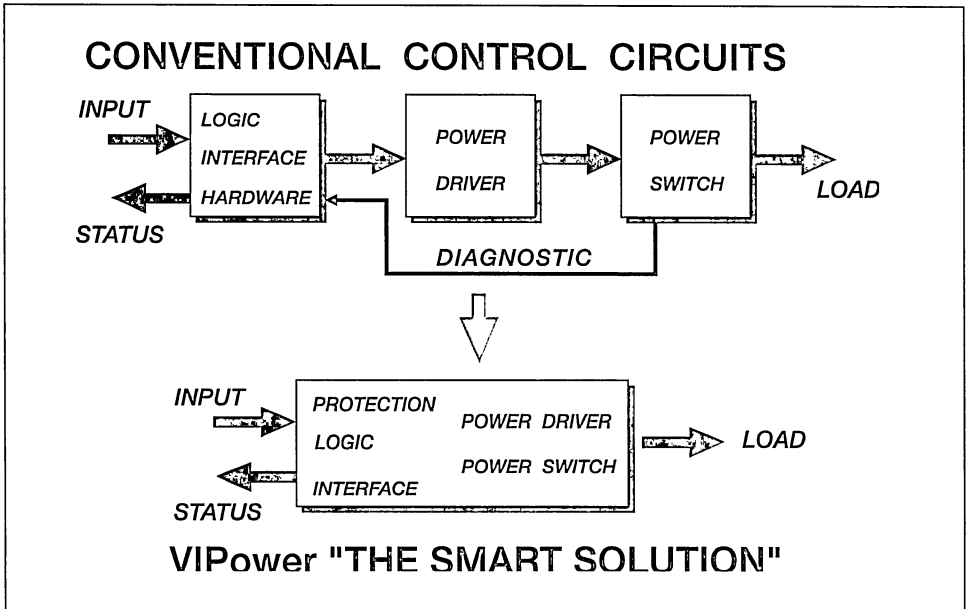
The ever increasing demand for cost reduction and higher levels of circuit complexity and reliability have directed the semiconductor manufacturer's attention towards smart power technologies which allow the production of totally integrated monolithic circuit solutions that include a power stage, control, driving and protection circuits on the same chip.

Vertical intelligent power, (VIPower™) an SGS-THOMSON Microelectronics patented technology, established over 7 years ago, uses a fabrication process which allows the integration of complete digital and/or analog control circuits driving a vertical power transistor on the same chip. The power handling capability of this type of structure compares favourably with monolithic smart power devices of equivalent chip size which use lateral, or "U-turn"

power output structures.

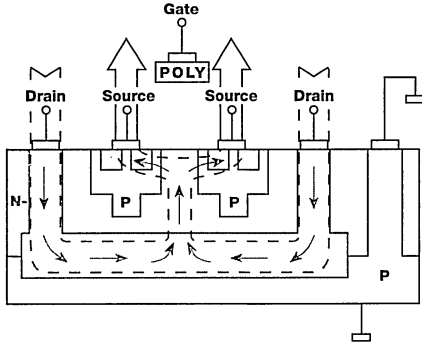
The VIPower technology M0 used for making these High Side Drivers produces a monolithic silicon chip which combines control and protection circuitry with a standard power MOSFET structure where the power stage current flows vertically through the silicon.

High Side Drivers, with their integrated extra features are power switches that can handle high currents and work up to about 40V supply voltage. They require only a simple TTL logic input and incorporate a fault condition status output. They can drive an inductive load without the need for a freewheeling diode. For complete protection the devices have an over-temperature sensing circuit that will shut



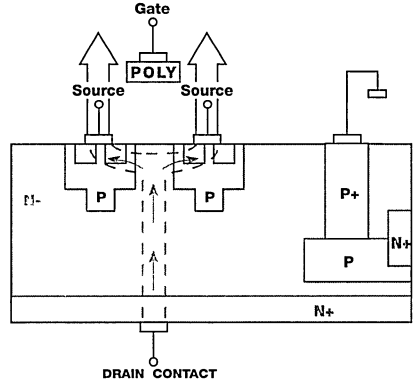
SMART POWER APPROACHES

CONVENTIONAL SMART POWER ICs



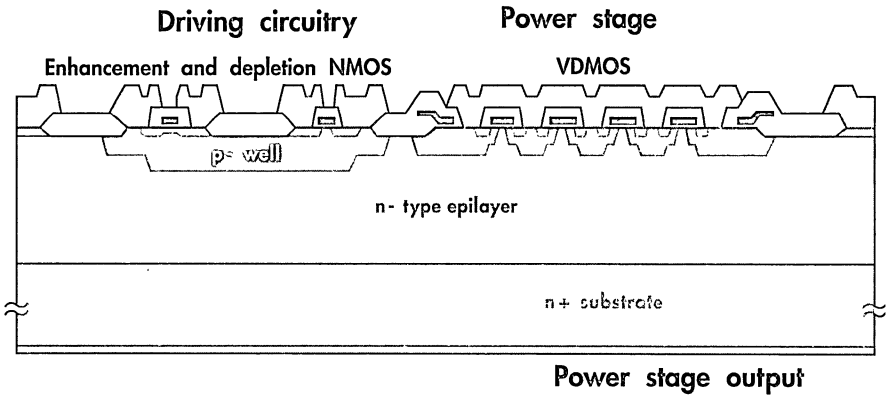
"U-TURN" PROCESS

VIpower



VERTICAL PROCESS

CROSS SECTION OF MØ VIpower™ TECHNOLOGY



down the chip under over-temperature conditions. They also have an under-voltage shutdown feature. It is simple to introduce some differences in the control logic to produce devices with features which cater for different working environments.

Each application exerts an external influence over the switch. A filament lamp or DC motor, for example, have in-rush currents that any switch has to handle. Solenoids and motors have an inductive effect and must lose the residual magnetism when the current is turned off. This gives rise to induced voltages and the need to remove this stored energy. External fault conditions can also stress the drivers and their associated circuitry. The following discussion has been designed to explain the basic principles involved in using these devices and to help to understand how they react under the influence of various applications.

Almost every electronic switch used in a modern automobile application is a high side switch. This configuration is preferred for automotive use because:

- a) - This configuration protects the load from continuous operation and resulting failure, if there is a short circuit to the ground. Since the body of a car is metal and 95% of the total car is ground, the short to ground is much more common than short to V_{CC} .
- b) - High Side Drivers cause less problems with electrochemical corrosion. It is of primary importance in automotive systems because the electrical components are in an adverse environment, specifically adverse temperatures and humidity and the presence of salt. For this reason the series switch is connected between the load and the positive power source. Therefore when the electrical component is not powered (that is for the greatest part of the lifetime of the car) it is at the lowest potential and electrochemical corrosion does not take place.

Integrated High Side Drivers offer numerous advantages over the popular automotive relay used in cars today. Diagnostic information output from the High Side Driver helps the on-board microcontroller to quickly identify and isolate faults saving repair time and often improving safety. High Side Drivers can reduce the size and weight of switch modules, and where multiplexed systems are used, dramatically reduce the size of the wiring harness.

Process control applications offer another use for High Side Drivers. A considerable improvement in reliability and reduction in down time can be obtained by using them in place of relays. Process control systems, often consisting of powerful computers that control large numbers of actuators, are perfect environments for these devices. The semiconductor manufacturer has little control over the nature of the load being driven and these can vary - solenoids, motors, transducers, leds. In these situations, software process monitoring by a mP can detect a fault reported by a status output and offers the option of taking corrective action. In the unlikely event of a failure in a High Side Driver in critical processes, a second device can be programmed to operate instead.

SGS-THOMSON High Side Drivers are designed to provide the user with simple, self protected, remotely controlled power switches. They have the general structure as shown in figure 1.

Some typical applications are shown in figure 2.

THE GENERAL FEATURES OF HIGH SIDE DRIVERS.

The diagram in figure 3 shows the control and protection circuit elements and the power stage of a basic device.

Input

The 5V TTL input to these High Side Drivers is protected against electrostatic discharge. General rules concerning TTL logic should be applied to the input. The input voltage is clamped internally at about 6V. It is possible to drive the input with a higher input voltage using an external resistor calculated to give a current not exceeding 10mA at the input.

Internal power supply

To accommodate the wide supply voltage range experienced by the logic and control functions, these devices have an internal power supply. Some parts of the chip are only active when the input is high, the status output and charge pump for example. This means it is possible to conserve power when the device is idle. The internal power supply has therefore been designed in two parts. One section supplies power to the basic functions of the chip all the time, even when the input is 0V. The second section supplies power only when the input is high. This ensures that the stand-by current is limited to 50mA maximum in the off-state.

Figure 1. Standard current and voltage conventions

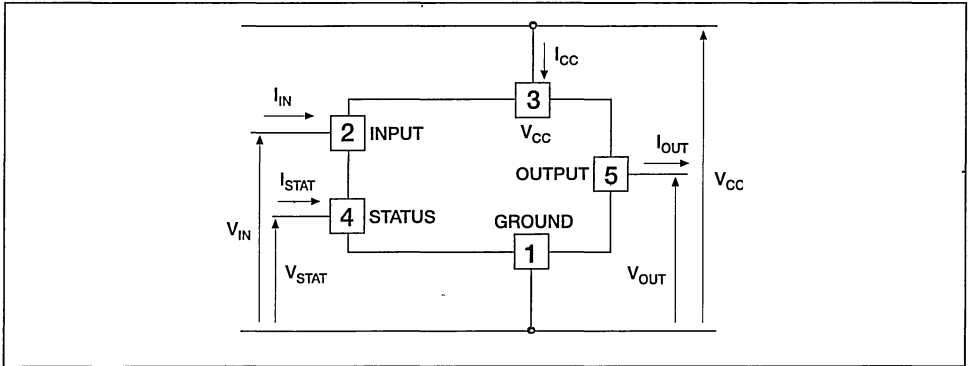


Figure 2. High Side Drivers interfaces between control logic and power load

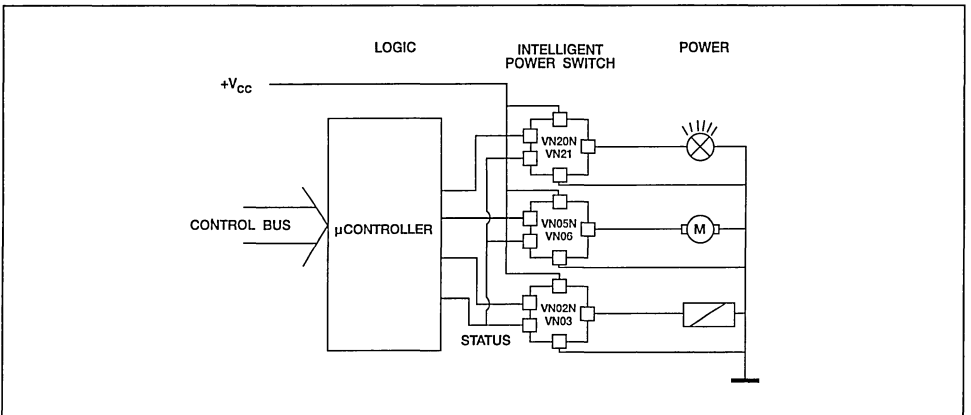
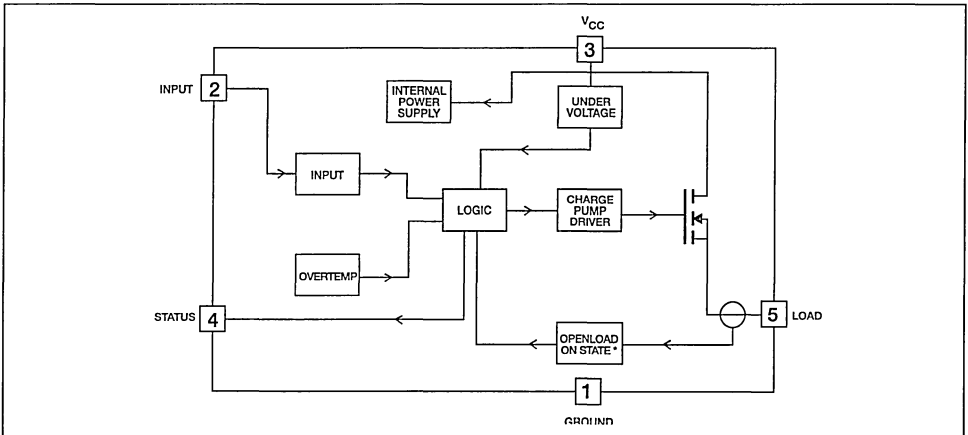


Figure 3. Generic Internal Block Diagram



THE CONTROL CIRCUIT.

Under voltage lock-out.

Under-voltage protection occurs when the supply voltage drops to a low level specified in the datasheet as V_{USD} . The under-voltage level set at this value ensures the device functions correctly. Inductive effects must be considered in understanding the function of this feature. The di/dt is controlled by the device and not by the external circuit. The controlled value is calculated for a line inductance of $5\mu\text{H}$ ($\approx 5\text{mt}$. of wire). Typically $di/dt=0.5\text{A}/\mu\text{s}$ for a normal load and $1\text{A}/\mu\text{s}$ for a short circuit. At turn on this generates an opposing voltage. If this opposing voltage is too large, the apparent supply voltage will drop below the under-voltage lock-out level and the device will turn off. Using the specified conditions, the induced voltage will not be large enough to reduce the supply voltage below 6V. This is important in the case where the load is a near short circuit when in-rush current occurs, as in the case of a car headlamp filament turning on.

Open load detection and stuck-on to V_{CC} .

Open load detection occurs when the load becomes disconnected.. In the VN20N family open load detection only occurs in the on-state.

An extra feature for load disconnection detection is that open load detection during the off-state as well as in the on-state can be provided. The circuit for the off-state open load detection requires an external resistor between V_{CC} and the output pin.

Open load detection is possible in the off-state in the VN21 family and it conforms to the I.S.O. norms for automotive applications. If an open load condition is detected the status flag goes low. Should an external supply be applied to the load (output pin) or the device is externally short circuited, the off-state open load detection can detect this "stuck-on" to V_{CC} condition.

Over-temperature protection

Over-temperature protection is based on sensing the chip temperature only. The location of the sensing element on the chip in the power stage area, ensures that accurate, very fast, temperature detection is achieved. The range within which over-temperature cutout occurs is $140^{\circ}\text{C} - 180^{\circ}\text{C}$ with 160°C being a typical level.

Over-temperature protection acts to protect the device from thermal damage and consequently also limits the average current when short circuits occur in the load.

Figure 4. Equivalent Schematic for the open load detection current in off-state

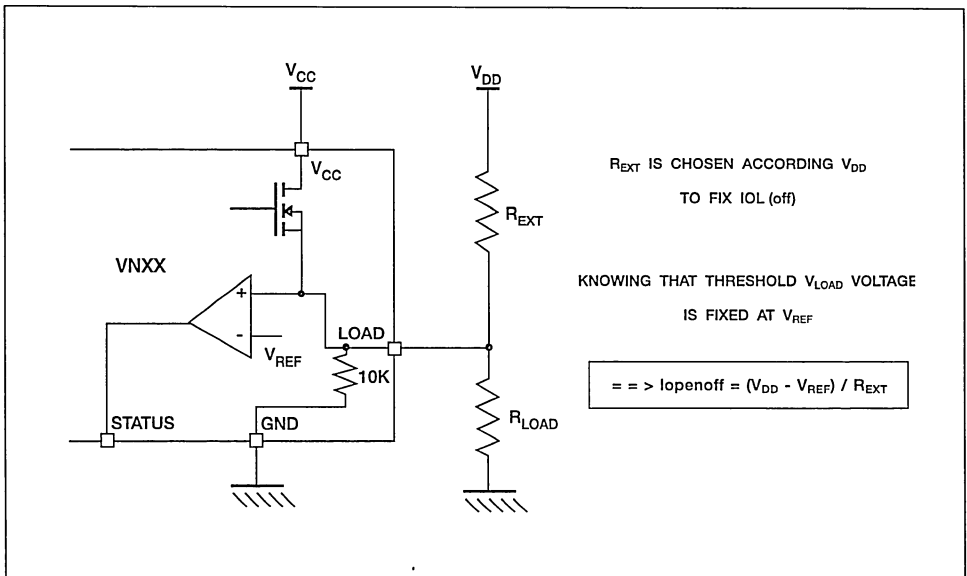
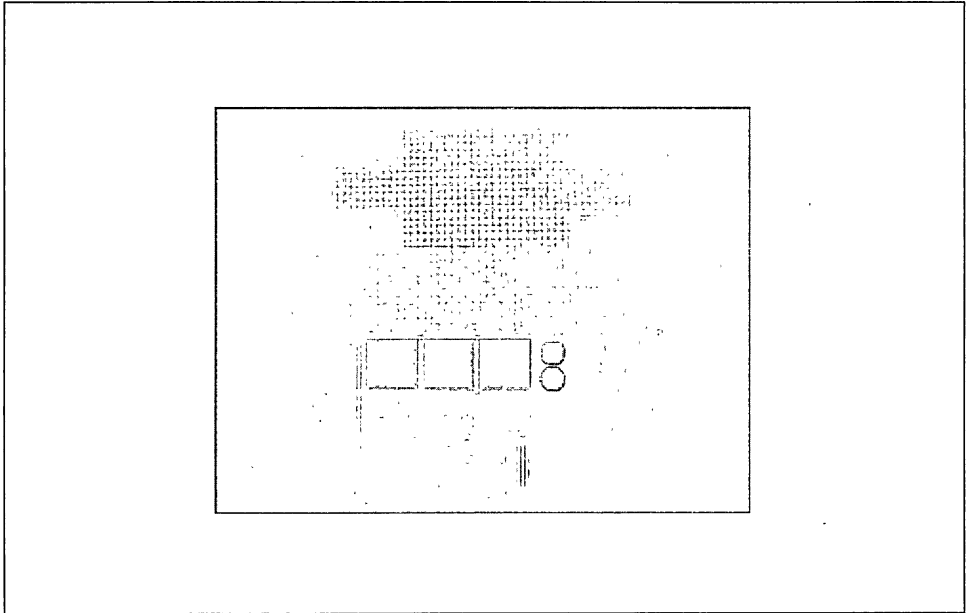


Figure 5. Die Layout of a VIPower chip - Note the thermal sensor inside the Power MOSFET



Driving the power MOSFET.

The power MOSFET output stage is driven by an internally generated gate voltage. A charge pump provides sufficient voltage to turn on the gate.

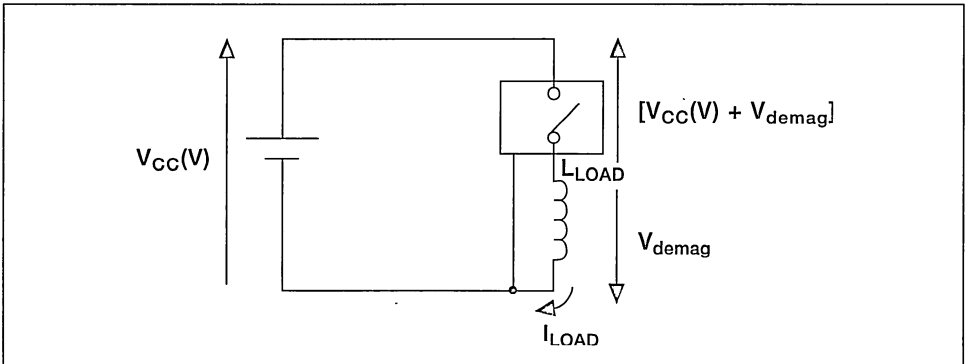
Turn-on

As previously explained, the High Side Drivers are turned-on with a controlled di/dt.

Turn-off: Normal and fast load demagnetization

When a High Side Driver turns off an inductance a reverse potential appears across the load. The source of the power MOSFET becomes more negative than the ground until it reaches the demagnetization voltage, V_{demag} , of the specific device. In this condition the inductive load is

Figure 6. Inductive load demagnetization turn-off for the VN20N family



demagnetized and its stored energy is dissipated in the power MOSFET according to the equation shown below:

$$P_{\text{demag}} = 0.5 L_{\text{load}} [I_{\text{load}}]^2 \times \frac{[V_{\text{cc}} + V_{\text{demag}}]}{V_{\text{demag}}} \times f$$

where f is the switching frequency and V_{demag} the demagnetization voltage.

In the basic High Side Driver family the typical value of, $|V_{\text{demag}}|$ is = 4V.

In the I.S.O. and industrial series, to reduce the dissipated energy, an internal circuit has been added in order to have a typical $|V_{\text{demag}}| = 18V$.

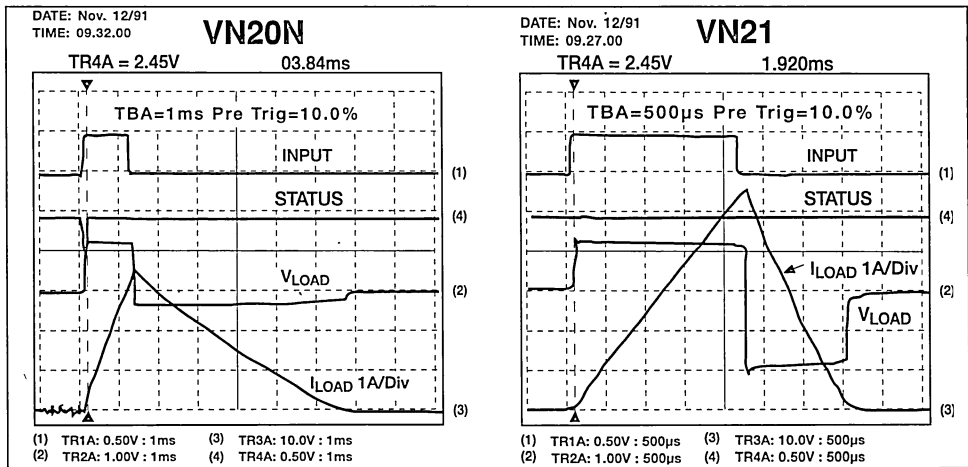
In this condition the stored energy is removed rapidly and the power dissipation in the power MOSFET is reduced - see equation. Figure 7a/b compares the waveforms of the normal and fast demagnetization techniques.

Figure 7b shows the VN21 driving an inductive load. During the on period, the current in the load rises linearly to a maximum. At turn-off the current

decrease linearly, but, at a sufficiently fast rate for fast demagnetization of the load. There is no fault output from the status pin. In the VN20N, the basic High Side Driver with no special feature for fast demagnetization, the turn-off takes up to 5 times longer than the VN21. Note that the status output will pulse at turn on because the internal circuit detects a very short duration open load, see figure 7a.

The maximum inductance which causes the chip temperature to reach the shut down temperature in a specified thermal environment, is a function of the load current for a fixed V_{CC} , V_{demag} and switching frequency. This is the maximum rate at which the drivers can be demagnetized. Figure 8 shows the maximum inductance for a given load current for devices meeting I.S.O. requirements, assuming a chip temperature of 160°C at turn-off and a supply voltage of 13V. The values are for a single pulse with 85°C case temperature. Note that the devices are not protected against overtemperature during turn-off.

Figure 7. VN20N-VN21 Driving an Inductive Load

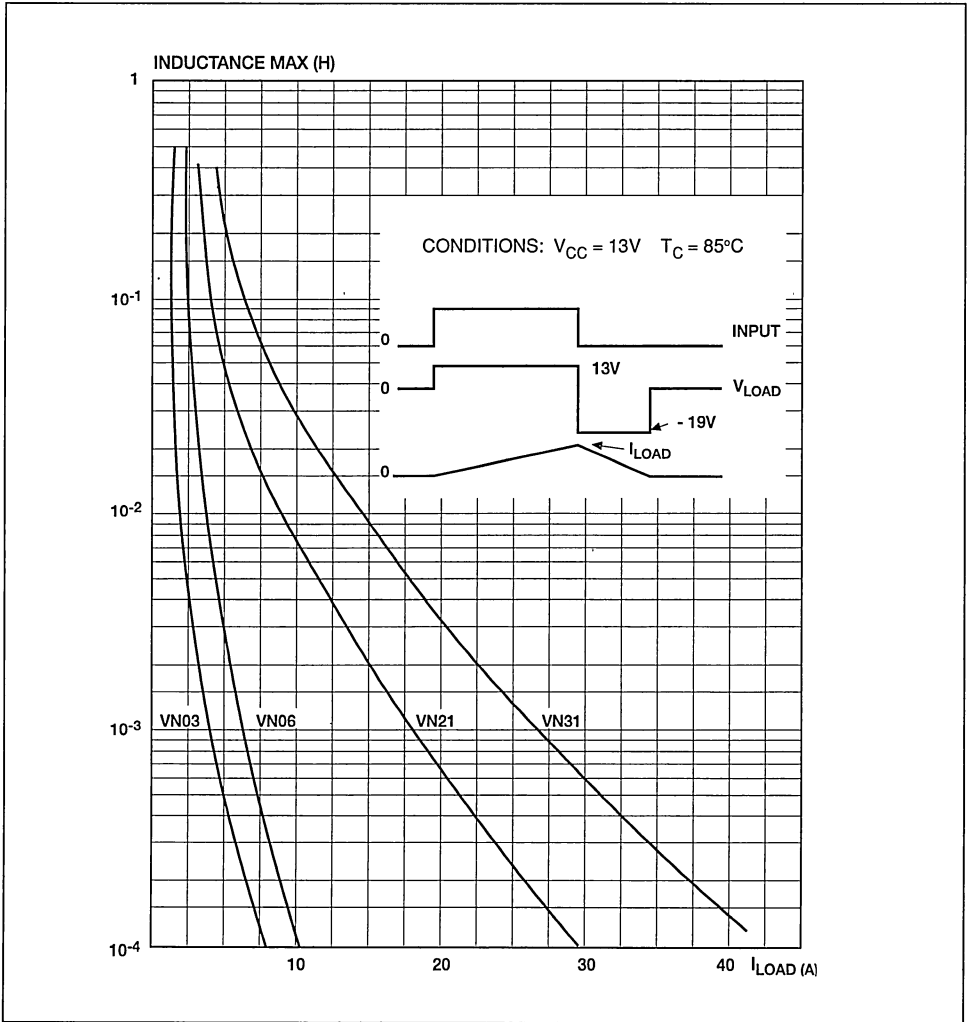


Additional Features of the High Side Drivers

High Side Drivers are designed for use in various market segments, the precise requirements of the drivers varying a little with the application. There are additional features to accommodate these requirements.

To reduce the on-state quiescent current for some applications, particularly industrial ones, the open load detection circuit is not included. There will consequently also be a lower power dissipation, an important point when similar, multiple High Side

Figure 8. Max inductance which produces a temperature of 160°C at turn off with $V_{CC} = 13V$. The values are for a single pulse with $T_c = 85^\circ C$



Drivers are mounted on one board. It can mean the difference between using or not using a heatsink. The operating voltage range can vary e.g. 5.5V to 26V for automotive applications and 7V to 36V for process control. Some devices have fast demagnetization of the load, ground disconnection protection, on- and off- state open load detection and 5ms filtering of the status output.

Status output and status output signal filtering.

The difference in electrical behaviour between the non-filtered and the filtered High Side Drivers is that the status output filtering circuit provides a continuous signal for the fault condition after an initial delay of about 5ms in the filtered version. This means that a disconnection during normal operation, with a duration of less than 5ms does not affect the

status output. Equally, any re-connection during a disconnection of less than 5ms duration does not affect the status output. No delay occurs for the status to go low in case of overtemperature conditions. From the falling edge of the input signal the status output initially low in fault condition (overtemperature or open load) will go back high with a delay t_{POVL} in case of overtemperature condition and a delay t_{POL} in case of open load. These features fully comply with International Standards Office, (I.S.O.), requirements for automotive High Side Drivers.

ABNORMAL LOAD CONDITIONS:

Load short circuits

Should a load become short circuited, various effects occur and certain steps need to be taken to deal with them, particularly choosing the correct heatsink. Two clear cases of short circuit occur:

1. The load is shorted at start-up.
2. The load becomes short during the on-state.

Start-up with the load short circuited.

At turn-on the gate voltage is zero and begins to increase. Short circuit current starts to flow and power is dissipated in the High Side Driver according the formula:

$$P_d = V_{DS} \times I_D$$

The effect is to cause the silicon to heat up. The power MOSFET stays in the linear region. When the silicon temperature reaches about 160°C the over temperature detection operates and the switch is turned off. Passive cooling of the device occurs

until the reset temperature is reached and the device turns back on again. The cycle is repetitive and stops when the power is removed, the input taken low or the short circuit is removed.

Even in this configuration, the device controls the di/dt. Figure 9 shows a start-up when there is a short circuited load driven by a VN05N. The initial peak current is 30A for this 180mΩ device.

A short circuit occurring during the on-state.

When a short circuit occurs during the on-state, the power MOSFET gate is already at a high voltage, about $V_{CC} + 8V$, so the gate is hard on. Hence the short circuit di/dt is higher than in the first case, and only controlled by the load itself. After the steady state thermal condition is reached, thermal cycling is the same as in the previous case.

Automatic thermal cycle.

The thermal cycling in overload conditions produces repetitive current peaks. The device switches on, the silicon heats up until the over-temperature sensing acts to turn the device off. The rate of passive cooling depends on the thermal capacity of the thermal environment. This, in turn, determines the length of the off-state during thermal cycling.

It is important to evaluate the average and RMS current during short circuit conditions. This is required in order to determine the track dimensions for printed circuit boards and the correct value for any fuse used. In all practical situations there is no danger to pcb tracks from these high peak current for track designed to handle the nominal load current.

Figure 9. Automatic Thermal cycle at start - up with the load short - circuited.

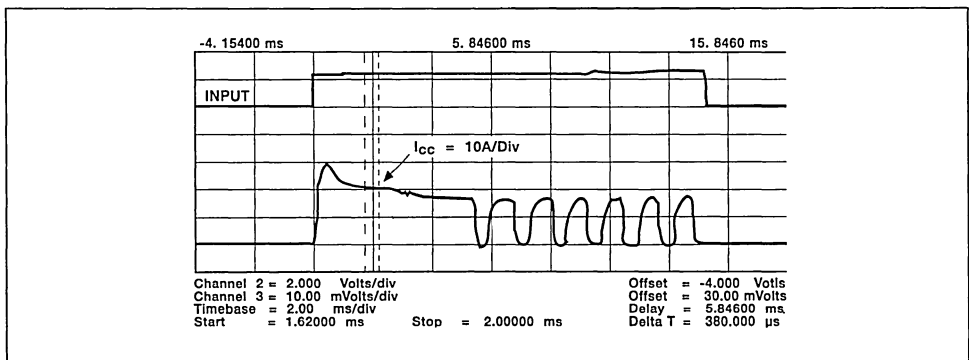


Figure 10. Automatic thermal cycle for a short circuit occurring during the on - state

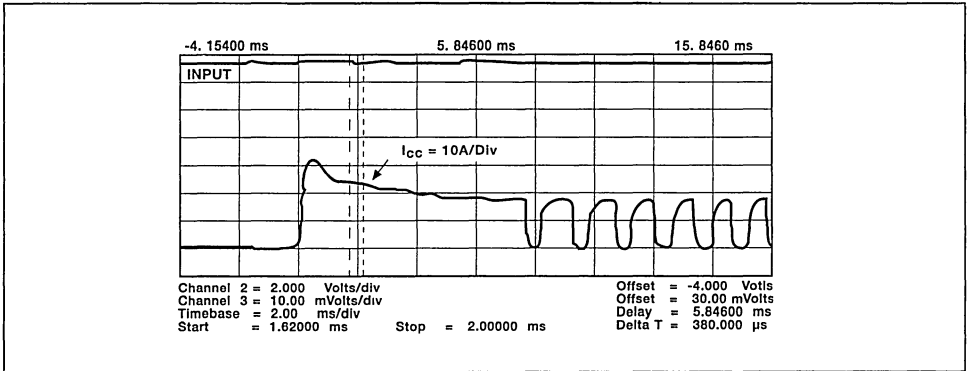
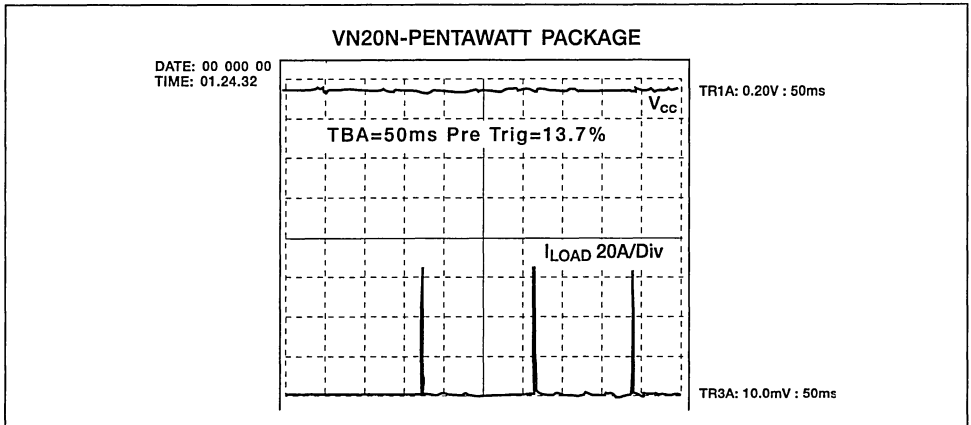


Figure 11. Automatic Thermal cycle in overload condition



Evaluating the Average current

In steady state conditions the junction temperature oscillates between T_j (shutdown) and T_j (reset).

$$T_j(av.) = (T_j(\text{shutdown}) + T_j(\text{reset})) / 2 \approx 135^\circ\text{C}$$

Dissipated power:

$$P_D = I_{(AV)} \times V_{CC}$$

For a specific package

$$P_D = (T_{J(AV)} - T_{case}) / R_{thj-case}$$

$$I_{(AV)} = (T_{J(AV)} - T_{case}) / (R_{thj-case} \times V_{CC})$$

Note that $I_{average}$ does not depend on the peak current $I_{(PK)}$.

Example:

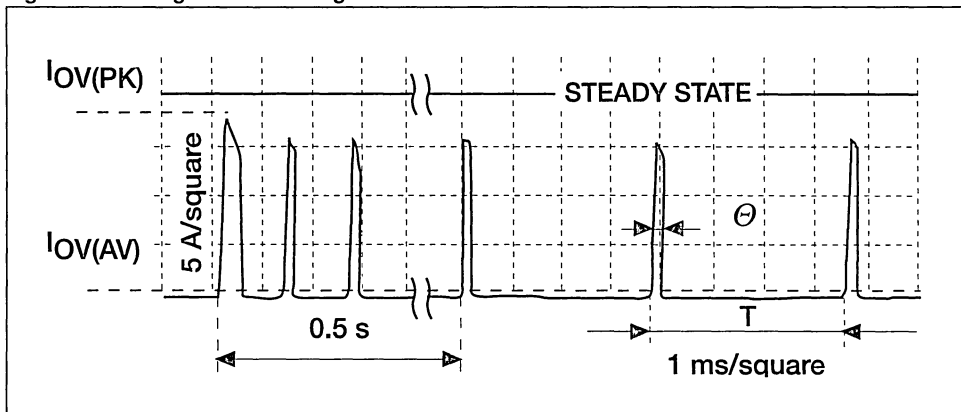
VN21 with $T_{case} = 85^\circ\text{C}$ has an average current, $I_{(AV)} = 3.85\text{A}$,

at $R_{thj-case} = 1^\circ\text{C/W}$ and $V_{CC} = 13\text{V}$

The average current is independent of the peak current.

Generally, a current limiter does not decrease the average current.

Figure 12. Average current during an hard short - circuit test



Evaluating the RMS current

The RMS current, I_{RMS} , generates heat in the copper track on PCBs during short circuits.

$$I_{RMS}^2 = 1/T \int_0^T I^2(t) dt$$

$I_{RMS} = I_{PK} \times \sqrt{\Theta/T}$, where Θ/T is the duty cycle.

with $I_{AV} = 1/T \int_0^T I(t) dt = I_{PK} \times \Theta/T$

$$I_{RMS} = \sqrt{I_{PK} \times I_{AV}}$$

The RMS current increases proportionally to the square root of the peak current $\rightarrow +40\%$ if I_{PK} is doubled. Schemes to limit the current do not decrease the RMS current significantly.

Heatsink requirements.

Overload protection is based on device heating. If you want to detect an overload, i.e. a damaged load, the chip must be allowed to heat up so that the thermal sensor located on the chip is activated. This leads to the following general rules for sizing heatsinks for the VN High Side Drivers.

1. Do not use a too big heatsink.
2. Do not use a VN device which has R_{ON} much lower than that which the application requires.

This example illustrates a specific case.

Conditions:

- a supply voltage of 14V,
- a load resistance of 2Ω ,
- VN20N - $R_{DS(on)}$ at $25^\circ\text{C} = 50\text{m}\Omega$

- load current = 7A

To detect an over current of 20A, assuming that $R_{DS(on)}$ at $150^\circ\text{C} = 100\text{m}\Omega$ (see datasheet) hence:

$$P_D = (20)^2 \times 100 \times 10^{-3} = 40\text{W}$$

R_{thj-a} should be dimensioned for

$$\Theta_{\text{thermal shutdown}} - \Theta_{\text{Ambient}} < P_D \times R_{thj-a}$$

For example $160^\circ\text{C} - 25^\circ\text{C} < 40\text{W} \times R_{thj-a}$

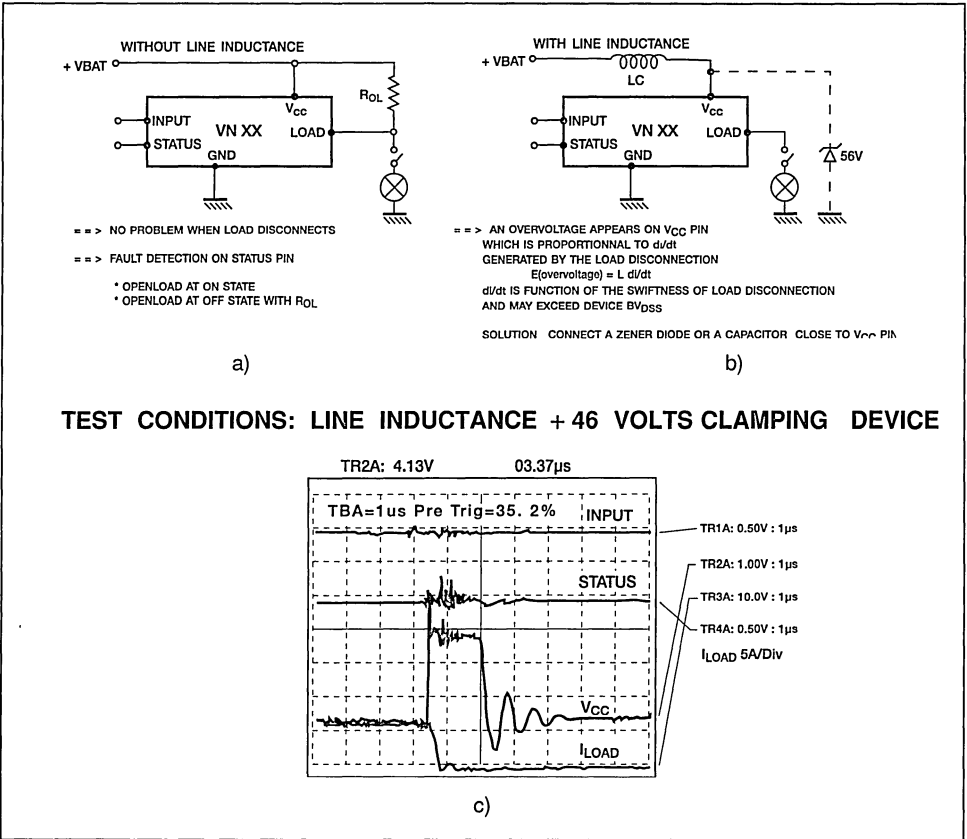
The effects of load disconnection.

When a load becomes disconnected there can be over-voltages caused by the change of load current. Figures 13 a and b summarize the likely effects. Figure 13a, shows a load driven by a VN21. The supply to the VN21 has a very low parasitic inductance. When the load becomes disconnected, the current changes at a rate determined by the time taken for the load to disconnect. This controls di/dt .

In this present case, there is virtually no inductance in the supply line. Hence no over-voltage is generated and V_{CC} is unaffected. The status pin goes low to indicate an open-load state

In the second case illustrated, figure 13b, the supply line has parasitic inductance and capacitance. When the load is disconnected an over-voltage is generated, ($V_{\text{over-voltage}} = L di/dt$). The di/dt is not controlled by the device but by how fast the load is disconnected. It is possible that the over-voltage may exceed the breakdown voltage of the device. It is a wise precaution where the supply connection pins are likely to have some inductance, to use a

Figure 13: a) Turn-off with low line inductance b) Turn-off with high line inductance c) Behaviour of VN21 during load disconnection



56V zener diode or a capacitor close to the supply pin of the switch. Figure 13c shows a test made using a zener clamp to overcome line inductance.

PROTECTION AGAINST GROUND DISCONNECTION

There are a number of distinct situations that can occur when one of the ground connections is broken in circuits using the High Side Drivers.

The first case, shown in fig. 14a, is when the GND pin of the High Side Driver is disconnected while the μC and the load are connected to ground. In this case in the I.S.O. and industrial High Side Drivers nothing happens and the device remains off. In the VN20N family a voltage of about 2V appears on the load and consequently there is a power dissipation:

$$P_D = (V_{CC} - 2) \times I_{LOAD}$$

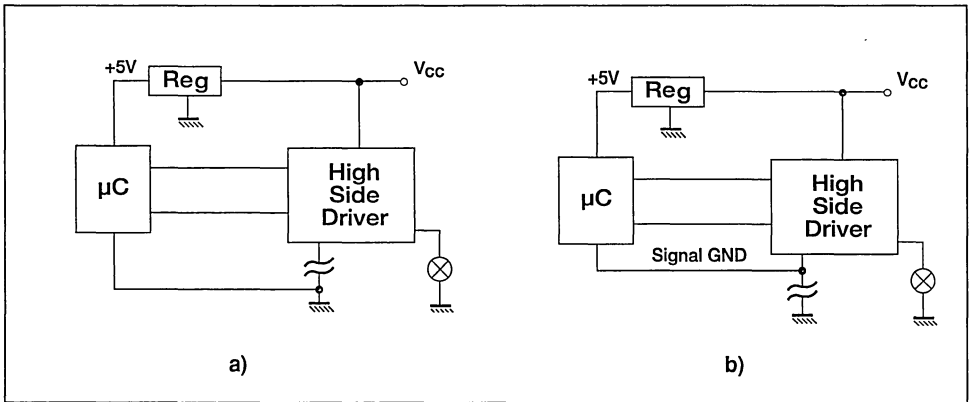
usually very low. In these conditions the diagnostic is not functioning.

The second case, shown in fig. 14b, is when both the GND pins of the High Side Driver and of the μC are disconnected while the load is connected to ground. In this situation the signal GND rises up to V_{CC}. In the I.S.O. and industrial High Side Drivers nothing happens up to V_{CC}<18V and the diagnostic output remains in high state at V_{CC}. In the VN20N family a voltage of about 4V appears on the load and consequently there is a power dissipation:

$$P_D = (V_{CC} - 4) \times I_{LOAD}$$

If P_D is excessive with respect to the heatsink capability, destruction may occur since the

Figure 14. Ground disconnection of High Side Driver: a) μC and load remain grounded
b) Load only remains grounded



protections are not functioning. The load is permanently activated.

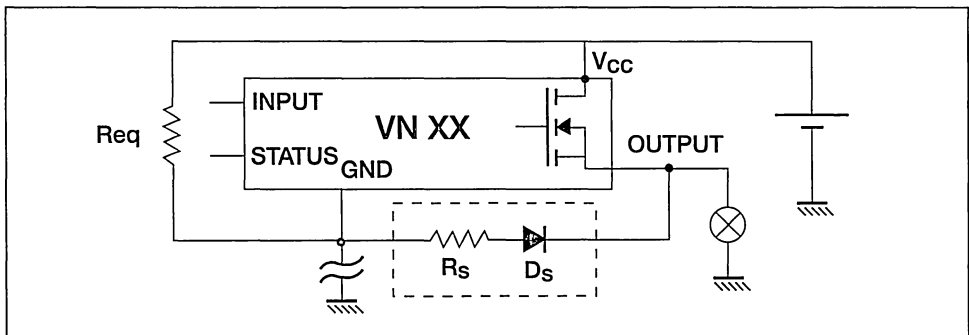
Another practical case is when an external component supplies current to the High Side Driver GND pin which is disconnected from the ground. This might occur if the VN device is mounted on a local PCB with other devices and has a local ground while the load may be grounded to the frame or body of the equipment, figure 15. Also, in this case, for internally protected devices, the output remains off up to the point where the voltage on the GND pin is $\leq 18\text{V}$ with reference to real ground at 0V . This will reduce the maximum V_{CC} the High Side Driver is able to withstand before turning on with the control circuit in-operative. One solution to this problem is to insert a resistor and diode in between the device

GND pin and the output pin. The series resistor, R_s , must be calculated so that the sum of the current, I_s , of the High Side Driver chip connected to the GND node plus the current drawn by the external elements, produces a voltage drop of less than 18V across $R_s + D_s + R_{\text{load}}$ for I.S.O. or industrial High Side Drivers and less than 2V for STD devices.

CONCLUSION

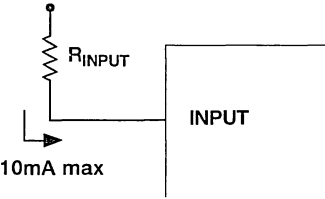
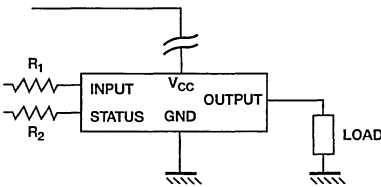
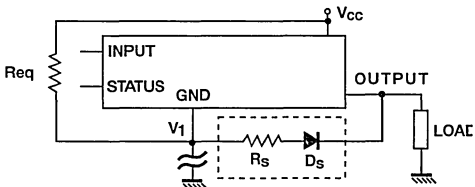
The VN series of High Side Drivers offers designers a highly attractive method of controlling a variety of inductive and resistive loads. The option to use a selection of extra features such as fast demagnetization or status filtering makes them equally suitable for general or specialised use, typically in the automotive environment.

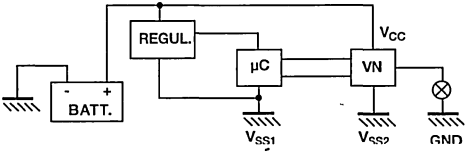
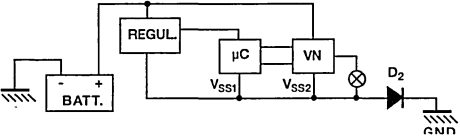
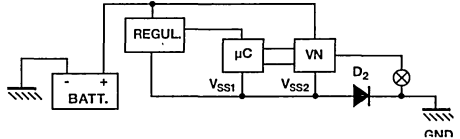
Figure 15. Ground disconnection occurring when an equivalent resistor supplies current on the GND pin.



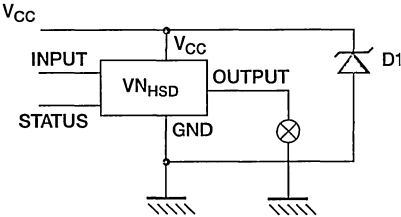
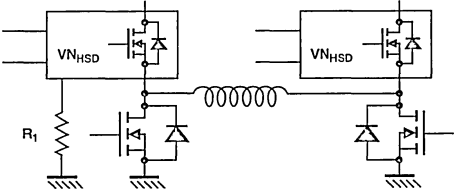
	SYMPTOM	DEVICE	COMPONENT	COMMENT	SCHEMATIC	NOTES
1	Off-state open load detection	VN03 VN06 VN21 VN31	R_{EXT}	It is necessary to set the current that fixes the voltage, V_{LOAD} , in the off state. When R_{LOAD} fails - goes open or high resistance - V_{LOAD} increases and an internal comparator triggers the status flag to go low.		<p>Choose R_{EXT} to match V_{DD} to fix $I_{OL(off)}$. The threshold V_{LOAD} is fixed at V_{REF}.</p> $I_{OL(off)} = (V_{DD} - V_{REF}) / R_{EXT}$ <p>The open load detection in off-state is only possible for a nominal value of $R_{LOAD} \ll 10k\Omega$</p>
2	Voltage spike on V_{CC} when load disconnects.	ALL	D4 or C1	If the line inductance is not zero and di/dt caused by disconnection of the load is high, an over voltage $E = L di/dt$ appears on V_{CC} . The V_{BRIDSS} of the output power MOSFET could be exceeded.		<p>Use a 56V zener diode to clamp V_{CC} or put a capacitor, C1 (about 100nF), near V_{CC} pin.</p>
3	Over voltage on V_{CC} from external circuit	ALL	D4 or R_{LIM}	D4 can be used as a decentralized clamp (V_{CC} clamp and energy clamp). Otherwise a resistor, R_{LIM} , can be added on the ground pin to limit the current in the signal section of the device in case it exceeds the signal path breakdown voltage.		<p>$R_{LIM} = 150\Omega$ is a general value to protect devices from the effects of a load dump. Refer to the specific data sheet.</p>

	SYMPTOM	DEVICE	COMPONENT	COMMENT	SCHEMATIC	NOTES
4	Supply reversal	ALL		Refer to the equivalent schematic seen by user through pins: Load, Input, GND		<p>*$V_{CC} > 1V$ \rightarrowMGND"ON"\rightarrowVSS= GND Normal case $\cdot -4 < V_{CC} < 0$ \rightarrowMGND OFF \rightarrowNo current across input and GND pins \rightarrowA DC current flows in the load and DBody</p> <p>WARNING : If the load is an inductance with a parallel free wheeling diode, the user sees 2 forward biased diodes between GROUND and V_{CC}. \rightarrowDo not exceed i_{max} to prevent damage.</p>
5	Supply reversal - case 1	ALL		Battery connection reversed; correct connection of the High Side Driver devices.		<p>If the battery is short circuited by 3 x 2 series diodes (typically an alternator diode configuration) the supply voltage, V_{CC}, is clamped to about -3V and no damage occurs to the VN device.</p>
6	Supply reversal - case 2	ALL	D1 or D2	High Side Driver reverse connected with the battery correctly connected.		<p>V_{CC} for the device is -13V. To prevent damage to the device use either a bipolar or Schottky diode in series with the ground pin connection. Use R1 and R2 to limit the negative current in the input and status pins because the internal ground drops to V_{CC}.</p>

	SYMPTOM	DEVICE	COMPONENT	COMMENT	SCHEMATIC	NOTES
7	Input driving.	ALL	R_{INPUT}	Driving the input from a voltage greater than 6V		To drive the input from a line voltage > 6V insert a series resistor to limit the input current $I_{INmax} < 10mA$
8	Pin disconnection - V_{CC}	ALL	R1 R2	Driving an inductive load, this kind of disconnection has the same electrical effects as V_{CC} reversal.		<p>1) Resistive load - no problem of damage.</p> <p>2) Inductive load - V_{CC} reversal occurs. If current and inductance of leads are too high the device may be damaged but the safety margin is wide - up to 100mH and 8A for the VN21</p> <p>In this case, input and status pins are pulled to a negative voltage so it is recommended to insert resistors in series with these pins in order to protect the μC.</p>
9	Pin disconnection - Ground	VN03 VN06 VN21 VN31 VN02AN VN20AN		An external component, R_{eq} , supplies current to the High Side Driver GND pin. The local ground is separate from the load ground.		The devices are internally protected (output stage off) if the voltage on the GND pin is $\leq 18V$ with reference to the real ground at 0 V. To avoid the High Side Driver to turn-on if GND is over 18V is possible insert R_s and D_s as shown in figure. Choose R_s so that $V_1 < 18V$

	SYMPTOM	DEVICE	COMPONENT	COMMENT	SCHEMATIC	NOTES
10	Ground potential differences	ALL		Voltage range for all High Side Drivers is defined between V_{CC} and V_{SS2} (V_{Nxx} GND). All voltages V_{IL} , V_{IH} , V_{USD} are referred to V_{SS2} .		If V_{SS1} and V_{SS2} are different, recalculate V_{IL} , V_{IH} , V_{USD} and beware of application bugs. (See points 11/12/13/14)
11	Ground potential differences - case 1	ALL	D2	Using power diode to withstand reversed battery. Case 1: $V_{SS1} = V_{SS2} \neq$ GND with $V_{SS1} >$ GND		Voltage losses in power diode. Input and status levels are not affected. Under-voltage shutdown level increased by diode V_F . Off-state open load level, V_{REF} , increased by V_F . A general rule is: level shift is ($V_{SS2} - \text{GND}$).
12	Ground potential differences - case 2	ALL	D2	Using a diode to protect the High Side Driver against reversed battery. (See point 6 above) $V_{SS1} = V_{SS2} \neq$ GND with $V_{SS1} >$ GND		The input and status are unaffected. $V_{USD} = (V_{SS2} - \text{GND}) + V_{USD0}$. Off-state open load level, V_{REF} , is increased by ($V_{SS2} - \text{GND}$). Not suitable if the μ Controller uses an analog transducer referred to ground.

	SYMPTOM	DEVICE	COMPONENT	COMMENT	SCHEMATIC	NOTES
13	Ground potential differences - case 3	ALL	R1, D2	Using a diode to protect the High Side Driver against reversed battery. $V_{SS1} \neq V_{SS2}$ $V_{SS2} > V_{SS1}$		V_L and V_{IH} shifted by $(V_{SS2} - V_{SS1})$. $R1$ limits any negative current when the μ Controller takes I/O to ground. On the status pin the zero corresponds to the V_p of $D2$. V_{USD} and V_{OL} being increased by $(V_{SS2} - GND)$.
14	Ground potential differences - case 4	ALL	R2, D2	Using a diode to protect the μ C against reversed battery. $V_{SS1} \neq V_{SS2}$ $V_{SS2} < V_{SS1}$		In fault conditions the device pulls the status pin down to V_{SS2} and the μ Controller sees a negative voltage - $(V_{SS1} - V_{SS2})$. There is a risk of latch up for the μ Controller CMOS output. Add $R2$ to limit the current. Undervoltage and off-state open load levels are not shifted.
15	Summary of the influence of ground differences, pin disconnections and over voltage protection.	ALL	R1, R2, D2, D7.	Recommended scheme		<ul style="list-style-type: none"> * common ground for μController and VN device * Reversed battery protection - Schottky diode * Series resistor for input and status pins * Over-voltage protection - bi-directional Zener

	SYMPTOM	DEVICE	COMPONENT	COMMENT	SCHEMATIC	NOTES
16	Load dump: battery disconnection whilst the alternator is working	ALL	D1	High voltages can be generated if the battery is disconnected when the generator is running in a car. Damaging effects can be overcome by using a clamping diode with at least $V_{BR} > 26V$ as 2 x 12V batteries are often used to jump start cars. This for overvoltage transient higher than specified in datasheets.		Protection against over-voltages are efficient if connected between pin 3 (V_{CC}) and pin 1 (ground).
17	$V_{LOAD} > V_{CC}$ (Bridge circuit)	ALL	R1	In full bridge applications during the demagnetization phase $V_{LOAD} > V_{CC}$. A current will flow out of GND pin, possibly damaging the bonding.		Insert a resistance, R1 (suggested value 47Ω), in the ground pin to limit the ground current and avoid damaging the bonding.

CAR IGNITION WITH IGBTs

by M. Melito

ABSTRACT

IGBTs are used in a variety of switching applications thanks to their attractive characteristics, particularly their peak current capability, ruggedness and simple gate drive requirements. Until recently their use was limited to the electrical drive sector, where they were required to be fast like Power MOSFETs and to have low conduction losses like BJTs.

As automotive ignition switches operate at low frequencies, they are not required to be

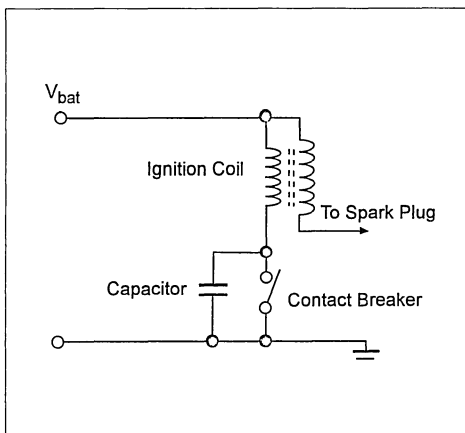
very fast. However they must have very low $V_{CE(sat)}$, and be very rugged. Existing technology allows a compromise between switching speed, ruggedness and power dissipation.

This paper gives a brief explanation of the physics and structure of the device, and highlights the characteristics which make IGBTs particularly suitable as power switches in automotive ignition systems.

1. INTRODUCTION

The inductive discharge ignition has evolved very little in its basic structure since its origin. The topology of this system using an ignition coil, contact breaker (points) and capacitor is shown in figure 1.

Figure 1: Inductive Ignition schematic



1.1 Conventional ignition systems

As the car engine rotates, the points close allowing a current to flow in the ignition coil. As the fuel-air mixture to be burnt reaches maximum compression in the cylinder, the points open, so interrupting this current and causing a large over-voltage pulse on the primary of the ignition coil. This pulse is converted by the coil to a voltage sufficient to produce arcing across the sparkplug, which ignites the fuel.

A capacitor is connected across the points to limit the rate of rise of voltage when the contacts open, so suppressing unwanted arcing which causes contact wear and reduces system output.

The performance of this type of ignition system falls significantly at high R.P.M., with low battery voltages (e.g. during starting) or

with fouled plugs.

Also, even with the capacitor connected across the points some arcing does occur, causing wear and consequently timing variations. Modern inductive discharge ignition systems remove these limitations.

One of the weaknesses of the circuit of fig.1 is the points, which have a restricted current carrying capability, and limited rate of voltage rise on opening. Introduction of semiconductor components to replace these has led to significant improvements in overall performance and reliability of automotive ignition switching systems.

1.2 Electronic alternatives

If an electronic switch is used to switch the ignition coil current, then the points can be used only to switch a small non-inductive sensing current, or can even be eliminated by using more reliable electronic sensors (such as Hall-effect or magnetic).

This allows the use of a low inductance, higher peak current ignition coil, resulting in an improved performance at high R.P.M. and better firing of fouled plugs.

To further improve system reliability more modern automotive ignition systems do not use a distributor, whose function is instead performed by a specially designed ignition coil. This is the basis of the transistor assisted ignition system.

It should be noted that unless a special ignition coil is used, there is a little to be gained in performance by adding a transistor assisted ignition to an automobile.

1.3 Specification of an ignition switch

An automotive ignition switch must meet certain specifications concerning voltage and current rates, minimum energy handling capability in case of spark plug disconnection and driving requirements, over the whole temperature range.

The main requirements are related to :

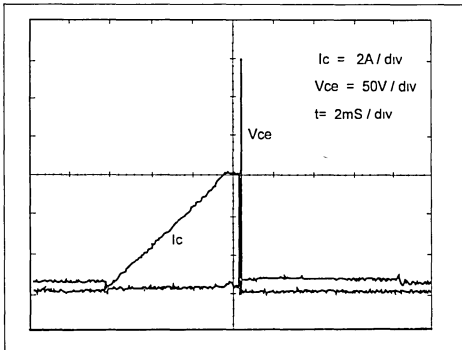
- Breakdown voltage
- Current and saturation voltage
- Safe Operating Area
- Input characteristics
- Temperature range and power dissipation.

1.3.1 Breakdown voltage

A pulse of 250-300 V on the primary side is normally easily sufficient to activate a spark. Of course the voltage peak on the spark plug will reach 20kV or more, because of the turn ratio, before the spark is actually ignited.

Immediately after this pulse both the primary and secondary voltages collapse, and during the spark they remain significantly lower than the peak (fig.2). Consequently the protecting Zener can not be made to operate below 350V, to ensure that the voltage pulse will be high enough.

Figure 2: I_C , V_{CE} Waveforms



The switch breakdown, which must be never exceeded, must therefore be specified at least 50 V higher than the Zener breakdown to give a reasonable safe margin. Currently IGBTs are available covering a range of BV_{CES} from 400V to 1500V.

1.3.2 Current and saturation voltage

The maximum permissible current density

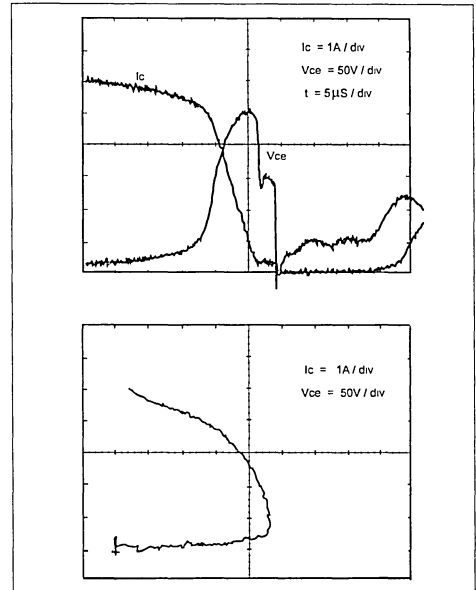
of an IGBT rated at 500V and 8A is up to twice that of a bipolar transistor with comparable ratings, in terms not only of breakdown and saturation voltage, but also in terms of Safe Operating Area. Consequently it is possible to achieve the same performance as a standard ignition Darlington with a smaller silicon area (and hence lower cost), or alternatively to have a better thermal resistance.

1.3.3 Safe Operating Area

The Safe Operating Area describes the capability of a transistor to withstand high levels of voltage and current at the same time. There are two main conditions that would subject an ignition switch to this combined stress:

- a) In normal operating condition the falling edge of the collector current during turn-off causes the collector voltage to rise until the spark occurs (fig. 3a,3b). During this phase the ignition switch must withstand high

Figure 3: a) I_C , V_{CE} waveforms during spark
b) Load line during spark

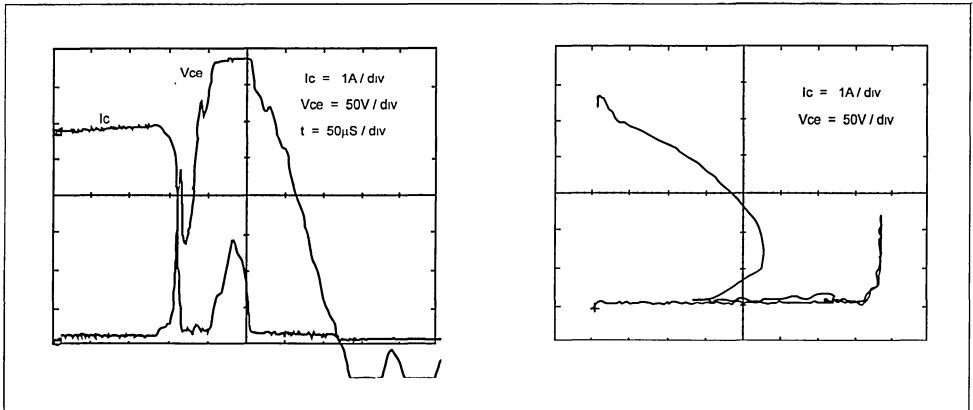


voltage and current levels simultaneously, without damage or degradation of reliability. This can be achieved only if the voltage and current levels are within the boundaries of the guaranteed turn-off (Reverse Bias) Safe Operating Area (RBSOA); otherwise an aid network is required to shape the voltage and current waveforms. Current technology allows the production of IGBTs with a square RBSOA whose voltage boundary is the BV_{CES} , and whose current limit is at least twice the nominal current of the device; thus an aid network is not needed.

b) In the case of disconnection of a spark plug, the ignition switch must be able to absorb the energy that the coil is unable to

release in the generation of the spark. All of the stored electromagnetic energy tends to concentrate across circuit parasitic capacitances, charging them to high voltages and putting the device in avalanche, with a risk of going into second breakdown and failing. This problem is overcome by dissipating this energy on the power switch through a protection Zener placed between the collector and the base of the device, which turns the device on as soon as the collector voltage exceeds the nominal Zener voltage (fig. 4a,4b). The usual way to indicate the minimum energy the switch can absorb without damage is to specify the battery voltage, the coil inductance and coil current,

**Figure 4: a) I_C , V_{CE} waveforms in case of spark plug disconnection
b) Load line in case of spark plug disconnection**



the clamp voltage for the Zener and, if present, the collector-to-emitter capacitance. With a reasonable margin for the current, e.g. 8A, the switch must survive the switch-off without load on the coil secondary side.

A battery voltage to the upper limit of its range would be the worst case, as the energy to dissipate is :

$$E = 0.5 * L_{coil} * I_{coil}^2 * \frac{V_{cl}}{V_{cl} - V_b}$$

The worst case I_{coil} will also be specified, and L_{coil} at its maximum possible value:

$$I_{coil} = 8A$$

$$L_{coil} = 7mH$$

$$V_b = 14V$$

Considering a clamping voltage of 400V the total energy is:

$$E = 232mJ$$

This kind of specification is usually referred to as the "use test" and it can be easily guaranteed for IGBTs .

1.3.4 Input characteristics

The ignition switch must be specified to ensure that the current and voltage available from the driving stage are enough to switch it on and off under all temperature conditions. The input characteristics of IGBTs are similar to that of a MOS, and they need a very small amount of energy for switching; a driving energy that is at least two orders of magnitude less than that needed by Darlingtons. Moreover, logic level IGBTs, such as the STGP10N50L, can be turned on with a gate voltage of as little as 3V.

1.3.5 Temperature range and power dissipation

The electronic components in an automotive environment are expected to work in the so called automotive under-hood temperature range, -40°C to 100°C.

However it is preferable to specify the critical parameters not only at room temperature, but also at the junction temperature

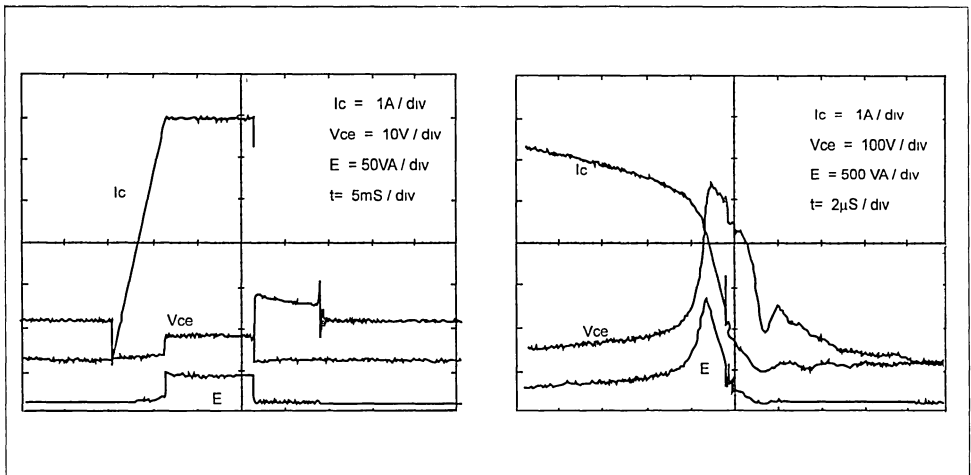
extremes of -40°C and 150°C due to the temperature increase caused by the electrical power dissipated in the device itself.

The power dissipation of an ignition switch in a high energy ignition system reaches a maximum during the current limiting interval, fig.5a, apart from a short, very high peak at the end of it due to the switch-off phase, fig.5b, and since the device is used in the linear mode the lower $V_{CE(sat)}$ has little influence in power dissipation. The junction temperature must be kept below its maximum allowable value by a heatsink whose thermal resistance must be calculated considering :

- the maximum ambient (under-hood) temperature,
- the maximum thermal resistance, junction to case, of the switch
- the thermal resistance, case to heatsink, due to the contact.

The final criterion cannot be ignored, as in some cases it can be comparable with the thermal resistance of the device itself.

Figure 5: a) I_C , V_{CE} , $V \cdot I$ waveforms
b) I_C , V_{CE} , $V \cdot I$ waveforms (expanded scale)

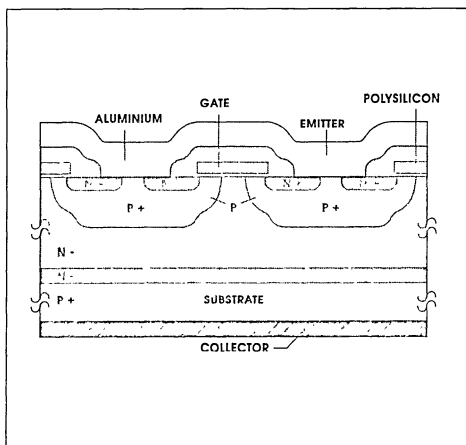


2. IGBT TECHNOLOGY AND CHARACTERISTICS

2.1 Structure

Except for the p^+ substrate, the silicon cross section of an IGBT (fig.6) is virtually identical to that of a standard Power MOSFET. Both devices have the same cellular design with p^+/p^+ body, n^+ source and polysilicon gate structure. In both devices the n^- material under the p bodies is sized in thickness and resistivity to sustain the full voltage rating of the device.

Figure 6: Basic structure of an IGBT



Although their structures are similar, the physical operation of the IGBT is very different from that of the Power MOSFET; the IGBT is a minority carrier device, and its behaviour is closer to that of bipolar transistor. This is due to the p^+ substrate which, during conduction, injects holes in the n^- region, significantly reducing its resistivity.

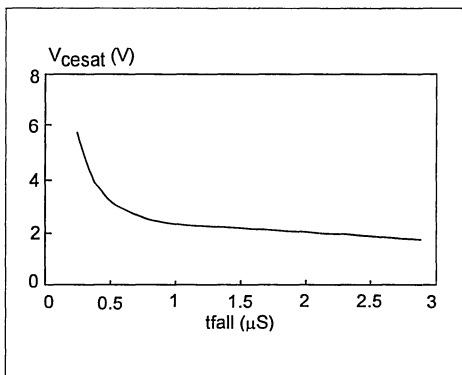
Because of the conductivity modulation, an IGBT has lower power losses than a Power MOSFET, and has a better efficiency than a bipolar transistor because the emitter covers the entire area of the die.

The switching speed of the IGBT is in general not as fast as a Power MOSFET, but this is not a limiting factor in this case because of the very low switching frequencies used in automotive ignition.

Due to the sandwiched layers of the device, the area with the extra p^+ layer forms a pnp bipolar transistor which defines the fall time of the IGBT. During turn-off the BJT portion has an open base, and switching only terminates when all the excess minority carriers within the base recombine. In a BJT, it is possible to increase the switching speed by extracting these carriers from the base, but with an IGBT it is not possible to access the base of the bipolar section. Consequently the turn-off is dominated by the lifetime of the minority carriers in the n^- region.

In order to improve the fall time in IGBTs, techniques such as electron beam irradiation and doping with lifetime killers have been used to control the lifetime of minority carriers. Structural design changes, such as the insertion of a n^+ buffer layer have also been introduced (fig.6). The optimization of these techniques in IGBTs has allowed t_{fall} and $V_{CE(sat)}$ tuning (fig.7) thus allowing the best compromise between switching speed, power losses and ruggedness over a wide range of applications.

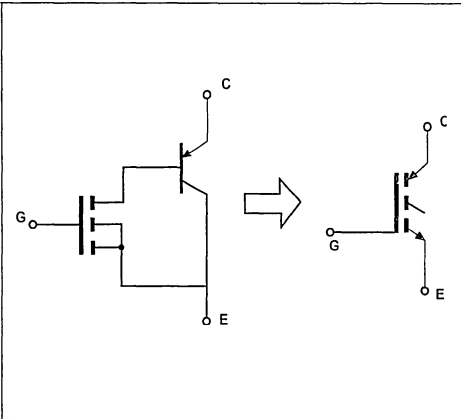
Figure 7: $V_{CE(sat)}$ versus t_{fall}



2.2 Output characteristics

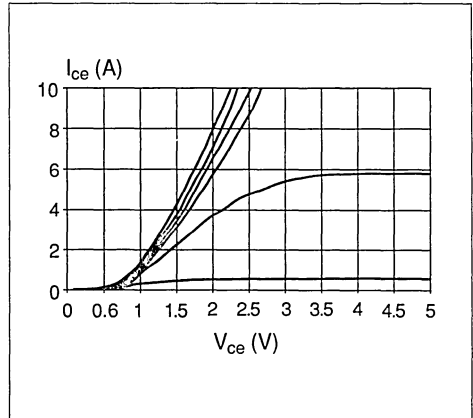
As a first order approximation the IGBT can be modelled as a pnp transistor driven by an n-channel Power MOSFET (fig.8). This model is very simple and does not take into account second order effects due to the common power MOSFET drain and BJT base region, but is useful to explain the characteristics of the IGBT.

Figure 8: Simplified equivalent circuit of IGBT, and JEDEC symbol



As is apparent from the equivalent circuit, the voltage drop across the IGBT is the sum of two components: a diode drop across the p-n junction, and the voltage drop across the driving Power MOSFET. Thus, like a Darlington, the on-state voltage drop across an IGBT never goes below a diode threshold. As the second stage of a pseudo-Darlington, the PNP is never in heavy saturation and its voltage drop is higher than that which could be obtained from the same PNP in heavy saturation. It should be noted, however, that the emitter of an IGBT covers the entire area of the die, hence its injection efficiency and conduction drop are much superior to that of a bipolar transistor of the same size. The typical output characteristics of an IGBT are given in fig.9.

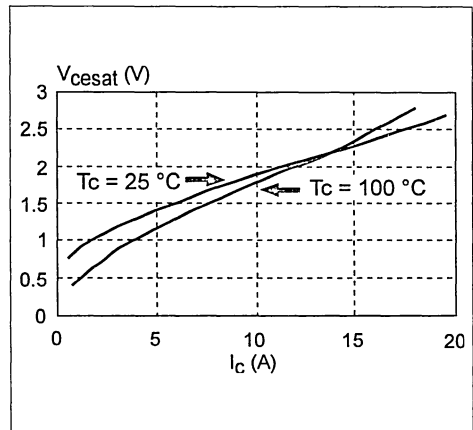
Figure 9: IGBT output characteristics



2.3 Temperature coefficient

The temperature coefficient of the $V_{CE(sat)}$ of an IGBT is similar to that of a bipolar transistor up to approximately $I_{C(max)}$. At this point the temperature coefficient becomes zero. At collector currents greater than $I_{C(max)}$, the temperature coefficient becomes positive and looks like that of a Power MOSFET. A typical temperature coefficient of $V_{CE(sat)}$ as a function of collector current for two junction temperatures is given in fig.10.

Figure 10: $V_{CE(sat)}$ versus I_c



2.4 Switching

Because of the similar structure, the switching behaviour of IGBTs in some aspects looks like a Power MOSFET, with the unavoidable intrinsic capacitances of the device added. In the same way the main parameters governing switching behaviour are the gate bias, the driving impedance, the gate charge and the stray inductances, but unlike the Power MOSFET the influence of the driving circuit on the current fall-time of IGBTs is negligible.

2.4.1 Turn-on

The turn-on behaviour of the IGBT is very similar to that of a Power MOSFET, and in a similar way it is possible to control the turn-on time by adjusting the gate voltage and the impedance of the driving circuit.

2.4.2 Turn-off

IGBT turn-off, shown in fig.11, can be divided into three consecutive phases:

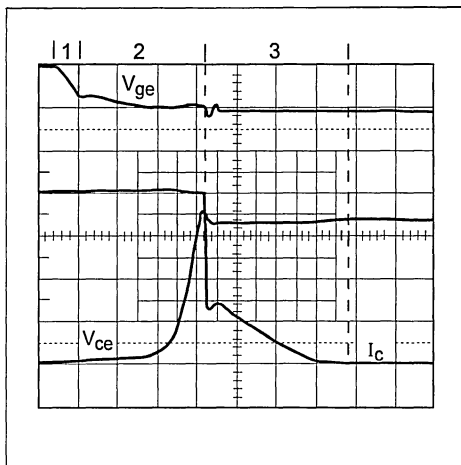
1) The gate voltage begins to decrease until it reaches the value when the Miller effect occurs; during this phase the collector voltage increases slightly changing the output characteristics with constant I_c .

2) This phase shows the Miller effect, and the gate voltage remains constant because of modulation of the collector gate capacitance. This is due to collector voltage rapidly increasing to its maximum value.

3) The collector current begins to fall quickly, and then continues with a "tail" which is due to recombination of minority carriers in the substrate.

The current tail, which causes the major part of the switching losses, is heavily related to technology, and its effect cannot be reduced by the driving circuit. The faster part of the collector current is due to the turn-off of the MOS portion of the IGBT structure. This part is connected to the PNP current gain, which, for ignition

Figure 11: IGBT turn off



devices, is designed to be relatively high to obtain a lower $V_{CE(sat)}$. The lower $V_{CE(sat)}$ is paid for with a longer current tail, see fig.7, but this price is acceptable because switching losses are negligible because of low switching frequency, compared to the losses during the on phase and during the current regulation. Moreover a very low $V_{CE(sat)}$ is important to allow the engine to start when the battery voltage is at its lower limit.

3. FUTURE IMPROVEMENTS

The structural characteristics of IGBTs lend themselves to improvements in similar ways to the developments made in Power MOSFET technology. Logic level IGBTs are available, and they can be directly interfaced to CMOS, TTL, PMOS and NMOS logic circuits, and microprocessors operated from 5V supplies. Moreover temperature sensing, current sensing, gate to emitter and collector to gate voltage clamping can be designed into IGBTs at the cost of a small increase of the silicon area and the addition of only one masking layer to the process.

The functions that can be obtained provide

significant improvement in ruggedness, reliability, protection and system cost reduction.

4. CONCLUSIONS

IGBTs are high voltage power switches which work with a very high current density. The drive simplicity coupled with excellent intrinsic ruggedness, the significant improvement in reliability, protection, system cost reduction and ruggedness improvement achievable by integrating additional functions in the same silicon make the IGBTs a very strong competitor in automotive ignition market.

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**THE VB027: ELECTRONIC IGNITION IN
VIPower™ TECHNOLOGY**

by M. Melito

ABSTRACT

This paper describes a solid state integrated ignition driver circuit designed to drive a high energy coil in a microprocessor based EMS (Engine Management System) under the direct control of a micro-controller.

The paper begins with a review of the principal characteristics of SGS-THOMSON Microelectronics' Vertical Intelligent Power technology, and then introduces the VB027, a novel fully-protected switch for electronic ignition which directly interfaces with a microprocessor controller.

INTRODUCTION

The trend for cleaner, lean-burn engines has lead to the increased use of microprocessor-based Engine Management Systems (EMS) with electronic ignition.

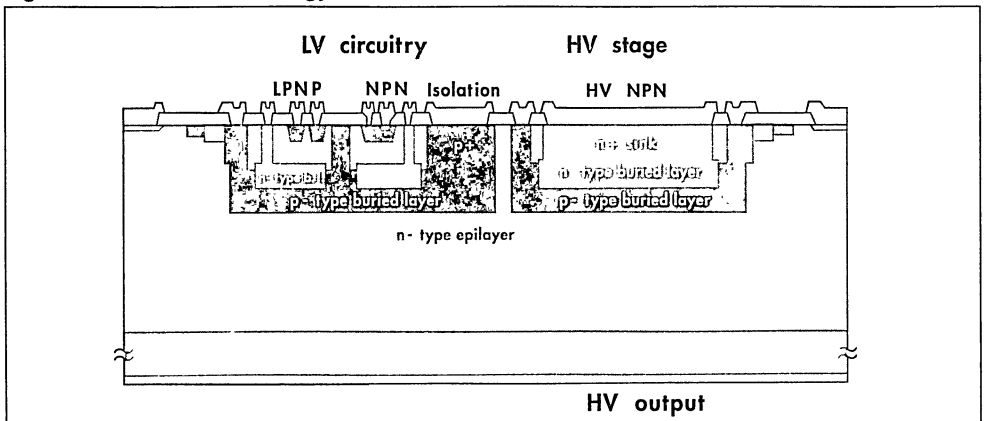
The main requirements for the power switch in ignition applications are for an easy to drive, rugged device capable of blocking 350 to 400 Volts and conducting 8 to 9 Amperes with less than a 2 Volts drop. Bipolar Darlingtion Transistors have traditionally been used, but recently alternatives have appeared on the scene. VIPower (Vertical Intelligent Power) devices are the most promising.

Smart power technologies attempt to close the gap between discrete power devices and integrated circuits. They have been developed with two goals in mind: to achieve the same current capability and breakdown voltage as a discrete power device, and to integrate smart functions with only a small increase in the cost of the device. These technologies are inevitably the result of a compromise between optimum power handling and signal processing versatility. VIPower M1 technology has allowed the development of a family of devices for automotive ignition, for example the VB027, that allows a simple logic-level driving circuit together with increased ruggedness. Moreover, the latest generation permits TO-220 packaging rather than TO-218 and, at the same time, offers more intelligence on a single chip.

TECHNOLOGY OVERVIEW

The VIPower M1 structure shown in Figure 1 combines a vertical current flow NPN power transistor and a low-voltage junction insulated IC on the same silicon substrate. The signal processing section is constructed inside a diffused p-type buried layer that takes the place of the reverse-biased p-substrate of conventional ICs, and must be connected

Figure 1. VIPower M1 technology overview

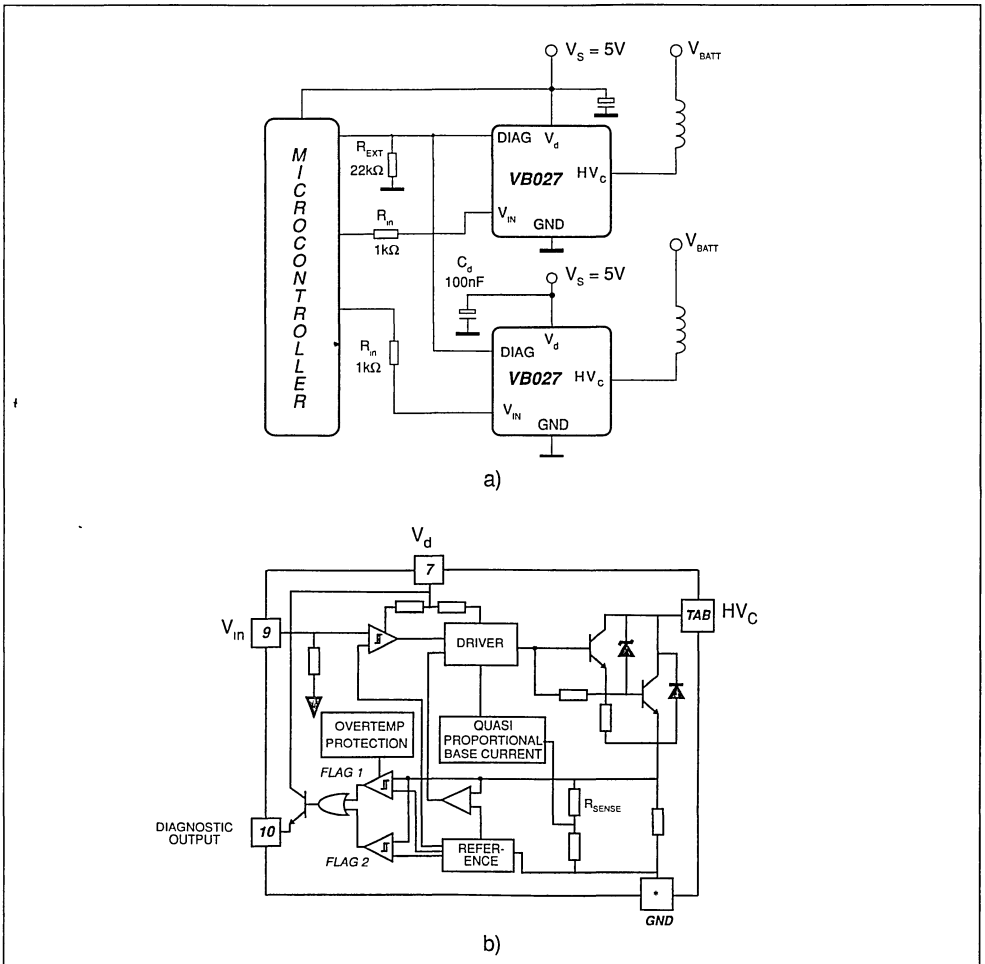


to the most negative supply. The selection of an n-type substrate as the starting point allows complete compatibility between vertical NPN and IC fabrication steps. As in standard power NPN, the thickness and resistivity of the first epi layer set the BV_{CEO} and the ruggedness of the high voltage device, whereas the second epi growth defines the characteristics of the low voltage device. The choice of a suitable value for the substrate thickness and resistivity, together with an appropriate edge termination, allows the structure to handle any blocking voltage up to 1.2kV.

FUNCTIONAL DESCRIPTION

The VB027 is a solid state integrated ignition driver circuit designed to drive a high-energy coil under the direct control of a micro-controller. It is constructed utilising VIpower M1 technology, the Vertical Intelligent Power technology from SGS-THOMSON Microelectronics. The typical system configuration and block diagram of the device are shown in figure 2.

**Figure 2. a) Application circuit
b) Block diagram**



Its main features are:

- minimum external components required
- coil current limit internally set
- built-in collector-emitter voltage clamping
- TTL/CMOS compatible input
- output diagnostic to microprocessor for dwell angle control and overtemperature protection
- die-size compatible with TO-220 package.

The input V_{in} of the VB027 is fed by a low power signal generated by an external controller that determines both dwell time and ignition point.

During V_{in} high, Figure 3, the power output of the VB027 is turned on and the current in the primary of the ignition coil increases until it reaches the internally

set maximum current level.

The device then regulates the output current in a stable dwell regulation loop through an internal sensing resistor.

A voltage signal is generated on the diagnostic output to inform the micro-controller of the primary coil current level. The diagnostic signal goes high typically when the coil current exceeds 4.5A, and low when it exceeds 5.8A. This information allows the micro-controller to govern the dwell angle and to detect coil saturation. The spark is generated by turning off the device, which is under the control of the micro-controller through the diagnostic line. An internal clamping device ensures that the voltage on the primary output is limited typically to 360V, even in case of spark plug disconnection: see Figure 4.

Figure 3. Normal operating cycle

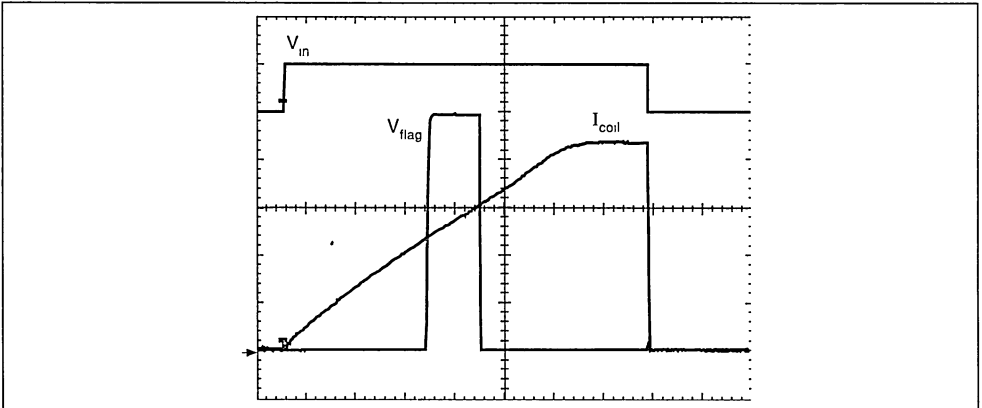
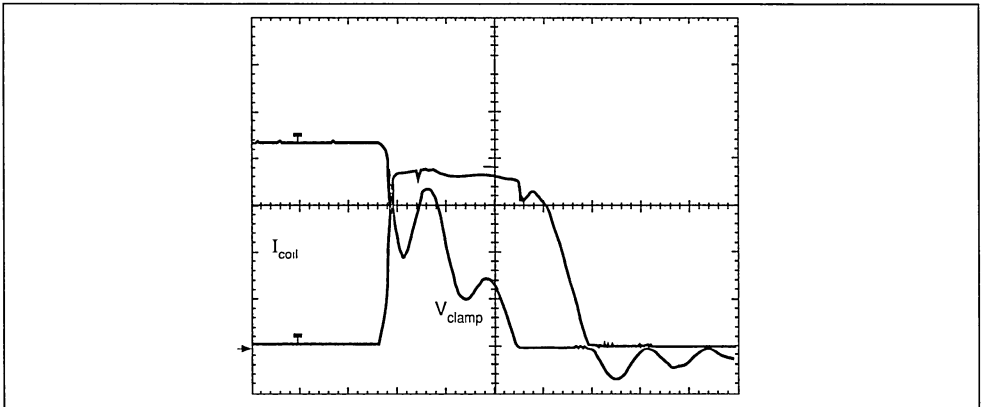


Figure 4. Primary voltage limitation



A. Current Limitation and Quasi Proportional Base Driving

Due to the low resistance of the high energy ignition coil, a current limitation system has to keep the output current within the boundaries of the Safe Operating Areas (Reverse and Forward), and limit the energy stored in the coil.

The coil current is converted to a voltage by an internal sensing resistor in series with the emitter of the Darlington. This voltage is monitored by two functional blocks: the current limiter block and the quasi-proportional base current block, which perform the functions described in the following paragraphs.

The current limiter block compares the monitored voltage to an internal reference. When the internally fixed threshold is reached, a feedback amplifier drives the power Darlington to keep the voltage across the sensing resistor (and hence also the coil current) constant, until the falling edge of the input signal starts the turn-off of the device. An active pull-down

is performed to accelerate the turn-off of the output power.

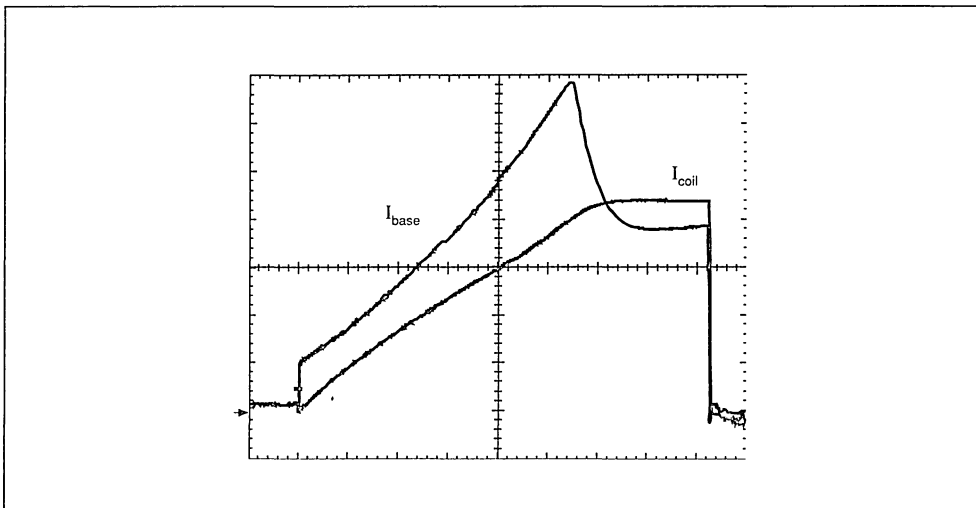
The quasi-proportional base current block generates a base current which increases proportionally to the collector current. The base driver circuit must supply a base current to the output power Darlington large enough to turn on the device with an operating supply voltage ranging from 4.5V to 5.5V. A conventional driving circuit performs this function, supplying a constant current to the device, regardless of the output current value.

The driving circuit built inside the VB027 functions in more complex manner, allowing energy saving and lower stress of the low voltage supply circuit.

Figure 5 shows how the circuit works.

The current supplied to the V_b pin, which is very close to the base current supplied to the output Darlington, increases quasi-proportionally to the output current.

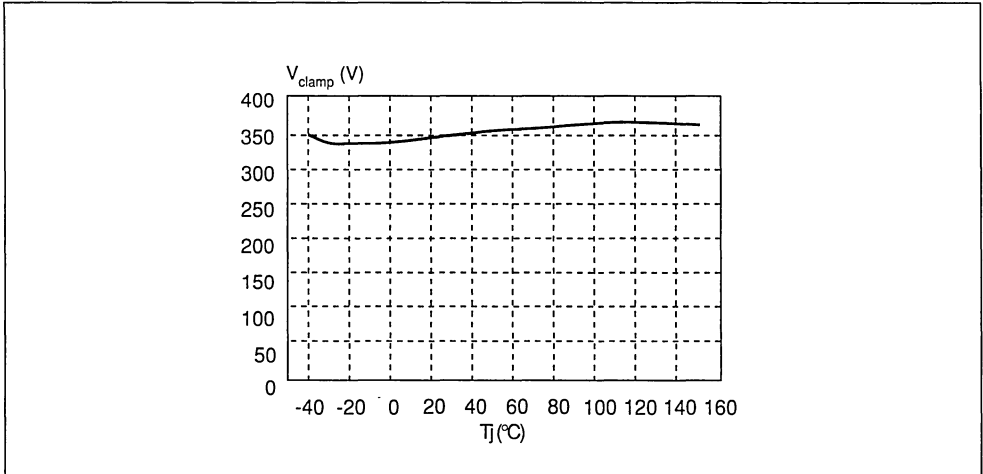
Figure 5. Base driver operation



B. High Voltage Clamp

An integrated high voltage zener is connected between the collector and the base of the output stage of the Darlington. Its typical value is 360V, and the voltage versus temperature characteristics are shown in Figure 6.

In reality this clamp is not realized with a single high voltage zener, but with a series of low voltage zeners, allowing accurate trimming of the zener voltage without any process modification.

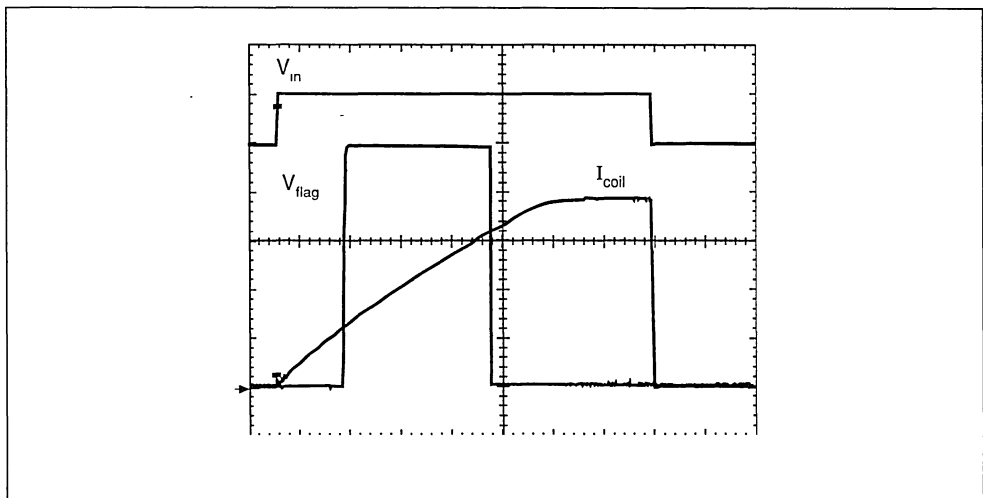
Figure 6. V_{clamp} versus temperature

C. Diagnostic Output and Over-temperature Protection

The diagnostic signal indicates the primary coil current level to the micro-controller. The diagnostic output goes high when the coil current exceeds 4.5A, and low when it exceeds 5.8A, as shown in Figure 3. This information allows the micro-controller to govern the dwell angle and to detect the coil

saturation. In addition information on the chip temperature is supplied. If the temperature of the die exceeds 150°C, the diagnostic signal goes high when the collector current exceeds 2.5A, Figure 7, allowing the micro-controller to start taking suitable action. It returns to normal working mode when the chip temperature falls to 130°C.

Figure 7. Over-temperature behaviour



D. Dynamic Bias of the P-type buried layer

At turn-on, when the current in the primary coil is close to zero, it is evident that the effect of the oscillation of the secondary current is due, mainly, to the ignition coil parasitic element. An oscillating current is added to the primary magnetizing current and it forces, during its negative phase, the collector-emitter voltage to reverse, thus directly biasing the p-buried-layer/n-epi junction. This effect could lead to excessive sinking current from V_d and to undesirable effects on the control circuit because of failure of the insulation. A patent pending circuit has been designed to perform a dynamic bias of the p-type buried layer, whose voltage is forced to follow

the collector voltage when it becomes negative. Figure 8 shows the operation of this circuit.

E. Power Darlington

In the horizontal layout, shown in Figure 9, the power Darlington is, in some respects, very similar to a standard discrete transistor. The main differences are in a novel, patent pending, vertical structure, the cross section of which is shown in Figure 10. The deep-base structure and the original layout of the emitter and base ballast resistors have allowed a considerable increase in the current density and in the Safe Operating Areas of the device. The device has an energy handling capability of up to 1 Joule.

Figure 8. Dynamic bias of p-type buried layer

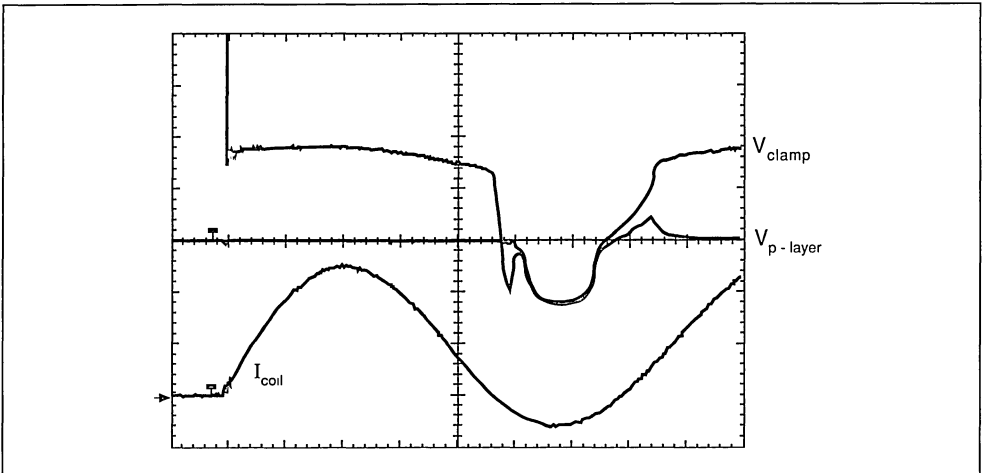


Figure 9. Standard package (TO-220 - 5 leads) and top view of the device

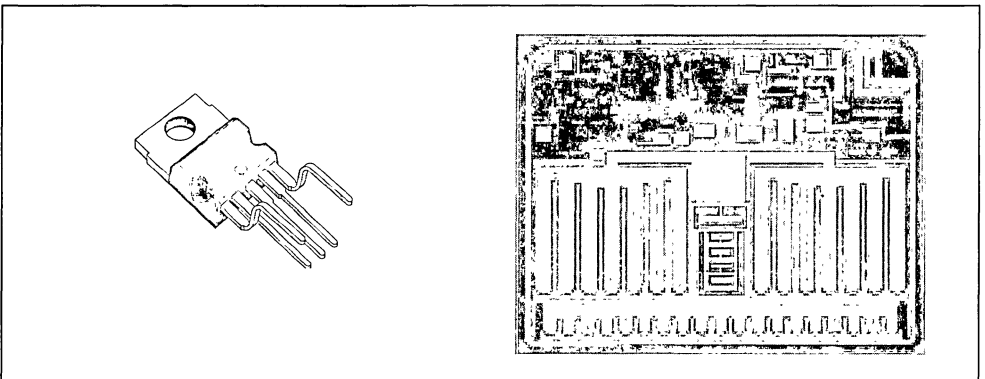
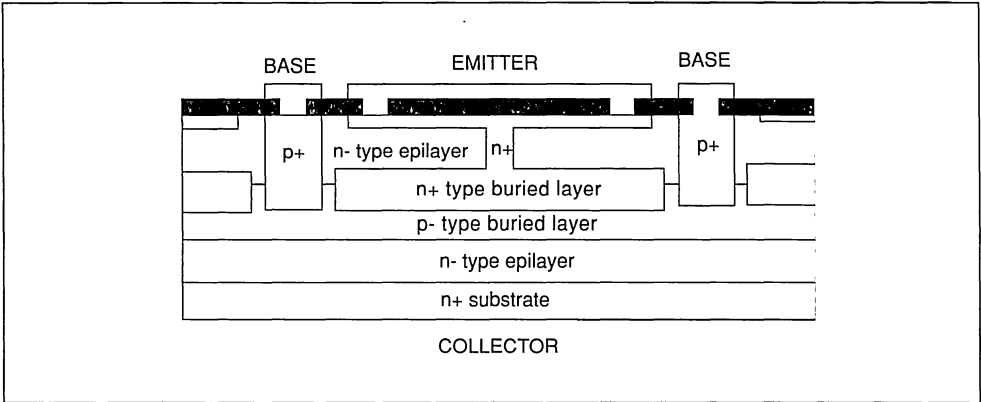


Figure 10. VIPower M1 technology overview - power cross section



CONCLUSION

The VB027 is the latest and the most representative element of a new family of automotive devices developed in VIPower™ M1 technology. The main characteristics of the device can be summarized as follows: the coil current is internally limited, built-in collector-emitter voltage clamping is present, the input is TTL/CMOS compatible, and a diagnostic output to the micro-processor for the dwell angle control and overtemperature protection is available. Moreover the die-size is compatible with the TO-220 package. These features, which are unique in a single device, make the VB027 one of the most aggressive competitors in microprocessor based EMS.

Presented at
International Symposium on Power Semiconductor Devices
Monterrey, CA., USA May 1993

LIGHTING APPLICATIONS

ELECTRONIC FLUORESCENT LAMP BALLAST

1. INTRODUCTION

Fluorescent lamps have applications in most areas of lighting, where they give longer lifetime and lower power consumption for equivalent light output compared to filament bulbs, with the disadvantage of higher initial cost. In operation, a voltage is applied across the ends of a sealed glass tube containing mercury vapour, causing the vapour to be ionised. This ionised vapour radiates light in the ultra violet part of the spectrum, which is converted to visible light by a fluorescent coating on the inside of the tube.

1.1 Driving a fluorescent tube

When the lamp is first turned on, the mains voltage across it is not sufficient to cause the initial ionisation of the vapour. A starting element is thus needed to provide a high voltage pulse across the tube to start the process.

Once the gas in the tube is ionised however, its impedance becomes negative; that is to say the more current that flows through the lamp, the more conductive it becomes (this is because the increased current increases the degree of ionisation of the gas). Therefore, some form of limiter must be added to prevent the current increasing to a level where the lamp is destroyed. The current limiter is usually known as a ballast.

2. CONVENTIONAL LAMP BALLAST

The simplest form of ballast is an inductor. Figure 1 shows a driving circuit for a fluorescent lamp operated from the 220/240V mains.

2.1 The starter

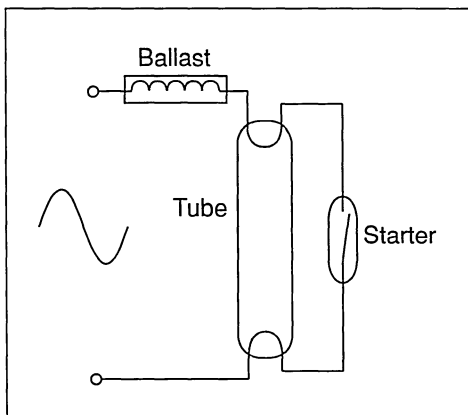
The starter triggers the tube when it is first turned on. It consists of two contact strips, one normal and one bimetallic, which are normally open, enclosed in a glass envelope filled with inert gas. When mains is applied to the circuit, the voltage is not sufficient to cause spontaneous ionisation of the gas in the main tube, and the lamp remains in a high impedance state (i.e. not turned on). However, the electric field which the mains creates in the small gap between

by A. Vitanza, R. Scollo, A. Hayes

the contacts in the starter is sufficient to ionise the gas there. This allows a current to flow in the metal strips and through the gas (and also through the filaments of the main tube, which heats them and facilitates the subsequent ionisation). The heat generated by the current flow through the gas causes the bimetallic strip to bend towards the other. When the contacts finally touch, two things occur: firstly the gas in the starter de-ionises, and so the bimetallic strip begins to cool. Secondly, as the impedance of the circuit falls, the current through the ballast inductor and the filaments of the main tube increases.

A few tenths of a second later, the bimetallic strip has cooled sufficiently to bend back slightly, reopening the gap. The sudden increase in impedance and consequent sharp reduction in inductor current causes a large overvoltage across the inductor. Given the correct conditions (see section 2.2 below for a discussion of these) this overvoltage is large enough to cause ionisation of the gas in the main tube. At this point the impedance of the fluorescent tube falls to a minimum, and the voltage drop across it falls to a level below that required to ionise the gas in the starter contact gap. The contacts thus remain open until the lamp is next turned on.

Figure 1. Simple conventional lamp ballast



2.2 “False starts”

Since there is no synchronisation with the (sinusoidal) mains input, the starter operates at a random time on the current waveform, the contacts opening at an inductor current level anywhere between zero and the maximum. This means the overvoltage generated may not be large enough to cause sustained ionisation of the gas in the tube. If this is the case, the process repeats itself until full ionisation occurs, causing the “flashing” commonly seen at the start up of conventional fluorescent ballasts.

2.3 Problems with conventional ballasts

There are also physical problems with this type of lighting. When the current in the tube falls to zero in each 50/60Hz cycle, the gas in the tube de-ionises and stops emitting light, resulting in a 50/60Hz flicker. This can cause disturbing “stroboscopic” optical effects with moving machinery and VDUs. In industrial plants, fluorescent tubes are used in pairs in a single light spreader, each lamp being fed from different phases, either real or virtual via a capacitor. This helps to eliminate flickering observed by the human eye.

3. ELECTRONIC ALTERNATIVES

Electronic ballasts replace the starting and inductive elements of the conventional system. The aim of using an electronic ballast is to increase the operating frequency of the system above the 50 or 60Hz determined by the mains - typically to a few tens of kHz. This has a two main effects:

- a) The gas in the tube does not have time to de-ionise between current cycles, which leads to lower power consumption (typically about 70% of that with conventional ballast), longer tube life and almost no flicker.
- b) The inductor required to generate a large enough overvoltage to ionise the tube is smaller, and so generates less resistive losses, and the weight of the system is reduced.

However, the electronic solution is more complex and has a higher initial cost - although this will eventually be paid back by the savings in energy.

It should be clear from the section 2 that the electronic replacement for the conventional ballast should perform two main functions: first to provide the start-up ionisation energy, and secondly to provide a constant RMS supply to the tube in normal operation.

The most commonly used electronic drive circuits for fluorescent lamps are voltage fed half-bridge

quasi-resonant circuits (figure 2), current fed half-bridge resonant circuits (figure 5), and push-pull resonant circuits (figure 8).

3.1 Voltage fed quasi-resonant circuit.

The simplicity and low cost of this topology means that this configuration is the only option for Compact Fluorescent Lamp (CFL) ballasts (those used as direct replacements for incandescent bulbs) in the 7W to 32W range. It is also used in large (industrial) ballasts driving two or more full-sized tubes, but requires additional protection circuits in this case.

3.1.1 Starting the oscillation

Resistor R1, capacitor C2 and diac D2 form the first base current pulse for TR2 to start the oscillation. After start-up, this generator is made inoperative by diode D1 (this diode prevents the voltage across the diac from becoming high enough to bias the device on), and the circuit is maintained in oscillation by feedback to the gates of the transistors from the output circuit via the transformer T1.

The tube is fed by generating an overvoltage across capacitor C4, by means of the series resonant circuit consisting of the serial combination of the inductor L and capacitors C3 and C4. Before the tube is started, as C4 is much smaller than C3, C4 dominates the resonant frequency of this circuit. Depending on the value at which the tube lights, the overvoltage generated across C4 at this frequency is between around 600V and 1.2kV.

3.1.2 Steady-state operation

Once the tube ionised, as there is effectively a short circuit across C4, the operating frequency is defined by C3 only, and so is lower. At this frequency the overvoltage generated is also lower - just sufficient to keep the tube lit.

In normal operation, when the transistor is first turned on, the current through transformer T1 increases until its core saturates. At this point the feedback to the base of the transistor is removed, and after the storage time of the transistors has passed, it turns off. In this way, apart from the value of C3, the operating frequency of the circuit is also defined by the size and maximum flux density of the core of T1, and the storage times of the transistors. This frequency is generally designed to be slightly higher than the natural resonance frequency of the circuit.

As the circuit is operating at slightly higher than its resonant frequency, the combined reactance of C3

Figure 2. Voltage fed half-bridge quasi-resonant lamp ballast (startup circuit shown shaded grey)

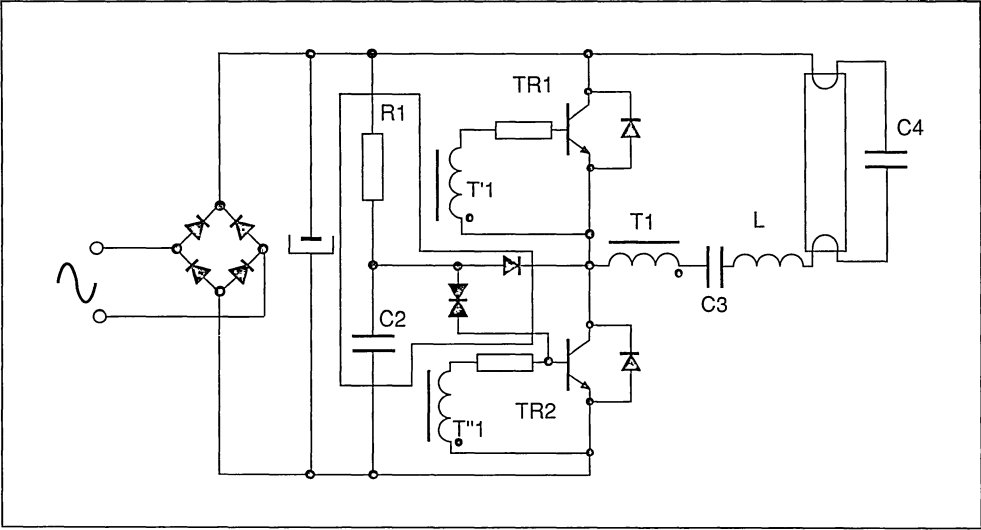
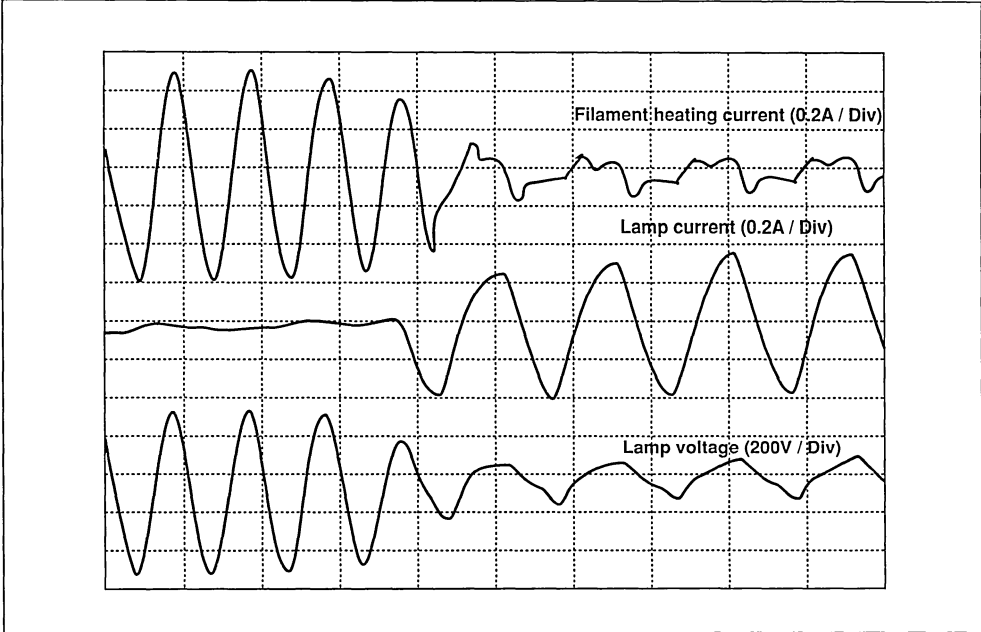


Figure 3. Start-up of the voltage fed ballast



and L is not zero - hence the V_{CE} voltage of the transistors is shared between the tube and the capacitor/inductor combination.

At start-up, the voltage across capacitor C4 causes more or less instantaneous ionisation of the fluorescent tube - there are no "false starts" as there

are with conventional ballasts. Figure 3 shows the voltage and current in the lamp at start-up. The peak collector current at start-up is around 3 - 5 times the normal operating current, and so it is necessary to select transistors with ratings to withstand this: in the resonant condition the current in the network is limited only by the DC resistance.

Waveforms for the circuit in the steady state are shown in figure 4.

3.1.3 Slow-starting or damaged lamps

Although the circuit can withstand being turned on with no lamp connected (as it will not resonate), a great deal of stress is placed upon it if for some reason the lamp will not start correctly (for example if the gas has leaked out), or if the lamp is too slow to start. This is because the transistors can only stand the high levels of current at start-up for a short period of time, before they overheat and are destroyed.

This problem does not exist for the other topologies, as even in the start-up phase the level of current is not excessive.

3.2 Current fed resonant circuits

3.2.1 Starting the oscillation

The start-up circuit operates in the same way as in

the voltage fed topology. The high voltage to strike the tube comes from the action of the output transformer - before the lamp is struck, the transformer sees an open load, and so the voltage it generates is higher than in normal operation.

Note that the circuit shown has no filament pre-heating - however it would be possible to add circuits such as those described later for the push-pull topology. The lack of pre-heating means that in this case the tubes will strike at a higher voltage.

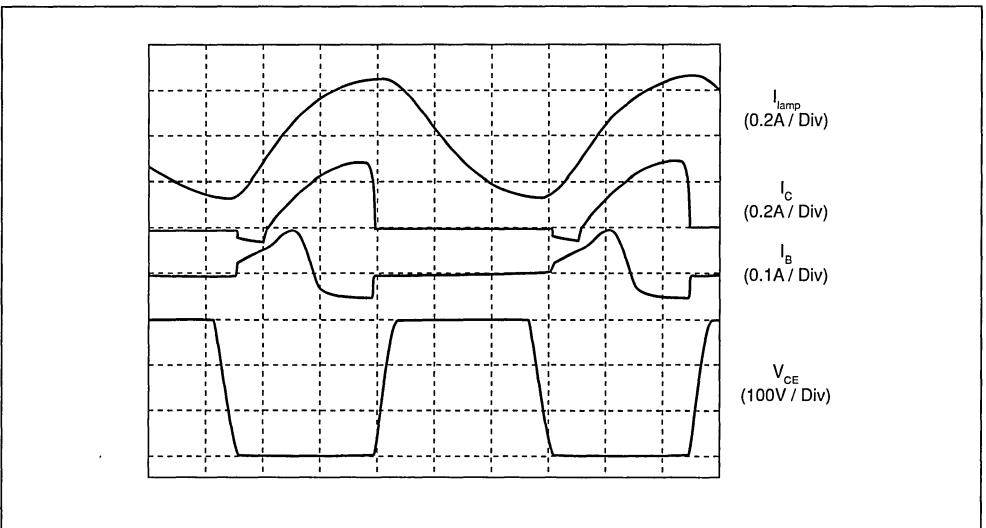
3.2.2 Steady-state operation

Once the lamps are struck the voltage generated by the output transformer falls, as it sees them as a resistive load.

The circuit oscillates due to the resonance of C_3 , C_R and the inductance of T1. The primary and secondary of T2 are coupled such that one transistor connects the positive part of the wave, and the other the negative. Base drive for the transistors is provided by feedback windings of the output transformer.

Waveforms for the circuit in the steady-state are shown in figure 6, while figure 7 shows the worst-case conditions which the transistors must be designed to withstand; start-up with a supply voltage

Figure 4. Steady state waveforms of the voltage source ballast



20V above the nominal value of 120V RMS and no lamp connected in a), and "arcing" testing of the ballast during installation in b). Figure 7a shows that the V_{CE} of the transistor can reach around 600V,

while figure 7b shows that a device with a large safe operating area is required, as large voltages and currents exist simultaneously.

Figure 5. Current fed half bridge resonant lamp ballast (start-up circuit shown shaded grey)

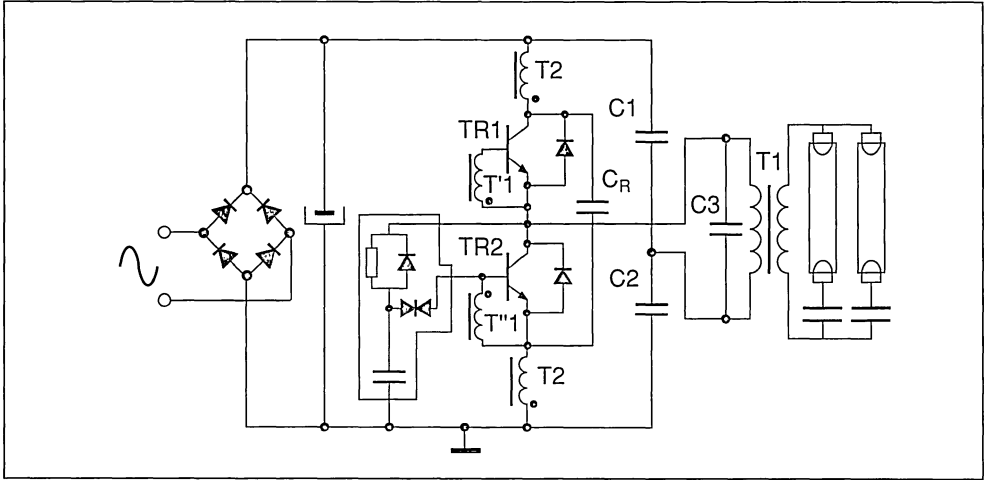


Figure 6. Steady state waveforms of the current fed ballast

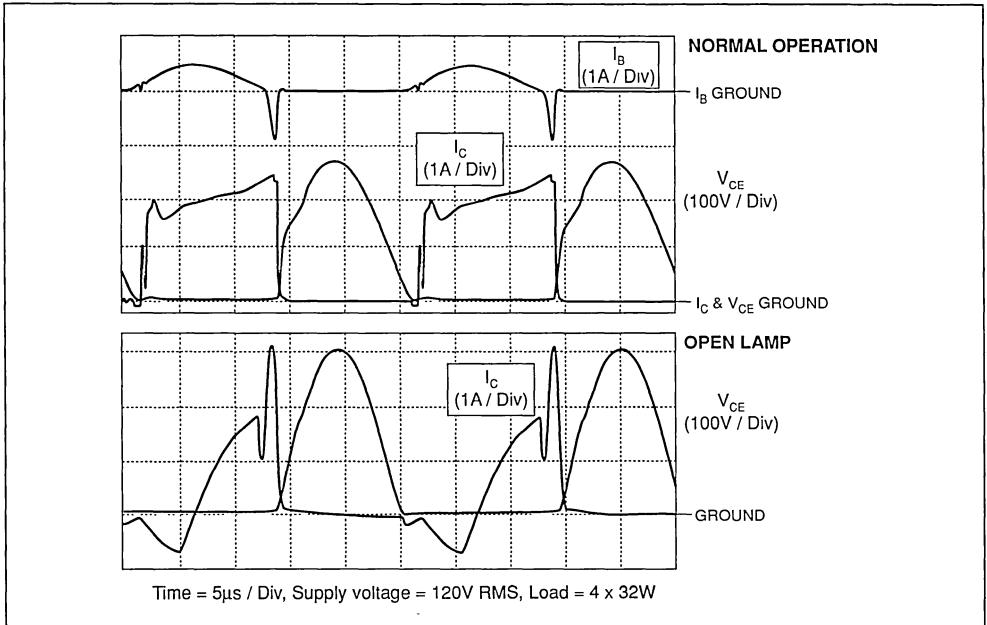
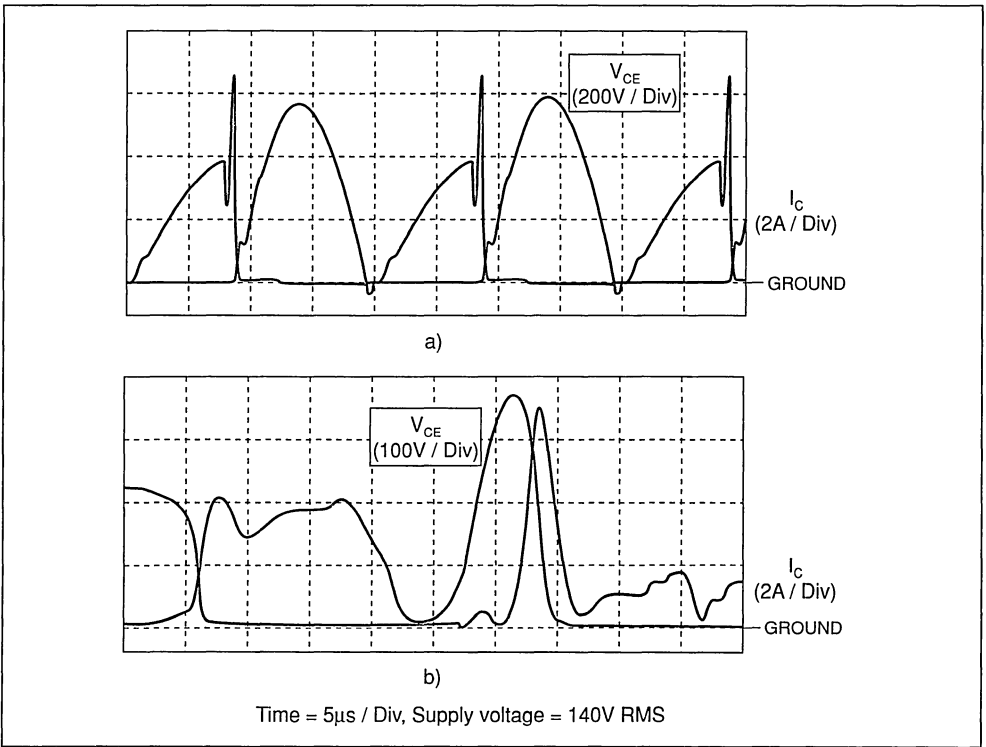


Figure 7. Worst-case operating conditions for the current-fed ballast circuit:

- a) Start-up with open load
- b) Transient which may occur during "arcing test"



3.3 Push-pull resonant circuits.

This topology has a main advantage in that it can tolerate open or short circuited loads indefinitely. It is generally used in large ballasts. It generates an almost perfectly sinusoidal voltage through the lamp, each transistor producing half of the sin wave.

3.3.1 Starting the oscillation

The circuit oscillates due to the capacitor C1, and the inductance of the transformer. The inductor L acts as a constant current source, maintaining the resonant circuit in oscillation by feeding energy into it to compensate for that absorbed by the load.

The oscillation is triggered by the high-value resistor R1, which pulls up the base-emitter voltage of the transistors. Once the oscillation has started, and before the lamp is ionised, the windings S1 and S2 generate a current to heat the lamp filaments, while

S3 generates the high voltage required to ionise the lamp (the voltage it generates is high as it is effectively connected across an open load).

3.3.2 Steady-state operation

Once the lamp is ionised, S2 provides the drive for the lamp. As the impedance of the lamp has fallen, the voltage across S2 is much smaller in this situation than in start-up. The voltage across S1 and S3, and consequently the filament currents, also reduce.

Base drive for the transistors is provided by means of feedback windings from the output transformer.

Waveforms for the circuit in the steady-state are shown in figure 9. The collector-current spikes at each switching event are caused by both transistors conducting simultaneously - one in the forward direction, and the other in the reverse, through the collector-base diode.

Figure 8. Push-pull resonant ballast

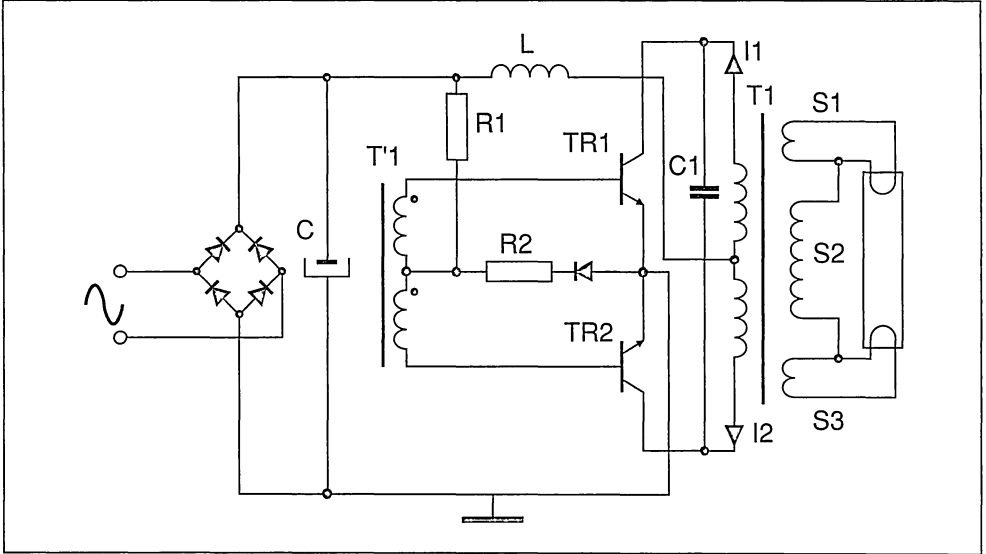
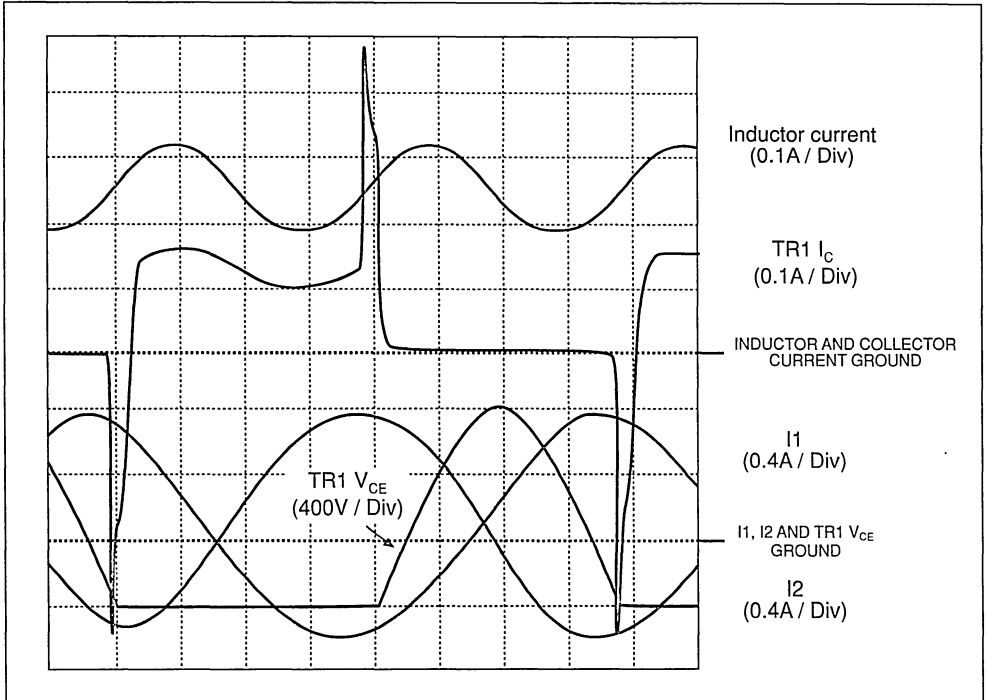


Figure 9. Steady state waveforms of the push-pull ballast



3.4 Problems with electronic ballasts

3.4.1 Dimming

The most common technique used in dimming in general is phase control (feeding only a part of the supply sinewave to the lamp). However, this will lead to problems of flicker in electronic lamp ballasts.

The lamp could feasibly be dimmed by controlling the oscillation frequency of the circuit (and hence the voltage drop on the inductor), although there are problems with this. The basic circuit oscillates at a frequency affected by a large number of factors, not at a fixed, known frequency determined by the designer. If the frequency is to be controlled, the circuit must be designed to operate within certain limits to avoid inefficient operation and possible malfunction of the devices. This means a much greater design effort and a much more complex and costly circuit. For this reason dimming circuits are not often included in electronic ballasts.

3.4.2 Power factor and EMI reduction

Because it operates at a higher frequency than the mains, an electronic ballast will transmit EMI back to the supply. Also, most ballasts draw a non-sinewave current from the mains - that is they do not have a unity power factor - unlike an incandescent bulb. To satisfy the requirements of the power supply companies requires the addition of some form of power factor correction (PFC). For a low power application, a simple passive filter will be sufficient, but high power ballasts will require an active power factor corrector circuit.

4. SELECTION OF TRANSISTORS

4.1 Choosing between MOSFETs and Bipolars

In many cases, there can be very little to choose between a Power MOSFET and a Power Bipolar in an application. In general terms, the Power Bipolar is fractionally cheaper, and is currently the most popular choice for this reason. However, the Power MOSFET does not have the problems associated with variations in storage time (see section 4.5 below) and so no special selections have to be carried out. The performance is also more predictable and varies less between circuits, particularly the frequency of oscillation - this can be extremely important in applications requiring power factor correction and the limiting of EMI interference, as the frequency emissions of the circuit will be much more predictable and testable.

4.2 Selecting the blocking voltage of the transistors

4.2.1 Voltage-fed topology

The peak voltage across the transistors is equal to the peak mains voltage, plus a 15% allowance for mains voltage variation, plus a 10% safety margin.

For example, for the 220V RMS mains:

$$\begin{aligned} \text{Peak voltage} &= (220\text{V} \times \sqrt{2}) + 15\% + 10\% \\ &= 394\text{V} \end{aligned}$$

It would seem that devices with a BV_{CES} of 400V could be used - however this would mean that the devices would have a BV_{CEO} less than the voltage applied by the mains, which is not advisable. Hence the transistors should have a BV_{CEO} rating of 400V minimum.

The same type of calculation can be used for other supply voltages:

Supply voltage	120V	220V	277V
BV_{CEO}	300V	400V	4~500V

4.2.2 Current-fed topology

As can be seen in the waveforms in figure 7, the peak voltage experienced by a transistor in a 120V system in worst-case operation is around 600V. The presence of transients due to the inductances and capacitances of the circuit means that in practice and additional safety margin is added, and devices of around 800V are used.

Supply voltage	120V	220V	277V
BV_{CES}	7~900V	900~1kV	1.2~1.3kV

4.2.3 Push-pull topology

The peak voltage across the transistors in the steady state is equal to twice the peak mains voltage, due to reflection from the transformer:

$$V_{\text{peak}} = 2 \times \sqrt{2} \times V_{\text{mains}}$$

For the 220V mains, this gives a value of around 620V. In practice a safety margin is added to protect the device from transients at turn-on and turn-off, leading to the use of devices rated at around 1400.

Supply voltage	120V	220V	277V
BV_{CES}	800~1kV	1.3~1.5kV	1.6kV

4.3 Current ratings

The calculation of the current rating of the transistors used varies considerably depending on the topology, power rating etc. Table1 shows approximate values.

Table1. Approximate working collector current values for lamp ballast topologies

Topology	Power	120V	220V	277V
Voltage fed (CFL)	17~32W	0.4~0.8A	0.3~0.6A	-
Voltage fed (Industrial)	36~132W	1~4A	0.5~2A	0.5~2A
Current fed	36~132W	1~2.5A	0.5~1.5A	0.5~1.5A
Push-Pull	36~132W	1~2A	0.6~1.2A	0.5~1A

4.4 Storage times

When Bipolar transistors are used, the operating frequency of the generator is heavily dependent on the storage time of the transistors. This parameter can affect the operation of the circuit in two main ways:

- If the storage time of the transistors is high, the oscillation frequency of the circuit will fall, causing the voltage across the lamp to increase, in turn possibly damaging them. This effect is most important in the voltage-fed topology (see section 3.1.2).
- If the storage times of the pair of transistors are too dissimilar, one transistor will generate more switching losses, causing it to heat up more, and possibly causing the device to go into thermal runaway.

The SGS-THOMSON BULxxx series of power bipolar transistors produced for electronic lamp ballast applications is characterised specifically by storage times to meet this criterion.

4.5 D.C. gain (h_{FE})

In all topologies, this must be sufficiently high at the start-up levels of current levels (around five times the nominal) to ensure that the circuit starts correctly at all temperatures. Additionally, the transistors in a push-pull topology must also have a sufficiently high gain at very low current levels to start up the ballast, as this topology relies on startup by "noise" (rather than the forced startup by diac as used in the other topologies).

5. CONCLUSIONS

Electronic ballast can be used to replace both the starting element and the conventional ballast of fluorescent lamps.

Although they are more complex and costly than their electromagnetic counterparts, they offer increased light output efficiency, reduced weight, and a removal of the problems of flicker. All this is achieved by increasing the frequency at which the tube is driven above the 50Hz defined by the mains frequency. The higher initial cost of the system will eventually be compensated for by the reduction in energy consumed.

SOFT LIGHT DIMMER

by J. M. Charreton

1. INTRODUCTION

The circuit described in this paper is a new proposal for dimming incandescent lamps which offer a resistive load, and halogen lamps with their electronic converter which are, in effect, capacitive loads.

Power, in conventional dimming circuits, is controlled by TRIACs. They require a series inductor for RFI filtering and a fuse to protect them against overload and short circuit conditions. Additionally, the fuse may require maintenance. The circuit is potentially noisy due to the AC current flowing through the inductor.

In this new circuit design, power is controlled by means of an IGBT. The IGBT switching behaviour can be slowed down at turn-on and turn-off, hence a series inductance need not be used. An additional feature is that the circuit can be designed to provide short circuit protection which eliminates the need for a fuse and the necessary access for fuse replacement. There is virtually no acoustic noise.

2. MAIN FEATURES

The power supplied to the load can be adjusted between 0 and 90%. Control is achieved by varying the conduction time of the IGBT. Because the IGBT is controlled at turn-off, overload and short circuit protection can be implemented - a feature that removes the need to incorporate a fuse.

Slowing down the rate at which the current falls at turn-off reduces the amount of R.F.I. generated and avoids the use of a series choke. It also reduces any tendency for audible noise generation.

IGBTs, unlike TRIACs, do not have a threshold current limit. This means that no flicker is observed as is the case when using TRIACs.

This dimmer can work at any mains voltage by adapting the power switch to the load.

In order to use the full half sine wave of the rectified mains voltage, the time constant can be adjusted from, for example, 0ms to 9 ms (approximately half of the full wave period) in the case of a 50Hz mains system.

The circuit complies with the IEC5555¹ norm when controlling a load up to a limit of 1kW.

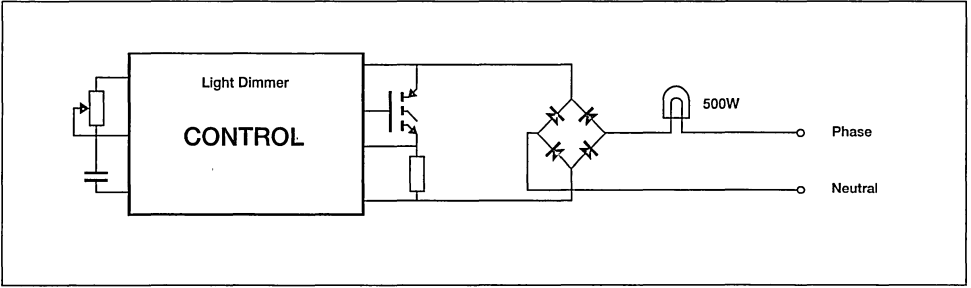
3. PROPOSED SOLUTION

3.1 Circuit description

The light dimmer uses an isolated gate power

switch such as a MOSFET or an IGBT. A controlled AC switch is made by using the power switch to control a diode bridge, figure 1.

Figure 1:



A standard timer, a TS555 controls conduction in the power switch. This controls the light intensity. The timer is triggered on the zero voltage crossing of the rectified mains voltage.

Short circuit protection eliminates the need for a fuse which would otherwise be a heat source in the circuit.

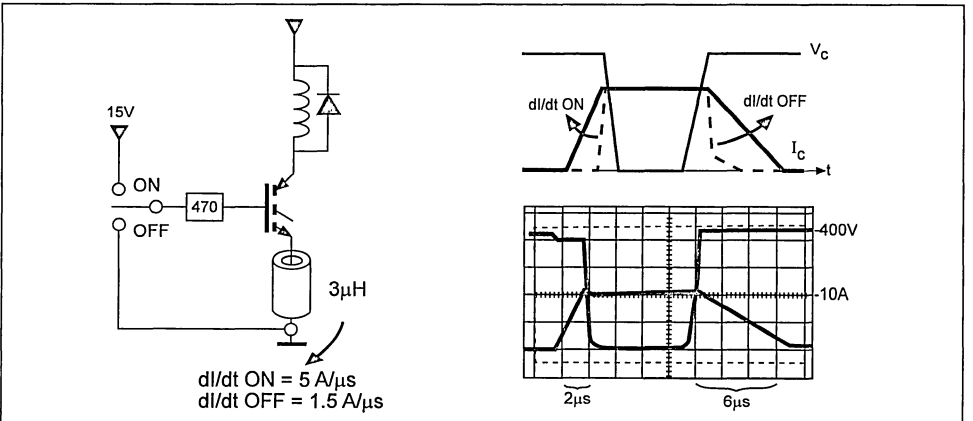
Short circuit protection.

Should a short circuit occur, the over-current is sensed across the shunt resistor. As soon as the shunt voltage reaches a predetermined level, the power switch is turned off and the timer is reset for a long enough period to avoid spurious restart.

Control of di/dt and dV/dt.

di/dt can be slowed down both at turn-on and turn-off by placing a small inductor in the emitter lead of the IGBT. The current variations are controlled by the IGBT itself. During di/dt the voltage across the inductor ($e=L di/dt$) must be equal to the gate-source voltage minus the Miller effect voltage, figure 2.

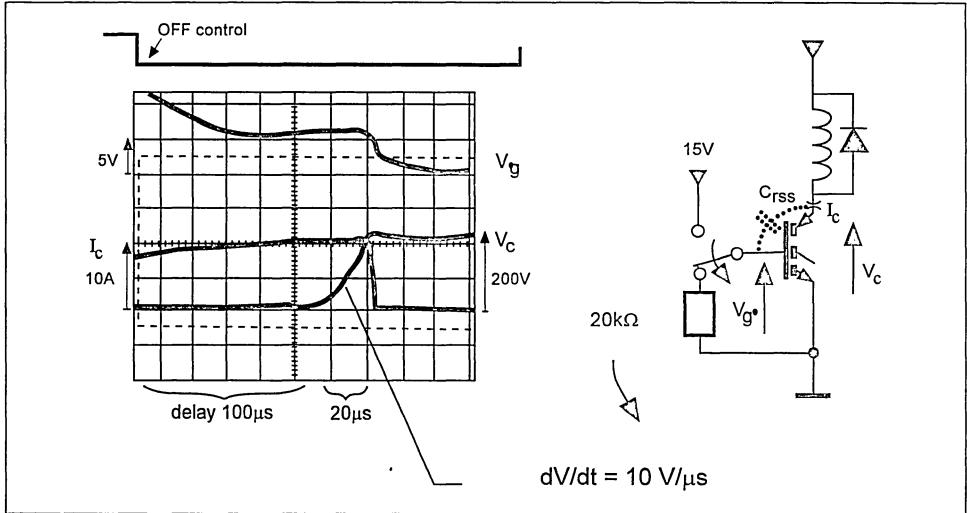
Figure 2: di/dt control



dV/dt can be drastically slowed down at turn-off by using a very high value of gate resistor (R_{goff}) to turn off the IGBT. The typical dV/dt can be reduced by a factor of 1000 compared to normal switching. Reducing dV/dt results in the losses being

low when switching at a frequency of 100Hz. During dV/dt the IGBT is desaturated. The current through the Miller capacitor ($i=C dV/dt$) flows through the gate resistor generating a voltage equal to the gate threshold voltage, figure 3.

Figure 3: dV/dt control



The advantages of controlling dV/dt and dI/dt are that EMI is reduced and hence the cost of filters is reduced. Eliminating the series inductor also saves valuable space on the printed circuit board and eliminates the magnetic constriction noise.

3.2 Power Switch: Selection and Performance

Basically, both power MOSFETs and IGBTs are both well suited for use in this application. Evaluations of the performance of this light dimmer have been made using both types of power switch. The results are given in Table 1.

Evaluation of the losses showed:

- turning on at zero crossing voltage eliminates turn-on losses

- the conduction losses are dependent on the type of power switch and the conduction time,
- by slowing down the turn-off switching, the losses at this point in the switching cycle are the same for both types of power switch and are at a maximum at 50% conduction time.

Conditions:

- for this evaluation, power switches with the same die size were used.
- the Power MOSFET STP5N50 has an $R_{DS(on)} = 1.5\Omega$ at 25°C and the IGBT STGP10N50A has $V_{CE(on)} = 1.8\text{V}$ at $I_c = 10\text{A}$ and $T_c = 100^\circ\text{C}$.

The results in Table 1 are for a load of 300W.

TABLE 1: Power switch comparison, MOSFET vs. IGBT, using a 300W load.

CONDUCTION MODE	MOSFET		IGBT	
	Conduction losses	Switching losses	Conduction losses	Switching losses
HALF-WAVE	3.2W	1.2W	1.2W	1.2W
FULL-WAVE	4W	-	1.8W	-

As the losses in the IGBT were lower than those in the power MOSFET, the IGBT was chosen as the power switch for this application.

Further evaluation of the IGBT as a power switch, using an increased load of 500W, gave the results shown in Table 2. The data was obtained using a heat sink rated at 17°C/W and at an ambient temperature of 23°C.

TABLE 2: Working temperature of sources of heat in the light dimming circuit.

	Half-wave conduction $t_{on} = 5ms$	Full-wave conduction $t_{on} = 8.5ms$
Power switch heatsink	61°C	61°C
Sense resistor	58°C	70°C
Rectifier diode	60°C	80°C

TABLE 3: Heat losses in the power switch, sense resistor and rectifier diode.

Source of power losses	Half-wave conduction $t_{on} = 5ms$	Full-wave conduction $t_{on} = 8.5ms$
Power switch	2.7W	3.1W
Sense resistor	0.3W	0.5W
Rectifier diode	2.3W	4.1W

4. PRACTICAL REALIZATION

The heart of the circuit is the TS555 timer and the IGBT STGP10N50A. The complete schematic is shown in figure 4.

The timer is triggered on the zero crossing voltage pulse. The conduction angle is dependent on the time constant determined by C5/R14+R15.

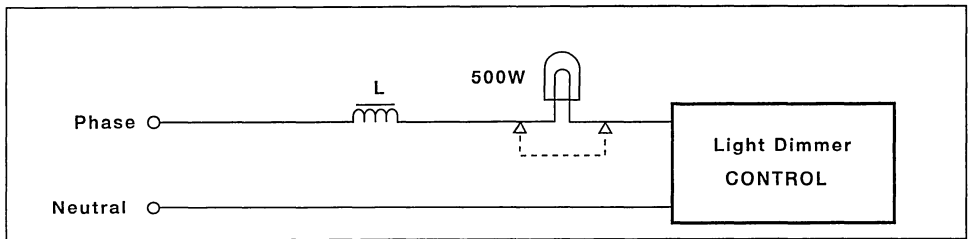
In order to guarantee that a correct voltage level is applied to the gate of the IGBT, the under-voltage control, T2 - T3, inhibits the power switch until the auxiliary supply voltage reaches 8V.

Over-current and short circuit protection

are based on the current sense resistor, R5. When the voltage across R5 reaches the gate trigger voltage of the sensitive gate thyristor ,T4, the gate of the IGBT is taken low and it turns off. At the same time the timer is reset. This current limiting also provides automatic soft-start and hence protection against excessive in-rush current.

Figure 5 shows the equivalent circuit of a load which includes an equivalent line inductance. When an overload or short circuit occurs, the power switch is turned off. At this time the energy stored in the inductance is dissipated in the IGBT through the transil diode D4, making the IGBT operate as a power zener clamping

Figure 5: Equivalent Schema with Line Inductance



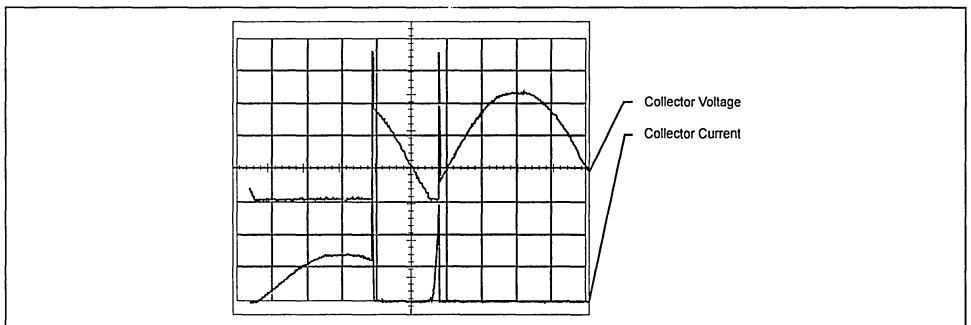
diode. The IGBT must be sized to sustain the energy stored in the inductance during this period (see figure 6).

If the short circuit is still present at the next mains crossing, the IGBT is turned on until the current protection is reached. This means that, in permanent short circuit

conditions, a series of current pulses are produced. Therefore the IGBT should be sized to sustain the resulting energy.

Figure 6 illustrates the collector voltage and current when an accidental short circuit occurs and is followed by a permanent short circuit.

Figure 6: Short Circuit Behaviour



At the time of the short circuit, the power switch must sustain the energy stored in the line inductance. Switching off the current generates an over-voltage. The IGBT is protected from the over-voltage by a transistor placed between the drain and the gate.

A summary of the switching losses for normal operation, accidental short circuit and for a permanent short circuit are given in Table IV.

The TS555 timer is reset for a period of about 5ms to prevent parasitic turn-on of the power switch due to the voltage oscillations that can occur after current limiting.

The auxiliary power supply is provided during the off state of the power switch. This means there is a conduction time

Table 4: Stress on the switch for a load containing a series inductor.

Parasitic Line Inductance	Maximum switching losses 500W(100Hz)	Energy for short circuit during conduction	Losses (100Hz)for Turn-on Short Circuit
80µH	0.9W	9mJ	6mW
1.5mH	1.6W	0.2J	2.9W

ranging from 0% to 90%. Hence the power supplied to the load varies between 0% and 90%.

5. CONCLUSION

di/dt control of an IGBT in a light dimming application reduces the amount of R.F.I. generated and avoids the use of a series inductor for this purpose as is used in the case of a more conventional dimmer.

Removing the inductor makes the circuit noiseless and saves printed circuit board space.

If over-current protection is provided, no conventional fuse is necessary while the self protection of the circuit is enhanced with short circuit protection and control over the in-rush current.

¹Norm concerning disturbances in supply systems caused by household appliances and similar electrical equipment.

ELECTRONIC TRANSFORMER FOR A 12V HALOGEN LAMP

by P. Fichera, R. Scollo

1. INTRODUCTION

Lighting that uses halogen lamps is commonly found in residential environments, where it offers a warm light in comparison with that generated by fluorescent tubes, and greater efficiency than conventional filament bulbs.

These lamps are available with voltage ratings of 6, 12 or 24 Volts, and so a transformer is needed in order to provide the lamp with a low voltage supply from either 110V a.c. or 220V a.c. mains. They are generally available with power ratings of 50, 75, 100 and 250 Watts.

The "electronic" transformer represents an alternative means of power conversion to the more standard iron core, 50Hz transformer technique.

The advantages of the electronic transformer compared with the classical solution are:

- The output power from the electronic transformer to the lamp can be varied, thus dimming control can be added;

- It is possible to include protection against short circuit of the lamp filament;
- Weight can be reduced and the construction made more compact; and
- Acoustic noise (mains hum) is eliminated.

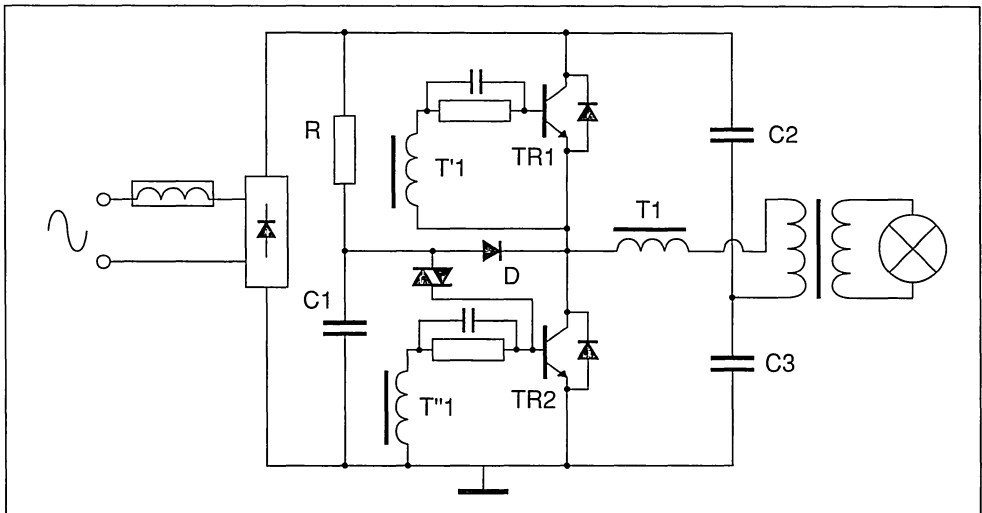
2. THE ELECTRONIC SOLUTION

The topology of the circuit is the classic half-bridge. The control circuit could be realised using an IC (so fixing the operating frequency), but there is a more economical solution which consists of a self-oscillating circuit where the two transistors are driven in opposing phase by feedback from the output circuit.

3. CIRCUIT DESCRIPTION

The line voltage is rectified by the full-bridge rectifier, generating a semi-sinusoidal voltage at double the line frequency. The diac starts to conduct during each cycle, starting the half-bridge oscillation. The turn-on of the diac can be varied by modifying the time constant of the RC network formed by R and

Figure 1. Electronic transformer for 12V Halogen Lamp



C1. This can be varied to provide a lamp dimming feature.

Once the cycle has started, the diode D maintains the voltage across C1 at a value less than the diac conduction threshold voltage, so the transistor can switch off.

The frequency of oscillation depends mainly upon the size and maximum flux density of the core used in the feedback transformer, and the storage time of the transistors. When the cycle has started, the current in the feedback transformer increases until the core saturates. At this point the feedback drive of the active transistors is therefore removed, and, once its storage time has passed, it turns off. In this application the oscillation frequency would be around 35kHz, generally around ten times the natural frequency of the circuit.

The dependence upon the storage time is minimised by the RC network at the base of the transistor, which increases the rate of charge extraction from the base at turn-off. The network also serves to decouple the base from the oscillation caused by the base transformer at turn-off, preventing spurious turn-on of the device.

The anti-parallel diodes allow current to flow when devices are off.

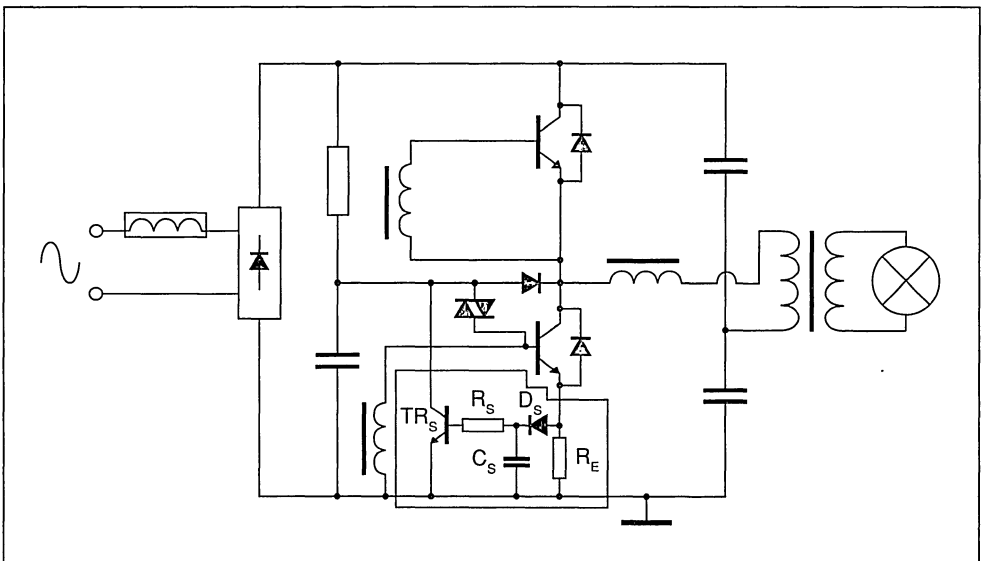
3.1 Short Circuit Protection

Figure 2 shows a circuit with circuitry to protect against a short circuit of the load added (note - some components have been removed for clarity). The circuit operates as follows.

A short circuit of the lamp will cause an excessive current to flow through the transistors, which will eventually cause them to overheat and be destroyed. However, this current will also cause the voltage across R_E to increase. This causes transistor TR_S to turn on, which in turn prevents the diac from triggering the circuit at the start of each cycle. R_S and C_S serve to delay the turn-on of the transistor, preventing the protection being triggered during the inrush phase at the turn on of the lamp (when the lamp filament is cold, it has a very low resistance, causing a large but brief current to flow through the transistors at turn-on. This resistance increases when the lamp heats up, and the current through the transistors falls to its steady-state value). Diode D_S prevents the small-value resistor R_E disrupting the operation of the filter.

After a short time (a few operating cycles), the capacitor C_S will become discharged and so will be unable to keep TR_S turned on, and the circuit will attempt to restart itself. If the fault condition still

Figure 2. Transformer with short-circuit protection added (shown shaded grey)



exists, the protection will be re-triggered after a short time. In this way the circuit limits the energy dissipated by the transistors.

It should be noted that the transistor must be robust enough to withstand the fault condition while the short circuit protection reacts - that is to say devices with a large RBSOA must be used.

4. TRANSISTOR SELECTION

Because of the tight cost constraints and the voltage range of this application, the bipolar is the usual choice of transistor. The voltage and current ratings of the power devices used must be selected based on the circuit topology, the required output power and the frequency of operation.

4.1 Voltage rating

The required voltage rating of the devices is defined by the half-bridge topology. Supplying the circuit with 220V RMS A.C. mains, calculating peak value, and adding a safety margin, gives a maximum supply voltage V_{CC} of:

$$\begin{aligned} V_{CC(\max)} &= 220V \times \sqrt{2} + 10\% \\ &= 310V + 10\%. \\ &\approx \mathbf{350V}. \end{aligned}$$

To this figure must also be added the overvoltage generated by the input filter at turn-off. In practice, devices are used with a rating of:

$$V_{CE(\max)} = 450 - 500V$$

4.2 Current rating

The nature of the half-bridge topology is such that in normal operation, half the supply voltage is dropped across each device, so from the above figures V_{CE} in the steady state is $310V / 2$, 155V. Hence the collector current in the steady state can be calculated using:

$$\begin{aligned} P_{OUT} &= I_{C(RMS)} \cdot V_{CE(RMS)} \\ V_{CE(RMS)} &= 1/2 \cdot V_{mains} \\ I_{C(RMS)} &= \frac{2 \cdot P_{OUT}}{V_{mains}} \\ I_{C(RMS)} &= \frac{I_{C(\text{peak})}}{\sqrt{2}} \\ I_{C(\text{peak})} &= \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{V_{mains}} \\ &= \frac{2 \cdot \sqrt{2} \cdot 50W}{220V} \end{aligned}$$

$$I_{C(\text{peak})} = \mathbf{0.64A}$$

As stated above, when the circuit is first turned on, the low initial resistance the lamp filament causes a large current to flow through the transistors. This current can be up to ten times the current in the steady state, and the devices must be selected to withstand this.

In this example then it is recommended that the device used is bipolar transistor, rated at 450V and around 7A. An example is the BUL38-D, which also incorporates an integrated anti-parallel diode.

4.3 Storage and fall times

The fall time, t_{fall} , of the transistors influences the losses of the circuit, while the storage time, t_s , is important as it affects the switching frequency of the converter. The nature of the processes used to produce bipolar transistors means that the storage time between batches of transistors may vary considerably. The transistors used must be manufactured, tested and selected to have storage times within certain limits.

Transistors with too large a storage time may cause the circuit to oscillate below the operating limits of the output transformer, causing saturation of the core towards the end of each cycle. This will cause a spike in the collector current of the transistors every cycle, which will eventually cause them to overheat and be destroyed.

5. POWER FACTOR CORRECTION

As the capacitor at the input of the circuit is relatively small, there is little deformation of the input current waveform. However, this type of circuit generates a certain amount of electro-magnetic interference, due to the high frequency source that feeds the resonant network, and so a suitable filter must be inserted in the circuit before the rectifier bridge to prevent this interference being fed back to the mains. This filter must satisfy VDS and UL norms concerning maximum RFI levels, clearance and creepage distances and the frequency response of the filter.

CONCLUSION

Electronic transformers can offer an economic, simple and compact alternative to the traditional 50Hz transformer. This technique is particularly useful in halogen lamp applications because of the short circuit protection, reduced weight, absence of acoustic noise and the possibility of including a dimming facility.

APPLICATION NOTE

The simple general circuit shown and the guidance given in choosing a suitable transistor should provide a useful starting point for developing more specific applications.

RECOMMENDED TRANSISTOR TYPES

Lamp Power	Recommended Transistor
50-60W	BUL38D*
50-100W	BUL67/ BUL58D*
100-120W	BUL87
150W	BUL810
200-250W	BUV48/BUL810

* With integrated diode

TELEVISION and MONITORS



TRANSISTORS FOR HORIZONTAL DEFLECTION IN TELEVISIONS AND MONITORS

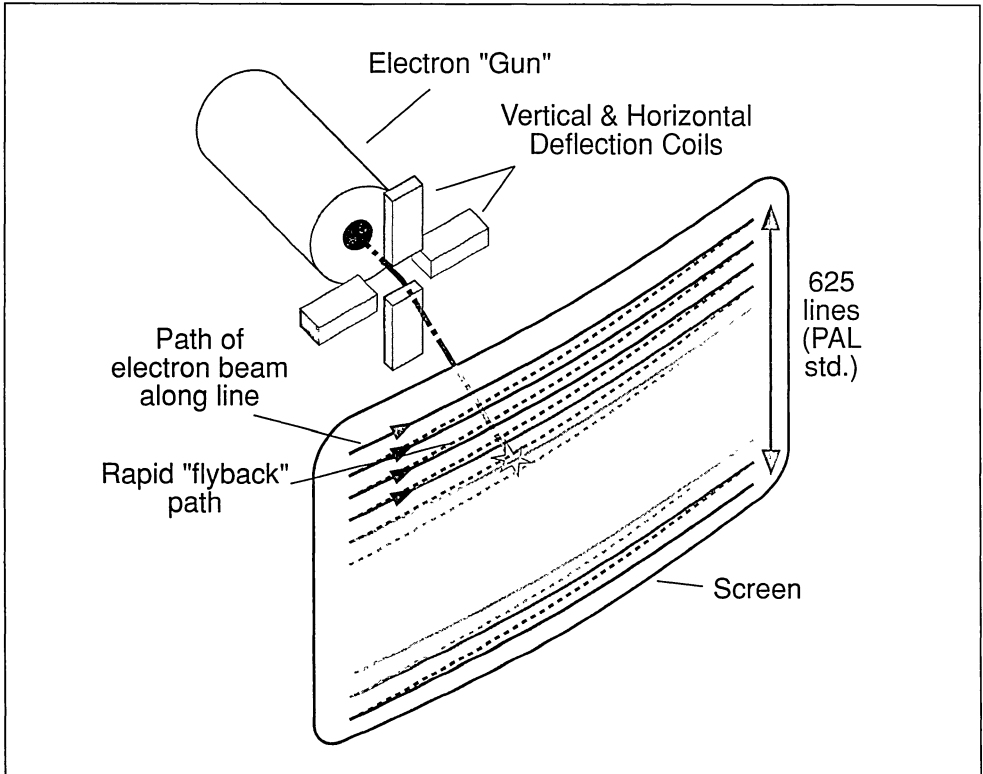
by V. Sukumar

ABSTRACT

The low cost and good performance of high voltage bipolar transistors have meant that these devices remain as the designers first choice in horizontal deflection circuits. As higher definition monitors and television circuits appear, the frequency of operation of the transistors has moved from 16kHz to 32kHz, 64kHz, and up to 100kHz. This paper shows how improved design of die and packages result in transistors optimised for operation at these higher frequencies.

The first section of the paper is an introduction to the operation of the deflection transistor. The switching times and power losses are analysed. The following section describes the characteristics of different transistor technologies. The various options that a power transistor designer has are outlined. The transistor characteristics are divided into three areas: (i) edge termination, (ii) the emitter layout and (iii) the vertical structure. Each of these topics are dealt with in detail. The performance of transistors of similar voltage ratings and die size but with different

Figure 1. Simplified representation of horizontal deflection



design are compared. The possibility of higher frequency operation and the different techniques used to increase the speed of the transistors are also discussed. Isolated packages designed specially for TV and monitor applications are shown in the next section. The performance trade-offs implied in the integration of the damper diode are discussed briefly. The designed trends of the future are mentioned in brief.

1. INTRODUCTION

The designers of TV and monitor horizontal deflection circuits have traditionally required a switch working at around 1500V and at frequencies around 16kHz. The current requirements of the transistor switch varied between 2A and 7A, depending on the screen size, resolution of the picture tube etc. For many years the switch chosen for horizontal deflection has been a high voltage power bipolar transistor like the well known BU508A.

The trend towards monitors with better resolution and, to some extent, higher definition televisions has led to the development of high frequency transistors designed specifically for this application. While many modern TVs have their horizontal deflection frequency increased from 16kHz to 32kHz, the advances in computer graphics, especially monitors for workstations and desktop personal computers have pushed the horizontal deflection frequency of computer desktop monitors to 64, 80 and up to 100kHz.

Today, the low price and good performance of 1500V bipolar transistors have precluded other circuit options like MOSFETs and IGBTs.

We shall limit our discussion to the horizontal deflection transistor, since vertical deflection transistors are often incorporated into a vertical deflection power IC.

2. TELEVISION DEFLECTION

A greatly simplified view of the operation of the CRT in a domestic television using the PAL (625 line) standard is shown in figure 1.

The picture on a television or monitor tube is produced by an electron gun, which produces a beam which is scanned across the inner surface of the tube, causing a coating of phosphors to fluoresce. In order to cover the entire screen, the movement of the striking point of this beam is controlled by magnetic coils in two axes - horizontally and vertically - in such a way as to cover the screen in a pattern of horizontal lines. The refresh rate of the screen is thus defined by the rate at which the beam travels from the top of the screen to the bottom. The point of impact of the beam is moved in the vertical direction relatively slowly - often refreshing the screen at half the mains frequency, 25 or 30Hz. In these applications, the horizontal switching frequency is generally 16kHz, although for a very high resolution computer monitor with a high refresh rate (eg 72Hz) this can be around 80kHz.

3. THE HORIZONTAL DEFLECTION CIRCUIT

A basic deflection circuit using a base drive transformer is shown in figure 2, and figure 3 shows circuit waveforms.

The purpose of the horizontal deflection circuit is to provide a signal to the horizontal deflection coil to

Figure 2. Basic Deflection Circuit

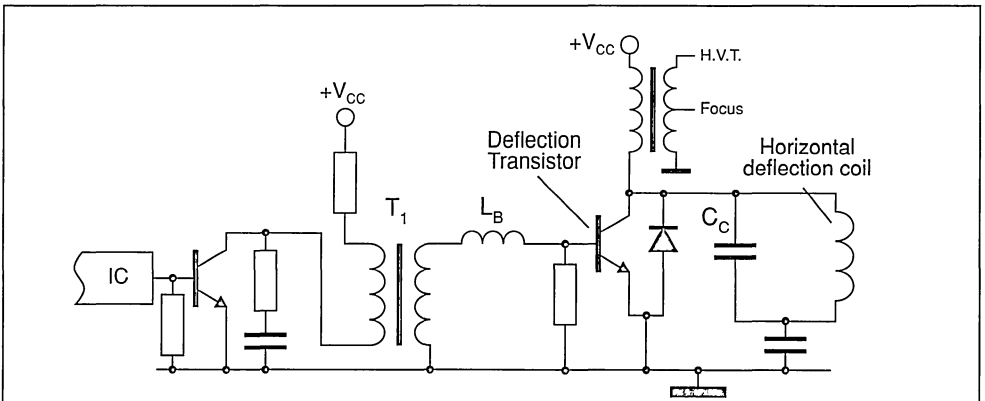
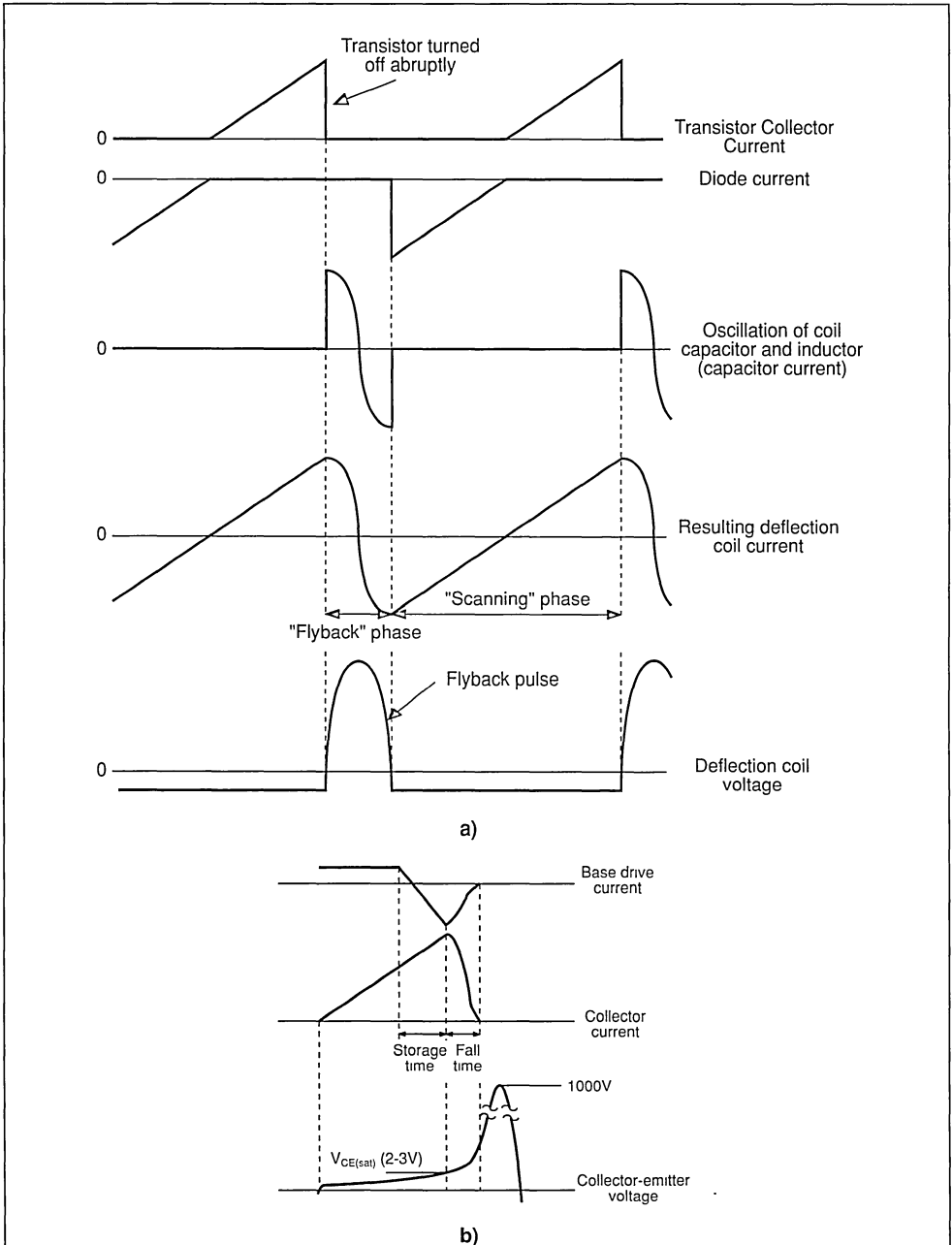


Figure 3. Transistor Switching Waveforms: a) Circuit operation
b) Transistor switching



cause the beam to scan across the screen at a constant speed, and then to make the beam to “fly back” at the end of the write cycle, ready to write another line on the screen. This is achieved by generating a current ramp for the duration of the write cycle, and then turning off the transistor abruptly at the end of the cycle, causing a high voltage pulse in the deflection coil. Transistor turn on causes a current ramp through the inductor. Abrupt turn off of the transistor results in a large flyback pulse seen at the collector of the transistor. This flyback pulse is stepped up to several kilovolts by the flyback transformer, which pulls the electron beam back from one side of the screen to the other. Normally a supply voltage of around 150V results in a peak collector voltage of over 1200V. Traditionally, this has made the use of 1500V (V_{CBO}) transistors common in this application.

Where possible, base drive of the high voltage transistor should follow the collector current ramp. A proportional base drive scheme is best to provide a constant forced gain of adequate level during the time the transistor is on and prevents the transistor from going into hard saturation. Hard saturation of the transistor can lead to current tailing, which in extreme cases can result in thermal runaway and destruction of the transistor. Often a base inductor, shown as L_B in figure 2, is used to decrease the fall time of the transistor and hence the losses. At turn-off, the high reverse base-emitter voltage caused by this inductor will result in the (harmless) avalanche breakdown of the base-emitter junction of the transistor every switching cycle.

4. DEFLECTION TRANSISTOR LOSSES

The most important power losses in the high voltage transistor are:

- i) Saturation Losses or On State Losses. The on-state losses and transistor dynamic saturation are usually significantly less important than the turn off losses in the transistor.
- ii) Turn Off Losses. This can be further divided into:
 - a) Losses in the storage time. During this time, the current through the transistor remains close to I_{Cmax} while the voltage across the transistor is increasing. Adequate forward base drive prior to turn off along with careful design of the transistor are needed to avoid dynamic desaturation of the transistor. Dynamic desaturation of the transistor leads to increased on-state voltage, $V_{CE(on)}$, during

the storage time, which in turn increases the losses.

- b) Losses associated with the fall time. This value is usually small but a current tail here could significantly increase the losses. Minimizing the current tail is an important goal in transistor design.

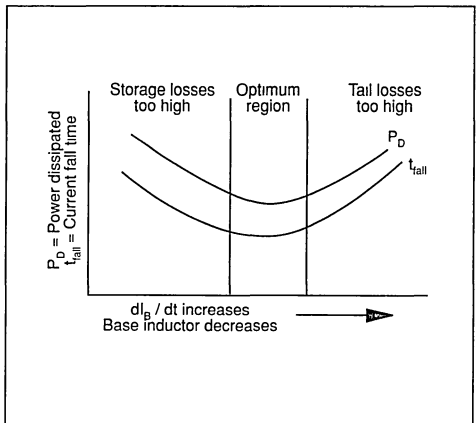
We will assume that the turn on and leakage losses are negligible. In general it is seen that the bulk of the losses are not during the ‘on’ condition but during turnoff (storage and fall time losses).

4.1 Rate of Change of Turn Off Base Current.

In traditional transistor designs, the rate of change of base current (di_B/dt) at turn-off is very important in determining the losses. di_B/dt , of course, depends on the inductor L_B in series with the base drive transformer. The power losses and the current fall time curves vary with the rate of fall of reverse base current, as shown in figure 4.

This curve shows that there is an optimum range of the rate of change of base current. If the transistor is turned off too slowly, the excess minority carriers are not extracted quickly enough from the lightly doped N- collector area. The voltage across the transistor increases, leading to higher switching losses. If the extraction of the charges is too fast, the collector-base diode junction recovers more slowly than the base-emitter junction. The minority carriers trapped in the lightly doped N- region give rise to a ‘current tail’ that can dramatically increase the switching losses. The current tail has a positive temperature coefficient and hence can lead to thermal

Figure 4. Variation of Losses with Base Current



runaway which can destroy the transistor. The optimal drive conditions therefore fall in between the high storage losses region and the high current tail losses region.

It is possible to some extent to design a transistor to make the extraction of minority carriers easier. From the point of view of a designer of the transistor die, the flatter the curves shown in figure 4 can be made, the more versatile the transistor will be, since it will be more immune to variations in the drive circuit. It is preferable to design a transistor with slightly higher power losses if the losses are reasonably independent of the base inductance (dl_b/dt).

4.2 Base drive design

The base drive design for the horizontal deflection transistor is important, to minimise the losses. There are a number of solutions available, and the choice of solution depends on the characteristics of the individual application. They fall into two basic classes: those used for TVs; and those used for monitors.

In a TV, the horizontal frequency and screen size are known and fixed, and hence many electrical parameters (e.g. I_C , $V_{CE(tyback)}$) are already defined. The main tasks of the drive are therefore to generate the base current to achieve these values (compensating for variations in the h_{FE} of the devices used), and to produce an optimised reverse base current to reduce turn-off losses.

In monitor circuits, the horizontal frequency and screen size are usually not fixed (monitors are often multi frequency, and the screen size may be varied by the user), and so I_C and $V_{CE(tyback)}$ are not fixed. In this case it is important to have a base drive which can adapt to the various conditions. One way in which this can be achieved is to use a proportional base drive, where the base current follows the collector current.

5. BIPOLAR TRANSISTOR TYPES

Having to switch voltages in the range of 1200V or more, and allowing a safety margin, means that 1500V transistors are the de facto standard. One goal in transistor design is to ensure that the transistor is, less dependent on variations in the base drive circuit (especially rate of change of base current). Switching speeds should be as fast as possible. The spread in device characteristics from device to device, especially the dc gain (h_{FE}), storage time etc. should be minimised. The same device used in horizontal deflection is, for cost reasons, often used

in the SMPS in the TV or monitor as well. This means that although the transistor used in the deflection circuit does not require a large RBSOA, as the transistor used in the SMPS does, the transistor designer should design for the largest possible RBSOA to maximise the ruggedness for a given transistor area.

5.1 Edge termination

The design of the edge termination of the transistor is important (indirectly) in determining the switching performance of the transistor. The techniques used in edge termination could be used regardless of the type of transistor: MOSFET, bipolar, IGBT etc.

The two edge termination techniques most commonly used in horizontal deflection transistors are:

- i) Mesa edge termination, and
- ii) Planar edge termination techniques.

Both termination techniques are widely used in the industry today. Their advantages and disadvantages can only be evaluated in the context of the design of the entire transistor, especially the design of the vertical structure.

Once a decision is made to use mesa or planar edge termination design, the efficiency and reproducibility of the design process will greatly affect the transistor performance. For example, the quality of the edge termination determines whether, in order to meet a guaranteed 1500V V_{CES} specification, the average transistor will have a breakdown voltage of 1550V or 1800V. Process parameters will, in this way, affect switching losses and performance as much as design. The efficiency of edge termination of the transistor determines how the edge termination can be achieved in the minimal area and how much higher the bulk resistance of the silicon should be increased for good yield at the specification limit.

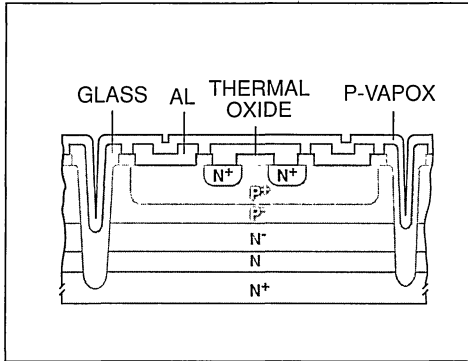
5.2 Layout Design of the transistor- Emitter Layout.

This part generally refers to the design of the emitter and base fingers or cells.

5.2.1 Design of the emitter structure

Figure 5 shows the structure of a hollow emitter transistor. The traditional structure has been a hollow emitter. The 'hollow' is created by an oxide layer in the centre of the emitter forcing the current only to the edges. The increased peripheral area reduces current crowding, leading to faster switching. Hollow

Figure 5. Hollow Emitter Transistor



emitter transistors have been in use for over ten years with good results. The major disadvantage of the hollow emitter transistor is that conduction is limited to the periphery of the emitter region. In other words, some of the silicon area of the hollow emitter transistor is “wasted” as the current that can be switched per unit area of silicon is reduced. Efficient emitter design can mean better cell layout, which significantly increase the power handling capability (especially turn off current at high temperature).

The latest trends in emitter design have included:

- i) Emitter strips. This implies a finer geometry. This can be understood as the shrinking of the thickness of the emitter finger till, at the limit the oxide layer creating the hollow emitter disappears entirely.
- ii) Cellular Emitter. This is the extension of the Emitter Strips technique to a second dimension to form small cells in the emitter structure. These cells, which are connected by a metal layer result in faster removal of charge at turn-off, improving switching speed. Figure 6 shows the structure of a cellular emitter design.
- iii) Base Islands. This technology is similar to the cellular emitter. Here the base, not the emitter is placed inside an island and the emitter connections are interspersed between the base islands.

Figures 7 compares the various technologies. Planar transistors designed with these new layout designs have a better RBSOA than those of conventional design. Our results show that the cellular emitter has high current gain characteristics superior to alternative emitter structures. The difference between these three different emitter design technologies, however, is not very large.

Figure 6. Cellular Emitter Transistor:
a. Cross Section (single cell)
b. Plan View

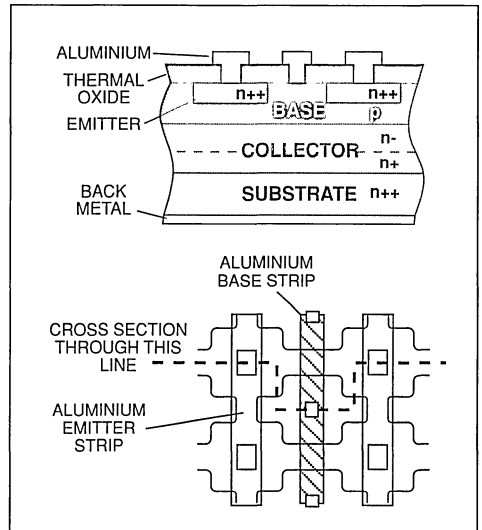
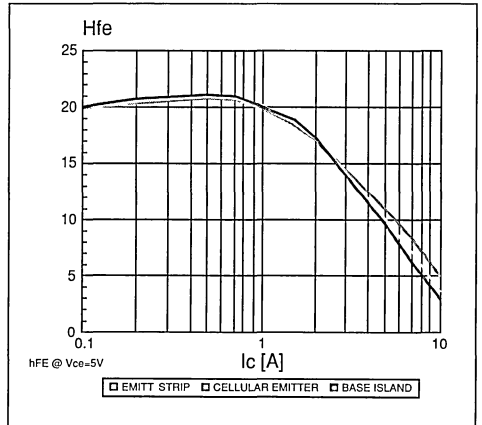


Figure 7. Effect of Emitter Geometry on hfe



5.3 Design of the Vertical Structure

As the transistor breakdown voltage increases, the variations in the emitter layout are not as important as those in the vertical structure. The 1500V deflection transistors that are used for horizontal deflection voltage have large lightly doped collector epitaxial structures (over 110 micrometers). There is not a great amount of variation possible in the

design of the collector structure.

The optimisation of the base structure is one of the most important parameters affecting device switching performance. In a transistor of conventional design, the safe operating area at turn off could be improved by the addition of an 'energy layer' a thin additional epitaxial N+ layer. This increases the RBSOA, but at the expense of switching speed. That is, the thicker the energy layer, the better the RBSOA but the slower the transistor. It has been found that by careful optimisation of base diffusion design of the planar transistor, the RBSOA can be increased while keeping the switching speed of the device high.

Significant other performance improvements can be achieved by optimising the base structure of the transistor. By optimising the design of the junction, better stability after HTRB is possible. The gain of

the transistor can be made flatter and less dependent on the value of the current. An incidental benefit of this is that the variation of the current gain (h_{FE}) with temperature is lowered. This is important in horizontal deflection circuit design since it protects against transistor runaway.

The optimisation of the vertical structure and the emitter layout lead to a decrease in the (equivalent) base parasitic resistance r_{bb} . This makes the turn off base current more effective in removing stored charge in the transistor. Switching times and hence switching losses are reduced.

Figures 8 and 9 compare the SOA and fall times of similar conventional hollow emitter and the newer generation planar transistor. In the conventional hollow emitter transistor, the rounded waveform of the reverse bias base current is caused by a high

Figure 8. Effect of Base Design on RBSOA: a. Hollow Emitter Transistor
b. Cellular Emitter Transistor

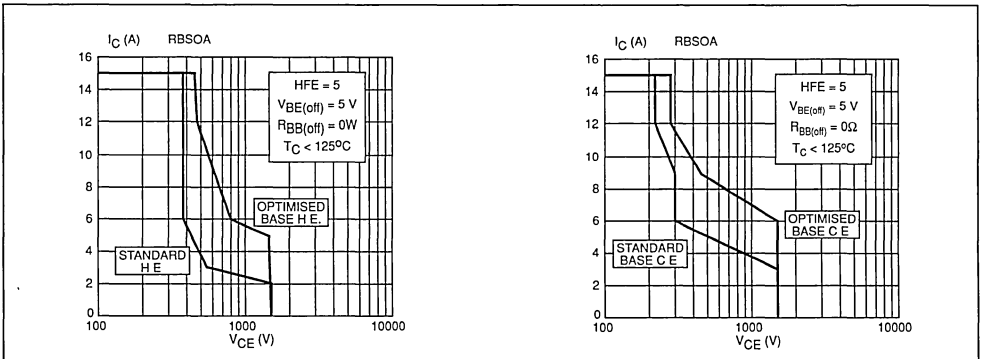
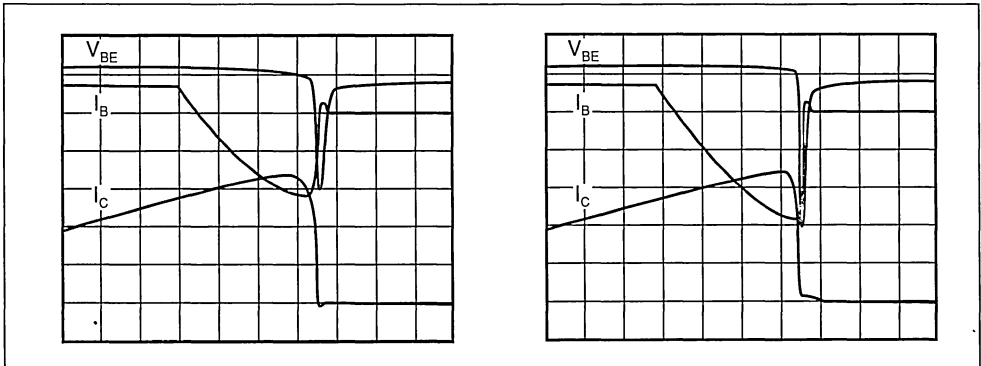


Figure 9. Turn Off Times: a. Hollow Emitter Transistor
b. Cellular Emitter Transistor



value of the base spreading resistance. The new planar transistor with reduced $r_{bb'}$ has current fall times about two thirds of that of the conventional transistor. The techniques explained below can lead to a further reduction of storage and fall times in the transistor.

5.4 Techniques for Improved Switching Speed

Techniques of a similar nature are used in rectifier diodes, IGBTs and bipolar transistors to increase switching speeds. The excess charge present at turn off is removed by the creation of recombination centres. These recombination centres are made by precious metal (Pt, Au) doping or by fundamental particle irradiation. Electron irradiation is one example of how recombination centres are created. The flaws in the crystalline structure caused by irradiation is where the recombination occurs. The minority carrier lifetime, a physical parameter of the transistor which controls the gain, and switching times for a transistor of a given breakdown voltage can be reduced significantly. As a result of the creation of these recombination centres, these devices exhibit higher on-state voltage than before but their switching times are reduced dramatically.

The storage times and the fall times are significantly reduced by irradiation. The tail in the collector current in turnoff is lowered. This results in significant reductions in the turn off losses and hence device junction temperature. The on voltage during the storage time period is also increased but the total losses during this period are marginally reduced because of the reduction in the storage time itself. The unit-to-unit spread in the switching parameters of the transistors are greatly reduced. This is also very important from the circuit design point of view.

Another method to increase the switching speed of the transistors is to monolithically integrate portions of the drive circuit on to the high voltage transistor. Here the challenge is to manufacture this complex circuit at the very competitive prices common in this market.

6. ISOLATED PACKAGES FOR DEFLECTION

Isolation of the high voltage transistors is very important. In high volume applications such as TVs and monitors, isolated packages save manufacturing costs and time and increase safety and reliability. Some of these packages, such as the ISOWATT218 are similar to their non-isolated counterparts but with a thin layer (a few tenths of a mm) of a thermally

conductive but electrically insulating plastic layer to provide the isolation. To meet VDE and EN isolation requirements, a second generation of smaller, low cost packages was developed for increased isolation as well as creepage distances. These methods of moulding thermally conductive plastic over the heat spreader is easy to automate. This results in lower costs and better reliability.

7. THE DAMPER DIODE

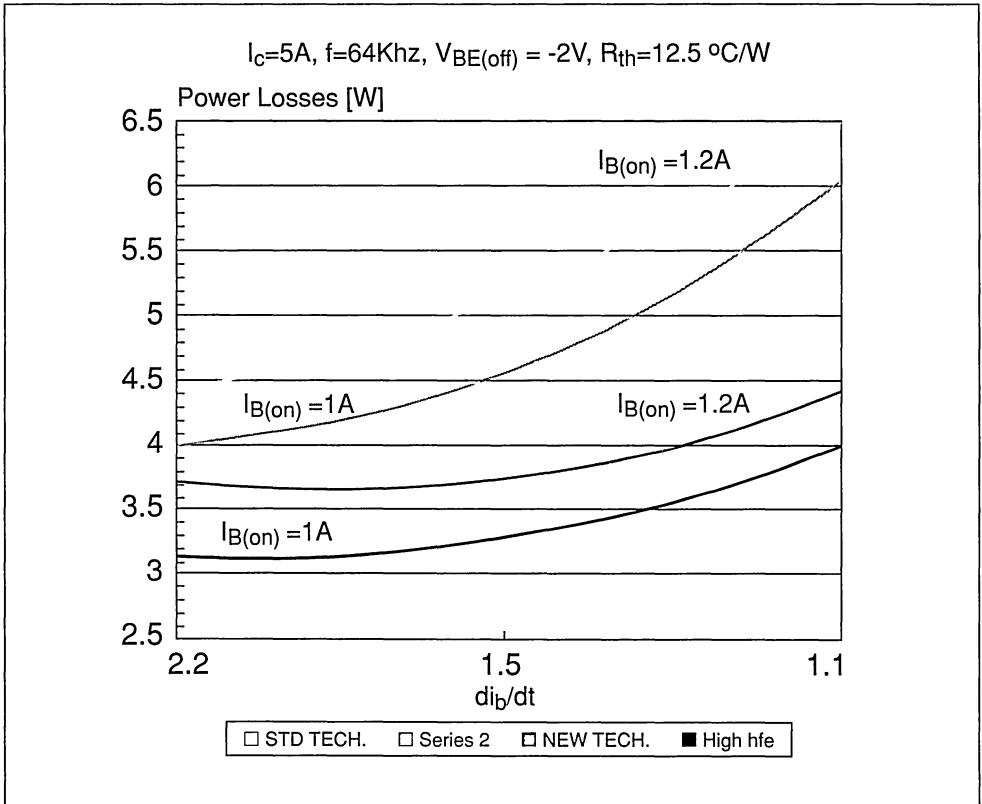
It is possible to manufacture a planar or mesa deflection transistor with an integral collector-emitter anti-parallel rectifier diode, simply by changing one or two masks in the process. Some design compromises are sure to result if the antiparallel diode is integrated. The integrated antiparallel diode, for example, will have recovery times at least twice that of an external rectifier diode designed solely for this application. Techniques designed to speed up the fall time of the transistor usually speed up the recovery times of the diode as well. Therefore, for low frequency operation, deflection transistors with integrated collector-emitter diodes can be used, while at high frequencies, specially designed "damper diodes" are used. These diodes designed specifically to minimise the forward recovery time and the turn on forward voltage overshoot. An example of this kind of damper diode is the DTV32F1500A.

8. FUTURE TRENDS

Figure 10 compares the total losses in two similar 1500V switching transistors while switching a peak collector current of 5A at 64kHz. These current and frequency specifications are a real challenge for the transistors of such a small die size. A typical modern planar transistor is compared with a conventional transistor, sorted for high gain. The low gain conventional transistors went into thermal runaway under these conditions. By using transistors with larger die size, even higher current and higher frequency operation is possible.

In the short to medium term, bipolar horizontal deflection transistors are not likely to be replaced by MOSFETs or IGBTs. A more likely replacement would perhaps be a Power IC, an intelligent power switch specifically designed for horizontal deflection. An example of this type of circuit is a 1500V monolithic emitter switch with built in drive and protection features.. In the near future, the careful layout and design will keep the bipolar transistor as the device of choice in horizontal deflection circuits.

Figure 10. Comparison of Transistor Losses



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- (ii) A. Galluzzo and A. Morgan, "Improved Power Transistor Performance with Fast switch Hollow Emitter Technology", AN360/0689, SGS-THOMSON Power Transistor Application Manual, 1st Edition.
- (iii) L. Wuidart, "A Transistor for 100kHz Converters: ETD" , AN361/0689, SGS-THOMSON Designers Guide To Power Products, 2nd Edition.

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PCIM Europe

June 1994

Nürnberg, Germany

**TV AND MONITORS :
CHOICE OF DIODE FOR A HORIZONTAL DEFLECTION**

B. Rivet

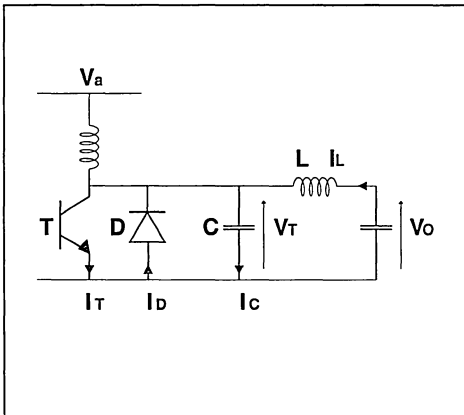
I - INTRODUCTION

The purpose of this note is to review the operation of the basic horizontal deflection circuit, to do an analysis of the different losses in the damper diode, and to suggest criteria for choosing between the DTV32-1500A and DTV32-1500B for a given application.

II - BEHAVIOUR OF THE BASIC HORIZONTAL DEFLECTION CIRCUIT

The basic horizontal deflection circuit is shown in Fig.1

Fig.1 : Basic horizontal deflection circuit



The current and voltage waveforms in the circuit are shown in Fig.2

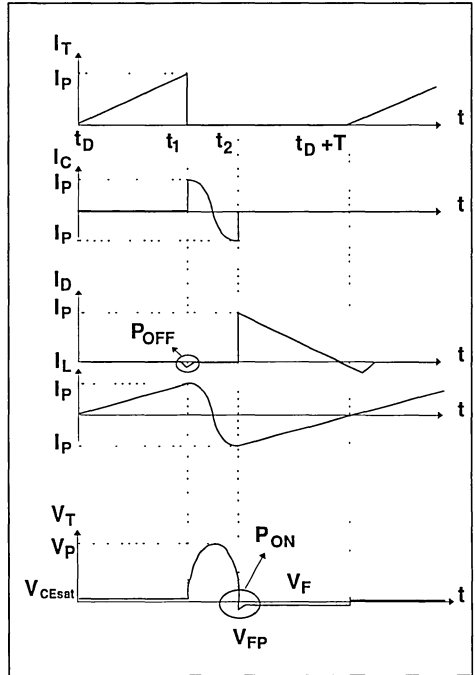
At $t = t_0$ the transistor starts to turn ON. The current in the line yoke and in the transistor is given by

$$I_T(t) = I_L(t) = \frac{V_0 \cdot t}{L}$$

The voltage V_T across the diode is equal to the V_{CEsat} of the transistor. The damper diode is blocked.

At $t = t_1$ the transistor starts to turn OFF, the circuit becomes resonant ($V_0 \cdot L \cdot C$). The current in the line decreases from I_p to $-I_p$ and an overvoltage (V_{FP}) appears across the diode.

Fig.2 : Waveforms in the basic horizontal deflection circuit



At $t = t_2$ the voltage V_T across the diode becomes negative and the damper diode conducts. The current in the diode and in the line Yoke is then :

$$I_D(t) = -I_L(t) = I_p - \frac{V_0 \cdot t}{L}$$

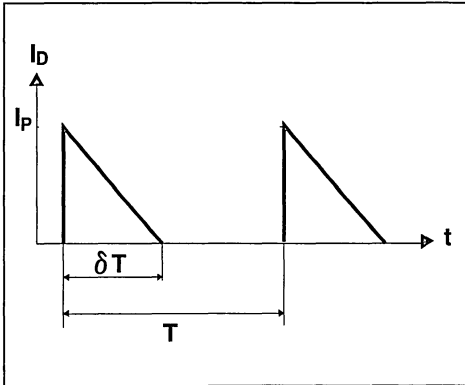
At $t = t_0 + T$ a new cycle starts

III - ANALYSIS OF THE POWER LOSSES IN THE DAMPER DIODE

a) Conduction losses : P_{COND}

The current in the damper diode is triangular Fig.3

Fig.3 : Current in the damper diode



The conduction losses are given by :

$$P_{COND} = V_{TO} \cdot I_{F(AV)} + r_d I_{F(RMS)}^2$$

with

$$I_{F(AV)} = \frac{I_P \delta}{2}$$

and

$$I_{F(RMS)}^2 = \frac{I_P^2 \delta}{3}$$

Example : With a DTV32-1500 A

$$\begin{aligned} V_{TO} &= 1 \text{ V} \\ r_d &= 25 \text{ m}\Omega \\ \text{and} \\ I_P &= 6 \text{ A} \\ \delta &= 0.45 \end{aligned}$$

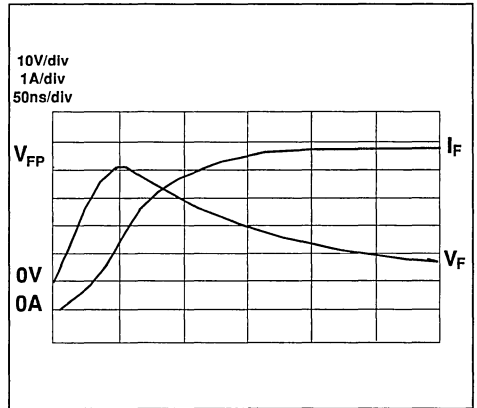
We find $P_{COND} = 1.5 \text{ W}$

b) Switch ON losses : P_{ON}

When the diode switches ON ($t=t_2$ Fig.2), the current in it increases from 0 to I_P with a high dI/dt ($80 \text{ A}/\mu\text{s}$). This current variation results in an overvoltage across the diode (V_{FP}) and switch ON losses.

Fig.4 shows the oscillogram of the current and the voltage across the damper diode when it is switched ON.

Fig.4 : Current and voltage in the damper diode at switch ON



P_{ON} is calculated with the oscillogram of Fig.4 and the following formula :

$$P_{ON} = \frac{1}{T} \int_0^{t_{fr}} V_F \cdot I_F dt$$

t_{fr} is the time during which the voltage across the diode increases from 0V to V_{FP} and then decreases from V_{FP} to $V_{FR} = 2V$

Example : With a DTV32-1500B

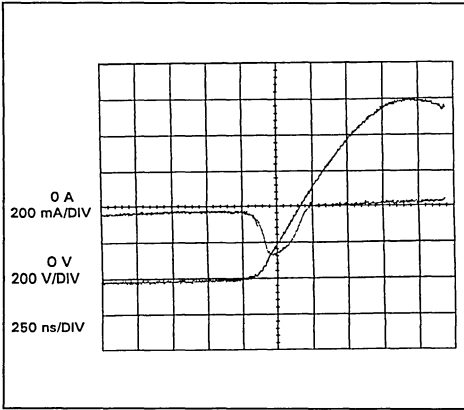
$$\begin{aligned} \text{and} \\ T_j &= 100^\circ\text{C} \\ dI/dt &= 80 \text{ A}/\mu\text{s} \\ V_{FP} &= 42 \text{ V} \\ f &= 32 \text{ kHz} \\ I_P &= 6 \text{ A} \end{aligned}$$

We find : $P_{ON} = 1 \text{ W}$

c) Switch OFF losses : P_{OFF}

When the switching frequency of the horizontal deflection circuit is low (40 kHz), P_{OFF} is negligible. The diode disposes of all its stored charge with a low voltage across it (V_{CEsat}). At high frequencies there is insufficient time to complete this discharge during the conduction time of the transistor. In this case, when the transistor switches off, a current appears in the diode (at $t=t_1$ Fig.2) and the voltage reaches a high value (600 V) resulting in switch-OFF losses (Fig.5)

Fig.5 : Current and voltage in the damper diode at switch OFF ($f = 70\text{kHz}$)



Example : With a DTV32-1500A
 and $P = 6\text{A}$
 $f = 70\text{kHz}$
 $T_j = 80^\circ\text{C}$
 $t_{rr} = 210\text{ns}$

($T_j = 25^\circ\text{C}$ $I_F = 1\text{A}$ $V_R = 30\text{V}$ $dI/dt = -50\text{A/s}$)
 P_{OFF} is estimated at $P_{OFF} = 0.9\text{W}$

This estimate has been made by measurements on the board whose circuit diagram is given in appendix A.

IV - CHOICE BETWEEN THE DTV32-1500A AND THE DTV32-1500B FOR A GIVEN APPLICATION

SGS THOMSON offers two high voltage damper diodes : the DTV32- 1500A and the DTV32-1500B. The principal characteristics of these two diodes are given in the following table :

: Principal characteristics of the DTVV32-1500A and the DTV32-1500B

Parameters		DTV32-1500A	DTV32-1500B
V_{TO}	max	1 V	1.2 V
r_d	max	25 mΩ	34 mΩ
V_{FP}	80 A/μs	30 V	39 V
typ	$V_{FR} = 2\text{V}$		
t_{fr}	typ	500 ns	600 ns
t_{rr}	25°C $I_F = 1\text{A}$ $V_R = 30\text{V}$ -50 A/μs typ	250 ns	130 ns

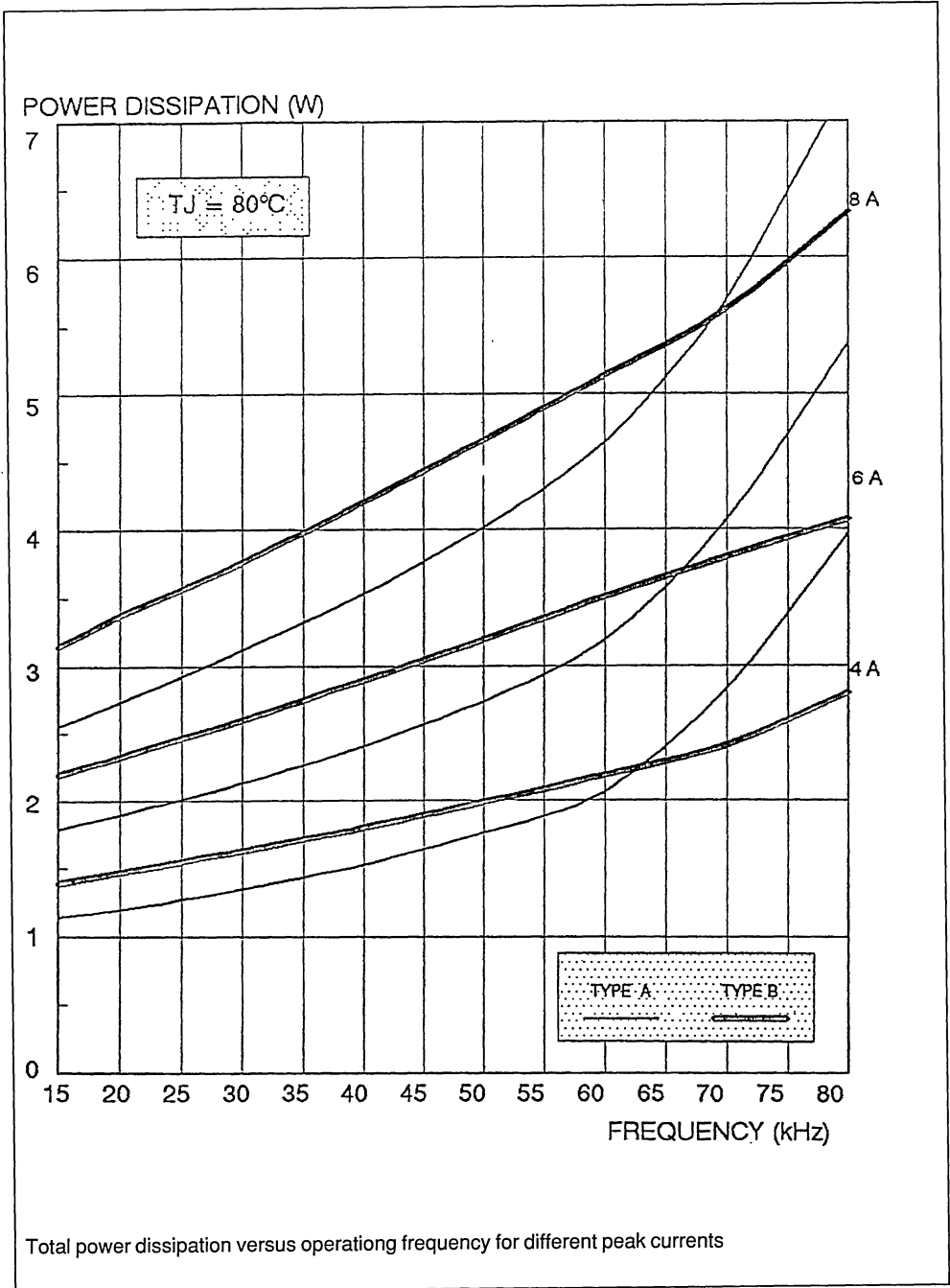
Figs:7 - 9 show the total loss ($P_T = P_{COND} + P_{ON} + P_{OFF}$) in the damper diodes A and B versus frequency, for different currents I_P and different junction temperatures.

These curves have the same forms for the different junction temperatures ($80^\circ\text{C} - 100^\circ\text{C} - 120^\circ\text{C}$)

For the lower frequencies ($< 55\text{kHz}$) total losses are greater in the DTV32-1500B. In this area conduction and switch ON losses are predominant. For the high frequencies ($> 65\text{kHz}$) total losses become greater in the DTV32-1500A (switch OFF losses are more significant in this diode). This difference in high- frequency losses between the two devices also increases with temperature.

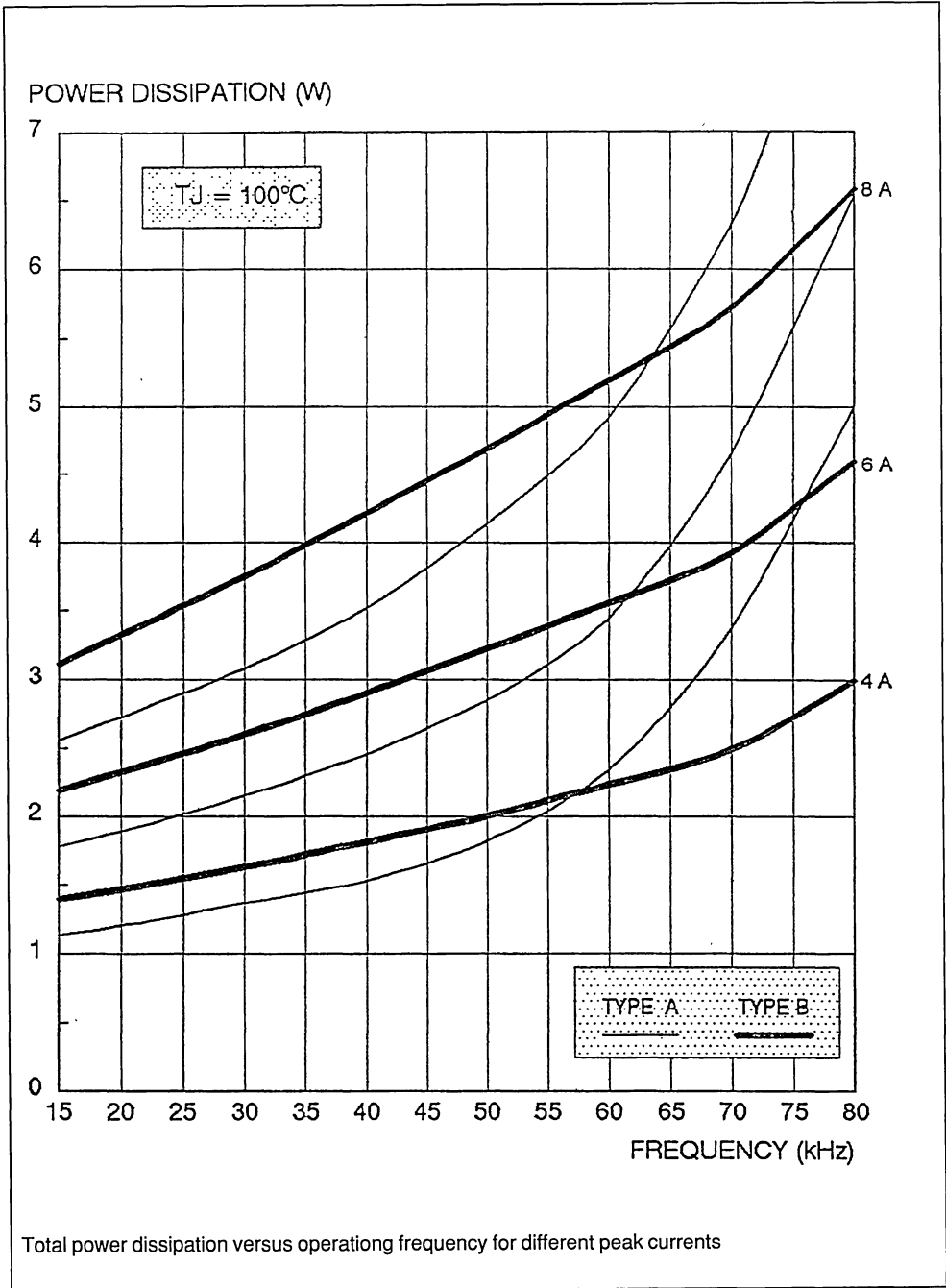
APPLICATION NOTE

Fig.6 : Comparison type "A" and type "B" at $T_j = 80^\circ\text{C}$



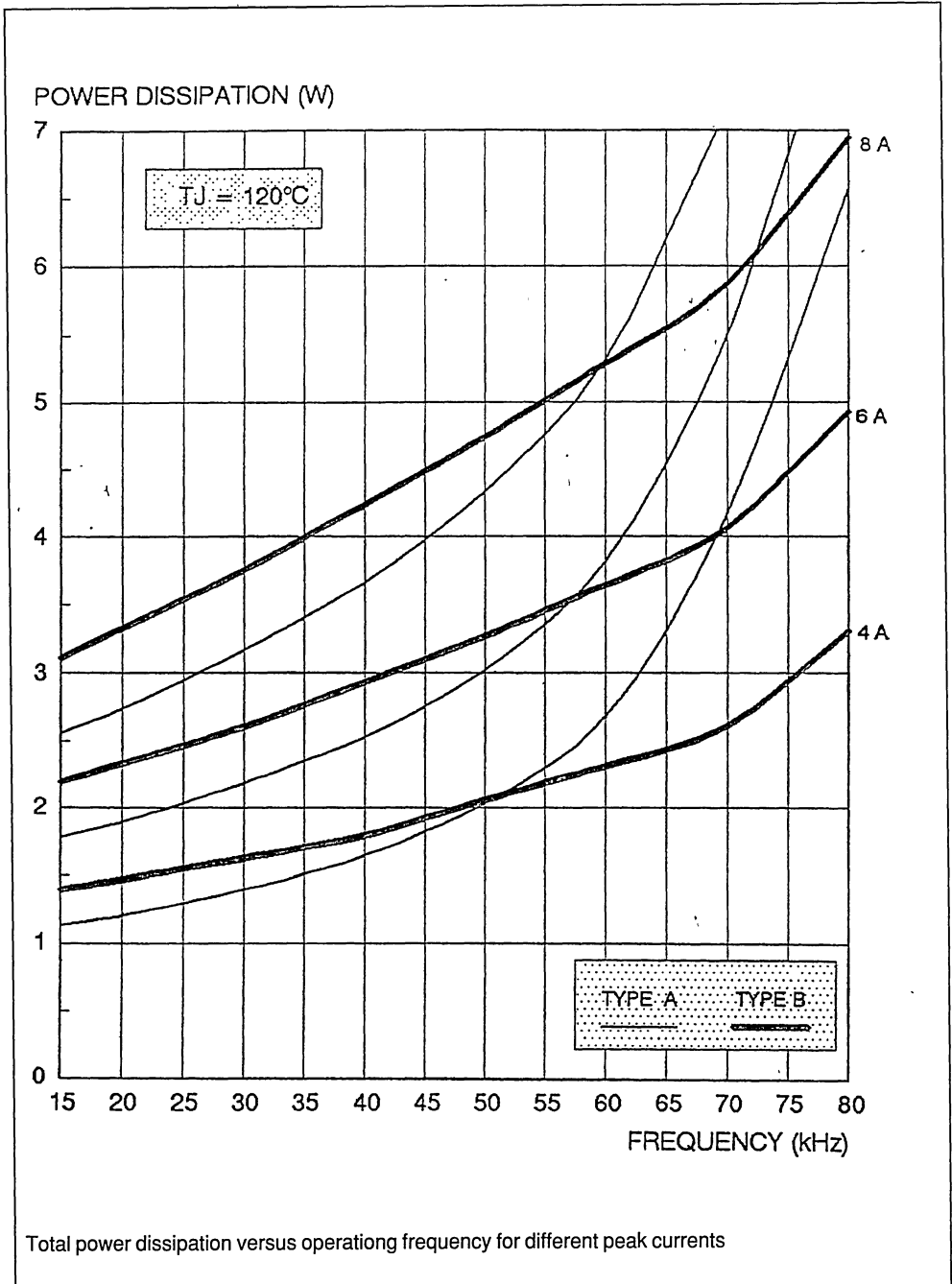
Total power dissipation versus operating frequency for different peak currents

Fig.7 : Comparison type "A" and type "B" at $T_J = 100^\circ\text{C}$



APPLICATION NOTE

Fig.8 : Comparison type "A" and type "B" at $T_j = 120^\circ\text{C}$

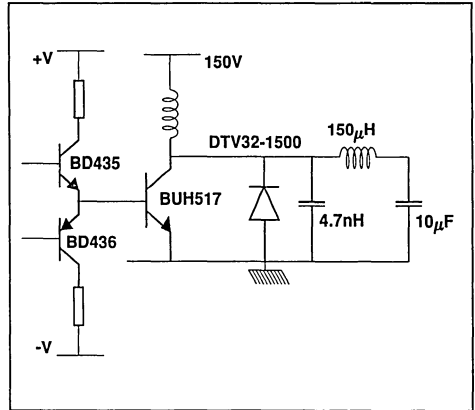


Total power dissipation versus operating frequency for different peak currents

V - CONCLUSION

SGS-THOMSON offers two Damper diodes to cover the need in horizontal deflection circuit for televisions and monitors. The operating frequency determines the choice of damper diode. For frequencies below 55 kHz the DTV32-1500A is preferable while above 65 kHz the DTV32-1500B is the better choice.

APPENDIX A



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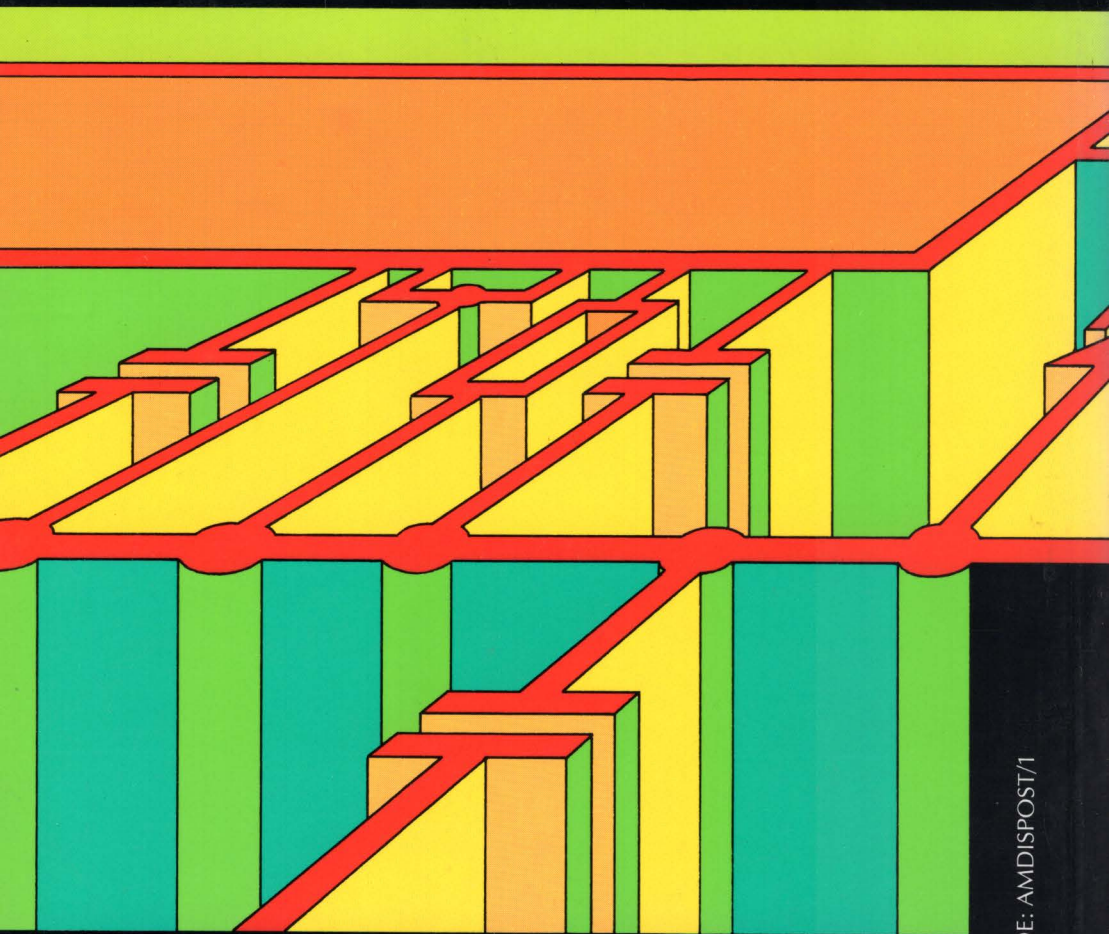
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