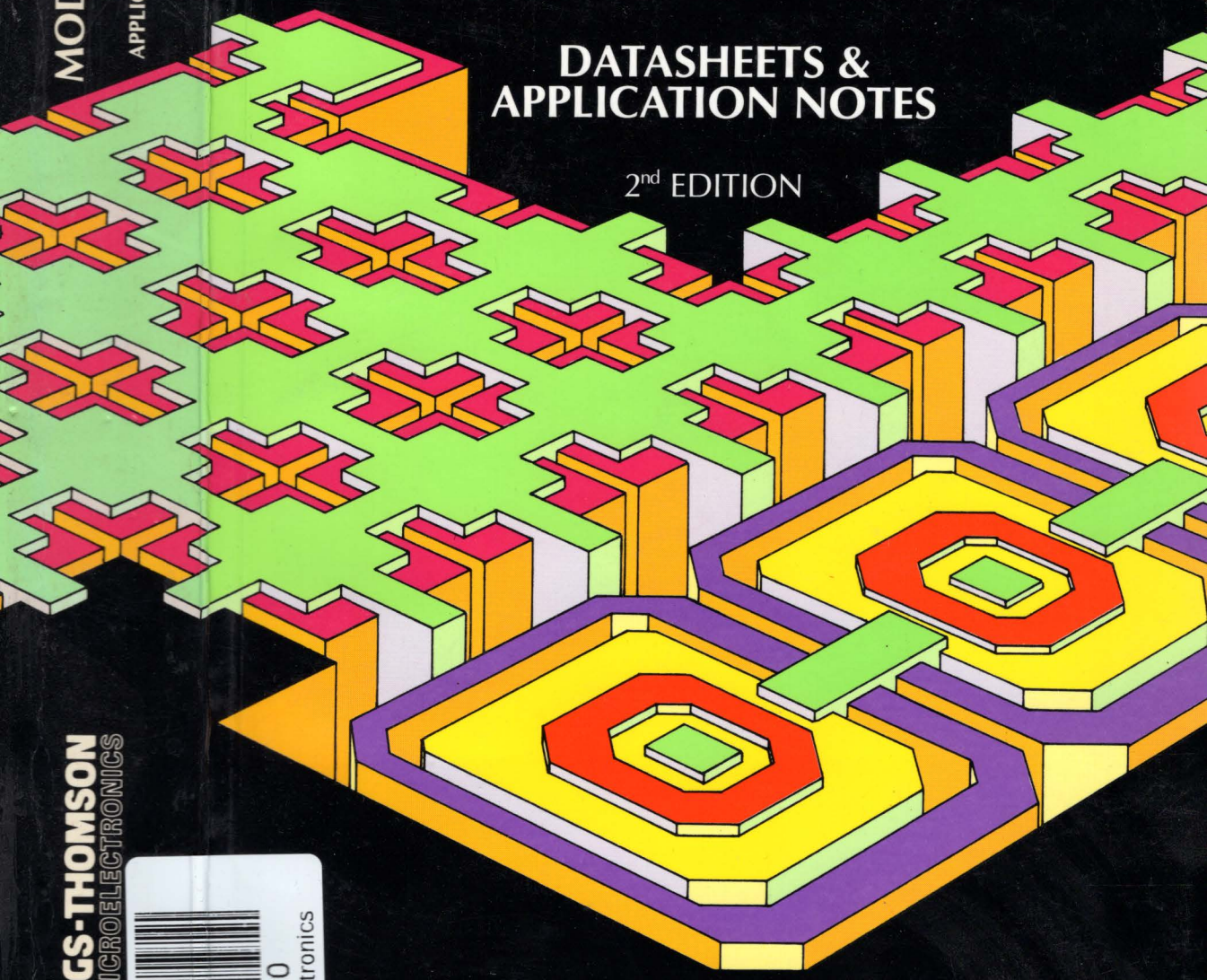
MODEM ICs
DATASHEETS & APPLICATION NOTES

MODEM INTEGRATED CIRCUITS

DATASHEETS & APPLICATION NOTES

2nd EDITION



SGS-THOMSON MICROELECTRONICS

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MODEM INTEGRATED CIRCUITS

DATASHEETS AND APPLICATION NOTES

2nd EDITION

AUGUST 1995

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1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TABLE OF CONTENTS

INTRODUCTION

With Modem integrated circuits from SGS-THOMSON, data, be it fax or voice, can be transmitted via any telephone or power line, any time, at any speed, in any standard or protocol and in any size down to PCMICIA type II format.

The SGS-THOMSON Modem and Power Line Modem IC product range focuses on high performance and high quality devices. All are made with the most appropriate choice of technology, carefully selected from a broad portfolio that is unique to SGS-THOMSON.

With the information contained in the following pages, an optimum solution can be selected in a few seconds. The first table enables selection of a Telephone Line Modem, according to the transmission standard needed. The selection depends on the needs of the user : a complete solution; just a Data Pump; or a leading Modem Analog Front End for V.34 implementation.

Intentionally, the table has been simplified to enable quick selection of a device. It does not pretend to show all embedded functions. For a comprehensive function list, the first page of the datasheet should be consulted. For example, some Modem ICs also include voice functions; Analog Front-end devices include clock generation and can also be used as an Audio Front-end.

The second tables gives a quick summary of Power Line Modem products, arranged according to the required data transmission speed. Again, this table is intentionally simplified and does not pretend to show all the capabilities of the devices or the powerful development tools which allow the user quick turnaround time for a working solution.

Should an appropriate solution not be found in this databook, please contact the nearest SGS-THOMSON Microelectronics representative or salesperson. The solution required may already be in development stage, close to being introduced. And if quantity justifies it, a custom solution can be tailored to meet specific needs, using SGS-THOMSON's wide and proven telecom design experience.

Should other semiconductor components be needed for completion of designs - memories, micros, standard circuits, for instance ask for the SGS-THOMSON Shortform Catalog or CD "Data on Disc" which contain details of the Company's entire product range.

ALPHANUMERICAL INDEX

DATASHEETS

APPLICATION NOTES

MISCELLANEOUS

MODEM

	ITU-T									
	V.21	V.23	V.22	V.22bis	V.32	V.32bis	V.34	V.27T	V.29	V.17
BELL	103		212A							
Modulation	FSK / FDM		DPSK / FDM		DPSK / E.C.			DPSK		
Bps	0-300	75 1200	600 1200	1200 2400	4800 9600	7200 9600 12000 14400	14400 19200 24000 28800	2400 4800	4800 7200 9600	7200 9600 12000 24000
Mode	Full Duplex						Full Duplex Half Duplex	Half Duplex		
Application		Teletext	PC				PC / FAX	FAX		

DATA PUMPS	TS7514				
	TS7515	TS7515			
	ST75C502 / ST7544				ST75C502 / ST7544
	ST75C52 / C520				ST75C52 / C520
MAFE	ST7544 / ST7546				
PCMCIA	ST7548				

Note : For clarity purpose, the slection table is simplified. Data Pumps include many functions which do not appear on this table such as Tone/DTMF generation and detection or caller ID demodulation. Please look at the first page of datasheet to have a complete view of functionalities.

POWER LINE MODEM

	ST7536	ST7537	ST7537HS1
Modulation	FSK Synchronous	FSK Asynchronous	FSK Asynchronous
Bps	600/1200	Up to 1200	Up to 2400
Mode	Half Duplex	Half Duplex	Half Duplex
Carrier Frequency	< 95kHz	≤ 132.5kHz	≤ 132.5kHz

ANALOG FRONT-END

SGS-THOMSON MICROELECTRONICS

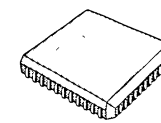
ST7544

UNIVERSAL MODEM ANALOG FRONT-END (UMAFE)

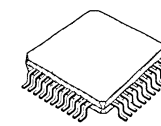
- FULL ECHO CANCELLING CAPABILITY
- FULLY COMPATIBLE WITH THE ST7543 (7543 mode)
- 16-BIT OVERSAMPLING A/D AND D/A CONVERTERS
  - Programmable down-sampling frequency from 7200 to 16000Hz
  - Sampling frequency can be 3, 4, 6, 8, 12, 16 x symbol rate
  - Programmable Over sampling frequency (128 or 160 x sampling frequency)
  - The ST7544 can work with external oversampling clocks
  - Programmable symbol rate (600, 1200, 1600, 2400, 2560, 2743, 2800, 2954, 3000, 3200, 3429 and 3491)
  - Bit rates of 300bps, 600bps, 1200 and all multiples of 2400bps up to 28800bps can be generated
  - Dynamic range : 92dB with a sampling frequency 9600Hz, oversampling ratio 160
  - Total harmonic distortion : -89dB
- ON CHIP REFERENCE VOLTAGE
- THREE PROGRAMMABLE DIGITAL FILTERS SECTIONS :
  - Tx interpolation filter
  - Rx decimation filter (up to 14th order each)
  - Rx reconstruction filter (coefficients loaded into RAM)
- ANCILLARY CONVERTERS FOR EYE-DIAGRAM MONITORING
- CLOCK SYSTEM BASED ON DIGITAL PHASE LOCKED LOOPS
  - Separate Tx DPLL and Rx DPLL
  - Terminal clock input for Tx synchronization on all multiples of 2400Hz (VFast synchronization mode) or on sub-multiple of baud rate (7543 synchronization mode)
  - Bit, Baud, sampling and highest synchronous clock outputs
  - Maximum master clock frequency is 38MHz
- SINGLE OR DUAL SYNCHRONOUS SERIAL INTERFACE TO DSP
- SINGLE POWER SUPPLY VOLTAGE : +5V
- LOW POWER CONSUMPTION :
  - 260mW operating power at the nominal crystal frequency of 36.864MHz
  - 160mW operating power at the crytal frequency of 18.432MHz
  - Less than 5mW in the Low-Power Reset Mode
- 1.2µm CMOS PROCESS
- PLCC44 OR TQFP44 (1.4mm body thickness)

DESCRIPTION

The ST7544 is a single chip Analog Front-End (AFE) designed to implement high speed voice-grade Modems up to 28800 bps with echo cancelling capability.
Associated with one or several Digital Signal Processors (DSP), such as the ST189XX family, it provides a powerful solution for the implementation of multi-mode Modems meeting CCITT (V.21, V.22, V.22 bis, V.23, V.26, V.27, V.29, V.32,V.32 bis and V.33) and BELL (103, 202, 212A...) recommendations. It is fully compatible with the ST7543 in 7543 mode and is also well suited emerging applications involving bit rates up to 28800 bps (in the VFast synchronization mode).
The transmit section includes a 16-bit over-sampling D/A converter with a programmable interpolating filter. The receive section includes a 16-bit oversampling A/D converter with two programmable filters (one for decimation and the other for reconstruction). Oversampling ratio is selectable to either 128 or 160. Two additional 8-bit D/A converters allow eyediagram monitoring on a scope for modem performance adjustment.
Two independant clock generator systems are provided, one synchronized on the Tx rate and the other on the Rx rate.
In External Clock Mode, external oversampling clocks can be provided to the chip.
Two independant synchronous serial interfaces (SSI) allow several versatile ways of communicating with standard DSPs.
To save power, e.g. in lap-top modem applications, the lowpower reset mode can be used to reduce the power consumption to less than 5mW.



PLCC44
(Plastic Chip Carrier)
ORDER CODE : ST7544CFN



TQFP44
(Plastic Quad Flat Pack)
ORDER CODE : ST7544CQFP

TABLE OF CONTENTS

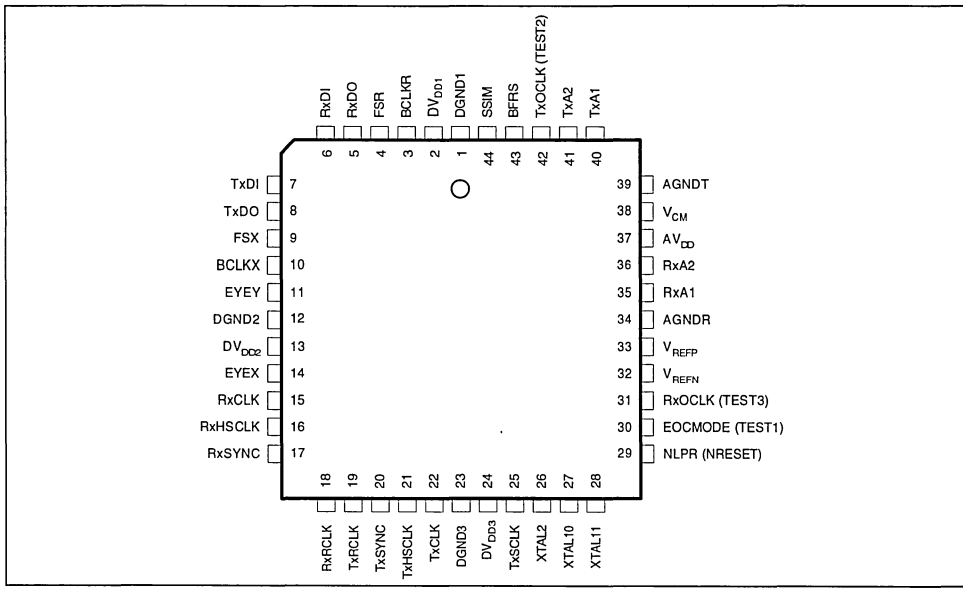
TABLE OF CONTENTS (continued) **Document page**

TABLE OF CONTENTS (continued) **Document page**

I - PIN DESCRIPTION

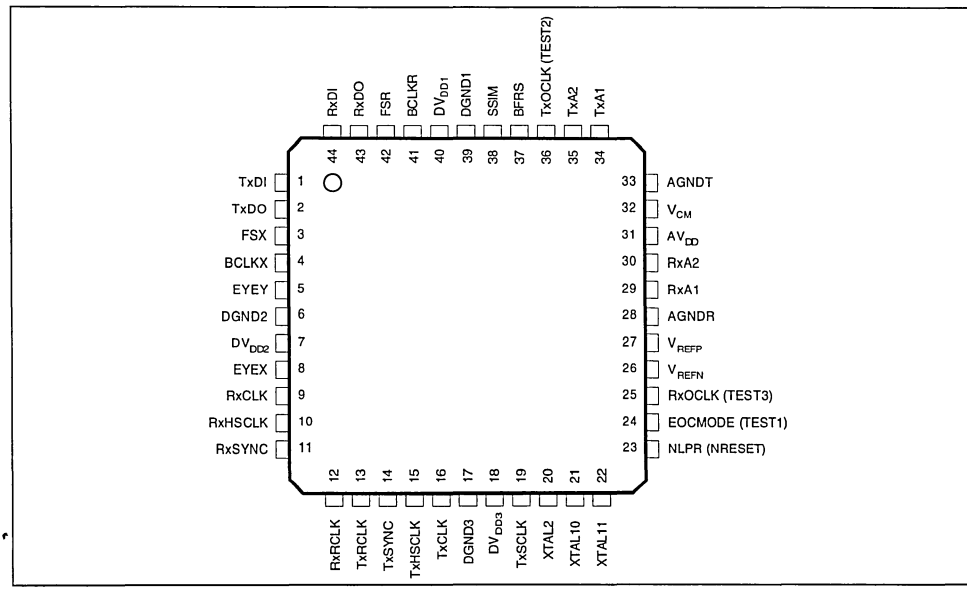
I.1 - PIN CONNECTIONS (Top View)

PLCC44



7544-01.EPS

TQFP44



7544-01.EPS

Note : The pin names in the parenthesis are the corresponding for the ST7543.

I - PIN DESCRIPTION (continued)

I.2 - PIN LIST

PQFP	PLCC	NAME	DESCRIPTION
39	1	DGND1	Digital Ground (0V)
40	2	DV_{DD1}	Positive Digital Power Supply. (+5V±5%)
41	3	BCLKR	Receive bit Clock Output
42	4	FSR	Receive Frame Synchronization Output
43	5	RxDO	Receive Serial Data Output
44	6	RxDI	Receive Serial Data Input
1	7	TxDI	Transmit Serial Data Input
2	8	TxDO	Transmit Serial Data Output
3	9	FSX	Transmit Frame Synchronization Output
4	10	BCLKX	Transmit Bit Clock Output
5	11	EYEY	8 bit YD/AC Output for Eye Pattern display
6	12	DGND2	Digital Ground (0V)
7	13	DV_{DD2}	Positive Digital Power Supply. (+5V±5%)
8	14	EYEX	8bit XD/AC Output for Eye Pattern display
9	15	RxCLK	Receive Bit Rate Clock Output
10	16	RxHSCLK	Receive Highest Clock Output
11	17	RxSYNC	Receive Synchronization Pulse Output
12	18	RxRCLK	Receive Baud Rate Clock Output
13	19	TxRCLK	Transmit Baud Rate Clock Output
14	20	TxSYNC	Transmit Synchronous Pulse Output
15	21	TxHSCLK	Transmit Highest Clock Output
16	22	TxCLK	Transmit Bit Rate Clock Output
17	23	DGND3	Digital Ground (0V)
18	24	DV_{DD3}	Positive Digital Power Supply. (+5V±5%)
19	25	TxSCLK	Transmit Synchronization Clock Input
20	26	XTAL2	Crystal Output
21	27	XTAL10	External Clock/Crystal Input 1
22	28	XTAL11	External Clock/Crystal Input 2
23	29	NLPR	Low Power Reset Input
24	30	EOCMODE (TEST1)	External Oversampling Clock Mode Input. Must be tied to DGND in either the ST7544 normal mode or the 7543 mode.
25	31	RxOCLK (TEST3)	Receive Oversampling Clock Input. Output high-impedance in normal mode.
26	32	V_{REFN}	16 bit D/AC and A/DC Negative Reference Voltage
27	33	V_{REFP}	16 bit D/AC and A/DC Positive Reference Voltage
28	34	AGNDR	Analog Ground (0V)
29	35	RxA1	Receive Positive Analog Input
30	36	RxA2	Receive Negative Analog Input
31	37	AV_{DD}	Positive Analog Power Supply (+5V±5%)
32	38	V_{CM}	Common Mode Voltage Input (2.5V ±10%)
33	39	AGNDT	Analog ground (0V)
34	40	TxA1	Smoothing filter positive Output
35	41	TxA2	Smoothing filter negative Output
36	42	TxOCLK (TEST2)	Transmit Oversampling Clock Input. Output high-impedance in normal mode.
37	43	BFRS	Bit Frame Rate Select Input
38	44	SSIM	Serial Synchronous Interface Mode Input

Note : The pin names in brackets are the corresponding names for the ST7543.

I - PIN DESCRIPTION (continued)

I.3 - PIN FUNCTION

I.3.1 - Power Supply (9 Pins)

Analog V_{DD} Supply (AV_{DD})
This pin is the positive analog power supply (+5V±5%) for the Transmit and the Receive sections. It is not internally connected to digital V_{DD} supply (DV_{DD1-3}).

Digital V_{DD} Supply (DV_{DD1},DV_{DD2},DV_{DD3})
These pins are the positive digital power supply (+5V±5%) for Transmit and Receive digital internal circuitry.

Analog Ground (AGNDT,AGNDR)
These pins are the analog ground return of the analog Transmit (Receive) section.

Digital Ground (DGND1,DGND2,DGND3)
These pins are the ground connections for Transmit and Receive internal digital circuitry.

Note 1 : To obtain published performance, the analog V_{DD} and Digital V_{DD} should be decoupled with respect to AGND and DGND, respectively. The decoupling is intended to isolate digital noise from the analog section; decoupling capacitors should be as close as possible to the respective analog and digital supply pins.

Note 2 : All the ground pins must be tied together. In the following section, the ground and supply pins are refered to as GND and V_{DD}, respectively.

I.3.2 - Clock and Control Signals (16 Pins)

External Clock/Crystal Inputs (XTAL10,XTAL11)
XTAL10 and XTAL11 inputs must be tied to external crystal(s) or external clock(s). These inputs are selected from the TxCtrl register. The maximum clock rate is 38MHz. XTAL10 is the default External Clock/Crystal input. It is mandatory to shortcircuit XTAL10 and XTAL11 when a single external crystal or clock generator is used. The nominal master clock frequency is 36.864MHz (this frequency and the frequency 25.8048MHz are well suited for the V.Fast application) but the onchip amplifier is designed for a parrallel crystal oscillator with a frequency equal to 18.432MHz. The other master clocks frequencies (18.432MHz, 25.8048MHz and 29.4912MHz) are well suited for the well known CCITT recommendations (V.21 through V.32bis).

Crystal Outputs (XTAL2)
This output is to be tied to one or two external crystals (see Figure 1). If an external clock is used, XTAL2 should be left open circuit.

Low power and Reset Input (NLPR)
This pin , when low, synchronizes the ST7544 clock system and puts it in low power mode. NLPR pin must be tied to V_{DD} during normal operation. Access to the chip is disabled during power-on reset until the clock oscillator starts. The reset time duration can be increased by connecting the NLPR input to an external RC network (see Figure 9). The Low-Power Reset Mode is actived when this pin is tied to GND (Operation of all clocks and the analog section is stopped).

Transmit Synchronization Clock Input (TxSCLK)
This pin can be connected to an external terminal clock to phase-lock to the internal transmit clocks. It can be disabled under software control to allow the Tx DPLL to free run or phase lock to on the Rx clock system.

Transmit Bit Rate Clock Output (TxCLK)
This pin outputs the synchronous transmit bit clock selected for the MODEM.

Transmit Baud Rate Clock Output (TxRCLK)
This pin, when the bit D4 within receive register RxCR3 is set to 0, outputs the synchronous transmit baud rate clock (initial state). When bit D4 is set to 1 this pin outputs the frequency comparison signal FCOMP (used by the TxDPLL in both 7543 mode and V.Fast synchronization).

Transmit Synchronization Pulse Output (TxSYNC)
This pin outputs the synchronization transmit reset pulse when a soft reset is applied to the ST7544. Combined with TxHSCLK clock it can be used to externally provide any synchronous transmit clock.

Transmit Highest Clock Output (TxHSCLK)
This pin outputs the highest synchronous transmit clock to provide any external or multiplexing clock.

Transmit Oversampling Clock input (TxOCLK)
This input can be connected to an external clock to provide the chip with the over-sampling clock, depending on the External Over sampling Mode input (EOCMODE). In normal mode this pin should be static (tied to GND or V_{DD}).

Receive Bit Rate Clock Output (RxCLK)
This pin outputs the synchronous receive bit clock selected for the MODEM.

Receive Baud Rate Clock Output (RxRCLK)
This pin outputs the synchronous Receive baud rate clock.

Receive Synchronization Pulse Output (RxSYNC)
This pin outputs the synchronization receive reset pulse when a soft reset is applied to the ST7544. Combined with RxHSCLK clock it can be used to externally provide any synchronous receive clock.

Receive Highest Clock Output (RxHSCLK)
This pin outputs the highest synchronous receive clock to give any external or multiplexing clock.

I - PIN DESCRIPTION (continued)

Receive Oversampling Clock input (RxOCLK)
This input can be connected to an external clock to provide the chip with the oversampling clock, depending on the External Over sampling Mode input (EOCMODE). In normal mode this pin should be static (tied to GND or V_{DD}).

External Oversampling Clock Mode (EOCMODE)
This pin is used for selecting one of the two possible oversampling modes. When EOCMODE is tied to GND, all the clock are provide internally (mode compatible with the ST7543). When EOCMODE is tied to V_{DD}, the oversampling clocks must be input on TxOCLK and RxOCLK pins. The TxHSCLK (RxHCLK) and TxSync (RxSync) signals along with external fractional divider can be used to provide the oversampling clocks to the ST7544.

I.3.3 - Synchronous Serial Interfaces (SSIA,SSIB) (10 pins)

Serial Synchronous Interface Mode input (SSIM)
This input activates one or both serial interfaces. When SSIM is tied to V_{DD}, both A and B ports are functional : port A (SSIA) is dedicated to the Transmit channel and port B (SSIB) is dedicated to the Receive channel.
When SSIM is tied to GND only port A (SSIA) is selected. In this case SSIA carries both Tx and Rx Signals and EYE pattern.

Bit Frame Rate Select input (BFRS)
This input selects one of the two possible bit frequencies for the BCLKX and BCLKR clocks. When BFRS is tied to V_{DD} the BCLKX (BCLKR) frequencies are 128 (160 (1)) times the FSX (FSR) frequencies. When BFRS is tied to GND, BCLKX (BCLKR) frequencies are 64 (80 (1)) times the FSX (FSR) frequencies.

Frame Synchronization Transmit output (FSX)
This output clock is the Transmit Frame synchronization pulse signal of the SSIA port which has nominal frequency equal to the transmit sampling frequency. This pulse indicates the beginning of the 16-bit serial words on the serial data input/output port A.

Bit Clock Transmit output (BCLKX)
This output pin provides the serial bit clock for the SSI port A. The BCLKX frequency equals 128 (160 (1)) or 64 (80 (1)) times the Transmit sampling frequency, depending on the Bit Frame Select Input (BFRS).

Serial Data Transmit input (TxDI)
This input receives word-oriented serial data. Data is loaded from TxDI into the Transmit Shift Register (TSRIN) on the falling edge of BCLKX and transfered to the Transmit Buffer Register (TBRIN) when a complete 16 bit word has been received. Data is assumed to be received MSB first.

Serial Data Transmit output (TxDO)
This output sends word-oriented serial data. The 16 bit Data Word loaded in the Transmit Buffer Register (TBROUT) is transfered to the Transmit Shift Register (TSROUT) and clocked out of TSROUT on the rising edge of BCLKX. Serial words are transmitted MSB first.

Receive Frame Synchronization output (FSR)
This output clock is the Receive Frame synchronization pulse signal of SSI port B which has frequency equal to the receive sampling frequency. This pulse is used to indicate the beginning of serial words on the serial data input/output port B.

Receive Bit Clock output (BCLKR)
This output pin provides the serial bit clock for the SSI port B. The BCLKR frequency is 128 (160 (1)) times or 64 (80 (1)) times, selected by BFRS) the receive sampling frequency.

Receive Serial Data input (RxDI)
This input receives word-oriented serial data. Data is clocked from RxDI into the Receive Shift Register (RSRIN) on the falling edge of BCLKR and transfered to the Receive Buffer Register (RBRIN) when a complete 16-bit word has been received. Data is assumed to be received MSB first.

Receive Serial Data output (RxDO)
This output sends word-oriented serial data. The 16-bit Data Word loaded in the Receive Buffer Register (RBROUT) is transfered to the Receive Shift Register (RSROUT) and clocked out of RSROUT on the rising edge of BCLKR. Serial words are transmitted MSB first.

Note 1 : The oversampling ratio is selectable using the V divider (Table 40)

I.3.4 - Analog Interface (9 pins)

D/AC and A/DC Positive Reference Voltage output (V_{REFP})
This pin provides the Positive Reference Voltage used by the 16-bit converters. The reference voltage, V_{REF}, is the voltage difference between the V_{REFP} and V_{REFN} outputs, and its nominal value is 2.5V. V_{REFP} should be externally decoupled with respect to V_{CM} (see Figure 17).

D/AC and A/DC Negative Reference Voltage (V_{REFN})
This pin provides the Negative Reference Voltage used by the 16 bit converters, and should be externally decoupled with respect to V_{CM}.

I - PIN DESCRIPTION (continued)

Common Mode Voltage input (V_{CM})
This input pin is the common mode Voltage (AV_{DD}-AGND)/2 that should be externally provided. This input must be decoupled with respect to GND.

Smoothing filter positive Output (TxA1)
This pin is the positive output of the fully differential analog smoothing filter.

Smoothing filter negative Output (TxA2)
This pin is the negative output of the fully differential analog smoothing filter. Outputs TxA1 and TxA2 provide analog signals with maximum peak to peak amplitude 2 x V_{REF}, and must be followed by an external continuous time two pole smoothing filter (see Figure 16) (1). The external filter follows the internal single pole switch capacitor filter (see section V.2.2). The cutoff frequency of the external filter must be greater than two times the transmit sampling frequency (Fsx), so that the combined frequency response of both the internal and external filters is flat in the pass band.

Receive Positive Analog Input (RxA1)
This pin is the differential positive A/DC Input.

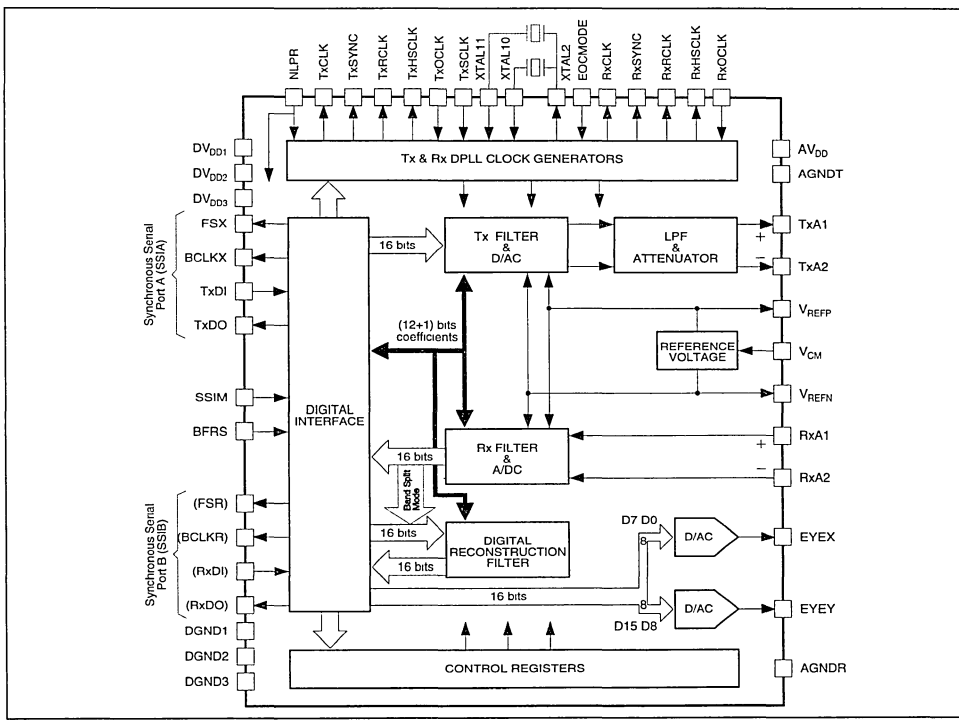
Receive Negative Analog Input (RxA2)
This pin is the differential negative A/DC Input.
These analog inputs (RxA1,RxA2) are presented to the SigmaDelta modulator, the analog input peak to peak signal range must be less than 2 x V_{REF}, and must be preceded by an external continuous-time single pole anti-aliasing filter (see Figure 16). The cut-off frequency of the filter must be lower than one half the transmit over-sampling frequency (TxOSCK). These filters should be set as close as possible to the RxA1 (RxA2) pins.

D/AC output for Eye Pattern (EYEX,EYEY)
These pins are the outputs of two 8-bit digital to analog converters used to monitor, on a CRT, the X and Y quadrature signals of the eye pattern of the demodulated signal.

Note 1 : The smoothing filter order depends of the acceptable transmit signal spectrum on the line

II - BLOCK DIAGRAM

Figure 1 : General Block Diagram

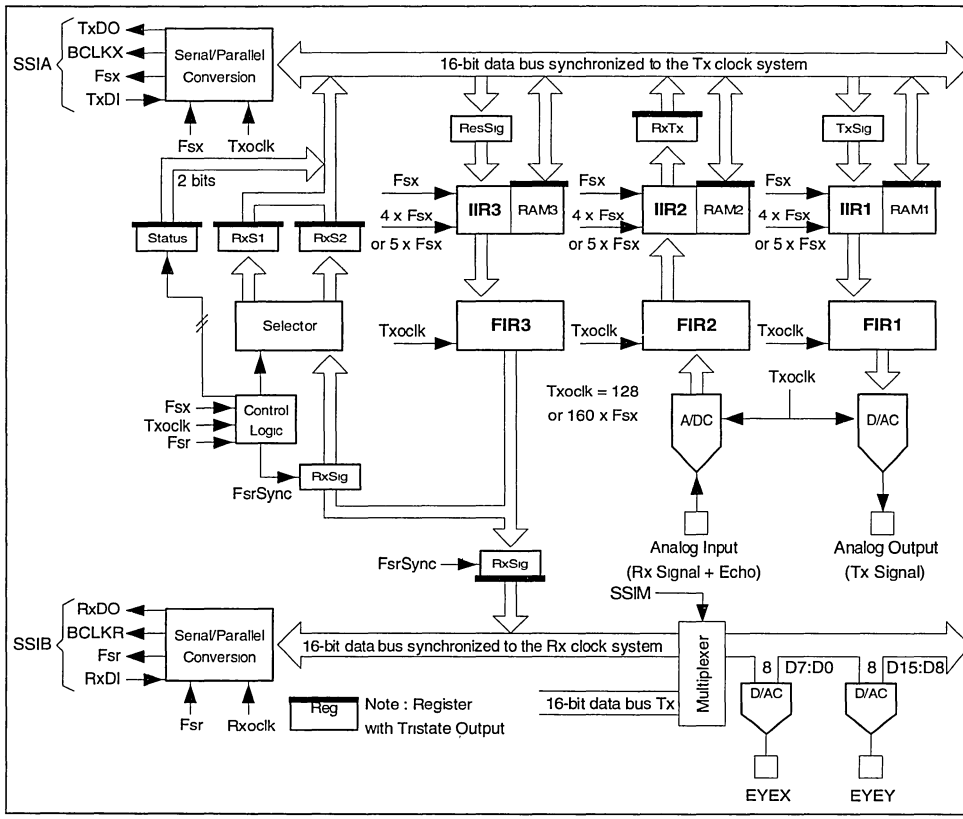


III - FUNCTIONAL DESCRIPTION

III.1 - SIGNAL TRANSFER BLOCK DIAGRAM

The ST7544 Block Diagram illustrates three paths as follows : The Transmit D/A Section, the Receive A/D section and the Receive Reconstruction section.

Figure 2 : Signal Transfer Block Diagram



III - FUNCTIONAL DESCRIPTION (continued)

III.2 - TRANSMIT D/A SECTION

The functions included in the Tx D/A section are detailed hereafter.

III.2.1 - Interpolation Filters

The oversampling is performed by two cascaded digital interpolating filters : IIR1 and FIR1. Two oversampling frequency are available. The IIR1 and FIR1 filters are sampled at 4 x Fsx and 128 x Fsx (5 x Fsx and 160 x Fsx), respectively.

III.2.1.1 - Programmable Interpolation Filter (IIR1)

IIR1 is an infinite impulse response interpolating filter.

The purpose of this digital filter is to interpolate 4-times (5times) the digital signal coming from the DSP. This filter is sampled at 4-times (5times) the basic sampling frequency, e.g. 9600 x 4 Hz (9600 x 5 Hz), and must exhibit, as a minimum, a low-pass section which is mandatory to remove replicas above half the sampling frequency (e.g. 4800Hz) (see Figure 13).

The digital samples are encoded in 16-bit two's complement format.

The IIR1 filter is a cascade of seven biquads (see Figure A1). The filter coefficients are loaded into the associated RAM (38 x 13). Each coefficient is coded into 12bits and can be doubled by virtue of an extra bit. All 38 coefficients have to be loaded to implement an IIR transfer function (see Annexe A).

This filter has been made programmable to offer each user the possibility to add filtering characteristics, e.g. high-pass section or equalization, matched to a particular application.

III.2.1.2 - FIR Filter (FIR1)

FIR1 is a finite impulse response interpolating filter. Its input sampling frequency is 4 x Fsx (or 5 x Fsx) and its interpolation ratio is 32. The Z transfer function of this FIR is :

$$H(z) = \left(\frac{1 - z^{-32}}{32\,(1 - z^{-1})} \right)^3$$

with Z = exp (j2πF/Txoclk)
and Txoclk = 128 (160) x Fsx

III.2.2 - D/A Converter

The 128-times (160times) oversampled D/A converter includes a second order digital noise shaper, a one bit D/A converter and a single pole analog low-pass filter. The gain of the last output stage can be programmed to 0dB,-6dB or infinite attenuation. The cut-off frequency of the single pole switch-capacitor low-pass filter is :

$$fc\text{-}3dB = Txoclk / (2 \times \pi \times 10)$$

where Txoclk = 128 (160) x Fsx

Continuous-time filtering of the analog differential output is necessary using an off-chip amplifier and a few external passive components (see Figure 16).

At least 86dB signal to noise plus distortion ratio can be obtained in the frequency band 300-3400Hz, with a -6dBr output signal.

III.3 - RECEIVE A/D SECTION

The different functions included in the Rx A/D section are detailed hereafter. The format used at the digital interfaces of the Rx channel is two's complement encoded 16-bit.

III.3.1 - A/D Converter

The 128 (160) oversampled A/D converter is based on a second order sigma-delta modulator. The signal to noise plus distortion ratio obtained for a signal spectrum limited to the 300-3400Hz telephone band, is typically 86dB with a -6dBr input signal.

III.3.2 - Decimation Filters

The 128 (160) decimation is performed by two interpolating digital filters : FIR2 and IIR2, which are sampled at 128 x Fsx and 4 x Fsx (160 x Fsx and 5 x Fsx), respectively .

III.3.2.1 - FIR Filter (FIR2)

FIR2 is a finite impulse response decimating filter. Its sampling frequency is 128 x Fsx (or 160 x Fsx) and its decimation ratio is 32. The Z transfer function of this FIR is :

$$H(z) = \left(\frac{1 - z^{-32}}{32\,(1 - z^{-1})} \right)^3$$

with Z = exp (j2πF/Txoclk)
and Txoclk = 128 (160) x Fsx

III - FUNCTIONAL DESCRIPTION (continued)

III.3.2.2 - Programmable Decimation Filter (IIR2)

IIR2 is an infinite impulse response filter. It provides the low-pass filtering needed to remove the noise remaining above half the sampling frequency (e.g. 4800Hz) (see Figure 14). The output of the IIR2, RxTx, will be processed by the DSP. In "band split" mode (see Table 21), RxTx becomes the input signal to IIR3. The RxTx will always be available on serial interface (SSIA in Figure 2).

The IIR2 filter is a cascade of seven biquads. The filter coefficients are loaded into the associated RAM (38 x 13).

The filter transfer function has been made programmable in order to meet specific requirements. The sampling frequency is 4-times (5-times) the down-sampling frequency selected for the Tx section (e.g. 9600 x 4Hz or 9600 x 5Hz).

To support echo cancelling applications the clocks used for the A/D converter and the decimation filters are synchronized on the Tx system clock, i.e. on the Tx rate. It must be pointed out that using a single clock system in A/D and D/A conversions is important for reducing induced noise.

The 12+1 bit filter coefficients are loaded into the internal RAM2 and must be loaded from the serial bus. All 38 coefficients have to be loaded to implement an IIR transfer function.

III.3.3 - Eye-diagram Display

Two 8-bit digital to analog converters are provided to monitor, on a CRT, the X and Y quadrature signals of the eye pattern related to the demodulated signal. The format of the data input is MSB first, 8-bit two's complement, and most significant byte for EYEY sample and least significant byte for the EYEX sample. The reference voltage of these two converters is the power supply voltage V_{DD}. The EYE pattern can be monitored on one or two Synchronous Serial Interface mode.

III.4 - RECEIVE RECONSTRUCTION SECTION

As the Rx channel sampling is synchronized to the Tx system clock, it is necessary to reconstruct the Rx signal in order to get samples synchronized to the Rx symbol rate recovered in the demodulator. The function of the reconstruction filter (IIR3 and FIR3) is to oversample by 128 x Fsx (160 x Fsx) the receive signal (ResSig) comming from the DSP after echo cancellation. The oversampled signal is then down-sampled at Fsr rate to make it available to the DSP as RxSig at SSIB or RxS1/RxS2 at SSIA (see section IV.1 and IV.2). The down sampling process does not introduce significant error.

The transfer function of the first section of the reconstruction filter is programmable in the same way as the Tx and Rx IIR filters previously described.

III.4.1 - Programmable Interpolation Filter (IIR3)

IIR3 is an infinite impulse response interpolating filter.

The purpose of this digital filter is to interpolate 4-times (5-times) the digital signal from the DSP. This filter is sampled at 4-times (5-times) the basic sampling frequency, e.g. 9600 x 4 Hz (9600 x 5 Hz).

The digital samples are encoded in 16-bit two's complement format.

The IIR3 filter is a cascade of seven biquads. The filter coefficients are loaded into the associated RAM (38 x 13). Each coefficient is coded into 12 bits and can be doubled by virtue of an extra bit. All 38 coefficients have to be loaded to implement an IIR transfer function.

This filter has been made programmable to offer each user the possibility to add filtering characteristics, e.g. highpass section or equalization, matched to a particular application.

For example, in a band-split MODEM application, the first section can be a wide channel band-pass filter (allowing the DSP to supervise boundary audio tones) and the second section can be dedicated to high band and low band splitting.

III.4.2 - FIR Filter (FIR3)

FIR3 is a finite impulse response interpolating filter. Its input sampling frequency is 4 x Fsx (5 x Fsx) and the interpolation ratio is 32. The Z transfer function of this FIR is :

$$H(z) = \left(\frac{1 - z^{-32}}{32\,(1 - z^{-1})} \right)^3$$

with $Z = \exp(j2\pi F/Txoclk)$
and $Txoclk = 128\ (160) \times Fsx$

III - FUNCTIONAL DESCRIPTION (continued)

III.5 - CLOCK GENERATION

Master clock is obtained from either a crystal tied between pins XTAL10 (or XTAL11) and XTAL2 or from an external signal connected to the XTAL10 (or XTAL11) pin, in the latter case, the XTAL2 pin should be left open circuit.

Two external crystals (or two external master clock signals), software selectable one at a time, can be used to cope with complex applications. It is mandatory to shortcircuit XTAL10 and XTAL11 when a single external crystal or clock generator is used

To insure the start-up of the ST7544, the XTAL10 input must always be tied to a crystal or an external clock signal, as that pin is automatically selected when powering-on the device.

The different transmit (Tx) and Receive (Rx) clocks are obtained by master clock frequency division in several programmable counters. The Tx and Rx clocks can be synchronized on external signals by performing phase shifts in the frequency division process (equivalent to adding or suppressing master clock transitions at the counter inputs). Two independant digital phase locked loops (DPLL) are implemented using this principle , one for Tx and one for Rx.

Two clock modes are available, selected by the External Oversampling Clock Mode input pin (EOCMODE). When the EOCMODE pin is tied to the GND the internal clock mode is selected. In this mode all the clock are generated internally. When the EOCMODE pin is tied to V_{DD}, the External Oversampling Clock Mode is selected.

In the latter case, the user must provide the chip with the oversampling frequency knowing the interpolation and the decimation ratios selected in the TxCR3 and RxCR3 register. The oversampling clock can be provided by an external clock system. It can also be provided from the highest synchronous clock (TxHSCLK and RxHSCLK) using an external divider. In any case, the user will have to comply with the relation : Crystal frequency FQ must be greater than 470 x 4 x Fsx with an oversampling ratio of 128 or than 470 x 5 x Fsx with an oversampling ratio of 160.

Several values can be chosen for the master clock frequency. The four frequencies given in table 1 are of particular interest, as they are compatible with standard Modem frequencies.

Note : In the remainder of the datasheet, unless otherwise indicated, 36.864MHz will be considered as the nominal master clock frequency. The maximum master clock frequency is 38MHz.

Table 1 : List of usual frequency available

Crystal Frequency	Symbol Rate Frequency	Bit Rate (bps)		Sampling (bps)
FQ (MHz)	Fbaud (baud)	All up to 19200	others	Fsx, Fsr (Hz) (1)
18.432 (2)	600, 1200, 1600, 2400	Yes		3,4,5,6,8,12 or 16 times Fbaud
25.8048	600, 1200, 1600, 2400, 2800	Yes	19600/22400	3,4,5,6,8,12 or 16 times Fbaud
29.4912 (2)	600, 1200, 1600, 2400	Yes		3,4,5,6,8,12 or 16 times Fbaud
36.864 (3)	600, 1200, 1600, 2400, 2560, 2743, 2954, 3000, 3200, 3429, 3491	All up to 28800		3,4,5,6,8,12 or 16 times Fbaud

Notes : 1. Depending on the symbol rate frequency
2. 7543 mode
3. This crystal frequency provides all the symbol rates satisfying the relation :
Symbol rate = (2400 x 16)/K with K = (16, 15, 14, 13, 12, 11)
Symbol rate = (2400 x 8)/K with K = (8, 7, 6)
Symbol rate = (2400 x 10)/K with K = (8, 7)

III - FUNCTIONAL DESCRIPTION (continued)

III.5.1 - Transmit DPLL

Frequency control of the Tx clock system (Figure 10) is obtained by performing additional up or down counting steps in the three input dividers M, N and P. These elementary phase shifts of one master clock period are repeated at either the rate of the Fsx clock, or half that rate, depending on the required capture and tracking ranges (see table 15 and 26). The average updated frequency then varies between the following limits :

$$FQ - FSHIFT \leq Faverage \leq FQ + FSHIFT$$

Where FQ is the master clock frequency and FSHIFT equals Fsx or Fsx/2 (see table 26).

The TxDPLL phase comparison which determines lead or lag decisions, is simply obtained by sampling the synchronization clock, TxSCLK or RxCLK, on the falling edges of an internal clock taken from the division chain, FCOMP (see table 25). FCOMP frequency must be an integer submultiple of the synchronization clock. This frequency determines the Tx jitter magnitude. In V.Fast synchronization mode FCOMP is equal to 2400Hz, and in 7543 mode the synchronization clock FCOMP can be chosen to be equal to the baud rate frequency. Only phase shifts of the same sense (lead or lag) are performed during each FCOMP period. The actual phase shifts during FCOMP period are given by the ratio

FSHIFT/FCOMP

These phase shifts are performed at the inputs of the M,N, and P dividers to lock the DPLL to the synchronisation signal (see Table 22). The Tx clock system may also run freely without any phase shift. In this case, the TxSCLK input is no longer active.

The DPLL capture and tracking range equals ±FSHIFT/FQ. They have to be greater than ± 200ppm to comply with CCITT recommendations. FSHIFT = Fsx/2 minimizes the jitter. Because of this, there is a trade-off between higher capture and tracking ranges and lower jitter.

Ex : FQ = 36.864MHz and FSHIFT = 9600Hz.

Capture and tracking range = ± FSHIFT/FQ
= ± 9600Hz/36.864MHz = ± 260ppm

III.5.2. Transmit Clocks

III.5.2.1 - Internal Mode

The internal clock mode is selected when the pin EOCMODE is tied to GND. In this mode the ST7544 provides three Tx programmable synchronous modem clocks :

- a transmit bit rate clock TxCLK
- a transmit baud rate clock TxRCLK
- a transmit highest synchronous clock TxHSCLK, associated with the TxSYNC synchronization pulse, useful to generate additional clocks (e.g. extra divisors) if needed.

The outputs of the latter two clocks, can be disabled when not used, but in 7543 synchronisation mode a correct baud rate frequency must be programmed as the FCOMP clock frequency depends on it.

The Tx clock system provides the sampling and oversampling clocks as well as the bit and synchro clocks (BCLKX and FSX) used by the serial interface A (SSI-A) described in section IV.

The counters of the Tx clock system (Figure 10) are automatically reset when powering-on the ST7544 and when the NLPR input level is low. They can also be reset, under software control, during the following conditions :

- on the next falling edge of the TxSCLK terminal clock or of the RxCLK receive bit rate clock (SST bit table 22).
- on the next falling edge of the TxRCLK transmit baud rate clock when any Tx register is accessed.

The former gives the capability to speed-up the Tx DPLL synchronization; the latter is useful to fix the phase of the bit rate clock with respect to the baud rate clock, in particular after each modification of the bit or baud rate value.

The internally generated pulse resetting the Tx counters is output at the TxSYNC pin in order to synchronize external functions using the TxHSCLK clock.

III.5.2.2 - External Mode

The external clock mode is selected when the pin EOCMODE is tied to the V_{DD}. In this mode the user must provide the ST7544 with the transmit oversampling clock. The internal DPLL can be used if the external transmit oversampling clock is generated by a divider synchronized by both the TxHSCLK and TxSync signals.

III - FUNCTIONAL DESCRIPTION (continued)

III.5.3 - Receive DPLL

The synchronization of the Rx counters delivering the Rx clocks (Figure 11) is performed by addition or suppression of master clock periods under DSP control. In this case, the phase comparison function of the RxDPLL is implemented in the associated DSP recovering the received symbols.
Two types of phase shift control are provided in the ST7544 :

- a coarse phase lag of programmable magnitude, obtained from the suppression of 64 to 4096 successive master clock transitions. This control is to be used to reduce the RxDPLL locking time.
- a fine phase lead or lag of programmable magnitude (i.e. 8 to 32 master clock periods or one Tx oversampling clock period) continuously used to implement the phase control loop. (see Table 38). Each elementary phase shift, corresponding to an addition or a subtraction of one master clock transition, is synchronized on an internal clock with frequency equal to the Rxoclk (128 or 160 times the Rx sampling frequency Fsr). A phase shift is ,therefore, always completed in less than one Fsr period.

III.5.4 - Receive Clocks

III.5.4.1- Internal Mode

The internal clock mode is selected when the pin EOCMODE is tied to GND. In this mode the ST7544 provides three Rx synchronous programmable modem clocks :

- receive bit rate clock RxCLK
- receive baud-rate clock RxRCLK
- receive highest synchronous clock, RxHSCLK associated with the RxSYNC synchronization pulse useful to generate additional clocks

The RxRCLK and RxHSCLK outputs can be disabled when not used. The bit rate clock frequency of the Rx modem can be chosen to be different from its Tx counterpart, provided Rx to Tx loopback is not required. The Rx clock system also provides the Rx sampling clock as well as the bit and synchro clocks (BCLKR and FSR) used by the serial interface B (SSI-B) described in section IV. The digital reconstruction filter implemented in the ST7544 makes possible the choice of a receive nominal sampling frequency different from the transmit nominal sampling frequency. The counters of the Rx clock system (Figure 11) are reset when powering on the ST7544 and when the NLPR input level is low. They can also be reset, under software control, on the next falling edge of the RxRCLK receive baud rate clock when the RxCR0 or RxCR1 register are accessed : this feature is used to fix the phase of the bit rate clock with respect to the baud rate clock, e.g. after each modification of the bit or baud rate value. The internally generated pulse resetting the Rx counters is output at the RxSYNC pin in order to be used with the RxHSCLK clock.

III.5.4.2 - External Mode

The external clock mode is selected when the pin EOCMODE is tied the V_{DD}. In this mode the user must provide the ST7544 with the receive oversampling clock. The internal DPLL can be used if the external receive oversampling clock is generated by a divider synchronized by both the RxHSCLK and RxSync signals.

III.6 - SERIAL INPUT/OUTPUT SYNCHRONOUS INTERFACES

The MAFE has two Synchronous Serial Interfaces ports, SSIA and SSIB. They allow independent transmit and receive paths. Through the two serial ports, the MAFE can talk to various digital signal processors. The various serial interface signals and internal registers are given below :

SSI PORT A (SSIA)

- Transmit Frame Synchronization output (FSX)
- Transmit Bit clock output (BCLKX)
- Transmit Serial Data input (TxDI)
- Transmit input Shift Register (TSRIN)
- Transmit input Buffer Register (TBRIN)
- Transmit output Shift Register (TSROUT)
- Transmit Serial Data output (TxDO)

SSI PORT B (SSIB)

- Receive Frame Synchronization output (FSR)
- Receive Bit clock output (BCLKR)
- Receive Serial Data input (RxDI)
- Receive input Shift Register (RSRIN)
- Receive input Buffer Register (RBRIN)
- Receive output Shift Register (RSROUT)
- Receive Serial Data output (RxDO)

INPUT MODES

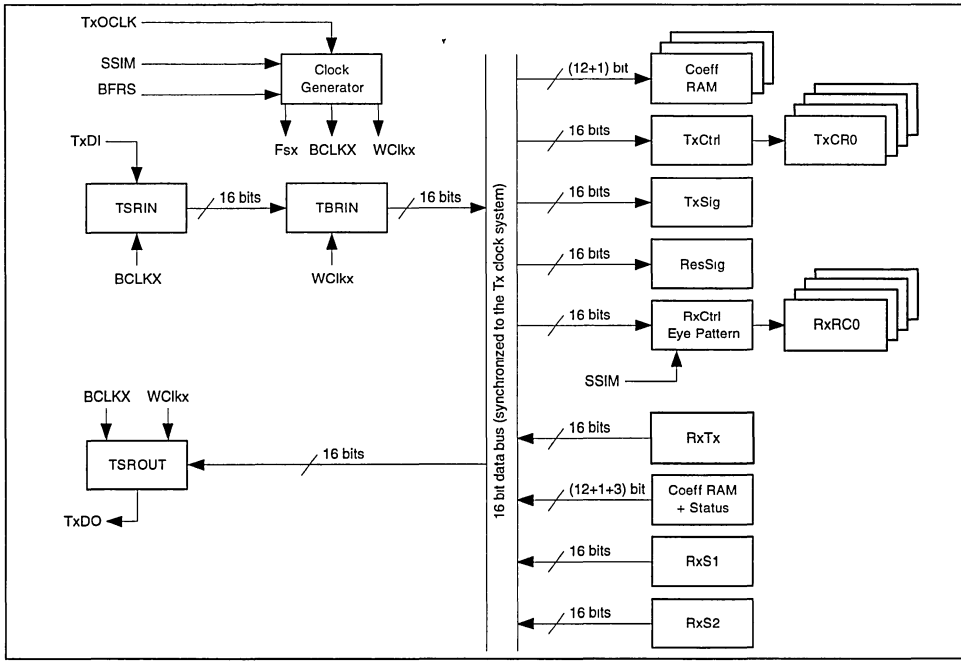
- Synchronous Serial Interface Mode (SSIM)
- Bit Frame Rate Select (BFRS)

With SSIM input, the user can choose either single interface mode or dual interface mode. In single interface mode (section VI.2), only port SSIA is operational. Where as in dual interface mode (section VI.1), both SSIA and SSIB ports are operational. These two ports carry data inside a synchronous frame consisting of four/five or eight/ten sixteen bit time slots (only the four first time slots are used for transporting information. SSIA port is synchronous to the Tx system clock and SSIB port is synchronous to Rx system clock. The format of the signal samples carried on these port is two's complement with MSB sent or received first. As explained hereafter it is also possible to use the port A only to transfer the data between the ST7544 and the associated DSP.

III - FUNCTIONAL DESCRIPTION (continued)

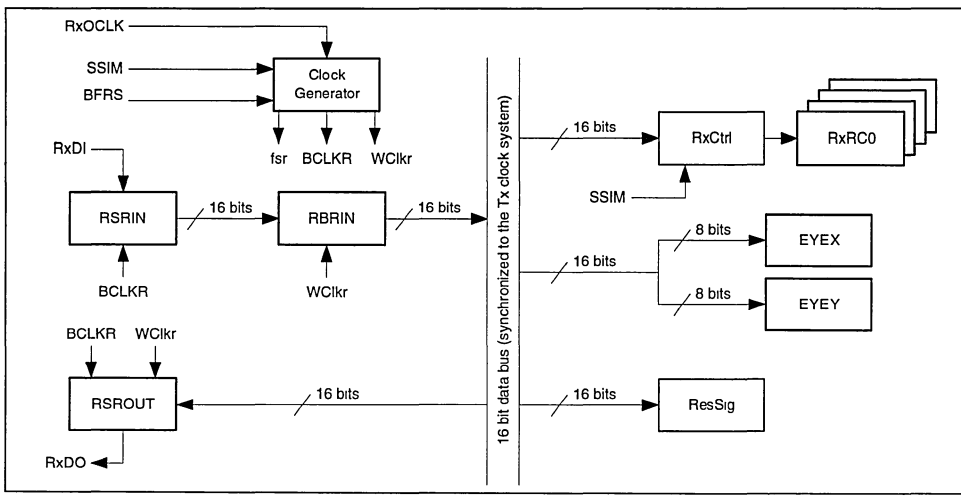
III.6.1 - Tx Clock Related Registers

Figure 3 : Tx Clocks Related Registers



III.6.2 - Rx Clock Related Registers

Figure 4 : Rx Clocks Related Registers



IV - SERIAL INTERFACE OPERATION

Serial data transmission (reception) is initiated by a frame synchro signal FSX (FSR). The Data is clocked from TxDI (RxDI) into TSRIN (RSRIN) on the falling edge of BCLKX (BCLKR) and transfered to the TBRIN (RBRIN) register when a complete 16 bit word has been received. Data is assumed to be received MSB first.

Serial data transmission (reception) output is initiated by a frame synchro signal FSX (FSR). The 16-bit Data word is loaded into TSROUT (RSROUT) and serially clocked out of TSROUT (RSROUT) to TxDO (RxDO) on the rising edge of BCLKX (BCLKR).

BCLKX (BCLKR) frequency can be programmed to be either 64 or 128 (80 or 160) times Fsx (Fsr) using the Bit Frame Select (BFRS) input pin. This mean that the frame contains four, five, eight or ten time slots of 16 bits. The time slots used for circuit operation are indicated in the next paragraph.

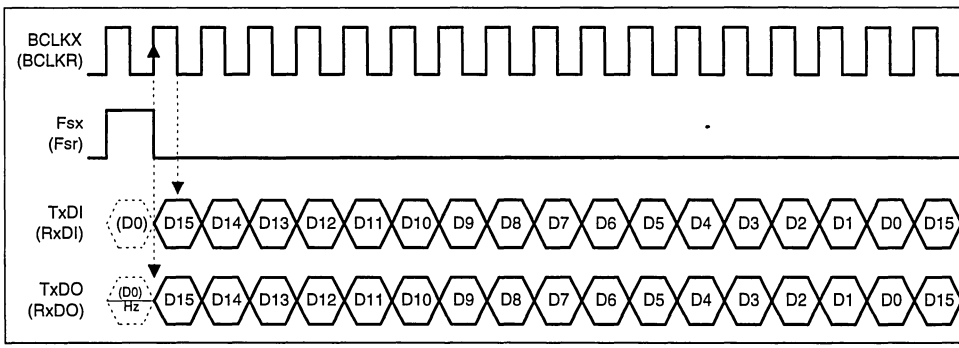
IV.1 - DUAL SERIAL INTERFACE MODE (SSIA, SSIB)

When SSIM is tied to V_{DD}, both A and B ports are functional : port A (SSIA) is dedicated to the Tx channel and port B (SSIB) to the Rx channel. The timing diagram showing the data format is given in Figures 5 and 6.

The time-slot TXO1 is dedicated to RAM coefficient reading. The RAM coefficient is selected by the address bits RA0 to RA1 in the TxCtrl word (see Table 4). Reading is initiated by the rising edge of Start bit Stb (bit D14 in Table 3) in the TxCtrl word.

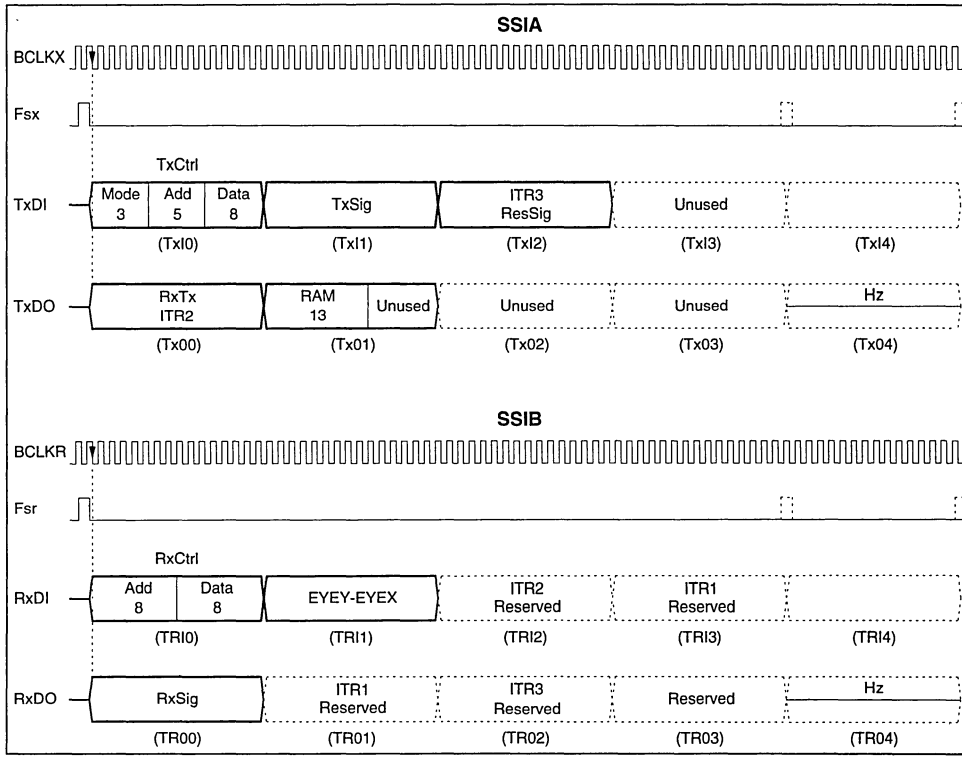
Note : RxSig is also available in two time slot RxS1 and RxS2 on the time slot TxO2 and TxO3 on SSIA (see section IV.2)

Figure 5 : Serial Channel Timing



IV - SERIAL INTERFACE OPERATION (continued)

Figure 6 : Serial Channel Timing. Dual Port Mode



IV.2 - SINGLE SERIAL INTERFACE MODE

When SSIM is tied to GND, only port A (SSIA) is selected. In this case, port A carries both Tx and Rx signal samples and control words at Tx sampling rate (Fsx). The RxDI input should be tied to V_{DD}. Since port B is not functional in this mode, the RxSig (synchronized to Fsr) will be available in the two time slots, RxS1 and RxS2, synchronized to Fsx. The reason for the two time slots is that the Fsr could be different in magnitude and phase from the Fsx. The status bit St0 and St1 are used to indicate which of the RxS1 and RxS2 are valid. Please see the table following. For example, if Fsx = 9600Hz and Fsr = 14400Hz both RxS1 and RxS2 could carry valid data. Figure 7 shows the timing diagram.

The time-slot TXO1 is dedicated to RAM coefficient reading. The RAM coefficient is selected by address bits (RA0 to RA1) in the TxCtrl word (see Table 4). Reading is initiated by the rising edge of a Start bit Stb (bit D14 in Table 3) in the TxCtrl word. The time-slot TxI3 is dedicated to the RxCtrl word or the EYE-PATTERN, selected in the TxCtrl (see table 5).

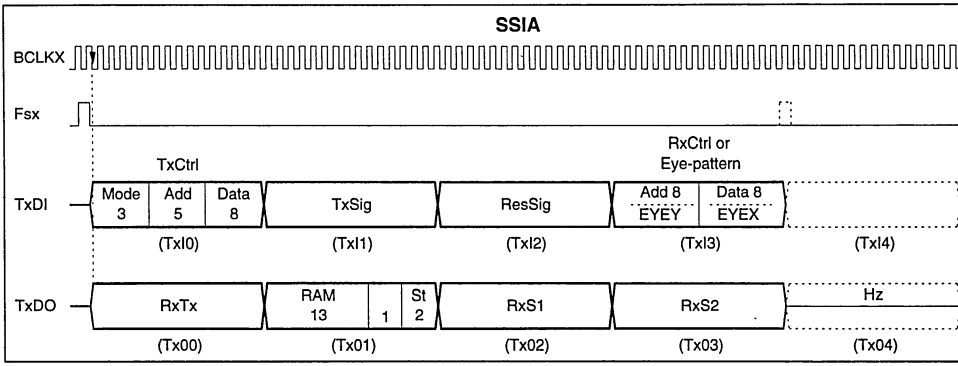
Table 2

STATUS WORD IN TxO1 TIME SLOT		
D1	D0	Valid Data
St1	St0	
0	0	None
0	1	None
1	0	RxS2
1	1	RxS1 and RxS2 (1)

Note 1 : The RxS1 sample precedes the RxS2 sample.

IV - SERIAL INTERFACE OPERATION (continued)

Figure 7 : Serial Channel Timing. Single Port Mode



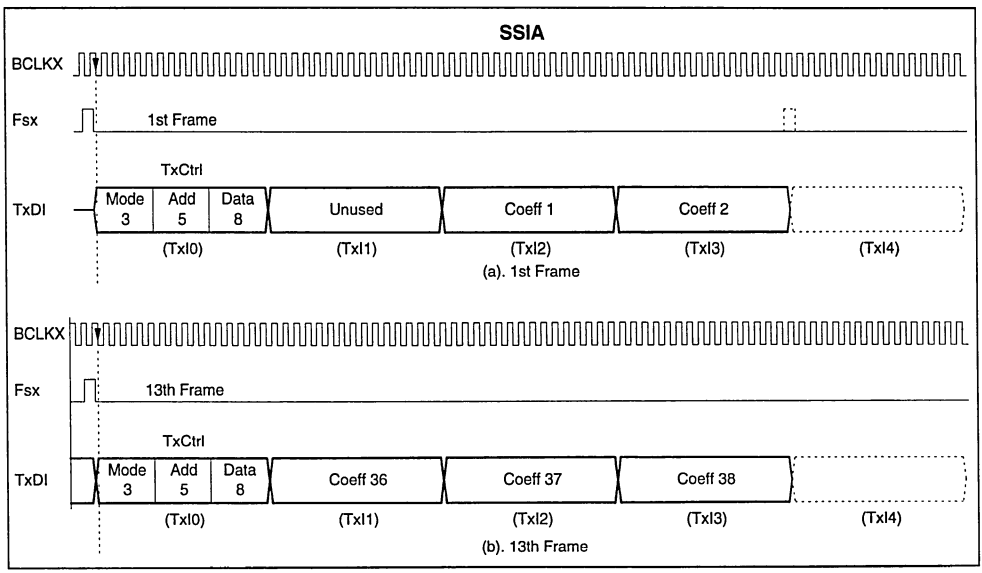
IV.3 - COEFFICIENT LOADING MODE

The Coefficient Loading Mode is selected by the Mode Select bit (MS) in the TxCtrl Word (Table 3). When the MS bit is a logic "1" the loading mode is selected. The IIR RAMS (RAM1 to RAM3) are selected in the TxCtrl word by two address bits (RA0 to RA1). Each coefficient RAM stores 38 coefficients of 13 bits. Therefore the size of the coefficient RAM is 38 x 16 bits. The first frame transfers 2 coefficients and the 12 following frames each transfer 3 coefficients into the selected RAM, as shown in Figure 8. The transfer is initiated by the rising edge of the Start bit coefficient Stb which is loaded into the TxCtrl word. When the coefficient loading mode is selected all data path are fixed to zero.

Notes : 1. Coefficient loading is the same for both dual and single interface modes.

2. In coefficient loading mode , the EYE-PATTERN (time slot TxI3) (and the RxCtrl in a single serial interface) cannot be accessed

Figure 8 : Coefficient Loading Mode



IV - SERIAL INTERFACE OPERATION (continued)

IV.4 - COEFFICIENT READING

Coefficient reading is selected in DATA mode only, i.e. when the Mode Select bit (MS) in the TxCtrl word is tied to logical 0. The IIR RAMS (RAM1 to RAM3) are selected in the TxCtrl word by two address bits (RA0 to RA1). The 38 coeficients of 13 bits are available, one per frame, in the timeslot TxO1 on the output Tx port A (see Figures 6, 7). The reading is available on the rising edge of the Start bit Stb loaded into the TxCtrl word. The first coefficient is output with one frame of delay on TxO1.

IV.5 - CRYSTAL SELECTION (XTAL10, XTAL11)

For application needing different or higher symbol rates, the user can software select different master clock frequencies for the ST7544. Two XTAL inputs are provided for this purpose. The active XTAL input is selected in the time slot TxI1 with the Quartz Select bit (QS). It is mandatory to shortcircuit the XTAL10 and XTAL11 inputs when a single external crystal or clock generator is used.

IV.6 - FRAME FREQUENCY PROGRAMMING

When using the nominal master clock frequency, the frame frequency can be from 7200Hz to 16000Hz (see Tables 15 and 32). Whenever the frame frequency Fsx (Fsr) is modified, the data to the ST7544 during that frame should be high in the time slots TxI1 (RxI1), TxI2 (RxI2) and TxI3 (RxI3). This is because the BCLKX (BCLKR) during that frame may not be correct. Therefore, whenever the Fsx (Fsr) is changed the user has to send information to the ST7544 after one frame delay.

IV.7 - INITIALIZATION AND LOW-POWER RESET MODE

Internal power-on circuitry automatically resets the DPLL, the clock generator counters, and initializes the internal control registers. The clocks affected are the symbol clock, the bit clock and the sampling clock. The initial status of these registers is given in the PROGRAMMABLE FUNCTIONS section. The transmit attenuator is initialized to an infinite attenuation mode (see Table 24) to avoid the transmission of undesirable signals on the phone line.

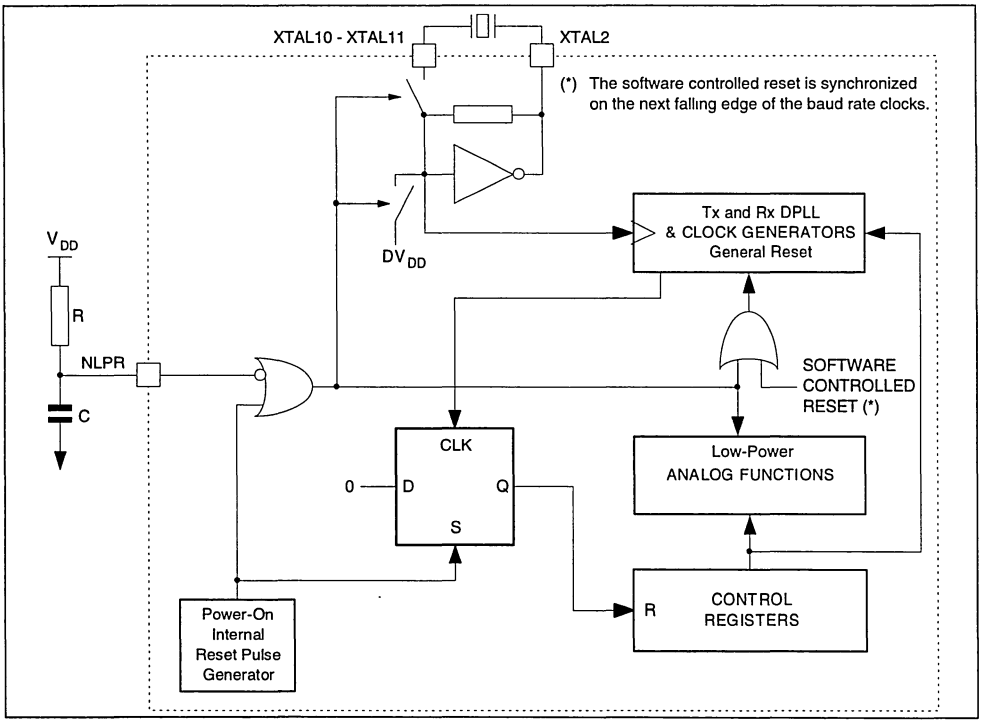
During hardware low power reset (NLPR pin is tied to GND), the input of the inverter (across the crystal) will be high (DV_{DD}), the DPLLs and the clock generator counters are initialized, all the analog circuitry is placed in low-power mode and the XTAL oscillator is stopped.

Access to the circuit is disabled during reset until the clock oscillator starts. The duration of the reset time can be increased by connecting the NLPR input to an external RC timeconstant as indicated in Figure 9.

In normal operation the NLPR input is used to control the LowPower mode. When NLPR is not used, it must be tied to V_{DD}.

IV - SERIAL INTERFACE OPERATION (continued)

Figure 9 : Power-on Initialization Circuitry



V - CIRCUIT PROGRAMMING

This section defines the control and status words required to program the ST7544.

The circuit configuration is managed by the control words TxCtrl and RxCtrl and the SSIM, BFRS inputs. The control words contain three fields :

- **Mode Field** 3 bits (D15-D13) mode control bit
- **Address Field** 5 bits (D12-D8) 2 bits for Coeff Ram address
  3 bits for Control Registers address
- **Data Field** 8 bits (D7-D0) Control Registers content

V.1 - MODE FIELD

Table 3 : Mode Field

TxCtrl Word			
D15	D14	D13	Select mode
MS	Stb	QS	
0	-	-	Data Mode and Control Register access mode
1	-	-	Coefficient Loading Mode and Filter Data Memory Reset (INI)
-	↑	-	Start bit for Coefficient Loading or Reading. The loading is initiated by a rising edge, i.e. a logical one programmed after a logical zero.
-	-	1	XTAL10 Selected (INI)
-	-	0	XTAL11 Selected

INI : initial value

V.2 - ADDRESS FIELD

V.2.1 - RAM Address Field

Table 4 : RAM Address Field

TxCtrl Word								
D15	D14	D13	D12	D11	D10	D9	D8	RAM Address
MS	Stb	QS	RA0	RA1	AD2	AD1	AD0	
-	↑	-	0	0	-	-	-	RAM 1 (INI)
-	↑	-	0	1	-	-	-	RAM 2
-	↑	-	1	0	-	-	-	RAM 3
-	-	-	1	1	-	-	-	Not RAM access

INI : initial value

V.2.2 - Transmit Control Register Address Field

Table 5 : Transmit Control Register Address Field

Register Name	TxCtrl Word (2)							
	D15	D14	D13	D12	D11	D10	D9	D8
	MS	Stb	QS	RA0	RA1	AD2	AD1	AD0
TxCR0	-	-	-	-	-	0	0	0
TxCR1	-	-	-	-	-	0	0	1
TxCR2	-	-	-	-	-	0	1	0
TxCR3	-	-	-	-	-	0	1	1
None	-					1	1	1
EYE Pattern on TxI3						1	1	0 (3)

Notes : 1. A reset is generated when programming any Tx registers, this reset is synchronous with the falling edge of the Tx symbol clock.
2. No register access for the non-specified code
3. In single interface mode only

V - CIRCUIT PROGRAMMING (continued)

V.2.3 - Receive Control Register Address Field

Table 6 : Receive Control Register Address Field

Register Name	RxCtrl Word (3)							
Note 1	D15	D14	D13	D12	D11	D10	D9	D8
	-	-	-	-	-	AD2	AD1	AD0
RxCR0	-	-	-	-	-	0	0	0
RxCR1	-	-	-	-	-	0	0	1
RxCR2	-	-	-	-	-	0	1	0
RxCR3	-	-	-	-	-	0	1	1
None	-	-	-	-	-	1	1	1

Notes : 1. A reset is generated when programming the RxCR0 and RxCR1 registers, this reset is synchronous with the falling edge of the Rx symbol clock.
2. In single interface mode, the RxCtrl registers cannot be programmed during the coefficient loading mode (see Figures 7 and 8).
3. No register access for the non-specified code

V.3 - CONTROL REGISTER DATA FIELD

V.3.1 - Transmit Control Register Programming

Table 7 : Transmit Control Register Programming

Register	Data								Programmed Function
	D7	D6	D5	D4	D3	D2	D1	D0	
TxCR0	N0	R1	R0	S1	S0	T2	T1	T0	Tx Bit rate clock generator
TxCR1	M0	Q1	Q0	U2	U1	U0	P0	BS	Tx Sampling, Baud and HS clock generators; Band Split configuration.
TxCR2	AT1	AT0	LTX	LC	SST	-	VF	R2	Tx Attenuator, TxClock Synchronization, V.Fast Synchronization mode, Divider by 12/11 Bit clock
TxCR3	V2	V1	V0	W	HQ1	HQ0	Ts0	DL	Tx Sampling (used with TxCR1), FCOMP and FSHIFT frequency programming HALF-INTEGER Q DIVIDER (used with TxCR1), Test configuration

V.3.2 - Receive Control Register Programming

Table 8 : Receive Control Register Programming

Register	Data								Programmed Function
	D7	D6	D5	D4	D3	D2	D1	D0	
RxCR0	N0	R1	R0	S1	S0	T2	T1	T0	Rx Bit rate clock generator
RxCR1	M0	Q1	Q0	U2	U1	U0	P0	ECK	Rx Sampling, Baud and HS clock generators, Baud and HS clock Enable
RxCR2	LL	PS3	PS2	PS1	PS0	AP2	AP1	AP0	Rx Fine and Coarse Phase, Shift Control
RxCR3	V2	V1	V0	EMX	R2	-	HQ1	HQ0	Rx Sampling (used with RxCr1), FCOMP or TxRCLK output enable HALF-INTEGER Q DIVIDER (used with RxCR1), Divider by 12/11 Bit clock, Test configuration

V - CIRCUIT PROGRAMMING (continued)

V.3.3 - Control Bit Function Summary

V.3.3.1 - TxCTRL WORD

Table 9 : TxCTRL Word, Programmed Function

Table	Bit	Programmed Function
11,12,13,14	N0	N Divisor rank : 3, 4.
"	R2,R1,R0	R Divisor rank : 12/11, 10/9, 8/7, 6/5, 4/3, 1. (1)
"	S1,S0	S Divisor rank : 1, 3, 5, 7.
"	T2,T1,T0	T Divisor rank : 4, 8, 16, 32, 64, 128, 256, 512.
14,15,16,17,18	M0	M Divisor rank : 3, 4.
"	Q1,Q0	Q Divisor rank : 5, 6, 7, 8.
19	U2,U1,U0	U Divisor rank : 3, 4, 5, 6 ,7, 8, 12, 16.
20	P0	P Divisor rank : 3, 4.
21	BS	Band Split or Echo cancelling mode. (In band split mode the IIR2 Filter output is internally tied to IIR3 Filter Input.)
22	LTX	Synchronization signal : TxSCLK or RxCLK.
22	LC	Synchronization enabling : Lock or Free DPLL.
22	SST	TxDPLL reset on the next falling edge of the synchronization signal. SST is automatically reset after its action is completed.
23	VF	7543 and VFAST synchronization mode
23	R2	R divisor rank : +4 on R1, R0 divisor rank.
24	AT1,AT0	Tx Attenuation: 0dB, 6dB or infinite.
25	V2,V1,V0	V Divisor rank : 128 , 160
25	F	F divisor rank.
24	W	FSHIFT frequency : Fsx or Fsx / 2 (Related to frequency capture range of the TxDPLL as FQ-FSHIFT < FAVERAGE < FQ + FSHIFT)
27	Ts0,HQ1, HQ0	HALF-INTEGER Q DIVIDER (used with TxCR1 Q bit). Test Functions. Must be set to logical 0 for normal operation
27	DL	Test Loop

Note 1 : The R2 bit is found in the TxCR2 register Table 23

V.3.3.2 - RxCTRL WORD

Table 10 : RxCTRL Word, Programmed Function

Table	Bit	Programmed Function
28,29,30,31	N0	N Divisor rank : 3, 4.
"	R2,R1,R0	R Divisor rank : 12/11, 10/9, 8/7, 6/5, 4/3, 1. (1)
"	S1,S0	S Divisor rank : 1, 3, 5, 7.
"	T2,T1,T0	T Divisor rank : 4, 8, 16, 32, 64, 128, 256, 512.
32,33,34,35	M0	M Divisor rank : 3, 4.
"	Q1,Q0	Q Divisor rank : 5, 6, 7, 8.
36	U2,U1,U0	U Divisor rank : 3, 4, 5, 6 ,7, 8, 12, 16.
37	P0	P Divisor rank : 3, 4.
37	ECK	Tx/RxRCLK and Tx/RxHSCLK output enabling.
38	LL	Rx DPLL Lead/Lag control.
38	PS1,PS0	Rx DPLL Phase Shift magnitude : 0, 8, 12, 16, 20, 24, 28, PS2
38	PS3	Rx DPLL Phase Shift magnitude : One 128*Fsx period. This bit is reset after phase shift completion.
39	AP2,AP1	Rx DPLL Coarse Phase Lag : 0, 64, 128, 256 512, 1024, AP0
40	V2,V1,V0	V Divisor rank.
41	EMX	FCOMP or TxRCLK output enable (used in V.Fast synchronization mode to multiplex the transmit bit Frame.
41	HQ0,HQ1	Test Functions. Must be set to logical 0 for normal operation.
41	R2	R divisor rank : +4 on R1, R0 divisor rank. HALF-INTEGER Q DIVIDER (used with RxCR1 Q bit)

Note 1 : The R2 bit is found in the RxCR3 register Table 41

VI - PROGRAMMABLE FUNCTIONS

VI.1 - TRANSMIT SECTION

The different transmit (Tx) clocks are obtained by frequency division in several counters (see Figure 10).

Note 1 : TxPCLK is an internal Processing Clock used by the three IIR filters

Note 2 : The phase of internal clock FCOMP will be compared to the synchronization signal (Table 22) in order to control TxDPLL (see Tables 22, 25 and 26). In VFast synchronization mode FCOMP is automatically set to 2400/F Hz if the crystal frequency is equal to 36.864MHz or 25.8048MHz and if the bit rate clock is multiple of 2400Hz chosen from the Table. In 7543 mode V divisor must be chosen such that the FCOMP frequency is an integral sub-multiple of the synchronization frequency. In the latter case the most typical frequency for FCOMP is the baud rate frequency.

During each period of FCOMP the average input frequency of the transmit clock generator can be :

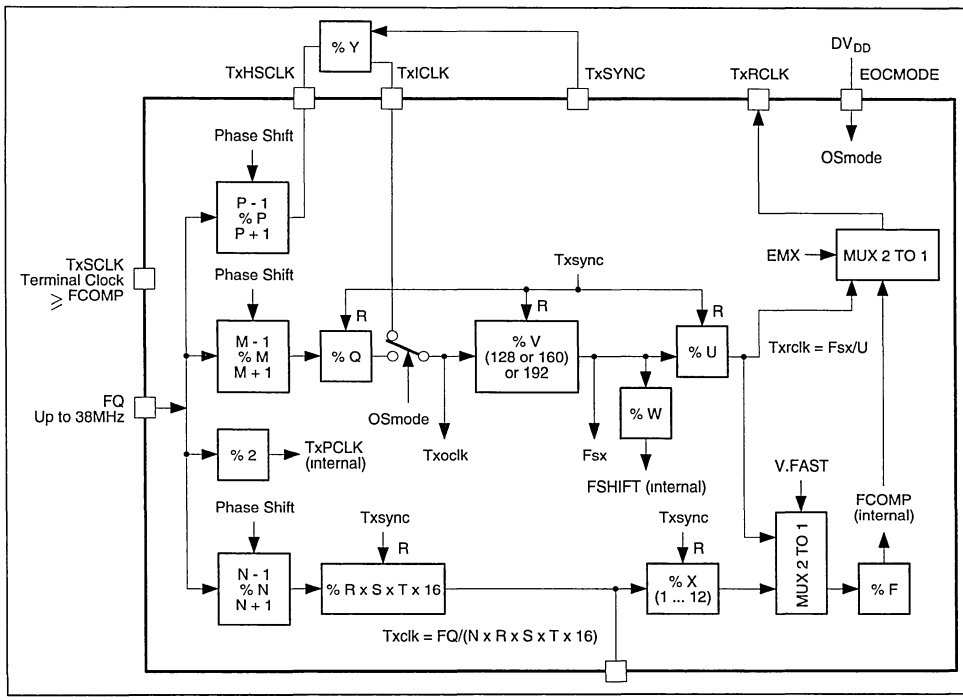
FQ , FQ + FSHIFT or FQ - FSHIFT
with FSHIFT = Fsx or Fsx/2

Note 3 : In 7543 mode the bit rate frequency must always be an integer multiple of the baud rate frequency for the transmit DPLL to lock onto the synchronization signal.

Note 4 : The Transmit clock system (without the TxHSCLK) is reset on next falling edge of the TxRCLK transmit baud clock when any Tx register is accessed.

Note 5 : The X divisor is programed automatically with the R, S and T bit.

Figure 10 : Transmit Clock Generator



VI - PROGRAMMABLE FUNCTIONS (continued)

VI.1.1 - Transmit Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

Table 11 : Transmit Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

TxCRO Register									Bit Rate Clock Frequency(Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	(FQ = 36.864MHz) Txclk = FQ/(N*R*S*T*16) (1)
N0	R1	R0	S1	S0	T2	T1	T0		
0	1	1	0	1	0	0	1	1152	32000 (2)
1	1	1	1	0	0	0	0	1280	28800
1	0	0	1	0	0	0	0	1280x12/11	26400
1	1	1	0	1	0	0	1	1536	24000
1	1	0	1	0	0	0	0	1280x4/3	21600
0	1	1	1	0	0	0	1	1920	19200 (INI)
0	0	0	1	0	0	0	1	1920x8/7	16800
0	1	1	0	1	0	1	0	2304	16000 (2)
1	1	1	1	0	0	0	1	2560	14400
1	1	1	0	1	0	1	0	3072	12000
0	1	1	1	0	0	1	0	3840	9600
0	1	1	0	1	0	1	1	4608	8000 (2)
1	1	1	1	0	0	1	0	5120	7200
0	1	1	1	0	0	1	1	7680	4800
0	1	1	1	0	1	0	0	15360	2400
0	1	1	1	0	1	0	1	30720	1200
0	1	1	1	0	1	1	0	61440	600
0	1	1	1	0	1	1	1	122880	300

Notes : 1. To use the 12/11 and the 10/9 divisor the R2 bit in the TxCR2 register (bit D0) must be set to 1. In all other case the R2 bit must be set to 0.

2. In VFAST synchronization mode the FCOMP frequency will be equal to the bit clock, as for all combinaison of the bit N0, R1, S1, S0, T2 - T0 not specified in the Table 11, 12 and 13.

VI.1.2 - Transmit Bit Rate Clock Frequency Programming with Master clock Frequency FQ=25.8048MHz

Table 12 : Transmit Bit Rate Clock Frequency Programmingwith Master Clock Frequency FQ=25.8048MHz

TxCRO Register									Bit Rate Clock Frequency (Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	(FQ = 25.8048MHz) Txclk = FQ/(N*R*S*T*16) (1)
N0	R1	R0	S1	S0	T2	T1	T0		
0	1	1	1	1	0	0	0	1344	19200
0	0	0	1	1	0	0	0	1344*8/7	16800
0	0	1	1	1	0	0	0	1344*6/5	16000 (2)
1	1	1	1	1	0	0	0	1792	14400
1	0	1	1	1	0	0	0	1792*6/5	12000
0	1	1	1	1	0	0	1	2688	9600
0	0	1	1	1	0	0	1	2688*6/5	8000 (2)
1	1	1	1	1	0	0	1	3584	7200
0	1	1	1	1	0	1	0	5376	4800
0	1	1	1	1	0	1	1	10752	2400
0	1	1	1	1	1	0	0	21504	1200
0	1	1	1	1	1	0	1	43008	600
0	1	1	1	1	1	1	0	86016	300

Notes : 1. The bit R2 in the TxCR2 register (bit D0) must be set to 0.

2. In VFAST synchronization mode the FCOMP frequency will be equal to the bit clock, as for all combinaison of the bit N0, R1, S1, S0, T2 - T0 not specified in the Table 11, 12 and 13.

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.1.3 - Transmit Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

Table 13 : Transmit Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

TxCRO Register									Bit Rate Clock Frequency (Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	Txclk= FQ/(N*R*S*T*16) (1)
N0	R1	R0	S1	S0	T2	T1	T0		
0	1	1	0	1	0	0	0	576	32000 (2)
1	1	1	0	1	0	0	0	768	24000
0	1	1	1	0	0	0	0	960	19200
0	0	0	1	0	0	0	0	960x8/7	16800
0	1	1	0	1	0	0	1	1152	16000 (2)
1	1	1	1	0	0	0	0	1280	14400
1	1	1	0	1	0	0	1	1536	12000
0	1	1	1	0	0	0	1	1920	9600 (INI)
0	1	1	0	1	0	1	0	2304	8000 (2)
1	1	1	1	0	0	0	1	2560	7200
0	1	1	1	0	0	1	0	3840	4800
0	1	1	1	0	0	1	1	7680	2400
0	1	1	1	0	1	0	0	15360	1200
0	1	1	1	0	1	0	1	30720	600
0	1	1	1	0	1	1	0	61440	300

INI : initial value

Notes : 1. The bit R2 in the TxCR2 register (bit D0) must be set to 0.

2. In VFAST synchronization mode the FCOMP frequency will be equal to the bit clock, as for all combinaison of the bit N0, R1, S1, S0, T2 - T0 not specified in the Table 11, 12 and 13.

VI.1.4 - Transmit Bit Clock Frequency Programming. Divisor Rank

Table 14 : Transmit Bit Clock Frequency Programming. Divisor Rank

TxCR0 Register								Bit Rate Clock Frequency(Hz) Txclk = FQ/(N*R*S*T*16)			
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank			
N0	R1	R0	S1	S0	T2	T1	T0	N	R	S	T
0	-	-	-	-	-	-	-	3(INI)			
1	-	-	-	-	-	-	-	4			
-	0	0	-	-	-	-	-	12/11 (with R2 = 1) (1)			
-	0	1	-	-	-	-	-	10/9 (with R2 = 1) (1)			
-	0	0	-	-	-	-	-	8/7 (with R2 = 0) (1)			
-	0	1	-	-	-	-	-	6/5 (with R2 = 0) (1)			
-	1	0	-	-	-	-	-	4/3 (with R2 = 0) (1)			
-	1	1	-	-	-	-	-	1(INI) (with R2 = 0 or 1) (1)			
-	1	1	-	-	-	-	-		1(INI)		
-	-	-	0	0	-	-	-			1	
-	-	-	0	1	-	-	-			3	
-	-	-	1	0	-	-	-			5 (INI)	
-	-	-	1	1	-	-	-			7	
-	-	-	-	-	0	0	0				4
-	-	-	-	-	0	0	1				8 (INI)
-	-	-	-	-	0	1	0				16
-	-	-	-	-	0	1	1				32
-	-	-	-	-	1	0	0				64
-	-	-	-	-	1	0	1				128
-	-	-	-	-	1	1	0				256
-	-	-	-	-	1	1	1				512

INI : initial value

Note : 1. To use the 12/11 and 10/9 divider the R2 bit in the TxCR2 register (bit D0) must be set to 1. In all other case the R2 bit must be set to 0.

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.1.5 - Transmit Sampling Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

Table 15 : Transmit Sampling Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

Symbol rate (baud)	U	M x (Y or Q) ratio	Sampling Frequency(Hz)	V Over-sampling ratio	W	Capture range
600	12	4 x 8	7200	160	1	1.95E-4
600	16	4 x 6	9600	160	1	2.60E-4
1200	6	4 x 8	7200	160	1	1.95E-4
1200	8	4 x 6	9600	160	1	2.60E-4
1600	5	4 x 6	8000	192	1	2.17E-4
1600	6	4 x 6	9600	160	1	2.60E-4
2400	3	4 x 8	7200	160	1	1.95E-4
2400	4	4 x 6	9600	160	1	2.60E-4
2400	6	4 x 5	14400 (INI)	128	2	1.95E-4
2560	3	4 x 7.5	7680	160	1	2.08E-4
2560	4	3 x 7.5	10240.00	160	1	2.77E-4
2560	6	3 x 5	15360.00	160	2	2.98E-4
2742.86	3	4 x 7	8228.57	160	1	2.40E-4
2742.86	4	3 x 7	10971.43	160	1	2.98E-4
2953.85	3	4 x 6.5	8861.54	160	1	2.40E-4
2953.85	4	3 x 6.5	11815.38	160	1	3.21E-4
3000	3	4 x 8	9000	128	1	2.44E-4
3000	4	3 x 8	12000	128	1	3.26E-4
3200	3	4 x 6	9600	160	1	2.60E-4
3200	4	3 x 6	12800	160	1	3.48E-4
3200	5	3 x 6	16000	128	1	4.34E-4
3428.57	3	4 x 7	10285.71	128	1	2.79E-4
3428.57	4	3 x 7	13714.28	128	2	1.86E-4
3490.91	3	4 x 5.5	10472.73	160	1	2.84E-4
3490.91	4	3 x 5.5	13963.64	160	1	3.79E-4

INI : initial value

VI.1.6 - Transmit Sampling Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

Table 16 : Transmit Sampling Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

Symbol rate (baud)	U	M x Qratio	Sampling Frequency(Hz)	V Over-sampling ratio	W	Capture range
2800	3	4 x 6	8400	128	1	3.26E-4
2800	4	3 x 6	11200	128	2	2.17E-4
2400	3	4 x 7	7200	128	1	2.79E-4
2400	4	3 x 7	9600	128	2	1.86E-4

VI.1.7 - Transmit Sampling Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

Table 17 : Transmit Sampling Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

Symbol Rate (baud)	U	M x Q ratio	Sampling Frequency (Hz)	V Over-sampling ratio	W	Capture range
1600	5	3 x 6	8000	128	2	2.17E-4
1600	6	3 x 5	9600	128	2	2.60E-4
2400 (INI)	3	4 x 5	7200	128	2	1.95E-4
2400	4	3 x 5	9600	128	2	2.60E-4

INI : initial value

VI - PROGRAMMABLE FUNCTIONS (continued)

VIII.1.8. Transmit Sampling Clock Frequency Programming. Divisor Rank

Table 18 : Transmit Sampling Clock Frequency Programming. Divisor Rank

TxCR1 Register								Sampling Clock frequency Fsx = FQ/(MxQxV) (1)	
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	
M0	Q1	Q0	U2	U1	U0	P0	BS	M	Q (2)
0	-	-	-	-	-	-	-	3	
1	-	-	-	-	-	-	-	4 (INI)	
-	0	0	-	-	-	-	-		5 (INI) (4.5)
-	0	1	-	-	-	-	-		6 (5.5)
-	1	0	-	-	-	-	-		7 (6.5)
-	1	1	-	-	-	-	-		8 (7.5)

INI : initial value

Notes : 1. The V divider is programmed in the TxCR3 register.
2. To use the fractional Q divider bits HQ1 and HQ0 in Table 27 must be set to "1" (otherwise they are set to "0").

VIII.1.9. Transmit Baud Rate Frequency Programming. Divisor Rank

Table 19 : Transmit Baud Rate Frequency Programming. Divisor Rank

TxCR1 Register								Baud rate Frequency Txrclk = Fsx / U
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank
M0	Q1	Q0	U2	U1	U0	P0	BS	U
-	-	-	0	0	0	-	-	3 (INI)
-	-	-	0	0	1	-		4
-	-	-	0	1	0	-	-	5
-	-	-	0	1	1	-	-	6
-	-	-	1	0	0	-	-	8
-	-	-	1	0	1	-	-	12
-	-	-	1	1	0	-	-	16
-	-	-	1	1	1	-	-	16

INI : initial value

VIII.1.10. Highest Synchronous Transmit Frequency Programming. Divisor Rank

Table 20 : Highest Synchronous Transmit Frequency Programming. Divisor Rank

TxCR1 Register								Highest Synchronous Transmit Frequency Txhsclk=FQ/P
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank
M0	Q1	Q0	U2	U1	U0	P0	BS	P
-	-	-	-	-	-	0	-	3
-	-	-	-	-	-	1		4

INI : initial value

VIII.1.11. Band Split Mode

Table 21 : Band Split Mode

TxCR1 Register								Band Split Mode
D7	D6	D5	D4	D3	D2	D1	D0	
M0	Q1	Q0	U2	U1	U0	P0	BS	
-	-	-	-	-	-	-	0	Inactive (INI)
-	-	-	-	-	-	-	1	Active : Rx Filter Output connected to reconstruction filter input (see Figure 1).

INI : initial value

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.1.12 - Transmit Synchronization Signal Programming

Table 22 : Transmit Synchronization Signal Programming

TxCR2 Register								Tx DPLL Clock
D7	D6	D5	D4	D3	D2	D1	D0	Synchronization
AT1	AT0	LTX	LC	SST	-	VF	R2	
-	-	0	1	-	-	-	-	TxSCLK (1)
-	-	1	1	-	-	-	-	RxCLK (1)
-	-	-	1	1	-	-	-	Reset on the Next falling edge of the Synchronization Signal (1) (2)
-	-	-	0	-	-	-	-	No Synchronization (INI)

INI : initial value

Notes : 1. If D4 = 1, the TxDPLL will be locked to the synchronization signal. Otherwise, the Tx DPLL will be free-running.
2. The SST bit is automatically reset after its action is completed.

VI.1.13 - Clock Mode Programming & R2 Divisor

Table 23 : Clock Mode Programming & R2 Divisor

TxCR2 Register								Mode Programming & R2 divisor
D7	D6	D5	D4	D3	D2	D1	D0	
AT1	AT0	LTX	LC	SST	-	VF	R2	
-	-	-	-	-	-	0	-	7543 synchronization Mode (INI)
-	-	-	-	-	-	1	-	V.Fast synchronization Mode
-	-	-	-	-	-	-	R2	see Table 14 - R2 = 0 (INI)

INI : initial value

VI.1.14 - Transmit Attenuator Programming

Table 24 : Transmit Attenuator Programming

TxCR2 Register								Transmit Attenuator
D7	D6	D5	D4	D3	D2	D1	D0	Attenuation (dB)
AT1	AT0	LTX	LC	SST	-	VF	R2	
0	0	-	-	-	-	-	-	Infinite (INI)
1	0	-	-	-	-	-	-	-6
1	1	-	-	-	-	-	-	0

INI : initial value

VI.1.15 - Phase Comparator Frequency and Decimation & Interpolation Ratio

Table 25 : Phase Comparator Frequency And Decimation & Interpolation Ratio

TxCR3 Register								Tx Phase Comparator Frequency FCOMP = Txrclk / F or 2400 / F (2) and V Divisor rank	
D7	D6	D5	D4	D3	D2	D1	D0	FCOMP	Oversampling ratio
V2	V1	V0	W	HQ1	HQ0	Ts0	DL	F	V
0	0	0	-	-	-	-	-	1	128
0	0	1	-	-	-	-	-	2	128
0	1	0	-	-	-	-	-	1	160
0	1	1	-	-	-	-	-	2	160
1	0	0	-	-	-	-	-	4	128 (INI)
1	0	1	-	-	-	-	-	1	192
1	1	0	-	-	-	-	-	4	160
1	1	1	-	-	-	-	-	1	256 (1)

INI : initial value

Notes : 1. The performance is not guaranteed with this oversampling ratio.
2. FCOMP is depending of the synchronization mode (normal or VFAST).

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.1.16 - Phase Shift Frequency

Table 26 : Phase Shift Frequency

TxCR3 Register								Phase Shift Frequency (1) FSHIFT = Fsx / W
D7	D6	D5	D4	D3	D2	D1	D0	(Average updated master clock frequency)
V2	V1	V0	W	HQ1	HQ0	Ts0	DL	W
-	-	-	0	-	-	-	-	Fsx/2 (INI) (FQ ± Fsx/2)
-	-	-	1	-	-	-	-	Fsx (FQ ± Fsx)

INI : initial value

Note 1 : The W bit selects the phase shift frequency of the TxDPLL, and hence the capture range (see Figure 9)

VI.1.17 - Transmit Test Programming

Table 27 : Transmit Test Programming

TxCR3 Register								Test Modes
D7	D6	D5	D4	D3	D2	D1	D0	
V2	V1	V0	W	HQ1	HQ0	Ts0	DL	
				0	0	0	0	Normal Mode (INI)
-	-	-	-	-	-	-	1	Digital Loop Test (1)
-	-	-	-	-	-	1	-	Test 0 (Internal use only)
-	-	-	-	0	1	-	-	Test 1 (Internal use only)
-	-	-	-	1	0	-	-	Test 2 (Internal use only)
-	-	-	-	1	1	-	-	HALF-INTEGER Q DIVIDER (see Table 18) (2)

INI : initial value

Notes : 1. To perform the digital loop test, the single serial interface and band split modes should be selected, the signal at TxD0 pin should be looped into the RxDI pin, and the Fsx should be equal to the Fsr. Under these conditions, the A/DC input will appear at the output on the D/AC. This test is useful to verify the performance of the ADC, DAC and IIR filters.

2. Test pin EOCMODE must be set to "0" in this configuration.

VI - PROGRAMMABLE FUNCTIONS (continued)

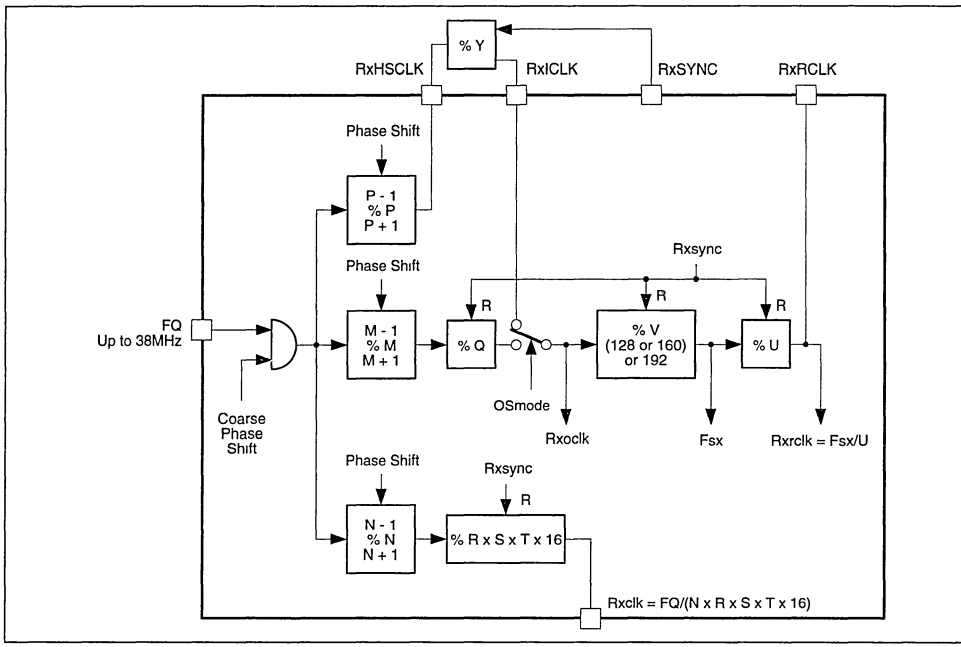
VI.2 - RECEIVE SECTION

The different Receive (Rx) clocks are derived from the master clock (FQ) using the dividers shown in Figure 11.

The counters of the Rx clock system (without the RxHSCLK) are reset when powering on the ST7544 and when the NLPR input level is low.

They can also be reset, under software control, on the next falling edge of the RxRCLK receive baud rate clock when the RxCR0 or RxCR1 register are accessed : this feature is used to fix the phase of the bit rate clock with respect to the baud rate clock, e.g. after each modification of the bit or baud rate value.

Figure 11 : Receive Clock Generator



VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.1 - Receive Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

Table 28 : Receive Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

RxCRO Register									Bit Rate Clock Frequency (Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	(FQ = 36.864MHz) Rxclk = FQ/(N*R*S*T*16)
N0	R1	R0	S1	S0	T2	T1	T0		
0	1	1	0	1	0	0	1	1152	32000 (2)
1	1	1	1	0	0	0	0	1280	28800
1	0	0	1	0	0	0	0	1280x12/11	26400 (1)
1	1	1	0	1	0	0	1	1536	24000
1	1	0	1	0	0	0	0	1280x4/3	21600
0	1	1	1	0	0	0	1	1920	19200 (INI)
0	0	0	1	0	0	0	1	1920x8/7	16800
0	1	1	0	1	0	1	0	2304	16000 (2)
1	1	1	1	0	0	0	1	2560	14400
1	1	1	0	1	0	1	0	3072	12000
0	1	1	1	0	0	1	0	3840	9600
0	1	1	0	1	0	1	1	4608	8000 (2)
1	1	1	1	0	0	1	0	5120	7200
0	1	1	1	0	0	1	1	7680	4800
0	1	1	1	0	1	0	0	15360	2400
0	1	1	1	0	1	0	1	30720	1200
0	1	1	1	0	1	1	0	61440	600
0	1	1	1	0	1	1	1	122880	300

INI : initial value

Notes : 1. To use the 12/11 and the 10/9 divisor the R2 bit in the TxCR2 register (bit D0) must be set to 1. In all other case the R2 bit must be set to 0.

2. In VFAST synchronization mode the FCOMP frequency will be equal to the bit clock, as for all combinaison of the bit N0, R1, S1, S0, T2 - T0 not specified in the Table 11, 12 and 13.

VI.2.2 - Receive Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

Table 29 : Receive Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

RxCRO Register									Bit Rate Clock Frequency (Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	(FQ = 25.8048MHz) Rxclk = FQ/(N*R*S*T*16) (1)
N0	R1	R0	S1	S0	T2	T1	T0		
0	1	1	1	1	0	0	0	1344	19200
1	0	0	1	1	0	0	0	1344*8/7	16800
0	0	1	1	1	0	0	0	1344*6/5	16000 (2)
1	1	1	1	1	0	0	0	1792	14400
1	0	1	1	1	0	0	0	1792*6/5	12000
0	1	1	1	1	0	0	1	2688	9600
0	0	1	1	1	0	0	1	2688*6/5	8000 (2)
1	1	1	1	1	0	0	1	3584	7200
0	1	1	1	1	0	1	0	5376	4800
0	1	1	1	1	0	1	1	10752	2400
0	1	1	1	1	1	0	0	21504	1200
0	1	1	1	1	1	0	1	43008	600
0	1	1	1	1	1	1	0	86016	300

Notes : 1. The bit R2 in the TxCR2 register (bit D0) must be set to 0.

2. In VFAST synchronization mode the FCOMP frequency will be equal to the bit clock, as for all combinaison of the bit N0, R1, S1, S0, T2 - T0 not specified in the Table 11, 12 and 13.

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.3 - Receive Bit Rate Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

Table 30 : Receive Bit Rate Clock Frequency Programming With Master Clock Frequency FQ=18.432MHz

RxCRO Register									Bit Rate Clock Frequency (Hz)
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	(FQ = 18.432MHz) Rxclk = FQ/(N*R*S*T*16) (1)
N0	R1	R0	S1	S0	T2	T1	T0		
0	1	1	0	1	0	0	0	576	32000 (2)
1	1	1	0	1	0	0	0	768	24000
0	1	1	1	0	0	0	0	960	19200
0	0	0	1	0	0	0	0	960*8/7	16800
0	1	1	0	1	0	0	1	1152	16000 (2)
1	1	1	1	0	0	0	0	1280	14400
1	1	1	0	1	0	0	1	1536	12000
0	1	1	1	0	0	0	1	1920	9600 (INI)
0	1	1	0	1	0	1	0	2304	8000 (2)
1	1	1	1	0	0	0	1	2560	7200
0	1	1	1	0	0	1	0	3840	4800
0	1	1	1	0	0	1	1	7680	2400
0	1	1	1	0	1	0	0	15360	1200
0	1	1	1	0	1	0	1	30720	600
0	1	1	1	0	1	1	0	61440	300

INI : initial value

Notes : 1. The bit R2 in the TxCR2 register (bit D0) must be set to 0.

2. In VFAST synchronization mode the FCOMP frequency will be equal to the bit clock, as for all combinaison of the bit N0, R1, S1, S0, T2 - T0 not specified in the Table 11, 12 and 13.

VI.2.4 - Receive Bit Rate Clock Frequency Programming. Divisor Rank

Table 31 : Receive Bit Rate Clock Frequency Programming. Divisor Rank

RxCR0 Register								Bit rate clock frequency Rxclk=FQ/(N*R*S*T*16)			
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank			
N0	R1	R0	S1	S0	T2	T1	T0	N	R	S	T
0	-	-	-	-	-	-	-	3 (INI)			
1	-	-	-	-	-	-	-	4			
-	0	0	-	-	-	-	-		12/11 (with R2 = 1) (1)		
-	0	1	-	-	-	-	-		10/9 (with R2 = 1) (1)		
-	0	0	-	-	-	-	-		8/7 (with R2 = 0) (1)		
-	0	1	-	-	-	-	-		6/5 (with R2 = 0) (1)		
-	1	0	-	-	-	-	-		4/3 (with R2 = 0) (1)		
-	1	1	-	-	-	-	-		1(INI)		
-	-	-	0	0	-	-	-			1	
-	-	-	0	1	-	-	-			3	
-	-	-	1	0	-	-	-			5 (INI)	
-	-	-	1	1	-	-	-			7	
-	-	-	-	-	0	0	0				4
-	-	-	-	-	0	0	1				8 (INI)
-	-	-	-	-	0	1	0				16
-	-	-	-	-	0	1	1				32
-	-	-	-	-	1	0	0				64
-	-	-	-	-	1	0	1				128
-	-	-	-	-	1	1	0				256
-	-	-	-	-	1	1	1				512

INI : initial value

Note : 1. To use the 12/11 and the 10/9 divider register the bit R2 in the RxCR3 register (bit D3) must be set to 1 either in all other case R2 must be set to 0

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.5 - Receive Sampling Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

Table 32 : Receive Sampling Clock Frequency Programming with Master Clock Frequency FQ=36.864MHz

Symbol Rate (baud)	U	M x Y or M x Q ratio	Sampling Frequency (Hz)	V OverSampling ratio
600	12	4 x 8	7200	160
600	16	4 x 6	9600	160
1200	6	4 x 8	7200	160
1200	8	4 x 6	9600	160
1600	5	4 x 6	8000	160
1600	6	4 x 6	9600	192
2400	3	4 x 8	7200	160
2400	4	4 x 6	9600	160
2400	6	4 x 5	14400 (INI)	128
2560	3	4 x 7.5	7680	160
2560	4	3 x 7.5	10240.00	160
2560	6	3 x 5	15360.00	160
2742.86	3	4 x 7	8228.57	160
2742.86	4	3 x 7	10971.43	160
2953.85	3	4 x 6.5	8861.54	160
2953.85	4	3 x 6.5	11815.38	160
3000	3	4 x 8	9000	128
3000	4	3 x 8	12000	128
3200	3	4 x 6	9600	160
3200	4	3 x 6	12800	160
3200	5	3 x 6	16000	128
3428.57	3	4 x 7	10285.71	128
3428.57	4	3 x 7	13714.28	128
3490.91	3	4 x 5.5	10472.73	160
3490.91	4	3 x 5.5	13963.64	160

INI : initial value

VI.2.6 - Receive Sampling Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

Table 33 : Receive Sampling Clock Frequency Programming with Master Clock Frequency FQ=25.8048MHz

Symbol Rate (baud)	U	Mx(Y or Q)	Sampling ratio	V OverSampling Frequency (Hz)
2800	3	4 x 6	8400	128
2800	4	3 x 6	11200	128
2400	3	4 x 7	7200	128
2400	4	3 x 7	9600	128

VI.2.7 - Receive Sampling Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

Table 34 : Receive Sampling Clock Frequency Programming with Master Clock Frequency FQ=18.432MHz

Symbol Rate (baud)	U	M x Q	Sampling ratio	V OverSampling Frequency (Hz)
1600	5	3 x 6	8000	128
1600	6	3 x 5	9600	128
2400 (INI)	3	4 x 5	7200	128
2400	4	3 x 5	9600	128

INI : initial value

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.8 - Receive Sampling Clock Frequency Programming. Divisor Rank

Table 35 : Receive Sampling Clock Frequency Programming. Divisor Rank

RxCR1 Register								Sampling Clock frequency Fsr=FQ/(M x Q x V) (1)	
D7	D6	D5	D4	D3	D2	D1	D0	Divisor rank	
M0	Q1	Q0	U2	U1	U0	P0	ECK	M	Q (2)
0	-	-	-	-	-	-	-	3	
1	-	-	-	-	-	-	-	4 (INI)	
-	0	0	-	-	-	-	-		5 (INI) (4.5)
-	0	1	-	-	-	-	-		6 (5.5)
-	1	0	-	-	-	-	-		7 (6.5)
-	1	1	-	-	-	-	-		8 (7.5)

INI : initial value

Notes : 1. The V divider is programmed in the RxCR3 Register
2. To use the fractional divider bits HQ1 and HQ0 in Table 41 must be set to "1" (otherwise they are set to "0").

VI.2.9 - Receive Baud Rate Frequency Programming. Divisor Rank

Table 36 : Receive Baud Rate Frequency Programming. Divisor Rank

RxCR1 Register								Baud rate frequency Rxrclk = Fsr / U
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank U
M0	Q1	Q0	U2	U1	U0	P0	ECK (1)	
-	-	-	0	0	0	-	1	3 (INI)
-	-	-	0	0	1	-	1	4
-	-	-	0	1	0	-	1	5
-	-	-	0	1	1	-	1	6
-	-	-	1	0	0	-	1	8
-	-	-	1	0	1	-	1	12
-	-	-	1	1	0	-	1	16
-	-	-	1	1	1	-	1	16

INI : initial value

Note : 1. ECK bit is used to enable the RxRCLK and RxHSCLK outputs (as well as TxRCLK and TxHSCLK clock outputs) when set at logical 1. The baud rate clock must be programmed to its correct value even though the corresponding output pin is disabled (ECK = 0).

VI.2.10 - Highest Synchronous Transmit Bit Frequency Programming. Divisor Rank

Table 37 : Highest Synchronous Transmit Bit Frequency Programming. Divisor Rank

RxCR1 Register								Highest Synchronous Receive frequency RxhsClk=FQ/P0
D7	D6	D5	D4	D3	D2	D1	D0	Divisor Rank P
M0	Q1	Q0	U2	U1	U0	P0	ECK (1)	
-	-	-	-	-	-	0	1	3
-	-	-	-	-	-	1	1	4

INI : initial value

Note : 1. ECK bit is used to enable the RxRCLK and RxHSCLK outputs (as well as TxRCLK and TxHSCLK clock outputs) when set at logical 1. The baud rate clock must be programmed to its correct value even though the corresponding output pin is disabled (ECK = 0).

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.11 - Receive Fine Phase Shift Programming

Table 38 : Receive Fine Phase Shift Programming

RxCR2 Register								Receive Fine Phase Shift Programming
D7	D6	D5	D4	D3	D2	D1	D0	Action on RxDPLL Number of Master Clock Pulses Suppressed
LL	PS3	PS2	PS1	PS0	AP2	AP1	AP0	
0	0	0	0	0	0	0	0	No phase shift (INI)
0	0	0	0	1	0	0	0	8
0	0	0	1	0	0	0	0	12
0	0	0	1	1	0	0	0	16
0	0	1	0	0	0	0	0	20
0	0	1	0	1	0	0	0	24
0	0	1	1	0	0	0	0	28
0	0	1	1	1	0	0	0	32
0	1	0	0	0	0	0	0	One Txoclk oversampling period (1)
1	-	-	-	-	-	-	-	As above but lead instead of lag (i.e. addition of Master-Clock pulses)

INI : initial value

Note 1 : Available only with an internal Q divider. To shift one oversampling period, the chip must know the Q divider value currently used

VI.2.12 - Receive Coarse Phase Shift Programming

Table 39 : Receive Coarse Phase Shift Programming

RxCR2 Register								Receive Coarse Phase Shift Amplitude Programming
D7	D6	D5	D4	D3	D2	D1	D0	Number of Master Clock Pulses Suppressed
LL	PS3	PS2	PS1	PS0	AP2	AP1	AP0	
0	0	0	0	0	0	0	0	No Phase Shift (INI)
0	0	0	0	0	0	0	1	64
0	0	0	0	0	0	1	0	128
0	0	0	0	0	0	1	1	256
0	0	0	0	0	1	0	0	512
0	0	0	0	0	1	0	1	1024
0	0	0	0	0	1	1	0	2048
0	0	0	0	0	1	1	1	4096

INI : initial value

VI - PROGRAMMABLE FUNCTIONS (continued)

VI.2.13 - Interpolation Ratio

Table 40 : Interpolation Ratio

RxCR3 Register								INTERPOLATION RATIO Divisor value
D7	D6	D5	D4	D3	D2	D1	D0	V
V2	V1	V0	EMX	R2	-	HQ1	HQ0	
0	0	0	-	-	-	-	-	128
0	0	1	-	-	-	-	-	128
0	1	0	-	-	-	-	-	160
0	1	1	-	-	-	-	-	160
1	0	0	-	-	-	-	-	128 (INI)
1	0	1	-	-	-	-	-	192
1	1	0	-	-	-	-	-	160
1	1	1	-	-	-	-	-	256 (1)

INI : initial value

Note 1 : The performances are not garanted with this oversampling ratio.

VI.2.14 - Receive Test Programming & R2 Divisor

Table 41 : Receive Test Programming And R2 Divisor

RxCR3 Register								Test Mode & R2 divisor
D7	D6	D5	D4	D3	D2	D1	D0	
V2	V1	V0	EMX	R2	-	HQ1	HQ0	
-	-	-	-	-	0	0	0	Normal Mode (INI)
-	-	-	-	R2	-	-	-	see Table 31 (RxCR0) R2 = 0 (INI)
-	-	-	0	-	-	-	-	Tx RCLK output on TxRCLK pin (INI)
-	-	-	1	-	-	-	-	FCOMP output on TxRCLK pin (see Figure 10)
-	-	-	-	-	-	1	1	HALF-INTEGER Q DIVIDER (see Table 35)

INI : initial value

VII - ELECTRICAL SPECIFICATIONS

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for V_{DD} = +5V , T_{amb} = 25°C and for nominal crystal frequency FQ = 36.864MHz.

VII.1 - ABSOLUTE MAXIMUM RATINGS (referenced to GND)

Table 42 : Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply voltage	-0.3 to 7.0	V
V_I,V_{IN}	Digital or analog input voltage	- 0.3, V_{DD} +0.3	V
I_I,I_{IN}	Digital or analog input current	± 1	mA
I_O	Digital output current	± 20	mA
I_{OUT}	Analog output current	± 10	mA
T_A	Operating temperature range	0, +70	°C
T_{stg}	Storage temperature range (plastic)	- 40, + 125	°C
P_{Dmax}	Maximum power dissipation	500	mW

VII.2 - DC CHARACTERISTICS

V_{DD} = 5.0 V ± 5%, GND = 0 V, T_a = 0 to +70 °C (unless otherwise specified)

VII.2.1 - Power Supply and Common Mode Voltage

Table 43 : Power Supply And Common Mode Voltage

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		4.75	5	5.25	V
I_{DD}	Supply current	FQ = 18.432MHz FQ = 36.864MHz		32 52	37	mA mA
I_{DD}-LP	Supply current in low power mode			0.6		mA
V_{CM}	Input common mode voltage		V_{DD}/2 -5%	V_{DD}/2	V_{DD}/2 +5%	V

VII.2.2 - Digital Interface

All digital pins except XTAL pins.

Table 44 : Digital Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage	-0.3		0.8	V
V_{IH}	High Level Input Voltage	2.2			V
I_I	Input Current V_I = V_{DD} or V_I = GND	-10	±1	+10	µA
V_{OH}	High Level Output Voltage (I_{LOAD} = -2mA)	2.4			V
V_{OL}	Low Level Output Voltage (I_{LOAD} = 2 mA)			0.4	V
C_{IN}	Input Capacitance		5		pF

VII.2.3 - Crystal Oscillator Interface (XTAL10,XTAL11)

Table 45 : Crystal Oscillator Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage			1.5	V
V_{IH}	High Level Input Voltage	3.5			V
I_L	Low Level Input Current (GND ≤ V_I ≤ V_{IL}max)		-15		µA
I_H	High Level Input Current (V_{IH}min ≤ V_I ≤ V_{DD})		15		µA

VII - ELECTRICAL SPECIFICATIONS (continued)

VII.2.4 - Analog Interface

Table 46 : Analog Interface

Symbol	Parameter		Min	Typ	Max	Unit
V_{REF}	Differential Reference Voltage Output = V_{REFP}-V_{REFN}		2.40	2.50	2.60	V
Tempco (V_{REF})	V_{REF} Temperature Coefficient			200		ppm/°C
$V_{CMO\ IN}$	Input Common Mode Offset Voltage = $\frac{RxA1 + RxA2}{2} - V_{CM}$		-300		300	mV
$V_{DIF\ IN}$	Differential Input Voltage : RxA1-RxA2 <= 2*V_{REF}			2 * V_{REF}		Vpp
$V_{OFF\ IN}$	Differential Input DC Offset Voltage : RxA1 = RxA2 = V_{CM} (1)					
			-100		100	mV
$V_{CMO\ OUT}$	Output common mode voltage offset = $\frac{TxA1 + TxA2}{2} - V_{CM}$		200		200	mV
$V_{DIF\ OUT}$	Differential Output Voltage : TxA1-TxA2 <= 2*V_{REF}			2 * V_{REF}		Vpp
$V_{OFF\ OUT}$	Differential Output DC Offset Voltage : (TxA1 - TxA2)DC		-100		100	mV
V_{OUT}	Output Voltage EYEX,EYEY		GND		VDD	V
R_{IN}	Input Resistance RxA1, RxA2		100			kΩ
R_{OUT}	Output Resistance	TxA1,TxA2 EYEX, EYEY			20 50	Ω Ω
R_L	Load Resistance	TxA1,TxA2 EYEX, EYEY	10 1			kΩ kΩ
C_L	Load Capacitance	TxA1,TxA2 EYEX, EYEY			50 30	pF pF

Note 1 : Input DC offset can be cancelled by high-pass filtering in IIR2 filter

VII - ELECTRICAL SPECIFICATIONS (continued)

VII.3 - AC ELECTRICAL SPECIFICATIONS (V_{DD} = 5.0 V ± 5%, T_a = 0 to +70 °C)

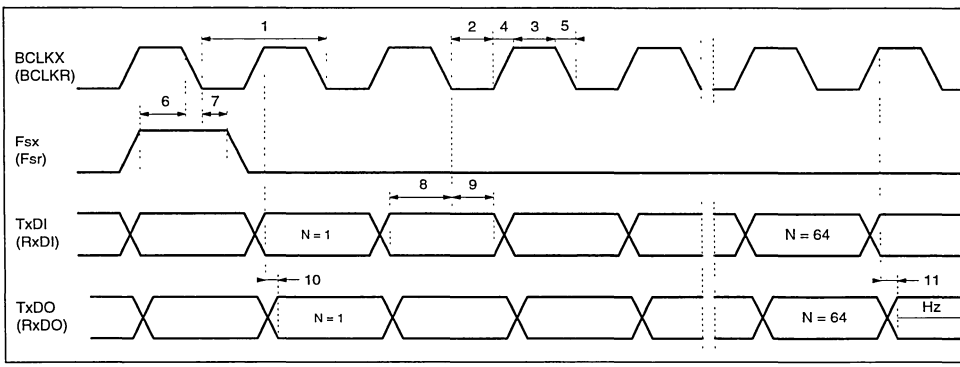
Output Load = 50 pF, Reference levels : V_{IL} = 0.8 V, V_{IH} = 2.2 V, V_{OL} = 0.4 V, V_{OH} = 2.4 V

VII.3.1 - Serial Channel Timing

Table 47 : Serial Channel Timing

Number	Parameter	Min.	Typ.	Max.	Unit
1	BCLKX, BCLKR Period	300			ns
2	BCLKX, BCLKR Width Low	135			ns
3	BCLKX, BCLKR Width High	135			ns
4	BCLKX, BCLKR Rise Time			30	ns
5	BCLKX, BCLKR Fall Time			30	ns
6	FSX, FSR to BCLKX, BCLKR Setup	100			ns
7	FSX, FSR to BCLKX, BCLKR Hold	100			ns
8	TxDI, RxDI to BCLKX, BCLKR Setup	20			ns
9	TxDI, RxDI to BCLKX, BCLKR Hold	0			ns
10	BCLKX, BCLKR High to TxDO, RxDO Valid		50	50	ns
11	BCLKX, BCLKR To TxDO, RxDO Hiz		50	50	ns

Figure 12 : Serial Channel Timming

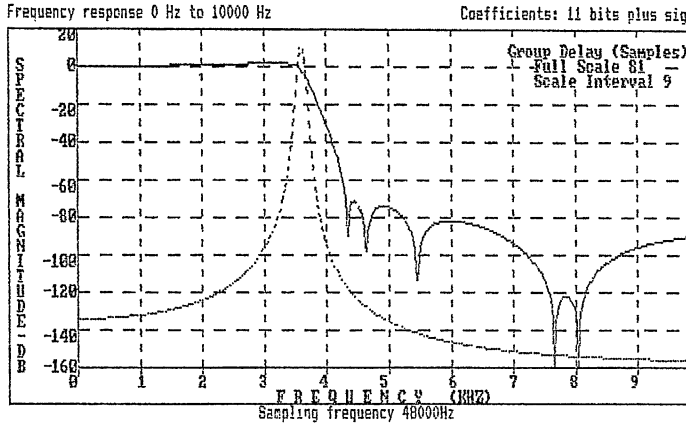


VIII - TRANSMIT CHARACTERISTICS

VIII.1 - TEST CONDITIONS

The Tx characteristics depend on the transfer function of the transmit filter. The indicated performance is measured when IIR1 filter implements the 8th order low-pass transfer function (including sinx/x correction) shown in Figure 13. This is achieved by loading the coefficients given in table 48.
The frequency response in Figure 13 includes the gain of 72.25dB in front of the biquad 1 (see Figure A1)

Figure 13 : Filter Transfer Function (Sampling frequency = 48000Hz, Fsx = 9600Hz, Sample of group delay = 1/5 x Fsx)



7544-15.TIF

Table 48 : Interpolator Filter Coefficients

WORD	7200,9600	WORD	7200,9600	WORD	7200,9600	WORD	7200,9600	WORD	7200,9600
1	0000,0000	9	0000,ca08	17	4c98,5070	25	a000,a000	33	0750,0858
2	0000,0000	10	0000,a000	18	2438,3508	26	adb8,ac18	34	6aa8,4098
3	a000,a000	11	b368,b570	19	d7a8,cfa0	27	5e70,6118	35	a000,a000
4	0000,0000	12	4400,48a0	20	a000,a000	28	0748,07a0	36	0000,0000
5	0000,0000	13	0200,2838	21	af18,aed8	29	a280,3368	37	0000,0000
6	0000,b7d8	14	d330,cb68	22	5690,59d0	30	a000,a000	38	0008,0008
7	0000,42b0	15	a000,a000	23	2118,2898	31	a910,adf0	-	-
8	a000,0118	16	b118,b268	24	4f80,dd90	32	5120,5338	-	-

Filter coefficients (HEX FORMAT) for Fsx equal to 7200 and 9600Hz respectively

VIII.2 - PERFORMANCE OF THE Tx CHAIN (from IIR1 filter input to (TxA1-TxA2) output)

Typical values are given for V_{DD} = +5V , T_{amb} = 25°C and for nominal crystal frequency FQ = 36.864MHz. Measurement band = DC to 3.4kHz - Tx DPLL free running.

Table 49 : Performance of the Tx chain

Symbol	Parameter		Min	Typ	Max	Unit
Gabs	Absolute gain at 1kHz		-0.5	0	0.5	dB
THD	Total harmonic distortion (differential Tx signal : V_{OUT} = 2.5V_{PP}, f = 1kHz)	Fsx = 7200Hz Fsx = 9600Hz		-89 -89		dB dB
DR	Dynamic range (1) (f = 1kHz, OverSampling ratio 160)	Fsx = 7200Hz Fsx = 9600Hz		91 92		dB dB
PSRR	Power supply rejection ratio (f = 1kHz, V_{AC} = 200mV_{PP})			50		dB
CTxRx	Crosstalk (transmit channel to receive channel)			95		dB

Note 1 : Measured over the full 0 to Fsx/2 with a -10dBr input and extrapolated to fullscale

VIII.3 - SMOOTHING FILTER TRANSFER CHARACTERISTICS

The cut-off frequency of the single pole switch-capacitor low-pass filter following the DAC (Figure 1) is :

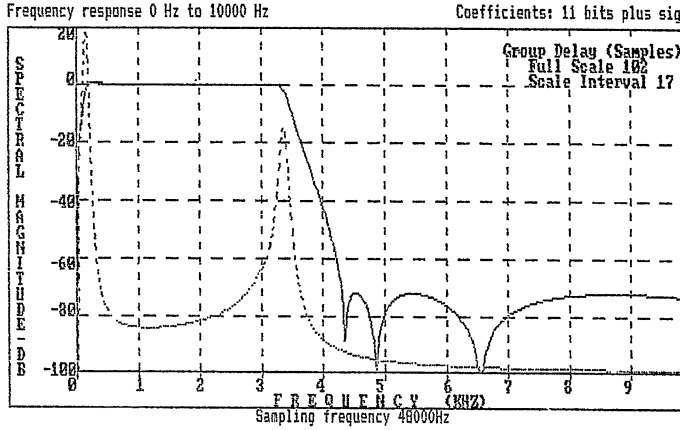
$$fc\text{-}3dB = 128*Fsx/(2*\pi*10) \text{ or } fc\text{-}3dB = 160*Fsx/(2*\pi*10)$$

IX - RECEIVE CHARACTERISTICS

IX.1 - TEST CONDITIONS

The Rx characteristics depend on the transfer function of the receive filter. The indicated performance is measured when IIR2 filter implements the 6th order band-pass transfer function shown in Figure 14. This is achieved by loading the coefficients given in Table 50.

Figure 14 : Filter Transfer Function (Sampling frequency = 48000Hz, Fsx = 9600Hz, Sample of group delay = 1/5 x Fsx)



7544-16.TIF

Table 50 : Decimator Filter Coefficients

WORD	7200,9600	WORD	7200,9600	WORD	7200,9600	WORD	7200,9600	WORD	7200,9600
1	0000,0000	9	0000,e000	17	4d90,4250	25	a000,a000	33	0d38,0618
2	0000,0000	10	e000,0000	18	25b8,2890	26	ab60,b5b0	34	0000,1a38
3	a000,a000	11	b2c0,bf38	19	d1b0,ca18	27	5a40,4e88	35	a000,a000
4	0000,0000	12	5998,4188	20	a000,a000	28	09b8,23c8	36	0000,0000
5	0000,0000	13	12c8,0188	21	b1f8,b748	29	2c30,d620	37	0000,0000
6	0000,0000	14	4c80,e000	22	4668,47a8	30	a000,a000	38	0008,0008
7	0000,0000	15	a000,0000	23	1408,1b98	31	a088,b470	-	-
8	20f8,3208	16	a5e0,b8e0	24	de78,cc80	32	6a30,5468	-	-

Filter coefficients (HEX FORMAT) for Fsx equal to 7200 AND 9600Hz respectively

IX.2 - PERFORMANCE OF THE Rx CHAIN (from (RxA1-RxA2) input to IIR2 filter output)

Typical values are given for V_{DD} = +5V , T_{amb} = 25°C and for nominal crystal frequency FQ=36.864MHz. Measurement band = DC to 3.4kHz - Tx DPLL free running.

Table 51: Performance of the Rx chain

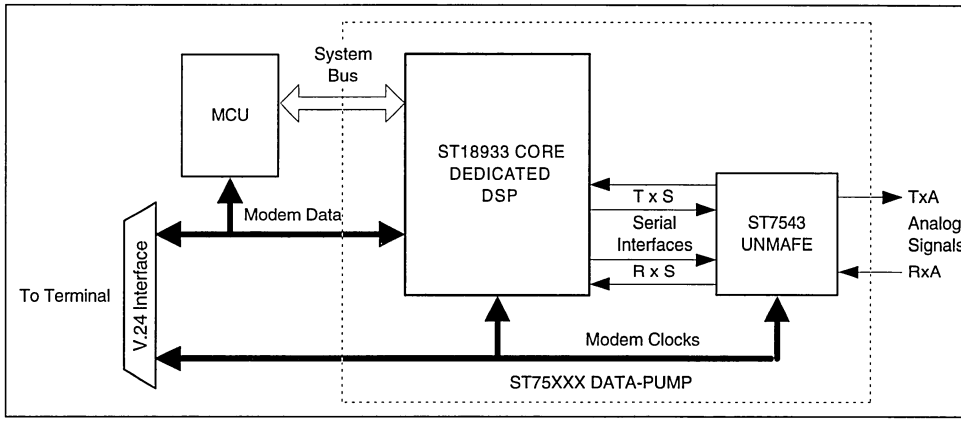
Symbol	Parameter		Min	Typ	Max	Unit
Gabs	Absolute gain at 1 kHz		-0.5	0	0.5	dB
THD	Total harmonic distortion (differential Tx signal : V_{OUT} = 2.5 V_{PP}, f = 1kHz)	Fsx = 7200 Hz Fsx = 9600 Hz		-89 -89		dB dB
DR	Dynamic range (1) f = 1kHz, OverSampling ratio 160	Fsx = 7200 Hz Fsx = 9600 Hz		91 92		dB dB
PSRR	Power supply rejection ratio (f = 1kHz, V_{AC} = 200mV_{PP})			50		dB
CTxRx	Crosstalk (receive channel to transmit channel)			95		dB

Note 1 : Measured over the full 0 to Fsx/2 with a -10dBr input and extrapolated to fullscale

X - TYPICAL APPLICATIONS

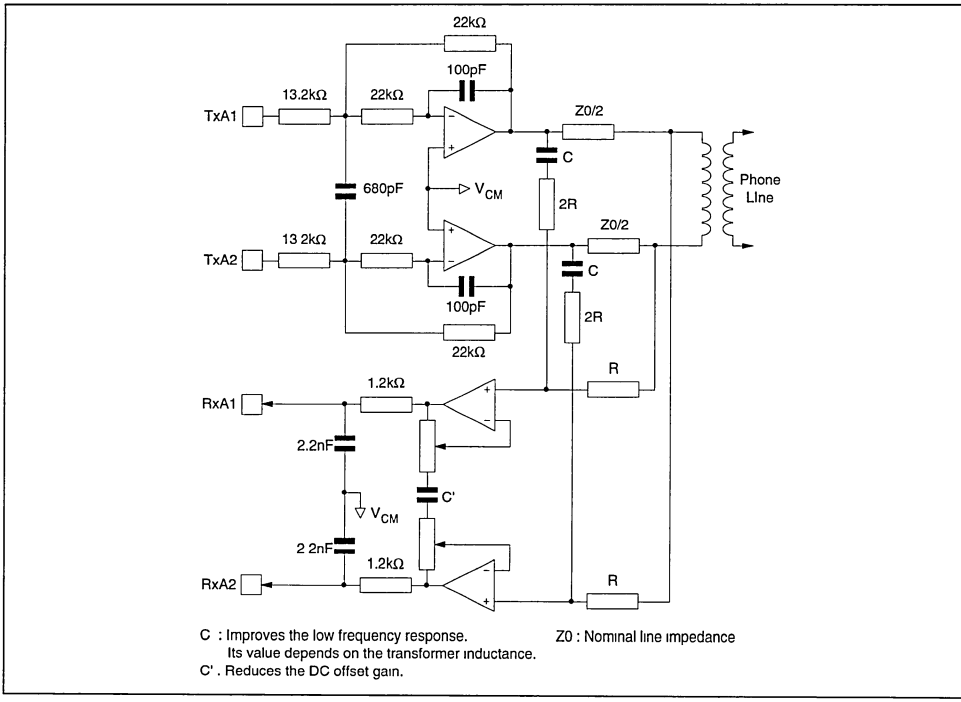
X.1 - MULTI-STANDARD MODEM WITH ECHO CANCELLING

Figure 15 : Multistandard Modem with Echo Cancelling Capability



X.2 - LINE INTERFACE

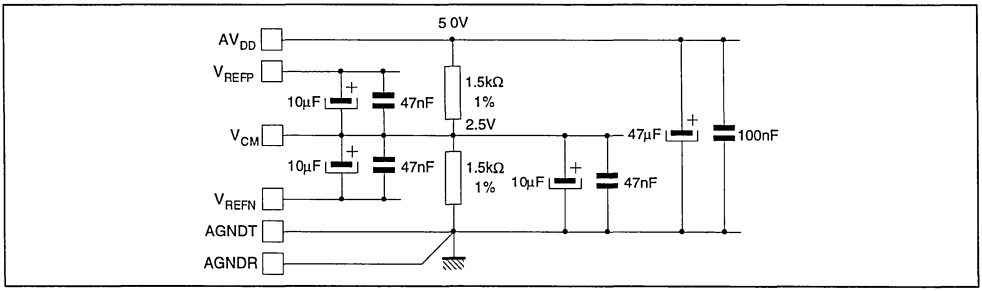
Figure 16 : Differential Duplexer



X - TYPICAL APPLICATIONS (continued)

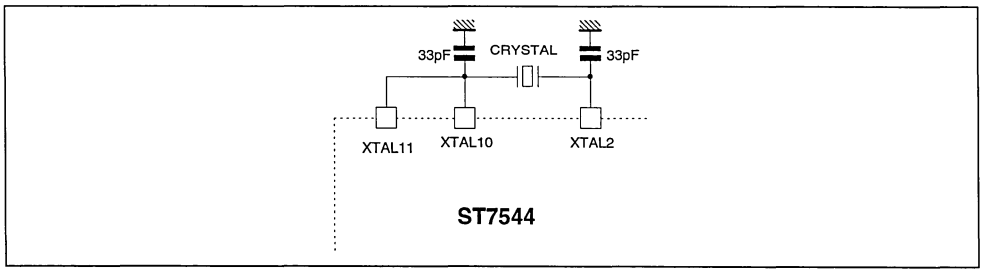
X.3 - COMMON MODE VOLTAGE GENERATION AND DECOUPLING

Figure 17 : Voltage Decoupling



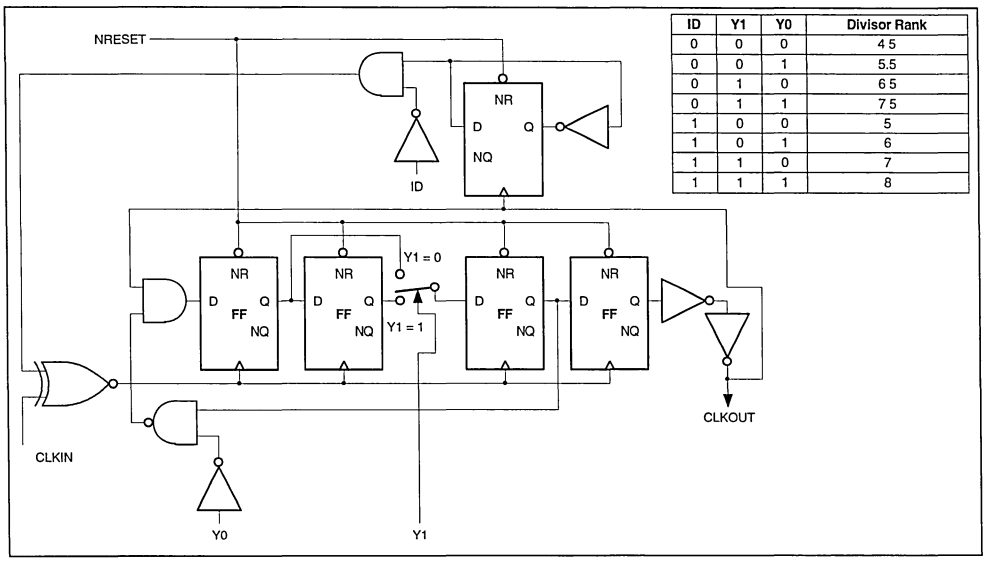
X.4 - CRYSTAL OSCILLATOR

Figure 18 : External Components for Crystal Oscillator



X.5 - EXAMPLE OF PROGRAMMABLE EXTERNAL HALF-INTEGER DIVIDER

Figure 19 : Programmable Divider by 4.5, 5.5, 6.5, 7.5, 8



ID	Y1	Y0	Divisor Rank
0	0	0	4 5
0	0	1	5.5
0	1	0	6 5
0	1	1	7 5
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

XI - ANNEXE A

XI.1 - IIR FILTER OPERATION

Each IIR filtering section included in the ST7544 can perform up to seven biquadratic transfer functions in cascade, operating at four times the sampling frequency (see Figure A1).

Each biquad is defined by five coefficients, A, B, C, D and E (see Figure A2). An additional coefficient ,F, scales the IIR filter output.

Unused biquads are made transparent by programming A to one and the four remaining coefficients to zero. Such biquads should preferably be located in the first sections of the IIR filter in order to reduce the calculation noise.

XI.1.1 - Coefficient Rounding

Initially, coefficients of the filter to be implemented must be exclusively between +2 and -2. To derive the actual usable 12+1 bit coefficients, the rounding process described in Figure A3 must be performed.

Each 13 bit coefficient K is split into its doubling factor K2, and its 12 bit basic value K1, as the IIR architecture works with 12 bit coefficients and uses an extra accumulation when coefficient doubling is needed.

$$K2 \in [0,1] \text{ and } -2^{12} < K1 < +2^{12}$$

The coefficients are loaded into the different IIR filters through 16 bit wide time slots. The format to be used is as follows :

MSB	K1	LSB
K2	(12-bit)	0 0 0
(1 bit)		(3-bit)

<--------- 16 bit word -------->

To programme one IIR filter it is necessary to send five words per biquad followed by two additional words set to zero and the F coefficient word :

B(1), C(1), A(1), D(1), E(1), B(2),..., E(7), 0000_H, 0000_H, F

The total number of words sent is therefore 38.

XI.1.2 - Detailed Operation

The architecture of the device supporting the IIR filter is based on 28 bit data path. The basic function is as follows: one coefficient K(N) is multipled by one sample X(N) followed by one accumulation with value clampling. It can be precisely described as follows :

FUNCTION PAC K(N), X(N), S
LOCAL P
P = **TRUNC** (K1(N) x X(N)/2^{12})
S = S + P
IF ABS(S) > 2^{27} **THEN**
IF SIGN(S) > 0 **THEN CLAMP** S **TO** 2^{27}-1
ELSE CLAMP S **TO** 2^{27}

IF K2(N) = 1 **THEN** S = S + P
IF ABS(S) > 227 **THEN**
IF SIGN(S) > 0 **THEN CLAMP** S **TO** 2^{27}-1
ELSE CLAMP S **TO** 2^{27}

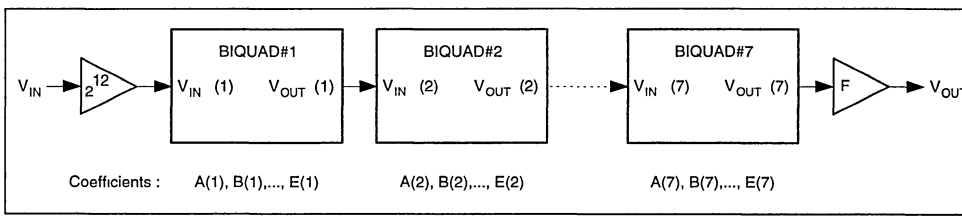
END OF FUNCTION

The TRUNC function is a two's complement truncature.

As previously mentionned, the second accumulation is controlled by the doubling factor K2(N).

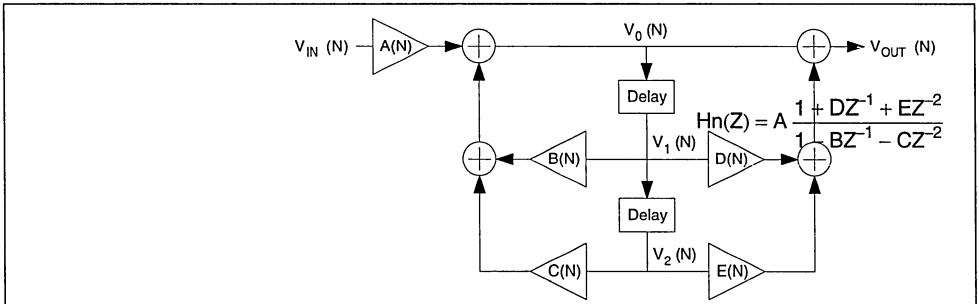
The complete process of computing 16 bit output samples (V_{OUT}) from 16 bit input samples (V_{IN}) appears in Figure A4.

Figure A1 : IIR Filter Diagram



XI - ANNEXE A (continued)

Figure A2 : BIQUAD Structure

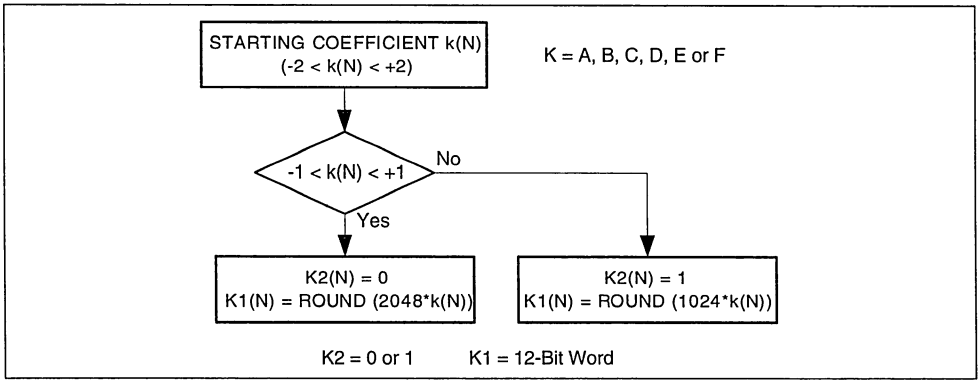


Equation Set : $V_0(N) = B(N) \times V_1(N) + C(N) \times V_2(N) + A(N) \times V_{IN}(N)$ N = BIQUAD NUMBER (1:7)
$V_{OUT}(N) = V_0(N) + D(N) \times V_1(N) + E(N) \times V_2(N)$

Next Step with : $V_2(N) = V_1(N)$
$V_1(N) = V_0(N)$

7544-23 EPS

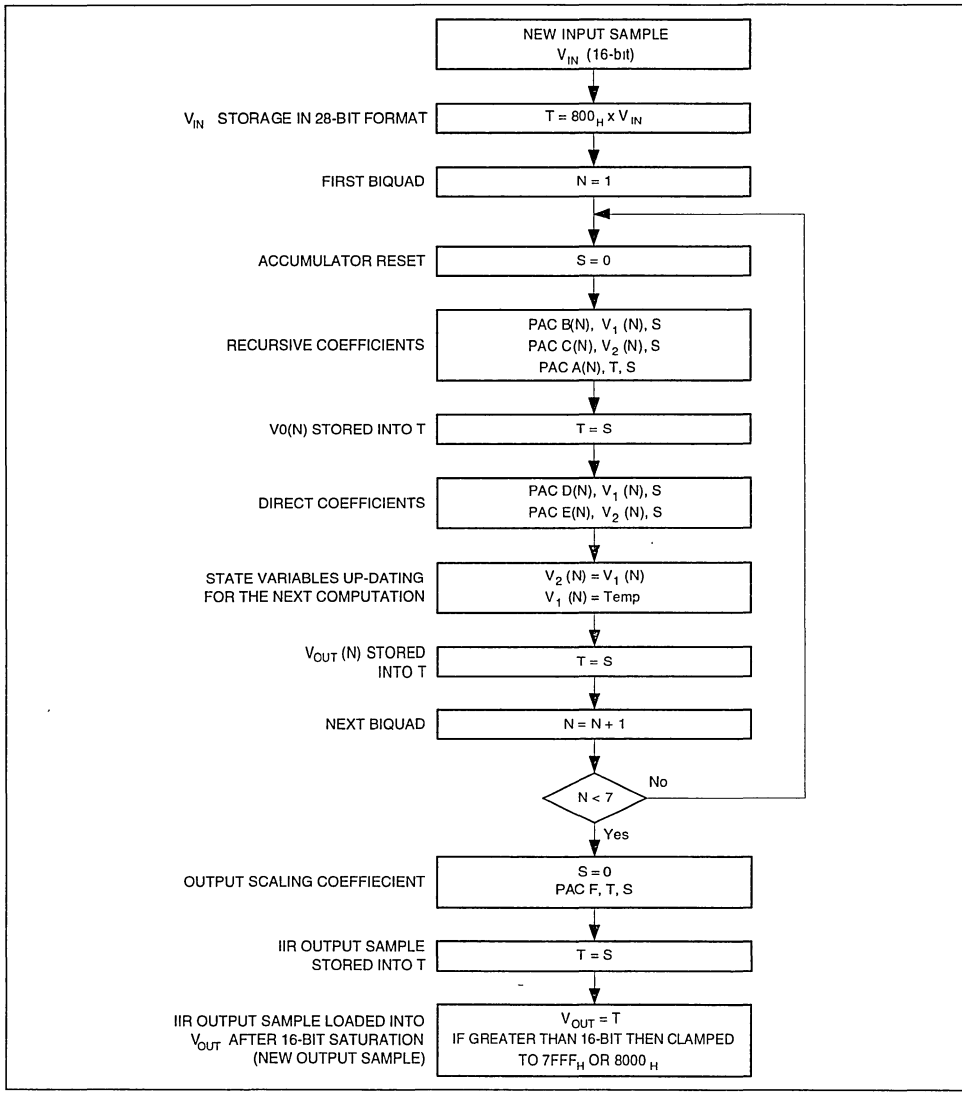
Figure A3 : IIR Coefficients Rounding



7544-24 EPS

XI - ANNEXE A (continued)

Figure A4 : IIR Operating Sequence



SGS-THOMSON MICROELECTRONICS

ST7546

SIMPLIFIED V.34 ANALOG FRONT END

PRELIMINARY DATA

- GENERAL-PURPOSE SIGNAL PROCESSING ANALOG FRONT END (AFE)
- TARGETED FOR V.34 MODEM AND BUSINESS AUDIO APPLICATIONS
- 16-BIT OVERSAMPLING ΣΔ A/D AND D/A CONVERTERS
- 80dB SIGNAL-TO-(NOISE+DISTORTION) RATIO FOR SAMPLING FREQUENCY (FS) UP TO 22.5kHz @5V
- MAX SAMPLING FREQUENCY : 45kHz
- PROGRAMMABLE ADC AND DAC OVERSAMPLING FREQUENCIES. OVERSAMPLING FREQUENCY = N x 32 x FS, N = 2, 3, 4, 5, 6. THE OVERSAMPLING FREQUENCY CAN BE FROM 0.5MHz TO 2.88MHz
- FILTER BANDWIDTHS : 0.425 x THE SAMPLING FREQUENCY
- ON-CHIP REFERENCE VOLTAGE
- DIFFERENTIAL OUTPUT WITH PROGRAMMABLE ATTENUATION : 0dB, 6dB OR INFINITE
- TWO SETS OF DIFFERENTIAL INPUTS WITH PROGRAMMABLE GAINS OF 0dB AND 6dB
- 16-BIT SYNCHRONOUS SERIAL INTERFACE WHOSE OPERATION IS EITHER HARDWARE OR SOFTWARE CONTROLLABLE
- SINGLE POWER SUPPLY RANGE : 5V ±5% OR DOUBLE POWER SUPPLY : +3.3 TO 5V ±5% DIGITAL PART ; 5.0V ±5% ANALOG PART
- LOW POWER CONSUMPTION : 100mW OPERATING POWER AT THE NOMINAL FREQUENCY OF 1.536MHz AND 5.0V SINGLE SUPPLY (70mW @ 3.3V). LESS THAN 50µW IN THE LOW POWER MODE WHEN THE MCLK NOT RUNNING
- 0.8µm CMOS PROCESS
- TQFP44 AND PLCC28 PACKAGES

DESCRIPTION

The ST7546 is a high-resolution analog-to-digital and digital-to-analog converter targeted for V.34 modem and consumer audio applications.

This device has a 16-bit oversampling ADC and DAC, filters and control logic for the serial interface. The oversampling frequencies for the ADC and DAC are user programmable.

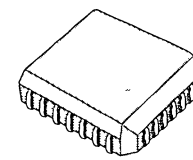
The device operation is controlled by reading the 16-bit information control register.

The major functions of the ST7546 are :

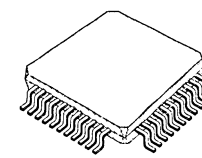
- To convert the audio-signal to 16-bit 2's complement data format through the ADC channel.
- To communicate with an external digital signal processor via serial interface logic.
- To convert 16-bit 2's complement data from a digital signal processor to an audio signal through the DAC channel.

The ST7546 consists of two signal-processing channels, an ADC channel and a DAC channel, and the associated digital control. The two channels operate synchronously so that the transmitted data to the DAC channel and received data from the ADC channel occur during the same time interval. The data transfer is in 2s complement format.

To save power, e.g. in lap-top modem applications, the low-power reset mode can be used to reduce the power consumption to less than 1mW.



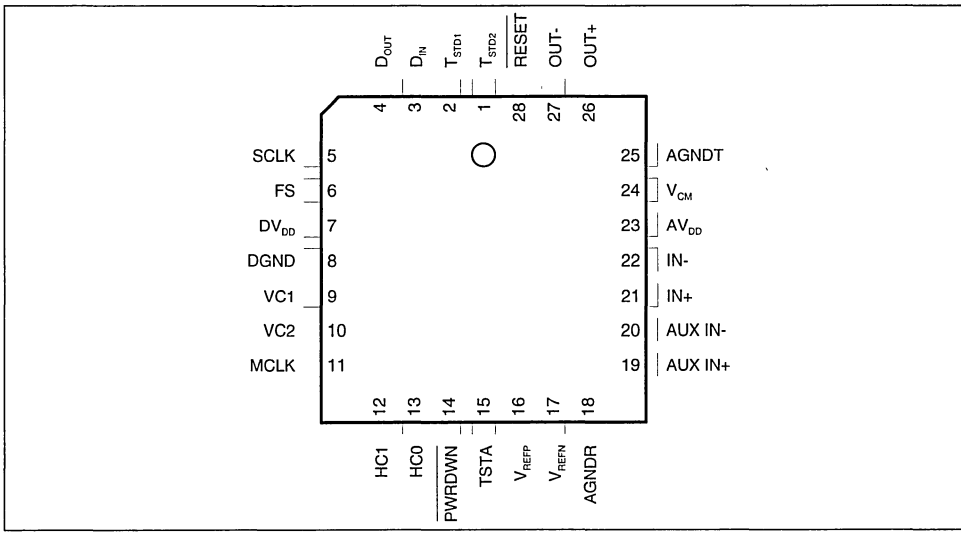
PLCC28
(Plastic Package)



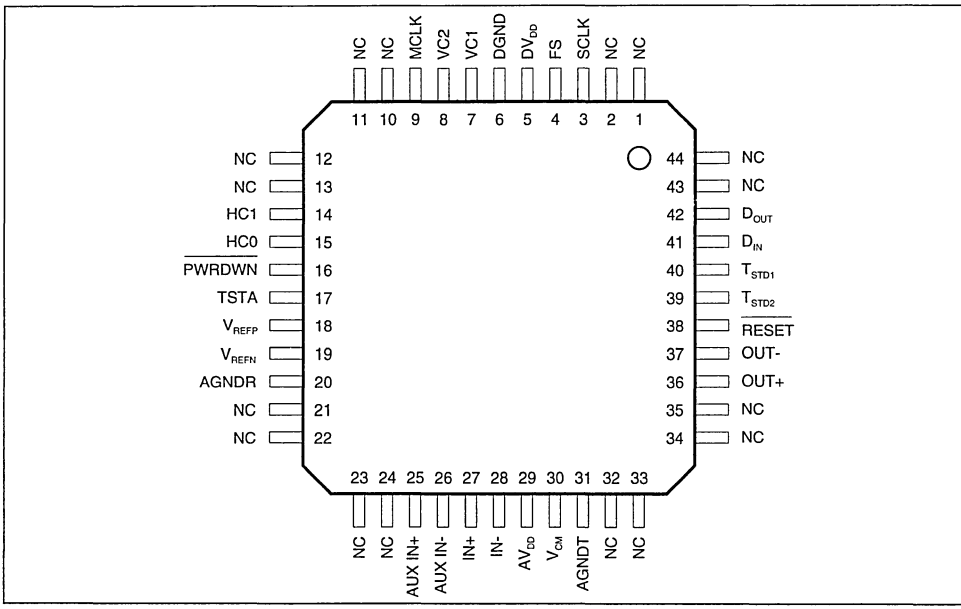
TQFP44
(Plastic Quad Flat Package)

PIN CONNECTIONS

ST7546 Top View (PLCC28)



ST7546 Top View (TQFP44)



PIN LIST

Name	Pin Number		Type	Description
	PLCC28	TQFP44		
SCLK	5	3	O	Shift Clock Output
FS	6	4	O	Frame Synchronization Output
DV_{DD}	7	5	I	Positive Digital Power Supply (+3.15V to 5.25V)
DGND	8	6	I	Digital Ground (0V)
VC1	9	7	O	Voltage Control (should be tied to ground through a 1MΩ resistor)
VC2	10	8	O	Voltage Control (should be tied to ground through a 47nF capacitor)
MCLK	11	9	I	Master Clock Input (equal to the ADC and DAC oversampling frequency)
HC1	12	14	I	Hardware Control Input
HC0	13	15	I	Hardware Control Input
$\overline{PWRDWN}$	14	16	I	Power-down Input
TSTA	15	17	O	Analog Output Reserved for Test
V_{REFP}	16	18	O	16-bit DAC and ADC Positive Reference Voltage
V_{REFN}	17	19	O	16-bit DAC and ADC Negative Reference Voltage
AGNDR	18	20	I	Analog Ground (0V)
AUX IN+	19	25	I	NonInverting Input to Auxiliary Analog Input
AUX IN-	20	26	I	Inverting Input to Auxiliary Analog Input
IN+	21	27	I	NonInverting Input to Analog Input Amplifier
IN-	22	28	I	Inverting Input to Analog Input Amplifier
AV_{DD}	23	29	I	Positive Analog Power Supply (5V ±5%)
V_{CM}	24	30	O	Common Mode Voltage Output (AV_{DD}/2 ±5%)
AGNDT	25	31	I	Analog Ground (0V)
OUT+	26	36	O	Noninverting Smoothing Filter Output.
OUT-	27	37	O	Inverting Smoothing Filter Output.
$\overline{RESET}$	28	38	I	Reset Function to Initialize the Internal Counters
T_{STD2}	1	39	I	Digital Input Reserved for Test.
T_{STD1}	2	40	O	Digital Output Reserved for Test
D_{IN}	3	41	I	Serial Data Input
D_{OUT}	4	42	O	Serial Data Output

7546-01 TBL

PIN DESCRIPTION

1 - POWER SUPPLY (5 pins)

1.1 - Analog V_{DD} Supply (AV_{DD})

This pin is the positive analog power supply voltage (4.75V to 5.25V) for the DAC and the ADC section. It is not internally connected to digital V_{DD} supply (DV_{DD}).

In any case the voltage on this pin must be higher or equal to the voltage of the Digital power supply (DV_{DD}).

1.2 - Digital V_{DD} Supply (DV_{DD})

This pin is the positive digital power supply for DAC and ADC digital internal circuitry.

1.3 - Analog Ground (AGNDT, AGNDR)

These pins are the ground return of the analog DAC (ADC) section.

1.4 - Digital Ground (DGND)

This pin is the ground for DAC and ADC internal digital circuitry.

Notes : 1. To obtain published performance, the analog V_{DD} and Digital V_{DD} should be decoupled with respect to Analog Ground and Digital Ground, respectively. The decoupling is intended to isolate digital noise from the analog section ; decoupling capacitors should be as close as possible to the respective analog and digital supply pins.

2. All the ground pins must be tied together. In the following section, the ground and supply pins are referred to as GND and V_{DD}, respectively.

2 - HOST INTERFACE (8 pins)

2.1 - Data In (D_{IN})

In Data Mode, the data word is the input of the DAC channel. In Control Mode, the data word is followed by the control register word.

2.2 - Data Out (D_{OUT})

In Data Mode, the data word is the ADC conversion result. In Control Mode, the data word is followed by the register read.

2.3 - Frame Synchronization (FS)

The frame synchronization signal is used to indicate that the device is ready to send and receive data. The data transfer begins on the falling edge of the frame-sync signal. The frame-sync is generated internally and goes low on the rising edge of SCLK.

2.4 - Serial Bit Clock (SCLK)

Clocks the digital data into D_{IN} and out of D_{OUT} during the frame synchronization interval. The Serial bit clock is generated internally and equal to the Master clock signal frequency.

2.5 - Reset Function ($\overline{\text{RESET}}$)

The reset function is to initialize the internal counters and control register. A minimum low pulse of 100ns is required to reset the chip. This reset function initiates the serial data communications. The reset function will initialize all the registers to their default value and will put the device in a pre-programmed state. After a low-going pulse on $\overline{\text{RESET}}$, the device registers will be initialized to provide an over-sampling ratio equal to 160, the serial interface will be in data mode, the DAC attenuation will be set to infinite, the ADC gain will be set to 0dB, the Differential input mode on the ADC converter will be selected, and the multiplexor will be set on the main inputs IN+ and IN-. After a reset condition, the first frame synchronization corresponds to the primary channel.

2.6 - Power Down ($\overline{\text{PWRDWN}}$)

The Power-Down input powers down the entire chip (<50µW). When $\overline{\text{PWRDWN}}$ pin is taken low, the device powers down such that the existing internally programmed state is maintained. When $\overline{\text{PWRDWN}}$ is driven high, full operation resumes after 1ms.

If the $\overline{\text{PWRDWN}}$ input is not used, it should be tied to V_{DD}.

2.7 - Hardware Control (HC0, HC1)

These two pins are used for Hardware/Software Control of the device. The data on HC0 and HC1 will be latched on to the device on the rising edge of the Frame Synchronization Pulse. If these two pins are low, Software Control Mode is selected. When in Software Control Mode, the LSB of the 16-bit word will select the Data Mode (LSB = 0) or the Control Mode (LSB = 1). Other combinations of HC0/HC1 are for Hardware Control. These inputs should be tied low if not used.

3 - CLOCK SIGNALS (3 pins)

3.1 - Master Clock (MCLK)

Master clock input. This signal is the oversampling clock of the D/A and A/D convertor. It also provides all the clocks of the serial interface. This input may be driven by a CMOS signal with a frequency from 0.5MHz up to 2.88MHz (maximum).

3.2 - Voltage Control (VC1, VC2)

The voltage control output from the internal PLL. The VC2 should be tied to ground through a capacitor and the VC1 should be tied to ground through a resistor.

PIN DESCRIPTION (continued)

4 - ANALOG INTERFACE (9 pins)

4.1 - DAC and ADC Positive Reference Voltage Output (V_{REFP})

This pin provides the Positive Reference Voltage used by the 16-bit converters. The reference voltage, V_{REF}, is the voltage difference between the V_{REFP} and V_{REFN} outputs, and its nominal value is 2.5V. V_{REFP} should be externally decoupled with respect to V_{CM}.

4.2 - DAC and ADC Negative Reference Voltage Output (V_{REFN})

This pin provides the Negative Reference Voltage used by the 16-bit converters, and should be externally decoupled with respect to V_{CM}.

4.3 - Common Mode Voltage Output (V_{CM})

This output pin is the common mode voltage (AV_{DD} - AGND)/2. This output must be decoupled with respect to GND.

4.4 - Non-inverting Smoothing Filter Output (OUT+)

This pin is the non-inverting output of the fully differential analog smoothing filter.

4.5 - Inverting Smoothing Filter Output (OUT-)

This pin is the inverting output of the fully differential analog smoothing filter. Outputs OUT+ and OUT- provide analog signals with maximum peak to peak amplitude 2 x V_{REF}, and must be followed by an external two pole smoothing filter. The external filter follows the internal single pole switch capacitor filter. The cutoff frequency of the external filter must be greater than two times the sampling frequency (FS), so that the combined frequency response of both the internal and external filters is flat in the passband . The attenuator of the last output stage can be programmed to 0dB, 6dB or infinite.

4.6 - Non-inverting Analog Input (IN+)

This pin is the differential non-inverting ADC input.

4.7 - Inverting Analog Input (IN-)

This pin is the differential inverting ADC input. These analog inputs (IN+, IN-) are presented to the Sigma-Delta modulator via a multiplexer. The analog input peak to peak differential signal range must be less than 2 x V_{REF}, and must be preceded by an external single pole anti-aliasing filter. The cut-off frequency of the filter must be lower than one half the over-sampling frequency (MCLK). These filters should be set as close as possible to the IN+ and IN- pins. The gain of the first stage is 0dB and can be programmed to 6dB in differential hardware configuration.

4.8 - Non-inverting Auxiliary Analog Input (AUX IN+)

This pin is the differential non-inverting auxiliary ADC input. The characteristics are same as the IN+ input.

4.9 - Inverting Auxiliary Analog Input (AUX IN-)

This pin is the differential inverting auxiliary ADC input. The characteristics are same as the IN- input. The input pair (IN+/IN- or AUX IN+/AUX IN-) are software selectable.

5 - TEST (3 pins)

5.1 - Test Outputs (TSTD1)

Digital output reserved for test. Can be left open.

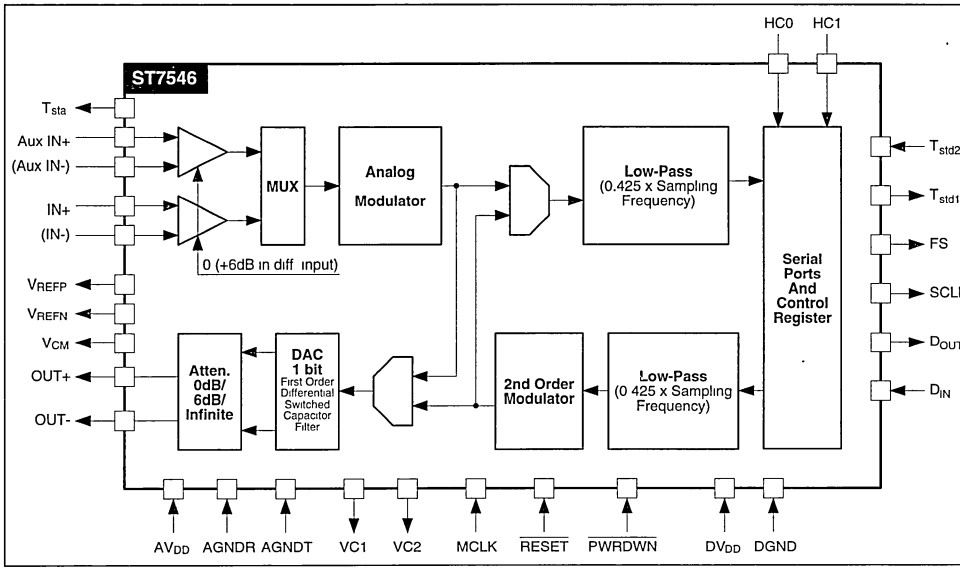
5.2 - Test Input (TSTD2)

Digital input reserved for test.Should be connected to GND.

5.3 - Analog Test Output (TSTA)

Analog output reserved for test. Can be left open.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1 - TRANSMIT D/A SECTION

The functions included in the Tx D/A section are detailed hereafter.

16-bit 2's complement data format is used in the DAC channel.

1.1 - Transmit Low Pass Filters

The transmit low pass filter is basically an interpolating filter. It is a combination of Finite Impulse Response filter (FIR) and an Infinite Impulse Response filter (IIR).

The digital signal from the serial interface gets interpolated by 2, 3, 4, 5 or 6 x Sampling Frequency (FS) through the IIR filter. The signal is further interpolated by 32 x FS x n (with n equal to 2, 3, 4, 5, 6) through the IIR and FIR filter. The low pass filter is followed by the DAC. The DAC is oversampled at 64, 96, 128, 160, 192 x FS. The oversampling ratio is user selectable.

1.2 - D/A Converter

The oversampled D/A converter includes a second order digital noise shaper, a one bit D/A converter and a single pole analog low-pass filter.

The gain of the last output stage can be programmed to 0dB, -6dB or infinite attenuation. The cut-off frequency of the single pole switch-capacitor low-pass filter is :

$$fc_{-3dB} = \frac{MCLK}{2 \cdot \pi \cdot 10}$$

with MCLK = Master Clock frequency.

Continuous-time filtering of the analog differential output is necessary using an off-chip amplifier and a few external passive components.

At least 86dB signal to noise plus distortion ratio can be obtained in the frequency band of 0.425 x 9.6kHz (with an oversampling ratio equal to 160).

2 - RECEIVE A/D SECTION

The different functions included in the ADC channel section are described below. 16-bit 2's complement data format is used in the ADC.

2.1 - A/D Converter

The oversampled A/D converter is based on a second order sigma-delta modulator. To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data. Single-ended mode can also be used. The ADC is oversampled at 64, 96, 128, 160 or 192 x FS. The oversampling ratio is user selectable. At least -86dB SNDR can be expected in the 0.425 x 9.6kHz bandwidth with a -6dBr differential input signal and an oversampling ratio equal to 160.

FUNCTIONAL DESCRIPTION (continued)

2.2 - Receive Low Pass Filter

It is a decimation filter. The decimation is performed by two decimation digital filters : one decimation FIR filter and one decimation IIR filter.

The purpose of the FIR filter is to decimate 32 times the digital signal coming from the ADC modulator.

The IIR is a cascade of 5 biquads. It provides the low-pass filtering needed to remove the noise remaining above half the sampling frequency. The output of the IIR will be processed by the DSP.

3 - Clock Generator

The master clock, MCLK is provided by the user. The ADC and DAC are oversampled at the MCLK frequency. MCLK is equal to the shift clock used in the serial interface. The MCLK frequency should be :
MCLK = Oversampling ratio x Sampling frequency

The clock generator provides, via an internal PLL, the clocks needed for the computation in the digital section. The MCLK clock is used by the PLL for the clock reference.

4 - Host Interface

The Host interface consist of the shift clock, the frame synchronization signal, the ADC-channel data output, and the DAC-channel data input.

The ST7546 internally generates the shift clock and frame-sync signal for the serial communication. These signals are derived from the input master clock (MCLK). Two modes of serial transfer are available. The first is the software mode for 15-bit transmit data transfer and 16-bit receive data transfer, and the second is the hardware mode for 16-bit data transfer. Both modes are selected by the Hardware Control pins (HC0, HC1).

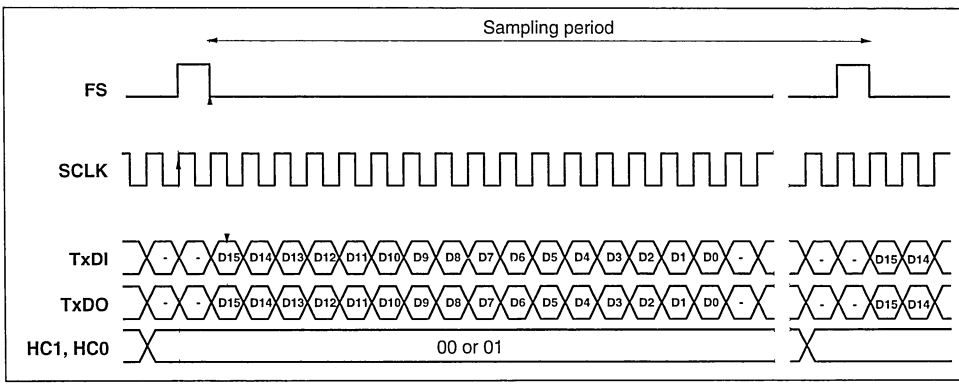
The data to the device, input/output are MSB-first in 2's complement format (see Table 1).

Table 1 : Mode Selection

HC1	HC0	Selected mode
0	0	Software mode Data/control through the LSB of the 16-bit word. LSB = 0 for data and LSB = 1 for control. At the end of the Secondary Frame Synchronization the device automatically returns to data mode.
0	1	Hardware mode for data transfer only. The 16-bit data word is input to the DAC. The 16-bit data word output is the ADC conversion result (operation equivalent to the software mode with LSB = 0).
1	X	Hardware mode for device programming and control register read. Operation equivalent to the Software mode with LSB = 1 16-bit data is written to or read from the device during Primary Frame Synchronization. During the Secondary Frame Synchronization, the 16-bit control information is input to the device and the 16-bit data word output is the Register read data.

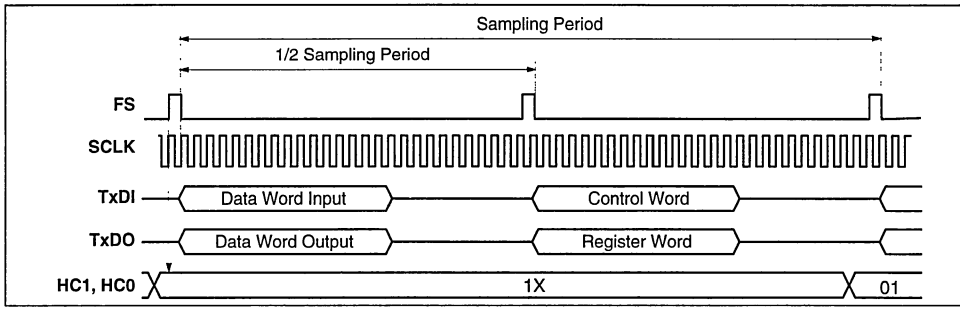
When Control Mode is selected, the device will internally generate an additional Frame Synchronization Pulse (Secondary Frame Synchronization Pulse) at the midpoint of the original Frame Period. The Original Frame Synchronization Pulse will also be referred to as the Primary Frame Synchronization Pulse.

Figure 1 : Data Mode



FUNCTIONAL DESCRIPTION (continued)

Figure 2 : Mixed Mode



5 - Control Register

This section defines the control and device status information. The register programming occurs only during Secondary Frame Synchronization. After a reset condition, the device is always in data mode.

Table 2

Bits	Symbol	Function
0	-	-
1	AUX/MAIN	Auxiliary / Main receive input
2	SING/DIFF	Single-ended /Differential Receive input
3	0VS0	Oversampling bit 0
4	0VS1	Oversampling bit 1
5	0VS2	Oversampling bit 2
6	AT0	Attenuator transmit bit 0
7	AT1	Attenuator transmit bit10
8	-	-
9	RL/RH	Voltage (reference low/reference high)
10	NC1	Not used
11	NC2	Not used
12	TEST0	Test mode bit 0
13	TEST1	Test mode bit 1
14	TEST2	Test mode bit 2
15	TEST3	Test mode bit 3

Table 3 : Auxiliary/Main Input (AUX/MAIN)

D1	Function
0	Main receive input
1	Auxiliary receive input

Table 4 : Single-ended/Differential Inputs (SING/DIFF)

D2	Function
0	Differential input : +0dBr gain
1	Single-ended input : 0dBr gain Differential input : +6dBr gain

Note : 0dBr = 2 x V_{REF} peak-to-peak signal.

Table 5 : Oversampling Ratio

D5	D4	D3	Function
0	0	0	160
0	0	1	192
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	64
1	1	0	96
1	1	1	128

Table 6 : Transmit Attenuator

D7	D6	Function
0	0	Infinite
0	1	Reserved
1	0	-6dB
1	1	0dB

Table 7 : Reserved Mode

D15	D14	D13	D12	D11	D10	D9	Function
0	0	0	0	0	0	0	Reserved

ELECTRICAL SPECIFICATIONS

Unless otherwise noted, Electrical Characteristics are specified over the operating range.
Typical values are given for V_{DD} = +5V, T_{amb} = 25°C and for nominal Master clock frequency MCLK = 1.536MHz and oversampling ratio = 160.

ABSOLUTE MAXIMUM RATINGS (referenced to GND)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3, 7.0	V
V_I,V_{IN}	Digital or Analog Input Voltage	-0.3, V_{DD}+0.3	V
I_I,I_{IN}	Digital or Analog Input Current	±1	mA
I_O	Digital Output Current	±20	mA
I_{OUT}	Analog Output Current	±10	mA
T_{oper}	Operating Temperature	0, 70	°C
T_{stg}	Storage Temperature	-40, 125	°C
P_{DMAX}	Maximum Power Dissipation	200	mW

DC CHARACTERISTICS (V_{DD} = 5.0V ± 5%, GND = 0V, T_A = 0 to 70°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
POWER SUPPLY AND COMMON MODE VOLTAGE					
SINGLE POWER SUPPLY (DV_{DD} = AV_{DD})					
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DDA}	Analog Supply Current		8.5		mA
I_{DDD}	Digital Supply Current		11.5		mA
I_{DD}-LP	Supply Current in Low Power Mode MCLK Stopped MCLK Running		10 800		µA µA
V_{CM}	Output Common Mode Voltage V_{CM} Output Voltage Load Current (see Note 1)	V_{DD}/2-5%	V_{DD}/2	V_{DD}/2+5%	V
DOUBLE POWER SUPPLY (DV_{DD} # AV_{DD})					
DV_{DD}	Digital Supply Voltage	3.15	3.3	3.45	V
AV_{DD}	Analog Supply Voltage	4.75	5	5,25	V
I_{DDA}	Analog Supply Current		8		mA
I_{DDD}	Digital Supply Current		6		mA
V_{CM}	Output Common Mode Voltage (see Note 1)	V_{DD}/2-5%	V_{DD}/2	V_{DD}/2+5%	V
DIGITAL INTERFACE					
(T_A = 25°C, DV_{DD} = +5V)					
V_{IL}	Low Level Input Voltage			0.8	V
V_{IH}	High Level Input Voltage	DV_{DD}-0.5			V
I_I	Input Current V_I = V_{DD} or V_I = GND	-10	±1	10	µA
V_{OH}	High Level Output Voltage (I_{LOAD} = -1mA)	DV_{DD}-0.5			V
V_{OL}	Low Level Output Voltage (I_{LOAD} = 1mA)			0.4	V
C_{IN}	Input Capacitance		5		pF
(T_A = 25°C, DV_{DD} = +3.3V)					
V_{IL}	Low Level Input Voltage	-0.3		0.5	V
V_{IH}	High Level Input Voltage	DV_{DD}-0.5			V
I_I	Input Current V_I = V_{DD} or V_I = GND	-10	±1	10	µA
V_{OH}	High Level Output Voltage (I_{LOAD} = -600µA)	DV_{DD}-0.5			V
V_{OL}	Low Level Output Voltage (I_{LOAD} = 800µA)			0.3	V

Note : 1. Device is very sensitive to noise on V_{CM} Pin V_{CM} output voltage load current must be DC (<10µA). in order to drive dynamic load, V_{CM} must be buffered. AC variation in V_{CM} current magnitude decrease A/D and D/A performance.

ELECTRICAL SPECIFICATIONS (continued)

DC CHARACTERISTICS

(V_{DD} = 5.0V ± 5%, GND = 0V, T_A = 0 to 70°C unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
ANALOG INTERFACE					
V_{REF} with AV_{DD} = +5V	Differential Reference Voltage Output $V_{REF} = (V_{REFP} - V_{REFN})$	2.4	2.5	2.6	V
Tempco (V_{REF})	V_{REF} Temperature Coefficient		200		ppm/°C
$V_{CMO\ IN}$	Input Common Mode Offset Voltage = [(IN+)+(IN-)]/2 -V_{CM} or [(AUX IN+)+(AUX IN-)]/2 -V_{CM}	-300		300	mV
$V_{DIF\ IN}$	Differential Input Voltage : [(IN+)-(IN-)] ≤ 2 x V_{REF} or [(IN+)-(IN-)] ≤ 2 x V_{REF}		2 x V_{REF}		Vpp
$V_{SIG\ IN}$	Single Ended Input Voltage : IN+ or IN- ≤ V_{REF}		V_{REF}		Vpp
$V_{OFF\ IN}$	Differential Input DC Offset Voltage : IN+ = IN- = V_{CM} (id. AUX IN)	-100		100	mV
$V_{CMO\ OUT}$	Output Common Mode Voltage Offset : (OUT+ + OUT-)/2 - V_{CM} (see Note 2)	-200		200	mV
$V_{DIF\ OUT}$	Differential Output Voltage : OUT+ - OUT- ≤ 2 x V_{REF}		2 x V_{REF}		V
$V_{OFF\ OUT}$	Differential Output DC Offset Voltage : (OUT+ - OUT-)	-100		100	mV
R_{IN}	Input Resistance IN+, IN- (id. AUX IN)	100			kΩ
R_{OUT}	Output Resistance (OUT+, OUT-)			20	Ω
R_L	Load Resistance (OUT+, OUT-)	10			kΩ
C_L	Load Capacitance (OUT+, OUT-)			20	pF
$V_{ADO\ OUT}$	Output A/D Modulator Voltage Offset		10		mV

Note : 2. Device is very sensitive to noise on V_{CM} Pin. V_{CM} output voltage load current must be DC (<10µA). in order to drive dynamic load, V_{CM} must be buffered. AC variation in V_{CM} current magnitude decrease A/D and D/A performance.

AC ELECTRICAL CHARACTERISTICS

(Reference level V_{IL} = 0.8V, V_{IH} = DV_{DD} - 0.5V, V_{OL} = 0.4V, V_{OH} = DV_{DD} - 0.5V, DV_{DD} = 5V, Output load = 50pF unless otherwise)

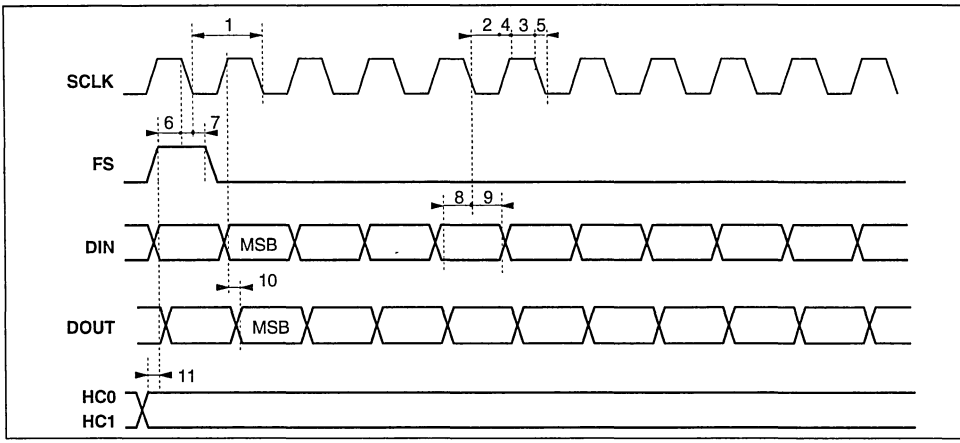
Symbol	N°	Parameter	Min.	Typ.	Max.	Unit
SERIAL CHANNEL TIMING (see Figure 3 for Parameter numbers)						
	1	SCLK Period	300			ns
	2	SCLK Width Low	150			ns
	3	SCLK Width High	150			ns
	4	SCLK Rise Time			10	ns
	5	SCLK Fall Time			10	ns
	6	FS Setup	100			ns
	7	FS Hold	100			ns
	8	DIN Setup	50			ns
	9	DIN Hold	0			ns
	10	DOUT Valid			20	ns
	11	HC0,HC1 Set-up	20			ns

MASTER CLOCK INTERFACE (MCLK) (DV_{DD} = +5V or +3.3V)

MCLK	-	Master Clock Input	0.92	1.54	2.8	MHz
tpw		Master Clock Duty Cycle Pulse Width	360	650		%
tph/tpw		Pulse Width High	45		55	%
tpl/tpw		Pulse Width Low	45		55	%

ELECTRICAL SPECIFICATIONS (continued)

Figure 3 : Serial Interface Timing Diagram



TRANSMIT CHARACTERISTICS

Performance of the Tx Channel

Typical values are given for AV_{DD} = +5V, T_{amb} = 25°C and for nominal master clock MCLK = 1.536MHz, differential mode and oversampling ratio = 160. Measurement band = DC to 0.425 x Sampling frequency.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Gabs	Absolute Gain at 1kHz	-0.5	0	0.5	dB
Ripple	Ripple in Band : 0 to 0.425 x FS (the sinX/X distortion must be corrected in the DSP)		±0.2		dB
THD	Total Harmonic Distortion (differential Tx signal :V_{OUT} = 2.5V_{PP}, f = 1kHz)		-89		dB
DR	Dynamic Range (f = 1kHz) (measured over the full 0 to FS/2 with a -20dBr output signal and extrapolated to full scale) (see Note 3)		94		dB
PSRR	Power Supply Rejection Ratio (f = 1kHz, V_{AC} = 200mV_{PP})		50		dB
CRxTx	Crosstalk (transmit channel to receive channel)		90		dB

Smoothing Filter Transfer Characteristics

The cut-off frequency of the single pole switch-capacitor low-pass filter following the DAC is :

$$fc_{-3dB} = \frac{n \cdot 32 \cdot FS}{2 \cdot \pi \cdot 10} \quad \text{with } n = 2, 3, 4, 5, 6.$$

RECEIVE CHARACTERISTICS

Performance of the Rx Channel

Typical values are given for AV_{DD} = +5V, T_{amb} = 25°C and for nominal master clock MCLK = 1.536MHz, differential mode and oversampling ratio = 160. Measurement band = DC to 0.425 x Sampling Frequency.

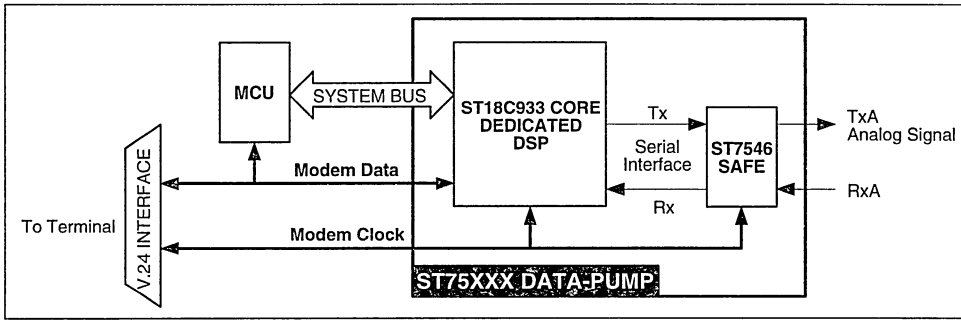
Symbol	Parameter	Min.	Typ.	Max.	Unit
Gabs	Absolute Gain at 1kHz	-0.5	0	0.5	dB
Ripple	Ripple in Band : 0 to 0.425 x FS		±0.2		dB
THD	Total Harmonic Distortion (differential Rx signal : V_{IN} = 2.5V_{PP}, f = 1kHz)		-89		dB
DR	Dynamic Range (f = 1kHz) (measured over the full 0 to FS/2 with a -20dBr input and extrapolated to full scale) (see Note 3)		94		dB
PSRR	Power Supply Rejection Ratio (f = 1kHz, V_{AC} = 200mV_{PP})		50		dB
CTxRx	Crosstalk (transmit channel to receive channel)		90		dB

Note : 3. The dynamic range can be measured in bit with : $N_{bit} = \frac{DR - 1.76}{6.02}$ with DR in dB.

TYPICAL APPLICATIONS

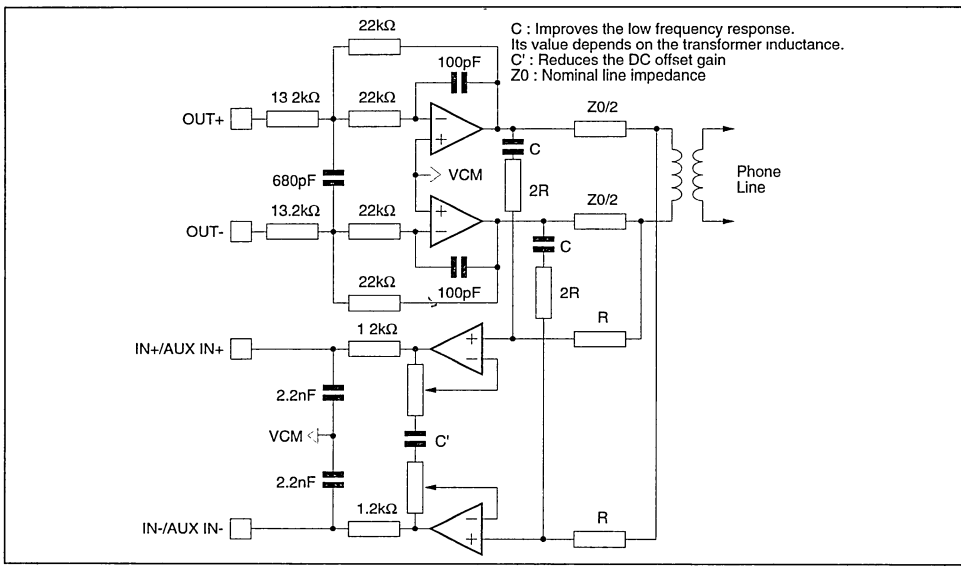
Multi-Standard Modem with Echo Cancelling

Figure 4



Line Interface - Differential Duplexor

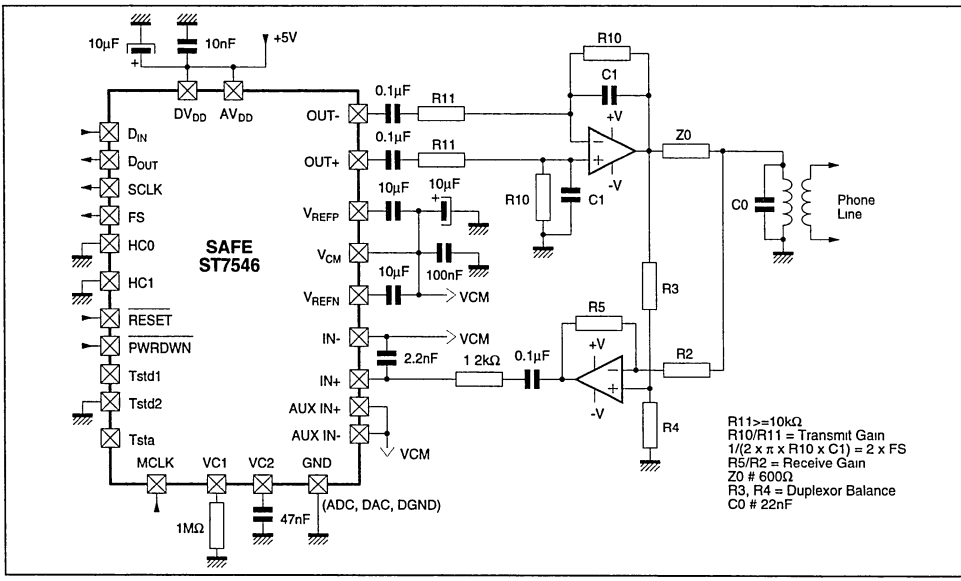
Figure 5



TYPICAL APPLICATIONS (continued)

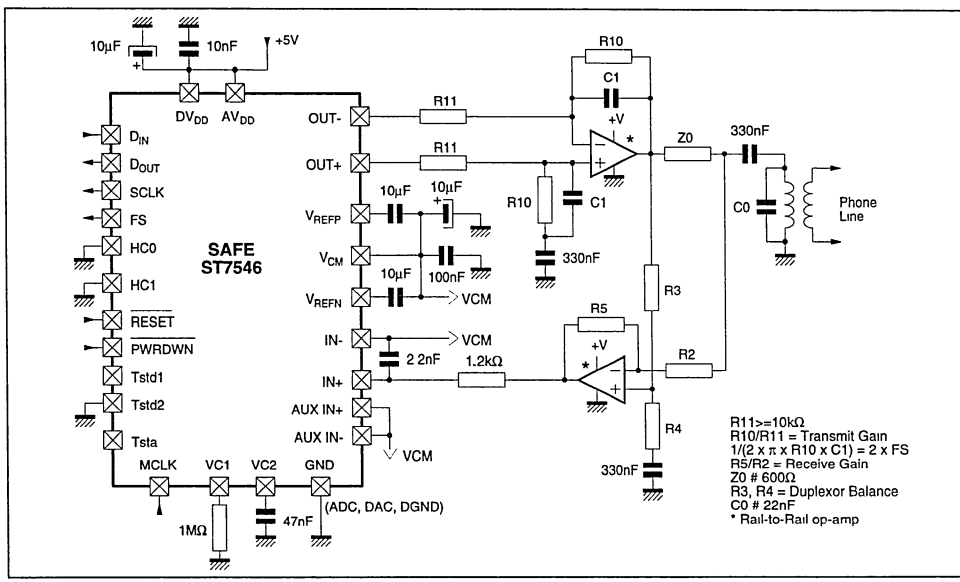
Line Interface - Low-Cost Duplexor

Figure 6



Line Interface - Low-Cost Duplexor Mono Supply

Figure 7



DEFINITION AND TERMINOLOGY

Data Transfer Interval	The time during which data is transfered from D_{OUT} and to D_{IN}. This interval is 16 shift clocks provides by the chip.
Signal Data	This refers to the input signal and all the converted representations through the ADC channel and the DAC channel.
Data Mode	This refers to the data transfer. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Control Mode	This refers to the digital control data transfer into DIN and the register read data from D_{OUT}. The control mode interval occurs when requested by hardware or software.
Frame Sync.	Frame sync refers only to the falling edge of the signal which initiates the data transfer interval. The primary frame sync starts the Data Mode and the secondary frame sync starts the Control Mode.
Frame Sync and Sampling Period	The time between falling edges of successive primary frame sync signals.
ADC Channel	This term refers to all signal processing circuits between the analog input and the digital conversion result at D_{OUT}.
DAC Channel	This term refers to all signal processing circuits between the digital data word applied to D_{IN} and the differential output analog signal available at OUT+ and OUT- pins.
OverSampling Ratio	This term refer to the ratio between the master clock MCLK corresponding to the oversampling frequency and the sampling frequency FS.
Resolution	The number of bits in the input words to the DAC, and the output words in the ADC.
Dynamic Range	The S/(N+D) with a 1kHz, -20dBr input signal and extrapolated to full scale. Use of a small input signal reduces the harmonic distortion components of the noise to insignificance. Units in dB or in N_{bit} as explained before.
Signal-to-(Noise+Distortion)	S/(THD+N) is the ratio of the rms of the input signal to the rms of all other spectral components within the measurement bandwidth (0.425 x Sampling Frequency). Units in dB.
Crosstalk	The amount of 1kHz signal present on the output of the grounded input channel with 1kHz 0dB signal present on the other channel. Units in dB.
Powersupply Rejection Ratio	PSSR. The amount of 1kHz signal present on the output of the grounded input channel with 1kHz 200mV_{PP} signal present on the power supply.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

ST7544 - UNIVERSAL ANALOG FRONT-END

By Joël HULOUX

SUMMARY **Document page**

I - ST7544

I.1 - FEATURES

- FULL ECHO CANCELLING CAPABILITY
- FULLY COMPATIBLE WITH THE ST7543 (7543 mode)
- 16-BIT OVERSAMPLING A/D AND D/A CONVERTERS
  - Programmable down-sampling frequency from 7200 to 16000Hz
  - Sampling frequency can be 3, 4, 6, 8, 12, 16 x Symbol rate
  - Programmable Over sampling frequency (128 or 160 x Sampling frequency)
  - The ST7544 can work with external oversampling clocks
  - Programmable Symbol rate (600, 1200, 1600, 2400, 2560, 2743, 2800, 2954, 3000, 3200, 3429 and 3491)
  - Bit rates of 300 bps, 600bps, 1200 and all multiples of 2400 bps up to 28800 bps can be generated
  - Dynamic range : 92dB with a sampling frequency 9600Hz, Oversampling ratio 160
  - Total harmonic distortion : -89dB
- ON CHIP REFERENCE VOLTAGE
- THREE PROGRAMMABLE DIGITAL FILTERS SECTIONS :
  - Tx interpolation filter
  - Rx decimation filter
    Up to 14th order each
  - Rx reconstruction filter
    Coefficients loaded into RAM
- ANCILLARY CONVERTERS FOR EYE-DIAGRAM MONITORING
- CLOCK SYSTEM BASED ON DIGITAL PHASE LOCKED LOOPS
  - Separate Tx DPLL and Rx DPLL
  - Terminal clock input for Tx synchronization on all multiples of 2400Hz (V.Fast synchronization mode) or on sub-multiple of baud rate (7543 synchronization mode)
  - Bit, Baud, Sampling and Highest synchronous clock outputs
  - Maximum master clock frequency is 38MHz
- SINGLE OR DUAL SYNCHRONOUS SERIAL INTERFACE TO DSP
- SINGLE POWER SUPPLY VOLTAGE : +5V
- LOW POWER CONSUMPTION :
  - 260mW operating power at the nominal crystal frequency of 36.864MHz
  - 160mW operating power at the crystal frequency of 18.432MHz
  - Less than 5mW in the LOW-POWER RESET MODE
- 1.2MM CMOS PROCESS
- 44-PIN PLCC OR
  44-PIN TPQFP (1.4mm body thickness)

I.1 - GENERAL DESCRIPTION

The ST7544 is a single chip Analog Front-End (AFE) designed to implement high speed voice-grade Modems up to 28800 bps with echo cancelling capability.

Associated with one or several Digital Signal Processors (DSP), such as the ST189XX family, it provides a powerful solution for the implementation of multi-mode Modems meeting CCITT (V.21, V.22, V.22 bis, V.23, V.26, V.27, V.29, V.32,V.32 bis and V.33) and BELL (103, 202, 212A...) recommendations. It is fully compatible with the ST7543 in 7543 mode and is also well suited emerging applications involving bit rates up to 28800 bps (in the VFast synchronization mode).

The transmit section includes a 16-bit over-sampling D/A converter with a programmable interpolating filter. The receive section includes a 16-bit oversampling A/D converter with two programmable filters (one for decimation and the other for reconstruction). Oversampling ratio is selectable to either 128 or 160. Two additional 8-bit D/A converters allow eyediagram monitoring on a scope for modem performance adjustment.

Two independant clock generator systems are provided, one synchronized on the Tx rate and the other on the Rx rate.

In External Clock Mode, external oversampling clocks can be provided to the chip.

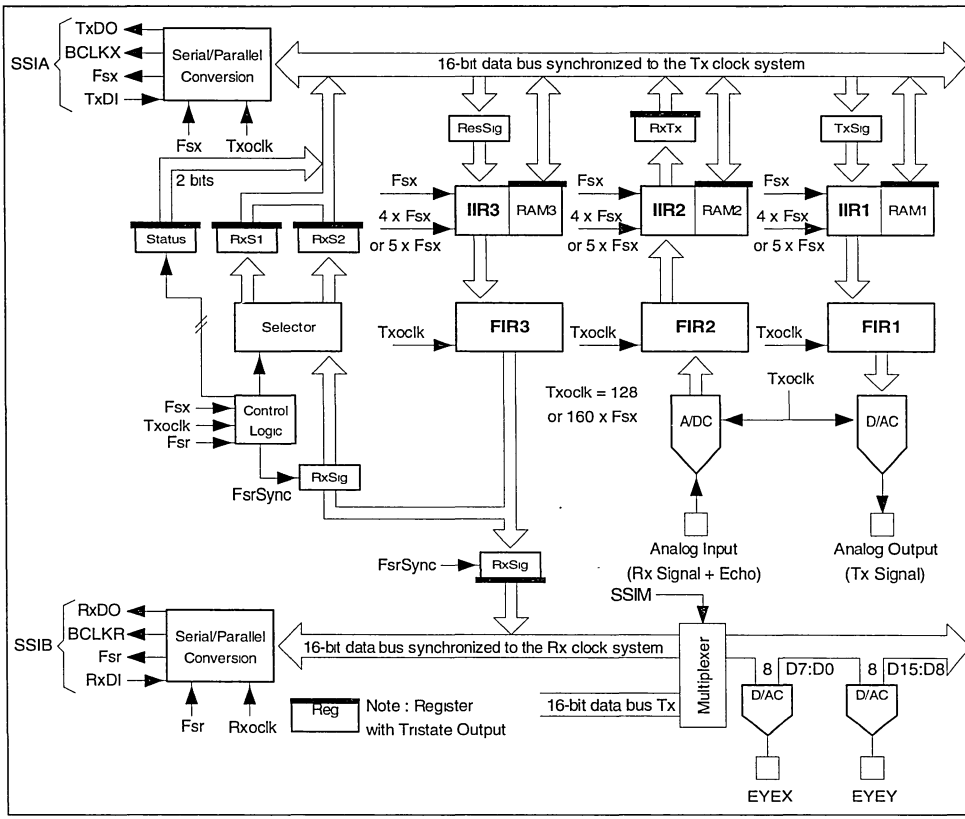
Two independant synchronous serial interfaces (SSI) allow several versatile ways of communicating with standard DSPs.

To save power, e.g. in lap-top modem applications, the lowpower reset mode can be used to reduce the power consumption to less than 5mW.

I.3 - SIGNAL TRANSFER BLOCK DIAGRAM

The ST7544 Block Diagram (Figure 1) illustrates three paths as follows : The Transmit D/A Section, the Receive A/D section and the Receive Reconstruction section.

Figure 1



I.4 - IIR FILTER OPERATION

Each IIR filtering section included in the ST7544 can perform up to seven biquadratic transfer functions in cascade, operating at four times the sampling frequency (see Figure 2).

Each biquad is defined by five coefficients, A, B, C, D and E (see Figure 3). An additional coefficient F, scales the IIR filter output.

Unused biquads are made transparent by programming A to one and the four remaining coefficients to zero. Such biquads should preferably be located in the first sections of the IIR filter in order to reduce the calculation noise.

I.4.1 - Coefficient Rounding

Initially, coefficients of the filter to be implemented must be exclusively between +2 and -2. To derive the actual usable 12+1 bit coefficients, the rounding process described in Figure 4 must be performed.

Each 13 bit coefficient K is split into its doubling factor K2, and its 12 bit basic value K1, as the IIR architecture works with 12 bit coefficients and uses an extra accumulation when coefficient doubling is needed.

$$K2 \in [0,1] \text{ and } -2^{12} < K1 < +2^{12}$$

The coefficients are loaded into the different IIR filters through 16 bit wide time slots. The format to be used is as follows :

MSB	K1	LSB
K2	(12-bit)	0 0 0
(1 bit)		(3-bit)

<--------- 16 bit word -------->

To programme one IIR filter it is necessary to send five words per biquad followed by two additional words set to zero and the F coefficient word :

B(1), C(1), A(1), D(1), E(1), B(2),..., E(7), 0000_H, 0000_H, F

The total number of words sent is therefore 38.

I.4.2 - Detailed Operation

The architecture of the device supporting the IIR filter is based on 28 bit data path. The basic function is as follows: one coefficient K(N) is multipled by one sample X(N) followed by one accumulation with value clampling. It can be precisely described as follows :

FUNCTION PAC K(N), X(N), S
LOCAL P
P = **TRUNC** (K1(N) x X(N)/2^{12})
S = S + P
IF ABS(S) > 2^{27} **THEN**
IF SIGN(S) > 0 **THEN CLAMP** S **TO** 2^{27}-1
ELSE CLAMP S **TO** 2^{27}

IF K2(N) = 1 **THEN** S = S + P
IF ABS(S) > 227 **THEN**
IF SIGN(S) > 0 **THEN CLAMP** S **TO** 2^{27}-1
ELSE CLAMP S **TO** 2^{27}

END OF FUNCTION

The TRUNC function is a two's complement truncature.

As previously mentionned, the second accumulation is controlled by the doubling factor K2(N).

The complete process of computing 16 bit output samples (V_{OUT}) from 16 bit input samples (V_{IN}) appears in Figure 5.

Figure 2 : IIR Filter Diagram

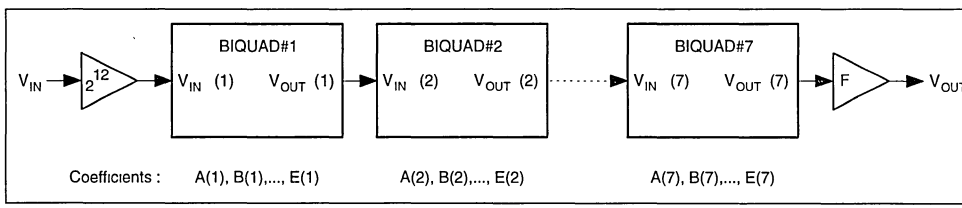
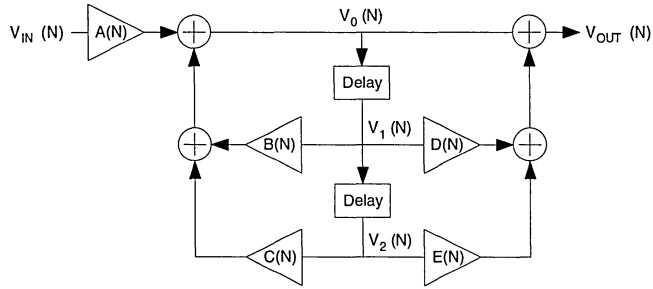


Figure 3 : BIQUAD Structure



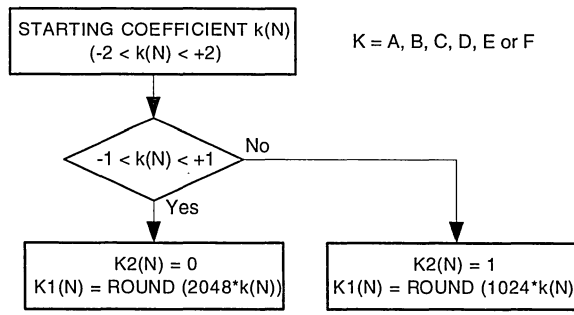
$$Hn(Z) = A\frac{1 + DZ^{-1} + EZ^{-2}}{1 - BZ^{-1} - CZ^{-2}}$$

Equation Set : $V_0(N) = B(N) \times V_1(N) + C(N) \times V_2(N) + A(N) \times V_{IN}(N)$ N = BIQUAD NUMBER (1:7)
$V_{OUT}(N) = V_0(N) + D(N) \times V_1(N) + E(N) \times V_2(N)$

Next Step with : $V_2(N) = V_1(N)$
$V_1(N) = V_0(N)$

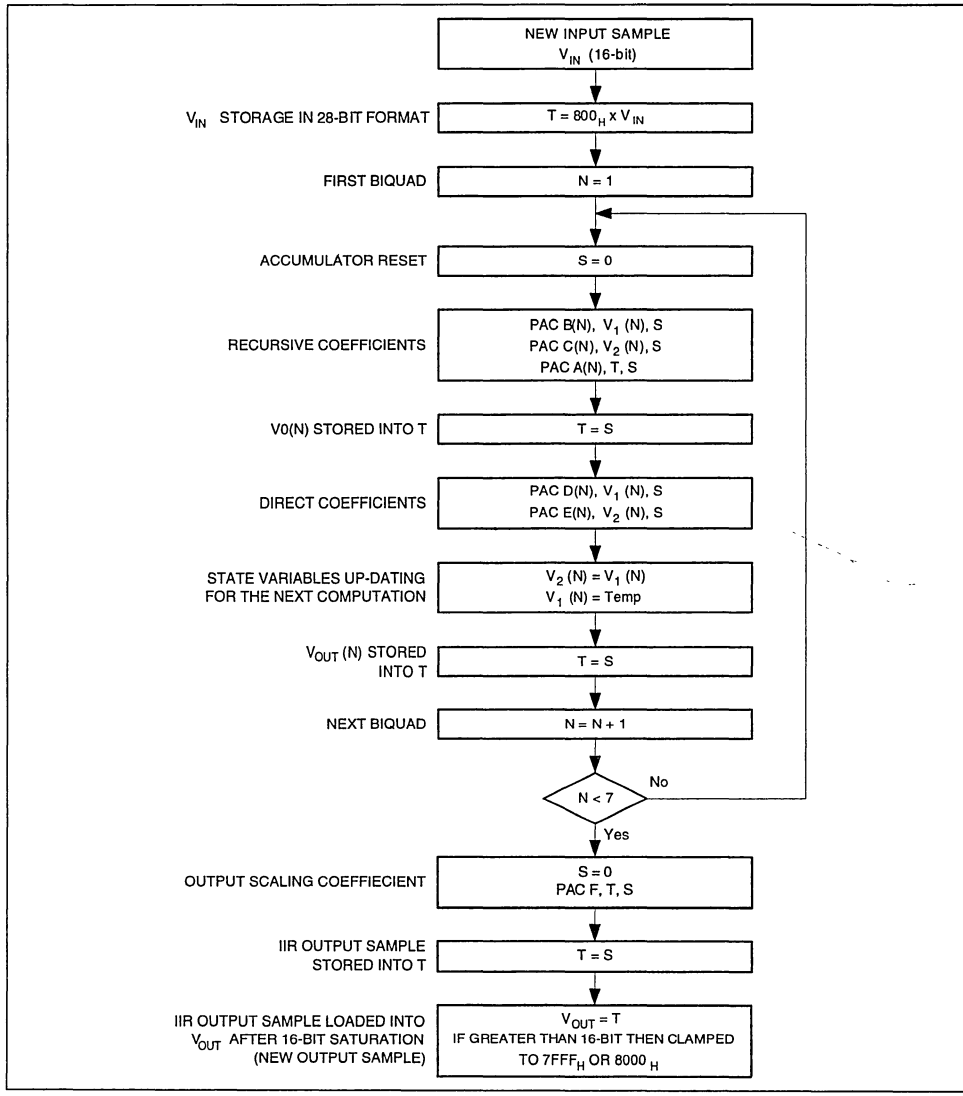
7544-23 EPS

Figure 4 : IIR Coefficients Rounding



7544-24 EPS

Figure 5 : IIR Operating Sequence



I.5. - IIR FILTER PROGRAMMING EXAMPLE

I.5.1 - Example of Configuration

- one external clock : 36.864MHz
- serial port mode : dual
- transmit sampling frequency : 9600Hz
- receive sampling frequency : 9600Hz
- bit frame clock frequency : 160*Fsx(r)
- transmit bit clock frequency : 14400Hz
- receive bit clock frequency : 14400Hz
- transmit baud clock frequency : 2400Hz
- receive baud clock frequency : 2400Hz
- transmit filter : low-pass (spec table 48)
- receive filter : banp-pass spec table 50)
- interpolation filter : low-pass (spec table 43)

I.5.2 Hardware Configuration

- XTAL10 and XTAL11 hard-wired to the external clock
- TxDI and RxDI must be tied to Vdd while the serial interface is not managed by the host processor.
- RC network on NLPR pin.Typically RC=10ms (R=100kΩ ,C=100nF) (This time must include the external clock start-up time,and the ST7544 set up time).
- SSIM pin tied to DV_{DD} : dual serial port mode.
- BFRS pin tied to DV_{DD} : bit frame frequency set to 160 time Fsx(r).

I.5.3 - Software Configuration

Writing convention :

'x'	frame number
FRAME x,1	frame for RAM 1 loading
FRAME x,2	frame for RAM 2 loading
FRAME x,3	frame for RAM 3 loading
'#"	delimits a programmer's remark (comments)
'b'	indicates a binary number
'h'	indicates an hexadecimal number
'XXXX'	user defined

 # SYNCHRONOUS SERIAL INTERFACE A

```
#FRAME 0.1. Select the correct sampling frequency and set Stb bit in order to select a RAM
B9A4h #TxI0     MS =1       coefficient loading mode selected
#               Stb=0       start bit coefficient loading activated
#               QS =1       XTAL 10 selected
#               RAi=11b     no RAM accessed
#               ADi=001b    TxCR1 selected
#               Di =A4h     Fsx=9600Hz, Txrclk=2400Hz
#                           TxHSCLK=12.288MHz
#                           Band split mode inactive
FFFFh#TxI1
FFFFh#TxI2
FFFFh#TxI3
#
#FRAME 1.1 Select RAM 1 and start the coefficient loading of the low-pass filter,and select TxCLK
E0F1h#TxI0      MS =1
#               stb=1
#               QS =1
#               RAi=00b     RAM 1 selected.
#               ADi=000b    TxCR0 selected.
#               Di =F1h     TxCLK = 14400Hz
FFFFh#TxI1      unused
0000h#TxI2      word 1 RAM 1 ( first IIR coefficient)
0000h#TxI3      word 2 RAM 1
#
FRAME 2.1 RAM 1 coeff loading,fcomp and fshift prog and Stb ready to select another RAM
A340h #TxI0     MS =1
#               stb=0
#               QS =1
#               RAi=00b     RAM 1 selected.
#               ADi=011b    TxCR3 selected.
#               Di =40h     fcomp = 2400Hz, fshift=Fsx/2
A000h #TxI1     word 3 RAM 1
0000h #TxI2     word 4 RAM 1
0000h #TxI3     word 5 RAM 1
#
#
#FRAME 3.1 RAM 1 coefficient loading, no control register access
A7FFh #TxI0
B7D8h #TxI1     word 6 RAM 1
42B0h #TxI2     word 7 RAM 1
0118h #TxI3     word 8 RAM 1
#
#FRAME 4.1 to 12.1 RAM 1 coefficient loading, no control register access
A7FFh #TxI0
XXXXh
XXXXh
XXXXh
```

```
#FRAME 13.1 Last RAM 1 loading frame
A7FFh #TxI0
0000h #TxI1     word 36 RAM 1
0000h #TxI2     word 37 RAM 1
0008h #TxI3     word 38 RAM 1
#
#
#RAM 2 COEFFICIENT LOADING
#FRAME 1.2 Select RAM 2 and start the coefficient loading of BP filter
EFFFh #TxI0     MS =1
#               Stb=1
#               QS =1
#               RAi=01b    RAM 2 selected
#               ADi=111b
FFFFh #TxI1     unused
0000h #TxI2     word 1 RAM 2
0000h #TxI3     word 2 RAM 2
#
#FRAME 2.2 RAM 2 coefficient loading,no control register access and rest Stb
AFFFh #TxI0     MS =1
#               Stb=0
#               QS =1
#               RAi=01b    RAM 2 selected
#               ADi=111b
A000h #TxI1     word 3 RAM 2
0000h #TxI2     word 4 RAM 2
0000h #TxI3     word 5 RAM 2
#
#FRAME 13.2 Last RAM 2 loading frame
A7FFh #TxI0
0000h #TxI1     word 36 RAM 2
0000h #TxI2     word 37 RAM 2
0008h #TxI3     word 38 RAM 2
#
#
#
#RAM 3 COEFFICIENT LOADING
#FRAME 1.3 select RAM 3 and start coeff loading
F7FFh #TxI0     MS =1
#               Stb=1
#               QS =1
#               RAi=10b    RAM 3 selected
#               ADi=111b
FFFFh #TxI1     unused
0000h #TxI2     word 1 RAM 3
0000h #TxI3     word 2 RAM 3
#
#
```

```
#FRAME 2.3 RAM 3 coefficient loading,no control register access and rest Stb
#
#
B7FFh #TxI0
A000h #TxI1     word 3 RAM 2
0000h #TxI2     word 4 RAM 2
0000h #TxI3     word 5 RAM 2
#
#
#FRAME 3.3 to 12.3 RAM 3 coefficient loading, no control register access
B7FFh #TxI0
XXXXh
XXXXh
XXXXh
#
#
#FRAME 13.3 Last RAM 3 loading frame
B2C4h #TxI0     MS =1
#               Stb=0
#               QS =1
#               RAi=10b   RAM 3 selected
#               ADi=010b  TxCR2 selected
#               Di =C4h   0dB attenuation on XMIT channel and synchronize the TxCLK  clock on
                          TxRCLK
0000h #TxI1     word 36 RAM 2
0000h #TxI2     word 37 RAM 2
0008h #TxI3     word 38 RAM 2
#
#
# FRAME 14
3FFFh #TxI0     MS =0     Data mode
#               Stb=0     ready to read ram
#               QS =1
#               RAi=11b   No RAM access
#               ADi=111b  No Control register access
XXXXh #TxI1     Txsig
XXXXh #TxI2     Ressig
XXXXh #TxI3     unused
#
#
```

 # SYNCHRONOUS SERIAL INTERFACE B

```
#
#FRAME 0. Select the correct sampling frequency
01A4h #Trl0     ADi=001b   RxCR1 selected
#               Di =A4h    Fsr=9600Hz, Rxrclk=2400Hz
#                          RxHSCLK=12.288MHz
FFFFh #Trl1
FFFFh #Trl2
FFFFh #Trl3
#
#FRAME 1. Select the correct receive bit clock (RxCLK) frequency
00F1h #Trl0     ADi=000b   RxCR0 selected
#               Di =F1h    RxCLK=14400Hz
FFFFh #Trl1
FFFFh #Trl2
FFFFh #Trl3
#
#FRAME 2. No phase shift selected
0200h #Trl0     ADi=010b   RxCR2 selected
#
#               Di =00h    no phase shift
FFFFh #Trl1
FFFFh #Trl2
FFFFh #Trl3
#
#
#FRAME 3. select interpolation factor
0340h #Trl0     ADi=011b   RxCR3 selected
#               Di =40h    interpolation factor = 160
FFFFh #Trl1
FFFFh #Trl2
FFFFh #Trl3
#
#
#FRAME 4
FFFFh #Trl0     ADi=111b   no control register access
XXXXh #Trl1     EYEX-EYEY
FFFFh #Trl2     reserved
FFFFh #Trl3     reserved
#
#
```

I.6 - FILTER COEFFICIENT CODING IN ST7544 TIME-SLOT FORMAT

I.6.1 FILTER CHARACTERISTICS

Type	:	band-pass filter
Order	:	11
Sampling frequency	:	9.6kHz*5 = 48kHz
passband edge HP	:	300Hz (3dB , butterworth)
stopband edge HP	:	200Hz
stopband loss HP	:	8dB
passband edge LP	:	3200Hz (Cauer)
stopband edge LP	:	4200Hz
stopband loss LP	:	60dB
passband ripple	:	0.1dB
coefficient wordlength	:	11 bits + sign

I.6.2 - Filter Coefficients Table

B	C	A	D	E
0	0	0.9	- 1	0
0.9614815	0	0.8414686	- 1	0
1.706978	- 0.7952128	0.1985583	- 1	0
1.959984	- 0.961496	0.1774637	- 1.33996	1
1.675779	- 0.7113152	0.0346	0.35224561	1
1.747247	- 0.8925031	0.1021413	- 1.698336	1
1.789548	- 0.967721	0.4543867	- 1.627507	1
0	0	0.0025201	0	0

I.6.3 - Coefficient Coding in ST7544 Time-slot Format

Example of subroutine to code the coefficients in the ST7544 time-slot format.

```
SUB CODE(A(),NbBiquad,AA())
LOCAL i,EXTRABIT()
  FOR i=1 TO NbBiquad
     IF ABS(A(i))=1 THEN
        EXTRABIT(i)=-32768
        AA(i)=CINT((A(i)/2)*2048)
     ELSE
        EXTRABIT(i)=0
        AA(i)=CINT(A(i)*2048)
     END IF
        AA(i)=(AA(i)<3)AND 32767
        AA(i)=(AA(i) OR EXTRABIT(i))
     NEXT
END SUB
```

with :

INPUT :
NbBiquad number of biquadratic function.
A() Coefficient in decimal format

OUTPUT:
AA() Coefficient in ST7544 time-slot format.

writing convention:
ABS() return an absolute value
CINT() convert its argument to an integer.
(if the fractional part of an argument is equal to 0.5, it is rounded toward the even number).

≤ **n** left shift of n bit.

Note : It is not possible to code -1 or 1 , we therefore do as following
+1 = 2 * +0.5
-1 = 2 * -0.5
So IT IS NOT POSSIBLE TO CODE +/- 2

Filter table in Hexadecimal format.

B	C	A	D	E
000	0000	3C88h	E000h	0000
3D88h	0000	37E0h	E000h	0000
B6A0h	4D18h	CE0h	E000h	0000
BEB8h	4278h	B58h	C9A8h	A000h
B940h	4210h	E68h	CBE8h	A000h
B7E8h	46E0h	F98h	D520h	A000h
B5A0h	5278h	238h	1690h	A000h
0000	0000	20H	0000	0000

I.6.4 - Transfer Function

Figure 6

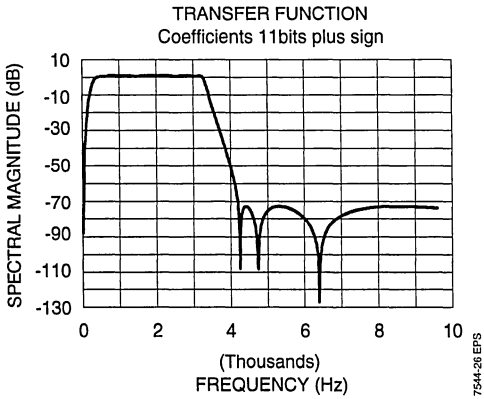


Figure 7

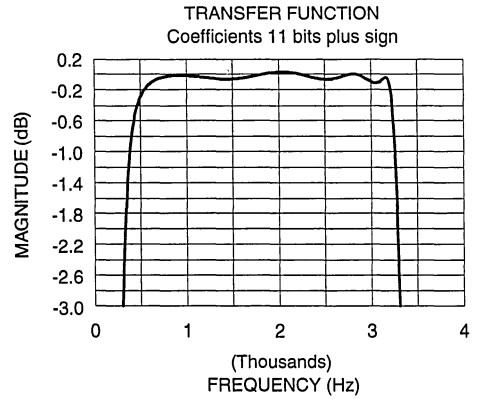
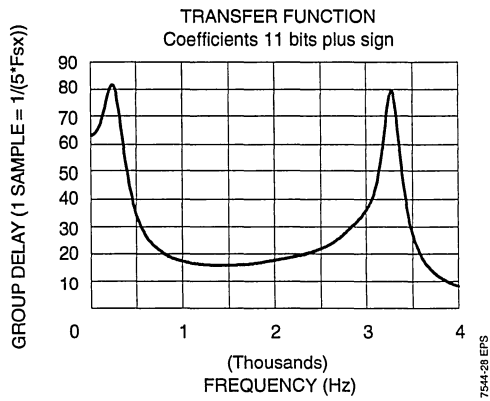


Figure 8

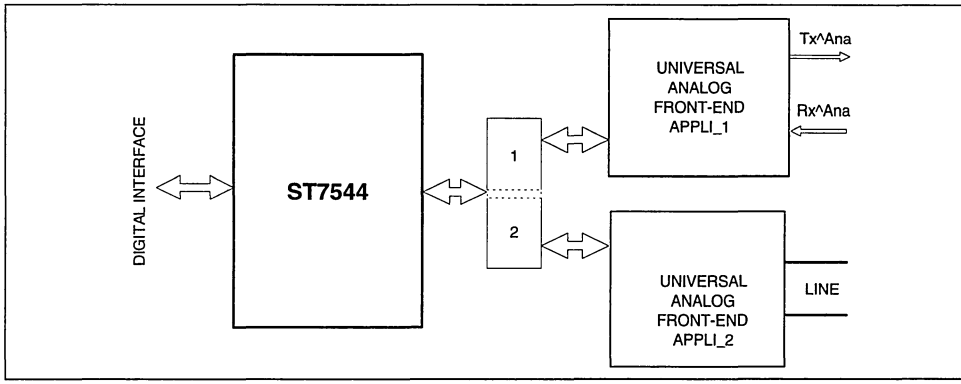


II - ST7544 APPLICATION BOARD

The ST7544 application board will give you a powerful analog front-end evaluation/development tool.

Two applications are available on board :
- Appli 1 : Analog front-end,
- Appli 2 : Modem analog front-end.

Figure 9



- Digital interface gives all necessary signals in order to control and program the ST7544.
- The Digital interface connector is fully compatible with **ST18933** development tools.
- Functionality with 2 crystals available on board,
- Eye diagram monitoring,
- Single-ended application.
- Full differential duplexer application.

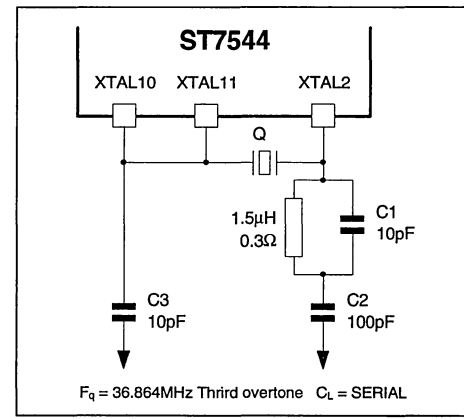
II.1 - CRYSTAL OSCILLATOR

XTAL10 and XTAL11 inputs must be tied to external crystal(s) or external clock(s).These inputs are selected from the TxCtrl register.The maximum clock rate is 38MHz.XTAL10 is the default external clock/crystal input.It is mandatory to short-circuit XTAL10 and XTAL11 when a single external crystal or clock generator is used.The nominal master clock frequency is 36.864MHz but the onchip amplifier is designed for a parallel crystal oscillator with a frequency equal to 18.432MHz.

XTAL2 output is to be tied to one or two external crystal (Figures 10 and 11). If an external clock is used, XTAL2 should be left open.

II.1.1 - Single Crystal Oscillator

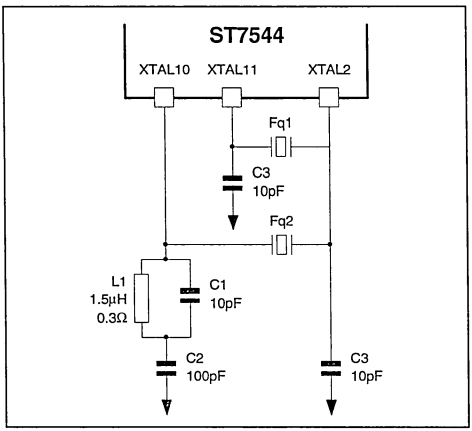
Figure 10



Operating range : 0 - 70 deg, 5V ± 5%
Start-up : Max. = 10mS
Typ. = 3.7 mS

II.1.2 - Double Crystal Oscillator

Figure 11



Operating range : 0 - 70 deg, 5V ± 5%
Start-up : Max. = 10mS
Typ. = 1.5 mS

II.1.3 - Quartz Specification

When you order a quartz, you have to specify the following parameters :
- Nominal frequency (e.g 36.864MHz ,25.848MHz)
- MODE (3rd overtone, Fundamental)
- Load capacitance (SERIAL, 30pF)
- Frequency tolerance (50 ppm from 0 to 70°C)

II.2 - APPLICATION 1 (single-ended)

II.2.1 - Transmit

The transmit part is a differential single-ended with low-pass filter realised by R6//C12 and R7//C13.The resistors R6 and R7 must be equal as must the capacitor C12 and C13.

The 3dB cut-off frequency of the 1st order filter inside the ST7544 is :

$$Fc = TxOCLK / (2 \cdot \pi \cdot 10)$$

E.g : 1st LP : Fsx = 7.2kHz over=4
then Fc = 14.7kHz
2nd LP : R =15kΩ C=680pF
then Fc = 15.6kHz

As the transfer function of the filters are known,the digital signal can be compensated if needed.

The C14=1µF gives on BNC J5 a signal referenced to AGND.

II.2.2 - Receive

The receive part is single-ended to differential.There is a low-pass filter realised by R13,R14 and C16.

$$Fc = 1 / (2 * PI * 1.2E03 * 2E-12) = 66kHz$$

Having a Fc at 66kHz, we have a flat transfer function in working Band (0-4kHz).

We DO NOT recommend the use of OP-AMP based filter as OP-AMP will present high impedance at high frequencies.This low-pass filter **must be implemented as close as posssible to the pins RxA1 and RxA2.**

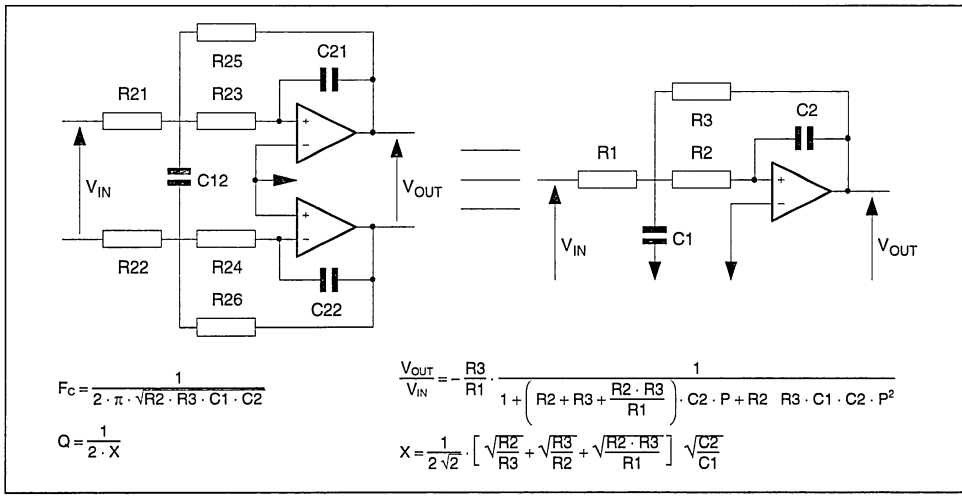
II.3 - APPLICATION 2 (duplexer)

II.3.1 - Transmit

We have a full differential low-pass filter on transmit the side before the DAA (see Figure 12)

R1 = R21 = R22 = 13.2kΩ
R2 = R23 = R24 = 22kΩ
R3 = R25 = R26 = 22kΩ
C1 = 2 * C12 = 2*680pF = 1360pF
C2 = C21 = 100pF
Fc = 19.6kHz
Ao = - R3/R1 = -1.66
X = 5 - Q= 0.1

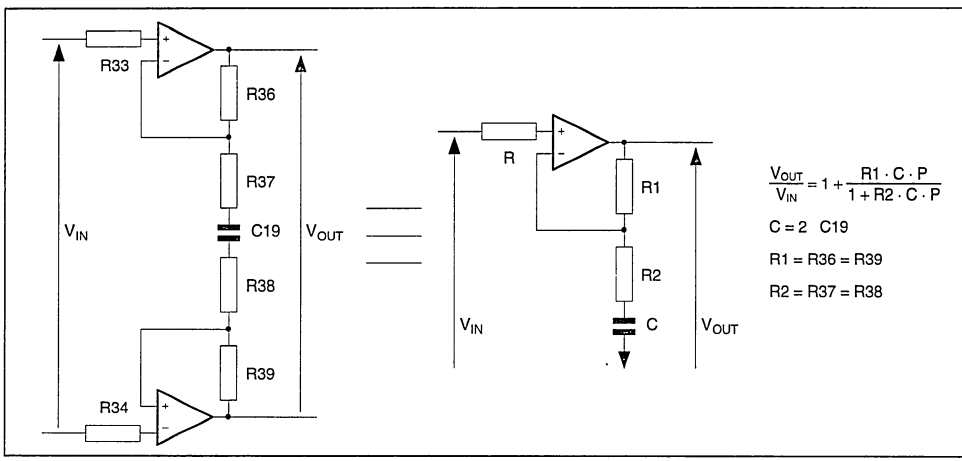
Figure 12



II.3.2 - Receive

We have 2 filters as in application 1 (LPF, Fc = 66kHz) and describe below (DC offset suppress, Fc = 85Hz)

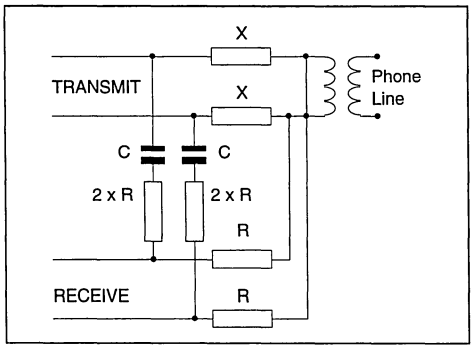
Figure 13



II.3.3 - Duplexer

R,C : Improves the low frequency response.These values depend on the transfer function of the transformer.Filter transfer function realised by R,C must compensate for the loss in transformer at low frequency.

Figure 14



Z0 : Nominal line impedance.(e.g : Z0 = 600Ω)

TRANSFO : M = 1 , Rs = Rp = 100Ω

$2 * X = Z0/M^2 - Rp - Rs/M^2$

$2 * X = Z0 - 2 * Rp = 600 - 200 = 400$

X = 200Ω

II.4 - PERFORMANCE MEASUREMENT

II.4.1 - Configuration

The following measurements have been made with ST7544 application board on application (1) with crystal 36.864MHz.The analog transmit signal (J5) is connected to analog receive signal (J4).

The IIR1 filter (low-pass) file is the following :

FFFF	0000	0000	A000	0000	0000
B7D8	42B0	0118	CA08	A000	B570
48A0	2838	CB68	A000	B268	5070
3508	CFA0	A000	AED8	59D0	2898
DD90	A000	AC18	6118	07A0	3368
A000	ADF0	5338	0858	4098	A000
0000	0000	0008			

The IIR2 and IIR3 filter (band-pass filter) files are the following :

FFFF	0000	0000	3C88	E000	0000
3D88	0000	37E0	E000	0000	B6A0
4D18	0CE0	E000	0000	BEB8	4278
0B58	C9A8	A000	B940	4210	0E68
CBE8	A000	B7E8	46E0	0F98	D520
A000	B5A0	5278	0238	1690	A000
0000	0000	0020			

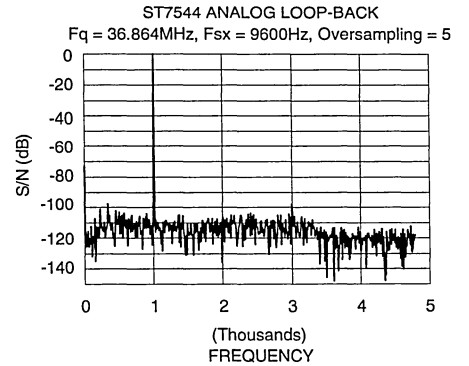
The control registers are programmed as following :

F9A4	TxCR1	M*Q=4*6 U=4 P0=3 and BS=0, Fsx = 9600Hz, Symbol rate = 2400 baud, Txhsclk = 12.288MHz, Band split Mode inactive
F8F1	TxCR0	NRST=F1h, Bit rate clock frequency = 14400Hz
FB40	TxCR3	V=010b , W=0 , Ts=000 , DL=0, Fcomp = Txrclk, Oversampling ratio = 160, Phase shift freq (Fsx/2 (Fq ± Fsx/2))normal mode
FAC4	TxCR2	AT=11b, LTX=0, LC=0, SST=0, VF=0, R2=0, attenuation = 0dB, mode 7543, synchronize TxCLK on TxRCLK, Normal mode synchronization
01A4	RxCR1	idem TxCR1
00F1	RxCR0	idem TxCR0
0200	RxCR2	no phase shift
0340	RxCR3	V = 160 - Interpolation ratio

II.4.2 - Measurement

We generate a digital sinewave of 1003.125Hz (1024 samples).This signal is sent to Txsig.Then we do a FFT (1024 samples) on the digital receive signal RxTx.

Figure 15



We have S/N = 84.43 dB. The band noise is double because of analog loop-back ,so if we want to calculate the dynamic range of the ST7544 ,we add 3dB to the S/N.

S/N = 84.43+3 = 87.43 dB at Signal = -6.13dBr

S/N = 87.43 + 6.13 = **93.56dB = DYNAMIC**

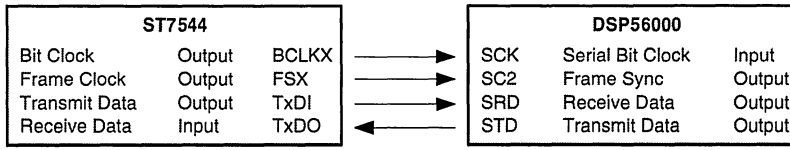
S/N = 6.02 * Nbit + 1.76

Nbit = (93.56-1.76)/6.02 = **15.25 bits**

III - INTERFACING ST7544 WITH DSP56000 (MOTOROLA)

You will find below a suggested interface of our ST7544 with DSP56000 series from Motorola.
We use the ST7544 in single SSI. The different connection are as following :

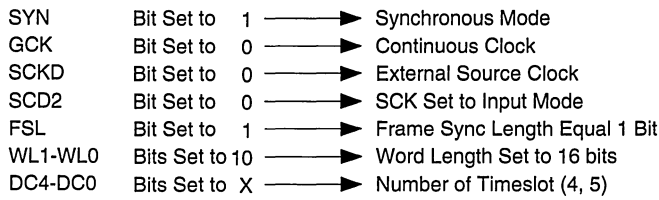
Figure 16



7544-46 EPS

The DSP56000 control register bit has to be configured as following :

Figure 17



7544-47 EPS

And you have to program the DSP in Network mode.

ANNEXE 1 : Demoboard Schematics

Figure 18

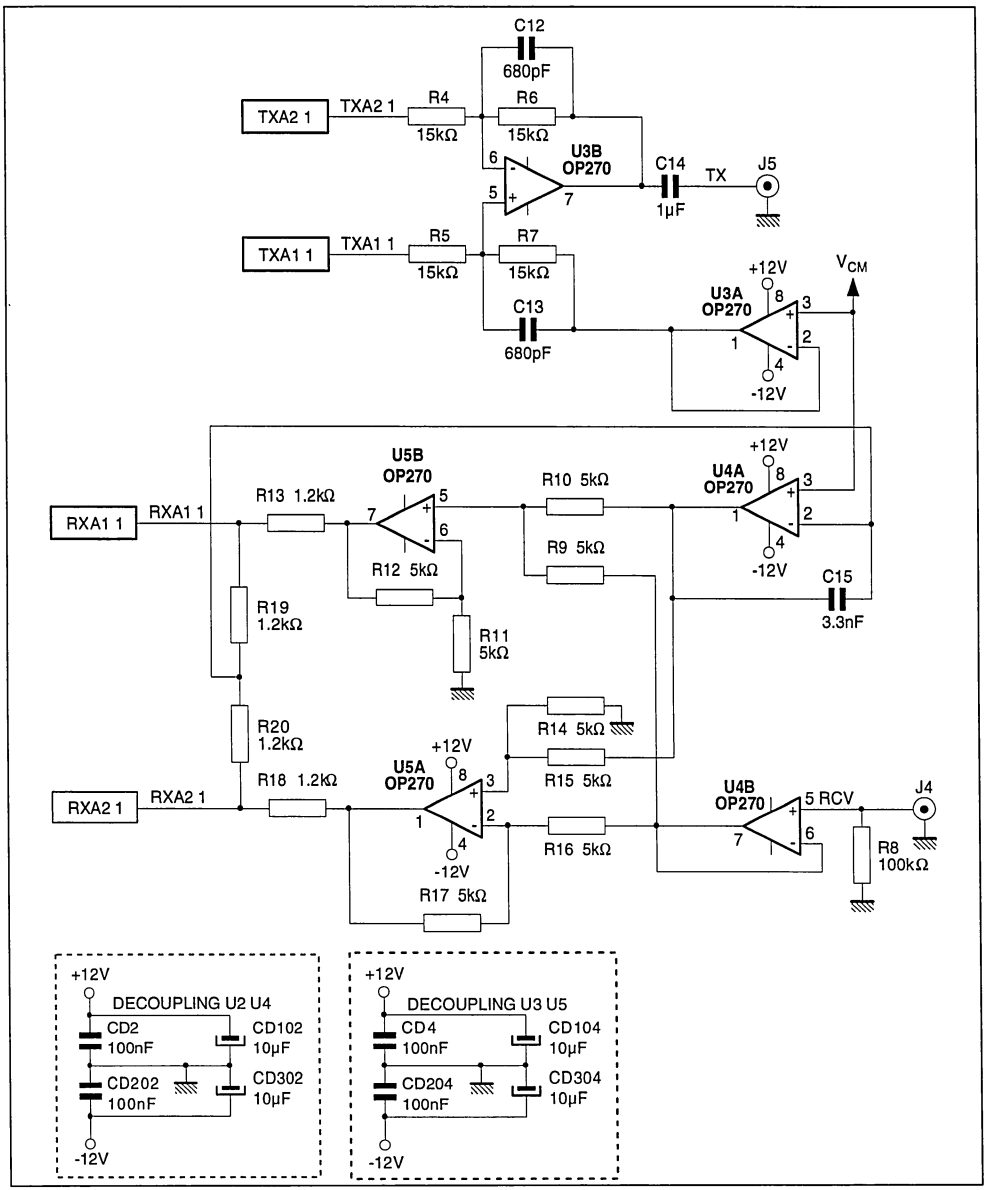


Figure 19

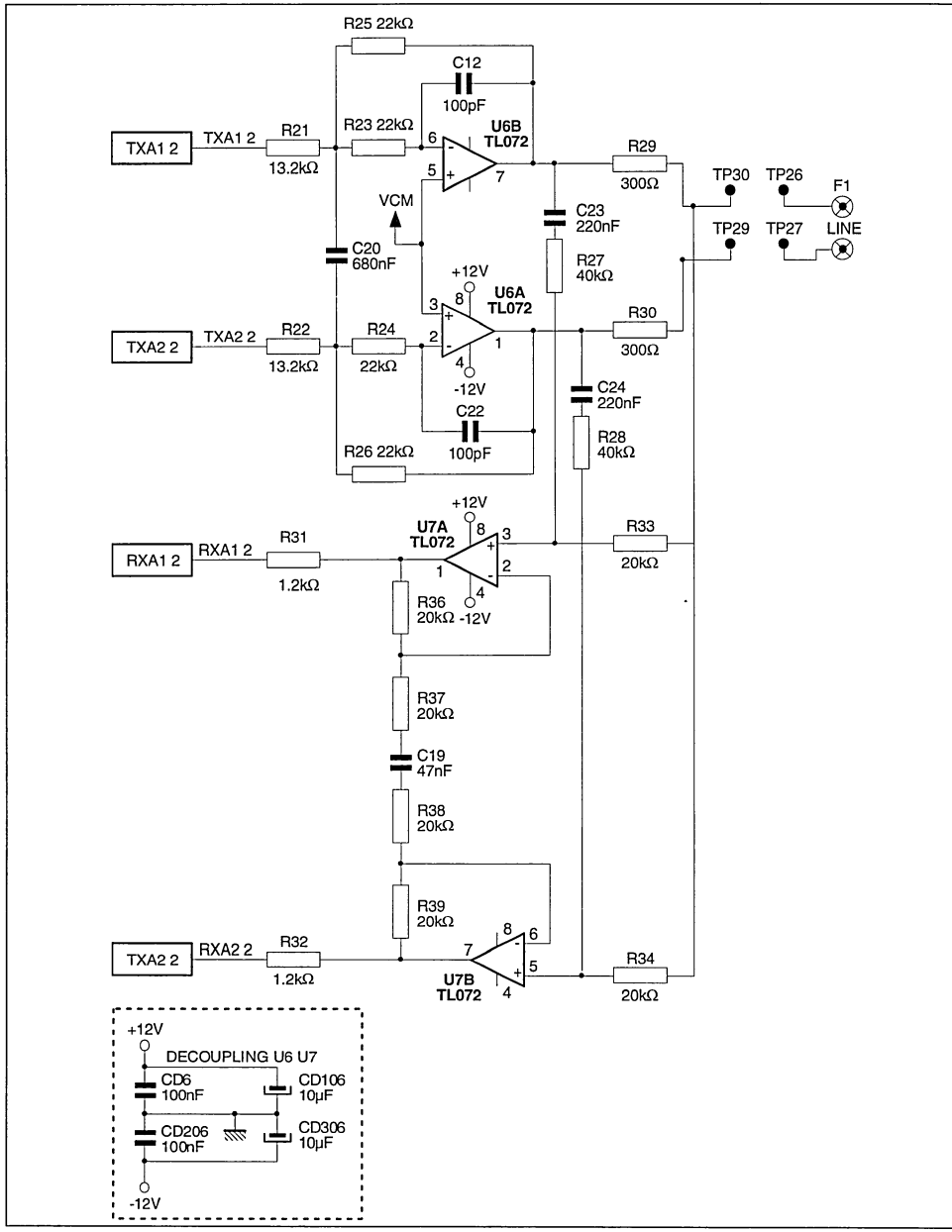
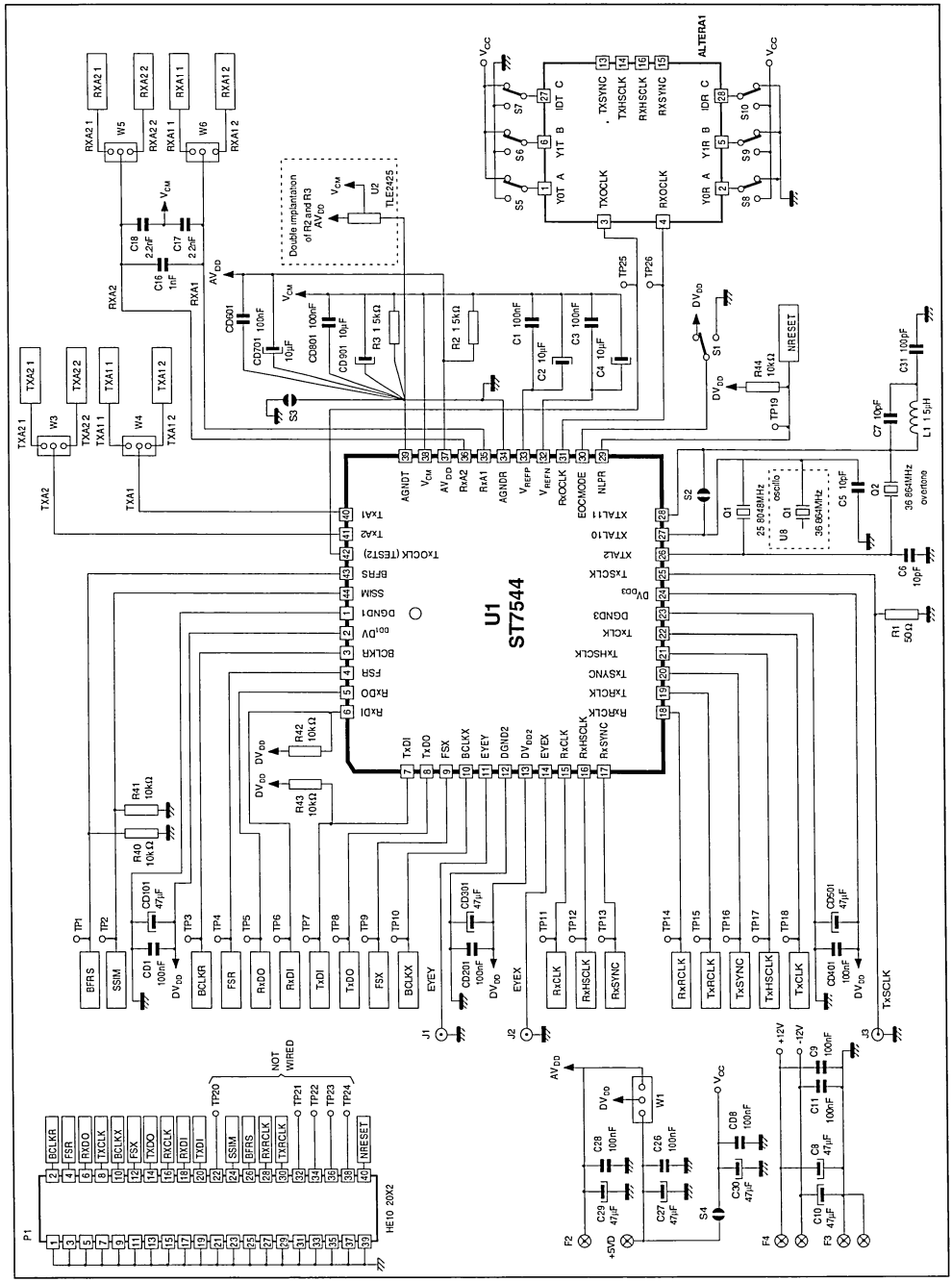

R25 22kΩ
C12
100pF
TXA1 2
R21
13.2kΩ
R23 22kΩ
U6B
TL072
R29
300Ω
TP30
TP26
F1
VCM
C23
220nF
TP29
TP27
LINE
C20
680nF
+12V
R27
40kΩ
U6A
TL072
TXA2 2
R22
13.2kΩ
R24
22kΩ
R30
300Ω
-12V
C24
220nF
C22
100pF
R28
40kΩ
R26 22kΩ
+12V
U7A
TL072
RXA1 2
R31
1.2kΩ
R33
20kΩ
R36
20kΩ
-12V
R37
20kΩ
C19
47nF
R38
20kΩ
R39
20kΩ
TXA2 2
RXA2 2
R32
1.2kΩ
U7B
TL072
R34
20kΩ
+12V
DECOUPLING U6 U7
CD6
100nF
CD106
10µF
CD206
100nF
CD306
10µF
-12V
7544-37 EPS

Figure 20


U1
ST7544
ALTERA1
TLE2425
Double implantation of R2 and R3
NOT WIRED
HE10 20X2
7544-38.EPS

ANNEXE 2 : Layout

Figure 21

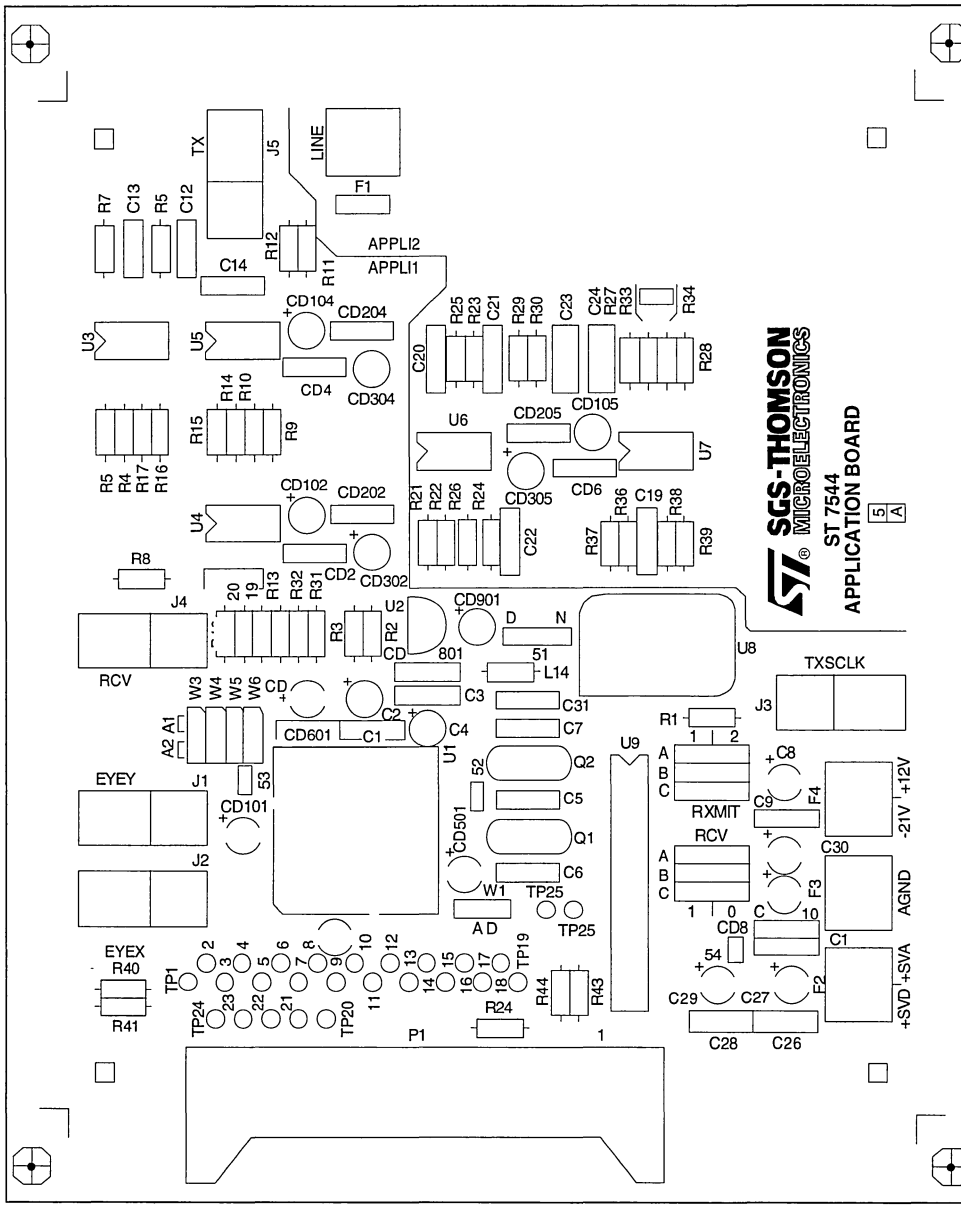
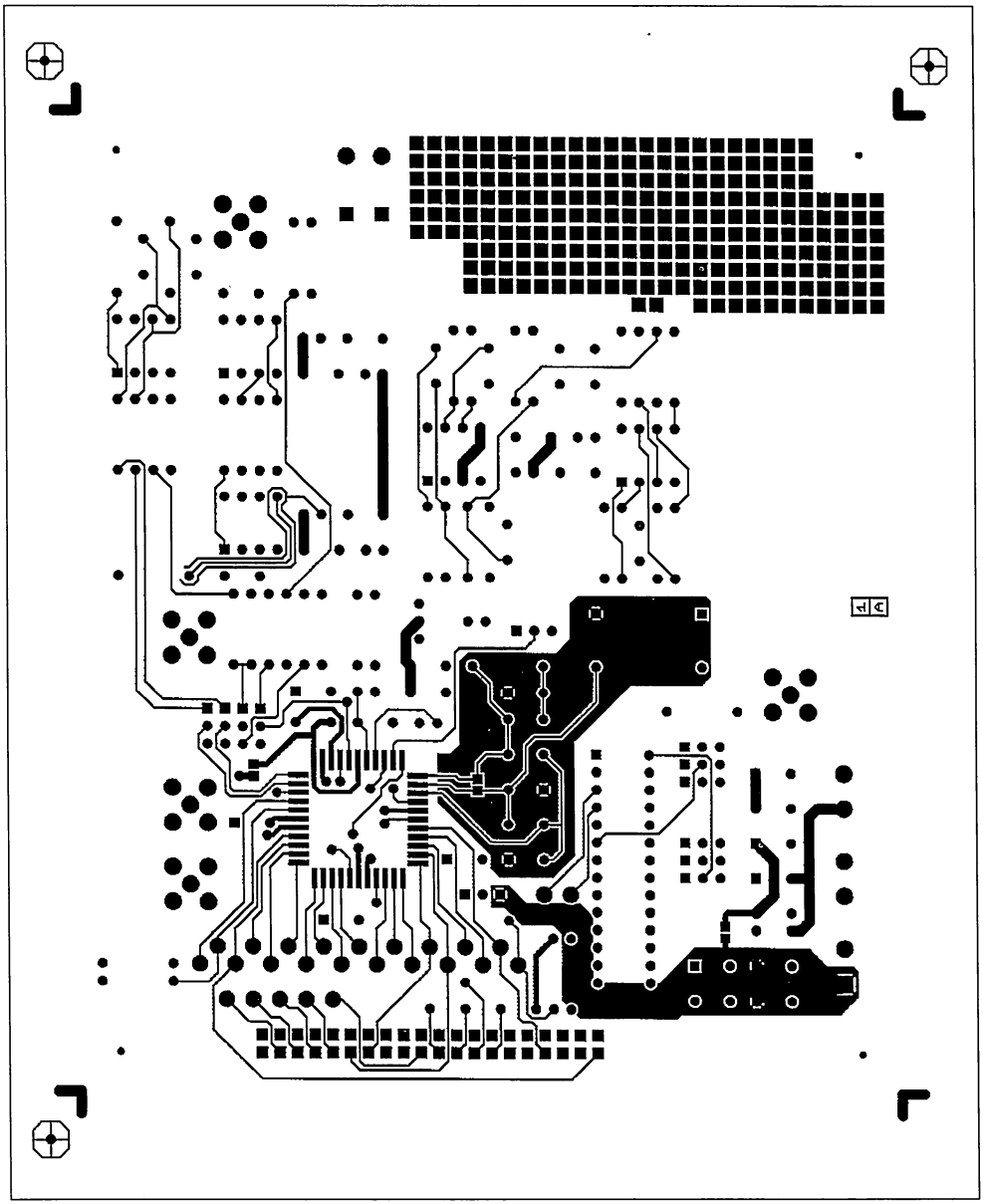
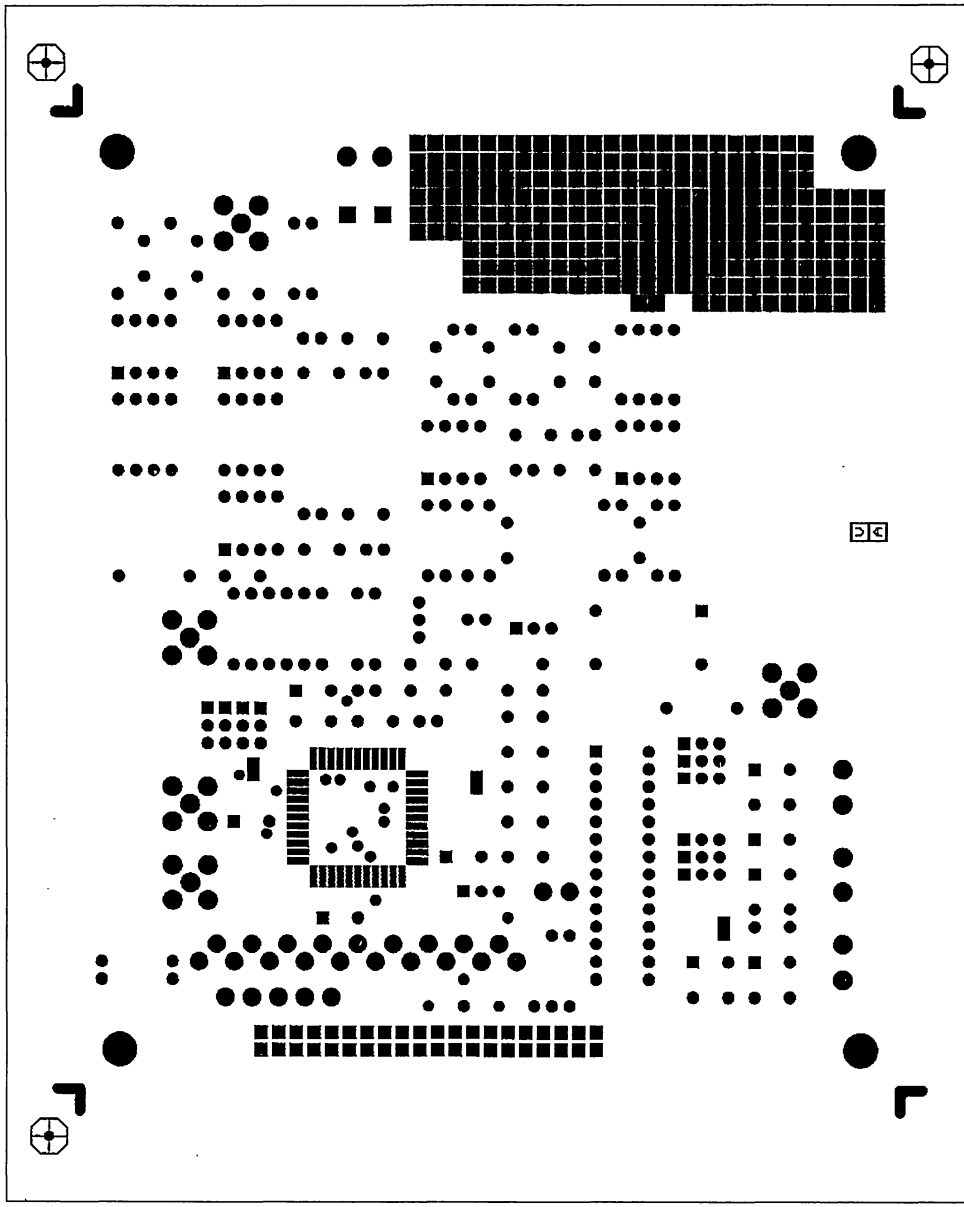


Figure 22 : Layer 1 - Components Side



7544-40.TIF

Figure 23 : Layer 1



7544-41.TIF

Figure 24 : Layer 2 - GNDD, AGND

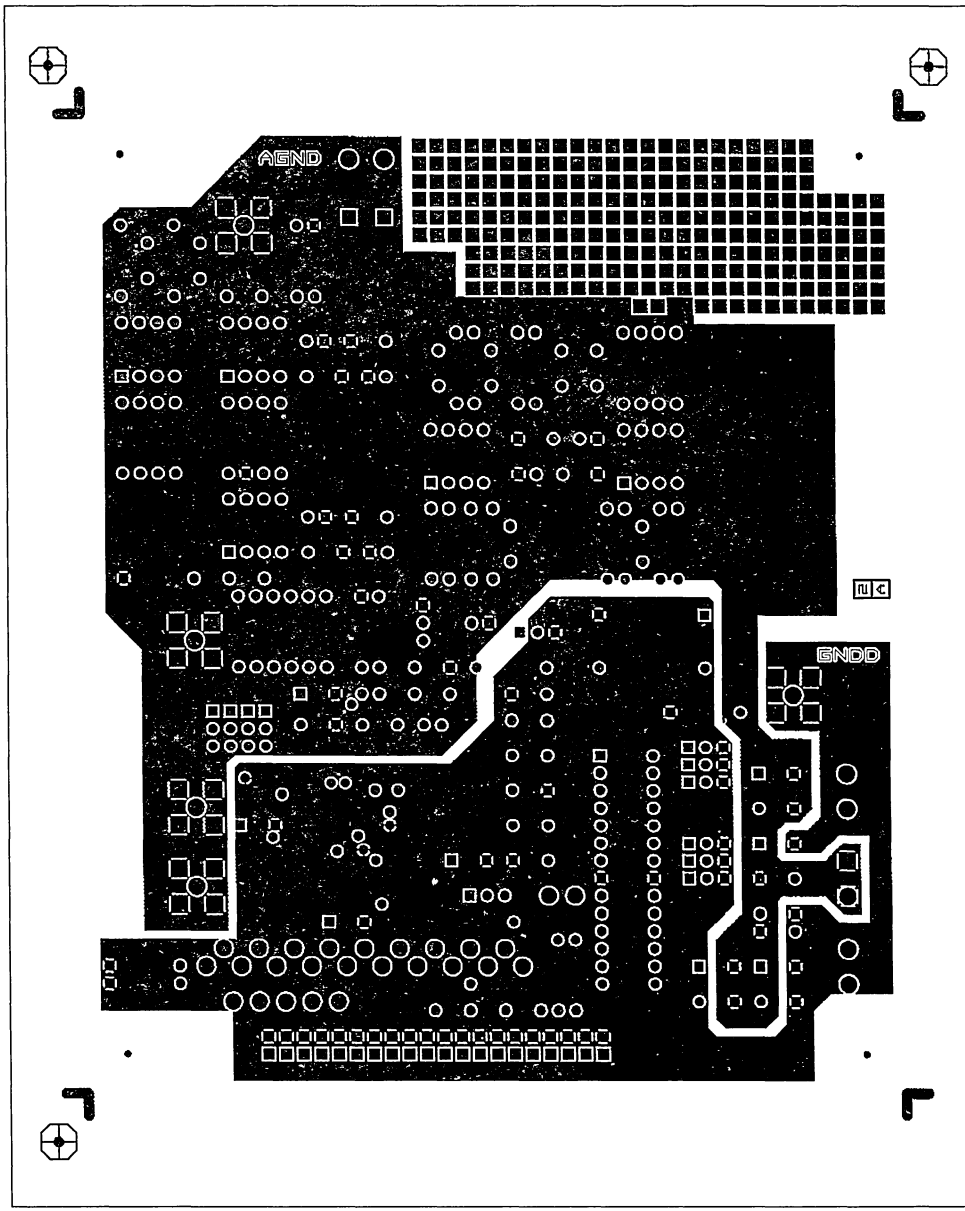


Figure 25 : Layer 3 - DV_{DD}, AV_{DD}

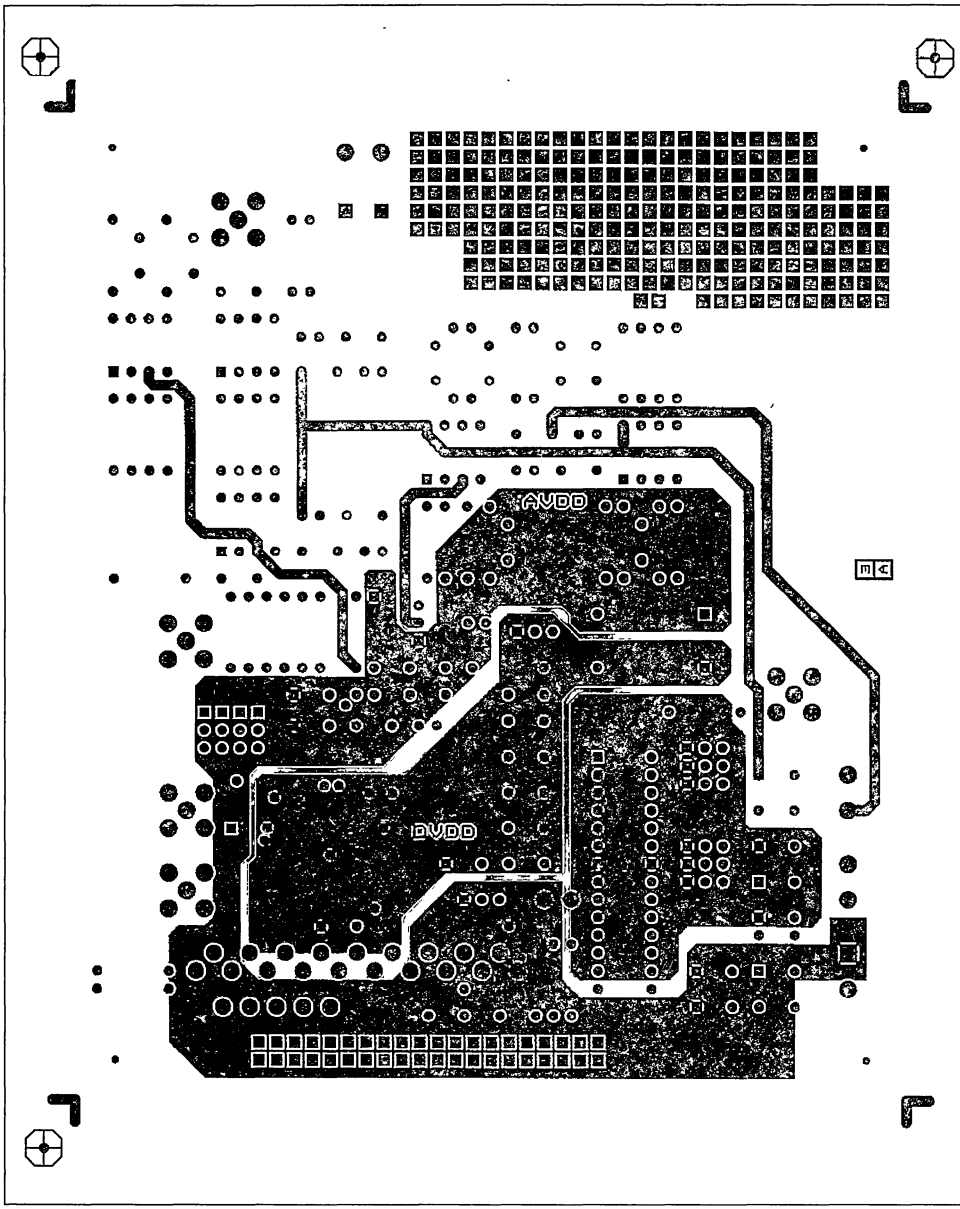
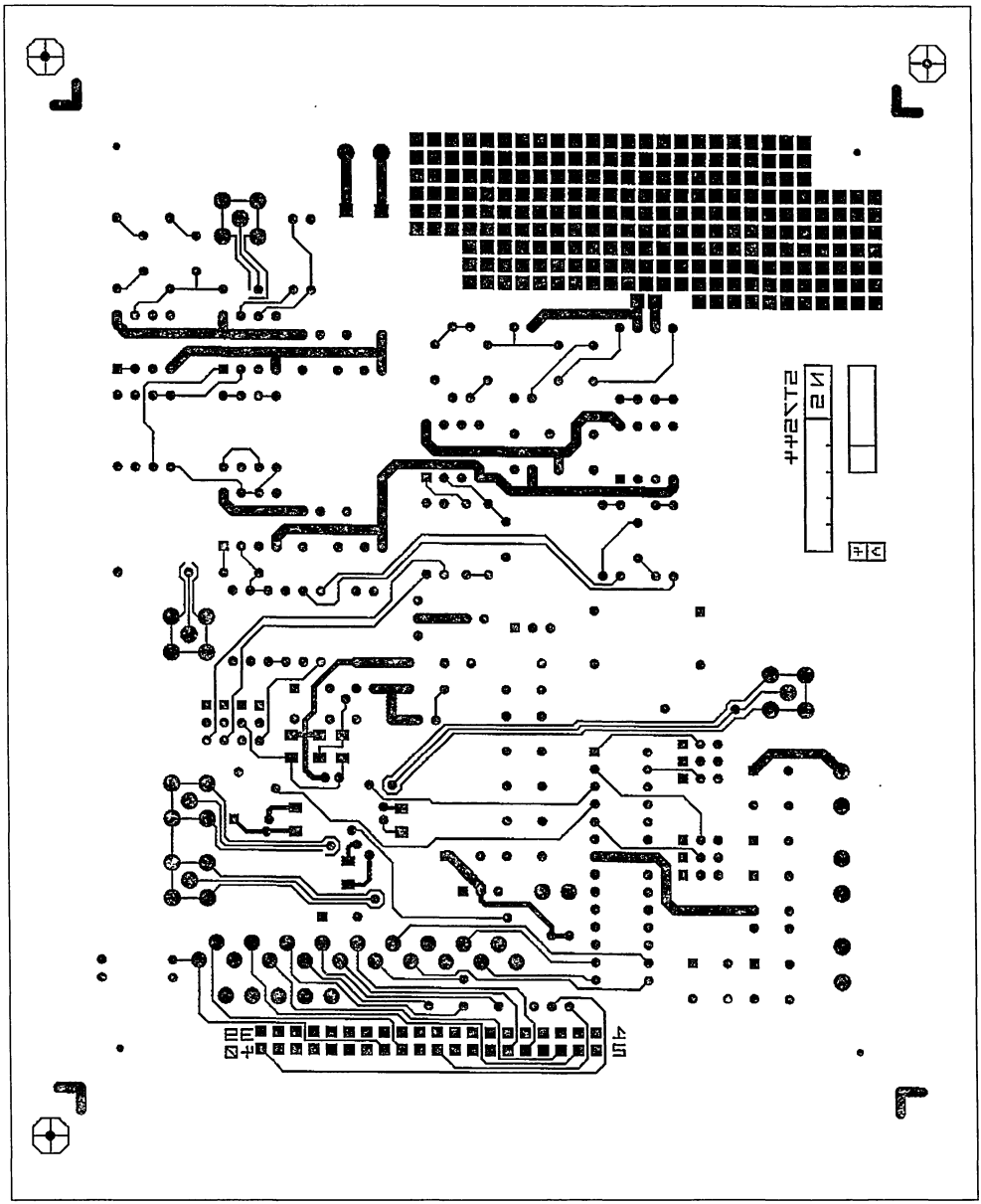
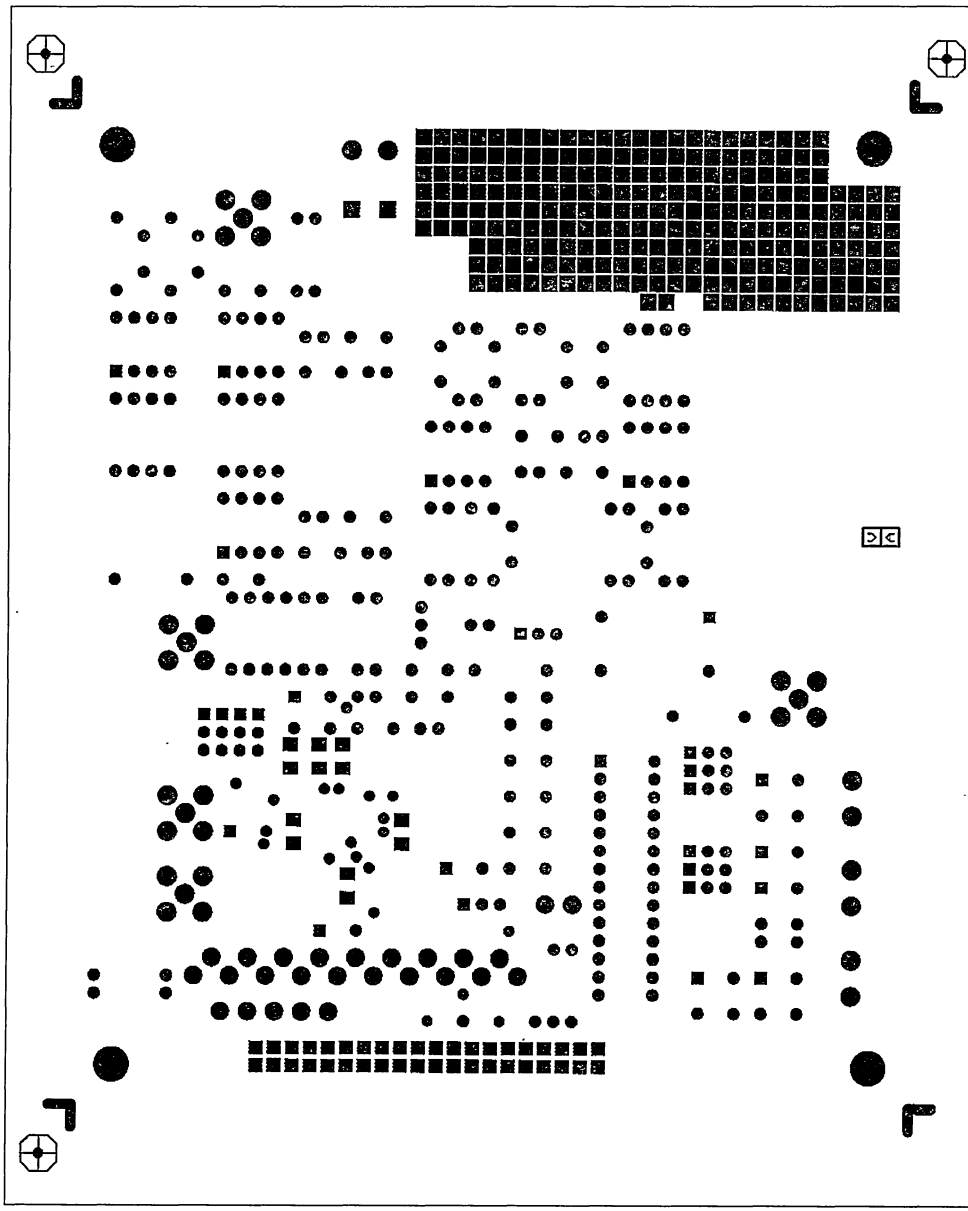


Figure 26 : Layer 4



7544-44.TIF

Figure 27 : Layer 4



7544-45.TIF

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

ST7546 - SIMPLIFIED ANALOG FRONT-END

By Joël HULOUX

CONTENTS

I - INTRODUCTION

The ST7546 is a high resolution analog-to-digital and digital-to-analog converter targeted for V.34 modem and consumer audio applications.

This device has a 16 bit oversampling ADC and DAC, filters and control logic for the serial interface. The oversampling ratio consequently the sampling frequency for the ADC and DAC are user programmable.

The devices operation is controlled by reading the 16-bit information control register.

The major functions of the ST7546 are :

- To convert the audio-signal to 16-bit 2's complement data format through ADC channel.
- To communicate with an external digital signal processor via serial interface logic.
- To convert 16-bit 2's complement data from a digital signal processor to an audio signal through the DAC channel.

The ST7546 consists of two signal-processing channels, an ADC channel and a DAC channel, and the associated digital control. The two channels operate synchronously so that the transmitted data to the DAC channel and received data from the ADC channel occur during the same time interval. The data transfer is in 2's complement format.

To save power, the low-power reset mode can be used to reduce the power consumption to less than 1mW (typ. 50µW).

II - DIGITAL INTERFACE (9 Pins)

The ST7546 is a very simple device to use thanks to the preprogrammed filters and its only one control register. In a short time you will be familar to the high efficiency integration function.

II.1 - Data Exchange

The data exchange (DATA and CONTROL) are done through the pins Data in (Din) and Data out (Dout).

Pin	Data Mode	Control Mode
Din	Word is input of the DAC	Data word followed by control control register word
Dout	Word is ADC conversion result	Data word followed by register read

II.2 - Register Programmation (16 Bits Word)

The control of the device can be done in two way, for register programmation, by setting the pins HC0 and HC1.

HC1	HC0	Selected Mode
0	0	Software mode : LSB = 0 for Data, LSB = 1 for control the device generates one pulse at 1/2 sampling period for control word. At the end of the secondary frame the device automatically returns to data mode.
0	1	Hardware mode for data transfer only
1	X	Hardware mode for device programming and register read

Figure 1 resume all possible mode with the ST7546. In this chart, we see the different data length according to the programmation (transmit data could be on 15 bits in software mode or 16 bits in hardware mode). The hardware mode could be selected easily by connecting HC0 to $+DV_{DD}$.

Figure 1

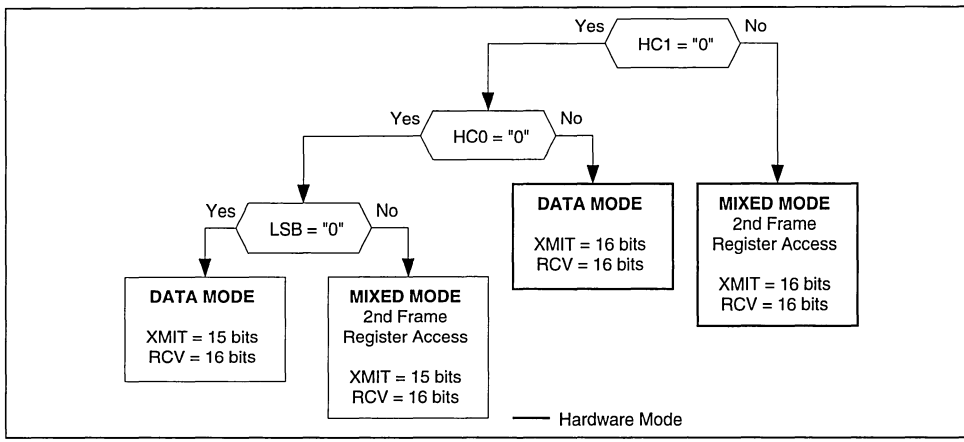
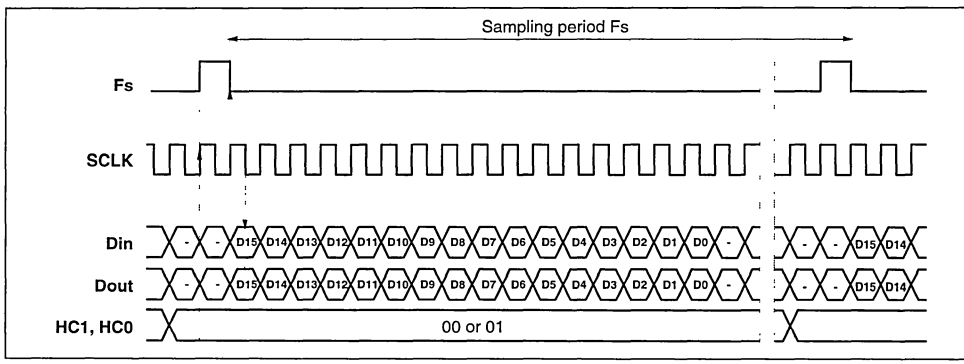
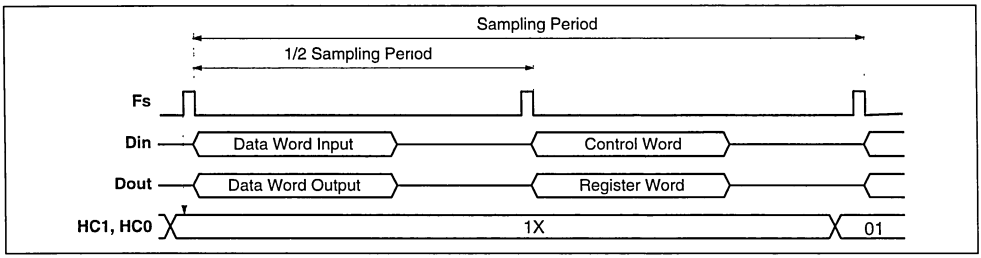


Figure 2 : Data Mode



II - DIGITAL INTERFACE (9 Pins) (continued)

Figure 3 : Access Register Mode (obtained also with LSB data = "1")



II.3 - Clocks Signals

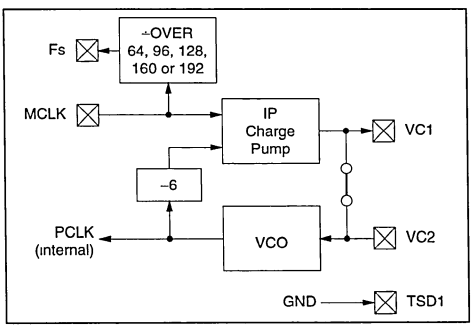
- MCLK : Master Clock Input. This signal is the oversampling clock of the D/A and A/D convertor. It also provides the clocks of the serial interface (Fs, SCLK). The master clock is equal to Fs x OVER (OVER = oversampling ratio = 64, 96, 128, 160 or 192). For proper operation there must be no jitter on MCLK.
- Fs : Frame Synchronization (Sampling frequency) signal generated internally goes low on rising edge of SCLK. This signal indicates that the ST7546 is ready to send or receive data.
- SCLK : Serial bit clock clocks data into Din and out of Dout during Fs. SCLK = $\overline{MCLK}$

The clock generator provides, via an internal PLL, the clocks needed for the computation in the digital section (PCLK = Processing Clock). The MCLK clock is used by the PLL for the clock reference.

Thanks to the control register, different configurations can be obtained for the clock generator. We use the bits D15 and D14 of the control register.

D15	D14	Mode
0	X	PLL normal mode, TSD1 Pin is grounded internally
1	0	PLL open loop, Tsd1 Pin = PCLK output (TEST3)
1	1	PLL open loop, Tsd1 Pin = PCLK input (TEST4)

Figure 4 : Normal Mode



TEST3 : see Figure 5

In this mode you can observe the Processing clock on Pin TSD1. Do not forget to connect externally the Pin VC1 and VC2 for the PLL loop.

TEST 4 : see Figure 6

If you are in the mode to enter the processing clock which is equal to 6 times the MCLK do not forget to provide the Master clock to the ST7546.

Figure 5 : TEST3

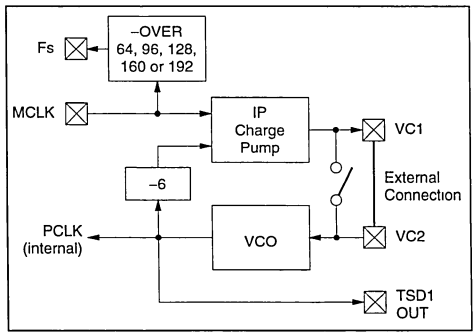
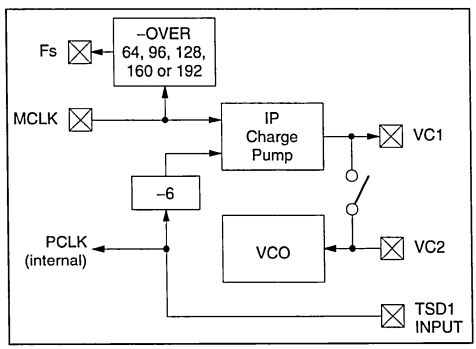


Figure 6 : TEST4



II - DIGITAL INTERFACE (9 Pins) (continued)

II.4 - Reset - Power Down

RESET : The reset function is to initialize the internal counters and control register. A minimum low pulse of 100ns is required to reset the ST7546. This reset initiates the serial data communications.

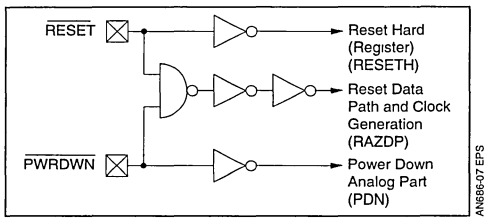
The reset will initialize the register to default value providing the following status for the ST7546 :

- Oversampling ratio equal to 160
- Serial interface in data mode
- DAC attenuation set to infinite
- ADC gain set to 0dB
- Differential input mode selected on ADC convertor
- Multiplexor set on main inputs IN+ and IN-

After a reset the first frame synchronization corresponds to the primary channel.

POWER DOWN (PWRDWN) : The PWRDWN powers down the entire chip (50µW). When this pin is set low the internally programmed state is maintained. Full operation can be resumed within 5ms by putting back PWRDWN pin to High. When not used this pin should be tied to V_{DD}.

Figure 7



III - TEST FEATURES

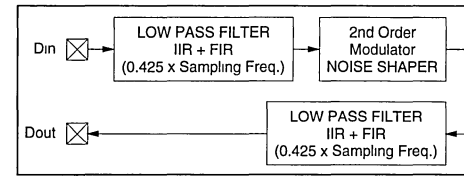
Some test features have been introduced in the ST7546 in order to help you for the debug. These features are accessed through the bit D13 and D12 of the control register or by setting a certain level on Pin Tstd2.

III.1 - Control Register Test Features

D13	D12	Function
0	0	Normal Mode
0	1	Digital Test (TEST 1)
1	0	Analog Test (TEST 2)
1	1	Reserved

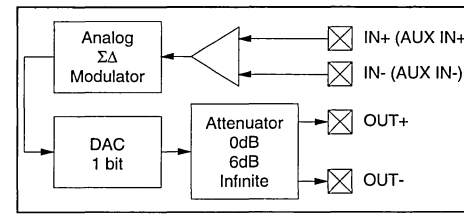
TEST 1 : Digital Test (see Figure 8)
In order to test only the digital path, in this mode internally we connect the transmit output Noise Shaper to the Receive FIR filter. So the test does not depend on the analog hardware.

Figure 8 : TEST1



TEST 2 : Analog Test (see Figure 9)
In order to check the analog hardware, in this mode we connect internally the sigma delta modulator output to the DAC (1 bit) input.

Figure 9 : TEST2



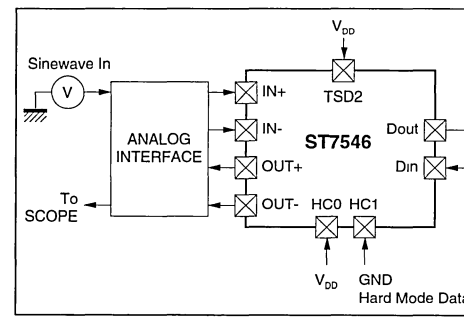
III.2 - Pin Tstd2 Features

In normal mode the pin Tstd2 is set to Ground (0V). Two differents test features could be obtained by setting this pin to V_{DD} or $V_{DD}/2$.

III.2.1 - Tstd2 = V_{DD}

In this configuration we force the transmit attenuator to 0dB. In that case you can test the complete device plus the analog interface by doing a RESET (see default configuration at Chapter II.4) and then you set the Pin Tstd2 to V_{DD} and connect externally the Pin Dout to the Pin Din. You enter a sinewave on the input receive and you will get a sinewave at the transmit output. This feature is good to check your complete hardware without having doubt on your DSP software as this one is not used.

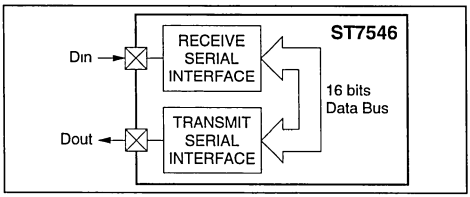
Figure 10



III - TEST FEATURES (continued)
III.2.2 - Tsd2 = V_{DD} / 2

In this configuration we connect internally the output of the transmit serial interface to the input of the receive serial interface. So you will be able to check what has really been taken into account in the device on the received data.

Figure 11



IV - DSP INTERFACE

The interface of the ST7546 and a DSP is done through a SSI (Synchronous Serial Interface) or SERIAL PORT. Any wellknown DSP on the market has such communication port.

We will see the interconnection for 3 types of DSP : SGS-THOMSON, MOTOROLA and TEXAS INSTRUMENTS.

IV.1 - SGS-THOMSON Microelectronics DSP (see Figure 12)

IV. 2 - MOTOROLA DSP (see Figure 13)

The SSI of the 56000 family DSP must be programmed as following :

SYN	bit = 1	Synchronous mode
GCK	bit = 0	Continuous clock
SCKD	bit = 0	External source clock
SCD2	bit = 0	SCK set to input mode
FSL	bit = 1	Frame sync length equal 1 bit
WL1-WL0	bits = 10	Word length set to 16 bits
DC4_DC0	bits = 0000	Number of time slot (1)

IV.3 - TEXAS INSTRUMENTS DSP (see Figure 14)

The SERIAL PORT of the TMS320C5x DSP family has to be programmed through the serial port control register as following :

DLB	bit = 1	With MCM=0 we have CLKX=CLKR (external)
MCM	bit = 0	External clock bit source
FO	bit = 0	Word length is 16 bits
FSM	bit = 1	Frame sync pulse required for each word
TXM	bit = 0	FSX pin is an input

Figure 12

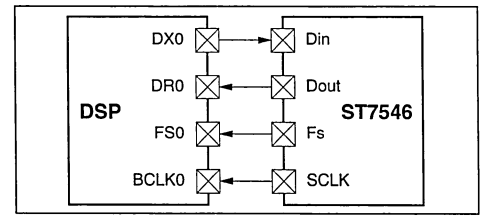


Figure 13

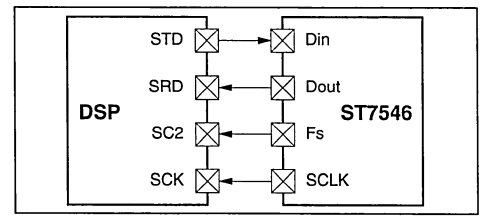
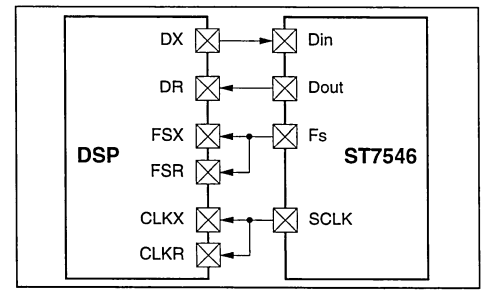


Figure 14

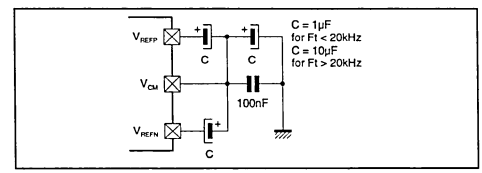


V - ANALOG INTERFACE

V.1 - DAC and ADC Reference Voltage - Common Mode Voltage

These pins provide the positive and negative reference voltage used by the 16-bits convertors (V_{REFP}, V_{REFN}). These pins should be externally decoupled with respect to V_{CM} which is the common mode voltage equal to (AV_{DD} - AGND) / 2. V_{CM} should be externally decoupled with respect to the ground.

Figure 15



V - ANALOG INTERFACE (continued)

V.2 - Analog Outputs (OUT+, OUT-)

The analog outputs are the output of the fully differential analog smoothing filter. Outputs OUT+ and OUT- provide analog signals with maximum peak to peak amplitude 2 x V_{REF}, and must be followed by an external two pole smoothing filter (V_{REF} = V_{REFP} - V_{REFN} = 2.5V). The cut-off frequency of the external filter must be greater than 2 x FS (sampling frequency), so the combined frequency response of both the internal and external filters is flat in the passband.

Different output stage could be realized :
- Fully differential output filter (Figure 16)
- Single ended output filter (Figure 17)
- Single ended mono supply (Figure 18)

Figure 16 : Fully Differential Output Filter

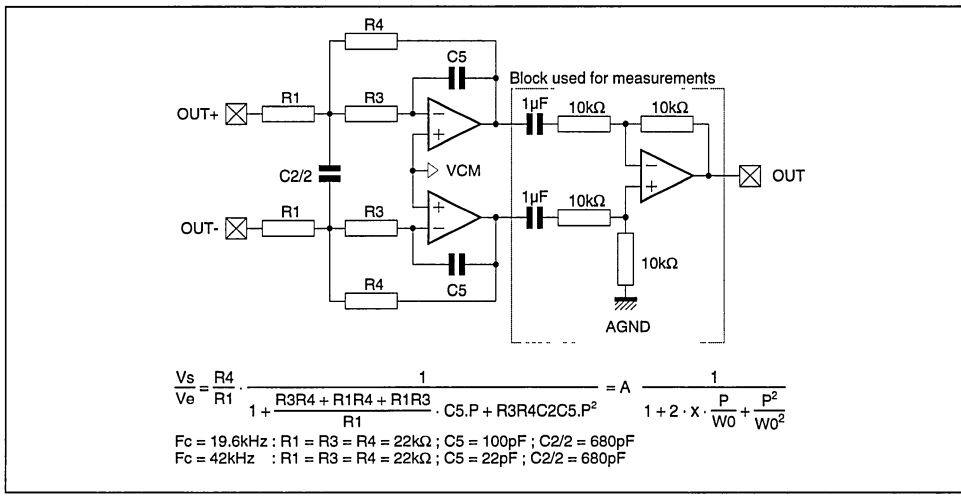


Figure 17 : Single-ended Output Filter

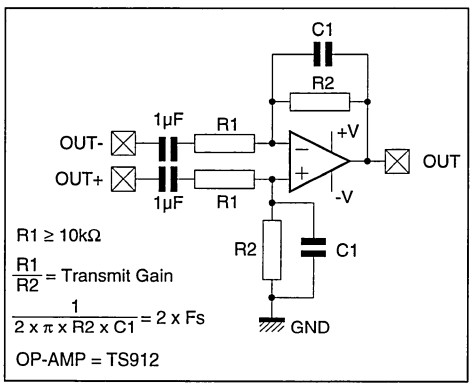
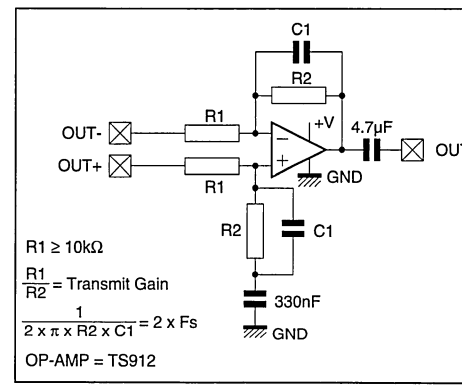


Figure 18 : Single-ended Mono Supply



V - ANALOG INTERFACE (continued)

V.3 - Analog Inputs (IN+, IN-, AUX IN+, AUX IN-)

These pins are the differential ADC input.

The analog input signal is presented to the sigma-delta modulator via a multiplexer (IN or AUX IN).

The analog input peak to peak differential signal range must be less than than two times V_{REF} and must be preceded by an external single pole anti-aliasing filter.

The cut-off frequency of the filter must be lower than one half the over-sampling frequency (MCLK). The filter should be as close as possible to the input pins (IN or AUX IN).

Figure 19 : Differential Input Filter

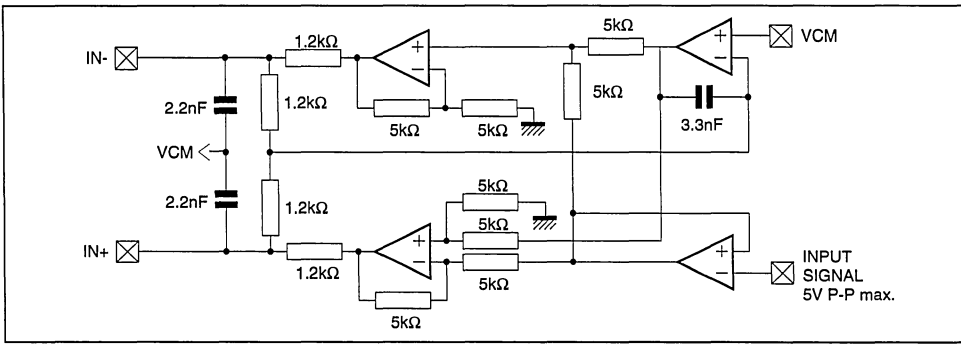
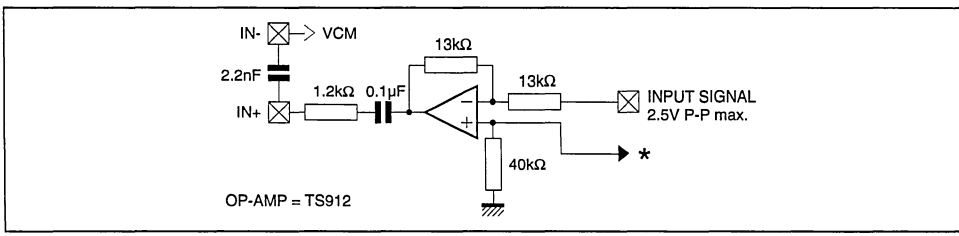
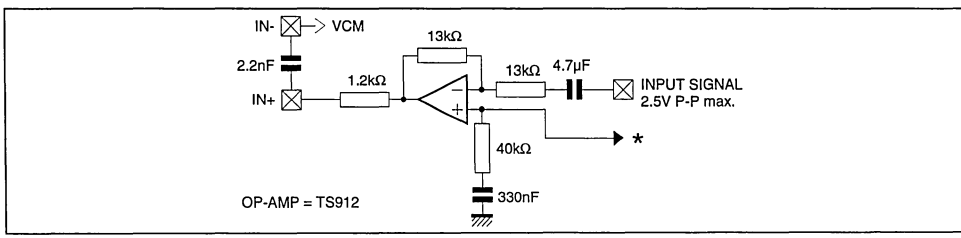


Figure 20 : Single-ended Input Filter



Note : In complete Modem application the node (*) is connected to transmit output throught a 40kΩ resistor.

Figure 21 : Single-ended Input Filter Mono Supply



Note : The node (*) is connected to the transmit output with a 40kΩ resistor which fix the common mode.

VI - PERFORMANCES

We have seen 3 differents kind of analog interface :
- Case A : fully differential
- Case B : single-ended
- Case C : single-ended mono supply

VI.1 - Fully Differential

The measurements have been done with a RODHE&SCHWARZ AUDIO ANALYZER 2Hz-300kHz UPD.

Figure 22 is the output spectrum on the receive side, the analog input signal is at 1kHz / -9dBr (relative to V_{REF}).We have the total harmonic distorsion + noise equal to -85dB.The sampling frequency is 9.6kHz and oversampling ratio equal to 160.

Figure 23 is the output spectrum on the receive side, the analog input signal is at 2kHz / -9dBr (relative to V_{REF}).We have the total harmonic distorsion + noise equal to -78dB. The sampling frequency is 22.5kHz and the oversampling ratio is equal to 96.

Figure 24 is the output spectrum is obtained in digital loop-back so we input an analog input signal on the receive side and we measure the analog output signal with rejector on fondamental (transmit and receive noise are added in this case).

The input level is -20dBr at frequency 1kHz.

In the following chart (Figures 26 and 27) we can see the complete dynamic range of the receive side alone and the receive plus transmit (in that case the transmit and receive noise are added).

The measurements have been done for two sampling frequency 9.6kHz and 22.5kHz.

VI.2 - Single-ended Application Board (ST7546DEMO1B)

The measurements have been done with a R&S audio analyzer and ST DSP emulator PC board. The complete schematics of the demoboard are given in annexe.

***Transmit Side** (D/A)*

We generate a digital waveform at 1kHz and the DSP send the word to the AFE whose output is connected to the R&S analyzer (Figures 25, 28).

***Receive Side** (A/D)*

For testing the receive side we use a sine generator type 1051 from BRUEL & KJAER for the input signal and we perform a Fast Fourier Transform on the digital receive signal (Figures 29, 30).

VI.3 - Single-ended Mono-Supply

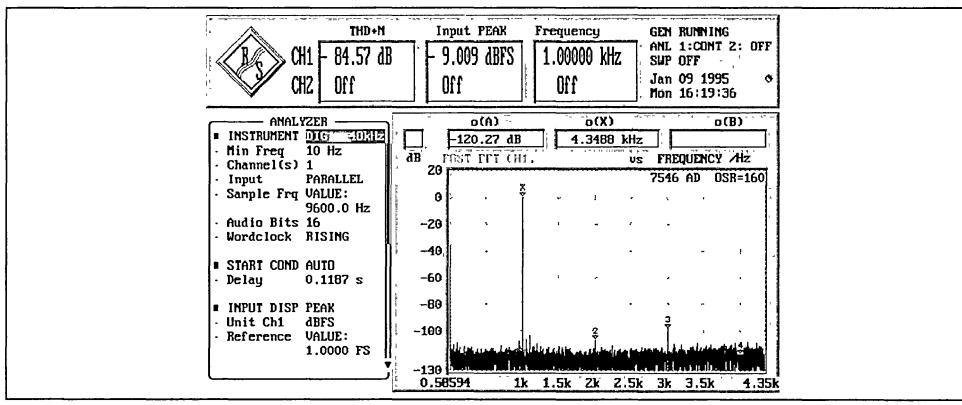
The results of this case are similar to the single-ended ±5V.

VI.4 - Conclusions

We have seen different type of analog interface differential and single-ended.We observe difference of around 2dB between the two types.

With standard two layers printed circuit board (ST7546DEMO1B) we have outstanding performances at least 92dB of dynamics.

Figure 22



VI - PERFORMANCES (continued)

Figure 23

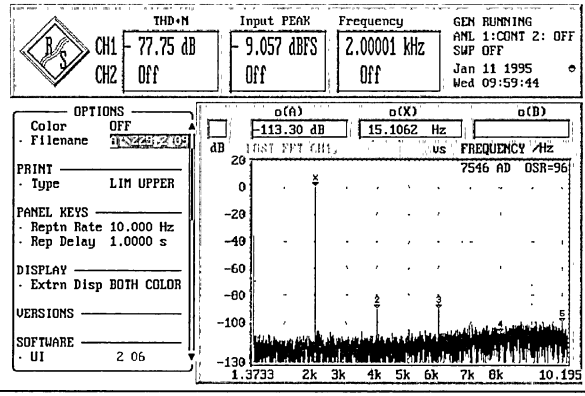


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Figure 24

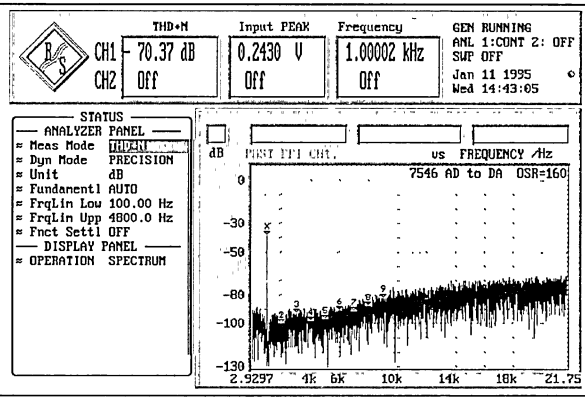

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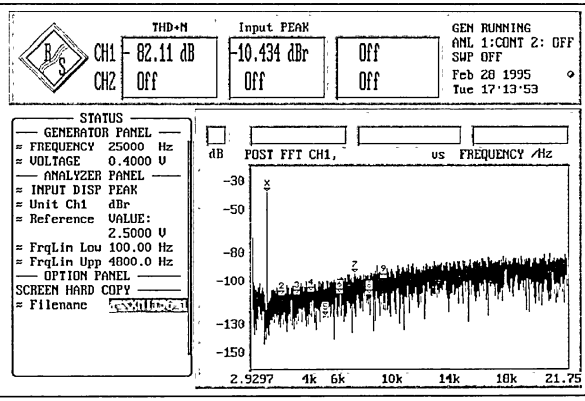
Figure 25



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VI - PERFORMANCES (continued)

Figure 26 : F_S = 9.6kHz, MCLK = 1.536MHz and OVER = 160

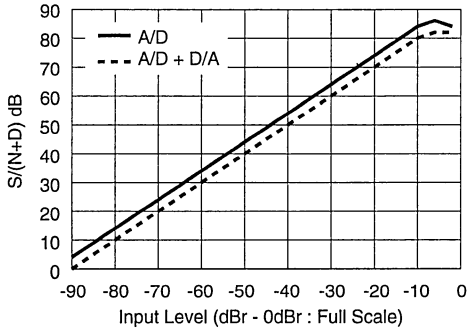


Figure 27 : F_S = 22.5kHz, MCLK = 2.16MHz and OSR = 96

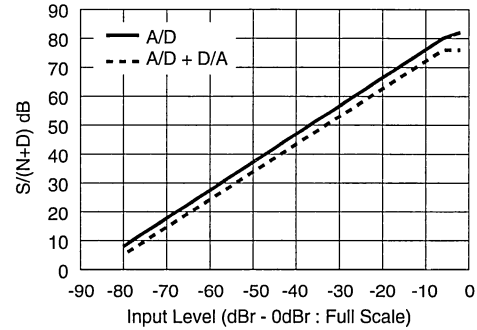


Figure 28 : F_S = 9.6kHz, MCLK = 1.536MHz and OSR = 160

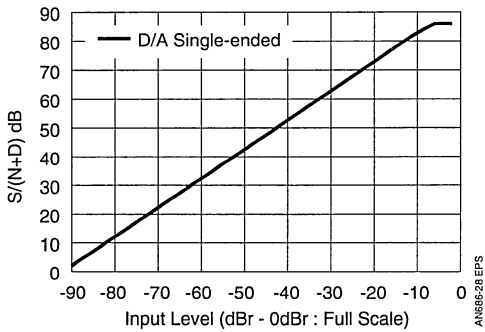


Figure 29 : F_S = 9.6kHz, MCLK = 1.536MHz and OSR = 160

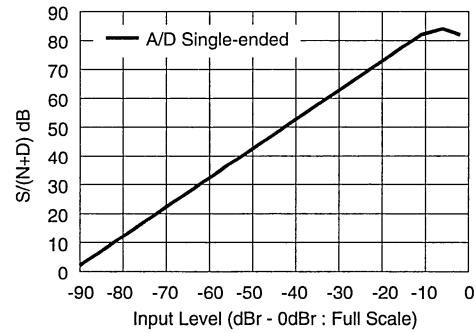
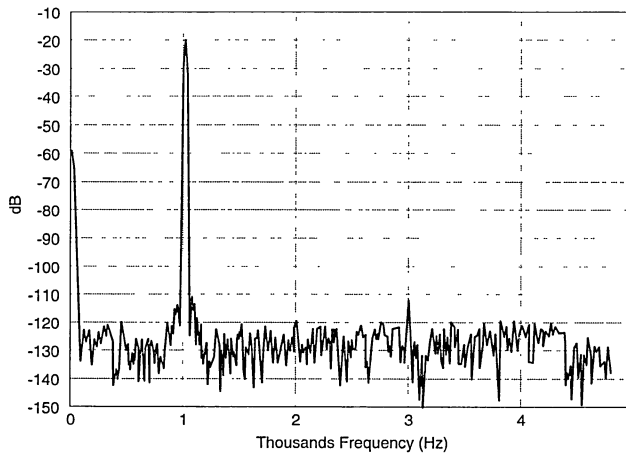
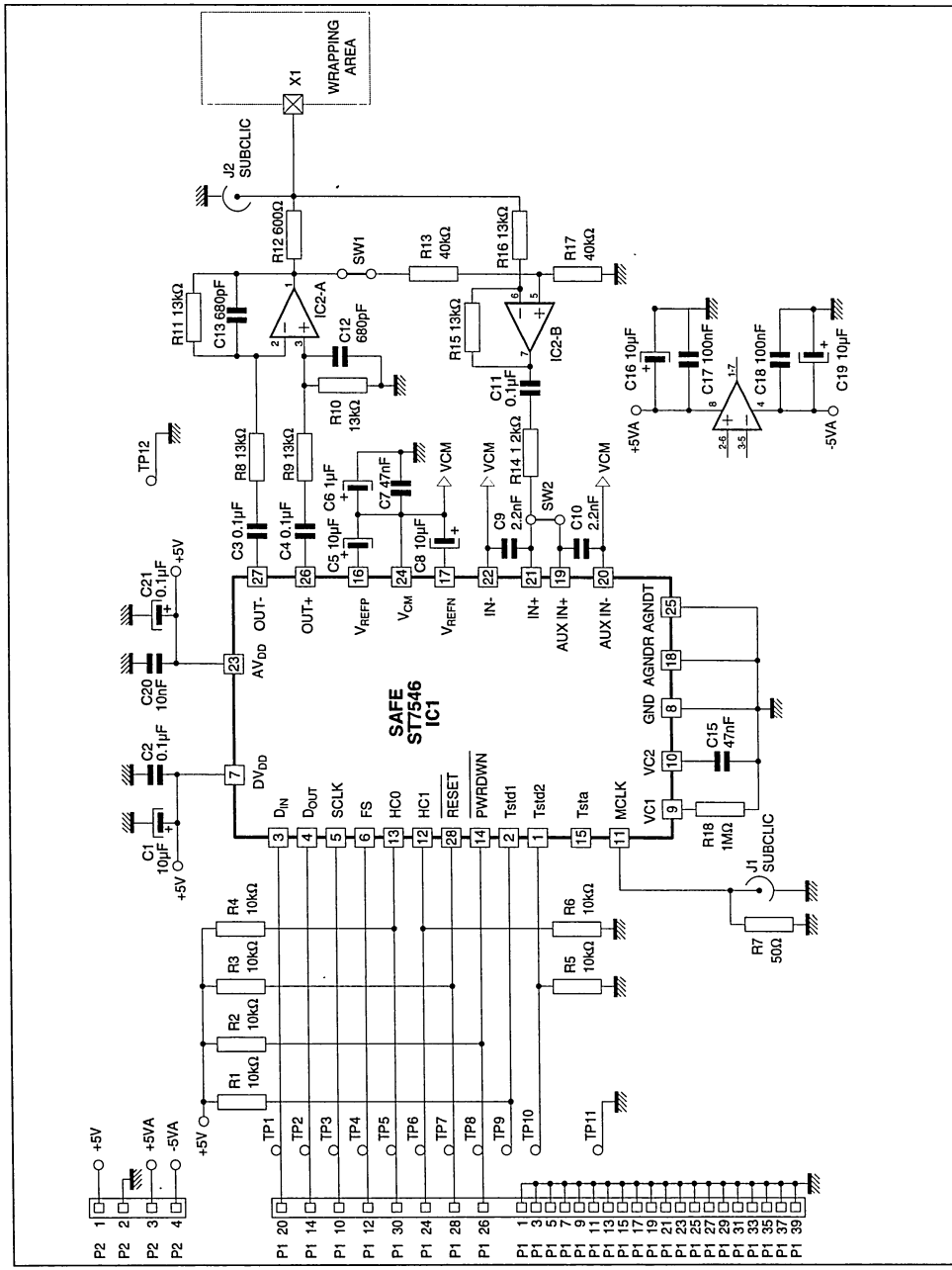


Figure 30 : F_S = 9.6kHz, MCLK = 1.536MHz



VII - ANNEXE : ST7546DEMO1B SCHEMATICS AND LAYOUT

Figure 31



VII - ANNEXE : ST7546DEMO1B SCHEMATICS AND LAYOUT (continued)

Figure 32

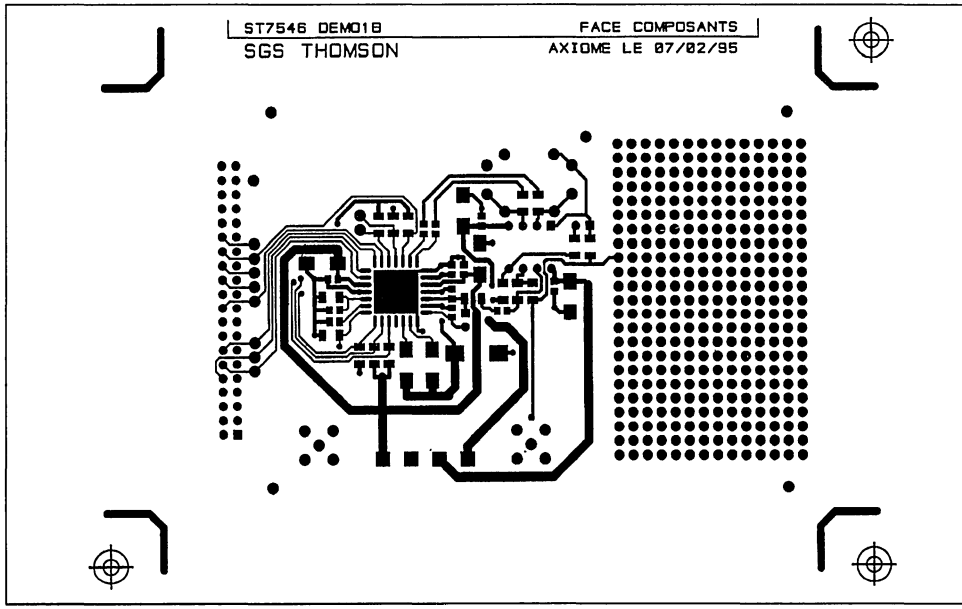
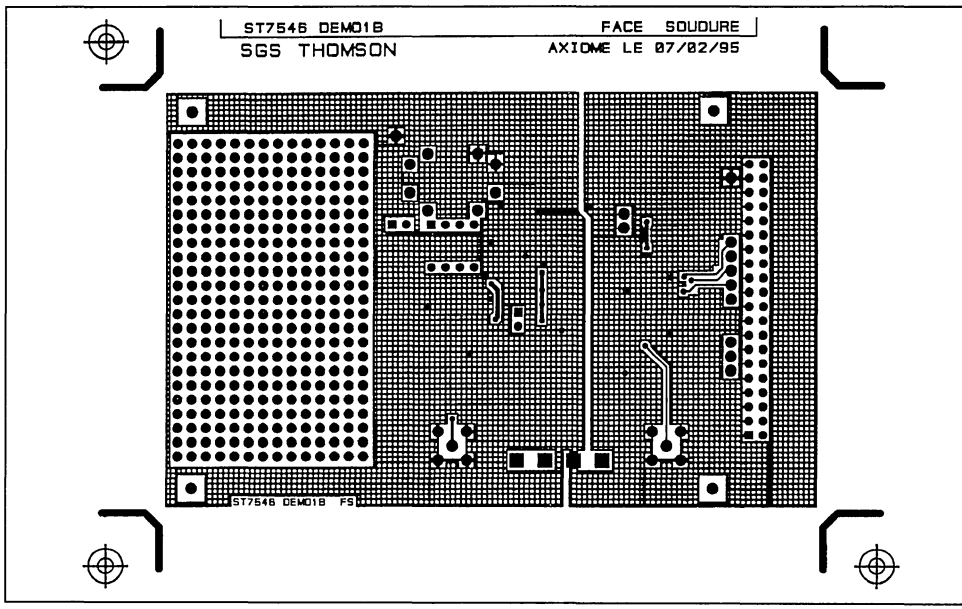


Figure 33



VII - ANNEXE : ST7546DEMO1B SCHEMATICS AND LAYOUT (continued)

Figure 34

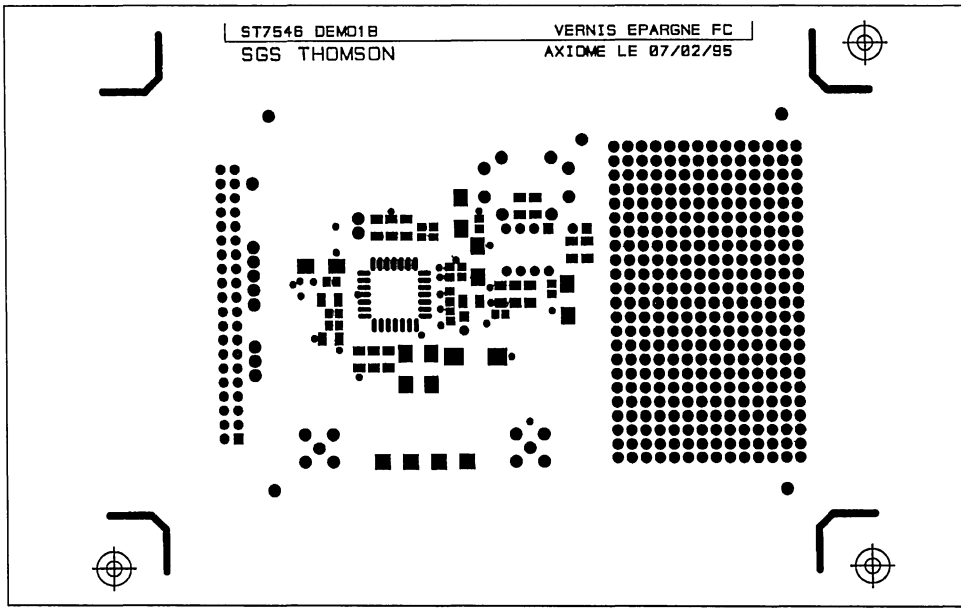
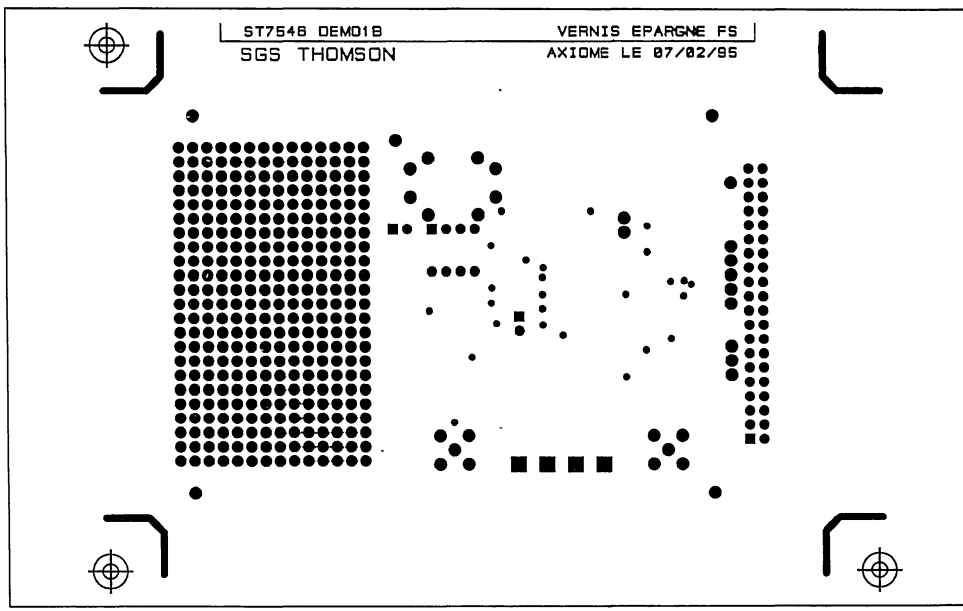
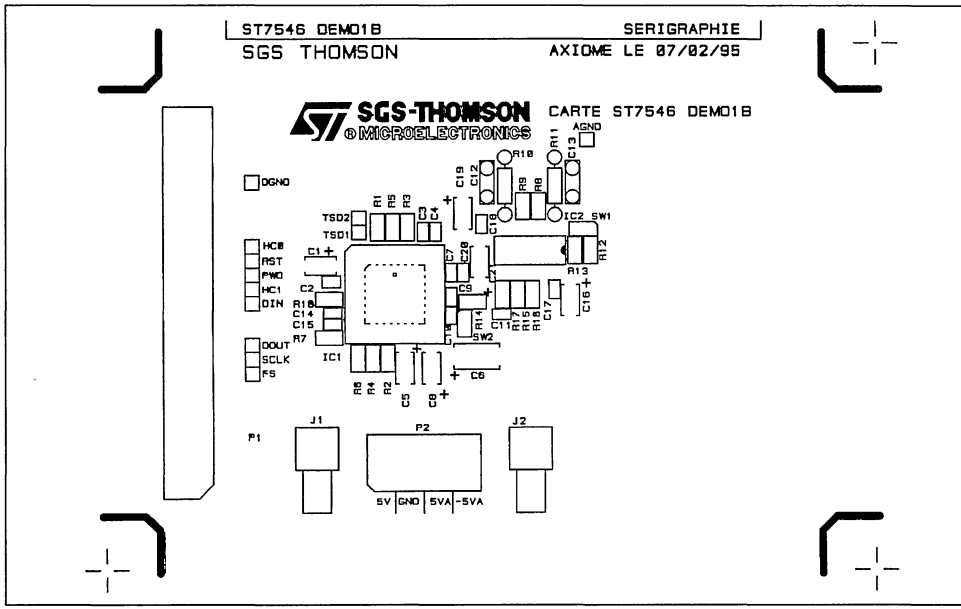


Figure 35



VII - ANNEXE : ST7546DEMO1B SCHEMATICS AND LAYOUT (continued)

Figure 36



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

A STEREO AUDIO SOLUTION FOR MULTIMEDIA APPLICATIONS USING TWO ST7546 A/D AND D/A CONVERTERS

ST7546 is a general-purpose signal processing Analog Front End, dedicated to full audio band applications.

ST7546 basically has to be connected to the serial interface of a DSP for data exchanges, and to a DAA (Data Access Arrangement) on analog side, which can be simply implemented as a differential to single ended amplifier on output and only an amplifier on signal input.

Main signals on the ST7546 host interface are :

- Din, data serial input : 16 bits per frame from DSP.
- Dout, data serial output : 16 bits per frame to the signal processor.
- FS, frame synchronisation provided to the host.
- SCLK, serial bit clock also provided to the processor, which is MCLK.
- NRESET, reset from host to ST7546.

The goal of note is to describe a simple way to manage at least two ST7546 Analog Front End from a single DSP.

Let's have a look on the startup sequence of the device from a reset pulse. The first FS falling edge will be generated after a number of cycles depending on the programmed value of N : 32 x N + offset as showned on Figure 1. So if data has to be sent just after reset the device, designer must take care of this delay.

Data word input/output are available after the falling edge of the Frame Synchronisation output of the device, and are sampled during the sixteen first cycles of clock after the frame synchronization signal.

So, to control a pair of ST7546, the DSP has to send and receive 32 bits words, where the first 16 bits are dedicated to the left audio channel, and second half to the right side for example. Each device must be synchronized on the NRESET signal provided by the signal processor.

A synchronous reset block is needed, where a single sequence of two sixteen MCLK cycles delayed signals NRESET1 and NRESET2, is gener-

Figure 1

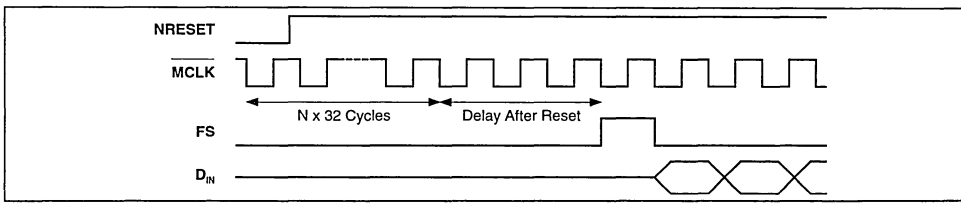
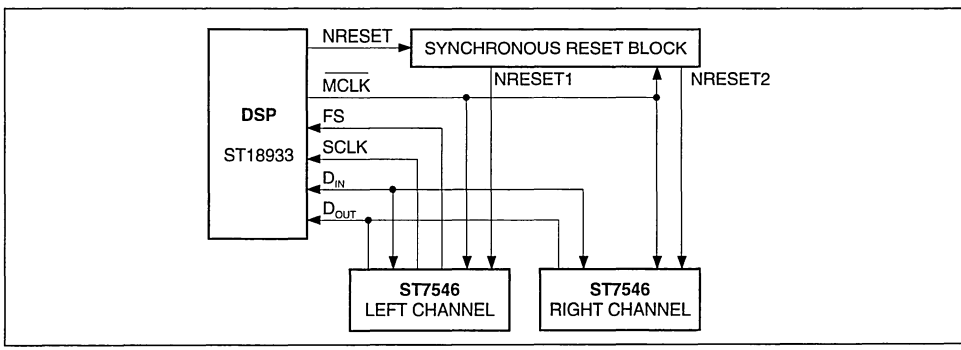


Figure 2



ated after the master reset NRESET (Figure 2). Both ST7546 are supposed to be in the same mode selected with HC0 and HC1 pins.

Figure 3 shows the phase delay between FS_left connected to the DSP, and FS_right.

For the processor, everything is like if there is a single interface on an hardware point of view ; the second ST7546 may be considered as a slave part. For correct control of data flow to dual ST7546 system, a burst must be generated by the processor as shown on Figure 4.

The synchronous reset block can be simply implemented with one synchronous 4 bits counter, two type D flip-flops, and three nand gates (Figure 5).

Figure 3

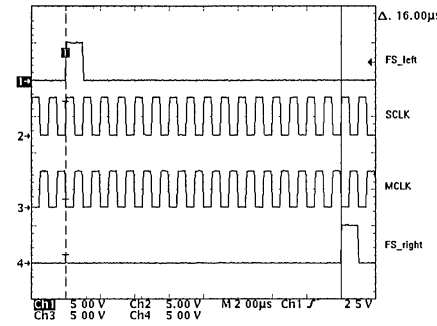


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Figure 4

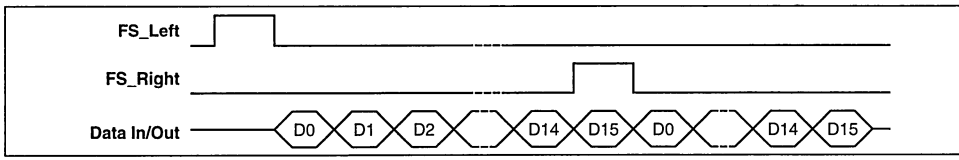

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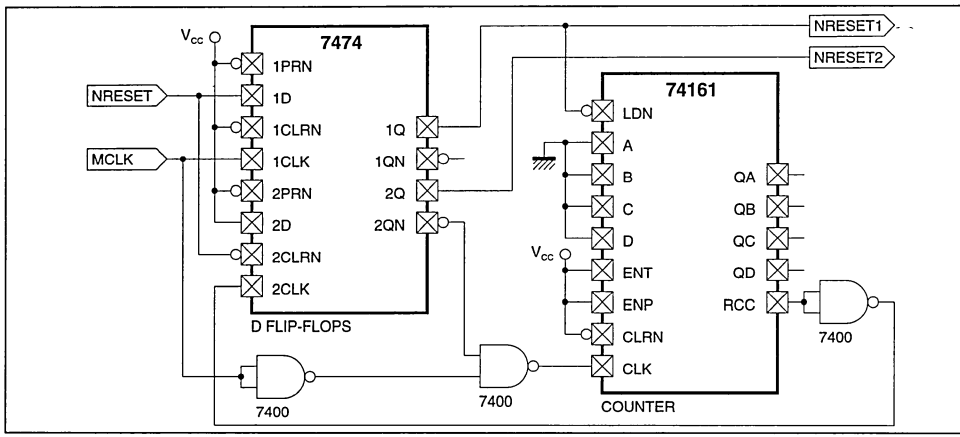
Figure 5



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HIGH SPEED MODEM

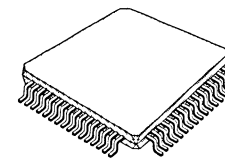
SGS-THOMSON MICROELECTRONICS

ST7548

PCMCIA AND PC GENERAL PURPOSE INTERFACE

ADVANCE DATA

- PCMCIA AND PC GENERAL PURPOSE INTERFACE (MODEM, ISDN, MULTIMEDIA)
- ExCA™ COMPATIBLE (see Note 1)
- 494 BYTES INTERNAL RAM WITH BUS ARBITRATION
- PCMCIA CONFIGURATION REGISTERS (R0, R1)
- CONFIGURABLE I/O DECODER
- I^2C EEPROM INTERFACE (256 BYTES)
- 16C550 UART
- CONFIGURABLE CLOCK GENERATOR
- I/O - MCU - MEMORY EXTENSION 8 BITS PORT
- HIGH THROUGHPUT :
  - 115200Bps THROUGH UART
  - 2MBYTES THROUGH RAM
- 3.3V OR 5V SUPPLY (±10%)
- LOW POWER
- SMALL OUTLINE TQFP80 PACKAGE
- ALSO AVAILABLE WITH COMPLETE MODEM CHIP SET



TQFP80
(Plastic Package)

ORDER CODE : ST7548CQFP

GENERAL DESCRIPTION

The ST7548 is a flexible interface for the PCMCIA and PC buses mainly dedicated to telecommunications. It is fully in accordance with PCMCIA standard and is designed to be coupled to a modem. It includes a 16C550 compatible UART, a 494 bytes internal memory, an I^2C interface allowing chip initialization from an external EEPROM, and a programmable clock generator.

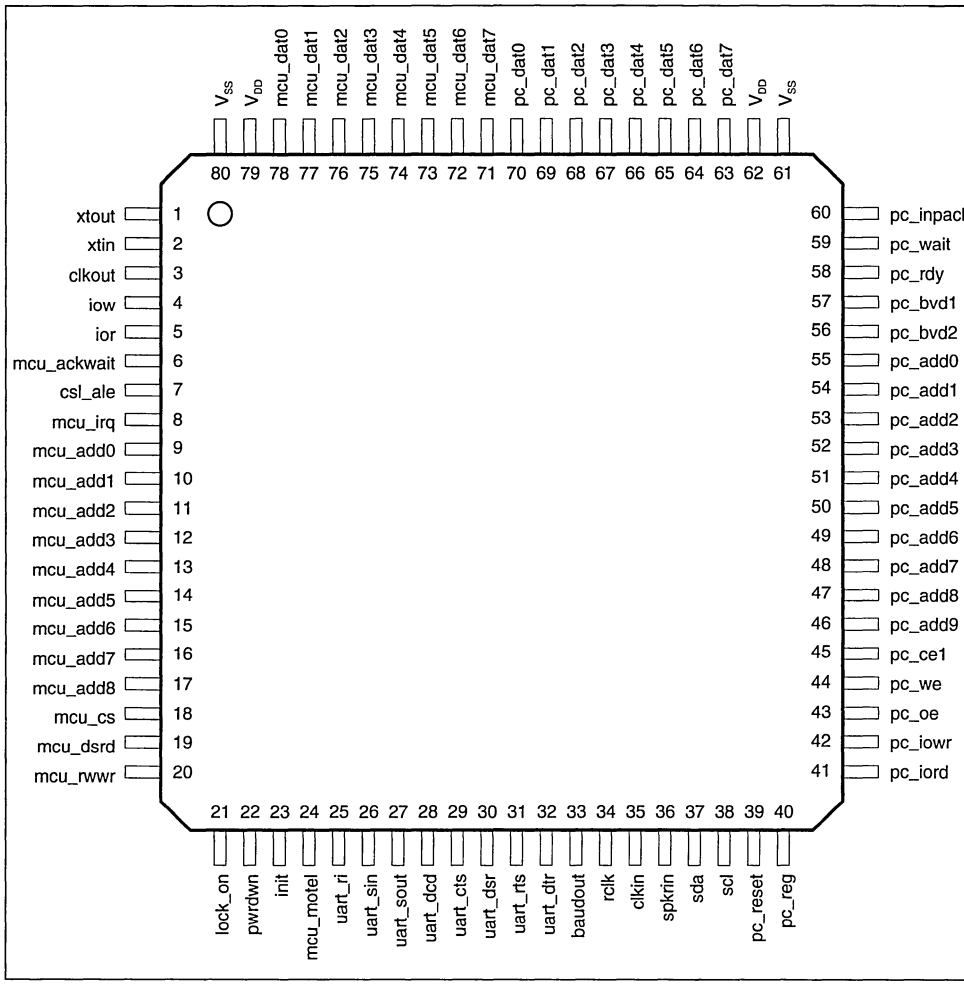
It also includes a configurable port which can be used either as I/O or memory extension or as an interface to a wide range of microprocessors. In this case, using the internal memory, high speed data transfers can be achieved between the PC and the application.

It is realised in an ultra-flat TQFP80 package suitable for PCMCIA cards.

Note : 1. ExCa is a trademark of Intel Corporation.

CONTENTS

I - PIN CONNECTIONS



II - PIN DESCRIPTION

Name	Pin	Type	Function
POWER PINS (ALL THE POWER AND GROUND PINS MUST BE CONNECTED)			
V_{DD1}	62	Power	DC Supply
V_{DD2}	79	Power	DC Supply
V_{SS1}	61	Ground	DC Ground
V_{SS2}	80	Ground	DC Ground
PC address bus			
PC_ADD_0	55	I	PCMCIA Address Bus Bit 0 (LSB)
PC_ADD_1	54	I	PCMCIA Address Bus Bit 1
PC_ADD_2	53	I	PCMCIA Address Bus Bit 2
PC_ADD_3	52	I	PCMCIA Address Bus Bit 3
PC_ADD_4	51	I	PCMCIA Address Bus Bit 4
PC_ADD_5	50	I	PCMCIA Address Bus Bit 5
PC_ADD_6	49	I	PCMCIA Address Bus Bit 6
PC_ADD_7	48	I	PCMCIA Address Bus Bit 7
PC_ADD_8	47	I	PCMCIA Address Bus Bit 8
PC_ADD_9	46	I	PCMCIA Address Bus Bit 9 (MSB)
PC DATA BUS			
PC_DAT_0	70	I/O	PCMCIA DATA Bus Bit 0 (LSB)
PC_DAT_1	69	I/O	PCMCIA DATA Bus Bit 1
PC_DAT_2	68	I/O	PCMCIA DATA Bus Bit 2
PC_DAT_3	67	I/O	PCMCIA DATA Bus Bit 3
PC_DAT_4	66	I/O	PCMCIA DATA Bus Bit 4
PC_DAT_5	65	I/O	PCMCIA DATA Bus Bit 5
PC_DAT_6	64	I/O	PCMCIA DATA Bus Bit 6
PC_DAT_7	63	I/O	PCMCIA DATA Bus Bit 7 (MSB)
PC CONTROL SIGNALS			
PC_CE1	45	I Pull-up	Chip-select. Active low.
PC_WE	44	I Pull-up	Memory Write Enable. Active low.
PC_OE	43	I Pull-up	Memory Output Enable. Active low.
PC_IOWR	42	I Pull-up	I/O Write Enable. Active low.
PC_IORD	41	I Pull-up	I/O Read Enable. Active low.
PC_REG	40	I Pull-up	Common (1) or Attribute (0) Memory Indicator
PC_RESET	39	I, Trigger	Hard Reset. Active high.
PC_INPACK	60	O	I/O Read Indicator (0 indicates that an I/O read access is being performed)
PC_WAIT	59	O	Wait Signal. Active low.
PC_RDY	58	O	Ready/Interrupt Active Low : In all modes, indicates when low that the circuit Is under initialization (CIS being read or written). If no EEPROM is connected, PC_RDY remains low after reset until the MCU writes something in the PROGN register. In I/O modes(2), transmits the interrupt coming from the UART, the I/O port or the RAM.
PC_BVD1	57	O	In memory modes : always 1. In I/O modes : if RINGEN = 1, reproduces UART_RI. if RINGEN = 0, always 1.
PC_BVD2	56	O	In memory modes : always 1. In I/O modes : if AUDIO = 1, reproduces SPKRIN. if AUDIO = 0, always 1.

II - PIN DESCRIPTION

Name	Pin	Type	Function
MCU ADDRESS BUS			
MCU_ADD_0	9	I	MCU Address Bus Bit 0 (LSB)
MCU_ADD_1	10	I	MCU Address Bus Bit 1
MCU_ADD_2	11	I	MCU Address Bus Bit 2
MCU_ADD_3	12	I	MCU Address Bus Bit 3
MCU_ADD_4	13	I	MCU Address Bus Bit 4
MCU_ADD_5	14	I	MCU Address Bus Bit 5
MCU_ADD_6	15	I	MCU Address Bus Bit 6
MCU_ADD_7	16	I	MCU Address Bus Bit 7
MCU_ADD_8	17	I	MCU Address Bus Bit 8 (MSB)
MCU - I/O - MEMORY EXTENSION DATA BUS(3)			
MCU_DAT_0	78	I/O	MCU, I/O or Memory Extension Data Bus Bit 0 (LSB)
MCU_DAT_1	77	I/O	MCU, I/O or Memory Extension Data Bus Bit 1
MCU_DAT_2	76	I/O	MCU, I/O or Memory Extension Data Bus Bit 2
MCU_DAT_3	75	I/O	MCU, I/O or Memory Extension Data Bus Bit 3
MCU_DAT_4	74	I/O	MCU, I/O or Memory Extension Data Bus Bit 4
MCU_DAT_5	73	I/O	MCU, I/O or Memory Extension Data Bus Bit 5
MCU_DAT_6	72	I/O	MCU, I/O or Memory Extension Data Bus Bit 6
MCU_DAT_7	71	I/O	MCU, I/O or Memory Extension Data Bus Bit 7 (MSB)
MCU - I/O - MEMORY EXTENSION CONTROL SIGNALS			
MCU_CS	18	I	Chip Select. Active low
MCU_DSRD	19	I	Data Strobe or Read Enable, depending on MCU_MOTEL (active low)
MCU_RWWR	20	I	Read-Write or Write Enable, depending on MCU_MOTEL (active low)
MCU_MOTEL	24	I	Motorola (1) or Intel (0) Like Bus Style
MCU_ACKWAIT	6	O open collector	Wait or Acknowledge depending on MCU-MOTEL (active low)
CSL_ALE	7	I/O	In memory extension mode : output, active low. Indicates (when 0) an access to the memory extension. In I/O extension mode : output, active low. Indicates (when 0) that the I/O port address has been recognized. In other modes : address latch enable input active high. It is used when the MCU data bus is multiplexed to validate the 8 lsb's of the address on MCU_DAT. The address is latched inside the circuit when CSL_ALE goes low. When the MCU bus is not multiplexed, CSL_ALE must be connected to 0.
MCU_IRQ	8	I/O open collector	In memory extension mode : output, not used. In I/O extension mode : interrupt input active low, transmitted to the PC on the PC_RDY pin. In other modes : interrupt output towards the MCU, active low.
IOW	4	O	In memory extension mode : reproduces PC_WE. In I/O extension mode, reproduces PC_IOW when the I/O port address is recognized (otherwise takes value 1). In other modes : remains at 1.
IOR	5	O	In memory extension mode : reproduces PC_OE. In I/O extension mode, reproduces PC_IOR when the I/O port address is recognized (otherwise takes value 1). In other modes : remains at 1.

II - PIN DESCRIPTION

Name	Pin	Type	Function
UART RELATED PINS			
UART_RI	25	I	Ring Input : can be reproduced on PC_BVD1
UART_SIN	26	I	Serial Input
UART_SOUT	27	O	Serial Output
UART_DCD	28	I	Data Carrier Detect
UART_CTS	29	I	Clear To Send
UART_DSR	30	I	Data Set Ready
UART_RTS	31	O	Request To Send
UART_DTR	32	O	Data Terminal Ready
BAUDOUT	33	O	UART Transmit Clock
RCLK	34	I	Receive Clock for the UART
SERVICE PORTS			
INIT	23	O	Initialization signal provided by the chip for use on the PCMCIA card. It is active high when the card receives a hard or a soft reset.
PWRDWN	22	O	Reproduces Bit PWRDWN of Register R1. active high.
LOCK_ON	21	I	Two consecutive rising transitions on this signal put the chip in stand-by : CLKOUT receives MCU_DIV output instead of the internal clock, unless between these two transitions, stand-by procedure is cancelled. Stand-by procedure is cancelled when any of UART_RI or UART_SOUT goes low, or when any of PWRDWN or PC_RESET goes high.
CLKIN	35	I	Alternate Clock Input. (possibly delivered by a data-pump modem). It is either this clock (when Bit 3 of PROGN register is '1'), or the internal oscillator clock (when Bit 3 of PROGN register is '0') which will be used by UART_DIV to produce the CLOCK for the internal UART.
CLKOUT	3	O	Output Clock Available for a MCU. It is either the internal oscillator clock, or the clock coming from MCU_DIV in stand-by mode when it is desired to reduce the MCU's power consumption.
XTIN	2	I	Oscillator Input. Can be connected either on an external quartz to use the internal oscillator, or on an external oscillator output. The clock on this pin is the one which is used internally by the circuit to operate its internal logic and state machines. The clock used by the UART can come from XTIN or from CLKIN after a division to get the proper frequency.
XTOUT	1	O	Internal Oscillator Output. When the internal oscillator is used, to be connected on the other pin of the quartz crystal.
SPKRIN	36	I	Speaker Input. This input can be reproduced on PC_BVD2 output in I/O mode when AUDIO Bit is one.
I^2C LINE (PORTS RELATED TO THE EXTERNAL EEPROM)			
SDA	37	I/O open collector	I^2C Bus Data Line
SCL	38	I/O open collector	I^2C Bus Clock Line. Although this pin is inout, the circuit only uses this Pin as an out Pin. For this reason, one cannot modify the I^2C line frequency by forcing SCL low from outside the chip.

Notes :

1. Memory mode : mode for which, depending on the value of bits UE, MODE0, MODE1 in R0 register, only common or attribute memory accesses are allowed (i.e., no I/O access is allowed).
2. I/O mode : mode for which, depending on the value of bits UE, MODE0, MODE1 in R0 register, only attribute memory and I/O accesses are allowed (i.e., no common memory access is allowed).
3. A number of pins can be used in different ways either to connect a MCU or to connect a memory extension or an I/O extension. These pins are MCU_DAT[7..0], MCU_IRQ, CSL_ALE, IOW and IOR. This corresponds to three different behaviours for the circuit.

III - BLOCK DIAGRAMS

The here under schematic shows the main functions and data flows of the chip.

The CIS (Card Information Structure in PCMCIA terminology) is a memory and registers area which describes the PCMCIA card configuration. During chip initialization, it is loaded from an external EEPROM through the I^2C channel (this is the normal behaviour when such a memory is present) or from the MCU (if no E2PROM is connected ; in this case, loading the CIS is under the MCU's responsibility).

The RAM allows high speed transfers between the PC and the MCU.

The 16C550 compatible UART may exchange informations with another compatible UART.

When no MCU is necessary, it is possible to connect instead a peripheral requiring an 8 bits parallel interface, or an 8 bits memory extension. There is only one set of ports for the MCU, the peripheral and the memory extension. Therefore, only one of them may be connected at a time on the chip.

After reset, the RAM memory contains the CIS (loaded from the EEPROM through the I^2C bus, or by the MCU). The RAM is also used to exchange information between the PC and the MCU. Its capacity is 494 bytes (hexadecimal addresses ranging from x"000" to x"1ED"). It is organized in such a way that the CIS does not take all the available room. Thus it is possible to perform exchanges between the PC and the MCU while keeping the CIS available for read.

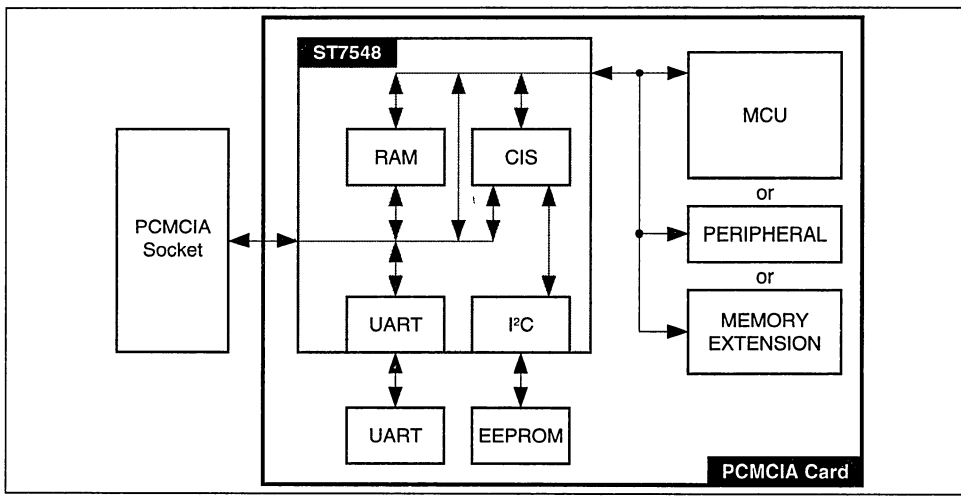
The clocks block produces the necessary clock signals. It contains multiplexers and frequency dividers which can be programmed with the PROGN register. With its internal oscillator, it delivers the external clock CLKOUT which can be used to drive a MCU. It provides the UART with the required clock, building it either from the internal oscillator, or from the external clock input CLKIN. It incorporates programmable dividers which allow to adapt the different clock frequencies.

The registers are used to configurate the chip and to synchronise data transfer between the PC and the MCU.

The circuit considers that they are three masters : the PCMCIA, the MCU and the I^2C interfaces. The registers and the memory can be reached by the masters. The table in paragraph IV.11 "ADDRESSING CAPABILITIES TABLE" shows the access permission. Each device which is supposed to be reached by at least two masters is placed on a common internal bus. An arbitration logic manages the resulting access conflicts. For this reason, accessing one of the registers or memory placed on the common bus makes the related master support WAIT cycles.

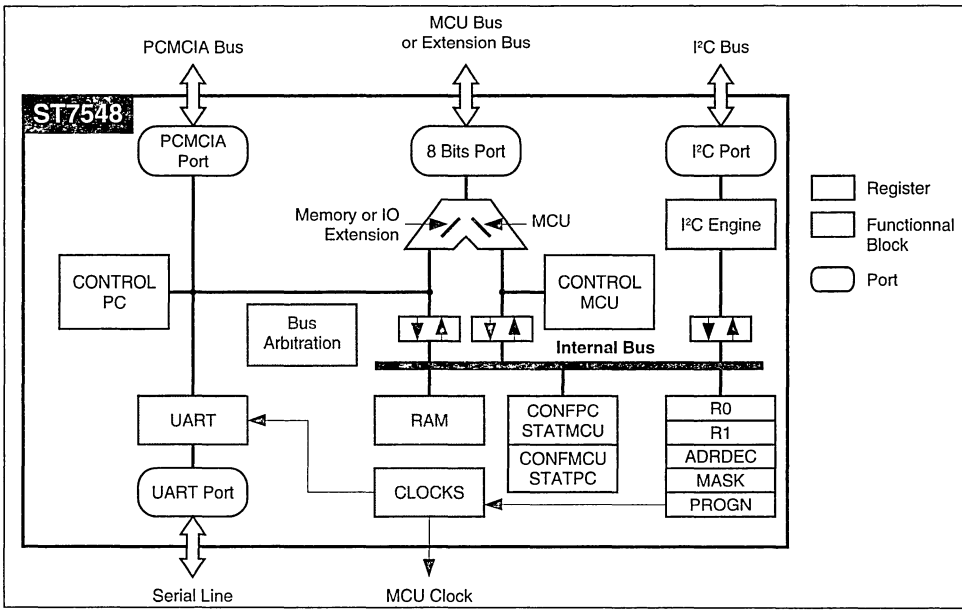
The addresses are given in the table. Two elements can be placed at variable addresses : the UART and the I/O port. For the first one, the address is defined in the R0 register ; for the second one, it is defined in the ADRDEC register, and the recognized address field width is defined in the MASK register.

Figure 1 : Simplified Block Diagram of the Data Flows Allowed by the Chip



III - BLOCK DIAGRAMS (continued)

Figure 2 : Chip Block Diagram



IV - FUNCTIONNAL DESCRIPTION

IV.1 - PCMCIA ADDRESSING MODES

Through a PCMCIA port, a computer may perform its accesses in three different modes : the common memory mode, the attribute memory mode, and the I/O mode.

The usual addressing mode for memory is common memory mode. The PC_REG signal is '1', and the PC_OE and PC_WE signals are used as read/write signals.

The attribute memory mode is mainly used to read configuration information (in registers or memory) of the PCMCIA cards. It differs from the common memory mode in that the PC_REG signal is '0'.

The I/O mode is used to access I/O ports. In this case, the PC_REG is '0' and the read/write signals are PC_IORD and PC_IOWR. The I/O mode allows interrupts to be transmitted to the PCMCIA port. That is why, in the ST7548, the I/O mode can be used not only to access the I/O port, but also to access the memory, thus allowing to synchronize data transfer between the MCU and the PC using interrupts.

In the ST7548, from the PC (or PCMCIA) point of view, there are registers, a memory, an UART, an I/O port and a memory extension port. Each of them cannot be addressed in any mode. For example, the UART and the I/O port can be addressed only in I/O mode. The table in paragraph IV.11 "ADDRESSING CAPABILITIES TABLE" shows in the PCMCIA columns under which conditions the PCMCIA port accesses the different blocks in the circuit, and when the circuit generates a wait state to the PCMCIA interface. It also shows what can be addressed by the MCU (and if a WAIT is sent to the MCU), and what can be reached by the I^2C channel.

IV - FUNCTIONNAL DESCRIPTION (continued)

IV.2 - CLOCKS (Figure 3)

Introduction

The circuit includes an oscillator (XTIN and XTOUT pins) which has been tuned for frequencies ranging from 12 to 24MHz. This oscillator requires an external quartz crystal. It is also possible to operate the circuit at frequencies outside this range, but in this case a quartz crystal cannot be used : an external oscillator must deliver the desired frequency on the XTIN pin. Regardless of its origin, the clock present on XTIN becomes internally CLK, the basic clock of the ST7548. CLK is also named "internal oscillator clock". It is used to operate the internal logic of the chip (state machines and others).

The circuit delivers the CLKOUT clock which relies on the internal oscillator clock. CLKOUT can be used as the basic clock for an MCU placed outside the ST7548. In stand-by, CLKOUT can be slowed down owing to the "MCU_DIV" divider.

The on-chip UART receives the clock which goes out of the frequency divider named "UART_DIV". The input of this divider is either the internal oscillator clock or an external clock connected on CLKIN pin. The division ratios in UART_DIV are well suited to the following clock frequencies : 3.6864MHz, 7.3728MHz, 14.7456MHz, 18.432MHz, 22.1184MHz, 29.4912MHz, 33.1776MHz, 36.864MHz.

The clocks operate in three different ways : normal behaviour, stand-by, and power down.

Normal Behaviour

After reset is released, the clocks run freely, and it is the internal oscillator clock that is sent on UART_DIV. Then, depending on the content of PROGN register bit 3, the UART clock may come from CLK or CLKIN divided in UART_DIV

The MCU_DIV divider is not used : the multiplexer which follows and delivers CLKOUT uses the CLK or CLK/2 input. Thus, on CLKOUT, it is CLK/2 which is issued when PROGN register bit 7 is '0' (default value), and CLK when this bit is '1'.

Stand-by

What is desired in this mode, is to temporarily reduce the PCMCIA card power consumption, but the card remains able to become operational again at any moment.

Putting the card in stand-by depends upon a MCU action. For this, it sends two consecutive rising edges on the LOCK_ON pin. Doing this causes MCU_DIV to become active. This divider then takes into account the division ratio indicated in the PROGN register. The frequency delivered on CLKOUT is then a sub-multiple of CLK. A PC_RESET (active high) or one of the UART signals UART_RI, UART_SOUT at '0' wake up the circuit and put it back in normal mode. In the same way, if one of these signals occurs between the two rising edges on LOCK_ON, the stand-by procedure is cancelled.

Depending upon the way that the circuit is used (use in conjunction with a 75C501 data pump for example), the MCU may also stop the 75C501. In this case, the 18.432MHz frequency is no longer delivered on CLKIN, and the UART is stopped, unless the user links the UART_DIV input to the local oscillator (by programming accordingly the PROGN register). Switching between CLKIN and the local oscillator clock is done in such a way that no glitch nor shortened cycle happens. The counterpart is that the clock cycle may temporarily be longer.

Waking up After a Stand-by

The circuit goes out of stand-by if a reset happens or if at least one of the UART signals UART_RI or UART_SOUT becomes '0' or if PWRDWN becomes '1'.

If the PC wants to wake up the circuit, it can do it with the UART, simply sending a byte to it.

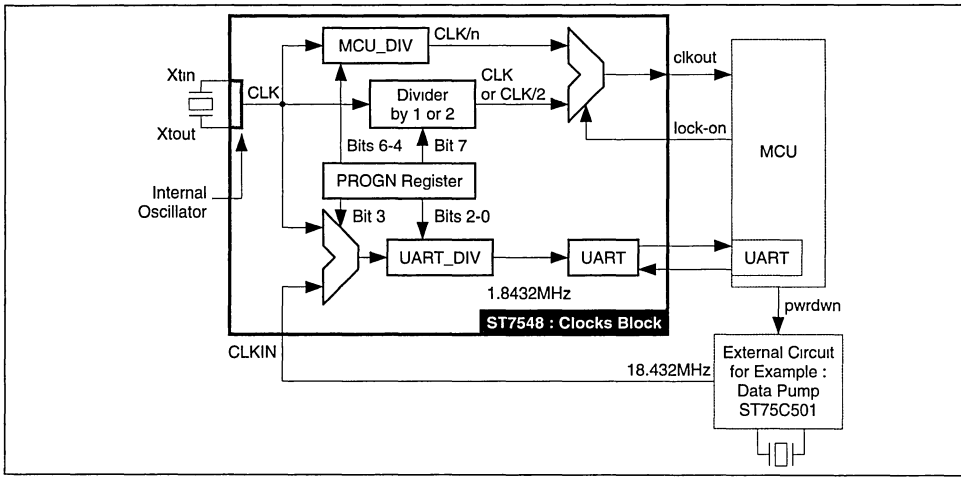
Powerdown Mode

In this mode, the user doesn't intend to use the PCMCIA card on which the circuit is placed. So it is not the UART that will wake it up.

The circuit is placed in powerdown under the PC's responsibility. The PC writes a '1' in R1 register PWRDWN bit. The circuit then no longer delivers any clock neither on CLKOUT nor on the UART, and is no longer able to perform accesses to anything else than the R0 and R1 registers. The circuit will only restart after the PC has written a '0' in the PWRDWN bit.

IV - FUNCTIONNAL DESCRIPTION (continued)

Figure 3 : Theoretical Schematic



IV.3 - UART

The UART is fully compatible with a 16C550 UART. Please refer to the documentation on this type of UART to have a detailed description of its behaviour.

The UART may only be used when the UE bit (Uart Enable) in register R0 is set to '1'. The UART address can be chosen between four values depending on the content of R0 register. The three LSB's of the PCMCIA address bus are transmitted to the UART : they are used to select the internal UART registers. The UART thus covers an 8 bytes address range.

The clock which enters the UART is divided by the value held in DLM and DLL UART registers to produce the NBAUD signal. The most common frequency for the UART clock is 1.8432MHz. The table below shows the required divisor value in DLM-DLL to generate typical baud rates for a set of input frequencies (Table 2).

After reset, DLL and DLM are undefined. They are not affected by reset.

Table 1 : UART Registers

Address (Note 1)	DLAB (Note 2)	Register Name	Comment
0	0	RBR Receiver Buffer Register	Read only
0	0	THR Transmitter Holding Register	Write only
1	0	IER Interrupt Enable Register	
2	X	IIR Interrupt Ident Register	Read only
2	X	FCR Fifo Control Register	Write only
3	X	LCR Line Control Register	
4	X	MCR Modem Control Register	
5	X	LSR Line Status Register	Read only (Note 3)
6	X	MSR Modem Status Register	
7	X	SCR Scratch Register	
0	1	DLL Divisor Latch (LSB)	
1	1	DLM Divisor Latch (MSB)	

Notes : 1. The address given in this column refers to the 3 LSBs of the PCMCIA address bus. The complete address of a register is obtained by adding the indicated address and the one of the COM port as defined in the chip's R0 register.

2. DLAB is bit 7 of the UART_LCR register.

3. This register is intended to be read only during normal operation and written during production testing.

IV - FUNCTIONNAL DESCRIPTION (continued)

Table 2

Line Baud Rate	NBAUD Frequency	UART Clock = 1.8432MHz	UART Clock = 3.072MHz	UART Clock = 8.00MHz (Note 1)
50	800	2304	3840	10000
75	1200	1536	2560	6667
110	1760	1047	1745	4545
134.5	2152	857	1428	3717
150	2400	768	1280	3333
300	4800	384	640	1667
600	9600	192	320	833
1200	19200	96	160	417
1800	28800	64	107	278
2000	32000	58	96	250
2400	38400	48	80	208
3600	57600	32	53	139
4800	76800	24	40	104
7200	115200	16	27	69
9600	153600	12	20	52
19200	307200	6	10	26
38400	614400	3	5	13
56000	896000	2	** (Note 2)	9
115200	1843200	1	**	**
128000	2048000	**	**	4
256000	4096000	**	**	2

Notes : 1. In this column, most theoretical divisors are decimal numbers. They have been rounded to the nearest integer.
2. ** = No suitable divisor.

IV.4 - I^2C LINE INTERFACE

IV.4.1 - Introduction

An I^2C line has two wires : the SDA wire carries serial data, the SCL wire carries the clock. It is used for a wide range of applications, including some EEPROMs. It allows several master and slave devices to exchange data while efficiently managing access conflicts. Each device present on the bus has a unique address. Data transfers, whatever their direction is, are always initialized by a master. The slave may slow down the clock if it finds it is too fast.

It is a simplified version of this line which is incorporated in the circuit. It doesn't manage accesses conflicts between several masters. In fact, the ST7548 will always be the only master on the line. The EEPROM is the slave. This is quite enough for the application area. The I^2C line is managed by a state machine clocked by the internal oscillator clock. The EEPROM must be wired at address 0. The recommended model is a ST24C02A or compatible.

IV.4.2 - State Machine Behaviour

The line is managed by a state machine. After a hard or soft reset, the state machine will try and read an EEPROM using the "Sequential Random Read" protocol. If it doesn't get any answer, there is no EEPROM, and it stops.

The PC may also ask the ST7548 to copy in the EEPROM data that have previously been placed in the RAM. It is a convenient way of working on the CIS. This operation is launched by writing a '1' in CONTROLPC register bit 7 (VALWREEPROM). The state machine puts this bit back to '0' when the dump is finished. The state machine uses the "Byte Write" protocol to transfer the data to the EEPROM.

IV - FUNCTIONNAL DESCRIPTION (continued)

IV.4.3 - Sequential Random Read Protocol

The state machine sends the device address (the EEPROM address on the I^2C line), followed by the first byte address (an address inside the EEPROM). Then, it sends again the device address and reads the first byte, then the second, and so on, without sending any address again. The EEPROM internally performs address incrementing. When the state machine wants to stop reading, it doesn't acknowledge the last received byte and sends a STOP condition on the line (see Figure 4).

IV.4.4 - Byte Write Protocol

The state machine performs a complete write cycle for each byte, (sends the device address, the byte address, and the byte to write) and repeats this operation as long as there is something to write. The EEPROM may take some time to physically write the data, and hence, not be ready when the next data comes. In this case, it answers no_acknowledge after it has received the device address. The state machine makes a polling on this signal (sends the device address until there is an acknowledge) to ensure that every byte will be written (see Figure 5).

The above sequence is repeated for each byte.

IV.5 - BUS ARBITRATION

This block manages access conflicts which can occur during accesses requiring use of the internal bus. Its function is to register access requests, allow accesses and put in a wait state those that can't be satisfied immediately by sending them wait signals. It is controlled by a state machine which operates with the internal oscillator clock.

Between the MCU and the PCMCIA, if requests are sent at high speed, the access priority is switched after each access to prevent one of them from always taking the bus. When the I^2C line requires access, it has absolute priority : when the CIS is being read or dumped, no bus access is possible for the MCU and the PCMCIA.

Each access to any register or RAM by a MOTOROLA like MCU automatically produces a DTACK like wait signal on the MCU_ACKWAIT pin, even if no bus arbitration took place.

Figure 4

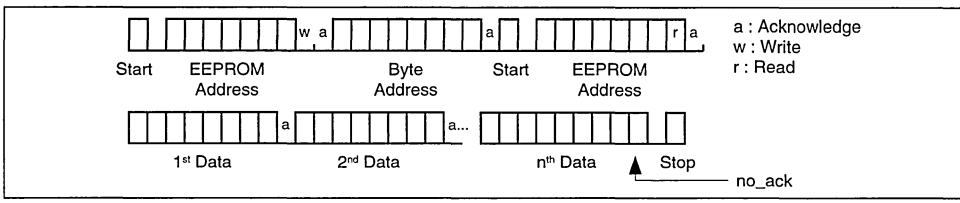
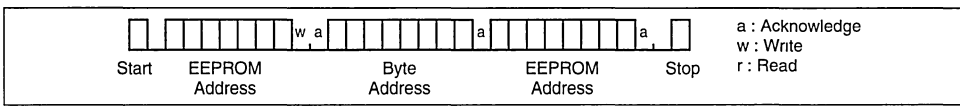


Figure 5



IV - FUNCTIONNAL DESCRIPTION (continued)

IV.6 - REGISTERS

IV.6.1 - Control PC (8 bits, address x"1EE", R/W)

This register is only accessible from the PCMCIA side. Neither the MCU nor the I^2C line can reach it. After a hard or soft reset, the register has all bits at 0.

Bit	Name	Action
7	VALWREEPROM	'1' = initiate a dump of the RAM in the EEPROM (automatically returns to '0' when the dump is done)
6	UART TEST BIT	Must be left at '0'
5	I^2C ESCAPE BIT	Must be left at '0'
4	Not Used	
3	Not Used	
2	Not Used	
1	EIOMEM	Extend I/O Memory Address Space
0	MASK_IT_MCU	at '1', masks the interrupt coming from the MCU

Bit 7 (VALWREEPROM) set at '1' indicates that it is desired to dump a CIS previously written in memory at addresses x"000" to x"0FF" into the EEPROM. This bit is switched back to '0' when the dump is done.

Bit 1 (EIOMEM) : when it is '0' (default value), valid RAM addresses in I/O mode start at x"100" : addresses smaller than x"100" cannot be reached. When set at '1', I/O memory addresses for the RAM start at x"000".

Bit 0 (MASK_IT_MCU) when set at '1' masks the interrupt coming from the MCU.

Bits 5 and 6 (I^2C ESCAPE BIT and UART TEST BIT) are kept for test purposes. After a hard or soft reset, their value is '0'. The user must leave them at '0', otherwise the chip's behaviour would not be in accordance with the specification.

IV.6.2 - Control MCU (8 bits, address x"1EE", R/W)

This register is only accessible from the MCU side. Neither the PCMCIA nor the I^2C line can reach it. After a hard or soft reset, the register has all bits at '0'.

Bit	Name	Action
7	Not Used	
6	Not Used	
5	Not Used	
4	Not Used	
3	Not Used	
2	Not Used	
1	Not Used	
0	MASK_IT_PC	At '1' masks the interrupt coming from the PC

IV.6.3 - Configuration_status (8 bits, address x"1EF")

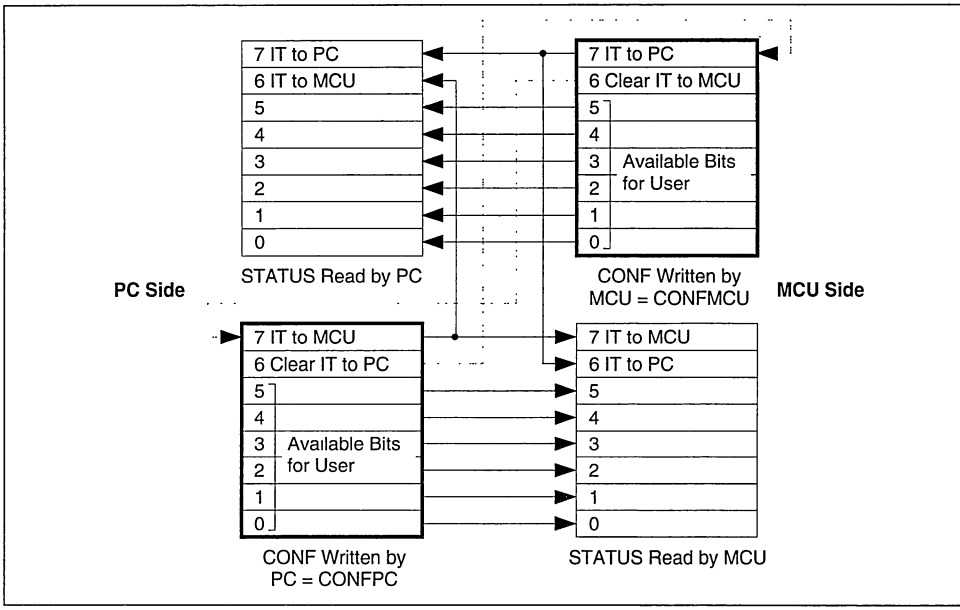
This is a couple of registers which is provided to synchronize data transfer between the PC and the MCU.

Only the configuration registers drawn with bold outline actually exist. The status registers are in fact only the outputs (with a proper wiring) of the configuration registers. Bits 6 and 7 of these registers are active high. (the interrupt is present when a '1' is written on bit 7). Clearing the interrupt which is in bit 7 of one of the CONF registers is done by writing a '1' in bit 6 of the other register. For instance, clearing bit 7 of CONFPC is done by MCU writing a '1' in bit 6 of CONFMCU. It is not necessary to put back bit 6 to '0' after this operation. Erasing the interrupt by writing a '1' in bit 6 will work even if there was already a '1' in this bit, because it is just the fact of writing a '1' which operates, not the fact of having a pulse or an edge on this bit.

The bit range named "available bits for user" can be used freely. It can be used for example to transfer a code telling how many words are to be found, how many transfers there will be, or anything else (see Figure 6).

IV - FUNCTIONNAL DESCRIPTION (continued)

Figure 6



IV.6.4 - R0 (8 bits, address x"1F0", R/W)

This register, accessible by PC and MCU, is initialized by the I^2C channel if an EEPROM is present ; it is a PCMCIA configuration register. It is mainly used to chose the operating mode of the ST7548, seen from the PC side : use with or without an MCU, in I/O or memory, with or without an UART, UART address, interrupts style...

Bit	Name	Action
7	SRESET	Soft reset by PCMCIA active high
6	INTL	Interrupts style (towards PC) : '0' = pulse of at least 5µs, '1' = level
5	UE	Uart Enable : when '1', allows UART use at I/O addresses defined by SEL0 and SEL1
4	Not Used	
3	MODE1	ST7548 operating mode
2	MODE0	ST7548 operating mode
1	SEL1	UART (communication port) selection code
0	SEL0	UART (communication port) selection code

ST7548 operating mode (see also paragraph IV.11 "ADDRESSING CAPABILITIES TABLE") :

MODE1	MODE0	ST7548 Operating Mode
'0'	'0'	Used with an MCU. Memory addressed in common memory
'0'	'1'	Used as memory extension (no MCU)
'1'	'0'	Used as an I/O port (no MCU)
'1'	'1'	Used with a MCU. Memory addressed in I/O mode, allowing interrupts to be sent to the PC.

Communication port selection code :

SEL0	SEL1	Communication Port	Address
'0'	'0'	com1	x"3F8"
'0'	'1'	com2	x"2F8"
'1'	'0'	com3	x"3E8"
'1'	'1'	com4	x"2E8"

During a hard or soft reset (PC_RESET port or SRSET bit at '1'), R0 is reset at '0' except its bit 7 (SRESET) which doesn't turns itself back to'0' when it has been set at '1' : the PC has to turn it back to '0' after a soft reset. Apart from this, for what regards the chip's behaviour, the soft reset has the same action as the hard reset. The circuit waits until the soft or hard reset is finished to start reading the EEPROM.

IV - FUNCTIONNAL DESCRIPTION (continued)

IV.6.5 - R1 (8 bits, address x"1F2", R/W)

This register, accessible by PC and MCU, is initialized by the I^2C channel ; it is a PCMCIA configuration register. It contains all '0' after a hard or soft reset.

Bit	Name	Action
7	Not Used	Leave at '0'
6	Not Used	Leave at '0'
5	Not Used	Leave at '0'
4	RINGEN	Ring Enable : when '1', connects UART_RI to PC_BVD1, otherwise leaves PC_BVD1 at '1'
3	AUDIO	Audio enable : when '1', connects SPKRIN to PC_BVD2, otherwise leaves PC_BVD2 at '1'
2	PWRDWN	Power down active high
1	Not Used	Leave at '0'
0	Not Used	Leave at '0'

During powerdown (when bit PWRDWN is '1'), the circuit prevents from accessing the UART, stops the clock dividers, and doesn't allow I/O and common memory accesses. It only allows attribute memory accesses.

IV.6.6 - ADRDEC (8 bits, address x"1F4", R/W)

This register, accessible by PC and MCU, is initialized by the I^2C channel ; it is a configuration register. It contains all '0' after a hard or soft reset. It is one of the two registers that manage accesses to the I/O port. It defines the base address that the ST7548 will recognize for the I/O port.

Bit	Name	Action
7	A9	I/O port address
6	A8	I/O port address
5	A7	I/O port address
4	A6	I/O port address
3	A5	I/O port address
2	A4	I/O port address
1	A3	I/O port address
0	A2	I/O port address

The I/O port address is decoded by comparing the content of this register with the bits PC_ADD[9..2] on the PC address bus.

Bits 1 and 0 of the address are ignored, so that the decoded address field width is at least 4 bytes. Moreover, depending upon the MASK register content, additional bits in the PC address bus may be ignored, thus making the decoded address range larger. The number of additional bits ignored is given in the MASK register. There may be 0 to 4 additional address bits ignored (PC_ADD[2] to PC_ADD[5]).

IV.6.7 - MASK (8 bits, address x"1F6", R/W)

This register, accessible by PC and MCU, is initialized by the I^2C channel ; it is a configuration register. Its content is all '0' after a hard or soft reset. It is the second register which manages accesses to the I/O port. It has an action on the decoded address field width.

Bit	Name	Action
7	Not Used	
6	Not Used	
5	Not Used	
4	Not Used	
3	Not Used	
2	W2	Decoded address field width code
1	W1	
0	W0	

Address field width code table :

W2	W1	W0	Action	Decoded I/O Address Field Width
'0'	'0'	'0'	PC_ADD[2..5] not masked	4 bytes corresponding to PC_ADD[0. 1]
'0'	'0'	'1'	PC_ADD[2] masked PC_ADD[3..5] not masked	8 bytes corresponding to PC_ADD[0. 2]
'0'	'1'	'0'	PC_ADD[2..3] masked PC_ADD[4..5] not masked	16 bytes corresponding to PC_ADD[0..3]
'0'	'1'	'1'	PC_ADD[2..4] masked PC_ADD[5] not masked	32 bytes corresponding to PC_ADD[0..4]
'1'	'0'	'0'	PC_ADD[2..5] masked	64 bytes corresponding to PC_ADD[0..5]

IV - FUNCTIONNAL DESCRIPTION (continued)

IV.6.8 - PROGN (8 bits, address x"1F8", R/W)

This register, accessible by PC and MCU, is initialized by the I²C channel ; it is a configuration register. It contains all '0' after a hard or soft reset. It drives the clock dividers which generate the UART clock and the clock output on port CLKOUT.

Bit	Name	Action
7	NOT_HALF_CLK	Frequency choice for CLKOUT in normal operation : '0' : CLKOUT frequency is half the one on XTIN port. '1' : CLKOUT frequency is the same as the one on XTIN port. This bit is meaningless in stand-by.
6	MCU_DIV(2)	MCU_DIV division ratio code during stand-by for CLKOUT
5	MCU_DIV(1)	
4	MCU_DIV(0)	
3	UART_CLK	Clock input choice for UART_DIV which generates the UART clock
2	UART_DIV(2)	UART_DIV division ratio code for the UART clock
1	UART_DIV(1)	
0	UART_DIV(0)	

- Bit 3 : input clock choice for UART_DIV :
  - '0' → internal oscillator clock (XTIN port).
  - '1' → external clock input port CLKIN.
- Code giving UART_DIV division ratio : report to tables below.

CLKOUT port stand-by division ratio table :

Bit 6	Bit 5	Bit 4	Stand-by Division Ratio
'0'	'0'	'0'	2
'0'	'0'	'1'	4
'0'	'1'	'0'	8
'0'	'1'	'1'	16
'1'	'0'	'0'	32
'1'	'0'	'1'	64
'1'	'1'	'0'	128
'1'	'1'	'1'	256

UART clock division ratio table :

Bit 2	Bit 1	Bit 0	UART Clock Division Ratio	Example : UART Divider Input Clock giving 1.8432MHz on the UART
'0'	'0'	'0'	2	3.6864MHz
'0'	'0'	'1'	4	7.3728MHz
'0'	'1'	'0'	8	14.7456MHz
'0'	'1'	'1'	10	18.432MHz
'1'	'0'	'0'	12	22.1184MHz
'1'	'0'	'1'	16	29.4912MHz
'1'	'1'	'0'	18	33.1776MHz
'1'	'1'	'1'	20	36.864MHz

IV.7 - RAM

The RAM is a 494 bytes memory. It is used to store the CIS and to exchange data between the PCMCIA bus and the MCU bus. The CIS takes only a part of the memory, so that it is possible to keep it visible in the memory while performing data transfer through the RAM. Nevertheless, if a large amount of memory is need for these data transfers, and if the CIS is no longer necessary after it has been read, it is possible to use the CIS area in the RAM to exchange the data. The correspondence between addresses seen by the PC, those seen by the MCU and those seen by the I²C interface is detailed in a separate paragraph later.

IV.8 - I/O - MCU - MEMORY EXTENSION MULTI-PURPOSE PORT

IV.8.1 - Introduction

The same pins are used to connect either a peripheral, a memory extension or a MCU. This corresponds to different behaviours for the chip. Choosing one configuration must be done depending upon how the chip will be used. It is obviously not possible to switch in real time from one behaviour to another since it would mean that the chip environment changes at the same time. The choice is done after the reset owing to R0 register's content.
The multi-purpose port has 8 pins for data, 9 for the addresses and a few other pins for control signals.

IV - FUNCTIONNAL DESCRIPTION (continued)

IV.8.2 - I/O port

The I/O port is an 8 bits parallel port that the PC may access. It uses the pins MCU_DAT[7..0] to transfer data. The nine address pins are useless and they must be tied to either '0' or '1' to avoid power consumption. The chip generates a chip-select on CSL_ALE and reproduces on IOW and IOR outputs the PC_IOWR and PC_IORD signals coming from the PC when the I/O port address is decoded. The I/O port address is programmable owing to registers ADRDEC and MASK.

IV.8.3 - MCU port

The MCU port allows a parallel 8 bits connection between a MCU and the PC through the ST7548. The MCU may read and write in the RAM and in some registers. The MCU port either works with separate data and address buses, or with a multiplexed address/data bus. The ST7548 automatically detects if the bus is multiplexed. In the multiplexed mode, since the address on the MCU side is on 9 bits, the 8 LSBs of the address are multiplexed with the data and the MSB is carried on the address bus at its normal location.

In addition to the fact of working with a multiplexed or non multiplexed MCU bus, for maximum flexibility, the ST7548 also accepts two styles of control signals for the MCU. One is called "Motorola-like" and the other "Intel-like". Motorola-like style is chosen by wiring the MCU_MOTEL pin to '1', Intel-like style by wiring it to '0'.

- The "Motorola-like" style has the following characteristics :
  - MCU_DSRD pin is interpreted as a data strobe active low.
  - MCU_RWWR pin is interpreted as a level active signal indicating "read" when'1' and "write" when '0'.
  - MCU_ACKWAIT is interpreted as a "dtack" signal which goes low to indicate that the MCU can terminate its memory cycle. The ST7548 always issues a DTACK on MCU_ACKWAIT since it is mandatory for the MCU to achieve its memory cycle.
- The "Intel-like" style has the following characteristics :
  - MCU_DSRD pin is interpreted as a read signal active low.
  - MCU_RWWR pin is interpreted as a write signal active low.
  - MCU_ACKWAIT is interpreted as a "wait" signal which is maintained low by the ST7548 as long as it wants the MCU to wait during its memory cycle. If it doesn't need any cycle extension, the ST7548 will not issue a wait on MCU_ACKWAIT.

IV.8.4 - Memory Extension

Used in the memory extension mode, the ST7548 just extends the 8 bits data bus PC_DAT, and reproduces the read/write signals on its outputs. When the circuit is placed in memory extension mode, the following things occur :

- PC_CE1 is reproduced on pin CSL_ALE (only for common memory accesses whith PC_REG = '1').
- PC_WE is reproduced on pin IOW if there is a common memory write on the chip.
- PC_OE is reproduced on pin IOR if there is a common memory read on the chip.
- PC_DAT* and MCU_DAT* are connected together according to IOW and IOR signals.

The addresses are not transmitted by the circuit : they have to be handled outside the chip.

IV - FUNCTIONNAL DESCRIPTION (continued)

IV.9 - ADDRESSES CORRESPONDENCE

IV.9.1 - Addresses Correspondence in Attribute Memory Mode (Figure 7)

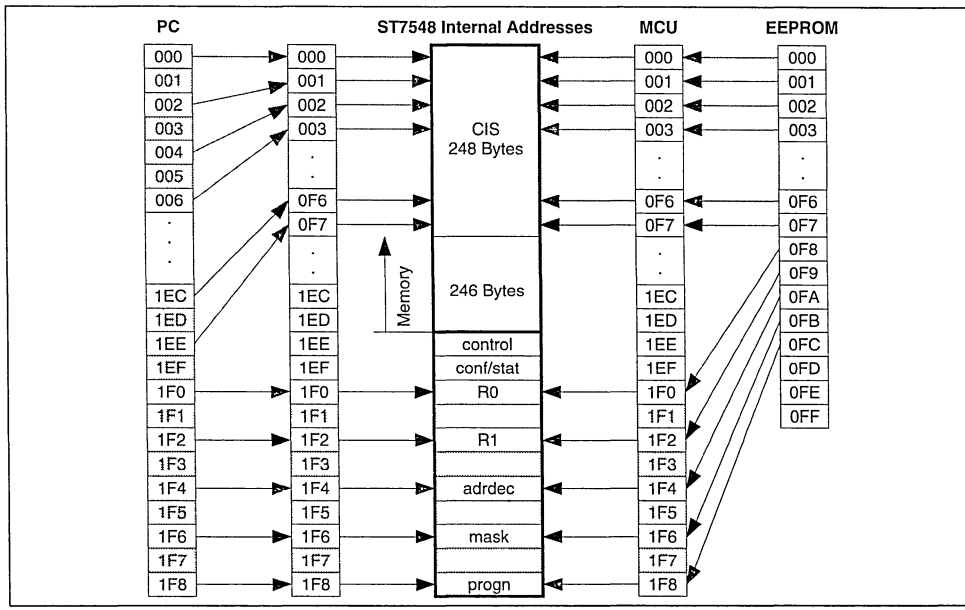
The attribute memory is accessible on the PCMCIA side when PC_CE1 = '0', PC_REG = '0', and with the read/write signals PC_OE et PC_WE. In attribute memory, only even addresses are allowed. One address out of two is thus used. In order to avoid wasting room in the chip's RAM, and to allow the user to keep the CIS in memory while having enough room to perform exchanges between the PCMCIA bus and the MCU, the CIS is "compressed" at the beginning of the RAM. To achieve this, attribute memory addresses seen on the PCMCIA bus are divided by two (shifted one bit right) internally when they are comprised between x"000" and x"1EE". Higher addresses (which correspond to registers) are transmitted without any modification.

When the CIS is loaded in memory by the MCU, since the MCU has total freedom for its addressing, it uses the addresses directly seen by the RAM, between x"00" and x"F7".

When the CIS and the registers are loaded from the EEPROM, it is the opposite operation of that which is performed for the PCMCIA bus. The addresses from x"00" to x"F7" of the EEPROM are copied in the RAM memory from x"00" to x"F7". Then, the following addresses correspond to registers and they are shifted one bit left so that they fall in the registers.

When the chip is used on a true PCMCIA board, the user should put x"00" in the EEPROM at addresses x"F8" and x"F9", because they correspond to registers R0 and R1 which are usually loaded by the PCMCIA bus after the CIS has been loaded. When the chip is used directly with a PC, the user can put directly at these locations, the information he wants to have in R0 and R1.

Figure 7



IV - FUNCTIONNAL DESCRIPTION (continued)

IV.9.2 - Addresses Correspondence in Common Memory (Figure 8)

Common memory is accessible on the PCMCIA side when PC_CE1 = '0', PC_REG = '1', and with the read/write signals PC_OE and PC_WE. In common memory, on the PCMCIA side, even and odd addresses are allowed, and the addresses inside the chip are the same as those transmitted on PC_ADD and MCU_ADD address buses.

Possible addresses on PC_ADD range from x"000" to x"1EF". They correspond to the RAM and to the first two registers: CONTROLPC and CONF/STATUS.

The circuit RAM memory extends from address x"000" to address x"1ED" : it overlaps the CIS area. It is up to the user to destroy or not to destroy the CIS when he uses the memory.

IV.9.3 - Address Correspondence in I/O Memory Mode (Figure 9)

I/O accesses on the PCMCIA side are characterized by PC_CE1 = '0', PC_REG = '0' and the use of PC_IORD and PC_IOWR as read/write signals. I/O addresses start at x"100" and extend to x"1EF". They correspond to the second half of the memory and to the first two registers: CONTROLPC and CONF/STATUS which are preferably used to synchronize exchanges between PC and MCU. The internal addresses exactly correspond to those that are sent by the PC and the MCU.

When the ST7548 RAM is used in I/O memory mode, the circuit filters addresses on the PC side which are outside the range x"100" to x"1EF", except those which are for the UART. This filter is deactivated when the I/O port is used because in this case, the internal memory is not used.

On the MCU side, no filtering is done on accesses : it is up to the user to care.

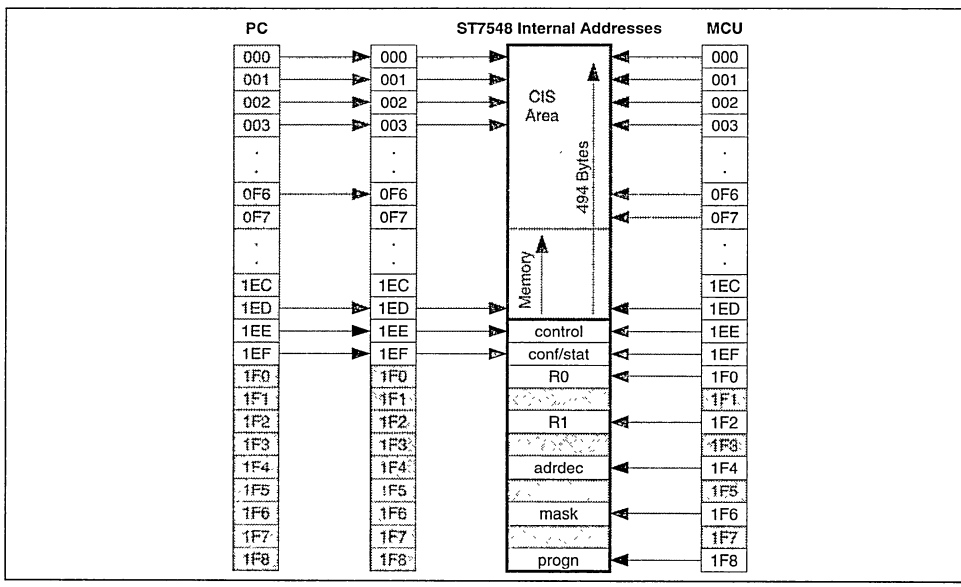
IV.9.4 - How to Dump a CIS in the EEPROM (Figure 10)

The circuit has been provided with a facility to program the EEPROM without the use of an external programming tool : it is possible to write a CIS in common memory mode into the RAM and then to transfer it in the EEPROM automatically. The transfer is initiated just by writing a '1' on bit 7 of CONTROLPC register.

The ST7548 writes the first 256 addresses of its internal RAM in the corresponding addresses in the EEPROM. So, the CIS to dump must have previously been placed in common memory at addresses x"000" to x"0FF".

During the dump in the EEPROM, the signal PC_RDY shows "busy" ('0').

Figure 8



IV - FUNCTIONNAL DESCRIPTION (continued)

Figure 9

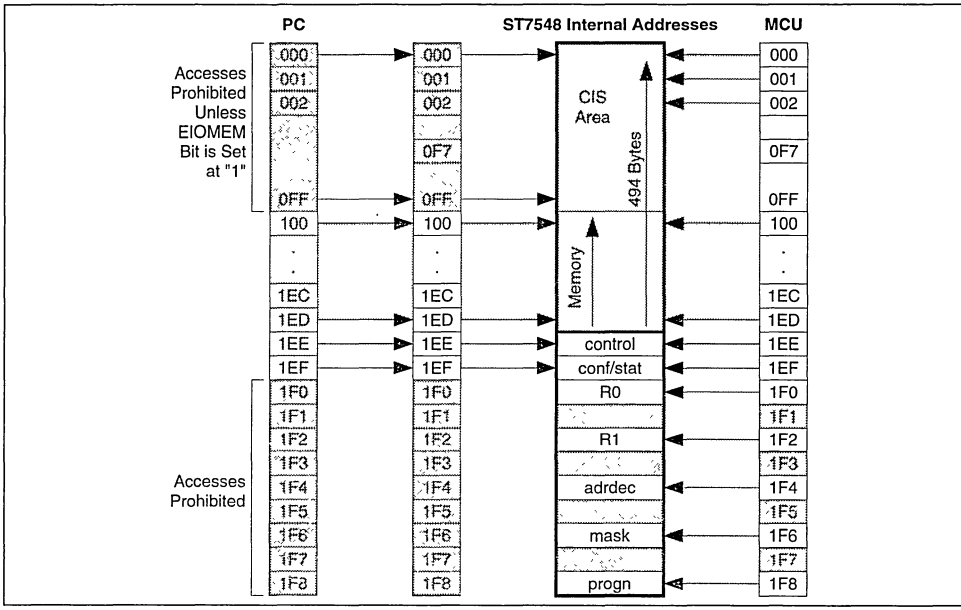
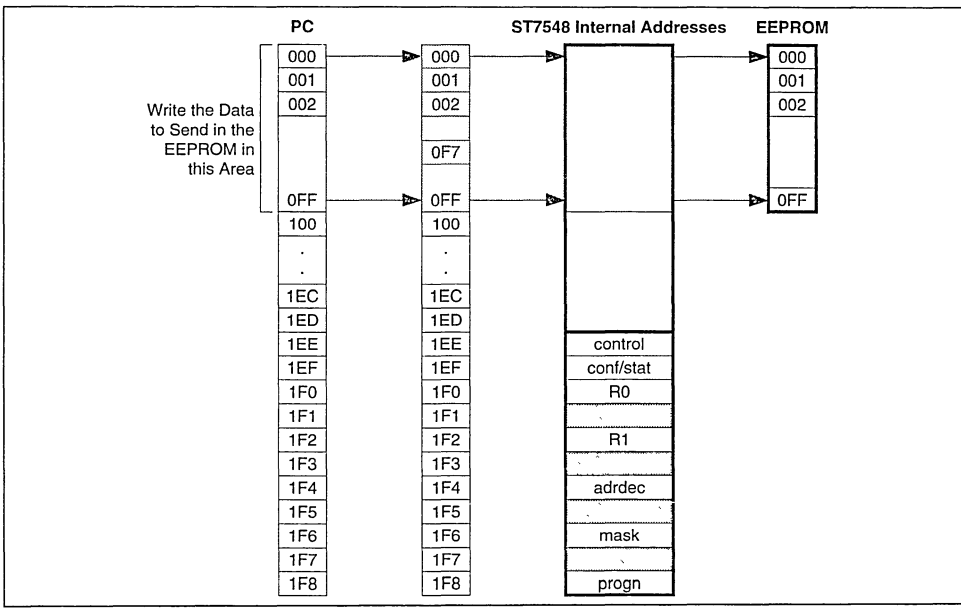


Figure 10



IV - FUNCTIONNAL DESCRIPTION (continued)

IV.10 - INTERRUPTS

IV.10.1 - Interrupts Towards the PC

Interrupts Level

Interrupts towards the PC are active when there is a '0' on the PC_RDY port. INTL bit in register R0 makes it possible to choose between an interrupt active on a level (as long as the interrupt is present, PC_RDY remains at '0') and a pulse interrupt (when the interrupt happens, PC_RDY goes low for at least 5 micro-seconds, and then goes back to '1', independently of the fact that the interrupt has been acquitted or not).

INTL = '0' ⇀ pulse
INTL = '1' ⇀ level

The PC can only receive interrupts in the modes where I/O accesses are enabled.

Interrupts Origin

Interrupts towards the PC have three possible origins :

- The UART : the UART emits an interrupt when its INTR output is '1'. In order to have this interrupt transmitted to the PC, it is necessary to have the UART validated (bit UE in R0 register at '1') and that the UART output OUT2 be at '0'. Refer to data sheets of 16C550 UARTS to have a detailed description on UART interrupts.
- The I/O port : in this case, interrupts come from a peripheral device. The peripheral sends an interrupt by putting a '0' on MCU_IRQ port. This interrupt is transmitted to the PC when the I/O port is enabled (bit MODE1 at '1' and bit MODE0 at '0' in R0 register). Conditions upon which interrupts appear or disappear on this pin depend upon what is connected on the port.
- The MCU : the ST7548 RAM must be placed in the I/O field of the PC in order to have interrupts enabled (bits MODE1 and MODE0 in register R0 at '1'). In this mode, the RAM is used to exchange data between the PC and a MCU, and interrupts may be used to manage this transfer. The MCU sends an interrupt to the PC by writing a '1' on bit 7 in CONFMCU register. This interrupt reaches the PC if the PC has not masked it (the interrupt is masked with a '1' on bit 0 in CONTROLPC register). To acknowledge this interrupt and make it disappear, the PC must write a '1' on bit 6 in its CONFPC register.

IV.10.2 - Interrupts Towards the MCU

Only the PC may send interrupts to the MCU. The PC sends an interrupt to the MCU by writing a '1' on bit 7 in CONFPC register. The MCU may mask this interrupt by writing a '1' on bit 0 in its CONTROLMCU register. To acknowledge the interrupt and make it disappear, the MCU must write a '1' on bit 6 in its CONFMCU register.

Interrupts operation is exactly symmetrical for the PC and the MCU.

IV - FUNCTIONNAL DESCRIPTION (continued)

IV.11 - ADDRESSING CAPABILITIES TABLE

	Hexa-decimal Address	PCMCIA Addressing Mode				MCU		I^2C	R0 Content		
		common memory pc_ce1=0 pc_reg=1 pc_we pc_oe	attribute memory pc_ce1=0 pc_reg=0 pc_we pc_oe	I/O memory pc_ce1=0 pc_reg=0 pc_iord pc_iowr	Wait	Access	Wait		UE	MODE 1	MODE 0
Memory	0→1ED	yes	no	no	yes	yes	yes	yes	'X'	'0'	'0'
	0→1EE	no	yes						'X'	'X'	'X'
	100(1)→1ED		no	yes					'X'	'1'	'1'
control PC	1EE	yes	no	no	no	no		no	'X'	'0'	'0'
		no		yes					'X'	'1'	'1'
control MCU				no		yes	no		'X'	'X'	'X'
confPC = statMcu	1EF	write			yes	read	yes		'X'	'0'	'0'
		no		write					'X'	'1'	'1'
confMcu = statPC		read		no		write			'X'	'0'	'0'
				read					'X'	'1'	'1'
R0	1F0	no	yes	no		yes		yes	'X'	'X'	'X'
R1	1F2										
Adrdec	1F4										
Mask	1F6										
Progn	1F8										
UART	2E8 2F8 3E8 3F8	no	no	yes	no	no		no	'1'	'X'	'X'
I/O port	000→3FF	no	no	yes	no	no		no	'X'	'1'	'0'
Mem ext	XXX	yes	no	no	no	no		no	'X'	'0'	'1'

Note : 1. The lowest address in I/O memory mode can be reduced to 000 if EIOMEM bit is set to "1" in CONTROLPC.

This table describes the access capabilities for all the circuit, i.e. for the memory, registers, UART, I/O port, and memory extension port. The CONTROLPC and CONTROLMCU registers are seen at the same address on the PC side and on the MCU side, but in fact they are two different registers, and the PC, for example only sees CONTROLPC. The circuit distinguishes them from where the access comes from. It is the same thing for CONFMCU and CONFPC. In addition, the configuration/status registers are actually "configuration" when they are written and "status" when they are read. Their access permission when they are status are written in bold italic. Their access permission when they are configuration are written in regular characters.

Remark about wait : when the MCU is a Motorola or equivalent, a wait (or more precisely a DTACK) is systematically generated, even for an access to the CONTROLMCU register. This is mandatory to allow the MCU to terminate its memory cycle. In this case, the wait duration is as short as possible.

V - ABSOLUTE MAXIMUM RATINGS AND OPERATING VALUES

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5, 6.0	V
V_I	Digital Input Voltage	-0.5, V_{DD} + 0.5	V
I_o	Digital Output Current	4	mA
T_A	Operating Temperature	0, 70	°C
T_{STG}	Storage Temperature	-40, +125	°C
PDmax	Maximum Power Dissipation	100	mW
T_L	Lead Temperature (Soldering, 10s)	+300	°C

VI - DIGITAL INTERFACE (V_{DD} = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{il}	Input Low Voltage	All digital inputs			0.8	V
V_{ih}	Input High Voltage	All digital inputs	2.2			V
V_{ol}	Output Low Voltage	I_L = 4mA			0.4	V
V_{oh}	Output High Voltage	I_L = 4mA	2.4			V
I_{il}	Input Low Current	Any digital input, Gnd < V_{in} < V_{il}			10	µA
I_{ih}	Input High Current	Any digital input, V_{ih} < V_{in} < V_{il}			10	µA
I_{OZ}	Output Current in High Impedance	All digital tri-state I/Os without internal pull-up or pull-down resistor			10	µA

Never let any unused input not connected. This could cause excessive power dissipation and may damage the component. Unused inputs must be connected either to '0' or '1', unless otherwise specified in the documentation.

VII - CLOCK FREQUENCY (V_{DD} = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CLKIN	CLKIN Max Frequency				36.864	MHz
XTIN	XTIN Max Frequency				36.864	MHz

VIII - POWER CONSUMPTION AND SUPPLY VOLTAGE (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	DC Supply Voltage		4.5	5	5.5	V
I_{CC}	DC Current			20		mA

IX - TIMING CHARACTERISTICS

IX.1 - PCMCIA Bus Timing (Common Memory Cycle)

***Read Timing** (see Figure 11)*

Symbol	IEEE	Parameter	Min.	Typ.	Max.	Unit
tdis(OE)	t_{GHQZ}	Output Disable Time from OE			50	ns
tsu(A)	t_{AVGL}	Address Setup Time	10			ns
th(A)	t_{GHAX}	Address Hold Time	15			ns
tsu(CE)	t_{ELGL}	Card Enable Setup Time	0			ns
th(CE)	t_{GHEH}	Card Enable Hold Time	15			ns
tv(WT-OE)	t_{GLWTV}	Wait Valid from OE			35	ns
tw(WT)	t_{WTLWTH}	Wait Pulse Width			12	µs
tv(WT)	t_{QVWTH}	Data Setup for Wait Released	0			ns

***Write Timing** (see Figure 12)*

Symbol	IEEE	Parameter	Min.	Typ.	Max.	Unit
tsu(A)	t_{AVWL}	Address Setup Time	10			ns
tsu(D-WEH)	t_{DVWH}	Data Setup Time for WE	40			ns
th(D)	t_{WMDX}	Data Hold Time	15			ns
trec(WE)	t_{WMAX}	Write Recover Time	15			ns
tsu(CE)	t_{ELWL}	Card Enable Setup Time	0			ns
th(CE)	t_{GHEH}	Card Enable Hold Time	15			ns
tv(WT-WE)	t_{WLWTV}	Wait Valid from WE			35	ns
tw(WT)	t_{WTLWTH}	Wait Pulse Width			12	µs
tv(WT)	t_{WTHWH}	WE High from Wait Released	0			ns
tv(D-WE)		Data Valid from WE			40	ns

IX.2 - PCMCIA Bus Timing (Attribute Memory Cycle)

***Read Timing** (see Figure 11)*

Symbol	IEEE	Parameter	Min.	Typ.	Max.	Unit
tdis(OE)	t_{GHQZ}	Output Disable Time from OE			100	ns
tsu(A)	t_{AVGL}	Address Setup Time	30			ns
th(A)	t_{GHAX}	Address Hold Time	20			ns
tsu(CE)	t_{ELGL}	Card Enable Setup Time	0			ns
th(CE)	t_{GHEH}	Card Enable Hold Time	20			ns
tv(WT-OE)	t_{GLWTV}	Wait Valid from OE			35	ns
tw(WT)	t_{WTLWTH}	Wait Pulse Width			12	µs
tv(WT)	t_{QVWTH}	Data Setup for Wait Released	0			ns

***Write Timing** (see Figure 12)*

Symbol	IEEE	Parameter	Min.	Typ.	Max.	Unit
tsu(A)	t_{AVWL}	Address Setup Time	30			ns
tsu(D-WEH)	t_{DVWH}	Data Setup Time for WE	80			ns
th(D)	t_{WMDX}	Data Hold Time	30			ns
trec(WE)	t_{WMAX}	Write Recover Time	30			ns
tsu(CE)	t_{ELWL}	Card Enable Setup Time	0			ns
th(CE)	t_{GHEH}	Card Enable Hold Time	20			ns
tv(WT-WE)	t_{WLWTV}	Wait Valid from WE			35	ns
tw(WT)	t_{WTLWTH}	Wait Pulse Width			12	µs
tv(WT)	t_{WTHWH}	WE High from Wait Released	0			ns
tv(D-WE)		Data Valid from WE			40	ns

IX - TIMING CHARACTERISTICS (continued)

Figure 11 : Read Timing Diagram

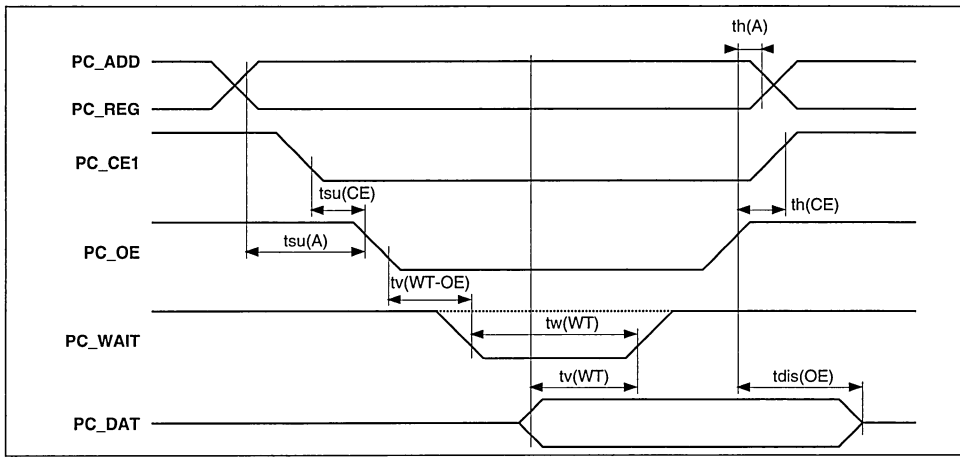
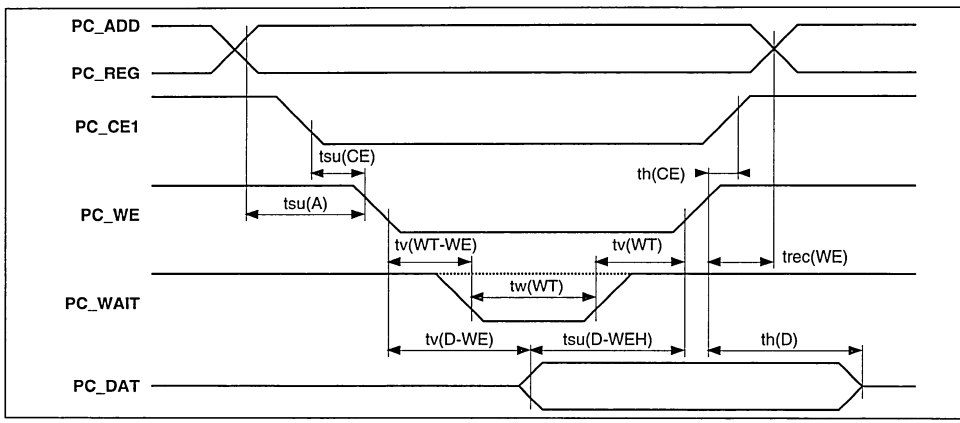
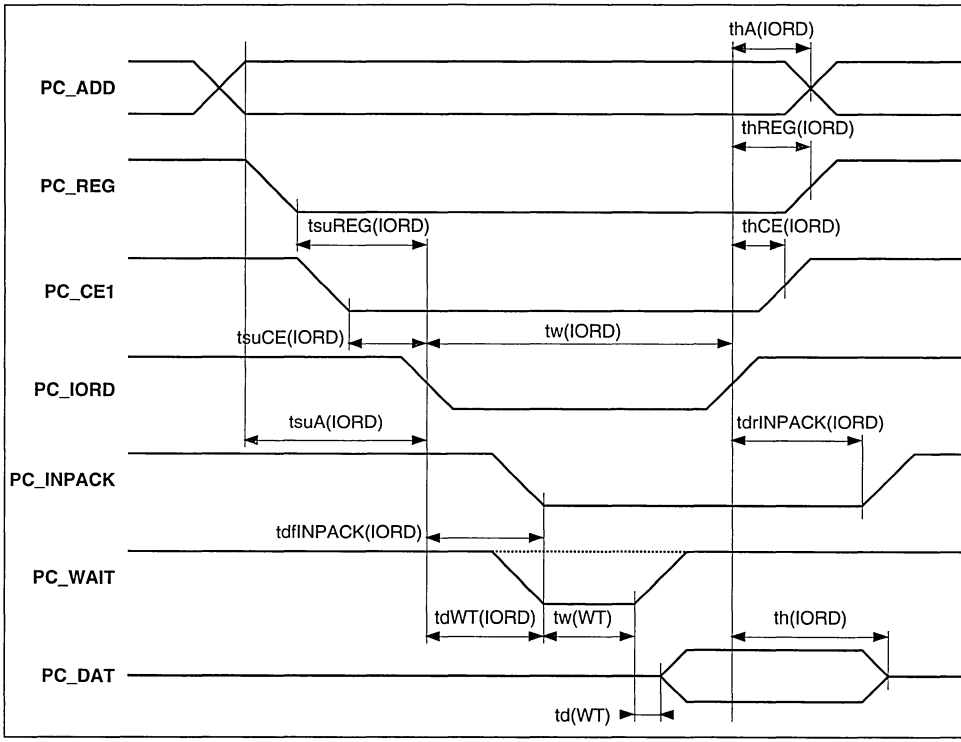


Figure 12 : Write Timing Diagram



IX - TIMING CHARACTERISTICS (continued)
IX.3 - PCMCIA Bus Timing (I/O Cycle)

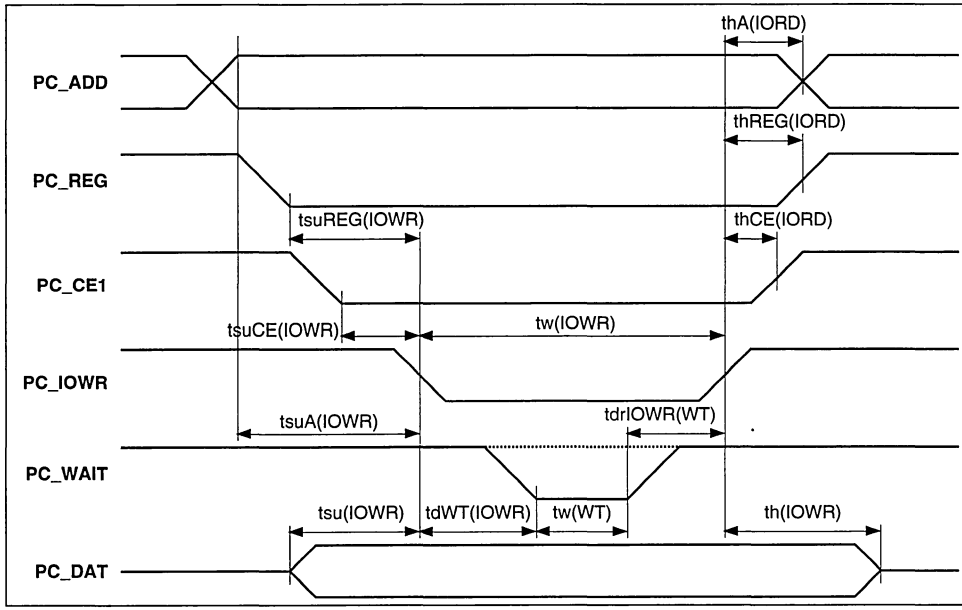
Figure 15 : Read Timing Diagram



Symbol	IEEE	Parameter	Min.	Typ.	Max.	Unit
th(IORD)	t_{IGHQX}	Data Hold following IORD	0			ns
twIORD	t_{IGLIGH}	IORD Width Time	165			ns
tsuA(IORD)	t_{AVIGL}	Address Set-up before IORD	70			ns
tha(IORD)	t_{IGHAX}	Address Hold following IORD	20			ns
tsuCE(IORD)	t_{ELIGL}	CE Set-up before IORD	5			ns
thCE(IORD)	t_{IGHEH}	CE Hold following IORD	20			ns
tsuREG(IORD)	t_{RGLIGL}	REG Setup before IORD	5			ns
thREG(IORD)	t_{IGHRGH}	REG Hold following IORD	0			ns
tdfINPACK(IORD)	t_{IGLIAL}	INPACK Delay Falling from IORD	0		45	ns
tdrINPACK(IORD)	t_{IGHIAH}	INPACK Delay Rising from IORD			45	ns
tdWT(IORD)	t_{IGLWTL}	WAIT Delay Falling from IORD			35	ns
td(WT)	t_{WTHQV}	Data Delay from Wait Rising			35	ns
tw(WT)	t_{WTLWTH}	WAIT Width Time			12	µs

IX - TIMING CHARACTERISTICS (continued)
IX.3 - PCMCIA Bus Timing (I/O Cycle) (contined)

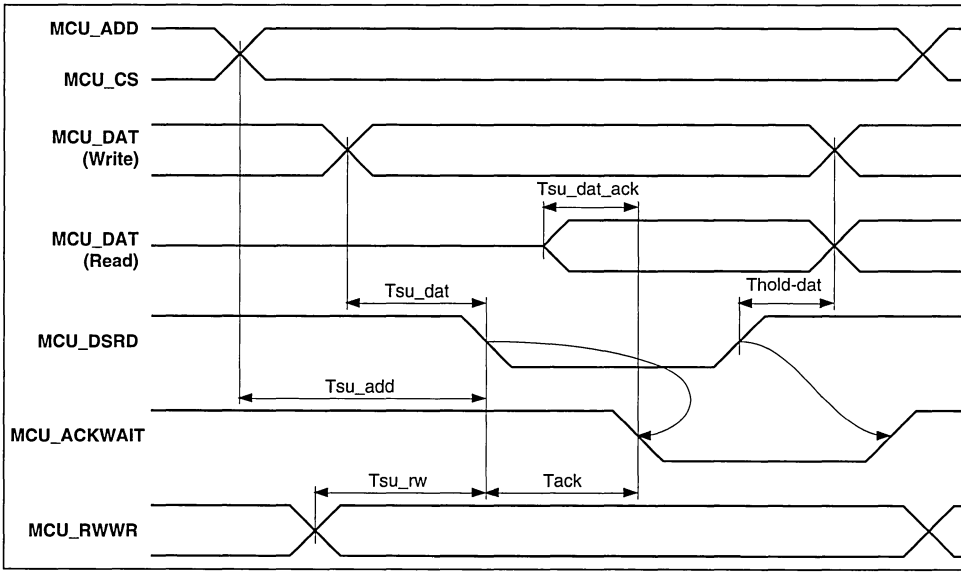
Figure 16 : Write Timing Diagram



Symbol	IEEE	Parameter	Min.	Typ.	Max.	Unit
tsu(IOWR)	t_{DVIWL}	Data Set-up before IOWR	60			ns
th(IOWR)	t_{IWHDX}	Data Hold following IOWR	30			ns
twIOWR	t_{IWLIWH}	IOWR Width Time	165			ns
tsuA(IOWR)	t_{AVIWL}	Address Set-up before IOWR	70			ns
thA(IOWR)	t_{IWHAX}	Address Hold following IOWR	20			ns
tsuCE(IOWR)	t_{ELIWL}	CE Set-up before IOWR	5			ns
thCE(IOWR)	t_{IWHEH}	CE Hold following IOWR	20			ns
tsuREG(IOWR)	t_{RGLIWL}	REG Set-up before IOWR	5			ns
thREG(IOWR)	t_{IWHRGH}	REG Hold following IOWR	0			ns
tdWT(IOWR)	t_{IWLWTL}	WAIT Delay Falling from IOWR			35	ns
tw(WT)	t_{WTLWTH}	WAIT Width Time			12	µs
tdrIOWR(WT)	t_{WTHIWL}	IOWR High from WAIT High	0			ns

IX - TIMING CHARACTERISTICS (continued)
IX.4 - MCU Bus Timing
IX.4.1 - Motorola, Not Multiplexed

Figure 17 : MCU_MOTEL is Tied to '1'



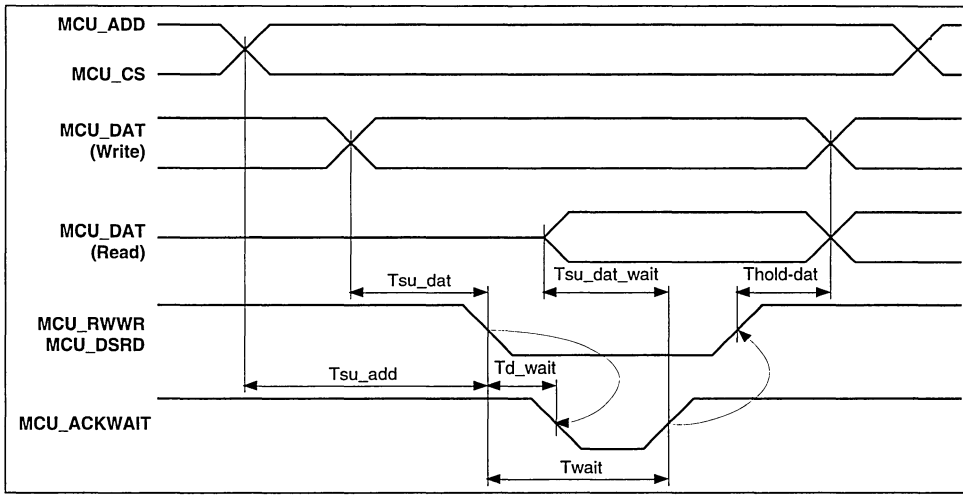
The first edge on MCU_ACKWAIT indicates to the MCU that it can terminate its memory cycle.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Tsu_dat_ack	Data Read Set-up Time	20			ns
Tsu_dat	Data Write Set-up Time	10			ns
Thold_dat	Data Hold Time	0			ns
Tsu_add	Address Set-up Time	20			ns
Tsu_rw	Read/Write Set-up Time	10			ns
Tack	Ack Delay Time			12 (1)	µs

Note : 1. The typical value depends upon chip operating frequency.

IX - TIMING CHARACTERISTICS (continued)
IX.4 - MCU Bus Timing (continued)
IX.4.2 - Intel, Not Multiplexed

Figure 18 : MCU_MOTEL is Tied to '0'



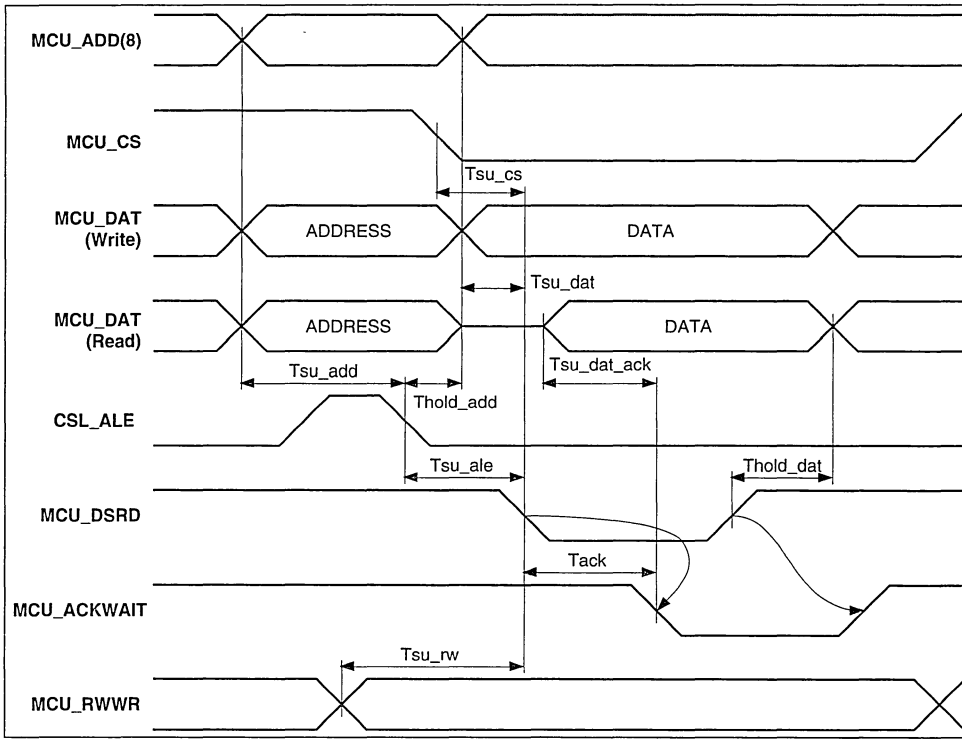
The second edge on MCU_ACKWAIT indicates to the MCU that it may terminate its memory cycle. If the access doesn't require to extend the memory cycle, MCU_ACKWAIT remains at '1'.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Tsu_dat	Data Write Set-up Time	10			ns
Thold_dat	Data Hold Time	0			ns
Tsu_dat_wait	Data Read Set-up Time	20			ns
Tsu_add	Address Set-up Time	20			ns
Td_wait	Wait Delay Time			35	ns
Twait	Wait Width Time			12 (1)	µs

Note : 1. The typical value depends upon chip operating frequency.

IX - TIMING CHARACTERISTICS (continued)
IX.4 - MCU Bus Timing (continued)
IX.4.3 - Motorola, Multiplexed

Figure 19 : MCU_MOTEL is Tied to '1'



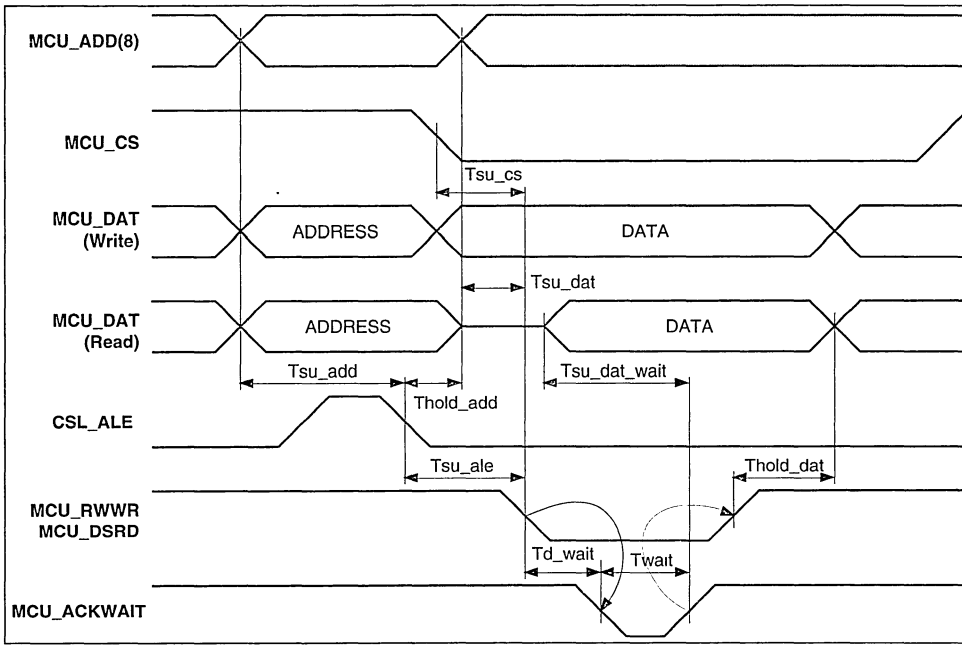
The first edge on MCU_ACKWAIT indicates to the MCU that it can terminate its memory cycle.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Tsu_cs	Chip Select Set-up Time	20			ns
Tsu_dat	Data Write Set-up Time	10			ns
Tsu_add	Address Set-up Time	20			ns
Thold_add	Address Hold Time	10			ns
Tsu_dat_ack	Data Read Setup Time	20			ns
Tsu_ale	Address Latch Enable Set-up Time	20			ns
Thold_dat	Data Hold Time	0			ns
Tsu_rw	Read/write Set-up Time	10			ns
Tack	Ack Delay Time			12 (1)	µs

Note : 1. The typical value depends upon chip operating frequency.

IX - TIMING CHARACTERISTICS (continued)
IX.4 - MCU Bus Timing (continued)
IX.4.4 - Intel, Multiplexed

Figure 20 : MCU_MOTEL is Tied to '0'

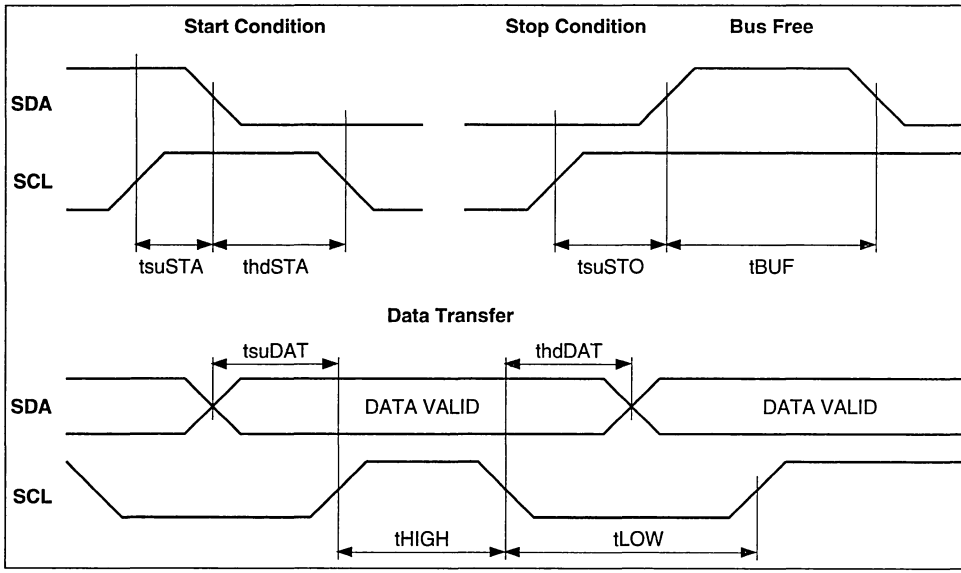


The second edge on MCU_ACKWAIT indicates to the MCU that it may terminate its memory cycle. If the access doesn't require to extend the memory cycle, MCU_ACKWAIT remains at '1'.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Tsu_cs	Chip Select Set-up Time	20			ns
Tsu_dat	Data Write Set-up Time	10			ns
Tsu_add	Address Set-up Time	20			ns
Thold_add	Address Hold Time	10			ns
Tsu_dat_wait	Data Read Set-up Time	20			ns
Tsu_ale	Address Latch Enable Set-up Time	20			ns
Thold_dat	Data Hold Time	0			ns
Td_wait	Wait Delay Time			35	ns
Twait	Wait Width Time			12 (1)	µs

Note : 1. The typical value depends upon chip operating frequency.

IX - TIMING CHARACTERISTICS (continued)
IX.5 - I²C Bus Timing
Figure 21



Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{HIGH}	Clock Pulse Width High	4			µs
t_{LOW}	Clock Pulse Width Low	4.7			µs
tsuSTA	Set-up Time for Start Condition	4.7			µs
thdSTA	Hold Time for Start Condition	4			µs
tsuSTO	Set-up Time for Stop Condition	4.7			µs
t_{BUF}	Time Bus Free before New Transmission	4.7			µs
tsuDAT	Set-up Time for Data	250			ns
thDAT	Hold Time for Data	0			µs

X - APPLICATIONS

X.1 - Introduction

Although it has been designed mainly for telecommunications, the circuit can be used in different ways in a wide range of applications.

For a better understanding of the given examples, we will assume that the following functions are available in the PC or MCU software :

```
PCWMEM(address, data)   /* PC write in common memory mode */
PCRMEM (address)        /* PC read in common memory mode */
PCWATTR (address, data) /* PC write in attribute memory mode */
PCRATTR (address)       /* PC read in attribute memory mode */
PCWIO (address, data)   /* PC write in I/O memory mode */
PCRIO (address)         /* PC read in I/O memory mode */
MCUW (address, data)    /* MCU write */
MCUR (address)          /* MCU read */
```

X.2 - MCU Connection

X.2.1 - Wiring

The following example shows how to connect a Motorola non multiplexed bus on the chip.
Connect :

- MCU_CS on a logic function that decodes an address space dedicated to the ST7548.
- MCU_MOTEL to '1'.
- CSL_ALE to '0'.
- MCU_DAT on MCU data bus.
- MCU_ADD on MCU address bus.
- MCU_RWWR on MCU RW signal.
- MCU_DSRD on MCU data strobe.
- MCU_ACKWAIT on MCU DTACK.
- MCU_IRQ on a MCU interrupt input line.
- IOW and IOR may be left open.

X.2.2 - Polling

The PC doesn't use interrupts. Therefore it is not necessary to perform accesses in I/O mode.

```
PCWATTR (R0, x"00")           /* set chip in common memory mode */
PCWMEM (CONTROLPC, x"01")     /* PC disables MCU's interrupts */
```

The available bits in CONFPC and CONFMCU can be used as flags to manage the data transfer. On the PC side, the memory can be reached by PCWMEM and PCRMEM functions.

X.2.3 - Interrupts

The PC uses interrupts. It is mandatory to perform accesses in I/O mode.

```
PCWATTR (R0, x"4C")           /* set chip in I/O memory, interrupt = level */
PCWIO (CONTROLPC, x"00")      /* PC enables MCU's interrupts */
...
MCUW (add0, data0)            /* MCU places data in memory */
MCUW (add1, data1)
...
MCUW (CONFMCU, x"80")         /* MCU sends interrupt to PC */
...
PCRIO(add0)                   /* PC reads data from memory */
PCRIO(add1)
...
PCWIO (CONFPC, x"40")         /* PC acknowledges interrupt and makes it disappear*/
```

X - APPLICATIONS (continued)

X.3 - UART Use

The following example assumes that CLKIN is used and that a 18.432MHz frequency is available on this pin.

```
PCWATTR(R0, x"60")        /* put chip in mcu memory mode, enable UART, IT level,
                             UART address = x"3f8" */
PCWATTR(PROGN, x"0B")     /* use clkin, divide by 10 to get 1.8432MHz on the UART */
PCWIO(x"3fb", x"83")      /* set UART DLAB bit at 1,8 bits, no parity */
PCWIO(x"3f8", x"03")      /* program divisor latch to 38400 bauds */
PCWIO(x"3f9", x"00")
PCWIO(x"3fb", x"03")      /* reset UART DLAB bit at 0 to continue */
PCWIO(x"3f8", x"55")      /* send a data */
PCRIO(x"3f8")             /* read a data */
```

X.4 - I/O Extension

X.4.1 - Wiring

The following example shows how to connect a peripheral on the chip. Connect :

- MCU_CS to '1' (it is not used).
- MCU_MOTEL to '1' (it is not used).
- CSL_ALE to the chip select input of your peripheral.
- MCU_DAT on the data line of your peripheral.
- MCU_ADD to '1' (it is not used).
- MCU_RWWR to '1' (it is not used).
- MCU_DSRD to '1' (it is not used).
- MCU_ACKWAIT may be left open.
- MCU_IRQ on a peripheral interrupt output line.
- IOW on the peripheral Write Enable input.
- IOR on the peripheral Read Enable input.

X.4.2 - Operation

```
PCWATTR (R0, x"48")       /* set chip in I/O extension mode, level interrupts*/
PCWATTR (ADRDEC, x"80")   /* peripheral address = x"200" */
PCWATTR (MASK, x"01")     /* peripheral address width = 8 bytes */
PCWIO (x"200", MY_DATA)   /* send a data to the peripheral device */
```

X.5 - Memory Extension

X.5.1 - Wiring

The following example shows how to connect a memory extension on the chip. Connect :

- MCU_CS to '1' (it is not used).
- MCU_MOTEL to '1' (it is not used).
- CSL_ALE to the chip select input of your memory.
- MCU_DAT on the data line of your memory.
- MCU_ADD to '1' (it is not used).
- MCU_RWWR to '1' (it is not used).
- MCU_DSRD to '1' (it is not used).
- MCU_ACKWAIT may be left open.
- MCU_IRQ to '0'.
- IOW on the memory extension Write Enable input.
- IOR on the memory extension Read Enable input.
- PC_ADD to the memory extension address bus.

X.5.2 - Operation

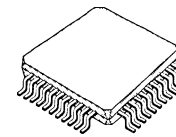
```
PCWATTR (R0, x"04")       /* set chip in memory extension mode */
PCWMEM (x"123", MY_DATA)  /* send a data to the memory extension */
PCRMEM (x"123")           /* send a data to the memory extension */
```

SGS-THOMSON MICROELECTRONICS

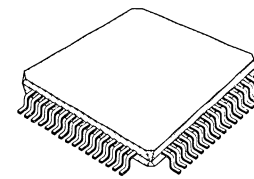
ST75C502

V.32bis/V.17 HIGH SPEED MODEM DATA PUMP

- 2 CHIP DATA PUMP (ST75C502, ST7544)
- V.32BIS, V.17, V.33, V.32, V.29, V.27ter, V.22BIS, V.22, V.21, V.23, BELL212A, 103 (SHORT TRAIN INCLUDING V.29/T104)
- GROUP 3 FAX AT 14400, 12000, 9600, 7200, 4800, 2400BPS
- PARALLEL/SERIAL SYNCHRONOUS DATA HANDLING
- DIGITAL FAR AND NEAR END ECHO CANCELLATION SUPPORTING A DELAY OF 2 SATELLITE HOPS (1.6 seconds) AND PHASE ROLL UP TO 10Hz
- AUTODIAL AND AUTOANSWER
- COMPLETE HANDSHAKE MANAGEMENT
- WIDE DYNAMIC RANGE (> 48dB)
- COMPROMISE TRANSMIT EQUALIZER
- AUTOMATIC ADAPTIVE EQUALIZER
- VOICE MODE (A LAW)
- ENHANCED PROGRAMMABLE TONE DETECTOR (INCLUDING DTMF)
- AUTO MODE (WITH MCU SUPPORT)
- ITU-T V.54 SIGNALLING
- ANCILLARY CONVERTERS FOR EYE PATTERN MONITORING
- VERSATILE INTERFACES
  - PARALLEL 64x8 DUAL PORT RAM
  - SYNCHRONOUS SERIAL I/O
  - AUXILLIARY PARALLEL I/O
- CALLER ID DEMODULATION
- LOW PROFILE TQFP PACKAGE OPTION



TQFP44
(Plastic Quad Flat Pack)



TQFP80
(Plastic Quad Flat Pack)

ORDERING INFORMATION

Sales Type	Function	Package
ST7544 CQFP	Mafe	TQFP 44
ST7544 CFN	Mafe	PLCC 44
ST75C502 CQFP	Romed DSP	TQFP 80
ST18933 PQFP	Customisable DSP	PQFP 160
STI8933 EMU-PC	PC Software Developement Tool	PC BOARD
SATURN	Modem Application with Protocols (V.42bis/FAX)	BOARD/CS

SUMMARY

I - GENERAL DESCRIPTION

This highly integrated modem consists of 2 chips, the first being a dedicated DSP (ST75C502), the second being the ST7544 MAFE. Emphasis has been put on performance and size/power consumption for portable applications.

This product gives a high performance modem conformant to ITU-T recommendations V.32bis, V.17, V.33, V.32, V.29, V.27ter, V.22bis, V.22, V.21 and V.23. Also Bell 212A and 103.

As a data modem the ST75C502 can operate at 14400, 12000, 9600, 7200, 4800, 2400, 1200, 300 or 75 bits per second as standard. As a fax, the ST75C502 fully supports group 3 send and receive speeds of 14400, 12000, 9600, 7200, 4800 and 2400 bits per second.

Programmable features allow the product to be tailored to a wide range of high speed modem requirements.In addition, to add to the flexibility of this product, the customer can develop, on a similar hardware platform to the standard product, proprietary code for ROMing into the memory of the DSP. If required, ability to access external memory of up to 64K x 32 is given such that customer specific modes of operation can be added and easily updated.Code development is made simple via a slot in PC development card and is fully supported by SGS-THOMSON (STI8933 PC-EMU).

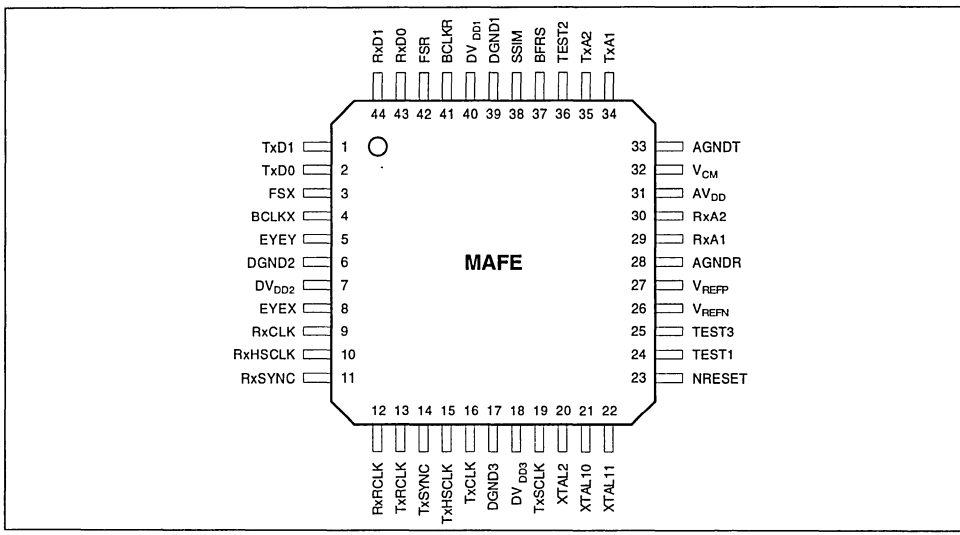
The voice mode allows for implementation of enhanced telephony functions such as answering machines.

For customer specific code requiring access to external memory, a 160 pin flatpack containing the DSP and a 44 pin flatpack containing the MAFE are also available (type numbers ST18933 and ST7544 respectively).

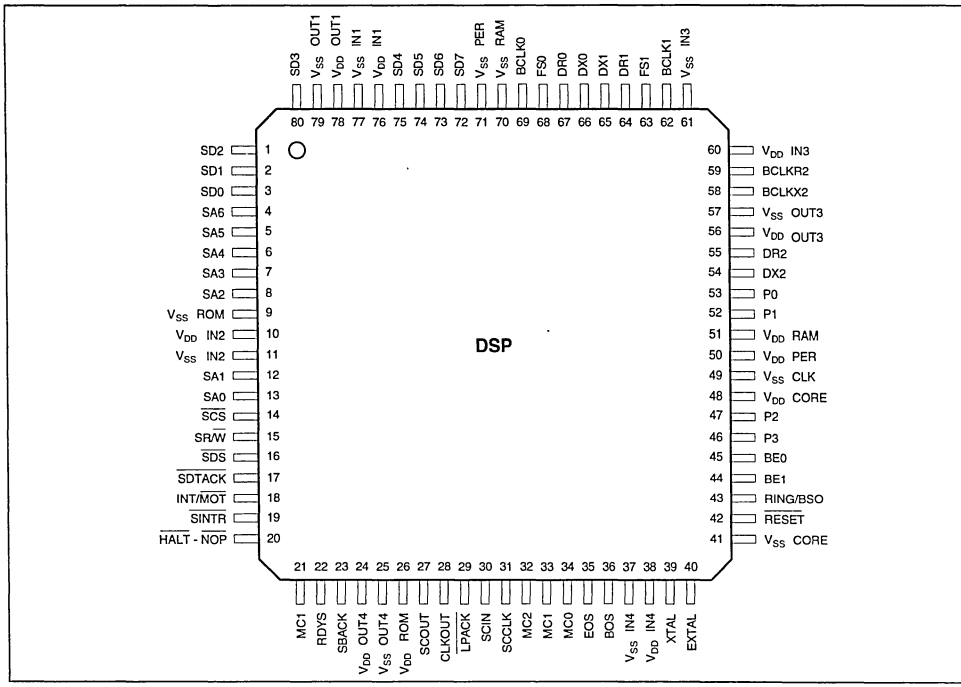
Further information on the DSP (STI8933) and MAFE (ST7544) can be found in the relevant datasheets

II - PIN CONNECTIONS

II.1 - ST7544CQFP Top View (TQFP44)

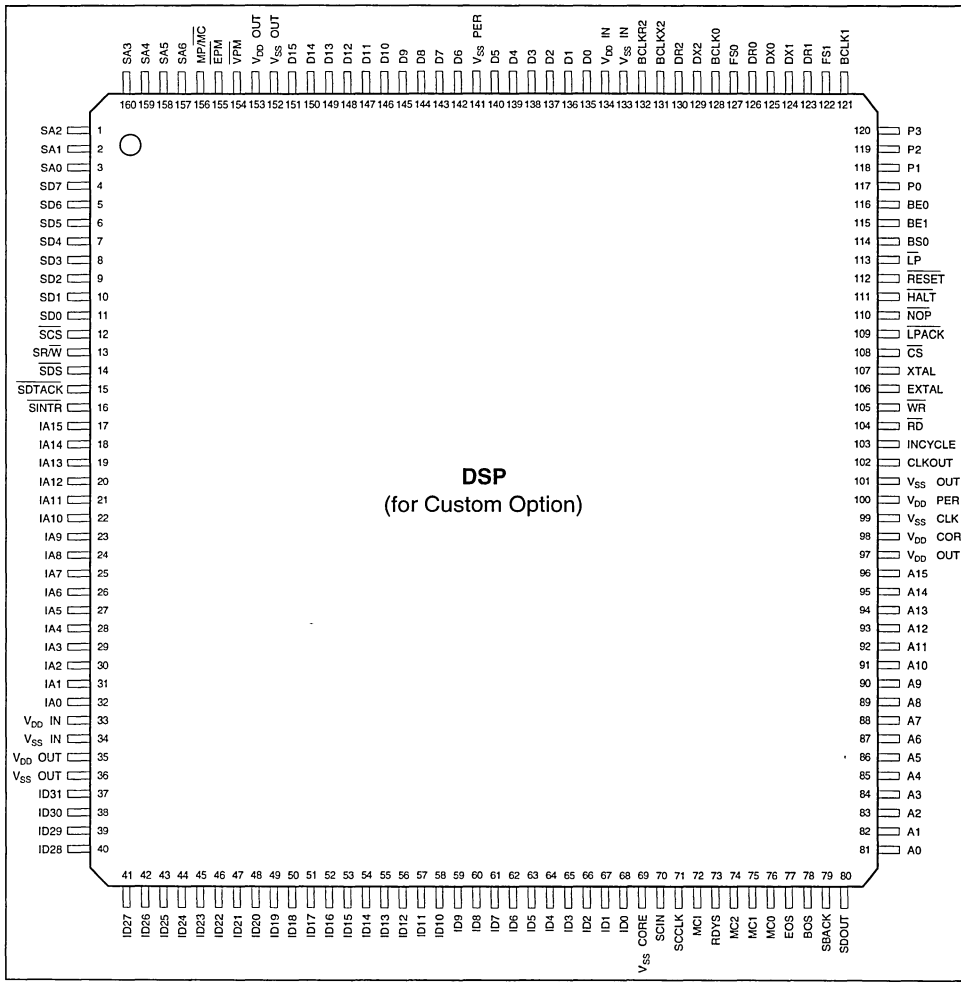


II.2 - ST75C502CQFP Top View (TQFP80)



75C50202 EPS

II.3 - ST18933PQFP Top View (PQFP160)



III - PIN DESCRIPTION

See Figure F2 in appendix F for complete schematics.

III.1 - Host Interface

The exchanges with the control processor proceed through a 64 Bytes DUAL port RAM shared between the DSP and the Host. The pins associated with this interface are :

Pin Name	Type	Description
SD0..SD7	I/O	System Data Bus. 8-bit data bus used for asynchronous exchanges between the ST75C502 and the Host through the DUAL port RAM. High impedance when exchanges are not active.
SA0..SA6	I	System Address Bus. 7-bit address bus for DUAL port RAM.
$\overline{SDS}$ ($\overline{SDS}$)	I	System Data Strobe. Active low. Synchronizes all the exchanges. In Motorola mode initiates the exchange, active low. In Intel mode initiates a read exchange, active low.
SR/$\overline{W}$ ($\overline{SWR}$)	I	System Read/Write. In Motorola mode defines the type of exchange read/write. In Intel mode initiates a write exchange, active low.
$\overline{SCS}$	I	System Chip Select. Active low.
$\overline{SDTACK}$	O	System Bus Data Acknowledge. Active low.
$\overline{SINTR}$	O	System Interrupt Request. Active low. This signal is asserted by the ST75C502 and negated by the Host.
$\overline{RESET}$	I	Reset. Active low.
$\overline{RING}$	I	Ring Detect Signal. Active low.
INT/$\overline{MOT}$	I	Select Intel/Motorola Interface.

III.2 - Serial Interface

The transmit and receive synchronous data exchanges between the DSP and microprocessor can pass via the Simplified Synchronous Serial Interface. Two pins are allowed for the data :

Pin Name	Type	Description
DR2	O	Synchronous Data Output
DX2	I	Synchronous Data Input

III.3 - Auxiliary Interface

A set of auxiliary signals are provided to simplify the DAA Interface. This is made by a three line General Purpose Parallel Input/Output.

Pin Name	Type	Description
P0	I/O	Parallel Input/Output 0
P1	I/O	Parallel Input/Output 1
P2	I/O	Parallel Input/Output 2

III.4 - Miscellaneous

Pin Name	Type	Description
XTAL	O	Internal oscillator Output. Left open if not used.
EXTAL	I	Internal oscillator Input, or External Clock
CLKOUT	0	Internal clock (XTAL frequency divided by 2)

Note : The nominal external clock frequency of the DSP is 36.864MHz. The nominal external clock frequency of the MAFE is 18.432MHz with a precision better than $\pm 5.10^{-5}$ (and is output from the DSP on the CLKOUT Pin).
When in Sleep Mode the CLKOUT clock is not available.

III.5 - Mafe Interface

A set of signals is use for interconnection between the DSP and the Analog Front End.

Pin Name		Description
DSP	MAFE	
P3	NRESET	Reset of the Analog Front End
BCLK0	BCLKR	Receive Serial I/O Clock
FS0	FSR	Receive Serial I/O Frame Synchro
DX0	RXDI	Receive Serial I/O Input
DR0	RXDO	Receive Serial I/O Output
BCLK1	BCLKX	Transmit Serial I/O Clock
FS1	FSX	Transmit Serial I/O Frame Synchro
DX1	TXDI	Transmit Serial I/O Input
DR1	TXDO	Transmit Serial I/O Output
BCLKX2	RXCLK	Receive Bit Clock
BCLKR2	TXCLK	Transmit Bit Clock
BE0	RXRCLK	Receive Baud Clock
BE1	TXRCLK	Transmit Baud Clock

III.6 - Power Supply

Pin Name	Number	Description
V_{DD}	11	+5V Supply (Pins 10, 24, 26, 38, 48, 50, 51, 56, 60, 76, 78)
V_{SS}	12	0V (Pins 9, 11, 25, 37, 41, 49, 57, 61, 70, 71, 77, 79)

III.7 - Boundary Scan Interface

A set of 13 signals are dedicated for Testing the DSP. These signals can be used in a development phase, associated with SGS-THOMSON ST18932 Boundary Scan Development Tools, to Debug the application Hardware and Software. Input signals must be grounded.

Pin Name	Type	Description
SCIN	I	Scan Data Input
SCCLK	I	Scan Clock
SCOUT	O	Scan Data Output
BOS	I	Begin of Scan Control
EOS	I	End of Scan
MC0..MC2	I	Mode Control
SBACK	O	Software Breakpoint Acknowledge
MCI	O	Multicycle Instruction
RDYS	O	Ready to Scan Flag
$\overline{\text{HALT}}$	I	Stop ST75C502 Execution. Active Low.
$\overline{\text{LPACK}}$	O	Acknowledge Low Power Mode

IV. - ELECTRICAL SPECIFICATIONS

Unless otherwise specified, electrical characteristics are specified over the operating range. Typical value are given for V_{DD} = +5V and T_{amb} = 25°C and for nominal crystal frequency of 36.864 MHz.

IV.1 - Maximum Ratings (referenced to GND)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3, +7.0	V
V_I, V_{IN}	Digital Input Voltage	-0.3, V_{DD} + 0.3	V
I_I, I_{IN}	Digital Input Current	± 1	mA
I_O	Digital Output Current	± 20	mA
T_A	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature (plastic)	-40, +125	°C
P_{tot}	Maximum Power Dissipation	TBD	mW

Stresses above those hereby listed may cause damage to the device. The ratings are stress related only and functional operation of the device in conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

IV.2 - DC Characteristics

V_{DD} = 5V ± 5%, GND = 0V, T_A = 0 to 70°C (Unless otherwise specified).

IV.2.1 POWER SUPPLY AND COMMON MODE VOLTAGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DD}	Supply Current		110		mA
I_{DD}-LP	Supply Current in Low Power Mode		8		mA

IV.2.2 - Digital Interface

All digital pins except XTAL pins.

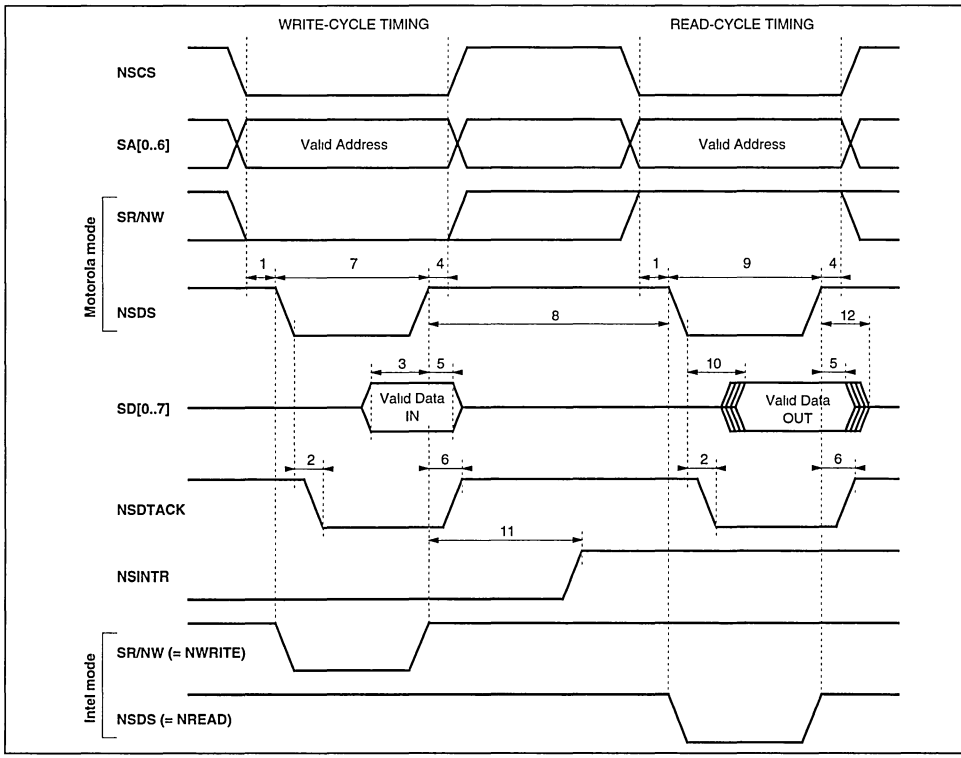
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage	-0.3		0.8	V
V_{IH}	High Level Input Voltage	2.4			V
I_I	Input Current V_I = V_{DD} or V_I = GND	-10	0	+10	µA
V_{OH}	High Level Output Voltage (I_{LOAD} = 2mA)	2.8			V
V_{OL}	Low Level Output Voltage (I_{LOAD} = 2mA)			0.5	V
I_{OZ}	Three State Input Leakage Current (GND < V_O < V_{DD})	-10	0	10	µA
C_{IN}	Input Capacitance		5		pF

IV.2.3 - Crystal Oscillator Interface (XTAL, EXTAL)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage			0.8	V
V_{IH}	High Level Input Voltage	2.7			V
I_L	Low Level Input Current GND < V_I < V_{ILmax}	-20		-7	µA
I_H	High Level Input Current V_{IHmin} < V_I < V_{DD}	7		20	µA

IV.3 - AC Electrical Characteristics
IV.3.1 - Dual Port Ram Host Timing

Figure 1

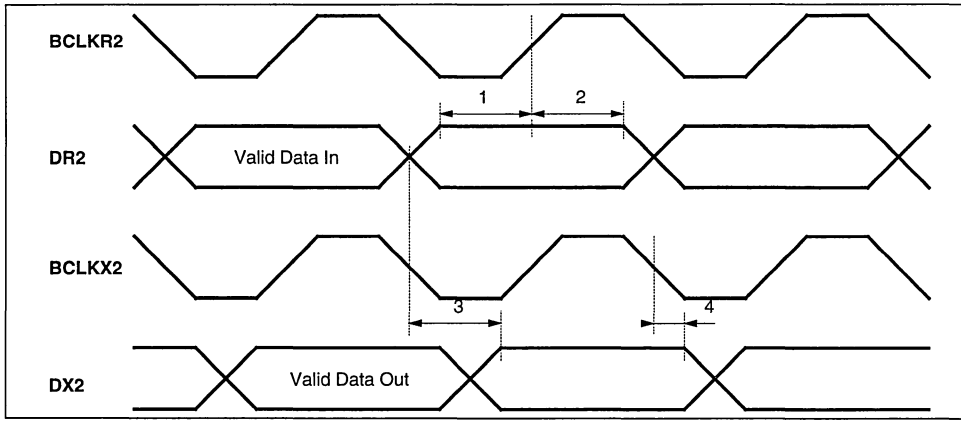


Number	Description	Min.	Typ.	Max.	Unit
1	Address and Control Setup Time	5			ns
2	SDTACK Acknowledge			20	ns
3	Data Setup Time	10			ns
4	Address and Control Hold Time	0			ns
5	Data Hold Time	5			ns
6	SDTACK Hold Time	0			ns
7	Write Enable Low State	45			ns
8	Access Inhibition High State (1)	70			ns
9	Read Enable Low State	45			ns
10	Read Data Access			35	ns
11	SINTR Clear Delay			50	ns
12	Data Valid to Tristate			15	ns

Note 1 : A minimum delay of 70ns is required only from the rizing edge of NWRITE to the falling edge of the next selected NREAD or NWRITE.

IV.3.2 - Serial Interface Timing

Figure 2



Number	Description	Min.	Typ.	Max.	Unit
1	DR2 to BCLKR2 Set-up Time	30			ns
2	DR2 to BCLKR2 Hold Time	10			ns
3	DX2 Valid to BCLKX2 Delay Time			100	ns
4	DX2 to BCLKX2 Hold Time. DX2 Signal is High Z Just After Reset	0			ns

V - FUNCTIONAL DESCRIPTION

V.1 - System Architecture

The system is based on a two-chip set. The first chip is the ST75C502 dedicated DSP handling all the signal processing routines for transmission, reception and echo cancellation on modem signals. It also holds the tone generators and detectors. Alternately the ST18933 DSP is available for customer specific operations. The second chip is the ST7544 delta-sigma MAFE, which performs the AD/DA conversions as well as the signal pre or post-filtering, and the sampling interpolation on the echo cancellation path.

The chip set allows the design of a complete V.32bis data-pump without any external component. A versatile dual port RAM allows an easy interface with most popular micro-controllers.

V.2 - Chip Set Interconnect Circuitry

Please refer to appendix F for a detailed schematic of the chip set interconnect circuitry.

V.3 - Operation

V.3.1 - Modes

The modem implementation is fully compatible with many popular ITU-T and Bell recommendations. The modulation can be either Trellis Coded Modulation (TCM) as in V.33 14400, 12000, V.32bis 14400, 12000, 9600, 7200, V.32 9600 bps rates, Quadrature Amplitude Modulation (QAM) as in V.32bis 4800, V.32 9600, 4800, V.22bis 2400, Differential Phase Shift Keying (DPSK) as in V.22 1200, Bell 212A 1200 bps rates, or Frequency Shift Keying (FSK) as in V.21, V.23 and Bell 103 modes. Both the bit rate and the treillis options are determined during the initial modem handshake sequence. V.29, V.27ter and V.17 are also available for FAX transmission. Other modes of operation include tone and DTMF detection or generation and voice mode.

V.3.2 - Transmitter Description

The signal pulses are shaped in a dedicated filter combined with a compromise transmit equalizer suited for transmission over strongly distorted lines. 2 different compromise equalizers are available and can be selected by software. User defined transmit equalizers can be downloaded in the DSP RAM.

V.3.3 - Echo Canceller Description

The echo canceller consists of a near end and a far end echo canceller. Both are fractionally spaced and achieve a high cancellation of the echo paths. The receive signal reconstruction is purely digital by virtue of the MAFE architecture. The far end echo requires either an external low cost 8kx8-100ns memory (for the customisable product STI8933), or the allocation of an equivalent amount of RAM in the controller memory space. It also sustains up to 10Hz of frequency offset on the far end echo path without degradation of performance.

V.3.4 - Receiver Description

The receiver section handles complex signals and uses a fractionally spaced complex equalizer. It is able to cope with distant modem frequency drifts up to 10^{-4} as specified in the ITU-T recommendations. It also compensates for phase jitter at multiple and simultaneous frequencies.

V.3.5 - Tone Generator Description

Four tones can be simultaneously generated by the ST75C502. The tones are determined by their frequencies and by the output amplitude level. A set of specific command is also available for DTMF generation (using two of the four generators available).

V.3.6 - Tone Detector Description

16 tones can be simultaneously detected by the ST75C502. Each of the tones to be detected is defined by the coefficients of a 4th order programmable IIR. Detection thresholds are also programmable from -45dBm up to -10dBm.

V.3.7 - DTMF Detector Description

A DTMF detector is included In the ST75C502, it permits detection of valid DTMF digits. A valid DTMF digit is defined as a dual tone with total power higher than -35dBm, duration greater than 40ms and differential amplitude within 8dB (positive or negative).

V.3.8 - Voice Mode Description

The ST75C502 voice mode allows the implementation of enhanced telephony functions such as answering machines. Incoming samples (7200Hz) from the line are PCM-A-law coded and are written into the dual port RAM. The outgoing samples are decompressed using the same A-law and are output to the telephone line.

The voice mode is entered using a CONF command, it can be either transmit voice from the dual RAM Tx buffer to the telephone line, receive voice from the telephone line to the dual RAM buffer, or both of these functions simultaneously. The format of the signal is A-law coded without complementation of the even bits. The buffer mechanism, between the host micro-controler and the ST75C502 is identical to the mechanism used for parallel data exchanges except that it starts immediately after CONF command, the size of the transmit and received buffer, are and must be 8 bytes, there is no need for a XMIT command, and if an overrun or underrun condition occurs no error will be reported to the host processor.

V.3.9 - Analog Loop Back Test Mode

In any transmission standard and any data format, the ST75C502 can be configured for analog loop back test

V.3.10 - Digital Loop Back Test Mode

These loop back modes comply with the test loop 2 of the ITU-T V.54 recommendation for V.32 and V.32 bis. For V.22 and V.22 bis the digital loop back modes comply with these recommendations.

V.3.11 - Low Power Mode

When entering the low power mode all the peripherals of the DSP core are stopped in order to reduce the power consumption, the ST7544 is set in low power mode. The dual RAM is made inaccessible.

A hardware RESET must awake the ST75C502.

V.3.12 - Reset

After a hardware RESET, or an INIT command, the ST75C502 clears all its internal memories, clears the whole DUAL RAM and starts to initialize the ST7544 Delta Sigma Analog converters. As soon as these initializations are completed, the ST75C502 clears the DUAL RAM address 0 (COMSYS), generates an interrupt IT6 (command Acknoledge) and is programmed to send and receive tones, the bit clocks are programmed to 9600Hz. The transmit sample clock is set to 7200Hz and the receive sample clock to 9600Hz.

The total duration of this "cold" RESET sequence is about 500ms. After that time the ST75C502 is ready to execute commands sent by the host micro-controler. Be carrefull that any command send in this reset time will be lost.

The minimum duration of the RESET signal is 700ns.

In order to speed up the RESET time, a "Warm" initialization is possible using the INIT 01 command ; in this case the RESET time is less than 10ms ; the only difference is that the ST7544 is not initialized again.

V.4 - Modem Interface

V.4.1 - Analog Interface

The modem designer must provide a proper hybrid interface to the ST7544. An example of hybrid design is given in appendix F (see Figure F1). The inputs and outputs of the MAFE are differential, thus achieving better noise immunity.

V.4.2 - Host Interface

The host interface is seen by the micro as a 64x8 RAM, with additional registers accessible through an 7-bit address space. This RAM can be used for data transmission using the SERIAL command.

V.4.3 - Auxiliary Parallel Interface

The auxiliary parallel interface is a general purpose 3-bit parallel interface, which carries various signals, used by the controller and the analog part of the modem. Each pin can be independently programmed for input or output.

V.4.4 - Auxiliary Serial Interface

The auxilliary serial interface is a serial synchronous I/O, which carries the bit data flow.

V.4.5 - Eye Pattern Converters

The output from these two D to A converters on ST7544 provides direct display of the constellation.

VI - USER INTERFACE
VI.1 - Dual Port Ram Description

The dual port RAM is the standard interface between the controller and the ST75C502, for either commands or data. This memory is addressed through a 7-bit address bus. The locations from $00 to $3F are RAM locations, while locations from $40 to $50 are control registers dedicated to the interrupt handling.

Several functional area are defined in the dual port RAM, namely :
- the command area,
- the report area,
- the status area,
- the bulk delay exchange area,
- the data buffer areas.

VI.1.1 - Mapping
VI.1.1.1 - Command Area

The command area is located from $00 to $04. Address $00 holds the command byte COMSYS, and the four next locations hold the parameters COMPAR[0..3]. The command parameters must be entered before the command word is issued. Once the command has been entered, the command byte is reset and an acknowledge report is issued. A new command should not be issued before the acknowledge counter COMACK is incremented. The command exchange rate has a maximum of 2400Hz.

VI.1.1.2 - Report Area

The report area is located from address $05 to address $07. Location $05 holds the acknowledge counter COMACK. Each time a command is acknowledged, the report bytes COMREP[0..1] (if any) are written into locations $06 and $07, and the content of COMACK is incremented. This counter allows an acurate monitoring of the command processing by the ST75C502.

VI.1.1.3 - Status Area

The status area is located from address $08 to $0A. The error status word SYSERR is located at address $08. This error status word is updated each time an error condition occurs. An optional interruption IT0 may be triggered as well in the case of an error condition. Locations $09 and $0A hold the general status bytes STATUS[0..1]. The meaning of the bits depends of the mode of operation, and is described in Appendix B. The third byte at address $0B holds the Quality Monitor byte STAQUA.

VI.1.1.4 - Optional Status Area

The user can program (through the DOSR command) the three locations STAOPT[0..2] of the Optional Status Area ($0C to $0E) for the real time monitoring of three arbitrary memory locations.

VI.1.1.5 - Bulk Delay Exchange Area

This area is reserved for V.32 / V.32bis storage of Far End echo canceller symbols. Refer to Appendix H and application note.

This area has two sub-sections :a flagging section ($0F to $13) and a bulk data area ($14 to $1B).

Location $0F holds the bulk data buffer status SYMSTA. Locations $10 and $11 (resp. $12 and $13) contain a pointer to the bulk data buffer SYMADR[0..1] (resp. SYMADT[0..1]), in the controller space, which should receive (resp. send) the next group of 8 delayed symbols. The ST75C502 manages thus an area of 4k bytes in a circular addressing mode inside the controller memory space. The buffer SYMBUF[0..7] containing the symbols received or sent to the controller is located from $14 to $1B.

VI.1.1.6 - Data Buffer Area

The Data Buffer Area is made of two double 8-byte Buffers. Each of the four buffers is attached to a status byte. This status byte contains the number of valid Data Byte inside the Data Buffer. Within each buffer, D0 represents the first bit in time.

VI.1.2 - Interruptions

The ST75C502 can generate 6 interrupts for the controller. The interrupt handling is made with a set of registers located from $40 to $50.

The interruptions generated by the ST75C502 come from seven different sources. Once the ST75C502 rises an interrupt, a signal is sent to the controller. The controller has then to process the interrupt and clear it. The interrupt source can be examined in the Interrupt Source Register ITSCRC located at $50. According to this status byte, the interrupt source can be determined. Then, writing a zero at one of the memory location $40 to $46 (Reset Interrupt Registers ITREST[0..6]) will reset the corresponding interrupt (and thus acknowledge it). These six sources of interruptions can be masked globally or individually using the Interrupt Mask Register ITMASK located at $4F.

The 7 series interrupt sources are :

IT0 Error/Warning : an error has occurred and the error code is available in the error status byte SYSERR. This byte can be selectively cleared by the CSE command.

IT1 Bulk Delay : the bulk delay buffer requires an action from the controller, for emptying it and for filling it with symbols.

IT2 Tx Buffer : each time the ST75C502 frees a buffer, this interrupt is generated.

IT3 Rx Buffer : each time the ST75C502 has filled a buffer, this interrupt is generated.

IT4 Status Byte : the modem status byte has changed and has to be checked by the controller.

IT6 Command Acknowledge : the ST75C502 has read the last command entered by the host, incremented the command counter COMACK, and is ready for a new command.

ITSRCR	x	D6	x	D4	D3	D2	D1	D0

D0 = 1 IT0 Pending
D1 = 1 IT1 Pending
Dn = 1 ITn Pending

ITMASK	D7	D6	x	D4	D3	D2	D1	D0

D7 and D0 = 1 IT0 Enabled
D7 and D1 = 1 IT1 Enable
D7 and Dn = 1 ITn Enabled

VI.1.3 - Host Interface Summary

Address (hex)	Description	Size (Byte)	Mnemonic
COMMAND AREA			
$00	Command	1	COMSYS
$01-$04	Command Parameters	4	COMPAR[0..3]
REPORT AREA			
$05	Acknowledge Counter	1	COMACK
$06-$07	Report	2	COMREP[0..1]
STATUS AREA			
$08	Error Status	1	SYSERR
$09	General Status	2	STATUS[0..1]
$0B	Quality Monitor	1	STAQUA
$0C-$0E	Optional Report	3	STAOPT[0..2]
BULK DELAY AREA			
$OF	Symbol Buffer Status	1	SYMSTA
$10-$11	Symbol Rx Buffer Pointer	2	SYMADR[0..1]
$12-$13	Symbol Tx Buffer Pointer	2	SYMADT[0..1]
$14-$1B	Symbol Buffer	8	SYMBUF[0..7]
DATA AREA			
$1C	Data Rx Buffer 0 Status	1	DTRBS0
$25	Data Rx Buffer 1 Status	1	DTRBS1
$2E	Data Tx Buffer 0 Status	1	DTTBS0
$37	Data Tx Buffer 1 Status	1	DTTBS1
$1D-$24	Data Rx Buffer 0	8	DTRBF0[0..7]
$26-$2D	Data Rx Buffer 1	8	DTRBF1[0..7]
$2F-$36	Data Tx Buffer 0	8	DTTBF0[0..7]
$38-$3F	Data Tx Buffer 1	8	DTTBF1[0..7]
INTERRUPT AREA			
$40-$46	Reset Interrupt Register	7	ITREST[0..6]
$4F	Interrupt Mask Registe	1	ITMASK
$50	Interrupt Source Register	1	ITSRCR

VI.2 - Command Set

The Command Set has the following attractive features :

- user friendly with easy to remember mnemonics.
- possibility of straight forward expansion with new commands to suit specific customer requirements.
- easy upgrade of existing software using previous modem based SGS-THOMSON products.

The command set has been designed to provide the necessary functional control on the ST75C502. Each command is classified according to its syntax and the presence/absence of parameters. In the case of a parametric command, parameters must first be written into the dual port RAM before the command is issued. Acknowledge and error report is issued for each command entered.

VI.2.1 - Command Set Summary

VI.2.1.1 - Operational Control Commands

INIT Initialize. Initialize the modem chipset. Set all parameters to their default values and wait for commands of the control processor. Parametric command.

IDT Identify. Return the product identification code. Non parametric command.

SLEEP Turn to Low Power Mode. The modem engine issues a control signal to the MAFE in order to switch to Sleep Power Mode, then switches itself into Sleep Power Mode. Non parametric command.

HSHK Handshake. Begins the handshake sequence. The modem chipset carries all the steps defined in the ITU-T recommendations. A status report indicates to the control processor the state of the handshake and the final negotiated transmission bit rate. This command only applies to modes where a handshake sequence is defined. A CONF command must have been issued prior to the use of HSHK. Non parametric command.

RTRA Retrain. Start sending the retrain sequence as specified in the ITU-T recommendation. This command only applies to modes where a retrain sequence is defined. In V.32bis, this command also initiates the rate negotiation sequence. Parametric command.

CSE Clear Status Error. Selectively clears the Error status byte SYSERR. Parametric command.

SETGN Set gain. This command sets the global gain factor, which is used for the transmit samples. Parametric command.

STOP FAX Stop. Stop FAX half duplex transmitter. Non parametric command.

SYNC FAX Synchronize. Start/Stop of FAX half duplex receiver. Parametric command.

VI.2.1.2 - Data Communication Commands

XMIT Transmit data. Enable/disables the transmission of data in parallel mode. After a XMIT command, the ST75C502 sends the data contained in its dual port RAM. Parametric command.

SERIAL This command selects the data source, i.e. either parallel or serial. The parallel mode uses a part of the dual port RAM as a double buffer. The serial mode uses the serial synchronous I/O. Parametric command.

VI.2.1.3 - Digital Loop Back Commands

V54 V.54 Digital Loop Back. Enables/Disables the transmission and reception of V.54 patterns. This command must be used only in V.32 bis or V.32 mode. Parametric command.

V22L2 V.22/V.22 bis Digital Loop Back. Enables/Disables the transmission and reception of V.22 Loop 2 patterns. This command must be used only in V.22 bis or V.22 mode. Parametric command.

VI.2.1.4 - Memory Handling Commands

MW Memory Write. This command is used to write an arbitrary 16-bit value into the writable memory location currently specified by a parameter. Parametric command.

MR Memory Read. This command allows the controller to read any of the RAM locations without interrupting the processor. Parametric command.

CR Complex Read. This command allows the controller to read at the same time the real and imaginary part of a complex value stored in a double RAM location. This feature is very interesting for eye pattern software control as well as for equalization monitoring. This command insures that the real and imaginary part are sampled in the memory at the same time (integrity). Parametric command.

VI.2.1.5 - Configuration Control Commands

CONF Configures. This command configures the modem chipset for data transmission and handshake procedures (if any) in any of the supported modes. The transmission parameters are set to their default values and can be modified with the MODC command. This command also defines the parameters in the case of an automatic standard recognition and the boundaries of the speed negotiation. Parametric command.

MODC Modify Configuration. This command allows modification of part of the parameters set up by the CONF command. Parametric command.

BULK Define Symbol Bulk Management. This command selects the dual port RAM symbol management, in V.32bis and V.32 modes. Parametric command.

DOSR Define Optional Status report. This command allow the modification of the optional status report located in the status area of the dual port RAM. One can thus select a particular parameter to be monitored during all modes of operation. Parametric command.

DSIT Define Status Interrupt. This command allows the programmation of the status word bit that will generate an Interrupt to the controller. Parametric command.

PPS Parallel Port Set. This command allows the modification of the parallel port configuration. Each of the four bits of this port can be programmed either as an input or an output. Parametric command.

PPR Parallel Port Read. This command reads the value of the 4-bit parallel port. The value is read whether it is an input or not. Non parametric command.

PPW Parallel Port Write. This command writes a 4-bit value into the parallel port. The bits are masked according to their input/output status. Parametric command.

VI.2.1.6 - MAFE Control Commands

WMR Write MAFE register. Causes the DSP to write a parameter into a MAFE register. Parametric command.

VI.2.1.7 - Tone Generation Commands

TONE Select Tone. Programs the tone generator(s) for the desired default tone(s). Additional mnemonics provide quick programming of DTMF tones or other currently used tones. Parametric command.

DEFT Define Tone. Programs the tone generator(s) for arbitrary tone synthesis. Parametric command.

TGEN Tone Generator Control. Enables or disables the tone generator(s). Parametric command.

IV.2.1.8 Tone Detection Commands

TDRC Read coefficients of tone detection cell. Parametric command.

TDWC Write coefficients of tone detection cell. Parametric command.

TDRW Read wiring of tone detection cell. Parametric command.

TDWW Write wiring to tone detection cell. Parametric command.

TDZ Clear the values of tone detection cell. Parametric command.

VI.2.2 - Command Set Short Form

Mnemonic	Value	Description
XMIT	0X01	Receive/TransMIT data
SETGN	0X02	SET GaiN
SLEEP	0X03	Low Power mode
HSHK	0X04	HandSHaKe
RTRA	0X05	ReTRAin
INIT	0X06	INITialization
SERIAL	0X07	SERIAL mode
CSE	0X08	Clear Status Error
MR	0X10	Memory Read
CR	0X11	Complex Read
MW	0X12	Memory Write
DSIT	0X13	Define Status word InTerrupt
IDT	0X14	IDenTify
PPS	0X15	Parallel Port Set
PPR	0X16	Parallel Port Read
PPW	0X17	Parallel Port Write
JSR	0X18	Jump to Sub Routine
CALL	0X19	CALL a sub routine
CONF	0X20	CONFigure
MODC	0X21	MODify Configuration
BULK	0X22	Define symbol BULK management
V54	0X23	Enable/Disable V.54
V22L2	0X24	Enable/Disable V.22 Loop2
STOP	0X25	FAX STOP Transmitter
SYNC	0X26	FAX SYNChronize Receiver
DOSR	0X0A	Define Optional Status Report
WMR	0X0B	Write Mafe Register
TONE	0X0C	Select TONE
TGEN	0X0D	Tone GENerator control
DEFT	0X0E	DEFine Tone
TDRC	0X1A	Tone Detect Read Coefficient
TDWC	0X1C	Tone Detect Write Coefficient
TDRW	0X1B	Tone Detect Read Wiring
TDWW	0X1D	Tone Detect Write Wiring
TDZ	0X1E	Tone Detect Zero cell

VI.2.2.1 - Miscellaneous Commands

CALL Call a Subroutine. Call a Subroutine with one parameter.

JSR Call a low level Subroutine. Call an internal subroutine with one parameter.

VI.3 - Status - Reports

VI.3.1 - Status

The ST75C502 has a dedicated status reporting area located in its dual port RAM. This allows a continuous monitoring of the status variables without interrupting the DSP.
The first status byte gives the error status. Issuing of an error status can be also flagged by a maskable interrupt for the controller. The signification of the error codes is given in Annexe B.
The second and third status bytes give the general status of the modem. This two byte status can generate, when a change occurs, an interrupt to the controller; each bit of that two byte word can be masked independently.
The fourth byte gives, in real time, a measure of the reception quality. This information may be used by the controller for retrain purpose.
Three other locations are dedicated for custom status reporting. This status includes, for example, the handshake phase, the negotiated data rate, and other items described in Annexe B. The controller can program the ST75C502 for a real time monitoring of any of its internal RAM location. High byte or low byte of any word can thus be monitored.

VI.3.2 - Reports

The ST75C502 features an acknowledge and report facility. The acknowledge of a command is monitored by a counter COMACK located in the dual port RAM. Each time a command is executed from the command area, the ST75C502 will increment this counter. For instance, when a MR (Memory Read) command is issued, the data is first written in the report area, and the counter is incremented afterwards. This way of processing insures the data integrity as well as an additional synchronization between the controller and the data pump.

VI.4 - Data Exchange

The ST75C502 accepts two kinds of data exchange : Parallel synchronous through the DUAL RAM or SERIAL synchronous. Detailed description of the Data Buffer Exchange modes of operation is available in Appendix H.

VI.4.1 - Parallel Data Mode

VI.4.1.1 - Transmit

The controller must first fill at least the first buffer of data (Tx Buffer 0) with the bits to be transmitted. In order to perform this operation, the controller must first check the Tx Buffer 0 status word DTTBS0. If this buffer is empty, the controller fills the data buffer locations (up to 8 bytes), and then writes in DTTBS0 the number of bits contained in the buffer. The controller can then either proceed with the second buffer or initiate the transmission with a XMIT command.
The ST75C502 copies the contents of the data buffer and then clears the buffer status word in order to make it again available. The number of bytes specified by the status word is then queued for transmission. The process goes on with the two

buffers until an XMIT command stops the transmission. After the finishing XMIT command has been issued, the last buffers are emptied by the ST75C502.
Error occurs when both buffers are empty while the transmit byte queue is also empty. Error is signalled with an interruption to the controller through the SYSERR register.

VI.4.1.2 - Receive

The controller should take care of releasing the Rx buffers before the Data Carrier Detect goes true. This is made by writing a zero in the Rx Buffer Status 0 and 1. The ST75C502 then fills the first buffer, and once filled sets the status word with the number of bytes received. It then takes control of the second buffer and operates in the same way. The controller must check the status of the buffers and empty them. Once the data is read, the controller must release the used buffer and wait for the next buffer to be full. Interrupts are available for an additional flagging of these events.
Error occurs when both buffers are declared full, and incoming bytes still arrive from the line.
Synchronous Data Buffer Exchanges are described in Annex H.

VI.4.2 - Serial Exchanges

The second mode of operation for data exchanges is the Serial Synchronous Mode. In this mode, the data I/O is made through a pair of dedicated hardware pins (DR2, DX2).

VI.4.3 - Mafe Clocks

The MAFE generates all the transmit and receive clocks necessary for the modem application, some of them are to be also connected to the ST75C502 (see Table paragraph III.5 - MAFE INTERFACE). For more detailed information, please, refer to the ST7544 Data Sheet.

Table 1 : Modem Modes

Mode	Modulation	Carrier Frequency (Hz)	Data Rate (Bps)	Baud or symbol per second	Bits per symbol	Constellation points	TxCLK	RxCLK
V.32bis	QAM TCM	1800	14400 12000 9600 7200 4800	2400	6 5 4 3 2	128 64 32 16 4	14400 12000 9600 7200 4800	idem TxCLK
V.32	QAM TCM	1800	9600 4800	2400	4 2	32, 16 4	9600 4800	idem TxCLK
V.22bis originate	QAM	1200	2400 1200	600	4 2	16 4	2400 1200	idem TxCLK
V.22bis answer	QAM	2400	2400 1200	600	4 2	16 4	2400 1200	idem TxCLK
V.22 or Bell 212 originate	DPSK	1200	1200	600	2	4	1200	idem TxCLK
V.22 or Bell 212 answer	DPSK	2400	1200	600	2	4	1200	idem TxCLK
V.23 answer	FSK	1300, 2100	1200	1200	1	-	7200	9600
V.23 originate	FSK	390, 450	75	75	1	-	7200	9600
Bell 103 originate	FSK	1270, 1070	300	300	1	-	7200	9600
Bell 103 answer	FSK	2225, 2025	300	300	1	-	7200	9600
V.21 originate	FSK	980, 1180	300	300	1	-	7200	9600
V.21 answer	FSK	1650, 1850	300	300	1	-	7200	9600
V.33	QAM TCM	1800	14400 12000	2400	6 5	128 64	14400 12000	idem TxCLK
V.17	QAM TCM	1800	14400 12000 9600	2400	6 5 4 3	128 64 32 16	14400 12000 9600 7200	idem TxCLK
V.29	QAM	1700	9600 7200 4800	2400	4 3 2	16 8 4	9600 7200 4800	idem TxCLK
V.27ter	DPSK	1800	4800 2400	1600 1200	3 2	3 2	4800 2400	idem TxCLK
V.21 ch 2	FSK	1650, 1850	300	300	1	-	300	300

APPENDIX A : COMMAND SET DESCRIPTION

Commands are presented according to the following form :

COMMAND - Command name meaning

Opcode : hexadecimal digit

X	X	X	X	X	X	X	X

Synopsis

Short description of the functions performed by the command

Parameters

Field	Byte	Pos.	Value	Definition
Name	X	a..b		Explanation of the parameter
			xx *	Default value

Field : Name of the addressed bit field.
Byte : Index (or address in the dual port RAM) of the parameter byte (from 1 to 4).
Pos. : Bit field position inside the parameter byte. Can either be a single position (from 0 to 7, 0 being LSB) or a range.
Value : Possible values for the bit (resp. bit field). *range* means all values are allowded. A value followed by a star means a default value. Values are expressed either under the form of a bit string, or under hexadecimal format.

Command :

BULK - Define Symbol Management

Opcode : 22

0	0	1	0	0	0	1	0

Synopsis

BULK allows the use of the DUAL RAM symbol area. This additional task into host firmware is only needed in V.32/V.32bis mode. This mode of operation is mandatory.

In this command the user sets the virtual memory base address and the top memory address (the base address must be on a 8 byte boundary and the top address on a 8 byte boundary - 1 eg : 0x67FF) of the MCU memory space reserved for BULK DELAY symbols storage.

Parameters

Field	Byte	Pos.	Value	Definition
BA_ADDR_L	1	7..0		Low byte of the base address
BA_ADDR_H	2	7..0		High byte of the base address
TO_ADDR_L	3	7..0		Low byte of the top memory address
TO_ADDR_H	4	7..0		High byte of the top memory address

(required capacity in MCU memory space is 2400 x d (d = BULK DELAY in seconds))

CALL - Call a subroutine

Opcode : 19

0	0	0	1	1	0	0	1

Synopis

CALL allows to execute a part of the DSP firmware with a specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	7..0		Low byte of the call address
C_ADDR_H	2	7..0		High byte of the call address
C_DATA_L	3	7..0		Low byte of the argument
C_DATA_H	4	7..0		High byte of the argument

CONF - Configure for operations

Opcode : 20

0	0	1	0	0	0	0	0

Synopsis

CONF allows the complete definition of the ST75C502 operation, including the mode of operation (Tone, Data Transmit, FAX Transmit, Voice Transmit, Voice Receive, DTMF Receive, ...) and the Modem Parameters (Standard, Speed, ...).

Parameters

Field	Byte	Pos.	Value	Definition
CONF_OPER	1	3..0	-	Mode of operation, see below
CONF_ANAL	1	4	0 1	Normal mode Analog loop back
CONF_PSTN	1	5	0 1	PSTN (carrier detect set to -43/-48dBm) Lease line (carrier detect -33/-38dBm)
CONF_AO	1	6	0 1	Answer mode Originate mode
CONF_MODE	2	5..0	0 1 2 3 4 5 6 7 8 9 A B C D Other	Automode Bell 103 Bell 212A V.21 V.23 V.22 V.22bis V.27ter V.29 V.17 V.32 V.32bis V.33 V.21 channel 2 Reserved

Parameters (continued)

Field	Byte	Pos.	Value	Definition
CONF_TXEQ	2	7..6	0 1 2 3	No transmit equalizer Transmit equalizer #1 (1/2 of M1020) Transmit equalizer #2 (1/2 of M1040) Reserved
CONF_QAM	3	0	0 1	QAM/DPSK only (Automode) FSK allowed (Automode)
CONF_TCM	3	1	0 1	Treillis coding not allowed (V.32 only) Treillis coding allowed (V.32bis, V.32)
CONF_SP0	3	7..2	xxxx01 xxxx0x xxx10x xx1x0x x1xx0x 1xxx0x	300 bps allowed (V.21, Bell 103) Reserved (must be set to 0) 1200 bps allowed (V.22, V.22bis, V.23, Bell 212A) 2400 bps allowed (V.22bis, V.27) 4800 bps allowed (V.32bis, V.32, V.29, V.27) 7200 bps allowed (V.32bis, V.29, V.17)
CONF_SP1	4	2..0	xx1 x1x 1xx	9600 bps allowed (V.32bis, V.32, V.29, V.17) 12000 bps allowed (V.32bis, V.33, V.17) 14400 bps allowed (V.32bis, V.33, V.17)

According with the 4 first bits of the CONF_OPER the ST75C502 is put into the following mode of operation.

CONF_OPER	Transmit	Receive	Number of tone detectors available
0000*	Tones	Tones	16
0010	Voice	Tones	16
0100	Tone	DTMF	4 (1)
0110	Voice	DTMF	4 (1)
1000	Tones	Voice	16
1010	Voice	Voice	16
1111	**Modem**	**Modem**	0 (2)
Other	Not allowed	Not allowed	-

Notes : **1.** 12 of the tone detectors are used by the DTMF detector.

2. When in Data Modem Mode, the number of tone detectors is set to 0. The user can set it up to 2 if the SERIAL link is used (instead of the parallel data mode). it is set to 2 in FAX Receive Mode, and 8 in V.21 channel 2 mode. To modify the number of tone detectors available, the user must overwrite the _NTDCELL DSP internal variable with a MW command (refer to "RAM mapping Application Note").

3. Unless otherwise required Tx equalizer #1 should be selected for better compromize on the general switched telephone network.

CR - Complex read

Opcode : 11

0	0	0	1	0	0	0	1

Synopsis

CR allows the reading of a complex parameter. The parameter specifies the parameter address (for the real part : the imaginary part is next location). CR returns the high byte value of both real and imaginary part of the addressed complex parameter.

Parameters

Field	Byte	Pos.	Value	Definition
CR_ADDR_L	1	7..0		Low byte of the 16-bit address
CR_ADDR_H	2	7..0		High byte of the 16-bit address

CSE - Clear error status

Opcode : 08

0	0	0	0	1	0	0	0

Synopsis

CSE is used to clear the ST75C502 error status SYSERR byte. It is also used as an acknowledge to the error condition handler.

Parameters

Field	Byte	Pos.	Value	Definition
ERR_MASK	1	7..0		Error mask . See report appendix for detailed meaning.

DEFT - Define arbitrary tone

Opcode : 0E

0	0	0	0	1	1	1	0

Synopsis

DEFT programs one of the four tone generator for arbitrary tone generation. The parameter is the frequency of the generated tone in Hertz between 0 and 3600 Hz (expressed in hexadecimal).

Parameters : Example 1000 Hz is represented by 03E8

Field	Byte	Pos.	Value	Definition
TONE_GEN_SL	1	1..0		Index of the tone generator (0..3)
TONE_FREQ_L	2	7..0		Low byte of the frequency
TONE_FREQ_H	3	7..0		High byte of the frequency (internally masked with 0F)
TONE_SCALE	4	7..0		Amplitude scaling factor (high byte) 3F gives the nominal amplitude

DOSR - Define optional status report

Opcode : 0A

0	0	0	0	1	0	1	0

Synopsis

DOSR specifies the address of the RAM variables to be monitored in the 3 locations STAOPT[0..2] of the dual port RAM. It also specifies the assignment within the 3 locations.

Parameters

Field	Byte	Pos.	Value	Definition
STA_OPT_ASS	1	2..0		Index of the STAOPT destination
STA_OPT_ADL	2	7..0		Low byte of source address
STA_OPT_ADH	3	3..0		High byte of source address
STA_OPT_HL	3	7	0 1	Select low byte of source Select high byte of source

DSIT - Define status interrupt

Opcode : 13

0	0	0	1	0	0	1	1

Synopsis

DSIT specifies the bit mask used with the **STATUS[0]** or **STATUS[1]** byte to generate an interrupt **IT4** to controller. Each time a bit change will append in the general status words, assuming the corresponding bit mask will be set, an interrupt will be generated.

Parameters

Field	Byte	Pos.	Value	Definition
STA_IT_MSK0	1	7..0		Status 0 Bit Mask pattern
STA_IT_MSK1	2	7..0		Status 1 Bit Mask pattern

Note : The default IT status is 0X3F for STATUS [0] and 0XFF for STATUS [1].

HSHK - Handshake

Opcode : 04

0	0	0	0	0	1	0	0

Synopsis

HSHK is used to command the ST75C502 to begin the handshake sequence processing. The progress of the handshake is reported to the control processor.

Parameters : non parametric command

IDT - Identify

Opcode : 14

0	0	0	1	0	1	0	0

Synopsis

IDT returns the ST75C502 Harware and Software release number. See Appendix B, paragraph I.2.2.

Parameters : non parametric command

Bits 15 to 12 represent the product identity number. For the ST75C502 this is 0
Bits 11 to 4 represent the product software release
Bits 3 to 0 represent the software sub release

INIT - Initialization

Opcode : 06

0	0	0	0	0	1	1	0

Synopsis

INIT forces the ST75C502 to reset all parameters to their default values and restart operations as after a Hardware Reset. It clears all the internal RAM, the DUAL RAM and restarts in Tone mode.

Parameters

Field	Byte	Pos.	Value	Definition
INIT_MODE	1	0	0	"Cold initialization" : initialize all variables and ST7544 chip. Maximum duration 500ms.
			1	"Warm initialization" : initialize only the variables. Maximum duration 10ms.

Notes : 1. This command makes a software reset of the ST75C502 and so cannot have the regular handshake protocol. It does not increment the COMACK, nor generate an Interrupt.

2. The INIT command does not affect the contains of the ITMASK and ITSRCR registers.

JSR - Call a low level subroutine

Opcode : 18

0	0	0	1	1	0	0	0

Synopsis

JSR allows execution of a part of the DSP firmware with specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	7..0		Low byte of the call address
C_ADDR_H	2	7..0		High byte of the call address
C_DATA_L	3	7..0		Low byte of the argument
C_DATA_H	4	7..0		High byte of the argument

MODC - Modify configuration

Opcode : 21

0	0	1	0	0	0	0	1

Synopsis

MODC allows modification of the configuration for special purposes. This command has no effect while in data mode, the parameters are just sampled when starting to transmit or receive.

Parameters

Field	Byte	Pos.	Value	Definition
MODC_SH	1	6	0* 1	Normal training sequence Short training (1) sequence
MODC_V22G	2	1..0	00* 01 10	No guard tone 1800Hz guard tone 550Hz guard tone
MODC_FPT	2	3..2	00* 10	No echo protection tone Long echo protection tone (180ms) (FAX only)
MODC_NOTA	2	4	0*	Answer mode : generate answer tone for handshake Originate mode : wait answer tone for handshake
			1	Answer mode : do not generate answer tone for handshake Originate mode : do not wait answer tone for handshake
MODC_NOSA	2	6	0* 1	Cut answer tone when receiving AA (V.32bis, V.32) Continue answer tone when receiving AA
MODC_NOQA	2	7	0* 1	Enable V.32bis handshake on quality Disable handshake on quality

Note1 : Short train sequence must be preceded by at least one normal training sequence.

MR - Memory read

Opcode : 10

0	0	0	1	0	0	0	0

Synopsis

MR allows the reading of a 16-bit parameter. The parameter specifies the parameter address.

Parameters

Field	Byte	Pos.	Value	Definition
MR_ADDR_L	1	7..0		Low byte of the 16-bit address
MR_ADDR_H	2	7..0		High byte of the 16-bit address

MW - Memory write

Opcode : 12

0	0	0	1	0	0	1	0

Synopsis

MW allows the writing of a 16-bit parameter. The parameter specifies the address, as well as the value, to be transferred.

Parameters

Field	Byte	Pos.	Value	Definition
MW_ADDR_L	1	7..0		Low byte of the 16-bit address
MW_ADDR_H	2	7..0		High byte of the 16-bit address
MW_VALUE_L	3	7..0		Low byte of the 16-bit value
MW_VALUE_H	4	7..0		High byte of the 16-bit value

PPR - Read parallel port

Opcode : 16

0	0	0	1	0	1	1	0

Synopsis

Read parallel port. The values of the 4-bit parallel port is read, whether the port is configured in input or in output.

Parameters : non parametric command

PPS - Parallel port set

Opcode : 15

0	0	0	1	0	1	0	1

Synopsis

Configure parallel port. Each of the 4 pins of the parallel port can be either programmed for input or for output.

Parameters

Field	Byte	Pos.	Value	Definition
PP_IO0	1	0	0* 1	Pin 0 programmed as input Pin 0 programmed as output
PP_IO1	1	1	0* 1	Pin 1 programmed as input Pin 1 programmed as output
PP_IO2	1	2	0* 1	Pin 2 programmed as input Pin 2 programmed as output
PP_IO3	1	3	0 1*	Pin 3 programmed as input Pin 3 programmed as output

Note : Pin 3 is reserved for MAFE control and therefore must be programmed as an output.

PPW - Parallel port write

Opcode : 17

0	0	0	1	0	1	1	1

Synopsis

Write to the parallel port. This operation will be effective only if the bits are programmed as outputs.

Parameters

Field	Byte	Pos.	Value	Definition
PP_VAL0	1	0		Pin 0 logical value
PP_VAL1	1	1		Pin 1 logical value
PP_VAL2	1	2		Pin 2 logical value
PP_VAL3	1	3	1	Pin 3 logical value must be set to 1

RTRA - Retrain

Opcode : 05

0	0	0	0	0	1	0	1

Synopsis

RTRA is used to force the ST75C502 to initiate a retrain sequence on the channel. The parameter determines the target speed for the retrain.

Parameters

Field	Byte	Pos.	Value	Definition
RTRA_NEGO	1	0	0 1	Retrain (V.22bis, V.32, V.32bis) Rate Negotiation (V.22bis, V.32bis)
RTRA_NEGO	1	1	1 0	Treillis coding enabled Treillis coding not enabled
RTRA_1200	1	4	0 1	1200 bps speed not allowed 1200 bps speed allowed
RTRA_2400	1	5	0 1	2400 bps speed not allowed 2400 bps speed allowed
RTRA_4800	1	6	0 1	4800 bps speed not allowed 4800 bps speed allowed
RTRA_7200	1	7	0 1	7200 bps speed not allowed 7200 bps speed allowed
RTRA_9600	2	0	0 1	9600 bps speed not allowed 9600 bps speed allowed
RTRA_12000	2	1	0 1	12000 bps speed not allowed 12000 bps speed allowed
RTRA_14400	2	2	0 1	14400 bps speed not allowed 14400 bps speed allowed

SERIAL - Select serial or parallel mode

Opcode : 07

0	0	0	0	0	1	1	1

Synopsis

SERIAL defines the data path, i.e. either serial or parallel.

Parameters

Field	Byte	Pos.	Value	Definition
TX_SDATA	1	0	0* 1	Use serial link for Tx data Use parallel link for Tx data
RX_SDATA	1	1	0* 1	Use only serial link for Rx data Use also parallel link for Rx data

Note : The received bits always go to output pin DX2, even when the Rx_SDATA bit is set.

SETGN - Set output gain

Opcode : 02

0	0	0	0	0	0	1	0

Synopsis

SETGN is a command which sets the scaling factor of the transmit samples. It is used for setting the output level or for setting the level of the tone generators. The gain value is given in the form of a 2's complement 16-bit value.

Parameters

Field	Byte	Pos.	Value	Definition
GAIN_L	1	7..0	range FF*	Low byte of the 16-bit gain value
GAIN_H	2	7..0	range 7F*	Hight byte of the 16-bit gain value

Example :

Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)
0	7FFF	-5	47FA	-10	287A
-1	7214	-6	4026	-11	2413
-2	65AC	-7	392C	-12	2026
-3	5A9D	-8	32F5	-13	1CA7
-4	50C3	-9	2D6A	-14	198A

SLEEP - Turn to low power mode

Opcode : 03

0	0	0	0	0	0	1	1

Synopsis

SLEEP is used to force the ST75C502 to turn to low power mode.

Parameters : non parametric command

Note : When receiving this command the ST75C502 will stop processing and so cannot have the regular handshake protocol It does not increment the COMACK, nor generate an Interrupt.

STOP - FAX stop transmitter

Opcode : 25

0	0	1	0	0	1	0	1

Synopsis

STOP is used, in FAX modes, to force the ST75C502 to turn-off the transmitter in accordance with the corresponding ITU-T V.33 / V.17 / V.29 / V.27ter / V.21 channel 2 recommendations.

Parameters : non parametric command

Note : When receiving this command the ST75C502 will stop sending regular data. In parallel mode this command must be preceded by a **XMIT** stop command. After receiving the **STOP** command the ST75C502 will wait until all the transmit buffers are sent commencing with the stop sequence.

SYNC - FAX synchronize the receiver

Opcode : 26

0	0	1	0	0	1	1	0

Synopsis

SYNC is used, in FAX modes, to force the ST75C502 to start/stop the receiver in accordance with the corresponding ITU-T V.33 / V.17 / V.29 / V.27ter / V.21 channel 2 recommendations.

As soon as the ST75C502 receives the **SYNC** start command it sets its receiver to detect the FAX synchronization signal.

This commdand is the equivalent **HSHK** command for the receiver.

Parameters

Field	Byte	Pos.	Value	Definition
RX_SYNC	1	0	0* 1	Stop receiver Start receiver synchronization

TDRC - Tone detector read coefficient

Opcode : 1A

0	0	0	1	1	0	1	0

Synopsis

TDRC read one coefficient of the selected tone detector cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_C_ADDR	2	7..0	0..B 10 20 other	Biquad coefficient Energy coefficient Static level Reserved

The command answer is : low byte of coefficient followed by high byte of coefficient.

TDRW - Tone detector read wiring

Opcode : 1B

0	0	0	1	1	0	1	1

Synopsis

TDRW read wiring of the selected tone detector cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_W_ADDR	2	0	0 1 other	Biquad and energy input Comparator inputs Reserved

The command answer is :

a) if TD_W_ADDR = 0 :
   - first byte is the node number of signal connected to biquadratic filter input,
   - second byte is the node number of the signal connected to the energy estimator input.

b) if TD_W_ADDR = 1 :
   - first byte is the node number of signal connected to comparator negative input,
   - second byte is the node number of the signal connected to the comparator positive input.

TDWC - Tone detector write coefficient

Opcode : 1C

0	0	0	1	1	1	0	0

Synopsis

TDWC write one coefficient of the selected tone detector cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_C_ADDR	2	7..0	0..B 10 20	Biquad coefficient Energy coefficient Static level
TD_COEFL	3	7..0		Low byte of coefficient
TD_COEFH	4	7..0		High byte of coefficient

TDWW - Tone detector write wiring

Opcode : 1D

0	0	0	1	1	1	0	1

Synopsis

TDWW write wiring of the selected tone detector cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_W_ADDR	2	0	0 1	Biquad and energy input Comparator inputs

if TD_W_ADDR = 0 (select biquad and energy inputs)

Field	Byte	Pos.	Value	Definition
TD_W_ERN	3		0..3F	Energy estimator signal input
TD_W_BIQ	4		0..3F	Biquad filter signal input

if TD_W_ADDR = 1 (select comparator inputs)

Field	Byte	Pos.	Value	Definition
TD_W_CN	3		0..3F	Negative comparator signal input
TD_W_CP	4		0..3F	Positive comparator signal input

TDZ - Tone detector clear cell

Opcode : 1E

0	0	0	1	1	1	1	0

Synopsis

TDZ clears all internal variables of one Tone detector cell including filter local variables and energy estimator. This command must be sent after changing coefficients of a cell to avoid instability.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number

TGEN - Enable/disable tone generators

Opcode : 0D

0	0	0	0	1	1	0	1

Synopsis

TGEN causes the ST75C502 to enable or disable the four tone generators.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_0_ENA	1	0	0* 1	Generator #0 disabled Generator #0 enabled
TONE_1_ENA	1	1	0* 1	Generator #1 disabled Generator #1 enabled
TONE_2_ENA	1	2	0* 1	Generator #2 disabled Generator #2 enabled
TONE_3_ENA	1	3	0* 1	Generator #3 disabled Generator #3 enabled

TONE - Predefined tones

Opcode : 0C

0	0	0	0	1	1	0	0

Synopsis

TONE programs the tone generators for the predefined tones. The tone generators #0 and eventually #1 are reprogrammed with this command. Eventualy the tone generator #0 and #1 are enabled. Using an argument not in the following table will disable tone generator #0 and #1.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_SELECT	1	5..0	0	DTMF 0 (941 & 1336Hz)
			1	DTMF 1 (697 & 1209Hz)
			2	DTMF 2 (697 & 1336Hz)
			3	DTMF 3 (697 & 1477Hz)
			4	DTMF 4 (770 & 1209Hz)
			5	DTMF 5 (770 & 1336Hz)
			6	DTMF 6 (770 & 1477Hz)
			7	DTMF 7 (852 & 1209Hz)
			8	DTMF 8 (852 & 1336Hz)
			9	DTMF 9 (852 & 1477Hz)
			A	DTMF A (697 & 1633Hz)
			B	DTMF B (770 & 1633Hz)
			C	DTMF C (852 & 1633Hz)
			D	DTMF D (941 & 1633Hz)
			E	DTMF * (941 & 1209Hz)
			F	DTMF # (941 & 1477Hz)
			10	Answer Tone (2100Hz)
			11	Tone (1650Hz)
			12	Answer Tone (2225Hz)
			13	Tone (1300Hz)

V22L2 - V22 loop 2 generator/detector

Opcode : 24

0	0	1	0	0	1	0	0

Synopsis

V22L2 selects the transmission and detection of V.22/V.22bis patterns required for remote digital loop back as defined in the ITU-T specification. The STA_V22L bit in the STA_LOOP optional status word will follow the detection of the receiver setting. This command must only be used in V.22 or V.22bis modes.

Note that the STA_V22A bit (alternate "1010" or "0101") in the STA_LOOP is always active.

Parameters

Field	Byte	Pos.	Value	Definition
V22L2_TX	1	1..0	00*	Data mode
			01	Transmit unscrambled "1"
			10	Transmit scrambled "1"
			11	Transmit scrambled "1010"
V22L2_RX	2	0	0*	Detect unscrambled "1"
			1	Detect scrambled "1"

V54 - Generator/detector

Opcode : 23

0	0	1	0	0	0	1	1

Synopsis

V.54 selects the transmission and detection of V.54 patterns required for remote digital loop back as defined in the ITU-T specification. The STA_V54D bit in the STA_LOOP optional status word will follow the detection of the receiver setting. This command must only be used in V.32 or V.32bis modes.

When the transmit generator completes the required pattern it will continue to send the same sequence and set the STA_V54E bit in the STA_LOOP.

Parameters

Field	Byte	Pos.	Value	Definition
V54_TX	1	1..0	00* 01 10 11	Data mode Transmit 2048 V54 scrambled "0" Transmit 1948 V54 scrambled "1" Transmit 8192 V54 scrambled "1"
V54_RX	2	1..0	00* 01 10 11	No V54 detection Reserved Detect 256 V54 scrambled "0" Detect 256 V54 scrambled "1"

XMIT - Start/stop transmission

Opcode : 01

0	0	0	0	0	0	0	1

Synopsis

XMIT enables or disables the transmission of the data according to the selected mode (serial or parallel).

Parameters

Field	Byte	Pos.	Value	Definition
TX_START	1	0	0* 1	Stop transmission Start transmission

WMR - Write MAFE Register

Opcode : 11

0	0	0	1	0	0	0	1

Synopsis

WMR allows the writing of a 8-bit parameter into one of the ST7544 MAFE chip register.

Parameters

Field	Byte	Pos.	Value	Definition
MWR_DATA	1	7..0		Byte od data
MWR_ADDR	2	1..0		Byte of the 2-bit address
MWR_RXTX	3	7..0	0 0	Acess Tx Register Access Rx Register

This command must be used to lock the Transmit clock on an external clock or the received clock :

WMR D0 **02** **00** Tx Clock locked on TxSCLK input Pin.
WMR F0 02 **00** Tx Clock locked on Rx Clock.
WMR C0 **02** **00** Tx Clock free running

APPENDIX B : STATUS DESCRIPTION

This appendix is dedicated to the ST75C502 reporting features. In the following sections are explained the command acknowledge process and the report and status definitions.

I - COMMAND ACKNOWLEDGE AND REPORT

I.1 - Command Acknowledge Process

The ST75C502 features an acknowledge process based on a counter COMACK. On power-on reset, this counter's value is set to 0. Each time a command is executed, the acknowledge counter COMACK is incremented. This allows a precise monitoring of the command entered and avoids command collision.

The acknowledge counter is incremented as soon as the command has been properly executed. Furthermore, the ST75C502 resets the value of the COMSYS register. The interruption IT6 is raised just after the counter is incremented.

In the case of a memory reading command (CR, MR or PPR), the process is slightly different. The command entered is executed, the report area is then filled and the acknowledge counter is incremented afterwards. This insures that the controller reads the value corresponding to its request. Figure B1 gives a flowchart of the command acknowledge process.

I.2 - Reports Specification

The report section of the Dual Port RAM is dedicated to memory reading. In response to a CR, MR, IDT or PPR command, the value to be read is transferred to the Report registers COMREP[0..1].

I.2.1 - CR Command

Issuing a CR command causes the ST75C502 to dump a specific memory location in complex mode. This instruction is particularly usefull for equalizer state analysis or for software eye-pattern display. The report area has this meaning :

RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0	COMREP[0]

IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	COMREP[1]

RP7..RP0 is the MSB part of the 16-bit value of the real part and IP7..IP0 is the MSB part of the imaginary part. The CR command insures that the real and imaginary parts of the desired complex value are sampled internally at the same time. The address given in the parameter field of CR is the address of the real part.

I.2.2 - MR/TDRC/IDT/TDRW Commands

The report issued by the MR/TDRC command is followings the same rules as the CR. The report meaning is :

D7	D6	D5	D4	D3	D2	D1	D0	COMREP[0]

D15	D14	D13	D12	D11	D10	D9	D8	COMREP[1]

D15..D0 is the 16-bit value required by the MR/TDRC command.

In the case of IDT, D15..D12 contains the product identification (0 for ST75C502), D11..D8 contains the hardware revision identification and D7..D0 contains the software revision identification.

I.2.3 - PPR Command

The PPR command issues the following report :

0	0	0	0	PP3	PP2	PP1	PP0	COMREP[0]

PP0..PP3 are the values read on the 4 pins of the parallel port. The result doesn't take into acccount the fact that those pins are input or output pins.

II - STATUS

II.1 - Modem Status

The status of the ST75C502 is divided into 4 fields :

- the error status byte SYSERR that provides information about error. This status can trigger an IT0 interrupt,
- the general status byte STATUS[0] and STATUS[1] that contains all the modem signals. These status bytes can trigger an IT4 interrupt,
- the quality status STAQUA, that contains the quality of the received transmission,
- the optional status bytes STAOP[0], STAOP[1] and STAOP[2], that contains additional information regarding the ST75C502 operating mode. This default information can be changed to monitor any internal variables using the DOSR command.

All these infomations are updated on a baud basis :

Mode	Baud Rate (Hz) (2)
Tone, DTMF, Voice	2400
V.32bis, V.32	2400
V.22bis, V.22, Bell 212A	2400
V.21, Bell 103	2400
V.23	2400
V.27ter 2400bps	1200
V.27ter 4800bps	1600 (1)
V.29	2400
V.17, V.23	2400
V.21 channel 2	2400

Notes : 1. The tone detectors outputs are update 800 times by seconds.
2. This baud rate defines also, the maximum command rate. Each baud time the ST75C502 looks at the COMSYS location (Address $00) to see if a command have been send by the host processor. If the content of this location is different from zero the ST75C502 execute the command.

Starting at the address $08 the status area have the following format :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$08	SYSERR	ERR_RTK	-	-	ERR_IPRM	ERR_IOCD	ERR_SYM	ERR_RX	ERR_TX
$09	STATUS0	STA_109F	STA_CLR	STA_RNEG	STA_RTRN STA_HR	STA_AT	STA_CCITT	STA_TIM	STA_H
$0A	STATUS1	HSHK_PHA							
$0B	STAQUA	Quality							
$0C	STAOP0	Depend on operating mode (see below)							
$0D	STAOP1								
$0E	STAOP2								

II.2 - Error Status

The error status is changed each time an error occurs. When the ST75C502 signals an error by setting one of the SYSERR bit, it generate an interrupt IT0. These bits can only be cleared by the host-controler using the CSE command.
The meaning of the different bits of the SYSERR byte is discribed below :

SYSERR		
Field	**Pos.**	**Meaning when set**
ERR_TX	0	Transmit buffer underflow. Loss of synchronisation between the host and ST75C502 transmit data buffer managment
ERR_RX	1	Receive buffer overflow. Loss of synchronisation between the host and ST75C502 receive data buffer managment
ERR_SYM	2	Symbol buffer synchronization error (V.32, V.32bis)
ERR_IOCD	3	Incorrect CCI command
ERR_IPRM	4	Incorrect parameter for the CCI command
ERR_RTK	7	Real time kernel error. ST75C502 not able to perform all its tasks within the Baud period (transmit or receive samples lost)

II.3 - Modem General Status

The modem general status word is composed of two bytes STATUS[0] and STATUS[1]. Any bit change can generate an IT4 interrupt. Using the DSIT command allows the selection of the corresponding bit that will generate an interrupt each time they will change. The default pattern is $3F for STATUS[0] and $FF for STATUS[1]. The different bits have the following meaning :

STATUS[0]		
Field	**Pos.**	**Meaning when set**
STA_109	0	ITU-T circuit 109 (carrier detect). Indicates that valid data are received. When 0 the output data RxD are clamped to constant mark. Valid only in modem mode.
STA_107	1	ITU-T circuit 107 (data set ready). Valid only in modem mode.
STA_106	2	ITU-T circuit 106 (clear to send). Indicates that the training sequence has been completed and that any data at TxD pin (serial mode) or in the transmit buffer (parallel mode) will be transmitted. Valid only in modem mode.
STA_RING	3	Ring detected. A ring signal (from 15Hz to 68Hz) is present at the RING pin. Valid only in tones modes. The precise frequency can be read in the optional status byte STAOP2. The detection time is 1 period of the ring signal. The detection lost time is 20ms after the last transition on the ring signal.
STA_CPT0	4	Call progress tone detector #0. Low pass filter 650Hz. Valid only in tones modes.
STA_CPT1	5	Call progress tone detector #1. High pass filter 600Hz. Valid only in tones modes.
STA_CPT10	6	Signal in filter #0 is higher than #1. Valid only in tones modes.
STA_109F	7	Fast carrier detect. Valid only in FAX modem mode.

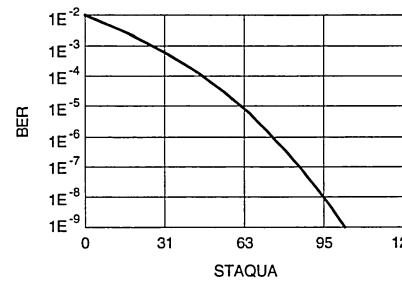
STATUS[1]		
Field	**Pos.**	**Meaning when set**
STA_H	0	Transmit synchronization in progress. Valid only in modem mode.
STA_TIM	1	Handshake timeout. Valid only in data modem mode.
STA_CCITT	2	Originate mode or tone : 2100Hz versus 2225Hz detected Answer mode : 1800Hz (AA signal) versus 2225Hz detected
STA_AT	3	Answer tone detect, either 2100Hz (or 1800Hz) or 2225Hz. This bit allows the sampling of the STA_CCITT bit.
STA_RTRN **STA_HR**	4	V.32bis, V.32, V.22bis : remote retrain detected Fax mode (including V.21 channel 2) : receiver synchronization in progress
STA_RNEG	5	V.32bis, V.32, V.22bis : remote rate negociation detected
STA_CLR	6	V.32bis, V.32 : cleardown detected
STA_DTMF	7	DTMF digit detect. The digit itself is available in the optional status byte STAOP2. Valid only in DTMF receive mode.

II.4 - Quality Status

The quality byte STAQUA monitors an evaluation of the line quality. It is updated once per baud and its value ranges from 127 (perfect quality) to 0 (terrible quality).

This value is automatically adjusted according to the current receiving mode (not valid in FSK modes).

Refer to the following chart to convert the value into its bit error rate equivalence.



75C50219 EPS

II.5 - Optional Status

According to the operating mode of the ST75C502 the optional status is displaying different informations.

The optional status are automatically reprogrammed after each CONF command with the address of the variables to monitor according with the operating mode selected (CONF_OPER). After the CONF command the user must overwrite this default programming by using the DOSR command. In order to change the default setup ; please refer to the "RAM Mapping ApplicationNlote" to obtain the addresses of the DSP internal variables.

II.5.1 - Default Optional Status in Tone Mode

While in tone mode the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	TDT7	TDT6	TDT5	TDT4	TDT3	TDT2	TDT1	TDT0
$0D	STAOP1	TDT15	TDT14	TDT13	TDT12	TDT11	TDT10	TDT9	TDT8
$0E	STAOP2	RING_PERIOD (1)							

Notes : 1. RING_PERIOD is valid when the bit 3 of the STATUS[0] (STA_RING) goes high). This value is updated at each falling edge of the RING signal. The RING_PERIOD value must be divided by 2400 to obtain the period in seconds.
2. TDTx is the output of the tone detector x.

II.5.2 - Default Optional Status in DTMF Receiver Mode

While in DTMF receiver mode the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	TDT7 (1)	TDT6 (1)	TDT5 (1)	TDT4 (1)	TDT3	TDT2	TDT1	TDT0
$0D	STAOP1	TDT15 (1)	TDT14 (1)	TDT13 (1)	TDT12 (1)	TDT11 (1)	TDT10 (1)	TDT9 (1)	TDT8 (1)
$0E	STAOP2	DTMF_DIGIT (2)							

Notes : 1. These cells are used by the DTMF detector.
2. DTMF_DIGIT is valid when the bit 7 of STATUS[1] (STA_DTMF) goes high. This value remains unchanged until a new DTMF digit is detected.

II.5.3 - Default Optional Status in Data Modem Mode

While in the DATA modem mode (V.32bis, V.32, V.22bis, V.22, V.23, V.21, Bell 212A or Bell 103) the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	NEG_MODE	-	-	-	NEG_SPEED				NEG_PRG
$0D	LOOP_STA	-	-	-	-	STA_V22L	STA_V22A	STA_V54E	STA_V54D
$0E	HSHK_PHA	HSHK_PHA							

Where the NEG_MODE byte indicates the issue of the rate negotiation. Its meaning is :

Field	Position	Value	Description
NEG_PRG	0	0 1	Negotiation in progress Negotiation completed
NEG_SPEED	4..1	0 1 2 3 4 5 6 7 8	Reserved Reserved Negociated speed is 1200 bps Negociated speed is 2400 bps Negociated speed is 4800 bps Negociated speed is 7200 bps Negociated speed is 9600 bps Negociated speed is 12000 bps Negociated speed is 14400 bps

The LOOP_STA byte provides information about the loop status, for V.22bis and V.54 loops. This status byte must be used in accordance with the V22L2 and V54 commands. Its meaning is :

STA_LOOP		
Field	**Pos.**	**Meaning when set**
STA_V54D	0	V.54 pattern detected : when set 256 bit of the V.54 pattern has been detected
STA_V54E	1	V.54 pattern completed : when set the transmit V.54 pattern has been completely send
STA_V22A	2	V.22bis alternate "0101" or "1010" pattern detected (typicaly 53ms)
STA_V22L	3	V.22bis loop pattern detected (typicaly 13ms)
Reserved	7..4	Reserved

The HSHK_PHA byte provides information about the handshake phase state (automode, V.32bis, V.32, V.22bis, V.22, Bell 212A). This is a number between 0 and 255 that is associated with some handshake events. Refer to the "RAM mapping application note" to obtain the event equivalence table.

II.5.4 - Default Optional Status in FAX Modem Mode

While in the FAX modem mode (V.17, V.33, V.29, V.27 or V.21 channel 2) the format of the STAOP word is as follows :

Add.	**Name**	**Bit**							
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0C	NEG_MODE	-	-	-	NEG_SPEED (2)				NEG_PRG (1)
$0D	STAOP1	Not used							
$0E	HSHK_PHA	PNSUCs	PRDETs	PNDETs	SCR1s	PRs	PNs	P2s	P1s

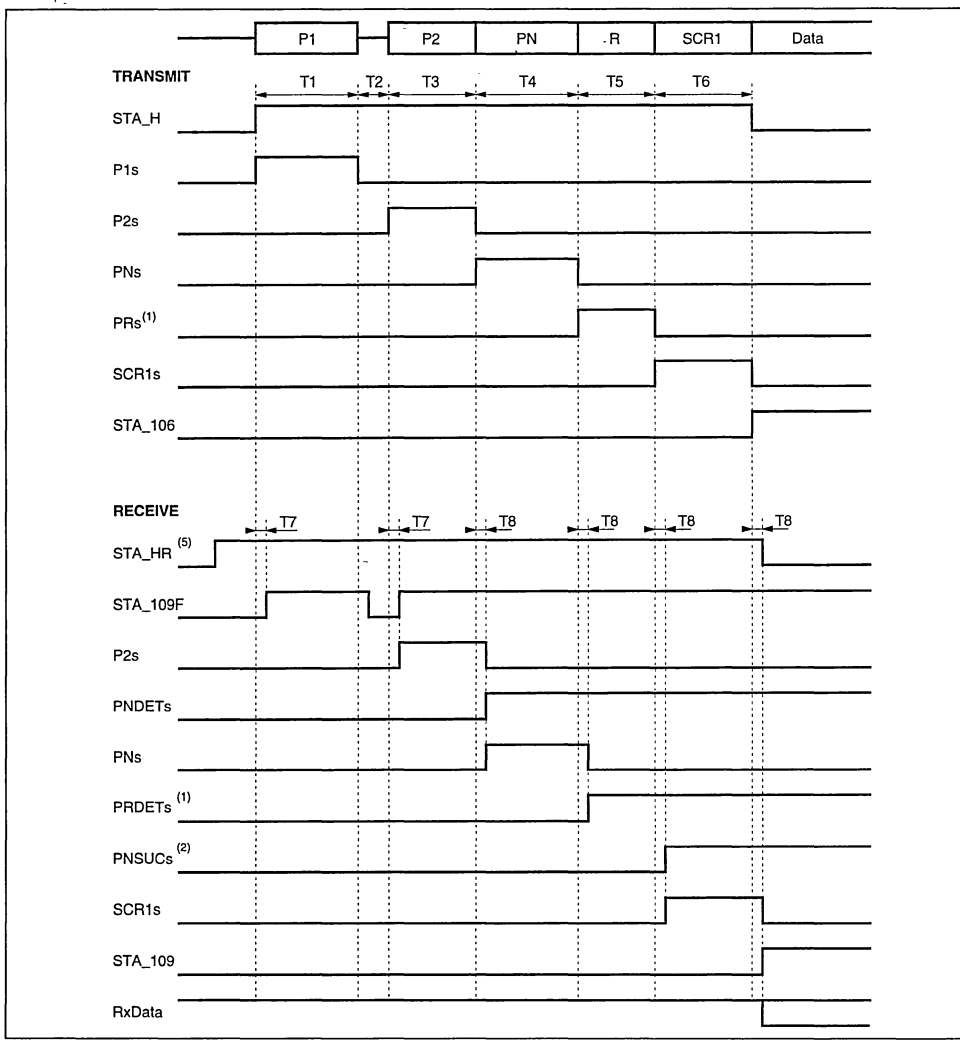
Notes : 1. SPVAL is active in V.33 receiver only at the same time as the rising transition of the SCR1s signal. Went SPVAL is set, it indicates that the SPEED bits contain the data speed information.

2. SPEED is valid in V.33 receiver only. It can have 2 values, after the SCR1s signal goes high : 1000 for 14400bps and 0111 for 12000bps.

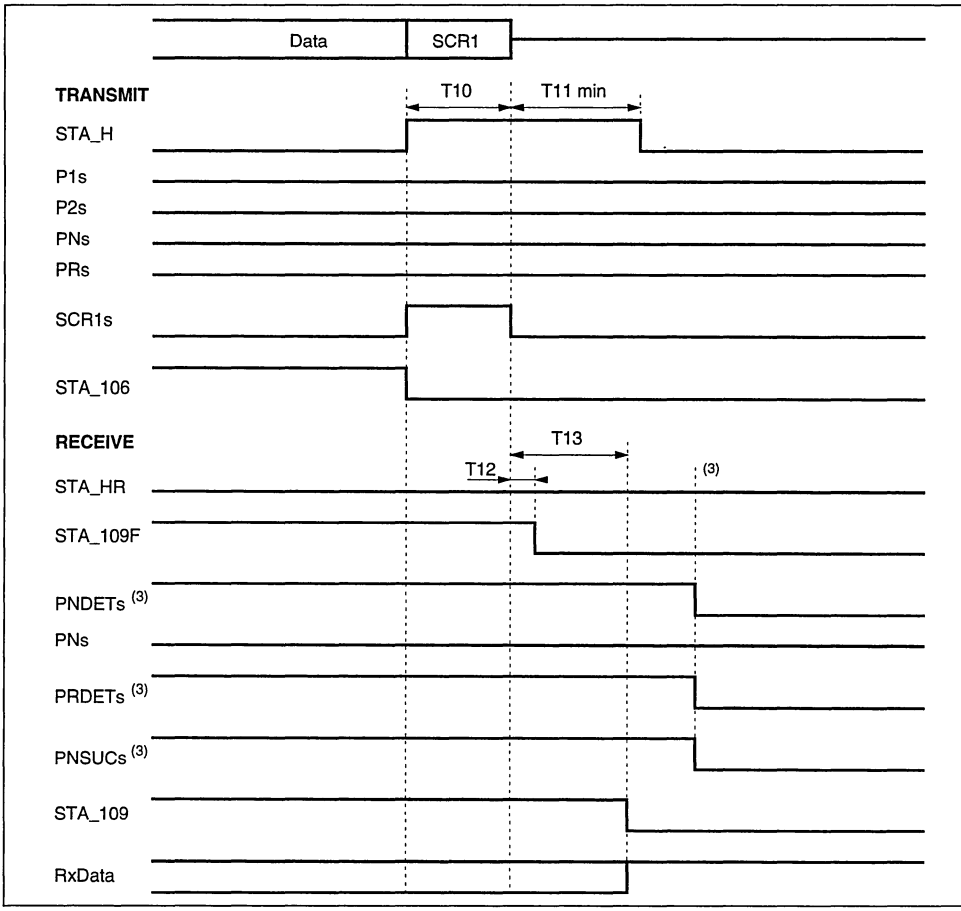
3. The HSHK_PHA bit reflects the progression of the synchronization.
It has the following meaning :

Name	**Position**	**Description**	**Tx**	**Rx**
P1s	0	Unmodulated carrier sequence. Optional, used for echo protection.	X	
P2s	1	Continuous 180° phase reversal sequence	X	X
PNs	2	Equalizer trainning sequence	X	X
PRs	3	V.33 and V.17 rate sequence	X	
SCR1s	4	Continuous scrambled 1 sequence	X	X
PNDETs	5	Turned on after PN sequence detection		X
PRDETs	6	Turned on after PR sequence detection (V.33 and V.17 only)		X
PNSUCs	7	Turned on after succesfull training of the receive equalizer. When on at the end of the synchronization, the transmition BER is statisticaly bellow 10ppm.		X

With the following timing :



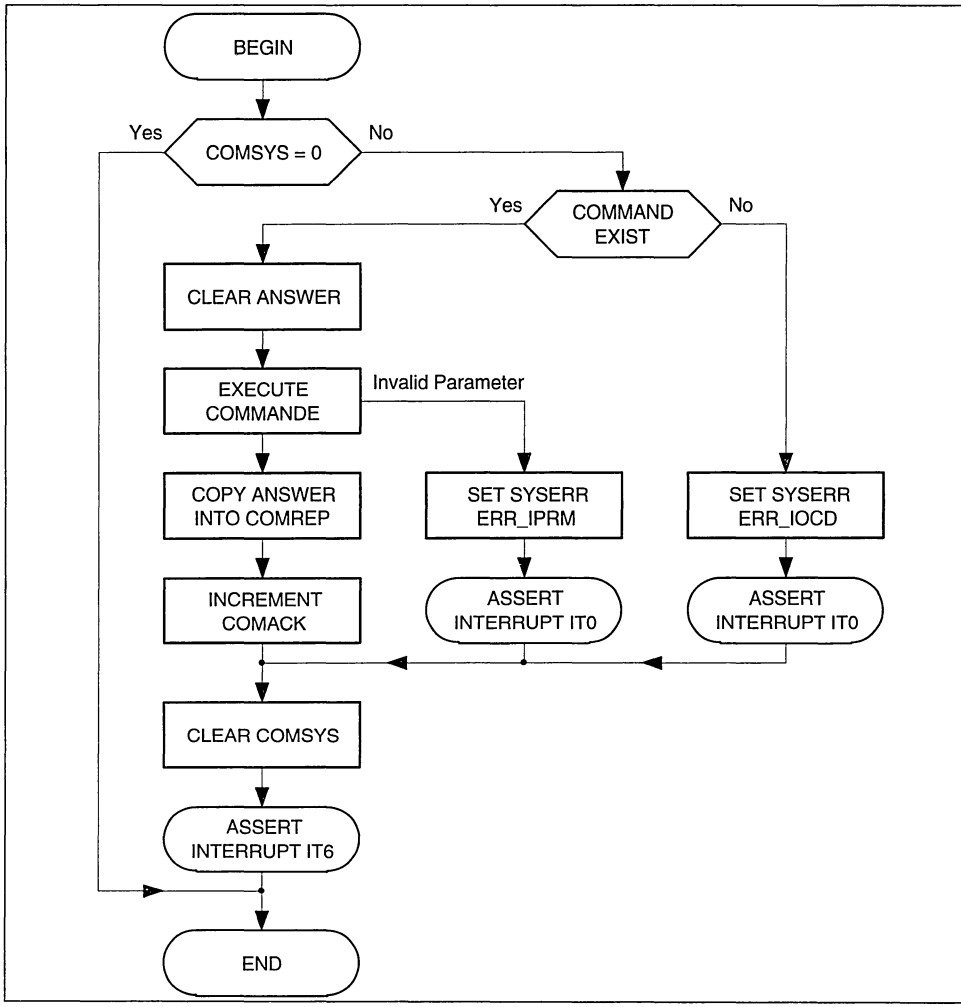
Mode	T1 (4)	T2	T3	T4	T5	T6	T7	T8	Unit
V.17	192	22	107	1240	27	20	5	7	ms
V.17 short	192	22	107	16	0	20	5	7	ms
V.29	192	22	53	160	0	20	5	7	ms
V.29 short	192	22	41	26	0	8	5	7	ms
V.27 4800	192	22	31	670	0	5	5	7	ms
V.27 4800 short	192	22	9	36	0	5	5	7	ms
V.27 2400	192	22	42	895	0	7	6	7	ms
V.27 2400 short	192	22	12	48	0	7	6	7	ms



Mode	T10	T11	T12	T13	Unit
V.17	13	20	8	25	ms
V.17 short	13	20	8	25	ms
V.29	13	20	8	25	ms
V.29 short	13	20	8	25	ms
V.27 4800	20	30	8	25	ms
V.27 4800 short	20	30	8	25	ms
V.27 2400	27	40	8	25	ms
V.27 2400 short	27	40	8	25	ms

Notes : 1. In the case of V.29 or V.27, PRs and PRDETs bits are not active.
2. PNSUCs indicates the quality of the Rx signal that will give a ber of approximation of 10^{-5}. PNSUCs is sampled at the end of sequence PN (R for V.17). The quality is resampled and PNSUCs is recalculated 256 Bauds (106ms for V.17, V.29 ; 160ms for V.27 4800bps and 212ms for V.27 2400bps) after the falling edge of SCR1s.
3. After sending the command SYNC0, all bits are reset.
4. When using long echo protection tone, otherwise 0.
5. After sending the command SYNC1, this bit is set.

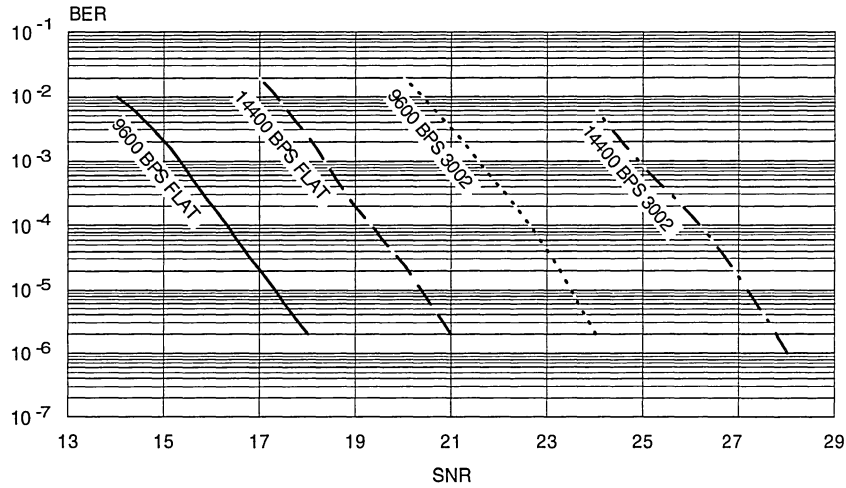
Figure B1 : Command Acknoledge



APPENDIX C : TYPICAL BER PERFORMANCES

This appendix shows the typical Bit Error Rate curves obtained on lines Flat and US3002, using a TAS® Series II equipment and a V.56 AGC. Sample size is 10^7 bit.

Figure C1 : Typical V32bis BER Performances



APPENDIX D : DEFAULT CALL PROGRESS TONE DETECTORS

Figure D1 : Call Progress Tone Detector Band 0

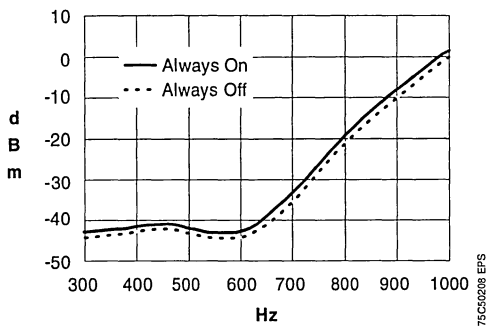
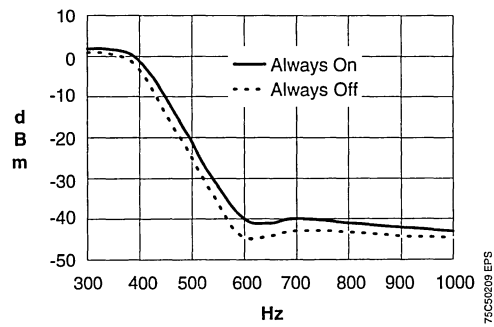
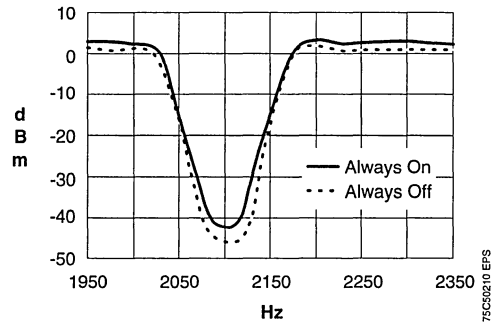


Figure D2 : Call Progress Tone Detector Band 1



APPENDIX E : DEFAULT ANSWER TONE DETECTORS

Figure E1 : 2100Hz Answer Tone Detector



APPENDIX F : ELECTRICAL SCHEMATICS

This appendix contains the following schematics :
- example of hybrid line design,
- chip interconnect circuitry required in the case of the minimal configuration.

Figure F1 : Typical Line Interface

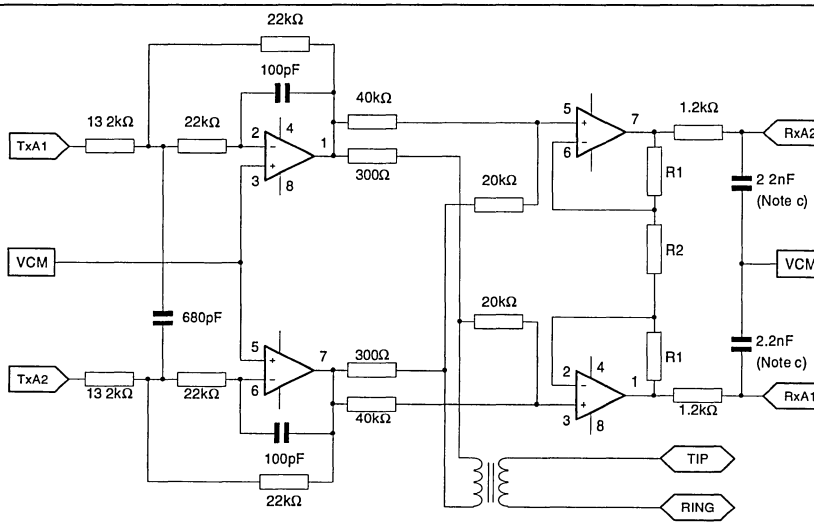
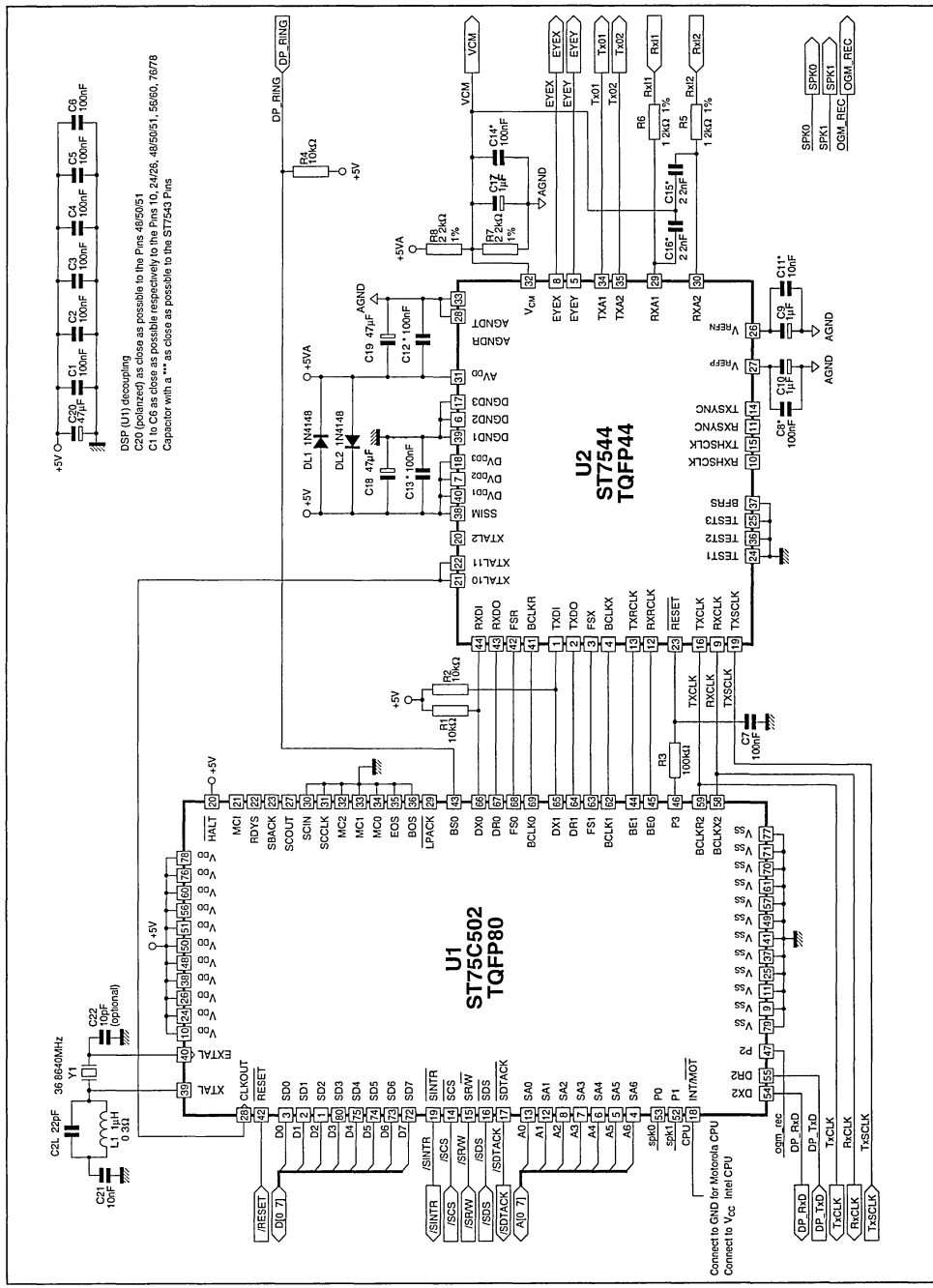


Figure F2


U1
ST75C502
TQFP80
U2
ST7544
TQFP44
DSP (U1) decoupling
C20 (polarized) as close as possible to the Pins 48/50/51
C1 to C6 as close as possible respectively to the Pins 10, 24/26, 48/50/51, 56/60, 76/78
Capacitor with a *** as close as possible to the ST7543 Pins
Connect to GND for Motorola CPU
Connect to VCC Intel CPU
DP_RING
VCM
AGND
+5V
+5VA
EYEX
EYEY
TxO1
TxO2
RxI1
RxI2
SPK0
SPK1
OGM_REC
DP_RxD
DP_TxD
TxCLK
RxCLK
TxSCLK
/RESET
/SINTR
/SCS
/SRW
/SDS
/SDTACK
75C50222 EPS

APPENDIX G

I - TONE DETECTORS

I.1 - Overview

The general purpose TS75C50/51/52 tone detector block is a powerful module that covers a lot of applications :

- call progress tone detection, fully programmable for all different countries,
- DTMF detection,
- high level handshake for all main modem standards,
- FAX, voice, data automatic detection,
- call waiting detection, while in voice or data mode.

I.2 - Description

The tone detector block is a set of 16 identical cells. Each cell is composed of a double biquadratic filter, a power estimator section, a static level and a level comparator.

Each biquadratic filter, power estimator and static level can be programmed using a complete set of commands (TDRC, TDRW, TDWC, TDWW, TDZ).

The wiring between the different cells can be defined by the user using the command allowing a wide range of applications.

The 16 comparator outputs give, on a baud basis, the information into a two 8 bits word TONEDET0 (for cells number 0 to 7) and TONEDET1 (for cells number 8 to F). These TONEDET variables can be accessed using a MR command or, more easily, monitored on a baud basis using the DOSR command.

While in FAX half duplex receive IDLE mode a set of 8 cells allows to implement customized handshake short sequences.

I.2.1 - Biquadratic Filters (see Figure G1)

Each biquadratic filter is a double regular section that can perform any transfer function with 4 poles and 4 zeros. This routine is run on a sample basis.

The corresponding transfer function is :

$$\frac{Out}{Input} = C0 \cdot \frac{C5 + 2 \cdot C3 \cdot z^{-1} + 2 \cdot C4 \cdot z^{-2}}{1 - 2 \cdot C1 \cdot z^{-1} - 2 \cdot C2 \cdot z^{-2}} \cdot C6 \cdot \frac{CB + 2 \cdot C9 \cdot z^{-1} + 2 \cdot CA \cdot z^{-2}}{1 - 2 \cdot C7 \cdot z^{-1} - 2 \cdot C8 \cdot z^{-2}} \cdot z^{-1}$$

Note : All coefficients are coded on 16 bits 2's complement in the range +1, -1 (Q15). To avoid the possibility of overflow the user must check that the internal node must not be higher that 0.5 (in Q15 representation).

I.2.2 - Power Estimation (see Figure G2)

The power estimation cell is needed to measure the amplitude of the different tones. It is run on a sample basis.

The corresponding transfer function is :

$$Out = |Input| \cdot z^{-1} \cdot \frac{P1}{1 - (1 - P1) \cdot z^{-1}}$$

Note : To deal with the high dynamic range of the analog front end, the computation loop of the power estimation is run with 32 bits accuracy. The output and input of that cell are however 16 bit words (Q15).

Figure G1 : Biquadratic IIR Filter

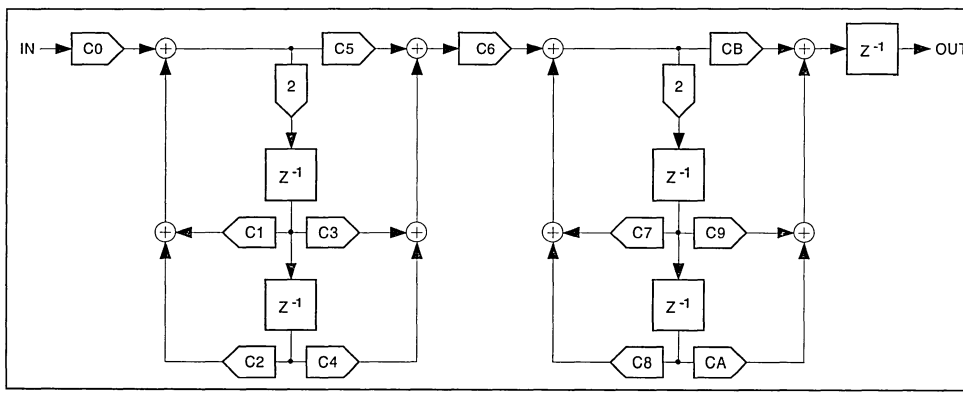
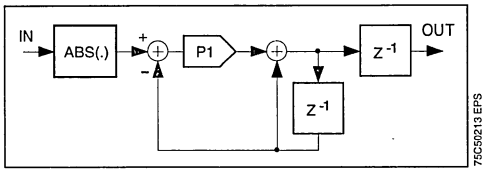


Figure G2 : Power Estimator



I.2.3 - Static Level

A single threshold level is associated with each cell. It can be use to compare the output of a power estimation with an absolute value.

I.2.4 - Comparator

The comparator computes on a baud basis, the difference of the signal on its positive input and its negative input. If the result is higher that zero it set the corresponding bit in the TONEDET[0..1] word if not it clears this bit.

I.2.5 - Wiring

The user must specify the connection (wiring) between the input/output of the filter, the input/output of the power estimator, the output of the static levels and the two inputs of the comparators.

The outputs signal have an absolute address :

Node Address		
Signal Name	**Address**	**Description**
Ground	00	Signal always equal to 0000
RxSig	01	Receive signal from the analog front end, (after echo-substraction in V.32 mode)
RxSig2	02	Receive signal multiplied by 2
RxSig4	03	Receive signal multiplied by 4
	04..0F	Reserved
Filter [0..F]	10..1F	Biquadratic filter outputs
Power [0..F]	20..2F	Power estimator outputs
Level [0..F]	30..3F	Static levels

The user specifies the inputs of the filters, power and comparators. At least one input must come from the RxSig (node 01, 02 or 03). It is mandatory to connect all unused cell input to the ground signal (node 00).

III - EXAMPLE (see Figure G5)

Hereunder is an example of programming a single tone detector (using cell #3) and a complex differential tone detector (using cell #4 and #5).

The bit 3 of the TONEDET variable will be triggered each time the energy of that filtered signal is higher than static level number 3.

The bit 4 of the TONEDET variable will be on each time a receive signal has energy higher than the static level number 4. The bit 5 will be on only when the filtered (filter section 4 and 5) received signal is higher than the energy of the wideband signal number 4 ; this prevents triggering on noise.

Program cell #3 :

TDWW 03 00 13 01
Connect received signal to filter and filter to energy
TDWW 03 01 33 23
Connect level to comparator negative input and energy to positive input

Program cell #4 and #5 :

TDWW 04 00 01 01
Connect received signal to filter and energy
TDWW 04 01 34 24
Connect level to comparator negative input and energy to positive input
TDWW 05 00 15 14
Connect filter #4 output to filter and filter to energy
TDWW 05 01 24 25
Connect wideband energy to negative input and energy to positive input

Figure G3 : Tone Detector Wiring Address (first half)

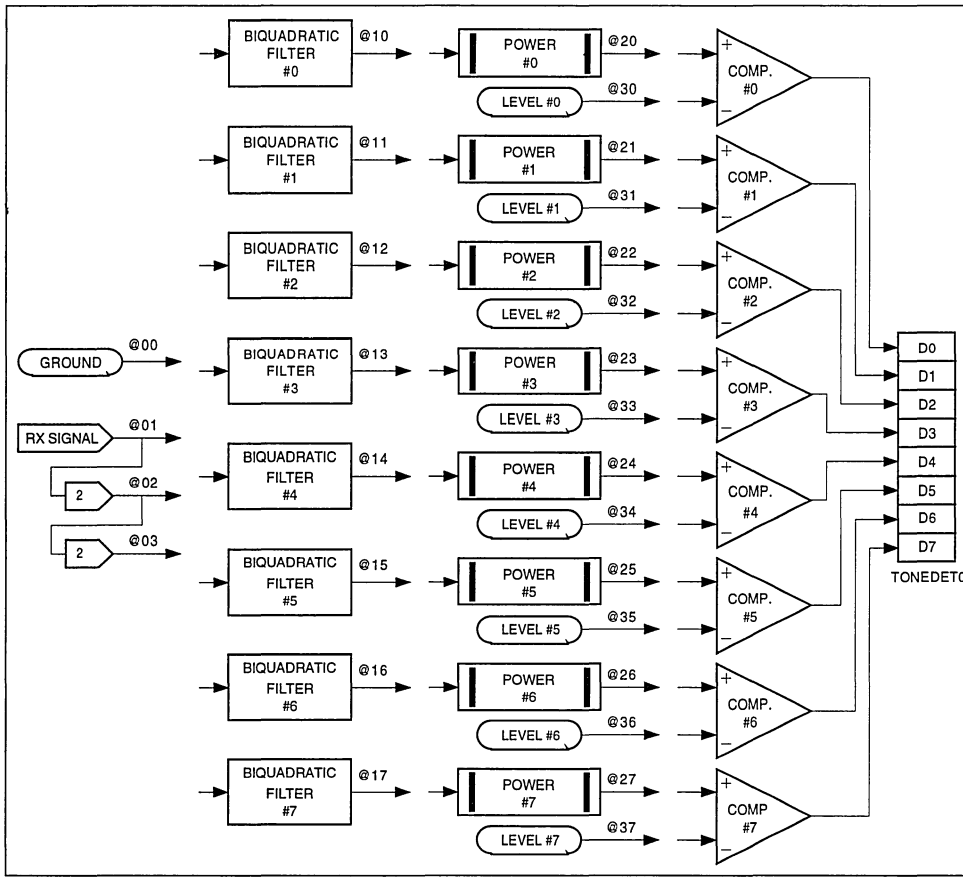


Figure G4 : Tone Detector Wiring Address (second half)

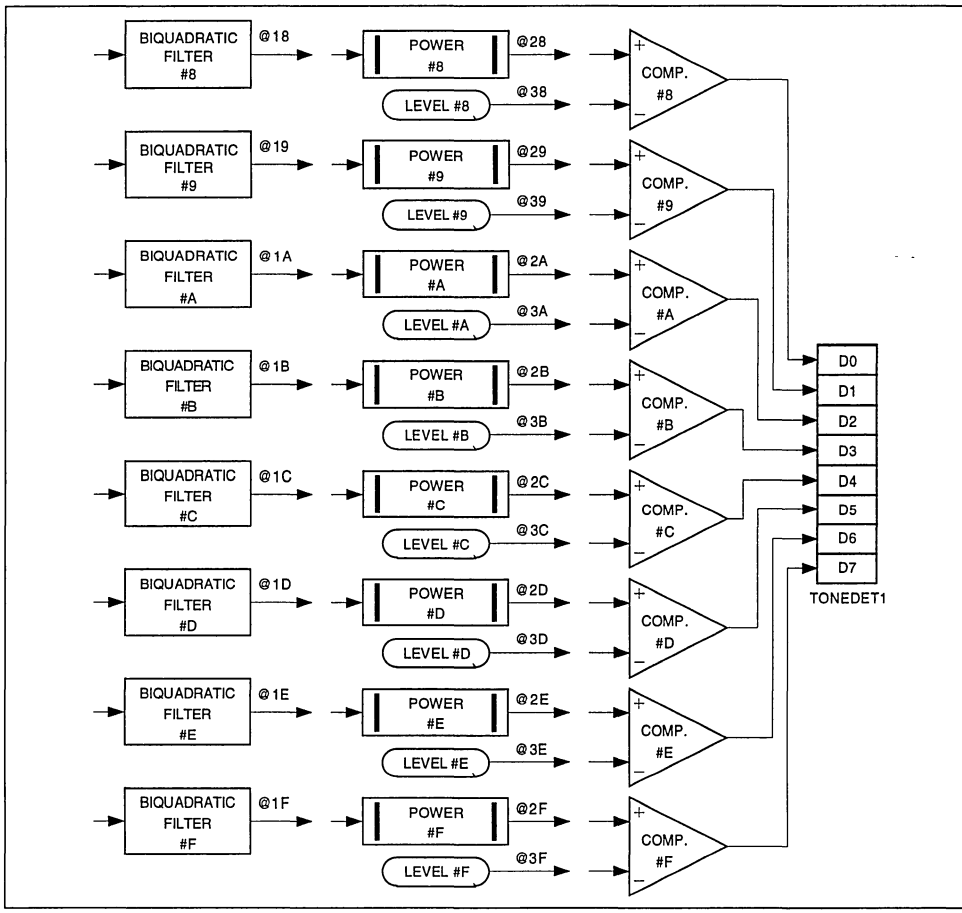
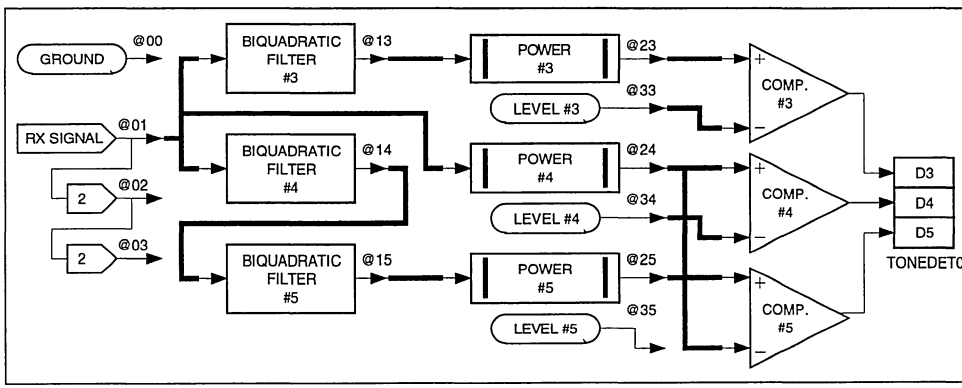


Figure G5 : Wiring Example



APPENDIX H : BUFFER OPERATIONS

I - INTRODUCTION

This appendix is dedicated to the buffer operations, either the data buffers, used either in data exchanges or the symbol buffer operations dedicated to bulk delay management.

II - RECEIVE OPERATIONS OVERVIEW

Figure H1 describes the receive data flow.
The ST75C502 uses parallel synchronous data.
8 bit words are synchronously available in the receive buffers. The buffer status holds the numbers of valid bytes received.
Each time the receiver has filled up a new buffer, it sets the corresponding flag with the proper status then generates the IT3 interrupt. The availability of the buffers is tested just before starting to fill them. This means that the host must not perform any buffer operation on the data part while the status remains 0.

III - TRANSMIT OPERATIONS OVERVIEW

Figure H2 describes the transmit data flow.
The ST75C502 uses parallel synchronous data.
8 bit words are synchronously read from the transmit buffers. The transmit status buffer holds the number of valid bytes to be transmitted (up to 8 per buffer).
Each time the transmitter has emptied a buffer, the IT2 interrupt is raised.

IV - BUFFER STATUS AND FORMAT DESCRIPTION

The following section describes the meaning and use of the buffer status words.

IV.1 - Transmit buffer

The transmit buffer status words are DTTBS0 and DTTBS1 (see the *Host Interface Summary* section in the main document) and are more likely to be seen as control words. These flags must be set by the host and are reset by the ST75C502. The data buffer exchanges being synchronized through these status words, an improper setting will trigger the error Err_Tx in the error status SYSERR. A value of 0 for DTTBS0 or DTTBS1 means that the corresponding buffers are empty : this value is written by the ST75C502. The unused bits of DTTBSx must be set to 0 by the host.

Field	Pos.	Val.	Description
BUFF_LENG	3..0	8..1	Number of valid bytes in the buffer

IV.2 - Receive buffer

The receive buffer status words are DTRBS0 and DTRBS1 (see the *Host Interface Summary* section in the main document). These flags are set by the ST75C502 and must be reset by the host. The data buffer exchanges being synchronized through these status words, an improper resetting will trigger the error Err_Rx in the error status SYSERR. A value of 0 for DTRBS0 or DTRBS1 means that the corresponding buffers are empty : this value must be written by the host.

Field	Pos.	Val.	Description
BUFF_LENG	3..0	8..1	Number of valid bytes in the buffer

Figure H1 : Rx Buffer Schematics

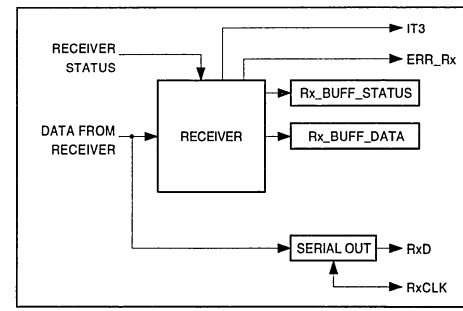
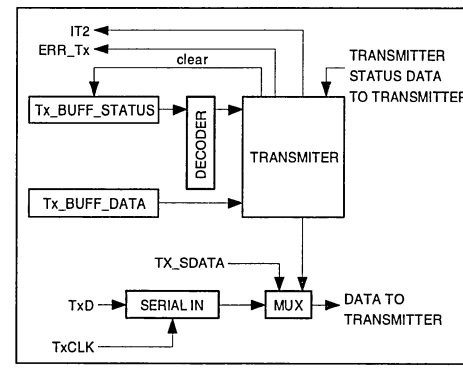


Figure H2 : Tx Buffer Schematics



V - DATA BUFFER MANAGEMENT

In the transmit path, the data buffer exchanges should always begin with the filling of buffer 0, then with the update of the buffer 0 status word. The initiation of the data exchanges is initiated then with the XMIT command.

VI - BULK DELAY MANAGEMENT

The processing of the bulk delay uses a simplified buffer exchange scheme. Each time the ST75C502 has internally buffered enough symbols, it writes them inside the symbol buffer area, then computes the address inside the host space where these symbols should be written. This address is a relative address inside the host data space, allowing thus the host to dispose this area the most convenient way. The target address is located in the SYMADR[0..1] registers under a 16-bit form.

These addresses must be defined by the user using the BULK command. It can be any valid 16 bit number assuming the base address (BA_ADDR) is on a 8 byte boudary and the top address (TO_ADDR) is higher and on a 8 byte boundary minus 1.

Eg : if we want to be able to cancel a 2 satellites Round trip delay we must have a bulk delay bigger than 2 times 560ms, lets say 1.5 seconds. The symbols needed are 1.5 · 2400 (3600 bytes). If we say that the base address is, for example, 0x4230 the top address must be 0x503F (= 0x4230 + 3600 - 1).

According to the current round trip delay, the ST75C502 computes the address of the symbols required for the far end echo computation. This address is computed (as the previous one) according to a circular addressing scheme inside the base .. top address space.

The symbol buffer status SYSSTA is then set to FF and the IT1 interrupt is raised. The host should then perform the following operations in sequence :

1) read the address SYMADR[0..1] of the target location for the symbols,
2) read SYMBU[7..0], the corresponding symbols, and store them at the addressed lolcation (8 symbols),
3) read the address SYMADT[0..1] of the symbols required by the ST75C502,
4) fetch the required 8 symbols and store them in the SYMBUF[7..0] array,
5) write the proper status word (00) in SYMSTA.

The ST75C502 meanwhile pools for the status word to be 00, then stores the symbols inside its own memory space for processing and sets the status word to its idle value FF.

VI.1 - Status Word

The status word SYSSTA can have the following values :

Field	Pos.	Val.	Description
SYSTA	7..0	00	Symbol buffer owned by the DSP
		FF	Symbol buffer owned by the host

VI.2 - Interrupt

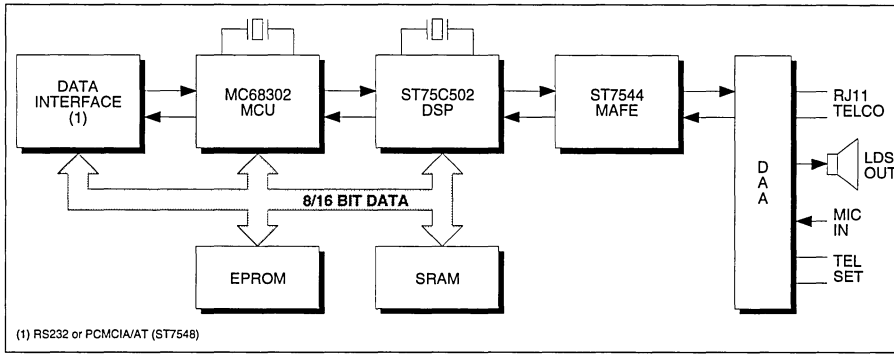
Each time a symbol buffer is processed by the ST75C502 an IT1 interrupt is generated. The host has an 8 symbols time (3.3ms) to process this interrupt otherwise an error occurs that will be signaled into the SYSERR bit 2 ERR_SYM.

SATURN

FUNCTION	***V.32bis / V.17*** ***DATA / FAX / VOICE MODEM***
APPLICATIONS	■ PC data/FAX/voice add-on card ■ Stand-alone modem ■ PCMCIA communication cards

GENERAL DESCRIPTION	SATURN is a **S**ystem **A**daptable **TURN**-key complete modem solution available as a chip set bundled with software package or as a ready to use demonstration board. The demonstration board includes a V.32bis/V.17 2 chip data pump (ST75C502/ST7544), a MC68302 16 bit MCU with software package (V.42, V.42bis, MNP2-5, FAX, V.25bis, AT commands), memories (EPROM, SRAM) and data interface (RS232, PCMCIA/AT bus).
MAIN FEATURES	■ All TQFP packages (PCMCIA compatible) ■ 2 chip data pump (ST75C502/ST7544) ■ ITU-T V.32bis, V.32, V.22bis, V.22, V.23, V.21, V.17, V.29, V.27t, V.21 channel 2 ■ Bell 103, 212A ■ Tone and DTMF programmable generation/detection ■ V.42bis/MNP5 data comp/decomp (F.D. 115200Bps) ■ V.42/MNP4 error detection/correction ■ FAX class I and class II (EIA/TIA) ■ V.25bis automatic call / answer ■ AT command set ■ Adaptable data interface (RS232, AT bus/PCMCIA (ST7548)) ■ Easy MCU software customization (MMA licence)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (CHIP SET)

Parameter	Symbol	Condition	Rating	Unit
Max. supply voltage	V_{DD}max.	T_A = 25°C	-0.3 to +7.0	V
Input/output voltage	V_i, V_o	T_A = 25°C	-0.3 to V_{DD} +0.3	V
Storage temperature	T_{stq}		-40 to +125	°C
Operating temperature	T_A		0 to +70	°C

SGS-THOMSON MICROELECTRONICS

USER'S MANUAL

SATURN
V.32bis / V.17 modem with V.42bis, FAX Class 1 & 2 and MNP

SUMMARY **Document page**

I - INTRODUCTION

This document describes the System Adaptable TURNkey (SATURN), a highly integrated High Speed modem built around the ST75C502 data pump from SGS-THOMSON microelectronics and the MC68302 software from Modem Manufacturers Associates.

The ST75C502 data pump includes all ITU-T modulation standards from V.32 bis to V.22, V.17 to V27 ter, and FSK V.23 & V.21.

With its powerful 68000-family core CPU, the SATURN integrates Automatic Call Unit (ACU), error correction / data compression (i.e. V.42 bis, MNP 5) and FAX functionality into a single processor and all with higher performance than was achievable with older 8-bit processor designs.

Designed for use in a variety of environments, the SATURN may be connected to asynchronous and synchronous microcomputers and / or terminals. It is compatible with both dial-up (GSTN) and leased lines.

Information contained herein serves as a development tool to instruct the modem manufacturer in both the SATURN's basic design as well as customizing its operation to meet specific requirements.

The SATURN has been designed to satisfy two vital needs within the data communications equipment manufacturing industry : The software design of the SATURN allows the manufacturer to make custom modifications to suit customer-specific needs. As well, the power inherent in the SATURN's software and hardware provide outstanding performance as well as a solid platform to accommodate recent technological innovations (e.g. V.FC, V.34, V.34bis).

The SATURN design is made up of different "communications modules". Each module performs specific tasks in the SATURN and all of them have been specified to conform with a clear and specific definition for all pin connections. The modules perform functions such as the controller (otherwise referred to as the automatic call unit or ACU), data pump, data access arrangement (DAA), hybrid and audio, and RS-232 interface.

Upgrades and new UCM's will be added to the SATURN in the form of Appendices. Because of the modular structure of the SATURN's basic design, any enhancements may be easily incorporated into any existing product.

I.1 - How this Manual is Organized

This document has been written to familiarize the customer with the operation, use and features of the SATURN. The manual is divided into five chapters and four appendices. The chapters describe the SATURN's operation as it is delivered to the customer.

The appendices provide basic information about SATURN design as well as electricals schematics for each UCM. The parts list supplied gives the comprehensive bill of materials required to populate the printed circuit board as specified.

Chapter I	is an introduction to this manual and the SATURN.
Chapter II	is an overview of the general features and functionality of the SATURN. Issues such as compatibility, front and back panel organization as well as jumper settings are among those discussed.
Chapter III	gives a complete description of the SATURN's AT Command set as well as the Facsimile and Autologon features.
Chapter IV	gives a complete description of the SATURN's V.25 bis command set.
Chapter V	gives a complete description of the SATURN's S-registers, including default values and bit mapped arrangements.
Appendix A	shows the basic block diagram of the SATURN, and gives the different possible adaptation of the basic design.
Appendix B	shows a simplified layout schematic of the stand alone modem as it is delivered.
Appendix C	supplies the electrical schematics of the SATURN stand alone modem.
Appendix D	supplies the complete part list of the SATURN stand alone application.

II.2 - Conventions

Please note the following conventions used throughout this document.

Signals

High = 1 bit = +5V

Low = 0 bit = 0V

Bit Order

The bits within a byte are always numbered 0 through 7 with 0 being the least significant bit (LSB).

II - GENERAL DESCRIPTION

The SATURN has been designed to transmit and receive data over standard telephone communications lines in accordance with the following standards/recommendations : ITU-T V.32 bis, V.32, V.23, V.22 bis, V.22, V.21, Bell 212A and Bell 103. For facsimile transmission, ITU-T V.17, V.29, V.27 ter, and V.21 channel 2 are supported. In addition, the SATURN supports MNP error correction and MNP Class 5 data compression as well as V.42 error correction and V.42 bis data compression. The latter can provide error-free full-duplex data transmission at data rates approaching 115.2 kbits/s. This is achieved through a combination of high speed modulation techniques (i.e. ITU-T V.32 bis which allows a basic rate of 14400 bits/s) coupled with the efficient data compression techniques provided by the error correction and data compression protocols.

In addition to the above features, the SATURN provides all of the standard features found on other commercially available modems including : Automatic dialing and call progress monitoring, autoanswer capabilities, storage of modem configurations and telephone numbers in non-volatile internal memory, industry-standard AT command set, lamps that give visual indication of some aspects of the SATURN's operating state and remote/internal test modes.

The AT command set deserves special mention. This feature allows the user to access or control the SATURN's behaviour through the use of data sent to it through the DTE interface. Whenever the user issues such a command, a response will be sent that may occur in two forms. The first form is referred to as "information text". This consists of information that the user has explicitly requested as a part of a specific command (e.g. the I command causes the SATURN to return information about its software version to the DTE as information text). The second form is referred to as a "result code" and gives information about either a change in operating state of the SATURN or the result of an AT command. For example, the result code "OK" will be sent after the completion of the I command while a "NO CARRIER" result code informs the user that a connection with a remote modem has been terminated.

While result codes may be generated by the SATURN asynchronously (i.e. as an indication of a change in operating state rather than as a response to an AT command), information text is always sent as a response to a command.

Facsimile transmission and reception is also managed through extensions to the AT command set. The SATURN supports both EIA/TIA Class 1 and Class 2 command sets.

II.1 - Compatibility

The SATURN supports the following ITU-T recommendations :

V.32bis Full duplex asynchronous at 14400, 12000, 9600, 7200 or 4800 bps with or without MNP, V.42 and V.42 bis.
Full duplex synchronous at 14400, 12000, 9600, 7200 or 4800 bps.

V.32 Full duplex asynchronous at 9600 or 4800 bps with or without MNP, V.42 and V.42 bis.
Full duplex synchronous at 9600 or 4800 bps.

V.17 Half duplex synchronous at 14400, 12000, 9600 or 7200 bps for fax tx & rx.

V.29 Half duplex synchronous at 9600, 7200 or 4800 bps for fax tx & rx.

V.27ter Half duplex synchronous at 4800 or 2400 bps for fax tx & rx.

V.23 Full duplex asynchronous at 1200 bps in forward channel and 75 bps in reverse channel.

V.22bis Full duplex asynchronous at 2400 bps with or without MNP, V.42 and V.42 bis.
Full duplex synchronous at 2400 bps.

V.22 Full duplex asynchronous at 1200 bps with or without MNP, V.42 and V.42 bis.
Full duplex synchronous at 1200 bps.

V.21 Full duplex asynchronous at 300 bps with or without MNP.
Full duplex synchronous at 300 bps for facsimile transmission and reception.

The SATURN also supports the following Bell standards :

212A Full duplex asynchronous at 1200 bps with or without MNP, V.42 and V.42 bis.
Full duplex synchronous at 1200 bps.

103 Full duplex asynchronous at 300 bps with or without MNP.

The SATURN supports facsimile transmission and reception through compliance with EIA/TIA standard 578 (Fax Class 1) and proposal EIA 2388 (Fax Class 2).

The SATURN incorporates V.42 and MNP levels 2 through 4 error correction as well as V.42 bis and MNP Class 5 data compression.

II.2 - Front Panel

The SATURN offers a lot of front panel LEDs with the following meanings :

TX : Data Transmit (V.24 103).
RX : Data Receive (V.24 104)
DCD : Data Carrier Detect (V24 109).
CTS : Clear To Send (V.24 106).
DSR : Data Set Ready (V.24 107).
DTR : Data Terminal Ready (V.24 108).
OH : Off Hook indicator.
TST : Test indicator (V.24 142).
PWR : Power supply indicator.

Two female 3.5 jack connector socket are available for the use of an external loudspeaker (HP) or an externel microphone (MIC). The internal electret microphone is located very close to the external microphone connector socket.

II.3 - Back Panel

The back panel of the SATURN stand alone modem consists of a DB25 female connector socket for the V.24 DTE interface (RS 232), a standard 2.5 jack connector socket for connection to the 7.5V power supply (PW 7.5V), two RJ11c style jacks (one for the GSTN line connection - LINE - and the other for a phone connection - PHONE -) and a reset pushbutton (RST).

II.4 - DB25 Pinout

Pin	V.24 Circuit	Function	Direction
1	101	Protective Ground	GND
2	103	Transmit Data	Input
3	104	Receive Data	Output
4	105	Request to Send	Input
5	106	Clear to Send	Output
6	107	Data Set Ready	Output
7	102	Signal Ground	GND
8	109	Receive Line Signal Detect	Output
15	114	Transmit clock	Output
17	115	Receive Clock	Output
18	141	Local Analog Loopback	Input
20	108	Data Terminal Ready	Input
21	140	Remote Digital Loopback	Input
22	125	Ring Indicator	Output
24	113	External Clock	Input
25	142	Test	Output

II.5 - Dumb Mode

The SATURN may be configured to ignore commands issued from the DTE. In order to do this, dumb mode must be enabled. When in dumb mode the SATURN ignores AT commands (including the escape sequence) and refrains from sending result codes to the DTE. This is especially useful in applications where the SATURN is permanently connected to a host that does not support the AT command set. In this case, the use of dumb mode ensures that only user data will flow between the SATURN and the host and that the SATURN cannot accidentally be placed in on-line command mode by user data.

II.6 - Functional Operation

This section describes the various operational modes that the SATURN may assume. Each of these modes exists so that a certain capability of the SATURN (e.g. command, data transfer) may be invoked.

Command Mode

For the SATURN to accept and process a command it must be in command mode. When powered up, it recalls the appropriate stored configuration (see the &V command) and then enters command mode from which you may place or receive calls, or alter any of its settings. If dumb mode has been selected, it is not possible to alter the settings of the SATURN because it does not response to AT commands. It is still possible to make or answer calls through other facilities provided by the SATURN (e.g. DTR dial, auto-answer) if an appropriate configuration was stored in its non-volatile memory previously.

Connect Mode

The SATURN is in this mode while the channel establishment procedures are occurring. The data pump handshake is performed at this time as well as any possible MNP or LAP-M link establishment. Note that the D command is used by the call originator and the A command (or auto-answer) is employed by the call answerer. The negotiation that occurs during the connect state will fail if the proper command is not given.

If the SATURN has been configured for facsimile operation, the appropriate data pump handshake is performed while in connect mode.

On-Line Mode

To transmit or receive data, the SATURN must be in the on-line mode. This occurs once a connection has been established. In this mode, data received from the DTE is transmitted to the remote modem (with appropriate MNP, LAP-M or facsimile proc-

essing, as necessary) while data received from the remote modem is, in turn, passed onto the DTE.

Time Independent Escape Sequence (TIES) and On-Line Command Mode

The following text relating to TIES was extracted from the VEN-TEL document Rev 1.06. When transferring into on-line command mode, in every instance an "AT" command will follow the three character escape sequence (ex. +++). All "AT" commands or command strings MUST be preceded by "AT" and terminated by the contents of S3 (typically a <CR>.

The TIES escape sequence, as in all AT command strings, must be terminated by the contents of <S3>. If <CR> characters are detected immediately before the <S3> terminating character, it is to be ignored. This is the same as any normal AT command line.

Note : TIES is an escape detection scheme - not an escape generation scheme.

A TIES escape sequence is comprised of the following :

a) A three character escape sequence user programmable case sensitive.
b) Followed by mandatory "AT" characters non user programmable case insensitive.
c) Followed by valid AT commands and settings case insensitive.
d) Followed by a mandatory terminating character terminating character is stored in S3 the default for <S3> is <CR>.

Note : Case insensitivity only pertains to alpha characters.

When a TIES modem detects a valid three character escape sequence, and only the three character escape sequence, it immediately enters in the command mode (no guard time is required). The modem stays in the command mode until one of the following occurs :

a) Detection of an invalid AT command string after the last character of the three character escape sequence.
b) ATO (return to data mode) is detected in the subsequent valid AT command string.
c) ATH (disconnect from telephone line) is detected in the subsequent valid AT command string.

"Valid" Three Character Escape Sequence

The TIES escape characters must be preceded by the standard three character escape sequence (typically +++).

TIES requires that the three character escape sequence be continuous and not repeated. That is, the character immediately preceding the first character of the three character escape sequence cannot be equal to the first character. For example, if the three character escape sequence is AAA, the character before the first A cannot be an A. If the three character escape sequence is +++, the character before the first + cannot be a +.

"Valid" AT Command Strings and Settings

The three character escape sequence is monitored to recognize the first three valid characters, then an A must be detected, then a T must be detected followed by valid AT string(s) and setting(s).

If the modem detects the valid three character escape sequence, followed by valid AT command string characters, and then is terminated by <S3>, the modem will execute the AT command and stay in the command mode.

Note : The acceptable length of the TIES valid AT command string detection is 40 characters.

"Invalid" TIES Command Strings

Up to the terminating <S3> any invalid character(s) will immediately return back to the data mode.

If invalid AT commands are detected, TIES immediately returns back into the data mode and any valid commands which may have been in the string will be ignored and not implemented.

Once the <S3> terminates a valid TIES escape sequence, any subsequent invalid AT command strings will not cause a return to the data mode. Only the normal return method is used (i.e. ATO or ATH).

TIES "Ignore" Characters

While detecting a valid TIES command string, it is possible that some characters may be detected which are not true AT commands. If TIES considers any AT commands as invalid, TIES will return the modem back to the data mode. This could give TIES the false reputation of not functioning with some software packages.

To avoid these instances we must generate a list of characters which may be found in some AT command strings which will be considered ignore characters. These characters are to be treated as non-existent to the TIES escape command string. Ignore characters may be found any time or place between the third + (or equivalent value in S2) and the terminating <S3> character.

"Ignore" Character Table

Keyboard Character	Hex Value	Decimal Value
LF> (^J)	0A	10
<space>	20	32
<CR>	0D	13

Notes : 1. <CR> is ignired only when S3 is not equal to 13 Decimal.
2. Additional characters may be added to this ignore table as software packages are discovered which may use illogical characters for special applications

The "OK" Response

There are two conditions to which the "OK" response will be returned to the DTE :

Note : The modem enters the command mode immediately upon detection of the valid three character escape sequence. Remember, posting of the OK does not indicate when the modem actually entered into the command mode. The posted OK simply indicates the status of the mode.

1) An OK response is posted to the DTE one EPD (Escape Prompt Delay) time (set in S12) after detection of the last character of the valid three character escape sequence.

IT IS IMPORTANT TO NOTE, AT THIS POINT TIES HAS ALREADY ENTERED INTO THE COMMAND MODE - THE THREE CHARACTER ESCAPE SEQUENCE AND ONLY THE THREE CHARACTER ESCAPE SEQUENCE CAUSED TIES TO ENTER THE COMMAND MODE - NOT THE EPD TIMER.

The EPD time is used only for posting the OK message. The EPD time does not indicate when TIES actually entered into the command mode.

The modem does not return OK if any characters are detected within one EPD time after the last character of the valid three character escape sequence.

If data is being received in condition 1), the data continues to be received as normal. The OK is returned in the receive data stream. That is, the received data may look like this :

xxxxxxxxxxxxxxxxxxxxxOKxxxxxxxxxxxxxxxxxxxx

2) An OK will be posted to the DTE upon detection of the AT followed by the TIES escape sequence with the terminating <S3> character.

If data is being received from the remote modem in condition 2), the OK is sent on RXD and any further received data is blocked from appearing on the DTE.

In condition 2), you will see two OKs posted. The two OKs will emerge if you wait the EPD time, then send the rest of the valid escape sequence with the <S3> terminator.

If an OK has been sent to the DTE and the modem does not stay in the command mode, a proper "CONNECT XXX" must be sent indicating the modem has returned to the data mode.

Note : In TIES, you may be in the command mode even if the OK has not been sent. GUARD TIME Time dependent escape sequences require that no characters appear a pre-set time before and/or after the escape characters. TIES is unlike time dependent methods in that it functions whether or not guard time intervals are present. This allows TIES complete compatibility with both methods.

THE TIES ESCAPE SEQUENCE DOES NOT REQUIRE ANY TIME PERIOD OR GUARD TIME, WHATSOEVER.

To be very specific, the three character escape sequence and subsequent AT command string can appear with or without a guard time. It makes absolutely no difference to the TIES detection scheme.

On-Line Command Mode

Once a connection has been established, the SATURN must be returned to the command mode before it will accept any AT commands. The escape sequence (the three characters "+++" received from the DTE) allows the user to put the SATURN into on-line command mode. Dropping DTR if the &D1 option has been selected will also cause the SATURN to make the transition from on-line mode to on-line command mode.

In on-line command mode, operation of the SATURN is identical to command mode described above except that the physical connection with the remote modem is still maintained.

Note that the O command is used to return to on-line mode. The H command will terminate the physical connection and leave the SATURN in command mode.

Refer to the next chapter for a full description of the AT command handler and the escape sequence.

Test Mode

The SATURN will enter test mode when it receives a command (either from the user or from a remote modem) to do so.

Various tests are supported by the SATURN, including the capability to make a connection with itself locally (analog loopback) or echo data received from the remote modem back to that modem (digital loopback). Digital loopback may be local (initiated by an AT command) or remote (initiated by a request from the remote modem). The SATURN can also initiate digital loopback in a remote modem.

For more information about tests, refer to the description of the &T command as well as S-registers S16 and S18.

III - AT COMMANDS, FACSIMILE AND AUTOLOGON FACILITY

This section discusses the operation of the AT command interpreter as well as describing all AT commands supported by the SATURN. Note that the SATURN includes the capability to have its command set modified as desired. Refer to chapter 5 for more information.

Also discussed here is the Autologon feature. With this, the user may implement a system where the SATURN provides a level of security designed to prevent unauthorized access to any data processing system.

III.1 - The AT Command Interpretor

The SATURN implements the industry-standard AT command set in a manner consistent with that of most commercial modem manufacturers. These commands are only available to the user when the SATURN is in command or on-line command mode and are realized in the form of asynchronous characters received from the DTE. Here is a basic description of its operation :

The AT Prefix

All command lines must begin with the two letters "A" and "T". Either upper case or lower case is acceptable but both letters should have the same case.

The SATURN attempts to determine the speed of the "A" by measuring the duration of its start bit. The "A" must be received at one of the speeds supported by the SATURN (i.e. 300, 1200, 2400, 4800, 9600, 19200, 38400, 57600 or 115200 bps) or this process will not succeed and the command process will fail.

Once the "A" and "T" characters have been received, the SATURN determines the parity of the DTE by analyzing the parity bits of these two characters. All result codes and information text issued by the SATURN will be generated with this parity.

The following asynchronous character formats are supported :

Start Bit	Data Bits	Parity Bit	Stop Bits
1	7	Even or Odd	1
1	7	None	2
1	7	Mark or Space	1
1	8	None	1

If the SATURN receives a character but fails to detect it as an "A", it begins to search for another "A" character. If the SATURN receives an "A" but it is not followed by a "T", the SATURN begins searching for an "A" again.

The A/ Command

If the characters A/ (instead of AT) are received, the SATURN will re-execute the most recently received command line. In this case, the parity is assumed to be the same as that of the most recently received AT prefix.

Command Line Characters

All characters that follow the AT prefix are taken to be commands (these are described below).

The parity bit of all command characters is ignored.

Spaces (20 Hex) between command characters (and option characters) are ignored.

No more than 255 command line characters are allowed. If more than this is received, the command line will be ignored and the "ERROR" result code will be returned when the carriage return character is received. This behaviour applies even if an attempt to remove the excess characters is made using the backspace character.

The Carriage Return Character

The carriage return character is used to signify the end of the command line. When this character is received, the SATURN will begin to process the command characters previously received.

The default value for this character is Control-M (D Hex) but it may be changed through modification of the appropriate S-register.

The Backspace Character

The backspace character is used to edit the command line. If it is received, the SATURN will ignore the most recently received command character and issue a backspace-space-backspace sequence to the DTE (if echoing is enabled).

If an attempt is made to backspace onto the AT sequence, the SATURN will ignore the backspace character and take no action.

The default value for this character is Control-H (8 Hex) but it may be changed through modification of the appropriate S-register.

Characters Ignored by the SATURN

Other than the above characters, all ASCII control characters (value less than 20 Hex) are ignored.

Processing Command Characters

The SATURN processes each command character in the sequence that it was received. Any change in operational state required by a command occurs as soon as the command is processed.

If an error occurs in the processing of a command, the SATURN will stop processing the command line and output the "ERROR" result code.

The detection of an unimplemented command during processing causes a command processing error.

Some commands (e.g. E, I, Q, V) may be followed by numeric arguments which select a particular option for that command. If the argument is missing, a value of zero is assumed. If the value is outside the valid range of arguments for that command, a command processing error occurs.

If command line processing completes without error, the "OK" result code will be output.

III.2 - Basic AT Commands Supported by the SATURN

This section discusses the AT commands generally used to handle the transmission of asynchronous data.

A : Answer mode

Causes the SATURN to go off hook and attempt a handshake in answer mode.

B : Bell/ITU-T Mode

B0	ITU-T modulation schemes are used (at 1200 bps).
B1	Bell modulation schemes are used (at 1200 bps).

D : Dial Number

Instructs the SATURN to go off-hook and execute the dial string which follows the D. Commands which may be part of the dial string are listed below. Any unrecognized character in the dial string is ignored. Once dialing is complete, the SATURN attempts a handshake in originate mode (unless the R parameter is given).

0-9 (any numeric digit)	Causes the indicated symbol to be dialled.
A, B, C, D, # or * (tone dial only)	Causes the indicated symbol to be dialled.
P	Causes subsequent numbers to be pulse dialled.
T	Causes subsequent numbers to be tone dialled.
R	Forces the SATURN to dial a call in answer mode.
W	Causes the SATURN to wait for a dial tone using S7 as a time out.
,	Causes a delay, determined by S8, before the SATURN proceeds with the next command or digit.
!	Causes the SATURN to go on-hook for .5 sec and then off-hook for .5 seconds before continuing.
@	Causes the SATURN to wait until it detects 5 seconds of silence before continuing.
;	Causes the SATURN to go to the command mode when the number is dialled. In order to proceed with channel establishment mode ATO or ATD must be entered. Any characters that follow this parameter are treated as AT commands.
L	Causes the last telephone number that was dialled by the SATURN to be re-dialled.
S	Causes the SATURN to dial the number in stored position "n" [format is S = n or Sn].
^	Causes the SATURN to skip emitting calling tone after dialling.

Note : If S41 is set to a value other than 0, the SATURN will attempt a maximum of S41 redials upon call failure.

E : Echo Commands

Defines whether characters are echoed back from the SATURN to the DTE when in command mode.

E0	Command echo inhibited.
E1	Command echo enabled.

H : Hook Switch Control

Controls the hook switch relay of SATURN.

H0	Causes the SATURN to go on-hook.
H1	Causes the SATURN to go off-hook.

In error correction mode S38 dictates the delay before going on-hook.

I : Interrogate SATURN Status

I0	Requests SATURN product code.
I1	Requests that a checksum calculation be performed on the software ROM. The answer is displayed as three hexadecimal digits.
I2	The SATURN performs a ROM checksum, compares the result against a stored value, and returns an OK or ERROR message depending on the success of the comparison.
I3	The SATURN sends its firmware revision number.
I4	The SATURN sends its ASCII string test.
I5	The SATURN sends its data pump chipset revision.

L : Speaker Volume

Sets the speaker volume when speaker is on.

L0 Low volume.
L1 Low volume.
L2 Medium volume.
L3 High volume.

M : Speaker Control

Controls how speaker behaves when off-hook.

M0 Speaker always off.
M1 Speaker on until handshake is complete.
M2 Speaker always on.
M3 Similar to M1 except speaker is off when dialing.

N : Handshaking

Selects whether a connection will be forced to a specific speed.

N0 Sets the required connection speed to that set under S37.
N1 If S-register S37 is not equal to 255 it allows handshaking at the highest speed supported by both modems. If S-register S37 equals 255 it allows handshaking at the highest speed supported by both modems and DTE.

O : Return to On-Line State

Applicable when a physical connection with a remote modem exists and the SATURN is in the on-line command state.

O0 Returns the SATURN to the on-line state.
O1 As O0 except that when a 2400 bps or higher connection is established an equalizer retrain sequence is transmitted.

P : Pulse Dialing

Causes subsequent dial digits to be executed as pulses.

Q : Return Result Codes

Defines whether or not the SATURN will issue result codes to the DTE.

Q0 Result codes returned.
Q1 Result codes not returned.
Q2 Result codes returned in originate mode only.

T : Tone Dialing

Causes subsequent dial digits to be executed as DTMF tones.

V : Verbose mode

Defines the form of result codes returned by the SATURN.

V0 Numeric form responses enabled.
V1 Verbose responses enabled (English responses).

W : Connection Result Codes

Defines the type of (extended) negotiation result codes to return.

W0 Negotiation codes not reported.
W1 Negotiation codes reported in 3 line format (Hayes format).
W2 Negotiation codes reported in 1 line format (Microcom format).

X : Extended Response Codes

Defines the GSTN network tones which are recognized by the SATURN.

X0 Causes the SATURN to ignore any network tones and omit the connection speed message.
X1 As above but enables the connection speed result codes.
X2 Causes the SATURN to detect dial tone.
X3 Causes the SATURN to detect busy tone.
X4 Causes the SATURN to detect busy and dial tones.
X5 Causes the SATURN to report ringing, but dial tone is ignored.
X6 Causes the SATURN to perform adaptive dialing (automatically determine if dialing can be performed using DTMF signalling).

Y : Long Space Disconnect

Y0 Disabled.
Y1 Enabled.

When set for Y1, on-line and not in error correction : The SATURN will disconnect if it receives a continuous "break" from the remote modem for a period of time greater than or equal to 1.6 seconds. As well, when the SATURN is instructed by the DTE to hang up it will send a 4 second break to the remote modem prior to going on-hook.

Z : Recall User Configuration

The user configuration stored in non-volatile memory is recalled to become the active configuration.

Z0 Resets SATURN and recalls user profile 0.
Z1 Resets SATURN and recalls user profile 1.
Z2 Resets SATURN and recalls user profile 2.
Z3 Resets SATURN and recalls user profile 3.

&A : ODP/ADP for V.42 Initiator

Defines whether the SATURN will send the ODP (Originating Detection Pattern) and detect the ADP (Answer Detection Pattern) when initiating a V.42

handshaking. This command is effective only when the SATURN is set for V.42 auto-reliable.

&A0 The SATURN will not transmit the ODP thus will not detect the ADP and will immediately beginning synchronous handshaking.

&A1 The SATURN will transmit the ODP and detect the ADP.

&B : Data Terminal Equipment Speed in Data Mode

&B0 DTE speed equals the line speed.

&B1 DTE speed equals the speed of the last AT command or the default value on power up.

&C : Data Carrier Detect Options

Defines what the SATURN outputs as the DCD signal on the DTE interface.

&C0 The interface control signal DCD is always ON.

&C1 In command and connect modes the DCD signal is OFF. When on-line without error-correction, the signal DCD remains OFF until the carrier is detected, for the period defined by S9, at which time DCD goes ON. When on-line with error correction, the signal DCD goes ON once error correction is established.

&D : Data Terminal Ready Options

Defines how the DTR signal is interpreted by the SATURN. If S25 is not zero the DTR signal is ignored for S25 seconds after a call is indicated (See S25 definition).

For asynchronous mode :

&D0 DTR is ignored.

&D1 If DTR drops for a period of S25 milliseconds while the SATURN is on-line, the effect is the same as if the escape sequence is received, forcing the SATURN into command mode without dropping the connection. At other times DTR is ignored.

&D2 DTR functions as ITU-T circuit 108.2. While DTR is OFF the SATURN will not answer a call. If DTR drops for a period of S25 milliseconds while the SATURN is on-line, the call is immediately terminated.

&D3 As for &D2 except that the transition of the DTR signal from ON to OFF has the same effect as entering the ATZ command except that the retrieved configuration profile will be as per the &Y command.

For synchronous mode :

If &Q1 is set, DTR is interpreted as for asynchronous mode when off-line and placing calls. When on-line and set for &D1, an ON to OFF transition of DTR will cause the SATURN to enter asynchronous on-line command mode. For all other &D settings an ON to OFF transition of DTR will cause the SATURN to hang up.

If &Q2 is set the &D command is ignored. A OFF to ON transition of DTR when off-line will cause the SATURN to initiate a call using the telephone number stored in location 0. An ON to OFF transition of DTR when on-line will cause the SATURN to hang up. No calls will be answered if DTR is low.

If &Q3 is set the &D command is ignored. A OFF to ON transition of DTR when off-line will cause the SATURN to initiate a call using the ATD command. An ON to OFF transition of DTR when on-line will cause the SATURN to hang up. No calls will be answered if DTR is low.

&E : Auto Retrain

Determines whether the SATURN will suspend transmission and send a retraining sequence if line conditions deteriorate.

&E0 Disable auto retrain & enable auto disconnect.

&E1 Enable auto retrain & auto disconnect.

&E2 Disable auto retrain & auto disconnect (for B.E.R. test, only when direct or normal modes).

&F : Recall Factory Configuration

The factory configuration contained in the ROM is loaded to become the SATURN's active configuration.

&F0 V.42 factory defaults.

&F1 MNP factory defaults.

&F2 Basic asynchronous operation defaults.

&G : Guard Tone

Defines what guard tone SATURN transmits when answering a call (1200, 2400 bps).

&G0 No guard tone.

&G1 550Hz guard tone.

&G2 1800Hz guard tone.

&I : Break Mode Control

Defines how the SATURN handles a break condition on the DTE interface.

&I0 The break is sent in sequence with the received data (non-expedited / non-destructive).

&I1 The break is immediately passed through without buffering by either modem (non-destructive / expedited).

&I2 The break is expedited and destructive. The break causes the data buffers at both ends to be cleared and the break is immediately passed through.

&K : Flow Control

Defines the flow control options

&K0 Flow control is off.

&K3 Hardware Flow Control [RTS/CTS].

&K4 Software Flow Control [Local XON/XOFF]. In this mode the SATURN recognizes and transmits the XON/XOFF characters from and to the DTE in order to start or stop data. The SATURN will not transmit the XON/XOFF characters received from the DTE to the remote modem.

&K8 Unidirectional Software Flow Control [Transparent XON/XOFF]. In this mode the SATURN recognizes the XON/XOFF characters from the DTE in order to start or stop data. The SATURN will also transmit the XON/XOFF characters received from the DTE to the remote modem. With this type of flow control, the SATURN does not use the XON/XOFF characters to flow control the DTE.

&K12 Software Flow Control [Local/Transparent XON/XOFF]. In this mode the SATURN recognizes and transmits the XON/XOFF characters from and to the DTE in order to start or stop data. The SATURN will also transmit the XON/XOFF characters received from the DTE to the remote modem.

&K16 Software Flow Control [Internal XON/XOFF - for non error correcting mode]. In this mode the SATURN recognizes and transmits the XON/XOFF characters from and to the remote modem in order to start or stop data. The SATURN will not transmit the XON/XOFF characters received from the remote modem to the DTE. There is no flow control on the DTE interface. This is also known as DCE to DCE software flow control.

&K20 Software Flow Control [Internal and Local XON/XOFF - for non error correcting mode]. In this mode the SATURN recognizes and transmits the XON/XOFF characters from and to the remote modem in order to start or stop data. The SATURN will not transmit the XON/XOFF characters received from the remote modem to the DTE. The SATURN also recognizes and transmits the XON/XOFF characters from and to the DTE in order to start or stop data. The SATURN will not transmit the XON/XOFF characters received from the DTE to the remote modem.

&L : Line Type Select

Selects if the SATURN operates in lease line mode or GSTN.

&L0 GSTN mode.

&L1 Leased line mode.

In lease line mode user has to set Bit 7 o f S14 depending on whether he wants "answer" or "call" mode. Bit 7 of S14 is automatically set when entering the "D" command and automatically cleared when entering the "A" command. In this mode the SATURN will attempt a line connection at the same rate as the DTE speed (up to 14 400). It will attempt to handshake for 30 seconds. If it fails it will report NO CARRIER and will give the user 3 seconds to enter a command. If during this time no user commands were entered, the SATURN will again proceed with a 30s handshaking. This will go on until a connection succeeds or until a user command is entered between handshaking attempts. If lease line is configured in the stored profile to retrieve on power up, the SATURN will enter handshaking after power up at the DTE speed (S23) and mode (Bit 7 o f S14) stored in this profile. The user can break this procedure by entering any AT command after the NO CARRIER message.

DTE Speed	Handshake Speed	DTE Speed	Handshake Speed
300	300	19200	14400
1200	1200	38400	14400
2400	2400	57600	14400
4800	4800	115200	14400
9600	9600	-	-

&N : Error Control Fallback Character

Selects if the fallback character is to be checked for during the error control mode negotiation sequence. This character will cause the SATURN to immediately fall back to regular asynchronous mode. This character is stored in S46.

&N0 Disable fallback control character.

&N1 Enable fallback control character.

Note : This command affects how data received from the DCE is processed.

&O : Error Control Buffer Control

Determines buffering to be performed during the error control negotiation period.

&O0 Discard data received during negotiation.

&O1 Buffer data received during negotiation. The buffered data will be sent to the DTE after the connect result code if error control negotiation fails.

Note : This command affects how data received from the DCE is processed.

&P : Pulse Dial Make/Break Ratio

Sets the make/break ratio to be used when pulse dialing.

&P0 39% / 61% ratio for North American telephone networks.

&P1 33% / 67% ratio for United Kingdom telephone networks.

&Q : Communications Mode

Selects the operating mode of the SATURN. If the SATURN is in error control mode and S36 is not equal to 0, it will automatically fallback to asynchronous operation when communicating with a modem that does not support error control.

&Q0 Asynchronous mode.

&Q1 Synchronous mode 1.

&Q2 Synchronous mode 2.

&Q3 Synchronous mode 3.

&Q4 Asynchronous direct mode.

&Q5 MNP error control mode.

&Q6 V.42 error control mode.

&Q7 V.42 error control only (overrides S-register S36).

Synchronous Mode 1 : This mode is used for terminals which communicate both synchronously and asynchronously over the same port. The SATURN initiates a call in asynchronous mode using the standard dial commands and switches to synchronous operation once a connection has been established. Striking a key during dialing will abort the call and return the OK prompt. If the key is pressed after dialing but before the connect message, the NO CARRIER message is displayed.

Once a connection has been established, the SATURN ignores the state of DTR for a period set by the value of S25 in seconds. After the pause, if the SATURN identifies DTR as being ON, the SATURN enters the synchronous state and data transfer can start. If DTR is identified as being OFF for the period of time specified by S25 in milliseconds, the SATURN disconnects and returns to the asynchronous command state. It will disconnect if &D is set to either &D0, &D2 or &D3. When set to &D1 if DTR is OFF, the SATURN enters asynchronous on-line command mode.

Synchronous Mode 2 : This mode is for synchronous terminals or asynchronous computers with a synchronous card. In this mode, when DTR OFF-to-ON transition is detected, the SATURN automatically dials the number stored in position 0. When DTR ON-to-OFF is detected for a period longer than the value contained in S25, the SATURN hangs up and returns to asynchronous command mode. If the carrier is lost for a period of time longer than the value contained in S10, the SATURN hangs up and returns to asynchronous command mode. In synchronous mode 2 the DTR setting selected with the &D command is ignored.

Synchronous Mode 3 : This mode is used with either synchronous terminals or asynchronous computers with a synchronous card. Mode 3 is used when there is a need for the call to be placed in "voice" mode and then switched to "data" mode. The operator manually dials the required number and then switches the SATURN to data mode by turning DTR ON. When carrier is lost for a period of time longer than the value contained in S10, the SATURN exits the synchronous on-line state and returns to asynchronous command state. When DTR ON-to-OFF is detected for a period longer than the value contained in S25, the SATURN hangs up and returns to asynchronous command mode. In synchronous mode 3 the DTR setting selected with the &D command is ignored.

&R : Clear to Send (When in Synchronous On-Line State)

Defines the state of the CTS signal while the SATURN is on-line in synchronous mode.

&R0 CTS is OFF whenever RTS is OFF. When RTS goes ON, CTS goes ON after a delay defined by S26. This is the normal setting for full duplex synchronous operation.

&R1 CTS remains ON whenever the SATURN is on-line.

&S : Data Set Ready Options

Defines how the DSR signal is handled by the SATURN.

&S0 DSR is always ON.

&S1 DSR is compatible with ITU-T recommendations. In command mode DSR is OFF. When originating a call DSR is forced ON when the SATURN receives 2100Hz (or 2225Hz) answer tone, or (if this is absent) when valid carrier is detected. When answering a call DSR is forced ON during handshaking as defined by V.25.

&T : Test Commands

&T0 Test currently in progress is terminated.

&T1 Local analog loopback test is initiated (ITU-T V.54).

&T3 Local digital loopback test is initiated.

&T4 Allows SATURN to respond to a request (from remote modem) for a Remote Digital Loopback.

&T5 Prohibits the SATURN from granting a request from the remote modem for a Remote Digital Loopback.
&T6 Remote digital loopback test (ITU-T V.54) when on-line.
&T7 Not implemented.
&T8 Not implemented.
&T9 Enable test with 140 and 141 signals of the V.24 interface.
&T10 Disable test with 140 and 141 signals of the V.24 interface.

&U : Data Compression

&U0 Data compression disabled.
&U1 Data compression enabled. This command is only meaningful when the SATURN is set to &Q5, &Q6, &Q7, \N2, \N3, \N4, \N5, \N6 or \N7.

&V : Display Configuration

Causes the SATURN to display the its current configuration of AT commands.

&V0 Displays the active configuration, stored profiles 0 and 1 as well as the first 3 stored phone numbers.
&V1 Displays stored profiles 2 and 3 as well as the first 4 stored phone numbers.

&W : Write a Profile to Memory

The SATURN's active configuration is stored in the non-volatile memory as Profile 0, 1, 2 or 3.

&W0	User profile	0.
&W1	User profile	1.
&W2	User profile	2.
&W3	User profile	3.

&X : Synchronous Clock Source

Defines the source of the transmit clock when the SATURN is operating in synchronous mode.

&X0 Internal.
&X1 External (from RS-232 (V.24) interface).
&X2 Slave receive. The SATURN uses its receiver derived clock to drive the modulator.

&Y : Recall Preset Configuration on Power Up

The profile stored under &W0, &W1, &W2 or &W3 can be assigned as the default profile which is automatically installed on power up.

&Y0	Designate user profile	0.
&Y1	Designate user profile	1.
&Y2	Designate user profile	2.
&Y3	Designate user profile	3.

&Z : Store Number Command

Store the desired telephone number in location 0 through 9. The maximum length of each stored number is 36 digits. The format of the stored number is identical to that accepted by the D command.

&Zn = x stores telephone number "x" in position n.
&Zn? displays the telephone number stored in position n.

III.3 - "\" and "%" Style Commands

The "\" and "%" commands supported by the SATURN follow :

%A : Auto-Reliable Fallback Character

n = 0-127ASCII (same effect as changing S46)

%C : Data Compression (same as &U command)

%C0 Compression Off (same as &U0).
%C1 Compression On (same as &U1).

%D : Disposition of Buffered Data upon Hang up

%D0 Hang up without clearing buffer.
%Dn Wait for receive buffer to be sent to DTE before hanging up. n = number of seconds to wait (same as S38).

%En : Fixed Compromise Equalizer

%E0 Fixed compromise equalizer disabled.
%E1 Enables fixed compromise equalizer 1 (3 dB).
%E2 Enables fixed compromise equalizer 2 (6 dB).

%H - PTT Testing Utilities

Facilities PTT testing of signal levels by providing continuous signals regardless of whether the modem is connected or not. The signal transmitted is in accordance with the parameter provided.

This is a range of commands that allow the user to initiate a series of signals that are necessary for PTT approval. The signals emitted include answer tone, modulation, carriers, and other pertinent signals. A test is initiated upon receipt of an %H, and the test is aborted when a ATH command is entered. The modem will continuously transmit the tone or carrier according to the parameter supplied and to S35 output level (except for DTMF tones).

%H0-%H9 DTMF tone dial digits 0 to 9.
%H10 DTMF digit *.
%H11 DTMF digit A.
%H12 DTMF digit B.
%H13 DTMF digit C.
%H14 DTMF digit #.
%H15 DTMF digit D.
%H16 V.21 channel 1 mark (originate) symbol.
%H17 V.21 channel 2 mark symbol.
%H18 V.23 backward channel mark symbol.
%H19 V.23 forward channel mark symbol.
%H20 Not used.

%H21 V.22 originate (call mark) signalling at 1200 bps.
%H22 V.22 bis originate (call mark) signalling at 2400 bps.
%H23 V.22 answer signalling (guard tone if selected).
%H24 V.22 bis answer signalling (guard tone if selected).
%H25 V.21 channel 1 space symbol.
%H26 V.32 9600 bps.
%H27 V.32 bis 14400 bps.
%H28 V.21 channel 2 space symbol.
%H29 V.23 backward channel space symbol.
%H30 V.23 forward channel space symbol.
%H31 Silence (on-line), i.e., go off-hook.
%H32 V.25 answer tone.
%H33 1800 Hz guard tone.
%H34 V.25 calling tone (1300 Hz).
%H35 Fax calling tone (1100 Hz).
%H36 V.21 channel 2 half duplex (for Fax application).
%H37 V.27 ter 2400 bps.
%H38 V.27 ter 4800 bps.
%H39 V.29 7200 bps.
%H40 V.29 9600 bps.
%H41 V.17 7200 bps long train.
%H42 V.17 7200 bps short train.
%H43 V.17 9600 bps long train.
%H44 V.17 9600 bps short train.
%H45 V.17 12000 bps long train.
%H46 V.17 12000 bps short train.
%H47 V.17 14400 bps long train.
%H48 V.17 14400 bps short train.
%H49 V.32 - 4800.
%H50 V.32 - 9600.
%H51 V.32 bis - 4800.
%H52 V.32 bis - 7200.
%H53 V.32 bis - 9600.
%H54 V.32 bis - 12000.
%H55 V.32 bis - 14400.
%H56 V.21 channel 2 carrier detection.
%H57 V.27ter 2400 bps carrier detection.
%H58 V.27ter 4800 bps carrier detection.
%H59 V.29 7200 bps carrier detection.
%H60 V.29 9600 bps carrier detection.
%H61 V.17 7200 bps carrier detection.
%H62 V.22 originate carrier detection at 1200 bps.
%H63 V.17 9600 bps carrier detection.
%H64 V.22bis originate carrier detection at 2400 bps.
%H65 V.17 12000 bps carrier detection.
%H66 V.22 answer carrier detection at 1200 bps.
%H67 V.17 14400 bps carrier detection.
%H68 V.22bis answer carrier detection at 2400 bps.

Note : The short train V.17 commands generates first a long train followed by 2 seconds of data mode, then a short train after 1 second of idle state.

For carrier detection measurements, the connection must be done with a remote modem by typing the proper %H command as described in the following table, and then modifying the line attenuation. The 109 V.24 line follows the carrier detection status.

In FSK modes, mark and space signaling can be inverted in order to make exhaustive measurements. (see table 1)

Table 1

Local Modem			Remote Modem		
Mode	**Command**	**Measurement**	**Mode**	**Command**	**Measurement**
V.21 ch 1 mark	%H16	valid (ch 2)	V.21 ch 2 mark	%H17	valid (ch 1)
V.21 ch 1 space	%H25	valid (ch 2)	V.21 ch 2 space	%H28	valid (ch 1)
V.23 b. ch mark	%H18	valid (f. ch)	V.23 f. ch mark	%H 19	valid (b. ch)
V.23 b. ch space	%H29	valid (f. ch)	V.23 f ch space	%H30	valid (b. ch)
V.22 originate	%H62	valid (high ch)	V.22 answer	%H66	valid (low ch)
V.22bis originate	%H64	valid (high ch)	V.22bis answer	%H68	valid (low ch)
V.21 ch 2 hd (fax)	%H56	valid	V.21 ch 2 hd (fax)	%H36	invalid
V.27ter 2400 bps	%H57	valid	V.27ter 2400 bps	%H37	invalid
V.27ter 4800 bps	%H58	valid	V.27ter 4800 bps	%H38	invalid
V.29 7200 bps	%H59	valid	V.29 7200 bps	%H39	invalid
V.29 9600 bps	%H60	valid	V.29 9600 bps	%H40	invalid
V.17 7200 bps	%H61	valid	V.17 7200 bps	%H41	invalid
V.17 9600 bps	%H63	valid	V.17 9600 bps	%H43	invalid
V.17 12000 bps	%H65	valid	V.17 12000 bps	%H45	invalid
V.17 14400 bps	%H67	valid	V.17 14400 bps	%H47	invalid

%K : V42/MNP Window Size

%Kn Maximum window size. 1<n<15.

%L : Line Signal Level Options

%L0 Return received line signal level in dB.

%L1 Return data pump's line status report.

%P : Negative ADP Selected

%P0 Disabled.

%P1 Enabled (only when normal mode selected, &Q0, \N0).

%Qn : Ignore Keyboard Abort On Answer

%Q0 Disabled.

%Q1 Enabled.

%R : Attempt to use CRC-32 When in V42

%R0 Disabled.

%R1 Enabled.

%S : Attempt to use Selective Reject When in V42

%S0 Disabled.

%S1 Enabled.

%T : Attempt to Negotiate Ability to Send Loop-back Test Frames When in V42

%T0 Disabled.

%T1 Enabled.

When negotiation succeeds after a V42 connection, a user can enter the command AT & T6 to test the line integrity. The SATURN will report test passed or test failed.

%V : V25 bis Selection

Speed as per S23 bits 3, 2, 1 and S39 bits 3,2.

%V0 AT command set.

%V1 V25 bis command set asynchronous.

%V2 V25 bis command set synchronous BSC.

%V3 V25 bis command set synchronous HDLC (NRZ).

%V4 V25 bis command set synchronous HDLC (NRZI).

%W :Acknowledgment Timer (T401)

%Wn Wait to retransmit time out. 0<n<63
T401 = 4 seconds + n x 100 ms.
exception when in MNP mode :
if n = 0 = use Microcom timers.
if n = 63 = use ITU-T V42 Annex A timers.

%Y : MNP Synchronous/Asynchronous

%Y0 Use synchronous mode when possible.

%Y1 Always use asynchronous mode.

\A : Error Correction Maximum Block Size

\A0 Sets maximum block size for error correction to 64 characters.

\A1 Sets maximum block size for error correction to 128 characters.

\A2 Sets maximum block size for error correction to 192 characters.

\A3 Sets maximum block size for error correction to 256 characters.

\B : Send Break (In On-Line Command Mode Only)

Bn Causes a break to be sent to the remote modem. The parameter "n" (0-9) is the break duration in 100s of milliseconds. If n is 0 or omitted, a 300 millisecond break will be sent.

\C : Data Buffering During Error Corrected Link Negotiation

Determines how the SATURN will process incoming data from the remote modem while trying to negotiate an error corrected link.

\C0 Does not buffer data during error corrected link negotiation and does not recognize the fallback character specified by the %A command or S46.

\C1 Buffers all data until 128 characters are received but does not recognize the fallback character.

\C2 Buffered data until 128 characters are received or until it detects the fallback character.

\G : Modem-to-Modem Flow Control During a Normal Connection

\G0 No modem-to-modem flow control.

\G1 Use modem-to-modem software flow control (XON/XOFF).

\J : Automatic DTE Speed Adjust

\J0 Serial port rate is not adjusted to the connection rate (same as &B1).

\J1 Speed of the serial port is matched to the speed of connection (same as &B0).

\K : Break Handling

\K1 The break is expedited and destructive. The break causes the data buffers at both ends to be cleared and the break is immediately passed through.

\K3 The break is immediately passed through without buffering by either modem (non-destructive/expedited).

\K5 The break is sent in sequence with the received data (non-expedited, non-destructive).

\N : Operational Mode

\N0 Buffered or Normal asynchronous mode.

\N1 Direct mode.

\N2 Reliable MNP.

\N3 Auto-reliable MNP (fallback to non error correction).

\N4 Reliable V.42.

\N5 Auto-reliable V.42 (fallback to non error correction).

\N6 Reliable V.42/MNP.

\N7 Auto-reliable V.42/MNP (fallback to non error correction).

\S : Display Configuration

\S0 Same as &V0.

\S1 Same as &V1.

\V : Extended Result Codes

\V0 Suppress extended result codes (same as W0).

\V1 Enable extended result code (same as W2).

\Y : Attempt Error Corrected Link (On Line Command Mode Only)

The modem will attempt to establish an error corrected link when this command is issued if the modem has already made a connection in either normal or direct mode.

\Z : Terminate Error Corrected Link (On Line Command Mode Only)

The modem will attempt to switch to normal mode if a reliable link is currently active. This also will cause the remote modem to attempt this switch. Any data in the buffer at this time may be lost.

III.4 - Facsimile AT Commands Supported by the SATURN

This section describes the extended AT commands, implemented in the SATURN, that are used to support the transmission and reception of facsimile files. Commands discussed in EIA/TIA standard 578 (Fax Class 1) and the Class 2 Fax command set are given here.

General Comments on Fax AT Commands

All commands require the AT prefix and are generally entered in the same way as the data modem AT commands (see the discussion at the beginning of the previous section for a detailed description of how commands are entered).

All commands except "+FTS" and "+FRS" support a syntax of the form "+<COMMAND>X" where X may be any of three different strings. The string "=" is used to provide a value for execution by the command. The string "=?" is used to interrogate the command as to its range of acceptable values (i.e. the command returns a string of comma-separated values that are those that can be provided to the command via the "=" string). The string "?" is used determine the value for that command that is currently in use.

All commands except "+FCLASS" cause a command processing error if received when the SATURN is on hook.

The transmit and receive facsimile commands require a modulation parameter <MOD>. Below is a list of the possible values of <MOD>:

<MOD>	Modulation Type	Speed (bps)
3	V.21 ch.2	300
24	V.27 ter	2400
48	V.27 ter	4800
72	V.29	7200
73	V.17	7200
74	V.17w/st	7200
96	V.29	9600
97	V.17	9600
98	V.17w/st	9600
121	V.17	12000
122	V.17w/st	12000
145	V.17	14400
146	V.17 w/st	14400

III.5 - Fax Class 1 Commands

+FCLASS : Identify Service Class

This command selects whether the SATURN is configured as a data or fax modem.

+FCLASS=0 SATURN configured as data modem.

+FCLASS=1 SATURN configured as Class 1 fax modem.

+FCLASS= 2 SATURN configured as Class 2 fax modem.

+FTS : Stop Transmission and Wait

Transmission is halted followed by a wait for the specified time.

+FTS=<TIME> Wait for the time (in increments of 10 ms) specified by <TIME> (0 - 2.55s).

+FRS : Receive Silence

This command completes execution when silence is detected from the remote modem for the specified amount of time. Processing of the command is aborted, without error, if a character is received from the DTE while attempting to detect the period of silence.

+FRS=<TIME> Wait for the time (in increments of 10 ms) specified by <TIME> (0 - 2.55s).

+FTM : Transmit Facsimile Data

A physical connection with the modulation type specified by <MOD> is first established. Data received from the DTE is then transmitted in facsimile format.

+FTM=<MOD> Transmit facsimile data using modulation <MOD>.

+FRM : Receive Facsimile Data

A physical connection with the modulation type specified by <MOD> is attempted with the remote modem. If this succeeds, data subsequently received from the remote modem is sent to the DTE in facsimile format. If the physical connection fails, the "+FCERROR" result code is returned.

+FRM=<MOD> Receive facsimile data using modulation <MOD>.

+FTH : Transmit Facsimile Data HDLC

A physical connection with the modulation type specified by <MOD> is first established. Data received from the DTE is then transmitted in facsimile format using HDLC framing.

+FTH=<MOD> Transmit facsimile data, HDLC format, using modulation <MOD>.

+FRH : Receive Facsimile Data HDLC

A physical connection with the modulation type specified by <MOD> is attempted with the remote modem. If this succeeds, data subsequently received from the remote modem, using HDLC framing, is sent to the DTE in facsimile format. If the physical connection fails, the "+FCERROR" result code is returned.

+FRH=<MOD> Receive facsimile data, HDLC format, using modulation <MOD>.

III.6 - Class 2 Commands

+FAA : Data/Fax Auto Answer

+FAA command configure the modem to automatically detect whether an incoming call is from a data modem or a fax modem.

+FBOR : Phase C Data Bit Order (Short form : +FBO)

This command controls the bit order for phase C.

+FBOR = 0 Select direct bit order for phase C.
+FBOR = 1 Select reversed bit order for phase C.

+FBUG : Debug Mode HDLC Frame (Short form : +FBU)

This command enables the DCE to report the content of the HDLC frames to the DTE.

+FBUG = 0 Disables HDLC frame reporting.
+FBUG = 1 Enables HDLC frame reporting.

+FDCC : Establish DCE Capabilities (Short form : +FCC)

This command allows the DTE to sense and constrain the capabilities of the facsimile DCE, from the choices defined in ITU-T T.30 Table 2. When the values of +FDCC are modified the DCE will copy +FDCC into +FDIS.

+FCQ : Copy Quality

This parameter controls copy quality checking by the DCE.

+FCQ = 0 The DCE does no copy quality checking.
+FCQ = 1 Copy Quality checking enable.

+FCR : Capability to Receive

Indicates if the DCE can receive a message.

+FCR = 0 The DCE can not receive a message. This option can be used when the DTE has insufficient storage.
+FCR = 1 The DCE can receive a message.

+FDCS : Current Session Parameters (Short form : +FCS)

The +FDCS is loaded with the negotiated T.30 parameters for the current session. A DCS is generated by the DCE every time that the unit is transmitting. This parameter is initialized to 0,0,0,0,0,0,0,0 at the beginning of a session. +FDCS is a read only command.

Syntax : +FDCS : VR, BR, WD, LN, DF, EC, BF, ST

+FDR : Receive a Page

This command initiates transition to phase C data reception.

+FDT : Send a Page

In phase B, the +FDT command releases the DCE to proceed with negotiation, and release the DCS message to the remote station. In phase C, the +FDT command resume transmission after the end of a prior transmit facsimile data.

+FET : End the Page or Document

The DCE uses this command in transmission mode to tell the DCE if any additional pages are to be sent.

+FET = 0 Another page is following, send MPS to the remote modem.

+FET = 2 No more pages are expected, send EOP to the remote modem.

+FHPS : Handshake Protocol

+FHPS = 0 Send "OK" to the DTE.

+FHPS = 1 Send "ERROR" to the DTE.

+FDIS : Current Session Negotiating Position (Short form : +FIS)

The +FDIS parameter allows the DTE to sense and constrain the capabilities used for the current session. The DCE uses +FDIS to generate DIS or DTC frames, and uses +FDIS and the received DIS frame to generate the DCS frame (transmission mode).

+FLID : Local FAX Station ID String (Short form : +FLI)

+FLID contains the local telephone number transmitted in the CSI frame to the remote modem.

+FMINSP : Minimum Phase C Speed (Short form : +FMS)

This parameter limits the lowest negotiable speed for a session. This parameter is useful for limiting the cost of a transmission. If the facsimile cannot negotiate to the minimum speed it will disconnect.

+FPTS : Page Transfer Status (Short form : +FPS)

The +FPTS parameter contains a value representing the post page response, including copy quality and related end-of-page status.

+FPTS = 1 An MCF frame has been received. (page good).

+FPTS = 2 An RTN frame has been received. (page bad).

III.7 - Class 2 Responses

+FCON : Connection Response (Short form : +FCO)

Indicates a connection with a fax machine. +FCON message is released when the unit receives the beginning of the first HDLC frame.

+FTSI : Report the Remote ID (Short form : +FTI)

The message +FTSI reports the received remote string sent in the TSI frame.

Syntax : +FTSI : "<TSI ID string>"

+FCSI : Report the Remote ID (Short form : +FCI)

The message +FCSI reports the received remote string sent in the CSI frame.

+FDCS : Report the Negotiated Parameters (Short form : +FCS)

This message will be generated during the execution of +FDT or +FDR commands, before the CONNECT result code, if new DCS frames are generated or received. The codes are given in the table 8.4 of the class 2 EIA standard proposal.

Syntax : +FDCS : VR, BR, WD, LN, DF, EC, BF, ST

+FET : Post Message Response

This message is generated by the facsimile DCE after the end of Phase C reception. The +FET is generated during the execution of a +FDR command. The parameter received tell the DCE which post message command the unit had received.

+FET : 0 A MPS frame has been received.

+FET : 2 A EOP frame has been received.

+FDIS : Report Remote Facsimile Station Capabilities (Short form : +FIS)

This message will be generated during the execution of +FDT or +FDR commands. This message is sent when the unit is receiving a DIS frame, and contains the capabilities of the remote station. The codes are the same as the +FDCS response.

Syntax : +FDIS : VR, BR, WD, LN, DF, EC, BF, ST

+FHT : Report Transmit HDLC Frames

This message is generated when +FBUG = 1 and when a HDLC frame is transmitted. This response shows the frame transmitted to the remote station.

Syntax : +FHT : <Address><control><fis><fif1><fif2>...

+FHR : Report Received HDLC Frame

This message is generated when +FBUG = 1 and when a HDLC frame has been received. This response shows the frame received by the DCE.

Syntax : +FHR : <Address><control><fis><fif1><fif2>...

+FPTS : Page Transfer Status Response (RX and TX) (Short form : +FPS)

The +FPTS message is generated by the DCE at the end of Phase C data reception, during the execution of a +FDR command. The first parameter <ppr> is generated by the DCE ; it depends on the DCE capability at T.4 error checking controlled by the +FCQ parameter. The second and the third parameters are generated only in the reception mode, and represent the total number of lines and the bad line count.

Syntax : +FPTS : <ppr>,<lc>,<blc>

+FNSF : Report Received Non Standard Negotiation Frame (Short form : +FNS)

This response indicates the reception of a NSF frame. The information of the frame is transmitted after the +FNSF response.

Syntax : +FNSF : <1><2><3><4>...

+FNSC : Report Received Non Standard Negotiation Frame (Short form : +FNC)

This response indicates the reception of a NSC frame. Same as the +FNSF frame.

III.8 - Description of the Autologon Facility

Autologon : Modem security

The SATURN has the ability to store Autologon sequences in conjunction with the numbers stored with the &Z = n command (n = 0 to 9). The SATURN can be instructed to execute this sequence when originating or auto-answering a call. The sequence consists of a number of Transmit and Receive fields, limited only by the size of the SATURN's dial input buffer (70 characters).

Inputting an Autologon Sequence

Storing an Autologon sequence should be done as follows :

Type : AT&Zn = xxx.

Where n is the Autologon number and xxx is a phone number if desired. Enter all desired Transmit, Receive, or Command fields.

Transmit fields are prefixed with "Control T".

Receive fields are prefixed with "Control R".

Command fields are prefixed with "Control C" (always last).

To complete the storing of the Autologon sequence, simply hit the "Enter" key. Investigation of the logon sequence stored in location n can be accomplished by typing : AT&Zn?<CR>

Autologon Operation

If the first logon field is a transmit field it will be transmitted and the SATURN will look for a response corresponding to the first receive field. When this is received the next transmit field (if any) is transmitted. This procedure can be repeated.

If the first logon field is a receive field, the SATURN waits for the message to be received from the remote before transmitting the first transmit field.

The SATURN starts a thirty second timeout when it enters the receive message state; if the expected message is not received within this period, the SATURN outputs :

AUTO-LOGON FAILED

and disconnects the call.

In originate mode the logon sequence is executed using ATDSn or ATDS = n where n is the desired stored sequence. When the number has been dialled and the call connected, the SATURN will enter the logon sequence.

To cause the SATURN to use a logon sequence when answering a call, register S34 must be set the required stored sequence with the command :

ATS34=n (n=0 to 9)

Typing ATS34 = 0 will disable the answer Autologon (Only 9 Autologon sequences are available in answer mode).

In answer mode the stored phone number associated with the chosen sequence is ignored.

Control Characters

A carriage return may be entered into any field by typing : ^A (Control A).

The SATURN's response is : (Return).

If the logon fields include control characters, they must be entered as Hex values. Any Hex value can be entered into a field by typing :

^Xnn (Control X)nn.

Where nn is a two digit hex code. The SATURN will echo : (HEX) nn.

A pause can be entered, anywhere in the Transmit fields, with : ^P (Control P).

The SATURN's response is : (PAUSE).

To allow the SATURN to execute an AT command, the character : ^C (Control C).

must be entered as the last control character in an Autologon sequence.

Example of Autologon as Call Back Security

Set up answer SATURN as follows :

Step	Typed by User	Echoed to Screen
1.	ATS0=1<CR>	ATS0=1<CR><CR><LF>
2.	ATS34=2<CR>	ATS34=2<CR><CR><LF>
3.	AT&Z2=^T	AT&Z2=<CR><LF> (Transmit)
4.	Password? ^R	Password? <CR><LF>(Receive)
5.	MONIQUE^C	MONIQUE<CR><LF> (Command)
6.	HDT7470254<CR>	ATHDT7470254<CR> <LF>OK

Step 1. Sets the SATURN to answer after 1 ring.

Step 2. Instructs the SATURN to use Autologon sequence #2 in answer mode.

Step 3. Entering of Auto logon sequence begins. Transmit field is requested.

Step 4. Desired transmit field is "Password? ". This is entered and Receive field is requested.

Step 5. Desired receive field is "MONIQUE". This is entered and Command field is requested.

Step 6. Desired command field is "HDT7470254". This is entered and Autologon configuration mode is ended.

Once one ring is detected and the SATURN has passed through the handshaking process and entered error correction mode if necessary, this Autologon sequence will perform the following task : when the SATURN is programmed with the above sequence, it will execute Autologon Sequence #2 and transmit the string "Password?". It then waits for the calling modem to reply with the string "MONIQUE". When this string is received the SATURN will perform the AT command requested in the command field, (i.e. HDT7470254<CR>). The effect of this command is to cause the SATURN to hang up and tone dial the line with the specified phone number. If any error occurs during the process of the receive field the SATURN will hang up and display AUTOLOGON FAILED.

IV - V.25BIS COMMANDS

Modem operation may be controlled through the use of the V.25 bis command set. This is implemented by command, response and circuit signalling providing addressed call and/or answer via circuit 108/2 in accordance with V.25 bis. V.25 bis is a ITU-T recommendation that defines a method of exchanging commands and indications across a DTE interface (RS232/V.24). V25bis defines modem behaviour only while the modem is off-hook and is attempting to establish a connection. The following terms are used in the V.25bis description.

COMMAND : An instruction issued by the DTE to the modem as part of the automatic calling procedure.

INDICATION : A response message issued by the modem to the DTE as part of the automatic calling procedure.

PARAMETER : A variable which may accompany commands or indications. In general, more than one parameter may be used in a command or indication.

Formats for Commands and Indications

The modem will accept commands either in synchronous mode HDLC (NRZ or NRZI), BSC or in asynchronous mode (%Vn command).The command set conforms to the ITU-T recommendation with two extension for asynchronous mode.

Synchronous Signalling

HDLC Frames, Commands and indications are HDLC frames with data fields called messages.

FLAG	HEX "7E"
ADDRESS	HEX "FF"
CONTROL	HEX "13"
MESSAGE	Data. Must be an integer number of 8 bit characters between 3 and 60.
FCS	Sixteen bit cyclic redundancy check based on the polynomial : X16 + X12 + X5 + X1

Synchronous Framing Rules

Framing may be preceded and followed by any data including additional flags.

A Frame with an address, control, or FCS field error is invalid. A frame with more than 125 characters in the message field is invalid. A frame with 3 or less characters in the message field is rejected with the INV indication.

Invalid frame frames are ignored.

For every valid command frame received, the modem responds with exactly one indication.

When the modem receives a valid command frame, it will ignore another command frame until it has completed sending its indication back to the attached DTE or until the connection is terminated whichever occurs last.

The modem can accept a valid command frame that follows an invalid frame if there is a pause of at least 2 bits time between the end of the invalid frame and the start of the valid frame.

Command and indication frames contain inserted zero bits as required by HDLC. The receiving entity (modem or DTE) must strip out these extra bits.

BSC Frames

The format for synchronous character oriented format shall be in accordance with ISO 1745.

SYN	HEX "16"
SYN	HEX "16"
STX	HEX "02"
MESSAGE	Data. Must be an integer number of 8 bit characters between 3 and 60. (ASCII 7 data bits, odd parity).
ETX	HEX "83"

BSC Framing Rules

Framing may be preceded and followed by any data including additional SYN characters.

A Frame with a parity error is invalid. A frame with more than 123 characters in the message field is invalid. A frame with 3 or less characters in the message field is rejected with the INV indication.

Invalid frame frames are ignored.

For every valid command frame received, the modem responds with exactly one indication if the connection is not completed and no indication if the connection is completed. The modem does not recognize or send any of the short "ack" type messages used in character oriented protocols.

When the modem receive a valid command frame, it will ignore another command frame until it has completed sending its indication back to the attached DTE or until the connection is terminated whichever occurs last.

The modem can accept a valid command frame that follows an invalid frame if there is a pause of at least 2 bit times between the end of the invalid frame and the start of the valid frame.

Asynchronous Signalling

The format for asynchronous character oriented format shall be the following :

MESSAGE <CR><LF>

The default data rate for commands and parameters will be the maximum data rate permitted by the modem recommendation.

The message field can contain between 3 and 60, 8 bit (as per the AT command format) which define the parameters. Each frame can contain only one command followed by as many parameters that will fill the limit.

Command/Indication Exchange Protocol

The modem will ignore a command issued from the DTE before it has completed execution of the previous command and given an appropriate response. The modem will ignore a command from the DTE while it is sending an indication to the DTE.

A command received with a message field of less than 3 characters or more than 60 characters is regarded as an error in the message and will result in the negative acknowledgment of the command by the return of the invalid message (INV).

DTE Adaptation

In asynchronous mode, the modem uses the speed stored in S23. The modem then accepts and sends characters according to this selection of speed, parity and length.

The following commands are implemented. Parameters applicable to each command are noted following the description of the command.

IV.1 - Standard V.25bis Commands

CIC : Connect Incoming Call

The modem will go on line in answer mode, canceling any DIC command previously issued. If no incoming call is present the modem will issue the INV message.

CRN : Call Request with Number

The modem will go on line, dial according to the dial string entered and attempt to establish a connection.

0-9	Digit 0 to 9.
A,B,C,D	Digit A, B, C and D : tone dialing only.
*	The "star" digit : tone dialing only.
#	the "gate" digit : tone dialing only.
T	Select tone dialing : affects current and subsequent dialing.
P	Select pulse dialing : affects current and subsequent dialing.
<	Short dial pause : period controlled by S8 : the modem will pause before dialing the digits following "<".
=	Long dial pause : period twice as long as the short dial pause.
:	Wait for dial tone : the modem will wait for dial tone before dialing the digits following ":".
&	Flash : causes the modem to go on-hook for .5 sec and then off-hook for .5 sec.
@	Wait for silence : the modem will wait for 5 sec of line silence before dialing the digits following "@".

CRS : Call Request with Memory Address

The modem will go on-line, dial according to the dial string entered in the dial string memory addressed and attempt to establish a connection.

0-9	Dial string memory address.

DIC : Disregard Incoming Call

The modem, though configured for auto-answer will disregard the incoming call. If there is no incoming call or auto-answer is not enabled the modem will issue the invalid message, the command not being applicable to the subsequent calls.

PRN : Program Normal

The modem will store the dial string specified into the dial string memory referenced.

0-9 Dial string memory address.

; Separator : inserted between dial string memory address and dial string.

x..x Dial string : a string of dial characters : 0-9AD* # T P< = &@ : characters accepted : an empty string clears the identification memory referenced.

RLN : List Request of Stored Numbers (Dial Strings)

The modem will return the dial string or the list of dial strings according to the parameter supplied.

0-9 Dial string memory address : if no address is supplied a full list of all stored dial string will be returned

The modem provides the indication/responses listed. Parameters applicable to each message are noted following the description of the response.

IV.2 - Standard V.25bis Indications

CFI : Call Failure Indication

The modem will send this message when a call fails to connect. A parameter is included to give the reason for the failure.

AB No dial tone.

ET Busy detected.

NT Aborted; handshaking failure or loss of carrier.

RT Ringback detected.

NS Number requested not stored.

CNX : Connect Indication

This gives an indication of the line speed.

CNX 300
CNX 75TX/1200RX
CNX 1200TX/75RX
CNX 1200
CNX 2400
CNX 4800
CNX 7200
CNX 9600
CNX 12000
CNX 14400

INC : Incoming Call

The modem will send this message when incoming ringing is detected on the line.

INV : Invalid

The modem will send this message if the command line contain a syntax error or it is unable to execute the command.

LSN : List of Stored Numbers (Dial Strings)

The modem will use this message in response to the RLN command.

LSN 4; 19 : 1 = 7470336 response to RLN4

LSN 0; response to RLN
LSN 1;
LSN 2;
LSN 3;
LSN 4; 19 : 1 =7470336
LSN 5;
LSN 6;
LSN 7;
LSN 8;
LSN 9;

VAL : Valid

The modem will send this message when it successfully executes the command issued and there is no other applicable response.

IV.3 - Extended V.25bis Command Set

There is one extension to the V.25bis command set.

CNL : Local Configuration

Any AT command string may be entered as a parameter of this command (e.g. CNLS0 = 2).

IV.4 - V.25bis Escape Sequence

An escape sequence function for V.25bis asynchronous operation is provided which operates exactly as the AT escape sequence.

V - S-REGISTERS

S-registers are byte-wide locations in SATURN memory that contain information about the configuration and operational status of the SATURN.

Many of the SATURN's options can be directly set via the S-registers and some extended features are only available through setting of these registers. Examples of this are S35 which is used to select the transmit level and S41 which selects the number of re-dial attempts.

Some S-registers are bit-mapped, that is, the individual bits (or, sometimes, groups of bits) contain significant information as opposed to the contents of the register as a whole. When references to bit-mapped registers are made, the least significant bit is bit 0 while the most significant bit is bit 7.

V.1 - Reading an S-register

To display the value of an S-register in decimal format the command Sn? is used where "n" references the desired register. To display an S-register's value in hexadecimal format, use the Sn! command.

V.2 - Writing an S-register

An S-register's value may be altered by the Sn = X command where "n" is the register to be changed and "X" is the new decimal value to be assigned to it.

V.3 - Defaults

Entering AT! or AT? will display the content on the last register accessed while AT = n will alter the last accessed S register with the decimal value "n".

If the Sn = X command is used and the value "X" is not given, zero will be written to the appropriate S-register.

Any value of "n" or "X" is evaluated modulo 256 before any command processing takes place (i.e. the remainder of the expression [n or X] / 256 is the actual value of "n" or "X" used by the SATURN.

Unless otherwise specified, any value between 0 and 255 (decimal) may be written to an S-register. Out of range values are rejected and cause a command processing error.

Writing a value to an S-register designated as "reserved" (see below) will place that value in the register but has no effect on the SATURN's operation.

Reading an S-register "n" where "n" is 50 or greater will always return zero. Attempting to write such a register causes a command processing error.

V.4 - S-Register Descriptions

The complete set of S-registers is listed below with the corresponding bit maps where applicable.

All values are in decimal format. Default values indicated in bold type are those written after execution of the &F0 command. If the register TYPE is non-storable then this default value will also be written whenever the SATURN is reset. For storable register, however, the value after reset will be set to that stored in the appropriate stored profile.

Any register not specifically mentioned below is reserved.

S0 : Ring To Answer On

0 = No auto answer

Any other = SATURN answers after this number of rings

Default = 0

TYPE : Storable

S1 : Ring Count

This register is reset to 0 if 8 seconds elapse since receipt of the previous ring

Default = 0

TYPE : Non-Storable

S2 : Escape Sequence Character

If the value is greater than 127, escape sequence is disabled.

Default = 43 (+)

TYPE : Non-Storable

S3 : Carriage Return Character

Value : 0 - 127

Default = 13 (ASCII CR)

TYPE : Non-Storable

S4 : Line Feed Character

Value : 0 - 127

Default = 10 (ASCII LF)

TYPE : Non-Storable

S5 : Backspace Character

Value : 0 - 255

Default = 8 (ASCII BS)

TYPE : Non-Storable

S6 : Wait Time Before Dialing

Value : 2 - 255 s

Default = 2

TYPE : Storable

S7 : Wait Time For Carrier / Dial Tone

Value : 1 - 255 s

Default = 30

TYPE : Storable

S8 : Duration for Pause (,) Dial Modifier

Value : 0 - 255 s

Default = 2

TYPE : Storable

S9 : Carrier Detect Response Time

Value : 1 - 255 in .1 s increments (.1 - 25.5 s)

Default = 1

TYPE : Storable

S10 : Delay Between Lost Carrier And Hang Up

Value : 1 - 255 in .1 s increments (.1 - 25.5 s)

Default = 14

Note : S10 = 255 implies infinite delay

TYPE : Storable

S11 : DTMF Tone Duration and Silence Time Between Tones

Value : 50 - 255 in 1 ms increments (55 - 255 ms)

Default = 95

TYPE : Storable

S12 : Escape Sequence Prompt Time

Value : 0 - 255 in 20 ms increments (0 - 5.1 s)

0 = Do not check guard time

Default = 50

TYPE : Storable

S14 : Bit-mapped

Bit 0 Reserved

Bit 1 Echo command characters (E CMD)
0 = No echo
1 = Echo

Bit 4,2 Generate result codes (Q CMD)
0 = Enable result codes
1 = No result codes
2 = Result codes enabled only when originate mode in effect

Bit 3 Verbose / numeric result codes (V CMD)
0 = Numeric result codes
1 = Verbose result codes

Bit 5 Tone / Dial (P and T CMD)
0 = Tone dialing (T CMD)
1 = Pulse dialing (P CMD)

Bit 6 Reserved

Bit 7 Answer / Originate
0 = Answer mode
1 = Originate mode

TYPE : Storable

S16 : Test Status (Bit-mapped)

ALB = Analog loopback, DLB = Local digital loopback, RDLB = Remote digital loopback.

Bit 0 ALB (&T1 CMD)
0 = No ALB
1 = ALB active

Bit 1 Reserved

Bit 2 Digital loopback (&T3 CMD)
0 = No DLB
1 = DLB active

Bit 3 Status of DLB initiated by remote mode
0 = No DLB
1 = DLB initiated by remote modem active

Bit 4 Remote digital loopback (&T6 CMD)
0 = No RDLB active
1 = RDLB initiated and granted by remote

Bit 5 RDLB with self test (&T7 CMD)
0 = No RDLB active
1 = RDLB with self test initiated and granted by remote

Bit 6 ALB with self test (&T8 cmd)
0 = No ALB
1 = ALB with self test active

Bit 7 Reserved

TYPE : Non-Storable

S18 : Test Timer

Value : 0 - 255 s

0 = Infinite test time

Any other = Test is terminated after specified time elapses

Default = 0

TYPE : Storable

S21 : Bit-mapped

Bit 0 Reserved

Bit 1 Reserved

Bit 2 CTS control (&R CMD)
0 = CTS follows RTS
1 = CTS always on

Bit 4,3 DTR control (&D CMD)
0 = Ignore
1 = Command state
2 = Hang up
3 = Reset

Bit 5 DCD control (&C CMD)
0 = DCD always on
1 = DCD controlled by SATURN

Bit 6 DSR control (&S CMD)
0 = DSR always on
1 = DSR controlled by SATURN

Bit 7 Long space disconnect (&Y CMD)
0 = Disabled
1 = Enabled

TYPE : Storable

S22 : Bit-mapped

Bit 1,0 Speaker volume control (L CMD)
0 = Low
1 = Low
2 = Medium
3 = High

Bit 3,2 Speaker control (M CMD)
0 = Always off
1 = On until carrier detected
2 = Always on when off hook
3 = Off during dialing and after carrier detected

Bit 6,5,4 Extended response codes (X CMD)
0 = Ignore GSTN status and do not report connection speed - (X0)
1 = Detect busy and ringing tones and report connection speed - (X5)
2 = As for X5 and also detect dial tone and perform adaptive dialing - (X6)
3 = As for X6 - (X7)
4 = As for X0 and also report connection speed - (X1)
5 = Detect dial tone and report connection speed - (X2)
6 = Detect busy tone and report connection speed - (X3)
7 = Detect dial and busy tones and report connection speed - (X4)

Bit 7 Make / break ratio when pulse dialing (&P CMD)
0 = U.S. (39%/61%)
1 = U.K. (33%/67%)

TYPE : Storable

S23 : Bit-mapped

Bit 0 Detect RDLB (&T4 and &T5 CMD)
0 = Deny RDLB (&T5 CMD)
1 = Accept RDLB (&T4 CMD)

Bit 3,2,1 DTE port communications speed (bps)
0 = 300
1 = 57600
2 = 1200
3 = 2400
4 = 4800
5 = 9600
6 = 19200
7 = 38400

Note : bits 3,2 and 1 of S23 are only valid if bit 3 of S39 = 0.

Bit 5,4 Parity
0 = Even
1 = Space / none
2 = Odd
3 = Mark

Bit 7,6 Guard Tone
0 = None
1 = 550Hz
2 = 1800Hz
3 = Not used

TYPE : Storable

S24 : Bit-mapped

Bit 0 Error control fallback character (&N, \C CMD)
0 = No fallback character
1 = Enable fallback character in S46

Bit 1 Error control buffer control (&O, \C CMD)
0 = Don't buffer incoming data during negotiation
1 = Buffer data

Bit 2 Data compression control (&U, %C CMD)
0 = Disable
1 = Enable

Bit 3 Not used

Bit 4 DCE speed to be negotiated during handshake (N CMD)
0 = S37 speed
1 = Optimum speed if S37 ! = 255
Optimum speed up to DTE if S37 = 255

Bit 6,5 Extended connection result code (W, \V CMD)
0 = No extended result code
1 = Hayes extended result code
2 = Microcom extended result code
3 = Not used

Bit 7 DTE speed after handshake completed (&B, \J CMD)
0 = DTE set to DCE speed
1 = DTE speed not changed by DCE

TYPE : Storable

S25 : DTR Detection

Value : 0 - 255 in .01 s or in 1 s increments (0 - 2.55 s or 0 - 255 s) see &D command description

Default = 5

TYPE : Storable

S26 : RTS To CTS Delay

Value : 0 - 255 in .01 s increments (0 - 2.55 s)

Default = 1

TYPE : Storable

S27 : Bit-mapped

Bit 3,1,0 Communication mode (&Q, N CMD)
0 = Normal asynchronous
1 = Sync mode 1
2 = Sync mode 2
3 = Sync mode 3
4 = Direct
5 = MNP
6 = MNP/V.42
7 = V.42

Bit 2 Leased line (&L CMD)
0 =GSTN
1 = Lease line

Bit 5,4 Synchronous transmit clock source (&X CMD)
0 = Internal
1 = External
2 = Derive from receiver (slave)

Bit 6 Bell / ITU-T (B CMD)
0 = ITU-T
1 = Bell

Bit 7 Reserved

TYPE : Storable

S28 : Bit-mapped

Bit 1,0 Error Correction Maximum Block Size (\A CMD)
0 = 64 bytes
1 = 128 bytes
2 = 192 bytes
3 = 256 bytes

Bit 6 to 2 V.42 detection period (T400) in 50 milliseconds increments
0 = Infinite
1 to 155 = (1 to 255) times .05 second
Default = 16 for .8 seconds

Bit 7 ODP/ADP (&A CMD)
0 = Do not use ODP/ADP when initiating a reliable V.42 handshake
1 = Use ODP/ADP when initiating a reliable V.42 handshake

TYPE : Storable

S29 : Bit-mapped

Bits 5 to 0 V.42 acknowledgment timer (T401)(%W CMD) These six bits are interpreted as an integer that specifies the number of 100 millisecond increments which are added to the base value of four seconds in order to arrive at the T401 value. Because of he way it is specified here, the minimum value of T401 is 4 seconds and the maximum value of T401 is 10.3 seconds. The default value is zero which corresponds to a T401 value of 4 seconds.
Default = 0 for 4 seconds

Bit 6 V.42 frame check sequence (%R CMD)
0 = Always use CRC-16
1 = Attempt use if CRC-32

Bit 7 V.42 selective reject (%S CMD)
0 = Disabled
1 = Enabled

TYPE : Stored

S30 : Bit-Mapped

Bits 4 to 0 V.42 windows size (k)(%K CMD) These 5 bits are interpreted as an integer that specifies the maximum number of unacknowledged packets that V.42 and MNP will allow at anytime. Although the bits may be set to any value between 0 and 31 a setting of zero is undefined and should not be used. The default value is 01111 (binary) = 15 (decimal).
Default = 15 packets

Bit 5 Negative ADP (%V CMD)
0 = Disabled
1 = Enabled

Bit 6 Force asynchronous MNP (Class 2)(%Y CMD)
0 = Do not force asynchronous MNP
1 = Force asynchronous MNP

Bit 7 V.42 remote loopback test (%T CMD)
0 = Ignore loopback frame received from remote
1 = Process loopback frame received from remote

TYPE : Storable

S31 : Bit-mapped

Bits 1,0 V.25bis selection (%V CMD)
0 = Asynchronous V.25 (%V1)
1 = Bisync V.25bis NRZ(%V2)
2 = HDLC V.25bis NRZ (%V3)
3 = HDLC V.25bis NRZI (%V4)

Bit 2 Synchronous mode V.13 operation (&C CMD)
0 = Disable
1 = Enable

Bit 3 Ignore keyboard abort on answer (%Q CMD)
0 = Disable
1 = Enable

Bits 6 to 4 Reserved

Bit 7 V.25bis mode (%V CMD)
0 = Disabled (AT commands %VO)
1 = V.25bis enabled as per bits 1,0 (for other than %VO)

TYPE : Storable

S32 : Bit-mapped

Bits 1,0 Encryption mode select (#S CMD)
00 = No encryption (#S0)
01 = Force V.42bis encryption(#S1)
10 = Reserved for later use
11 = Reserved for later use

Bits 3,2 MNP Extended Services (-K CMD)
00 = Disabled (-K0)
01 = Enabled (-K1)
10 = Enabled without MNP indication during the answer detect phase. (-K2)

Bit 4 Power level adjustment setting (M CMD)
0 = Disable (M0)
1 = Enabled (M1)

Bits 6-5 Force an initial connection speed (*H CMD)
00 = Highest supported (*H0)
01 = 1200 bps (*H1)
10 = 4800 bps (*H2)

Bit 7 Not used

TYPE : Storable

S33 : Cellular Transmit Level

Value : 0 - 20

Default = 9

TYPE : Storable

S34 : Answer Logon Sequence

Value : 0 - 9 (If 0 then no logon in answer)

Default = 0

TYPE : Storable

S35 : Transmit Level (dBm)

Value : 0 - 20

Default = 9

TYPE : Storable

S36 : Error Correction Negotiation Failure Treatment

0 = Disconnect

1 = Normal asynchronous (no error control)

TYPE : Storable

S37 : Desired DCE Speed

• for N0 command :
0 = Last AT command speed
1 = 300 (Bell 103)
2 = 300 (Bell 103)
3 = 300 (Bell 103)
4 = Reserved
5 = 1200
6 = 2400
7 = V.32 4800
8 = Reserved
9 = V.32 9600 with Trellis Coded Modulation (TCM)
10 = V.32 9600 without TCM
11 = 300 (V.21)
12 = 1200 (V.23)
13 = reserved
14 = reserved
15 = V.32bis 4800
16 = V.32bis 7200
17 = V.32bis 9600
18 = V.32bis 12000
19 = V.32bis 14400
20 to 254 = Reserved
255 = Last AT command speed

• for N1 command :

0 to 19 = Connect at the highest possible speed regardless of the DTE speed.

255 = Connect at the highest possible speed up to the last AT command speed.

TYPE : Storable

S38 : Reliable Link Delay Before Forced Hang Up

Value : 0 - 254 s

Default = 20

TYPE : Storable

S39 : Bit-mapped

Bit 0 Not used

Bit 1 Auto disconnect (&E CMD, meanfull when direct or normal modes only.)
0 = Enable
1 = Disable

Bit 2 Reserved

Bit 3 DTE rate at 115200 bps
0 = DTE rate is according to bits 1,2 and 3 of S23 or bit 2 of S39
1 = DTE rate is at 115200 bps

Bit 5,4 Break handling (&I, K CMD)
0 = Non-destructive / non-expedited
1 = Non-destructive / expedited
2 = Destructive / expedited

Bit 6 EIA loopback test control (&T9 , &T10 CMD)
0 = Ignore EIA loopback test (&T10)
1 = Process EIA loopback test (&T9)

Bit 7 Auto retrain (&E CMD)
0 = Disable
1 = Enable

TYPE : Storable

S40 : Inactivity Timer

Value : 0 - 255 minutes (0 = Inactivity timer disabled)

Default = 0

TYPE : Storable

S41 : Dial Retry

Value : 0 - 10

Default = 0 (No retry)

TYPE : Non-Storable

S44 : Error Correction in Use

0 = No error correction
2 = MNP class 2
3 = MNP class 3
4 = MNP class 4
5 = MNP class 5
6 = V.42
7 = V.42bis
TYPE : Non-storable

S45 : Reason for Disconnection

0 = Lost carrier
1 = User interrupt
2 = Training failure
3 = Retrain failure
4 = Inactivity time out
5 = Long space disconnect
6 = Negotiation failure
TYPE : Non-storable

S46 : Fallback Character For Error Correction Negotiation

Value : 0 - 127

Default = 13 (ASCII CR)

TYPE : Storable

S47 : XON Character

Value : 0 - 127

Default = 17

TYPE : Storable

S48 : XOFF Character

Value : 0 - 127

Default = 19

TYPE : Storable

S49 : Bit-mapped

Bit 4 to 0 Flow Control (&K CMD)
0 = No flow control
3 = Hardware flow control
4 = SATURN to DTE, bi-directional flow control
8 = SATURN to DTE, unidirectional flow control
12 = SATURN to DTE, bi-directional, transparent flow control
16 = SATURN to remote modem, bi-directional flow control
20 = DTE to SATURN to remote modem bi-directional flow control

Bit 5 Compromise equalizer
(meanfull if bit 7 = 0)
0 = Compromize equalizer 1 (3dB)
1 = Compromize equalizer 2 (6dB)

Bit 6 Dumb mode
0 = Smart mode
1 = Dumb mode

Bit 7 Compromise equalizer
0 = Compromise equalizer enabled
1 = Compromise equalizer disabled

TYPE : Storable

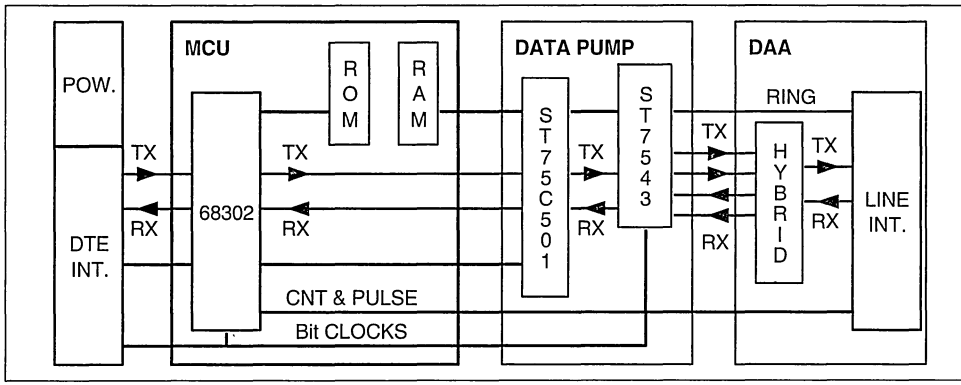
V.5 - S-Registers Factory defaults

Register	F0	F1	F2	Y0	Y1	Y2	Y3	Range	Status
S00	000	000	000	000	000	000	000	000 255	
S01	000	000	000	000	000	000	000	000 000	NS
S02	043	043	043	043	043	043	043	000 255	NS
S03	013	013	013	013	013	013	013	000 127	NS
S04	010	010	010	010	010	010	010	000 127	NS
S05	008	008	008	008	008	008	008	000 255	NS
S06	002	002	002	002	002	002	002	002 255	
S07	030	030	030	030	030	030	030	001 255	
S08	002	002	002	002	002	002	002	000 255	
S09	006	006	006	006	006	006	006	001 255	
S10	014	014	014	014	014	014	014	001 255	
S11	095	095	095	095	095	095	095	050 255	
S12	050	050	050	050	050	050	050	000 255	
S13	000	000	000	000	000	000	000	000 255	NS
S14	138	138	138	138	138	138	138	000 255	
S15	000	000	000	000	000	000	000	000 255	NS
S16	000	000	000	000	000	000	000	000 255	NS
S17	000	000	000	000	000	000	000	000 255	NS
S18	000	000	000	000	000	000	000	000 255	
S19	000	000	000	000	000	000	000	000 255	NS
S20	000	000	000	000	000	000	000	000 255	NS
S21	000	000	000	000	000	000	000	000 255	
S22	118	118	118	118	118	118	118	000 255	
S23	023	023	023	023	023	023	023	000 255	
S24	016	190	191	016	016	016	016	000 255	
S25	005	005	005	005	005	005	005	000 255	
S26	001	001	001	001	001	001	001	000 255	
S27	064	073	074	064	064	064	064	000 255	
S28	000	000	000	000	000	000	000	000 255	NS
S29	000	000	000	000	000	000	000	000 255	NS
S30	000	000	000	000	000	000	000	000 255	NS
S31	000	000	000	000	000	000	000	000 255	NS
S32	000	000	000	000	000	000	000	000 255	NS
S33	000	000	000	000	000	000	000	000 255	NS
S34	000	000	000	000	000	000	000	000 003	
S35	009	009	009	009	009	009	009	000 015	
S36	001	001	001	001	001	001	001	000 255	
S37	000	000	000	000	000	000	000	000 255	
S38	020	020	020	020	020	020	020	000 255	
S39	128	128	128	128	128	128	128	000 255	
S40	000	000	000	000	000	000	000	000 255	
S41	000	000	000	000	000	000	000	000 010	NS
S42	000	000	000	000	000	000	000	000 255	NS
S43	000	000	000	000	000	000	000	000 255	NS
S44	000	000	000	000	000	000	000	000 255	NS
S45	000	000	000	000	000	000	000	000 255	NS
S46	013	013	013	013	013	013	013	000 127	
S47	017	017	017	017	017	017	017	000 255	
S48	019	019	019	019	019	019	019	000 255	
S49	000	003	003	000	000	000	000	000 255	

Note : The STATUS column only applies to the Yn configurations. Those S-registers defined as Non Storable (NS) will be taken from the F0 configuration

VI - APPENDIX A : SATURN BLOCK DIAGRAM AND POSSIBLE EVOLUTIONS

Figure 1 : Block Diagram



Stand Alone :

DTE interface = RS 232.

Power suply = 7.5V rectified & filtered AC adapter and TDA8137 double 5V linear regulator.

PC board :

DTE interface = 16C550 or ST7548.

Power supply = from PC with low power 5V linear regulator for analog.

PCMCIA board :

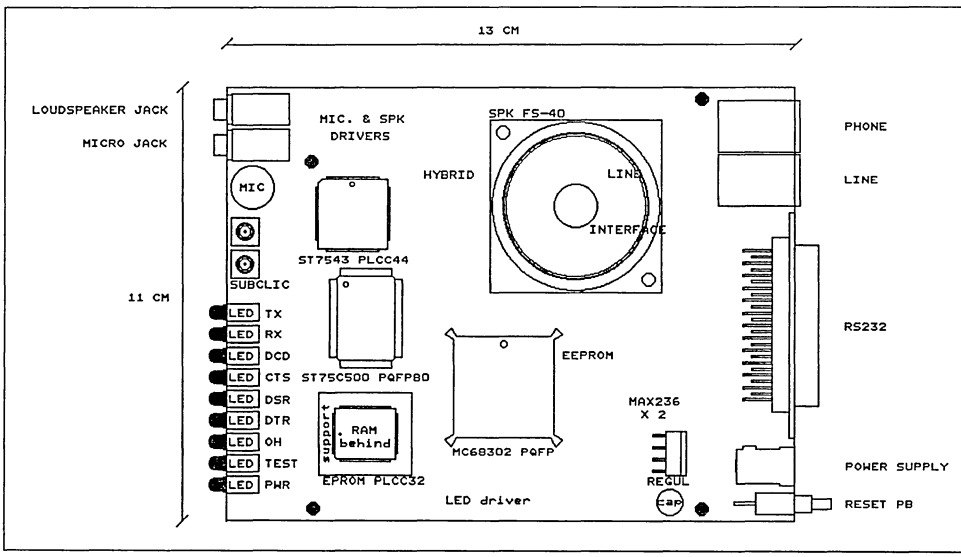
DTE interface = ST7548.

Power supply = from PCMCIA bus.

SATURN possible evolutions

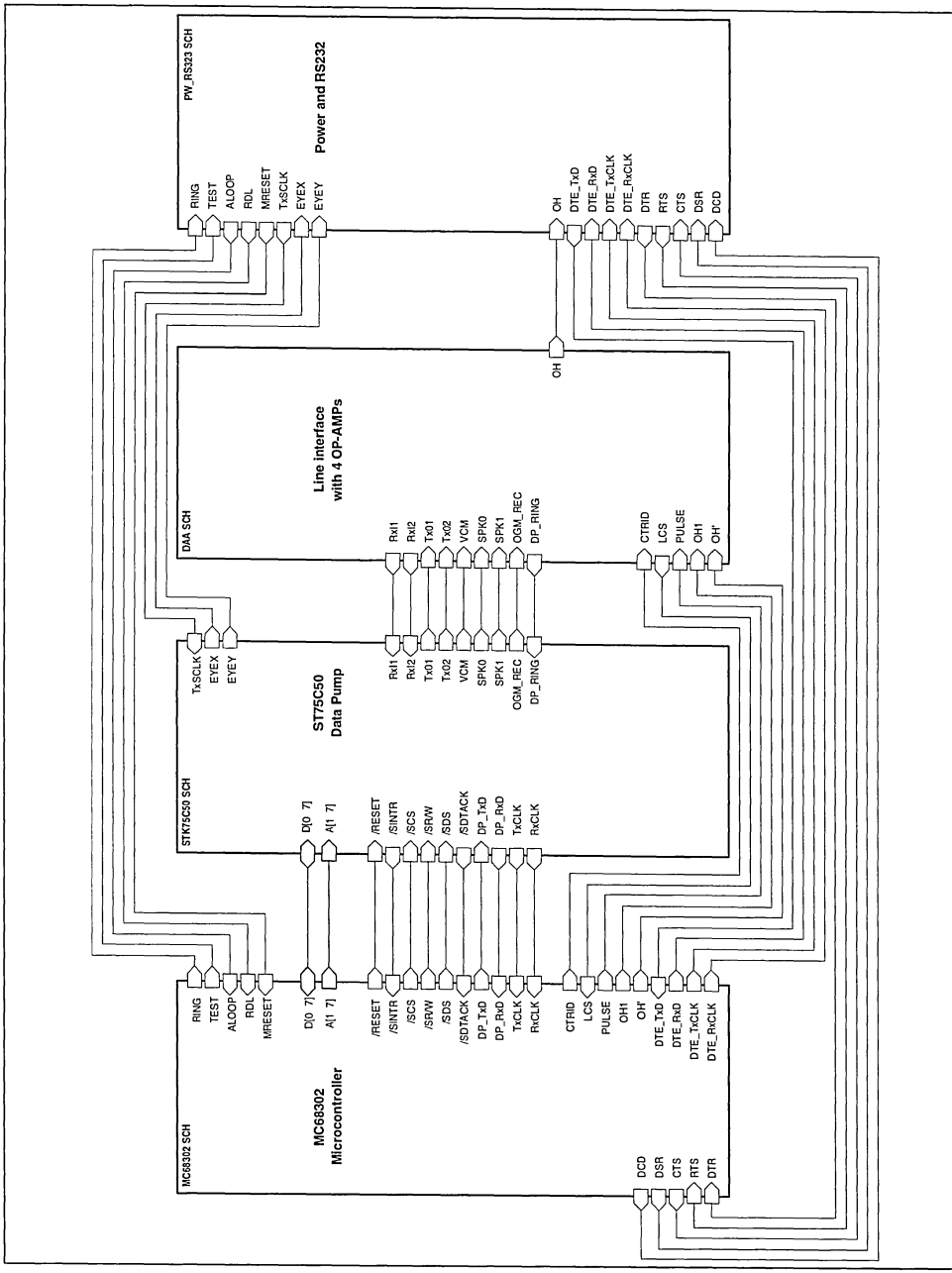
VII - APPENDIX B : SATURN STAND ALONE BOARD LAYOUT SCHEMATICS

Figure 2



VIII - APPENDIX C : SATURN STAND ALONE BOARD ELECTRICAL SCHEMATICS

Figure 3 : Main Sheet



SAT-03.EPS

Figure 4 : Microcontroller and Memories

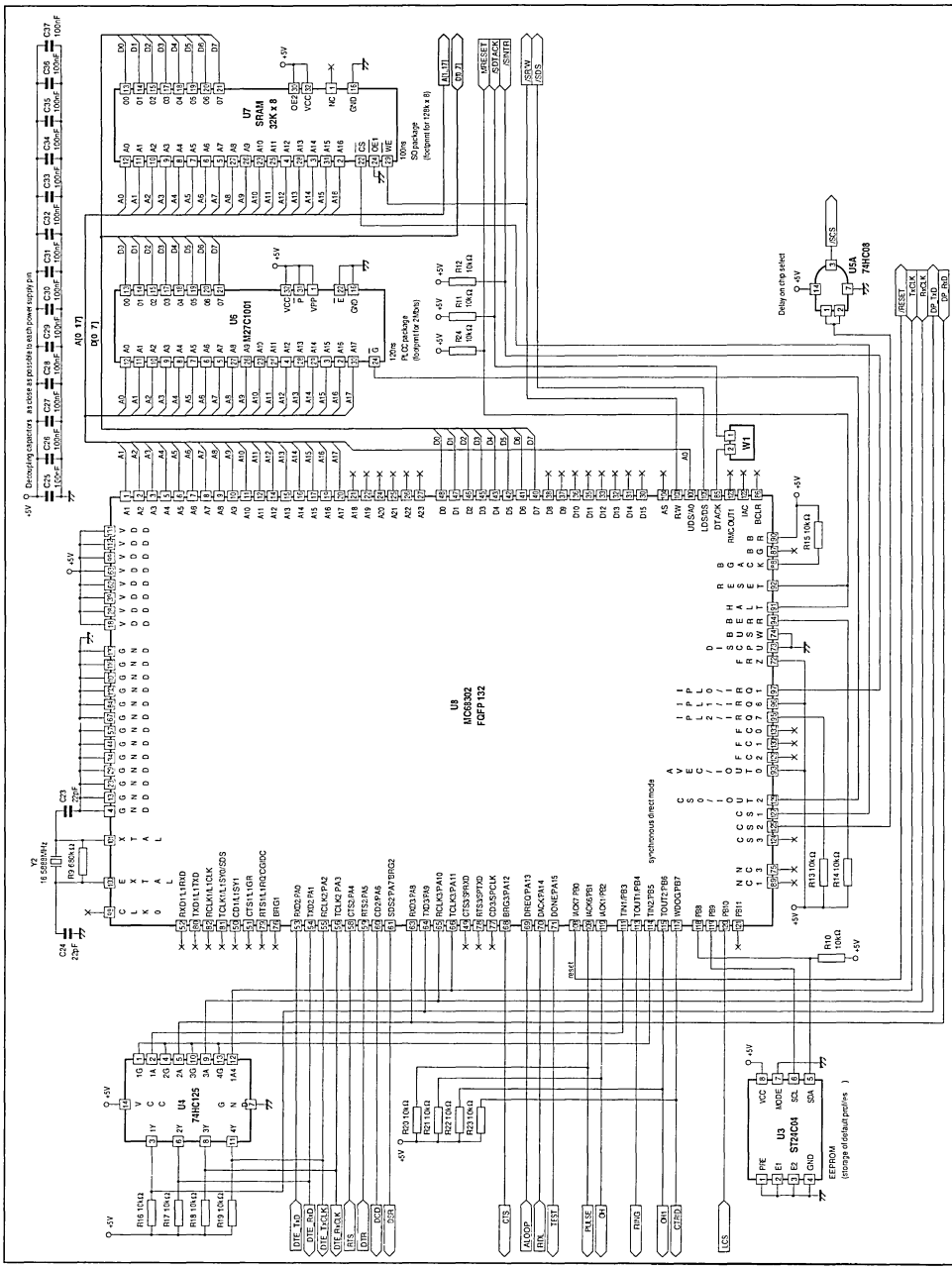


Figure 5 : Data Pump

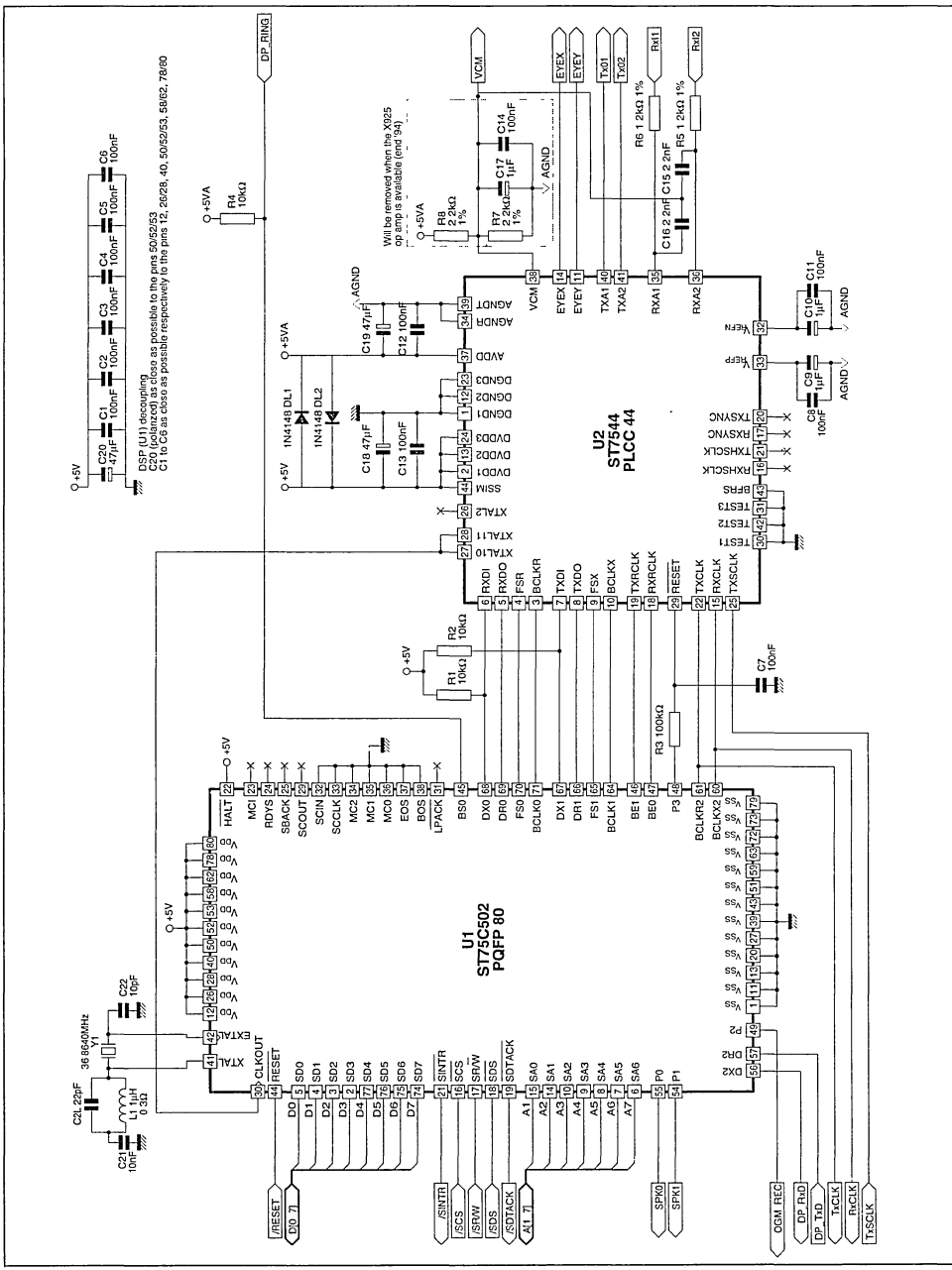
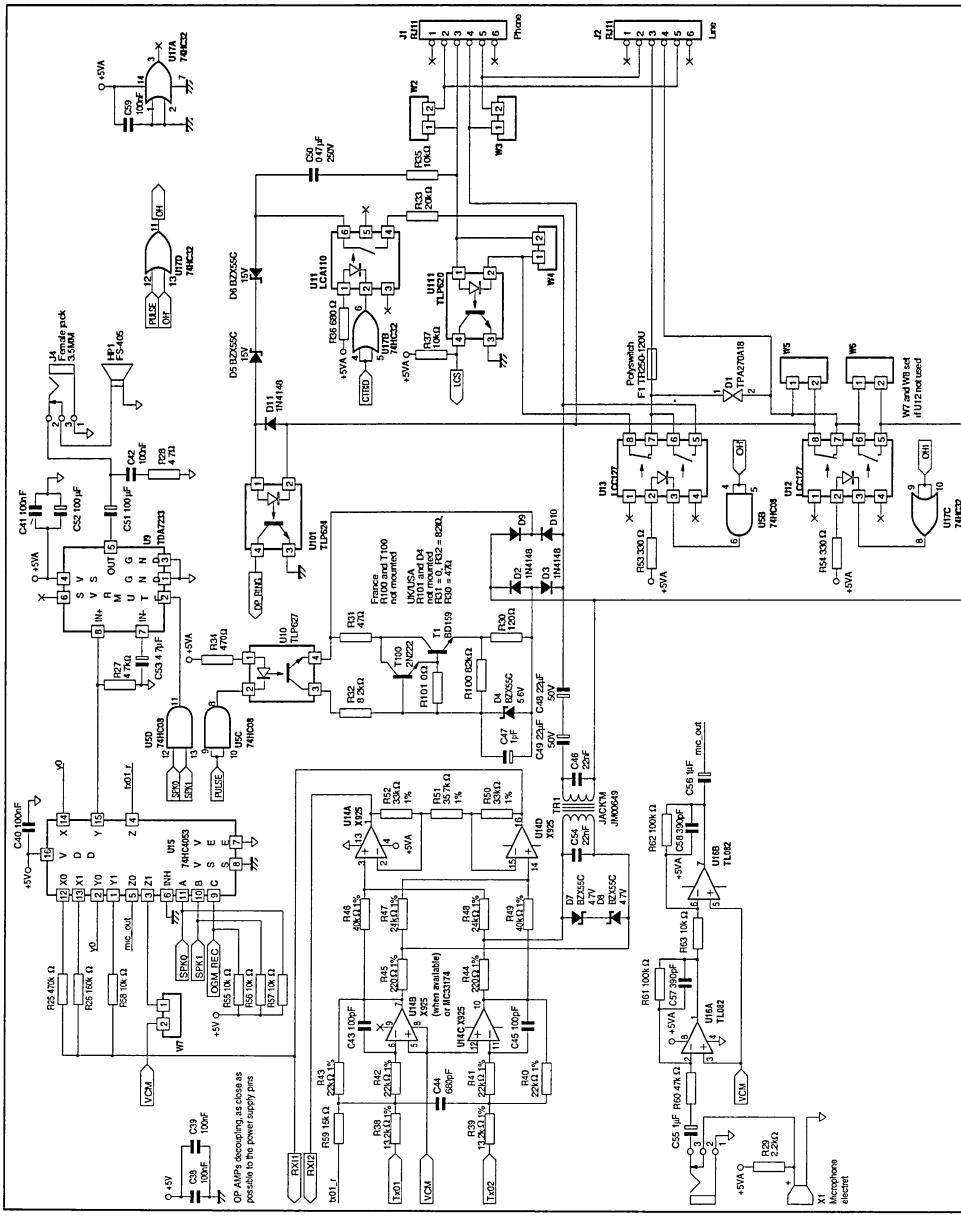
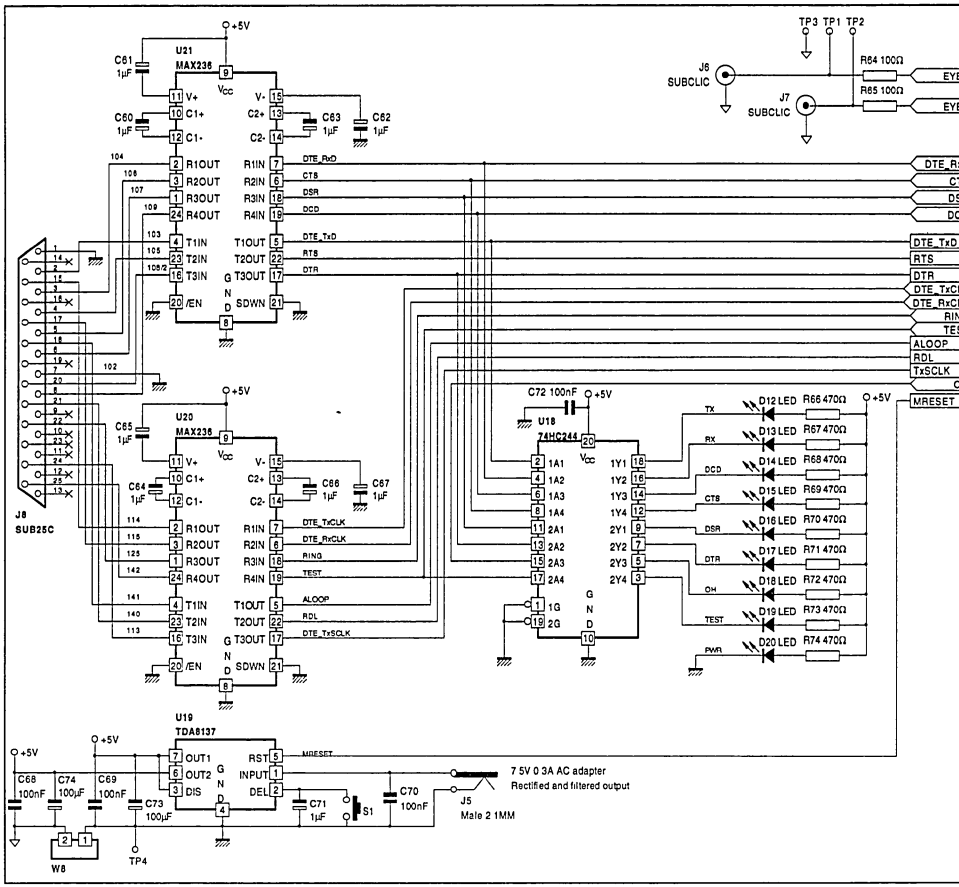


Figure 6 : Hybrid and Line Interface



Note : The op amp X925 package is a SO16. The MC33174 (SO14) used as long as the X925 is not available must be mounted Pin1 on Pin1.

Figure 7 : RS232 Interface and Power Supply



IX - APPENDIX D : SATURN STAND ALONE BOARD PART LIST

Item	Quantity	Reference	Part
1	35	C1,C2,C3,C4,C5,C6,C7,C8,C11,C12,C13,C14,C25,C26, C27,C28,C29,C30,C31,C32,C33,C34,C35,C36,C37,C38, C39,C40,C41,C42,C59,C68,C69,C70,C72	100nF CERAMIC
2	3	C2L,C23,C24	22pF CERAMIC
3	14	C9,C10,C17,C47,C55,C56,C60,C61,C62,C63,C64,C65, C66,C67	1µF 16V TANTALUM
4	2	C15,C16	2.2nF CERAMIC
5	3	C18,C19,C20	47µF 16V TANTALUM
6	1	C21	10nF CERAMIC
7	1	C22	10pF CERAMIC
8	2	C43,C45	100pF CERAMIC
9	1	C44	680pF CERAMIC
10	2	C46,C54	22nF CERAMIC
11	2	C48,C49	22µF 50V CHEMICAL
12	1	C50	0.47µF 250V
13	4	C51,C52,C73,C74	100µF 16V CHEMICAL
14	1	C53	4.7µF 16V TANTALUM
15	2	C57,C58	390pF CERAMIC
16	1	C71	1µF 16V TANTALUM
17	7	DL1,DL2,D2,D3,D9,D10,D11	1N4148
18	1	D1	TPA270A18
19	1	D4	BZX55C 5.6V
20	2	D5,D6	BZX55C 15V
21	2	D7,D8	BZX55C 4.7V
22	2	D12,D13	LED GREEN
23	7	D14,D15,D16,D17,D18,D19,D20	LED RED
24	1	F1	TR250-120U POLYSWITCH
25	1	HP1	FS-40S 8Ω
26	2	J1,J2	RJ11 MOLEX 95001-2661 LOW PROFILE
27	2	J3,J4	FEMALE JACK 3.5MM
28	1	J5	MALE 2.1MM POWER SUPPLY
29	2	J6,J7	SUBCLIC EYE MONITORING (OPTIONAL)
30	1	J8	SUBD25C FEMALE
31	1	L1	1µH O.3Ω
32	25	R1,R2,R4,R10,R11,R12,R13,R14,R15,R16,R17,R18,R19, R20,R21,R22,R23,R24,R35,R37,R55,R56,R57,R58,R63	10kΩ 1/4W 5%
33	3	R3,R61,R62	100kΩ 1/4W 5%
34	2	R5,R6	1.2kΩ 1/4W 1%
35	2	R7,R8	2.2kΩ 1/4W 1%
36	1	R9	680kΩ 1/4W 5%
37	1	R25	470kΩ 1/4W 5%
38	2	R26,R60	47kΩ 1/4W 5%
39	1	R27	4.7kΩ 1/4W 5%
40	1	R28	4.7Ω 1/4W 5%
41	1	R29	2.2kΩ 1/4W 5%
42	1	R30	120Ω 1/2W 5%
43	1	R31	47Ω 1/4W 5%
44	1	R32	8.2kΩ 1/4W 5%

Item	Quantity	Reference	Part
45	1	R33	20kΩ 1/4W 5%
46	10	R34,R66,R67,R68,R69,R70,R71,R72,R73,R74	470Ω 1/4W 5%
47	1	R36	680Ω 1/4W 5%
48	2	R38,R39	13.2kΩ 1/4W 1%
49	4	R40,R41,R42,R43	22kΩ 1/4W 1%
50	2	R44,R45	220Ω 1/4W 1%
51	2	R46,R49	40kΩ 1/4W 1%
52	2	R47,R48	24kΩ 1/4W 1%
53	2	R50,R52	33kΩ 1/4W 1%
54	1	R51	35.7kΩ 1/4W 1%
55	2	R53,R54	330Ω 1/4W 5%
56	1	R59	15kΩ 1/4W 5%
57	2	R64,R65	100Ω 1/4W 5%
58	1	R100	82kΩ
59	1	R101	0Ω
60	1	S1	PUSH BUTTON
61	4	TP1,TP2,TP3,TP4	TEST POINT SINGLE PIN
62	1	TR1	JACK'M JM00649 TRANSFORMER
63	1	T1	BD159
64	1	T100	2N2222
65	1	U1	ST75C502 PQFP 80
66	1	U2	ST7544 PLCC 44
67	1	U3	ST24C04
68	1	U4	74HC125
69	1	U5	74HC08
70	1	U6	M27C1001 120 NS - PLCC PACKAGE (FOOTPRINT FOR 2 MBITS)
71	1	U7	SRAM 128K X 8 100 NS - SO PACKAGE (FOOTPRINT FOR 128K X 8)
72	1	U8	MC68302 PQFP 132
73	1	U9	TDA7233
74	1	U10	TLP627 TOSHIBA
75	1	U11	LCA110 CLARE (OPTIONAL)
76	1	U12	LCC127 OR LCC 110 CLARE (OPTIONAL)
77	1	U13	LCC127 OR LCC 110 CLARE
78	1	U14	X925 (WHEN AVAILABLE) OR MC33174
79	1	U15	74HC4053
80	1	U16	TL082
81	1	U17	74HC32
82	1	U18	74HC244
83	1	U19	TDA8137
84	2	U20,U21	MAX236
85	1	U101	TLP624 TOSHIBA
86	1	U111	TLP620 TOSHIBA (OPTIONAL)
87	8	W1,W2,W3,W4,W5,W6,W7,W8	JP2 SOLDERED STRAP
88	1	X1	MICROPHONE ELECTRET
89	1	Y1	36.8640MHz THIRD OVERTONE CRYSTAL 50 PPM LOW PROFILE (ATS 49)
90	1	Y2	16.5888MHz CRYSTAL LOW PROFILE (ATS 49)

ST75C502 - DEFAULT TONE DETECTORS

1 - INTRODUCTION

The purpose of this application note is to describe the default setup for the tone detection, and the way they are managed during the Automode Handshake.

Refer to ST75C502 for explanation of the Tone detectors.

The 16 cells of the tone detectors are used, by the ST75C502, for various functions. The internal variable **_NTDCELL** define the number of tone detectors currently executed by the DSP.

This number is set to 16 after a RESET, and will be set to 0 as soon as the Autobaud phase is completed. The Autobaud Handshake is complete when we perfectly know the transmission standard.

While configuring for DTMF Detection, the upper 12 cells are overwritten to detect the 8 DTMF tones, plus 4 cells to split the band for differentiate Low group and High group of tones.

Refer to the Appendix for the default wiring of the tone detector.

2 - CELL DESCRIPTION

The First cell (#0) is programmed as a 440Hz tone detector (Call Waiting Detection) and is never changed whatever the DSP is doing. After a RESET (or ***init*** command) or any ***conf*** command, its parameters are set to detect the 440Hz single tone.

The template of this Tschebyscheff filter is :

Name	Cell Number	Type	Pass Band (Hz)	Stop Band (Hz)	Ripple (dB)	Reject (dB)
CALLWAIT	0	Band Pass	430, 450	340, 540	0.1	25

The second and third cell (#1 and #2) are used for Call progress detection. It is a Low pass filter with a cutoff frequency of 650 Hz. this filter like the previous one is never changed.

The template of this Tschebyscheff filter is :

Name	Cell Number	Type	Pass Band (Hz)	Stop Band (Hz)	Ripple (dB)	Reject (dB)
CPLOW	1, 2	Low Pass	0, 650	1000	0.2	45

Due to the DAA implementation and to the ST7544 analog front end receive filter, the frequencies below 300Hz are attenuated. Refer to Measurement Report for the detection area.

The cell mumber 3 and 4 are used for Call progress tone detection. It is a High pass filter with a cutoff frequency of 600Hz.

The template of this Tschebyscheff filter is :

Name	Cell Number	Type	Pass Band (Hz)	Stop Band (Hz)	Ripple (dB)	Reject (dB)
CPHIGH	3,4	High Pass	600, 3600	400	0.2	45

Frequencies above 3200Hz are attenuated due to the DAA and the ST7544 Receive filter.

While using the DTMF Mode (with a ***conf*** command) the cell 4 to 15 are overwritten with the DTMF detector parameters.

Starting from cell 5 the following 11 Cells are used for Autobaud Handshake. The default autobaud mode corresponds to the V.32bis Originate mode. While selecting the Answer mode (with a ***conf*** command) some cells are overwritten.

Cell number 5 and 6 are used to remove from the received signal what we are transmitting. This give a better immunity to noise than regular comparators. The corresponding filters are notch filters to remove the 2100Hz Answer tone in answer mode and the 1800Hz AA V.32bis tone in the originate mode.

The templates of these Butterworth filters are :

Mode	Name	Cell Number	Type	Pass Band (Hz)	Stop Band (Hz)	Ripple (dB)	Reject (dB)
Orig	AZ1800	5,6	Notch	1650, 1950	1780, 1820	3	30
Answer	OZ2100	5,6	Notch	1950, 2250	2080, 2120	3	30

Cell number 7 and 8 are used to detect the V.32bis AC tone. This signal is composed of a 600Hz and 3000Hz tones. Due to the possible amplitude distortion introduced by the telephone line only the 600Hz is used for AC detector. In Answer mode these cells are not used.

The template of this Tchebyscheff filter is :

Name	Cell Number	Type	Pass Band (Hz)	Stop Band (Hz)	Ripple (dB)	Reject (dB)
AN600	7, 8	Band Pass	580, 620	500, 700	0.3	45

Cell number 9 is used to detect the V.23 1300Hz Mark tone in Originate mode and the V.23 390Hz in Answer Mode.

The template of these Eliptic filters are :

Mode	Name	Cell Number	Type	Pass Band (Hz)	Stop Band (Hz)	Ripple (dB)	Reject (dB)
Orig	AN1300	9	Band Pass	1275, 1325	1000, 1600	0.5	45
Answ	ORG390	9	Band Pass	360, 420	200, 650	1	40

Cell number 10 and 11 are used to detect the V.21 1650Hz Mark tone in originate Mode and V.21 980Hz Mark tone in Answer Mode.

The template of these Tchebyscheff filters are :

Mode	Name	Cell Number	Type	Pass Band (Hz)	Stop Band (Hz)	Ripple (dB)	Reject (dB)
Orig	AN1650	10,11	Band Pass	1625, 1675	1500, 1800	0.1	45
Answ	ORG980	10,11	Band Pass	968, 992	900, 1060	0.05	45

Cell number 12 and 13 are used to detect CCITT 2100Hz Answer tone while in Originate mode and the V.32bis AA signal (1800Hz) while in Answer mode.

The template of these Tchebyscheff filters are :

Mode	Name	Cell Number	Type	Pass Band (Hz)	Stop Band (Hz)	Ripple (dB)	Reject (dB)
Orig	ANS2100	12,13	Band Pass	2080, 2120	2030, 2170	0.3	45
Answer	ORG1800	12,13	Band Pass	1780, 1820	1700, 1900	0.3	45

In Originate Mode the Cells number 14 and 15 are used to detect the Bell 212 and Bell 103 Answer 2225Hz Answer tone. This filter covers also the V.22 unscrambled "1" at the beginning of the answer mode handshake.

In Answer Mode these cells are used to detect the Bell 103 1270Hz.

The template of these Tchebyscheff filters are :

Mode	Name	Cell Number	Type	Pass Band (Hz)	Stop Band (Hz)	Ripple (dB)	Reject (dB)
Orig	ANS2225	14,15	Band Pass	2205, 2270	2140, 2360	0.5	45
Answ	ORG1270	14,15	Band Pass	1250, 1290	1150, 1390	0.1	45

3 - BIT DESCRIPTION

Refer to the Appendix for the default wiring of the cells

The 16 bits output of the tone detectors have the following meaning.

Word	Bit	Description	
0	0	440Hz higher than -36dBm	
0	1	wide band signal higher than -27dBm	
0	2	Low Pass signal (650Hz) higher than -36dBm	
0	3	High Pass signal (600Hz) higher than -36dBm	
0	4	Low Pass signal higher than High Pass signal	
		Originate	**Answer**
0	5	signal without 1800Hz higher than -45dBm	signal without 2100Hz higher than -45dBm
0	6	V.32bis AC signal higher than -45dBm	not used
0	7	AC signal higher than wide signal without 1800Hz	not used
1	0	V.23 1300Hz Mark signal higher than -45dBm	V.23 390Hz Mark signal higher than -41dBm
1	1	V.23 1300Hz signal higher than wide signal without 1800Hz	V.23 390Hz signal higher than wide signal without 2100Hz + 4dB
1	2	V.21 1650Hz Mark signal higher than -45dBm	V.21 980Hz Mark signal higher than -45dBm
1	3	V.21 1650Hz signal higher than wide signal without 1800Hz	V.21 980Hz signal higher than wide signal without 2100Hz
1	4	CCITT 2100Hz Answer tone higher than -45dBm	V.32bis AA signal (1800Hz) higher than -45dBm
1	5	CCITT signal higher than wide signal without 1800Hz	V.32bis AA signal higher than wide signal without 2100Hz
1	6	Bell 2225 or Unscrambled Mark higher than -45dBm	Bell 103 1270Hz Mark signal higher than -45dBm
1	7	Bell signal higher than wide signal without 1800Hz	Bell 103 1270Hz signal higher than wide signal without 2100Hz

4 - APPENDIX

Figure 1

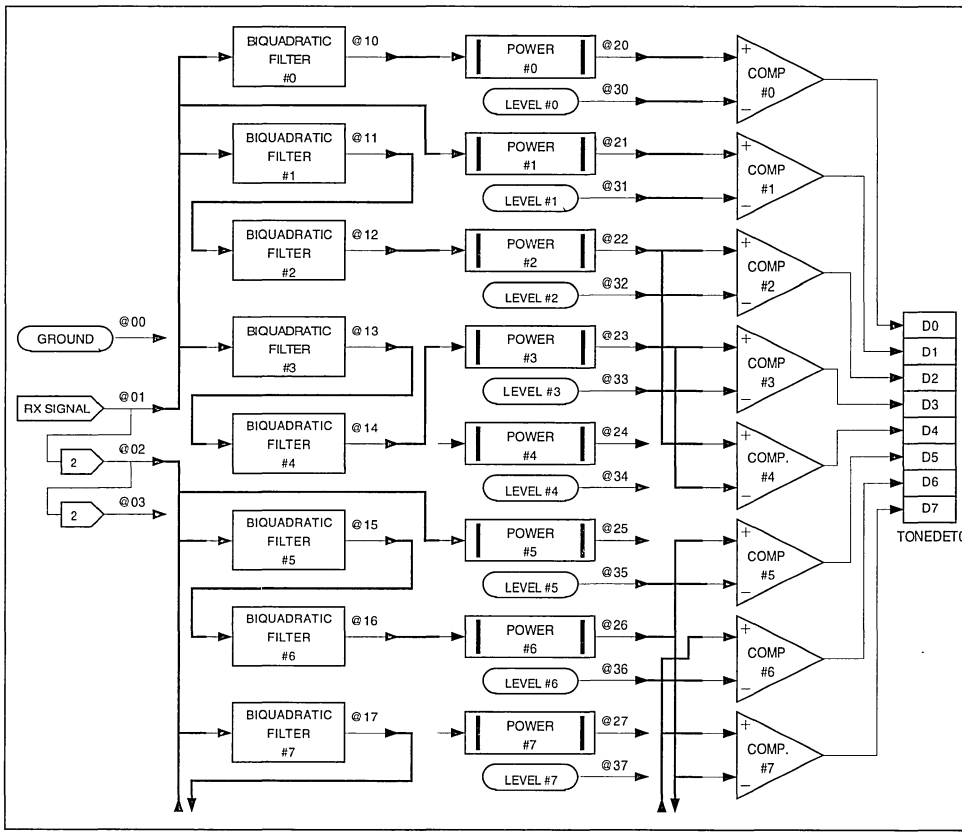
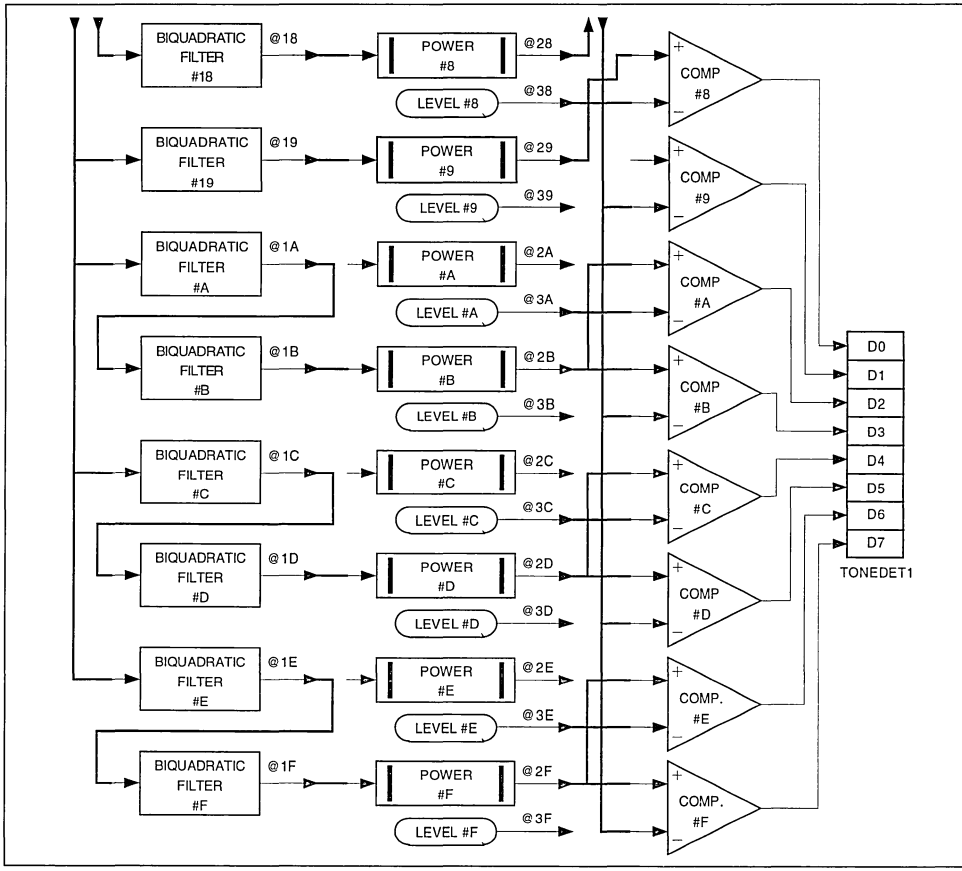


Figure 2


BIQUADRATIC FILTER #18
@18
POWER #8
@28
LEVEL #8
@38
COMP #8
BIQUADRATIC FILTER #19
@19
POWER #9
@29
LEVEL #9
@39
COMP #9
BIQUADRATIC FILTER #A
@1A
POWER #A
@2A
LEVEL #A
@3A
COMP #A
BIQUADRATIC FILTER #B
@1B
POWER #B
@2B
LEVEL #B
@3B
COMP #B
BIQUADRATIC FILTER #C
@1C
POWER #C
@2C
LEVEL #C
@3C
COMP #C
BIQUADRATIC FILTER #D
@1D
POWER #D
@2D
LEVEL #D
@3D
COMP #D
BIQUADRATIC FILTER #E
@1E
POWER #E
@2E
LEVEL #E
@3E
COMP. #E
BIQUADRATIC FILTER #F
@1F
POWER #F
@2F
LEVEL #F
@3F
COMP. #F
D0
D1
D2
D3
D4
D5
D6
D7
TONEDET1
AN537-02 EPS

ST75C502 - BULK DELAY MANAGEMENT

1 - INTRODUCTION

The purpose of this application note is to describe the way the user must handle the interrupt reserved for Bulk delay managment.

A V.32bis modem use echo canceller technology, it substract from its received signal an estimation of its own signal echoed by the PSTN. As the transmition can have a very long delay, especialy while using satellite (up to 1.4 Second), its is mandatory to memorise all the signal that have been send during the last 1.4 second. To reduce the size of the memory needed, instead of storing the signal, we just store the symbols that were transmitted. However one can see that, if we want to handle two satellites hops, it is necessary to have a 1.4 second * 2400 symbols by second = 3360 symbols. Each symbol can be packed using a single byte, so the size of this BULK memory is 3360 bytes.

In the ST75C502, instead of adding a 4K byte inside the DSP, just to be used like a FIFO, to store and recall one symbol (Byte) each baud (0.4ms), the Bulk Delay can be implemented using the Host interface Memory. We assume that the host processor have enough memory to allocate a 4K byte inside its own Data Memory.

2 - INITIALIZATION

Prior to any operation, the user must assign the Bulk Delay (bulk_delay_line) inside its data space. The length of the bulk delay is depending of the Maximum Round Trip Delay (MAX_BULK_DELAY) that we want to handle.

```
#define MAX_BULK_DELAY 3360          /* 1.4 Second Maximum Roud Trip Delay */

unsigned char bulk_delay_line[MAX_BULK_DELAY];    /* Symbol's Storage Area */
```

Code : 1 /* "C" Global Declaration */

For further understanding we define few prototype functions :
- ST75c5x_read: read a DUAL RAM location.
- ST75c5x_write: write a DUAL RAM location.
- ST75c5x_send_cci_command: send a CCI Command to the ST75C502.

```
/* Read a DUAL RAM Location: return code is the contain of the RAM */
unsigned char ST75c5x_read(unsigned char address);

/* Write a DUALRAM Location: write data at address                 */
void ST75c5x_write(unsigned char address, unsigned char data);

/* Send a CCI Command to the ST75C502                               */
unsigned char ST75c5x_send_cci_command(unsigned char opcode, unsigned char param[4]);
```

Code : 2 /* "C" Prototype Function */

An Example of implementation of ST75c5x_send_cci_command is given at the end of this application note.

The mechanism implemented inside the ST75C502 assumes that the address of the bulk_delay_line is a 16 bit word (short int) and that each byte of the bulk_delay_line are located continiously (+1). At the begining we must initialize this mechanism by giving it the two addresses **BA_ADDR** and **TO_ADDR**.

We assume that the "**C**" compiler contains two functions to convert a pointer into its physical address and an address (as a short int) into a pointer. Let define these two prototypes:

```
/* Convert a Pointer into a Physical Address */
short int PTR_ADDR( unsigned char *var);

/* Convert a Physical Address into a Pointer */
unsigned char *ADDR_PTR( short int var);
```

Code : 3 /* "C" Pointer to Interger Conversion Prototype */

After the CONF command used to select the V.32bis mode of operation, we have to initialize the bulk delay mechanism with a BULK command:

```
/* Global declaration */
#define  CCI_BULK  0x22       /* CCI Bulk Opcode */

unsigned char ST75c5x_init_bulk()

{

        /* local declaration */
        short int i, base_addr, top_addr;
        unsigned char param[4];

        /* Get Physical address for Base of Bulk_Delay_Line */
        i = PTR_ADDR(&bulk_delay_line[0]);
        /* Be sure this number is on a 8 bytes boundary */
        while ((i%8)!=0) i++;
        base_addr = i;

        /* Get Physical address for Top of Bulk_Delay_Line */
        i = PTR_ADDR(&bulk_delay_line[MAX_BULK_DELAY-1]);
        /* Be sure this number is on a 8 bytes boundary */
        while (((i+1)%8)!=0) i--;
        top_addr = i;

        /* Prepare Parameters for sending Command */
        param[0]=(unsigned char) base_addr % 256;
        param[1]=(unsigned char) base_addr > 8;
        param[2]=(unsigned char) top_addr % 256;
        param[3]=(unsigned char) top_addr > 8;

        /* Send CCI Command */
        return( ST75c5x_send_cci_command( CCI_BULK, param ));

}
```

Code : 4 /* "C" Bulk initialization */

There is no particular timming to respect between the **CONF** command, the **HSHK** command and the **BULK** command. However, to work properly, the **BULK** command must be send before the Echo canceller is started (CA-AC transition in answer mode, R1 detection in originate mode).

We can also send the **BULK** command in other mode than V.32 (or V.32 autobaud) this will not have any effect.

At that steep we must known if we want to proceed the bulk delay managment by pooling or by interrupt. As the Interrupt task is very simple we recommand the use of an interrupt; however just pooling the **SYMSTA DUAL RAM** Location will give the same results.

If we use interrupt we must enable the interrupt bit inside the **ITMASK** register, this will allow the ST75C502 to generate a signal on its **SINTR** Pin.

```
/* Enable ST75c5x bulk Interrupt */
#define  ADDR_ITMASK       0x4F    /* ST75c5x Interrupt Mask */
#define  DUAL_EN_BULK_IT   0x02    /* Enable Bulk Interrupt Bit */

void ST75c5x_enable_bulk_it()
{
         ST75c5x_write(ADDR_ITMASK,
           ST75c5x_read(ADDR_ITMASK) | DUAL_EN_BULK_IT));
}
```

Code : 5 /* "C" Enable Bulk Interrupt */

3 - MAIN TASK

Each 8 symbols (3.3ms) it is mandatory to serve the Bulk delay mechanism, otherwise an error occurs that will be signaled into the **SYSERR** bit 2 **(ERR_SYM).**

The following routine is just the part of the interrupt mandatory to serve the Bulk Delay. Its suppose that the Interrupt **(ITSRCR)** source have been correctely decoded and that the other interrupts (Error, Command, Status, Data_Tx, Data_Rx) are well served.

```
/* Global Declaration                                          */

#define  ADDR_SYMSTA             0x0F    /* Symbol Buffer Status     */
#define  ADDR_SYMADT             0x10    /* Symbol Tx Buffer Pointer */
#define  ADDR_SYMADR             0x12    /* Symbol Rx Buffer Pointer */
#define  ADDR_SYMBUF             0x14    /* Symbol Buffer            */

#define  ADDR_ITSRCR             0x50    /* Interrupt Source Byte    */
#define  DUAL_CLR_IT_BULK        0x41    /* Clear IT1                */

/* !!!! Only Part of the Interrupt !!!! */
        /* Local Declaration                              */
        short int addr;           /* Local address        */
        unsigned char *p;         /* Local Pointer        */
        unsigneg char i;          /* Local Loop Counter   */

        /* Read Interrupt Source */
        if (ST75c5x_read(ADDR_ITSRCR)&DUAL_IT_BULK)) {

          /**** The BULK Service is Required *****/

          /* Read First Address */
          addr=(short int) ST75c5x_read(ADDR_SYMADR);
          addr+=(ST75c5x_read(ADDR_SYMADR+1)<8));
          p=ADDR_PTR(addr); /* Convert into a Pointer     */

          /* Move from DUAL RAM to bulk_delay_line        */
          for (i=0;i<8;i++) ST75c5x_write (ADDR_SYMBUF+i, *p++);

          /* Clear the Bulk Interrupt Pending Bit         */
          ST75c5x_write (DUAL_CLR_IT_BULK, 0);

/* !!!! Continu processing with the other interrupts !!!! */
```

Code 6 : /* "C" Interrupt Bulk Managment */

4 - APPENDIX

```
/* Global Definition of DUAL RAM Address                */
#define ADDR_COMSYS       0x00  /* Command Word         */
#define ADDR_COMPAR       0x01  /* Parameters           */
#define ADDR_SYSERR       0x08  /* Error Status         */

/* OPTIONAL: ERROR Return Codes                         */
#define DUAL_ERR_NREADY   0x01  /* ST75c5X not Ready    */
#define DUAL_ERR_IOCD     0x02  /* Incorrect Opcode     */
#define DUAL_ERR_IPRM     0x04  /* Incorrect Parameter  */
#define CCI_ERR_MASK      0x18  /* Mask for IOCD or IPRM */
#define CCI_ERR_MASKIO    0x08  /* Mask for IOCD        */

/* Send a CCI Command to the ST75c5x                    */

unsigned char ST75c5x_send_cci_command( unsigned char opcode, unsigned char param[4])
{

        unsigned char i; /* local */

        /* OPTIONAL: Test if the ST75c5x is ready to Execute a command */
        if (ST75c5x_read(ADDR_COMSYS)!=0x00) return(DUAL_ERR_NREADY);

        /* Write Parameters                             */
        for (i=0;i<=3;i++) ST75c5x_write(ADDR_COMPAR+i, param[i]);

        /* Last Write opcode to start transfer          */
        ST75c5x_write(ADDR_COMSYS, opcode);

        /* Wait until COMSYS Empty                      */
        while (ST75c5x_read(ADDR_COMSYS)!=0x00) /* wait */;

        /* OPTIONAL: Read the Error Status to check if the command was successfull */
        i = (ST75c5x_read(ADDR_SYSERR)&CCI_ERR_MASK);

        /* OPTIONAL: test if CCI Error                  */
        if (i!=0) {
          if (i&CCI_ERR_MASKIO) return(DUAL_ERR_IOCD);
          else return(DUAL_ERR_IPRM);
          }

        return (0);

}
```

Code : 7 /* "C" ST75c5x_send_cci_command Example of Implementation */

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

ST75C502 - RAM MAPPING

By William GLASS

CONTENTS **Document page**

I - INTRODUCTION

The purpose of this application note is to explain what are the "interesting internal variables" that can be Read, Written or Modified using the **MR**, **MW**, **CR** commands.
Some of these variables have dedicated commands to modify them, like SETGN for **_TXGAIN** or tone detector. However the whole RAM (even external when using the ST18933) and also the DUAL RAM and internal peripherals can be accessed using the three above mentioned commands.

The address, characteristic (R = Read, W = Write, R/W = Read or Write), and function of key data pump variables is listed below by basic modem functional blocks.

Caution : The Mapping of the variables, given in the appendix is only valid for Revision 2.0 of the ST75C502.
There is no guarantee that it will remain exactely the same for further revisions.

II - ECHO CANCELLER (V.32bis only)

_RTDELAY (R) Round trip delay in number of bauds.

_EC_STA (R/W) Echo canceller execution status word. the echo canceller can be frozen in data mode by reading _EC_STA and performing a logical or with the value $0002 before writing to _EC_STA (i.e. other bits must not be changed).

PWREST (R) Residual echo power estimator for determining loss of connection. The ABS() value of this variable will be greater than $20 to indicate connection loss, otherwise near 0.

FREQOFF (R) Far-end echo frequency offset. offset = FREQOFF x 0.0366 in Hz typically, FREQOFF = $1b(27) for 1Hz.

DELTA (R) Initial far-end echo power after near end echo canceller convergance. This variable can be read in data mode and has the following typical values.

	VALUE	POWER
$FFF6	(-10)	- 9dBm
$FFF7	(- 9)	-12dBm
.	.	.
$0000	(0)	-39dBm
.	.	.
$000A	(+10)	-69dBm

FEECENBL (R) Far end echo canceller is enabled. $FFFF = Enabled, $0000 = Disabled (when initial far-end power is less than -69dBm).

III - TIMING RECOVERY

FRQOFFLT (R) Receive clock frequency offset.

PSITHRSH (R) 0.94 Degree timing phase adjustement threshold for timing signal dpll.

Comments : The local-to-remote modem timing offset can be calculated using the following formula :

$$\text{TIMING OFFSET} = \frac{\text{FRQOFFLT}}{\text{PSITHRSH}} \cdot \frac{0.94}{360}$$

The normal timing offset is within $\pm 10^{-4}$ for most connections.

IV - CARRIER RECOVERY

FRQOFF (R) Receive carrier frequency offset. OFFSET = FRQOFF x 0.0366 in Hz. Typically, FRQOFF = $1B(27) for 1Hz.

V - EQUALIZER, AGC

_RX_STA (R/W) Equalizer and AGC can be frozen independently or simultaneously.

Bit 0 : Freeze Equalizer (the Equalizer is frozen if this bit is 1).

Bit 2 : Freeze AGC (the AGC is frozen if this bit is 1).

_RX_STA must be modified in data mode and the other bits must be unchanged. Read the value and change only the corresponding bits in the _RX_STA word.

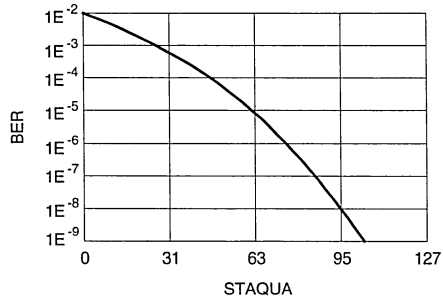
_AGCSCA (R/W) Automatic gain control level for receive signal varies from $80(0dBm) to $7fff (48dBm).

RDQUA (R) Equalizer error energy gives an idea of signal to noise ratio seen by the receiver. RDQUA has the following typical values.

VALUE	POWER
$00C0	30dB
$0180	27dB
$0300	24dB
$0600	21dB
$0C00	18dB
$1800	15dB
$3000	12dB

STAQUA (R) A 16-bit number between 0 and 127 indicating the receive quality (also available in 8-bit status word byte 2, STAQUA in dual port RAM). The following formula is implemented in DSP software :
STAQUA = 127 – SCAQUA · RDQUA
and is limited between 0 and 127. A value of 127 indicates a very good receive signal quality while 0 indicates a very poor signal quality. The coefficient SCAQUA is mode dependendent and was chosen to give a value for STAQUA of 63 when the receive SNR is such that the expected bit error rate is 10e-5, that is, 1 error for every 100 000 bits received.
Refer to the following charts for expected values of STAQUA, BER on flat telephone line.

Figure 1



AN539-01.EPS

SCAQUA (R/W) The coefficient for calculing STAQUA above is automatically programmed according to the mode specified in the CONF command and it is possible to overwrite its value at the end of the synchronization sequence if the user desires a different value for the quality indication. Generally, reducing the value read by 1/2 will imply that an STAQUA value of 31 will correspond with a 10^{-5} BER and doubling the value will imply that an STAQUA value of 127 will correspond with a 10^{-5} BER in the above table.

_SUCTH (R/W) A threshold value for STAQUA for determining the programming of PNSUCS bit in HSHK_PHA word described below. The default value is programmed to 64 at the execution of a CONF command and can be modified there after.

_RDCPT (R) Output of demodulator. Complex number, can be used to display the received eye.

EQFRK0E (R/W) 32 Complex even equalizer coefficients.

EQFRK1E (R/W) 32 Complex odd equalizer coefficients.

VI - HANDSHAKE, RETRAIN, RATE NEGOTIATION

_SSPEED (R) Negociated speed. This 8-bit number is available in STAOP0 in modem mode (refer to Data Sheet for values).

_STAV54E (R) this 8-bit number is available in STAOP1 in modem mode and indicates status V.54 and V.22bis test logs (refer to Data Sheet for values).

HSHK_PHA (R) Handshake progression counter contains information about the progress of the handshake in V.32 and V.22bis modes. This 8-bit value is available in STAOP2 in modem mode. It can be read to examine the progression of the handshake and it contains normal values and error values as below :

AUTOBAUD ORIG MODE

EVENT	HSHK_PHA Value
Wait Answer Tone	$01
Wait End Answer Tone	$02
No Autobaud and Waiting USC1	$03
Autobaud Waiting AC or USC1	$04

AUTOBAUD ANSW MODE

EVENT	HSHK_PHA Value
Waiting HSK Command	$10
Generating Answer Tone	$11
Generating Silence	$12

V.32 ORIG MODE

EVENT	HSHK_PHA Normal Value	HSHK_PHA Error Value
AC_DET	$20	
AC/CA DET	$21	$1
CA/AC DET	$22	$2
NO AC DET	$23	$B for RTRN, $C for RRN
S_DET	$24	$4
SB_DET	$25	$5
R1_DET	$26	$6
S_DET	$27	$7
SB_DET	$28	$8
R3_DET	$29	$9, $D no R5 det after RRN
E_DET	$2A	$A
DATA_MODE	$30	

V.32 ANSW MODE

EVENT	HSHK_PHA Normal Value	HSHK_PHA Error Value
AA_DET	$40	$8 for RTRN, $9 for RRN
AA/CC DET	$41	$1
NO CC DET	$42	$2
S_DET	$43	$3
S_DET2	$44	$4
SB_DET	$45	$5
R2_DET	$46	$6, $A no R det after RRN
E_DET	$47	$7
DATA_MODE	$50	

V.22bis ORIG MODE

EVENT	HSHK_PHA Normal Value
HSHK	$60
USC1_DET	$61
SCR1_DET	$62
S1_DET	$63
DATA_MODE	$70

V.22bis ANSW MODE

EVENT	HSHK_PHA Normal Value
HSHK	$80
SCR1_DET	$82
S1_DET	$83
DATA_MODE	$90

FAX MODE

While Transmiting	
P1s	= %00000001 generate echo protection tone
P2s	= %00000010 generate phase reversals
PNs	= %00000100 generate training sequence
PRs	= %00001000 generate rate sequence
SCR1s	= %00010000 generate scrambled one's
While Receiving	
P2s	= %00000010 detect phase reversals
PNDETs	= %00100000 detect training sequence (latched)
PNs	= %00000100 detect training sequence
PRDETs	= %01000000 detect rate sequence (latched)
PNSUCs	= %10000000 equalizer trainning succes (latched)
SCR1s	= %00010000 detect scrambled one's

Note that PRs and PRDET are only valid in V.17 and V.33 modes.

_RE_HSK (R) Stored R and E word values which were sent and received in their chronological order during the handshake, retrain, or rate negotiation. Positions _RE_HSK to (_RE_HSK+4) contain history during handshake or retrain while (_RE_HSK+5) to (_RE_HSK+8) contain history during a rate negotiation request.

_TSPEED (R/W) Target speed initialized by CONF or RTRA commands but can be changed in data mode for the case of a remote RTRA or RRN requests.

%0000000000000010 = 1200 BPS
%0000000000000011 = 2400 BPS
%0000000000000100 = 4800 BPS
%0000000000000101 = 7200 BPS
%0000000000000110 = 9600 BPS
%0000000000000111 = 12000 BPS
%0000000000001000 = 14400 BPS

_TRWORD
_RWORD (R/W) Target RWORD initialized by CONF or RTRA commands but can be changed (both of them) in data mode for the case of remote RTRA or RRN requests. In reference to the CCITT recommendation the bits are programmed in the following order :

(ITU-T RECOMMENDATION)

B00, B01, B02, B03, B04, B05, B06, B07, B08, B09, B10, B11, B12, B13, B14, B15

. . . . . .

D15, D14, D13, D12, D11, D10, D09, D08, D07, D06, D05, D04, D03, D02, D01, D00

(_TRWORD)

RNTHRSH (R/W) Threshold for rate negotiation during handshake or retrain. The quality of the receive signal is observed (can be disabled by the command MODC) and the corresponding R word is proposed in the handshake or retrain rate negotiation. The default value is $300. This gives the typical R word authorization characteristics as shown below :

SPEED Authorized	SNR
14400	> 24dB
12000	< 24dB
9600	< 21dB
7200	< 18dB

Doubling the threshold will decrease the corresponding snr by 3dB approximately.

_CURMOD (R/W) To give the final negotiated mode for Autobaud applications (especially useful for FSK) or data mode configuration.

D7	D6	D5	D4	D3	D2	D1	D0
CCITT	QAMMD	TCMMD	FDUMD	LOWMD	ECCMD	Not Used	ANSMD

CCITT : 1 : CCITT modes.
0 : Bell modes.
QAMMD : 1 : QAM V.32bis, V.32, V.22bis, V.22, B212A, V.17, V.33, V.29, V.27.
0 : V.21, V.23, B103 FSK modes.
TCDMMD : 1 : Trellis mode (V.17, V.33 or V.32(bis)).
0 : Non-trellis mode.
FDUMD : 1 : Full duplex mode such as V.32(bis), V.22(bis), B212A, V.21, V.23, B103.
0 : Half duplex modes (fax) V.21ch2, V.17, V.33, V.29, V.27.
LOWMD : 1 : V.27 or V.32 or V.22 or V.21 or B103.
0 : V.29 or V.32bis or V.22b or V.23.
ECCMD : 1 : Echo canceller mode V.32(bis).
0 : No echo canceller mode (others).
ANSMD : 1 : Answer mode.
0 : Originate mode.

VII - CARRIER DETECT

DETH1 (R/W) Fast detection threshold.
DETH (R/W) Slow detection threshold.
LOSSTH1 (R/W) Slow loss threshold.
LOSSTH (R/W) Fast loss threshold.

The carrier detect contains 2 signal level integrators, a fast integrator for quick detection with a limited precision and a slow integrator for enhanced precision. There are four thresholds programmed with default values for each of the modes V.22bis, V.33, V.17, FSK, V.29, and V.27 which can be modified by the user after the conf command. Typical values are shown below and doubling the value will increase the threshold by approximately 6dB :

(-40dBM)	$B0	DETH1 (fast detection threshold)
(-44dBM)	$90	DETH (slow detectiion threshold)
(-47dBM)	$60	LOSSTH1 (slow loss threshold)
(-51dBM)	$40	LOSSTH (fast loss threshold)

VIII - TRANSMIT FILTER COEFICIENTS

TXCOEF (R/W) Address of first pulse shaping/compromise equalizer complex coefficient (16-bit real,16-bit imag).

GAIN (R/W) Attenuation factor for the transmit filter.

SHIFTVAL (R/W) Gain (Left shift value) from 0 to 15. To be use in conjonction with GAIN for fine adjustment of the transmit signal. Up and down scaling.

The pass-band pulse shaping and transmit compromise equalizer functions are combined in the transmit filter coeficients. The pulse shaping also performs the multi-phase interpolation from different baud rates to a fixed sample rate 7200Hz (14400Hz for V.27 4800) thus requiring multiple coeficient sub-tables containing complex (16-bit real,16-bit imag) coeficients. The number of coeficients depends on the shape, baud rate,and sampling rate. A default table depending on the compromise equalizer selected in the conf command is loaded from coeficient memory to external memory, after which, if desired, they can be modified by the user. The table below summarizes the location and the number of coeficients to be loaded.

(* = DEFAULT VALUES)

MODE	BAUD RATE	PHASE	COEF/PHS	STRT ADR	ROLL-OFF*	NO. OF COMPEQ*
V.32/33/17	2400	0 1 2	32	TXCOEF (TXCOEF+64) (TXCOEF+128)	0.125	3
V.29	2400	0 1 2	24	TXCOEF (TXCOEF+48) (TXCOEF+96)	0.20	2
V.27(2400)	1200	0 1 2 3 4 5	8	TXCOEF (TXCOEF+16) (TXCOEF+32) (TXCOEF+48) (TXCOEF+64) (TXCOEF+80)	0.50	1(FLAT)
V.27(4800)	1600	0 1 2 3 4 5 6 7 8	7	TXCOEF (TXCOEF+14) (TXCOEF+28) (TXCOEF+42) (TXCOEF+56) (TXCOEF+70) (TXCOEF+84) (TXCOEF+98) (TXCOEF+112)	0.50	1(FLAT)
V.22 ORIG/ANS	600	0 1 2 3 4 5 6 7 8 9 10 11	5	TXCOEF (TXCOEF+10) (TXCOEF+20) (TXCOEF+30) (TXCOEF+40) (TXCOEF+50) (TXCOEF+60) (TXCOEF+70) (TXCOEF+80) (TXCOEF+90) (TXCOEF+100) (TXCOEF+110)	0.50	1(FLAT)

IX - TONE DETECTOR PROGRAMMING

LEVOUT (R/W) 16 Programmable static levels.

BIQCOEF (R/W) 16*2*6 Biquad coeficients.
Coef. order for each of 16 4th order cells :
C0, C1, C2, C3, C4, C5, C6, C7, C8, C9, CA, CB
Where each 4th order cell has the following xfer function :

$$\frac{OUT}{IN} = C0 \cdot \frac{C5 \cdot Z^2 + 2 \cdot C3 \cdot Z + 2 \cdot C4}{Z^2 - 2 \cdot C1 \cdot Z - 2 \cdot Z} \cdot C6 \cdot \frac{CB \cdot Z^2 + 2 \cdot C9 \cdot Z + 2 \cdot CA}{Z^2 - 2 \cdot C7 \cdot Z - 2 \cdot C8}$$

POWCOEF (R/W) 16 Power coeficients p1 Power estimator using absolute value of the input signal :

$$\frac{OUT}{IN} = P1 \cdot \frac{1}{Z - (1 - P1)}$$

BPWIRE (R/W) 16 Biquad and pwr estimator input wiring addresses.
FORMAT = [4TH ORDER BIQ(MSB),PWR(LSB)]

CPWIRE (R/W) 16 Comparator input wiring addresses.
FORMAT = [COMPARATOR+(MSB),COMPARATOR-(LSB)]
The wiring addresses furnished in bpwire,cpwire are from the following possible sources :

GND	$00
RX SIGNAL	$01
RX SIGNAL*2	$02
RX SIGNAL*4	$03
4TH ORDER BIQ BLOCK OUTPUT	$10 to $1F
POWER OUTPUT	$20 to $2F
STATIC LEVELS PROGRAMMED IN LEVOUT	$30 to $3F

_NTDCELL (R/W) Number of tone detector cells active (0-15)

_TONEDET (R) Outputs of tone detectors. The low byte of _TONEDET contains the outputs of tone detector cells 0 to 8. The low byte of _TONEDET+1 contains outputs of cells 9 to 15. When the corresponding bit is "1" the signal at the positive input of the comparator is higher than that at the negative input. Only _NTDCELL bits are valid at one time, the other one are 0.

	TONEDET0		TONEDET1
D0	CALL WAIT BPF 440Hz	D0	AN1300 BPF
D1	RXSIG < -21dBM	D1	ORG : AN1300 > AZ1800 ANS : AN1300 > OZ2100
D2	CPLOW LPF 650Hz	D2	AN1650 BPF
D3	CPHIGH HPF 600Hz	D3	ORG : AN1650 > AZ1800 ANS : AN1650 > OZ2100
D4	CPHIGH < CPLOW	D4	ORG : ANS2100 BPF ANS : ORG1800 BPF
D5	ORG: AZ1800 NOTCH ANS: OZ2100 NOTCH	D5	ORG : ANS2100 > AZ1800 ANS : ORG1800 > OZ2100
D6	AN600 BPF 600Hz	D6	ANS2225 BPF
D7	ORG : AN600 > AZ1800 ANS : AN600 > OZ2100	D7	ORG : ANS2225 > AZ1800 ANS : ANS2225 > OZ2100

X - GENERAL PURPOSE

_TXGAIN (R/W) Transmit gain. Any signal to transmit is multiplied by this number. This is the value modified by SETGN command.

XI - TONE GENERATOR

_TGNFLG (R/W) Tone generator flag. Each of the four low bits of this variable define if the corresponding tone generator is enabled. This is the value modified by a TGEN command.

_TG0PHC (R/W) Tone generator #0 phase reversal threshold. If different from 0, a phase reversal will be executed on the tone genarator #0 after _TG0PHC bauds. This is used in V.32 answer tone generation (default value is 1080 for 450ms).

_TGNBLK (R/W) For each of the four tone generators (i) contains:
_TGNBLK+(3*i): Frequence of tone (i.e. $4000 = 1800Hz).
_TGNBLK+1+(3*i): Instantanous phase.
_TGNBLK+2+(3*i): Amplitude ($7FFF refers to maximum signal).

XII - DEFAULT OPTIONAL STATUS

UADDR (R/W) Size 3 : address of the DSP's variable regulary displayed into the optionnal status word. These address can be modified with the DOSR command.

XIII - RING

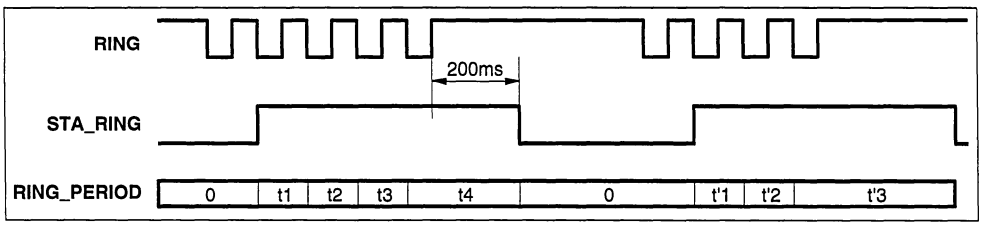
RNG_FMIN (R/W) The default value for this variable is 35. A ring signal of 68Hz is periodic every 35 bauds at 2400Hz.

RNG_FMAX (R/W) The default value for this variable is 160. A ring signal of 15Hz is periodic every 160 bauds at 2400Hz.

RING_PERIOD (R) Output of the RING detector. This word is identiqual to the STAOP2 byte when in tone mode (neither DTMF receiver neither modem mode). The content of that word is the duration of the RING period. The formula to compute the RING frequency is :

$$\text{RING\_frequency} = \frac{2400}{\text{RING\_PERIOD}} \text{ in Hz.}$$

Figure 2



XIV - ADPCM

NOISE (R/W) The default value is $C after CONF command and can be modified to increase or decrease the background noise level in the voice activity detection algorithm. The value is complemented at the sample rate giving a periodic signal at 3600Hz.

TRANSMAX (R/W) The default value is 90 after CONF command and represents, in each frame of 30ms, the maximum number of transitions or zero-crossings to keep the voice activity detector active. The internal signal, VOICE, represents the output of this detector and is updated every 30ms.

CNTMAX (R/W) The default value is 14400 (2s) after CONF command and represents the preload value for a counter. The counter is update at the sample rate of 7200Hz. It is either preloaded if VOICE (from above) is active or decremented if VOICE is inactive. If the counter is not 0, CARRIER DETECT is raised. Effectively, the user can increase (decrease) the duration of CARRIER DETECT after loss of a voice signal by increasing (decreasing) the value of CNTMAX.

PRGTHRSH (R/W) The voice activity detector has an absolute signal level threshold in parallel with the zero-crossing detector described above. The default value of PRGTHRSH is 0 after the CONF command and designates the threshold to be the average level measured during the previous detection of voice activity by the zero-crossing method. If PRGTHRSH is changed by the user to a non-zero value, the actual value programmed is the threshold for the detector. Thus, the absolute signal detector can be disabled by programming a large value such as $7fff for PRGTHRSH.

XV - APPENDIX : Address Equivalences for Version 1.0 and 1.2

Variable	Address
ECHO CANCELLER	
_RTDELAY	$1016
_EC_STA	$1019
PWREST	$1BAD
FREOFF	$1BB1
DELTA	$1BBD
FEECENBL	$1BCE
TIMING RECOVERY	
FRQOFFT	$1E8C
PSITHRSH	$1E97
CARRIER RECOVERY	
FRQOFF	$1EA3
EQUALIZER,AGC	
_RX_STA	$1017
_AGCSCA	$1193
RDQUA	$12A7
_RDCPT	$1048
EQFRK0E	$1CBC
EQFRK1E	$1CFC
STAQUA	$1058
SCAQUA	$12A6
_SUCTH	$1FCE
HANDSHAKE,RETRAIN, RATE NEGOTIATION	
HSHK_PHA	$11BB
_RE_HSK	$11BD
_TSPEED	$11AF
_TRWORD	$11B0
_RWORD	$1014
RNTHRSH	$12AA
_CURMOD	$1011
_SSPEED	$11BA
_STAV54E	$11A1
CARRIER DETECT	
DETH1	$1F9A
DETH	$1F99
LOSSTH1	$1F9C
LOSSTH	$1F9B

Variable	Address
TRANSMIT FILTER COEFICIENTS	
TXCOEF	$12E4
GAIN	$12E2
SHIFTVAL	$12E1
TONE DETECTOR PROGRAMMING	
LEVOUT	$13E6
BIQCOEF	$1476
POWCOEF	$1536
BPWIRE	$1456
CPWIRE	$1466
_NTDCELL	$1006
_TONEDET	$1007
GENERAL PURPOSE	
_TXGAIN	$1001
TONE GENERATOR	
_TGNFLG	$1002
_TG0PHC	$1003
_TGNBLK	$13A8
DEFAULT OPTIONNAL STATUS	
UADDR	$1E6E
_TONEDET	$1007
DTMF_DIGIT	$174A
NEG_MODE	$11BA
HSHK_PHA	$11BB
STA_LOOP	$11A1
RING_PERIOD	$1DD8
RING	
RNG_FMAX	$1DDC
RNG_FMIN	$1DDB
RING_PERIOD	$1DDA
ADPCM	
NOISE	$1595
TRANSMAX	$1596
CNTMAX	$1599
PRGTHRSH	$159F

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

HOW TO USE THE DUAL PORT RAM FOR PARALLEL DATA TRANSFER WITH THE ST75C502

By Laurent CLARAMOND

CONTENTS — Document page

I - INTRODUCTION

I.1 - Overall

This application note describes the way to use the ST75C502 Data Buffers.

These Data Buffers are implemented into the DUAL RAM of the ST75C502. They are shared between the Host processor and the ST75C502. A mechanism of Flags and interrupts is associated with them to allow an easy management of the Data.

I.2 - Cautions

The mechanism described below is only valid while in regular Data Transmission, not in Handshaking neither in Call progress (or DTMF) tone detection modes.

I.3 - Notations

Any ***bold_italic*** command refers to reserved Nam.
"Host" refers to the Micro-controller connected to the ST75C502 Data Pump.
"Transmit Data" (or Tx) means Data transfered by the ST75C502, via the modulator, to the telephone line, and "Receive Data" (or Rx) means Data coming from the telephone line and demodulated by the ST75C502.

II - PARALLEL DATA EXCHANGE

II.1 - Overview

While in Parallel Mode, the transmitted (respectively Received) Data to (from) the telephone line are exchanged between the Host and the ST75C502.

Two totally independent channels are provived for Transmit and Receive Data. Even while using Half Duplex modes of operation, the transmitted data comes from the Transmit buffers and the receive Data arrives in the Receive buffers.

Two independent Interrupts, ***IT2*** (for Transmit) and ***IT3*** (for Receive) are available for synchronizing the ST75C502 and the Host. An additional ***IT0*** interrupt will signal the errors in the synchronization mechanism.

The equivalent Data Flow is shown in Figure 1.

II.2 - Select Parallel Mode

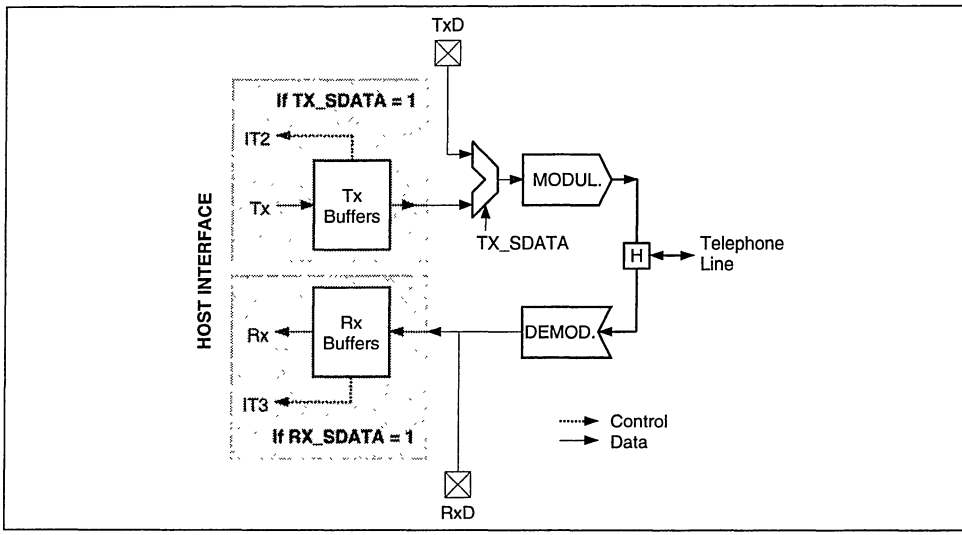
The ***SERIAL*** command allows the independent selection of the parallel mode for the Transmit and/or Receive Data path. The parameter syntax is as follows :

Field	Byte	Pos.	Value	Definition
TX_SDATA	1	0	0*	Use Serial Link for Tx Data
			1	Use Parallel Link for Tx Data
RX_SDATA	1	1	0*	Use only Serial Link for Rx Data
			1	Use both Serial an Parallel Link for Rx Data

Note : Even if the parallel mode is selected for the Receiver, the Received Bit Stream is available on the RxD pin of the ST75C502.

This command must be sent in Data Mode, when the Transmit or Receive data links are established. This corresponds with the presence of the signals ***STA_106*** (for Tx) and/or ***STA_109*** (for Rx).

Figure 1



II - PARALLEL DATA EXCHANGE (continued)

II.3 - Transmit Buffers

Two identical buffers are provided to exchange the data between the Host interface and the ST75C502. When the Host is writing data into a buffer, the ST75C502 is transmitting the other one. After that, both the Host and the ST75C502 switch to use the other buffer. This mechanism, called "Double-Buffering", ensures that the host has the maximum time to fill one buffer. The DUAL RAM area associated with the transmit buffers is as follows :

Name	Address	Description
DTTBS0	$2E	Buffer 0 Status Byte
DTTBF0[0]	$2F	Buffer 0 Data Byte 0
DTTBF0[1]	$30	Buffer 0 Data Byte 1
DTTBF0[2]	$31	Buffer 0 Data Byte 2
DTTBF0[3]	$32	Buffer 0 Data Byte 3
DTTBF0[4]	$33	Buffer 0 Data Byte 4
DTTBF0[5]	$34	Buffer 0 Data Byte 5
DTTBF0[6]	$35	Buffer 0 Data Byte 6
DTTBF0[7]	$36	Buffer 0 Data Byte 7
DTTBS1	$37	Buffer 1 Status Byte
DTTBF1[0]	$38	Buffer 1 Data Byte 0
DTTBF1[1]	$39	Buffer 1 Data Byte 1
DTTBF1[2]	$3A	Buffer 1 Data Byte 2
DTTBF1[3]	$3B	Buffer 1 Data Byte 3
DTTBF1[4]	$3C	Buffer 1 Data Byte 4
DTTBF1[5]	$3D	Buffer 1 Data Byte 5
DTTBF1[6]	$3E	Buffer 1 Data Byte 6
DTTBF1[7]	$3F	Buffer 1 Data Byte 7

The Bit 0 (LSB) of the Buffer 0 Data Byte 0 is the first in time to be transmited.

A value of 0 in the Status Byte of the Buffer signals to the Host that a buffer is empty. This value is set by the ST75C502 each time it has emptied the buffer. After having used one buffer, the host must select the other buffer for the next operation. The host must start with the Buffer 0 as soon as the ***ST_106*** signal is on and the ***SERIAL Tx*** is selected and BEFORE the ***XMIT 1*** command is sent.

A mechanism of interruption (***IT2*** for Transmit) is associated with the Data Buffer management. Each time a Buffer is emptied by the ST75C502 it generates an interrupt.

II.4 - Receive Buffers

Symetrically two identical buffers are provided to exchange receive data between the ST75C502 and the Host processor. While the ST75C502 is filling one of the buffers with the receive bits, the Host processor is reading the other buffer. As soon as the host has emptied a buffer it frees it by writing 0 in the Buffer Status Byte.

The DUAL RAM area associated with the receive buffers is as follows :

Name	Address	Description
DTRBS0	$1C	Buffer 0 Status Byte
DTRBF0[0]	$1D	Buffer 0 Data Byte 0
DTRBF0[1]	$1E	Buffer 0 Data Byte 1
DTRBF0[2]	$1F	Buffer 0 Data Byte 2
DTRBF0[3]	$20	Buffer 0 Data Byte 3
DTRBF0[4]	$21	Buffer 0 Data Byte 4
DTRBF0[5]	$22	Buffer 0 Data Byte 5
DTRBF0[6]	$23	Buffer 0 Data Byte 6
DTRBF0[7]	$24	Buffer 0 Data Byte 7
DTRBS1	$25	Buffer 1 Status Byte
DTRBF1[0]	$26	Buffer 1 Data Byte 0
DTRBF1[1]	$27	Buffer 1 Data Byte 1
DTRBF1[2]	$28	Buffer 1 Data Byte 2
DTRBF1[3]	$29	Buffer 1 Data Byte 3
DTRBF1[4]	$2A	Buffer 1 Data Byte 4
DTRBF1[5]	$2B	Buffer 1 Data Byte 5
DTRBF1[6]	$2C	Buffer 1 Data Byte 6
DTRBF1[7]	$2D	Buffer 1 Data Byte 7

The Bit 0 (LSB) of the Buffer 0 Data Byte 0 is the first received bit in time (the oldest).

A value of 0 in the Status byte of the Buffer signals to the ST75C502 that a buffer is empty. This value is set by the Host each time it has emptied the buffer. After having used one buffer, the host must select the other buffer for the next operation. The Host must start with the Buffer 0 as soon as the ***STA_109*** signal is on and the ***SERIAL Rx*** is selected.

A mechanism of interruption (***IT3*** for Receive) is associated with the Data Buffer management. Each time a buffer is filled by the ST75C502 it generates an interrupt.

II - PARALLEL DATA EXCHANGE (continued)

II.5 - Interruption

Two Interrupt signals are provided in order to synchronize the Data Buffer Exchanges. ***IT2*** is associated with the Transmit Buffer mechanism and ***IT3*** with the Receive Buffer mechanism.

In order to enable these interrupts, the Host processor must set the bit 2 (for ***IT2***) and the bit 3 (for ***IT3***) of the ***ITMASK*** Register to 1. It must also set the Bit 7 of the ***ITMASK*** register to 1 in order to globally enable all the selected sources of interruption.

When an Interrupt occurs (low level on $\overline{SINTR}$ pin) the user must read the ***ITSRCR*** Register to determine the source of the interrupt, either ***IT2*** for Tx (if the bit 2 is 1) or ***IT3*** for Rx (if the bit 3 is 1).

Once the Interrupt has been serviced, the host must acknowledge it by writing a $00 value into the register ***ITRES2*** for ***IT2***, or ***ITRES3*** for ***IT3***.

These registers have the following address :

Name	Address	Type	Description
ITRES2	$42	Write Only	Clear IT2
ITRES3	$43	Write Only	Clear IT3
ITMASK	$4F	Read/Write	Interrupt Mask
ITSRCR	$50	Read Only	Interrupt Source

Notes : 1. The ST75C502 does not check that the interrupt has been acknowledged.

2. Even if the Host does not use the interruption, the ST75C502 will set the bit 2 (for ***IT2***) and/or bit 3 (for ***IT3***) of the ***ITSRCR***.

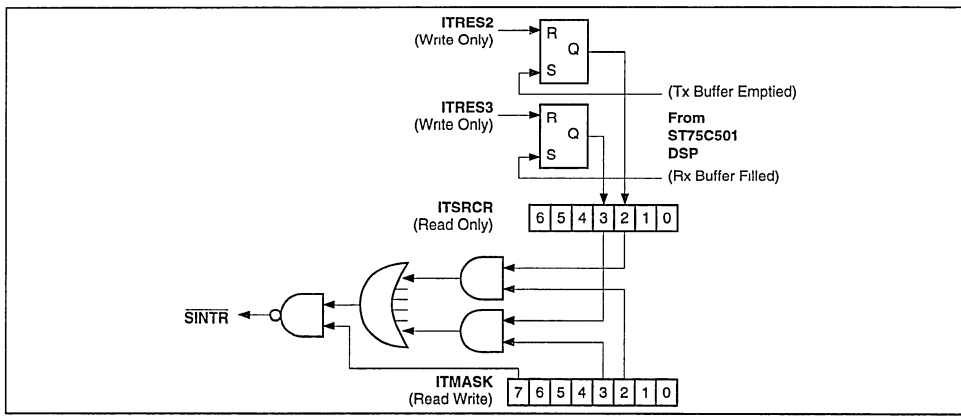
3. The ST75C502 uses only the Data Buffer Status Bytes to detect Overrun or Underrun Error. These errors are reported into the ***SYSERR*** byte, and could generate an interrupt ***IT0***.

The equivalent schematic is shown in Figure 2.

The interrupt mechanism assumes that the Host processor uses a Level sensitive interrupt (active low). The Flow chart of the Host interrupt service routine looks generaly like Figure 3.
The transmitter reads the bits in the DUAL RAM Buffer ***DTTBFx*** (starting with the Bit 0 of Byte 0 of Buffer 0) and sends them over the telephone line. The Buffer Status Byte ***DTTBSx*** contains the number of Data Bytes to transmit.
The receiver write the received bits comming from the Telephone line and write them into the DUAL RAM Buffer ***DTRBFx*** (starting with the Bit 0 of the Byte 0 of the Buffer 0). The Buffer Status Byte ***DTRBSx*** contains the number of Data Bytes received (generaly 8).
The time between each ***IT2*** interrupts (or ***IT3***) is equal to 64 bit if the number of Data Bytes is set to 8. The Host has the full 64 bits time to serve the interrupt :

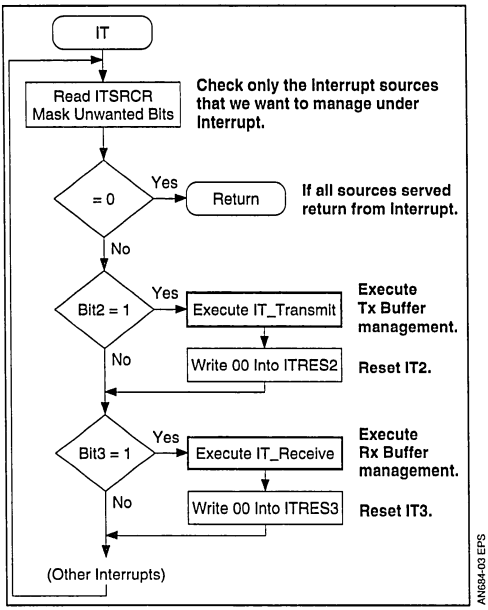
	Bit Rate (bps)	Interrupt Time (ms)
Modem	14400	4.4
	12000	5.3
	9600	6.6
	7200	8.8
	4800	13.3
	2400	26.6
	1200	53.3
	300	213.3
	75	853.3
Voice	A-Law	1.1
ADPCM	28.8k	2.2
	21.6k	2.9
	14.4k	4.4

Figure 2



II - PARALLEL DATA EXCHANGE (continued)

Figure 3



II.6 - Transmitting in Parallel Mode

II.6.1 - Description

When the ***STA_106*** (CTS) signal is on, the user must select the parallel mode by enabling the parallel link with ***TX_SDATA*** bit set in ***SERIAL*** command. After that the ST75C502 will start transmitting continuous "1". Note that for a proper operation each time the ***STA_106*** signal goes on, the ***SERIAL*** command must be sent.

II.6.1.1 - XMIT Command

The ***XMIT*** Command works like a CTS signal for the Parallel process.

When ***XMIT*** is off, the ST75C502 transmits continuous "1". When on the ST75C502 transmits Data and starts to manage the Data Buffer.

This command can be sent at any time, while in Data Mode.

Field	Byte	Pos.	Value	Definition
TX_START	1	0	0*	(OFF) Send continuous "1" (1)
			1	(ON) Send data according

Note : 1. The XMIT Off command takes effect only when the two Transmit buffers are empty : ***DTTBF0*** and ***DTTBF1*** equal to $00.

II.6.1.2 - STOP Command

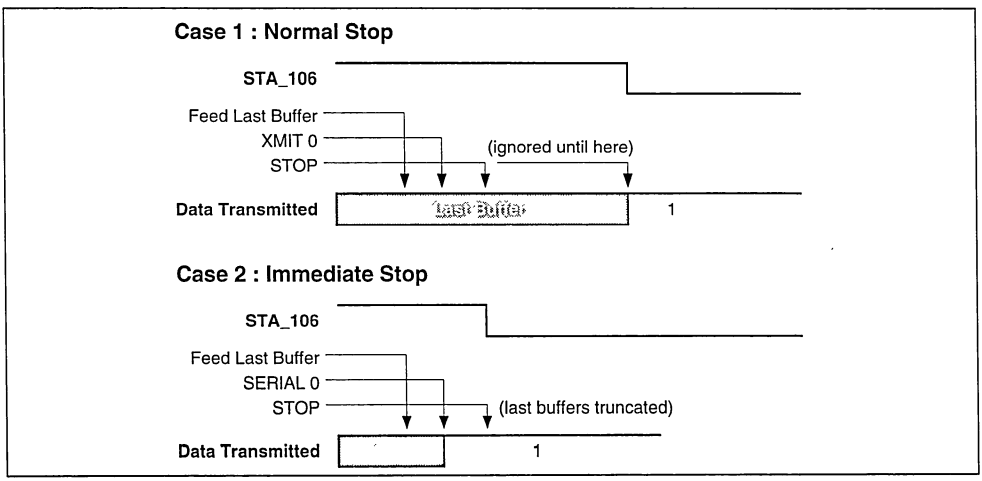
The ***STOP*** command is used in FAX Mode, at the end of the transmission, to stop sending the carrier on the telephone line.

Prior to the ***STOP*** command the user must have stop the parallel transmission with a ***XMIT off*** command.

II.6.1.3 - Timing

Here are regular sequences to stop properly the transmission (See Figure 4).

Figure 4



II - PARALLEL DATA EXCHANGE (continued)

II.6.1.4 - FSK Full Duplex Mode

In FSK Full Duplex Mode the Parallel Mode assumes that the bit time duration is the nominal bit rate. Each bit element from the Transmit buffer is maintained during the full bit time. The nominal bit clock is defined as follows :

FSK Standard	Nominal Transmit Bit Rate (Hz)(1)	Bit Clock on Rx Pin (Hz)	Bit Clock on Tx Pin (Hz)
V.21	300	9600	7200
Bell 103	300	9600	7200
V.23 Originate	75	9600	7200
V.23 Answer	1200	9600	7200

Note : 1. The accuracy of the Bit clock is given by the ST75C502 oscillator, and must better than 50ppm.

II.6.2 - Modem Flow Chart

When in the Parrallel Data Mode, each time the ST75C502 need a bit to transmit it executes the following routine (See Figure 5).

Where x starts with the value 0 and toggle thereafter between 1 and 0.

II.6.3 - Host Flow Chart

Here after are Flowcharts to :

- Establish a V.29 transmission.
- Send synchronous continuous "$AA, $55, $AA, $55, ..." sequence. The management of the Buffers are done under interrupt.
- Stop properly the transmission.

Establish a V.29 transmission and send the very first Buffer (see Figure 6).

Figure 5

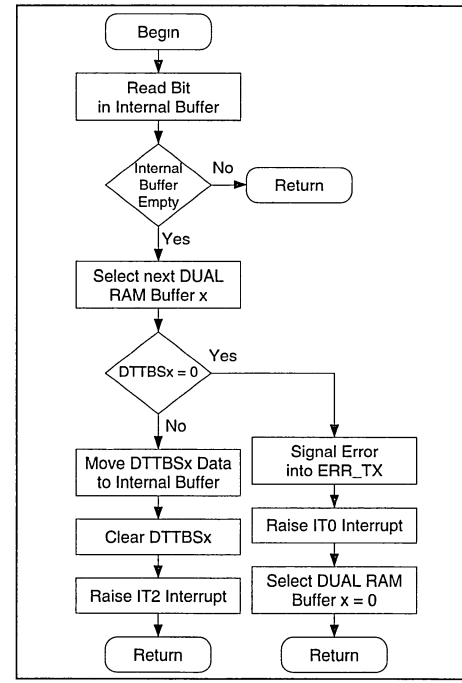
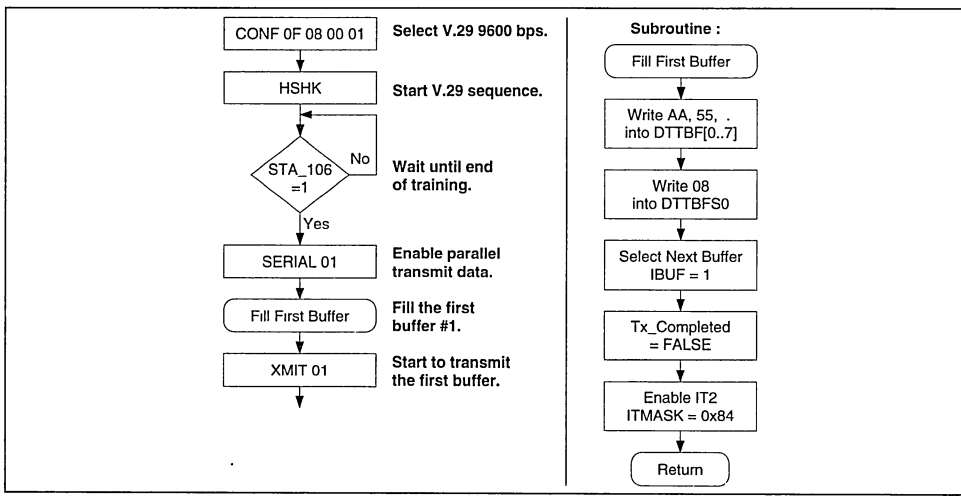


Figure 6



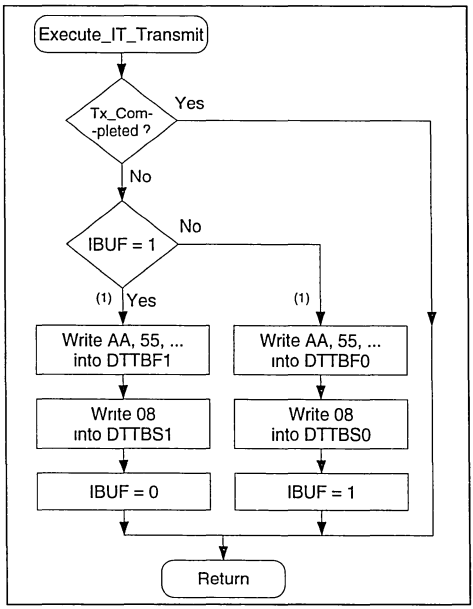
II - PARALLEL DATA EXCHANGE (continued)

These flowcharts show two CPU variables labeled ***IBUF*** and ***Tx_Completed***, they are necessary for the understanding of the mechanism, but there is different manners to implement it. These two variables have the following meanning :

- ***IBUF***: This is the number of the DUAL RAM Buffer currently in use by the Host processor. It starts with 0 and then alternate 1, 0, 1, 0, ...
- ***Tx_Completed***: This is a Flag to dialog with the interrupt process in order to stop properly the transmission.

The other Buffers are sent under interrupt control (refer to the interrupt flow chart, Figure 7).

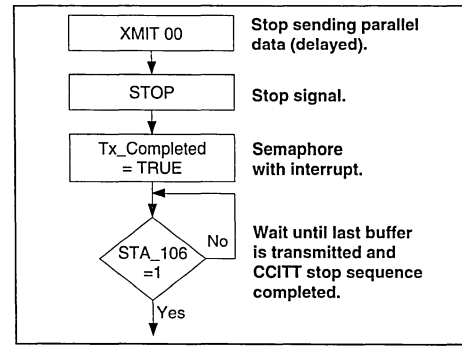
Figure 7



Note : 1. At this step the host can check that the corresponding ***DTTBSx*** buffer is empty (equal to $00), otherwise it is an error

To stop properly the transmission, without loss of Data (See Figure 8).

Figure 8



II.6.4 - Error Detection

Error occurs when the ST75C502 need some bits from the transmit buffer ***DTTBSx*** and this buffer is empty. This condition is called "Underflow".

This error is signaled in the bit ***ERR_TX*** of the ***SYSERR*** byte, and generates an interrupt ***IT0***. To clear the error a ***CSE 01*** command must be issued.

An Underflow condition occurs when the host processor "forgets" to feed the current ***DTTBSx*** buffer.

When an Underflow condition occur the Host must restart the whole parallel initialization, as explained above.

II.6.5 - Data Transmission

II.6.5.1 - Description

The ST75C502 transmits the bits contained in the DUAL RAM Buffer without any modification. It starts with the Bit 0 of the ***DTTBF0[0]*** byte.

II.6.5.2 - Status Word Format

The Transmit Status Bytes ***DTTBS0*** or ***DTTBS1*** have the same meaning (See Table 1).

This status byte must be written by the Host, after filling the corresponding data buffer ***DTTBFx[0..7]*** with the right number of data bytes to transmit.

This status byte is cleared by the ST75C502, just before generating the ***IT2*** interrupt.

Table 1 : DTTBSx in Synchronous Mode

Field	Pos.	Value	Definition
BUFF_LENG	3..0	0	Buffer empty
		1	1 Byte to transmit (***DTTBFx[0]***)
		2	2 Bytes to transmit (***DTTBFx[0]*** and ***DTTBFx[1]***)
		...	...
		8	8 Bytes to transmit (***DTTBFx[0..7]***)
		Other	Not allowed
Other	7..4	0	Reserved, must be 0

AN684-01 TBL

II - PARALLEL DATA EXCHANGE (continued)

II.7 - Receiving in Parallel Mode

II.7.1 - Description

When the ***STA_109*** (CD) signal goes on, the user must select the parallel mode by enabling the parallel link with ***RX_SDATA*** set in the ***SERIAL RX*** command. After that the ST75C502 will write received data into the DUAL RAM buffer ***DTRBS0***. Note that for a proper operation, each time the ***STA_109*** goes on the ***SERIAL*** command must be send.

II.7.1.1 - Initialization

The host processor must enable the ***IT3*** receive interrupt first.

Then it must empty the two ***DTRBS0*** and ***DTRBS1*** registers by writting $00 at these locations.

Then it must send the ***SERIAL RX*** command.

As soon as the first ***IT3*** interrupt appears, the host must proceed with the ***DTRBS0*** buffer.

II.7.1.2 - Loss of Carrier

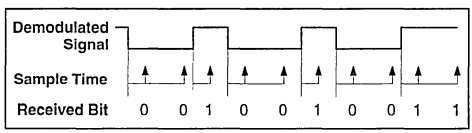
Each time a loss of carrier appears the ST75C502 stops updating the data buffer.

If the carrier reappers the host must proceed again with the INITIALIZATION sequence.

II.7.1.3 - FSK Synchronization

The FSK Full Duplex demodulator uses an algorithm based on the transitions of the received signal. The synchronization mechanism is adjusted with each signal transition in order to sample the demodulated signal at the midle of the bit (see Figure 9).

Figure 9

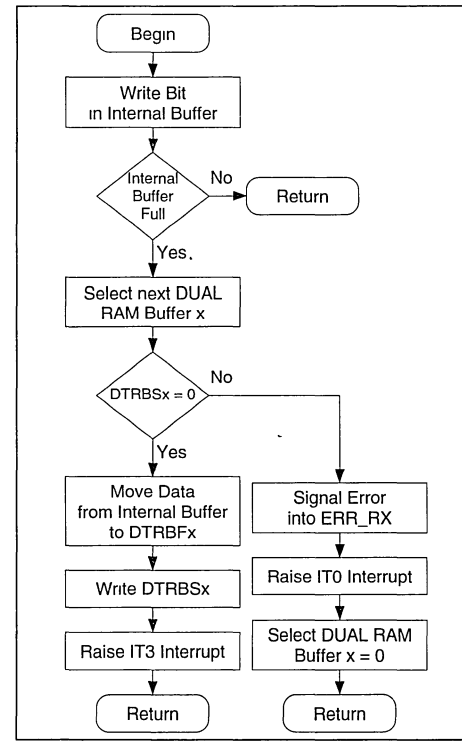


II.7.2 - Modem Flow Chart

When in parallel data mode, each time the ST75C502 has received some bit of data it executes the following routine (see Figure 10).

Where x start with the value 0 and toggle between 1 and 0.

Figure 10



II.7.3 - Host Flow Chart

Hereafter are flowcharts to :

- Establish a V.29 reception.
- Receive synchronous data. This task is performed under interrupt.
- Handle properly some temporary loss of carrier.

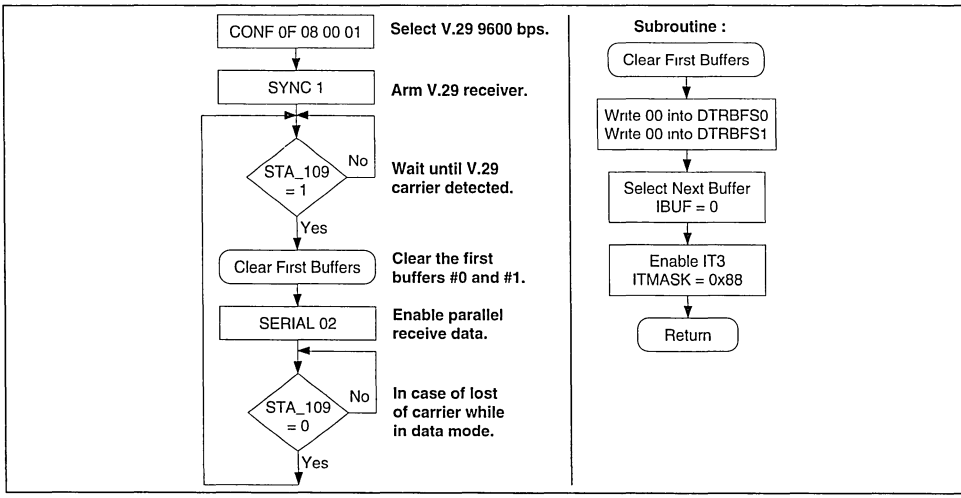
Establish the reception (see Figure 11).

These flowcharts show one CPU variable labeled ***IBUF*** which is necessary for the understanding of the mechanism, but there are different manners to implement it.

- ***IBUF***: this is the number of the DUAL RAM buffer currently in use by the Host processor. It starts with 0 an then alternates 1, 0, 1, 0, ...

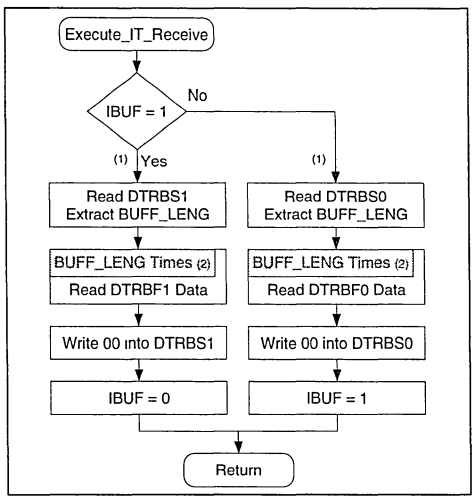
II - PARALLEL DATA EXCHANGE (continued)

Figure 11



The received bits are read by an interrupt routine (see Figure 12).

Figure 12



Notes : 1. At that step the host can check that the corresponding ***DTRBSx*** buffer is full (different from $00), otherwise it is an error.

2. This means read ***BUFF_LENG*** bytes, inside the Receive buffer ***DTRBFx*** starting from location ***DTRBFx[0]*** to ***DTRBFx[BUFF_LENG - 1]***
The ***BUFF_LENG*** is always 8 bytes, except when a ***STA_109*** lost appears in the middle of the buffer.

II.7.4 - Error Detection

Error occurs when the ST75C502 has received some bits and that the buffer ***DTRBSx*** is not empty, this condition is called "Overflow".

This error is signaled in the bit ***ERR_RX*** of the ***SYSERR*** byte, and generates an interrupt ***IT0***. To clear the error a ***CSE 02*** command must be issued.

An Overflow condition occurs when the host processor "forgets" to empty the current ***DTRBSx*** buffer.

When an Overflow condition occurs the host must restart the whole parallel INITIALIZATION.

II.7.5 - Data Reception

II.7.5.1 - Description

The ST75C502 writes the received bit into the DUAL RAM Buffer without any modification. It starts with the Bit 0 of the ***DTRBF0[0]*** byte.

II.7.5.2 - Status Word Format

The receive Status Byte ***DTRBS0*** or ***DTRBS1*** have the same meaning (see Table 2).

The ***BUFF_LENG*** is always 8 except when a lost of carrier (***STA_109*** going to 0) happens.

This status byte is set by the ST75C502, just before generating the ***IT3*** interrupt.

II - PARALLEL DATA EXCHANGE (continued)

Table 2 : DTRBSx in Synchronous Mode

Field	Pos.	Value	Definition
BUFF_LENG	3..0	0 1 2 ... 8 Other	Buffer empty 1 Byte to transmit (***DTRBFx[0]***) 2 Bytes to transmit (***DTRBFx[0]*** and ***DTRBFx[1]***) ... 8 Bytes to transmit (***DTRBFx[0..7]***) Not used
Other	7..4	0	Not used

AN684-02 TBL

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SET-UP, HANDSHAKE AND COMMUNICATION MONITORING IN MODEM AND FAX MODE WITH THE ST75C502

By Laurent CLARAMOND

CONTENTS — Document page

I - INTRODUCTION

I.1 - Overall

The ST75C502 is a complete and powerful modem/fax data pump which provides all the facilities to establish modem connections from the V.32bis at 14400bps to the V.23 at 75/1200bps or 1200/75 bps and fax communications from V.17 at 14400bps to V.27ter at 4800bps.

Such a component is always used via a microcontroller (MCU). The software interface (often called modem_driver) between the MCU and the data pump will incorporate all the functions needed to use the component. To write these functions the engineer has to :

- understand how to perform the set up of the data pump,
- understand how the handshake is done and what kind of monitoring is required by the MCU,
- understand how the communication must be supervised using status given in real time by the data pump.

So the purpose of this application note is to provide all the information for the set up, the handshake and the communication monotoring. In other words, we would like to give the answers before the engineer asks for questions. Examples will be given each time they may help to understand.

I.2 - SATURN Modem Driver

SGS-THOMSON has developed an application board called SATURN. It looks like a stand alone modem/fax Hayes compatible which allows asynchronous and synchronous communications. We will take the examples from the modem driver written for this application.

I.3 - Notations

Any ***bold_italic*** command refers to reserved Name.

0x value means a value given in hexadecimal.

0b value means a value given in binary.

II - TYPICAL SOFTWARE FUNCTIONS FOR MODEM AND FAX COMMUNICATION

The main loop of the SATURN software uses the functions available in the modem driver called DP_ST.C. The set up, the handshake and the communication monitoring are separated in more than three functions (more than one for each task) to have a structured software which could be easily modified. To help the engineer to write his software we give some of these functions used in SATURN modem/fax application as example.

- Channel establishement :
  - dp_set_modulation_type()
  - dp_init_handshake()
  - dp_monitor_handshake()
  - dp_get_modulation_type()
  - dp_get_rate_sequence()
  - dp_analyzer()
- Line interface monitoring :
  - dp_carrier_detect()
  - dp_init_retrain()
  - dp_init_rate_renegotiation()
  - dp_detect_retrain()
- Fax operation :
  - dp_set_idle()
  - dp_set_v21_detector_fax()
  - dp_detect_v21_fax()
  - dp_detect_v21_in_high_speed_fax()
  - dp_facsimile_data_mode()

II.1 - Function Definition

dp_set_modulation_type() :
Configures the data pump to begin handshaking with the modulation type required. An argument could be used to determine if the data pump can fallback to slower speed if the communication cannot be established at the initial speed.

dp_init_handshake() :
Begins handshaking according to the configuration specified by dp_set_modulation_type().

dp_monitor_handshake() :
Monitors the progression of the handshake during channel establishment and give a message result. This function must be called repeatedly by the main loop until a final message is return.

dp_get_modulation_type() :
When in data mode, gets the data pump's current modulation type.

dp_get_rate_sequence() :
Give the last V.32, V.32bis rate sequence received.

dp_analyzer() :
This function is called repeatedly by the main loop. Some monitoring required by the data pump could be placed in this function.

dp_carrier_detect() :
This function tests if the received carrier is detected.

dp_init_retrain() :
This function requests to the data pump to initiate a retrain using the current configuration. This function could use two arguments, one to select the fastest modulation type to be used to start the handshake and one to allow a fallback to slower speed if the data pump can fallbak to slower speed if the communication cannot be established at the initial speed.

dp_init_rate_renegotiation() :
This function requests to the data pump to initiate a rate negotiation in V.32bis. An argument could be used to defined the new modulation type desired.

dp_detect_retrain() :
This function detects if a retrain or a rate negotiation initiated by the remote modem is in progress.

dp_set_idle() :
This function is only used in fax mode. The data pump returns in idle mode. In this mode, the data pump stops transmitting or receiving and waits for a new modulation type.

dp_set_v21_detector_fax() :
This function could be called by a fax module in originate. Prepare the data pump to detect V.21 ch2 modulation using dp_detect_v21_fax().

dp_detect_v21_fax() :
This function is only called by a fax module in originate. Interrogate the data pump about detecting V.21 ch2 modulation. This function must be called repeatedly by the main loop while sending CNG tone (ITU_T tone at 1100Hz).

dp_detect_v21_in_high_speed_fax() :
Function only used in fax mode. When the data pump is configured in high speed mode (V.27, V.29 and V.17) reception, this function tests if the remote modem is sending V.21 ch2 modulation.

dp_facsimile_data_mode() :
Function only used in fax mode. When the data pump is configured in high speed mode (V.27, V.29 and V.17) reception, this function detect if the data pump is in data mode.

III - FIRST STEP : SET-UP OF THE DATA PUMP

The set up of the ST75C502 is done using the two main commands ***CONF*** and ***MODC***.

The ***CONF*** command is essential since it is the only way to select one of the different operating modes for the Transmit and the Receive part.

The following table shows the possible operation mode :

CONF_OPER	Transmit	Receive
0000 *	Tones	Tones
0010	Voice	Tones
0100	Tone	DTMF
0110	Voice	DTMF
1000	Tones	Voice
1010	Voice	Voice
1111	Modem	Modem
Other	Not allowed	Not allowed

* Default value.

The ***CONF*** command needs 4 parameters which must be used each time. The parameters are byte size, byte 1 being the first and byte 4 the last. The Table 1 shows the meaning of the parameters.

The ***MODC*** command is used to modified default parameters value which will be used when the data pump will do the handshake and also to enable or disable some particular type of operation.

Here after we give some example of modifications that could be request by the application :
- the user can select two kind of guard tone in V.22 and V.22bis (answer mode only),
- the application requests a short train sequence instead a long train sequence in V.17 to send data while in C phase of the FAX T.30 protocol.

The selection of the modifications is done using 2 parameters (byte size) with the ***MODC*** command. The Table 2 shows the meaning of the parameters.

The purpose of the set up phase is to initialize with the good value some of the parameters of the ***CONF*** and ***MODC*** command. The others ***CONF***'s parameters and ***MODC***'s parameters will be initialized when the software will do the initialisation of the handsahke (select leased line, transmit equalizer, ...). Mainly the set up phase will select auto-mode or fixed mode and the wanted speeds.

Table 1

Field	Byte	Pos.	Value	Definition
CONF_OPER	1	3..0	-	Mode of operation see above
CONF_ANAL	1	4	0 1	Normal mode Analog loop back
CONF_PSTN	1	5	0 1	PSTN (carrier detect -43/-48dBm) Leased line (carrier detect -33/-38dBm)
CONF_AO	1	6	0 1	Answer mode (see Note) Originate mode (see Note)
CONF_MODE	2	5..0	0 1 2 3 4 5 6 7 8 9 A B C D Other	Automode Bell 103 Bell 212A V.21 V.23 V.22 V.22bis V.27ter V.29 V.17 V.32 V.32bis V.33 V.21 Channel 2 Reserved
CONF_TXEQ	2	7..6	0 1 2 3	No transmit equalizer Transmit equalizer #1 (1/2 of M1020) Transmit equalizer #2 (1/2 of M1040) Reserved
CONF_QAM	3	0	0 1	QAM/DPSK only (Automode) FSK allowed (Automode)
CONF_TCM	3	1	0 1	Treillis coding not allowed (V.32 only) Treillis coding allowed (V.32bis, V.32)
CONF_SP0	3	7..2	xxxx01 xxxx0x xxx10x xx1x0x x1xx0x 1xxx0x	300bps allowed(V.21, Bell 103) Reserved (must be set to 0) 1200bps allowed (V.22, V.22bis, V.23, Bell 212A) 2400bps allowed (V.22bis, V.27) 4800bps allowed (V.32bis, V.32, V.29, V.27) 7200bps allowed (V.32bis, V.29, V.17)
CONF_SP1	4	2..0	xx1 x1x 1xx	9600bps allowed (V.32bis, V.32, V.29) 12000bps allowed (V.32 bis, V.33, V.17) 14400bps allowed (V.32bis, V.33, V.17)

AN816-01 TBL

Table 2

Field	Byte	Pos.	Value	Definition
MODC_SH	1	6	0* 1	Normal training sequence Short training sequence
MODC_V22G	2	1..0	00* 01 10	No guard tone 1800Hz guard tone 550Hz guard tone
MODC_FPT	2	3..2	00* 10	No echo protection tone Long echo protection tone (180ms) (FAX only)
MODC_NOTA	2	4	0* 1	Answer : generate answer tone for handshake Originate : wait answer tone for handshake Answer : do not generate answer tone for handshake Orignate : do not wait answer tone for hansshake
MODC_NOSA	2	6	0* 1	Cut answer tone when receiving AA (V.32bis (short train sequence must be preceded by at least one normal training sequence), V.32). Continue answer tone when receiving AA
MODC_NOQA	2	7	0* 1	Enable V.32bis handshake on quality Disable handshake on quality

AN816-02 TBL

* Default value.

III.1 - Modem Set-up

We suggest the following flow chart (Figure 1) to illustrate the set up phase before making a handshake initialization. This flow chart explains the algorithm of the dp_set_modulation_type function() introduced on chapter II. This function uses two arguments (Mode_type, fallback) and set a flag (b_flag_half_duplex) :

- Mode_type : contains the wanted mode when not in automode.
- Fallback : 1 for automode, 0 for fixed mode.
- b_flag_half_duplex : 1 when half_duplex mode will be used, 0 for full_duplex mode.

Remark : At the end of the set up phase the dp_set_modulation_type() function only did the initialization of ***CONF***'s parameters and ***MODC***'s parameter without sending the command and the parameters to the data pump.

III.2 - FAX Set-up

In FAX mode the automode does not exist since we only use the V.21 ch2 in phase B, D and E of the T.30 protocol, and in phase C of the T.30 protocol the application will used the high speed modulation negociated in B phase (V.17, V.29 or V.27).

The possible configurations are :

V.21 ch2	CONF 0x0F 0x0D 0x00 0x00
V.17 14400	CONF 0x0F 0x09 0x00 0x04
V.17 12000	CONF 0x0F 0x09 0x00 0x02
V.17 9600	CONF 0x0F 0x09 0x00 0x01
V.17 7200	CONF 0x0F 0x09 0x80 0x00
V.29 9600	CONF 0x0F 0x08 0x00 0x01
V.29 7200	CONF 0x0F 0x08 0x80 0x00
V.29 4800	CONF 0x0F 0x08 0x40 0x00
V.27 4800	CONF 0x0F 0x07 0x40 0x00
V.27 2400	CONF 0x0F 0x07 0x20 0x00

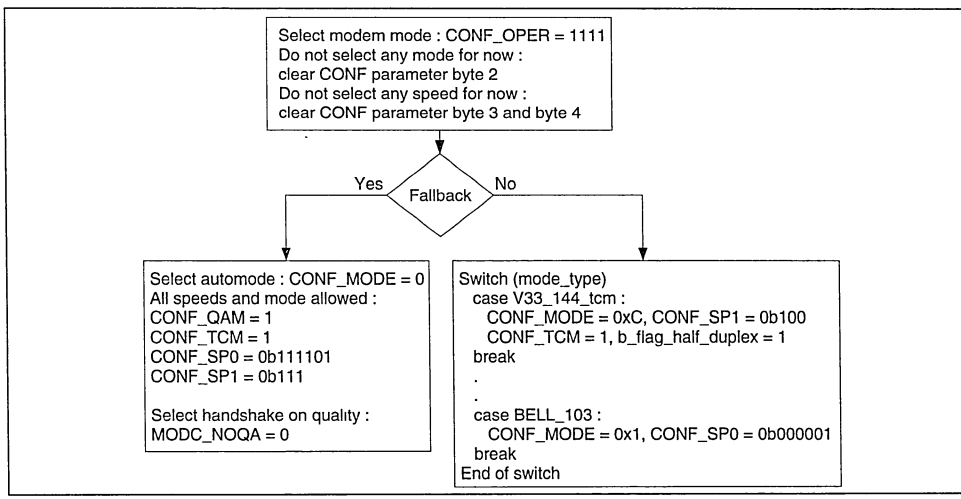
IV - SECOND STEP : HANDSHAKE

IV.1 - Modem Mode

First we must proceed to the initialization of the handshake to :

- send the ***CONF*** command with its parameters,
- send the ***MODC*** command with its parameters (optional),
- send the bulk command with its parameters in case of automode or V.32bis, V.32,
- enable ***IT1*** which is the bulk interrupt using the itmask register of the data pump,

Figure 1



- send the **DSIT** command with its parameters to select the status change which will generate **IT4** (status interrupt, optional),
- start the handshake using **HSK** or **SYNC** command (except for FSK full duplex),
- set some flag and variable for the software allowing the handshake monitoring (state variable of the state machine for handshake monitoring, ...).

We will make reference to the software function implemented in the SATURN application.

The following flow chart (Figure 2) illustres the algorithm of the dp_init_handshake() function introduced in chapter II. Dp_init_handshake() uses b_flag_half_duplex set by dp_set_mudulation_type().

The flag and variable set by dp_init_handshake() are :

- b_flag_hsh_started which will be used by dp_monitor_handshake(),
- automod_handshake_phase which will be used by dp_analizer() when monitoring repeatedly the status given by the data pump.

The next step is to make a monitoring of the handshake. This step is quite complicated since the handshake could be in automode (answer or originate) or in fixed mode. The monitoring is doing by the dp_monitor_handshake() function which must be called repeatedly by the main loop. Dp_monitor_hanshake() will return a result. Dp_monitor_handshake() uses direct status given by the data pump and the value of the state variable of a state machine implemanted in the dp_analizer() function to. This state machine using status given by the data pump.

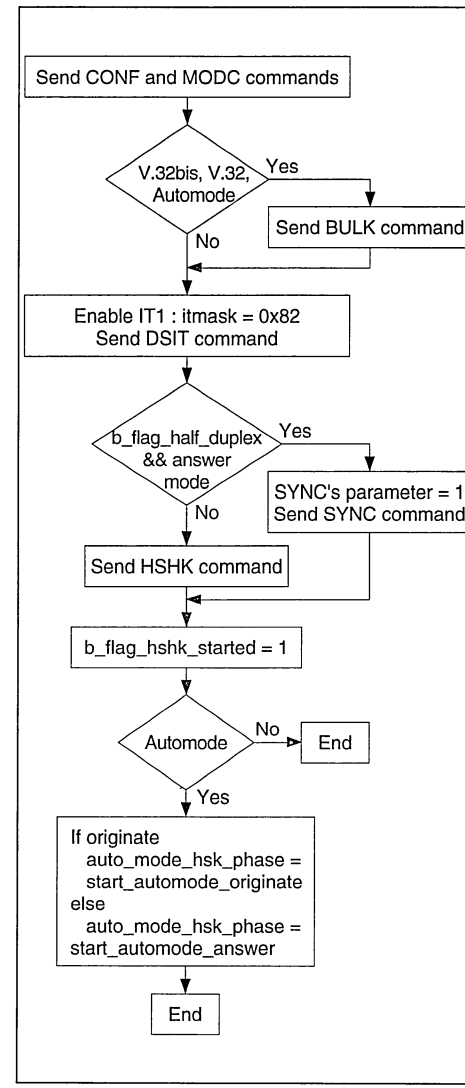
The possible values for automode_hsk_phase variable are :

- HANDSHAKE_FINISHED
- HANDSHAKE_FAILED

The data pump status used are bit0 and bit1of the ***STATUS[1]*** byte . The 2 bits are grouped to make the b_sta_h variable which can have the values 0, 1 or 2.

Dp_monitor_handshake() will use the b_flag_hsk_started flag set by dp_init_handshake().

Figure 2



We propose the flow chart (Figure 3) of dp_monitor_handshake's algorithm as an example.

The monitoring of the handshake uses a state machine architecture placed in the dp_analyzer() function. The user could choose another architecture. To help the engineer to choose the architecture which will be the best in its software application we provide one flow chart for the automode algorithm in originate mode and one flow chart for the automode algorithm in answer mode.

A handshake progression counter contains information about the progress of the handshake in V.32bis, V.32 and V.22bis modes. This 8 bit value is available in ***STAOP2*** (optional status byte 2 of the Dual Port RAM). It can be read to examine the progression of the handshake and it contains normal and error values as show on the following tables :

Table 3 : V.22bis Originate Mode

EVENT	SHSK Normal Value
HSK	0x60
USCR1 DET	0x61
SCR1 DET	0x62
S1 DET	0x63
DATA MODE	0x70

Table 4 : V.22bis Answer Mode

EVENT	SHSK Normal Value
HSK	0x80
SCR1 DET	0x82
S1 DET	0x83
DATA MODE	0x90

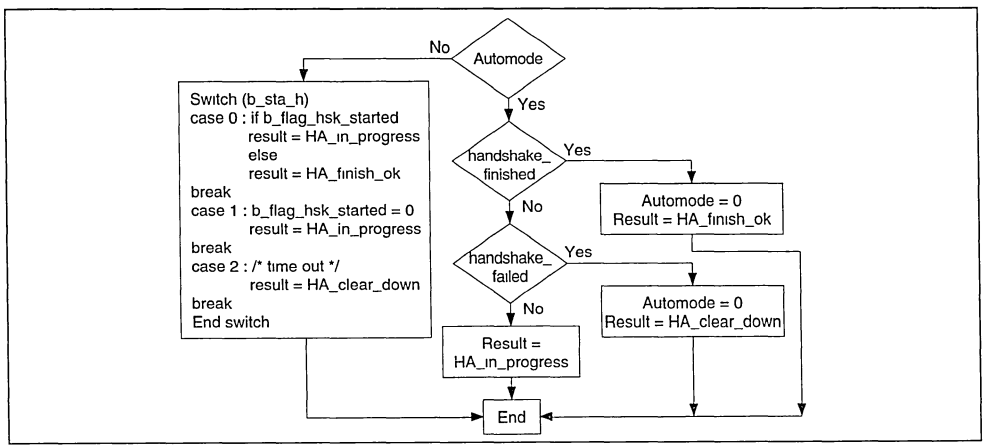
Table 5 : V.32bis Originate Mode

EVENT	SHSK Normal Value	SHSK Error Value
AC DET	0x20	
AC/CA DET	0x21	0x1
CA/AC DET	0x22	0x2
NO AC DET	0x23	0xB for RTRN, 0xC for RRN
S DET	0x24	0x4
SB DET	0x25	0x5
R1 DET	0x26	0x6
S DET	0x27	0x7
SB DET	0x28	0x8
R3 DET	0x29	0x9, 0xD no R5 det after RRN
E DET	0x2A	0xA
DATA MODE	0x30	

Table 6 : V.32bis Answer Mode

EVENT	SHSK Normal Value	SHSK Error Value
AA DET	0x40	0x8 for RTRN, 0x9 for RRN
AA/CC DET	0x41	0x1
NO CC DET	0x42	0x2
S DET	0x43	0x3
S DET2	0x44	0x4
SB DET	0x45	0x5
R2 DET	0x46	0x6, 0xA no R DET after RRN
E DET	0x47	0x7
DATA MODE	0x50	

Figure 3



The above informations are preceded by the following information (always given in ***STAOP2***) in automode mode.

Table 7 : Automode Originate Mode

EVENT	SHSK Value
Wait answer tone	0x01
Wait end of answer tone	0x02
No automode and waiting USC1	0x03
Automode waiting AC or USC1	0x04

Table 8 : Automode Answer Mode

EVENT	SHSK Value
Waiting HSK command	0x10
Generating answer tone	0x11
Generating silence	0x12

The ***_curmod*** variable gives the final negociated mode for Automode applications (especially useful for FSK) or data mode configuration. This variable is inside the ST75C502. We suggest to use the ***STAOP1*** (optional status 1 in the Dual Port Ram interface) during the handshake progression to monitor ***_curmod*** to avoid to use the ***MR*** (Memory Read) command. It will be easier for the modem driver to only read the ***STAOP1*** byte instead to send a ***MR*** command and then to read the answer.

The Table 9 gives the description of _curmod is.

Figure 4 : Automode Originate

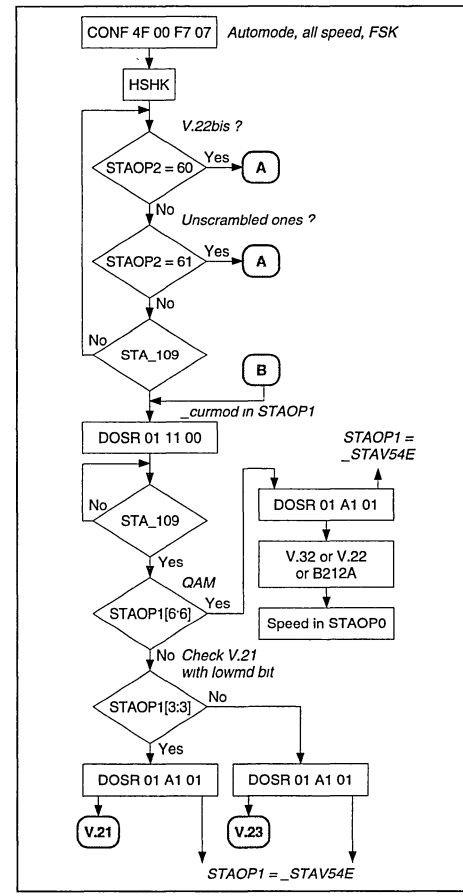


Table 9

Bit	Value	Description
D7 (ITU_T)	1 0	ITUT FSK modes Bell FSK modes
D6 (QAMMD)	1 0	QAM V.32bis, V.32, V.22bis, V.22, B212A, V.17, V.33, V.29, V.27 V.21, V.23, B103 FSK modes
D5 (TCDMMD)	1 0	Treillis mode (V.17, V.33, V.32(bis)) Non treillis mode
D4 (FDUMD)	1 0	Full duplex mode such as V.32(bis), V.22(bis), B212A, V.21, V.23, B103 Half duplex modes (fax) V.21 ch2, V.17, V.29, V.27, V.33
D3 (LOWMD)	1 0	V.27 or V.32 or V.22 or V.21 or B103 V.29 or V.32bis or V.22bis or V.23
D2 (ECCMD)	1 0	Echo canceller mode V.32bis, V.32 No echo canceller mode (others)
D1		Not used
D0 (ANSMD)	1 0	Answer mode Originate mode

AN816-03.TBL

Figure 5 : Automode Originate

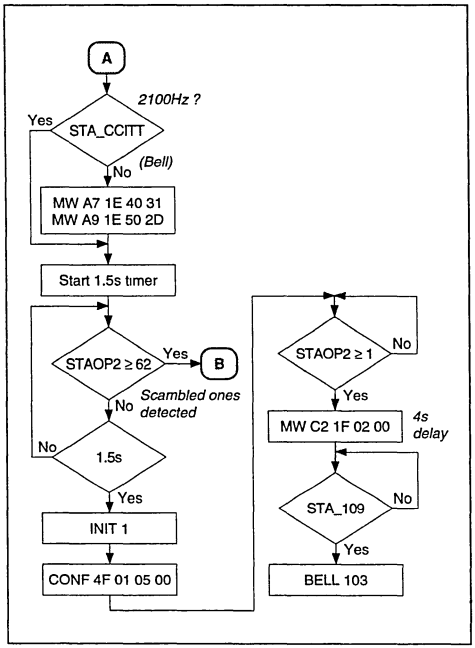


Figure 6 : Automode Answer

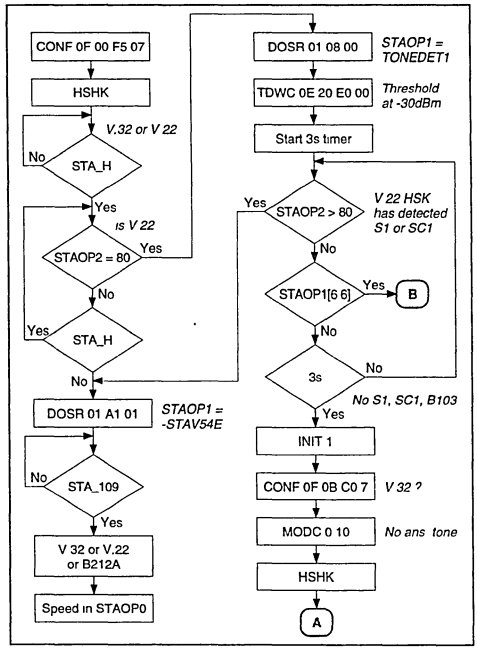


Figure 7 : Automode Answer

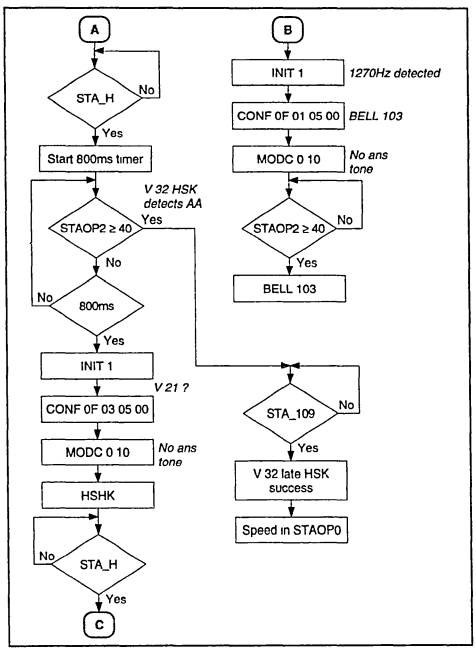


Figure 8 : Automode Answer

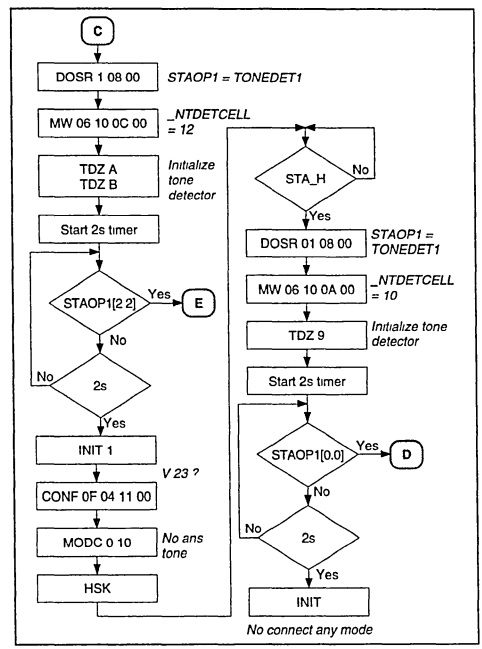
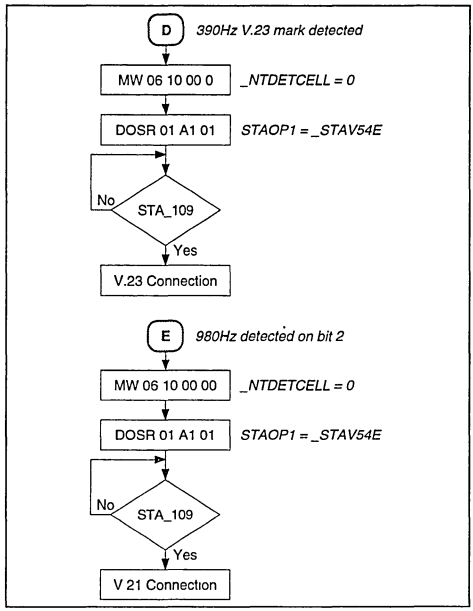


Figure 9 : Automode Answer



At the end of the handshake the MCU software place the modem board in data mode and normaly send a connect result to the terminal. Using the above information and the bit 4..1 of the ***STAOP0*** byte (optional status 0 in the Dual Port RAM) the MCU software will have all the information to send the good information to the terminal. The ***STAOP0*** information is only available for QAM or TCM modulation and provides the speed which is negotiated.

Table 10 : STAOP0 bit 4..1

Value of bit 4..1	Description
0	Reserved
1	Reserved
2	Negociated speed is 1200bps
3	Negociated speed is 2400bps
4	Negociated speed is 4800bps
5	Negociated speed is 7200bps
6	Negociated speed is 9600bps
7	Negociated speed is 12000bps
8	Negociated speed is 14400bps

IV.2 - Fax Mode

To send a carrier the only thing to do is to send the ***HSHK*** command. The user must set to the good value the ***MODC***'s parameter in case of V.17 to select the long train sequence in phase B and the short train sequence in C phase of the T.30 protocol.

The following table summarizes the parameters for the ***MODC*** command in all the case for the V.17, V.29 and V.27 modulations when the equipment is the sending unit :

Training	MODC's Parameters
Long train sequence with echo protection Long train sequence without echo protection	0x00 0x08 0x00 0x00
Short train sequence with echo protection Short train sequence without echo protection	0x40 0x08 0x40 0x00

To received a carrier the only thing to do is to send the ***SYNC 1*** command. The user must set to the good value ***MODC***'s parameters in case of V.17 to select the long train sequence in phase B and the short train sequence in C phase.

The following table summarizes the parameters for the ***MODC*** command in all the case for the V.17, V.29 and V.27 modulations when the equipment is the receiving unit :

Training	MODC's Parameters
Long train sequence	0x00 0x00
Short train sequence	0x40 0x00

V - THIRD STEP : COMMUNICATION MONITORING

V.1 - Modem Mode

While in data mode the MCU must monitoring the status given by the ST75C502 which indicate that a valid carrier is detected and that valid data are received. In all the mode execpt V.32 and V.32bis mode the status is given by the ***STA_109*** bit of the ***STATUS[0]*** byte in the Dual Port RAM interface (see above).

For the V.32 and V.32bis modulation two variables (***PWREST*** and ***RDQUA***) must be checked by the MCU.

PWREST : ***PWREST*** is the residual echo power estimate calculated by the DSP. This number is actually a correlation between the residual echo and the echo estimate. In the case of a normal connection with or without noise at any speed, the absolute value of ***PWREST*** should be near 0. If there is a local disconnect (local cable disconnect), this number's absolute value (***PWREST*** could be negative or positive) should be greater than 0x20. The address of ***PWREST*** is 1B AD.

RDQUA : We suggest detection of remote modem hang_up by monitoring the variable ***RDQUA***, equalizer error energy. ***RDQUA*** also gives an idea of signal to noise ration by the receiver. The address of ***RDQUA*** is 12 A7.

RDQUA has the following typical values in hexadecimal :

Value	RX SNR
0x0080	30dB
0x0100	27dB
0x0200	24dB
0x0400	21dB
0x0800	18dB
0x1000	15dB
0x2000	12dB
> 0x4000	Remote modem hangup

RDQUA may not be greater than 0x4000 for local cable disconnect as the local receiver may try to lock on to the large local transmit echo caused by impedance mismatching when the connection is brocken. Due to this, the quality may be quite good.

In conclusion, if both local cable disconnect and remote hang_ups are to be detected, both ***RDQUA*** and ***PWREST*** should be monitored by the MCU.

How to supervise the *RDQUA* and the *PWREST* value ?

As in data mode the ***STAOP0*** and ***STAOP2*** bytes in the dual port RAM are not used we suggest to used the ***DOSR*** command to request to the ST75C502 to put the LSB of ***PWREST*** in ***STAOP0*** and the MSB of ***RDQUA*** in ***STAOP2***. It will be easier for the MCU to read ***STAOP0*** and ***STAOP2*** instead to send twice the ***MR*** (Memory Read) command and to read each time the value given by the DSP in the ***COMREP0*** and ***COMREP1*** of the Dual Port RAM interface.

The following flow chart (Figure 10) explain how to use the ***DOSR*** command.

The monitoring of the carrier detection (hang_up detection) is made by the Dp_carrier_detect() function in SATURN.

Dp_carrier_detect() is called by the main loop and return True if the carrier is detected and false if the carrier is not detected.

In case of no echo_cancellation mode the Dp_carrier_detect() function return the value of ths ***STA_109*** bit of the ***STATUS[0]*** byte in the Dual Port RAM interface.

In case of echo_cancellation mode (V.32 and V.32bis mode) Dp_carrier_detect() reads ***STAOT0*** and ***STAOPT2*** than counts the number of time the ***STAOPT0***'s value or ***STAOPT2***'s value is higher than a threshold. If ***STAOPT0***'s value or ***STAOPT2***'s value is five times higher than a threshold Dp_carrier_detect() return false. The ***PWREST***'s threshold PWREST_MAX is equal to 0x2A, and the ***RDQUA***'s threshold RDQUA_MAX is equal to 0x40.

Figure 10

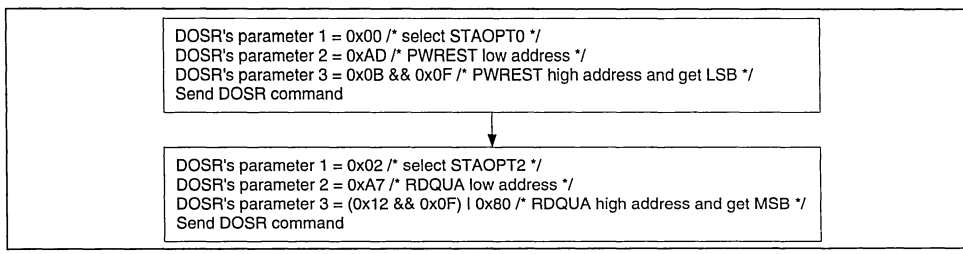
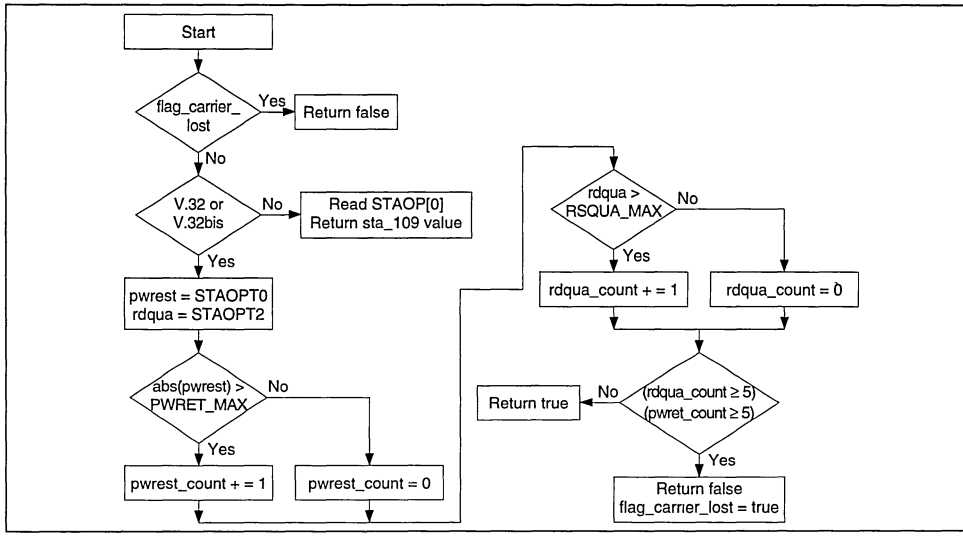


Figure 11



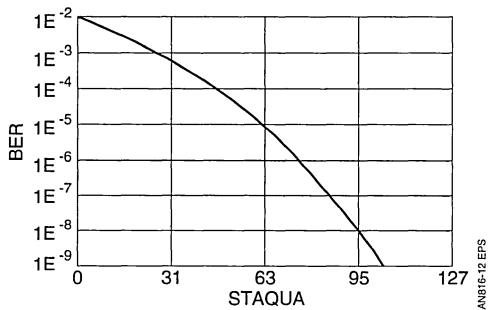
We suggest the flow chart of these function as example (Figure 11).

Note : flag_carrier_lost is set to fasle at the beginning of the data mode (just at the end of the handshake).

The application software could also monitor the Quality Status provide by the ST75C502.

The quality byte ***STAQUA*** (address 0x0B in the Dual Port RAM interface) monitors an evaluation of the line quality. It is updated once per baud and its value ranges is from 127 (perfect quality) to 0 (terrible quality). The value is automatically adjusted according to the current receiving mode (not valid in FSK modes). Refer to the Figure 12 to convert the value into its bit error rate equivalence.

Figure 12



V.2 - Fax Mode

In fax mode the monitoring is simpler. The carrier detect information is provide for all the modes by the ***STA_109*** bit in ***STAOP0*** byte.

The software could monitor the quality reading the ***STAQUA*** byte as in modem mode.

VI - SPECIAL FUNCTIONS FOR FAX COMMUNICATIONS

A fax application needs some function as V.21 ch2 flag detection, stop to send or to receive carrier, ... In SATURN the following software function group these needs : **Dp_set_idle(), Dp_set_v21_fax(), Dp_detect_v21_fax(), dp_detect_v21_in_high_speed_fax()**. We are going to describe in this chapter the algoritms of all these function. Refer to the definition of these functions given in chapter II.

VI.1 - Stop Transmit or Receive

The ***STOP*** command must be used to stop the carrier transmission, and the ***SYNC*** command with its parameter equal to 0 must be used to stop carrier reception. This is done by dp_set_idle() function.

Stop transmit : send STOP.

Stop reception : send SYNC 0.

VI.2 - Flag Detection when the Data Pump is Set-up for High Speed Reception

The application must be able to detect V.21 ch2 flag when the data pump is set up to received in high speed mode (V.27, V.29, V.17). As no particular function is available in the ST75C502 for that purpose the user has to use 2 tone detectors : tone detector cell number 0 and 1 are the only available tone cells in that case. The status given by these tone detectors will be in ***TONEDT0*** byte on bit 0 and 1. In data fax mode the ***STAOP1*** byte is available. That's why we suggest to the user to monitor ***TONEDT0*** byte via ***STAOP1*** byte using ***DOSR*** command.

The final sequence for the application will be :

- Send the ***CONF*** command to select V.17, V.29 or V.27,
- Send ***SYNC 1*** command,
- Set up the cells 0 and 1 of the tone detector,
- Use ***DOSR*** command for monitoring the ***TONEDT0*** status.

Each time the application will need to know if the far end FAX equipment send a V.21 ch2 flag sequence (preamble), the MCU will have to read the ***STAOP1*** byte and test if bit 0 and 1 are equal to 1. This is done in SATURN application by the dp_detect_v21_in_high_speed_fax() function.

Here after we provide the information to set up the tone detector cell 0 and 1.

The user has first to set up this tone detector as shows below :

/* select the reference level at - 40dBm */
TDWC's parameter 1 = 0x00 ; /* tone detector cell number */
TDWC's parameter 2 = 0x20 ; /* select static level */
TDWC's parameter 3 = 0x70 ; /* Low byte of the coefficient */
TDWC's parameter 4 = 0x00 ; /* High byte of the coefficient */
send ***TDWC*** command

/* Load the coefficients of the two biquad to detect 1650Hz using the ***TDWC*** command */

Each tone cell needs 12 coefficients given in the following table the cells 0 and 1. The coefficients are 16 bits size. The table contains 24 bytes for each cell. The table starts with the MSB of the first coefficient, then the LSB of the first coefficient, then the MSB of the second coefficient, then the LSB of the second coefficient, ...

MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
0x01	0xC1	0x0F	0x35	0xC1	0xC3	0x00	0x00	0xC0	0x00	0x7F	0xFF
0x02	0xAB	0x11	0xC0	0xC1	0xC2	0x00	0x00	0xC0	0x00	0x7F	0xFF
0x01	0xE7	0x0D	0x83	0xC0	0xBD	0x00	0x00	0xC0	0x00	0x7F	0xFF
0x05	0x4F	0x13	0xB2	0xC0	0xBC	0x00	0x00	0xC0	0x00	0x7F	0xFF

/* Programme biquad and energy input for cell number 0 */
TDWW's parameter 1 = 0 ; /* cell number 0 */
TDWW's parameter 2 = 0 ; /* biquad energy input */
TDWW's parameter 3 = 0x11 ; /* energy estimator input */
TDWW's parameter 4 = 0x02 ; /* biquad filter signal input */
send ***TDWW*** command

/* Programme biquad and energy input for cell number 1 */
TDWW's parameter 1 = 1 ; /* cell number 1 */
TDWW's parameter 2 = 0 ; /* biquad energy input */
TDWW's parameter 3 = 0x01 ; /* energy estimator input */
TDWW's parameter 4 = 0x10 ; /* biquad filter signal input */
send ***TDWW*** command

/* Programme comparator inputs cell number 0 */
TDWW's parameter 1 = 0 ; /* cell number 0 */
TDWW's parameter 2 = 1 ; /* comparator input */
TDWW's parameter 3 = 0x30 ; /* negative comparator signal input */
TDWW's parameter 4 = 0x20 ; /* positive comparator signal input */
send ***TDWW*** command

/* Programme comparator inputs cell number 1 */
TDWW's parameter 1 = 1 ; /* cell number 1 */
TDWW's parameter 2 = 1 ; /* comparator input */
TDWW's parameter 3 = 0x21 ; /* negative comparator signal input */
TDWW's parameter 4 = 0x20 ; /* positive comparator signal input */
send ***TDWW*** command

/* clear the tone detector cell 0 */
TDZ's parameter = 0 ; /* cell number 0 */
send ***TDZ*** command

/* clear the tone detector cell 1 */
TDZ's parameter = 1 ; /* cell number 1 */
send ***TDZ*** command

Here after we provide the parameters for the ***DOSR*** command to monitor ***TONEDT0*** in ***STAOP1*** byte :
DOSR's parameter 1 = 0x01 ;
DOSR's parameter 2 = 0x07 ;
DOSR's parameter 3 = 0x00 ;
DOSR's parameter 4 = 0x00 ;
send ***DOSR*** command

Figure 13

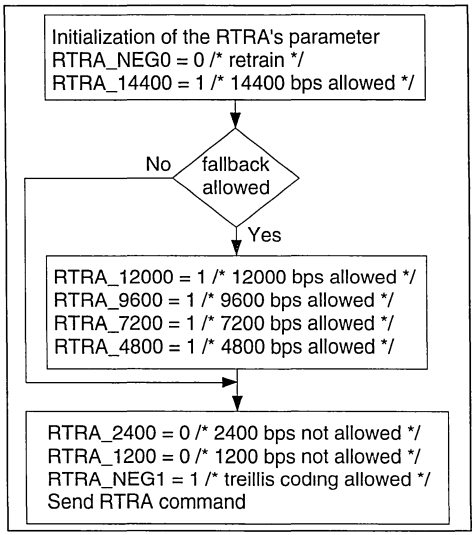
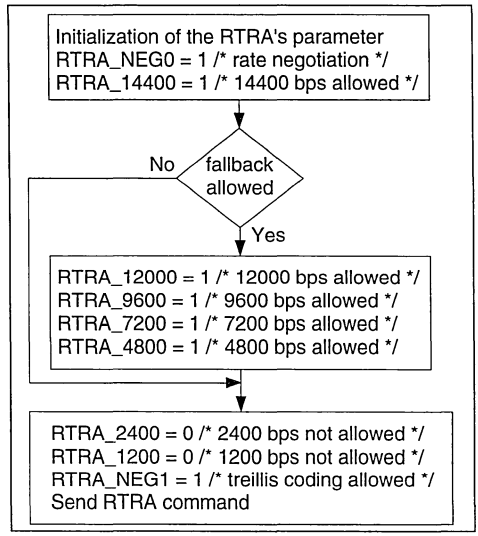


Figure 14



VI.3 - Flag Detection when the Application is Calling a Far End Fax Equipment

The equipment which is the calling unit must be able to detect V.21 ch2 modulation while sending the CNG tone (ITU_T 1100Hz tone). In this case the ST75C502 will be set up in tone mode and will provide on bit 2 of the ***STAOP1*** byte (in the Dual Port RAM interface) a status which indicates if a frequency of 1650Hz greater than -45dBm id detected.

The MCU has only to read the ***STAOP1*** byte and to test the bit 2 value. In SATURN application this done by the dp_detect_v21_fax() function.

VII - RETRAIN AND RATE RENEGOTIATION

The ST75C502 allows the application to initialize and to detect retrain or rate renegotion.

The Figure 13 explain how to initialize a retrain in V.32bis. The principle is the same in V.32 and V.22bis.

The Figure 14 explain how to initialize a rate renegotiation in V.32bis 14400. The principle is the same in V.32 and V.22bis.

After the retrain or rate renegotiation initialization, the monitoring must be done by testing the bits ***STA_H*** and ***STA_TIM*** of the ***STATUS[1]*** byte.

STA_H = Transmit synchronisation in progress. Valid only in modem mode.

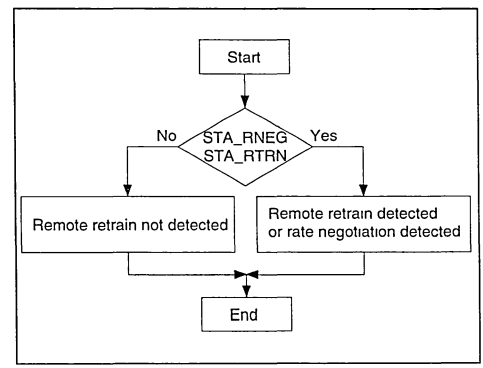
STA_TIM = Handshake timeout. Valid only in data modem mode.

STA_TIM, STA_H 0 Synchronisation Completed
1 Synchronisation in Progress
2 Synchronisation Time Out

The speed negociated is given in bit 4..1 of ***STAOP0*** (see chapter IV.1 of this application for information).

The detection of a remote retrain or rate renegotiation is done by testing ***STA_RTRN*** and ***STA_RNEG*** bits in ***STATUS[1]*** byte. The following flow chart (Figure 15) give the algorithm of the dp_detect_retrain() function in SATURN application.

Figure 15



ST75C5XX : LOW POWER MODE

By Laurent CLARAMOND

I - INTRODUCTION

This application explains how to use the Low Power Mode when using the ST75C5XX component in modem and or fax applications. All the user know that the power consumption must be reduced while in normal mode (transmit and/or receive) but also when the system equipment is not used. That is why SGS-THOMSON studies its telecommunication components to be used in such a situation.

II - MAIN MANAGEMENT

The main software loop could be as Figure 1.

While the Microprocessor (CPU) detects an activity (connection with a far end equipment, Ring, user request for dialing, ...) the application remains in Normal Mode. In case where there is no activity the CPU set up the ST75C5XX to go in Low Power Mode. If the CPU is able to also have such a function, the software will set up the CPU to go in Low Power Mode to.

But how to awake the system equipment ?

We suggest to select the different events : a user resquest, a RING signal or a data sent by the terminal which could be connected to the telecommunication equipment (using a serial link for example). In all the cases the awake signals must active an interrupt in the CPU. After that the CPU will initialize the application and set up the ST75C5XX using the ***RESET*** signal (master reset of the component).

The Figure 2 is a block diagram of such an application.

III - HOW TO SET-UP IN LOW POWER MODE THE ST75C5XX

It is easy to set up the ST75C5XX in Low Power Mode. The only thing to do is to send the ***SLEEP*** command to the DSP via the Dual port RAM. To do that the CPU writes the hexadecimal value 0x03 (***SLEEP*** command) in the ***COMSYS*** byte in the Dual Port RAM at address 0. Be carrefull the ***SLEEP*** command will not be acknowledge by the ST75C5XX.

Figure 1

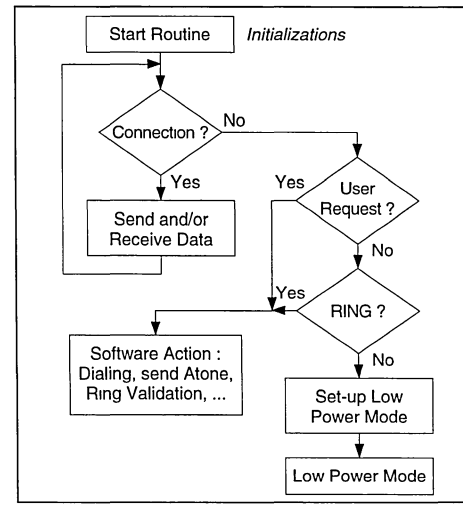
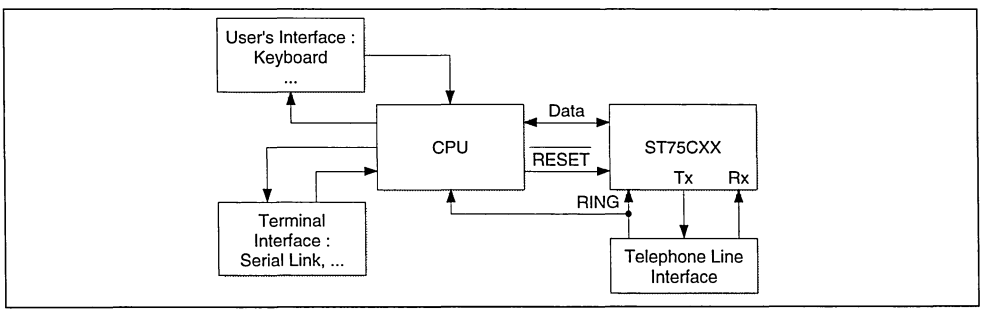


Figure 2



When the DSP recognizes the ***SLEEP*** command it will stop the clock (***CLKOUT*** will not be provided from the ST75C5XX) and goes in Low Power Mode. It will take less than 1ms to enter the low Power Mode.

In Low Power Mode the Dual Port RAM can not be read. Take care that the ST75C5XX will provide the ***SDTACK*** signal even if the read is not effective. The CPU must not try to write in the Dual Port RAM.

Note : The ST75C52 does not provide any $\overline{SDTACK}$ signal while in Low Power Mode in others words ***SDTACK*** will remain high.

IV - HOW TO AWAKE THE ST75C5XX ?

Activating the $\overline{RESET}$ signal will awake the ST75C5XX. When waking up the ST75C5XX processes exactly as after a hardware reset as described below :

- $\overline{RESET}$ signal low at least a time ***T1*** (which is equal to 700ns when using an external oscillator, or which is equal to 4ms when using an external third harmonic crystal) to have a ***CLKOUT*** signal stable and valid. ***CLKOUT*** is the internal clock and is equal to the external clock divided by two.
- $\overline{RESET}$ signal high.
- The ST75C5XX clears all its internal memories, clears the whole Dual Port RAM and starts to initialize the delta sigma analog converters. As soon as the initializations are completed, the ST75C5XX clears the Dual Port RAM address 0, generates an ***IT6*** interrupt (command acknowledge) and is programmed to send and receive tones, the bit clock are programmed to 9600Hz. The total duration of the reset sequence (reset time ***T2***) is equal to 5ms for the ST75C52 and the ST75C520 and equals to 500ms for the ST75C502. Be carrefull that any command in this reset time ***T2*** will be lost.
- The ***IT6*** interrupt must be cleared using the ***ITREST[6]*** register : The CPU writes 00 at address 0x46 in the Dual Port RAM interface.
- After that time the ST75C5XX is ready to execute commands sent by the CPU.

Note : As the DSP clears all the Dual Port RAM, the interrupts which could be sent by the ST75C5XX are masked. That is why the CPU must set up the ***ITMASK*** register in the Dual Port RAM interface (at address 0x4F) to 0xC0 to be able to receive the ***IT6*** interrupt on the ***SINTR*** signal. The set up of the ***ITMASK*** register must be done when ***RESET*** pin is high after the reset time ***T2***.

The Figures 3 and 4 show the relation between the ***RESET*** and the ***CLKOUT*** signals in both cases : external oscillator and external third harmonic crystal.

Figure 3 : ST75C5XX Use an External Oscillator

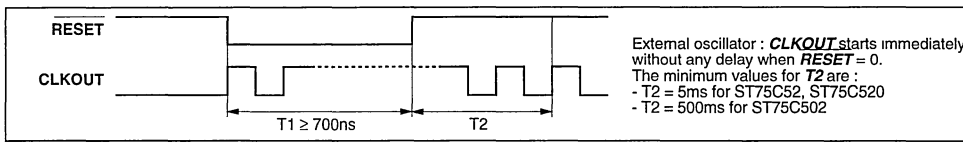
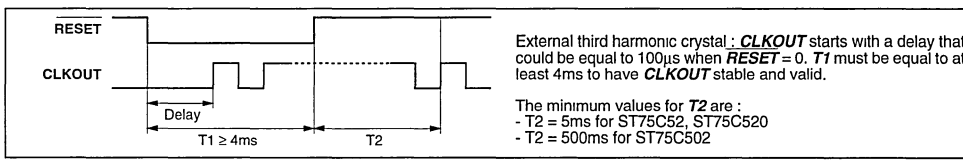


Figure 4 : ST75C5XX Uses a Third Harmonic Crystal



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

COMPUTATION OF TONE DETECTOR COEFFICIENTS USING TD SOFTWARE FOR ST75C502

I - Tone Detector Description

Refer to the ST75C502 Data Sheet for detailed description of the tone detectors, Figure 2 (ST75C502 Data Sheet) for the biquadratic IIR filter, Figure 3 for the power estimator, Figure 4 for the tone detector wiring address (first half) and Figure 5 for the tone detector wiring address (second half).

There are 16 programmable tone detector cells available. Each cell contains a 4th order IIR (biquadratic) filter, energy estimator consisting of an absolute value measurement and a 1st order low pass filter, 2 input comparator, and a static level.

Detect information is sent to status word ***TONEDET***. The user has the possibility of sending commands to the data pump to program the tone detectors for almost any desired transfer function. For each cell, the command ***TDWC*** can be used to program the 12 coefficients of the 4th order IIR filter (C0 to CB), the 1st order low pass filter coefficient, and the static level. The command ***TDWW*** can be used to program the wiring between cells for cascading and signal routing. One is free to program the IIR input, energy estimator input, and comparator + and - inputs.

II - Program TD Description

The user has the possibility of calculating his proper coefficients and determining the corresponding ***TDWC*** and ***TDWW*** commands manually but, the program TD was written to facilitate this task.

The purpose of this chapter is to give the operating instructions for using program TD for quick development of the code needed to program the detectors.

III - Compatability and Input/output

Program TD is written in FORTRAN and is executable on almost any PC with hard disk using MS-DOS.

Input is from the keyboard and output is on the screen.

Also, several useful files are generated by the program :

a) TD.SPC - contains trace of filter specifications given by user
b) TD.RES - shows floating-point frequency response of specified filter
c) TD.CCI - CCI commands needed for the data pump for specified filter

IV - Starting the Program

To start the program, the user should first create a directory and load program TD.EXE into the directory. The command TD is now sent while in the created directory to start program execution. The program will then display ENTER TYPE. The following paragraph will describe the filter types.

V - Choosing a Filter Type

Four possible filter types are available to the user with the following characteristics :

- BUTTERWORTH : This type of filter has a maximally flat pass-band with no ripple. It has multiple zeroes at half the sampling frequency (3600Hz) or D.C. or at the center of the band for band-stop configurations.
- CHEBYCHEV : Equiripple in the pass band and flat response in the stop band which is particularly useful for band rejection filtering.
- INVERSE CHEBYCHEV : Ripple-free pass band and more efficient than the Butterworth. For the same target design template, a lower order filter is necessary. Equiripple stop-band characteristics render this type useful for band-pass, low-pass or high-pass filtering.
- ELLIPTIC : This type of filter is the most efficient and can have narrow transition bands. However, it is characterized by ripple in the pass and stop bands. Once the type is chosen, the program will ask for LOPASS, HIPASS, BANDPASS, or BAND REJECT filters.

VI - Choosing a Filter Order

For all but Elliptic types, the program TD will ask the desired order. The user must specify the number of cascaded biquads (2nd order sections) desired.

VII - Defining and Optimizing a Target Template

The corner frequencies for pass band and/or stop band are required by the program, and attenuation in the pass band and/or stop band for all types except Butterworth. These attenuations are in dB referenced from the input to the output. The program now calculates the transfer function in the Z domain displaying locations of poles and zeroes, and the required number of 4th order tone detector cells needed. This information is displayed on the screen and output to file TD.SPC. For the case of an Elliptic type, the order required is calculated from the transition band specified by the user, rather than specified directly by the user as for the other types. The order may be too high for the number of cells available or desired. The user may re-specify the filter. In general, one or more of the following steps may be performed, if the application enables it, to decrease the required order of an Elliptic type filter :

- change from band pass or band reject to low pass or high pass,
- increase difference between pass band and stop band frequencies,
- increase the pass band ripple and/or decrease the stop band atten.

Using an iterative process, one can optimize the target specification of the filter before continuing to the next step.

VIII - Displaying the Ideal Frequency Response

The program TD will now calculate the frequency response of the specified filter and normalize coefficients to avoid overflow in the DSP ALU. The program now proceeds with the display of the frequency response on the screen. The user is asked by the program TD to specify start, stop, and step frequencies to facilitate interest in a particular portion of the frequency response. Once displayed, the program asks if the response is to be re-displayed allowing the user to change the frequency ranges. The desired frequency response is calculated in floating-point while the actual program implemented in the data pump uses a fixed-point DSP. In most cases, there should not be too much difference between the two calculation methods if the transition bands are not too narrow in the case of Elliptic types or the order is not too high for all types. At this point, the user has a better idea of the transition bands for Butterworth and Chebychev designs and also the unity gain loss. The normalization process may, in some cases to avoid overflow, result in an attenuation in the pass band or unity gain loss. Increasing the order of the Butterworth or Chebychev filters may be necessary for a narrower transition band. Widening of the transition band may be necessary for diminuing the unity gain lossof an Elliptic filter. In any case, the frequency response is written to file CP.RES for reference after the end of program execution. This can be especially useful for reference if several optimization attempts are desired.

IX - Choosing the Used Cells

The program TD will now ask for the starting cell number (a number from 0 to F). The program will write CCI instructions for programming n (n = order/4) cells starting from the given address. The program cascades the biquadratic filters. However, only the last comparator and static level are used for the detection decision. This means that, eventually, the comparators or static levels for intermediate cells could be programmed for other functions. If the user, for example chooses 1 for the starting address, and there are 3 cells used, then the detection bit for this configuration will be available in ***TONEDET(0)*** position 3 (refer to ST75C5x Data Sheet). The user should choose a relatively low starting address beginning with the first unused position, if possible. This is because the execution time of the detectors in the non-idle mode may necessitate the utilizaton of less than 16 cells (NTDCELL .lt. 16 refer to ram mapping application note). In this case the higher cell numbers are not executed.

X - Selecting the Detection Thresholds

The detection threshold is now asked for by the program to define the minimum detectable input signal level at a pass band frequency with 0dB unity gain loss. The program will remind the user of the actual unity gain loss due to normalization and, in general, the desired threshold must be lowered by the number of dB in the unity gain loss. However, threshold levels lower than -50dBm are not reliable as the minimum dynamic range of the detectors will be surpassed.

XI - Selecting the Energy Estimator Time Constant

The energy estimator time constant is now asked for by the program and the user will specify the value in milliseconds. A typical value of 8 is used for the default tone detectors but, if the user designs a filter with a particularly large group delay, he should also increase this value to avoid undesirable transients in the detection decision. Please note that group delay calculation is beyond the scope of this program and must be calculated by other techniques from the coefficients in TD.SPC.

XII - Example Listings

The following listings give an example printout of the files TD.SPC, TD.RES, TD.CCI for a Butterworth 8th order low pass filter with cut-off frequency of 1000Hz.

```
EXAMPLE FOR 8th ORDER BUTTERWORTH
LPF FC=1000HZ, TH=-40dBM

          TD.SPC
          ------

 ENTER TYPE: 1 BUTTERW, 2 CHEBY, 3 ICHEBY, 4 ELLIP
    1
 ENTER 1 LOPASS, 2 HIPASS, 3 BPASS, 4 BREJ
    1
 ENTER NUMBER OF CASCADED BIQUADS DESIRED
    4
 ENTER BAND EDGE IN UN-NORMALIZED HZ
  1000.000
 Z PLANE
 #,   ZEROS  (REAL,  IMAG),      POLES (REAL, IMAG)
 1     -1.000000      0.000000      0.367029      0.085334
 2     -1.000000      0.000000      0.392676      0.259992
 3     -1.000000      0.000000      0.450892      0.446792
 4     -1.000000      0.000000      0.559214      0.653640
 5      1.000000      0.000000      1.000000      0.000000

          2 4TH ORDER TONE DETECTOR CELLS NEEDED !

 F(Z) = (Z*Z + B1Z + B2)/(Z*Z + A1Z + A2)
      1    2.000000    1.000000     -0.734059    0.141992
      2    2.000000    1.000000     -0.785351    0.221790
      3    2.000000    1.000000     -0.901784    0.402926
      4    2.000000    1.000000     -1.118428    0.739966

               TD.RES
               ------

Freq(Hz):                                                Gain(dB):
---------                                                ---------
    0.*************************************************    0.0
  100.*************************************************    0.0
  200.*************************************************    0.0
  300.*************************************************    0.0
  400.*************************************************    0.0
  500.*************************************************    0.0
  600.*************************************************    0.0
  700.*************************************************    0.0
  800.************************************************    -0.1
  900.**********************************************      -0.6
 1000.*******************************************         -3.0
 1100.*****************************************           -8.3
 1200.*********************************                   -15.0
 1300.*************************                           -21.7
 1400.*********************                               -28.3
 1500.***************                                     -34.6
 1600.*********                                           -40.8
 1700.***                                                 -46.9
 1800.                                                    -53.0
 1900.                                                    -59.1
 2000.                                                    -65.2
 2100.                                                    -71.4
 2200.                                                    -77.8
 2300.                                                    -84.3
 2400.                                                    -91.2
 2500.                                                    -98.4
 2600.                                                   -100.0
 2700.                                                   -100.0
 2800.                                                   -100.0
 2900.                                                   -100.0
 3000.                                                   -100.0
 3100.                                                   -100.0
```

XII - Example Listings (continued)

TD.CCI

```
; 4TH ORDER BIQUAD CELL 9 COEFS
CCI TDWC 9 0 1B 1A
CCI TDWC 9 1 FA 2E
CCI TDWC 9 2 EA F6
CCI TDWC 9 3 00 40
CCI TDWC 9 4 00 20
CCI TDWC 9 5 00 40
CCI TDWC 9 6 EE 1B
CCI TDWC 9 7 43 32
CCI TDWC 9 8 CF F1
CCI TDWC 9 9 00 40
CCI TDWC 9 A 00 20
CCI TDWC 9 B 00 40
; 4TH ORDER BIQUAD CELL A COEFS
CCI TDWC A 0 12 20
CCI TDWC A 1 B6 39
CCI TDWC A 2 37 E6
CCI TDWC A 3 00 40
CCI TDWC A 4 00 20
CCI TDWC A 5 00 40
CCI TDWC A 6 9E 23
CCI TDWC A 7 94 47
CCI TDWC A 8 A5 D0
CCI TDWC A 9 78 47
CCI TDWC A A BC 23
CCI TDWC A B 78 47
; POWER ESTIMATOR AND BIQUAD INPUTS
CCI TDWW 9 0 19 02
CCI TDWW A 0 1A 19
; COMPARATOR - AND + INPUTS
CCI TDWW A 1 3A 2A
; DETECTION THRESHOLD AT   -40.00 DB
CCI TDWC A 20 70 00
; ENERGY TIME CONSTANT IS     8.00 MS
CCI TDWC A 10 E3 08
; CLEAR INTERNAL VARIABLES OF ALL USED CELLS
CCI TDZ 9
CCI TDZ A
```

FAX MODEM

SGS-THOMSON MICROELECTRONICS

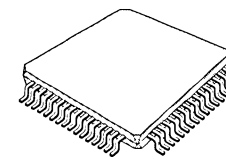
ST75C52

HIGH SPEED FAX MODEM DATA PUMP

- ITU-T V.17, V.29, V.27ter, V.21 WITH FAX SUPPORT
- ITU-T V.23, V.21, BELL 103
- V.17, V.29 (T104), V.27ter SHORT TRAINS
- V.33 HALF-DUPLEX
- 1800Hz OR 1700Hz CARRIER
- SINGLE CHIP COMPLETE DATA PUMP
- SINGLE 5V POWER SUPPLY :
  - TYPICAL ACTIVE POWER CONSUMPTION : 500mW
  - LOW POWER MODE (typ. 5mW)
- EXTENDED MODES OF OPERATIONS :
  - FULL IMPLEMENTATION OF THE V.17, V.33, V.29 AND V.27ter HANDSHAKES
  - AUTODIAL AND AUTOANSWER CAPABILITY
  - PROGRAMMABLE TONE DETECTION AND FSK V.21 FLAG PATTERN DETECTION DURING HIGH SPEED RECEPTION
  - PROGRAMMABLE CALL PROGRESS AND CALL WAITING TONE DETECTORS INCLUDING DTMF
  - PROGRAMMABLE CLASS™ DETECTION CAPABILITY
  - WIDE DYNAMIC RANGE (>48dB)
  - A-LAW VOICE PCM MODE
- VERSATILE INTERFACES :
  - PARALLEL 64 x 8-BIT DUAL PORT RAM
  - SYNCHRONOUS/HDLC PARALLEL DATA HANDLING
  - HDLC FRAMING SUPPORT
  - V.24 INTERFACE
  - FULL OPERATING STATUS REAL TIME MONITORING
  - FULL DIAGNOSTIC CAPABILITY
  - DUAL 8-BIT DAC FOR CONSTELLATION DISPLAY

DESCRIPTION

The SGS-THOMSON Microelectronics ST75C52 chip is a highly integrated modem engine, which can operate with all currently used FAX group III standards up to 14400bps. Full V.21, V.23 and Bell 103 full duplex modem standards are implemented.



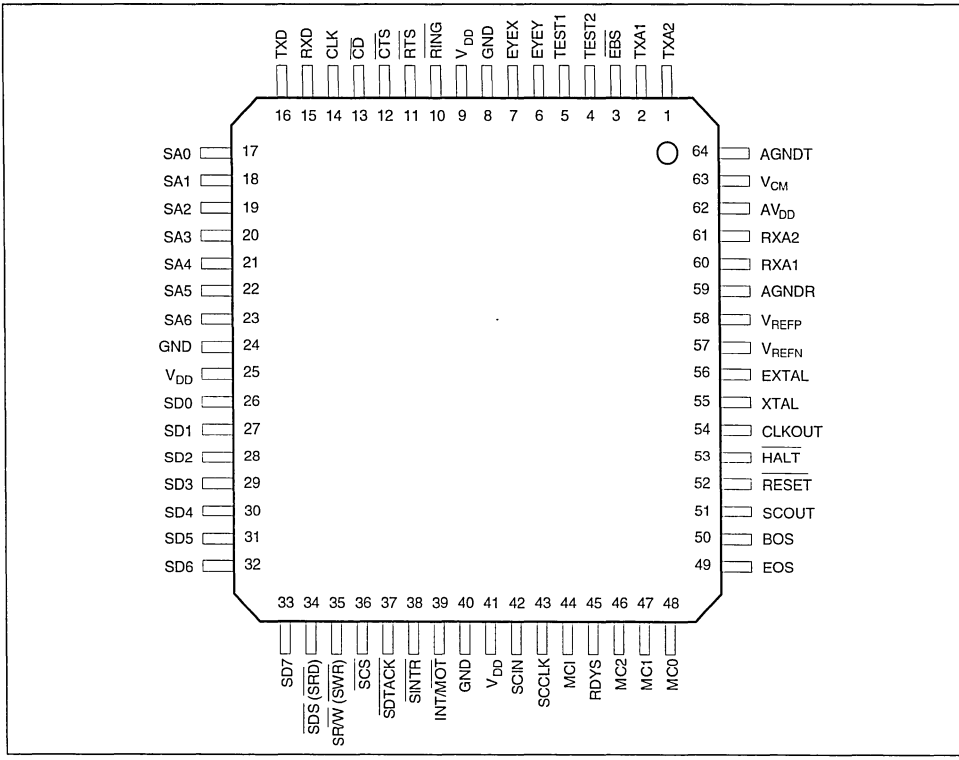
PQFP64
(Plastic Quad Flat Pack)

ORDER CODE : ST75C52 PQFP

SUMMARY

I - PIN DESCRIPTION

I.1 - Pin Connections



I.2 - Host Interface

The exchanges with the control processor proceed through a 64 Bytes DUAL port RAM shared between the ST75C52 and the Host. The signals associated with this interface are :

Pin Name	Type	Description
SD0..SD7	I/O	System Data Bus. 8-bit data bus used for asynchronous exchanges between the ST75C52 and the Host through the dual port RAM. High impedance when exchanges are not active.
SA0..SA6	I	System Address Bus. 7-bit address bus for dual port RAM.
$\overline{SDS}$ ($\overline{SRD}$)	I	System Data Strobe. Active low. Synchronizes all the exchanges. In Motorola mode initiates the exchange, active low. In Intel mode initiates a read exchange, active low.
SR/$\overline{W}$ ($\overline{SWR}$)	I	System Read/Write. In Motorola mode defines the type of exchange read/write. In Intel mode initiates a write exchange, active low.
$\overline{SCS}$	I	System Chip Select. Active low.
$\overline{SDTACK}$	OD	System Bus Data Acknowledge. Active low. Open drain.
$\overline{SINTR}$	OD	System Interrupt Request. Active low. This signal is asserted by the ST75C52 and negated by the host. Open drain.
$\overline{RESET}$	I	Reset. Active low.
$\overline{RING}$	I	Ring Detect Signal : awake ST75C52 from its sleep mode, active low.
INT/$\overline{MOT}$	I	Select Intel/Motorola Interface.

I.3 - Analog Interface

Pin Name	Type	Description
TXA1	O	Transmit Analog Output 1
TXA2	O	Transmit Analog Output 2. Outputs TXA1 and TXA2 provide analog signals with maximum peak to peak amplitude 2 x V_{REF}, and must be followed by an external continous-time two pole smoothing filter (where $V_{REF} = V_{REFP} - V_{REFN}$).
RXA1	I	Receive Analog Input 1
RXA2	I	Receive Analog Input 2. The analog differential input peak to peak signal must be less than 2 x V_{REF}. It must be preceded by an external continous-time single pole anti-aliasing filter. This filter must be as close as possible to the RXA1 and RXA2 Pins (where $V_{REF} = V_{REFP} - V_{REFN}$).
V_{CM}	I/O	Analog Common Voltage (nominal +2.5V). This input must be decoupled with respect to AGND.
V_{REFN}	I	Analog Negative Reference (nominal V_{CM} - 1.25V). This input must be decoupled with respect to V_{CM}.
V_{REFP}	I	Analog Positive Reference (nominal V_{CM}+1.25V). This input must be decoupled with respect to V_{CM}.

I.4 - V.24 Interface

Pin Name	Type	Description
$\overline{RTS}$	I	Request to Send. Active low.
CLK	O	Data Bit Clock. Falling edge coïncides with DATA change.
$\overline{CTS}$	O	Clear to Send. Active low.
RxD	O	Receive Data
TxD	I	Transmit Data sampled with rising edge of CLK
$\overline{CD}$	O	Carrier Detect. Active low.

I.5 - Miscellaneous

Pin Name	Type	Description
XTAL	O	Internal Oscillator Output. Left open if not used.
EXTAL	I	Internal Oscillator Input, or External Clock
EYEX	O	Constellation X analog coordinate
EYEY	O	Constellation Y analog coordinate
TEST1		To be left open
TEST2		To be left open

Note : The nominal external clock frequency of the ST75C52 is 29.4912MHz with a precision better than $\pm 5.10^{-5}$

I.6 - Boundary Scan Interface

A set of 13 signals are dedicated for Testing the ST75C52 Component. These signals can be used in a development phase, associated with the SGS-THOMSON ST18932 Boundary Scan Development Tools, to Debug the application Hardware and Software. If not used all input signals must be grounded and all output signals left open.

Pin Name	Type	Description
SCIN	I	Scan Data Input
SCCLK	I	Scan Clock
SCOUT	O	Scan Data Output
BOS	I	Begin of Scan Control
EOS	I	End of Scan
MC0..MC2	I	Mode Control
$\overline{HALT}$	I	Stop ST75C52 Execution
MCI	O	Multicycle Instruction
RDYS	O	Ready to Scan Flag
$\overline{EBS}$	I	Enable Boundary Scan. Active low (must be set low in normal mode).
CLKOUT	O	Internal ST75C52 Clock (XTAL frequency divided by 2)

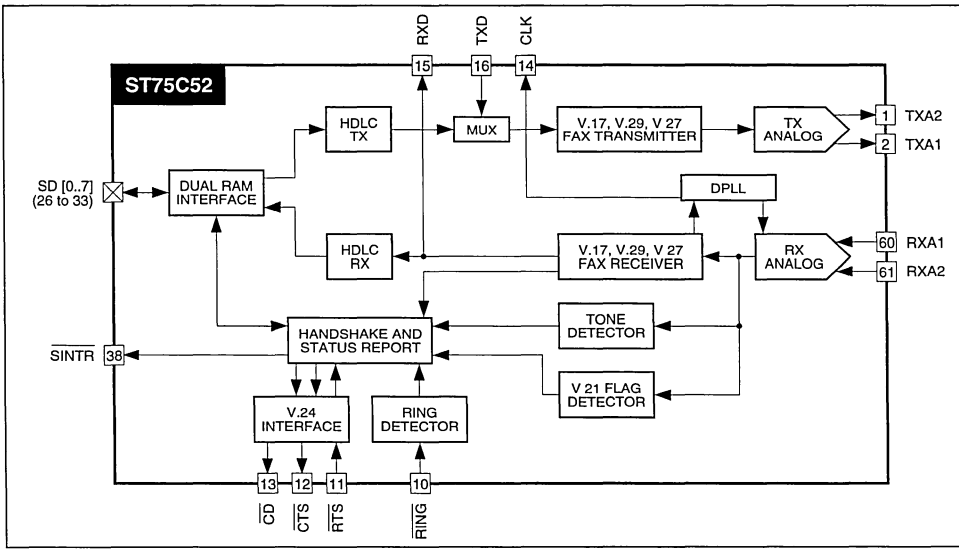
I.7 - Power Supply

Symbol	Parameter
V_{DD}	Digital +5V (Pin 9, 25, 41). To be connected to AV_{DD} (see below).
GND	Digital Ground (Pin 8, 24, 40). To be connected to AGNDT and AGNDR (see below).
AV_{DD}	Analog +5V (Pin 62). To be connected to V_{DD} (see below).
AGNDT	Analog Transmit Ground (Pin 64). To be connected to GND (see below).
AGNDR	Analog Receive Ground (Pin 59). To be connected to GND (see below).

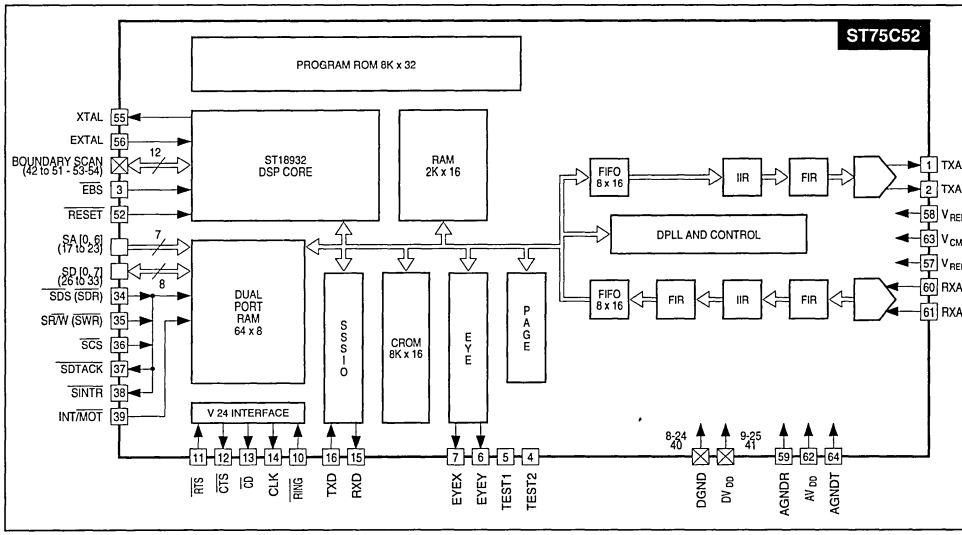
AGNDT and AGNDR must be connected together as close as possible to the chip.
GND and AGNDR board plans should be separated, then connected together as close as possible to the chip, at a single point. Similarly V_{DD} and AV_{DD} must ne connected as close as possible to the chip, at a single point.

II - BLOCK DIAGRAMS

II.1 - Functional Block Diagram



II.2 - Hardware Block Diagram



III - ELECTRICAL SPECIFICATIONS

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical value are given for V_{DD} = +5V and t_{amb} = 25°C.

III.1 - Maximum Ratings (referenced to GND)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3 to 7.0	V
V_I, V_{IN}	Digital or Analog Input Voltage	-0.3 to (V_{DD} + 0.3)	V
I_I, I_{IN}	Digital or Analog Input Current	± 1	mA
I_O	Digital Output Current	± 20	mA
I_{OUT}	Analog Output Current	± 10	mA
T_{oper}	Operating Temperature	0, + 70	°C
T_{stg}	Storage Temperature (plastic)	- 40, + 125	°C
P_{tot}	Maximum Power Dissipation	1000	mW

Stresses above those hereby listed may cause damage to the device. The ratings are stress related only and functional operation of the device at conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

III.2 - DC Characteristics

V_{DD} = 5.0V ± 5%, GND = 0V, T_{amb} = 0 to 70°C (unless otherwise specified).

III.2.1 - Power Supply and Common Mode Voltage

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DD}	Supply Current		100	130	mA
I_{DD-lp}	Supply Current in Low Power Mode		1		mA
V_{CM}	Common Mode Voltage	V_{DD}/2 -5%	V_{DD}/2	V_{DD}/2 + 5%	V

III.2.2 - Digital Interface

All digital pins except XTAL Pins.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage	-0.3		0.8	V
V_{IH}	High Level Input Voltage	2.2			V
I_I	Input Current $V_I = V_{DD}$ or V_I = GND	-10	0	+10	µA
V_{OH}	High Level Output Voltage (I_{load} = 2mA)	2.4			V
V_{OL}	Low Level Output Voltage (I_{load} = 2mA)			0.4	V
I_{OZ}	Three State Input Leakage Current (GND < V_O < V_{DD})	-50	0	50	µA
C_{IN}	Input Capacitance		5		pF

Crystal oscillator interface (XTAL, EXTAL).

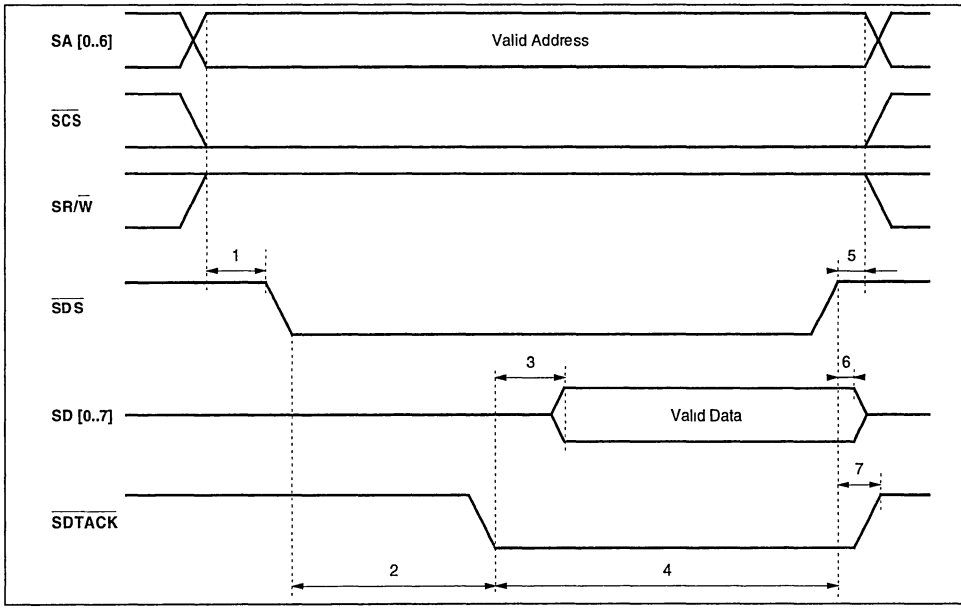
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage			1.5	V
V_{IH}	High Level Input Voltage	3.5			V
I_L	Low Level Input Current GND < V_I < V_{ILmax}	-15			µA
I_H	High Level Input Current VIHmin < V_I < V_{DD}			15	µA

III.2.3 - Analog Interface

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{REF}	Differential Reference Voltage Input = V_{REFP} - V_{REFN}		2.40	2.50	2.60	V
V_{CMOin}	Input Common Mode Offset, v = (RXA1+RXA2)/2 - V_{CM}		-300		300	mV
V_{DIFin}	Differential Input Voltage RXA1 - RXA2				2 x V_{REF}	V_{PP}
V_{CMOout}	Output Common Mode Voltage Offset = (TXA1+TXA2)/2 - V_{CM}		-200		200	mV
V_{DIFout}	Differential Output Voltage TXA1 - TXA2				2 x V_{REF}	V_{PP}
VOFFOut	Differential Output DC Offset (TXA1 - TXA2)		-100		100	mV
Rin	Input Resistance	RXAx	100			kΩ
Rout	Output Resistance	TXAx			20	Ω
RL	Load Resistance	TXAx	10			kΩ
CL	Load Capacitance	TXAx			50	pF

III.3 - AC Electrical Characteristics

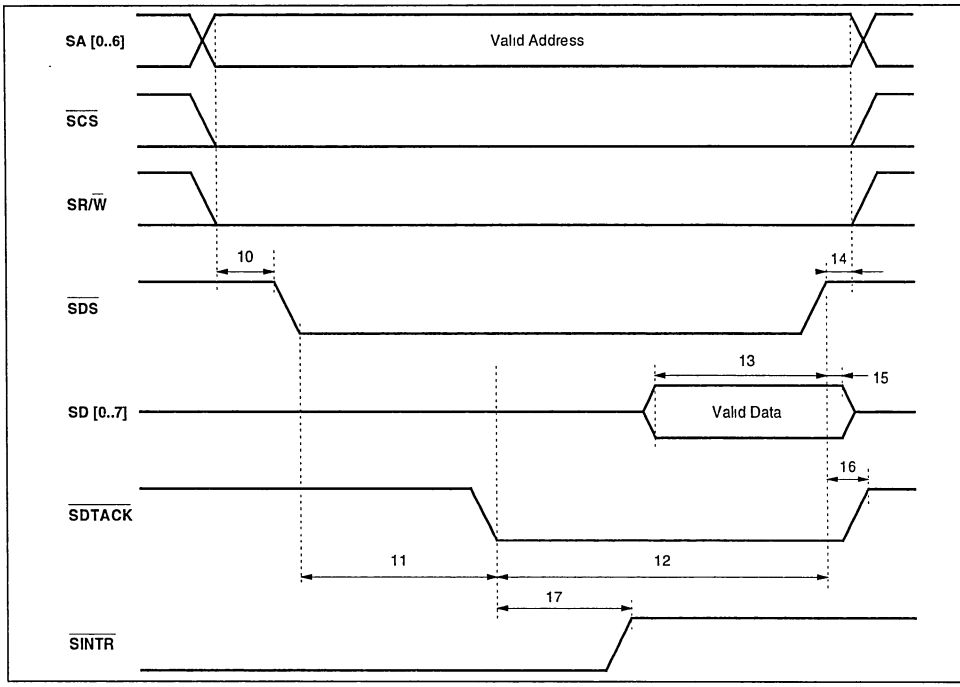
III.3.1 - Dual Port RAM Host Read-Cycle Timing (MOTOROLA mode) (1)



Number	Description	Min.	Typ.	Max.	Unit
1	Address, SR/W, SCS Setup Time	5			ns
2	SDTACK Acknowledge			282(2)	ns
3	SDTACK Prepositionment Time			30	ns
4	Data Strobe Delay	50(3)			ns
5	Address Hold Time	5			ns
6	Data Hold Time	5			ns
7	SDTACK Hold Time	0		10	ns

Notes : 1. This mode is selected if the signal INT/$\overline{MOT}$ is connected to GND.
2. This value is given for a ST75C52 cycle time of 68ns. For different cycle time t_c this value is $4 \cdot t_c + 10$ ns.
3. If the application does not use the SDTACK signal, the minimum SDS low state must be 340ns (or $5 \cdot t_c$).

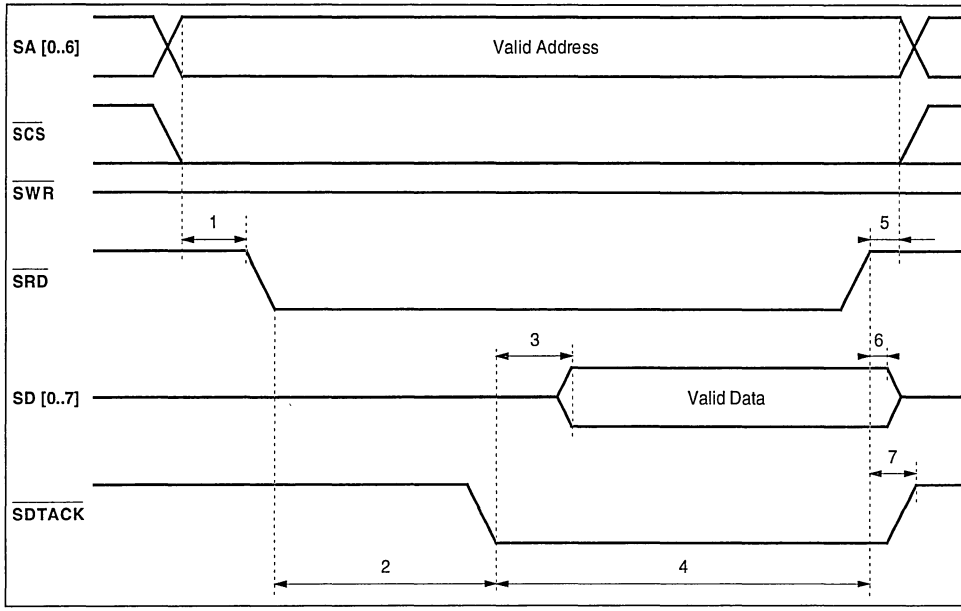
III.3.2 - Dual Port RAM Host Write-Cycle Timing (MOTOROLA mode)



Number	Description	Min.	Max.	Unit
10	Address, SR/W, SCS Setup Time	5		ns
11	SDTACK Acknowledge		282(1)	ns
12	Data Strobe Delay	50(2)		ns
13	Data Setup Time	10		ns
14	Address Hold Time	5		ns
15	Data Hold Time	5		ns
16	SDTACK Hold Time	0	10	ns
17	SINTR Clear Delay	0	78(3)	ns

Notes : 1. This value is given for a ST75C52 cycle time of 68ns. For different cycle time t_c this value is 4 t_c + 10 ns.
2. If the application does not use the SDTACK signal, the minimum SDS low state must be 340ns (or 5 · t_c).
3. The maximum value is t_c + 10ns.

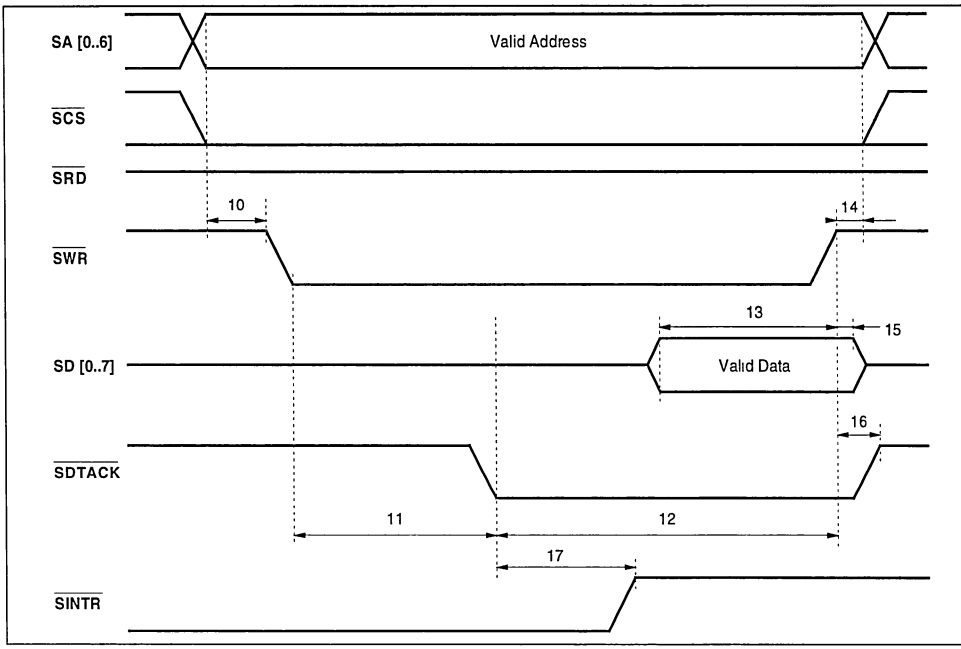
III.3.3 - Dual Port RAM Host Read-Cycle Timing (INTEL mode) (1)



Number	Description	Min.	Typ.	Max.	Unit
1	Address, SCS Setup Time	5			ns
2	SDTACK Acknowledge			282(2)	ns
3	SDTACK Prepositionment Time			30	ns
4	SRD Delay	50(3)			ns
5	Address Hold Time	5			ns
6	Data Hold Time	5			ns
7	SDTACK Hold Time	0		10	ns

Notes : 1. This mode is selected if the signal INT/$\overline{MOT}$ is connected to V_{DD}.
2. This value is given for a ST75C52 cycle time of 68ns. For different cycle time t_c this value is 4 t_c + 10 ns
3. If the application does not use the SDTACK signal, the minimum SRD low state must be 340ns (or 5 t_c).

III.3.4 - Dual Port RAM Host Write-Cycle Timing (INTEL mode)



Number	Description	Min.	Max.	Unit
10	Address, SCS Setup Time	5		ns
11	SDTACK Acknowledge		282(1)	ns
12	SWR Delay	50(2)		ns
13	Data Setup Time	10		ns
14	Address Hold Time	5		ns
15	Data Hold Time	5		ns
16	SDTACK Hold Time	0	10	ns
17	SINTR Clear Delay	0	78(3)	ns

Notes : 1. This value is given for a ST75C52 cycle time of 68ns. For different cycle time t_c this value is $4 \cdot t_c + 10$ ns.
2. If the application does not use the SDTACK signal, the minimum SWR low state must be 340ns (or 5 t_c).
3. The maximum value is $t_c + 10$ns.

IV - FUNCTIONAL DESCRIPTION

IV.1 - System Architecture

The chip allows the design of a complete FAX data-pump without any external component. A versatile dual port RAM allows an easy interface with most micro-controllers.

IV.2 - Operation

IV.2.1 - Modes

The modem implementation is fully compatible with FAX modulation recommendations. The modulation can be either Trellis Coded Modulation (TCM) as in V.17 14400, 12000, 9600, 7200bps rates, Quadrature Amplitude Modulation (QAM) as in V.29 9600, 7200, 4800 and V.27ter 4800 and 2400bps. Other modes of operation include tone and DTMF detection or generation, or speech mode.

IV.2.2 - Transmitter Description

The signal pulses are shaped in a dedicated filter further combined with a compromise transmit equalizer suited for transmission over strongly distorted lines. 3 different compromise equalizers are available and can be selected by software.

IV.2.3 - Receiver Description

The receiver section handles complex signals and uses a fractionally spaced complex equalizer. It is able to cope with distant modem timing drifts up to 10^{-4} as specified in the ITU-T recommendations. It also compensate for frequency drift up to 10Hz and for phase jitter at multiple and simultaneous frequencies.

IV.2.4 - Tone Generator Description

Four tones can be simultaneously generated by the ST75C52. The tones are determined by their frequencies and by the output amplitude level. A set of specific commands are also available for DTMF generation (using two of the four generators available).

IV.2.5 - Tone Detector Description

Sixteen tones can be simultaneously detected by the ST75C52. Each of the tones to be detected is defined by the coefficients of a 4th order programmable IIR. Detection thresholds are also programmable from -45dBm up to -10dBm. DTMF detection is also available and is performed by a specific filter section (that requires no programming).

IV.2.6 - DTMF Detector Description

A DTMF Detector is included in the ST75C52, it allows detection of valid DTMF Digits. A valid DTMF Digit is defined as a dual Tone with a total power higher than -35dBm, a duration higher than 40ms and a differential amplitude within 8dB (negative or positive).

IV.2.7 - Voice Mode

The ST75C52 voice mode allows the implementation of enhanced telephone functions like answering machines. The incoming samples (9600Hz), received from the line are PCM A-law coded and writen into the dual port RAM. The outpoing samples are decompressed using the same A-law and output to the telephone line.

The voice mode is entered using a CONF command, it can be either transmit voice from the dual RAM Tx buffer to the telephone line, receive voice from the telephone line to the dual RAM buffer, or both of these functions simultaneously. The format of the signal is A-law coded without complementation of the even bits. The buffer mechanism, between the host micro-controler and the ST75C52, is identical to the mechanism used for parallel data exchanges except that it starts immediately after CONF command, the size of the transmit and received buffer, are and must be 8 bytes, there is no need for a XMIT command, and if an overrun or underrun condition occurs no error will be reported to the host processor.

IV.2.8 - Analog Loop Back Test Mode

In any transmission standard and serial data format, the ST75C52 can be configured for analog loop back test.

IV.2.9 - Low Power Mode

Sleep state can be attained by a SLEEP command. Activating the reset signal or any other interrupt signal will wake up the data-pump. When in sleep mode, the dual port RAM is unavailable and the clocks are disabled.

When entering the low power mode, the ST75C52 stops its oscillator, all the peripherals of the DSP core are stopped in order to reduce the power consumption. The dual RAM is made inacessible. The ST75C52 can be awakened by a hardware reset.

When waking up, the ST75C52 processes exactly as after a hardware reset or an INIT command as described after.

There is a maximum time of 20ms to restart the oscillator after waking up and an additional 5ms after the interrupt to be able to accept any command coming from the host.

IV.2.10 - Reset

After a hardware reset, or an INIT command, the ST75C52 clears all its internal memories, clears the whole dual RAM and starts to initialize the delta sigma analog converters. As soon as these initializations are completed, the ST75C52 clears the dual RAM address 0 (COMSYS), generates an interrupt IT6 (command acknoledge) and is programmed to send and receive tones, the bit clock and the sample clock are programmed to 9600Hz. The total duration of the reset sequence is about 5ms. After that time the ST75C52 is ready to execute commands sent by the host micro-controller. The duration of the reset signal should be greater than 700ns.

IV.3 - Modem Interface

IV.3.1 - Analog Interface

The modem designer must provide a proper hybrid interface to the ST75C52. An example of hybrid design is given in paragraphs XII and XIII. The inputs and outputs of the MAFE are differential, achieving thus a better noise immunity. The D/A converter output amplifier includes a single pole low-pass filter, its cut-off frequency is :

F_c - 3dB # 19200Hz.

Continuous-time filtering of the analog differential output is necessary using an off-chip amplifier and a few external passive components.

IV.3.2 - Host Interface

The host interface is seen by the micro as a 64x8 RAM, with additional registers accessible through an 8-bit address space. A selection Pin (INT/MOT) allows to configure the host bus for either INTEL or MOTOROLA type control signals.

V - USER INTERFACE

V.1 - Dual Port Ram Description

The dual port RAM is the standard interface between the controller and the ST75C52, for either commands or data. This memory is addressed through a 7-bit address bus. The locations from $00 to $3F are RAM locations, while locations from $40 to $50 are control registers dedicated to the interrupt handling.

Several functional areas are defined in the dual port RAM, namely :

- the command area,
- the report area,
- the status area,
- the data buffer area.

V.1.1 - Mapping

V.1.1.1 - Command Area

The command area is located from $00 to $04. Address $00 holds the command byte COMSYS, and the next four locations hold the parameters COMPAR[0..3]. The command parameters must be entered before the command word is issued. Once the command has been entered, the command byte is reset and an acknowledge report is issued. A new command should not be issued before the acknowledge counter COMACK is incremented.

V.1.1.2 - Report Area

The report area is located from address $05 to address $07. Location $05 holds the acknowledge counter COMACK. Each time a command is acknowledged, the report bytes COMREP[0..1] (if any) are written by the ST75C52 into locations $06 and $07, and the content of COMACK is incremented. This counter allows the ST75C52 to accurately monitor the command processing.

V.1.1.3 - Status Area

The status area is located from address $08 to $0A. The error status word SYSERR is located at address $08. This error status word is updated each time an error condition occurs. An optional interruption IT0 may additionally be triggered in the case of an error condition. Locations $09 and $0A hold the general status bytes STATUS[0..1]. The meaning of the bits depends on the mode of operation, and is described in Chapter VII. The third byte at address $0B holds the Quality Monitor byte STAQUA.

V.1.1.4 - Optional Status Area

The user can program (through the DOSR command) the three locations STAOPT[0..2] of the Optional Status Area ($0C to $0E) for the real time monitoring of three arbitrary memory locations.

V.1.1.5 - Data Buffer Area

The data area is made of four 8-byte buffers. Two are dedicated to transmission and the two others to reception. Each of the four buffers is attached to a status byte. the meaning of the status byte depends on the selected format of transmission. Within each buffer, D0 represents the first bit in time.

V.1.2 - Interruptions

The ST75C52 can generate 5 interrupts for the controller. The interrupt handling is made with a set of registers located from $40 to $50.

The interruptions generated by the ST75C52 come from several different sources. Once the ST75C52 raises an interrupt, a signal is sent to the controller. The controller has then to process the interrupt and clear it. The interrupt source can be examined in the Interrupt Source Register ITSRCR located at $50. According to this status byte, the interrupt source can be determined. Then, writing a zero at one of the memory location $40 to $46 (Reset Interrupt Registers ITREST[0..6]) will reset the corresponding interrupt (and thus acknowledge it). These sources of interruptions can be masked globally or individually using the Interrupt Mask Register ITMASK located at $4F.

The interrupt sources are :

- **IT0 : Error/Warning**
  This signifies that an error has occurred and the error code is available in the error status byte SYSERR. This byte can be selectively cleared by the CSE command.
- **IT2 : Tx Buffer**
  Each time the ST75C52 frees a buffer, this interrupt is generated.
- **IT3 : Rx Buffer**
  Each time the ST75C52 has filled a buffer, this interrupt is generated.
- **IT4 : Status Byte**
  This signifies that the status byte has changed and must be checked by the controller.
- **IT6 : Command Acknowledge**
  This signifies that the ST75C52 has read the last command entered by the host, incremented the command counter COMACK, and is ready for a new command.

ITSRCR	X	D6	X	D4	D3	D2	X	D0

D0 = 1 IT0 Pending
D2 = 1 IT2 Pending
Dn = 1 ITn Pending

ITMASK	D7	D6	D5	D4	D3	D2	X	D0

D7 and D0 = 1 IT0 Enable D
D7 and D2 = 1 IT2 Enable D
....
D7 and D6 = 1 IT6 Enable D

V.1.3 - Host Interface Summary

Address (hex)	Description	Size (Byte)	Mnemonic
COMMAND AREA			
$00	Command	1	COMSYS
$01-$04	Command Parameters	4	COMPAR[0..3]
REPORT AREA			
$05	Acknowledge Counter	1	COMACK
$06-$07	Report	2	COMREP[0..1]
STATUS AREA			
$08	Error Status	1	SYSERR
$09-$0A	General Status	2	STATUS[0..1]
$0B	Quality Monitor	1	STAQUA
$0C-$0E	Optional Report	3	STAOPT[0..2]
DATA AREA			
$1C	Data Rx Buffer 0 Status	1	DTRBS0
$1D-$24	Data Rx Buffer 0	8	DTRBF0[0..7]
$25	Data Rx Buffer 1 Status	1	DTRBS1
$26-$2D	Data Rx Buffer 1	8	DTRBF1[0..7]
$2E	Data Tx Buffer 0 Status	1	DTTBS0
$2F-$36	Data Tx Buffer 0	8	DTTBF0[0..7]
$37	Data Tx Buffer 1 Status	1	DTTBS1
$38-$3F	Data Tx Buffer 1	8	DTTBF1[0..7]
INTERRUPT AREA			
$40-$46	Reset Interrupt Reg.	7	ITREST[0..6]
$4F	Interrupt Mask Reg.	1	ITMASK
$50	Interrupt Source Reg.	1	ITSRCR

V.2 - Command Set

The Command Set has the following attractive features :

- user friendly with easy to remember mnemonics,
- possibility of straightforward expansion with new commands to suit specific customer requirements,
- easy upgrade of existing software using previous modem based SGS-THOMSON products.

The command set has been designed to provide the necessary functional control on the ST75C52. Each command is classified according to its syntax and the presence/absence of parameters. In the case of a parametric command, parameters must first be written into the dual port RAM before the command is issued. Acknowledge and error report is issued for each command entered.

V.2.1 - Command Set Summary

V.2.1.1 - Operational Control Commands

INIT Initialize. Initialize the modem engine. Set all parameters to their default values and wait for commands of the control processor. Non parametric command.

IDT Identify. Return the product identification code. Non parametric command.

SLEEP Turn to low power mode, the ST75C52 enters the low power mode and stops its crystal oscillator to reduce power consumption. In this mode all the clocks are stopped and the dual RAM is unreachable. It can be awakened by either a hardware reset, a low level on the RING Pin or a dummy write of its dual RAM.

HSHK Handshake. Begins the handshake sequence. The modem engine generates all the sequences defined in the ITU-T recommendations. A status report indicates to the control processor the state of the handshake. This command only applies to modes where a handshake sequence is defined. A CONF command must have been issued prior to the use of HSHK. Non parametric command.

STOP FAX Stop. Stop FAX Half-duplex transmitter. Non parametric command.

SYNC FAX Synchronize. Start/Stop of FAX Half-duplex receiver. Parametric command.

CSE Clear Status Error. Selectively clears the Error status byte SYSERR. Parametric command.

SETGN Set Gain. This command sets the global gain factor, which is used for the transmit samples. Parametric command.

V.2.1.2 - Data Communication Commands

XMIT Transmit Data. Start/stop the transmission of data in parallel mode. After a XMIT command, the ST75C52 sends the data contained in its dual port RAM.

SERIAL Select Serial or Parallel Mode. This command selects the data source, i.e. either parallel or serial. The parallel mode uses a part of the dual port RAM as a double buffer. The serial mode uses the serial synchronous I/O. Parametric command.

FORM Selects the Transmission Format (only in parallel mode). This command configures the data interface for both receiver and transmitter according to the selected data format. Parametric command (HDLC or synchronous). In serial mode, format is always synchronous.

V.2.1.3 - Memory Handling Commands

MW Memory Write. This command is used to write an arbitrary 16-bit value into the writable memory location currently specified by a parameter. Parametric command.

MR Memory Read. This command allows the controller to read any of the ERAM or CROM (ST75C52 memory spaces) location without interrupting the processor. Parametric command.

CR Complex Read. This command allows the controller to read at the same time the real and imaginary part of a complex value stored in a double ERAM or CROM location. This feature is very interesting for eye pattern software control and for equalization monitoring. This command insures that the real and imaginary parts are sampled in the memory at the same time (integrity). Parametric command.

V.2.1.4 - Configuration Control Commands

CONF Configure. This command configures the modem engine for data transmission and handshake procedures (if any) in any of the supported modes. The transmission parameters are set to their default values and can be modified with the MODC command. Parametric command.

MODC Modify Configuration. This command allows modification of some of the parameters which have been set up by the CONF command. It can also be used to alter the mode of operations (short train). Parametric command.

DOSR Define Optional Status Report. This command allows the modification of the optional status report located in the status area of the dual port RAM. One can thus select a particular parameter to be monitored during all modes of operation. Parametric command.

DSIT Define Status Interrupt. This command allows the programming of the status word bit that will generate an Interrupt to the controller. Parametric command.

V.2.1.5 - Tone Generation Commands

TONE Select Tone. Programs the tone generator(s) for the desired default tone(s). Additional mnemonics provide quick programming of DTMF tones or other currently used tones. Parametric command.

DEFT Define Tone. Programs the tone generator(s) for arbitrary tone synthesis. Parametric command.

TGEN Tone Generator Control. Enables or disables the tone generator(s). Parametric command.

IV.2.1.6 - Tone Detection Commands

TDRC Read Tone Detector Coefficient. Read one Tone Detector Coefficient. Parametric command.

TDWC Write Tone Detector Coefficient. Write one Tone Detector Coefficient. Parametric command.

TDRW Read Tone Detector Wiring. Read one Tone Detector Wiring connection. Parametric command.

TDWW Write Tone Detector Wiring. Write one Tone Detector Wiring connection. Parametric command.

TDZ Clear Tone Detector Cell. Clear internal variables of a Tone Detector Cell. Parametric command.

V.2.1.7 - Miscellaneous Commands

CALL Call a Subroutine. Call a subroutine with one Parameter. Parametric command.

JSR Call a Low Level Subroutine. Call an internal subroutine with one parameter. Parametric command.

V.3 - Command Set Short Form

CCI Command		
Mnemonic	**Value**	**Description**
XMIT	0x01	Transmit Data
SETGN	0x02	Set Transmit Gain
SLEEP	0x03	Power Down the ST75C52
HSHK	0x04	Start Handshake
INIT	0x06	Initialize (Software Master RESET)
SERIAL	0x07	Enable/disable Data Serial Mode
CSE	0x08	Clear Error Status Word
FORM	0x09	Define Parallel Data Format
DOSR	0x0A	Define Optional Status Report
TONE	0x0C	Generate Predefined Tones
TGEN	0x0D	Enable Tone Generator
DEFT	0x0E	Define Arbitrary Tone
MR	0x10	Memory Read
CR	0x11	Complex Read
MW	0x12	Memory Write
DSIT	0x13	Define Status Interrupt
IDT	0x14	Return Product Identification Code
JSR	0x18	Call a Low Level Subroutine
CALL	0x19	Call a Subroutine
TDRC	0x1A	Tone Detector Read Coefficient
TDRW	0x1B	Tone Detector Read Wiring
TDWC	0x1C	Tone Detector Write Coefficient
TDWW	0x1D	Tone Detector Write Wiring
TDZ	0x1E	Tone Detector Clear Cell
CONF	0x20	Configure
MODC	0x21	Modify Default Configuration
STOP	0x25	FAX Stop Transmitter
SYNC	0x26	FAX Synchronize Receiver

V.4 - Status - Reports

V.4.1 - Status

The ST75C52 has a dedicated status reporting area located in its dual port RAM. This allow a continuous monitoring of the status variables without interrupting the ST75C52.
The first status byte gives the error status. Issuing of an error status can also be flagged by a maskable interrupt for the controller. The signification of the error codes are given in Chapter VII.
The second and third status bytes give the general status of the modem. These status include for example the ITU-T circuit status and other items described in appendix. These two status can generate, when a change occurs, an interrupt to the controller ; each bit of the two byte word can be masked independently.
The forth byte gives in real time a measure of the reception quality. This information may be used by the controller to monitor the quality of the received bits.
Three other locations are dedicated for custom status reporting. The controller can program the ST75C52 for a real time monitoring of any of its internal RAM location. High byte or low byte of any word can thus be monitored.

V.4.2 - Reports

The ST75C52 features an acknowledge and report facility. The acknowledge of a command is monitored by a counter COMACK located in the dual port RAM. Each time a command is read from the command area, the ST75C52 will increment this counter. For instance, when a MR (Memory Read) command is issued, the data is first written in the report area, and the counter is incremented afterwards. This way of processing insures data integrity and gives additional synchronization between the controller and the data pump.

V.5 - Data Exchanges

The ST75C52 accepts many kinds of data exchange : the default mode uses the synchronous serial exchange. Other modes include HDLC framing support and synchronous parallel exchanges. Detailed description of the Data Buffer Exchanges modes is available in the paragraph IX.

V.5.1 - Synchronous Parallel Mode

The data exchanges are made through the dual port RAM and are byte synchronous oriented. The double buffer facilities of the ST75C52 allow an efficient buffering of the data.

V.5.1.1 - Transmit

The controller must first fill at least the first buffer of data (Tx Buffer 0) with the bits to be transmitted. In order to perform this operation, the controller must first check the Tx Buffer 0 status word DTTBS0. If this buffer is empty, the controller fills the data buffer locations (up to 64 bits), and then writes in DTTBS0 the number of bytes contained in the buffer. The controller can then either proceed with the second buffer or initiate the transmission with a XMIT command.
The ST75C52 copies the contents of the data buffer and then clears the buffer status word in order to make it again available, then generates an IT2 interrupt. The number of bytes specified by the status word is then queued for transmission. The process goes on with the two buffers until an XMIT command stops the transmission. After the finishing XMIT command has been issued, the last buffers are emptied by the ST75C52.
Errors occur when both buffers are empty while the transmit bit queue is also empty. Error is signalled with an IT0 interruption to the controller.

V.5.1.2 - Receive

The controller should take care of releasing the Rx buffers before the Data Carrier Detect goes true. This is made by writing zero in the Rx Buffer Status 0 and 1. The ST75C52 then fills the first buffer, and once filled sets the status word with the number of bytes received and then generates an IT3 interrupt. It then takes control of the second buffer and operates the same way. The controller must check the status of the buffers and empty them. Once the data read, the controller must release the used buffer and wait for the next buffer to be filled.
Error occurs when both buffers are declared full, and incoming bits continue to arrive from the line. Error is signaled by an IT0 interrupt.

V.5.2 - HDLC Parallel Mode

This mode implements part of the High Level Data Link Control formats and procedures. It is well suited for error correcting protocols like ECM or FAX T4/T30 recommendations. It supports the flagging generation, 16-bit Frame Check Sequence, as well as the Zero insertion/deletion mechanism.

V.5.3 - Serial Exchanges

The other mode of operation for data exchanges is the Serial Synchronous Mode. In this mode, the data I/O is made through the V.24 interface (page 4). Even when using the parallel mode described above, the received bits are available on the ST75C52 RxD Pin. See paragraph VII.2.1 table for clock values.

VI - COMMAND SET DESCRIPTION

The appendix A contains the description of the complete command set. Commands are presented according to the following form :

COMMAND

Command Name Meaning

COMMAND

Opcode Hexadecimal digit

X	X	X	X	X	X	X	X

Synopsis Short description of the functions performed by the command.

Parameters

Field	Byte	Pos.	Value	Definition
Name	X	b..a	xx *	Explanation of the parameter Default value

Field Name of the addressed bit field.

Byte Index (or address in the dual port RAM) of the parameter byte (from 1 to 4).

Pos. Bit field position inside the parameter byte. Can either be a single position (from 0 to 7, 0 being LSB) or a range.

Value Possible values for the bit (resp. bit field). Range means all values are allowed. A star means a default value. Values are expressed either under the form of a bit string, or under hexadecimal format.

CALL

Call a Subroutine

CALL

Opcode: 19

0	0	0	1	1	0	0	1

Synopsis CALL allows to execute a part of the ST75C52 firmware with a specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	7..0		Low byte of the call address
C_ADDR_H	2	7..0		High byte of the call address
C_DATA_L	3	7..0		Low byte of the argument
C_DATA_H	4	7..0		High byte of the argument

CONF — Configure for Operations — CONF

Opcode 20

0	0	1	0	0	0	0	0

Synopsis CONF allows the complete definition of the ST75C52 operation, including the mode of operation (tone, FAX transmit, FAX receive, voice transmit, voice receive, DTMF receive, ...) and the modem parameters (standard, speed, ...).

Parameters

Field	Byte	Pos.	Value	Definition
CONF_OPER	1	3..0	-	Mode of operation, see below
CONF_ANAL	1	4	0 1	Normal mode Analog loop back (test mode only)
CONF_PSTN	1	5	0 1	PSTN (carrier detect set to -43/-48dBm) Leased line (carrier detect -33/-38dBm)
CONF_AO	1	6	0 1	Answer mode (FSK full duplex only) Originate mode (FSK full duplex only)
CONF_V24	1	7	0 1	Do not use RTS pin signal Use RTS pin signal
CONF_MODE	2	5..0	1 3 4 7 8 9 C D Other	Bell 103 (full duplex) V.21 (full duplex) V.23 (full duplex) V.27ter V.29 V.17 V.33 (half duplex) V.21 channel 2 Reserved
CONF_TXEQ	2	7..6	0 1 2 3	No transmit equalizer Transmit equalizer #1 Transmit equalizer #2 Transmit equalizer #3
CONF_CAR	3	0	0 1	1800Hz carrier (V.17/V.33 only) 1700Hz carrier (V.17/V.33 only)
CONF_SP0	3	7..5	xx1 x1x 1xx	2400bps allowed (V.27) 4800bps allowed (V.27, V.29) 7200bps allowed (V.29, V.17)
CONF_SP1	4	2..0	xx1 x1x 1xx	9600bps allowed (V.29, V.17) 12000bps allowed (V.17, V.33) 14400bps allowed (V.17, V.33)

According with the 4 first bits of the CONF_OPER the ST75C52 is put into the following mode of operation.

CONF_OPER	Transmit	Received
0000*	Tones	Tones
0010	Voice	Tones
0100	Tone	DTMF
0110	Voice	DTMF
1000	Tones	Voice
1010	Voice	Voice
1111	Modem	Modem
Other	Not allowed	Not allowed

CR — Complex Read — CR

Opcode: 11

0	0	0	1	0	0	0	1

Synopsis CR allows the reading of a complex parameter. The parameter specifies the parameter address (for the real part : the imaginary part is next location). CR returns the high byte value of both real and imaginary part of the addressed complex parameter.

Parameters

Field	Byte	Pos.	Value	Definition
CR_ADDR_L	1	7..0		Low byte of the 16-bit address
CR_ADDR_H	2	7..0		High byte of the 16-bit address

CSE — Clear Error Status — CSE

Opcode: 08

0	0	0	0	1	0	0	0

Synopsis CSE is used to clear the ST75C52 error status SYSERR byte. It is also used as an acknowledge to the error condition handler. For details, please refer to the corresponding appendix.

Parameters

Field	Byte	Pos.	Value	Definition
ERR_MASK	1	7..0		Error mask See report appendix for detailed meaning

DEFT — Define Arbitrary Tone — DEFT

Opcode: 0E

0	0	0	0	1	1	1	0

Synopsis DEFT programs one of the four tone generator for arbitrary tone generation. The parameter is the frequency of the generated tone expressed in Hertz between 0 and 3600Hz.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_GEN_SL	1	1..0		Index of the tone generator (3..0)
TONE_FREQ_L	2	7..0		Low byte of the frequency
TONE_FREQ_H	3	7..0		High byte of the frequency (internally masked with 0F)
TONE_SCALE	4	7..0		Amplitude scaling factor (high byte) 3F gives the nominal amplitude

DOSR — Define Optional Status Report — DOSR

Opcode: 0A

0	0	0	0	1	0	1	0

Synopsis DOSR specifies the address of the RAM variables to be monitored in the 3 locations STAOPT[0..2] of the dual port RAM. It also specifies the assignment within the 3 locations.

Parameters

Field	Byte	Pos.	Value	Definition
STA_OPT_ASS	1	1..0	0..2	Index of the STAOPT destination
STA_OPT_ADL	2	7..0		Low byte of source address
STA_OPT_ADH	3	3..0		High byte of source address
STA_OPT_HL	3	7	0 1	Select low byte of source Select high byte of source

DSIT — Define Status Interrupt — DSIT

Opcode: 13

0	0	0	1	0	0	1	1

Synopsis DSIT specifies the bit mask used with the STATUS[0] and STATUS[1] byte to generate an interrupt IT4 to controller. Each time a bit change happens in the status words, assuming the corresponding bit mask will be set, an interrupt will be generated.

Parameters

Field	Byte	Pos.	Value	Definition
STA_IT_MSK0	1	7..0		Status[0] bit mask pattern
STA_IT_MSK1	2	7..0		Status[1] bit mask pattern

Notes : The default IT Status is 0x3F for STATUS[0] and 0xFF for STATUS[1].

FORM — Select Transmission Format — FORM

Opcode: 09

0	0	0	0	1	0	0	1

Synopsis FORM defines the type of transmission used. This format is valid only in the parallel data mode. The default format, unless specified, is synchronous.

Parameters

Field	Byte	Pos.	Value	Definition
X_SYNC	1	1..0	00* 01 10 11	Synchronous format Transmit continous "1" (1) HDLC framing Transmit continous "0" (1)

Notes : 1. This format is only valid for the transmiter.

HSHK — Handshake — HSHK

Opcode: 04

0	0	0	0	0	1	0	0

Synopsis HSHK is used to command the ST75C52 to begin the transmit handshake sequence processing. The progress of the handshake is reported to the control processor.

Parameter Non parametric command.

IDT — Identify — IDT

Opcode: 14

0	0	0	1	0	1	0	0

Synopsis IDT Return the ST75C52 Hardware and Software release number. See paragraph VII.1.4.

Parameter Non parametric command.

INIT — Initialization — INIT

Opcode: 06

0	0	0	0	0	1	1	0

Synopsis INIT forces the ST75C52 to reset all parameters to their default conditions and restart operations.

Parameter Non parametric command.

Notes : This command makes a software reset of the ST75C52 and so cannot have the regular handshake protocol. It does not increment the COMACK, neither generate an Interrupt.

JSR — Call a Low Level Subroutine — JSR

Opcode: 18

0	0	0	1	1	0	0	0

Synopsis JSR allows to execute a part of the ST75C52 firmware with a specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	7..0		Low byte of the call address
C_ADDR_H	2	7..0		High byte of the call address
C_DATA_L	3	7..0		Low byte of the argument
C_DATA_H	4	7..0		High byte of the argument

MODC — Modify Configuration — MODC

Opcode: 21

0	0	1	0	0	0	0	1

Synopsis MODC allows modification of the configuration for special purpose. This command has no effect while in data mode, the parameters are just sampled when starting to transmit or receive. The value of these parameters are not affected when sending a CONF command.

Parameters

Field	Byte	Pos.	Value	Definition
MODC_SH	1	6	0* 1	Normal training sequence Short training (1) sequence
MODC_FPT	2	3..2	00* 01 10	No echo protection tone Long echo protection tone (180ms) Short echo protection tone (30ms)

Notes : 1. Short train sequence must be preceded by at least one normal training sequence.

MR — Memory Read — MR

Opcode: 10

0	0	0	1	0	0	0	0

Synopsis MR allows the reading of a 16-bit parameter. The parameter specifies the parameter address.

Parameters

Field	Byte	Pos.	Value	Definition
MR_ADDR_L	1	7..0		Low byte of the 16-bit address
MR_ADDR_H	2	7..0		High byte of the 16-bit address

MW — Memory Write — MW

Opcode: 12

0	0	0	1	0	0	1	0

Synopsis MW allows the writing of a 16-bit parameter. The parameter specifies the address as well as the value to be transferred.

Parameters

Field	Byte	Pos.	Value	Definition
MW_ADDR_L	1	7..0		Low byte of the 16-bit address
MW_ADDR_H	2	7..0		High byte of the 16-bit address
MW_VALUE_L	3	7..0		Low byte of the 16-bit value
MW_VALUE_H	4	7..0		High byte of the 16-bit value

SERIAL — Select Serial or Parallel Mode — SERIAL

Opcode: 07

0	0	0	0	0	1	1	1

Synopsis SERIAL defines the data path, i.e. either serial or parallel.

Parameters

Field	Byte	Pos.	Value	Definition
TX_SDATA	1	0	0* 1	Use serial link for Tx Data Use parallel link for Tx Data
RX_SDATA	1	1	0* 1	Use only serial link for Rx Data Use also parallel link for Rx Data

Notes : The received Bits always go to the output pin RXD, even when the RX_SDATA bit is set.

SETGN — Set Output Gain — SETGN

Opcode: 02

0	0	0	0	0	0	1	0

Synopsis SETGN is a command which sets the scaling factor of the transmit samples. It is used for setting the output level or for setting the level of the tone generators. The gain value is given in the form of a 2's complement 16-bit value.

Parameters

Field	Byte	Pos.	Value	Definition
GAIN_L	1	7..0	range FF*	Low byte of the 16-bit gain value
GAIN_H	2	7..0	range 7F*	High byte of the 16-bit gain value

Example

Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)
0	7FFF	-5	47FA	-10	287A
-1	7214	-6	4026	-11	2413
-2	65AC	-7	392C	-12	2026
-3	5A9D	-8	32F5	-13	1CA7
-4	50C3	-9	2D6A	-14	198A

SLEEP — Turn to Sleep Mode — SLEEP

Opcode: 03

0	0	0	0	0	0	1	1

Synopsis SLEEP is used to force the ST75C52 to turn to low power mode.

Parameter Non parametric command.

Notes : When receiving this command the ST75C52 will stop processing and so cannot have the regular handshake protocol. It does not increment the COMACK, neither generate an Interrupt. A negative level on the RING Pin or a dummy dual RAM write will awake the ST75C52, generate an IT5 Interrupt and execute a Software Reset (idem **init**).

STOP — FAX Stop Transmitter — STOP

Opcode: 25

0	0	1	0	0	1	0	1

Synopsis STOP is used, in FAX Modes, to force the ST75C52 to turn off the transmitter in accordance with the corresponding ITU-T V.33/V.17/V.29/V.27 recommendation.

Parameter Non parametric command.

Notes : When receiving this command the ST75C52 will stop sending regular Data. In parallel mode this command must be preceded by a **XMIT** Stop command. In parallel mode the ST75C52 will wait until all the transmit buffers are sent before starting the Stop sequence.

SYNC — FAX Synchronize the Receiver — SYNC

Opcode: 26

0	0	1	0	0	1	1	0

Synopsis SYNC is used, in FAX Modes, to force the ST75C52 to Start/Stop the receiver in accordance with the corresponding ITU-T V.33/V.17/V.29/V.27 recommendation.As soon as the ST75C52 receives the **SYNC** Start command it sets its receiver to detect the FAX synchronization signal.This command is the equivalent **HSHK** command for the receiver.

Parameters

Field	Byte	Pos.	Value	Definition
RX_SYNC	1	0	0* 1	Stop receiver Start receiver synchronization

TDRC — Tone Detector Read Coefficient — TDRC

Opcode: 1A

0	0	0	1	1	0	1	0

Synopsis TDRC Read one Coefficient of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_C_ADDR	2	7..0	0..B 10 20 Other	Biquad coefficient Energy coefficient Static level Reserved

The command answer is : Low Byte of Coefficient followed by High Byte of Coefficient.

TDRW — Tone Detector Read Wiring — TDRW

Opcode: 1B

0	0	0	1	1	0	1	1

Synopsis TDRC Read Wiring of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_W_ADDR	2	0	0 1 Other	Biquad and energy input Comparator inputs Reserved

The command answer is:

a) If TD_W_ADDR = 0 :
- First Byte is the Node Number of the Signal connected to Biquadratic Filter input.
- Second Byte is the Node Number of the Signal connected to the Energy estimator input.

b) if TD_W_ADDR = 1 :
- First Byte is the Node Number of the Signal connected to Comparator Negative input.
- Second Byte is the Node Number of the Signal connected to the Comparator Positive input.

TDWC — Tone Detector Write Coefficient — TDWC

Opcode: 1C

0	0	0	1	1	1	0	0

Synopsis TDWC Write one Coefficient of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_C_ADDR	2	7..0	0..B 10 20 Other	Biquad coefficient Energy coefficient Static level Reserved
TD_COEFL	3	7..0		Low byte of coefficient
TD_COEFH	4	7..0		High byte of coefficient

TDWW — Tone Detector Write Wiring — TDWW

Opcode: 1D

0	0	0	1	1	1	0	1

Synopsis TDRC Write Wiring of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_W_ADDR	2	0	0 1 Other	Biquad and energy input Comparator inputs Reserved

If TD_W_ADDR = 0 (Select Biquad and Energy Inputs)

Parameters

Field	Byte	Pos.	Value	Definition
TD_W_ERN	3		0..3F	Energy estimator signal input
TD_W_BIQ	4		0..3F	Biquad filter signal input

If TD_W_ADDR = 1 (Select Comparator Inputs)

Parameters

Field	Byte	Pos.	Value	Definition
TD_W_CN	3		0..3F	Negative comparator signal input
TD_W_CP	4		0..3F	Positive comparator signal input

TDZ — Tone Detector Clear Cell — TDZ

Opcode: 1E

0	0	0	1	1	1	1	0

Synopsis TDZ Clears all internal variables of one Tone detector cell including Filter local variables and energy estimator. This command must be sent after changing coefficients of a cell to avoid instability.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number

TGEN — Enable/disable Tone Generators — TGEN

Opcode: 0D

0	0	0	0	1	1	0	1

Synopsis TGEN causes the ST75C52 to enable or disable the four tone generators.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_0_ENA	1	0	0* 1	Generator #0 disabled Generator #0 enabled
TONE_1_ENA	1	1	0* 1	Generator #1 disabled Generator #1 enabled
TONE_2_ENA	1	2	0* 1	Generator #2 disabled Generator #2 enabled
TONE_3_ENA	1	3	0* 1	Generator #3 disabled Generator #3 enabled

TONE — Predefined Tones — TONE

Opcode: 0C

0	0	0	0	1	1	0	0

Synopsis TONE programs the tone generators for the predefined tones. The tone generators #0 and eventually #1 are reprogrammed with this command. Eventually the tone generator #0 and #1 are enabled. Using a value not in the following table will disable tone generator #0 and #1.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_SELECT	1	5..0	0 1 2 3 4 5 6 7 8 9 A B C D E F 10 11 12 13	DTMF 0 (941 & 1336Hz) DTMF 1 (697 & 1209Hz) DTMF 2 (697 & 1336Hz) DTMF 3 (697 & 1477Hz) DTMF 4 (770 & 1209Hz) DTMF 5 (770 & 1336Hz) DTMF 6 (770 & 1477Hz) DTMF 7 (852 & 1209Hz) DTMF 8 (852 & 1336Hz) DTMF 9 (852 & 1477Hz) DTMF A (697 & 1633Hz) DTMF B (770 & 1633Hz) DTMF C (852 & 1633Hz) DTMF D (941 & 1633Hz) DTMF * (941 & 1209Hz) DTMF # (941 & 1477Hz) Answer tone (2100Hz) Tone (1650Hz) Answer tone (2225Hz) Tone (1300Hz)

XMIT — Start/stop Transmission — XMIT

Opcode: 01

0	0	0	0	0	0	0	1

Synopsis XMIT start or stop the transmission of the Parallel Transmit Data. This command work only if the Parallel Transmit Data mode has been selected with a **SERIAL** command.

Parameters

Field	Byte	Pos.	Value	Definition
TX_START	1	0	0* 1	Stop transmission Start transmission

VII - STATUS DESCRIPTION

This appendix is dedicated to the ST75C52 reporting features. in the following sections the command acknowledge process and the report and status definitions are explained.

VII.1 - Command Acknowledge and Report

VII.1.1 - Command Acknowledge Process

(see Figure 1)

The ST75C52 features an acknowledge process based on a counter COMACK. On power-on reset (or INIT command), this counter's value is set to 0. Each time a command is successfully executed by the ST75C52, the acknowledge counter COMACK is incremented. This allows a precise monitoring of the command entered and avoids command collision.

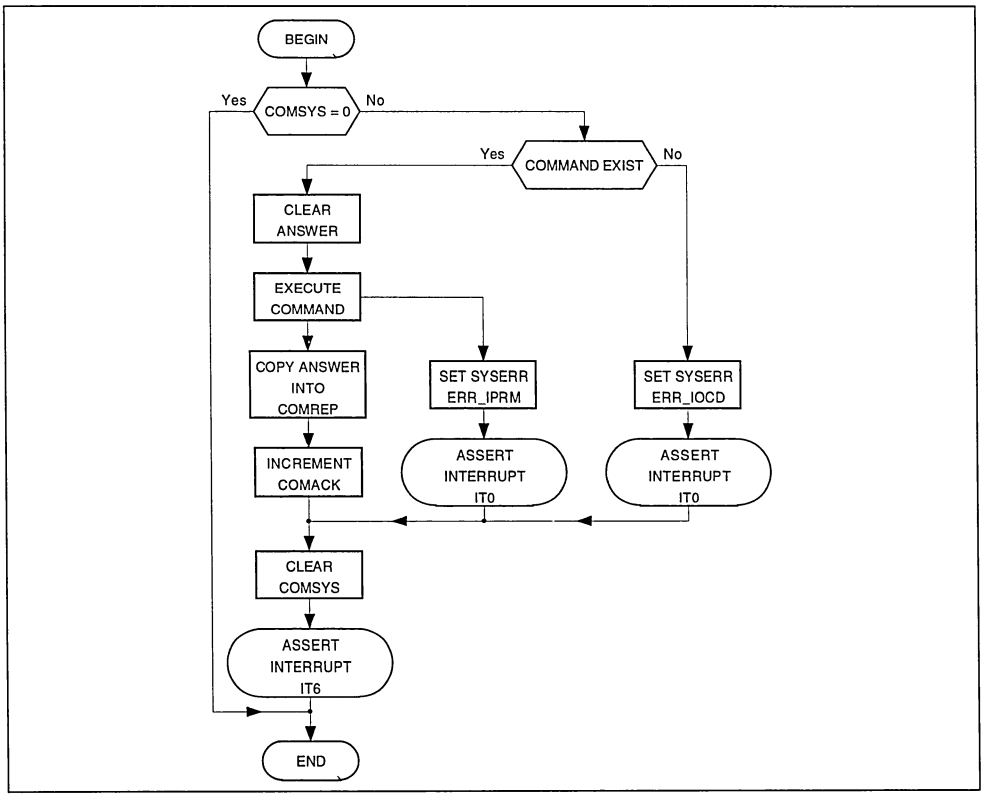
In the case of a memory reading command (CR, TDRC, TDRW, IDT or MR) once the command entered is executed, the report area is filled and the acknowledge counter is incremented afterwards. This insures that the controller will read the value corresponding to its request.

Furthermore, the ST75C52 resets the value of the COMSYS register once the command has been read. The interruption IT6 is raised just after the counter is incremented.

VII.1.2 - Reports Specification

The report section of the Dual Port RAM is dedicated to memory reading. In response to a CR, MR, TDRC, TDRW, IDT commands, the value read is transferred to the report registers COMREP[0..1].

Figure 1 : Command Acknowledge Process



VII.1.3 - CR Command

Issuing a CR command causes the ST75C52 to dump a specific memory location in complex mode. This instruction is particularly useful for equalizer state analysis or for software eye-pattern display. The report area has this meaning :

RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0	COMREP[0]
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	COMREP[1]

RP0..RP7 is the MSB part of the 16-bit value of the real part and IP0..IP7 is the MSB part of the imaginary part. The CR command insures that the real and imaginary part of the desired complex value are sampled internally at the same time. The address given in the parameter field of CR is the address of the real part.

VII.1.4 - MR/TDRC/TDRW/IDT Commands

The report issued by the MR/TDRC/TDRW/IDT commands follow the same rules as for CR. The report meaning is :

D7	D6	D5	D4	D3	D2	D1	D0	COMREP[0]
D15	D14	D13	D12	D11	D10	D9	D8	COMREP[1]

D0..D15 is the 16-bit value required by the MR/TDRC command.

In the case of IDT, D15..D12 contains the product identification (2 for ST75C52), D11..D8 contains the hardware revision identification and D7..D0 contains the software revision identification.

VII.2 - Modem Status

VII.2.1 - Modem Status Description

The Status of ST75C52 is divided into 4 fields :

- The error status byte SYSERR that provides information about error. This status can trigger an IT0 interrupt,
- The general status byte STATUS[0] and STATUS[1] that contains all the modem signals. These status bytes can trigger an IT4 interrupt,
- The quality status STAQUA, that contains the quality of the received transmission,
- The optional status bytes STAOP[0], STAOP[1] and STAOP[2], that contains additional information regarding the ST75C52 operating mode. This default information can be changed to monitor any internal variables using the DOSR command.

All these informations are updated on a Baud basis :

Mode	Baud Rate [2] (Hz)	CLK (Hz)
Tone, DTMF, Voice	2400	9600
Bell 103 (full duplex)	2400	9600
V.21 (full duplex)	2400	9600
V.23 (full duplex)	2400	9600
V.27ter 2400bps	1200	2400
V.27ter 4800bps	1600 [1]	4800
V.29	2400	9600/7200/4800
V.17	2400	14400/12000/9600/7200
V.33	2400	14400/12000
V.21 channel 2	2400	300

Notes : 1. The tone detectors outputs are update 800 times by second.

2. This baud rate defines also, the maximum command rate. Each baud time the ST75C52 looks at the COMSYS location (addesss $00) to see if a command have been sent by the host processor. If the content of this location is different from zero the ST75C52 execute the command.

Starting at the adddress $08 the status area have the following format :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$08	SYSERR	ERR_RTK	-	-	ERR_IPRM	ERR_IOCD	-	ERR_RX	ERR_TX
$09	STATUS0	STA_109F	STA_CPT10	STA_CPT1	STA_CPT0	STA_RING	STA_106	STA_107	STA_109
$0A	STATUS1	STA_DTMF	STA_FLAG	-	STA_HR	STA_AT	STA_CCITT	-	STA_H
$0B	STAQUA	-	Quality						
$0C	STAOP0	Depend on operating mode (see below)							
$0D	STAOP1								
$0E	STAOP2								

VII.2.2 - Error Status

The error status changes each time an error occurs. When the ST75C52 signals an error by setting one of the SYSERR bit, it generates an interrupt IT0. These bits can only be cleared by the host controler using the CSE command.

The meaning of the different bits of the SYSERR byte is discribed below :

SYSERR		
Field	**Pos.**	**Meaning when set**
ERR_TX	0	Transmit buffer underflow. Loss of synchronisation between the host and ST75C52 transmit data buffer managment.
ERR_RX	1	Receive buffer overflow. Loss of synchronisation between the host and ST75C52 receive data buffer managment.
ERR_IOCD	3	Incorrect CCI command
ERR_IPRM	4	Incorrect parameter for the CCI command
ERR_RTK	7	Real time kernel error. ST75C52 not able to perform all its tasks within the baud period (transmit or receive samples lost).

VII.2.3 - Modem General Status

The modem general status word is composed of two bytes STATUS[0] and STATUS[1]. Any bit change can generate an IT4 interrupt. Using the DSIT command allows the selection of the corresponding bit that will generate an interrupt each time they will change. The default pattern is $3F for STATUS[0] and $FF for STATUS[1].

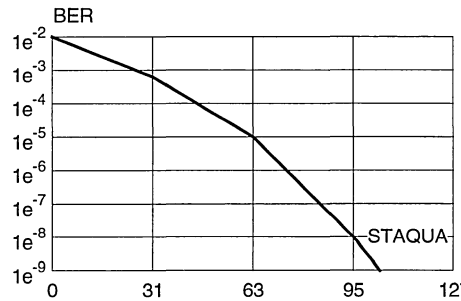
The different bits have the following meaning :

STATUS[0]		
Field	**Pos.**	**Meaning when set**
STA_109	0	CCITT circuit 109 (carrier detect). Indicates that valid data are received. When 0 the output data RxD are clamped to constant mark. Valid only in modem mode.
STA_107	1	CCITT circuit 107 (data set ready). Valid only in modem mode.
STA_106	2	CCITT circuit 106 (clear to send). Indicates that the training sequence has been completed and that any data at TxD pin (serial mode) or in the transmit buffer (parallel mode) will be transmitted. valid only in modem mode.
STA_RING	3	Ring detected. A ring signal (from 15Hz to 68Hz) is present at the RING pin. Valid only in tones modes. The precise frequency can be read in the optional status byte STAOP2. The detection time is 1 period of the ring signal. The detection lost time in 20ms after the last transition on the ring signal.
STA_CPT0	4	Call progress tone detector #0. Low pass filter 650Hz. Valid only in tones modes.
STA_CPT1	5	Call progress tone detector #1. High pass filter 600Hz. Valid only in tones modes.
STA_CPT10	6	Signal in filter #0 is highter than #1. Valid only in tones modes.
STA_109F	7	Fast Carrier Detect. Valid only in modem mode.

STATUS[1]		
Field	**Pos.**	**Meaning**
STA_H	0	Transmit synchronisation in progress. Valid only in modem mode.
STA_CCITT	2	CCITT 2100Hz versus 2225Hz answer tone detect. Valid if STA_AT is set. Valid only in tones modes.
STA_AT	3	Answer tone (either 2100Hz or 2225Hz) detected. Valid only in tones modes.
STA_HR	4	Receive synchronisation in progress. Valid only in modem mode.
STA_FLAG	6	V.21 channel 2 flag detect. Valid only in FAX modem mode and tone mode.
STA_DTMF	7	DTMF digit detect. The digit itself is available in the optional status byte STAOP2. Valid only in DTMF receive mode.

VII.2.4 - Quality Status

The quality byte STAQUA monitors an evaluation of the line quality. It is updated once per baud and its value ranges from 127 (perfect quality) to 0 (terrible quality). This value is automaticaly adjusted according to the current receiving mode. Refer to the following chart to convert the value into its Bit Error Rate equivalence.



75C52-22.EPS

VII.2.5 - Optional Status

According to the operating mode of the ST75C52 the optional status is displaying different informations.

The optional status are automatically reprogrammed after each CONF command with the address of the variables to monitor according with the operating mode selected (CONF_OPER). After the CONF command the user must overwrite this default programming by using the DOSR command.

VII.2.6 - Default Optional Status in Tone Mode

While in tone mode the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	TDT7	TDT6	TDT5	TDT4	TDT3	TDT2	TDT1	TDT0
$0D	STAOP1	TDT15	TDT14	TDT13	TDT12	TDT11	TDT10	TDT9	TDT8
$0E	STAOP2	RING_PERIOD (1)							

Notes : 1. RING_PERIOD is valid when the bit 3 of the STATUS[0] (STA_RING) goes high. This value is updated at each falling edge of the RING signal. The RING_PERIOD value must be divided by 2400 to obtain the period in seconds.

2. TDTx is the output of the tone detector x.

VII.2.7 - Default Optional Status in DTMF Receiver Mode

While in DTMF receiver mode the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	TDT7 (1)	TDT6 (1)	TDT5 (1)	TDT4 (1)	TDT3	TDT2	TDT1	TDT0
$0D	STAOP1	TDT15 (1)	TDT14 (1)	TDT13 (1)	TDT12 (1)	TDT11 (1)	TDT10 (1)	TDT9 (1)	TDT8 (1)
$0E	STAOP2	DTMF_DIGIT (2)							

Notes : 1. These cells are used by the DTMF detector.
2. DTMF_DIGIT is valid when the bit 7 of STATUS[1] (STA_DTMF) goes high. This value remains unchanged until a new DTMF digit is detected.

VII.2.8 - Default Optional Status in Modem Mode

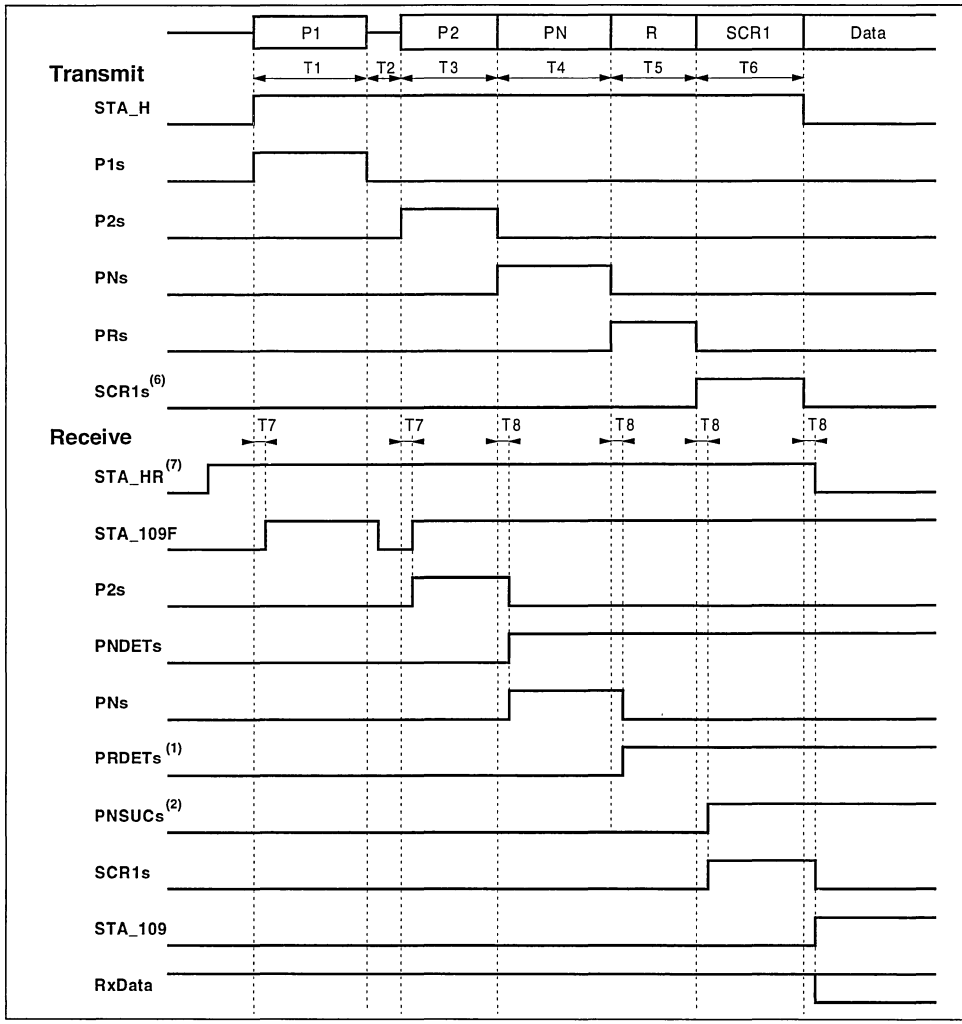
While in modem mode the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	x	x	x	SPEED (2)				SPVAL (1)
$0D	STAOP1	Not used							
$0E	STAOP2	PNSUCs	PRDETs	PNDETs	SCR1s	PRs	PNs	P2s	P1s

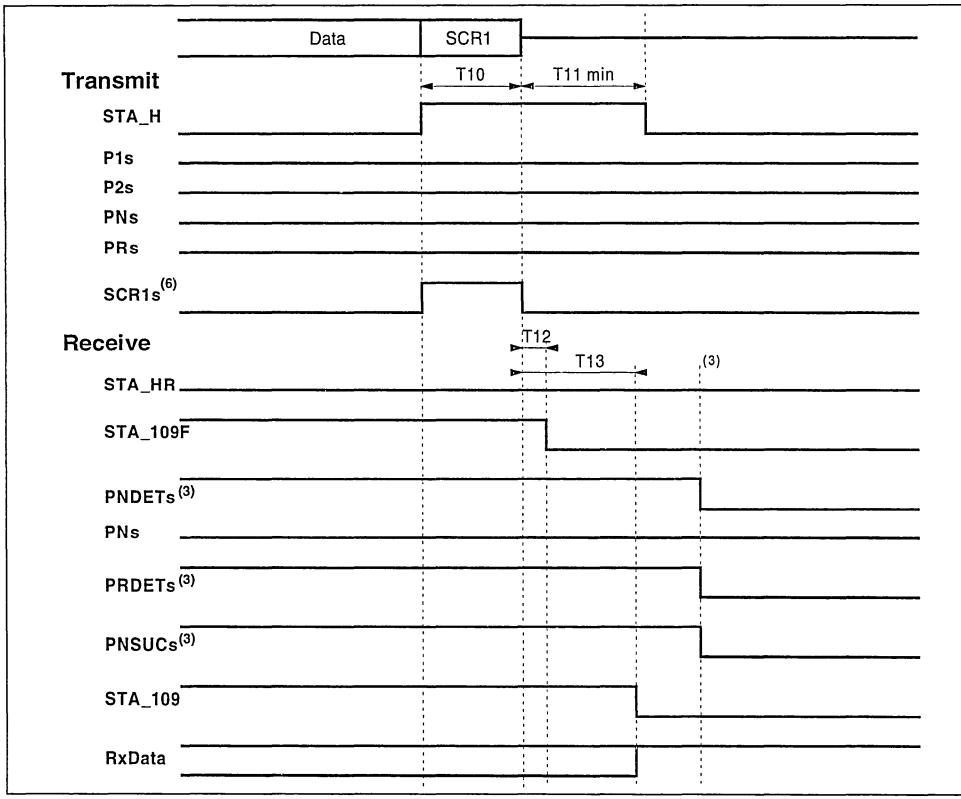
Notes : 1. SPVAL is active in V.33 receiver only at the same time as the rising transition of the SCR1s signal. Went SPVAL is set, it indicates that the SPEED bits contain the data speed information.
2. SPEED is valid in V.33 receiver only. It can have 2 values, after the SCR1s signal goes high : 1000 for 14400bps and 0111 for 12000bps.
3. The STAOP2 bit reflects the progression of the synchronization. The STAOP2 bits have the following meaning :

Name	Position	Description	Tx	Rx
P1s	0	Unmodulated carrier sequence. Optional, used for echo protection.	X	
P2s	1	Continuous 180° phase reversal sequence	X	X
PNs	2	Equalizer trainning sequence	X	X
PRs	3	V.33 and V.17 rate sequence	X	
SCR1s	4	Continuous scrambled 1 sequence	X	X
PNDETs	5	Turned on after PN sequence detection		X
PRDETs	6	Turned on after PR sequence detection (V.33 and V.17 only)		X
PNSUCs	7	Turned on after succesfull training of the receive equalizer. When on at the end of the synchronization, the transmition BER is statisticaly bellow 10ppm.		X

With the following timing :



Mode	T1 (4)	T1p (5)	T2	T3	T4	T5	T6	T7	T8	Unit
V.17	192	30	22	107	1240	27	20	5	7	ms
V.17 short	192	30	22	107	16	0	20	5	7	ms
V.29	192	30	22	53	160	0	20	5	7	ms
V.29 short	192	30	22	41	26	0	8	5	7	ms
V.27 4800	192	30	22	31	670	0	5	5	7	ms
V.27 4800 short	192	30	22	9	36	0	5	5	7	ms
V.27 2400	192	30	22	42	895	0	7	6	7	ms
V.27 2400 short	192	30	22	12	48	0	7	6	7	ms



Mode	T10	T11	T12	T13	Unit
V.17	13	20	8	25	ms
V.17 short	13	20	8	25	ms
V.29	13	20	8	25	ms
V.29 short	13	20	8	25	ms
V.27 4800	20	30	8	25	ms
V.27 4800 short	20	30	8	25	ms
V.27 2400	27	40	8	25	ms
V.27 2400 short	27	40	8	25	ms

Notes : 1. In the case of V.29 or V.27, PRs and PRDETs bits are not active.
2. PNSUCs indicates the quality of the Rx signal that will give a ber of approximation of $1e^{-5}$.
3. After sending the command SYNC0, all bits are reset.
4. When using long echo protection tone, otherwise 0.
5. When using short echo protection tone, otherwise 0.
6. STA-106 is set at the end of T6 and reset at the beginning of T10.
7. After sending the command SYNC1, this bit is set.

VIII - TONE DETECTORS

VIII.1 - Overview

The general purpose TS75C52 tone detectors block is a powerful module that covers a lot of applications :

- call progress tone detection, fully programmable for all countries,
- DTMF detection,
- FAX, voice, data automatic detection,
- call waiting detection, while in voice or data mode.

VIII.2 - Description

The tone detector block is a set of 16 identical Cells. Each cell is composed of a Double Biquadratic Filter, a Power estimator section, a Static level and a Level comparator.

Each Biquadratic Filter, Power Estimator and Static Level can be programmed using a complete set of Commands (**TDRC**, **TDRW**, **TDWC**, **TDWW**, **TDZ**).

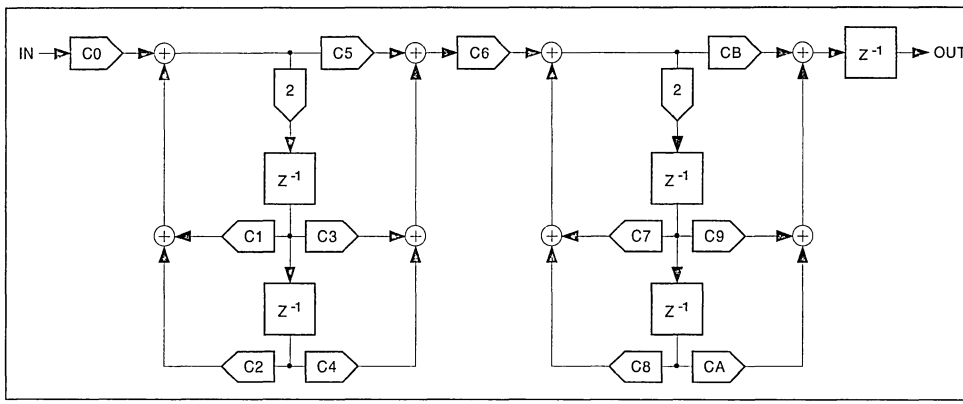
The wiring between the different Cells can be defined by the user, using the associatedCommand allowing a wide range of applications.

The 16 Comparator Outputs give, on a baud basis, the information into two 8 bits words **TONEDET0** (for cells number 0 to 7) and **TONEDET1** (for cells number 8 to F). These TONEDET variables can be accessed using a **MR** command or, more easily, monitored on a baud basis using the **DOSR** command.

VIII.2.1 - Biquadratic Filters

Each Biquadratic Filter is a double regular section that can perform any Transfer function with 4 Poles and 4 Zeros. This routine is run on a sample basis.

Figure 2 : Biquadratic IIR Filter



The corresponding transfer function is :

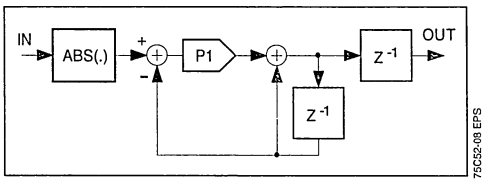
$$\frac{Out}{Input} = C0 \cdot \frac{C5 + 2 \cdot C3 \cdot z^{-1} + 2 \cdot C4 \cdot z^{-2}}{1 - 2 \cdot C1 \cdot z^{-1} - 2 \cdot C2 \cdot z^{-2}} \cdot C6 \cdot \frac{CB + 2 \cdot C9 \cdot z^{-1} + 2\ CA \cdot z^{-2}}{1 - 2 \cdot C7 \cdot z^{-1} - 2 \cdot C8 \cdot z^{-2}} \cdot z^{-1}$$

Note : All coefficients are coded on 16 bits 2's complement in the range +1, -1 (Q15). To avoid the possibility of overflow the user must check that the internal node must not be higher that 0.5 (in Q15 representation).

VIII.2.2 - Power Estimation

The Power estimation Cell is needed to measure the amplitude of the different tones. It is run on a sample basis.

Figure 3 : Power Estimator



The corresponding transfer function is :

$$Out = |\,Input\,| \cdot z^{-1} \cdot \frac{P1}{1-(1-P1)\cdot z^{-1}}$$

VIII.2.3 - Static Level

A single Threshold level is associated with each Cell. It can be use to compare the output of a Power Estimation with an Absolute Value.

VIII.2.4 - Comparator

The Comparator computes, on a baud basis, the difference of the signal on its Positive and Negative Inputs. If the result is Higher that zero it sets the corresponding bit into the TONEDET[0..1] word; if not it clear this bit.

VIII.2.5 - Wiring

The user must specify the connection (wiring) between the input/output of the Filter, the input/output of the Power estimator, the output of the static levels and the two inputs of the Comparators.

The output signals have an absolute address:

Node Address		
Signal Name	**Address**	**Description**
Ground	00	Signal always equal to 0000
RxSig	01	Receive signal from the Analog front end
RxSig2	02	Receive signal multiplied by 2
RxSig4	03	Receive signal multiplied by 4
	04..0F	Reserved
Filter[0..F]	10..1F	Biquadratic Filter Outputs
Power[0..F]	20..2F	Power Estimator Outputs
Level[0..F]	30..3F	Static Levels

The user will specify the inputs of the filters, Power and Comparator. At least one input must come from the RxSig (node 01, 02 or 03). It is mandatory to connect all unused cell inputs to the Ground signal (node 00).

Figure 4 : Tone Detector Wiring Address (first half)

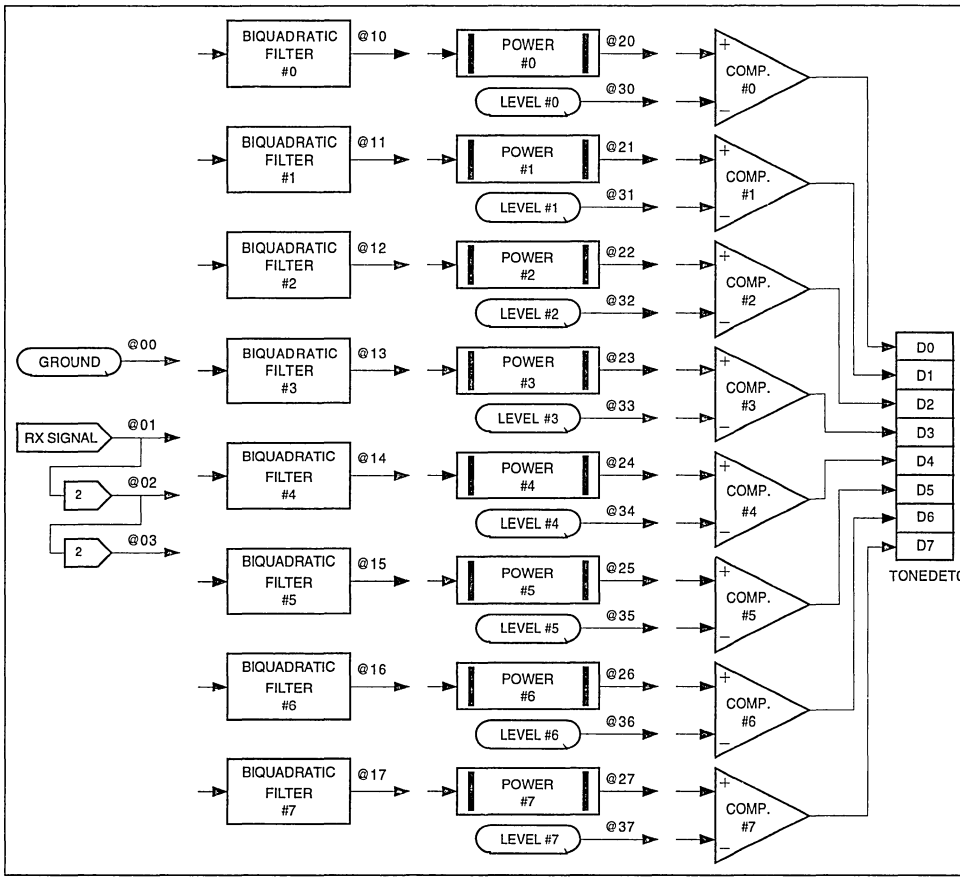
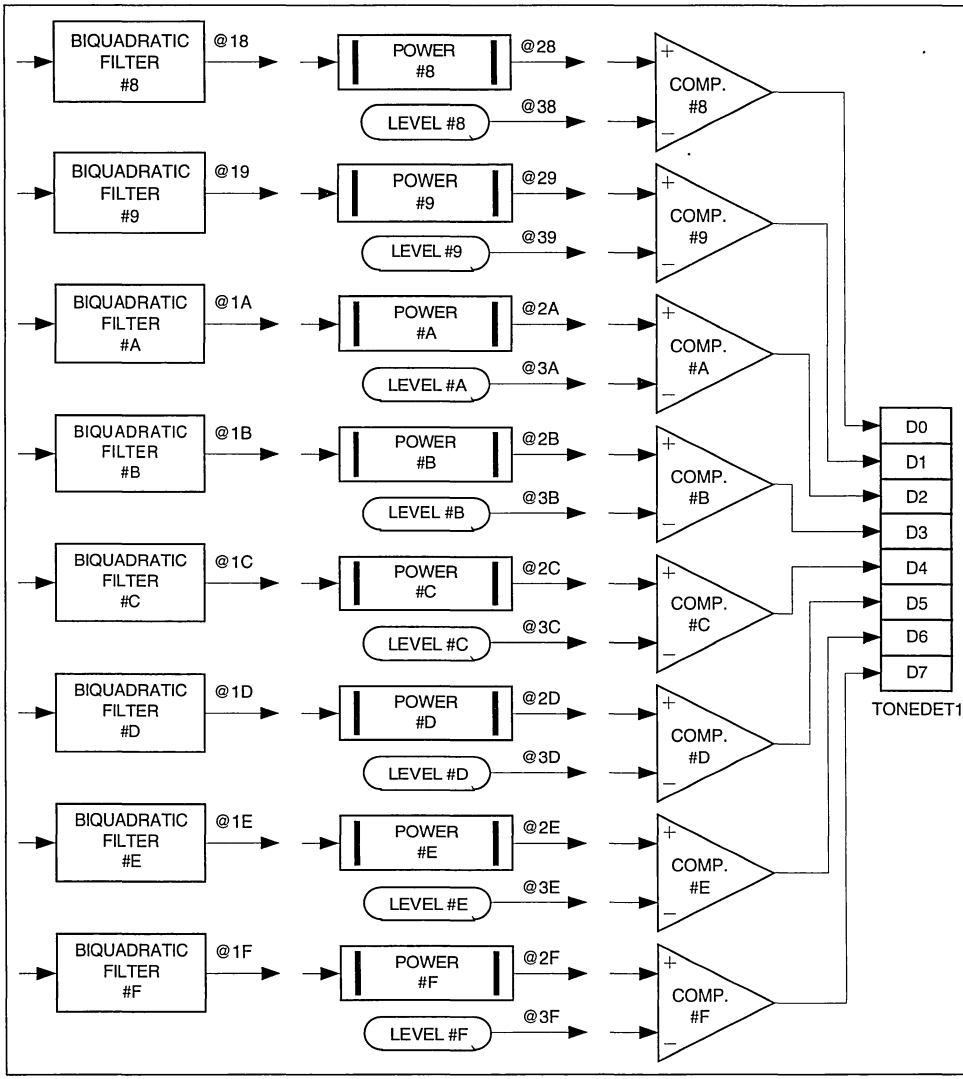


Figure 5 : Tone Detector Wiring Address (second half)

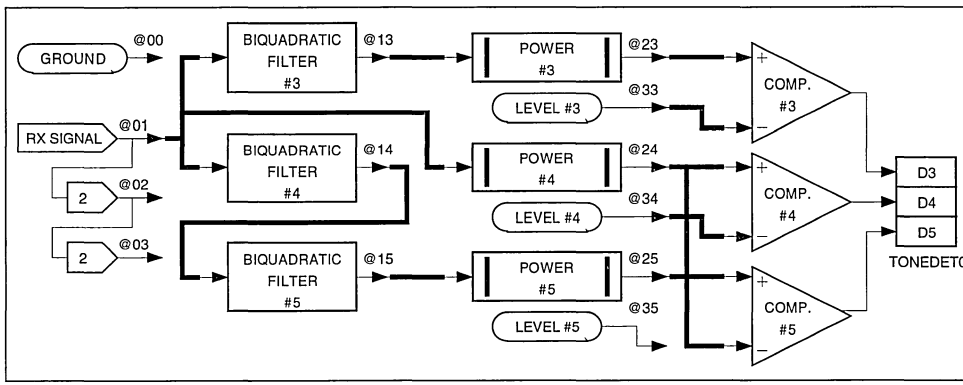


VIII.3 - Example

Hereunder is an example of programming a single Tone detection (using Cell #3) and a complex differential tone detection (using Cell #4 and #5).
Bit 3 of the TONEDET variable will be triggered each time the energy of that filtered signal is higher than Static Level number 3.

Bit 4 of the TONEDET variable will be on each time a receive signal has an energy higher than the Static Level number 4. Bit 5 will be on only when the Filtered (Filter section 4 and 5) received signal higher than the energy of the wide-band signal number 4 ; this prevents triggering on noise.

Figure 6 : Wiring Example



Program Cell #3 :

TDWW	**03**	**00**	**13**	**01**

Connect Received signal to Filter and Filter to Energy.

TDWW	**03**	**01**	**33**	**23**

Connect Level to Comparator Neg Input and Energy to Pos Input.

Program Cell #4 and #5 :

TDWW	**04**	**00**	**01**	**01**

Connect Received Signal to Filter and Energy.

TDWW	**04**	**01**	**34**	**24**

Connect Level to Comparator Neg Input and Energy to Pos Input.

TDWW	**05**	**00**	**15**	**14**

Connect Filter#4 Output to Filter and Filter to Energy.

TDWW	**05**	**01**	**24**	**25**

Connect Wide-band Energy to Neg Input and Energy to Pos Input.

IX - BUFFER OPERATIONS

IX.1 - Introduction

This appendix is dedicated to buffer operation, either the data buffers used in data exchanges or in particular Modes (like Voice).

The first part is oriented towards a functional description of the buffer operation, while the second section is more oriented towards the management of the buffers.

IX.2 - Receive Operations Overview

Figure 7 describes the receive data flow.

The ST75C52 can handle the following types of format for the data :

- parallel synchronous mode : 8-bit words are synchronously available in the receive buffers. The buffer status holds the number of valid bytes received,
- parallel HDLC framing mode : 8-bit data is available in the receive buffers. Framing information (like flags, CRC, additional "0") is interpreted by the ST75C52 and reported when necessary in the receive buffer status (CRC error, aborted frame, framing error, etc). This feature greatly eases the implementation of protocols as well as FAX data management.

Each time the receive deframer has filled up a new buffer, it sets the corresponding flag with the proper status then generates the IT3 interrupt. The availability of the buffers is tested just before starting to fill them. This further means that the host must not perform any buffer operation on the data part while the status remains 0.

IX.3 - Transmit Operations Overview

Figure 8 describes the transmit data flow. The following modes are available :

- parallel synchronous mode : 8-bit words are synchronously read from the transmit buffers. The transmit status buffer holds the number of valid bytes to be transmitted (up to 8 per buffer),
- parallel HDLC framing mode : 8-bit data is received from the transmit buffers. Framing information (frame open, frame close, frame abort, number of byte per buffer) is carried by the transmit buffer status and processed by the ST75C52. CRC, padding and other operations are automatically handled by the ST75C52.

Each time the transmit framer has emptied a buffer, the IT2 interrupt is raised.

Figure 7 : Rx Buffer Schematics

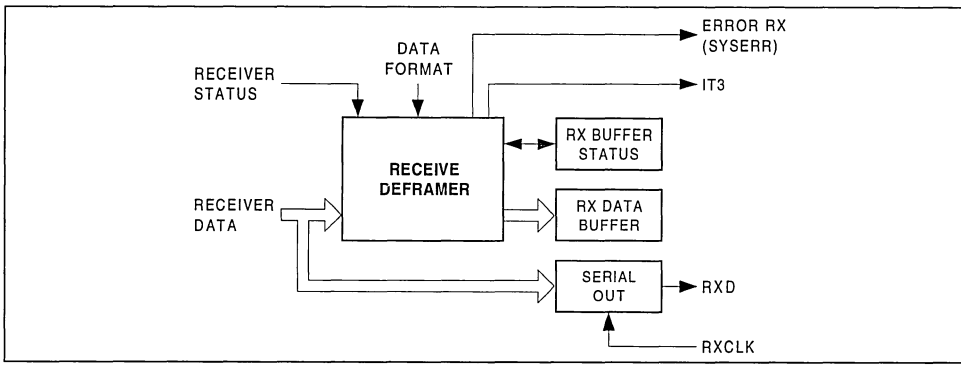
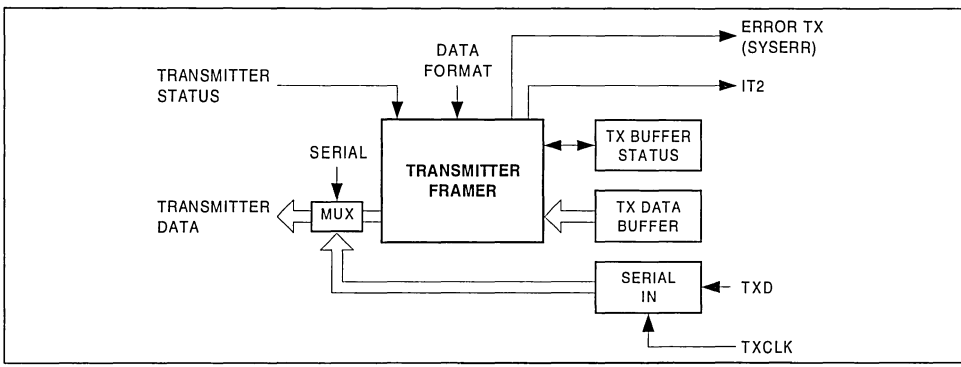


Figure 8 : Tx Buffer Schematics



IX.4 - Buffer Status and Format Description

The following section describes the meaning and use of the buffer status words.

IX.4.1 - Transmit Buffer

The transmit buffer status words are DTTBS0 and DTTBS1 (see the **Host Interface Summary** section in the main document) and are more likely to be seen as control words. These words must be set by the host and are reset by the ST75C52. The data buffer exchanges are synchronized through these status words, (see Buffer Status and format description) an improper setting will trigger the error Err_Tx in the error status SYSERR. A value of 0 for DTTBS0 or DTTBS1 means that the corresponding buffers are empty : this value is written by the ST75C52. The unused bits of DTTBSx must be set to 0 by the host.

In FSK Mode, when working in the parallel data mode, the transmitter expands each bit to the nominal baud time (1200Hz/300Hz/75Hz).

IX.4.2 - Synchronous Mode

Field	Pos.	Val.	Description
BUFF_LENG	3..0	1..8	Number of valid bytes in the buffer

IX.4.3 - HDLC Framing Mode

Field	Pos.	Val.	Description
BUFF_LENG	3..0	1..8	Number of valid bytes in the buffer
BUFF_SFRM	4	0 1	Data stream Start of frame
BUFF_EFRM	5	0 1	Data stream End of frame
BUFF_FRAB	6	0 1	Normal process Abort frame (no data in buffer)

IX.5 Receive Buffer

The receive buffer status words are DTRBS0 and DTRBS1 (see the **Host Interface Summary** section in the main document). These flags are set by the ST75C52 and must be reset by the host. The data buffer exchanges are synchronized through these status words, an improper resetting will trigger the error Err_Rx in the error status SYSERR. A value of 0 for DTRBS0 or DTRBS1 means that the corresponding buffers are empty : this value must be written by the host.

In FSK or V.21 Channel 2 Mode, when working in the parallel data mode, the receiver extract each bit using the nominal baud rate (1200Hz/300Hz/75Hz).

IX.5.1 - Synchronous Mode

Field	Pos.	Val.	Description
BUFF_LENG	3..0	1..8	Number of valid bytes in the buffer

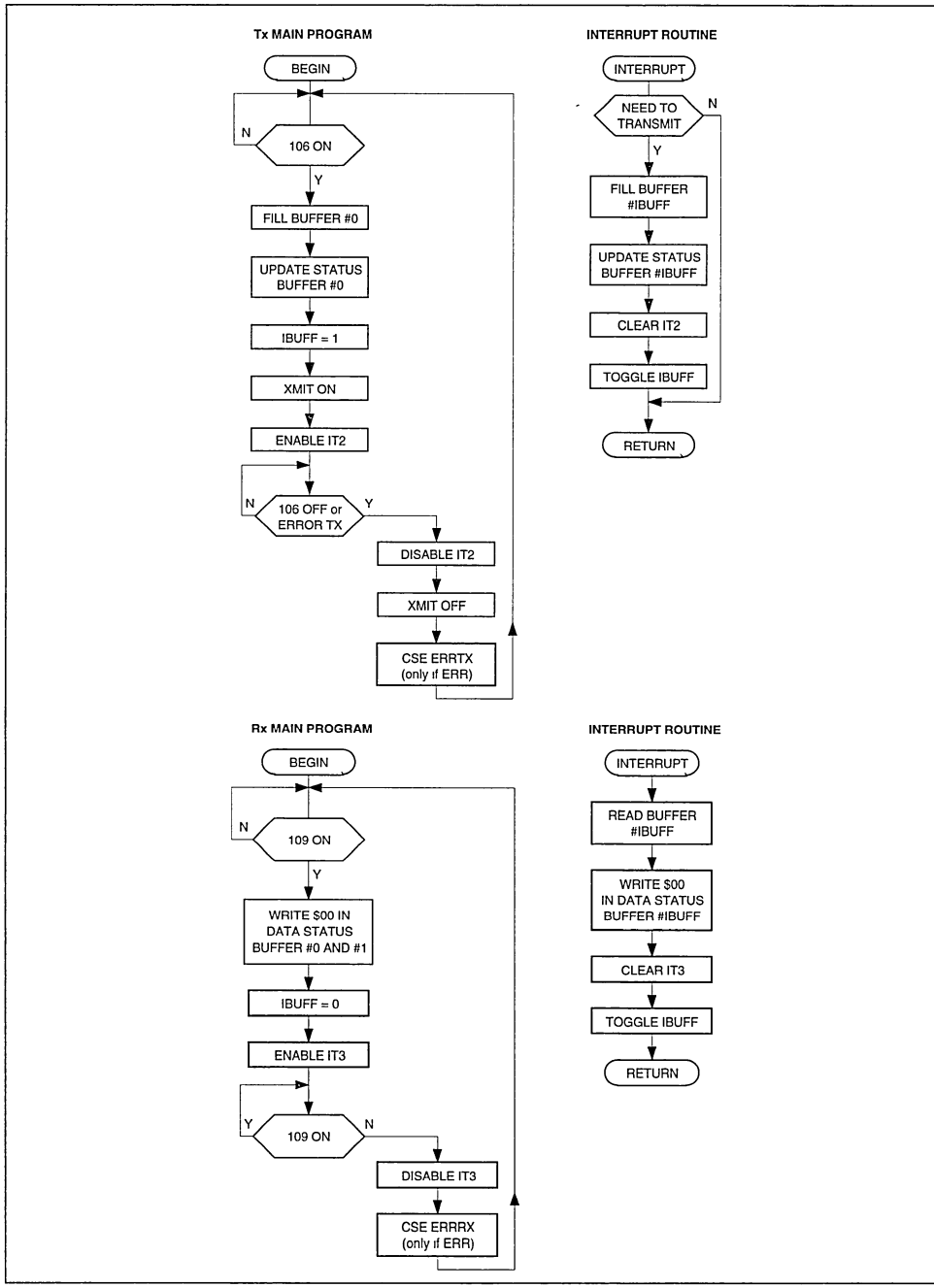
IX.5.2 - HDLC Framing Mode

Field	Pos.	Val.	Description
BUFF_LENG	3..0	1..8	Number of valid bytes in the buffer
BUFF_ERRS	5..4	00 01 10 11	No error CRC error Non byte-aligned frame Aborted frame
BUFF_SFRM	6	0 1	Data stream Start of frame
BUFF_EFRM	7	0 1	Data stream End of frame

IX.6 - Data Buffer Management

Figure 9 shows the general flow chart for transmit data buffer management. In the transmit path, the data buffer exchanges should always begin with the filling of buffer 0, then with the update of the buffer 0 status word. The initiation of the data exchanges is initiated then with the **XMIT** command.

Figure 9 : Buffer Operations Synchronization



75C52-27 EPS / 75C52-14 EPS

X - DEFAULT CALL PROGRESS TONE DETECTORS

Figure 10 : Call Progress Tone Detector Band 1

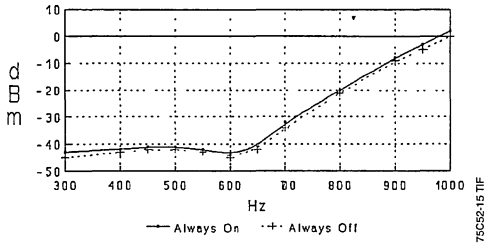
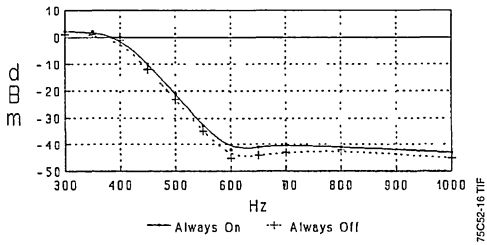


Figure 11 : Call Progress Tone Detector Band 2



XI - DEFAULT ANSWER TONE DETECTORS

Figure 12 : 2100Hz Answer Tone Detector

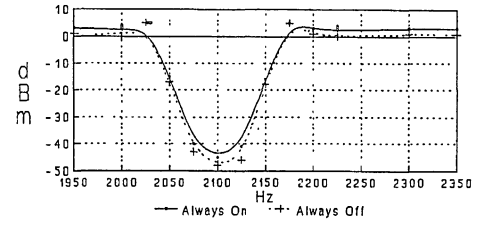
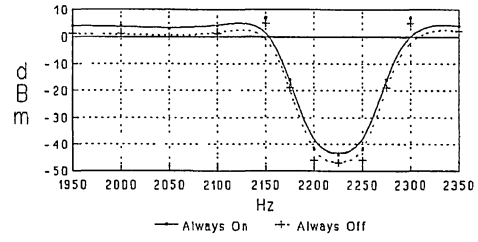


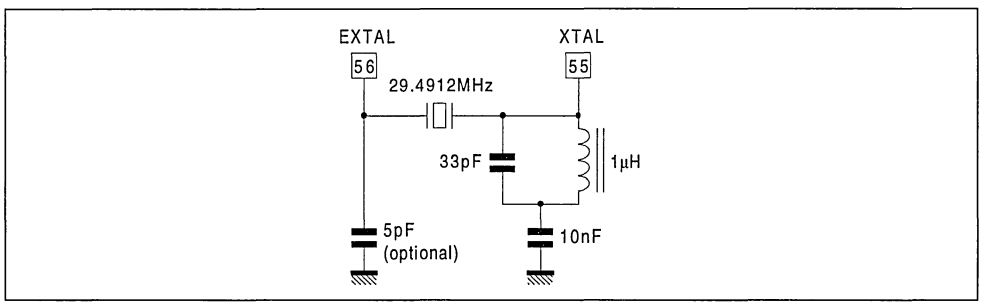
Figure 13 : 2225Hz Answer Tone Detector



XII - ELECTRICAL SCHEMATICS

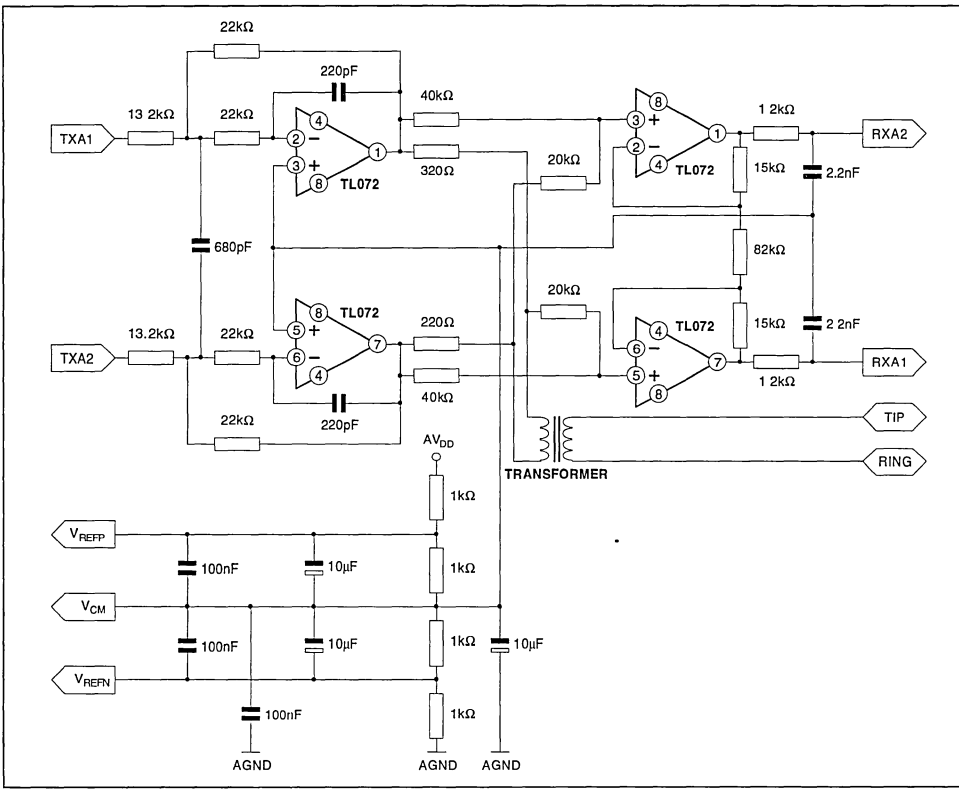
Oscillator

When using a third harmonic crystal oscillator in series resonance mode ($R_S < 40\Omega$, $C_0 = 6pF$, $P_e = 0.1mW$), we recommend the following schematic :



XII - ELECTRICAL SCHEMATICS (continued)

Figure 14



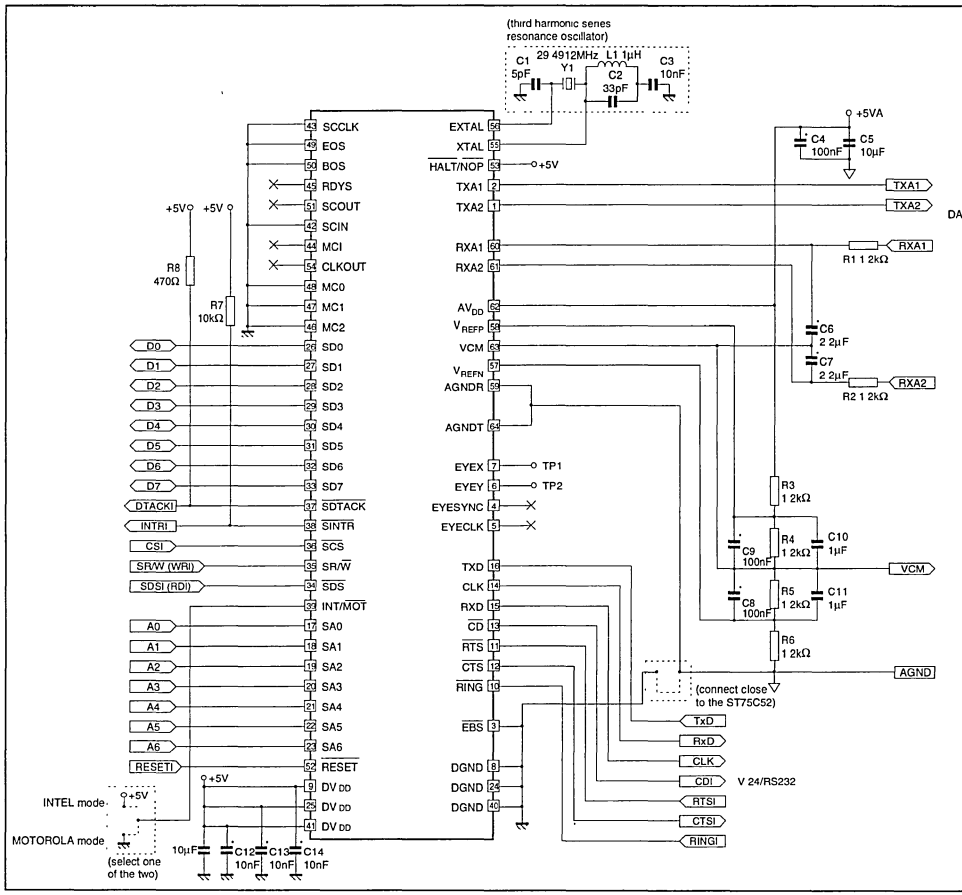
XIII - PCB DESIGN GUIDELINES

Performances of the FAX modem depends on the ST75C52 intrinsic performances and on the proper PC board layout. All aspects of the proper engineering practices, for PC board design, are beyond the scope of this paragraph.

We recommend the following points :

- in a 4-layer PC board :
  Separated digital ground and analog ground, connected together at one point, as close as possible to the ST75C52,
- in a 2-layer PC board :
  Provide a ground grid in all space around and under components on both sides of the band and connect to avoid small islands,
- both AGNDR and AGNDT must be connected with very low impedance to a single point, (see Chapter I.7, Power Supply),
- the two 2.2nF capacitors connected to the RXA1 and RXA2 Pins must be as close as possible to them,
- the two 100nF capacitors connected to the V_{REFP} and V_{REFN} pins must be as close as possible to them,
- analog and digital supplies must be connected together, at a single point, as close as possible to the chip (see Chapter I.7, Power Supply).

TYPICAL APPLICATION



Notes : All capacitor with a "*" must be implanted close to the ST75C52 pin.
All signal name ending with a "1" are active low.
R3, R4, R5, R6 are needed if the hybrid will sink a current on V_{CM}.

SGS-THOMSON MICROELECTRONICS

ST75C520

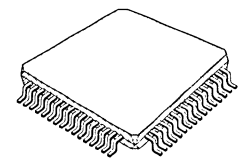
HIGH SPEED FAX MODEM DATA PUMP

PRELIMINARY DATA

- ITU-T V.17, V.29, V.27ter, V.21 WITH FAX SUPPORT
- ITU-T V.23, V.21, BELL 103
- V.17, V.29 (T104), V.27ter SHORT TRAINS
- V.33 HALF-DUPLEX
- 1800Hz OR 1700Hz CARRIER
- SINGLE CHIP COMPLETE DATA PUMP
- SINGLE 5V POWER SUPPLY :
  - TYPICAL ACTIVE POWER CONSUMPTION : 375mW
  - LOW POWER MODE (typ. 5mW)
- EXTENDED MODES OF OPERATIONS :
  - FULL IMPLEMENTATION OF THE V.17, V.33, V.29 AND V.27ter HANDSHAKES
  - AUTODIAL AND AUTOANSWER CAPABILITY
  - PROGRAMMABLE TONE DETECTION AND FSK V.21 FLAG PATTERN DETECTION DURING HIGH SPEED RECEPTION
  - PROGRAMMABLE CALL PROGRESS AND CALL WAITING TONE DETECTORS INCLUDING DTMF
  - PROGRAMMABLE CLASS™ DETECTION CAPABILITY
  - WIDE DYNAMIC RANGE (>48dB)
  - A-LAW VOICE PCM MODE
- VERSATILE INTERFACES :
  - PARALLEL 64 x 8-BIT DUAL PORT RAM
  - SYNCHRONOUS/HDLC PARALLEL DATA HANDLING
  - HDLC FRAMING SUPPORT
  - V.24 INTERFACE
  - FULL OPERATING STATUS REAL TIME MONITORING
  - FULL DIAGNOSTIC CAPABILITY
  - DUAL 8-BIT DAC FOR CONSTELLATION DISPLAY

DESCRIPTION

The SGS-THOMSON Microelectronics ST75C520 chip is a highly integrated modem engine, which can operate with all currently used FAX group III standards up to 14400bps. Full V.21, V.23 and Bell 103 full duplex modem standards are implemented.



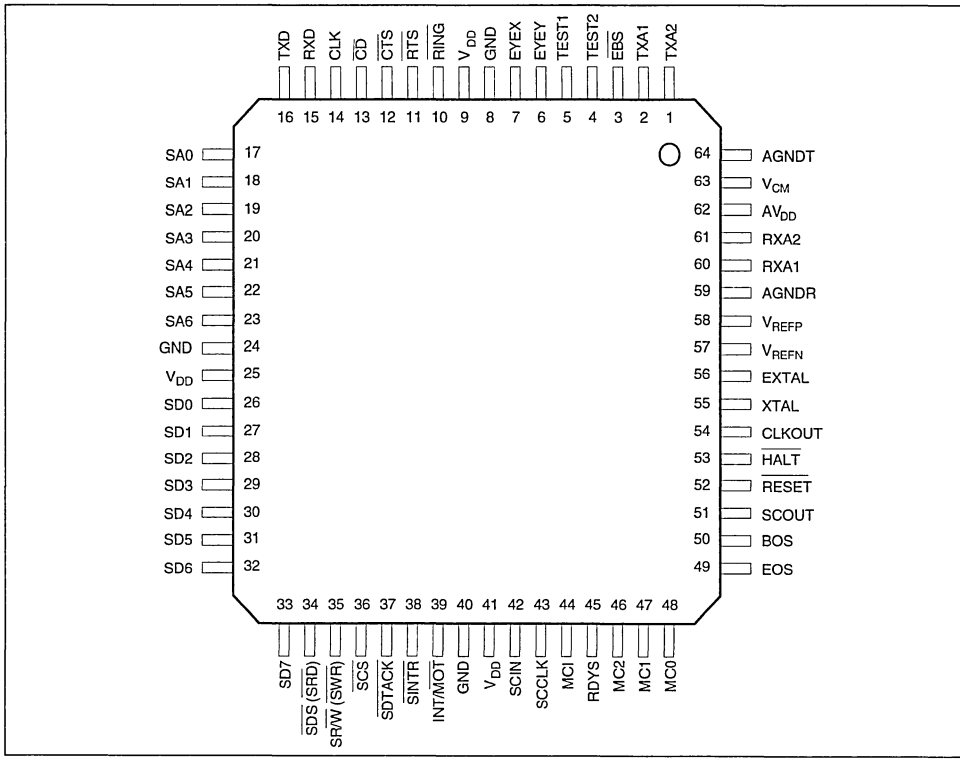
PQFP64
(Plastic Quad Flat Pack)

ORDER CODE : ST75C520 PQFP

CONTENTS

I - PIN DESCRIPTION

I.1 - Pin Connections



75C52001 EPS

I.2 - Host Interface

The exchanges with the control processor proceed through a 64 Bytes DUAL port RAM shared between the ST75C520 and the Host. The signals associated with this interface are :

Pin Name	Type	Description
SD0..SD7	I/O	System Data Bus. 8-bit data bus used for asynchronous exchanges between the ST75C520 and the Host through the dual port RAM. High impedance when exchanges are not active.
SA0..SA6	I	System Address Bus. 7-bit address bus for dual port RAM.
$\overline{SDS}$ ($\overline{SRD}$)	I	System Data Strobe. Active low. Synchronizes all the exchanges. In Motorola mode initiates the exchange, active low. In Intel mode initiates a read exchange, active low.
SR/$\overline{W}$ ($\overline{SWR}$)	I	System Read/Write. In Motorola mode defines the type of exchange read/write. In Intel mode initiates a write exchange, active low.
$\overline{SCS}$	I	System Chip Select. Active low.
$\overline{SDTACK}$	OD	System Bus Data Acknowledge. Active low. Open drain.
$\overline{SINTR}$	OD	System Interrupt Request. Active low. This signal is asserted by the ST75C520 and negated by the host. Open drain.
$\overline{RESET}$	I	Reset. Active low.
$\overline{RING}$	I	Ring Detect Signal. Active low.
INT/$\overline{MOT}$	I	Select Intel/Motorola Interface.

I.3 - Analog Interface

Pin Name	Type	Description
TXA1	O	Transmit Analog Output 1
TXA2	O	Transmit Analog Output 2. Outputs TXA1 and TXA2 provide analog signals with maximum peak to peak amplitude 2 x V_{REF}, and must be followed by an external continous-time two pole smoothing filter (where $V_{REF} = V_{REFP} - V_{REFN}$).
RXA1	I	Receive Analog Input 1
RXA2	I	Receive Analog Input 2. The analog differential input peak to peak signal must be less than 2 x V_{REF}. It must be preceded by an external continous-time single pole anti-aliasing filter. This filter must be as close as possible to the RXA1 and RXA2 Pins (where $V_{REF} = V_{REFP} - V_{REFN}$).
V_{CM}	I/O	Analog Common Voltage (nominal +2.5V). This input must be decoupled with respect to AGND.
V_{REFN}	I	Analog Negative Reference (nominal V_{CM} - 1.25V). This input must be decoupled with respect to V_{CM}.
V_{REFP}	I	Analog Positive Reference (nominal V_{CM}+1.25V). This input must be decoupled with respect to V_{CM}.

I.4 - V.24 Interface

Pin Name	Type	Description
$\overline{RTS}$	I	Request to Send. Active low.
CLK	O	Data Bit Clock. Falling edge coïncides with DATA change.
$\overline{CTS}$	O	Clear to Send. Active low.
RxD	O	Receive Data
TxD	I	Transmit Data sampled with rising edge of CLK
$\overline{CD}$	O	Carrier Detect. Active low.

I.5 - Miscellaneous

Pin Name	Type	Description
XTAL	O	Internal Oscillator Output. Left open if not used.
EXTAL	I	Internal Oscillator Input, or External Clock
EYEX	O	Constellation X analog coordinate
EYEY	O	Constellation Y analog coordinate
TEST1		To be left open
TEST2		To be left open

Note : The nominal external clock frequency of the ST75C520 is 29.4912MHz with a precision better than $\pm 5.10^{-5}$

I.6 - Boundary Scan Interface

A set of 13 signals are dedicated for Testing the ST75C520 Component. These signals can be used in a development phase, associated with the SGS-THOMSON ST18932 Boundary Scan Development Tools, to Debug the application Hardware and Software. If not used all input signals must be grounded and all output signals left open.

Pin Name	Type	Description
SCIN	I	Scan Data Input
SCCLK	I	Scan Clock
SCOUT	O	Scan Data Output
BOS	I	Begin of Scan Control
EOS	I	End of Scan
MC0..MC2	I	Mode Control
$\overline{HALT}$	I	Stop ST75C520 Execution
MCI	O	Multicycle Instruction
RDYS	O	Ready to Scan Flag
$\overline{EBS}$	I	Enable Boundary Scan. Active low (must be set low in normal mode).
CLKOUT	O	Internal ST75C520 Clock (XTAL frequency divided by 2)

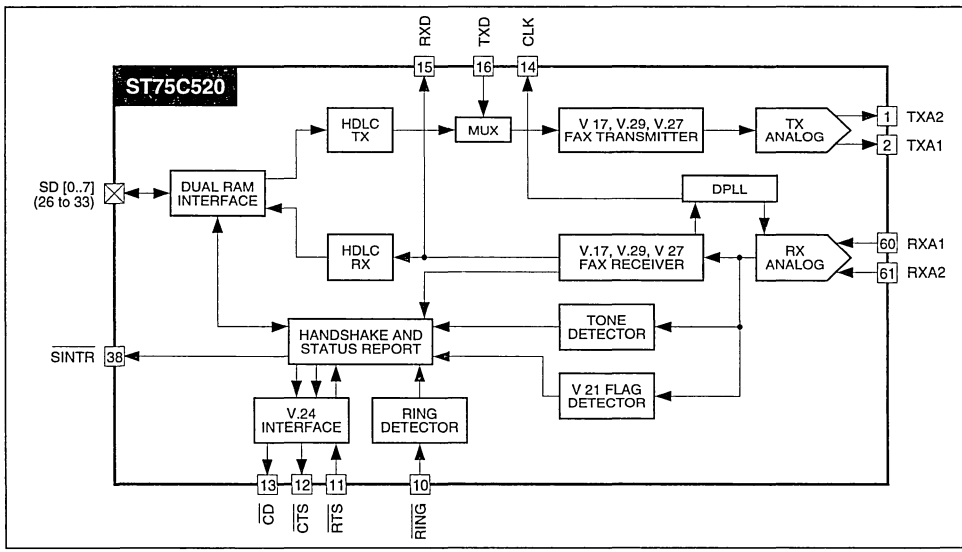
I.7 - Power Supply

Symbol	Parameter
V_{DD}	Digital +5V (Pin 9, 25, 41). To be connected to AV_{DD} (see below).
GND	Digital Ground (Pin 8, 24, 40). To be connected to AGNDT and AGNDR (see below).
AV_{DD}	Analog +5V (Pin 62). To be connected to V_{DD} (see below).
AGNDT	Analog Transmit Ground (Pin 64). To be connected to GND (see below).
AGNDR	Analog Receive Ground (Pin 59). To be connected to GND (see below).

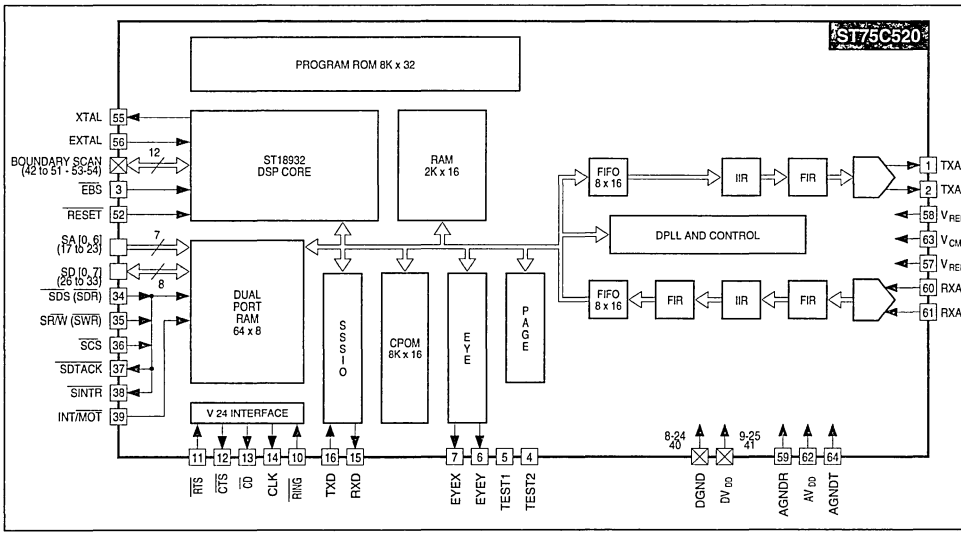
AGNDT and AGNDR must be connected together as close as possible to the chip.
GND and AGNDR board plans should be separated, then connected together as close as possible to the chip, at a single point. Similarly V_{DD} and AV_{DD} must ne connected as close as possible to the chip, at a single point.

II - BLOCK DIAGRAMS

II.1 - Functional Block Diagram



II.2 - Hardware Block Diagram



III - ELECTRICAL SPECIFICATIONS

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical value are given for V_{DD} = +5V and t_{amb} = 25°C.

III.1 - Maximum Ratings (referenced to GND)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3 to 7.0	V
V_I, V_{IN}	Digital or Analog Input Voltage	-0.3 to (V_{DD} + 0.3)	V
I_I, I_{IN}	Digital or Analog Input Current	± 1	mA
I_O	Digital Output Current	± 20	mA
I_{OUT}	Analog Output Current	± 10	mA
T_{oper}	Operating Temperature	0, + 70	°C
T_{stg}	Storage Temperature (plastic)	- 40, + 125	°C
P_{tot}	Maximum Power Dissipation	1000	mW

Stresses above those hereby listed may cause damage to the device. The ratings are stress related only and functional operation of the device at conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

III.2 - DC Characteristics

V_{DD} = 5.0V ± 5%, GND = 0V, T_{amb} = 0 to 70°C (unless otherwise specified).

III.2.1 - Power Supply and Common Mode Voltage

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DD}	Supply Current (internal oscillator)		75	100	mA
I_{DD-lp}	Supply Current in Low Power Mode		1		mA
V_{CM}	Common Mode Voltage	V_{DD}/2 -5%	V_{DD}/2	V_{DD}/2 + 5%	V

III.2.2 - Digital Interface

All digital pins except XTAL Pins.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage	-0.3		0.8	V
V_{IH}	High Level Input Voltage	2.2			V
I_I	Input Current $V_I = V_{DD}$ or V_I = GND	-10	0	+10	µA
V_{OH}	High Level Output Voltage (I_{load} = 2mA)	2.4			V
V_{OL}	Low Level Output Voltage (I_{load} = 2mA)			0.4	V
I_{OZ}	Three State Input Leakage Current (GND < V_O < V_{DD})	-50	0	50	µA
C_{IN}	Input Capacitance		5		pF

Crystal oscillator interface (XTAL, EXTAL).

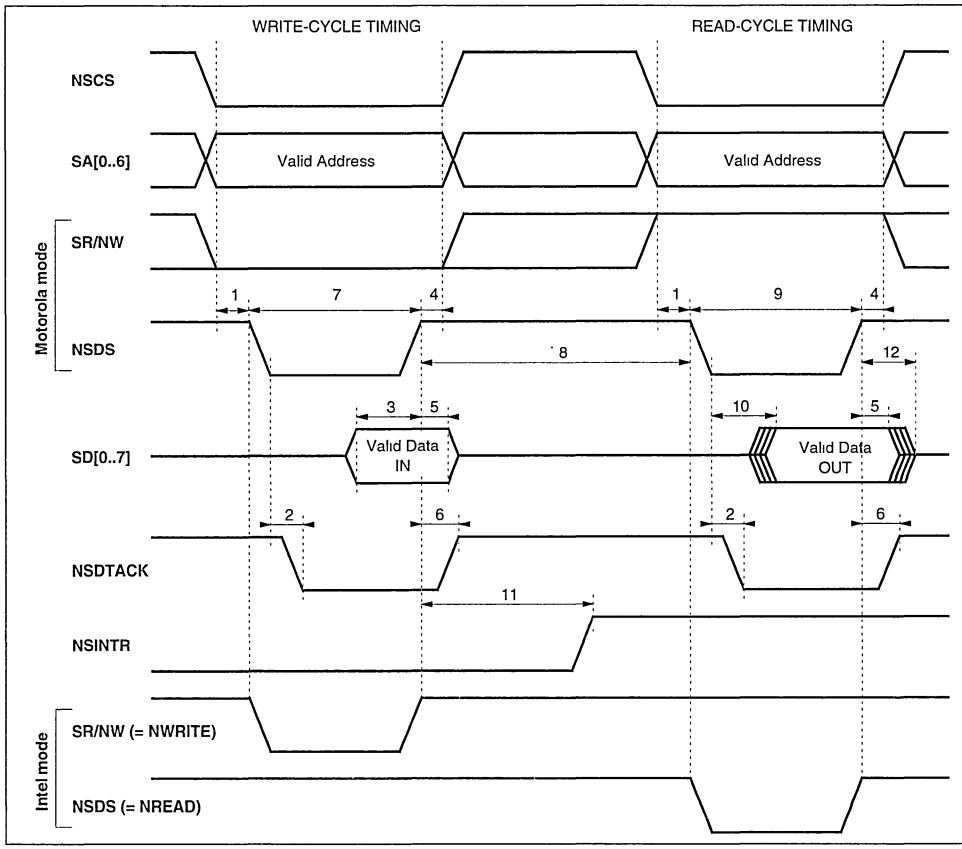
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage			1.5	V
V_{IH}	High Level Input Voltage	3.5			V
I_L	Low Level Input Current GND < V_I < V_{ILmax}	-15			µA
I_H	High Level Input Current VIHmin < V_I < V_{DD}			15	µA

III.2.3 - Analog Interface

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{REF}	Differential Reference Voltage Input = V_{REFP} - V_{REFN}		2.40	2.50	2.60	V
V_{CMOin}	Input Common Mode Offset, v = (RXA1+RXA2)/2 - V_{CM}		-300		300	mV
V_{DIFin}	Differential Input Voltage RXA1 - RXA2				2 x V_{REF}	V_{PP}
V_{CMOout}	Output Common Mode Voltage Offset = (TXA1+TXA2)/2 - V_{CM}		-200		200	mV
V_{DIFout}	Differential Output Voltage TXA1 - TXA2				2 x V_{REF}	V_{PP}
VOFFOut	Differential Output DC Offset (TXA1 - TXA2)		-100		100	mV
Rin	Input Resistance	RXAx	100			kΩ
Rout	Output Resistance	TXAx			20	Ω
RL	Load Resistance	TXAx	10			kΩ
CL	Load Capacitance	TXAx			50	pF

III.3 - AC Electrical Characteristics

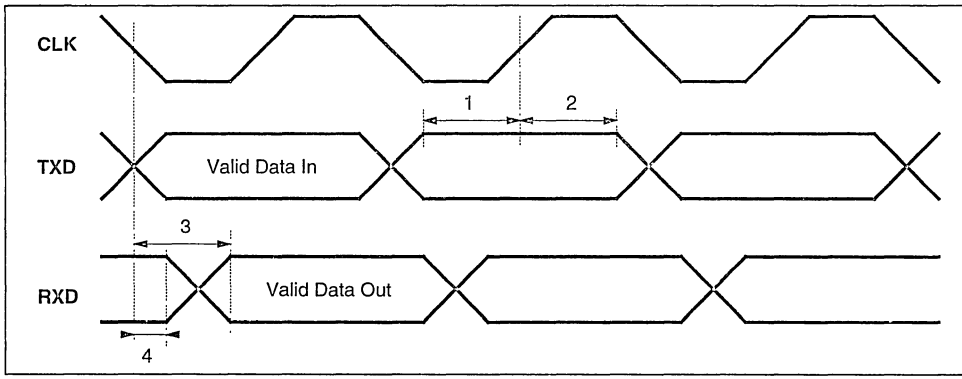
III.3.1 - Dual Port RAM Host Timing



Number	Description	Min.	Typ.	Max.	Unit
1	Address and Control Set-up Time	5			ns
2	SDTACK Acknowledge			20	ns
3	Data Set-up Time	10			ns
4	Address and Control Hold Time	0			ns
5	Data Hold Time	5			ns
6	SDTACK Hold Time	0			ns
7	Write Enable Low State	45			ns
8	Access Inhibition High State (see Note)	70			ns
9	Read Enable Low State	45			ns
10	Read Data Access			35	ns
11	SINTR Clear Delay			50	ns
12	Data Valid to Tristate			15	ns

Note : A minimum delay of 70ns is required only from the rizing edge of NWRITE to the falling edge of the next selected NREAD or NWRITE.

III.3.2 - Serial V.24 Interface Timing



Number	Description	Min.	Typ.	Max.	Unit
1	TXD to CLK Set-up Time	30			ns
2	TXD to CLK Hold Time	10			ns
3	RXD Valid to CLK Delay Time			100	ns
4	RXD Valid to CLK Hold Time	0			ns

IV - FUNCTIONAL DESCRIPTION

IV.1 - System Architecture

The chip allows the design of a complete FAX data-pump without any external component. A versatile dual port RAM allows an easy interface with most micro-controllers.

IV.2 - Operation

IV.2.1 - Modes

The modem implementation is fully compatible with FAX modulation recommendations. The modulation can be either Trellis Coded Modulation (TCM) as in V.17 14400, 12000, 9600, 7200bps rates, Quadrature Amplitude Modulation (QAM) as in V.29 9600, 7200, 4800 and V.27ter 4800 and 2400bps. Other modes of operation include tone and DTMF detection or generation, or speech mode.

IV.2.2 - Transmitter Description

The signal pulses are shaped in a dedicated filter further combined with a compromise transmit equalizer suited for transmission over strongly distorted lines. 3 different compromise equalizers are available and can be selected by software.

IV.2.3 - Receiver Description

The receiver section handles complex signals and uses a fractionally spaced complex equalizer. It is able to cope with distant modem timing drifts up to 10^{-4} as specified in the ITU-T recommendations. It also compensate for frequency drift up to 10Hz and for phase jitter at multiple and simultaneous frequencies.

IV.2.4 - Tone Generator Description

Four tones can be simultaneously generated by the ST75C520. The tones are determined by their frequencies and by the output amplitude level. A set of specific commands are also available for DTMF generation (using two of the four generators available).

IV.2.5 - Tone Detector Description

Sixteen tones can be simultaneously detected by the ST75C520. Each of the tones to be detected is defined by the coefficients of a 4th order programmable IIR. Detection thresholds are also programmable from -45dBm up to -10dBm. DTMF detection is also available and is performed by a specific filter section (that requires no programming).

IV.2.6 - DTMF Detector Description

A DTMF Detector is included in the ST75C520, it allows detection of valid DTMF Digits. A valid DTMF Digit is defined as a dual Tone with a total power higher than -35dBm, a duration higher than 40ms and a differential amplitude within 8dB (negative or positive).

IV.2.7 - Voice Mode

The ST75C520 voice mode allows the implementation of enhanced telephone functions like answering machines. The incoming samples (9600Hz), received from the line are PCM A-law coded and writen into the dual port RAM. The outpoing samples are decompressed using the same A-law and output to the telephone line.

The voice mode is entered using a CONF command, it can be either transmit voice from the dual RAM Tx buffer to the telephone line, receive voice from the telephone line to the dual RAM buffer, or both of these functions simultaneously. The format of the signal is A-law coded without complementation of the even bits. The buffer mechanism, between the host micro-controler and the ST75C520, is identical to the mechanism used for parallel data exchanges except that it starts immediately after CONF command, the size of the transmit and received buffer, are and must be 8 bytes, there is no need for a XMIT command, and if an overrun or underrun condition occurs no error will be reported to the host processor.

IV.2.8 - Analog Loop Back Test Mode

In any transmission standard and serial data format, the ST75C520 can be configured for analog loop back test.

IV.2.9 - Low Power Mode

Sleep state can be attained by a SLEEP command. Activating the reset signal will wake up the data-pump. When in sleep mode, the dual port RAM is unavailable and the clocks are disabled.

When entering the low power mode, the ST75C520 stops its oscillator, all the peripherals of the DSP core are stopped in order to reduce the power consumption. The dual RAM is made inacessible.

The ST75C520 can be awakened by a hardware reset.

There is a maximum time of 20ms to restart the oscillator after waking up and an additional 5ms after the interrupt to be able to accept any command coming from the host.

IV.2.10 - Reset

After a hardware reset, or an INIT command, the ST75C520 clears all its internal memories, clears the whole dual RAM and starts to initialize the delta sigma analog converters. As soon as these initializations are completed, the ST75C520 clears the dual RAM address 0 (COMSYS), generates an interrupt IT6 (command acknoledge) and is programmed to send and receive tones, the bit clock and the sample clock are programmed to 9600Hz. The total duration of the reset sequence is about 5ms. After that time the ST75C520 is ready to execute commands sent by the host micro-controller. The duration of the reset signal should be greater than 700ns.

IV.3 - Modem Interface

IV.3.1 - Analog Interface

The modem designer must provide a proper hybrid interface to the ST75C520. An example of hybrid design is given in paragraphs XII and XIII. The inputs and outputs of the MAFE are differential, achieving thus a better noise immunity. The D/A converter output amplifier includes a single pole low-pass filter, its cut-off frequency is :

F_c - 3dB # 19200Hz.

Continuous-time filtering of the analog differential output is necessary using an off-chip amplifier and a few external passive components.

IV.3.2 - Host Interface

The host interface is seen by the micro as a 64x8 RAM, with additional registers accessible through an 8-bit address space. A selection Pin (INT/MOT) allows to configure the host bus for either INTEL or MOTOROLA type control signals.

V - USER INTERFACE

V.1 - Dual Port Ram Description

The dual port RAM is the standard interface between the controller and the ST75C520, for either commands or data. This memory is addressed through a 7-bit address bus. The locations from $00 to $3F are RAM locations, while locations from $40 to $50 are control registers dedicated to the interrupt handling.

Several functional areas are defined in the dual port RAM, namely :

- the command area,
- the report area,
- the status area,
- the data buffer area.

V.1.1 - Mapping

V.1.1.1 - Command Area

The command area is located from $00 to $04. Address $00 holds the command byte COMSYS, and the next four locations hold the parameters COMPAR[0..3]. The command parameters must be entered before the command word is issued. Once the command has been entered, the command byte is reset and an acknowledge report is issued. A new command should not be issued before the acknowledge counter COMACK is incremented.

V.1.1.2 - Report Area

The report area is located from address $05 to address $07. Location $05 holds the acknowledge counter COMACK. Each time a command is acknowledged, the report bytes COMREP[0..1] (if any) are written by the ST75C520 into locations $06 and $07, and the content of COMACK is incremented. This counter allows the ST75C520 to accurately monitor the command processing.

V.1.1.3 - Status Area

The status area is located from address $08 to $0A. The error status word SYSERR is located at address $08. This error status word is updated each time an error condition occurs. An optional interruption IT0 may additionally be triggered in the case of an error condition. Locations $09 and $0A hold the general status bytes STATUS[0..1]. The meaning of the bits depends on the mode of operation, and is described in Chapter VII. The third byte at address $0B holds the Quality Monitor byte STAQUA.

V.1.1.4 - Optional Status Area

The user can program (through the DOSR command) the three locations STAOPT[0..2] of the Optional Status Area ($0C to $0E) for the real time monitoring of three arbitrary memory locations.

V.1.1.5 - Data Buffer Area

The data area is made of four 8-byte buffers. Two are dedicated to transmission and the two others to reception. Each of the four buffers is attached to a status byte. the meaning of the status byte depends on the selected format of transmission. Within each buffer, D0 represents the first bit in time.

V.1.2 - Interruptions

The ST75C520 can generate 5 interrupts for the controller. The interrupt handling is made with a set of registers located from $40 to $50.

The interruptions generated by the ST75C520 come from several different sources. Once the ST75C520 raises an interrupt, a signal is sent to the controller. The controller has then to process the interrupt and clear it. The interrupt source can be examined in the Interrupt Source Register ITSRCR located at $50. According to this status byte, the interrupt source can be determined. Then, writing a zero at one of the memory location $40 to $46 (Reset Interrupt Registers ITREST[0..6]) will reset the corresponding interrupt (and thus acknowledge it). These sources of interruptions can be masked globally or individually using the Interrupt Mask Register ITMASK located at $4F.

The interrupt sources are :

- **IT0 : Error/Warning**
  This signifies that an error has occurred and the error code is available in the error status byte SYSERR. This byte can be selectively cleared by the CSE command.
- **IT2 : Tx Buffer**
  Each time the ST75C520 frees a buffer, this interrupt is generated.
- **IT3 : Rx Buffer**
  Each time the ST75C520 has filled a buffer, this interrupt is generated.
- **IT4 : Status Byte**
  This signifies that the status byte has changed and must be checked by the controller.
- **IT6 : Command Acknowledge**
  This signifies that the ST75C520 has read the last command entered by the host, incremented the command counter COMACK, and is ready for a new command.

ITSRCR	X	D6	X	D4	D3	D2	X	D0

D0 = 1 IT0 Pending
D2 = 1 IT2 Pending
Dn = 1 ITn Pending

ITMASK	D7	D6	X	D4	D3	D2	X	D0

D7 and D0 = 1 IT0 Enable D
D7 and D2 = 1 IT2 Enable D
....
D7 and D6 = 1 IT6 Enable D

V.1.3 - Host Interface Summary

Address (hex)	Description	Size (Byte)	Mnemonic
COMMAND AREA			
$00	Command	1	COMSYS
$01-$04	Command Parameters	4	COMPAR[0..3]
REPORT AREA			
$05	Acknowledge Counter	1	COMACK
$06-$07	Report	2	COMREP[0..1]
STATUS AREA			
$08	Error Status	1	SYSERR
$09-$0A	General Status	2	STATUS[0..1]
$0B	Quality Monitor	1	STAQUA
$0C-$0E	Optional Report	3	STAOPT[0..2]
DATA AREA			
$1C	Data Rx Buffer 0 Status	1	DTRBS0
$1D-$24	Data Rx Buffer 0	8	DTRBF0[0..7]
$25	Data Rx Buffer 1 Status	1	DTRBS1
$26-$2D	Data Rx Buffer 1	8	DTRBF1[0..7]
$2E	Data Tx Buffer 0 Status	1	DTTBS0
$2F-$36	Data Tx Buffer 0	8	DTTBF0[0..7]
$37	Data Tx Buffer 1 Status	1	DTTBS1
$38-$3F	Data Tx Buffer 1	8	DTTBF1[0..7]
INTERRUPT AREA			
$40-$46	Reset Interrupt Reg.	7	ITREST[0..6]
$4F	Interrupt Mask Reg.	1	ITMASK
$50	Interrupt Source Reg.	1	ITSRCR

V.2 - Command Set

The Command Set has the following attractive features :

- user friendly with easy to remember mnemonics,
- possibility of straightforward expansion with new commands to suit specific customer requirements,
- easy upgrade of existing software using previous modem based SGS-THOMSON products.

The command set has been designed to provide the necessary functional control on the ST75C520. Each command is classified according to its syntax and the presence/absence of parameters. In the case of a parametric command, parameters must first be written into the dual port RAM before the command is issued. Acknowledge and error report is issued for each command entered.

V.2.1 - Command Set Summary

V.2.1.1 - Operational Control Commands

INIT Initialize. Initialize the modem engine. Set all parameters to their default values and wait for commands of the control processor. Non parametric command.

IDT Identify. Return the product identification code. Non parametric command.

SLEEP Turn to low power mode, the ST75C520 enters the low power mode and stops its crystal oscillator to reduce power consumption. In this mode all the clocks are stopped and the dual RAM is unreachable.

HSHK Handshake. Begins the handshake sequence. The modem engine generates all the sequences defined in the ITU-T recommendations. A status report indicates to the control processor the state of the handshake. This command only applies to modes where a handshake sequence is defined. A CONF command must have been issued prior to the use of HSHK. Non parametric command.

STOP FAX Stop. Stop FAX Half-duplex transmitter. Non parametric command.

SYNC FAX Synchronize. Start/Stop of FAX Half-duplex receiver. Parametric command.

CSE Clear Status Error. Selectively clears the Error status byte SYSERR. Parametric command.

SETGN Set Gain. This command sets the global gain factor, which is used for the transmit samples. Parametric command.

V.2.1.2 - Data Communication Commands

XMIT Transmit Data. Start/stop the transmission of data in parallel mode. After a XMIT command, the ST75C520 sends the data contained in its dual port RAM.

SERIAL Select Serial or Parallel Mode. This command selects the data source, i.e. either parallel or serial. The parallel mode uses a part of the dual port RAM as a double buffer. The serial mode uses the serial synchronous I/O. Parametric command.

FORM Selects the Transmission Format (only in parallel mode). This command configures the data interface for both receiver and transmitter according to the selected data format. Parametric command (HDLC or synchronous). In serial mode, format is always synchronous.

V.2.1.3 - Memory Handling Commands

MW Memory Write. This command is used to write an arbitrary 16-bit value into the writable memory location currently specified by a parameter. Parametric command.

MR Memory Read. This command allows the controller to read any of the ERAM or CROM (ST75C520 memory spaces) location without interrupting the processor. Parametric command.

CR Complex Read. This command allows the controller to read at the same time the real and imaginary part of a complex value stored in a double ERAM or CROM location. This feature is very interesting for eye pattern software control and for equalization monitoring. This command insures that the real and imaginary parts are sampled in the memory at the same time (integrity). Parametric command.

V.2.1.4 - Configuration Control Commands

CONF Configure. This command configures the modem engine for data transmission and handshake procedures (if any) in any of the supported modes. The transmission parameters are set to their default values and can be modified with the MODC command. Parametric command.

MODC Modify Configuration. This command allows modification of some of the parameters which have been set up by the CONF command. It can also be used to alter the mode of operations (short train). Parametric command.

DOSR Define Optional Status Report. This command allows the modification of the optional status report located in the status area of the dual port RAM. One can thus select a particular parameter to be monitored during all modes of operation. Parametric command.

DSIT Define Status Interrupt. This command allows the programming of the status word bit that will generate an Interrupt to the controller. Parametric command.

V.2.1.5 - Tone Generation Commands

TONE Select Tone. Programs the tone generator(s) for the desired default tone(s). Additional mnemonics provide quick programming of DTMF tones or other currently used tones. Parametric command.

DEFT Define Tone. Programs the tone generator(s) for arbitrary tone synthesis. Parametric command.

TGEN Tone Generator Control. Enables or disables the tone generator(s). Parametric command.

IV.2.1.6 - Tone Detection Commands

TDRC Read Tone Detector Coefficient. Read one Tone Detector Coefficient. Parametric command.

TDWC Write Tone Detector Coefficient. Write one Tone Detector Coefficient. Parametric command.

TDRW Read Tone Detector Wiring. Read one Tone Detector Wiring connection. Parametric command.

TDWW Write Tone Detector Wiring. Write one Tone Detector Wiring connection. Parametric command.

TDZ Clear Tone Detector Cell. Clear internal variables of a Tone Detector Cell. Parametric command.

V.2.1.7 - Miscellaneous Commands

CALL Call a Subroutine. Call a subroutine with one Parameter. Parametric command.

JSR Call a Low Level Subroutine. Call an internal subroutine with one parameter. Parametric command.

V.3 - Command Set Short Form

CCI Command		
Mnemonic	**Value**	**Description**
XMIT	0x01	Transmit Data
SETGN	0x02	Set Transmit Gain
SLEEP	0x03	Power Down the ST75C520
HSHK	0x04	Start Handshake
INIT	0x06	Initialize (Software Master RESET)
SERIAL	0x07	Enable/disable Data Serial Mode
CSE	0x08	Clear Error Status Word
FORM	0x09	Define Parallel Data Format
DOSR	0x0A	Define Optional Status Report
TONE	0x0C	Generate Predefined Tones
TGEN	0x0D	Enable Tone Generator
DEFT	0x0E	Define Arbitrary Tone
MR	0x10	Memory Read
CR	0x11	Complex Read
MW	0x12	Memory Write
DSIT	0x13	Define Status Interrupt
IDT	0x14	Return Product Identification Code
JSR	0x18	Call a Low Level Subroutine
CALL	0x19	Call a Subroutine
TDRC	0x1A	Tone Detector Read Coefficient
TDRW	0x1B	Tone Detector Read Wiring
TDWC	0x1C	Tone Detector Write Coefficient
TDWW	0x1D	Tone Detector Write Wiring
TDZ	0x1E	Tone Detector Clear Cell
CONF	0x20	Configure
MODC	0x21	Modify Default Configuration
STOP	0x25	FAX Stop Transmitter
SYNC	0x26	FAX Synchronize Receiver

V.4 - Status - Reports

V.4.1 - Status

The ST75C520 has a dedicated status reporting area located in its dual port RAM. This allow a continuous monitoring of the status variables without interrupting the ST75C520.
The first status byte gives the error status. Issuing of an error status can also be flagged by a maskable interrupt for the controller. The signification of the error codes are given in Chapter VII.
The second and third status bytes give the general status of the modem. These status include for example the ITU-T circuit status and other items described in appendix. These two status can generate, when a change occurs, an interrupt to the controller ; each bit of the two byte word can be masked independently.
The forth byte gives in real time a measure of the reception quality. This information may be used by the controller to monitor the quality of the received bits.
Three other locations are dedicated for custom status reporting. The controller can program the ST75C520 for a real time monitoring of any of its internal RAM location. High byte or low byte of any word can thus be monitored.

V.4.2 - Reports

The ST75C520 features an acknowledge and report facility. The acknowledge of a command is monitored by a counter COMACK located in the dual port RAM. Each time a command is read from the command area, the ST75C520 will increment this counter. For instance, when a MR (Memory Read) command is issued, the data is first written in the report area, and the counter is incremented afterwards. This way of processing insures data integrity and gives additional synchronization between the controller and the data pump.

V.5 - Data Exchanges

The ST75C520 accepts many kinds of data exchange : the default mode uses the synchronous serial exchange. Other modes include HDLC framing support and synchronous parallel exchanges. Detailed description of the Data Buffer Exchanges modes is available in the paragraph IX.

V.5.1 - Synchronous Parallel Mode

The data exchanges are made through the dual port RAM and are byte synchronous oriented. The double buffer facilities of the ST75C520 allow an efficient buffering of the data.

V.5.1.1 - Transmit

The controller must first fill at least the first buffer of data (Tx Buffer 0) with the bits to be transmitted. In order to perform this operation, the controller must first check the Tx Buffer 0 status word DTTBS0. If this buffer is empty, the controller fills the data buffer locations (up to 64 bits), and then writes in DTTBS0 the number of bytes contained in the buffer. The controller can then either proceed with the second buffer or initiate the transmission with a XMIT command.
The ST75C520 copies the contents of the data buffer and then clears the buffer status word in order to make it again available, then generates an IT2 interrupt. The number of bytes specified by the status word is then queued for transmission. The process goes on with the two buffers until an XMIT command stops the transmission. After the finishing XMIT command has been issued, the last buffers are emptied by the ST75C520.
Errors occur when both buffers are empty while the transmit bit queue is also empty. Error is signalled with an IT0 interruption to the controller.

V.5.1.2 - Receive

The controller should take care of releasing the Rx buffers before the Data Carrier Detect goes true. This is made by writing zero in the Rx Buffer Status 0 and 1. The ST75C520 then fills the first buffer, and once filled sets the status word with the number of bytes received and then generates an IT3 interrupt. It then takes control of the second buffer and operates the same way. The controller must check the status of the buffers and empty them. Once the data read, the controller must release the used buffer and wait for the next buffer to be filled.
Error occurs when both buffers are declared full, and incoming bits continue to arrive from the line. Error is signaled by an IT0 interrupt.

V.5.2 - HDLC Parallel Mode

This mode implements part of the High Level Data Link Control formats and procedures. It is well suited for error correcting protocols like ECM or FAX T4/T30 recommendations. It supports the flagging generation, 16-bit Frame Check Sequence, as well as the Zero insertion/deletion mechanism.

V.5.3 - Serial Exchanges

The other mode of operation for data exchanges is the Serial Synchronous Mode. In this mode, the data I/O is made through the V.24 interface (page 4). Even when using the parallel mode described above, the received bits are available on the ST75C520 RxD Pin. See paragraph VII.2.1 table for clock values.

VI - COMMAND SET DESCRIPTION

The appendix A contains the description of the complete command set. Commands are presented according to the following form :

COMMAND **Command Name Meaning** **COMMAND**

Opcode Hexadecimal digit

X	X	X	X	X	X	X	X

Synopsis Short description of the functions performed by the command.

Parameters

Field	Byte	Pos.	Value	Definition
Name	X	b..a	xx *	Explanation of the parameter Default value

Field Name of the addressed bit field.

Byte Index (or address in the dual port RAM) of the parameter byte (from 1 to 4).

Pos. Bit field position inside the parameter byte. Can either be a single position (from 0 to 7, 0 being LSB) or a range.

Value Possible values for the bit (resp. bit field). Range means all values are allowed. A star means a default value. Values are expressed either under the form of a bit string, or under hexadecimal format.

CALL **Call a Subroutine** **CALL**

Opcode: 19

0	0	0	1	1	0	0	1

Synopsis CALL allows to execute a part of the ST75C520 firmware with a specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	7..0		Low byte of the call address
C_ADDR_H	2	7..0		High byte of the call address
C_DATA_L	3	7..0		Low byte of the argument
C_DATA_H	4	7..0		High byte of the argument

CONF — Configure for Operations — CONF

Opcode 20

0	0	1	0	0	0	0	0

Synopsis CONF allows the complete definition of the ST75C520 operation, including the mode of operation (tone, FAX transmit, FAX receive, voice transmit, voice receive, DTMF receive, ...) and the modem parameters (standard, speed, ...).

Parameters

Field	Byte	Pos.	Value	Definition
CONF_OPER	1	3..0	-	Mode of operation, see below
CONF_ANAL	1	4	0 1	Normal mode Analog loop back (test mode only)
CONF_PSTN	1	5	0 1	PSTN (carrier detect set to -43/-48dBm) Leased line (carrier detect -33/-38dBm)
CONF_AO	1	6	0 1	Answer mode (FSK full duplex only) Originate mode (FSK full duplex only)
CONF_V24	1	7	0 1	Do not use RTS pin signal Use RTS pin signal
CONF_MODE	2	5..0	1 3 4 7 8 9 C D Other	Bell 103 (full duplex) V.21 (full duplex) V.23 (full duplex) V.27ter V.29 V.17 V.33 (half duplex) V.21 channel 2 Reserved
CONF_TXEQ	2	7..6	0 1 2 3	No transmit equalizer Transmit equalizer #1 Transmit equalizer #2 Transmit equalizer #3
CONF_CAR	3	0	0 1	1800Hz carrier (V.17/V.33 only) 1700Hz carrier (V.17/V.33 only)
CONF_SP0	3	7..5	xx1 x1x 1xx	2400bps allowed (V.27) 4800bps allowed (V.27, V.29) 7200bps allowed (V.29, V.17)
CONF_SP1	4	2..0	xx1 x1x 1xx	9600bps allowed (V.29, V.17) 12000bps allowed (V.17, V.33) 14400bps allowed (V.17, V.33)

According with the 4 first bits of the CONF_OPER the ST75C520 is put into the following mode of operation.

CONF_OPER	Transmit	Received
0000*	Tones	Tones
0010	Voice	Tones
0100	Tone	DTMF
0110	Voice	DTMF
1000	Tones	Voice
1010	Voice	Voice
1111	Modem	Modem
Other	Not allowed	Not allowed

CR — Complex Read — CR

Opcode: 11

0	0	0	1	0	0	0	1

Synopsis CR allows the reading of a complex parameter. The parameter specifies the parameter address (for the real part : the imaginary part is next location). CR returns the high byte value of both real and imaginary part of the addressed complex parameter.

Parameters

Field	Byte	Pos.	Value	Definition
CR_ADDR_L	1	7..0		Low byte of the 16-bit address
CR_ADDR_H	2	7..0		High byte of the 16-bit address

CSE — Clear Error Status — CSE

Opcode: 08

0	0	0	0	1	0	0	0

Synopsis CSE is used to clear the ST75C520 error status SYSERR byte. It is also used as an acknowledge to the error condition handler. For details, please refer to the corresponding appendix.

Parameters

Field	Byte	Pos.	Value	Definition
ERR_MASK	1	7..0		Error mask See report appendix for detailed meaning

DEFT — Define Arbitrary Tone — DEFT

Opcode: 0E

0	0	0	0	1	1	1	0

Synopsis DEFT programs one of the four tone generator for arbitrary tone generation. The parameter is the frequency of the generated tone expressed in Hertz between 0 and 3600Hz.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_GEN_SL	1	1..0		Index of the tone generator (3..0)
TONE_FREQ_L	2	7..0		Low byte of the frequency
TONE_FREQ_H	3	7..0		High byte of the frequency (internally masked with 0F)
TONE_SCALE	4	7..0		Amplitude scaling factor (high byte) 3F gives the nominal amplitude

DOSR — Define Optional Status Report — DOSR

Opcode: 0A

0	0	0	0	1	0	1	0

Synopsis DOSR specifies the address of the RAM variables to be monitored in the 3 locations STAOPT[0..2] of the dual port RAM. It also specifies the assignment within the 3 locations.

Parameters

Field	Byte	Pos.	Value	Definition
STA_OPT_ASS	1	1..0	0..2	Index of the STAOPT destination
STA_OPT_ADL	2	7..0		Low byte of source address
STA_OPT_ADH	3	3..0		High byte of source address
STA_OPT_HL	3	7	0 1	Select low byte of source Select high byte of source

DSIT — Define Status Interrupt — DSIT

Opcode: 13

0	0	0	1	0	0	1	1

Synopsis DSIT specifies the bit mask used with the STATUS[0] and STATUS[1] byte to generate an interrupt IT4 to controller. Each time a bit change happens in the status words, assuming the corresponding bit mask will be set, an interrupt will be generated.

Parameters

Field	Byte	Pos.	Value	Definition
STA_IT_MSK0	1	7..0		Status[0] bit mask pattern
STA_IT_MSK1	2	7..0		Status[1] bit mask pattern

Notes : The default IT Status is 0x3F for STATUS[0] and 0xFF for STATUS[1].

FORM — Select Transmission Format — FORM

Opcode: 09

0	0	0	0	1	0	0	1

Synopsis FORM defines the type of transmission used. This format is valid only in the parallel data mode. The default format, unless specified, is synchronous.

Parameters

Field	Byte	Pos.	Value	Definition
X_SYNC	1	1..0	00* 01 10 11	Synchronous format Transmit continous "1" (1) HDLC framing Transmit continous "0" (1)

Notes : 1. This format is only valid for the transmiter.

HSHK — Handshake — HSHK

Opcode: 04

0	0	0	0	0	1	0	0

Synopsis HSHK is used to command the ST75C520 to begin the transmit handshake sequence processing. The progress of the handshake is reported to the control processor.

Parameter Non parametric command.

IDT — Identify — IDT

Opcode: 14

0	0	0	1	0	1	0	0

Synopsis IDT Return the ST75C520 Hardware and Software release number. See paragraph VII.1.4.

Parameter Non parametric command.

INIT — Initialization — INIT

Opcode: 06

0	0	0	0	0	1	1	0

Synopsis INIT forces the ST75C520 to reset all parameters to their default conditions and restart operations.

Parameter Non parametric command.

Notes : This command makes a software reset of the ST75C520 and so cannot have the regular handshake protocol It does not increment the COMACK, neither generate an Interrupt.

JSR — Call a Low Level Subroutine — JSR

Opcode: 18

0	0	0	1	1	0	0	0

Synopsis JSR allows to execute a part of the ST75C520 firmware with a specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	7..0		Low byte of the call address
C_ADDR_H	2	7..0		High byte of the call address
C_DATA_L	3	7..0		Low byte of the argument
C_DATA_H	4	7..0		High byte of the argument

MODC — Modify Configuration — MODC

Opcode: 21

0	0	1	0	0	0	0	1

Synopsis MODC allows modification of the configuration for special purpose. This command has no effect while in data mode, the parameters are just sampled when starting to transmit or receive. The value of these parameters are not affected when sending a CONF command.

Parameters

Field	Byte	Pos.	Value	Definition
MODC_SH	1	6	0* 1	Normal training sequence Short training (1) sequence
MODC_FPT	2	3..2	00* 01 10	No echo protection tone Long echo protection tone (180ms) Short echo protection tone (30ms)

Notes : 1. Short train sequence must be preceded by at least one normal training sequence.

MR — Memory Read — MR

Opcode: 10

0	0	0	1	0	0	0	0

Synopsis MR allows the reading of a 16-bit parameter. The parameter specifies the parameter address.

Parameters

Field	Byte	Pos.	Value	Definition
MR_ADDR_L	1	7..0		Low byte of the 16-bit address
MR_ADDR_H	2	7..0		High byte of the 16-bit address

MW — Memory Write — MW

Opcode: 12

0	0	0	1	0	0	1	0

Synopsis MW allows the writing of a 16-bit parameter. The parameter specifies the address as well as the value to be transferred.

Parameters

Field	Byte	Pos.	Value	Definition
MW_ADDR_L	1	7..0		Low byte of the 16-bit address
MW_ADDR_H	2	7..0		High byte of the 16-bit address
MW_VALUE_L	3	7..0		Low byte of the 16-bit value
MW_VALUE_H	4	7..0		High byte of the 16-bit value

SERIAL — Select Serial or Parallel Mode — SERIAL

Opcode: 07

0	0	0	0	0	1	1	1

Synopsis SERIAL defines the data path, i.e. either serial or parallel.

Parameters

Field	Byte	Pos.	Value	Definition
TX_SDATA	1	0	0* 1	Use serial link for Tx Data Use parallel link for Tx Data
RX_SDATA	1	1	0* 1	Use only serial link for Rx Data Use also parallel link for Rx Data

Notes : The received Bits always go to the output pin RXD, even when the RX_SDATA bit is set.

SETGN — Set Output Gain — SETGN

Opcode: 02

0	0	0	0	0	0	1	0

Synopsis SETGN is a command which sets the scaling factor of the transmit samples. It is used for setting the output level or for setting the level of the tone generators. The gain value is given in the form of a 2's complement 16-bit value.

Parameters

Field	Byte	Pos.	Value	Definition
GAIN_L	1	7..0	range FF*	Low byte of the 16-bit gain value
GAIN_H	2	7..0	range 7F*	High byte of the 16-bit gain value

Example

Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)
0	7FFF	-5	47FA	-10	287A
-1	7214	-6	4026	-11	2413
-2	65AC	-7	392C	-12	2026
-3	5A9D	-8	32F5	-13	1CA7
-4	50C3	-9	2D6A	-14	198A

SLEEP — Turn to Sleep Mode — SLEEP

Opcode: 03

0	0	0	0	0	0	1	1

Synopsis SLEEP is used to force the ST75C520 to turn to low power mode.

Parameter Non parametric command.

Notes : When receiving this command the ST75C520 will stop processing and so cannot have the regular handshake protocol. It does not increment the COMACK, neither generate an Interrupt.

STOP — FAX Stop Transmitter — STOP

Opcode: 25

0	0	1	0	0	1	0	1

Synopsis STOP is used, in FAX Modes, to force the ST75C520 to turn off the transmitter in accordance with the corresponding ITU-T V.33/V.17/V.29/V.27 recommendation.

Parameter Non parametric command.

Notes : When receiving this command the ST75C520 will stop sending regular Data In parallel mode this command must be preceded by a **XMIT** Stop command. In parallel mode the ST75C520 will wait until all the transmit buffers are sent before starting the Stop sequence.

SYNC

FAX Synchronize the Receiver

SYNC

Opcode: 26

0	0	1	0	0	1	1	0

Synopsis SYNC is used, in FAX Modes, to force the ST75C520 to Start/Stop the receiver in accordance with the corresponding ITU-T V.33/V.17/V.29/V.27 recommendation.As soon as the ST75C520 receives the **SYNC** Start command it sets its receiver to detect the FAX synchronization signal.This command is the equivalent **HSHK** command for the receiver.

Parameters

Field	Byte	Pos.	Value	Definition
RX_SYNC	1	0	0* 1	Stop receiver Start receiver synchronization

TDRC

Tone Detector Read Coefficient

TDRC

Opcode: 1A

0	0	0	1	1	0	1	0

Synopsis TDRC Read one Coefficient of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_C_ADDR	2	7..0	0..B 10 20 Other	Biquad coefficient Energy coefficient Static level Reserved

The command answer is : Low Byte of Coefficient followed by High Byte of Coefficient.

TDRW

Tone Detector Read Wiring

TDRW

Opcode: 1B

0	0	0	1	1	0	1	1

Synopsis TDRC Read Wiring of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_W_ADDR	2	0	0 1 Other	Biquad and energy input Comparator inputs Reserved

The command answer is:

a) If TD_W_ADDR = 0 :
- First Byte is the Node Number of the Signal connected to Biquadratic Filter input.
- Second Byte is the Node Number of the Signal connected to the Energy estimator input.

b) if TD_W_ADDR = 1 :
- First Byte is the Node Number of the Signal connected to Comparator Negative input.
- Second Byte is the Node Number of the Signal connected to the Comparator Positive input.

TDWC — Tone Detector Write Coefficient — TDWC

Opcode: 1C

0	0	0	1	1	1	0	0

Synopsis TDWC Write one Coefficient of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_C_ADDR	2	7..0	0..B 10 20 Other	Biquad coefficient Energy coefficient Static level Reserved
TD_COEFL	3	7..0		Low byte of coefficient
TD_COEFH	4	7..0		High byte of coefficient

TDWW — Tone Detector Write Wiring — TDWW

Opcode: 1D

0	0	0	1	1	1	0	1

Synopsis TDRC Write Wiring of the selected Tone Detector Cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_W_ADDR	2	0	0 1 Other	Biquad and energy input Comparator inputs Reserved

If TD_W_ADDR = 0 (Select Biquad and Energy Inputs)

Parameters

Field	Byte	Pos.	Value	Definition
TD_W_ERN	3		0..3F	Energy estimator signal input
TD_W_BIQ	4		0..3F	Biquad filter signal input

If TD_W_ADDR = 1 (Select Comparator Inputs)

Parameters

Field	Byte	Pos.	Value	Definition
TD_W_CN	3		0..3F	Negative comparator signal input
TD_W_CP	4		0..3F	Positive comparator signal input

TDZ — Tone Detector Clear Cell — TDZ

Opcode: 1E

0	0	0	1	1	1	1	0

Synopsis TDZ Clears all internal variables of one Tone detector cell including Filter local variables and energy estimator. This command must be sent after changing coefficients of a cell to avoid instability.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number

TGEN — Enable/disable Tone Generators — TGEN

Opcode: 0D

0	0	0	0	1	1	0	1

Synopsis TGEN causes the ST75C520 to enable or disable the four tone generators.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_0_ENA	1	0	0* 1	Generator #0 disabled Generator #0 enabled
TONE_1_ENA	1	1	0* 1	Generator #1 disabled Generator #1 enabled
TONE_2_ENA	1	2	0* 1	Generator #2 disabled Generator #2 enabled
TONE_3_ENA	1	3	0* 1	Generator #3 disabled Generator #3 enabled

TONE — Predefined Tones — TONE

Opcode: 0C

0	0	0	0	1	1	0	0

Synopsis TONE programs the tone generators for the predefined tones. The tone generators #0 and eventually #1 are reprogrammed with this command. Eventually the tone generator #0 and #1 are enabled. Using a value not in the following table will disable tone generator #0 and #1.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_SELECT	1	5..0	0 1 2 3 4 5 6 7 8 9 A B C D E F 10 11 12 13	DTMF 0 (941 & 1336Hz) DTMF 1 (697 & 1209Hz) DTMF 2 (697 & 1336Hz) DTMF 3 (697 & 1477Hz) DTMF 4 (770 & 1209Hz) DTMF 5 (770 & 1336Hz) DTMF 6 (770 & 1477Hz) DTMF 7 (852 & 1209Hz) DTMF 8 (852 & 1336Hz) DTMF 9 (852 & 1477Hz) DTMF A (697 & 1633Hz) DTMF B (770 & 1633Hz) DTMF C (852 & 1633Hz) DTMF D (941 & 1633Hz) DTMF * (941 & 1209Hz) DTMF # (941 & 1477Hz) Answer tone (2100Hz) Tone (1650Hz) Answer tone (2225Hz) Tone (1300Hz)

XMIT — Start/stop Transmission — XMIT

Opcode: 01

0	0	0	0	0	0	0	1

Synopsis XMIT start or stop the transmission of the Parallel Transmit Data. This command work only if the Parallel Transmit Data mode has been selected with a **SERIAL** command.

Parameters

Field	Byte	Pos.	Value	Definition
TX_START	1	0	0* 1	Stop transmission Start transmission

VII - STATUS DESCRIPTION

This appendix is dedicated to the ST75C520 reporting features. in the following sections the command acknowledge process and the report and status definitions are explained.

VII.1 - Command Acknowledge and Report

VII.1.1 - Command Acknowledge Process

(see Figure 1)

The ST75C520 features an acknowledge process based on a counter COMACK. On power-on reset (or INIT command), this counter's value is set to 0. Each time a command is successfully executed by the ST75C520, the acknowledge counter COMACK is incremented. This allows a precise monitoring of the command entered and avoids command collision.

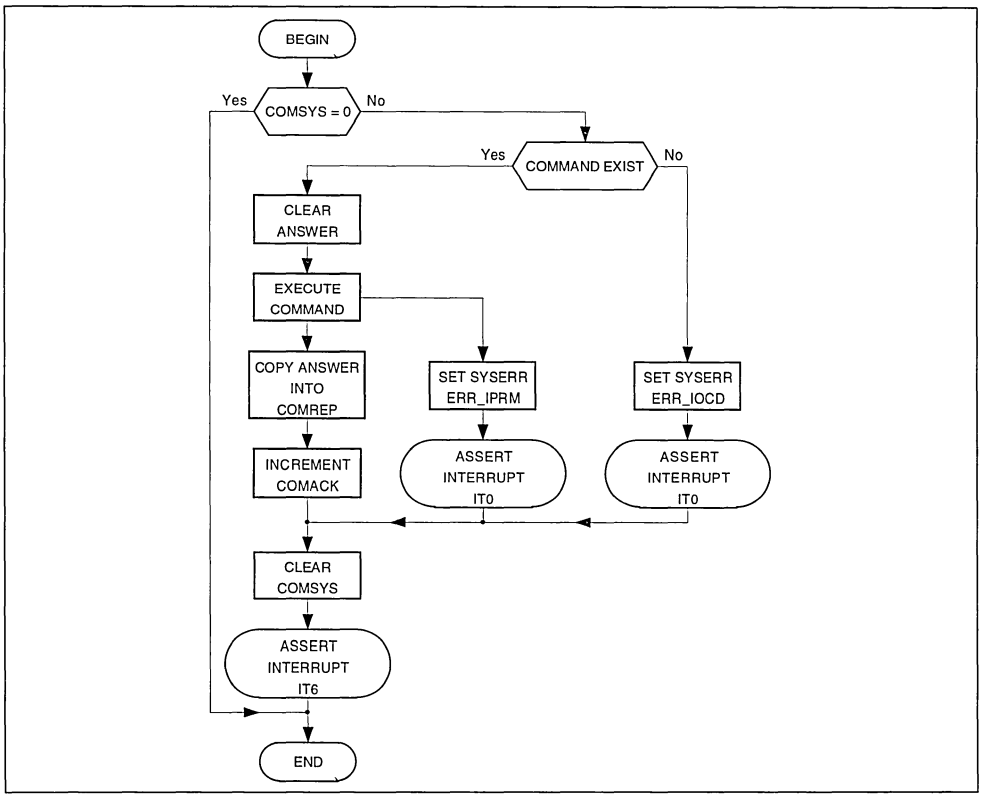
In the case of a memory reading command (CR, TDRC, TDRW, IDT or MR) once the command entered is executed, the report area is filled and the acknowledge counter is incremented afterwards. This insures that the controller will read the value corresponding to its request.

Furthermore, the ST75C520 resets the value of the COMSYS register once the command has been read. The interruption IT6 is raised just after the counter is incremented.

VII.1.2 - Reports Specification

The report section of the Dual Port RAM is dedicated to memory reading. In response to a CR, MR, TDRC, TDRW, IDT commands, the value read is transferred to the report registers COMREP[0..1].

Figure 1 : Command Acknowledge Process



VII.1.3 - CR Command

Issuing a CR command causes the ST75C520 to dump a specific memory location in complex mode. This instruction is particularly useful for equalizer state analysis or for software eye-pattern display. The report area has this meaning :

RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0	COMREP[0]
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	COMREP[1]

RP0..RP7 is the MSB part of the 16-bit value of the real part and IP0..IP7 is the MSB part of the imaginary part. The CR command insures that the real and imaginary part of the desired complex value are sampled internally at the same time. The address given in the parameter field of CR is the address of the real part.

VII.1.4 - MR/TDRC/TDRW/IDT Commands

The report issued by the MR/TDRC/TDRW/IDT commands follow the same rules as for CR. The report meaning is :

D7	D6	D5	D4	D3	D2	D1	D0	COMREP[0]
D15	D14	D13	D12	D11	D10	D9	D8	COMREP[1]

D0..D15 is the 16-bit value required by the MR/TDRC command.

In the case of IDT, D15..D12 contains the product identification (2 for ST75C520), D11..D8 contains the hardware revision identification and D7..D0 contains the software revision identification.

VII.2 - Modem Status

VII.2.1 - Modem Status Description

The Status of ST75C520 is divided into 4 fields :

- The error status byte SYSERR that provides information about error. This status can trigger an IT0 interrupt,
- The general status byte STATUS[0] and STATUS[1] that contains all the modem signals. These status bytes can trigger an IT4 interrupt,
- The quality status STAQUA, that contains the quality of the received transmission,
- The optional status bytes STAOP[0], STAOP[1] and STAOP[2], that contains additional information regarding the ST75C520 operating mode. This default information can be changed to monitor any internal variables using the DOSR command.

All these informations are updated on a Baud basis :

Mode	Baud Rate [2] (Hz)	CLK (Hz)
Tone, DTMF, Voice	2400	9600
Bell 103 (full duplex)	2400	9600
V.21 (full duplex)	2400	9600
V.23 (full duplex)	2400	9600
V.27ter 2400bps	1200	2400
V.27ter 4800bps	1600 [1]	4800
V.29	2400	9600/7200/4800
V.17	2400	14400/12000/9600/7200
V.33	2400	14400/12000
V.21 channel 2	2400	300

Notes : 1. The tone detectors outputs are update 800 times by second.

2. This baud rate defines also, the maximum command rate. Each baud time the ST75C520 looks at the COMSYS location (addesss $00) to see if a command have been sent by the host processor. If the content of this location is different from zero the ST75C520 execute the command.

Starting at the adddress $08 the status area have the following format :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$08	SYSERR	ERR_RTK	-	-	ERR_IPRM	ERR_IOCD	-	ERR_RX	ERR_TX
$09	STATUS0	STA_109F	STA_CPT10	STA_CPT1	STA_CPT0	STA_RING	STA_106	STA_107	STA_109
$0A	STATUS1	STA_DTMF	STA_FLAG	-	STA_HR	STA_AT	STA_CCITT	-	STA_H
$0B	STAQUA	-	Quality						
$0C	STAOP0	Depend on operating mode (see below)							
$0D	STAOP1								
$0E	STAOP2								

VII.2.2 - Error Status

The error status changes each time an error occurs. When the ST75C520 signals an error by setting one of the SYSERR bit, it generates an interrupt IT0. These bits can only be cleared by the host controler using the CSE command.

The meaning of the different bits of the SYSERR byte is discribed below :

SYSERR		
Field	**Pos.**	**Meaning when set**
ERR_TX	0	Transmit buffer underflow. Loss of synchronisation between the host and ST75C520 transmit data buffer managment.
ERR_RX	1	Receive buffer overflow. Loss of synchronisation between the host and ST75C520 receive data buffer managment.
ERR_IOCD	3	Incorrect CCI command
ERR_IPRM	4	Incorrect parameter for the CCI command
ERR_RTK	7	Real time kernel error. ST75C520 not able to perform all its tasks within the baud period (transmit or receive samples lost).

VII.2.3 - Modem General Status

The modem general status word is composed of two bytes STATUS[0] and STATUS[1]. Any bit change can generate an IT4 interrupt. Using the DSIT command allows the selection of the corresponding bit that will generate an interrupt each time they will change. The default pattern is $3F for STATUS[0] and $FF for STATUS[1].

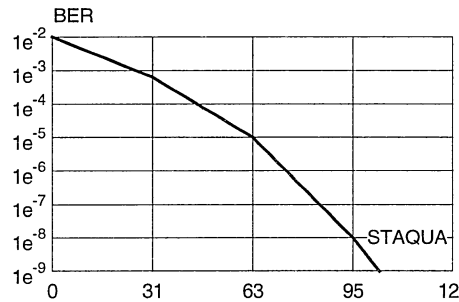
The different bits have the following meaning :

STATUS[0]		
Field	**Pos.**	**Meaning when set**
STA_109	0	CCITT circuit 109 (carrier detect). Indicates that valid data are received. When 0 the output data RxD are clamped to constant mark. Valid only in modem mode.
STA_107	1	CCITT circuit 107 (data set ready). Valid only in modem mode.
STA_106	2	CCITT circuit 106 (clear to send). Indicates that the training sequence has been completed and that any data at TxD pin (serial mode) or in the transmit buffer (parallel mode) will be transmitted. valid only in modem mode.
STA_RING	3	Ring detected. A ring signal (from 15Hz to 68Hz) is present at the RING pin. Valid only in tones modes. The precise frequency can be read in the optional status byte STAOP2. The detection time is 1 period of the ring signal. The detection lost time in 20ms after the last transition on the ring signal.
STA_CPT0	4	Call progress tone detector #0. Low pass filter 650Hz. Valid only in tones modes.
STA_CPT1	5	Call progress tone detector #1. High pass filter 600Hz. Valid only in tones modes.
STA_CPT10	6	Signal in filter #0 is highter than #1. Valid only in tones modes.
STA_109F	7	Fast Carrier Detect. Valid only in modem mode.

STATUS[1]		
Field	**Pos.**	**Meaning**
STA_H	0	Transmit synchronisation in progress. Valid only in modem mode.
STA_CCITT	2	CCITT 2100Hz versus 2225Hz answer tone detect. Valid if STA_AT is set. Valid only in tones modes.
STA_AT	3	Answer tone (either 2100Hz or 2225Hz) detected. Valid only in tones modes.
STA_HR	4	Receive synchronisation in progress. Valid only in modem mode.
STA_FLAG	6	V.21 channel 2 flag detect. Valid only in FAX modem mode and tone mode.
STA_DTMF	7	DTMF digit detect. The digit itself is available in the optional status byte STAOP2. Valid only in DTMF receive mode.

VII.2.4 - Quality Status

The quality byte STAQUA monitors an evaluation of the line quality. It is updated once per baud and its value ranges from 127 (perfect quality) to 0 (terrible quality). This value is automaticaly adjusted according to the current receiving mode. Refer to the following chart to convert the value into its Bit Error Rate equivalence.



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VII.2.5 - Optional Status

According to the operating mode of the ST75C520 the optional status is displaying different informations.

The optional status are automatically reprogrammed after each CONF command with the address of the variables to monitor according with the operating mode selected (CONF_OPER). After the CONF command the user must overwrite this default programming by using the DOSR command.

VII.2.6 - Default Optional Status in Tone Mode

While in tone mode the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	TDT7	TDT6	TDT5	TDT4	TDT3	TDT2	TDT1	TDT0
$0D	STAOP1	TDT15	TDT14	TDT13	TDT12	TDT11	TDT10	TDT9	TDT8
$0E	STAOP2	RING_PERIOD (1)							

Notes : 1. RING_PERIOD is valid when the bit 3 of the STATUS[0] (STA_RING) goes high. This value is updated at each falling edge of the RING signal. The RING_PERIOD value must be divided by 2400 to obtain the period in seconds.

2. TDTx is the output of the tone detector x.

VII.2.7 - Default Optional Status in DTMF Receiver Mode

While in DTMF receiver mode the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	TDT7 (1)	TDT6 (1)	TDT5 (1)	TDT4 (1)	TDT3	TDT2	TDT1	TDT0
$0D	STAOP1	TDT15 (1)	TDT14 (1)	TDT13 (1)	TDT12 (1)	TDT11 (1)	TDT10 (1)	TDT9 (1)	TDT8 (1)
$0E	STAOP2	DTMF_DIGIT (2)							

Notes : 1. These cells are used by the DTMF detector.
2. DTMF_DIGIT is valid when the bit 7 of STATUS[1] (STA_DTMF) goes high. This value remains unchanged until a new DTMF digit is detected.

VII.2.8 - Default Optional Status in Modem Mode

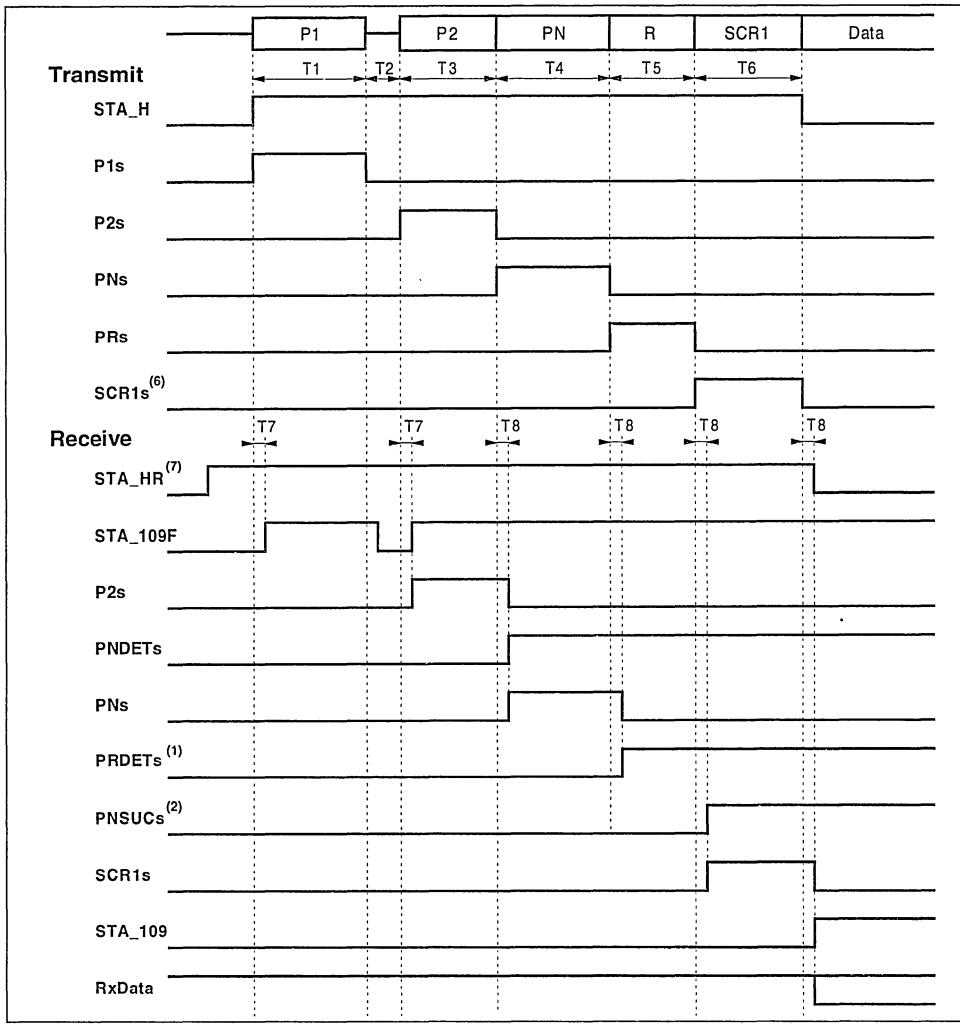
While in modem mode the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	x	x	x	SPEED (2)				SPVAL (1)
$0D	STAOP1	Not used							
$0E	STAOP2	PNSUCs	PRDETs	PNDETs	SCR1s	PRs	PNs	P2s	P1s

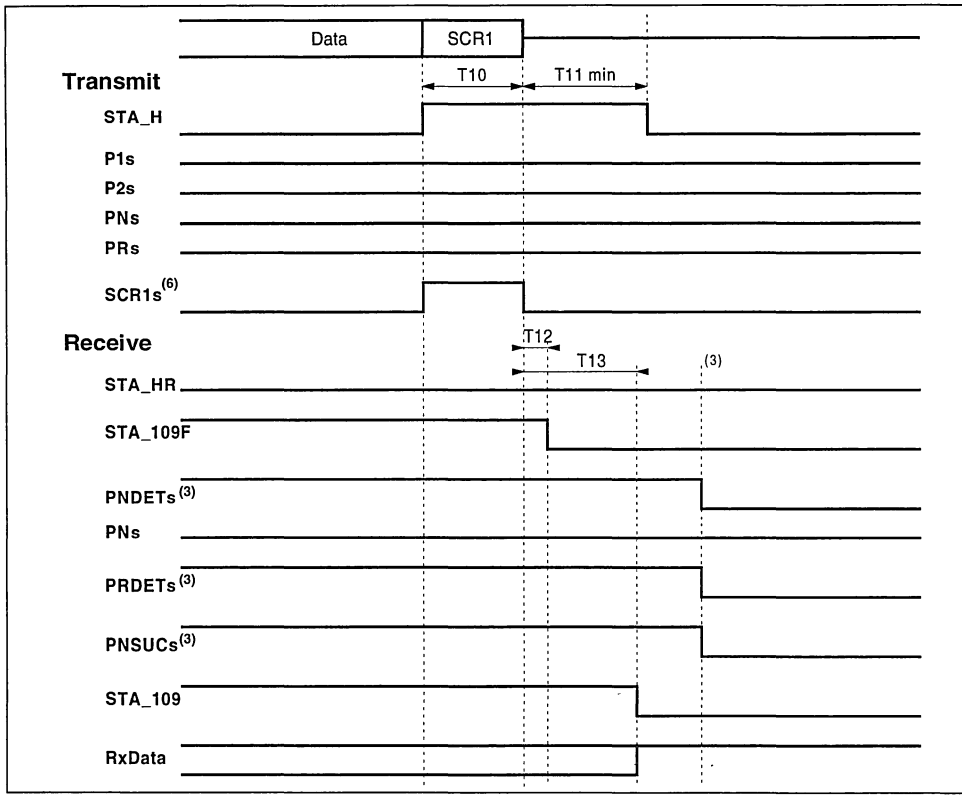
Notes : 1. SPVAL is active in V.33 receiver only at the same time as the rising transition of the SCR1s signal. Went SPVAL is set, it indicates that the SPEED bits contain the data speed information.
2. SPEED is valid in V.33 receiver only. It can have 2 values, after the SCR1s signal goes high : 1000 for 14400bps and 0111 for 12000bps.
3. The STAOP2 bit reflects the progression of the synchronization. The STAOP2 bits have the following meaning :

Name	Position	Description	Tx	Rx
P1s	0	Unmodulated carrier sequence. Optional, used for echo protection.	X	
P2s	1	Continuous 180° phase reversal sequence	X	X
PNs	2	Equalizer trainning sequence	X	X
PRs	3	V.33 and V.17 rate sequence	X	
SCR1s	4	Continuous scrambled 1 sequence	X	X
PNDETs	5	Turned on after PN sequence detection		X
PRDETs	6	Turned on after PR sequence detection (V.33 and V.17 only)		X
PNSUCs	7	Turned on after succesfull training of the receive equalizer. When on at the end of the synchronization, the transmition BER is statisticaly bellow 10ppm.		X

With the following timing :



Mode	T1 (4)	T1p (5)	T2	T3	T4	T5	T6	T7	T8	Unit
V.17	192	30	22	107	1240	27	20	5	7	ms
V.17 short	192	30	22	107	16	0	20	5	7	ms
V.29	192	30	22	53	160	0	20	5	7	ms
V.29 short	192	30	22	41	26	0	8	5	7	ms
V.27 4800	192	30	22	31	670	0	5	5	7	ms
V.27 4800 short	192	30	22	9	36	0	5	5	7	ms
V.27 2400	192	30	22	42	895	0	7	6	7	ms
V.27 2400 short	192	30	22	12	48	0	7	6	7	ms



Mode	T10	T11	T12	T13	Unit
V.17	13	20	8	25	ms
V.17 short	13	20	8	25	ms
V.29	13	20	8	25	ms
V.29 short	13	20	8	25	ms
V.27 4800	20	30	8	25	ms
V.27 4800 short	20	30	8	25	ms
V.27 2400	27	40	8	25	ms
V.27 2400 short	27	40	8	25	ms

Notes : 1. In the case of V.29 or V.27, PRs and PRDETs bits are not active.
2. PNSUCs indicates the quality of the Rx signal that will give a ber of approximation of $1e^{-5}$.
3. After sending the command SYNC0, all bits are reset.
4. When using long echo protection tone, otherwise 0.
5 When using short echo protection tone, otherwise 0.
6. STA-106 is set at the end of T6 and reset at the beginning of T10.
7. After sending the command SYNC1, this bit is set.

VIII - TONE DETECTORS

VIII.1 - Overview

The general purpose TS75C520 tone detectors block is a powerful module that covers a lot of applications :

- call progress tone detection, fully programmable for all countries,
- DTMF detection,
- FAX, voice, data automatic detection,
- call waiting detection, while in voice or data mode.

VIII.2 - Description

The tone detector block is a set of 16 identical Cells. Each cell is composed of a Double Biquadratic Filter, a Power estimator section, a Static level and a Level comparator.

Each Biquadratic Filter, Power Estimator and Static Level can be programmed using a complete set of Commands (**TDRC**, **TDRW**, **TDWC**, **TDWW**, **TDZ**).

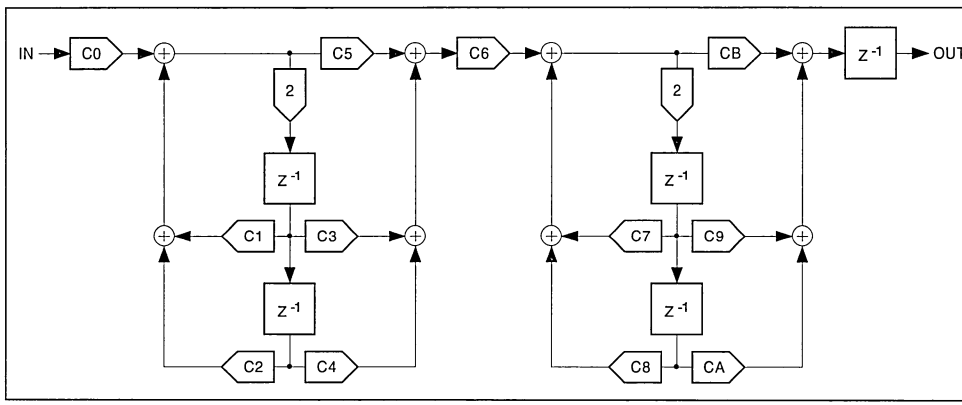
The wiring between the different Cells can be defined by the user, using the associatedCommand allowing a wide range of applications.

The 16 Comparator Outputs give, on a baud basis, the information into two 8 bits words **TONEDET0** (for cells number 0 to 7) and **TONEDET1** (for cells number 8 to F). These TONEDET variables can be accessed using a **MR** command or, more easily, monitored on a baud basis using the **DOSR** command.

VIII.2.1 - Biquadratic Filters

Each Biquadratic Filter is a double regular section that can perform any Transfer function with 4 Poles and 4 Zeros. This routine is run on a sample basis.

Figure 2 : Biquadratic IIR Filter



The corresponding transfer function is :

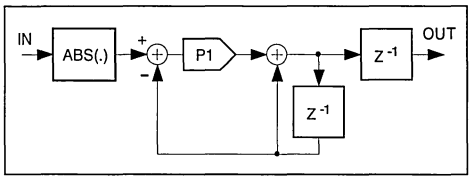
$$\frac{Out}{Input} = C0 \cdot \frac{C5 + 2 \cdot C3 \cdot z^{-1} + 2 \cdot C4 \cdot z^{-2}}{1 - 2 \cdot C1 \cdot z^{-1} - 2 \cdot C2 \cdot z^{-2}} \cdot C6 \cdot \frac{CB + 2 \cdot C9 \cdot z^{-1} + 2 \cdot CA \cdot z^{-2}}{1 - 2 \cdot C7 \cdot z^{-1} - 2 \cdot C8 \cdot z^{-2}} \cdot z^{-1}$$

Note : All coefficients are coded on 16 bits 2's complement in the range +1, -1 (Q15). To avoid the possibility of overflow the user must check that the internal node must not be higher that 0 5 (in Q15 representation).

VIII.2.2 - Power Estimation

The Power estimation Cell is needed to measure the amplitude of the different tones. It is run on a sample basis.

Figure 3 : Power Estimator



The corresponding transfer function is :

$$Out = |Input| \cdot z^{-1} \cdot \frac{P1}{1-(1-P1)\cdot z^{-1}}$$

VIII.2.3 - Static Level

A single Threshold level is associated with each Cell. It can be use to compare the output of a Power Estimation with an Absolute Value.

VIII.2.4 - Comparator

The Comparator computes, on a baud basis, the difference of the signal on its Positive and Negative Inputs. If the result is Higher that zero it sets the corresponding bit into the TONEDET[0..1] word; if not it clear this bit.

VIII.2.5 - Wiring

The user must specify the connection (wiring) between the input/output of the Filter, the input/output of the Power estimator, the output of the static levels and the two inputs of the Comparators.

The output signals have an absolute address:

Node Address		
Signal Name	**Address**	**Description**
Ground	00	Signal always equal to 0000
RxSig	01	Receive signal from the Analog front end
RxSig2	02	Receive signal multiplied by 2
RxSig4	03	Receive signal multiplied by 4
	04..0F	Reserved
Filter[0..F]	10..1F	Biquadratic Filter Outputs
Power[0..F]	20..2F	Power Estimator Outputs
Level[0..F]	30..3F	Static Levels

The user will specify the inputs of the filters, Power and Comparator. At least one input must come from the RxSig (node 01, 02 or 03). It is mandatory to connect all unused cell inputs to the Ground signal (node 00).

Figure 4 : Tone Detector Wiring Address (first half)

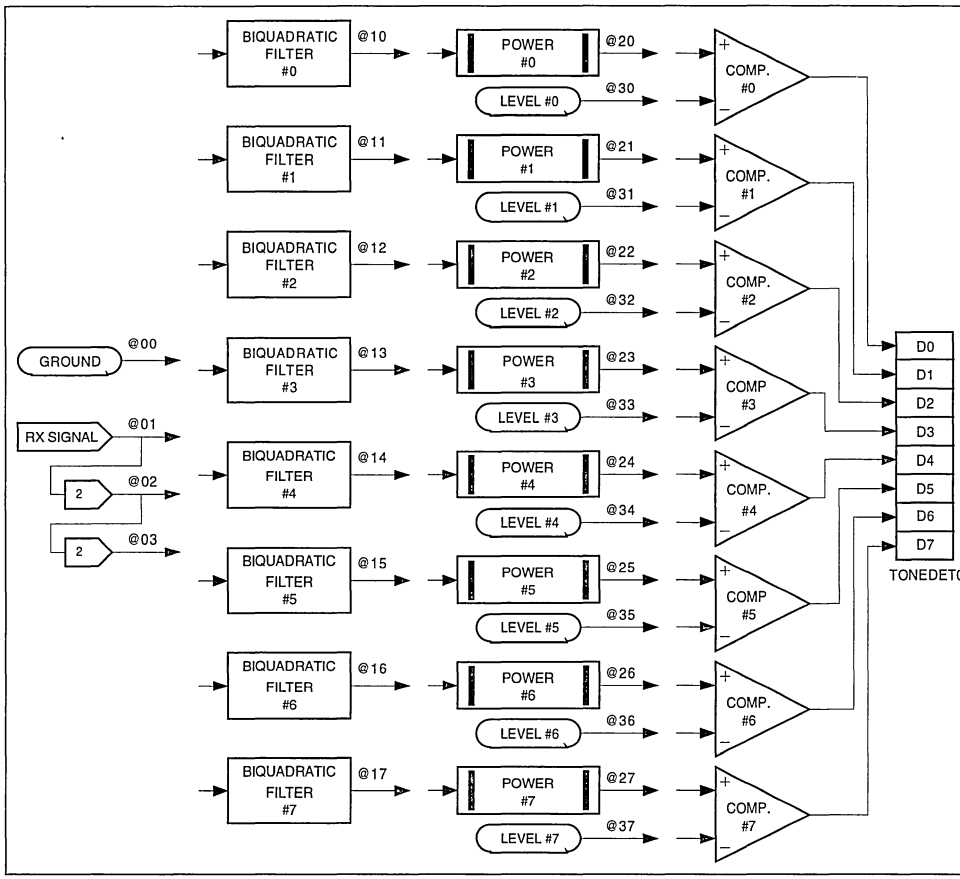
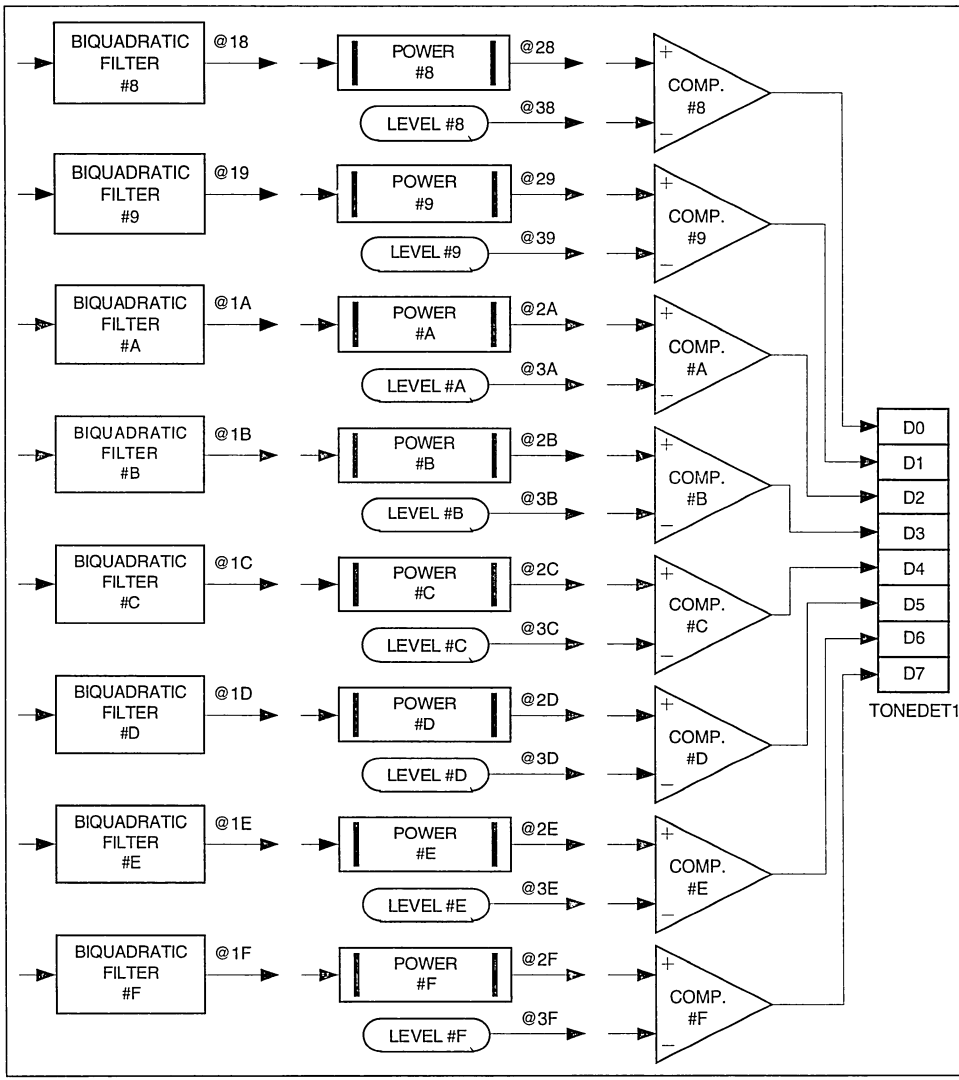


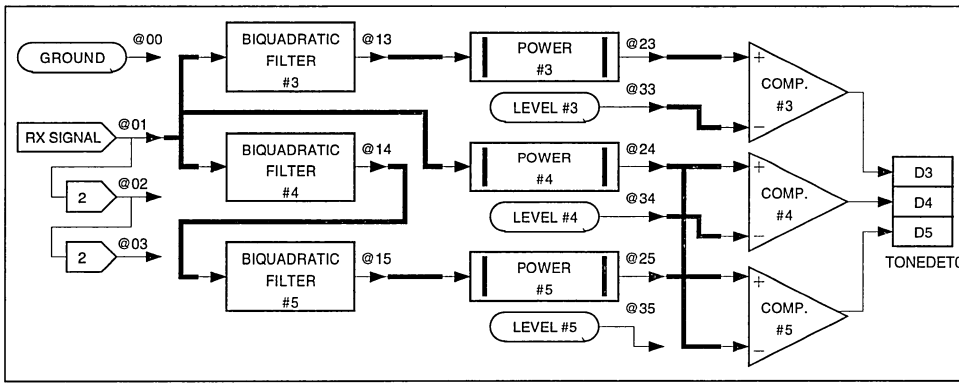
Figure 5 : Tone Detector Wiring Address (second half)



VIII.3 - Example

Hereunder is an example of programming a single Tone detection (using Cell #3) and a complex differential tone detection (using Cell #4 and #5).
Bit 3 of the TONEDET variable will be triggered each time the energy of that filtered signal is higher than Static Level number 3.
Bit 4 of the TONEDET variable will be on each time a receive signal has an energy higher than the Static Level number 4. Bit 5 will be on only when the Filtered (Filter section 4 and 5) received signal higher than the energy of the wide-band signal number 4 ; this prevents triggering on noise.

Figure 6 : Wiring Example



Program Cell #3 :

TDWW	**03**	**00**	**13**	**01**

Connect Received signal to Filter and Filter to Energy.

TDWW	**03**	**01**	**33**	**23**

Connect Level to Comparator Neg Input and Energy to Pos Input.

Program Cell #4 and #5 :

TDWW	**04**	**00**	**01**	**01**

Connect Received Signal to Filter and Energy.

TDWW	**04**	**01**	**34**	**24**

Connect Level to Comparator Neg Input and Energy to Pos Input.

TDWW	**05**	**00**	**15**	**14**

Connect Filter#4 Output to Filter and Filter to Energy.

TDWW	**05**	**01**	**24**	**25**

Connect Wide-band Energy to Neg Input and Energy to Pos Input.

IX - BUFFER OPERATIONS

IX.1 - Introduction

This appendix is dedicated to buffer operation, either the data buffers used in data exchanges or in particular Modes (like Voice).

The first part is oriented towards a functional description of the buffer operation, while the second section is more oriented towards the management of the buffers.

IX.2 - Receive Operations Overview

Figure 7 describes the receive data flow.

The ST75C520 can handle the following types of format for the data :

- parallel synchronous mode : 8-bit words are synchronously available in the receive buffers. The buffer status holds the number of valid bytes received,
- parallel HDLC framing mode : 8-bit data is available in the receive buffers. Framing information (like flags, CRC, additional "0") is interpreted by the ST75C520 and reported when necessary in the receive buffer status (CRC error, aborted frame, framing error, etc). This feature greatly eases the implementation of protocols as well as FAX data management.

Each time the receive deframer has filled up a new buffer, it sets the corresponding flag with the proper status then generates the IT3 interrupt. The availability of the buffers is tested just before starting to fill them. This further means that the host must not perform any buffer operation on the data part while the status remains 0.

IX.3 - Transmit Operations Overview

Figure 8 describes the transmit data flow. The following modes are available :

- parallel synchronous mode : 8-bit words are synchronously read from the transmit buffers. The transmit status buffer holds the number of valid bytes to be transmitted (up to 8 per buffer),
- parallel HDLC framing mode : 8-bit data is received from the transmit buffers. Framing information (frame open, frame close, frame abort, number of byte per buffer) is carried by the transmit buffer status and processed by the ST75C520. CRC, padding and other operations are automatically handled by the ST75C520.

Each time the transmit framer has emptied a buffer, the IT2 interrupt is raised.

Figure 7 : Rx Buffer Schematics

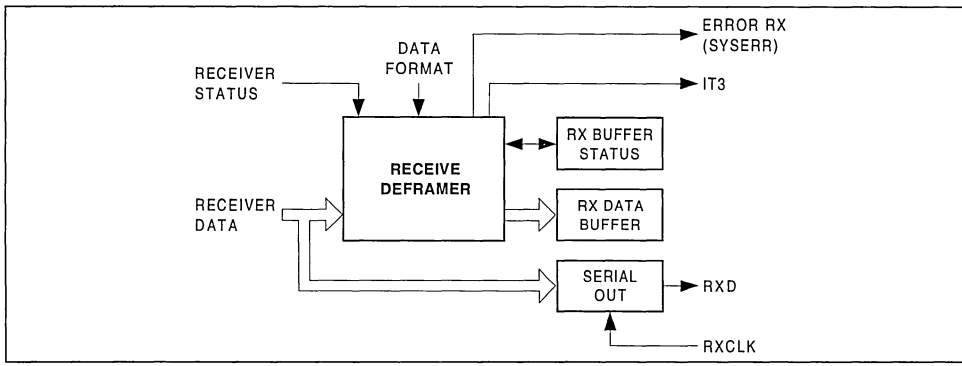
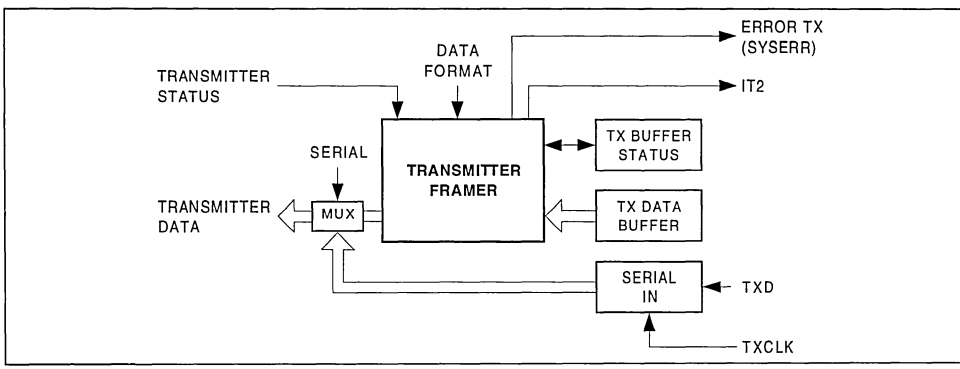


Figure 8 : Tx Buffer Schematics



IX.4 - Buffer Status and Format Description

The following section describes the meaning and use of the buffer status words.

IX.4.1 - Transmit Buffer

The transmit buffer status words are DTTBS0 and DTTBS1 (see the **Host Interface Summary** section in the main document) and are more likely to be seen as control words. These words must be set by the host and are reset by the ST75C520. The data buffer exchanges are synchronized through these status words, (see Buffer Status and format description) an improper setting will trigger the error Err_Tx in the error status SYSERR. A value of 0 for DTTBS0 or DTTBS1 means that the corresponding buffers are empty : this value is written by the ST75C520. The unused bits of DTTBSx must be set to 0 by the host.

In FSK Mode, when working in the parallel data mode, the transmitter expands each bit to the nominal baud time (1200Hz/300Hz/75Hz).

IX.4.2 - Synchronous Mode

Field	Pos.	Val.	Description
BUFF_LENG	3..0	1..8	Number of valid bytes in the buffer

IX.4.3 - HDLC Framing Mode

Field	Pos.	Val.	Description
BUFF_LENG	3..0	1..8	Number of valid bytes in the buffer
BUFF_SFRM	4	0 1	Data stream Start of frame
BUFF_EFRM	5	0 1	Data stream End of frame
BUFF_FRAB	6	0 1	Normal process Abort frame (no data in buffer)

IX.5 Receive Buffer

The receive buffer status words are DTRBS0 and DTRBS1 (see the **Host Interface Summary** section in the main document). These flags are set by the ST75C520 and must be reset by the host. The data buffer exchanges are synchronized through these status words, an improper resetting will trigger the error Err_Rx in the error status SYSERR. A value of 0 for DTRBS0 or DTRBS1 means that the corresponding buffers are empty : this value must be written by the host.

In FSK or V.21 Channel 2 Mode, when working in the parallel data mode, the receiver extract each bit using the nominal baud rate (1200Hz/300Hz/75Hz).

IX.5.1 - Synchronous Mode

Field	Pos.	Val.	Description
BUFF_LENG	3..0	1..8	Number of valid bytes in the buffer

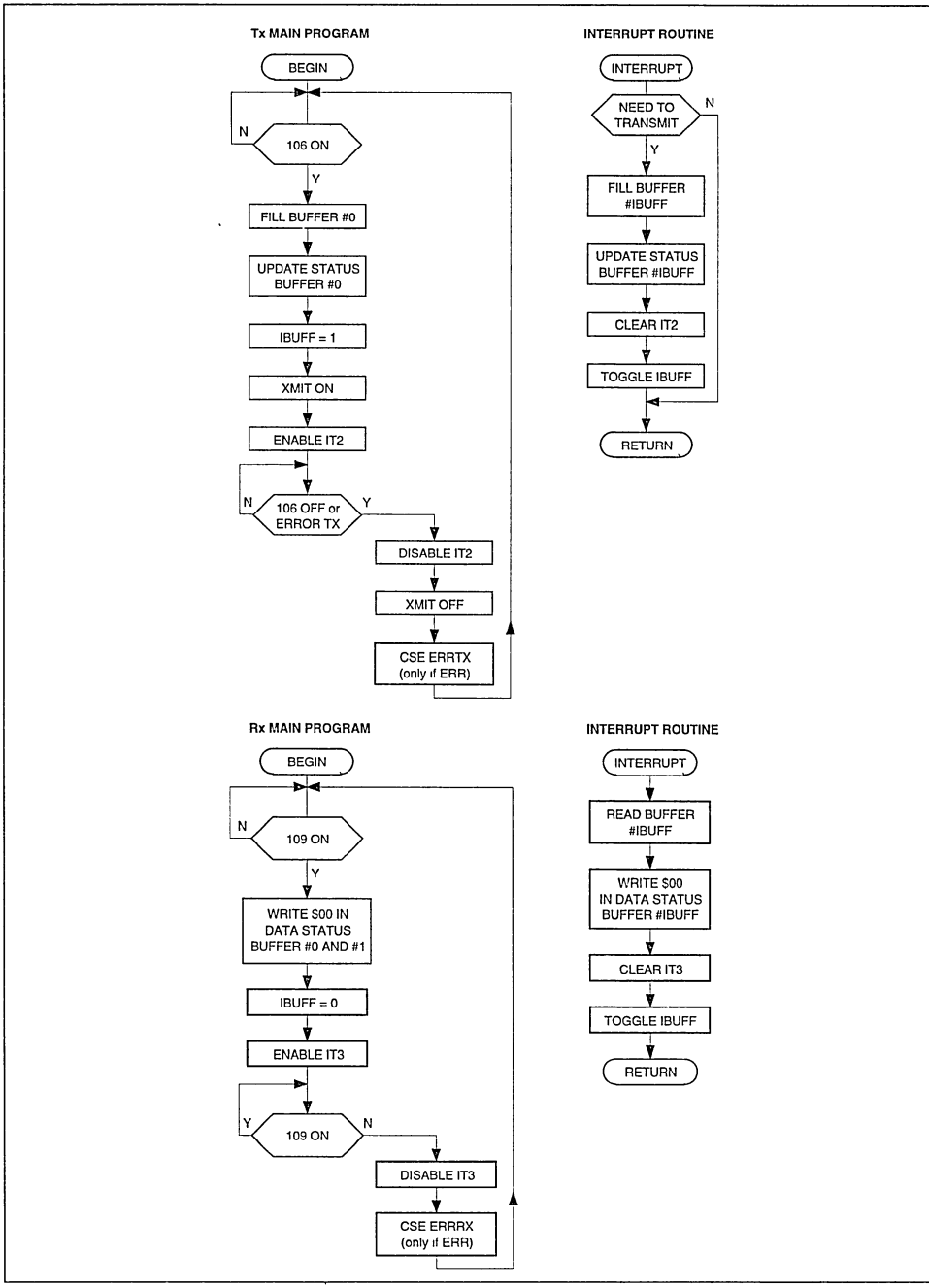
IX.5.2 - HDLC Framing Mode

Field	Pos.	Val.	Description
BUFF_LENG	3..0	1..8	Number of valid bytes in the buffer
BUFF_ERRS	5..4	00 01 10 11	No error CRC error Non byte-aligned frame Aborted frame
BUFF_SFRM	6	0 1	Data stream Start of frame
BUFF_EFRM	7	0 1	Data stream End of frame

IX.6 - Data Buffer Management

Figure 9 shows the general flow chart for transmit data buffer management. In the transmit path, the data buffer exchanges should always begin with the filling of buffer 0, then with the update of the buffer 0 status word. The initiation of the data exchanges is initiated then with the **XMIT** command.

Figure 9 : Buffer Operations Synchronization



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X - DEFAULT CALL PROGRESS TONE DETECTORS

Figure 10 : Call Progress Tone Detector Band 1

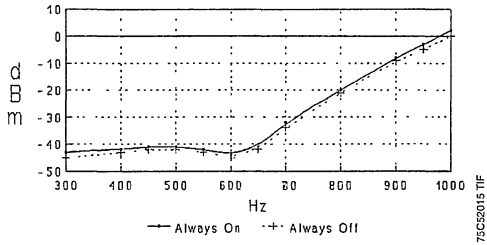
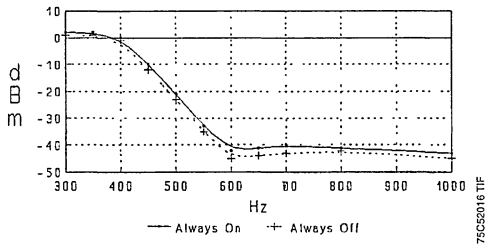


Figure 11 : Call Progress Tone Detector Band 2



XI - DEFAULT ANSWER TONE DETECTORS

Figure 12 : 2100Hz Answer Tone Detector

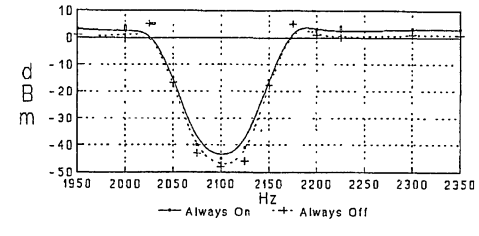
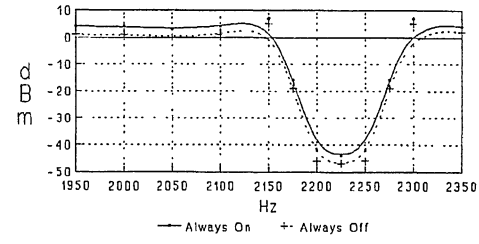


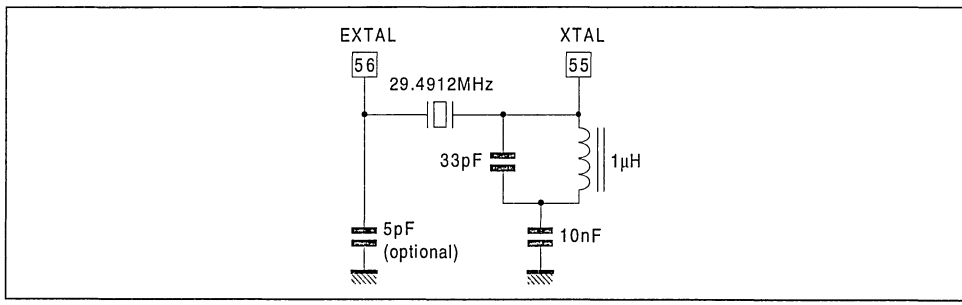
Figure 13 : 2225Hz Answer Tone Detector



XII - ELECTRICAL SCHEMATICS

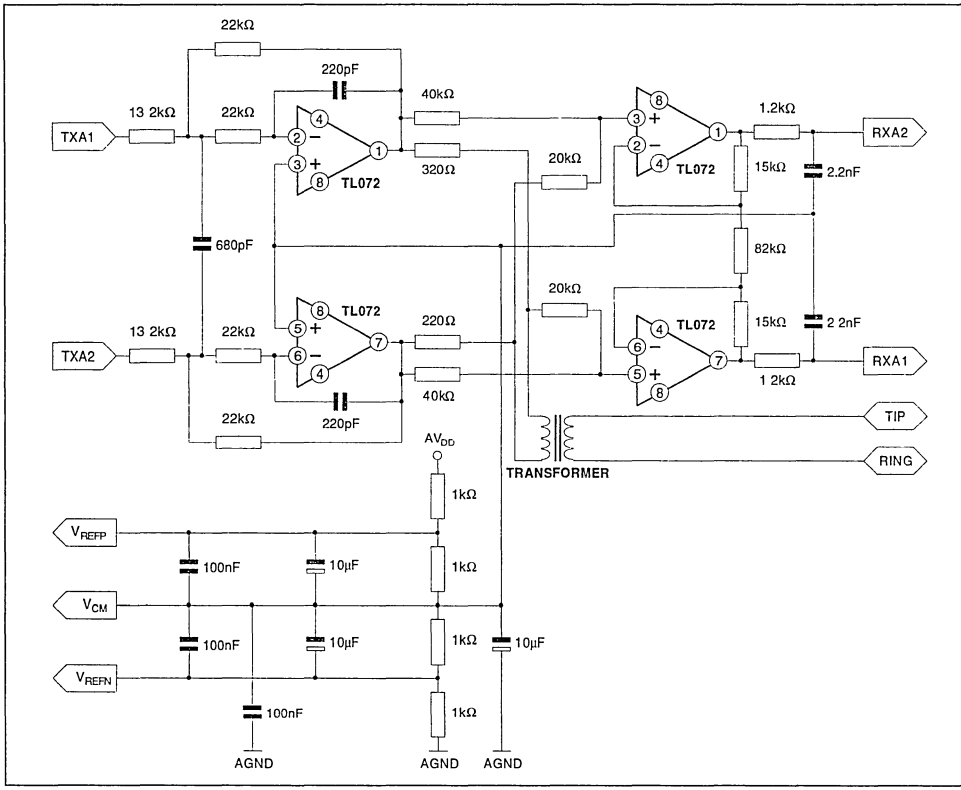
Oscillator

When using a third harmonic crystal oscillator in series resonance mode ($R_S < 40\Omega$, $C_0 = 6pF$, $P_e = 0.1mW$), we recommend the following schematic :



XII - ELECTRICAL SCHEMATICS (continued)

Figure 14



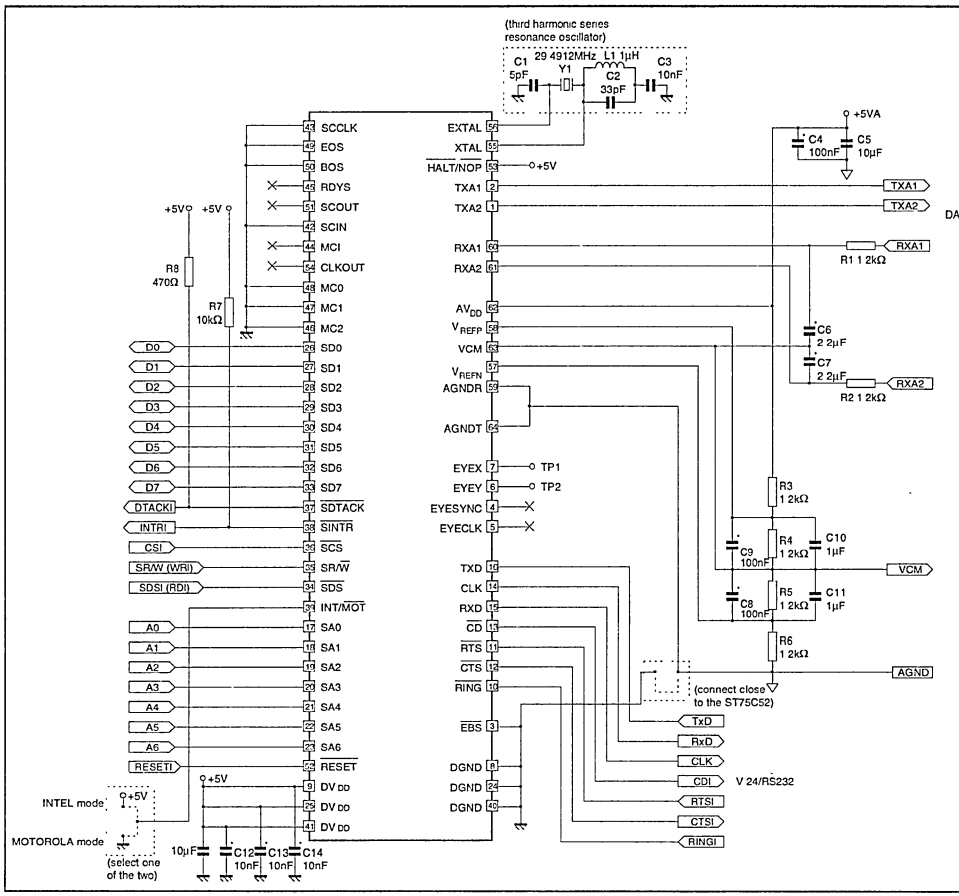
XIII - PCB DESIGN GUIDELINES

Performances of the FAX modem depends on the ST75C520 intrinsic performances and on the proper PC board layout. All aspects of the proper engineering practices, for PC board design, are beyond the scope of this paragraph.

We recommend the following points :

- in a 4-layer PC board :
  Separated digital ground and analog ground, connected together at one point, as close as possible to the ST75C520,
- in a 2-layer PC board :
  Provide a ground grid in all space around and under components on both sides of the band and connect to avoid small islands,
- both AGNDR and AGNDT must be connected with very low impedance to a single point, (see Chapter I.7, Power Supply),
- the two 2.2nF capacitors connected to the RXA1 and RXA2 Pins must be as close as possible to them,
- the two 100nF capacitors connected to the V_{REFP} and V_{REFN} pins must be as close as possible to them,
- analog and digital supplies must be connected together, at a single point, as close as possible to the chip (see Chapter I.7, Power Supply).

TYPICAL APPLICATION



Notes : All capacitor with a "*" must be implanted close to the ST75C520 pin.
All signal name ending with a "1" are active low.
R3, R4, R5, R6 are needed if the hybrid will sink a current on V_{CM}.

ST75C52 - ST75C520

SUMMARY

I - PRELIMINARY

The ST75C52/520 includes FAX, modem and voice modes.

In FAX mode the chip works as a G3 synchronous half-duplex modem including all the possibilities to work on the public telephone networks. With a microcontroller (such as SANYO LC82141) a complete G3 facsimile system can be built including all the functions (image processor, motor interface, PIO...). Tones can be sent or detected using programmable tone generators and detectors.

In Modem mode FSK full-duplex communications using V.23, V.21, Bell 103 modulation/demodulation on PSTN or leased lines are possible.

In voice mode the user can record or send messages using PCM A-law standard.

Tones (DTMF...) can be sent and/or detected.

This component satisfies the communication requirements specified in ITU-T recommandations V.33 (1), V.17, V.29 (T104), V.27 ter (with short train), V.21 ch2, V.21, V.23, or Bell 103 and communication at a data rate of 14400, 12000, 9600, 7200, 4800, 2400, 300, 1200/75 is possible.

Convention :

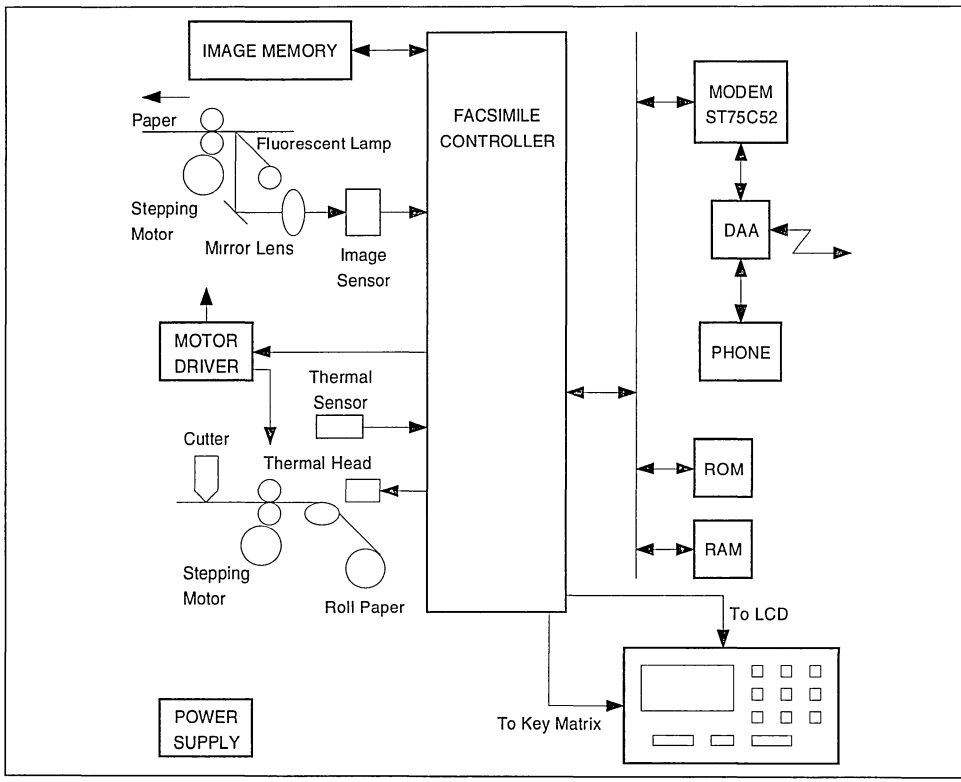
- default value or parameter will be followed by a *,
- all addresses are in hexadecimal,
- all numbers starting with a $ are hexadecimal, % are binary numbers, others are decimal numbers,
- bold italic words refer to key words used in the ST75C52/520 Data Sheet.

Note 1 : The ST75C52/520 only supports V.33 in a half duplex mode.

I.1 - FAX Architecture

The Figure 1 is an example of facsimile system (using thermal printer type) built with the ST75C52/520.

Figure 1



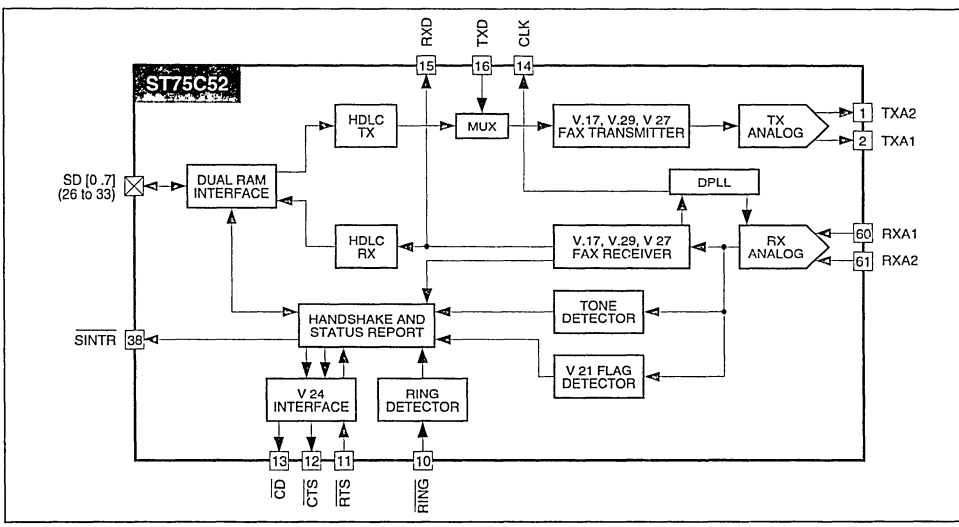
II - FEATURES

II.1 - Basic Functions

The ST75C52/520 provides the following functions :

- modulations for FAX implementation : ITU-T V.17, V.29, V.27 ter, V.21 ch2,
- basic low speed full duplex FSK modulations for special applications (VIDEOTEX, ...) : ITU-T V.23, V.21 and BELL 103,
- high speed modulations for faster FAX equipments : V.17, V.33 with the possibility to use the standard carrier frequency of 1800Hz or an optional frequency of 1700Hz,
- the optional short train sequence can be used in V.17 (for FAX equipment), V.29 (T104) recommendation) and V.27 ter for high speed VIDEOTEX application,
- integrated implementation on one single Digital Signal Processor (DSP) chip including intergrated Delta Sigma Modem Analog Front End (MAFE),
- single 5V power supply,
- a low power mode provides the possibility to reduce the power consumption till 5mW (typ),
- the DSP firmware allows a lot of operations such as :
  - full implementation of the V.17,V.33,V.29, V.27 ter handshakes,
  - real time status monitoring and full diagnostic capability,
  - auto dial and auto answer capability,
  - programmable tone detection and FSK V.21 flag pattern detection during high speed reception,
  - programmable call progress and call waiting tone detectors including DTMF,
  - programmable tone generators (DTMF and others),
  - programmable class detection capability,
  - voice mode using A-law to record or send messages,
  - full implementation of the HDLC protocol.
- the analog interface provides a wide dynamic range (> 48dB),
- initialisation and managment of the ST75C52/520 with commands given though the Dual Port Ram (DPR) interface,
- a versatile User Interface proposes different possibilities :
  - data transmission/reception with serial interface or with parallel interface,
  - parallel mode in synchronous transparent mode or in HDLC mode using in both cases 2x8 bytes data buffer in transmission and 2x8 bytes data buffer in reception,
  - connection with 8-bit data processor (both MOTOROLA or INTEL timing),
  - synchronization between the ST75C52/520 and the host processor by using interruption mode for different functions (transmission, reception, error detection, status managment, command acknowledge),
  - two 8-bit DACS for constellation display without any external components.

Figure 2 : Functional Diagram



II.2 - System Architecture

Figure 3 shows the basic connection between the ST75C52/520 and the different elements : telephone line interface, processor, synchronous/asynchronous serial, ...

Power

The modem/fax chip requires only one +5V Digital and Analog supply.

Hybrid and Telephone Line Interface

The sigma delta convertor provides the carrier on ***TxA1*** and ***TxA2***. The far end carrier will be received on ***RxA1*** and ***RxA2***. Both transmit and receive path are differential for better performance at low level. A hybrid interface must be used to connect the analog interface to the telephone line interface. At this point the hybrid interface and the line interface will be adjusted to meet the different technical requirements in each country (for example the reference impedance for the return loss can be real or complex, DC current features will be different ...). The incomming call detection could be easily facilitated using the ***RING*** detection of the ST75C52/520.

Serial Interface

Data communications in both half duplex and fullduplex modes are possible using the serial interface. The serial interface is optional since all the operations can be done through the DPR in parallel mode.

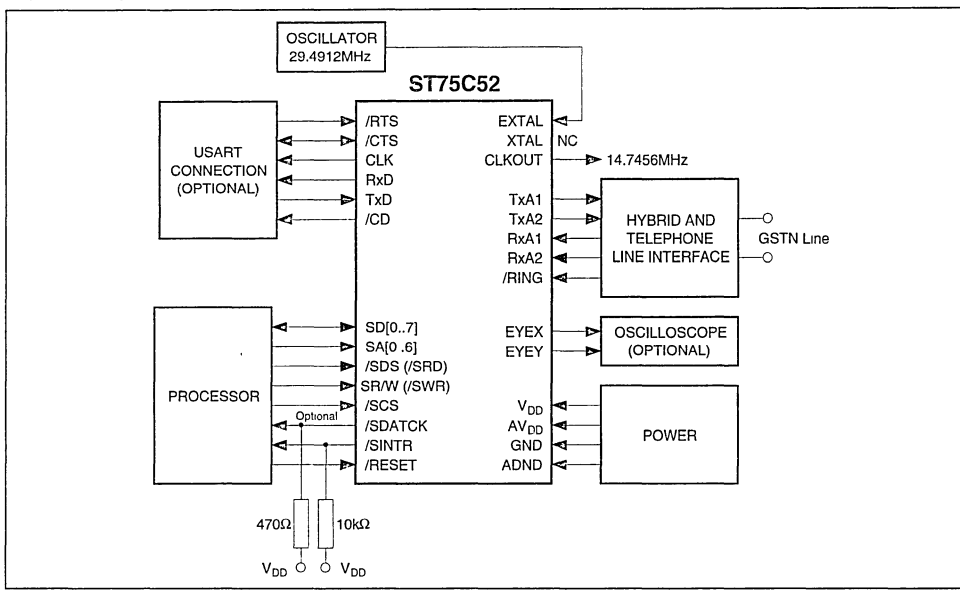
Processor Interface

Signals provide the possibility to use 8-bit data processors with both mode MOTOROLA and INTEL type. The processor can control the hardware initialisation with the ***RESET*** Pin. synchronization during read or write access are done with the ***SDTACK*** signal. Main program processor can be interrupted for special or priority purpose (data reception, status change...) with the ***SINTR*** signal. Both ***SDTACK*** and ***SINTR*** are open drain signals (external resistors must be installed) and must be tied to V_{DD} with 10kΩ for ***SINTR*** and 470Ω for ***SDTACK***.

Oscillator

The ST75C52/520 provides the possibility to use a crystal on ***EXTAL*** and ***XTAL*** pin or an external oscillator can be used and connected to ***EXTAL*** pin. The nominal value is CLK = 29.4912MHz. When using a crystal we recommend to install a third harmonic quartz which is cheaper than a fundamental quartz. ***CLKOUT*** gives the internal ST75C52/520 (14.7456MHz or CLK/2).

Figure 3 : System Connection



II.3 - Operations

In this chapter we remind the user the main operations performed with the ST75C52/520.
Refer to the others chapters for more details.

II.3.1 - Modulation Method, Transmission Speed, Carrier Frequency

The modem implementation is fully compatible with current FAX modulation recommendations.
The modulation can be either Trellis Coded Modulation (TCM) as in V.17 14400, 12000, 9600, 7200 bps rates, Quadrature Amplitude Modulation (QAM) as in V.29 9600, 7200, 4800 and Differential Phase Shift Keying (DPSK) as in V.27 ter 4800 and 2400bps rates.
Frequency Shift Keying (FSK) modulations are also supported for V.21 ch2 300bps rate, full duplex V.21 300/300bps rates, full duplex V.23 75/1200 and 1200/75bps rates and BELL 103 300/300bps rate.

The Table 1 summarizes the different modes with their features.

II.3.2 - Transmitter Description

Data coming from the Data Terminal Equipment (DTE) both in parallel mode or in serial mode pass through the following modules shown on the Figure 4.

The different steps in transmission are :
- scrambling the data (scrambler block),
- coding the scrambled information (Diff encoder and trellis encoder block),
- conversion from real encoded data to complex encoded data (Signal mapping block),
- pulse shaping in a dedicated filter to avoid symbol interference (Pulse shaping block),
- modulation over the required carrier. After that we keep the real part of the signal,
- improve performance by using compromise equalizer (Comp equalizer block). Three compromise equalizers are available,
- selection of transmit gain,
- digital to analog conversion with a sigma delta convertor (D/A block).

II.3.3 - Receiver Description

The received carrier coming from the line is passed through the following modules showed in the Figure 5.

The different steps in reception are :
- analog to digital conversion with a sigma delta convertor (A/D block),
- filtering of the received information (RCV filter block) with result given on complex format,
- automatic control of the gain in reception (AGC block),
- equalization due to line impairment (equalizer block),
- slicer which gives real data for the decoder,
- decoder using first a Viterbi decoder (Viterbi decoder block) and second a differential decoder (diff decoder block),
- descrambling the data to obtain the initial sent data.

Table 1

Mode	Modulation	Carrier Frequency in Hz	Data Rate in bps ± 0/01%	Baud or Symbols/Sec	Bits per Symbol	Constellation Points
V.33/V.17 14400	TCM	1700 (2) 1800 (1)	14400	2400	6	128
V.33/V.17 12000	TCM	1700 (2) 1800 (1)	12000	2400	5	64
V.17 9600	TCM	1700 (2) 1800 (1)	9600	2400	4	32
V.17 7200	TCM	1700 (2) 1800 (1)	7200	2400	3	16
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.29 4800	QAM	1700	4800	2400	2	4
V.27ter 4800	DSPK	1800	4800	1600	3	8
V.27ter 2400	DSPK	1800	2400	1200	2	4
V.21 High	FSK	1650,1850	300	300	1	-
V.21 Low	FSK	980,1180	300	300	1	-
V.23 High	FSK	1300,2100	1200	1200	1	-
V.23 Low	FSK	390,450	75	75	1	-
V.21 ch2	FSK	1650,1850	300	300	1	-

Notes : 1. ITU-T recommended carrier
2. Optional carrier

Figure 4

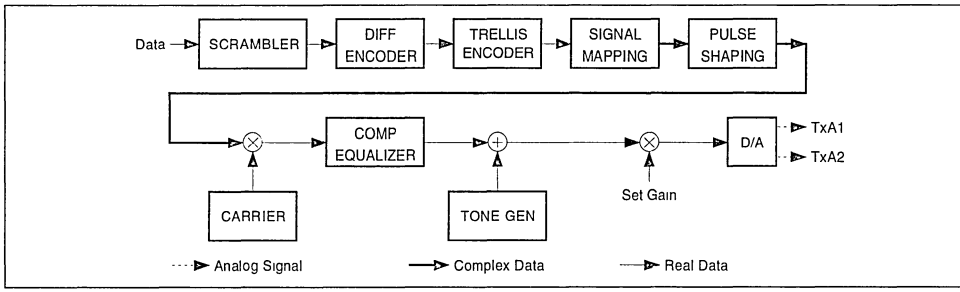
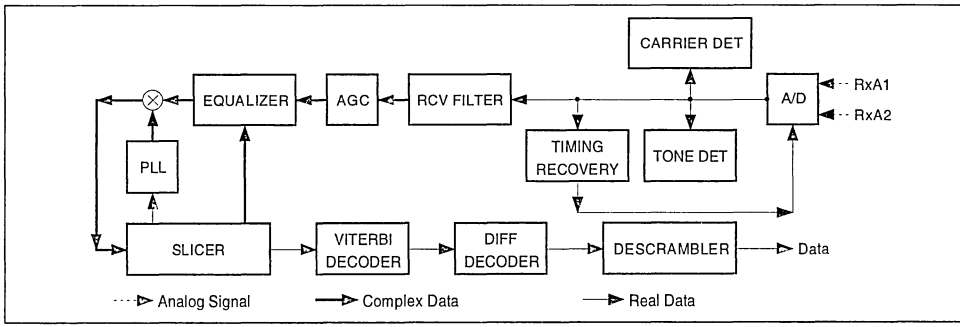


Figure 5



II.3.4 - Tone Generator Description

Four tones can be simultaneously generated by the ST75C52/520. The tones are determined by their frequencies and by the output amplitude level. A set of specific commands is also available for DTMF generation (using two of the four generators available).

II.3.5 - Tone Detector Description

Sixteen tones can be simultaneously detected by the ST75C52/520. Each of the tones to be detected is defined by the coefficients of a 4th order programmable IIR filter. Detection thresholds are also programmable from -45dBm up to -10dBm. DTMF detection is also available and is performed by a specific filter section that requires no programming.

II.3.6 - DTMF Detector Description

A DTMF Detector is included in the ST75C52/520, it allows detection of valid DTMF Digits. A valid DTMF tone is defined as a dual Tone with a total power higher than -35dBm, a duration higher than 40ms and a differential amplitude within 8dB (negative or positive).

II.3.7 - Voice Mode

The ST75C52/520 voice mode allows the implementation of enhanced telephone functions like answering machines. The incoming voice is sampled at a rate of 9600Hz. The samples, received from the line are PCM A-law coded and written into the dual port RAM. The outgoing samples are decompressed using the same A-law and output to the telephone line.

II.3.8 - Analog Loop Back Test Mode

In any transmission standard and serial data format, the ST75C52/520 can be configured for analog loop back test. This mode of operation is for test purposes only.

II.3.9 - Low Power Mode

A sleep state can be obtained by a ***SLEEP*** command. This is very interesting to reduce power consumption when no activity is detected by the processor in charge of the fax system equipment. The ST75C52/520 can be awakened with the ***RESET*** signal or the ***RING*** signal, or a dummy write into the Dual Port Ram. An interruption can be sent by the ST75C52/520.

The ST75C52 can only be awakened with the ***RESET*** signal.

II.3.10 - Reset

After a hadware reset, or an ***INIT*** command, the ST75C52/520 clears all its internal memories, clears the whole dual RAM and starts to initialize the delta sigma analog convertors. As soon as these initialization are completed, the ST75C52/520 clears the dual RAM address 0 (***COMSYS***), generates an interrupt ***IT6*** **(command acknoledge)** and is programmed to send and receive tones, the bit clock and the sample clock are programmed to 9600Hz. The total duration of the reset sequence is about 5ms. After that time the ST75C52/520 is ready to execute commands sent by the host micro-controller.

We suggest that the ***RESET*** signal is managed by the host micro-controller using a general purpose output port. In such a case the ***RESET*** signal could be equal to 0 till the micro-controller initialize it to 1 at the entry point of the main program, and software initialization could be done both by the ***RESET*** or the ***INIT*** command.

For a hardware reset the signal ***RESET*** must be tide to GND at least 700ns (see Figure 6).

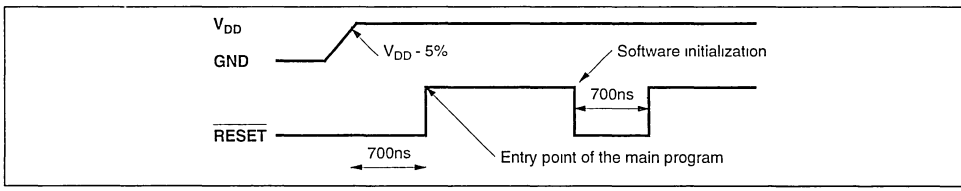
II.3.11 - Analog Interface

The modem designer must provide a proper hybrid interface to the ST75C52/520. Analog hybrid examples are given in this User's Manual. The inputs and the outputs of the MAFE are differential, achieving thus a better noise immunity. The D/A converter output amplifier includes a single pole low-pass filter, its cut-off frequency is : Fc -3dB # 19200Hz.
Continuous-time filtering of the analog differential output is necessary using an off-chip amplifier and a few passive components.

II.3.12 - Host Interface

The host interface is seen by the micro-controller as a 64x8 RAM, with additional registers accessible through a 7-bit address space. A selection pin (***INT/MOT***) allows to configure the host bus for either INTEL or MOTOROLA type control signals.

Figure 6



Note : The interrupt registers ITMASK and ITSRCR are not changed by an ***INIT*** command.

II.4 - Hardware Block Diagram

Figure 7

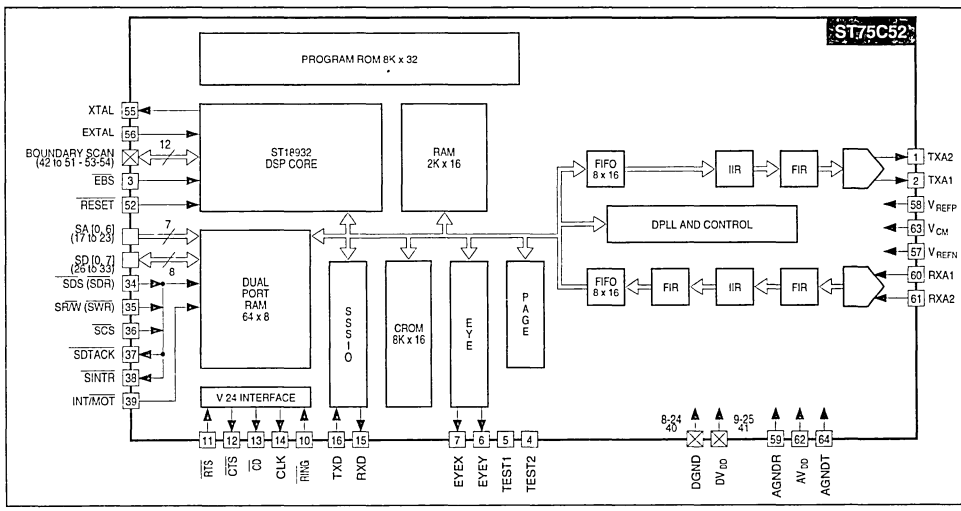


Table 2 : Pin Connections

Pin Name	Type	Pin Number
TxA2	Output	1
TxA1	Output	2
$\overline{EBS}$	Input	3
TEST2	To be left open	4
TEST1	To be left open	5
EYEY	Output	6
ETEX	Output	7
GND	Ground	8
V_{DD}	Digital +5V	9
$\overline{RING}$	Input	10
$\overline{RTS}$	Input	11
$\overline{CTS}$	Output	12
$\overline{CD}$	Output	13
CLK	Output	14
Rxd	Output	15
TxD	Input	16
SA0	Input	17
SA1	Input	18
SA2	Input	19
SA3	Input	20
SA4	Input	21
SA5	Input	22
SA6	Input	23
GND	Ground	24
V_{DD}	Digital +5V	25
SD0	Input / Output	26
SD1	Input / Output	27
SD2	Input / Output	28
SD3	Input / Output	29
SD4	Input / Output	30
SD5	Input / Output	31
SD6	Input / Output	32

Pin Name	Type	Pin Number
SD7	Input / Output	33
$\overline{SDS}$ (SRD)	Input	34
SR/$\overline{W}$ ($\overline{SWR}$)	Input	35
$\overline{SCS}$	Input	36
$\overline{SDTACK}$	Output open Drain	37
$\overline{SINTR}$	Output open Drain	38
INT/$\overline{MOT}$	Input	39
GND	Ground	40
V_{DD}	Digital +5V	41
SCIN	Input	42
SCCLK	Input	43
MCI	Output	44
RDYS	Output	45
MC2	Input	46
MC1	Input	47
MC0	Input	48
EOS	Input	49
BOS	Input	50
SCOUT	Output	51
$\overline{RESET}$	Input	52
$\overline{HALT}$	Input	53
CLKOUT	Output	54
XTAL	Output	55
EXTAL	Input	56
V_{REFN}	Input	57
V_{REFP}	Input	58
AGNDR	Analog Ground	59
RxA1	Input	60
RxA2	Input	61
AV_{DD}	Analog +5V	62
VCM	Input / Output	63
AGNDT	Analog Ground	64

III - G3 FAX EQUIPMENT

III.1 - T.30 Protocol

The ITU-T recommendation T.30 explains the procedures for the facsimile transmission over the public telephone network. The recommandation describes how to initiate, transmit (receive) and close a fax communication.
T.30 recommandation uses five phases called A, B, C, D, E.

Phase A : communication establishment
Phase B : preliminary operations for indentification , request and recognition of the possibilities (group, speed, resolution, ...)
Phase C : high speed message transmission with eventually phase adjust and synchronization
Phase D : post-message procedure including end message, confirmation and procedures for multiple documents
Phase E : end of communication

III.1.1 - Phase A

Four methods are possible for the establishment (manual to manual, manual to automatic, automatic to manual, and automatic to automatic). Manual means a human action while automatic means a machine attempt.
Here are details for an automatic to automatic establishment (usually done by complete facsimile system).

Calling Unit	*Answering Unit*
Off-Hook	
Dialtone detection	
Dials the Fax number	
Sends the calling tone (CNG tone at 1100Hz) and waits to the answer tone (CED tone at 2100Hz)	Incoming call detection off-Hook sends the answer tone (CED at 2100Hz)

Remark : some of manufactures wait for the preamble (HDLC flag with V.21 ch2 modulation) instead of the CED tone.

III.1.2 - Phase B

The preliminary procedure uses the following sequence :
- the answering unit sends the preamble, the identification signal,
- the calling unit waits for the preamble, identification signal and answers with a command signal,
- the transmitting unit sends a training at high speed (V.17 or V.29 or V.27 ter),
- the receiving unit answers to confirm that the training was correct.

The identification, command and answer signals are sent using HDLC protocol over V.21 ch2 Frequency Shift Keying (FSK) modulation.
The preamble is a series of HDLC flags during one second ±15%.

Remark : Identification, command and answer signals are called normalized HDLC frames. Some others frames which are optional can be sent including special information (FAX phone number...) before the identification signal.

Here is an example for phase B where the calling unit wants to send page(s).

Calling Unit	*Answering Unit*
Detect carrier	Send V.21 ch2 carrier
Get preamble	Send preamble
Get DIS frame	Send DIS frame
Detect loss of carrier	Cut off carrier
Send V.21 ch2 carrier	Detect carrier
Send preamble	Get preamble
Send DCS frame	Get DCS frame
Cut off carrier	
Set up to high speed	Set up to high speed
Send V.17 carrier	Detect V.17 carrier
Send TCF data	Get TCF data
Cut off carrier	
Detect carrier	Send V.21 ch2 carrier
Detect preamble	Send preamble
Get CFR frame	Send CFR frame
Detect loss of carrier	Cut off carrier

DIS frame : Digital Identification Signal (DIS) sent by the answering unit to inform the calling unit about its possibilities (group, data rate, resolution...).

DCS frame : Digital Command Signal (DCS) sent by the calling unit to inform the answering unit about the choices for this facsimile communication.

TCF : Training Check Frame (TCF) sent by the calling unit. During TCF the calling unit sends a series of zeroes for a time duration of 1.5s ±10%.

CFR : Configuration to Receive (CFR) is sent by the answering unit to inform the calling unit of a complete successful preliminary procedure (go to phase C). In case where the training fails the answering unit will send the Failure to Train frame (FTT) instead of the CFR frame. In such a case the protocol goes to the DCS step untill the CFR is received by the calling unit.

III.1.3 - Phase C

After completed training in phase B the data are transferred at high speed. The data are com-Pressed with the standard Modified Huffman (MH) or Modified Read (MR) algorithm before being sent. At the receive end the data will be decompressed.

Phase C starts with End of Line (EOL) character. The data following the first EOL until the end of the line. A new line begins with another EOL character. Six EOL characters mean the end of the document transmission and Return To Control (RTC) command.

Normally data are sent in the high speed (V.17 or V.29 or V.27 ter) mode in phase C but a classification signal in the low speed mode (V.21 ch2 with HDLC) may be sent if the handshake fails (CFR was sent by the answering unit but not received by the calling unit due to line distortion...). In such a case the calling unit will return to the procedure to perform DCS (Digital Command Signal). Therefore, the facsimile must wait in high speed mode and with low speed flag detection active.

Calling Unit	*Answering Unit*
Send V.17 carrier	Detect carrier
Send page data	Receive data
Cut off carrier	Detect loss of carrier

III.1.4 - Phase D

Phase D determines whether to terminate or continue Data Tranmission using the HDLC protocol using V.21 ch2 modulation.

Typically the calling unit will send End Of Message (EOM) or Multiple Page signal (MPS) or End Of Procedure (EOP) signal. The answering unit responds to an EOM, MPS or EOP signal with a Message Confirmation (MCF) command.

EOM frame : Informs that it is the end of the page and asking for parameters renegotiation, the protocol FAX goes to phase B.

MPS frame : Signals to the answering unit that there are more pages.

EOP frame : Signals to the answering unit the end of the data transmission (no more pages).

Here is an example with the End Of Procedure signal sent by the calling unit.

Calling Unit	*Answering Unit*
Send V.21 ch2 carrier	Detect carrier
Send preamble	Detect preamble
Send EOP frame	Receive EOP
Cut off carrier	
Detect carrier	Send V.21 ch2 carrier
Receive preamble	Send preamble
Get MCF frame	Send MCF frame
Detect loss of carrier	Cut off carrier

III.1.5 - Phase E

Phase E is executed with an HDLC format cutoff command signal (usually Disconnect (DCN) command).

Calling Unit	*Answering Unit*
Send V.21 ch2 carrier	Detect carrier
Send preamble	Detect preamble
Send DCN frame	Receive DCN
Cut off the carrier	
Hang up	Hang up

III.2 - G3 Transmission (Setup and Training)

III.2.1 - Transmit in High Speed Mode (HM)

The high speed mode uses V.17 or V.29 or V.27 ter ITU-T standards. For each modulation method more than one data rate is possible but only one will be chosen at the end of phase B. We simply summarize hereafter the different possibilities for every modulation. The parameters (P1 to P4) for the CONF command are given too.

Be careful that the V.17 long train is only used at the first time (in PHASE B) when sending the TCF signal. After that the short train option must be used. To select the short train sequence use the MODC command with the first parameter equal to $40 and to select the long train sequence use the same command with the first parameter equal to $00.

In this example we do not select the transmit equalizer, the RTS signal is not used and the standard 1800Hz ITU-T carrier is chosen in V.17.

Modulation	**Data Rate (bps)**	**CONF**	**P1**	**P2**	**P3**	**P4**
V.17	14400	CONF	$0F	$09	$00	$04
V.17	12000	CONF	$0F	$09	$00	$02
V.17	9600	CONF	$0F	$09	$00	$01
V.17	7200	CONF	$0F	$09	$80	$00
V.29	9600	CONF	$0F	$08	$00	$01
V.29	7200	CONF	$0F	$08	$80	$00
V.29	4800	CONF	$0F	$08	$40	$00
V.27 ter	4800	CONF	$0F	$07	$40	$00
V.27 ter	2400	CONF	$0F	$07	$20	$00

The typical sequence to set up the ST75C52/520 could be :

STEP_1 : Select modulation, data rate with ***CONF*** command.

STEP_2 : Start the training sequence with the ***HSHK*** command. It is also possible to start the training sequence with the ***RTS*** Pin if the ST75C52/520 is setup for such a control (***CONF_V24*** bit 7 in the first parameter of ***CONF*** command must be equal to 1). RTS signal can be used in both mode parallel and serial.

STEP_3 : Check that ***STA_H*** (bit 0 in ***STATUS[1]*** of Modem General Status) equals 1 (this step is optional).

STEP_4 : Wait until ***STA_106*** (bit 2 in ***STATUS[0]*** of Modem General Status) equals 1.

STEP_5 : In parallel mode to use interrupts for data transmission enable ***IT2*** interrupt with Interrupt Mask Register ***ITMASK*** doing ITMASK = ITMASK or $84.
Start to transmit Data :
IF parallel mode
SERIAL 01
FORM 00
fill the first buffer (buffer 0)
enable ***IT2***
send ***XMIT 1*** command
send Data with TX buffers every ***IT2*** interrupt
else
send Data on ***TxD*** pin

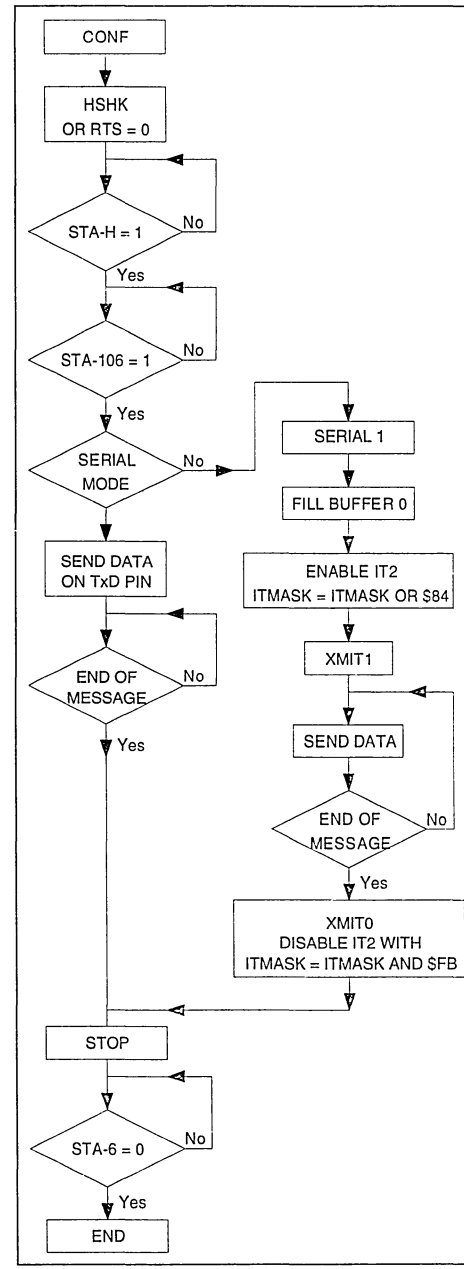
STEP_6 : Stop transmitting Data. In parallel mode send ***XMIT 0*** command. Disable ***IT2*** interrupt with Interrupt Mask Register ***ITMASK*** doing ITMASK = ITMASK and $FB.

STEP_7 : Stop sending carrier with ***STOP*** command.

STEP_8 : Wait end of ITU-T stop sequence (***STA_106 = 0***).

The following flow chart summarizes the above sequence.

Figure 8



III.2.2 - Transmit in Low Speed Mode (LM)

The low speed uses channel 2 of the V.21 ITU-T standard in phase B, D and E to send signal with HDLC protocol over the PSTN network.

The ST75C52/520 gives two posibilities :

- The HDLC is done with an external component. In such a case the transmit data are sent with the serial mode (TxD Pin).
- The ST75C52/520's HDLC controller is used to send data. The ST75C52/520 must be setup for parallel mode and HDLC format.

The typical sequence to set up the ST75C52/520 in parallel mode with HDLC could be :

STEP_1 : Select V.21 ch2 with ***CONF $0F $0D $00 $00*** command (in this example the ***RTS*** signal is not used).

STEP_2 : Start to send the carrier with ***HSHK*** command.

STEP_3 : Check that ***STA_H*** (bit 0 in ***STATUS[1]*** of Modem General Status) equal 1 (this step is optional).

STEP_4 : Wait until ***STA_106*** (bit 2 in ***STATUS[0]*** of Modem General Status) equal 1.

STEP_5 : Select parallel mode with ***SERIAL 1*** command.
Select HDLC format with ***FORM 2*** command.

STEP_6 : Send preamble (the HDLC controller sends flags during one second). To do that send ***XMIT 1*** command and wait one second.

STEP_7 : To use interrupts for data transmission enable ***IT2*** interrupt with Interrupt mask register ***ITMASK*** doing ITMASK = ITMASK or $84.

Start to transmit data :
Fill the first Tx buffer (buffer 0).
Setup ***BUFF_SFRM*** (bit 4 of the transmit buffer status word ***DTTSB0***) to 1 to indicate Start of Frame.
Enable ***IT2***
Continue to send data with Tx buffers (***BUFF_SFRM*** and ***BUFF_EFRM*** respectively bit 4, 5 of ***DDTTSB0*** and ***DDTSB1*** must be equal to 0).

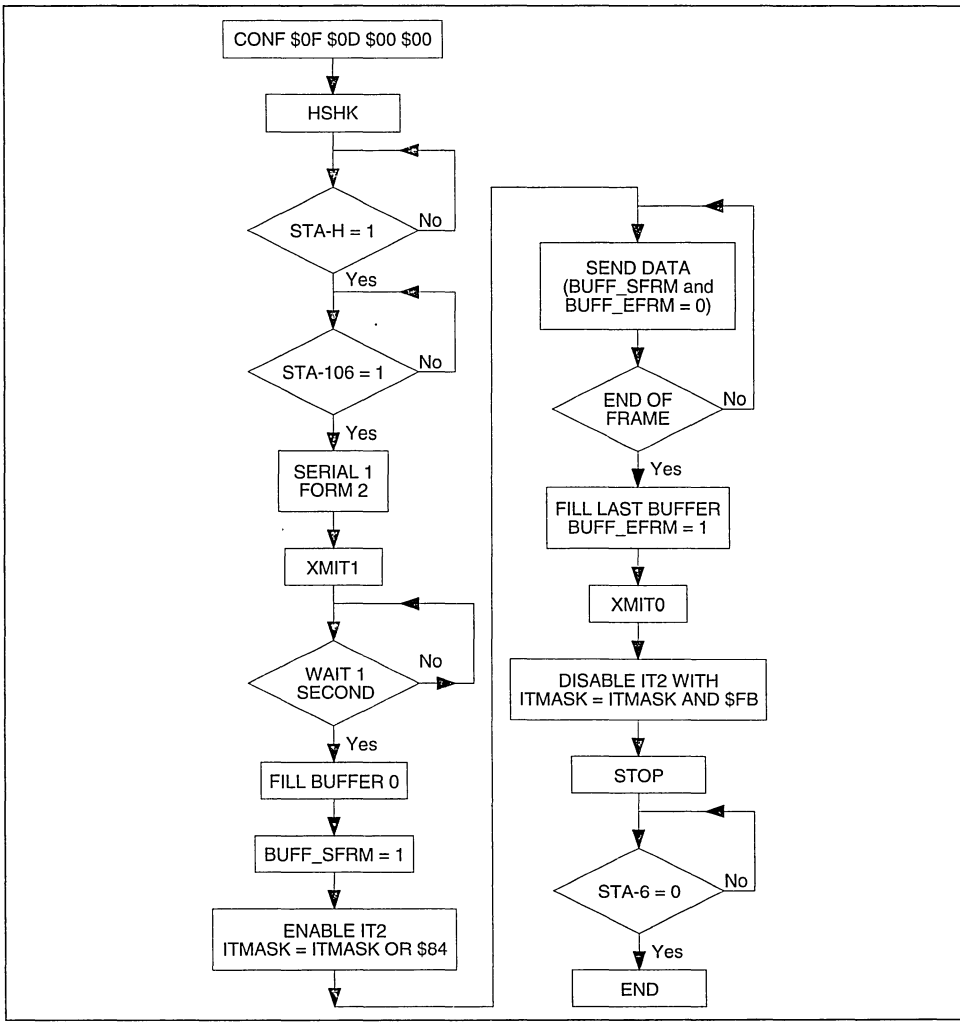
STEP_8 : Stop the data transmission :
Fill the last Tx buffer with data.
Setup ***BUFF_EFRM*** (bit 5 of ***DTTSBX*** with x = 0 or 1 respectively for buffer 0 and 1) to 1 to indicate End of Frame.
Send ***XMIT 0*** to stop data transmission. Desable ***IT2*** with Interrupt Mask Register ***ITMASK*** doing ITMASM = ITMASK and $FB.

STEP_9 : Stop sending carrier with ***STOP*** command.

STEP_10 : Wait end of ***STOP*** sequence (***STA_106*** equal to 0).

The following flow chart summarizes the above sequence.

Figure 9



The typical sequence to set up the ST75C52/520 in serial mode could be :

STEP_1 : Select V.21 ch2 with ***CONF $0F $0D $00 $00*** command (in this example we do not select the transmit equalizer, the ***RTS*** signal is not used).

STEP_2 : Select serial mode with ***SERIAL $00*** command.

STEP_3 : Start to send the carrier with ***HSHK*** command.

STEP_4 : Check that ***STA_H*** (bit 0 in ***STATUS[1]*** of Modem General Status) equal 1 (this step is optional).

STEP_5 : Wait until ***STA_106*** (bi 2 in ***STATUS[0]*** of Modem General Status) equal 1.

STEP_6 : Send preamble (HDLC flag during one second) with ***TxD*** Pin.

STEP_7 : Start to transmit data on ***TxD*** Pin.

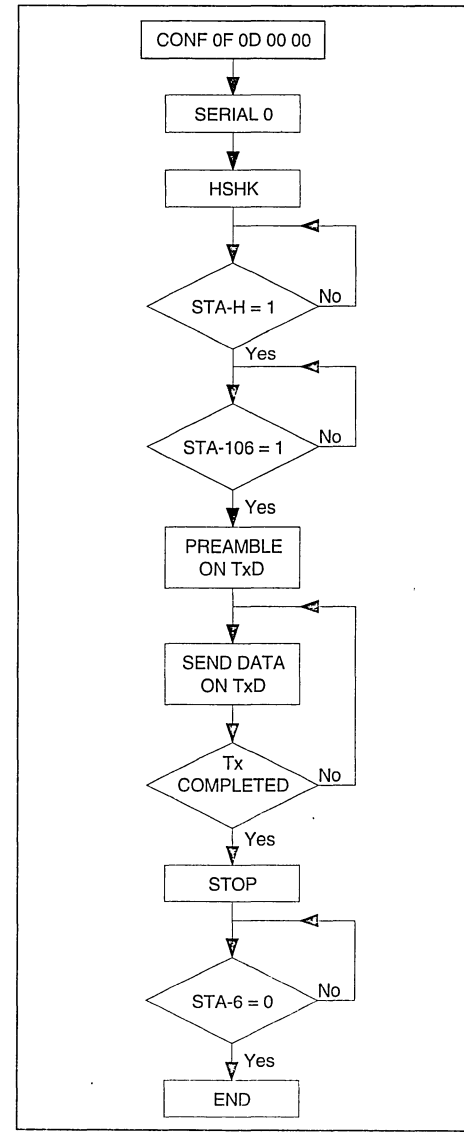
STEP_8 : Stop the data transmission on ***TxD*** Pin.

STEP_9 : Stop to send carrier with ***STOP*** command.

STEP_10 : Wait end of ***STOP*** sequence (***STA_106*** equal to 0).

The following flow chart summarizes the above sequence.

Figure 10



III.3 - G3 Reception (Setup and Synchronization)

III.3.1 - Reception in Phase A

Two cases are possible : the ST75C52/520 is in the calling unit or in the called unit (answering unit).

In the first case (calling unit) the ST75C52/520 is used to detect busy tone, answer tone and preamble.

In the second case (called unit) the ST75C52/520 detects the calling tone (CNG tone at 1100Hz) to recognize an automatic fax call.

The following sequence is an example to set up and to use the ST75C52/520 in the calling unit.

The ST75C52/520 send CNG tone, detect busy tone, answer tone and V.21 channel 2 flag.

STEP_1 : Start a time out (e.g 30s to 60s).

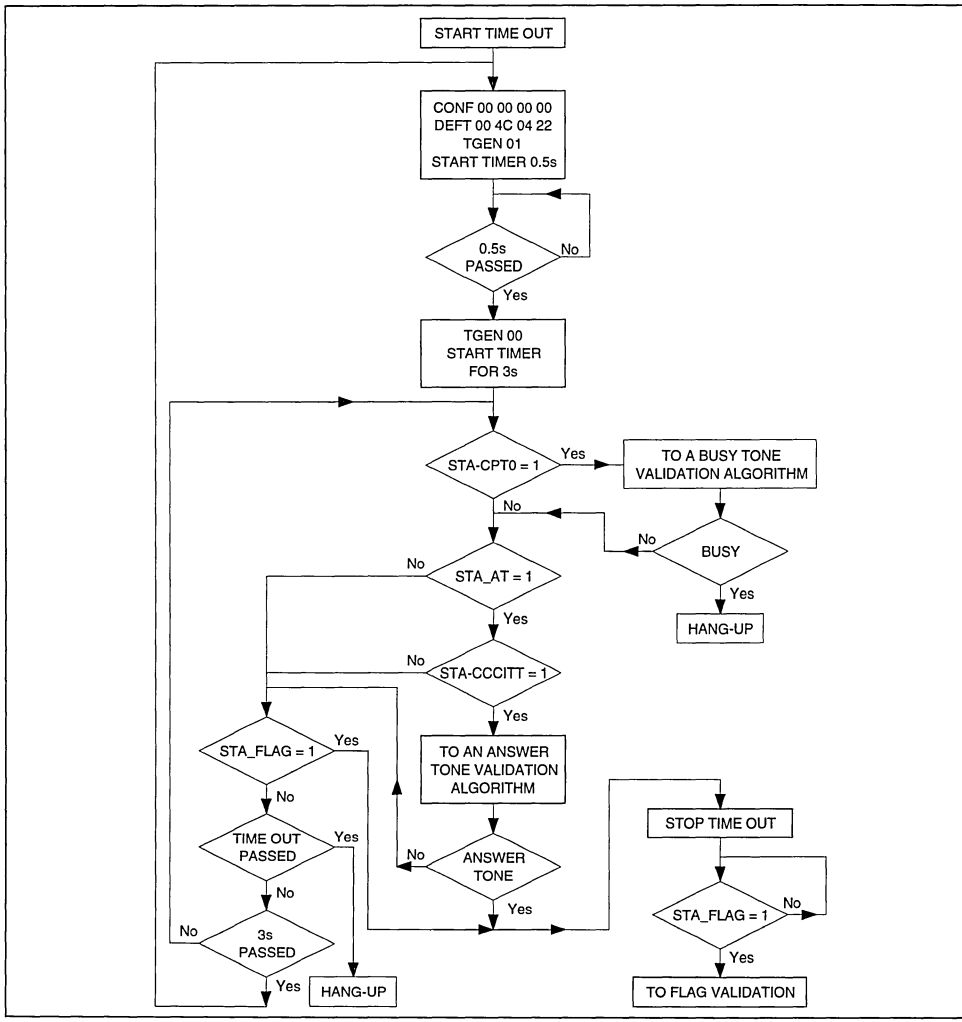
STEP_2 : Setup the ST75C52/520 to send 1100Hz (CNG tone), detect busy tone, answer tone and V.21 flag with the following commands :
CONF $00 $00 $00 $00
DEFT $00 $4C $04 $ZZ (ZZ depend of the wanted level, ZZ = $30 for nominal value).
TGEN $01
wait 0.5s.

STEP_3 : Stop sending CNG tone with ***TGEN $00*** command and start a timer for 3 seconds.

STEP_4 : If ***STA_CPT0*** (bit 4 in ***STATUS[0]*** of Modem General Status) equal 1 begin a Busy tone validation algorithm.
If ***STA_AT*** and ***STA_CCITT*** (bits 3 and 2 in ***STATUS[1]*** of Modem General Status) equal 1 begin an Answer tone validation algorithm.
If ***STA_FLAG*** (bit 6 in ***STATUS[1]*** of Modem General Status) equal 1 begin flag detection (preamble).
If no detection and timer 3s is not elapsed go to the beginning of STEP_4.
If timer 3s is elapsed go to STEP_2 and repeat until Time out.

The following flow chart summarizes the above sequence.

Figure 11



The following sequence is an example to set up and to use the ST75C52/520 in the called unit.

The ST75C52/520 detects the CNG tone and after detection sends the answer tone.

STEP_1 : Start a timer for 4 second.

STEP_2 : Setup the ST75C52/520 to detect tone with the ***CONF $0 $00 $00 $00*** command.
After that the ST75C52/520 will indicate with ***TDT8*** (bit 0 in ***STAOP1*** of Optional Status) equal 1 the 1100Hz detection.

STEP_3 : Validation of the 1100Hz

STEP_4 : Send answer tone (2100Hz) with ***TONE $10*** command.
Wait 3.3 second and stop sending 2100Hz with ***TGEN $00*** command.

Note : Detection of the CNG tone could be optional, since the calling unit can be manual.

The flow chart (Figure 12) summarizes the above sequence.

III.3.2 - Reception in Phase B

As in phase A two cases are possible. In the first case the ST75C52/520 detects and receives preamble, HDLC frame over V.21 ch2 modulation. In the second case the ST75C52/520 detects and receives training over High speed standards (V.17 or V.29 or V.27 ter).

Hereafter is an example to set up the ST75C52/520 to detect and receive preamble, HDLC frame over V.21 ch2 (use parallel mode).

STEP_1 : Setup V.21 ch2 with ***CONF $0F $0D $00 $00*** command.
Arm the receiver with ***SYNC $01*** command.
Wait until a V.21 ch2 signal is received by testing ***STA_109*** (bit 0 in ***STATUS[0]*** of Modem General Status) equal 1.

STEP_2 : Wait until HDLC flag is received (preamble) with ***STA_FLAG*** (bit 6 in ***STATUS[1]*** of Modem General Status) equal 1.

STEP_3 : Enable Parallel reception (***IT3*** interrupt) with the following sequence :
write $00 into ***DTRBF0***
write $00 into ***DTRBF1***
enable ***IT3*** doing ITMASK = ITMASK or $88
select HDLC and parallel format with ***FORM $02*** and ***SERIAL $02*** commands.

The flow chart (Figure 13) summarizes the above sequence.

Figure 12

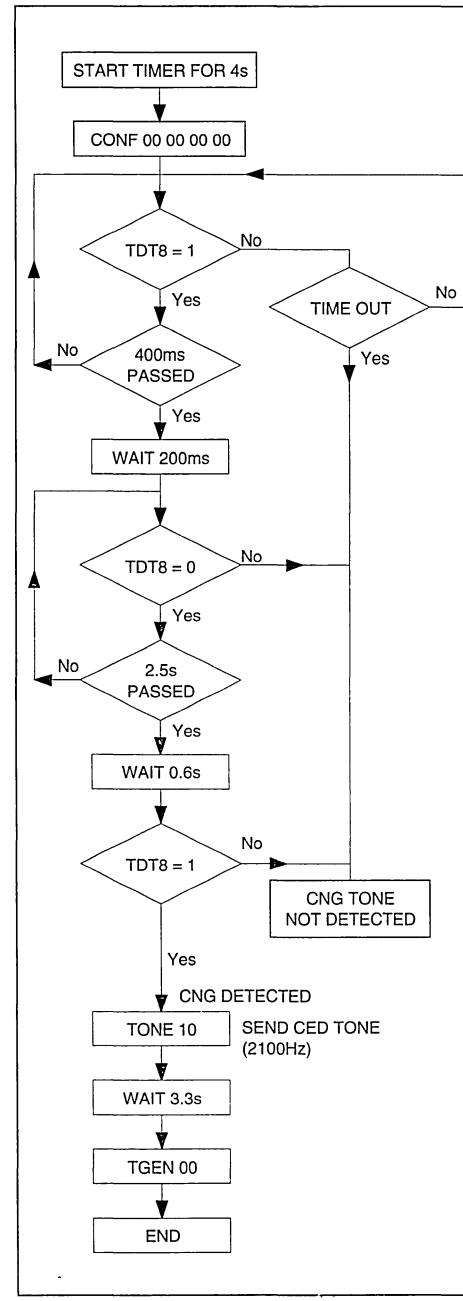
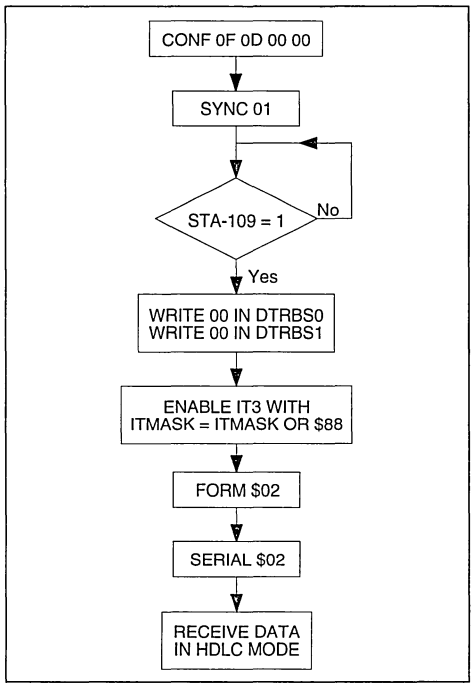


Figure 13



Hereafter is an example to set up the ST75C52/520 to detect V.21 ch2 carrier and after that to be used in serial mode.

STEP_1 : Setup V.21 ch2 with ***CONF $0F $0D $00 $00*** command.
Send ***SERIAL $00*** to use serial interface.
Arm the receiver with ***SYNC 1*** to detect V.21 ch2 carrier.

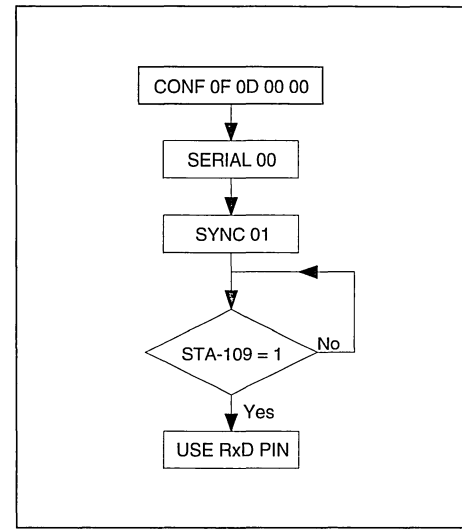
STEP_2 : Wait ***STA_109*** (bit 0 in ***STATUS[0]*** of Modem General Status) equal 1 or ***CD*** Pin equal 0.

STEP_3 : Receive Preamble and Data Frame on ***RxD*** Pin.

The flow schart (Figure 14) summarizes the above sequence.

In phase B the two units select a high speed among the different possibilities (V.17, V.29 or V.27 ter). At this point the transmitting unit must send a training check (TCF) with the selected speed. The receiving unit must be set up to receive it.
Please see the Table given at chapter III.1.2 for CONF's parameters for all the high speed possibilities.

Figure 14



For parallel reception the typical sequence to setup the ST75C52/520 could be :

STEP_1 : Select modulation, data rate with ***CONF*** command.

STEP_2 : Arm the receiver with ***SYNC $01*** command.

STEP_3 : Wait for the beginning of the receive synchronization by testing ***STA_HR*** (bit 4 in ***STATUS[1]*** of Modem General Status) equal 1 (this step is optional).

STEP_4 : Wait for the end of the receive synchronization and the beginning of the data mode by testing ***ST_109*** (bit 0 in ***STATUS[0]*** of modem General Status) equal 1.

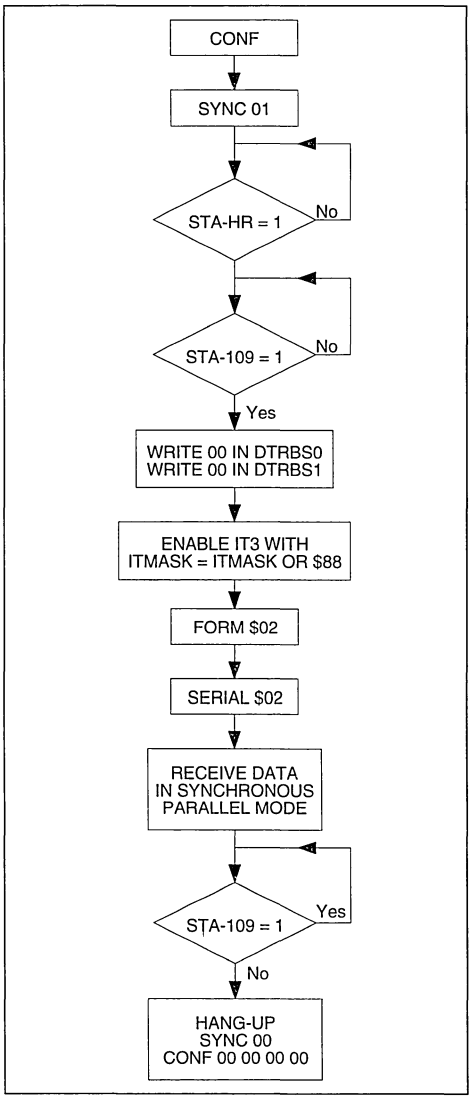
STEP_5 : Enable parallel reception (IT3 interrupt) with the following sequence.
write $00 into ***DTRBF0***
write $00 into ***DTRBF1***
enable ***IT3*** doing ITMASK = ITMASK or $88
select synchronous parallel format with ***FORM $00*** and ***SERIAL $02*** commands.

STEP_6 : Receive data. If ***STAT_109*** equal 0 go to STEP_7.

STEP_7 : Hang_up.

The flow chart (Figure 15) summarizes the above sequence.

Figure 15



For serial reception the typical sequence to set up the ST75C52/520 could be :

STEP_1 : Select modulation, data rate with ***CONF*** command.

STEP_2 : Arm the receiver with ***SYNC $01*** command.

STEP_3 : Wait for the beginning of the receive synchronization by testing ***STA_HR*** (bit 4 in ***STATUS[1]*** of Modem General Status) equal 1 (this step is optional).

STEP_4 : Wait until the end of the receive synchronization and the beginning of the data mode by testing ***ST_109*** (bit 0 in ***STATUS[0]*** of modem General Status) equal 1.

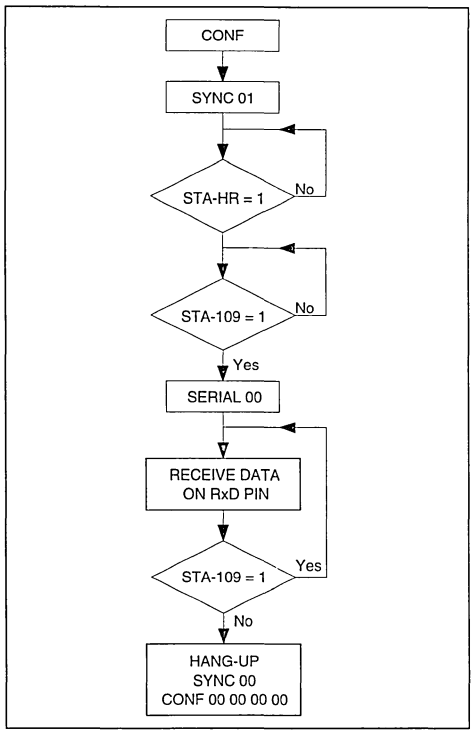
STEP_5 : Select serial mode with ***SERIAL $00*** command.

STEP_6 : Receive data on ***RxD*** Pin. If ***STAT_109*** equal 0 go to STEP_7.

STEP_7 : Hang_up.

The flow chart (Figure 16) summarizes the above sequence.

Figure 16



III.3.3 - Reception in Phase C

As explained in Chapter III.1.3 the receiving unit must be able to detect reception in both modes (high speed and low speed).

Please see the Table given at Chapter III.1.2 for CONF's parameters for all the high speed possibilities.

Be careful that in V.17 the long train sequence is only allowed for the TCF in phase B, that is why the V.17 will always use the short train sequence in phase C. The ***MODC*** command with its first parameter equals $40 will select the short train sequence (the same parameter equal to $00 selects the long train sequence).

For parallel reception in phase C the following sequence could be :

STEP_1 : Select modulation data rate with ***CONF*** command.

STEP_2 : If V.17 short train requested send ***MODC $40 $00*** command.

STEP_3 : Arm the receiver with ***SYNC $01*** command.

STEP_4 : If ***STA_FLAG*** (bit 6 in ***STATUS[1]*** of Modem General Status) equals 1 go to STEP_9.
If ***P2s*** (bit 1 in ***STAOP2*** of the Optional Status) equal 1 go to STEP_5.

STEP_5 : If ***STA_FLAG*** equal 1 go to STEP_9.
If ***PNDETs*** (bit 5 in ***STAOP2*** of the Optional Status) equals 1 go to STEP_6.

STEP_6 : Wait until ***STA_109*** (bit 0 in ***STATUS[0]*** of the Modem General Status) equal 1.

STEP_7 : STEP_7 : Enable parallel reception (***IT3*** interrupt) with the following sequence :
write $00 into ***DTRBF0***
write $00 into ***DTRBF1***
enable ***IT3*** doing ITMASK = ITMASK or $88
select synchronous parallel format with ***FORM $00*** and ***SERIAL $02*** commands.

STEP_8 : Receive data. If ***STA_109*** equal 0 go to STEP_13.

STEP_9 : Stop synchronization with ***SYNC 0*** command.
Setup V.21 ch2 with ***CONF $0F $0D $00 $00*** command.
Arm the receiver with ***SYNC $01*** command.

STEP_10 : wait until ***STA_109*** equal 1.

STEP_11 : Enable HDLC, parallel reception and ***IT3*** interrupt with the following sequence :
write $00 into ***DTRBF0***
write $00 into ***DTRBF1***
enable ***IT3*** doing ITMASK = ITMASK or $88
select HDLC, parallel format with ***FORM $02*** and ***SERIAL $02*** commands.

STEP_12 : Receive data. If ***STA_109*** equal 0 go to STEP_13.

STEP_13 : Hang_up.

The flow chart (Figure 17) summarizes the above sequence.

For serial reception in phase C the following sequence could be :

STEP_1 : Select modulation data rate with ***CONF*** command.
Select serial mode with ***SERIAL $00*** command.

STEP_2 : If V.17 short train requested send ***MODC $40 $00*** command.

STEP_3 : Arm the receiver with ***SYNC $01*** command.

STEP_4 : If ***STA_FLAG*** (bit 6 in ***STATUS[1]*** of Modem General Status) equal 1 go to STEP_7.
If ***P2s*** (bit 1 in ***STAOP2*** of the Optional Status) equal 1 go to STEP_5.

STEP_5 : If ***STA_FLAG*** equal 1 go to STEP_7.
If ***PNDETs*** (bit 5 in ***STAOP2*** of the Optional Status) equal 1 go to STEP_6.

STEP_6 : Wait until ***STA_109*** (bit 0 in ***STATUS[0]*** of the Modem General Status) equal 1 and than go to STEP_9.

STEP_7 : Stop synchronization with ***SYNCH $00*** command.
SetupV.21 ch2 with ***CONF $0F $0D $00 $00*** command.
Arm the receiver with ***SYNCH $01*** command.

STEP_8 : Wait until ***STA_109*** equal 1 and go to STEP_9.

STEP_9 : Receive data on ***RxD*** Pin.
If ***STAT_109*** equal 0 go to STEP_10.

STEP_10 : Hang_up.

The flow chart (Figure 18) summarizes the above sequence.

Figure 17

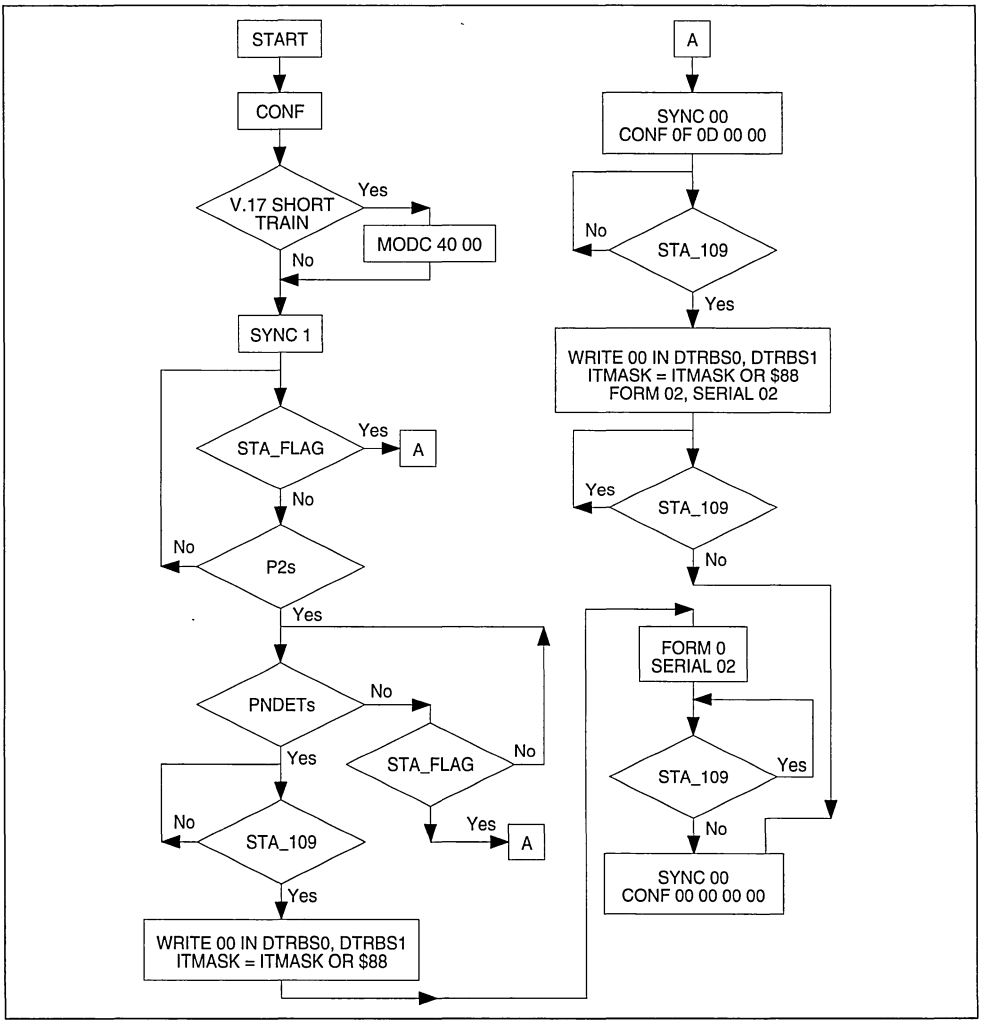
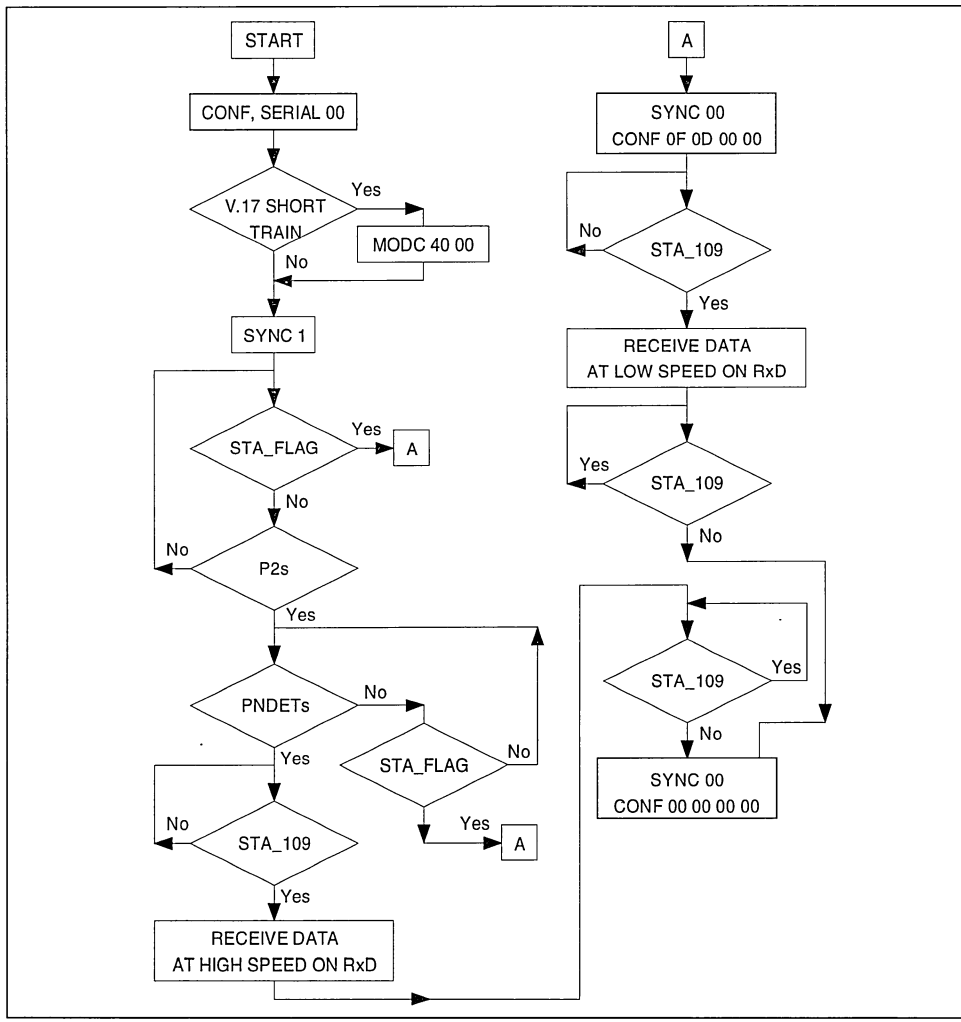

START
CONF
V.17 SHORT TRAIN
Yes
MODC 40 00
No
SYNC 1
STA_FLAG
Yes
A
No
P2s
No
Yes
PNDETs
No
STA_FLAG
No
Yes
Yes
STA_109
No
Yes
A
Yes
WRITE 00 IN DTRBS0, DTRBS1
ITMASK = ITMASK OR $88
A
SYNC 00
CONF 0F 0D 00 00
No
STA_109
Yes
WRITE 00 IN DTRBS0, DTRBS1
ITMASK = ITMASK OR $88
FORM 02, SERIAL 02
Yes
STA_109
No
FORM 0
SERIAL 02
STA_109
Yes
No
SYNC 00
CONF 00 00 00 00
75C52-42 EPS

Figure 18



III.3.4 - Reception in Phase D

As in phase B the FAX system will receive data in V.21 ch2 with the HDLC format.

See the example detailed in Chapter III.3.2 for setup the ST75C52/520 to detect and receive preamble, HDLC frame over V.21 ch2.

III.3.5 - Reception in phase E

The FAX system must receive DCN signal (deconnection) in low speed mode.

After that no reception will be done by the FAX system in phase E, so after deconnection we suggest to setup the ST75C52/520 with ***CONF $00 $00 $00 $00*** command to be able to send and detect tones.

If power management is important we suggest to put the ST75C52/520 in low power mode with the following sequence :
Enable ***IT5*** interrupt doning ITMASK = ITMASK or $A0.
Send SLEEP command.

IV - DATA EXHANGES

This chapter describes the way to use the ST75C52/520 Data Buffers.

These Data Buffers are implemented into the DUAL RAM of the ST75C52/520. They are shared between the Host processor and the ST75C52/520. A mechanism of Flags and Interrupts is associated with them to allow an easy management of the Data.

The mechanism described below is only valid while in regular Data Transmission, not in Handshaking neither in Call progress (or DTMF) tone detection modes.

"Host" refers to the Micro-controller connected to the ST75C52/520 Data Pump.

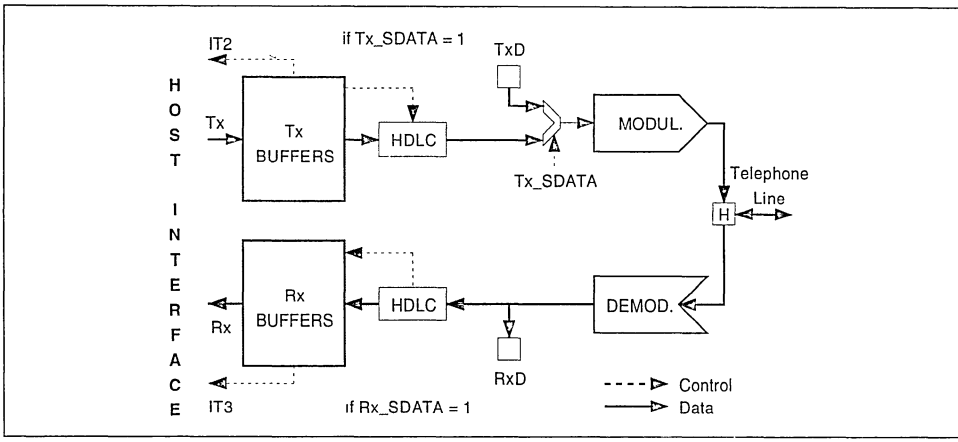
"Transmit Data" (or Tx) means Data transfered by the ST75C52/520, via the modulator, to the telephone line, and "Receive Data" (or Rx) means Data comming from the telephone line and Demodulated by the ST75C52/520.

IV.1 - Overview

While in Parallel mode, the Transmitted (respectively Received) Data to (from) the telephone line are exchanged between the Host and the ST75C52/520.
Two totally independent channels are provived for Transmit and Receive Data. Even while using Half Duplex modes of operation, the transmitted data comes from the Transmit buffers and the receive data arrives in the Receive buffers.

Two independent Interrupts, ***IT2*** (for Transmit) and ***IT3*** (for Receive) are available for synchronizing the ST75C52/520 and the Host. An additional ***IT0*** interrupt will signal the errors in the synchronization mechanism.
The equivalent Data Flow is as follows (see Figure 19).
The ST75C52/520 has a buit-in HDLC capability. This feature automatically performs HDLC framing/deframing, CRC Generation/detection and "0" Insertion/deletion. This Format of Data is selected by the ***FORM*** Command described bellow.

Figure 19



IV.2 - Select Parallel Mode

IV.2.1 - SERIAL Command

The ***SERIAL*** command allows the independent selection of the parallel mode for the Transmit and/or Receive Data path. The parameter syntax is as follows (see Table 3).

Table 3

Field	Byte	Pos.	Value	Definition
TX_SDATA	1	0	0 * 1	Use Serial Link for Tx Data Use both Serial and Parallel Link for Tx Data
RX_SDATA	1	1	0 * 1	Use only Serial Link for Rx Data Use both Serial and Parallel Link for Rx Data

Note : Even if the parallel mode is selected for the Receiver, the Received Bit Stream is available on the RxD Pin of the ST75C52/520. This command must be sent in Data Mode, when the Transmit or Receive data links are established. This corresponds with the presence of the signals STA_106 (for Tx) and/or ***STA_109*** (for Rx).

IV.3 - Transmit Buffers

Two identical buffers are provided to exchange the data between the Host interface and the ST75C52/520. When the host is writing data into a buffer, the ST75C52/520 is transmitting the other one. After that, both the Host and the ST75C52/520 switch to use the other buffer. This mechanism, called "Double-Buffering", ensures that the host has the maximum time to fill one buffer.

The DUAL Ram area associated with the transmit buffers is as follows :

Table 4

Name	Address	Description
DTTBS0	$2E	Buffer 0 Status Byte
DTTBS0 [0]	$2F	Buffer 0 Status Byte 0
DTTBS0 [1]	$30	Buffer 0 Status Byte 1
DTTBS0 [2]	$31	Buffer 0 Status Byte 2
DTTBS0 [3]	$32	Buffer 0 Status Byte 3
DTTBS0 [4]	$33	Buffer 0 Status Byte 4
DTTBS0 [5]	$34	Buffer 0 Status Byte 5
DTTBS0 [6]	$35	Buffer 0 Status Byte 6
DTTBS0 [7]	$36	Buffer 0 Status Byte 7
DTTBS1	$37	Buffer 1 Status Byte
DTTBS1 [0]	$38	Buffer 1 Status Byte 0
DTTBS1 [1]	$39	Buffer 1 Status Byte 1
DTTBS1 [2]	$3A	Buffer 1 Status Byte 2
DTTBS1 [3]	$3B	Buffer 1 Status Byte 3
DTTBS1 [4]	$3C	Buffer 1 Status Byte 4
DTTBS1 [5]	$3D	Buffer 1 Status Byte 5
DTTBS1 [6]	$3E	Buffer 1 Status Byte 6
DTTBS1 [7]	$3F	Buffer 1 Status Byte 7

The Bit 0 (LSB) of the Buffer 0 Data Byte 0 is the first in time to be transmited.

According to the Data Format, the Status byte of a buffer has different meanings. However a value of 0 signals to the host that a buffer is empty. This value is set by the ST75C52/520 each time it has emptied the buffer. After having used one buffer, the host must select the other buffer for the next operation. The host must start with the Buffer 0 as soon as the ***ST_106*** signal is on and the ***SERIAL Tx*** is selected and BEFORE the ***XMIT 1*** command is sent.

A mechanism of interruption (IT2 for Transmit) is associated with the Data Buffer management. Each time a Buffer is emptied by the ST75C52/520 it generates an interrupt.

IV.4 - Receive Buffers

Symetrically two identical buffers are provided to exchange receive data between the ST75C52/520 and the Host processor. While the ST75C52/520 is filling one of the buffers with the receive bits, the Host processor is reading the other buffer. As soon as the host has emptied a buffer it frees it by writing 0 in the buffer status byte.

The DUAL Ram area associated with the receive buffers is as follows :

Table 5

Name	Address	Description
DTRBS0	$1C	Buffer 0 Status Byte
DTRBS0 [0]	$1D	Buffer 0 Status Byte 0
DTRBS0 [1]	$1E	Buffer 0 Status Byte 1
DTRBS0 [2]	$1F	Buffer 0 Status Byte 2
DTRBS0 [3]	$20	Buffer 0 Status Byte 3
DTRBS0 [4]	$21	Buffer 0 Status Byte 4
DTRBS0 [5]	$22	Buffer 0 Status Byte 5
DTRBS0 [6]	$23	Buffer 0 Status Byte 6
DTRBS0 [7]	$24	Buffer 0 Status Byte 7
DTRBS1	$25	Buffer 1 Status Byte
DTRBS1 [0]	$26	Buffer 1 Status Byte 0
DTRBS1 [1]	$27	Buffer 1 Status Byte 1
DTRBS1 [2]	$28	Buffer 1 Status Byte 2
DTRBS1 [3]	$29	Buffer 1 Status Byte 3
DTRBS1 [4]	$2A	Buffer 1 Status Byte 4
DTRBS1 [5]	$2B	Buffer 1 Status Byte 5
DTRBS1 [6]	$2C	Buffer 1 Status Byte 6
DTRBS1 [7]	$2D	Buffer 1 Status Byte 7

The Bit 0 (LSB) of the Buffer 0 Data Byte 0 is the first received bit in time (the oldest).

According to the Data Format, the Status byte of a buffer has different meaning. However a value of 0 signals to the ST75C52/520 that a buffer is empty. This value is set by the Host each time it has emptied the buffer. After having used one buffer, the host must select the other buffer for the next operation. The Host must start with the Buffer 0 as soon as the ***STA_109*** signal is on and the ***SERIAL Rx*** is selected.

A mechanism of interruption (***IT3*** for Receive) is associated with the Data Buffer management. Each time a buffer is filled by the ST75C52/520 it generates an interrupt.

IV.5 - Interruption

Two Interrupt signals are provided in order to synchronize the Data Buffer Exchanges. ***IT2*** is associated with the Transmit Buffer mechanism and ***IT3*** with the Receive Buffer mechanism.

In order to enable these interrupts, the Host processor must set the bit 2 (for ***IT2***) and the bit 3 (for ***IT3***) of the ***ITMASK*** Register to 1. It must also set the Bit 7 of the ***ITMASK*** register to 1 in order to globally enable all the selected sources of interruption.

When an Interrupt occurs (low level on ***SINTR*** Pin) the user must read the ***ITSRCR*** Register to determine the source of the interrupt, either ***IT2*** for Tx (if the bit 2 is 1) or ***IT3*** for Rx (if the bit 3 is 1).

Once the Interrupt has been serviced, the host must acknowledge it by writing a $00 value into the register ***ITRES2*** for ***IT2***, or ***ITRES3*** for ***IT3***.

These registers have the following address (see Table 6).

Table 6

Name	Address	Type	Description
ITRES2	$42	Write only	Clear IT2
ITRES3	$43	Write only	Clear IT3
ITMASK	$4F	Read/Write	Interrupt Mask
ITSRCR	$50	Read Only	Interrupt Source

Notes : 1. The ST75C52/520 does not check that the interrupt has been acknowledged.

2. Even if the Host does not use the interruption, the ST75C52/520 will set the bit 2 (for ***IT2***) and/or bit 3 (for ***IT3***) of the ***ITSRCR***.

3. The ST75C52/520 uses only the Data Buffer Status Bytes to detect Overrun or Underrun Error. These errors are reported into the ***SYSERR*** byte, and could generate an interrupt ***IT0***.

The equivalent schematic is : see Figure 20.

The interrupt mechanism assumes that the Host processor uses a Level sensitive interrupt (active low). The flow chart of the Host interrupt service routine looks generaly like this (see Figure 21).

Figure 20

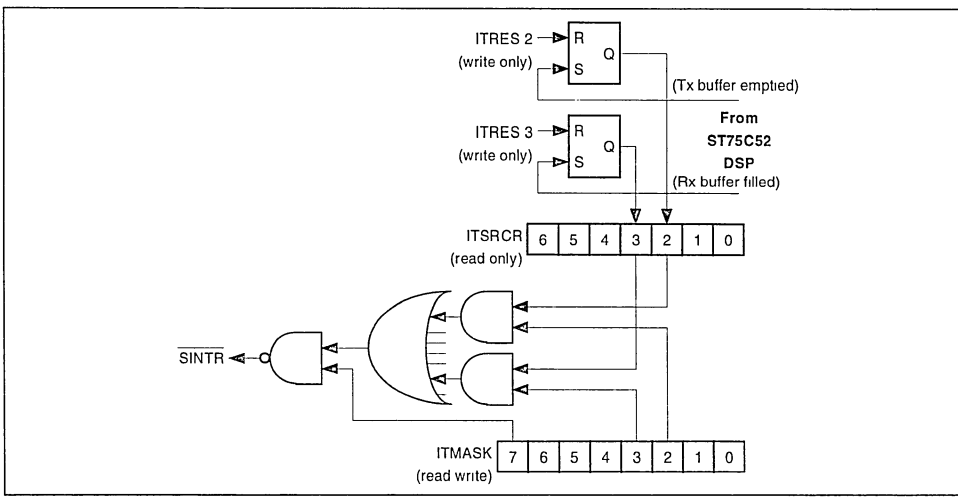
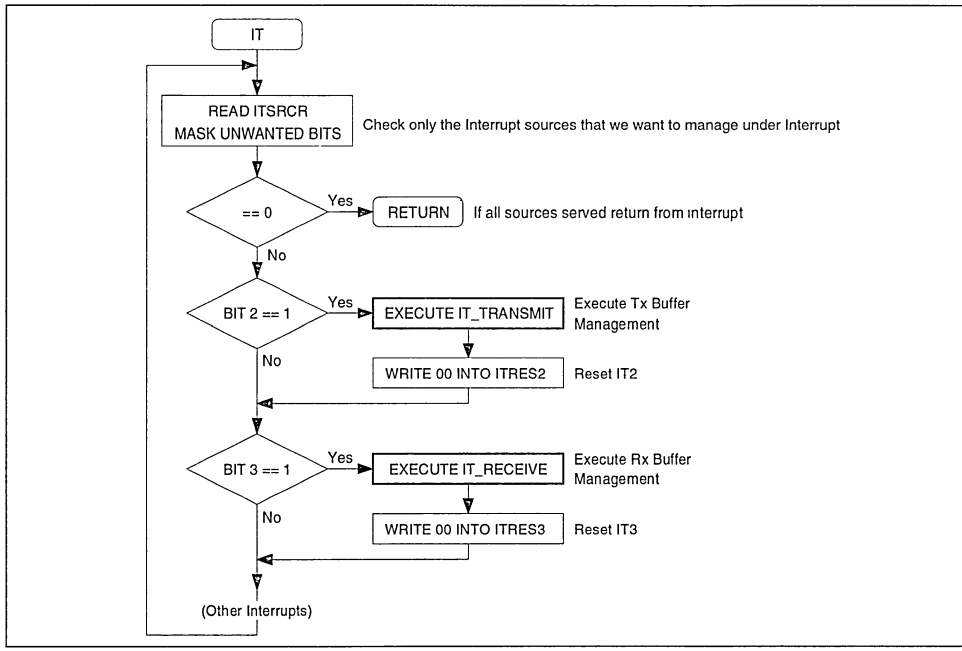


Figure 21



IV.6 - Data Format

Different Formats of Data can be Transmitted/Received to/from the Telephone Line. These Formats can be selected when entering the Data Mode by using the ***FORM*** command.
The Format of the Data can be changed, on the fly in the Data Mode during the same communication, by sending a different ***FORM*** command at any time. Note that for Full Duplex operation the Data Format is the same for the transmitter and the receiver.

IV.6.1 - FORM Command

The ***FORM*** command allows the selection of the Data Format. The Parameter syntax is as follows :

Table 7

Field	Byte	Pos.	Value	Tx Rx	Definition
X_SYNC	1	1..0	00*	X X	Synchronous format
			01	X	Continuous "1" (Tx only)
			10	X X	HDLC framing /deframing
			11	X	Continuous "0" (Tx only)

IV.6.2 - Synchronous Mode

The synchronous mode is the default mode, if no ***FORM*** command is used.

The transmitter reads the bits in the DUAL Ram Buffer ***DTTBFx*** (starting with the Bit 0 of Byte 0 of Buffer 0) and send them over the Telephone line. The Buffer Status Byte ***DTTBSx*** contains the number of Data Bytes to transmit.

The Receiver write the received bits comming from the Telephone line and write them into the DUAL Ram Buffer ***DTRBFx*** (starting with the Bit 0 of the Byte 0 of the Buffer 0). The Buffer Status Byte ***DTRBSx*** contains the number of Data Bytes received (generaly 8).

The time between each ***IT2*** interrupts (or ***IT3***) is equal to 64-bit if the number of Data Bytes is set to 8. The Host has the full 64 bits time to serve the interrupt.

Table 8

Bit Rate (bps)	Interrupt Time (ms)
14400	4.4
12000	5.3
9600	6.6
7200	8.8
4800	13.3
2400	26.6
1200	53.3
300	213.3
75	853.3

IV.6.3 - HDLC Mode

The HDLC Format can be used for T.30 or ECM implementations

IV.6.3.1 - HDLC Transmit

The HDLC Transmitter performs the following tasks :
- flag generation (7E) while in inter-frame,
- flag generation (7E) at the beginning of a frame,
- zero insertion (after 5 consecutive "1"),
- CRC16 computation,
- CRC16 transmission at the end of a frame,
- flag generation (7E) at the end of a frame,
- abort frame.

The Buffer Status Byte ***DTTBSx*** defines the frame type, and the number of Data Bytes to transmit.

IV.6.3.2 - HDLC Receive

The HDLC Receiver performs the following tasks :
- flag recognition,
- opening flag recognition,
- zero deletion,
- CRC16 computation,
- CRC16 check; error CRC16 detection,
- closing flag recognition,
- abort frame detection.

The Buffer Status Byte ***DTRBSx*** contains the frame type, the number of Data Bytes and the error report if any.

The errors detected are :
- CRC16 Error : Wrong CRC received,
- non byte-alligned frame : The number of Data bits between the beginning of the frame and the end of the frame (after "zero" deletion) is not a byte-multiple,
- aborted frame : More that 6 consecutive "1" received.

IV.7 - Transmitting in Parallel Mode

IV.7.1 - Description

When the ***STA_106*** (CTS) signal is on, the user must select the parallel mode by enabling the parallel link with ***TX_SDATA*** bit set in ***SERIAL*** command. After that the ST75C52/520 will start transmitting continuous "1". Note that for a proper operation each time the ***STA_106*** signal goes on, the ***SERIAL*** command must be sent.

IV.7.1.1 - XMIT Command

The ***XMIT*** Command works like a CTS signal for the Parallel process.

When ***XMIT*** is off, the ST75C52/520 transmits continuous "1". When on the ST75C52/520 transmits Data in accordance with the ***FORM*** command and starts to manage the Data Buffer.

This command can be sent at any time, while in Data Mode (see Table 9).

IV.7.1.2 - FORM Command

The ***FORM*** Command can be sent at any time to redefine the current format. The effect will take place only when ***XMIT*** is on.

Here is a formal example showing the relationship between ***SERIAL***, ***XMIT***, and ***FORM*** Commands : see Figure 22.

IV.7.1.3 - STOP Command

The ***STOP*** command is used, at the end of the transmission, to stop sending the carrier on the telephone line. According to the Parallel/Serial mode (defined with the ***SERIAL*** command) and the Format (defined with the ***FORM*** command) the effect of this command is as in Table 10.

Prior to the ***STOP*** command the user must have stop the parallel transmission with a ***XMIT off*** command.

Table 9

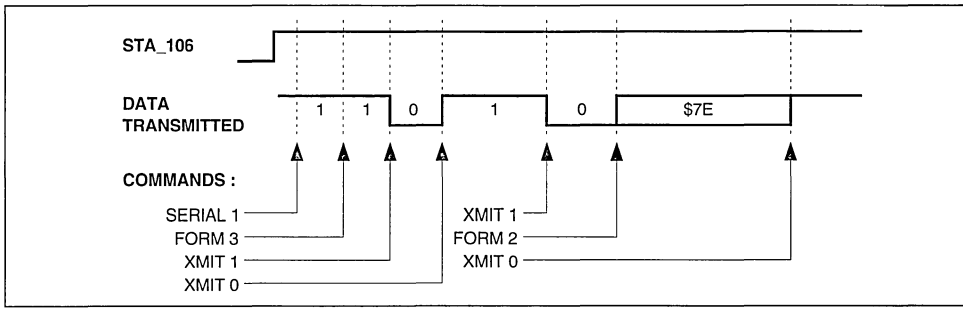
Field	Byte	Pos.	Value	Definition
TX_START	1	0	0 * 1	(Off) Send continuous "1" (1). (On) Send Data according with the Format defined in the ***FORM*** command.

Note 1 : The XMIT Off command takes effect only when the two Transmit buffers are empty : ***DTTBF0*** and ***DTTBF1*** equal to $00.

Table 10

Mode	TX-SDATA	Observed actions
Serial	0	Immediate
Parallel	1	When the current data buffer will be totaly transmitted, and that no more buffers will be available, that is to said both ***DTTBF0*** and ***DTTBF1*** will be $00 (equivalent to an Underrun condition).

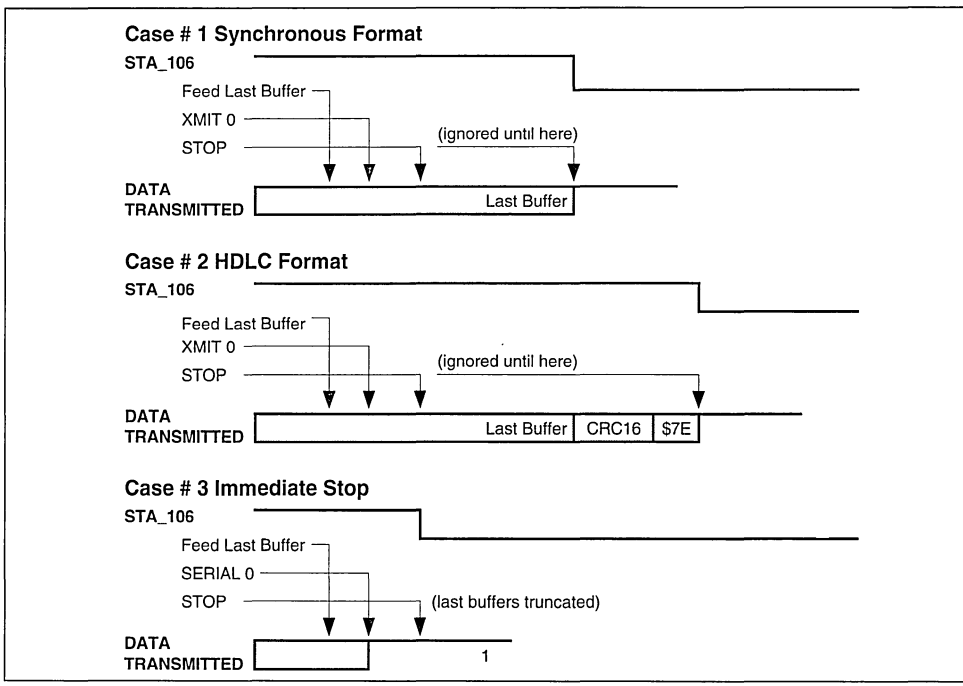
Figure 22



IV.7.1.4 - Timing

Here are regular sequences to stop properly the transmission : see Figure 23.

Figure 23



IV.7.1.5 - FSK Full Duplex Mode

In FSK Full duplex Mode the parallel mode assumes that the Bit time duration is the nominal Bit rate. Each bit element from the Transmit buffer is maintained during the full bit time. The Nominal bit clock is defined as follows :

Table 11

FSK Standard	Nominal Transmit Bit Rate (Hz) (1)	Bit Clock on CLK Pin (Hz)
V.21	300	9600
Bell 103	300	9600
V.23 Originate	75	9600
V.23 Answer	1200	9600

Note 1 : The accuracy of the Bit clock is given by the ST75C52/520 oscillator, and must better than 50ppm

IV.7.2 - Modem Flow Chart

When in the Parrallel Data Mode, each time the ST75C52/520 need a bit to transmit it executes the following routine (see Figure 24).

Where **x** starts with the value 0 and toggle thereafter between 1 and 0.

IV.7.3 - Host Flow Chart

Here after are Flowcharts to :

- establish a V.29 transmission
- send Synchronous continuous "$AA, $55, $AA, $55..." sequence.
  The management of the Buffers are done under Interrupt.
- stop properly the transmission.

Establish a V.29 transmission and send the very first Buffer (see Figure 25).

Figure 24

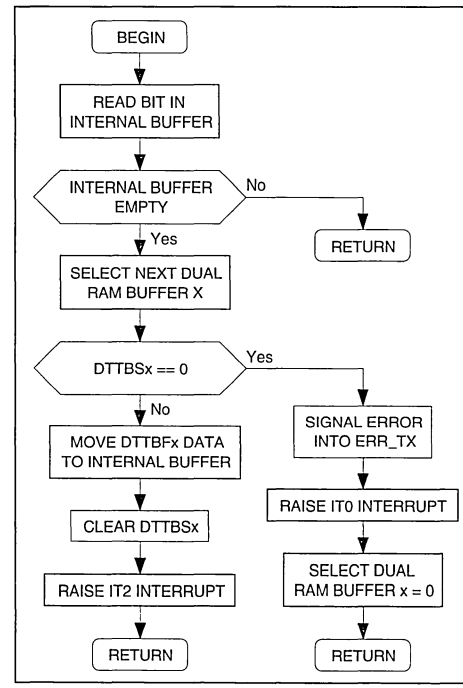
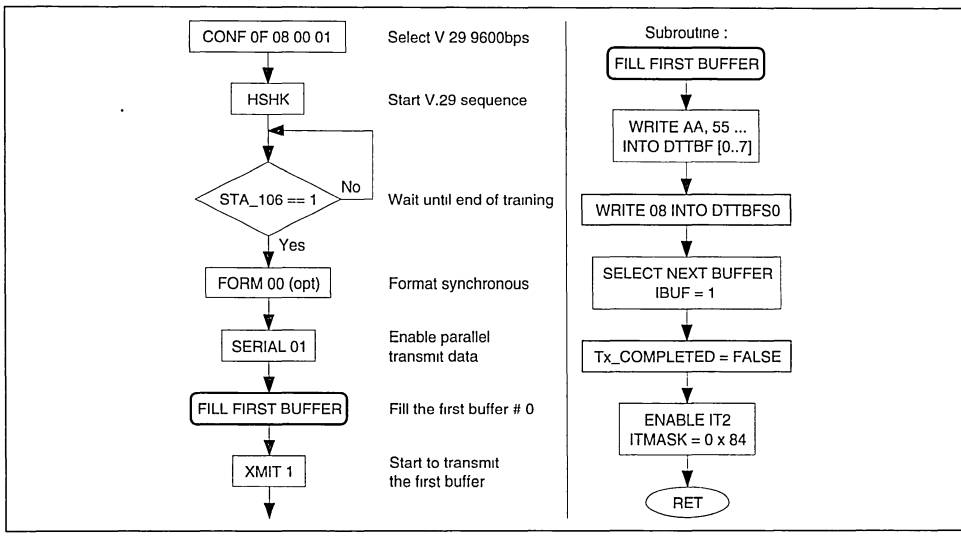


Figure 25

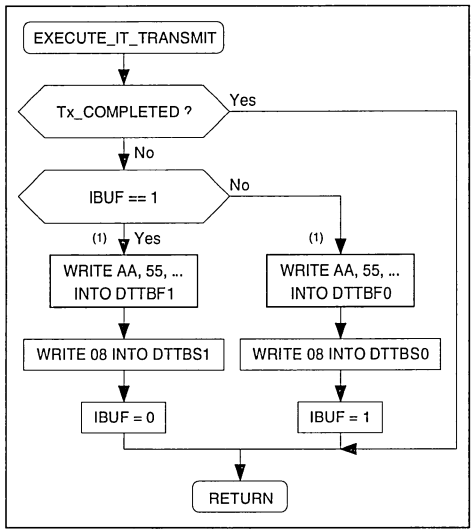


These flowcharts show two CPU variables labeled IBUF and Tx_Completed, they are necessary for the understanding of the mechanism, but there is different manners to implement it. These two variables have the following meanning :

- IBUF: This is the number of the DUAL Ram Buffer currently in use by the Host processor. It starts with 0 and then alternate 1, 0, 1, 0...
- Tx_Completed: This is a Flag to dialog with the interrupt process in order to stop properly the transmission.

The other Buffers are sent under interrupt control (refer to the interrupt flow chart, Figure 26).

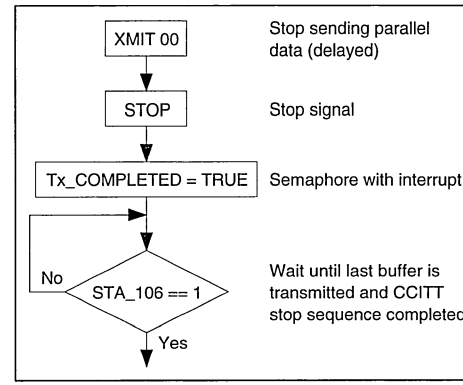
Figure 26



Note : (1) At this step the host can check that the corresponding ***DTTBSx*** buffer is empty (equal to $00), otherwise it is an error.

To stop properly the transmission, without loss of Data (see Figure 27).

Figure 27



IV.7.4 - Error Detection

Error occurs when the ST75C52/520 need some bits from the transmit buffer DTTBSx and this buffer is empty. This condition is called "Underflow".
This error is signaled in the bit ***ERR_TX*** of the ***SYSERR*** byte, and generates an interrupt IT0. To clear the error a ***CSE 01*** command must be issued.

An Underflow condition occurs when :

- in synchronous mode : the host processor "forgets" to feed the current ***DTTBSx*** buffer,
- in HDLC mode : when, while inside a frame, the host processor "forgets" to feed the current ***DTTBSx*** buffer. An abort frame is transmitted in place of the regular Buffer.

When an underflow condition occur the host must restart the whole parallel initialization, as explained above.

IV.7.5 - Synchronous Mode

IV.7.5.1 - Description

In synchronous mode the ST75C52/520 transmits the bits contained in the DUAL Ram Buffer without any modification. It starts with the Bit 0 of the ***DTTBF0[0]*** byte.

IV.7.5.2 - Status Word Format

The Transmit Status Bytes ***DTTBS0*** or ***DTTBS1*** have the same following meaning :

Table 12

DTTBSx **in Synchronous Mode**			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 2 .. 8 Other	Buffer empty. 1 Byte to transmit (***DTTBFx[0]***). 2 Bytes to transmit (***DTTBFx[0]*** and ***DTTBFx[1]***). .. 8 Bytes to transmit (***DTTBFx[0 .. 7]***). Not allowed.
Other	7 .. 4	0	Reserved, must be 0.

This status byte must be written by the Host, after filling the corresponding data buffer ***DTTBFx[0..7]*** with the right number of data bytes to transmit.
This status byte is cleared by the ST75C52/520, just before generating the ***IT2*** interrupt.

IV.7.6 - HDLC Mode

IV.7.6.1 - Description

In HDLC mode the ST75C52/520 transmits the data bytes contained into the DUAL Ram buffer packed inside an HDLC frame. The mechanism is as follows :

- while the Host has no frame to transmit, that is: as long as ***DTTBSx*** equals $00, the ST75C52/520 transmits the HDLC Flag $7E.
- when the Host wants to send some data, it feeds the buffer with some data bytes to transmit (between 1 and 8) and set the ***BUFF_SFRM*** bit in the ***DTTBSx*** status buffer.
  At that time the ST75C52/520 start sending data contained in the Buffer, computing the CRC and performing "zero insertion" if needed.
- when the host wants to send additional data (within the same frame) it feeds the buffers just like in synchronous mode. If an Underflow condition occurs, the ST75C52/520 will abort the frame by sending 8 consecutive "1", and the Host must restart the whole parallel initialization.
- when the host wants to close a frame, it set the ***BUFF_EFRM*** bit in the ***DTTBSx*** status buffer. At that time the ST75C52/520 will send the contents of the buffer, then send the CRC and an HDLC closing flag $7E.
- if the Host, wants to abort a frame (while sending a frame) it set the ***BUFF_FRAB*** bit in the ***DTTBSx*** status buffer. At that time, as soon as the last buffer will be transmitted, the ST75C52/520 will send 8 consecutive "1" and wait for the next buffer.

IV.7.6.2 - Status Word Format

Table 13

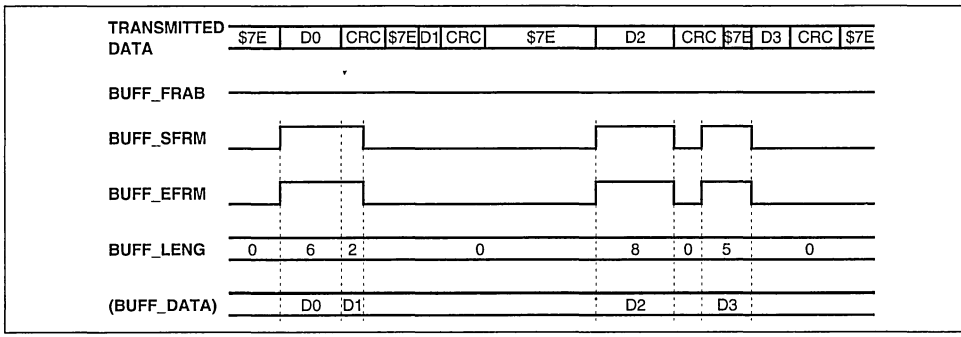
DTTBSx **in HDLC Mode**			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 2 .. 8 other	Buffer emty. 1 Byte to transmit (***DTTBFx[0]***). 2 Bytes to transmit (***DTTBFx[0]*** and ***DTTBFx[1]***). .. 8 Bytes to transmit (***DTTBFx[0 .. 7]***). Not allowed.
BUFF_SFRM	4	0 1	Data stream. Start of frame : the buffer is a beginning of frame.
BUFF_EFRM	5	0 1	Data stream. End of frame : the buffer will be followed by the transmission of the CRC and closing flag.
BUFF_FRAB	6	0 1	Data stream. Abort frame : 8 consecutive "1" will be transmitted (whatever ***BUFF_LENG*** is).
Other	7	0	Reserved, must be 0.

Notes : 1. A buffer can have ***BUFF_SFRM*** and ***BUFF_EFRM*** set in the same ***DTTBSx*** byte, this means that the frame transmitted is short (between 1 and 8 Bytes long).

2. An ending frame (with ***BUFF_EFRM*** set) must have at least ONE byte of data to transmit.

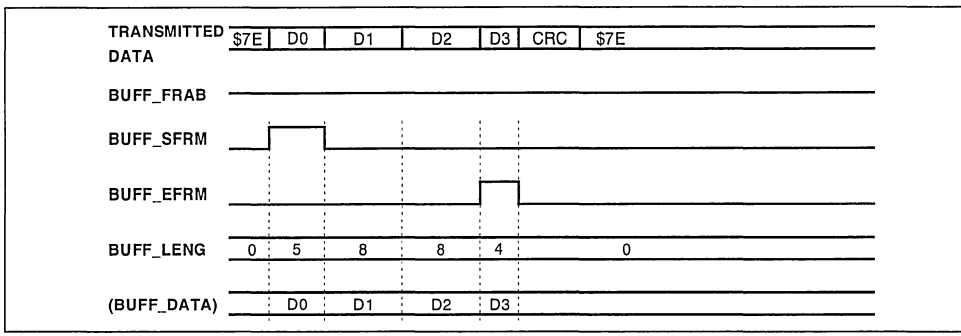
IV.7.6.3 - Single Short Frame

Figure 28



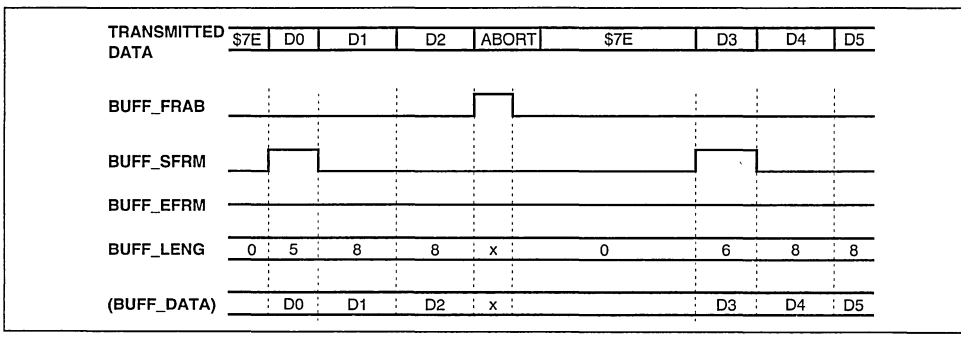
IV.7.6.4 - Long Frame

Figure 29



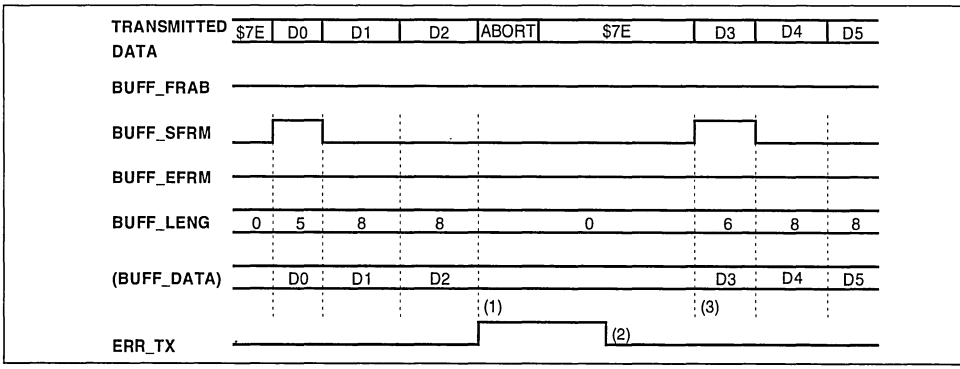
IV.7.6.5 - Abort Frame

Figure 30



IV.7.6.6 - Abort due to Underflow

Figure 31



Where : 1. The Underflow condition appears when the ST75C52/520 needs, inside a frame, some bytes to transmit and that the corresponding buffer is empty.

2. The ***ERR_TX*** bit is cleared with a ***CSE 01*** Command.

3. After an Underflow condition restart the initialization of the parallel mode and use the buffer number 0

IV.8 - Receiving In Parallel Mode

IV.8.1 - Description

When the ***STA_109*** (CD) signal goes on, the user must select the parallel mode by enabling the parallel link with ***RX_SDATA*** set in the ***SERIAL RX*** command. After that the ST75C52/520 will write received data into the DUAL Ram Buffer ***DTRBS0***. Note that for a proper operation, each time the ***STA_109*** goes on the ***SERIAL*** command must be send.

IV.8.1.1 - Initialization

The host processor must enable the ***IT3*** receive interrupt first.
Then it must empty the two ***DTRBS0*** and ***DTRBS1*** registers by writting $00 at these locations.
Then it must send the ***SERIAL RX*** command.

As soon as the first ***IT3*** interrupt appears, the host must proceed with the ***DTRBS0*** buffer.

IV.8.1.2 - Loss of Carrier

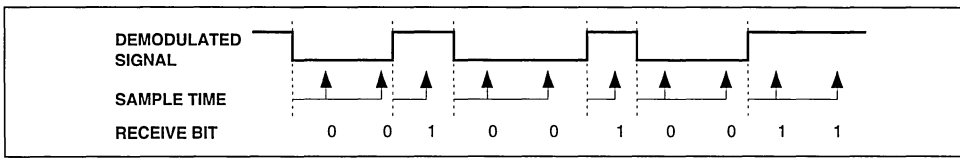
Each time a loss of carrier appears the ST75C52/520 stops updating the Data buffer.

If the carrier reappers the host must proceed again with the initialisation sequence.

IV.8.1.3 - FSK Synchronization

The FSK Full Duplex demodulator uses an algorithm based on the transitions of the received signal. The synchronization mechanism is adjusted with each signal transition in order to sample the demodulated signal at the midle of the bit (see Figure 32).

Figure 32



IV.8.2 - Modem Flow Chart

When in parallel data mode, each time the ST75C52/520 has received some bit of data it executes the following routine (see Figure 33).

Where ***X*** start with the value 0 and toggle between 1 and 0.

IV.8.3 - Host Flow Chart

Hereafter are flowcharts to :
- establish a V.29 reception,
- receive synchronous data. This task is performed under interrupt,
- handle properly some temporary loss of carrier.

Establish the reception (see Figure 34).

These flowcharts show one CPU variable labeled IBUF which is necessary for the understanding of the mechanism, but there are different manners to implement it.

- IBUF : this is the number of the DUAL Ram Buffer currently in use by the Host processor. It starts with 0 an then alternates 1, 0, 1, 0 ...

The received bits are read by an interrupt routine (see Figure 35).

Figure 33

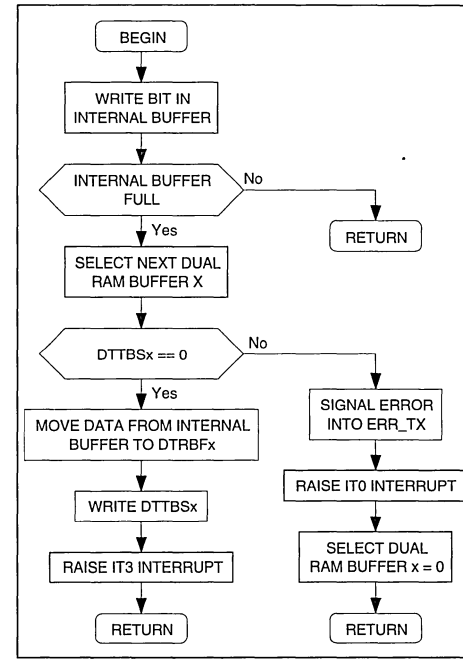


Figure 34

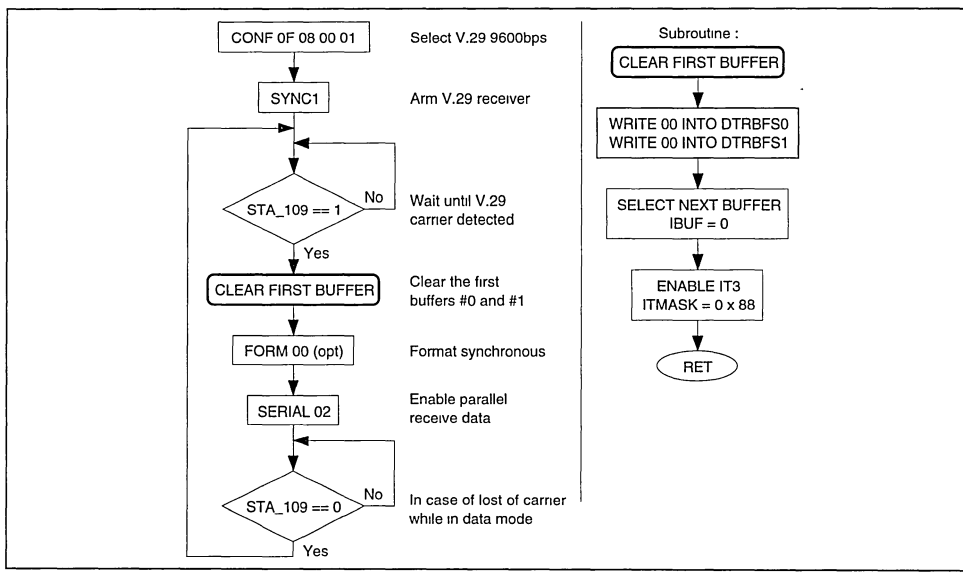
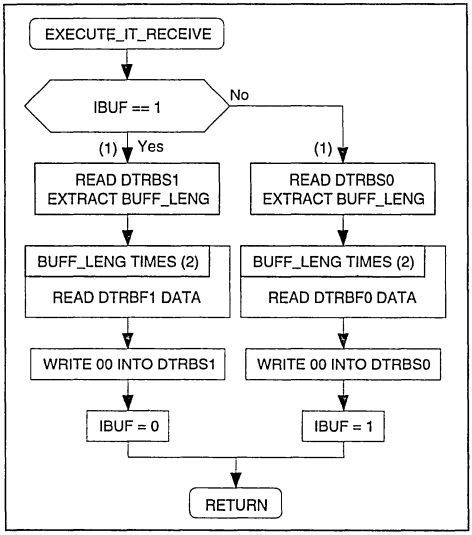


Figure 35



Notes : 1. At that step the host can check that the corresponding ***DTRBSx*** buffer is full (different from $00), otherwise it is an error.

2. This means read ***BUFF_LENG*** bytes, inside the Receive buffer ***DTRBFx*** starting from location ***DTRBFx[0]*** to ***DTRBFx[BUFF_LENG - 1]***. In synchronous mode, the ***BUFF_LENG*** is always 8 bytes, except when a ***STA_109*** lost appears in the middle of the buffer.

IV.8.4 - Error Detection

Error occurs when the ST75C52/520 has received some bits and that the buffer ***DTRBSx*** is not empty, this condition is called "Overflow".

This error is signaled in the bit ***ERR_RX*** of the ***SYSERR*** byte, and generates an interrupt IT0. To clear the error a ***CSE 02*** command must be issued.

An Overflow condition occurs when :

- in synchronous mode: the host processor "forgets" to empty the current ***DTRBSx*** buffer,
- in HDLC mode: when, while inside a frame, the host processors "forgets" to empty the current ***DTRBSx*** buffer.

When an Overflow condition occurs the host must restart the whole parallel initialisation.

IV.8.5 - Synchronous Mode

IV.8.5.1 - Description

In synchronous mode the ST75C52/520 writes the received bit into the DUAL Ram Buffer without any modification. It starts with the Bit 0 of the ***DTRBF0[0]*** byte.

IV.8.5.2 - Status Word Format

The receive Status Byte ***DTRBS0*** or ***DTRBS1*** have the same following meaning (see Table 14).

Table 14

DTRBSx in Synchronous Mode			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 2 .. 8 Other	Buffer emty. 1 Byte received (***DTRBFx[0]***). 2 Bytes received (***DTRBFx[0]*** and ***DTRBFx[1]***). .. 8 Bytes received (***DTRBFx[0 .. 7]***). Not used.
Other	7 .. 4	0	Not used.

The BUFF_LENG is always 8 except when a lost of carrier (***STA_109*** going to 0) happens.
This status byte is set by the ST75C52/520, just before generating the ***IT3*** interrupt.

IV.8.6 - HDLC Mode

IV.8.6.1 - Description

In HDLC mode the ST75C52/520 extracts from the received HDLC frame the Data information only. It reports, trough the DUAL Ram Buffer, only data information and frame validity. The mechanism is as follows :

- as long as the ST75C52/520 receives continuous HDLC Flag $7E, nothing happens. Note that the ST75C52/520 allows zero sharing between adjacent flags.
- when the ST75C52/520 receives some data, it removes inserted "zero" if needed, and starts to compute the CRC. As soon as its internal buffer is full, the ST75C52/520 writes the received data into the ***DTRBFx*** buffer and sets the ***BUFF_SFRM*** inside the ***DTRBSx*** status byte.
- when receiving additional data, the ST75C52/520 feeds the buffer just like in synchronous mode.
- when the ST75C52/520 receives a closing flag (which can be shared with the following opening flag) it compares the received CRC with its internal computation. It writes the contents of the received last data into the ***DTRBFx*** buffer, sets the ***BUFF_EFRM*** bit and reports any frame error in the ***DTRBSx*** register via the ***BUFF_ERRS*** bits. Reported errors are :
  CRC error (lowest priority) : the received CRC is not equal to the computed CRC. Some bits, inside the frame, are erroneous.
  Non Byte-Aligned frame (middle priority) : the received data bit count (after deletion of the "zero inserted"), between the opening and the closing flag, is not a multiple of 8.
  Aborted frame (highest priority) : the frame was aborted with at least 7 consecutive "1"
- an abort frame can be also detected, while in the inter frame mode, if instead of receiving $7E flag, the ST75C52/520 receive more than 7 consecutive "1". In this case only one Aborted frame is signaled, event if the "1" condition is maintained.

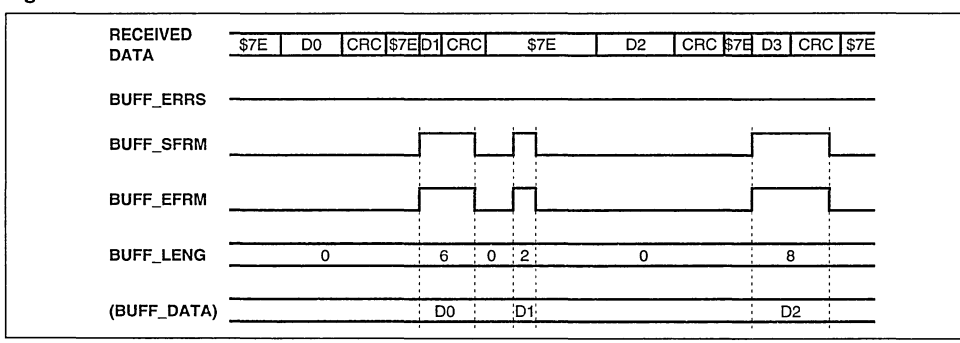
IV.8.6.2 - Status Word Format

Table 15

DTRBSx in HDLC Mode			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 2 .. 8 other	Buffer emty. 1 Byte received (***DTRBFx[0]***). 2 Bytes received (***DTRBFx[0]*** and ***DTRBFx[1]***). .. 8 Bytes received (***DTRBFx[0 .. 7]***). Not allowed.
BUFF_ERRS	5 .. 4	0 0 0 1 1 0 1 1	No error. CRC error. Non Byte-Aligned frame. Aborted frame.
BUFF_SFRM	6	0 1	Data stream. Start of frame : the buffer is a beginning of frame.
BUFF_EFRM	7	0 1	Data stream. End of frame : the buffer is a closing frame.

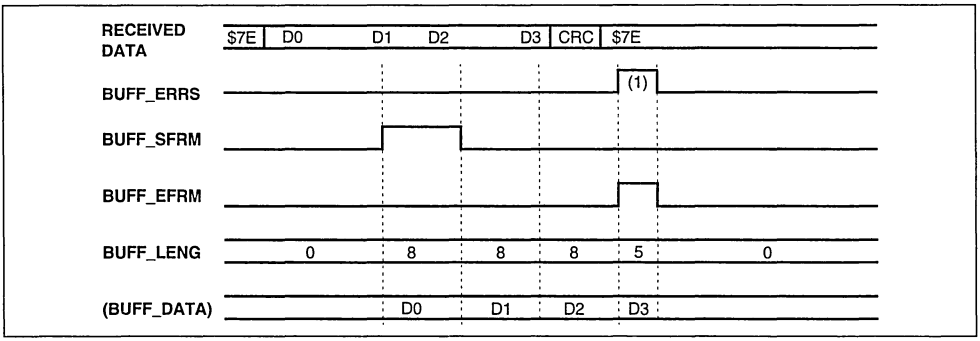
IV.8.6.3 - Single Short Frame

Figure 36



IV.8.6.4 - Long Frame

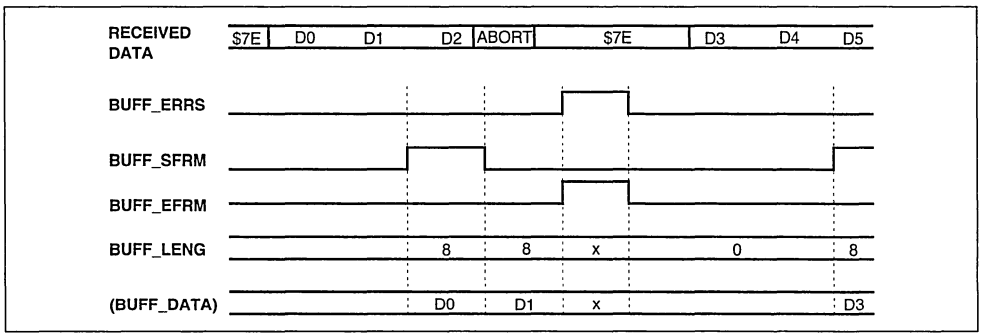
Figure 37



Note 1 : If error occurs during the reception, it is signaled in this last buffer.

IV.8.6.5 - Aborted Frame

Figure 38



V - TONE DETECTORS

For additional information about the TONE DETECTORS please refer to Chapter VIII of the ST75C52/520 Data Sheet.

V.1 - Computation of Tone Detector Coefficient and How to Change Them

1) Elementary Properties of IIR Filter

The filters included in the modem are biquad filter (see above) that is IIR filter. The most general form of the z transform of IIR can be written as :

$$H(z) = \frac{\sum_{i=0}^{M} b_i \cdot z^{-i}}{1 + \sum_{i=0}^{N} a_j \cdot z^{-j}}$$

The magnitude-squared response of a filter is defined as :

$$\left(\left| H\left[\exp\left(2 \cdot \pi \cdot j \cdot \frac{f}{Fe} \right) \right] \right| \right)^2$$

The poles and zeros of a magnitude-squared function are distributed with mirror-image symmetry with respect to the unit circle in the Z plane. The filter is stable if all poles of the transfer function are situated inside the unit circle in the z-plane. The group delay of a filter is a measure of the average delay of the filter as a function of frequency. A desirable group delay characteristic is approximately constant over the passband of the filter.

Choosing a filter type :

The well-known analog filter classes are the Butterworth, Chebyshev and Cauer or elliptic filter. If the characteristic of the filter is not severe, a Butterworth filter can be used because of the flat response in the passband and the small group delay . The drawback is a relatively wide transition band. If the characteristics of the filter are severe with a narrow transition band for instance, an elliptic filter should be chosen in order to minimize filter order. The drawback is a very non uniform group delay , especially a large value when approaching the passband edge.

2) Computation of Tone Detector Coefficients

We will take a Butterworth filter for a simplicity of tuning :

We have

$$B1\ (C,z) = \left(C_0 \cdot \frac{C_5 + 2 \cdot C_3 \cdot z^{-1} + 2 \cdot C_4 \cdot z^{-2}}{1 - 2 \cdot C_1 \cdot z^{-1} - 2 \cdot C_2 \cdot z^{-2}} \right) \cdot C_6 \cdot \frac{C_{11} + 2 \cdot C_9 \cdot z^{-1} + 2 \cdot C_{10} \cdot z^{-2}}{1 - 2 \cdot C_7 \cdot z^{-1} - 2 \cdot C_8 \cdot z^{-2}}$$

Let $C_3 = C_9 = 0$, $C_5 = C_{11} = 1$, $C_4 = C_{10} = -0.5$

This :

$$B1\ (C,z) = C_0 \cdot \frac{1 - z^{-2}}{1 - 2 \cdot R \cdot \cos(\theta) + R^2} \cdot C_6 \cdot \frac{1 - z^{-2}}{1 - 2 \cdot R_a \cdot \cos(\theta 1) + (R_a)^2}$$

with R = Ra

$C_1 = R \cdot \cos(\theta)$, $C_7 = R \cdot \cos(\theta 1)$,

$C_2 = -\frac{R^2}{2}$, $C_8 = -\frac{R^2}{2}$

This method is available for any frequency in the 400Hz -3kHz band. The radius of the tone detector pole was chosen so that each filter has a high Q factor without being unstable.
We choose R in the Table 16.

$$\theta = 2 \cdot \pi \cdot \frac{Fo}{Fe}$$

Were Fo is the desired center frequency and Fe is the sample frequency (Fe = 7200Hz).

We take two different filters, first one is centered on (Fo - Fa), second one on (Fo + Fa), were Fa is the frequency offset. The value of Fa is approximately 72% of the band width divided by 2.

$$\theta = 2 \cdot \pi \cdot \frac{Fo - Fa}{Fe} \qquad \theta 1 = 2 \cdot \pi \cdot \frac{Fo + Fa1}{Fe}$$

The value of Fa should be equal to Fa1. However, Fa may be choosen 1% smaller than Fa1 to compensate for the fact that the overall cascade response is not perfectly symmetrical.

The values for the coefficients C0 and C6 that give unity gain were measured and plotted versus center frequency Fo. Three equations corresponding to three linear approximations result :

$$400 \le f \le 1400 \quad C_0 = \frac{\frac{5}{16} \cdot f + 100}{32768} \quad (C0_f)$$

$$1400 \le f \le 2400 \quad C_0 = \frac{\frac{3}{32} \cdot f + 400}{32768} \quad (C01_f)$$

$$2400 \le f \le 3000 \quad C_0 = \frac{\frac{1}{8} \cdot f + 325}{32768} \quad (C02_f)$$

Figure 39

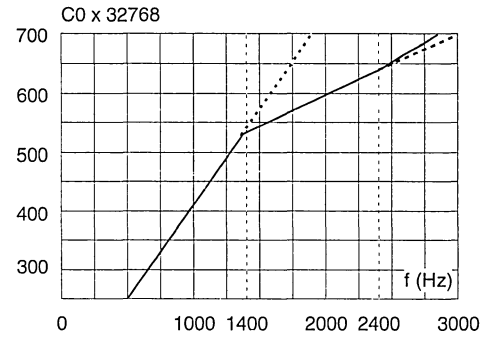


Table 16

Frequency Range	400-800Hz	800-1200Hz	1200-200Hz	2000-3000Hz
-((R x R) / 2) x 32767	$C084	$C0C4	$C0E6	$C147
R	0.996	0.994	0.993	0.990

V.1.1 - Computation of Tone Detector Coefficients using Mathcad Software

Mathcad software is a popular software from mathsoft Inc. We simply give an example of computation using this software to illustrated the above theory.

Tuning of coefficient for a band pass 1850Hz filter

*** Enter filter characteristic ***

Sampling Frequency Fe = 7200
Central Frequency Fo = 1850
Frequency offset Fa = 18

*** Define some Mathcad constant and formula ***

Default sampling Frequency Fe = 7200

Complex constant $j = \sqrt{-1}$

Complex Frequency Function $Z(f) = \exp\left(2 \cdot \pi \cdot j \frac{f}{Fe}\right)$

dB Function $dB(x) = 20 \cdot \log(x + 10^{-5})$

Hexadecimal Function H(x) = if (x < 32768, X, X - 65536)

Hexa to Fractional Function $D(x) = \frac{H(x)}{32768}$

Hexadecimal Display Function X(x) = if (x < 0, 65536 + x, x)

The transfer function is $B1(C,z) = C_0 \frac{C_5 + 2\ C_3\ z^{-1} + 2\ C_4\ z^{-2}}{1 - 2\ C_1 \cdot z^{-1} - 2\ C_2 \cdot z^{-2}}\ C_6 \frac{C_{11} + 2\ C_9\ z^{-2} + 2\ C_{10}\ z^{-2}}{1 - 2\ C_7\ z^{-1} - 2\ C_8 \cdot z^{-2}}$

*** Extract Pole Location ***

Band pass center Frequency $\theta = 2\pi \cdot \frac{Fo - Fa}{Fe}$, $\theta 1 = 2\pi \cdot \frac{Fo + Fa}{Fe}$

Take care to have the good value of radius

$300 \le Fo \le 800$ R : = 0.996 $1200 \le Fo \le 2000$ R : = 0.993
$800 \le Fo \le 1200$ R : = 0.994 $2000 \le Fo \le 3000$ R : = 0.990

Fo = 1.85 · 103 then **Pole radius** : R = 0.993

*** Compute coefficients ***

Coefficients Formula k = 0 .. 11

$C_0 = \frac{\frac{3}{32} \cdot Fo + 400}{32768}$ $C_1 = R \cdot \cos(\theta)$ $C_2 = \frac{-R \cdot R}{2}$ $C_3 = 0$ $C_4 = -0.5$ $C_5 = 1 - \frac{1}{32768}$

$C_6 = \frac{\frac{3}{32} \cdot Fo + 400}{32768}$ $C_7 = R \cdot \cos(\theta 1)$ $C_8 = \frac{-R \cdot R}{2}$ $C_9 = 0$ $C_{10} = -0.5$ $C_{11} = 1 - \frac{1}{32768}$

Coefficients in Hexadecimal form : C_k =

H(023DH)
H(0FC74H)
H(0C0E6H)
H(0)
H(0C000H)
H(07FFFH)
H(023DH)
H(0F877H)
H(0C0E6H)
H(0)
H(0C000H)
H(07FFFH)

Coefficients to be downloaded into the Modem with TDWC commands

*** Compute Transfer Function ***

$C_k = \frac{C_k}{32768}$

Frequency Range : f = 0,1 .. 3000

$F1_f$ = dB (|B1(C,Z(f))|) $F1_{1850} = 0.387$dB

*** Display Transfer Functions ***

Figure 40

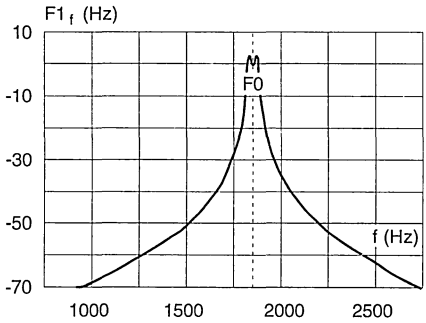
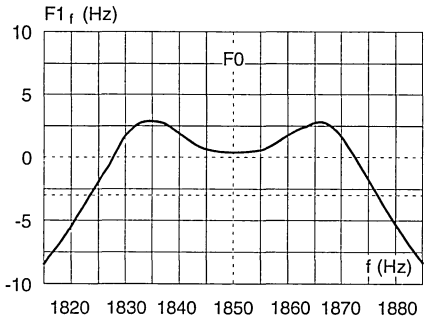


Figure 41



V.1.2 - Computation of Tone Detector Coefficients using TD Software

Tone Detector Description

Refer to the ST75C52/520 Data Sheet for detailed description of the tone detectors, Figure 2 (ST75C52/520 Data Sheet) for the Biquadratic IIR filter, Figure 3 for the Power estimator, Figure 4 for the tone detector wiring address (first half) and Figure 5 for the tone detector wiring address (second half). There are 16 programmable tone detector cells available. Each cell contains a 4th order IIR(biquadratic) filter, energy estimator consisting of an absolute value measurement and a 1st order low pass filter, 2-input comparator, and a static level. Detect information is sent to status word ***TONEDET***. The user has the possibility of sending commands to the data pump to program the tone detectors for almost any desired transfer function. For each cell, the command ***TDWC*** can be used to program the 12 coefficients of the 4th order IIR filter (C0 to CB), the 1st order low pass filter coefficient, and the static level. The command ***TDWW*** can be used to program the wiring between cells for cascading and signal routing. One is free to program the IIR input, energy estimator input, and comparator + and - inputs.

Program TD Description

The user has the possibility of calculating his proper coefficients and determining the corresponding ***TDWC*** and ***TDWW*** commands manually but, the program TD was written to facilitate this task. The purpose of this chapter is to give the operating instructions for using program TD for quick development of the code needed to program the detectors.

Compatability and Input/Output

Program TD is written in FORTRAN and is executable on almost any PC with hard disk using MS-DOS. Input is from the keyboard and output is on the screen. Also, several useful files are generated by the program :

a) TD.SPC - contains trace of filter specifications given by user
b) TD.RES - shows floating-point frequency response of specified filter
c) TD.CCI - CCI commands needed for the data pump for specified filter

Starting the Program

To start the program, the user should first create a directory and load program TD.EXE into the directory. The command TD is now sent while in the created directory to start program execution. The program will then display ENTER TYPE. The following paragraph will describe the filter types.

Choosing a Filter Type

Four possible filter types are available to the user with the following characteristics :

BUTTERWORTH : This type of filter has a maximally flat pass-band with no ripple. It has multiple zeroes at half the sampling frequency (3600Hz) or D.C. or at the center of the band for band-stop configurations.

CHEBYCHEV : Equiripple in the pass band and flat response in the stop band which is particularly useful for band rejection filtering.

INVERSE CHEBYCHEV : Ripple-free pass band and more efficient than the Butterworth. For the same target design template, a lower order filter is necessary. Equiripple stop-band characteristics render this type useful for band-pass, low-pass or high-pass filtering.

ELLIPTIC : This type of filter is the most efficient and can have narrow transition bands. However, it is characterized by ripple in the pass and stop bands. Once the type is chosen, the program will ask for LOPASS, HIPASS, BANDPASS, or BAND REJECT filters.

Choosing a Filter Order

For all but Elliptic types, the program TD will ask the desired order. The user must specify the number of cascaded biquads (2nd order sections) desired.

Defining and Optimizing a Target Template

The corner frequencies for pass band and/or stop band are required by the program, and attenuation in the pass band and/or stop band for all types except Butterworth. These attenuations are in dB referenced from the input to the output. The program now calculates the transfer function in the Z domain displaying locations of poles and zeroes, and the required number of 4th order tone detector cells needed. This information is displayed on the screen and output to file TD.SPC. For the case of an Elliptic type, the order required is calculated from the transition band specified by the user, rather than specified directly by the user as for the other types. The order may be too high for the number of cells available or desired. The user may re-specify the filter. In general, one or more of the following steps may be performed, if the application enables it, to decrease the required order of an Elliptic type filter.

- change from band pass or band reject to low pass or high pass,
- increase difference between pass band and stop band frequencies,
- increase the pass band ripple and/or decrease the stop band atten.

Using an iterative process, one can optimize the target specification of the filter before continuing to the next step.

Displaying the Ideal Frequency Response

The program TD will now calculate the frequency response of the specified filter and normalize coefficients to avoid overflow in the DSP ALU. The program now proceeds with the display of the frequency response on the screen. The user is asked by the program TD to specify start, stop, and step frequencies to facilitate interest in a particular portion of the frequency response. Once displayed, the program asks if the response is to be re-displayed allowing the user to change the frequency ranges. The desired frequency response is calculated in floating-point while the actual program implemented in the data pump uses a fixed-point DSP. In most cases, there should not be too much difference between the two calculation methods if the transition bands are not too narrow in the case of Elliptic types or the order is not too high for all types. At this point, the user has a better idea of the transition bands for Butterworth and Chebychev designs and also the unity gain loss. The normalization process may, in some cases to avoid overflow, result in an attenuation in the pass band or unity gain loss. Increasing the order of the Butterworth or Chebychev filters may be necessary for a narrower transition band. Widening of the transition band may be necessary for diminuing the unity gain lossof an Elliptic filter. In any case, the frequency response is written to file CP.RES for reference after the end of program execution. This can be especially useful for reference if several optimization attempts are desired.

Choosing the Used Cells

The program TD will now ask for the starting cell number (a number from 0 to F). The program will write CCI instructions for programming n (n= order/4) cells starting from the given address. The program cascades the biquadratic filters. However, only the last comparator and static level are used for the detection decision. This means that, eventually, the comparators or static levels for intermediate cells could be programmed for other functions. If the user, for example chooses 1 for the starting address, and there are 3 cells used, then the detection bit for this configuration will be available in ***TONEDET(0)*** position 3 (refer to ST75c5x data sheet). The user should choose a relatively low starting address beginning with the first unused position, if possible. This is because the execution time of the detectors in the non-idle mode may necessitate the utilizaton of less than 16 cells (NTDCELL .lt. 16 refer to ram mapping application note). In this case the higher cell numbers are not executed.

Selecting the Detection Thresholds

The detection threshold is now asked for by the program to define the minimum detectable input signal level at a pass band frequency with 0dB unity gain loss. The program will remind the user of the actual unity gain loss due to normalization and, in general, the desired threshold must be lowered by the number of dB in the unity gain loss. However, threshold levels lower than -50dBm are not reliable as the minimum dynamic range of the detectors will be surpassed.

Selecting the Energy Estimator Time Constant

The energy estimator time constant is now asked for by the program and the user will specify the value in milliseconds. A typical value of 8 is used for the default tone detectors but, if the user designs a filter with a particularly large group delay, he should also increase this value to avoid undesirable transients in the detection decision. Please note that group delay calculation is beyond the scope of this program and must be calculated by other techniques from the coefficients in TD.SPC.

Example Listings

The following listings give an example printout of the files TD.SPC, TD.RES, TD.CCI for a Butterworth 8th order low pass filter with cut-off frequency of 1000Hz.

```
EXAMPLE FOR 8th ORDER BUTTERWORTH
LPF FC=1000HZ, TH=-40dBM

          TD.SPC
          ------

 ENTER TYPE: 1 BUTTERW, 2 CHEBY, 3 ICHEBY, 4 ELLIP
    1
 ENTER 1 LOPASS, 2 HIPASS, 3 BPASS, 4 BREJ
    1
 ENTER NUMBER OF CASCADED BIQUADS DESIRED
    4
 ENTER BAND EDGE IN UN-NORMALIZED HZ
  1000.000
 Z PLANE
 #,   ZEROS  (REAL,  IMAG),      POLES (REAL, IMAG)
 1     -1.000000      0.000000      0.367029      0.085334
 2     -1.000000      0.000000      0.392676      0.259992
 3     -1.000000      0.000000      0.450892      0.446792
 4     -1.000000      0.000000      0.559214      0.653640
 5      1.000000      0.000000      1.000000      0.000000

          2 4TH ORDER TONE DETECTOR CELLS NEEDED !

 F(Z) = (Z*Z + B1Z + B2)/(Z*Z + A1Z + A2)
      1    2.000000    1.000000      -0.734059    0.141992
      2    2.000000    1.000000      -0.785351    0.221790
      3    2.000000    1.000000      -0.901784    0.402926
      4    2.000000    1.000000      -1.118428    0.739966

               TD.RES
               ------

Freq(Hz):                                                Gain(dB):
---------                                                ---------
    0.************************************************      0.0
  100.************************************************      0.0
  200.************************************************      0.0
  300.************************************************      0.0
  400.************************************************      0.0
  500.************************************************      0.0
  600.************************************************      0.0
  700.************************************************      0.0
  800.************************************************     -0.1
  900.***********************************************      -0.6
 1000.*********************************************        -3.0
 1100.*****************************************            -8.3
 1200.*********************************                   -15.0
 1300.****************************                       -21.7
 1400.**********************                             -28.3
 1500.***************                                     -34.6
 1600.*********                                           -40.8
 1700.***                                                 -46.9
 1800.                                                    -53.0
 1900.                                                    -59.1
 2000.                                                    -65.2
 2100.                                                    -71.4
 2200.                                                    -77.8
 2300.                                                    -84.3
 2400.                                                    -91.2
 2500.                                                    -98.4
 2600.                                                   -100.0
 2700.                                                   -100.0
 2800.                                                   -100.0
 2900.                                                   -100.0
 3000.                                                   -100.0
 3100.                                                   -100.0
```

```
                    TD.CCI
                    ------

; 4TH ORDER BIQUAD CELL 9 COEFS
CCI TDWC 9 0 1B 1A
CCI TDWC 9 1 FA 2E
CCI TDWC 9 2 EA F6
CCI TDWC 9 3 00 40
CCI TDWC 9 4 00 20
CCI TDWC 9 5 00 40
CCI TDWC 9 6 EE 1B
CCI TDWC 9 7 43 32
CCI TDWC 9 8 CF F1
CCI TDWC 9 9 00 40
CCI TDWC 9 A 00 20
CCI TDWC 9 B 00 40
; 4TH ORDER BIQUAD CELL A COEFS
CCI TDWC A 0 12 20
CCI TDWC A 1 B6 39
CCI TDWC A 2 37 E6
CCI TDWC A 3 00 40
CCI TDWC A 4 00 20
CCI TDWC A 5 00 40
CCI TDWC A 6 9E 23
CCI TDWC A 7 94 47
CCI TDWC A 8 A5 D0
CCI TDWC A 9 78 47
CCI TDWC A A BC 23
CCI TDWC A B 78 47
; POWER ESTIMATOR AND BIQUAD INPUTS
CCI TDWW 9 0 19 02
CCI TDWW A 0 1A 19
; COMPARATOR - AND + INPUTS
CCI TDWW A 1 3A 2A
; DETECTION THRESHOLD AT   -40.00 DB
CCI TDWC A 20 70 00
; ENERGY TIME CONSTANT IS     8.00 MS
CCI TDWC A 10 E3 08
; CLEAR INTERNAL VARIABLES OF ALL USED CELLS
CCI TDZ 9
CCI TDZ A
```

V.2 - DTMF Detection

The way the DTMF detector is implemented is differential. First we split the 300Hz - 3kHz band signal in upper band and lower band. These two signals feed the input of 2 times 4 band filters (tuned on the 8 DTMF frequencies). To detect a valid DTMF signal, we check that the ratio between the upper band and the lower band is within plus or minus 8dB. Then we check if only one band pass detector is higher than the half band signal (either upper or lower band).

STAOPT0 and ***STAOPT1*** (in the optional status) indicate the tone detectors ***TDT0*** to ***TDT15***. In this receive mode the 12 last tone detectors are set to detect the DTMF frequencies (the first 3 Tone detectors are unchanged).

Table 17

TDT0	:	440Hz (unchanged)
TDT1	:	Wide Band (unchanged)
TDT2	:	Call Progress low pass 650Hz (unchanged).
TDT3	:	Not used
TDT4	:	Low Pass 960Hz filter (Chebishev order 8)
TDT5	:	High Pass 1190Hz filter (Chebishev order 8)
TDT6	:	Not available
TDT7	:	Not available
TDT8	:	Band Pass 697Hz Filter ± 12Hz
TDT9	:	Band Pass 770Hz Filter ± 13Hz
TDT10	:	Band Pass 852Hz Filter ± 15Hz
TDT11	:	Band Pass 941Hz Filter ± 16Hz
TDT12	:	Band Pass 1209Hz Filter ± 20Hz
TDT13	:	Band Pass 1336Hz Filter ± 22Hz
TDT14	:	Band Pass 1477Hz Filter ± 24Hz
TDT15	:	Band Pass 1633Hz Filter ± 26Hz

Figure 42

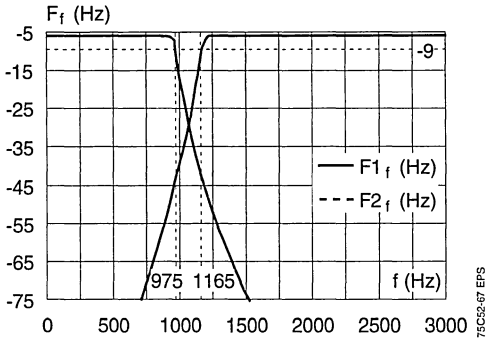


Figure 43

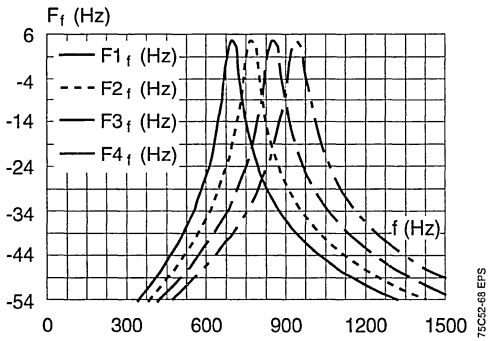
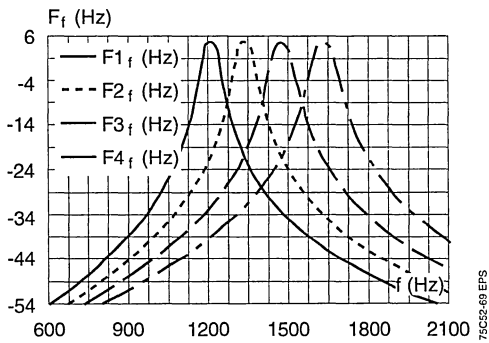


Figure 44



Hereafter are given the coefficients for the different filters used in DTMF detection.

Coefficients for Low Pass Filter from C0 to C23 are :
300h, 6BE2h, D117h, 401Ch, 200Eh, 401Ch, DB9h, 638Ch, CE22h, 20BFh, 105Fh, 20BFh, 1C6Eh, 592Ch, C934h, 4065h, 2032h, 4065h, 212Eh, 53EAh, C33Eh, 4C16h, 260Bh, 4C16h

Coefficients for High Pass Filter from C0 to C23 are :
1C8Eh, C933h, EB14h, BB3Fh, 2260h, 44C1h, 5975h, 249h, DA0Dh, B9FDh, 2301h, 4603h, 6E54h, 2BC0h, CC87h, A6E1h, 2C8Fh, 591Fh, 2DE8h, 3EE4h, C3C4h, 8000h, 4000h, 7FFFh

Coefficients for Band Pass 697Hz Filter from C0 to C11 are :
26Ah, 671Dh, C164h, 0, C000h, 7FFFh, 2A8h, 68B6h, C15Ah, 0, C000h, 7FFFh

Coefficients for Band Pass 770Hz Filter from C0 to C11 are :
2E8h, 6213h, C180h, 0, C000h, 7FFFh, 2CBh, 63F2h, C175h, 0, C549h, 756Dh

Coefficients for Band Pass 852Hz Filter from C0 to C11 are :
378h, 5BE9h, C1A4h, 0, C000h, 7FFFh, 30Eh, 5E22h, C199h, 0, C9FDh, 6C04h

Coefficients for Band Pass 941Hz Filter from C0 to C11 are :
35Bh, 574Fh, 408h, 54B4h, C1C8h, 0, C000h, 7FFFh, C1BDh, 0, CDFFh, 6401h

Coefficients for Band Pass 1209Hz Filter from C0 to C11 are :
5D6h, 3C1Eh, C237h, 0, C000h, 7FFFh, 44Bh, 3FF4h, C22Ch, 0, D60Eh, 53E3h

Coefficients for Band Pass 1336Hz Filter from C0 to C11 are :
6BAh, 2F45h, C269h, 0, C000h, 7FFFh, 4ABh, 33ADh, C25Fh, 0, D846h, 4F72h

Coefficients for Band Pass 1477Hz Filter from C0 to C11 are :
7A1h, 2058h, C2A3h, 0, C000h, 7FFFh, 52Bh, 2563h, C29Bh, 0, D9EFh, 4C1Fh

Coefficients for Band Pass 1633Hz Filter from C0 to C11 are :
891h, F53h, C2E1h, 0, C000h, 7FFFh, 5B2h, 1501h, C2DCh, 0, DB27h, 49B0h

V.3 - Default Tone Detectors ST75C52/520

Cell Description

The first cell (# 0) is programmed as a 440Hz tone detector (Call Waiting Detection) and is never changed whatever the DSP is doing. After a RESET (or INIT command) or any conf command, its parameters are set to detect the 440Hz single tone.
The Template of this filter is :

Table 18

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
Callwait	0	Band Pass	430,450Hz	360,530Hz	0.1	25

The second and third cell (#1 and #2) are used for Call progress detection. It is a Low pass filter with a cutt of frequency of 650Hz. This filter like the previous one is never changed.
The Template of this filter is :

Table 19

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
Cplow	1,2	Low Pass	0,650Hz	1000Hz	0.2	45

The cells number 3 and 4 are used for Call progress tone detection. It is a High pass filter with a cutoff frequency of 600Hz.
The Template of this filter is :

Table 20

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
Cphigh	3,4	High Pass	600,3600Hz	400Hz	0.2	45

While using the DTMF Mode (with a conf command) the cell 4 to 15 are overwritted with the DTMF detector parameters.

Cells number 5 and 6 are not used

The cell number 7 is used to detect the 462Hz single tone. It is a band pass filter.
The Template of this filter is :

Table 21

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
AN462	7	Band Pass	448,476Hz	340,540Hz	0.3	45

Cell number 8 is used to detect the 1100Hz single Tone.
The Template of this filter is :

Table 22

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
AN1100	8	Band Pass	1070,1130Hz	1000,1275Hz	0.3	45

Cell number 9 is used to detect the 1300Hz single Tone.
The Template of this filter is :

Table 23

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
AN1300	9	Band Pass	1275,1325Hz	1000,1600Hz	0.5	45

Cells number 10 and 11 are used to detect the V21.1650Hz Mark Tone.
The Template of this filter is :

Table 24

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
AN1650	10,11	Band Pass	1625,1675Hz	1500,1800Hz	0.1	45

Cells number 12 and 13 are used to detect ITU2100Hz Answer Tone.
The Template of this filter is :

Table 25

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
ANS2100	12,13	Band Pass	2080,2120Hz	2030,2170Hz	0.3	45

Cells number 14 and 15 are used to detect 2225Hz Answer Tone.
The Template of this filter is :

Table 26

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
ANS2225	14,15	Band Pass	2205,2270Hz	2140,2360Hz	0.5	45

Bit Description

Refer to the figure hereunder for the default wiring of the cells.
The 16 bits output of the tone detectors have the following meaning :

Table 27

Tonedet Word	Tonedet Bit	Filter Function	Biquad	Power	Level
0	0	Band pass 440Hz	Cell 0	Cell 0	Cell 0
0	1	Flat (signal > -21dBm)	-	Cell 1	Cell 1
0	2	Call progress low pass 650Hz	Cell 1,2	Cell 2	Cell 2
0	3	Call progress high pass 600Hz	Cell 3,4	Cell 3	Cell 3
0	4	CP High < CP Low	-	-	-
0	5	Not used	-	-	-
0	6	Not used	-	-	-
0	7	Band pass 462Hz	Cell 7	Cell 7	Cell 7
1	0	Band pass 1100Hz	Cell 8	Cell 8	Cell 8
1	1	Band pass 1300Hz	Cell 9	Cell 9	Cell 9
1	2	Band pass 1650Hz	Cell A,B	Cell B	Cell A
1	3	Not used	-	-	-
1	4	Band pass 2100Hz	Cell C,D	Cell D	Cell C
1	5	Not used	-	-	-
1	6	Band pass 2225Hz	Cell E,F	Cell F	Cell E
1	7	Not used	-	-	-

Note : Biquad of cells 5 and 6 are not used Power of cells 4, 5, 6, A, C and E are not used. Level of cells 4, 5, 6, B, D and F are not used.

Figure 45 : Tone Detector Wiring Address (first half)

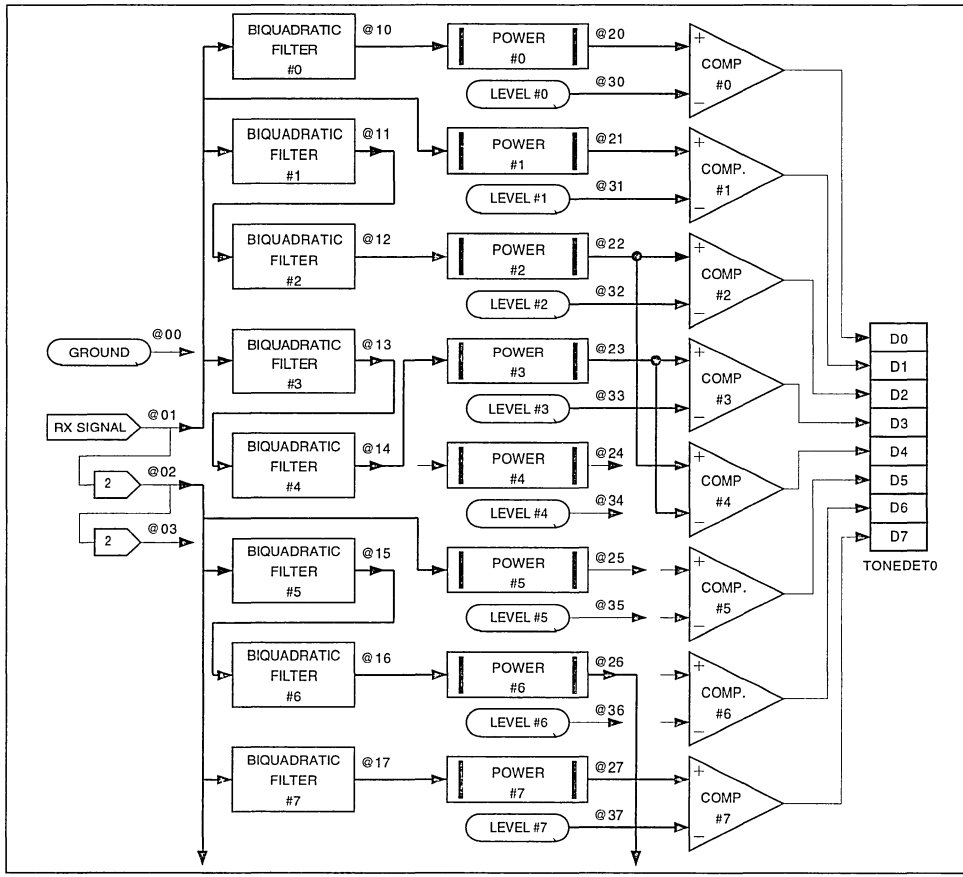
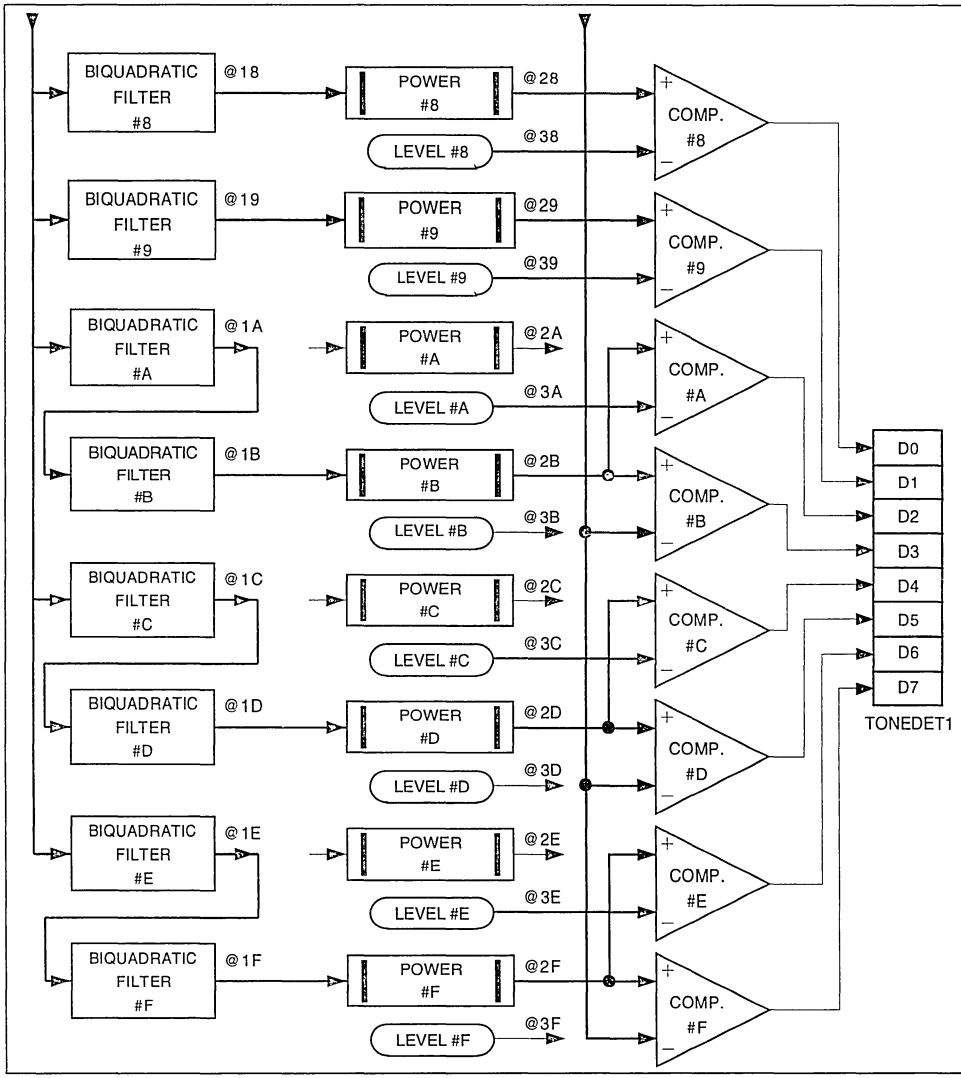
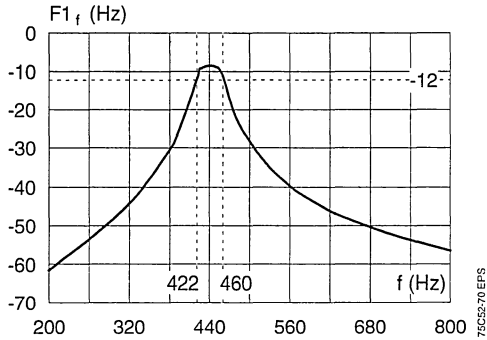


Figure 46 : Tone Detector Wiring Address (second half)



V.3.1 - Band Pass 440Hz Filter

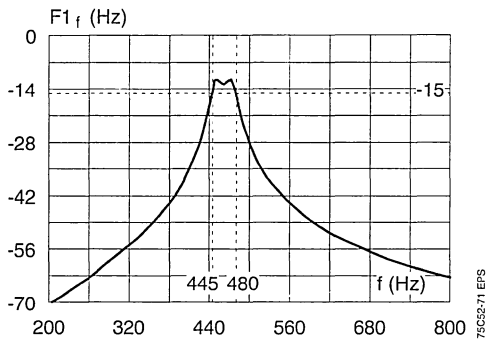
Figure 47



Coefficients for band pass 440Hz filter from Co to C11 are :
085h, 74D7h, C15Ah, 0,C000h, 7FFFh, 02D4h, 760F, C146h, 0, C000h, 7FFFh

V.3.2 - Band Pass 462Hz Filter

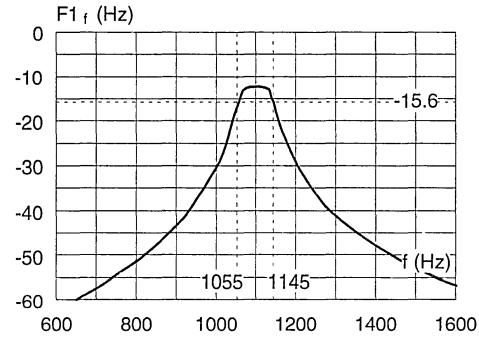
Figure 48



Coefficients for band pass 462Hz filter from C0 to C11 are :
066H, 7461H, C0E0H, 0 , C000H , 7FFFH, 0251H, 7583H, C0D5H, 0 , D555H, 5554H

V.3.3 - Band Pass 1100Hz Filter

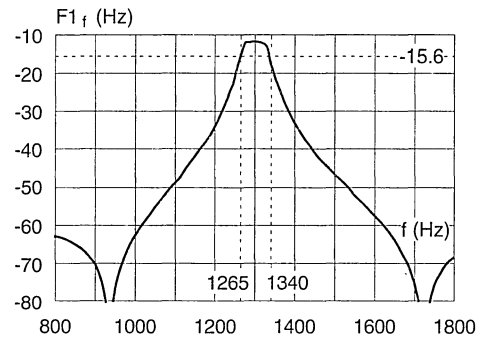
Figure 49



Coefficients for band pass 1100Hz filter from C0 to C11 are :
1FDh, 4551h, C263h, 0, C000h, 7FFFh, 64Dh, 4AC7h, C24Eh, 0, EC8Ah, 26EBh

V.3.4 - Band Pass 1300Hz Filter

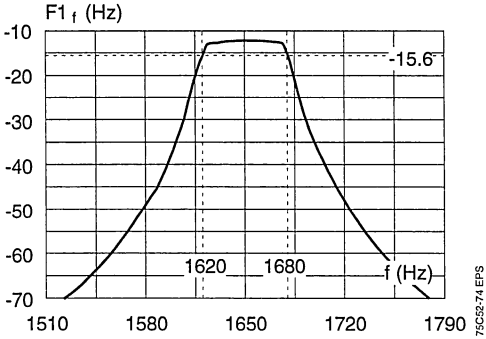
Figure 50



Coefficients for band pass 1300Hz filter from C0 to C11 are :
1DFh, 32BDh, C1FAh, F788h, 4000h, 7FFFh, C95H, 37C6h, C1F0h, A882h, 4000h, 7FFFh

V.3.5 - Band Pass 1650Hz Filter

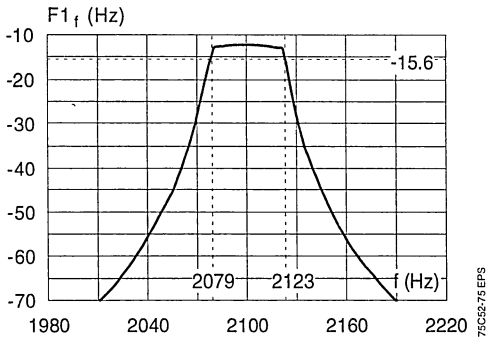
Figure 51



Coefficients for band pass 1650Hz filter from C0 to C23 are :
1C1h, F35h, C1C3h, 0, C000H, 7FFFh, 2ABh, 11C0h, C1C2h, 0, C000h, 7FFFh, 1E7h, D83h, C0BDh, 0, C000H, 7FFFh, 54Fh, 13B2h, C0BCh, 0, F0B6h, 1E91h

V.3.6 - Band Pass 2100Hz Filter

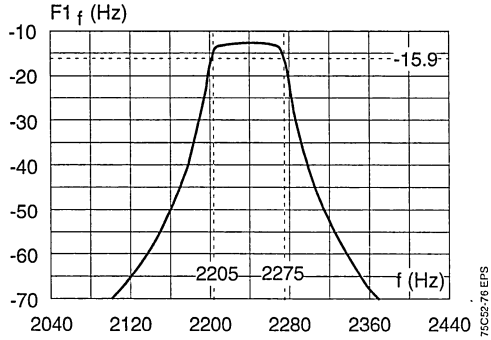
Figure 52



Coefficients for band pass 2100Hz filter from C0 to C23 are :
10Fh, E014h, C116h, 0, C000h, 7FFFh, 1E7h, DE39h, C115h, 0, C000h, 7FFFh, 13Dh, E13Eh, C074h, 0, C000h, 7FFFh, 468h, DCBFh, C073h, 0, F017h, 1FD1h

V.3.7 - Band Pass 2225Hz Filter

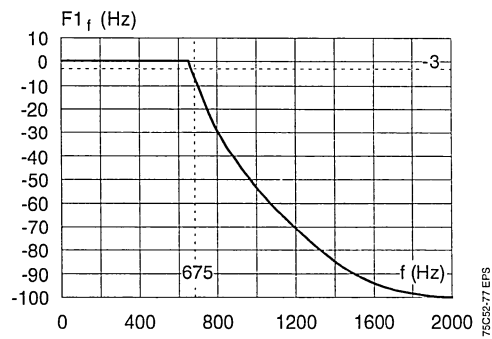
Figure 53



Coefficients for band pass 2225Hz from C0 to C23 are :
17Bh, D245h, C187h, 0, C000h, 7FFFh, 2DEh, CF76h, C183h, 0, C000h, 7FFFh, 206h, D3FAh, C0A4h, 0, C000h, 7FFFh, 672h, CD29h, C0A1h, 0, EFDFh, 203Fh

V.3.8 - Low Pass 650Hz Filter

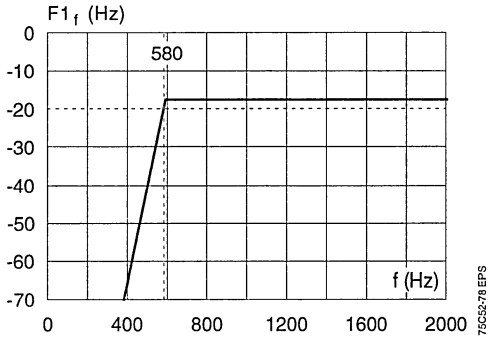
Figure 54



Coefficients for low pass 650Hz filter from C0 to C23 are :
230h, 6C2Ch, D1A8h, 3FFFh, 1FFFh, 3FFFh, 738h, 69CAh, CEFDh, 4000h, 2000h, 4000h, E73h, 6760h, CA21h, 400Eh, 2007h, 400Eh, 124Dh, 681Bh, C3ACh, 453Ch, 229Eh, 453Ch

V.3.9 - High Pass 600Hz Filter

Figure 55



Coefficients for high pass 600Hz filter from C0 to C23 are :
33C0h, 116Dh, F836h, 91ACh, 372Ah, 6E54h, 44C4h, 4527h, DB80h, 8000h, 4000h, 7FFFh, 3ED0h, 608Fh, CB9Fh, 8000h, 4000h, 7FFFh, 20ACh, 6C9Dh, C350h, 8001h, 4000h, 7FFFh

VI - CONTROL IN TRANSMIT MODE

VI.1 - Analog Hybrid Implementation

The following schematic shows the hybrid used on the ST9 SGS-THOMSON application board. This hybrid is designed to use the ST75C52/520's maximum performances (differential Input and Output). The operational amplifier U1 is only used for transmit purpose and powered between +12V and -12V. The reference signal (Pin 3 and 5 of U1) is tied to V_{CM} which is the reference for the ST75C52/520 sigma delta digital to analog convertor.

The user could connect Pin 3 and 5 of U1 to the analog ground. In such a case TXA1 and TXA2 must be connected to the 13.2kΩ resistors through capacitors (minimum 100nF).

The Transmit Gain is given by the ratio 22kΩ/13.2kΩ. It gives a default level of -9dBm on the telephone line. We have a full differential low-pass filter on transmit side before the DAA (second order) with Fc = 19.6kHz.

The return loss (very important parameter) could be adjusted by changing R3. In fact R3 value depents on the transformer. In our case R3 = 220Ω.

VI.2 - Default Level (Tones, Carriers, DTMF)

The following table gives the default level on the telephone line for all the possible carriers, the tones (predifined), and the DTMF signals.

Table 28

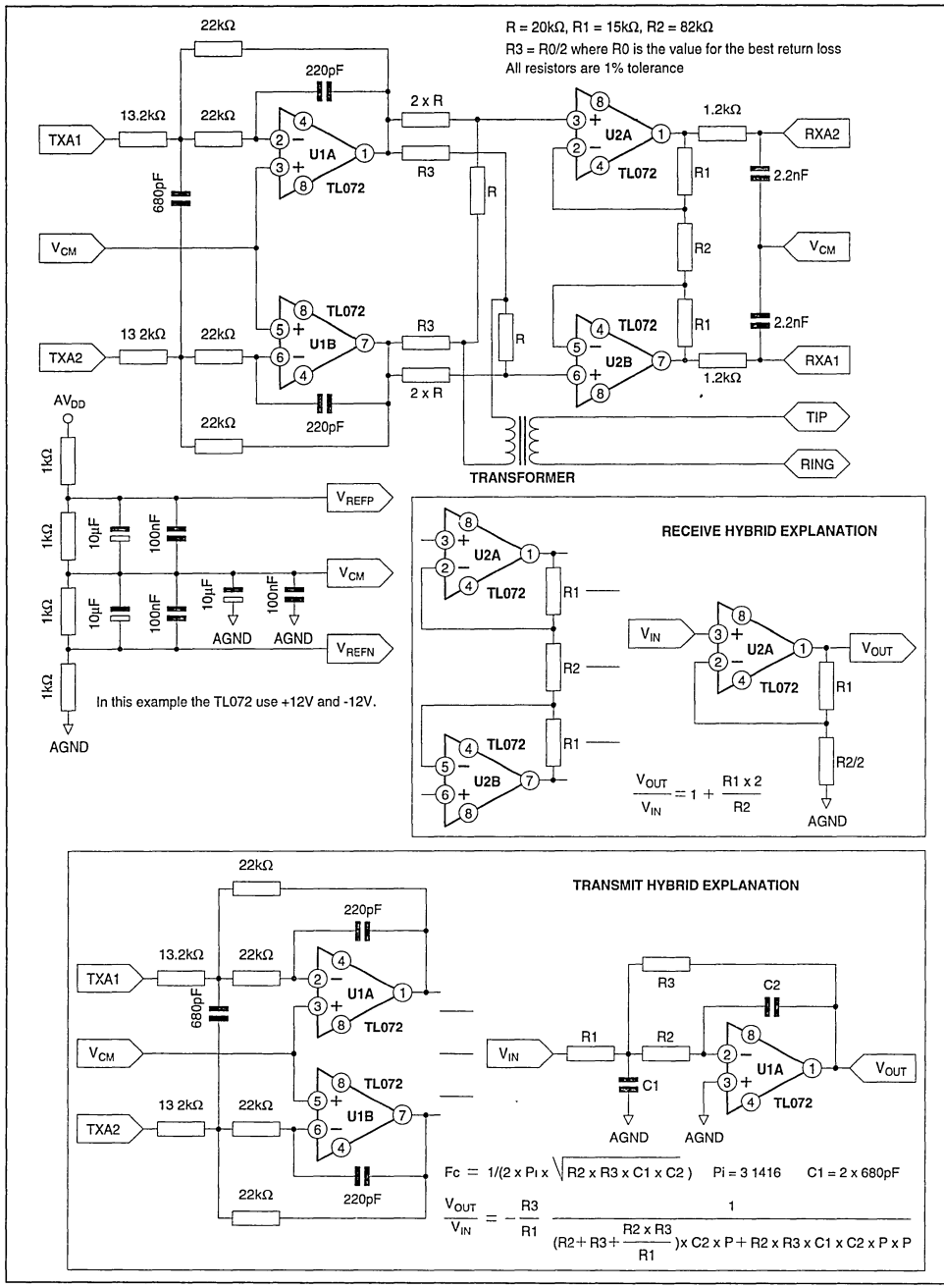
Signal	Default Level (dBm)
Bell 103 Originate	- 8.8
Bell 103 Answer	- 8.6
V.23 Originate	- 9.2
V.23 Answer	- 9.1
V.21 Originate	- 8.7
V.21 Answer	- 8.8
V.21 ch2	- 8.8
V.27 ter	- 8.9
V.29	- 8.8
V.17	- 9
V.33	- 9

Hybrid implementation for differential input and output (all the levels given in the chapter where measured with this schematic) (see Figure 56).

Table 29

Signal	Default Level (dBm)
DTMF0	- 9.32
DTMF1	- 9.31
DTMF2	- 9.33
DTMF3	- 9.37
DTMF4	- 9.3
DTMF5	- 9.32
DTMF6	- 9.36
DTMF7	- 9.29
DTMF8	- 9.32
DTMF9	- 9.35
DTMFA	- 9.4
DTMFB	- 9.39
DTMFC	- 9.39
DTMFD	- 9.39
DTMF*	- 9.29
DTMF#	- 9.35
2100Hz	- 9.38
2225Hz	- 9.46
1300Hz	- 9
1650Hz	- 9.13

Figure 56 : High Performance Differential Hybrid



VI.3 - How to Adjust Level Transmission

The user can adjust the level on the line with the SET OUTPUT GAIN (***SETGN***) command, which is done to set the Scaling Factor of the Transmit samples. ***SETGN*** is used for setting both the output level or the tone generators level. The gain value is given in the form of a 2's complement 16-bit value. ***SETGN*** parameters are given in two bytes :

Table 30

Field	Byte	Pos.	Value	Definition
GAIN_L	1	7..0	range FF*	Low byte of the 16-Bit gain value
GAIN_H	2	7..0	range 7F*	High byte of the 16-bit gain value

Table 31 : Examples

Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)
0	7FFF	- 5	47FA	- 10	287A
- 1	7214	- 6	4026	- 11	2413
- 2	65AC	- 7	392C	- 12	2026
- 3	5A9D	- 8	32F5	- 13	1CA7
- 4	50C3	- 9	2D6A	- 14	198A

The default level for DTMF is tuned to obtain -9dBm on the telephone line with the default value of SETGN (7FFF or 0dB). To increase the level of the DTMF the user must use the variable ***TGNBLK*** for the tone generator 0 and the the tone generator 1.

For example to obtain -4.5dBm on the line, the amplitude must be multipled by 1.73. The actual amplitude for tone generator 0 and tone generator 1 are located at address $11EE and $11F1. The default values are read with the ***MR*** command and the new values are initialized with the ***MW*** command.

The sequence is :

MR EE 11 : Read the tone generator 0 amplitude
COMREP[0] = 36 : Low byte value
COMREP[1] = 0F : High byte value
MW EE 11 50 1A : Write new tone generator 0 amplitude
MR F1 11 : Read the tone generator 1 amplitude
COMREP[0] = 7A : Low byte value
COMREP[1] = 13 : High byte value
MW F1 11 B1 21 : Write new tone generator 1 amplitude

The value which will be used for ***SETGN*** will add or substract dB to the new tone generator amplitude.

If we want to decrease the level given in Chapter VI.2 (default level) by 2dB for example we only have to send ***STEGN AC 65***. The following tables show the new levels measured on the telephone line after a 2dB theoric attenuation.

Table 32 : Example

Signal	Default Level (dBm)	Attenuated Signal with SETGN (dBm)
Bell 103 Originate	- 8.8	- 10.8
Bell 103 Answer	- 8.6	- 10.6
V.23 Originate	- 9.2	- 11.2
V.23 Answer	- 9.1	- 11.1
V.21 Originate	- 8.7	- 10.7
V.21 Answer	- 8.8	- 10.8
V.21 ch2	- 8.8	- 10.8
V.27 ter	- 8.9	- 10.8
V.29	- 8.8	- 10.8
V.17	- 9	- 11
V.33	- 9	- 11

Table 33 : Example

Signal	Default Level (dBm)	Attenuated Signal with SETGN (dBm)
DTMF0	- 9.32	- 11.32
DTMF1	- 9.31	- 11.31
DTMF2	- 9.33	- 11.33
DTMF3	- 9.37	- 11.37
DTMF4	- 9.3	- 11.3
DTMF5	- 9.32	- 11.32
DTMF6	- 9.36	- 11.36
DTMF7	- 9.29	- 11.29
DTMF8	- 9.32	- 11.32
DTMF9	- 9.35	- 11.35
DTMFA	- 9.4	- 11.4
DTMFB	- 9.39	- 11.39
DTMFC	- 9.39	- 11.39
DTMFD	- 9.39	- 11.39
DTMF*	- 9.29	- 11.29
DTMF#	- 9.35	- 11.35
2100Hz	- 9.38	- 11.38
2225Hz	- 9.46	- 11.46
1300Hz	- 9	- 11.0
1650Hz	- 9.13	- 11.13

VI.4 - Transmit Equalizers

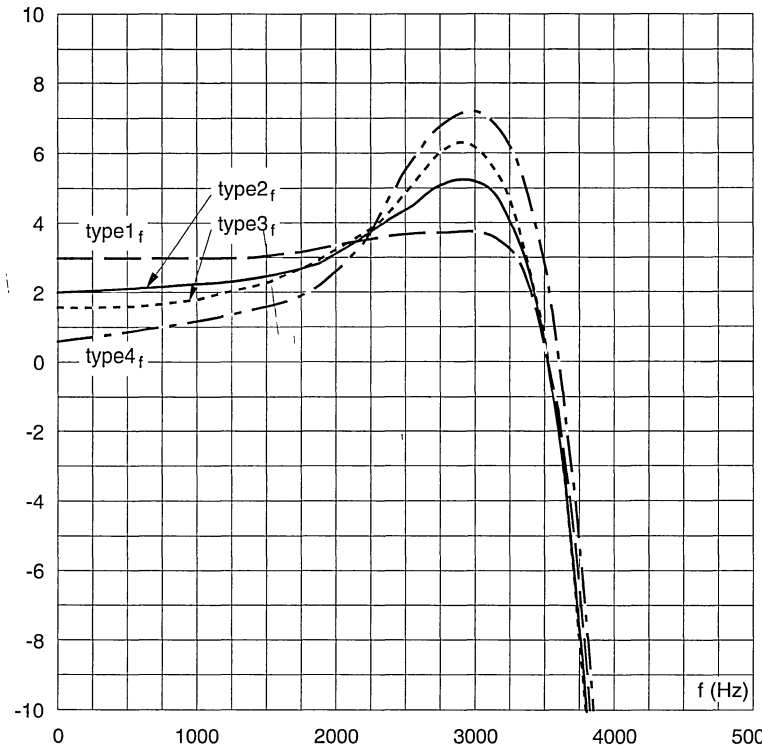
The following types of equalizers are built into the modem to improve the transmission performance when the line conditions are poor. They are also built to compensate the interpolation filter of the analog front end part of the ST75C52/520.

4 equalizers can be selected :

- type 0 built to compensate just the filter of the analog front end part,
- type 1 built to compensate the filter of the analog front end and the amplitude distorsion of the 0.4mm diameter non-loaded cables of 1.8km,
- type 2 built to compensate the filter of the analog front end and the amplitude distorsion of the 0.4mm diameter non-loaded cables of 3.6km,
- type 3 built to compensate the filter of the analog front end and the amplitude distorsion of the 0.4mm diameter non-loaded cables of 7.2km.

The characteristics of amplitude equalizers are ploted on the figure hereunder (see Figure 57).

Figure 57 : Amplitude Equalizer Characteristics



75C52-80 EPS

VII - CONTROL IN RECEIVE MODE

VII.1 - Analog Hybrid Implementation

Refer to the schematic showed in Chapter VI.1. As for the transmit hybrid the receive hybrid is designed to use the ST75C52/520's maximum performances (differential Input). The operational amplifier U2 is only used for reception purpose and powered between +12V and -12V. This analog interface allows to receive a signal up to 0dBm.

The receive gain is given by the formula Grec = 1 + (R1x2)/R2, with R1 = 15kΩ and R2 = 82kΩ.

Both RXA1 and RXA2 must be referenced to V_{CM}.

VII.2 - Carrier Detect Signal

The DSP uses the following internal variables for carrier detection :

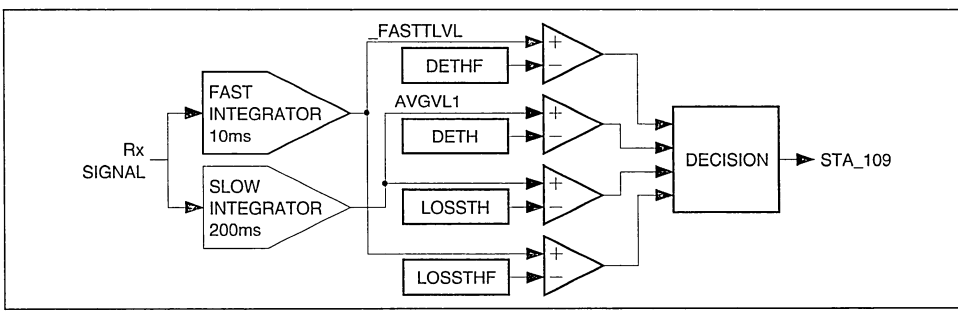
DETHF(R/W)	Fast detection threshold	at address $16C2
DETH (R/W)	Slow detection threshold	at address $16C1
LOSSTH (R/W)	Slow loss threshold	at address $16C4
LOSSTHF (R/W)	Fast loss threshold	at address $16C3

The carrier detect is displayed on status byte 0, bit 0 as well as on the ***CD*** pin of the ST75C52/520 serial interface and is active at the end of the synchronization sequence for V.17, V.29, V.27, V.21 ch 2 provided the detection threshold has been reached. For FSK modes, it is active provided the threshold has been reached. The carrier detect algorithms use, 2 signal level integrators a fast integrator for quick detection with a limited precision and a slow integrator for enhanced precision. There are four thresholds programmed with default values for each of the modes V.33, V.17, FSK, V.29, and V.27 which can be modified by the user after the conf command. Typical values for V.17 are shown below as an example and doubling the value read will increase the threshold by approximately 6dB :

(-40dBm)	$167	DETHF (fast detection threshold)
(-44dBm)	$140	DETH (slow detection threshold)
(-47dBm)	$D0	LOSSTH (slow loss threshold)
(-51dBm)	$A0	LOSSTHF (fast loss threshold)

note that it is mandatory to have :
DETHF > DETH > LOSSTH > LOSSTHF

Figure 58



AVGLVL1 (R) Carrier detect level.
This level is the ouput of the slow level integrator with a 200ms time constant. The formula for the rx lvl on the line for a V.17 receive signal, for example, is a function of x, the value of the variable at address AVGLVL1 :
RxLevel = 20 * log(x) - 93 in dBm

_FASTLVL (R) Fast carrier detect level.
This level is the output of the fast level integrator calculated with a 10ms time constant and obeying the same formula as above with, of course, more ripple for a given level due to the smaller time constant.

VII.3 - Received Signal Dynamic Range

The received signal dynamic range mainly depents of the hybrid. The ST75C52/520 with the above hybrid using the differential input can receive carrier up to 0dBm. Be careful that the hybrid is powered between +12V and -12V.

Carrier detection threshold is -44dBm, and carrier loss threshold is -47dBm.

DTMF detection is only possible for level higher than -35dBm.

Tone detector detection thresholds are programmable from -45dBm up to -10dBm.

All the results given in this chapter refer to the above hybrid (Chapter VI.1).

The table hereafter summarizes the test results for the carrier detection. You will find detection level, droptout level and hysteresis for fax modes. Tests were done on Automatic Modem Test Equipment AUTOTEST 1AE AEA.

Table 34

Modes	Detection (dBm)	Dropout (dBm)	Hysteresis (dB)
V.17 14400bps	44.06	46.38	2.32
V.17 1200bps	44.06	46.38	2.32
V.17 9600bps	44.06	46.38	2.32
V.17 7200bps	44.36	46.8	2.44
V.29 9600bps	44.5	46.22	1.72
V.29 7200bps	44.5	46.22	1.72
V.29 4800bps	43.62	46.7	3.08
V.27 4800bps	44.02	47	2.98
V.27 2400bps	44.2	47	2.8
V.21 Channel 2	44.2	46.2	2

The table hereafter summarizes the timing of carrier detection and the timing for loss of carrier detect. The time for carrier detection is about 3ms and the time for loss of signal carrier Detect cdt) is about 14ms.

Table 35

Modes	Timings for Loss (ms)	Timing for Detection (ms)
V.17 14400bps	13.1	2.3
V.17 1200bps	11.7	2.3
V.17 9600bps	12	2.3
V.17 7200bps	12.2	2.2
V.29 9600bps	13.3	2.5
V.29 7200bps	12.3	2.1
V.29 4800bps	12.7	2.5
V.27 4800bps	13.7	2.7
V.27 2400bps	13.3	3.6
Bell 103	19.5	5
V.21	19.1	5

VII.4 - PSTN/Leased Line Selection

The ST75C52/520 can be used both over PSTN network and over leased line (2 wire).

The choice is made with bit 5 (CONF_PSTN) of the first parameter of the CONF command.

CONF_PSTN = 0 will select PSTN network
CONF_PSTN =1 will select leased line.

The nominal carrier detect thresholds for such networks are :
- -33/-38dBm for leased line
- -43/-48dBm for PSTN.

VII.5 - Constellation

For all the high speed FAX modulations the user can observe the constellation with an oscilloscope using the EYEX and EYEY signals. This feature is always available (no validation required).

VIII - ELECTRICAL SCHEMATICS

VIII.1 - First Hybrid Example

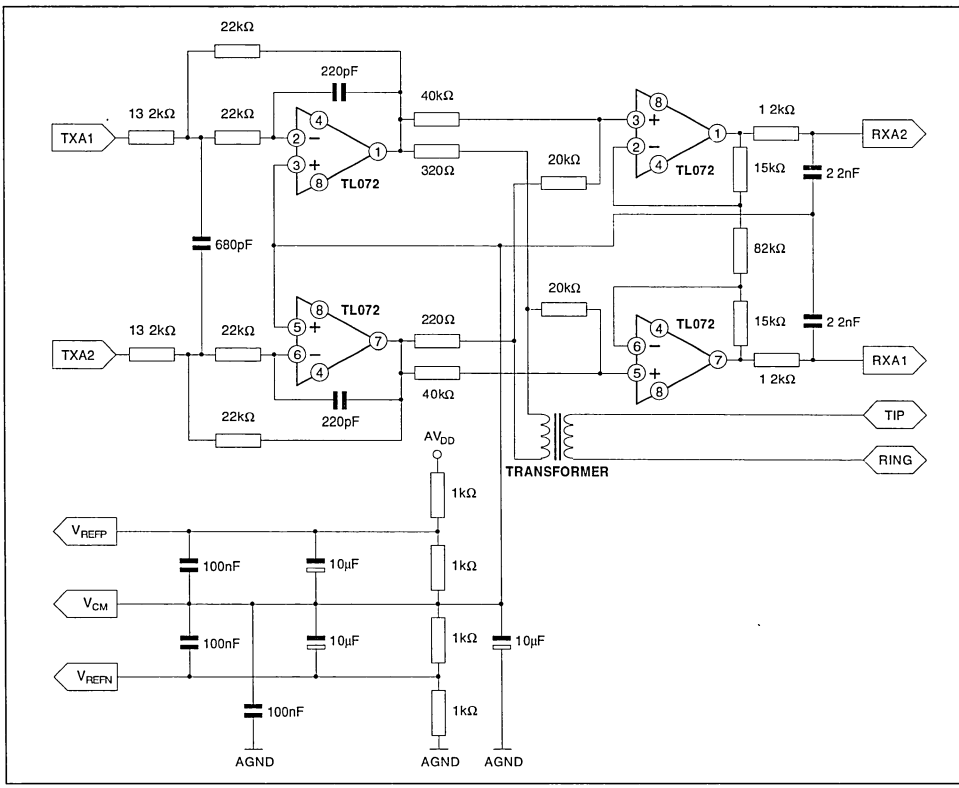
The example is detailed on the following schematic. It is the hybrid used on the application boards of SGS-THOMSON. All the tests were done with this hybrid. With such a solution (differential output and input) and with a double power for the operational amplifier the user can have the ST75C52/520's maximum performances.

The transmit gain is tuned to send carrier at - 9dBm (default value). If the user wants to be able to send carrier signal at 0dBm the transmit gain must be increased. We recommand the following procedure :

- Replace the two 13.2kΩ 1% with two 4.64kΩ 1%.
- Replace the two 220pF with two 47pF.
- use ***SETGN*** command to decrease the level around -9dBm.

If user wants to use +5V and -5V instead +12V and -12V we recommand to use Rail to Rail operational amplifier to avoid distortion.

Figure 59



VIII.2 - Second Hybrid Example

The following schematic is an example of a cheaper hybrid solution. The main difference is that the reception does not use the differential possibility of the ST75C52/520. The received signal is connected on RXA1 and RXA2 is tied to V_{CM}. The signal at RXA1 must not be higher than 2.5V. The receive gain must be tuned to detect carrier at -43dBm and we suggest to limit the maximum level at -9dBm.

Tuning :
- adjust the return loss,
- ajust the transmit gain,
- adjust the receive gain,
- adjust the duplexor.

Return loss : adjust R0 and C0 to meet the technical requirements in your country which imposes the reference impedance (600Ω or complex impedance), and the different parameters such DC voltage and DC current on the line.

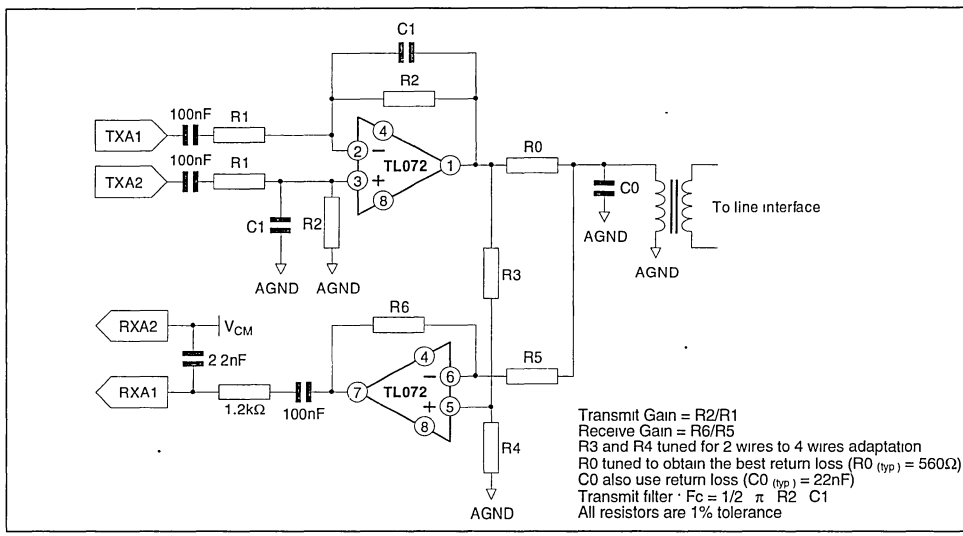
Transmit gain : we recommand the following procedure.
- Keep the ***SETGN*** default value (7FFF)
- adjust the transmit gain (R2 and R1) and the transmit filter (C1) to have 0dBm and Fc at 19.6kHz.
- adjust ***SETGN*** to obtain -9dBm (default value for carrier) and -4.5dBm (default value for the DTMF). ***STEGN*** may be different for carrier and DTMF.

Receive gain : adjust R6 and R5 to detect carrier around -44dBm.

Duplexor : adjust R3 and R4 to remove unwanted carrier when in ful duplex mode.

Hybrid implementation for differential output and single input (operational amplifiers use +12V and -12V) (see Figure 60).

Figure 60



IX - PCB DESIGN GUIDE

IX.1 - DAA

The DAA has both digital and analog portions in which we need to have sufficient dielectrique isolation from the telephone line and to suppress EMI.

Different technical requirements (FCC in USA, EN41003 in Europa...) influence the PCB design. In all cases the PCB layout must keep the insulation given by the components (i.e the distance between input and output for an optocoupler usally used for RING detection, between primary side and secondary side of the line transformer...). We suggest to have a visible dielectric barrier of 4mm (minimum value).

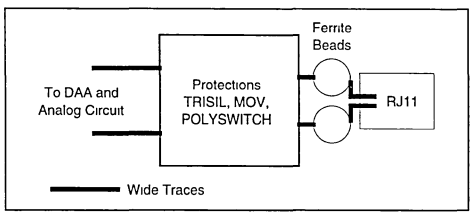
The layout may have wide traces in all the DAA part to avoid problems due to surge tests and to carrie eventualy high DC current.

We suggest to use polyswitch (fuse with auto rearmament) instead of narrow traces to implement fusible mechanism. The polyswitch must be associated with a TRISIL
(such TPA 220 of SGS-THOMSON).

Both transmit carrier (analog signal at - 9dBm) and receive signal (that can be as low as -48dBm) carry all the information through the analog circuit and the DAA. These two parts must be located as close as possible to the RJ-11 telephone jack.

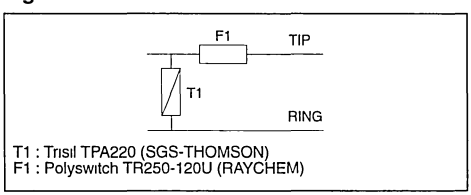
All the protections (surge limiter, MOV or TRISIL) and ferrite beads must be installed just near the RJ-11 telephone jack.

Figure 61



We suggest to use the following protection which meet EN41003 technical requirements :

Figure 62



IX.2 - Digital Circuit

The Hook-control, Pulse-control, Ring-detection, DC current line detection (optional), ST75C52/520 Dual Port Ram Interface, microcontroller, memory and DTE interface are installed in the digital part of the PCB.

The equipment will use frequencies such as 29.412MHz (for the ST75C52/520) and other high frequencies for the microcontroller and different peripherals. For such reasons the digital power (V_{DD}) and the digital ground (DGND) must be separated from the analog power (AV_{DD}) and the analog ground (AGND). We suggest to have a four layers PCB with one layer for the V_{DD} and one layer for the DGND.

It is recommanded to install a bead just at the output of each voltage regulator.

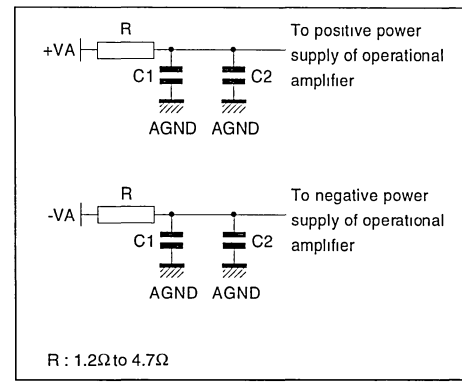
All the components must have a 100nF capacitor between V_{DD} and DGND. Some component (such microcontroller, MODEM/FAX...) required other capacitors usally higher than 1µF. All the capacitors must be connected with the shortest distance from the powers pins.

IX.3 - Analog Circuit

The hybrid, the analog interface of the ST75C52/520 and the transformer line interface only carry analog signals. The power (AV_{DD}) of the ST75C52/520 must be connected to the V_{DD} Pin of the ST75C52/520. The analog ground (AGND) must be connected to the digital point with a very low impedance, at one point and as close as possible to the ST75C52/520.

The Hybrid interface uses one positive power supply and one negative power supply. Simple filters (resistors and capacitors) can be used for each power signal.

Figure 63

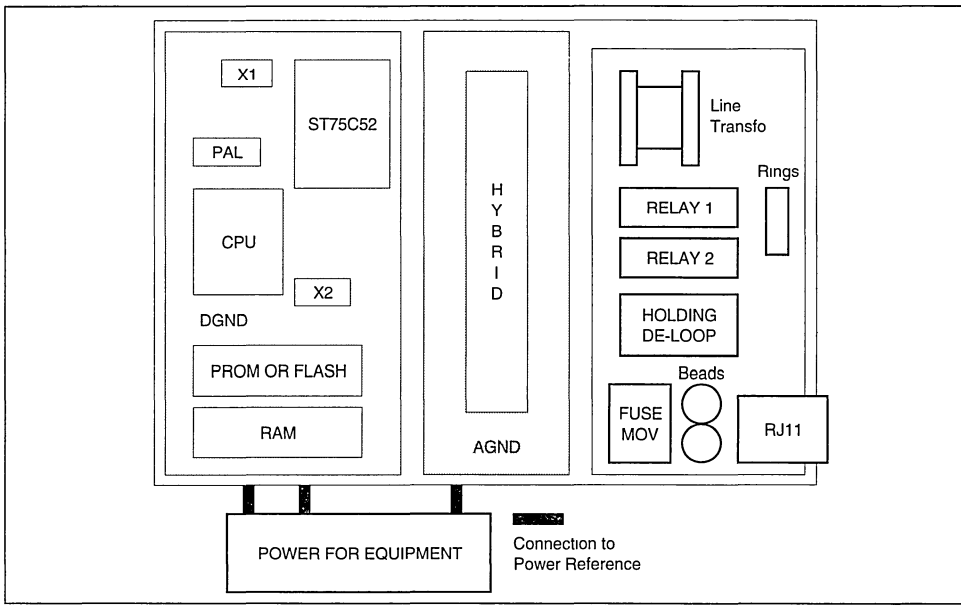


We recommand the following points :

- the V_{CM} reference must be generated as close as possible to the ST75C52/520,
- the two 2.2nF capacitors connected to the RXA1 and RXA2 Pins must be as close as possible to them,
- the two 100nF capacitors connected to the V_{REFP} and V_{REFN} Pins must be as close as possible to them.
- the ground for loudspeaker circuit must be separated from all the other analog modem circuit. In fact due to the audio current during the handshake the receive signal could be affected.
- use wide traces for all the power signals.

The analog ground could be a part of the ground layer, but the connection between the two references must be done only at one point. When possible the analog ground will be connected directly to the reference of the power equipment without going through the digital ground layer as shown on the Figure 64.

Figure 64



X - ST75C52/520 VARIABLES DESCRIPTION

Introduction

This chapter describes the most interesting variables that can be read or modified by the user. In order to read a variable a ***MR*** command (or ***CR*** for complex read) must be issued, and the answer is available in the Dual Ram, in the ***COMREP*** and ***COMREP+1*** locations. In order to overwrite a variable a ***MW*** command must be issued.

The address, characteristic (R = read, W = write, R/W = read or write), and function of key data pump variables is listed below by basic modem functional block. All numbers starting with a $ are Hexadecimal numbers, % are binary numbers.

Some of the variables and the explanations were some times introduced in above chapters.

Timing Recovery

FRQOFFT (R) Receive clock frequency offset.

PSITHRSH (R) 0.7 Deg timing phase adjustement threshold for timing signal dpll. The local-to-remote modem timing offset for all modes except V.21 channel 2 can be calculated using the following formula :

$$TOffset = \frac{FRQOFFT}{PSITHRSH} \cdot \frac{0.7}{360}$$

FRQ (R) V.21 ch. 2 receive clock frequency offset. V.21 channel 2 has a wider range of timing offset tracking permitting ±0.3% and it can be calculated using the following formula :

$$TOffset = \frac{FRQ}{32767} \cdot \frac{1.4}{360}$$

PLLcount (R/W) a counter which is decremented every baud in the timing recovery routine and, when > 0 selects wide bandwidth timing recovery DPLL. When = 0 selects narrow bandwidth timing recovery DPLL. For short train applications, it is useful to write PLLcount = 4800 (around 2s) after sending the SYNC 1 command to have a good success rate for many successive short train sequences, especially when there is a large timing offset.

Carrier Recovery

FRQOFF (R) Receive carrier frequency offset :

Offset = FRQOFF x 0.0366

in Hz. Typically, FRQOFF = $1B(27) for 1Hz.

Equalizer, AGC

_RX_STA (R/W) Equalizer and AGC can be frozen independently or simultaneously.

- Bit 0 : Freeze Equalizer (the Equalizer is frosen if this bit is 1).
- Bit 2 : Freeze AGC (the AGC is frosen if this bit is 1).

_RX_STA must be modified in data mode and the other bits must be unchanged. Read the value and change only the corresponding bits in the _RX_STA word.

_AGCSCA (R) Automatic gain control level for receive signal varies from $80 (0dBm) to $7FFF (-48dBm) according to the following table :

Table 36

Value	RXLVL (dBm)
$0080	0
$0100	- 6
$0200	- 12
$0400	- 18
$0800	- 24
$1000	- 30
$2000	- 36
$4000	- 42
$7FFF	- 48

The level calculated above must be corrected by 0 or -12dB to indicate the real receive analog level on the line. (See _GAINSTA below). The exact formula is :

RxLevel = (-20 x log(value)) + 46 - 6 x (_GAINSTA)

_GAINSTA (R) This variable tells whether the 12dB analog gain between input RXA and the analog to digital converter output has been activated. This gain enables a receive dynamic range between 0 and -50dBm. In the case that it has been activated, it has the value 2, otherwise 0.

_GAINCTL (R/W) This variable contains the following information :

- bit 0: FRZGAIN,
- bit 1: FORCE0,
- bit 2: FORCE12,
- all other bits are 0.

The user has the possibility of forcing 12dB, 0dB, or freezing the analog input gain. If desired, this word is programmed before sending the CONF

command and is effective after its execution. The variable _GAINCTL is initialized to 0 after a hardware reset or issuing of the init command, and if not programmed by the user, will allow the analog gain to be automatically enabled or disabled via the DSP software according to the actual input level. A built-in hysteresis avoids glitches on the receive digital samples. The input gain is switched to 0dB if the input analog instantaneous level exceeds -12dBm and to 12dB if the instantanenous level never exceeds -30dBm for 8ms.The FRZGAIN bit in _GAINCTL will be automatically set following the detection of phase reversals in the synchronization sequence for V.17, V.29, V.27 reception modes. This insures reliable demodulation for the receiver and, during a particular connection, the receive attenuation will not appreciably change.

RDQUA (R) Equalizer error energy gives an idea of signal to noise ratio seen by the receiver. The square of the equalizer error is updated once per baud (2400Hz for V.17, V.33, V.29, 1600Hz for V.27 4800bps, 1200Hz for V.27 2400bps) with a low pass 1st order IIR digital filter with a pole radius of 0.96875. This implies a time constant of around 80ms.

RDQUA has the following typical values :

Table 37

Value	RX SNR
$00C0	30dB
$0180	27dB
$0300	24dB
$0600	21dB
$0C00	18dB
$1800	15dB
$3000	12dB

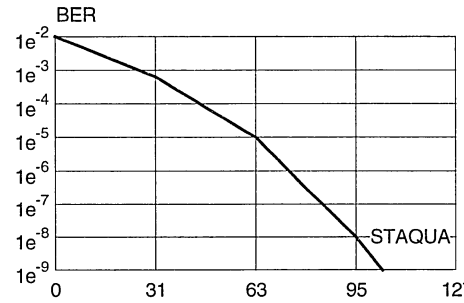
_RDQUA (R) A 16-bit number ranging between 0 and 127 indicating the receive quality (also available in 8-bit status word byte 2, STAQUA in dual port ram). The following formula is implemented in DSP software :

$$\_RDQUA = 127 - SCAQUA \times RDQUA$$

and is limited between 0 and 127. A value of 127 indicates a very good receive signal quality while 0 indicates a very poor signal quality. The coefficient SCAQUA is mode dependent and was chosen to give a value for _RDQUA of 63 when the receive SNR is such that the expected bit error rate is 10^{-5}, that is, 1 error for every 100000 bits received.

Refer to the following charts for expected values of _RDQUA, BER on flat telephone line.

Figure 65



SCAQUA (R/W) The coefficient for calculating _RDQUA above is automatically programmed according to the mode specified in the conf command and it is possible to overwrite its value at the end of the synchronization sequence if the user desires a different value for the quality indication. Generally, reducing the value read by 1/2 will imply that an _RDQUA value of 31 will correspond with a 10-5 BER and doubling the value will imply that an _RDQUA value of 127 will correspond with a 10-5 BER in the above tables.

_SUCTH (R/W) A threshold value for _RDQUA for determining the programming of pnsucs bit in _SHSK word described below. The default value is programmed to 64 at the execution of a conf command can be modified thereafter (espacially for short train applications).

_RDCPT (R) Output of Demodulator. Complex number, can be use to display the received eye pattern on a console or print-out. The user must perform a CR (complex read) command to insure reading of the real and imaginary parts of the signal during the same baud.

EQFRK0E (R/W) 32 Complex even equalizer coefficients.
EQFRK1E (R/W) 32 Complex odd equalizer coefficients.

Handshake, Synchronization

_SHSK (R) Contains information about the progress of the handshake or synchronization in all fax modes. This variable is also avalilable in optional status word 2 STAOPT2 in the dual port ram. The handshake bit positions are programmed on the 8 lsb of _SHSK and are defined below :

While Transmiting :

P1s = %00000001 generate echo protection tone
P2s = %00000010 generate phase reversals
PNs = %00000100 generate training sequence
PRs = %00001000 generate rate sequence
SCR1s = %00010000 generate scrambled one's

While Receiving :

P2s = %00000010 detect phase reversals
PNDETs = %00100000 detect training sequence (latched)
PNs = %00000100 detect training sequence
PRDETs = %01000000 detect rate sequence (latched)
PNSUCs = %10000000 detect scrambled one's (latched)
SCR1s = %00010000 detect scrambled one's note that PRs and PRDET are only valid in V.17 and V.33 Modes.

_TSPEED (R) Target speed initialized by CONF command.

%0000000000000011 = 2400bps
%0000000000000100 = 4800bps
%0000000000000101 = 7200bps
%0000000000000110 = 9600bps
%0000000000000111 = 1200bps
%0000000000001000 = 14400bps

_SPEED (R) Negotiated speed after synchronization May differ from _TSPEED for V.33 mode and has the same format as _TSPEED.

Carrier Detect

DETHF (R/W) Fast detection threshold
DETH (R/W) Slow detection threshold
LOSSTH (R/W) Slow loss threshold
LOSSTHF (R/W) Fast loss threshold

The carrier detect is displayed on status byte 0, bit 0 as well as on the **CD** Pin of the ST75C52/520 V.24 interface and is active at the end of the synchronization sequence for V.17, V.29, V.27, V.21 ch2 provided the detection threshold has been reached. For fsk modes, it is active provided the threshold has been reached. The carrier detect algorithms, 2 signal level integrators a fast integrator for quick detection with a limited precision and a slow integrator for enhanced precision. There are four thresholds programmed with default values for each of the modes V.33, V.17, FSK, V.29 and V.27 which can be modified by the user after the conf command. Typical values for V.17 are shown below as an example and doubling the value read will increase the threshold by approximately 6dB :

(-40dBm) $167 DETHF (fast detection threshold)
(-44dBm) $140 DETH (slow detectiion threshold)
(-47dBm) $D0 LOSSTH (slow loss threshold)
(-51dBm) $A0 LOSSTHF (fast loss threshold)

note that it is mandatory to have :
DETHF > DETH > LOSSTH > LOSSTHF

AVGLVL1 (R) Carrier detect level. This level is the ouput of the slow level integrator with a 200ms time constant and is automatically corrected for the possible 12dB analog gain explained above. The formula for the rx lvl on the line for a V.17 receive signal, for example, is a function of x, the value of the variable at address AVGLVL1 :

RXLEVEL = 20 x log(x) - 93 in dBm.

_FASTLVL (R) Fast carrier detect level. This level is the output of the fast level integrator calculated with a 10ms time constant and obeying the same formula as above with, of course, more ripple for a given level due to the smaller time constant.

_LVLSAV (R/W) Storage of value of (_FASTLVL/2) described above and memorized during the detection of P2 portion of sync sequence by the receiver. This is the threshold for the fast carrier detect comparator. Memorizing the level on a valid signal avoids false detection or non-detection due to noise thus providing a very accurate indication of presence of a carrier. It updates bit 7 of status byte 0 in the dual port ram. Its value can eventually be changed by the user by first reading and then writing into this memory location after p2s bit is activated in the optional status word 2.

V21FDET (R) Detection of presence of V.21 flag also available in status word 1 bit 6 (STA_FLAG). The detector signals presence of 2 or more consecutive sequences of $7E (%01111110) modulated according to the V.21 ch. 2 FSK specification (1 = 1850Hz, 0 = 1650Hz) at 300bps. The detector signals the loss of V.21 flag at the end of the first following erroneous bit and is automatically re-armed. The detector is always active during tone, dtmf, audio or V.21 channel 2 conf modes. It is active in V.17, V.33, V.29, V.27 Conf modes after the SYNC 1 command is issued and before the data mode (carrier detect active).

Tone Detector Programming

LEVOUT (R/W) 16 Programmable static levels.

BIQCOEF (R/W) 16*2*6 Biquad coeficients.

Coefficient order for each of 16 4th order cells :
C0, C1, C2, C3, C4, C5, C6, C7, C8, C9, CA, CB

Where each 4th order cell has the following transfer function :

$$\frac{OUT}{IN} = C_0 \cdot \frac{C_5 + 2 \cdot C_3 \cdot z^{-1} + 2 \cdot C_4 \cdot z^{-2}}{1 - 2 \cdot C_1 \cdot z^{-1} - 2 \cdot C_2 \cdot z^{-2}} \quad C_6 \cdot \frac{C_B + 2 \cdot C_9 \cdot z^{-1} + 2 \cdot C_A \cdot z^{-2}}{1 - 2 \cdot C_7 \cdot z^{-1} - 2 \cdot C_8 \cdot z^{-2}}$$

When programming the coefficients, care must be taken to avoid overflow of internal nodes. Effectively, the structure of each 2nd order section is such that the recursive portion is executed before the non-recursive. Therefore, C0 and C6 must be chosen to insure that the maximum of :

$$C_0 \cdot \frac{1}{1 - 2 \cdot C_1 \cdot z^{-1} - 2 \cdot C_2 \cdot z^{-2}} \quad \text{or}$$

$$C_6 \cdot \frac{1}{1 - 2 \cdot C_7 \cdot z^{-1} - 2 \cdot C_8 \cdot z^{-2}}$$

never exceeds 1 ($7fff) or -1 ($8000)

POWCOEF (R/W) 16 Power coeficients p1, Power estimator using absolute value of the input signal :

$$\frac{OUT}{IN} = P1 \cdot \frac{z^{-1}}{1 - (1 - P1) \cdot z^{-1}}$$

BPWIRE (R/W) 16 Biquad and pwr estimator input wiring addresses
FORMAT = [4TH ORDER BIQ(MSB), PWR(LSB)]

CPWIRE (R/W) 16 Comparator input wiring addresses
FORMAT = [COMPARATOR+(MSB), COMPARATOR-(LSB)]

The wiring addresses furnished in bpwire, cpwire are from the following possible sources :

GND	$00
Rx signal	$01
Rx signal*2	$02
Rx signal*4	$03
4th order biquad output	$10 to $1F
Power output	$20 to $2F
Static levels	$30 to $3F

Notes : 1. A value of $276 on RX signal corresponds to a real signal level on the line of -25dBm. For example, suppose one wants to detect a certain RXLVL on the line via RX SIGNAL assuming a gain of 1.0 in the biquadratic filter. The value of Levout, the comparison threshold, can be calculated : Levout = 10[(RXVL+81)/20]

2. The 0 or 12dB analog gain is automatically compensated for at the power outputs and need not be accounted for in the above formula. Some modifications to the calculated value may be needed for low detection levels near -50dBm, or the RX SIGNAL*2 input may be used.

_NTDCELL (R/W) Number of tone detector cells active (0-15). The default values for _NTDCELL are according with the following Phases : see Figure 66 and Table 38.

The user can modify _NTDCELL on-the-fly but must be careful to avoid real time kernel errors (ERR_RTK) in the SYSERR status byte. The execution time of each cell is roughly 200 machine cycles. For example, if the HDLC is not used, 400 additional machine cycles could be available for additional cells.

_TONEDET (R) Outputs of tone detectors. The low byte of _TONEDET contains the outputs of tone detectors cells 0 to 7. The low byte of _TONEDET+1 contains outputs of cells 8 to 15. When the corresponding bit is "1" the signal at the positive input of the comparator is higher that at the negative input. Only _NTDCELL bits are valid at any one time and the others are 0.

_RING (R) Output of the RING Detector.This word is identiqual to the STAOP2 byte when in Tone mode (neither DTMF receiver neither Modem mode). The content of that word is the duration of the RING Period.

The formula to compute the RING Frequency - in Hz) is :

$$\text{RING\_Frequency} = \frac{1}{\text{RING} \cdot 2400}$$

This value is updated at each falling edge of the RING Signal. Refer to the following diagram for the phase relation between the STA_RING and the RING Signal (see Figure 67).

General Purpose

_TXGAIN (R/W) Transmit gain. Any signal to transmit is multyplied by this number. This is the value modified by **SETGN** command.

_FSKSYNC (R/W) $FFFF, for V.21 ch2 and 0 for all other modes. The user must use the memory write command to write 0 to this variable when passing from V.21 ch2 to FAX modes just before sending the corresponding **CONF** command.

Figure 66

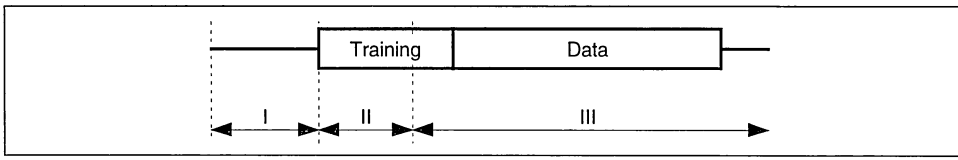
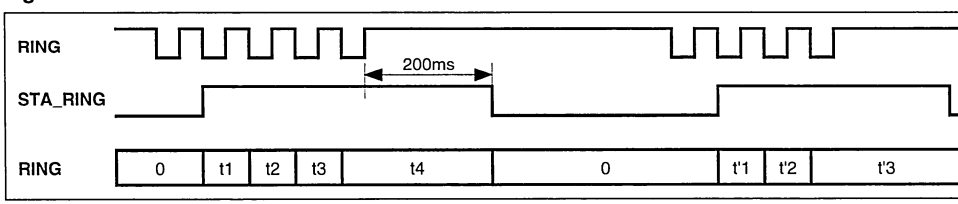


Table 38

Mode/Phase	Config.	Phase I	Phase II	Phase III
Tone, DTM (1), Voice	16 (2)	-	-	-
FSK Full Duplex	-	4	4	4
V.21 Ch 2 Tx	-	16 (2)	8 (2)	8 (2)
V.21 Ch 2 Rx	-	4 (2)	4 (2)	4
V.17/V.33/V.29/V.27 Tx	-	8	8	8
V.17/V.33/V.29/V.27 Rx	-	8 (2)	2 (2)	2

Notes : 1. The DTMF Receiver uses 12 of the 16 cells.
2. The V.21 Flag detector is active.

Figure 67



Tone Generator

_TGNFLG (R/W) Tone generator flag. Each of the four low bits of this variable define if the corresponding tone generator is enabled. This is the value modified by a **TGEN** and **TONE** command.

_TGNBLK (R/W) For each of the four tone generators (i) contains :

_TGNBLK+(3*i) : Frequency of tone (freq*32767/4800).
_TGNBLK+1+(3*i) : Instantanous phase (0 to 65535).
_TGNBLK+2+(3*i) : Amplitude ($7FFF refers to maximum signal).

Address Equivalences for Version 1.0 and 1.1 (DSP software version)

Timing Recovery	
FRQOFFT	$15D9
PSITHRSH	$15E3
FRQ	$1777
PLLCOUNT	$15DF
Carrier Recovery	
FRQOFF	$15F1
Equalizer, AGC	
_RX_STA	$1015
_AGCSCA	$10CF
_GAINSTA	$17D3
_GAINCTL	$17D2
RDQUA	$11DD
_RDQUA	$1054
SCAQUA	$11DC
_SUCTH	$17DD
_RDCPT	$1044
EQFRKOE	$1438
EQFRK1E	$1478
Handshake, Synchronisation	
_SHSK	$10F1
_TSPEED	$10E5
_SPEED	$1012
Carrier Detect	
DETHF	$16C2
DETH	$16C1
LOSSTH	$16C4
LOSSTHF	$16C3
AVGLVL1	$16BF
_FASTLVL	$172B
_LVLSAV	$16DF
V21FDET	$17B8
Tone Detector Programming	
LEVOUT	$122A
BIQCOEF	$12BA
POWCOEF	$137A
BPWIRE	$129A
CPWIRE	$12AA
_NTDCELL	$1006
_TONEDET	$1007
_RING	$1554
General Purpose	
_TXGAIN	$1001
_FSKSYNC	$16E8
Tone Generator	
_TGNFLG	$1002
_TG0PHC	$1003
_TGNBLK	$11EC

XI - PERFORMANCES

The curves hereafter define performances under various line conditions. All tests were run half duplex with a ST75C52/520 REV 1.0 as reference modem. The tests are run under the following conditions.

US LINES (type of channel) :
- Flat line ; US lines 3002, C1,C2
- Rx level : -25dBm
- Tx level : - 9dBm
- No AGC

EUROPEAN LINES (type of channel) :
- 1040, 1020 and 1025
- Rx level : -25dBm
- Tx level : - 9dBm
- No AGC

JAPANESE LINES (type of channel) :
- JPN1, JPN2, JPN3, JPN4, JPN5, JPN6, JPN7
- Rx level : -25dBm
- Tx level : - 9dBm
- AGC V56 (rms)

Figures 68 to 71 show performances of fax modes on all lines above in V.17 14400 and in V.29 9600.

Figure 68 : V.17 14400bps BER versus SNR on European and US Lines

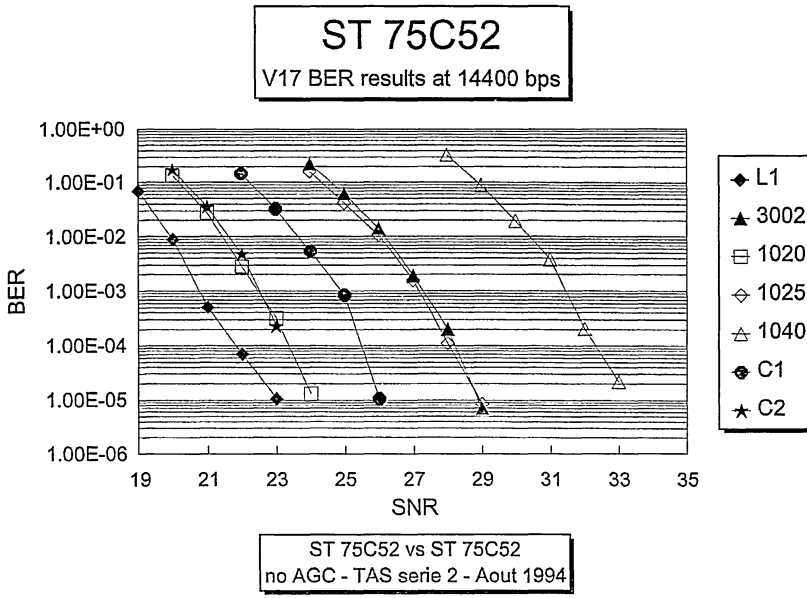
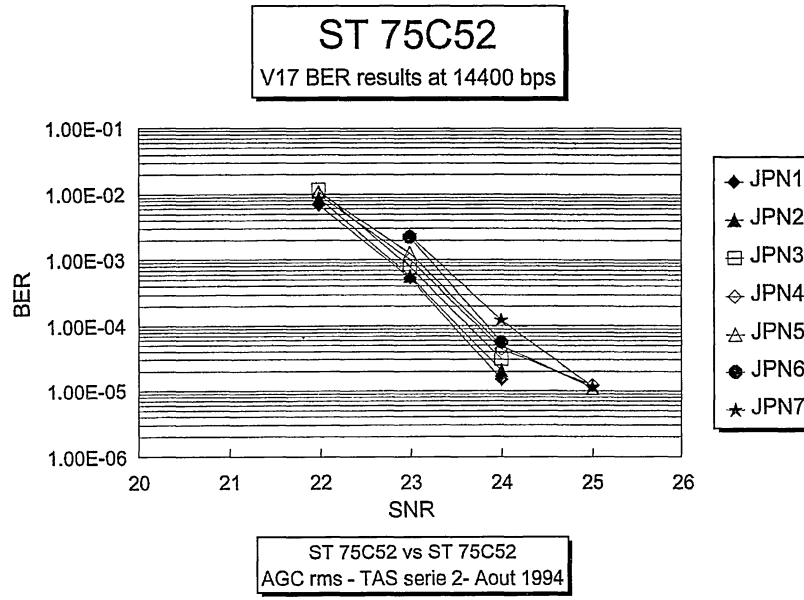
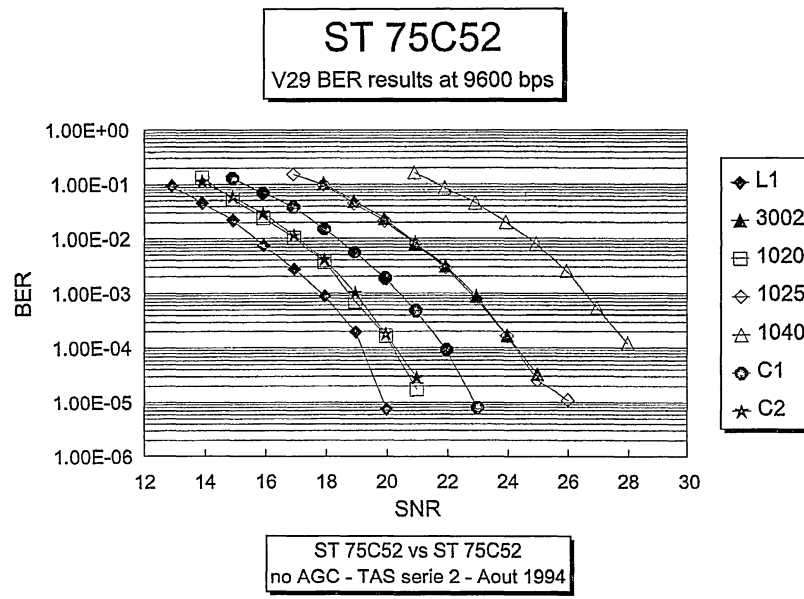


Figure 69 : V.17 14400bps BER versus SNR on Japanese Lines



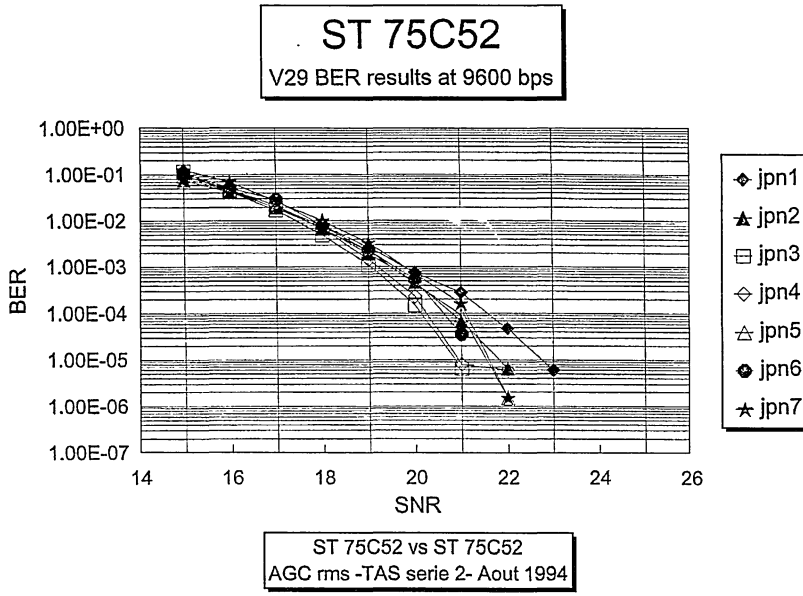
75C52-90.TIF

Figure 70 : V29 9600bps BER Results versus SNR on European and US Lines



75C52-91.TIF

Figure 71 : V29 9600bps BER Results versus SNR on Japanese Lines



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

V.17 FAX EQUIPMENT REPLACING THE R144EFX WITH THE ST75C52/520

By Laurent CLARAMOND and Joël HULOUX

SUMMARY

I - PRELIMINARY

The ST75C52/520 are a monolithic complete V.17 fax modem which is a superset of the R144EFX.

All functions found in the R144EFX can be found in the ST75C52/520, plus a few additional ones (class detection, 16 tone detectors, analog DAC for eyediagram, etc) as you will see in the chapter III table.

Although similar, the ST75C52/520 are not a plug-in replacement for R144EFX. You will need a few software and hardware adjustments, and with our help, it will cost you less than two man-months to do it.

A small effort, compared to your benefits. If you are thinking about integrating the ST75C52/520 with your prefered MCU and ASIC, call us immediately.

II - INTRODUCTION

II.1 - Overall

This application note describes the way to replace the ROCKWELL R144EFX by the SGS-THOMSON ST75C52/520 in a V.17 FAX equipment system.

This application note uses information detailed in the ST75C52/520 Data Sheet and User's Manual.

First, you will find comparison on the features of the ST75C52/520 and the R144EFX.

Second, will be listed the features required to implement FAX communications.

Third, will be presented to the user the different chapters in the ST75C52/520 and User's manual where information was detailed.

At the end of this application note is presented a software and hardware user's guide.

II.2 - A Few Modidifications in the Software

The user's fax software can be divided in two parts. The first part which is *the main* and *the biggest* is completly independent of the modem chip and is in charge of the following task :

- User interface (keyboard, screen, printer).
- ECM, T30, T4.
- Real time kernel.
- Control.
- ...

Layers 2 and 3 are in this part of the software.

This software can be reused in the final application without any modification and any perturbation when running in V.17 fax equipment including a ST75C52/520 modem chip.

The second part (which is *the smallest*) is dependent of the modem chip and includes the driver routines needed to provide a complete list of services to the layer 2 and 3. We mainly find the following drivers :

- Interrupts driver.
- Modem configuration.
- Data transfer (emission/reception).
- Tone detection/generation.

All the modifications will be easily done since :

- **the ST75C52/520's software interface is based on COMMAND SET using friendly mnemonics,**
- **interrupts use dedicated registers clearly identified,**
- **data transfer will use FIFO principle to save CPU time.**

II.3 - Hardware Evolutions

Performances and low cost are the *two key parameters* that have been followed by SGS-THOMSON.

The user can to remove the negative power supply (-5V) since the ST75C52/520 needs only one power supply of +5V. The differential analog output and input will increase performances at low level even on a two-layer printed circuit board. EMI problems can be reduced using a crystal of 29.4912MHz instead 38.00053MHz.

III - COMPARISON BETWEEN R144EFX AND ST75C52/520

Features	R144EFX	ST75C52/520
Package	QUIP 64 and PLCC68	PQFP64
Power	+5V ±5%, -5V ±5%	+5V ±5%
Supply Current at 25°C	97mA and 14mA (555mW)	100mA (500mW, 5mW low power mode)
Supply Current at 0°C	105mA and 16mA (605mW)	130mA (650mW)
Operating Range	0 to 70°C	0 to 70°C
Storage Temperature	-55 to 125°C	-45° to 125°C
Frequency	38.000530MHz	29.4912MHz
MCU Bus	65XX/80XX bus	MOTOROLA, INTEL bus
Interface with DSP	32 registers	60 registers
Interrupts	2 interrupts, one can be activated with a selectif mask from one of the 32 registers	One interrupt. Six sources with possible individual mask
Serial Interface	YES	YES
TX Buffer	1 byte	2 x 8 bytes
RX Buffer	1 byte	2 x 8 bytes
FAX Group 3	V.33 (14.4, 12kbps, 17000 and 1800Hz) idem V.17 V.17 (14.4, 12, 9.6, 7.2kbps, 1700 and 1800Hz) with short train V.29 (9.6, 7.2, 4.8kbps), no short train V.27ter (4.8, 2.4kbps) with short train	V.33 (14.4, 12kbps, 17000 and 1800Hz) idem V.17 V.17 (14.4, 12, 9.6, 7.2kbps, 1700 and 1800Hz) with short train V.29 (9.6, 7.2, 4.8kbps), with short train V.27ter (4.8, 2.4kbps) withshort train
Short Train	V.27ter, V.17	V.27ter, V.29, V.17
HDLC	YES	YES
TX Level	0 to -15dBm	0 to -48dBm
Dynamic Range	0 to -43dBm	0 to -43dBm
Turn On	-10 to -47dBm	-10 to -51dBm
Turn Off	-10 to -52dBm	-15 to -55dBm
Reception Timing	±0.01% frequency error	±0.01% frequency error
Tone Generator	2 from 0 to 4800Hz (step 0.15Hz), attenuation if f > 300Hz	4 from 0 to 3600Hz (step 1Hz)
DTMF Generation	Uses the 2 generators	Uses 2 of the 4 generators
Tone Detector	FR1, FR2 and FR3 from 400 to 3000Hz (FR1 and FR2 not available in high speed reception)	2 to 16 detectors programmable from 0 to 3600Hz : 2 if training FAX high speed reception, else 8, 4 if DTMF detection, 16 if tone reception or audio transmission and reception
DTMF Detection	Gives the DTMF digit. Twist (-8 to +4dB)	Gives the DTMF digit. Threshold -35dBm. T_{on} > 40ms, Twist (±8dB)
Flag Detection	Available in high speed reception except in V.27 ter short train and tone detection	Available in high speed reception, and tone detection mode
Voice Mode	7.2, 8 and 9.6kHz on 8 bits till 10 to 16 bits	7.2, 8 and 9.6kHz A law on 8 bits
Equalizers (Transmission and Reception)	4	4
Input/Output	NO	NO
V.23 (Full Duplex)	NO	YES
Eye Monitoring	Yes with serial link	Yes with analog output
Analog Interface	Mono	Differential
Max Output Level	±3 3V	±2.5V
Max Input Level	0dBm at RXA	±2.5V
Bell 103-V.21 Full Duplex	NO	YES
Class Detection	NO	YES

IV - FEATURES REQUIRED FOR FAX COMMUNICATIONS

In phase A (T.30 protocol) the modem chip must provide all features to establish or to answer a call. The user will use Tone Detectors for network tones detection (dialtone, busy tone, ring back tone), for answer tone detection (CED 2100Hz tone) and for flag detection.

In the calling unit, tone generators will be used to send DTMF digit, and the calling tone (CNG tone at 1100Hz).

When on-hook, the modem chip can help the host make incoming call detection.

In phase B, D and E (T.30 protocol) the modem chip must be able to send or receive :

- In V.21 ch2,
- HDLC frame over V.21 ch2 modulation,
- TCF frame in high speed mode (only in phase B).

In phase C the chip must be able to send or receive in high speed mode (V.27ter, V.29, V.17), and to detect V.21 flag (HDLC fanion) while in high speed mode reception.

The user must be able to adjust level in transmission (carrier, tone).

Complete HDLC (transmit and receive) function must also be available in high speed mode to allow ECM (Error Correcting Mode).

Some others features such as DTMF detection, voice mode may be required in the final application.

To use all the above features the user will initialize registers in the DSP and must read status. So, the chip must provide a friendly interface to a host microprocessor.

All the above features included in the R144EFX *can be easily used* with the ST75C52/520.

V - DATA SHEET AND USER'S MANUAL GUIDE LINE

Firstly the user has to read carefully the ST75C52/520 Data Sheet and User's Manual.

Secondly the user can use the following list which identifies the main chapters in the ST75C52/520 documentation. These chapters detail the features introduced in the previous chapter.

Digital Interface :
- Data Sheet Chapter III
- User's Manual Chapter II.2

User Interface :
- Data Sheet Chapter V

Analog Interface :
- Data Sheet Chapter XII
- User's Manual Chapter VIII

Tone Generator :
- Data Sheet Chapter IV.2.4
- Data Sheet Chapter VI :
  - DEFT, Tone, TGEN commands

Tone Detector :
- Data Sheet Chapter VIII
- User's Manual Chapter V

Interruptions :
- Data Sheet Chapter V.I.2

Configuration for G3 FAX :
- Data Sheet Chapter VI :
  - HSHK, SYNC, CONF, MODC commands
- Data Sheet Chapter VII
- User's Manual Chapter VII

HDLC Function :
- Data Sheet Chapter VI
  - FORM, SERIAL commands
- Data Sheet Chapter IX
- User's Manual Chapter IV

Control in Transmit Mode :
- User's Manual Chapter VI

Control in Receive Mode :
- User's Manual Chapter VII

PCB Guide Line :
- User's Manual Chapter IX

VI - SOFTWARE GUIDE LINE

As the main differences between the R144EFX and the ST75C52/520 are found in the software management, we suggest to the user the following steps to understand the ST75C52/520 software interface :

1.Study the User interface, the Command set, the Command Acknowledge.

2.Study the interruptions features.

3.Study the Parallel exchange in synchronous and in HDLC mode.

4.Study the status report.

5.Study the flow scharts for G3 FAX configuration.

VI.1 - User Interface

The host processor will be connected to the ST75C52/520 using a dual port ram with dedicated memory addresses for :
- Command and Parameters,
- Command Acknowledge,
- Data Tx buffer (transmission),
- Data Rx buffer (reception),
- Status information,
- Interrupt registers.

The address space within the host RAM mapping is a 128 byte block requiring 7 address lines instead 5 for the RFX144EFX.

The host processor will use commands (with or without parameters) to initialized the modem chip and to start/stop a specific task such as : send a tone, a carrier or detect a tone, a DTMF, a carrier, ...

Hereafter is described the syntax for each command :

Opcode : Hexadecimal Value

X	X	X	X	X	X	X	X

Parameters :

Field	Byte	Pos	Value	Definition
Name	X	a..b	XX*	Explanation of the parameter

Field : Name of the addressed bit field.

Byte : Index of the parameter byte (1 to 4).

Pos : Bit field position inside the parameter byte.

Value : Possible values for the bit (resp. bit field). A value followed by a star means a default value.

Each command will be acknowledge by the DSP.

The host processor must not send a new command without waiting for the acknowledge of the previous command.

Figure 1 is summarized the command acknowledge.

VI.2 - Interruptions

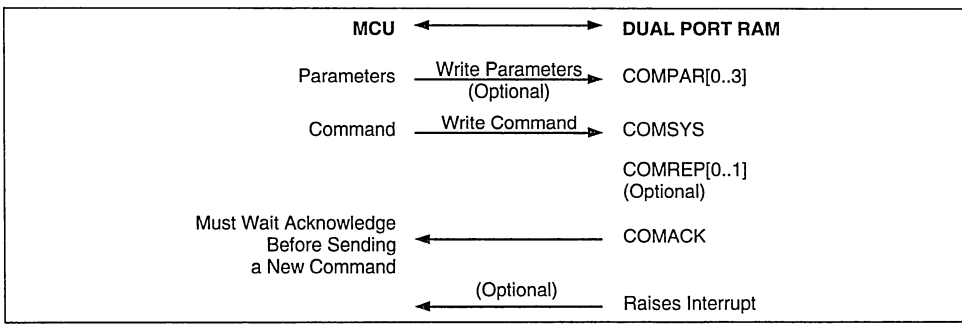
Six sources of interruptions can be used by the software handler routine :

Error	: IT0, if errors have occured
Tx Buffer	: IT2, the ST75C52/520 frees one of the 2 Tx buffers
Rx Buffer	: IT3, the ST75C52/520 has filled one of the 2 Rx buffers
Status byte	: IT4 to signify that the modem status has changed
Low power mode	: IT5 when the ST75C52/520 has been awakened
Command acknowledge	: IT6, the ST75C52/520 is ready for a new command

One 8 bit source register **ITSRCR** located at address **$50** in the dual port ram memory identifies the source :

D0 = 1	IT0 pending
D1	Not used
D2 = 1	IT2 pending
D3 = 1	IT3 pending
D4 = 1	IT4 pending
D5 = 1	IT5 pending
D6 = 1	IT6 pending

Figure 1



The interrupt source will be reset and acknowledge by writing a **$00** at one of the memory location **$40** to **$46** (Reset Interrupt registers **ITREST[0..6]**) in the dual port ram memory.

ITREST[0] at address $40 is dedicated to IT0.

ITREST[2] at address $42 is dedicated to IT2.

...

ITREST[6] at address $46 is dedicated to IT6.

Figure 2 is an example for IT2.

All sources of interrupt can be masked individually or globaly with the interrupt mask register **ITMASK** located at the address **$4F** in the dual port ram memory.

ITMASK register definition :

D7 = 0	All interrupts are masked (global mask)
D6 = D7 = 1	IT6 enable
D5 = D7 = 1	IT5 enable
D4 = D7 = 1	IT4 enable
D3 = D7 = 1	IT3 enable
D2 = D7 = 1	IT2 enable
D1	Not used must be equal to 0
D0 = D7 = 1	IT0 enable

Even if an interrupt is masked, the DSP will always set the corresponding bit in the source register (ITSRCR) to allow polling by the host processor.

Figure 3 illustrates for IT2 and IT3 the interruption principle, the user could easily transpose this principle to the other interrupts :

- IT2 and IT3 are set by the DSP,
- IT2 and IT3 are cleared and acknowledged by the host processor,
- ITSRCR is only read by the host processor,
- ITMASK is read or write by the host processor.

Figure 2

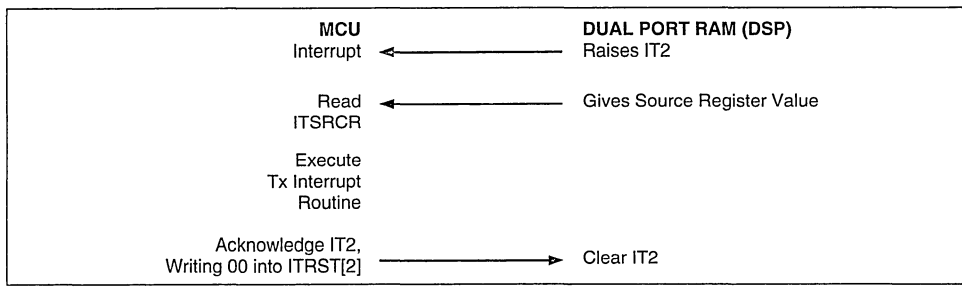
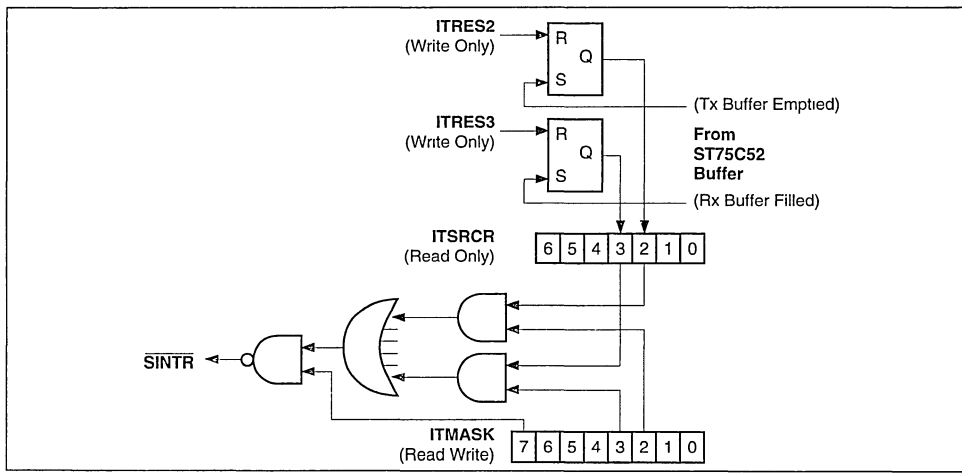


Figure 3



VI.3 - Parallel Exchange in Synchronous and in HDLC Mode

Data Tx Buffer :

The R144EFX uses only *one* TX buffer of *one* byte in parallel transmission. This architecture is very simple since the DSP has to write succesive bytes at the same address. The drawback is that the R144EFX will raise an interrupt *every* sent byte.

To save MCU (host processor) time the principle is quite different with a ST75C52/520.

Two Tx buffers will be used in parallel transfer, TX_BUFFER_0 called **DTTBF0** and TX_BUFFER_1 called **DTTBF1**. Each Tx buffer contains 8 bytes. The host processor can write one to eight bytes in the same buffer.

The Tx interrupt (IT2) will only be raised when the complet TX buffer will be empty (e.g for TX buffers filled with 8 bytes the IT2 will be activated every 8 bytes). As this principle save MCU time between two interrupts, the host processor could be more efficiency used for other main tasks such as Error Correcting Mode (ECM), ...

One status byte **DTTBS0** is dedicated to DTTBF0 and another **DTTBS1** is associated with DTTBF1.

Parallel transmission must be initialized with **SERIAL**, **FORM** and **XMIT** commands. In parallel transmission the two buffers *must* be used, *always* starting with buffer 0. The host processor must send data alternatively into DTTBF0, DTTBF1, DTTBF0, DTTBF1, DTTBF0, ...

The host processor writes data into a Tx buffer then writes the number of bytes into the dedicated status. The DSP reads the Tx buffer and clears the dedicated status, then raises IT2.

Figure 4 is illustrated the exchange in transmit parallel mode (initialization with the FORM, SERIAL and XMIT was already done).

Complet and detailed information is given in chapter IV of the ST75C52/520 User's Manual.

Data Rx Buffers :

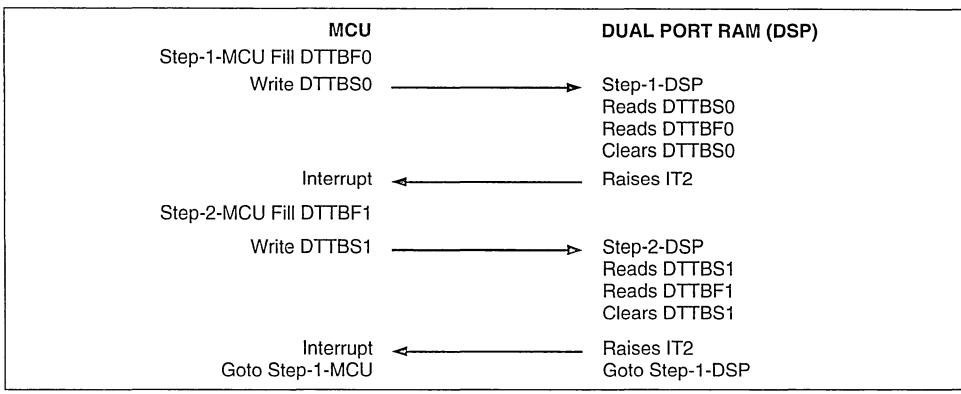
The R144EFX uses only *one* RX buffer of *one* byte in parallel reception. This architecture is very simple since the DSP has to read succesive bytes at the same address. The drawback is that the R144EFX will raise an interrupt *every* received byte.

To save MCU (host processor) time the principle is quite different with a ST75C52/520.

Two RX buffers will be used in parallel transfer, RX_BUFFER_0 called **DTRBF0** and RX_BUFFER_1 called **DTRBF1**. Each Rx buffer contains 8 bytes. The host processor will generaly read eight bytes in the same buffer except if the modem chip detects a loss of carrier.

One status byte **DTRBS0** is dedicated to DTRBF0, and another **DTRBS1** is dedicated to DTRBF1.

Figure 4 : Data Tx Buffer Flow Chart



The Rx interrupt (IT3) will only be raised when the complet RX buffer will be full (IT3 will be activated every 8 bytes). As this principle saves MCU time between two interrupts, the host processor could be more efficiency used for other main tasks such as ECM, ...

Parallel reception must be initialized with SERIAL and FORM commands.

In parallel reception the two buffers must always be used, starting with buffer 0. The DSP will alternatively fill DTRBF0, DTRBF1, DTRBF0, DTRBF1, ...

The DSP will fill one Rx buffer, then fill the dedicated status register and then raises IT3.

Each time an Rx buffer is filled the host processor must read it and then clear the dedicated status register.

Figure 5 is illustrated the exchange in receive parallel mode (initialization with the FORM, SERIAL already done).

Complet and detailed information is given in chapter IV of the ST75C52/520 User's manual.

VI.4 - Status Report

The host processor needs some status information writen by the ST75C52/520 to folllow tone detection result, synchronisation in high speed mode, DTMF detection, ...

For that purpose the ST75C52/520 provides following status :

ERROR STATUS (address $08) :

Provides information about error, can generate an interrupt **IT0**.

STATUS[0], STATUS[1] (addresses $09, $0A) :

Contain all the Modem signals, can generate an interrupt **IT4**.

STAQUA (address $0B) :

Contains the quality of the received signal.

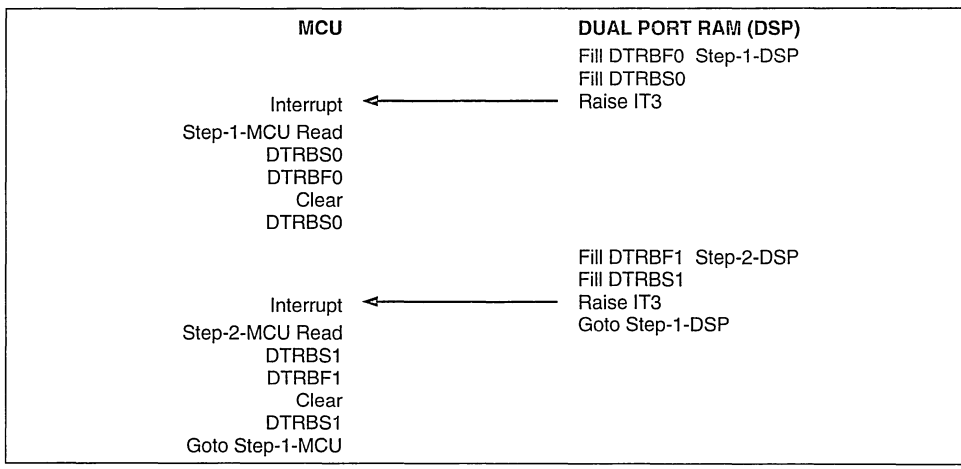
STAOP[0], STAOP[1], STAOP[2] (addresses $0C, $0D, $0E) :

Optional status that contain additional information regarding the ST75C52/520 operating mode. This default information can be changed to monitor any internal variables.

VI.5 - G3 Fax Equipment

All the information to set up the ST75C52/520 in phase A,B,C,D and E (T.30 protocol) are described in chapter III of the ST75C52/520 User's Manual. The user will find the COMMAND, STATUS information required. A lot of flow charts detail the procedure to initialize low speed (V.21 ch2) and high speed (V.27ter, V.29 , V.17) transmission and reception.

Figure 5 : Data Rx Buffer Flow Chart



VII - FLAG DETECTION

This chapter describes the way to use the flag_detection provided by the ST75C52/520 status report which will be used by a Host micro-controller.

VII.1 - V.21 Chanel 2 Flag 7E Detection

The ST75C52/520 provides in the **STATUS1** (address $0A in the host interface) the **STA_FLAG** bit. **STATUS1** is an 8 bit register that can be read (only) by the host. Bit position 7 corresponds to the MSB and bit position 0 corresponds of the LSB.

In this register bit 6 (position 6) is called **STA_FLAG** (valid only in FAX modem and tone mode). **STA_FLAG** equal to 1 means that a V.21 ch2 flag is detected.

Three flags are necessary to validate V.21 flag. So minimum timing for V.21 flag detection is :

3.3ms x 8 x 3 = 79.2ms.

At this optimum timing you have to add the response time for the filters and the time for synchronisation of state machine at the beginning of the flag. The overall detection of V.21 ch2 flag is between **92** and **98ms**.

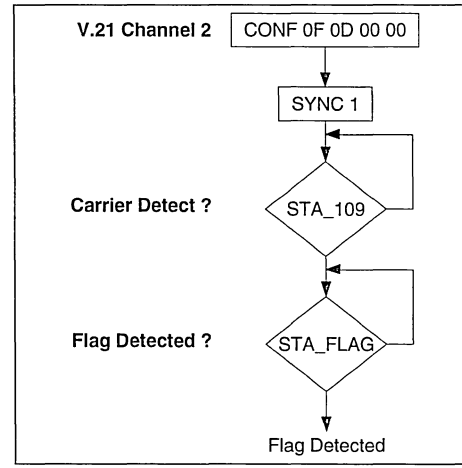
The overall time for loss of V.21 ch2 flag is between **17** and **25ms**.

VII.2 - Flag Detection in V.21 Channel 2 Mode

If the ST75C52/520 is set to receive in V.21 channel 2 mode, the V.21 flag detector is always available.

The following flow chart shows how the host must used the ST75C52/520 to detect V.21 ch2 flag while receiving in low speed mode (See Figure 6).

Figure 6



VII.3 - Flag Detection in High Speed Mode

VII.3.1 - Flag Detection at the Beginning of C Phase or TCF Reception

In such a case the ST75C52/520 is setting up to receive in V.27, V.29 or V.17. When the host starts the synchronisation of the reception sending the **SYNC 1** command to the ST75C52/520, the internal DSP executes two tasks in which the V.21 ch2 flag detection is activated :

- looking for V.21 ch2 signal,
- looking for training in high speed mode.

The V.21 ch2 flag detection is not available when the ST75C52/520 is in data mode (the training is completed, the carrier detect signal and the **STA_109** are true indicating a received high speed modulation).

Figure 7 shows when the flag detection is available.

Figure 7 : ST75C52/520 High Speed Received Sequence

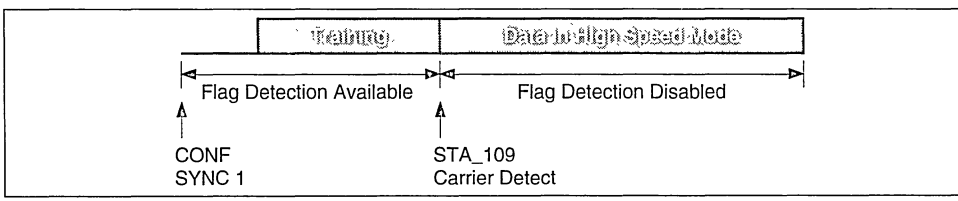


Figure 8 shows how the host can use the ST75C52/520 for flag detection when receiving TCF frame or at the beginning of C phase.

VII.3.2 - Flag Detection in C Phase

As said above the flag detection is not available while the ST75C52/520 is receiving data in high speed mode (V.17, V.29, V.27) since the DSP disables it as soon as the carrier detect status (**STA_109**) is true.

It could be interesting for the host to have the **STA_FLAG** information available in C phase just after a loss of the high speed carrier because the next received signal could be a V.21 ch2 instead a high speed carrier without a training.

Figure 9 summarizes the two cases.

In the first case the transmit unit has cut the high speed transmission (which causes the loss of the carrier) and start to send HDLC frames in V.21 ch2.

In the second case the loss of the carrier may be due to a problem on the PSTN network.

Figure 8

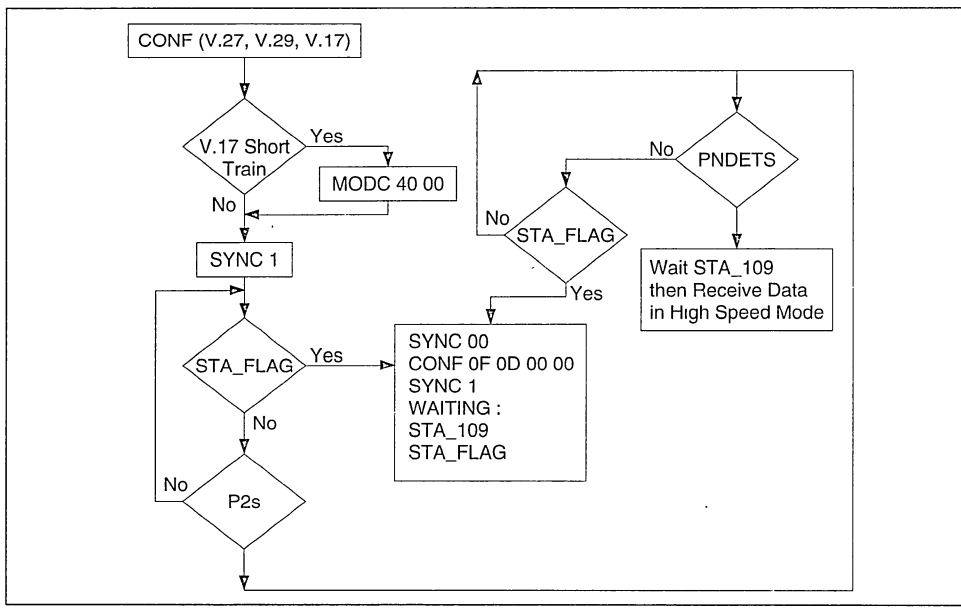


Figure 9 : ST75C52/520 Received Signal with Loos of Carrier

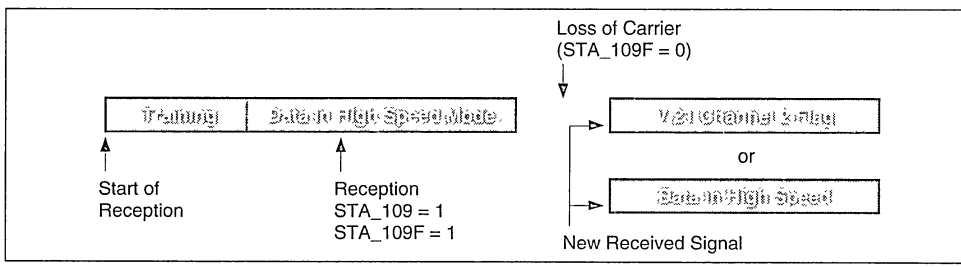


Figure 10 gives to the user the way to be able to detect V.21 ch2 flag just after a loss of high speed carrier.

To enable and disable the flag detection the host will performe a Memory Write (MW) command (see Table 1 for addresses and parameters). As the short train is only used in C phase while receiving in V.17 mode the host can avoid to send the Enb short sequence to the ST75C52/520 in V.29 and V.27.

This flow chart (Figure 10) could be used in phase B but take care that the Enb short sequence must only be sent in C phase.

VIII - EQUALIZER AT RECEPTION SIDE

The DSP provides an equalizer function in the reception section. It computes the coefficients of this equalizer firstly during the training and secondly during the first seconds of the data mode (carrier detect signal and **STA_109** are true).

In Fax application the coefficients are firstly computed when receiving the TCF frame (continuous 0 during 1.5s) in phase B of the T.30 protocol. As the DSP rev 1.0 software takes more than 1.5s when in data mode to compute the coefficients of the equalizer the host must reduce these time sending to the DSP two memory write (**MW**) command. The two **MW** must be sent just after **STA_109** equals 1 indicating a high speed modulation signal :

First MW MW E3 16 01 00

Second MW MW E3 16 B0 04

The DSP will take now 1.2s after the beginning of the data mode (**STA_109 = 1**) to compute the coefficients of the equalizer.

For DSP rev 1.1 software the problem is solved and the two **MW** need not be sent by the host.

Figure 10

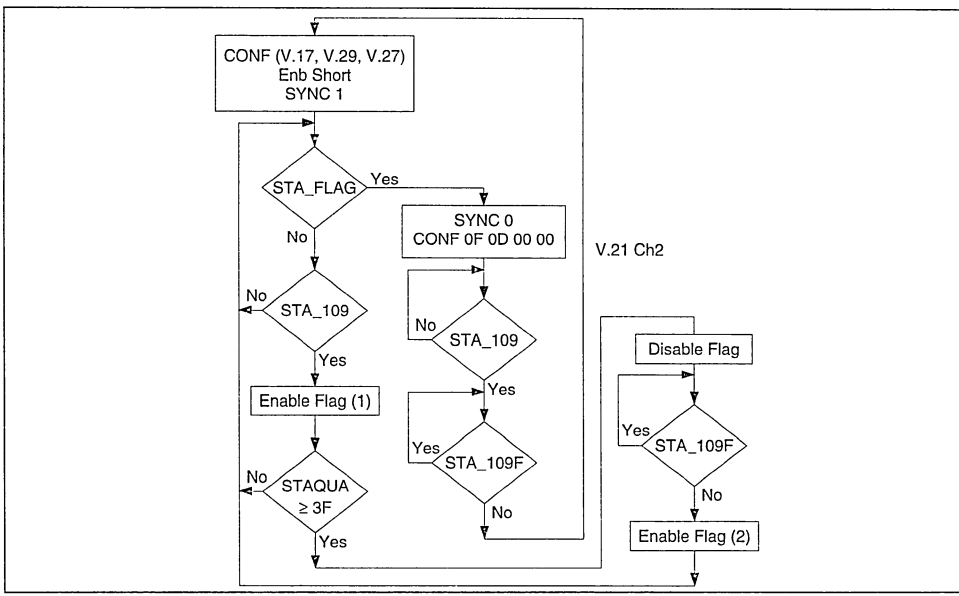


Table 1

	V.17	V.29	V.27
CONF HIGH SPEED	CONF 0F 09 00 04	CONF 0F 08 00 01	CONF 0F 07 40 00
Enbl Flag (1)	MW 15 10 14 00	MW 15 10 12 00	MW 15 10 12 00
Enbl Flag (2)	MW 15 10 14 00	MW 15 10 10 00	MW 15 10 10 00
Disable Flag	MW 15 10 04 00	MW 15 10 00 00	MW 15 10 00 00
Enb Short	MODC 40 00	MODC 00 00	MODC 00 00

AN814-01 TBL

IX - HOW ADJUST THE TRANSMIT LEVEL

As explained in the ST75C52/520 User's Manual in chapter VI.3 the user can adjust the level on the line using the **SETGN** command. Like that the user chooses an attenuation in the transmit section (no attenuation means a 0dB value for the parameter of the **SETGN** command).

There is no limitation for the attenuation values. You can use different attenuation values with a step less than 1dB between each value. The USER'S MANUAL gives as example the value for attenuation between 0dB and -14dB with a step of 1dB.

How to compute the value of the parameter for the **SETGN** command ?

As the attenuation is provided by a gain in the transmit section you must know the value of the next gain which gives the wanted attenuation. 0dB attenuation means a unit gain (Gt = 1). For 0dB the value of the **SETGN** parameter is 7FFF (hexa decimal value) or 32768 (decimal value). Suppose you would like a -10dB attenuation, in such a case your attenuation gain will have a value of Gt = 0.6065. The value of the **SETGN** parameter will be equal to 32768 x 0.6065 (decimale value) or 287A (hexadecimal value).

Now the host has only to send **SETNG 287A** (command and parameter) to the DSP to set up the attenuation gain at the wanted value.

X - HARDWARE GUIDE LINE

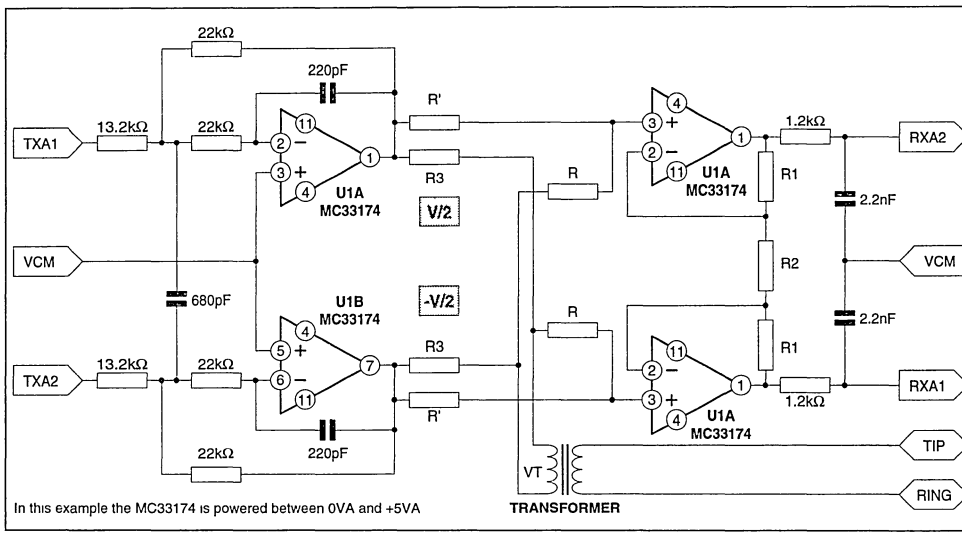
The ST75C52/520 can be connected to a host processor using INTEL or MOTOROLA bus.

A synchronisation between the ST75C52/520 and the host is provided with **SDTACK** (for data acknowledge) and **SINTR** (for interrupts) signals which are both open drain.

The analog interface is detailed in chapter VI, VII, VII of the ST75C52/520 User's Manual.

Here, we briefly cover the basic schematics and hybrid interface tuning (See Figure 11).

Figure 11



Components :

All resistors are 1% tolerance

Operational Amplifier SGS-THOMSON : MC33174

Tuning :

Return Loss :

$$R3 = \frac{R0}{2}$$

Where R0 is the value for the best return loss versus the reference inpedance Z0. And Z0 = 600Ω or Complex Impedance

Duplexor :

$$VT = \frac{Z0 \cdot V}{(Z0 + R0)}$$

$$Coef = \frac{VT}{V} = \frac{Z0}{Z0 + R0}$$

To have the best rejection : $R' = \frac{R}{Coef}$

Example 1:

Z0 = 600Ω, R0 = 600Ω

Coef = 0.5

R = 20kΩ and R' = 40kΩ

Example 2 :

Z0 = 600Ω, R0 = 440Ω

Coef = 0.577

R = 23.08kΩ and R' = 40kΩ

Transmit Gain :

Tx_Gain = 22kΩ/13.2kΩ

Today tuned to have -9dBm on the line.

To transmit at 0dBm you must :

- Replace the two 13.2kΩ 1% by two 4.64kΩ 1%.
- Replace the two 220pF by 47pF.
- Power supply of the Amplifier : +V and -V.

Receive Gain :

$$Rx\_Gain = 1 + \frac{R1}{\left(\frac{R2}{2}\right)}$$

Typical values R1 = 15kΩ, R2 = 82kΩ

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

ST75C52/ST75C520 - SINGLE ENDED AND SINGLE POWER SUPPLY HYBRID CIRCUIT

CONTENTS

I - INTRODUCTION

The ST75C52/520 uses basically a hybrid interface which allows to receive a V.17 signal between 0dBm and -45dBm with very good performances (see test report of the ST75C52/520). Such hybrid interface is perfect for high end equipment. The drawback is that the user has to use 4 operationnal amplifiers rather than 3 usally. As some manufactuers need to reduce the cost of their design we are going to introduce in this application note a simpler hybrid circuit which will save cost but also provide high performances.

II - FEATURES

II.1 - Transmission

The hybrid will use the differential output ***TXA1*** and ***TXA2*** of the ST75C52/520.

The nominal output level for each tone and each carrier must be equal to **0dBm** when no attenuation is selected in the ST75C52/520 (default setting of the ST75C52/520).

II.2 - Reception

The hybrid will only use the ***RXA1*** input of the ST75C52/520 rather than ***RXA1*** and ***RXA2*** differential inputs in the basic hybrid.

The far end carrier (modem signal) can be received between **-1dBm** and **-44dBm**.

II.3 - Power Supply

Uses only one +12V power supply.

III - ELECTRICAL SCHEMATIC

The Figures 1 and 2 show the complet electronic used (ST75C52/520 connection and its hybrid interface). As the telephone line interface is particular for each country we did not provide it on the figure.

The return loss is adjusted by the following components : R5, C7 and C8 (the values will change if the reference impedance change). In our example the reference impedance is a 600Ω resistor.

The 2 wires to 4 wires part (duplexer) is obtained by R6, R7, R8 and R9. The rejection of the unwanted signal (transmit signal at the ***RXA1*** Pin) is equal to 30dB which is enough for the full duplex modulations V.21, V.23 and BELL 103.

The transmit gain is fixed by the ratio R4/R3 and is adjusted to have an output level at 0dBm on 600Ω when no attenuation is selected in the ST75C52/520. A filter at 9.6kHz is installed on the ***TXA1*** and the ***TXA2*** output.

The receive gain is fixed by the ratio R9/R8 and must be adjusted each time the customer changes is telephone line interface components (mainly the transformer could have an insertion loss between 1 and 2dB). The received signal is connected to ***RXA1*** input and ***RXA2*** input is tied to VCM. The signal at ***RXA1*** must not be higher than 2.5V.

The tuning of such a hybrid interface could be done as indicated below :

- adjust your telephone line interface (DC current...),
- adjust the return loss,
- adjust the transmit gain,
- adjust the receive gain,
- adjust the duplexor.

Note : an iteration between step 4 and 5 could be necessary.

III.1 - Return Loss

Adjust R5, C7 and C8 to meet the technical requirements in your country which imposes the reference impedance (600Ω or complex impedance), and the different parameters as DC voltage and DC current on the line.

III.2 - Transmit Gain

We recommand the following procedure :

- keep the ***SETGN*** default value (0x7FFF) which selects no attenuation on the transmit signal,
- adjust the ratio R4/R3 to have 0dBm,
- adjust the attenuation (parameter of the ***SETGN*** command) for each signal which will be sent by the ST75C52/520. We suggest to adjust the output level at **-9dBm** for the tones and the carriers. For the DTMF we suggest an output level equal to **-4.4dBm**.

The method to compute the ***SETGN*** 's parameter is :

- no attenuation → parameter equals to 0x7FFF (hexa decimal value),
- convert this value in decimal → 32767,
- multiply 32767 by the absolute decimal value of the wanted attenuation (usally you know it in dB, so you must convert dB to absolute value),
- convert the result in hexadecimal, you have now the parameter of the ***SEGTN*** command.

Example :
Parameter for an attenuation equal to -10dB or a gain equal to 0.3162.
SETGN 's parameter in decimal value =
32767 x 0.3162 = 10361
SETGN 's parameter in hexadecimal value =
0x2879.

There is no limitation when using ***SETGN*** command, you can make a very fine tuning which is not necessarily equal to 1dB.

III.3 - Receive Gain

Adjust the ratio R9/R8 to detect carrier at -44dBm.

III.4 - Duplexer

Adjust the resistors R7 and R6 to remove unwanted carrier when in full duplex mode.

IV - OUTPUT LEVELS

With this hybrid interface the typical output levels for the different carriers when no attenuation is selected (default value for ***SETGN***'s parameter) are :

Carrier	Level (dBm on 600Ω)
Bell 103 Answer	0.88
Bell 103 Originate	0.97
V.21 Answer	0.8
V.21 Originate	1.1
V.23 Answer	0.65
V.23 Originate	0.87
V.27 ter	0.44
V.29	0
V.17	0
V.33	0
V.21 Channel 2	0.8

In the same conditions the output levels for the tones are :

Tones	Level (dBm on 600Ω)	Tones	Level (dBm on 600Ω)
DTMF 0	-0.35	DTMF A	-0.47
DTMF 1	-0.3	DTMF B	-0.47
DTMF 2	-0.35	DTMF C	-0.47
DTMF 3	-0.4	DTMF D	-0.47
DTMF 4	-0.35	DTMF *	-0.3
DTMF 5	-0.35	DTMF #	-0.35
DTMF 6	-0.4	2100Hz	0.15
DTMF 7	-0.3	1650Hz	0.52
DTMF 8	-0.35	2225Hz	0
DTMF 9	-0.4	1300Hz	0.75

To adjust the factory output level of your equipment use the ***SETGN*** command as explain on Chapter III. We simply recall the parameters for typical attenuation (see Table below).

Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)
0	7FFF	-5	47FA	-10	287A
-1	7214	-6	4026	-11	2413
-2	65AC	-7	392C	-12	2026
-3	5A9D	-8	32F5	-13	1CA7
-4	50C3	-9	2D6A	-14	198A

V - PCB GUIDE LINE

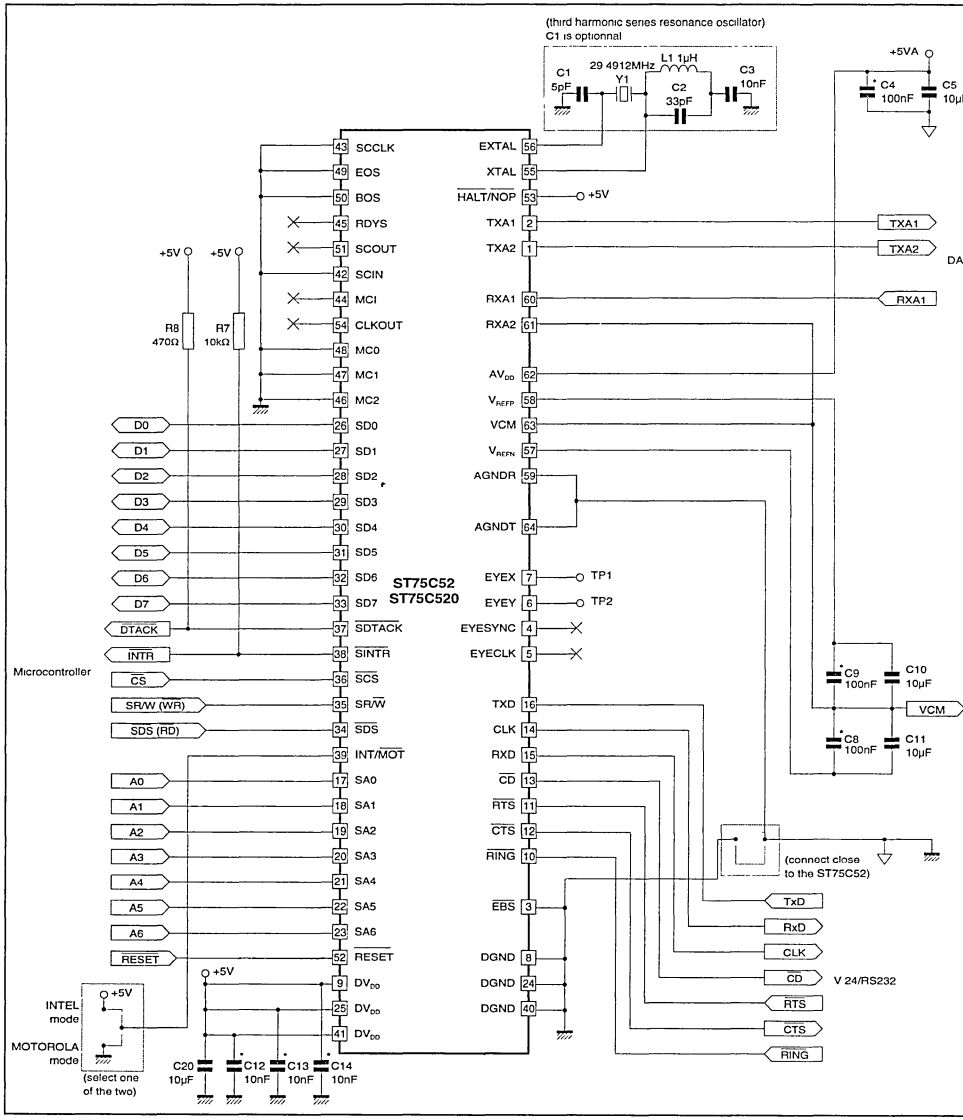
For that application note we use a two layers board.

Analog (***AV_{DD}***) and digital (***DV_{DD}***) power supplies are connected together. The capacitors used for the power supply (***DV_{DD}***, ***AV_{DD}***) decoupling are installed as close as possible to the power pins.
The capacitors used for the voltage refence (between V_{REFP}/VCM and V_{REFN}/VCM) are connected as close as possible to the pins.
Both analog ground ***AGNDR*** and ***AGNDT*** must be connected with very low impedance to a single point.
The 2.2nF connected beween ***RXA1*** and ***RXA2*** Pins must be as close as possible to them.
Provide a ground grid in all around and under components on both sides of the band and connect them to avoid small islands.

VI - OUT OF BAND POWER

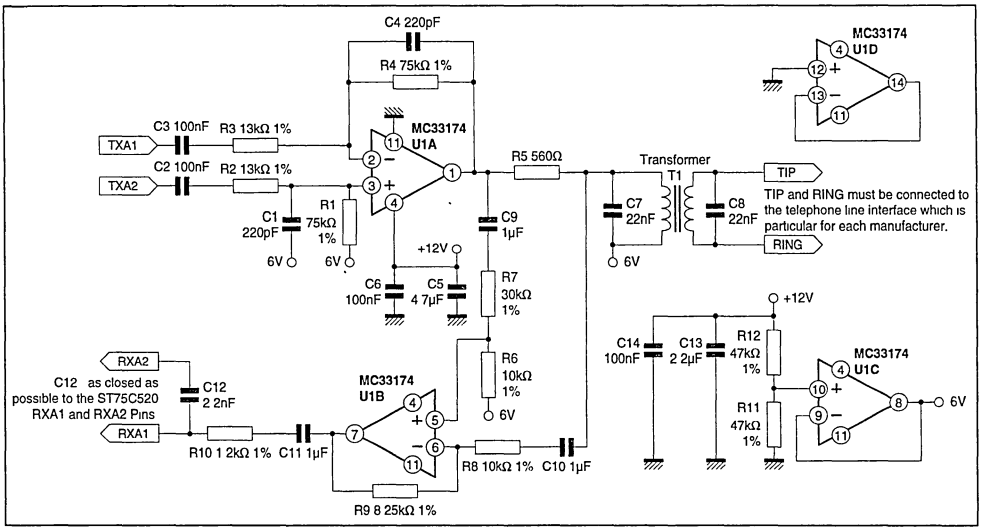
This hybrid (Figure 2) needs a filter in the transmit side to avoid out of band power due to the sigma delta convertors. Two one pole filters are used. The first is built around the MC33174 operational amplifier (Pin 1, 2, 3) with the R3, R4, C4, R2, R1, C1 components (Fc is equal to 9.6kHz). The second pole is introduced with C7 in parallel with the line transformer.
In that case the out of band power (frequencies above 4kHz) is 60dB lower than the in band power.

Figure 1



Note : All capacitor with a "*" must be implented close to the ST75C52/520 pin.

Figure 2 : Differential Output and Single Ended Reception Uses only One Power Supply



VII - PERFORMANCES AT 14400bps (V.17)

We tested this hybrid doing Bit Error Rate Test (BERT) on a TAS equipment. Mainly we did BERT versus different Signal to Noise Ratio (SNR) for various lines.

The Figures 3 and 4 show the results on a Flat line (L1) while receiving between -1dBm and -43dBm. The ST75C52/520 begins to make error in reception at a SNR equals to 23dB ±1dB. These results are identical to thus obtained with the hybrid which uses the differential inputs ***RXA1*** and ***RXA2***.

The Figure 5 shows the result when receiving via European line, US lines and Japanese lines. Also in that case the performances are equal to thus that we obtained with the first hybrid which uses the differential inputs ***RXA1*** and ***RXA2***.

Figure 3 : Reception on Flat Line L1 at -1, -3, -6, -9, -20dBm

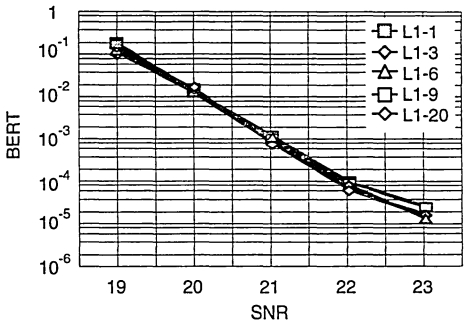


Figure 4 : Reception on Flat Line L1 at -30, -35, -38, -40, -43dBm

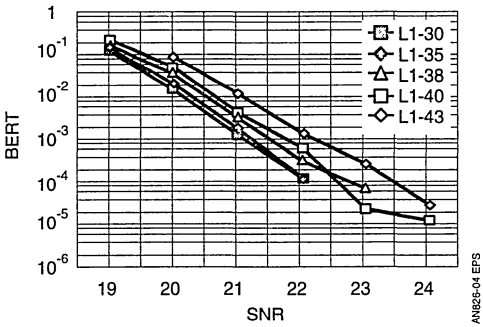
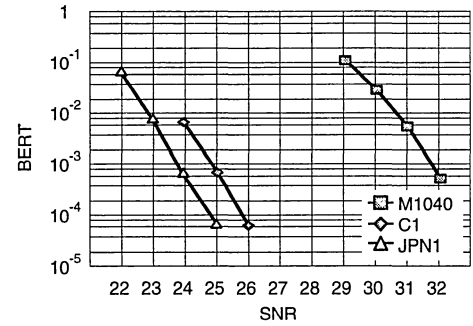


Figure 5 : BERT on M1040, C1, JPN1



VIII - CONCLUSION

This new hybrid interface is simpler than the full differential (differential outputs and inputs) introduced in the Data Sheet.

It will be easier for the customer to adjust return loos again complex impedance with this new hybrid.

Single power supply is some times necessary to save cost of the power equipment.

The performances still remain very good.

We suggest this hybrid interface in some application where level has to be transmitted at high level (greater than -9dBm) and where single power supply schematic must be used.

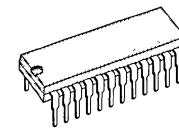
LOW SPEED MODEM

PROGRAMMABLE V.23 MODEM WITH DTMF

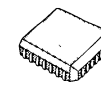
- PROGRAMMABLE MODES :
  - Modem 75bps transmit, 1200bps receive
  - Modem 1200bps transmit, 75bps receive
  - DTMF dialing
  - Call status tone detection
  - Auxiliary analog transmit input
  - Analog test loopback
- PROGRAMMABLE FUNCTIONS :
  - Transmission level
  - Hysteresis and detection level
  - Filters (reception and transmission)
  - Line monitoring and buzzer
  - DTMF frequencies
- FIXED COMPROMISE LINE EQUALIZER
- AUTOMATIC BIAS ADJUSTMENT
- INTEGRATED DUPLEXER
- STANDARD LOW COST CRYSTAL (3.579MHz)
- TAX TONE REJECTION
- POWER-UP INITIALIZATION OF REGISTERS
- OPERATES FROM ±5V
- CMOS

DESCRIPTION

The TS7514 is an FSK modem which can be programmed for asynchronous half-duplex voice-band communications on a 2-wire line or full duplex on a 4-wire line. Its programming concept makes it the ideal component to design low-cost intelligent modems, featuring auto dialing and auto answering. The TS7514 conforms to CCITT V.23 recommendation. The chip incorporates DTMF dialing, line monitoring, tone and dialing detection.



DIP24
(Plastic Package)



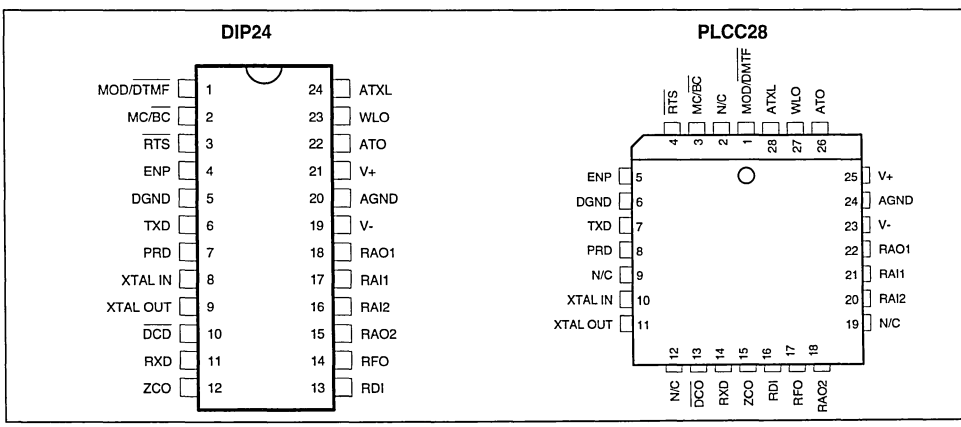
PLCC28
(Plastic Package)

ORDER CODES

Part Number	Temperature Range	Package
TS7514CP	0 to 70°C	DIP24
TS7514CFN	0 to 70°C	PLCC28

7514-01 TBL

PIN CONNECTIONS



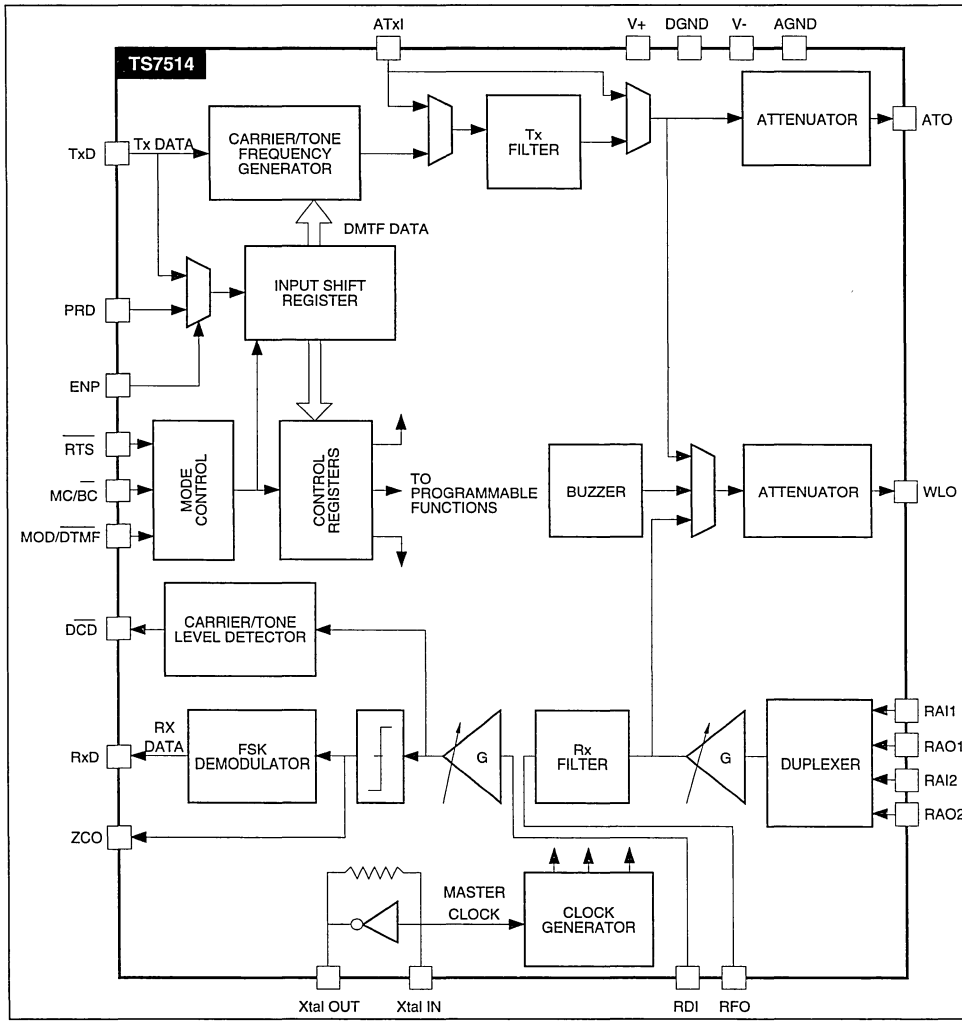
7514-01 EPS / 7514-02 EPS

PIN DESCRIPTION

Name	Pin Number		Description
	DIP24	PLCC28	
MOD/$\overline{DMTF}$	1	1	MODEM or DMTF Operating Mode Selection. Also controls write operations to control registers (if MOD/$\overline{DMTF}$ = 0 and MC/$\overline{BC}$ = 0).
MC/$\overline{BC}$	2	3	Digital Control Input. In MODEM mode, it sets transmission mode to main or back channel. It also permits selection of dialing or control registers programming.
$\overline{RTS}$	3	4	Request to Send. When $\overline{RTS}$ = 0, the circuit sends an analog signal to the ATO output. The signal depends on the operating mode selected. When $\overline{RTS}$ = 1, the signal sent to ATO is suppressed after its first zero crossing. When MOD/$\overline{DMTF}$ = 0 and MC/$\overline{BC}$ = 0, the $\overline{RTS}$ pin acts as a clock for serial data loading into the input register.
ENP	4	5	Serial Register Write Select Input. When ENP = 0, the serial register input is connected to TxD. When ENP = 1, the register input is connected to PRD.
DGND	5	6	Digital Ground = 0V. All digital signals are referenced to this pin.
TxD	6	7	Digital Input for Transmit or Control Data
PRD	7	8	Digital Input for Control Data. Selected through ENP
XtalIN	8	10	Crystal Oscillator Input. Can be tied to an external clock generator. F quartz = 3.579MHz.
XtalOUT	9	11	Crystal Oscillator Output
DCD	10	13	Data Carrier Detect Output
RxD	11	14	Digital Receive Data Output
ZCO	12	15	Zero Crossing Rx Digital Output (ringing detection)
RDI	13	16	Analog Output for the Receive Signal after Filtering or Analog Input for the Amplifier-limiter.
RFO	14	17	Analog Receive Filter Output
RAO2	15	18	A2 Amplifier Output
RAI2	16	20	A2 Amplifier Inverting Input
RAI1	17	21	A1 Amplifier Inverting Input
RAO1	18	22	A1 Amplifier Output
V-	19	23	Negative Supply Voltage : – 5V ±5%
AGND	20	24	Analog Ground = 0 V. Reference Pin for Analog Signals
V+	21	25	Positive Supply Voltage : + 5V ±5%
ATO	22	26	Analog Transmit Output
WLO	23	27	Analog Output for Line Monitoring and Buzzer
ATxI	24	28	Direct Analog Input Transmit Filter

7514-02.TBL

Figure 1 : Simplified Block Diagram



FUNCTIONAL DESCRIPTION

The TS7514 circuit is an FSK modem for half-duplex, voice-band asynchronous transmissions on a 2-wire line according to CCITT recommendation V.23 or full duplex on 4 wire-line.

The circuit features DTMF dialing, call status tone detection and line monitoring in both dialing and automatic answer modes. A signalling frequency is available at the line monitoring output (buzzer).

Ring detection is possible by using the signal detection function and bypassing the receive filter. The receive signal at ZCO output can be filtered in the associated microprocessor.

The TRANSMIT channel (Tx) includes :
- Two programmable frequency generators.
- One switched capacitor filter (SCF) with low-pass or bandpass configuration and its associated propagation delay corrector.
- One continuous time low-pass smoothing filter.
- One attenuator, programmable from 0 to + 13dB by 1dB steps.
- One programmable analog input.

The RECEIVE channel (Rx) includes :
- Two operational amplifiers for duplexer implementation.
- One continuous time low-pass anti-aliasing filter.
- One programmable gain amplifier.
- One linear compromise equalizer.
- One switched capacitor band pass filter (can be set to either main or back channel).
- One continuous time low pass smoothing filter.
- One limiting amplifier.
- One correlation demodulator.
- One programmable level signal detector.

The LINE MONITORING channel includes :
- One buzzer.
- One 3-channel multiplexer to select beetwen :
  - Transmit channel monitoring.
  - Receive channel monitoring.
  - Buzzer.
- One programmable attenuator

Internal Control

POWER-UP INITIALIZATION

The TS7514 includes power-up initialization of control registers. This system sets the ATO transmission output to an infinite attenuation position, leaving time for the microprocessor to set up the RPROG input on power up. Control registers are also initialized when V+ is lower than 3V or V- greater than -3V.

REGISTERS

Write access to the DTMF data register and to other control registers is achieved in serial mode through TxD input or PRD input. Addressing of these 4 bit registers is indirect. They are accessed through an 8 bit shift register addressed when MOD/DTMF = 0 and MC/BC = 0. Data sent to the TxD input is strobed on the RTS signal trailing edge.

Serial data is sent to the TxD input, with Least Significant Bit (LSB) first. The 4 Most Significant Bits (MSB) contain the control register address while the 4 LSB contain associated data.

Data transfer from the input register to the control register (addressed by the MSB's) is started by the operating mode (MODEM or DTMF) selection (MOD/DTMF = 1 or MC/BC = 1).

Figure 2 : Internal Control Register

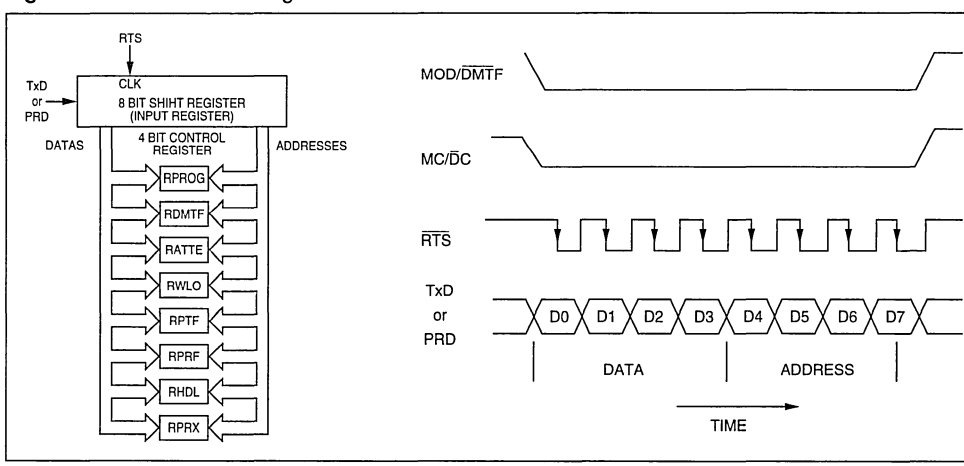
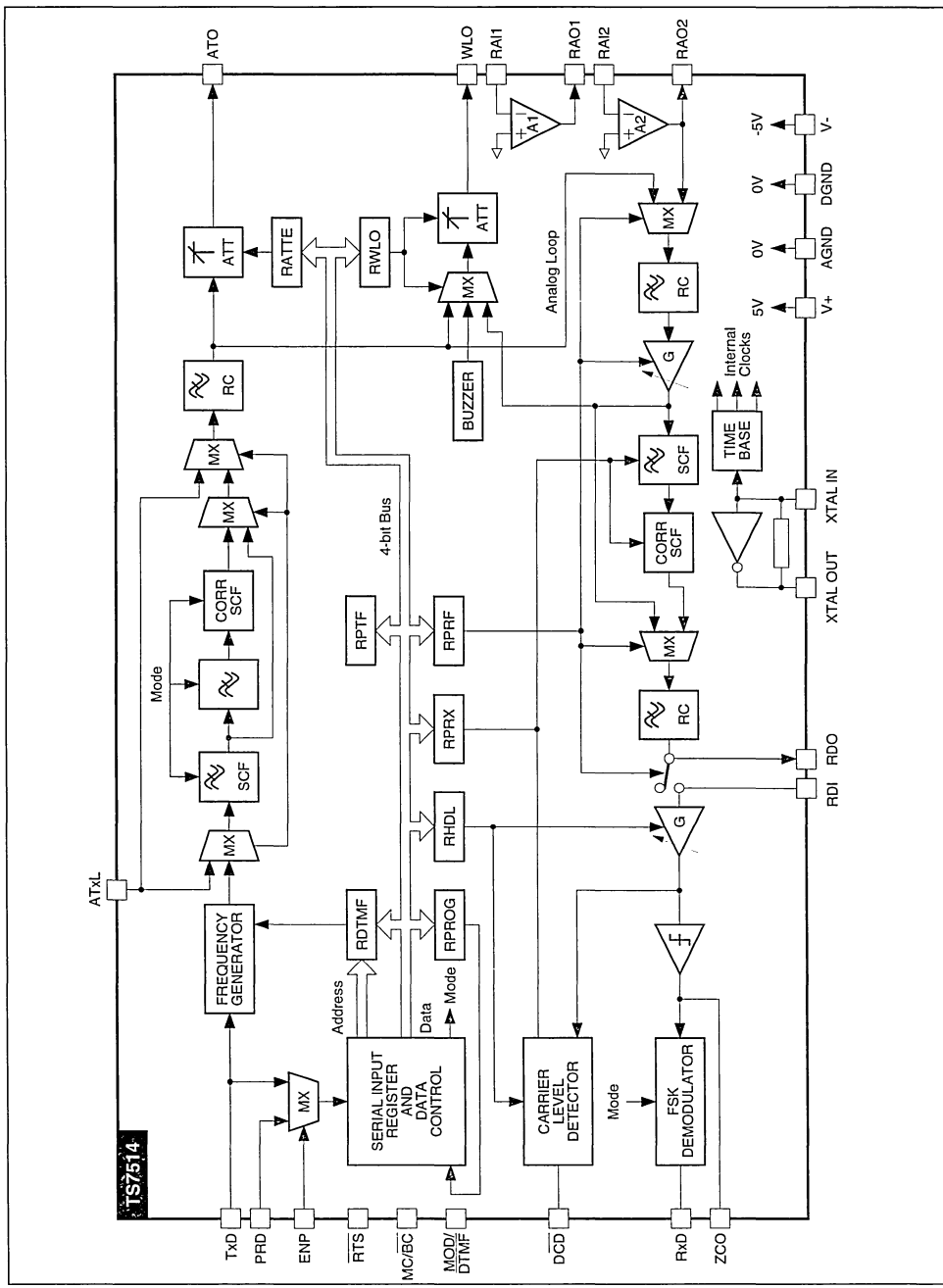


Figure 3 : Detailed Block Diagram



OPERATING MODES

The various operating modes are defined by MC/$\overline{BC}$ and MOD/$\overline{DTMF}$ inputs, and by the content of a control register RPROG.

The TS7514 includes 8 control registers. Access to each control register is achieved through an auxiliary 8-bit shift register (input register). The input of that shift register is connected either to TxD or PRD, depending upon the status of the ENP control pin (ie when ENP = 0 and ENP = 1 respectively). In both cases, the $\overline{RTS}$ input receives the shift clock and sequentialy transfer is controlled by setting simultaneously MOD/$\overline{DTMF}$ and MC/$\overline{BC}$ to 0. The previous internal status and data are memorized during loading of the input register so that transmission continues properly. That feature allows the user to modify transmission level or line monitoring selection during transmission. The transmit channel operating mode (Modem main or back channel, DTMF) can only be modified when $\overline{RTS}$ = 1. When RTS = 0, the ATO transmit output is enabled and the preselected operating mode is activated. When RTS returns to 1, Modem or DTMF transmission is inhibited after the first zero crossing of the generated signal.

MOD/$\overline{DTMF}$	MC/$\overline{BC}$	**Transmission** (ATO)	**Reception** (RxD, $\overline{DCD}$)
1	1	MODEM, Main Channel	MODEM, Back Channel
1	0	MODEM, Back Channel	MODEM, Main Channel
0	1	DTMF	$\overline{DCD}$= Active Tone Detection (270 -500Hz) if $\overline{RTS}$ = 1... DCD = 1 if RTS = 0
0	0	If $\overline{RTS}$ = 0 when that configuration occurs, transmission and reception are not modified. If RTS = 1 (no signal sent on the line), transmission is not modified and reception is set up to detect 2100Hz tone (note 1).	

Note 1 : The decision threshold of the demodulator output is shifted, so that RxD changes from 0 to 1 at 1950Hz instead of 1700Hz.

MODEM TRANSMISSION FREQUENCIES

Modulation Rate	TxD	CCITT R35 AND V.23 Recommendations (Hz)	Frequency Generated with Xtal at 3.579MHz (Hz)	Error (Hz)
75bps	1 0	390 ±2 450 ±2	390.09 450.45	+0.09 +0.45
1200bps	1 0	1300 ±10 2100 ±10	1299.76 2099.12	-0.24 -0.88

DTMF TRANSMISSION FREQUENCIES

	Specifications DTMF (Hz)	Frequency Generated with Xtal at 3.579MHz (Hz)	Dividing Ratio	Error (%)
f1	697 ±1.8%	699.13	5120	+0.31
f2	770 ±1.8%	771.45	4640	+0.19
f3	852 ±1.8%	853.90	4192	+0.22
f4	941 ±1.8%	940.01	3808	-0.10
f5	1209 ±1.8%	1209.31	2960	+0.03
f6	1336 ±1.8%	1335.65	2680	-0.03
f7	1477 ±1.8%	1479.15	2420	+0.15
f8	1633 ±1.8%	1627.07	2200	+0.36

CARRIER LEVEL DETECTOR

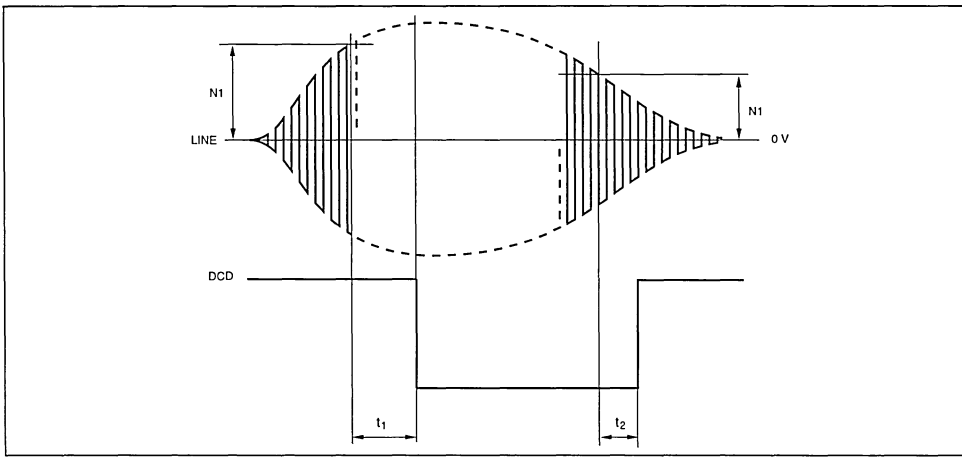
- Output Level Detection conditions
  The DCD signal detector output is set to logic state 0 if the RMS value of the demodulator input signal is greater than N1. The DCD output has logic state 1 if the RMS value is less than N2.
  The detector has an hysteresis effect : N1 - N2.

- Timing Detection Requirements
  Signal detection time constants at the $\overline{DCD}$ output comply with CCITT Recommendation V.23.

Modulation Ratio	DCD Transition	CCITT V.23 (min)	Min.	Max.	CCITT V.23 (max)	Unit
1200bps	t1 t2	10 5	10 5	20 15	20 15	ms ms
75bps (Note 1)	t1 t2	0 15	15 15	40 40	80 80	ms ms

Note 1 : wide band Rx filter used (see Figure 7c).

Figure 4 : Signal Detection Time Out



Note : When delays are bypassed (see RPRX register programming) response time ranges from 0 to 5ms in receive mode at 1200bps, and from 0 to 10ms at 75bps.

PROGRAMMING REGISTER

RPROG

Address				Data				Selected Mode (note 1)
D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	0 0	X X	0 1	0 1	The most significant bit (D7) is not used when decoding control register addresses.
				0	X	0	1	Control register addressing is enabled when D7 = 0 (see note 2).
				0	X	1	0	Control register addressing is enabled when D7 = 1 (see note 2).
				0	0	X	X	Reception positioned in the channel opposite to the transmission channel controlled by MC/BC
				0	1	X	X	Reception positioned in the same channel as transmission (see note 3).
				1	X	X	X	Programming inhibited in normal operating mode. This mode is used for testing purposes.

Notes : 1. RPROG is set to 0000 on power-up.
2. Excepted for RPROG register whose address is always 000, regardless of D0 and D1.
3. This mode allows either full duplex operation on a 4-wire line, or circuit testing with external Tx/Rx loopback.

DTMF DIALING DATA REGISTER

RDTMF REGISTER

Address				Data				Tone Frequency (Hz)	
D7	D6	D5	D4	D3	D2	D1	D0	LOW	HIGH
P	0	0	1	X	X	0	0	697	X
				X	X	0	1	770	X
				X	X	1	0	852	X
				X	X	1	1	941	X
				0	0	X	X	X	1209
				0	1	X	X	X	1336
				1	0	X	X	X	1477
				1	1	X	X	X	1633

Notes : This register is not initialized on power-up.
X : don't care value.
P : 1,0 or X depending upon RPROG content.

DATA REGISTER FOR THE TRANSMISSION ATTENUATOR

RATE REGISTER

Address				Data				Attenuation (dB)	Output Transmit Level (dBm)	On Line Level (dBm) Coupler Gain (- 6dB)
D7	D6	D5	D4	D3	D2	D1	D0			
P	0	1	0	0	0	0	0	0	+ 4	– 2
				0	0	0	1	1		+ 3
				0	0	1	0	2	+ 2	– 4
				0	0	1	1	3	+ 1	– 5
				0	1	0	0	4	0	– 6
				0	1	0	1	5	– 1	– 7
				0	1	1	0	6	– 2	– 8
				0	1	1	1	7	– 3	– 9
				1	0	0	0	8	– 4	– 10
				1	0	0	1	9	– 5	– 11
				1	0	1	0	10	– 6	– 12
				1	0	1	1	11	– 7	– 13
				1	1	0	0	12	– 8	– 14
				1	1	0	1	13	– 9	– 15
				1	1	1	0	Infinite	< – 64	< – 70
				1	1	1	1	Infinite*	< – 64 *	< – 70 *

* Power-up configuration.

LINE MONITORING PROGRAMMING REGISTER

RWLO REGISTER

Address				Data				Line Monitoring In Transmit Mode Relative Level (dB)	Line Monitoring In Receive Mode Relative Level (dB)	
D7	D6	D5	D4	D3	D2	D1	D0			
P	0	1	1	0	0	0	0	– 10		
				0	0	0	1	– 20		
				0	0	1	0	– 31		
				0	0	1	1	– 42		
				0	1	0	0		0	
				0	1	0	1		– 10	
				0	1	1	0		– 20	
				0	1	1	1		– 31	
				1	0	0	0			0.42 V_{PP}
				1	0	0	1			– 10dB
				1	0	1	0			– 20dB
				1	0	1	1			– 31dB
				1	1	X	X			< – 60dB*

* Power-up configuration.
Note : Signaling frequency is a square wave signal at 2982Hz.

RECEIVE FILTER SELECTION AND GAIN PROGRAMMING REGISTER

RPRF REGISTER

Address				Data				Reception Gain (dB) (note 1)	Comments
D7	D6	D5	D4	D3	D2	D1	D0		
P	1	0	1	X	X	0	0	0	
				X	X	0	1	+ 6 *	
				X	X	1	0	+ 12	
				X	X	1	1	0	Rx Channel Band = Tx Channel B and Tx to Rx Loopback – 33dBm ≤ Rx Level ≤ 40dBm
				X	0	X	X	X	Receive Filter Selected
				X	1	X	X	X	Receive Filter Desabled
				1	X	X	X	X	Receive Filter Disconnected from RDI Output and from Demodulator. Offset Disabled.

* Power-up configuration.
Note 1 : Depending on the line length, the received signal can be amplified. Programmable reception gain allows a level close to +3dBm at the filter input to take benefit of the maximum filter dynamic range (S/N ratio). The following requirement must be met : max. line level + prog. gain ≤+3dBm.

TRANSMISSION FILTER PROGRAMMING REGISTER

RPTF REGISTER

Address				Data				ATO Transmission
D7	D6	D5	D4	D3	D2	D1	D0	
P	1	0	0	0	0	0	0	MODEM or DTMF Signal*
				0	0	0	1	ATxI via Smoothing Filter and Attenuator
				0	0	1	0	ATxI via Low-pass Filter and Attenuator
				0	0	1	1	ATxI via Band-pass Filter and Attenuator
				0	1	0	0	In DTMF Mode, Transmision of High Tone Frequency
				1	0	0	0	In DTMF Mode, Transmission of Low Tone Frequency

* Power-up configuration.

HYSTERESIS AND SIGNAL DETECTION LEVEL PROGRAMMING REGISTER

RHDL REGISTER

Address				Data				N2 (dBm) (note 1) See Figure 4	N1/N2 (dB)
D7	D6	D5	D4	D3	D2	D1	D0		
P	1	1	0	X	0	0	0	– 43 *	X
				X	0	0	1	– 41	X
				X	0	1	0	– 39	X
				X	0	1	1	– 37	X
				X	1	0	0	– 35	X
				X	1	0	1	– 33	X
				X	1	1	0	– 31	X
				X	1	1	1	– 29	X
				0	X	X	X	X	3 *
				1	X	X	X	X	3.5

* Power-up configuration.
Note 1 : Detection low level measured at the demodulator input. The line signal detection level is obtained by reducing the gain ate the filter.

RECEIVE CHANNEL PROGRAMMING REGISTER

RPRX REGISTER

Address				Data				Configuration
D7	D6	D5	D4	D3	D2	D1	D0	
P	1	1	1	X	X	0	X	Low Frequency Wide Band Selected (Figure 7b) (Note 1)
				X	X	1	X	Low Frequency Narrow Band Selected (Figure 7c)
				X	X	X	0	Carrier Level Detector Delay Enabled*
				X	X	X	1	Carrier Level Detector Delay Disabled.

Note 1 : In active tone detection mode (MOD/$\overline{\text{DTMF}}$ = Ø, MC/$\overline{\text{BC}}$ = 1, $\overline{\text{RTS}}$ = 1 see op. modes),
The low frequency wide band is automatically selected for the receive channel, whatever the RPRX register programming value.
After a switch back to modem mode (MOD/DTMF = 1, MC/BC = Ø or 1) the RPRX register indicates again the value programmed before the active tone detection mode.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
DGND	DGND (digital ground) to AGND (analog ground)	– 0.3, + 0.3	V
V+	Supply Voltage V+ to DGND ro AGND	– 0.3, + 7	V
V–	Supply Voltage V- to DGND or AGND	– 7, + 0.3	V
V_I	Voltage at any Digital Input	DGND - 0.3, V+ + 0.3	V
V_{in}	Voltage at any Analog Input	V– 0.3, V + + 0.3	V
I_o	Current at any Digital Output	– 20, + 20	mA
I_{out}	Current at any Analog Output	– 10, + 10	mA
P_{tot}	Power Dissipation	500	mW
T_{op}	Operating Temperature	0, + 70	°C
T_{stg}	Storage Temperature	– 65, + 150	°C
T_{lead}	Lead Temperature (soldering, 10s)	+ 260	°C

7514-03 TBL

If the Maximum Ratings are exceeded, permanent damage may be caused to the device. This is a stress rating only, and functional operation of the device under these or any other conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to the device.

ELECTRIC OPERATING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V+	Positive Supply Voltage	4.75	5	5.25	V
V–	Negative Supply Voltage	– 5.25	– 5.0	– 4.75	V
I+	V+ Operating Current	–	10	15	mA
I-	V- Operating Current	– 15	– 10	–	mA

7514-04 TBL

DC AND OPERATING CHARACTERISTICS

Electrical characteristics are guaranteed over the complete temperature range, with typical load unless otherwise specified. Typical values are given for : V^+ = +5V, V^- = -5V and room temperature = 25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DIGITAL INTERFACE (MOD/$\overline{DTMF}$, $\overline{RTS}$, $\overline{DCD}$, RxD, ZCO, TxD, MC/$\overline{BC}$, ENP, PRD)						
V_{IL}	Input Voltage, Low Level		–	–	0.8	V
V_{IH}	Input Voltage, High Level		– 2.2	–	–	–
I_{IL}	Input Current, Low Level	DGND < V_I < V_{IL} (max)	– 10	–	10	µA
I_{IH}	Input Current, High Level	V_{IH} (min) < V_I < V+	– 10	–	10	µA
I_{OL}	Output Current, Low Level	V_{OL} = 0.4V	1.6	–	–	mA
I_{OH}	Output Current, High Level	V_{OH} = 2.8V	–	–	– 250	µA
ANALOG INTERFACE-PROGRAMMABLE (ATxI)						
V_{in}	Input Voltage Range		– 1.8	–	+ 1.8	V
I_{in}	Input Current (filter output selected)		– 10	–	+ 10	µA
C_{in}	Input Capacitance (ATT output selected)		–	–	20	pF
R_{in}	Input Resistance (ATT output selected)		100	–	–	kΩ
ANALOG INTERFACE - TRANSMIT OUTPUT (ATO) (load conditions R_L = 560Ω, C_L = 100pF)						
V_{OS}	Output Offset Voltage		– 250	–	+ 250	mV
C_L	Load Capacitance		–	–	100	pF
R_L	Load Resistance		–	560	–	Ω
V_{out}	Output Voltage Swing		– 1.8	–	+ 1.8	V
R_{out}	Output Resistance		10	–	25	Ω
–	ATO Attenuation Ratio when $\overline{RTS}$ = 1		70	–	–	dB

7514-05 TBL

DC AND OPERATING CHARACTERISTICS (continued)

Electrical characteristics are guaranteed over the complete temperature range, with typical load unless otherwise specified. Typical values are given for : $V^+ = +5V$, $V^- = -5V$ and room temperature = 25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ANALOG INTERFACE - LINE MONITORING (WLO (load conditions , $R_L = 10k\Omega$, $C_L = 50pF$)						
V_{OS}	Output Offset Voltage		– 250	–	+ 250	mV
C_L	Load Capacitance		–	–	100	pF
R_L	Load Resistance		10	–	–	kΩ
V_{out}	Output Voltage Swing		– 1.8	–	+ 1.8	V
R_{out}	Output Resistance		–	–	15	Ω
–	WLO Attenuation Ratio		70	–	–	dB
ANALOG INTERFACE - DUPLEXER (RAI+, RAI-, RA0)						
V_{in}	Input Voltage Range RAI+, RAI–		–2	–	+2	V
I_{in}	Input Current RAI+, RAI–		–10	–	+10	µA
C_{in}	Input Capacitance RAI+, RAI–		–	–	10	pF
V_{off}	Input Offset Voltage RAI+, RAI–		–20	–	+20	mV
V_{out}	Output voltage Swing, RA0	$C_L = 100pF$ $R_L = 600\Omega$ $R_L = 300\ \Omega$	–1.8 –0.9	– –	+1.8 +0.9	V V
C_L	Load Capacitance RA01	$C_L = 100pF$	–	–	100	pF
R_L	Load Resistance RA01		300	–	–	Ω
G	DC voltage Gain in Large Signals, RA01	$C_L = 100pF$, $R_L = 300\Omega$	60	–	–	dB
CMRR	Common Mode Rejection Ratio, RA01, RA02		60	–	–	dB
PSRR	Supply Voltage Rejection Ratio, RA01, RA02		60	–	–	dB
V_{out}	Output Voltage Swing, RA02	$C_L = 50pF$, $R_L = 10k\Omega$	–2.5	–	2.5	pF
C_L	Load Capacitance, RA02		–	–	50	pF
R_L	Load Resistance, RA02		10	–	–	kΩ
AV_O	DC Voltage Gain in Large Signals, RA02		–		–	dB
ANALOG INTERFACE-RECEIVE FILTER OUTPUT (RFO) Amplifier Limiter Input (RDI)						
V_{in}	Input Voltage Range (RPRF = 1 xxx)		– 2.2	–	+ 2.2	V
R_{in}	Input Resistance (RPRF = 1 xxx)		1.5	–	–	kΩ
C_{in}	Input Capacitance (RPRF = 1 xxx)		–	–	20	pF
C_L	Load Capacitance (RPRF = 1 xxx)		–	–	50	pF
R_L	Load Resistance		1.5	–	–	kΩ
V_{out}	Output Voltage Swing	$C_L = 50pF$, $R_L = 1.5k\Omega$	– 1.8	–	+ 1.8	V
R_{out}	Output Resistance		–	–	15	Ω
DYNAMIC CHARACTERISTICS FOR PROGRAMMING REGISTER ACCESS (see Figures 5 and 6)						
t_{CYC} (1)	Cycle Time		600	–	–	ns
P_{wel} (2)	Pulse Width, $\overline{RTS}$ Low		300	–	–	ns
P_{Weh} (3)	Pulse Width, $\overline{RTS}$ High		300	–	–	ns
t_r, t_f (4)	$\overline{RTS}$ Rise and Fall Times		–	–	50	ns
t_{HCE} (5)	Control Input Holding Time		100	–	–	ns
t_{SCE} (6)	Control Input Setup Time		300	–	–	ns
t_{SDI} (7)	TxD or PRD Input Setup Time		200	–	–	ns
t_{HDI} (8)	TxD or PRD Input Hold Time		100	–	–	ns
t_{WW} (9)	TWW Input Writing Inpulsion Width (high level)		300	–	–	ns
t_{BD} (10)	TxD Input Setup Time		100	–	–	ns
t_{HD} (11)	TxD Input Hold Time		100	–	–	ns

7514-06 TBL

INPUT SHIFT REGISTER ACCESS

Figure 5 : 1st Case : Programmation without Data Transmission

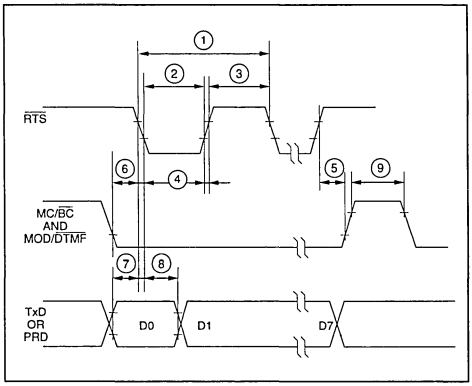
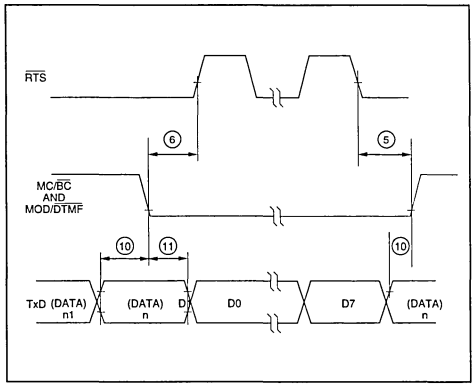


Figure 6 : 2nd Case : Programmation with TXD During Data Transmission



DC AND OPERATING CHARACTERISTICS (continued)

Electrical characteristics are guaranteed over the complete temperature range, with typical load unless otherwise specified. Typical values are given for : $V^+ = +5V$, $V^- = -5V$ and room temperature = 25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TRANSMIT FILTER TRANSFER FUNCTION (load conditions : $R_L = 560\Omega$, $C_L = 100pF$)						
G_{AR}	Absolute Gain at 2100Hz		–	0	–	dB
G_{HH}	Gain Relative to Gain at 1700Hz	Band-pass				
		< 390Hz	–	–	- 30	dB
		= 390Hz	–	–	- 35	dB
		= 450Hz	–	–	- 35	dB
		= 1100Hz	- 0.5	–	+0.5	dB
		Band-pass or Low-pass				
		1100Hz to 2300Hz	- 0.5	–	+0.5	dB
		3300Hz	–	– 3	–	dB
		5800Hz	–	–	- 15	dB
		> 16000Hz	–	–	- 35	dB
D_{AR}	Group Delay (modem transmission)					
	Main Channel : from 380 to 460Hz		90	–	110	µs
	Back Channel : from 1100 to 2300Hz		1.04	–	1.08	ms
ATTENUATOR TRANSFER FUNCTION						
A_{TT}	Absolute Gain for 0dB Programmed		0.3	0	0.3	dB
R_{AT}	Attenuation Relative to Programmed Value		- 0.5	-	+0.5	dB
	Attenuation for Programmed Value = ∞		70	-		dB
R_{LT}	Relative Attenuation between two Consecutive Steps		0.8	-	1.2	dB
TRANSMIT GENERAL CHARACTERISTICS						
	Modem Amplitude (Att = 0dB)	390Hz	+3.5	–	+4.5	dBm
		450Hz	+3.5	–	+4.5	dBm
		1300Hz	+3.5	–	+4.5	dBm
		2100Hz	+3.5	–	+4.5	dBm
	DTMF Amplitude (Att = 0dB)					
	- Low Frequency Group		- 3	–	- 1.5	dBm
	- Low Frequency Group versus Low Frequency Group		+1.5	–	+2.5	dB
	Psophometric Noise		–	–	250	µV

7514-07 TBL

DC AND OPERATING CHARACTERISTICS (continued)

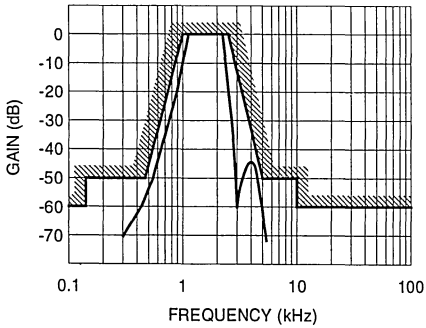
Electrical characteristics are guaranteed over the complete temperature range, with typical load unless otherwise specified. Typical values are given for : V^+ = +5V, V^- = -5V and room temperature = 25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RECEIVE FILTER TRANSFER FUNCTION						
G_{AR}	Absolute Gain at 1100Hz - Main Channel (0dB programmed)		– 0.5	–	+ 0.5	dB
G_{RR}	Gain Relative to the Gain at 1300Hz (0dB programmed)	< 150Hz 150Hz to 450Hz 1300Hz 2100Hz 2300Hz 5500Hz to 10000Hz > 10000Hz	– – – 0.5 1.1 – – –	– – – 1.8 – – –	– 60 – 50 0.5 2.3 2.7 – 50 – 60	dB dB dB dB dB dB dB
G_{AR}	Absolute Gain at 420Hz (back channel - narrow band) (0dB programmed)		0.5	–	+ 0.5	dB
G_{RR}	Gain Relative to Gain at 420Hz (0dB programmed)	< 150Hz 380Hz 400Hz to 440Hz 460Hz 1100Hz to 10000Hz > 10000Hz	– – – 0.5 – – –	– – – – – –	– 50 + 0.5 + 0.5 + 0.5 – 50 – 60	dB dB dB dB dB dB
G_{AR}	Absolute Gain at 425Hz (tone detection or back channel wide band) (0dB programmed)		– 0.5	–	+ 0.5	dB
G_{RR}	Gain Relative to Gain at 425Hz (0dB programmed)	< 112Hz 275Hz 300Hz to 525Hz 575Hz 1375Hz to 10000Hz > 10000Hz	– – – 0.5 – – –	– – – – – –	– 50 + 0.5 + 0.5 + 0.5 – 50 – 60	dB dB dB dB dB dB
	Psophometric Noise		–	–	300	µV
RECEIVE TRANSFER - GENERAL CHARACTERISTICS						
	Absolute Filter Gain for : 0dB programmed 6dB programmed 12dBprogrammed		 – 0.5 + 5.5 + 11.5	 – – –	 + 0.5 + 6.5 12.5	dB
R_{DS}	Signal Detection Level Relative to Programmed Value		– 0.5	–	+ 0.5	dB
R_{HY}	Hysteresis Value		– 2	–	–	dB
	Signal Level (loop 3) at Reception Input		– 40	– 35	– 33	dBm
LINE MONITORING - GENERAL CHARACTERISTICS (load conditions : R_L = 10kΩ, C_L = 50pF)						
A_{TT}	Absolute Gain for 0dB Programmed		–	0	–	dB
R_{AT} -	Attenuation Relative to Programmed Value Attenuation for Programmed Value		– 1 70	– –	+ 1	dB dB
FS	Buzzer Signalling Frequency		–	2982	–	Hz
	Signalling Frequency Amplitude at 0.42V_{PP} Programmed		0.38	0.42	0.46	V_{PP}

7514-08.TBL

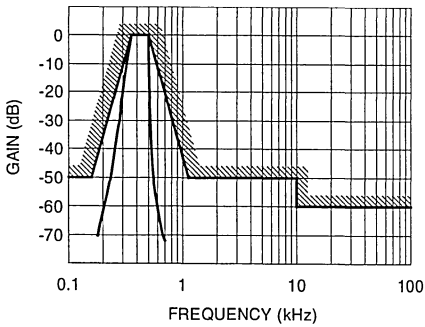
Receive Filter Transfer Characteristics

Figure 7a : Main Channel



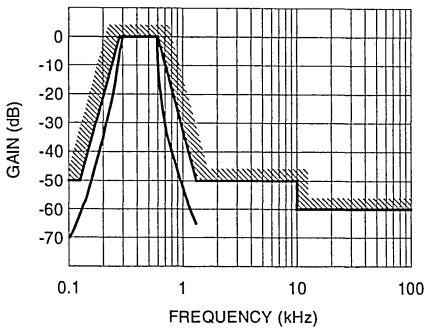
7514-09A EPS

Figure 7b : Back Channel - Narrow Band



7514-09B EPS

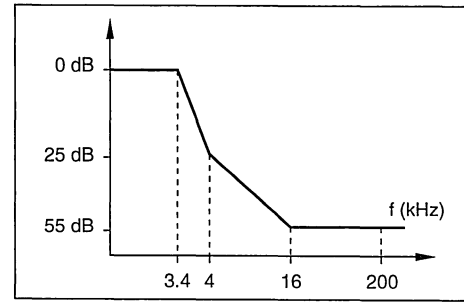
Figure 7c : Basic Channel
Wide band and Tone Detection



7514-09C EPS

Transmission Spectrum

At the ATO output, the out-of-band signal power conforms to the following specifications :



7514-10.AI

Receiver

Measurement conditions
Local transmit level : -10dBm on lower channel at 75bps.
Receive level : -25dBm, with 511 bit pseudo-random test pattern.

Test equipment : TRT sematest.

Isochronous distortion

The following table shows typical isochronous distortion obtained with the TS7514 circuit :

Line	Reception (1200)	Reception (75)
Line 1 (fiat)	10 %	4 %
Line 2	12 %	4 %
Line 3	18 %	6 %
Line 4	14 %	6 %

Bit error rate

Typical bit error rates versus while noise are as follows (noise and signal levels are measured without weighting on the 300/3400Hz) :

	Reception (1200)		Reception (75)	
	S/N	BER	S/N	BER
Line 1	6 dB	2.10^{-3}	– 3 dB	2.10^{-3}
Line 2	7 dB	2.10^{-3}	– 3 dB	2.10^{-3}
Line 3	8 dB	2.10^{-3}	– 3 dB	2.10^{-3}
Line 4	7 dB	2.10^{-3}	– 3 dB	2.10^{-3}

CHARACTERISTICS OF TEST LINES

Figure 8

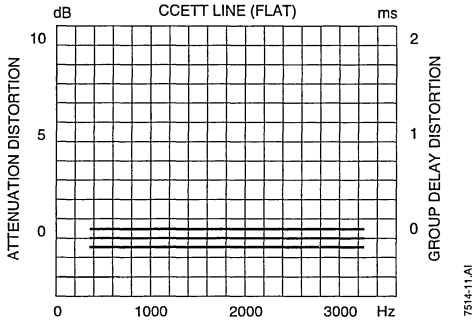


Figure 9

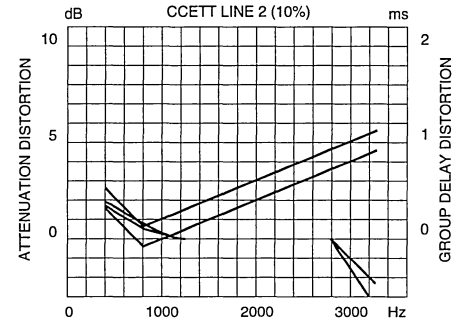


Figure 10

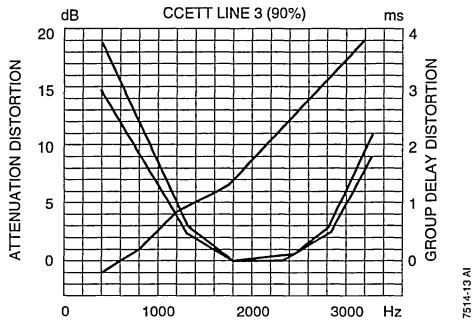
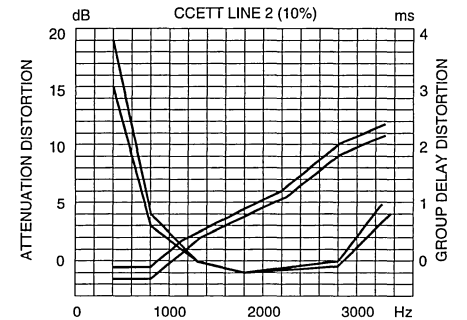
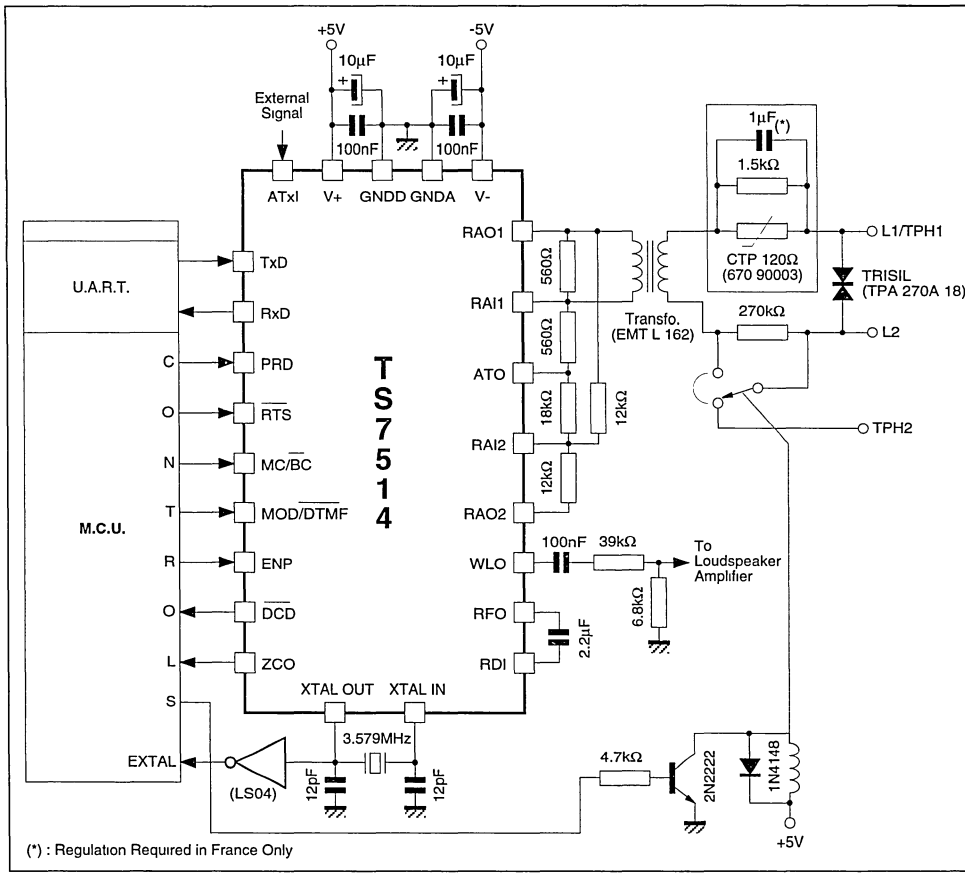


Figure 11



TYPICAL APPLICATION INFORMATION



POWER SUPPLIES DECOUPLING AND LAYOUT CONSIDERATIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performances of the TS7514 operating in close proximity to digital systems, supply and ground noise should be minimized.

This involves attention to power supply design and circuit board layout.

The Power supplies should be bypassed with tantalum or electrolytic capacitors to obtain noise free operation. These capacitors should be located close to the TS7514. The electrolytic type capacitors for improved high frequency performance.

Power supplies connections should be short and direct. Ground loops should be avoided.

SGS-THOMSON MICROELECTRONICS

TS7515

SINGLE CHIP DPSK AND FSK MODEM

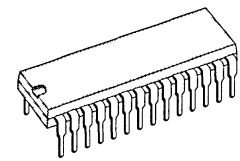
- MONOLITHIC DEVICE (INCLUDES BOTH TRANSMIT AND RECEIVE FILTERS)
- MIXING ANALOG AND DIGITAL TECHNICS
- STANDARD LOW COST CRYSTAL (4.9152MHz)
- AVAILABLE CLOCK FOR MICROPROCESSOR AT 4.9152MHz
- LOW POWER DISSIPATION (CMOS technology)
- SHARP ADJACENT CHANNEL REJECTION
- FIXED COMPROMIZE EQUALIZATION IN TRANSMITTER AND RECEIVER
- TEST LOOPS (local analog, local digital and remote digital loopbacks)
- CARRIER DETECTION OUTPUT
- CCITT AND BELL SIGNALING TONE
- 1200BPS AND 600BPS BIT SYNCHRONOUS FORMAT IN DPSK
- 1200BPS AND 600BPS +1%, -2.5% OR +2.3%, -2.5% CHARACTER ASYNCHRONOUS FORMAT (8, 9, 10 or 11 bits) IN DPSK
- 0 TO 300BPS IN FSK
- AUTOMATIC DIAL LINE MONITORING CAPABILITY
- BREAK SIGNAL SUPERVISION
- EXTERNAL VOICE BAND TONE FILTERING AVAILABLE (i.e. 550Hz or DTMF)
- CMOS AND TTL COMPATIBLE
- DIRECT INTERFACE TO STANDARD MICROPROCESSOR FAMILIES

DESCRIPTION

The TS7515 is a single chip DPSK and FSK voiceband modem, compatible with the BELL 103, 212A and CCITT V.22 A/B recommended standards.

MAIN OPERATING MODES

- Standard selection (Bell 212A/Bell 103/V.22)
- Answer tone selection (2100 or 2225Hz)
- Low speed mode selection
- Channel selection (answer/originate)
- Synchronous/asynchronous mode selection
- 8 bits to 11 bits word length selection in character asynchronous format mode
- Overspeed selection in character asynchronous format mode
- Scrambler selection
- 1800Hz guard tone selection in V.22
- Test loop selection (Digital/Analog)



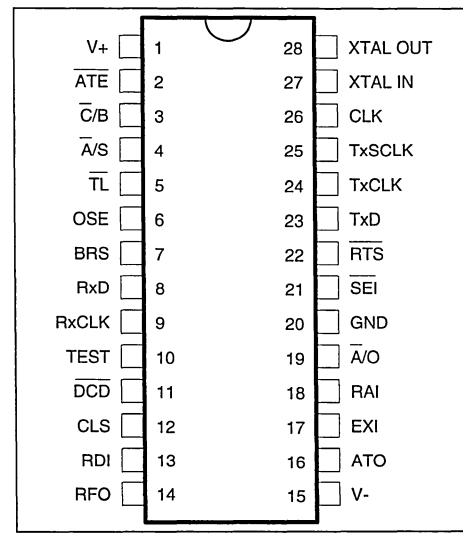
DIP28
(Plastic Package)

ORDERING INFORMATION

Part Number	Temperature Range	Package
TS7515CP	0 to +70°C	DIP28
TS7515IP	-25 to +85°C	DIP28

7515-01 TBL

PIN CONNECTIONS



7515-01 EPS

PIN DESCRIPTION

Name	Pin Type	N°	Function	Description
COMMON SECTION (supply, clock, handshaking and mode selection)				
V^+	I	1	Positive Power Supply	+5V
V^-	I	15	Negative Power Supply	-5V
GND	I	20	Ground	0V
XIN	I	27	Oscillator Input	This pin corresponds to the input of the oscillator. It is normally connected to an external crystal but may also be connected to a pulse generator. The nominal frequency of the oscillator is 4.9152MHz.
XOUT	O	28	Oscillator Output	This pin corresponds to the output of an inverter with sufficient loop gain to start and maintain the crystal oscillating.
CLK	O	26	Clock	This pin delivers a clock signal, the frequency of which is the crystal frequency. It may be used as a buffered clock a microcontroller.
$\overline{C}$/B	I	3	CCITT/BELL Selection	This three-state input selects the features corresponding to CCITT or BELL recommandation.
$\overline{A}$/S	I	4	Synchronous/ Asynchronous Selection	This three-state input selects the synchronous bit format or the asynchronous character format mode in DPSK transmission. This input allows also character length selection (refer to table 8).
CLS	I	12	Character Length	This input selects the character length in conjunction with $\overline{A}$/S input (refer to table 8).
OSE	I	6	Over-speed Selection	This input selects the over-speed in asynchronous character format mode required by CCITT recommandation (refer to table 8).
BRS	I	7	Binary Rate Selection	A Logic "0" on this input turns chip on1200 bps rate. A logic "1" turns the chip on 600bps or 0-300bps according to C/B selection.
$\overline{A}$/O	I	19	Answer/Orig. Selection	A logic "0" on this input turns the chip on answer mode. A logic "1" turns the chip on originate mode.
$\overline{TL}$	I	5	Test Loop Selection	This three-state input, selects the test loops mode (refer to table 6).
TRANSMIT SECTION				
TxD	I	23	Transmit Data	Data bits to be transmitted are serially presented on this input. A mark corresponds to a logic "1" and a space to a logic "0". This data determines which phase or frequency appears at any instant at the ATO pin in DPSK or FSK modes.
ATO	O	16	Analog Transmit Output	The analog output is the modulated carrier or the answer tone to be conditionned and sent over the phone line mixed with the filtered signal from EXI.
EXI	I	17	External Tone Input	This analog input allows external tone to be filtered by an internal low-pass filter. Filtered signal appears at ATO whatever RTS.
$\overline{ATE}$	I	2	Answer Tone Enable	A logic "0" on this input instructs the chip to enter answer signaling tone mode according C/B selection. A logic "1" turns the chip on transmit data mode (refer to table 9).
$\overline{SEI}$	I	21	Scrambler Enable Input	A logic "0" on this input enables the internal scrambler. A logic "1" instructs the chip to bypass the scrambler.
TxCLK	O	24	Transmit Clock from Modem	This output delivers a transmit bit clock generated by chip in synchronous mode. When TxSCLK is used, TxCLK is locked on TxSCLK. This output generates a logic "1" in asynchronous mode.
TxSCLK	I	25	Transmit Clock from Terminal	This input receives a bit clock supplied by the DTE. This clock synchronizes the internal transmit clock of the chip. In line monitoring mode this input receives the filters clock.
$\overline{RTS}$	I	22	Request to Send Terminal	When a logic "0" is present on this input, the chip delivers on ATO a modulated signal or a signaling tone and the filtered signal from EXI. When a logic "1" is present on this input, ATO delivers only the filtered signal from EXI. When a logic "-1" is present on this input, the receive section may be used for line monitoring and ATO delivers only the filtered signal from EXI.

7515-02 TBL

PIN DESCRIPTION (continued)

Name	Pin Type	N°	Function	Description
RECEIVE SECTION				
RAI	I	18	Receive Analog Input	This input receives the analog signal from the hybrid. It corresponds to the input of the receive filters.
RFO	O	14	Receive Filter Output	This analog output is the signal received on RAI once filtered. The receive filter also equalizes the signal for adaptation to most existing lines. This output must be connected to RDI through a capacitor to meet the level detection conditions.
RDI	I	13	Receive Demodulator Input	This pin is the input of the carrier detection logic and of the demodulator
$\overline{DCD}$	O	11	Data Carrier Detect	A logic "0" on this output indicates that a valid carrier signal is present on RAI. A logic "1" means that no valid signal is being received. The hysteresis meet standards recommendation.
RxD	O	8	Receive Data	Data bits demodulated are available serially at this output.
RxCLK	O	9	Receive Clock	This output delivers a receive bit clock generated by the chip. In asynchronous mode this clock is 16 times the modulation rate. In synchronous mode the clock is equal to the bit rate.
TEST	O	10	Test	This output is an intermediate demodulator output intended for handshake and test purposes.

7515-03.TBL

The TS7515 is a general purpose monolithic DPSK and FSK modem implemented with double poly CMOS process.

It is capable of generating and receiving phase modulated signals at data rates of 1200bps or 600bps as well as frequency modulated signals at data rates up to 300bps on voice-grade telephone lines.

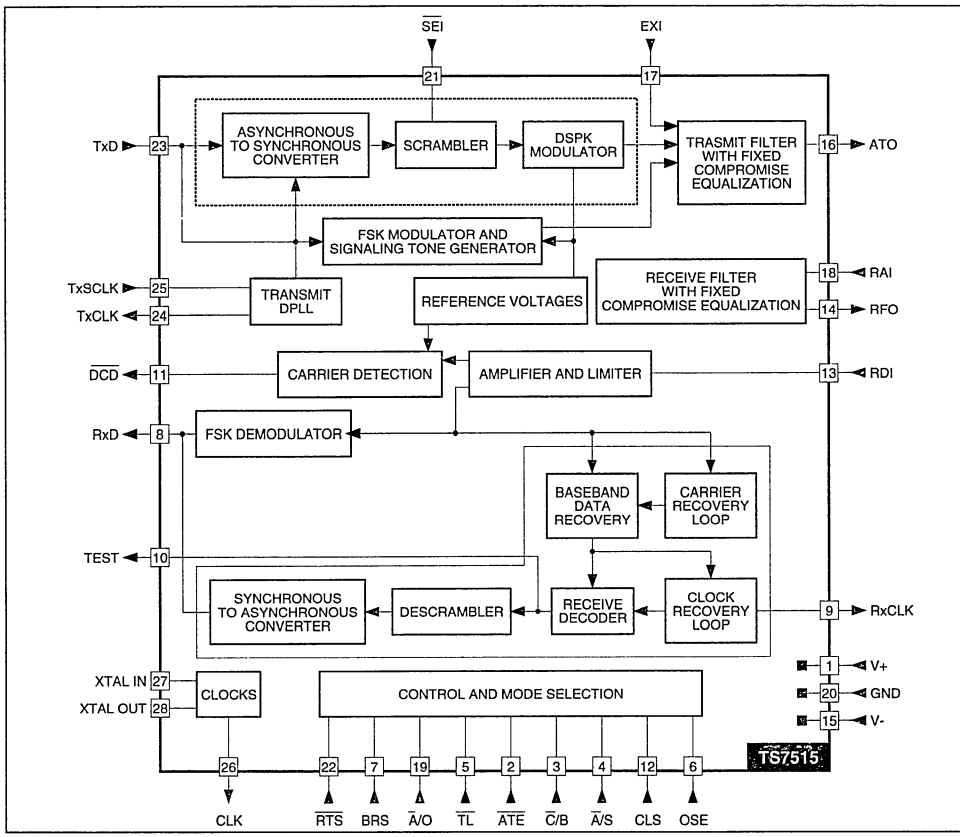
It is offered in a 28 or 44 in plastic package and is able to operate in full-duplex mode according to three pin selectable standards :
- CCITT V.22 A-B
- Bell 212A with its low speed mode
- Bell 103

All filtering functions required for frequency generation, out-of-band noise rejection and demodulation are performed by on-chip switched capacitor filters.

In phase modulation the modem provides all data buffering and scrambling functions necessary for bit synchronous format and asynchronous character format modes of operation.

Internal frequencies are generated from a 4.9152MHz crystal reference.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V^+	Supply Voltage	+7	V
V^-	Supply Voltage	-7	V
V_{in}	Analog Input	$V^- < V_{in} < V^+$	V
V_I	Digital Input (except three-state inputs)	$GND < V_I < V^+$	V
V_{i3}	Three-state Input	$V^- < V_{i3} < V^+$	V
T_{amb}	Operating Temperature	0 to 70	°C
T_{stg}	Storage Temperature	-55, 125	°C
T_S	Pin Temperature (soldering, 10s)	260	°C

7515-04.TBL

Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

ELECTRICAL OPERATING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Supply Voltage	4.75	5	5.25	V
V^-	Negative Supply Voltage	-5.25	-5	-4.75	V
I^+	V^+ Operating Current	–	10	30	mA
I^-	V^- Operating Current	-20	-7	–	mA

7515-05 TBL

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V^+ = +5V \pm 5\%$, $V^- = -5V \pm 5\%$, GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit
DIGITAL INTERFACE					
I_L	Input Current (V_{IL}min < V_I < V_{IH} max)	-50	–	50	µA
I_{OL}	Output Low Level Current (V_{OL} = 0.4V)	800	–	–	µA
I_{OH}	Output High Level Current (V_{OH} = 2.4V)	–	–	-40	µA
V_{IL}	Input Low Voltage	GND	–	0.8	V
V_{IH}	Input High Voltage	2	–	V^+	V
V_{in}	Input Negative Voltage	V^-	–	-4	V
ANALOG INTERFACE, FILTERS INPUTS AND OUTPUTS (RAI-RFO, EXI-ATO)					
I_L	Input leakage Current (– 3V < V_{IN} < + 3V)	-10	–	10	µA
R_I	Input Resistance		3	–	MΩ
V_{IN}	Input Voltage Swing	-3	–	+3	V
V_{OF}	Output Offset Voltage	-500	–	+ 500	mV
V_{OS}	Output Voltage Swing (R_L > 10kΩ)	-2	–	+2	V
O_L	Load Capacitance	–	–	20	pF
R_L	Load Resistance	10	–		kΩ
D	Signal Distortion		-40		dB
ANALOG INTERFACE, TRANSMIT OUTPUT (ATO) EXI CONNECTED TO GND					
V_{OF}	Output Offset Voltage	-500	–	+ 500	mV
V_O	Output Voltage Swing (R_L/10kΩ, C_L = 20pF) - Carriers - Guard Tone 1800Hz/Data Signal	 -7	 2.2 -6	 -5	 V_{pp} dB
A_T	$\overline{RTS}$ Attenuation	55	–	–	dB
ANALOG INTERFACE, RECEIVE DEMODULATOR INPUT (RDI)					
Clink **	Serial Capacitor from RFO	+1	1	–	µF
NI	Maximum Detection Level to Valid $\overline{DCD}$ Output	–	–	5.5	mV_{RMS}
N2	minimum Detection Level to Valid $\overline{DCD}$ Output	3.1	–	–	mV_{RMS}
N1/N2	Hysteresis Effect	2	–	5	dB

7515-06 TBL

* Typical values are for T_{amb} = 25°C and nominal power supply values.
* * This capacitor must be unpolarized type capacitor

DYNAMIC CHARACTERISTICS

RECEIVE FILTER TRANSFER CHARACTERISTICS IN DSPK

Symbol	Parameter		Min.	Typ. *	Max.	Unit
Low Channel						
GA	Absolute Passband Gain at :	1200Hz	–	+9.5	–	dB
GR	Relative Gain to GA at :	600Hz	–	-45	–	dB
		900Hz	–	-0.5	–	dB
		1500Hz	–	+0.8	–	dB
		1800Hz	–	-50	–	dB
		2400Hz	–	-65	–	dB
High Channel						
GA	Absolute Passband Gain at :	2400Hz	–	+9.5	–	dB
GR	Relative Gain to GA at :	2100Hz		-0.2		dB
		2700Hz	–	+0.7	–	dB
		1800Hz	–	-25	–	dB
		1200Hz	–	-68	–	dB

7515-07 TBL

RECEIVE FILTER TRANSFER CHARACTERISTICS IN FSK

In FSK the receive filter is the same as in DSPK but the sampling frequency is multiplied be a 14/15 ratio (i.e. 2400Hz in DSPK becomes 2240Hz in FSK).

Symbol	Parameter		Min.	Typ. *	Max.	Unit
Low Channel						
GA	Absolute Passband Gain at :	1120Hz	–	9.5	–	dB
High Channel						
GA	Absolute Passband Gain at :	2240Hz	–	9.5	–	dB

7515-08 TBL

* Typical values are for T_{amb} = 25°C and nominal power supply values.

DEVICE OPERATION

Transmitter

The transmitter consists of two analog signal generators followed by switched capacitor and continuous filters. In phase modulation operation mode the DPSK signal generator is preceded by a selectable scrambler and an asynchronous to synchronous converter is included in character asynchronous format mode.

Tone allocation : the modem on the end of the line which initiates the call is called the originate modem. In normal transmission operation it transmits in low channel and receives in high channel. The other modem is the answer modem which transmits in high channel and receives in low channel.

Modulators

DPSK modulator : the phase modulation type is differential quadrature four phase shift keying (see Table 1). The 1200bps data stream to be transmitted is converted into two 300 dibits per second streams which modulate alternatively two independant carriers. Consequently the base band shaping is included is a 5-bit address ROM which generates samples for a 8-bit switched capacitor DAC at a frequency equals to 8 times the carrier frequency.

Table 1 : DPSK Modulation

BRS	TxD		Phase Shift
	n – 1	n	
0	0	0	+90 °
		1	0 °
	1	1	+270 °
		0	+180 °
1	X *	0	+90 °
		1	+270 °

* x : don't care.

FKS modulator and tone generator : a frequency synthesizer provides accurate clocks to a switched capacitor sine wave generator (see Table 2). Phase continuity is maintained when a frequency shift occurs.

Table 2 : FSK Modulation (BELL 103)

$\overline{A}$/0	TxD	Standard Frequency
0	0	2025Hz
	1	2225Hz
1	0	1070Hz
	1	1270Hz

Transmit Filters

To avoid unwanted frequency components to be echoed by the hybrid in the reception path, to maintain the level of spurious out-of-band signals transmitted to the telephone line below the limits specified by administrations (see figure 1) and to complete statistical amplitude and phase equalization, the analog signals are processed by ten poles sharp pass-band switched capacitor filters. The response of these filters depends on the selected channel (Answer/Originate) and the selected standard (BELL 212 - V.22 BELL 103). A continuous filter eliminates parasitic sampling effects. An additional low-pass filter input is provided. This allows to mix and filter such tones as DTMF signals or special guard tones (550Hz) to the transmitted signal.

Scrambler

The scrambler used during phase modulation ensures the transmission of a continuously changing pattern. This avoids the receiving modem to drop out of lock on certain continuous repetitious data patterns.

This scrambler may be disabled during handshaking procedures. In V.22 a special unlocking sequence is performed on 64 spaces pattern at scrambler output.

Asynchronous To Synchronous Converter

The DPSK signal is synchronous in nature but the modem has both an asynchronous as well as a synchronous mode of operation in DPSK. So a data buffer is necessary to convert variable rate asynchronous character data to an equivalent bit oriented synchronous data stream. This is done by inserting or deleting stop bits. If serial input data contains a break signal through one character (including start and stop bits). One break will be extended to at least 2 * M + 3 bits long (where N is the number of transmitted bit/character).

Figure 1 : Transmitted Signal Template

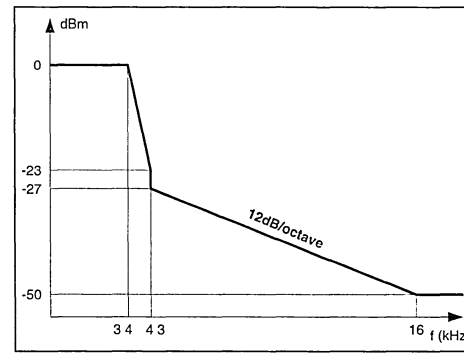


Table 3 : Output Frequency Deviation

Standard Frequency	Frequency Using 4.91MHz	% Deviation from Standard	Mode
1070Hz	1066.7Hz	-0.3%	BELL 103 Originate
1200Hz	1200Hz		BELL 212A or V22, Originate
1270Hz	1269.4Hz	-0.05%	BELL 103 Originate
1800Hz	1807.4Hz	+0.4%	Guard Tone V.22
2025Hz	2021Hz	-0.2%	BELL 103 Answer
2100Hz	2104.1Hz	+0.2%	Answer Tone CCITT
2225Hz	2226.1Hz	+0.05%	BELL 103 Answer or Answer Tone BELL
2400Hz	2400Hz		BELL 212A or V.22, Answer

RECEIVER

The receiver includes two band-pass filters followed by an amplifier and a hard limiter. Depending on selected standard, the detector output is passed through a DPSK demodulator or a FSK demodulator. The DPSK demodulator is followed by a descrambler and a selectable synchronous to asynchronous converter. In addition a carrier detector monitors the level of the received signal.
Tone allocation : in normal transmission operation the originate modem receives in high channel and transmits in low channel. The answer modem receives in low channel and transmits in high channel.

Receive Filters

The signal delivered by the hybrid to the receive analog input is a mixture of transmitted signal, received signal and noise with a level in the range from -48dBm to -0dBm. Depending on the operating mode and the selected standard the 20 poles receive switched capacitor band-pass filter selects the frequency band of the low channel or the high channel. A ratio of 14/15 is applied on the sampling clock frequency between FSK and DPSK in the same operating mode (Answer/Originate). These filter reject out-of-band transmission noise components and undesirable adjacent channel echo signals which can be fed from the transmit section into the receive section. Fixed equalization is included in order to assure low error rate.

Amplifier And Hard Limiter

Once filtered the received signal is amplified and fed to the carrier detector. In order to limit analog parts in the design all the demodulator techniques used in the TS7515 are based on zero crossing detection. So the received signal is just limited before entering demodulator.

Demodulators

DPSK demodulator : a DPLL is used to recover the carrier signal. This DPLL has a lock range of ±2Hz but as the incoming carrier may present an offset of ±7Hz a second loop allows the first DPLL to lock on the exact frequency of the carrier with an accuracy of ±1Hz and to follow its slow variations in 1200 bands mode only. Then the limited received signal is mixed through exclusive-Or with the recovered carrier and with the 90 degrees phase shifted recovered carrier. The results are processed through four poles Bessel filters wich provide a good amplitude propagation time compromise. The received sampling clock recovered from these base and data with a simple DPLL. The received data are sampled by this clock and then converted into a serial synchronous bit stream.

FSK demodulator : the zero crossing detector output is passed through a shift register whose length depends on the operating mode (Answer/Originate). The output of the shift register and the detector are mixed into an exlusive Or. Then they are processed through a four poles Bessel filter and a slicer.

Test Output

Once demodulated DPSK data are generally processed (cf next paragraph) but during call set-up procedures or data set testing it is of importante to monitor the demodulator output. So in DPSK mode demodulated data are available on TEST pin.

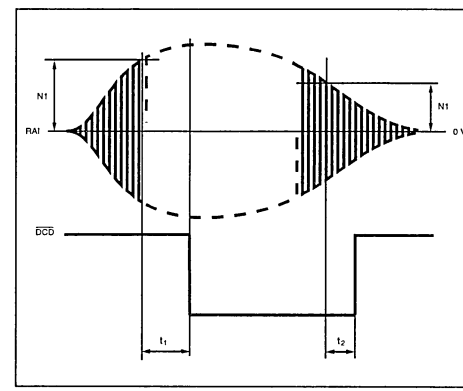
Descrambler and Synchronous to Asynchronous Converter

Data coming from the DPSK demodulator are unscrambled. In V.22 the unlocking sequence is detected at descrambler input and the original data are decoded before descrambling. In asynchronous character format mode of operation a data buffer is able to detect missing stop bits and reinsert them. The converter is able to recognize the break signal and transmits it without modification.

Carrier Detector

Whenever valid signals are being received at the input of the demodulator and are acceptable for demodulation, carrier detect output is pulled down. A delay is timed out before the carrier received or carrier lost signal changes carrier detect output to provide immunity against noise bursts. The modem also provides at least 2dB of hysteresis between the carrier ON and the carrier OFF thresholds (see Figure 2).

Figure 2



In DPSK mode $105ms \leq t_1 \leq 205ms$ $10ms \leq t_2 \leq 24ms$
In FSK mode $105ms \leq t_1 \leq 205ms$ $25ms \leq t_2 \leq 75ms$

LOOP TEST

Loop 3

This loop is called the analog loop. When it is selected the receive filters and the modulators are configured to process the same channel as the transmit section. The transmit carrier has to be looped back externally to the receive analog input. This loop allows the user or the DTE to check the satisfactory working of the local DCE.

Loop 2

This loop is called the digital loop. When it is selected received data, receive clock and data carrier detect signals are respectively and internally looped back on transmit data, transmit clock from terminal and request to send . This loop allows the user or the DTE to check the satisfactory working of the line and the remote DCE.

Clocks

In synchronous mode of operation TxCLK, TxSCLK and RxCLK are respectively working as the V.24 circuits C114, C13 and C15. In asynchronous mode of operation RxCLK can be used as baud rate clock to synchronize the transmit and the receive sections of a UART (see table 4).

Oscillator Output

The buffered master clock (4.9152MHz) is made available at output CLK. It can be used as a clock for a microcontroller.

Voltage Reference

A temperature compensated voltage reference build with a zener is included in the chip. This vol-tage is used to calibrate transmit levels and to generate the carrier detection thresholds.

LINE MONITORING

A special mode has been included in the TS7515 to monitor the line during an automatic call. When this mode is selected (A/S = 0, RTS = -1) receive filters clock is directly derived from TxSCLK which allows the user to precisely observe broad frequency bands. Furthermore the DCD performs a fast carrier detection equivalent to an envelope detection. As the center frequency of the receive filters is proportional to TxSCLK frequency in this mode it is possible to tune the passband according to the frequency to be detected (see Table 5).

TxSCLK : must be created from the TS7515 master clock (4.9152MHz).

Table 4 : Clock Operation

A/S	C/B	BRS	TxCLK	RxCLK	Mode
-1 or 0	-1 or 0	0	1	19.2kHz	V.22 Asynchronous
		1	1	9.6kHz	
	1	0	1	19.2kHz	BELL 212A Asynchronous and BELL 103
		1	1	4.8kHz	
1	-1 or 0	0	1200Hz	1200Hz	V.22 Synchronous
		1	600Hz	600Hz	
	1	0	1200Hz	1200Hz	BELL 212A Synchronous and BELL 103
		1	1	4.8kHz	

Table 5

TxSCLK	Originate (A/O = 1)		Answer (A/O = 0)		Application
	Center Frequency	Passband at 3dB	Center Frequency	Passband at 3dB	
210kHz	2400Hz	±400Hz	1200Hz	±400Hz	Voice Detection
45kHz	510Hz	±85Hz			440Hz Detection
			260Hz	±85Hz	330Hz Detection
76.8kHz			440Hz	±150Hz	Dial Tone and Busy Tone Detection

APPLICATION INFORMATION

In a typical application a microcontroller provides control and interface to the Data Terminal Equipment (DTE), and a Direct Access Arrangement provides connection to the telephone line. Then the TS7515 can communicate with the most popular modems (BELL 103 and BELL 212A) in countries under BELL standards and popular modems (V.22) in countries under CCITT recommendations.

Power Supplies Decoupling and Layout Considerations

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performances of the TS7515 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout.

The power supplies should be bypassed with tantalum or electrolytic capacitors to obtain noise free operation. These capacitors should be located close to the TS7515. The electrolytic type capacitors should be bypassed with ceramic capacitors for improved high frequency performance.
Power supplies connections should be short and direct. Ground loops should be avoided.
Coupling between analog inputs and digital lines should be minimized by careful layout. The RDI input (Pin 13) is extremely sensitive to noise.
The connection between this point and RFO (Pin 14) through a ceramic type capacitor should be as short as possible and coupling between this connection and digital signals should be minimized by careful layout.

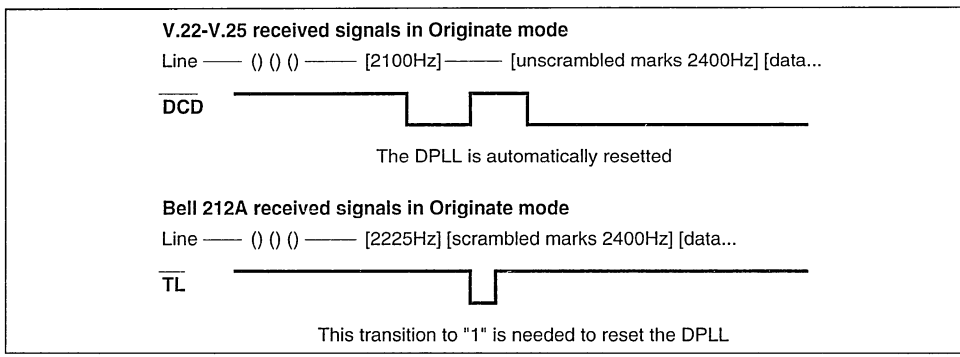
Carrier Recovery Loop

The carrier recovery loop utilizes a digital phase lock loop. Performances of the TS7515 depend directly on this DPLL which needs to be resetted before receiving a DPSK carrier.

Three ways of resetting the DPLL exist on the TS7515 :
- A trailing edge on $\overline{DCD}$.
- Changing FSK mode to DPSK mode or reversely.
- Changing receive channel.

These three ways of resetting the DPLL should be used in the software included in the microcontroller to perform the various set-up procedures and handshakes.

Figure 3 : Examples



TYPICAL PERFORMANCES

The typical performances listed below are achieved with the environment described in the previous paragraph.

- Dynamic range : 0dBm to - 45dBm.
- BER performances :

Conditions : Xmit level = - 10dBm,
Rec level = - 25dBm,
Message 511 bits on CCETT lines 1, 2, 3, 4 and CNET lines QN and 3 VHF and US lines C4, C2, and C0.

1200 bps operation
- BER 10^{-3} for a 7 dB SNR
- BER 10^{-6} for a 11 dB SNR

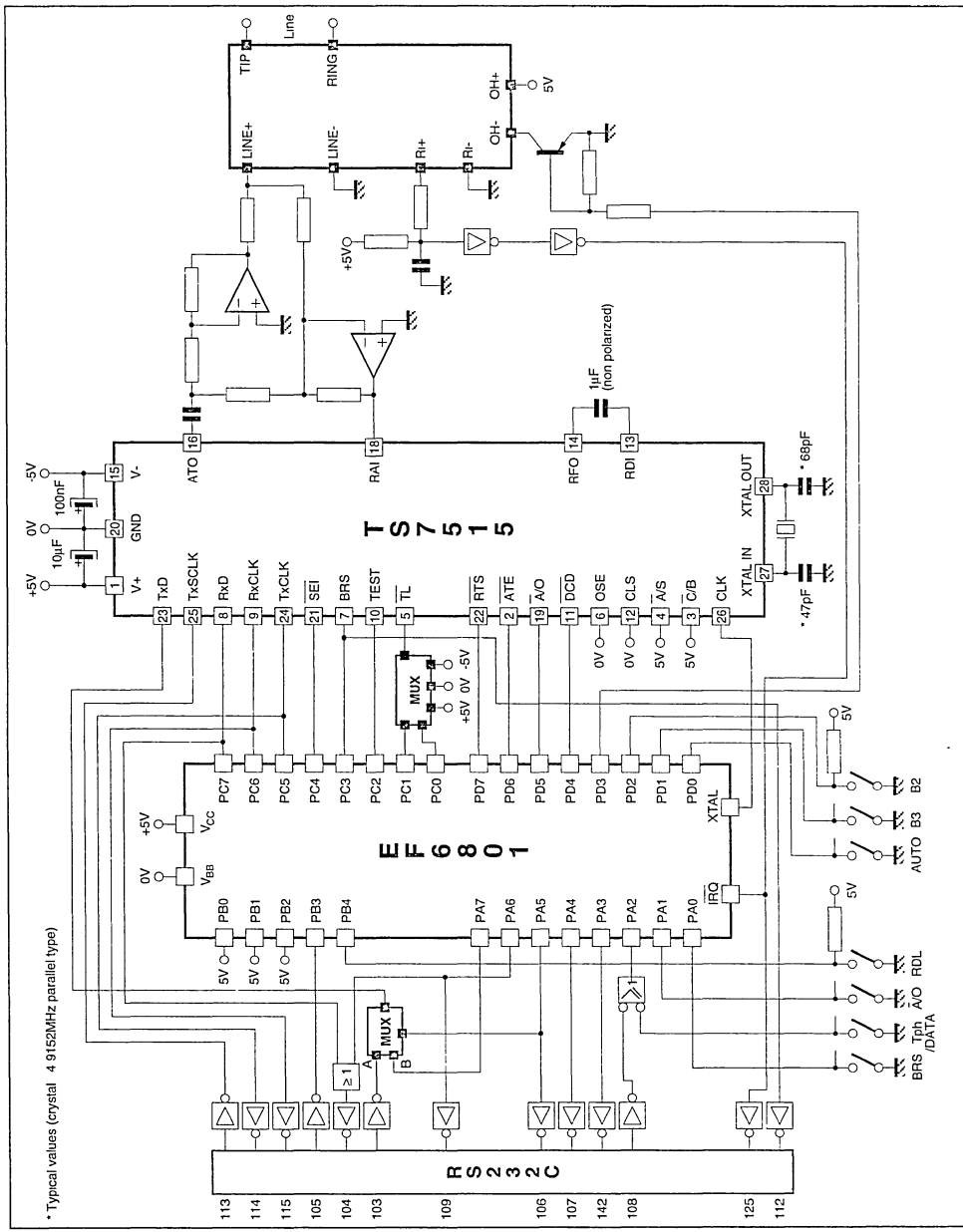
300 bps operation
- BER 10^{-3} for a 3 dB SNR
- BER 10^{-6} for a 8 dB SNR

- Specific DPSK performances

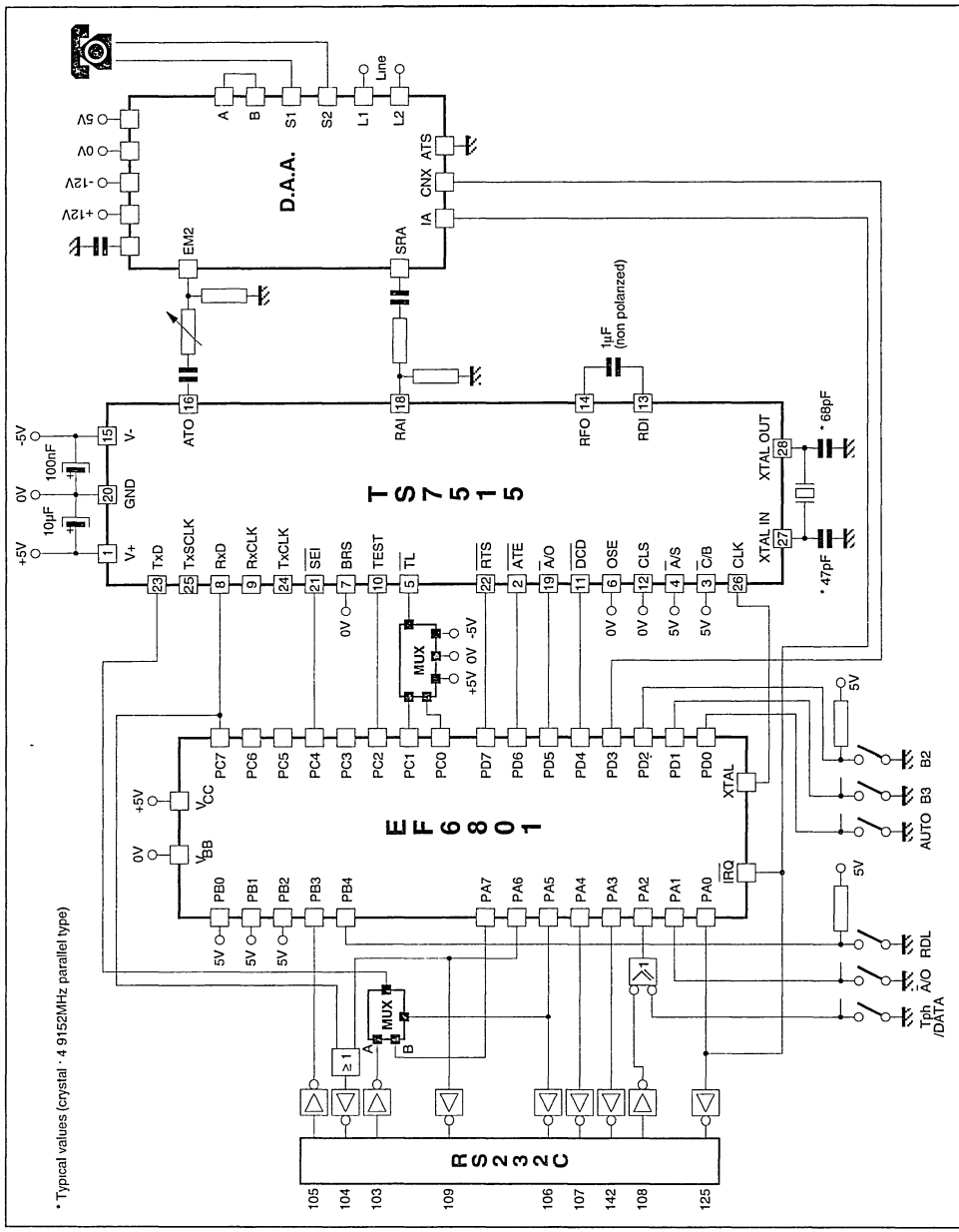
Phase hits sensitivity	:	25 degree	BER $< 10^{-6}$
Phase Jitter	:	35 degree	
Amplitude hits sensitivity	:	± 10dB	
Offset carrier sensitivity	:	SNR increase < +1dB	
1800Hz guard tone sensitivity	:	SNR increase < +2dB	

- Specific FSK performances
  Bias Distortion : less than 5 %
  Jitter : less than 12 %

BELL 212A APPLICATION (synchronous)



V.22 (asynchronous, 10 bits, 1200bps)



SELECTION MODE TABLES

SYNTHESIS OF DIFFERENT MODES FOR RECEIVE SECTION

Table 6

$\overline{C/B}$	BRS	$\overline{TL}$	$\overline{A/0}$	Receive	Mode
-1 ou 0	X	-1	0	DPSK Originate Loop 3	V.22
			1	DPSK Answer Loop 3	
		0	0	DPSK Answer Loop 2	
			1	DPSK Originate Loop 2	
		1	0	DPSK Answer	
			1	DPSK Originate	
1	0	-1	0	DPSK Originate Loop 3	BELL 212 A including BELL 103
			1	DPSK Answer Loop 3	
		0	0	DPSK Answer Loop 2	
			1	DPSK Originate Loop 2	
		1	0	DPSK Answer	
			1	DPSK Originate	
	1	-1	0	FSK Originate Loop 3	
			1	FSK Answer Loop 3	
		0	0	FSK Answer Loop 2	
			1	FSK Originate Loop 2	
		1	0	FSK Answer	
			1	FSK Originate	

7515-09 TBL

Answer : Receive in low channel
Onginate : Receive in high channel
Loop 3 : Analog loop
Loop 2 : Digital loop

SYNTHESIS OF DIFFERENT MODES FOR TRANSMIT SECTION

Table 7

$\overline{ATE}$	$\overline{C/B}$	BRS	$\overline{A/0}$	Transmit	Mode
0	– 1 or 0	X	X	2100Hz	Answer Tone
	1			2225Hz	
1	– 1	0	0	DPSK 1200bps Answer	V.22 without Guard Tone
			1	DPSK 1200bps Originate	
		1	0	DPSK 600bps Answer	
			1	DPSK 600bps Originate	
	0	0	0	DPSK 1200bps Answer	V.22 with 1800Hz Guard Tone
			1	DPSK 1200bps Originate	
		1	0	DPSK 600bps Answer	
			1	DPSK 600bps Originate	
	1	0	0	DPSK 1200bps Answer	BELL 212A
			1	DPSK 1200bps Originate	
		1	0	FSK 0-300bps Answer	
			1	FSK 0-300bps Originate	

7515-10 TBL

Answer : Receive in high channel
Originate : Receive in low channel

SELECTION MODE TABLES (continued)

MODE SELECTION IN PHASE MODULATION TRANSMISSION

Table 8

$\overline{A/S}$	CLS	OSE
-1	0	0
		1
	1	0
		1
0	0	0
		1
	1	0
		1
1	0	0

Transmission Mode	Length	Over-speed
Asynchronous	8	+1%, -2.5%
		+2.3%, -2.5%
	11	+1%, -2.5%
		+2.3%, -2.5 %
	9	+1%, -2.5%
		+2.3%, -2.5%
	10	+1%, -2.5%
		+2.3%, -2.5%
Synchronous		

7515-11 TBL

TEST PIN

Table 9

$\overline{ATE}$	$\overline{C/B}$	BRS
0	-1 or 0	0
		1
	1	0
		1
1	-1	0
		1
	0	0
		1
	1	0
		1

Transmit	Receive	Test
2100Hz	V.22 DPSK 600bps	DDO
	V.22 DPSK 1200bps	DDO
2225Hz	BELL 212A DPSK 1200bps	DDO
	BELL 103 FSK 0-300bps	HLO
V.22 without Guard Tone DPSK 1200bps		DDO
V.22 without Guard Tone DPSK 600bps		DDO
V.22 with Guard Tone DPSK 1200bps		DDO
V.22 with Guard Tone DPSK 600bps		DDO
BELL 212A DPSK 1200bps		DDO
BELL 103 FSK 0-300bps		HLO

7515-12 TBL

DDO : DPSK demodulator output
HLO : Hard limiter output

SUMMARY OF THE DIFFERENCES BETWEEN BELL 212A AND V.22 A-B

Table 10

Feature	BELL 212A	V.22
Low Speed Mode	0-300bps FSK	600bps DPSK
Guard Tone	No	1800Hz Optional *
Answer Tone	2225Hz	2100Hz
Character Length is Asynchronous Mode in DPSK	9, 10 bits	8, 9, 10, 11 bits **
Over Speed Mode in Asynchronous Mode in DPSK	No	Yes **
64 Spaces Detection	No	Yes

7515-13 TBL

* 550Hz may be externally generated and added to the transmit signal through EXI.
** Features of V.22 are available in BELL 212A on the chip.
All these differences are taken into consideration inside the TS7515.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

A VERY LOW COST AND POWERFUL SOLUTION FOR V.23 APPLICATION : TS7514

by O.LEENHARDT - R. GIRARD

SUMMARY

1 - INTRODUCTION

The TS7514 is a single chip F.S.K. voiceband modem offering a real low cost powerful solution for all C.C.I.T.T. V.23 recommended standard applications.

Indeed, TS7514 integrates many possibilities and functionalities by requiring only very few external components.

Its Block Diagram is shown Figure 1.

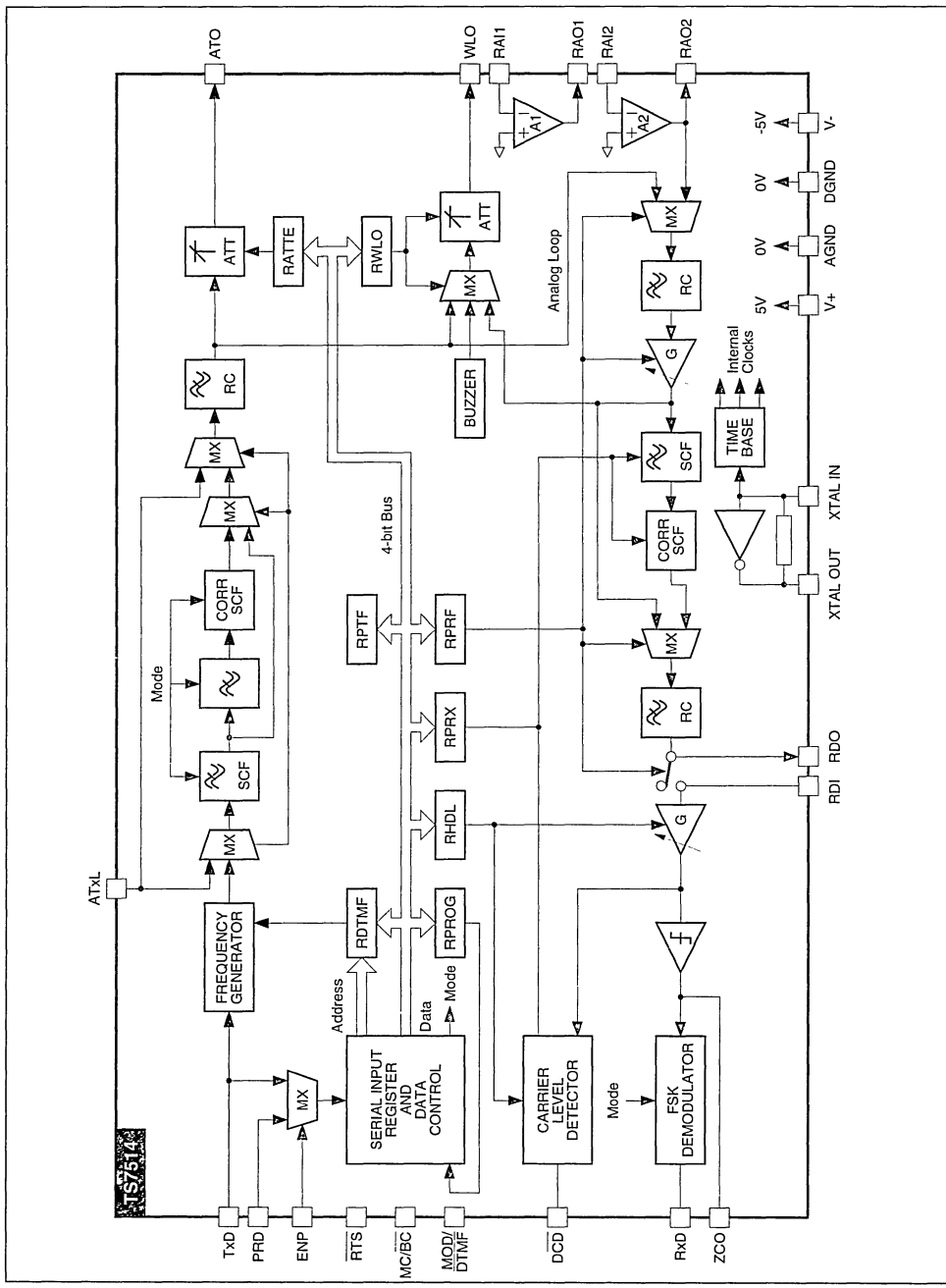
The TS7514 main features are :

PROGRAMMABLE MODES :
- MODEM 75/1200 or 1200/75 bps (full duplex on 2 wire line),
- MODEM 75/75 or 1200/1200 bps (full duplex on 4 wire line),
- D.T.M.F. dialing,
- Analog test loop,
- Tone detection (ring, dialing, ...)

PROGRAMMABLE FUNCTIONS :
- Transmit/receive levels,
- Receive filter gain,
- Hysteresis and detection levels,
- Line monitoring level,
- Signalling frequency (2982Hz) level

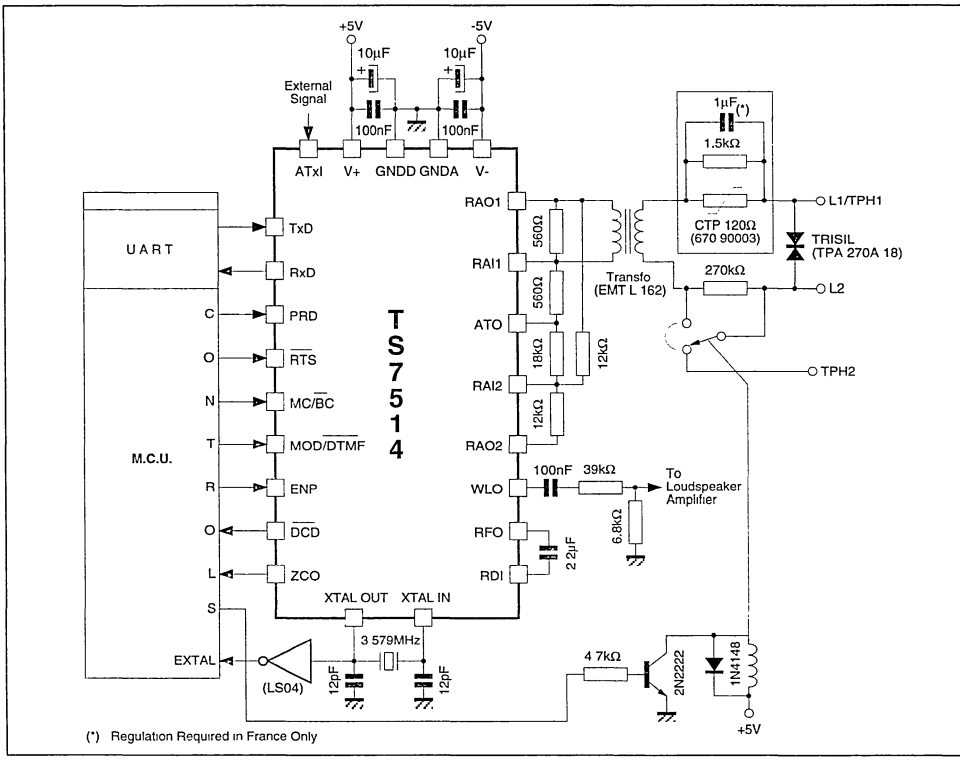
ADDITIONAL FEATURES :
- Integrated duplexer,
- Auxiliary analog signal transmission (voiceband),
- Automatic bias distortion adjustment,
- Tax rejection filter (12 and 16kHz),
- Fixed compromise equalization,
- Standard low cost crystal (3.579MHz),
- C.M.O.S. technology,
- Less than 100mW power dissipation,
- ± 5V supplies,
- 24 pin package.

Figure 1 : Detailed Block Diagram



This Application Note describes some of the TS7514 most important features detailed before from a typical and simplified application scheme shown Figure 2 (more information are given in the following sheets).

Figure 2 : Typical Application Information



2 - PROGRAMMABLE MODE

2.1 - With What to Program ?

The TS7514 contains 8 control registers.
The programming used is serial where data input is TxD or PRD and clock input RTS.

From now, it is important to point out that during programming, the RTS (Request To Send) signal and the TxD (Transmit Data) signal to be transmitted from the local terminal over the telephone line are internally safeguarded in order to not modify the transmission.

- By using TxD either to program or transmit data, only one signal has to be managed. In this case, you must take in care to program the TS7514 out of the transitions between two successive data bits and during a maximum duration equal to a "bit time" (833.3µsec. in 1200 bps) to avoid transmission errors.
- By using PRD to program the TS7514 allows to use TxD only for data to be transmitted and avoids the preceeding cautions but requires the management of these two signals.

The choice will depend on the application (microcontroller used, number of I/O ports, ..)

TxD is selected by ENP = "0" ; PRD by ENP = "1".

2.2 - How to Program ?

The programming is indirect via an 8 bit shift register, called input register, least significant bits first.

The 4 M.S.B.'s of the input register are the address of the control register to program ; the 4 L.S.B.'s the data.

The input register is selected by MOD/$\overline{\text{DTMF}}$ = MC/$\overline{\text{BC}}$ = "0".

Then, $\overline{\text{RTS}}$ (Request To Send) and TxD (Transmit Data) signals are internally safeguarded and the corresponding pins must be used as clock ($\overline{\text{RTS}}$) and data to be programmed (TxD).

The $\overline{\text{RTS}}$ clock, active on the falling edge, shifts the programming data available on TxD or PRD.

The transfer of programming data to the control register previously addressed is made by rising MOD/$\overline{\text{DTMF}}$ or MC/$\overline{\text{BC}}$.
From now, the $\overline{\text{RTS}}$ signal comes back to its previous functioning mode : Request To Send.

There are 2 cases of end of programming :
- At the end of programming of all the control registers, excepted RDTMF, MOD/$\overline{\text{DTMF}}$ rises to "1" while MC/$\overline{\text{BC}}$ indicates the channels used for transmission before programming ("0" for low channel transmission, "1" for high channel transmission).
- At the end of programming of RDTMF register only, MC/$\overline{\text{BC}}$ rises to "1" while MOD/$\overline{\text{DTMF}}$ and $\overline{\text{RTS}}$ are "0" during all the time of D.T.M.F. signal programmed transmission.

2.3 - Timing Diagrams

Figure 3 : Programming without Transmission

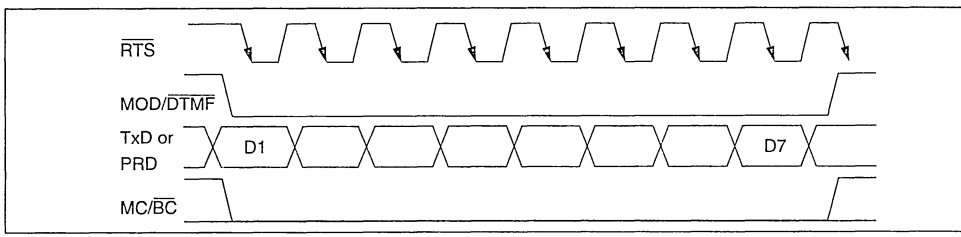


Figure 4 : Programming during Transmission

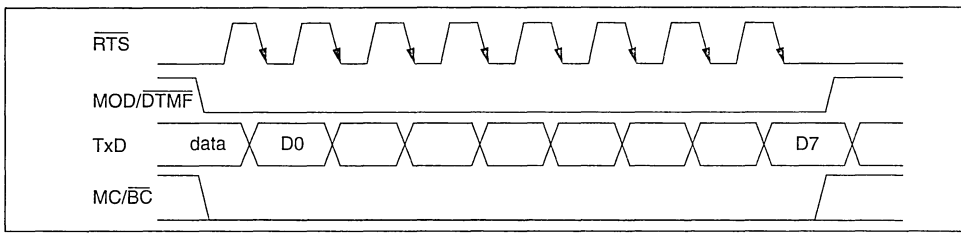
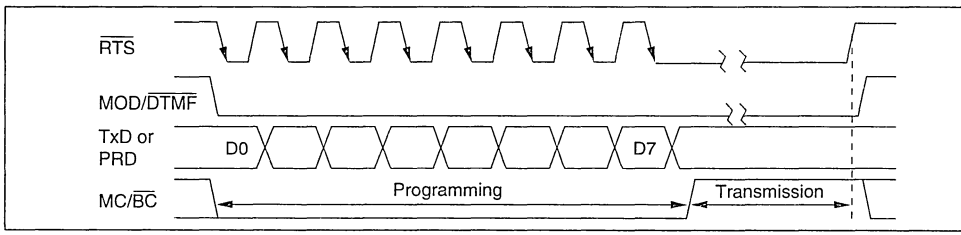


Figure 5 : DTMF Programming and Transmission



3 - THE TS7514 REGISTERS

We are going to describe now the most important points to know about these eight control registers.

Note : In the following, all the bits described are the data bits of the control registers (X = don't care). For additional informations on these registers, refer to the TS7514 corresponding data sheet.

3.1 - Mode Register : RPROG

This control register allows to choose the functioning mode of the TS7514 : either two different or the same channels for transmit and receive.

The most used mode (power-up initialization) is the receive channel programmed in the opposite way to the transmit channel controlled by MC/BC pin. In this case, bits 2 and 3 must be programmed to "0".

If bit 3 is programmed to "0" while bit 2 is programmed to "1", then transmit and receive channels are the same (high channel if MC/BC is "1", low channel if MC/BC is "0").

This last mode can be used for the full duplex on 4 wire line modem functioning or for the test with an external analog loop between transmit and receive sections (this last mode is not a loop 3 (see RPRF register)).

3.2 - D.T.M.F. Register : RDTMF

This control register allows the D.T.M.F. dialing from the TS7514.

Bits 0 and 1 program the 4 low frequencies of the D.T.M.F. signal, bits 2 and 3 the 4 high frequencies.

This register is not initialized at the power-up.

The following table give the correspondance between the digit to be dialed and the data to be programmed.

Digit	D3	D2	D1	D0	Frequency (Hz)	
					Low	High
0	0	1	1	1	941	1336
1	0	0	0	1	697	1209
2	0	1	0	1	697	1336
3	1	0	0	1	697	1477
4	0	0	1	0	770	1209
5	0	1	1	0	770	1336
6	1	0	1	0	770	1477
7	0	0	1	1	852	1209
8	0	1	1	1	852	1336
9	1	0	1	1	852	1477
A	1	1	0	0	697	1633
B	1	1	0	1	770	1633
C	1	1	1	0	852	1633
D	1	1	1	1	941	1633
*	0	0	1	1	941	1209
"	1	0	1	1	941	1477

3.3 - Transmit Attenuation Register : RATTE

This control register allows to program a transmit attenuation from 0 (0000) to 13dB (1101), with 1dB step.

With such values, the analog transmit output level on ATO pin varies from + 4 (0000) to – 9dBm (1101).

Two programming values (1110 and 1111) allows an infinite attenuation.

Such attenuation is automatically programmed at the power-up initialization. So, a different attenuation will have to be programmed to transmit data (typically 0dBm (0100) on ATO pin).

3.4 - Line Monitoring Register : RWLO

This control register allows :

- to monitor the transmit signal from – 10 (0000) to – 40dB (0011) with 10dB step,
- to monitor the receive signal from 0 (0100) to – 30dB (0111) with 10dB step,
- to send a square wave signalling frequency (2982Hz) with a level comprised between – 4 (1000) and –34dBm (1011).

This register is initialized to 11XX (neither monitoring nor signalling transmission) at the power-up.

If a receive signal monitoring is programmed, it is possible to monitor also simultaneously the transmit signal on account of the non infinite rejection ratio of the hybrid (typically 20dB) and thanks to the TS7514 internal architecture (see Figure 1), the receive signal monitoring being implemented before the receive filter.

3.5 - Transmit Filter Register : RPTF

This control register allows to transmit on ATO pin one of the following signals :

- normal (power-up initialization) modem or D.T.M.F. signals (0000),
- external voiceband analog signal through :
  - smoothing filter and attenuator (0001),
  - low-pass filter and attenuator (0010),
  - band-pass filter and attenuator (0011),
- low frequency only (0100) in D.T.M.F. mode,
- high frequency only (1000) in D.T.M.F. mode.

3.6 - Receive Filter Register : RPRF

This control register allows to program different configurations for the receive filter :
- receive filter gain of 0 (XX00), 6 (XX01) or 12dB (XX10),
- receive channel looped back on the transmit channel with a – 35dBm level and a 0dB gain (XX11) for analog test loop (loop 3),
- receive filter bypassed (X1XX) or not (X0XX),
- external connection (1XXX) via a 2.2µF non-polarized capacitor between RFO and RDI pins.

The external connection (bit 3 programmed to "1") with the capacitor is the most used mode to connect the receive filter output to the demodulator input.

Nevertheless, if an internal connection is used, bit 3 has to be programmed to "0" and external capacitor and connection between RFO and RDI pins have to be suppressed.

This register is initialized to X001 (receive filter enabled with 6dB gain) at the power-up.

3.7 - Detection Level and Hysteresis Register : RHCD

This register allows to control :
- the loss carrier detection level between – 41 (X000) and – 27dBm (X111) with 2dB step,
- the hysteresis between carrier detect on and off : 2.5 (0XXX) or 3.25 (1XXX) dB.

Be careful that the loss carrier detection level value (N2) is given related to the demodulator input (RDI). The on-line loss carrier detection level (NL) is obtained by substracting from N2 the receive filter and the hybrid gain values.

In consequence, the on-line detection level is obtained by adding to NL the hysteresis value.

This register is initialized to 0000 (– 41dBm for loss carrier detection level with a 2.5dB hysteresis) at the power-up.

3.8 - Receive Channel Register : RPRX

This control register allows to program different configurations for the receive channel :
- to use a wide (for data and tone detection) (XX0X) or a narrow (for data only) (XX1X) band filter for the receive low channel,
- to suppress (XXX1) or not (XXX0) the carrier detection delays for a "fast" carrier detection (DCD digital signal following the receive carrier signal level variations).

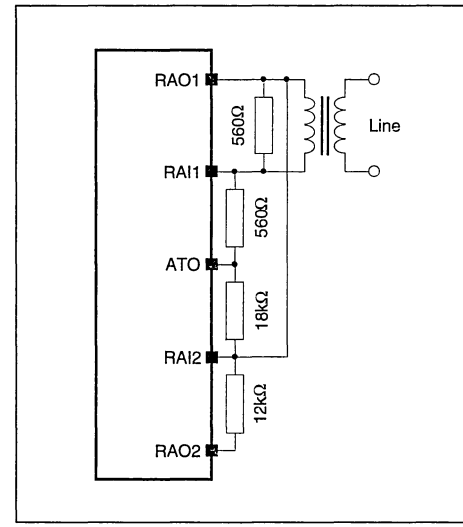
This register is initialized to XX00 (wide band filter and carrier detection delays) at the power-up.

4 - THE 4/2 WIRE CONVERSION : THE HYBRID

The TS7514 integrates two operational amplifiers. So, the hybrid implementation consists of selecting only 5 resistors in order to obtain the best adaptation and rejection possible.

With 5 % resistors and a transformer 600Ω/600Ω respecting the local agreement conditions, the hybrid so designed offers an ATO/RA02 rejection ratio upper than 20 dB.

Figure 6



5 - THE D.T.M.F. DIALING

To dial a digit (0,..., 9, A, B, C, D,*,#) in D.T.M.F. consists of programming the RDTMF control register like an other register but leaving, at the end of programming, the MOD/DTMF and RTS signals to "0" during all the time desired (in practise, the time of pressing key on a dialer).

No external component is required for this dialing.

6 - RING DETECTION

Thanks to ZCO output, it is possible to obtain in a digital way the analog zero crossing signal available on the RA02 pin of the TS7514. Then, by not totally insulating the modem from the telephone line (L1, L2) and bypassing the receive filter, ZCO can deliver the digital form of the ringing signal that may be then processed by the microcontroller.

With the scheme given Figure 7, we avoid to use opto-coupler and other external associated components to detect ring, the only external components required being a resistor and a capacitor.

When the modem is connected to the telephone line (L1, L2), the components are bypassed (see relay) and the telephone set (TPH1, TPH2) disconnected.

The ringing signal (50Hz alternative voltage superimposed to the 50V telephone line voltage), is so attenuated by the resistor but the level is sufficient to be detected by the TS7514.

Do not forget during the detection to bypass the receive filter in the RPRF register (bit 2 programmed to "1").

So programmed, the TS7514 output on ZCO pin a 50Hz digital signal and on DCD pin the ring "enveloppe" (Figure 8).

Figure 7

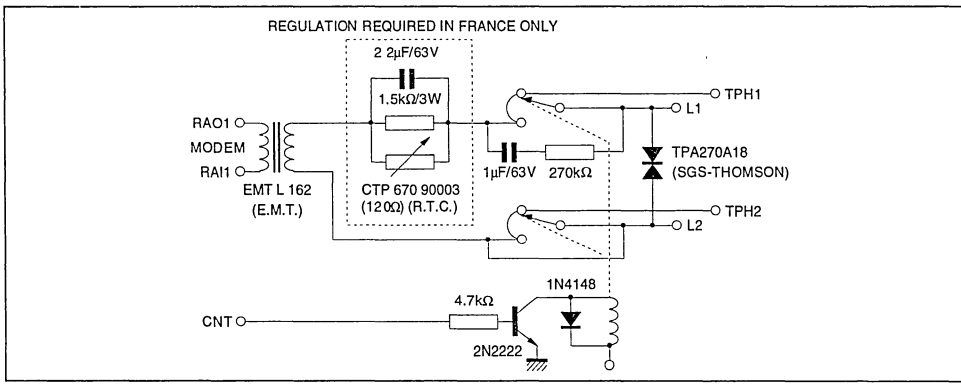
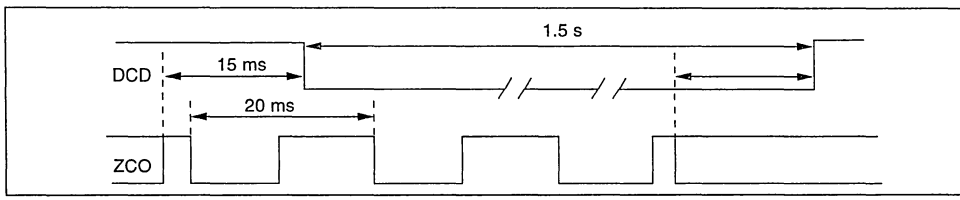


Figure 8



7 - ONE TRANSMISSION AND DETECTION

7.1 - 2100Hz Transmission (Figure 9)

To send the 2100Hz answer tone over the telephone line, the TS7514 must be programmed as follows :
- MOD/$\overline{\text{DTMF}}$ = "1" (modem),
- MC/$\overline{\text{BC}}$ = "1" (main channel),
- $\underline{\text{TxD}}$ = "0" (2100 Hz),
- $\overline{\text{RTS}}$ = "0" (transmission).

7.2 - 2100Hz Detection (Figure 10)

To detect the 2100Hz answer tone sended by the far-end modem, the TS7514 must be programmed as follows :
- $\overline{\text{RTS}}$ = "1" (no transmission),
- MOD/$\overline{\text{DTMF}}$ = "0" (tone detection),
- MC/$\overline{\text{BC}}$ = "0" (back channel).

So programmed, the $\underline{\text{TS7514}}$ detects the 2100Hz answer tone on line if $\overline{\text{DCD}}$ = "0" (carrier detection) and RxD = "0" (2100Hz).

7.3 - Low Frequency Tone Detection (Figure 11)

To detect low frequency tones (typically the 440Hz dialing tone in France) ; the TS7514 must be programmed as follows :
- $\overline{\text{RTS}}$ = "1" (no transmission),
- MOD/$\overline{\text{DTMF}}$ = "0" (tone detection),
- MC/$\overline{\text{BC}}$ = "1" (main channel),

Then, such tones are present on line if $\overline{\text{DCD}}$ = "0" (carrier detection).

Figure 9

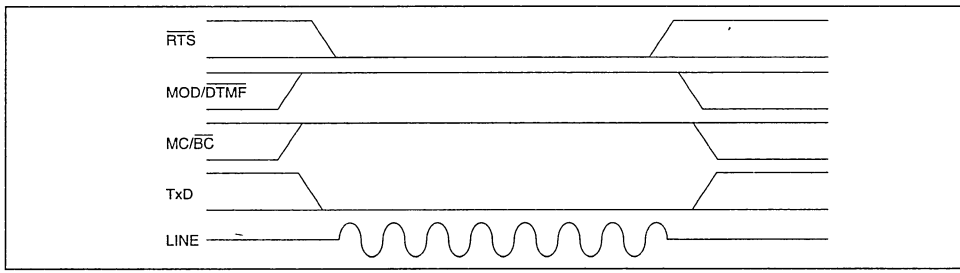


Figure 10

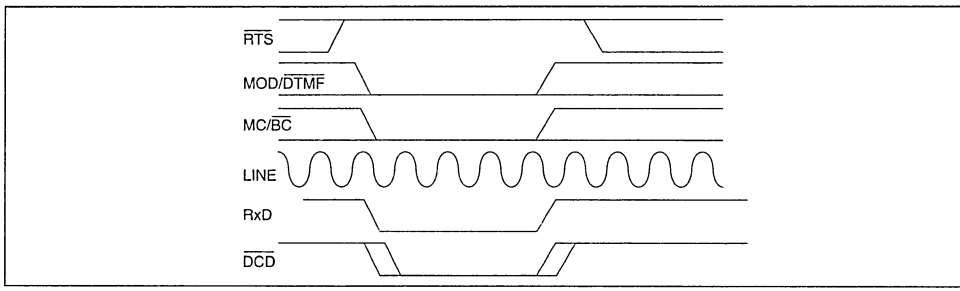
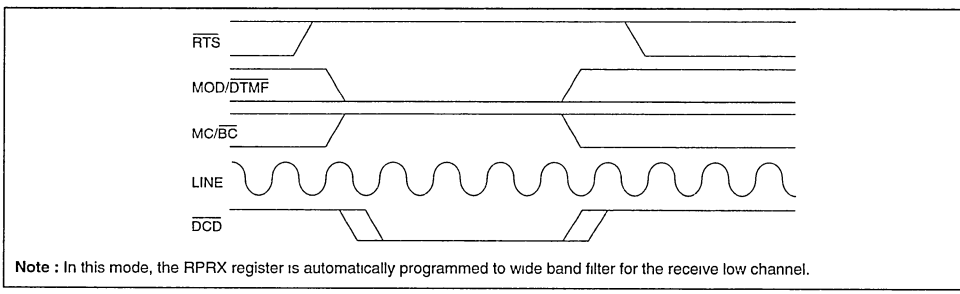


Figure 11



Note : In this mode, the RPRX register is automatically programmed to wide band filter for the receive low channel.

8 - LINE MONITORING

To monitor the different signals present on the telephone line, Figures 12 and 13 give two typical loud-speaker amplifier application schemes.

Thanks to RWLO monitoring level programming register, no external potentiometer is required to adjust the volume.

Figure 12

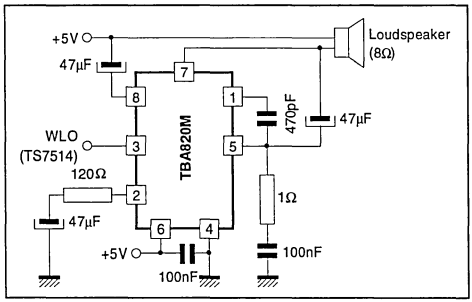
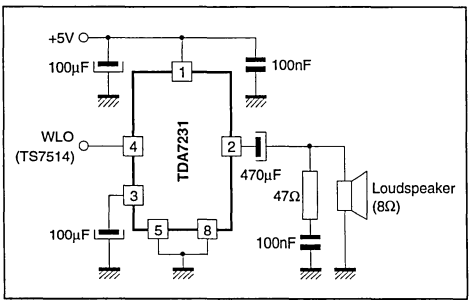


Figure 13



9 - OTHER FEATURES

- by ATxI, it is possible to send a voiceband signal over the telephone line,
- the XtalOUT may be used to implement via a buffer, the external clock of the microcontroller,
- the lay-out implementation must be as clean as possible in order to obtain the best electrical performances :
  - separation between analog and digital parts and tracks of the board,
  - analog and digital grounds separated and connected in a single point,
  - a ground plane for the component side,
  - a star distributed power supplies (idem for ground) to avoid any possible loop,
  - a maximum capacitive uncoupling as close as possible to the device,
  - a connection as short as possible between RFO and RDI via the external capacitor.

10 - CONCLUSION

We just saw, with this application note, the different functions and internal possibilities included in the TS7514 among which D.T.M.F. dialing, integrated duplexer, tone and ring detection and transmit and receive channel programmings are the most interesting.

For these features and all the others, only about 20 external passive components (resistors, capacitors, ...) are required (out of microcontroller interface) to implement a complete V.23 modem.

The TS7514 is a real low cost and powerful solution for all C.C.I.T.T. V.23 recommended standard applications.

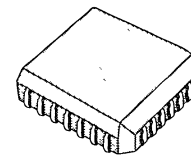
POWER LINE MODEM

SGS-THOMSON MICROELECTRONICS

ST7536

POWER LINE MODEM

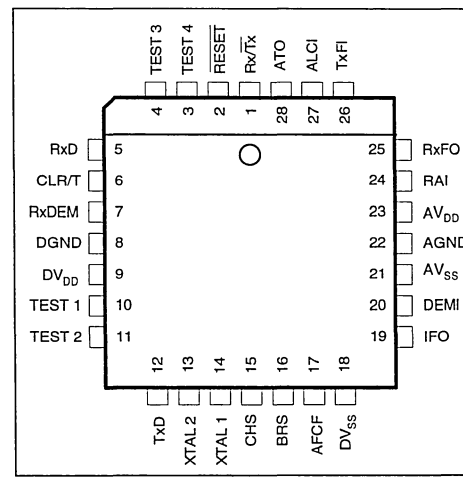
- HALF DUPLEX SYNCHRONOUS FSK MODEM
  - Two programmable channels for 600bps data rate
  - Two programmable channels for 1200bps data rate
- AUTOMATICALLY TUNED Rx AND Tx FILTERS
- TX CARRIER FREQUENCIES SYNTHESIZED FROM EXTERNAL CRYSTAL
- LOW DISTORTION Tx SIGNAL (S/H2 ≥ 50dB)
- AUTOMATIC LEVEL CONTROL ON Tx SIGNAL
- Rx SENSITIVITY : $2mV_{RMS}$ (600bps)
  $3mV_{RMS}$ (1200bps)
- Rx CLOCK RECOVERY
- POWER-DOWN MODE
- SUITABLE TO APPLICATION IN ACCORDANCE WITH DH028/29 ENEL, EN50065-1 CENELEC AND FCC SPECIFICATIONS



PLCC28
(Plastic Package)

ORDER CODE : ST7536CFN

PIN CONNECTIONS



DESCRIPTION

The ST7536 is a half duplex synchronous FSK MODEM designed for power line communication network applications.

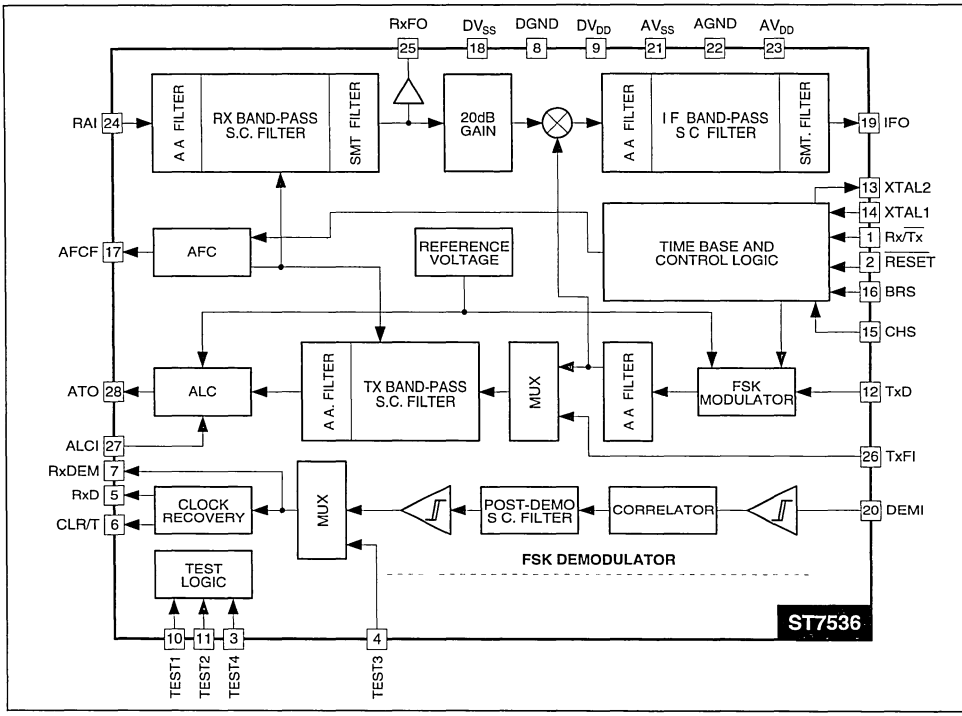
It operates from a dual power supply +5V and -5V, and requires an external interface for the coupling to the power line. It offers two programmable data rate with two programmable channels each.

PIN DESCRIPTION

Pin Name	Pin Number	Pin Type	Description
Rx/$\overline{Tx}$	1	Digital	Rx or Tx mode selection input
$\overline{RESET}$	2	Digital	Logic reset and power-down mode input. Active when low.
TEST4	3	Digital	Test input which selects the Tx band-pass filter input (TxFI) when high.
TEST3	4	Digital	Test input which gives an access to the clock recovery input stage. This input is selected when TEST1 is high.
RxD	5	Digital	Synchronous receive data output
CLR/T	6	Digital	Rx or Tx clock according to the functional mode
RxDEM	7	Digital	Demodulated data output
DGND	8	Supply	Digital ground
DVDD	9	Supply	Digital positive supply voltage : 5V ± 5%
TEST1	10	Digital	Test input which cancels the Tx to Rx mode automatic switching and validates TEST3 input. Active when high.
TEST2	11	Digital	Test input which reduces the Tx to Rx mode automatic switching time. Active when high.
TxD	12	Digital	Transmit data input
XTAL2	13	Digital	Crystal oscillator output
XTAL1	14	Digital	Crystal oscillator input
CHS	15	Digital	Channel selection input
BRS	16	Digital	Baud rate selection input
AFCF	17	Analog	Automatic frequency control output for connecting compensation network.
DVSS	18	Supply	Digital negative supply voltage : -5V ± 5%
IFO	19	Analog	Intermediate frequency filter output
DEMI	20	Analog	FSK demodulator input
AVSS	21	Supply	Analog negative supply voltage : -5V ± 5%
AGND	22	Supply	Analog ground : 0V
AVDD	23	Supply	Analog positive supply voltage : 5V ± 5%
RAI	24	Analog	Receive analog input
RxFO	25	Analog	Receive filter output
TxFI	26	Analog	Transmit filter input (selected when TEST4 is high)
ALCI	27	Analog	Automatic level control input
ATO	28	Analog	Analog transmit output

7536-01 TBL

BLOCK DIAGRAM



TRANSMIT SECTION

The transmit mode is set when Rx/$\overline{Tx}$ = 0, if Rx/$\overline{Tx}$ is held at 0 longer than 3 seconds, then the device switches automatically in the Rx mode. A new activation of the Tx mode requires Rx/$\overline{Tx}$ to be returned to 1 for a minimum 2 microsecond period before being set to 0.

The Transmit Data (TxD) is sampled on a positive edge of CLR/T which delivers the transmit bit clock when the transmit mode is selected. This data enters a FSK modulator whose two basic frequencies are selected by the Baud Rate Selection pin (BRS) and the Channel Selection pin (CHS) according to the Table 1.

Figure 1 : Tx Data Input Timing

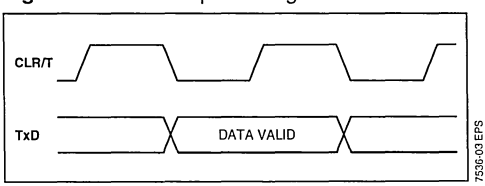


Table1

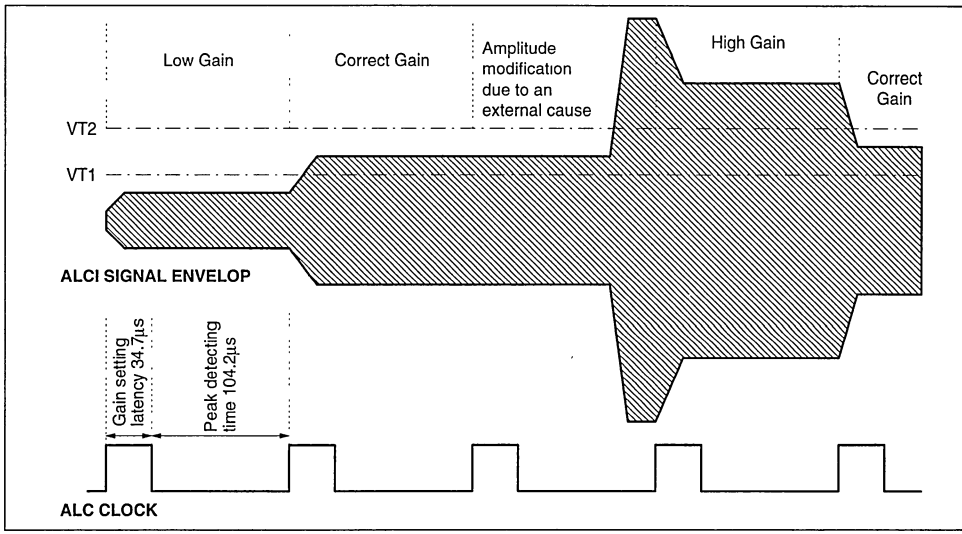
BRS	CHS	Baud Rate (Baud)	Tx Frequencies (kHz) TxD=1 - TxD=0
0	0	600	81.75 - 82.35
0	1	600	67.2 - 67.8
1	0	1200	71.4 - 72.6
1	1	1200	85.95 - 87.15

These frequencies are synthesized from a 11.0592MHz crystal oscillator ; their precision is the same as the crystal one's (100 ppm).

The modulated signal coming out of the FSK modulator is filtered by a switched-capacitor band-pass filter (Tx band-pass) in order to limit the output spectrum and to reduce the level of harmonic components.

The output stage of the Tx path consists of an Automatic Level Control (ALC) system which keeps the output signal (ATO) amplitude independant of the line impedance variations. This ALC is a variable gain system (with 32 discrete values) controlled by an analog feed-back signal ALCI (see Figure 2).

Figure 2 : Automatic Level Control Timing Chart



The ALC gain range is 0dB to -26dB and gain change is clocked at 7200Hz. Gain steps are of magnitude 0.84dB typically.

A period of this clock is decomposed into a 34.7µs gain settling latency and a 104.2µs peak detecting time. The gain change is related to the result of a peak detection obtained by making a direct comparison of ALCI maximum value (during detecting time) with two threshold voltages V_{T1} and V_{T2} (see Figure 2).

- max (VALCI)< V_{T1} - The next gain is increased by 0.84dB
- $V_{T1} \leq$ max (VALCI)$\leq V_{T2}$ - No gain change
- V_{T2} < max (VALCI) - The next gain is decreased by 0.84dB.

RECEIVE SECTION

The receive section is active when Rx/$\overline{Tx}$ = 1.

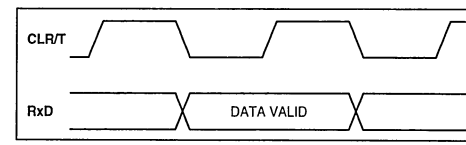
The baud rate and channel selection is also made according to Table 1.

The Rx signal is applied on RAI with a common mode voltage of 0 volt and filtered by a band-pass switched capacitor filter (Rx band-pass) centered on the received carrier frequency and whose bandwidth is around 6 kHz. The input voltage range on RAI is $2mV_{RMS}$ - $2V_{RMS}$.

The Rx filter output is amplified by a 20dB gain stage which provides symmetrical limitations for large voltage. The resulting signal is down-converted by a mixer which receives a local oscillator synthesized by the FSK modulator block. Finally an intermediate frequency band-pass filter (IF band-pass) whose central frequency is 2.7kHz when BRS = 0 and 5.4kHz when BRS = 1 improves the signal to noise ratio before entering the FSK demodulator. The coupling of the intermediate frequency filter output (IFO) to the FSK demodulator input (DEMI) is made by an external capacitor C5 (1µF ±10%, 10V) which cancels the Rx path offset voltage.

A clock recovery circuit extracts the receive clock (CLR/T) from the demodulated output (RxDEM) and delivers synchronous data (RxD) on the positive edge of CLR/T.

Figure 3 : Rx Data Output Timing



ADDITIONAL DIGITAL AND ANALOG FUNCTIONS

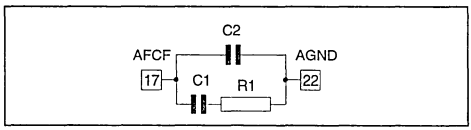
A reset intput ($\overline{RESET}$) initializes the device.

When $\overline{RESET}$ = 0, the device is in power-down mode and all the internal logic is reset. When $\overline{RESET}$ = 1, the device is active.

A time base section delivers all the internal clocks from a crystal oscillator (11.0592MHz). The crystal is connected between XTAL1 and XTAL2 pins and needs two external capacitors C3 and C4 depending on the crystal characteristic typically 22pF ±10% for proper operation. It is also possible to provide directly the clock on pin XTAL1 ; in this case C3 and C4 should be removed.

An Automatic Frequency Control (AFC) Section adjusts the central frequency of Rx and Tx band-pass filter to the carrier central frequency. The stability of the AFC loop is ensured by an external compensation network C1 (470nF ±10%, 10V), C2 (47nF ±10%, 10V) and R1 (1.5kΩ ±5%) connected to pin AFCF.

Figure 4 : Automatic Frequency Loop Filter



TESTING FEATURES

- An additionnal amplifier allows the observation of the Rx band-pass filter output on pin RxFO.
- A direct input to the Tx band-pass filter (TxFI) is available and selected when TEST4 = 1.
- The 3 second normal duration of the Tx to Rx mode automatic switching is reduced to 1.48ms when TEST2 = 1.
- When TEST1 = 1 the Tx to Rx mode automatic switching is desactivated and the functional mode of the circuit is controlled by Rx/$\overline{\text{Tx}}$ as follow : when Rx/$\overline{\text{Tx}}$ = 0 the circuit is transmitting continuously, when Rx/$\overline{\text{Tx}}$ = 1 the clock recovery block is disconnected from the FSK demodulator for testing purpose, in this configuration TEST 3 is the data input of the clock recovery block, RXDEM follow TEST3 and RxD delivers the resynchronized data.

POWER SUPPLIES WIRING AND DECOUPLING PRECAUTIONS

The ST7536 has two positive power supply pins, two negative power supply pins and two ground pins in order to separate internal analog and digital supplies. The analog and digital terminals of each supply pair must be connected together externally and require special routing precautions in order to get the best receive sensitivity performances. The three major routing requirements are :

- The ground impedance should be as low as possible, for this purpose the AGND an DGND terminals can be connected via a local plane.
- The positive and negative power supplies (AV_{DD}, DV_{DD}, AV_{SS}, DV_{SS}) should be star-connected, avoiding common current path for the digital and analog power supplies terminals.
- Five decoupling capacitors located as close as possible to the power supply terminals should be used. Two 2.2µF tantalum and two 100nF ceramic capacitors perform the main decoupling function in the vicinity of the analog power supplies and a 100nF ceramic capacitor in the vicinity of the positive digital power supply is used to reduce the high frequency perturbations generated by the logic part of the circuit.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
AV_{DD}/DV_{DD}	Positive Supply Voltage (1)	-0.3, +7	V
AV_{SS}/DV_{SS}	Negative Supply Voltage (1)	-7, +0.3	V
$V_{AGND/DGND}$	Voltage between AGND and DGND	-0.3, +0.3	V
V_I	Digital Input Voltage	DGND-0.3, DV_{DD}+0.3	V
V_O	Digital Output Voltage	DGND-0.3, DV_{DD}+0.3	V
I_O	Digital Output Current	-5, +5	mA
V_i	Analog Input Voltage	AV_{SS}-0.3, AV_{DD}+0.3	V
V_o	Analog Output Voltage	AV_{SS}-0.3, AV_{DD}+0.3	V
I_o	Analog Output Current	-5, +5	mA
P_D	Power Dissipation	500	mW
T_{oper}	Operating Temperature	- 25, + 70	°C
T_{stg}	Storage Temperature	- 65, + 150	°C

7536-02.TBL

Notes : 1. The voltages are referenced to AGND and DGND.
2. Latch-up problems can be overcome with 2 reverse biased schottky diodes connected respectively between A/DV_{DD} & A/DGND and A/DV_{SS} & A/DGND.
3. Absolute maximum ratings are values beyond which damage to device may occur. Functional operation under these conditions is not implied

GENERAL ELECTRICAL CHARACTERISTICS

The test conditions are A/DV_{DD} = +5V, A/DV_{SS} = -5V, A/DGND = 0V,
T_{amb} = -10 to 70°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ	Max	Unit
AV_{DD}/DV_{DD}	Positive Supply Voltage		4.75	5	5.25	V
AV_{SS}/DV_{SS}	Negative Supply Voltage		-5.25	-5	-4.75	V
$AI_{DD} + DI_{DD}$	Positive Supply Current in Tx Mode	$\overline{RESET}$ = 1, RX/$\overline{Tx}$ = 0		30	35	mA
$AI_{DD} + DI_{DD}$	Positive Supply Current in Rx Mode	$\overline{RESET}$ = 1, RX/$\overline{Tx}$ = 1		29	34	mA
$AI_{SS} + DI_{SS}$	Negative Supply Current in Tx Mode	$\overline{RESET}$ = 1, RX/$\overline{Tx}$ = 0	- 34	- 29		mA
$AI_{SS} + DI_{SS}$	Negative Supply Current in Rx Mode	$\overline{RESET}$ = 1, RX/$\overline{Tx}$ = 1	- 33	- 28		mA
$AI_{DD} + DI_{DD}$	Positive Power-down Current	$\overline{RESET}$ = 0, RX/$\overline{Tx}$ = 1 XTAL1 = 1			1.2	mA
$AI_{SS} + DI_{SS}$	Negative Power-down Current		- 1.2			mA
V_{IH}	High Level Input Voltage	Digital inputs except XTAL1	2.2			V
V_{IL}	Low Level Input Voltage	Digital inputs			0.8	V
V_{OH}	High Level Output Voltage	Digital outputs, I_{OH} = - 400µA	2.4			V
V_{OL}	Low Level Output Voltage	Digital outputs, I_{OL} = 1.6mA			0.4	V
V_{IH}	High Level Input Voltage	XTAL1 input	3.6			V
DC	XTAL1 Clock Duty Cycle	External clock	40		60	%

7536-03 TBL

TRANSMITTER ELECTRICAL CHARACTERISTICS

The test conditions are A/DV_{DD} = +5V, A/DGND = 0V, A/DV_{SS} = -5V,
T_{amb} = -10 to +70°C unless othewise specified

Symbol	Parameter	Test Conditions	Min.	Typ	Max	Unit
V_{TAC}	Max Carrier Output AC Voltage	R_L = 2kΩ, $V_{ALCI} < V_{T1}$	2.8	3.2	3.7	V_{PP}
HD2	Second Harmonic Distortion	R_L = 2kΩ, $V_{ALCI} < V_{T1}$			0.32	%
FD	FSK Peak-to-peak Deviation	BRS = 0 BRS = 1		600 1200		Hz Hz
TRxTx	Carrier Activation Time	After Rx/$\overline{Tx}$ 1 → 0 transition			1	ms
TALC	Carrier Stabilisation Time	ALC maximum settling time 32 gain steps			5	ms
DRNG	ALC Dynamic Range		25	26	27	dB
VT1	ALC Low Threshold Voltage		1.81	1.87		V
VT2	ALC High Threshold Voltage			2.12	2.18	V
GST	ALC Gain Step			0.84		dB
PSRR1 PSRR2	Power supply rejection ratio on ATO (1)	V_{IN} = 200mV_{PP}, f_{IN} = 50Hz on V_{DD} or V_{SS}	35 10			dB dB

7536-04 TBL

Note 1 : This characteristic is guaranteed by correlation.

RECEIVER ELECTRICAL CHARACTERISTICS

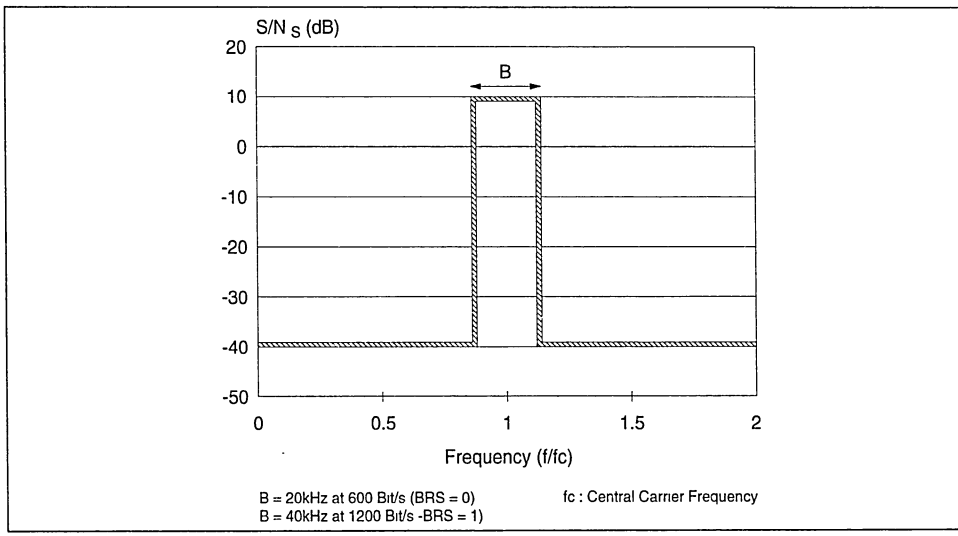
The test conditions are A/DV_{DD} = +5V, A/DGND = 0V, A/DV_{SS} = -5V,
T_{amb} = -10 to +70°C unless othewise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Maximum Input Signal				2	V_{RMS}
R_{IN}	Input Impedance		100			kΩ
RCJ	Recovered Clock Jitter	Percentage of the nominal clock	- 5		+ 5	%
PSRR1 PSRR2	Power supply rejection ratio on RxFO (1)	V_{IN} = 200mV_{PP}, f_{IN} = 50Hz on V_{DD} or V_{SS}	35 10			dB dB
V_{IN0} V_{IN1}	Rx sensitivity (1)	Typical measured BER < 10^{-5} BRS = 0 BRS = 1			2 3	mV_{RMS}
BER1 BER2	Bit error rate at minimum Rx signal (1)	White Noise, S/N = 15dB RAI = 2mV_{RMS}, BRS = 0 RAI = 3mV_{RMS}, BRS = 1		$2 \cdot 10^{-5}$ $3 \cdot 10^{-4}$	10^{-3} 10^{-3}	
BER3	Bit error rate at maximum Rx signal (1)	RAI = 2V_{RMS}, White Noise S/N = 25dB		10^{-7}	10^{-3}	
BER4	Bit error rate at medium Rx signal (1)	RAI= 0.6V_{RMS}, S/N= 15dB		10^{-6}	10^{-3}	
BER5	Bit error rate with impulsive noise (1)	RAI = 90mV_{RMS}, N = 5V_{PP} pulse wave, f = 100Hz, duty cycle = 10%			10^{-3}	
BER6 BER7	Bit error rate with modulated sinusoidal noise Ns (1)	S+ Ns < 0.2V_{RMS}, Ns = sine carrier with 80% AM modul., f_m = 1kHz, See Figure 5 S_{min} = 2mV_{RMS}, BRS = 0 S_{min} = 3mV_{RMS}, BRS = 1			 10^{-3} 10^{-3}	

7536-05 TBL

Note 1 : This characteristic is guaranteed by correlation

Figure 5 : S/N Mask for 80% AM Sine Noise



7536-07 EPS

FILTER TEMPLATES

Frequency (kHz)	Test Conditions	Amplitude (dB)		
		Min.	Typ.	Max.
RECEIVE AND TRANSMIT FILTER				
54	BRS = 0, CHS = 0			- 35
79.05		- 4	- 3	- 2
Ref 82.05			0	
85.05		- 4	- 3	- 2
123				- 35
44.4	BRS = 0, CHS = 1			- 35
65		- 4	- 3	- 2
Ref 67.46			0	
69.93		- 4	- 3	- 2
101.13				- 35
47.57	BRS = 1, CHS = 0			- 35
69.64		- 4	- 3	- 2
Ref 72.28			0	
74.92		- 4	- 3	- 2
108.36				- 35
57.08	BRS = 1, CHS = 1			- 35
83.57		- 4	- 3	- 2
Ref 86.74			0	
89.91		- 4	- 3	- 2
130.03				- 35
INTERMEDIATE FREQUENCY FILTER				
1.2	BRS = 0			- 35
2.15		- 5	- 3	- 2
Ref 2.7			0	
3.25		- 5	- 3	- 2
5.8				- 35
2.4	BRS = 1			- 35
4.3		- 5	- 3	- 2
Ref 5.4			0	
6.5		- 5	- 3	- 2
11.6				- 35

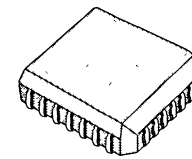
7536-06.TBL

SGS-THOMSON MICROELECTRONICS

ST7537

HOME AUTOMATION MODEM

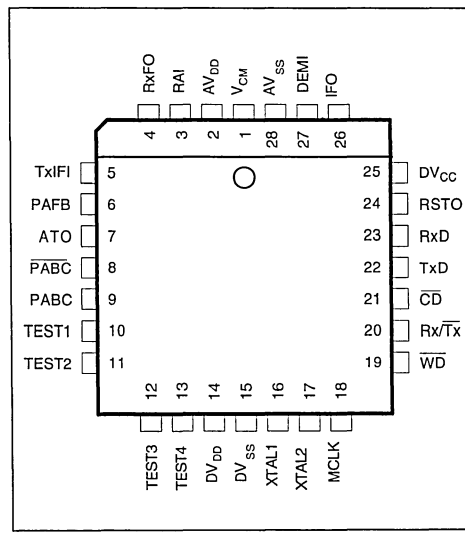
- HALF DUPLEX ASYNCHRONOUS 1200bps FSK MODEM
- Tx CARRIER FREQUENCY SYNTHESIZED FROM EXTERNAL CRYSTAL
- LOW DISTORTION Tx SIGNAL
- Rx SENSITIVITY BETTER THAN 1mV$_{RMS}$
- CARRIER DETECTION
- WATCH-DOG INPUT
- RESET AND MASTER CLOCK OUTPUTS FOR MICROCONTROLLER
- POWER AMPLIFIER BIAS CURRENT CONTROL (HIGH IMPEDANCE IN Rx MODE)
- SIMPLE AND ECONOMICAL APPLICATION SCHEMATICS
- COMPATIBLE WITH CENELEC EN 50065-1 AND FCC SPECIFICATION
- CARRIER DETECT CLAMPING ON RxD PROGRAMMABLE (ALLOWING DEMODULATION ON VERY LOW RECEIVE LEVEL, 1mV$_{RMS}$ TYPICALLY)



PLCC28
(Plastic Chip Carrier)

ORDER CODE : ST7537

PIN CONNECTIONS



DESCRIPTION

The ST7537 is a half duplex asynchronous FSK MODEM designed for home automation communication on the domestic electric mains which complies with the EN 50065-1 CENELEC standard.

It mainly operates from a 10V power supply and a 5V power supply for the microcontroller digital interface.

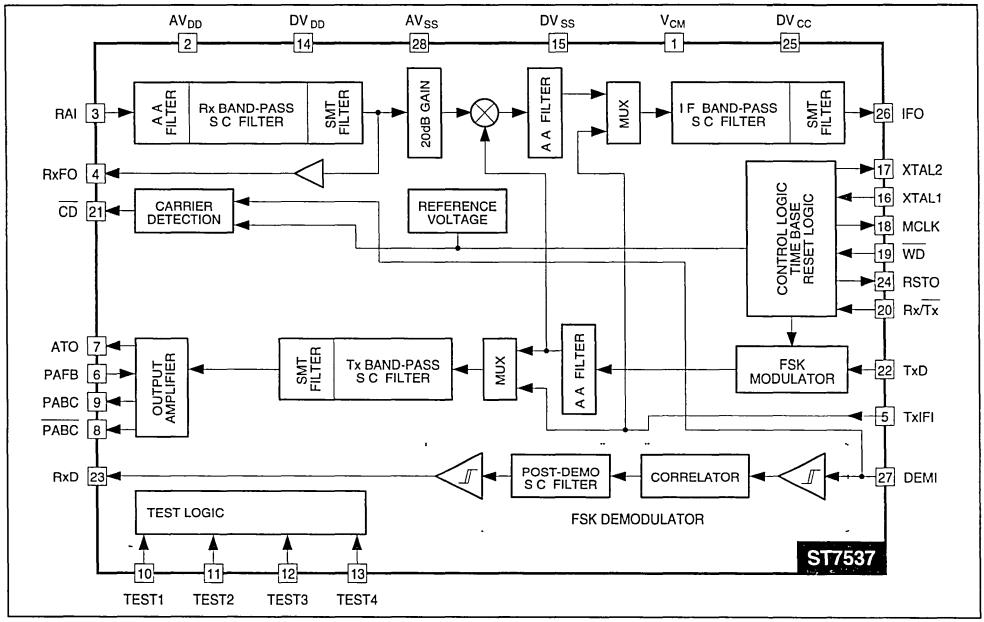
It is interfaced to the power line by an external driver, and a transformer (see Application Schematic Diagram). Its data transmission rate is 1200 bps and its carrier frequency is 132.45kHz.

PIN DESCRIPTION

Pin Name	Pin Number	Pin Type	Description
V_{CM}	1	Analog	Common Mode Voltage
AV_{DD}	2	Supply	Analog Power Supply : 10V ±5 %
RAI	3	Analog	Receive Analog Input
RxFO	4	Analog	Receive Filter Output
TxIFI	5	Analog	Transmit and Intermediate Frequency Filters Test Input (mode TEST3)
PAFB	6	Analog	Power Amplifier Feed-back Input
ATO	7	Analog	Analog Transmit Output
$\overline{PABC}$	8	Digital (10V)	Power Amplifier Bias Current Control Complementary Output
PABC	9	Digital (10V)	Power Amplifier Bias Current Control Output
TEST1	10	Digital	Tx to Rx Automatic Mode Switching Control Input
TEST2	11	Digital	Automatic Mode Switching Time and Watch-dog Time Reduction Control Input
TEST3	12	Digital	TxIFI Selection Input
TEST4	13	Digital	Undelayed Reset Input
DV_{DD}	14	Supply	Digital Power Supply : 10V ±5%
DV_{SS}	15	Supply	Digital Ground : 0V
XTAL1	16	Digital (10V)	Crystal Oscillator Input
XTAL2	17	Digital (10V)	Crystal Oscillator Output
MCLK	18	Digital	Master Clock Output
$\overline{WD}$	19	Digital	Watch-dog Input
Rx/$\overline{Tx}$	20	Digital	Rx or Tx Mode Selection Input
$\overline{CD}$	21	Digital	Carrier Detect Output
TxD	22	Digital	Transmit Data Input
RxD	23	Digital	Receive Data Output
RSTO	24	Digital	Reset Output
DV_{CC}	25	Supply	Digital Buffers Supply Voltage : 5 V ±5 %
IFO	26	Analog	Intermediate Frequency Filter Output
DEMI	27	Analog	Demodulator Input
AV_{SS}	28	Supply	Analog Ground : 0V

7537-01 TBL

BLOCK DIAGRAM



TRANSMIT SECTION

The transmit mode is set when Rx/$\overline{Tx}$ = 0, if Rx/$\overline{Tx}$ is held at 0 longer than 1 second, then the device switches automatically in the Rx mode. A new activation of the Tx mode requires Rx/$\overline{Tx}$ to be returned to 1 for a minimum 2 microsecond period before being set to 0.

The Transmit Data (TxD) enter asynchronously the FSK modulator with a nominal intra-message data rate of 1200 bps.

The basic transmit frequencies are :
- f(TxD=0) = 133.05kHz
- f(TxD=1) = 131.85kHz

These frequencies are synthesized from a 11.0592MHz crystal oscillator; their precision is the same as the crystal one's (100ppm).
The modulated signal coming out of the FSK modulator is filtered by a switched-capacitor band-pass filter (Tx band-pass) in order to limit the output spectrum and to reduce the level of harmonic components.
The final stage of the Tx path consists of an operational amplifier which needs a feed-back signal (PAFB) from the power amplifier as shown on Application Schematic Diagram.
In Tx mode the Receive Data (RxD) signal is set to 1.

RECEIVE SECTION

The receive section is active when Rx/$\overline{Tx}$ = 1.

The Rx signal is applied on RAI and filtered by a band-pass switched capacitor filter (Rx band-pass) centered on the carrier frequency and whose bandwidth is around 12kHz.

The Rx filter output is amplified by a 20dB gain stage which provides symetrical limitations for large voltage.

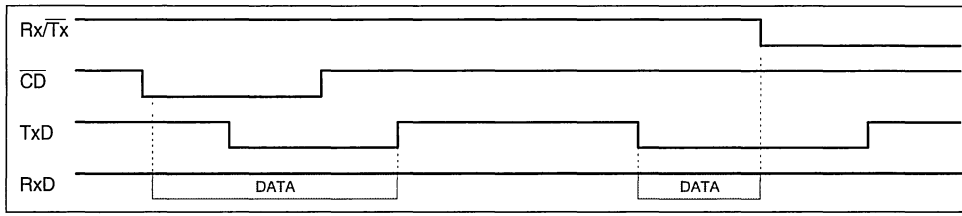
The resulting signal is down-converted by a mixer which receives a local oscillator synthesized by the FSK modulator block. Finally an intermediate frequency band-pass filter (IF band-pass) whose central frequency is 5.4kHz improves the signal to noise ratio before entering the FSK demodulator.

The coupling of the intermediate frequency filter output (IFO) to the FSK demodulator input (DEMI) is made by an external capacitor C5 (100nF ±10%, 10V) which cancels the Rx path offset voltage.

The RxD output delivers the demodulated signal if the carrier detect ($\overline{CD}$) signal is low and is set to high level when CD = 1.

The RxD output can delivers the demodulated signal whatever the level of $\overline{CD}$ (0 or 1) if Rx/$\overline{Tx}$ = 1 and TxD = 0 (see Figure 1).

Figure 1 : Data Timing Chart



ADDITIONAL DIGITAL AND ANALOG FUNCTIONS

Time base

A time base section delivers all the internal clocks from a crystal oscillator (11.0592MHz). The crystal is connected between XTAL1 and XTAL2 pins and needs two external capacitors C3 and C4 (22pF ±10%, 10V) for proper operation.

Reset and watch-dog

The reset output (RSTO) is driven high when the supply voltage is lower than Vrh (typically 7.6V) with an hysteresis Vrh-Vrl (typically 300mV) or when no negative transition occurs on the watch-dog input (WD) for more than 1.5 second (see the timing chart on Figure 2). When a reset occurs RSTO is held high for at least 50ms.

Signal detection

The Carrier Detect output ($\overline{CD}$) is driven low when the input signal amplitude on RAI is greater than V_{CD} for at least T_{CD} (typically 6ms see the timing chart on Figure 3). When the input signal desappears or becomes lower than V_{CD}, $\overline{CD}$ is held low for at least Tcd before returning to a high level. V_{CD} is the carrier detection threshold voltage which is set internally to detect $5mV_{RMS}$ typically.

External power amplifier bias control

Two dedicated digital output (PABC and $\overline{PABC}$) delivering a signal between 0V and 10V are driven low respectively high, when the circuit is set in the receive mode (Rx/$\overline{Tx}$=1) or when the transmit mode time out (1 second) is exceeded; in the same time the output ATO is put in a high impedance state.

TESTING FEATURES

- An additionnal amplifier allows the observation of the Rx band-pass filter output on pin RxFO.
- A direct input to the Tx band-pass filter and to the IF filter (TxIFI) is selected when TEST3 = 1.
- The 1 second normal duration of the Tx to Rx mode automatic switching is reduced to 488µs and the 1.5 second watch-dog time out is reduced to 46.3µs when TEST2 = 1.
- When TEST1 = 1 the Tx to Rx mode automatic switching is desactivated and the functional mode of the circuit is fully controlled by Rx/$\overline{Tx}$.
- TEST4 is a reset input which allows an undelayed control of RSTO and of the internal state of the circuit.

POWER SUPPLIES WIRING PRECAUTIONS

The ST7537 has two positive power supply terminals (AV_{DD},DV_{DD}) and two ground terminals (AV_{SS},DV_{SS}) in order to separate internal analog and digital supplies. The analog and digital terminals of each supply pair must be connected together externally for proper operation.

The V_{DD} must be protected against short-circuit for proper operation.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
AV_{DD}/DV_{DD}	Supply Voltage (1)	- 0.3, + 12	V
V_I	Digital Input Voltage	DV_{SS} - 0.3, DV_{DD} + 0.3	V
V_O	Digital Output Voltage (microcontroller interface)	DV_{SS} - 0.3, DV_{CC} + 0.3	V
V_O	Digital Output Voltage (PABC and $\overline{PABC}$)	DV_{SS} - 0.3, DV_{DD} + 0.3	V
I_O	Digital Output Current	- 5, + 5	mA
V_I	Analog Input Voltage	AV_{SS} - 0.3, AV_{DD} + 0.3	V
V_O	Analog Output Voltage	AV_{SS} - 0.3, AV_{DD} + 0.3	V
I_O	Analog Output Current	- 5, + 5	mA
P_D	Power Dissipation	500	mW
T_{oper}	Operating Temperature	0, + 70	°C
T_{stg}	Storage Temperature	- 55, + 150	°C

7537-02 TBL

Notes : 1. The voltages are referenced to AV_{SS} and DV_{SS}.
2. Absolute maximum ratings are values beyond which damage to device may occur. Functional operation under these conditions is not implied.

GENERAL ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0°C \leq T_{amb} \leq 70°C$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AV_{DD} DV_{DD}	Supply Voltage		9.5	10	10.5	V
AI_{DD} + DI_{DD}	Supply Current			30		mA
DV_{CC}	Digital Output Supply Voltage		4.75		5.25	V
DI_{CC}	Digital Output Supply Current			1.5		mA
V_{IH}	High Level Input Voltage	Digital Inputs	4.2			V
V_{IL}	Low Level Input Voltage	Digital Inputs			0 8	V
V_{OH}	High Level Output Voltage	I_{OH} = -100µA • Digital Outputs • Digital Outputs PABC and $\overline{PABC}$	 4.9 9.8			 V V
V_{OL}	Low Level Output Voltage	I_{OL} = 100µA • Digital Outputs • Digital Outputs PABC and $\overline{PABC}$			 0.1 0.2	 V V
DC	Duty Cycle	MCLK Output, C_L = 15pF	40		60	%

7537-03 TBL

TRANSMITTER ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0°C \leq T_{amb} \leq 70°C$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VTAC	Max Carrier Output AC Voltage	R_L = 5.6kΩ $R_L(AV_{SS})$ = 5.6kΩ R(ATO, PAFB) = 1kΩ	0.8	1.0	1.3	V_{RMS}
HD2	Second Harmonic Distortion			- 50		dB
HD3	Third Harmonic Distortion			- 60		dB
FD	FSK Peak-to-peak Deviation			1200		Hz

7537-04 TBL

RECEIVER ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0°C \leq T_{amb} \leq 70°C$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input Sensitivity			1	10	mV_{RMS}
V_{IN}	Maximum Input Signal				2	V_{RMS}
R_{IN}	Input Impedance		15			kΩ
GRx	Receive Gain	f = 132.45kHz		20		dB
BER	Bit Error Rate (1)	S/N = 15dB, S = 10mV_{RMS}, N : white		10^{-5}	10^{-3}	
t_{DEM}	Demodulation Time	Alternate 0 , 1 sequence		3		T bit
V_{CD}	Carrier Detection Level	f = 132.45kHz, sine wave		5	10	mV_{RMS}

7537-05 TBL

Note 1 : This parameter is guaranteed by correlation

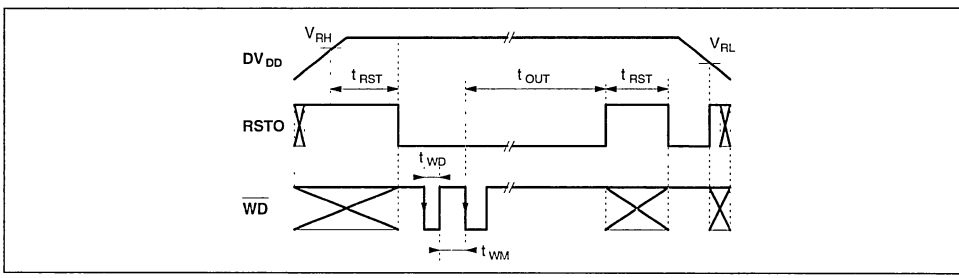
ADDITIONAL DIGITAL AND ANALOG FUNCTIONS ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0°C \leq T_{amb} \leq 70°C$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	High Level Reset Voltage	See Figure 2		7.9		V
V_{RL}	Low Level Reset Voltage	See Figure 2		7.6		V
t_{RST}	Reset Time	See Figure 2	50			ms
t_{WD}	Watch-dog Pulse Width	See Figure 2	500			ns
t_{WM}	Watch-dog Pulse Period	See Figure 2	800			µs
t_{OUT}	Watch-dog Time Out	See Figure 2			1.5	s
t_{CD}	Carrier Detection Time	See Figure 3	3		6.5	ms

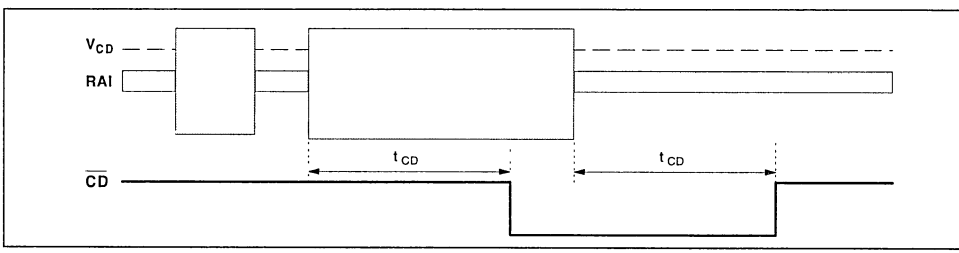
7537-06 TBL

Figure 2 : Reset and Watch-dog Timing Chart



7537-04 EPS

Figure 3 : Carrier Detection Timing Chart



7537-05 EPS

FILTER TEMPLATES

Receive and Transmit Filter

Frequency (kHz)	Gain (dB)		
	Min.	Typ.	Max.
92			- 30
126.45	- 5	- 3	- 2
Ref 132.45		0	
138.45	- 5	- 3	- 2
180			- 30

Intermediate FrequencyFilter

Frequency (kHz)	Gain (dB)		
	Min.	Typ.	Max.
2.4			- 35
4.3	- 4	- 3	- 1
Ref 5.4		0	
6.5	- 5	- 3	- 2
11.6			- 35

7537-07 TBL

APPLICATION SCHEMATIC INFORMATIONS

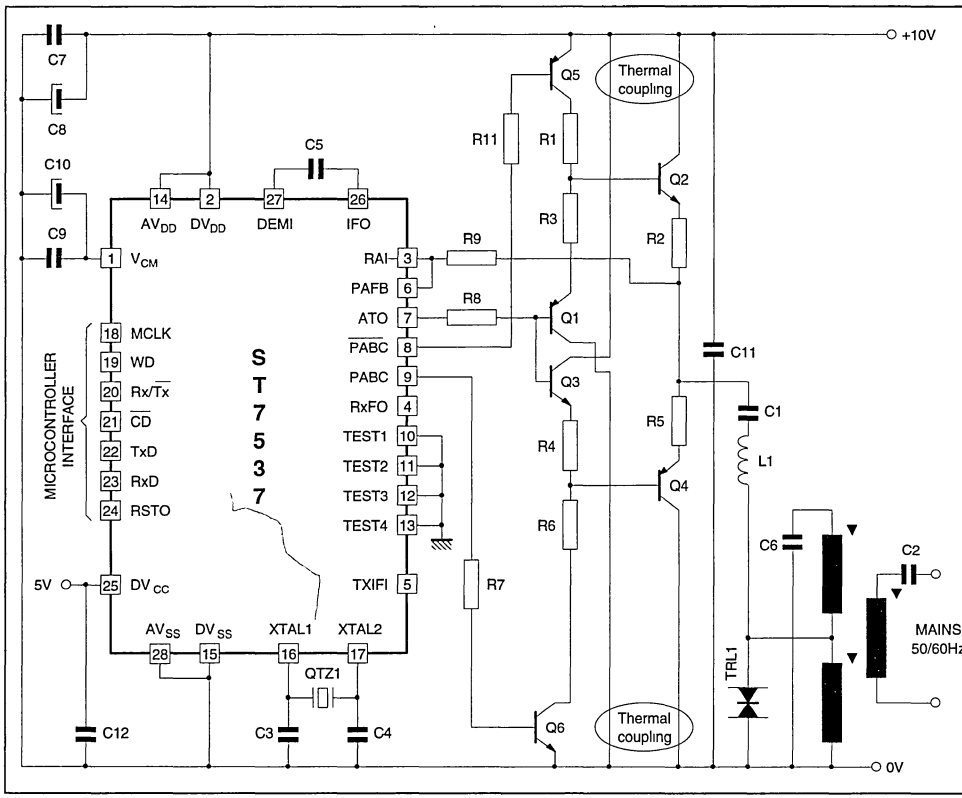
RESISTORS			CAPACITORS			
R1	180Ω		C1	1µF		Ceramic 50
R2	2.2Ω		C2	470nF		Paper, class X2
R3	2.2Ω		C3 (2)	22pF	10%	Ceramic 10V
R4	2.2Ω		C4 (2)	22pF	10%	Ceramic 10V
R5	2.2Ω		C5	100nF	10%	Ceramic 10V
R6	180Ω		C6	6.8nF	5%	Plastic Film 50V
R7	47kΩ		C7	100nF		Ceramic 10V
R8	1kΩ		C8	2.2µF		
R9	1kΩ	5%	C9	100nF		Ceramic 10V
R11	47kΩ		C10	2.2µF		
INDUCTOR			C11 (1)	100nF		Ceramic 10V
L1	10µH	≅ 1.5Ω	C12 (1)	100nF		Ceramic 10V

TRANSISTORS	TRANSIL
Q1 : 2N2907 Q2 : 2N2222 Q3 : 2N2222 Q4 : 2N2907 Q5 : 2N2907 Q6 : 2N2222	TRL1 : SGS-THOMSON P6KE6V8CP
	TRANSFORMER
	TR1 : TOKO T1002 N
	CRYSTAL
	QTZ1 : 11.0592MHz parallel resonance

7537-08 TBL

Notes : 1. These capacitors might not be necessary if the overall power supplies decoupling is sufficient.
2. The value of these capacitors depends on the crystal parameters

APPLICATION SCHEMATIC DIAGRAM

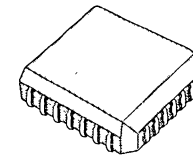


SGS-THOMSON MICROELECTRONICS

ST7537HS1

HOME AUTOMATION MODEM

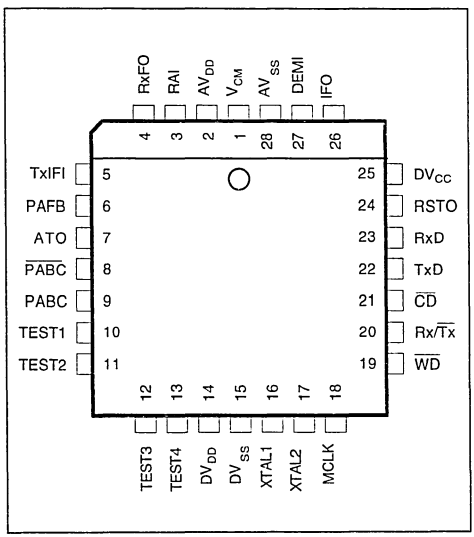
- HALF DUPLEX ASYNCHRONOUS 2400bps FSK MODEM
- Tx CARRIER FREQUENCY SYNTHESIZED FROM EXTERNAL CRYSTAL
- LOW DISTORTION Tx SIGNAL
- Rx SENSITIVITY BETTER THAN 1mV$_{RMS}$
- CARRIER DETECTION
- WATCH-DOG INPUT
- RESET AND MASTER CLOCK OUTPUTS FOR MICROCONTROLLER
- POWER AMPLIFIER BIAS CURRENT CONTROL (HIGH IMPEDANCE IN Rx MODE)
- SIMPLE AND ECONOMICAL APPLICATION SCHEMATICS
- COMPATIBLE WITH CENELEC EN 50065-1 AND FCC SPECIFICATION
- CARRIER DETECT CLAMPING ON RxD PROGRAMMABLE (ALLOWING DEMODULATION ON VERY LOW RECEIVE LEVEL, 1mV$_{RMS}$ TYPICALLY)



PLCC28
(Plastic Chip Carrier)

ORDER CODE : ST7537HS1

PIN CONNECTIONS



DESCRIPTION

The ST7537HS1 is a half duplex asynchronous FSK MODEM designed for home automation communication on the domestic electric mains which complies with the EN 50065-1 CENELEC standard.

It mainly operates from a 10V power supply and a 5V power supply for the microcontroller digital interface.

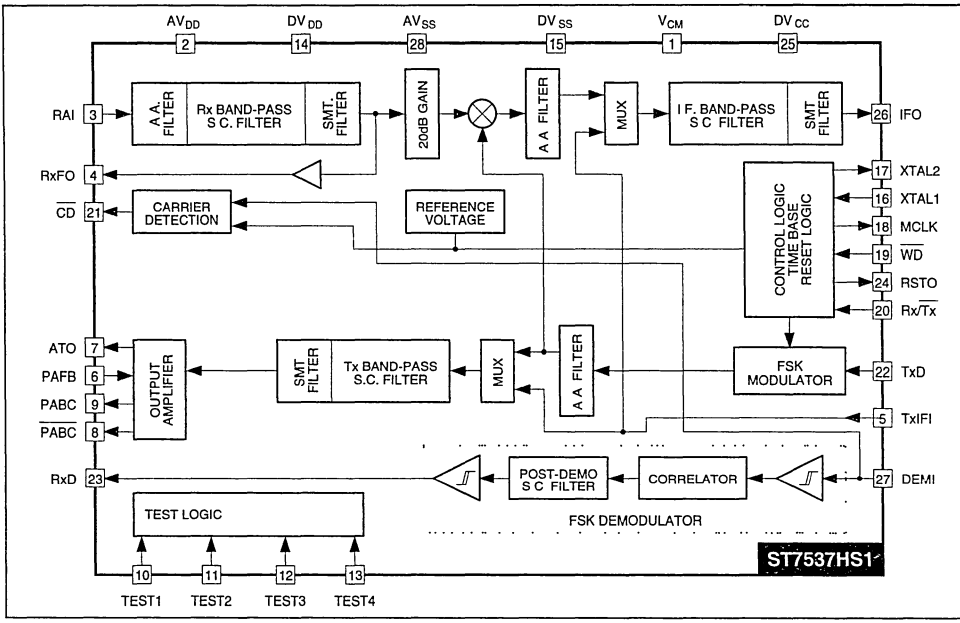
It is interfaced to the power line by an external driver, and a transformer (see Application Schematic Diagram). Its data transmission rate is 2400 bps and its carrier frequency is 132.45kHz.

PIN DESCRIPTION

Pin Name	Pin Number	Pin Type	Description
V_{CM}	1	Analog	Common Mode Voltage
AV_{DD}	2	Supply	Analog Power Supply : 10V ±5 %
RAI	3	Analog	Receive Analog Input
RxFO	4	Analog	Receive Filter Output
TxIFI	5	Analog	Transmit and Intermediate Frequency Filters Test Input (mode TEST3)
PAFB	6	Analog	Power Amplifier Feed-back Input
ATO	7	Analog	Analog Transmit Output
$\overline{PABC}$	8	Digital (10V)	Power Amplifier Bias Current Control Complementary Output
PABC	9	Digital (10V)	Power Amplifier Bias Current Control Output
TEST1	10	Digital	Tx to Rx Automatic Mode Switching Control Input
TEST2	11	Digital	Automatic Mode Switching Time and Watch-dog Time Reduction Control Input
TEST3	12	Digital	TxIFI Selection Input
TEST4	13	Digital	Undelayed Reset Input
DV_{DD}	14	Supply	Digital Power Supply : 10V ±5%
DV_{SS}	15	Supply	Digital Ground : 0V
XTAL1	16	Digital (10V)	Crystal Oscillator Input
XTAL2	17	Digital (10V)	Crystal Oscillator Output
MCLK	18	Digital	Master Clock Output
$\overline{WD}$	19	Digital	Watch-dog Input
Rx/$\overline{Tx}$	20	Digital	Rx or Tx Mode Selection Input
$\overline{CD}$	21	Digital	Carrier Detect Output
TxD	22	Digital	Transmit Data Input
RxD	23	Digital	Receive Data Output
RSTO	24	Digital	Reset Output
DV_{CC}	25	Supply	Digital Buffers Supply Voltage : 5V ±5 %
IFO	26	Analog	Intermediate Frequency Filter Output
DEMI	27	Analog	Demodulator Input
AV_{SS}	28	Supply	Analog Ground : 0V

7537H-01 TBL

BLOCK DIAGRAM



TRANSMIT SECTION

The transmit mode is set when Rx/$\overline{Tx}$ = 0, if Rx/$\overline{Tx}$ is held at 0 longer than 1 second, then the device switches automatically in the Rx mode. A new activation of the Tx mode requires Rx/$\overline{Tx}$ to be returned to 1 for a minimum 2 microsecond period before being set to 0.

The Transmit Data (TxD) enter asynchronously the FSK modulator with a nominal intra-message data rate of 2400 bps.

The basic transmit frequencies are :
- f(TxD=0) = 133.05kHz
- f(TxD=1) = 131.85kHz

These frequencies are synthesized from a 11.0592MHz crystal oscillator; their precision is the same as the crystal one's (100ppm).

The modulated signal coming out of the FSK modulator is filtered by a switched-capacitor band-pass filter (Tx band-pass) in order to limit the output spectrum and to reduce the level of harmonic components.

The final stage of the Tx path consists of an operational amplifier which needs a feed-back signal (PAFB) from the power amplifier as shown on Application Schematic Diagram.

In Tx mode the Receive Data (RxD) signal is set to 1.

RECEIVE SECTION

The receive section is active when Rx/$\overline{Tx}$ = 1.

The Rx signal is applied on RAI and filtered by a band-pass switched capacitor filter (Rx band-pass) centered on the carrier frequency and whose bandwidth is around 12kHz.

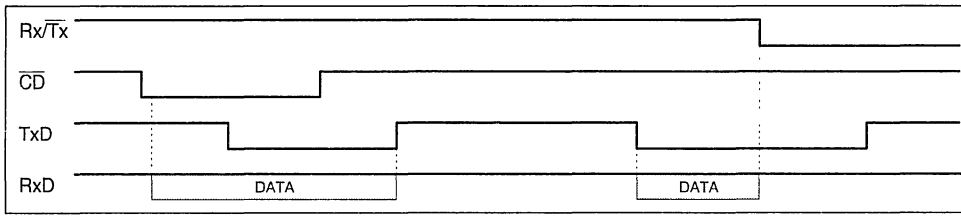
The Rx filter output is amplified by a 20dB gain stage which provides symetrical limitations for large voltage. The resulting signal is down-converted by a mixer which receives a local oscillator synthesized by the FSK modulator block. Finally an intermediate frequency band-pass filter (IF band-pass) whose central frequency is 5.4kHz improves the signal to noise ratio before entering the FSK demodulator.

The coupling of the intermediate frequency filter output (IFO) to the FSK demodulator input (DEMI) is made by an external capacitor C5 (100nF ±10%, 10V) which cancels the Rx path offset voltage.

The RxD output delivers the demodulated signal if the carrier detect ($\overline{CD}$) signal is low and is set to high level when $\overline{CD}$ = 1.

The RxD output can delivers the demodulated signal whatever the level of $\overline{CD}$ (0 or 1) if Rx/$\overline{Tx}$ = 1 and TxD = 0 (see Figure 1).

Figure 1 : Data Timing Chart



ADDITIONAL DIGITAL AND ANALOG FUNCTIONS

Time base

A time base section delivers all the internal clocks from a crystal oscillator (11.0592MHz). The crystal is connected between XTAL1 and XTAL2 pins and needs two external capacitors C3 and C4 (22pF ±10%, 10V) for proper operation.

Reset and watch-dog

The reset output (RSTO) is driven high when the supply voltage is lower than Vrh (typically 7.6V) with an hysteresis Vrh-Vrl (typically 300mV) or when no negative transition occurs on the watch-dog input (WD) for more than 1.5 second (see the timing chart on Figure 2). When a reset occurs RSTO is held high for at least 50ms.

Signal detection

The Carrier Detect output ($\overline{CD}$) is driven low when the input signal amplitude on RAI is greater than V_{CD} for at least T_{CD} (typically 6ms see the timing chart on Figure 3). When the input signal desappears or becomes lower than V_{CD}, $\overline{CD}$ is held low for at least Tcd before returning to a high level. V_{CD} is the carrier detection threshold voltage which is set internally to detect $5mV_{RMS}$ typically.

External power amplifier bias control

Two dedicated digital output (PABC and $\overline{PABC}$) delivering a signal between 0V and 10V are driven low respectively high, when the circuit is set in the receive mode (Rx/$\overline{Tx}$=1) or when the transmit mode time out (1 second) is exceeded; in the same time the output ATO is put in a high impedance state.

TESTING FEATURES

- An additionnal amplifier allows the observation of the Rx band-pass filter output on pin RxFO.
- A direct input to the Tx band-pass filter and to the IF filter (TxIFI) is selected when TEST3 = 1.
- The 1 second normal duration of the Tx to Rx mode automatic switching is reduced to 488µs and the 1.5 second watch-dog time out is reduced to 46.3µs when TEST2 = 1.
- When TEST1 = 1 the Tx to Rx mode automatic switching is desactivated and the functional mode of the circuit is fully controlled by Rx/$\overline{Tx}$.
- TEST4 is a reset input which allows an undelayed control of RSTO and of the internal state of the circuit.

POWER SUPPLIES WIRING PRECAUTIONS

The ST7537HS1 has two positive power supply terminals (AV_{DD},DV_{DD}) and two ground terminals (AV_{SS},DV_{SS}) in order to separate internal analog and digital supplies. The analog and digital terminals of each supply pair must be connected together externally for proper operation.

The V_{DD} must be protected against short-circuit for proper operation.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
AV_{DD}/DV_{DD}	Supply Voltage (1)	- 0.3, + 12	V
V_I	Digital Input Voltage	DV_{SS} - 0.3, DV_{DD} + 0.3	V
V_O	Digital Output Voltage (microcontroller interface)	DV_{SS} - 0.3, DV_{CC} + 0.3	V
V_O	Digital Output Voltage (PABC and $\overline{PABC}$)	DV_{SS} - 0.3, DV_{DD} + 0.3	V
I_O	Digital Output Current	- 5, + 5	mA
V_I	Analog Input Voltage	AV_{SS} - 0.3, AV_{DD} + 0.3	V
V_O	Analog Output Voltage	AV_{SS} - 0.3, AV_{DD} + 0.3	V
I_O	Analog Output Current	- 5, + 5	mA
P_D	Power Dissipation	500	mW
T_{oper}	Operating Temperature	0, + 70	°C
T_{stg}	Storage Temperature	- 55, + 150	°C

7537H-02 TBL

Notes : 1. The voltages are referenced to AV_{SS} and DV_{SS}.
2. Absolute maximum ratings are values beyond which damage to device may occur. Functional operation under these conditions is not implied.

GENERAL ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0°C \le T_{amb} \le 70°C$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AV_{DD} DV_{DD}	Supply Voltage		9.5	10	10.5	V
AI_{DD} + DI_{DD}	Supply Current			30		mA
DV_{CC}	Digital Output Supply Voltage		4.75		5.25	V
DI_{CC}	Digital Output Supply Current			1.5		mA
V_{IH}	High Level Input Voltage	Digital Inputs	4.2			V
V_{IL}	Low Level Input Voltage	Digital Inputs			0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -100µA • Digital Outputs • Digital Outputs PABC and $\overline{PABC}$	 4.9 9.8			 V V
V_{OL}	Low Level Output Voltage	I_{OL} = 100µA • Digital Outputs • Digital Outputs PABC and $\overline{PABC}$			 0.1 0.2	 V V
DC	Duty Cycle	MCLK Output, C_L = 15pF	40		60	%

7537H-03 TBL

TRANSMITTER ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0°C \le T_{amb} \le 70°C$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VTAC	Max Carrier Output AC Voltage	R_L = 5.6kΩ $R_L(AV_{SS})$ = 5.6kΩ R(ATO, PAFB) = 1kΩ	0.8	1.0	1.3	V_{RMS}
HD2	Second Harmonic Distortion			- 50		dB
HD3	Third Harmonic Distortion			- 60		dB
FD	FSK Peak-to-peak Deviation			1200		Hz

7537H-04 TBL

RECEIVER ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0^{o}C \leq T_{amb} \leq 70^{o}C$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input Sensitivity			1	10	mV_{RMS}
V_{IN}	Maximum Input Signal				2	V_{RMS}
R_{IN}	Input Impedance		15			kΩ
GRx	Receive Gain	f = 132.45kHz		20		dB
BER	Bit Error Rate (1)	S/N = 15dB, S = 10mV_{RMS}, N : white		10^{-5}	10^{-3}	
t_{DEM}	Demodulation Time	Alternate 0 , 1 sequence		3		T bit
V_{CD}	Carrier Detection Level	f = 132.45kHz, sine wave		5	10	mV_{RMS}

7537H-05 TBL

Note 1 : This parameter is guaranteed by correlation

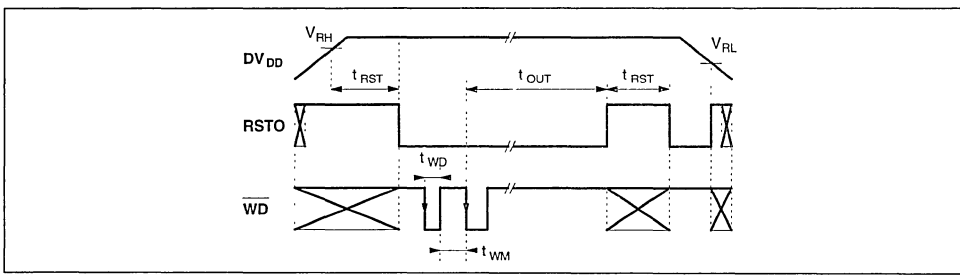
ADDITIONAL DIGITAL AND ANALOG FUNCTIONS ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0^{o}C \leq T_{amb} \leq 70^{o}C$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	High Level Reset Voltage	See Figure 2		7.9		V
V_{RL}	Low Level Reset Voltage	See Figure 2		7.6		V
t_{RST}	Reset Time	See Figure 2	50			ms
t_{WD}	Watch-dog Pulse Width	See Figure 2	500			ns
t_{WM}	Watch-dog Pulse Period	See Figure 2	800			µs
t_{OUT}	Watch-dog Time Out	See Figure 2			1.5	s
t_{CD}	Carrier Detection Time	See Figure 3	3		6.5	ms

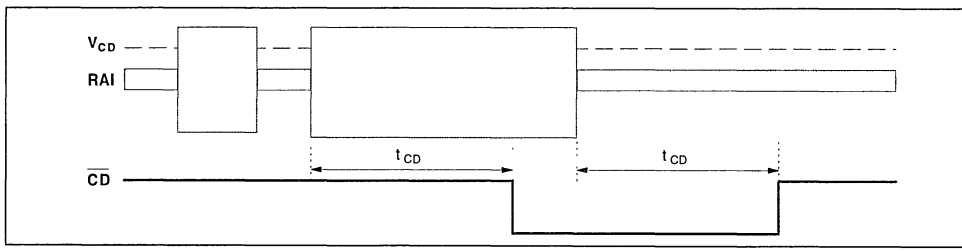
7537H-06 TBL

Figure 2 : Reset and Watch-dog Timing Chart



7537H-04 EPS

Figure 3 : Carrier Detection Timing Chart



7537H-05 EPS

FILTER TEMPLATES

Receive and Transmit Filter

Frequency (kHz)	Gain (dB)		
	Min.	Typ.	Max.
92			- 30
126.45	- 5	- 3	- 2
Ref 132.45		0	
138.45	- 5	- 3	- 2
180			- 30

Intermediate FrequencyFilter

Frequency (kHz)	Gain (dB)		
	Min.	Typ.	Max.
2.4			- 35
4.3	- 4	- 3	- 1
Ref 5.4		0	
6.5	- 5	- 3	- 2
11.6			- 35

7537H-07 TBL

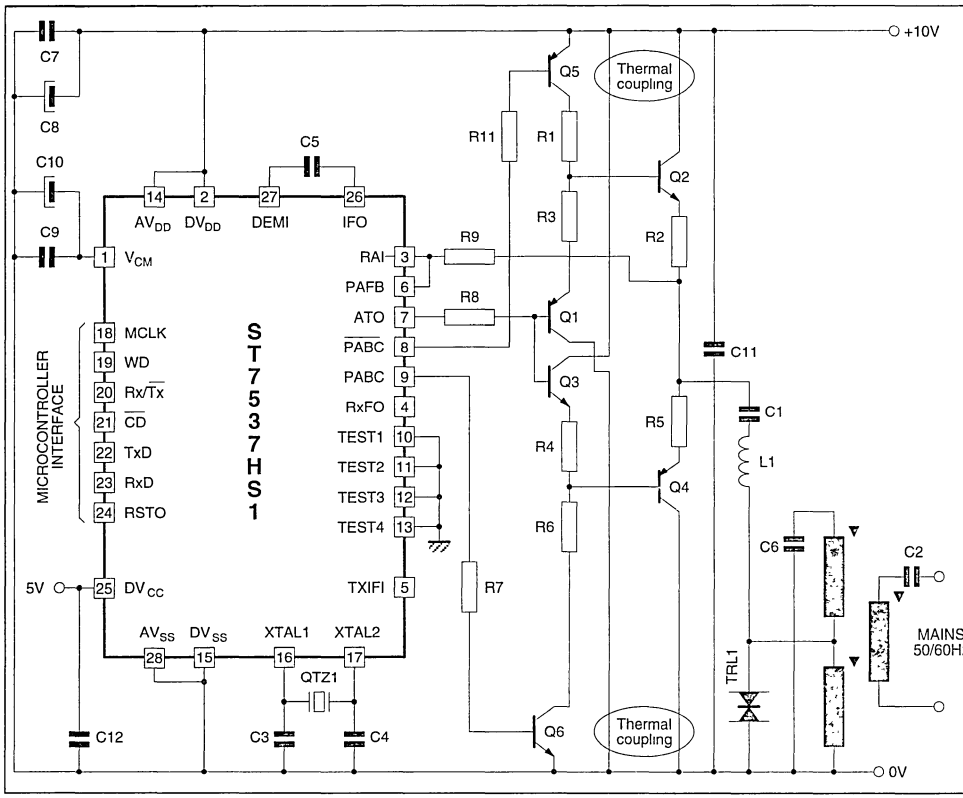
APPLICATION SCHEMATIC INFORMATIONS

RESISTORS			CAPACITORS			
R1	180Ω		C1	1µF		Ceramic 50
R2	2.2Ω		C2	470nF		Paper, class X2
R3	2.2Ω		C3 (2)	22pF	10%	Ceramic 10V
R4	2.2Ω		C4 (2)	22pF	10%	Ceramic 10V
R5	2.2Ω		C5	100nF	10%	Ceramic 10V
R6	180Ω		C6	6.8nF	5%	Plastic Film 50V
R7	47kΩ		C7	100nF		Ceramic 10V
R8	1kΩ		C8	2.2µF		
R9	1kΩ	5%	C9	100nF		Ceramic 10V
R11	47kΩ		C10	2.2µF		
INDUCTOR			C11 (1)	100nF		Ceramic 10V
L1	10µH	≅ 1.5Ω	C12 (1)	100nF		Ceramic 10V
TRANSISTORS			TRANSIL			
Q1 : 2N2907 Q2 : 2N2222 Q3 : 2N2222 Q4 : 2N2907 Q5 : 2N2907 Q6 : 2N2222			TRL1 : SGS-THOMSON P6KE6V8CP			
			TRANSFORMER			
			TR1 : TOKO T1002 N			
			CRYSTAL			
			QTZ1 : 11.0592MHz parallel resonance			

7537H-08 TBL

Notes : 1. These capacitors might not be necessary if the overall power supplies decoupling is sufficient.
2 The value of these capacitors depends on the crystal parameters.

APPLICATION SCHEMATIC DIAGRAM



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

ST7536

By Joël HULOUX

SUMMARY

I - INTRODUCTION TO THE ST7536

The ST7536 is a half duplex synchronous FSK-modem, and has been designed to operate on powerline networks. For a complete communication system, a micro-controller and a powerline-interface (PLI) are needed (see Figure 1).

Such a system is able to transmit and receive on 4 different channels with 2 different data rates (600 and 1200 baud). The baudrate (BRS) and channel (CHS) selection is made, according to the table 1:

Table 1

BRS	CHS	Bitrate	Xmit Freq (KHz) TxD = 1	Xmit Freq (KHz) TxD = 0
0	0	600	81.75	82.35
0	1	600	67.20	67.80
1	0	1200	71.40	72.60
1	1	1200	85.95	87.15

The ST7536 is a half duplex modem, as it has two operation modes; receive or transmit data. The mode selection is made with a Rx/$\overline{Tx}$ control input.

Data input and output are related to the clock signal; it's a synchronous modem. This clock signal is generated by the ST7536.

Only a few external components have to be added for full operation of the ST7536: a crystal, four resistors and five capacitors.

II - ST7536 DESCRIPTION

The ST7536 is a single chip modem; all the electrical circuits needed for a complete modem are inside the chip. The modem is available in 28 pins PLCC (see Figure 2).

In transmit mode the Transmit Data (TXD) is sampled on the positive edge of the clock (CLR/T). Then the data enters the FSK modulator. The frequency on which this modulator operates is set by the time base and control logic. In normal operation the multiplexer (MUX) selects the FSK modulator signal to be send to the transmit filter. This filter is a switched capacitor band-pass filter.

The time base and control logic uses the Automatic Frequency Control (AFC) to set this filter at the transmit frequency, corresponding to the selected channel. After filtering, the transmit signal is sent to an Automatic Level Control (ALC). This control is used to overcome problems with line impedance variations. The powerlines on which the modem has to operate, have variations in their line characteristics, which are very frequent and totally unpredictable. The automatic level control uses a feed back signal (ALCI) from the powerline interface to adjust the transmit output (ATO).

In receive mode the signal enters the chip on the Receive Analog Input (RAI). The received signal is filtered in the receive band-pass filter. It's just like the transmit filter , a switched capacitor filter.The automatic frequency control is used to set it on the right frequency. After being amplified the signal is down converted and filtered in the intermediate frequency band-pass filter. The resulting signal is sent to the FSK demodulator. The coupling of the intermediate frequency filter output (IFO) to the FSK DEModulator Input (DEMI) is made by an external capacitor which cancels an eventual offset voltage. A clock recovery circuit extracts the receive clock (CLR/T) from the demodulated output (RXDEM) of the FSK demodulator. Synchronous received data (RXD) is delivered on the positive edge of the clock.

A time base section delivers all the internal clock signals from a crystal oscillator running at 11.0592 MHz. The crystal is connected between the XTAL1 and XTAL2 pins. It is also possible to provide directly a clock signal on XTAL1 instead of using a crystal.

To debug the chip and test external circuits the ST7536 provides some test options. The transmit band-pass filter can be observed using a direct input on the filter. This input (TXFI) is selected by the multiplexer if TEST4 = 1. The Receive band-pass Filter Output (RXFO) is provided at pin 25. Finally the clock recovery can be observed when TEST1 = 1. In this case the TEST3 input gives a direct input to the clock recovery block.

Figure 1

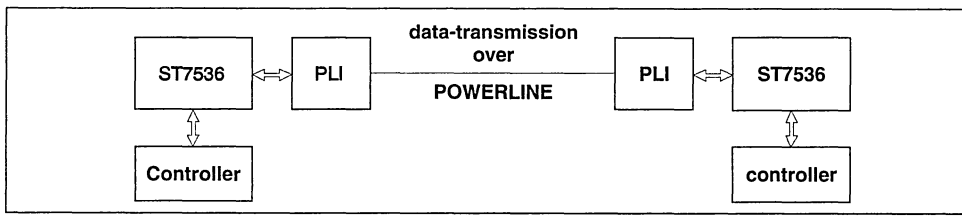
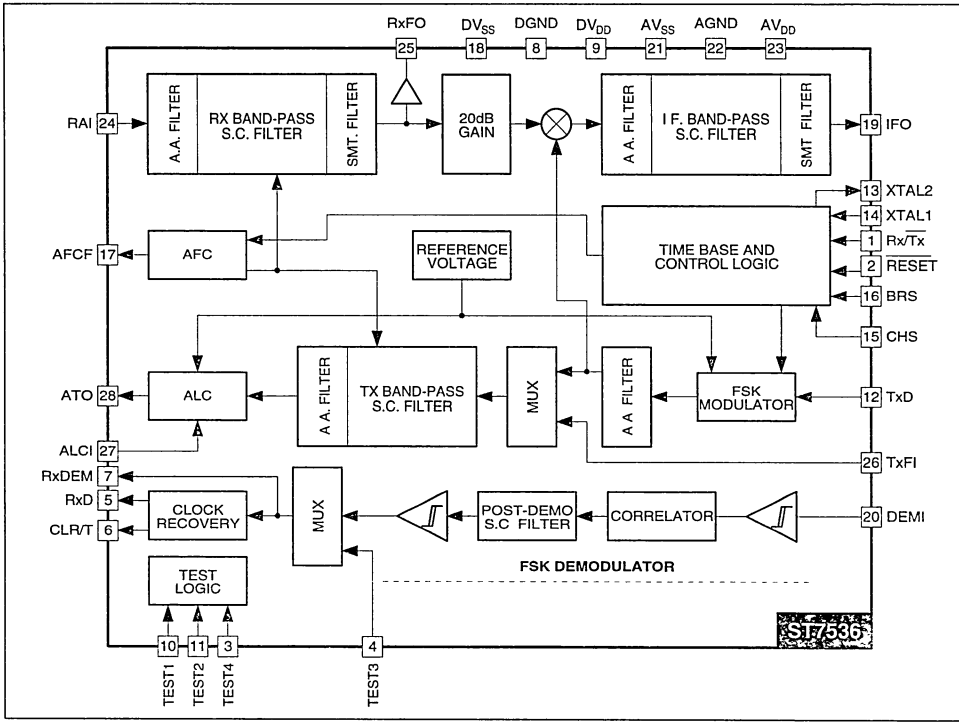


Figure 2 : Block Diagram



III - ST7536 PIN DESCRIPTION

The pin decription is not given in numerical order, but the pins are described in relation with their function and consequently sometimes with other pins.

- power supply input
- channel selection
- crystal oscillator input
- AFCF stabilisation
- automatic level control input
- data input and output
- test inputs
- IFO/DEMI output/input
- transmit output and receive input
- Rx/Tx control input
- reset input

III.1 - Power Supply Input

- pin 8 (DGND) : Digital ground (0V)

- pin 9 (DV_{DD}) : Digital positive supply voltage (+5V)

- pin 18 (DV_{SS}) : Digital negative supply voltage (-5V)

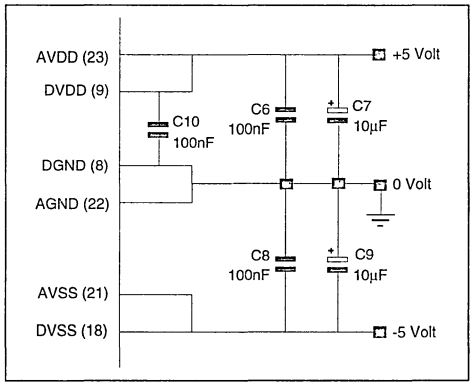
- pin 21 (AV_{SS}) : Analog negative supply voltage (-5V)

- pin 22 (AGND) : Analog ground (0V)

- pin 23 (AV_{DD}) : Analog positive supply voltage (+5V)

Internally the ST7536 has separated power supplies: the digital and analog circuits are separated. Externally the power supplies should be connected together. For decoupling, both the positive and negative supplies are decoupled with 2 capacitors. C6 and C7 decouple the positive, C8 and C9 the negative supplies. For proper operation the digital positive supply voltage should be decoupled with a capacitor (C10) mounted close to pin 9. C6,C8 and C10 are 100nF/16V ceramic capacitors, C7 and C9 10µF/16V tantal capacitors (see Figure 3).

Figure 3



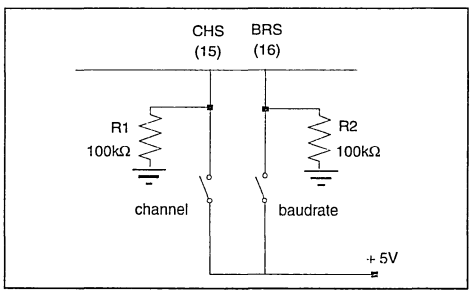
III.2 - Channel Selection

- **pin 15 (CHS)** : Channel selection input
- **pin 16 (BRS)** : Baudrate selection input

Both inputs are digital inputs (0/+5V). The ST7536 operates with two bitrates: 600 and 1200 baud. These bitrates are selected with pin 16 (BRS). For both bitrates the ST7536 offers two channels, which are selected with pin 15 (CHS).

A logical "0" is represented by 0V, a "1" by +5V. R1 and R2 are pull-down resistors, creating a logical "0". Closing a switch gives a "1". The selection is made according to table I.

Figure 4



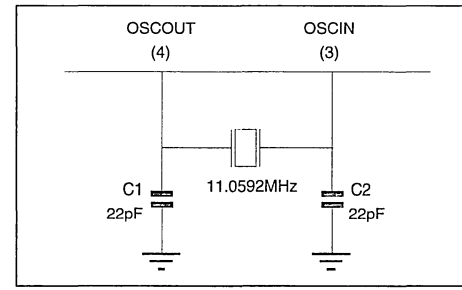
III.3 - Crystal Oscillator Input

- **pin 13 (XTAL2)** : Crystal oscillator output
- **pin 14 (XTAL1)** : Crystal oscillator input

The internal crystal oscillator of the ST7536 needs an external crystal. This one should be a 11.0592MHz crystal. Two capacitors (C1 and C2) have to be added for proper operation. They are typically 22pF/10V ceramic capacitors.

It is also possible to connect directly a clock signal to the oscillator input, in this case the crystal and the capacitors should be removed. On the application board this option is not used. The ST7536 clock signal is the time reference of the system.

Figure 5

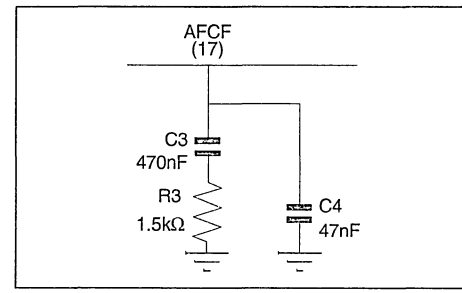


III.4 - AFCF Stabilisation

- **pin 17 (AFCF)** : Automatic frequency control output

In the ST7536 an automatic control section adjusts the central frequency of the receive and transmit band-pass filters. The stability of this section has to be ensured with an external RC network.

Figure 6



III.5 - Automatic Level Control Input

- **pin 27 (ALCI)** : Automatic level control input

The output stage of the transmit path consists of an automatic level control (ALC). It offers the possibility to keep the output voltage of the power amplifier independent of variations of the powerline network. The impedance of these networks can be anywhere in the range of 5 - 100Ω. If the impedance of the powerline changes, the output of the amplifier will change. With the ALC input it is possible to correct these output variations. To control the output of the powerline interface a feed-back signal is

needed. This signal is sent through an amplifier. The automatic level control can decrease the maximum transmit output in 32 steps of 0.84dB. The gain range is 0dB → -26dB. A peak detection is done on the signal presented on the ALCInput and the ALC compares it to two reference voltages, VT1 (1.87V) and VT2 (2.12V).

If max. VALCI < VT1 the next gain is increased by 0.84dB.

If VT1 < max. VALCI < VT2 there is no gain change. If VT2 < max. VALCI the next gain is decreased by 0.84dB.

The gain of the feed-back amplifier is such that the feed-back signal peak voltage falls between V_{T1} and V_{T2}.

Example:
The wanted interface output voltage is 0.5V(peak).
For a 0.5V output peak voltage

$$G = \frac{V_{out\ peak}}{\left(\frac{V_{T1} + V_{T2}}{2}\right)} = \frac{0.5}{2} = 4\ (12dB).$$

Then the feed-back amplifier should have a gain of 4x (= +12dB). The ST7536 starts up. VALCI = 0V (VALCI < VT1). The ATO output is increased with a gain of +0.84dB. On a certain moment the output voltage over the powerline will become 0.5 V(peak). This signal is amplified to 2.0 V(peak). Then the ALC stops increasing the ATO output, which will remain at its actual level. If the line impedance increases, the power amplifier of the interface might deliver more output voltage. If the output voltage of this amplifier increases, the ALCI voltage will be higher than VT2. The ALC will then immediately decrease the ATO output. And so the output of the interface can be made independent of impedance variations of the powerline.

Of course this will operate only if the power amplifier in the interface is able to drive all the impedances at the required output voltage. Let's say the impedance of the line becomes 0.1Ω. The ALC will increase the output of the ATO. But if the power amplifier is not able to drive such low impedances, the only result will be an output signal with a large distortion. Therefore on the application board the ALCInput is set at 0V with a resistor (R4). The ATO will be always at maximum output (1.25 Vrms). The powerline interface has been designed to drive all impedances from 0.5 - 100Ω with this input. To be able to do some experiments with the ALC, a resistor is used to set the ALCI at 0V. It gives the possibility to inject a signal on the ALCI. This would not have been possible if on the printed circuit board a short circuit to ground had been made (see Figure 7)

III.6 - Data Input and Output

- **pin 5 (RxD)** : Synchronous receive data output
- **pin 6 (CLR/T)** : Receive and transmit clock
- **pin 7 (RxDEM)** : Demodulated data output
- **pin 12 (TxD)** : Transmit data input

The ST7536 is a synchronous modem; data input and output are related to the clock (CLR/T). In transmit mode the ST7536 generates this clock signal. The transmit data are sampled on the positive edge of CLR/T. Therefore the TxD should be valid at that moment. In receive mode the demodulated (receive) data is available at pin 7 (RxDEM). A clock recovery circuit extracts the clock signal from the demodulated data and delivers synchronous data (RxD) on the positive edge of CLR/T.

On the application board the RxDEM data output is not used. All the data signals from and to the ST7536 (RxD, TxD) are related to the clock (CLR/T) (see Figure 8).

Figure 7

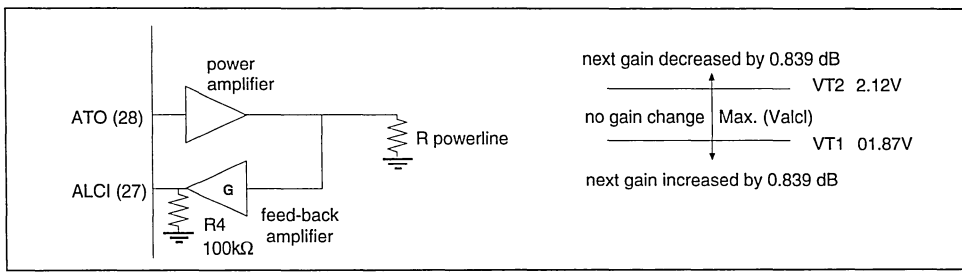
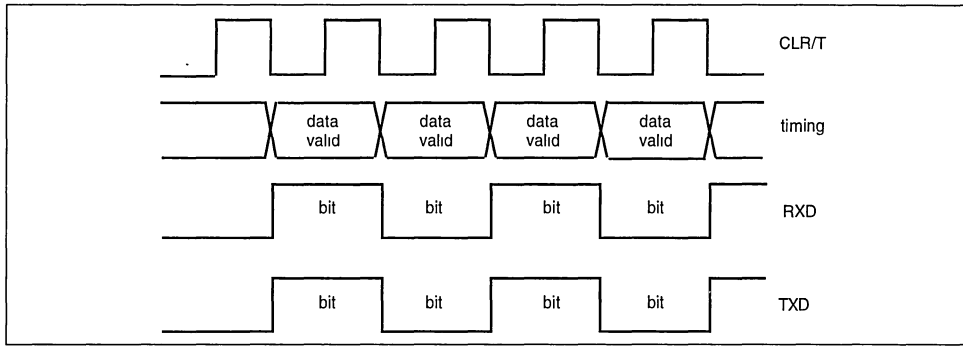


Figure 8



III.7 - Test Inputs

- **pin 3 (TEST4)** : Test input, with a "1" on this pin the multiplexer selects the transmit band-pass filter input (TXFI).
- **pin 4 (TEST3)** : Test input which gives a direct acces to the clock recovery circuit.This input is selected when TEST1 = "1".
- **pin 10 (TEST1)** : Test input, a "1" on this pin cancels the automatic switching from transmit to receive mode, and validates the TEST3 input to the clock recovery circuit.
- **pin 11 (TEST2)** : Test input, a "1" on this pin reduces the automatic switching time (from transmit to receive mode) to 1.48 msec.

On the application board TEST 2/3/4 are not used, and pin 3, 4, and 11 are therefore set at 0V. With a switch TEST1 can be set at "0" or "1". See also the Rx/$\overline{Tx}$ control input.

III.8 - IFO/DEMI Output / Input

- **pin 19 (IFO)** : Intermediate frequency filter output
- **pin 20 (DEMI)** : FSK demodulator input

The connection between the intermediate frequency filter output and the FSK demodulator input should be made externally with a capacitor (C5, 1µF/10V).

III.9 - Transmit Output and Receive Input

- **pin 24 (RAI)** : Receive analog input
- **pin 28 (ATO)** : Analog transmit output

Pin 24 is the receive input of the ST7536. The receive output of the powerline interface should be connected to this pin. The maximum input voltage is $2V_{RMS}$. The receive sensitivity of the ST7536 is $2mV_{RMS}$ f on channel 1 and 2 (600 baud), and $3mV_{RMS}$ on channel 3 and 4 (1200 baud).

Pin 28 is the transmit output of the ST7536. The transmit input of the powerline interface should be connected to this pin. The ATO output is regulated by the ALCI circuit. The maximum output voltage is $3.5V_{PP}$. The second harmonic distortion is about -53dB.

III.10 - Rx/$\overline{Tx}$ Control Input

- **pin 1 (Rx/$\overline{Tx}$)** : Receive or transmit mode selection input

The ST7536 is a half duplex modem and has therefore two operation modes: receive and transmit. This mode selection is done with the Rx/$\overline{Tx}$ input. The transmit mode is selected when Rx/$\overline{Tx}$ is "0". If Rx/$\overline{Tx}$ is held at "0" longer than 3 seconds, the ST7536 switches back to receive mode. To set the ST7536 again in transmit mode, Rx/$\overline{Tx}$ should be held at "1" for a minimum of 3 microseconds before being set to "0".

The carrier activation time is 1 msec.

To be able to observe the transmit output of the ST7536 on the power line interface for a longer time than 3 seconds it is possible to use the test 1 Input. If this input is set at "1" the automatic switching is disactivated.

Then it is possible to transmit a signal but not to receive.

III.11 - Reset Input

- pin 2 (RESET) : logic reset and power-down input

When this input is set at "0" the ST7536 is in power-down mode. All the internal logic is then reset. For normal operation this input should be set at "1". On the application board this input is controlled by the micro-controller.

IV - POWERLINE INTERFACE

The power line interface (PLI) connects the ST7536 to the powerlines.The following PLI has been designed according to the ENEL (italian electricity distributor) specifications : (This PLI is suitable to CENELEC european specification and the FCC USA spec) (see Figure 9)

transmit output :

R powerline > 5Ω → 1 - 2 V_{RMS}

R powerline < 5Ω → 200-400mA_{RMS}

Second Harmonic Distortion ← 72dB for R powerline = 18Ω

receive sensitivity : 1.5mV_{RMS}

In transmit mode the powerline interface amplifies and filters the transmit signal (ATO) from the ST7536. The maximum output current that can be taken from ATO is 1mA. Therefore a buffer is used to protect the ST7536 and in order to drive the next stages in the powerline interface. The Second Harmonic Distortion (HD2) of the transmit signal from the ST7536 is -53dB. To suppress the harmonics a low pass filter (LPF) is used. The filtered signal is then sent to a power amplifier, which must drive powerlines with impedances from 1 to 100Ω,via the transformer. The transformer is not only used to put signals on the powerlines. It's also used as a band pass filter, in order to suppress the second harmonic of the transmit signal to a level of less than -72dB.

In receive mode the transformer extracts the signal from the powerline. Before sending it to the receive input (RAI) of the ST7536, it is amplified with a level of 34dB in the preamplifier.

The buffer and power amplifier are switched off in receive mode,in order to avoid the low output impedance of the power amplifier attenuating the received signals.

IV.1 - Buffer and Low Pass Filter

These two functions are build up around UA1 (see Figure 10).

Figure 9

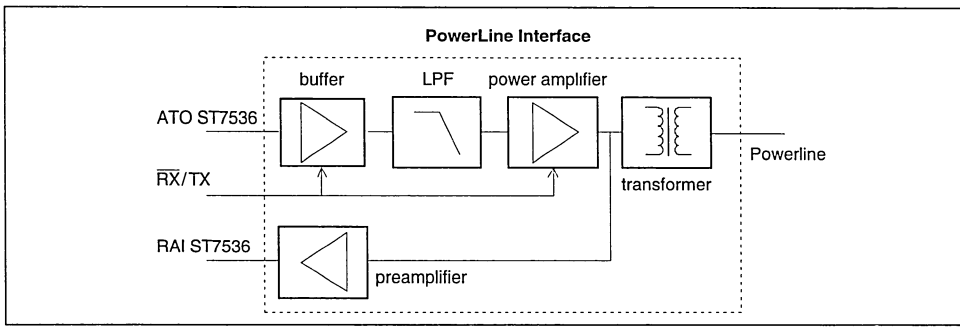
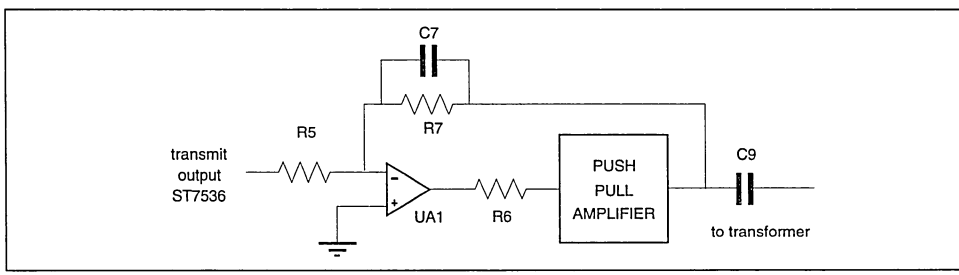


Figure 10



A feed back from the output of the power amplifier to the operational amplifier is done with R7/C7. This gives a low pass function and therefore the possibility to create a low pass filter.The ST7536 operates on 4 channels : 67, 72, 82 and 86kHz. With R7 and C7 the cut off frequency of this filter is set.If this frequency is set at 75kHz, the difference between 75kHz and 150kHz (second harmonic) signals is only 3dB,because such a filter has already an attenuation of 3dB at the cutoff frequency (see figures below).

Figure 11

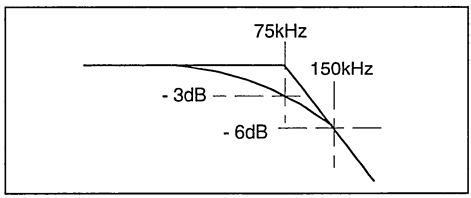
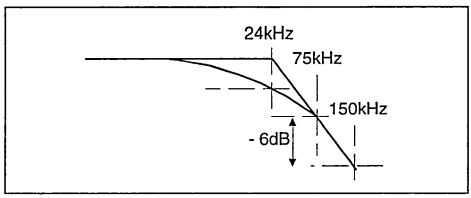


Figure 12



To ensure an attenuation of 6dB of the second harmonic, the cut off frequency has been set at 24kHz.

With R7 = 10kΩ
f = 1/(6.28*R7*C7) = 24kHz
C7 = 680pF

The ratio R7/R5 provides sufficient amplification on the transmit frequency, to drive the power amplifier at optimum performances.The frequency differences of the four channels result in a different output of the low pass filter. Therefore the ratio of R7/R5 is not the same for all the four channels.

Channel	R7 (Ω)	R5 (Ω)	ATO (Vpp)
1	10k	1500	3.3
2	10k	1800	3.6
3	10k	1800	3.5
4	10k	1500	3.2

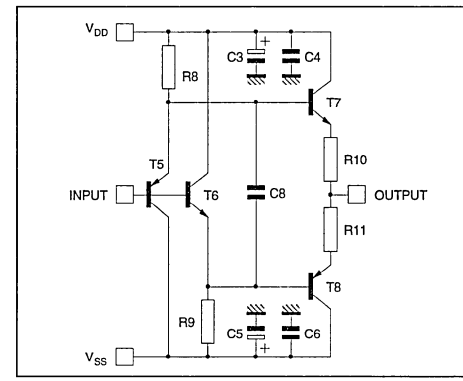
The connection of the operational amplifier to the power amplifier is done with R6. This resistor is added to avoid oscillation. Without this resistor stable operation cannot be guaranteed. The value of R6 is determinated with experiments to be 330Ω.

An other function of R6 is to increase the load impedance seen by the operational amplifier. The impedance is R6 plus the input impedance of the power amplifier. If this impedance is to low the operational amplifier will not be able to drive the power amplifier in optimum performances. The maximum voltage swing will decrease and the second harmonic distortion will increase. Different operational amplifiers have been tested. The TL071C gives the best performances.

IV.2 - Power Amplifier

The power amplifier increases the output signal of the operational amplifier and low pass filter (UA1).

Figure 13



The input impedance is increased because it's multiplied by the Beta of T5/6, which are no longer used as diodes. Therefore R8 and R9 could be decreased, to deliver more current to T7/T8. The optimum performances of the amplifier were obtained with a value of 820Ω for R8 and R9. An other solution to deliver more current to the output transistors is the addition of C8. It will decrease the input impedance, but also deliver extra current to T7 by T6, and to T8 by T5. Other transistors have been used also a BD237 for T6/T7, a BD238 for T5/T8. These transistors can deliver more output power, and are not much expensive than the 2N2222/2N2907. Furthermore, the collectors are connected to the (metal) package. This gives the possibility for a mechanical connection of T5/T8 and T6/T7. This will result in the same temperature in both transistors, what will avoid thermal runaway. To decouple the power supplies C3/C5 (22µF/16V) and C4/C6 (100nF/16V) are used, mounted close to T7 and T8.
Using this configuration, it is possible to provide 1 → 2 V_{RMS} in powerlines with impedances from 5 → 100Ω.

IV.3 - Transformer

A transformer is used to connect the power amplifier and the preamplifier to the powerline.This transformer has to :

- separate the rest of the interface from the powerline
- put the transmit signal on the powerline
- extract the received signal from the powerline
- filter the 50/60Hz signal coming from the powerline
- filter the second harmonic of the transmit signal.

The transformer is a TOKO T1002N,which has two primary windings and one secondary winding. The ratios of the windings are 4:1:1 (turns) (see also the Figure 14). Typical values of the transformer are:

L1t windings : 9.4 µH
L4t winding : 140 µH

The primary windings of the transformer are used to create a bandpass filter. The resonance frequency is set at the transmit frequency with C10/C11. These capacitors are in parallel with the primary windings (1t/4t). The equivalent value for those two windings can be calculated according to:

$$Leq = L1t + L4t + 2M$$

$$M = k \cdot \sqrt{L1t \cdot L4t} \quad \left(k = \frac{1}{\sqrt{2}}\right) \qquad (16)$$

With the given values:

$M = (9.4\,\mu H * 140\,\mu H)^{0.5}$
$= (1316\,\mu H)^{0.5} = 36.3\,\mu H$
$Leq = L1t + L4t + 2 \cdot (L1t \cdot L4t)^{0.5}$
$= 9.4\mu H + 140\mu H + 2 \cdot 25.6\mu H = 200\mu H$

The resonance frequency of this LC network is dependent of Ceq = Cp = C10//C11 and Leq according to:

$$f_{res} = \frac{1}{2\pi \times \sqrt{L_{eq} \cdot C_p}} \qquad (17)$$

$$C_P = \frac{\left(\frac{1}{2\pi \cdot f_{res}}\right)^2}{Leq} \qquad (18)$$

As this filter is very sharp, there are different values for Cp on each (transmit) frequency.

channel 1 : f = 82kHz → Cp = 18nF = 10nF // 6.8nF
channel 2 : f = 67kHz → Cp= 28nF = 22nF // 6.8nF
channel 3 : f = 72kHz → Cp = 24nF (only 1 capacitor)
channel 4 : f = 86kHz → Cp = 17nF = 10nF // 5.6nF

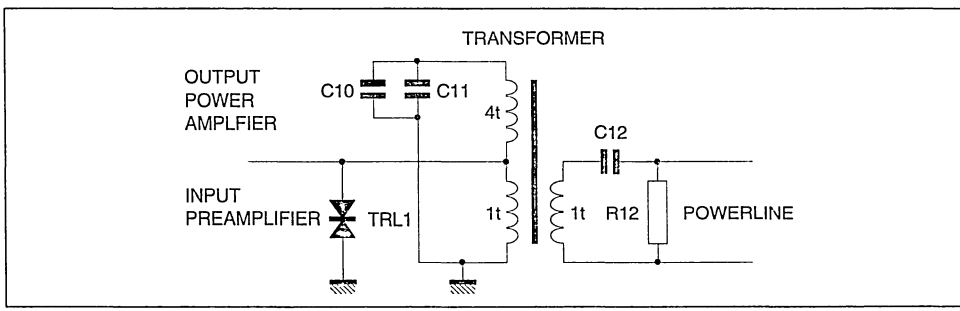
On channel 3 only 1 capacitor is needed and therefore C11 doesn't exist. On a printed circuit board the capacitors should be mounted close to the transformer. In order to get the best filter performances.The capacitors (C10/C11) have to be linear, such as the KS (styroflex) types.

C12 is used to filter the 50/60Hz signal from the powerline. The capacitor filters low frequencies 50/60Hz and lets the high (transmit) frequencies pass. The capacitor is a class X2 capacitor. These capacitors have a short circuit protection, which is absolutely necessary,because in case of a short circuit in the capacitor, the 50/60Hz filtering is lost, and the powerline interface will be destroyed, or might be dangerous for persons working with the interface and the ST7536.

As a final protection against any possible spikes, a transil (TRL1) is used. It is a 6.8V bipolar type. If a voltage 6.8V appears, the transil will act as a short circuit to ground, protecting the other parts of the powerline interface from damage.

R12 is added to discharge C12 after disconnecting the interface from the powerline. Without this resistor, C12 will not be discharged and shock hazard might occur if someone touches the powerline connector. This resistor is only usefull in evaluation systems. In all other cases when disconnecting from the powerline never takes place R12 can be removed.

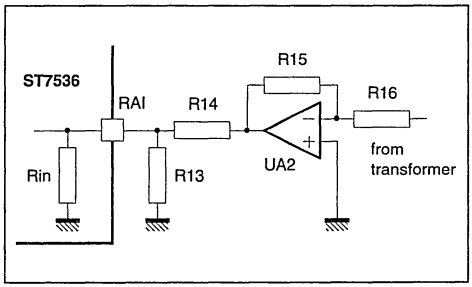
Figure 14



IV.4 - Preamplifier

Receive signals on the powerline are extracted by the transformer and (pre)amplified before sending them to the Receive Analog Input (RAI) of the ST7536. This is done to have, according to the specifications, a receive sensitivity of 1.5mV$_{RMS}$. The sensitivity of the ST7536 is 2mV$_{RMS}$.for channel 1 & 2, and 3mV$_{RMS}$ for channel 3 & 4. To increase the sensitivity the received signal is filtered in the transformer, and then amplified with a gain of 40dB. A limiter is used to protect the ST7536 against signals > 2V$_{RMS}$.

Figure 15



In receive mode the power amplifier is virtually disconnected from the power supply, in order to avoid its low output impedance attenuating the received signals. Signals that are extracted from the powerline are filtered in the transformer, in the same way that the transmitted signals.

After filtering, the signals are amplified. This is done with UA2, an inverting amplifier. The gain of this amplifier is set with R15 and R16.

gain = R15 / R16 = 100k / 1k = 100 x = +40dB

The maximum input level at the RAI is 2V$_{RMS}$.Therefore the signals coming from the preamplifier have to be limited to avoid transmodulation to the ST7536. Amplifier UA2 operates with a power supply of -5V and +5V. The maximum output voltage of the amplifier is then ± 4V. With R13 and R14 a simple limiter has been created. The output voltage of this limiter is the voltage over R13. The input resistance of the RAI (Rin) is 100kΩ.

The gain of the limiter
= (R$_{IN}$//R13) / (R$_{IN}$//R13 + R14)
= (100k//47k) / (100k//47k + 47k)
= 0.4 x (= -8dB)

With a maximum output of the amplifier of 4V, the maximum output of the limiter is set at 0.4 x 4V = 1.6V. Strong input signals are clamped by UA2, but tests showed that this clamping has no effect on correct demodulation.

The total gain of the preamplifier is: +40dB + -8dB = +32dB providing the required receive sensitivity of 1.5mV$_{RMS}$.

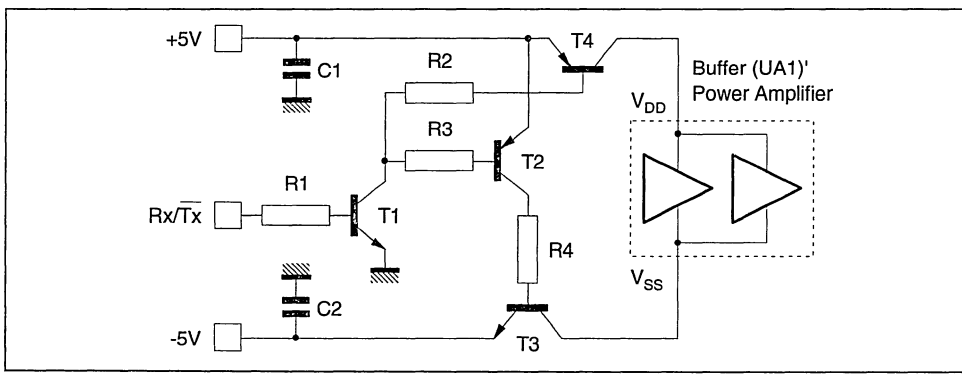
IV.5 - Power on/off Switch

The powerline interface has two operation modes: transmit and receive. Normally the ST7536 system (and therefore the interface) is in received mode, waiting for commands or data requests from the master system.The interface will be used in transmit mode ,only when the system has to respond to the master,

To save energy costs, the buffer and power amplifier in the transmit path are switched off. Also if the interface is used in a master system, which will be often in transmit mode, this switching can be usefull.

A second reason to switch off the transmit power amplifier is the fact that its low output impedance will attenuate the incoming signals in receive mode. Therefore the power amplifier is virtually disconnected from the power supply (see Figure 16).

Figure 16



Switching the positive (V_{DD}) and the negative (Vss) input voltage is done with T3 & T4. If these transistors are switched off the high resistance of the collectors will provide the virtual disconnection. In transmit mode these transistors are switched on, and the voltage lost over the transistors (V_{CE}) will be 0.2V.

The Control of the switch is done with a Rx/$\overline{Tx}$ control line from the controller. In transmit mode this line is +5V, in receive mode 0V. The +5V will open T1, which delivers the base current for T2 and T4. T3 is switched by T2.

In transmit mode the buffer and power amplifier will operate with HF-signals (the transmit signals have frequencies 67...86kHz). Therefore the input (± 5V) of the switching transistors has to be decoupled. This is done with C1 and C2, which have both a value of 100nF.

R1 is 47kΩ, to create a high input impedance. R2, R3 and R4 are 270Ω. T1 and T3 are a 2N2222, T2 and T4 the equivalent pnp version; a 2N2907. These transistors can deliver a maximum current of 0.8A, more than enough for the buffer and power amplifier.

IV.6 - Building-up the Powerline Interface

The whole described parts make a complete powerline interface. The interface has to be connected to the ST7536 as described before.

Because the interface is supposed to operate with the ST7536, the input and output names correspond to the related pin names of the ST7536. for instance: the ATO pin of the ST7536 should be connected to the ATO pin of the powerline interface.

The ATO and RAI are the analog output and input from/to the ST7536. The Rx/$\overline{Tx}$ control input is connected to the controller. The controller switches the interface from transmit mode to receive mode and vice versa. The +/-5 Volt inputs are connected to the power supply connections of the application board. These inputs are HF-decoupled on the board. See also the schematic of the ST7536. If the interface has to operate separated from the application board, using an external power supply, the ± 5V inputs should be decoupled with four capacitors (see Figure 17)

The operation mode of the interface is set with the Rx/$\overline{Tx}$ input line. A high input (+5V) on this line selects the transmit mode, a low input (0V) selects the receive mode. A micro-controller has to be used to control this input.

The 'power line' outputs are the powerline connections. On the application board these connections are located close to C12 and the transformer, to avoid long tracks carrying high voltage.

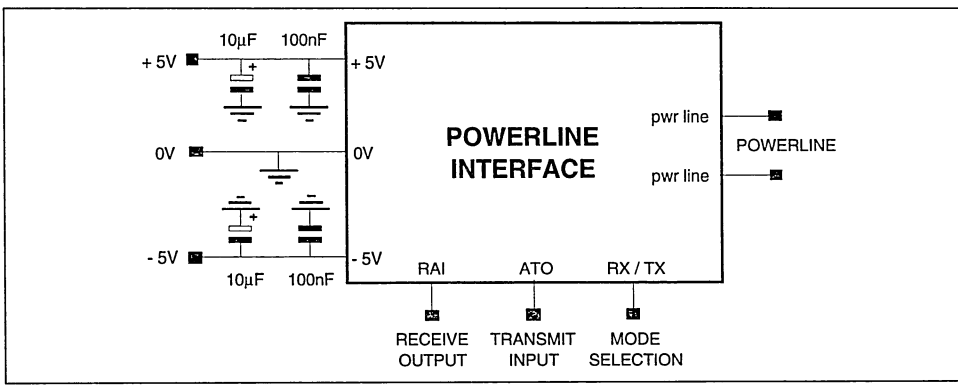
IV.7 - Performances of the Powerline Interface

The following tests have been done on the powerline interface :

- power consumption
- transmit output
- receive sensitivity

All the tests are done with the powerline interface connected to the ST7536.

Figure 17



IV.7.1 - Power consumption

The power consumption is measured both in transmit and receive mode.
In both modes the powerline has been simulated with a 5Ω resistor (worse case simulation). In transmit mode the data input (TxD) was a logical 0 (0V).

The results remained the same for the four channels.

The current consumption :

The input voltage : - 5.00V, + 5.00V
transmit mode : - $150mA_{RMS}$, + $180mA_{RMS}$
receive mode : - $1mA_{RMS}$, + $1mA_{RMS}$

The power consumption :

transmit mode : -5V x -150mA + +5V x +180mA
0.75W + 0.9W = 1.65W
receive mode : -5V x -1mA + +5V x +1mA
0.005W + 0.005W = 0.01W
(= 10mW)

In transmit mode the powerline interface delivered 0.340 W into a 5Ω load. With an input of 1.65 W the efficiency is 20%. This does not imply a waste of energy. A ST7536 system is almost allways in receive mode, and the lost of energy is consequently limited.

In receive mode the buffer and the power amplifier are switched off. Power is only consumed by the preamplifier. This explanes the low power consumption in receive mode.

Test equipment : Keithley 165 Multimeter
Test conditions : T = +25°C

IV.7.2 - Transmit output

The transmit output of the powerline interface is measured with the powerline simulated by resistors.

The interface is tested on the four channels. On each channel the ST7536 uses two signals : one for TxD = 1 (lower freq.) and one or TxD = 0 (higher freq.) Therefore the output on each channel is measured for TxD = 1 and TxD = 0. This makes 4 (channels) x 2 (TxD 0/1) = 8 signals to test.

The powerline is simulated with resistors. Six different impedances are tested : R = 0.5, 1, 5, 10, 50, 100Ω.

A spectrum analyzer is used to test the output of the powerline interface It measures the output power and generates a frequency spectrum plot. With this plot the harmonic distortion can be calculated (see Figure 18)

Test results. (see ANNEXE B)

With the spectrum analyzer the output power on the transmit frequency (H1) is measured. Then the power of the harmonics is measured. The difference between those two signals is the harmonic distortion.

Example : TxD = CHS = BRS = 0
(channel 1, txd = 0 → 81.75kHz.)
R powerline = 5Ω.

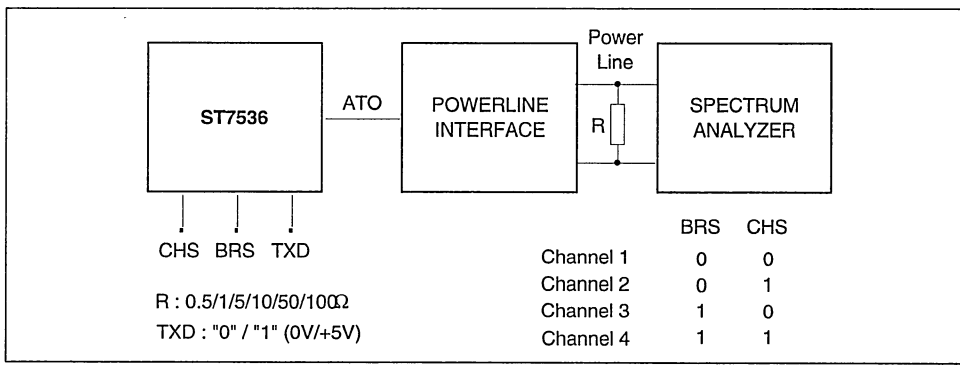
H1 : f= 81.75kHz, measured power = +15.2dBm.
H2 : f = 163.5kHz, measured power = -58.8dBm.

The difference between H1 and H2 is + 15.2dB - -58.8dB = 74dB.
The second harmonic of the signal is in this case suppressed to a level of -74dB (compared to H1).

The measured output power of H1 = +15.2dBm. Then the output voltage can be calculated.

0 dBm is 1mW power into a resistor of 50Ω. So +15.2 dBm is 33mW power into a resistor of 50Ω. Vout(rms) is therefore (33mW * 50Ω)^0.5. In this case the output voltage is $1.29V_{RMS}$.

Figure 18



The output current is also calculated :
Iout(rms) = Vout(rms) / R.
For example; the output voltage with R powerline = 0.5Ω is 0.18V_{RMS}. Then the output current is 360mA_{RMS}.

Channel 1 : 82kHz

Rline (Ω)	Output (V_{RMS}) TxD = 1	Output (V_{RMS}) TxD = 0	H2 (dB) TxD = 1	H2 (dB) TxD = 0
0.5	0.18	0.18	-51	-54
1	0.31	0.31	-51	-55
5	1.29	1.29	-74	-76
10	1.70	1.68	-77	-81
50	2.06	2.02	-74	-77
100	2.09	2.06	-74	-76

Channel 2 : 67kHz

Rline (Ω)	Output (V_{RMS}) TxD = 1	Output (V_{RMS}) TxD = 0	H2 (dB) TxD = 1	H2 (dB) TxD = 0
0.5	0.16	0.16	-67	-68
1	0.28	0.28	-68	-68
5	1.21	1.20	-75	-75
10	1.70	1.65	-78	-75
50	2.16	2.11	-83	-75
100	2.21	2.16	-84	-75

Channel 3 : 72kHz

Rline (Ω)	Output (V_{RMS}) TxD = 1	Output (V_{RMS}) TxD = 0	H2 (dB) TxD = 1	H2 (dB) TxD = 0
0.5	0.16	0.16	-65	-67
1	0.28	0.28	-66	-67
5	1.17	1.16	-73	-76
10	1.62	1.56	-75	-79
50	2.02	1.95	-74	-75
100	2.06	2.00	-73	-75

Channel 4 : 86kHz

Rline (Ω)	Output (V_{RMS}) TxD = 1	Output (V_{RMS}) TxD = 0	H2 (dB) TxD = 1	H2 (dB) TxD = 0
0.5	0.17	0.17	-56	-52
1	0.29	0.30	-60	-57
5	1.21	1.18	-77	-77
10	1.55	1.53	-82	-82
50	1.86	1.80	-82	-78
100	1.88	1.84	-80	-78

Summary of the test results :

Channel 1 :
R < 5Ω : 310-360mA_{RMS}
R > 5Ω : 1.3 - 2.1V_{RMS}
R 10/50Ω : H2 < -74dB
Channel 2 :
R < 5Ω : 280-320 mA_{RMS}
R > 5Ω : 1.2 - 2.2 V_{RMS}
R 10/50Ω : H2 < -75dB
Channel 3 :
R < 5Ω : 280-320mA_{RMS}
R > 5Ω : 1.2 - 2.0V_{RMS}
R 10/50Ω : H2 < -74dB
Channel 3 :
R < 5Ω : 290-340mA_{RMS}
R > 5Ω : 1.2 - 1.9V_{RMS}
R 10/50Ω : H2 < -78dB

With impedances < 5Ω the output current is for all the four channels in the range 280-360mA_{RMS}.

The output voltage on impedances > 5Ω is both on channel 3 and 4 in the range 1.2 - 2.0V_{RMS}. On channel 1 and 2 it's in the range 1.2 - 2.2V_{RMS}.

On all the channels the second harmonic of the signals is < -74dB, on channel 4 the second harmonic is even < -78dB.

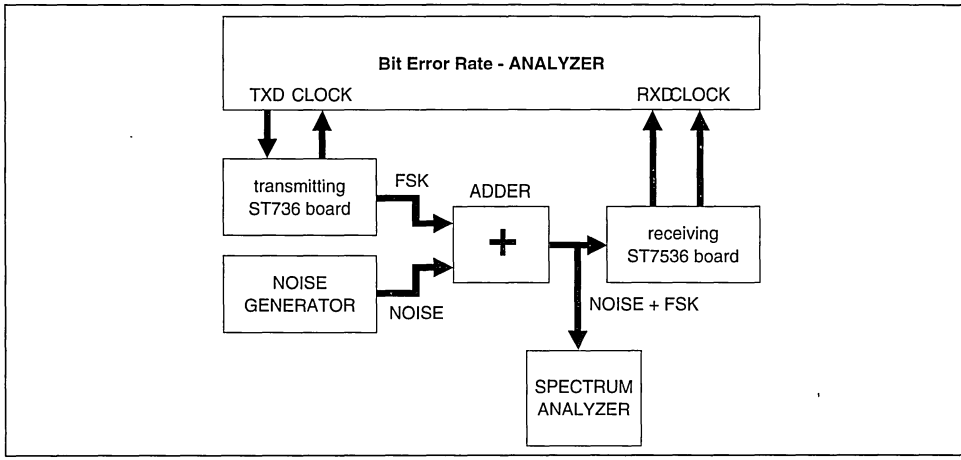
IV.7.3 - Receive sensitivity

The receive sensitivity of the powerline interface is measured with a Bit Error Rate (B.E.R.) test. The Bit Error Rate is the amount of wrong bits in a received bit pattern. For example, if 2 out of 1000 received bits is wrong detected, the B.E.R. is 2/1000 = 2 E-3. If the B.E.R. with an input of 1mV_{RMS} is worse than with an input of 5mV_{RMS}, the receive sensitivity is not 1mV_{RMS} but 5mV_{RMS} (or more).

Test configuration
In this test two ST7536 boards are used. Each board has a ST7536 + powerline interface.

One board is in transmit mode, the other in receive mode. A Bit Error Rate Analyzer is used to generate bit patterns, and to compare these patterns with the receive patterns. Because the ST7536 is a synchronous modem, both the received data (RxD) and transmitted data (TxD) are related to the clock signal generated by the ST7536. Therefore the clock signals of the boards are delivered to the analyzer (see Figure 19).

Figure 19



The output of the transmitting board is a Frequency Shift Keying (FSK) signal. This signal is added with the signal from a noise generator. This to observe the B.E.R. under different Signal/Noise-ratio conditions. In the adder the FSK signal is attenuated to a level of 0.5 - 5mV$_{RMS}$. The output signal is then send to the receiving board.
A spectrum analyzer is used to measure all the signals.

Measurements

Two tests are done on channel 3 (72kHz/1200 baud).

First B.E.R. test is made with a FSK input of 1mV$_{RMS}$ (= -60dBV). With the noise level set at -68....-74dBV. This gives a S/N ratio from 8....14dB.

A second test is done with a FSK input of 5mV$_{RMS}$ (= -46dBV). With the noise level set at -54...-60dBV. These values are set by adjusting the mixer, and measured with the spectrum analyzer.

The spectrum analyzer measurements are made in a spectrum of 1200Hz. This is done because the FSK signal has two main frequencies on 1200 Hz distance from each other. The noise signal is therefore measured in this band. In annexe B example plot are given from all the tests, with a S/N ratio of 10dB.

The B.E.R. is calculated from the number of errors counted by the B.E.R. analyzer.

Example :
For instance the bit rate is 1200 baud. In 10 minutes the analyzer counted 800 errors. The measure time is then 10 x 60 seconds is 600 seconds. Each second 1200 bits are transfered, so in 600 seconds 720000 bits. Then the bit error rate is 800/720000 = 1.1 E-3.

→ B.E.R. = number of errors / (time in seconds x bit rate)

Test results (see ANNEXE A)

The results of the B.E.R. test are almost the same for both 1mV$_{RMS}$ and 5mV$_{RMS}$ (FSK signal level) input. Compared to B.E.R. test results of a stand alone ST7536, the results are even 1dB (S/N ratio) better.
These results demonstrate that the receive sensitivity is at least 1mV$_{RMS}$, and therefore the other channels are tested with an input of 1mV$_{RMS}$.

Channel 1, 2 and 4 are tested with a FSK signal input of 1mV$_{RMS}$. On those channels the results are also compared to B.E.R. test results of a stand alone ST7536. On channel 2 there is no difference between the B.E.R. of a stand alone ST7536 and a ST7536 + powerline interface. On channel 1 and 4 the B.E.R. is 0.5dB better than a stand alone ST7536.

Typical B.E.R. : (input FSK 1mV)

S/N (dB)	Channel 1	Channel 2	Channel 3	Channel 4
8	1.2E-2	1.2E-2	2.0E-2	1.0E-2
10	2.0E-3	2.0E-3	4.5E-3	1.2E-3
12	1.0E-4	1.0E-4	4.5E-4	1.0E-4
14	4.0E-6	4.0E-6	4.5E-5	3.0E-6

IV.7.4 - Conclusions

The B.E.R. tests confirm a receive sensitivity of $1mV_{RMS}$. This is according to the specifications under which the powerline interface has to operate. Moreover, the B.E.R. tests showed that the powerline interface improved the performances of the ST7536 ; the results of a ST7536 in combination with the powerline interface are better than a stand alone ST7536.

Remark :
To test if these results are not only valid for a laboratory set up, both boards have been connected to the 220V powerline network. The distance between the two boards was 30 meter. After a measure period of 15 minutes, not even 1 error was detected !

Test equipment : (see Figure 20)
Shlumberger SI 7703B B.E.R. analyzer
HP3562A Spectrum analyzer
Rohde & Schwarz SUF2 Noise generator
Mixer :

V - HEATING CONTROL APPLICATION

V.1 - Introduction

We will do a heating control system, using the ST7536 and a ST6 micro controller.

We have two boards (see Figure 21) :
- MASTER : control and set temperature in each room
- SLAVE : temperature reading,switch on/off of heater.

Figure 20

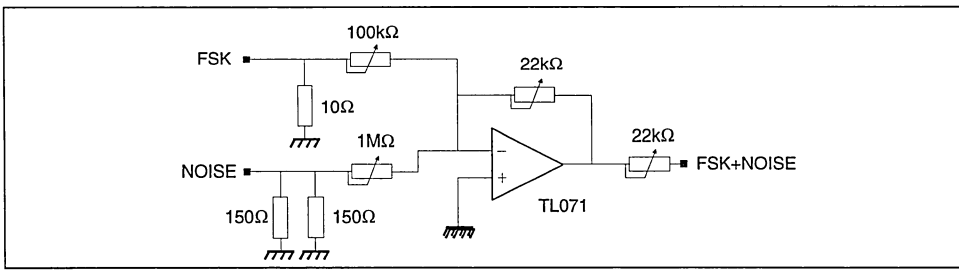
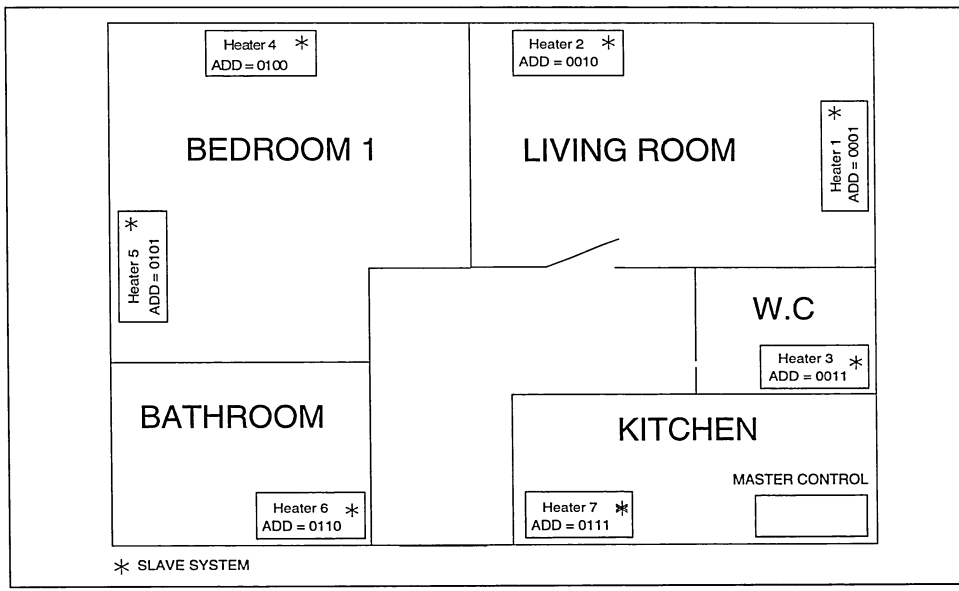


Figure 21

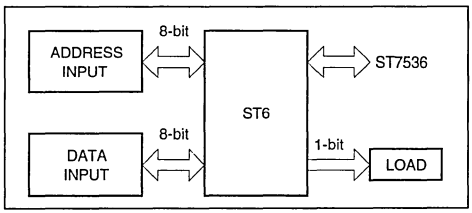


V.2 - Micro-controllers

Two different micro-controllers have been set up, one for the slave systems, and one for the master system. The main differences between the two controllers are the different input/output facilities.

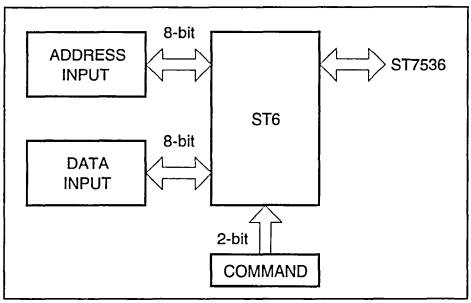
The slave version needs one 8-bit data input to initialize its own address, and one 8-bit input to read data from an external measure system. It should also provide an output that switches a load. This load will be simulated by a LED.

Figure 22 : Slave Micro-controller



The master version will have its own address initialized in the software. Therefore no data input is needed for that. Data input (8-bit) is needed to read the destination (slave) address. To display data, an 8-bit data output has to be provided. Furthermore, it needs a 2-bit command input.

Figure 23 : Master Micro-controller



Both the master and the slave version need also data exchange with the ST7536; the clock, transmit data, receive data, reset and Rx/$\overline{Tx}$ control lines.

V.3 - Hardware

As a micro-controller the ST6 has been chosen. This controller provides 20 data input/output pins, a reset and a non maskable interrupt input. Only a few external components have to be added to this micro-controller for full operation. The used ST6 is a 2K byte program memory EPROM version; the ST62E15. The ST6 has an internal oscillator circuit. One machine cycle takes 13 oscillator pulses. This means that with a clock frequency of 8MHz a machine cycle takes 1.625µs. Most of the instructions (load instructions, bit manipulations) take 4 machine cycles. The maximum bitrate the ST6 has to serve is 1200 baud. One bit has a lenght of 833µs, which is equal to 512 machine cycles. This means that during each bit about 130 instructions can be executed.

The ST6 has an on chip watchdog circuit. There are two different versions of the ST62E15. On one there is a software selectable watchdog, and on the other (the hardware version) this watchdog is allways activated. The version that is used for these micro-controllers is the hardware version.

V.4 - Slave

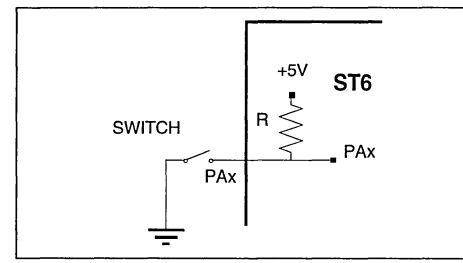
This micro-controller is in fact just an ST6 with a very few external components. A few switches, resistors, capacitors, a crystal and a 74LS04 are connected to have a complete controller. Each of these components is used to set the ST6 in the correct configuration.

Pin configuration slave controller

For each pin a short discription is given, such as the configuration chosen for this micro-controller.

- **pin 27..20 (PA0..PA7) :** Input/output port A.
  Port A of the ST6 is used for reading the (8-bit) home address of the slave system. Switches are used to set each bit. The ST6 provides an internal pull-up resistor which will cause an "1". Closing a switch (to 0V) will cause a "0".

Figure 24

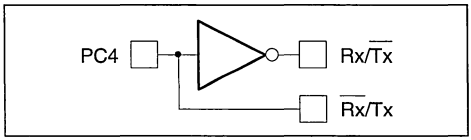


- **pin 19..12 (PB0..PB7) :** Input/output port B.
  Port B of the ST6 is used to read (8-bit) data from an external measure system. This system is simulated by switches. The same as for port A, the ST6 provides an internal pull-up resistor which will cause an "1". Closing a switch (to 0V) will cause a "0".
- **pin 9 (PC4) :** Port C bit4.
  This output is used as the Rx/$\overline{Tx}$ control. Transmit mode of the ST7536 and the powerline interface is selected if this output is "1". Receive mode is

selected with an "0".

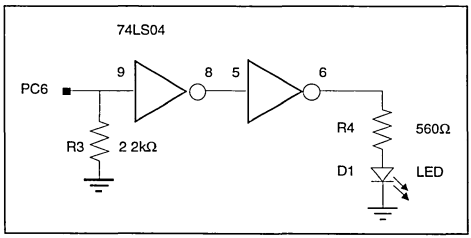
- **pin 8 (PC5) :** Port C bit5.
  This pin is used as the transmit data (TxD) output to the ST7536.

Figure 25



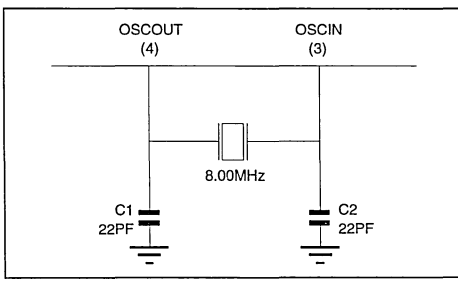
- **pin 6 (PC7) :** Port C bit7.
  This pin is used as the receive data input (RxD) from the ST7536.
- **pin 7 (PC6) :** Port C bit6.
  This is the load switching output. The load is simulated by a LED. Two inverters are used as a buffer between the ST6 and the LED. Because the ST6 outputs are in high impedance during a reset, a pull down resistor (R3/2k2) is used to avoid the load switching on.

Figure 26



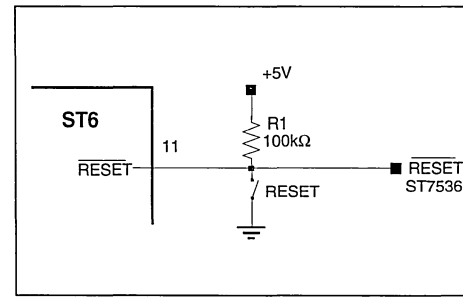
- **pin 4 (OSCOUT) :** Oscillator output.
- **pin 3 (OSCIN) :** Oscillator input.
  Between these pins a 8.00MHz crystal has to be connected. If the internal oscillator of the ST6 runs at 8MHz, one machine cycle is 1.625µs. This speed is needed to be able to serve the 1200 baud bitrate from the ST7536.

Figure 27



- **pin 5 (NMI) :** Non maskable interrupt.
  The NMI is used as input of the (inverted) clock of the ST7536. The NMI is falling edge sensitive. An external pull-up resistor (R2/100k) is added to provide +5V for debugging the controller without the 74LS04 (the inverter).
- **pin 11 (RESET) :** Reset input.
  The reset of the ST6 is active low. To restart the microcontroller at the beginning of its program, this pin should be set to 0V by closing the switch. For normal operation the +5V is provided by a pull-up resistor (R1/100k).

Figure 28



- **pin 2 (TIMER) :** Timer output, not used.
- **pin 10 (TEST) :** Test input.
  The test pin is used to set the ST6 in a special operation mode. For normal operation this pin is set at 0V.
- **pin 1 (V_{DD}) :** Power supply, +5V.
- **pin 28 (V_{SS}) :** Ground, 0V.

V.5 - Master

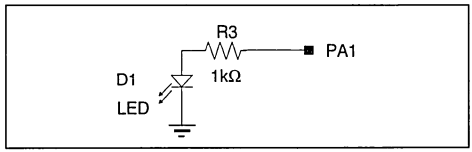
The main difference between the master and the slave version of the micro-controller is the fact that the master needs one extra input/output pin. The slave version has 1 output to control a load, where the master needs 2 inputs to read a command. Therefore one input/output (PC5) has been multiplexed, it serves both the RxD and TxD lines to the ST7536.

Pin configuration master controller

The pin configuration of the master differs from the slave on the next pins:

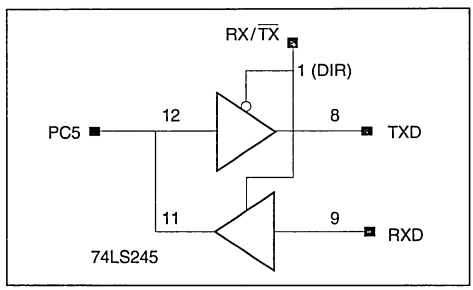
- **pin 27..20 (PA0..PA7) :** Port A.
  The master uses port A to display data. Light Emitting Diodes (LED's) are used to do this. The maximum current that can be taken from each pin is 5mA. Therefore the serial resistor has a value of 1kΩ (current = U/R = 5-0.6/1k = 4.4mA).

Figure 29



- **pin 19..12 (PB0..PB7) :** Port B.
  The hardware configuration of these pins is the same as on the slave, but on the master these pins are used to read a (destination) address.
- **pin 7/6 (PC6/7) :** Port C bit6/bit7.
  On the master these pins are used to read a command (see also the software discription). The hardware configuration is the same as for port B.
- **pin 9 (PC5) :** Port C bit5.
  The slave uses PC7 as received data input (RxD). Because the master already uses this pin for reading a command, PC5 has to be multiplexed. This is done with an 74LS245. It is a (8-bit) bus receiver/transceiver. The Rx/$\overline{Tx}$ line is used to select whether the RxD should be send to PC5, or the data from PC5 to the TxD (that's the opposite direction).

Figure 30



V.6 - Software

The software that has been developed for the micro-controllers has to be regarded as an introduction to more complex communication protocols. Therefore a very simple but effective protocol has been set up. With this protocol it should be possible to evaluate the performances and possible applications of a ST7536 system.

V.7 - Protocol

The protocol has been set up in such a way that all kind of features can be added easily. A simple but powerfull frame format is used. It gives the possibility to use error correction and detection.

Each frame consists of a preamble, a system address, a destination address, a control block and a data block. The preamble and the system address length is 2 bytes, the destination address, the control block and the data block are 3 bytes long.

The preamble is used to train both the transmitting and receiving ST7536. It consists of two 8-bit patterns (10101010). The receiving ST7536 needs it to train its clock recovering. Because the 3 first bits transmitted by an ST7536 are not guaranteed to be correct, the preamble is also used to overcome unreliable data in the beginning of a transmission. This because the preamble doesn't contain data.

The system address is used to be able to have more than one ST7536 system operating on a certain powerline network. For example a remote metering system and a traffic light control system. It is also used to avoid interference with other (no ST7536) systems. The lenght of the address is only 8 bits, and therefore it's send twice, to avoid unwanted activation of a group that has not been called.

The lenght of the preamble and system address together is 4 bytes (32 bits) (see Figure 31)

The preamble and the system address inside the frame (see Figure 32).

The received destination address, control block and data block should be very reliable, and therefore an error correction is done. To be able to do this all these data is send 3 times. The destination address has a lenght of 1 byte (8 bits), which is send 3 times: in block 1, block 2, and block 3. This is the same for the control byte and the data byte. As an example the destination address inside the frame (see Figure 33)

So all the blocks (block 1/2/3) contain the same byte. The error correction uses them to extract the correct byte out of the 3 that have been received. The destination address is used to select 1 user (slave) in a system group. All the slaves in a system have their own 'home' address. To activate a slave, it has to recognize the received destination address inside a frame as its own 'home' address.

In this simple protocol there is only communication between a master and the slaves. Therefore the destination address is transmitted by each slave is the master address. In the frame which transmitted by the master, the destination address is the home address of the slave that is called.

Figure 31

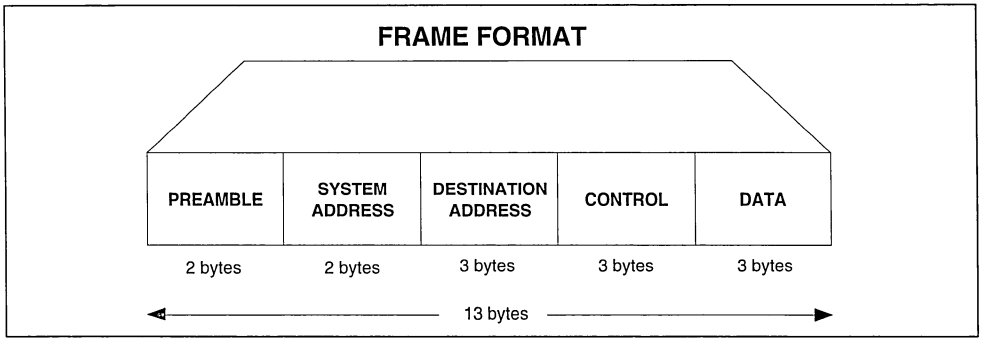


Figure 32

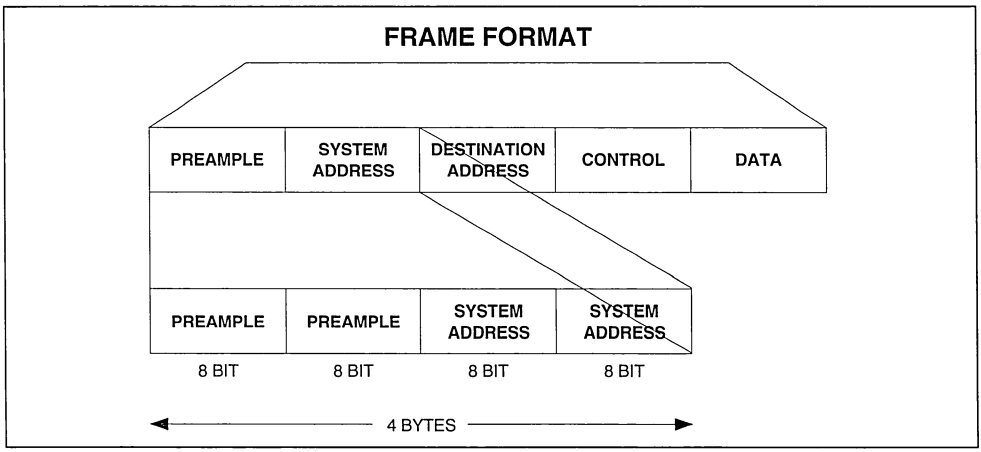
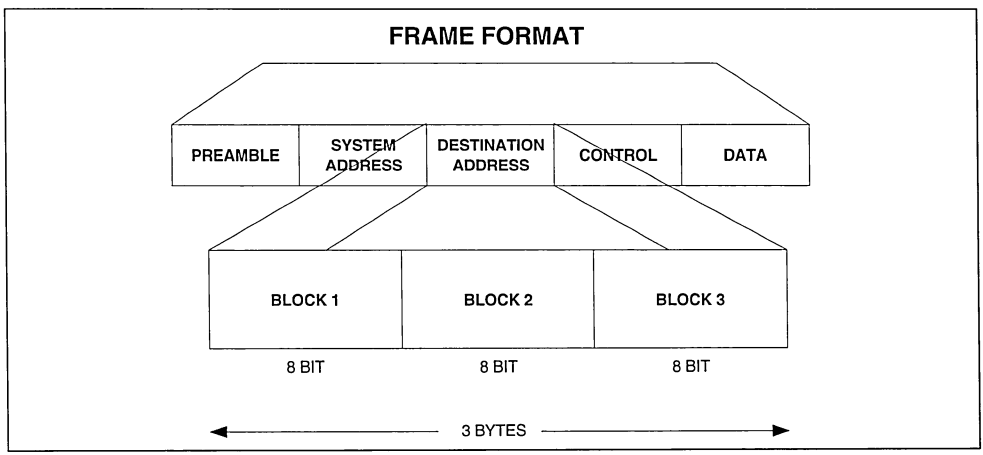


Figure 33



The control byte can be used for all kind of information about the frame. In this protocol the control block is only used to say if the frame is a command or a response. This is done with bit 7. If this bit is set it means that the data byte contains a command (from the master to the slave), and the data byte will contain the command. If this bit is reset it means that the frame is a response (from the slave to the master), and the data byte will contain the requested data.

Control Byte	Status	Data Byte
10000000	command	command
00000000	response	requested data

In the control byte only bit 7 is used. Bit 0...6 are reset. They can be used to add severall features to the protocol.

Error detection and correction

A possible feature that can be added is error detection. In the protocol this feature is not available. This because, to be really usefull, error detection would require the possibility to send a message from the receiver to the transmitter, indicating that an error has been detected. It will need a more detailed protocol, which uses the free bits in the control byte. The intention of this protocol was to be very simple and clear. Therefore the error detection is not provided.
Although there is no error detection, the protocol provides an error correction. It would be very unrealistic to assume that all the bits in a received frame are correct. Therefore the most important parts of the frame (destination address, control byte and data byte) are protected with an error correction.

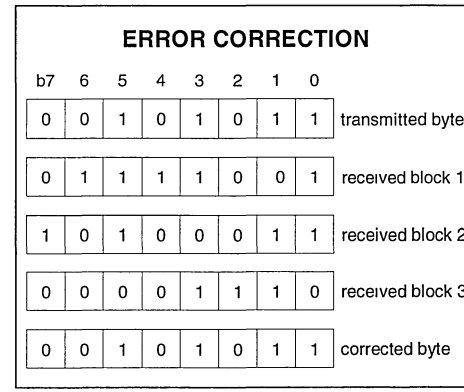
The error correction is done with bit-overlay. This is a very powerfull method to correct bytes that are transmitted over very noise lines. Each byte is transmitted (and received) 3 times. The software uses the 3 received bytes to extract the (probably) correct byte. This is done by performing a bitwise majority decision on all the received blocks.

Even if all the 3 received blocks contain errors, it's still possible to extract the correct byte out of these blocks.
example :
The first received block contains 3 errors (b6/b4 and b1), the second block contains 2 errors (b7 and b3) and the third block contains 3 errors (b5/b2 and b0) (see Figure 34).

The error corrector will take bitwise a decision what is probably the correct bit. If two out of three bits are "1", the resulting bit will be "1". If two out of three bits are "0", the resulting bit will be "0".

This system can correct 1 error out of 3 bits. If more blocks are send, let's say 9, it would be possible to correct 4 out of 9 bits. This is a very interesting method to overcome problems on very noisy powerlines.

Figure 34



V.8 - Application software

The protocol has been designed to demonstrate typical applications of the ST7536.

All the slaves have been programmed with one program. With this program it is possible to set a load (simulated by a LED) on or off. This load can be for example (depending on the application) a traffic light. With this program it's also possible to read data (simulated by 8 switches) from an external measure system, and send this data to the master if requested. The measure system, for example, can be reading an electricity meter. Remote reading these meters, can save the costs for manual reading (such a system is allready operational in Italy). So there has been written 1 program for the slaves, that can simulate different applications.

Each typical application should be programmed in the master. It gives the possibilty to demonstrate different applications without reprogramming all the slaves.

One application program has been developed for the master.It demonstrates the good functioning of the system: a remote heater control. With this application it's possible to control in a building in each room the heater (which is equipped with an ST7536). The LED on the slave simulates in this case the heater. With the master each heater can be set manual on or off, and even more, the master can regulate automatically the heater, by reading out the room temperature. This temperature is simulated with the 8 switches on the slave. The

master has 4 different commands:

1:(00)	manual off	00000000	heater on
2:(01)	manual on Temperature :	00001111	
3:(10)	not used	00010000	
4:(11)	automatic control →	11111111	heater off

V.8.1 - ST6 programs

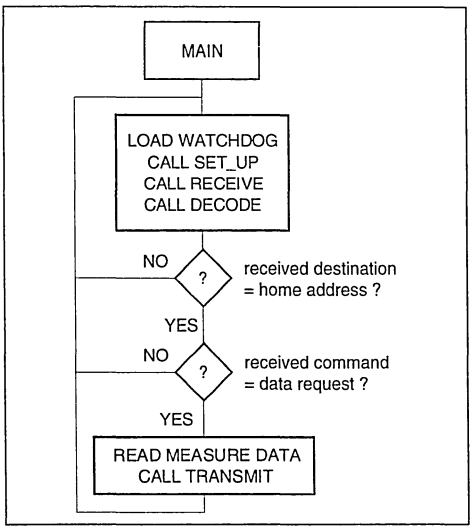
The programs for both the master and the slave have been written in assembly language. An assembler is used to create the executable code. A special ST6 kit is used to debug the programs. The EPROMs are also programmed with this kit. The program memory size of the ST62E15 is 2K byte. The slave program is 1.6K byte, the application program for the master 1.8K byte long.

Some subroutines are used in both the master and the slave program, like the transmit/receive subroutines and the error decoding.

From both programs the most important subroutines are described on the next pages. The flow charts that are used do not give a detailed representation of the subroutines, but are used to explain the structure of the subroutine.

V.8.1.1 - Slave program

Figure 35



In the main program first of all the watchdog is (re)loaded. The watchdog is a down-counter that generates a reset when it's not in time reloaded. It provides a recovery from a software upset.

Then the home address is read from the switches in the set-up routine. The slave will go in receive mode and be maintened until a complete frame is received.

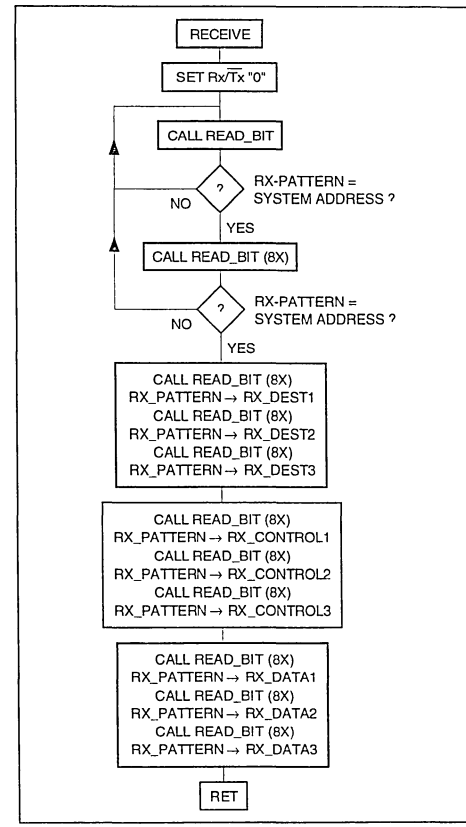
After that the contents of this frame is decoded. In the decode subroutine the bytes are corrected and depending on the received command the led is set on or off.

If the received destination address was the slaves home address and the received command was a data request the (simulated) measure data is read and then transmitted to the master.

Receive subroutine

The receive subroutine is used to read a frame. It ignores all the RxD until the system address is received. When it is received for the second time, the next bytes of the frame are read and stored. To read the RxD this subroutine uses the read_bit subroutine which is discribed on the next page.

Figure 36



First of all the Rx/$\overline{Tx}$ line is reset. The ST7536 and the powerline interface will then be in receive mode. Then the read_bit subroutine is called, whlch will add the next received bit to the Rx_pattern. As long as the system address is not received, the programs continue read the RxD.

When the system address is received, the next 8 bits will be loaded using the read_bit subroutine, and after that the Rx_pattern should contain again the system address. If this is not the case this procedure starts again. Else the next bytes will be read and stored.

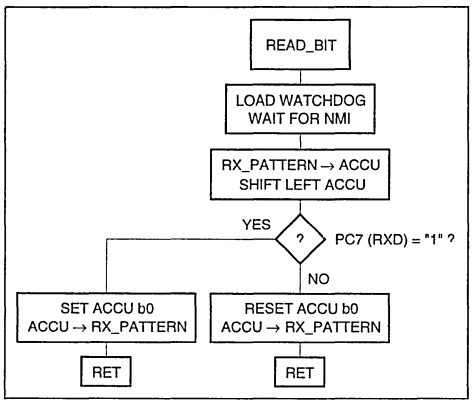
Flrst the 3 destlnatlon addresses. The read_bit subroutine is called 8 times and the Rx_pattern will then contain the next byte (Rx_dest1) which is stored. The next 2 bytes (Rx_dest2, Rx_dest3) are read in the same way.

When the destination addresses are received the control bytes and the data bytes are received and stored in the same way.

Read-bit routine

This routine is used to read the RxD is presented on PC7 (for the master on PC5). The ST7536 delivers valid data on the positive edge of its clock. The inverted clock is used as the NMI input of the ST6. This NMI is falling edge sensitive - > an NMI will be generated on the positive edge of the ST7536 clock. This means that the RxD should be read immediately after a NMI interrupt. The received bit is then added to the (Rx_)pattern.

Figure 37



First of all the watchdog is reloaded.

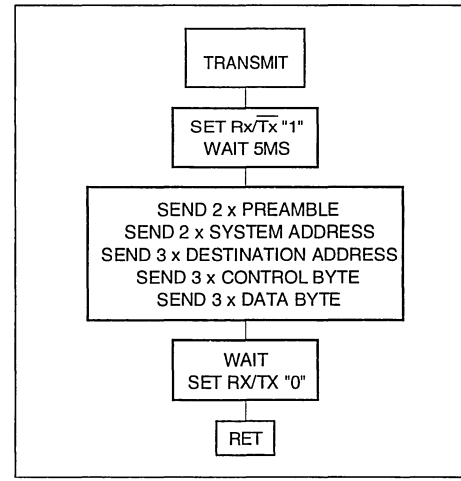
Then the ST6 will wait for the NMI (interrupt). The Rx_pattern is loaded into the accumulator and then shifted left. If the received data bit is a "1" the next bit (b0 in the accumulator) is set to "1". If the received bit is a "0", this bit will be set to "0".

At the end the new pattern is stored.

Transmit subroutine

This subroutine uses the send 8-bit subroutine to send a 8-bit pattern. This subroutine is discribed on the next page.

Figure 38



In the transmit subroutine first off all the Rx/$\overline{Tx}$ line is set "1". The ST7536 and the powerline interface are then in transmit mode. Typical carrier stabilisation time of the ST7536 is 5ms. Therefore the program waits this time before sending all the bytes.

First the preamble (10101010) is send 2 times and then the system address. The destination address, the control byte and the data byte are send 3 time. This is done with the send 8-bit subroutine.

Send 8bit pattern subroutine

The ST7536 samples the TxD on the positive edge of the clock. The inverted clock is used as the NMI input of the ST6. On the positive edge of the clock (CLR/T) an NMI interrupt occurs. The software waits then 304 machine cycles before changing the TxD. When the TxD is changed it waits for the next NMI and again 304 cycles before storing the next TxD on PC5. Using these delays it is possible to present the ST7536 valid TxD on the positive edge of its clock. Both 600 (channel 1/2) and 1200 (channel 3/4) baud bitrates can be handled this way.

Figure 39

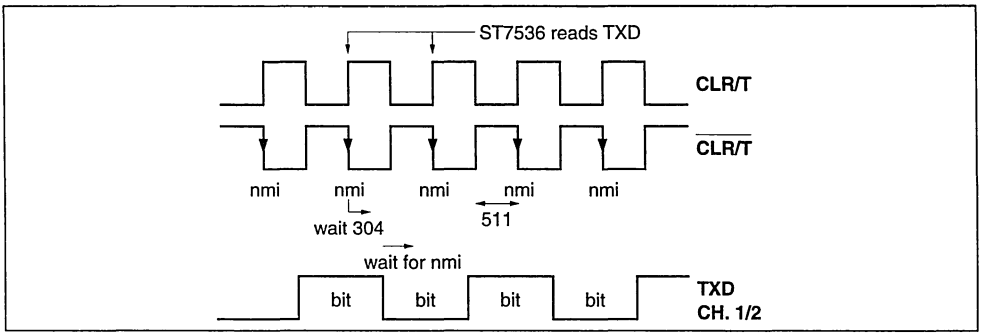


Figure 40

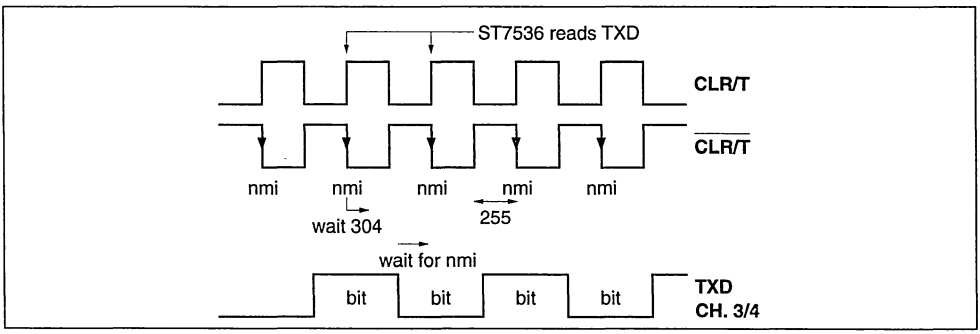
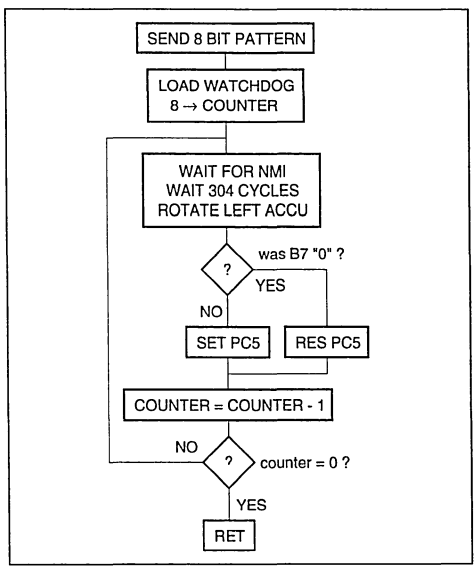


Figure 41



In the subroutine the watchdog is (re)loaded. Then the counter is set at 8. The ST6 waits for the NMI and then 304 cycles. The accumulator contains the pattern that has to be transmitted. This pattern is shift left; the carry bit will contain b7, b7 will contain b6 etc. If b7 was a "0" PC5 (the TxD output of the ST6) is reset, if it was a ' 1 ' PC5 is set. Bit7 is then transmitted.

The counter is then decreased by 1, the software waits the same time, and the accumulator is shift left again. The carry bit will then contain b6 of the pattern that should be transmitted. The same as before, this bit is transferred to the TxD output.

This is also done with b5..b0. If b0 is transferred(transmitted) the counter will be 0. And then the ST6 will jump out of the subroutine.

Decode subroutine

When a frame is received the main program jumps to this subroutine. In this subroutine first of all the error correction is called. After the correction, described below, the subroutine checks if the destination address of the frame was the home address of the slave. In this case, and then the control byte

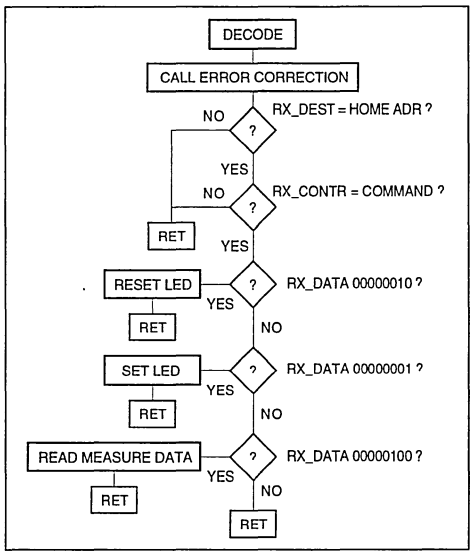
indicates a command in the data byte, the subroutine decodes the data byte. Then there is a jump out of the subroutine (see Figure 42)

Three commands are used in this program :

1: data = 0000 0001 → LED off.
2: data = 0000 0010 → LED on.
3: data = 0000 0100 → data request.

Depending on the received data byte the led will be set on or off, or in case of a data request, the ST6 reads the data on the system.

Figure 42



Error correction subroutine

In this subroutine the bits of the 3 received bytes are compared. The resulting should be set ("1") if at least 2 out of 3 received bit are set. If 2 or more received bits are reset, the resulting bit should be reset ("0"). All the bits of the bytes are tested this way. This is done bit by bit (bit x), using the same procedure (see Figure 43).

V.8.1.2 - Master program

For the master one application program is set up. It presents the ST7536 in a central heating control. The receive, transmit and error correction subroutines are almost the same as described for the slave program. The master has a 2 bit command input (PC6/PC7).

After reading the command it is checked if it's a new command or an old command. The program continues if a new command is read (from the switches). Then this command is decoded :

PC6/7: 00 → heater off
PC6/7: 01 → heater on
PC6/7: 10 → not used
PC6/7: 11 → automatic control

The program will jump to the subroutine corresponding to the command that is decoded; the automatic, manual on or manual off subroutine (see Figure 44).

Figure 43

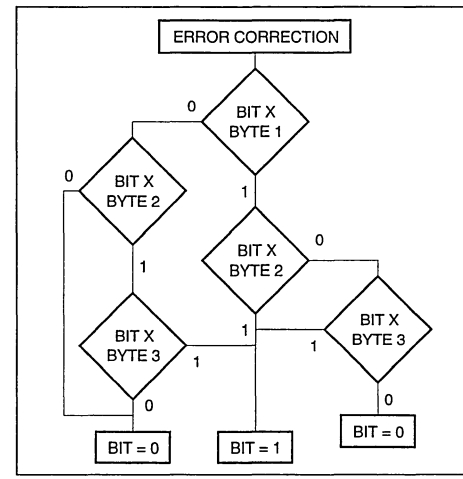
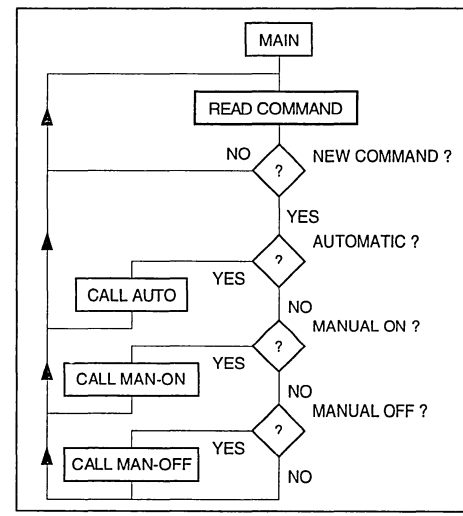


Figure 44



Automatic control subroutine

In this subroutine the master compares the receive data (temperature) from the slave to the reference value (00001 1 1 1). If the data < reference the heater is set on, else the heater is set off.

First the master sends a datarequest command to the slave. Then it goes in receive mode, to wait for the response of the slave. The received frame is then corrected, and the received destination address and control byte are checked. If the control byte indicates a response the received data is compared to the reference value (00001111). If the received data < the reference, a heater on command will be transmitted, else a heater off command. After that the command input is checked to be still an automatic control command. In this case, the master will continue with controlling the heater (see Figure 45).

Manual on/off subroutines

Although these routines are very simple, their functions are given in the flow charts below, to have a complete overview of the application program. The manual on subroutine sends a frame containing a heater on command, the manual off routine a frame containing a heater off command (see Figure 46).

V.8.1.3 - Evaluation of the software

The used protocol seems to be rather effective and functional. The system has been tested on very noise powerline networks, and no (software) problems occured. The ST6 programs have been written and tested step by step. When the programs were operating according to the protocol they have not been 're-written'. Therefore the programs might not be as well structured as possible. For final application software, it might be usefull to evaluate the programs, and then rewrite some subroutines. The program size may be decrease, and a 'clean up' will make the programs easier to understand.

Figure 45

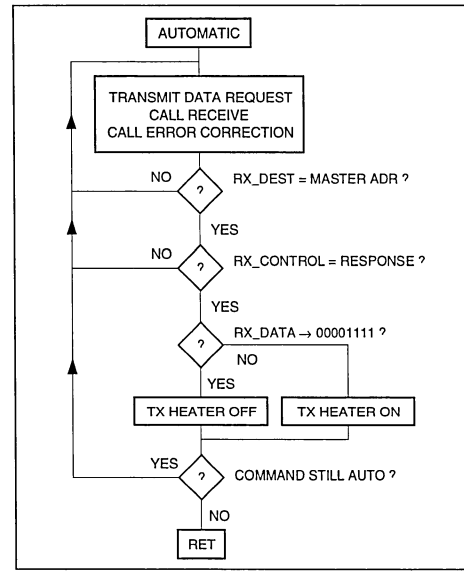
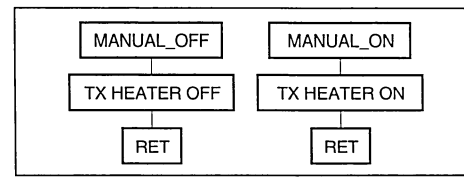


Figure 46



ANNEXE A

Figure 47 : B.E.R. ST7536 Application Board Comparison of channel 1/2/3/4 T = 25°C, Line Input = 1mV

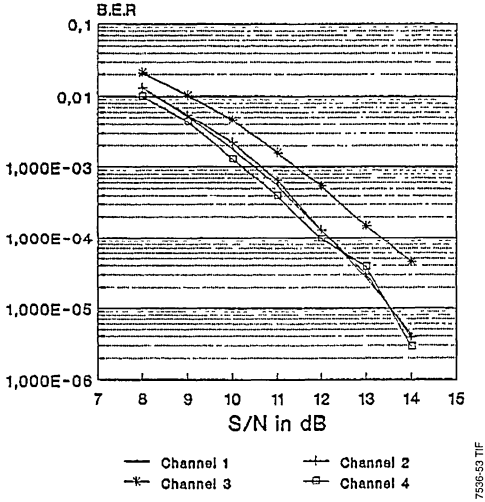


Figure 48 : B.E.R. Channel 3 (72kHz.) ST7536 board input 1mV & 5mV versus stand alone ST7536 RAI input 3mV

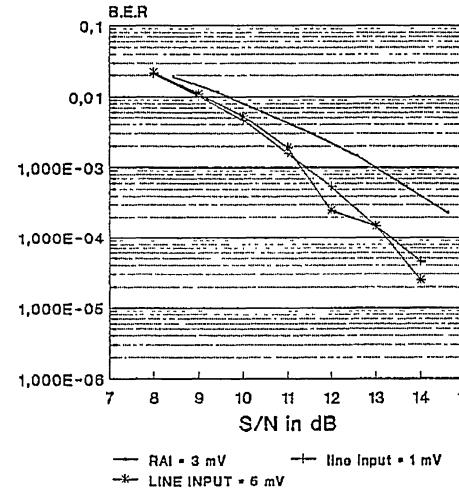


Figure 49 : B.E.R. comparison - ST7536 board versus stand alone ST7536 T = 25°C, Channel 1 (82kHz)

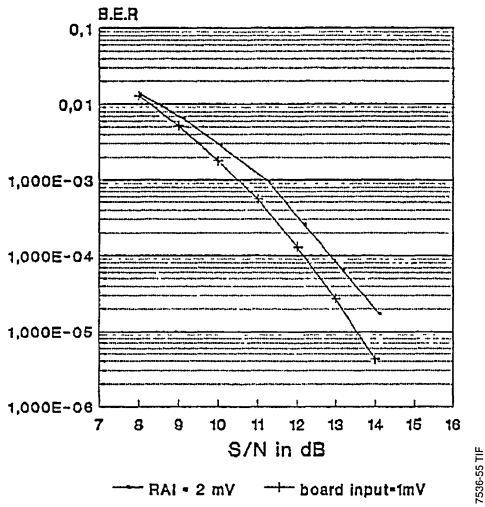


Figure 50 : B.E.R. comparison - ST7536 board versus stand alone ST7536 T = 25°C, Channel 2 (67kHz)

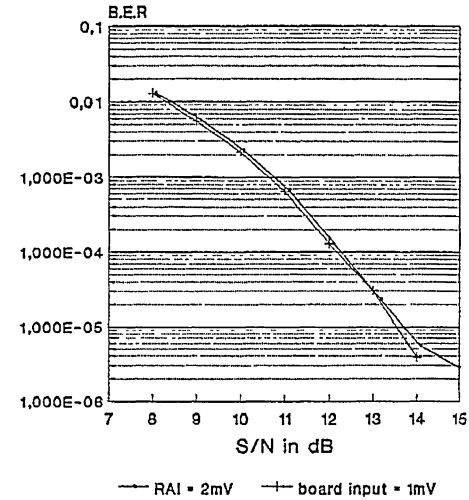


Figure 51 : B.E.R. comparison - ST7536 board versus stand alone ST7536
T = 25°C, Channel 3 (72kHz)

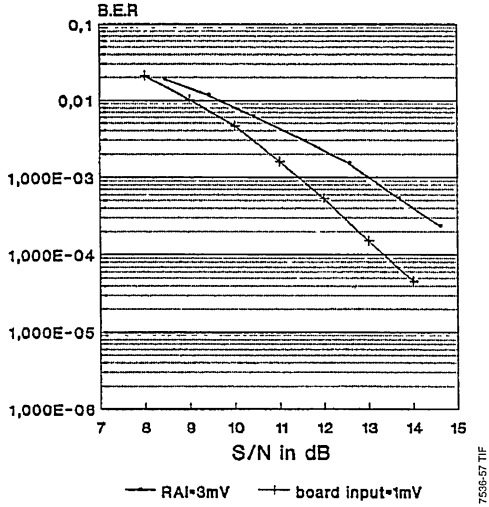
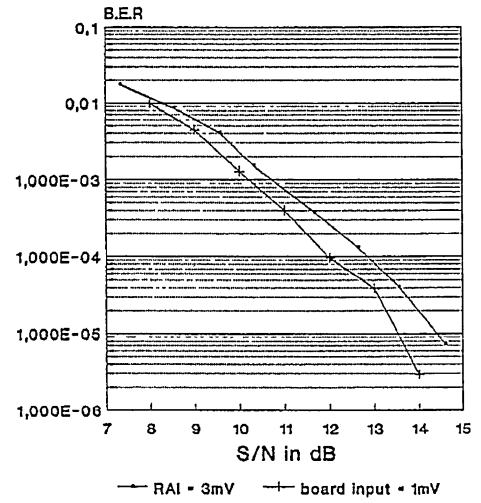
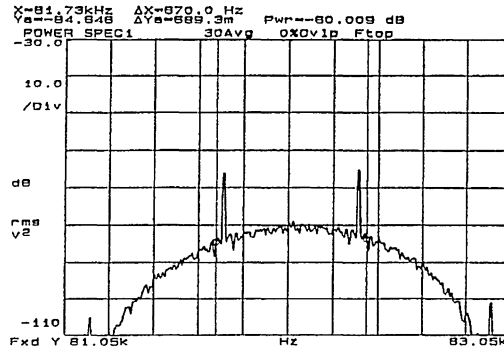


Figure 52 : B.E.R. comparison - ST7536 board versus stand alone ST7536
T = 25°C, Channel 4 (86kHz)



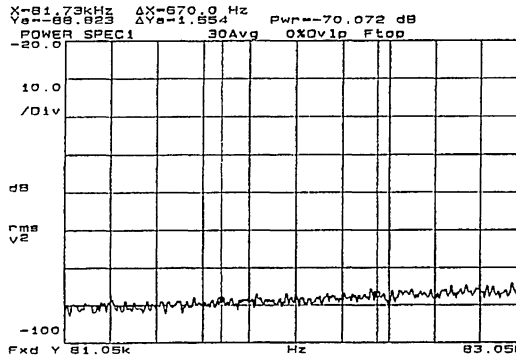
ANNEXE B : B.E.R. ST7536 APPLICATION BOARD (Signal/Noise frequency spectra)

Figure 53 : Channel 1 (82kHz) - S/N = -10dB, Input 1mV = -60dB
FSK (-60dB) - 1mV



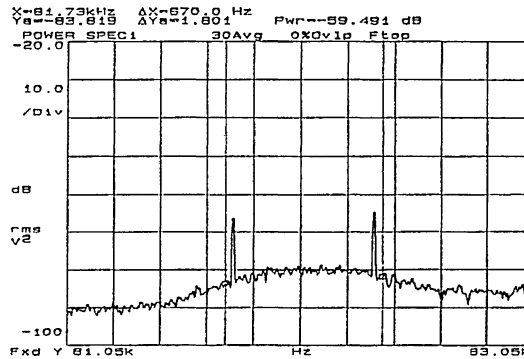
7536-59 TIF

Figure 54 : Channel 1 (82kHz) - S/N = -10dB, Input 1mV = -60dB
Noise (-70dB)



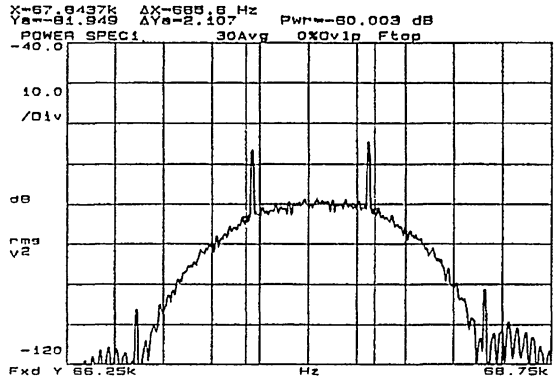
7536-60 TIF

Figure 55 : Channel 1 (82kHz) - S/N = -10dB, Input 1mV = -60dB
FSK + Noise



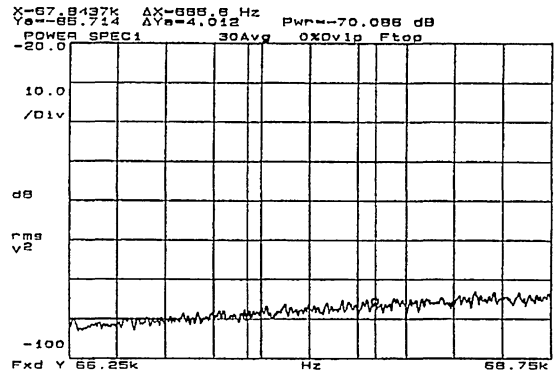
7536-61 TIF

Figure 56 : Channel 2 (67kHz) - S/N = -10dB, Input 1mV = -60dB FSK (-60dB) - 1mV



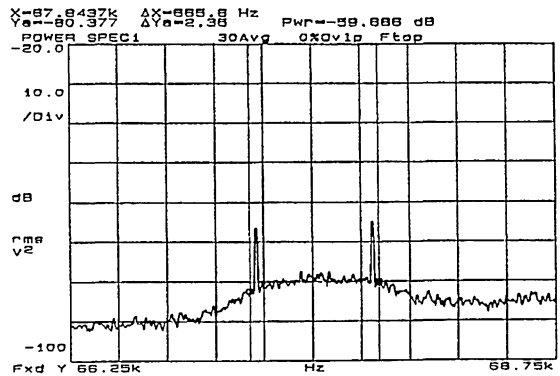
7536-62.TIF

Figure 57 : Channel 2 (67kHz) - S/N = -10dB, Input 1mV = -60dB Noise (-70dB)



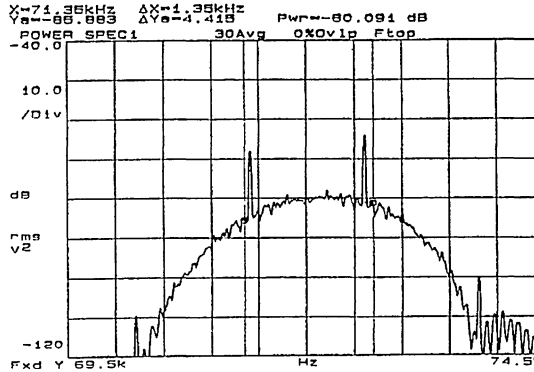
7536-63.TIF

Figure 58 : Channel 2 (67kHz) - S/N = -10dB, Input 1mV = -60dB FSK + Noise



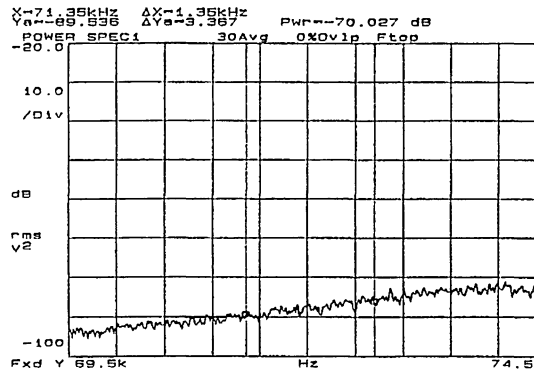
7536-64.TIF

Figure 59 : Channel 3 (72kHz) - S/N = -10dB, Input 1mV = -60dB
FSK (-60dB) - 1mV



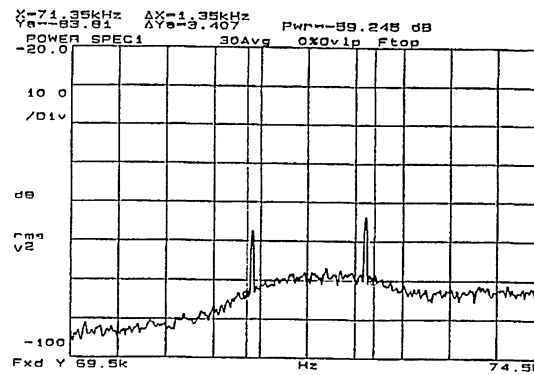
7536-65 TIF

Figure 60 : Channel 3 (72kHz) - S/N = -10dB, Input 1mV = -60dB
Noise (-70dB)



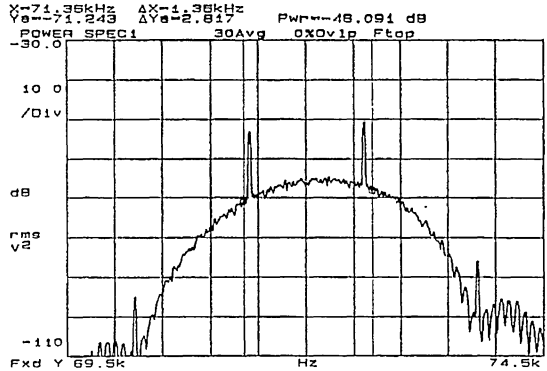
7536-66 TIF

Figure 61 : Channel 3 (72kHz) - S/N = -10dB, Input 1mV = -60dB
FSK + Noise



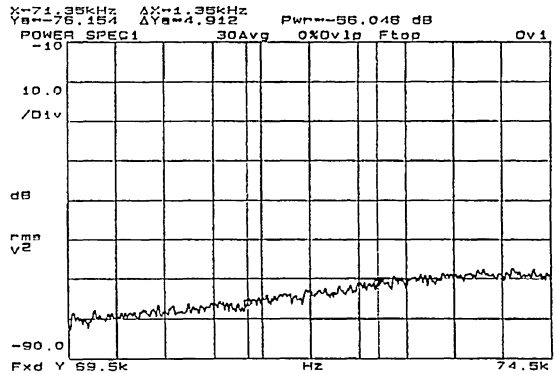
7536-67 TIF

Figure 62 : Channel 3 (72kHz) - S/N = -10dB, Input 5mV = -46dB FSK (-46dB) - 5mV



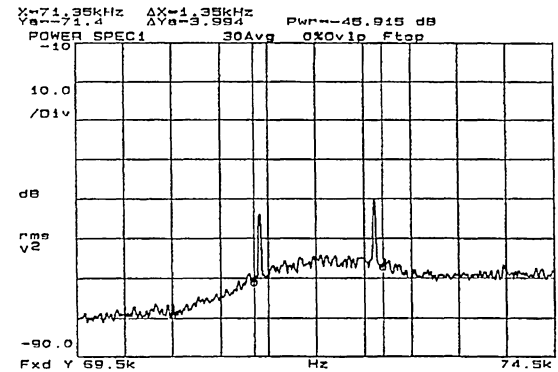
7536-68.TIF

Figure 63 : Channel 3 (72kHz) - S/N = -10dB, Input 5mV = -46dB Noise (-56dB)



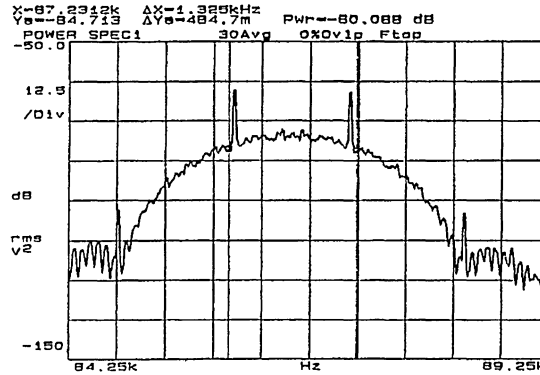
7536-69.TIF

Figure 64 : Channel 3 (72kHz) - S/N = -10dB, Input 5mV = -46dB FSK + Noise



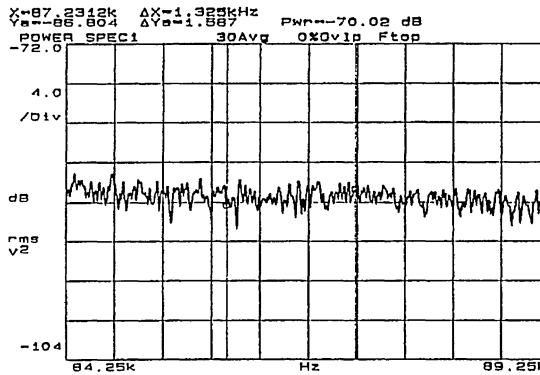
7536-70.TIF

Figure 65 : Channel 4 (86kHz) - S/N = -10dB, Input 1mV = -60dB
FSK (-60dB) - 1mV



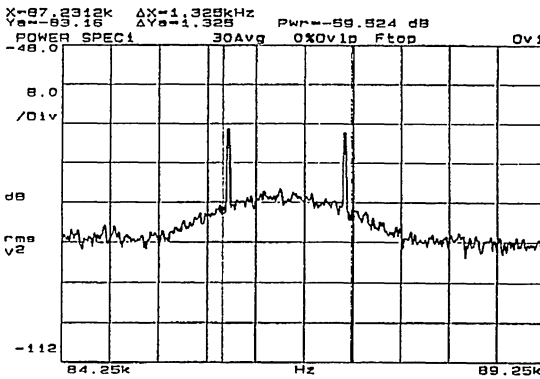
7536-71.TIF

Figure 66 : Channel 4 (86kHz) - S/N = -10dB, Input 1mV = -60dB
Noise (-70dB)



7536-72.TIF

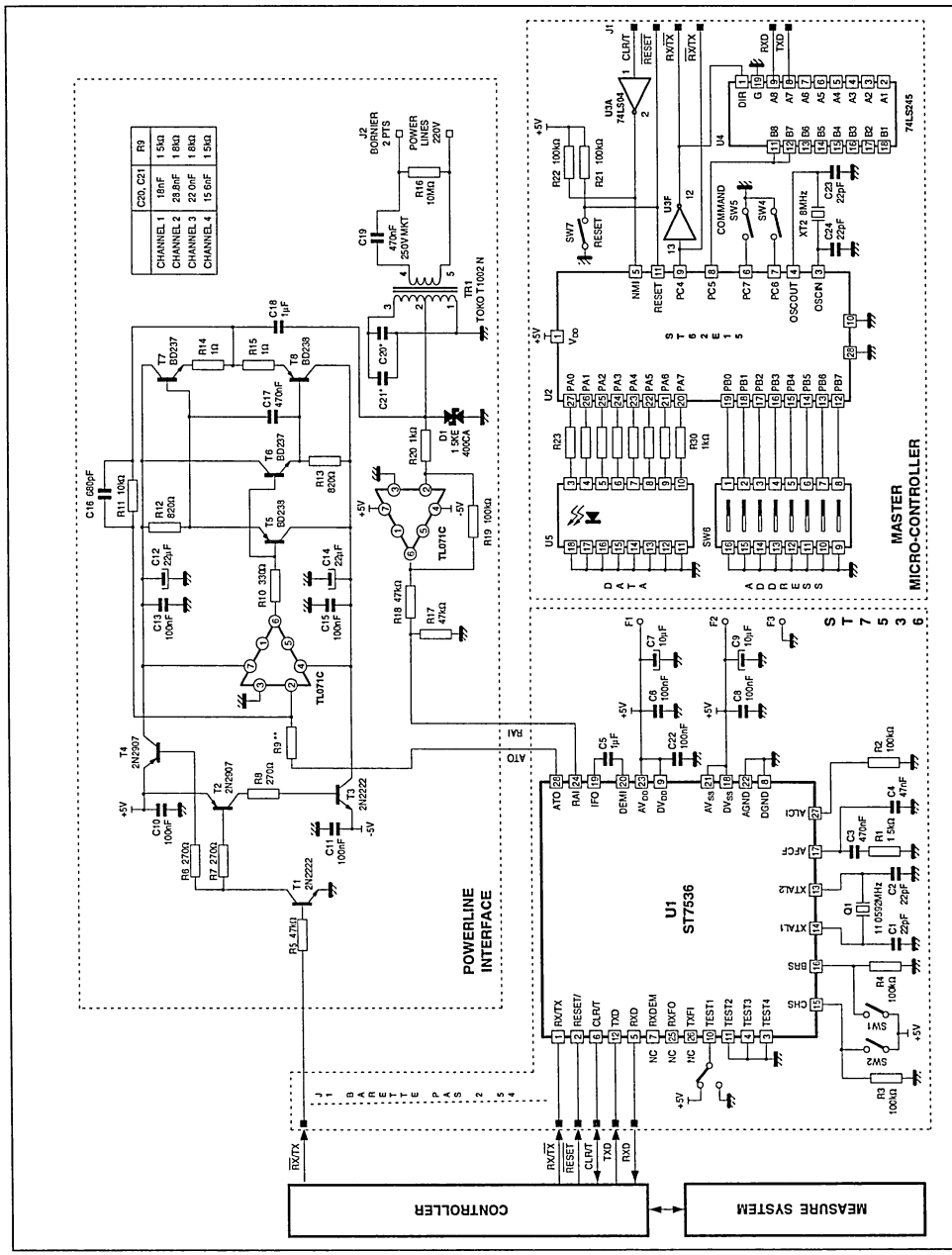
Figure 67 : Channel 4 (86kHz) - S/N = -10dB, Input 1mV = -60dB
FSK + Noise



7536-73.TIF

ANNEXE C : BOARD SCHEMATICS

Figure 68 : ST7536 Master



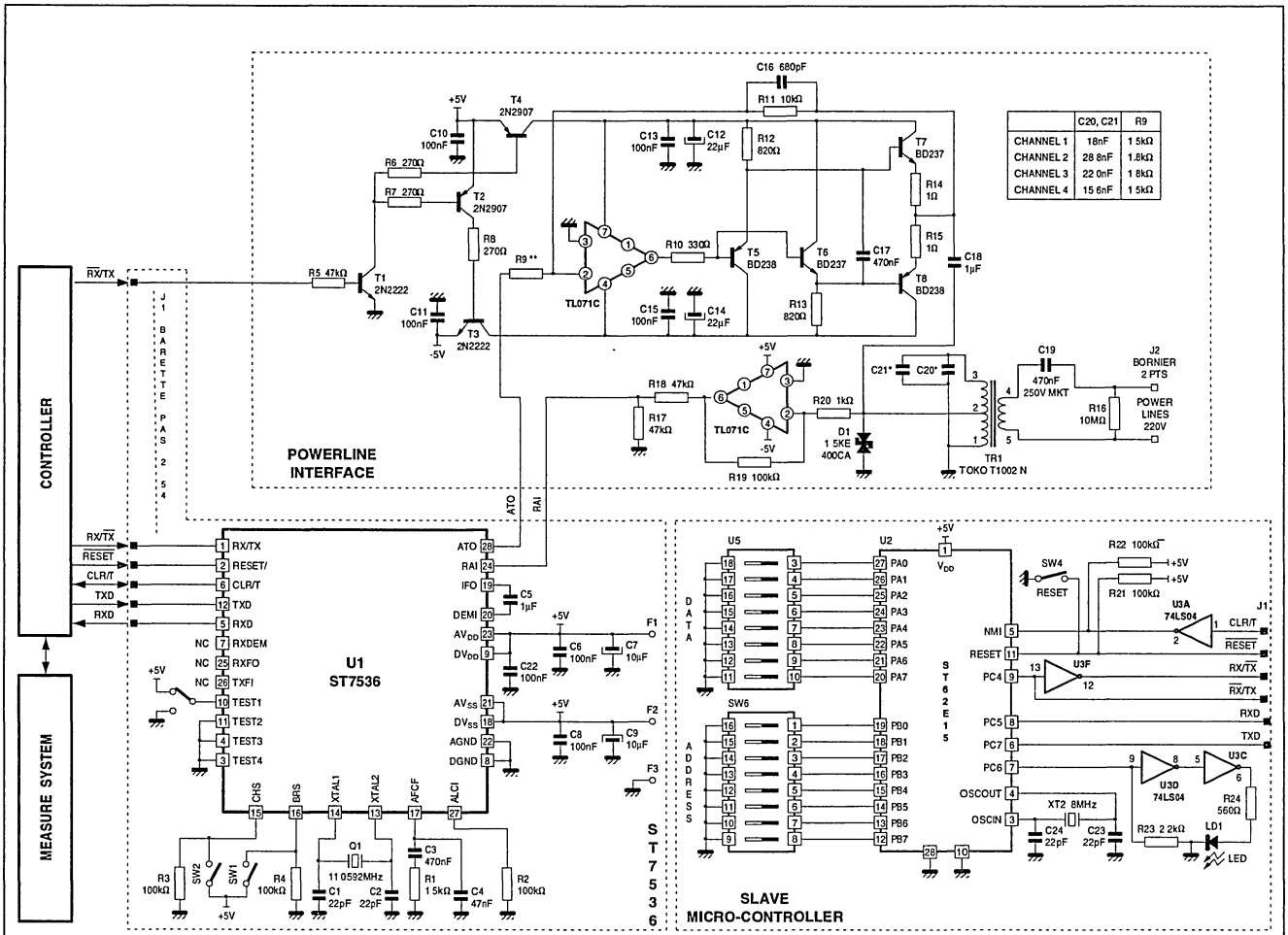


Figure 69 : ST7536 Slave

SGS-THOMSON MICROELECTRONICS

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

ST7537 POWER LINE MODEM APPLICATION

By Joël HULOUX and Laurent HANUS

SUMMARY

I - FOREWORD :

HOME AUTOMATION CONCEPT

Kenneth P. Wacks, consultant to the home automation industry, has written an article clearly defining the concept of home automation. An extract is given below :

"... Over the past six years a new industry called "home automation" has been developing. This industry will create the next generation of consumer appliances. The primary value added by home automation is the integration of products and services for household use. A few small companies are marketing home automation systems. Large companies and institutions are exploring this emerging industry to determine the market potential.

A communication network in the house will provide the infra-structure for linking appliances, sensors, controllers, and control panels inside the house. This has become feasible by tailoring the communications technologies developed for office automation to the home environment.

I.1 - Home Automation Appliances

In home automation, the term "appliances" refers not only to the familiar kitchen, audio/video, and portable appliances, but also to the components of a heating and cooling system, a security system, and lighting features. Home automation covers a broad range of products and services intended for consumer use. These items are expected to share some common attributes, among which are :

- Emphasis on Subsystems :
  Most appliances in houses today are self-contained in metal or plastic cabinets. Each appliance operates independently to the others. Each appliance has a different set of user control.
  Appliances in a home automation environment are able to exchange data. This allows appliances to be grouped into subsystems. Examples range from familiar subsystems, such as security and audio/video systems, to sophisticated lighting controls with preset dimming levels for banks of lights. A future subsystem might permit a washing machine or a dish-washer to request that a water heater preheat water when needed or when the energy cost is lowest.
- Incorporation of Communications Standard :
  Some of the subsystems mentioned already exist. However, the components of each are interconnected using custom-designed technologies and custom wiring. Home automation standards will relieve the manufacturer of the need to invent an ad hoc communications protocol and to provide wiring for data signals.
- Diverse Locations :
  Once communications standards are developed, manufacturers will be able to locate components of appliances outside the cabinet. Control panels could be placed where convenient for the user, not necessarely mounted on the cabinet. Related appliances, such as clothes washer and a clothes dryer, could share a control panel so the knobs and dials are consistent and easier to operate.

I.2 - The Growth of the Industry

Communications technology and standards play important roles in forecasting the home automation industry. However, the development of applications to use these technologies will set the growth rate that simplify routine activities, spark a desire consumers, or save money.

Thus, the growth rate of the home automation industry is ultimately determinated by the actions of appliance manufacturers. Key among these decisions are :

- Adoption of an Emerging Communications Standard :
  The appliance manufacturers will greatly influence the establishment of a particular communications standard. They may even force an amalgamation of standards from among the current contenders.

- Create New Appliances or Appliances Features : The development of standard communications methods can benefit manufacturers and consumers. The design staff would more likely be encouraged and financed to invent appliances that depend on the exchange of data if a communications infra-structure were already in the house..."

II - INTRODUCTION

In the latest generation of home automation systems, appliances can exchange information by transmitting data over the domestic mains wiring. As a result there is no need to install extra control cables and appliances can be connected to the "network" simply by plugging them into the nearest wall socket. Apart from the obvious saving in installation cost, this virtual network also makes modification and enhancement very simple since new devices just have a wall socket to be instantly connected to the network.

What makes these systems feasible is a new dedicated modem integrated circuit, the SGS-THOMSON ST7537 Home Automation Modem IC, developed specifically for this new high volume consumer market as part of a European Community "ESPRIT" project on domestic automation.

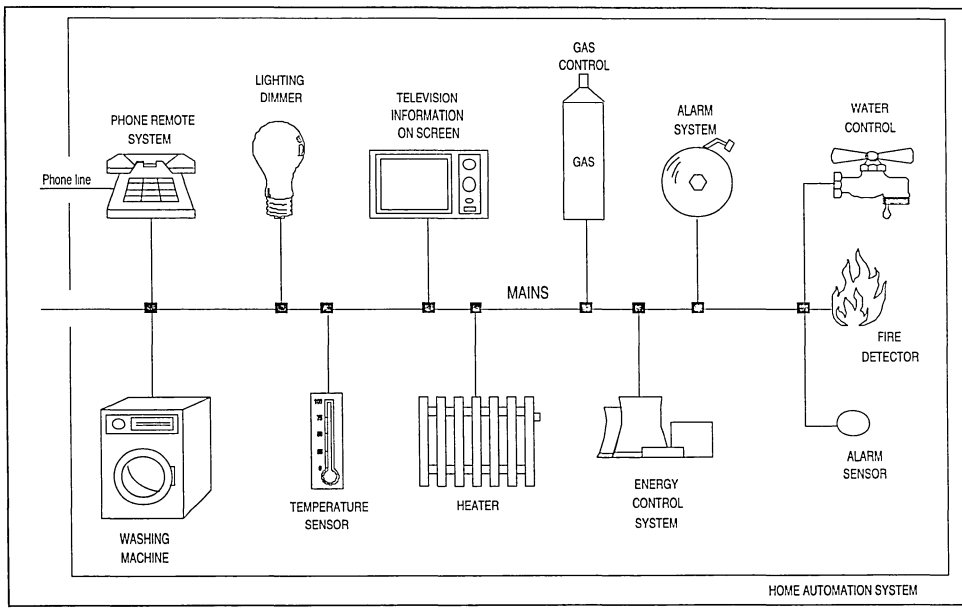
A typical household scenario is shown in Figure 1, where various appliances, sensors, utility controls, a telephone interface and a TV screen display are all connected to the power line using power line modem.

If this automated house catches fire the detector will send a warning message over the line. This will be picked up by the gas control which can cut off the gas supply, by an alarm system that can alert anyone in the house, and even by the telephone interface that can call the emergency services.

The telephone interface also allows the householder to give instructions to appliances from outside. You might, for example, phone home and tell the air conditioner to precool certain rooms at a specified time.

Where there is a limit on energy consumption, or where demand energy pricing is used (now that the technology is available this is likely to be applied extensively in future) various appliances can negociate power requirements through an energy control system. For example, a washing machine can agree with the heating system when it can start a cycle to avoid sudden and unnecessary peaks of demand.

Figure 1 : Typical Household Scenario



III - THE ELECTRICAL NETWORK

Research has been done on the communication properties of the residential power circuit by J.B O'Neal Jr. An extract of his written work is presented below :
"... The primary objective in most residential power line carrier systems is to communicate information from one power outlet in a residence to another. The communication medium, therefore, consists of everything connected on power outlets. This includes house wiring in the walls of the building, appliance wiring, the appliances themselves, the service panel, the triplex wire connecting the service panel to the distribution transformer and the distribution transformer itself. Since distribution transformers usually serve more than one residence, the loads and wiring of all residences connected to the same transformer must be included.

III.1 - Impedance of Power Lines

The most extensive data on this subject has been published by Malack and Engstrom of IBM (Electromagnetic Compatibility Laboratory), who measured the RF impedance of 86 commercial AC power distribution systems in six European countries (see Figure 2).
These measurements show that the impedance of the residential power circuits increases with frequency and is in the range from about 1.5 to 80Ω at 100kHz. It appears that this impedance is determined by two parameters - the loads connected to the network and the impedance of the distribution transformer. The loads at a neighbor's residence can effect this impedance. Wiring seems to have a relatively small effect. The impedance is usually inductive.
For typical resistive loads, signal attenuation is expected to be from 2 to 40dB at 150kHz depending on the distribution transformer used and the size of the loads. Moreover, it may be possible for capacitive loads to resonate with the inductance of the distribution transformer and cause the signal attenuation to vary wildly with frequency.

III.2 - Noise

The principal source of noise is caused by appliances connected to the same transformer secondary to which the power line carrier system is connected. The two primary sources of noise will be triacs used in light dimmers and universal motors. Triacs generate noise synchronous with the 50Hz power signal and this noise appears as harmonics of 50Hz. Universal motors found in mixers, sewing machines, and sanders also create noise, but it is not as strong as light dimmer noise, and not generally synchronous with 50Hz. Furthermore, light dimmers are often left on for long periods of time whereas universal motors are used intermittently. The Figure 3 shows noise sources as well as background noise in a typical residential environment.

Figure 2 : Aggregate European Power Line Impedance (by Malack and Engstrom)

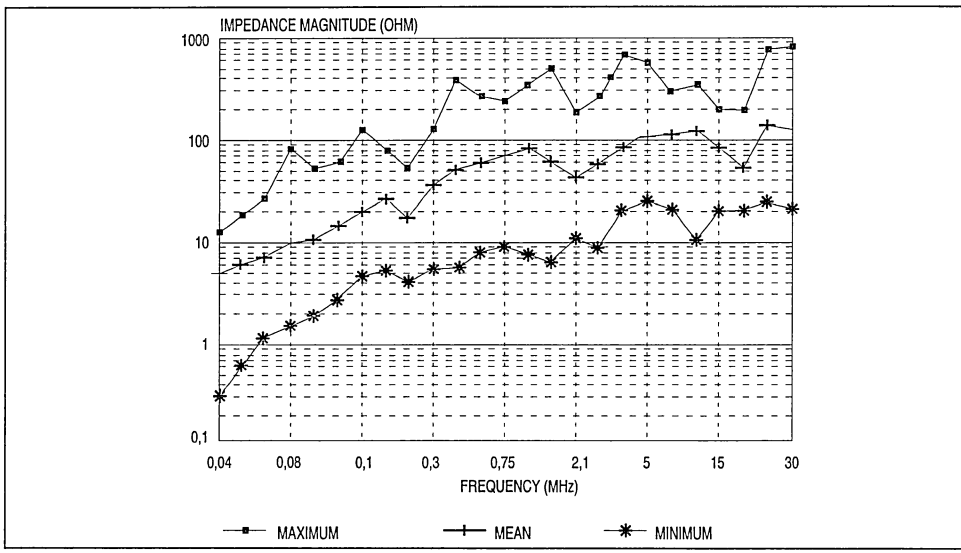
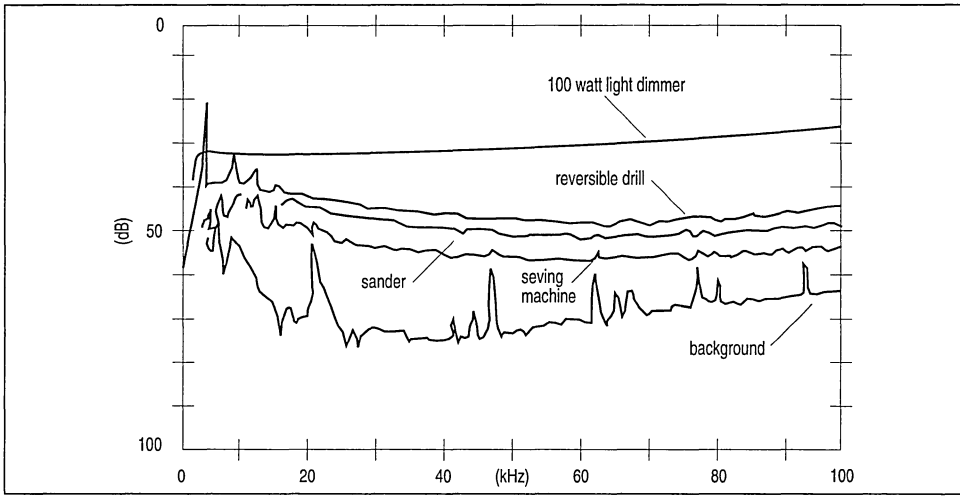


Figure 3 : Voltage spectra for 3 universal motors compared to light dimmers operating into the 60Hz power circuit (by Vines, Trussel, Gale and O'Neal Jr.)



III.3 - Standing Waves

Standing wave effects will begin to occur when the physical dimensions of the communication medium are similar to about one-eight of a wavelenght, which is about 375 and 250 meters at 100 and 150kHz respectively. The length of the communication path on the secondary side of the power distribution system will be determined primarily by the length of the triplex wire connecting the residences to the distribution transformer. Usually, several residences use the same distribution transformer. It would be rare that a linear run of this wiring would exceed 250 meters in length although the total length of branches might occasionally exceed 250 meters. Thus standing wave effects would be rare at frequencies below 150kHz for residential wiring..."

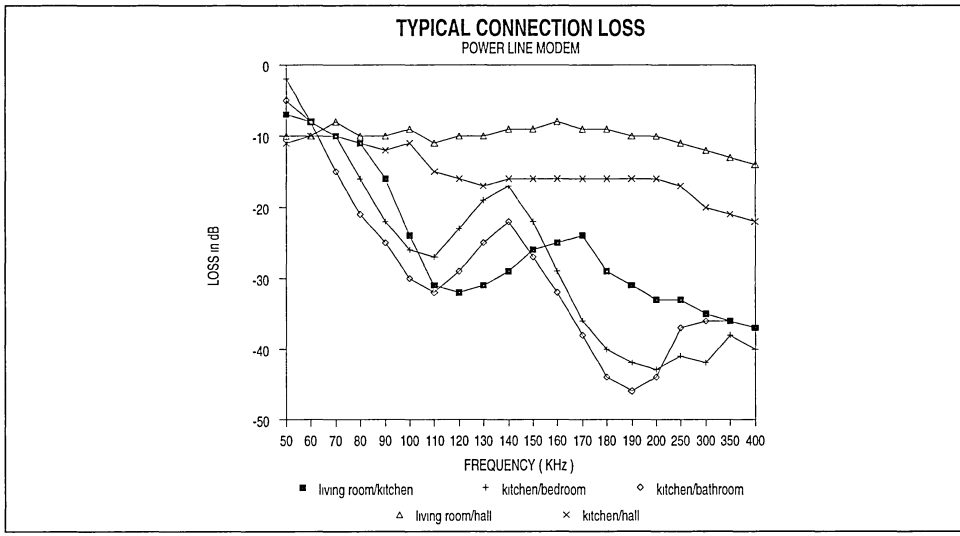
III.4 - Typical Connection Loss (see Figure 4)

We notice two classes of value at a transmit frequency of about 130kHz :

- from 10dB to 15dB : in this case, the transmitter and the receiver are connected to the same branch circuit.
- from 20dB to 30dB : in that case, the transmission path goes from one branch circuit to another through the service panel which induces an additional attenuation of 10dB to 20dB.

Therefore, the transmit range of a home automation system depends on the physical topology of the electric power distribution network inside the building where the system is installed.

Figure 4 : Static Attenuation for Several Paths (by Daniel CHAFFANJON)



IV - ST7537 POWER LINE MODEM

Fabricated in analog CMOS technology, the ST7537 transmits and receives data up to 1200bps in half duplex mode using a carrier frequency of 132.45kHz, complying with Europe's CENELEC EN 50065 standard (which specifies the use of 125kHz to 140kHz carrier frequencies for home automation) and US FCC regulations (which specifies the use of carrier frequencies lower than 450kHz).

Frequency-shift keying is used for transmission, a fundamental design choice that makes it possible to achieve rugged transmission in a very noisy electrical environment at an affordable cost for high volume consumer markets. Among the alternatives, amplitude-shift keying is too susceptible to noise and spread-spectrum, though theoretically more reliable, requires complex and costly circuits. Moreover, field trials in a critical remote utility meter reading application have proven the dependability of the SGS-THOMSON approach.

Included on the chip are all of the functional blocks necessary for the transmission and reception of data over power lines. In addition to this IC the only external components needed are a line driver and a transformer, plus, of course, the microcontroller that prepares and interprets message data.

Transmit data enters the FSK modulator asynchronously with a nominal intra-message data rate of 1200bps. Inside the modulator, the data is transformed into two frequencies (133.05kHz for a "0" and 131.85kHz for a "1"), derived from an inexpensive 11.0592MHz crystal.

The modulated signal from the FSK modulator is filtered by a switched-capacitor bandpass filter (TX bandpass) to limit the output spectrum and to reduce the level of harmonic components. The final stage of the transmit path consists of an operational amplifier which needs a feedback signal from the power amplifier.

In the receive section, the incoming signal is applied at the RAI input (with a typical sensitivity of $1mV_{RMS}$) where it is first filtered by a switched-capacitor bandpass filter with a pass band of around 12kHz, centered on the carrier frequency. The output of the filter is amplified by a 20dB gain stage which provides symetrical limitation for overvoltages. The resulting signal is downconverted by a mixer which receives a local oscillator synthesized by the FSK modulator block.

Finally, an intermediate frequency bandpass filter whose central frequency is 5.4kHz improves the signal-to-noise ratio before entering the FSK demodulator. The coupling of the intermediate frequency filter output to the FSK demodulator input is made by an external capacitor which cancels the receive path offset.

In the ST7537 there are two important additional functions: the carrier detector and the watchdog. Carrier detection is needed because in practically all applications more than two appliances will be connected to the power line. Before attempting to

transmit, an appliance must first check that there is no carrier present, and if there is, it must wait and retry later.

The watchdog function is provided to ensure that the modem's control micro is functioning correctly. Software in the micro must include instructions that send a pulse to the watchdog input of the ST7537 at least once every 1.5s. If no negative transition is observed at this input for 1.5s a reset signal is generated to restart the micro. This watchdog monitor scheme ensures that any disruption caused by glitches are quickly corrected.

V - DEMOBOARD FEATURES

Power line interface

The power line interface has been designed in order to follow the CENELEC EN 50065-1 and US FCC specification. It has to amplify and filter the output signal of the ST7537.

Test pin

It is possible to program the different test modes of the ST7537 with the switches SW1, SW2, SW3 and SW4 corresponding to TEST1, TEST2, TEST3 and TEST4. The most important test mode is TEST1 which allows continuous transmission.

RS232C interface

On the application board, there is an RS232C interface allowing you to debug your system. This interface is connected to the ST7537 by four switches SW5, SW6, SW7 and SW8.

Remark : It is mandatory to provide the watchdog clock to the ST7537.

Wrapping area

You can wire your application and do its debug by connecting relevant digital signals to SW5, SW6, SW7 and SW8 (pin not used) and watchdog, master clock and RSTO.

VI - HARDWARE DESCRIPTION

VI.1 - About CENELEC Specifications

The CENELEC specifications are given for an imaginary network (50Ω/ 50µH + 5Ω) simulating the power line. This network looks like a 54Ω impedance at a transmit frequency of 132.45kHz. The transmitted signal is measured in relation to a reference of this network (see Annexe B). With this configuration, some of the specifications are :

- maximum output level : 116dBµV
- harmonics level of less than 46dBµV mean.

In this chapter, the transmitted signal is measured between the phase and the neutral of the simulated power line. Then, the measured voltages are twice the ones measured with CENELEC test configuration. Thus, it is necessary to add 6dBµV to the specifications given above :

- maximum output level : 122dBµV
- harmonics level of less than 52dBµV mean.

Henceforth, these values will be used .

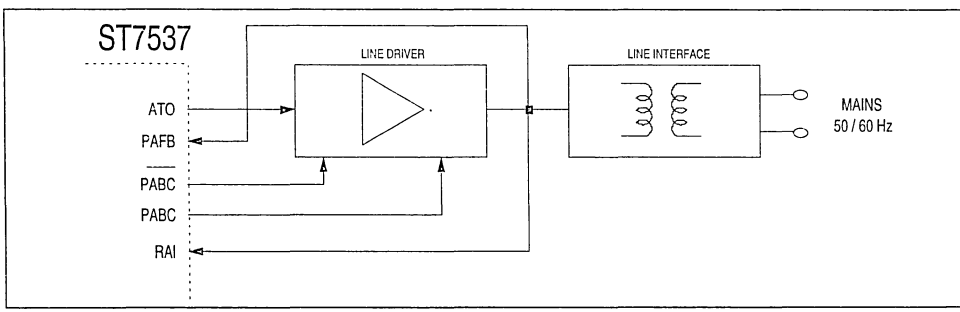
VI.2 - Power Line Interface

The power line interface connects the ST7537 to the power lines and meets the CENELEC and FCC specifications. It has the following functions :

- in transmit mode : to amplify and filter the transmit signal (ATO) from the ST7537
- in receive mode : to provide received signal from powerlines to the receive input (RAI) of the ST7537
- protection against spikes and overvoltages.

It is composed of a line driver and a line interface as it is shown in Figure 5.

Figure 5 : Power Line Interface Description



In transmit mode, the power line interface has to be able to drive, via the line interface, power lines with impedances from 1 to 100Ω. The line interface is not only used to put signals on the power line. It is also used as a bandpass filter, in order to reduce the harmonics of the transmit signal to a level of less than 52dBμV .

In receive mode, the line driver is switched off to avoid the low output impedance of the line driver attenuating the received signals and to save energy costs.

VI.2.1 - The Line Driver

The line driver has to amplify the output signal (ATO) of the ST7537 (see Figure 6).

First, a normal Push-Pull amplifier has been set up with two bipolar transistors Q4 (2N2222) and Q3 (2N2907). These types of transistors (2N2222 and 2N2907) have been chosen as they are cheap and widely used.

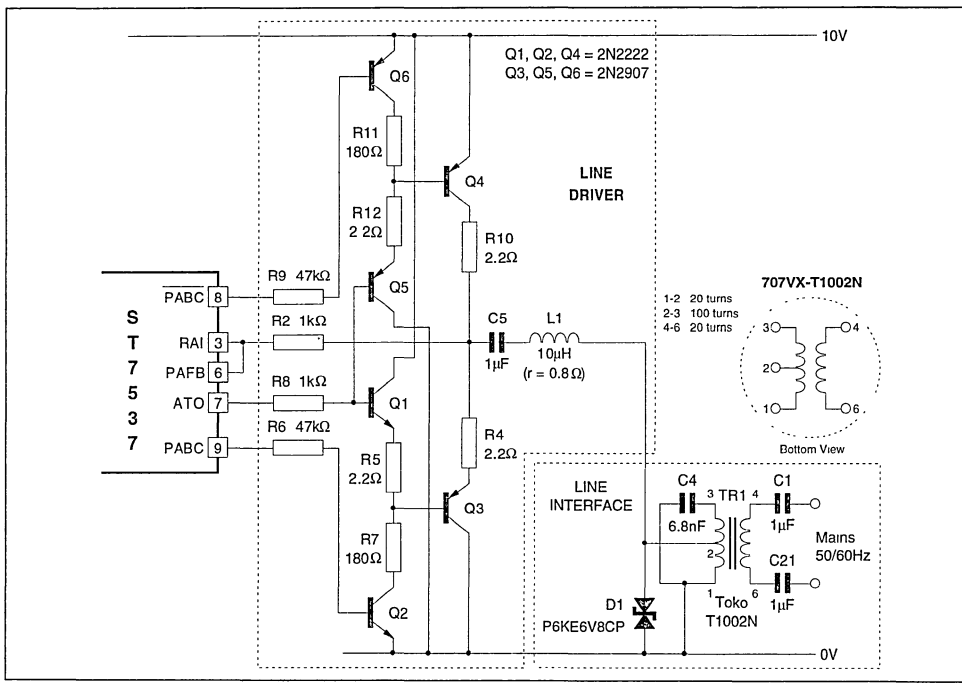
The resistors R4, R5, R10 and R12 degenerate the emitter of Q5, Q4, Q1, Q3 in order to define the bias current of the ouput branch independently of the mismatch of the transistors. The Push-Pull is polarized with two common collector amplifiers composed of Q1 (2N2222) and Q5 (2N2907). As far as resistors R7 and R11 are concerned, their value (180Ω) has been defined to obtain the optimum performances of the amplifiers thus define the bias current of the system.

The bipolar transistors Q2 (2N2222) and Q6 (2N2907) are used to switch off the power amplifier during the receive mode, thanks to the ST7537 output signals PABC and $\overline{PABC}$ which follow the Rx/Tx mode.

In order to avoid thermal runaways, it is mandatory to connect thermically Q1/Q4 and Q3/Q5. This is possible since the collectors of the transistors used are connected to the metal package. Consequently, both transistors will have the same temperature.

Main characteristics of the line driver :
- voltage gain = 1
- high input impedance
- low output impedance

Figure 6 : Power Line Interface Schematics



VI.2.2 - The Line Interface

In order to adapt the line driver to the power line, a transformer is used (see Figure 6). This transformer has :

- to isolate the rest of the interface from the power line
- to put the transmit signal on the power line
- to extract the received signal from the power line
- to filter 50Hz/60Hz signal coming from the power line
- to filter the harmonics of the transmit signal.

The used transformer is a TOKO T1002N. It has two primary windings and one secondary winding. The ratios of these windings are 4:1:1 (turns). Typical values of the transformer are :

- L1t windings : 9.4µH
- L4t windings : 140µH.

The primary windings of the transformer are used to create a bandpass filter. The resonance frequency is set at the transmit frequency with C4. This capacitor is in parallel with the primary winding (1t/4t). The equivalent value for those two windings can be calculated according to :

$$Leq = L1t + L4t + 2M$$

$$M = k \cdot \sqrt{L1t \cdot L4t}$$

With the given values :

$$k = 1/2^{1/2}$$
$$M = (9.4\mu H \cdot 140\mu H / 2)^{1/2} = 25.7\mu H$$
$$Leq = L1t + L4t + 2 \cdot M = 200.7\mu H$$

The resonance frequency of this LC network is dependant of C4 and Leq according to :

$$Fres = \frac{1}{2\pi \cdot \sqrt{Leq \cdot C4}}$$

$$C4 = \frac{1}{Leq \cdot (2\pi \cdot Fres)^2}$$

For Fres = 132.45kHz → C4 = 7.2nF (6.8nF is chosen since it is the nearest capacitor value available).

The capacitor C4 must be very linear in order avoid harmonic distortion. That's why a KS (styroflex or NPO ceramic capacitor) capacitor has been used.

In order to filter the 50Hz/60Hz signal from the powerlines, C1 is used. The capacitor filters the low frequencies (50Hz/60Hz) and lets the high (Transmit) frequencies pass. It is a class X2 capacitor. These capacitors have a short circuit protection, which is absolutely necessary. Indeed if a short circuit in the capacitor occurs, the 50Hz/60Hz filtering is lost, and the powerline interface will be destroyed, or worse, danger might occur for persons working with the interface and the ST7537. Moreover, since the TOKO transformer cannot overcome higher than 800V spikes, the safety norms are not met and the capacitor C1 is required to comply with them. An additional capacitor C21 is used as the phase location is unknown.

As a final protection against any possible spikes, a transil (TRL1) is used. It is a 6.8V bidirectional type. If a voltage greater than 6.8V appears, voltage between pins of the system will be set to 6.8V, protecting the other parts of the power line interface from damage.

R1 is added to discharge C1 after disconnecting the interface from the powerline. Without this resistor, C1 will not be discharged and schock hazard might occur if someone touches the powerline connector. This resistor is only useful in evaluation systems. In all other cases where disconnection from the power line never takes place, R1 can be removed, saving undesired energy loss.

VI.2.3 - The Power Line Interface

The complete power line interface has been described in the two preceding parts. The interface has to be connected to the ST7537 as described in Figure 7.

The ATO and RAI are the analog output and input from/to the ST7537. The control of the transmit/receive mode is made with PABC and PABC signals from the ST7537. A high output (+10V) on PABC line selects the transmit mode, whereas a low output (0V) selects the receive mode.

The "pwr" outputs are the power line connections. On the application board, these connections are located close to C1 and the transformer in order to avoid long tracks carrying high voltage.

VI.2.4 - Performances of the power line interface

The following tests have been done on the power line interface :

- output impedance of the powerline interface versus the frequency
- Bit Error Rate (BER) test
- spectrum analysis of the transmit signal.

VI.2.4.1 - OUTPUT IMPEDANCE OF THE POWER LINE INTERFACE VERSUS THE FREQUENCY

The output impedance of the power line interface is measured with an impedance analyzer as it is shown in Figure 8. The board is set in receive mode.

The results are given in annexe B.

Test equipment : 41924 LF Impedance Analyzer
5Hz-13MHz (Hewlett Packard)

Test conditions : T = +25°C

Figure 7 : Power Line Interface Inputs and Outputs

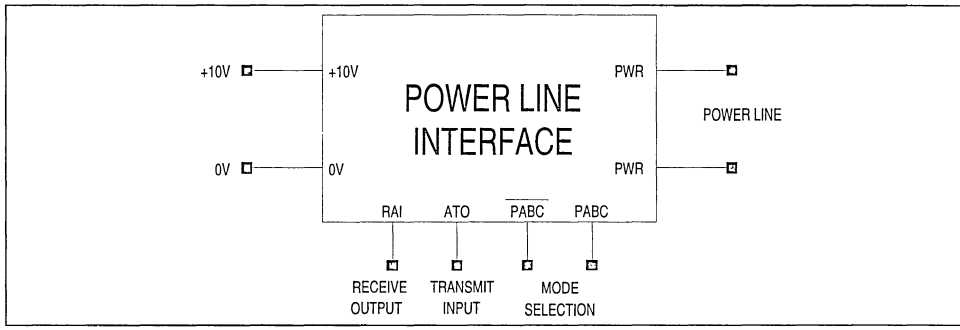
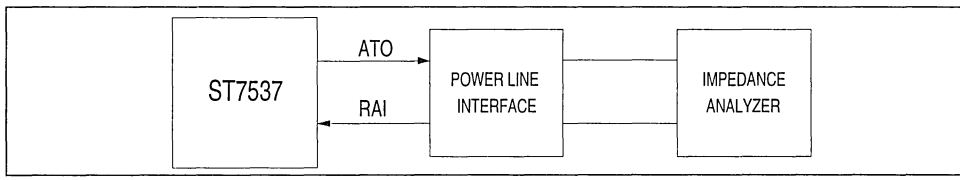


Figure 8 : Output Impedance Measurement Configuration



VI.2.4.2 - BER TEST

Two boards are required : one for the transmission, the other one for the reception.

White noise is added to the ATO transmit output of the ST7537 thanks to a mixer. The aim is to measure the BER under different Signal/Noise ratio conditions. The mixed signal is transmitted to the RAI receive input of the modem. The digital signal injected in TxD is a 2^{15}-1 pseudo-random pattern long, generated by a bit error rate analyzer (with internal 1.2kHz asynchronous clock).

In the reception board, a 1.2kHz clock (CRX) is built thanks to the ST7537 MCLK clock. The received digital signal RxD is amplified (RxDL) and synchronized with the CRX clock. Both of them (CRX and RxDL) are analyzed by the BER analyzer.

The measurements are made with different RAI input level. The Figures 10 and 11 gives respectively the B.E.R with a RAI input level of 10.023mV$_{RMS}$ and 1.14mV$_{RMS}$.

Conclusion

Under the test conditions of the ST7537 specification (RAI = 10mV$_{RMS}$ and S/N = 15dB) the BER is 4.10-7. With an RAI input level of 1.14mV$_{RMS}$ the BER is around 10-4 with the same S/N ratio. Therefore, the ST7537 is able to communicate with low input signal level of about 1mV$_{RMS}$. This test illustrates the high sensitivity of the power line modem.

In Figure 10, the measured BER (with an RAI input level of 10mV$_{RMS}$) is compared with the theorical BER of a conventional BFSK modulator/demodulator.

Test equipment : SI7703B BER analyzer
Rhode and Schwartz noise generator

Test condition : T = +25°C

Figure 9 : BER Test Configuration

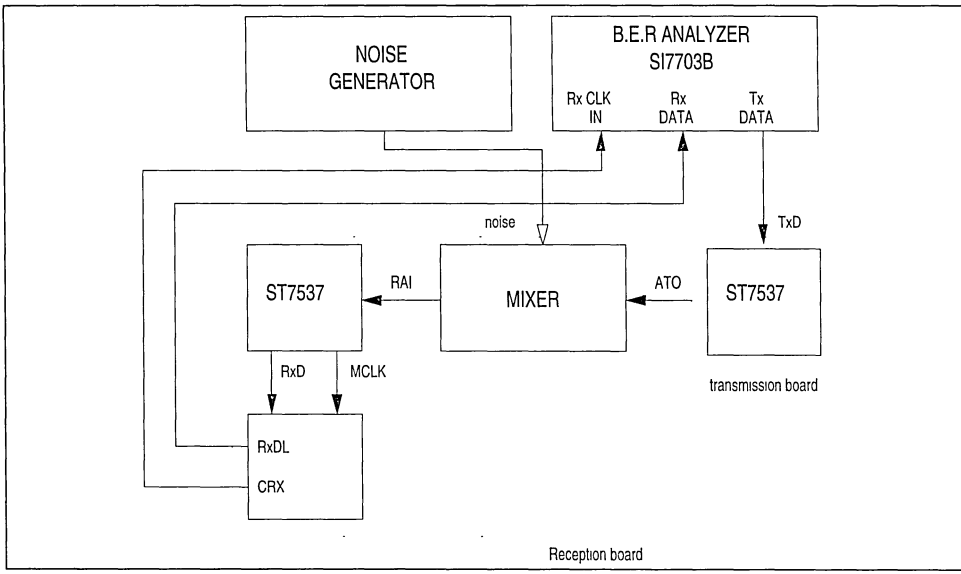


Figure 10 : BER Test for an RAI Input Amplitude of 10.023mV$_{RMS}$

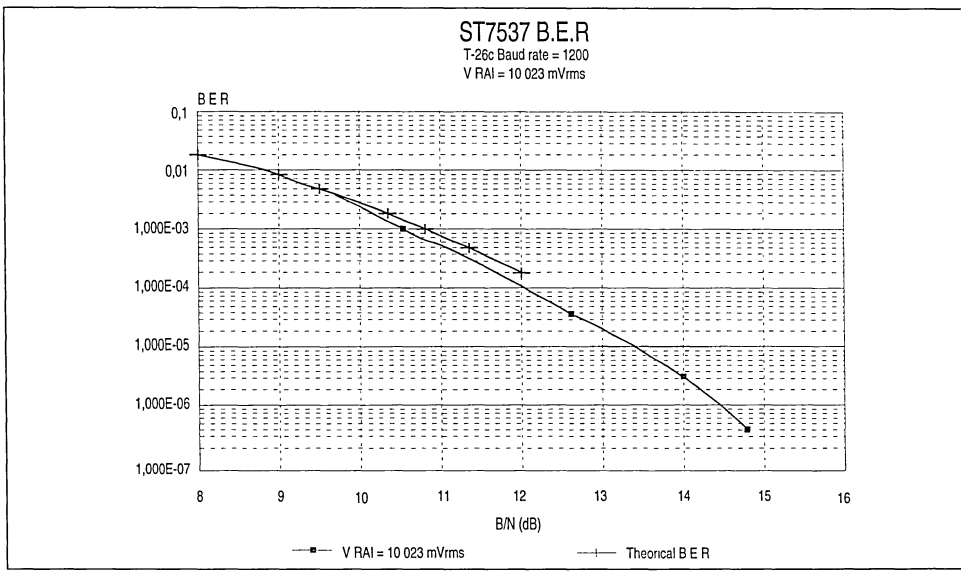
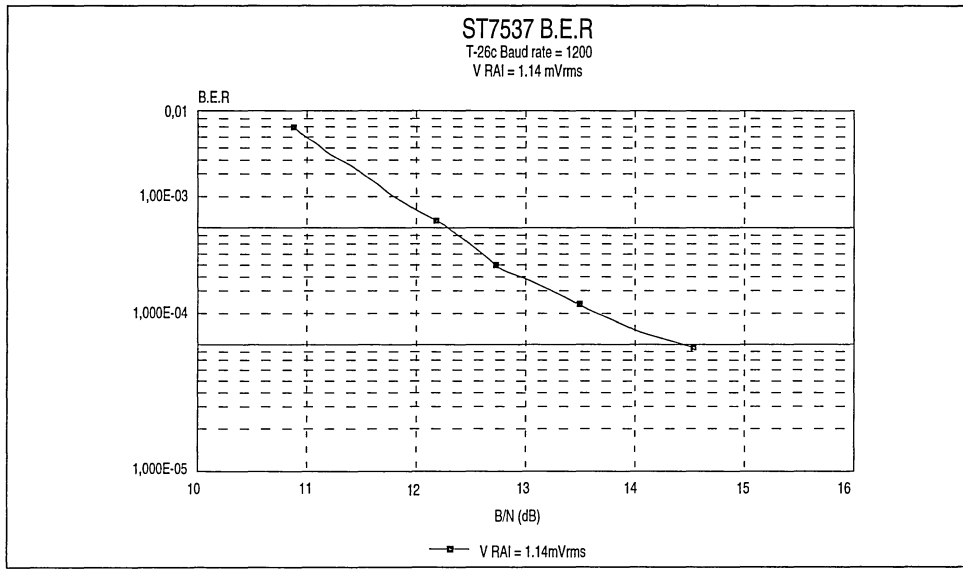


Figure 11 : BER Test for an RAI Input Level of 1.14mV$_{RMS}$



VI.2.4.3 - TRANSMIT SIGNAL SPECTRUM ANALYSIS

The transmit output signal of the power line interface is measured with the power line simulated by resistors : R = 1, 5, 10, 50, 100Ω.
A spectrum analyzer is used to display the output signal frequency spectrum of the power line interface (see Figure 12).

In a first design of the board, a 2.2Ω resistor was used instead of the inductance L1. In this configuration, whatever the power line impedance, the output level was at least 106dBµV up to 119dBµV (see Figure 13). Thus no communication problems had been noticed during the test session.
To improve the frequency spectrum of the transmit signal, the resistor has been replaced by an inductance L1 of 68µH, 1.6Ω (see Figures 14 and 15).

However, tests on a real site showed that the transmit level was very low with this inductance in case of low power line impedance : with an impedance of 1Ω, the output level is 87dBµV, so that communication difficulties occur. At the transmit frequency (132.45kHz), the inductance looks like an impedance of about 56Ω, which introduces significant attenuations on the transmit signal compared to those induced by the 2.2Ω resistor.

To improve the output signal amplitude, the inductance value must be modified. A compromise has to be found between filtering the pertubation voltages and lowering the impedance of the inductance at the transmit frequency. An inductance of 10 µH (0.8Ω) has been chosen which looks like an impedance of 8Ω at 132.45kHz frequency (see Figures 16 and 17).

Figure 12 : Spectrum Analysis Configuration

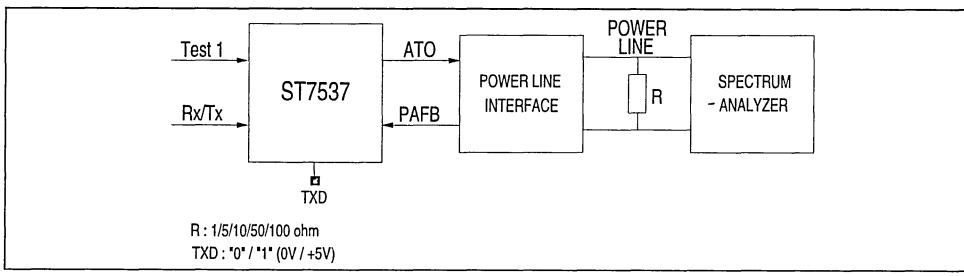


Figure 13 : Output Transmit Level (dBµV) with 2.2Ω Resistor

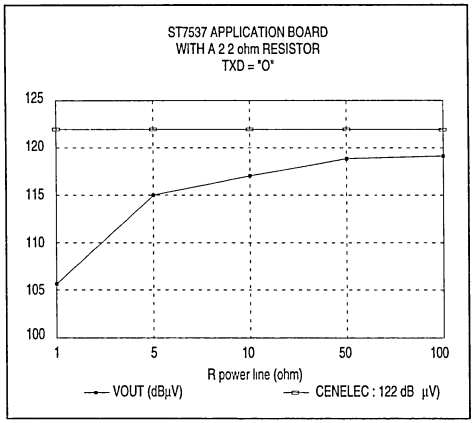


Figure 14 : Output Transmit Level (dBµV) with 68µH Inductance

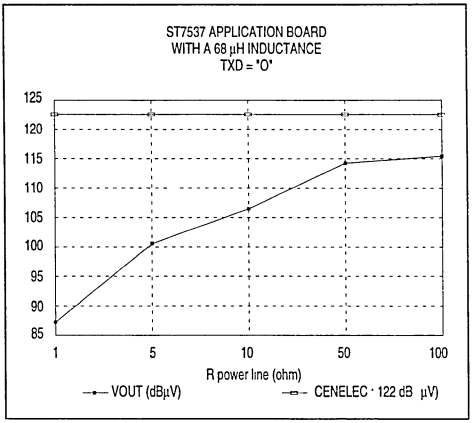


Figure 15 : Second and Third Harmonics Level (dBµV) with 68µH Inductance

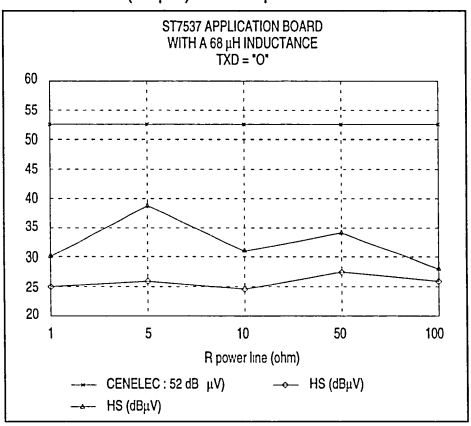


Figure 16 : Output Transmit Level (dBµV) with 10µH Inductance

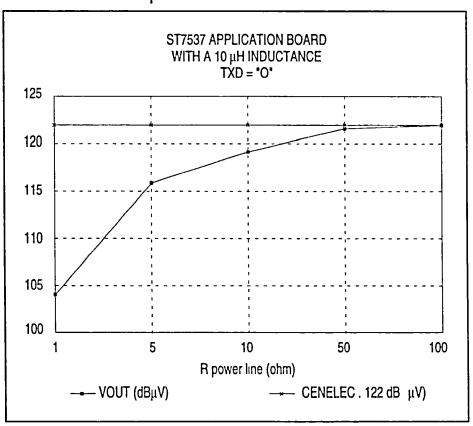
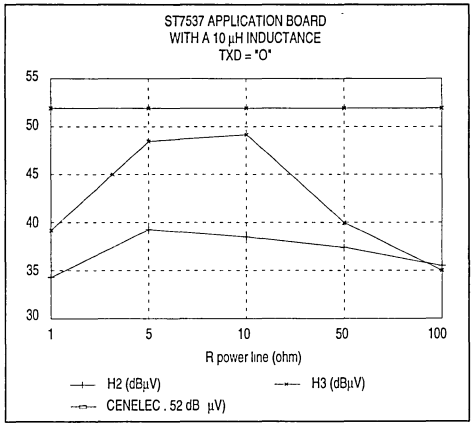
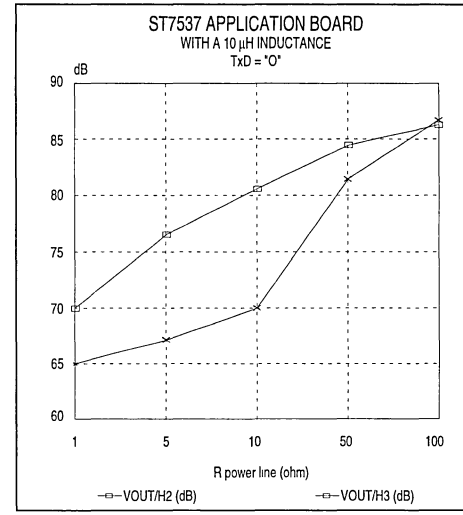


Figure 17 : Second and Third Harmonics Level



VOUT/H2 and VOUT/H3 variations with the 10µH inductance versus the power line impedance are given in Figure 18.

Figure 18 : Demoboard Transmit Performances



Test results (with L1 = 10µH)	CENELEC specifications	FCC specifications
VOUT < 122 dBµV	VOUT < 122 dBµV,	
H2 < 39 dBµV	H2 < 56 dBµV mean	H2 < 48 dBµV (extended to 60 dBµV)
H3 < 49 dBµV	H3 < 52 dBµV mean	H3 < 48 dBµV (extended to 60 dBµV)
VOUT/H2 > 70 dB		
VOUT/H3 > 65 dB		

Conclusion

With L1 = 10 µH, the required harmonics level is reached and the output voltage is smaller than 122 dBµV. Therefore, the power line interface is fully operating according to the CENELEC and FCC specifications. Moreover, for very low power line impedances, the output transmit level is high enough to ensure a good communication quality.

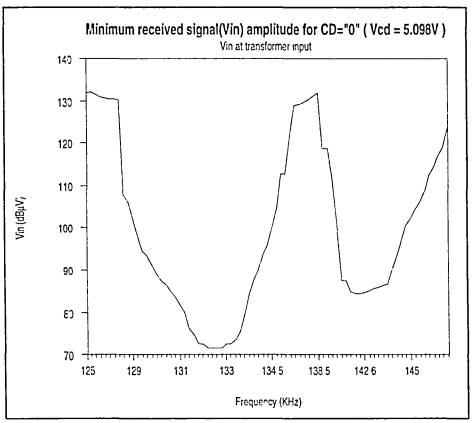
Test equipment : 3585A Spectrum Analyzer 20Hz-40MHz (Hewlett Packard)
Test conditions : T = +25°C

VI.3 - Carrier Detect

The carrier detect output ($\overline{CD}$) is driven low when the input signal amplitude on RAI is greater than V_{CD} typically $5mV_{RMS}$ for at least T_{CD} (typically 4ms). When the input signal disappears or becomes lower than V_{CD}, $\overline{CD}$ is held low for at least T_{CD} before returning to a high level. V_{CD} input is the carrier detection threshold voltage which is set internally.

The graph, given in Figure 19, represents the minimum amplitude of the received signal which can be detected (which corresponds to $\overline{CD}$ = 0) according to the frequency. Thus input signals at a frequency of 133.05kHz (high logic level) and 131.85kHz (low logic level) can de detected at a very low level. For frequencies smaller than 129kHz or greater than 150kHz, the detection is made at a very high level of input signal. Therefore, only significant frequencies received signals are detected.

Figure 19 : RAI Input Minimum Detection Level



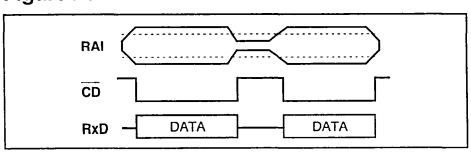
7537-61 AI

VI.4 - Improving Sensitivity

In all modem, the carrier detector clamps the outgoing digital data RxD when the incoming analog receive signal is below a defined level (carrier detector level 7537 typ = $5mV_{RMS}$).

That means we are loosing the data when the signal is less than $\overline{CD}$ level.

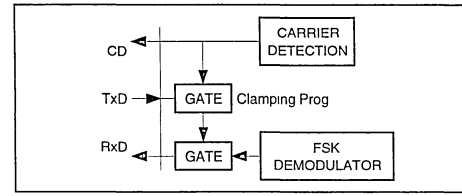
Figure 20



7537-40 EPS

In the ST7537, the clamping of $\overline{CD}$ on RxD is programmable thanks to TxD pin.

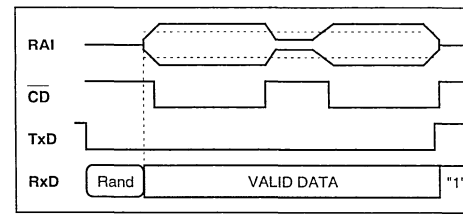
Figure 21



7537-41 EPS

So we are able to receive data even if the incoming analog receive signal is less than 5mV. When removing the clamping of RxD by $\overline{CD}$ we are able to get RxD data without error with a receive level of 400 micro Volt.

Figure 22



7537-42 EPS

As you can see on previous Figure even when RAI is lower than the carrier detect level we get the datas because TxD = "0".
When TxD = "0" and the receive signal is not one of the 7537 (e.g Noise), the RxD is random (in most configuration the RxD is at "0").

Example of Implementation

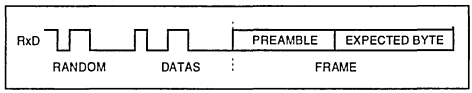
We have seen that by programming the TxD to "0" in receive mode we increase the sensitivity of the ST7537 because there is no more clamping by $\overline{CD}$. You will be able to have good communication with a receive signal of around 50dBµV which means a dynamic of around 70dB.

Because we want to get the benefit of the very good sensitivity of the ST7537, we will program TxD to "0" in receive mode and create by soft a frame detector. We will use the $\overline{CD}$ signal as mentionned by CENELEC only when we want to transmit a frame.

Different software frame detector can be implemented depending of the ressources of your microcontroller.

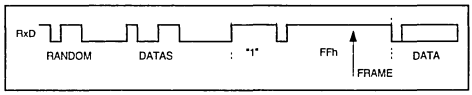
You can program your microcontroller to go in receive frame when it received the expected byte.

Figure 23



So the preamble is for demodulator training (when you start a communication the 3 first bits are lost by the receiver) and when you will match with expected byte the microcontroller will go in receive frame routine.
On the ST6 microcontroller we have implemented the following frame detector.

Figure 24



We put TxD = "1" on the transmitter for around 4ms (for demodulator training) and after we send in asynchronous mode FFh following by the complete frame.
On the receiver, we check that we have RxD equal to "1" for at least 7ms (we are looking for FFh), then we go in receive and we will have frame synchronization on the first start bit of the data.
We did a trial in our lab with this system during 2 hours without having the ST6 going in frame receive routine on bad datas dued to noise signal.

VI.5 - Communication with a RS232C Interface

The application board can be connected to a Personal Computer (PC) thanks to the RS232C interface. As the electrical levels of the RS232 port (±12V) do not match the electrical levels of the ST7537 (TTL levels 0/+5V), a MAX232 is used to make communication possible. This device has two RS232 receivers to convert RS232 levels into TTL levels and two RS232 transmitters to convert TTL levels into RS232 levels. The connections between the ST7537 and the RS232 interface are given in Figure 25. Not all the pins from the RS232 port are used. The RXD, TXD and Carrier Detect (CD) signals are directly converted. The Request To Send (RTS) line is used to set the ST7537 in receive or transmit mode, but also to give the PC a Clear To Send (CTS) signal. The Data Set Ready (DSR) line is connected to the Data Terminal Ready (DTR) line. This simulates the transmission of the DSR signal by the power line modem when the PC is ready. The RI output of the PC is only used for telephone network modems, and therefore it is not connected. If the RS232 port of the PC is used, it is necessary to provide the board with a watchdog clock (e.g : 1kHz) in order to get the PC communication working. A suggested clock generator is given Figure 26. It uses a NE555 timer working in astable mode.

The output HIGH time of the clock is :
$t_H = 0.693*(R1 + R2)*C1$

The output LOW time of the clock is :
$t_L = 0.693*(R2)*C1$

Thus the total period T is : $T = t_H + tL$
The frequency of oscillation is : $f = 1/T = 1/(t_H + t_L)$

Calculations provides the following results :
R1 = 1kΩ, R2 = 100kΩ, C1 = 7nF.

Figure 25 : Connections between ST7537 and RS232 Interface

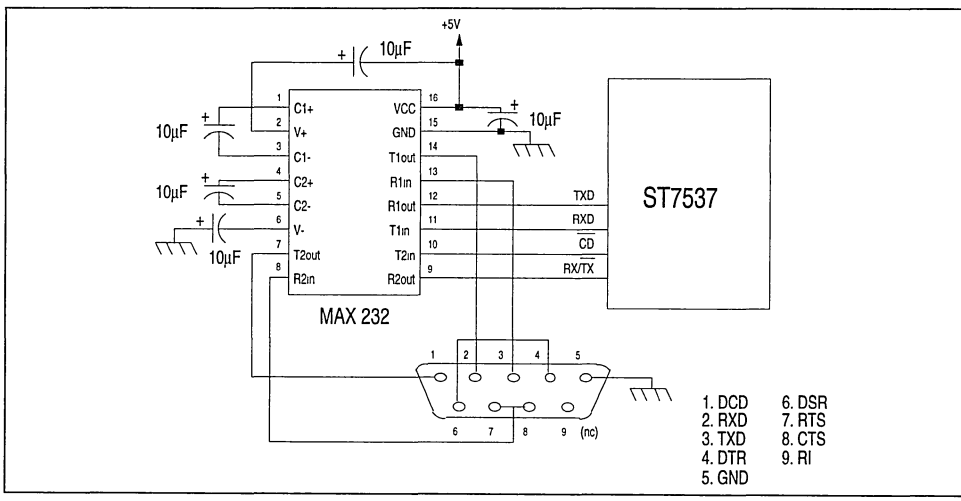
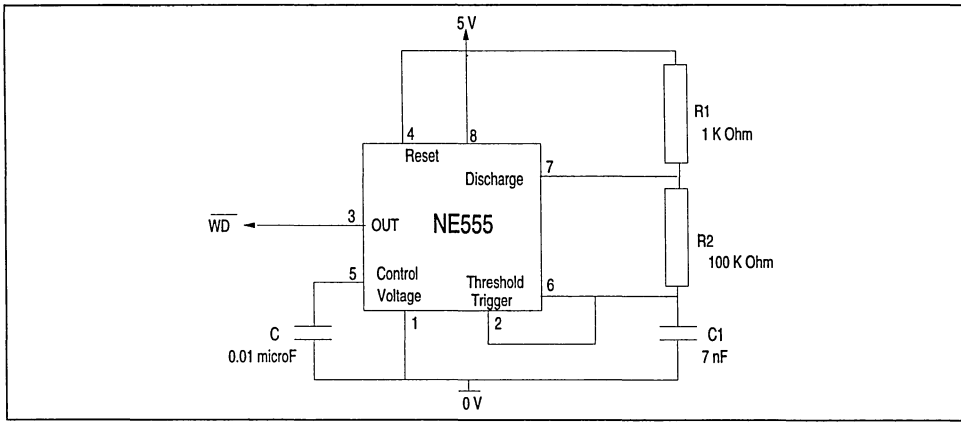


Figure 26 : Watchdog Clock



RS232C Communication Problem

We have discovered that with some computer the communication program does not work correctly. In some new PC generation the UART is sensitive to the RxD jitter and then shows characters errors on PLM communication.

The following hardware avoid the jitter on RxD for the UART of the PC.

Figure 27

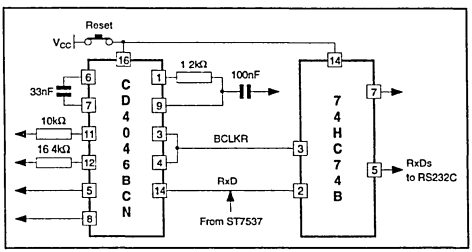
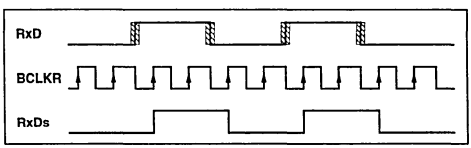


Figure 28



After power-up the 7537 demoboard, you have to reset the receive recovery block.

Before doing this extra hardware we recommend you to test your PC with the new program and if there are time to time some errors the hardware has to be adapted as shown above (you can use BCLKR for the watchdog clock).

VI.6 - Demoboard Communicating Application

The ST7537 power line modem enables you to design "communicating" appliances, which meet your specific requirements and comply with the CENELEC specifications. Equipped with a single low-cost ST90E28 microcontroller, it makes it possible to build a "smart" home network, where each device is able to use any information required either if it is local (sensors) or remote (inside any other communicating appliance).

This paragraph is intended to provide design basics for the implementation of the ST90E28 on the ST7537 demoboard.

VI.7 - Overview of the ST90E28 MCU

The ST90E28 microcontroller chosen to equip the ST7537 demoboard is a 16Kbyte program memory EPROM version with 256 bytes of RAM and 256 bytes of register file. Within this file, 224 general purpose registers are available as RAM, accumulators or index pointers, allowing code efficiency. This MCU has an internal clock generator, a 16-bit watchdog timer for system integrity, a powerful serial communications interface (SCI) with included baud rate generator and outstanding character search capability, and a 16-bit multifunction timer for complex user applications; it provides a reset input and up to 36 input/output pins, including 7 external interrupts and a non-maskable interrupt.

Most of the instructions take 14 clock cycles: with a clock frequency of 11.0592MHz, one instruction lasts about 90ns. Connected to the ST7537, the microcontroller has to deliver a maximum bit rate of 1200 bauds: one bit is at least 833µs long.

VI.8 - Implementation of the ST90E28 MCU

Two configurations have been set up, one for the slave appliances, and one for the master system. Both versions will have their address initialized in the software in this first release. Besides, they use one data output to display information about the main program execution by means of a led: you know that the main program is running well, when this led is blinking as the appliance is powered on. The main differences between the two controllers are the input/ouput facilities.

The slave configuration provides an ouput that switches a load. This load will be simulated by a LED (see Figure 29).

The master configuration provides a 3-bit command input to control the slaves. This command will be simulated by a KEYBOARD : one key is available for each slave, and one specific key enables the user to supervise all the slaves inside a room at once. This configuration also uses a 3-bit data output to let you know whether a particular slave is on, or whether the room is lit up. This information will be displayed by one led attached to the key dedicated to a particular device (see Figure 30). All the slaves addresses will be stored in the master version of the software.

Furthermore, both configurations need a 7 bit data exchange with the ST7537 : clock, transmit data, receive data, reset, Rx/Tx control lines (see Figure 31). No external component is needed to interface the microcontroller with the power line modem, allowing cost savings.

- OSCIN (Pin 2) : The MCU oscillator is driven with the PLM master clock, so that no additional crystal is needed. In this case, the oscillator output pin must stay unconnected.
- Port 5 bit 1 (Pin 42) : This output bit provides the PLM watchdog input with negative transitions, before the timeout end is reached. The watchdog pulses must be at least 500ns wide with a period of at least 800µs and up to 1.5s.
- Port 5 bit 0 (Pin 43) : This output controls the Rx/Tx mode. When this bit is 0, the transmit mode is set, otherwise the receive mode is selected. Remember that the ST7537 switches automatically in the receive mode, when this bit is held at 0 longer than 1s.
- INT1 (Pin 26) : The PLM carrier detect signal channels through this external interrupt input pin, which is triggered on falling edge. On signal detection, the carrier detect output is driven low and generates an interrupt request.
- SOUT (Pin 30) : The microcontroller provides the ST7537 with Tx data by means of the SCI output.
- SIN (Pin 31) : The ST7537 provides the microcontroller with Rx data through the SCI input.
- NMI (Pin 18) : The PLM reset output signal acts as an MCU external watchdog, in order to detect hardware or software failures. This signal channels through the MCU external non maskable interrupt input pin, which is triggered on rising edge. When the power supply is too low or when no negative transition occurs on the PLM watchdog input for more than 1.5s, the reset ouput is driven high and generates a top level interrupt request, which resets the microcontroller. As for the MCU internal watchdog timer, the watchdog mode is disabled, so that a second 16-bit programmable timer is available for customer applications.

Figure 29 : Slave Configuration

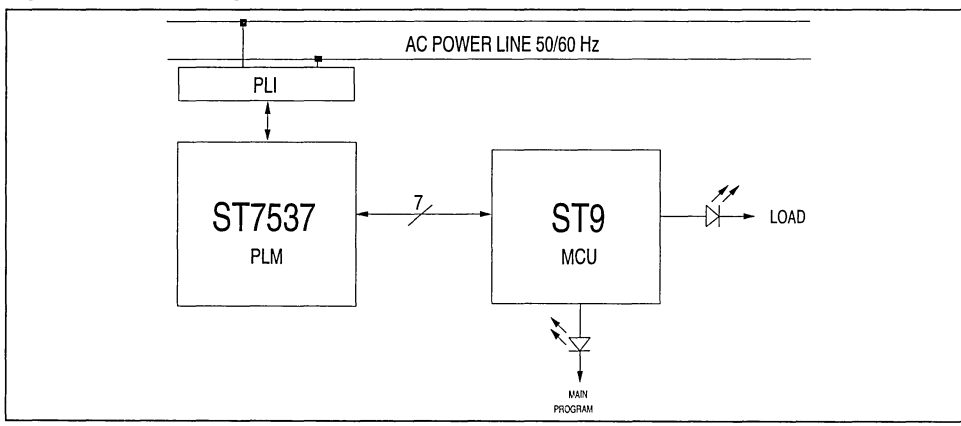


Figure 30 : Master Configuration

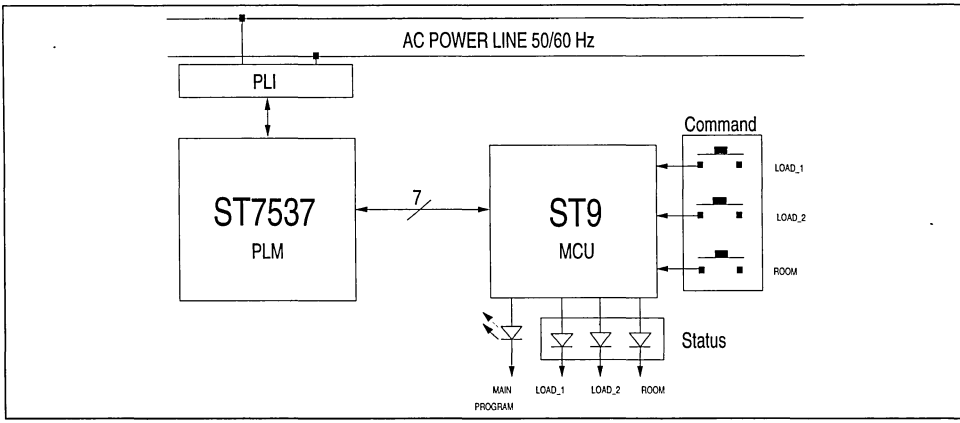
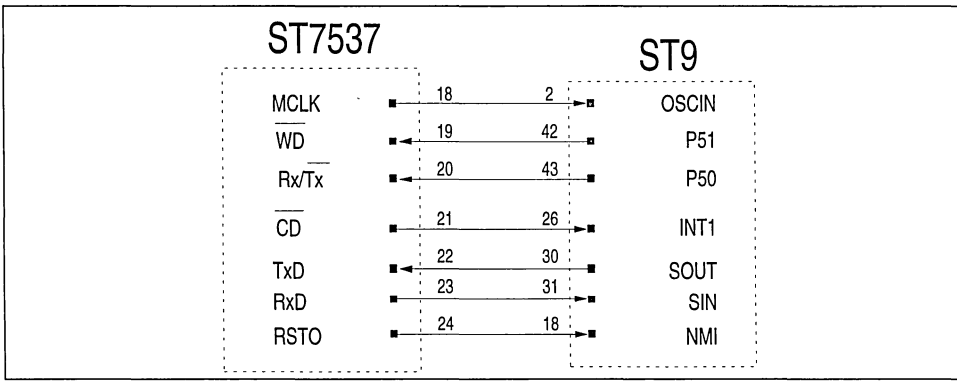


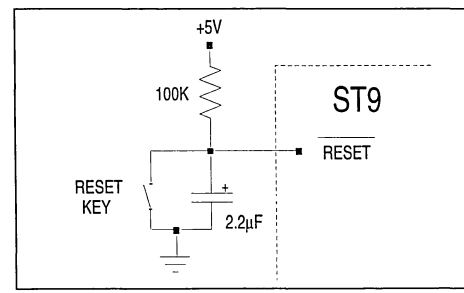
Figure 31 : Interface between ST7537 and ST90E28



VI.8.1 - Applicative Pin Configuration

- V_{SS} (Pin 1) : Digital Circuit Ground
- V_{DD} (Pin 21) : Main Power Supply Voltage +5V. A decoupling capacitor of 47µF is connected between V_{DD} and V_{SS} pins. The V_{DD} of the microcontroller should be connected also to the DV_{CC} of the ST7537 in order to reference the digital level of the ST7537.
- RESET (Pin 3) : This input is active low. To restart the microcontroller, the reset key has to be pressed (see Figure 32). A capacitor (2.2µF) will keep the input low for a minimum startup period, whereas a pull-up resistor (100kΩ) will keep it high for normal operation.

Figure 32 : Reset Command



- Display Output : Light emitting diodes are used to display data. The maximum current provided by each output pin is 0.8mA. Therefore the serial resistor R has a minimum value of 4.7kΩ (see Figure 33 : current = (4.2-0.6)/4.7e3 = 0.77mA).

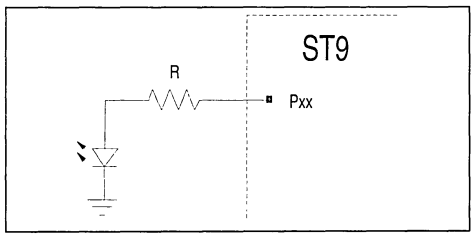
  The slave configuration uses 2 display output pins.

  Port 2 bit 3 (Pin 25) : blinking led
  Port 2 bit 5 (Pin 27) : load (slave led)

  The master configuration uses 4 display output pins.

  Port 2 bit 3 (Pin 25) : blinking led
  Port 2 bit 5 (Pin 27) : load 1 status
  Port 2 bit 6 (Pin 28) : load 2 status
  Port 5 bit 5 (Pin 38) : room status

Figure 33 : Display Output

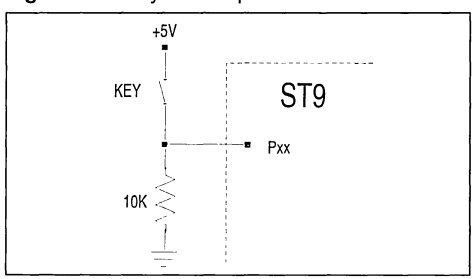


- Keyboard Input : Switch keys are used to enter commands. The keyboard pin is active high (see Figure 34). A pull-down resistor of 10kΩ keeps the input low, whereas a key press holds it high for active operation.

  The master configuration uses 3 keyboard input pins.

  Port 5 bit 2 (Pin 41) : load 1 command
  Port 5 bit 3 (Pin 40) : load 2 command
  Port 5 bit 4 (Pin 39) : room command

Figure 34 : Keyboard Input



VI.8.2 - Power Consumption

The power consumption of each configuration has been measured. Both master and slave boards were connected to the AC power mains : the slave led and all master status leds are switched ON by pressing the master room key (worst case simulation).

The current consumption is measured with a digitizing oscilloscope (channel 2) by means of a serial resistor, which value is small enough to avoid big supply voltage drops (about 1Ω typically).

A dual tracking power supply provides each board with the same power voltage, which value is displayed on a multimeter.

Test equipment : Fluke 45 Multimeter, Tektronix TDS460 Digitizing Oscilloscope
Test conditions : R = 1.04Ω , Valim = +10.006 V
T = +25°C

- Slave board : the oscilloscope is triggered on the falling edge of the Carrier Detect ($\overline{CD}$) signal displayed on channel 1 (see Figure 35). Therefore, the current consumption is displayed on channel 2 in receive mode on stand-by ($\overline{CD}$ = 1) and active ($\overline{CD}$ = 0) states.
  Current consumption (Rx mode) :+146mA$_{RMS}$
  Power consumption :
  (+10.006V - 1.04Ω · 146mA) · 146mA = +1.44W

  Slave board current consumption test results (see Figure 36)
  Channel 1 : Carrier Detect signal
  Channel 2 : Supply current

- Master board : the oscilloscope is triggered on the falling edge of the Rx/$\overline{Tx}$ signal on channel 1 (see Figure 37). The current consumption is displayed on channel 2 in both receive and transmit modes.

  Current consumption :
  Rx mode +160mA$_{RMS}$
  Tx mode +230mA$_{RMS}$

  Power consumption :
  Rx mode (+10.006V - 1.04Ω · 160mA) · 160mA = +1.57W
  Tx mode (+10.006V - 1.04Ω · 230mA) · 230mA = +2.25W

Master board current consumption test results (see Figure 38)
Channel 1 : Rx/$\overline{Tx}$ signal
Channel 2 : Supply current

Figure 35 : Slave Board Current Consumption Test

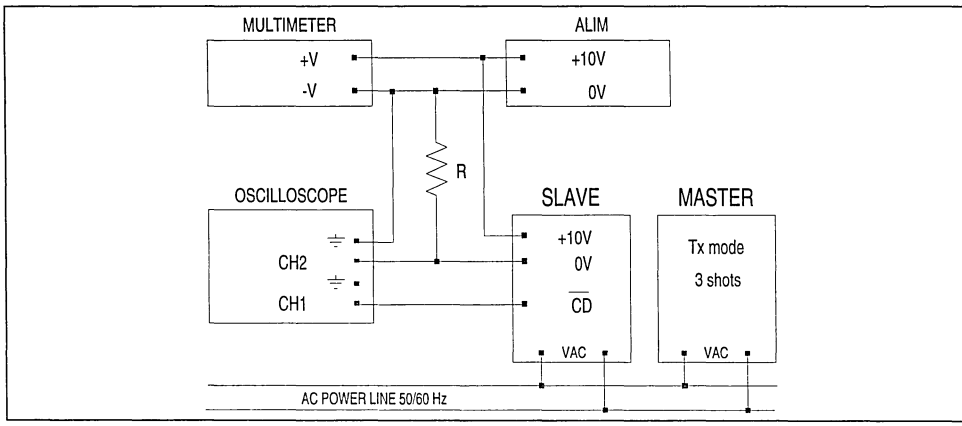


Figure 36 : Slave Board Current Consumption Test Results

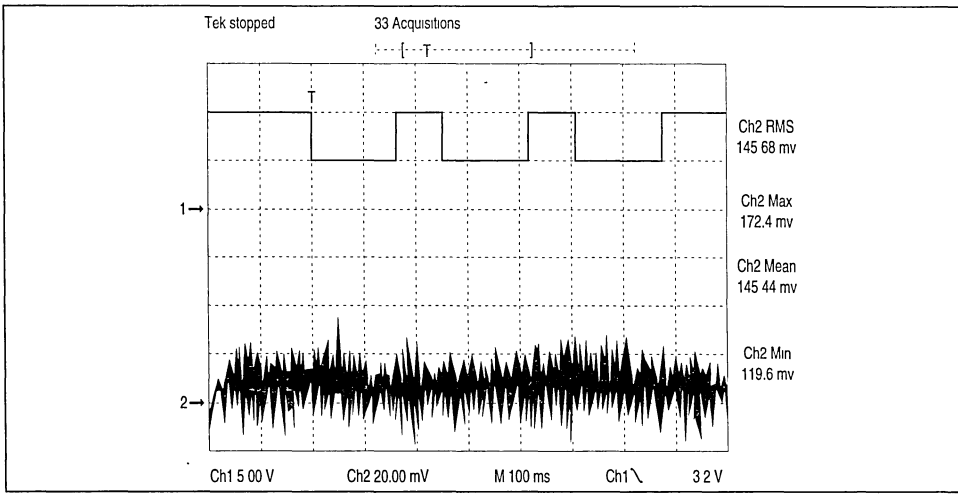


Figure 37 : Master Board Current Consumption Test

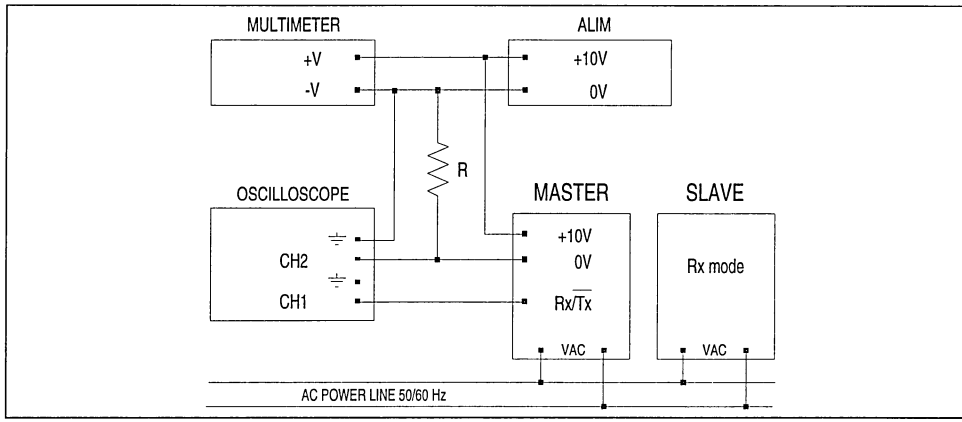
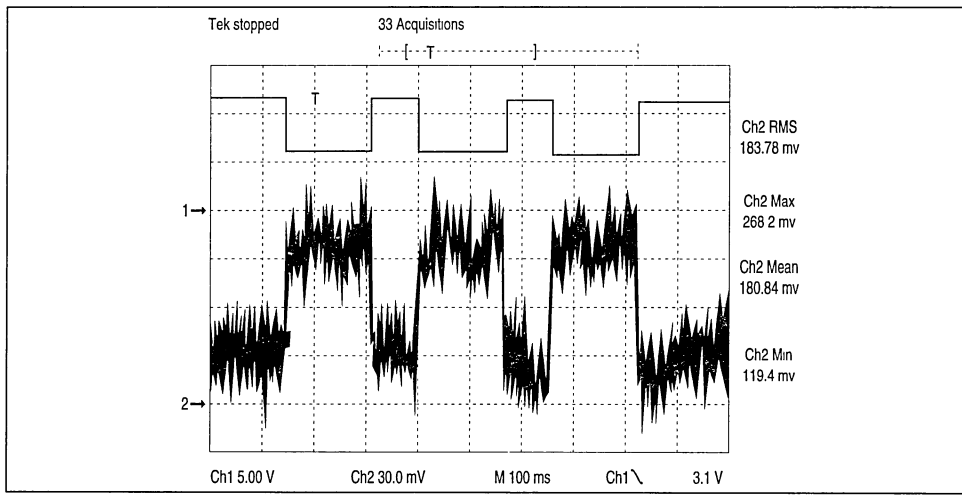


Figure 38 : Master Board Current Consumption Test Results



V.9 - Power Supply

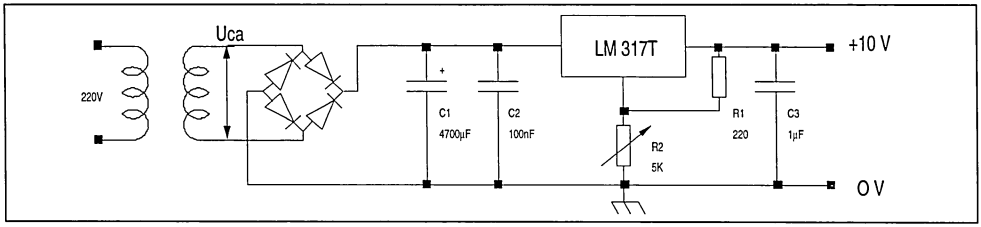
V.9.1 - Power supply features

The power supply features are :
- one reference voltage of 10 V_{DC}
- output current of 400 mA

The 5 V_{DC} voltage needed for the numeric part of the application is provided by a voltage regulator LM 7805, which already exists on the board.

The power supply schematic is given in Figure 39 : The LM317T regulator is ajustable between 1.2V and 37V thanks to the R1 & R2 resistors. It could be replaced by a +10V regulator.

Figure 39 : Power Supply Schematics



V.9.2 - Power supply sizing

The rectified voltage between pins of the capacitor C1 is shown in Figure 40 :

Uca = transformer secondary voltage (V_{RMS})
Ucc = voltage between pins of the capacitor C1
Urtt = ripple voltage
U = minimum voltage which has to exist between input and output of the voltage regulator
Us = output power supply voltage
Ud = rectifier diodes voltage drop
I = output power supply current

Hypothesis :
- I = 400mA
- Umin = 3V
- Ud = 1V

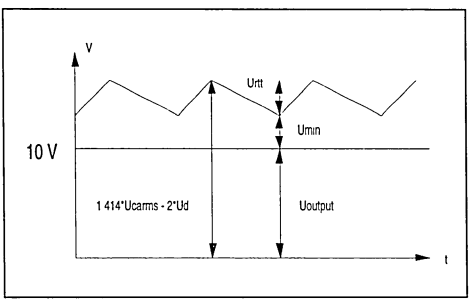
The minimum voltage the transformer has to provide is :

$$Uca = (Us + Umin + Urtt + 2Ud) / 2$$

The ripple voltage is :

$$Urtt = 10 * I / C1 \text{ (with I in mA and C1 in } \mu F)$$

Figure 40 : Rectified Voltage Parameters



V.9.3 - Using a 2x6 V secondary voltage transformer

The transformer must be able to supply I = 400mA, so that a 5 VA transformer is required.

The maximum value of Urtt is :

$$Urtt \text{ max} = 2*Uca - Us - Umin - 2*Ud = 2V$$

$\Rightarrow$ C1 min = 10*I / Urtt max
C1 min = 2000µF

We choose a C1 capacitor value of : 4700µF

The maximum voltage Vmax which can be applied between C1 pins has to be higher than the maximum secondary voltage of the transformer. Therefore, with a safety margin of 25% :

$$Vmax = (2 * Uca) * 1.25 = 21.2V$$

The maximum power dissipated by the voltage regulator is :

$$Pd = U * I$$

U = 2*Uca - Us - Urtt - 2*Ud
Urtt = (10 * 400) / 4700 = 0.85V
$\Rightarrow$Pd = 1.6W

In short, the power supply sizing is :
- secondary voltage of the transformer : 2x6V
- 5 VA transformer
- C1 = 4700µF with a maximum voltage of 25V between its pins.

VII - PC SOFTWARE

With the application board, we provide you a communication program written in Turbo C language which allows :
- to drive the RS232 interface
- to transmit data via power lines thanks to the ST7537
- to receive data from power lines thanks to the ST7537
- to process data
- to run character error test.

It is possible to transmit :
- characters
- text (maximum 80 characters)
- hexadecimal data (maximum 64 bytes)
- file.

The communication program allows you to run different types of communication :
- communication between 2 computers.
- communication between 2 ports COM on the same computer.

VIII - TYPICAL APPLICATION

VIII.1 - Protocol Design

The software described in the following parts provides you with a simple efficient protocol kernel, which is fully interrupt handled and uses almost no CPU time. Therefore it enables you to develop friendly interactive applications with a short response time.

This protocol uses a packet encapsulation mechanism with two level error detection capability, both for the packet level and for the byte level. During reception, burst noise can affect the communication channel, so that a frame check sum is used to detect excessive errors. In many cases, impulsive noise may cause unpredictable data loss without modifying the frame check sum. Therefore, each byte is transmitted and received in an asynchronous mode inside a 11-bit type word including a start bit, one stop bit, and an odd parity bit to ensure byte integrity.

VIII.1.1 - Frame Format (see Figure 41)

Each frame consists of a preamble, a header, a house address, a link control, a source address, a destination address, a data block, and a frame check sum.

The preambule is 8-bit field with a fixed value FFh: it trains the FSK demodulator, allows a good uart synchronisation for next character. The header consists of a 8-bit pattern AAh chosen with a low probability of wrongly detecting noise or preamble as the header. On a message reception, a matching test is run on the house address field to overcome perturbations coming from a neighbouring home network.

VIII.2 - Use of the ST90E28 resources

- The Watchdog/Timer :
  The watchdog mode is disabled and the timer is operated in continuous mode.
  On each timer interrupt request, network access parameters, keyboard delay time, common system clock parameters are updated. Besides, the ST7537 watchdog input is reset.
- The Serial Communication Interface (SCI) :
  The SCI is configured in asynchronous mode to exchange data between the power line modem and the microcontroller. Every character sent (or received) by the SCI has the following format: 1 start bit, 8 data bits, 1 parity bit (odd parity selected), 1 stop bit. The transmit rate is 1200 bauds.
  To start transmitting a frame, the transmitter buffer register is loaded with the preambule value FFh in order to run the SCI. Each data byte end of transmission results in the generation of an TXHEM (transmitter buffer empty) interrupt request to load the next transmit data byte.
  An outstanding character search is performed to detect the header of an incoming frame (see Figure 42). This is achieved by comparing each received data byte to the content of the data compare register. If the incoming character matches, an RXA (receiver address match) interrupt is requested to enable the analysis of the next data frame fields. Every time the reception of a data byte is completed, a RxD (receive data) interrupt request is generated to store the received data byte.

Figure 40 : Frame Fields

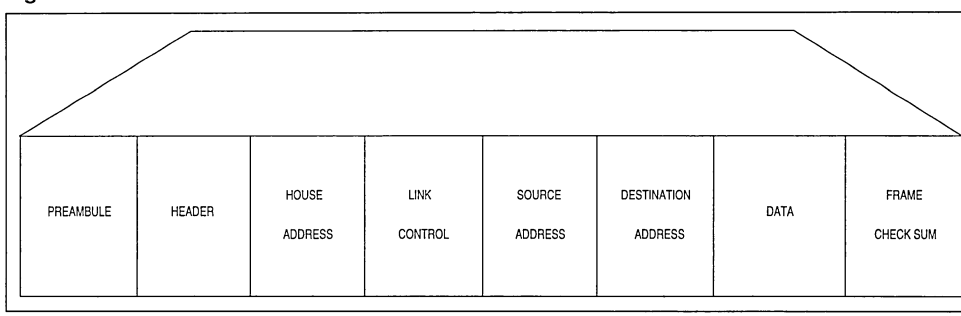
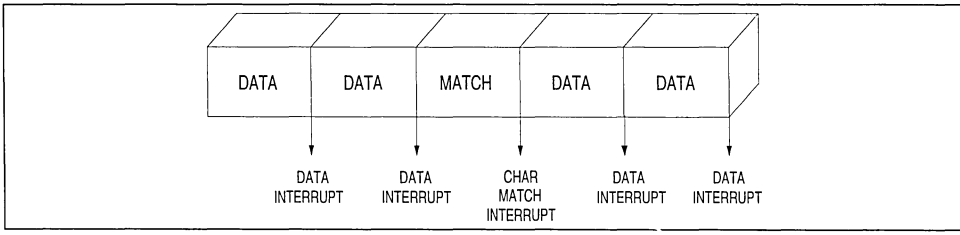
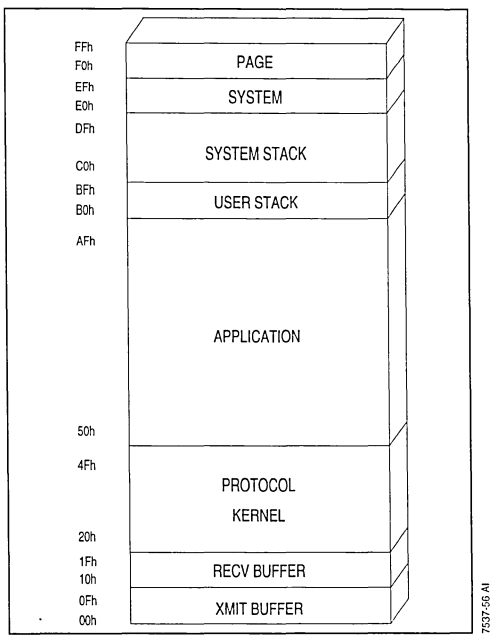


Figure 42 : Character Search Function



- The Register File (see Figure 43) :
  Among the 224 available global purpose registers, 16 registers are reserved as a transmit frame buffer, another group of 16 registers is reserved as a receive frame buffer, 48 registers are dedicated to the protocol kernel, and another group of 48 registers is allocated to the system & user stacks, which leaves 96 registers for storage of applicative values.
- The Input/Output Ports :
  Two of the port pins must be used for the Rx/$\overline{Tx}$ (P5.0) and $\overline{WD}$ (P5.1) output signals. Four must be initialized as alternate function for the RSTO (P2.0), $\overline{CD}$ (P2.4), RxD (P3.6) and TxD (P3.7) signals. Details concerning the initialization of these ports are given in next section.

Figure 43 : Register File Map



VIII.2.1 - Initialization of ST90E28 core and on-chip peripherals

- Core initialization : The user and system stacks are set up in the internal register file. The internal clock frequency is set to 11.0592MHz. The priority level of the main program is set to 7 (lowest), whereas the non-maskable interrupt (RSTO signal) has the top level priority.
- Initialization of the Input/Output ports : Only six input/outputs are required to exchange data between the ST7537 and the ST90E28. The corresponding pins are initialized as follows :

NMI	(Port 2 bit 0)	→ Alternate function, open drain, TTL
$\overline{CD}$	(Port 2 bit 4)	→ AF, OP, TTL
RxD	(Port 3 bit 6)	→ AF, OP, TTL
TxD	(Port 3 bit 7)	→ Alternate function, Push pull, TTL
Rx/$\overline{Tx}$	(Port 5 bit 0)	→ Output, Push pull, TTL
$\overline{WD}$	(Port 5 bit 1)	→ OUT, PP, TTL

  The NMI pin is programmed rising edge sensitive, whereas the CD/ input signal triggers an external interrupt request on a falling edge (INT1 pin) with a priority level set to 1.

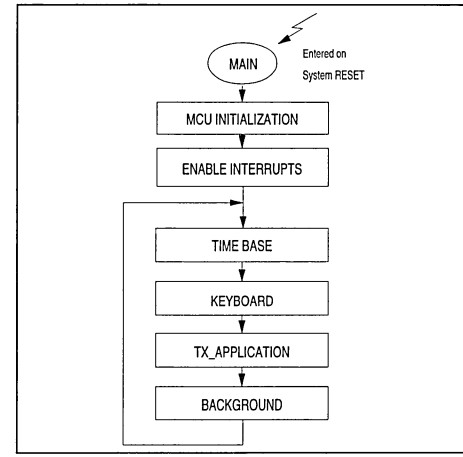
  As for the applicative features, each port pin is initialized as follows :
  display pin → Output, push pull, TTL
  keyboard pin → Input, tristate, TTL
- Timer : The watchdog mode is disabled. Continuous mode is selected with count down from a fixed value of 767, each underflow resulting in an interrupt request and reload of the fixed initial counter value. The internal clock rate, prescaler and initial count value are chosen to give an interrupt request every 555.56µs (1.8kHz = 36*50Hz = 30*60Hz). The timer counter is loaded with the value 767 to complete an end of count every 555.56µs. On each counter underflow an interrupt request (INT0) is generated with a priority level set to 0 (high).
- Serial Communication Interface : The asynchronous mode is selected. The serial interface programmed characteristics are : 8-bit word length,

odd parity generation and detection, 1 stop bit generation, AAh header search. In this mode, each data bit is sampled 16 times, so that each data bit period will be 16 SCI clock periods long. The counter of the baud rate generator is loaded with the fixed value 576 to set the SCI clock rate to 16*1200 = 19200 bauds. The priority level of all SCI interrupts (RXA, RxD, TXHEM) is set to 1.

VIII.2.2 - Main Program

The main is automatically entered on system reset, and first initializes the internal clock, stacks, ports, register file, serial communication interface, and timer. Then the timer starts counting down towards zero from an initial value of 767. Each time the counter clears to zero, an high priority interrupt request will be generated, which will initiate an update of the network access parameters.
The main program loops around the main modules.

Figure 44 : Main Program Flow Chart



ANNEXE A : DEMOBOARD OUTPUT IMPEDANCE

Figure 45

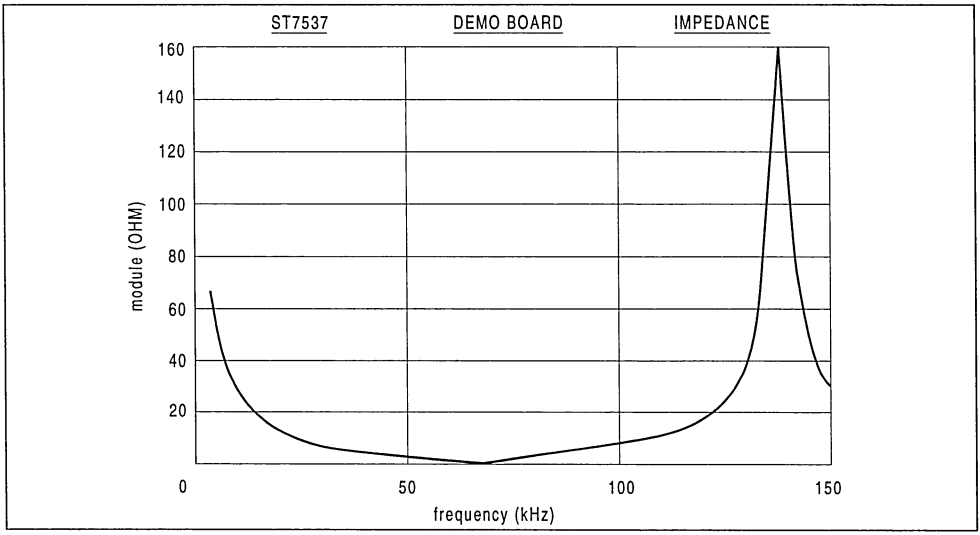
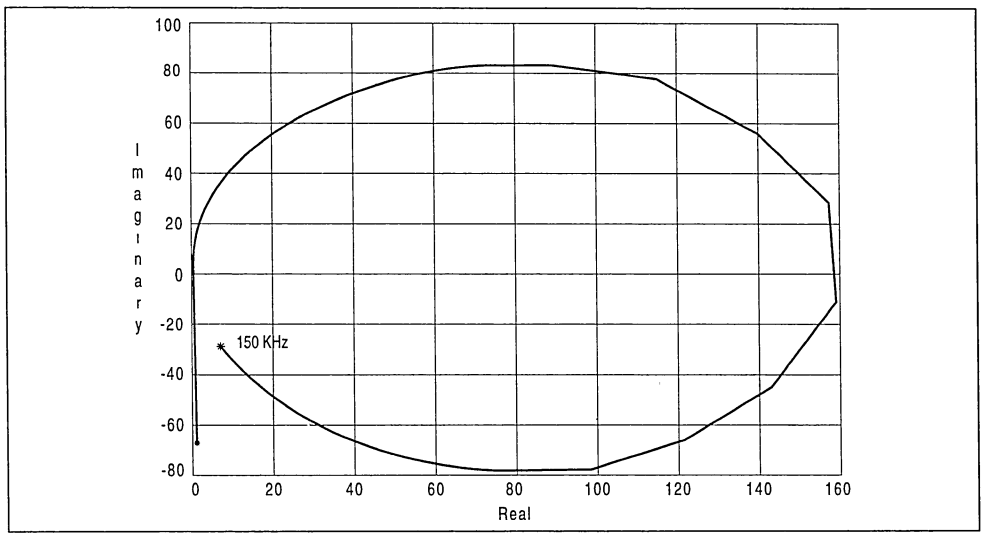


Figure 46



ANNEXE B : DEMOBOARD SCHEMATICS & LAY OUT

Figure 47 : Application Board 7537 DEMO1

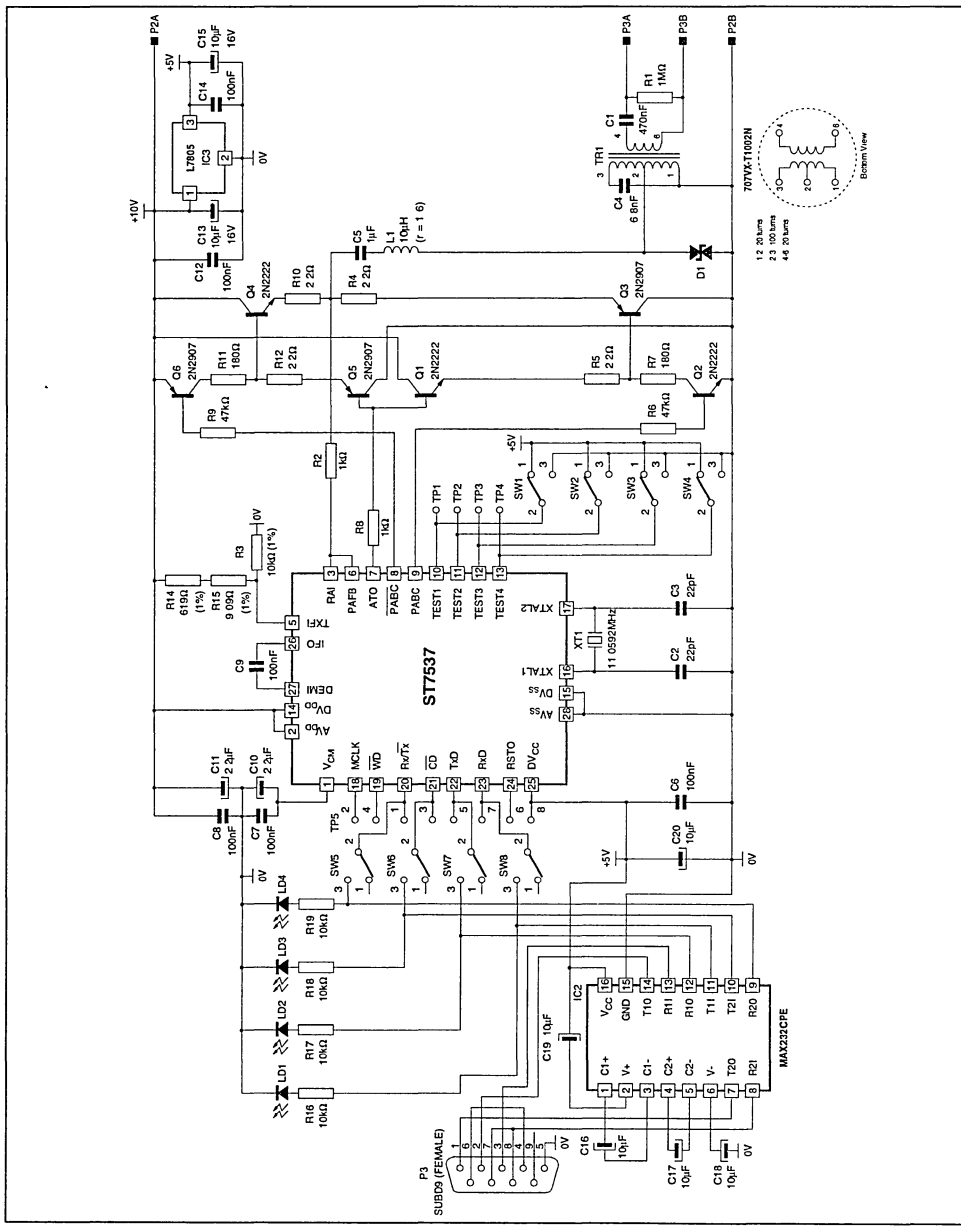
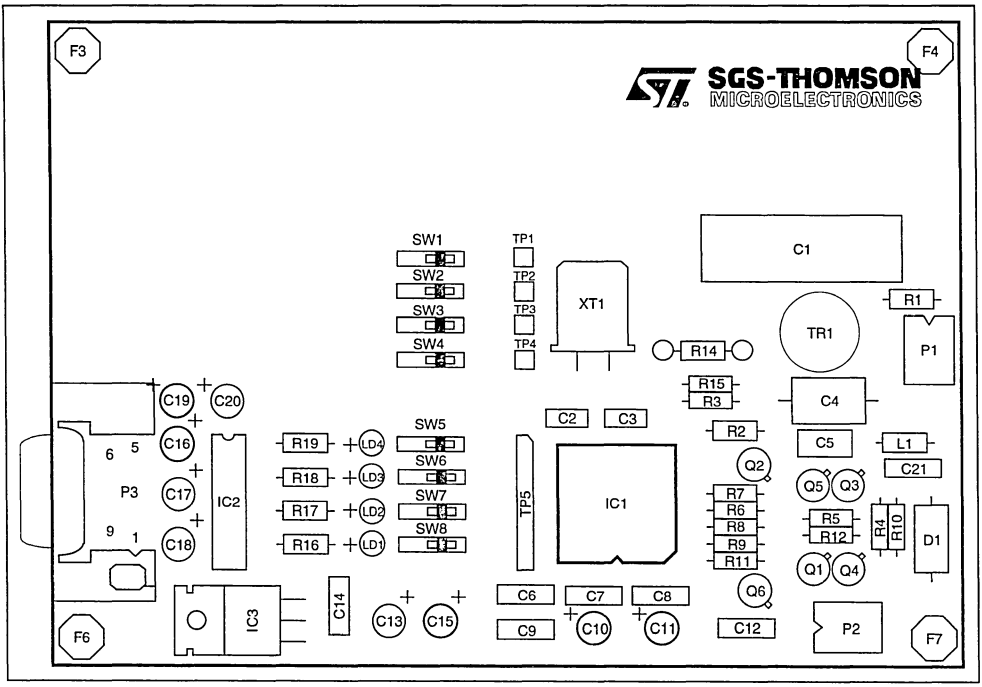


Figure 48 : Layout



Bill Of Materials

Item	Qty.	Reference	Part
1	2	C11,C10	2.2µF
2	6	C7,C6,C8,C9,C12,C14	100nF
3	4	LD4,LD1,LD2,LD3	LED
4	1	IC1	ST7537
5	8	SW8, SW1, SW2, SW3, SW4, SW5, SW6, SW7	
6	1	XT1	CRYSTAL
7	2	R8, R2	1kΩ
8	2	R6, R9	47kΩ
9	3	Q2, Q1, Q4	2N2222
10	3	Q3, Q5, Q6	2N2907
11	1	C4	6.8nF
12	1	C1	470nF
13	1	R1	1MΩ
14	4	R4, R5, R10, R12	2.2Ω
15	2	R11, R7	180Ω
16	1	IC2	MAX232CPE
17	1	IC3	LM7805

Item	Qty.	Reference	Part
18	1	R14	619 (1%)
19	4	R19, R16, R17, R18	10kΩ
20	5	C16, C17, C18, C19, C20	10µF
21	1	C21	15nF
22	2	PICO1, PICO2	PICO
23	2	C13, C15	10nF/16V
24	1	L1	10µH (r=0.8)
25	1	D1	DIODE
26	5	TP2, TP1, TP3, TP4, TP5	POINT
27	1	P3	SUBD9 (FEMALE)
28	1	P2	ALIM
29	1	P1	ALIM+
30	1	TR1	TOKO
31	1	R15	9.09kΩ (1%)
32	1	R3	10kΩ (1%)
33	2	C2, C3	22pF
34	1	C5	1µF

Figure 49 : Master Configuration Board

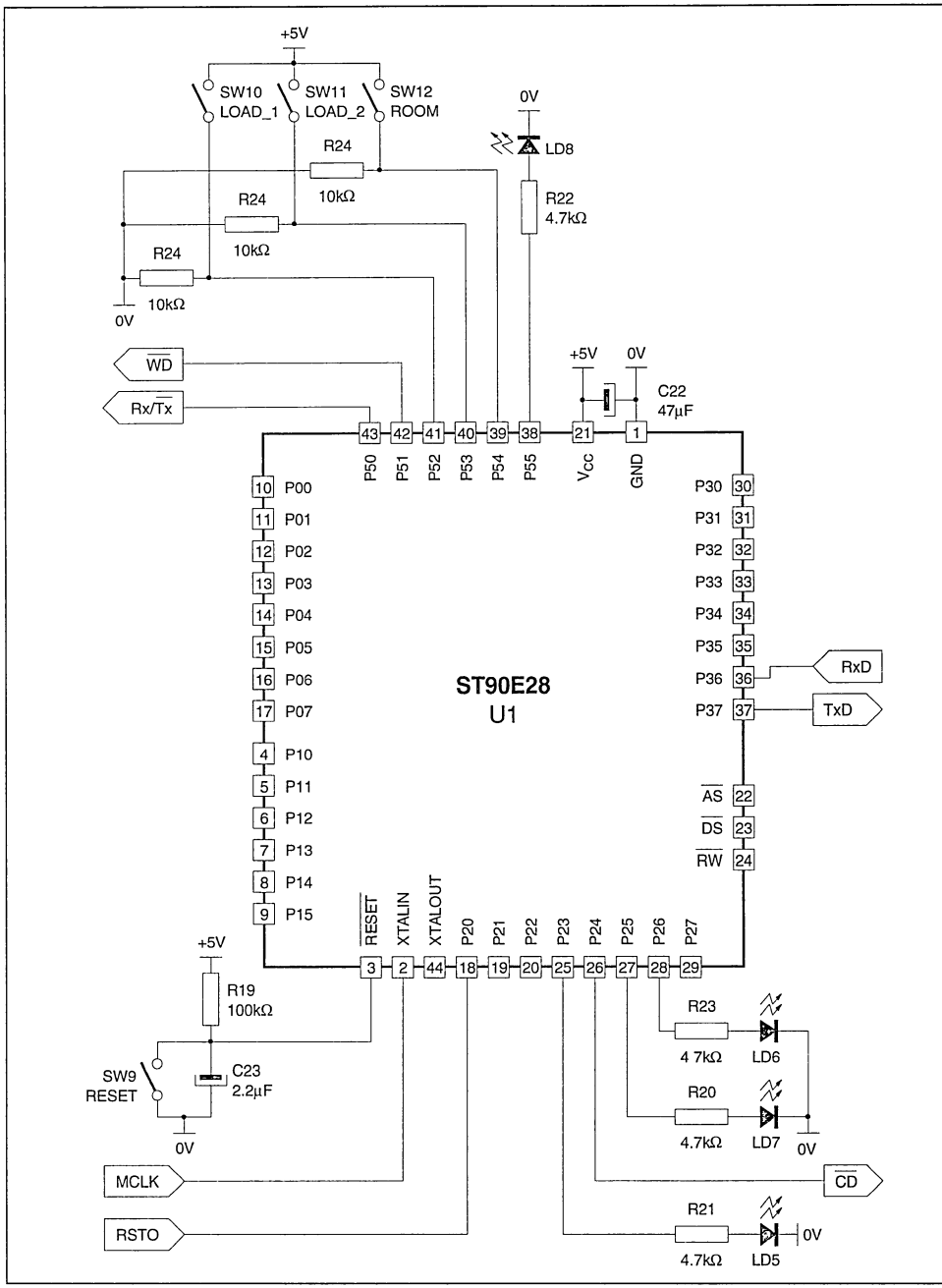
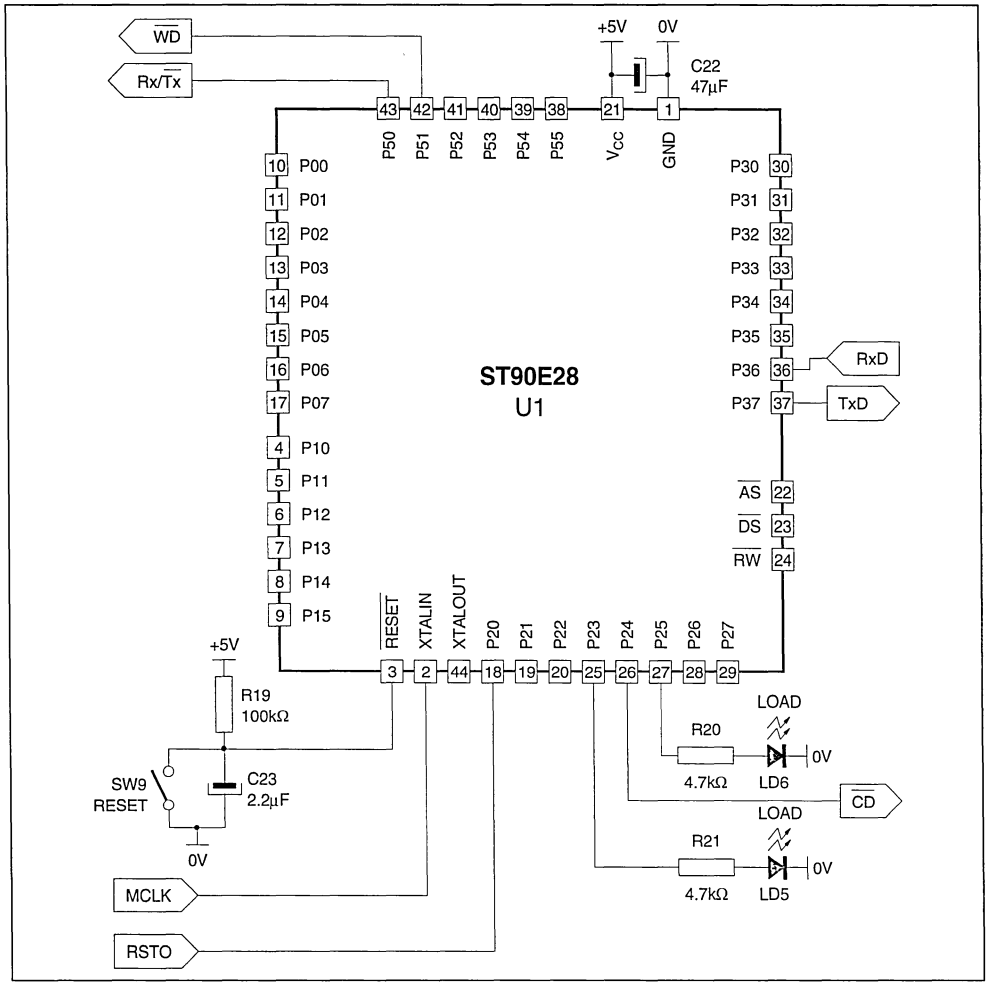


Figure 50 : Slave Configuration Board



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SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

POWER LINE MODEM APPLICATION REMOTE CONTROL USING ST7537 AND ST6

By Joël HULOUX, Patrice MOREL

SUMMARY

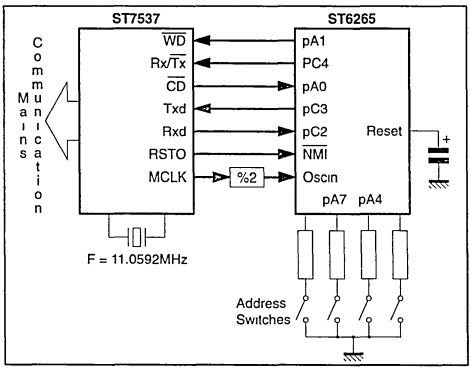
PRELIMINARY

All benefits and features of the ST7537CFN have been detailed in Application Note AN655. I suggest the reader to read this one before starting with this new application.

I- INTERFACE BETWEEN ST7537 AND ST626x

SGS-THOMSON is now introducing with this interface between the power line modem ST7537 and the low cost family ST6MCU a wide range of applications for home automation. This module allows communication between distant equipment by the mains and then remote control can be done in an easy way. This include applications like lighting dimmer, heater control, or phone remote system.

Figure 1 : Hardware Connection Between ST7537 and ST6265



I.1 - Interface

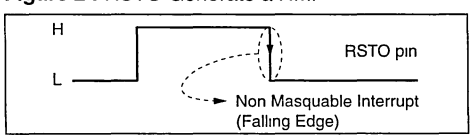
The choice of these ST6 pins is not the only one, but the software suggested is written for this interface.

I.2 - Pins Descriptions

I.2.1 - RSTO and NMI

The RSTO is the reset output of the ST7537. It set to high when the supply voltage is lower than a limit (typically 7.6V) or when no negative transition occurs on the watchdog input for more than 1.5s. Then, the RSTO is going back to low level. This falling edge is used to make an NMI on the ST6 chip. The NMI vector (number 0) must be the same as the reset vector in order to comply with Home System specifications.

Figure 2 : RSTO Generate a NMI



I.2.2 - Carrier Detect

The Carrier detect is driven low when the signal amplitude on the receive analog input is greater than a carrier detection level (typically 5mV). It has to be connected to an interrupt pin in order to start the receive program, even if the ST6 is doing something else. So the pin pA0 has to be programmed as an interrupt (with pull-up) to allow receiving.

I.2.3 - Rx/$\overline{Tx}$

The Rx/$\overline{Tx}$ pin is used to switch between receive and transmit mode. It has to be connected to an output port of the ST6, to allow the ST6 to switch between Rx and $\overline{Tx}$. pC4 has to be programmed as output port.

I.2.4 - Rxd and Txd

Digital datas are going over these pins. They have to be connected to pC2 and pC3 for the data transfer. Then, the programmer can use the PSI (Programmable Serial Interface) or work on the data values by programming pC3 as output and pC2 as input (without interrupt and with pull-up).

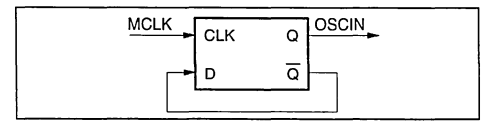
I.2.5 - Watchdog

This pin is connected to pA1, which must have a falling edge at least every 1.5s (MAX value). This feature has been included in ST7537 for security reason. So pA1 has to be set and reset at least every 1.5s (see RSTO pin description).

I.2.6 - Oscin

The maximum operating frequency of ST6265 microcontroller is 8MHz with a 5V DC supply (and 8.5MHz with 6V). In order to use the 11.0592MHz provided by the P.L.M., we must decrease this frequency. An easy way is to divide by 2 the master clock :

Figure 3 : The Flip-flop D-type Divide the Clock



A flip-flop D-type is used to divide MCLK by 2. So, the microcontroller has an input frequency of 5.5296MHz (quartz frequency divided by 2).

I.2.7 - Other ST6265 Pins

I.2.7.1 - RESET Pin

To provide a good initialisation, a 2.2µF capacitor is connected to the ST6265 reset pin. An internal 300kΩ is loading the capacitor during the power on. This provides a delay that allows power supply stabilisation. The high value of the resistor requires a tantalum capacitor type.

I.2.7.2 - pA4..pA7 Pins

These pins are used to enter an objet address (network configuration). pA4..pA7 are programmed in input with pull-up. Address number can be modified if necessary.

I.3 - Software Initialization

At reset state, all the ports are in input with pull-up, and interrupt register (IOR) is cleared, so the reset routine must configure the ports to comply with hardware connections.

Table 1 : Port Configuration

Register	Bits Values	Byte Value (e.g.)	Description
IOR	GEN (D4) set LES (D6) set	50 h	Enable all interrupts Level sensitive mode on interrupt #1 (port A)
DDRA	D0 res D1 set D4..D7 res	02 h	A0 in input A1 in output A4..A7 in input
ORA	DO set D1 set D4..D7 res	03 h	A0 interrupt with pull-up A1 in output push-pull set to 1 A4..A7 in input with pull-up
DRA	D0 res D1 set D4..D7 res	02h	
DDRB	D0..D7 set	FF h	B0..B7 in output
ORB	D0..D7 set	FF h	B0..B7 in push-pull output set to 1
DRB	D0..D7 set	FF h	
DDRC	D2 res D3 set C4 set	0C h	C2 in input C3 in output C4 in output
ORC	D2 res D3 set D4 set	0C h	C2 interrupt with pull-up C3 in output push-pull set to 1 C4 in output push-pull set to 1
DRC	D2 res D3 set D4 set	0C h	

The hexadecimal values are given only for example, these values will change due to the others pins programming (application software). In the program, every write to port A and port C must be done by writing a copy register, because these ports are in input and output, and this includes single bit operation (see ST6265 datasheet for further details).

I.4 - Timer 1 for 1200Bps

The MCU frequency is 5.5296MHz. With an internal clock divider set to 1, a prescaler set to 4 and a counter set to 96, the transmit and receive rate is 1200.08Bps (Figure 4).

The quartz is a 11.0592MHz with a accuracy of 100ppm. That means a final variation of 0.12Bps around 1200.08Bps.

When the timer 1 is not used for the baudrate this one is used for C.S.M.A. management (see II.3).

Table 2 : Baudrate Variation

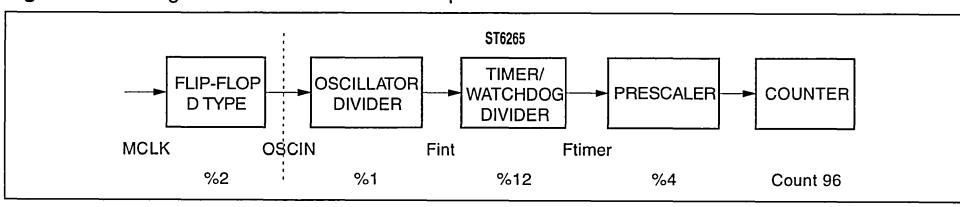
	Min.	Nom.	Max.	Unit
Rate	1,199.96	1,200.08	1,200.2	Bps

That means the following registers values :

Table 3 : Timer 1 and Oscillator Configuration

Register	Bit	Value
Oscillator control register OSCR	RS0 RS1	0 0
Timer status control register TSCR1	PS0 PS1 PS2	0 1 0
Timer counter register TCR1	D0 - D7	96 (decimal value)

Figure 4 : Dividing MCU Clock to Obtain 1200Bps



I.5 - Interrupt Routines

Interrupt vectors are mostly defined by the transmission program. NMI (vector #0) and the port A interrupt (vector #1) are used by the communication program. The port C (vector #2) does not need interrupt. The Timer 1 and ADC interrupt is used for communication timing (see CSMA recommendation).

AutoReload timer interrupt is also available.

Table 4 : Interrupt Programming

Vector #0	NMI	JP RESET
Vector #1	Port A and B	JP RECEIVE (or cascaded interrupt)
Vector #2	Port C and SPI	NOP and RETI
Vector #3	AR Timer	Available interrupt for application
Vector #4	ADC and Timer 1	Communication timing

I.5.1 - NMI Interrupt

The RSTO pin of the ST7537 is connected to the NMI pin of the ST6265 pin. The NMI interrupt provides the reset of the system.

I.5.2 - Receive Interrupt

This interrupt manages frame reception, that means :

- Power line modem pins control,
- Bit reception (synchronisation),
- Byte control,
- Frame control.

The interrupt program set bits in network/application register (NA-CTRL) then the main program is able to know the communication status by reading this register.

I.5.3 - Timer 1 Interrupt

This interrupt is enabled at the end of a frame reception or transmission to allow a delay between communication events (see C.S.M.A. specifications). It also leave time for application program.

II - TRANSMISSION METHOD

II.1 - Main Aspect of Communication

- Asynchronous 1200Bps,
- Transmit mode must be set for less than 1s (Cenelec specifications),
- Carrier detect is set between 4 and 6ms after the beginning of the Reception (the first 3 or 4 bits are lost) and is reseted in the same delay (an interference byte is received at the end of the frame). This delay corresponds to the demodulator trainning.

II.1.1 - Asynchronous 1200Bps

In order to transmit at 1200Bps, the transmit program needs a timer (TIMER 1) to send a bit every 1/1200s. In the receiving routine, the program is synchronised on every startbit, and use a timer (Timer 1) to read a bit every 1/1200s. This allows synchronisation on each byte, and the reception is aborted if carrier disappears between byte reception. During byte reception Txd is set to "0" in order to be independent of CD level (noise independant).

II.1.2 - Carrier Detect

The Figure 5 shows the timing diagram of a communication.

In order to allow a good transmission, the frame must contain a header that is more than 3 bits long and that contains no 0 (start bit) : FF h for example. An easy way to avoid the last bad bit is to know the frame length (fixed length for instance).

II.1.3 - Programs Specifications

In transmit mode, the Rx/$\overline{Tx}$ pin must be low, and set to high after the transmission of the frame. Transmission time must be shorter than 1s : that allows a maximum frame length of :

$$\frac{1200}{11} = 109 \text{ bytes (1 byte = 1 start bit + 8 data bits + 1 parity bit + 1 stopbit = 11 bits).}$$

Figure 5 : Flow Diagram of Digital Datas

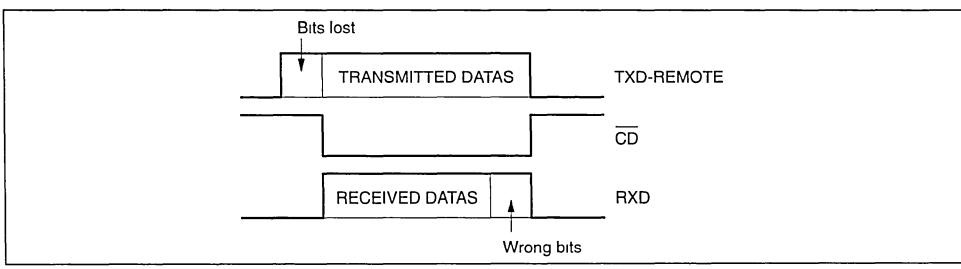


Figure 6 : Byte Format

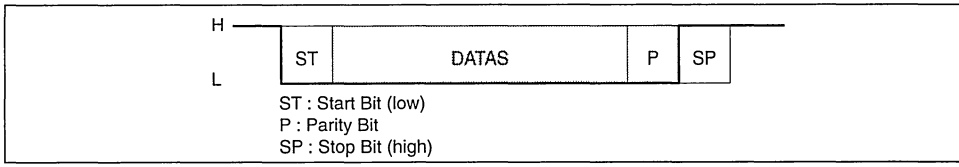
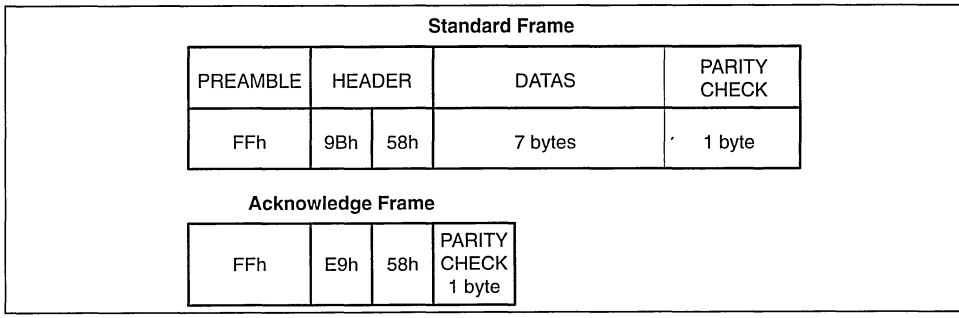


Figure 7 : Frames Format



II.2 - Packed message

The power line medium and the modulation employed require a special two level encapsulation mechanism :

- The byte level,
- The packet level.

The byte level control is a low level control, it only checks the start bit, the stop bit and the parity bit. The parity control can be done with byte shift and bit test (sla, jrr, jrs, ...) (Figure 6).

The packet level control is checking the received values. Preamble is used to synchronise and avoid loose of meaning datas. Header works out the frame type (Figure 7). For instance :

- 9B58h : Standard frame
- E958h : Acknowledge frame

The parity check byte is composed by all the parity bits of the data block of the frame (see parity register).

II.3 - C.S.M.A. Protocol Specifications

The protocol used is Carrier Sense Multiple Access Protocol. The telegram acknowledge is used to detect non-delivery. Before transmitting, the device must verify that there is no carrier on the network thanks to /CD, then send its message (standard frame) and wait for an acknowledge of the remote device (acknowledge frame). The device is able to check the transmission integrity by comparing the transmitted and the received parity check byte. The remote device is sending an acknowledge only if the packet is good (byte and packet control).

The C.S.M.A. protocol definition includes a timing for each stage of the communication. These values are given in the Table 5.

This is the theoretical definition of CSMA specifications. The programs proposed are using a register that is decreased in the main loop, providing a pseudo-random value (1 to 5). For the timing, the timer 1 counts for a delay (depending on the random register).

Table 5 : C.S.M.A. Specifications

Stage	Min. Time	Max. Time	Number of Values
Total duration of transmission		2s	
Duration of transmission after starting		1s	
Length to wait from the end of a remote transmission to initiate a transmission	85ms	115ms	7
Acknowledge sent after	0ms	30ms	Defined by software
Retry transmitting (after ack. time)	0ms	42ms	Uniformly distributed
Duration between two transmissions of the same device	125ms		

II.4 - Real Time and Communication

Time is one of the most important factor in this communication application :
- Mains is acting as a network (see C.S.M.A. specification),
- Home automation system requires a time delay below 0.5s.

So, communication time as to be taken into account. The table below gives values for message delivery (message + acknowledge) with the following values :
- Standard frame time : 100ms,
- Acknowledge frame time : 40ms,
- C.S.M.A. specifications.

In order to approximate to the reality, we have considered 1 error communication and/or a time waited to dispose of communication channel.

In Table 6, Tother is the time from the moment the object wants to transmit (but somebody is already transmitting) to the moment the communication channel is free.

A message needs about 155ms to be transmitted with acknowledge. In the worth case, even if 7 objects want to transmit in the same delay, all the messages will be delivered in less than 2s.

II.5 - Frame Definition

Here is the definition of frames implemented in ST6265 microcontroller.

II.5.1 - Standard Frame

Figure 8 : Standard Frame Format

PREAMBLE	HEADER	DATAS	PARITY CHECK

- Preamble : FFh
- Header : 9B58h
- Datas : Explained below
- Parity check : Parity bits of the data block

Figure 9 : Data Block Format

H.A. 2 bytes	C.B. 1 byte	S.A. 1 byte	D.A. 1 byte	ORDER 1 byte	DATA 1 byte

The Datas block is the real message. It contains the house address, to prevent from sending order to other houses objects. The source and destination addresses are used to define who's talking to who. The Control byte contains network facilities as priority, frame counter, ...
- H.A : (Home address) address of the house
- C.B : (Control byte) contain frame counter, priority, group command bit
- S.A. : (Source Address) address from the transmitter
- D.A. : (Destination Address) address of the receiver
- Order : Object of the message
- Data : Data byte eventually

II.5.2 - Acknowledge Frame

Figure 10 : Acknowledge Frame Format

PREAMBLE	HEADER	RECEIVED PARITY

- Header : E958h

The standard frame is 11 bytes long, that means 100ms at 1200Bps (with 11 bits by byte).

The acknowledge frame is 4 bytes long, that means 40ms at 1200Bps (with 11 bits by byte).

Table 6 : Message Delivery Time

Communication Time (ms)	No Communication Errors			One Communication Error		
	Min.	Mean	Max.	Min.	Mean	Max.
Don't wait before transmit	140	155	170	310	326	342
Wait before transmit	220 + Tother	252 + Tother	285 + Tother	390 + Tother	423.5 + Tother	457 + Tother

II.6 - Communication Registers Definition

II.6.1 - Communication Registers

Several registers are used by communication programs. they are listed below :

Table 7 : Communication Register Definition

Register Name	Register Description
outstart	Output buffer start address
in_start	Input buffer start address
out_par	Parity byte to be send
rand_r	Random register
b_count	Byte counter
reg_delay	Delay before allowing carrier detect
portacopy	Port A data copy
portccopy	Port C data copy
start_sav	Begining of interrupt stack (down stack)
na_ctrl	communication control register (see below)
r_pa_reg	Register for received parity calculation
t_pa_reg	Register for transmit parity calculation
retry	Register for transmission retry(before aborting)
r_mess_r	Received message register
t_mess_r	Transmit message register
reg_trans	buffer for a single value
r_ad_r	Instantaneous address (read on switch)
t_dat_r	Transmitted data register
r_dat_r	Received data register
t_r_adr	Transmitted remote address
t_adr	Transmitted address

These 21 registers have a name, but more than 17 bytes are needed for communication. In fact, communication program needs 43 registers (that include software stack and buffer for communication).

II.6.2 - Network /Application Register

Application program is not sequential because of the use of several interrupts. These interrupts are used for reception and communication timing. The main program is able to know what are the communication status by looking at the Network/Application register.

The network/application register is used in two ways :

- To interface the application program with the communication program. The application program is able to know if order has been received or if an acknowledge has been received,
- To enable protocol control inside network program. That means byte error, unexpected frame, time-out, bad frame parity, transmit-enable.

Table 8 : NA_CTRL Definition

D0	D1	D2	D3	D4	D5	D6	D7
Byte error	Unexpected frame	Bad frame parity	Time-out	Transmit enable	Too many errors	frame acknowledge	order received

II.6.3 - Parity Register

Parity registers are used to compare received and transmitted parity frame value (last byte of frame). The parity registers have the same look, that is given below :

Table 9 : Parity Registers Definition

D0	D1	D2	D3	D4	D5	D6	D7
0	Pdata	Porder	Pda	Psa	Pctrl	Pha2	Pha1

- Pdatas : Parity of data byte
- Porder : Parity of order byte
- Pda : Parity of destination address byte
- Psa : Parity of Source address byte
- Pctrl : Parity of control byte
- Pha1 : Parity of first home address byte
- Pha2 : Parity of second home address byte

II.7 - Mains Flow

The ST6 must be able to receive a frame whenever it comes, but it is really important to leave CPU time for Application program. That's why the main is a loop, where the application program is running. When a frame arrives, an IT occurs, the MCU receives the frame, modifies the communication status in Na_ctrl register and then go back to the main loop. If it is an order, the MCU send an acknowledge and does the order.

II.7.1 - Main Flow (see Figure 11)

When the board send a frame, it is waiting for an acknowledge, and tries 3 times if nothing is coming for a delay. If an acknowledge arrives, it is checked (parity check) and if a problem occurs, the MCU tries again (3 times maximum).The slave system main flow is the same as the master system, but of course, the application program changes.

Figure 11 : Main Program Organisation

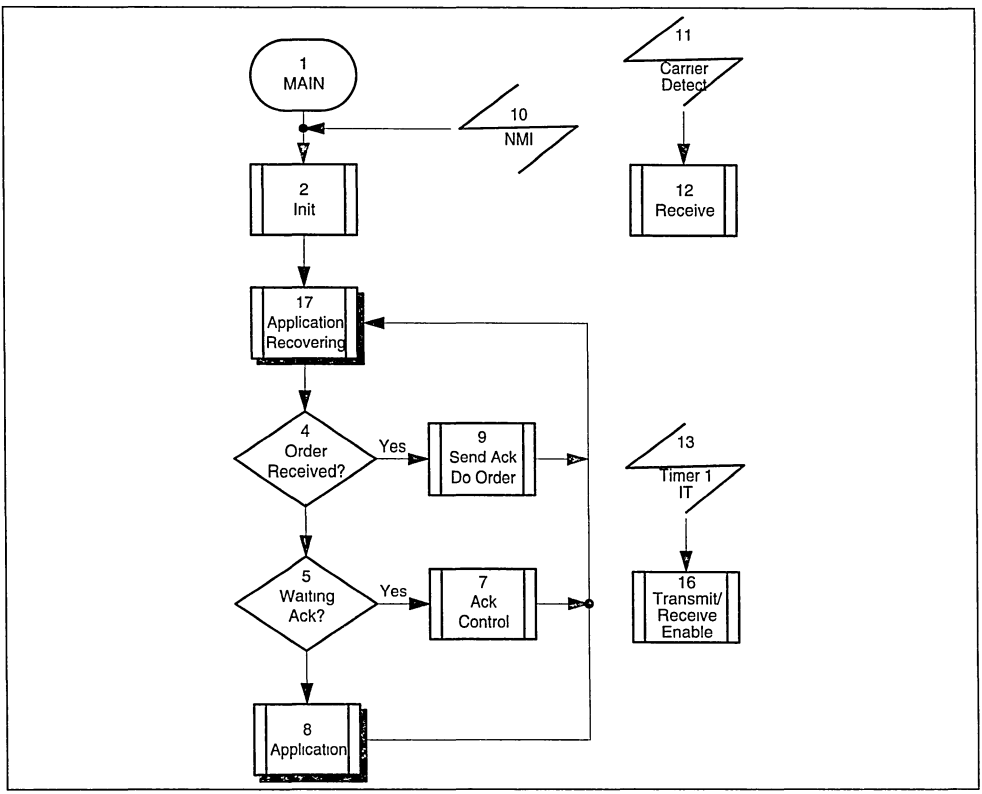
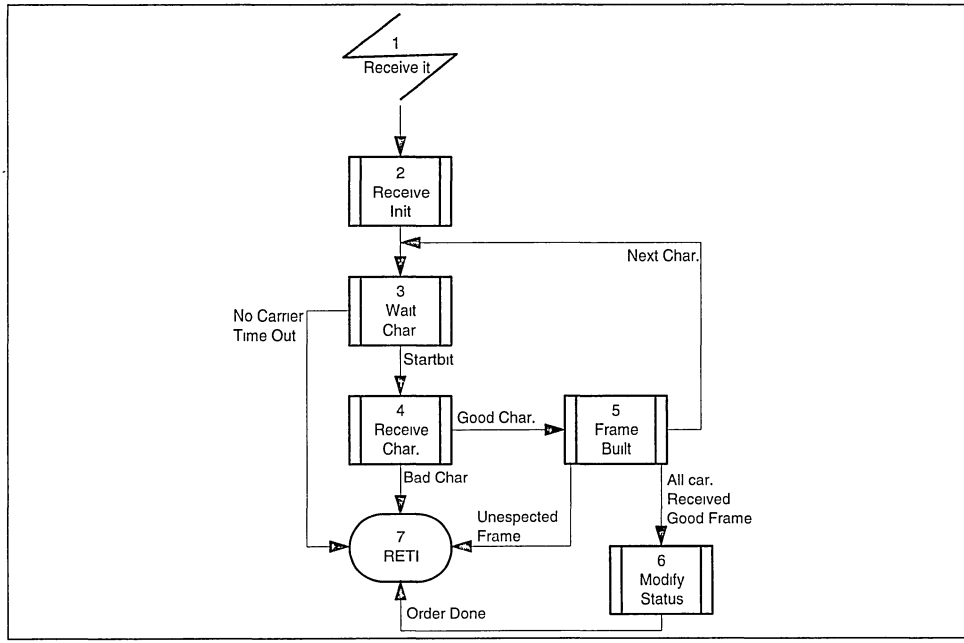


Figure 12 : Receive Routine



II.7.2 - Reception Flow

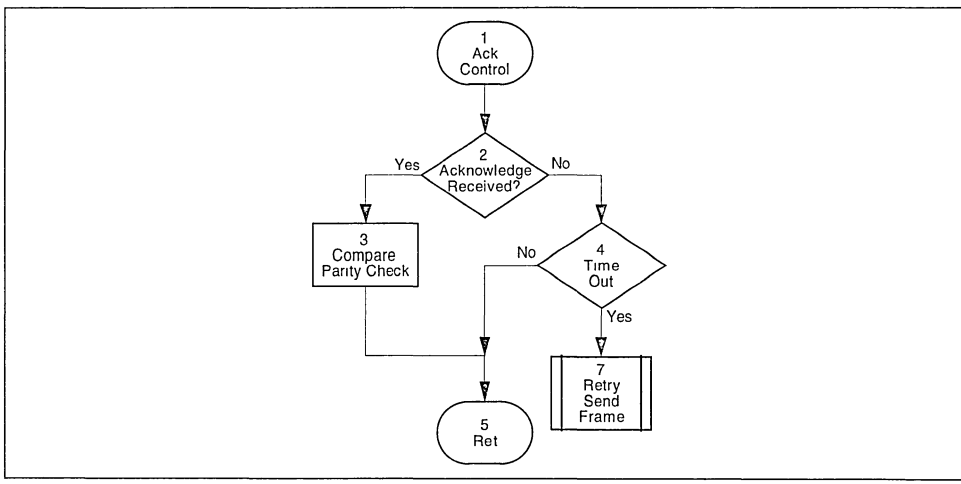
The synchronisation is done on each startbit : it's a byte synchronisation.

II.7.3 - Acknowledge Control Flow

The transmit part will not be detailed, it is just a pins and a timer control. The parity byte is calculated as the frame is sent, and it is sent after.

In order to leave MCU time for application, receive IT is disabled after each frame reception and for a delay of 30ms. This time is controlled by the Timer 1 and the reg_delay register.

Figure 13 : Ack Control Routine



III - APPLICATION : DIMMER CONTROL

III.1 - General Description (see Figure 14)

This section gives an example of an application that allows the dimming control of a remote light (or something else) by using the transmission with P.L.M. This application needs two boards :

- A master system, with a push-button (Dimming/off), 2 potentiometers and a 7 segments display,
- A slave system, with a 7 segments display and a plug for dimming control.

When the user presses the key (command), or turns a potentiometer, the master system sends a message, lights the decimal point on and waits an acknowledge. The remote board receives the message, sends an acknowledge and does the order. If no problem occurs, the master system receives the good acknowledge and switches the decimal point off. Otherwise, after trying sending the message 3 times, the decimal point remains lighting : a communication error occurs.

With the push-button, you can turn the light off or on. With the dimmer potentiometer, you can control the light intensity. With the display potentiometer, you change the number on the display. This feature has been added to prove that the ST6265 is able to receive and send order while it is dimming.

If you plug the master system in first, it will try to connect with the slave system three times, then it will light the error led (digital point of the 7 segments display). So you will have to plug the slave system and send an order (push the button and turn the display potentiometer) in order to return in normal mode.

The dimming control is done by the use of a triac (BTA08-600TW) so the load connected to the plug must not exceed 1000W.

III.2 - Schematics (see Figures 15 and 16)

This section gives the schematics of the two boards. pB7, pC0 and pA2 have different meaning on the master and on the slave board, that 's why we give two schematics. But it is possible to make a single board with dual implantation.

Warning : on this board the VDD is connected (via 0Ω resistor) to the neutral mains.

That means all the board is on the Mains supply voltage!

Figure 14 : Dimmer Control Application Description

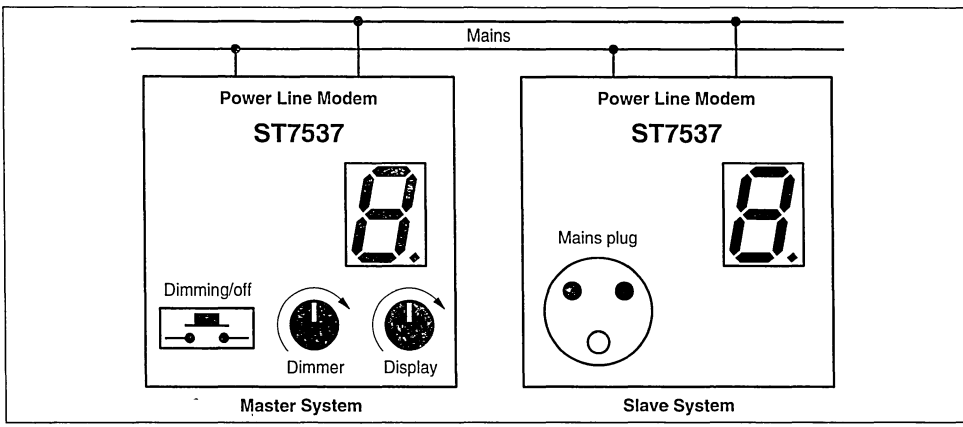


Figure 15 : Slave Board Schematic

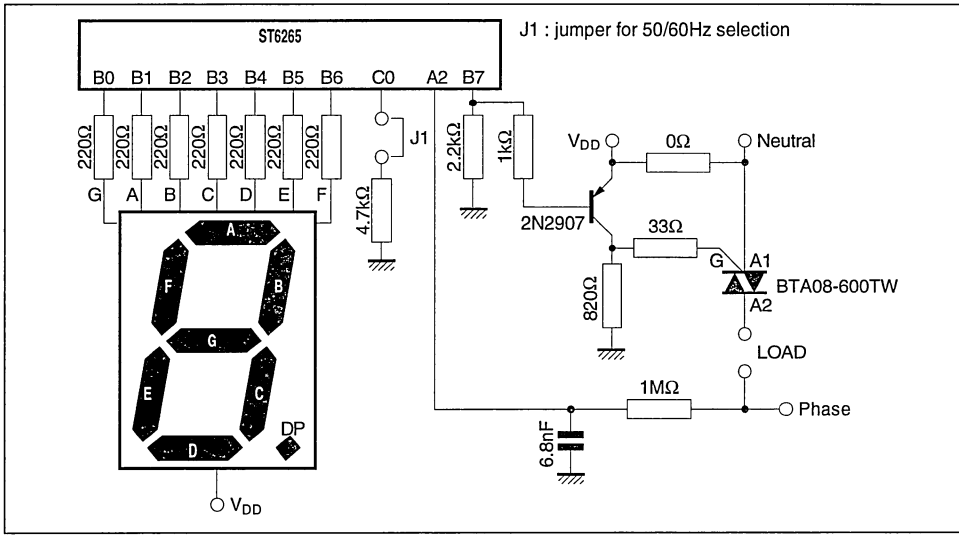
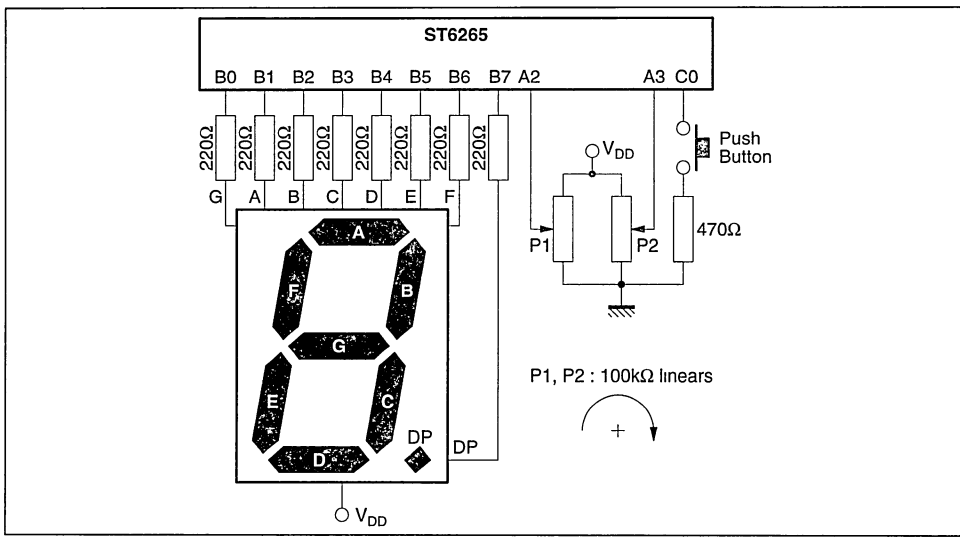


Figure 16 : Master Board Schematic



III.3 - Pins Description & Software Initialisation

III.3.1 - Slave Board

On this board, there is a 7 segments display application and a dimmer application.

The display application is very simple. The pins B0 to B6 have to be programmed in output with pull-up (push-pull). They are connected to the display by 220Ω resistors to limit the LED current. The display is a common anode so the pins have to be reseted to make the display lighting.

The dimmer application is most sophisticated, because it requires a zero crossing detection, and the possibility to wait a delay before firing the triac. See dimmer control part for more information.

The pin A2 is connected to the phase (via 1MΩ), in order to provide the zero crossing. This needs Neutral connected to V_{DD} to have a reference level. A2 has to be programmed in input.

The pin B7 has to be programmed in push-pull output to provide the pulse. B7 is the only pin that is connected to Auto Reload timer, so the fire signal needs to be amplified before driving the triac (the amplification stage is realised with a PNP transistor). At reset state B7 is configured in input with pull-up, so B7 is held at V_{SS} by a 2.2kΩ resistor.

This application is working with both 50Hz and 60Hz mains. The jumper connected to C0 is used to select between the two type of mains. Co has to be programmed in input with pull-up.

The pin configuration is the following :

Table 10 : Slave System Pins Configuration

Register	Bits Values	Byte Value (e.g.)	Description
DDRA	D2 res	00 h	A2 in input
ORA	D2 res	00 h	A2 in input
DRA	D2 set	04h	
DDRB	D0..D7 set	FF h	B0..B7 in output
ORB	D0..D7 set	FF h	B0..B7 in push-pull output set to 1
DRB	D0..D7 set	FF h	
DDRC	D0 res	00 h	C0 in input
ORC	D0 res	00 h	C0 with pull-up
DRC	D0 res	00 h	

III.3.2 - Master Board

On the master system, there are a display application and a control application :

- The display application the same as in slave system, but here, the decimal point is connected to B7. This decimal point is used as a warning light for communication acknowledgement. B0 to B7 have to be programmed in output push-pull,
- C0 is connected to a push-button, and has to be programmed in input with pull-up,
- A2 and A3 are input for analogic values coming from the potentiometers, so they have to be programmed in input, and reading an analogic value is done by programming one of these two pins in analog input, but not both in the same time.

Table 11 : Master System Pins Configuration

Register	Bits Values	Byte Value (e.g.)	Description
DDRA	D2 res D3 res	00 h	A2 in input A3 in input
ORA	D2 res/set D3 set/res	04 h /08 h	(A2 in input analog A3 in input) / (A3 in input analog A2 in input)
DRA	D2 set D3 set	0C h	
DDRB	D0..D7 set	FF h	B0..B7 in output
ORB	D0..D7 set	FF h	B0..B7 in push-pull output set to 1
DRB	D0..D7 set	FF h	
DDRC	D0 res	00 h	C0 in input
ORC	D0 res	00 h	C0 with pull-up
DRC	D0 res	00 h	

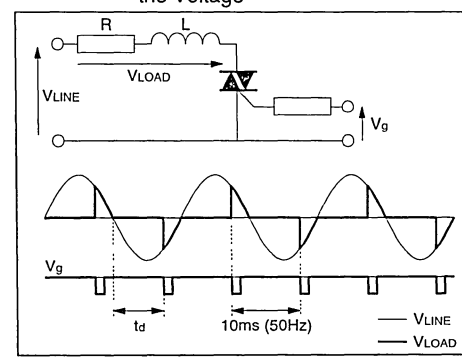
III.4 - Dimmer Control

III.4.1 - General Description

This section describes the main aspect of the power control system used on the slave system. For further details, refers to power control applications notes.

The output power is controlled by the phase delay of the triac drive. This delay is referred to the zero crossing of the line voltage. That needs an additional connection to main voltage, but in a remote application, this is not a problem.

Figure 17 : Power Control Based on the Monitoring of the Zero Crossing of the Voltage



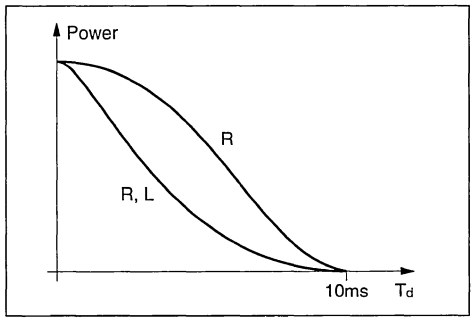
III.4.2 - Triac Specification

The triac used is a BTA08-600TW (SGS-Thomson) Logic Level triac. It has a maximum specified gate triggering current of 10mA (at 25°C). The current is provided by the amplifier stage (transistor), and the pulse width is programmed by software.

III.4.3 - Timing Specification

T_d determines the power used by the load. Between two pulses, there is a delay of 10ms, except during T_d variation.

Figure 18 : Load Power Consumption versus Time Delay



As shown in Figure 18, a small delay variation can affect the load power (that means light intensity in dimmer control), so this application is very sensitive to delay variations, and the timer has to be tuned very precisely. The timer is loaded with values stored in a table in ROM (one table for 50Hz, one for 60Hz).

III.5 - Application Software

III.5.1 - Display Application

The display routine is only checking the range of the transmitted data and setting the corresponding port B pins in order to display a digit. The display data is stored in the led_status register.

III.5.2 - Slave System

III.5.2.1 - AR Timer Configuration

The dimmer application is using the Auto Reload timer to provide the time delay (T_d). When a zero crossing voltage is detected on the mains voltage, the AR timer is launched with a delay (corresponding to T_d), And immediately after, the reload value is changed to a value corresponding to 10ms delay (50Hz). So, when an interrupt occurs (Receive mode for instance) the MCU is running in IT mode while the AR timer is providing the power control. The dimming intensity is controlled by the time delay, which has to be between Arr_min, and Arr_max.

The 10ms (or 8ms for 60Hz) delay is provided with the Arr_sd value. The Arcp value is loaded with Arrc + puls_siz ; this register defines the pulse width. All theses values are depending on the AR timer configuration :

- AR timer in autorelad mode with IT disabled : Armc = 20h
- AR prescaler set to 128 and clock division set to 3 : Arsc1 = 0E1h

Table 12 : AR Timer Configuration

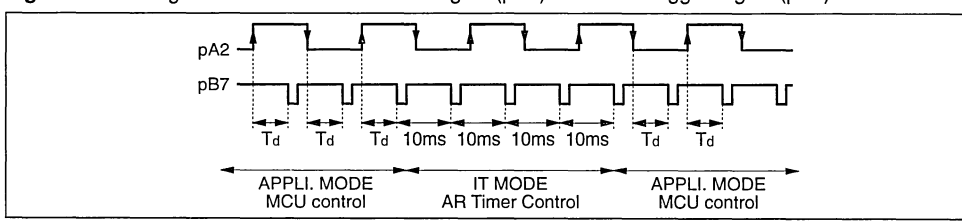
Register	50Hz Values	60Hz Values
Armc	20h	
Arsc1	0E1h	
Arrc during MCU control	Arr_min < Arrc < Arr_max	
Arrc during AR timer control	Arr_sd_10	Arr_sd_8
Arcp	Arrc + pulse_siz	

The values of Arr_min, Arr_max, Arr_sd are depending on the frequency of the MCU (Fint) and of the mains (50Hz or 60Hz). The delay waited between the zero crossing detection and the triac pulse is given by :

$T_d = T_{ar} \cdot (FFh - Arrc)$.

Where T_{ar} is the time for 1 count : T_{ar} = 6.98E-5s (at 5.5MHz).

Figure 19 : Timing Chart of Zero Cross Level Signal (pA2) and Triac Trigger Signal (pB7)



III.5.2.2 - Registers for Power Control

The application register is used to store the dimming status (on/off) and the zero crossing voltage.

Table 13 : Application Register Definition

D0	D1	D2	D3	D4	D5	D6	D7
lght_on	zero_dt	0	0	0	0	0	0

- lght_on : Set when dimming
- zero_dt : Set when pA0 is 0

Other bits are unused.

III.5.2.3 - Dimmer Flow

The dimmer procedure has to be launched very often because it provides dimmer synchronisation. If this procedure is not launched for more than 0.2ms, a test has to be performed in order to see if a zero crossing has appened during this delay. In this case, it is to late to synchronise on this zero crossing so the zero_dt bit of appli_reg has to be modified and the software will synchronise on the following zero crossing (Figure 20).

In the left flow : see Figure 20a

- Dimm_ctrl check if a new value has arrived for dimmer, calculate the new delay and eventually switch off or on the dimmer control,
- Aff_value checks if a new value has arrived for display, calculate the new digit and display it,
- get_level is a macro that get the level of the main voltage (1 for positive voltage and 0 for negative) and that modify the zero_dt bit of application register. This macro avoids delayed zero crossing detection.

In the right flow : see Figure 20b

- Zero crossing detection is done by comparing the instantaneous level (on pA2 pin) with the bit zero_dt in application register,
- AR timer control loads the arrc value corresponding to time delay, launch the timer, reload arrc value for a 10ms delay and arcp for the pulse width.

III.5.2.4 - Push-button

The detection of an action on the button is made simply by reading the value on pin C0. If somebody push on it the MCU sends a frame and waits for an acknowledge. This action needs more than 130ms so it makes a kind of debounce.

III.5.2.5 - Potentiometers

The main program reads the converted value on potentiometers, and compares it to the stored value (in dimm_val and in aff_val). If the difference between the read and stored value is higher than 8, the MCU send an order to remote system.

Figure 20 : Application Recover and Dimmer Procedure Flows

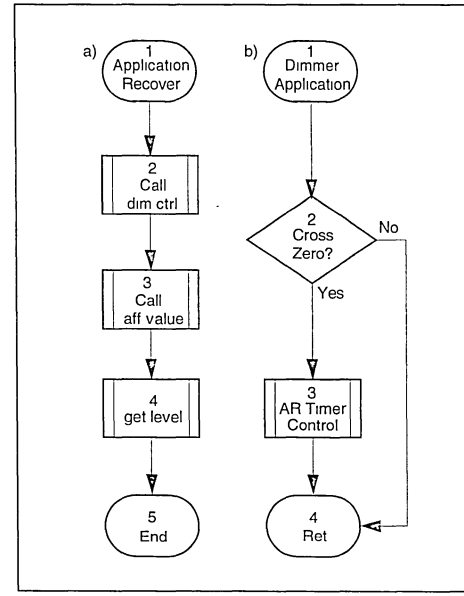
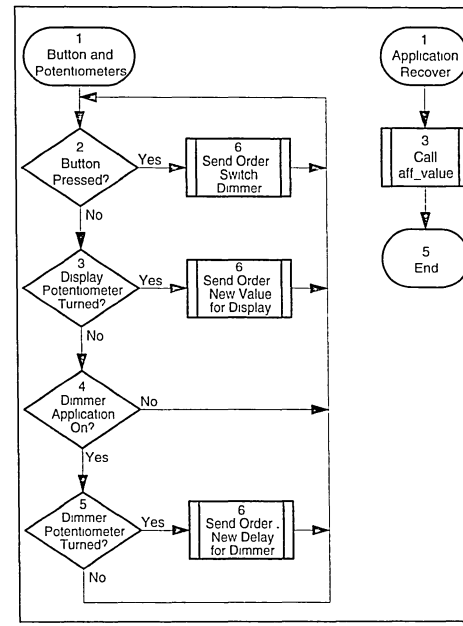


Figure 21 : Application Recover and Button and Potentiometer Control Procedure Flows



IV - NETWORK

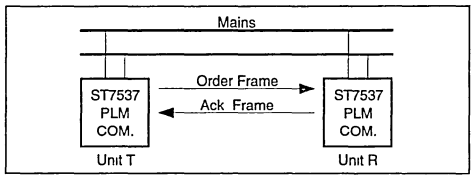
IV.1 NETWORK SPECIFICATION

Power Line communication uses mains distribution cables that constitute a network adapted to the control of devices already connected on it. The ST7537CFN power line modem complies with the regulation described in the CENELEC EN50.065-1 document, (so frequency, bit coding and other useful features are included in the chip). Nevertheless, the designer of an application has to take in account the power line communication specification when writing his protocol. For instance, access protocols are required for coexistence on the medium. The following paragraphs give a concrete case of communication on power line network. In first, only 2 devices are connected to the network. Then, others devices are connected, and we will be confronted to a real network specification.

IV.1.1 - Communication between 2 Units

This is the simplest case of communication. Only two devices are able to send and receive packet on the network. One unit sends an order, the other one is replying with an acknowledge.

Figure 22



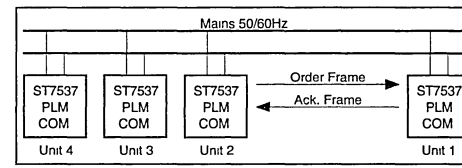
The unit T checks that the network is free for access thanks to the Carrier Detector, then it sends its frame and waits an acknowledge during a delay Twack. The unit R receive a frame and sends an acknowledge if R is the destination of the frame. R must send the ack. frame before the end of Twack.

If it is not the case, or if T has not received the acknowledge, T tries again to send the order. Of course the frame format must allows error detection by the receiver (order checksum) an by the transmitter (checksum in ack. frame). In most of the case, communication occurs without error, and the both units must keep silent for a delay Tsilent in order to leave time for application control. To allow the two units to transmit, the unit T has to wait more than R2, so R will be the first to take the channel if it needs to transmit.

If the two units send a frame exactly at the same time, they will not receive ack. frame, so they will retry after a delay (Twack). A random value is added to make one of the two unit faster than the other one. The total delay is Tretrans.

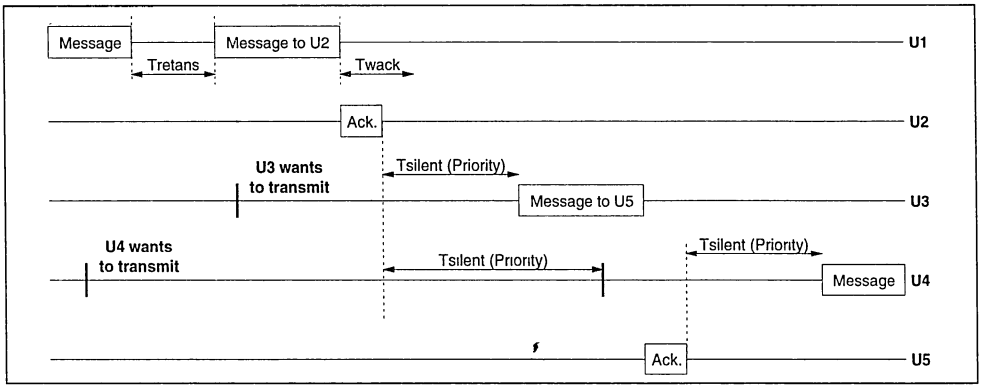
IV.1.2 - Communication with Several Units

Figure 23



With several units, the timing is the same, but even if a unit is not concerned with a communication, it has to get the frames in account for timing control. For instance, it has to reload its time to keep silent. And if several units have reload there time to keep silent at the end of a communication, the values reloaded must be different to avoid conflicts on the next communication. Again, a random value is added to make timing different.
Here is a data timing chart of the transmitted signal of the different units (see Figure 24).
Anyway, all units must send there message in less than two seconds.

Figure 24



IV.1.3 - Timing Control

All these timing are resumes in the following table.

Symbol	Description	Time	Comment
Tmax	Total duration of transmission	2s	
	Maximum duration of transmission after starting	1s	Feature included in ST7537CFN
TsilentR	Lenght to wait from the end of a remote transmission to initiate a transmission	85 .. 125ms	At least 7 values
Twack	Acknowledge sent after	0 .. 30ms	
Tretransmit	Retry transmitting	30 .. 72ms	
TsilentT	Duration between two transmissions of the same device	125ms	

In order to implement these timing, an easy way is to use a single timer and several registers corresponding to the different delays you want to count. The timer will decrease the registers at each overflow, and the counters are "launched" by loading a value in the corresponding register. An example of implementation on ST6265 is given in part III.
This access protocol allows an additional network priority: if you allow unit 1 (U1) to transmit before unit 2 (U2), then U1 will always sends its messages before U2, and will have a highest network priority. By choosing the range of TsilentR of a unit, you will then choose its priority.

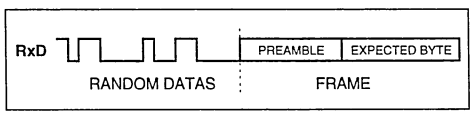
Values for TsilentR.

Range	Priority
85..94ms	Highest priority
95..104ms	Standard priority
105..115ms	Lowest priority

IV.2 - Example of Implementation of Soft Carrier Detector

We have seen that by programming the TxD to "0" in receive mode we increase the sensitivity of the ST7537 because there is no more clamping by CD. You will be able to have good communication with a receive signal of around 50dBµV which means a dynamic of around 70dB.
Because we want to get the benefit of the very good sensitivity of the ST7537, we will program Txd to "0" in receive mode and create by soft a frame detector . We will use the CD signal as mentioned by CENELEC only when we want to transmit a frame . Different software frame detector can be implemented depending of the resources of your microcontroller. You can program your microcontroller to go in receive frame when it received the expected byte.

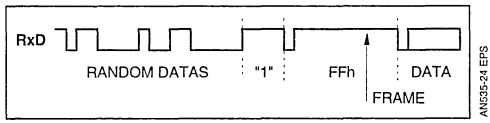
Figure 25



So the preamble is for demodulator training (when you start a communication the 3 first bits are lost by the receiver) and when you will match with expected byte the microcontroller will go in receive frame routine.

On the ST6 microcontroller we have implemented the following frame detector.

Figure 26



We put Txd =" 1" on the transmitter for around 4ms (for demodulator training) and

after we send in asynchronous mode FFh following by the complete frame. On the receiver , we check that we have RxD equal to "1" for at least 7ms (we are looking for FFh) , then we go in receive and we will have frame synchronisation on the first start bit of the data.

We did a trial in our lab with this system during 2 hours without having the ST6 going in frame receive routine on bad datas dued to noise signal.

IV.3 - Implementation of C.S.M.A on ST6265

The C.S.M.A. (Carrier Sense Multiple Access) needs a Timer for its implementation. But the ST6265 timer 1 is already used for bit time and software carrier detect. Furthermore, sometimes the timer has several functions at the same time, so the timer programming becomes very complicated.

In order to simplify this programming, we have implemented a single time delay corresponding to bit time (f = 1200Hz). So for each mode there is a counter corresponding to a delay. The counters are incremented (or decremented) in the timer interrupt routine while they are cleared (or affected with values) in main program.

For C.S.MA. specifications, we use two counters :

- Xmit_count
  This is the delay before retransmitting
- Rmit_count
  This is the delay before transmitting after a reception

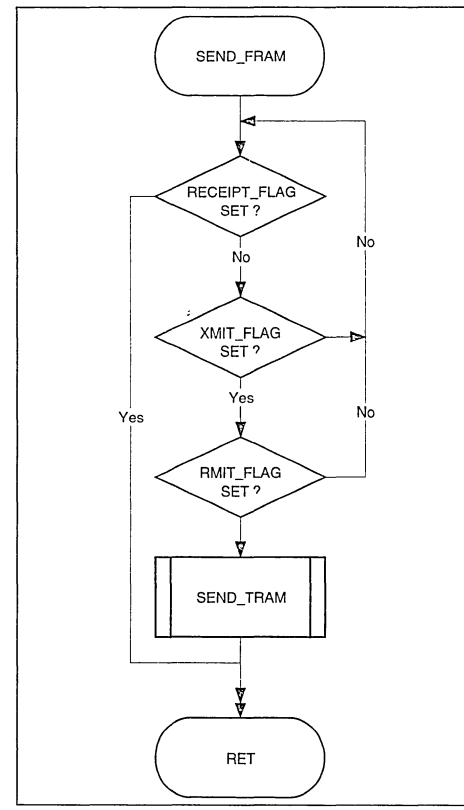
These counters are decremented in Timer 1 interrupt routine and flags are set when they become null. These flags are allowing the sending of a frame. Acknowledge frames are not concerned with these timing.

With this way of programming , the places where counters are loaded are very significant :

- Xmit_count is loaded at the end of the message sending procedure in order to wait an acknowledge (30ms) and at the end of the reception of a good acknowledge (time between two transmissions of the same device : 125ms).
- Rmit_count is loaded at the end of a reception with a random value (time between two transmission of different devices : 85 to 115ms).

The timer will allow the sending of a frame after C.S.M.A. delays.

Figure 27 : Sending a frame after C.S.M.A Delays



V - CONCLUSION

The ST7537 master and slave systems are demonstrative applications with low cost components. These boards are realised with discrete components but the size of these applications can be reduced by using a switching power supply and SMD (the ST7537 and the ST6265 are both available in small outline plastic). Several improvements should be done in order to make a more flexible product :

- Network management : All the addresses are fixed except the slave system address (switches). The software should be able to change the Home address, and objects addresses. This job needs management frame reception, emission and control,
- Byte transmission improvement : the software is reading the value on Rxd pin only one time (at the half of the bit), it would be better to do it several time to avoid spike perturbations,
- Frame transmission : the transmission is asynchronous with odd parity and there is a frame parity byte at the end of the frame, but if errors are detected, they are not corrected. A correcting code should be implemented in less than 200 bytes on ST6x,
- Power control : the 50Hz/60Hz detection should be done automatically instead of using a jumper. And the number of stages in dimming mode should be increased to obtain a pseudo-continuous variation.

All these modifications are realisable, because the program is less than 800 bytes long and the MCU is working at 5.5MHz, so there is place and CPU time left. The software is divided in module, so parts can be removed, and mains programs source (master.asm and slave.Asm) are less than 300 lines long.

VI - ANNEXE A : ST6x PROGRAMS

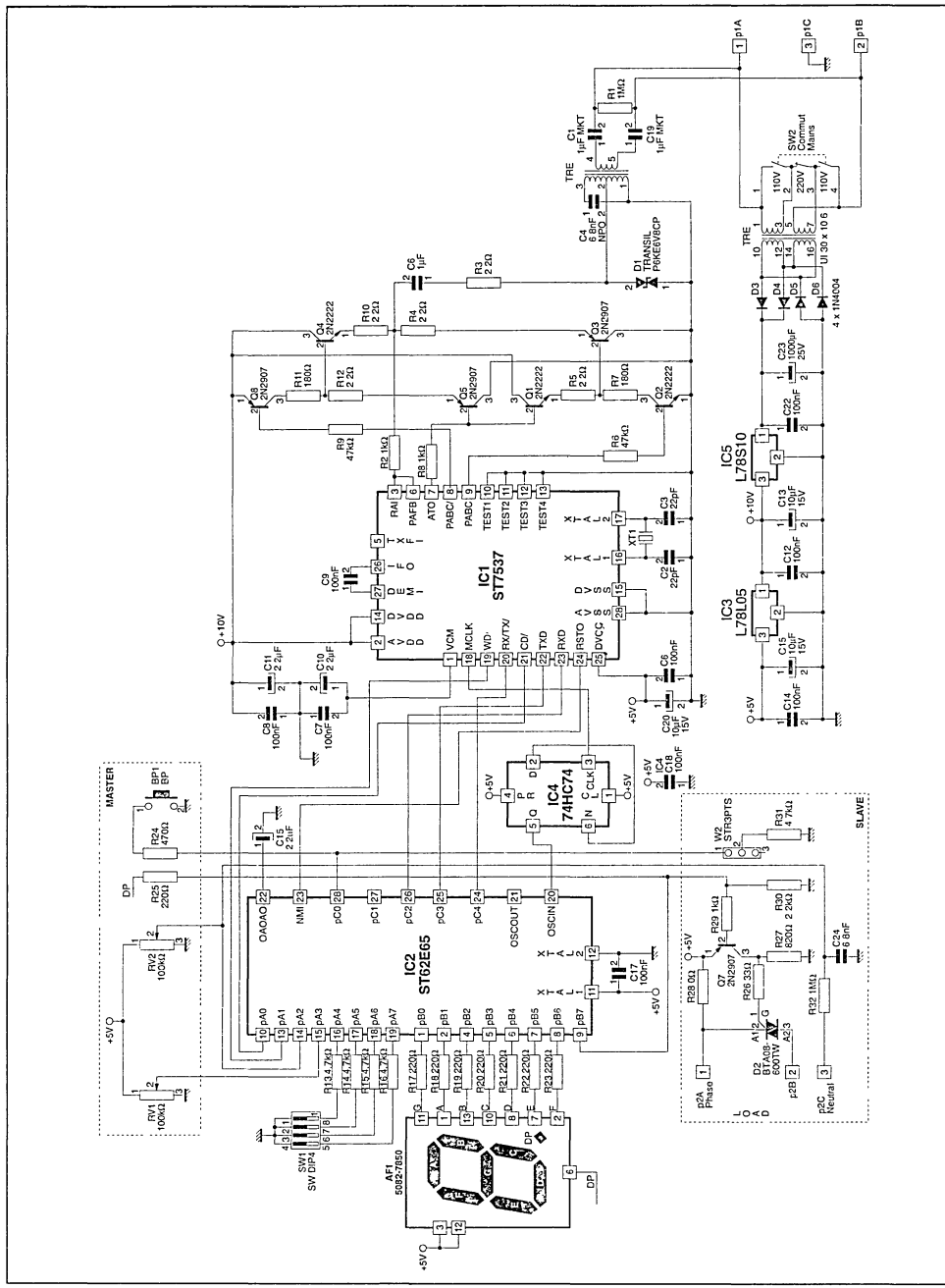
The program is divided in several modules, so it is easy to take parts of it and it is more readable. The master system and the slave system have common parts, but the mains programs are not the same.

Table 14 : Modules Used in Master and Slave Boards

Name	Function	System
6215_reg.asm	Common 62xx core registers	Master/Slave
ST6_7537 asm	Byte communication with ST7537	Master/Slave
Def_fram.asm	Frame control	Master/Slave
Address.asm	Address switches management	Master/Slave
Display.asm	7 segment display management	Master/Slave
Pot_et_b.asm	Potentiometers and push-button management	Master
Powerctl.asm	Power control	Slave
Master.asm	Main master program	Master
Dimmer.asm	Main slave program	Slave

The master and slave programs are compiled without linker, but when using the powerctl.asm module the option :
block 64% S64
is included in order to provide a good window banking for the tables in rom (AR values for dimmer application). That makes the object code bigger than it is but it is the price to pay.

VII - ANNEXE B : SCHEMATICS



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

PHONE REMOTE SYSTEM

By Joël HULOUX, Patrice MOREL

CONTENTS — Document page

I - INTRODUCTION

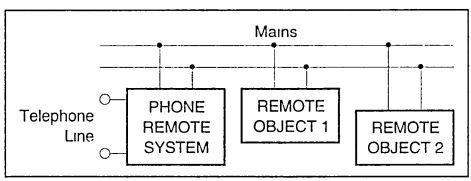
I.1 - General Purpose

In the Application Note AN535, we described how to implement the basis of a power line network using the dedicated modem chip ST7537CFN. This network has been validated with ST7537 MASTER & SLAVE systems, and shows the feasibility of power line control. But Home automation systems allow more than switching a light, or changing the value of a digit. The possibilities of the network increase each time we connect a new device on it. For instance, adding a phone remote system will allow the remote (from anywhere on the planet) control of devices connected on the network only by calling your house. The phone remote system is now demonstrating this fact : a telephone interface that allows the householder to give instructions to appliances from outside.

I.2 - Description

The phone remote system is a device connected to both telephone line and power line network. It is able to detect the phone ring, to hang up the line, and "converse" with the householder. This dialogue is done by using the DTMF (digital tone multi-frequency) generated by the remote phone. To answer back, the phone remote system is beeping. Of course, this is a low cost choice and the system can be improved by using a voice synthesiser with on line help and so on...

Figure 1 : Phone Remote System Connected to the Power Line Network



In a classical electric installation, this device would have used one control cable for each controlled object. With power line control, you just have to plug it and the link is done with all devices controlled by mains network.

I.3 - Improvements

The part II describes several improvements done to the communication program explained in AN535.These modifications allow new features :

- software carrier detect,
- C.S.M.A. timings (Carrier Sense Multiple Access),

and the use of communication modules in phone remote program.

II - POWER LINE COMMUNICATION USING ST7537CFN

The ST7537 CFN power line modem complies with the regulation described in the CENELEC EN50.065-.1 document, (so frequency, bit coding and other useful features are included in the chip). Nevertheless, the designer of an application has to take in account the power line communication specification when writing his protocol. For instance, access protocols are required for coexistence on the medium.

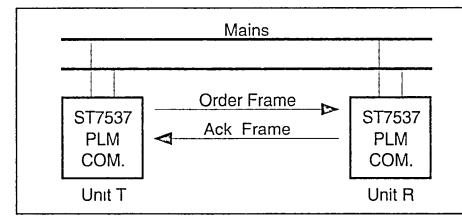
II.1 - C.S.M.A. Timings

The following paragraphs give a concrete case of communication on power line network. In first, only 2 devices are connected to the network. Then, others devices are connected, and we will be confronted to a real network specification.

Communication between 2 units

This is the simplest case of communication. Only two devices are able to send and receive packet on the network. One unit sends an order, the other one is replying with an acknowledge (see Figure 2).

Figure 2 : Two Units on the Mains



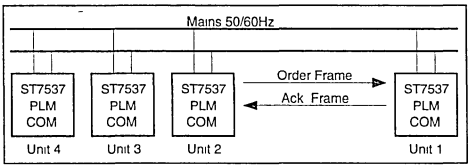
The unit T checks that the network is free for access thanks to the Carrier Detector, then it sends its frame and waits an acknowledge during a delay Twack. The unit R receive a frame and sends an acknowledge if R is the destination of the frame. R must send the ack. frame before the end of Twack. If it is not the case, or if T has not received the acknowledge, T tries again to send the order. Of course the frame format must allows error detection by the receiver (order checksum) an by the transmitter (checksum in ack. frame). In most of the case, communication occurs without error, and the both units must keep silent for a delay Tsilent in order to leave time for application control. To allow the two units to transmit, the unit T has to wait more than R, so R will be the first to take the channel if it needs to transmit.

If the two units send a frame exactly at the same time, they will not receive ack. frame, so they will retry after a delay (Twack). A random value is added

to make one of the two unit faster than the other one. The total delay is Tretrans.

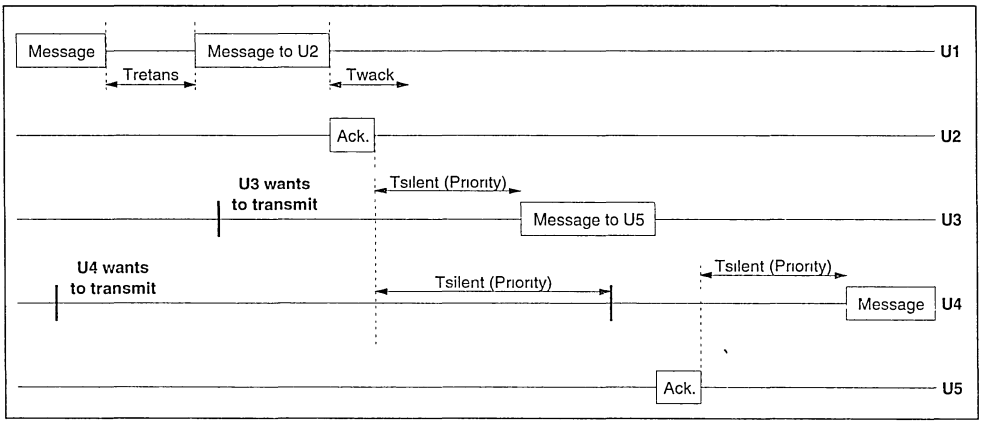
Communication with several units

Figure 3 : Several Units on the Mains



With several units, the timing is the same, but even if a unit is not concerned with a communication, it has to get the frames in account for timing control. For instance, it has to reload its time to keep silent. And if several units have reload there time to keep silent at the end of a communication, the values reloaded must be different to avoid conflicts on the next communication. Again, a random value is added to make timing different. Here is a data timing chart of the transmitted signal of the different units (see Figure 4). Anyway, all units must send there message in less than two seconds.

Figure 4 : Power Line Communication Data Timing



Timing control

All these timing are resumed in the Table 1.

Table 1 : C.S.M.A. Timing

Symbol	Description	Time	Comment
Tmax	Total duration of transmission	2s	
	Maximum duration of transmission after Starting	1s	Feature included in ST7537CFN
TsilentR	Length to wait from the end of a remote transmission to initiate a transmission	85 .. 125ms	Al least 7 values
Twack	Acknowledge sent after	0 .. 30ms	
Tretransmit	Retry transmitting	30 .. 72ms	
TsilentT	Duration between two transmissions of the same device	125ms	

In order to implement these timing, an easy way is to use a single timer and several registers corresponding to the different delays you want to count. The timer will decrease the registers at each overflow, and the counters are "launched" by loading a value in the corresponding register.

This access protocol allows an additional network priority: if you allow unit 1 (U1) to transmit before unit 2 (U2), then U1 will always sends its messages before U2, and so will have a highest network priority. By choosing the range of TsilentR of a unit, you will then choose its priority.

Table 2 : Priority According to TsilentR

Range	Priority
85 .. 94ms	Highest priority
95 .. 104ms	Standard priority
105 .. 115ms	Lowest priority

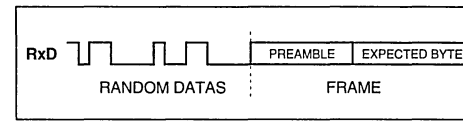
II.2 - Soft Carrier Detector

We have seen that by programming the TxD to "0" in receive mode we increase the sensitivity of the ST7537 because there is no more clamping by CD.

You will be able to have good communication with a receive signal of around 50dBµV which means a dynamic of around 70dB.

Because we want to get the benefit of the very good sensitivity of the ST7537 , we will program Txd to "0" in receive mode and create by soft a frame detector . We will use the CD signal as mentioned by CENELEC only when we want to transmit a frame . Different software frame detectors can be implemented depending of the resources of your microcontroller. You can program your microcontroller to go in receive frame when it received the expected byte.

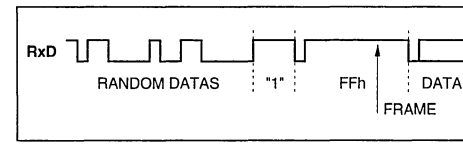
Figure 5 : Rxd Data Timing



So the preamble is for demodulator training (when you start a communication the 3 first bits are lost by the receiver) and when you will match with expected byte the micro-controller will go in receive frame routine.

On the ST6 microcontroller we have implemented the following frame detector.

Figure 6 : Preamble Detector



We put Txd = " 1" on the transmitter for around 4ms (for demodulator training) and after we send in asynchronous mode FFh following by the complete frame. On the receiver , we check that we have RxD equal to "1" for at least 7ms (we are looking for FFh), then we go in receive and we will have frame synchronisation on the first start bit of the data.

We did a trial in our lab with this system during 2 hours without having the ST6 going in frame receive routine on bad datas due to noise signal.

II.3- Implementation on ST6265

The C.S.M.A. (Carrier Sense Multiple Access) needs a Timer for its implementation. But the ST6265 timer 1 is already used for bit time and software carrier detect. Furthermore, sometimes the timer has several functions at the same time, so the timer programming becomes very complicated.

In order to simplify this programming, we have implemented a single time delay corresponding to bit time (f = 1200Hz). So for each mode there is a counter corresponding to a delay. The counters are incremented (or decremented) in the timer interrupt routine while they are cleared (or affected with values) in main program. For C.S.M.A. specifications, we use two counters :

- Xmit_count : This is the delay before retransmitting,
- Rmit_count : This is the delay before transmitting after a reception.

These counters are decremented in Timer 1 interrupt routine and flags are set when they become null. These flags are allowing the sending of a frame. Acknowledge frames are not concerned with these timing.

The timer will allow the sending of a frame after C.S.M.A. delays (see Figure 7).

With this way of programming, the places where counters are loaded are very significant (see Figure 8) :

- Xmit_count is loaded at the end of the message sending procedure in order to wait an acknowledge (30ms) and at the end of the reception of a good acknowledge (time between two transmissions of the same device : 125ms),
- Rmit_count is loaded at the end of a reception with a random value (time between two transmission of different devices : 85 to 115ms).

Figure 7 : Sending a Frame After C.S.M.A. Delays

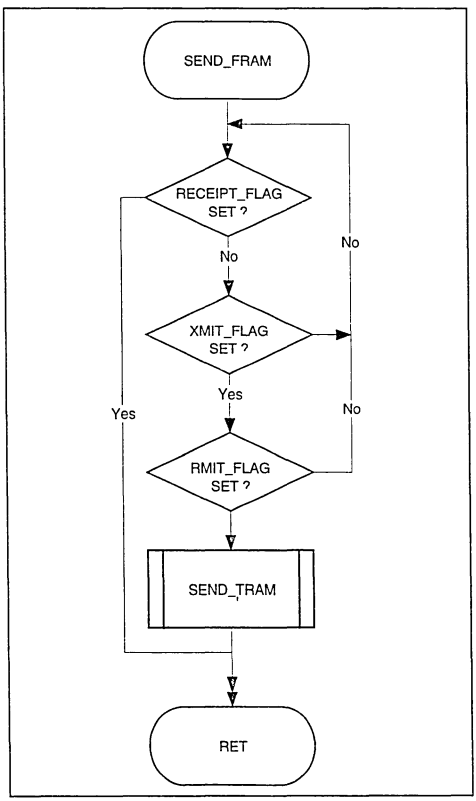
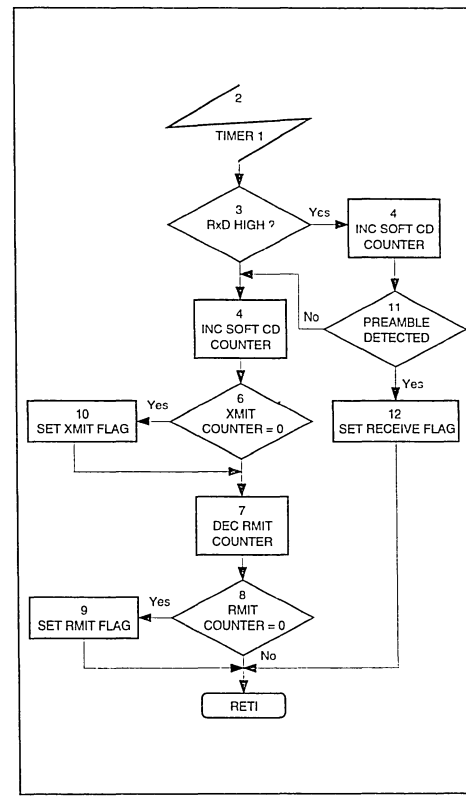


Figure 8 : Timer 1 Flow Chart



III - PHONE REMOTE SYSTEM

III.1 - General Description

The phone remote system is using the ST7537CFN chip and its line interface for power line communication (see Figure 9). The control unit is ST6265 microcontroller (SGS-THOMSON) that has several functions.

The telephone interface is described in further detail in next paragraph. The MCU mains functions are :

- detect a ring,
- take the line and hang up,
- decode DTMF code,
- make some "beep",
- control the modem chip,
- display its status (leds for instance).

These functions are the minimum required to provide remote control. The Figure 10 propose these functions.

Figure 9 : Block Diagram

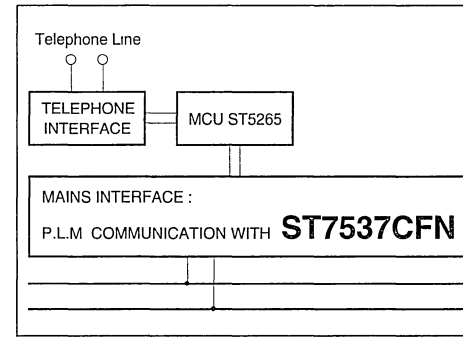
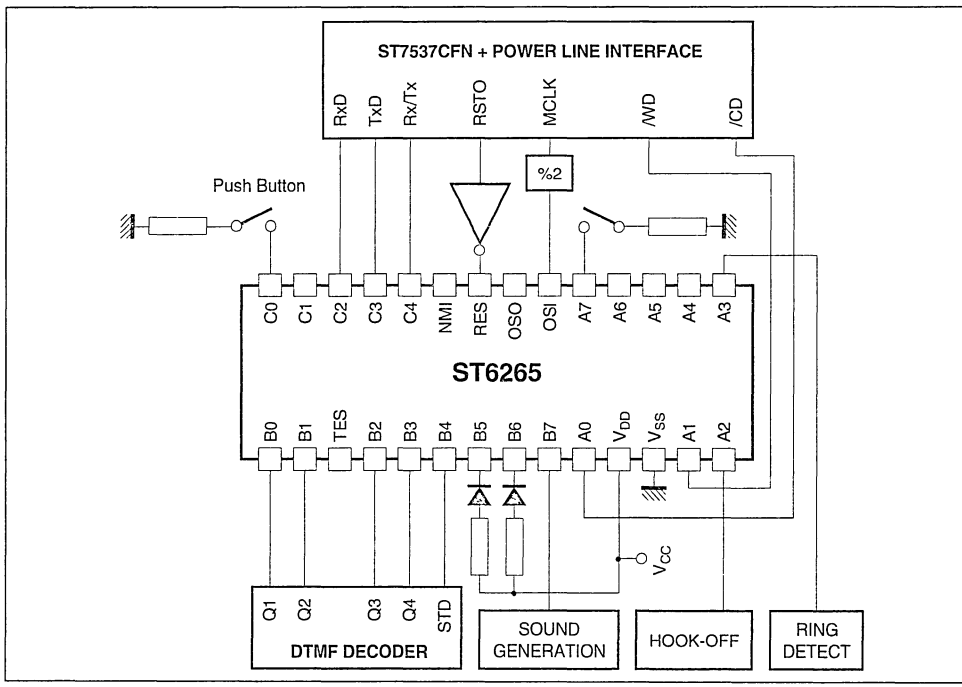


Figure 10 : ST6265 Application



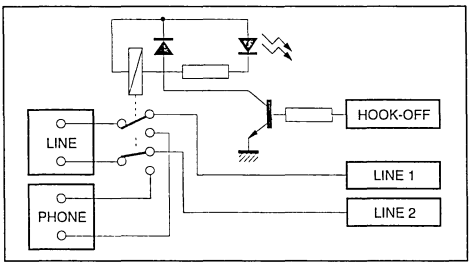
ST7537 interface

The ST6265 is directly connected to ST7537, excepted the clock that must be divided by a factor 2 (ST6265 is validated at 8MHz max. and ST7537 provides a 11MHz clock signal). For further details, refer to AN535.

Hook-off

The hook-off system must be able to take the line. A relay connected to the two wires of the telephone line complies with all regulations. See telephone interface part for more information.

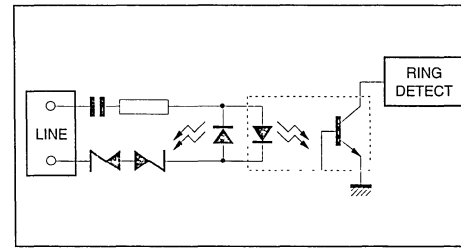
Figure 11 : Hook-off Schematic



Ring Detect

An opto-transistor is used to detect the ring signal on the line. So the system is isolated from the line and the microcontroller receive a 0 to 5V signal.

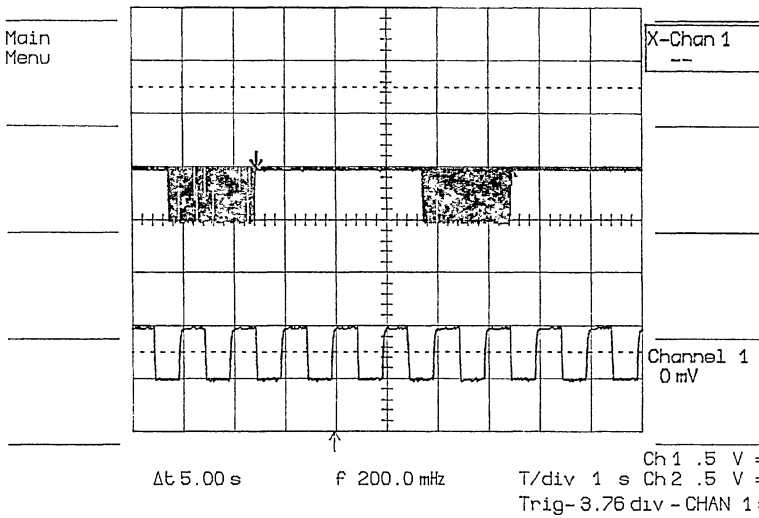
Figure 12 : Ring Detect Schematic



For example, this is what appears on ring detect pin with a French standard line (see Figure 13).

The first line is the ring detect signal which is zoomed on the second line. On French lines, the ring is about 1.5 second and the silence is about 3.5 second. That means a ring period of 5 seconds.

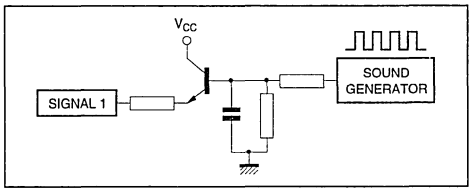
Figure 13 : Ring Detect Signal & Ring Detect Signal Zoomed



Sound Generation

Sound generation allows reply from the system. MCU just sends square signal that makes a beep.

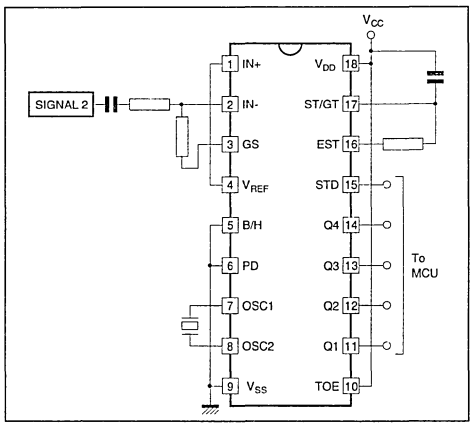
Figure 14 : Sound Generation Schematic



DTMF Decoder

Users send orders with DTMF code. These codes are decoded with a DTMF receiver LC7385 (SANYO). It is configured in single ended input. It has a dynamic range input of 29dBM.

Figure 15 : Single Ended Input Configuration

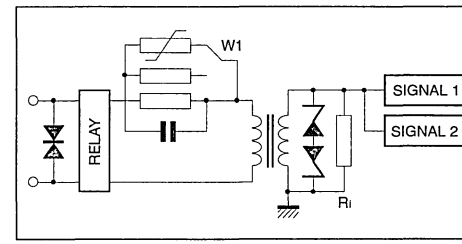


When receiving DTMF code, this IC chip is generating the following signal (see Figure 16).

III.2 - Telephone Line Interface

The line interface must verify regulation of system connected to telephone line, that's why it is described in detail here. Line interface input impedance and current consumption has been adjusted. In the following schematic, the transformer accept continuous current and current consumption is done by a resistor and a capacitor in parallel.

Figure 17 : Telephone Line Interface



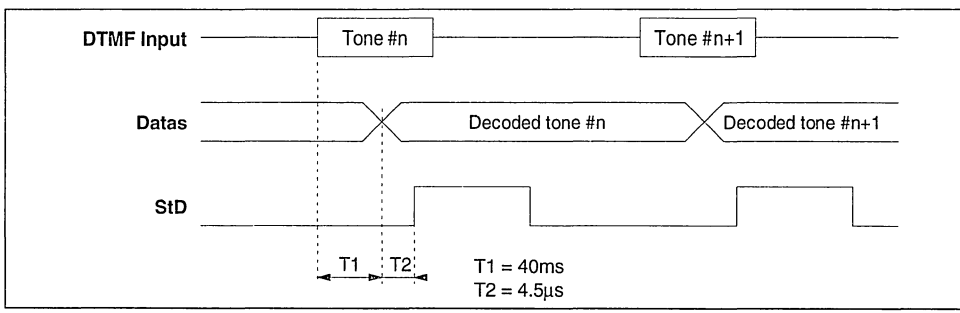
III.2.1- Isolation

As the phone remote system is connected to the telephone line, it must be isolated from high voltages that may occurs on it. There are two connections to the line :

- the ring detect interface is isolated with an optotransistor,
- the DTMF & sound generation interface isolation is made by a transformer and a voltage limitation by zener diodes.

Furthermore, a transil diode between the two line wires limits the input voltage.

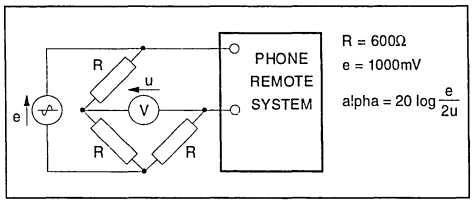
Figure 16 : DTMF Receiver Timing Diagram



III.2.2 - Input Impedance

The input impedance has been adjusted by changing RI value (see Figure 17) with a Wheastone's bridge method explained in the Figure 18.

Figure 18 : Wheastone Bridge



e is generated by a HP3325B generator and u is read on a Fluke 45 controller. We made e scanning frequency from 300 to 4000Hz. The maximum values for u are shown in the Table 3.

Table 3 : Error Voltage versus Ri

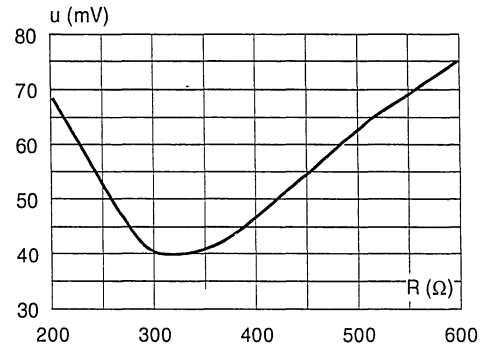
Ri (Ω)	u (mV)	Ri (Ω)	u (mV)	Ri (Ω)	u (mV)
200	69	325	40	400	47
275	44	350	41	500	63
300	40	375	45	600	75

Ri has been fixed at 300Ω. That mean an adapting coefficient (alpha) :

$$\text{alpha} = 20 \log \frac{1}{2 \cdot 0.04} = \mathbf{21dBm}$$

French standard specifies a value superior to 14dBm.

Figure 19 : Error Voltage Versus Ri



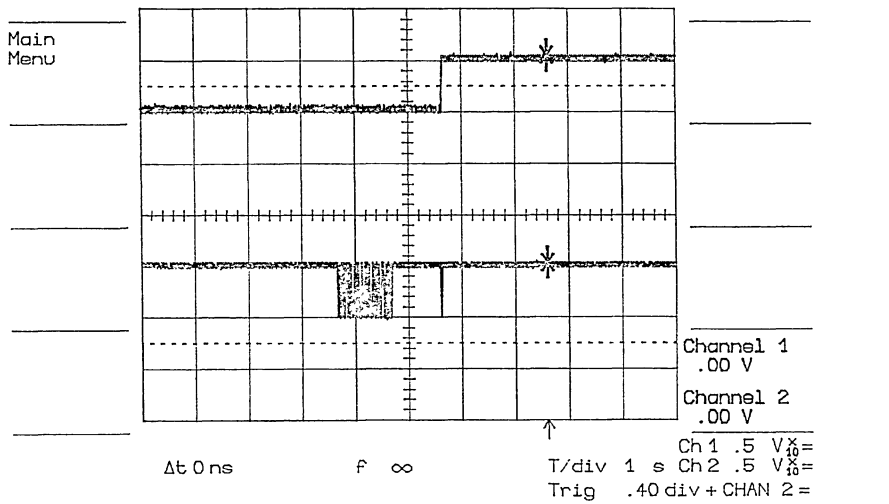
III.2.3 - Current Regulation

Line current regulation is not needed in several countries. For these countries, a strap allows to disable current regulation which is done by a CTP resistor.

III.2.4 - Hook-off Procedure

When taking the line, the system must care of the ring train. If it takes the line when phone is ringing, the relay will switch a voltage superior to 70 Volts. To avoid this, the best way is to wait a silence (no ring). The phone remote system is waiting the end of a ring to take the line, as shown in the Figure 20. The first line is the relay command and the second line is the ring signal.

Figure 20 : Hook-off Between Two Rings



III.3 - Mains Flow

The phone remote system has a very simple progress. It only has to wait after a ring, count for a pre-defined number of rings, take the line, ask for a password, and then send the user's orders on the power line network (see Figure 21).

For security reasons, the user has only three tries to enter his password. If this operation is successful, he is allowed to send orders, otherwise the system hangs up (see Figures 22 and 23).

Figure 21 : Phone Program Main Flow

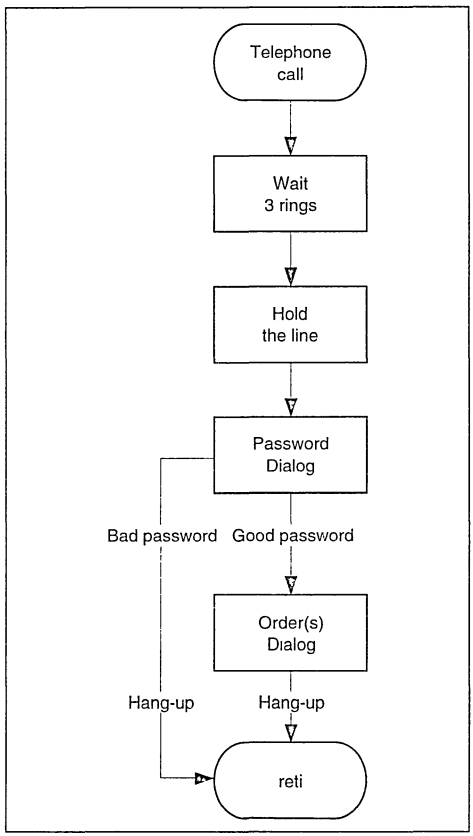


Figure 22 : Password Dialogue

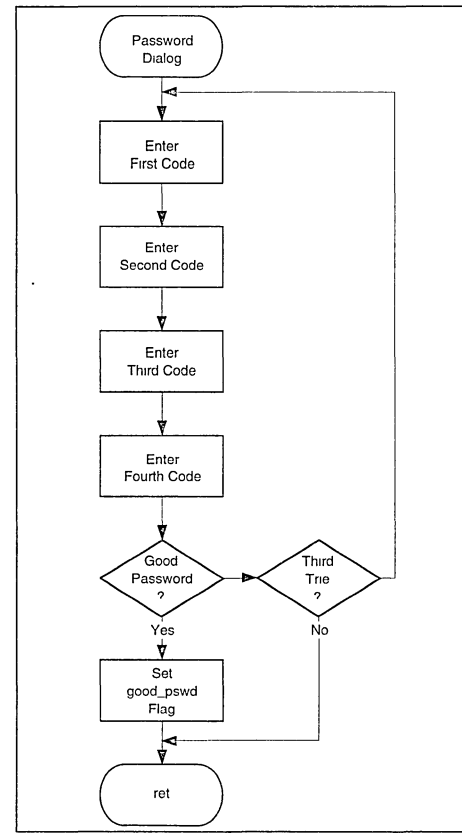
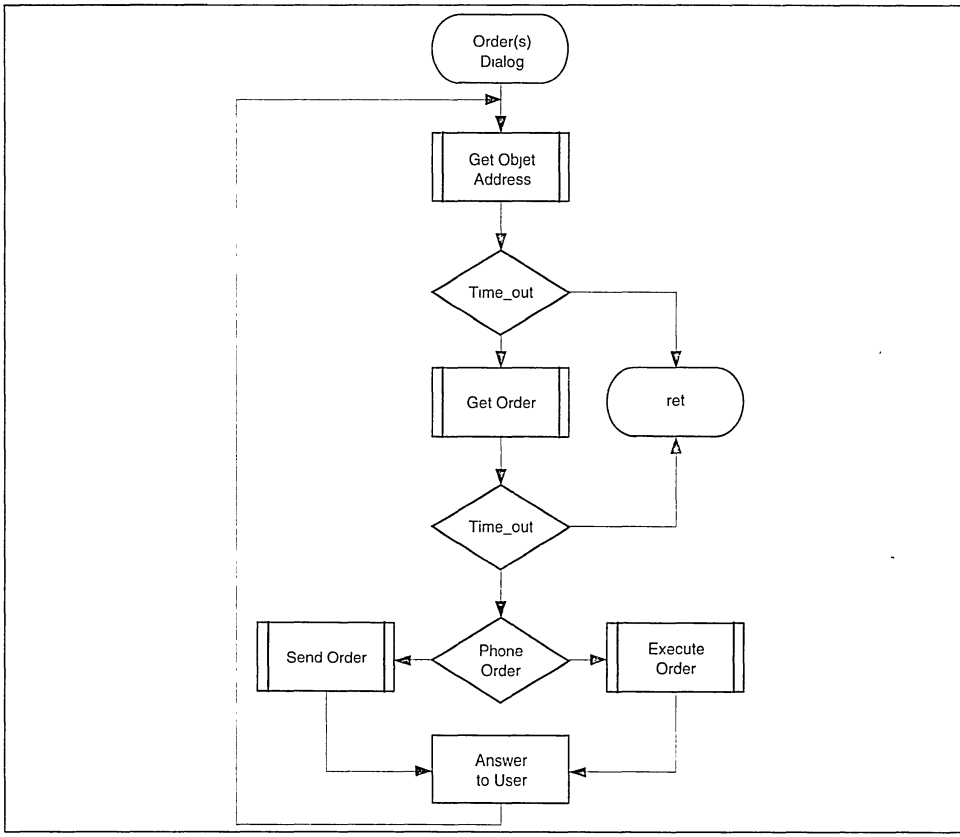


Figure 23 : Orders Dialogue



III.4 - Application Procedure

This part describes installation and utilisation of the phone remote system.

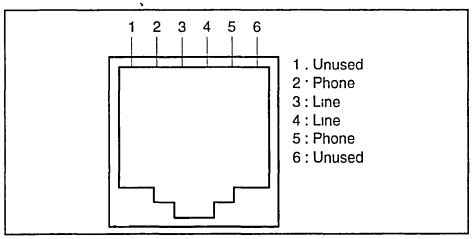
III.4.1 - Installation

The phone remote system needs to be connected to the mains and to the telephone line.

Connecting to mains :
Before connecting the phone remote system to mains, verify that the selected voltage is the same as your mains installation. The default voltage is 220 Volts/50Hz.

Connecting to telephone line :
The telephone line connector is a RJ11 type. This connector is wired according to French specifications.

Figure 24 : RJ11 Connector



III.4.2 - Description

The phone remote system owns several switches and LEDs that indicate status and allow the configuration of parameters as number of rings, confidential code, ...

Table 4 : Parts Description

Part	Description
Switch	User for switch the device ON/OFF
Mini switch	User to select the delay before hook-off : 3 or 5 rings
Push button	User to reinitialize the status LEDs (single push) or to reinitialze the protection code (3 seconds push)
Red LED (L1)	Violation LED (wrong code)
Green LED (L3)	Hook-off LED
Yellow LED (L4)	Ring LED
Orange LED (L2)	Bad power line network address : no acknowledge

III.4.3 - Use

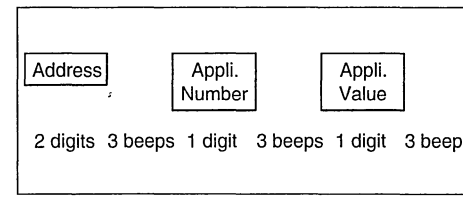
Enter Confidential Code

When calling the phone remote system, you have to wait three or five rings. Then the system hooks off and beeps three times. You have twenty seconds to enter the confidential code by using your phone keyboard. Only DTMF phones are supported. The initial value of the code is 0000, but of course you can change it. If the code entered is the good one, you are allowed to give orders. Otherwise, you have two other attempts.

Enter Orders

An order is an object address (two digits), an application number (one digit) and a value (one digit). After you have entered the objet address, you hear three beeps (or you have to retry). Then you enter the application number, and you hear three more beeps. At last, you enter the application value. If you hear three beeps, that means the message has been sent and that an acknowledge has been received. Then you are allowed to send an other order.

Figure 25 : Address Format



The slave sytems have address values from 00 to15. For these systems the application number select the dimmer (number 1) or the digit (number 2). The value is the number diplayed on the digit, or the light intensity. For instance :

- "15,2,0" will display 0 on the slave system wich address is 15,
- "13,1,9" will switch the light on slave system number 13 on.

There are special orders for phone control :

- if you enter "99,1", then the system will beep you the confidential code. If the code is 3456, you will hear 3 beeps then four, then five and then six beeps,
- if you enter "99,2", and four digits, these four digits will be the new confidential code to use for further call.

Table 5 : Allowed Orders

Enter	Values	Action
XX,Y,Z	$00 \leq XX \leq 15$ $0 \leq Z \leq 9$	Y = 1 Light intensity = Z Y = 2 Display value = Z
99,1		Beeps the confidential code
99,2,XXXX	$0000 \leq XXXX \leq 9999$	New value for confidential code

Local Configuration

The yellow LED is lighting when "the phone is ringing". After 3 or 5 rings (depending on mini-switch), the system takes the line, and the green LED remains on during all the phone dialogue. If three bad codes are sent, the red LED will switch on. If a power line communication error occurs, the Orange LED will light. The red and the orange LED will be left on, so a single push on the push-button will switch these LED off.

If you push on the push-button for more than 3 seconds, the confidential code will be changed to 0000. The confidential code is stocked in EEPROM and will remains even if you disconnect mains.

IV - CONCLUSION

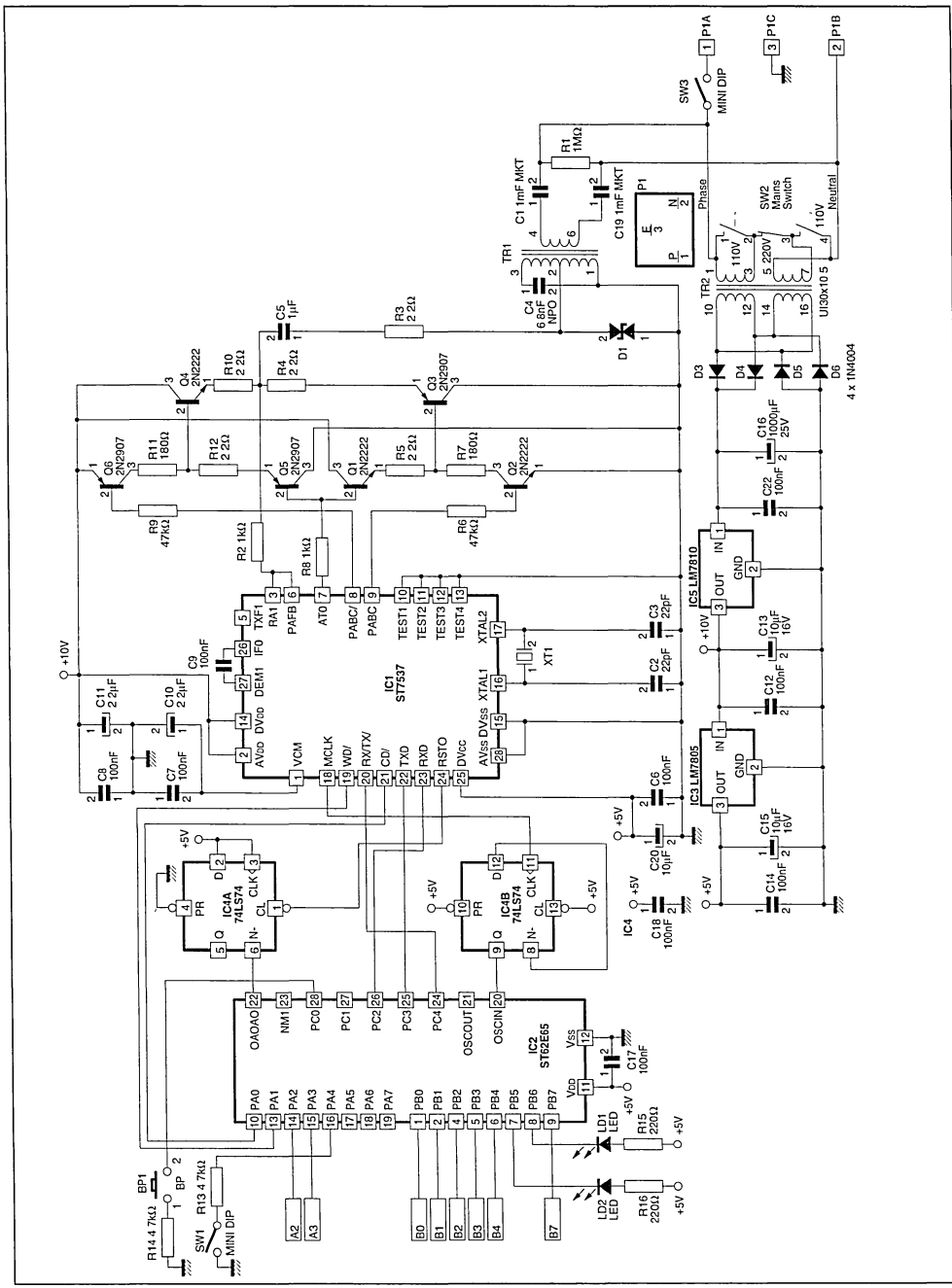
The phone remote system increases the facilities offered by your automation network. With this system you can send orders by using DTMF code. By using a memory phone or a pocket dialler, you would be able to send orders only by choosing the system you want to talk to. For instance, you push the button called "heating on" and the order is immediately sent to the heater. Furthermore, you could select an other temperature for the heating system, or ask for the temperature in any room of your house. These improvements are possible by adding a voice generator (SGS-THOMSON has dedicated voice chips) and if temperature sensor and heater are connected to the network. The phone remote system detailed in this note has not all these facilities, but it is a very low cost application with only few components and low cost choice for MCU and phone interface. The ST7537 is providing the power line communication and a hardware watchdog, while leaving resources for a low cost microcontroller.

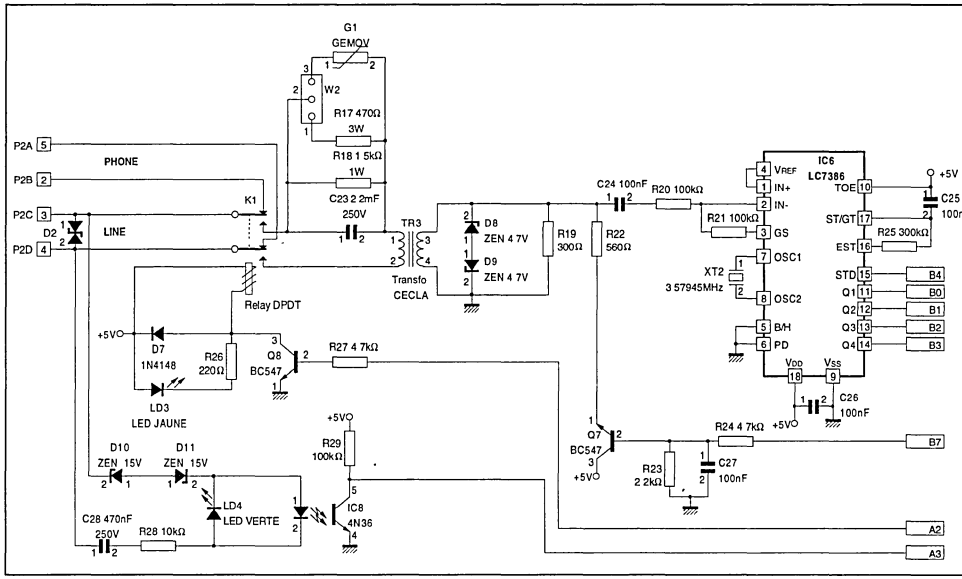
V - ANNEXE 1 : BILL OF MATERIALS

Designation	Value	Package
BP1	BP	BP
C1	1mF	CAPC4
C2	22pF	CAPD4
C3	22pF	CAPD4
C4	6.8nF	CAPD4
C5	1µF	CAPC4
C6	100nF	CAPD4
C7	100nF	CAPD4
C8	100nF	CAPD4
C9	100nF	CAPD4
C10	2.2µF	CAPC4
C11	2.2µF	CAPC4
C12	100nF	CAPD4
C13	10µF	CAPC4
C14	100nF	CAPD4
C15	10µF	CAPC4
C16	1000µF	CAP12
C17	100nF	CAPD4
C18	100nF	CAPD4
C19	1mF	CAPC4
C20	10µF	CAPC4
C22	100nF	CAPD4
C23	2.2mF	CAPC4
C24	100nF	CAPD4
C25	100nF	CAPD4
C26	100nF	CAPD4
C27	100nF	CAPD4
C28	470nF	CAPD4
D1	Diode	DIODE
D2	Diode	TRANSIL
D3	1N4004	DIDB8
D4	1N4004	DIDB8
D5	1N4004	DIDB8
D6	1N4004	DIDB8
D7	1N4148	DIDA8
D8	ZEN.4.7V	DIDA8
D9	ZEN.4.7V	DIDA8
D10	ZEN.15V	DIDA8
D11	ZEN.15V	DIDA8
G1	GEMOV	GEMOV
IC1	ST7537	ST7537
IC2	ST62E65	ST62E65
IC3	LM7805	BTO220
IC4	74LS74	DIL14
IC5	LM7810	BTO220
IC6	LC6385	DIL18
IC8	4N36	DIL6
K1	RELAY_DPDT	RELAY
LD1	LED	LED
LD2	LED	LED

Designation	Value	Package
LD3	LED_JAUNE	LED
LD4	LED_VERTE	LED
P1	ALIM220V	ALIM220V
P2	RJ11	RJ11
Q1	2N2222	BTO922
Q2	2N2222	BTO922
Q3	2N2907	BTO5
Q4	2N2222	BTO922
Q5	2N2907	BTO5
Q6	2N2907	BTO5
Q7	BC547	BTO5
Q8	BC547	BTO5
R1	1mΩ	RES8
R2	1kΩ	RES8
R3	2.2Ω	RES8
R4	2.2Ω	RES8
R5	2.2Ω	RES8
R6	47kΩ	RES8
R7	180Ω	RES8
R8	1kΩ	RES8
R9	47kΩ	RES8
R10	2.2Ω	RES8
R11	180Ω	RES8
R12	2.2Ω	RES8
R13	4.7kΩ	RES8
R14	4.7kΩ	RES8
R15	220Ω	RES8
R16	220Ω	RES8
R17	470Ω 3W	RES14
R18	1.5kΩ 1W	RES12
R19	300Ω	RES8
R20	100kΩ	RES8
R21	100kΩ	RES8
R22	560Ω	RES8
R23	2.2kΩ	RES8
R24	4.7kΩ	RES8
R25	300kΩ	RES8
R26	220Ω	RES8
R27	4.7kΩ	RES8
R28	10kΩ	RES8
R29	100kΩ	RES8
SW1	MINI_DIP	SMINI
SW2	COMMUT	COMMUT
SW3	MINI_DIP	MINI
TR1	TOKO	TOKO
TR2	UI30X10.5	UI30X10.5
TR3	TR3	TRANSFO CECLA
W2	STRAP_3PTS	STRAP
XT1	CRYSTAL	CRYSTAL
XT2	3.57945MHz	HC49U

VI - ANNEXE 2 : SCHEMATICS




G1
GEMOV
W2
R17 470Ω
3W
R18 1 5kΩ
1W
C23 2 2mF
250V
TR3
Transfo
CECLA
D8
ZEN 4 7V
D9
ZEN 4 7V
R19
300Ω
R22
560Ω
C24 100nF
R20 100kΩ
R21 100kΩ
IC6
LC7386
VREF
IN+
IN-
GS
OSC1
OSC2
B/H
PD
VDD
Vss
TOE
ST/GT
EST
STD
Q1
Q2
Q3
Q4
+5V
C25
100nF
R25 300kΩ
XT2
3 57945MHz
B4
B0
B1
B2
B3
C26
100nF
P2A
PHONE
P2B
P2C
P2D
LINE
K1
Relay DPDT
+5VO
D7
1N4148
R26
220Ω
Q8
BC547
R27 4 7kΩ
LD3
LED JAUNE
D10
ZEN 15V
D11
ZEN 15V
R29
100kΩ
LD4
LED VERTE
IC8
4N36
C28 470nF
250V
R28 10kΩ
Q7
BC547
R24 4 7kΩ
R23
2 2kΩ
C27
100nF
B7
A2
A3
AN488-27 EPS

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

4.5W FLYBACK CONVERTER FOR POWER LINE MODEM APPLICATIONS

By Joël HULOUX, Patrice MOREL, Jean-Michel RAVON

SUMMARY

I - SWITCHING POWER SUPPLY DESCRIPTION

The power supply described in this document has been realised in order to powering the Power Line Modem ST7537 applications. It provides 5V and 10V to supply the ST7537 and a microcontroller. This power supply has the advantage of its small size, that is very important for Home System devices.

I.1 - General Description

The power supply is a 4.5W flyback converter which supply 10V DC with a switching supply process. Its uses a UC3845 circuit that generate a 32.5kHz square signal which drives a STK 2N50 MOS or equivalent. The 5V DC is provided by a regulator L78M05 CS. In the version of the supply tested the supply board side is less than 4cm.

Table 1 : Flyback Converter Specifications

Parameter	Test Conditions	Value	Unit
Output Voltage	20% of load 100% of load	10.15 and 5 9.75 and 5	V
Output Maximum Power		4.5	W
Dynamic of Input Voltage		130 to 264	V DC
Precision of Regulation	Between 20% and 100% of load	4	%
Variation in Voltage According to Mains	At 75% of load	0.4	%
Yield	80% of max. power, 0.218A on 10V and 0.15A on 5V 100% of max. power, 0.3A on 10V and 0.15A on 5V 100% of max. power 0.45A on 10V	59 61 74	%
Working Temperature	Ambient temperature : 25°C	55	°C
Maximum Life Time	Ambient temperature : 85°C Ambient temperature : 55°C	8000 64000	Hours
Output Noise Level	I_O = 450mA before regulator	80 peak-peak	mV
Protective Measure	Short cut protected		

I.2 - Schematic

Figure 1 : Flyback Converter

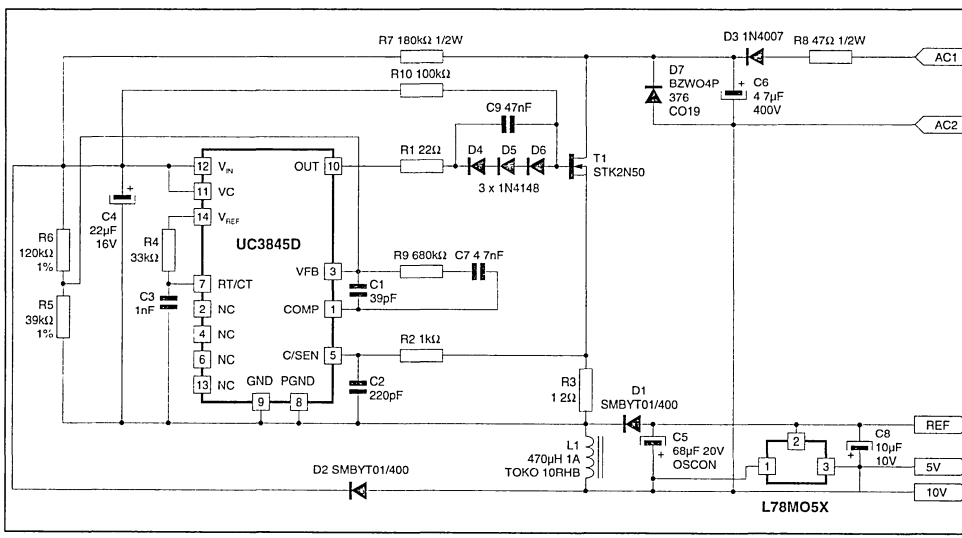


Table 2 : Bill of Materials

Item	Quantity	Reference	Part
1	1	C1	39pF
2	1	C2	220pF
3	1	C3	1nF
4	1	C4	22µF 16V
5	1	C5	68µF 20V OSCON SANYO
6	1	C6	4.7µF 400V
7	1	C7	4.7nF
8	1	C8	10µF 10V
9	1	C9	47nF
10	2	D1 D2	BYT01/400 BYT01/400
11	1	D3	1N4007
12	3	D4 D5 D6	1N4148 1N4148 1N4148
13	1	D7	BZWO4P 376 CO19
14	1	L1	10RHB 470µH TOKO or equivalent
15	1	R1	22Ω
16	1	R2	1kΩ
17	1	R3	1.2Ω
18	1	R4	33kΩ
19	1	R5	39kΩ 1%
20	1	R6	120kΩ 1%
21	1	R7	180kΩ 1/2W
22	1	R8	47Ω 1/2W
23	1	R9	680kΩ
24	1	R10	100kΩ
25	1	T1	STK 2N50 MOS (SOT-82) 600Ω 500V
26	1	U1	UC3845D (SGS-THOMSON)
27	1	U2	L78M05X

II - SWITCHING POWER SUPPLY TESTS

Several tests have been done on the flyback converter and this section describes the way the tests have been done and shows the results.

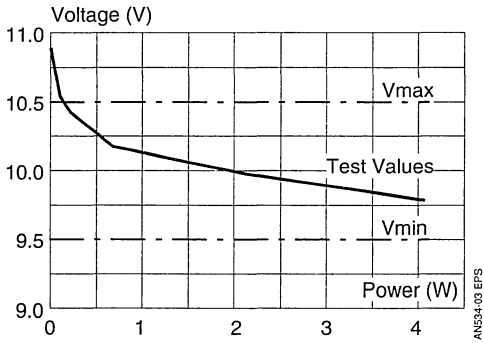
II.1 - Voltage versus Power

The power supply has been loaded on its 10V output by resistors of different values . The 5V DC has not been connected. The power has been calculated and results are shown below.

Table 3 : Voltage, Current and Power Consumption

Load (Ω)	Voltage (V)	Intensity (10^{-3}A)	Power (W)
Nothing	10.87		
23.5	9.78	420	4.07
47	9.97	210	2.11
150	10.17	68	0.68
500	10.42	20.8	0.22
1,000	10.54	10.5	0.11
Demo-board Tx	10.02	86.8	
Demo-board Rx	10.18	28.5	

Figure 2 : Voltage Versus Power



II.2 - Current Consumption

The consumptions of the ST7537 demo-board have been tested during the B.E.R. test with the flyback converter powering the transmitter, and then the receiver. Values are given in the table below. In the Worst case, the load on the mains was only a few Ohms : all the laboratory devices were connected to the mains (with a personal computer which has a switching supply). The 5V does not depend on the impedance of the mains, it is only powering the microcontroller (ST90E28L6), the 3 LED's, and the RS232 driver (MAX 232).

Table 4 : Flyback Converter with Demo-board Consumption

Voltage	Transmitting	Receiving
220V AC	25.8mA	19mA
220V AC (worst case)	31mA	19mA
10V DC	86.8mA	28.5mA
10V DC (worst case)	133mA	28.5mA
5V DC	32mA	35.4mA

II.3 - B.E.R. with Switching Power Supply

The Bit Error Rate test needs two demo-boards, one for transmission, the other one for reception. The board with the switching supply has been set in receive mode and in transmit mode. Each time the B.E.R. results are the same as with regulated supply. On the transmitting demo board the pin TEST1 is set to 1 to allow continuous transmission.

Figure 3 : Switching Power Supply Powering Transmitter

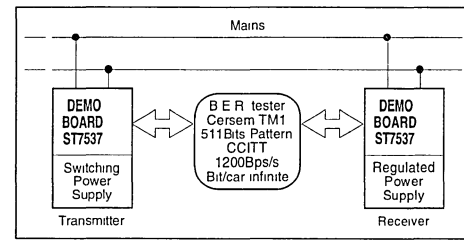
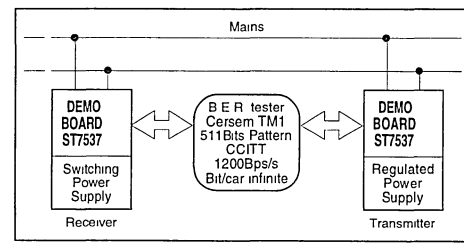


Figure 4 : Switching Power Supply Powering Receiver



Results

Measurements are made using the laboratory power network. On this network, several devices were producing noise :

- Tektronix 2247A oscilloscope,
- HP 3225B synthetiser,
- Weller WECP-20 soldering iron,
- Topward TPS 4000 power supply,
- A light.

There has been no error for more than a 15 minutes test period (in the two conditions). In 15 minutes there is :

$$15 \cdot 60 \cdot 1200 = 1080000 \text{ bits.}$$

That means a B.E.R. $< 10^{-6}$.

B.E.R. $< 10^{-6}$

II.4 - Spectrum Frequency and Cenelec

The P.L.M. has been connected to a spectrum analyser in order to see the influences of the flyback converter. The Cenelec specification n° EN 50065-1 PEAK values limit has been drawn (see the following table). The spectrum has been done with a HP 3585 spectrum analyser, configured according to Cenelec ; that means a bandwidth of 100Hz, and the use of the MAX HOLD function in order to keep the peak values.

Table 5 : Cenelec Specifications

Frequency Band (MHz)	Limits (dBµV) Peak Values	Limits (dBµV) Means
0.15 to 0.5	66 to 46	56 to 46
0.5 to 5	56	46
5 to 30	60	50

Figure 5 : ST7537 Demo-board with Flyback Converter

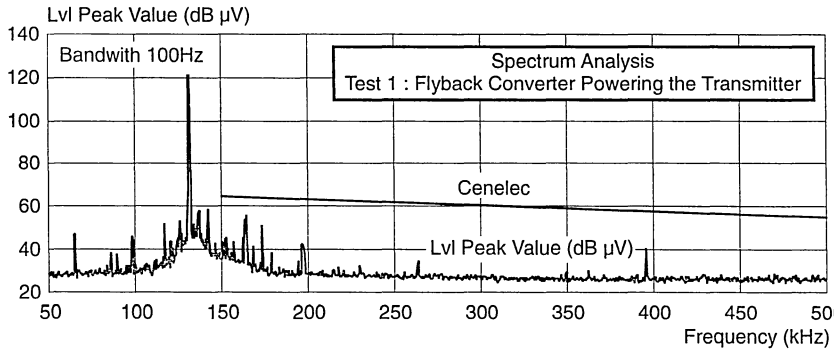
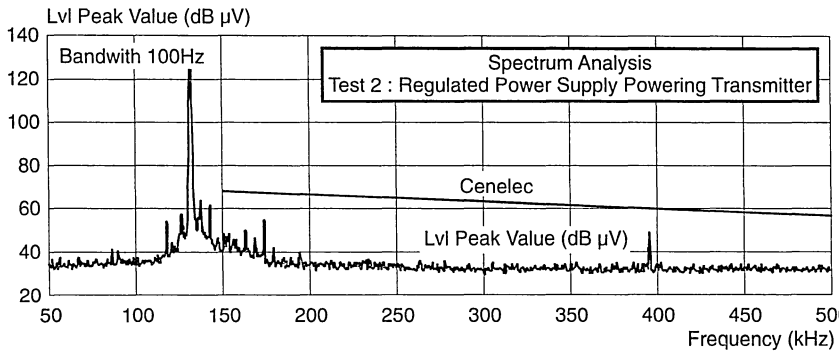


Figure 6 : ST7537 Demo-board with Regulated Supply



III - MEASURE ON MAINS

During these tests, the transmit signal has been measured by connecting a spectrum analyser as described in Figure 7. This operation needs to isolate the analyser from the earth and to connect its ground level to the neutral. A capacitor of 2.2nF is used to filter the 50Hz and a voltage divider (resistors) is used to measure the signal. The supply is shielded to avoid radiation.

The values give theses results :

$R_{TOTAL} = 4800 + 1450 = 6250\Omega$

$F_C = (R_{TOTAL} \cdot C \cdot 2 \cdot \pi) = 1.1kHz$

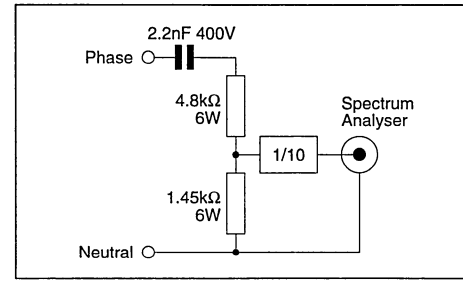
$F_C = 1.1kHz$

$$V_{REAL} = 10 \cdot V_{MES} \cdot \frac{R_{TOTAL}}{1450}$$

$V_{REALdB} = V_{MESdB} + 32.7dB$

The values read on the spectrum analyser are 32.7dB under the real values. The values on all the following spectrums has been corrected and take into account the 32.7dB gain.

Figure 7 : Connecting the Spectrum Analyser to the Mains



III.1 - Mains Alone

In this case, the spectrum analyser has been connected to a laboratory mains without device on. This test gives an idea of the noise you can get on the mains.

Figure 8 : Mains without Device

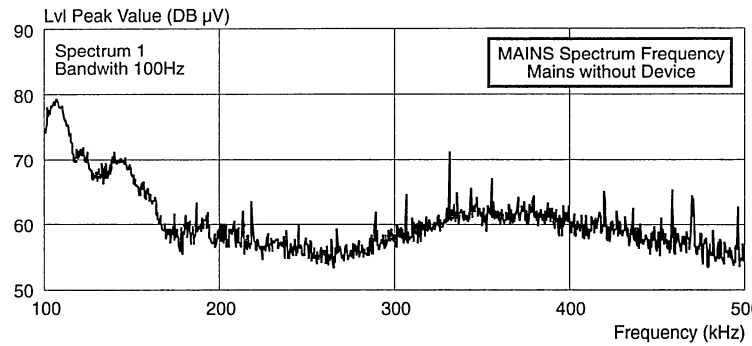
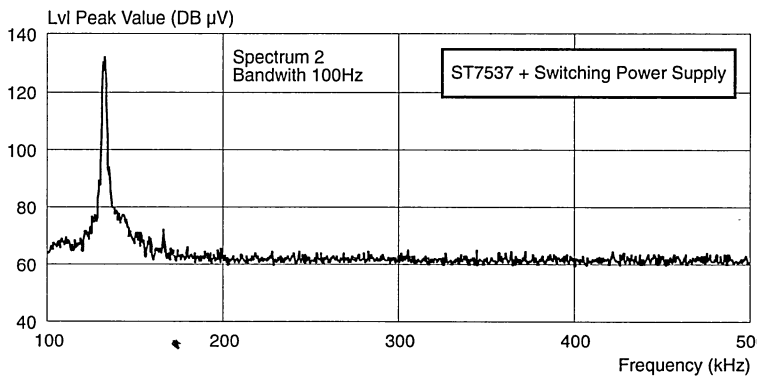


Figure 9 : The P.L.M. is Alone on the Mains



III.2 - Mains with P.L.M. Communication

This spectrum has been realised while the B.E.R. test was in progress. The two ST7537 demo-board were the only devices connected to the mains. The peak values have been obtained by using the MAX HOLD function of the spectrum analyser. The carrier frequency is at 132.45kHz.

III.3 - Mains with P.L.M. Communication and Several Generators

These tests have been realised with several devices such as drill, Hoover, ... So the noise appears on the spectrum, and it is possible to compare the noise level and the signal level. During all theses tests, the B.E.R. test was in progress.

No errors has been detected.

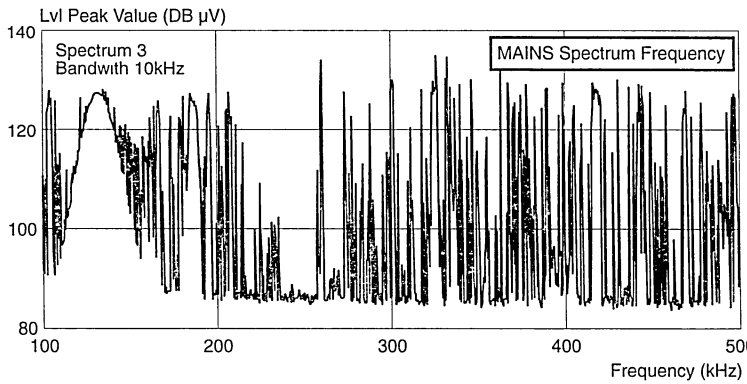
The table on the following page gives the conditions at the moment of the realisation of the spectrum. The values have been registered by the use of the spectrum analyser HPIB interface, and are peak values. Each graph is realised with 1001 points.

Table 6 : Conditions of the Tests

Spectre	Device	Conditions	Frequency Range
Figure 11	DRILL BOSCH 420W REF. 1123-7	Several Switch ON/OFF Accelerating	100kHz to 500kHz
Figure 12	DRILL BOSCH 420W REF. 1123-7	Several Switch ON/OFF Accelerating	1kHz to 5MHz
Figure 13	Neon Lighting OSRAM15W REF. RZ2	Several Switch ON/OFF	50kHz to 500kHz
Figure 14	Hoover NILFISK 700W MODEL GST	Several Switch ON/OFF	50kHz to 500kHz
Figure 15	All Laboratory Devices	Normal Use	50kHz to 500kHz

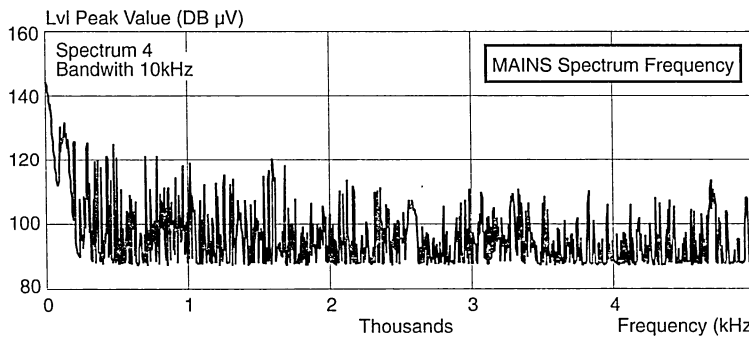
All the devices are operating under 220V 50Hz. The analyser bandwidth has been set to 10kHz. The different spectrum are given below.

Figure 10 : Transmitting while Using a Drill



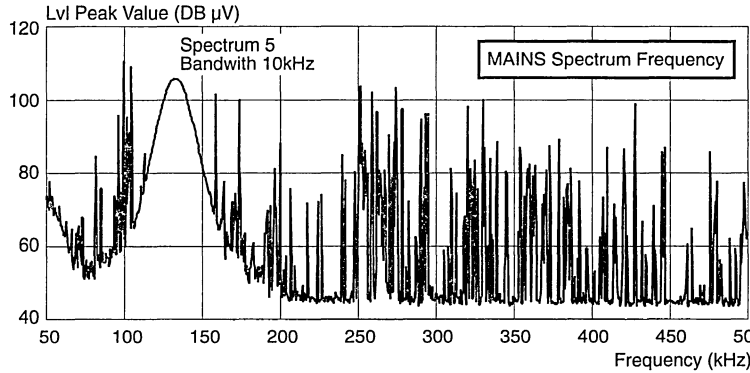
AN534-11 AI

Figure 11 : Transmitting while Using a Drill (wide Spectrum)



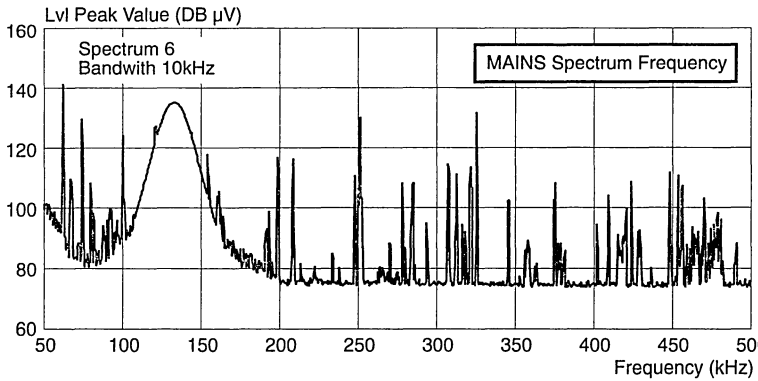
AN534-12 AI

Figure 12 : Transmitting while Using a Neon Lighting



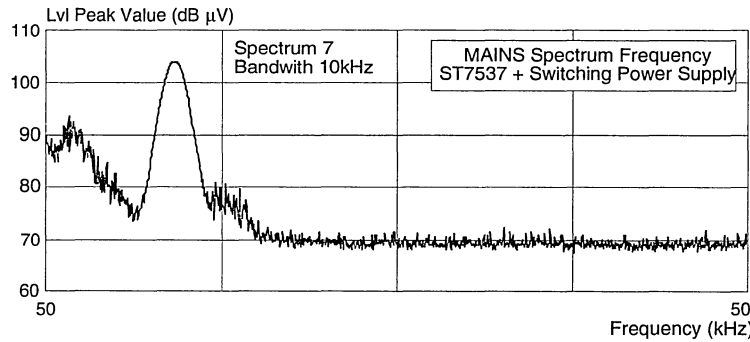
AN534-13 AI

Figure 13 : Transmitting while Using a Hoover



AN534-14 AI

Figure 14 : All the Laboratory Devices on Use



AN534-15 EPS

In this last graph, the level of the ST7537 carrier has fallen to 104dB µV because of the load on the mains (we have connected a personal computer which has a switching power supply). Nevertheless, the communications occurs without any errors.

IV - CONCLUSION

Even with a high level noise or important disturbance on mains, or even a load under 5Ω, the ST7537 has a B.E.R. under 10^{-6} (we have not detected any error during all the test period). Power line system communication needs a ST7537, a power line interface, a control system, and a 10V DC supply. The power line interface is already existing, and SGS-Thomson provides a large range of microcontrollers (interface between ST9 microcontroller and ST7537 has been realised). The flyback converter comes to provides 10V DC for P.L.M. (and a 5V DC for the microcontroller) and replace the classical regulated supply. The ST7537 and power line interface consumption lets more than 2.5W for microcontroller and application, available in both 5 and 10V. The 10V fluctuations are under the ST7537 specifications (which needs 10V ±10%).

In fact, the flyback converter is really suited to ST7537 applications :

- Its voltages complies with ST7537 specifications,
- It does not disturb the transmit spectrum,
- The performances of the power line modem are the same as with regulated supply,
- Its size allows its use in small systems, like home system applications,
- The 4.5W power provides supply for both P.L.M and microcontroller.

ST7537 POWER LINE MODEM

By Joël HULOUX

SUMMARY

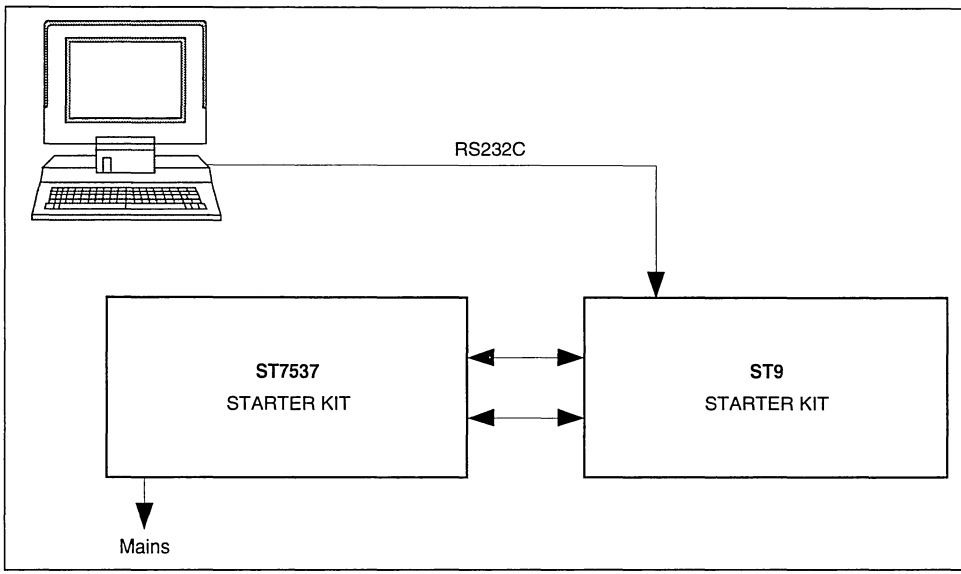
I - INTRODUCTION

The ST7537 starter kit has been developped in order to help customer for designing a Home Automation System.

Everything needed for using the micro-controller ST9 is on board and the ST7537 starter kit is fully compatible with the ST9 starter kit.

All connections for ST7537 and ST9 are on board and the only wiring you have to do is your application.

The board has been designed for the ST90E40 so you are not limited on resources and you can choose the microcontroller you want.



II - STARTER KIT FEATURES

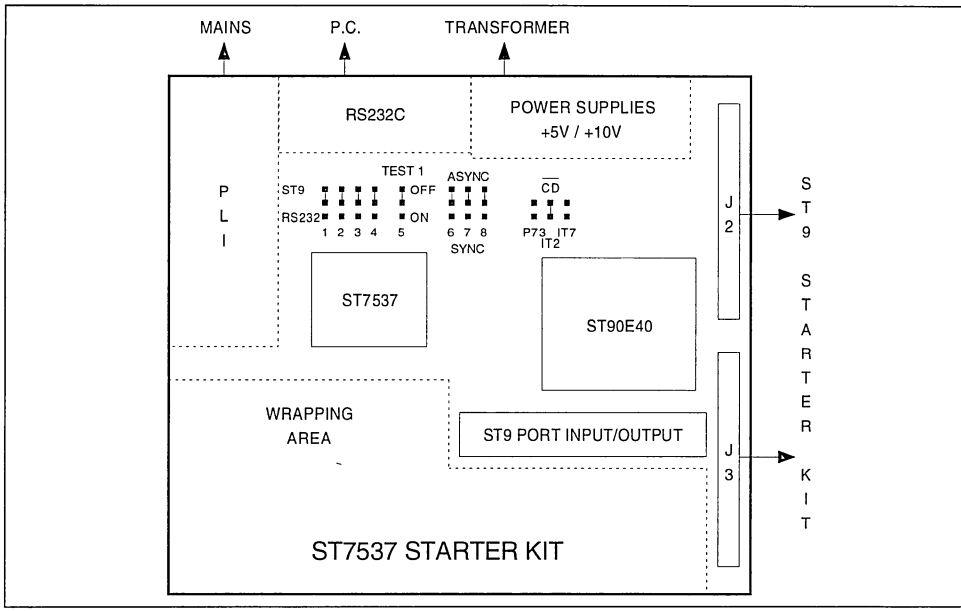
On the starter kit 2 applications are selectable :

- RS232C application
- ST9 application

With the starter kit you have :

- application note
- starter kit board
- power transformer
- RS232C cable
- demo software

III - BOARD CONFIGURATION



- Application choice is made thanks to SW 1,2,3 and 4. You can select ST9 or RS232C application.
- During your developpment you could need to transmit more than 1 sec (specified by CENELEC), you can do so with SW5 (Pin TEST1 of 7537).
- The Carrier Detector can be connected either to INT2, INT5 or INT7 by using the JP1.
- The starter can be configured to work in asynchronous or in synchronous mode with :

SW6	→	Rxd connected to Sin (P70)	Async
		Rxd connected to P74	Sync
SW7	→	Txd connected to Sout (P71)	Async
		Txd connected to P75	Sync

IV - SCHEMATICS

Figure 1

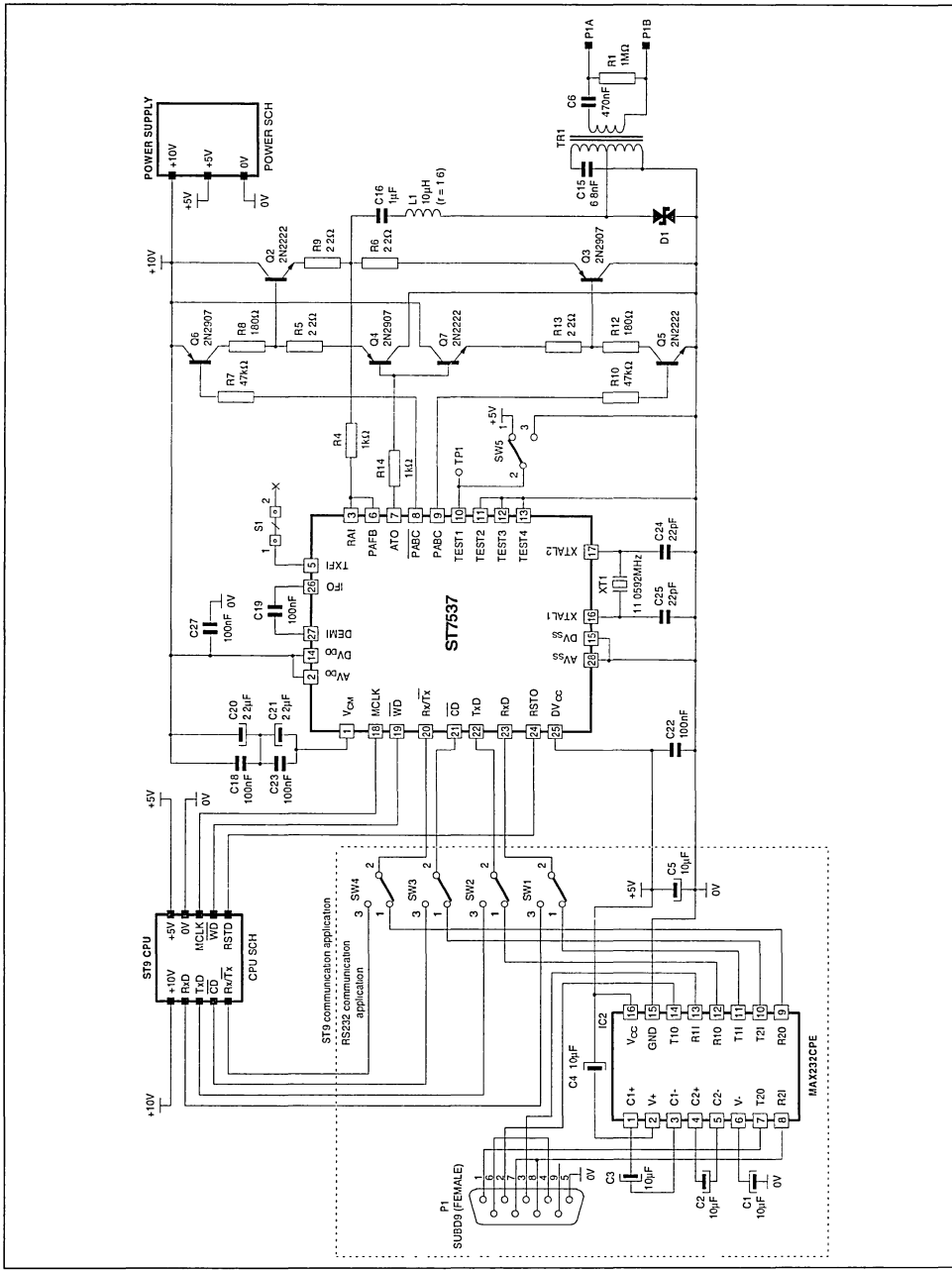


Figure 2

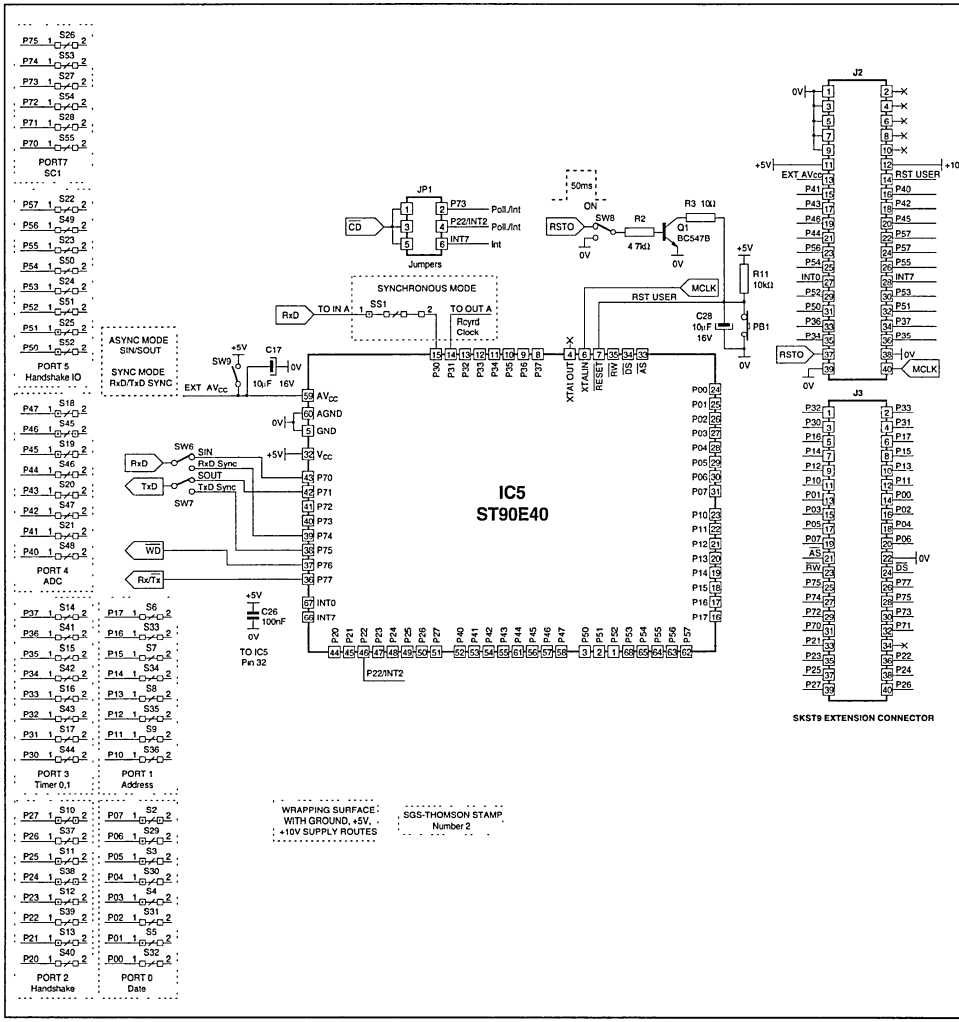
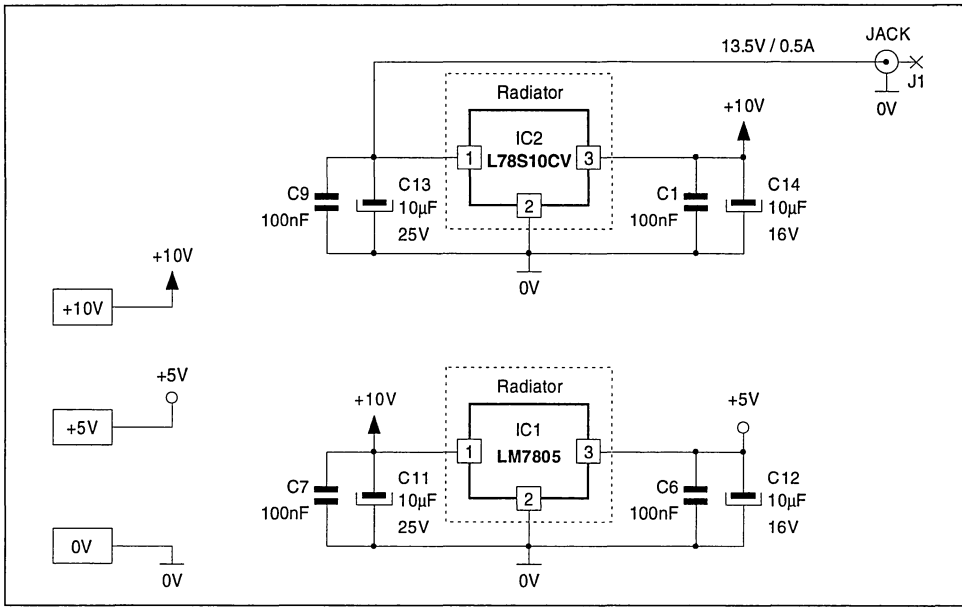

IC5
ST90E40
JP1
Jumpers
SYNCHRONOUS MODE
ASYNC MODE
SIN/SOUT
SYNC MODE
RxD/TxD SYNC
WRAPPING SURFACE
WITH GROUND, +5V,
+10V SUPPLY ROUTES
SGS-THOMSON STAMP
Number 2
J2
J3
SKST9 EXTENSION CONNECTOR
PORT7
SC1
PORT5
Handshake IO
PORT4
ADC
PORT3
Timer 0,1
PORT1
Address
PORT2
Handshake
PORT0
Data
7537-82 EPS

Figure 3


13.5V / 0.5A
JACK
J1
0V
Radiator
IC2
L78S10CV
1
2
3
+10V
C9
100nF
C13
10µF
25V
C1
100nF
C14
10µF
16V
0V
+10V
+10V
+5V
+5V
0V
0V
Radiator
IC1
LM7805
1
2
3
+10V
+5V
C7
100nF
C11
10µF
25V
C6
100nF
C12
10µF
16V
0V
7537-83 EPS

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SYNCHRONOUS POWER LINE MODEM COMMUNICATION WITH ST9 MULTIFUNCTION TIMER

Required tools : ST9/ST7537 PLM Starter Kit, By O. GARREAU

INTRODUCTION

This application note provides an example of an ST9 MFT application handling a Home Automation synchronous protocol. It presents a way to easily communicate on a synchronous Network. Each node of this network may consist of the Power Line Modem (PLM) Starter Kit or of the Home Service (HS) macro-component, provided that it includes the ST9 plus ST7537 modem chipset.
This PLM Starter Kit helps also in developing the ST9 version of 'HOME SERVICE' European Home Automation Protocol.

The ST7537 modem may work in both synchronous and asynchronous modes at a Baud rate of 1200. There is no problem in building an asynchronous interface with the ST9 due to the capabilities of its SCI (Serial Communication Interface). The asynchronous protocol may be programmed directly and all work is done by the SCI. However the synchronous protocol has different requirements.

In order to program a synchronous protocol, it is not possible to use the SCI lines that are reserved for asynchronous communications. The solution resides in using the Multifunction Timer of the ST9.

The most simplified synchronous protocol may consist in a simple 3-wire link (The Receive Data line, RxD, the Transmit Data line, TxD and the signal Ground).

Similar to the asynchronous mode, no clock signal is available in the PLM synchronous mode and the time reference is included in the RxD signal. It is clear that the clock frequency should be known and determined in advance by both emitter and receiver. For our application working as the LAYER 0 of the 'HS' Protocol, this frequency is 1200Hz and generates thus a 1200 baud rate. Note that the signals concerned (RxD and TxD) are 'NRZ, Non Return to Zero' signals.

The first task that the following procedure performs is 'Transmission BitClock Recovery'. Here the Multifunction Timer T0 of the ST9 is used in the background. This basic clock signal is also output on a timer pin (T0OUTA).

The procedure that tests the link between distant modems, consists in sending from the master modem a standard frame, compatible with the 'HS' protocol or not, and in sending back from the slave modem the received frame in order to make a match test, for example, in the master system (which is, in our case, controlled by a Windows 3.1(TM) program).

This method can even validate asynchronous modes. The test frame is stored in the internal memory of the ST9 (in the first 128 bytes of the Register File).

In addition to the RxD and TxD lines, it is possible to improve protocol management with extra lines called RSTO, CDn, RXTXn and WDn. These lines mean respectively RESET modem controller, CARRIER DETECT, RECEIVE OR TRANSMIT, and WATCHDOG signal. 'n' means that the signal is active LOW.

These lines are specific to the ST7537 modem as it is working in its HALF-DUPLEX mode. The direction of data flow is chosen by RXTXn state. CDn indicates that the modem is about to receive data. The WATCHDOG signal is used by the modem to check the presence and activity of the CPU (ST9) and if activity (meaning a minimum of one negative transition per second) is absent, the modem will try to reset the CPU.

To prevent this shut down, WDn may be connected to the recovered BitClock (1200 transitions per second) or to an IO port (P76 in this case).

Note : To fully understand this Note, it is recommended that the reader refers to the relevant chapters of the ST9 databook for the Multifunction Timers.

I - HARDWARE LINK BETWEEN ST9 AND ST7537

Figure 1 shows the schematic of this link. As can be seen, no additional hardware or components are needed. This interface needs only 5 point-to-point wires plus the signal ground. It is the lowest cost way to connect a ST7537 to an ST9.

All wires are TTL compatible and mono-directional. Only one 8-bit port 7 of the ST9 is required, Port 3.0 (T0INA) is also reserved for this application, signal on T0OUTA (P3.1) is the recovered clock, event trigger and control the timer, P7.3 P7.4 P7.5 P7.6 P7.7 are used as simple TTL I/O bits.

The RxD line is managed by a technique which attaches a double function to this single signal. RxD triggers the timer and is acting as a synchroniser. Its level indicates also the input bit state. The kernel of this application is a sophisticated software PLL.

P7.3 is programmed as an input and reads Carrier Detect signal (CDn).
P7.4 is programmed as an input and reads the current input bit state (RxD).
P7.5 is programmed as an output and sends the current output bit (TxD).
P7.6 is programmed as an output and activates the WatchDog signal (WD).
P7.7 is programmed as an output and chooses the direction of data flow (RXTXn).

The corresponding timing chart of these signals is given in the next section. Note that it is not necessary to connect ST7537 signals like DVCC (Digital Output Supply Voltage), RSTO (Reset Output) and MCLK (Master Clock) when this application is running on the ST9 STARTER KIT. The signal ground is of course essential and common to all these lines. When the ST7537 Starter Kit is in stand-alone mode, the ST9 uses RSTO and MCLK

II - TIMING CHARTS OF CONTROL AND DATA SIGNALS

Figure 2 shows the timing and event charts considering an example of 3 bits input or output or both. The first chart displays Carrier Detect signal, which enables the start of transfer.

The second timing shows the input signal used as trigger and data signal. Each '0' or '1' pulse lasts 833.3µs. The third line is a relative time axis for the internal counter T0. The next axis is the 'Event' axis. The next chart displays the output waveform for the recovered BitClock; this preferably should have a 50% cyclic ratio.

The last chart is an example of the TxD output signal.

Figure 1 : Direct Connection in the Stand-alone Mode

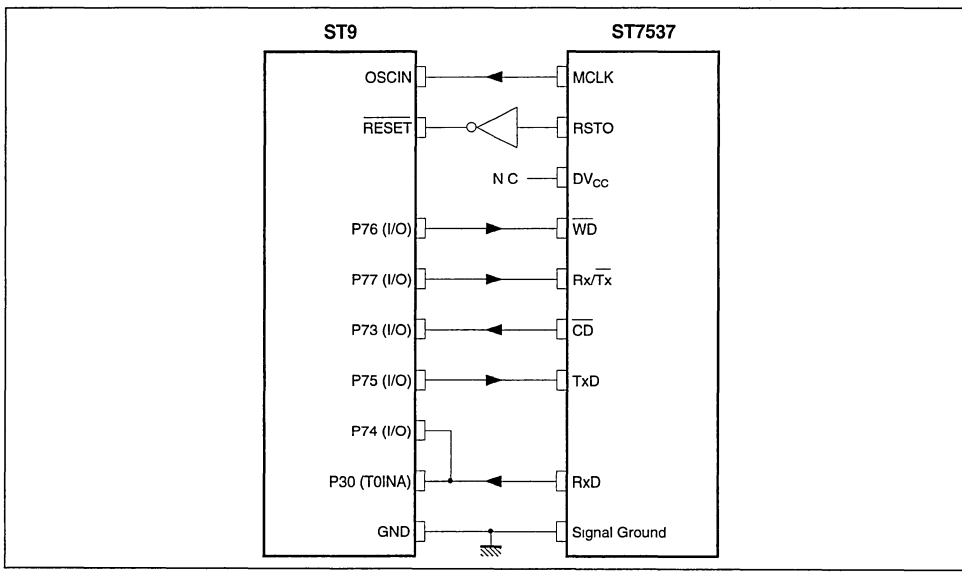
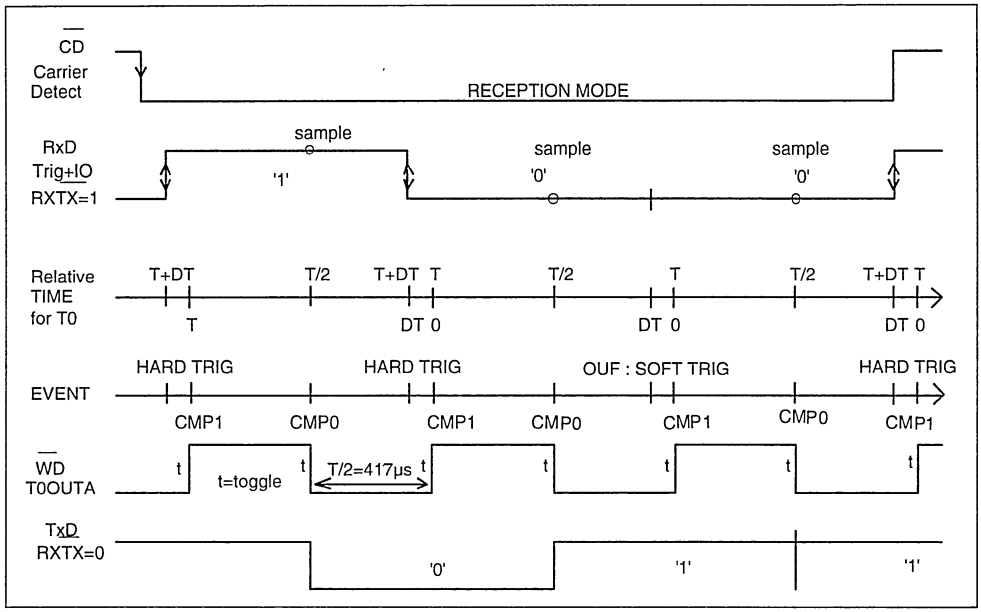


Figure 2 : Timing Chart of Signal and Data Signals



All the powerful features of a ST9 timer are used in this application. These include Hardware Trigger (HT), Software Trigger (ST), Compare (CMP0, CMP1) and Over/UnderFlow (OUF) Events. Both HT and ST events reload TIMER0 from the REG0R Load register. The HT event is automatically generated by every low to high or high to low transition on the RxD line.

The CMP1 event is used to rebuild the initial clock frequency (of the emitter). The CMP0 event samples the input signal on RxD or outputs the transmitted signal on TxD or both.

The OUF event (over-under/flow) allows the counter to be reloaded by an ST action, this acts as a WatchDog, controlled under software and corrects (synchronises) for frequency shift, frequency fluctuations and phase shift.

During the time gap (called DT), these parameters may vary and can be taken into account, if their variation is not too wide. A software parameter controls this correction : 'variation' represents a percentage of the whole bit pulse period, called T.

Figure 3 : Software Structure

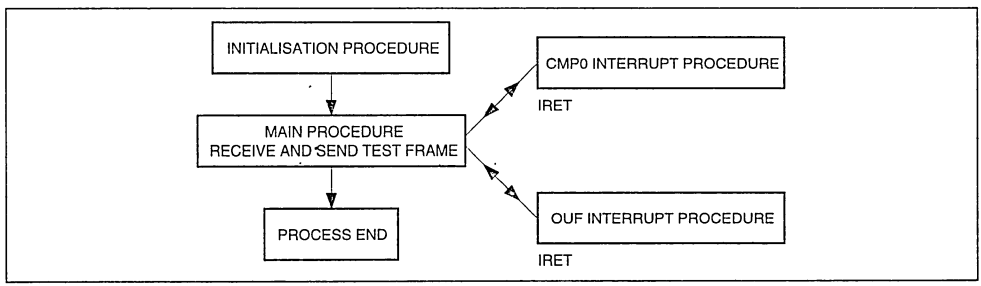
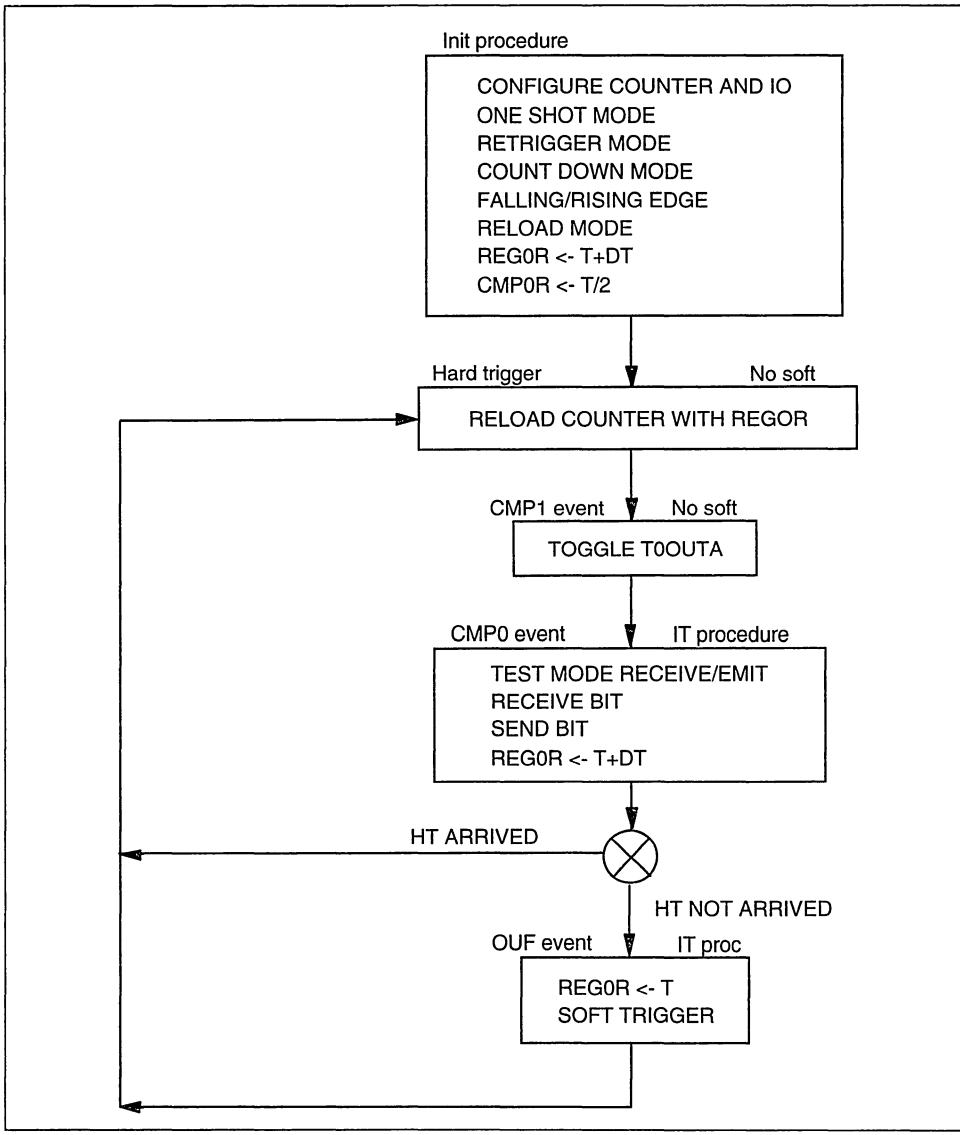


Figure 4 : Procedure Algorithm



III - SUMMARY

The aim of this application note is to demonstrate to Hardware designers just how simple it is to interface an ST7537 with a member of the ST9 family. The schematic described in part one is an example of the electrical link, however it also depends on a good quality and conformity of input signals.

First, it is obvious that the RxD signal should be perfectly stable and defined during the acquisition phase. Then, its working frequency (1200Hz) should be reasonably stable and the stability should not be worse than 90%. With practical testing, it is shown that the application works correctly between 1150Hz and 1250Hz. All these characteristics are software programmable.

This routine has been tested at various transmission rates, from 300Hz up to 9600Hz. The software defines constants called 'Rxxxxbds' that correspond to these rates. That way, this application software will stay compatible with new generations of multi-speed ST7537 modem.

Warning : the user must RECALCULATE these constants if the ST9 has an external clock (crystal) DIFFERENT to the frequency used in this example.

The nominal working frequency should be 1200Hz or 2400Hz in the case of the 'HS' protocol.

In this protocol, data packets are composed of a particular frame. Each frame starts with a specific header. Typically the beginning of such a header is 4 bytes: generally FFh, FFh, AAh and AAh. Many bits of the first FFh may be lost but the synchronisation is made actually on the AAh bytes. It is thus possible to improve the accuracy of the process. The byte AAh is a succession of bits at '1' and '0' and can allow frequency optimisation. Using first the timer 0 in its 'Capture' mode will define the precise distant frequency, a pre-calibration.

This software improvement may be useful in case of a distant frequency very far from the expected working frequency (1200Hz in this case).

The user is free to modify these routines. The bits of Port 7 (P73, P74, P75, P76 and P77) are used here as I/O bits. It is clear that another port may be defined as I/O port in order to free access to PORT 7.

Finally, the user can test a link between two distant nodes, or on a bigger network, and use equally synchronous or asynchronous protocol .

As a conclusion, the ST9 microcontroller is a cost effective solution for home automation modem applications and a synchronous protocol like 'HS' or other customer protocol can be performed in the background, requiring little CPU time.

IV - APPENDIX : SCHEMATICS OF ST7537 STARTER KIT

Figure 5 : PLM Interface

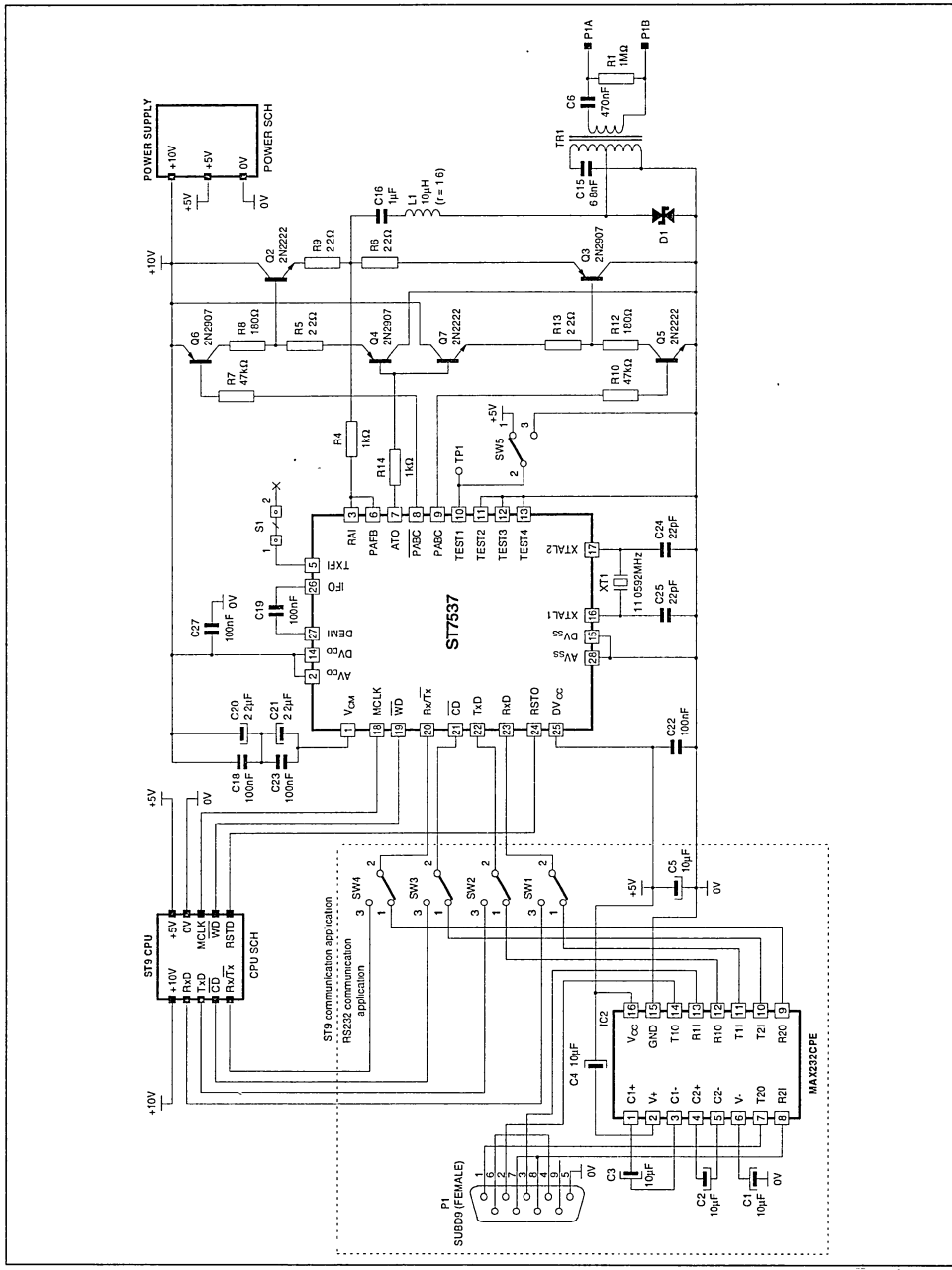


Figure 6 : ST9 Connections

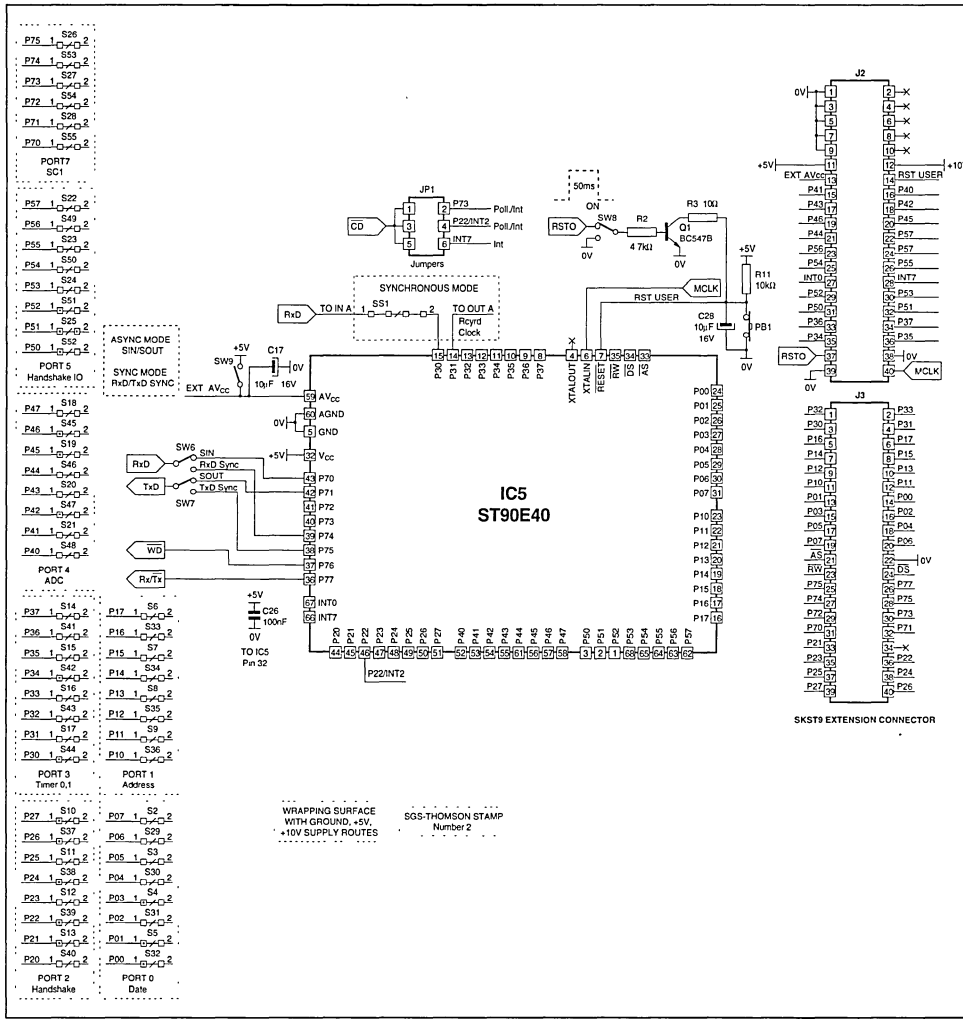
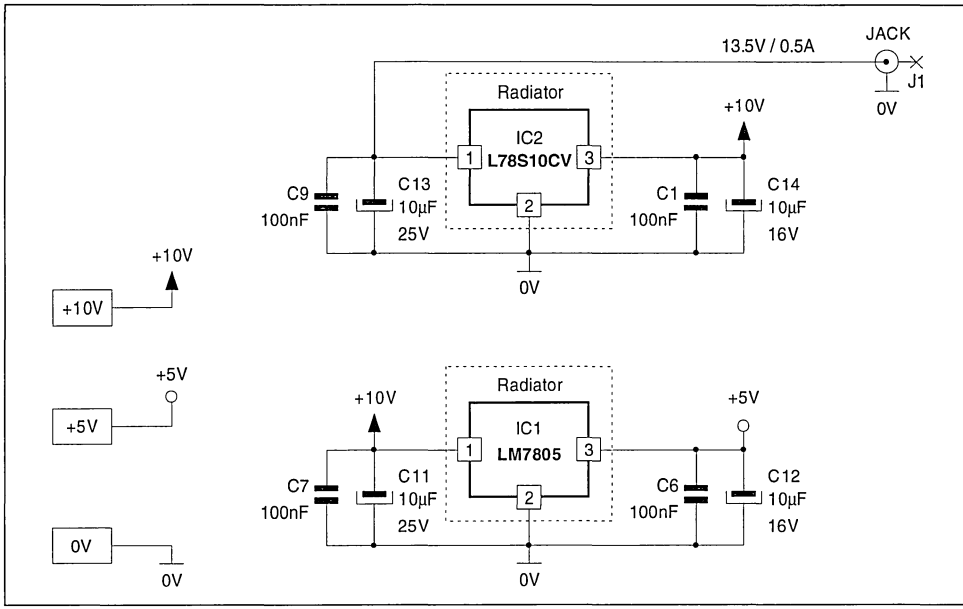


Figure 7 : Power Supply



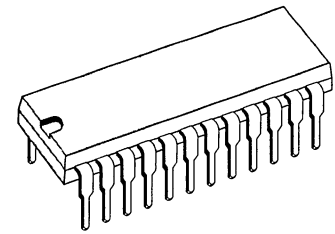
PACKAGES

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DDIP24 TBL

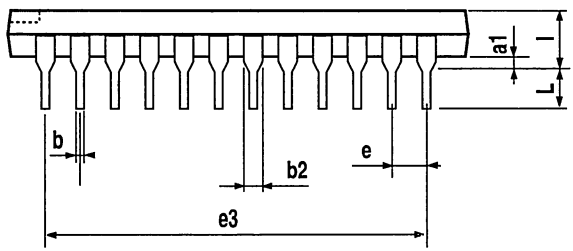
SGS-THOMSON MICROELECTRONICS

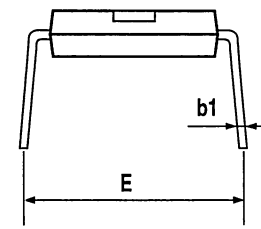
OUTLINE AND MECHANICAL DATA

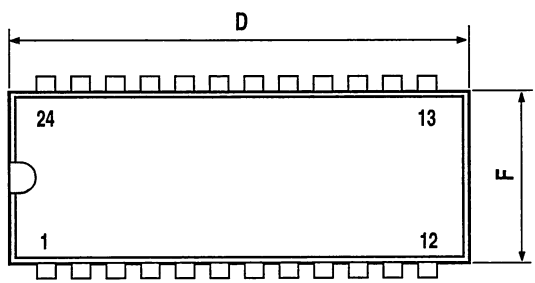


DIP24 EPS

DIP24







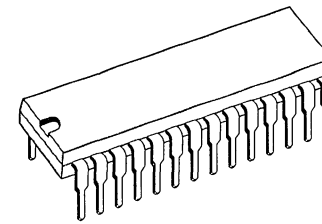
PM-DIP24.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.4			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DDIP28 TBL

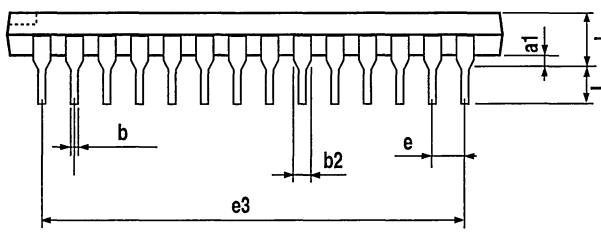
SGS-THOMSON MICROELECTRONICS

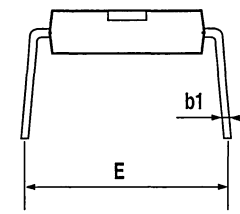
OUTLINE AND MECHANICAL DATA

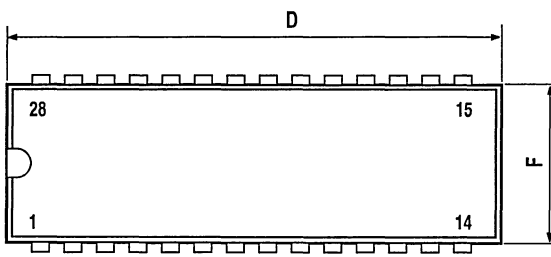


DIP28 EPS

DIP28







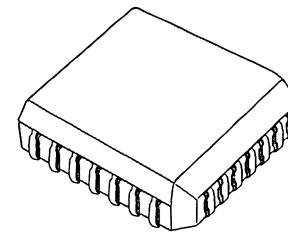
PM-DIP28 EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

DPLCC28 TBL

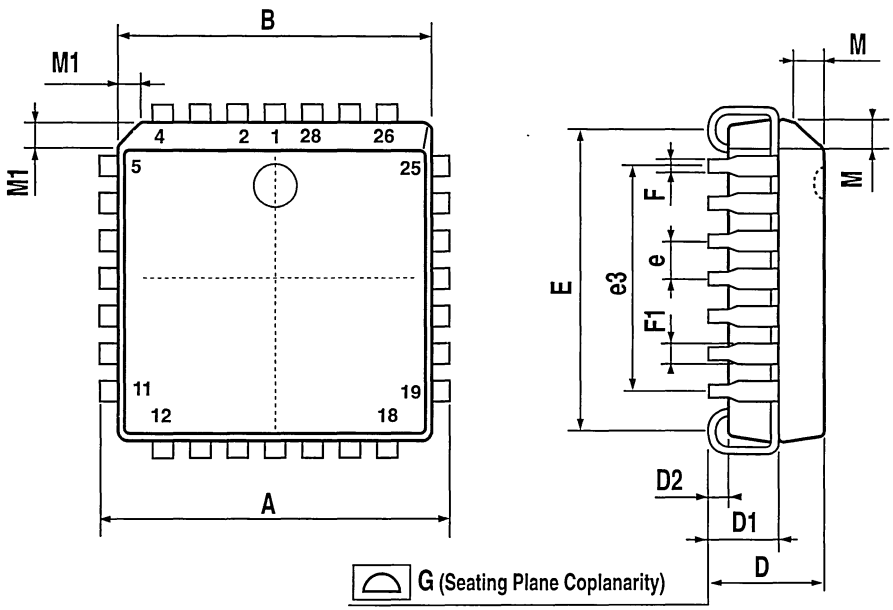
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PLCC28 EPS

PLCC28



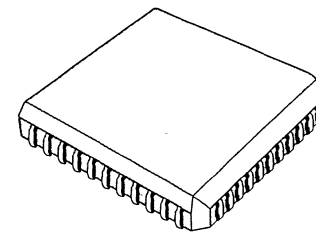
PMPLCC28 EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

DPLCC44 TBL

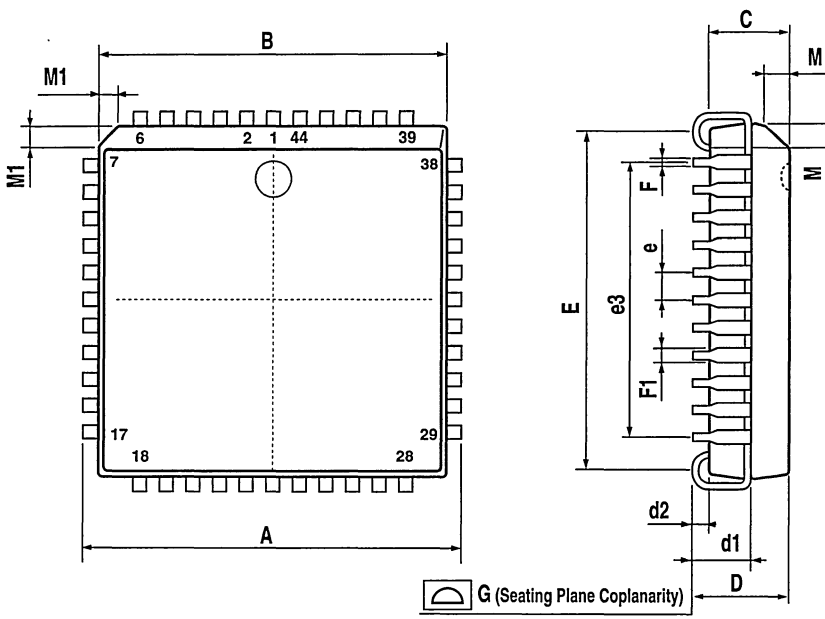
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PLCC44 EPS

PLCC44



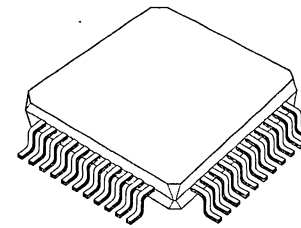
PMPLCC44 EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1		0.25			0.01	
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.35		0.50	0.014		0.020
C			0.17			0.007
D	15.75	16.00	16.25	0.620	0.630	0.640
D1	13.90	14.00	14.10	0.547	0.551	0.555
D2		10.00			0.394	
e		1.00			0.039	
E	15.75	16.00	16.25	0.620	0.630	0.640
E1	13.90	14.00	14.10	0.547	0.551	0.555
E2		10.00			0.394	
F		1.60			0.063	
K	0° (min.), 7° (max.)					
L	0.45	0.60	0.75	0.018	0.024	0.030

DPQFP44 TBL

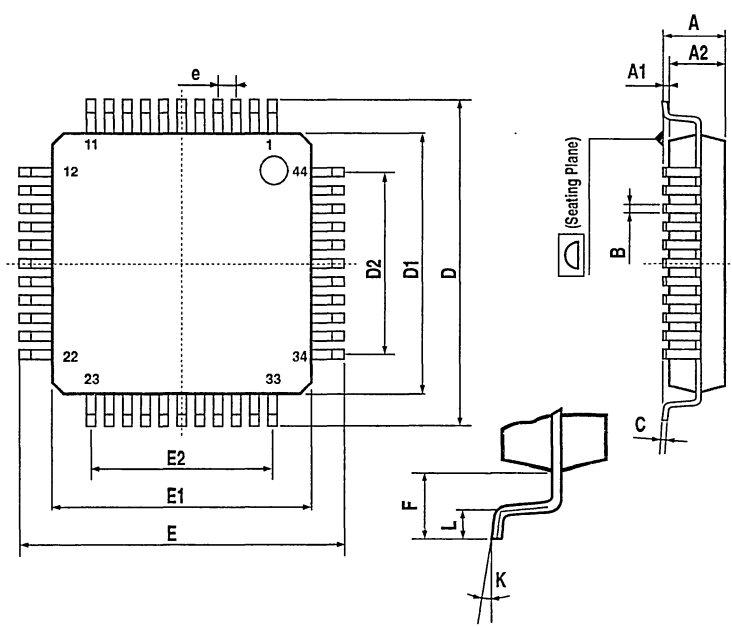
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PQFP44 WMF

PQFP44



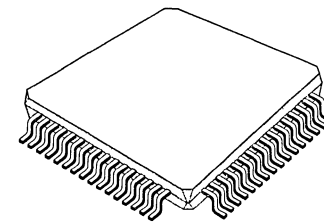
PMPQFP44 EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.40			0.134
A1	0.25			0.01		
A2	2.55	2.80	3.05	0.10	0.11	0.12
B	0.30		0.45	0.012		0.018
C	0.13		0.23	0.005		0.009
D	16.95	17.20	17.45	0.667	0.677	0.687
D1	13.90	14.00	14.10	0.547	0.551	0.555
D2		12.00			0.472	
e		0.80			0.031	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E2		12.00			0.472	
F		1.60			0.063	
K	0° (min.), 7° (max.)					
L	0.65	0.80	0.95	0.025	0.031	0.037

DPQFP64 TBL

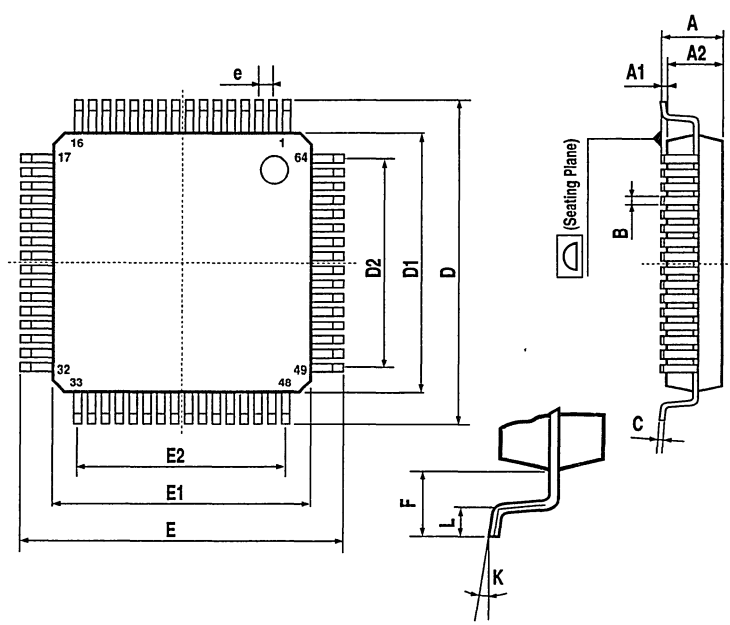
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PQFP64 EPS

PQFP64



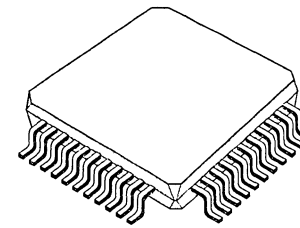
PMPQFP64 EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1		0.25			0.01	
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.35		0.50	0.014		0.020
C			0.17			0.007
D	15.75	16.00	16.25	0.620	0.630	0.640
D1	13.90	14.00	14.10	0.547	0.551	0.555
D2		10.00			0.394	
e		1.00			0.039	
E	15.75	16.00	16.25	0.620	0.630	0.640
E1	13.90	14.00	14.10	0.547	0.551	0.555
E2		10.00			0.394	
F		1.60			0.063	
K	0^o (min.), 7^o (max.)					
L	0.45	0.60	0.75	0.018	0.024	0.030

DTQFP44 TBL

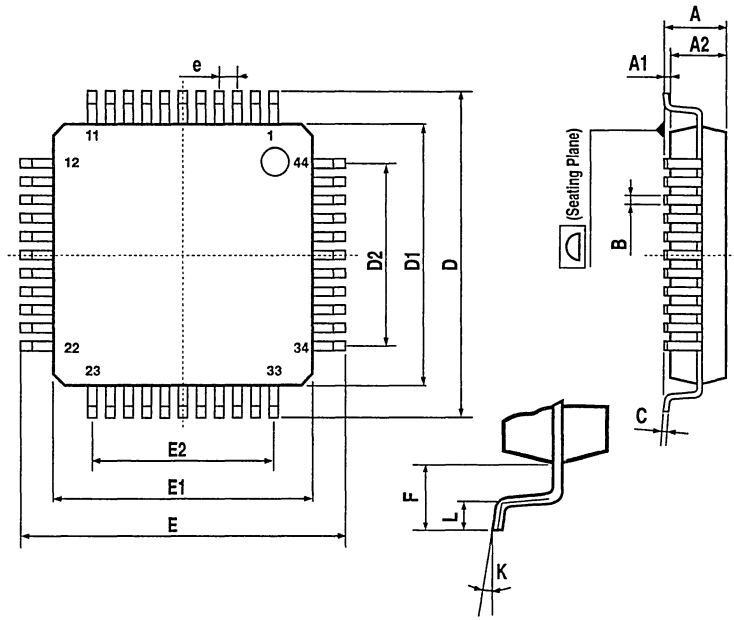
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POFP44 WMF

TQFP44



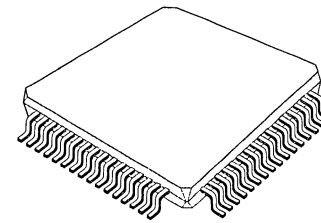
PMPQFP44 EPS

Dim.	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.22	0.32	0.38	0.010	0.012	0.014
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.35			0.486	
e		0.65			0.0314	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.35			0.486	
L	0.45	0.60	0.75	0.020	0.024	0.030
L1		1.00			0.039	
K	0° (min.), 7° (max.)					

DTQFP80 TBL

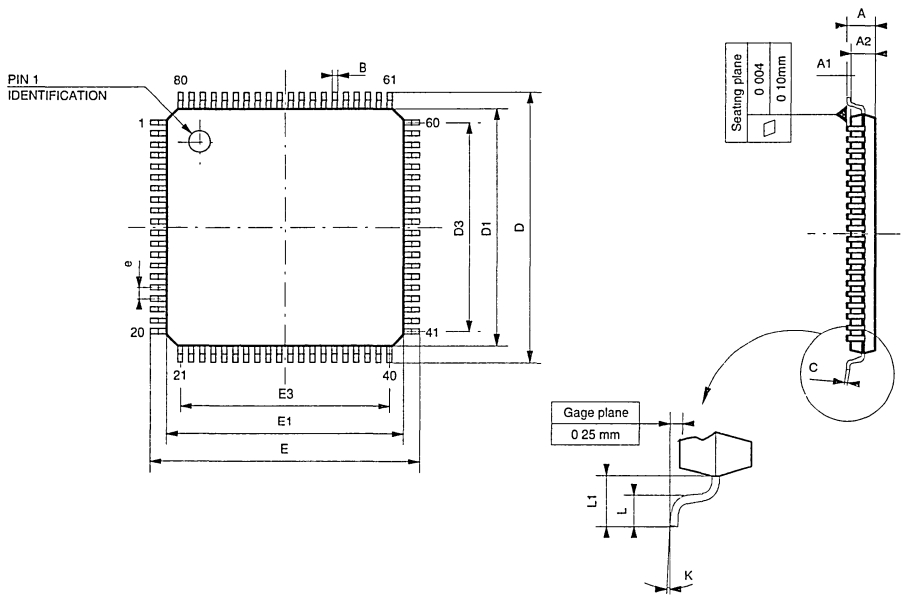
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POFP64 EPS

TQFP80



PMTQFP80 EPS

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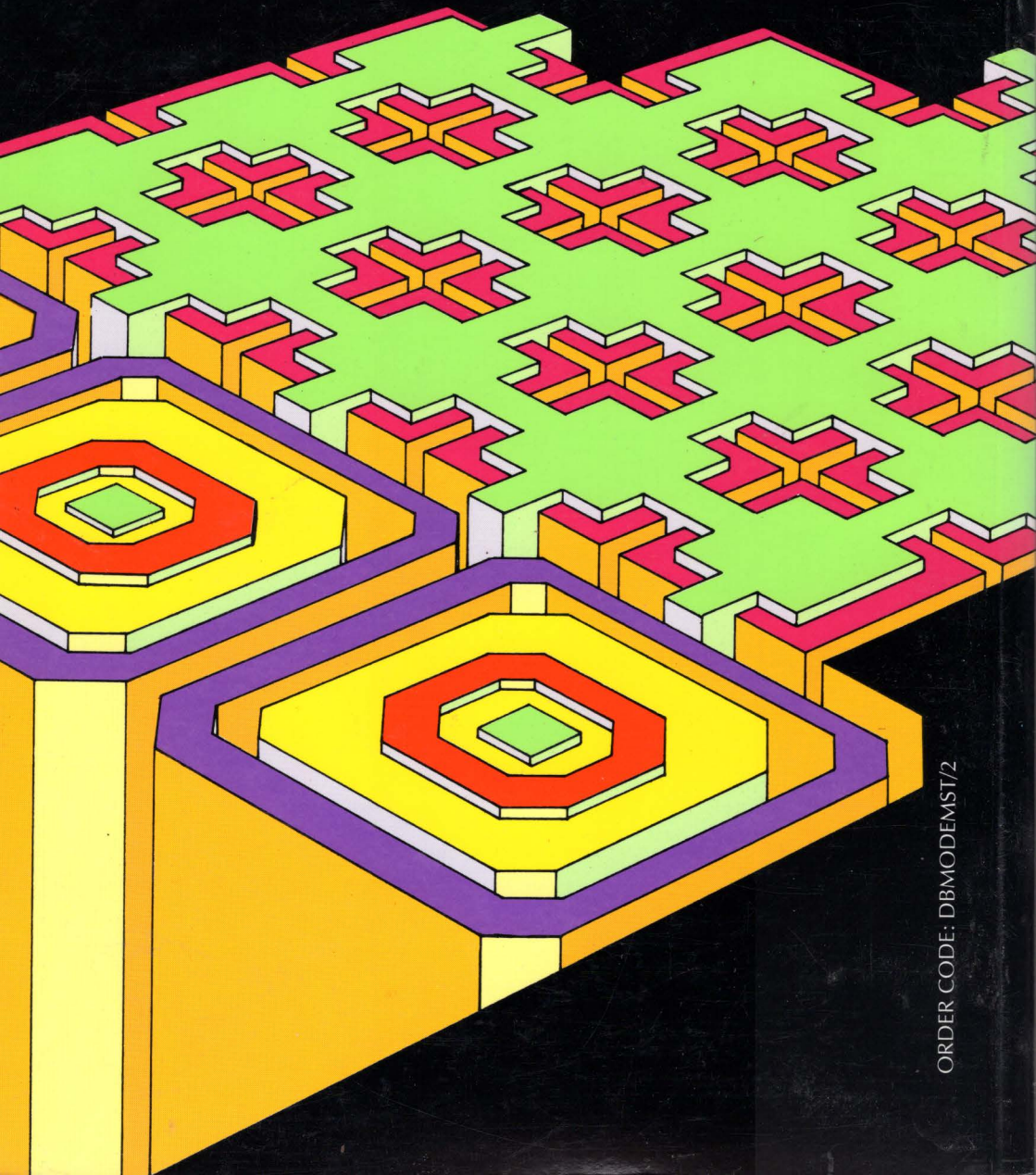

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